AMD Geode™ CS5530A Companion Device Data Book

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Trademarks

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1 AMD Geode™ CS5530A Companion Device

1.1 General Description

The AMD Geode™ CS5530A companion device is designed to work in conjunction with an AMD Geode™ GX1 processor. Together, the Geode GX1 processor and CS5530A companion device provide a system-level solution well suited for the high performance needs of a host of devices which include digital set-top boxes and thin client devices. Due to the low power consumption of the GX1 processor, this solution satisfies the needs of battery powered devices such as AMD's WebPAD system, and thermal design is eased allowing for fanless system design.

The CS5530A is a PCI-to-ISA bridge (South Bridge), ACPI-compliant chipset that provides AT/ISA style functionality. The device contains state-of-the-art power management that enables systems, especially battery powered systems, to significantly reduce power consumption.

Audio is supported through PCI bus master engines that connect to an AC97 compatible codec. If industry standard audio is required, a combination of hardware and software called Virtual System Architecture™ (VSA) technology is provided.

The Geode GX1 processor's graphics/video output is connected to the CS5530A. The CS5530A graphics/video support includes a PLL that generates the DOT clock for the GX1 processor (where the graphics controller is located), video acceleration hardware, gamma RAM plus three DACs for RGB output to CRT, and digital RGB that can be directly connected to TFT panels or NTSC/PAL encoders.

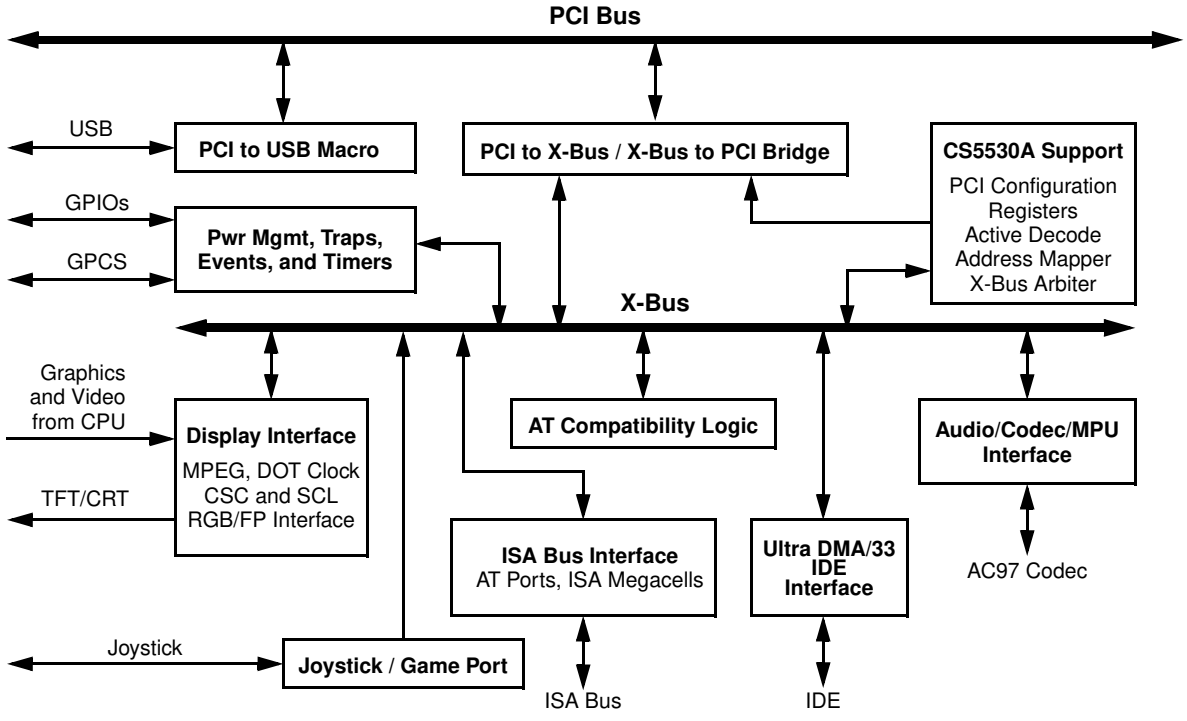


Figure 1-1. Block Diagram

Two bus mastering IDE controllers are included for support of up to four ATA-compliant devices. A two-port Universal Serial Bus (USB) provides high speed, Plug & Play expansion for a variety of consumer peripheral devices such as a keyboard, mouse, printer, and digital camera. If additional functions are required like real-time clock, floppy disk, PS2 keyboard, and PS2 mouse, a SuperI/O device can be easily connected to the CS5530A.

1.2 Features

General Features

- Designed for use with AMD's Geode GX1 processor
- 352 PBGA (Plastic Ball Grid Array) package
- 3.3V or 5.0V PCI bus compatible
- 5.0V tolerant on all inputs
- 3.3V core

PCI-to-ISA Bridge

- PCI 2.1 compliant
- Supports PCI initiator-to-ISA and ISA master-to-PCI cycle translations
- PCI master for audio I/O and IDE controllers
- Subtractive agent for unclaimed transactions
- PCI-to-ISA interrupt mapper/translator

AT Compatibility

- Two 8259A-equivalent interrupt controllers
- 8254-equivalent timer
- Two 8237-equivalent DMA controllers
- Boot ROM and keyboard chip select
- Extended ROM to 16 MB

Bus Mastering IDE Controllers

- Two controllers with support for up to four IDE devices
- Independent timing for master and slave devices for both channels
- PCI bus master burst reads and writes
- Ultra DMA/33 (ATA-4) support
- Multiword DMA support
- Programmed I/O (PIO) Modes 0-4 support

Power Management

- Intelligent system controller supports multiple power management standards:
  - Full ACPI and Legacy (APM) support
  - Directly manages all GX1 processor's power states (including automatic Suspend modulation for optimal performance/thermal balancing)
- I/O traps and idle timers for peripheral power management
- Up to eight GPIOs for system control:
  - All eight are configurable as external wakeup events
- Dedicated inputs for keyboard and mouse wakeup events

XpressAUDIO™ Subsystem

- Provides "back-end" hardware support via six buffered PCI bus masters
- AC97 codec interface:
  - Specification Revision 1.3, 2.0, and 2.1 compliant interface. Note that the codec must have SRC (sample rate conversion) support

Display Subsystem Extensions

- Complements the GX1 processor's graphics and video capabilities:
  - Three independent line buffers for accelerating video data streams
  - Handles asynchronous video and graphics data streams concurrently from the processor
  - YUV to RGB conversion hardware
  - Arbitrary X & Y interpolative scaling
  - Color keying for graphics/video overlay
- VDACs / Display interface:
  - Three integrated DACs
  - Gamma RAM:
    - Provides gamma correction for graphics data streams
    - Provides brightness/contrast correction for video data streams
  - Integrated DOT clock generator
  - Digital RGB interface drives TFT panels or standard NTSC/PAL encoders
  - Up to 1280x1024 @ 85 Hz

Universal Serial Bus

- Two independent USB interfaces:
  - Open Host Controller Interface (OpenHCI) specification compliant
  - Second generation proven core design

2 Architecture Overview

The Geode CS5530A can be described as providing the functional blocks as shown in Figure 1-1 on page 11.

- Processor support
- PCI bus master/slave interface
- ISA bus interface
- AT compatibility logic
- IDE controllers
- Power management:
  — GPIO interfaces
  — Traps, Events, Timers
- Joystick/Game port interface
- Virtual audio support hardware
- Video display, which includes MPEG accelerator, RAMDAC, and video ports
- USB controller

2.1 Processor Support

The traditional south bridge functionality included in the CS5530A companion device has been designed to support the GX1processor. When combined with a GX1 processor, the CS5530A provides a bridge which supports a standard ISA bus and system ROM. As part of the video subsystem, the CS5530A provides MPEG video acceleration and a digital RGB interface, to allow direct connection to TFT LCD panels. This chip also integrates a gamma RAM and three DACs, allowing for direct connection of a CRT monitor. Figure 2-1 shows a typical system block diagram.

For detailed information regarding processor signal connections refer to Section 4.1 "Processor Interface" on page 48.

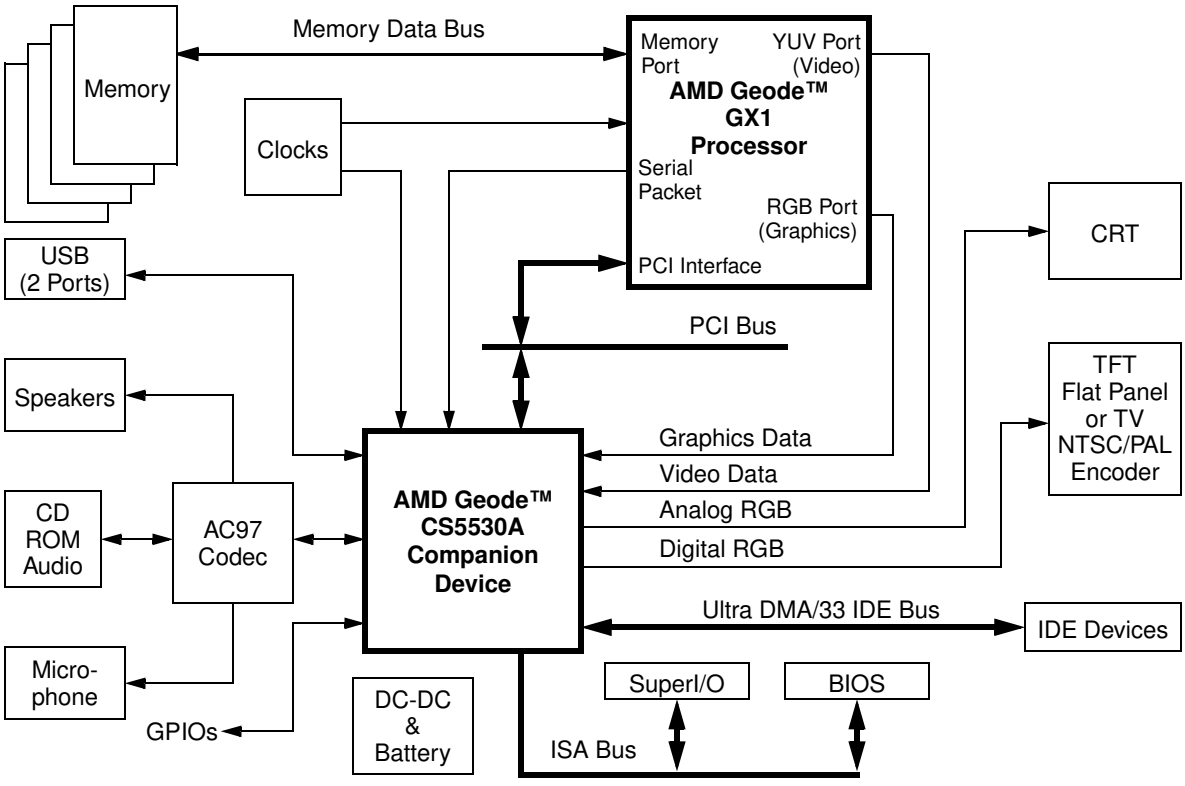


Figure 2-1. Example System Block Diagram

2.2 PCI Bus Interface

The CS5530A provides a PCI bus interface that is both a slave for PCI cycles initiated by the CPU or other PCI master devices, and a non-preemptable master for DMA transfer cycles. The chip also is a standard PCI master for the IDE controllers and audio I/O logic. The CS5530A supports positive decode for configurable memory and I/O regions and implements a subtractive decode option for unclaimed PCI accesses. The CS5530A also generates address and data parity and performs parity checking. The CS5530A does not include the PCI bus arbiter, which is located in the processor.

Configuration registers are accessed through the PCI interface using the PCI Bus Type 1 configuration mechanism as described in the PCI 2.1 Specification.

2.3 ISA Bus Interface

The CS5530A provides an ISA bus interface for unclaimed memory and I/O cycles on PCI. The CS5530A is the default subtractive decoding agent and forwards all unclaimed memory and I/O cycles to the ISA interface; however, the CS5530A may be configured to ignore either I/O, memory, or all unclaimed cycles (subtractive decode disabled).

The CS5530A supports two modes on the ISA interface. The default mode, Limited ISA Mode, supports the full memory and I/O address range without ISA mastering. The address and data buses are multiplexed together, requiring an external latch to latch the lower 16 bits of address of the ISA cycle. The signal SA_LATCH is generated when the data on the SA/SD bus is a valid address. Additionally, the upper four address bits, SA[23:20], are multiplexed on GPIO[7:4].

The second mode, ISA Master Mode, supports ISA bus masters and requires no external circuitry. When the CS5530A is placed in ISA Master Mode, a large number of pins are redefined. In this mode, the CS5530A cannot support TFT flat panels or TV controllers since most of the signals used to support these functions have been redefined. This mode is required if ISA slots or ISA masters are used. ISA master cycles are only passed to the PCI bus if they access memory. I/O accesses are left to complete on the ISA bus.

For further information regarding mode selection and operational details refer to Section 4.5.2.2 "Limited ISA and ISA Master Modes" on page 92.

2.4 AT Compatibility Logic

The CS5530A integrates:

- Two 8237-equivalent DMA controllers with full 32-bit addressing
- Two 8259-equivalent interrupt controllers providing 13 individually programmable external interrupts
- An 8254-equivalent timer for refresh, timer, and speaker logic
- NMI control and generation for PCI system errors and all parity errors
- Support for standard AT keyboard controllers
- Positive decode for the AT I/O register space
- Reset control

2.4.1 DMA Controller

The CS5530A supports the industry standard DMA architecture using two 8237-compatible DMA controllers in cascaded configuration. CS5530A-supported DMA functions include:

- Standard seven-channel DMA support
- 32-bit address range support via high page registers
- IOCHRDY extended cycles for compatible timing transfers
- ISA bus master device support using cascade mode

2.4.2 Programmable Interval Timer

The CS5530A contains an 8254-equivalent programmable interval timer. This device has three timers, each with an input frequency of 1.193 MHz.

2.4.3 Programmable Interrupt Controller

The CS5530A contains two 8259-equivalent programmable interrupt controllers (PICs), with eight interrupt request lines each, for a total of 16 interrupts. The two controllers are cascaded internally, and two of the interrupt request inputs are connected to the internal circuitry. This allows a total of 13 externally available interrupt requests.

Each CS5530A IRQ signal can be individually selected as edge- or level-sensitive. The PCI interrupt signals are routed internally to the PICs IRQs.

2.5 IDE Controllers

The CS5530A integrates two PCI bus mastering, ATA-4 compatible IDE controllers. These controllers support Ultra DMA/33 (enabled in Microsoft® Windows 95 and Windows NT® by using a driver provided by AMD), Multiword DMA, and Programmed I/O (PIO) modes. Two devices are supported on each controller. The data-transfer speed for each device on each controller can be independently programmed. This allows high-speed IDE peripherals to coexist on the same channel as lower speed devices. Faster devices must be ATA-4 compatible.

2.6 Power Management

The CS5530A integrates advanced power management features including:

- Idle timers for common system peripherals
- Address trap registers for programmable address ranges for I/O or memory accesses
- Up to eight programmable GPIOs
- Clock throttling with automatic speedup for the CPU clock
- Software CPU stop clock
- Save-to-Disk/RAM with peripheral shadow registers
- Dedicated serial bus to/from the GX1 processor providing CPU power management status

The CS5530A is an ACPI (Advanced Control and Power Interface) compliant chipset. An ACPI compliant system is one whose underlying BIOS, device drivers, chipset and peripherals conform to revision 1.0 or newer of the ACPI specification. The “Fixed Feature” and “General Purpose” registers are virtual. They are emulated by the SMI handling code rather than existing in physical hardware. To the ACPI compliant operating system, the SMI-base virtualization is transparent; however, to eliminate unnecessary latencies, the ACPI timer exists in physical hardware.

The CS5530A V-ACPI (Virtual ACPI) solution provides the following support:

- CPU States — C1, C2
- Sleep States — S1, S2, S4, S4BIOS, S5
- Embedded Controller (Optional) — SCI and SWI event inputs.
- General Purpose Events — Fully programmable GPE0 Event Block registers.

2.6.1 GPIO Interface

Eight GPIO pins are provided for general usage in the system. GPIO[3:0] are dedicated pins and can be configured as inputs or outputs. GPIO[7:4] can be configured as the upper addresses of the ISA bus, SA[23:20]. All GPIOs can also be configured to generate an SMI on input edge transitions.

2.7 XpressAUDIO™ Subsystem

XpressAUDIO™ architecture in the CS5530A offers a combined hardware/software support solution to meet industry standard audio requirements. XpressAUDIO architecture uses VSA technology along with additional hardware features to provide the necessary support for industry standard 16-bit stereo synthesis and OPL3 emulation.

The hardware portion of the XpressAUDIO subsystem can broadly be divided into two categories. Hardware for:

- Transporting streaming audio data to/from the system memory and an AC97 codec.
- VSA technology support.

2.7.1 AC97 Codec Interface

The CS5530A provides an AC97 Specification Revision 1.3, 2.0, and 2.1 compatible interface. Any AC97 codec which supports an independent input and output sample rate conversion interface can be used with the CS5530A. This type of codec allows for a design which meets the requirements for PC97 and PC98-compliant audio as defined by Microsoft Corporation. Figure 2-2 shows the codec and CS5530A signal connections. For specifics on the serial interface, refer to the appropriate codec manufacturer’s data sheet.

Low latency audio I/O is accomplished by a buffered PCI bus mastering controller.

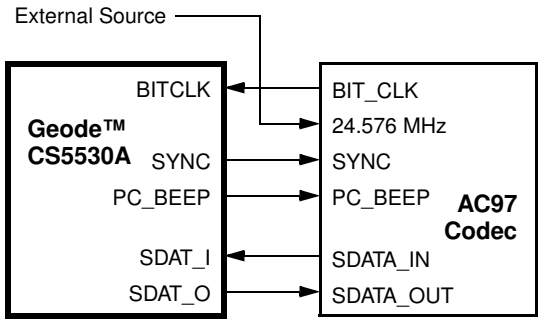


Figure 2-2. AC97 Codec Signal Connections

2.7.2 VSA Technology Support Hardware

The CS5530A companion device incorporates the required hardware in order to support VSA technology for the capture and playback of audio using an external codec. This eliminates much of the hardware traditionally associated with industry standard audio functions.

XpressAUDIO software provides 16-bit compatible sound. This software is available to OEMs for incorporation into the system BIOS ROM.

2.8 Display Subsystem Extensions

The CS5530A incorporates extensions to the GX1 processor's display subsystem. These include:

- Video Accelerator
  - — Buffers and formats input YUV video data from the processor
  - — 8-bit interface to the processor
  - — X & Y scaler with bilinear filter
  - — Color space converter (YUV to RGB)
- Video Overlay Logic
  - — Color key
  - — Data switch for graphics and video data
- Gamma RAM
  - — Brightness and contrast control
- Display Interface
  - — Integrated RGB Video DACs
  - — VESA DDC2B/DPMS support
  - — Flat panel interface

Figure 2-3 shows the data path of the display subsystem extensions.

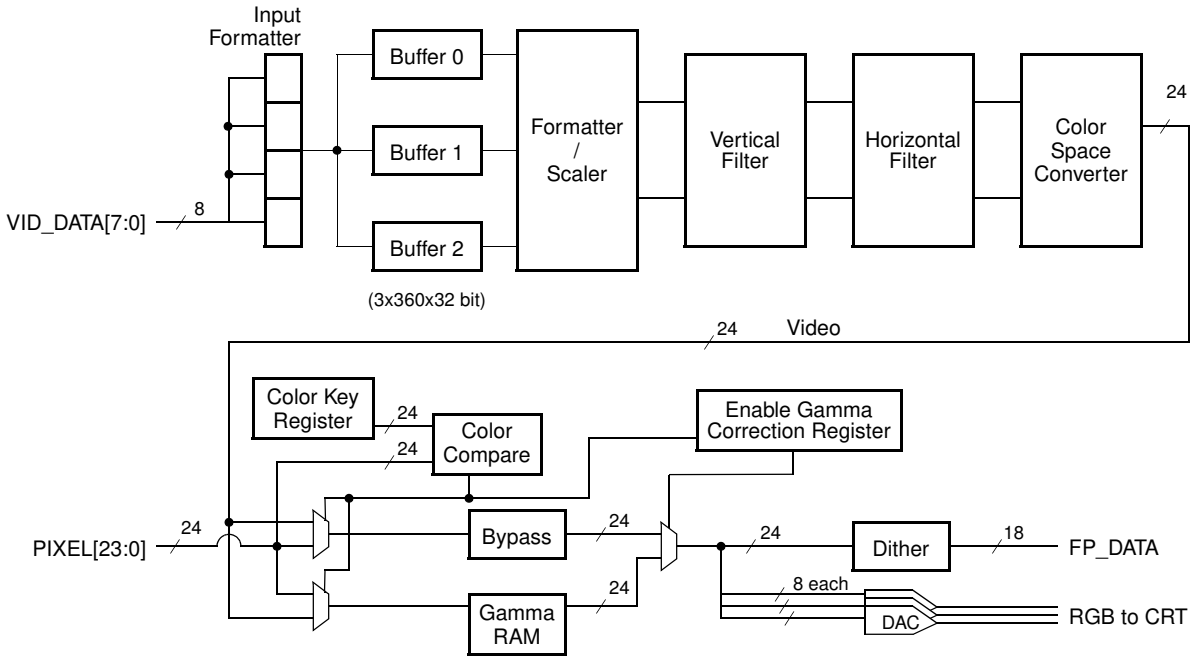


Figure 2-3. 8-Bit Display Subsystem Extensions

2.9 Clock Generation

In a CS5530A/GX1 processor based system, the CS5530A generates only the video DOT clock (DCLK) for the CPU and the ISA clock. All other clocks are generated by an external clock chip.

The ISACLK is created by dividing the PCICLK. For ISA compatibility, the ISACLK nominally runs at 8.33 MHz or less. The ISACLK dividers are programmed via F0 Index 50h[2:0].

DCLK is generated from the 14.31818 MHz input (CLK_14MHZ). A combination of a phase locked loop (PLL), linear feedback shift register (LFSR) and divisors are used to generate the desired frequencies for the DCLK. The divisors and LFSR are configurable through the F4BAR+Memory Offset 24h. For applications that do not use the GX1 processor's graphics subsystem, this is an available clock for general purpose use.

Figure 2-4 shows a block diagram for clock generation within the CS5530A.

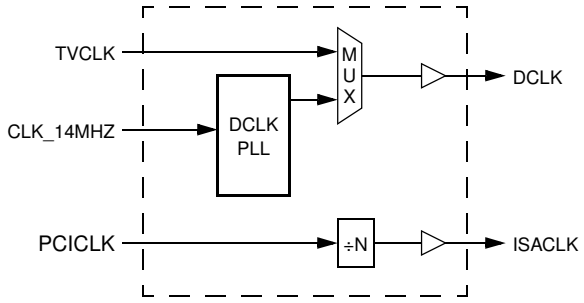


Figure 2-4. CS5530A Clock Generation

2.10 Universal Serial Bus

The CS5530A provides two complete, independent USB ports. Each port has a Data "–" and a Data "+" pin.

The USB controller is a compliant Open Host Controller Interface (OpenHCI). The OpenHCI specification provides a register-level description for a host controller, as well as a common industry hardware/software interface and drivers (see OpenHCI Specification, Revision 1.0, for description).

3 Signal Definitions

This section defines the signals and describes the external interface of the Geode CS5530A. Figure 3-1 shows the pins organized by their functional groupings (internal test and electrical pins are not shown).

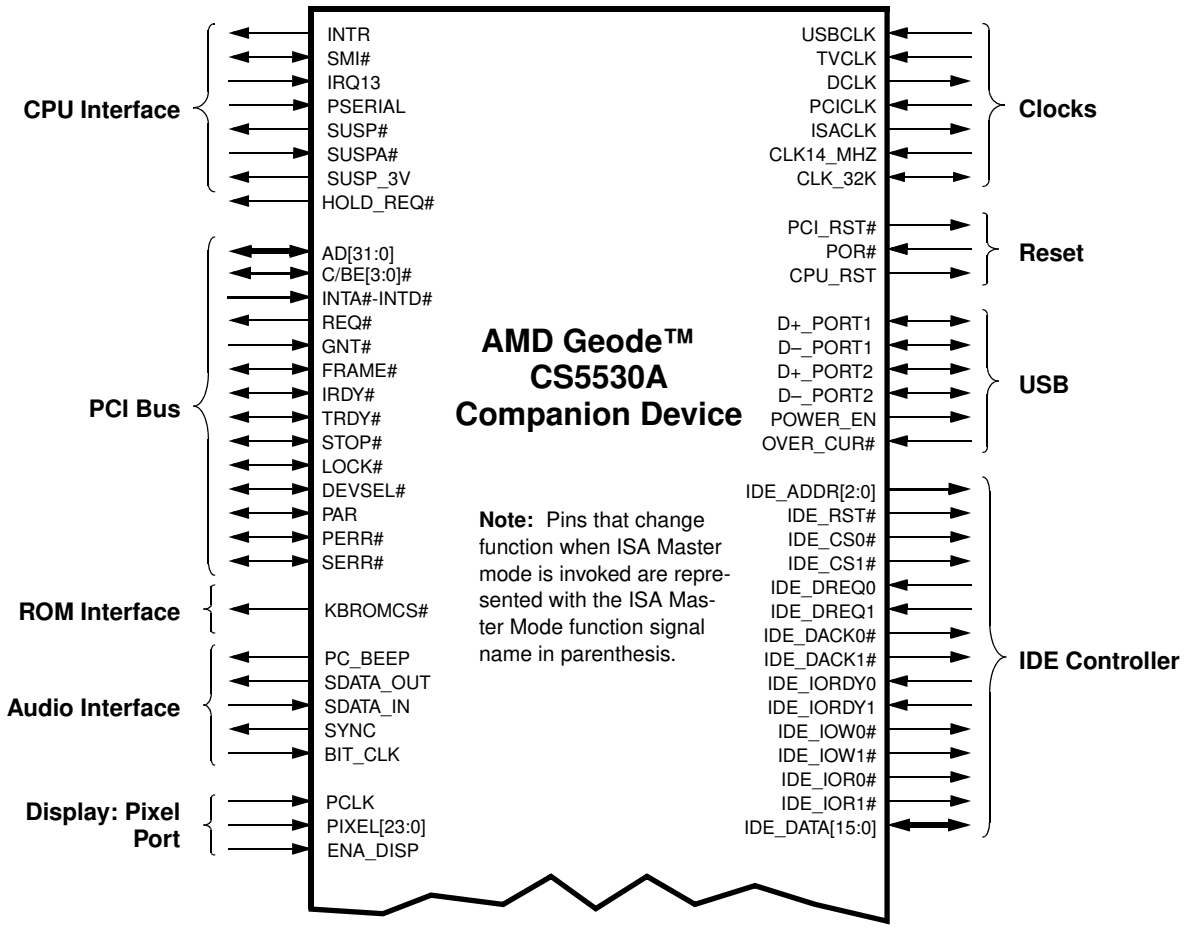


Figure 3-1. CS5530A Signal Groups

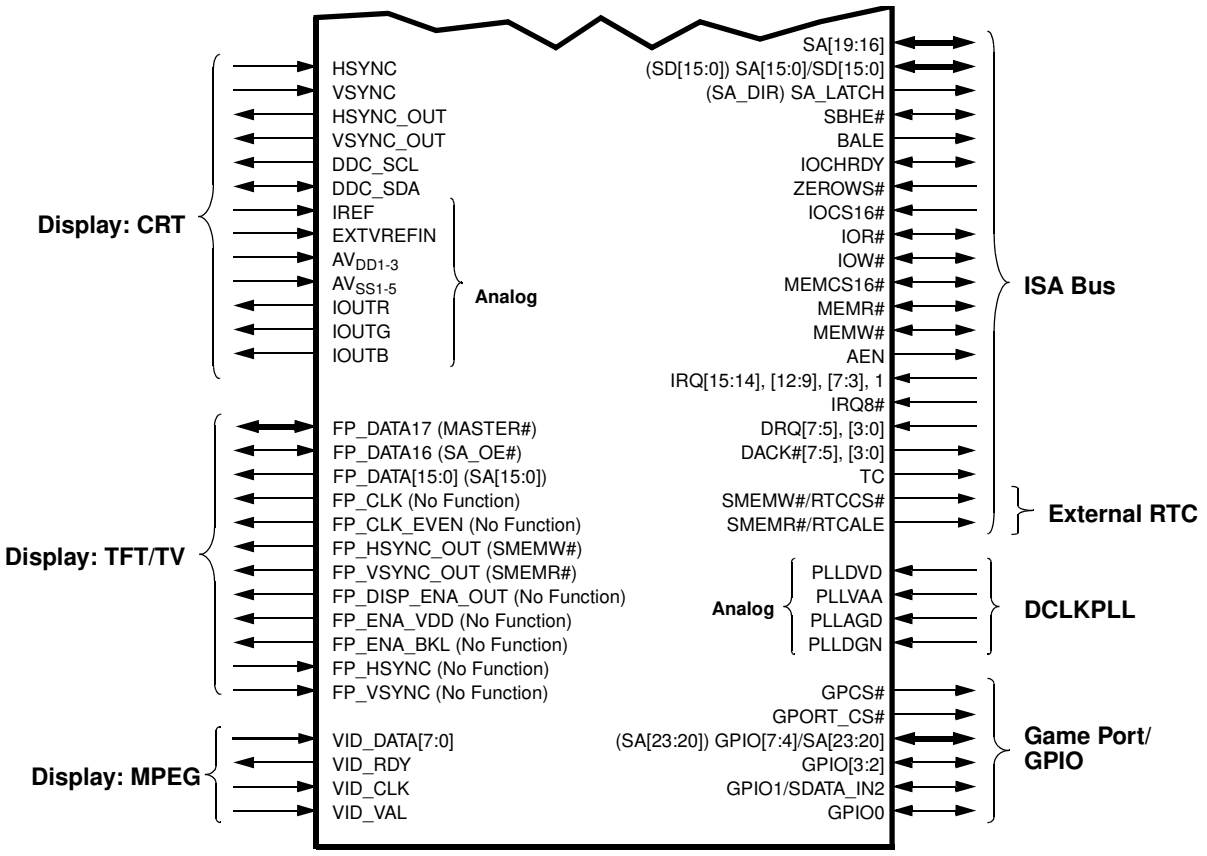


Figure 3-1. CS5530A Signal Groups (Continued)

3.1 Pin Assignments

The tables in this section use several common abbreviations. Table 3-1 lists the mnemonics and their meanings.

Figure 3-2 shows the pin assignment for the CS5530A with Tables 3-2 and 3-3 listing the pin assignments sorted by pin number and alphabetically by signal name, respectively.

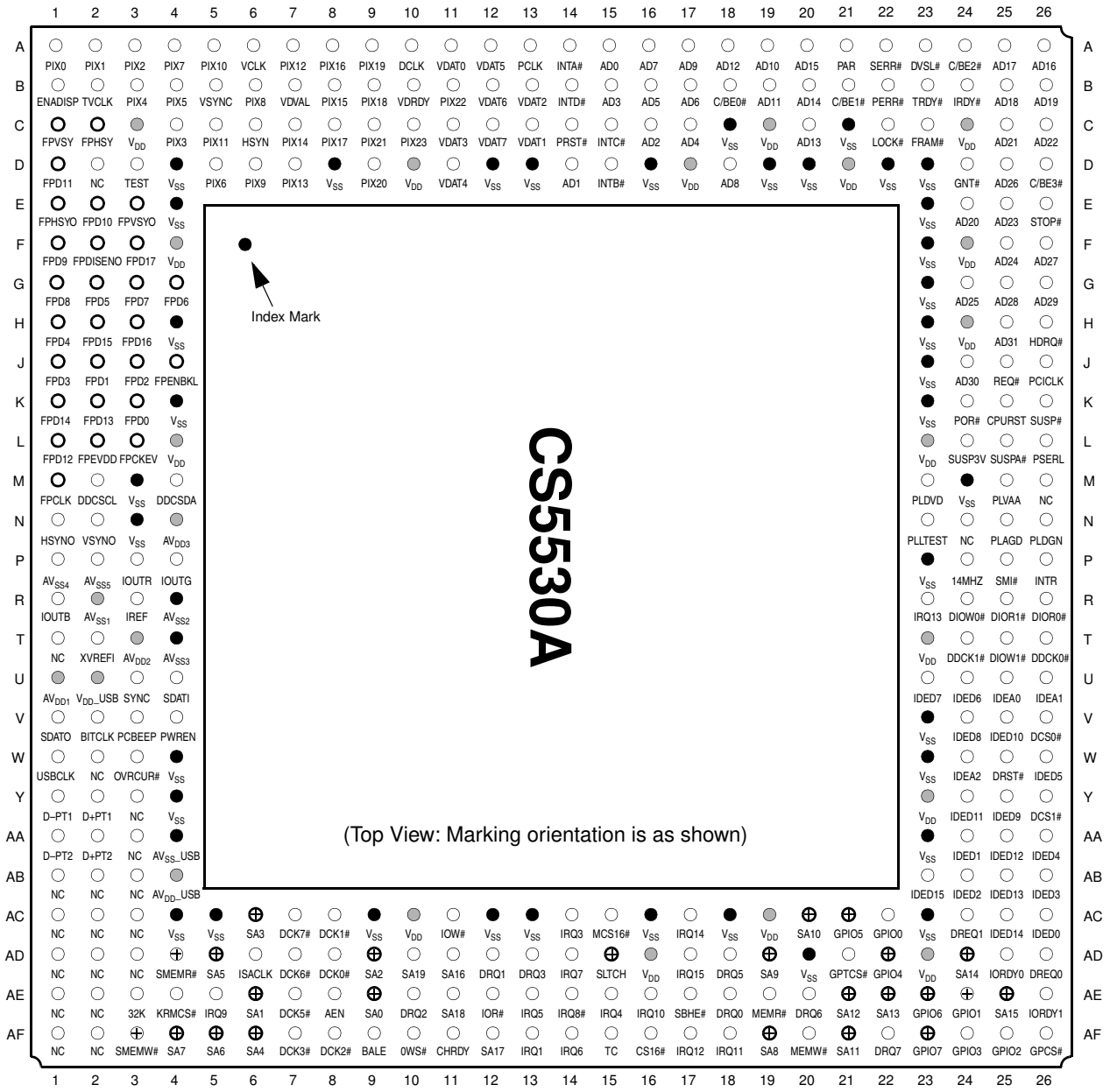
In Section 3.2 "Signal Descriptions" on page 29 a description of each signal within its associated functional group is provided.

In the signal definitions, references to F0-F4, F1BAR, F2BAR, F3BAR, F4BAR, and PCIUSB are made. These terms relate to designated register spaces. Refer to Table 5-1 "PCI Configuration Address Register (0CF8h)" on page 144 for details regarding these register spaces and their access mechanisms.

Table 3-1. Pin Type Definitions

Mnemonic	Definition
I	Input pin[1]
I/O	Bidirectional pin[1,2]
O	Output pin[1, 2]
OD	Open-drain output structure that allows multiple devices to share the pin in a wired-OR configuration
PU	Pull-up resistor
SMT	Schmitt Trigger
VDD (PWR)	Power pin
VSS (GND)	Ground pin
#	The “#” symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When “#” is not present after the signal name, the signal is asserted when at a high voltage level.

1. All buffers are 5 volt tolerant.
2. All digital bidirectional and output pins can be TRI-STATE signals unless a weak pull-up is enabled.



Note: Signal names have been abbreviated in this figure due to space constraints.

● = GND terminal ⊕ = Multiplexed signal
○ = PWR terminal O = Changes function in ISA Master Mode

Figure 3-2. 352 PBGA Pin Assignment Diagram
Order Number: CS5530A-UCE

Table 3-2. 352 PBGA Pin Assignments - Sorted by Pin Number

Pin No.	Signal Name	
	Limited ISA Mode	ISA Master Mode
A1	PIXEL0	
A2	PIXEL1	
A3	PIXEL2	
A4	PIXEL7	
A5	PIXEL10	
A6	VID_CLK	
A7	PIXEL12	
A8	PIXEL16	
A9	PIXEL19	
A10	DCLK	
A11	VID_DATA0	
A12	VID_DATA5	
A13	PCLK	
A14	INTA#	
A15	AD0	
A16	AD7	
A17	AD9	
A18	AD12	
A19	AD10	
A20	AD15	
A21	PAR	
A22	SERR#	
A23	DEVSEL#	
A24	C/BE2#	
A25	AD17	
A26	AD16	
B1	ENA_DISP	
B2	TVCLK	
B3	PIXEL4	
B4	PIXEL5	
B5	VSYNC	
B6	PIXEL8	
B7	VID_VAL	
B8	PIXEL15	
B9	PIXEL18	
B10	VID_RDY	
B11	PIXEL22	
B12	VID_DATA6	
B13	VID_DATA2	
B14	INTD#	
B15	AD3	
B16	AD5	
B17	AD6	
B18	C/BE0#	
B19	AD11	
B20	AD14	
B21	C/BE1#	
B22	PERR#	
B23	TRDY#	
B24	IRDY#	
B25	AD18	
B26	AD19	
C1	FP_VSYNC	No Function
C2	FP_HSYNC	No Function
C3	V_{DD}	
C4	PIXEL3	
C5	PIXEL11	
C6	HSYNC	
C7	PIXEL14	
C8	PIXEL17	
C9	PIXEL21	
C10	PIXEL23	
C11	VID_DATA3	
C12	VID_DATA7	
C13	VID_DATA1	
C14	PCI_RST#	
C15	INTC#	
C16	AD2	
C17	AD4	
C18	V_{SS}	
C19	V_{DD}	
C20	AD13	
C21	V_{SS}	
C22	LOCK#	
C23	FRAME#	
C24	V_{DD}	
C25	AD21	
C26	AD22	
D1	FP_DATA11	SA11
D2	NC	
D3	TEST	
D4	V_{SS}	
D5	PIXEL6	
D6	PIXEL9	
D7	PIXEL13	
D8	V_{SS}	
D9	PIXEL20	
D10	V_{DD}	
D11	VID_DATA4	
D12	V_{SS}	
D13	V_{SS}	
D14	AD1	
D15	INTB#	
D16	V_{SS}	
D17	V_{DD}	
D18	AD8	
D19	V_{SS}	
D20	V_{SS}	
D21	V_{DD}	
D22	V_{SS}	
D23	V_{SS}	
D24	GNT#	
D25	AD26	
D26	C/BE3#	
E1	FP_HSYNC_OUT	SMEMW#
E2	FP_DATA10	SA10
E3	FP_VSYNC_OUT	SMEMR#
E4	V_{SS}	
E23	V_{SS}	
E24	AD20	
E25	AD23	
E26	STOP#	
F1	FP_DATA9	SA9
F2	FP_DISP_ENA_OUT	No Function
F3	FP_DATA17	MASTER#
F4	V_{DD}	
F23	V_{SS}	
F24	V_{DD}	
F25	AD24	
F26	AD27	
G1	FP_DATA8	SA8
G2	FP_DATA5	SA5
G3	FP_DATA7	SA7
G4	FP_DATA6	SA6
G23	V_{SS}	
G24	AD25	
G25	AD28	
G26	AD29	
H1	FP_DATA4	SA4
H2	FP_DATA15	SA15
H3	FP_DATA16	SA_OE#
H4	V_{SS}	
H23	V_{SS}	
H24	V_{DD}	
H25	AD31	
H26	HOLD_REQ#	
J1	FP_DATA3	SA3
J2	FP_DATA1	SA1
J3	FP_DATA2	SA2
J4	FP_ENA_BKL	No Function
J23	V_{SS}	
J24	AD30	
J25	REQ#	
J26	PCICLK	
K1	FP_DATA14	SA14
K2	FP_DATA13	SA13
K3	FP_DATA0	SA0
K4	V_{SS}	
K23	V_{SS}	
K24	POR#	
K25	CPU_RST	
K26	SUSP#	
L1	FP_DATA12	SA12

Table 3-2. 352 PBGA Pin Assignments - Sorted by Pin Number (Continued)

Pin No.	Signal Name	
	Limited ISA Mode	ISA Master Mode
L2	FP_ENA_VDD	No Function
L3	FP_CLK_EVEN	No Function
L4	V_{DD}	
L23	V_{DD}	
L24	SUSP_3V	
L25	SUSPA#	
L26	PSERIAL	
M1	FP_CLK	No Function
M2	DDC_SCL	
M3	V_{SS}	
M4	DDC_SDA	
M23	PLLDVD	
M24	V_{SS}	
M25	PLLVAA	
M26	NC	
N1	HSYNC_OUT	
N2	VSYNC_OUT	
N3	V_{SS}	
N4	AV_{DD3} (DAC)	
N23	PLLTEST	
N24	NC	
N25	PLLAGD	
N26	PLLDGN	
P1	AV_{SS4} (ICAP)	
P2	AV_{SS5} (DAC)	
P3	IOUTR	
P4	IOUTG	
P23	V_{SS}	
P24	CLK_14MHZ	
P25	SMI#	
P26	INTR	
R1	IOUTB	
R2	AV_{SS1} (DAC)	
R3	IREF	
R4	AV_{SS2} (ICAP)	
R23	IRQ13	
R24	IDE_IOW0#	
R25	IDE_IOR1#	
R26	IDE_IOR0#	
T1	NC	
T2	EXTVREFIN	
T3	AV_{DD2} (VREF)	
T4	AV_{SS3} (VREF)	
T23	V_{DD}	
T24	IDE_DACK1#	
T25	IDE_IOW1#	
T26	IDE_DACK0#	
U1	AV_{DD1} (DAC)	
U2	V_{DD}_USB	
U3	SYNC	
U4	SDATA_IN	

Pin No.	Signal Name	
	Limited ISA Mode	ISA Master Mode
U23	IDE_DATA7	
U24	IDE_DATA6	
U25	IDE_ADDR0	
U26	IDE_ADDR1	
V1	SDATA_OUT	
V2	BIT_CLK	
V3	PC_BEEP	
V4	POWER_EN	
V23	V_{SS}	
V24	IDE_DATA8	
V25	IDE_DATA10	
V26	IDE_CS0#	
W1	USBCLK	
W2	NC	
W3	OVER_CUR#	
W4	V_{SS}	
W23	V_{SS}	
W24	IDE_ADDR2	
W25	IDE_RST#	
W26	IDE_DATA5	
Y1	D–_PORT1	
Y2	D+_PORT1	
Y3	NC	
Y4	V_{SS}	
Y23	V_{DD}	
Y24	IDE_DATA11	
Y25	IDE_DATA9	
Y26	IDE_CS1#	
AA1	D–_PORT2	
AA2	D+_PORT2	
AA3	NC	
AA4	AV_{SS}_USB	
AA23	V_{SS}	
AA24	IDE_DATA1	
AA25	IDE_DATA12	
AA26	IDE_DATA4	
AB1	NC	
AB2	NC	
AB3	NC	
AB4	AV_{DD}_USB	
AB23	IDE_DATA15	
AB24	IDE_DATA2	
AB25	IDE_DATA13	
AB26	IDE_DATA3	
AC1	NC	
AC2	NC	
AC3	NC	
AC4	V_{SS}	
AC5	V_{SS}	
AC6	SA3/SD3	SD3
AC7	DACK7#	

Pin No.	Signal Name	
	Limited ISA Mode	ISA Master Mode
AC8	DACK1#	
AC9	V_{SS}	
AC10	V_{DD}	
AC11	IOW#	
AC12	V_{SS}	
AC13	V_{SS}	
AC14	IRQ3	
AC15	MEMCS16#	
AC16	V_{SS}	
AC17	IRQ14	
AC18	V_{SS}	
AC19	V_{DD}	
AC20	SA10/SD10	SD10
AC21	GPIO5/SA21	SA21
AC22	GPIO0	
AC23	V_{SS}	
AC24	IDE_DREQ1	
AC25	IDE_DATA14	
AC26	IDE_DATA0	
AD1	NC	
AD2	NC	
AD3	NC	
AD4	SMEMR#/RTCALE	
AD5	SA5/SD5	SD5
AD6	ISACLK	
AD7	DACK6#	
AD8	DACK0#	
AD9	SA2/SD2	SD2
AD10	SA19	
AD11	SA16	
AD12	DRQ1	
AD13	DRQ3	
AD14	IRQ7	
AD15	SA_LATCH	SA_DIR
AD16	V_{DD}	
AD17	IRQ15	
AD18	DRQ5	
AD19	SA9/SD9	SD9
AD20	V_{SS}	
AD21	GPORT_CS#	
AD22	GPIO4/SA20	SA20
AD23	V_{DD}	
AD24	SA14/SD14	SD14
AD25	IDE_IORDY0	
AD26	IDE_DREQ0	
AE1	NC	
AE2	NC	
AE3	CLK_32K	
AE4	KBROMCS#	
AE5	IRQ9	
AE6	SA1/SD1	SD1

Table 3-2. 352 PBGA Pin Assignments - Sorted by Pin Number (Continued)

Pin No.	Signal Name	
	Limited ISA Mode	ISA Master Mode
AE7	DACK5#	
AE8	AEN	
AE9	SA0/SD0	SD0
AE10	DRQ2	
AE11	SA18	
AE12	IOR#	
AE13	IRQ5	
AE14	IRQ8#	
AE15	IRQ4	
AE16	IRQ10	
AE17	SBHE#	
AE18	DRQ0	
AE19	MEMR#	
AE20	DRQ6	
AE21	SA12/SD12	SD12
AE22	SA13/SD13	SD13
AE23	GPIO6/SA22	SD22
AE24	GPIO1/SDATA_IN2	
AE25	SA15/SD15	SD15
AE26	IDE_IORDY1	
AF1	NC	
AF2	NC	
AF3	SMEMW#/RTCCS#	
AF4	SA7/SD7	SD7
AF5	SA6/SD6	SD6
AF6	SA4/SD4	SD4
AF7	DACK3#	
AF8	DACK2#	
AF9	BALE	
AF10	ZEROWS#	
AF11	IOCHRDY	
AF12	SA17	
AF13	IRQ1	
AF14	IRQ6	
AF15	TC	
AF16	IOCS16#	
AF17	IRQ12	
AF18	IRQ11	
AF19	SA8/SD8	SD8
AF20	MEMW#	
AF21	SA11/SD11	SD11
AF22	DRQ7	
AF23	GPIO7/SA23	SA23
AF24	GPIO3	
AF25	GPIO2	
AF26	GPCS#	

Table 3-3. 352 PBGA Pin Assignments - Sorted Alphabetically by Signal Name

Signal Name		Pin Type[1]	Buffer Type[2]	Pin No.
Limited ISA Mode	ISA Master Mode			
AD0		I/O	PCI	A15
AD1		I/O	PCI	D14
AD2		I/O	PCI	C16
AD3		I/O	PCI	B15
AD4		I/O	PCI	C17
AD5		I/O	PCI	B16
AD6		I/O	PCI	B17
AD7		I/O	PCI	A16
AD8		I/O	PCI	D18
AD9		I/O	PCI	A17
AD10		I/O	PCI	A19
AD11		I/O	PCI	B19
AD12		I/O	PCI	A18
AD13		I/O	PCI	C20
AD14		I/O	PCI	B20
AD15		I/O	PCI	A20
AD16		I/O	PCI	A26
AD17		I/O	PCI	A25
AD18		I/O	PCI	B25
AD19		I/O	PCI	B26
AD20		I/O	PCI	E24
AD21		I/O	PCI	C25
AD22		I/O	PCI	C26
AD23		I/O	PCI	E25
AD24		I/O	PCI	F25
AD25		I/O	PCI	G24
AD26		I/O	PCI	D25
AD27		I/O	PCI	F26
AD28		I/O	PCI	G25
AD29		I/O	PCI	G26
AD30		I/O	PCI	J24
AD31		I/O	PCI	H25
AEN		O	8 mA	AE8
AV_{DD1} (DAC)		I, Analog	--	U1
AV_{DD2} (VREF)		I, Analog	--	T3
AV_{DD3} (DAC)		I, Analog	--	N4
AV_{DD}_USB		PWR	--	AB4
AV_{SS1} (DAC)		I, Analog	--	R2
AV_{SS2} (ICAP)		I, Analog	--	R4
AV_{SS3} (VREF)		I, Analog	--	T4
AV_{SS4} (ICAP)		I, Analog	--	P1
AV_{SS5} (DAC)		I, Analog	--	P2
AV_{SS}_USB		GND	--	AA4
BALE		O	8 mA	AF9
BIT_CLK		I	8 mA	V2
C/BE0#		I/O	PCI	B18
C/BE1#		I/O	PCI	B21
C/BE2#		I/O	PCI	A24
C/BE3#		I/O	PCI	D26
CLK_14MHZ		I (SMT)	CLK	P24
CLK_32K		I/O	8 mA	AE3
CPU_RST		O	8 mA	K25

Signal Name		Pin Type[1]	Buffer Type[2]	Pin No.
Limited ISA Mode	ISA Master Mode			
DACK0#		O	8 mA	AD8
DACK1#		O	8 mA	AC8
DACK2#		O	8 mA	AF8
DACK3#		O	8 mA	AF7
DACK5#		O	8 mA	AE7
DACK6#		O	8 mA	AD7
DACK7#		O	8 mA	AC7
DCLK		O	DOTCLK	A10
DDC_SCL		O	8 mA	M2
DDC_SDA		I/O	8 mA	M4
DEVSEL#		I/O	PCI	A23
D–_PORT1		I/O	USB	Y1
D+_PORT1		I/O	USB	Y2
D–_PORT2		I/O	USB	AA1
D+_PORT2		I/O	USB	AA2
DRQ0		I	8 mA	AE18
DRQ1		I	8 mA	AD12
DRQ2		I	8 mA	AE10
DRQ3		I	8 mA	AD13
DRQ5		I	8 mA	AD18
DRQ6		I	8 mA	AE20
DRQ7		I	8 mA	AF22
ENA_DISP		I	8 mA	B1
EXTVREFIN		I, Analog	--	T2
FP_CLK	No Function	O	FP_CLK	M1
FP_CLK_EVEN	No Function	O	8 mA	L3
FP_DATA0	SA0	I/O	8 mA	K3
FP_DATA1	SA1	I/O	8 mA	J2
FP_DATA2	SA2	I/O	8 mA	J3
FP_DATA3	SA3	I/O	8 mA	J1
FP_DATA4	SA4	I/O	8 mA	H1
FP_DATA5	SA5	I/O	8 mA	G2
FP_DATA6	SA6	I/O	8 mA	G4
FP_DATA7	SA7	I/O	8 mA	G3
FP_DATA8	SA8	I/O	8 mA	G1
FP_DATA9	SA9	I/O	8 mA	F1
FP_DATA10	SA10	I/O	8 mA	E2
FP_DATA11	SA11	I/O	8 mA	D1
FP_DATA12	SA12	I/O	8 mA	L1
FP_DATA13	SA13	I/O	8 mA	K2
FP_DATA14	SA14	I/O	8 mA	K1
FP_DATA15	SA15	I/O	8 mA	H2
FP_DATA16	SA_OE#	O	8 mA	H3
FP_DATA17	MASTER#	I/O	8 mA	F3
FP_DISP_ENA_OUT	No Function	O	8 mA	F2
FP_ENA_BKL	No Function	O	8 mA	J4
FP_ENA_VDD	No Function	O	8 mA	L2
FP_HSYNC	No Function	I	8 mA	C2
FP_HSYNC_OUT	SMEMW#	O	8 mA	E1
FP_VSYNC	No Function	I	8 mA	C1

Table 3-3. 352 PBGA Pin Assignments - Sorted Alphabetically by Signal Name (Continued)

Signal Name		Pin Type[1]	Buffer Type[2]	Pin No.
Limited ISA Mode	ISA Master Mode			
FP_VSYNC_OUT	SMEMR#	O	8 mA	E3
FRAME#		I/O	PCI	C23
GNT#		I	PCI	D24
GPCS#		O	8 mA	AF26
GPIO0		I/O	8 mA	AC22
GPIO1/SDATA_IN2		I/O	8 mA	AE24
GPIO2		I/O	8 mA	AF25
GPIO3		I/O	8 mA	AF24
GPIO4/SA20	SA20	I/O	8 mA	AD22
GPIO5/SA21	SA21	I/O	8 mA	AC21
GPIO6/SA22	SA22	I/O	8 mA	AE23
GPIO7/SA23	SA23	I/O	8 mA	AF23
GPORT_CS#		O	8 mA	AD21
HOLD_REQ# (strap pin)		I/O	PCI	H26
HSYNC		I	8 mA	C6
HSYNC_OUT		O	8 mA	N1
IDE_ADDR0		O	IDE	U25
IDE_ADDR1		O	IDE	U26
IDE_ADDR2		O	IDE	W24
IDE_CS0#		O	IDE	V26
IDE_CS1#		O	IDE	Y26
IDE_DACK0#		O	IDE	T26
IDE_DACK1#		O	IDE	T24
IDE_DATA0		I/O	IDE	AC26
IDE_DATA1		I/O	IDE	AA24
IDE_DATA2		I/O	IDE	AB24
IDE_DATA3		I/O	IDE	AB26
IDE_DATA4		I/O	IDE	AA26
IDE_DATA5		I/O	IDE	W26
IDE_DATA6		I/O	IDE	U24
IDE_DATA7		I/O	IDE	U23
IDE_DATA8		I/O	IDE	V24
IDE_DATA9		I/O	IDE	Y25
IDE_DATA10		I/O	IDE	V25
IDE_DATA11		I/O	IDE	Y24
IDE_DATA12		I/O	IDE	AA25
IDE_DATA13		I/O	IDE	AB25
IDE_DATA14		I/O	IDE	AC25
IDE_DATA15		I/O	IDE	AB23
IDE_DREQ0		I	IDE	AD26
IDE_DREQ1		I	IDE	AC24
IDE_IOR0#		O	IDE	R26
IDE_IOR1#		O	IDE	R25
IDE_IORDY0		I	IDE	AD25
IDE_IORDY1		I	IDE	AE26
IDE_IOW0#		O	IDE	R24
IDE_IOW1#		O	IDE	T25
IDE_RST#		O	IDE	W25
INTA#		I	PCI	A14
INTB#		I	PCI	D15
INTC#		I	PCI	C15
INTD#		I	PCI	B14
INTR (strap pin)		I/O	8 mA	P26
IOCHRDY		I/O, OD	8 mA	AF11
IOCS16#		I	8 mA	AF16
IOR#		I/O (PU)	8 mA	AE12
IOUTB		O, Analog	--	R1
IOUTR		O, Analog	--	P3
IOUTG		O, Analog	--	P4
IOW#		I/O (PU)	8 mA	AC11
IRDY#		I/O	PCI	B24
IREF		I, Analog	--	R3
IRQ1		I	8 mA	AF13
IRQ3		I	8 mA	AC14
IRQ4		I	8 mA	AE15
IRQ5		I	8 mA	AE13
IRQ6		I	8 mA	AF14
IRQ7		I	8 mA	AD14
IRQ8#		I	8 mA	AE14
IRQ9		I	8 mA	AE5
IRQ10		I	8 mA	AE16
IRQ11		I	8 mA	AF18
IRQ12		I	8 mA	AF17
IRQ13		I	8 mA	R23
IRQ14		I	8 mA	AC17
IRQ15		I	8 mA	AD17
ISACLK		O	8 mA	AD6
KBROMCS#		O	8 mA	AE4
LOCK#		I/O	PCI	C22
MEMCS16#		I/O, OD	8 mA	AC15
MEMR#		I/O (PU)	8 mA	AE19
MEMW#		I/O (PU)	8 mA	AF20
NC		--	--	AA3
NC		--	--	AB1
NC		--	--	AB2
NC		--	--	AB3
NC		--	--	AC1
NC		--	--	AC2
NC		--	--	AC3
NC		--	--	AD1

Table 3-3. 352 PBGA Pin Assignments - Sorted Alphabetically by Signal Name (Continued)

Signal Name		Pin Type[1]	Buffer Type[2]	Pin No.
Limited ISA Mode	ISA Master Mode			
NC		--	--	AD2
NC		--	--	AD3
NC		--	--	AE1
NC		--	--	AE2
NC		--	--	AF1
NC		--	--	AF2
NC		--	--	D2
NC		--	--	M26
NC		--	--	N24
NC		--	--	T1
NC		--	--	W2
NC		--	--	Y3
OVER_CUR#		I	8 mA	W3
PAR		I/O	PCI	A21
PC_BEEP		O	8 mA	V3
PCICLK		I (SMT)	CLK	J26
PCI_RST#		O	8 mA	C14
PCLK		I	8 mA	A13
PERR#		I/O	PCI	B22
PIXEL0		I	8 mA	A1
PIXEL1		I	8 mA	A2
PIXEL2		I	8 mA	A3
PIXEL3		I	8 mA	C4
PIXEL4		I	8 mA	B3
PIXEL5		I	8 mA	B4
PIXEL6		I	8 mA	D5
PIXEL7		I	8 mA	A4
PIXEL8		I	8 mA	B6
PIXEL9		I	8 mA	D6
PIXEL10		I	8 mA	A5
PIXEL11		I	8 mA	C5
PIXEL12		I	8 mA	A7
PIXEL13		I	8 mA	D7
PIXEL14		I	8 mA	C7
PIXEL15		I	8 mA	B8
PIXEL16		I	8 mA	A8
PIXEL17		I	8 mA	C8
PIXEL18		I	8 mA	B9
PIXEL19		I	8 mA	A9
PIXEL20		I	8 mA	D9
PIXEL21		I	8 mA	C9
PIXEL22		I	8 mA	B11
PIXEL23		I	8 mA	C10
PLLAGD		I, Analog	--	N25
PLLDGN		I, Analog	--	N26
PLLDVD		I, Analog	--	M23
PLLTEST		--	--	N23
PLLVAA		I, Analog	--	M25
POR#		I	8 mA	K24
POWER_EN		O	8 mA	V4
PSERIAL		I	8 mA	L26

Signal Name		Pin Type[1]	Buffer Type[2]	Pin No.
Limited ISA Mode	ISA Master Mode			
REQ#		O	PCI	J25
SA0/SD0	SD0	I/O (PU)	8 mA	AE9
SA1/SD1	SD1	I/O (PU)	8 mA	AE6
SA2/SD2	SD2	I/O (PU)	8 mA	AD9
SA3/SD3	SD3	I/O (PU)	8 mA	AC6
SA4/SD4	SD4	I/O (PU)	8 mA	AF6
SA5/SD5	SD5	I/O (PU)	8 mA	AD5
SA6/SD6	SD6	I/O (PU)	8 mA	AF5
SA7/SD7	SD7	I/O (PU)	8 mA	AF4
SA8/SD8	SD8	I/O (PU)	8 mA	AF19
SA9/SD9	SD9	I/O (PU)	8 mA	AD19
SA10/SD10	SD10	I/O (PU)	8 mA	AC20
SA11/SD11	SD11	I/O (PU)	8 mA	AF21
SA12/SD12	SD12	I/O (PU)	8 mA	AE21
SA13/SD13	SD13	I/O (PU)	8 mA	AE22
SA14/SD14	SD14	I/O (PU)	8 mA	AD24
SA15/SD15	SD15	I/O (PU)	8 mA	AE25
SA16		I/O (PU)	8 mA	AD11
SA17		I/O (PU)	8 mA	AF12
SA18		I/O (PU)	8 mA	AE11
SA19		I/O (PU)	8 mA	AD10
SA_LATCH	SA_DIR	O	8 mA	AD15
SBHE#		I/O (PU)	8 mA	AE17
SDATA_IN		I	8 mA	U4
SDATA_OUT		O	8 mA	V1
SERR#		I/O, OD	PCI	A22
SMEMR#/RTCALE		O	8 mA	AD4
SMEMW#/RTCCS#		O	8 mA	AF3
SMI#		I/O	8 mA	P25
STOP#		I/O	PCI	E26
SUSP#		O	8 mA	K26
SUSPA#		I	8 mA	L25
SUSP_3V		I/O	8 mA	L24
SYNC		O	8 mA	U3
TC		O	8 mA	AF15
TEST		I	8 mA	D3
TRDY#		I/O	PCI	B23
TVCLK		I	8 mA	B2
USBCLK		I (SMT)	CLK	W1
V_{DD}		PWR	--	D10
V_{DD}		PWR	--	D17
V_{DD}		PWR	--	AC10
V_{DD}		PWR	--	AC19
V_{DD}		PWR	--	AD16
V_{DD}		PWR	--	AD23

Table 3-3. 352 PBGA Pin Assignments - Sorted Alphabetically by Signal Name (Continued)

Signal Name		Pin Type[1]	Buffer Type[2]	Pin No.
Limited ISA Mode	ISA Master Mode			
V_{DD}		PWR	--	C19
V_{DD}		PWR	--	C24
V_{DD}		PWR	--	C3
V_{DD}		PWR	--	D21
V_{DD}		PWR	--	F24
V_{DD}		PWR	--	F4
V_{DD}		PWR	--	H24
V_{DD}		PWR	--	L23
V_{DD}		PWR	--	L4
V_{DD}		PWR	--	T23
V_{DD}		PWR	--	Y23
V_{DD}_USB		PWR	--	U2
VID_CLK		I	8 mA	A6
VID_DATA0		I	8 mA	A11
VID_DATA1		I	8 mA	C13
VID_DATA2		I	8 mA	B13
VID_DATA3		I	8 mA	C11
VID_DATA4		I	8 mA	D11
VID_DATA5		I	8 mA	A12
VID_DATA6		I	8 mA	B12
VID_DATA7		I	8 mA	C12
VID_RDY		O	8 mA	B10
VID_VAL		I	8 mA	B7
V_{SS}		GND	--	D12
V_{SS}		GND	--	D13
V_{SS}		GND	--	D16
V_{SS}		GND	--	AA23
V_{SS}		GND	--	AC12
V_{SS}		GND	--	AC13
V_{SS}		GND	--	AC16
V_{SS}		GND	--	AC18
V_{SS}		GND	--	AC23
V_{SS}		GND	--	AC4
V_{SS}		GND	--	AC5
V_{SS}		GND	--	AC9
V_{SS}		GND	--	AD20
V_{SS}		GND	--	C18
V_{SS}		GND	--	C21
V_{SS}		GND	--	D19
V_{SS}		GND	--	D20
V_{SS}		GND	--	D22
V_{SS}		GND	--	D23
V_{SS}		GND	--	D4
V_{SS}		GND	--	D8
V_{SS}		GND	--	E23
V_{SS}		GND	--	E4
V_{SS}		GND	--	F23
V_{SS}		GND	--	G23
V_{SS}		GND	--	H23
V_{SS}		GND	--	H4
V_{SS}		GND	--	J23
V_{SS}		GND	--	K23
V_{SS}		GND	--	K4
V_{SS}		GND	--	M24
V_{SS}		GND	--	M3
V_{SS}		GND	--	N3
V_{SS}		GND	--	P23
V_{SS}		GND	--	V23
V_{SS}		GND	--	W23
V_{SS}		GND	--	W4
V_{SS}		GND	--	Y4
VSYNC		I	8 mA	B5
VSYNC_OUT		O	8 mA	N2
ZEROWS#		I	8 mA	AF10

1. See Table 3-1 "Pin Type Definitions" on page 20 for pin type definitions.
2. See Table 6-4 "DC Characteristics" on page 235 and Table 6-8 "AC Characteristics" on page 239 for more information on buffer types. Note that some bidirectional buffers are used as input only, indicated by an "I" in the Pin Type column.

3.2 Signal Descriptions

3.2.1 Reset Interface

Signal Name	Pin No.	Pin Type	Description
PCI_RST#	C14	O	**PCI Reset** PCI_RST# resets the PCI bus and is asserted while POR# is asserted, and for approximately 9 ms following the deassertion of POR#.
POR#	K24	I	**Power On Reset** POR# is the system reset signal generated from the power supply to indicate that the system should be reset.
CPU_RST	K25	O	**CPU Reset** CPU_RST resets the CPU and is asserted while POR# is asserted, and for approximately 9 ms following the deassertion of POR#. CLK_14MHZ is used to generate this signal.

3.2.2 Clock Interface

Signal Name	Pin No.	Pin Type	Description
PCICLK	J26	I (SMT)	**PCI Clock** The PCI clock is used to drive most circuitry of the CS5530A.
TVCLK	B2	I	**Television Clock** The TVCLK is an input from a digital NTSC/PAL converter which is optionally re-driven back out onto the DCLK signal under software program control. This is only used if interfacing to a compatible digital NTSC/PAL encoder device.
DCLK	A10	O	**DOT Clock** DOT clock is generated by the CS5530A and typically connects to the processor to create the clock used by the graphics subsystem. The minimum frequency of DCLK is 10 MHz and the maximum is 200 MHz. However, when DCLK is used as the graphics subsystem clock, the Geode processor determines the maximum DCLK frequency.
ISACLK	AD6	O	**ISA Bus Clock** ISACLK is derived from PCICLK and is typically programmed for approximately 8 MHz. F0 Index 50h[2:0] are used to program the ISA clock divisor.
CLK_14MHZ	P24	I (SMT)	**14.31818 MHz Clock** This clock is used to generate CPU_RST to the Geode processor. DOT clock (DCLK) is also derived from this clock.
USBCLK	W1	I (SMT)	**USBCLK** This input is used as the clock source for the USB. In this mode, a 48 MHz clock source input is required.
CLK_32K	AE3	I/O	**32 KHz Clock** CLK_32K is a 32.768 KHz clock used to generate reset signals, as well as to maintain power management functionality. It should be active when power is applied to the CS5530A. CLK_32K can be an input or an output. As an output CLK_32K is internally derived from CLK_14MHZ. F0 Index 44h[5:4] are used to program this pin.

3.2.3 CPU Interface

Signal Name	Pin No.	Pin Type	Description
INTR	P26 Strap Option Pin	O	**CPU Interrupt Request** INTR is the level output from the integrated 8259 PICs and is asserted if an unmasked interrupt request (IRQ_n) is sampled active.
		I	**Strap Option Select Pin** Pin P26 is a strap option select pin. It is used to select whether the CS5530A operates in Limited ISA or ISA Master mode. ISA Limited Mode—Strap pin P26 low through a 10-kohm resistor. ISA Master Mode—Strap pin P26 high through a 10-kohm resistor.
SMI#	P25	I/O	**System Management Interrupt** SMI# is a level-sensitive interrupt to the CPU that can be configured to assert on a number of different system events. After an SMI# assertion, System Management Mode (SMM) is entered, and program execution begins at the base of SMM address space. Once asserted, SMI# remains active until all SMI sources are cleared.
IRQ13	R23	I	**IRQ13** IRQ13 is an input from the processor indicating that a floating point error was detected and that INTR should be asserted.
PSERIAL	L26	I	**Power Management Serial Interface** PSERIAL is the unidirectional serial data link between the GX1 processor and the CS5530A. An 8-bit serial data packet carries status on power management events within the CPU. Data is clocked synchronous to the PCICLK input clock.
SUSP#	K26	O	**CPU Suspend** SUSP# asserted requests that the CPU enters Suspend mode and the CPU asserts SUSPA# after completion. The SUSP# pin is deasserted if SUSP# has gone active and any Speedup or Resume event has occurred, including expiration of the Suspend Modulation ON timer, which is loaded from F0 Index 95h. If the SUSP#/SUSPA# handshake is configured as a system 3 Volt Suspend, the deassertion of SUSP# is delayed by an interval programmed in F0 Index BCh[7:4] to allow the system clock chip and the processor to stabilize. The SUSP#/SUSPA# handshake occurs as a result of a write to the Suspend Notebook Command Register (F0 Index AFh), or expiration of the Suspend Modulation OFF timer (loaded from F0 Index 94h) when Suspend Modulation is enabled. Suspend Modulation is enabled via F0 Index 96h[0]. If SUSPA# is asserted as a result of a HALT instruction, SUSP# does not deassert when the Suspend Modulation ON timer (loaded from F0 Index 95h) expires.
SUSPA#	L25	I	**CPU Suspend Acknowledge** SUSPA# is a level input from the processor. When asserted it indicates the CPU is in Suspend mode as a result of SUSP# assertion or execution of a HALT instruction.

3.2.3 CPU Interface (Continued)

Signal Name	Pin No.	Pin Type	Description
SUSP_3V	L24	I/O	**Suspend 3 Volt Active** SUSP_3V can be connected to the output enable (OE) of a clock synthesis or buffer chip to stop the clocks to the system. SUSP_3V is asserted after the SUSP#/SUSPA# handshake that follows a write to the Suspend Notebook Command Register (F0 Index AFh) with bit 0 set in the Clock Stop Control Register (F0 Index BCh). As an input, SUSP_3V is sampled during power-on-reset to determine the inactive state. This allows the system designer to match the active state of SUSP_3V to the inactive state for a clock driver output enabled with a pull-up/down 10-kohm resistor. If pulled down, SUSP_3V is active high. If pulled up, SUSP_3V is active low.

3.2.4 PCI Interface

Signal Name	Pin No.	Pin Type	Description
AD[31:0]	Refer to Table 3-3	I/O	**PCI Address/Data** AD[31:0] is a physical address during the first clock of a PCI transaction; it is the data during subsequent clocks. When the CS5530A is a PCI master, AD[31:0] are outputs during the address and write data phases, and are inputs during the read data phase of a transaction. When the CS5530A is a PCI slave, AD[31:0] are inputs during the address and write data phases, and are outputs during the read data phase of a transaction.
C/BE[3:0]#	D26, A24, B21, B18	I/O	**PCI Bus Command and Byte Enables** During the address phase of a PCI transaction, C/BE[3:0]# define the bus command. During the data phase of a transaction, C/BE[3:0]# are the data byte enables. C/BE[3:0]# are outputs when the CS5530A is a PCI master and inputs when it is a PCI slave.
INTA#, INTB#, INTC#, INTD#	A14, D15, C15, B14	I	**PCI Interrupt Pins** The CS5530A provides inputs for the optional “level-sensitive” PCI interrupts (also known in industry terms as PIRQx#). These interrupts may be mapped to IRQs of the internal 8259s using PCI Interrupt Steering Registers 1 and 2 (F0 Index 5Ch and 5Dh). The USB controller uses INTA# as its output signal. Refer to PCIUSB Index 3Dh.
REQ#	J25	O	**PCI Bus Request** The CS5530A asserts REQ# in response to a DMA request or ISA master request to gain ownership of the PCI bus. The REQ# and GNT# signals are used to arbitrate for the PCI bus. REQ# should connect to the REQ0# of the GX1 processor and function as the highest-priority PCI master.

3.2.4 PCI Interface (Continued)

Signal Name	Pin No.	Pin Type	Description
GNT#	D24	I	**PCI Bus Grant** GNT# is asserted by an arbiter that indicates to the CS5530A that access to the PCI bus has been granted. GNT# should connect to GNT0# of the GX1 processor and function as the highest-priority PCI master.
HOLD_REQ#	H26 Strap Option Pin	O	**PCI Bus Hold Request** This pin's function as HOLD_REQ# is no longer applicable.
		I	**Strap Option Select Pin** Pin H26 is a strap option select pin. It allows selection of which address bits are used as the IDSEL. Strap pin H26 low: IDSEL = AD28 (Chipset Register Space) and AD29 (USB Register Space) Strap pin H26 high: IDSEL = AD26 (Chipset Register Space) and AD27 (USB Register Space)
FRAME#	C23	I/O	**PCI Cycle Frame** FRAME# is asserted to indicate the start and duration of a transaction. It is deasserted on the final data phase. FRAME# is an input when the CS5530A is a PCI slave.
IRDY#	B24	I/O	**PCI Initiator Ready** IRDY# is driven by the master to indicate valid data on a write transaction, or that it is ready to receive data on a read transaction. When the CS5530A is a PCI slave, IRDY# is an input that can delay the beginning of a write transaction or the completion of a read transaction. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
TRDY#	B23	I/O	**PCI Target Ready** TRDY# is asserted by a PCI slave to indicate it is ready to complete the current data transfer. TRDY# is an input that indicates a PCI slave has driven valid data on a read or a PCI slave is ready to accept data from the CS5530A on a write. TRDY# is an output that indicates the CS5530A has placed valid data on AD[31:0] during a read or is ready to accept the data from a PCI master on a write. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
STOP#	E26	I/O	**PCI Stop** As an input, STOP# indicates that a PCI slave wants to terminate the current transfer. The transfer is either aborted or retried. STOP# is also used to end a burst. As an output, STOP# is asserted with TRDY# to indicate a target disconnect, or without TRDY# to indicate a target retry. The CS5530A asserts STOP# during any cache line crossings if in single transfer DMA mode or if busy.

3.2.4 PCI Interface (Continued)

Signal Name	Pin No.	Pin Type	Description
LOCK#	C22	I/O	**PCI Lock** LOCK# indicates an atomic operation that may require multiple transactions to complete. If the CS5530A is currently the target of a LOCKed transaction, any other PCI master request with the CS5530A as the target is forced to retry the transfer. The CS5530A does not generate LOCKed transactions.
DEVSEL#	A23	I/O	**PCI Device Select** DEVSEL# is asserted by a PCI slave, to indicate to a PCI master and subtractive decoder that it is the target of the current transaction. As an input, DEVSEL# indicates a PCI slave has responded to the current address. As an output, DEVSEL# is asserted one cycle after the assertion of FRAME# and remains asserted to the end of a transaction as the result of a positive decode. DEVSEL# is asserted four cycles after the assertion of FRAME# if DEVSEL# has not been asserted by another PCI device when the CS5530A is programmed to be the subtractive decode agent. The subtractive decode sample point is configured in F0 Index 41h[2:1]. Subtractive decode cycles are passed to the ISA bus.
PAR	A21	I/O	**PCI Parity** PAR is the parity signal driven to maintain even parity across AD[31:0] and C/BE[3:0]#. The CS5530A drives PAR one clock after the address phase and one clock after each completed data phase of write transactions as a PCI master. It also drives PAR one clock after each completed data phase of read transactions as a PCI slave.
PERR#	B22	I/O	**PCI Parity Error** PERR# is pulsed by a PCI device to indicate that a parity error was detected. If a parity error was detected, PERR# is asserted by a PCI slave during a write data phase and by a PCI master during a read data phase. When the CS5530A is a PCI master, PERR# is an output during read transfers and an input during write transfers. When the CS5530A is a PCI slave, PERR# is an input during read transfers and an output during write transfers. Parity detection is enabled through F0 Index 04h[6]. An NMI is generated if I/O Port 061h[2] is set. PERR# can assert SERR# if F0 Index 41h[5] is set.
SERR#	A22	I/O OD	**PCI System Error** SERR# is pulsed by a PCI device to indicate an address parity error, data parity error on a special cycle command, or other fatal system errors. SERR# is an open-drain output reporting an error condition, and an input indicating that the CS5530A should generate an NMI. As an input, SERR# is asserted for a single clock by the slave reporting the error. System error detection is enabled with F0 Index 04h[8]. An NMI is generated if I/O Port 061h[2] is set. PERR# can assert SERR# if F0 Index 41h[5] is set.

3.2.5 ISA Bus Interface

Signal Name	Pin No.	Pin Type	Description
SA_LATCH/ SA_DIR	AD15	O	**Limited ISA Mode: System Address Latch** This signal is used to latch the destination address, which is multiplexed on bits [15:0] of the SA/SD bus.
			ISA Master Mode: System Address Direction Controls the direction of the external 5.0V tolerant transceiver on bits [15:0] of the SA bus. When low, the SA bus is driven out. When high, the SA bus is driven into the CS5530A by the external transceiver.
SA_OE#/ FP_DATA16	H3	O	**Limited ISA Mode: Flat Panel Data Port Line 16** Refer to Section 3.2.11 "Display Interface" on page 40 for this signal's definition.
		O	**ISA Master Mode: System Address Transceiver Output Enable** Enables the external transceiver on bits [15:0] of the SA bus.
MASTER#/ FP_DATA17	F3	O	**Limited ISA Mode: Flat Panel Data Port Line 17** Refer to Section 3.2.11 "Display Interface" on page 40 for this signal's definition.
		I	**ISA Master Mode: Master** The MASTER# input asserted indicates an ISA bus master is driving the ISA bus.
SA23/GPIO7	AF23	I/O	**Limited ISA Mode: System Address Bus Lines 23 through 20 or General Purpose I/Os 7 through 4** These pins can function either as the upper four bits of the SA bus or as general purpose I/Os. Programming is done through F0 Index 43h, bits 6 and 2. Refer to Section 3.2.9 "Game Port and General Purpose I/O Interface" on page 39 for further details when used as GPIOs.
SA22/GPIO6	AE23		
SA21/GPIO5	AC21		
SA20/GPIO4	AD22		
			ISA Master Mode: System Address Bus Lines 23 through 20 The pins function only as the four MSB (most significant bits) of the SA bus.
SA[19:16]	AD10, AE11, AF12, AD11	I/O (PU)	**System Address Bus Lines 19 through 16** Refer to SA[15:0] signal description.
SA[15:0]/SD[15:0]	Refer to Table 3-3	I/O (PU)	**Limited ISA Mode: System Address Bus / System Data Bus** This bus carries both the addresses and data for all ISA cycles. Initially, the address is placed on the bus and then SA_LATCH is asserted in order for external latches to latch the address. At some time later, the data is put on the bus, for a read, or the bus direction is changed to an input, for a write. Pins designated as SA/SD[15:0] are internally connected to a 20-kohm pull-up resistor.
			ISA Master Mode: System Data Bus These pins perform only as SD[15:0] and pins FP_DATA[15:0] take on the functions of SA[15:0]. Pins designated as SA/SD[15:0] are internally connected to a 20-kohm pull-up resistor.

3.2.5 ISA Bus Interface (Continued)

Signal Name	Pin No.	Pin Type	Description
SMEMW#/ FP_HSYNC_OUT	E1	O	**Limited ISA Mode: Flat Panel Horizontal Sync Output** Refer to Section 3.2.11 "Display Interface" on page 40 for this signal's definition. Note that if Limited ISA Mode of operation is selected, SMEMW# is available on pin AF3 (multiplexed with RTCCS#).
			ISA Master Mode: System Memory Write SMEMW# is asserted for any memory write accesses below 1 MB (i.e., A23:A20 set to 0). This enables 8-bit memory slaves to decode the memory address on SA[19:0].
SMEMR#/ FP_VSYNC_OUT	E3	O	**Limited ISA Mode: Flat Panel Vertical Sync Output** Refer to Section 3.2.11 "Display Interface" on page 40 for this signal's definition. Note that if Limited ISA Mode of operation is selected, SMEMR# is available on pin AD4 (multiplexed with RTCALE).
			ISA Master Mode: System Memory Read SMEMR# is asserted for memory read accesses below 1 MB (i.e., A23:A20 set to 0). This enables 8-bit memory slaves to decode the memory address on SA[19:0].
SMEMW#/ RTCCS#	AF3	O	**System Memory Write / Real-Time Clock Chip Select** If Limited ISA Mode of operation has been selected, then SMEMW# can be output on this pin. SMEMW# is asserted for any memory write accesses below 1 MB (i.e., A23:A20 set to 0). This enables 8-bit memory slaves to decode the memory address on SA[19:0]. RTCCS# is a chip select to an external real-time clock chip. This signal is activated on reads or writes to I/O Port 071h. Function selection is made through F0 Index 53h[2]: 0 = SMEMW#, 1 = RTCCS#.
SMEMR#/ RTCALE	AD4	O	**System Memory Read / Real-Time Clock Address Latch Enable** If Limited ISA Mode of operation has been selected, then SMEMR# can be output on this pin. SMEMR# is asserted for memory read accesses below 1 MB (i.e., A23:A20 set to 0). This enables 8-bit memory slaves to decode the memory address on SA[19:0]. RTCALE is a signal telling an external real-time clock chip to latch the address, which is on the SD bus. Function selection is made through F0 Index 53h[2]: 0 = SMEMR#, 1 = RTCALE.
SBHE#	AE17	I/O (PU)	**System Bus High Enable** The CS5530A or ISA master asserts SBHE# to indicate that SD[15:8] will be used to transfer a byte at an odd address. SBHE# is an output during non-ISA master DMA operations. It is driven as the inversion of AD0 during 8-bit DMA cycles. It is forced low for all 16-bit DMA cycles. SBHE# is an input during ISA master operations. This pin is internally connected to a 20-kohm pull-up resistor.
BALE	AF9	O	**Buffered Address Latch Enable** BALE indicates when SA[23:0] and SBHE# are valid and may be latched. For DMA transfers, BALE remains asserted until the transfer is complete.

3.2.5 ISA Bus Interface (Continued)

Signal Name	Pin No.	Pin Type	Description
IOCHRDY	AF11	I/O OD	**I/O Channel Ready** IOCHRDY deasserted indicates that an ISA slave requires additional wait states. When the CS5530A is an ISA slave, IOCHRDY is an output indicating additional wait states are required.
ZEROWS#	AF10	I	**Zero Wait States** ZEROWS# asserted indicates that an ISA 8- or 16-bit memory slave can shorten the current cycle. The CS5530A samples this signal in the phase after BALE is asserted. If asserted, it shortens 8-bit cycles to three ISACLKs and 16-bit cycles to two ISACLKs.
IOCS16#	AF16	I	**I/O Chip Select 16** IOCS16# is asserted by 16-bit ISA I/O devices based on an asynchronous decode of SA[15:0] to indicate that SD[15:0] will be used to transfer data. 8-bit ISA I/O devices only use SD[7:0].
IOR#	AE12	I/O (PU)	**I/O Read** IOR# is asserted to request an ISA I/O slave to drive data onto the data bus. This pin is internally connected to a 20-kohm pull-up resistor.
IOW#	AC11	I/O (PU)	**I/O Write** IOW# is asserted to request an ISA I/O slave to accept data from the data bus. This pin is internally connected to a 20-kohm pull-up resistor.
MEMCS16#	AC15	I/O OD	**Memory Chip Select 16** MEMCS16# is asserted by 16-bit ISA memory devices based on an asynchronous decode of SA[23:17] to indicate that SD[15:0] will be used to transfer data. 8-bit ISA memory devices only use SD[7:0].
MEMR#	AE19	I/O (PU)	**Memory Read** MEMR# is asserted for any memory read accesses. It enables 16-bit memory slaves to decode the memory address on SA[23:0]. This pin is internally connected to a 20-kohm pull-up resistor.
MEMW#	AF20	I/O (PU)	**Memory Write** MEMW# is asserted for any memory write accesses. It enables 16-bit memory slaves to decode the memory address on SA[23:0]. This pin is internally connected to a 20-kohm pull-up resistor.
AEN	AE8	O	**Address Enable** AEN asserted indicates that a DMA transfer is in progress, informing I/O devices to ignore the I/O cycle.
IRQ[15:14], [12:9], [7:3], 1	Refer to Table 3-3	I	**ISA Bus Interrupt Request** IRQ inputs indicate ISA devices or other devices requesting a CPU interrupt service.
IRQ8#	AE14	I	**Real-Time Clock Interrupt** IRQ8# is the (active-low) interrupt that comes from the external RTC chip and indicates a date/time update has completed.

3.2.5 ISA Bus Interface (Continued)

Signal Name	Pin No.	Pin Type	Description
DRQ[7:5], DRQ[3:0]	Refer to Table 3-3	I	**DMA Request - Channels 7 through 5 and 3 through 0** DRQ inputs are asserted by ISA DMA devices to request a DMA transfer. The request must remain asserted until the corresponding DACK is asserted.
DACK[7:5]#, DACK[3:0]#	Refer to Table 3-3	O	**DMA Acknowledge - Channels 7 through 5 and 3 through 0** DACK outputs are asserted to indicate when a DRQ is granted and the start of a DMA cycle.
TC	AF15	O	**Terminal Count** TC signals the final data transfer of a DMA transfer.

3.2.6 ROM Interface

Signal Name	Pin No.	Pin Type	Description
KBROMCS#	AE4	O	**Keyboard/ROM Chip Select** KBROMCS# is the enable pin for the BIOS ROM and for the keyboard controller. For ROM accesses, KBROMCS# is asserted for ISA memory accesses programmed at F0 Index 52h[2:0]. For keyboard controller accesses, KBROMCS# is asserted for I/O accesses to I/O Ports 060h, 062h, 064h, and 066h.

3.2.7 IDE Interface

Signal Name	Pin No.	Pin Type	Description
IDE_RST#	W25	O	**IDE Reset** This signal resets all the devices that are attached to the IDE interface.
IDE_ADDR[2:0]	W24, U26, U25	O	**IDE Address Bits** These address bits are used to access a register or data port in a device on the IDE bus.
IDE_DATA[15:0]	Refer to Table 3-3	I/O	**IDE Data Lines** IDE_DATA[15:0] transfers data to/from the IDE devices.
IDE_IOR0#	R26	O	**IDE I/O Read for Channels 0 and 1** IDE_IOR0# is the read signal for Channel 0, and IDE_IOR1# is the read signal for Channel 1. Each signal is asserted on read accesses to the corresponding IDE port addresses. When in Ultra DMA/33 mode, these signals are redefined: Read Cycle — DMARDY0# and DMARDY1# Write Cycle — STROBE0 and STROBE1
IDE_IOR1#	R25	O	
IDE_IOW0#	R24	O	**IDE I/O Write for Channels 0 and 1** IDE_IOW0# is the write signal for Channel 0, and IDE_IOW1# is the read signal for Channel 1. Each signal is asserted on write accesses to corresponding IDE port addresses. When in Ultra DMA/33 mode, these signals are redefined: Read Cycle — STOP0 and STOP1 Write Cycle — STOP0 and STOP1
IDE_IOW1#	T25	O	
IDE_CS0#	V26	O	**IDE Chip Selects** The chip select signals are used to select the command block registers in an IDE device.
IDE_CS1#	Y26	O	
IDE_IORDY0	AD25	I	**I/O Ready Channels 0 and 1** When deasserted, these signals extend the transfer cycle of any host register access when the device is not ready to respond to the data transfer request. When in Ultra DMA/33 mode, these signals are redefined: Read Cycle — STROBE0 and STROBE1 Write Cycle — DMARDY0# and DMARDY1#
IDE_IORDY1	AE26	I	
IDE_DREQ0	AD26	I	**DMA Request Channels 0 and 1** The DREQ is used to request a DMA transfer from the CS5530A. The direction of the transfers are determined by the IDE_IOR/IOW signals.
IDE_DREQ1	AC24	I	
IDE_DACK0#	T26	O	**DMA Acknowledge Channels 0 and 1** The DACK# acknowledges the DREQ request to initiate DMA transfers.
IDE_DACK1#	T24	O	

3.2.8 USB Interface

Signal Name	Pin No.	Pin Type	Description
POWER_EN	V4	O	**Power Enable** This pin enables the power to a self-powered USB hub.
OVER_CUR#	W3	I	**Over Current** This pin indicates the USB hub has detected an overcurrent on the USB.
D+_PORT1	Y2	I/O	**USB Port 1 Data Positive** This pin is the Universal Serial Bus Data Positive for port 1.
D–_PORT1	Y1	I/O	**USB Port 1 Data Minus** This pin is the Universal Serial Bus Data Minus for port 1.
D+_PORT2	AA2	I/O	**USB Port 2 Data Positive** This pin is the Universal Serial Bus Data Positive for port 2.
D–_PORT2	AA1	I/O	**USB Port 2 Data Minus** This pin is the Universal Serial Bus Data Minus for port 2.
V_{DD}_USB	U2	PWR	**Power for USB**
AV_{DD}_USB	AB4	I Analog	**Analog Power for USB**
AV_{SS}_USB	AA4	I Analog	**Analog Ground for USB**

3.2.9 Game Port and General Purpose I/O Interface

Signal Name	Pin No.	Pin Type	Description
GPORT_CS#	AD21	O	**Game Port Chip Select** GPORT_CS# is asserted upon any I/O reads or I/O writes to I/O Port 200h and 201h.
GPCS#	AF26	O	**General Purpose Chip Select** GPCS# is asserted upon any I/O access that matches the I/O address in the General Purpose Chip Select Base Address Register (F0 Index 70h) and the conditions set in the General Purpose Chip Select Control Register (F0 Index 72h).
GPIO7/SA23	AF23	I/O	**Limited ISA Mode: General Purpose I/Os 7 through 4 or System Address Bus Lines 23 through 20** These pins can function either as general purpose I/Os or as the upper four bits of the SA bus. Selection is done through F0 Index 43h[6,2]. Refer to GPIO[3:2] signal description for GPIO function description.
GPIO6/SA22	AE23		
GPIO5/SA21	AC21		
GPIO4/SA20	AD22		
			ISA Master Mode: System Address Bus Lines 23 through 20 These pins function as the four MSB (most significant bits) of the SA bus.
GPIO3	AF24	I/O	**General Purpose I/Os 3 and 2** GPIOs can be programmed to operate as inputs or outputs via F0 Index 90h. As an input, the GPIO can be configured to generate an external SMI. Additional configuration can select if the SMI# is generated on the rising or falling edge. GPIO external SMI generation/edge selection is done in F0 Index 92h and 97h.
GPIO2	AF25	I/O	

3.2.9 Game Port and General Purpose I/O Interface (Continued)

Signal Name	Pin No.	Pin Type	Description
GPIO1/ SDATA_IN2	AE24	I/O	**General Purpose I/O 1 or Serial Data Input 2** This pin can function either as a general purpose I/O or as a second serial data input pin if two codecs are used in the system. In order for this pin to function as SDATA_IN2, it must first be configured as an input (F0 Index 90h[1] = 0). Then setting F3BAR+Memory Offset 08h[21] = 1 selects the pin to function as SDATA_IN2. Refer to GPIO[3:2] signal description for GPIO function description.
GPIO0	AC22	I/O	**General Purpose I/O 0** Refer to GPIO[3:2] signal description for GPIO function description.

3.2.10 Audio Interface

Signal Name	Pin No.	Pin Type	Description
BIT_CLK	V2	I	**Audio Bit Clock** The serial bit clock from the codec.
SDATA_OUT	V1	O	**Serial Data I/O** This output transmits audio serial data to the codec.
SDATA_IN	U4	I	**Serial Data Input** This input receives serial data from the codec.
SYNC	U3	O	**Serial Bus Synchronization** This bit is asserted to synchronize the transfer of data between the CS5530A and the AC97 codec.
PC_BEEP	V3	O	**PC Beep** Legacy PC/AT speaker output.

3.2.11 Display Interface

Signal Name	Pin No.	Pin Type	Description
Pixel Port			
PCLK	A13	I	**Pixel Clock** This clock is used to sample data on the PIXEL input port. It runs at the graphics DOT clock (DCLK) rate.
PIXEL[23:0]	Refer to Table 3-3	I	**Pixel Data Port** This is the input pixel data from the processor's display controller. If F4BAR+Memory Offset 00h[29] is reset, the data is sent in RGB 8:8:8 format. Otherwise, the pixel data is sent in RGB 5:6:5 format which has been dithered by the processor. The other eight bits are used in conjunction with VID_DATA[7:0] to provide 16-bit video data. This bus is sampled by the PCLK input.

3.2.11 Display Interface (Continued)

Signal Name	Pin No.	Pin Type	Description
ENA_DISP	B1	I	**Display Enable Input** This signal qualifies active data on the pixel input port. It is used to qualify active pixel data for all display modes and configurations and is not specific to flat panel display.
Display CRT			
HSYNC	C6	I	**Horizontal Sync Input** This is the CRT horizontal sync input from the processor's display controller. It is used to indicate the start of a new video line. This signal is pipelined for the appropriate number of clock stages to remain in sync with the pixel data. A separate output (HSYNC_OUT) is provided to re-drive the CRT and flat panel interfaces.
HSYNC_OUT	N1	O	**Horizontal Sync Output** This is the horizontal sync output to the CRT. It represents a delayed version of the input horizontal sync signal with the appropriate pipeline delay relative to the pixel data. The pipeline delay and polarity of this signal are programmable.
VSYNC	B5	I	**Vertical Sync Input** This is the CRT vertical sync input from the processor's display controller. It is used to indicate the start of a new frame. This signal is pipelined for the appropriate number of clock stages to remain in sync with the pixel data. A separate output (VSYNC_OUT) is provided to re-drive the CRT and flat panel interfaces.
VSYNC_OUT	N2	O	**Vertical Sync Output** This is the vertical sync output to the CRT. It represents a delayed version of the input vertical sync signal with the appropriate pipeline delay relative to the pixel data. The pipeline delay and polarity of this signal are programmable.
DDC_SCL	M2	O	**DDC Serial Clock** This is the serial clock for the VESA Display Data Channel interface. It is used for monitoring communications. The DDC2B standard is supported by this interface.
DDC_SDA	M4	I/O	**DDC Serial Data** This is the bidirectional serial data signal for the VESA Display Data Channel interface. It is used to monitor communications. The DDC2B standard is supported by this interface. The direction of this pin can be configured through F4BAR+Memory Offset 04h[24]: 0 = Input; 1 = Output.
IREF (Video DAC)	R3	I Analog	**VDAC Current Reference Input** Connect a 680 ohm resistor between this pin and AV_{SS} (analog ground for Video DAC).
EXTVREFIN (Video DAC)	T2	I Analog	**External Voltage Reference Pin** Connect this pin to a 1.235V voltage reference.

3.2.11 Display Interface (Continued)

Signal Name	Pin No.	Pin Type	Description
AV_{DD1} (DAC)	U1	I Analog	**Analog Power for Video DAC** These pins provide power to the analog portions of the Video DAC. A 47 µF capacitor should be connected between the DAC analog power and DAC analog ground. Analog power is AV_{DD1} (pin U1) and AV_{DD3} (pin N4). Analog ground is AV_{SS1} (pin R2) and AV_{SS5} (pin P2).
AV_{DD2} (VREF)	T3		
AV_{DD3} (DAC)	N4		
AV_{SS1} (DAC)	R2	I Analog	**Analog Ground for Video DAC** These pins provide the ground plane connections to the analog portions of the Video DAC. A 47 µF capacitor should be connected between the DAC analog power and DAC analog ground. Analog power is AV_{DD1} (pin U1) and AV_{DD3} (pin N4). Analog ground is AV_{SS1} (pin R2) and AV_{SS5} (pin P2).
AV_{SS2} (ICAP)	R4		
AV_{SS3} (VREF)	T4		
AV_{SS4} (ICAP)	P1		
AV_{SS5} (DAC)	P2		
IOUTR (Video DAC)	P3	O Analog	**Red DAC Output** Red analog output.
IOUTG (Video DAC)	P4	O Analog	**Green DAC Output** Green analog output.
IOUTB (Video DAC)	R1	O Analog	**Blue DAC Output** Blue analog output.
Display TFT/TV			
FP_DATA17/ MASTER#	F3	O	**Limited ISA Mode: Flat Panel Data Port Line 17** Refer to FP_DATA[15:0] signal description.
		I	**ISA Master Mode: Master** Refer to Section 3.2.5 "ISA Bus Interface" on page 34 for this signal's definition.
FP_DATA16/ SA_OE#	H3	O	**Limited ISA Mode: Flat Panel Data Port Line 16** Refer to FP_DATA[15:0] signal description.
		O	**ISA Master Mode: System Address Transceiver Output Enable** Refer to Section 3.2.5 "ISA Bus Interface" on page 34 for this signal's definition.
FP_DATA[15:0]/ SA[15:0]	Refer to Table 3-3	O	**Limited ISA Mode: Flat Panel Data Port Lines 15 through 0** This is the data port to an attached active matrix TFT panel. This port may optionally be tied to a DSTN formatter chip, LVDS transmitter, or digital NTSC/PAL encoder. F4BAR+Memory Offset 04h[7] enables the flat panel data bus: 0 = FP_DATA[17:0] is forced low 1 = FP_DATA[17:0] is driven based upon power sequence control
		I/O	**ISA Master Mode: System Address Bus Lines 15 through 0** These pins function as SA[15:0] and the pins designated as SA/SD[15:0] function only as SD[15:0]. Note that SA[19:16] are dedicated address pins and GPIO[7:4] function as SA[23:20] only.

3.2.11 Display Interface (Continued)

Signal Name	Pin No.	Pin Type	Description
FP_CLK	M1	O	**Limited ISA Mode: Flat Panel Clock** This is the clock for the flat panel interface.
		--	**ISA Master Mode: No Function** In the ISA Master mode of operation, the CS5530A cannot support TFT flat panels or TV controllers.
FP_CLK_EVEN	L3	O	**Limited ISA Mode: Flat Panel Even Clock** This is an optional output clock for a set of external latches used to de-multiplex the flat panel data bus into two channels (odd/even). Typically this would be used to interface to a pair of LVDS transmitters driving an XGA resolution flat panel. F4BAR+Memory Offset 04h[12] enables the FP_CLK_EVEN output: 0 = Standard flat panel 1 = XGA flat panel
		--	**ISA Master Mode: No Function** In the ISA Master mode of operation, the CS5530A can not support TFT flat panels or TV controllers.
FP_HSYNC	C2	I	**Limited ISA Mode: Flat Panel Horizontal Sync Input** This is the horizontal sync input reference from the processor's display controller. The timing of this signal is independent of the standard (CRT) horizontal sync input to allow a different timing relationship between the flat panel and an attached CRT.
		--	**ISA Master Mode: No Function** In the ISA Master mode of operation, the CS5530A can not support TFT flat panels or TV controllers.
FP_HSYNC_OUT /SMEMW#	E1	O	**Limited ISA Mode: Flat Panel Horizontal Sync Output** This is the horizontal sync for an attached active matrix TFT flat panel. This represents a delayed version of the input flat panel horizontal sync signal with the appropriate pipeline delay relative to the pixel data.
			ISA Master Mode: System Memory Write Refer to Section 3.2.5 "ISA Bus Interface" on page 34 for this signal's definition.
FP_VSYNC	C1	I	**Limited ISA Mode: Flat Panel Vertical Sync Input** This is the vertical sync input reference from the processor's display controller. The timing of this signal is independent of the standard (CRT) vertical sync input to allow a different timing relationship between the flat panel and an attached CRT.
		--	**ISA Master Mode: No Function** In the ISA Master mode of operation, the CS5530A can not support TFT flat panels or TV controllers.
FP_VSYNC_OUT /SMEMR#	E3	O	**Limited ISA Mode: Flat Panel Vertical Sync Output** This is the vertical sync for an attached active matrix TFT flat panel. This represents a delayed version of the input flat panel vertical sync signal with the appropriate pipeline delay relative to the pixel data.
			ISA Master Mode: System Memory Read Refer to Section 3.2.5 "ISA Bus Interface" on page 34 on for this signal's definition.

3.2.11 Display Interface (Continued)

Signal Name	Pin No.	Pin Type	Description
FP_DISP_ ENA_OUT	F2	O	**Flat Panel Display Enable Output** This is the display enable for an attached active matrix TFT flat panel. This signal qualifies active pixel data on the flat panel interface.
		--	**ISA Master Mode: No Function** In the ISA Master mode of operation, the CS5530A can not support TFT flat panels or TV controllers.
FP_ENA_VDD	L2	O	**Flat Panel VDD Enable** This is the enable signal for the V_{DD} supply to an attached flat panel. It is under the control of power sequence control logic. A transition on bit 6 of the Display Configuration Register (F4BAR+Memory Offset 04h) initiates a power-up/down sequence.
		--	**ISA Master Mode: No Function** In the ISA Master mode of operation, the CS5530A can not support TFT flat panels or TV controllers.
FP_ENA_BKL	J4	O	**Flat Panel Backlight Enable Output** This is the enable signal for the backlight power supply to an attached flat panel. It is under control of the power sequence control logic.
		--	**ISA Master Mode: No Function** In the ISA Master mode of operation, the CS5530A can not support TFT flat panels or TV controllers.
Display MPEG			
VID_DATA[7:0]	C12, B12, A12, D11, C11, B13, C13, A11	I	**Video Data Port** This is the input data for a video (MPEG) or graphics overlay in its native form. For video overlay, this data is in an interleaved YUV 4:2:2 format. For graphics overlay, the data is in RGB 5:6:5 format. This port operates at the VID_CLK rate.
VID_CLK	A6	I	**Video Clock** This is the clock for the video port. This clock is completely asynchronous to the input pixel clock rate.
VID_VAL	B7	I	**Video Valid** This signal indicates that valid video data is being presented on the VID_DATA input port. If the VID_RDY signal is also asserted, the data will advance.
VID_RDY	B10	O	**Video Ready** This signal indicates that the CS5530A is ready to receive the next piece of video data on the VID_DATA port. If the VID_VAL signal is also asserted, the data will advance.

3.2.12 DCLK PLL

Signal Name	Pin No.	Pin Type	Description
PLLTEST	N23	--	**PLLTEST** Internal test pin. This pin should not be connected for normal operation.
PLLVAA	M25	I Analog	**Analog PLL Power (V_{DD})** PLLVAA is the analog positive rail power connection to the PLL.
PLLAGD	N25	I Analog	**Analog PLL Ground (V_{SS})** PLLAGD is the analog ground rail connection to the PLL.
PLLDVD	M23	I Analog	**Digital PLL Power (V_{DD})** This pin is the digital V_{DD} power connection for the PLL.
PLLDGN	N26	I Analog	**Digital PLL Ground (V_{SS})** This pin is the digital ground (V_{SS}) connection for the PLL.

3.2.13 Power, Ground, and No Connects

Signal Name	Pin No.	Pin Type	Description
V_{DD}	Refer to Table 3-3 (Total of 17)	PWR	**3.3V (Nominal) Power Connection** Note that the USB power (V_{DD}_USB, AV_{DD}_USB) connections are listed in Section 3.2.8 "USB Interface" on page 39.
V_{SS}	Refer to Table 3-3 (Total of 38)	GND	**Ground Connection** Note that the USB ground (AV_{SS}_USB) connection is listed in Section 3.2.8 "USB Interface" on page 39.
NC	Refer to Table 3-3 (Total of 20)	--	**No Connection** These lines should be left disconnected. Connecting a pull-up/-down resistor or to an active signal could cause unexpected results and possible malfunctions.

3.2.14 Internal Test and Measurement

Signal Name	Pin No.	Pin Type	Description
TEST	D3	I	**Test Mode** TEST should be tied low for normal operation.

4 Functional Description

The AMD Geode™ CS5530A companion device provides many support functions for a GX1 processor. This chapter discusses the detailed operations of the CS5530A in two categories: system-level activities and operations/programming of the major functional blocks.

The system-level discussion topics revolve around events that affect the device as a whole unit and as an interface with other chips (e.g., processor): Topics include:

- Processor Interface
  - — Display Subsystem Connections
  - — PSERIAL Pin Interface
- PCI Bus Interface
  - — PCI Initiator
  - — PCI Target
  - — Special Bus Cycles–Shutdown/Halt
  - — PCI Bus Parity
  - — PCI Interrupt Routing Support
  - — Delayed Transactions
- Resets and Clocks
  - — Resets
  - — ISA Clock
  - — DOT Clock
- Power Management
  - — CPU Power Management
  - — APM Support
  - — Peripheral Power Management

All of the major functional blocks interact with the processor through the PCI bus, or via its own direct interface. The major functional blocks are divided out as:

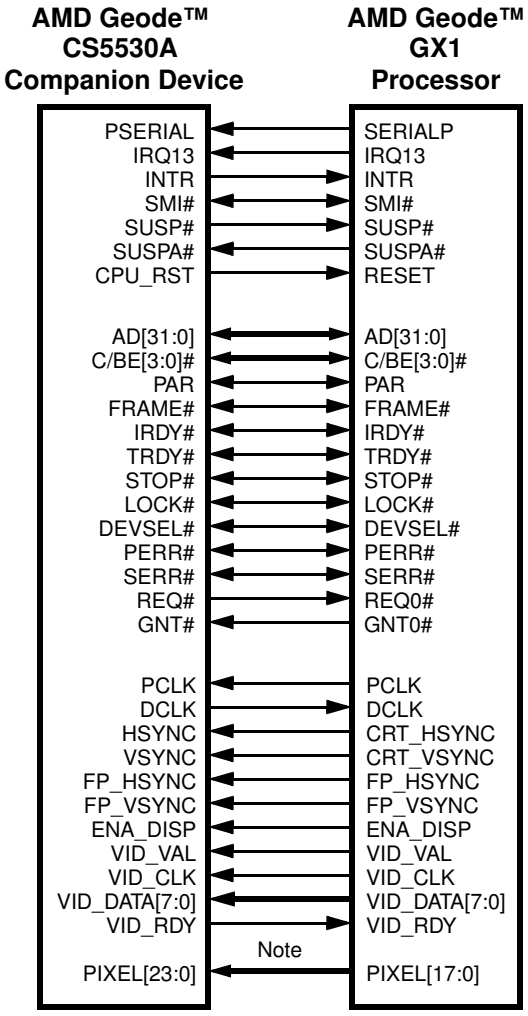
- PC/AT Compatibility Logic
  - — ISA Subtractive Decode
  - — ISA Bus Interface
  - — ROM Interface
  - — Megacells
  - — I/O Ports 092h and 061h System Control
  - — Keyboard Interface Function
  - — External Real-Time Clock Interface
- IDE Controller
  - — IDE Interface Signals
  - — IDE Configuration Registers
- XpressAUDIO™ Subsystem
  - — Subsystem Data Transport Hardware
  - — VSA Technology Support Hardware
- Display Subsystem Extensions
  - — Video Interface Configuration Registers
  - — Video Accelerator
  - — Video Overlay
  - — Gamma RAM
  - — Display Interface
- Universal Serial Bus Support
  - — USB PCI Controller
  - — USB Host Controller
  - — USB Power Management

Note that this Functional Description section of the data book describes many of the registers used for configuration of the CS5530A; however, not all registers are reported in detail. Some tables in the following subsections show only the bits (not the entire register) associated with a specific function being discussed. For access, register, and bit information regarding all CS5530A registers refer to Section 5.0 "Register Descriptions" on page 143.

4.1 Processor Interface

The CS5530A interface to the GX1 processor consists of seven miscellaneous connections, the PCI bus interface signals, plus the display controller connections. Figure 4-1 shows the interface requirements. Note that the PC/AT legacy pins NMI, WM_RST, and A20M are all virtual functions executed in SMM (System Management Mode) by the BIOS.

- PSERIAL is a one-way serial bus from the processor to the CS5530A used to communicate power management states and VSYNC information for VGA emulation.
- IRQ13 is an input from the processor indicating that a floating point error was detected and that INTR should be asserted.
- INTR is the level output from the integrated 8259 PICs and is asserted if an unmasked interrupt request (IRQn) is sampled active.
- SMI# is a level-sensitive interrupt to the processor that can be configured to assert on a number of different system events. After an SMI# assertion, SMM is entered and program execution begins at the base of the SMM address space. Once asserted, SMI# remains active until the SMI source is cleared.
- SUSP# and SUSPA# are handshake pins for implementing CPU Clock Stop and clock throttling.
- CPU_RST resets the CPU and is asserted for approximately 9 ms after the negation of POR#.
- PCI bus interface signals.
- Display subsystem interface connections.



Note: Refer to Figure 4-3 on page 50 for correct interconnection of PIXEL lines with the processor.

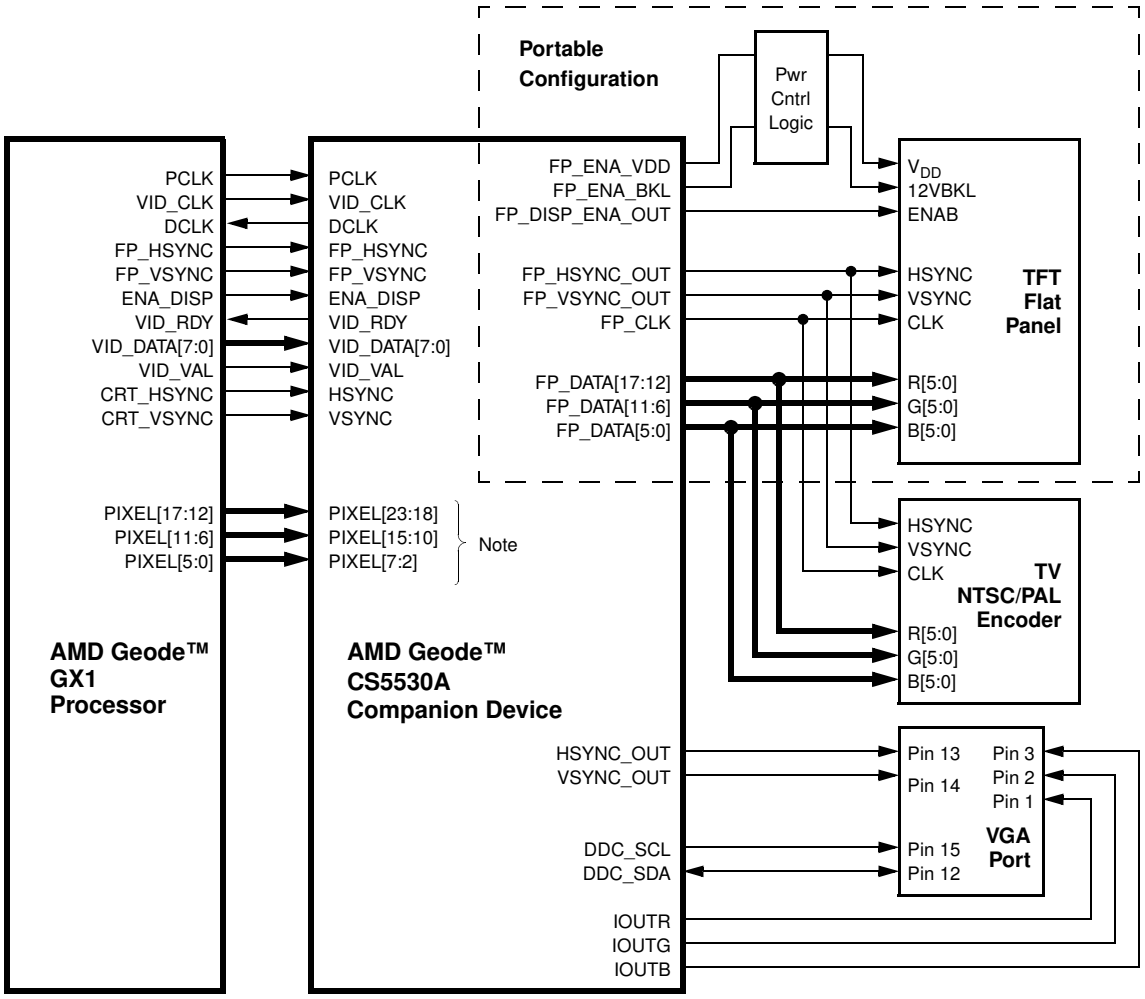
Figure 4-1. Processor Signal Connections

4.1.1 Display Subsystem Connections

When a GX1 processor is used in a system with the CS5530A, the need for an external RAMDAC is eliminated. The CS5530A contains the DACs, a video accelerator engine, and the TFT interface.

The CS5530A also supports both portable and desktop configurations. Figure 4-2 shows the signal connections for both types of systems.

Figure 4-3 on page 50 details how PIXEL[17:0] on the processor connects with PIXEL[23:0] of the CS5530A.



Note: Connect PIXEL[17:16] PIXEL[9:8], and PIXEL[1:0] on the CS5530A to ground.
See Figure 4-3 "PIXEL Signal Connections" on page 50.

Figure 4-2. Portable/Desktop Display Subsystem Configurations

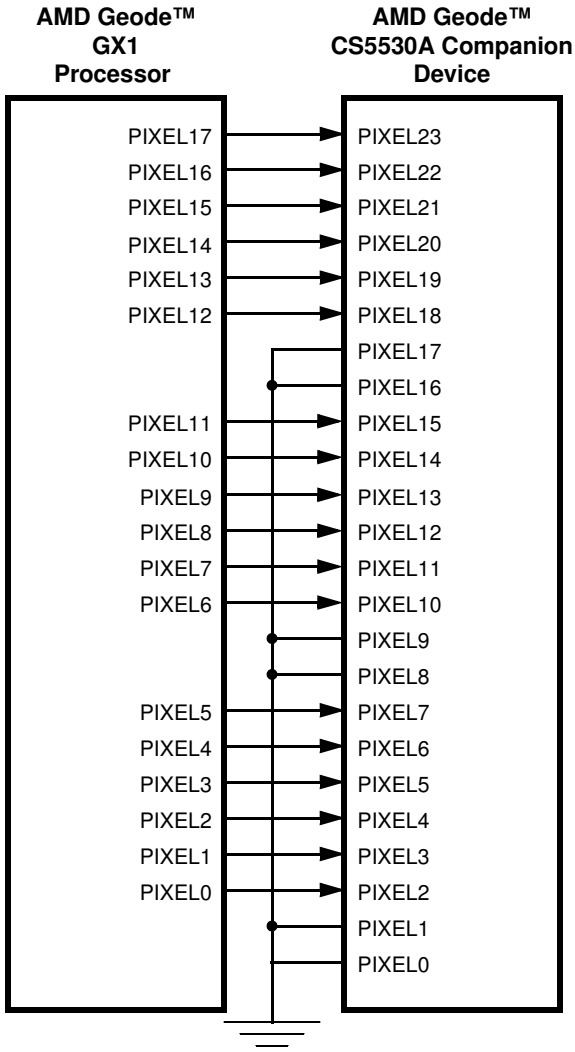


Figure 4-3. PIXEL Signal Connections

4.1.2 PSERIAL Pin Interface

The majority of the system power management logic is implemented in the CS5530A, but a minimal amount of logic is contained within the GX1 processor to provide information that is not externally visible (e.g., graphics controller).

The processor implements a simple serial communications mechanism to transmit the CPU status to the CS5530A. The processor accumulates CPU events in an 8-bit register (defined in Table 4-1) which it transmits serially every 1 to 10 µs.

The packet transmitter holds the serial output pin (PSERIAL) low until the transmission interval timer has elapsed. Once the timer has elapsed, the PSERIAL pin is held high for two clocks to indicate the start of packet transmission. The contents of the Serial Packet Register are then shifted out starting from bit 7 down to bit 0. The PSERIAL pin is held high for one clock to indicate the end of packet transmission and then remains low until the next transmission interval. After the packet transmission is complete, the processor's Serial Packet Register's contents are cleared.

The processor's input clock is used as the clock reference for the serial packet transmitter.

Once a bit in the register is set, it remains set until the completion of the next packet transmission. Successive events of the same type that occur between packet transmissions are ignored. Multiple unique events between packet transmissions accumulate in this register. The processor transmits the contents of the serial packet only when a bit in the Serial Packet Register is set and the interval timer has elapsed.

For more information on the Serial Packet Register referenced in Table 4-1, refer to the *AMD Geode™ GX1 Processor Data Book*.

The CS5530A decodes the serial packet after each transmission and performs the power management tasks related to video retrace.

Table 4-1. GX1 Processor Serial Packet Register

Bit	Description
7	**Video IRQ:** This bit indicates the occurrence of a video vertical sync pulse. This bit is set at the same time that the VINT (Vertical Interrupt) bit gets set in the DC_TIMING_CFG register. The VINT bit has a corresponding enable bit (VIEN) in the DC_TIM_CFG register.
6	**CPU Activity:** This bit indicates the occurrence of a level 1 cache miss that was not a result of an instruction fetch. This bit has a corresponding enable bit in the PM_CNTL_TEN register.
5:2	**Reserved**
1	**Programmable Address Decode:** This bit indicates the occurrence of a programmable memory address decode. The bit is set based on the values of the PM_BASE register and the PM_MASK register. The PM_BASE register can be initialized to any address in the full CPU address range.
0	**Video Decode:** This bit indicates that the CPU has accessed either the display controller registers or the graphics memory region. This bit has a corresponding enable bit in the PM_CNTRL_TEN.

4.1.2.1 Video Retrace Interrupt

Bit 7 of the "Serial Packet" can be used to generate an SMI whenever a video retrace occurs within the processor. This function is normally not used for power management but for SoftVGA routines.

Setting F0 Index 83h[2] = 1 (bit details on page 164) enables this function. A read only status register located at F1BAR+Memory Offset 00h[5] (bit details on page 181) can be read to see if the SMI was caused by a video retrace event.

4.2 PCI Bus Interface

The PCI bus interface is compliant with the PCI Bus Specification Rev. 2.1.

The CS5530A acts as a PCI target for PCI cycles initiated by the processor or other PCI master devices, or as an initiator for DMA, ISA, IDE, and audio master transfer cycles. It supports positive decode for memory and I/O regions and is the subtractive decode agent on the PCI bus. The CS5530A also generates address and data parity and performs parity checking. A PCI bus arbiter is not part of the CS5530A; however, one is included in the GX1 processor.

The PCI Command Register, located at F0 Index 04h (Table 4-2), provides the basic control over the CS5530A's ability to respond and perform PCI bus accesses.

4.2.1 PCI Initiator

The CS5530A acts as a PCI bus master on behalf of the DMA controller or ISA, IDE, and audio interfaces. The REQ# and GNT# signals are used to arbitrate for the PCI bus.

Note: In a GX1 processor based system, the REQ#/GNT# signals of the CS5530A must connect to the REQ0#/GNT0# of the processor. This configuration ensures that the CS5530A is treated as a non-preemptable PCI master by the processor.

The CS5530A asserts REQ# in response to a bus mastering or DMA request for ownership of the PCI bus. GNT# is asserted by the PCI arbiter (i.e., processor) to indicate that access to the PCI bus has been granted to the CS5530A. The CS5530A then issues a grant to the DMA controller. This mechanism prevents any deadlock situations across the bridge. Once granted the PCI bus, the ISA master or DMA transfer commences.

If an ISA master executes an I/O access, that cycle remains on the ISA bus and is not forwarded to the PCI bus. The CS5530A performs only single transfers on the PCI bus for legacy DMA cycles.

Table 4-2. PCI Command Register

Bit	Description
F0 Index 04h-05h	**PCI Command Register (R/W)** **Reset Value = 000Fh**
15:10	**Reserved:** Set to 0.
9	**Fast Back-to-Back Enable (Read Only):** This function is not supported when the CS5530A is a master. It is always disabled (always reads 0).
8	**SERR#:** Allow SERR# assertion on detection of special errors. 0 = Disable **(Default)**; 1 = Enable.
7	**Wait Cycle Control (Read Only):** This function is not supported in the CS5530A. It is always disabled (always reads 0).
6	**Parity Error:** Allow the CS5530A to check for parity errors on PCI cycles for which it is a target, and to assert PERR# when a parity error is detected. 0 = Disable **(Default)**; 1 = Enable.
5	**VGA Palette Snoop Enable (Read Only):** This function is not supported in the CS5530A. It is always disabled (always reads 0).
4	**Memory Write and Invalidate:** Allow the CS5530A to do memory write and invalidate cycles, if the PCI Cache Line Size Register (F0 Index 0Ch) is set to 16 bytes (04h). 0 = Disable **(Default)**; 1 = Enable.
3	**Special Cycles:** Allow the CS5530A to respond to special cycles. 0 = Disable; 1 = Enable **(Default)**. This bit must be enabled to allow the CPU Warm Reset internal signal to be triggered from a CPU Shutdown cycle.
2	**Bus Master:** Allow the CS5530A bus mastering capabilities. 0 = Disable; 1 = Enable **(Default)**. This bit must be set to 1.
1	**Memory Space:** Allow the CS5530A to respond to memory cycles from the PCI bus. 0 = Disable; 1 = Enable **(Default)**.
0	**I/O Space:** Allow the CS5530A to respond to I/O cycles from the PCI bus. 0 = Disable; 1 = Enable **(Default)**.

4.2.2 PCI Target

The CS5530A positively decodes PCI transactions intended for any internal registers, the ROM address range, and several peripheral and user-defined address ranges. For positive-decoded transactions, the CS5530A is a medium responder. Table 4-3 lists the valid C/BE# encoding for PCI target transactions.

The CS5530A acts as the subtractive agent in the system since it contains the ISA bridge functionality. Subtractive decoding ensures that all accesses not positively claimed by PCI devices are forwarded to the ISA bus. The subtractive-decoding sample point can be configured as slow, default, or disabled via F0 Index 41h[2:1]. Table 4-4 shows these programming bits. Figure 4-4 shows the timing for subtractive decoding.

Note: I/O accesses that are mis-aligned so as to include address 0FFFFh and at least one byte beyond will "wrap" around to I/O address 0000h.

Table 4-3. PCI Command Encoding

C/BE[3:0]#	Command Type
0000	Interrupt Acknowledge
0001	Special Cycles: Shutdown, AD[15:0] = 0000
	Special Cycles: Halt, AD[15:0] = 0001
0010	I/O Read
0011	I/O Write
010x	Reserved
0110	Memory Read
0111	Memory Write
100x	Reserved
1010	Configuration Read
1011	Configuration Write
1100	Memory Read Multiple (memory read only)
1101	Reserved
1110	Memory Read Line (memory read only)
1111	Memory Write, Invalidate (memory write)

Table 4-4. Subtractive Decoding Related Bits

Bit	Description
F0 Index 41h	**PCI Function Control Register 2 (R/W)** **Reset Value = 10h**
2:1	**Subtractive Decode:** These bits determine the point at which the CS5530A accepts cycles that are not claimed by another device. The CS5530A defaults to taking subtractive decode cycles in the default cycle clock, but can be moved up to the Slow Decode cycle point if all other PCI devices decode in the fast or medium clocks. Disabling subtractive decode must be done with care, as all ISA and ROM cycles are decoded subtractively. 00 = Default sample (4th clock from FRAME# active) 01 = Slow sample (3rd clock from FRAME# active) 1x = No subtractive decode

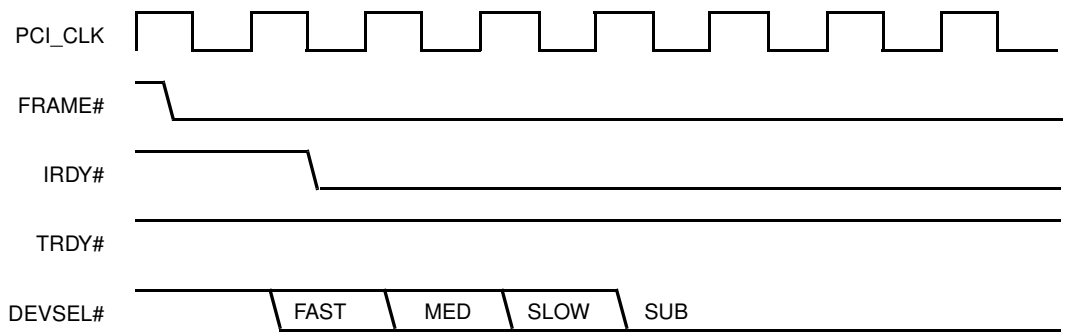


Figure 4-4. Subtractive Decoding Timing

4.2.3 Special Bus Cycles–Shutdown/Halt

The PCI interface does not pass Special Bus Cycles to the ISA interface, since special cycles by definition have no destination. However, the PCI interface monitors the PCI bus for Shutdown and Halt Special Bus Cycles.

Upon detection of a Shutdown Special Bus Cycle, a WM_RST SMI is generated after a delay of three PCI clock cycles. PCI Shutdown Special Cycles are detected when C/BE[3:0]# = 0001 during the address phase and AD[31:0] = xxxx0000h during the data phase. C/BE[3:0]# are also properly asserted during the data phase.

Upon detection of a Halt Special Bus Cycle, the CS5530A completes the cycle by asserting TRDY#. PCI Halt Special Bus Cycles are detected when CBE[3:0]# = 0001 during the address phase and AD[31:0] = xxxx0001h during the data phase of a Halt cycle. CBE[3:0]# are also properly asserted during the data phase.

4.2.4 PCI Bus Parity

When the CS5530A is the PCI initiator, it generates address parity for read and write cycles. It checks data parity for read cycles and it generates data parity for write cycles. The PAR signal is an even-parity bit that is calculated across 36 bits of AD[31:0] plus C/BE[3:0]#.

By default, the CS5530A does not report parity errors. However, the CS5530A detects parity errors during the data phase if F0 Index 04h[6] is set to 1. If enabled and a data parity error is detected, the CS5530A asserts PERR#. It also asserts SERR# if F0 Index 41h[5] is set to 1. This allows NMI generation.

The CS5530A also detects parity errors during the address phase if F0 Index 04h[6] is set. When parity errors are detected during the address phase, SERR# is asserted internally. Parity errors are reported to the CPU by enabling the SERR# source in I/O Port 061h (Port B) control register. The CS5530A sets the corresponding error bits in the PCI Status Register (F0 Index 06h[15:14]). Table 4-5 shows these programming bits.

If the CS5530A is the PCI master for a cycle and detects PERR# asserted, it generates SERR# internally.

Table 4-5. PERR#/SERR# Associated Register Bits

Bit	Description
F0 Index 04h-05h	**PCI Command Register (R/W)** **Reset Value = 000Fh**
6	**Parity Error:** Allow the CS5530A to check for parity errors on PCI cycles for which it is a target, and to assert PERR# when a parity error is detected. 0 = Disable **(Default)**; 1 = Enable.
F0 Index 06h-07h	**PCI Status Register (R/W)** **Reset Value = 0280h**
15	**Detected Parity Error:** This bit is set whenever a parity error is detected. Write 1 to clear.
14	**Signaled System Error:** This bit is set whenever the CS5530A asserts SERR# active. Write 1 to clear.
F0 Index 41h	**PCI Function Control Register 2 (R/W)** **Reset Value = 10h**
5	**PERR# Signals SERR#:** Assert SERR# any time that PERR# is asserted or detected active by the CS5530A (allows PERR# assertion to be cascaded to NMI (SMI) generation in the system). 0 = Disable; 1 = Enable.

4.2.5 PCI Interrupt Routing Support

The CS5530A allows the PCI interrupt signals INTA#, INTB#, INTC#, and INTD# (also know in industry terms as PIRQx#) to be mapped internally to any IRQ signal via register programming (shown in Table 4-6). Further details are supplied in Section 4.5.4.4 "PCI Compatible Interrupts" on page 103 regarding edge/level sensitivity selection.

4.2.6 Delayed Transactions

The CS5530A supports delayed transactions to prevent slow PCI cycles from occupying too much bandwidth and allows access for other PCI traffic.

Note: For systems which have only the GX1 processor and CS5530A on the PCI bus, system performance is improved if delayed transactions are disabled.

F0 Index 42h[5] and F0 Index 43h[1] are used to program this function. Table 4-7 shows these bit formats.

Table 4-6. PCI Interrupt Steering Registers

Bit	Description			
F0 Index 5Ch	**PCI Interrupt Steering Register 1 (R/W)**			**Reset Value = 00h**
7:4	**INTB# Target Interrupt:** Selects target interrupt for INTB#.			
	0000 = Disable	0100 = IRQ4	1000 = RSVD	1100 = IRQ12
	0001 = IRQ1	0101 = IRQ5	1001 = IRQ9	1101 = RSVD
	0010 = RSVD	0110 = IRQ6	1010 = IRQ10	1110 = IRQ14
	0011 = IRQ3	0111 = IRQ7	1011 = IRQ11	1111 = IRQ15
3:0	**INTA# Target Interrupt:** Selects target interrupt for INTA#.			
	0000 = Disable	0100 = IRQ4	1000 = RSVD	1100 = IRQ12
	0001 = IRQ1	0101 = IRQ5	1001 = IRQ9	1101 = RSVD
	0010 = RSVD	0110 = IRQ6	1010 = IRQ10	1110 = IRQ14
	0011 = IRQ3	0111 = IRQ7	1011 = IRQ11	1111 = IRQ15
Note: The target interrupt must first be configured as level sensitive via I/O Port 4D0h and 4D1h in order to maintain PCI interrupt compatibility.				
F0 Index 5Dh	**PCI Interrupt Steering Register 2 (R/W)**			**Reset Value = 00h**
7:4	**INTD# Target Interrupt:** Selects target interrupt for INTD#.			
	0000 = Disable	0100 = IRQ4	1000 = RSVD	1100 = IRQ12
	0001 = IRQ1	0101 = IRQ5	1001 = IRQ9	1101 = RSVD
	0010 = RSVD	0110 = IRQ6	1010 = IRQ10	1110 = IRQ14
	0011 = IRQ3	0111 = IRQ7	1011 = IRQ11	1111 = IRQ15
3:0	**INTC# Target Interrupt:** Selects target interrupt for INTC#.			
	0000 = Disable	0100 = IRQ4	1000 = RSVD	1100 = IRQ12
	0001 = IRQ1	0101 = IRQ5	1001 = IRQ9	1101 = RSVD
	0010 = RSVD	0110 = IRQ6	1010 = IRQ10	1110 = IRQ14
	0011 = IRQ3	0111 = IRQ7	1011 = IRQ11	1111 = IRQ15
Note: The target interrupt must first be configured as level sensitive via I/O Port 4D0h and 4D1h in order to maintain PCI interrupt compatibility.				

Table 4-7. Delay Transaction Programming Bits

Bit	Description	
F0 Index 42h	**PCI Function Control Register 3 (R/W)**	**Reset Value = ACh**
5	**Delayed Transactions:** Allow delayed transactions on the PCI bus. 0 = Disable; 1 = Enable. Also see F0 Index 43h[1].	
F0 Index 43h	**USB Shadow Register (R/W)**	**Reset Value = 03h**
1	**PCI Retry Cycles:** When the CS5530A is a PCI target and the PCI buffer is not empty, allow the PCI bus to retry cycles. 0 = Disable; 1 = Enable. This bit works in conjunction with PCI bus delayed transactions bit. F0 Index 42h[5] must = 1 for this bit to be valid.	

4.3 Resets and Clocks

The operations of resets and clocks in the CS5530A are described in this section of the Functional Description.

4.3.1 Resets

The CS5530A generates two reset signals, PCI_RST# to the PCI bus and CPU_RST to the GX1 processor. These resets are generated after approximately 100 µs delay from POR# active as depicted in Figure 4-5.

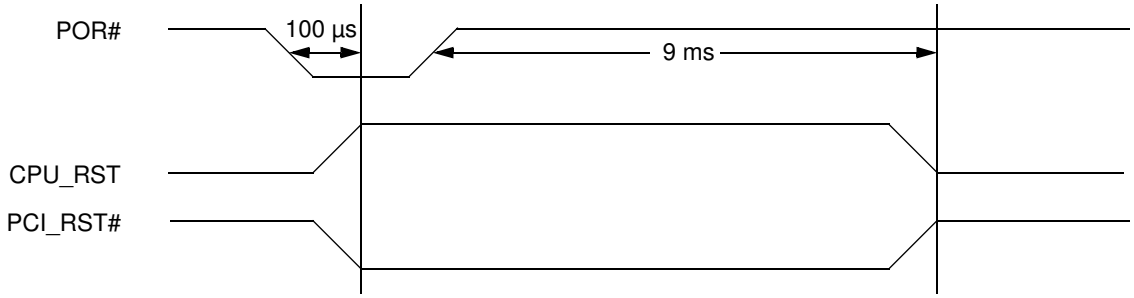
At any state, Power-on/Resume/Reset, the 14.31818 MHz oscillator must be active for the resets to function.

4.3.2 ISA Clock

The CS5530A creates the ISACLK from dividing the PCI-CLK. For ISA compatibility, the ISACLK nominally runs at 8.33 MHz or less. The ISACLK dividers are programmed via F0 Index 50h[2:0] as shown in Table 4-8.

Table 4-8. ISACLK Divider Bits

Bit	Description
F0 Index 50h	**PIT Control/ISA CLK Divider (R/W)** **Reset Value = 7Bh**
2:0	**ISA Clock Divisor:** Determines the divisor of the PCI clock used to make the ISA clock, which is typically programmed for approximately 8 MHz. 000 = Reserved 001 = Divide by two 010 = Divide by three 011 = Divide by four 100 = Divide by five 101 = Divide by six 110 = Divide by seven 111 = Divide by eight If 25 MHz PCI clock, use setting of 010 (divide by 3). If 30 or 33 MHz PCI clock, use a setting of 011 (divide by 4).



POR# minimum pulse width for CS5530A only (i.e., not a system specification) = 100 µs and 14 MHz must be running.

Figure 4-5. CS5530A Reset

4.3.3 DOT Clock

The DOT clock (DCLK) is generated from the 14.31818 MHz input (CLK_14MHZ). A combination of a phase locked loop (PLL), linear feedback shift register (LFSR) and divisors are used to generate the desired frequencies for the DOT clock. The divisors and LFSR are configurable through the F4BAR+Memory Offset 24h. The minimum frequency of DCLK is 10 MHz and the maximum is 200 MHz. However, system constraints limit DCLK to 150 MHz when DCLK is used as the graphics subsystem clock.

For applications that do not use the GX1 processor's graphics subsystem, this is an available clock for general purpose use.

The system clock distribution for a CS5530A/GX1 based system is shown in Figure 4-6.

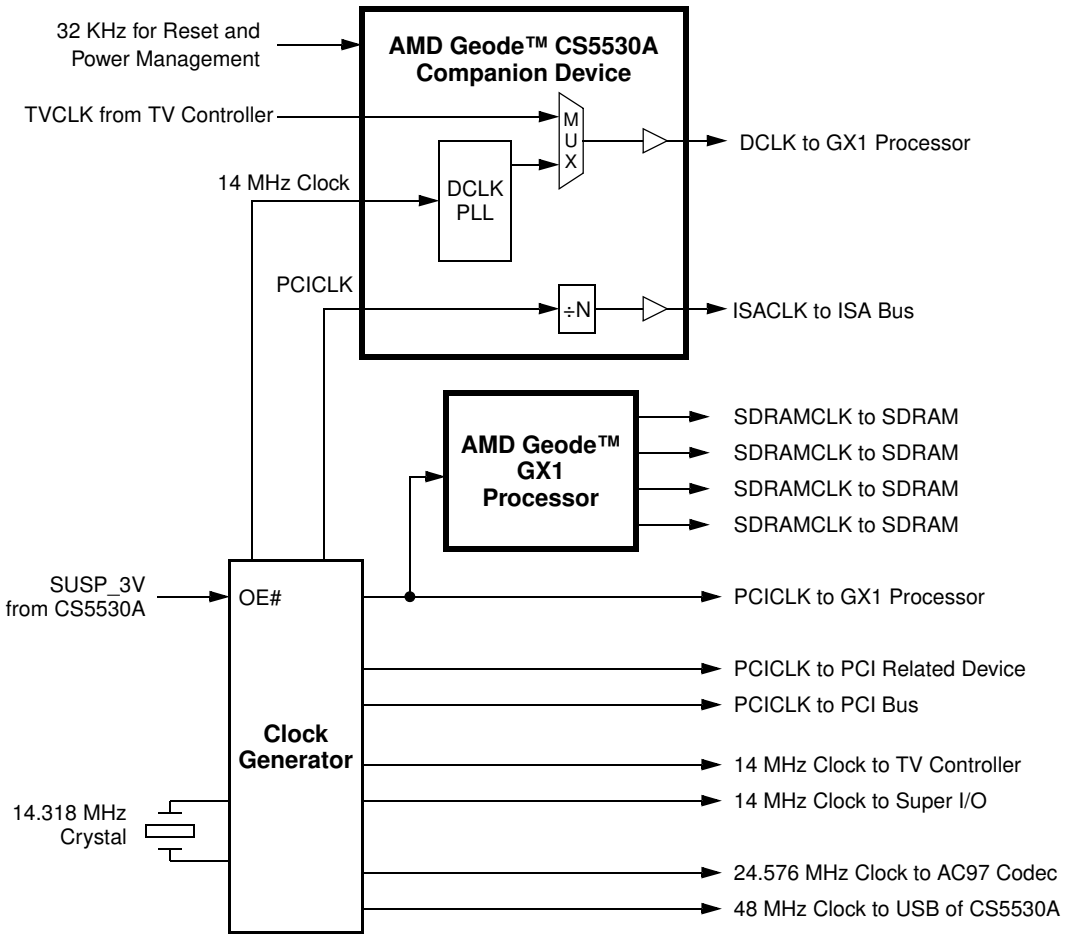


Figure 4-6. System Clock Distribution

4.3.3.1 DCLK Programming

The PLL contains an input divider (ID), feedback divider (FD) and a post divider (PD). The programming of the dividers is through F4BAR+Memory Offset 24h (see Table 4-9 on page 58). The maximum output frequency is 300 MHz. The output frequency is given by equation #1:

Equation #1:

DCLK = [CLK_14MHZ * FD] ÷ [PD *ID]

Condition:

140 MHz < [DCLK * PD] < 300 MHz

Where:

CLK_14MHZ is pin P24
FD is derived from N see equation #2 and #3:
PD is derived from bits [28:24]
ID is derived from bits [2:0]

Equation #2:

If FD is an odd number then: FD = 2*N +1

Equation #3:

If FD is an even number then: FD = 2*N +0

Where:

N is derived from bits [22:12]
+1 is achieved by setting bit 23 to 1.
+0 is achieved by clearing bit 23 to 0.

Example

Define Target Frequency:

Target frequency = 135 MHz

Satisfy the "Condition":

(140 MHz < [DCLK * PD] < 300 MHz)
140 MHz < [135 MHz * 2] < 300 MHz
Therefore PD = 2

Solve Equation #1:

DCLK = [CLK_14MHZ * FD] ÷ [PD *ID]
135 = [14.31818 * FD] ÷ [2 * ID]
135 = [7.159 * FD] ÷ ID
18.86 = FD ÷ ID
Guess: ID = 7, Solve for FD
FD = 132.02

Solve Equation #2 or #3:

FD = 2*N +1 for odd FD
FD = 2*N +0 for even FD
FD is 132, therefore even
132 = 2*N +0
N = 66

Summarize:

PD = 2: Bits [28:24] = 00111
ID = 7: Bits [2:0] = 101
N = 66: Bits [22:12] = 073h (found in Table 4-10), clear bit 23

Result:

DCLK = 135

The BIOS has been provided with a complete table of divisor values for supported graphics clock frequencies. Many combinations of divider values and VCO frequencies are possible to achieve a certain output clock frequency. These BIOS values may be adjusted from time to time to meet system frequency accuracy and jitter requirements. For applications that do not use the GX1 processor's graphics subsystem, this is an available clock for general purpose use.

The transition from one DCLK frequency to another is not guaranteed to be smooth or bounded; therefore, new divider coefficients should only be programmed while the PLL is off line in a situation where the transition characteristics of the clock are "don't care". The steps below describe (in order) how to change the DCLK frequency.

1) Program the new clock frequency.
2) Program Feedback Reset (bit 31) high and Bypass PLL (bit 8) high.
3) Wait at least 500 µs for PLL to settle.
4) Program Feedback Reset (bit 31) low.
5) Program Bypass PLL (bit 8) low.

Table 4-9. DCLK Configuration Register

Bit	Description
F4BAR+Memory Offset 24h-27h	**DOT Clock Configuration Register (R/W)**	**Reset Value = 00000000h**
31	**Feedback Reset:** Reset the PLL postscaler and feedback divider. 0 = Normal operation; 1 = Reset. A more comprehensive reset description is provided in bit 8.
30	**Half Clock:** 0 = Enable; 1 = Disable. For odd post divisors, half clock enables the falling edge of the VCO clock to be used to generate the falling edge of the post divider output to more closely approximate a 50% output duty cycle.
29	**Reserved:** Set to 0.
28:24	**5-Bit DCLK PLL Post Divisor (PD) Value:** Selects value of 1 to 31. 00000 = PD divisor of 8 — 01000 = PD divisor of 10 — 10000 = PD divisor of 9 — 11000 = PD divisor of 11 00001 = PD divisor of 6 — 01001 = PD divisor of 20 — 10001 = PD divisor of 7 — 11001 = PD divisor of 21 00010 = PD divisor of 18 — 01010 = PD divisor of 14 — 10010 = PD divisor of 19 — 11010 = PD divisor of 15 00011 = PD divisor of 4 — 01011 = PD divisor of 26 — 10011 = PD divisor of 5 — 11011 = PD divisor of 27 00100 = PD divisor of 12 — 01100 = PD divisor of 22 — 10100 = PD divisor of 13 — 11100 = PD divisor of 23 00101 = PD divisor of 16 — 01101 = PD divisor of 28 — 10101 = PD divisor of 17 — 11101 = PD divisor of 29 00110 = PD divisor of 24 — 01110 = PD divisor of 30 — 10110 = PD divisor of 25 — 11110 = PD divisor of 31 00111 = PD divisor of 2 — 01111 = PD divisor of 1* — 10111 = PD divisor of 3 — 11111 = Reserved *See bit 11 description.
23	**Plus 1 (+1):** Adds 1 or 0 to FD (DCLK PLL VCO Feedback Divisor) parameter in equation (see Note). 0 = Add 0 to FD; 1 = Add 1 to FD.
22:12	**N:** This bit represents “N” in the equation (see Note). It is used to solve the value of FD (DCLK PLL VCO feedback divisor). N can be a value of 1 to 400. For all values of N, refer to Table 4-10 on page 59.
11	**CLK_ON:** 0 = PLL disable; 1 = PLL enable. If PD = 1 (i.e., bits [28:24] = 01111) the PLL is always enabled and cannot be disabled by this bit.
10	**DOT Clock Select:** 0 = DCLK; 1 = TV_CLK.
9	**Reserved:** Set to 0
8	**Bypass PLL:** Connects the input of the PLL directly to the output of the PLL. 0 = Normal Operation; 1 = Bypass PLL. If this bit is set to 1, the input of the PLL bypasses the PLL and resets the VCO control voltage, which in turn powers down the PLL. Allow 0.5 ms for the control voltage to be driven to 0V.
7:6	**Reserved:** Set to 0.
5	**Reserved (Read Only):** Write as read
4:3	**Reserved:** Set to 0.
2:0	**PLL Input Divide (ID) Value:** Selects value of 2 to 9 (see Note). 000 = ID divisor of 2 — 100 = ID divisor of 6 — 001 = ID divisor of 3 — 101 = ID divisor of 7 010 = ID divisor of 4 — 110 = ID divisor of 8 — 011 = ID divisor of 5 — 111 = ID divisor of 9
Note:	To calculate DCLK output frequency: Equation #1: DCLK = [CLK_14MHZ * FD] ÷ [PD *ID] Condition: 140 MHz < [DCLK * PD] < 300 MHz Where: CLK_14MHZ is pin P24 FD is derived from N see equation #2 and #3 PD is derived from bits [28:24] ID is derived from bits [2:0] Equation #2: If FD is an odd number then: FD = 2*N +1 Equation #3: If FD is an even number then: FD = 2*N +0 Where: N is derived from bits [22:12] +1 is achieved by setting bit 23 to 1. +0 is achieved by clearing bit 23 to 0.

Table 4-10. F4BAR+Memory Offset 24h[22:12] Decode (Value of "N")

N	Reg. Value	N	Reg. Value	N	Reg. Value	N	Reg. Value	N	Reg. Value	N	Reg. Value	N	Reg. Value	N	Reg. Value
400	33A	349	23	298	331	247	7D0	196	143	145	551	94	19E	43	161
399	674	348	47	297	662	246	7A1	195	286	144	2A3	93	33C	42	2C2
398	4E8	347	8F	296	4C4	245	743	194	50D	143	547	92	678	41	585
397	1D0	346	11F	295	188	244	687	193	21B	142	28F	91	4F0	40	30B
396	3A0	345	23E	294	310	243	50E	192	437	141	51F	90	1E0	39	616
395	740	344	47D	293	620	242	21D	191	6E	140	23F	89	3C0	38	42C
394	681	343	FA	292	440	241	43B	190	DD	139	47F	88	780	37	58
393	502	342	1F5	291	80	240	76	189	1BB	138	FE	87	701	36	B1
392	205	341	3EA	290	101	239	ED	188	376	137	1FD	86	603	35	163
391	40B	340	7D4	289	202	238	1DB	187	6EC	136	3FA	85	406	34	2C6
390	16	339	7A9	288	405	237	3B6	186	5D8	135	7F4	84	C	33	58D
389	2D	338	753	287	A	236	76C	185	3B1	134	7E9	83	19	32	31B
388	5B	337	6A7	286	15	235	6D9	184	762	133	7D3	82	33	31	636
387	B7	336	54E	285	2B	234	5B2	183	6C5	132	7A7	81	67	30	46C
386	16F	335	29D	284	57	233	365	182	58A	131	74F	80	CF	29	D8
385	2DE	334	53B	283	AF	232	6CA	181	315	130	69F	79	19F	28	1B1
384	5BD	333	277	282	15F	231	594	180	62A	129	53E	78	33E	27	362
383	37B	332	4EF	281	2BE	230	329	179	454	128	27D	77	67C	26	6C4
382	6F6	331	1DE	280	57D	229	652	178	A8	127	4FB	76	4F8	25	588
381	5EC	330	3BC	279	2FB	228	4A4	177	151	126	1F6	75	1F0	24	311
380	3D9	329	778	278	5F7	227	148	176	2A2	125	3EC	74	3E0	23	622
379	7B2	328	6F1	277	3EF	226	290	175	545	124	7D8	73	7C0	22	444
378	765	327	5E2	276	7DE	225	521	174	28B	123	7B1	72	781	21	88
377	6CB	326	3C5	275	7BD	224	243	173	517	122	763	71	703	20	111
376	596	325	78A	274	77B	223	487	172	22F	121	6C7	70	607	19	222
375	32D	324	715	273	6F7	222	10E	171	45F	120	58E	69	40E	18	445
374	65A	323	62B	272	5EE	221	21C	170	BE	119	31D	68	1C	17	8A
373	4B4	322	456	271	3DD	220	439	169	17D	118	63A	67	39	16	115
372	168	321	AC	270	7BA	219	72	168	2FA	117	474	66	73	15	22A
371	2D0	320	159	269	775	218	E5	167	5F5	116	E8	65	E7	14	455
370	5A1	319	2B2	268	6EB	217	1CB	166	3EB	115	1D1	64	1CF	13	AA
369	343	318	565	267	5D6	216	396	165	7D6	114	3A2	63	39E	12	155
368	686	317	2CB	266	3AD	215	72C	164	7AD	113	744	62	73C	11	2AA
367	50C	316	597	265	75A	214	659	163	75B	112	689	61	679	10	555
366	219	315	32F	264	6B5	213	4B2	162	6B7	111	512	60	4F2	9	2AB
365	433	314	65E	263	56A	212	164	161	56E	110	225	59	1E4	8	557
364	66	313	4BC	262	2D5	211	2C8	160	2DD	109	44B	58	3C8	7	2AF
363	CD	312	178	261	5AB	210	591	159	5BB	108	96	57	790	6	55F
362	19B	311	2F0	260	357	209	323	158	377	107	12D	56	721	5	2BF
361	336	310	5E1	259	6AE	208	646	157	6EE	106	25A	55	643	4	57F
360	66C	309	3C3	258	55C	207	48C	156	5DC	105	4B5	54	486	3	2FF
359	4D8	308	786	257	2B9	206	118	155	3B9	104	16A	53	10C	2	5FF
358	1B0	307	70D	256	573	205	230	154	772	103	2D4	52	218	1	3FF
357	360	306	61B	255	2E7	204	461	153	6E5	102	5A9	51	431		
356	6C0	305	436	254	5CF	203	C2	152	5CA	101	353	50	62		
355	580	304	6C	253	39F	202	185	151	395	100	6A6	49	C5		
354	301	303	D9	252	73E	201	30A	150	72A	99	54C	48	18B		
353	602	302	1B3	251	67D	200	614	149	655	98	299	47	316		
352	404	301	366	250	4FA	199	428	148	4AA	97	533	46	62C		
351	8	300	6CC	249	1F4	198	50	147	154	96	267	45	458		
350	11	299	598	248	3E8	197	A1	146	2A8	95	4CF	44	B0		

4.4 Power Management

The hardware resources provided by a combined CS5530A/GX1 based system support a full-featured power management implementation. The extent to which these resources are employed depends on the application and the discretion of the system designer.

Power management resources can be grouped according to the function they enable or support. The major functions are as follows:

- CPU Power Management
  - — On
  - — Active Idle
  - — Suspend
  - — 3 Volt Suspend
  - — Off
  - — Save-to-Disk/Save-to-RAM
  - — Suspend Modulation
- APM Support
- Peripheral Power Management
  - — Device Idle Timers and Traps
  - — General Purpose Timers
  - — ACPI Timer Register
  - — General Purpose I/O Pins
  - — Power Management SMI Status Reporting Registers
  - — Device Power Management Register Programming Summary

Included in the following subsections are details regarding the registers used for configuring power management features. The majority of these registers are directly accessed through the PCI configuration register space designated as Function 0 (F0). However, included in the discussions are references to F1BAR+Memory Offset 10h. This refers to the registers accessed through a base address register in Function 1 (F1) at Index 10h (F1BAR). F1BAR sets the base address for the SMI status and ACPI timer support registers as shown in Table 3-11.

4.4.1 CPU Power Management

The three greatest power consumers in a system are the display, hard drive, and CPU. The power management of the first two is relatively straightforward and is discussed in Section 4.4.3 "Peripheral Power Management" on page 67. CPU power management is supported through several mechanisms resulting in five defined system power conditions:

- On
- Active Idle
- Suspend
- 3 Volt Suspend
- Off

There are also three derivative power conditions defined:

- Suspend Modulation
  - — Combination of On and Suspend
- Save-to-Disk
  - — Off with the ability to return back to the exact system condition without rebooting
- Save-to-RAM
  - — Extreme 3 Volt Suspend with only the contents of RAM still powered

4.4.1.1 On

System is running and the CPU is actively executing code.

Table 4-11. Base Address Register (F1BAR) for SMI Status and ACPI Timer Support

Bit	Description
F1 Index 10h-13h	**Base Address Register — F1BAR (R/W)** **Reset Value = 00000000h**
This register sets the base address of the memory mapped SMI status and ACPI timer related registers. Bits [7:0] are read only (00h), indicating a 256-byte memory address range. Refer to Table 5-16 for the SMI status and ACPI timer registers bit formats and reset values. The upper 16 bytes are always mapped to the ACPI timer, and are always memory mapped. **Note:** The ACPI Timer Count Register is accessible through F1BAR+Memory Offset 1Ch and I/O Port 121Ch.	
31:8	**SMI Status/Power Management Base Address**
7:0	**Address Range (Read Only)**

4.4.1.2 Active Idle

This state is the most powerful power management state because it is an operational state. The CPU has executed a HLT instruction and has asserted the SUSPA# signal. The operating system has control of the entry of this state because the OS has either executed the HLT or made a BIOS call to indicate idle, and the BIOS executed the HLT instruction. The display refresh subsystem is still active but the CPU is not executing code. The clock is stopped to the processing core in this state and considerable power is saved in the processor. The CS5530A takes advantage of this power state by stopping the clock to some of the internal circuitry. This power saving mode can be enabled/disabled by programming F0 Index 96h[4] (see Table 4-12). The CS5530A can still make bus master requests for IDE, audio, USB, and ISA from this state. When the CS5530A or any other device on the PCI bus asserts REQ#, the CPU deasserts SUSPA# for the duration of REQ# activity. Once REQ# has gone inactive and all PCI cycles have stopped, the CPU reasserts SUSPA#. SUSPA# remains active until the CPU receives an INTR or SMI event which ends the CPU halt condition.

4.4.1.3 Suspend

This state is similar to the Active Idle state except that the CPU enters this state because the CS5530A asserted SUSP#. The CS5530A deasserts SUSP# when an INTR or SMI event occurs. The Suspend Configuration register is shown in Table 4-12, however, also see the tables listed below for a more complete understanding on configuring the Suspend state.

- F0 Index BCh in Table 4-13 "Clock Stop Control Register" on page 62.
- Related registers in Table 4-14 "Suspend Modulation Related Registers" on page 64.
- F0 Index AEh in Table 4-16 "APM Support Registers" on page 67.

Table 4-12. Suspend Configuration Register

Bit	Description
F0 Index 96h	**Suspend Configuration Register (R/W)** **Reset Value = 00h**
7:5	**Reserved:** Set to 0.
4	**Power Savings Mode:** 0 = Enable; 1 = Disable.
3	**Include ISA Clock in Power Savings Mode:** 0 = ISA clock not included; 1 = ISA clock included.
2	**Suspend Mode Configuration:** “Special 3 Volt Suspend” mode to support powering down a GX1 processor during Suspend. 0 = Disable; 1 = Enable.
1	**SMI Speedup Configuration:** Selects how Suspend Modulation function reacts when an SMI occurs. 0 = Use the IRQ Speedup Timer Count Register (F0 Index 8Ch) to temporarily disable Suspend Modulation when an SMI occurs. 1 = Disable Suspend Modulation when an SMI occurs until a read to the SMI Speedup Disable Register (F1BAR+Memory Offset 08h). The purpose of this bit is to disable Suspend Modulation while the CPU is in the System Management Mode so that VSA technology and power management operations occur at full speed. Two methods for accomplishing this are either to map the SMI into the IRQ Speedup Timer Count Register (F0 Index 8Ch), or to have the SMI disable Suspend Modulation until the SMI handler reads the SMI Speedup Disable Register (F1BAR+Memory Offset 08h). The latter is the preferred method. The IRQ speedup method is provided for software compatibility with earlier revisions of the CS5530A. This bit has no effect if the Suspend Modulation feature is disabled (bit 0 = 0).
0	**Suspend Modulation Feature:** 0 = Disable; 1 = Enable. When enabled, the SUSP# pin will be asserted and deasserted for the durations programmed in the Suspend Modulation OFF/ON Count Registers (F0 Index 94h/95h).

4.4.1.4 3 Volt Suspend

This state is a non-operational state. To enter this state the display must have been previously turned off. This state is usually used to put the system into a deep sleep to conserve power and still allow the user to resume where they left off.

The CS5530A supports the stopping of the CPU and system clocks for a 3 Volt Suspend state. If appropriately configured, via the Clock Stop Control Register (F0 Index BCh, see Table 4-13), the CS5530A asserts the SUSP_3V pin after it has gone through the SUSP#/SUSPA# handshake. The SUSP_3V pin is a state indicator, indicating that the system is in a low-activity state. This indicator can be used to put the system into a low-power state (the system clock can be turned off).

The SUSP_3V pin is intended to be connected to the output enable of a clock generator or buffer chip, so that the clocks to the CPU and the CS5530A (and most other system devices) are stopped. The CS5530A continues to decrement all of its device timers and respond to external SMI interrupts after the input clock has been stopped, as long as the 32 KHz clock continues to oscillate. Any SMI event or unmasked interrupt pin causes the CS5530A to deassert the SUSP_3V pin, restarting the system clocks. As the CPU or other device might include a PLL, the CS5530A holds SUSP# active for a pre-programmed period of delay (the PLL re-sync delay) that varies from 0 to 15 ms. After this period has expired, the CS5530A deasserts SUSP#, stopping Suspend. SMI# is held active for the entire period, so that the CPU reenters SMM when the clocks are restarted.

Note: The SUSP_3V pin can be active either high or low. The pin is an input during POR, and is sampled to determine its inactive state. This allows a designer to match the active state of SUSP_3V to the inactive state for a clock driver output enable with a pull-up or pull-down resistor.

4.4.1.5 Off

The system is off and there is no power being consumed by the processor or the CS5530A.

Table 4-13. Clock Stop Control Register

Bit	Description
F0 Index BCh	**Clock Stop Control Register (R/W)** — **Reset Value = 00h**
7:4	**PLL Delay:** The programmed value in this field sets the delay (in milliseconds) after a break event occurs before the SUSP# pin is deasserted to the CPU. This delay is designed to allow the clock chip and CPU PLL to stabilize before starting execution. This delay is only invoked if the STP_CLK bit (bit 0) was set. The four-bit field allows values from 0 to 15 ms. 0000 = 0 ms, 0100 = 4 ms, 1000 = 8 ms, 1100 = 12 ms 0001 = 1 ms, 0101 = 5 ms, 1001 = 9 ms, 1101 = 13 ms 0010 = 2 ms, 0110 = 6 ms, 1010 = 10 ms, 1110 = 14 ms 0011 = 3 ms, 0111 = 7 ms, 1011 = 11 ms, 1111 = 15 ms
3:1	**Reserved:** Set to 0.
0	**CPU Clock Stop:** 0 = Normal SUSP#/ SUSPA# handshake; 1 = Full system Suspend.

Note: This register configures the CS5530A to support a 3 Volt Suspend. Setting bit 0 causes the SUSP_3V pin to assert after the appropriate conditions, stopping the system clocks. A delay of 0 to 15 ms is programmable (bits 7:4) to allow for a delay for the clock chip and CPU PLL to stabilize when an event Resumes the system.

A write to the CPU Suspend Command Register (F0 Index AEh) with bit 0 written as:

0 = SUSP#/SUSPA# handshake occurs. The CPU is put into a low-power state, and the system clocks are not stopped. When a break/resume event occurs, it releases the CPU halt condition.

1 = SUSP#/SUSPA# handshake occurs and the SUSP_3V pin is asserted, thus invoking a full system Suspend (both CPU and system clocks are stopped). When a break event occurs, the SUSP_3V pin will deassert, the PLL delay programmed in bits [7:4] will be invoked which allows the clock chip and CPU PLL to stabilize before deasserting the SUSP# pin.

4.4.1.6 Suspend Modulation

Suspend Modulation is a derivative of the On and Suspend states and works by asserting and de-asserting the SUSP# pin to the CPU for a configurable period and duty cycle. By modulating the SUSP# pin, an effective reduction in frequency is achieved. Suspend Modulation is the system power management choice of last resort. However, it is an excellent choice for thermal management. If the system is expected to operate in a thermal environment where the processor could overheat, then Suspend Modulation could be used to reduce power consumption in the overheated condition and thus reduce the processor's temperature.

When used as a power management state, Suspend Modulation works by assuming that the processor is idle unless external activity indicates otherwise. This approach effectively slows down the processor until external activity indicates a need to run at full speed, thereby reducing power consumption.

Suspend Modulation serves as the primary CPU power management mechanism when APM or some other power management software strategy is not present. It can also act as a backup for situations where the power management scheme does not correctly detect an Idle condition in the system.

In order to provide high-speed performance when needed, the SUSP# pin modulation can be temporarily disabled any time system activity is detected. When this happens, the processor is "instantly" converted to full speed for a programmed duration. System activities in the CS5530A are defined in hardware as: any unmasked IRQ, accessing Port 061h, SMI, and/or accessing the graphics controller. Since the graphics controller is integrated in the GX1 processor, the indication of graphics activity is sent to the CS5530A via the serial link (see Section 4.1.2 "PSERIAL Pin Interface" on page 50 for more information on serial link) and is automatically decoded. Graphics activity is defined as any access to the VGA register space, the VGA frame buffer, the graphics accelerator control registers and the configured graphics frame buffer.

The automatic speedup events (IRQ, SMI, and/or graphics) for Suspend Modulation should be used together with software-controlled speedup registers for major I/O events such as any access to the floppy disk controller, hard disk drive, or parallel/serial ports, since these are indications of major system activities. When major I/O events occur, Suspend Modulation can be temporarily disabled using the procedures described in the following subsections.

Bus master internal (Ultra DMA/33, Audio, USB, or ISA) or external requests do not directly affect the Suspend Modulation programming.

Configuring Suspend Modulation

Control of the Suspend Modulation feature is accomplished using the Suspend Modulation OFF Count Register, the Suspend Modulation ON Count Register, and the Suspend Configuration Register (F0 Index 94h, 95h, and 96h, respectively).

The Power Management Enable Register 1 (F0 Index 80h) contains the enables for the individual activity speedup timers.

Bit 0 of the Suspend Configuration Register (F0 Index 96h) enables the Suspend Modulation feature. Bit 1 controls how SMI events affect the Suspend Modulation feature. In general this bit should be set to a 1, which causes SMIs to disable Suspend Modulation until it is re-enabled by the SMI handler.

The Suspend Modulation OFF and ON Count Registers (F0 Index 94h and 95h) control two 8-bit counters that represent the number of 32 µs intervals that the SUSP# pin is asserted and then deasserted to the processor. These counters define a ratio which is the effective frequency of operation of the system while Suspend Modulation is enabled.

$$F_{eff} = F_{GX86} \times \frac{\text{Off Count}}{\text{On Count + Off Count}}$$

The IRQ and Video Speedup Timer Count registers (F0 Index 8Ch and 8Dh) configure the amount of time which Suspend Modulation is disabled when the respective events occur.

SMI Speedup Disable

If the Suspend Modulation feature is being used for CPU power management, the occurrence of an SMI disables the Suspend Modulation function so that the system operates at full speed while in SMM. There are two methods used to invoke this via bit 1 of the Suspend Configuration Register.

If F0 Index 96h[1] = 0: Use the IRQ Speedup Timer (F0 Index 8Ch) to temporarily disable Suspend Modulation when an SMI occurs.

If F0 Index 96h[1] = 1: Disable Suspend Modulation when an SMI occurs until a read to the SMI Speedup Disable Register (F1BAR+Memory Offset 08h).

The SMI Speedup Disable Register prevents VSA technology software from entering Suspend Modulation while operating in SMM. The data read from this register can be ignored. If the Suspend Modulation feature is disabled, reading this I/O location has no effect.

Table 4-14 shows the bit formats of the Suspend Modulation related registers.

Table 4-14. Suspend Modulation Related Registers

Bit	Description
F0 Index 80h	**Power Management Enable Register 1 (R/W)** **Reset Value = 00h**
4	**Video Speedup:** Any video activity, as decoded from the serial connection (PSERIAL register, bit 0) from the GX1 processor disables clock throttling (via SUSP#/SUSPA# handshake) for a configurable duration when the system is power managed using CPU Suspend modulation. 0 = Disable; 1 = Enable. The duration of the speedup is configured in the Video Speedup Timer Count Register (F0 Index 8Dh). Detection of an external VGA access (3Bxh, 3Cxh, 3Dxh and A000h-B7FFh) on the PCI bus is also supported. This configuration is non-standard, but it does allow the power management routines to support an external VGA chip.
3	**IRQ Speedup:** Any unmasked IRQ (per I/O Port 021h/0A1h) or SMI disables clock throttling (via SUSP#/SUSPA# handshake) for a configurable duration when the system is power managed using CPU Suspend modulation. 0 = Disable; 1 = Enable. The duration of the speedup is configured in the IRQ Speedup Timer Count Register (F0 Index 8Ch).
F0 Index 8Ch	**IRQ Speedup Timer Count Register (R/W)** **Reset Value = 00h**
7:0	**IRQ Speedup Timer Count:** This register holds the load value for the IRQ speedup timer. It is loaded into the timer when Suspend Modulation is enabled (F0 Index 96h[0] = 1) and an INTR or an access to I/O Port 061h occurs. When the event occurs, the Suspend Modulation logic is inhibited, permitting full performance operation of the CPU. Upon expiration, no SMI is generated; the Suspend Modulation begins again. The IRQ speedup timer's timebase is 1 ms. This speedup mechanism allows instantaneous response to system interrupts for full-speed interrupt processing. A typical value here would be 2 to 4 ms.
F0 Index 8Dh	**Video Speedup Timer Count Register (R/W)** **Reset Value = 00h**
7:0	**Video Speedup Timer Count:** This register holds the load value for the Video speedup timer. It is loaded into the timer when Suspend Modulation is enabled (F0 Index 96h[0] = 1) and any access to the graphics controller occurs. When a video access occurs, the Suspend Modulation logic is inhibited, permitting full-performance operation of the CPU. Upon expiration, no SMI is generated; the Suspend Modulation begins again. The video speedup timer's timebase is 1 ms. This speedup mechanism allows instantaneous response to video activity for full speed during video processing calculations. A typical value here would be 50 to 100 ms.
Index 94h	**Suspend Modulation OFF Count Register (R/W)** **Reset Value = 00h**
7:0	**Suspend Signal Deasserted Count:** This 8-bit value represents the number of 32 µs intervals that the SUSP# pin will be deasserted to the GX1 processor. This timer, together with the Suspend Modulation ON Count Register (F0 Index 95h), perform the Suspend Modulation function for CPU power management. The ratio of the on-to-off count sets up an effective (emulated) clock frequency, allowing the power manager to reduce CPU power consumption. This timer is prematurely reset if an enabled speedup event occurs. The speedup events are IRQ speedups and video speedups.
Index 95h	**Suspend Modulation ON Count Register (R/W)** **Reset Value = 00h**
7:0	**Suspend Signal Asserted Count:** This 8-bit value represents the number of 32 µs intervals that the SUSP# pin will be asserted. This timer, together with the Suspend Modulation OFF Count Register (F0 Index 94h), perform the Suspend Modulation function for CPU power management. The ratio of the on-to-off count sets up an effective (emulated) clock frequency, allowing the power manager to reduce CPU power consumption. This timer is prematurely reset if an enabled speedup event occurs. The speedup events are IRQ speedups and video speedups.

Table 4-14. Suspend Modulation Related Registers (Continued)

Bit	Description
Index 96h	**Suspend Configuration Register (R/W)** **Reset Value = 00h**
7:5	**Reserved:** Set to 0.
4	**Power Savings:** 0 = Enable; 1 = Disable.
3	**Include ISA Clock in Power Savings Mode:** 0 = ISA clock not included; 1 = ISA clock included.
2	**Suspend Mode Configuration:** "Special 3 Volt Suspend" mode to support powering down a GX1 processor during Suspend. 0 = Disable; 1 = Enable.
1	**SMI Speedup Configuration:** Selects how Suspend Modulation function reacts when an SMI occurs. 0 = Use the IRQ Speedup Timer Count Register (F0 Index 8Ch) to temporarily disable Suspend Modulation when an SMI occurs. 1 = Disable Suspend Modulation when an SMI occurs until a read to the SMI Speedup Disable Register (F1BAR+Memory Offset 08h). The purpose of this bit is to disable Suspend Modulation while the CPU is in the System Management Mode so that VSA technology and power management operations occur at full speed. Two methods for accomplishing this are either to map the SMI into the IRQ Speedup Timer Count Register (F0 Index 8Ch), or to have the SMI disable Suspend Modulation until the SMI handler reads the SMI Speedup Disable Register (F1BAR+Memory Offset 08h). The latter is the preferred method. The IRQ speedup method is provided for software compatibility with earlier revisions of the CS5530A. This bit has no effect if the Suspend Modulation feature is disabled (bit 0 = 0).
0	**Suspend Modulation Feature:** 0 = Disable; 1 = Enable. When enabled, the SUSP# pin will be asserted and deasserted for the durations programmed in the Suspend Modulation OFF/ON Count Registers (F0 Index 94h/95h).
F0 Index A8h-A9h	**Video Overflow Count Register (R/W)** **Reset Value = 0000h**
15:0	**Video Overflow Count:** Each time the Video Speedup timer (F0 Index 8Dh) is triggered, a 100 ms timer is started. If the 100 ms timer expires before the Video Speedup timer lapses, the Video Overflow Count Register increments and the 100 ms timer re-triggers. Software clears the overflow register when new evaluations are to begin. The count contained in this register may be combined with other data to determine the type of video accesses present in the system.
F1BAR+Memory Offset 08h-09h	**SMI Speedup Disable Register (Read to Enable)** **Reset Value = 0000h**
15:0	**SMI Speedup Disable:** If bit 1 in the Suspend Configuration Register is set (F0 Index 96h[1] = 1), a read of this register invokes the SMI handler to re-enable Suspend Modulation. The data read from this register can be ignored. If the Suspend Modulation feature is disabled, reading this I/O location has no effect.

4.4.1.7 Save-to-Disk/Save-to-RAM

This is a derivative of the Off state. The processor and the CS5530A have the capability to save their complete state. This state information can be saved to a hard disk or to RAM and the system can be turned off. When powered back on, the system can be returned exactly back to the state it was in when the save process began. This means that the system does not have to be rebooted in the traditional sense. In both cases, precautions must be taken in the system design to make sure that there is sufficient space on the hard drive or RAM to store the information. In the case of the RAM, it must also be powered at all times and can not be corrupted when the system is powered off and back on.

The PC/AT compatible floppy port is not part of the CS5530A. If a floppy is attached on the ISA bus in a SuperI/O or by some other means, some of the FDC registers are shadowed in the CS5530A because they cannot be safely read. The FDC registers are shown in Table 4-15. Additional shadow registers for other functions are described in:

- Table 4-40 "DMA Shadow Register" on page 98
- Table 4-42 "PIT Shadow Register" on page 100
- Table 4-45 "PIC Shadow Register" on page 102
- Table 4-53 "Real-Time Clock Registers" on page 109

Table 4-15. Power Management Shadow Registers

Bit	Description
F0 Index B4h	**Floppy Port 3F2h Shadow Register (RO)** **Reset Value = xxh**
7:0	**Floppy Port 3F2h Shadow (Read Only):** Last written value of I/O Port 3F2h. Required for support of FDC power ON/OFF and Save-to-Disk/RAM coherency. This register is a copy of an I/O register which cannot safely be directly read. Value in register is not deterministic of when the register is being read. It is provided here to assist in a Save-to-Disk operation.
F0 Index B5h	**Floppy Port 3F7h Shadow Register (RO)** **Reset Value = xxh**
7:0	**Floppy Port 3F7h Shadow (Read Only):** Last written value of I/O Port 3F7h. Required for support of FDC power ON/OFF and Save-to-Disk/RAM coherency. This register is a copy of an I/O register which cannot safely be directly read. Value in register is not deterministic of when the register is being read. It is provided here to assist in a Save-to-Disk operation.
F0 Index B6h	**Floppy Port 1F2h Shadow Register (RO)** **Reset Value = xxh**
7:0	**Floppy Port 1F2h Shadow (Read Only):** Last written value of I/O Port 1F2h. Required for support of FDC power ON/OFF and Save-to-Disk/RAM coherency. This register is a copy of an I/O register which cannot safely be directly read. Value in register is not deterministic of when the register is being read. It is provided here to assist in a Save-to-Disk operation.
F0 Index B7h	**Floppy Port 1F7h Shadow Register (RO)** **Reset Value = xxh**
7:0	**Floppy Port 1F7h Shadow (Read Only):** Last written value of I/O Port 1F7h. Required for support of FDC power ON/OFF and Save-to-Disk/RAM coherency. This register is a copy of an I/O register which cannot safely be directly read. Value in register is not deterministic of when the register is being read. It is provided here to assist in a Save-to-Disk operation.

4.4.2 APM Support

Some IA systems rely solely on an APM (Advanced Power Management) driver for enabling the operating system to power-manage the CPU. APM provides several services which enhance the system power management and is theoretically the best approach; but in its current form, APM is imperfect for the following reasons:

- APM is an OS-specific driver, and may not be available for some operating systems.
- Application support is inconsistent. Some applications in foreground may prevent Idle calls.
- APM does not help with Suspend determination or peripheral power management.

The CS5530A provides two entry points for APM support:

- Software CPU Suspend control via the CPU Suspend Command Register (F0 Index AEh)
- Software SMI entry via the Software SMI Register (F0 Index D0h). This allows the APM BIOS to be part of the SMI handler.

These registers are shown in Table 4-16.

4.4.3 Peripheral Power Management

The CS5530A provides peripheral power management using a combination of device idle timers, address traps, and general purpose I/O pins. Idle timers are used in conjunction with traps to support powering down peripheral devices. Eight programmable GPIO (general purpose I/O) pins are included for external device power control as well as other functions. All I/O addresses are decoded in 16 bits. All memory addresses are decoded in 32 bits.

4.4.3.1 Device Idle Timers and Traps

Idle timers are used to power manage a peripheral by determining when the peripheral has been inactive for a specified period of time, and removing power from the peripheral at the end of that time period.

Idle timers are provided for the commonly-used peripherals (FDC, IDE, parallel/serial ports, and mouse/keyboard). In addition, there are three user-defined timers that can be configured for either I/O or memory ranges. The Power Management enable bit (F0 Index 80h[1]) enables and disables the power management idle timers. The Trap bit in the same register (F0 Index 80h[2]) enables and disables device I/O traps.

The idle timers are 16-bit countdown timers with a 1 second time base, providing a time-out range of 1 to 65536 seconds (1092 minutes) (18 hours). General purpose timers can be programmed to count milliseconds instead of seconds (see Section 4.4.3.2 on page 77 for further information on general purpose timers).

When the idle timers are enabled, the timers are loaded from the timer count registers and start to decrement at the next timebase clock, but cannot trigger an interrupt on that cycle. If an idle timer is initially set to 1, it decrements to 0 on the first cycle and continues counting with 65535 on the next cycle. Starting at 2 gives 1 on the first cycle, and 0 on the second cycle, generating the interrupt. Since the timebase is one second, the minimum interval before the next interrupt from this timer is variable, from one to two seconds with a setting of two.

The idle timers continue to decrement until one of two possibilities occurs: a bus cycle occurs at that I/O or memory range, or the timer decrements to zero.

When a bus cycle occurs, the idle timer is reloaded with its starting value. It then continues to decrement.

Table 4-16. APM Support Registers

Bit	Description
F0 Index AEh	**CPU Suspend Command Register (WO)** **Reset Value = 00h**
7:0	**Software CPU Suspend Command (Write Only):** If bit 0 in the Clock Stop Control Register is set low (F0 Index BCh[0] = 0) and all SMI status bits are 0, a write to this register causes a SUSP#/SUSPA# handshake with the CPU, placing the CPU in a low-power state. The data written is irrelevant. Once in this state, any unmasked IRQ or SMI releases the CPU halt condition. If F0 Index BCh[0] = 1, writing to this register invokes a full system Suspend. In this case, the SUSP_3V pin is asserted after the SUSP#/SUSPA# halt. Upon a Resume event (see Note), the PLL delay programmed in the F0 Index BCh[7:4] is invoked, allowing the clock chip and CPU PLL to stabilize before deasserting the SUSP# pin. **Note:** If the clocks are stopped, the external IRQ4 and IRQ3 pins, when enabled (F3BAR+Memory Offset 1Ah[4:3]), are the only IRQ pins that can be used as a Resume event. If GPIO2, GPIO1, and GPIO0 are enabled as an external SMI source (F0 Index 92h[2:0]), they too can be used as a Resume event. No other CS5530A pins can be used to wake-up the system from Suspend when the clocks are stopped. As long as the 32 KHz clock remains active, internal SMI events are also Resume events.
F0 Index D0h	**Software SMI Register (WO)** **Reset Value = 00h**
7:0	**Software SMI (Write Only):** A write to this location generates an SMI. The data written is irrelevant. This register allows software entry into SMM via normal bus access instructions.

When the timer decrements to zero, if power management is enabled (F0 Index 80h[0] = 1), the timer generates an SMI. (F0 Index 80h[0] = 0 does not disable these timers from running, but only from generating SMI.)

When an idle timer generates an SMI, the SMI handler manages the peripheral power, disables the timer, and enables the trap. The next time an event occurs, the trap generates an SMI. This time, the SMI handler applies power to the peripheral, enables the timer (thus reloading its starting value), and disables the trap.

Tables 4-17 through 4-25 show the device associated idle timers and traps programming bits.

Table 4-17. Power Management Global Enabling Bits

Bit	Description
F0 Index 80h	**Power Management Enable Register 1 (R/W)** **Reset Value = 00h**
2	**Traps:** Globally enable all power management device I/O traps. 0 = Disable; 1 = Enable. This excludes the audio I/O traps. They are enabled at F3BAR+Memory Offset 18h.
1	**Idle Timers:** Globally enable all power management device idle timers. 0 = Disable; 1 = Enable. Note, disable at this level does not reload the timers on the enable. The timers are disabled at their current counts. This bit has no effect on the Suspend Modulation OFF/ON Timers (F0 Index 94h/95h), nor on the General Purpose (UDEFx) Timers (F0 Index 88h-8Bh). This bit must be set for the command to trigger the SUSP#/SUSPA# feature to function (see F0 Index AEh).
0	**Power Management:** Global power management. 0 = Disable; 1 = Enabled. This bit must be set (1) immediately after POST for some power management resources to function. Until this is done, the command to trigger the SUSP#/SUSPA# feature is disabled (see F0 Index AEh) and all SMI# trigger events listed for F0 Index 84h-87h are disabled. A '0' in this bit does NOT stop the Idle Timers if bit 1 of this register is a '1', but only prevents them from generating an SMI# interrupt. It also has no effect on the UDEF traps.

Table 4-18. Keyboard/Mouse Idle Timer and Trap Related Registers

Bit	Description
F0 Index 81h	**Power Management Enable Register 2 (R/W)** **Reset Value = 00h**
3	**Keyboard/Mouse Idle Timer Enable:** Load timer from Keyboard/Mouse Idle Timer Count Register (F0 Index 9Eh) and generate an SMI when the timer expires. 0 = Disable; 1 = Enable. If an access occurs in the address ranges (listed below) the timer is reloaded with the programmed count. Keyboard Controller: I/O Ports 060h/064h COM1: I/O Port 3F8h-3FFh (if F0 Index 93h[1:0] = 10 this range is included) COM2: I/O Port 2F8h-2FFh (if F0 Index 93h[1:0] = 11 this range is included) Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[3].
F0 Index 82h	**Power Management Enable Register 3 (R/W)** **Reset Value = 00h**
3	**Keyboard/Mouse Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs in the address ranges (listed below) an SMI is generated. Keyboard Controller: I/O Ports 060h/064h COM1: I/O Port 3F8h-3FFh (if F0 Index 93h[1:0] = 10 this range is included) COM2: I/O Port 2F8h-2FFh (if F0 Index 93h[1:0] = 11 this range is included) Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 86h/F6h[3].
F0 Index 93h	**Miscellaneous Device Control Register (R/W)** **Reset Value = 00h**
1	**Mouse on Serial Enable:** Mouse is present on a serial port. 0 = No; 1 = Yes. (Note)
0	**Mouse Port Select:** Selects which serial port the mouse is attached to. 0 = COM1; 1 = COM2. (Note)
Note:	Bits 1 and 0 - If a mouse is attached to a serial port (bit 1 = 1), that port is removed from the serial device list being used to monitor serial port access for power management purposes and added to the keyboard/mouse decode. This is done because a mouse, along with the keyboard, is considered an input device and is used only to determine when to blank the screen. These bits determine the decode used for the Keyboard/Mouse Idle Timer Count Register (F0 Index 9Eh) as well as the Parallel/Serial Port Idle Timer Count Register (F0 Index 9Ch).

Table 4-18. Keyboard/Mouse Idle Timer and Trap Related Registers (Continued)

Bit	Description
F0 Index 9Eh-9Fh	**Keyboard / Mouse Idle Timer Count Register (R/W)** — **Reset Value = 0000h**
15:0	**Keyboard / Mouse Idle Timer Count:** The idle timer loaded from this register determines when the keyboard and mouse are not in use so that the LCD screen can be blanked. The 16-bit value programmed here represents the period of inactivity for these ports after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to either the keyboard or mouse I/O address spaces, including the mouse serial port address space when a mouse is enabled on a serial port. The timer uses a 1 second timebase. To enable this timer set F0 Index 81h[3] = 1. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[3].

Table 4-19. Parallel/Serial Idle Timer and Trap Related Registers

Bit	Description
F0 Index 81h	**Power Management Enable Register 2 (R/W)** — **Reset Value = 00h**
2	**Parallel/Serial Idle Timer Enable:** Load timer from Parallel/Serial Port Idle Timer Count Register (F0 Index 9Ch) and generate an SMI when the timer expires. 0 = Disable; 1 = Enable. If an access occurs in the address ranges (listed below) the timer is reloaded with the programmed count. LPT1: I/O Port 378h-37Fh, 778h-77Ah LPT2: I/O Port 278h-27Fh, 678h-67Ah COM1: I/O Port 3F8h-3FFh (if F0 Index 93h[1:0] = 10 this range is excluded) COM2: I/O Port 2F8h-2FFh (if F0 Index 93h[1:0] = 11 this range is excluded) COM3: I/O Port 3E8h-3EFh COM4: I/O Port 2E8h-2EFh Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[2].
F0 Index 82h	**Power Management Enable Register 3 (R/W)** — **Reset Value = 00h**
2	**Parallel/Serial Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs in the address ranges (listed below) an SMI is generated. LPT1: I/O Port 378h-37Fh, 778h-77Ah LPT2: I/O Port 278h-27Fh, 678h-67Ah COM1: I/O Port 3F8h-3FFh (if F0 Index 93h[1:0] = 10 this range is excluded) COM2: I/O Port 2F8h-2FFh (if F0 Index 93h[1:0] = 11 this range is excluded) COM3: I/O Port 3E8h-3EFh COM4: I/O Port 2E8h-2EFh Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 86h/F6h[2].
F0 Index 93h	**Miscellaneous Device Control Register (R/W)** — **Reset Value = 00h**
1	**Mouse on Serial Enable:** Mouse is present on a serial port. 0 = No; 1 = Yes. (Note)
0	**Mouse Port Select:** Selects which serial port the mouse is attached to. 0 = COM1; 1 = COM2. (Note)
Note: Bits 1 and 0 - If a mouse is attached to a serial port (bit 1 = 1), that port is removed from the serial device list being used to monitor serial port access for power management purposes and added to the keyboard/mouse decode. This is done because a mouse, along with the keyboard, is considered an input device and is used only to determine when to blank the screen. These bits determine the decode used for the Keyboard/Mouse Idle Timer Count Register (F0 Index 9Eh) as well as the Parallel/Serial Port Idle Timer Count Register (F0 Index 9Ch).	
F0 Index 9Ch-9Dh	**Parallel / Serial Idle Timer Count Register (R/W)** — **Reset Value = 0000h**
15:0	**Parallel / Serial Idle Timer Count:** The idle timer loaded from this register is used to determine when the parallel and serial ports are not in use so that the ports can be power managed. The 16-bit value programmed here represents the period of inactivity for these ports after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to the parallel (LPT) or serial (COM) I/O address spaces. If the mouse is enabled on a serial port, that port is not considered here. The timer uses a 1 second timebase. To enable this timer set F0 Index 81h[2] = 1. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[2].

Table 4-20. Floppy Disk Idle Timer and Trap Related Registers

Bit	Description
F0 Index 81h	**Power Management Enable Register 2 (R/W)** **Reset Value = 00h**
1	**Floppy Disk Idle Timer Enable:** Load timer from Floppy Disk Idle Timer Count Register (F0 Index 9Ah) and generate an SMI when the timer expires. 0 = Disable; 1 = Enable. If an access occurs in the address ranges (listed below) the timer is reloaded with the programmed count. Primary floppy disk: I/O Port 3F2h, 3F4h, 3F5h, and 3F7 Secondary floppy disk: I/O Port 372h, 373h, 375h, and 377h Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[1].
F0 Index 82h	**Power Management Enable Register 3 (R/W)** **Reset Value = 00h**
1	**Floppy Disk Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs in the address ranges (listed below) an SMI is generated. Primary floppy disk: I/O Port 3F2h, 3F4h, 3F5h, or 3F7 Secondary floppy disk: I/O Port 372h, 373h, 375h, or 377h Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 86h/F6h[1].
F0 Index 93h	**Miscellaneous Device Control Register (R/W)** **Reset Value = 00h**
7	**Floppy Drive Port Select:** All system resources used to power manage the floppy drive use the primary or secondary FDC addresses for decode. 0 = Primary; 1 = Primary and Secondary.
F0 Index 9Ah-9Bh	**Floppy Disk Idle Timer Count Register (R/W)** **Reset Value = 0000h**
15:0	**Floppy Disk Idle Timer Count:** The idle timer loaded from this register is used to determine when the floppy disk drive is not in use so that it can be powered down. The 16-bit value programmed here represents the period of floppy disk drive inactivity after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to any of I/O Ports 3F2h, 3F4h, 3F5h, and 3F7h (primary) or 372h, 374h, 375h, and 377h (secondary). The timer uses a 1 second timebase. To enable this timer set F0 Index 81h[1] = 1. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[1].

Table 4-21. Primary Hard Disk Idle Timer and Trap Related Registers

Bit	Description
F0 Index 81h	**Power Management Enable Register 2 (R/W)** **Reset Value = 00h**
0	**Primary Hard Disk Idle Timer Enable:** Load timer from Primary Hard Disk Idle Timer Count Register (F0 Index 98h) and generate an SMI when the timer expires. 0 = Disable; 1 = Enable. If an access occurs in the address ranges selected in F0 Index 93h[5], the timer is reloaded with the programmed count. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[0].
F0 Index 82h	**Power Management Enable Register 3 (R/W)** **Reset Value = 00h**
0	**Primary Hard Disk Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs in the address ranges selected in F0 Index 93h[5], an SMI is generated. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 86h/F6h[0].
F0 Index 93h	**Miscellaneous Device Control Register (R/W)** **Reset Value = 00h**
5	**Partial Primary Hard Disk Decode:** This bit is used to restrict the addresses which are decoded as primary hard disk accesses. 0 = Power management monitors all reads and writes I/O Port 1F0h-1F7h, 3F6h 1 = Power management monitors only writes to I/O Port 1F6h and 1F7h
F0 Index 98h-99h	**Primary Hard Disk Idle Timer Count Register (R/W)** **Reset Value = 0000h**
15:0	**Primary Hard Disk Idle Timer Count:** The idle timer loaded from this register is used to determine when the primary hard disk is not in use so that it can be powered down. The 16-bit value programmed here represents the period of primary hard disk inactivity after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to the configured primary hard disk's data port (configured in F0 Index 93h[5]). The timer uses a 1 second timebase. To enable this timer set F0 Index 81h[0] = 1. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[0].

Table 4-22. Secondary Hard Disk Idle Timer and Trap Related Registers

Bit	Description
F0 Index 83h	**Power Management Enable Register 4 (R/W)** **Reset Value = 00h**
7	**Secondary Hard Disk Idle Timer Enable:** Load timer from Secondary Hard Disk Idle Timer Count Register (F0 Index ACh) and generate an SMI when the timer expires. 0 = Disable; 1 = Enable. If an access occurs in the address ranges selected in F0 Index 93h[4], the timer is reloaded with the programmed count. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 86h/F6h[4].
6	**Secondary Hard Disk Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs in the address ranges selected in F0 Index 93h[4], an SMI is generated. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 86h/F6h[5].
F0 Index 93h	**Miscellaneous Device Control Register (R/W)** **Reset Value = 00h**
4	**Partial Secondary Hard Disk Decode:** This bit is used to restrict the addresses which are decoded as secondary hard Disk accesses. 0 = Power management monitors all reads and writes I/O Port 170h-177h, 376h 1 = Power management monitors only writes to I/O Port 176h and 177h
F0 Index ACh-ADh	**Secondary Hard Disk Idle Timer Count Register (R/W)** **Reset Value = 0000h**
15:0	**Secondary Hard Disk Idle Timer Count:** The idle timer loaded from this register is used to determine when the secondary hard disk is not in use so that it can be powered down. The 16-bit value programmed here represents the period of secondary hard disk inactivity after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to the configured secondary hard disk's data port (configured in F0 Index 93h[4]). The timer uses a 1 second timebase. To enable this timer set F0 Index 83h[7] = 1. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 86h/F6h[4].

Table 4-23. User Defined Device 1 (UDEF1) Idle Timer and Trap Related Registers

Bit	Description
F0 Index 81h	**Power Management Enable Register 4 (R/W)** **Reset Value = 00h**
4	**User Defined Device 1 (UDEF1) Idle Timer Enable:** Load timer from UDEF1 Idle Timer Count Register (F0 Index A0h) and generate an SMI when the timer expires. 0 = Disable; 1 = Enable. If an access occurs in the programmed address range the timer is reloaded with the programmed count. UDEF1 address programming is at F0 Index C0h (base address register) and CCh (control register). Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[4].
F0 Index 82h	**Power Management Enable Register 3 (R/W)** **Reset Value = 00h**
4	**User Defined Device 1 (UDEF1) Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs in the programmed address range an SMI is generated. UDEF1 address programming is at F0 Index C0h (base address register), and CCh (control register). Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[9]. Second level SMI status is reported at F1BAR+Memory Offset 04h/06h[2].
Index A0h-A1h	**User Defined Device 1 Idle Timer Count Register (R/W)** **Reset Value = 0000h**
15:0	**User Defined Device 1 (UDEF1) Idle Timer Count:** The idle timer loaded from this register determines when the device configured as UDEF1 is not in use so that it can be power managed. The 16-bit value programmed here represents the period of inactivity for this device after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to memory or I/O address space configured at F0 Index C0h (base address register) and F0 Index CCh (control register). The timer uses a 1 second timebase. To enable this timer set F0 Index 81h[4] = 1. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[4].
F0 Index C0h-C3h	**User Defined Device 1 Base Address Register (R/W)** **Reset Value = 00000000h**
31:0	**User Defined Device 1 (UDEF1) Base Address [31:0]:** This 32-bit register supports power management (trap and idle timer resources) for a PCMCIA slot or some other device in the system. The value written is used as the address comparator for the device trap/timer logic. The device can be memory or I/O mapped (configured in F0 Index CCh).
F0 Index CCh	**User Defined Device 1 Control Register (R/W)** **Reset Value = 00h**
7	**Memory or I/O Mapped:** User Defined Device 1 is: 0 = I/O; 1 = Memory.
6:0	**Mask** If bit 7 = 0 (I/O): Bit 6 0 = Disable write cycle tracking 1 = Enable write cycle tracking Bit 5 0 = Disable read cycle tracking 1 = Enable read cycle tracking Bits 4:0 Mask for address bits A[4:0] If bit 7 = 1 (M/IO): Bits 6:0 Mask for address memory bits A[15:9] (512 bytes min. and 64 KB max.) and A[8:0] are ignored. **Note:** A “1” in a mask bit means that the address bit is ignored for comparison.

Table 4-24. User Defined Device 2 (UDEF2) Idle Timer and Trap Related Registers

Bit	Description
F0 Index 81h	**Power Management Enable Register 4 (R/W)** **Reset Value = 00h**
5	**User Defined Device 2 (UDEF2) Idle Timer Enable:** Load timer from UDEF2 Idle Timer Count Register (F0 Index A2h) and generate an SMI when the timer expires. 0 = Disable; 1 = Enable. If an access occurs in the programmed address range the timer is reloaded with the programmed count. UDEF2 address programming is at F0 Index C4h (base address register) and CDh (control register). Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[5].
F0 Index 82h	**Power Management Enable Register 3 (R/W)** **Reset Value = 00h**
5	**User Defined Device 2 (UDEF2) Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs in the programmed address range an SMI is generated. UDEF2 address programming is at F0 Index C4h (base address register) and CDh (control register). Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[9]. Second level SMI status is reported at F1BAR+Memory Offset 04h/06h[3].
F0 Index A2h-A3h	**User Defined Device 2 Idle Timer Count Register (R/W)** **Reset Value = 0000h**
15:0	**User Defined Device 2 (UDEF2) Idle Timer Count:** The idle timer loaded from this register determines when the device configured as UDEF2 is not in use so that it can be power managed. The 16-bit value programmed here represents the period of inactivity for this device after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to memory or I/O address space configured at F0 Index C4h (base address register) and F0 Index CDh (control register). The timer uses a 1 second timebase. To enable this timer set F0 Index 81h[5] = 1. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[5].
F0 Index C4h-C7h	**User Defined Device 2 Base Address Register (R/W)** **Reset Value = 00000000h**
31:0	**User Defined Device 2 (UDEF2) Base Address [31:0]:** This 32-bit register supports power management (trap and idle timer resources) for a PCMCIA slot or some other device in the system. The value written is used as the address comparator for the device trap/timer logic. The device can be memory or I/O mapped (configured in F0 Index CDh).
F0 Index CDh	**User Defined Device 2 Control Register (R/W)** **Reset Value = 00h**
7	**Memory or I/O Mapped:** User Defined Device 2 is: 0 = I/O; 1 = Memory.
6:0	**Mask** If bit 7 = 0 (I/O): Bit 6 0 = Disable write cycle tracking 1 = Enable write cycle tracking Bit 5 0 = Disable read cycle tracking 1 = Enable read cycle tracking Bits 4:0 Mask for address bits A[4:0] If bit 7 = 1 (M/IO): Bits 6:0 Mask for address memory bits A[15:9] (512 bytes min. and 64 KB max.) and A[8:0] are ignored. **Note:** A “1” in a mask bit means that the address bit is ignored for comparison.

Table 4-25. User Defined Device 3 (UDEF3) Idle Timer and Trap Related Registers

Bit	Description
F0 Index 81h	**Power Management Enable Register 4 (R/W)** **Reset Value = 00h**
6	**User Defined Device 3 (UDEF3) Idle Timer Enable:** Load timer from UDEF3 Idle Timer Count Register (F0 Index A4h) and generate an SMI when the timer expires. 0 = Disable; 1 = Enable. If an access occurs in the programmed address range the timer is reloaded with the programmed count. UDEF3 address programming is at F0 Index C8h (base address register) and CEh (control register). Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[6].
F0 Index 82h	**Power Management Enable Register 3 (R/W)** **Reset Value = 00h**
6	**User Defined Device 3 (UDEF3) Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs in the programmed address range an SMI is generated. UDEF3 address programming is at F0 Index C8h (base address register) and CEh (control register). Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[9]. Second level SMI status is reported at F1BAR+Memory Offset 04h/06h[4].
F0 Index A4h-A5h	**User Defined Device 3 Idle Timer Count Register (R/W)** **Reset Value = 0000h**
15:0	**User Defined Device 3 (UDEF3) Idle Timer Count:** The idle timer loaded from this register determines when the device configured as UDEF3 is not in use so that it can be power managed. The 16-bit value programmed here represents the period of inactivity for this device after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to memory or I/O address space configured at F0 Index C8h (base address register) and F0 Index CEh (control register). The timer uses a 1 second timebase. To enable this timer set F0 Index 81h[6] = 1. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[6].
F0 Index C8h-CBh	**User Defined Device 3 Base Address Register (R/W)** **Reset Value = 00000000h**
31:0	**User Defined Device 3 (UDEF3) Base Address [31:0]:** This 32-bit register supports power management (trap and idle timer resources) for a PCMCIA slot or some other device in the system. The value written is used as the address comparator for the device trap/timer logic. The device can be memory or I/O mapped (configured in F0 Index CEh).
F0 Index CEh	**User Defined Device 3 Control Register (R/W)** **Reset Value = 00h**
7	**Memory or I/O Mapped:** User Defined Device 3 is: 0 = I/O; 1 = Memory.
6:0	**Mask** If bit 7 = 0 (I/O): Bit 6 0 = Disable write cycle tracking 1 = Enable write cycle tracking Bit 5 0 = Disable read cycle tracking 1 = Enable read cycle tracking Bits 4:0 Mask for address bits A[4:0] If bit 7 = 1 (M/IO): Bits 6:0 Mask for address memory bits A[15:9] (512 bytes min. and 64 KB max.) and A[8:0] are ignored. **Note:** A “1” in a mask bit means that the address bit is ignored for comparison.

Although not considered as device idle timers, two additional timers are provided by the CS5530A. The Video Idle Timer used for Suspend determination and the VGA Timer used for SoftVGA.

These timers and their associated programming bits are listed in Tables 4-26 and 4-27.

Table 4-26. Video Idle Timer and Trap Related Registers

Bit	Description
F0 Index 81h	**Power Management Enable Register 2 (R/W)** **Reset Value = 00h**
7	**Video Access Idle Timer Enable:** Load timer from Video Idle Timer Count Register (F0 Index A6h) and generate an SMI when the timer expires. 0 = Disable; 1 = Enable. If an access occurs in the video address range (sets bit 0 of the GX1 processor's PSERIAL register) the timer is reloaded with the programmed count. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[7].
F0 Index 82h	**Power Management Enable Register 3 (R/W)** **Reset Value = 00h**
7	**Video Access Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs in the video address range (sets bit 0 of the GX1 processor's PSERIAL register) an SMI is generated. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 86h/F6h[7].
F0 Index A6h-A7h	**Video Idle Timer Count Register (R/W)** **Reset Value = 0000h**
15:0	**Video Idle Timer Count:** The idle timer loaded from this register determines when the graphics subsystem has been idle as part of the Suspend determination algorithm. The 16-bit value programmed here represents the period of video inactivity after which the system is alerted via an SMI. The count in this timer is automatically reset whenever an access occurs to the graphics controller space. The timer uses a 1 second timebase. In a GX1 processor based system the graphics controller is embedded in the CPU, so video activity is communicated to the CS5530A via the serial connection (PSERIAL register, bit 0) from the processor. The CS5530A also detects accesses to standard VGA space on PCI (3Bxh, 3Cxh, 3Dxh and A000h-B7FFh) in the event an external VGA controller is being used. To enable this timer set F0 Index 81h[7] = 1. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[7].

Table 4-27. VGA Timer Related Registers

Bit	Description
F0 Index 83h	**Power Management Enable Register 4 (R/W)** **Reset Value = 00h**
3	**VGA Timer Enable:** Turn on VGA Timer and generate an SMI when the timer reaches 0. 0 = Disable; 1 = Enable. VGA Timer programming is at F0 Index 8Eh and F0 Index 8Bh[6]. To reload the count in the VGA timer, disable it, optionally change the count value in F0 Index 8Eh[7:0], and reenable it before enabling power management. SMI Status reporting is at F1BAR+Memory Offset 00h/02h[6] (only). Although grouped with the power management Idle Timers, the VGA Timer is not a power management function. The VGA Timer counts whether power management is enabled or disabled.
F0 Index 8Bh	**General Purpose Timer 2 Control Register (R/W)** **Reset Value = 00h**
6	**VGA Timer Base:** Selects timebase for VGA Timer Register (F0 Index 8Eh). 0 = 1 ms; 1 = 32 µs.
F0 Index 8Eh	**VGA Timer Count Register**
7:0	**VGA Timer Load Value:** This register holds the load value for the VGA timer. The value is loaded into the timer when the timer is enabled (F0 Index 83h[3] = 1). The timer is decremented with each clock of the configured timebase (F0 Index 8Bh[6]). Upon expiration of the timer, an SMI is generated and the status is reported in F1BAR+Memory Offset 00h/02h[6] (only). Once expired, this timer must be re-initialized by disabling it (F0 Index 83h[3] = 0) and then enabling it (F0 Index 83h[3] = 1). When the count value is changed in this register, the timer must be re-initialized in order for the new value to be loaded. This timer's timebase is selectable as 1 ms (default) or 32 µs. (F0 Index 8Bh). **Note:** Although grouped with the power management Idle Timers, the VGA Timer is not a power management function. It is not affected by the Global Power Management Enable setting at F0 Index 80h[0].

4.4.3.2 General Purpose Timers

The CS5530A contains two general purpose timers, General Purpose Timer 1 (F0 Index 88h) and General Purpose Timer 2 (F0 Index 8Ah). These two timers are similar to the Device Idle Timers in that they count down to zero unless re-triggered, and generate an SMI when they reach zero. However, these are 8-bit timers instead of 16 bits, they have a programmable timebase, they are not enabled or disabled by Global Power Management bits F0 Index 80h[1:0], and the events which reload these timers are configurable. These timers are typically used for an indication of system inactivity for Suspend determination.

General Purpose Timer 1 can be re-triggered by activity to any of the configured user defined devices, keyboard and mouse, parallel and serial, floppy disk, or hard disk.

General Purpose Timer 2 can be re-triggered by a transition on the GPIO7 pin (if GPIO7 is properly configured). Configuration of the GPIO7 is explained in Section 4.4.3.4 "General Purpose I/O Pins" on page 80.

The timebase for both general purpose timers can be configured as either 1 second (default) or 1 millisecond. The registers at F0 Index 89h and 8Bh are the control registers for the general purpose timers. Table 4-28 show the bit formats for these registers.

After a general purpose timer is enabled or after an event reloads the timer, the timer is loaded with the configured count value. Upon expiration of the timer an SMI is generated and a status flag is set. Once expired, this timer must be re-initialized by disabling and enabling it.

The general purpose timer is not loaded immediately, but when the free-running timebase counter reaches its maximum value. Depending on the count at the time, this could be on the next 32 KHz clock (CLK_32K), or after a full count of 32, or 32,768 clocks (approximately 1 msec, or exactly 1 sec). The general purpose timer cannot trigger an interrupt until after the first count. Thus, the minimum time before the next SMI from the timer can be either from 1-2 msec or 1-2 sec with a setting of 02h.

Table 4-28. General Purpose Timers and Control Registers

Bit	Description
F0 Index 88h	**General Purpose Timer 1 Count Register (R/W)** **Reset Value = 00h**
7:0	**General Purpose Timer 1 Count:** This register holds the load value for GP Timer 1. This value can represent either an 8-bit or 16-bit timer (selected at F0 Index 8Bh[4]). It is loaded into the timer when the timer is enabled (F0 Index 83h[0] =1). Once enabled, an enabled event (configured in F0 Index 89h[6:0]) reloads the timer. The timer is decremented with each clock of the configured timebase. Upon expiration of the timer, an SMI is generated and the top level SMI status is reported at F1BAR+Memory Offset 00h/02h[9]. The second level SMI status is reported at F1BAR+Memory Offset 04h/06h[0]). Once expired, this timer must be re-initialized by either disabling and enabling it, or writing a new count value here. This timer's timebase can be configured as 1 msec or 1 sec at F0 Index 89h[7].
F0 Index 89h	**General Purpose Timer 1 Control Register (R/W)** **Reset Value = 00h**
7	**Timebase for General Purpose Timer 1:** Selects timebase for GP Timer 1 (F0 Index 88h). 0 = 1 sec; 1 = 1 msec.
6	**Re-trigger General Purpose Timer 1 on User Defined Device 3 (UDEF3) Activity:** 0 = Disable; 1 = Enable. Any access to the configured (memory or I/O) address range for UDEF3 reloads GP Timer 1. UDEF3 address programming is at F0 Index C8h (base address register) and CEh (control register).
5	**Re-trigger General Purpose Timer 1 on User Defined Device 2 (UDEF2) Activity:** 0 = Disable; 1 = Enable. Any access to the configured (memory or I/O) address range for UDEF2 reloads GP Timer 1. UDEF2 address programming is at F0 Index C4h (base address register) and CDh (control register).
4	**Re-trigger General Purpose Timer 1 on User Defined Device 1 (UDEF1) Activity:** 0 = Disable; 1 = Enable. Any access to the configured (memory or I/O) address range for UDEF1 reloads GP Timer 1. UDEF1 address programming is at F0 Index C0h (base address register) and CCh (control register)
3	**Re-trigger General Purpose Timer 1 on Keyboard or Mouse Activity:** 0 = Disable; 1 = Enable Any access to the keyboard or mouse I/O address range (listed below) reloads GP Timer 1. Keyboard Controller: I/O Ports 060h/064h COM1: I/O Port 3F8h-3FFh (if F0 Index 93h[1:0] = 10 this range is included) COM2: I/O Port 2F8h-2FFh (if F0 Index 93h[1:0] = 11 this range is included)
2	**Re-trigger General Purpose Timer 1 on Parallel/Serial Port Activity:** 0 = Disable; 1 = Enable. Any access to the parallel or serial port I/O address range (listed below) reloads the GP Timer 1. LPT1: I/O Port 378h-37Fh, 778h-77Ah LPT2: I/O Port 278h-27Fh, 678h-67Ah COM1: I/O Port 3F8h-3FFh (if F0 Index 93h[1:0] = 10 this range is excluded) COM2: I/O Port 2F8h-2FFh (if F0 Index 93h[1:0] = 11 this range is excluded) COM3: I/O Port 3E8h-3EFh COM4: I/O Port 2E8h-2EFh

Table 4-28. General Purpose Timers and Control Registers (Continued)

Bit	Description
1	**Re-trigger General Purpose Timer 1 on Floppy Disk Activity:** 0 = Disable; 1 = Enable. Any access to the floppy disk drive address ranges (listed below) reloads GP Timer 1. Primary floppy disk: I/O Port 3F2h, 3F4h, 3F5h, and 3F7 Secondary floppy disk: I/O Port 372h, 373h, 375h, and 377h The active floppy drive is configured via F0 Index 93h[7].
0	**Re-trigger General Purpose Timer 1 on Primary Hard Disk Activity:** 0 = Disable; 1 = Enable. Any access to the primary hard disk drive address range selected in F0 Index 93h[5] reloads GP Timer 1.
F0 Index 8Ah	**General Purpose Timer 2 Count Register (R/W)** **Reset Value = 00h**
7:0	**General Purpose Timer 2 Count:** This register holds the load value for GP Timer 2. This value can represent either an 8-bit or 16-bit timer (configured in F0 Index 8Bh[5]). It is loaded into the timer when the timer is enabled (F0 Index 83h[1] = 1). Once the timer is enabled and a transition occurs on GPIO7, the timer is re-loaded. The timer is decremented with each clock of the configured timebase. Upon expiration of the timer, an SMI is generated and the top level of status is F1BAR+Memory Offset 00h/02h[9] and the second level of status is reported in F1BAR+Memory Offset 04h/06h[1]). Once expired, this timer must be re-initialized by either disabling and enabling it, or writing a new count value here. For GPIO7 to act as the reload for this timer, it must be enabled as such (F0 Index 8Bh[2]) and be configured as an input (F0 Index 90h[7]). This timer's timebase can be configured as 1 msec or 1 sec in F0 Index 8Bh[3].
F0 Index 8Bh	**General Purpose Timer 2 Control Register (R/W)** **Reset Value = 00h**
7	**Re-trigger General Purpose Timer 1 on Secondary Hard Disk Activity:** 0 = Disable; 1 = Enable. Any access to the secondary hard disk drive address range selected in F0 Index 93h[4] reloads GP Timer 1.
6	**VGA Timer Base:** Selects timebase for VGA Timer Register (F0 Index 8Eh). 0 = 1 ms; 1 = 32 µs.
5	**General Purpose Timer 2 Shift:** GP Timer 2 is treated as an 8-bit or 16-bit timer. 0 = 8-bit; 1 = 16-bit. As an 8-bit timer, the count value is loaded into GP Timer 2 Count Register (F0 Index 8Ah). As a 16-bit timer, the value loaded into GP Timer 2 Count Register is shifted left by eight bits, the lower eight bits become zero, and this 16-bit value is used as the count for GP Timer 2.
4	**General Purpose Timer 1 Shift:** GP Timer 1 is treated as an 8-bit or 16-bit timer. 0 = 8-bit; 1 = 16-bit. As an 8-bit timer, the count value is that loaded into GP Timer 1 Count Register (F0 Index 88h). As a 16-bit timer, the value loaded into GP Timer 1 Count Register is shifted left by eight bit, the lower eight bits become zero, and this 16-bit value is used as the count for GP Timer 1.
3	**Timebase for General Purpose Timer 2:** Selects timebase for GP Timer 2 (F0 Index 8Ah). 0 = 1 sec; 1 = 1 msec.
2	**Re-trigger General Purpose Timer 2 on GPIO7 Pin Transition:** A configured transition on the GPIO7 pin reloads GP Timer 2 (F0 Index 8Ah). 0 = Disable; 1 = Enable. F0 Index 92h[7] selects whether a rising- or a falling-edge transition acts as a reload. For GPIO7 to work here, it must first be configured as an input (F0 Index 90h[7] = 0).
1:0	**Reserved:** Set to 0.

4.4.3.3 ACPI Timer Register

The ACPI Timer Count Register (F1BAR+Memory Offset 1Ch or a fixed I/O Port at 121Ch) provides the current value of the ACPI timer. The timer counts at 14.31818/4 MHz (3.579545 MHz). If SMI generation is enabled (F0 Index 83h[5] = 1), an SMI is generated when bit 23 toggles. Table 4-29 shows the ACPI Timer Count Register and the ACPI Timer SMI enable bit.

V-ACPI I/O Register Space

The register space designated as V-ACPI (Virtualized ACPI) I/O does not physically exist in the CS5530A. ACPI is supported in the CS5530A by virtualizing this register space. In order for ACPI to be supported, the V-ACPI module must be included in the BIOS. The register descriptions that follow are supplied here for reference only.

Fixed Feature space registers are required to be implemented by all ACPI-compatible hardware. The Fixed Feature registers in the V-ACPI solution are mapped to normal I/O space starting at Offset AC00h. However, the designer can relocate this register space at compile time, hereafter referred to as ACPI_BASE. Registers within the V-ACPI I/O space must only be accessed on their defined boundaries. For example, BYTE aligned registers must not be accessed via WORD I/O instructions, WORD aligned registers must not be accessed as DWORD I/O instructions, etc.

Table 4-29 summarizes the registers available in the V-ACPI I/O Register Space. The “Reference” column gives the table and page number where the bit formats for the registers are located.

Table 4-29. ACPI Timer Related Registers/Bits

Bit	Description
F1BAR+Memory Offset 1Ch-1Fh (Note) **ACPI Timer Count Register (RO)** **Reset Value = 00FFFFFCh**	
	ACPI_COUNT (Read Only): This read-only register provides the current value of the ACPI timer. The timer counts at 14.31818/4 MHz (3.579545 MHz). If SMI generation is enabled via F0 Index 83h[5], an SMI is generated when the MSB toggles. The MSB toggles every 2.343 seconds. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 87h/F7h[0].
31:24	**Reserved:** Always returns 0.
23:0	**Counter**
Note: The ACPI Timer Count Register is also accessible through I/O Port 121Ch.	
F0 Index 83h **Power Management Enable Register 4 (R/W)** **Reset Value = 00h**	
5	**ACPI Timer SMI:** Allow SMI generation for MSB toggles on the ACPI Timer (F1BAR+Memory Offset 1Ch or I/O Port 121Ch). 0 = Disable; 1 = Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 87h/F7h[0].

Table 4-30. V-ACPI I/O Register Space Summary

ACPI_ BASE	Type	Align	Length	Name	Reset Value	Reference (Table 5-34)
00h-03h	R/W	4	4	P_CNT: Processor Control Register	00000000h	Page 224
04h	RO	1	1	P_LVL2: Enter C2 Power State Register	00h	Page 224
05h	--	1	1	Reserved	00h	Page 224
06h	R/W	1	1	SMI_CMD: OS/BIOS Requests Register (ACPI Enable/ Disable Port)	00h	Page 224
07h	--	1	1	Reserved	00h	Page 225
08h-09h	R/W	2	2	PM1A_STS: PM1A Status Register	0000h	Page 225
0Ah-0Bh	R/W	2	2	PM1A_EN: PM1A Enable Register	0000h	Page 225
0Ch-0Dh	R/W	4	2	PM1A_CNT: PM1A Control Register	0000h	Page 225
0Eh-0Fh	R/W	2	2	SETUP_IDX: Setup Index Register (V-ACPI internal index register)	0000h	Page 226
10h-11h	R/W	2	2	GPE0_STS: General Purpose Event 0 Status Register	0000h	Page 226
12h-13h	R/W	2	2	GPE0_EN: General Purpose Event 0 Enable Register	0000h	Page 226
14h-17h	R/W	4	4	SETUP_DATA: Setup Data Register (V-ACPI internal data register)	00000000h	Page 227
18h-1Fh	--		8	Reserved: For Future V-ACPI Implementations	--	Page 227

4.4.3.4 General Purpose I/O Pins

The CS5530A provides up to eight GPIO (general purpose I/O) pins. Five of the pins (GPIO[7:4] and GPIO1) have alternate functions. Table 4-31 shows the bits used for GPIO pin function selection.

Each GPIO pin can be configured as an input or output. GPIO[7:0] can be independently configured to act as edge-sensitive SMI events. Each pin can be enabled and configured to be either positive-edge sensitive or negative-edge sensitive. These pins then cause an SMI to be generated when an appropriate edge condition is detected. The power management status registers indicate that a GPIO external SMI event has occurred.

The GPIO Pin Direction Register 1 (F0 Index 90h) selects whether the GPIO pin is an input or output. The GPIO Pin Data Register 1 (F0 Index 91h) contains the direct values of the GPIO pins. Write operations are valid only for bits defined as outputs. Reads from this register read the last written value if the pin is an output.

GPIO Control Register 1 (F0 Index 92h) configures the operation of the GPIO pins for their various alternate functions. Bits [5:3] set the edge sensitivity for generating an SMI on the GPIO[2:0] (input) pins respectively. Bits [2:0] enable the generation of an SMI. Bit 6 enables GPIO6 to act as the lid switch input. Bit 7 determines which edge transition will cause General Purpose Timer 2 (F0 Index 8Ah) to reload.

Table 4-32 shows the bit formats for the GPIO pin configuration and control registers.

Table 4-31. GPIO Pin Function Selection

Bit	Description
F0 Index 43h	**USB Shadow Register (R/W)** — **Reset Value = 03h**
6	**Enable SA20:** Pin AD22 configuration: 0 = GPIO4; 1 = SA20. If F0 Index 43h bit 6 or bit 2 is set to 1, then pin AD22 = SA20.
2	**Enable SA[23:20]:** Pins AF23, AE23, AC21, and AD22 configuration: 0 = GPIO[7:4]; 1 = SA[23:20]. If F0 Index 43h bit 6 or bit 2 is set to 1, then pin AD22 = SA20.
F3BAR+Memory Offset 08h-0Bh	**Codec Status Register (R/W)** — **Reset Value = 00000000h**
21	**Enable SDATA_IN2:** Pin AE24 functions as: 0 = GPIO1; 1 = SDATA_IN2. For this pin to function as SDATA_IN2, it must first be configured as an input (F0 Index 90h[1] = 0).

Table 4-32. GPIO Pin Configuration/Control Registers

Bit	Description
F0 Index 90h	**GPIO Pin Direction Register 1 (R/W)** — **Reset Value = 00h**
7	**GPIO7 Direction:** Selects if GPIO7 is an input or output: 0 = Input; 1 = Output.
6	**GPIO6 Direction:** Selects if GPIO6 is an input or output: 0 = Input; 1 = Output.
5	**GPIO5 Direction:** Selects if GPIO5 is an input or output: 0 = Input; 1 = Output.
4	**GPIO4 Direction:** Selects if GPIO4 is an input or output: 0 = Input; 1 = Output.
3	**GPIO3 Direction:** Selects if GPIO3 is an input or output: 0 = Input; 1 = Output.
2	**GPIO2 Direction:** Selects if GPIO2 is an input or output: 0 = Input; 1 = Output.
1	**GPIO1 Direction:** Selects if GPIO1 is an input or output: 0 = Input; 1 = Output.
0	**GPIO0 Direction:** Selects if GPIO0 is an input or output: 0 = Input; 1 = Output.
Note: Several of these pins have specific alternate functions. The direction configured here must be consistent with the pins' use as the alternate function.	
F0 Index 91h	**GPIO Pin Data Register 1 (R/W)** — **Reset Value = 00h**
7	**GPIO7 Data:** Reflects the level of GPIO7: 0 = Low; 1 = High.
6	**GPIO6 Data:** Reflects the level of GPIO6: 0 = Low; 1 = High.
5	**GPIO5 Data:** Reflects the level of GPIO5: 0 = Low; 1 = High.
4	**GPIO4 Data:** Reflects the level of GPIO4: 0 = Low; 1 = High.
3	**GPIO3 Data:** Reflects the level of GPIO3: 0 = Low; 1 = High.
2	**GPIO2 Data:** Reflects the level of GPIO2: 0 = Low; 1 = High.
1	**GPIO1 Data:** Reflects the level of GPIO1: 0 = Low; 1 = High.
0	**GPIO0 Data:** Reflects the level of GPIO0: 0 = Low; 1 = High.
Note: This register contains the direct values of GPIO[7:0] pins. Write operations are valid only for bits defined as output. Reads from this register will read the last written value if the pin is an output. The pins are configured as inputs or outputs in F0 Index 90h.	

Table 4-32. GPIO Pin Configuration/Control Registers (Continued)

Bit	Description
F0 Index 92h	**GPIO Control Register 1 (R/W)** **Reset Value = 00h**
7	**GPIO7 Edge Sense for Reload of General Purpose Timer 2:** Selects which edge transition of GPIO7 causes GP Timer 2 to reload. 0 = Rising; 1 = Falling (Note 2).
6	**GPIO6 Enabled as Lid Switch:** Allow GPIO6 to act as the lid switch input. 0 = GPIO6; 1 = Lid switch. When enabled, every transition of the GPIO6 pin causes the lid switch status to toggle and generate an SMI. The top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 87h/F7h[3]. If GPIO6 is enabled as the lid switch, F0 Index 87h/F7h[4] reports the current status of the lid's position.
5	**GPIO2 Edge Sense for SMI:** Selects which edge transition of the GPIO2 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 2 must be set to enable this bit.
4	**GPIO1 Edge Sense for SMI:** Selects which edge transition of the GPIO1 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 1 must be set to enable this bit.
3	**GPIO0 Edge Sense for SMI:** Selects which edge transition of the GPIO0 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 1 must be set to enable this bit.
2	**Enable GPIO2 as an External SMI Source:** Allow GPIO2 to be an external SMI source and generate an SMI on either a rising or falling edge transition (depends upon setting of bit 5). 0 = Disable; 1 = Enable (Note 3). Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 87h/F7h[7].
1	**Enable GPIO1 as an External SMI Source:** Allow GPIO1 to be an external SMI source and generate an SMI on either a rising- or falling-edge transition (depends upon setting of bit 4). 0 = Disable; 1 = Enable (Note 3). Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 87h/F7h[6].
0	**Enable GPIO0 as an External SMI Source:** Allow GPIO0 to be an external SMI source and generate an SMI on either a rising or falling edge transition (depends upon setting of bit 3). 0 = Disable; 1 = Enable (Note 3) Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 87h/F7h[5].
Notes: 1) For any of the above bits to function properly, the respective GPIO pin must be configured as an input (F0 Index 90h). 2) GPIO7 can generate an SMI (F0 Index 97h[3]) or re-trigger General Purpose Timer 2 (F0 Index 8Bh[2]) or both. 3) If GPIO[2:0] are enabled as external SMI sources, they are the only GPIOs that can be used as SMI sources to wake-up the system from Suspend when the clocks are stopped.	
F0 Index 97h	**GPIO Control Register 2 (R/W)** **Reset Value = 00h**
7	**GPIO7 Edge Sense for SMI:** Selects which edge transition of the GPIO7 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 3 must be set to enable this bit.
6	**GPIO5 Edge Sense for SMI:** Selects which edge transition of the GPIO5 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 2 must be set to enable this bit.
5	**GPIO4 Edge Sense for SMI:** Selects which edge transition of the GPIO4 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 1 must be set to enable this bit.
4	**GPIO3 Edge Sense for SMI:** Selects which edge transition of the GPIO3 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 0 must be set to enable this bit.
3	**Enable GPIO7 as an External SMI Source:** Allow GPIO7 to be an external SMI source and to generate an SMI on either a rising or falling edge transition (depends upon setting of bit 7). 0 = Disable; 1 = Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 84h/F4h[3].
2	**Enable GPIO5 as an External SMI Source:** Allow GPIO5 to be an external SMI source and to generate an SMI on either a rising or falling edge transition (depends upon setting of bit 6). 0 = Disable; 1 = Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 84h/F4h[2].
1	**Enable GPIO4 as an External SMI Source:** Allow GPIO4 to be an external SMI source and to generate an SMI on either a rising- or falling-edge transition (depends upon setting of bit 5). 0 = Disable; 1 = Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 84h/F4h[1].

Table 4-32. GPIO Pin Configuration/Control Registers (Continued)

Bit	Description
0	**Enable GPIO3 as an External SMI Source:** Allow GPIO3 to be an external SMI source and to generate an SMI on either a rising or falling edge transition (depends upon setting of bit 4) 0 = Disable; 1 = Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 84h/F4h[0].
Note: For any of the above bits to function properly, the respective GPIO pin must be configured as an input (F0 Index 90h).	

4.4.3.5 Power Management SMI Status Reporting Registers

The CS5530A updates status registers to reflect the SMI sources. Power management SMI sources are the device idle timers, address traps, and general purpose I/O pins.

Power management events are reported to the processor through the SMI# pin. It is active low. When an SMI is initiated, the SMI# pin is asserted low and is held low until all SMI sources are cleared. At that time, SMI# is deasserted.

All SMI sources report to the Top Level SMI Status Register (F1BAR+Memory Offset 02h) and the Top Level SMI Status Mirror Register (F1BAR+Memory Offset 00h). The Top SMI Status and Status Mirror Registers are the top level of hierarchy for the SMI handler in determining the source of an SMI. These two registers are identical except that reading the register at F1BAR+Memory Offset 02h clears the status.

Since all SMI sources report to the Top Level SMI Status Register, many of its bits combine a large number of events requiring a second level of SMI status reporting. The second level of SMI status reporting is set up very much like the top level. There are two status reporting registers, one “read only” (mirror) and one “read to clear”. The data returned by reading either offset is the same, the difference between the two being that the SMI can not be cleared by reading the mirror register.

Figure 4-7 on page 83 shows an example SMI tree for checking and clearing the source of general purpose timer and the user defined trap generated SMIs.

Table 4-33 on page 84 shows the bit formats of the read to clear Top Level SMI Status Register (F1BAR+Memory Offset 02h). Table 4-34 starting on page 85 shows the bit formats of the read to clear second level SMI status registers. For information regarding the location of the corresponding mirror register, refer to the note in the footer of the register description.

Keep in mind, all SMI sources in the CS5530A are reported into the Top Level SMI Status Registers (F1BAR+Memory Offset 00h/02h); however, this discussion is regarding power management SMIs. For details regarding audio SMI events/reporting, refer to Section 4.7.2.2 "Audio SMI Related Registers" on page 125.

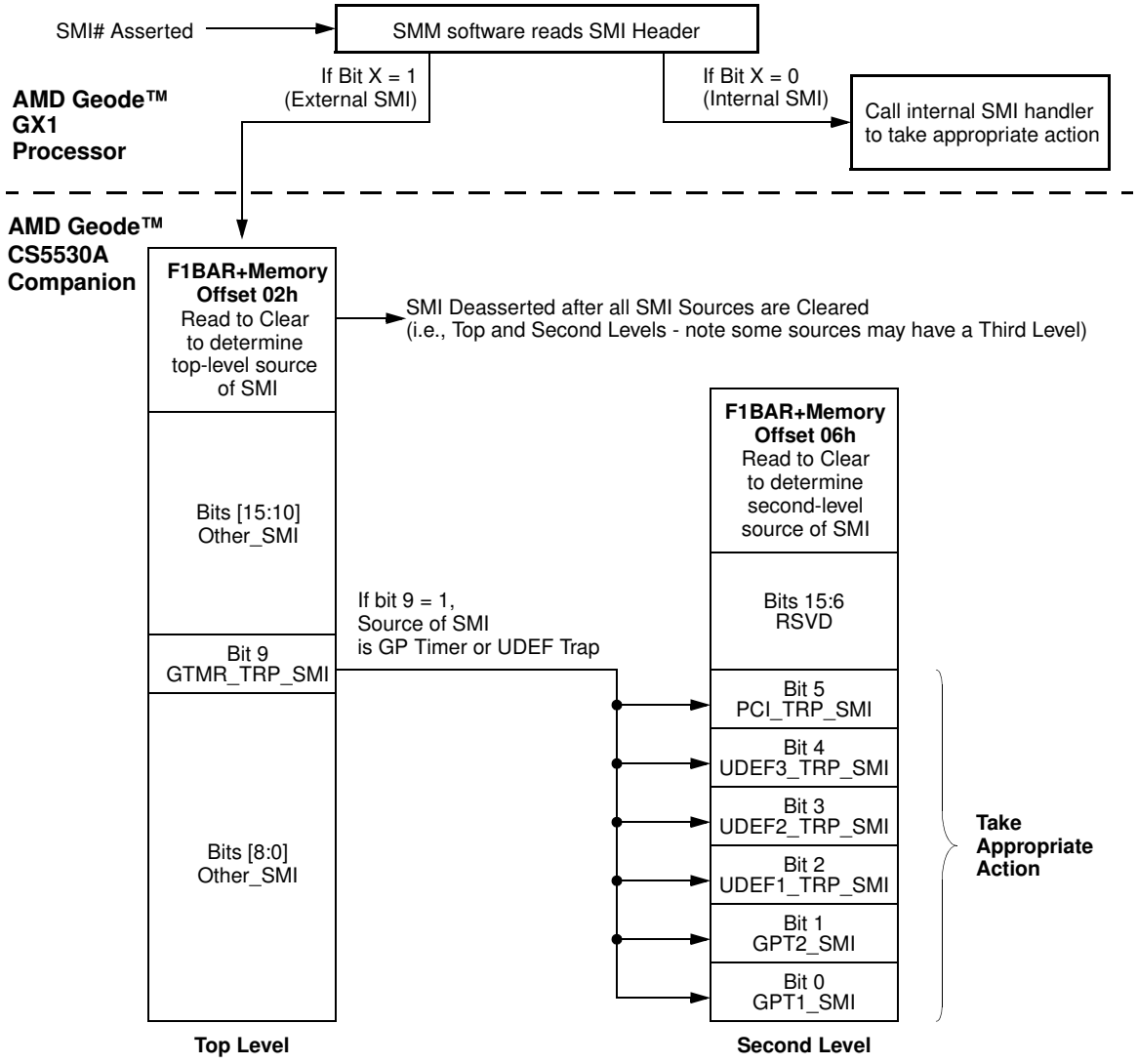


Figure 4-7. General Purpose Timer and UDEF Trap SMI Tree Example

Table 4-33. Top Level SMI Status Register (Read to Clear)

Bit	Description
F1BAR+Memory Offset 02h-03h	**Top Level SMI Status Register (RC)** **Reset Value = 0000h**
15	**Suspend Modulation Enable Mirror (Read to Clear):** This bit mirrors the Suspend Mode Configuration bit (F0 Index 96h[0]). It is used by the SMI handler to determine if the SMI Speedup Disable Register (F1BAR+Memory Offset 08h) must be cleared on exit.
14	**SMI Source is USB (Read to Clear):** SMI was caused by USB activity? 0 = No; 1 = Yes. SMI generation is configured in F0 Index 42h[7:6].
13	**SMI Source is Warm Reset Command (Read to Clear):** SMI was caused by Warm Reset command? 0 = No; 1 = Yes.
12	**SMI Source is NMI (Read to Clear):** SMI was caused by NMI activity? 0 = No; 1 = Yes.
11:10	**Reserved (Read to Clear):** Always reads 0.
9	**SMI Source is General Purpose Timers/User Defined Device Traps/Register Space Trap (Read to Clear):** SMI was caused by expiration of GP Timer 1/2; trapped access to UDEF3/2/1; trapped access to F1-F4 or ISA Legacy Register Space? 0 = No; 1 = Yes. The next level of status is found at F1BAR+Memory Offset 04h/06h.
8	**SMI Source is Software Generated (Read to Clear):** SMI was caused by software? 0 = No; 1 = Yes.
7	**SMI on an A20M# Toggle (Read to Clear):** SMI was caused by an access to either Port 092h or the keyboard command which initiates an A20M# SMI? 0 = No; 1 = Yes. This method of controlling the internal A20M# in the GX1 processor is used instead of a pin. SMI generation enabling is at F0 Index 53h[0].
6	**SMI Source is a VGA Timer Event (Read to Clear):** SMI was caused by the expiration of the VGA Timer (F0 Index 8Eh)? 0 = No; 1 = Yes. SMI generation enabling is at F0 Index 83h[3].
5	**SMI Source is Video Retrace (IRQ2) (Read to Clear):** SMI was caused by a video retrace event as decoded from the serial connection (PSERIAL register, bit 7) from the GX1 processor? 0 = No; 1 = Yes. SMI generation enabling is at F0 Index 83h[2].
4:2	**Reserved (Read to Clear):** Always reads 0.
1	**SMI Source is Audio Interface (Read to Clear):** SMI was caused by the audio interface? 0 = No; 1 = Yes. The next level SMI status registers is found in F3BAR+Memory Offset 10h/12h.
0	**SMI Source is Power Management Event (Read to Clear):** SMI was caused by one of the power management resources? 0 = No; 1 = Yes. The next level of status is found at F0 Index 84h-87h/F4h-F7h. **Note:** The status for the General Purpose Timers and the User Device Defined Traps are checked separately in bit 9.
Note: Reading this register clears all the SMI status bits. Note that bits 9, 1, and 0 have another level (second) of status reporting. A read-only “Mirror” version of this register exists at F1BAR+Memory Offset 00h. If the value of the register must be read without clearing the SMI source (and consequently deasserting SMI), the Mirror register may be read instead.	

Table 4-34. Second Level Pwr Mgmnt SMI Status Reporting Registers (Read to Clear)

Bit	Description
F1BAR+Memory Offset 06h-07h Second Level Gen. Traps/Timers SMI Status Register (RC)	**Reset Value = 0000h**
15:6	**Reserved (Read to Clear)**
5	**PCI Function Trap (Read to Clear):** SMI was caused by a trapped configuration cycle (listed below)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[9]. Trapped access to F0 PCI header registers other than Index 40h-43h; SMI generation enabling is at F0 Index 41h[0]. Trapped access to F1 PCI header registers; SMI generation enabling is at F0 Index 41h[3]. Trapped access to F2 PCI header registers; SMI generation enabling is at F0 Index 41h[6]. Trapped access to F3 PCI header registers; SMI generation enabling is at F0 Index 42h[0]. Trapped access to F4 PCI header registers; SMI generation enabling is at F0 Index 42h[1].
4	**SMI Source is Trapped Access to User Defined Device 3 (Read to Clear):** SMI was caused by a trapped I/O or memory access to the User Defined Device 3 (F0 Index C8h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[9]. SMI generation enabling is at F0 Index 82h[6].
3	**SMI Source is Trapped Access to User Defined Device 2 (Read to Clear):** SMI was caused by a trapped I/O or memory access to the User Defined Device 2 (F0 Index C4h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[9]. SMI generation enabling is at F0 Index 82h[5].
2	**SMI Source is Trapped Access to User Defined Device 1 (Read to Clear):** SMI was caused by a trapped I/O or memory access to the User Defined Device 1 (F0 Index C0h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[9]. SMI generation enabling is at F0 Index 82h[4].
1	**SMI Source is Expired General Purpose Timer 2 (Read to Clear):** SMI was caused by the expiration of General Purpose Timer 2 (F0 Index 8Ah)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[9]. SMI generation enabling is at F0 Index 83h[1].
0	**SMI Source is Expired General Purpose Timer 1 (Read to Clear):** SMI was caused by the expiration of General Purpose Timer 1 (F0 Index 88h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[9]. SMI generation enabling is at F0 Index 83h[0].
Note: Reading this register clears all the SMI status bits. A read-only "Mirror" version of this register exists at F1BAR+Memory Offset 04h. If the value of the register must be read without clearing the SMI source (and consequently deasserting SMI), the Mirror register may be read instead.	
F0 Index F4h **Second Level Power Management Status Register 1 (RC)**	**Reset Value = 84h**
7:5	**Reserved**
4	**Game Port SMI Status (Read to Clear):** SMI was caused by a R/W access to game port (I/O Port 200h and 201h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. Game Port Read SMI generation enabling is at F0 Index 83h[4]. Game Port Write SMI generation enabling is at F0 Index 53h[3].
3	**GPIO7 SMI Status (Read to Clear):** SMI was caused by transition on (properly-configured) GPIO7 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 97h[3].
2	**GPIO5 SMI Status (Read to Clear):** SMI was caused by transition on (properly-configured) GPIO5 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 97h[2].
1	**GPIO4 SMI Status (Read to Clear):** SMI was caused by transition on (properly-configured) GPIO4 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 97h[1].
0	**GPIO3 SMI Status (Read to Clear):** SMI was caused by transition on (properly-configured) GPIO3 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 97h[0].

Table 4-34. Second Level Pwr Mgmnt SMI Status Reporting Registers (Read to Clear) (Continued)

Bit	Description
Note: Properly-configured means that the GPIO pin must be enabled as a GPIO, an input, and to cause an SMI. This register provides status on various power-management SMI events. Reading this register clears the SMI status bits. A read-only (mirror) version of this register exists at F0 Index 84h.	
F0 Index F5h	**Second Level Power Management Status Register 2 (RC)** **Reset Value = 00h**
7	**Video Idle Timer SMI Status (Read to Clear):** SMI was caused by expiration of the Video Idle Timer Count Register (F0 Index A6h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[7].
6	**User Defined Device 3 (UDEF3) Idle Timer SMI Status (Read to Clear):** SMI was caused by expiration of the UDEF3 Idle Timer Count Register (F0 Index A4h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[6].
5	**User Defined Device 2 (UDEF2) Idle Timer SMI Status (Read to Clear):** SMI was caused by expiration of the UDEF2 Idle Timer Count Register (F0 Index A2h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[5].
4	**User Defined Device 1 (UDEF1) Idle Timer SMI Status (Read to Clear):** SMI was caused by expiration of the UDEF1 Idle Timer Count Register (F0 Index A0h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[4].
3	**Keyboard/Mouse Idle Timer SMI Status (Read to Clear):** SMI was caused by expiration of the Keyboard/Mouse Idle Timer Count Register (F0 Index 9Eh)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[3].
2	**Parallel/Serial Idle Timer SMI Status (Read to Clear):** SMI was caused by expiration of the Parallel/Serial Port Idle Timer Count Register (F0 Index 9Ch)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[2].
1	**Floppy Disk Idle Timer SMI Status (Read to Clear):** SMI was caused by expiration of the Floppy Disk Idle Timer Count Register (F0 Index 9Ah)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[1].
0	**Primary Hard Disk Idle Timer SMI Status (Read to Clear):** SMI was caused by expiration of the Primary Hard Disk Idle Timer Count Register (F0 Index 98h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[0].
Note: This register provides status on the Device Idle Timers to the SMI handler. A bit set here indicates that the device was idle for the duration configured in the Idle Timer Count register for that device, causing an SMI. Reading this register clears the SMI status bits. A read-only (mirror) version of this register exists at F0 Index 85h. If the value of the register must be read without clearing the SMI source (and consequently deasserting SMI), F0 Index 85h may be read instead.	
F0 Index F6h	**Second Level Power Management Status Register 3 (RC)** **Reset Value = 00h**
7	**Video Access Trap SMI Status (Read to Clear):** SMI was caused by a trapped I/O access to the Video I/O Trap? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 82h[7].
6	**Reserved (Read Only)**
5	**Secondary Hard Disk Access Trap SMI Status (Read to Clear):** SMI was caused by a trapped I/O access to the secondary hard disk? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 83h[6].

Table 4-34. Second Level Pwr Mgmnt SMI Status Reporting Registers (Read to Clear) (Continued)

Bit	Description
4	**Secondary Hard Disk Idle Timer SMI Status (Read to Clear):** SMI was caused by expiration of the Hard Disk Idle Timer Count Register (F0 Index ACh)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 83h[7].
3	**Keyboard/Mouse Access Trap SMI Status (Read to Clear):** SMI was caused by a trapped I/O access to the keyboard or mouse? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 82h[3].
2	**Parallel/Serial Access Trap SMI Status (Read to Clear):** SMI was caused by a trapped I/O access to either the serial or parallel ports? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 82h[2].
1	**Floppy Disk Access Trap SMI Status (Read to Clear):** SMI was caused by a trapped I/O access to the floppy disk? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 82h[1].
0	**Primary Hard Disk Access Trap SMI Status (Read to Clear):** SMI was caused by a trapped I/O access to the primary hard disk? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 82h[0].
Note: This register provides status on the Device Traps to the SMI handler. A bit set here indicates that an access occurred to the device while the trap was enabled, causing an SMI. Reading this register clears the SMI status bits. A read-only (mirror) version of this register exists at F0 Index 86h. If the value of the register must be read without clearing the SMI source (and consequently deasserting SMI), F0 Index 86h may be read instead.	
F0 Index F7h	**Second Level Power Management Status Register 4 (RO/RC)** **Reset Value = 00h**
7	**GPIO2 SMI Status (Read to Clear):** SMI was caused by transition on (properly-configured) GPIO2 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 92h[2].
6	**GPIO1 SMI Status (Read to Clear):** SMI was caused by transition on (properly-configured) GPIO1 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 92h[1].
5	**GPIO0 SMI Status (Read to Clear):** SMI was caused by transition on (properly-configured) GPIO0 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 92h[0].
4	**Lid Position (Read Only):** This bit maintains the current status of the lid position. If the GPIO6 pin is configured as the lid switch indicator, this bit reflects the state of the pin.
3	**Lid Switch SMI Status (Read to Clear):** SMI was caused by a transition on the GPIO6 (lid switch) pin? 0 = No; 1 = Yes. For this to happen, the GPIO6 pin must be configured both as an input (F0 Index 90h[6] = 0) and as the lid switch (F0 Index 92h[6] =1).
2	**Codec SDATA_IN SMI Status (Read to Clear):** SMI was caused by an AC97 codec producing a positive edge on SDATA_IN? 0 = No; 1 = Yes. This is the second level of status is reporting. The top level status is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 80h[5].
1	**RTC Alarm (IRQ8) SMI Status (Read to Clear):** SMI was caused by an RTC interrupt? 0 = No; 1 = Yes. This SMI event can only occur while in 3V Suspend and RTC interrupt occurs. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0].
0	**ACPI Timer SMI Status (Read to Clear):** SMI was caused by an ACPI Timer MSB toggle? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation configuration is at F0 Index 83h[5].
Note: Properly-configured means that the GPIO pin must be enabled as a GPIO, an input, and to cause an SMI. This register provides status on several miscellaneous power management events that generate SMIs, as well as the status of the Lid Switch. Reading this register clears the SMI status bits. A read-only (mirror) version of this register exists at F0 Index 87h.	

4.4.3.6 Device Power Management Register Programming Summary

Table 4-35 provides a programming register summary of the device idle timers, address traps, and general purpose I/O pins. For complete bit information regarding the registers listed in Table 4-35, refer to Section 5.3.1 "Bridge Configuration Registers - Function 0" on page 155 and Section 5.3.2 "SMI Status and ACPI Timer Registers - Function 1" on page 180.

Table 4-35. Device Power Management Programming Summary

Device Power Management Resource	Located at F0 Index xxh Unless Otherwise Noted			
	Enable	Configuration	Second Level SMI Status/No Clear	Second Level SMI Status/With Clear
Global Timer Enable	80h[1]	N/A	N/A	N/A
Keyboard / Mouse Idle Timer	81h[3]	93h[1:0]	85h[3]	F5h[3]
Parallel / Serial Idle Timer	81h[2]	93h[1:0]	85h[2]	F5h[2]
Floppy Disk Idle Timer	81h[1]	9Ah[15:0], 93h[7]	85h[1]	F5h[1]
Video Idle Timer (**Note 1**)	81h[7]	A6h[15:0]	85h[7]	F5h[7]
VGA Timer (**Note 2**)	83h[3]	8Eh[7:0]	F1BAR+Memory Offset 00h[6]	F1BAR+Memory Offset 02h[6]
Primary Hard Disk Idle Timer	81h[0]	98h[15:0], 93h[5]	85h[0]	F5h[0]
Secondary Hard Disk Idle Timer	83h[7]	ACh[15:0], 93h[4]	86h[4]	F6h[4]
User Defined Device 1 Idle Timer	81h[4]	A0h[15:0], C0h[31:0], CCh[7:0]	85h[4]	F5h[4]
User Defined Device 2 Idle Timer	81h[5]	A2h[15:0], C4h[31:0], CDh[7:0]	85h[5]	F5h[5]
User Defined Device 3 Idle Timer	81h[6]	A4h[15:0], C8h[31:0], CEh[7:0]	85h[6]	F5h[6]
Global Trap Enable	80h[2]	N/A	N/A	N/A
Keyboard / Mouse Trap	82h[3]	9Eh[15:0] 93h[1:0]	86h[3]	F6h[3]
Parallel / Serial Trap	82h[2]	9Ch[15:0], 93h[1:0]	86h[2]	F6h[2]
Floppy Disk Trap	82h[1]	93h[7]	86h[1]	F6h[1]
Video Access Trap	82h[7]	N/A	86h[7]	F6h[7]
Primary Hard Disk Trap	82h[0]	93h[5]	86h[0]	F6h[0]
Secondary Hard Disk Trap	83h[6]	93h[4]	86h[5]	F6h[5]
User Defined Device 1 Trap	82h[4]	C0h[31:0], CCh[7:0]	F1BAR+Memory Offset 04h[2]	F1BAR+Memory Offset 06h[2]
User Defined Device 2 Trap	82h[5]	C4h[31:0], CDh[7:0]	F1BAR+Memory Offset 04h[3]	F1BAR+Memory Offset 06h[3]
User Defined Device 3 Trap	82h[6]	C8h[31:0], CEh[7:0]	F1BAR+Memory Offset 04h[4]	F1BAR+Memory Offset 06h[4]
General Purpose Timer 1	83h[0]	88h[7:0], 89h[7:0], 8Bh[4]	F1BAR+Memory Offset 04h[0]	F1BAR+Memory Offset 06h[0]
General Purpose Timer 2	83h[1]	8Ah[7:0], 8Bh[5,3,2]	F1BAR+Memory Offset 04h[1]	F1BAR+Memory Offset 06h[1]
GPIO7 Pin	N/A	90h[7], 91h[7], 92h[7], 97h[7,3]	91h[7]	N/A
GPIO6 Pin	N/A	90h[6], 91h[6], 92h[6]	87h[4,3], 91h[6]	F7h[4,3]
GPIO5 Pin	N/A	90h[5], 91h[5], 97h[6,2]	91h[5]	N/A
GPIO4 Pin	N/A	90h[4], 91h[4], 97h[5,1]	91h[4]	N/A
GPIO3 Pin	N/A	90h[3], 91h[3], 97h[4,0]	91h[3]	N/A
GPIO2 Pin	N/A	90h[2], 91h[2], 92h[5,2]	87h[7], 91h[2]	F7h[7]
GPIO1 Pin	N/A	90h[1], 91h[1] 92h[4,1]	87h[6], 91h[1]	F7h[6]
GPIO0 Pin	N/A	90h[0], 91h[0], 92h[3,0]	87h[5], 91h[0]	F7h[5]
Suspend Modulation OFF/ON Video Speedup IRQ Speedup	96h[0] 80h[4] 80h[3]	94h[7:0]/95h[7:0] 8Dh[7:0] 8Ch[7:0]	N/A A8h[15:0] N/A	N/A N/A N/A

Note: 1. This function is used for Suspend determination.
2. This function is used for SoftVGA, not power management. It is not affected by Global Power Enable.

4.5 PC/AT Compatibility Logic

The CS5530A's PC/AT compatibility logic provides support for the standard PC architecture. This subsystem also provides legacy support for existing hardware and software. Support functions for the GX1 processor provided by these subsystems include:

- ISA Subtractive Decode
- ISA Bus Interface
  - — Delayed PCI Transactions
  - — Limited ISA and ISA Master Modes
- ROM Interface
- Megacells
  - — Direct Memory Access (DMA)
  - — Programmable Interval Timer
  - — Programmable Interrupt Controller
  - — PCI Compatible Interrupts
- I/O Ports 092h and 061h System Control
  - — I/O Port 092h System Control
  - — I/O Port 061h System Control
  - — SMI Generation for NMI
- Keyboard Interface Function
  - — Fast Keyboard Gate Address 20 and CPU Reset
- External Real-Time Clock Interface

The following subsections give a detailed description for each of these functions.

4.5.1 ISA Subtractive Decode

The CS5530A provides an ISA bus controller. The CS5530A is the default subtractive-decoding agent, and forwards all unclaimed memory and I/O cycles to the ISA interface. For reads and writes in the first 1 MB of memory (i.e., A23:A20 set to 0), MEMR# or MEMW# respectively will be asserted. However, the CS5530A can be configured using F0 Index 04h[1:0] to ignore either I/O, memory, or all unclaimed cycles (subtractive decode disabled, F0 Index 41h[2:1] = 1x). Table 4-36 shows these programming bits.

Table 4-36. Cycle Configuration Bits

Bit	Description
F0 Index 04h-05h	**PCI Command Register (R/W)** — **Reset Value = 000Fh**
1	**Memory Space:** Allow the CS5530A to respond to memory cycles from the PCI bus. 0 = Disable; 1 = Enable **(Default)**.
0	**I/O Space:** Allow the CS5530A to respond to I/O cycles from the PCI bus. 0 = Disable; 1 = Enable **(Default)**.
F0 Index 41h	**PCI Function Control Register 2 (R/W)** — **Reset Value = 10h**
2:1	**Subtractive Decode:** These bits determine the point at which the CS5530A accepts cycles that are not claimed by another device. The CS5530A defaults to taking subtractive decode cycles in the default cycle clock, but can be moved up to the Slow Decode cycle point if all other PCI devices decode in the fast or medium clocks. Disabling subtractive decode must be done with care, as all ISA and ROM cycles are decoded subtractively. 00 = Default sample (4th clock from FRAME# active) 01 = Slow sample (3rd clock from FRAME# active) 1x = No subtractive decode

4.5.2 ISA Bus Interface

The ISA bus controller issues multiple ISA cycles to satisfy PCI transactions that are larger than 16 bits. A full 32-bit read or write results in two 16-bit ISA transactions or four 8-bit ISA transactions. The ISA controller gathers the data from multiple ISA read cycles and returns TRDY# only after all of the data can be presented to the PCI bus at the same time.

SA[23:0] are a concatenation of ISA LA[23:17] and SA[19:0] and perform equivalent functionality at a reduced pin count.

Figure 4-8 shows the relationship between a PCI cycle and the corresponding ISA cycle generated.

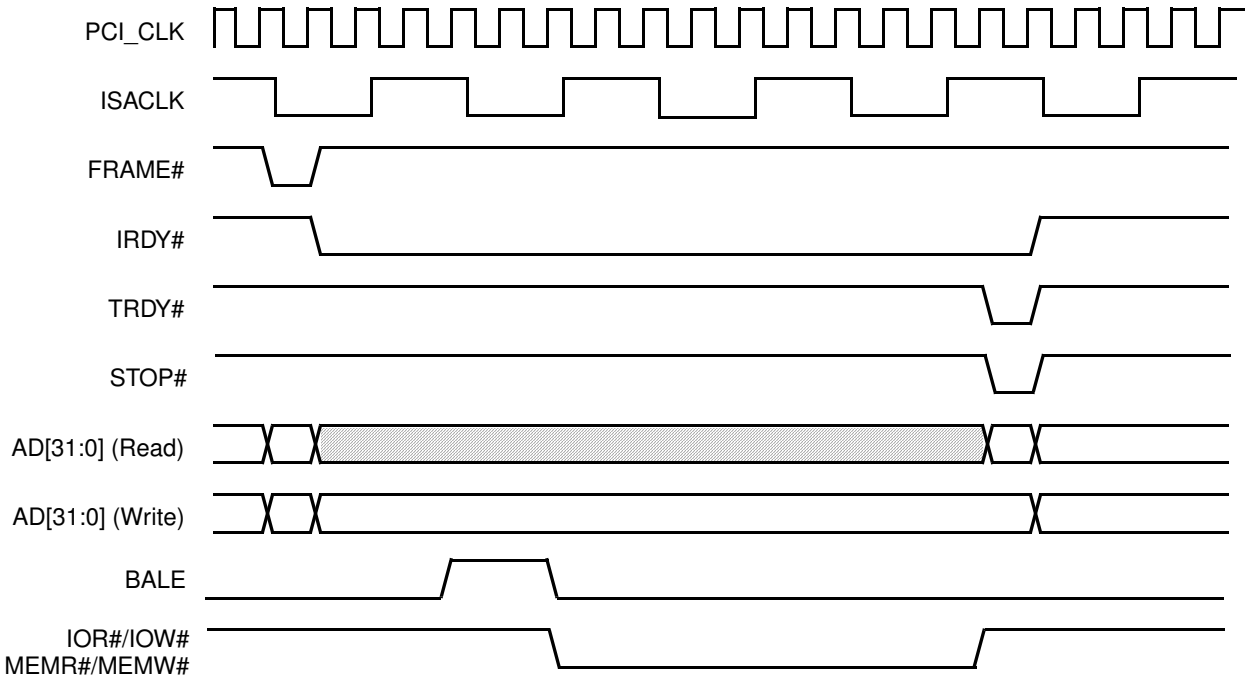
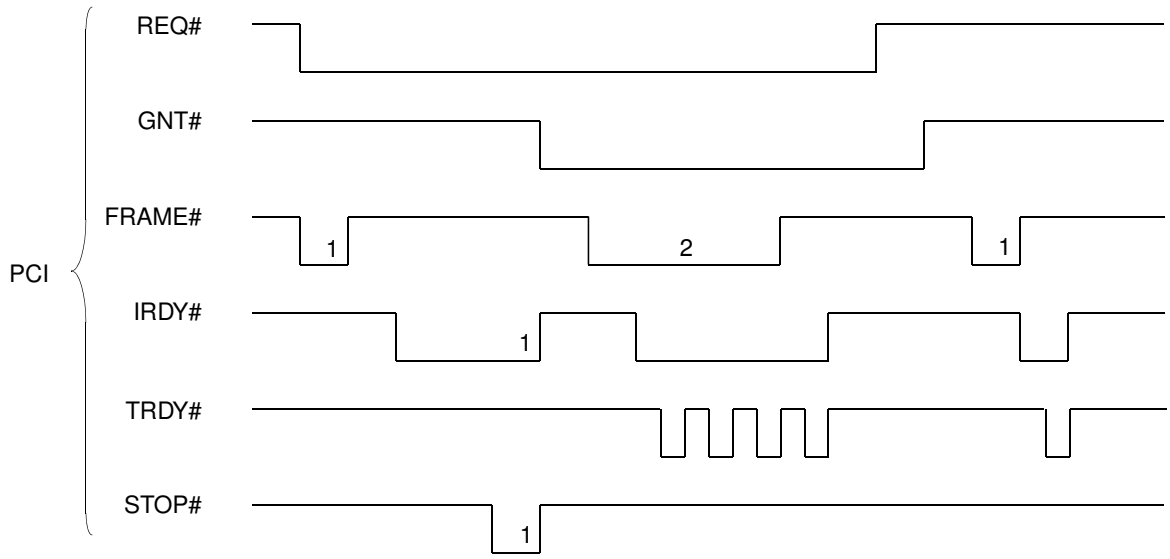


Figure 4-8. Non-Posted PCI-to-ISA Access

4.5.2.1 Delayed PCI Transactions

If PCI delayed transactions are enabled (F0 Index 42h[5] = 1) multiple PCI cycles occur for every slower ISA cycle. Figure 4-9 shows the relationship of PCI cycles to an ISA cycle with PCI delayed transactions enabled.

See Section 4.2.6 "Delayed Transactions" on page 54 for additional information.



1 - Delay
2 - IDE bus master - starts and completes
3 - End of ISA cycle

Figure 4-9. PCI to ISA Cycles with Delayed Transaction Enabled

4.5.2.2 Limited ISA and ISA Master Modes

The CS5530A supports two modes on the ISA interface. The default mode of the ISA bus is a fully functional ISA mode, but it does not support ISA masters, as shown in Figure 4-10 "Limited ISA Mode". When in this mode, the address and data buses are multiplexed together, requiring an external latch to latch the lower 16 bits of address of the ISA cycle. The signal SA_LATCH is generated when the data on the SA/SD bus is a valid address. Additionally, the upper four address bits, SA[23:20], are multiplexed on GPIO[7:4].

The second mode of the ISA interface supports ISA bus masters, as shown in Figure 4-11. When the CS5530A is placed in the ISA Master mode, a large number of pins are redefined as shown in Table 4-37.

In this mode of operation, the CS5530A cannot support TFT flat panels or TV controllers, since most of the signals used to support these functions have been redefined. This mode is required if ISA slots or ISA masters are used. ISA master cycles are only passed to the PCI bus if they access memory. I/O accesses are left to complete on the ISA bus.

The mode of operation is selected by the strapping of pin P26 (INTR):

- ISA Limited Mode — Strap pin P26 (INTR) low through a 10-kohm resistor.
- ISA Master Mode — Strap pin P26 (INTR) high through a 10-kohm resistor.

F0 Index 44h[7] (bit details on page 158) reports the strap value of the INTR pin (pin P26) during POR: 0 = ISA Limited; 1 = ISA Master.

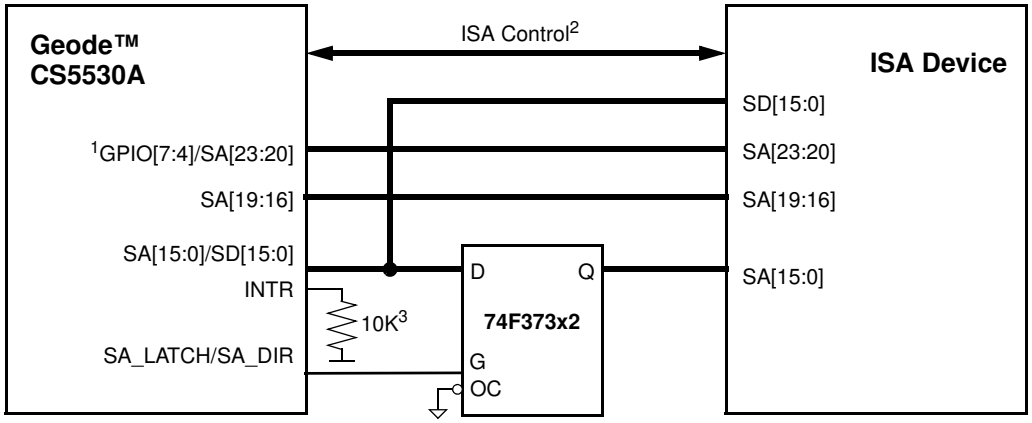
This bit can be written after POR# deassertion to change the ISA mode selected. Writing to this bit is not recommended due to the actual strapping done on the board.

ISA memory and ISA refresh cycles are not supported by the CS5530A, although, the refresh toggle bit in I/O Port 061h still exists for software compatibility reasons.

Table 4-37. Signal Assignments

Pin No.	Limited ISA Mode	ISA Master Mode
AD15	SA_LATCH	SA_DIR
AE25, AD24, AE22, AE21, AF21, AC20, AD19, AF19, AF4, AF5, AD5, AF6, AC6, AD9, AE6, AE9	SA[15:0]/SD[15:0]	SD[15:0]
H2, K1, K2, L1, D1, E2, F1, G1, G3, G4, G2, H1, J1, J3, J2, K3	FP_DATA[15:0]	SA[15:0]
H3	FP_DATA[16]	SA_OE#
F3	FP_DATA[17]	MASTER#
E1	FP_HSYNC_OUT	SMEMW#
E3	FP_VSYNC_OUT	SMEMR#
AF3 (**Note**)	SMEMW#	RTCCS#
AD4 (**Note**)	SMEMR#	RTCALE
AF23, AE23, AC21, AD22	GPIO[7:4] SA[23:20]	SA[23:20]

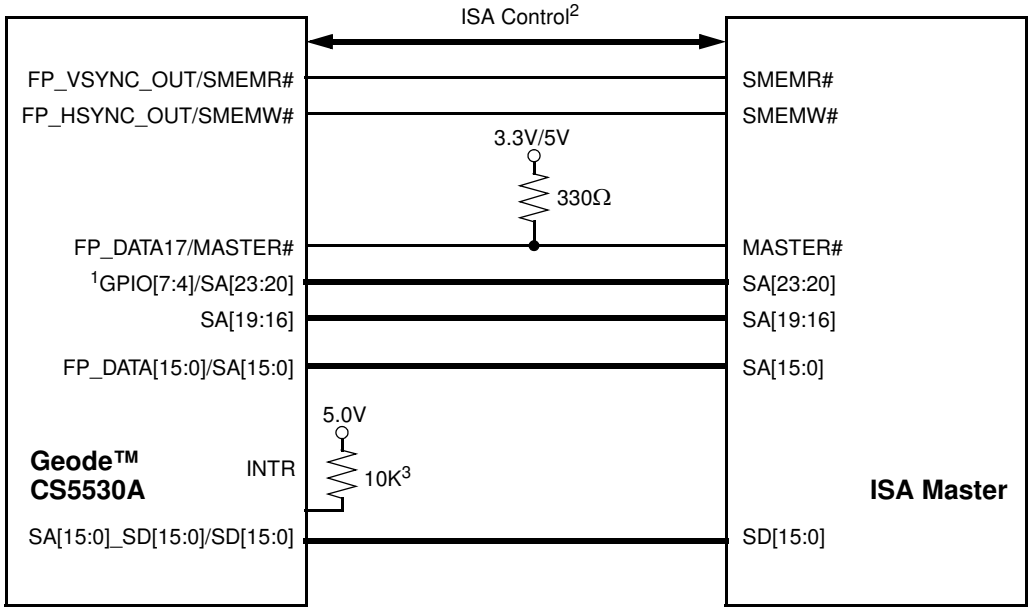
Note: If Limited ISA Mode of operation has been selected, SMEMW# and SMEMR# can be output on these pins by programming F0 Index 53[2] = 0 (bit details on page 159).



Notes:

1. F0 Index 43h[2] controls GPIO[7:4]/SA[23:20].
2. These signals are: MEMW#, MEMR#, IOR#, IOW#, TC, AEN, DREQ[7:5, 3:0], DACK[7:5, 3:0]#, MEMCS16#, ZEROWS#, SBHE#, IOCS16#, IOCHRDY, ISACLK.
3. This resistor is used at boot time to determine the mode of the ISA bus.

Figure 4-10. Limited ISA Mode



Notes:

1. When strapped for ISA Master mode, GPIO[7:4]/SA[23:20] are set to SA[23:20] and the settings in F0 Index 43h[2] are invalid.
2. These signals are: MEMW#, MEMR#, IOR#, IOW#, TC, AEN, DREQ[7:5, 3:0], DACK[7:5, 3:0]#, MEMCS16#, ZEROWS#, SBHE#, IOCS16#, IOCHRDY, ISACLK.
3. This resistor is used at boot time to determine the mode of the ISA bus.

Figure 4-11. ISA Master Mode

4.5.2.3 ISA Bus Data Steering

The CS5530A performs all of the required data steering from SD[7:0] to SD[15:0] during normal 8-bit ISA cycles, as well as during DMA and ISA master cycles. It handles data transfers between the 32-bit PCI data bus and the ISA bus. 8/16-bit devices can reside on the ISA bus. Various PC-compatible I/O registers, DMA controller registers, interrupt controller registers, and count registers (for loading timers) lie on the on-chip I/O data bus. Either the PCI bus master or the DMA controllers can become the bus owner.

When the PCI bus master is the bus owner, the CS5530A data steering logic provides data conversion necessary for 8/16/32-bit transfers to and from 8/16-bit devices on either the ISA bus or the 8-bit registers on the on-chip I/O data bus. When PCI data bus drivers of the CS5530A are tristated, data transfers between the PCI bus master and PCI bus devices are handled directly via the PCI data bus.

When the DMA requestor is the bus owner, the CS5530A allows 8/16-bit data transfer between the ISA bus and the PCI data bus.

4.5.2.4 I/O Recovery Delays

In normal operation, the CS5530A inserts a delay between back-to-back ISA I/O cycles that originate on the PCI bus. The default delay is four ISACLK cycles. Thus, the second of consecutive I/O cycles is held in the ISA bus controller until this delay count has expired. The delay is measured between the rising edge of IOR#/IOW# and the falling edge of BALE. This delay can be adjusted to a greater delay through the ISA I/O Recovery Control Register (F0 Index 51h, see Table 4-38).

Note: This delay is not inserted for a 16-bit ISA I/O access that is split into two 8-bit I/O accesses.

Table 4-38. I/O Recovery Programming Register

Bit	Description			
F0 Index 51h	**ISA I/O Recovery Control Register (R/W)**			**Reset Value = 40h**
7:4	**8-Bit I/O Recovery:** These bits determine the number of ISA bus clocks between back-to-back 8-bit I/O read cycles. This count is in addition to a preset one-clock delay built into the controller.			
	0000 = 1 ISA clock	0100 = 5 ISA clocks	1000 = 9 ISA clocks	1100 = 13 ISA clocks
	0001 = 2 ISA clocks	0101 = 6 ISA clocks	1001 = 10 ISA clocks	1101 = 14 ISA clocks
	0010 = 3 ISA clocks	0110 = 7 ISA clocks	1010 = 11 ISA clocks	1110 = 15 ISA clocks
	0011 = 4 ISA clocks	0111 = 8 ISA clocks	1011 = 12 ISA clocks	1111 = 16 ISA clocks
3:0	**16-Bit I/O Recovery:** These bits determine the number of ISA bus clocks between back-to-back 16-bit I/O cycles. This count is in addition to a preset one-clock delay built into the controller.			
	0000 = 1 ISA clock	0100 = 5 ISA clocks	1000 = 9 ISA clocks	1100 = 13 ISA clocks
	0001 = 2 ISA clocks	0101 = 6 ISA clocks	1001 = 10 ISA clocks	1101 = 14 ISA clocks
	0010 = 3 ISA clocks	0110 = 7 ISA clocks	1010 = 11 ISA clocks	1110 = 15 ISA clocks
	0011 = 4 ISA clocks	0111 = 8 ISA clocks	1011 = 12 ISA clocks	1111 = 16 ISA clocks

4.5.2.5 ISA DMA

DMA transfers occur between ISA I/O peripherals and system memory. The data width can be either 8 or 16 bits. Out of the seven DMA channels available, four are used for 8-bit transfers while the remaining three are used for 16-bit transfers. One BYTE or WORD is transferred in each DMA cycle.

Note: The CS5530A does not support DMA transfers to ISA memory.

The ISA DMA device initiates a DMA request by asserting one of the DRQ[7:5, 3:0] signals. When the CS5530A receives this request, it sends a bus grant request to the PCI arbiter. After the PCI bus has been granted, the respective DACK# is driven active.

The CS5530A generates PCI memory read or write cycles in response to a DMA cycle. Figures 4-12 and 4-13 are examples of DMA memory read and memory write cycles. Upon detection of the DMA controller's MEMR# or MEMW# active, the CS5530A starts the PCI cycle, asserts FRAME#, and negates an internal IOCHRDY. This assures the DMA cycle does not complete before the PCI cycle has provided or accepted the data. IOCHRDY is internally asserted when IRDY# and TRDY# are sampled active.

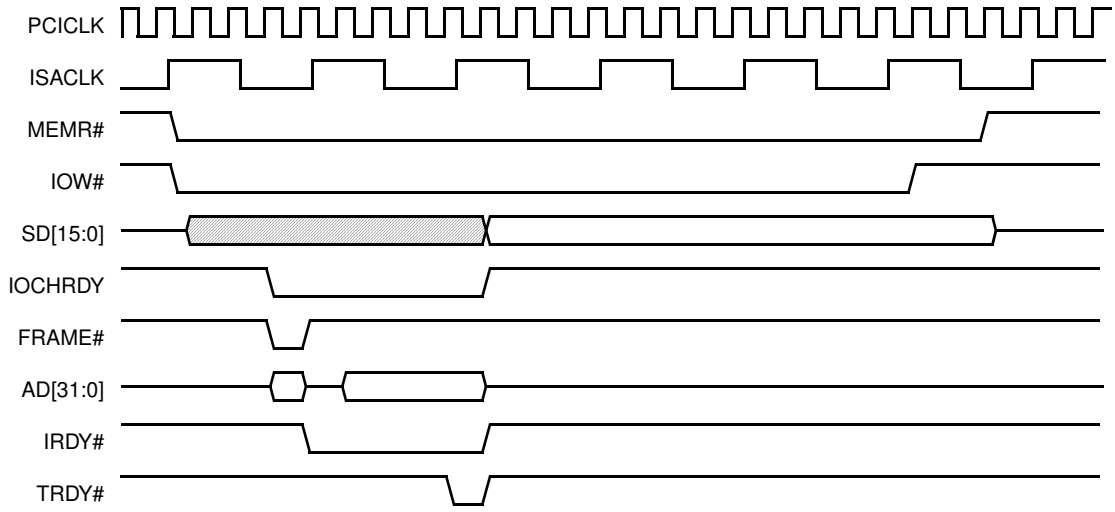


Figure 4-12. ISA DMA Read from PCI Memory

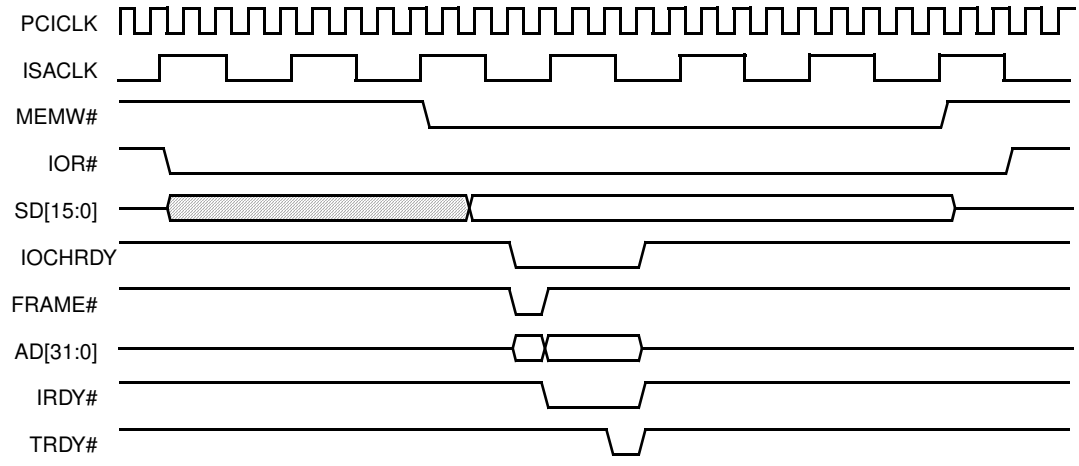


Figure 4-13. ISA DMA Write To PCI Memory

4.5.3 ROM Interface

The CS5530A positively decodes memory addresses 000F0000h-000FFFFFh (64 KB) and FFFC0000h-FFFFFFFFh (256 KB) at reset. These memory cycles cause the CS5530A to claim the cycle, and generate an ISA bus memory cycle with KBROMCS# asserted. The CS5530A can also be configured to respond to memory addresses FF000000h-FFFFFFFFh (16 MB) and 000E0000h-000FFFFFh (128 KB).

Flash ROM is supported in the CS5530A by enabling the KBROMCS# signal on write accesses to the ROM region. Normally only read cycles are passed to the ISA bus, and the KBROMCS# signal is suppressed. When the ROM Write Enable bit (F0 Index 52h[1]) is set, a write access to the ROM address region causes an 8-bit write cycle to occur with MEMW# and KBROMCS# asserted. Table 4-39 shows the ROM interface related programming bits.

4.5.4 Megacells

The CS5530A core logic integrates:

- Two 8237-equivalent DMA controllers (DMAC) with full 32-bit addressing for DMA transfers.
- Two 8259-equivalent interrupt controllers providing 13 individually programmable external interrupts.
- An 8254-equivalent timer for refresh, timer, and speaker logic.
- NMI control and generation for PCI system errors and all parity errors.
- Support for standard AT keyboard controllers, reset control, and VSA technology audio.

Table 4-39. ROM Interface Related Bits

Bit	Description
F0 Index 52h	**ROM/AT Logic Control Register (R/W)** — **Reset Value = F8h**
2	**Upper ROM Address Range:** KBROMCS# is asserted for ISA memory read accesses. 0 = FFFC0000h-FFFFFFFFh (256 KB, **Default**); 1 = FF000000h-FFFFFFFFh (16 MB) **Note:** PCI Positive decoding for the ROM space is enabled at F0 Index 5Bh[5]).
1	**ROM Write Enable:** Assert KBROMCS# during writes to configured ROM space (configured in bits 2 and 0), allowing Flash programming. 0 = Disable; 1 = Enable.
0	**Lower ROM Address Range:** KBROMCS# is asserted for ISA memory read accesses. 0 = 000F0000h-000FFFFFh (64 KB, **Default**); 1 = 000E0000h-000FFFFFh (128 KB). **Note:** PCI Positive decoding for the ROM space is enabled at F0 Index 5Bh[5]).
F0 Index 5Bh	**Decode Control Register 2 (R/W)** — **Reset Value = 20h**
5	**BIOS ROM Positive Decode:** Selects PCI positive or subtractive decoding for accesses to the configured ROM space. 0 = Subtractive; 1 = Positive. ROM configuration is at F0 Index 52h[2:0].

4.5.4.1 Direct Memory Access (DMA)

The 8237-compatible DMA controllers in the CS5530A control transfers between ISA I/O devices and system memory. They generate a bus request to the PCI bus when an I/O device requests a DMA operation. Once they are granted the bus, the DMA transfer cycle occurs. DMA transfers can occur over the entire 32-bit address range of the PCI bus. Software DMA is not supported.

The CS5530A contains registers for driving the high address bits (high page) and registers for generating the middle address bits (low page) output by the 8237 controller.

DMA Controllers

The CS5530A supports seven DMA channels using two standard 8237-equivalent controllers. DMA Controller 1 contains Channels 0 through 3 and supports 8-bit I/O adapters. These channels are used to transfer data between 8-bit peripherals and PCI memory or 8/16-bit ISA memory. Using the high and low page address registers, a full 32-bit PCI address is output for each channel so they can all transfer data throughout the entire 4 GB system address space. Each channel can transfer data in 64 KB pages.

DMA Controller 2 contains Channels 4 through 7. Channel 4 is used to cascade DMA Controller 1, so it is not available externally. Channels 5 through 7 support 16-bit I/O adapters to transfer data between 16-bit I/O adapters and 16-bit system memory. Using the high and low page address registers, a full 32-bit PCI address is output for each channel so they can all transfer data throughout the entire 4 GB system address space. Each channel can transfer data in 128 KB pages. Channels 5, 6, and 7 transfer 16-bit WORDs on even byte boundaries only.

DMA Transfer Modes

Each DMA channel can be programmed for single, block, demand or cascade transfer modes. In the most commonly used mode, single transfer mode, one DMA cycle occurs per DRQ and the PCI bus is released after every cycle. This allows the CS5530A to timeshare the PCI bus with the CPU. This is imperative, especially in cases involving large data transfers, so that the CPU does not get locked out for too long.

In block transfer mode, the DMA controller executes all of its transfers consecutively without releasing the PCI bus.

In demand transfer mode, DMA transfer cycles continue to occur as long as DRQ is high or terminal count is not reached. In this mode, the DMA controller continues to execute transfer cycles until the I/O device drops DRQ to indicate its inability to continue providing data. For this case, the PCI bus is held by the CS5530A until a break in the transfers occurs.

In cascade mode, the channel is connected to another DMA controller or to an ISA bus master, rather than to an I/O device. In the CS5530A, one of the 8237 controllers is designated as the master and the other as the slave. The HOLD output of the slave is tied to the DRQ0 input of the master (Channel 4), and the master's DACK0# output is tied to the slave's HLDA input.

In each of these modes, the DMA controller can be programmed for read, write, or verify transfers.

Both DMA controllers are reset at Power On Reset (POR) to fixed priority. Since master Channel 0 is actually connected to the slave DMA controller, the slave's four DMA channels have the highest priority, with Channel 0 as highest and Channel 3 as the lowest. Immediately following slave Channel 3, master Channel 1 (Channel 5) is the next highest, followed by Channels 6 and 7.

DMA Controller Registers

The DMA controller can be programmed with standard I/O cycles to the standard register space for DMA. The I/O addresses of all registers for the DMA controller are listed in Table 5-27 "DMA Channel Control Registers" on page 215.

Addresses under Master are for the 16-bit DMA channels, and Slave corresponds to the 8-bit channels. When writing to a channel's address or word-count register, the data is written into both the base register and the current register simultaneously. When reading a channel address or word count register, only the current address or word count can be read. The base address and base word count are not accessible for reading.

DMA Transfer Types

Each of the seven DMA channels may be programmed to perform one of three types of transfers: read, write, or verify. The transfer type selected defines the method used to transfer a BYTE or WORD during one DMA bus cycle.

For read transfer types, the CS5530A reads data from memory and writes it to the I/O device associated with the DMA channel.

For write transfer types, the CS5530A reads data from the I/O device associated with the DMA channel and writes to the memory.

The verify transfer type causes the CS5530A to execute DMA transfer bus cycles, including generation of memory addresses, but neither the Read nor Write command lines are activated. This transfer type was used by DMA Channel 0 to implement DRAM refresh in the original IBM PC/XT.

DMA Priority

The DMA controller may be programmed for two types of priority schemes: fixed and rotate (I/O Ports 008h[4] and 0D0h[4]), as shown in Table 5-27 "DMA Channel Control Registers" on page 215.

In fixed priority, the channels are fixed in priority order based on the descending values of their numbers. Thus, Channel 0 has the highest priority. In rotate priority, the last channel to get service becomes the lowest-priority channel with the priority of the others rotating accordingly. This prevents a channel from dominating the system.

The address and word count registers for each channel are 16-bit registers. The value on the data bus is written into the upper byte or lower byte, depending on the state of the internal addressing byte pointer. This pointer can be cleared by the Clear Byte Pointer command. After this command, the first read/write to an address or word count register will read/write to the low byte of the 16-bit register and the byte pointer will point to the high byte. The next read/write to an address or word-count register will read or write to the high byte of the 16-bit register and the byte pointer will point back to the low byte.

When programming the 16-bit channels (Channels 5, 6, and 7), the address which is written to the base address register must be the real address divided by two. Also, the base word count for the 16-bit channels is the number of 16-bit WORDs to be transferred, not the number of bytes as is the case for the 8-bit channels.

The DMA controller allows the user to program the active level (low or high) of the DRQ and DACK# signals. Since the two controllers are cascaded together internally on the chip, these signals should always be programmed with the DRQ signal active high and the DACK# signal active low.

DMA Shadow Registers

The CS5530A contains a shadow register located at F0 Index B8h (Table 4-40) for reading the configuration of the DMA controllers. This read-only register can sequence to read through all of the DMA registers.

DMA Addressing Capability

DMA transfers occur over the entire 32-bit address range of the PCI bus. This is accomplished by using the DMA controller's 16-bit memory address registers in conjunction with an 8-bit DMA Low Page register and an 8-bit DMA High Page register. These registers, associated with each channel, provide the 32-bit memory address capability. A write to the Low Page register clears the High Page register, for backward compatibility with the PC/AT standard. The starting address for the DMA transfer must be programmed into the DMA controller registers and the channel's respective Low and High Page registers prior to beginning the DMA transfer.

DMA Page Registers and Extended Addressing

The DMA Page registers provide the upper address bits during DMA cycles. DMA addresses do not increment or decrement across page boundaries. Page boundaries for the 8-bit channels (Channels 0 through 3) are every 64 KB and page boundaries for the 16-bit channels (Channels 5, 6, and 7) are every 128 KB.

Before any DMA operations are performed, the Page Registers must be written at the I/O Port addresses shown in Table 5-28 "DMA Page Registers" on page 218 to select the correct page for each DMA channel. The other address locations between 080h and 08Fh and 480h and 48Fh are not used by the DMA channels, but can be read or written by a PCI bus master. These registers are reset to zero at POR. A write to the Low Page register clears the High Page register, for backward compatibility with the PC/AT standard.

For most DMA transfers, the High Page register is set to zeros and is driven onto PCI address bits AD[31:24] during DMA cycles. This mode is backward compatible with the PC/AT standard. For DMA extended transfers, the High Page register is programmed and the values are driven onto the PCI addresses AD[31:24] during DMA cycles to allow access to the full 4 GB PCI address space.

DMA Address Generation

The DMA addresses are formed such that there is an upper address, a middle address, and a lower address portion.

The upper address portion, which selects a specific page, is generated by the Page registers. The Page registers for each channel must be set up by the system before a DMA operation. The DMA Page register values are driven on PCI address bits AD[31:16] for 8-bit channels and AD[31:17] for 16-bit channels.

Table 4-40. DMA Shadow Register

Bit	Description
F0 Index B8h	**DMA Shadow Register (RO)** **Reset Value = xxh**
7:0	**DMA Shadow (Read Only):** This 8-bit port sequences through the following list of shadowed DMA Controller registers. At power on, a pointer starts at the first register in the list and consecutively reads incrementally through it. A write to this register resets the read sequence to the first register. Each shadow register in the sequence contains the last data written to that location. The read sequence for this register is: 1. DMA Channel 0 Mode Register 2. DMA Channel 1 Mode Register 3. DMA Channel 2 Mode Register 4. DMA Channel 3 Mode Register 5. DMA Channel 4 Mode Register 6. DMA Channel 5 Mode Register 7. DMA Channel 6 Mode Register 8. DMA Channel 7 Mode Register 9. DMA Channel Mask Register (bit 0 is channel 0 mask, etc.) 10. DMA Busy Register (bit 0 or 1 means a DMA occurred within last 1 ms, all other bits are 0)

The middle address portion, which selects a block within the page, is generated by the DMA controller at the beginning of a DMA operation and any time the DMA address increments or decrements through a block boundary. Block sizes are 256 bytes for 8-bit channels (Channels 0 through 3) and 512 bytes for 16-bit channels (Channels 5, 6, and 7). The middle address bits are driven on PCI address bits AD[15:8] for 8-bit channels and AD[16:9] for 16-bit channels.

The lower address portion is generated directly by the DMA controller during DMA operations. The lower address bits are output on PCI address bits AD[7:0] for 8-bit channels and AD[8:1] for 16-bit channels.

SBHE# is configured as an output during all DMA operations. It is driven as the inversion of AD0 during 8-bit DMA cycles and forced low for all 16-bit DMA cycles.

4.5.4.2 Programmable Interval Timer

The CS5530A contains an 8254-equivalent Programmable Interval Timer (PIT) configured as shown in Figure 4-14. The PIT has three timers/counters, each with an input frequency of 1.19318 MHz (OSC divided by 12), and individually programmable to different modes.

The gates of Counter 0 and 1 are usually enabled, however, they can be controlled via F0 Index 50h (see Table 4-41). The gate of Counter 2 is connected to I/O Port 061h[0]. The output of Counter 0 is connected internally to IRQ0. This timer is typically configured in Mode 3 (square wave output), and used to generate IRQ0 at a periodic rate to be used as a system timer function. The output of Counter 1 is connected to I/O Port 061h[4]. The reset state of I/O Port 061h[4] is 0 and every falling edge of Counter 1 output causes I/O Port 061h[4] to flip states. The output of Counter 2 is brought out to the PC_BEEP output. This output is gated with I/O Port 061h[1].

Table 4-41. PIT Control and I/O Port 061h Associated Register Bits

Bit	Description
F0 Index 50h	**PIT Control/ISA CLK Divider (R/W)** **Reset Value = 7Bh**
7	**PIT Software Reset:** 0 = Disable; 1 = Enable.
6	**PIT Counter 1:** 0 = Forces Counter 1 output (OUT1) to zero; 1 = Allows Counter 1 output (OUT1) to pass to I/O Port 061h[4].
5	**PIT Counter 1 Enable:** 0 = Sets GATE1 input low; 1 = Sets GATE1 input high.
4	**PIT Counter 0:** 0 = Forces Counter 0 output (OUT0) to zero; 1 = Allows Counter 0 output (OUT0) to pass to IRQ0.
3	**PIT Counter 0 Enable:** 0 = Sets GATE0 input low; 1 = Sets GATE0 input high.
I/O Port 061h	**Port B Control Register (R/W)** **Reset Value = 00x01100b**
5	**PIT OUT2 State (Read Only):** This bit reflects the current status of the PIT Counter 2 (OUT2).
4	**Toggle (Read Only):** This bit toggles on every falling edge of Counter 1 (OUT1).
1	**PIT Counter2 (SPKR):** 0 = Forces Counter 2 output (OUT2) to zero; 1 = Allows Counter 2 output (OUT2) to pass to the speaker.
0	**PIT Counter2 Enable:** 0 = Sets GATE2 input low; 1 = Sets GATE2 input high.

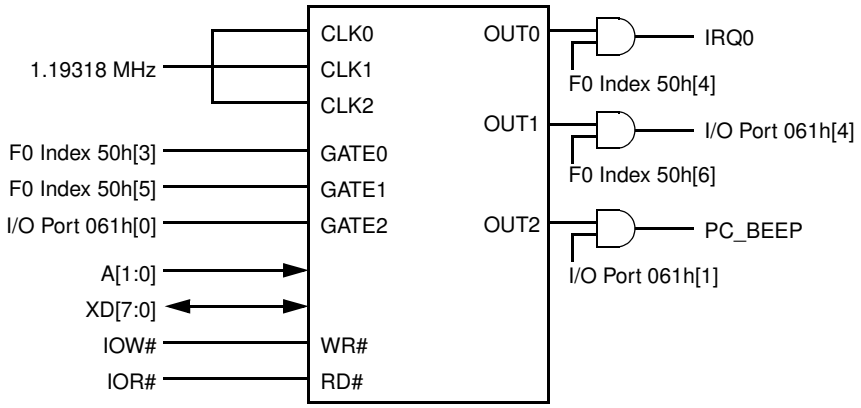


Figure 4-14. PIT Timer

PIT Registers

The PIT registers are summarized and bit formats are in Table 5-29 "Programmable Interval Timer Registers" on page 219.

PIT Shadow Register

The PIT registers are shadowed to allow for Save-to-Disk/ RAM to save/restore the PIT state by reading the PIT's counter and write-only registers. The read sequence for the shadow register is listed in F0 Index BAh, Table 4-42.

4.5.4.3 Programmable Interrupt Controller

The CS5530A includes an AT-compatible Programmable Interrupt Controller (PIC) configuration with two 8259-equivalent interrupt controllers in a master/slave configuration (Figure 4-15). These PIC devices support all x86 modes of operation except Special Fully Nested Mode.

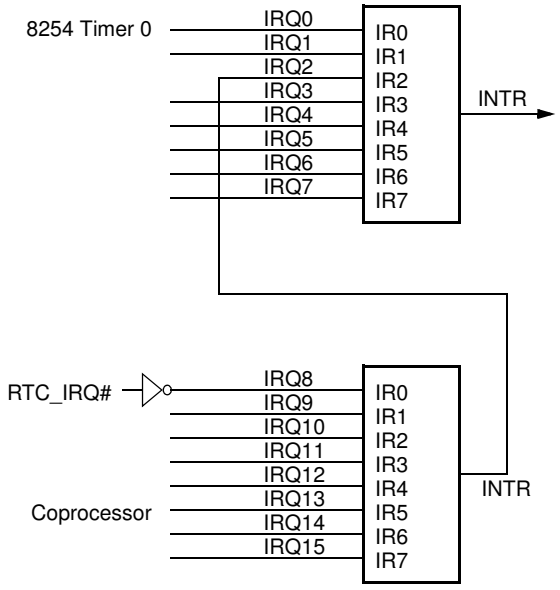


Figure 4-15. PIC Interrupt Controllers

Table 4-42. PIT Shadow Register

Bit	Description
F0 Index BAh	**PIT Shadow Register (RO)** **Reset Value = xxh**
7:0	**PIT Shadow (Read Only):** This 8-bit port sequences through the following list of shadowed Programmable Interval Timer registers. At power on, a pointer starts at the first register in the list and consecutively reads to increment through it. A write to this register resets the read sequence to the first register. Each shadow register in the sequence contains the last data written to that location. The read sequence for this register is: 1. Counter 0 LSB (least significant byte) 2. Counter 0 MSB 3. Counter 1 LSB 4. Counter 1 MSB 5. Counter 2 LSB 6. Counter 2 MSB 7. Counter 0 Command Word 8. Counter 1 Command Word 9. Counter 2 Command Word **Note:** The LSB/MSB of the count is the Counter base value, not the current value. Bits [7:6] of the command words are not used.

Of the 16 IRQs, four are mapped as shown in Table 4-43, leaving 12 external interrupts. The two controllers are cascaded through IRQ2. The internal 8254 PIT connects to IRQ0. The real-time clock interface chip (see Figure 4-18 "External RTC Interface" on page 109) and the external coprocessor interface (see Figure 4-1 "Processor Signal Connections" on page 48) connect to IRQ8# and IRQ13 respectively.

Table 4-43. PIC Interrupt Mapping

Master IRQ#	Mapping
IRQ0	Connected to the OUT0 (system timer) of the internal 8254 PIT.
IRQ2	Connected to the slave's INTR for a cascaded configuration.
IRQ8#	Connected to external real-time clock.
IRQ13	Connected to the coprocessor interface.
IRQ[15:14, 12:9, 7:3, 1]	External interrupts.

The CS5530A allows the PCI interrupt signals INTA#-INTD# (also known in industry terms as PIRQx#) to be routed internally to any IRQ signal. The routing can be modified through the CS5530A's configuration registers. If this is done, the IRQ input must be configured to be level- rather than edge-sensitive. IRQ inputs may be individually programmed to be active low, level-sensitive with the Interrupt Sensitivity configuration registers at I/O address space 4D0h and 4D1h. PCI interrupt configuration is discussed in further detail in Section 4.5.4.4 "PCI Compatible Interrupts" on page 103.

PIC Interrupt Sequence

A typical AT-compatible interrupt sequence is as follows. Any unmasked interrupt generates the INTR signal to the CPU. The interrupt controller then responds to the interrupt acknowledge (INTA) cycles from the CPU. On the first INTA cycle the cascading priority is resolved to determine which of the two 8259 controllers output the interrupt vector onto the data bus. On the second INTA cycle the appropriate 8259 controller drives the data bus with the correct interrupt vector for the highest priority interrupt.

By default, the CS5530A responds to PCI INTA cycles because the system interrupt controller is located within the CS5530A. This may be disabled with F0 Index 40h[7] (see Table 4-44). When the CS5530A responds to a PCI INTA cycle, it holds the PCI bus and internally generates the two INTA cycles to obtain the correct interrupt vector. It then asserts TRDY# and returns the interrupt vector.

PIC I/O Registers

Each PIC contains registers located in the standard I/O address locations, as shown in Table 5-30 "Programmable Interrupt Controller Registers" on page 220.

An initialization sequence must be followed to program the interrupt controllers. The sequence is started by writing Initialization Command Word 1 (ICW1). After ICW1 has been written, the controller expects the next writes to follow in the sequence ICW2, ICW3, and ICW4 if it is needed. The Operation Control Words (OCW) can be written after initialization. The PIC must be programmed before operation begins.

Since the controllers are operating in cascade mode, ICW3 of the master controller should be programmed with a value indicating that IRQ2 input of the master interrupt controller is connected to the slave interrupt controller rather than an I/O device as part of the system initialization code. In addition, ICW3 of the slave interrupt controller should be programmed with the value 02h (slave ID) and corresponds to the input on the master controller.

Table 4-44. PCI INTA Cycle Disable/Enable Bit

Bit	Description
F0 Index 40h	**PCI Function Control Register 1 (R/W)** **Reset Value = 89h**
7	**PCI Interrupt Acknowledge Cycle Response:** Allow the CS5530A responds to PCI interrupt acknowledge cycles. 0 = Disable; 1 = Enable.

PIC Shadow Register

The PIC registers are shadowed to allow for Save-to-Disk/RAM to save/restore the PIC state by reading the PIC's write-only registers. A write to this register resets the read sequence to the first register. The read sequence for the shadow register is listed in F0 Index B9h (Table 4-45).

Table 4-45. PIC Shadow Register

Bit	Description
F0 Index B9h	**PIC Shadow Register (RO)** **Reset Value = xxh**
7:0	**PIC Shadow (Read Only):** This 8-bit port sequences through the following list of shadowed Programmable Interrupt Controller registers. At power on, a pointer starts at the first register in the list and consecutively reads incrementally through it. A write to this register resets the read sequence to the first register. Each shadow register in the sequence contains the last data written to that location. The read sequence for this register is: 1. PIC1 ICW1 2. PIC1 ICW2 3. PIC1 ICW3 4. PIC1 ICW4 - Bits [7:5] of ICW4 are always 0 5. PIC1 OCW2 - Bits [6:3] of OCW2 are always 0 (Note) 6. PIC1 OCW3 - Bits [7, 4] are 0 and bit [6, 3] are 1 7. PIC2 ICW1 8. PIC2 ICW2 9. PIC2 ICW3 10. PIC2 ICW4 - Bits [7:5] of ICW4 are always 0 11. PIC2 OCW2 - Bits [6:3] of OCW2 are always 0 (Note) 12. PIC2 OCW3 - Bits [7, 4] are 0 and bit [6, 3] are 1 **Note:** To restore OCW2 to shadow register value, write the appropriate address twice. First with the shadow register value, then with the shadow register value ORed with C0h.

4.5.4.4 PCI Compatible Interrupts

The CS5530A allows the PCI interrupt signals INTA#, INTB#, INTC#, and INTD# (also known in industry terms as PIRQx#) to be mapped internally to any IRQ signal with the PCI Interrupt Steering Registers 1 and 2, F0 Index 5Ch and 5Dh (Table 4-46). This reassignment does not disable the corresponding IRQ pin. Two interrupt signals may not be assigned to the same IRQ.

PCI interrupts are low-level sensitive, whereas PC/AT interrupts are positive-edge sensitive; therefore, the PCI interrupts are inverted before being connected to the 8259.

Although the controllers default to the PC/AT-compatible mode (positive-edge sensitive), each IRQ may be individually programmed to be edge or level sensitive using the Interrupt Edge/Level Sensitivity registers in I/O Port 4D0h and 4D1h, as shown in Table 4-47. However, if the controllers are programmed to be level-sensitive via ICW1, all interrupts must be level-sensitive. Figure 4-16 shows the PCI interrupt mapping for the master/slave 8259 interrupt controller.

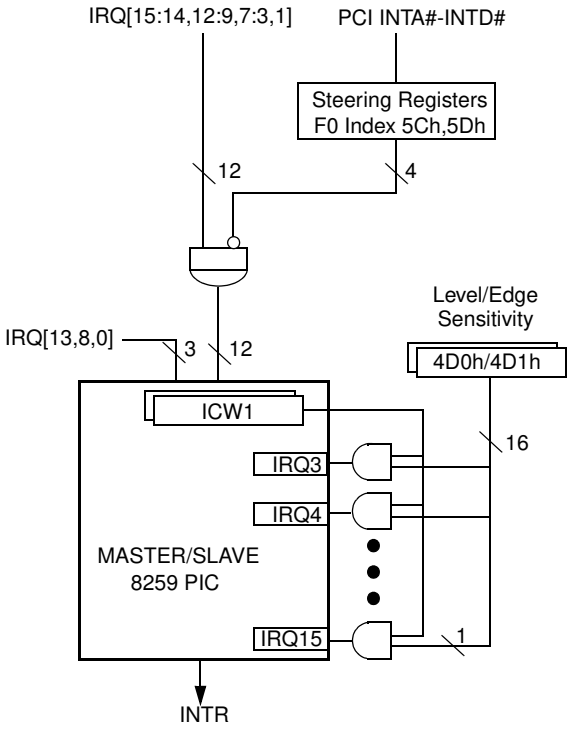


Figure 4-16. PCI and IRQ Interrupt Mapping

Table 4-46. PCI Interrupt Steering Registers

Bit	Description			
F0 Index 5Ch	**PCI Interrupt Steering Register 1 (R/W)**			**Reset Value = 00h**
7:4	**INTB# Target Interrupt:** Selects target interrupt for INTB#.			
	0000 = Disable	0100 = IRQ4	1000 = RSVD	1100 = IRQ12
	0001 = IRQ1	0101 = IRQ5	1001 = IRQ9	1101 = RSVD
	0010 = RSVD	0110 = IRQ6	1010 = IRQ10	1110 = IRQ14
	0011 = IRQ3	0111 = IRQ7	1011 = IRQ11	1111 = IRQ15
3:0	**INTA# Target Interrupt:** Selects target interrupt for INTA#.			
	0000 = Disable	0100 = IRQ4	1000 = RSVD	1100 = IRQ12
	0001 = IRQ1	0101 = IRQ5	1001 = IRQ9	1101 = RSVD
	0010 = RSVD	0110 = IRQ6	1010 = IRQ10	1110 = IRQ14
	0011 = IRQ3	0111 = IRQ7	1011 = IRQ11	1111 = IRQ15
Note: The target interrupt must first be configured as level sensitive via I/O Port 4D0h and 4D1h in order to maintain PCI interrupt compatibility.				
F0 Index 5Dh	**PCI Interrupt Steering Register 2 (R/W)**			**Reset Value = 00h**
7:4	**INTD# Target Interrupt:** Selects target interrupt for INTD#.			
	0000 = Disable	0100 = IRQ4	1000 = RSVD	1100 = IRQ12
	0001 = IRQ1	0101 = IRQ5	1001 = IRQ9	1101 = RSVD
	0010 = RSVD	0110 = IRQ6	1010 = IRQ10	1110 = IRQ14
	0011 = IRQ3	0111 = IRQ7	1011 = IRQ11	1111 = IRQ15
3:0	**INTC# Target Interrupt:** Selects target interrupt for INTC#.			
	0000 = Disable	0100 = IRQ4	1000 = RSVD	1100 = IRQ12
	0001 = IRQ1	0101 = IRQ5	1001 = IRQ9	1101 = RSVD
	0010 = RSVD	0110 = IRQ6	1010 = IRQ10	1110 = IRQ14
	0011 = IRQ3	0111 = IRQ7	1011 = IRQ11	1111 = IRQ15
Note: The target interrupt must first be configured as level sensitive via I/O Port 4D0h and 4D1h in order to maintain PCI interrupt compatibility.				

Table 4-47. Interrupt Edge/Level Select Registers

Bit	Description
I/O Port 4D0h	**Interrupt Edge/Level Select Register 1 (R/W)** **Reset Value = 00h**
7	**IRQ7 Edge or Level Select:** Selects PIC IRQ7 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
6	**IRQ6 Edge or Level Select:** Selects PIC IRQ6 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
5	**IRQ5 Edge or Level Select:** Selects PIC IRQ5 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
4	**IRQ4 Edge or Level Select:** Selects PIC IRQ4 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
3	**IRQ3 Edge or Level Select:** Selects PIC IRQ3 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
2	**Reserved:** Set to 0.
1	**IRQ1 Edge or Level Select:** Selects PIC IRQ1 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
0	**Reserved:** Set to 0.
Notes: 1. If ICW1 - bit 3 in the PIC is set as level, it overrides this setting. 2. This bit is provided to configure a PCI interrupt mapped to IRQ[x] on the PIC as level-sensitive (shared).	
I/O Port 4D1h	**Interrupt Edge/Level Select Register 2 (R/W)** **Reset Value = 00h**
7	**IRQ15 Edge or Level Select:** Selects PIC IRQ15 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
6	**IRQ14 Edge or Level Select:** Selects PIC IRQ14 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
5	**Reserved:** Set to 0.
4	**IRQ12 Edge or Level Select:** Selects PIC IRQ12 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
3	**IRQ11 Edge or Level Select:** Selects PIC IRQ11 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
2	**IRQ10 Edge or Level Select:** Selects PIC IRQ10 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
1	**IRQ9 Edge or Level Select:** Selects PIC IRQ9 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
0	**Reserved:** Set to 0.
Notes: 1. If ICW1 - bit 3 in the PIC is set as level, it overrides this setting. 2. This bit is provided to configure a PCI interrupt mapped to IRQ[x] on the PIC as level-sensitive (shared).	

4.5.5 I/O Ports 092h and 061h System Control

The CS5530A supports control functions of I/O Ports 092h (Port A) and 061h (Port B) for PS/2 compatibility. I/O Port 092h allows a fast assertion of the A20M# or CPU_RST. I/O Port 061h controls NMI generation and reports system status. Table 4-48 shows these register bit formats.

The CS5530A does not use a pin to control A20 Mask when used together with a GX1 processor. Instead, it generates an SMI for every internal change of the A20M# state and the SMI handler sets the A20M# state inside the CPU. This method is used for both the Port 092h (PS/2) and Port 061h (keyboard) methods of controlling A20M#.

Table 4-48. I/O Ports 061h and 092h

Bit	Description
I/O Port 061h	**Port B Control Register (R/W)** **Reset Value = 00x01100b**
7	**PERR#/SERR# Status (Read Only):** Was a PCI bus error (PERR#/SERR#) asserted by a PCI device or by the CS5530A? 0 = No; 1 = Yes. This bit can only be set if ERR_EN (bit 2) is set 0. This bit is set 0 after a write to ERR_EN with a 1 or after reset.
6	**IOCHK# Status (Read Only):** Is an I/O device reporting an error to the CS5530A? 0 = No; 1 = Yes. This bit can only be set if IOCHK_EN (bit 3) is set 0. This bit is set 0 after a write to IOCHK_EN with a 1 or after reset.
5	**PIT OUT2 State (Read Only):** This bit reflects the current status of the PIT Counter 2 (OUT2).
4	**Toggle (Read Only):** This bit toggles on every falling edge of Counter 1 (OUT1).
3	**IOCHK Enable:** 0 = Generates an NMI if IOCHK# is driven low by an I/O device to report an error. Note that NMI is under SMI control. 1 = Ignores the IOCHK# input signal and does not generate NMI.
2	**PERR#/SERR# Enable:** Generates an NMI if PERR#/SERR# is driven active to report an error. 0 = Enable; 1 = Disable
1	**PIT Counter2 (SPKR):** 0 = Forces Counter 2 output (OUT2) to zero; 1 = Allows Counter 2 output (OUT2) to pass to the speaker.
0	**PIT Counter2 Enable:** 0 = Sets GATE2 input low; 1 = Sets GATE2 input high.
I/O Port 092h	**Port A Control Register (R/W)** **Reset Value = 02h**
7:2	**Reserved:** Set to 0.
1	**A20M# SMI Assertion:** Assert A20M#. 0 = Enable mask; 1 = Disable mask.
0	**Fast CPU Reset:** WM_RST SMI is asserted to the BIOS. 0 = Disable; 1 = Enable. This bit must be cleared before the generation of another reset.

4.5.5.1 I/O Port 092h System Control

I/O Port 092h allows for a fast keyboard assertion of an A20# SMI and a fast keyboard CPU reset. Decoding for this register may be disabled via F0 Index 52h[3] (Table 4-49).

The assertion of a fast keyboard A20# SMI is controlled by either I/O Port 092h or by monitoring for the keyboard command sequence (see Section 4.5.6.1 "Fast Keyboard Gate Address 20 and CPU Reset" on page 108). If bit 1 of I/O Port 092h is cleared, the CS5530A internally asserts an A20M# SMI, which in turn causes an SMI to the processor. If bit 1 is set, A20M# SMI is internally deasserted again causing an SMI.

The assertion of a fast keyboard reset (WM_RST SMI) is controlled by bit 0 in I/O Port 092h or by monitoring for the keyboard command sequence. If bit 0 is changed from a 0 to a 1, the CS5530A generates a reset to the processor by generating a WM_RST SMI. When the WM_RST SMI occurs, the BIOS jumps to the Warm Reset vector. This bit remains set until the CS5530A is externally reset, or this bit is cleared by program control. Note that Warm Reset is not a pin; it is under SMI control.

4.5.5.2 I/O Port 061h System Control

Through I/O Port 061h, the speaker output can be enabled, NMI from IOCHK# or SERR# can be enabled, the status of IOCHK# and SERR# can be read, and the state of the speaker data (Timer2 output) and refresh toggle (Timer1 output) can be read back. Note that NMI is under SMI control. Even though the hardware is present, the IOCHK# pin does not exist so an NMI from IOCHK# can not happen.

4.5.5.3 SMI Generation for NMI

Figure 4-17 shows how the CS5530A can generate an SMI for an NMI. Note that NMI is not a pin.

Table 4-49. I/O Port 092h Decode Enable Bit

Bit	Description
F0 Index 52h	**ROM/AT Logic Control Register (R/W)** **Reset Value = F8h**
3	**Enable I/O Port 092h Decode (Port A):** I/O Port 092h decode and the logical functions. 0 = Disable; 1 = Enable.

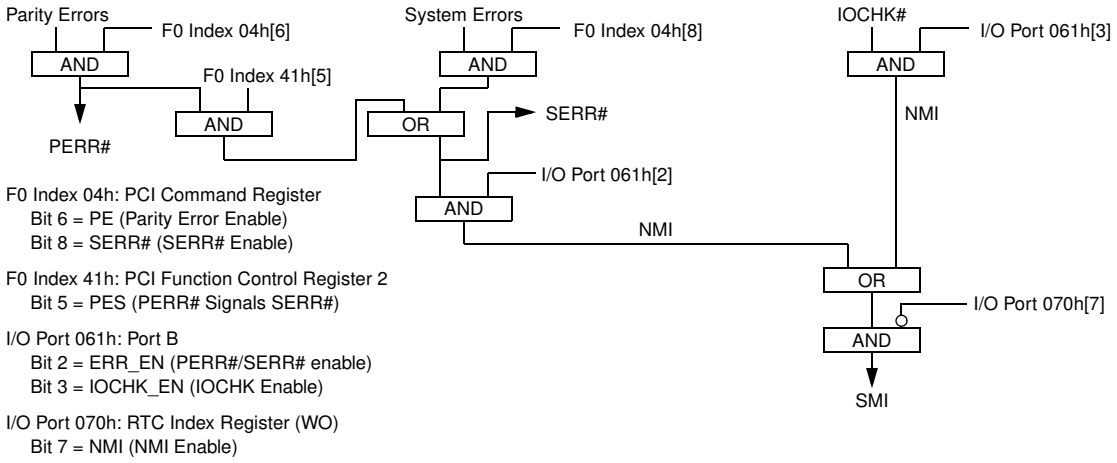


Figure 4-17. SMI Generation for NMI

4.5.6 Keyboard Interface Function

The CS5530A actively decodes the keyboard controller I/O Ports 060h and 064h, and generate an ISA I/O cycle with KBROMCS# asserted. Access to I/O Ports 062h and 066h must be enabled for KBROMCS# to be asserted. The CS5530A also actively decodes the keyboard controller I/O Ports 062h and 066h if F0 Index 5Bh[7] is set. Keyboard positive decoding can be disabled if F0 Index 5Ah[1] is cleared. Table 4-50 shows these two decoding bits.

Table 4-51 lists the standard keyboard control I/O registers and their bit formats.

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Table 4-50. Decode Control Registers

Bit	Description
F0 Index 5Ah	**Decode Control Register 1 (R/W)** **Reset Value = 03h**
1	**Keyboard Controller Positive Decode:** Selects PCI positive or subtractive decoding for accesses to I/O Port 060h and 064h (and 062h/066h if enabled). 0 = Subtractive; 1 = Positive.
Note: Positive decoding by the CS5530A speeds up the I/O cycle time. These I/O Ports do not exist in the CS5530A. It is assumed that if positive decode is enabled, the port exists on the ISA bus.	
F0 Index 5Bh	**Decode Control Register 2 (R/W)** **Reset Value = 20h**
7	**Keyboard I/O Port 062h/066h Decode:** This alternate port to the keyboard controller is provided in support of the 8051SL notebook keyboard controller mailbox**.** 0 = Disable; 1 = Enable.
Note: Positive decoding by the CS5530A speeds up the I/O cycle time. The keyboard, LPT3, LPT2, and LPT1 I/O Ports do not exist in the CS5530A. It is assumed that if positive decode is enabled, the port exists on the ISA bus.	

Table 4-51. External Keyboard Controller Registers

Bit	Description
I/O Port 060h (R/W)	**External Keyboard Controller Data Register**
Keyboard Controller Data Register: All accesses to this port are passed to the ISA bus. If the fast keyboard gate A20 and reset features are enabled through bit 7 of the ROM/AT Logic Control Register (F0 Index 52h[7]), the respective sequences of writes to this port assert the A20M# pin or cause a warm CPU reset.	
I/O Port 062h (R/W)	**External Keyboard Controller Mailbox Register**
Keyboard Controller Mailbox Register: Accesses to this port will assert KBROMCS# if the Port 062h/066h decode is enabled through bit 7 of the Decode Control Register 2 (F0 Index 5Bh[7]).	
I/O Port 064h (R/W)	**External Keyboard Controller Command Register**
Keyboard Controller Command Register: All accesses to this port are passed to the ISA bus. If the fast keyboard gate A20 and reset features are enabled through bit 7 of the ROM/AT Logic Control Register (F0 Index 52h[7]), the respective sequences of writes to this port assert the A20M# pin or cause a warm CPU reset.	
I/O Port 066h (R/W)	**External Keyboard Controller Mailbox Register**
Keyboard Controller Mailbox Register: Accesses to this port will assert KBROMCS# if the Port 062h/066h decode is enabled through bit 7 of the Decode Control Register 2 (F0 Index 5Bh[7]).	

4.5.6.1 Fast Keyboard Gate Address 20 and CPU Reset

The CS5530A monitors the keyboard I/O Ports 064h and 060h for the fast keyboard A20M# and CPU reset control sequences. If a write to I/O Port 060h[1] = 1 after a write takes place to I/O Port 064h with data of D1h, then the CS5530A asserts the A20M# signal. A20M# remains asserted until cleared by:

(1) a write to bit 1 of I/O Port 092h,

(2) a CPU reset of some kind, or

(3) write to I/O Port 060h[1] = 0 after a write takes place to I/O Port 064h with data of D1h.

The CS5530A also monitors the keyboard ports for the CPU reset control sequence. If a write to I/O Port 060h with data bit 0 set occurs after a write to I/O Port 064h with data of D1h, the CS5530A asserts a WM_RST SMI.

The fast keyboard A20M# and CPU reset can be disabled through F0 Index 52h[7]. By default, bit 7 is cleared, and the fast keyboard A20M# and CPU reset monitor logic is active. If bit 7 is clear, the CS5530A forwards the commands to the keyboard controller.

By default, the CS5530A forces the deassertion of A20M# during a warm reset. This action may be disabled if F0 Index 52h[4] is cleared.

Table 4-52. A20 Associated Programming Bits

Bit	Description
F0 Index 52h	**ROM/AT Logic Control Register (R/W)** **Reset Value = F8h**
7	**Snoop Fast Keyboard Gate A20 and Fast Reset:** Enables the snoop logic associated with keyboard commands for A20 Mask and Reset. 0 = Disable; 1 = Enable (snooping). If disabled, the keyboard controller handles the commands.
4	**Enable A20M# Deassertion on Warm Reset:** Force A20M# high during a Warm Reset (guarantees that A20M# is deasserted regardless of the state of A20). 0 = Disable; 1 = Enable.

4.5.7 External Real-Time Clock Interface

I/O Ports 070h and 071h decodes are provided to interface to an external real-time clock controller. I/O Port 070h, a write only port, is used to set up the address of the desired data in the controller. This causes the address to be placed on the ISA data bus, and the RTCALE signal to be triggered. A read of I/O Port 071h causes an ISA I/O read cycle to be performed while asserting the RTCCS# signal. A write to I/O Port 071h causes an ISA I/O write cycle to be performed with the desired data being placed on the ISA bus and the RTCCS# signal to be asserted. RTCCS#/SMEMW# and RTCALE/SMEMR# are multiplexed pins. The function selection is made through F0 Index 53h[2].

The connection between the CS5530A and an external real-time clock is shown in Figure 4-18.

The CS5530A also provides the RTC Index Shadow Register (F0 Index BBh) to store the last write to I/O Port 070h. Table 4-53 shows the bit formats for the associated registers for interfacing with an external real-time clock.

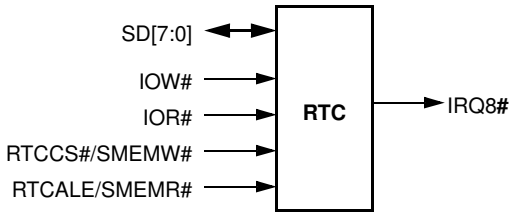


Figure 4-18. External RTC Interface

Table 4-53. Real-Time Clock Registers

Bit	Description
I/O Port 070h (WO)	**RTC Address Register**
7	**NMI Mask:** 0 = Enable; 1 = Mask.
6:0	**RTC Register Index:** A write of this register sends the data out on the ISA bus and also causes RTCALE to be triggered.
Note: This register is shadowed within the CS5530A and is read through the RTC Shadow Register (F0 Index BBh).	
I/O Port 071h (R/W)	**RTC Data Register**
A read of this register returns the value of the register indexed by the RTC Address Register plus initiates a RTCCS#. A write of this register sets the value into the register indexed by the RTC Address Register plus initiates a RTCCS#.	
F0 Index BBh	**RTC Index Shadow Register (RO)** **Reset Value = xxh**
7:0	**RTC Index Shadow (Read Only):** The RTC Shadow register contains the last written value of the RTC Index register (I/O Port 070h).
F0 Index 53h	**Alternate CPU Support Register (R/W)** **Reset Value = 00h**
2	**RTC Enable/RTC Pin Configuration:** 0 = SMEMW# (Pin AF3) and SMEMR# (Pin AD4), RTC decode disabled; 1 = RTCCS# (Pin AF3) and RTCALE (Pin AD4), RTC decode enabled. **Note:** The RTC Index Shadow Register (F0 Index BBh) is independent of the setting of this bit.

4.6 IDE Controller

The CS5530A integrates a fully-buffered, 32-bit, ANSI ATA-4-compliant (Ultra DMA33) IDE interface. The IDE interface supports two channels, primary and secondary, each supporting two devices that can operate in PIO Modes 1, 2, 3, 4, Multiword DMA, or Ultra DMA/133.

The IDE interface provides a variety of features to optimize system performance, including 32-bit disk access, post write buffers, bus master, Multiword DMA, look-ahead read buffer, and prefetch mechanism for each channel respectively.

The IDE interface timing is completely programmable. Timing control covers the command active and recover pulse widths, and command block register accesses. The IDE data-transfer speed for each device on each channel can be independently programmed allowing high-speed IDE peripherals to coexist on the same channel as older, compatible devices.

The CS5530A also provides a software-accessible buffered reset signal to the IDE drive, F0 Index 44h[3:2] (Table 4-54). The IDE_RST# signal is driven low during reset to the CS5530A and can be driven low or high as needed for device-power-off conditions.

4.6.1 IDE Interface Signals

The CS5530A has two completely separate IDE control signals, however, the IDE_RST#, IDE_ADDR[2:0] and IDE_DATA[15:0] are shared. The connections between the CS5530A and IDE devices are shown as Figure 4-19.

Table 4-54. IDE Reset Bits

Bit	Description
F0 Index 44h	**Reset Control Register (R/W)** **Reset Value = xx000000b**
3	**IDE Controller Reset:** Reset both of the CS5530A IDE controllers' internal state machines. 0 = Run; 1 = Reset. This bit is level-sensitive and must be explicitly cleared to 0 to remove the reset.
2	**IDE Reset:** Reset IDE bus. 0 = Deassert IDE bus reset signal; 1 = Assert IDE bus reset signal. This bit is level-sensitive and must be explicitly cleared to 0 to remove the reset.

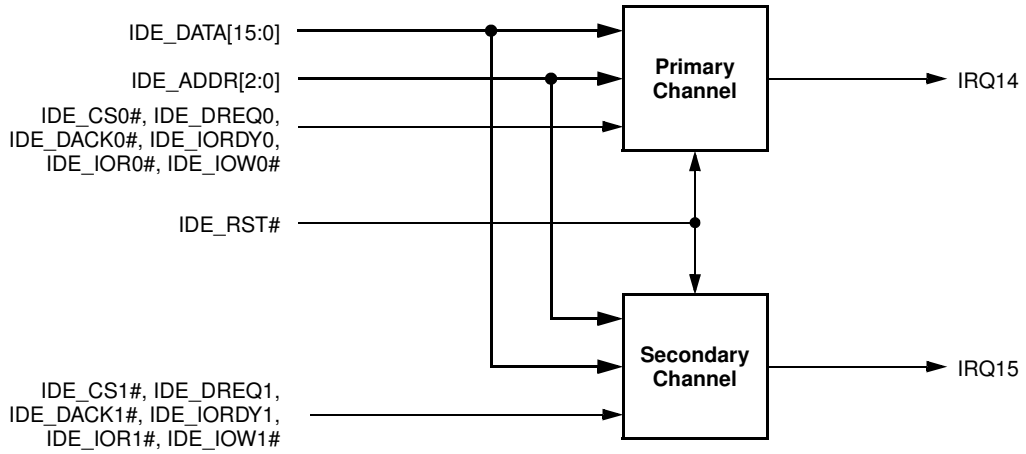


Figure 4-19. CS5530A and IDE Channel Connections

4.6.2 IDE Configuration Registers

Registers for configuring the IDE interface are accessed through F2 Index 20h, the Base Address Register (F2BAR) in Function 2. F2BAR sets the base address for the IDE Controllers Configuration Registers as shown in Table 4-55. For complete bit information, refer to Section 5.3.3 "IDE Controller Registers - Function 2" on page 184.

The following subsections discuss CS5530A operational/programming details concerning PIO, Bus Master, and Ultra DMA/33 modes.

4.6.2.1 PIO Mode

The IDE data port transaction latency consists of address latency, asserted latency and recovery latency. Address latency occurs when a PCI master cycle targeting the IDE data port is decoded, and the IDE_ADDR[2:0] and IDE_CS# lines are not set up. Address latency provides the setup time for the IDE_ADDR[2:0] and IDE_CS# lines prior to IDE_IOR# and IDE_IOW#.

Asserted latency consists of the I/O command strobe assertion length and recovery time. Recovery time is provided so that transactions may occur back-to-back on the IDE interface without violating minimum cycle periods for the IDE interface.

If IDE_IORDY is asserted when the initial sample point is reached, no wait states are added to the command strobe assertion length. If IDE_IORDY is negated when the initial sample point is reached, additional wait states are added.

Recovery latency occurs after the IDE data port transactions have completed. It provides hold time on the IDE_ADDR[2:0] and IDE_CS# lines with respect to the read and write strobes (IDE_IOR# and IDE_IOW#).

The PIO portion of the IDE registers is enabled through:

- Channel 0 Drive 0 Programmed I/O Register (F2BAR+I/O Offset 20h)
- Channel 0 Drive 1 Programmed I/O Register (F2BAR+I/O Offset 28h)
- Channel 1 Drive 0 Programmed I/O Register (F2BAR+I/O Offset 30h)
- Channel 1 Drive 1 Programmed I/O Register (F2BAR+I/O Offset 38h)

The IDE channels and devices can be individually programmed to select the proper address setup time, asserted time, and recovery time.

The bit formats for these registers are shown in Table 4-56. Note that there are different bit formats for each of the PIO programming registers depending on the operating format selected: Format 0 or Format 1.

F2BAR+I/O Offset 24h[31] (Channel 0 Drive 0 — DMA Control Register) sets the format of the PIO register. If bit 31 = 0, Format 0 is used and it selects the slowest PIO-MODE (bits [19:16]) per channel for commands. If bit 31 = 1, Format 1 is used and it allows independent control of command and data.

Also listed in the bit formats are recommended values for the different PIO modes.

Note: These are only recommended settings and are not 100% tested.

Table 4-55. Base Address Register (F2BAR) for IDE Support Registers

Bit	Description
F2 Index 20h-23h	**Base Address Register - F2BAR (R/W)** **Reset Value = 00000001h**
This register sets the base address of the I/O mapped bus mastering IDE and controller registers. Bits [6:0] are read only (0000 001), indicating a 128-byte I/O address range. Refer to Table 5-19 for the IDE configuration registers bit formats and reset values.	
31:7	**Bus Mastering IDE Base Address**
6:0	**Address Range (Read Only)**

Table 4-56. PIO Programming Registers

Bit	Description
F2BAR+I/O Offset 20h-23h	**Channel 0 Drive 0 PIO Register (R/W)** **Reset Value = 0000E132h (Note)**
If Offset 24h[31] = 0, Format 0: Selects slowest PIOMODE per channel for commands. Format 0 settings for: PIO Mode 0 = 00009172h PIO Mode 1 = 00012171h PIO Mode 2 = 00020080h PIO Mode 3 = 00032010h PIO Mode 4 = 00040010h	
31:20	**Reserved:** Set to 0.
19:16	**PIOMODE:** PIO mode
15:12	**t2I:** Recovery time (value + 1 cycle)
11:8	**t3:** IDE_IOW# data setup time (value + 1 cycle)
7:4	**t2W:** IDE_IOW# width minus t3 (value + 1 cycle)
3:0	**t1:** Address Setup Time (value + 1 cycle)
If Offset 24h[31] = 1, **Format 1:** Allows independent control of command and data. Format 1 settings for: PIO Mode 0 = 9172D132h PIO Mode 1 = 21717121h PIO Mode 2 = 00803020h PIO Mode 3 = 20102010h PIO Mode 4 = 00100010h	
31:28	**t2IC:** Command cycle recovery time (value + 1 cycle)
27:24	**t3C:** Command cycle IDE_IOW# data setup (value + 1 cycle)
23:20	**t2WC:** Command cycle IDE_IOW# pulse width minus t3 (value + 1 cycle)
19:16	**t1C:** Command cycle address setup time (value + 1 cycle)
15:12	**t2ID:** Data cycle recovery time (value + 1 cycle)
11:8	**t3D:** Data cycle IDE_IOW# data setup (value + 1 cycle)
7:4	**t2WD:** Data cycle IDE_IOW# pulse width minus t3 (value + 1 cycle)
3:0	**t1D:** Data cycle address Setup Time (value + 1 cycle)
Note: The reset value of this register is not a valid PIO Mode.	
Offset 28h-2Bh	**Channel 0 Drive 1 PIO Register (R/W)** **Reset Value = 0000E132h**
Channel 0 Drive 1 Programmed I/O Control Register: Refer to F2BAR+I/O Offset 20h for bit descriptions.	
Offset 30h-33h	**Channel 1 Drive 0 PIO Register (R/W)** **Reset Value = 0000E132h**
Channel 1 Drive 0 Programmed I/O Control Register: Refer to F2BAR+I/O Offset 20h for bit descriptions.	
Offset 38h-3Bh	**Channel 1 Drive 1 PIO Register (R/W)** **Reset Value = 0000E132h**
Channel 1 Drive 1 Programmed I/O Control Register: Refer to F2BAR+I/O Offset 20h for bit descriptions.	

4.6.2.2 Bus Master Mode

Two IDE bus masters are provided to perform the data transfers for the primary and secondary channels. The CS5530A off-loads the CPU and improves system performance in multitasking environments.

The bus master mode programming interface is an extension of the standard IDE programming model. This means that devices can always be dealt with using the standard IDE programming model, with the master mode functionality used when the appropriate driver and devices are present. Master operation is designed to work with any IDE device that supports DMA transfers on the IDE bus. Devices that work in PIO mode can only use the standard IDE programming model.

The IDE bus masters use a simple scatter/gather mechanism allowing large transfer blocks to be scattered to or gathered from memory. This cuts down on the number of interrupts to and interactions with the CPU.

Physical Region Descriptor Table Address

Before the controller starts a master transfer it is given a pointer (shown in Table 4-57) to a Physical Region Descriptor Table. This pointer sets the starting memory location of the Physical Region Descriptors (PRDs). The PRDs describe the areas of memory that are used in the data transfer. The PRDs must be aligned on a 4-byte boundary and the table cannot cross a 64 KB boundary in memory.

Primary and Secondary IDE Bus Master Registers

The IDE Bus Master Registers for each channel (primary and secondary) have an IDE Bus Master Command Register and Bus Master Status Register. These registers must be accessed individually; a 32-bit DWORD access attempting to include both the Command and Status registers may not operate correctly. Bit formats of these registers are given in Table 4-58.

Table 4-57. IDE Bus Master PRD Table Address Registers

Bit	Description
F2BAR+I/O Offset 04h-07h	**IDE Bus Master 0 PRD Table Address — Primary (R/W)** **Reset Value = 00000000h**
31:2	**Pointer to the Physical Region Descriptor Table:** This register is a PRD table pointer for IDE Bus Master 0. When written, this register points to the first entry in a PRD table. Once IDE Bus Master 0 is enabled (Command Register bit 0 = 1], it loads the pointer and updates this register to the next PRD by adding 08h. When read, this register points to the next PRD.
1:0	**Reserved:** Set to 0.
F2BAR+I/O Offset 0Ch-0Fh	**IDE Bus Master 1 PRD Table Address — Secondary (R/W)** **Reset Value = 00000000h**
31:2	**Pointer to the Physical Region Descriptor Table:** This register is a PRD table pointer for IDE Bus Master 1. When written, this register points to the first entry in a PRD table. Once IDE Bus Master 1 is enabled (Command Register bit 0 = 1], it loads the pointer and updates this register to the next PRD by adding 08h. When read, this register points to the next PRD.
1:0	**Reserved:** Set to 0.

Table 4-58. IDE Bus Master Command and Status Registers

Bit	Description
F2BAR+I/O Offset 00h	**IDE Bus Master 0 Command Register — Primary (R/W)**	**Reset Value = 00h**
7:4	**Reserved:** Set to 0. Must return 0 on reads.
3	**Read or Write Control:** Sets the direction of bus master transfers. 0 = PCI reads performed; 1 = PCI writes performed. This bit should not be changed when the bus master is active.
2:1	**Reserved:** Set to 0. Must return 0 on reads.
0	**Bus Master Control:** Controls the state of the bus master. 0 = Disable master; 1 = Enable master. Bus master operations can be halted by setting bit 0 to 0. Once an operation has been halted, it can not be resumed. If bit 0 is set to 0 while a bus master operation is active, the command is aborted and the data transferred from the drive is discarded. This bit should be reset after completion of data transfer.
F2BAR+I/O Offset 02h	**IDE Bus Master 0 Status Register — Primary (R/W)**	**Reset Value = 00h**
7	**Simplex Mode (Read Only):** Can both the primary and secondary channel operate independently? 0 = Yes; 1 = No (simplex mode).
6	**Drive 1 DMA Capable:** Allow Drive 1 to be capable of DMA transfers. 0 = Disable; 1 = Enable.
5	**Drive 0 DMA Capable:** Allow Drive 0 to be capable of DMA transfers. 0 = Disable; 1 = Enable.
4:3	**Reserved:** Set to 0. Must return 0 on reads.
2	**Bus Master Interrupt:** Has the bus master detected an interrupt? 0 = No; 1 = Yes. Write 1 to clear.
1	**Bus Master Error:** Has the bus master detected an error during data transfer? 0 = No; 1 = Yes. Write 1 to clear.
0	**Bus Master Active (Read Only):** Is the bus master active? 0 = No; 1 = Yes.
F2BAR+I/O Offset 04h-07h	**IDE Bus Master 0 PRD Table Address — Primary (R/W)**	**Reset Value = 00000000h**
31:2	**Pointer to the Physical Region Descriptor Table:** This register is a PRD table pointer for IDE Bus Master 0. When written, this register points to the first entry in a PRD table. Once IDE Bus Master 0 is enabled (Command Register bit 0 = 1], it loads the pointer and updates this register to the next PRD by adding 08h. When read, this register points to the next PRD.
1:0	**Reserved:** Set to 0.
F2BAR+I/O Offset 08h	**IDE Bus Master 1 Command Register — Secondary (R/W)**	**Reset Value = 00h**
7:4	**Reserved:** Set to 0. Must return 0 on reads.
3	**Read or Write Control:** Sets the direction of bus master transfers. 0 = PCI reads performed; 1 = PCI writes performed. This bit should not be changed when the bus master is active.
2:1	**Reserved:** Set to 0. Must return 0 on reads.
0	**Bus Master Control:** Controls the state of the bus master. 0 = Disable master; 1 = Enable master. Bus master operations can be halted by setting bit 0 = 0. Once an operation has been halted, it can not be resumed. If bit 0 is set to 0 while a bus master operation is active, the command is aborted and the data transferred from the drive is discarded. This bit should be reset after completion of data transfer.
F2BAR+I/O Offset 0Ah	**IDE Bus Master 1 Status Register — Secondary (R/W)**	**Reset Value = 00h**
7	**Simplex Mode (Read Only):** Can both the primary and secondary channel operate independently? 0 = Yes; 1 = No (simplex mode).
6	**Drive 1 DMA Capable:** Allow Drive 1 to be capable of DMA transfers. 0 = Disable; 1 = Enable.
5	**Drive 0 DMA Capable:** Allow Drive 0 to be capable of DMA transfers. 0 = Disable; 1 = Enable.
4:3	**Reserved:** Set to 0. Must return 0 on reads.
2	**Bus Master Interrupt:** Has the bus master detected an interrupt? 0 = No; 1 = Yes. Write 1 to clear.
1	**Bus Master Error:** Has the bus master detected an error during data transfer? 0 = No; 1 = Yes. Write 1 to clear.
0	**Bus Master Active (Read Only):** Is the bus master active? 0 = No; 1 = Yes.

Physical Region Descriptor Format

Each physical memory region to be transferred is described by a Physical Region Descriptor (PRD) as illustrated in Table 4-59. When the bus master is enabled (Command Register bit 0 = 1), data transfer proceeds until each PRD in the PRD table has been transferred. The bus master does not cache PRDs.

The PRD table consists of two DWORDs. The first DWORD contains a 32-bit pointer to a buffer to be transferred. This pointer must be 16-byte aligned. The second DWORD contains the size (16 bits) of the buffer and the EOT flag. The size must be in multiples of 16 bytes. The EOT bit (bit 31) must be set to indicate the last PRD in the PRD table.

Programming Model

The following steps explain how to initiate and maintain a bus master transfer between memory and an IDE device.

1) Software creates a PRD table in system memory. Each PRD entry is 8 bytes long, consisting of a base address pointer and buffer size. The maximum data that can be transferred from a PRD entry is 64 KB. A PRD table must be aligned on a 4-byte boundary. The last PRD in a PRD table must have the EOT bit set.
2) Software loads the starting address of the PRD table by programming the PRD Table Address Register.
3) Software must fill the buffers pointed to by the PRDs with IDE data.
4) Write 1 to the Bus Master Interrupt bit and Bus Master Error (Status Register bits 2 and 1) to clear the bits.
5) Set the correct direction to the Read or Write Control bit (Command Register bit 3).
6) Engage the bus master by writing a “1” to the Bus Master Control bit (Command Register bit 0).
7) The bus master reads the PRD entry pointed to by the PRD Table Address Register and increments the address by 08h to point to the next PRD. The transfer begins.
8) The bus master transfers data to/from memory responding to bus master requests from the IDE device. At the completion of each PRD, the bus master’s next response depends on the settings of the EOT flag in the PRD. If the EOT bit is set, then the IDE bus master clears the Bus Master Active bit (Status Register bit 0) and stops. If any errors occurred during the transfer, the bus master sets the Bus Master Error bit (Status Register bit 1).

Table 4-59. Physical Region Descriptor Format

	Byte 3								Byte 2								Byte 1								Byte 0							
DWORD	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Memory Region Physical Base Address [31:4] (IDE Data Buffer)																												0	0	0	0
1	EOT	Reserved															Size [15:4]												0	0	0	0

4.6.2.3 Ultra DMA/33 Mode

The CS5530A supports Ultra DMA/33. It utilizes the standard IDE Bus Master functionality to interface, initiate, and control the transfer. Ultra DMA/33 definition also incorporates a Cyclic Redundancy Check (CRC) error checking protocol to detect errors.

The Ultra DMA/33 protocol requires no extra signal pins on the IDE connector. The CS5530A redefines three standard IDE control signals when in Ultra DMA/33 mode. These definitions are shown in Table 4-60.

Table 4-60. Ultra DMA/33 Signal Definitions

CS5530A IDE Channel Signal	Ultra DMA/33 Read Cycle	Ultra DMA/33 Write Cycle
IDE_IOW#	STOP	STOP
IDE_IOR#	DMARDY#	STROBE
IDE_IORDY	STROBE	DMARDY#

All other signals on the IDE connector retain their functional definitions during the Ultra DMA/33 operation.

IDE_IOW# is defined as STOP for both read and write transfers to request to stop a transaction.

IDE_IOR# is redefined as DMARDY# for transferring data from the IDE device to the CS5530A. It is used by the CS5530A to signal when it is ready to transfer data and to add wait states to the current transaction. IDE_IOR# signal is defined as STROBE for transferring data from the CS5530A to the IDE device. It is the data strobe signal driven by the CS5530A on which data is transferred during each rising and falling edge transition.

IDE_IORDY is redefined as STROBE for transferring data from the IDE device to the CS5530A during a read cycle. It is the data strobe signal driven by the IDE device on which data is transferred during each rising and falling edge transition. IDE_IORDY is defined as DMARDY# during a write cycle for transferring data from the CS5530A to the IDE device. It is used by the IDE device to signal when it is ready to transfer data and to add wait states to the current transaction.

Ultra DMA/33 data transfer consists of three phases, a startup phase, a data transfer phase and a burst termination phase.

The IDE device begins the startup phase by asserting IDE_DREQ. When ready to begin the transfer, the CS5530A asserts IDE_DACK#. When IDE_DACK# is asserted, the CS5530A drives IDE_CS0# and IDE_CS1# asserted, and IDE_ADDR[2:0] low. For write cycles, the CS5530A negates STOP, waits for the IDE device to assert DMARDY#, and then drives the first data WORD and STROBE signal. For read cycles, the CS5530A negates STOP, and asserts DMARDY#. The IDE device then sends the first data WORD and asserts STROBE.

The data transfer phase continues the burst transfers with the CS5530A and the IDE via providing data, toggling STROBE and DMARDY#. IDE_DATA[15:0] is latched by the receiver on each rising and falling edge of STROBE. The transmitter can pause the burst cycle by holding STROBE high or low, and resume the burst cycle by again toggling STROBE. The receiver can pause the burst cycle by negating DMARDY# and resumes the burst cycle by asserting DMARDY#.

The current burst cycle can be terminated by either the transmitter or the receiver. A burst cycle must first be paused as described above before it can be terminated. The CS5530A can then stop the burst cycle by asserting STOP, with the IDE device acknowledging by negating IDE_DREQ. The IDE device stops the burst cycle by negating IDE_DREQ and the CS5530A acknowledges by asserting STOP. The transmitter then drives the STROBE signal to a high level. The CS5530A then puts the result of the CRC calculation onto IDE_DATA[15:0] while deasserting IDE_DACK#. The IDE device latches the CRC value on the rising edge of IDE_DACK#.

The CRC value is used for error checking on Ultra DMA/33 transfers. The CRC value is calculated for all data by both the CS5530A and the IDE device during the Ultra DMA/33 burst transfer cycles. This result of the CRC calculation is based on all data transferred with a valid STROBE edge while IDE_DACK# is asserted. At the end of the burst transfer, the CS5530A drives the result of the CRC calculation onto IDE_DATA[15:0] which is then strobed by the deassertion of IDE_DACK#. The IDE device compares the CRC result of the CS5530A to its own and reports an error if there is a mismatch.

The timings for Ultra DMA/33 are programmed into the DMA control registers:

- Channel 0 Drive 0 DMA Control Register (F2BAR+I/O Offset 24h)
- Channel 0 Drive 1 DMA Control Register (F2BAR+I/O Offset 2Ch)
- Channel 1 Drive 0 DMA Control Register (F2BAR+I/O Offset 34h)
- Channel 1 Drive 1 DMA Control Register (F2BAR+I/O Offset 3Ch)

The bit formats for these registers are given in Table 4-61. Note that F2BAR+I/O Offset 24h[20] is used to select either Multiword or Ultra DMA mode. Bit 20 = 0 selects Multiword DMA mode. If bit 20 = 1, then Ultra DMA/33 mode is selected. Once mode selection is made using this bit, the remaining DMA Control Registers also operate in the selected mode.

Also listed in the bit formats are recommended values for both Multiword DMA Modes 0-2 and Ultra DMA/33 Modes 0-2.

Note: These are only recommended settings and are not 100% tested.

Table 4-61. MDMA/UDMA Control Registers

Bit	Description
F2BAR+I/O Offset 24h-27h	**Channel 0 Drive 0 DMA Control Register (R/W)** **Reset Value = 00077771h**
If bit 20 = 0, Multiword DMA Settings for: Multiword DMA Mode 0 = 00077771h Multiword DMA Mode 1 = 00012121h Multiword DMA Mode 2 = 00002020h	
31	**PIO Mode Format:** 0 = Format 0; 1 = Format 1.
30:21	**Reserved:** Set to 0.
20	**DMA Operation:** 0 = Multiword DMA; 1 = Ultra DMA.
19:16	**tKR:** IDE_IOR# recovery time (4-bit) (value + 1 cycle)
15:12	**tDR:** IDE_IOR# pulse width (value + 1 cycle)
11:8	**tKW:** IDE_IOW# recovery time (4-bit) (value + 1 cycle)
7:4	**tDW:** IDE_IOW# pulse width (value + 1 cycle)
3:0	**tM:** IDE_CS0#/CS1# to IDE_IOR#/IOW# setup; IDE_CS0#/CS1# setup to IDE_DACK0#/DACK1#
If bit 20 = 1, Ultra DMA Settings for: Ultra DMA Mode 0 = 00921250h Ultra DMA Mode 1 = 00911140h Ultra DMA Mode 2 = 00911030h	
31	**PIO Mode Format:** 0 = Format 0; 1 = Format 1.
30:21	**Reserved:** Set to 0.
20	**DMA Operation:** 0 = Multiword DMA, 1 = Ultra DMA.
19:16	**tCRC:** CRC setup UDMA in IDE_DACK# (value + 1 cycle) (for host terminate CRC setup = tMLI + tSS)
15:12	**tSS:** UDMA out (value + 1 cycle)
11:8	**tCYC:** Data setup and cycle time UDMA out (value + 2 cycles)
7:4	**tRP:** Ready to pause time (value + 1 cycle). Note: tRFS + 1 tRP on next clock.
3:0	**tACK:** IDE_CS0#/CS1# setup to IDE_DACK0#/DACK1# (value + 1 cycle)
Offset 2Ch-2Fh	**Channel 0 Drive 1 DMA Control Register (R/W)** **Reset Value = 00017771h**
Channel 0 Drive 1 MDMA/UDMA Control Register: Refer to F2BAR+I/O Offset 24h for bit descriptions. **Note:** Once the PIO Mode Format is selected in F2BAR+I/O Offset 24h[31], bit 31 of this register is defined as reserved, read only.	
Offset 34h-37h	**Channel 1 Drive 0 DMA Control Register (R/W)** **Reset Value = 00017771h**
Channel 1 Drive 0 MDMA/UDMA Control Register: Refer to F2BAR+I/O Offset 24h for bit descriptions. **Note:** Once the PIO Mode Format is selected in F2BAR+I/O Offset 24h[31], bit 31 of this register is defined as reserved, read only.	
Offset 3Ch-3Fh	**Channel 1 Drive 1 DMA Control Register (R/W)** **Reset Value = 00017771h**
Channel 1 Drive 1 MDMA/UDMA Control Register: Refer to F2BAR+I/O Offset 24h for bit descriptions. **Note:** Once the PIO Mode Format is selected in F2BAR+I/O Offset 24h[31], bit 31 of this register is defined as reserved, read only.	

4.7 XpressAUDIO™ Subsystem

Through XpressAUDIO™ architecture, the CS5530A offers a combined hardware/software support solution to meet industry standard audio requirements. The XpressAUDIO architecture uses Virtual System Architecture™ (VSA) technology along with additional hardware features to provide the necessary support for industry standard 16-bit stereo synthesis and OPL3 emulation.

The hardware portion of the XpressAUDIO subsystem is for transporting streaming audio data to/from the system memory and an AC97 codec. This hardware includes:

- Six (three inbound/three outbound) buffered PCI bus mastering engines that drive specific AC97 interface slots.
- Interfaces to AC97 codecs for audio input/output.

Additional hardware provides the necessary functionality for VSA technology. This hardware includes the ability to:

- Generate an SMI to alert software to update required data. An SMI is generated when either audio buffer is half empty or full. If the buffers become completely empty or full, the Empty bit is asserted.
- Generate an SMI on I/O traps.
- Trap accesses for sound card compatibility at either I/O Port 220h-22Fh, 240h-24Fh, 260h-26Fh, or 280h-28Fh.
- Trap accesses for FM compatibility at I/O Port 388h-38Bh.
- Trap accesses for MIDI UART interface at I/O Port 300h-301h or 330h-331h.
- Trap accesses for serial input and output at COM2 (I/O Port 2F8h-2FFh) or COM4 (I/O Port 2E8h-2EFh).
- Support trapping for low (I/O Port 00h-0Fh) and/or high (I/O Port C0h-DFh) DMA accesses.
- Support hardware status register reads in CS5530A, minimizing SMI overhead.
- Support is provided for software-generated IRQs on IRQ 2, 3, 5, 7, 10, 11, 12, 13, 14, and 15.

Included in the following subsections are details regarding the registers used for configuring the audio interface. The registers are accessed through F3 Index 10h, the Base Address Register (F3BAR) in Function 3. F3BAR sets the base address for XpressAUDIO subsystem support registers as shown in Table 4-62.

4.7.1 Subsystem Data Transport Hardware

The data transport hardware can be broadly divided into two sections: bus mastering and the codec interface.

4.7.1.1 Audio Bus Masters

The CS5530A audio hardware includes six PCI bus masters (three for input and three for output) for transferring digitized audio between memory and the external codec. With these bus master engines, the CS5530A off-loads the CPU and improves system performance.

The programming interface defines a simple scatter/gather mechanism allowing large transfer blocks to be scattered to or gathered from memory. This cuts down on the number of interrupts to and interactions with the CPU.

Table 4-62. Base Address Register (F3BAR) for XpressAUDIO™ Subsystem Support Registers

Bit	Description
f3 Index 10h-13h	**Base Address Register - F3BAR (R/W)** **Reset Value = 00000000h**
This register sets the base address of the memory mapped audio interface control register block. This is a 128-byte block of registers used to control the audio FIFO and codec interface, as well as to support SMIs produced by VSA technology. Bits [6:0] are read only (0000 0000), indicating a 128-byte memory address range. Refer to Table 5-21 for the bit formats and reset values of the XpressAUDIO subsystem support registers.	
31:7	**Audio Interface Base Address**
6:0	**Address Range (Read Only)**

The six bus masters that directly drive specific slots on the AC97 interface:

- Audio Bus Master 0
  - — Output to codec
  - — PCI read
  - — 32-Bit
  - — Left and right channels
  - — Slots 3 and 4
- Audio Bus Master 1
  - — Input from codec
  - — PCI write
  - — 32-Bit
  - — Left and right channels
  - — Slots 3 and 4
- Audio Bus Master 2
  - — Output to codec
  - — PCI read
  - — 16-Bit
  - — Slot 5
- Audio Bus Master 3
  - — Input from codec
  - — PCI write
  - — 16-Bit
  - — Slot 5
- Audio Bus Master 4
  - — Output to codec
  - — PCI read
  - — 16-Bit
  - — Slot 6 or 11 (F3BAR+Memory Offset 08h[19] selects slot)
- Audio Bus Master 5
  - - Input from codec
  - — PCI write
  - — 16-Bit
  - — Slot 6 or 11 (F3BAR+Memory Offset 08h[20] selects slot)

Bus Master Audio Configuration Registers

The format for the bus master audio configuration registers is similar in that each bus master has a Command Register, an SMI Status Register and a PRD Table Address Register. Programming of the bus masters is generic in many ways, although specific programming is required of bit 3 in the Command Register. This bit selects read or write control and is dependent upon which Audio Bus Master is being programmed. For example, Audio Bus Master 0 is defined as an output only, so bit 3 of Audio Bus Master 0 Command Register (F3BAR+Memory Offset 20h[3]) must always be set to 1.

Table 4-63. Generic Bit Formats for Audio Bus Master Configuration Registers

Bit	Description
Command Register (R/W)	
7:4	**Reserved:** Set to 0. Must return 0 on reads.
3	**Read or Write Control:** Set the transfer direction of Audio Bus Master X: 0 = Memory reads performed (output to codec); 1 = Memory writes performed (input from codec). This bit should not be changed when the bus master is active. The setting of this bit is dependent upon the assigned bus master.
2:1	**Reserved:** Set to 0. Must return 0 on reads.
0	**Bus Master Control:** Controls the state of the Audio Bus Master X: 0 = Disable; 1 = Enable. Setting this bit to 1 enables the bus master to begin data transfers. When writing this bit to 0, the bus master must either be paused or have reached EOT. Writing this bit to 0 while the bus master is operating results in unpredictable behavior including the possibility of the bus master state machine crashing. The only recovery from this condition is a PCI reset.
Note: This register must be read and written as a BYTE.	
SMI Status Register (RC)	
7:2	**Reserved (Read to Clear)**
1	**Bus Master Error (Read to Clear):** Hardware encountered a second EOP (end of page) before software has cleared the first? 0 = No; 1 = Yes. If hardware encounters a second EOP before software has cleared the first, it causes the bus master to pause until this register is read to clear the error. Must be R/W as a byte.
0	**End of Page (Read to Clear**): Bus master transferred data which is marked by EOP bit in the PRD table (bit 30)? 0 = No; 1 = Yes.
Note: Must be read and written as a BYTE.	
PRD Table Address (R/W)	
31:2	**Pointer to the Physical Region Descriptor Table:** This register is a PRD table pointer for Audio Bus Master X. When written, this register points to the first entry in a PRD table. Once Audio Bus Master X is enabled (Command Register bit 0 = 1], it loads the pointer and updates this register to the next PRD by adding 08h. When read, this register points to the next PRD.
1:0	**Reserved:** Set to 0.

Table 4-63 on page 119 explains the generic format for the six audio bus masters. Table 4-64 gives the register locations, reset values and specific programming information of bit 3, Read or Write Control, in the Command Register for the Audio Bus Masters.

Table 4-64. Audio Bus Master Configuration Register Summary

Bit	Description	
Audio Bus Master 0: Output to Codec; 32-Bit; Left and Right Channels; Slots 3 and 4.		
F3BAR+Memory Offset 20h	**Command Register (R/W)**	**Reset Value = 00h**
F3BAR+Memory Offset 21h	**SMI Status Register (RC)**	**Reset Value = 00h**
F3BAR+Memory Offset 22h-23h	**Reserved**	**Reset Value = xxh**
F3BAR+Memory Offset 24h-27h	**PRD Table Address (R/W)**	**Reset Value = 00000000h**
Refer to Table 4-63 on page 119 for bit descriptions.		
Note: Bit 3 of the Command Register must be set to 0 (memory read) for correct operation.		
Audio Bus Master 1: Input from Codec; 32-Bit; Left and Right Channels; Slots 3 and 4.		
F3BAR+Memory Offset 28h	**Command Register (R/W)**	**Reset Value = 00h**
F3BAR+Memory Offset 29h	**SMI Status Register (RC)**	**Reset Value = 00h**
F3BAR+Memory Offset 2Ah-2Bh	**Reserved**	**Reset Value = xxh**
F3BAR+Memory Offset 2Ch-2Fh	**PRD Table Address (R/W)**	**Reset Value = 00000000h**
Refer to Table 4-63 on page 119 for bit descriptions.		
Note: Bit 3 of the Command Register must be set to 1 (memory write) for correct operation.		
Audio Bus Master 2: Output to Codec; 16-Bit; Slot 5.		
F3BAR+Memory Offset 30h	**Command Register (R/W)**	**Reset Value = 00h**
F3BAR+Memory Offset 31h	**SMI Status Register (RC)**	**Reset Value = 00h**
F3BAR+Memory Offset 32h-33h	**Reserved**	**Reset Value = xxh**
F3BAR+Memory Offset 34h-37h	**PRD Table Address (R/W)**	**Reset Value = 00000000h**
Refer to Table 4-63 on page 119 for bit descriptions.		
Note: Bit 3 of the Command Register must be set to 0 (memory read) for correct operation.		
Audio Bus Master 3: Input from Codec; 16-Bit; Slot 5.		
F3BAR+Memory Offset 38h	**Command Register (R/W)**	**Reset Value = 00h**
F3BAR+Memory Offset 39h	**SMI Status Register (RC)**	**Reset Value = 00h**
F3BAR+Memory Offset 3Ah-3Bh	**Reserved**	**Reset Value = xxh**
F3BAR+Memory Offset 3Ch-3Fh	**PRD Table Address (R/W)**	**Reset Value = 00000000h**
Refer to Table 4-63 for bit descriptions.		
Note: Bit 3 of the Command Register must be set to 1 (memory write) for correct operation.		
Audio Bus Master 4: Output to Codec; 16-Bit; Slot 6 or 11 (F3BAR+Memory Offset 08h[19] selects slot).		
F3BAR+Memory Offset 40h	**Command Register (R/W)**	**Reset Value = 00h**
F3BAR+Memory Offset 41h	**SMI Status Register (RC)**	**Reset Value = 00h**
F3BAR+Memory Offset 42h-43h	**Reserved**	**Reset Value = xxh**
F3BAR+Memory Offset 44h-47h	**PRD Table Address (R/W)**	**Reset Value = 00000000h**
Refer to Table 4-63 on page 119 for bit descriptions.		
Note: Bit 3 of the Command Register must be set to 0 (memory read) for correct operation.		
Audio Bus Master 5: Input from Codec; 16-Bit; Slot 6 or 11 (F3BAR+Memory Offset 08h[20] selects slot).		
F3BAR+Memory Offset 48h	**Command Register (R/W)**	**Reset Value = 00h**
F3BAR+Memory Offset 49h	**SMI Status Register (RC)**	**Reset Value = 00h**
F3BAR+Memory Offset 4Ah-4Bh	**Reserved**	**Reset Value = xxh**
F3BAR+Memory Offset 4Ch-4Fh	**PRD Table Address (R/W)**	**Reset Value = 00000000h**
Refer to Table 4-63 on page 119 for bit descriptions.		
Note: Bit 3 of the Command Register must be set to 1 (memory write) for correct operation.		

4.7.1.2 Physical Region Descriptor Table Address

Before the bus master starts a master transfer it must be programmed with a pointer (PRD Table Address Register) to a Physical Region Descriptor Table. This pointer sets the starting memory location of the Physical Region Descriptors (PRDs). The PRDs describe the areas of memory that are used in the data transfer. The descriptor table entries must be aligned on a 4-byte boundary and the table cannot cross a 64 KB boundary in memory.

4.7.1.3 Physical Region Descriptor Format

Each physical memory region to be transferred is described by a Physical Region Descriptor (PRD) as illustrated in Table 4-65. When the bus master is enabled (Command Register bit 0 = 1), data transfer proceeds until each PRD in the PRD table has been transferred. The bus master does not cache PRDs.

The PRD table consists of two DWORDs. The first DWORD contains a 32-bit pointer to a buffer to be transferred. The second DWORD contains the size (16 bits) of the buffer and flags (EOT, EOP, JMP). The description of the flags are as follows:

- EOT bit - If set in a PRD, this bit indicates the last entry in the PRD table (bit 31). The last entry in a PRD table must have either the EOT bit or the JMP bit set. A PRD can not have both the JMP and EOT bits set.
- EOP bit - If set in a PRD and the bus master has completed the PRD's transfer, the End of Page bit is set (Status Register bit 0 = 1) and an SMI is generated. If a second EOP is reached due to the completion of another PRD before the End of Page bit is cleared, the Bus Master Error bit is set (Status Register bit 1 = 1) and the bus master pauses. In this paused condition, reading the Status Register clears both the Bus Master Error and the End of Page bits and the bus master continues.
- JMP bit - This PRD is special. If set, the Memory Region Physical Base Address is now the target address of the JMP. There is no data transfer with this PRD. This PRD allows the creation of a looping mechanism. If a PRD table is created with the JMP bit set in the last PRD, the PRD table does not need a PRD with the EOT bit set. A PRD can not have both the JMP and EOT bits set.

Table 4-65. Physical Region Descriptor Format

	Byte 3								Byte 2								Byte 1								Byte 0							
DWORD	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	Memory Region Base Address [31:1] (Audio Data Buffer)																															0
1	EOT	EOP	JMP	Reserved													Size [15:1]															0

4.7.1.4 Programming Model

The following discussion explains, in steps, how to initiate and maintain a bus master transfer between memory and an audio slave device.

In the steps listed below, the reference to “Example” refers to Figure 4-20, PRD Table Example.

1) Software creates a PRD table in system memory. Each PRD entry is 8 bytes long; consisting of a base address pointer and buffer size. The maximum data that can be transferred from a PRD entry is 64 KB. A PRD table must be aligned on a 4-byte boundary. The last PRD in a PRD table must have the EOT or JMP bit set.

   Example - Assume the data is outbound. There are three PRDs in the example PRD table. The first two PRDs (PRD_1, PRD_2) have only the EOP bit set. The last PRD (PRD_3) has only the JMP bit set. This example creates a PRD loop.

2) Software loads the starting address of the PRD table by programming the PRD Table Address Register.

   Example - Program the PRD Table Address Register with Address_3.

3) Software must fill the buffers pointed to by the PRDs with audio data. It is not absolutely necessary to fill the buffers; however, the buffer filling process must stay ahead of the buffer emptying. The simplest way to do this is by using the EOP flags to generate an SMI when a PRD is empty.

   Example - Fill Audio Buffer_1 and Audio Buffer_2. The SMI generated by the EOP from the first PRD allows the software to refill Audio Buffer_1. The second SMI will refill Audio Buffer_2. The third SMI will refill Audio Buffer_2 and so on.

4) Read the SMI Status Register to clear the Bus Master Error and End of Page bits (bits 1 and 0).

   Set the correct direction to the Read or Write Control bit (Command Register bit 3). Note that the direction of the data transfer of a particular bus master is fixed and therefore the direction bit must be programmed accordingly. It is assumed that the codec has been properly programmed to receive the audio data.

   Engage the bus master by writing a “1” to the Bus Master Control bit (Command Register bit 0).

   The bus master reads the PRD entry pointed to by the PRD Table Address Register and increments the address by 08h to point to the next PRD. The transfer begins.

   Example - The bus master is now properly programmed to transfer Audio Buffer_1 to a specific slot(s) in the AC97 interface.

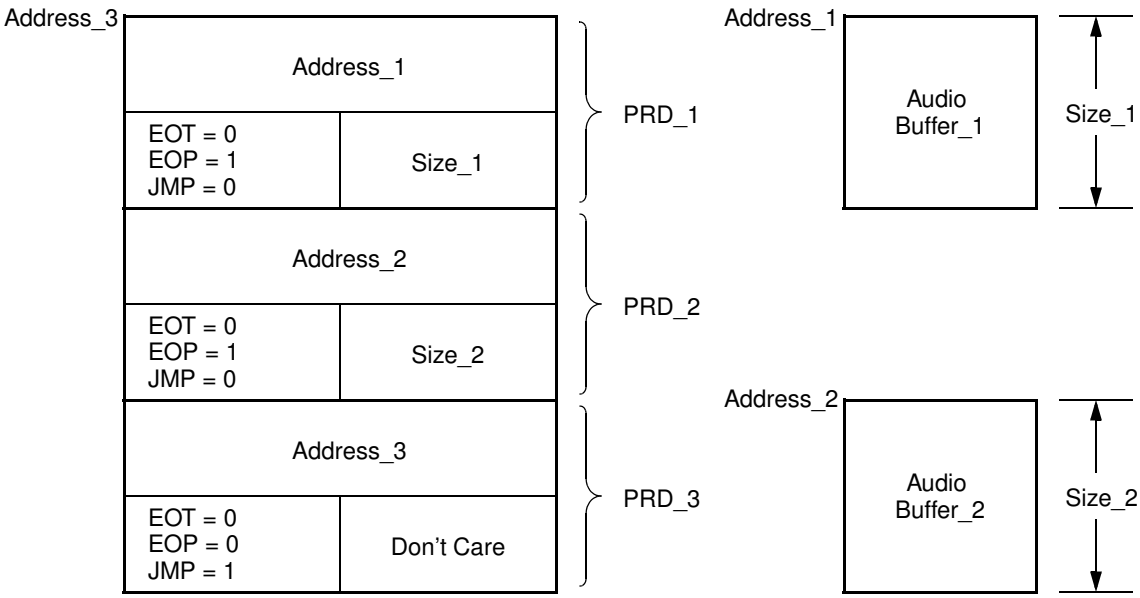


Figure 4-20. PRD Table Example

5) The bus master transfers data to/from memory responding to bus master requests from the AC97 interface. At the completion of each PRD, the bus master's next response depends on the settings of the flags in the PRD.

   Example - At the completion of PRD_1 an SMI is generated because the EOP bit is set while the bus master continues on to PRD_2. The address in the PRD Table Address Register is incremented by 08h and is now pointing to PRD_3. The SMI Status Register is read to clear the End of Page status flag. Since Audio Buffer_1 is now empty, the software can refill it.

   At the completion of PRD_2 an SMI is generated because the EOP bit is set. The bus master then continues on to PRD_3. The address in the PRD Table Address Register is incremented by 08h. The DMA SMI Status Register is read to clear the End of Page status flag. Since Audio Buffer_2 is now empty, the software can refill it. Audio Buffer_1 has been refilled from the previous SMI.

   PRD_3 has the JMP bit set. This means the bus master uses the address stored in PRD_3 (Address_3) to locate the next PRD. It does not use the address in the PRD Table Address Register to get the next PRD. Since Address_3 is the location of PRD_1, the bus master has looped the PRD table.

   Stopping the bus master can be accomplished by not reading the SMI Status Register End of Page status flag. This leads to a second EOP which causes a Bus Master Error and pauses the bus master. In effect, once a bus master has been enabled it never needs to be disabled, just paused. The bus master cannot be disabled unless the bus master has been paused or has reached an EOT.

4.7.1.5 AC97 Codec Interface

The CS5530A provides an AC97 Specification Revision 1.3, 2.0, and 2.1 compatible interface. Any AC97 codec that supports sample rate conversion (SRC) can be used with the CS5530A. This type of codec allows for a design which meets the requirements for PC97 and PC98-compliant audio as defined by Microsoft Corporation.

The AC97 codec is the master of the serial interface and generates the clocks to CS5530A, Figure 4-21 shows the codec and CS5530A signal connections. For specifications on the serial interface, refer to the appropriate codec manufacturer's data sheet.

For PC speaker synthesis, the CS5530A outputs the PC speaker signal on the PC_BEEP pin which is connected to the PC_BEEP input of the AC97 codec.

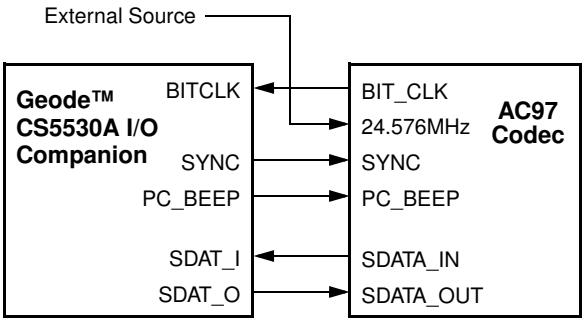


Figure 4-21. AC97 Signal Connections

Codec Configuration/Control Registers

The codec related registers consist of four 32-bit registers:

- Codec GPIO Status Register
- Codec GPIO Control Register
- Codec Status Register
- Codec Command Register

Codec GPIO Status and Control Registers (F3BAR+ Memory Offset 00h and 04h)

The Codec GPIO Status and Control Registers are used for codec GPIO related tasks such as enabling a codec GPIO interrupt to cause an SMI.

Codec Status Register (F3BAR+Memory Offset 08h)

The Codec Status Register stores the codec status word. It updates every valid Status Word slot.

Codec Control Register (F3BAR+Memory Offset 0Ch)

The Codec Control Register writes the control word to the codec. By writing the appropriate control words to this port, the features of the codec can be controlled. The contents of this register are written to the codec during the Control Word slot.

The bit formats for these registers are given in Table 4-66.

Table 4-66. Codec Configuration/Control Registers

Bit	Description
F3BAR+Memory Offset 00h-03h	**Codec GPIO Status Register (R/W)**	**Reset Value = 00100000h**
31	**Codec GPIO Interface:** 0 = Disable; 1 = Enable.
30	**Codec GPIO SMI:** Allow codec GPIO interrupt to generate an SMI. 0 = Disable; 1= Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[1]. Second level SMI status is reported at F3BAR+Memory Offset 10h/12h[1].
29:21	**Reserved:** Set to 0.
20	**Codec GPIO Status Valid (Read Only):** Is the status read valid? 0 = Yes; 1 = No.
19:0	**Codec GPIO Pin Status (Read Only):** This is the GPIO pin status that is received from the codec in slot 12 on SDATA_IN signal.
F3BAR+Memory Offset 04h-07h	**Codec GPIO Control Register (R/W)**	**Reset Value = 00000000h**
31:20	**Reserved:** Set to 0.
19:0	**Codec GPIO Pin Data:** This is the GPIO pin data that is sent to the codec in slot 12 on the SDATA_OUT signal.
F3BAR+Memory Offset 08h-0Bh	**Codec Status Register (R/W)**	**Reset Value = 00000000h**
31:24	**Codec Status Address (Read Only):** Address of the register for which status is being returned. This address comes from slot 1 bits [19:12].
23	**Codec Serial INT SMI:** Allow codec serial interrupt to generate an SMI. 0 = Disable; 1= Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[1]. Second level SMI status is reported at F3BAR+Memory Offset 10h/12h[1].
22	**SYNC Pin:** Selects SYNC pin level. 0 = Low; 1 = High.
21	**Enable SDATA_IN2:** Pin AE24 function selection. 0 = GPIO1; 1 = SDATA_IN2. For this pin to function as SDATA_IN2, it must first be configured as an input (F0 Index 90h[1] = 0).
20	**Audio Bus Master 5 AC97 Slot Select:** Selects slot for Audio Bus Master 5 to receive data. 0 = Slot 6; 1 = Slot 11.
19	**Audio Bus Master 4 AC97 Slot Select:** Selects slot for Audio Bus Master 4 to transmit data. 0 = Slot 6; 1 = Slot 11.
18	**Reserved:** Set to 0.
17	**Status Tag (Read Only):** Determines if the status in bits [15:0] is new or not. 0 = Not new; 1 = New.
16	**Codec Status Valid (Read Only):** Is the status in bits [15:0] valid? 0 = No; 1 = Yes.
15:0	**Codec Status (Read Only):** This is the codec status data that is received from the codec in slot 2 on SDATA_IN. Only bits [19:4] are used from slot 2.
F3BAR+Memory Offset 0Ch-0Fh	**Codec Command Register (R/W)**	**Reset Value = 00000000h**
31:24	**Codec Command Address:** Address of the codec control register for which the command is being sent. This address goes in slot 1 bits [19:12] on SDATA_OUT.
23:22	**CS5530A Codec Communication:** Selects which codec to communicate with. 00 = Primary codec 10 = Third codec 01 = Secondary codec 11 = Fourth codec **Note:** 00 and 01 are the only valid settings for these bits.
21:17	**Reserved:** Set to 0.
16	**Codec Command Valid:** Is the command in bits [15:0] valid? 0 = No; 1 = Yes. This bit is set by hardware when a command is loaded. It remains set until the command has been sent to the codec.
15:0	**Codec Command:** This is the command being sent to the codec in bits [19:12] of slot 2 on SDATA_OUT.

4.7.2 VSA Technology Support Hardware

The CS5530A companion device incorporates the required hardware in order to support the Virtual System Architecture (VSA) technology for capture and playback of audio using an external codec. This eliminates much of the hardware traditionally associated with industry standard audio functions.

XpressAUDIO software provides 16-bit compatible sound. This software is available to OEMs for incorporation into the system BIOS ROM.

4.7.2.1 VSA Technology

VSA technology provides a framework to enable software implementation of traditionally hardware-only components. VSA technology software executes in System Management Mode (SMM), enabling it to execute transparently to the operating system, drivers, and applications.

The VSA technology design is based upon a simple model for replacing hardware components with software. Hardware to be virtualized is merely replaced with simple access detection circuitry which asserts the SMI# (System Management Interrupt) pin when hardware accesses are detected. The current execution stream is immediately preempted, and the processor enters SMM. The SMM system software then saves the processor state, initializes the VSA technology execution environment, decodes the SMI source and dispatches handler routines which have registered requests to service the decoded SMI source. Once all handler routines have completed, the processor state is restored and normal execution resumes. In this manner, hardware accesses are transparently replaced with the execution of SMM handler software.

Historically, SMM software was used primarily for the single purpose of facilitating active power management for notebook designs. That software's only function was to manage the power up and down of devices to save power. With high performance processors now available, it is feasible to implement, primarily in SMM software, PC capabilities traditionally provided by hardware. In contrast to power management code, this virtualization software generally has strict performance requirements to prevent application performance from being significantly impacted.

4.7.2.2 Audio SMI Related Registers

The SMI related registers consist of:

- Second Level Audio SMI Status Registers
- I/O Trap SMI and Fast Write Status Register
- I/O Trap SMI Enable Register

The Top SMI Status Mirror and Status Registers are the top level of hierarchy for the SMI handler in determining the source of an SMI. These two registers are at F1BAR+Memory Offset 00h (Status Mirror) and F1BAR+Memory Offset 02h (Status). The registers are identical except that reading the register at F1BAR+Memory Offset 02h clears the status.

Second Level Audio SMI Status Registers

The second level of audio SMI status reporting is set up very much like the top level. There are two status reporting registers, one "read only" (mirror) and one "read to clear". The data returned by reading either offset is the same (i.e., SMI was caused by an audio related event). The difference between F3BAR+Memory Offset 12h and 10h (mirror) is in the ability to clear the SMI source at 10h.

Figure 4-22 shows an SMI tree for checking and clearing the source of an audio SMI. Only the audio SMI bit is detailed here. For details regarding the remaining bits in the Top SMI Status Mirror and Status Registers refer to Table 5-17 "F1BAR+Memory Offset xxh: SMI Status and ACPI Timer Registers" on page 181.

I/O Trap SMI and Fast Write Status Register

This 32-bit read-only register (F3BAR+Memory Offset 14h) not only indicates if the enabled I/O trap generated an SMI, but also contains Fast Path Write related bits.

I/O Trap SMI Enable Register

The I/O Trap SMI Enable Register (F3BAR+Memory Offset 18h) allows traps for specified I/O addresses and configures generation for I/O events. It also contains the enabling bit for Fast Path Write/Read features.

If Status Fast Path Read is enabled, the CS5530A intercepts and responds to reads to several status registers. This speeds up operations, and prevents SMI generation for reads to these registers. Status Fast Path Read is enabled via F3BAR+Memory Offset 18h[4].

In Status Fast Path Read the CS5530A responds to reads of the following addresses:

388h-38Bh
2x0h, 2x1h, 2x2h, 2x3h, 2x8h, and 2x9h

Note that if neither sound card nor FM I/O mapping is enabled, then status read trapping is not possible.

If Fast Path Write is enabled, the CS5530A captures certain writes to several I/O locations. This feature prevents two SMIs from being asserted for write operations that are known to take two accesses (the first access is an index and the second is data). Fast Path Write is enabled via F3BAR+Memory Offset 18h[11].

Fast Path Write captures the data and address bit 1 (A1) of the first access, but does not generate an SMI. A1 is stored in F3BAR+Memory Offset 14h[15]. The second access causes an SMI, and the data and address are captured as in a normal trapped I/O.

In Fast Path Write, the CS5530A responds to writes to the following addresses:

388h, 38Ah, and 38Bh
2x0h, 2x2h, and 2x8h

Table 4-67 on page 127 and Table 4-68 on page 129 show the bit formats of the second and third level SMI status reporting registers, respectively. Table 4-69 on page 130 shows the sound card I/O trap and Fast Path Read/Write programming bits.

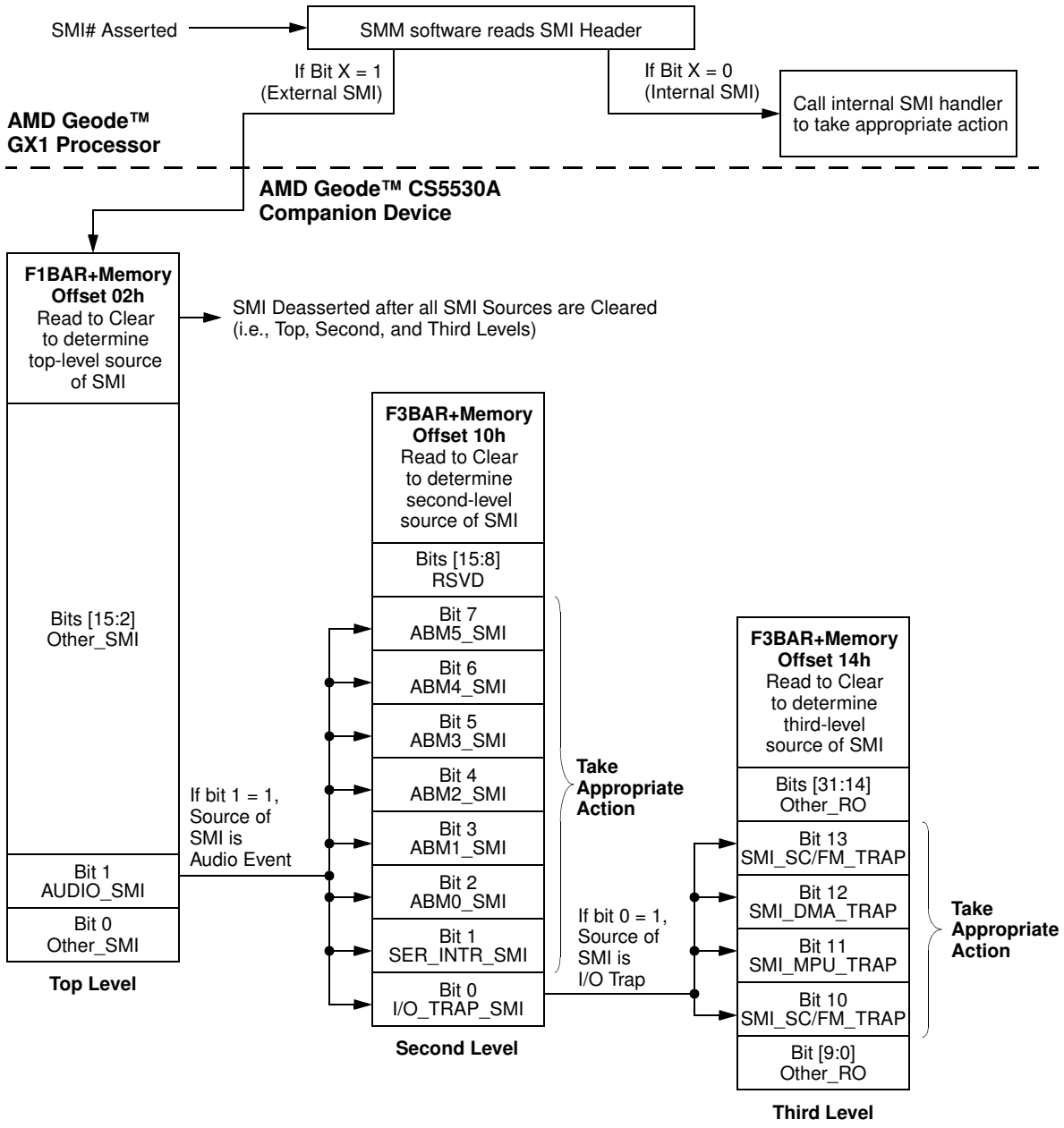


Figure 4-22. Audio SMI Tree Example

Table 4-67. Second Level SMI Status Reporting Registers

Bit	Description
F3BAR+Memory Offset 10h-11h Second Level Audio SMI Status Register (RC) Reset Value = 0000h	
15:8	**Reserved:** Set to 0.
7	**Audio Bus Master 5 SMI Status (Read to Clear):** SMI was caused by an event occurring on Audio Bus Master 5? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 5 is enabled (F3BAR+Memory Offset 48h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 49h[0] = 1).
6	**Audio Bus Master 4 SMI Status (Read to Clear):** SMI was caused by an event occurring on Audio Bus Master 4? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 4 is enabled (F3BAR+Memory Offset 40h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 41h[0] = 1).
5	**Audio Bus Master 3 SMI Status (Read to Clear):** SMI was caused by an event occurring on Audio Bus Master 3? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 3 is enabled (F3BAR+Memory Offset 38h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 39h[0] = 1).
4	**Audio Bus Master 2 SMI Status (Read to Clear):** SMI was caused by an event occurring on Audio Bus Master 2? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 2 is enabled (F3BAR+Memory Offset 30h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 31h[0] = 1).
3	**Audio Bus Master 1 SMI Status (Read to Clear):** SMI was caused by an event occurring on Audio Bus Master 1? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 1 is enabled (F3BAR+Memory Offset 28h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 29h[0] = 1).
2	**Audio Bus Master 0 SMI Status (Read to Clear):** SMI was caused by an event occurring on Audio Bus Master 0? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 0 is enabled (F3BAR+Memory Offset 20h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 21h[0] = 1).
1	**Codec Serial or GPIO Interrupt SMI Status (Read to Clear):** SMI was caused by a serial or GPIO interrupt from codec? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation enabling for codec serial interrupt: F3BAR+Memory Offset 08h[23] = 1. SMI generation enabling for codec GPIO interrupt: F3BAR+Memory Offset 00h[30] = 1.
0	**I/O Trap SMI Status (Read to Clear):** SMI was caused by an I/O trap? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The next level (third level) of SMI status reporting is at F3BAR+Memory Offset 14h. The top level is reported at F1BAR+Memory Offset 00h/02h[1].
Note: Reading this register clears the status bits. Note that bit 0 has another level (third) of SMI status reporting. A read-only “Mirror” version of this register exists at F3BAR+Memory Offset 12h. If the value of the register must be read without clearing the SMI source (and consequently deasserting SMI), the Mirror register may be read instead.	
F3BAR+Memory Offset 12h-13h Second Level Audio SMI Status Mirror Register (RO) Reset Value = 0000h	
15:8	**Reserved:** Set to 0.
7	**Audio Bus Master 5 SMI Status (Read Only):** SMI was caused by an event occurring on Audio Bus Master 5? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 5 is enabled (F3BAR+Memory Offset 48h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 49h[0] = 1).

Table 4-67. Second Level SMI Status Reporting Registers (Continued)

Bit	Description
6	**Audio Bus Master 4 SMI Status (Read Only):** SMI was caused by an event occurring on Audio Bus Master 4? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 4 is enabled (F3BAR+Memory Offset 40h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 41h[0] = 1).
5	**Audio Bus Master 3 SMI Status (Read Only):** SMI was caused by an event occurring on Audio Bus Master 3? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 3 is enabled (F3BAR+Memory Offset 38h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 39h[0] = 1).
4	**Audio Bus Master 2 SMI Status (Read Only):** SMI was caused by an event occurring on Audio Bus Master 2? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 2 is enabled (F3BAR+Memory Offset 30h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 31h[0] = 1).
3	**Audio Bus Master 1 SMI Status (Read Only):** SMI was caused by an event occurring on Audio Bus Master 1? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 1 is enabled (F3BAR+Memory Offset 28h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 29h[0] = 1).
2	**Audio Bus Master 0 SMI Status (Read Only):** SMI was caused by an event occurring on Audio Bus Master 0? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 0 is enabled (F3BAR+Memory Offset 20h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 21h[0] = 1).
1	**Codec Serial or GPIO Interrupt SMI Status (Read Only):** SMI was caused by a serial or GPIO interrupt from codec? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation enabling for codec serial interrupt: F3BAR+Memory Offset 08h[23] = 1. SMI generation enabling for codec GPIO interrupt: F3BAR+Memory Offset 00h[30] = 1.
0	**I/O Trap SMI Status (Read Only):** SMI was caused by an I/O trap? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The next level (third level) of SMI status reporting is at F3BAR+Memory Offset 14h. The top level is reported at F1BAR+Memory Offset 00h/02h[1].
Note: Reading this register does not clear the status bits. See F3BAR+Memory Offset 10h.	

Table 4-68. Third Level SMI Status Reporting Registers

Bit	Description
F3BAR+Memory Offset 14h-17h I/O Trap SMI and Fast Write Status Register (RO/RC) Reset Value = 00000000h	
31:24	**Fast Path Write Even Access Data (Read Only):** These bits contain the data from the last Fast Path Write Even access. These bits change only on a fast write to an even address.
23:16	**Fast Path Write Odd Access Data (Read Only):** These bits contain the data from the last Fast Path Write Odd access. These bits change on a fast write to an odd address, and also on any non-fast write.
15	**Fast Write A1 (Read Only):** This bit contains the A1 value for the last Fast Write access.
14	**Read or Write I/O Access (Read Only):** Last trapped I/O access was a read or a write? 0 = Read; 1 = Write.
13	**Sound Card or FM Trap SMI Status (Read to Clear):** SMI was caused by a trapped I/O access to the sound card or FM I/O Trap? 0 = No; 1 = Yes. (Note) Fast Path Write must be enabled, F3BAR+Memory Offset 18h[11] = 1, for the SMI to be reported here. If Fast Path Write is disabled, the SMI is reported in bit 10 of this register. This is the third level of SMI status reporting. The second level of SMI status is reported at F3BAR+Memory Offset 10h/12h[0]. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation enabling is at F3BAR+Memory Offset 18h[2].
12	**DMA Trap SMI Status (Read to Clear):** SMI was caused by a trapped I/O access to the DMA I/O Trap? 0 = No; 1 = Yes. (Note) This is the third level of SMI status reporting. The second level of SMI status is reported at F3BAR+Memory Offset 10h/12h[0]. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation enabling is at F3BAR+Memory Offset 18h[8:7].
11	**MPU Trap SMI Status (Read to Clear):** SMI was caused by a trapped I/O access to the MPU I/O Trap? 0 = No; 1 = Yes. (Note) This is the third level of SMI status reporting. The second level of SMI status is reported at F3BAR+Memory Offset 10h/12h[0]. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation enabling is at F3BAR+Memory Offset 18h[6:5].
10	**Sound Card or FM Trap SMI Status (Read to Clear):** SMI was caused by a trapped I/O access to the sound card or FM I/O Trap? 0 = No; 1 = Yes. (Note) Fast Path Write must be disabled, F3BAR+Memory Offset 18h[11] = 0, for the SMI to be reported here. If Fast Path Write is enabled, the SMI is reported in bit 13 of this register. This is the third level of SMI status reporting. The second level of SMI status is reported at F3BAR+Memory Offset 10h/12h[0]. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation enabling is at F3BAR+Memory Offset 18h[2].
9:0	**X-Bus Address (Read Only):** Bits [9:0] contain the captured ten bits of X-Bus address.
Note: For the four SMI status bits (bits [13:10]), if the activity was a fast write to an even address, no SMI is generated regardless of the DMA, MPU, or sound card status. If the activity was a fast write to an odd address, an SMI is generated but bit 13 is set to a 1.	

Table 4-69. Sound Card I/O Trap and Fast Path Enable Registers

Bit	Description
F3BAR+Memory Offset 18h-19h	**I/O Trap SMI Enable Register (R/W)**	**Reset Value = 0000h**
15:12	**Reserved:** Set to 0.
11	**Fast Path Write Enable:** Fast Path Write (an SMI is not generated on certain writes to specified addresses). 0 = Disable; 1 = Enable. In Fast Path Write, the CS5530A responds to writes to the following addresses: 388h, 38Ah and 38Bh; 2x0h, 2x2h, and 2x8h.
10:9	**Fast Read:** These two bits hold part of the response that the CS5530A returns for reads to several I/O locations.
8	**High DMA I/O Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs at I/O Port C0h-DFh, an SMI is generated. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[1]. Second level SMI status is reported at F3BAR+Memory Offset 10h/12h[0]. Third level SMI status is reported at F3BAR+Memory Offset 14h[12].
7	**Low DMA I/O Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs at I/O Port 00h-0Fh, an SMI is generated. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[1]. Second level SMI status is reported at F3BAR+Memory Offset 10h/12h[0]. Third level SMI status is reported at F3BAR+Memory Offset 14h[12].
6	**High MPU I/O Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs at I/O Port 330h and 331h, an SMI is generated. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[1]. Second level SMI status is reported at F3BAR+Memory Offset 10h/12h[0]. Third level SMI status is reported at F3BAR+Memory Offset 14h[11].
5	**Low MPU I/O Trap:** I0 = Disable; 1 = Enable. If this bit is enabled and an access occurs at I/O Port 300h and 301h, an SMI is generated. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[1]. Second level SMI status is reported at F3BAR+Memory Offset 10h/12h[0]. Third level SMI status is reported at F3BAR+Memory Offset 14h[11].
4	**Fast Path Read Enable/SMI Disable:** Read Fast Path (an SMI is not generated on reads from specified addresses). 0 = Disable; 1 = Enable. In Fast Path Read the CS5530A responds to reads of the following addresses: 388h-38Bh; 2x0h, 2x1h, 2x2h, 2x3h, 2x8h and 2x9h. Note that if neither sound card nor FM I/O mapping is enabled, then status read trapping is not possible.
3	**FM I/O Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs at I/O Port 388h to 38Bh, an SMI is generated. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[1]. Second level SMI status is reported at F3BAR+Memory Offset 10h/12h[0].
2	**Sound Card I/O Trap:** 0 = Disable; 1 = Enable If this bit is enabled and an access occurs in the address ranges selected by bits [1:0], an SMI is generated. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[1]. Second level SMI status is reported at F3BAR+Memory Offset 10h/12h[0]. Third level SMI status is reported at F3BAR+Memory Offset 14h[10].
1:0	**Sound Card Address Range Select:** These bits select the address range for the sound card I/O trap. 00 = I/O Port 220h-22Fh 01 = I/O Port 240h-24Fh 10 = I/O Port 260h-26Fh 11 = I/O Port 280h-28Fh

4.7.2.3 IRQ Configuration Registers

The CS5530A provides the ability to set and clear IRQs internally through software control. If the IRQs are configured for software control, they will not respond to external hardware. There are three registers provided for this feature:

- Internal IRQ Enable Register
- Internal IRQ Mask Register
- Internal IRQ Control Register

Internal IRQ Enable Register

This register configures the IRQs as internal (software) interrupts or external (hardware) interrupts. Any IRQ used as an internal software driven source must be configured as internal.

Internal IRQ Mask Register

Each bit in the Mask register individually disables the corresponding bit in the Control Register.

Internal IRQ Control Register

This register allows individual software assertion/deassertion of the IRQs that are enabled as internal and unmasked.

The bit formats for these registers are given in Table 4-70.

Table 4-70. IRQ Configuration Registers

Bit	Description
F3BAR+Memory Offset 1Ah-1Bh	**Internal IRQ Enable Register (R/W)**	**Reset Value = 0000h**
15	**IRQ15 Internal:** Configure IRQ15 for internal (software) or external (hardware) use. 0 = External; 1 = Internal.
14	**IRQ14 Internal:** Configure IRQ14 for internal (software) or external (hardware) use. 0 = External; 1 = Internal.
13	**Reserved:** Set to 0.
12	**IRQ12 Internal:** Configure IRQ12 for internal (software) or external (hardware) use. 0 = External; 1 = Internal.
11	**IRQ11 Internal:** Configure IRQ11 for internal (software) or external (hardware) use. 0 = External; 1 = Internal.
10	**IRQ10 Internal:** Configure IRQ10 for internal (software) or external (hardware) use. 0 = External; 1 = Internal.
9	**IRQ9 Internal:** Configure IRQ9 for internal (software) or external (hardware) use. 0 = External; 1 = Internal.
8	**Reserved:** Set to 0.
7	**IRQ7 Internal:** Configure IRQ7 for internal (software) or external (hardware) use. 0 = External; 1 = Internal.
6	**Reserved:** Set to 0.
5	**IRQ5 Internal:** Configure IRQ5 for internal (software) or external (hardware) use. 0 = External; 1 = Internal.
4	**IRQ4 Internal:** Configure IRQ4 for internal (software) or external (hardware) use. 0 = External; 1 = Internal.
3	**IRQ3 Internal:** Configure IRQ3 for internal (software) or external (hardware) use. 0 = External; 1 = Internal.
2:0	**Reserved:** Set to 0.
Note: Must be read and written as a WORD.	
F3BAR+Memory Offset 1Ch-1Dh	**Internal IRQ Control Register (R/W)**	**Reset Value = 0000h**
15	**Assert Masked Internal IRQ15:** 0 = Disable; 1 = Enable.
14	**Assert Masked Internal IRQ14:** 0 = Disable; 1 = Enable.
13	**Reserved:** Set to 0.
12	**Assert Masked Internal IRQ12:** 0 = Disable; 1 = Enable.
11	**Assert masked internal IRQ11:** 0 = Disable; 1 = Enable.
10	**Assert Masked Internal IRQ10:** 0 = Disable; 1 = Enable.
9	**Assert Masked Internal IRQ9:** 0 = Disable; 1 = Enable.
8	**Reserved:** Set to 0.
7	**Assert Masked Internal IRQ7:** 0 = Disable; 1 = Enable.
6	**Reserved:** Set to 0.
5	**Assert Masked Internal IRQ5:** 0 = Disable; 1 = Enable.
4	**Assert Masked Internal IRQ4:** 0 = Disable; 1 = Enable.

Table 4-70. IRQ Configuration Registers (Continued)

Bit	Description
3	**Assert Masked Internal IRQ3:** 0 = Disable; 1 = Enable.
2:0	**Reserved:** Set to 0.
F3BAR+Memory Offset 1Eh-1Fh	**Internal IRQ Mask Register (Write Only)** **Reset Value = xxxxh**
15	**Mask Internal IRQ15:** 0 = Disable; 1 = Enable.
14	**Mask Internal IRQ14:** 0 = Disable; 1 = Enable.
13	**Reserved:** Set to 0.
12	**Mask Internal IRQ12:** 0 = Disable; 1 = Enable.
11	**Mask Internal IRQ11:** 0 = Disable; 1 = Enable.
10	**Mask Internal IRQ10:** 0 = Disable; 1 = Enable.
9	**Mask Internal IRQ9:** 0 = Disable; 1 = Enable.
8	**Reserved:** Set to 0.
7	**Mask Internal IRQ7:** 0 = Disable; 1 = Enable.
6	**Reserved:** Set to 0.
5	**Mask Internal IRQ5:** 0 = Disable; 1 = Enable.
4	**Mask Internal IRQ4:** 0 = Disable; 1 = Enable.
3	**Mask Internal IRQ3:** 0 = Disable; 1 = Enable.
2:0	**Reserved:** Set to 0.

4.8 Display Subsystem Extensions

The CS5530A incorporates extensions to the GX1 processor's' display subsystem. These include:

- Video Interface Configuration Registers
  - — Line Buffers
  - — Video Port Protocol
  - — Video Format
  - — X and Y Scaler / Filter
  - — Color-Space-Converter
- Video Accelerator
- Gamma RAM
- Display Interface
  - — Video DACs
  - — VESA DDC2B / DPMS
  - — Flat Panel Support

Figure 4-23 shows the data path of the display subsystem extensions.

4.8.1 Video Interface Configuration Registers

Registers for configuring the video interface are accessed through F4 Index 10h, the Base Address Register (F4BAR) in Function 4. F4BAR sets the base address for the Video Interface Configuration Registers as shown in Table 4-71.

Note: All Video Interface Configuration Registers have a 32-bit access granularity (only).

The following subsections describe the video interface and the registers used for programming purposes. However, for complete bit information refer to Section 5.3.5 "Video Controller Registers - Function 4" on page 198.

Table 4-71. Base Address Register (F4BAR) for Video Controller Support Registers

Bit	Description
F4 Index 10h-13h	**Base Address Register — F4BAR (R/W)** **Reset Value = 00000000h**
This register sets the base address of the memory mapped video controller registers. Bits [11:0] are read only (0000 0000 0000), indicating a 4 KB memory address range. Refer to Table 5-23 for the video controller register bit formats and reset values.	
31:12	**Video Controller and Clock Control Base I/O Address**
11:0	**Address Range (Read Only)**

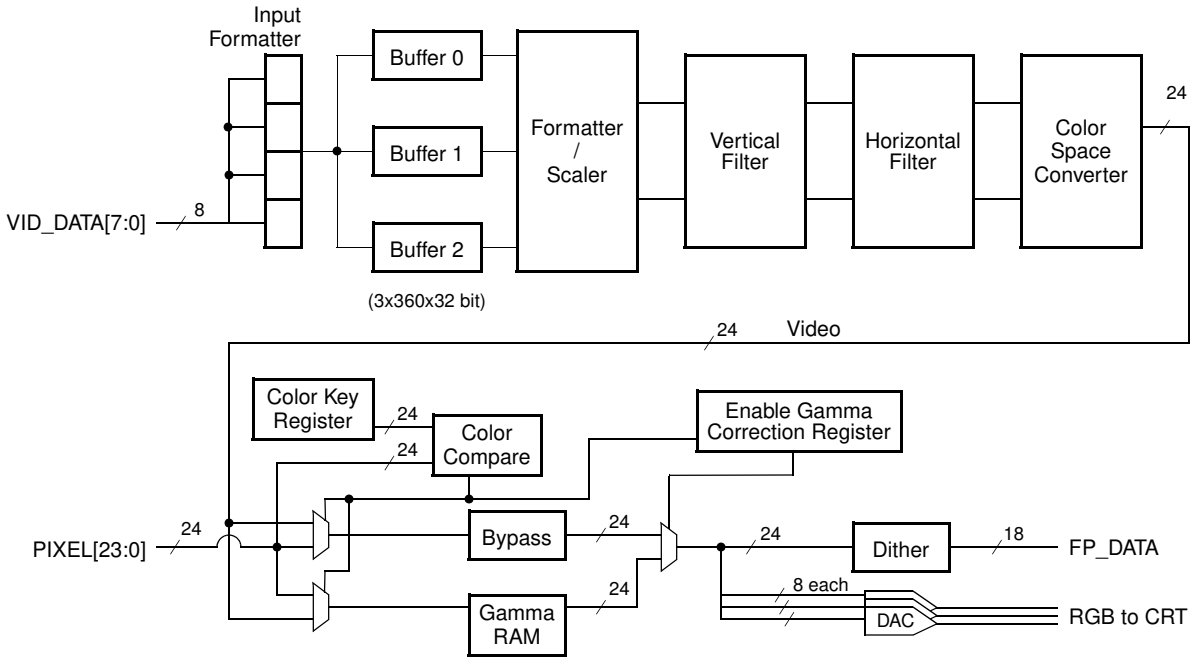


Figure 4-23. 8-Bit Display Subsystem Extensions

4.8.2 Video Accelerator

The CS5530A off-loads the processor from several computing-intensive tasks related to the playback of full motion video. By incorporating this level of hardware-assist, a CS5530A/GX1 processor based system can sustain 30 frames-per-second of MPEG quality video.

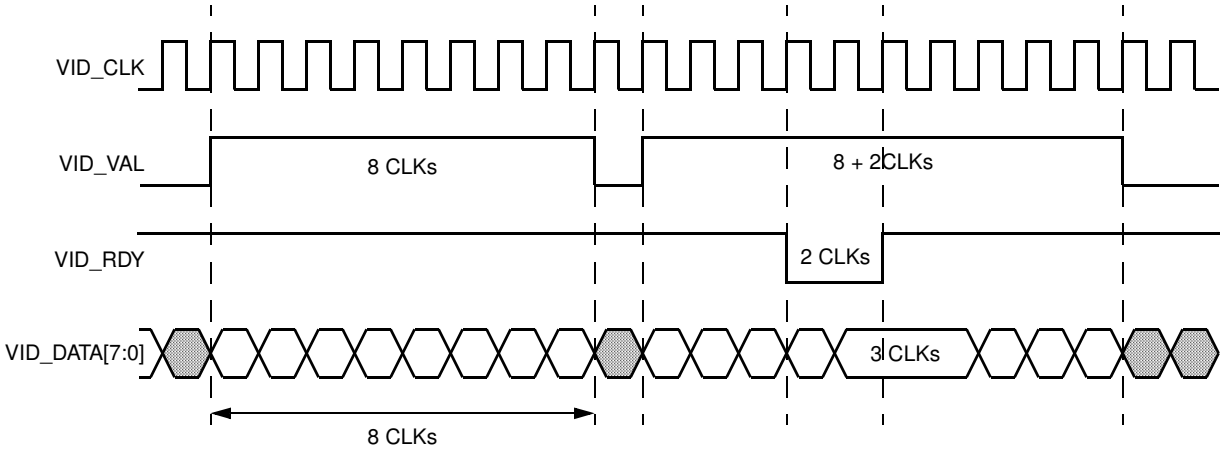
4.8.2.1 Line Buffers

The CS5530A accepts an 8-bit video stream from the processor and provides three full MPEG resolution line buffers (3x360x32-bit). MPEG source horizontal resolutions up to 720 pixels are supported. By having three line buffers, the display pipeline can read from two lines while the next line of data is being loaded from the processor. This minimizes memory bandwidth utilization by requiring that a source line be transferred only once per frame. Peak bandwidth is also reduced by requiring that the video source line be transferred within the horizontal line time rather than forcing the transfer to occur during the active video window. This efficient utilization of memory bandwidth allows the processor and graphics accelerator an increased opportunity to access the memory subsystem and improves overall system performance during video playback.

4.8.2.2 Video Port Protocol

The video port operates at one-half the processor's core clock rate and utilizes a two-wire handshake protocol. The VID_VAL input signal indicates that valid data has been placed on the VID_DATA[7:0] bus. When the CS5530A is ready to accept data, it asserts VID_RDY to indicate that a line buffer is free to accept the next line. When both VID_VAL and VID_RDY are asserted, VID_DATA advances.

The VID_RDY signal is driven by the CS5530A one clock early to the processor while the VID_VAL signal is driven by the processor coincident with valid data on VID_DATA. A sample timing diagram is shown in Figure 4-24.



Note: VID_CLK = CORE_CLK/2

Figure 4-24. Video Port Protocol

4.8.2.3 Video Format

The video input data can be in interleaved YUV 4:2:2 or RGB 5:6:5 format. The sequence of the individual YUV components is selectable to one of four formats via bits [3:2] in the Video Configuration Register (F4BAR+Memory Offset 00h[3:2]). The decode for these bits is shown in Table 4-72.

Table 4-72. Video Input Format Bits

Bit	Description
F4BAR+Memory Offset 00h-03h	**Video Configuration Register (R/W)**	**Reset Value = 00000000h**
31	**Reserved:** Set to 0
30	**High Speed Timing for Video Interface:** High speed timings for the video interface. 0 = Disable; 1= Enable. If bit 30 is enabled, bit 25 should be set to 0.
29	**16-bit Video Interface:** Allow video interface to be 16 bits. 0 = Disable; 1= Enable. If bit 29 is enabled, 8 bits of pixel data is used for video. The 24-bit pixel data is then dithered to 16 bits. **Note:** F4BAR+Memory Offset 04h[25] should be set to the same value as this bit (bit 29).
28	**YUV 4:2:2 or 4:2:0 Mode:** 0 = 4:2:2 mode; 1= 4:2:0 mode. If 4:2:0 mode is selected, bits [3:2] should be set to 01 for 8-bit video mode and 10 for 16-bit video mode. **Note:** The GX1 processor does not support 4:2:0 mode.
27	**Video Line Size (DWORDs):** This is the MSB of the Video Line Size (DWORDs). See bits [15:8] for description.
26	**Reserved:** Set to 0
25	**Early Video Ready:** Generate VID_RDY output signal one-half VID_CLK period early to improve the speed of the video port operation. 0 = Disable; 1 = Enable. If bit 30 is enabled, this bit (bit 25) should be set to 0.
24	**Initial Buffer Read Address:** This is the MSB of the Initial Buffer Read Address. See bits [23:16] for description.
23:16	**Initial Buffer Read Address:** This field is used to preload the starting read address for the line buffers at the beginning of each display line. It is used for hardware clipping of the video window at the left edge of the active display. It represents the DWORD address of the source pixel which is to be displayed first. For an unclipped window, this value should be 0.
15:8	**Video Line Size (DWORDs):** This field represents the horizontal size of the source video data in DWORDs.
7	**Y Filter Enable:** Vertical filter. 0 = Disable; 1= Enable.
6	**X Filter Enable:** Horizontal filter. 0 = Disable; 1 = Enable.
5	**CSC Bypass:** Allows color-space-converter to be bypassed. Primarily used for displaying an RGB graphics overlay rather than a YUV video overlay. 0 = Overlay data passes through CSC; 1 = Overlay data bypasses CSC.
4	**GV Select:** Selects whether graphics or video data will be passed through the scaler hardware. 0 = Video data; 1 = Graphics data.
3:2	**Video Input Format:** This field defines the byte ordering of the video data on the VID_DATA bus. **8-Bit Mode (Value Byte Order [0:3])** — **16-Bit Mode (Value Byte Order [0:3])** 00 = U Y0 V Y1 (also used for RGB 5:6:5 input) — 00 = U Y0 V Y1 (also used for RGB 5:6:5 input) 01 = Y1 V Y0 U or 4:2:0 — 01 = Y0 U Y1 V 10 = Y0 U Y1 V — 10 = Y1 V Y0 U or 4:2:0 11 = Y0 V Y1 U — 11 = Reserved If bit 28 is set for 4:2:0 mode, these bits (bits [3:2]) should be set to 01 for 8-bit video mode and 10 for 16-bit video mode. **Note:** U = Cb, V = Cr
1	**Video Register Update:** Allow video position and scale registers to be updated simultaneously on next occurrence of vertical sync. 0 = Disable; 1 = Enable.
0	**Video Enable:** Video acceleration hardware. 0 = Disable; 1 = Enable.

4.8.2.4 X and Y Scaler / Filter

The CS5530A supports horizontal and vertical scaling of the video stream up to eight times the source resolution. The scaler uses a Digital-Differential-Analyzer (DDA) based upon the values programmed in the Video Scale Register (F4BAR+Memory Offset 10h, see Table 4-73)

The scaled video stream is then passed through horizontal and vertical filters which perform a 2-tap, 8-phase bilinear filter on the resulting stream. The filtering function removes the “blockiness” of the scaled video thereby significantly improving the quality of the displayed image.

By performing the scaling and filtering function in hardware, video performance is substantially improved over pure software implementations by requiring that the decompression software only output the video stream at the native source resolution. This saves both processor overhead and memory bandwidth.

4.8.2.5 Color-Space-Converter

After scaling and filtering have been applied, the YUV video data is passed through the color-space converter to obtain 24-bit RGB video data. The color-space conversion equations are based on the CCIR Recommendation 601-1 as follows:

R = 1.164(Y–16) + 1.596(V–128)
G = 1.164(Y–16) – 0.813(V–128) – 0.391(U–128)
B = 1.164(Y–16) + 2.018(U–128)

The color-space converter clamps inputs to acceptable limits if the data is not well behaved. The color-space converter is bypassed for overlaying 16 bpp RGB graphics data.

Table 4-73. Video Scale Register

Bit	Description
F4BAR+Memory Offset 10h-13h	**Video Scale Register (R/W)** **Reset Value = xxxxxxxxh**
31:30	**Reserved:** Set to 0.
29:16	**Video Y Scale Factor:** This field represents the video window vertical scale factor according to the following formula. VID_Y_SCL = 8192 * (Ys - 1) / (Yd - 1) Where: Ys = Video source vertical size in lines Yd = Video destination vertical size in lines
15:14	**Reserved:** Set to 0.
13:0	**Video X Scale Factor:** This field represents the video window horizontal scale factor according to the following formula. VID_X_SCL = 8192 * (Xs - 1) / (Xd - 1) Where: Xs = Video source horizontal size in pixels Xd = Video destination horizontal size in pixels

4.8.3 Video Overlay

The video data from the color-space converter is then mixed with the graphics data based upon the video window position. The video window position is programmable via the Video X and Y Position Registers (F4BAR+Memory Offset 08h and 0Ch). A color-keying mechanism is employed to compare either the source (video) or destination (graphics) color to the color key programmed via the Video Color Key Register (FBAR+Offset 14h) and to select the appropriate pixel for display within the video window. The range of the color key is programmable by setting the appropriate bits in the Video Color Mask Register (F4BAR+Memory Offset 18h). This mechanism greatly reduces the software overhead for computing visible pixels, and ensures that the video display window may be partially occluded by overlapping graphics data. Tables 4-74 and 4-75 show the bit formats for these registers

The CS5530A accepts graphics data over the PIXEL[23:0] interface from the GX1 processor at the screen DOT clock rate. The CS5530A is capable of displaying graphics resolutions up to 1600x1200 at color depths up to 24 bits per pixel (bpp) while simultaneously overlaying a video window. However, system maximum resolution is not determined by the CS5530A since it is not the source of the graphics data and timings.

Table 4-74. Video X and Y Position Registers

Bit	Description
F4BAR+Memory Offset 08h-0Bh	**Video X Register (R/W)** — **Reset Value = xxxxxxxxh**
31:27	**Reserved:** Set to 0.
26:16	**Video X End Position:** This field represents the horizontal end position of the video window according to the following formula. Position programmed = screen position + (H_TOTAL – H_SYNC_END) – 13.
15:11	**Reserved:** Set to 0.
10:0	**Video X Start Position:** This field represents the horizontal start position of the video window according to the following formula. Position programmed = screen position + (H_TOTAL – H_SYNC_END) – 13.
F4BAR+Memory Offset 0Ch-0Fh	**Video Y Register (R/W)** — **Reset Value = xxxxxxxxh**
31:27	**Reserved:** Set to 0.
26:16	**Video Y End Position:** This field represents the vertical end position of the video window according to the following formula. Position programmed = screen position + (V_TOTAL – V_SYNC_END) + 1.
15:11	**Reserved:** Set to 0.
10:0	**Video Y Start Position:** This field represents the vertical start position of the video window according to the following formula. Position programmed = screen position + (V_TOTAL – V_SYNC_END) + 1.

Table 4-75. Video Color Registers

Bit	Description
F4BAR+Memory Offset 14h-17h	**Video Color Key Register (R/W)** — **Reset Value = xxxxxxxxh**
31:24	**Reserved:** Set to 0.
23:0	**Video Color Key:** This field represents the video color key. It is a 24-bit RGB value. The graphics or video data being compared may be masked prior to the compare by programming the Video Color Mask Register (F4BAR+Memory Offset 18h) appropriately.
F4BAR+Memory Offset 18h-1Bh	**Video Color Mask Register (R/W)** — **Reset Value = xxxxxxxxh**
31:24	**Reserved:** Set to 0.
23:0	**Video Color Mask:** This field represents the video color mask. It is a 24-bit RGB value. Zeroes in the mask cause the corresponding bits in the graphics or video stream being compared to be ignored.

4.8.4 Gamma RAM

Either the graphics or video stream may be routed through an on-chip gamma RAM (3x256x8-bit) which can be used for gamma-correction of either data stream, or contrast/ brightness adjustments in the case of video data.

A bypass path is provided for either the graphics or video stream (depending on which is sent through the gamma RAM). The two streams are merged based on the results of the color key compare.

Configuration for this feature and the display interface are through the Display Configuration Register (F4BAR+Memory Offset 04h). Table 4-76 shows the bit formats for this register.

Table 4-76. Display Configuration Register

Bit	Description
F4BAR+Memory Offset 04h-07h	**Display Configuration Register (R/W)**	**Reset Value = 00000000h**
31	**DDC Input Data (Read Only):** This is the DDC input data bit for reads.
30:28	**Reserved:** Set to 0.
27	**Flat Panel On (Read Only):** This bit indicates whether the attached flat panel display is powered on or off. The bit transitions at the end of the power-up or power-down sequence. 0 = Off; 1 = On.
26	**Reserved:** Set to 0.
25	**16-Bit Graphics Enable:** This bit works in conjunction with the 16-bit Video Interface bit at F4BAR+Memory Offset 00h[29]. This bit should be set to the same value as the 16-bit Video Interface bit.
24	**DDC Output Enable:** This bit enables the DDC_SDA line to be driven for write data. 0 = DDC_SDA (pin M4) is an input; 1 = DDC_SDA (pin M4) is an output.
23	**DDC Output Data:** This is the DDC data bit.
22	**DDC Clock:** This is the DDC clock bit. It is used to clock the DDC_SDA bit.
21	**Palette Bypass:** Selects whether graphics or video data should bypass the gamma RAM. 0 = Video data; 1 = Graphics data.
20	**Video/Graphics Color Key Select:** Selects whether the video or graphics data stream will be used for color/chroma keying. 0 = Graphics data is compared to color key; 1 = Video data is compared to color key.
19:17	**Power Sequence Delay:** This field selects the number of frame periods that transpire between successive transitions of the power sequence control lines. Valid values are 001 to 111.
16:14	**CRT Sync Skew:** This 3-bit field represents the number of pixel clocks to skew the horizontal and vertical syncs that are sent to the CRT. This field should be programmed to 100 as the baseline. The syncs may be moved forward or backward relative to the pixel data via this register. It is used to compensate for the pipeline delay through the graphics pipeline.
13	**Flat Panel Dither Enable:** This bit enables flat panel dithering. It enables 24 bpp display data to be approximated with an 18-bit flat panel display. 0 = Disable; 1 = Enable.
12	**XGA Flat Panel:** This bit enables the FP_CLK_ EVEN output signal which can be used to demultiplex the FP_DATA bus into even and odd pixels. 0 = Standard flat panel; 1 = XGA flat panel.
11	**Flat Panel Vertical Synchronization Polarity:** Selects the flat panel vertical sync polarity. 0 = FP vertical sync is normally low, transitioning high during sync interval. 1 = FP vertical sync is normally high, transitioning low during sync interval.
10	**Flat Panel Horizontal Synchronization Polarity:** Selects the flat panel horizontal sync polarity. 0 = FP horizontal sync is normally low, transitioning high during sync interval. 1 = FP horizontal sync is normally high, transitioning low during sync interval.
9	**CRT Vertical Synchronization Polarity:** Selects the CRT vertical sync polarity. 0 = CRT vertical sync is normally low, transitioning high during sync interval. 1 = CRT vertical sync is normally high, transitioning low during sync interval.
8	**CRT Horizontal Synchronization Polarity:** Selects the CRT horizontal sync polarity. 0 = CRT horizontal sync is normally low, transitioning high during sync interval. 1 = CRT horizontal sync is normally high, transitioning low during sync interval.
7	**Flat Panel Data Enable:** Enables the flat panel data bus. 0 = FP_DATA [17:0] is forced low; 1 = FP_DATA [17:0] is driven based upon power sequence control.
6	**Flat Panel Power Enable:** The transition of this bit initiates a flat panel power-up or power-down sequence. 0 -> 1 = Power-up flat panel; 1 -> 0 = Power-down flat panel.
5	**DAC Power-Down (active low):** This bit must be set to power-up the video DACs. It can be cleared to power-down the video DACs when not in use. 0 = DACs are powered down; 1 = DACs are powered up.
4	**Reserved:** Set to 0.

Table 4-76. Display Configuration Register (Continued)

Bit	Description
3	**DAC Blank Enable:** This bit enables the blank to the video DACs. 0 = DACs are constantly blanked; 1 = DACs are blanked normally.
2	**CRT Vertical Sync Enable:** Enables the CRT vertical sync. Used for VESA DPMS support. 0 = Disable; 1 = Enable.
1	**CRT Horizontal Sync Enable:** Enables the CRT horizontal sync. Used for VESA DPMS support. 0 = Disable; 1 = Enable.
0	**Display Enable:** Enables the graphics display pipeline. It is used as a reset for the display control logic. 0 = Reset display control logic; 1 = Enable display control logic.

4.8.5 Display Interface

The CS5530A interfaces directly to a variety of display devices including conventional analog CRT displays, TFT flat panels, or optionally to digital NTSC/PAL encoder devices.

4.8.5.1 Video DACs

The CS5530A incorporates three 8-bit video Digital-to-Analog Converters (DACs) for interfacing directly to CRT displays. The video DACs meet the VESA specification and are capable of operation up to 157.5 MHz for supporting up to 1280x1024 display at a 85 Hz refresh rate and are VESA compliant.

4.8.5.2 VESA DDC2B / DPMS

The CS5530A supports the VESA DDC2B and DPMS standards for enhanced monitor communications and power management support.

4.8.5.3 Flat Panel Support

The CS5530A also interfaces directly to industry standard 18-bit Active Matrix Thin-Film-Transistor (TFT) flat panels. The CS5530A includes 24-bit to 18-bit dithering logic to increase the apparent number of colors displayed on 18-bit flat panels.

In addition, the CS5530A incorporates power sequencing logic to simplify the design of a portable system.

If flat panel support is not required, the flat panel output port may be used to supply digital video data to one of several types of NTSC/PAL encoder devices on the market.

Flat Panel Power-Up/Down Sequence

When the Flat Panel Power Enable bit (F4BAR+Memory Offset 04h[6]) transitions from a 0 to 1, the FP_ENA_VDD signal is enabled. This is followed by the data bus (including syncs and ENA_DISP). Finally, FP_ENA_BKL is enabled. The time between each of these successive stages is set by the value of the Power Sequence Delay bits (F4BAR+Memory Offset 04h[19:17]). The value in these bits refer to the number of graphics frames that will elapse between each successive enabling of the TFT signals. For example, if the Power Sequence Delay is set to 3h (011b), then three frame times will elapse between the time when FP_ENA_VDD is transitioned and the data bus is transitioned. Likewise, three frame times will elapse between the data bus getting enabled and the FP_ENA_BKL is transitioned. If the panel is being refreshed at 100 Hz, each frame lasts 1 ms. So, if the Power Sequence Delay is set to 3, 3 ms will elapse between transitions. When powering off the panel, the signals are transitioned in the opposite order (FP_ENA_BKL, data bus, FP_ENA_VDD) using the same Power Sequence Delay in the power-down sequence.

4.9 Universal Serial Bus Support

The CS5530A integrates a Universal Serial Bus (USB) controller which supports two ports. The USB controller is OpenHCI compliant, a standard developed by Compaq, Microsoft, and National Semiconductor. The USB core consists of three main interface blocks: the USB PCI interface controller, the USB host controller, and the USB interface controller. Legacy keyboard and mouse controllers are also supported for DOS compatibility with those USB devices.

This document must be used along with the following public domain reference documents for a complete functional description of the USB controller:

- USB Specification Revision 1.0
- OpenHCI Specification, Revision 1.0
- PCI Specification, Version 2.1

4.9.1 USB PCI Controller

The PCI controller interfaces the host controller to the PCI bus. As a master, the PCI controller is responsible for running cycles on the PCI bus on behalf of the host controller. As a target, the PCI controller monitors the cycles on the PCI bus and determines when to respond to these cycles. The USB core is a PCI target when it decodes cycles to its internal PCI configuration registers or to its internal PCI memory mapped I/O registers.

The USB core is implemented as a unique PCI device in the CS5530A. It has its own PCI Header and Configuration space. It is a single-function device, containing only Function #0. Depending on the state of the HOLD_REQ# strap pin at reset, its PCI Device Number for Configuration accesses varies:

If HOLD_REQ# is low, it uses pin AD29 as its IDSEL input, appearing as Device #13h in a Geode system.

If HOLD_REQ# is high, it uses pin AD27 as its IDSEL input, appearing as Device #11h in a Geode system.

The USB core is also affected by some bits in registers belonging to the other (Chipset) device of the CS5530A. In particular, the USB device can be disabled through the Chipset device, F0 Index 43h[0], and its IDSEL can be remapped by changing F0 Index 44h[6] (though this also affects the Chipset device's IDSEL and is not recommended).

All registers can be accessed via 8-, 16-, or 32-bit cycles (i.e., each byte is individually selected by the byte enables). Registers marked as Reserved, and reserved bits within a register are not implemented and should not be modified. These registers are summarized in Table 4-77. For complete bit information, see Table 5-25 "USB Index xxh: USB PCI Configuration Registers" on page 205.

Table 4-77. USB PCI Configuration Registers

USB Index	Type	Name
00h-01h	RO	Vendor Identification
02h-03h	RO	Device Identification
04h-05h	R/W	Command Register
06h-07h	R/W	Status Register
08h	RO	Device Revision ID
09h-0Bh	RO	Class Code
0Ch	R/W	Cache Line Size
0Dh	R/W	Latency Timer
0Eh	RO	Header Type
0Fh	RO	BIST Register
10h-13h	R/W	**Base Address Register (USB BAR):** Sets the base address of the memory mapped USB controller registers.
14h-3Bh	--	Reserved
3Ch	R/W	Interrupt Line Register
3Dh	RO	Interrupt Pin Register
3Eh	RO	Min. Grant Register
3Fh	RO	Max. Latency Register
40h-43h	R/W	ASIC Test Mode Enable Register
44h-45h	R/W	ASIC Operational Mode Enable
46h-47h	--	Reserved
48h-FFh	--	Reserved

4.9.2 USB Host Controller

In the USB core is the operational control block. It is responsible for the host controller's operational states (Suspend, Disable, Enable), special USB signals (Reset, Resume), status, interrupt control, and host controller configuration.

The host controller interface registers are memory mapped registers, mapped by USB F0 Index 10h (Base Address Register). These memory mapped registers are summarized in Table 4-78. For bit definitions, refer to Table 5-26 "USB BAR+Memory Offset xxh: USB Controller Registers" on page 208.

4.9.3 USB Power Management

At this time, USB supports minimal system level power management features. The only power management feature implemented is the disabling of the USB clock generator in USB Suspend state. Additional power management features require slight modifications.

The design supports PCICLK frequencies from 0 to 33 MHz. Synchronization between the PCI and USB clock domains is frequency independent. Remote wakeup of USB is asynchronously implemented from the USB Ports to PCI INTA#.

The design needs USBCLK to be operational at all times. If it is necessary to stop the 48 MHz clock, the system design requires that the signal used to enable/disable the USB clock generators is also used to wake the 48 MHz clock source. Currently, the RemoteWakeupConnected and RemoteWakeupEnable bits in the HcControl register are not implemented.

Table 4-78. USB Controller Registers

USB BAR+ Memory Offset	Type	Name
00h-03h	R/W	HcRevision
04h-07h	R/W	HcControl
08h-0Bh	R/W	HcCommandStatus
0Ch-0Fh	R/W	HcInterruptStatus
10h-13h	R/W	HcInterruptEnable
14h-17h	R/W	HcInterruptDisable
18h-1Bh	R/W	HcHCCA
1Ch-1Fh	R/W	HcPeriodCurrentED
20h-23h	R/W	HcControlHeadED
24h-27h	R/W	HcControlCurrentED
28h-2Bh	R/W	HcBulkHeadED
2Ch-2Fh	R/W	HcBulkCurrentED
30h-33h	R/W	HcDoneHead
34h-37h	R/W	HcFmInterval
38h-3Bh	RO	HcFrameRemaining
3Ch-3Fh	RO	HcFmNumber
40h-43h	R/W	HcPeriodicStart
44h-47h	R/W	HcLSThreshold
48h-4Bh	R/W	HcRhDescriptorA
4Ch-4Fh	R/W	HcRhDescriptorB
50h-53h	R/W	HcRhStatus
54h-57h	R/W	HcRhPortStatus[1]
58h-5Bh	R/W	HcRhPortStatus[2]
5Ch-5Fh	--	Reserved
60h-9Fh	--	Reserved
100h-103h	R/W	HceControl
104h-107h	R/W	HceInput
108h-10Dh	R/W	HceOutput
10Ch-10Fh	R/W	HceStatus

5 Register Descriptions

The Geode CS5530A is a multi-function device. Its register space can be broadly divided into four categories in which specific types of registers are located:

1) Chipset Register Space (F0-F4)
2) USB Controller Register Space (PCIUSB)
3) ISA Legacy I/O Register Space (I/O Port)
4) V-ACPI I/O Register Space (I/O Port)

The Chipset and the USB Controller Register Spaces are accessed through the PCI interface using the PCI Type One Configuration Mechanism.

The **Chipset Register Space** of the CS5530A is comprised of five separate functions (F0-F4) each with its own register space consisting of PCI header registers and memory or I/O mapped registers.

F0: Bridge Configuration Registers
F1: SMI Status and ACPI Timer Registers
F2: IDE Controller Registers
F3: XpressAUDIO™ Subsystem Registers
F4: Video Controller Registers

The PCI header is a 256-byte region used for configuring a PCI device or function. The first 64 bytes are the same for all PCI devices and are predefined by the PCI specification. These registers are used to configure the PCI for the device. The rest of the 256-byte region is used to configure the device or function itself.

The **USB Controller Register Space** consists of the standard PCI header registers. The USB controller supports two ports and is OpenHCI-compliant.

The **ISA Legacy I/O Register Space** contains all the legacy compatibility I/O ports that are internal, trapped, shadowed, or snooped.

The **V-ACPI I/O Register Space** contains two types of registers: Fixed Feature and General Purpose. These registers are emulated by the SMI handling code rather than existing in physical hardware. To the ACPI-compliant operating system, the SMI-base virtualization is transparent. An ACPI compliant system is one whose underlying BIOS, device drivers, chipset and peripherals conform to revision 1.0 or newer of the Advanced Control and Power Interface specification.

The CS5530A V-ACPI (Virtual ACPI) solution provides the following support:

- CPU States — C1, C2
- Sleep States — S1, S2, S4, S4BIOS, S5
- Embedded Controller (Optional) — SCI and SWI event inputs
- General Purpose Events — Fully programmable GPE0 Event Block registers

The remaining subsections of this chapter are as follows:

- A brief discussion on how to access the registers located in the PCI Configuration Space
- Register summary
- Detailed bit formats of all registers

5.1 PCI Configuration Space and Access Methods

Configuration cycles are generated in the processor. All configuration registers in the CS5530A are accessed through the PCI interface using the PCI Type One Configuration Mechanism. This mechanism uses two DWORD I/O locations at 0CF8h and 0CFCh. The first location (0CF8h) references the Configuration Address Register. The second location (0CFCh) references the Configuration Data Register.

To access PCI configuration space, write the Configuration Address (0CF8h) Register with data that specifies the CS5530A as the device on PCI being accessed, along with the configuration register offset. On the following cycle, a read or write to the Configuration Data Register (CDR) causes a PCI configuration cycle to the CS5530A. BYTE, WORD, or DWORD accesses are allowed to the CDR at 0CFCh, 0CFDh, 0CFEh, or 0CFFh.

The CS5530A has six configuration register sets, one for each function (F0-F4) and USB (PCIUSB). Base Address Registers (BARs) in the PCI header registers are pointers for additional I/O or memory mapped configuration registers.

Table 4-1 shows the PCI Configuration Address Register (0CF8h) and how to access the PCI header registers.

Table 5-1. PCI Configuration Address Register (0CF8h)

31	30 24	23 16	15 11	10 8	7 2	1 0
Configuration Space Mapping	**RSVD**	**Bus Number**	**Device Number**	**Function**	**Index**	**DWORD 00**
1 (Enable)	000 0000	0000 0000	xxxx x **(Note)**	xxx	xxxx xx	00 (Always)
Function 0 (F0): Bridge Configuration Register Space						
80h		0000 0000	1001 0 or 1000 0	000	Index	
Function 1 (F1): SMI Status and ACPI Timer Register Space						
80h		0000 0000	1001 0 or 1000 0	001	Index	
Function 2 (F2): IDE Controller Register Space						
80h		0000 0000	1001 0 or 1000 0	010	Index	
Function 3 (F3): XpressAUDIO™ Subsystem Register Space						
80h		0000 0000	1001 0 or 1000 0	011	Index	
Function 4 (F4): Video Controller Register Space						
80h		0000 0000	1001 0 or 1000 0	100	Index	
PCIUSB: USB Controller Register Space						
80h		0000 0000	1001 1 or 1000 1	000	Index	

Note: The device number depends upon the strapping of pin H26 (HOLD_REQ#) during POR.
Strap pin H26 low: IDSEL = AD28 for Chipset Register Space and AD29 for USB Register Space
Strap pin H26 high: IDSEL = AD26 for Chipset Register Space and AD27 for USB Register Space

The strapping of pin H26 can be read back in F0 Index 44h[6].

5.2 Register Summary

The tables in this subsection summarize all the registers of the CS5530A. Included in the tables are the register's reset values and page references where the bit formats are found.

Table 5-2. Function 0: PCI Header and Bridge Configuration Registers Summary

F0 Index	Width (Bits)	Type	Name	Reset Value	Reference (Table 5-15)
00h-01h	16	RO	Vendor Identification Register	1078h	Page 155
02h-03h	16	RO	Device Identification Register	0100h	Page 155
04h-05h	16	R/W	PCI Command Register	000Fh	Page 155
06h-07h	16	R/W	PCI Status Register	0280h	Page 155
08h	8	RO	Device Revision ID Register	xxh	Page 156
09h-0Bh	24	RO	PCI Class Code Register	060100h	Page 156
0Ch	8	R/W	PCI Cache Line Size Register	00h	Page 156
0Dh	8	R/W	PCI Latency Timer Register	00h	Page 156
0Eh	8	RO	PCI Header Type Register	80h	Page 156
0Fh	8	RO	PCI BIST Register	00h	Page 156
10h-1Fh	--	--	Reserved	xxh	Page 156
20h-3Fh	--	--	Reserved	00h	Page 156
40h	8	R/W	PCI Function Control Register 1	89h	Page 156
41h	8	R/W	PCI Function Control Register 2	10h	Page 157
42h	8	R/W	PCI Function Control Register 3	ACh	Page 157
43h	8	R/W	USB Shadow Register	03h	Page 157
44h	8	R/W	Reset Control Register	01h	Page 158
45h-4Fh	--	--	Reserved	00h	Page 158
50h	8	R/W	PIT Control/ISA CLK Divider	7Bh	Page 158
51h	8	R/W	ISA I/O Recovery Control Register	40h	Page 159
52h	8	R/W	ROM/AT Logic Control Register	F8h	Page 159
53h	8	R/W	Alternate CPU Support Register	00h	Page 159
54h-59h	--	--	Reserved	xxh	Page 160
5Ah	8	R/W	Decode Control Register 1	03h	Page 160
5Bh	8	R/W	Decode Control Register 2	20h	Page 160
5Ch	8	R/W	PCI Interrupt Steering Register 1	00h	Page 160
5Dh	8	R/W	PCI Interrupt Steering Register 2	00h	Page 161
5Eh-6Fh	--	--	Reserved	xxh	Page 161
70h-71h	16	R/W	General Purpose Chip Select Base Address Register	0000h	Page 161
72h	8	R/W	General Purpose Chip Select Control Register	00h	Page 161
73h-7Fh	--	--	Reserved	xxh	Page 161
80h	8	R/W	Power Management Enable Register 1	00h	Page 161
81h	8	R/W	Power Management Enable Register 2	00h	Page 162
82h	8	R/W	Power Management Enable Register 3	00h	Page 163
83h	8	R/W	Power Management Enable Register 4	00h	Page 164
84h	8	RO	Second Level Power Management Status Mirror Register 1	00h	Page 165
85h	8	RO	Second Level Power Management Status Mirror Register 2	00h	Page 165
86h	8	RO	Second Level Power Management Status Mirror Register 3	00h	Page 166
87h	8	RO	Second Level Power Management Status Mirror Register 4	00h	Page 166
88h	8	R/W	General Purpose Timer 1 Count Register	00h	Page 167
89h	8	R/W	General Purpose Timer 1 Control Register	00h	Page 167
8Ah	8	R/W	General Purpose Timer 2 Count Register	00h	Page 168
8Bh	8	R/W	General Purpose Timer 2 Control Register	00h	Page 168
8Ch	8	R/W	IRQ Speedup Timer Count Register	00h	Page 168
8Dh	8	R/W	Video Speedup Timer Count Register	00h	Page 169
8Eh	8	R/W	VGA Timer Count Register	00h	Page 169

Table 5-2. Function 0: PCI Header and Bridge Configuration Registers Summary (Continued)

F0 Index	Width (Bits)	Type	Name	Reset Value	Reference (Table 5-15)
8Fh	--	--	Reserved	xxh	Page 169
90h	8	R/W	GPIO Pin Direction Register 1	00h	Page 169
91h	8	R/W	GPIO Pin Data Register 1	00h	Page 169
92h	8	R/W	GPIO Control Register 1	00h	Page 169
93h	8	R/W	Miscellaneous Device Control Register	00h	Page 170
94h	8	R/W	Suspend Modulation OFF Count Register	00h	Page 170
95h	8	R/W	Suspend Modulation ON Count Register	00h	Page 170
96h	8	R/W	Suspend Configuration Register	00h	Page 171
97h	8	R/W	GPIO Control Register 2	00h	Page 171
98h-99h	16	R/W	Primary Hard Disk Idle Timer Count Register	0000h	Page 172
9Ah-9Bh	16	R/W	Floppy Disk Idle Timer Count Register	0000h	Page 172
9Ch-9Dh	16	R/W	Parallel / Serial Idle Timer Count Register	0000h	Page 172
9Eh-9Fh	16	R/W	Keyboard / Mouse Idle Timer Count Register	0000h	Page 172
A0h-A1h	16	R/W	User Defined Device 1 Idle Timer Count Register	0000h	Page 172
A2h-A3h	16	R/W	User Defined Device 2 Idle Timer Count Register	0000h	Page 172
A4h-A5h	16	R/W	User Defined Device 3 Idle Timer Count Register	0000h	Page 173
A6h-A7h	16	R/W	Video Idle Timer Count Register	0000h	Page 173
A8h-A9h	16	R/W	Video Overflow Count Register	0000h	Page 173
AAh-ABh	--	--	Reserved	xxh	Page 173
ACh-ADh	16	R/W	Secondary Hard Disk Idle Timer Count Register	0000h	Page 173
AEh	8	WO	CPU Suspend Command Register	00h	Page 173
AFh	8	WO	Suspend Notebook Command Register	00h	Page 174
B0h-B3h	--	--	Reserved	xxh	Page 174
B4h	8	RO	Floppy Port 3F2h Shadow Register	xxh	Page 174
B5h	8	RO	Floppy Port 3F7h Shadow Register	xxh	Page 174
B6h	8	RO	Floppy Port 1F2h Shadow Register	xxh	Page 174
B7h	8	RO	Floppy Port 1F7h Shadow Register	xxh	Page 174
B8h	8	RO	DMA Shadow Register	xxh	Page 174
B9h	8	RO	PIC Shadow Register	xxh	Page 175
BAh	8	RO	PIT Shadow Register	xxh	Page 175
BBh	8	RO	RTC Index Shadow Register	xxh	Page 175
BCh	8	R/W	Clock Stop Control Register	00h	Page 175
BDh-BFh	--	--	Reserved	xxh	Page 176
C0h-C3h	32	R/W	User Defined Device 1 Base Address Register	00000000h	Page 176
C4h-C7h	32	R/W	User Defined Device 2 Base Address Register	00000000h	Page 176
C8h-CBh	32	R/W	User Defined Device 3 Base Address Register	00000000h	Page 176
CCh	8	R/W	User Defined Device 1 Control Register	00h	Page 176
CDh	8	R/W	User Defined Device 2 Control Register	00h	Page 176
CEh	8	R/W	User Defined Device 3 Control Register	00h	Page 176
CFh	--	--	Reserved	xxh	Page 177
D0h	8	WO	Software SMI Register	00h	Page 177
D1h-EBh	--	--	Reserved	xxh	Page 177
ECh	8	R/W	Timer Test Register	00h	Page 177
EDh-F3h	--	--	Reserved	xxh	Page 177
F4h	8	RC	Second Level Power Management Status Register 1	00h	Page 177
F5h	8	RC	Second Level Power Management Status Register 2	00h	Page 177
F6h	8	RC	Second Level Power Management Status Register 3	00h	Page 178
F7h	8	RO/RC	Second Level Power Management Status Register 4	00h	Page 179
F8h-FFh	--	--	Reserved	xxh	Page 179

Table 5-3. Function 1: PCI Header Registers for SMI Status and ACPI Timer Summary

F1 Index	Width (Bits)	Type	Name	Reset Value	Reference (Table 5-16)
00h-01h	16	RO	Vendor Identification Register	1078h	Page 180
02h-03h	16	RO	Device Identification Register	0101h	Page 180
04h-05h	16	R/W	PCI Command Register	0000h	Page 180
06h-07h	16	RO	PCI Status Register	0280h	Page 180
08h	8	RO	Device Revision ID Register	00h	Page 180
09h-0Bh	24	RO	PCI Class Code Register	068000h	Page 180
0Ch	8	RO	PCI Cache Line Size Register	00h	Page 180
0Dh	8	RO	PCI Latency Timer Register	00h	Page 180
0Eh	8	RO	PCI Header Type Register	00h	Page 180
0Fh	8	RO	PCI BIST Register	00h	Page 180
10h-13h	32	R/W	**Base Address Register (F1BAR):** Sets base address for memory mapped SMI status and ACPI timer support registers (summarized in Table 4-4).	00000000h	Page 180
14h-3Fh	--	--	Reserved	00h	Page 180
40h-FFh			Reserved	xxh	Page 180

Table 5-4. F1BAR: SMI Status and ACPI Timer Registers Summary

F1BAR+ Memory Offset	Width (Bits)	Type	Name	Reset Value	Reference (Table 5-17)
00h-01h	16	RO	Top SMI Status Mirror Register	0000h	Page 181
02h-03h	16	RC	Top SMI Status Register	0000h	Page 181
04h-05h	16	RO	Second Level General Traps & Timers Status Mirror	0000h	Page 182
06h-07h	16	RC	Second Level General Traps & Timers Status Register	0000h	Page 182
08h-09h	16	Read to Enable	SMI Speedup Disable Register	0000h	Page 183
0Ah-1Bh	--	--	Reserved	xxh	Page 183
1Ch-1Fh	32	RO	ACPI Timer Count **Note:** The ACPI Timer Count Register is accessible through I/O Port 121Ch.	00FFFFFCh	Page 183
20h-4Fh	--	--	Reserved	xxh	Page 183
50h-FFh	**Note:** The registers located at F1BAR+Memory Offset 50h-FFh can also be accessed at F0 Index 50h-FFh. The preferred method is to program these registers through the F0 Register Space. Refer to Table 5-2 "Function 0: PCI Header and Bridge Configuration Registers Summary" on page 145 for summary information.				

Table 5-5. Function 2: PCI Header Registers for IDE Controller Summary

F2 Index	Width (Bits)	Type	Name	Reset Value	Reference (Table 5-18)
00h-01h	16	RO	Vendor Identification Register	1078h	Page 184
02h-03h	16	RO	Device Identification Register	0102h	Page 184
04h-05h	16	R/W	PCI Command Register	0000h	Page 184
06h-07h	16	RO	PCI Status Register	0280h	Page 184
08h	8	RO	Device Revision ID Register	00h	Page 184
09h-0Bh	24	RO	PCI Class Code Register	010180h	Page 184
0Ch	8	RO	PCI Cache Line Size Register	00h	Page 184
0Dh	8	RO	PCI Latency Timer Register	00h	Page 184
0Eh	8	RO	PCI Header Type Register	00h	Page 184
0Fh	8	RO	PCI BIST Register	00h	Page 184
10h-1Fh	--	--	Reserved	00h	Page 184
20h-23h	32	R/W	**Base Address Register (F2BAR):** Sets base address for I/O mapped IDE controller configuration registers (summarized in Table 4-6).	00000001h	Page 184
24h-3Fh	--	--	Reserved	00h	Page 184
40h-FFh	--	--	Reserved	xxh	Page 184

Table 5-6. F2BAR: IDE Controller Configuration Registers Summary

F2BAR+ I/O Offset	Width (Bits)	Type	Name	Reset Value	Reference (Table 5-19)
00h	8	R/W	IDE Bus Master 0 Command Register: Primary	00h	Page 185
01h	--	--	Reserved	xxh	Page 185
02h	8	R/W	IDE Bus Master 0 Status Register: Primary	00h	Page 185
03h	--	--	Reserved	xxh	Page 185
04h-07h	32	R/W	IDE Bus Master 0 PRD Table Address: Primary	00000000h	Page 185
08h	8	R/W	IDE Bus Master 1 Command Register: Secondary	00h	Page 185
09h	--	--	Reserved	xxh	Page 185
0Ah	8	R/W	IDE Bus Master 1 Status Register: Secondary	00h	Page 185
0Bh	--	--	Reserved	xxh	Page 186
0Ch-0Fh	32	R/W	IDE Bus Master 1 PRD Table Address: Secondary	00000000h	Page 186
10h-1Fh	--	--	Reserved	xxh	Page 186
20h-23h	32	R/W	Channel 0 Drive 0: PIO Register	0000E132h	Page 186
24h-27h	32	R/W	Channel 0 Drive 0: DMA Control Register	00077771h	Page 187
28h-2Bh	32	R/W	Channel 0 Drive 1: PIO Register	0000E132h	Page 187
2Ch-2Fh	32	R/W	Channel 0 Drive 1: DMA Control Register	00077771h	Page 187
30h-33h	32	R/W	Channel 1 Drive 0: PIO Register	0000E132h	Page 187
34h-37h	32	R/W	Channel 1 Drive 0: DMA Control Register	00077771h	Page 187
38h-3Bh	32	R/W	Channel 1 Drive 1: PIO Register	0000E132h	Page 187
3Ch-3Fh	32	R/W	Channel 1 Drive 1: DMA Control Register	00077771h	Page 187
40h-FFh	--	--	Reserved	xxh	Page 187

Table 5-7. Function 3: PCI Header Registers for XpressAUDIO™ Subsystem Summary

F3 Index	Width (Bits)	Type	Name	Reset Value	Reference (Table 5-20)
00h-01h	16	RO	Vendor Identification Register	1078h	Page 188
02h-03h	16	RO	Device Identification Register	0103h	Page 188
04h-05h	16	R/W	PCI Command Register	0000h	Page 188
06h-07h	16	RO	PCI Status Register	0280h	Page 188
08h	8	RO	Device Revision ID Register	00h	Page 188
09h-0Bh	24	RO	PCI Class Code Register	040100h	Page 188
0Ch	8	RO	PCI Cache Line Size Register	00h	Page 188
0Dh	8	RO	PCI Latency Timer Register	00h	Page 188
0Eh	8	RO	PCI Header Type Register	00h	Page 188
0Fh	8	RO	PCI BIST Register	00h	Page 188
10h-13h	32	R/W	**Base Address Register (F3BAR):** Sets base address for memory mapped XpressAUDIO™ subsystem configuration registers (summarized in Table 4-8).	00000000h	Page 188
14h-3Fh	--	--	Reserved	00h	Page 188
40h-FFh	--	--	Reserved	xxh	Page 188

Table 5-8. F3BAR: XpressAUDIO™ Subsystem Configuration Registers Summary

F3BAR+ Memory Offset	Width (Bits)	Type	Name	Reset Value	Reference (Table 5-21)
00h-03h	32	R/W	Codec GPIO Status Register	00100000h	Page 189
04h-07h	32	R/W	Codec GPIO Control Register	00000000h	Page 189
08h-0Bh	32	R/W	Codec Status Register	00000000h	Page 189
0Ch-0Fh	32	R/W	Codec Command Register	00000000h	Page 189
10h-11h	16	RO	Second Level Audio SMI Source Mirror Register	0000h	Page 189
12h-13h	16	RC	Second Level Audio SMI Source Register	0000h	Page 190
14h-17h	32	RO/RC	I/O Trap SMI and Fast Write Status Register	00000000h	Page 191
18h-19h	16	R/W	I/O Trap SMI Enable Register	0000h	Page 192
1Ah-1Bh	16	R/W	Internal IRQ Enable Register	0000h	Page 193
1Ch-1Dh	16	R/W	Internal IRQ Control Register	0000h	Page 193
1Eh-1Fh	16	WO	Internal IRQ Mask Register	xxxxh	Page 193
20h	8	R/W	Audio Bus Master 0 Command Register	00h	Page 194
21h	8	RC	Audio Bus Master 0 SMI Status Register	00h	Page 194
22h-23h	--	--	Reserved	xxh	Page 194
24h-27h	32	R/W	Audio Bus Master 0 PRD Table Address	00000000h	Page 194
28h	8	R/W	Audio Bus Master 1 Command Register	00h	Page 194
29h	8	RC	Audio Bus Master 1 SMI Status Register	00h	Page 194
2Ah-2Bh	--	--	Reserved	xxh	Page 195
2Ch-2Fh	32	R/W	Audio Bus Master 1 PRD Table Address	00000000h	Page 195
30h	8	R/W	Audio Bus Master 2 Command Register	00h	Page 195
31h	8	RC	Audio Bus Master 2 SMI Status Register	00h	Page 195
32h-33h	--	--	Reserved	xxh	Page 195
34h-37h	32	R/W	Audio Bus Master 2 PRD Table Address	00000000h	Page 195
38h	8	R/W	Audio Bus Master 3 Command Register	00h	Page 195
39h	8	RC	Audio Bus Master 3 SMI Status Register	00h	Page 196
3Ah-3Bh	--	--	Reserved	xxh	Page 196
3Ch-3Fh	32	R/W	Audio Bus Master 3 PRD Table Address	00000000h	Page 196

Table 5-8. F3BAR: XpressAUDIO™ Subsystem Configuration Registers Summary (Continued)

F3BAR+ Memory Offset	Width (Bits)	Type	Name	Reset Value	Reference (Table 5-21)
40h	8	R/W	Audio Bus Master 4 Command Register	00h	Page 196
41h	8	RC	Audio Bus Master 4 SMI Status Register	00h	Page 196
42h-43h	--	--	Reserved	xxh	Page 196
44h-47h	32	R/W	Audio Bus Master 4 PRD Table Address	00000000h	Page 197
48h	8	R/W	Audio Bus Master 5 Command Register	00h	Page 197
49h	8	RC	Audio Bus Master 5 SMI Status Register	00h	Page 197
4Ah-4Bh	--	--	Reserved	xxh	Page 197
4Ch-4Fh	32	R/W	Audio Bus Master 5 PRD Table Address	00000000h	Page 197
50h-FFh	--	--	Reserved	xxh	Page 197

Table 5-9. Function 4: PCI Header Registers for Video Controller Summary

F4 Index	Width (Bits)	Type	Name	Reset Value	Reference (Table 5-22)
00h-01h	16	RO	Vendor Identification	1078h	Page 198
02h-03h	16	RO	Device Identification	0104h	Page 198
04h-05h	16	R/W	PCI Command	0000h	Page 198
06h-07h	16	RO	PCI Status	0280h	Page 198
08h	8	RO	Device Revision ID	00h	Page 198
09h-0Bh	24	RO	PCI Class Code	030000h	Page 198
0Ch	8	RO	PCI Cache Line Size	00h	Page 198
0Dh	8	RO	PCI Latency Timer	00h	Page 198
0Eh	8	RO	PCI Header Type	00h	Page 198
0Fh	8	RO	PCI BIST Register	00h	Page 198
10h-13h	32	R/W	**Base Address Register (F4BAR):** Sets base address for memory mapped video controller configuration registers (summarized in Table 4-10).	00000000h	Page 198
14h-3Fh	--	--	Reserved	00h	Page 198
40h-FFh	--	--	Reserved	xxh	Page 198

Table 5-10. F4BAR: Video Controller Configuration Registers Summary

F4BAR+ Memory Offset	Width (Bits)	Type	Register Name	Reset Value	Reference (Table 5-23)
00h-03h	32	R/W	Video Configuration Register	00000000h	Page 199
04h-07h	32	R/W	Display Configuration Register	x0000000h	Page 200
08h-0Bh	32	R/W	Video X Register	xxxxxxxxh	Page 201
0Ch-0Fh	32	R/W	Video Y Register	xxxxxxxxh	Page 201
10h-13h	32	R/W	Video Scale Register	xxxxxxxxh	Page 201
14h-17h	32	R/W	Video Color Key Register	xxxxxxxxh	Page 201
18h-1Bh	32	R/W	Video Color Mask Register	xxxxxxxxh	Page 201
1Ch-1Fh	32	R/W	Palette Address Register	xxxxxxxxh	Page 201
20h-23h	32	R/W	Palette Data Register	xxxxxxxxh	Page 201
24h-27h	32	R/W	Dot Clock Configuration Register	00000000h	Page 202
28h-2Bh	32	R/W	CRC Signature and TFT/TV Configuration Register	00000100h	Page 203
2Ch-FFh	--	--	Reserved	xxh	Page 203

Table 5-11. USB PCI Configuration Registers Summary

USB Index	Width (Bits)	Type	Name	Reset Value	Reference (Table 5-25)
00h-01h	16	RO	Vendor Identification	0E11h	Page 205
02h-03h	16	RO	Device Identification	A0F8h	Page 205
04h-05h	16	R/W	Command Register	0000h	Page 205
06h-07h	16	R/W	Status Register	0280h	Page 205
08h	8	RO	Device Revision ID	06h	Page 206
09h-0Bh	24	RO	Class Code	0C0310h	Page 206
0Ch	8	R/W	Cache Line Size	00h	Page 206
0Dh	8	R/W	Latency Timer	00h	Page 206
0Eh	8	RO	Header Type	00h	Page 206
0Fh	8	RO	BIST Register	00h	Page 206
10h-13h	32	R/W	**Base Address Register (USB BAR):** Sets the base address of the memory mapped USB controller registers. Refer to Table 5-26 for the USB controller register bit formats and reset values.	00000000h	Page 206
14h-3Bh	--	--	Reserved	xxh	Page 206
3Ch	8	R/W	Interrupt Line Register	00h	Page 206
3Dh	8	RO	Interrupt Pin Register	01h	Page 206
3Eh	8	RO	Min. Grant Register	00h	Page 206
3Fh	8	RO	Max. Latency Register	50h	Page 206
40h-43h	32	R/W	ASIC Test Mode Enable Register	000F0000h	Page 206
44h-45h	16	R/W	ASIC Operational Mode Enable	0000h	Page 206
46h-47h	--	--	Reserved	00h	Page 207
48h-FFh	--	--	Reserved	xxh	Page 207

Table 5-12. USB BAR: USB Controller Registers Summary

USB BAR+ Memory Offset	Width (Bits)	Type	Name	Reset Value	Reference (Table 5-26)
00h-03h	32	R/W	HcRevision	00000110h	Page 208
04h-07h	32	R/W	HcControl	00000000h	Page 208
08h-0Bh	32	R/W	HcCommandStatus	00000000h	Page 208
0Ch-0Fh	32	R/W	HcInterruptStatus	00000000h	Page 208
10h-13h	32	R/W	HcInterruptEnable	00000000h	Page 209
14h-17h	32	R/W	HcInterruptDisable	C000006Fh	Page 209
18h-1Bh	32	R/W	HcHCCA	00000000h	Page 209
1Ch-1Fh	32	R/W	HcPeriodCurrentED	00000000h	Page 209
20h-23h	32	R/W	HcControlHeadED	00000000h	Page 209
24h-27h	32	R/W	HcControlCurrentED	00000000h	Page 209
28h-2Bh	32	R/W	HcBulkHeadED	00000000h	Page 209
2Ch-2Fh	32	R/W	HcBulkCurrentED	00000000h	Page 209
30h-33h	32	R/W	HcDoneHead	00000000h	Page 210
34h-37h	32	R/W	HcFmInterval	00002EDFh	Page 210
38h-3Bh	32	RO	HcFrameRemaining	00002Exxh	Page 210
3Ch-3Fh	32	RO	HcFmNumber	00000000h	Page 210
40h-43h	32	R/W	HcPeriodicStart	00000000h	Page 210
44h-47h	32	R/W	HcLSThreshold	00000628h	Page 210
48h-4Bh	32	R/W	HcRhDescriptorA	01000002h	Page 210

Table 5-12. USB BAR: USB Controller Registers Summary (Continued)

USB BAR+ Memory Offset	Width (Bits)	Type	Name	Reset Value	Reference (Table 5-26)
4Ch-4Fh	32	R/W	HcRhDescriptorB	00000000h	Page 211
50h-53h	32	R/W	HcRhStatus	00000000h	Page 211
54h-57h	32	R/W	HcRhPortStatus[1]	00000628h	Page 212
58h-5Bh	32	R/W	HcRhPortStatus[2]	01000002h	Page 213
5Ch-5Fh	32	--	Reserved	00000000h	Page 213
60h-9Fh	--	--	Reserved	xxh	Page 213
100h-103h	32	R/W	HceControl	00000000h	Page 214
104h-107h	32	R/W	HceInput	000000xxh	Page 214
108h-10Dh	32	R/W	HceOutput	000000xxh	Page 214
10Ch-10Fh	32	R/W	HceStatus	00000000h	Page 214

Table 5-13. ISA Legacy I/O Registers Summary

I/O Port	Type	Name	Reference
DMA Channel Control Registers (Table 5-27)			
000h	R/W	DMA Channel 0 Address Register	Page 215
001h	R/W	DMA Channel 0 Transfer Count Register	Page 215
002h	R/W	DMA Channel 1 Address Register	Page 215
003h	R/W	DMA Channel 1 Transfer Count Register	Page 215
004h	R/W	DMA Channel 2 Address Register	Page 215
005h	R/W	DMA Channel 2 Transfer Count Register	Page 215
006h	R/W	DMA Channel 3 Address Register	Page 215
007h	R/W	DMA Channel 3 Transfer Count Register	Page 215
008h	Read	DMA Status Register, Channels 3:0	Page 215
	Write	DMA Command Register, Channels 3:0	Page 215
009h	WO	Software DMA Request Register, Channels 3:0	Page 216
00Ah	R/W	DMA Channel Mask Register, Channels 3:0	Page 216
00Bh	WO	DMA Channel Mode Register, Channels 3:0	Page 216
00Ch	WO	DMA Clear Byte Pointer Command, Channels 3:0	Page 216
00Dh	WO	DMA Master Clear Command, Channels 3:0	Page 216
00Eh	WO	DMA Clear Mask Register Command, Channels 3:0	Page 216
00Fh	WO	DMA Write Mask Register Command, Channels 3:0	Page 216
0C0h	R/W	DMA Channel 4 Address Register (Not used)	Page 216
0C2h	R/W	DMA Channel 4 Transfer Count Register (Not Used)	Page 216
0C4h	R/W	DMA Channel 5 Address Register	Page 216
0C6h	R/W	DMA Channel 5 Transfer Count Register	Page 216
0C8h	R/W	DMA Channel 6 Address Register	Page 216
0CAh	R/W	DMA Channel 6 Transfer Count Register	Page 216
0CCh	R/W	DMA Channel 7 Address Register	Page 216
0CEh	R/W	DMA Channel 7 Transfer Count Register	Page 216
0D0h	Read	DMA Status Register, Channels 7:4	Page 217
	Write	DMA Command Register, Channels 7:4	Page 217
0D2h	WO	Software DMA Request Register, Channels 7:4	Page 217
0D4h	R/W	DMA Channel Mask Register, Channels 7:0	Page 217
0D6h	WO	DMA Channel Mode Register, Channels 7:4	Page 217
0D8h	WO	DMA Clear Byte Pointer Command, Channels 7:4	Page 217

Table 5-13. ISA Legacy I/O Registers Summary (Continued)

I/O Port	Type	Name	Reference
0DAh	WO	DMA Master Clear Command, Channels 7:4	Page 217
0DCh	WO	DMA Clear Mask Register Command, Channels 7:4	Page 217
0DEh	WO	DMA Write Mask Register Command, Channels 7:4	Page 217
DMA Page Registers (Table 5-28)			
081h	R/W	DMA Channel 2 Low Page Register	Page 218
082h	R/W	DMA Channel 3 Low Page Register	Page 218
083h	R/W	DMA Channel 1 Low Page Register	Page 218
087h	R/W	DMA Channel 0 Low Page Register	Page 218
089h	R/W	DMA Channel 6 Low Page Register	Page 218
08Ah	R/W	DMA Channel 7 Low Page Register	Page 218
08Bh	R/W	DMA Channel 5 Low Page Register	Page 218
08Fh	R/W	ISA Refresh Low Page Register	Page 218
481h	R/W	DMA Channel 2 High Page Register	Page 218
482h	R/W	DMA Channel 3 High Page Register	Page 218
483h	R/W	DMA Channel 1 High Page Register	Page 218
487h	R/W	DMA Channel 0 High Page Register	Page 218
489h	R/W	DMA Channel 6 High Page Register	Page 218
48Ah	R/W	DMA Channel 7 High Page Register	Page 218
48Bh	R/W	DMA Channel 5 High Page Register	Page 218
Programmable Interval Timer Registers (Table 5-29)			
040h	Write	PIT Timer 0 Counter	Page 219
	Read	PIT Timer 0 Status	Page 219
041h	Write	PIT Timer 1 Counter (Refresh)	Page 219
	Read	PIT Timer 1 Status (Refresh)	Page 219
042h	Write	PIT Timer 2 Counter (Speaker)	Page 219
	Read	PIT Timer 2 Status (Speaker)	Page 219
043h	Write	PIT Mode Control Word Register	Page 219
043h	R/W	PIT Read-Back Command	
		Read Status Command	
		Counter Latch Command	
Programmable Interrupt Controller Registers (Table 5-30)			
020h / 0A0h	WO	Master / Slave PCI IWC1	Page 220
021h / 0A1h	WO	Master / Slave PIC ICW2	Page 220
021h / 0A1h	WO	Master / Slave PIC ICW3	Page 220
021h / 0A1h	WO	Master / Slave PIC ICW4	Page 220
021h / 0A1h	R/W	Master / Slave PIC OCW1	Page 220
020h / 0A0h	WO	Master / Slave PIC OCW2	Page 220
020h / 0A0h	WO	Master / Slave PIC OCW3	Page 221
020h / 0A0h	RO	Master / Slave PIC Interrupt Request and Service Registers for OCW3 Commands	Page 221
Keyboard Controller Registers (Table 5-31)			
060h	R/W	External Keyboard Controller Data Register	Page 222
061h	R/W	Port B Control Register	Page 222
062h	R/W	External Keyboard Controller Mailbox Register	Page 222
064h	R/W	External Keyboard Controller Command Register	Page 222
066h	R/W	External Keyboard Controller Mailbox Register	Page 222
092h	R/W	Port A Control Register	Page 222

Table 5-13. ISA Legacy I/O Registers Summary (Continued)

I/O Port	Type	Name	Reference
Real Time Clock Registers (Table 5-32)			
070h	WO	RTC Address Register	Page 222
071h	R/W	RTC Data Register	Page 222
Miscellaneous Registers (Table 5-33)			
170h-177h/ 376h	R/W	Secondary IDE Registers	Page 223
1F0h-1F7h/ 3F6h	R/W	Primary IDE Registers	Page 223
4D0h	R/W	Interrupt Edge/Level Select Register 1	Page 223
4D1h	R/W	Interrupt Edge/Level Select Register 2	Page 223
121Ch-121Fh	RO	ACPI Timer Count Register **Note:** The ACPI Timer Count Register is accessible through I/O Port 121Ch. Otherwise use F1BAR+Offset 1Ch.	Page 223

Table 5-14. V-ACPI I/O Register Space Summary

ACPI_ BASE	Type	Align	Length	Name	Reset Value	Reference (Table 5-34)
00h-03h	R/W	4	4	P_CNT: Processor Control Register	00000000h	Page 224
04h	RO	1	1	P_LVL2: Enter C2 Power State Register	00h	Page 224
05h	--	1	1	Reserved	00h	Page 224
06h	R/W	1	1	SMI_CMD: OS/BIOS Requests Register (ACPI Enable/ Disable Port)	00h	Page 224
07h	--	1	1	Reserved	00h	Page 225
08h-09h	R/W	2	2	PM1A_STS: PM1A Status Register	0000h	Page 225
0Ah-0Bh	R/W	2	2	PM1A_EN: PM1A Enable Register	0000h	Page 225
0Ch-0Dh	R/W	4	2	PM1A_CNT: PM1A Control Register	0000h	Page 225
0Eh-0Fh	R/W	2	2	SETUP_IDX: Setup Index Register (V-ACPI internal index register)	0000h	Page 226
10h-11h	R/W	2	2	GPE0_STS: General Purpose Event 0 Status Register	0000h	Page 226
12h-13h	R/W	2	2	GPE0_EN: General Purpose Event 0 Enable Register	0000h	Page 226
14h-17h	R/W	4	4	SETUP_DATA: Setup Data Register (V-ACPI internal data register)	00000000h	Page 227
18h-1Fh	--		8	Reserved: For Future V-ACPI Implementations	--	Page 227

5.3 Chipset Register Space

The Chipset Register Space of the CS5530A is comprised of five separate functions (Function 0 through 4, F0-F4), each with its own register space and PCI header registers. F1-F4 have memory or I/O mapped registers from a Base Address Register (BAR). The PCI header registers in all functions are very similar.

F0: Bridge Configuration Register Space
F1: SMI Status and ACPI Timer Register Space
F2: IDE Controller Register Space
F3: XpressAUDIO™ Subsystem Register Space
F4: Video Controller Register Space

5.3.1 Bridge Configuration Registers - Function 0

The register space designated as Function 0 (F0) contains registers used to configure features (e.g., power management) and functionality unique to the CS5530A. All registers in Function 0 are directly accessed (i.e., there are no memory or I/O mapped registers in F0). Table 5-15 gives the bit formats for these registers.

The registers at F0 Index 50h-FFh can also be accessed at F1BAR+Memory Offset 50h-FFh. The preferred method is to program these registers through the F0 register space.

If the F0 PCI Configuration Trap bit (F0 Index 41h[0]) is enabled and an access is attempted to any of the F0 PCI header and bridge configuration registers except F0 Index 40h-43h, an SMI is generated instead.

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers

Bit	Description
Index 00h-01h	**Vendor Identification Register (RO)** — **Reset Value = 1078h**
15:0	**Vendor Identification Register (Read Only)**
Index 02h-03h	**Device Identification Register (RO)** — **Reset Value = 0100h**
15:0	**Device Identification Register (Read Only)**
Index 04h-05h	**PCI Command Register (R/W)** — **Reset Value = 000Fh**
15:10	**Reserved:** Set to 0.
9	**Fast Back-to-Back Enable (Read Only):** This function is not supported when the CS5530A is a master. It is always disabled (always reads 0).
8	**SERR#:** Allow SERR# assertion on detection of special errors. 0 = Disable **(Default)**; 1 = Enable.
7	**Wait Cycle Control (Read Only):** This function is not supported in the CS5530A. It is always disabled (always reads 0).
6	**Parity Error:** Allow the CS5530A to check for parity errors on PCI cycles for which it is a target, and to assert PERR# when a parity error is detected. 0 = Disable **(Default)**; 1 = Enable.
5	**VGA Palette Snoop Enable (Read Only):** This function is not supported in the CS5530A. It is always disabled (always reads 0).
4	**Memory Write and Invalidate:** Allow the CS5530A to do memory write and invalidate cycles, if the PCI Cache Line Size Register (F0 Index 0Ch) is set to 16 bytes (04h). 0 = Disable **(Default)**; 1 = Enable.
3	**Special Cycles:** Allow the CS5530A to respond to special cycles. 0 = Disable; 1 = Enable **(Default)**. This bit must be enabled to allow the CPU Warm Reset internal signal to be triggered from a CPU Shutdown cycle.
2	**Bus Master:** Allow the CS5530A bus mastering capabilities. 0 = Disable; 1 = Enable **(Default)**. This bit must be set to 1.
1	**Memory Space:** Allow the CS5530A to respond to memory cycles from the PCI bus. 0 = Disable; 1 = Enable **(Default)**.
0	**I/O Space:** Allow the CS5530A to respond to I/O cycles from the PCI bus. 0 = Disable; 1 = Enable **(Default)**.
Index 06h-07h	**PCI Status Register (R/W)** — **Reset Value = 0280h**
15	**Detected Parity Error:** This bit is set whenever a parity error is detected. Write 1 to clear.
14	**Signaled System Error:** This bit is set whenever the CS5530A asserts SERR# active. Write 1 to clear.
13	**Received Master Abort:** This bit is set whenever a master abort cycle occurs while the CS5530A is the master. A master abort occurs when a PCI cycle is not claimed, except for special cycles. Write 1 to clear.

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
12	**Received Target Abort:** This bit is set whenever a target abort is received while the CS5530A is the master for the PCI cycle. Write 1 to clear.
11	**Signaled Target Abort:** This bit is set whenever the CS5530A signals a target abort. This occurs when an address parity error occurs for an address that hits in the active address decode space of the CS5530A. Write 1 to clear.
10:9	**DEVSEL# Timing (Read Only):** These bits are always 01, as the CS5530A always responds to cycles for which it is an active target with medium DEVSEL# timing. 00 = Fast; 01 = Medium; 10 = Slow; 11 = Reserved
8	**Data Parity Detected:** This bit is set when: 1) The CS5530A asserted PERR# or observed PERR# asserted. 2) The CS5530A is the master for the cycle in which a parity error occurred and the Parity Error bit is set (F0 Index 04h[6] = 1). Write 1 to clear.
7	**Fast Back-to-Back Capable (Read Only):** As a target, the CS5530A is capable of accepting fast back-to-back transactions. 0 = Disable; 1 = Enable. This bit is always set to 1.
6:0	**Reserved:** Set to 0.
Index 08h	**Device Revision ID Register (RO)** — **Reset Value = xxh**
7:0	**Device Revision ID (Read Only):** Device revision level. 20h for revision A; 30h for revision B.
Index 09h-0Bh	**PCI Class Code Register (RO)** — **Reset Value = 060100h**
Index 0Ch	**PCI Cache Line Size Register (R/W)** — **Reset Value = 00h**
7:0	**PCI Cache Line Size Register:** This register sets the size of the PCI cache line, in increments of four bytes. For memory write and invalidate cycles, the PCI cache line size must be set to 16 bytes (04h), and the Memory Write and Invalidate bit must be set (F0 Index 04h[4] = 1).
Index 0Dh	**PCI Latency Timer Register (R/W)** — **Reset Value = 00h**
7:4	**Reserved:** Set to 0.
3:0	**PCI Latency Timer Value:** The PCI Latency Timer Register prevents system lockup when a slave does not respond to a cycle that the CS5530A masters. If the value is set to 00h (default), the timer is disabled. If the timer is written with any other value, bits [3:0] become the four most significant bytes in a timer that counts PCI clocks for slave response. The timer is reset on each valid data transfer. If the timer expires before the next assertion of TRDY# is received, the CS5530A stops the transaction with a master abort and asserts SERR#, if enabled to do so (F0 Index 04h[8] = 1).
Index 0Eh	**PCI Header Type Register (RO)** — **Reset Value = 80h**
7:0	**PCI Header Type Register (Read Only):** This register defines the format of this header. This header is of type format 0. Additionally, bit 7 defines whether this PCI device is a multifunction device (bit 7 = 1) or not (bit 7 = 0).
Index 0Fh	**PCI BIST Register (RO)** — **Reset Value = 00h**
7	**BIST Capable (Read Only):** Is device capable of running a built-in self-test (BIST)? 0 = No; 1 = Yes,
6	**Start BIST:** Setting this bit to a one starts up a BIST on the device. The device resets this bit when the BIST has been completed. (Not supported.)
5:4	**Reserved (Read Only)**
3:0	**BIST Completion Code (Read Only):** Upon completion of the BIST, the completion code is stored in these bits. A completion code of zero indicates the BIST has successfully been completed. All other values indicate some type of BIST failure.
Index 10h-1Fh	**Reserved** — **Reset Value = xxh**
Index 20h-3Fh	**Reserved** — **00h**
Index 40h	**PCI Function Control Register 1 (R/W)** — **Reset Value = 89h**
7	**PCI Interrupt Acknowledge Cycle Response:** Allow the CS5530A responds to PCI interrupt acknowledge cycles. 0 = Disable; 1 = Enable.
6	**Single Write Mode:** The CS5530A accepts only single cycle write transfers as a slave on the PCI bus and performs a target disconnect with the first data transferred. 0 = Disable (accepts burst write cycles); 1 = Enable.
5	**Single Read Mode:** The CS5530A accepts only single cycle read transfers as a slave on the PCI bus and performs a target disconnect with the first data transferred. 0 = Disable (accepts burst read cycles); 1 = Enable.
4	**Retry PCI Cycles:** Retry inbound PCI cycles if data is buffered and waiting to go outbound on PCI. 0 = No Retry; 1 = Retry.

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
3	**Write Buffer:** PCI slave write buffer. 0 = Disable; 1 = Enable.
2:1	**Reserved:** Set to 0.
0	**BS8/16:** This bit can not be written. Always = 1.
Note: Bits 6 and 5 emulate the behavior of first generation SIO devices developed for PCI. They should normally remain cleared.	
Index 41h	**PCI Function Control Register 2 (R/W)** **Reset Value = 10h**
7	**Burst to Beat:** If this bit is set to 1, the CS5530A performs a single access from the PCI bus. If set to 0, burst accesses are enabled.
6	**F2 IDE Configuration Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access is attempted to one of the F2 PCI header registers, an SMI is generated instead. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[9]. Second level SMI status is reported at F1BAR+Memory Offset 04h/06h[5].
5	**PERR# Signals SERR#:** Assert SERR# any time that PERR# is asserted or detected active by the CS5530A (allows PERR# assertion to be cascaded to NMI (SMI) generation in the system). 0 = Disable; 1 = Enable.
4	**Write Buffer Enable:** Allow 16-byte buffering for X-Bus to PCI bus writes. 0 = Disable; 1 = Enable.
3	**F1 Power Management Configuration Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs to one of the F1 PCI configuration header registers, an SMI is generated. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[9]. Second level SMI status is reported at F1BAR+Memory Offset 04h/06h[5].
2:1	**Subtractive Decode:** These bits determine the point at which the CS5530A accepts cycles that are not claimed by another device. The CS5530A defaults to taking subtractive decode cycles in the default cycle clock, but can be moved up to the Slow Decode cycle point if all other PCI devices decode in the fast or medium clocks. Disabling subtractive decode must be done with care, as all ISA and ROM cycles are decoded subtractively. 00 = Default sample (4th clock from FRAME# active) 01 = Slow sample (3rd clock from FRAME# active) 1x = No subtractive decode
0	**F0 PCI Configuration Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access is attempted to any of the F0 PCI header registers except F0 Index 40h-43h, an SMI is generated instead. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[9]. Second level SMI status is reported at F1BAR+Memory Offset 04h/06h[5].
Index 42h	**PCI Function Control Register 3 (R/W)** **Reset Value = ACh**
7	**USB SMI I/O Configuration:** Route USB-generated SMI to SMI# pin. 0 = Disable; 1 = Enable, USB-generated SMI pulls SMI# pin active (low).
6	**USB SMI Power Mgmnt Configuration:** Route USB-generated SMI to Top Level SMI Status Register, F1BAR+Memory Offset 00h/02h[14]. 0 = Disable; 1 = Enable.
5	**Delayed Transactions:** Allow delayed transactions on the PCI bus. 0 = Disable; 1 = Enable. Also see F0 Index 43h[1].
4	**DMA Priority:** Allow USB DMA to have priority over other DMA requests. 0 = Disable; 1 = Enable.
3	**No X-Bus ARB, Buffer Enable:** When the CS5530A is a PCI target, allow buffering of PCI transactions without X-Bus arbitration. 0 = Disable; 1 = Enable.
2	**HOLD_REQ# (Pin H26):** HOLD_REQ# signal (pin H26). 0 = Disable; 1 = Enable. **Note:** Although the HOLD_REQ# signal function is no longer applicable, this bit must remain at its reset value (i.e., enabled, set to 1) for non-preemptive arbitration to operate correctly.
1	**F4 Video Configuration Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access is attempted to one of the F4 PCI header registers, an SMI is generated instead. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[9]. Second level SMI status is reported at F1BAR+Memory Offset 04h/06h[5].
0	**F3 Audio Configuration Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access is attempted to one of the F3 PCI header registers, an SMI is generated instead. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[9]. Second level SMI status is reported at F1BAR+Memory Offset 04h/06h[5].
Index 43h	**USB Shadow Register (R/W)** **Reset Value = 03h**
7	**Reserved:** Set to 0.

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
6	**Enable SA20:** Pin AD22 configuration. 0 = GPIO4; 1 = SA20. If bit 6 or bit 2 is set to 1, then pin AD22 = SA20.
5	**Legacy Cycles Assert HOLD_REQ#:** Allow legacy cycles to cause HOLD_REQ# to be asserted. 0 = Disable; 1 = Enable. **Note:** The HOLD_REQ# signal function is no longer applicable, this bit must remain at its reset value (i.e., disable).
4	**Read Cycles Assert HOLD_REQ#:** Allow read cycles to cause HOLD_REQ# to be asserted. 0 = Disable; 1 = Enable. **Note:** The HOLD_REQ# signal function is no longer applicable, this bit must remain at its reset value (i.e., disable).
3	**Any Cycle Asserts HOLD_REQ#:** Allow any cycle to cause HOLD_REQ# to be asserted. 0 = Disable; 1 = Enable. **Note:** The HOLD_REQ# signal function is no longer applicable, this bit must remain at its reset value (i.e., disable).
2	**Enable SA[23:20]:** Pins AF23, AE23, AC21, and AD22 configuration. 0 = GPIO[7:4]; 1 = SA[23:20]. If F0 Index 43h bit 6 or bit 2 is set to 1, then pin AD22 = SA20.
1	**PCI Retry Cycles:** When the CS5530A is a PCI target and the PCI buffer is not empty, allow the PCI bus to retry cycles. 0 = Disable; 1 = Enable. This bit works in conjunction with PCI bus delayed transactions bit. F0 Index 42h[5] must = 1 for this bit to be valid.
0	**USB Core:** 0 = Disable; 1 = Enable.
Index 44h	**Reset Control Register (R/W)** — **Reset Value = 01h**
7	**ISA Mode:** This bit is set to read back the strap value of the INTR pin (pin P26) during POR. 0 = ISA Limited; 1 = ISA Master. This bit can be written after POR# deasserts to change the ISA mode selected. However, writing to this bit is not recommended due to the actual strapping done on the board.
6	**IDSEL Mode:** This bit is set to read back the strap value of the HOLD_REQ# pin (pin H26) during POR. 0 = AD28 is IDSEL for Chipset Register Space and AD29 is IDSEL for USB Register Space; 1 = AD26 is IDSEL for Chipset Register Space and AD27 is IDSEL for USB Register Space. This bit can be written after POR# deasserts to change the IDSEL settings. However, writing to this bit is not recommended due to the actual strapping done on the board.
5:4	**Clock 32K Control:** Controls the source of the CLK_32K pin (AE3). 00 = CLK_32K is internally derived from CLK_14MHZ (pin P24) and is not output on pin AE3 (**Default**) 01 = CLK_32K is internally derived from CLK_14MHZ (pin P24) and is output on pin AE3 10 = CLK_32K is an input 11 = Invalid
3	**IDE Controller Reset:** Reset both of the CS5530A IDE controllers' internal state machines. 0 = Run; 1 = Reset. This bit is level-sensitive and must be explicitly cleared to 0 to remove the reset.
2	**IDE Reset:** Reset IDE bus. 0 = Deassert IDE bus reset signal; 1 = Assert IDE bus reset signal. This bit is level-sensitive and must be explicitly cleared to 0 to remove the reset.
1	**PCI Reset:** Reset PCI bus. 0 = Disable; 1 = Enable. When set, the CS5530A PCI_RST# output signal (pin C14) is asserted and all devices on the PCI bus including PCIUSB are reset. No other function within the CS5530A is affected by this bit. It does not reset PCI registers. Write 0 to clear. This bit is level-sensitive and must be cleared after the reset is enabled.
0	**X-Bus Warm Start:** Reading and writing this bit has two different meanings/functions. Reading this bit: Has a warm start occurred since power-up? 0 = Yes; 1 = No Writing this bit: 0 = NOP; 1 = Execute system wide reset (used only for clock configuration at power-up). **Note:** X-Bus warm start will toggle the CPU_RST and PCI_RST# lines.
Index 45h-4Fh	**Reserved** — **Reset Value = 00h**
Index 50h	**PIT Control/ISA CLK Divider (R/W)** — **Reset Value = 7Bh**
7	**PIT Software Reset:** 0 = Disable; 1 = Enable.
6	**PIT Counter 1:** 0 = Forces Counter 1 output (OUT1) to zero; 1 = Allows Counter 1 output (OUT1) to pass to I/O Port 061h[4].
5	**PIT Counter 1 Enable:** 0 = Sets GATE1 input low; 1 = Sets GATE1 input high.
4	**PIT Counter 0:** 0 = Forces Counter 0 output (OUT0) to zero; 1 = Allows Counter 0 output (OUT0) to pass to IRQ0.
3	**PIT Counter 0 Enable:** 0 = Sets GATE0 input low; 1 = Sets GATE0 input high.

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
2:0	**ISA Clock Divisor:** Determines the divisor of the PCI clock used to make the ISA clock, which is typically programmed for approximately 8 MHz. 000 = Reserved 001 = Divide by two 010 = Divide by three 011 = Divide by four 100 = Divide by five 101 = Divide by six 110 = Divide by seven 111 = Divide by eight If 25 MHz PCI clock, use setting of 010 (divide by 3). If 30 or 33 MHz PCI clock, use a setting of 011 (divide by 4).
Index 51h	**ISA I/O Recovery Control Register (R/W)** — **Reset Value = 40h**
7:4	**8-Bit I/O Recovery:** These bits determine the number of ISA bus clocks between back-to-back 8-bit I/O read cycles. This count is in addition to a preset one-clock delay built into the controller. 0000 = 1 ISA clock 0001 = 2 ISA clocks 0010 = 3 ISA clocks 0011 = 4 ISA clocks 0100 = 5 ISA clocks 0101 = 6 ISA clocks 0110 = 7 ISA clocks 0111 = 8 ISA clocks 1000 = 9 ISA clocks 1001 = 10 ISA clocks 1010 = 11 ISA clocks 1011 = 12 ISA clocks 1100 = 13 ISA clocks 1101 = 14 ISA clocks 1110 = 15 ISA clocks 1111 = 16 ISA clocks
3:0	**16-Bit I/O Recovery:** These bits determine the number of ISA bus clocks between back-to-back 16-bit I/O cycles. This count is in addition to a preset one-clock delay built into the controller. 0000 = 1 ISA clock 0001 = 2 ISA clocks 0010 = 3 ISA clocks 0011 = 4 ISA clocks 0100 = 5 ISA clocks 0101 = 6 ISA clocks 0110 = 7 ISA clocks 0111 = 8 ISA clocks 1000 = 9 ISA clocks 1001 = 10 ISA clocks 1010 = 11 ISA clocks 1011 = 12 ISA clocks 1100 = 13 ISA clocks 1101 = 14 ISA clocks 1110 = 15 ISA clocks 1111 = 16 ISA clocks
Index 52h	**ROM/AT Logic Control Register (R/W)** — **Reset Value = F8h**
7	**Snoop Fast Keyboard Gate A20 and Fast Reset:** Enables the snoop logic associated with keyboard commands for A20 Mask and Reset. 0 = Disable; 1 = Enable (snooping). If disabled, the keyboard controller handles the commands.
6	**Game Port GPORT_CS# on Writes:** Allow GPORT_CS# to be asserted for writes to the game port (I/O Port 200h and 201h). 0 = Disable; 1 = Enable.
5	**Game Port GPORT_CS# on Reads:** Allow GPORT_CS# to be asserted for reads to the game port (I/O Port 200h and 201h). 0 = Disable; 1 = Enable.
4	**Enable A20M# Deassertion on Warm Reset:** Force A20M# high during a Warm Reset (guarantees that A20M# is deasserted regardless of the state of A20). 0 = Disable; 1 = Enable.
3	**Enable I/O Port 092h Decode (Port A):** I/O Port 092h decode and the logical functions. 0 = Disable; 1 = Enable.
2	**Upper ROM Address Range:** KBROMCS# is asserted for ISA memory read accesses. 0 = FFFC0000h-FFFFFFFFh (256 KB, **Default**); 1 = FF000000h-FFFFFFFFh (16 MB) **Note:** PCI Positive decoding for the ROM space is enabled at F0 Index 5Bh[5]).
1	**ROM Write Enable:** Assert KBROMCS# during writes to configured ROM space (configured in bits 2 and 0), allowing Flash programming. 0 = Disable; 1 = Enable.
0	**Lower ROM Address Range:** KBROMCS# is asserted for ISA memory read accesses. 0 = 000F0000h-000FFFFFh (64 KB, **Default**); 1 = 000E0000h-000FFFFFh (128 KB). **Note:** PCI Positive decoding for the ROM space is enabled at F0 Index 5Bh[5]).
Index 53h	**Alternate CPU Support Register (R/W)** — **Reset Value = 00h**
7	**Reserved:** Set to 0.
6	**Game Port Write Blocks ISA:** Block ISA cycle on game port (I/O Port 200h and 201h) write. 0 = Disable; 1 = Enable.
5	**Bidirectional SMI Enable:** 0 = Disable; 1 = Enable. This bit must be set to 0.
4	**Game Port Read Block ISA:** Block ISA cycle on game port (I/O Port 200h and 201h) read. 0 = Disable; 1 = Enable.
3	**Game Port Write SMI:** Allow SMI generation on writes to game port (I/O Port 200h and 201h). 0 = Disable; 1 = Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 84h/F4h[4]. For “Game Port Read SMI”, see F0 Index 83h[4].
2	**RTC Enable/RTC Pin Configuration:** 0 = SMEMW# (Pin AF3) and SMEMR# (Pin AD4), RTC decode disabled; 1 = RTCCS# (Pin AF3) and RTCALE (Pin AD4), RTC decode enabled. **Note:** The RTC Index Shadow Register (F0 Index BBh) is independent of the setting of this bit.
1	**Reserved:** Set to 1 after register reset. Failure to do this leaves IRQ13 in an unsupported mode.

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
0	**Generate SMI on A20M# toggle:** 0 = Disable; 1 = Enable. This bit must be set to 1. SMI status is reported in F1BAR+Memory Offset 00h/02h[7] (only).
Index 54h-59h	**Reserved** — **Reset Value = xxh**
Index 5Ah	**Decode Control Register 1 (R/W)** — **Reset Value = 03h**
7	**Secondary Floppy Positive Decode:** Selects PCI positive or subtractive decoding for accesses to I/O Port 372h, 373h, 375h, and 377h. 0 = Subtractive; 1 = Positive.
6	**Primary Floppy Positive Decode:** Selects PCI positive or subtractive decoding for accesses to I/O Port 3F2h, 3F4h, 3F5h, and 3F7h. 0 = Subtractive; 1 = Positive.
5	**COM4 Positive Decode:** Selects PCI positive or subtractive decoding for accesses to I/O Port 2E8h-2EFh. 0 = Subtractive; 1 = Positive.
4	**COM3 Positive Decode:** Selects PCI positive or subtractive decoding for accesses to I/O Port 3E8h-3EFh. 0 = Subtractive; 1 = Positive.
3	**COM2 Positive Decode:** Selects PCI positive or subtractive decoding for accesses to I/O Port 2F8h-2FFh. 0 = Subtractive; 1 = Positive.
2	**COM1 Positive Decode:** Selects PCI positive or subtractive decoding for accesses to I/O Port 3F8h-3FFh. 0 = Subtractive; 1 = Positive.
1	**Keyboard Controller Positive Decode:** Selects PCI positive or subtractive decoding for accesses to I/O Port 060h and 064h (and 062h/066h if enabled). 0 = Subtractive; 1 = Positive.
0	**Real Time Clock Positive Decode:** Selects PCI positive or subtractive decoding for accesses to I/O Port 070h-7Fh. 0 = Subtractive; 1 = Positive.
Note: Positive decoding by the CS5530A speeds up the I/O cycle time. These I/O Ports do not exist in the CS5530A. It is assumed that if positive decode is enabled, the port exists on the ISA bus.	
Index 5Bh	**Decode Control Register 2 (R/W)** — **Reset Value = 20h**
7	**Keyboard I/O Port 062h/066h Decode:** This alternate port to the keyboard controller is provided in support of the 8051SL notebook keyboard controller mailbox**.** 0 = Disable; 1 = Enable.
6	**Reserved:** Set to 0.
5	**BIOS ROM Positive Decode:** Selects PCI positive or subtractive decoding for accesses to the configured ROM space. 0 = Subtractive; 1 = Positive. ROM configuration is at F0 Index 52h[2:0].
4	**Secondary IDE Controller Positive Decode:** Selects PCI positive or subtractive decoding for accesses to I/O Port 170h-177h and 376h. 0 = Subtractive; 1 = Positive. **Note:** Subtractive Decode mode disables this IDE controller entirely and routes any register references to the ISA bus.
3	**Primary IDE Controller Positive Decode:** Selects PCI positive or subtractive decoding for accesses to I/O Port 1F0h-1F7h and 3F6h. 0 = Subtractive; 1 = Positive. **Note:** Subtractive Decode mode disables this IDE controller entirely and routes any register references to the ISA bus.
2	**LPT3 Positive Decode:** Selects PCI positive or subtractive decoding for accesses to I/O Port 278h-27Fh. 0 = Subtractive; 1 = Positive. This bit does not affect 7BCh-7BEh, which is always decoded subtractively.
1	**LPT2 Positive Decode:** Selects PCI positive or subtractive decoding for accesses to I/O Port 378h-37Fh. 0 = Subtractive; 1 = Positive. This bit does not affect 678h-67Ah, which is always decoded subtractively.
0	**LPT1 Positive Decode:** Selects PCI positive or subtractive decoding for accesses to I/O Port 3BCh-3BFh. 0 = Subtractive; 1 = Positive. This bit does not affect 778h-77Ah, which is always decoded subtractively.
Note: Positive decoding by the CS5530A speeds up the I/O cycle time. The keyboard, LPT3, LPT2, and LPT1 I/O Ports do not exist in the CS5530A. It is assumed that if positive decode is enabled, the port exists on the ISA bus.	
Index 5Ch	**PCI Interrupt Steering Register 1 (R/W)** — **Reset Value = 00h**
7:4	**INTB# Target Interrupt:** Selects target interrupt for INTB#. 0000 = Disable; 0001 = IRQ1; 0010 = RSVD; 0011 = IRQ3; 0100 = IRQ4; 0101 = IRQ5; 0110 = IRQ6; 0111 = IRQ7; 1000 = RSVD; 1001 = IRQ9; 1010 = IRQ10; 1011 = IRQ11; 1100 = IRQ12; 1101 = RSVD; 1110 = IRQ14; 1111 = IRQ15

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
3:0	**INTA# Target Interrupt:** Selects target interrupt for INTA#. 0000 = Disable 0100 = IRQ4 1000 = RSVD 1100 = IRQ12 0001 = IRQ1 0101 = IRQ5 1001 = IRQ9 1101 = RSVD 0010 = RSVD 0110 = IRQ6 1010 = IRQ10 1110 = IRQ14 0011 = IRQ3 0111 = IRQ7 1011 = IRQ11 1111 = IRQ15
Note: The target interrupt must first be configured as level sensitive via I/O Port 4D0h and 4D1h in order to maintain PCI interrupt compatibility.	
Index 5Dh	**PCI Interrupt Steering Register 2 (R/W)** **Reset Value = 00h**
7:4	**INTD# Target Interrupt:** Selects target interrupt for INTD#. 0000 = Disable 0100 = IRQ4 1000 = RSVD 1100 = IRQ12 0001 = IRQ1 0101 = IRQ5 1001 = IRQ9 1101 = RSVD 0010 = RSVD 0110 = IRQ6 1010 = IRQ10 1110 = IRQ14 0011 = IRQ3 0111 = IRQ7 1011 = IRQ11 1111 = IRQ15
3:0	**INTC# Target Interrupt:** Selects target interrupt for INTC#. 0000 = Disable 0100 = IRQ4 1000 = RSVD 1100 = IRQ12 0001 = IRQ1 0101 = IRQ5 1001 = IRQ9 1101 = RSVD 0010 = RSVD 0110 = IRQ6 1010 = IRQ10 1110 = IRQ14 0011 = IRQ3 0111 = IRQ7 1011 = IRQ11 1111 = IRQ15
Note: The target interrupt must first be configured as level sensitive via I/O Port 4D0h and 4D1h in order to maintain PCI interrupt compatibility.	
Index 5Eh-6Fh	**Reserved** **Reset Value = xxh**
Index 70h-71h	**General Purpose Chip Select Base Address Register (R/W)** **Reset Value = 0000h**
15:0	**General Purpose Chip Select I/O Base Address:** This 16-bit value represents the I/O base address used to enable the assertion of the GPCS# signal. This register, together with General Purpose Chip Select Control Register (F0 Index 72h) is used to configure the operation of the GPCS# pin.
Index 72h	**General Purpose Chip Select Control Register (R/W)** **Reset Value = 00h**
7	**General Purpose Chip Select:** GPCS# (pin AF26). 0 = Disable; 1 = Enable. If the GPCS# signal is disabled (i.e., this bit = 0) its output is permanently driven high.
6	**Writes Result in Chip Select:** Writes to configured I/O address (base address configured in F0 Index 70h and range configured in bits [4:0]) causes GPCS# signal to be asserted. 0 = Disable; 1 = Enable.
5	**Reads Result in Chip Select:** Reads from configured I/O address (base address configured in F0 Index 70h and range configured in bits [4:0]) causes GPCS# signal to be asserted. 0 = Disable; 1 = Enable.
4:0	**General Purpose Chip Select I/O Address Range:** This 5-bit field selects the range of GPCS# signal. 00000 = 1 byte 01111 = 16 bytes 00001 = 2 bytes 11111 = 32 bytes 00011 = 4 bytes All other combinations are reserved. 00111 = 8 bytes
Note: This register, together with General Purpose Chip Select Base Address Register (F0 Index 70h) is used to configure the operation of the GPCS# pin.	
Index 73h-7Fh	**Reserved** **Reset Value = xxh**
Index 80h	**Power Management Enable Register 1 (R/W)** **Reset Value = 00h**
7:6	**Reserved:** Set to 0.
5	**Codec SDATA_IN SMI:** Allow AC97 codec to generate an SMI due to codec producing a positive edge on SDATA_IN. 0 = Disable; 1 = Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 87h/F7h[2].
4	**Video Speedup:** Any video activity, as decoded from the serial connection (PSERIAL register, bit 0) from the GX1 processor disables clock throttling (via SUSP#/SUSPA# handshake) for a configurable duration when the system is power managed using CPU Suspend modulation. 0 = Disable; 1 = Enable. The duration of the speedup is configured in the Video Speedup Timer Count Register (F0 Index 8Dh). Detection of an external VGA access (3Bxh, 3Cxh, 3Dxh and A000h-B7FFh) on the PCI bus is also supported. This configuration is non-standard, but it does allow the power management routines to support an external VGA chip.

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
3	**IRQ Speedup:** Any unmasked IRQ (per I/O Port 021h/0A1h) or SMI disables clock throttling (via SUSP#/SUSPA# handshake) for a configurable duration when the system is power managed using CPU Suspend modulation. 0 = Disable; 1 = Enable. The duration of the speedup is configured in the IRQ Speedup Timer Count Register (F0 Index 8Ch).
2	**Traps:** Globally enable all power management device I/O traps. 0 = Disable; 1 = Enable. This excludes the audio I/O traps. They are enabled at F3BAR+Memory Offset 18h.
1	**Idle Timers:** Globally enable all power management device idle timers. 0 = Disable; 1 = Enable. Note, disable at this level does not reload the timers on the enable. The timers are disabled at their current counts. This bit has no effect on the Suspend Modulation OFF/ON Timers (F0 Index 94h/95h), nor on the General Purpose (UDEFx) Timers (F0 Index 88h-8Bh). This bit must be set for the command to trigger the SUSP#/SUSPA# feature to function (see F0 Index AEh).
0	**Power Management:** Global power management. 0 = Disable; 1 = Enabled. This bit must be set (1) immediately after POST for some power management resources to function. Until this is done, the command to trigger the SUSP#/SUSPA# feature is disabled (see F0 Index AEh) and all SMI# trigger events listed for F0 Index 84h-87h are disabled. A '0' in this bit does NOT stop the Idle Timers if bit 1 of this register is a '1', but only prevents them from generating an SMI# interrupt. It also has no effect on the UDEF traps.
Index 81h	**Power Management Enable Register 2 (R/W)** **Reset Value = 00h**
7	**Video Access Idle Timer Enable:** Load timer from Video Idle Timer Count Register (F0 Index A6h) and generate an SMI when the timer expires. 0 = Disable; 1 = Enable. If an access occurs in the video address range (sets bit 0 of the GX1 processor's PSERIAL register) the timer is reloaded with the programmed count. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[7].
6	**User Defined Device 3 (UDEF3) Idle Timer Enable:** Load timer from UDEF3 Idle Timer Count Register (F0 Index A4h) and generate an SMI when the timer expires. 0 = Disable; 1 = Enable. If an access occurs in the programmed address range the timer is reloaded with the programmed count. UDEF3 address programming is at F0 Index C8h (base address register) and CEh (control register). Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[6].
5	**User Defined Device 2 (UDEF2) Idle Timer Enable:** Load timer from UDEF2 Idle Timer Count Register (F0 Index A2h) and generate an SMI when the timer expires. 0 = Disable; 1 = Enable. If an access occurs in the programmed address range the timer is reloaded with the programmed count. UDEF2 address programming is at F0 Index C4h (base address register) and CDh (control register). Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[5].
4	**User Defined Device 1 (UDEF1) Idle Timer Enable:** Load timer from UDEF1 Idle Timer Count Register (F0 Index A0h) and generate an SMI when the timer expires. 0 = Disable; 1 = Enable. If an access occurs in the programmed address range the timer is reloaded with the programmed count. UDEF1 address programming is at F0 Index C0h (base address register) and CCh (control register). Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[4].
3	**Keyboard/Mouse Idle Timer Enable:** Load timer from Keyboard/Mouse Idle Timer Count Register (F0 Index 9Eh) and generate an SMI when the timer expires. 0 = Disable; 1 = Enable. If an access occurs in the address ranges (listed below) the timer is reloaded with the programmed count. Keyboard Controller: I/O Ports 060h/064h COM1: I/O Port 3F8h-3FFh (if F0 Index 93h[1:0] = 10 this range is included) COM2: I/O Port 2F8h-2FFh (if F0 Index 93h[1:0] = 11 this range is included) Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[3].

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
2	**Parallel/Serial Idle Timer Enable:** Load timer from Parallel/Serial Port Idle Timer Count Register (F0 Index 9Ch) and generate an SMI when the timer expires. 0 = Disable; 1 = Enable. If an access occurs in the address ranges (listed below) the timer is reloaded with the programmed count. LPT1: I/O Port 378h-37Fh, 778h-77Ah LPT2: I/O Port 278h-27Fh, 678h-67Ah COM1: I/O Port 3F8h-3FFh (if F0 Index 93h[1:0] = 10 this range is excluded) COM2: I/O Port 2F8h-2FFh (if F0 Index 93h[1:0] = 11 this range is excluded) COM3: I/O Port 3E8h-3EFh COM4: I/O Port 2E8h-2EFh Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[2].
1	**Floppy Disk Idle Timer Enable:** Load timer from Floppy Disk Idle Timer Count Register (F0 Index 9Ah) and generate an SMI when the timer expires. 0 = Disable; 1 = Enable. If an access occurs in the address ranges (listed below) the timer is reloaded with the programmed count. Primary floppy disk: I/O Port 3F2h, 3F4h, 3F5h, and 3F7 Secondary floppy disk: I/O Port 372h, 373h, 375h, and 377h Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[1].
0	**Primary Hard Disk Idle Timer Enable:** Load timer from Primary Hard Disk Idle Timer Count Register (F0 Index 98h) and generate an SMI when the timer expires. 0 = Disable; 1 = Enable. If an access occurs in the address ranges selected in F0 Index 93h[5], the timer is reloaded with the programmed count. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[0].
Index 82h	**Power Management Enable Register 3 (R/W)** **Reset Value = 00h**
7	**Video Access Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs in the video address range (sets bit 0 of the GX1 processor's PSERIAL register) an SMI is generated. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 86h/F6h[7].
6	**User Defined Device 3 (UDEF3) Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs in the programmed address range an SMI is generated. UDEF3 address programming is at F0 Index C8h (base address register) and CEh (control register). Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[9]. Second level SMI status is reported at F1BAR+Memory Offset 04h/06h[4].
5	**User Defined Device 2 (UDEF2) Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs in the programmed address range an SMI is generated. UDEF2 address programming is at F0 Index C4h (base address register) and CDh (control register). Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[9]. Second level SMI status is reported at F1BAR+Memory Offset 04h/06h[3].
4	**User Defined Device 1 (UDEF1) Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs in the programmed address range an SMI is generated. UDEF1 address programming is at F0 Index C0h (base address register), and CCh (control register). Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[9]. Second level SMI status is reported at F1BAR+Memory Offset 04h/06h[2].
3	**Keyboard/Mouse Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs in the address ranges (listed below) an SMI is generated. Keyboard Controller: I/O Ports 060h/064h COM1: I/O Port 3F8h-3FFh (if F0 Index 93h[1:0] = 10 this range is included) COM2: I/O Port 2F8h-2FFh (if F0 Index 93h[1:0] = 11 this range is included) Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 86h/F6h[3].

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
2	**Parallel/Serial Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs in the address ranges (listed below) an SMI is generated. LPT1: I/O Port 378h-37Fh, 778h-77Ah LPT2: I/O Port 278h-27Fh, 678h-67Ah COM1: I/O Port 3F8h-3FFh (if F0 Index 93h[1:0] = 10 this range is excluded) COM2: I/O Port 2F8h-2FFh (if F0 Index 93h[1:0] = 11 this range is excluded) COM3: I/O Port 3E8h-3EFh COM4: I/O Port 2E8h-2EFh Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 86h/F6h[2].
1	**Floppy Disk Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs in the address ranges (listed below) an SMI is generated. Primary floppy disk: I/O Port 3F2h, 3F4h, 3F5h, or 3F7 Secondary floppy disk: I/O Port 372h, 373h, 375h, or 377h Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 86h/F6h[1].
0	**Primary Hard Disk Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs in the address ranges selected in F0 Index 93h[5], an SMI is generated. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 86h/F6h[0].
Index 83h	**Power Management Enable Register 4 (R/W)** **Reset Value = 00h**
7	**Secondary Hard Disk Idle Timer Enable:** Load timer from Secondary Hard Disk Idle Timer Count Register (F0 Index ACh) and generate an SMI when the timer expires. 0 = Disable; 1 = Enable. If an access occurs in the address ranges selected in F0 Index 93h[4], the timer is reloaded with the programmed count. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 86h/F6h[4].
6	**Secondary Hard Disk Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs in the address ranges selected in F0 Index 93h[4], an SMI is generated. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 86h/F6h[5].
5	**ACPI Timer SMI:** Allow SMI generation for MSB toggles on the ACPI Timer (F1BAR+Memory Offset 1Ch or I/O Port 121Ch). 0 = Disable; 1 = Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 87h/F7h[0].
4	**Game Port Read SMI:** Allow SMI generation on reads to game port (I/O Port 200h and 201h). 0 = Disable; 1 = Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 84h/F4h[4]. For “Game Port Write SMI” see F0 Index 53h[3].
3	**VGA Timer Enable:** Turn on VGA Timer and generate an SMI when the timer reaches 0. 0 = Disable; 1 = Enable. VGA Timer programming is at F0 Index 8Eh and F0 Index 8Bh[6]. To reload the count in the VGA timer, disable it, optionally change the count value in F0 Index 8Eh[7:0], and reenable it before enabling power management. SMI Status reporting is at F1BAR+Memory Offset 00h/02h[6] (only). Although grouped with the power management Idle Timers, the VGA Timer is not a power management function. The VGA Timer counts whether power management is enabled or disabled.
2	**Video Retrace Interrupt SMI:** Allow SMI generation whenever video retrace occurs. 0 = Disable; 1 = Enable. This information is decoded from the serial connection (PSERIAL register, bit 7) from the GX1 processor. This function is normally not used for power management but for softVGA routines. SMI status reporting is at F1BAR+Memory Offset 00h/02h[5] (only).
1	**General Purpose Timer 2 (GP Timer 2) Enable:** Turn on GP Timer 2 and generate an SMI when the timer expires. 0 = Disable; 1 = Enable. This idle timer is reloaded from the assertion of GPIO7 (if programmed to do so). GP Timer 2 programming is at F0 Index 8Ah and 8Bh[5,3,2]. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[9]. Second level SMI status is reported at F1BAR+Memory Offset 04h/06h[1].

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
0	**General Purpose Timer 1 (GP Timer 1) Enable:** Turn on GP Timer 1 and generate an SMI when the timer expires. 0 = Disable; 1 = Enable. This idle timer's load is multi-sourced and is reloaded any time an enabled event (F0 Index 89h[6:0]) occurs. GP Timer 1 programming is at F0 Index 88h and 8Bh[4]. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[9]. Second level SMI status is reported at F1BAR+Memory Offset 04h/06h[0]
Index 84h	**Second Level Power Management Status Mirror Register 1 (RO)** **Reset Value = 00h**
7:5	**Reserved**
4	**Game Port SMI Status (Read Only):** SMI was caused by R/W access to game port (I/O Port 200h and 201h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. Game Port Read SMI generation enabling is at F0 Index 83h[4]. Game Port Write SMI generation enabling is at F0 Index 53h[3].
3	**GPIO7 SMI Status (Read Only):** SMI was caused by transition on (properly-configured) GPIO7 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 97h[3].
2	**GPIO5 SMI Status (Read Only):** SMI was caused by transition on (properly-configured) GPIO5 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 97h[2].
1	**GPIO4 SMI Status (Read Only):** SMI was caused by transition on (properly-configured) GPIO4 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 97h[1].
0	**GPIO3 SMI Status (Read Only):** SMI was caused by transition on (properly-configured) GPIO3 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 97h[0].
Note: Properly-configured means that the GPIO pin must be enabled as a GPIO (if multiplexed pin), as an input, and to cause an SMI. This register provides status on various power management SMI events to the SMI handler. It is called a Mirror register since an identical register exists at F0 Index F4h. Reading this register does not clear the status, while reading its counterpart at F0 Index F4h does clear the status.	
Index 85h	**Second Level Power Management Status Mirror Register 2 (RO)** **Reset Value = 00h**
7	**Video Idle Timer SMI Status (Read Only):** SMI was caused by expiration of the Video Idle Timer Count Register (F0 Index A6h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[7].
6	**User Defined Device 3 (UDEF3) Idle Timer SMI Status (Read Only):** SMI was caused by expiration of the UDEF3 Idle Timer Count Register (F0 Index A4h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[6].
5	**User Defined Device 2 (UDEF2) Idle Timer SMI Status (Read Only):** SMI was caused by expiration of the UDEF2 Idle Timer Count Register (F0 Index A2h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[5].
4	**User Defined Device 1 (UDEF1) Idle Timer SMI Status (Read Only):** SMI was caused by expiration of the UDEF1 Idle Timer Count Register (F0 Index A0h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[4].
3	**Keyboard/Mouse Idle Timer SMI Status (Read Only):** SMI was caused by expiration of the Keyboard/Mouse Idle Timer Count Register (F0 Index 9Eh)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[3].

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
2	**Parallel/Serial Idle Timer SMI Status (Read Only):** SMI was caused by expiration of the Parallel/Serial Port Idle Timer Count Register (F0 Index 9Ch)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[2].
1	**Floppy Disk Idle Timer SMI Status (Read Only):** SMI was caused by expiration of the Floppy Disk Idle Timer Count Register (F0 Index 9Ah)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[1].
0	**Primary Hard Disk Idle Timer SMI Status (Read Only):** SMI was caused by expiration of the Primary Hard Disk Idle Timer Count Register (F0 Index 98h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[0].
Note: This register provides status on the Device Idle Timers to the SMI handler. A bit set here indicates that the device was idle for the duration configured in the Idle Timer Count register for that device, causing an SMI. It is called a Mirror register since an identical register exists at F0 Index F5h. Reading this register does not clear the status, while reading its counterpart at F0 Index F5h does clear the status.	
Index 86h	**Second Level Power Management Status Mirror Register 3 (RO)** **Reset Value = 00h**
7	**Video Access Trap SMI Status (Read Only):** SMI was caused by a trapped I/O access to the Video I/O Trap? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 82h[7].
6	**Reserved (Read Only)**
5	**Secondary Hard Disk Access Trap SMI Status (Read Only):** SMI was caused by a trapped I/O access to the secondary hard disk? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 83h[6].
4	**Secondary Hard Disk Idle Timer SMI Status (Read Only):** SMI was caused by expiration of Hard Disk Idle Timer Count Register (F0 Index ACh)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 83h[7].
3	**Keyboard/Mouse Access Trap SMI Status (Read Only):** SMI was caused by a trapped I/O access to the keyboard or mouse? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 82h[3].
2	**Parallel/Serial Access Trap SMI Status (Read Only):** SMI was caused by a trapped I/O access to either the serial or parallel ports? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 82h[2].
1	**Floppy Disk Access Trap SMI Status (Read Only):** SMI was caused by a trapped I/O access to the floppy disk? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 82h[1].
0	**Primary Hard Disk Access Trap SMI Status (Read Only):** SMI was caused by a trapped I/O access to the primary hard disk? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 82h[0].
Note: This register provides status on the Device Traps to the SMI handler. A bit set here indicates that an access occurred to the device while the trap was enabled, causing an SMI. It is called a Mirror register since an identical register exists at F0 Index F6h. Reading this register does not clear the status, while reading its counterpart at F0 Index F6h does clear the status.	
Index 87h	**Second Level Power Management Status Mirror Register 4 (RO)** **Reset Value = 00h**
7	**GPIO2 SMI Status (Read Only):** SMI was caused by transition on (properly-configured) GPIO2 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 92h[2].

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
6	**GPIO1 SMI Status (Read Only):** SMI was caused by transition on (properly-configured) GPIO1 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 92h[1].
5	**GPIO0 SMI Status (Read Only):** SMI was caused by transition on (properly-configured) GPIO0 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 92h[0].
4	**Lid Position (Read Only):** This bit maintains the current status of the lid position. If the GPIO6 pin is configured as the lid switch indicator, this bit reflects the state of the pin.
3	**Lid Switch SMI Status (Read Only):** SMI was caused by a transition on the GPIO6 (lid switch) pin? 0 = No; 1 = Yes. For this to happen, the GPIO6 pin must be configured both as an input (F0 Index 90h[6] = 0) and as the lid switch (F0 Index 92h[6] =1).
2	**Codec SDATA_IN SMI Status (Read Only):** SMI was caused by AC97 codec producing a positive edge on SDATA_IN? 0 = No; 1 = Yes. This is the second level of status is reporting. The top level status is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 80h[5].
1	**RTC Alarm (IRQ8) SMI Status (Read Only):** SMI was caused by an RTC interrupt? 0 = No; 1 = Yes. This SMI event can only occur while in 3V Suspend and an RTC interrupt occurs. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0].
0	**ACPI Timer SMI Status (Read Only):** SMI was caused by an ACPI Timer MSB toggle? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[0]. SMI generation configuration is at F0 Index 83h[5].
Note: Properly-configured means that the GPIO pin must be enabled as a GPIO (if multiplexed pin), an input, and to cause an SMI. This register provides status on several miscellaneous power management events that generate SMIs, as well as the status of the Lid Switch. It is called a Mirror register since an identical register exists at F0 Index F7h. Reading this register does not clear the status, while reading its counterpart at F0 Index F7h does clear the status.	
Index 88h	**General Purpose Timer 1 Count Register (R/W)** **Reset Value = 00h**
7:0	**General Purpose Timer 1 Count:** This register holds the load value for GP Timer 1. This value can represent either an 8-bit or 16-bit timer (selected at F0 Index 8Bh[4]). It is loaded into the timer when the timer is enabled (F0 Index 83h[0] =1). Once enabled, an enabled event (configured in F0 Index 89h[6:0]) reloads the timer. The timer is decremented with each clock of the configured timebase. Upon expiration of the timer, an SMI is generated and the top level SMI status is reported at F1BAR+Memory Offset 00h/02h[9]. The second level SMI status is reported at F1BAR+Memory Offset 04h/06h[0]). Once expired, this timer must be re-initialized by either disabling and enabling it, or writing a new count value here. This timer's timebase can be configured as 1 msec or 1 sec at F0 Index 89h[7].
Index 89h	**General Purpose Timer 1 Control Register (R/W)** **Reset Value = 00h**
7	**Timebase for General Purpose Timer 1:** Selects timebase for GP Timer 1 (F0 Index 88h). 0 = 1 sec; 1 = 1 msec.
6	**Re-trigger General Purpose Timer 1 on User Defined Device 3 (UDEF3) Activity:** 0 = Disable; 1 = Enable. Any access to the configured (memory or I/O) address range for UDEF3 reloads GP Timer 1. UDEF3 address programming is at F0 Index C8h (base address register) and CEh (control register).
5	**Re-trigger General Purpose Timer 1 on User Defined Device 2 (UDEF2) Activity:** 0 = Disable; 1 = Enable. Any access to the configured (memory or I/O) address range for UDEF2 reloads GP Timer 1. UDEF2 address programming is at F0 Index C4h (base address register) and CDh (control register).
4	**Re-trigger General Purpose Timer 1 on User Defined Device 1 (UDEF1) Activity:** 0 = Disable; 1 = Enable. Any access to the configured (memory or I/O) address range for UDEF1 reloads GP Timer 1. UDEF1 address programming is at F0 Index C0h (base address register) and CCh (control register)
3	**Re-trigger General Purpose Timer 1 on Keyboard or Mouse Activity:** 0 = Disable; 1 = Enable Any access to the keyboard or mouse I/O address range (listed below) reloads GP Timer 1. Keyboard Controller: I/O Ports 060h/064h COM1: I/O Port 3F8h-3FFh (if F0 Index 93h[1:0] = 10 this range is included) COM2: I/O Port 2F8h-2FFh (if F0 Index 93h[1:0] = 11 this range is included)

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
2	**Re-trigger General Purpose Timer 1 on Parallel/Serial Port Activity:** 0 = Disable; 1 = Enable. Any access to the parallel or serial port I/O address range (listed below) reloads the GP Timer 1. LPT1: I/O Port 378h-37Fh, 778h-77Ah LPT2: I/O Port 278h-27Fh, 678h-67Ah COM1: I/O Port 3F8h-3FFh (if F0 Index 93h[1:0] = 10 this range is excluded) COM2: I/O Port 2F8h-2FFh (if F0 Index 93h[1:0] = 11 this range is excluded) COM3: I/O Port 3E8h-3EFh COM4: I/O Port 2E8h-2EFh
1	**Re-trigger General Purpose Timer 1 on Floppy Disk Activity:** 0 = Disable; 1 = Enable. Any access to the floppy disk drive address ranges (listed below) reloads GP Timer 1. Primary floppy disk: I/O Port 3F2h, 3F4h, 3F5h, and 3F7 Secondary floppy disk: I/O Port 372h, 373h, 375h, and 377h The active floppy drive is configured via F0 Index 93h[7].
0	**Re-trigger General Purpose Timer 1 on Primary Hard Disk Activity:** 0 = Disable; 1 = Enable. Any access to the primary hard disk drive address range selected in F0 Index 93h[5] reloads GP Timer 1.
Index 8Ah	**General Purpose Timer 2 Count Register (R/W)** **Reset Value = 00h**
7:0	**General Purpose Timer 2 Count:** This register holds the load value for GP Timer 2. This value can represent either an 8-bit or 16-bit timer (configured in F0 Index 8Bh[5]). It is loaded into the timer when the timer is enabled (F0 Index 83h[1] = 1). Once the timer is enabled and a transition occurs on GPIO7, the timer is re-loaded. The timer is decremented with each clock of the configured timebase. Upon expiration of the timer, an SMI is generated and the top level of status is F1BAR+Memory Offset 00h/02h[9] and the second level of status is reported in F1BAR+Memory Offset 04h/06h[1]). Once expired, this timer must be re-initialized by either disabling and enabling it, or writing a new count value here. For GPIO7 to act as the reload for this timer, it must be enabled as such (F0 Index 8Bh[2]) and be configured as an input (F0 Index 90h[7]). This timer's timebase can be configured as 1 msec or 1 sec in F0 Index 8Bh[3].
Index 8Bh	**General Purpose Timer 2 Control Register (R/W)** **Reset Value = 00h**
7	**Re-trigger General Purpose Timer 1 on Secondary Hard Disk Activity:** 0 = Disable; 1 = Enable. Any access to the secondary hard disk drive address range selected in F0 Index 93h[4] reloads GP Timer 1.
6	**VGA Timer Base:** Selects timebase for VGA Timer Register (F0 Index 8Eh). 0 = 1 ms; 1 = 32 µs.
5	**General Purpose Timer 2 Shift:** GP Timer 2 is treated as an 8-bit or 16-bit timer. 0 = 8-bit; 1 = 16-bit. As an 8-bit timer, the count value is loaded into GP Timer 2 Count Register (F0 Index 8Ah). As a 16-bit timer, the value loaded into GP Timer 2 Count Register is shifted left by eight bits, the lower eight bits become zero, and this 16-bit value is used as the count for GP Timer 2.
4	**General Purpose Timer 1 Shift:** GP Timer 1 is treated as an 8-bit or 16-bit timer. 0 = 8-bit; 1 = 16-bit. As an 8-bit timer, the count value is that loaded into GP Timer 1 Count Register (F0 Index 88h). As a 16-bit timer, the value loaded into GP Timer 1 Count Register is shifted left by eight bit, the lower eight bits become zero, and this 16-bit value is used as the count for GP Timer 1.
3	**Timebase for General Purpose Timer 2:** Selects timebase for GP Timer 2 (F0 Index 8Ah). 0 = 1 sec; 1 = 1 msec.
2	**Re-trigger General Purpose Timer 2 on GPIO7 Pin Transition:** A configured transition on the GPIO7 pin reloads GP Timer 2 (F0 Index 8Ah). 0 = Disable; 1 = Enable. F0 Index 92h[7] selects whether a rising- or a falling-edge transition acts as a reload. For GPIO7 to work here, it must first be configured as an input (F0 Index 90h[7] = 0).
1:0	**Reserved:** Set to 0.
Index 8Ch	**IRQ Speedup Timer Count Register (R/W)** **Reset Value = 00h**
7:0	**IRQ Speedup Timer Count:** This register holds the load value for the IRQ speedup timer. It is loaded into the timer when Suspend Modulation is enabled (F0 Index 96h[0] = 1) and an INTR or an access to I/O Port 061h occurs. When the event occurs, the Suspend Modulation logic is inhibited, permitting full performance operation of the CPU. Upon expiration, no SMI is generated; the Suspend Modulation begins again. The IRQ speedup timer's timebase is 1 ms. This speedup mechanism allows instantaneous response to system interrupts for full-speed interrupt processing. A typical value here would be 2 to 4 ms.

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
Index 8Dh	**Video Speedup Timer Count Register (R/W)** **Reset Value = 00h**
7:0	**Video Speedup Timer Count:** This register holds the load value for the Video speedup timer. It is loaded into the timer when Suspend Modulation is enabled (F0 Index 96h[0] = 1) and any access to the graphics controller occurs. When a video access occurs, the Suspend Modulation logic is inhibited, permitting full-performance operation of the CPU. Upon expiration, no SMI is generated; the Suspend Modulation begins again. The video speedup timer's timebase is 1 ms. This speedup mechanism allows instantaneous response to video activity for full speed during video processing calculations. A typical value here would be 50 to 100 ms.
Index 8Eh	**VGA Timer Count Register (R/W)** **Reset Value = 00h**
7:0	**VGA Timer Load Value:** This register holds the load value for the VGA timer. The value is loaded into the timer when the timer is enabled (F0 Index 83h[3] = 1). The timer is decremented with each clock of the configured timebase (F0 Index 8Bh[6]). Upon expiration of the timer, an SMI is generated and the status is reported in F1BAR+Memory Offset 00h/02h[6] (only). Once expired, this timer must be re-initialized by disabling it (F0 Index 83h[3] = 0) and then enabling it (F0 Index 83h[3] = 1). When the count value is changed in this register, the timer must be re-initialized in order for the new value to be loaded. This timer's timebase is selectable as 1 ms (default) or 32 µs. (F0 Index 8Bh). **Note:** Although grouped with the power management Idle Timers, the VGA Timer is not a power management function. It is not affected by the Global Power Management Enable setting at F0 Index 80h[0].
Index 8Fh	**Reserved** **Reset Value = xxh**
Index 90h	**GPIO Pin Direction Register 1 (R/W)** **Reset Value = 00h**
7	**GPIO7 Direction:** Selects if GPIO7 is an input or output. 0 = Input; 1 = Output.
6	**GPIO6 Direction:** Selects if GPIO6 is an input or output. 0 = Input; 1 = Output.
5	**GPIO5 Direction:** Selects if GPIO5 is an input or output. 0 = Input; 1 = Output.
4	**GPIO4 Direction:** Selects if GPIO4 is an input or output. 0 = Input; 1 = Output.
3	**GPIO3 Direction:** Selects if GPIO3 is an input or output. 0 = Input; 1 = Output.
2	**GPIO2 Direction:** Selects if GPIO2 is an input or output. 0 = Input; 1 = Output.
1	**GPIO1 Direction:** Selects if GPIO1 is an input or output. 0 = Input; 1 = Output.
0	**GPIO0 Direction:** Selects if GPIO0 is an input or output. 0 = Input; 1 = Output.
Note: Several of these pins have specific alternate functions. The direction configured here must be consistent with the pins' use as the alternate function.	
Index 91h	**GPIO Pin Data Register 1 (R/W)** **Reset Value = 00h**
7	**GPIO7 Data:** Reflects the level of GPIO7. 0 = Low; 1 = High.
6	**GPIO6 Data:** Reflects the level of GPIO6. 0 = Low; 1 = High.
5	**GPIO5 Data:** Reflects the level of GPIO5. 0 = Low; 1 = High.
4	**GPIO4 Data:** Reflects the level of GPIO4. 0 = Low; 1 = High.
3	**GPIO3 Data:** Reflects the level of GPIO3. 0 = Low; 1 = High.
2	**GPIO2 Data:** Reflects the level of GPIO2. 0 = Low; 1 = High.
1	**GPIO1 Data:** Reflects the level of GPIO1. 0 = Low; 1 = High.
0	**GPIO0 Data:** Reflects the level of GPIO0. 0 = Low; 1 = High.
Note: This register contains the direct values of GPIO[7:0] pins. Write operations are valid only for bits defined as output. Reads from this register read the last written value if the pin is an output. The pins are configured as inputs or outputs in F0 Index 90h.	
Index 92h	**GPIO Control Register 1 (R/W)** **Reset Value = 00h**
7	**GPIO7 Edge Sense for Reload of General Purpose Timer 2:** Selects which edge transition of GPIO7 causes GP Timer 2 to reload. 0 = Rising; 1 = Falling (Note 2).
6	**GPIO6 Enabled as Lid Switch:** Allow GPIO6 to act as the lid switch input. 0 = GPIO6; 1 = Lid switch. When enabled, every transition of the GPIO6 pin causes the lid switch status to toggle and generate an SMI. The top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 87h/F7h[3]. If GPIO6 is enabled as the lid switch, F0 Index 87h/F7h[4] reports the current status of the lid's position.
5	**GPIO2 Edge Sense for SMI:** Selects which edge transition of the GPIO2 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 2 must be set to enable this bit.

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
4	**GPIO1 Edge Sense for SMI:** Selects which edge transition of the GPIO1 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 1 must be set to enable this bit.
3	**GPIO0 Edge Sense for SMI:** Selects which edge transition of the GPIO0 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 1 must be set to enable this bit.
2	**Enable GPIO2 as an External SMI Source:** Allow GPIO2 to be an external SMI source and generate an SMI on either a rising or falling edge transition (depends upon setting of bit 5). 0 = Disable; 1 = Enable (Note 3). Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 87h/F7h[7].
1	**Enable GPIO1 as an External SMI Source:** Allow GPIO1 to be an external SMI source and generate an SMI on either a rising- or falling-edge transition (depends upon setting of bit 4). 0 = Disable; 1 = Enable (Note 3). Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 87h/F7h[6].
0	**Enable GPIO0 as an External SMI Source:** Allow GPIO0 to be an external SMI source and generate an SMI on either a rising or falling edge transition (depends upon setting of bit 3). 0 = Disable; 1 = Enable (Note 3) Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 87h/F7h[5].
Notes: 1) For any of the above bits to function properly, the respective GPIO pin must be configured as an input (F0 Index 90h). 2) GPIO7 can generate an SMI (F0 Index 97h[3]) or re-trigger General Purpose Timer 2 (F0 Index 8Bh[2]) or both. 3) If GPIO[2:0] are enabled as external SMI sources, they are the only GPIOs that can be used as SMI sources to wake-up the system from Suspend when the clocks are stopped.	
Index 93h	**Miscellaneous Device Control Register (R/W)** **Reset Value = 00h**
7	**Floppy Drive Port Select:** All system resources used to power manage the floppy drive use the primary or secondary FDC addresses for decode. 0 = Primary; 1 = Primary and Secondary.
6	**Reserved:** This bit must always be set to 1.
5	**Partial Primary Hard Disk Decode:** This bit is used to restrict the addresses which are decoded as primary hard disk accesses. 0 = Power management monitors all reads and writes I/O Port 1F0h-1F7h, 3F6h 1 = Power management monitors only writes to I/O Port 1F6h and 1F7h
4	**Partial Secondary Hard Disk Decode:** This bit is used to restrict the addresses which are decoded as secondary hard Disk accesses. 0 = Power management monitors all reads and writes I/O Port 170h-177h, 376h 1 = Power management monitors only writes to I/O Port 176h and 177h
3:2	**Reserved:** Set to 0.
1	**Mouse on Serial Enable:** Mouse is present on a serial port. 0 = No; 1 = Yes. (Note)
0	**Mouse Port Select:** Selects which serial port the mouse is attached to. 0 = COM1; 1 = COM2. (Note)
Note: Bits 1 and 0 - If a mouse is attached to a serial port (bit 1 = 1), that port is removed from the serial device list being used to monitor serial port access for power management purposes and added to the keyboard/mouse decode. This is done because a mouse, along with the keyboard, is considered an input device and is used only to determine when to blank the screen. These bits determine the decode used for the Keyboard/Mouse Idle Timer Count Register (F0 Index 9Eh) as well as the Parallel/ Serial Port Idle Timer Count Register (F0 Index 9Ch).	
Index 94h	**Suspend Modulation OFF Count Register (R/W)** **Reset Value = 00h**
7:0	**Suspend Signal Deasserted Count:** This 8-bit value represents the number of 32 µs intervals that the SUSP# pin will be deasserted to the GX1 processor. This timer, together with the Suspend Modulation ON Count Register (F0 Index 95h), perform the Suspend Modulation function for CPU power management. The ratio of the on-to-off count sets up an effective (emulated) clock frequency, allowing the power manager to reduce CPU power consumption. This timer is prematurely reset if an enabled speedup event occurs. The speedup events are IRQ speedups and video speedups.
Index 95h	**Suspend Modulation ON Count Register (R/W)** **Reset Value = 00h**
7:0	**Suspend Signal Asserted Count:** This 8-bit value represents the number of 32 µs intervals that the SUSP# pin will be asserted. This timer, together with the Suspend Modulation OFF Count Register (F0 Index 94h), perform the Suspend Modulation function for CPU power management. The ratio of the on-to-off count sets up an effective (emulated) clock frequency, allowing the power manager to reduce CPU power consumption. This timer is prematurely reset if an enabled speedup event occurs. The speedup events are IRQ speedups and video speedups.

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
Index 96h	**Suspend Configuration Register (R/W)** **Reset Value = 00h**
7:5	**Reserved:** Set to 0.
4	**Power Savings Mode:** 0 = Enable; 1 = Disable.
3	**Include ISA Clock in Power Savings Mode:** 0 = ISA clock not included; 1 = ISA clock included.
2	**Suspend Mode Configuration:** "Special 3 Volt Suspend" mode to support powering down the GX1 processor during Suspend. 0 = Disable; 1 = Enable.
1	**SMI Speedup Configuration:** Selects how Suspend Modulation function reacts when an SMI occurs. 0 = Use the IRQ Speedup Timer Count Register (F0 Index 8Ch) to temporarily disable Suspend Modulation when an SMI occurs. 1 = Disable Suspend Modulation when an SMI occurs until a read to the SMI Speedup Disable Register (F1BAR+Memory Offset 08h). The purpose of this bit is to disable Suspend Modulation while the CPU is in the System Management Mode so that VSA technology and power management operations occur at full speed. Two methods for accomplishing this are either to map the SMI into the IRQ Speedup Timer Count Register (F0 Index 8Ch), or to have the SMI disable Suspend Modulation until the SMI handler reads the SMI Speedup Disable Register (F1BAR+Memory Offset 08h). The latter is the preferred method. The IRQ speedup method is provided for software compatibility with earlier revisions of the CS5530A. This bit has no effect if the Suspend Modulation feature is disabled (bit 0 = 0).
0	**Suspend Modulation Feature:** 0 = Disable; 1 = Enable. When enabled, the SUSP# pin will be asserted and deasserted for the durations programmed in the Suspend Modulation OFF/ON Count Registers (F0 Index 94h/95h).
Index 97h	**GPIO Control Register 2 (R/W)** **Reset Value = 00h**
7	**GPIO7 Edge Sense for SMI:** Selects which edge transition of the GPIO7 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 3 must be set to enable this bit.
6	**GPIO5 Edge Sense for SMI:** Selects which edge transition of the GPIO5 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 2 must be set to enable this bit.
5	**GPIO4 Edge Sense for SMI:** Selects which edge transition of the GPIO4 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 1 must be set to enable this bit.
4	**GPIO3 Edge Sense for SMI:** Selects which edge transition of the GPIO3 pin generates an SMI. 0 = Rising; 1 = Falling. Bit 0 must be set to enable this bit.
3	**Enable GPIO7 as an External SMI Source:** Allow GPIO7 to be an external SMI source and to generate an SMI on either a rising or falling edge transition (depends upon setting of bit 7). 0 = Disable; 1 = Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 84h/F4h[3].
2	**Enable GPIO5 as an External SMI Source:** Allow GPIO5 to be an external SMI source and to generate an SMI on either a rising or falling edge transition (depends upon setting of bit 6). 0 = Disable; 1 = Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 84h/F4h[2].
1	**Enable GPIO4 as an External SMI Source:** Allow GPIO4 to be an external SMI source and to generate an SMI on either a rising- or falling-edge transition (depends upon setting of bit 5). 0 = Disable; 1 = Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 84h/F4h[1].
0	**Enable GPIO3 as an External SMI Source:** Allow GPIO3 to be an external SMI source and to generate an SMI on either a rising or falling edge transition (depends upon setting of bit 4) 0 = Disable; 1 = Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status reporting is at F0 Index 84h/F4h[0].
Note: For any of the above bits to function properly, the respective GPIO pin must be configured as an input (F0 Index 90h).	

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
Index 98h-99h	**Primary Hard Disk Idle Timer Count Register (R/W)** — **Reset Value = 0000h**
15:0	**Primary Hard Disk Idle Timer Count:** The idle timer loaded from this register is used to determine when the primary hard disk is not in use so that it can be powered down. The 16-bit value programmed here represents the period of primary hard disk inactivity after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to the configured primary hard disk's data port (configured in F0 Index 93h[5]). The timer uses a 1 second timebase. To enable this timer set F0 Index 81h[0] = 1. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[0].
Index 9Ah-9Bh	**Floppy Disk Idle Timer Count Register (R/W)** — **Reset Value = 0000h**
15:0	**Floppy Disk Idle Timer Count:** The idle timer loaded from this register is used to determine when the floppy disk drive is not in use so that it can be powered down. The 16-bit value programmed here represents the period of floppy disk drive inactivity after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to any of I/O Ports 3F2h, 3F4h, 3F5h, and 3F7h (primary) or 372h, 374h, 375h, and 377h (secondary). The timer uses a 1 second timebase. To enable this timer set F0 Index 81h[1] = 1. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[1].
Index 9Ch-9Dh	**Parallel / Serial Idle Timer Count Register (R/W)** — **Reset Value = 0000h**
15:0	**Parallel / Serial Idle Timer Count:** The idle timer loaded from this register is used to determine when the parallel and serial ports are not in use so that the ports can be power managed. The 16-bit value programmed here represents the period of inactivity for these ports after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to the parallel (LPT) or serial (COM) I/O address spaces. If the mouse is enabled on a serial port, that port is not considered here. The timer uses a 1 second timebase. To enable this timer set F0 Index 81h[2] = 1. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[2].
Index 9Eh-9Fh	**Keyboard / Mouse Idle Timer Count Register (R/W)** — **Reset Value = 0000h**
15:0	**Keyboard / Mouse Idle Timer Count:** The idle timer loaded from this register determines when the keyboard and mouse are not in use so that the LCD screen can be blanked. The 16-bit value programmed here represents the period of inactivity for these ports after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to either the keyboard or mouse I/O address spaces, including the mouse serial port address space when a mouse is enabled on a serial port. The timer uses a 1 second timebase. To enable this timer set F0 Index 81h[3] = 1. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[3].
Index A0h-A1h	**User Defined Device 1 Idle Timer Count Register (R/W)** — **Reset Value = 0000h**
15:0	**User Defined Device 1 (UDEF1) Idle Timer Count:** The idle timer loaded from this register determines when the device configured as UDEF1 is not in use so that it can be power managed. The 16-bit value programmed here represents the period of inactivity for this device after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to memory or I/O address space configured at F0 Index C0h (base address register) and F0 Index CCh (control register). The timer uses a 1 second timebase. To enable this timer set F0 Index 81h[4] = 1. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[4].
Index A2h-A3h	**User Defined Device 2 Idle Timer Count Register (R/W)** — **Reset Value = 0000h**
15:0	**User Defined Device 2 (UDEF2) Idle Timer Count:** The idle timer loaded from this register determines when the device configured as UDEF2 is not in use so that it can be power managed. The 16-bit value programmed here represents the period of inactivity for this device after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to memory or I/O address space configured at F0 Index C4h (base address register) and F0 Index CDh (control register). The timer uses a 1 second timebase. To enable this timer set F0 Index 81h[5] = 1. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[5].

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
Index A4h-A5h	**User Defined Device 3 Idle Timer Count Register (R/W)** — **Reset Value = 0000h**
15:0	**User Defined Device 3 (UDEF3) Idle Timer Count:** The idle timer loaded from this register determines when the device configured as UDEF3 is not in use so that it can be power managed. The 16-bit value programmed here represents the period of inactivity for this device after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to memory or I/O address space configured at F0 Index C8h (base address register) and F0 Index CEh (control register). The timer uses a 1 second timebase. To enable this timer set F0 Index 81h[6] = 1. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[6].
Index A6h-A7h	**Video Idle Timer Count Register (R/W)** — **Reset Value = 0000h**
15:0	**Video Idle Timer Count:** The idle timer loaded from this register determines when the graphics subsystem has been idle as part of the Suspend determination algorithm. The 16-bit value programmed here represents the period of video inactivity after which the system is alerted via an SMI. The count in this timer is automatically reset whenever an access occurs to the graphics controller space. The timer uses a 1 second timebase. In a GX1 processor based system the graphics controller is embedded in the CPU, so video activity is communicated to the CS5530A via the serial connection (PSERIAL register, bit 0) from the processor. The CS5530A also detects accesses to standard VGA space on PCI (3Bxh, 3Cxh, 3Dxh and A000h-B7FFh) in the event an external VGA controller is being used. To enable this timer set F0 Index 81h[7] = 1. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 85h/F5h[7].
Index A8h-A9h	**Video Overflow Count Register (R/W)** — **Reset Value = 0000h**
15:0	**Video Overflow Count:** Each time the Video Speedup timer (F0 Index 8Dh) is triggered, a 100 ms timer is started. If the 100 ms timer expires before the Video Speedup timer lapses, the Video Overflow Count Register increments and the 100 ms timer re-triggers. Software clears the overflow register when new evaluations are to begin. The count contained in this register may be combined with other data to determine the type of video accesses present in the system.
Index AAh-ABh	**Reserved** — **Reset Value = xxh**
Index ACh-ADh	**Secondary Hard Disk Idle Timer Count Register (R/W)** — **Reset Value = 0000h**
15:0	**Secondary Hard Disk Idle Timer Count:** The idle timer loaded from this register is used to determine when the secondary hard disk is not in use so that it can be powered down. The 16-bit value programmed here represents the period of secondary hard disk inactivity after which the system is alerted via an SMI. The timer is automatically reloaded with the count value whenever an access occurs to the configured secondary hard disk's data port (configured in F0 Index 93h[4]). The timer uses a 1 second timebase. To enable this timer set F0 Index 83h[7] = 1. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 86h/F6h[4].
Index AEh	**CPU Suspend Command Register (WO)** — **Reset Value = 00h**
7:0	**Software CPU Suspend Command (Write Only):** If bit 0 in the Clock Stop Control Register is set low (F0 Index BCh[0] = 0) and all SMI status bits are 0, a write to this register causes a SUSP#/SUSPA# handshake with the CPU, placing the CPU in a low-power state. The data written is irrelevant. Once in this state, any unmasked IRQ or SMI releases the CPU halt condition. If F0 Index BCh[0] = 1, writing to this register invokes a full system Suspend. In this case, the SUSP_3V pin is asserted after the SUSP#/SUSPA# halt. Upon a Resume event (see Note), the PLL delay programmed in the F0 Index BCh[7:4] is invoked, allowing the clock chip and CPU PLL to stabilize before deasserting the SUSP# pin. **Note:** If the clocks are stopped, the external IRQ4 and IRQ3 pins, when enabled (F3BAR+Memory Offset 1Ah[4:3]), are the only IRQ pins that can be used as a Resume event. If GPIO2, GPIO1, and GPIO0 are enabled as an external SMI source (F0 Index 92h[2:0]), they too can be used as a Resume event. No other CS5530A pins can be used to wake-up the system from Suspend when the clocks are stopped. As long as the 32 KHz clock remains active, internal SMI events are also Resume events.

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
Index AFh	**Suspend Notebook Command Register (WO)** **Reset Value = 00h**
7:0	**Software CPU Stop Clock Suspend (Write Only):** A write to this register causes a SUSP#/SUSPA# handshake with the CPU, placing the CPU in a low-power state. Following this handshake, the SUSP_3V pin is asserted. The SUSP_3V pin is intended to be used to stop all system clocks. Upon a Resume event (see Note), the SUSP_3V pin is deasserted. After a slight delay, the CS5530A deasserts the SUSP# signal. Once the clocks are stable, the processor deasserts SUSPA# and system operation resumes. **Note:** If the clocks are stopped the external IRQ4 and IRQ3 pins, when enabled (F3BAR+Memory Offset 1Ah[4:3]), are the only IRQ pins that can be used as a Resume event. If GPIO2, GPIO1, and GPIO0 are enabled as an external SMI source (F0 Index 92h[2:0]), they too can be used as a Resume event. No other CS5530A pins can be used to wake-up the system from Suspend when the clocks are stopped.
Index B0h-B3h	**Reserved** **Reset Value = xxh**
Index B4h	**Floppy Port 3F2h Shadow Register (RO)** **Reset Value = xxh**
7:0	**Floppy Port 3F2h Shadow (Read Only):** Last written value of I/O Port 3F2h. Required for support of FDC power ON/OFF and Save-to-Disk/RAM coherency. This register is a copy of an I/O register which cannot safely be directly read. Value in register is not deterministic of when the register is being read. It is provided here to assist in a Save-to-Disk operation.
Index B5h	**Floppy Port 3F7h Shadow Register (RO)** **Reset Value = xxh**
7:0	**Floppy Port 3F7h Shadow (Read Only):** Last written value of I/O Port 3F7h. Required for support of FDC power ON/OFF and Save-to-Disk/RAM coherency. This register is a copy of an I/O register which cannot safely be directly read. Value in register is not deterministic of when the register is being read. It is provided here to assist in a Save-to-Disk operation.
Index B6h	**Floppy Port 1F2h Shadow Register (RO)** **Reset Value = xxh**
7:0	**Floppy Port 1F2h Shadow (Read Only):** Last written value of I/O Port 1F2h. Required for support of FDC power ON/OFF and Save-to-Disk/RAM coherency. This register is a copy of an I/O register which cannot safely be directly read. Value in register is not deterministic of when the register is being read. It is provided here to assist in a Save-to-Disk operation.
Index B7h	**Floppy Port 1F7h Shadow Register (RO)** **Reset Value = xxh**
7:0	**Floppy Port 1F7h Shadow (Read Only):** Last written value of I/O Port 1F7h. Required for support of FDC power ON/OFF and Save-to-Disk/RAM coherency. This register is a copy of an I/O register which cannot safely be directly read. Value in register is not deterministic of when the register is being read. It is provided here to assist in a Save-to-Disk operation.
Index B8h	**DMA Shadow Register (RO)** **Reset Value = xxh**
7:0	**DMA Shadow (Read Only):** This 8-bit port sequences through the following list of shadowed DMA Controller registers. At power on, a pointer starts at the first register in the list and consecutively reads incrementally through it. A write to this register resets the read sequence to the first register. Each shadow register in the sequence contains the last data written to that location. The read sequence for this register is: 1. DMA Channel 0 Mode Register 2. DMA Channel 1 Mode Register 3. DMA Channel 2 Mode Register 4. DMA Channel 3 Mode Register 5. DMA Channel 4 Mode Register 6. DMA Channel 5 Mode Register 7. DMA Channel 6 Mode Register 8. DMA Channel 7 Mode Register 9. DMA Channel Mask Register (bit 0 is channel 0 mask, etc.) 10. DMA Busy Register (bit 0 or 1 means a DMA occurred within last 1 ms, all other bits are 0)

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
Index B9h	**PIC Shadow Register (RO)** — **Reset Value = xxh**
7:0	**PIC Shadow (Read Only):** This 8-bit port sequences through the following list of shadowed Programmable Interrupt Controller registers. At power on, a pointer starts at the first register in the list and consecutively reads incrementally through it. A write to this register resets the read sequence to the first register. Each shadow register in the sequence contains the last data written to that location. The read sequence for this register is: 1. PIC1 ICW1 2. PIC1 ICW2 3. PIC1 ICW3 4. PIC1 ICW4 - Bits [7:5] of ICW4 are always 0 5. PIC1 OCW2 - Bits [6:3] of OCW2 are always 0 (Note) 6. PIC1 OCW3 - Bits [7, 4] are 0 and bit [6, 3] are 1 7. PIC2 ICW1 8. PIC2 ICW2 9. PIC2 ICW3 10. PIC2 ICW4 - Bits [7:5] of ICW4 are always 0 11. PIC2 OCW2 - Bits [6:3] of OCW2 are always 0 (Note) 12. PIC2 OCW3 - Bits [7, 4] are 0 and bit [6, 3] are 1 **Note:** To restore OCW2 to shadow register value, write the appropriate address twice. First with the shadow register value, then with the shadow register value ORed with C0h.
Index BAh	**PIT Shadow Register (RO)** — **Reset Value = xxh**
7:0	**PIT Shadow (Read Only):** This 8-bit port sequences through the following list of shadowed Programmable Interval Timer registers. At power on, a pointer starts at the first register in the list and consecutively reads to increment through it. A write to this register resets the read sequence to the first register. Each shadow register in the sequence contains the last data written to that location. The read sequence for this register is: 1. Counter 0 LSB (least significant byte) 2. Counter 0 MSB 3. Counter 1 LSB 4. Counter 1 MSB 5. Counter 2 LSB 6. Counter 2 MSB 7. Counter 0 Command Word 8. Counter 1 Command Word 9. Counter 2 Command Word **Note:** The LSB/MSB of the count is the Counter base value, not the current value. Bits [7:6] of the command words are not used.
Index BBh	**RTC Index Shadow Register (RO)** — **Reset Value = xxh**
7:0	**RTC Index Shadow (Read Only):** The RTC Shadow register contains the last written value of the RTC Index register (I/O Port 070h).
Index BCh	**Clock Stop Control Register (R/W)** — **Reset Value = 00h**
7:4	**PLL Delay:** The programmed value in this field sets the delay (in milliseconds) after a break event occurs before the SUSP# pin is deasserted to the CPU. This delay is designed to allow the clock chip and CPU PLL to stabilize before starting execution. This delay is only invoked if the STP_CLK bit (bit 0) was set. The four-bit field allows values from 0 to 15 ms. 0000 = 0 ms, 0100 = 4 ms, 1000 = 8 ms, 1100 = 12 ms 0001 = 1 ms, 0101 = 5 ms, 1001 = 9 ms, 1101 = 13 ms 0010 = 2 ms, 0110 = 6 ms, 1010 = 10 ms, 1110 = 14 ms 0011 = 3 ms, 0111 = 7 ms, 1011 = 11 ms, 1111 = 15 ms
3:1	**Reserved:** Set to 0.

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
0	**CPU Clock Stop:** 0 = Normal SUSP#/ SUSPA# handshake; 1 = Full system Suspend.
Note:	This register configures the CS5530A to support a 3 Volt Suspend. Setting bit 0 causes the SUSP_3V pin to assert after the appropriate conditions, stopping the system clocks. A delay of 0 to 15 ms is programmable (bits 7:4) to allow for a delay for the clock chip and CPU PLL to stabilize when an event Resumes the system. A write to the CPU Suspend Command Register (F0 Index AEh) with bit 0 written as: 0 = SUSP#/SUSPA# handshake occurs. The CPU is put into a low-power state, and the system clocks are not stopped. When a break/resume event occurs, it releases the CPU halt condition. 1 = SUSP#/SUSPA# handshake occurs and the SUSP_3V pin is asserted, thus invoking a full system Suspend (both CPU and system clocks are stopped). When a break event occurs, the SUSP_3V pin will deassert, the PLL delay programmed in bits [7:4] will be invoked which allows the clock chip and CPU PLL to stabilize before deasserting the SUSP# pin.
Index BDh-BFh	**Reserved** — **Reset Value = xxh**
Index C0h-C3h	**User Defined Device 1 Base Address Register (R/W)** — **Reset Value = 00000000h**
31:0	**User Defined Device 1 (UDEF1) Base Address [31:0]:** This 32-bit register supports power management (trap and idle timer resources) for a PCMCIA slot or some other device in the system. The value written is used as the address comparator for the device trap/timer logic. The device can be memory or I/O mapped (configured in F0 Index CCh).
Index C4h-C7h	**User Defined Device 2 Base Address Register (R/W)** — **Reset Value = 00000000h**
31:0	**User Defined Device 2 (UDEF2) Base Address [31:0]:** This 32-bit register supports power management (trap and idle timer resources) for a PCMCIA slot or some other device in the system. The value written is used as the address comparator for the device trap/timer logic. The device can be memory or I/O mapped (configured in F0 Index CDh).
Index C8h-CBh	**User Defined Device 3 Base Address Register (R/W)** — **Reset Value = 00000000h**
31:0	**User Defined Device 3 (UDEF3) Base Address [31:0]:** This 32-bit register supports power management (trap and idle timer resources) for a PCMCIA slot or some other device in the system. The value written is used as the address comparator for the device trap/timer logic. The device can be memory or I/O mapped (configured in F0 Index CEh).
Index CCh	**User Defined Device 1 Control Register (R/W)** — **Reset Value = 00h**
7	**Memory or I/O Mapped:** User Defined Device 1 is: 0 = I/O; 1 = Memory.
6:0	**Mask** If bit 7 = 0 (I/O): Bit 6 0 = Disable write cycle tracking 1 = Enable write cycle tracking Bit 5 0 = Disable read cycle tracking 1 = Enable read cycle tracking Bits 4:0 Mask for address bits A[4:0] If bit 7 = 1 (M/IO): Bits 6:0 Mask for address memory bits A[15:9] (512 bytes min. and 64 KB max.) and A[8:0] are ignored. **Note:** A “1” in a mask bit means that the address bit is ignored for comparison.
Index CDh	**User Defined Device 2 Control Register (R/W)** — **Reset Value = 00h**
7	**Memory or I/O Mapped:** User Defined Device 2 is: 0 = I/O; 1 = Memory.
6:0	**Mask** If bit 7 = 0 (I/O): Bit 6 0 = Disable write cycle tracking 1 = Enable write cycle tracking Bit 5 0 = Disable read cycle tracking 1 = Enable read cycle tracking Bits 4:0 Mask for address bits A[4:0] If bit 7 = 1 (M/IO): Bits 6:0 Mask for address memory bits A[15:9] (512 bytes min. and 64 KB max.) and A[8:0] are ignored. **Note:** A “1” in a mask bit means that the address bit is ignored for comparison.
Index CEh	**User Defined Device 3 Control Register (R/W)** — **Reset Value = 00h**
7	**Memory or I/O Mapped:** User Defined Device 3 is: 0 = I/O; 1 = Memory.

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
6:0	**Mask** If bit 7 = 0 (I/O): Bit 6 0 = Disable write cycle tracking 1 = Enable write cycle tracking Bit 5 0 = Disable read cycle tracking 1 = Enable read cycle tracking Bits 4:0 Mask for address bits A[4:0] If bit 7 = 1 (M/IO): Bits 6:0 Mask for address memory bits A[15:9] (512 bytes min. and 64 KB max.) and A[8:0] are ignored. **Note:** A "1" in a mask bit means that the address bit is ignored for comparison.
Index CFh	**Reserved** **Reset Value = xxh**
Index D0h	**Software SMI Register (WO)** **Reset Value = 00h**
7:0	**Software SMI (Write Only):** A write to this location generates an SMI. The data written is irrelevant. This register allows software entry into SMM via normal bus access instructions.
Index D1h-EBh	**Reserved** **Reset Value = xxh**
Index ECh	**Timer Test Register (R/W)** **Reset Value = 00h**
7:0	**Timer Test Value:** The Timer Test Register is intended only for test and debug purposes. It is not intended for setting operational timebases.
Index EDh-F3h	**Reserved** **Reset Value = xxh**
Index F4h	**Second Level Power Management Status Register 1 (RC)** **Reset Value = 00h**
7:5	**Reserved**
4	**Game Port SMI Status (Read to Clear):** SMI was caused by a R/W access to game port (I/O Port 200h and 201h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. Game Port Read SMI generation enabling is at F0 Index 83h[4]. Game Port Write SMI generation enabling is at F0 Index 53h[3].
3	**GPIO7 SMI Status (Read to Clear):** SMI was caused by transition on (properly-configured) GPIO7 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 97h[3].
2	**GPIO5 SMI Status (Read to Clear):** SMI was caused by transition on (properly-configured) GPIO5 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 97h[2].
1	**GPIO4 SMI Status (Read to Clear):** SMI was caused by transition on (properly-configured) GPIO4 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 97h[1].
0	**GPIO3 SMI Status (Read to Clear):** SMI was caused by transition on (properly-configured) GPIO3 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 97h[0].
Note: Properly-configured means that the GPIO pin must be enabled as a GPIO, an input, and to cause an SMI. This register provides status on various power-management SMI events. Reading this register clears the SMI status bits. A read-only (mirror) version of this register exists at F0 Index 84h.	
Index F5h	**Second Level Power Management Status Register 2 (RC)** **Reset Value = 00h**
7	**Video Idle Timer SMI Status (Read to Clear):** SMI was caused by expiration of the Video Idle Timer Count Register (F0 Index A6h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[7].
6	**User Defined Device 3 (UDEF3) Idle Timer SMI Status (Read to Clear):** SMI was caused by expiration of the UDEF3 Idle Timer Count Register (F0 Index A4h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[6].

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
5	**User Defined Device 2 (UDEF2) Idle Timer SMI Status (Read to Clear):** SMI was caused by expiration of the UDEF2 Idle Timer Count Register (F0 Index A2h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[5].
4	**User Defined Device 1 (UDEF1) Idle Timer SMI Status (Read to Clear):** SMI was caused by expiration of the UDEF1 Idle Timer Count Register (F0 Index A0h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[4].
3	**Keyboard/Mouse Idle Timer SMI Status (Read to Clear):** SMI was caused by expiration of the Keyboard/Mouse Idle Timer Count Register (F0 Index 9Eh)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[3].
2	**Parallel/Serial Idle Timer SMI Status (Read to Clear):** SMI was caused by expiration of the Parallel/Serial Port Idle Timer Count Register (F0 Index 9Ch)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[2].
1	**Floppy Disk Idle Timer SMI Status (Read to Clear):** SMI was caused by expiration of the Floppy Disk Idle Timer Count Register (F0 Index 9Ah)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[1].
0	**Primary Hard Disk Idle Timer SMI Status (Read to Clear):** SMI was caused by expiration of the Primary Hard Disk Idle Timer Count Register (F0 Index 98h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 81h[0].
Note: This register provides status on the Device Idle Timers to the SMI handler. A bit set here indicates that the device was idle for the duration configured in the Idle Timer Count register for that device, causing an SMI. Reading this register clears the SMI status bits. A read-only (mirror) version of this register exists at F0 Index 85h. If the value of the register must be read without clearing the SMI source (and consequently deasserting SMI), F0 Index 85h may be read instead.	
Index F6h	**Second Level Power Management Status Register 3 (RC)** **Reset Value = 00h**
7	**Video Access Trap SMI Status (Read to Clear):** SMI was caused by a trapped I/O access to the Video I/O Trap? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 82h[7].
6	**Reserved (Read Only)**
5	**Secondary Hard Disk Access Trap SMI Status (Read to Clear):** SMI was caused by a trapped I/O access to the secondary hard disk? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 83h[6].
4	**Secondary Hard Disk Idle Timer SMI Status (Read to Clear):** SMI was caused by expiration of the Hard Disk Idle Timer Count Register (F0 Index ACh)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 83h[7].
3	**Keyboard/Mouse Access Trap SMI Status (Read to Clear):** SMI was caused by a trapped I/O access to the keyboard or mouse? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 82h[3].
2	**Parallel/Serial Access Trap SMI Status (Read to Clear):** SMI was caused by a trapped I/O access to either the serial or parallel ports? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 82h[2].
1	**Floppy Disk Access Trap SMI Status (Read to Clear):** SMI was caused by a trapped I/O access to the floppy disk? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 82h[1].

Table 5-15. F0 Index xxh: PCI Header and Bridge Configuration Registers (Continued)

Bit	Description
0	**Primary Hard Disk Access Trap SMI Status (Read to Clear):** SMI was caused by a trapped I/O access to the primary hard disk? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 82h[0].
Note: This register provides status on the Device Traps to the SMI handler. A bit set here indicates that an access occurred to the device while the trap was enabled, causing an SMI. Reading this register clears the SMI status bits. A read-only (mirror) version of this register exists at F0 Index 86h. If the value of the register must be read without clearing the SMI source (and consequently deasserting SMI), F0 Index 86h may be read instead.	
Index F7h	**Second Level Power Management Status Register 4 (RO/RC)** **Reset Value = 00h**
7	**GPIO2 SMI Status (Read to Clear):** SMI was caused by transition on (properly-configured) GPIO2 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 92h[2].
6	**GPIO1 SMI Status (Read to Clear):** SMI was caused by transition on (properly-configured) GPIO1 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 92h[1].
5	**GPIO0 SMI Status (Read to Clear):** SMI was caused by transition on (properly-configured) GPIO0 pin? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 92h[0].
4	**Lid Position (Read Only):** This bit maintains the current status of the lid position. If the GPIO6 pin is configured as the lid switch indicator, this bit reflects the state of the pin.
3	**Lid Switch SMI Status (Read to Clear):** SMI was caused by a transition on the GPIO6 (lid switch) pin? 0 = No; 1 = Yes. For this to happen, the GPIO6 pin must be configured both as an input (F0 Index 90h[6] = 0) and as the lid switch (F0 Index 92h[6] =1).
2	**Codec SDATA_IN SMI Status (Read to Clear):** SMI was caused by an AC97 codec producing a positive edge on SDATA_IN? 0 = No; 1 = Yes. This is the second level of status is reporting. The top level status is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation enabling is at F0 Index 80h[5].
1	**RTC Alarm (IRQ8) SMI Status (Read to Clear):** SMI was caused by an RTC interrupt? 0 = No; 1 = Yes. This SMI event can only occur while in 3V Suspend and RTC interrupt occurs. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0].
0	**ACPI Timer SMI Status (Read to Clear):** SMI was caused by an ACPI Timer MSB toggle? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[0]. SMI generation configuration is at F0 Index 83h[5].
Note: Properly-configured means that the GPIO pin must be enabled as a GPIO, an input, and to cause an SMI. This register provides status on several miscellaneous power management events that generate SMIs, as well as the status of the Lid Switch. Reading this register clears the SMI status bits. A read-only (mirror) version of this register exists at F0 Index 87h.	
Index F8h-FFh	**Reserved** **Reset Value = xxh**

5.3.2 SMI Status and ACPI Timer Registers - Function 1

The register space for the SMI status and ACPI Timer registers is divided into two sections. The first section is used to configure the PCI portion of this support hardware. A Base Address Register at F1 Index 10h (F1BAR) points to the base address of where the second portion of the register space is located. This second section contains the SMI status and ACPI timer support registers.

Note: The ACPI Timer Count Register is accessible through F1BAR+Memory Offset 1Ch and I/O Port 121Ch.

Table 5-16 shows the PCI header registers of F1. The memory mapped registers accessed through F1BAR are shown in Table 5-17.

If the Power Management Configuration Trap bit (F0 Index 41h[3]) is enabled, an access to the PCI header registers causes an SMI. Access through F1BAR is not affected by this bit.

Table 5-16. F1 Index xxh: PCI Header Registers for SMI Status and ACPI Timer

Bit	Description	
Index 00h-01h	**Vendor Identification Register (RO)**	**Reset Value = 1078h**
Index 02h-03h	**Device Identification Register (RO)**	**Reset Value = 0101h**
Index 04h-05h	**PCI Command Register (R/W)**	**Reset Value = 0000h**
15:2	**Reserved (Read Only)**	
1	**Memory Space:** Allow CS5530A to respond to memory cycles from the PCI bus. 0 = Disable; 1 = Enable. This bit must be enabled to access memory offsets through F1BAR (F1 Index 10h).	
0	**Reserved (Read Only)**	
Index 06h-07h	**PCI Status Register (RO)**	**Reset Value = 0280h**
Index 08h	**Device Revision ID Register (RO)**	**Reset Value = 00h**
Index 09h-0Bh	**PCI Class Code Register (RO)**	**Reset Value = 068000h**
Index 0Ch	**PCI Cache Line Size Register (RO)**	**Reset Value = 00h**
Index 0Dh	**PCI Latency Timer Register (RO)**	**Reset Value = 00h**
Index 0Eh	**PCI Header Type (RO)**	**Reset Value = 00h**
Index 0Fh	**PCI BIST Register (RO)**	**Reset Value = 00h**
Index 10h-13h	**Base Address Register — F1BAR (R/W)**	**Reset Value = 00000000h**
This register sets the base address of the memory mapped SMI status and ACPI timer related registers. Bits [7:0] are read only (00h), indicating a 256-byte memory address range. Refer to Table 5-17 for the SMI status and ACPI timer registers bit formats and reset values. The upper 16 bytes are always mapped to the ACPI timer, and are always memory mapped. **Note:** The ACPI Timer Count Register is accessible through F1BAR+Memory Offset 1Ch and I/O Port 121Ch.		
31:8	**SMI Status/Power Management Base Address**	
7:0	**Address Range (Read Only)**	
Index 14h-3Fh	**Reserved**	**Reset Value = 00h**
Index 40h-FFh	**Reserved**	**Reset Value = xxh**

Table 5-17. F1BAR+Memory Offset xxh: SMI Status and ACPI Timer Registers

Bit	Description
Offset 00h-01h	**Top Level SMI Status Mirror Register (RO)** **Reset Value = 0000h**
15	**Suspend Modulation Enable Mirror (Read Only):** This bit mirrors the Suspend Mode Configuration bit (F0 Index 96h[0]). It is used by the SMI handler to determine if the SMI Speedup Disable Register (F1BAR+Memory Offset 08h) must be cleared on exit.
14	**SMI Source is USB (Read Only):** SMI was caused by USB activity? 0 = No; 1 = Yes. SMI generation is configured in F0 Index 42h[7:6].
13	**SMI Source is Warm Reset Command (Read Only):** SMI was caused by Warm Reset command? 0 = No; 1 = Yes.
12	**SMI Source is NMI (Read Only):** SMI was caused by NMI activity? 0 = No; 1 = Yes.
11:10	**Reserved (Read Only):** Always reads 0.
9	**SMI Source is General Purpose Timers/User Defined Device Traps/Register Space Trap (Read Only):** SMI was caused by expiration of GP Timer 1/2; trapped access to UDEF3/2/1; trapped access to F1-F4 or ISA Legacy Register Space? 0 = No; 1 = Yes. The next level of status is found at F1BAR+Memory Offset 04h/06h.
8	**SMI Source is Software Generated (Read Only):** SMI was caused by software? 0 = No; 1 = Yes.
7	**SMI on an A20M# Toggle (Read Only):** SMI was caused by an access to either Port 092h or the keyboard command which initiates an A20M# SMI? 0 = No; 1 = Yes. This method of controlling the internal A20M# in the GX1 processor is used instead of a pin. SMI generation enabling is at F0 Index 53h[0].
6	**SMI Source is a VGA Timer Event (Read Only):** SMI was caused by the expiration of the VGA Timer (F0 Index 8Eh)? 0 = No; 1 = Yes. SMI generation enabling is at F0 Index 83h[3].
5	**SMI Source is Video Retrace (IRQ2) (Read Only):** SMI was caused by a video retrace event as decoded from the serial connection (PSERIAL register, bit 7) from the GX1 processor? 0 = No; 1 = Yes. SMI generation enabling is at F0 Index 83h[2].
4:2	**Reserved (Read Only):** Always reads 0.
1	**SMI Source is Audio Interface (Read Only):** SMI was caused by the audio interface? 0 = No; 1 = Yes. The next level SMI status registers is found in F3BAR+Memory Offset 10h/12h.
0	**SMI Source is Power Management Event (Read Only):** SMI was caused by one of the power management resources? 0 = No; 1 = Yes. The next level of status is found at F0 Index 84h-87h/F4h-F7h. **Note:** The status for the General Purpose Timers and the User Device Defined Traps are checked separately in bit 9.
Note: Reading this register does not clear the status bits. See F1BAR+Memory Offset 02h.	
Offset 02h-03h	**Top Level SMI Status Register (RC)** **Reset Value = 0000h**
15	**Suspend Modulation Enable Mirror (Read to Clear):** This bit mirrors the Suspend Mode Configuration bit (F0 Index 96h[0]). It is used by the SMI handler to determine if the SMI Speedup Disable Register (F1BAR+Memory Offset 08h) must be cleared on exit.
14	**SMI Source is USB (Read to Clear):** SMI was caused by USB activity? 0 = No; 1 = Yes. SMI generation is configured in F0 Index 42h[7:6].
13	**SMI Source is Warm Reset Command (Read to Clear):** SMI was caused by Warm Reset command? 0 = No; 1 = Yes.
12	**SMI Source is NMI (Read to Clear):** SMI was caused by NMI activity? 0 = No; 1 = Yes.
11:10	**Reserved (Read to Clear):** Always reads 0.
9	**SMI Source is General Purpose Timers/User Defined Device Traps/Register Space Trap (Read to Clear):** SMI was caused by expiration of GP Timer 1/2; trapped access to UDEF3/2/1; trapped access to F1-F4 or ISA Legacy Register Space? 0 = No; 1 = Yes. The next level of status is found at F1BAR+Memory Offset 04h/06h.
8	**SMI Source is Software Generated (Read to Clear):** SMI was caused by software? 0 = No; 1 = Yes.
7	**SMI on an A20M# Toggle (Read to Clear):** SMI was caused by an access to either Port 092h or the keyboard command which initiates an A20M# SMI? 0 = No; 1 = Yes. This method of controlling the internal A20M# in the GX1 processor is used instead of a pin. SMI generation enabling is at F0 Index 53h[0].

Table 5-17. F1BAR+Memory Offset xxh: SMI Status and ACPI Timer Registers (Continued)

Bit	Description
6	**SMI Source is a VGA Timer Event (Read to Clear):** SMI was caused by the expiration of the VGA Timer (F0 Index 8Eh)? 0 = No; 1 = Yes. SMI generation enabling is at F0 Index 83h[3].
5	**SMI Source is Video Retrace (IRQ2) (Read to Clear):** SMI was caused by a video retrace event as decoded from the serial connection (PSERIAL register, bit 7) from the GX1 processor? 0 = No; 1 = Yes. SMI generation enabling is at F0 Index 83h[2].
4:2	**Reserved (Read to Clear):** Always reads 0.
1	**SMI Source is Audio Interface (Read to Clear):** SMI was caused by the audio interface? 0 = No; 1 = Yes. The next level SMI status registers is found in F3BAR+Memory Offset 10h/12h.
0	**SMI Source is Power Management Event (Read to Clear):** SMI was caused by one of the power management resources? 0 = No; 1 = Yes. The next level of status is found at F0 Index 84h-87h/F4h-F7h. **Note:** The status for the General Purpose Timers and the User Device Defined Traps are checked separately in bit 9.
Note: Reading this register clears all the SMI status bits. Note that bits 9, 1, and 0 have another level (second) of status reporting. A read-only "Mirror" version of this register exists at F1BAR+Memory Offset 00h. If the value of the register must be read without clearing the SMI source (and consequently deasserting SMI), the Mirror register may be read instead.	
Offset 04h-05h	**Second Level General Traps & Timers SMI Status Mirror Register (RO)** **Reset Value = 0000h**
15:6	**Reserved (Read Only)**
5	**PCI Function Trap (Read Only):** SMI was caused by a trapped configuration cycle (listed below)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[9]. Trapped access to F0 PCI header registers other than F0 Index 40h-43h; SMI generation enabling is at F0 Index 41h[0]. Trapped access to F1 PCI header registers; SMI generation enabling is at F0 Index 41h[3]. Trapped access to F2 PCI header registers; SMI generation enabling is at F0 Index 41h[6]. Trapped access to F3 PCI header registers; SMI generation enabling is at F0 Index 42h[0]. Trapped access to F4 PCI header registers; SMI generation enabling is at F0 Index 42h[1].
4	**SMI Source is Trapped Access to User Defined Device 3 (Read Only):** SMI was caused by a trapped I/O or memory access to the User Defined Device 3 (F0 Index C8h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[9]. SMI generation enabling is at F0 Index 82h[6].
3	**SMI Source is Trapped Access to User Defined Device 2 (Read Only):** SMI was caused by a trapped I/O or memory access to the User Defined Device 2 (F0 Index C4h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[9]. SMI generation enabling is at F0 Index 82h[5].
2	**SMI Source is Trapped Access to User Defined Device 1 (Read Only):** SMI was caused by a trapped I/O or memory access to the User Defined Device 1 (F0 Index C0h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[9]. SMI generation enabling is at F0 Index 82h[4].
1	**SMI Source is Expired General Purpose Timer 2 (Read Only):** SMI was caused by the expiration of General Purpose Timer 2 (F0 Index 8Ah)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[9]. SMI generation enabling is at F0 Index 83h[1].
0	**SMI Source is Expired General Purpose Timer 1 (Read Only):** SMI was caused by the expiration of General Purpose Timer 1 (F0 Index 88h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[9]. SMI generation enabling is at F0 Index 83h[0].
Note: Reading this register does not clear the status bits. See F1BAR+Memory Offset 06h.	
Offset 06h-07h	**Second Level General Traps & Timers SMI Status Register (RC)** **Reset Value = 0000h**
15:6	**Reserved (Read to Clear)**

Table 5-17. F1BAR+Memory Offset xxh: SMI Status and ACPI Timer Registers (Continued)

Bit	Description
5	**PCI Function Trap (Read to Clear):** SMI was caused by a trapped configuration cycle (listed below)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[9]. Trapped access to F0 PCI header registers other than Index 40h-43h; SMI generation enabling is at F0 Index 41h[0]. Trapped access to F1 PCI header registers; SMI generation enabling is at F0 Index 41h[3]. Trapped access to F2 PCI header registers; SMI generation enabling is at F0 Index 41h[6]. Trapped access to F3 PCI header registers; SMI generation enabling is at F0 Index 42h[0]. Trapped access to F4 PCI header registers; SMI generation enabling is at F0 Index 42h[1].
4	**SMI Source is Trapped Access to User Defined Device 3 (Read to Clear):** SMI was caused by a trapped I/O or memory access to the User Defined Device 3 (F0 Index C8h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[9]. SMI generation enabling is at F0 Index 82h[6].
3	**SMI Source is Trapped Access to User Defined Device 2 (Read to Clear):** SMI was caused by a trapped I/O or memory access to the User Defined Device 2 (F0 Index C4h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[9]. SMI generation enabling is at F0 Index 82h[5].
2	**SMI Source is Trapped Access to User Defined Device 1 (Read to Clear):** SMI was caused by a trapped I/O or memory access to the User Defined Device 1 (F0 Index C0h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[9]. SMI generation enabling is at F0 Index 82h[4].
1	**SMI Source is Expired General Purpose Timer 2 (Read to Clear):** SMI was caused by the expiration of General Purpose Timer 2 (F0 Index 8Ah)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[9]. SMI generation enabling is at F0 Index 83h[1].
0	**SMI Source is Expired General Purpose Timer 1 (Read to Clear):** SMI was caused by the expiration of General Purpose Timer 1 (F0 Index 88h)? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported in F1BAR+Memory Offset 00h/02h[9]. SMI generation enabling is at F0 Index 83h[0].
Note: Reading this register clears all the SMI status bits. A read-only “Mirror” version of this register exists at F1BAR+Memory Offset 04h. If the value of the register must be read without clearing the SMI source (and consequently deasserting SMI), the Mirror register may be read instead.	
Offset 08h-09h	**SMI Speedup Disable Register (Read to Enable)** — **Reset Value = 0000h**
15:0	**SMI Speedup Disable:** If bit 1 in the Suspend Configuration Register is set (F0 Index 96h[1] = 1), a read of this register invokes the SMI handler to re-enable Suspend Modulation. The data read from this register can be ignored. If the Suspend Modulation feature is disabled, reading this I/O location has no effect.
Offset 0Ah-1Bh	**Reserved** — **Reset Value = xxh**
Offset 1Ch-1Fh (Note)	**ACPI Timer Count Register (RO)** — **Reset Value = 00FFFFFCh**
ACPI_COUNT (Read Only): This read-only register provides the current value of the ACPI timer. The timer counts at 14.31818/4 MHz (3.579545 MHz). If SMI generation is enabled via F0 Index 83h[5], an SMI is generated when the MSB toggles. The MSB toggles every 2.343 seconds. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported at F0 Index 87h/F7h[0].	
31:24	**Reserved:** Always returns 0.
23:0	**Counter**
Note: The ACPI Timer Count Register is also accessible through I/O Port 121Ch.	
Offset 20h-4Fh	**Reserved** — **Reset Value = xxh**
Offset 50h-FFh	The memory mapped registers located here (F1BAR+Memory Offset 50h-FFh) can also be accessed at F0 Index 50h-FFh. The preferred method is to program these register through the F0 register space. Refer to Table 5-15 "F0 Index xxh: PCI Header and Bridge Configuration Registers" on page 155 for bit information regarding these registers.

5.3.3 IDE Controller Registers - Function 2

The register space for the IDE controllers is divided into two sections. The first section is used to configure the PCI portion of the controller. A Base Address Register at F2 Index 20h points to the base address of where the second portion of the register space is located. This second section contains the registers used by the IDE controllers to carry out operations.

Table 5-18 shows the PCI header registers of F2. The I/O mapped registers, accessed through F2BAR, are shown in Table 5-19.

If the IDE Configuration Trap bit (F0 Index 41h[6]) is set, access to the PCI header registers causes an SMI. Access through F2BAR is not affected by this bit.

Table 5-18. F2 Index xxh: PCI Header Registers for IDE Configuration

Bit	Description	
Index 00h-01h	**Vendor Identification Register (RO)**	**Reset Value = 1078h**
Index 02h-03h	**Device Identification Register (RO)**	**Reset Value = 0102h**
Index 04h-05h	**PCI Command Register (R/W)**	**Reset Value = 0000h**
15:3	**Reserved (Read Only)**	
2	**Reserved**	
1	**Reserved (Read Only)**	
0	**I/O Space:** Allow CS5530A to respond to I/O cycles from the PCI bus. 0 = Disable; 1 = Enable. This bit must be enabled to access I/O offsets through F2BAR (F2 Index 20h).	
Index 06h-07h	**PCI Status Register (RO)**	**Reset Value = 0280h**
Index 08h	**Device Revision ID Register (RO)**	**Reset Value = 00h**
Index 09h-0Bh	**PCI Class Code Register (RO)**	**Reset Value = 010180h**
Index 0Ch	**PCI Cache Line Size Register (RO)**	**Reset Value = 00h**
Index 0Dh	**PCI Latency Timer Register (RO)**	**Reset Value = 00h**
Index 0Eh	**PCI Header Type (RO)**	**Reset Value = 00h**
Index 0Fh	**PCI BIST Register (RO)**	**Reset Value = 00h**
Index 10h-1Fh	**Reserved**	**ReservedReset Value = 00h**
Index 20h-23h	**Base Address Register - F2BAR (R/W)**	**Reset Value = 00000001h**
This register sets the base address of the I/O mapped bus mastering IDE and controller registers. Bits [6:0] are read only (0000 001), indicating a 128-byte I/O address range. Refer to Table 5-19 for the IDE configuration registers bit formats and reset values.		
31:7	**Bus Mastering IDE Base Address**	
6:0	**Address Range (Read Only)**	
Index 24h-3Fh	**Reserved**	**Reset Value = 00h**
Index 40h-FFh	**Reserved**	**Reset Value = xxh**

Table 5-19. F2BAR+I/O Offset xxh: IDE Configuration Registers

Bit	Description
Offset 00h	**IDE Bus Master 0 Command Register — Primary (R/W)** **Reset Value = 00h**
7:4	**Reserved:** Set to 0. Must return 0 on reads.
3	**Read or Write Control:** Sets the direction of bus master transfers. 0 = PCI reads performed; 1 = PCI writes performed. This bit should not be changed when the bus master is active.
2:1	**Reserved:** Set to 0. Must return 0 on reads.
0	**Bus Master Control:** Controls the state of the bus master. 0 = Disable master; 1 = Enable master. Bus master operations can be halted by setting bit 0 to 0. Once an operation has been halted, it can not be resumed. If bit 0 is set to 0 while a bus master operation is active, the command is aborted and the data transferred from the drive is discarded. This bit should be reset after completion of data transfer.
Offset 01h	**Reserved** **Reset Value = xxh**
Offset 02h	**IDE Bus Master 0 Status Register — Primary (R/W)** **Reset Value = 00h**
7	**Simplex Mode (Read Only):** Can both the primary and secondary channel operate independently? 0 = Yes; 1 = No (simplex mode).
6	**Drive 1 DMA Capable:** Allow Drive 1 to be capable of DMA transfers. 0 = Disable; 1 = Enable.
5	**Drive 0 DMA Capable:** Allow Drive 0 to be capable of DMA transfers. 0 = Disable; 1 = Enable.
4:3	**Reserved:** Set to 0. Must return 0 on reads.
2	**Bus Master Interrupt:** Has the bus master detected an interrupt? 0 = No; 1 = Yes. Write 1 to clear.
1	**Bus Master Error:** Has the bus master detected an error during data transfer? 0 = No; 1 = Yes. Write 1 to clear.
0	**Bus Master Active (Read Only):** Is the bus master active? 0 = No; 1 = Yes.
Offset 03h	**Reserved** **Reset Value = xxh**
Offset 04h-07h	**IDE Bus Master 0 PRD Table Address — Primary (R/W)** **Reset Value = 00000000h**
31:2	**Pointer to the Physical Region Descriptor Table:** This register is a PRD table pointer for IDE Bus Master 0. When written, this register points to the first entry in a PRD table. Once IDE Bus Master 0 is enabled (Command Register bit 0 = 1], it loads the pointer and updates this register to the next PRD by adding 08h. When read, this register points to the next PRD.
1:0	**Reserved:** Set to 0.
Offset 08h	**IDE Bus Master 1 Command Register — Secondary (R/W)** **Reset Value = 00h**
7:4	**Reserved:** Set to 0. Must return 0 on reads.
3	**Read or Write Control:** Sets the direction of bus master transfers. 0 = PCI reads performed; 1 = PCI writes performed. This bit should not be changed when the bus master is active.
2:1	**Reserved:** Set to 0. Must return 0 on reads.
0	**Bus Master Control:** Controls the state of the bus master. 0 = Disable master; 1 = Enable master. Bus master operations can be halted by setting bit 0 = 0. Once an operation has been halted, it can not be resumed. If bit 0 is set to 0 while a bus master operation is active, the command is aborted and the data transferred from the drive is discarded. This bit should be reset after completion of data transfer.
Offset 09h	**Reserved** **Reset Value = xxh**
Offset 0Ah	**IDE Bus Master 1 Status Register — Secondary (R/W)** **Reset Value = 00h**
7	**Simplex Mode (Read Only):** Can both the primary and secondary channel operate independently? 0 = Yes; 1 = No (simplex mode).
6	**Drive 1 DMA Capable:** Allow Drive 1 to be capable of DMA transfers. 0 = Disable; 1 = Enable.
5	**Drive 0 DMA Capable:** Allow Drive 0 to be capable of DMA transfers. 0 = Disable; 1 = Enable.
4:3	**Reserved:** Set to 0. Must return 0 on reads.
2	**Bus Master Interrupt:** Has the bus master detected an interrupt? 0 = No; 1 = Yes. Write 1 to clear.
1	**Bus Master Error:** Has the bus master detected an error during data transfer? 0 = No; 1 = Yes. Write 1 to clear.

Table 5-19. F2BAR+I/O Offset xxh: IDE Configuration Registers (Continued)

Bit	Description
0	**Bus Master Active (Read Only):** Is the bus master active? 0 = No; 1 = Yes.
Offset 0Bh	**Reserved** **Reset Value = xxh**
Offset 0Ch-0Fh	**IDE Bus Master 1 PRD Table Address — Secondary (R/W)** **Reset Value = 00000000h**
31:2	**Pointer to the Physical Region Descriptor Table:** This register is a PRD table pointer for IDE Bus Master 1. When written, this register points to the first entry in a PRD table. Once IDE Bus Master 1 is enabled (Command Register bit 0 = 1], it loads the pointer and updates this register to the next PRD by adding 08h. When read, this register points to the next PRD.
1:0	**Reserved:** Set to 0.
Offset 10h-1Fh	**Reserved** **Reset Value = xxh**
Offset 20h-23h	**Channel 0 Drive 0 PIO Register (R/W)** **Reset Value = 0000E132h (Note)**
If Offset 24h[31] = 0, Format 0: Selects slowest PIOMODE per channel for commands. Format 0 settings for: PIO Mode 0 = 00009172h PIO Mode 1 = 00012171h PIO Mode 2 = 00020080h PIO Mode 3 = 00032010h PIO Mode 4 = 00040010h	
31:20	**Reserved:** Set to 0.
19:16	**PIOMODE:** PIO mode
15:12	**t2I:** Recovery time (value + 1 cycle)
11:8	**t3:** IDE_IOW# data setup time (value + 1 cycle)
7:4	**t2W:** IDE_IOW# width minus t3 (value + 1 cycle)
3:0	**t1:** Address Setup Time (value + 1 cycle)
If Offset 24h[31] = 1, **Format 1:** Allows independent control of command and data. Format 1 settings for: PIO Mode 0 = 9172D132h PIO Mode 1 = 21717121h PIO Mode 2 = 00803020h PIO Mode 3 = 20102010h PIO Mode 4 = 00100010h	
31:28	**t2IC:** Command cycle recovery time (value + 1 cycle)
27:24	**t3C:** Command cycle IDE_IOW# data setup (value + 1 cycle)
23:20	**t2WC:** Command cycle IDE_IOW# pulse width minus t3 (value + 1 cycle)
19:16	**t1C:** Command cycle address setup time (value + 1 cycle)
15:12	**t2ID:** Data cycle recovery time (value + 1 cycle)
11:8	**t3D:** Data cycle IDE_IOW# data setup (value + 1 cycle)
7:4	**t2WD:** Data cycle IDE_IOW# pulse width minus t3 (value + 1 cycle)
3:0	**t1D:** Data cycle address Setup Time (value + 1 cycle)
Note: The reset value of this register is not a valid PIO Mode.	

Table 5-19. F2BAR+I/O Offset xxh: IDE Configuration Registers (Continued)

Bit	Description
Offset 24h-27h	**Channel 0 Drive 0 DMA Control Register (R/W)** — **Reset Value = 00077771h**
If bit 20 = 0, Multiword DMA Settings for: Multiword DMA Mode 0 = 00077771h Multiword DMA Mode 1 = 00012121h Multiword DMA Mode 2 = 00002020h	
31	**PIO Mode Format:** 0 = Format 0; 1 = Format 1.
30:21	**Reserved:** Set to 0.
20	**DMA Operation:** 0 = Multiword DMA; 1 = Ultra DMA.
19:16	**tKR:** IDE_IOR# recovery time (4-bit) (value + 1 cycle)
15:12	**tDR:** IDE_IOR# pulse width (value + 1 cycle)
11:8	**tKW:** IDE_IOW# recovery time (4-bit) (value + 1 cycle)
7:4	**tDW:** IDE_IOW# pulse width (value + 1 cycle)
3:0	**tM:** IDE_CS0#/CS1# to IDE_IOR#/IOW# setup; IDE_CS0#/CS1# setup to IDE_DACK0#/DACK1#
If bit 20 = 1, Ultra DMA Settings for: Ultra DMA Mode 0 = 00921250h Ultra DMA Mode 1 = 00911140h Ultra DMA Mode 2 = 00911030h	
31	**PIO Mode Format:** 0 = Format 0; 1 = Format 1.
30:21	**Reserved:** Set to 0.
20	**DMA Operation:** 0 = Multiword DMA, 1 = Ultra DMA.
19:16	**tCRC:** CRC setup UDMA in IDE_DACK# (value + 1 cycle) (for host terminate CRC setup = tMLI + tSS)
15:12	**tSS:** UDMA out (value + 1 cycle)
11:8	**tCYC:** Data setup and cycle time UDMA out (value + 2 cycles)
7:4	**tRP:** Ready to pause time (value + 1 cycle). Note: tRFS + 1 tRP on next clock.
3:0	**tACK:** IDE_CS0#/CS1# setup to IDE_DACK0#/DACK1# (value + 1 cycle)
Offset 28h-2Bh	**Channel 0 Drive 1 PIO Register (R/W)** — **Reset Value = 0000E132h**
Channel 0 Drive 1 Programmed I/O Control Register: Refer to F2BAR+I/O Offset 20h for bit descriptions.	
Offset 2Ch-2Fh	**Channel 0 Drive 1 DMA Control Register (R/W)** — **Reset Value = 00077771h**
Channel 0 Drive 1 MDMA/UDMA Control Register: Refer to F2BAR+I/O Offset 24h for bit descriptions. **Note:** Once the PIO Mode Format is selected in F2BAR+I/O Offset 24h[31], bit 31 of this register is defined as reserved, read only.	
Offset 30h-33h	**Channel 1 Drive 0 PIO Register (R/W)** — **Reset Value = 0000E132h**
Channel 1 Drive 0 Programmed I/O Control Register: Refer to F2BAR+I/O Offset 20h for bit descriptions.	
Offset 34h-37h	**Channel 1 Drive 0 DMA Control Register (R/W)** — **Reset Value = 00077771h**
Channel 1 Drive 0 MDMA/UDMA Control Register: Refer to F2BAR+I/O Offset 24h for bit descriptions. **Note:** Once the PIO Mode Format is selected in F2BAR+I/O Offset 24h[31], bit 31 of this register is defined as reserved, read only.	
Offset 38h-3Bh	**Channel 1 Drive 1 PIO Register (R/W)** — **Reset Value = 0000E132h**
Channel 1 Drive 1 Programmed I/O Control Register: Refer to F2BAR+I/O Offset 20h for bit descriptions.	
Offset 3Ch-3Fh	**Channel 1 Drive 1 DMA Control Register (R/W)** — **Reset Value = 00077771h**
Channel 1 Drive 1 MDMA/UDMA Control Register: Refer to F2BAR+I/O Offset 24h for bit descriptions. **Note:** Once the PIO Mode Format is selected in F2BAR+I/O Offset 24h[31], bit 31 of this register is defined as reserved, read only.	
Offset 40h-FFh	**Reserved** — **Reset Value = xxh**

5.3.4 XpressAUDIO™ Subsystem Registers - Function 3

The register space for the XpressAUDIO™ subsystem is divided into two sections. The first section is used to configure the PCI portion of the audio interface hardware. A Base Address Register at F3 Index 10h (F3BAR) points to the base address of where the second portion of the register space is located. This second section contains the control and data registers of the audio interface.

Table 5-20 shows the PCI header registers of F3. The memory mapped registers accessed through F3BAR are shown in Table 5-21.

If the F3 Audio Configuration Trap bit (F0 Index 42h[0]) is enabled, an access to the PCI header registers causes an SMI. Access through F3BAR is not affected by this bit.

Table 5-20. F3 Index xxh: PCI Header Registers for XpressAUDIO™ Subsystem

Bit	Description	
Index 00h-01h	**Vendor Identification Register (RO)**	**Reset Value = 1078h**
Index 02h-03h	**Device Identification Register (RO)**	**Reset Value = 0103h**
Index 04h-05h	**PCI Command Register (R/W)**	**Reset Value = 0000h**
15:3	**Reserved (Read Only)**	
2	**Reserved (Read/Write)**	
1	**Memory Space:** Allow CS5530A to respond to memory cycles from the PCI bus. 0 = Disable; 1 = Enable. This bit must be enabled to access memory offsets through F3BAR (F3 Index 10h).	
0	**Reserved (Read Only)**	
Index 06h-07h	**PCI Status Register (RO)**	**Reset Value = 0280h**
Index 08h	**Device Revision ID Register (RO)**	**Reset Value = 00h**
Index 09h-0Bh	**PCI Class Code Register (RO)**	**Reset Value = 040100h**
Index 0Ch	**PCI Cache Line Size Register (RO)**	**Reset Value = 00h**
Index 0Dh	**PCI Latency Timer Register (RO)**	**Reset Value = 00h**
Index 0Eh	**PCI Header Type (RO)**	**Reset Value =00h**
Index 0Fh	**PCI BIST Register (RO)**	**Reset Value = 00h**
Index 10h-13h	**Base Address Register - F3BAR (R/W)**	**Reset Value = 00000000h**
This register sets the base address of the memory mapped audio interface control register block. This is a 128-byte block of registers used to control the audio FIFO and codec interface, as well as to support SMIs produced by VSA technology. Bits [6:0] are read only (0000000), indicating a 128-byte memory address range. Refer to Table 5-21 for the bit formats and reset values of the XpressAUDIO subsystem support registers.		
31:7	**Audio Interface Base Address**	
6:0	**Address Range (Read Only)**	
Index 14h-3Fh	**Reserved**	**Reset Value = 00h**
Index 40h-FFh	**Reserved**	**Reset Value = xxh**

Table 5-21. F3BAR+Memory Offset xxh: XpressAUDIO™ Subsystem Configuration Registers

Bit	Description
Offset 00h-03h	**Codec GPIO Status Register (R/W)** — **Reset Value = 00100000h**
31	**Codec GPIO Interface:** 0 = Disable; 1 = Enable.
30	**Codec GPIO SMI:** Allow codec GPIO interrupt to generate an SMI. 0 = Disable; 1= Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[1]. Second level SMI status is reported at F3BAR+Memory Offset 10h/12h[1].
29:21	**Reserved:** Set to 0.
20	**Codec GPIO Status Valid (Read Only):** Is the status read valid? 0 = Yes; 1 = No.
19:0	**Codec GPIO Pin Status (Read Only):** This is the GPIO pin status that is received from the codec in slot 12 on SDATA_IN signal.
Offset 04h-07h	**Codec GPIO Control Register (R/W)** — **Reset Value = 00000000h**
31:20	**Reserved:** Set to 0.
19:0	**Codec GPIO Pin Data:** This is the GPIO pin data that is sent to the codec in slot 12 on the SDATA_OUT signal.
Offset 08h-0Bh	**Codec Status Register (R/W)** — **Reset Value = 00000000h**
31:24	**Codec Status Address (Read Only):** Address of the register for which status is being returned. This address comes from slot 1 bits [19:12].
23	**Codec Serial INT SMI:** Allow codec serial interrupt to generate an SMI. 0 = Disable; 1= Enable. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[1]. Second level SMI status is reported at F3BAR+Memory Offset 10h/12h[1].
22	**SYNC Pin:** Selects SYNC pin level. 0 = Low; 1 = High.
21	**Enable SDATA_IN2:** Pin AE24 function selection. 0 = GPIO1; 1 = SDATA_IN2. For this pin to function as SDATA_IN2, it must first be configured as an input (F0 Index 90h[1] = 0).
20	**Audio Bus Master 5 AC97 Slot Select:** Selects slot for Audio Bus Master 5 to receive data. 0 = Slot 6; 1 = Slot 11.
19	**Audio Bus Master 4 AC97 Slot Select:** Selects slot for Audio Bus Master 4 to transmit data. 0 = Slot 6; 1 = Slot 11.
18	**Reserved:** Set to 0.
17	**Status Tag (Read Only):** Determines if the status in bits [15:0] is new or not. 0 = Not new; 1 = New.
16	**Codec Status Valid (Read Only):** Is the status in bits [15:0] valid? 0 = No; 1 = Yes.
15:0	**Codec Status (Read Only):** This is the codec status data that is received from the codec in slot 2 on SDATA_IN. Only bits [19:4] are used from slot 2.
Offset 0Ch-0Fh	**Codec Command Register (R/W)** — **Reset Value = 00000000h**
31:24	**Codec Command Address:** Address of the codec control register for which the command is being sent. This address goes in slot 1 bits [19:12] on SDATA_OUT.
23:22	**CS5530A Codec Communication:** Selects which codec to communicate with. 00 = Primary codec 10 = Third codec 01 = Secondary codec 11 = Fourth codec **Note:** 00 and 01 are the only valid settings for these bits.
21:17	**Reserved:** Set to 0.
16	**Codec Command Valid:** Is the command in bits [15:0] valid? 0 = No; 1 = Yes. This bit is set by hardware when a command is loaded. It remains set until the command has been sent to the codec.
15:0	**Codec Command:** This is the command being sent to the codec in bits [19:12] of slot 2 on SDATA_OUT.
Offset 10h-11h	**Second Level Audio SMI Status Register (RC)** — **Reset Value = 0000h**
15:8	**Reserved:** Set to 0.
7	**Audio Bus Master 5 SMI Status (Read to Clear):** SMI was caused by an event occurring on Audio Bus Master 5? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 5 is enabled (F3BAR+Memory Offset 48h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 49h[0] = 1).

Table 5-21. F3BAR+Memory Offset xxh: XpressAUDIO™ Subsystem Configuration Registers (Contin-

Bit	Description
6	**Audio Bus Master 4 SMI Status (Read to Clear):** SMI was caused by an event occurring on Audio Bus Master 4? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 4 is enabled (F3BAR+Memory Offset 40h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 41h[0] = 1).
5	**Audio Bus Master 3 SMI Status (Read to Clear):** SMI was caused by an event occurring on Audio Bus Master 3? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 3 is enabled (F3BAR+Memory Offset 38h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 39h[0] = 1).
4	**Audio Bus Master 2 SMI Status (Read to Clear):** SMI was caused by an event occurring on Audio Bus Master 2? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 2 is enabled (F3BAR+Memory Offset 30h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 31h[0] = 1).
3	**Audio Bus Master 1 SMI Status (Read to Clear):** SMI was caused by an event occurring on Audio Bus Master 1? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 1 is enabled (F3BAR+Memory Offset 28h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 29h[0] = 1).
2	**Audio Bus Master 0 SMI Status (Read to Clear):** SMI was caused by an event occurring on Audio Bus Master 0? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 0 is enabled (F3BAR+Memory Offset 20h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 21h[0] = 1).
1	**Codec Serial or GPIO Interrupt SMI Status (Read to Clear):** SMI was caused by a serial or GPIO interrupt from codec? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation enabling for codec serial interrupt: F3BAR+Memory Offset 08h[23] = 1. SMI generation enabling for codec GPIO interrupt: F3BAR+Memory Offset 00h[30] = 1.
0	**I/O Trap SMI Status (Read to Clear):** SMI was caused by an I/O trap? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The next level (third level) of SMI status reporting is at F3BAR+Memory Offset 14h. The top level is reported at F1BAR+Memory Offset 00h/02h[1].
Note: Reading this register clears the status bits. Note that bit 0 has another level (third) of SMI status reporting. A read-only “Mirror” version of this register exists at F3BAR+Memory Offset 12h. If the value of the register must be read without clearing the SMI source (and consequently deasserting SMI), the Mirror register may be read instead.	
Offset 12h-13h	**Second Level Audio SMI Status Mirror Register (RO)** **Reset Value = 0000h**
15:8	**Reserved:** Set to 0.
7	**Audio Bus Master 5 SMI Status (Read Only):** SMI was caused by an event occurring on Audio Bus Master 5? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 5 is enabled (F3BAR+Memory Offset 48h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 49h[0] = 1).
6	**Audio Bus Master 4 SMI Status (Read Only):** SMI was caused by an event occurring on Audio Bus Master 4? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 4 is enabled (F3BAR+Memory Offset 40h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 41h[0] = 1).
5	**Audio Bus Master 3 SMI Status (Read Only):** SMI was caused by an event occurring on Audio Bus Master 3? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 3 is enabled (F3BAR+Memory Offset 38h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 39h[0] = 1).

Table 5-21. F3BAR+Memory Offset xxh: XpressAUDIO™ Subsystem Configuration Registers (Contin-

Bit	Description
4	**Audio Bus Master 2 SMI Status (Read Only):** SMI was caused by an event occurring on Audio Bus Master 2? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 2 is enabled (F3BAR+Memory Offset 30h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 31h[0] = 1).
3	**Audio Bus Master 1 SMI Status (Read Only):** SMI was caused by an event occurring on Audio Bus Master 1? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 1 is enabled (F3BAR+Memory Offset 28h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 29h[0] = 1).
2	**Audio Bus Master 0 SMI Status (Read Only):** SMI was caused by an event occurring on Audio Bus Master 0? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation is enabled when Audio Bus Master 0 is enabled (F3BAR+Memory Offset 20h[0] = 1). An SMI is then generated when the End of Page bit is set in the SMI Status Register (F3BAR+Memory Offset 21h[0] = 1).
1	**Codec Serial or GPIO Interrupt SMI Status (Read Only):** SMI was caused by a serial or GPIO interrupt from codec? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation enabling for codec serial interrupt: F3BAR+Memory Offset 08h[23] = 1. SMI generation enabling for codec GPIO interrupt: F3BAR+Memory Offset 00h[30] = 1.
0	**I/O Trap SMI Status (Read Only):** SMI was caused by an I/O trap? 0 = No; 1 = Yes. This is the second level of SMI status reporting. The next level (third level) of SMI status reporting is at F3BAR+Memory Offset 14h. The top level is reported at F1BAR+Memory Offset 00h/02h[1].
Note: Reading this register does not clear the status bits. See F3BAR+Memory Offset 10h.	
Offset 14h-17h	**I/O Trap SMI and Fast Write Status Register (RO/RC)** **Reset Value = 00000000h**
31:24	**Fast Path Write Even Access Data (Read Only):** These bits contain the data from the last Fast Path Write Even access. These bits change only on a fast write to an even address.
23:16	**Fast Path Write Odd Access Data (Read Only):** These bits contain the data from the last Fast Path Write Odd access. These bits change on a fast write to an odd address, and also on any non-fast write.
15	**Fast Write A1 (Read Only):** This bit contains the A1 value for the last Fast Write access.
14	**Read or Write I/O Access (Read Only):** Last trapped I/O access was a read or a write? 0 = Read; 1 = Write.
13	**Sound Card or FM Trap SMI Status (Read to Clear):** SMI was caused by a trapped I/O access to the sound card or FM I/O Trap? 0 = No; 1 = Yes. (Note) Fast Path Write must be enabled, F3BAR+Memory Offset 18h[11] = 1, for the SMI to be reported here. If Fast Path Write is disabled, the SMI is reported in bit 10 of this register. This is the third level of SMI status reporting. The second level of SMI status is reported at F3BAR+Memory Offset 10h/12h[0]. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation enabling is at F3BAR+Memory Offset 18h[2].
12	**DMA Trap SMI Status (Read to Clear):** SMI was caused by a trapped I/O access to the DMA I/O Trap? 0 = No; 1 = Yes. (Note) This is the third level of SMI status reporting. The second level of SMI status is reported at F3BAR+Memory Offset 10h/12h[0]. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation enabling is at F3BAR+Memory Offset 18h[8:7].
11	**MPU Trap SMI Status (Read to Clear):** SMI was caused by a trapped I/O access to the MPU I/O Trap? 0 = No; 1 = Yes. (Note) This is the third level of SMI status reporting. The second level of SMI status is reported at F3BAR+Memory Offset 10h/12h[0]. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation enabling is at F3BAR+Memory Offset 18h[6:5].

Table 5-21. F3BAR+Memory Offset xxh: XpressAUDIO™ Subsystem Configuration Registers (Contin-

Bit	Description
10	**Sound Card or FM Trap SMI Status (Read to Clear):** SMI was caused by a trapped I/O access to the sound card or FM I/O Trap? 0 = No; 1 = Yes. (Note) Fast Path Write must be disabled, F3BAR+Memory Offset 18h[11] = 0, for the SMI to be reported here. If Fast Path Write is enabled, the SMI is reported in bit 13 of this register. This is the third level of SMI status reporting. The second level of SMI status is reported at F3BAR+Memory Offset 10h/12h[0]. The top level is reported at F1BAR+Memory Offset 00h/02h[1]. SMI generation enabling is at F3BAR+Memory Offset 18h[2].
9:0	**X-Bus Address (Read Only):** Bits [9:0] contain the captured ten bits of X-Bus address.
Note: For the four SMI status bits (bits [13:10]), if the activity was a fast write to an even address, no SMI is generated regardless of the DMA, MPU, or sound card status. If the activity was a fast write to an odd address, an SMI is generated but bit 13 is set to a 1.	
Offset 18h-19h	**I/O Trap SMI Enable Register (R/W)** **Reset Value = 0000h**
15:12	**Reserved:** Set to 0.
11	**Fast Path Write Enable:** Fast Path Write (an SMI is not generated on certain writes to specified addresses). 0 = Disable; 1 = Enable. In Fast Path Write, the CS5530A responds to writes to the following addresses: 388h, 38Ah and 38Bh; 2x0h, 2x2h, and 2x8h.
10:9	**Fast Read:** These two bits hold part of the response that the CS5530A returns for reads to several I/O locations.
8	**High DMA I/O Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs at I/O Port C0h-DFh, an SMI is generated. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[1]. Second level SMI status is reported at F3BAR+Memory Offset 10h/12h[0]. Third level SMI status is reported at F3BAR+Memory Offset 14h[12].
7	**Low DMA I/O Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs at I/O Port 00h-0Fh, an SMI is generated. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[1]. Second level SMI status is reported at F3BAR+Memory Offset 10h/12h[0]. Third level SMI status is reported at F3BAR+Memory Offset 14h[12].
6	**High MPU I/O Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs at I/O Port 330h and 331h, an SMI is generated. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[1]. Second level SMI status is reported at F3BAR+Memory Offset 10h/12h[0]. Third level SMI status is reported at F3BAR+Memory Offset 14h[11].
5	**Low MPU I/O Trap:** I0 = Disable; 1 = Enable. If this bit is enabled and an access occurs at I/O Port 300h and 301h, an SMI is generated. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[1]. Second level SMI status is reported at F3BAR+Memory Offset 10h/12h[0]. Third level SMI status is reported at F3BAR+Memory Offset 14h[11].
4	**Fast Path Read Enable/SMI Disable:** Read Fast Path (an SMI is not generated on reads from specified addresses). 0 = Disable; 1 = Enable. In Fast Path Read the CS5530A responds to reads of the following addresses: 388h-38Bh; 2x0h, 2x1h, 2x2h, 2x3h, 2x8h and 2x9h. Note that if neither sound card nor FM I/O mapping is enabled, then status read trapping is not possible.
3	**FM I/O Trap:** 0 = Disable; 1 = Enable. If this bit is enabled and an access occurs at I/O Port 388h to 38Bh, an SMI is generated. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[1]. Second level SMI status is reported at F3BAR+Memory Offset 10h/12h[0].
2	**Sound Card I/O Trap:** 0 = Disable; 1 = Enable If this bit is enabled and an access occurs in the address ranges selected by bits [1:0], an SMI is generated. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[1]. Second level SMI status is reported at F3BAR+Memory Offset 10h/12h[0]. Third level SMI status is reported at F3BAR+Memory Offset 14h[10].
1:0	**Sound Card Address Range Select:** These bits select the address range for the sound card I/O trap. 00 = I/O Port 220h-22Fh 10 = I/O Port 260h-26Fh 01 = I/O Port 240h-24Fh 11 = I/O Port 280h-28Fh

Table 5-21. F3BAR+Memory Offset xxh: XpressAUDIO™ Subsystem Configuration Registers (Contin-

Bit	Description
Offset 1Ah-1Bh	**Internal IRQ Enable Register (R/W)** **Reset Value = 0000h**
15	**IRQ15 Internal:** Configure IRQ15 for internal (software) or external (hardware) use. 0 = External; 1 = Internal.
14	**IRQ14 Internal:** Configure IRQ14 for internal (software) or external (hardware) use. 0 = External; 1 = Internal.
13	**Reserved:** Set to 0.
12	**IRQ12 Internal:** Configure IRQ12 for internal (software) or external (hardware) use. 0 = External; 1 = Internal.
11	**IRQ11 Internal:** Configure IRQ11 for internal (software) or external (hardware) use. 0 = External; 1 = Internal.
10	**IRQ10 Internal:** Configure IRQ10 for internal (software) or external (hardware) use. 0 = External; 1 = Internal.
9	**IRQ9 Internal:** Configure IRQ9 for internal (software) or external (hardware) use. 0 = External; 1 = Internal.
8	**Reserved:** Set to 0.
7	**IRQ7 Internal:** Configure IRQ7 for internal (software) or external (hardware) use. 0 = External; 1 = Internal.
6	**Reserved:** Set to 0.
5	**IRQ5 Internal:** Configure IRQ5 for internal (software) or external (hardware) use. 0 = External; 1 = Internal.
4	**IRQ4 Internal:** Configure IRQ4 for internal (software) or external (hardware) use. 0 = External; 1 = Internal.
3	**IRQ3 Internal:** Configure IRQ3 for internal (software) or external (hardware) use. 0 = External; 1 = Internal.
2:0	**Reserved:** Set to 0.
Note: Must be read and written as a WORD.	
Offset 1Ch-1Dh	**Internal IRQ Control Register (R/W)** **Reset Value = 0000h**
15	**Assert Masked Internal IRQ15:** 0 = Disable; 1 = Enable.
14	**Assert Masked Internal IRQ14:** 0 = Disable; 1 = Enable.
13	**Reserved:** Set to 0.
12	**Assert Masked Internal IRQ12:** 0 = Disable; 1 = Enable.
11	**Assert masked internal IRQ11:** 0 = Disable; 1 = Enable.
10	**Assert Masked Internal IRQ10:** 0 = Disable; 1 = Enable.
9	**Assert Masked Internal IRQ9:** 0 = Disable; 1 = Enable.
8	**Reserved:** Set to 0.
7	**Assert Masked Internal IRQ7:** 0 = Disable; 1 = Enable.
6	**Reserved:** Set to 0.
5	**Assert Masked Internal IRQ5:** 0 = Disable; 1 = Enable.
4	**Assert Masked Internal IRQ4:** 0 = Disable; 1 = Enable.
3	**Assert Masked Internal IRQ3:** 0 = Disable; 1 = Enable.
2:0	**Reserved:** Set to 0.
Offset 1Eh-1Fh	**Internal IRQ Mask Register (Write Only)** **Reset Value = xxxxh**
15	**Mask Internal IRQ15:** 0 = Disable; 1 = Enable.
14	**Mask Internal IRQ14:** 0 = Disable; 1 = Enable.
13	**Reserved:** Set to 0.
12	**Mask Internal IRQ12:** 0 = Disable; 1 = Enable.
11	**Mask Internal IRQ11:** 0 = Disable; 1 = Enable.
10	**Mask Internal IRQ10:** 0 = Disable; 1 = Enable.
9	**Mask Internal IRQ9:** 0 = Disable; 1 = Enable.
8	**Reserved:** Set to 0.
7	**Mask Internal IRQ7:** 0 = Disable; 1 = Enable.
6	**Reserved:** Set to 0.
5	**Mask Internal IRQ5:** 0 = Disable; 1 = Enable.
4	**Mask Internal IRQ4:** 0 = Disable; 1 = Enable.
3	**Mask Internal IRQ3:** 0 = Disable; 1 = Enable.
2:0	**Reserved:** Set to 0.

Table 5-21. F3BAR+Memory Offset xxh: XpressAUDIO™ Subsystem Configuration Registers (Contin-

Bit	Description
Offset 20h	**Audio Bus Master 0 Command Register (R/W)**	**Reset Value = 00h**
Audio Bus Master 0: Output to Codec; 32-Bit; Left and Right Channels; Slots 3 and 4.	
7:4	**Reserved:** Set to 0. Must return 0 on reads.
3	**Read or Write Control:** Set the transfer direction of Audio Bus Master 0. 0 = PCI reads performed; 1 = PCI writes performed. This bit must be set to 0 (read) and should not be changed when the bus master is active.
2:1	**Reserved:** Set to 0. Must return 0 on reads.
0	**Bus Master Control:** Controls the state of the Audio Bus Master 0. 0 = Disable; 1 = Enable. Setting this bit to 1 enables the bus master to begin data transfers. When writing this bit to 0, the bus master must either be paused or reach EOT. Writing this bit to 0 while the bus master is operating results in unpredictable behavior; including the possibility of the bus master state machine crashing. The only recovery from this condition is a PCI reset.
Note: Must be read and written as a BYTE.	
Offset 21h	**Audio Bus Master 0 SMI Status Register (RC)**	**Reset Value = 00h**
Audio Bus Master 0: Output to Codec; 32-Bit; Left and Right Channels; Slots 3 and 4.	
7:4	**Reserved (Read to Clear)**
1	**Bus Master Error (Read to Clear):** Hardware encountered a second EOP before software has cleared the first? 0 = No; 1 = Yes. If hardware encounters a second EOP (end of page) before software has cleared the first, it causes the bus master to pause until this register is read to clear the error.
0	**End of Page (Read to Clear):** Bus master transferred data which is marked by EOP bit in the PRD table (bit 30)? 0 = No; 1 = Yes.
Note: Must be read and written as a BYTE.	
Offset 22h-23h	**Reserved**	**Reset Value = xxh**
Offset 24h-27h	**Audio Bus Master 0 PRD Table Address (R/W)**	**Reset Value = 00000000h**
Audio Bus Master 0: Output to Codec; 32-Bit; Left and Right Channels; Slots 3 and 4.	
31:2	**Pointer to the Physical Region Descriptor Table:** This register is a PRD table pointer for Audio Bus Master 0. When written, this register points to the first entry in a PRD table. Once Audio Bus Master 0 is enabled (Command Register bit 0 = 1], it loads the pointer and updates this register to the next PRD by adding 08h. When read, this register points to the next PRD.
1:0	**Reserved:** Set to 0.
Offset 28h	**Audio Bus Master 1 Command Register (R/W)**	**Reset Value = 00h**
Audio Bus Master 1: Input from Codec; 32-Bit; Left and Right Channels; Slots 3 and 4.	
7:4	**Reserved:** Set to 0. Must return 0 on reads.
3	**Read or Write Control:** Set the transfer direction of Audio Bus Master 1. 0 = PCI reads performed; 1 = PCI writes performed. This bit must be set to 1 (write) and should not be changed when the bus master is active.
2:1	**Reserved:** Set to 0. Must return 0 on reads.
0	**Bus Master Control:** Controls the state of the Audio Bus Master 1. 0 = Disable; 1 = Enable. Setting this bit to 1 enables the bus master to begin data transfers. When writing this bit to 0, the bus master must be either paused or reached EOT. Writing this bit to 0 while the bus master is operating results in unpredictable behavior including the possibility of the bus master state machine crashing. The only recovery from this condition is a PCI reset.
Note: Must be read and written as a BYTE.	
Offset 29h	**Audio Bus Master 1 SMI Status Register (RC)**	**Reset Value = 00h**
Audio Bus Master 1: Input from Codec; 32-Bit; Left and Right Channels; Slots 3 and 4.	
7:2	**Reserved (Read to Clear)**
1	**Bus Master Error (Read to Clear):** Hardware encountered a second EOP before software has cleared the first? 0 = No; 1 = Yes. If hardware encounters a second EOP (end of page) before software has cleared the first, it causes the bus master to pause until this register is read to clear the error.

Table 5-21. F3BAR+Memory Offset xxh: XpressAUDIO™ Subsystem Configuration Registers (Contin-

Bit	Description
0	**End of Page (Read to Clear):** Bus master transferred data which is marked by EOP bit in the PRD table (bit 30)? 0 = No; 1 = Yes.
Note: Must be read and written as a BYTE.	
Offset 2Ah-2Bh	**Reserved** — **Reset Value = xxh**
Offset 2Ch-2Fh	**Audio Bus Master 1 PRD Table Address (R/W)** — **Reset Value = 00000000h**
Audio Bus Master 1: Input from Codec; 32-Bit; Left and Right Channels; Slots 3 and 4.	
31:2	**Pointer to the Physical Region Descriptor Table:** This register is a PRD table pointer for Audio Bus Master 1. When written, this register points to the first entry in a PRD table. Once Audio Bus Master 1 is enabled (Command Register bit 0 = 1], it loads the pointer and updates this register to the next PRD by adding 08h. When read, this register points to the next PRD.
1:0	**Reserved:** Set to 0.
Offset 30h	**Audio Bus Master 2 Command Register (R/W)** — **Reset Value = 00h**
Audio Bus Master 2: Output to Codec; 16-Bit; Slot 5.	
7:4	**Reserved:** Set to 0. Must return 0 on reads.
3	**Read or Write Control:** Set the transfer direction of Audio Bus Master 2. 0 = PCI reads performed; 1 = PCI writes performed. This bit must be set to 0 (read) and should not be changed when the bus master is active.
2:1	**Reserved:** Set to 0. Must return 0 on reads.
0	**Bus Master Control:** Controls the state of the Audio Bus Master 2. 0 = Disable; 1 = Enable. Setting this bit to 1 enables the bus master to begin data transfers. When writing this bit to 0, the bus master must be either paused or reached EOT. Writing this bit to 0 while the bus master is operating results in unpredictable behavior including the possibility of the bus master state machine crashing. The only recovery from this condition is a PCI reset.
Note: Must be read and written as a BYTE.	
Offset 31h	**Audio Bus Master 2 SMI Status Register (RC)** — **Reset Value = 00h**
Audio Bus Master 2: Output to Codec; 16-Bit; Slot 5.	
7:4	**Reserved (Read to Clear)**
1	**Bus Master Error (Read to Clear):** Hardware encountered a second EOP before software has cleared the first? 0 = No; 1 = Yes. If hardware encounters a second EOP (end of page) before software has cleared the first, it causes the bus master to pause until this register is read to clear the error.
0	**End of Page (Read to Clear):** Bus master transferred data which is marked by EOP bit in the PRD table (bit 30)? 0 = No; 1 = Yes.
Note: Must be read and written as a BYTE.	
Offset 32h-33h	**Reserved** — **Reset Value = xxh**
Offset 34h-37h	**Audio Bus Master 2 PRD Table Address (R/W)** — **Reset Value = 00000000h**
Audio Bus Master 2: Output to Codec; 16-Bit; Slot 5.	
31:2	**Pointer to the Physical Region Descriptor Table:** This register is a PRD table pointer for Audio Bus Master 2. When written, this register points to the first entry in a PRD table. Once Audio Bus Master 2 is enabled (Command Register bit 0 = 1], it loads the pointer and updates this register to the next PRD by adding 08h. When read, this register points to the next PRD.
1:0	**Reserved:** Set to 0.
Offset 38h	**Audio Bus Master 3 Command Register (R/W)** — **Reset Value = 00h**
Audio Bus Master 3: Input from Codec; 16-Bit; Slot 5.	
7:4	**Reserved:** Set to 0. Must return 0 on reads.
3	**Read or Write Control:** Set the transfer direction of Audio Bus Master 3. 0 = PCI reads performed; 1 = PCI writes performed. This bit must be set to 1 (write) and should not be changed when the bus master is active.
2:1	**Reserved:** Set to 0. Must return 0 on reads.

Table 5-21. F3BAR+Memory Offset xxh: XpressAUDIO™ Subsystem Configuration Registers (Contin-

Bit	Description
0	**Bus Master Control:** Controls the state of the Audio Bus Master 3. 0 = Disable; 1 = Enable. Setting this bit to 1 enables the bus master to begin data transfers. When writing this bit to 0, the bus master must be either paused or reached EOT. Writing this bit to 0 while the bus master is operating results in unpredictable behavior including the possibility of the bus master state machine crashing. The only recovery from this condition is a PCI reset.
Note: Must be read and written as a BYTE.	
Offset 39h	**Audio Bus Master 3 SMI Status Register (RC)** **Reset Value = 00h**
Audio Bus Master 3: Input from Codec; 16-Bit; Slot 5.	
7:4	**Reserved (Read to Clear)**
1	**Bus Master Error (Read to Clear):** Hardware encountered a second EOP before software has cleared the first? 0 = No; 1 = Yes. If hardware encounters a second EOP (end of page) before software has cleared the first, it causes the bus master to pause until this register is read to clear the error.
0	**End of Page (Read to Clear):** Bus master transferred data which is marked by EOP bit in the PRD table (bit 30)? 0 = No; 1 = Yes.
Note: Must be read and written as a BYTE.	
Offset 3Ah-3Bh	**Reserved** **Reset Value = xxh**
Offset 3Ch-3Fh	**Audio Bus Master 3 PRD Table Address (R/W)** **Reset Value = 00000000h**
Audio Bus Master 3: Input from Codec; 16-Bit; Slot 5.	
31:2	**Pointer to the Physical Region Descriptor Table:** This register is a PRD table pointer for Audio Bus Master 3. When written, this register points to the first entry in a PRD table. Once Audio Bus Master 3 is enabled (Command Register bit 0 = 1], it loads the pointer and updates this register to the next PRD by adding 08h. When read, this register points to the next PRD.
1:0	**Reserved:** Set to 0.
Offset 40h	**Audio Bus Master 4 Command Register (R/W)** **Reset Value = 00h**
Audio Bus Master 4: Output to Codec; 16-Bit; Slot 6 or 11 (F3BAR+Memory Offset 08h[19] selects slot).	
7:4	**Reserved:** Set to 0. Must return 0 on reads.
3	**Read or Write Control:** Set the transfer direction of Audio Bus Master 4. 0 = PCI reads performed; 1 = PCI writes performed. This bit must be set to 0 (read) and should not be changed when the bus master is active.
2:1	**Reserved:** Set to 0. Must return 0 on reads.
0	**Bus Master Control:** Controls the state of the Audio Bus Master 4. 0 = Disable; 1 = Enable. Setting this bit to 1 enables the bus master to begin data transfers. When writing this bit to 0, the bus master must be either paused or reached EOT. Writing this bit to 0 while the bus master is operating results in unpredictable behavior including the possibility of the bus master state machine crashing. The only recovery from this condition is a PCI reset.
Note: Must be read and written as a BYTE.	
Offset 41h	**Audio Bus Master 4 SMI Status Register (RC)** **Reset Value = 00h**
Audio Bus Master 4: Output to Codec; 16-Bit; Slot 6 or 11 (F3BAR+Memory Offset 08h[19] selects slot).	
7:4	**Reserved (Read to Clear)**
1	**Bus Master Error (Read to Clear):** Hardware encountered a second EOP before software has cleared the first? 0 = No; 1 = Yes. If hardware encounters a second EOP (end of page) before software has cleared the first, it causes the bus master to pause until this register is read to clear the error.
0	**End of Page (Read to Clear):** Bus master transferred data which is marked by EOP bit in the PRD table (bit 30)? 0 = No; 1 = Yes.
Note: Must be read and written as a BYTE.	
Offset 42h-43h	**Reserved** **Reset Value = xxh**

Table 5-21. F3BAR+Memory Offset xxh: XpressAUDIO™ Subsystem Configuration Registers (Contin-

Bit	Description
Offset 44h-47h	**Audio Bus Master 4 PRD Table Address (R/W)** **Reset Value = 00000000h**
Audio Bus Master 4: Output to Codec; 16-Bit; Slot 6 or 11 (F3BAR+Memory Offset 08h[19] selects slot).	
31:2	**Pointer to the Physical Region Descriptor Table:** This register is a PRD table pointer for Audio Bus Master 4. When written, this register points to the first entry in a PRD table. Once Audio Bus Master 4 is enabled (Command Register bit 0 = 1], it loads the pointer and updates this register to the next PRD by adding 08h. When read, this register points to the next PRD.
1:0	**Reserved:** Set to 0.
Offset 48h	**Audio Bus Master 5 Command Register (R/W)** **Reset Value = 00h**
Audio Bus Master 5: Input from Codec; 16-Bit; Slot 6 or 11 (F3BAR+Memory Offset 08h[20] selects slot).	
7:4	**Reserved:** Set to 0. Must return 0 on reads.
3	**Read or Write Control:** Set the transfer direction of Audio Bus Master 5. 0 = PCI reads performed; 1 = PCI writes performed. This bit must be set to 1 (write) and should not be changed when the bus master is active.
2:1	**Reserved:** Set to 0. Must return 0 on reads.
0	**Bus Master Control:** Controls the state of the Audio Bus Master 5. 0 = Disable; 1 = Enable. Setting this bit to 1 enables the bus master to begin data transfers. When writing this bit to 0, the bus master must be either paused or reached EOT. Writing this bit to 0 while the bus master is operating results in unpredictable behavior including the possibility of the bus master state machine crashing. The only recovery from this condition is a PCI reset.
Note: Must be read and written as a BYTE.	
Offset 49h	**Audio Bus Master 5 SMI Status Register (RC)** **Reset Value = 00h**
Audio Bus Master 5: Input from Codec; 16-Bit; Slot 6 or 11 (F3BAR+Memory Offset 08h[20] selects slot).	
7:4	**Reserved (Read to Clear)**
1	**Bus Master Error (Read to Clear):** Hardware encountered a second EOP before software has cleared the first? 0 = No; 1 = Yes. If hardware encounters a second EOP (end of page) before software has cleared the first, it causes the bus master to pause until this register is read to clear the error.
0	**End of Page (Read to Clear):** Bus master transferred data which is marked by EOP bit in the PRD table (bit 30)? 0 = No; 1 = Yes.
Note: Must be read and written as a BYTE.	
Offset 4Ah-4Bh	**Reserved** **Reset Value = xxh**
Offset 4Ch-4Fh	**Audio Bus Master 5 PRD Table Address (R/W)** **Reset Value = 00000000h**
Audio Bus Master 5: Input from Codec; 16-Bit; Slot 6 or 11 (F3BAR+Memory Offset 08h[20] selects slot).	
31:2	**Pointer to the Physical Region Descriptor Table:** This register is a PRD table pointer for Audio Bus Master 5. When written, this register points to the first entry in a PRD table. Once Audio Bus Master 5 is enabled (Command Register bit 0 = 1], it loads the pointer and updates this register to the next PRD by adding 08h. When read, this register points to the next PRD.
1:0	**Reserved:** Set to 0.
Offset 50h-FFh	**Reserved** **Reset Value = xxh**

5.3.5 Video Controller Registers - Function 4

The register space for the video controller is divided into two sections. The first section is used to configure the PCI portion of the controller. A Base Address Register at F4 Index 10h (F4BAR) points to the base address of where the second portion of the register space is located. The second section contains the registers used by the video controller to carry out video operations.

Table 5-22 shows the PCI header registers of F4. The memory mapped registers accessed through F4BAR, and shown in Table 5-23, must be accessed using DWORD operations. When writing to one of these 32-bit registers, all four bytes must be written.

If the F4 Video Configuration Trap bit (F0 Index 42h[1]) is set, access to the PCI header registers causes an SMI. Access through F4BAR is not affected by this bit.

Table 5-22. F4 Index xxh: PCI Header Registers for Video Controller Configuration

Bit	Description	
Index 00h-01h	**Vendor Identification Register (RO)**	**Reset Value = 1078h**
Index 02h-03h	**Device Identification Register (RO)**	**Reset Value = 0104h**
Index 04h-05h	**PCI Command Register (R/W)**	**Reset Value = 0000h**
15:2	**Reserved (Read Only)**	
1	**Memory Space:** Allow CS5530A to respond to memory cycles from the PCI bus. 0 = Disable; 1 = Enable. This bit must be enabled to access memory offsets through F4BAR (F4 Index 10h).	
0	**Reserved (Read Only)**	
Index 06h-07h	**PCI Status Register (RO)**	**Reset Value = 0280h**
Index 08h	**Device Revision ID Register (RO)**	**Reset Value = 00h**
Index 09h-0Bh	**PCI Class Code Register (RO)**	**Reset Value = 030000h**
Index 0Ch	**PCI Cache Line Size Register (RO)**	**Reset Value = 00h**
Index 0Dh	**PCI Latency Timer Register (RO)**	**Reset Value = 00h**
Index 0Eh	**PCI Header Type (RO)**	**Reset Value = 00h**
Index 0Fh	**PCI BIST Register (RO)**	**Reset Value = 00h**
Index 10h-13h	**Base Address Register - F4BAR (R/W)**	**Reset Value = 00000000h**
This register sets the base address of the memory mapped video controller registers. Bits [11:0] are read only (0000 0000 0000), indicating a 4 KB memory address range. Refer to Table 5-23 for the video controller register bit formats and reset values.		
31:12	**Video Controller and Clock Control Base I/O Address**	
11:0	**Address Range (Read Only)**	
Index 14h-3Fh	**Reserved**	**Reset Value = 00h**
Index 40h-FFh	**Reserved**	**Reset Value = xxh**

Table 5-23. F4BAR+Memory Offset xxh: Video Controller Configuration Registers

Bit	Description
Offset 00h-03h	**Video Configuration Register (R/W)** **Reset Value = 00000000h**
31	**Reserved:** Set to 0
30	**High Speed Timing for Video Interface:** High speed timings for the video interface. 0 = Disable; 1= Enable. If bit 30 is enabled, bit 25 should be set to 0.
29	**16-bit Video Interface:** Allow video interface to be 16 bits. 0 = Disable; 1= Enable. If bit 29 is enabled, 8 bits of pixel data is used for video. The 24-bit pixel data is then dithered to 16 bits. **Note:** F4BAR+Memory Offset 04h[25] should be set to the same value as this bit (bit 29).
28	**YUV 4:2:2 or 4:2:0 Mode:** 0 = 4:2:2 mode; 1= 4:2:0 mode. If 4:2:0 mode is selected, bits [3:2] should be set to 01 for 8-bit video mode and 10 for 16-bit video mode. **Note:** The GX1 processor does not support 4:2:0 mode.
27	**Video Line Size (DWORDs):** This is the MSB of the Video Line Size (DWORDs). See bits [15:8] for description.
26	**Reserved:** Set to 0
25	**Early Video Ready:** Generate VID_RDY output signal one-half VID_CLK period early to improve the speed of the video port operation. 0 = Disable; 1 = Enable. If bit 30 is enabled, this bit (bit 25) should be set to 0.
24	**Initial Buffer Read Address:** This is the MSB of the Initial Buffer Read Address. See bits [23:16] for description.
23:16	**Initial Buffer Read Address:** This field is used to preload the starting read address for the line buffers at the beginning of each display line. It is used for hardware clipping of the video window at the left edge of the active display. It represents the DWORD address of the source pixel which is to be displayed first. For an unclipped window, this value should be 0.
15:8	**Video Line Size (DWORDs):** This field represents the horizontal size of the source video data in DWORDs.
7	**Y Filter Enable:** Vertical filter. 0 = Disable; 1= Enable.
6	**X Filter Enable:** Horizontal filter. 0 = Disable; 1 = Enable.
5	**CSC Bypass:** Allows color-space-converter to be bypassed. Primarily used for displaying an RGB graphics overlay rather than a YUV video overlay. 0 = Overlay data passes through CSC; 1 = Overlay data bypasses CSC.
4	**GV Select:** Selects whether graphics or video data will be passed through the scaler hardware. 0 = Video data; 1 = Graphics data.
3:2	**Video Input Format:** This field defines the byte ordering of the video data on the VID_DATA bus. **8-Bit Mode (Value Byte Order [0:3])** 00 = U Y0 V Y1 (also used for RGB 5:6:5 input) 01 = Y1 V Y0 U or 4:2:0 10 = Y0 U Y1 V 11 = Y0 V Y1 U **16-Bit Mode (Value Byte Order [0:3])** 00 = U Y0 V Y1 (also used for RGB 5:6:5 input) 01 = Y0 U Y1 V 10 = Y1 V Y0 U or 4:2:0 11 = Reserved If bit 28 is set for 4:2:0 mode, these bits (bits [3:2]) should be set to 01 for 8-bit video mode and 10 for 16-bit video mode. **Note:** U = Cb, V = Cr
1	**Video Register Update:** Allow video position and scale registers to be updated simultaneously on next occurrence of vertical sync. 0 = Disable; 1 = Enable.
0	**Video Enable:** Video acceleration hardware. 0 = Disable; 1 = Enable.

Table 5-23. F4BAR+Memory Offset xxh: Video Controller Configuration Registers (Continued)

Bit	Description
Offset 04h-07h	**Display Configuration Register (R/W)** — **Reset Value = 00000000h**
31	**DDC Input Data (Read Only):** This is the DDC input data bit for reads.
30:28	**Reserved:** Set to 0.
27	**Flat Panel On (Read Only):** This bit indicates whether the attached flat panel display is powered on or off. The bit transitions at the end of the power-up or power-down sequence. 0 = Off; 1 = On.
26	**Reserved:** Set to 0.
25	**16-Bit Graphics Enable:** This bit works in conjunction with the 16-bit Video Interface bit at F4BAR+Memory Offset 00h[29]. This bit should be set to the same value as the 16-bit Video Interface bit.
24	**DDC Output Enable:** This bit enables the DDC_SDA line to be driven for write data. 0 = DDC_SDA (pin M4) is an input; 1 = DDC_SDA (pin M4) is an output.
23	**DDC Output Data:** This is the DDC data bit.
22	**DDC Clock:** This is the DDC clock bit. It is used to clock the DDC_SDA bit.
21	**Palette Bypass:** Selects whether graphics or video data should bypass the gamma RAM. 0 = Video data; 1 = Graphics data.
20	**Video/Graphics Color Key Select:** Selects whether the video or graphics data stream will be used for color/chroma keying. 0 = Graphics data is compared to color key; 1 = Video data is compared to color key.
19:17	**Power Sequence Delay:** This field selects the number of frame periods that transpire between successive transitions of the power sequence control lines. Valid values are 001 to 111.
16:14	**CRT Sync Skew:** This 3-bit field represents the number of pixel clocks to skew the horizontal and vertical syncs that are sent to the CRT. This field should be programmed to 100 as the baseline. The syncs may be moved forward or backward relative to the pixel data via this register. It is used to compensate for the pipeline delay through the graphics pipeline.
13	**Flat Panel Dither Enable:** This bit enables flat panel dithering. It enables 24 bpp display data to be approximated with an 18-bit flat panel display. 0 = Disable; 1 = Enable.
12	**XGA Flat Panel:** This bit enables the FP_CLK_ EVEN output signal which can be used to demultiplex the FP_DATA bus into even and odd pixels. 0 = Standard flat panel; 1 = XGA flat panel.
11	**Flat Panel Vertical Synchronization Polarity:** Selects the flat panel vertical sync polarity. 0 = FP vertical sync is normally low, transitioning high during sync interval. 1 = FP vertical sync is normally high, transitioning low during sync interval.
10	**Flat Panel Horizontal Synchronization Polarity:** Selects the flat panel horizontal sync polarity. 0 = FP horizontal sync is normally low, transitioning high during sync interval. 1 = FP horizontal sync is normally high, transitioning low during sync interval.
9	**CRT Vertical Synchronization Polarity:** Selects the CRT vertical sync polarity. 0 = CRT vertical sync is normally low, transitioning high during sync interval. 1 = CRT vertical sync is normally high, transitioning low during sync interval.
8	**CRT Horizontal Synchronization Polarity:** Selects the CRT horizontal sync polarity. 0 = CRT horizontal sync is normally low, transitioning high during sync interval. 1 = CRT horizontal sync is normally high, transitioning low during sync interval.
7	**Flat Panel Data Enable:** Enables the flat panel data bus. 0 = FP_DATA [17:0] is forced low; 1 = FP_DATA [17:0] is driven based upon power sequence control.
6	**Flat Panel Power Enable:** The transition of this bit initiates a flat panel power-up or power-down sequence. 0 -> 1 = Power-up flat panel; 1 -> 0 = Power-down flat panel.
5	**DAC Power-Down (active low):** This bit must be set to power-up the video DACs. It can be cleared to power-down the video DACs when not in use. 0 = DACs are powered down; 1 = DACs are powered up.
4	**Reserved:** Set to 0.
3	**DAC Blank Enable:** This bit enables the blank to the video DACs. 0 = DACs are constantly blanked; 1 = DACs are blanked normally.
2	**CRT Vertical Sync Enable:** Enables the CRT vertical sync. Used for VESA DPMS support. 0 = Disable; 1 = Enable.
1	**CRT Horizontal Sync Enable:** Enables the CRT horizontal sync. Used for VESA DPMS support. 0 = Disable; 1 = Enable.
0	**Display Enable:** Enables the graphics display pipeline. It is used as a reset for the display control logic. 0 = Reset display control logic; 1 = Enable display control logic.

Table 5-23. F4BAR+Memory Offset xxh: Video Controller Configuration Registers (Continued)

Bit	Description
Offset 08h-0Bh	**Video X Register (R/W)** — **Reset Value = xxxxxxxxh**
31:27	**Reserved:** Set to 0.
26:16	**Video X End Position:** This field represents the horizontal end position of the video window according to the following formula. Position programmed = screen position + (H_TOTAL – H_SYNC_END) – 13.
15:11	**Reserved:** Set to 0.
10:0	**Video X Start Position:** This field represents the horizontal start position of the video window according to the following formula. Position programmed = screen position + (H_TOTAL – H_SYNC_END) – 13.
Offset 0Ch-0Fh	**Video Y Register (R/W)** — **Reset Value = xxxxxxxxh**
31:27	**Reserved:** Set to 0.
26:16	**Video Y End Position:** This field represents the vertical end position of the video window according to the following formula. Position programmed = screen position + (V_TOTAL – V_SYNC_END) + 1.
15:11	**Reserved:** Set to 0.
10:0	**Video Y Start Position:** This field represents the vertical start position of the video window according to the following formula. Position programmed = screen position + (V_TOTAL – V_SYNC_END) + 1.
Offset 10h-13h	**Video Scale Register (R/W)** — **Reset Value = xxxxxxxxh**
31:30	**Reserved:** Set to 0.
29:16	**Video Y Scale Factor:** This field represents the video window vertical scale factor according to the following formula. VID_Y_SCL = 8192 * (Ys - 1) / (Yd - 1) Where: Ys = Video source vertical size in lines Yd = Video destination vertical size in lines
15:14	**Reserved:** Set to 0.
13:0	**Video X Scale Factor:** This field represents the video window horizontal scale factor according to the following formula. VID_X_SCL = 8192 * (Xs - 1) / (Xd - 1) Where: Xs = Video source horizontal size in pixels Xd = Video destination horizontal size in pixels
Offset 14h-17h	**Video Color Key Register (R/W)** — **Reset Value = xxxxxxxxh**
31:24	**Reserved:** Set to 0.
23:0	**Video Color Key:** This field represents the video color key. It is a 24-bit RGB value. The graphics or video data being compared may be masked prior to the compare by programming the Video Color Mask Register (F4BAR+Memory Offset 18h) appropriately.
Offset 18h-1Bh	**Video Color Mask Register (R/W)** — **Reset Value = xxxxxxxxh**
31:24	**Reserved:** Set to 0.
23:0	**Video Color Mask:** This field represents the video color mask. It is a 24-bit RGB value. Zeroes in the mask cause the corresponding bits in the graphics or video stream being compared to be ignored.
Offset 1Ch-1Fh	**Palette Address Register (R/W)** — **Reset Value = xxxxxxxxh**
31:8	**Reserved:** Set to 0.
7:0	**Palette Address:** The value programmed is used to initialize the palette address counter.
Offset 20h-23h	**Palette Data Register (R/W)** — **Reset Value = xxxxxxxxh**
31:24	**Reserved:** Set to 0.
23:0	**Palette Data:** This register contains the read or write data for a Gamma RAM access.

Table 5-23. F4BAR+Memory Offset xxh: Video Controller Configuration Registers (Continued)

Bit	Description
Offset 24h-27h	**DOT Clock Configuration Register (R/W)** — **Reset Value = 00000000h**
31	**Feedback Reset:** Reset the PLL postscaler and feedback divider. 0 = Normal operation; 1 = Reset. A more comprehensive reset description is provided in bit 8.
30	**Half Clock:** 0 = Enable; 1 = Disable. For odd post divisors, half clock enables the falling edge of the VCO clock to be used to generate the falling edge of the post divider output to more closely approximate a 50% output duty cycle.
29	**Reserved:** Set to 0.
28:24	**5-Bit DCLK PLL Post Divisor (PD) Value:** Selects value of 1 to 31. 00000 = PD divisor of 8 — 01000 = PD divisor of 10 — 10000 = PD divisor of 9 — 11000 = PD divisor of 11 00001 = PD divisor of 6 — 01001 = PD divisor of 20 — 10001 = PD divisor of 7 — 11001 = PD divisor of 21 00010 = PD divisor of 18 — 01010 = PD divisor of 14 — 10010 = PD divisor of 19 — 11010 = PD divisor of 15 00011 = PD divisor of 4 — 01011 = PD divisor of 26 — 10011 = PD divisor of 5 — 11011 = PD divisor of 27 00100 = PD divisor of 12 — 01100 = PD divisor of 22 — 10100 = PD divisor of 13 — 11100 = PD divisor of 23 00101 = PD divisor of 16 — 01101 = PD divisor of 28 — 10101 = PD divisor of 17 — 11101 = PD divisor of 29 00110 = PD divisor of 24 — 01110 = PD divisor of 30 — 10110 = PD divisor of 25 — 11110 = PD divisor of 31 00111 = PD divisor of 2 — 01111 = PD divisor of 1* — 10111 = PD divisor of 3 — 11111 = Reserved *See bit 11 description.
23	**Plus 1 (+1):** Adds 1 or 0 to FD (DCLK PLL VCO Feedback Divisor) parameter in equation (see Note). 0 = Add 0 to FD; 1 = Add 1 to FD.
22:12	**N:** This bit represents “N” in the equation (see Note). It is used to solve the value of FD (DCLK PLL VCO feedback divisor). N can be a value of 1 to 400. For all values of N, refer to Table 5-24 on page 204.
11	**CLK_ON:** 0 = PLL disable; 1 = PLL enable. If PD = 1 (i.e., bits [28:24] = 01111) the PLL is always enabled and cannot be disabled by this bit.
10	**DOT Clock Select:** 0 = DCLK; 1 = TV_CLK.
9	**Reserved:** Set to 0
8	**Bypass PLL:** Connects the input of the PLL directly to the output of the PLL. 0 = Normal Operation; 1 = Bypass PLL. If this bit is set to 1, the input of the PLL bypasses the PLL and resets the VCO control voltage, which in turn powers down the PLL. Allow 0.5 ms for the control voltage to be driven to 0V.
7:6	**Reserved:** Set to 0.
5	**Reserved (Read Only):** Write as read
4:3	**Reserved:** Set to 0.
2:0	**PLL Input Divide (ID) Value:** Selects value of 2 to 9 (see Note). 000 = ID divisor of 2 — 100 = ID divisor of 6 — 001 = ID divisor of 3 — 101 = ID divisor of 7 010 = ID divisor of 4 — 110 = ID divisor of 8 — 011 = ID divisor of 5 — 111 = ID divisor of 9

Note: To calculate DCLK output frequency:

Equation #1: DCLK = [CLK_14MHZ * FD] ÷ [PD *ID]
Condition: 140 MHz < [DCLK * PD] < 300 MHz

Where: CLK_14MHZ is pin P24
FD is derived from N see equation #2 and #3
PD is derived from bits [28:24]
ID is derived from bits [2:0]

Equation #2: If FD is an odd number then: FD = 2*N +1
Equation #3: If FD is an even number then: FD = 2*N +0

Where: N is derived from bits [22:12]
+1 is achieved by setting bit 23 to 1.
+0 is achieved by clearing bit 23 to 0.

Table 5-23. F4BAR+Memory Offset xxh: Video Controller Configuration Registers (Continued)

Bit	Description
Offset 28h-2Bh	**CRC Signature and TFT/TV Configuration Register (R/W)** **Reset Value = 00000100h**
31:8	**24-Bit Video Signature Data (Read Only)**
7	**SYNC Override:** Drive VSYNC_OUT on FP_VSYNC_OUT and HSYNC_OUT on FP_HSYNC_OUT. 0 = Disable; 1 = Enable.
6	**Invert FP_CLK:** 0 = Disable; 1 = Enable. (Applicable for TV not TFT.)
5	**Invert FP_CLK_EVEN:** 0 = Disable; 1 = Enable.
4	**Reserved (Read Only)**
3	**Signature Source Select:** 0 = RGB data; 1 = FP data. (FP data occupies the top 6 bits of each color byte to the signature, with the bottom two bits always zero.)
2	**Signature Free Run:** 0 = Disable; 1 = Enable. When high, with the signature enabled, the signature generator captures data continuously across multiple frames. This bit may be set high when the signature is started, then later set low, which causes the signature generation process to stop at the end of the current frame.
1	**FP_HSYNC_OUT Delay:** 0 = Disable; 1 = Enable. (Applicable for TFT not TV.) When SYNC Override (bit 7) is high, this bit (bit 1) can be set high to delay FP_HSYNC_OUT by an extra two clock cycles. When the SYNC Override (bit 7) is low, this bit should also be set low.
0	**Signature Enable:** 0 = Disable; 1= Enable. When low, the signature register is reset to 000001h and held (no capture). When high, the signature register captures the pixel data signature with each pixel clock beginning with the next vsync.
Offset 2Ch-FFh	**Reserved** **Reset Value = xxh**

Table 5-24. F4BAR+Memory Offset 24h[22:12] Decode (Value of "N")

N	Reg. Value
400	33A
399	674
398	4E8
397	1D0
396	3A0
395	740
394	681
393	502
392	205
391	40B
390	16
389	2D
388	5B
387	B7
386	16F
385	2DE
384	5BD
383	37B
382	6F6
381	5EC
380	3D9
379	7B2
378	765
377	6CB
376	596
375	32D
374	65A
373	4B4
372	168
371	2D0
370	5A1
369	343
368	686
367	50C
366	219
365	433
364	66
363	CD
362	19B
361	336
360	66C
359	4D8
358	1B0
357	360
356	6C0
355	580
354	301
353	602
352	404
351	8
350	11

N	Reg. Value
349	23
348	47
347	8F
346	11F
345	23E
344	47D
343	FA
342	1F5
341	3EA
340	7D4
339	7A9
338	753
337	6A7
336	54E
335	29D
334	53B
333	277
332	4EF
331	1DE
330	3BC
329	778
328	6F1
327	5E2
326	3C5
325	78A
324	715
323	62B
322	456
321	AC
320	159
319	2B2
318	565
317	2CB
316	597
315	32F
314	65E
313	4BC
312	178
311	2F0
310	5E1
309	3C3
308	786
307	70D
306	61B
305	436
304	6C
303	D9
302	1B3
301	366
300	6CC
299	598

N	Reg. Value
298	331
297	662
296	4C4
295	188
294	310
293	620
292	440
291	80
290	101
289	202
288	405
287	A
286	15
285	2B
284	57
283	AF
282	15F
281	2BE
280	57D
279	2FB
278	5F7
277	3EF
276	7DE
275	7BD
274	77B
273	6F7
272	5EE
271	3DD
270	7BA
269	775
268	6EB
267	5D6
266	3AD
265	75A
264	6B5
263	56A
262	2D5
261	5AB
260	357
259	6AE
258	55C
257	2B9
256	573
255	2E7
254	5CF
253	39F
252	73E
251	67D
250	4FA
249	1F4
248	3E8

N	Reg. Value
247	7D0
246	7A1
245	743
244	687
243	50E
242	21D
241	43B
240	76
239	ED
238	1DB
237	3B6
236	76C
235	6D9
234	5B2
233	365
232	6CA
231	594
230	329
229	652
228	4A4
227	148
226	290
225	521
224	243
223	487
222	10E
221	21C
220	439
219	72
218	E5
217	1CB
216	396
215	72C
214	659
213	4B2
212	164
211	2C8
210	591
209	323
208	646
207	48C
206	118
205	230
204	461
203	C2
202	185
201	30A
200	614
199	428
198	50
197	A1

N	Reg. Value
196	143
195	286
194	50D
193	21B
192	437
191	6E
190	DD
189	1BB
188	376
187	6EC
186	5D8
185	3B1
184	762
183	6C5
182	58A
181	315
180	62A
179	454
178	A8
177	151
176	2A2
175	545
174	28B
173	517
172	22F
171	45F
170	BE
169	17D
168	2FA
167	5F5
166	3EB
165	7D6
164	7AD
163	75B
162	6B7
161	56E
160	2DD
159	5BB
158	377
157	6EE
156	5DC
155	3B9
154	772
153	6E5
152	5CA
151	395
150	72A
149	655
148	4AA
147	154
146	2A8

N	Reg. Value
145	551
144	2A3
143	547
142	28F
141	51F
140	23F
139	47F
138	FE
137	1FD
136	3FA
135	7F4
134	7E9
133	7D3
132	7A7
131	74F
130	69F
129	53E
128	27D
127	4FB
126	1F6
125	3EC
124	7D8
123	7B1
122	763
121	6C7
120	58E
119	31D
118	63A
117	474
116	E8
115	1D1
114	3A2
113	744
112	689
111	512
110	225
109	44B
108	96
107	12D
106	25A
105	4B5
104	16A
103	2D4
102	5A9
101	353
100	6A6
99	54C
98	299
97	533
96	267
95	4CF

N	Reg. Value
94	19E
93	33C
92	678
91	4F0
90	1E0
89	3C0
88	780
87	701
86	603
85	406
84	C
83	19
82	33
81	67
80	CF
79	19F
78	33E
77	67C
76	4F8
75	1F0
74	3E0
73	7C0
72	781
71	703
70	607
69	40E
68	1C
67	39
66	73
65	E7
64	1CF
63	39E
62	73C
61	679
60	4F2
59	1E4
58	3C8
57	790
56	721
55	643
54	486
53	10C
52	218
51	431
50	62
49	C5
48	18B
47	316
46	62C
45	458
44	B0

N	Reg. Value
43	161
42	2C2
41	585
40	30B
39	616
38	42C
37	58
36	B1
35	163
34	2C6
33	58D
32	31B
31	636
30	46C
29	D8
28	1B1
27	362
26	6C4
25	588
24	311
23	622
22	444
21	88
20	111
19	222
18	445
17	8A
16	115
15	22A
14	455
13	AA
12	155
11	2AA
10	555
9	2AB
8	557
7	2AF
6	55F
5	2BF
4	57F
3	2FF
2	5FF
1	3FF

5.4 USB Registers

The USB Host Controller exists logically as its own PCI "Device", separate from the Chipset functions. It is a single-function device, and so it contains a PCI Configuration space for only Function 0. Depending on the state of the HOLD_REQ# pin on reset, the USB Controller will respond to one of two Device numbers for access to its PCI Configuration registers:

HOLD_REQ# low: Responds to pin AD29 high (Device 13h in a Geode system).

HOLD_REQ# high: Responds to pin AD27 high (Device 11h in a Geode system).

The PCI Configuration registers are listed in Table 5-25. They can be accessed as any number of bytes within a single 32-bit aligned unit. They are selected by the PCI-standard Index and Byte-Enable method. Registers marked as "Reserved", and reserved bits within a register, should not be changed by software.

In the PCI Configuration space, there is one Base Address Register (BAR), at Index 10h, which is used to map the USB Host Controller's operational register set into a 4K memory space. Once the BAR register has been initialized, and the PCI Command register at Index 04h has been set to enable the Memory space decoder, these "USB Controller" registers are accessible.

The memory-mapped USB Controller Registers are listed in Table 5-26. They follow the Open Host Controller Interface (OHCI) specification.

Table 5-25. USB Index xxh: USB PCI Configuration Registers

Bit	Description
Index 00h-01h	**Vendor Identification Register (RO)** — **Reset Value = 0E11h**
Index 02h-03h	**Device Identification Register (RO)** — **Reset Value = A0F8h**
Index 04h-05h	**Command Register (R/W)** — **Reset Value = 0000h**
15:10	**Reserved:** Set to 0.
9	**Fast Back-to-Back Enable (Read Only):** USB only acts as a master to a single device, so this functionality is not needed. It is always disabled (must always be set to 0).
8	**SERR#:** USB asserts SERR# when it detects an address parity error. 0 = Disable; 1 = Enable.
7	**Wait Cycle Control:** USB does not need to insert a wait state between the address and data on the AD lines. It is always disabled (bit is set to 0).
6	**Parity Error:** USB asserts PERR# when it is the agent receiving data and it detects a data parity error. 0 = Disable; 1 = Enable.
5	**VGA Palette Snoop Enable (Read Only):** USB does not support this function. It is always disabled (bit is set to 0).
4	**Memory Write and Invalidate:** Allow USB to run Memory Write and Invalidate commands. 0 = Disable; 1 = Enable. The Memory Write and Invalidate command will only occur if the cache line size is set to 32 bytes and the memory write is exactly one cache line. If the CS5530A is being used in a GX1 processor based system, this bit must be set to 0.
3	**Special Cycles:** USB does not run special cycles on PCI. It is always disabled (bit is set to 0).
2	**PCI Master Enable:** Allow USB to run PCI master cycles. 0 = Disable; 1 = Enable.
1	**Memory Space:** Allow USB to respond as a target to memory cycles. 0 = Disable; 1 = Enable.
0	**I/O Space:** Allow USB to respond as a target to I/O cycles. 0 = Disable; 1 = Enable.
Index 06h-07h	**Status Register (R/W)** — **Reset Value = 0280h**
15	**Detected Parity Error:** This bit is set whenever the USB detects a parity error, even if the Parity Error (response) detection enable bit (PCIUSB 04h[6]) is disabled. Write 1 to clear.
14	**SERR# Status:** This bit is set whenever the USB detects a PCI address error. Write 1 to clear.
13	**Received Master Abort Status:** This bit is set when the USB, acting as a PCI master, aborts a PCI bus memory cycle. Write 1 to clear.
12	**Received Target Abort Status:** This bit is set when a USB generated PCI cycle (USB is the PCI master) is aborted by a PCI target. Write 1 to clear.
11	**Signaled Target Abort Status:** This bit is set whenever the USB signals a target abort. Write 1 to clear.
10:9	**DEVSEL# Timing (Read Only):** These bits indicate the DEVSEL# timing when performing a positive decode. Since DEVSEL# is asserted to meet the medium timing, these bits are encoded as 01b.
8	**Data Parity Reported:** Set to 1 if the Parity Error Response bit (Command Register bit 6) is set, and USB detects PERR# asserted while acting as PCI master (whether PERR# was driven by USB or not).

Table 5-25. USB Index xxh: USB PCI Configuration Registers (Continued)

Bit	Description
7	**Fast Back-to-Back Capable (Read Only):** USB does support fast back-to-back transactions when the transactions are not to the same agent. This bit is always 1.
6:0	**Reserved:** Set to 0.
Note: The PCI specification defines this register to record status information for PCI related events. This is a read/write register. However, writes can only reset bits. A bit is reset whenever the register is written and the data in the corresponding bit location is a 1.	
Index 08h — **Device Revision ID Register (RO)** — **Reset Value = 06h**	
Index 09h-0Bh — **PCI Class Code Register (RO)** — **Reset Value = 0C0310h**	
This register identifies this function as an OpenHCI device. The base class is 0Ch (serial bus controller). The sub class is 03h (universal serial bus). The programming interface is 10h (OpenHCI).	
Index 0Ch — **Cache Line Size Register (R/W)** — **Reset Value = 00h**	
This register identifies the system cache line size in units of 32-bit WORDs. The USB only stores the value of bit 3 in this register since the cache line size of 32 bytes is the only value applicable to the design. Any value other than 08h written to this register is read back as 00h. In a CS5530A/GX1 processor based system this register must be set to 00h since the GX1 processor has a 16-byte cache line size.	
Index 0Dh — **Latency Timer Register (R/W)** — **Reset Value = 00h**	
This register identifies the value of the latency timer in PCI clocks for PCI bus master cycles.	
Index 0Eh — **Header Type Register (RO)** — **Reset Value = 00h**	
This register identifies the type of the predefined header in the configuration space. Since the USB is a single function device and not a PCI-to-PCI bridge, this byte should be read as 00h.	
Index 0Fh — **BIST Register (RO)** — **Reset Value = 00h**	
This register identifies the control and status of Built In Self Test. The USB does not implement BIST, so this register is read only.	
Index 10h-13h — **Base Address Register (R/W)** — **Reset Value = 00000000h**	
This BAR sets the base address of the memory mapped USB controller registers. Bits [11:0] are read only (0000 0000 0000), indicating a 4 KB memory address range. Refer to Table 5-26 for the USB controller register bit formats and reset values.	
31:12	**USB Controller Base Address**
11:0	**Address Range (Read Only)**
Index 14h-3Bh — **Reserved** — **Reset Value = xxh**	
Index 3Ch — **Interrupt Line Register (R/W)** — **Reset Value = 00h**	
This register identifies which of the system interrupt controllers the devices interrupt pin is connected to. The value of this register is used by device drivers and has no direct meaning to the USB.	
Index 3Dh — **Interrupt Pin Register (RO)** — **Reset Value = 01h**	
This register identifies which interrupt pin a device uses. Since the USB uses INTA#, this value is set to 01h.	
Index 3Eh — **Min. Grant Register (RO)** — **Reset Value = 00h**	
This register specifies the desired settings for how long of a burst the USB needs assuming a clock rate of 33 MHz. The value specifies a period of time in units of 1/4 microsecond.	
Index 3Fh — **Max. Latency Register (RO)** — **Reset Value = 50h**	
This register specifies the desired settings for how often the USB needs access to the PCI bus assuming a clock rate of 33 MHz. The value specifies a period of time in units of 1/4 microsecond.	
Index 40h-43h — **ASIC Test Mode Enable Register (R/W)** — **Reset Value = 000F0000h**	
Used for internal debug and test purposes only.	
Index 44h-45h — **ASIC Operational Mode Enable Register (R/W)** — **Reset Value = 0000h**	
15:9	**Reserved:** Read/Write 0s.
8	**SIE Pipeline Disable:** When set, waits for all USB bus activity to complete prior to returning completion status to the List Processor. This is a fail-safe mechanism to avoid potential problems with the clk_dr transition between 1.5 MHz and 12 MHz.
7:1	**Write Only:** Read as 0s.
0	**Data Buffer Region 16:** When set, the size of the region for the data buffer is 16 bytes. Otherwise, the size is 32 bytes.

Table 5-25. USB Index xxh: USB PCI Configuration Registers (Continued)

Bit	Description	
Index 46h-47h	Reserved	Reset Value = 00h
Index 48h-FFh	Reserved	Reset Value = xxh

Table 5-26. USB BAR+Memory Offset xxh: USB Controller Registers

Bit	Description
Offset 00h-03h	**HcRevision Register (RO)** — **Reset Value = 00000110h**
31:8	**Reserved:** Read/Write 0s.
7:0	**Revision (Read Only):** Indicates the Open HCI Specification revision number implemented by the Hardware. USB supports 1.0 specification. (X.Y = XYh).
Offset 04h-07h	**HcControl Register (R/W)** — **Reset Value = 00000000h**
31:11	**Reserved:** Read/Write 0s.
10	**RemoteWakeupConnectedEnable:** If a remote wakeup signal is supported, this bit enables that operation. Since there is no remote wakeup signal supported, this bit is ignored.
9	**RemoteWakeupConnected (Read Only):** This bit indicated whether the HC supports a remote wakeup signal. This implementation does not support any such signal. The bit is hard-coded to 0.
8	**InterruptRouting:** This bit is used for interrupt routing: 0 = Interrupts routed to normal interrupt mechanism (INT); 1 = Interrupts routed to SMI.
7:6	**HostControllerFunctionalState:** This field sets the HC state. The HC may force a state change from UsbSuspend to UsbResume after detecting resume signaling from a downstream port. States are: 00 = UsbReset 01 = UsbResume 10 = UsbOperational 11 = UsbSuspend
5	**BulkListEnable:** When set, this bit enables processing of the Bulk list.
4	**ControlListEnable:** When set, this bit enables processing of the Control list.
3	**IsochronousEnable:** When clear, this bit disables the Isochronous List when the Periodic List is enabled (so Interrupt EDs may be serviced). While processing the Periodic List, the HC will check this bit when it finds an isochronous ED.
2	**PeriodicListEnable:** When set, this bit enables processing of the Periodic (interrupt and isochronous) list. The HC checks this bit prior to attempting any periodic transfers in a frame.
1:0	**ControlBulkServiceRatio:** Specifies the number of Control Endpoints serviced for every Bulk Endpoint. Encoding is N-1 where N is the number of Control Endpoints (i.e., 00 = 1 Control Endpoint; 11 = 3 Control Endpoints).
Offset 08h-0Bh	**HcCommandStatus Register (R/W)** — **Reset Value = 00000000h**
31:18	**Reserved:** Read/Write 0s.
17:16	**ScheduleOverrunCount:** This field increments every time the SchedulingOverrun bit in HcInterruptStatus is set. The count wraps from 11 to 00.
15:4	**Reserved:** Read/Write 0s.
3	**OwnershipChangeRequest:** When set by software, this bit sets the OwnershipChange field in HcInterruptStatus. The bit is cleared by software.
2	**BulkListFilled:** Set to indicate there is an active ED on the Bulk List. The bit may be set by either software or the HC and cleared by the HC each time it begins processing the head of the Bulk List.
1	**ControlListFilled:** Set to indicate there is an active ED on the Control List. It may be set by either software or the HC and cleared by the HC each time it begins processing the head of the Control List.
0	**HostControllerReset:** This bit is set to initiate a software reset. This bit is cleared by the HC upon completion of the reset operation.
Offset 0Ch-0Fh	**HcInterruptStatus Register (R/W)** — **Reset Value = 00000000h**
31	**Reserved:** Read/Write 0s.
30	**OwnershipChange:** This bit is set when the OwnershipChangeRequest bit of HcCommandStatus is set.
29:7	**Reserved:** Read/Write 0s.
6	**RootHubStatusChange:** This bit is set when the content of HcRhStatus or the content of any HcRhPortStatus register has changed.
5	**FrameNumberOverflow:** Set when bit 15 of FrameNumber changes value.
4	**UnrecoverableError (Read Only):** This event is not implemented and is hard-coded to 0. Writes are ignored.
3	**ResumeDetected:** Set when HC detects resume signaling on a downstream port.
2	**StartOfFrame:** Set when the Frame Management block signals a Start of Frame event.
1	**WritebackDoneHead:** Set after the HC has written HcDoneHead to HccaDoneHead.

Table 5-26. USB BAR+Memory Offset xxh: USB Controller Registers (Continued)

Bit	Description
0	**SchedulingOverrun:** Set when the List Processor determines a Schedule Overrun has occurred.
Note: All bits are set by hardware and cleared by software.	
Offset 10h-13h	**HcInterruptEnable Register (R/W)** **Reset Value = 00000000h**
31	**MasterInterruptEnable:** This bit is a global interrupt enable. A write of 1 allows interrupts to be enabled via the specific enable bits listed above.
30	**OwnershipChangeEnable:** 0 = Ignore; 1 = Enable interrupt generation due to Ownership Change.
29:7	**Reserved:** Read/Write 0s.
6	**RootHubStatusChangeEnable:** 0 = Ignore; 1 = Enable interrupt generation due to Root Hub Status Change.
5	**FrameNumberOverflowEnable:** 0 = Ignore; 1 = Enable interrupt generation due to Frame Number Overflow.
4	**UnrecoverableErrorEnable:** This event is not implemented. All writes to this bit are ignored.
3	**ResumeDetectedEnable:** 0 = Ignore; 1 = Enable interrupt generation due to Resume Detected.
2	**StartOfFrameEnable:** 0 = Ignore; 1 = Enable interrupt generation due to Start of Frame.
1	**WritebackDoneHeadEnable:** 0 = Ignore; 1 = Enable interrupt generation due to Writeback Done Head.
0	**SchedulingOverrunEnable:** 0 = Ignore; 1 = Enable interrupt generation due to Scheduling Overrun.
Note: Writing a 1 to a bit in this register sets the corresponding bit, while writing a 0 leaves the bit unchanged.	
Offset 14h-17h	**HcInterruptDisable Register (R/W)** **Reset Value = C000006Fh**
31	**MasterInterruptEnable:** Global interrupt disable. A write of 1 disables all interrupts.
30	**OwnershipChangeEnable:** 0 = Ignore; 1 = Disable interrupt generation due to Ownership Change.
29:7	**Reserved:** Read/Write 0s.
6	**RootHubStatusChangeEnable:** 0 = Ignore; 1 = Disable interrupt generation due to Root Hub Status Change.
5	**FrameNumberOverflowEnable:** 0 = Ignore; 1 = Disable interrupt generation due to Frame Number Overflow.
4	**UnrecoverableErrorEnable:** This event is not implemented. All writes to this bit will be ignored.
3	**ResumeDetectedEnable:** 0 = Ignore; 1 = Disable interrupt generation due to Resume Detected.
2	**StartOfFrameEnable:** 0 = Ignore; 1 = Disable interrupt generation due to Start of Frame.
1	**WritebackDoneHeadEnable:** 0 = Ignore; 1 = Disable interrupt generation due to Writeback Done Head.
0	**SchedulingOverrunEnable:** 0 = Ignore; 1 = Disable interrupt generation due to Scheduling Overrun.
Note: Writing a 1 to a bit in this register clears the corresponding bit, while writing a 0 to a bit leaves the bit unchanged.	
Offset 18h-1Bh	**HcHCCA Register (R/W)** **Reset Value = 00000000h**
31:8	**HCCA:** Pointer to HCCA base address.
7:0	**Reserved:** Read/Write 0s.
Offset 1Ch-1Ch	**HcPeriodCurrentED Register (R/W)** **Reset Value = 00000000h**
31:4	**PeriodCurrentED:** Pointer to the current Periodic List ED.
3:0	**Reserved:** Read/Write 0s.
Offset 20h-23h	**HcControlHeadED Register (R/W)** **Reset Value = 00000000h**
31:4	**ControlHeadED:** Pointer to the Control List Head ED.
3:0	**Reserved:** Read/Write 0s.
Offset 24h-27h	**HcControlCurrentED Register (R/W)** **Reset Value = 00000000h**
31:4	**ControlCurrentED:** Pointer to the current Control List ED.
3:0	**Reserved:** Read/Write 0s.
Offset 28h-2Bh	**HcBulkHeadED Register (R/W)** **Reset Value = 00000000h**
31:4	**BulkHeadED:** Pointer to the Bulk List Head ED.
3:0	**Reserved:** Read/Write 0s.
Offset 2Ch-2Fh	**HcBulkCurrentED Register (R/W)** **Reset Value = 00000000h**
31:4	**BulkCurrentED:** Pointer to the current Bulk List ED.
3:0	**Reserved:** Read/Write 0s.

Table 5-26. USB BAR+Memory Offset xxh: USB Controller Registers (Continued)

Bit	Description
Offset 30h-33h	**HcDoneHead Register (R/W)** — **Reset Value = 00000000h**
31:4	**DoneHead:** Pointer to the current Done List Head ED.
3:0	**Reserved:** Read/Write 0s.
Offset 34h-37h	**HcFmInterval Register (R/W)** — **Reset Value = 00002EDFh**
31	**FrameIntervalToggle (Read Only):** This bit is toggled by HCD when it loads a new value into FrameInterval.
30:16	**FSLargestDataPacket (Read Only):** This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame.
15:14	**Reserved:** Read/Write 0s.
13:0	**FrameInterval:** This field specifies the length of a frame as (bit times - 1). For 12,000 bit times in a frame, a value of 11,999 is stored here.
Offset 38h-3Bh	**HcFrameRemaining Register (RO)** — **Reset Value = 00002Exxh**
31	**FrameRemainingToggle (Read Only):** Loaded with FrameIntervalToggle when FrameRemaining is loaded.
30:14	**Reserved:** Read 0s.
13:0	**FrameRemaining (Read Only):** When the HC is in the UsbOperational state, this 14-bit field decrements each 12 MHz clock period. When the count reaches 0, (end of frame) the counter reloads with FrameInterval. In addition, the counter loads when the HC transitions into UsbOperational.
Offset 3Ch-3Fh	**HcFmNumber Register (RO)** — **Reset Value = 00000000h**
31:16	**Reserved:** Read 0s.
15:0	**FrameNumber (Read Only):** This 16-bit incrementing counter field is incremented coincident with the loading of FrameRemaining. The count rolls over from FFFFh to 0h.
Offset 40h-43h	**HcPeriodicStart Register (R/W)** — **Reset Value = 00000000h**
31:14	**Reserved:** Read/Write 0s.
13:0	**PeriodicStart:** This field contains a value used by the List Processor to determine where in a frame the Periodic List processing must begin.
Offset 44h-47h	**HcLSThreshold Register (R/W)** — **Reset Value = 00000628h**
31:12	**Reserved:** Read/Write 0s.
11:0	**LSThreshold:** This field contains a value used by the Frame Management block to determine whether or not a low speed transaction can be started in the current frame.
Offset 48h-4Bh	**HcRhDescriptorA Register (R/W)** — **Reset Value = 01000002h**
31:24	**PowerOnToPowerGoodTime:** This field value is represented as the number of 2 ms intervals, ensuring that the power switching is effective within 2 ms. Only bits [25:24] are implemented as R/W. The remaining bits are read only as 0. It is not expected that these bits be written to anything other than 1h, but limited adjustment is provided. This field should be written to support system implementation. This field should always be written to a non-zero value.
23:13	**Reserved:** Read/Write 0s.
12	**NoOverCurrentProtection:** This bit should be written to support the external system port over-current implementation. 0 = Over-current status is reported; 1 = Over-current status is not reported.
11	**OverCurrentProtectionMode:** This bit should be written 0 and is only valid when NoOverCurrentProtection is cleared. 0 = Global Over-Current; 1 = Individual Over-Current
10	**DeviceType (Read Only):** USB is not a compound device.
9	**NoPowerSwitching:** This bit should be written to support the external system port power switching implementation. 0 = Ports are power switched. 1 = Ports are always powered on.
8	**PowerSwitchingMode:** This bit is only valid when NoPowerSwitching is cleared. This bit should be written 0. 0 = Global Switching; 1 = Individual Switching
7:0	**NumberDownstreamPorts (Read Only):** USB supports two downstream ports.
Note: This register is only reset by a power-on reset (PCIRST#). It is written during system initialization to configure the Root Hub. These bit should not be written during normal operation.	

Table 5-26. USB BAR+Memory Offset xxh: USB Controller Registers (Continued)

Bit	Description
Offset 4Ch-4Fh	**HcRhDescriptorB Register (R/W)** **Reset Value = 00000000h**
31:16	**PortPowerControlMask:** Global-power switching. This field is only valid if NoPowerSwitching is cleared and PowerSwitchingMode is set (individual port switching). When set, the port only responds to individual port power switching commands (Set/ClearPortPower). When cleared, the port only responds to global power switching commands (Set/ClearGlobalPower). 0 = Device not removable; 1 = Global-power mask. Port Bit relationship - Unimplemented ports are reserved, read/write 0. 0 = Reserved 1 = Port 1 2 = Port 2 ... 15 = Port 15
15:0	**DeviceRemoveable:** USB ports default to removable devices. 0 = Device not removable; 1 = Device removable. Port Bit relationship 0 = Reserved 1 = Port 1 2 = Port 2 ... 15 = Port 15 Unimplemented ports are reserved, read/write 0.
Note: This register is only reset by a power-on reset (PCIRST#). It is written during system initialization to configure the Root Hub. These bit should not be written during normal operation.	
Offset 50h-53h	**HcRhStatus Register (R/W)** **Reset Value = 00000000h**
31	**ClearRemoteWakeupEnable (Write Only):** Writing a 1 to this bit clears DeviceRemoteWakeupEnable. Writing a 1 has no effect.
30:18	**Reserved:** Read/Write 0s.
17	**OverCurrentIndicatorChange:** This bit is set when OverCurrentIndicator changes. Writing a 1 clears this bit. Writing a 0 has no effect.
16	**Read: LocalPowerStatusChange:** Not supported. Always read 0. **Write: SetGlobalPower:** Write a 1 issues a SetGlobalPower command to the ports. Writing a 0 has no effect.
15	**Read: DeviceRemoteWakeupEnable:** This bit enables ports' ConnectStatusChange as a remote wakeup event. 0 = Disabled; 1 = Enabled. **Write = SetRemoteWakeupEnable:** Writing a 1 sets DeviceRemoteWakeupEnable. Writing a 0 has no effect.
14:2	**Reserved:** Read/Write 0s.
1	**OverCurrentIndicator:** This bit reflects the state of the OVRCUR pin. This field is only valid if NoOverCurrentProtection and OverCurrentProtectionMode are cleared. 0 = No over-current condition; 1 = Over-current condition.
0	**Read: LocalPowerStatus:** Not Supported. Always read 0. **Write: ClearGlobalPower:** Writing a 1 issues a ClearGlobalPower command to the ports. Writing a 0 has no effect.
Note: This register is reset by the UsbReset state.	

Table 5-26. USB BAR+Memory Offset xxh: USB Controller Registers (Continued)

Bit	Description
Offset 54h-57h	**HcRhPortStatus[1] Register (R/W)** **Reset Value = 00000628h**
31:21	**Reserved:** Read/Write 0s.
20	**PortResetStatusChange:** This bit indicates that the port reset signal has completed. 0 = Port reset is not complete; 1 = Port reset is complete.
19	**PortOverCurrentIndicatorChange:** This bit is set when OverCurrentIndicator changes. Writing a 1 clears this bit. Writing a 0 has no effect.
18	**PortSuspendStatusChange:** This bit indicates the completion of the selective resume sequence for the port. 0 = Port is not resumed; 1 = Port resume is complete.
17	**PortEnableStatusChange:** This bit indicates that the port has been disabled due to a hardware event (cleared PortEnableStatus). 0 = Port has not been disabled; 1 = PortEnableStatus has been cleared.
16	**ConnectStatusChange:** This bit indicates a connect or disconnect event has been detected. Writing a 1 clears this bit. Writing a 0 has no effect. 0 = No connect/disconnect event; 1 = Hardware detection of connect/disconnect event. If DeviceRemoveable is set, this bit resets to 1.
15:10	**Reserved:** Read/Write 0s.
9	**Read: LowSpeedDeviceAttached:** This bit defines the speed (and bud idle) of the attached device. It is only valid when CurrentConnectStatus is set. 0 = Full Speed device; 1 = Low Speed device. **Write: ClearPortPower:** Writing a 1 clears PortPowerStatus. Writing a 0 has no effect.
8	**Read: PortPowerStatus:** This bit reflects the power state of the port regardless of the power switching mode. 0 = Port power is off; 1 = Port power is on. **Note:** If NoPowerSwitching is set, this bit is always read as 1. **Write: SetPortPower:** Writing a 1 sets PortPowerStatus. Writing a 0 has no effect.
7:5	**Reserved:** Read/Write 0s.
4	**Read: PortResetStatus:** 0 = Port reset signal is not active; 1 = Port reset signal is active. **Write: SetPortReset:** Writing a 1 sets PortResetStatus. Writing a 0 has no effect.
3	**Read: PortOverCurrentIndicator:** This bit reflects the state of the OVRCUR pin dedicated to this port. This field is only valid if NoOverCurrentProtection is cleared and OverCurrentProtectionMode is set. 0 = No over-current condition; 1 = Over-current condition. **Write: ClearPortSuspend:** Writing a 1 initiates the selective resume sequence for the port. Writing a 0 has no effect.
2	**Read: PortSuspendStatus:** 0 = Port is not suspended; 1 = Port is selectively suspended. **Write: SetPortSuspend:** Writing a 1 sets PortSuspendStatus. Writing a 0 has no effect.
1	**Read: PortEnableStatus:** 0 = Port disabled; 1 = Port enabled. **Write: SetPortEnable:** Writing a 1 sets PortEnableStatus. Writing a 0 has no effect.
0	**Read: CurrentConnectStatus:** 0 = No device connected; 1 = Device connected. **Note:** If DeviceRemoveable is set (not removable) this bit is always 1. **Write: ClearPortEnable:** Writing 1 a clears PortEnableStatus. Writing a 0 has no effect.
Note: This register is reset by the UsbReset state.	

Table 5-26. USB BAR+Memory Offset xxh: USB Controller Registers (Continued)

Bit	Description
Offset 58h-5Bh	**HcRhPortStatus[2] Register (R/W)** **Reset Value = 01000002h**
31:21	**Reserved:** Read/Write 0s.
20	**PortResetStatusChange:** This bit indicates that the port reset signal has completed. 0 = Port reset is not complete; 1 = Port reset is complete.
19	**PortOverCurrentIndicatorChange:** This bit is set when OverCurrentIndicator changes. Writing a 1 clears this bit. Writing a 0 has no effect.
18	**PortSuspendStatusChange:** This bit indicates the completion of the selective resume sequence for the port. 0 = Port is not resumed; 1 = Port resume is complete.
17	**PortEnableStatusChange:** This bit indicates that the port has been disabled due to a hardware event (cleared PortEnableStatus). 0 = Port has not been disabled; 1 = PortEnableStatus has been cleared.
16	**ConnectStatusChange:** This bit indicates a connect or disconnect event has been detected. Writing a 1 clears this bit. Writing a 0 has no effect. 0 = No connect/disconnect event; 1 = Hardware detection of connect/disconnect event. If DeviceRemoveable is set, this bit resets to 1.
15:10	**Reserved:** Read/Write 0s.
9	**Read: LowSpeedDeviceAttached:** This bit defines the speed (and bud idle) of the attached device. It is only valid when CurrentConnectStatus is set. 0 = Full Speed device; 1 = Low Speed device. **Write: ClearPortPower:** Writing a 1 clears PortPowerStatus. Writing a 0 has no effect.
8	**Read: PortPowerStatus:** This bit reflects the power state of the port regardless of the power switching mode. 0 = Port power is off; 1 = Port power is on. **Note:** If NoPowerSwitching is set, this bit is always read as 1. **Write: SetPortPower:** Writing a 1 sets PortPowerStatus. Writing a 0 has no effect.
7:5	**Reserved:** Read/Write 0s.
4	**Read: PortResetStatus:** 0 = Port reset signal is not active; 1 = Port reset signal is active. **Write: SetPortReset:** Writing a 1 sets PortResetStatus. Writing a 0 has no effect.
3	**Read: PortOverCurrentIndicator:** This bit reflects the state of the OVRCUR pin dedicated to this port. This field is only valid if NoOverCurrentProtection is cleared and OverCurrentProtectionMode is set. 0 = No over-current condition; 1 = Over-current condition. **Write: ClearPortSuspend:** Writing a 1 initiates the selective resume sequence for the port. Writing a 0 has no effect.
2	**Read: PortSuspendStatus:** 0 = Port is not suspended; 1 = Port is selectively suspended. **Write: SetPortSuspend:** Writing a 1 sets PortSuspendStatus. Writing a 0 has no effect.
1	**Read: PortEnableStatus:** 0 = Port disabled; 1 = Port enabled. **Write: SetPortEnable:** Writing a 1 sets PortEnableStatus. Writing a 0 has no effect.
0	**Read: CurrentConnectStatus:** 0 = No device connected; 1 = Device connected. **Note:** If DeviceRemoveable is set (not removable) this bit is always 1. **Write: ClearPortEnable:** Writing 1 a clears PortEnableStatus. Writing a 0 has no effect.
Note: This register is reset by the UsbReset state.	
Offset 5Ch-5Fh	**Reserved** **Reset Value = 00000000h**
Offset 60h-9Fh	**Reserved** **Reset Value = xxh**

Table 5-26. USB BAR+Memory Offset xxh: USB Controller Registers (Continued)

Bit	Description
Offset 100h-103h	**HceControl Register (R/W)**	**Reset Value = 00000000h**
31:9	**Reserved:** Read/Write 0s.
8	**A20State:** Indicates current state of Gate A20 on keyboard controller. Compared against value written to 60h when GateA20Sequence is active.
7	**IRQ12Active:** Indicates a positive transition on IRQ12 from keyboard controller occurred. Software writes this bit to 1 to clear it (set it to 0); a 0 write has no effect.
6	**IRQ1Active:** Indicates a positive transition on IRQ1 from keyboard controller occurred. Software writes this bit to 1 to clear it (set it to 0); a 0 write has no effect.
5	**GateA20Sequence:** Set by HC when a data value of D1h is written to I/O port 64h. Cleared by HC on write to I/O port 64h of any value other than D1h.
4	**ExternalIRQEn:** When set to 1, IRQ1 and IRQ12 from the keyboard controller cause an emulation interrupt. The function controlled by this bit is independent of the setting of the EmulationEnable bit in this register.
3	**IRQEn:** When set, the HC generates IRQ1 or IRQ12 as long as the OutputFull bit in HceStatus is set to 1. If the AuxOutputFull bit of HceStatus is 0, IRQ1 is generated: if 1, then an IRQ12 is generated.
2	**CharacterPending:** When set, an emulation interrupt will be generated when the OutputFull bit of the HceStatus register is set to 0.
1	**EmulationInterrupt (Read Only):** This bit is a static decode of the emulation interrupt condition.
0	**EmulationEnable:** When set to 1 the HC is enabled for legacy emulation and will decode accesses to I/O registers 60h and 64h and generate IRQ1 and/or IRQ12 when appropriate. The HC also generates an emulation interrupt at appropriate times to invoke the emulation software.
Note: This register is used to enable and control the emulation hardware and report various status information.	
Offset 104h-107h	**HceInput Register (R/W)**	**Reset Value = 000000xxh**
31:8	**Reserved:** Read/Write 0s.
7:0	**InputData:** This register holds data written to I/O ports 60h and 64h.
Note: This register is the emulation side of the legacy Input Buffer register.	
Offset 108h-10Bh	**HceOutput Register (R/W)**	**Reset Value = 000000xxh**
31:8	**Reserved:** Read/Write 0s.
7:0	**OutputData:** This register hosts data that is returned when an I/O read of port 60h is performed by application software.
Note: This register is the emulation side of the legacy Output Buffer register where keyboard and mouse data is to be written by software.	
Offset 10Ch-10Fh	**HceStatus Register (R/W)**	**Reset Value = 00000000h**
31:8	**Reserved:** Read/Write 0s.
7	**Parity:** Indicates parity error on keyboard/mouse data.
6	**Timeout:** Used to indicate a time-out
5	**AuxOutputFull:** IRQ12 is asserted whenever this bit is set to 1 and OutputFull is set to 1 and the IRQEn bit is set.
4	**Inhibit Switch:** This bit reflects the state of the keyboard inhibit switch and is set if the keyboard is NOT inhibited.
3	**CmdData:** The HC will set this bit to 0 on an I/O write to port 60h and on an I/O write to port 64h the HC will set this bit to 1.
2	**Flag:** Nominally used as a system flag by software to indicate a warm or cold boot.
1	**InputFull:** Except for the case of a Gate A20 sequence, this bit is set to 1 on an I/O write to address 60h or 64h. While this bit is set to 1 and emulation is enabled, an emulation interrupt condition exists.
0	**OutputFull:** The HC will set this bit to 0 on a read of I/O port 60h. If IRQEn is set and AuxOutputFull is set to 0 then an IRQ1 is generated as long as this bit is set to 1. If IRQEn is set and AuxOutputFull is set to 1 then and IRQ12 will be generated a long as this bit is set to 1. While this bit is 0 and CharacterPending in HceControl is set to 1, an emulation interrupt condition exists.
Note: This register is the emulation side of the legacy Status register.	

5.5 ISA Legacy I/O Register Space

The bit formats for the ISA Legacy I/O Registers plus two chipset-specific configuration registers used for interrupt mapping in the CS5530A are given in this section. These registers reside in the ISA I/O address space in the address range from 000h to FFFh and are accessed through typical input/output instructions (i.e., CPU direct R/W) with the designated I/O port address and 8-bit data. The registers are separated into the following categories:

- DMA Channel Control Registers, see Table 5-27
- DMA Page Registers, see Table 5-28
- Programmable Interval Timer Registers, see Table 5-29
- Programmable Interrupt Controller Registers, see Table 5-30
- Keyboard Controller Registers, see Table 5-31
- Real Time Clock Registers, see Table 5-32
- Miscellaneous Registers, see Table 5-33 (includes 4D0h and 4D1h Interrupt Edge/Level Select Registers and ACPI Timer Count Register at I/O Port 121Ch)

Table 5-27. DMA Channel Control Registers

Bit	Description
I/O Port 000h (R/W)	**DMA Channel 0 Address Register**
Written as two successive bytes, byte 0, 1.	
I/O Port 001h (R/W)	**DMA Channel 0 Transfer Count Register**
Written as two successive bytes, byte 0, 1.	
I/O Port 002h (R/W)	**DMA Channel 1 Address Register**
Written as two successive bytes, byte 0, 1.	
I/O Port 003h (R/W)	**DMA Channel 1 Transfer Count Register**
Written as two successive bytes, byte 0, 1.	
I/O Port 004h (R/W)	**DMA Channel 2 Address Register**
Written as two successive bytes, byte 0, 1.	
I/O Port 005h (R/W)	**DMA Channel 2 Transfer Count Register**
Written as two successive bytes, byte 0, 1.	
I/O Port 006h (R/W)	**DMA Channel 3 Address Register**
Written as two successive bytes, byte 0, 1.	
I/O Port 007h (R/W)	**DMA Channel 3 Transfer Count Register**
Written as two successive bytes, byte 0, 1.	
I/O Port 008h (R/W)	
Read	**DMA Status Register, Channels 3:0**
7	**Channel 3 Request:** Request pending? 0 = No; 1 = Yes.
6	**Channel 2 Request:** Request pending? 0 = No; 1 = Yes.
5	**Channel 1 Request:** Request pending? 0 = No; 1 = Yes.
4	**Channel 0 Request:** Request pending? 0 = No; 1 = Yes.
3	**Channel 3 Terminal Count:** TC reached? 0 = No; 1 = Yes.
2	**Channel 2 Terminal Count:** TC reached? 0 = No; 1 = Yes.
1	**Channel 1 Terminal Count:** TC reached? 0 = No; 1 = Yes.
0	**Channel 0 Terminal Count:** TC reached? 0 = No; 1 = Yes.
Write	**DMA Command Register, Channels 3:0**
7	**DACK Sense:** 0 = Active high; 1 = Active low.
6	**DREQ Sense:** 0 = Active high; 1 = Active low.
5	**Write Selection:** 0 = Late write; 1 = Extended write.
4	**Priority Mode:** 0 = Fixed; 1 = Rotating.
3	**Timing Mode:** 0 = Normal; 1 = Compressed.
2	**Channels 3 through 0:** 0 = Disable; 1 = Enable.
1:0	**Reserved:** Set to 0.

Table 5-27. DMA Channel Control Registers (Continued)

Bit	Description
I/O Port 009h (WO)	**Software DMA Request Register, Channels 3:0**
7:3	**Reserved:** Set to 0.
2	**Reserved:** Set to 0.
1:0	**Channel Number Request Select:** 00 = Channel 0; 01 = Channel 1; 10 = Channel 2; 11 = Channel 3. **Note:** Software DMA is not supported.
I/O Port 00Ah (R/W)	**DMA Channel Mask Register, Channels 3:0**
7:3	**Reserved:** Set to 0.
2	**Channel Mask:** 0 = Not masked; 1 = Masked.
1:0	**Channel Number Mask Select:** 00 = Channel 0; 01 = Channel 1; 10 = Channel 2; 11 = Channel 3.
I/O Port 00Bh (WO)	**DMA Channel Mode Register, Channels 3:0**
7:6	**Transfer Mode:** 00 = Demand; 01 = Single; 10 = Block; 11 = Cascade.
5	**Address Direction:** 0 = Increment; 1 = Decrement.
4	**Auto-initialize:** 0 = Disable; 1 = Enable.
3:2	**Transfer Type:** 00 = Verify; 01 = Memory read; 10 = Memory write; 11 = Reserved.
1:0	**Channel Number Mode Select:** 00 = Channel 0; 01 = Channel 1; 10 = Channel 2; 11 = Channel 3.
I/O Port 00Ch (WO)	**DMA Clear Byte Pointer Command, Channels 3:0**
I/O Port 00Dh (WO)	**DMA Master Clear Command, Channels 3:0**
I/O Port 00Eh (WO)	**DMA Clear Mask Register Command, Channels 3:0**
I/O Port 00Fh (WO)	**DMA Write Mask Register Command, Channels 3:0**
I/O Port 0C0h (R/W)	**DMA Channel 4 Address Register**
Not used.	
I/O Port 0C2h (R/W)	**DMA Channel 4 Transfer Count Register**
Not used.	
I/O Port 0C4h (R/W)	**DMA Channel 5 Address Register**
Memory address bytes 1 and 0.	
I/O Port 0C6h (R/W)	**DMA Channel 5 Transfer Count Register**
Transfer count bytes 1 and 0	
I/O Port 0C8h (R/W)	**DMA Channel 6 Address Register**
Memory address bytes 1 and 0.	
I/O Port 0CAh (R/W)	**DMA Channel 6 Transfer Count Register**
Transfer count bytes 1 and 0.	
I/O Port 0CCh (R/W)	**DMA Channel 7 Address Register**
Memory address bytes 1 and 0.	
I/O Port 0CEh (R/W)	**DMA Channel 7 Transfer Count Register**
Transfer count bytes 1 and 0.	

Table 5-27. DMA Channel Control Registers (Continued)

Bit	Description
I/O Port 0D0h (R/W)	
Read	**DMA Status Register, Channels 7:4**
7	**Channel 7 Request:** Request pending? 0 = No; 1 = Yes.
6	**Channel 6 Request:** Request pending? 0 = No; 1 = Yes.
5	**Channel 5 Request:** Request pending? 0 = No; 1 = Yes.
4	**Undefined**
3	**Channel 7 Terminal Count:** TC reached? 0 = No; 1 = Yes.
2	**Channel 6 Terminal Count:** TC reached? 0 = No; 1 = Yes.
1	**Channel 5 Terminal Count:** TC reached? 0 = No; 1 = Yes.
0	**Undefined**
Write	**DMA Command Register, Channels 7:4**
7	**DACK Sense:** 0 = Active high; 1 = Active low.
6	**DREQ Sense:** 0 = Active high; 1 = Active low.
5	**Write Selection:** 0 = Late write; 1 = Extended write.
4	**Priority Mode:** 0 = Fixed; 1 = Rotating.
3	**Timing Mode:** 0 = Normal; 1 = Compressed.
2	**Channels 7 through 4:** 0 = Disable; 1 = Enable.
1:0	**Reserved:** Set to 0.
I/O Port 0D2h (WO)	**Software DMA Request Register, Channels 7:4**
7:3	**Reserved:** Set to 0.
2	**Request Type:** 0 = Reset; 1 = Set.
1:0	**Channel Number Request Select:** 00 = Illegal; 01 = Channel 5; 10 = Channel 6; 11 = Channel 7. **Note:** Software DMA is not supported
I/O Port 0D4h (R/W)	**DMA Channel Mask Register, Channels 7:0**
7:3	**Reserved:** Set to 0.
2	**Channel Mask:** 0 = Not masked; 1 = Masked.
1:0	**Channel Number Mask Select:** 00 = Channel 4; 01 = Channel 5; 10 = Channel 6; 11 = Channel 7.
I/O Port 0D6h (WO)	**DMA Channel Mode Register, Channels 7:4**
7:6	**Transfer Mode:** 00 = Demand; 01 = Single; 10 = Block; 11 = Cascade.
5	**Address Direction:** 0 = Increment; 1 = Decrement.
4	**Auto-initialize:** 0 = Disabled; 1 = Enable.
3:2	**Transfer Type:** 00 = Verify; 01 = Memory read; 10 = Memory write; 11 = Reserved.
1:0	**Channel Number Mode Select:** 00 = Channel 4; 01 = Channel 5; 10 = Channel 6; 11 = Channel 7. Channel 4 must be programmed in cascade mode. This mode is not the default.
I/O Port 0D8h (WO)	**DMA Clear Byte Pointer Command, Channels 7:4**
I/O Port 0DAh (WO)	**DMA Master Clear Command, Channels 7:4**
I/O Port 0DCh (WO)	**DMA Clear Mask Register Command, Channels 7:4**
I/O Port 0DEh (WO)	**DMA Write Mask Register Command, Channels 7:4**

Table 5-28. DMA Page Registers

Bit	Description
I/O Port 081h (R/W)	**DMA Channel 2 Low Page Register**
Address bits [23:16] (byte 2).	
I/O Port 082h (R/W)	**DMA Channel 3 Low Page Register**
Address bits [23:16] (byte 2).	
I/O Port 083h (R/W)	**DMA Channel 1 Low Page Register**
Address bits [23:16] (byte 2).	
I/O Port 087h (R/W)	**DMA Channel 0 Low Page Register**
Address bits [23:16] (byte 2).	
I/O Port 089h (R/W)	**DMA Channel 6 Low Page Register**
Address bits [23:16] (byte 2).	
I/O Port 08Ah (R/W)	**DMA Channel 7 Low Page Register**
Address bits [23:16] (byte 2).	
I/O Port 08Bh (R/W)	**DMA Channel 5 Low Page Register**
Address bits [23:16] (byte 2).	
I/O Port 08Fh (R/W)	**ISA Refresh Low Page Register**
Refresh address.	
I/O Port 481h (R/W)	**DMA Channel 2 High Page Register**
Address bits [31:24] (byte 3). **Note:** This register is reset to 00h on any access to Port 081h.	
I/O Port 482h (R/W)	**DMA Channel 3 High Page Register**
Address bits [31:24] (byte 3). **Note:** This register is reset to 00h on any access to Port 082h.	
I/O Port 483h (R/W)	**DMA Channel 1 High Page Register**
Address bits [31:24] (byte 3). **Note:** This register is reset to 00h on any access to Port 083h.	
I/O Port 487h (R/W)	**DMA Channel 0 High Page Register**
Address bits [31:24] (byte 3). **Note:** This register is reset to 00h on any access to Port 087h.	
I/O Port 489h (R/W)	**DMA Channel 6 High Page Register**
Address bits [31:24] (byte 3). **Note:** This register is reset to 00h on any access to Port 089h.	
I/O Port 48Ah (R/W)	**DMA Channel 7 High Page Register**
Address bits [31:24] (byte 3). **Note:** This register is reset to 00h on any access to Port 08Ah.	
I/O Port 48Bh (R/W)	**DMA Channel 5 High Page Register**
Address bits [31:24] (byte 3). **Note:** This register is reset to 00h on any access to Port 08Bh.	

Table 5-29. Programmable Interval Timer Registers

Bit	Description
I/O Port 040h	
Write	**PIT Timer 0 Counter**
7:0	**Counter Value**
Read	**PIT Timer 0 Status**
7	**Counter Output:** State of counter output signal.
6	**Counter Loaded:** Last count written is loaded? 0 = Yes; 1 = No.
5:4	**Current Read/Write Mode:** 00 = Counter latch command; 01 = R/W LSB only; 10 = R/W MSB only; 11 = R/W LSB, followed by MSB.
3:1	**Current Counter Mode:** 0-5.
0	**BCD Mode:** 0 = Binary; 1 = BCD (binary coded decimal).
I/O Port 041h	
Write	**PIT Timer 1 Counter (Refresh)**
7:0	**Counter Value**
Read	**PIT Timer 1 Status (Refresh)**
7	**Counter Output:** State of counter output signal.
6	**Counter Loaded:** Last count written is loaded? 0 = Yes; 1 = No.
5:4	**Current Read/Write Mode:** 00 = Counter latch command; 01 = R/W LSB only; 10 = R/W MSB only; 11 = R/W LSB, followed by MSB.
3:1	**Current Counter Mode:** 0-5.
0	**BCD Mode:** 0 = Binary; 1 = BCD (binary coded decimal).
I/O Port 042h	
Write	**PIT Timer 2 Counter (Speaker)**
7:0	**Counter Value**
Read	**PIT Timer 2 Status (Speaker)**
7	**Counter Output:** State of counter output signal.
6	**Counter Loaded:** Last count written is loaded? 0 = Yes; 1 = No.
5:4	**Current Read/Write Mode:** 00 = Counter latch command; 01 = R/W LSB only; 10 = R/W MSB only; 11 = R/W LSB, followed by MSB.
3:1	**Current Counter Mode:** 0-5.
0	**BCD Mode:** 0 = Binary; 1 = BCD (binary coded decimal).
I/O Port 043h (R/W)	**PIT Mode Control Word Register**
7:6	**Counter Select:** 00 = Counter 0; 01 = Counter 1; 10 = Counter 2; 11 = Read-back command (Note 1).
5:4	**Current Read/Write Mode:** 00 = Counter latch command (Note 2); 01 = R/W LSB only; 10 = R/W MSB only; 11 = R/W LSB, followed by MSB.
3:1	**Current Counter Mode:** 0-5.
0	**BCD Mode:** 0 = Binary; 1 = BCD (binary coded decimal).

Notes: 1. If bits [7:6] = 11: Register functions as Read Status Command
Bit 5 = Latch Count, Bit 4 = Latch Status, Bit 3 = Select Counter 2, Bit 2 = Select Counter 1, Bit 1 = Select Counter 0, and Bit 0 = Reserved

2. If bits [5:4] = 00: Register functions as Counter Latch Command
Bits [7:6] = Selects Counter, and [3:0] = Don't care

Table 5-30. Programmable Interrupt Controller Registers

Bit	Description
I/O Port 020h / 0A0h (WO)	**Master / Slave PIC IWC1**
7:5	**Reserved:** Set to 0.
4	**Reserved:** Set to 1.
3	**Trigger Mode:** 0 = Edge; 1 = Level.
2	**Vector Address Interval:** 0 = 8-byte intervals; 1 = 4-byte intervals.
1	**Reserved:** Set to 0 (cascade mode).
0	**Reserved:** Set to 1 (ICW4 must be programmed).
I/O Port 021h / 0A1h (WO)	**Master / Slave PIC ICW2 (after ICW1 is written)**
7:3	**A[7:3]:** Address lines [7:3] for base vector for interrupt controller.
2:0	**Reserved:** Set to 0.
I/O Port 021h / 0A1h (WO)	**Master / Slave PIC ICW3 (after ICW2 is written)**
Master PIC ICW3	
7:0	**Cascade IRQ:** Must be 04h.
Slave PIC ICW3	
7:0	**Slave ID:** Must be 02h.
I/O Port 021h / 0A1h (WO)	**Master / Slave PIC ICW4 (after ICW3 is written)**
7:5	**Reserved:** Set to 0.
4	**Special Fully Nested Mode:** 0 = Disable; 1 = Enable. This function is not implemented and should always be disabled (i.e., set this bit to 0).
3:2	**Reserved:** Set to 0.
1	**Auto EOI:** 0 = Normal EOI; 1 = Auto EOI.
0	**Reserved:** Set to 1 (8086/8088 mode).
I/O Port 021h / 0A1h (R/W)	**Master / Slave PIC OCW1 (except immediately after ICW1 is written)**
7	**IRQ7 / IRQ15 Mask:** 0 = Not Masked; 1 = Mask.
6	**IRQ6 / IRQ14 Mask:** 0 = Not Masked; 1 = Mask.
5	**IRQ5 / IRQ13 Mask:** 0 = Not Masked; 1 = Mask.
4	**IRQ4 / IRQ12 Mask:** 0 = Not Masked; 1 = Mask.
3	**IRQ3 / IRQ11 Mask:** 0 = Not Masked; 1 = Mask.
2	**IRQ2 / IRQ10 Mask:** 0 = Not Masked; 1 = Mask.
1	**IRQ1 / IRQ9 Mask:** 0 = Not Masked; 1 = Mask.
0	**IRQ0 / IRQ8 Mask:** 0 = Not Masked; 1 = Mask.
I/O Port 020h / 0A0h (WO)	**Master / Slave PIC OCW2**
7:5	**Rotate/EOI Codes** 000 = Clear rotate in Auto EOI mode 001 = Non-specific EOI 010 = No operation 011 = Specific EOI (bits [2:0] must be valid) 100 = Set rotate in Auto EOI mode 101 = Rotate on non-specific EOI command 110 = Set priority command (bits [2:0] must be valid) 111 = Rotate on specific EOI command (bits [2:0] must be valid)
4:3	**Reserved:** Set to 0.
2:0	**IRQ Number (000-111)**

Table 5-30. Programmable Interrupt Controller Registers (Continued)

Bit	Description
I/O Port 020h / 0A0h (WO)	**Master / Slave PIC OCW3**
7	**Reserved:** Set to 0.
6:5	**Special Mask Mode** 00 = No operation 01 = No operation 10 = Reset Special Mask Mode 11 = Set Special Mask Mode
4	**Reserved:** Set to 0.
3	**Reserved:** Set to 1.
2	**Reserved:** Set to 0. Poll Command at this address is not supported.
1:0	**Register Read Mode** 00 = No operation 01 = No operation 10 = Read interrupt request register on next read of Port 20h 11 = Read interrupt service register on next read of Port 20h
I/O Port 020h / 0A0h (RO)	**Master / Slave PIC Interrupt Request and Service Registers for OCW3 Commands**
Interrupt Request Register	
7	**IRQ7 / IRQ15 Pending:** 0 = Yes; 1 = No.
6	**IRQ6 / IRQ14 Pending:** 0 = Yes; 1 = No.
5	**IRQ5 / IRQ13 Pending:** 0 = Yes; 1 = No.
4	**IRQ4 / IRQ12 Pending:** 0 = Yes; 1 = No.
3	**IRQ3 / IRQ11 Pending:** 0 = Yes; 1 = No.
2	**IRQ2 / IRQ10 Pending:** 0 = Yes; 1 = No.
1	**IRQ1 / IRQ9 Pending:** 0 = Yes; 1 = No.
0	**IRQ0 / IRQ8 Pending:** 0 = Yes; 1 = No.
Interrupt Service Register	
7	**IRQ7 / IRQ15 In-Service:** 0 = No; 1 = Yes.
6	**IRQ6 / IRQ14 In-Service:** 0 = No; 1 = Yes.
5	**IRQ5 / IRQ13 In-Service:** 0 = No; 1 = Yes.
4	**IRQ4 / IRQ12 In-Service:** 0 = No; 1 = Yes.
3	**IRQ3 / IRQ11 In-Service:** 0 = No; 1 = Yes.
2	**IRQ2 / IRQ10 In-Service:** 0 = No; 1 = Yes.
1	**IRQ1 / IRQ9 In-Service:** 0 = No; 1 = Yes.
0	**IRQ0 / IRQ8 In-Service:** 0 = No; 1 = Yes.
Note: The function of this register is set with bits [1:0] in a write to 020h.	

Table 5-31. Keyboard Controller Registers

Bit	Description
I/O Port 060h (R/W)	**External Keyboard Controller Data Register**
Keyboard Controller Data Register: All accesses to this port are passed to the ISA bus. If the fast keyboard gate A20 and reset features are enabled through bit 7 of the ROM/AT Logic Control Register (F0 Index 52h[7]), the respective sequences of writes to this port assert the A20M# pin or cause a warm CPU reset.	
I/O Port 061h (R/W)	**Port B Control Register** **Reset Value = 00x01100b**
7	**PERR#/SERR# Status (Read Only):** Was a PCI bus error (PERR#/SERR#) asserted by a PCI device or by the CS5530A? 0 = No; 1 = Yes. This bit can only be set if ERR_EN (bit 2) is set 0. This bit is set 0 after a write to ERR_EN with a 1 or after reset.
6	**IOCHK# Status (Read Only):** Is an I/O device reporting an error to the CS5530A? 0 = No; 1 = Yes. This bit can only be set if IOCHK_EN (bit 3) is set 0. This bit is set 0 after a write to IOCHK_EN with a 1 or after reset.
5	**PIT OUT2 State (Read Only):** This bit reflects the current status of the PIT Counter 2 (OUT2).
4	**Toggle (Read Only):** This bit toggles on every falling edge of Counter 1 (OUT1).
3	**IOCHK Enable:** 0 = Generates an NMI if IOCHK# is driven low by an I/O device to report an error. Note that NMI is under SMI control. 1 = Ignores the IOCHK# input signal and does not generate NMI.
2	**PERR#/SERR# Enable:** Generates an NMI if PERR#/SERR# is driven active to report an error. 0 = Enable; 1 = Disable
1	**PIT Counter2 (SPKR):** 0 = Forces Counter 2 output (OUT2) to zero; 1 = Allows Counter 2 output (OUT2) to pass to the speaker.
0	**PIT Counter2 Enable:** 0 = Sets GATE2 input low; 1 = Sets GATE2 input high.
I/O Port 062h (R/W)	**External Keyboard Controller Mailbox Register**
Keyboard Controller Mailbox Register: Accesses to this port will assert KBROMCS# if the Port 062h/066h decode is enabled through bit 7 of the Decode Control Register 2 (F0 Index 5Bh[7]).	
I/O Port 064h (R/W)	**External Keyboard Controller Command Register**
Keyboard Controller Command Register: All accesses to this port are passed to the ISA bus. If the fast keyboard gate A20 and reset features are enabled through bit 7 of the ROM/AT Logic Control Register (F0 Index 52h[7]), the respective sequences of writes to this port assert the A20M# pin or cause a warm CPU reset.	
I/O Port 066h (R/W)	**External Keyboard Controller Mailbox Register**
Keyboard Controller Mailbox Register: Accesses to this port will assert KBROMCS# if the Port 062h/066h decode is enabled through bit 7 of the Decode Control Register 2 (F0 Index 5Bh[7]).	
I/O Port 092h	**Port A Control Register (R/W)** **Reset Value = 02h**
7:2	**Reserved:** Set to 0.
1	**A20M# SMI Assertion:** Assert A20M#. 0 = Enable mask; 1 = Disable mask.
0	**Fast CPU Reset:** WM_RST SMI is asserted to the BIOS. 0 = Disable; 1 = Enable. This bit must be cleared before the generation of another reset.

Table 5-32. Real-Time Clock Registers

Bit	Description
I/O Port 070h (WO)	**RTC Address Register**
7	**NMI Mask:** 0 = Enable; 1 = Mask.
6:0	**RTC Register Index:** A write of this register sends the data out on the ISA bus and also causes RTCALE to be triggered.
Note: This register is shadowed within the CS5530A and is read through the RTC Shadow Register (F0 Index BBh).	
I/O Port 071h (R/W)	**RTC Data Register**
A read of this register returns the value of the register indexed by the RTC Address Register plus initiates a RTCCS#. A write of this register sets the value into the register indexed by the RTC Address Register plus initiates a RTCCS#.	

Table 5-33. Miscellaneous Registers

Bit	Description
I/O Ports 170h-177h/376h	**Secondary IDE Registers (R/W)**
When the local IDE functions are enabled, reads or writes to these registers cause the local IDE interface signals to operate according to their configuration rather than generating standard ISA bus cycles.	
I/O Ports 1F0h-1F7h/3F6h	**Primary IDE Registers (R/W)**
When the local IDE functions are enabled, reads or writes to these registers cause the local IDE interface signals to operate according to their configuration rather than generating standard ISA bus cycles.	
I/O Port 4D0h	**Interrupt Edge/Level Select Register 1 (R/W)** — **Reset Value = 00h**
7	**IRQ7 Edge or Level Select:** Selects PIC IRQ7 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
6	**IRQ6 Edge or Level Select:** Selects PIC IRQ6 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
5	**IRQ5 Edge or Level Select:** Selects PIC IRQ5 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
4	**IRQ4 Edge or Level Select:** Selects PIC IRQ4 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
3	**IRQ3 Edge or Level Select:** Selects PIC IRQ3 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
2	**Reserved:** Set to 0.
1	**IRQ1 Edge or Level Select:** Selects PIC IRQ1 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
0	**Reserved:** Set to 0.
Notes: 1. If ICW1 - bit 3 in the PIC is set as level, it overrides this setting. 2. This bit is provided to configure a PCI interrupt mapped to IRQ[x] on the PIC as level-sensitive (shared).	
I/O Port 4D1h	**Interrupt Edge/Level Select Register 2 (R/W)** — **Reset Value = 00h**
7	**IRQ15 Edge or Level Select:** Selects PIC IRQ15 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
6	**IRQ14 Edge or Level Select:** Selects PIC IRQ14 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
5	**Reserved:** Set to 0.
4	**IRQ12 Edge or Level Select:** Selects PIC IRQ12 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
3	**IRQ11 Edge or Level Select:** Selects PIC IRQ11 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
2	**IRQ10 Edge or Level Select:** Selects PIC IRQ10 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
1	**IRQ9 Edge or Level Select:** Selects PIC IRQ9 sensitivity configuration. 0 = Edge; 1 = Level. (Notes 1 and 2)
0	**Reserved:** Set to 0.
Notes: 1. If ICW1 - bit 3 in the PIC is set as level, it overrides this setting. 2. This bit is provided to configure a PCI interrupt mapped to IRQ[x] on the PIC as level-sensitive (shared).	
I/O Port 121Ch-121Fh (Note)	**ACPI Timer Count Register (RO)** — **Reset Value = 00FFFFFCh**
ACPI_COUNT (Read Only): This read-only register provides the current value for the ACPI timer. The timer counts at 14.31818/4 MHz (3.579545 MHz). If SMI generation is enabled via F0 Index 83h[5], an SMI is generated when the MSB toggles. The MSB toggles every 2.343 seconds. Top level SMI status is reported at F1BAR+Memory Offset 00h/02h[0]. Second level SMI status is reported is at F0 Index 87h/F7h[0].	
31:24	**Reserved:** Always returns 0.
23:0	**Counter**
Note: The ACPI Timer Count Register is also accessible through F1BAR+Offset 1Ch.	

5.6 V-ACPI I/O Register Space

The register space designated as V-ACPI I/O does not physically exist in the CS5530A. ACPI is supported in the CS5530A by virtualizing this register space, called V-ACPI. In order for ACPI to be supported, the V-ACPI VSA module must be included in the BIOS. The register descriptions that follow, are supplied here for reference only.

Fixed Feature Space registers are required to be implemented by all ACPI-compatible hardware. The Fixed Feature registers in the VSA/ACPI solution are mapped to normal I/O space starting at offset AC00h; however, the designer can relocate this register space at compile time, hence are hereafter referred to as ACPI_BASE. Registers within V-ACPI (Virtualized ACPI) I/O space must only be accessed on their defined boundaries. For example, byte aligned registers must not be accessed via WORD I/O instructions, WORD aligned registers must not be accessed as DWORD I/O instructions, etc.

The V-ACPI I/O Register Space can be broken up into major blocks:

- PM Event Block 1A (PM1A_EVT_BLK)
- PM Event Block 1A Control (PM1A_CNT_BLK)
- Processor Register Block (P_BLK)
- Command Block (CMD_BLK)
- Test/Setup Block (TST/SETUP_BLK)
- General Purpose Enable 0 Block (GPE0_BLK)

PM1A_EVT_BLK is 32-bit aligned and contains two 16-bit registers, PM1A_STS and PM1A _EN.

PM1A_CNT_BLK is 32-bit aligned and contains one 16-bit register, PM1A_CNT. PM1A_CNT contains the Fixed Feature control bits used for various power management enables and as communication flags between BIOS and the ACPI OS.

P_BLK is 32-bit aligned (one register block per processor) and contains two registers P_CNT and P_LVL2. P_LVL3 is currently not supported.

— P_CNT (Processor Control) - 16-bit register, Controls process duty cycle via CPU clock throttling.
DUTY_WIDTH = 3 (can be widened)
DUTY_OFFSET = 0

— P_LVL2 (Enter C2 Power State) - 8-bit, read only register. When read, causes the processor to enter C2 power state.

CMD_BLK contains one 8-bit register SMI_CMD which interprets and processes the ACPI commands (defined in Fixed ACPI Description Table, refer to ACPI Specification, Section 5.2.5).

TST/SETUP_BLK is provided by the VSA technology code and contains two registers, SETUP_IDX and SETUP_DATA for the purpose of configuring the CS5530A. Specifically, this pair of registers enables system software to map GPIO pins on the CS5530A to PM1A_STS and GPE0_STS register bits.

GPE0_BLK has registers used to enable system software to configure GPIO (General Purpose I/O) pins to generate SCI interrupts. GPE0_BLK is a 32-bit block aligned on a 4-byte boundary. It contains two 16-bit registers, GPE0_STS and GPE0_EN, each of which must be configured by the BIOS POST. In order for a GPE0_STS bit to generate an SCI, the corresponding enable bit in GPE0_EN must be set.

Table 5-34 gives the bit formats of the V-ACPI I/O registers.

Table 5-34. V-ACPI Registers

Bit	Description			
ACPI_BASE 00h-03h	**P_CNT — Processor Control Register (R/W)**			**Reset Value = 00000000h**
31:5	**Reserved:** Always 0.			
4	**THT_EN:** Enables throttling of the clock based on the CLK_VAL field.			
3	**Reserved:** Always 0.			
2:0	**CLK_VAL:** Clock throttling value. CPU duty cycle =			
	000 = Reserved	010 = 25%	100 = 50%	110 = 75%
	001 = 12.5%	011 = 37.5%	101 = 62.5%	111 = 87.5%
ACPI_BASE 04h	**P_LVL2 — Enter C2 Power State Register (RO)**			**Reset Value = 00h**
Reading this 8-bit read only register causes the processor to enter the C2 power state. Reads of P_LVL2 return 0. Writes have no effect.				
ACPI_BASE 05h	**Reserved**			**Reset Value = 00h**
ACPI_BASE 06h	**SMI_CMD — OS/BIOS Requests Register (R/W)**			**Reset Value = 00h**
Interpret and process the ACPI commands (defined in Fixed ACPI Description Table, refer to ACPI Specification, Section 5.2.5). 0x01 - ACPI_ENABLE 0x02 - ACPI_DISABLE 0x03 - S4BIOS_REQ (optional)				

Table 5-34. V-ACPI Registers (Continued)

Bit	Description
ACPI_BASE 07h	**Reserved** — **Reset Value = 00h**
ACPI_BASE 08h-09h	**PM1A_STS — PM1A Status Register (R/W)** — **Reset Value = 0000h**
15	**WAKE_STS:** Wake Status - Set when system was in sleep state and an enabled wakeup occurs.
14:11	**Reserved**
10	**RTC_STS:** Real Time Clock Status - This bit changes to 1 if an RTC alarm causes a wake up event. This bit is only set upon wakeup from a sleep state and IRQ8 is asserted by the RTC. Refer to Table 5-37.
9	**SLPBTN_STS:** Sleep Button Status (Optional) - This bit changes to 1 when the sleep button is pressed. If SLPBTN_EN is set, an SCI interrupt is generated. This bit must be configured to be set by a GPIO pin using SETUP_IDX values 0x10-0x17 in order to be set. Refer to Table 5-36.
8	**PWRBTN_STS:** Power Button Status - This bit is set when power button is pressed. If PWRBTN_EN is set, an SCI interrupt is asserted. This bit must be configured to be set by a GPIO pin using SETUP_IDX values 0x10-0x17 in order to be set. Refer to Table 5-36.
7:6	**Reserved**
5	**GBL_STS:** Global Status - The BIOS sets GBL_STS to 1 to release its global lock and return control to the ACPI OS. At the same time GBL_STS is set, the BIOS generates an SCI.
4	**BM_STS:** Bus Master Status - This bit is not supported by V-ACPI.
3:1	**Reserved**
0	**TMR_STS:** ACPI Timer Status - This bit changes to 1 whenever bit 23 of the ACPI timer (F1BAR+Memory Offset 1Ch or I/O Port 121Ch) changes state. The ACPI OS is responsible for clearing TMR_STS. If TMR_EN (ACPI_BASE 0Ah[0] is also set, then a SCI interrupt is asserted.
Note: Status bits are “sticky”. A write of a one (1) to a given bit location will reset the bit.	
ACPI_BASE 0Ah-0Bh	**PM1A_EN — PM1A Enable Register (R/W)** — **Reset Value = 0000h**
15:11	**Reserved**
10	**RTC_EN:** Real Time Clock Enable - If set, an SCI is asserted when RTC_STS changes to 1.
9	**SLPBTN_EN:** Sleep Button Enable (Optional) - If set, an SCI is asserted when SLPBTN_STS changes to 1.
8	**PWRBTN_EN:** Power Button Enable - If set, an SCI is asserted when PWRBTN_STS changes to 1.
7:6	**Reserved**
5	**GBL_EN:** Global Lock Enable - If set, writing a 1 to GBL_STS causes an SCI to be asserted.
4:1	**Reserved**
0	**TMR_EN:** ACPI Timer Enable - If set, an SCI is asserted when bit 23 of the ACPI timer (F1BAR+Memory Offset 1Ch or I/O Port 121Ch) changes state.
ACPI_BASE 0Ch-0Dh	**PM1A_CNT — PM1A Control Register (R/W)** — **Reset Value = 0000h**
15:14	**Reserved**
13	**SLP_EN (WO):** Sleep Enable (Write Only) - Setting this bit causes the system to enter the sleep state defined by SLP_TYPx. Reads of this bit always return zero.
12:10	**SLP_TYPx:** Sleep Type - Defines the type of sleep state the system enters when SLP_EN (bit 13) is set. 000 = Sleep State S0 (Full on) 001 = Sleep State S1 010 = Sleep State S2 011 = Reserved 100 = Sleep State S4 101 = Sleep State S5 (Soft off) 110 = Reserved 111 = Reserved
9:3	**Reserved**
2	**GBL_RLS (WO):** Global Lock Release (Write Only) - Used by ACPI OS to raise an event to the BIOS software (SMI). Used by ACPI driver to indicate a release of the global lock and the setting of the pending bit in the FACS table (refer to ACPI Specification, Section 5.2.8).
1	**BM_RLD:** This bit is not supported by V-ACPI.
0	**SCI_EN:** System Controller Interrupt Enable - Selects whether power management events are SCI or SMI. Set by hardware based on an ACPI_ENABLE/ACPI_DISABLE written to the SMI_CMD port.

Table 5-34. V-ACPI Registers (Continued)

Bit	Description
ACPI_BASE 0Eh-0Fh	**SETUP_IDX — Setup Index Register (R/W)** **Reset Value = 0000h**
SETUP_IDX is a 16-bit register that references an internal setting in the VSA (refer to Table 5-35). A read of SETUP_IDX returns the last value written to SETUP_IDX. A write of SETUP_IDX selects the index for a corresponding write to SETUP_DATA. Writes of any undefined index values to SETUP_IDX are ignored. If the current value of SETUP_IDX is invalid, a read of SETUP_DATA returns 0.	
ACPI_BASE 10h-11h	**GPE0_STS — General Purpose Event 0 Status Register (R/W)** **Reset Value = 0000h**
Each bit is set by an external event and cleared by a write of a one to that bit. The GPE0_STS bits are mapped to specific, chipset-resident GPIO signals using the SETUP_IDX and SETUP_DATA registers. Refer to Tables 5-35 through 5-37.	
15	**OEM_GPE_S15:** Original Equipment Manufacturer General Purpose Event Status Bit 15 - OEM defined.
14	**OEM_GPE_S14:** Original Equipment Manufacturer General Purpose Event Status Bit 14 - OEM defined.
13	**OEM_GPE_S13:** Original Equipment Manufacturer General Purpose Event Status Bit 13 - OEM defined.
12	**OEM_GPE_S12:** Original Equipment Manufacturer General Purpose Event Status Bit 12 - OEM defined.
11	**OEM_GPE_S11:** Original Equipment Manufacturer General Purpose Event Status Bit 11 - OEM defined.
10	**OEM_GPE_S10:** Original Equipment Manufacturer General Purpose Event Status Bit 10 - OEM defined.
9	**OEM_GPE_S09:** Original Equipment Manufacturer General Purpose Event Status Bit 9 - OEM defined.
8	**OEM_GPE_S08:** Original Equipment Manufacturer General Purpose Event Status Bit 8 - OEM defined.
7	**OEM_GPE_S07:** Original Equipment Manufacturer General Purpose Event Status Bit 7 - OEM defined.
6	**OEM_GPE_S06:** Original Equipment Manufacturer General Purpose Event Status Bit 6 - OEM defined. The recommended mapping for the lid switch input is to use GPIO6. If the recommended mapping is used, this bit (bit 6) needs to be mapped to GPIO6 at boot time via SETUP_IDX and SETUP_DATA. Similarly, the lid switch input needs to be routed to GPIO6 in hardware. If this method is selected, this bit is defined as: **LID_STS:** Lid Status - Set when lid state changes. If LID_EN (ACPI_BASE 12h[6] is set, a SCI interrupt is asserted. Reset by writing a 1 to this bit.
5	**OEM_GPE_S05:** Original Equipment Manufacturer General Purpose Event Status Bit 5 - OEM defined.
4	**OEM_GPE_S04:** Original Equipment Manufacturer General Purpose Event Status Bit 4 - OEM defined.
3	**OEM_GPE_S03:** Original Equipment Manufacturer General Purpose Event Status Bit 3 - OEM defined.
2	**OEM_GPE_S02:** Original Equipment Manufacturer General Purpose Event Status Bit 2 - OEM defined.
1	**OEM_GPE_S01:** Original Equipment Manufacturer General Purpose Event Status Bit 1 - OEM defined.
0	**OEM_GPE_S00:** Original Equipment Manufacturer General Purpose Event Status Bit 0 - OEM defined.
ACPI_BASE 12h-13h	**GPE0_EN — General Purpose Event 0 Enable Register (R/W)** **Reset Value = 0000h**
15	**OEM_GPE_E15:** Original Equipment Manufacturer General Purpose Event Enable Bit 15 - When set, enables a SCI to be generated when the corresponding GPE0_STS bit is set.
14	**OEM_GPE_E14:** Original Equipment Manufacturer General Purpose Event Enable Bit 14 - When set, enables a SCI to be generated when the corresponding GPE0_STS bit is set.
13	**OEM_GPE_E13:** Original Equipment Manufacturer General Purpose Event Enable Bit 13 - When set, enables a SCI to be generated when the corresponding GPE0_STS bit is set.
12	**OEM_GPE_E12:** Original Equipment Manufacturer General Purpose Event Enable Bit 12 - When set, enables a SCI to be generated when the corresponding GPE0_STS bit is set.
11	**OEM_GPE_E11:** Original Equipment Manufacturer General Purpose Event Enable Bit 11 - When set, enables a SCI to be generated when the corresponding GPE0_STS bit is set.
10	**OEM_GPE_E10:** Original Equipment Manufacturer General Purpose Event Enable Bit 10 - When set, enables a SCI to be generated when the corresponding GPE0_STS bit is set.
9	**OEM_GPE_E09:** Original Equipment Manufacturer General Purpose Event Enable Bit 9 - When set, enables a SCI to be generated when the corresponding GPE0_STS bit is set.
8	**OEM_GPE_E08:** Original Equipment Manufacturer General Purpose Event Enable Bit 8 - When set, enables a SCI to be generated when the corresponding GPE0_STS bit is set.
7	**OEM_GPE_E07:** Original Equipment Manufacturer General Purpose Event Enable Bit 7 - When set, enables a SCI to be generated when the corresponding GPE0_STS bit is set.
6	**LID_EN:** Lid Enable - Enables LID_STS to generate a SCI when set.
5	**OEM_GPE_E05:** Original Equipment Manufacturer General Purpose Event Enable Bit 5 - When set, enables a SCI to be generated when the corresponding GPE0_STS bit is set.
4	**OEM_GPE_E04:** Original Equipment Manufacturer General Purpose Event Enable Bit 4 - When set, enables a SCI to be generated when the corresponding GPE0_STS bit is set.

Table 5-34. V-ACPI Registers (Continued)

Bit	Description
3	**OEM_GPE_E03:** Original Equipment Manufacturer General Purpose Event Enable Bit 3 - When set, enables a SCI to be generated when the corresponding GPE0_STS bit is set.
2	**OEM_GPE_E02:** Original Equipment Manufacturer General Purpose Event Enable Bit 2 - When set, enables a SCI to be generated when the corresponding GPE0_STS bit is set.
1	**OEM_GPE_E01:** Original Equipment Manufacturer General Purpose Event Enable Bit 1 - When set, enables a SCI to be generated when the corresponding GPE0_STS bit is set.
0	**OEM_GPE_E00:** Original Equipment Manufacturer General Purpose Event Enable Bit 0 - When set, enables a SCI to be generated when the corresponding GPE0_STS bit is set.

ACPI_BASE 14h-17h **SETUP_DATA — Setup Data Register (R/W)** **Reset Value = 00000000h**

During a read operation, SETUP_DATA returns the value of the internal setting specified by the current value in SETUP_IDX (ACPI_ABASE 0Eh-0Fh)

ACPI_BASE 18h-1Fh **Reserved** **Reset Value = 00h**

Reserved for future V-ACPI Implementations.

Table 5-35. SETUP_IDX Values

Index	Operation
0x00	No operation
0x10	Configure GPIO0 to PM1A_STS or GPE0_STS bits
0x11	Configure GPIO1 to PM1A_STS or GPE0_STS bits
0x12	Configure GPIO2 to PM1A_STS or GPE0_STS bits
0x13	Configure GPIO3 to PM1A_STS or GPE0_STS bits
0x14	Configure GPIO4 to PM1A_STS or GPE0_STS bits
0x15	Configure GPIO5 to PM1A_STS or GPE0_STS bits
0x16	Configure GPIO6 to PM1A_STS or GPE0_STS bits
0x17	Configure GPIO7 to PM1A_STS or GPE0_STS bits
0x30	Configure IRQ0 to wakeup system
0x31	Configure IRQ1 to wakeup system
0x32	Do not use – Reserved for cascade interrupt
0x33	Configure IRQ3 to wakeup system
0x34	Configure IRQ4 to wakeup system
0x35	Configure IRQ5 to wakeup system
0x36	Configure IRQ6 to wakeup system
0x37	Configure IRQ7 to wakeup system
0x38	Configure IRQ8 to wakeup system (Defaults to RTC_STS in PM1A_STS)
0x39	Configure IRQ9 to wakeup system.
0x3A	Configure IRQ10 to wakeup system.
0x3B	Configure IRQ11 to wakeup system
0x3C	Configure IRQ12 to wakeup system
0x3D	Do not use – Reserved for math coprocessor
0x3E	Configure IRQ14 to wakeup system
0x3F	Configure IRQ15 to wakeup system
0x40	Generate GBL_STS – Sets the GLB_STS bit and generates a SCI to the OS
0x41	Configure IRQ to be used for SCI
0x42	Enable reads of ACPI registers
0x43	Do atomic I/O sequence
0x50	Video power
0x60	Soft SMI AX = 6000 emulation

Table 5-35. SETUP_IDX Values (Continued)

Index	Operation
0x61	Soft SMI AX = 6001 emulation
0x62	Soft SMI AX = 6002 emulation
0x63	Soft SMI AX = 6003 emulation
0x64	Audio power control

Table 5-36. GPIO Mapping (0x10-0x17)

SETUP_ DATA	Function
xx Value	
0x00	No mapping – Do not use this GPIO pin
0x08	Assign GPIOx to PWRBTN_STS bit in PM1A_STS
0x09	Assign GPIOx to SLPBTN_STS in PM1A_STS
0x10	Assign GPIOx to bit 0 in GPE0_STS register
0x11	Assign GPIOx to bit 1 in GPE0_STS register
0x12	Assign GPIOx to bit 2 in GPE0_STS register
0x13	Assign GPIOx to bit 3 in GPE0_STS register
0x14	Assign GPIOx to bit 4 in GPE0_STS register
0x15	Assign GPIOx to bit 5 in GPE0_STS register
0x16	Assign GPIOx to bit 6 in GPE0_STS register
0x17	Assign GPIOx to bit 7 in GPE0_STS register
0x18	Assign GPIOx to bit 8 in GPE0_STS register
0x19	Assign GPIOx to bit 9 in GPE0_STS register
0x1A	Assign GPIOx to bit 10 in GPE0_STS register
0x1B	Assign GPIOx to bit 11 in GPE0_STS register
0x1C	Assign GPIOx to bit 12 in GPE0_STS register
0x1D	Assign GPIOx to bit 13 in GPE0_STS register
0x1E	Assign GPIOx to bit 14 in GPE0_STS register
0x1F	Assign GPIOx to bit 15 in GPE0_STS register
y Value (y values may be ORed together to get the desired combination of features)	
0x01	Falling edge
0x02	Rising edge
0x04	Power button
0x08	Reserved

Note: For GPIO mapping, a value of 0000zyxx is used where:
z = a runtime/wake indicator
y = the edge to be used
xx = a bit in either PM1A_STS or GPE0_STS

When using V-ACPI both edges of GPIO6 can be sensed. When using the CS5530A, GPIO6 provides additional hardware that enables the chipset to generate an SMI on both the rising and falling edges of the input signal.

Table 5-37. IRQ Wakeup Status Mapping (0x30-0x3F)

SETUP_DATA	Function
0	Do not wakeup on IRQ activity.
0x0a	Assign IRQ Wake to bit 10 in PM1A_STS register
0x10	Assign IRQ Wake to bit 0 in GPE0_STS register
0x11	Assign IRQ Wake to bit 1 in GPE0_STS register
0x12	Assign IRQ Wake to bit 2 in GPE0_STS register
0x13	Assign IRQ Wake to bit 3 in GPE0_STS register
0x14	Assign IRQ Wake to bit 4 in GPE0_STS register
0x15	Assign IRQ Wake to bit 5 in GPE0_STS register
0x16	Assign IRQ Wake to bit 6 in GPE0_STS register
0x17	Assign IRQ Wake to bit 7 in GPE0_STS register
0x18	Assign IRQ Wake to bit 8 in GPE0_STS register
0x19	Assign IRQ Wake to bit 9 in GPE0_STS register
0x1A	Assign IRQ Wake to bit 10 in GPE0_STS register
0x1B	Assign IRQ Wake to bit 11 in GPE0_STS register
0x1C	Assign IRQ Wake to bit 12 in GPE0_STS register
0x1D	Assign IRQ Wake to bit 13 in GPE0_STS register
0x1E	Assign IRQ Wake to bit 14 in GPE0_STS register
0x1F	Assign IRQ Wake to bit 15 in GPE0_STS register

Note: When the ability to wakeup on an IRQ is desired use Index 0x31 through 0x3F. This will allow sensing of interrupts while sleeping and waking of the system when activity occurs. *The desired GPE0 Status bit will **only** be set if the system is sleeping and a wake event occurs. The system will only wake if the status bit is enabled in the corresponding enable register.*

IRQ8 (RTC) is assigned to the RTC_STS bit in the PM1A_STS register by default and should **NOT** be changed.

For enabling and selection of the GPE0 Status bit to be set when Wake on IRQ Activity is desired, use the SETUP_DATA values listed above.

Table 5-38. Commands (0x41-0x43, and 0x50)

Index	Function
0x41	**Configure IRQ to be used for SCI:** When mapping the SCI interrupt SETUP_IDX contains the number of the IRQ to be used for the SCI. Valid values are 3-7, 9-12, and 14-15. Invalid values will not change the assignment of the SCI IRQ. The default value for the SCI IRQ is 9.
0x42	**Enable Reads of ACPI Registers:** Prior to the issuance of this command only ***WRITES*** can be performed to the V-ACPI Fixed feature registers. This command MUST be issued to enable reading of the registers. This is to prevent the User Def 1 hook on NON-ACPI systems from interfering with system functions.
0x43	**Do Atomic I/O Sequence:** This command allows a sequence of I/O operations to be done with no interruption. Certain SuperI/O chips must receive unlock codes with NO intervening I/O. In addition other SuperI/O chips do not allow I/O to devices while in configuration mode. This command will insure that I/O operations are completed without interruption. The address of a sequence of I/O commands is placed in the SETUP_DATA register. The command sequence will then be processed immediately. The I/O command sequence consists of two parts: the signature/length block and the I/O block. There is only one signature/length block. There may be one or more I/O blocks. The signature block consists of four DWORDs (see Table 5-39). The I/O block consists of four bytes followed by three DWORDs (see Table 5-40).
0x50	**Video Power:** This command will control the power to the SoftVGA. If SETUP_DATA is written with a 0, power will be turned off. If a 1 is written, power will be turned on.

Table 5-39. Signature/Length Block for 0x43

Byte Offset	Value
0	**Signature:** Always 0x00000070
4	**Length:** The length of the entire buffer including the signature block in bytes.
8	**Reserved:** Set to 0
12	**Reserved:** Set to 0

Table 5-40. I/O Block for 0x43

Byte Offset	Description
0	**BYTE:** Operation Type. 1 = Read 2 = Write 3 = Read/And/Or/Write 4 = Define index and data ports In addition, values may be OR'ed in to the upper two bits of this byte to indicate that special functions are desired. 0x80 = Do not perform this operation (convert to NO-OP). 0x40 = This is an index operation.
1	**BYTE:** Reserved set to 0
2	**BYTE:** I/O Length - Determines whether a BYTE, WORD or DWORD operation is performed. 1 = BYTE operation 2 = WORD operation 3 = DWORD operation If BYTE 0 is a 4, then this field is used to indicate the size of the index write.
3	**BYTE:** Reserved set to 0
4	**DWORD:** I/O Address - This is the address in the I/O space to be used. It is always a WORD value. If this is a define index/data port operation, this DWORD contains the I/O address of the index port. If this is an index operation, other than define, this DWORD contains the value to be written to the index port.
8	**DWORD:** I/O Data - The meaning depends on the operation type. Read = This is where the data read from the I/O port will be placed. Write = This is the data to write to the I/O port. Read/AND/OR/Write = This is the data that will be ANDed with the data read from the I/O port. Define index/data port - This DWORD contains the I/O address of the data port.
12	**DWORD:** OR Data - This field is only used in a Read/AND/OR/Write operation. It contains the data that will be OR'ed after the data read was AND'ed with the previous field. After the OR is done, the data will be re-written to the I/O port.
Note: In all cases if the data called for is shorter than the field, the data will be stored or retrieved from the least significant portion of the DWORD.	

Table 5-41. Audio Soft SMI Emulation (0x60-0x63)

Soft SMI AX	SETUP_IDX	SETUP_DATA
0x6000	0x60	BP register value
0x6001	0x61	BP register value
0x6002	0x62	BX register value
0x6003	0x63	BX register value
Note: Arbitrary registers cannot be set in ASL code before issuing a soft SMI. These commands provide an I/O interface to allow AUDIO Soft SMIs to be emulated.		

Table 5-42. Audio Power Control (0x64)

Data Value	Action
0	Power codec off and mute output
1	Power codec off, do not mute (allows CD to play)
2	Power codec on and un-mute output
3	Power codec on only
Note: This command allows control of power to the audio codec as well as control of amplifier muting.	

6 Electrical Specifications

This section provides information on electrical connections, absolute maximum ratings, recommended operating conditions, and DC/AC characteristics for the Geode CS5530A. All voltage values in the electrical specifications are with respect to V_{SS} unless otherwise noted.

For detailed information on the PCI bus electrical specification refer to Chapter 4 of the PCI Bus Specification, Revision 2.1.

6.1 Electrical Connections

6.1.1 Pull-Up Resistors

Table 6-1 lists the pins that are internally connected to a 20-kohm pull-up resistor. When unused, these inputs do not require connection to an external pull-up resistor.

Table 6-1. Pins with Weak Internal Pull-Up

Signal Name	Type	Pin No.
IOR#	I/O	AE12
IOW#	I/O	AC11
MEMR#	I/O	AE19
MEMW#	I/O	AF20
SBHE#	I/O	AE17
SA[19:0]/ SD[19:0]	I/O	AD10, AE11, AF12, AD11, AE25, AD24, AD22, AE21, AF21, AC20, AD19, AF19, AF4, AF5, AD5, AF6, AC6, AD9, AE6, AD9

6.1.2 Unused Input Pins

All inputs not used by the system designer and not listed in Table 6-1 should be kept at either V_{SS} or $V_{DD.}$ To prevent possible spurious operation, connect active-high inputs to ground through a 20-kohm (±10%) pull-down resistor and active-low inputs to V_{DD} through a 20-kohm (±10%) pull-up resistor.

6.1.3 NC-Designated Pins

Pins designated NC should be left disconnected. Connecting an NC pin to a pull-up resistor, pull-down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

6.1.4 PWR/GND Connections and Decoupling

Testing and operating the CS5530A requires the use of standard high frequency techniques to reduce parasitic effects. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low-impedance wiring, and by using all of the V_{DD} and V_{SS} pins.

6.2 Absolute Maximum Ratings

Table 6-2 lists absolute maximum ratings for the CS5530A. Stresses beyond the listed ratings may cause permanent damage to the device. Exposure to conditions beyond these limits may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings may also result in reduced useful life and reliability These are stress ratings only and do not imply that operation under any conditions other than those listed under Table 6-3 is possible.

6.3 Operating Conditions

Table 6-3 lists the recommended operating conditions for the CS5530A.

Table 6-2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Operating Case Temperature	0	110	°C	Power Applied
Storage Temperature	–65	150	°C	No Bias
Supply Voltage		4.0	V	
Voltage On Any Pin	–0.5	5.5	V	
Input Clamp Current, I_{IK}	–0.5	10	mA	Power Applied
Output Clamp Current, I_{OK}		25	mA	Power Applied

Table 6-3. Operating Conditions

Symbol	Parameter (Note 1)	Min	Max	Units	Comments
T_C	Operating Case Temperature	0	85	°C	
V_{DD}	Supply Voltage	3.14	3.46	V	

1. For video interface specific parameters, refer to Table 6-17 "CRT, TFT/TV and MPEG Display Timing" on page 247.

6.4 DC Characteristics

All DC parameters and current measurements in this section were measured under the operating conditions listed in Table 6-3 on page 234, unless otherwise noted.

Table 6-4. DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Comments
V_{IL}	Low Level Input VoltageNote 1					
	8 mA			0.8	V	V_{DD} = 3.14V
	CLK			0.8		
	IDE			0.8		
	PCI	-0.5		$0.3V_{DD}$		
V_{IH}	High Level Input Voltage (Note 1)					
	8 mA	2.0			V	V_{DD} = 3.14V
	CLK	2.0				
	IDE	2.0				
	PCI	$0.5V_{DD}$		V_{DD}+0.5		
V_{OL}	Low Level Output Voltage (Note 1)					
	8 mA			0.4	V	V_{DD} = 3.14V, I_{OL} = 8 mA
	DOTCLK			0.4		V_{DD} = 3.14V, I_{OL} = 20 mA
	FP_CLK			0.4		V_{DD} = 3.14V, I_{OL} = 12 mA
	IDE			0.5		V_{DD} = 3.14V, I_{OL} = 12 mA
	PCI			$0.1V_{DD}$		V_{DD} = 3.14V, I_{OL} = 1.5 mA
	USB			0.3		R_L = 1.5 KΩ to V_{DD}, V_{DD} = 3.46V
V_{OH}	High Level Output Voltage (Note 1)					
	8 mA	2.4			V	V_{DD} = 3.14V, I_{OH} = -8 mA
	DOTCLK	2.4				V_{DD} = 3.14V, I_{OH} = -20 mA
	FP_CLK	2.4				V_{DD} = 3.14V, I_{OH} = -12 mA
	IDE	2.4				V_{DD} = 3.14V, I_{OH} = -400 µA
	PCI	$0.9V_{DD}$				V_{DD} = 3.14V, I_{OH} = -0.5 mA
	USB	2.8		V_{DD}		V_{DD} = 3.14V, R_L = 15 KΩ to V_{SS}
I_{LEAK}	Input Leakage Current Including Hi-Z Output Leakage (Note 1)					
	8 mA, CLK, DOTCLK, FP_CLK, IDE, PCI			+/-10	µA	V_{DD} = V_{DDIO} = 3.46V, V_{PAD} = 0 to 3.46V, Note 2
				+/-200		V_{DD} = V_{DDIO} = 3.46V, V_{PAD} = 3.46 to 5.5V, Note 2
I_{PU}	Weak Pull-Up Current (Note 1)					
	8 mA			-50	µA	V_{DDIO} = 3.46V, Note 2

Table 6-4. DC Characteristics (Continued)

Symbol	Parameter	Min	Typ	Max	Units	Comments
I_{OH}	Output High Current (Note 1)					
	8 mA			-8	mA	$V_{DD} = V_{DDIO} = V_{DDmin} = 3.14V$
	FP_CLK			-12		
	IDE			-0.5		
	PCI	-0.5				$V_{DD} = V_{DDIO} = V_{DDmin} = 3.14V$
I_{OL}	Output Low Current (Note 1)					
	8 mA			8	mA	$V_{DD} = V_{DDIO} = V_{DDmin} = 3.14V$
	FP_CLK			12		
	IDE			12		$V_{DD} = V_{DDIO} = V_{DDmin} = 3.14V$
	PCI	1.5				$V_{DD} = V_{DDIO} = V_{DDmin} = 3.14V$
V_H	Hysteresis Voltage 8 mA, CLK (Note 1)	350			mV	$V_{T+} - V_{T-}$
V_{DI}	USB - Differential Input Sensitivity	0.2			V	|(D+)-(D-)|, within V_{CM}, Note 3
V_{CM}	USB - Differential Common Mode Range	0.8		2.5	V	Includes V_{DI} range
V_{SE}	USB - Single Ended Receiver Threshold	0.8		2.0	V	
V_{CRS}	USB - Output Signal Crossover Voltage					
	Low Speed	1.3		2.0	V	V_{DD} = 3.14V to 3.46V, See Figure 6-9 and Figure 6-10 on page 245
	Full Speed	1.3		2.0	V	
C_{IN}	Input Capacitance (Note 1)					
	8 mA			5	pF	Note 3
	CLK	5		12		
	IDE			25		
	PCI			10		
C_{OUT}	Output Capacitance - All Digital Drivers			7	pF	Note 3

1. Pins with this buffer type are listed in Table 3-3 "352 PBGA Pin Assignments - Sorted Alphabetically by Signal Name" on page 25.
2. Pins with a pull-up always enabled are denoted in Table 6-1 "Pins with Weak Internal Pull-Up" on page 233. Note that the leakage specification does not apply to hard-wired pull-ups.
3. Not 100% tested.

6.4.1 Definition of System Conditions for Measuring "On" Parameters

The current of the CS5530A is highly dependent on the DCLK (DOT clock). Table 6-5 shows how these factors are controlled when measuring the typical average and absolute maximum CS5530A current parameters. Table 6-6 provides the CS5530A's core, DAC, and PLL DC characteristics during various power states.

Table 6-5. System Conditions Used to Determine CS5530A's Current Used During the "On" State

CPU Current Measurement	System Conditions	
	V_{DD} (Note 1)	DCLK Frequency (Note 2)
Typical Average	Nominal	50 MHz (Note 3)
Absolute Maximum	Max	135 MHz (Note 4)

1. See Table 6-3 on page 234 for nominal and maximum voltages.
2. Not all system designs support display modes that require a DCLK of 157 MHz. Therefore, absolute maximum current will not be realized in all system designs.
3. A DCLK frequency of 50 MHz is derived by setting the display mode to 800x600x8 bpp at 75 Hz, using a display image of vertical stripes (4-pixel wide) alternating between black and white with power management disabled.
4. A DCLK frequency of 157 MHz is derived by setting the display mode to 1280x1024x8 bpp at 85 Hz, using a display image of vertical stripes (1-pixel wide) alternating between black and white with power management disabled.

Table 6-6. DC Characteristics During Power States

Symbol	Parameter	Min	Typ	Max	Units	Comments
Core (Note 1)						
I_{DD_CORE}	Active I_{DD}		145	255	mA	Note 2 and Note 3
I_{DDAI_CORE}	Active Idle I_{DD}		85		mA	Note 4
I_{DDSM_CORE}	Suspend Mode I_{DD}		29		mA	Note 5
I_{DDSS_CORE}	Standby I_{DD}		5.7		mA	Note 6
DAC (Note 1)						
I_{DD_DAC}	Active I_{DD}		60	85	mA	Note 2 and Note 3
I_{DDAI_DAC}	Active Idle I_{DD}		60		mA	Note 4
I_{DDSM_DAC}	Suspend Mode I_{DD}		0.2		mA	Note 5
I_{DDSS_DAC}	Standby I_{DD}		0.2		mA	Note 6
PLL (Note 1)						
I_{DD_PLL}	Active I_{DD}		6	6	mA	
I_{DDAI_PLL}	Active Idle I_{DD}		6		mA	Note 4
I_{DDSM_PLL}	Suspend Mode I_{DD}		0.3		mA	Note 5
I_{DDSS_PLL}	Standby I_{DD}		0.2		mA	Note 6
EXTVREFIN						
$I_{DD\_EXTVREFIN}$	Active I_{DD}			75	µA	

1. Outputs unloaded.
2. Maximum current is measured under the following assumptions:
   PCICLK = 33 MHz, USBCLK = 48 MHz, DCLK = 157 MHz, and VID_CLK = 133 MHz.
3. Typical current is measured under the following assumptions:
   PCICLK = 33 MHz, USBCLK = 48 MHz, DCLK = 50 MHz, and VID_CLK = 0 MHz.
4. Active Idle current is measured under the following assumptions with SUSPA# asserted:
   PCICLK = 33 MHz, USBCLK = 48 MHz, DCLK = 50 MHz, and VID_CLK = 0 MHz.
5. Suspend current is measured under the following assumptions with SUSPA# asserted:
   PCICLK = 33 MHz, USBCLK = 48 MHz, DCLK = 0 MHz, and VID_CLK = 0 MHz.
6. Standby current is measured under the following assumptions with SUSPA# and SUSP_3V (stop clock signal) asserted:
   PCICLK = 0 MHz, USBCLK = 0 MHz, DCLK = 0 MHz, and VID_CLK = 0 MHz.

6.5 AC Characteristics

The following tables list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. The rising-clock-edge reference level, V_{REF}, and other reference levels are shown in Table 6-7. Input or output signals must cross these levels during testing.

Input setup and hold times are specified minimums that define the smallest acceptable sampling window for which a synchronous input signal must be stable for correct operation.

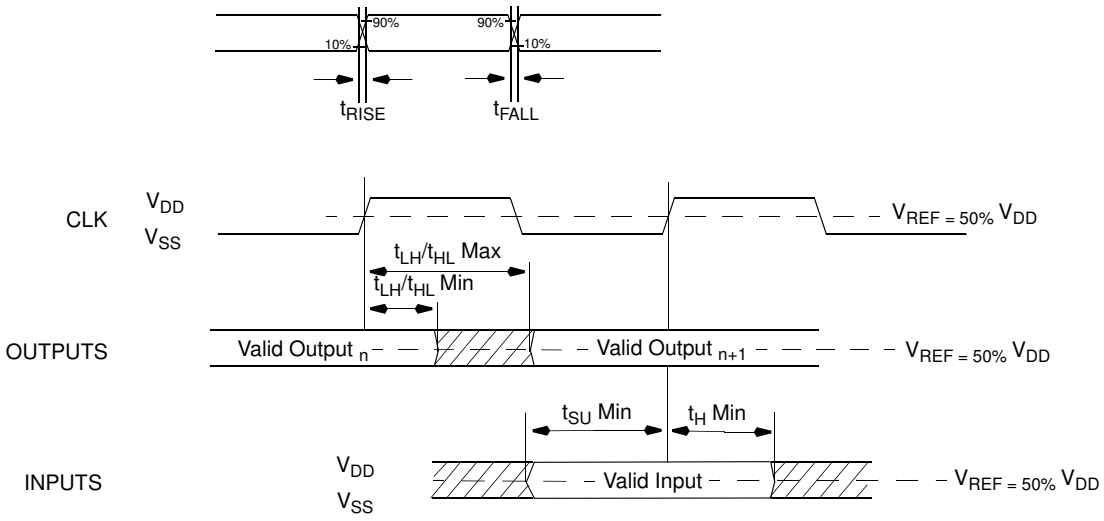
Table 6-7. Drive Level and Measurement Points for AC Characteristics

Symbol	Voltage (V)
V_{REF}	1.5
V_{DD}	3.14
V_{SS}	0

Table 6-8. AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments (Note 1)
t_{SU}	Input Setup Time to PCICLK	7			ns	See Figures 6-1 and 6-2 on page 240
t_H	Input Hold Time to PCICLK	0			ns	
t_{LH}	Low to High Propagation Delay (Referenced to PCICLK, Note 2)					
	PCI	2		11	ns	See Figure 6-2 on page 240 and Figure 6-3 on page 241 (also known as t_{VAL})
t_{HL}	High to Low Propagation Delay (Referenced to PCICLK, Note 2)					
	PCI	2		11	ns	See Figure 6-2 on page 240 and Figure 6-4 on page 241 (also known as t_{VAL})
$t_{RISE/FALL}$	Rising/Falling Edge Rate					
	IDE			1.25	V/ns	See Figures 6-1 and 6-2 on page 240, Note 3

1. All tests, unless otherwise specified, are at V_{DD} = 3.14V to 3.46V, T_C = 0°C to 85°C, and C_L = 50 pF.
2. Pins with this buffer type are listed in Table 3-3 "352 PBGA Pin Assignments - Sorted Alphabetically by Signal Name" on page 25.
3. Not 100% tested.



Legend:

t_{LH}/t_{HL} Max = Maximum Output Delay Specification
t_{LH}/t_{HL} Min = Minimum Output Delay Specification
t_{SU} Min = Minimum Input Setup Specification
t_H Min = Minimum Input Hold Specification

Note: See Table 6-7 "Drive Level and Measurement Points for AC Characteristics" on page 239 for V_{DD}, V_{SS}, and V_{REF} values.

Figure 6-1. Test Measurements for AC Characteristics

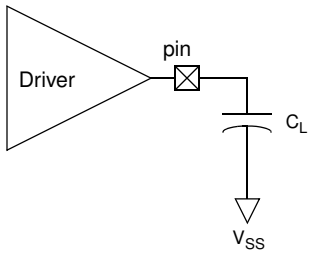


Figure 6-2. Test Circuit for AC Characteristics

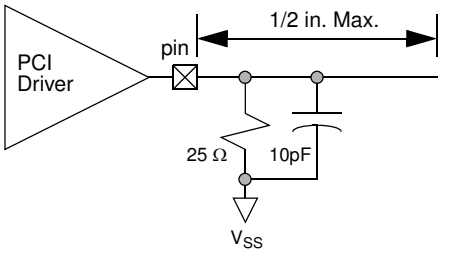


Figure 6-3. PCI Rising Edge (t_{LH}) Test Circuit

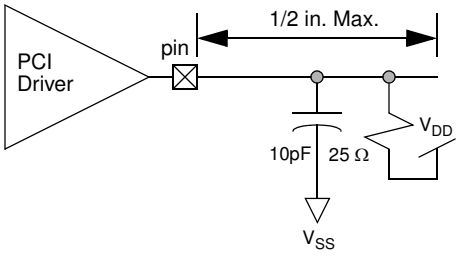


Figure 6-4. PCI Falling Edge (t_{HL}) Test Circuit

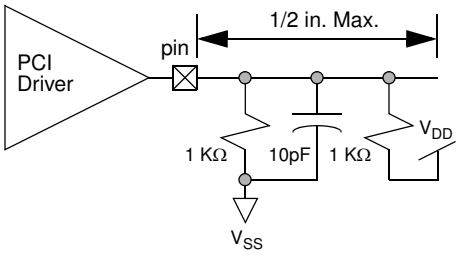


Figure 6-5. PCI Slew Rate Test Circuit

Table 6-9. Clock and Reset Specifications

Symbol	Parameter	Min	Max	Duty Cycle	Unit	Comments (Note 1)
Output Signals						
--	DCLK Frequency	25	157.5	40/60	MHz	Note 2
--	CLK_32K Frequency	32.768		50/50	kHz	Note 3
--	ISACLK Frequency		8.33333		MHz	
Input Signals						
--	CLK_14MHZ Frequency	14.31818		45/55	MHz	
--	USBCLK Frequency	48			MHz	
--	TVCLK Frequency		27		MHz	
--	VID_CLK Frequency		135		MHz	
t_{CYC}	PCICLK Cycle Time	30			ns	Note 4
t_{HIGH}	PCICLK High Time	11			ns	
t_{LOW}	PCICLK Low Time	11			ns	
--	PCICLK Slew Rate	1	4		V/ns	See Figure 6-1 on page 240 and Figure 6-5 on page 241 (known as $slew_r/slew_f$), Note 5, and Note 6
--	PCI_RST# Slew Rate	50	--		mV/ns	Rising edge only (deassertion), Note 6

1. All tests, unless otherwise specified, are at V_{DD} = 3.14V to 3.46V, T_C = 0°C to 85°C, and C_L = 50 pF.
2. Worst case duty cycle. Duty cycle is a function of PLL post divider. DCLK is programmable to standard video frequencies. Typical jitter < 650 ps peak-to-peak. CLK_14MHZ input jitter < 500 ps peak-to-peak.
3. CLK_32K jitter = period of CLK_14MHZ. CLK_32K output frequency = CLK_14MHZ/436.95621.
4. Frequency of operation is from DC to 33 MHz but at a single fixed frequency. Operation below 20 MHz is guaranteed by design.
5. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in Figure 6-6.
6. Not 100% tested.

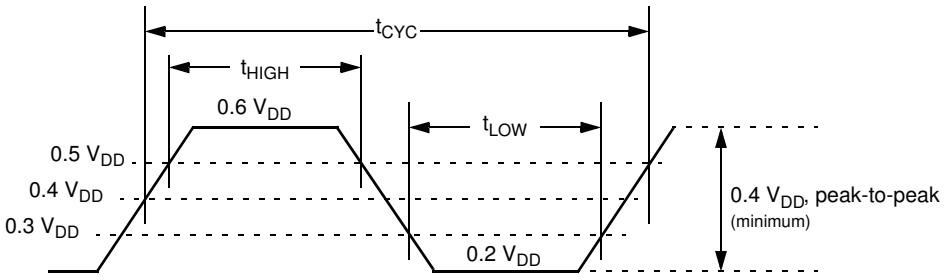


Figure 6-6. 3.3V PCICLK Waveform

Table 6-10. DCLK PLL Specifications

Symbol	Parameter	Min	Typ	Max	Units	Comments (Note 1)
f_{DCLK}	DCLK Clock Operating Frequency	25		157.5	MHz	Also known as CRT clock
f_{REF}	Input Reference Frequency		14.318		MHz	
$t_{RISE/FALL}$	Output Clock Rise/Fall Time			2	ns	@ 25 MHz
--	Jitter, Peak-to-Peak	-300		300	ps	
DC	Duty Cycle	40/60		60/40	%	

1. All tests, unless otherwise specified, are at V_{DD} = 3.14V to 3.46V, T_C = 0°C to 85°C, and C_L = 50 pF.

Table 6-11. CPU Interface Timing

Symbol	Parameter	Min	Max	Units	Comments (Note 1)
t_{SMI}	Rising PCICLK to SMI#	3	16	ns	
$t_{SUSP\#}$	Rising PCICLK to SUSP#	6	9	ns	
$t_{SUSPASetup}$	SUSPA# Setup to Rising PCICLK	0		ns	
$t_{SUSPAHold}$	SUSPA# Hold from Rising PCICLK	3		ns	
--	IRQ13 Input	Asynchronous input for IRQ decode.			
--	INTR Output	Asynchronous output from IRQ decode.			
--	SMI# Output	Asynchronous output from SMI decode.			

1. All tests, unless otherwise specified, are at V_{DD} = 3.14V to 3.46V, T_C = 0°C to 85°C, and C_L = 50 pF.

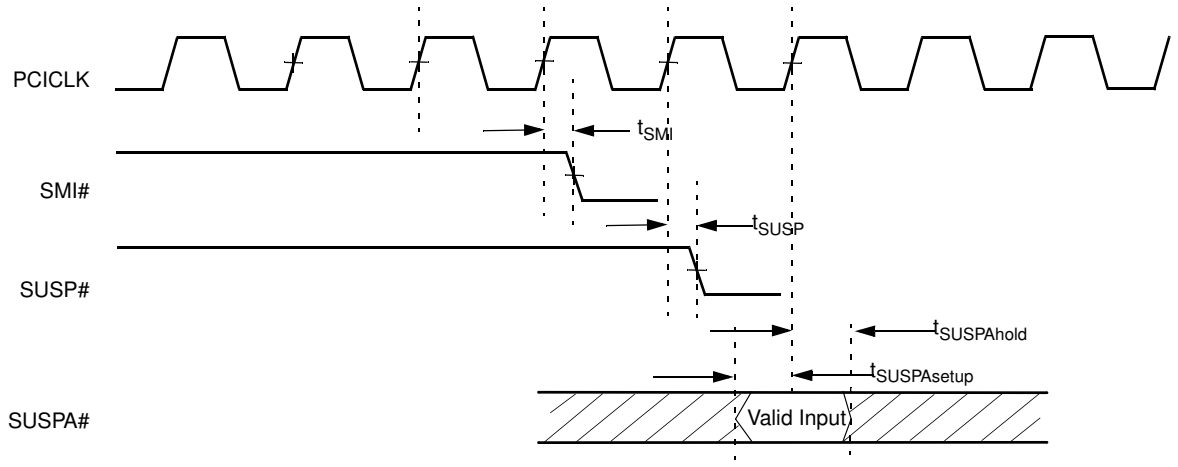


Figure 6-7. CPU Interface Timing

Table 6-12. Audio Interface Timing

Symbol	Parameter	Min	Max	Units	Comments (Note 1)
t_{BITCLK}	Rising BIT_CLK to SYNC		15	ns	
t_{SDAT}	Rising BIT_CLK to SDATA_OUT		15	ns	
$t_{SDATsetup}$	SDATA_IN setup to falling BIT_CLK	10		ns	
$t_{SDAThold}$	SDATA_IN hold from falling BIT_CLK	10		ns	

1. All tests, unless otherwise specified, are at V_{DD} = 3.14V to 3.46V, T_C = 0°C to 85°C, and C_L = 50 pF.

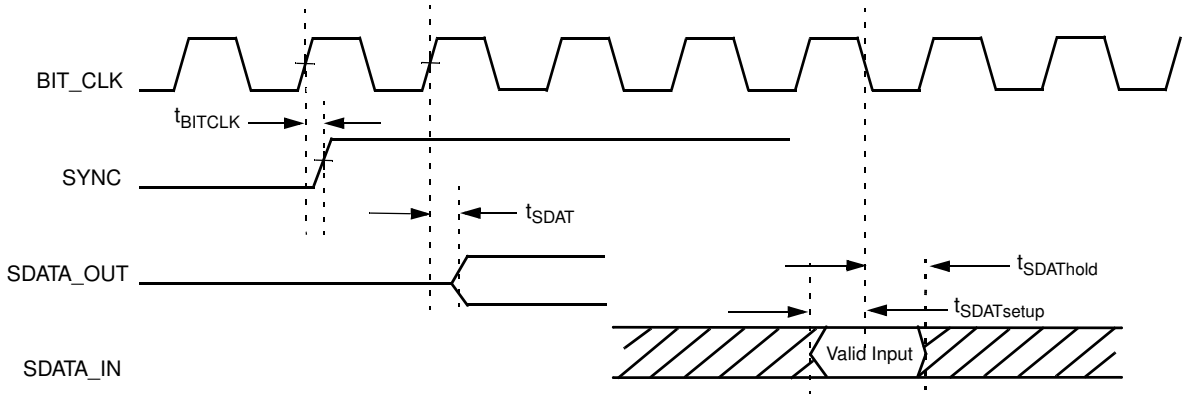


Figure 6-8. Audio Interface Timing

Table 6-13. USB Timing

Symbol	Parameter	Min	Max	Unit	Comments (Note 1)
Full Speed Mode					
t_R	Rise Time	4	20	ns	
t_F	Fall Time	4	20	ns	
Low Speed Mode					
t_R	Rise Time	75		ns	
			300		C_L = 350 pF
t_F	Fall Time	75		ns	
			300		C_L = 350 pF

1. All tests, unless otherwise specified, are at V_{DD} = 3.14V to 3.46V, T_C = 0°C to 85°C, and C_L = 50 pF.

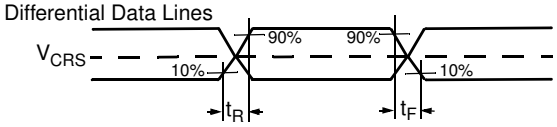


Figure 6-9. USB Timing

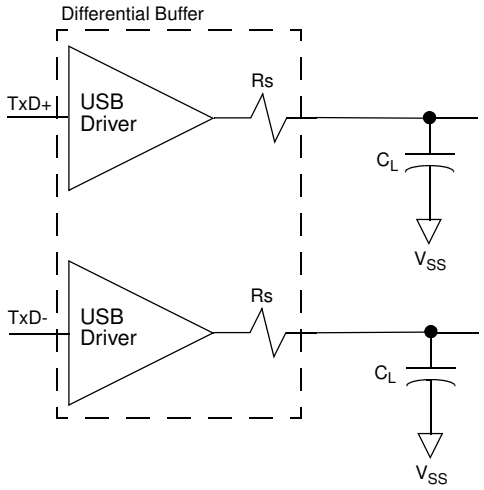


Figure 6-10. USB Test Circuit

6.6 Display Characteristics

The following tables and figures describe the characteristics of the CRT, TFT/TV and MPEG Display interfaces. It is divided into the following categories:

- CRT Display Recommended Operating Conditions
- CRT Display Analog (DAC) Characteristics
- Display Miscellaneous Characteristics
- CRT, TFT/TV and MPEG Display Timing

Additionally, Figure 6-13 on page 249 is provided showing a typical video connection diagram.

Table 6-14. CRT Display Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Comments
AV_{DD}	Power Supply connected to AV_{DD1}, AV_{DD2} and AV_{DD3}	3.14	3.3	3.46	V	
R_L	Output Load on each of the pins IOUTR, IOUTG and IOUTB		37.5		Ohms	R1, R2, and R3 as shown in Figure 6-13 on page 249
I_{OUT}	Output Current on each of the pins IOUTR, IOUTG and IOUTB			21	mA	
R_{SET}	Value of the full-scale adjust resistor connected to IREF		680		Ohms	This resistor should have a 1% tolerance.
$VEXT_{REF}$	External voltage reference connected to the EXTVREFIN pin		1.235		V	

Table 6-15. CRT Display Analog (DAC) Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Comments (Note 1)
V_{OM}	Output Voltage			0.735	V	
V_{OC}	Output Current			20	mA	
INL	Integral Linearity Error			+/-1	LSB	
DNL	Differential Linearity Error			+/-1	LSB	
t_{FS}	Full Scale Settling Time			2.5	ns	
--	DAC-to-DAC matching			5	%	
--	Power Supply Rejection			0.7	%	@ 1 KHz
t_{RISE}	Output Rise Time			3.8	ns	Note 2 and Note 3
t_{FALL}	Output Fall Time			3.8	ns	Note 2 and Note 4

1. All tests, unless otherwise specified, are at V_{DD} = 3.14V to 3.46V, T_C = 0°C to 85°C, and C_L = 50 pF.
2. Timing measurements are made with a 75 ohm doubly-terminated load, with $VEXT_{REF}$ = 1.235V and R_{SET} = 680 ohms.
3. 10% to 90% of full-scale transition.
4. Full-scale transition: time from output minimum to maximum, not including clock and data feedthrough.

Table 6-16. Display Miscellaneous Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Comments
	White Level Relative to Black	16.74	17.62	18.50	mA	
IAV_{DD}	AV_{DD} Supply Current		60		mA	(Static)

Table 6-17. CRT, TFT/TV and MPEG Display Timing

Symbol	Parameter	Min	Typ	Max	Units	Comments (Note 1)
Setup/Hold Time						
$t_{DisplaySetup}$	Display Setup to Rising PCLK: VSYNC, HSYNC, ENA_DISP, FP_VSYNC, FP_HSYNC, PIXEL[23:0]	2.2			ns	See Figure 6-1 on page 240.
$t_{DisplayHold}$	Display Hold from Rising PCLK: VSYNC, HSYNC, ENA_DISP, FP_VSYNC, FP_HSYNC, PIXEL[23:0]	1.0			ns	
$t_{VID\_VALSetup}$	VID_VAL Setup to Rising VID_CLK	3.0			ns	See Figure 6-1 on page 240.
$t_{VID\_VALHold}$	VID_VAL Hold from Rising VID_CLK	0.8			ns	
$t_{VID\_DATASetup}$	VID_DATA Setup to Rising VID_CLK	3.0			ns	See Figure 6-1 on page 240, Note 2
$t_{VID\_DATAHold}$	VID_DATA Hold from Rising VID_CLK	0.8			ns	
Clock Specification						
t_{VID_CLKMin}	VID_CLK Minimum Clock Period	7.4			ns	
Delay Time						
$FPOUT_{MinDelay}$, $FPOUT_{MaxDelay}$	TFT/TV Output Delays from FP_CLK: FP_DATA[17:0], FP_HSYNC_OUT, FP_VSYNC_OUT, FP_DISP_ENA_OUT, FP_ENA_VDD, FP_ENA_BKL, FP_CLK_EVEN	0.5		4.5	ns	Note 3
$VID\_RDY_{MinDelayE}$, $VID\_RDY_{MaxDelayE}$	VID_RDY Delay from Falling VID_CLK (early mode)	3.0		10.5	ns	Note 4
$VID\_RDY_{MinDelayN}$, $VID\_RDY_{MaxDelayN}$	VID_RDY delay from rising VID_CLK (normal mode)	3.0		9.5	ns	

1. All tests, unless otherwise specified, are at V_{DD} = 3.14V to 3.46V, T_C = 0°C to 85°C, and C_L = 50 pF.
2. Also applies to PIXEL[23:16] when in 16-bit video mode.
3. All flat panel applications use the falling edge of FP_CLK to latch their data.
4. The mode for VID_RDY (early or normal) is set with bit 25 of the Video Configuration Register (F4BAR+Memory Offset 00h[25]).

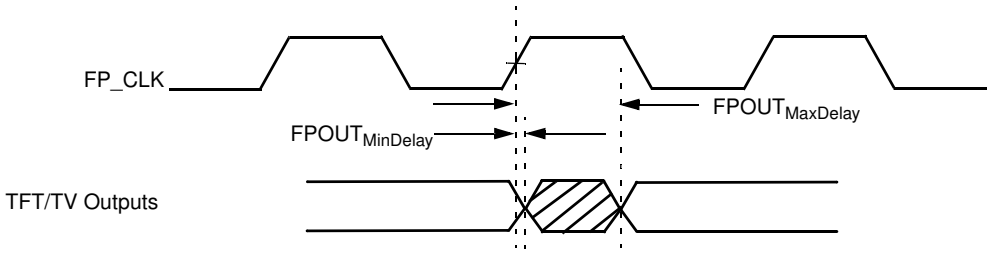


Figure 6-11. Display TFT/TV Outputs Delays

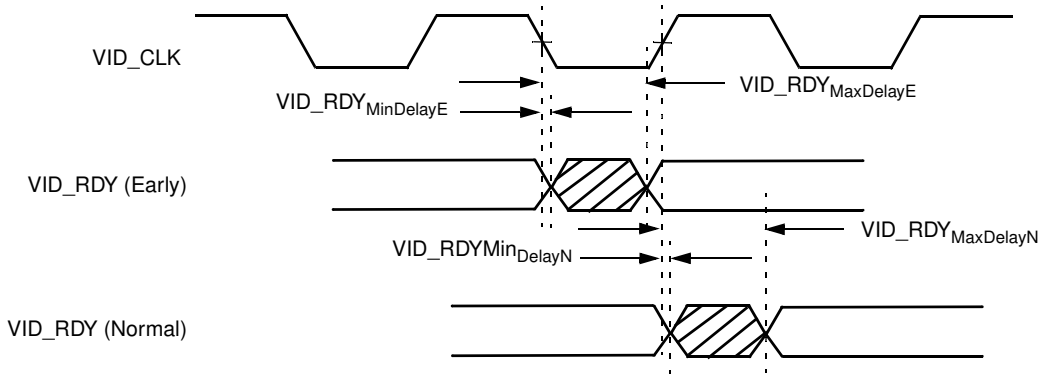
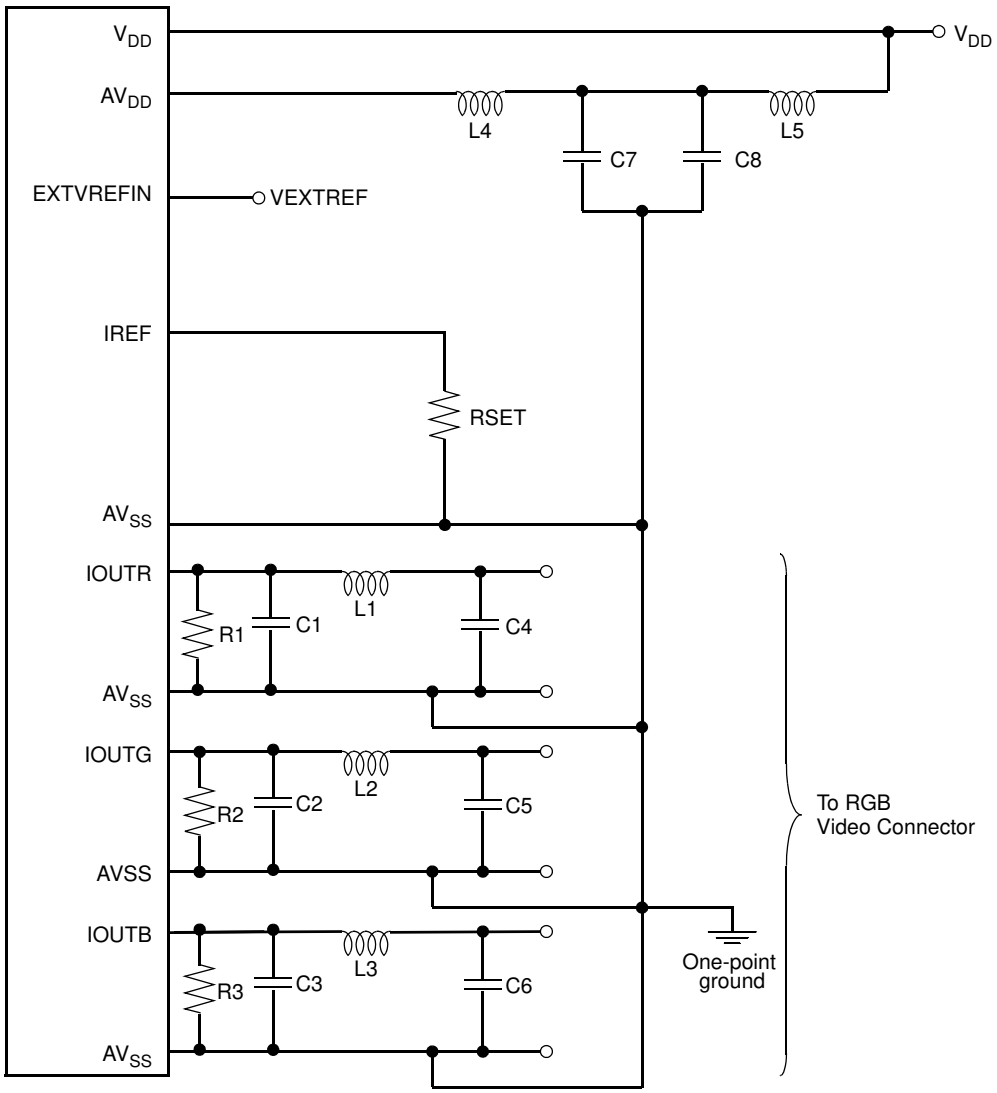


Figure 6-12. MPEG Timing



Legend

Part Designator	Value
R1-R3	75 Ohms, 1%
RSET	732 Ohms, 1%
C1-C6	33 pF
C7	0.1 µF, Ceramic
C8	2.2 µF, Electrolytic
L1-L3 (Optional)	120 Ohm Ferrite Bead
L4-L5 (Optional)	600 Ohm Ferrite Bead

Figure 6-13. Typical Video Connection Diagram

7 Test Mode Information

The CS5530A provides two test modes:

1) The NAND tree test mode for board-level automatic test equipment (ATE).
2) The I/O test mode for system design testing.

7.1 NAND Tree Test Mode

The NAND tree mode is used to test input and bidirectional pins which will be part of the NAND tree chain. Table 7-1 shows how to set the device for the NAND tree test.

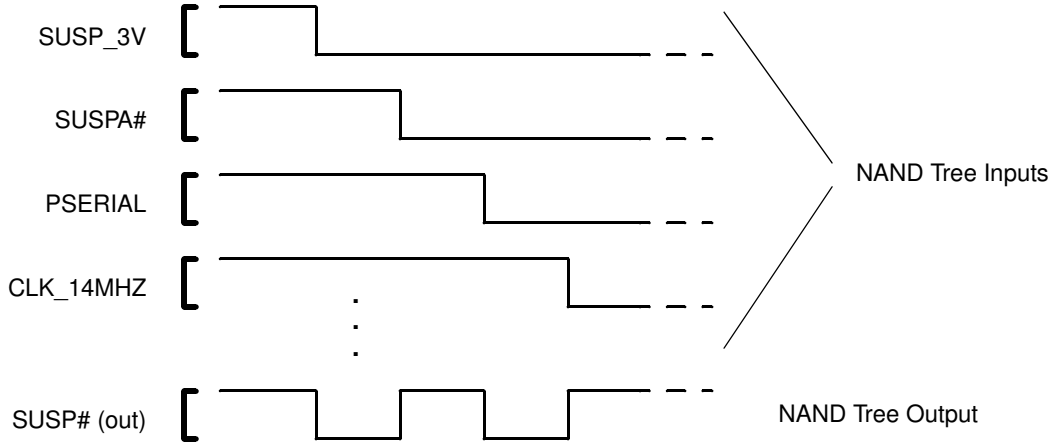
The output of the NAND tree is multiplexed on the SUSP# output (pin K26). After a POR# (pin K24) pulse, all inputs in Table 7-2 on page 252 are initialized to a “1” and then are successively pulled and held to a “0” starting with SUSP_3V (the first input pin in the tree). The output waveform on SUSP# will toggle on each input change as shown in Figure 7-1.

POR# is included as an input during the NAND Tree test, after being used to trigger the test first. IRQ7 (pin AD14) and TEST (pin D3) must be held high throughout the test.

Table 7-1. NAND Tree Test Selection

Signal Name	Pin No.	Setting
POR#	K24	0 -> 1
TEST	D3	1
IRQ7	AD14	1

Initial Conditions: TEST = 1, IRQ7 = 1, POR# = (first 0, then 1), all inputs ‘1’



The following pins are not in the NAND tree: AEN, BALE, CPU_RST, DACK[3:0]#, DACK[7:5]#, DCLK, DDC_SCL, D+_PORT1, D–_PORT1, D+_PORT2, D–_PORT2, EXTVREFIN, FP_CLK, FP_CLK_EVEN, FP_DISP_ENA_OUT, FP_ENA_BKL, FP_ENA_VDD, FP_HSYNC_OUT, FP_VSYNC_OUT, GPCS#, GPORT_CS#, HSYNC_OUT, IDE_ADDR[2:0], IDE_CS[1:0]#, IDE_DACK[1:0]#, IDE_IOR[1:0]#, IDE_IOW[1:0]#, IDE_RST#, IOUTB, IOUTG, IOUTR, IREF, IRQ7, ISACLK, KBROMCS#, PC_BEEP, PCI_RST#, PLLTEST, SA_LATCH, SDATA_OUT, SMEMR#/RTCALE, SMEMW#/RTCCS#, SUSP#, SYNC, TEST, VID_RDY, VSYNC_OUT, all NCs, and all analog/digital supplies.

Figure 7-1. Example: NAND Tree Output Waveform

Table 7-2. NAND Tree Test Mode Pins

Signal Name	Pin No.
SUSP_3V	L24
SUSPA#	L25
PSERIAL	L26
CLK_14MHZ	P24
SMI#	P25
INTR	P26
IRQ13	R23
IDE_DATA7	U23
IDE_DATA6	U24
IDE_DATA8	V24
IDE_DATA10	V25
IDE_DATA5	W26
IDE_DATA9	Y25
IDE_DATA11	Y24
IDE_DATA4	AA26
IDE_DATA12	AA25
IDE_DATA3	AB26
IDE_DATA1	AA24
IDE_DATA13	AB25
IDE_DATA2	AB24
IDE_DATA0	AC26
IDE_DATA14	AC25
IDE_DATA15	AB23
IDE_DREQ1	AC24
IDE_DREQ0	AD26
IDE_IORDY0	AD25
IDE_IORDY1	AE26
SA14/SD14	AD24
SA15/SD15	AE25
GPIO0	AC22
GPIO1	AE24
GPIO2	AF25
GPIO3	AF24
GPIO4	AD22
GPIO5	AC21
GPIO6	AE23
GPIO7	AF23
SA13/SD13	AE22
SA10/SD10	AC20
DRQ7	AF22
SA12/SD12	AE21
SA11/SD11	AF21
SA9/SD9	AD19
DRQ6	AE20
MEMW#	AF20
MEMR#	AE19
DRQ5	AD18
SA8/SD8	AF19
DRQ0	AE18
IRQ11	AF18
IRQ14	AC17
IRQ15	AD17
SBHE#	AE17

Signal Name	Pin No.
IRQ12	AF17
IRQ10	AE16
IOCS16#	AF16
MEMCS16#	AC15
IRQ4	AE15
TC	AF15
IRQ3	AC14
IRQ8#	AE14
IRQ6	AF14
DRQ3	AD13
IRQ5	AE13
IRQ1	AF13
DRQ1	AD12
IOR#	AE12
SA17	AF12
IOW#	AC11
SA16	AD11
SA18	AE11
IOCHRDY	AF11
SA19	AD10
DRQ2	AE10
ZEROWS#	AF10
SA2/SD2	AD9
SA0/SD0	AE9
SA4/SD4	AF6
SA1/SD1	AE6
SA6/SD6	AF5
SA3/SD3	AC6
IRQ9	AE5
SA5/SD5	AD5
SA7/SD7	AF4
CLK_32K	AE3
OVER_CUR#	W3
POWER_EN	V4
USBCLK	W1
BIT_CLK	V2
SDATA_IN	U4
DDC_SDA	M4
FP_DATA12	L1
FP_DATA0	K3
FP_DATA13	K2
FP_DATA14	K1
FP_DATA2	J3
FP_DATA1	J2
FP_DATA3	J1
FP_DATA15	H2
FP_DATA16	H3
FP_DATA4	H1
FP_DATA8	G1
FP_DATA5	G2
FP_DATA7	G3
FP_DATA6	G4
FP_DATA9	F1

Signal Name	Pin No.
FP_DATA17	F3
FP_DATA10	E2
FP_DATA11	D1
FP_VSYNC	C1
FP_HSYNC	C2
ENA_DISP	B1
TVCLK	B2
PIXEL0	A1
PIXEL3	C4
PIXEL6	D5
PIXEL4	B3
PIXEL1	A2
PIXEL2	A3
PIXEL11	C5
PIXEL9	D6
PIXEL5	B4
PIXEL7	A4
HSYNC	C6
VSYNC	B5
PIXEL13	D7
PIXEL14	C7
PIXEL10	A5
PIXEL8	B6
VID_CLK	A6
PIXEL17	C8
VID_VAL	B7
PIXEL12	A7
PIXEL15	B8
PIXEL20	D9
PIXEL21	C9
PIXEL16	A8
PIXEL18	B9
PIXEL19	A9
PIXEL23	C10
VID_DATA4	D11
VID_DATA3	C11
PIXEL22	B11
VID_DATA0	A11
VID_DATA7	C12
VID_DATA6	B12
VID_DATA5	A12
VID_DATA1	C13
VID_DATA2	B13
PCLK	A13
AD1	D14
INTD#	B14
INTA#	A14
INTB#	D15
INTC#	C15
AD3	B15
AD0	A15
AD2	C16
AD5	B16

Signal Name	Pin No.
AD7	A16
AD4	C17
AD6	B17
AD9	A17
AD8	D18
C/BE0#	B18
AD12	A18
AD11	B19
AD10	A19
AD15	A20
AD14	B20
AD13	C20
PAR	A21
C/BE1#	B21
SERR#	A22
PERR#	B22
LOCK#	C22
DEVSEL#	A23
TRDY#	B23
FRAME#	C23
C/BE2#	A24
IRDY#	B24
AD17	A25
AD18	B25
AD16	A26
GNT#	D24
AD21	C25
AD19	B26
AD22	C26
AD20	E24
AD26	D25
C/BE3#	D26
AD23	E25
AD25	G24
STOP#	E26
AD24	F25
AD27	F26
AD28	G25
AD29	G26
AD31	H25
AD30	J24
HOLD_REQ#	H26
REQ#	J25
PCICLK	J26
POR#	K24

7.2 I/O Test

This test affects all output and bidirectional pins. To trigger the I/O test, set the TEST and IRQ[3:7] pins according to Table 7-3, while holding POR# low. The test begins when POR# is brought high. Starting with the next rising edge of PCICLK, the states listed in Table 7-4 are entered by all digital output and I/O pins on successive PCICLK pulses:

Table 7-3. I/O Test Selection

Signal Name	Pin No.	Setting
POR#	K24	X
TEST	D3	1
IRQ3	AC14	0
IRQ4	AE15	1
IRQ5	AE13	1
IRQ6	AF14	0
IRQ7	AD14	1

Table 7-4. I/O Test Sequence

Clock #	Output Pin States
Before 1	Undefined
1	Floating
2	High
3	Low
4	Floating
5	Low
6	High
7	Floating
8 and beyond	Undefined

The following pins are INCLUDED in this test:

- AD[31:0], AEN, BALE, C/BE[3:0]#, CLK_32K, CPU_RST, DACK[7:5,3:0], DDC_SCL, DDC_SDA, DEVSEL#, FP_CLK, FP_CLK_EVEN, FP_DATA[17:0], FP_DISP_ENA_OUT, FP_ENA_BKL, FP_ENA_VDD, FP_HSYNC_OUT, FP_VSYNC_OUT, FRAME#, GPCS#, GPIO[7:0], GPORT_CS#, HOLD_REQ#, HSYNC_OUT, IDE_ADDR[2:0], IDE_CS[1:0]#, IDE_DACK[1:0]#, IDE_DATA[15:0], IDE_IOR[1:0]#, IDE_IOW[1:0]#, IDE_RST#, INTR, IOCHRDY, IOR#, IOW#, IRDY#, ISACLK, KBROMCS#, LOCK#, MEMCS16#, MEMR#, MEMW#, PAR, PCI_RST#, PC_BEEP, PERR#, POWER_EN, REQ#, SA/SD[15:0], SA[19:16], SA_LATCH, SBHE#, SDATA_OUT, SERR#, SMEMR#, SMEMW#, SMI#, STOP#, SUSP#, SUSP_3V, SYNC, TC, TRDY#, VID_RDY, VSYNC_OUT

Note: The SA/SD and SA bus, IOR#, IOW#, MEMR#, MEMW# and SBHE# pins never actually float, because they have internal weak pull-up devices that remain active.

The following pins are EXCLUDED from this test:

- Input-only pins: BIT_CLK, CLK_14MHZ, DRQ[7:5,3:0], ENA_DISP, FP_HSYNC, FP_VSYNC, GNT#, HSYNC, IDE_DREQ[1:0], IDE_IORDY[1:0], INTA#, INTB#, INTC#, INTD#, IOCS16#, IRQ1, IRQ[7:3], IRQ8#, IRQ[15:9], OVER_CUR#, PCICLK, PCLK, PIXEL[23:0], POR#, PSERIAL, SDATA_IN, SUSPA#, TEST, TVCLK, USBCLK, VID_CLK, VID_DATA[7:0], VID_VAL, VSYNC, ZEROWS#.
- USB pins: D+_PORT1, D–_PORT1, D+_PORT2, D–_PORT2, AV_{DD}_USB, AV_{SS}_USB.
- Time-critical output: DCLK.
- Analog pins (including supplies): EXTVREFIN, IOUTB, IOUTG, IOUTR, IREF, PLLAGD, PLLDGN, PLLDVD, PLLTEST, AV_{DDx}, AV_{SSx}.
- Digital supply pins (V_{DD}, V_{SS}) and No Connects (NC).

8 Physical Dimensions

The physical dimensions for the 352 PBGA (Plastic Ball Grid Array) package are provided in Figure 8-1.

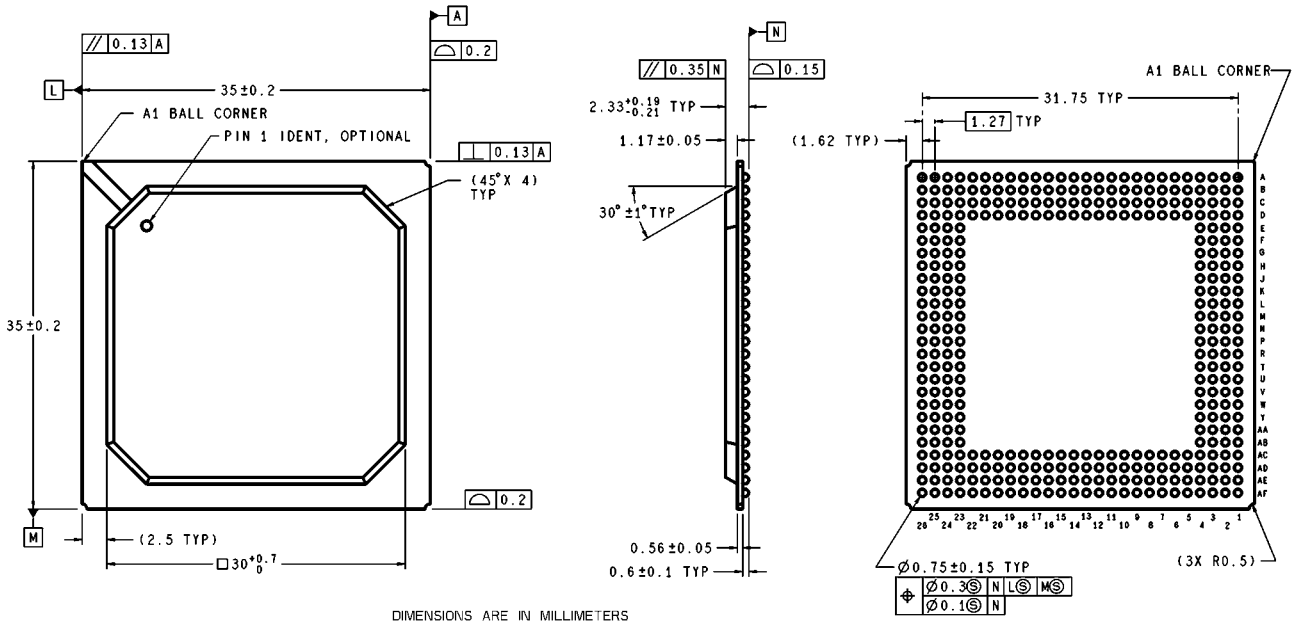


Figure 8-1. 352 PBGA Mechanical Package Outline

A Support Documentation

A.1 Revision History

This document is a report of the revision/creation process of the architectural specification for the CS5530A companion device. Any revisions (i.e., additions, deletions, parameter corrections, etc.) are recorded in the table(s) below.

Table A-1. Revision History

Revision # (PDF Date)	Revisions / Comments
0.1 (4/2/00)	Completed formatting first-pass of spec. Current spec is updated version of CS5530 data book with additional inputs from engineering. Differences between this spec's revision and the CS5530 data book are denoted with a change bar in the margin. Still need to proof-read for "ripple effects" made by engineering changes for next rev.
0.2 (6/16/00)	Corrections from Issues 1.3.
0.3 (6/27/00)	Further corrections from Issues 1.3. Partly indexed.
0.4 (7/5/00)	Corrections from Issues 1.3 and 1.5. Some issues remain to be resolved. Index markers inserted through AT chapter.
0.5 (7/19/00)	TME/Tech Pubs edits. See document revision 0.5 for revision history.
0.6 (8/7/00)	TME/Tech Pubs edits. See document revision 0.6 for revision history details.
0.7(9/18/00)	TME/Tech Pubs/Engr edits. See document revision 0.7 for revision history details. **Note:** Next revision to include section on "recommended soldering parameters" in Section 8.0 "Physical Dimensions".
1.0 (11/10/00)	TME/Tech Pubs/Engr edits. See document revision 1.0 for revision history details. **Note:** Will create separate applications note on "recommended soldering parameters" as opposed to adding as subsection in data book.
1.1 (5/1/01)	TME/Engr edits. See Table A-2 for details. **Note:** Will not create separate applications note on "recommended soldering parameters". Applications is fulfilling any customer inquiries with a document supplied by the Quality Group.

Table A-2. Edits to Create Revision 1.1

Section	Description
Section 3.0 "Signal Definitions"	
Section 3.2.2 "Clock Interface"	• Changed last sentence of DCLK signal description on page 29. Did say: "However, system constraints limit DCLK to 150 MHz when DCLK is used as the graphics subsystem clock." Now says: "However, when DCLK is used as the graphics subsystem clock, the Geode processor determines the maximum DCLK frequency."
Section 3.2.11 "Display Interface"	• Changed resistor value in IREF signal description (from 732 ohm to 680 ohm) on page 41.

Table A-2. Edits to Create Revision 1.1 (Continued)

Section	Description
Section 4.8 "Display Subsystem Extensions"	
Section 4.8.3 "Video Overlay"	• Added sentence to last paragraph on page 137: — "However, system maximum resolution is not determined by the CS5530A since it is not the source of the graphics data and timings." • Section 4.8.5.3 "Flat Panel Support" on page 139 — Added subsection titled "Flat Panel Power-Up/Down Sequence".
Section 6.0 "Electrical Specifications"	
Section 6.5 "AC Characteristics"	• Table 6-8 "AC Characteristics" on page 239: — Removed 8 mA, DOTCLK, and FP_CLK t_{LH} and t_{HL} parameters. • Table 6-10 "DCLK PLL Specifications" on page 243: — Removed Jitter, Sigma One parameter from table (completely). • Table 6-11 "CPU Interface Timing" on page 243: — Changed t_{SMI} max value from 9 ns to 16 ns. — Changed $t_{SUSPAHold}$ min value from 1 ns to 3 ns. • Table 6-15 "CRT Display Analog (DAC) Characteristics" on page 246: — Added V_{OM} max value of 0.735V. — Added V_{OC} max value of 20 mA. — Added t_{FS} max value of 2.5 ns. — Removed C_{OUT} parameter from table (completely). — Changed t_{RISE} max value from 3 to 3.8 ns. — Added t_{FALL} max value of 3.8 ns. — Changed R_{SET} value in Note 2 from 732 ohms to 680 ohms. • Table 6-17 "CRT, TFT/TV and MPEG Display Timing" on page 247: — Changed $t_{DisplaySetup}$ min value from 2.5 ns to 2.2 ns. — Changed $t_{VID\_VALSetup}$ min value from 3.75 ns to 3.0 ns. — Changed $t_{VID\_VALHold}$ min value from 0 ns to 0.8 ns. — Changed $t_{VID\_DATASetup}$ min value from 3.75 ns to 3.0 ns. — Changed $t_{VID\_DATAHold}$ min value from 0 ns to 0.8 ns. — Changed t_{VID_CLKMin} parameter description from "VID_CLK Minimum Pulse Width" to "VID_CLK Minimum Clock Period". — Changed $FPOUT_{MinDelay}$, $FPOUT_{MaxDelay}$ min value from 0.1 ns to 0.5 and max value from 5.2 ns to 4.5 ns.

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