CH92C64 Dual Graphics Clock Generator

Features

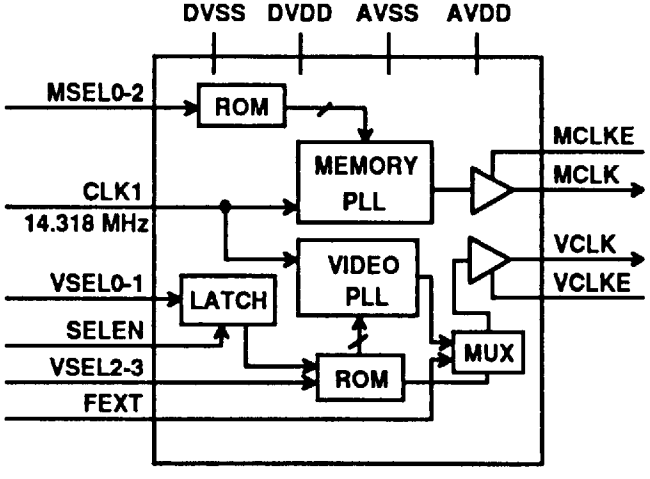
- 16 video clock frequencies, including one external frequency input, and 8 memory clock frequencies
- Supports graphic standards such as VGA, SuperVGA, XGA, and 8514A
- Supports output frequencies up to 135 MHz
- Backward pin compatible with ICS90C64/64A and ICS90C63
- Optimized to support WD90CXX graphics controller
- Built-in power supply conditioning circuitry for excellent jitter performance
- Proprietary VCO design for low phase jitter
- No need for external V_{DD} dropping resistor
- Only one external decoupling capacitor is needed
- High performance, low power CMOS technology
- Available in 20-pin plastic DIP, SOIC and PLCC
- 5V and 3.3V supply

Description

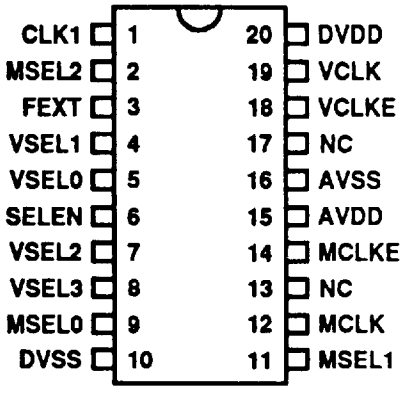
The *Chrontel* CH92C64 is a dual phase-locked loop frequency synthesizer designed for low power and high performance applications, such as graphics systems based on the VGA, SuperVGA, XGA, and 8514A formats. It can also be used in any application requiring multiple clocks, such as disk drives, CD-ROM systems, FAX-modems, etc.

To support the latest generation of high performance graphics controllers, CH92C64 provides separate memory clock (MLCK) and video clock (VCLK) outputs. The reference frequency is 14.318 MHz, which can be derived from the AT system bus or a crystal oscillator.

CH92C64 has built-in power supply conditioning circuitry which shields internal circuitry operation from external power supply noise variations. Therefore, low phase jitter is maintained in a noisy environment.



BLOCK DIAGRAM



PINOUT DIAGRAM

CH9001 Frequency Tables

Video Clock

VSEL				VCLK (MHz)	VCLK (MHz)
3	2	1	0	desired	actual
0	0	0	0	30.0	30.000
0	0	0	1	77.25	77.318
0	0	1	0	FEXT	70.289
0	0	1	1	80.0	79.943
0	1	0	0	31.5	31.500
0	1	0	1	36.0	36.121
0	1	1	0	75.0	75.000
0	1	1	1	50.0	49.802
1	0	0	0	40.0	39.972
1	0	0	1	50.0	49.802
1	0	1	0	32.0	32.005
1	0	1	1	44.9	44.864
1	1	0	0	25.175	25.189
1	1	0	1	28.322	28.325
1	1	1	0	65.0	64.983
1	1	1	1	36.0	36.121

Memory Clock

MSEL			MCLK (MHz)	MCLK (MHz)
2	1	0	desired	actual
0	0	0	33.0	33.011
0	0	1	49.218	49.180
0	1	0	60.0	60.000
0	1	1	30.5	30.504
1	0	0	41.612	41.612
1	0	1	37.5	37.500
1	1	0	36.0	36.121
1	1	1	44.296	44.297

Pin Description

Pin	Type	Symbol	Description
1	In	CLK1	Reference frequency input
2, 9, 11	In	MSEL2, MSEL0, MSEL1	Memory clock select inputs (internal pull-up)
3	In	FEXT	External frequency input (internal pull-down)
4, 5, 7, 8	In	VSEL1, VSEL0, VSEL2, VSEL3	Video clock select inputs (internal pull-up)
6	In	SELEN	VSEL0 and VSEL1 strobe input (rising edge)
10	Power	DVSS	Digital ground
12	Out	MCLK	Memory clock output
13, 17	—	NC	No connect, **MUST BE LEFT OPEN**
14	In	MCLKE	Memory clock output enable (internal pull-up)
15	Power	AVDD	Analog 5V supply
16	Power	AVSS	Analog ground
18	In	VCLKE	Video clock output enable (internal pull-up)
19	Out	VCLK	Video clock output
20	Power	DVDD	Digital 5V supply

Absolute Maximum Ratings

Symbol	Description	Value	Unit
V_{DD}	Power supply voltage with respect to Vss	−0.5 to +7.0	V
V_{IN}	Input voltage on any pin with respect to Vss	−0.5 to V_{DD}+0.5	V
T_{STOR}	Storage temperature	−55 to +150	°C

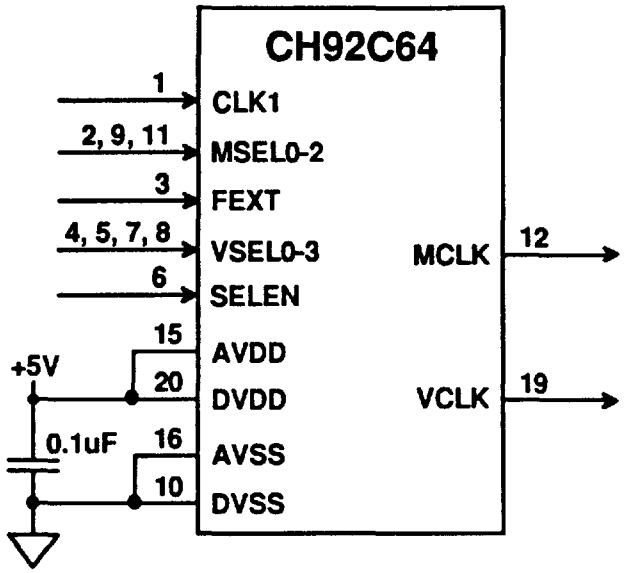
Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated under the Normal Operating Conditions sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Specifications (V_{DD} = +5V ± 5%)

Symbol	Description	Test Condition @T_A=25°C	Min	Typ	Max	Unit
V_{IL}	Input low voltage		Vss		0.8	V
V_{IH}	Input high voltage		2.0		V_{DD}	V
I_{IH}	Input leakage current	V_{IN} = V_{DD}			20	µA
I_{PU}	Input pull-up current			5	20	µA
V_{OL}	Output low voltage	I_{OL}=8.0 mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=4.0 mA	V_{DD}−0.4			V
V_{OH}	Output high voltage	I_{OH}=8.0 mA	2.4			V
I_{DD}	Supply current	V_{CLK}=28MHz, M_{CLK}=40MHz, No load		38	45	mA
I_{DD}	Supply current	V_{CLK}=80MHz, M_{CLK}=40MHz, No load		46	53	mA
C_{IN}	Input pin capacitance	Fc = 1 MHz			8	pF
C_{OUT}	Output pin capacitance	Fc = 1 MHz			12	pF

AC Specifications (V_{DD} = +5V ± 5%), Output pin loading = 15 pF

Symbol	Description	Test Condition @T_A=25°C	Min	Typ	Max	Unit
F_{IN}	Reference frequency input			14.318		MHz
T_{SU}	Setup time, data to strobe		20			ns
T_{HOLD}	Hold time, strobe to data		10			ns
T_{STROBE}	Strobe pulse width		20			ns
T_{DELAY}	Prop delay from F_{EXT} to V_{CLK}				20	ns
T_{JITTER}	Long term output phase jitter	10,000 cycles, 1 σ		300	800	ps
V_{CLK}	Video clock frequency		8		80	MHz
M_{CLK}	Memory clock frequency		8		80	MHz
T_R, T_F	F_{IN} rise/fall time	Duty Cycle : 42.5% to 57.5%			10	ns
T_R, T_F	V_{CLK} & M_{CLK} rise/fall time	0.8V – 2.0V		1.0	1.4	ns
T_R, T_F	V_{CLK} & M_{CLK} rise/fall time	0.3V_{DD} – 0.7V_{DD}		1.6	2.5	ns
T_{DC}	Output clock duty cycle	@1.4V Switch point	50		60	%
T_{DC}	Output clock duty cycle	@V_{DD}/2 Switch point	45		55	%



CH92C64 APPLICATION SCHEMATIC

ORDERING INFORMATION	
Part Number	Package Type
CH92C64-N	300 mil PDIP
CH92C64-S	300 mil SOIC

For the location of the sales office nearest you, contact:

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