CIRRUS LOGIC

CL-SH366

Data Sheet

FEATURES

Microcontroller Interface

- Supports high-speed processors (e.g., 16-MHz 8051, 16-MHz 68HC11)
- Supports multiplexed/non-multiplexed address and data bus
- Supports interrupt- or polled-processor interface
- Provides microcontroller access to five external switch settings
- Three-level power-down capability when idle, automatic power-up when command is received
- Supports host- and disk-interrupt pins

Formatter Interface

- Supports 1-bit NRZ interface disk data rates up to 40 Mbits/sec. — 64 Mbits/sec. for 2-bit NRZ
- Works with all disk encoding schemes
- Disk interfaces supported include ST506/412, ESDI and SMD
- Supports non-interleaved operations
- User-modifiable RAM-based disk formatter control store (31 x 4 bytes)
- Multiple WCS branch and WCS data field branch capability
- Variable split data field support for constant-density-recording formats
- Full-track multi-sector transfer capability with no microcontroller intervention
- Scheduled WCS access

(cont. next page)

High-Performance PC XT/AT Disk Controller

OVERVIEW

The CL-SH366 is a VLSI component that provides the majority of the hardware necessary to build a PC Winchester disk controller. It is typically configured with buffer memory and a microcontroller — with system RAM and ROM — to create a complete intelligent PC Winchester disk controller. The device combines an advanced Winchester disk formatter, a dual-port buffer memory manager, and extensive hardware support, including direct bus connection with 24-mA drivers. Electrical noise is reduced on the IDE cable by staggered driver turn-on times.

A static RAM buffer (up to 128K bytes of SRAM) or a dynamic RAM buffer (up to 4 Mbytes of DRAM) is controlled by the CL-SH366. It supports disk data rates up to 40 Mbits/second in single-bit NRZ Mode. For high-performance applications, a 2-bit NRZ interface option is available, supporting disk data rates up to 64 Mbits/second.

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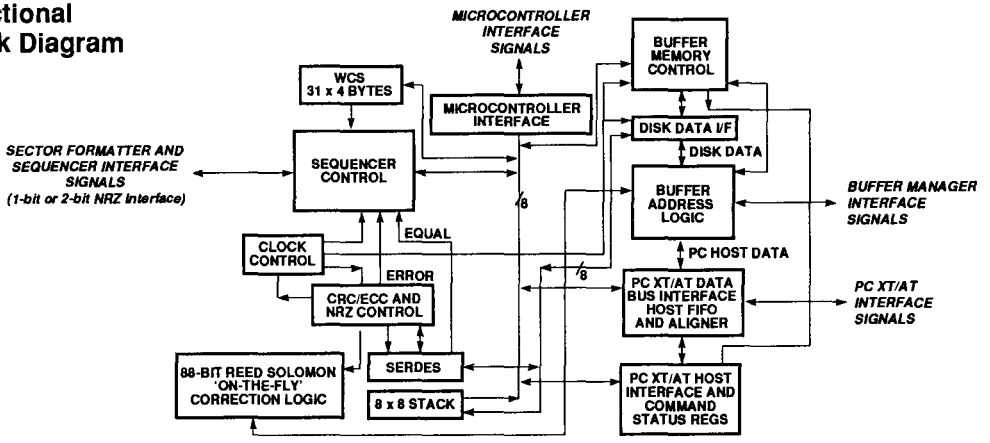
Functional Block Diagram



FEATURES (cont.)

Formatter Interface (cont.)

- User-programmable sector length up to a full track
- 16-bit CRC and 88-bit ECC polynomial with 'on-the-fly' hardware correction circuitry
- Flexible sector-level defect handling
- Buffer-derived ID field during format
- Two index timeout circuit for sector searches
- Programmable read synchronization timeout

Buffer Manager

- Dual-port circular buffer control with access priority resolver
- Direct-buffer addressing of up to 128K bytes of static RAM
- Direct-buffer addressing of up to 4 Mbytes of dynamic RAM
- Supports TMS48C128-TI 128K x 8 DRAM
- Supports Buffer Parity Bit in DRAM Mode
- Optimized buffer memory timing for highest throughput
- Fixed and variable buffer segmentation support
- Scheduled microcontroller write/read to/from buffer
- Supports internal division of buffer clock by one, two, three and four for ease of implementation
- Supports buffer memory throughput to 12 Mbytes/second
- Provides host overrun control
- Dual-buffer-chip enables to support two 32K x 8 SRAM buffers

PC XT/AT and Other Compatible Interfaces

- Supports 8- as well as 16-bit host bus transfer
- True real-time hardware and software compatibility with PC XT/AT and other compatible computers
- Programmable polarity for host reset and interrupt lines for electrical compatibility with the PCMCIA-ATA extension
- Direct bus interface logic with on-chip 24-mA staggered turn-on time drivers
- Supports any host speed with programmable and auto-wait-state generation
- PC XT/AT DMA handshake logic handles transfer to/from buffer memory at rates up to 4 Mwords/second
- Demand Mode DMA handshake logic (EISA Type 'B')
- Buffer data transfer supported under DMA or programmed I/O for both PC XT and PC AT
- FIFOs provided to synchronize buffer RAM access with the PC bus and formatter
- Emulates the IBM® task file for PC AT and IBM command descriptor block for PC XT
- Provides logic to speed-up command response
- Provides logic for daisy-chaining two XT- or AT-embedded drives
- Support of AT Master/Slave DASP* and PDIAG* Signals
- Separate status for bus reset and host program reset

Technology

- 100-pin PQFP and VQFP packages
- Advanced, low-power, double-metal CMOS technology

OVERVIEW (cont.)

At the same time, the Buffer Manager provides the handshake for PC-bus-programmed I/O or DMA data transfer at rates up to 4 Mwords/second.

The CL-SH366 Disk Formatter consists of a serializer/deserializer, a flexible RAM-based Sequencer, 16-bit CRC polynomial and an 88-bit Reed-Solomon ECC generator with on-the-fly hardware correction capability. The Formatter also supports variable split data fields for constant density recording formats.

The CL-SH366 is designed to work with a local processor. It has multiplexed or non-multiplexed address and data bus compatible to that provided by the Intel® 8051 and Motorola® 68HC11 family of controllers. The local processor interface also supports separate host and disk interrupt pins.

The CL-SH366 has a highly sophisticated power management capability. It supports three levels of power-down when idle, in full support of the ATA Specification. The extremely low power requirements of the CL-SH366 make it an ideal choice for laptop or other power-sensitive applications.

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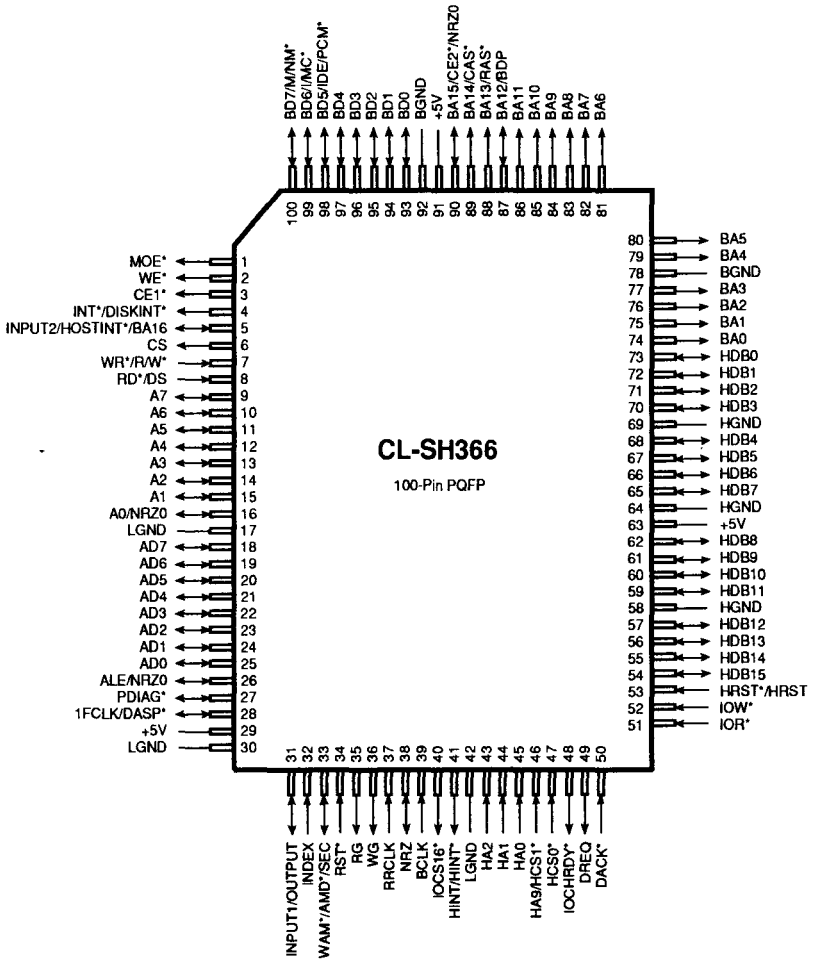
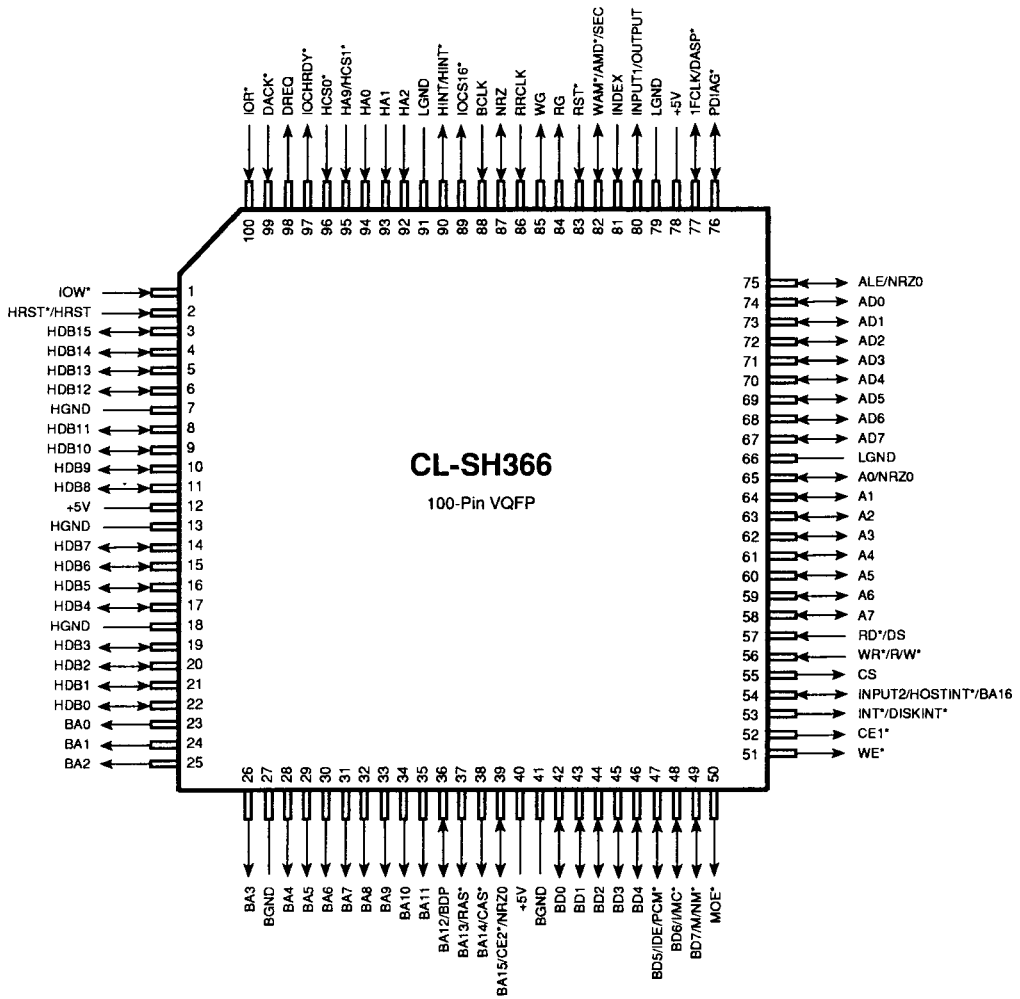
1. PIN INFORMATION

1.1 Pin Diagram for the 100-Pin Plastic Quad Flat Pack (PQFP)



1.2 Pin Diagram for the 100-Pin Very Low Profile Quad Flat Pack (VQFP)



2. PIN ASSIGNMENTS

The following conventions are used in the pin assignment table: (I) indicates an input; (O) indicates an output; (I/O) indicates an input/output; (OD) indicates an open-drain output; (Z) indicates a tri-state output or an input/output; (*) denotes a negative-true (active-low) signal.

2.1 100-Pin PQFP and VQFP Pin Assignments

NOTE: Unless otherwise specified, *all* references to pin locations include PQFP/VQFP pin numbers.

Symbol	PQFP No.	VQFP No.	Type	Description
BA15/CE2*/ NRZ0	90	39	I/O	**BUFFER ADDRESS LINE 15/BUFFER CHIP ENABLE 2/ NRZ0:** This signal can function as Buffer Address 15 or a second chip enable to control a second 32K SRAM buffer chip. It can also function as the second NRZ Bit if the 2-bit NRZ Mode is selected. This configuration is controlled by the NRZ0 Select Bit and the NRZ Interface Select Bit, (Shadow Register S71H, Bits 4 and 3).
BA14/CAS*	89	38	O	**BUFFER ADDRESS LINE14/COLUMN ADDRESS STROBE:** When the CL-SH366 is configured to operate with SRAM, this signal is Buffer Address 14. In DRAM Mode, this signal is the Column Address Strobe for the DRAM.
BA13/RAS*	88	37	O	**BUFFER ADDRESS LINE 13/ROW ADDRESS STROBE:** When the CL-SH366 is configured to operate with SRAM, this signal is Buffer Address 13. In DRAM Mode, this signal is the Row Address Strobe for the DRAM.
BA12/BDP	87	36	I/O	**BUFFER ADDRESS LINE 12/BUFFER DATA PARITY:** When the CL-SH366 is configured to operate with SRAM, this signal is Buffer Address 12. In DRAM Mode, this signal is the Buffer Data Parity Bit.
BA[11:0]	86-79 77-74	35-28 26-23	O	**BUFFER ADDRESS LINES:** Bits 11-0 are for addressing the buffer memory.
BD7/M/NM*	100	49	I/O	**BUFFER DATA BUS/MULTIPLEXED/NON-MULTIPLEXED ADDRESS CONFIGURATION:** This is Bit 7 of the 8-bit buffer data bus. The CL-SH366 is initialized to Multiplexed Mode if this input is connected to an external pull-up resistor (~20K ohm) after deassertion of the RST* Signal (Pin 34/83). Otherwise, it is configured in Non-multiplexed Mode.
BD6/I/MC*	99	48	I/O	**BUFFER DATA BUS/ INTEL/MOTOROLA:** This is Bit 6 of the 8-bit buffer data bus. The CL-SH366 is initialized to Motorola Mode if this input is connected to an external pull-down resistor (~20K ohm) after deassertion of the RST* Signal (Pin 34/83). Otherwise, it is configured in Intel Mode.

2.1 100-Pin PQFP and VQFP Pin Assignments *(cont.)*

Symbol	PQFP No.	VQFP No.	Type	Description
BD5/IDE/ PCMCIA*	98	47	I/O	**BUFFER DATA BUS/IDE/PCMCIA CONFIGURATION:** This is Bit 5 of the 8-bit buffer data bus. The CL-SH366 is initialized for PCMCIA electrical compatibility if this pin is connected to an external pull-down resistor (~20K ohm) after the deassertion of the RST* Signal (Pin 34/83). Otherwise, it is configured to operate in the standard IDE Mode. The firmware can override this selection by writing to Bit 0 in the IDE/PCMCIA Control Register (Register 6FH).
BD[4:0]	97-93	46-42	I/O	**BUFFER DATA BUS:** These five signals are Bits 4-0 of the 8-bit buffer data bus.
MOE*	1	50	O	**MEMORY OUTPUT ENABLE:** This signal is asserted when a RAM Buffer Operation is active. It is recommended that MOE* be connected to the RAM Output Enable for high-speed operation.
WE*	2	51	O	**WRITE ENABLE:** This signal is asserted when a buffer memory Write Operation is active.
CE1*	3	52	O	**BUFFER CHIP ENABLE 1:** This signal is the control signal for the full-buffer chip enable or the first 32K chip enable.
INT*/ DISKINT*	4	53	O,OD	**INTERRUPT/DISK INTERRUPT:** This is the microcontroller Interrupt*/Disk Interrupt* Pin, programmable for either push-pull or open-drain output circuitry. This pin contains an internal pull-up resistor. The INT*/DISKINT* pull-up can be disabled if the Interrupt Enable Bit (Register 77H, Bit 3) is set, and the Interrupt Pin Pull-up Disable Bit (Register 77H, Bit 4) is set.
INPUT2/ HOSTINT*/ BA16	5	54	I/O,OD	**INPUT2/HOST INTERRUPT/BA16:** When the CL-SH366 is in SRAM Mode and a 128K buffer is used, this pin functions as BA16. Otherwise, it can be configured as the microcontroller Host Interrupt Pin, programmable for either push-pull or open-drain output circuitry. This pin can also be used as an edge-sensitivity second input to the sequencer, and it contains an internal pull-up resistor that can be disabled by setting Bit 4 in Register 4FH.
CS	6	55	I	**CHIP SELECT:** This signal must be asserted to access the CL-SH366 registers.

2.1 100-Pin PQFP and VQFP Pin Assignments *(cont.)*

Symbol	PQFP No.	VQFP No.	Type	Description
WR*/R/W*	7	56	I	**WRITE STROBE/READ/WRITE:** When the Intel bus control interface is selected (the ***I/MC**** Signal — Pin 99/48 is asserted), this acts as the WR* Signal. When the Write Strobe Signal is asserted and the CS Signal (Pin 6/55) is asserted, the data on the AD lines will be written to the specified register. When the Motorola bus control interface is selected (the ***I/MC**** Signal (Pin 99/48) is deasserted), this signal acts as the R/W* Signal. A high on this input, along with the RD*/DS Signal (Pin 8/57) asserted and the CS Signal (Pin 6/55) asserted, it indicates a Read Operation. A low on this input, along with the RD*/DS Signal (Pin 8/57) asserted and CS Signal (Pin 6/55) asserted, indicates a Write Operation.
RD*/DS	8	57	I	**READ STROBE/DATA STROBE:** When the Intel bus control interface is selected (the ***I/MC**** Signal — Pin 99/48 is asserted), this signal acts as the RD* Signal. When the Read Strobe Signal is asserted and the CS Signal (Pin 6/55) is asserted, the data from the specified register will be driven onto the AD lines. When the Motorola bus control interface is selected (the ***I/MC**** Signal — Pin 99/48 is deasserted), this signal acts as the Data Strobe Signal. A high on this input, along with the WR*/R/W* Signal (Pin 7/56) asserted and the CS Signal (Pin 6/55) asserted, indicates a Read Operation. A high on this input, along with the WR*/R/W* (Pin 7/56) deasserted and the CS Signal (Pin 6/55) asserted, indicates a Write Operation.
A[7:1]	9-15	58-64	I/O	**LOCAL MICROCONTROLLER ADDRESS BUS:** These are non-multiplexed address input or demultiplexed address output lines.
A0/NRZ0	16	65	I/O	**LOCAL MICROCONTROLLER ADDRESS BUS/NRZ0:** If the CL-SH366 is configured in Non-multiplexed Mode, this pin functions as the Address 0 Input from the local microcontroller. In Multiplexed Mode, this signal defaults to a demultiplexed Address 0 Output, but it can be reconfigured as NRZ0 in 2-bit NRZ Mode.
AD[7:0]	18-25	67-74	I/O	**LOCAL MICROCONTROLLER ADDRESS/DATA:** These are tri-state address/data lines that interface with a multiplexed microcontroller address/data bus.

2.1 100-Pin PQFP and VQFP Pin Assignments *(cont.)*

Symbol	PQFP No.	VQFP No.	Type	Description
ALE/NRZ0	26	75	I/O	**ADDRESS LATCH ENABLE/NRZ0:** In Multiplexed Mode, this signal will latch the address from the AD bus; A[7:0] are the latched address outputs. When Non-multiplexed Mode is selected and the CL-SH366 is placed in the 2-bit NRZ Mode, this pin functions as NRZ0. In this mode, A[7:0] function as address inputs.
PDIAG*	27	76	I/O	**PASS DIAGNOSTICS:** This signal is used between two embedded AT drives for communicating drive diagnostic results. This pin contains an internal pull-up resistor that can be disabled by setting Bit 4 in Register 4FH.
1FCLK/DASP*	28	77	I/O	**1FCLK/SLAVE PRESENT:** The 1FCLK can be used for the ECC corrector circuit. For embedded AT drives, this pin can also function as the Slave Present Signal. This pin contains an internal pull-up resistor which can be disabled by setting Bit 4 in Register 4FH.
INPUT1/ OUTPUT	31	80	I/O	**INPUT1/OUTPUT:** The state of this pin is sampled by reading Register 7DH, Bit 2. It is also a branch input to the sequencer RAM. When the pin is programmed to be an output, it is controlled by Bit 2 of the Control Field (A0H-BEH) of the Sequencer WCS RAM. This pin contains an internal pull-up resistor. The resistor is disabled when the pin is configured as an output.
INDEX	32	81	I	**INDEX:** This is an input for the index pulse received from the drive.
WAM*/ AMD*/ SECTOR	33	82	I/O	**WRITE ADDRESS MARK/ADDRESS MARK DETECT/ SECTOR:** This signal can be configured to operate in Hard or Soft Sector Mode by initializing the Hard/Soft* Sector Mode Control Bit of the Formatter Mode Selection Register (Register 77H, Bit 7). The default is Soft Sector Mode. In Soft Sector Mode, when the RG Signal (Pin 35/84) is asserted, a low-level input on this signal indicates Address Mark detected. Also, in Soft Sector Mode, a 1-bit wide pulse is an output when WG (Pin 36/85) is active and an address mark is to be written. In Hard Sector Mode, this is the input for the sector pulse.

2.1 100-Pin PQFP and VQFP Pin Assignments *(cont.)*

Symbol	PQFP No.	VQFP No.	Type	Description
RST*	34	83	I	**RESET:** When this signal is asserted, it stops all operations within the chip and deasserts the RG Signal (Pin 35/84), the WG Signal (Pin 36/85), and the NRZ Signal (Pin 38/87). All I/O signals and host outputs are set to a high-impedance state. See Section 3.6, *Register Initialization.*
RG	35	84	O	**READ GATE:** This signal is asserted when the CL-SH366 is reading NRZ data from the storage device.
WG	36	85	O	**WRITE GATE:** This signal is asserted when the CL-SH366 is writing NRZ data to the storage device.
RRCLK	37	86	I	**READ REFERENCE CLOCK:** This is a multiplexed input sourced from the VFO oscillator during a Read Gate; otherwise, it is from the write oscillator. This is the primary clock for the Formatter section and must be present at all times, including during a Reset Operation.
NRZ	38	87	I/O	**NRZ:** This is a Read Data Input from the disk when the RG Signal (Pin 35/84) is active; this is a Write Data Output to the disk when the WG Signal (Pin 36/85) is active.
BCLK	39	88	I	**BUFFER CLOCK:** This is a clock input that is used to generate buffer memory access cycles.
IOCS16*	40	89	OD	**16-BIT DATA TRANSFER:** This signal indicates that a 16-bit data transfer is active on the PC bus.
HINT/HINT*	41	90	O,Z	**HOST INTERRUPT:** This signal, when enabled, sends an interrupt to the PC host. For PCMCIA electrical compatibility, this signal can be configured as active-low. The polarity of this signal can be chosen at power-up by the state of the BD5/IDE/PCMCIA Signal (Pin 98/47), or the firmware can select the output polarity by writing to Bit 0 in the IDE/PCMCIA Control Register (Register 6FH).
HA[2:0]	43-45	92-94	I	**PC BUS ADDRESS LINES:** The address lines HA[9,2:0] address the various AT/XT Control, Status, and Data Registers. Only the HA[1:0] lines are used for PC XT operation.

2.1 100-Pin PQFP and VQFP Pin Assignments *(cont.)*

Symbol	PQFP No.	VQFP No.	Type	Description
HA9/HCS1*	46	95	I	**PC ADDRESS LINE 9 or CHIP SELECT 1:** This is a Multiplexed Input Signal. When the HCS1 Mode Enable Bit (Register 52H, Bit 3) is reset, this input is PC Address Line 9; when the bit is set, the input is Host Chip Select 1. When this signal is configured as HCS1*, this input is ignored when the DACK* Signal (Pin 50/99) is asserted. This pin contains an internal pull-up resistor that can be disabled by setting Bit 4 in Register 4FH.
HCS0*	47	96	I	**CHIP SELECT 0:** When this signal is asserted, this input selects access to the Control, Status and Data Registers. This input is ignored during DMA data transfers, i.e., when the DACK* Signal (Pin 50/99) is asserted. This pin contains an internal pull-up resistor. It can be disabled by setting Bit 4 in Register 4FH.
IOCHRDY*	48	97	O	**I/O CHANNEL READY:** This signal is asserted to extend host transfer cycles when the controller is not ready to respond.
DREQ	49	98	O,Z	**DMA REQUEST:** The DMA Request Signal is used during DMA transfer between the host and controller. This signal is issued by the controller to start a DMA transfer.
DACK*	50	99	I	**DMA ACKNOWLEDGE**: The DMA Acknowledge Signal is used during DMA to complete the DMA handshake for data transfer between the host and the CL-SH366. The signal is active for each transfer on the host bus. This pin contains an internal pull-up resistor.
IOR*	51	100	I	**I/O READ STROBE**: This signal is asserted by the host during a Host Read Operation. When this signal is asserted with the HCS0*/HCS1* or the DACK* Signal, it enables status or data onto the host data bus.
IOW*	52	1	I	**I/O WRITE STROBE**: This signal is asserted by the host during a Host Write Operation. When this signal is asserted with the HCS0*/HCS1* or the DACK* Signal, data from the host data bus is strobed into the CL-SH366.

2.1 100-Pin PQFP and VQFP Pin Assignments *(cont.)*

Symbol	PQFP No.	VQFP No.	Type	Description
HRST*/HRST	53	2	I	**HOST RESET**: When this signal is asserted, it initializes the Control/Status Registers and stops any command in process. See Section 3.6, *Register Initialization*. This pin contains an internal pull-up resistor. For PCMCIA electrical compatibility, this signal can be configured as active-high. The polarity of this signal can be chosen at power-up by the state of the BD5/IDE/PCMCIA Signal (Pin 98/47), or the firmware can select the output polarity by writing to Bit 0 in the IDE/PCMCIA Control Register (Register 6FH).
HDB[15:0]	54-57, 59-62, 65-68 70-73	3-6, 8-11 14-17 19-22	I/O,Z	**HOST DATA BUS**: During PC AT operations, HDB[15:8] are used in conjunction with HDB[7:0] for word transfers between the sector buffer and the host; Bits HDB[7:0] are used for control status and ECC byte access. During PC XT operation, only HDB[7:0] lines are used; the HDB[15:8] lines are tri-stated.
HGND	58, 64, 69	7, 13 18		**HOST GROUND.**
BGND	78, 92	27, 41		**BUFFER BUS GROUND.**
LGND	17, 30, 42	66, 79 91		**LOGIC GROUND.**
+5V	29, 63, 91	12, 40 78		**POWER SUPPLY** (+5)

3. REGISTER TABLES

3.1 Buffer Manager Registers

Address	Type*	Description/Function
9FH, BFH, 30H/B0H 31H/B1H, 32H/B2H	R/W	Buffer Start Address
DFH/FFH, 34H/B4H 35H/B5H, 36H/B6H	R/W	Buffer End Address
68H	R/W	Scheduled Microcontroller Buffer Data Access
53H	R/W	Buffer Transfer Control
S53H	R/W	Buffer Mode Control
54H	R/W	Buffer Size/Segment Address
59H	R/W	Buffer/PC Reset Register
5AH-5BH, 20H/A0H 21H/A1H, 22H/A2H	R/W	Disk Address Pointer
5CH-5DH, 24H/A4H 25H/A5H, 26H/A6H	R/W	Host Address Pointer
5EH-5FH, 28H/A8H 29H/A9H, 2A/AAH	R/W	PC Stop Pointer
2C/ACH, 2D/ADH	R/W	Auto-Write Host Address Pointer
27H/A7H	R/W	Buffer DRAM Control/Parity Error Status
2BH/ABH	R/W	Buffer DRAM Timing Control
2F/AFH	R/W	DRAM Refresh Period Register
70H	R/W	Microcontroller Buffer Access
73H	W	Auto-Command 'Lock' Release: A write to this register unlocks the Buffer Manager Registers that were locked when the host issued an Auto-Command, i.e., Registers 53H, 5C-5FH, 68H and 70H. If the firmware has used the Local Microcontroller Power-Down Bit (Register 4FH, Bit 5), it will also be unlocked.

NOTE: Register types are as follows: R/W = Read/Write; R = Read Only; W = Write Only.

3.2 PC Interface Registers

Address	Type	Description/Function
40H-47H, 60H-67H	R/W	PC Interface Register File: These registers are for communication between the host PC and the local processor.
55H-57H	R/W	PC Interface Registers
50H	R/W	PC Interrupt Status Register
51H	R/W	PC Interrupt Enable Register
52H	R/W	Miscellaneous Control/Status Register
58H	R/W	PC Mode Control Register
6FH	R	Revision Register
6FH	W	IDE/PCMCIA Control Register

3.3 Formatter Registers

Address	Type	Description/Function
4DH	R	Data Latch Register (for read accesses of the data buffer through Registers 68H and 70H)
4EH	R/W	Sector Size Register (for larger than 512-byte data fields)
69H	R	Sector Status Register
69H	W	Increment Sector Count Register
6AH	R/W	Sector Target Register
6BH	R/W	Sector Count Register
6CH	R/W	React Branch Register
6DH	R/W	MSB Sector Remaining Counter
6EH	R/W	LSB Sector Remaining Counter
6FH	R	Revision Register
71H	R/W	Control Register for ECC: Bit 5 — which can be set from the RST* Pin or the microcontroller — is the Formatter reset. When set, a constant reset will be asserted that stops all operations within the Formatter and drops RG, WG, WAM and NRZ Outputs. This reset also clears the interrupt enables.
S71H	R/W	Shadow ECC Control Register

3.3 Formatter Registers *(cont.)*

Address	Type	Description/Function
72H	R	ECC Syndrome Shift Register
72H	W	Correction Done Reset
74H	R/W	ECC Offset Correction Count (MSB)
75H	R/W	ECC Offset Correction Count (LSB)
76H	R/W	Synchronization Byte-Count Limit
77H	R/W	Formatter Mode Selection
78H	W	Branch Address Register
79H	R	Formatter Status Register
79H	W	Sequencer Start Address Register
7AH	R/W	Operation Control/Status Register
7BH	R/W	WAM Output Timing Control Register
7CH	R/W	Address Mark Detect Control Register (to be compared with NRZ read data): The number of bits to be compared is controlled by Register 7FH.
7DH	R/W	Formatter Interrupt Status Register
7EH	R/W	Formatter Interrupt Enable Register
7FH	R	Stack: When reading, contents of the top of stack are presented to the bus and the stack is rotated.
7FH	W	Clock Control and Sync Compare Register

3.4 Control Registers

Address	Type	Description/Function
48H	R/W	Auxiliary Control Register 0 for mode selection of Formatter and buffer options.
4FH	R/W	Auxiliary Control Register 1 for mode selection of Formatter and local microcontroller interface options.

3.5 Sequencer Registers

Address	Type	Description/Function
80H-9EH	R/W	Next Address Field of the WCS Word: This is the address that the Sequencer will go to after the down-counter has reached zero, and a branch has not been taken.
A0H-BEH	R/W	Control Field of the WCS Word
C0H-DEH	R/W	Count Field of the WCS Word: This sets the initial value of the Sequencer counter when a new state is entered.
E0H-FEH	R/W	Data Field of the WCS Word: This is the source for all overhead bytes of data used by the device during Write Operations. During Read Operations, it is one of the operands to the comparison logic.
49H-4CH	R/W	This allows the microcontroller to access the Current Sequencer Word. There is no protection against access contention between the microcontroller and Sequencer. **These registers are for test purposes only.**

3.6 Register Initialization

3.6.1 Buffer Manager Register Initialization

Register Address	HRST*/HRST (Pin 53/2)	RST* (Pin 34/83)	Host Prog. Reset	REG 59H (Write)	REG 59H (Bit 0 = 1)	REG 71H (Bit 5 = 1)	REGISTER BIT VALUE 7 6 5 4 3 2 1 0	Notes
9FH		✓		✓	✓		0 0 0 0 0 0 0 0	
BFH		✓		✓	✓		0 0 0 0 0 0 0 0	
30H/B0H		✓		✓	✓		0 0 0 0 0 0 0 0	
31H/B1H		✓		✓	✓		0 0 0 0 0 0 0 0	
32H/B2H		✓		✓	✓		0 0 0 0 0 0 0 0	
DFH/FFH		✓			✓		1 1 1 1 1 1 1 1	
33H/B3H							X X X X X X X X	
34H/B4H		✓		✓	✓		X X 1 1 1 1 1 1	
35H/B5H		✓		✓	✓		1 1 1 1 1 1 1 1	
36H/B6H		✓		✓	✓		1 1 1 1 1 1 1 1	
68H		✓		✓	✓		0 0 0 0 0 0 0 0	
48H		✓					0 0 0 0 0 0 0 0	1
53H		✓					0 0 0 0 0 0 0 0	1
S53H		✓					0 0 0 0 0 0 1 1	1
54H		✓					1 1 1 1 1 1 1 1	
59H		✓					X X X X X X X 1	
5AH		✓		✓	✓		0 0 0 0 0 0 0 0	
5BH		✓		✓	✓		0 0 0 0 0 0 0 0	
20H/A0H		✓		✓	✓		0 0 0 0 0 0 0 0	
21H/A1H		✓		✓	✓		0 0 0 0 0 0 0 0	
22H/A2H		✓		✓	✓		0 0 0 0 0 0 0 0	
5CH		✓		✓	✓		0 0 0 0 0 0 0 0	2
5DH		✓		✓	✓		0 0 0 0 0 0 0 0	2
24H/A4H		✓		✓	✓		0 0 0 0 0 0 0 0	
25H/A5H		✓		✓	✓		0 0 0 0 0 0 0 0	
26H/A6H		✓		✓	✓		0 0 0 0 0 0 0 0	
5EH		✓		✓	✓		0 0 0 0 0 0 0 1	3
5FH		✓		✓	✓		1 1 1 1 1 1 1 1	3
28H/A8H		✓		✓	✓		X X 0 0 0 0 0 0	
29H/A9H		✓		✓	✓		0 0 0 0 0 0 0 1	
2A/AAH		✓		✓	✓		1 1 1 1 1 1 1 1	
2C/ACH		✓		✓	✓		0 0 0 0 0 0 0 1	
2D/ADH		✓		✓	✓		0 0 0 0 0 0 0 1	
27/A7H		✓		✓	✓		0 0 0 0 0 0 0 1	
2BH/ABH		✓					0 0 0 0 0 0 0 1	
2FH/AFH		✓					0 0 0 0 0 0 0 1	
70H							X X X X X X X X	

3.6.2 PC Interface Register Initialization

Register Address	HRST*/HRST (Pin 53/2)	RST* (Pin 34/83)	Host Prog. Reset	REG 59H (Write)	REG 59H (Bit 0 = 1)	REG 71H (Bit 5 = 1)	REGISTER BIT VALUE 7 6 5 4 3 2 1 0	Notes
40H-45H							X X X X X X X X	
46H	✓	✓	✓				0 0 0 0 0 0 0 0	
47H							X X X X X X X X	
60H-65H							X X X X X X X X	
66H	✓	✓	✓				0 0 0 0 0 0 0 0	
67H							X X X X X X X X	
55H - XT Mode	✓	✓	✓				1 0 0 0 0 0 0 0	1
56H - XT Mode							X X X X X X X X	
57H - XT Mode	✓		✓				X X X X X 0 0 0	
55H - AT Mode	✓						1 0 0 0 0 0 0 0	1
56H - AT Mode		✓					X X X 0 0 0 0 0	
57H - AT Mode		✓					X X X 0 0 0 0 0	
50H		✓					X X X 0 0 0 0 0	
51H		✓					X 0 0 0 0 0 0 0	
52H		✓					0 0 0 0 0 0 0 0	1
58H		✓					0 1 0 1 1 0 0 0	
6FH (Read)							0 0 0 0 0 0 0 0	
6FH (Write)		✓					X X X X X X X X	4

NOTES: The following notes apply to Sections 3.6.1 and 3.6.2, *Buffer Manager Register Initialization* and *PC Interface Register Initialization.*

1) These tables only list reset conditions that are common to all bits in each register. For reset conditions of individual bits in these registers, see the detailed register descriptions in Section 5.

2) Registers 5CH and 5DH are also reset by an auto-command.

3) Registers 5EH and 5FH are also set to 01H and 0FFH, respectively, by an auto-command.

4) The state of Bit 0 will depend on how the BD5/IDE/PCMCIA Signal (Pin 98/47) is configured.

3.6.3 Formatter Register Initialization

Register Address	HRST*/HRST (Pin 53/2)	RST* (Pin 34/83)	Host Prog. Reset	REG 59H (Write)	REG 59H (Bit 0 = 1)	REG 71H (Bit 5 = 1)	REGISTER BIT VALUE 7	6	5	4	3	2	1	0	Notes
4DH		✓				✓	0	0	0	0	0	0	0	0	
4EH		✓					0	0	0	0	0	0	0	0	
69H (Read)		✓					0	0	0	0	0	0	0	0	
69H (Write)							X	X	X	X	X	X	X	X	
6AH		✓					0	0	0	0	0	0	0	0	
6BH		✓					0	0	0	0	0	0	0	0	
6CH		✓					X	X	X	0	0	0	0	0	
6DH		✓					X	X	X	X	0	0	0	0	
6EH		✓					0	0	0	0	0	0	0	0	
71H		✓				✓	0	0	1	0	0	0	0	0	1
S71H		✓					0	0	0	0	0	0	0	0	
72H (Read)		✓					0	0	0	0	0	0	0	0	
74H		✓				✓	X	X	0	0	0	0	0	0	
75H		✓				✓	0	0	0	0	0	0	0	0	
76H		✓					0	0	0	0	0	0	0	1	
77H		✓					0	0	0	0	0	0	0	0	
78H (Read)		✓				✓	X	X	X	0	0	0	0	0	
78H (Write)		✓					0	0	0	0	0	0	0	0	
79H (Read)		✓				✓	0	0	0	0	0	0	0	0	1
79H (Write)		✓					0	0	0	0	0	0	0	0	
7AH		✓				✓	0	0	0	0	0	0	0	0	
7BH		✓					0	0	0	0	0	0	0	0	
7CH		✓					0	0	0	0	0	0	0	0	
7DH		✓				✓	0	0	0	0	0	0	0	0	
7EH		✓					0	0	0	0	0	0	0	0	
7FH (Read)							X	X	X	X	X	X	X	X	
7FH (Write)		✓					0	0	0	0	1	0	0	0	

3.6.4 Control Register Initialization

Register Address	HRST*/HRST (Pin 53/2)	RST* (Pin 34/83)	Host Prog. Reset	REG 59H (Write)	REG 59H (Bit 0 = 1)	REG 71H (Bit 5 = 1)	REGISTER BIT VALUE 7 6 5 4 3 2 1 0	Notes
48H	✓	✓	✓				X X X 0 X X X X	
4FH		✓					0 0 0 0 0 0 0 0	

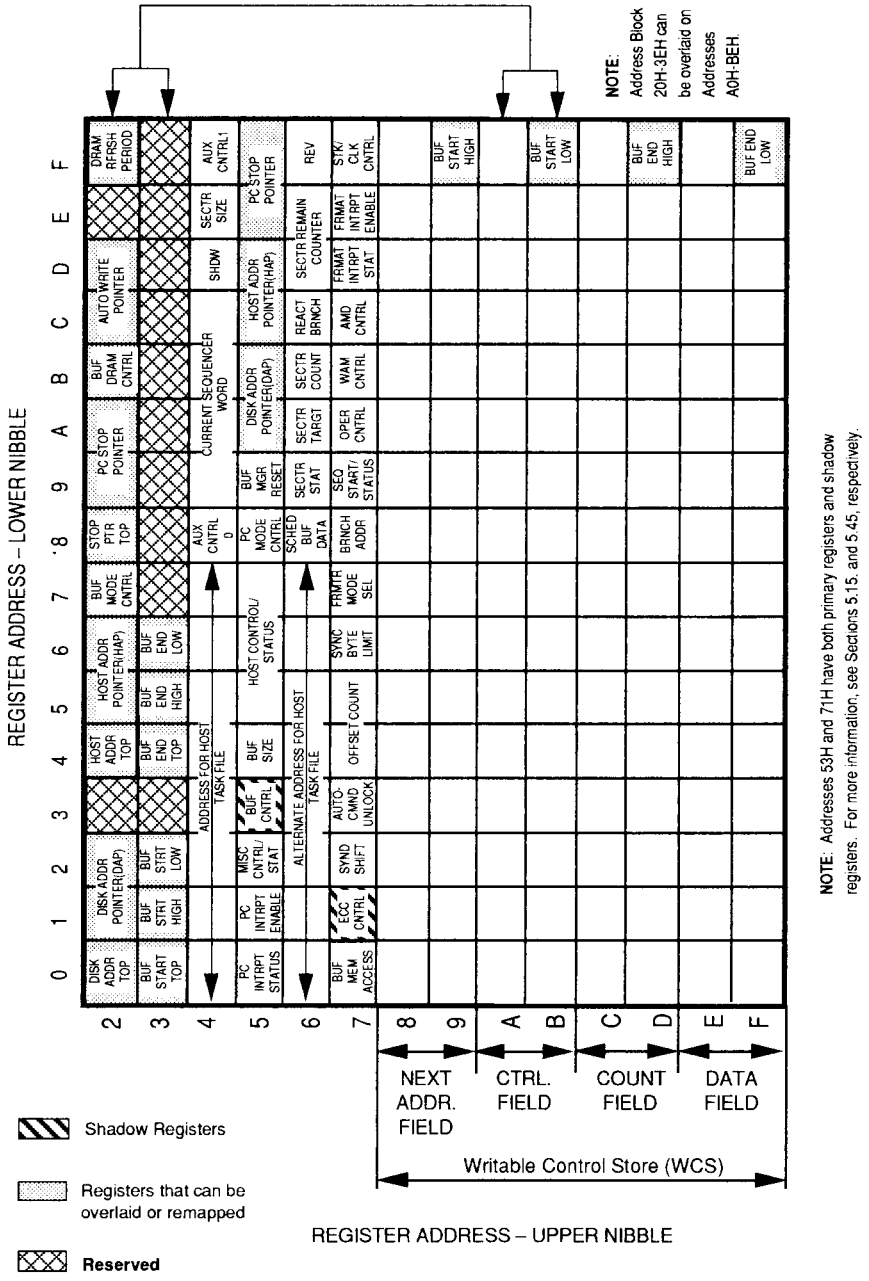
3.6.5 Sequencer Register Initialization

Register Address	HRST*/HRST (Pin 53/2)	RST* (Pin 34/83)	Host Prog. Reset	REG 59H (Write)	REG 59H (Bit 0 = 1)	REG 71H (Bit 5 = 1)	REGISTER BIT VALUE 7 6 5 4 3 2 1 0	Notes
80H-9EH							X X X X X X X X	
A0H-BEH							X X X X X X X X	
C0H-DEH							X X X X X X X X	
E0H-FEH							X X X X X X X X	
80H-9FH		✓			✓		0 0 0 0 0 0 0 0	
49H (Test only)		✓				✓	0 0 0 1 1 1 1 1	
4AH (Test only)		✓				✓	0 0 0 0 0 0 0 0	
4BH (Test only)		✓				✓	0 0 0 0 0 0 0 0	
4CH (Test only)		✓				✓	0 0 0 0 0 0 0 0	

NOTES: The following note applies to Sections 3.6.3, 3.6.4 and 3.6.5, *Formatter Register Initialization*, *Control Register Initialization*, and *Sequencer Register Initialization*.

1) These tables only list reset conditions that are common to all bits in each register. For reset conditions of individual bits in these registers, see the detailed register descriptions in Section 5.

3.7 Register Memory Map



4. FUNCTIONAL DESCRIPTION

The CL-SH366 is designed to be used with a low-cost microcontroller that allows it to maintain a 'loose' synchronization with the real-time disk operation. The CL-SH366 maintains 'close' synchronization with the data to and from the disk drive and provides the signals necessary to control this path. Using the CL-SH366 means a lower-total-part count for an intelligent disk drive design with the PC XT/AT interface.

The CL-SH366 has four functional blocks:

- **Microcontroller Interface**
- **Sector Formatter and Sequencer**
- **Buffer Manager Interface**
- **PC XT/AT Interface**

4.1 Microcontroller Interface

The microcontroller-to-CL-SH366 communication path is a multiplexed/non-multiplexed address and data bus similar to that provided by the Intel 8051- and the Motorola 68HC11-class of controllers. The CL-SH366 can use either the Intel or the Motorola method of data control. When the Intel interface is selected, the WR*/R/W* Signal (Pin 7/56) acts as a write strobe. In the case of a Write Operation, this write strobe provides the timing and control for the data transfers. Similarly, in the case of a Read Operation, the RD*/DS Signal (Pin 8/57) acts as a read strobe to provide the timing and control for the data transfers.

The BD6/I/MC* Signal (Pin 99/48) defaults to Intel Mode after reset, with no external resistor. An external pull-down resistor is required to operate in the Motorola Interface Mode. For the Motorola configuration, the WR*/R/W* Signal (Pin 7/56) is used only to determine the direction of the data transfer. When the input to this signal is high, a Read Operation is in progress; when it is low, a Write Operation is in progress. Data timing is derived with respect to the RD*/DS Signal (Pin 8/57). In the case of a Read Operation, the rising (leading) edge of the RD*/DS Signal (Pin 8/57) indicates when the CL-SH366 can start driving the data bus. In a Write Operation, the falling (trailing) edge is used by the CL-SH366 to latch the data from the microcontroller address/data bus.

The CL-SH366 uses the BD7/M/NM* Signal (Pin 100/49) after a reset to select a multiplexed or a non-multiplexed address and data path. The BD7/M/NM* Signal (Pin 100/49) has an internal pull-down. If this pin is connected to a pull-up resistor after reset, the CL-SH366 will recognize this condition and will automatically select Multiplexed Mode. Following reset, if the BD7/M/NM* Signal (Pin 100/49) is only connected to the Data Port of the buffer RAM without an external pull-up resistor, the CL-SH366 will recognize the low level (internal pull-down) on this signal and select Non-multiplexed Mode.

Table 4–1 provides the buffer data bus switch option settings in a tabular format.

Table 4–1. Buffer Data Bus Option Settings

Signal	Type of External Resistor	Mode with Resistor Present
BD7/M/NM*	Pull-up	Multiplexed Mode
BD6/I/MC*	Pull-down	Motorola Mode
BD5/IDE/PCMCIA*	Pull-down	PCMCIA-compatible Mode
BD4	Optional 'Switch'	User-defined
BD3	Optional 'Switch'	User-defined
BD2	Optional 'Switch'	User-defined
BD1	Optional 'Switch'	User-defined
BD0	Optional 'Switch'	User-defined

NOTE: BD4 through BD0 are general-purpose switches.

The CL-SH366 decodes addresses from 20H to FFH. To prevent erroneous operations, the controller design should reserve the decoding of Addresses 20H to FFH for the controller chip only. The registers at Addresses 20H-3EH can be overlaid onto Addresses A0H-BEH. If this is done, the controller design only needs to reserve Addresses from 40H to FFH for the controller chip. Some register addresses are mapped to two locations, a primary register and a shadow register. The shadow register can be accessed after setting the Shadow Register Select Bit in the Auxiliary Control Register (Register 48H, Bit 1). The CL-SH366 supports two shadow registers:

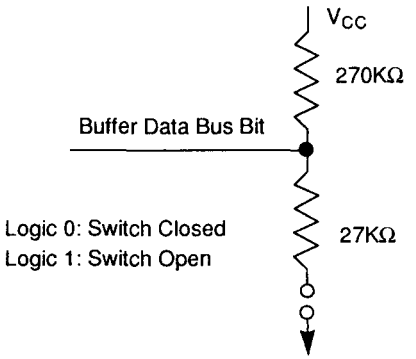
- Register S53H (Shadow 53H): Buffer Mode Control Register
- Register S71H (Shadow 71H): ECC Control Register

The PC Interface Register File is mapped to 40H-47H or 60H-67H. Upon a local reset (RST* — Pin 34/83), the access to the PC Register File is disabled until the Register File base address is programmed by the local microcontroller; this avoids contention on the read cycle, or errors on the write cycle.

The CL-SH366 has a programmable interrupt circuit. Four Interrupt Registers provide the status and mask programmability for interrupt sources. The programmable interrupt features include individual masks, a global enable, and an open-drain or push-pull output driver. The interrupt status registers may also be used as a focal point for microcontroller control when the CL-SH366 is being used in a Polled Mode. The interrupt sources are: PC Selection, PC Transfer Done, PC Reset, PC Transfer Overrun, Host Transfer Status Read Detected, Index Past, Sector Past, Disk Data Transfer Detected, ECC/Uncorrectable Error, Sequencer Stopped, Input Detected, and Sequencer Output Detected.

The processor-readable switches are multiplexed with the buffer data bus. These switches must be installed with relatively high-impedance pull-ups and pull-downs so that the resistor impedance does not affect the buffer performance. The processor accesses these switches by reading Registers 68H or 70H, with the MOE* Disable Bit set (Register 52H, Bit 0).

Switch Example



4.1.1 Access to External Buses

In addition to the normal data transfer operations, the CL-SH366 also supports microcontroller access to the buffer memory by addressing Registers 68H and 70H.

4.1.1.1 Microcontroller Scheduled Access to Buffer

A Register-68H decode is provided for the processor to gain scheduled access to the buffer. The address is generated based upon the contents of the Disk Address Pointer. The Disk Address Pointer will be incremented by a Register 68H access if the Buffer Pointer Auto-Increment Bit is set (Register 48H, Bit 0). The buffer read or write is scheduled by the Buffer Manager. This allows concurrent PC-and-local-microcontroller access to the buffer memory.

The processor-readable switches are also accessible by a Register-68H read. These switches must be installed as earlier described. (High-impedance pullups and pull-downs are recommended so buffer performance is not affected.)

4.1.1.2 Microcontroller Unscheduled Access to Buffer

A Register-70H decode is provided for the processor to gain access to the buffer when there is no PC disk transfer or ECC correction in progress. The processor-readable switches are also accessed by a Register 70H Read.

4.1.2 Power-Down Mode

The CL-SH366 can support three levels of firmware controlled Power-Down Operation. The level of power-down is selected by mode bits in Register 4FH. The appropriate mode is selected by the local microcontroller. The three levels of power-down in the CL-SH366 are summarized in the following table:

Register	Mode
4FH, Bit 5	Local Interface
4FH, Bit 6	Host ATA Power-Down
4FH, Bit 7	Host Deep Sleep Mode

The most power-saving level for the host interface is Host Deep Sleep Mode. In this mode, only the assertion of HRST*/HRST (Pin 53/2) or RST* (Pin 34/83) will activate the CL-SH366.

The next level of power-down is the Host ATA Mode. The CL-SH366 will exit this mode only when the host issues a soft reset by setting the RESET Bit (Bit 2) in the AT Fixed Disk Register (Host Register 3F6), the assertion of HRST*/HRST (Pin 53/2), or RST* (Pin 34/83).

The third level is the local interface. The CL-SH366 will recognize a write to the AT Command Register or the XT Controller Select Register, assertion of HRST*/HRST (Pin 53/2), RST* (Pin 34/83) or setting the Reset Bit in the AT Fixed Disk Register (Bit 2) and exiting this mode. When this mode is exited, the Assertion Bit (Register 4FH, Bit 5) will be 'locked' until the microcontroller has performed the 'unlock' write to Register 73H.

The highest level of power savings can be obtained by setting both the Local Interface Power-Down Bit (Register 4FH, Bit 5) and the Host Deep Sleep Power-Down Bit (Register 4FH, Bit 7). If the BCLK Input (Pin 39/88) is left running, power dissipation in this mode is estimated to be 7 mW. If the BCLK Input is grounded, power dissipation will drop to approximately 2 mW.

4.2 Sector Formatter and Sequencer

The basic operation of the Sector Formatter is controlled by the contents of the Sequencer Writable Control Store (WCS). A Sequencer program must be entered into the WCS before the CL-SH366 Sector Formatter can function properly. Under firmware control, the Sector Formatter can be made to sequence through different types of operations, such as: 'Read ID', 'Read ID and Read Data', 'Read ID and Write Data', and 'Write ID and Write Data'.

In order to accommodate the increased number of registers required by the CL-SH366, a section of the WCS address space can be shifted or 'overlaid' on another address block. The details of the overlay mapping are described in Section 5.15, *Register S53H: Buffer Mode Control.*

The Sequencer controls the timing relationships between the disk-interface output signals and monitors the disk-interface input lines to branch to different Sequencer locations. The track layout, such as gap lengths, sector size, and sector data fill character, can be flexibly defined in the WCS. The CL-SH366 Sector Formatter also has other registers that can be used to control the definition of the track format such as the SYNC character and the Address Mark.

The WCS consists of 124 bytes, organized as 31 words, each four bytes wide. The WCS can be broken down into Data/Branch, Count, Control, and Next Address Fields.

The Data/Branch Field contains data that may be used to initialize the track format, including gap, ID field, and sector-data-fill characters. This data can also be compared to the NRZ data-in to identify various fields in a sector or to execute sector data comparisons. The contents of this field may also be used as a branch address to tell the Sequencer which address to jump to upon the evaluation of a branch condition.

The Count Field specifies the number of counts during which the Sequencer will execute the current Sequencer Word. The initial value that is programmed into the Count Field must be one less than the desired count duration; e.g., if an operation in the WCS is meant to last for ten counts, program the Count Field with the number nine. The Sequencer counter is decremented once every eight Read/Reference Clock (RD/REF CLK)

cycles. When the count reaches zero, the Sequencer will go to the next address.

The next address will be based on the contents of the Next Address Field of the WCS word, unless a branch condition has been programmed and met during the last byte of the current WCS word.

The Control Field is used to generate and initiate all synchronous NRZ-data-handling operations.

The microcontrollers manipulation of the Sequencer revolves around the: Start/Status Register (Register 79H), Branch Register (Register 78H), WCS Data/Branch and the React Branch Register (Register 6CH). Writing to Register 79H loads the starting address where the Sequencer is to begin execution, and causes the four bytes at that WCS RAM word to be fetched and written into the Current Sequencer Word Registers. The next address to be fetched is based upon the contents of the Next Address Field in the Sequencer Registers, unless a specified branch condition is met. If the branch condition specified in the Next Address Field is met, the next address to be executed is based upon the contents of the Branch Address Register (Register 78H), the React Branch Register (Register 6CH), or the WCS Data Field. Thus, by setting up different branch conditions that are based on external or internal events, the chip can be made to sequence through different operations.

The serial data flow portion of the Sector Formatter consists of a 16-bit CRC, 88-bit ECC and a serializer/deserializer. Data to be written to the disk enters the CL-SH366 from the host in either a word, or a byte-wide format. The data is written into a byte-wide data buffer. When the data is ready to be written to the disk, it is read from the buffer, serialized, and processed through either a 16-bit CRC or an 88-bit ECC generator. An NRZ serial bit stream is then shifted out to the drive. Note that the NRZ-serial-bit stream will include serialized constants required for address marks, gaps, and ID fields, as well as the serialized data and ECC-generated output.

The CL-SH366 can operate with either a 1-bit or a 2-bit NRZ interface. In the standard 1-bit NRZ Mode, the maximum serial data rate is 40 Mbits/second. When operating in the 2-bit NRZ Mode, the maximum serial data rate is 64 Mbits/second.

The CL-SH366 will synchronize the NRZ data stream based on the sync-byte pattern chosen in the AMD Control Register (Register 7CH). When operating in 2-bit NRZ Mode, the CL-SH366 has circuitry to ensure that byte synchronization will occur whether the framing is on an odd- or an even-bit boundary.

The type of NRZ operation is controlled by Bit 3 in the ECC Control Register (Register S71H). If Register S71H, Bit 3 is reset, the single-bit NRZ interface is used. If Register S71H, Bit 3 is set, the 2-bit NRZ interface is selected. When the 2-bit NRZ Mode is selected (Register S71H, Bit 3 = 1), and the CL-SH366 is operating in Non-multiplexed Mode, the ALE/NRZ0 Signal (Pin 26/75) is configured as the NRZ0 Signal. If the CL-SH366 is operating in Multiplexed Mode, the location of the NRZ0 Signal is set by Bit 4 of Register S71H. If Register S71H, Bit 4 is reset, the Signal BA15/CE2*/NRZ0 (Pin 90/39) is configured as NRZ0. If Register S71H, Bit 4 is set, the Signal A0/NRZ0 (Pin 16/65) is configured as NRZ0.

The ECC can be programmed (in the WCS) for 16-bit CRC-CCITT for the ID field and an 88-bit Reed-Solomon polynomial for the data field. The 16-bit CRC-CCITT code can only be used for error detection. If an ECC error is detected after a Read Data Operation, the syndrome is saved in the internal correction registers and the ECC Error Bit (Register 79H, Bit 2) is set. The CL-SH366 has advanced correction logic that can determine the following conditions: If the error is correctable, calculate the error pattern and its displacement from the beginning of the data field, and correct the error in the buffer RAM. If the Hardware Correction Enable Bit (Register 71H, Bit 0) is set, hardware correction is performed while the next sector is being read. If the error is correctable, the hardware corrects the data and sets the Correction Done Bit (Register 79H, Bit 4). If the error is uncorrectable, the ECC Error and Uncorrectable ECC Error Bits (Register 79H, Bits 2 and 3) are set to prompt the local microcontroller to take appropriate action. If the Hardware Correction Enable Bit is reset, the ECC Error and Uncorrectable ECC Error Status Bits are set after the Read Data Operation, and the syndrome is transferred to the internal correction register. It is readable by the local microcontroller through Register 72H, and can be read in 8-bit increments for firmware-assisted correction.

The following is the 16-bit CRC-CCITT polynomial:

$$x^{16} + x^{12} + x^5 + 1$$

The 88-bit ECC Reed-Solomon code is a non-interleaved code of degree 8, operating on 10-bit symbols. The code is capable of correcting four 10-bit symbols that are in error. This gives the code the guaranteed ability to correct one 31-bit burst or two 11-bit bursts.

The on-the-fly hardware correction is set at 11 bits. This gives an on-the-fly detection capability of a 51-bit burst or three 11-bit bursts. It is recommended that software correction after retry be limited to a single 22-bit burst or two 11-bit bursts.

The probability of miscorrection for the on-the-fly circuitry is:

$$P_{mc} = \frac{n \times 2^{b1-1}}{2^m}$$

where,

n = sector length in bits, including redundancy bits

$b1$ = correction span in bits

m = total number of redundancy bits.

This provides the automatic on-the-fly hardware a miscorrection probability of approximately 10^{-20} per bit corrected for a 512-byte field (with a single-byte address mark).

The probability of miscorrection for the software correction algorithm is:

$$P_{mch} = \frac{1}{2^m} + \frac{n \times 2^{b2-1}}{2^m} + \frac{n \times (n-b3) \times (2^{b3-1})^2}{2^m}$$

where,

n = sector length in bits, including redundancy bits

$b2$ = single-burst correction span in bits

$b3$ = double-burst correction span in bits

m = total number of redundancy bits.

The CL-SH366 Sector Formatter also has a recirculating stack that is eight bytes deep. By enabling the stack (setting Bit 4 of the WCS Control Field) during a read process, information read from the drive can be pushed onto the stack to be examined later at a lower speed by the microcontroller. This capability can be used to pass the ID field to the microcontroller for defect management, seek verification and other disk controller tasks.

4.2.1 Extended-Data-Handling Operations

The CL-SH366 has the ability to flexibly handle a large variety of different sector configurations. The next four subsections discuss various sector sizes, split data fields, multiple-sector Read/Write Operations with minimal microcontroller intervention, and scheduled access to the WCS by the local microcontroller.

4.2.1.1 Variable Sector Size

The CL-SH366 Sector Formatter has an 8-bit data field length counter loadable from the Count Field of the Sequencer RAM. This field is programmable, and by setting this field to any value from 00H to FFH, a sector length up to 256 bytes can be written to the drive. The value of this counter is always one less than the actual sector length. For sector sizes greater than 256 bytes, several different methods can be used.

The simplest approach is to use as many Sequencer words as required to implement the count for the data field.

The next approach uses the Inhibit Carry Bit in the Operation Control Register (Register 7AH, Bit 7). By setting the Inhibit Carry Bit and programming the Next Address Field of the Formatter WCS with the most-significant bits set to 100 during data transfer, the CL-SH366 Sector Formatter will be inhibited from going to the Next Sequencer Word; another 256 bytes of data will be transferred. The 256-byte count number is programmed in the Sector Size Register (Register 4EH).

A value of zero (from a chip reset) will provide one suppression as described above, (i.e., for 532 bytes, start with the sector size set to one, and an initial count of 19).

4.2.1.2 Split Data Field Operation

For high-density drives, it is desirable to have more embedded servo fields on a track to keep the

head centered above the track. The Split Data Field Operation allows the data field of a sector to be split into multiple sections so that servo fields can be inserted. Split Data Field can also be used for flaw management. The programmability of the CL-SH366 Sequencer RAM provides flexible handling of split data fields.

There are two methods of handling data splits in the WCS. By resetting the Advance Multisector/ Multisector* Control Bit (Register 4FH, Bit 0), the Sequencer will use Bit 3 of the WCS Control Field as the Process Split/Flag Bit to control the split boundaries. Using this bit allows the transfer of data in full blocks or in split format from buffer to disk or disk to buffer. This method requires the microcontroller to update the WCS for every sector Read/Write Operation for proper data split handling.

The byte count of the split data field is specified by the count field of the Sequencer RAM. The servo-field sizes of split data fields are also specified by the Sequencer RAM Count Field.

The operation of freezing the ECC generation during a Write Operation or checking for a Split Data Field during a Read Operation is called Split/ Freeze ECC. Restarting the ECC circuitry for the remainder of the split data is called Restart ECC/ Continue Data Split.

To perform a Split/Freeze ECC Operation, the Process Split Bit of the WCS Data Control Field should be set in the last Data Transfer Sequencer Word. The CL-SH366 will recognize this operation; at the end of the data transfer count, it freezes the ECC generator and when the Data Transfer Bit of the Sequencer Control Field is set for the next split, it unfreezes the ECC generator and continues the transfer of data to/from the buffer. To further split the data, repeat the operation by setting the Process Split/Flag Bit of the WCS Data Control Field on the last Data Transfer Sequencer Word.

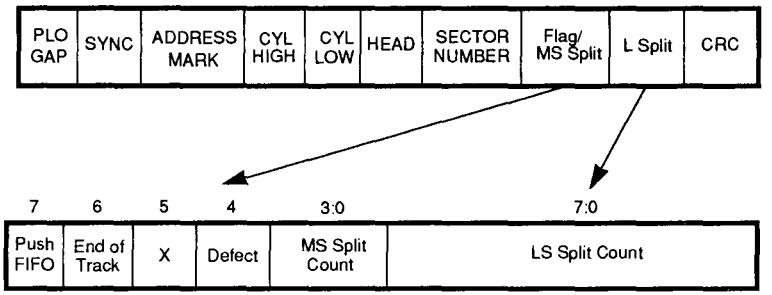
The second method is the Advanced Multisector Read/Write Operation where the splits are embedded in the ID field; by setting the proper flags, the split counts are processed by the Sequencer without the microcontroller having to intervene.

4.2.1.3 Multisector Read/Write Operation

The CL-SH366 supports Multisector Read or Write Operations with minimal microcontroller intervention. This can be accomplished by two methods. The simplest method is to load the next sector ID to be accessed while data transfer is active (Register 79H, Bit 7) for the present sector, and restarting the Read or Write Operation immediately after the end of the present sector.

The second approach uses the Sector Target ID Register and Sector Count Register to transfer multiple sectors to/from the buffer under WCS control. This method is selected by setting the Advanced Multisector/Multisector* Control Bit (Register 4FH, Bit 0). The CL-SH366 will use a number of internal registers to support advanced multisector transfers. These are: the Sector Remaining Register, the Sector Target Register and the Sector Count Register. The Sector Remaining Register controls the number of bytes per sector. This register is loaded by the microcontroller with the length, in bytes, of the data field. The Sector Target Register is loaded by the microcontroller with the starting sector number and the Sector Count Register is loaded with the number of sectors to be processed. Therefore, by proper programming of the WCS and the start address in the Sector Target Register and the number of sectors to be processed in the Sector Count Register, the Sequencer can perform Multisector Read/Write Operations with minimum real-time intervention by the microcontroller.

This method supports Constant Density Recording formats with variable data splits, and an alternate-/skipped-defective-sector scheme with minimal-latency sector operations. The data split counts for each sector are embedded in their ID field. Therefore, this allows the Sequencer to save these counts via an internal FIFO during the read of an ID and then use these values for proper handling of the data field with no intervention from the microcontroller. The split counts will be 12 bits in length for a maximum data split field length of 4K bytes. In addition, there are three flag bits for defect management and split-count designation. An example of the ID is illustrated in Figure 4–1 on the following page.



Flag/MS Split Count

Bit 7	**PUSH FIFO**: For Read and Write Operations, if this bit is set when the Advanced Multisector/Multisector* Control Bit (Register 4FH, Bit 0) is set, the Read Gate is asserted, and the Process Split/Flag Bit of the WCS Control Field is set, it pushes the contents of the Read ID Field Flag/MS Split Count value and the following byte LS Split Count value into the internal FIFO; these values are used for the actual split count of the data-field-format operations in the internal FIFO. If this bit is set when Write Gate is asserted and the Process Split/Flag Bit of the WCS Control Field is set, it pushes the content of the WCS Data Field Register into the internal FIFO where these values are used for the actual Split Count of the data field. Therefore, the firmware engineer only changes the WCS Data Field for the proper format of the actual sector. This saves time during format operation.
Bit 6	**END OF TRACK**: When this bit is set, if there was a good compare and good CRC and the Sector Count Register is not equal to zero, the Sector Target is reset to 00H at the end of the data transfer; the next sector to be read is Sector 00H. This function is used for Minimal Latency Operation, not Start/Stop Operation (explained in Section 4.2.1.3.1).
Bit 5	Not used.
Bit 4	**DEFECT**: This bit is used to indicate a defective sector. It is used for the Alternate Sector Scheme only where the defective sector is relocated to another location on the disk. This bit will determine the type of action to be taken using the proper WCS branch conditions.
Bits 3:0	These are the upper four bits of the split count for the data field.

LS Split Count

Bits 7:0	These are the lower eight bits of the split count for the data field.

Figure 4–1. Sample ID Field for Multisector Operation

NOTE: This refers to Section 4.2.1.3, *Multisector Read/Write Operation.*

4.2.1.3.1 Minimum-Latency Multisector Transfer

For minimum-latency operations, the Sector Count Register (6BH) should be loaded with the maximum number of sectors/track. The firmware reads the first ID field after the head reaches the track; it starts the Sequencer and only checks for good CRC and no defect, and pushes it into the stack. By reading the stack, it can appropriately load the Sector Target (6AH) with the next sector value and program the Disk Pointer (Register 5AH, 5BH) with the correct location of this sector in the buffer. The CL-SH366 will proceed to read/write the full track. At the end of the track, if the Sector Count Register is not equal to zero and the End of Track Bit in the ID Flag/LS Split Count Byte is set, the Sector Target Count Register (6AH) is appropriately reset to zero. The wrap of the Buffer Disk Pointer is controlled by setting the Buffer Start and Buffer End Address Pointers to values corresponding to the size of the track. Therefore, when the Disk Address Pointer (DAP) reaches the Buffer End Address, the DAP will be loaded with the Buffer Start Address. The next sector to be processed is Sector '00H'. This will save a maximum of one revolution before the right sector is reached.

4.2.1.3.2 Start/Stop Multisector Transfer

In a Start/Stop Multisector Operation, the Sector Count Register (6BH) is loaded with the number of sectors to be read or written, and the Sector Target Register (6AH) is loaded with the starting sector value. The Sequencer will start and stop appropriately at the end of the transfer of the last sector. There are multiple branch conditions that may stop the Sequencer before all the sectors are transferred. For example, if the previous sector ECC error is uncorrectable, the Sequencer will be stopped; if the Defect Bit in the Flag/LS Split Count Byte of the ID field is set, the Sequencer may stop or may take an alternate route in the WCS Map by the means of the React Branch Register (6CH).

4.2.1.4 Scheduled WCS Access

The WCS can be accessed by the microcontroller in a scheduled format. The Mode Bit — Scheduled WCS Access/Enable Bit (Register 7AH, Bit 6) — indicates the type of WCS access. If the Scheduled WCS Access/Enable Bit (Register 7AH, Bit 6) is set, the access to/from the WCS is scheduled through the Status WCS Byte Ready Bit (Register 7AH, Bit 4). When reading the WCS, the address is latched internally; the data is synchronously read from the WCS to an internal holding register, and the WCS Byte Ready Bit (Register 7AH, Bit 4) is set. After this bit is set, the microcontroller may read the next location or the same location again; the data read is the previous address data information and the process repeats. When writing to the WCS, the address and data is latched internally, and the data is synchronously written to the WCS. The WCS Byte Ready Bit (Register 7AH, Bit 4) is set to indicate that it is ready to accept another WCS Write Operation.

4.2.2 Functional Operation

The CL-SH366 performs two basic disk operations, reading NRZ data in and writing NRZ data out. These two operations can be combined easily into the following three major functions: Verify Sector, Format Sector and Disk Data Transfer. The CL-SH366 also performs data transfers to/from the PC. These can be broken down into two major groups: Data Transfer by PIO, and Data Transfer by DMA. These two host transfer options will be discussed in Section 4.4, *PC XT/AT Interface.*

4.2.2.1 Verify Sector

By setting the Suppress Transfer Bit in the Operation Control Register, (Register 7AH, Bit 5) and performing a Read Operation, the read data will only be verified for good ECC and will not be transferred to the buffer.

4.2.2.2 Format Sector

To format a track, the ID fields, all gaps (fill, postambles, and preambles), and data fields must be generated. This requires that the read ID field subroutine must be changed into a Write Operation, and appropriate gaps inserted. Also, by setting the Suppress Transfer Bit in the Operation Control Register (Register 7AH, Bit 5), the data for the Sector Data Field will be sourced from the Current Sequencer Word Data Field and will not be transferred from the buffer. The ID field bytes can be written from the buffer instead of updated by the local microcontroller. This is accomplished by setting the Data Transfer Bit in the WCS Control

Field. This will override the suppress-transfer function for the ID field only. If this method is used the local microcontroller must 'unlock' the buffer after the format command is received so that the ID field values can be retrieved.

4.2.2.3 Disk Data Transfer

For disk transfers, a byte is transferred each time the Formatter requires a data transfer (to serialize/deserialize a byte). The direction of transfer is determined by the Buffer/Disk R/W* Transfer Direction Bit (Register 53H, Bit 4). The Disk Address Pointer is used to select the buffer memory location.

For a Disk Read Operation, where disk NRZ data is deserialized and written to the buffer, the Buffer/Disk R/W* Transfer Direction Bit (Register 53H, Bit 4) must be set. When the disk transfer stops, the Disk Data Transfer Bit (Register 79H, Bit 7) is reset.

For a Disk Write Operation, where buffer data is serialized and written out to the disk as NRZ data, the Disk/Buffer R/W* Transfer Direction Bit (Register 53H, Bit 4) is reset. When the disk transfer stops, the Disk Data Transfer Bit (Register 79H, Bit 7) is reset.

4.2.3 Two Index Counter

Another component of the Format Sequencer is the Two Index Counter (TIC). This circuit is used to limit the execution of a Format Sequencer program to one complete revolution of the disk drive. This feature would typically be used to limit the number of the times that the Format Sequencer would attempt to search for the Sector ID Field of a Target Sector.

When the Two Index Detection Mode Enable Bit (Register 48H, Bit 6) is set, the Two Index Detection Mode circuitry is armed or rearmed by the WCS. The detection circuit is armed if the WCS Control Field has both Read Gate and Data Transfer off, and Bit 5 of the Count Field is set. Once the circuit is armed, it remains armed until one of following three events happens: 1) data transfer occurs between the Formatter and buffer; 2) Two Index pulses are detected and the Formatter is stopped; or 3) the Two Index Detection Mode Enable Bit is reset. When the detection circuit is armed, and the Two Index edges are detected, the Two Index Detected Status Bit is set (Register 48H, Bit 3). The status bit remains set until the Two Index Detection Mode is disabled (Register 48, Bit 6). When the Two Index Detected Status Bit is set, it asserts the 'stopped' signal to stop the Formatter Operation; this disarms the detection circuit.

4.2.4 Synchronization Timer

The Synchronization Timer is a circuit used to set a limit on the amount of time that the Format Sequencer is allotted to synchronize itself — or find and match the synchronization byte pattern defined in Register 7CH — with the incoming NRZ data stream. This limit is programmed in the CL-SH366 Synchronization Byte Count Limit Register (76H). This limit is specified in terms of a byte-count limit that can range from 0 to 255. Only one value can be programmed into Register 76H. When the Synchronization Timer is activated by the Format Sequencer program, the value in Register 76H is decremented for each byte time that passes. When the value within Register 76H reaches zero, a time-out occurs. When a time-out error occurs, the Format Sequencer can stop or branch (see Next Address Field Register description). In either case, the Synchronization Time-Out Error Bit (Register 48H, Bit 2) will also be set. The branch source is the WCS Data Field. This bit is reset by a Formatter reset (Register 71H, Bit 5) and a Sequencer start.

The Format Sequencer program can activate the Synchronization Timer by setting the Count/Start Synchronization Timer/Two Index Timer Bit (Bit 5 of the Writable Control Store (WCS) Count Field). This mode is selected when the Read Gate On (Bit 5-6 of the WCS Control Field Register) is set. Once the timer is activated, the time-out will either stop the Sequencer or branch to a new address. To set-up the branch condition, the WCS Data Field is set to the branch address during Read Gate On. The Synchronization Timer is reset under the following conditions: (1) when the Format Sequencer is reset, or (2) when the serial synchronization detector finds the synchronization character (as defined in Register 7CH) in the incoming NRZ data stream.

This feature would typically be used to limit the amount of time that the Format Sequencer is allowed to search for the Sector Data Field after it successfully completes a Sector-ID-Field comparison. The Synchronization Timer can also be used to limit the amount of time that the Format Sequencer searches for a Sector ID Field after a sector mark is detected in a hard-sectored disk drive.

4.3 Buffer Manager Interface

The third functional logic block of the CL-SH366 is the Buffer Manager interface. This block controls the flow of data between the external RAM data buffer and the CL-SH366 PC interface, the Sector Formatter data path, and the microcontroller buffer memory access ports. The Buffer Manager interface provides the external RAM addressing, timing, and control signals necessary for the CL-SH366 to interface with the RAM data buffer. The CL-SH366 can interface to either static RAM, (up to 128K bytes SRAM) or dynamic RAM, (up to 4 Mbytes DRAM). Details of both of these types of buffer RAM configuration will be given in the following sections.

4.3.1 SRAM Addressing Operation

The Buffer Manager interface can address up to 128K bytes of static memory. This requires 17 address lines that correspond to the Buffer Manager Address Signals BA[16:0] (PQFP Pins 5, 90-79 and 77-74; VQFP Pins 54, 39-28 and 26-23). The buffer memory address is never placed in a high-impedance state; it is always driven by one of three sources — the Disk Address Pointer (Registers 5AH-5BH or 20H/A0H-22H/A2H), the Host Address Pointer (Registers 5CH-5DH or 24H/A4H-26HA6H) or the ECC Corrector. These pointers have various initialization conditions, and their starting values can be changed via direct firmware control.

The Disk Address Pointer (Registers 5AH-5BH or 20H/A0H-22H/A2H) is dedicated for disk and microcontroller transfers. Any access to the RAM data buffer by the Sector Formatter selects the value in Registers 5AH-5BH or 20H/A0H-22H/A2H, (the Disk Address Pointer) that will be driven out on the buffer memory address bus.

When the local microcontroller accesses the buffer memory, the Disk Address Pointer (Registers 5AH-5BH or 20H/A0H-22H/A2H) is also used. Consequently, to prepare for a local microcontroller access to the buffer memory, all disk transfers to or from the CL-SH366 must be terminated before the Disk Address Pointer (Registers 5AH-5BH or 20H/A0H-22H/A2H) is loaded.

The Host Address Pointer (Registers 5CH-5DH or 24H/A4H-26H/A6H) is reserved for transfers between the PC bus and the RAM data buffer. Any access to the RAM data buffer by the PC interface logic selects the value in Registers 5CH-5DH or 24H/A4H-26H/A6H, the Host Address Pointer, and has the CL-SH366 drive this value onto the buffer memory address bus.

The Host Address Pointer (Registers 5CH-5DH or 24H/A4H-26H/A6H) is compared with the Stop Address Pointer (Registers 5EH-5FH or 28H/A8H-2AH/AAH) to contain the data transfers to a particular block-boundary value. To translate the value of the Host Address Pointer (Registers 5CH-5DH or 24H/A4H-26H/A6H) into a repeatable block size, the Buffer Size/Segment Address Register (54H) is used to mask the upper address bits of the Host Address Pointer (Registers 5CH-5DH or 24H/A4H-26H/A6H) and the Stop Address Pointer (Registers 5EH-5FH or 28H/A8H-2AH/AAH). Consequently, only the lower significant bits that are 'modulo a' block size are used for the comparison. When there is an equal comparison of the Host Address Pointer (Registers 5CH-5DH or 24H/A4H-26H/A6H) and the Stop Address Pointer (Register 5DH-5FH), masked by the Buffer Size/Segment Address Register (54H), then the host transfer is terminated.

Both the Disk Address Pointer (Registers 5AH-5BH or 20H/A0H-22H/A2H) and the Host Address Pointer (Registers 5CH-5DH or 24H/A4H-26H/A6H) are automatically incremented by a count of one after the completion of each access to the RAM data buffer.

4.3.2 SRAM Buffer Segmentation

For optimum data flow control, it is often desirable to divide the buffer memory into smaller segments. The CL-SH366 Buffer Manager can support fixed

and variable segment sizes. In Fixed Mode, the buffer can be divided into 4K, 8K, 16K, 32K, 64K or 128K segments. For example, with an attached buffer size of 32K and segment sizes of 4K, this would create eight 4K segments: 0000-0FFFH, 1000-1FFFH, 2000-2FFFH, 3000-3FFFH, 4000-4FFFH, 5000-5FFFH, 6000-6FFFH, 7000-7FFFH. When operating in this mode, the Buffer Start Address Registers (9FH-BFH or 30H/B0H-32H/B2H) and the Buffer End Address Registers (DFH-FFH or 34H/B4H-36H/B6H) are loaded with the physical size of the attached static RAM buffer. Each segment can be accessed by setting the upper four bits of the HAP and DAP to the desired segment address. In this configuration, once the address pointer (HAP or DAP) reaches X1FFFH, the next address will roll over to X1000H.

In the second mode, the CL-SH366 provides the ability to generate a variable segment within the buffer memory by providing Buffer Start Address Registers (9FH-BFH or 30H/B0H-32H/B2H) and Buffer End Address Registers (DFH-FFH or 34H/B4H-36H/B6H). By loading the Buffer Start Address Register (9FH-BFH or 30H/B0H-32H/B2H) with the starting segment address and the Buffer End Address Register (DFH-FFH or 34H/B4H-36H/B6H) with the ending segment address, whenever the Disk Address Pointer (DAP — Registers 5AH-5BH or 20H/A0H-22H/A2H) or Host Address Pointer (HAP — Registers 5CH-5DH or 24H/A4H-26H/A6H) are equal to the Buffer End Address Register, they are reloaded with the Buffer Start Address Register value. When operating in this mode, the Buffer Size/Segment Address Register (Register 54H) must be set to the physical size of the attached static RAM buffer.

4.3.3 SRAM Read/Write Access Control

The Buffer Manager accesses the buffer memory data bus to read or to write the contents of the RAM data buffer, or to read the static state of the data bus. The PC host, the Sector Formatter, and the local microcontroller all use unique methods to specify the direction of the access.

For PC host transfers, the read/write control is set by the PC R/W* Transfer Direction Bit (Bit 3) of the Buffer Transfer Control Register (53H). When this bit is set, the data read from the RAM data buffer is transferred through the CL-SH366 chip to the PC host interface. If this bit is reset, then the data is transferred from the PC host interface through the CL-SH366 and written to the RAM data buffer.

In the case of Sector Formatter transfers, the transfer direction is controlled by the Buffer/Disk R/W* Transfer Direction Bit (Bit 4) of the Buffer Transfer Control Register (53H). When this bit is reset, the data read from the RAM data buffer is transferred to the Sector Formatter. To write to the RAM data buffer from the Sector Formatter, this bit must be set.

For microcontroller transfers, the microcontroller control strobe is used to determine the transfer direction. A read of Register 68H (the Scheduled Buffer Data Register) or Register 70H (the Microcontroller Buffer Access Register) results in a read of the RAM data buffer. A write to Register 68H (the Scheduled Buffer Data Register) or Register 70H (the Microcontroller Buffer Access Register) causes a write to the RAM data buffer.

Both a Read and Write Operation commence when the correct address pointer — the Disk Address Pointer (Registers 5AH-5BH or 20H/A0H-22H/A2H), or the Host Address Pointer (Registers 5CH-5DH or 24H/A4H-26H/A6H) — is driven onto the buffer memory address bus.

For a read from the RAM data buffer, the Chip Enable Signal (CE1* — Pin 3/52) is asserted at the same time as the address is driven onto the address bus. The Memory Output Enable Signal (MOE* — Pin 1/50) is also asserted as the address is driven onto the address bus. This signal should be connected to the SRAM Output Enable(s) to ensure the highest throughput. Data must be provided from the SRAM shortly before the rising (trailing) edge of the Memory Output Enable Signal (MOE* — Pin 1/50). The Write Enable Signal (WE* — Pin 2/51) remains deasserted throughout the entire SRAM read access.

For a write to the RAM data buffer, the Chip Enable Signal (CE1* — Pin 3/52) is asserted at the same time as the address is driven onto the address bus; the Write Enable Signal (WE* — Pin 2/51) is asserted after the address is driven onto the address bus. The Memory Output Enable Signal

(MOE* — Pin 1/50) remains deasserted (high) throughout the entire SRAM access. Data is driven from the CL-SH366 to the RAM data buffer shortly after the address. The Write Enable Signal (WE* — Pin 2/51) is deasserted (high) near the end of the cycle. The CL-SH366 supports two-chip enables for 64K buffers. This mode is controlled by Register 53H, Bit 0, and uses BA15/CE2* (Pin 90/39) as the second chip enable.

4.3.4 SRAM Signal Timing

For both a read and a write access to the RAM data buffer, the correct address pointer (the Disk Address Pointer — Registers 5AH-5BH or 20H/A0H-22H/A2H and the Host Address Pointer — Registers 5CH-5DH or 24H/A4H-26H/A6H) is driven with respect to the rising edge of the BCLK Input Signal (Pin 39/88). For read accesses, the Memory Output Enable Signal (MOE* — Pin 1/50) is asserted after the rising edge of the BCLK at the same time as the address is driven onto the address bus. For write accesses, the Write Enable Signal (WE* —.Pin 2/51) is asserted one-half BCLK after the address is driven. The Memory Output Enable Signal (MOE* — Pin 1/50) and the Write Enable Signal (WE* — Pin 2/51) are both deasserted (high) by BCLK before the end of the SRAM access. This implies that the total SRAM access time controls the pulse width of these signals. The complete SRAM access time is programmed in terms of BCLK-Input-Signal (Pin 39/88) periods.

In the case of a read access to the RAM data buffer, data is clocked into the CL-SH366 by the rising edge of the Memory Output Enable Signal (MOE* — Pin 1/50). In the case of a write, data is held by the CL-SH366 until the deassertion of the Write Enable Signal (WE* — Pin 2/51).

The theoretical maximum Buffer Manager throughput is 12 Mbytes/second. The actual throughput is a function of the NRZ clock frequency from the disk drive, the SRAM speed used or required, the desired host throughput, the Input-BCLK-Signal (Pin 39/88) frequency, and the BCLK divider selected in the Clock Control Register (Register 7FH).

4.3.5 DRAM Addressing Operation

The Buffer Manager interface can address up to 4 Mbytes of dynamic RAM (DRAM) memory. This requires 12 address lines, one row address select (RAS), and one column address select (CAS). These signals correspond to the Buffer Manager Address Signals, BA[12:0] (PQFP Pins 86-79 and 77-74; VQFP Pins 35-28 and 26-23), row address select, RAS* (PQFP Pin 88; VQFP Pin 37), and column address select, CAS* (PQFP Pin 89; VQFP Pin 38). The buffer memory address bus is never placed in a high-impedance state; it will always be driven by the internal DRAM controller. The source for the address that will be output is either the Disk Address Pointer (Registers 5AH-5BH or 20H/A0H-22H/A2H), the Host Address Pointer (Registers 5CH-5DH or 24H/A4H-26HA6H) or the ECC Corrector. These pointers have various initialization conditions, and their starting values can be changed via direct firmware control.

The Disk Address Pointer (Registers 5AH-5BH or 20H/A0H-22H/A2H) is dedicated for disk and microcontroller transfers. Any access to the RAM data buffer by the Sector Formatter selects the value in Registers 5AH-5BH or 20H/A0H-22H/A2H (the Disk Address Pointer), this value will be converted to a physical address by the internal DRAM controller and driven out on the buffer memory address bus.

When the local microcontroller accesses the buffer memory, the Disk Address Pointer (Registers 5AH-5BH or 20H/A0H-22H/A2H) is also used. Consequently, to prepare for a local microcontroller access to the buffer memory, all disk transfers to or from the CL-SH366 must be terminated before the Disk Address Pointer (Registers 5AH-5BH or 20H/A0H-22H/A2H) is loaded.

The Host Address Pointer (Registers 5CH-5DH or 24H/A4H-26H/A6H) is reserved for transfers between the PC bus and the DRAM data buffer. Any access to the DRAM data buffer by the PC interface logic selects the value in Registers 5CH-5DH or 24H/A4H-26H/A6H, the Host Address Pointer, and has the CL-SH366 drive this value onto the buffer memory address bus.

The Host Address Pointer (Registers 5CH-5DH or 24H/A4H-26H/A6H) is compared with the Stop Address Pointer (Registers 5EH-5FH or 28H/A8H-2AH/AAH) to contain the data transfers to a particular block-boundary value. To translate the value of the Host Address Pointer (Registers 5CH-5DH or 24H/A4H-26H/A6H) into a repeatable block size, the Buffer Size/Segment Address Register (54H, DRAM Option) is used to mask the upper address bits of the Host Address Pointer (Registers 5CH-5DH or 24H/A4H-26H/A6H) and the Stop Address Pointer (Registers 5EH-5FH or 28H/A8H-2AH/AAH). Consequently, only the lower significant bits that are 'modulo a' block size are used for the comparison. When there is an equal comparison of the Host Address Pointer (Registers 5CH-5DH or 24H/A4H-26H/A6H) and the Stop Address Pointer (Register 5DH-5FH), masked by the Buffer Size/Segment Address Register (54H), then the host transfer is terminated.

Both the Disk Address Pointer (Registers 5AH-5BH or 20H/A0H-22H/A2H) and the Host Address Pointer (Registers 5CH-5DH or 24H/A4H-26H/A6H) are automatically incremented by a count of one after the completion of each access to the RAM data buffer.

4.3.6 DRAM Buffer Segmentation

For optimum data flow control, it is often desirable to divide the buffer memory into smaller segments. The CL-SH366 Buffer Manager can support fixed and variable segment sizes. In Fixed Mode, the buffer can be divided into 4K, 8K, 16K, 32K, 64K, 128K, 256K, 512K, 1M or 4M segments. For example, with an attached buffer size of 256K and segment sizes of 32K, this would create eight 32K segments: 00000-07FFFH, 08000-0FFFFH, 10000-17FFFH, 18000-1FFFFH, 20000-27FFFH, 28000-2FFFFH, 30000-37FFFH, 38000-3FFFFH. When operating in this mode, the Buffer Start Address Registers (9FH-BFH or 30H/B0H-32H/B2H) and the Buffer End Address Registers (DFH-FFH or 34H/B4H-36H/B6H) are loaded with the physical size of the attached dynamic RAM buffer. Each segment can be accessed by setting the upper seven bits of the HAP and DAP to the desired segment address. In this example, this will require changing the Host Address Pointer Top (HAPT, Register 24H/A4H) and the Host Address Pointer High (HAPH, Register 5CH or 25H/A5H). In this configuration, once the address pointer (HAP or DAP) reaches X7FFFH, the next address will roll over to X0000H (X = upper seven bits of the segment address).

In the second mode, the CL-SH366 provides the ability to generate a variable segment within the buffer memory by providing Buffer Start Address Registers (9FH-BFH or 30H/B0H-32H/B2H) and Buffer End Address Registers (DFH-FFH or 34H/B4H-36H/B6H). By loading the Buffer Start Address Register (9FH-BFH or 30H/B0H-32H/B2H) with the starting segment address and the Buffer End Address Register (DFH-FFH or 34H/B4H-36H/B6H) with the ending segment address, whenever the Disk Address Pointer (DAP — Registers 5AH-5BH or 20H/A0H-22H/A2H) or Host Address Pointer (HAP — Registers 5CH-5DH or 24H/A4H-26H/A6H) are equal to the Buffer End Address Register, they are reloaded with the Buffer Start Address Register value. When operating in this mode, the Buffer Size/Segment Address Register (Register 54H, DRAM Option) must be set to the physical size of the attached dynamic RAM buffer.

4.3.7 DRAM Read/Write Access Control

The Buffer Manager accesses the buffer memory data bus to read or to write the contents of the RAM data buffer, or to read the static state of the data bus. The PC host, the Sector Formatter, and the local microcontroller all use unique methods to specify the direction of the access.

For PC host transfers, the read/write control is set by the PC R/W* Transfer Direction Bit (Bit 3) of the Buffer Transfer Control Register (53H). When this bit is set, the data read from the RAM data buffer is transferred through the CL-SH366 chip to the PC host interface. If this bit is reset, then the data is transferred from the PC host interface through the CL-SH366 and written to the RAM data buffer.

In the case of Sector Formatter transfers, the transfer direction is controlled by the Buffer/Disk R/W* Transfer Direction Bit (Bit 4) of the Buffer Transfer Control Register (53H). When this bit is reset, the data read from the RAM data buffer is

transferred to the Sector Formatter. To write to the RAM data buffer from the Sector Formatter, this bit must be set.

For microcontroller transfers, the microcontroller control strobe is used to determine the transfer direction. A read of Register 68H (the Scheduled Buffer Data Register) results in a read of the DRAM data buffer. A write to Register 68H (the Scheduled Buffer Data Register) causes a write to the DRAM data buffer.

Both a Read and Write Operation commence when the correct address pointer — the Disk Address Pointer (Registers 5AH-5BH or 20H/A0H-22H/A2H), or the Host Address Pointer (Registers 5CH-5DH or 24H/A4H-26H/A6H) — is converted to a physical address by the internal DRAM controller and driven onto the buffer memory address bus.

4.3.8 DRAM Signal Timing

For both a read and a write access to the DRAM data buffer, the correct address pointer (the Disk Address Pointer — Registers 5AH-5BH or 20H/A0H-22H/A2H or the Host Address Pointer — Registers 5CH-5DH or 24H/A4H-26H/A6H) is driven out by the internal DRAM controller. When this is performing a Read Operation, it first decodes the desired address and drives out a row address followed by a Row Address Strobe (RAS* — Pin 88/37), and then a column address followed by a Column Address Strobe (CAS* — Pin 89/38). The DRAM controller uses the first rising edge of BCLK to drive the row address out. The RAS* Signal is asserted on the next falling edge of BCLK. The next rising edge of BCLK causes the address outputs to switch to the column address. The next falling edge of BCLK asserts both the CAS* Signal and the MOE* Signal. The RAS*, CAS*, and MOE* Signals are deasserted on the next falling edge of BCLK. This allows the next DRAM memory access cycle to start on the next rising edge of BCLK.

A Write Operation is similar to a Read Operation except that instead of MOE*, the WE* Signal is asserted by the same edge of BCLK that is used to assert the RAS*. WE* is then deasserted at the same time as RAS* and CAS*. For more detailed timing information, see the DRAM Write /Read/Refresh Timing in Chapter 9.

The theoretical maximum Buffer Manager throughput is 12 Mbytes/second. The actual throughput is a function of the NRZ clock frequency from the disk drive, the DRAM speed used or required, the desired host throughput, and the Input-BCLK-Signal (Pin 39/88) frequency.

4.3.9 DRAM Data Parity

The CL-SH366 can provide data parity protection for the DRAM buffer. This option can be enabled by setting the Buffer Parity Enable Bit in the Buffer Mode Control Register (Shadow Register 53H, Bit 2). If parity is enabled, the BDP Signal (Pin 87/36) will function as the parity bit for the 8-bit buffer data bus.

4.4 PC XT/AT Interface

The CL-SH366 provides the capability for direct connection to the host bus. The host bus drivers can sink up to 24 mA of current and drive a load of up to 300 pF. To reduce noise on the ATA bus, the host data bus drivers on the CL-SH366 have been specifically designed. The drivers turn on at 12 mA for a short period of time, then switch to the full 24-mA drive capability until the new voltage level is reached. This feature will reduce the noise on the ATA cable that is associated with high slew-rate signals.

The CL-SH366 uses the BD5/IDE/PCMCIA* Signal (Pin 98/47) after reset to select between IDE- or PCMCIA-compatible levels on the Host Reset Signal and Host Interrupt Signal. The BD5/IDE/PCMCIA* Signal (Pin 98/47) has an internal pull-up resistor. If this pin is connected to an external pull-down resistor after reset, the CL-SH366 will operate with HRST active-high and HINT* active-low (PCMCIA-compatible Mode). If this pin is only connected to the data port of the buffer RAM without an external pull-down resistor, the CL-SH366 will recognize the high level (internal pull-up) on this signal and will operate with HRST* active-low and HINT active-high (IDE Mode). The firmware can set the mode (IDE or PCMCIA) of operation by programming Bit 0 of the IDE/PCMCIA Register (Register 6FH).

4.4.1 PC Transfers

For transfers between the PC bus and buffer memory, data is transferred under DMA or PIO control. Transfers are enabled by setting the DMA Start Bit (Register 53H, Bit 1). The transfer direction is determined by the contents of the PC R/W* Transfer Direction Bit (Register 53H, Bit 3). The contents of the Host Address Pointer are used to address the buffer memory.

During the PC data transfer, the last buffer address that can be accessed is controlled by the PC Stop Pointer. This PC Stop Pointer is compared with the Host Address Pointer, masked by the content of the Buffer Size/Segment Address Register (Register 54H). When a match occurs, the PC Transfer Done Bit (Register 53H, Bit 2) is set, signifying the completion of the transfer to or from the PC bus.

4.4.1.1 PC Direct Memory Access (DMA) Operations

The CL-SH366 operates in DMA Mode for both XT and AT protocols. There are two modes of DMA operation: Single Transfer per Bus Arbitration and Multiple Transfers per Bus Arbitration (EISA Type 'B' Demand Mode). No interrupts to the host are generated during DMA transfers. The three control bits that select DMA Mode are: the AT Host Fixed Disk Register DMAENB (Register 52H, Bit 4), the Demand Mode DMA Enable Bit (Register 53H, Bit 7) and the PIO or DMA Select Bit (Register 58H, Bit 3).

Tables 4–2 and 4–3 summarize the use of these bits for XT and AT DMA operations.

Table 4–2. XT DMA

Reg 53H, Bit 7	Description
0	During the Data Phase, Single Transfer Mode can occur if the host enables Bit 0 of the Drive/DMA/Interrupt Enable Register.
1	During the Data Phase, Multiple Transfer Mode can occur if the host enables Bit 0 of the Drive/DMA/Interrupt Enable Register.

Table 4–3. AT DMA

Reg. 58H, Bit 3	Reg. 52H, Bit 4	Reg. 53H, Bit 7	Description
1	X	X	No DMA transfers enabled
0	0	0	Single-transfer DMA enabled through the Data Register (1F0H)
0	0	1	Multiple-transfer DMA enabled through the Data Register (1F0H)
0	1	0	Single-transfer DMA enabled if Bit 0 of the Fixed Disk Register (3F6H) is set through the Data Register (1F0H)
0	1	1	Multiple-transfer DMA enabled if Bit 0 of the Fixed Disk Register (3F6H) is set through the Data Register (1F0H)

NOTE: X = Don't care

4.4.1.1.1 Single-Transfer DMA

In Single-transfer DMA Mode, the CL-SH366 asserts DREQ (Pin 49/98) for each transfer. In this mode, the host bus is arbitrated for each transfer, since the DREQ Signal is deasserted in response to the DACK* (Pin 50/99) Signal.

4.4.1.1.2 Multiple-Transfer DMA (EISA Type 'B' Demand Mode)

In Multiple-transfer DMA Mode, the CL-SH366 asserts DREQ (Pin 49/98) for the length of the transfer, but will deassert DREQ to stop an overrun/underrun. If a higher-priority DMA device requires the bus, the host can deassert DACK* (Pin 50/99) during the transfer; or, if no other higher-priority device requests the bus, the host may assert DACK* for the length of the transfer.

4.4.2 PC Host Wait States

The CL-SH366 also provides circuitry to extend the host I/O cycle and insert wait states by asserting low the IOCHRDY* Signal (Pin 48/97). This circuit is only active during programmed I/O host transfers. The CL-SH366 inserts wait states in the following two ways:

1) It can be programmed in the PC Mode Control (Register 58H, Bits 0 and 1) to insert wait states on any host I/O transfer. This can be used to extend the width of the IOR*/IOW* pulse, in case of a fast CPU with short IOR*/IOW* pulses.

2) When the automatic wait-state generation feature is enabled (Register 58H, Bit 2 is set), a wait state will be automatically inserted by asserting low the IOCHRDY* Signal (Pin 48/97) (only during host I/O transfers to/from buffer memory) when the CL-SH366 is not ready for the transfer.

If programmed wait states (see Item 1) are enabled, and if any additional wait states are necessary, the automatic wait-state circuit will be activated. This occurs after the programmed number of wait states have been inserted.

4.4.3 PC Host Auto-Commands

The CL-SH366 has circuitry to speed up the performance of the disk controller by decoding write commands requiring data transfer from the host to the buffer memory, i.e., Format (5XH), Write Buffer (E8H), Write or Write Long (3XH). The CL-SH366 will automatically start accepting data from the host, without local microcontroller control, when the AT Host Command Register is loaded by the host. If interrupts are enabled, the CL-SH366 then generates an interrupt to the local microcontroller. The Stop Pointer (Registers 5EH and 5FH) is initialized to 01FFH. If the Buffer Stop Pointer Disable (Register 52H, Bit 6) is set, the local microcontroller must initialize the Stop Pointer (Registers 5EH and 5FH) to enable the comparison of the Host Address Pointer (HAP Registers 5CH and 5DH) with the Stop Pointer. The CL-SH366 Sector Formatter will disconnect from the Buffer Manager upon receipt of one of these commands. It will also disable write access by the local microcontroller to Registers 53H, 5CH-5FH, and read/write access to Registers 68H and 70H. Access to these registers will be enabled when the local microcontroller writes to Register 73H. The local microcontroller must write to Register 73H to enable transfers between the Sector Formatter and the buffer memory.

4.4.4 PC Host Long Commands

If Bit 1 of the command byte is set (for read/write long commands), then all buffer memory transfers to/from the host will exceed the Stop Pointer (Registers 5EH and 5FH) by the count of ECC bytes. Initially, the Stop Pointer is set at the end of the data field. When the Host Address Pointer (Registers 5CH and 5DH) matches the Stop Pointer, the internal FIFO will be emptied of the word-width data. The ECC bytes will then be transferred in Byte Mode, and the HAP will be incremented by the number of ECC bytes, as defined in the Host 32-/56-/88-Bit ECC Select (Register 71H, Bits 3-2).

4.4.5 PC Host Master/Slave Operation

The CL-SH366 provides circuitry to support two embedded AT or XT disk controller drives in a system. There are two bits (Bits 1 and 2) in Register 52H for this configuration. The Master/Slave Mode Enable Bit (Register 52H, Bit 1) must be set to enable the two-disk-drive master/slave configuration. The Master/Slave Select Bit (Register 52H, Bit 2) configures the disk drive as a master or slave. For the PC AT — if this bit is set — the disk controller responds as a slave (i.e., it responds when the disk drive number in the AT Host Drive/Head Register [Port 1F6H] is set to a 1). The register files in both controllers, when configured as master and slave, will be written to by the host, no matter which drive is selected in the AT Host Drive/Head Register. However, only the selected disk drive will execute the command. The only exception is during power-up or diagnostic commands; both the master and the slave will run the diagnostics, but the master will return the status for both drives to the host. For the PC XT, the controller responds as a slave if Bit 2 of the host DRV/DMA/IRQ Enable Register is set, and Register 52H, Bit 2 is set.

In addition to these features, the CL-SH366 also provides the local microcontroller with PDIAG* and DASP* support in the Auxiliary Control 1 Register (Register 4FH, Bits 2-1). This register may be programmed by the local microcontroller to implement ATA-compatible multiple-drive operation.

5. DETAILED INTERNAL REGISTER DESCRIPTION

The register tables refer to the following register types: R/W = Read/Write, R = Read only, W = Write only.

5.1 Register 30H/B0H: Buffer Start Address Top Register (BSAT) (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83), or Buffer Manager Reset (Register 59H, Bit 0). This register can **only** be accessed after a write to Register S53H (Shadow 53H).

Bits 5-0	R/W	These bits are the highest-order bits of the buffer memory start address.
Bits 7-6	—	Reserved.

5.2 Register 9FH *or* 31H/B1H: Buffer Start Address High Register (BSAH) (Read/Write)

Register 31H/B1H is the same as Register 9FH. Register 31H/B1H can **only** be accessed after a write to Register S53H (Shadow 53H).

This register is reset by the assertion of RST* (Pin 34/83), or Buffer Manager Reset (Register 59H, Bit 0).

Bits 7-0	This register is the high-order byte of the buffer memory start address.

5.3 Register BFH *or* 32H/B2H: Buffer Start Address Low Register (BSAL) (Read/Write)

Register 32H/B2H is the same as Register BFH. Register 32H/B2H can **only** be accessed after a write to Register S53H (Shadow 53H).

This register is reset by the assertion of RST* (Pin 34/83), or Buffer Manager Reset (Register 59H, Bit 0).

Bits 7-0	This register is the low-order byte of the buffer memory start address.

5.4 Register 34H/B4H: Buffer End Address Top Register (BEAT) (Read/Write)

This register is set to 3FH by the assertion of RST* (Pin 34/83), or Buffer Manager Reset (Register 59H, Bit 0). This register can **only** be accessed after a write to Register S53H (Shadow 53H).

Bits 5-0	R/W	These bits are the highest-order bits of the buffer memory end address.
Bits 7-6	—	Reserved.

5.5 Register DFH *or* 35H/B5H: Buffer End Address High Register (BEAH) (Read/Write)

Register 35H/B5H is the same as Register DFH. Register 35H/B5H can **only** be accessed after a write to Register S53H (Shadow 53H).

This register is set to FFH by the assertion of RST* (Pin 34/83), or Buffer Manager Reset (Register 59H, Bit 0).

Bits 7-0	This register is the high-order byte of the buffer memory end address.

5.6 Register FFH *or* 36H/B6H: Buffer End Address Low Register (BEAL) (Read/Write)

Register 36H/B6H is the same as Register FFH. Register 36H/B6H can **only** be accessed after a write to Register S53H (Shadow 53H).

This register is set to FFH by the assertion of RST* (Pin 34/83), or Buffer Manager Reset (Register 59H, Bit 0).

Bits 7-0	This register is the low-order byte of the buffer memory end address.

5.7 Register 48H: Auxiliary Control 0 Register (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83).

Bit 0	R/W	**BUFFER POINTER AUTO-INCREMENT ENABLE**: This bit, when set, allows auto-incrementing of the buffer address when the microcontroller reads or writes Register 68H or 70H for buffer accesses.
Bit 1	R/W	**SHADOW REGISTER SELECT:** This bit, when set, selects the Shadow Registers S53H and S71H.
Bit 2	R	**SYNCHRONIZATION TIME-OUT ERROR**: This bit is set after the timer limit that is held in the Synchronization Byte-Count Limit Register (Register 76H) has expired, and read synchronization has not occurred. This bit is reset by Register 71H, Bit 5 or a write to Register 79H.
Bit 3	R	**TWO INDEX DETECTED STATUS**: This bit is set when the Two Index Detection circuit has been enabled and Two Index edges have been detected without a data transfer between the formatter and buffer. This bit is reset when the Two Index Detection Mode is disabled (Register 48, Bit 6 = 0) or when the Two Index detection circuit is armed.

5.7 Register 48H: Auxiliary Control 0 Register (Read/Write) *(cont.)*

Bit 4	R/W	**CLEAR FIXED DISK REGISTER — BIT 0**: This bit is used to reset the DMA Enable Control Bit in the Fixed Disk Register (3F6H). To reset the Fixed Disk Register, Bit 0, set and clear this bit. This bit is reset by HRST*/HRST (Pin 53/2), RST* (Pin 34/83), and a host-programmed reset.
Bit 5	R	**PC HOST PROGRAM RESET**: This bit is set by a host-programmed reset. This bit is reset by RST* (Pin 34/83) or by setting the Clear PC Host Program Reset Bit (Register 48H, Bit 7). This bit is set for the duration of the host-program-reset active time.
Bit 6	R/W	**TWO INDEX DETECTION MODE ENABLE**: When this bit is set, the Two Index Detection Mode is enabled. When the Two Index Detection Mode is enabled, the index detection circuit is armed or rearmed by the WCS. The detection circuit is armed if the WCS Control Field has both Read Gate and Data Transfer off, and Bit 5 of the Count Field is set. Once the circuit is armed, it remains armed until one of the following three events takes place: 1) data transfer occurs between the formatter and buffer; 2) Two Index pulses are detected and the formatter is stopped; or, 3) the Two Index Detection Mode Enable Bit is reset. When the detection circuit is armed, and Two Index edges are detected, and the Two Index Detected Status Bit is set (Register 48H, Bit 3). The Status Bit remains set until the Two Index Detection Mode is disabled. When the Two Index Detected Status Bit is set, it asserts the 'stopped' signal to stop the Formatter Operation. This, in turn, disarms the detection circuit. This bit is reset by RST* (Pin 34/83) and Register 71H, Bit 5.
Bit 7	R	**BYTE READY**: When this bit is set, it indicates that a scheduled buffer memory access is complete, and that another scheduled buffer memory access may be started.
Bit 7	W	**CLEAR PC HOST PROGRAM RESET**: When this bit is set, it will clear the PC Host Program Reset Bit (Register 48H, Bit 5).

5.8 Register 4DH: 68H and 70H Read Data Register (Read Only)

This register is reset by the assertion of RST* (Pin 34/83) or Register 71H, Bit 5.

Bits 7-0	R	**BUFFER DATA SHADOW REGISTER**: When the microcontroller reads Registers 68H and 70H, the contents of the buffer memory data bus will be captured in Register 4DH for future reference. This register is reset by assertion of RST* (Pin 34/83) or when the Formatter Reset Bit (Register 71H, Bit 5) is set.

5.9 Register 4EH: Sector Size Register (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83).

Bits 7-0	R/W	Writing to this register sets the number of 256-byte data blocks transferred by the Disk Formatter when the Inhibit Carry Bit (Register 7AH, Bit 7) is used. If this register is set (or reset) to 00H, the Inhibit Carry function will be compatible with the CL-SH130. The value programmed, plus one, is the number of the Current Sequencer Count Field underflows that will be inhibited. For a 532-byte data field, set the WCS Count value to 13H (19), the Sector Size (Register 4EH) to 01H, and set the three most-significant bits of the Next Address Field Register of the WCS to 100 when the Data Transfer Bit (WCS Control Field Register, Bit 0) is set. For a 4096-byte data field, set the WCS count value to FFH, the sector size to 0EH (14), and set Inhibit Carry.

5.10 Register 4FH: Auxiliary Control 1 Register (Read/Write)

Bit 0	R/W	**ADVANCED MULTISECTOR/MULTISECTOR***: When set, the Sequencer will use the Sector Remaining Counter, Sector Target and Sector Count Register to control the Multisector Read/Write Operations. This will use the embedded-data-split counts in the ID field and the automatic increment of the sector number to control the Multisector Operations without the intervention of the microcontroller. When reset, the microcontroller must update the WCS for every sector of a Multisector Read/Write Operation. This bit is reset by the assertion of RST* (Pin 34/83).
Bit 1	R/W	**PASS DIAGNOSTICS**: This bit controls the PDIAG* (Pin 27/76) function that is used for master/slave operation on embedded AT drives. A read of this bit inputs the state of the pin, while a write of this bit drives the pin.
Bit 2	R/W	**SLAVE PRESENT**: This bit controls the 1FCLK/DASP*(Pin 28/77) when it is configured to operate as DASP* (Register 7FH — Bits 3 and 4 are not 00). The DASP* function is used for master/slave operations on embedded AT drives. A read of this bit inputs the state of the pin, while a write of this bit drives the pin.
Bit 3	R/W	**CLEAR XT BUSY ENABLE (PC/XT Mode only)**: This bit, when set, will allow the automatic clear of the Busy Bit (Register 55H, Bit 7) in the XT Mode when the host reads the Completion Status Byte at the end of all commands. This bit is reset by the assertion of RST* (Pin 34/83).
Bit 4	R/W	**DISABLE PIN PULL-UP RESISTORS**: This bit, when set, will disable the pull-up resistors on HCS0* (Pin 47/96), HA9/HCS1* (Pin 46/95), INPUT2/HOSTINT* (Pin 5/54), PDIAG* (Pin 27/76), and 1FCLK/DASP* (Pin 28/77).

5.10 Register 4FH: Auxiliary Control 1 Register (Read/Write) *(cont.)*

Bit 5	R/W	**LOCAL INTERFACE POWER DOWN**: The CL-SH366 will wake up from this mode by a write to the AT Command Register or XT Select Register, or assertion of HRST*/HRST (Pin 53/2), RST* (Pin 34/83), or by setting the Reset Bit in the AT Fixed Disk Register (3F6, Bit 2). This bit is locked by a write to the AT Command Register or the XT Select Register. It can be unlocked by a write to Register 73H.
Bit 6	R/W	**HOST ATA POWER DOWN**: The CL-SH366 will wake up from this mode by assertion of HRST*/HRST (Pin 53/2) or RST* (Pin 34/83), or by setting the Reset Bit in the AT Fixed Disk Register (3F6, Bit 2).
Bit 7	R/W	**HOST DEEP SLEEP MODE**: The CL-SH366 will wake up from this mode by assertion of HRST*/HRST (Pin 53/2) or RST* (Pin 34/83).

5.11 Register 50H: PC Interrupt Status Register (Read Only)

This register is reset by the assertion of HRST*/HRST (Pin 53/2), RST* (Pin 34/83), or a host-programmed reset. Bit 4 of this is reset by RST* (Pin 34/83) only. All bits are cleared by a read of this register.

Bit 0	R	**PC TRANSFER DONE**: When this bit is set, it indicates the completion of a host transfer [i.e., the PC Stop Pointer, (Registers 5EH-5FH), is equal to the Host Address Pointer, (HAP — Registers 5AH and 5BH)]. After this bit is set, the Host Address Pointer will read one byte more than the value of the PC Stop Pointer. This bit is reset when the host writes to the Command Register. In the Master/Slave Mode, this bit is only reset by a write to the Command Register if the DRV Select Bit matches the master/slave select configuration. This bit is the same as Register 53H, Bit 2.
Bit 1	R	**PC TRANSFER OVERRUN/UNDERRUN DETECTED**: When this bit is set, it indicates that a data transfer between the host and the buffer memory did not function properly. This bit is set when the IOCHRDY* Signal (Pin 48/97) is asserted low, and the rising (trailing) edge of the IOW* Signal (Pin 52/1) or the IOR* Signal (Pin 51/100) was detected. This bit is reset when the host writes to the Command Register.
Bit 2	R	**PC SELECTION DETECTED**: In the XT Mode, this bit is set when the host writes to Port 2. In PC AT Mode, this bit is set when the host writes to the AT Command Register (47H/67H).

5.11 Register 50H: PC Interrupt Status Register (Read Only) *(cont.)*

Bit 3	R	**AT STATUS READ DETECTED**: In AT Mode, this bit is set if the host reads the Primary Controller/Drive Status Register (1F7H or 177H) the first time following data transfers between the host and the FIFO. It is not set if the host reads the Alternate Controller/Drive Status Register (3F6H). In addition to the reset conditions described above, it is also cleared when the host writes to the Command Register.
Bit 4	R	**PC RESET DETECTED**: This bit is set by assertion of the Host Reset Signal HRST*/HRST (Pin 53/2) or a host-programmed reset, i.e., when the XT Host writes to Port 1 or the AT Host sets the RESET Bit (AT Host Fixed Disk Register, Bit 2). This bit is set for the duration of the host reset condition.
Bit 5	—	Reserved.
Bit 6	R	**BUFFER PARITY ERROR DETECTED:** This bit is set when a DRAM buffer parity error has been detected by the CL-SH366.
Bit 7	—	Reserved.

5.12 Register 51H: PC Interrupt Enable Register (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83).

Bit 0	R/W	**PC TRANSFER DONE ENABLE**: When this bit is set, it will cause the INT* Signal (Pin 4/53) to be asserted low, when the PC Transfer Done Bit (Register 50H, Bit 0 and Register 53H, Bit 2) is set.
Bit 1	R/W	**PC TRANSFER OVERRUN/UNDERRUN ENABLE**: When this bit is set, it will cause the INT* Signal (Pin 4/53) to be asserted low, when the PC Transfer Overrun/Underrun Detected Bit (Register 50H, Bit 1) is set.
Bit 2	R/W	**PC SELECTION ENABLE**: When this bit is set, it will cause the INT* Signal (Pin 4/53) to be asserted low when the PC Selection Detected Bit (Register 50H, Bit 2) is set.
Bit 3	R/W	**AT STATUS READ ENABLE**: When this bit is set, it will cause the INT* Signal (Pin 4/53) to be asserted low, when the AT Status Read Detected Bit (Register 50H, Bit 3) is set.
Bit 4	R/W	**PC RESET ENABLE:** When this bit is set, it will cause the INT* Signal (Pin 4/53) to be asserted low, when the PC Reset Detected Bit (Register 50H, Bit 4) is set.

5.12 Register 51H: PC Interrupt Enable Register (Read/Write) *(cont.)*

Bit 5	—	Reserved.
Bit 6	R/W	**BUFFER PARITY ERROR DETECTED:** When this bit is set, it will cause the INT* Signal (Pin 4/53) to be asserted low, when the Buffer Parity Error Detected Bit (Register 50H, Bit 6) is set.
Bit 7	—	Reserved.

5.13 Register 52H: Miscellaneous Control/Status Register (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83).

Bit 0	R/W	**MOE* DISABLE**: When this bit is set, the buffer memory MOE* Signal (Pin 1/50) is disabled from being asserted low. This is intended to support switch reads (via 70H) on the buffer memory data bus. This bit is reset by the assertion of RST* (Pin 34/83). In DRAM Mode, if this bit is set, and the local microcontroller accesses the buffer, the DRAM controller will not perform a buffer access. This will allow the local microcontroller to read the switch settings from the buffer memory data bus.
Bit 1	R/W	**MASTER/SLAVE MODE ENABLE**: When this bit is set, it enables the ability to daisy-chain two separate XT or AT interfaces together, one configured as master and the other as slave.
Bit 2	R/W	**MASTER/SLAVE SELECT**: When Bit 1 of Register 52 is set, this bit configures the CL-SH366 as master or slave. When this bit is reset, the CL-SH366 is configured as a master; when set, it is configured as a slave. The master responds to a Drive 0 select, and the slave responds to a Drive 1 select. For the PC AT, on a diagnostic command, both the master and slave respond; only the master is enabled to report status to the host.
Bit 3	R/W	**HCS1 MODE ENABLE**: (AT Mode only) When this bit is set, Pin 45/94 is the HCS1* Input; when this bit is reset, Pin 46/95 is the PC Address Line 9 Input.
Bit 4	R/W	**AT HOST FIXED DISK REGISTER DMAENB:** This bit is valid only in the PC AT Mode, and when the DMA Mode is enabled (i.e., Register 58H, Bits 3 and 7 are reset). When this bit is set, it allows Bit 0 of the AT Host Fixed Disk Register to control the enabling of the DMA channel. This bit should be set prior to enabling the DMA Mode (Register 58, Bit 3).
Bit 5	R	**AT DMAEN**: This bit reflects Bit 0 of the AT Host Fixed Disk Register. The Fixed Disk Register is a write-only host register that the local microcontroller can monitor through this read-only status bit.

5.13 Register 52H: Miscellaneous Control/Status Register (Read/Write) *(cont.)*

Bit 6	R/W	**BUFFER STOP POINTER DISABLE**: When set, this bit disables comparison of the PC Stop Pointer (Registers 5EH and 5FH), until Register 5EH is loaded.
Bit 7	R/W	**TEST MODE ENABLE**: This bit is reserved by Cirrus Logic for test purposes. The user should program this bit to a logical zero.

5.14 Register 53H: Buffer Transfer Control Register (Read/Write)

This register is reset by the assertion of HRST*/HRST (Pin 53/2), RST* (Pin 34/83), or Buffer Manager Reset (Register 59H, Bit 0), Bit 7 of this register is reset by RST* (Pin 34/83) only.

Bit 0	R/W	**DUAL-BUFFER CHIP ENABLE**: When this bit is set, it allows BA15/CE2*/NRZ0 (Pin 90/39) to operate as a second buffer chip enable when using two 32K SRAM buffer chips. This means CE1* (Pin 3/52) is connected to the first 32K chip enable and BA15/CE2*/NRZ0 (Pin 90/39) to the second 32K chip enable.
Bit 1	R/W	**DMA START**: When set, the CL-SH366 will start a DMA transfer; the direction of the transfer is programmed in the PC R/W* Transfer Direction (Bit 3).
Bit 2	R	**PC TRANSFER DONE**: When this bit is set, it indicates the completion of a host transfer (i.e., the PC Stop Pointer, Registers 5EH-5FH, is equal to the Host Address Pointer — Registers 5AH and 5BH). After this bit is set, the Host Address Pointer will read one byte more than the value of the PC Stop Pointer. This bit is the same as Register 50H, Bit 0.
Bit 3	R/W	**PC R/W* TRANSFER DIRECTION**: This bit indicates the information-transfer direction on the PC bus in both the Programmed I/O (PIO) and DMA Transfer Modes. When this bit is reset, information is transferred to the CL-SH366.
Bit 4	R/W	**BUFFER/DISK R/W* TRANSFER DIRECTION**: This bit indicates the information-transfer direction to/from the Sector Formatter when a disk data transfer is initiated by the Sector Formatter. When this bit is set, the data-transfer direction is from the Sector Formatter to the buffer memory. When this bit is reset, the data-transfer direction is from the buffer memory to the Sector Formatter.
Bit 5	R/W	**BUFFER CHIP ENABLE**: When this bit is set, it asserts the CE* Signal (Pin 3/52 or 90/39) until this bit is reset. This bit is used to enable buffer memory for Read/Write Operations. This bit may be set when both the disk and host are idle, and a Read 70H and Write 70H Operation is performed.
Bit 6	R/W	**BUFFER OUTPUT ENABLE**: When this bit is set, it asserts the MOE* Signal (Pin 1/50). This bit is used for a Read 70 Operation to improve the buffer access time for fast processors.

5.14 Register 53H: Buffer Transfer Control Register (Read/Write) *(cont.)*

Bit 7	R/W	**DEMAND MODE DMA ENABLE**: This bit, when set, enables the DMA logic to assert DREQ (Pin 49/98) for the length of the transfer or de-assert DREQ for underrun/overrun control. In this mode, multiple transfers can occur without arbitrating the host bus. This bit is reset by RST* (Pin 34/83) only.

5.15 Register S53H (Shadow 53H): Buffer Mode Control Register (Read/Write)

This register is reset by the assertion of HRST*/HRST (Pin 53/2), RST* (Pin 34/83), or Buffer Manager Reset (Register 59H, Bit 0). This register can only be accessed after the Shadow Register Select Bit (Register 48H, Bit 1) has been set.

Bit 0	R/W	**WCS OVERLAY ENABLE**: When this bit is reset, the Buffer Manager Block is mapped to Addresses 20H-3EH, and the WCS is mapped to Addresses A0H-BEH. When this bit is set, the decode of the address space from 20H-3EH is disabled, and this block of addresses is overlaid onto the WCS at Addresses A0H-BEH.
Bit 1	R/W	**WCS CONTROL FIELD SELECT**: When the WCS Overlay Enable Bit (Register S53H, Bit 0) is set, and this bit is reset, the Buffer Manager block is mapped to the A0H-BEH address space. When the WCS Overlay Enable Bit (Register S53H, Bit 0) is set, and this bit is set, the WCS Control Field is mapped to the A0H-BEH address space.

Bit 1	Bit 0	Mapping Addresses
X	0	Buffer Manager Block is at 20H-3EH; WCS is at A0H-BEH.
0	1	Buffer Manager Block is at A0H-BEH; Addresses 20H-3EH are disabled. WCS is not accessible.
1	1	WCS is at A0H-BEH; Addresses 20H-3EH are disabled. Buffer Manager Block is not accessible (default after initialization).

Bit 2	R/W	**BUFFER PARITY ENABLE:** When this bit is set, the buffer data parity function is enabled.
Bit 3	R/W	**DRAM REFRESH DISABLE:** When this bit is set, the automatic DRAM refresh is disabled. This feature can be used to reduce power consumption when the contents of the DRAM buffer memory can be discarded.
Bits 7- 4	—	Reserved.

5.16 Register 54H: Buffer Size/Segment Address Register (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83).

Bits 7-0	R/W	**For an SRAM buffer**, this register can operate in two modes. In Fixed Mode, the buffer can be divided into 4K, 8K, 16K, 32K, 64K or 128K segments. The smallest segment size with pointer wrap-around is 4K. For example, with an attached buffer size of 32K and segment sizes of 4K, this would create eight 4K segments: 0000-0FFFH, 1000-1FFFH, 2000-2FFFH, 3000-3FFFH, 4000-4FFFH, 5000-5FFFH, 6000-6FFFH, 7000-7FFFH. When operating in this mode, the Buffer Start Address Registers (9FH-BFH or 30H/B0H-32H/B2H) and the Buffer End Address Registers (DFH-FFH or 34H/B4H-36H/B6H) are loaded with the physical size of the attached static RAM buffer. Each segment can be accessed by setting the upper four bits of the HAP and DAP to the desired segment address. In this configuration, once the address pointer (HAP or DAP) reaches X1FFFH, the next address will roll over to X1000H. In the second mode, the CL-SH366 provides the ability to generate a variable segment within the buffer memory by providing Buffer Start Address Registers (9FH-BFH or 30H/B0H-32H/B2H) and Buffer End Address Registers (DFH-FFH or 34H/B4H-36H/B6H). By loading the Buffer Start Address Register (9FH-BFH or 30H/B0H-32H/B2H) with the starting segment address and the Buffer End Address Register (DFH-FFH or 34H/B4H-36H/B6H) with the ending segment address, whenever the Disk Address Pointer (DAP — Registers 5AH-5BH or 20H/A0H-22H/A2H) or Host Address Pointer (HAP — Registers 5CH-5DH or 24H/A4H-26H/A6H) are equal to the Buffer End Address Register, they are reloaded with the Buffer Start Address Register value. When operating in this mode, the Buffer Size/Segment Address Register (Register 54H) must be set to the physical size of the attached static RAM buffer. **For a DRAM buffer**, the register functions the same as above with the following exceptions: In Fixed Mode, the minimum segment size is 8K, and the maximum buffer size is 4 Mbyte.

For an AT interface auto-command sequence, the HAP pointer will be set to 0000H, regardless of the previous segment address.

The following table defines the allowable values that can be programmed into Register 54H[1].

SRAM	DRAM
00H = 128K bytes	00H = 8K bytes
01H = Reserved	01H = 16K bytes
03H = 1K bytes[2]	03H = 32K bytes
07H = 2K bytes[2]	07H = 64K bytes
0FH = 4K bytes	0FH = 128K bytes
1FH = 8K bytes	1FH = 256K bytes
3FH = 16K bytes	3FH = 512K bytes
7FH = 32K bytes	7FH = 1M bytes
FFH = 64K bytes	FFH = 4M bytes

NOTES: [1]This register cannot be modified while the buffer is being accessed.

[2]These values are possible, but the pointers will not wrap correctly with either a 1K or 2K value. For correct pointer wrapping, the minimum segment size is 4K.

Registers 55H-57H are XT/AT Registers. Please refer to Section 7, *Local Microcontroller-Host Interface.*

5.17 Register 58H: PC Mode Control Register (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83).

Bits 1-0	R/W	**PC WAIT STATE**: These bits specify the number of buffer memory cycles for which IOCHRDY* (Pin 48/97) will be asserted low for programmed I/O (PIO) transfers. These bits are reset by assertion of RST* (Pin 34/83). 00 = no buffer memory cycles 01 = 1-2 buffer memory cycle 10 = 2-3 buffer memory cycles 11 = 3-4 buffer memory cycles
Bit 2	R/W	**AUTO-WAIT-STATE GENERATION ENABLE**: When this bit is set, wait-states will be generated automatically for programmed I/O transfers between the host and the buffer memory when the CL-SH366 is not ready to transfer data. When auto-wait-state generation is enabled, IOCHRDY* (Pin 48/97) is negated when both the CL-SH366 is ready and the programmed number of wait states in the bus cycle specified by Register 58H, Bits 1-0, are generated. This bit is reset by assertion of RST* (Pin 34/83).
Bit 3	R/W	**PIO or DMA SELECT**: (PC/AT Mode only) When this bit is set, Programmed I/O(PIO) is selected. When the AT DMA Mode is selected, the PC can handshake the DREQ Line with either a HCS0* or a DACK*. By setting Register 52H, Bit 4, in AT DMA Mode, the PC can directly control the DMAEN of the DMA channel through Bit 0 of the Fixed Disk Register; (the local microcontroller can monitor this bit through Register 52H, Bit 5). This bit is set by assertion of RST* (Pin 34/83).
Bit 4	R/W	**ENABLE AUTO-INTERRUPT UPON START OF PC DATA TRANSFER**: (PC AT Mode only) When this bit is set, the CL-SH366 generates an interrupt to the host when the local microcontroller initiates a host data transfer. This is done by setting the Start DMA Bit (Register 53H, Bit 1) in the Buffer Transfer Control (Register 53H); or, if this bit is set, it is done by writing to Register 5EH. This bit is set by assertion of RST* (Pin 34/83).
Bit 5	R/W	**DISABLE AUTO-COMMAND EXECUTION**: When this bit is set, it disables automatic execution of write, write long, write buffer, and format commands. When this bit is set, it also disables the automatic transfer of ECC bytes for read/write long commands. This bit is reset by assertion of RST* (Pin 34/83).
Bit 6	R/W	**8-/16-BIT DATA**: (PC/AT Mode only) When this is set, it selects 16-bit data transfer to/from the PC. This bit is set by the assertion of RST* (Pin 34/83).

5.17 Register 58H: PC Mode Control Register (Read/Write) *(cont.)*

Bit 7	R/W	**XT/AT SELECT**: This bit controls which host interface is active, XT or AT. When this bit is set, the PC XT Mode is selected. This bit is reset by the assertion of RST* (Pin 34/83).

5.18 Register 59H: Buffer Manager/PC Reset Control Register (Read/Write)

Bit 0	R/W	**BUFFER MANAGER RESET**: When this bit is set, it holds all registers associated with the Buffer Manager and PC functions in the Reset State until this bit is reset. Assertion of RST* (Pin 34/83) will also set this bit. A write to this register resets the Host Address Pointer (HAP) and the Disk Address Pointer (DAP), Registers 5AH-5DH and sets the PC Stop Pointer (Registers 5EH and 5FH), to a 01FFH.
	CAUTION:	**Any write to this register also resets the PC Interface Operation. Bit 0 must be reset to execute PC AT auto-commands.**
Bits 7-1	—	Reserved.

5.19 Register 20H/A0H: Disk Address Pointer Top Register (DAPT) (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83), or Buffer Manager Reset (Register 59H, Bit 0). This register can **only** be accessed after a write to Register S53H (Shadow 53H).

Bits 5-0	R/W	**DISK ADDRESS POINTER TOP:** These bits are the highest-order bits of the buffer memory address for disk and microcontroller accesses.
Bits 7-6	—	Reserved.

5.20 Register 5AH *or* 21H/A1H: Disk Address Pointer High Register (DAPH) (Read/Write)

Register 21H/A1H is the same as register 5AH. Register 21H/A1H can **only** be accessed after a write to Register S53H (Shadow 53H).

This register is reset by the assertion of RST* (Pin 34/83), or Buffer Manager Reset (Register 59H, Bit 0).

Bits 7-0	R/W	**DISK ADDRESS POINTER HIGH BYTE:** These bits are the high-order byte of the buffer memory address for disk and microcontroller accesses.

5.21 Register 5BH *or* 22H/A2H: Disk Address Pointer Low Register (DAPL) (Read/Write)

Register 22H/A2H is the same as Register 5BH. Register 22H/A2H can **only** be accessed after a write to Register S53H (Shadow 53H).

This register is reset by the assertion of RST* (Pin 34/83), or the Buffer Manager Reset (Register 59H, Bit 0).

Bits 7-0	R/W	**DISK ADDRESS POINTER LOW BYTE**: These bits are the low-order byte of the buffer memory address for disk and microcontroller accesses.

5.22 Register 24H/A4H: Host Address Pointer Top Register (HAPT) (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83), or Buffer Manager Reset (Register 59H, Bit 0). This register can **only** be accessed after a write to Register S53H (Shadow 53H).

Bits 5-0	R/W	**HOST ADDRESS POINTER TOP:** These bits are the highest-order bits of the buffer memory address for host accesses. These bits are loaded from the Auto-Write Address Pointer Top (Register 2CH/ACH, Bits 5-0) whenever an auto-command is issued.
Bits 7-6	—	Reserved.

5.23 Register 5CH *or* 25H/A5H: Host Address Pointer High Register (HAPH) (Read/Write)

Register 25H/A5H is the same as Register 5CH. Register 25H/A5H can **only** be accessed after a write to Register S53H (Shadow 53H).

This register is reset by the assertion of RST* (Pin 34/83), or Buffer Manager Reset (Register 59H, Bit 0).

Bits 7-0	R/W	**HOST ADDRESS POINTER HIGH BYTE:** These bits are the high-order byte of the buffer memory address for host accesses. These bits are loaded from the Auto-Write Address Pointer High (Register 2DH/ADH, Bits 7-1) whenever an auto-command is issued.

5.24 Register 5DH *or* 26H/A6H: Host Address Pointer Low Register (HAPL) (Read/Write)

Register 26H/A6H is the same as Register 5DH. Register 26H/A6H can **only** be accessed after a write to Register S53H (Shadow 53H).

This register is reset by the assertion of RST* (Pin 34/83), or the Buffer Manager Reset (Register 59H, Bit 0).

Bits 7-0	R/W	**HOST ADDRESS POINTER LOW BYTE**: These bits are the low-order byte of the buffer memory address for host accesses. This register is also reset when an auto-command is issued.

5.25 Register 28H/A8H: Stop Pointer Top Register (SPT) (Read/Write)

This register is set to 01H by the assertion of RST* (Pin 34/83), or Buffer Manager Reset (Register 59H, Bit 0). This register can **only** be accessed after a write to Register S53H (Shadow 53H).

Bits 5-0	R/W	**STOP POINTER TOP:** These bits are the highest-order bits of the Stop Pointer (SP) for host accesses. These bits are loaded from the Auto-Write Address Pointer Top (Register 2CH/ACH, Bits 5-0) whenever an auto-command is issued.
Bits 7-6	—	Reserved.

5.26 Register 5EH *or* 29H/A9H: Stop Pointer High Register (SPH) (Read/Write)

Register 29H/A9H is the same as Register 5EH. Register 29H/A9H can **only** be accessed after a write to Register S53H (Shadow 53H).

This register is set to 01H by the assertion of RST* (Pin 34/83), or the Buffer Manager Reset (Register 59H, Bit 0).

Bits 7-0	R/W	**STOP POINTER HIGH BYTE**: These bits are the high-order byte of the Stop Pointer (SP). The Stop Pointer is used to detect the end of the host data transfer; it is compared with the Host Address Pointer (HAP — Register 5CH and 5DH). When they are equal, the Host Transfer Done Bit (Register 50H, Bit 0, Register 53H, Bit 2) is set and the transfer is halted. If a new value is programmed in this register, a new transfer cycle will begin again if the DMA Start Bit (Register 53H, Bit 1) is still set. These bits are loaded from the Auto-Write Address Pointer High (Register 2DH/ADH, Bits 5-0) whenever an auto-command is issued.

5.27 Register 5FH *or* 2AH/AAH: Stop Pointer Low Register (SPL) (Read/Write)

Register 2AH/AAH is the same as Register 5FH. Register 2AH/AAH can **only** be accessed after a write to Register S53H (Shadow 53H).

This register is set to FFH by the assertion of RST* (Pin 34/83), or the Buffer Manager Reset (Register 59H, Bit 0).

Bits 7-0	R/W	**STOP POINTER LOW BYTE**: These bits are the low-order byte of the Stop Pointer (SP). The Stop Pointer is used to detect the end of the host data transfer; it is compared with the Host Address Pointer (HAP — Register 5CH and 5DH). This register is also set to FFH when one of the auto-commands is issued.

5.28 Register 2CH/ACH: Auto-Write Address Pointer Top Register (AWPT) (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83), or Buffer Manager Reset (Register 59H, Bit 0). This register can **only** be accessed after a write to Register S53H (Shadow 53H).

Bits 5-0	R/W	**AUTO-WRITE ADDRESS POINTER TOP:** These bits are automatically loaded into both the Stop Pointer Top Register (Register 28H/A8H), and the Host Address Pointer Top Register (Register 24H/A4H) whenever an auto-command is issued.
Bits 7-6	—	Reserved.

5.29 Register 2DH/ADH: Auto-Write Address Pointer High Register (AWPH) (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83), or Buffer Manager Reset (Register 59H, Bit 0). This register can **only** be accessed after a write to Register S53H (Shadow 53H).

Bits 5-0	R/W	**AUTO-WRITE ADDRESS POINTER HIGH:** These bits are automatically loaded into both the Stop Pointer High Register (Register 5EH *or* 29H/A9H), and the Host Address Pointer High Register (Register 5CH *or* 25H/A5H) whenever an auto-command is issued.
Bits 7-6	—	Reserved.

5.30 Register 27H/A7H: Buffer Mode Control/Parity Error Status Register (BMC) (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83).

Bit 0	R/W	**DRAM/SRAM*:** When this bit is set, the DRAM Mode is selected. When this bit is reset, the SRAM Mode is selected.
Bits 2-1	R/W	**BUFFER SIZE SELECT**: If Bit 0 is set, Bits 2-1 are decoded as: **Bit 2** **Bit 1** **Description** 0 0 64K bytes DRAM 0 1 256K bytes/512K bytes DRAM 1 0 1 Mbyte DRAM 1 1 4 Mbytes DRAM If Bit 0 is reset, Bits 2-1 are decoded as: **Bit 2** **Bit 1** **Description** 0 X Less than 128K bytes SRAM 1 0 128K bytes SRAM 1 1 Reserved
Bit 3	R/W	**DRAM BURST LENGTH SELECT**: When this bit is reset, a DRAM burst length of four is selected. When this bit is set, a DRAM burst length of eight is selected.
Bit 4	R	**LOCAL PARITY ERROR**: This bit is set if there is a parity error during a local CPU read of the buffer. This bit is reset when it is read.
Bit 5	R	**HOST PARITY ERROR**: This bit is set if there is a parity error during a host read of the buffer. This bit is reset when it is read.
Bit 6	R	**DISK/CORRECTOR PARITY ERROR**: This bit is set if there is a parity error during a disk or correction read of the buffer. This bit is reset when it is read.
Bit 7	—	Reserved; this bit is set to 0.

5.31 Register 2B/ABH: Buffer DRAM Timing Control Register (BTC) (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83).

Bits 1-0 R/W

RAS* LOW TIME: This field specifies the number of BCLK cycles in which the BA13/RAS* Signal is asserted for a Non-page Mode access cycle.

In Page Mode, this is the RAS* low time for the first memory cycle.

T = BCLK Period

Twrl =

Bit 1	Bit 0	
0	0	= 2T
0	1	= 3T
1	0	= 4T
1	1	= 5T

Bits 3-2 R/W

RAS* HIGH TIME: This field specifies the minimum number of BCLK cycles for which the BA13/RAS* Signal is deasserted (RAS* precharge time).

T = BCLK Period

Twrh =

Bit 3	Bit 2	
0	0	= T
0	1	= 2T
1	0	= 3T
1	1	= 4T

Bits 5-4 R/W

CAS* LOW TIME: This field specifies the minimum number of BCLK cycles for which the BA14/CAS* Signal is asserted in Page Mode.

T = BCLK Period

Twcl =

Bit 5	Bit 4	
0	0	= T
0	1	= 2T
1	0	= 3T
1	1	= 4T

Bits 7-6 R/W

CAS* HIGH TIME: This field specifies the minimum number of BCLK cycles for which the BA14/CAS* Signal is deasserted in Page Mode.

T = BCLK Period

Twch =

Bit 7	Bit 6	
0	0	= T
0	1	= 2T
1	0	= 3T
1	1	= 4T

5.32 Register 2F/AFH: DRAM Refresh Period Register (DRP) (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83).

Bits 7-0	R/W	**DRAM REFRESH PERIOD:** This register holds the most significant eight bits of the 9-bit DRAM refresh period; the least-significant bit (inaccessible) is always set. The refresh period is specified in BCLK cycles.

5.33 Register 68H: Scheduled Buffer Data Register (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83), or Buffer Manager Reset (Register 59H, Bit 0).

Bits 7-0 R/W

SCHEDULED BUFFER DATA: This register is used to access the buffer memory (using the Disk Address Pointer), or to access switches on the buffer data bus (using MOE* Disable — Register 52H, Bit 0). Auto-incrementing of the DAP can be enabled by setting the Buffer Pointer Auto-increment Enable (Register 48, Bit 0). If this register is being used to write data to the buffer memory, the following algorithm must be used:

1. First, by program construction or by reading an active value on the Byte Ready Bit (Register 48H, Bit 7), verify that the scheduling mechanism is ready to accept a byte of data.
2. Next, if the DAP is not pointing to the desired buffer memory address, write the desired address to the DAP.
3. Write the byte to this register. Byte Ready will be reset until the byte has been written, and the DAP has been incremented (if auto-incrementing is enabled).
4. If another byte is desired, repeat this loop.

If this register is being used to read data from the buffer memory, the following algorithm must be used:

1. First, by program construction or by reading an active value on the Byte Ready Bit (Register 48H, Bit 7), verify that the scheduling mechanism is ready to read a byte of data.
2. Next, if the DAP is not pointing to the desired buffer memory address, write the desired address to the DAP.
3. Read this register. The data received will be data from a previous Scheduled Read or Scheduled Write Operation.
4. By program construction or by reading an active value on the Byte Ready Bit (Register 48H, Bit 7), verify that the scheduling mechanism is ready to read a byte of data; when it is, the desired byte is available to be read. Also, the DAP has been incremented (if auto-incrementing is enabled); therefore, a final read of this register will provide the desired data and trigger another scheduled read. If another byte is desired, repeat this loop; however, the next scheduled read will return the byte from the address pointed to by the incremented DAP (if auto-incrementing is enabled). If switches are used on the buffer data bus, the switches should be pulled up with 270K ohm resistors, and pulled down with 27K ohm resistors. To read the switches, set MOE* Disable, wait a time constant (about 30 µs), and then read this register twice. Note that the normal scheduling mechanism is still used.

5.34 Register 69H: Sector Status Register (Read Only)

This register is reset by the assertion of RST* (Pin 34/83).

Bit 0	R	**END OF TRACK**: This bit is set when the End of Track Bit in the ID Flag/MS Split Byte is set. It is reset after the read of this register.
Bit 1	R	**DEFECT**: This bit is set when Defect Bit in the ID Flag/MS Split Byte is set. It is reset after the read of this register.
Bit 2	R	**HOST RESET:** This bit shows the state of the HRST*/HRST (Pin 53/2) Signal.
Bit 3	R	**IDE/PCMCIA STATUS:** This bit shows the state of Bit 0 in the IDE/PCMCIA Control Register (Register 6FH — Write Only).
Bits 7-4	—	Reserved.

5.35 Register 69H: Increment Sector Count Register (Write Only)

Bits 7-0	—	A write to this register increments the Sector Count Register (Register 6BH) by 1. This function is always enabled, even if the Sequencer is stopped. The RRCLK (Pin 37/86) must be running in order for the Sector Count Register to increment.

5.36 Register 6AH: Sector Target Register (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83).

Bits 7-0	R/W	This register is loaded with the starting sector number to be read or written to/ from the disk. The Sequencer verifies the target sector by comparing the ID field from the disk with the internal ID values. The Sector Target Register is used as the source for the sector ID search. This register is incremented automatically, after the ECC is processed, for each sector.

5.37 Register 6BH: Sector Count Register (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83).

Bits 7-0	R/W	This register is loaded with the number of sectors to be processed. At the end of each sector, this register is decremented at the beginning of the 'process ECC time.' Given the proper branch conditions, when this register is equal to 00H, it informs the Sequencer of the last sector to be processed and will stop the Sequencer at the end of the current sector.

5.38 Register 6CH: React Branch Register (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83) or Register 71H, Bit 5.

Bits 4-0	R/W	**BRANCH ADDRESS**: Writing Bits 4-0 will cause the Sequencer RAM to jump to this address when a branch condition is programmed and met.
Bits 7-5	—	Reserved.

5.39 Register 6DH: Sector Remaining Counter MSB Register (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83).

Bits 3-0	R/W	This register is loaded with the length, in bytes, of the sector data field. For AT drives, the normal data length is 512 bytes.
Bits 7-4	—	Reserved.

5.40 Register 6EH: Sector Remaining Counter LSB Register (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83).

Bits 7-0	R/W	This register is loaded with the length, in bytes, of the sector data field. For an AT drive, the normal data length is 512 bytes.

5.41 Register 6FH: Revision Register (Read Only)

Bits 7-0	R	This register contains a revision code. For the CL-SH366, this register reads 00H (Rev. A), 01H (Rev. B), etc.

5.42 Register 6FH: IDE/PCMCIA Control Register (Write Only)

Bit 0	W	**IDE/PCMCIA SELECT**: When this bit is set, the polarity of the host interface signals HRST*/HRST (Pin 53/2) and HINT/HINT* (Pin 41/90) is configured to IDE Mode. When this bit is reset, the polarity of these signals is configured to PCMCIA-compatible Mode.
Bits 7-1	—	Reserved.

5.43 Register 70H: Unscheduled Buffer Access Register (Read/Write)

Bits 7-0	R/W	A Register 70H decode will internally bridge the buffer data bus and the multiplexed data address bus, allowing the microcontroller to access the buffer memory. The DAP Pointer is used to access the buffer. Read data from the buffer will also be latched into Register 4DH. MOE* Disable (Register 52H, Bit 0) allows the static value of the buffer data bus (switch read) to be accessed. To access the buffer through this register, there must be no PC or disk transfers in progress as this is an unscheduled access port. Also, the read or write of this register will automatically increment the Disk Address Pointer if the Buffer Pointer Auto-increment Enable Bit (Register 48H, Bit 0) is set.

5.44 Register 71H: ECC Control Register (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83) or Register 71H, Bit 5.

Bit 0	R/W	**HARDWARE CORRECTION ENABLE**: When set, this bit enables the on-the-fly correction circuitry. Resetting this bit saves the syndrome in the internal correction register, which can be read through Register 72H in 8-bit symbols.
Bit 1	R/W	**SYNDROME SHIFT CONTROL**: The function of this bit depends on Bit 0 of Register 71H. If Bit 0 is set, the internal on-the-fly correction circuitry is enabled, and Bit 1 is a don't care bit. If Bit 0 is reset, the ECC error can be corrected via firmware by reading the 10-byte syndrome from Register 72H in 8-bit segments. Setting Bit 1 will shift the syndrome by eight bits. This bit is cleared automatically after the shift is completed.
Bits 3-2	R/W	**HOST 32-/56-/88-BIT ECC SELECT**: (PC/AT Mode only) This bit is primarily used for long commands. These two bits set the transfer length for the ECC bytes with the host as follows:

Register 71H	Bit 3	Bit 2	
	0	0	32-Bit (4 bytes)
	0	1	88-Bit (11 bytes)
	1	0	56-Bit (7 bytes)
	1	1	—

NOTE: The formatter always uses 88-bit ECC. These bits are for host 'long' transfers only.

Bit 4	R/W	**ENABLE SECTOR BRANCH**: When set, this bit will cause the sector input to be OR'ed with the index so that the sequencer branch on index-or-sector command may be triggered by either index or sector.

5.44 Register 71H: ECC Control Register (Read/Write) *(cont.)*

Bit 5	R/W	**CHIP RESET**: Assertion of the RST* Pin will set this bit along with Bit 0 of Register 59H. If this bit is set by the microcontroller, then the Formatter Sequencer is stopped and only the following Formatter Registers are reset: 48H — Bits 2 and 6, 49-4DH, 71H, 74H, 75H, 78-7AH and 7D-7EH.
Bit 6	R/W	**INPUT2 (Pin 5/54) EDGE TRANSITION DIRECTION**: When this bit is reset, the edge of INPUT2 that causes a trigger is high-to-low; when this bit is set, it is low-to-high. This bit is reset by assertion of RST* only.
Bit 7	—	Reserved.

5.45 Register S71H (Shadow 71H): ECC Control Register (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83). This register can only be accessed after the Shadow Register Select Bit (Register 48H, Bit 1) has been set.

Bits 1-0	R/W	**ECC CORRECTION SPAN:** These bits select the ECC correction span when the ECC Hardware Correction Enable Bit (Register 71H, Bit 0) is set.

Bit 1	Bit 0	ECC Correction Span
0	0	ECC correction span of 11 bits
0	1	Reserved
1	0	Reserved
1	1	Reserved

Bit 2	—	Reserved.
Bit 3	R/W	**NRZ0 INTERFACE SELECT:** When this bit is reset, the one-bit NRZ interface is selected. When this bit is set, the two-bit NRZ interface is selected.
Bit 4	R/W	**NRZ0 SELECT:** In Two-bit NRZ Interface Mode (Register S71H, Bit 3 — the NRZ Interface Select — is set), the NRZ0 Signal is configured as follows: 1. In Non-mux Mode, ALE/NRZ0 (Pin 26/75) is configured as the NRZ0 Signal. 2. In Mux Mode, if this bit is reset, BA15/CE2*/NRZ0 (Pin 90/39) is configured as NRZ0. In Mux Mode, if this bit is set, A0/NRZ0 (Pin 16/65) is configured as the NRZ0 Signal.
Bits 7-5	—	Reserved.

5.46 Register 72H: Syndrome Shift Register (Read Only)

This register is reset by the assertion of RST* (Pin 34/83).

Bits 7-0	R	The data read from this register is only valid when the Hardware Correction Enable Bit (Register 71H, Bit 0) is reset. Use this register in conjunction with Register 71H, Bit 1 (Syndrome Shift Control), after a Data Read Operation and an ECC error. The 10-byte syndrome can be read by the local microcontroller, through this register, to attempt a firmware correction.

5.47 Register 72H: Correction Done Reset Register (Write Only)

This register is reset by the assertion of RST* (Pin 34/83).

Bits 7-0	W	A write to this register resets the Correction Done Status Bit in Register 79H, Bit 4.

5.48 Register 73H: Auto-Command 'Lock' Release Register (Write Only)

Bits 7-0	W	**AUTO-COMMAND 'LOCK' RELEASE**: A write to this register unlocks the Buffer Manager Registers. The registers were locked when the host issued an auto-command. Register 4FH, Bit 5 (Local Interface Power Down) is locked until a write to Register 73H. The other affected registers are 53H, 5CH-5FH, 68H and 70H.

5.49 Register 74H: Offset Count Register (MSB) (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83) or Register 71H, Bit 5.

Bits 7-0	R/W	This register contains the high-order byte of the maximum number of shifts to be performed by the hardware, before the error pattern is found. The Offset Registers (Registers 74H and 75H) are to be set to [(number of data bits - 8)/2] +1. For 512-byte sectors, the offset value is 07FDH.

5.50 Register 75H: Offset Count Register (LSB) (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83) or Register 71H, Bit 5.

Bits 7-0	R/W	This register contains the low-order byte of the maximum number of shifts to be performed by the hardware before the error pattern is found.

5.51 Register 76H: Synchronization Byte-Count Limit Register (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83).

Bits 7-0	R/W	This register holds the byte-count limit for the NRZ read data synchronization timer. This value is programmable from 0 to 255. Refer to the description of the Count/Start Synchronization Timer/Two Index Timer Bit (Bit 5 of the WCS Count Field). When the timer has been activated, the value is decremented for each byte time that passes. If the value reaches zero, the Synchronization Time Out Error Bit (Register 48H, Bit 2) is set. Reading this register provides the running count (if the timer is active), or the programmed limit if the timer is inactive.

5.52 Register 77H: Formatter Mode Selection Register (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83).

Bit 0	R/W	**ENABLE LOCAL MICROCONTROLLER HOST AND DISK INTERRUPTS**: This bit, when set, configures Host Interrupts (Register 50H) to the HOSTINT* (Pin 5/54) and Disk Interrupts (Register 7DH) to the INT*/DISKINT* (Pin 4/53). When this bit is reset, all interrupts affect the INT*/DISKINT* (Pin 4/53).
Bit 1	R/W	**PC REGISTER FILE ACCESS ENABLE**: When this bit is set, it allows the PC Registers to be accessed by the local microcontroller. The address space is specified by Bit 2. When this bit is reset, Addresses 40H-47H and 60H-67H are available for external system use.
Bit 2	R/W	**PC REGISTER FILE DECODE SELECT**: When this bit is set (and Bit 1 is set), the PC Register File Address is 40H-47H. (Addresses 60H-67H are available for external system use.) When this bit is reset (and Bit 1 is set), the PC Register File Address is 60H-67H (Addresses 40H-47H are available for external system use).
Bit 3	R/W	**LOCAL INTERRUPT ENABLE**: When this bit is set to a logical 1, it enables local interrupt capability. The individual sources of interrupt can still be disabled by the Interrupt Enable Registers (Registers 51H and 7EH).
Bit 4	R/W	**LOCAL INTERRUPT PIN PULL-UP DISABLE**: When set, this bit disables the pull-up on the output pin, leaving an open-drain output. This is intended to support multiple-interrupt sources.
Bit 5	R/W	**PROGRAMMED CONTROL INDEX**: When this bit is set, it simulates an active index condition. This bit can be used in place of INDEX (Pin 32/81).

5.52 Register 77H: Formatter Mode Selection Register (Read/Write) *(cont.)*

Bit 6	R/W	**SEQUENCER OUTPUT ENABLE**: When set, this bit activates the output enable of the Sequencer Input/Output Pin to configure it as an output. The value actually driven will be specified by the Current Sequencer Word Control Field, Bit 2.
Bit 7	R/W	**HARD/SOFT* SECTOR MODE CONTROL**: When reset, this bit selects the Soft Sector Mode. When set, this bit selects the Hard Sector Mode. The Soft Sector Mode selects the WAM*/AMD* functionality on the WAM*/AMD*/SECTOR (Pin 33/82). Note that the sector circuity, Sector Past (Register 7AH, Bit 1), and sector branch conditions, are now passed to the Address Mark Detect Signal. The Hard Sector Mode selects the sector functionality on the WAM*/ AMD*/ SECTOR (Pin 33/82). Note that the sector circuitry, Sector Past (Register 7AH, Bit 1), and Sector Branch Conditions, are now passed to the Sector Signal.

5.53 Register 78H: Branch Address Register (Write Only)

This register is reset by the assertion of RST* (Pin 34/83) or Register 71H, Bit 5.

Bits 4-0	W	**BRANCH ADDRESS**: Writing Bits 4-0 will cause the Sequencer RAM to jump to this address when a branch condition is programmed and met.
Bits 7-5	—	Reserved.

5.54 Register 79H: Formatter Status Register (Read Only)

This register is reset by the assertion of RST* (Pin 34/83) or Register 71H, Bit 5.

Bit 0	R	**COMPARE EQUAL**: This bit is set when the result of the compare operation is equal. The comparison is done between the Read Data and either the Buffer Memory Data or the WCS Data Field, on all bytes where comparison was enabled in the Compare Enable Bit (Bit 1) of the WCS Control Field. Compare Equal is not valid until the Sequencer is in the ECC field.
Bit 1	R	**ID CRC ERROR**: After the last bit of CRC data is read for the ID field, this bit will be set if all bits in the CRC are not zero. The reset conditions for this bit are: Register 71H, Bit 5; a write to Register 79H, and the beginning of new read/write.
Bit 2	R	**ECC ERROR**: This bit will be set after the last ECC Data Bit is read if there is a non-zero ECC syndrome indicating a data error. It will be reset when the next sequencer read/write is started. The reset conditions for this bit are: Register 71H, Bit 5; a write to Register 79H, and on the beginning of a new read/write.
Bit 3	R	**UNCORRECTABLE ERROR FOUND**: This bit is set when an uncorrectable error is found after an on-the-fly hardware correction process. (Register 71H, Bit 0, must be set, i.e., Hardware Correction is enabled). If Hardware Correction is disabled (Register 71H, Bit 0 is reset), then this bit is set following a read of the last ECC Data Bit, when there is a non-zero ECC syndrome. The reset conditions for this bit are: Register 71H, Bit 5, a write to Register 79H, the load of the Correction Register, and a host-issued auto-command (AT Mode only) if the Hardware Correction Enable Bit (Register 71H, Bit 0) is set. If the Hardware Correction Enable Bit (Register 71H, Bit 0) is reset, this bit is reset when Register 71H, Bit 5, is set and following a write to Register 79H.
Bit 4	R	**CORRECTION DONE**: This bit is set when a correctable error has been found and the read/write modification to correct the data in the buffer has been completed. The reset conditions for this bit are: Register 71H, Bit 5, the load of the Correction Register and a write to Register 72H.
Bit 5	R	**SEQUENCER STOPPED**: When this bit is set, it indicates that the Sequencer is stopped, i.e., the Sequencer RAM is at Address 1FH. The ECC contents have not been reset, and the RG (Pin 35/84) and WG (Pin 36/85) Signals are reset. This bit is reset by assertion of RST* (Pin 34/83) or Register 71H, Bit 5.
Bit 6	R	**BRANCH ACTIVE**: This bit is set whenever a branch condition is met. This bit will be reset after a read of this register.
Bit 7	R	**DATA TRANSFER STATUS:** This bit indicates the status of the Data Transfer Bit (WCS Control Field, Bit 0). It is set whenever data is being transferred between the buffer memory and the disk, regardless of the state of the Suppress Transfer Bit (Register 7AH, Bit 5). It is reset when the Sequencer stops.

5.55 Register 79H: Sequencer Start Register (Write Only)

This register is reset by the assertion of RST* (Pin 34/83) or Register 71H, Bit 5.

Bits 4-0	W	**START ADDRESS**: A write to this register will start the Sequencer at the latched address.
Bits 7-5	—	Reserved.

5.56 Register 7AH: Operation Control Register (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83) or Register 71H, Bit 5.

Bit 0	R	**INDEX PAST**: The index pulse from the device has been leading-edge-detected since the last time this register was read. Reading of this bit will reset the bit even while the index pulse is present. (Read only).
Bit 1	R	**SECTOR PAST**: The sector pulse has been leading-edge-detected from the device since the last read of this register. Reading of this bit will reset the bit even while the sector pulse is present. In a Soft Sector Mode configuration, the Address Mark Signal should be at least one byte wide to detect an edge. (Read only).
Bit 2	R	**AUTO-COMMAND STATUS**: (PC AT Mode only) This bit is set when an auto-command is received and the PC R/W* Transfer Direction (Register 53H, Bit 3) is deasserted. This bit is reset when a write to Register 73H is issued to unlock the Buffer Manager Registers, and for transfers between the Formatter and the buffer sections.
Bit 3	R	**SYNC DETECT**: This bit is set during a Disk Read Operation when the internal serializer/deserializer has been synchronized with the incoming NRZ data, and the data matches the preprogrammed sync character in Register 7CH. This bit is cleared on the falling (trailing) edge of the RG Signal (Pin 35/84). (Read only).
Bit 4	R	**WCS BYTE READY**: When this bit is set, it indicates that a scheduled WCS access is completed and that another scheduled WCS access may be started.
Bit 5	R/W	**SUPPRESS TRANSFER**: When this bit is set, serialized or deserialized data will not be read or written to the buffer (disabling the buffer access mechanism of data transfer — Current Sequencer Word Control Field, Bit 0). During a Write Operation, the NRZ data that is output will consist of the contents of the WCS Data Field. During RG, the incoming data will be compared with the contents of the WCS Data Field, ECC will be verified, but no data will be transferred to the buffer memory.

5.56 Register 7AH: Operation Control Register (Read/Write) *(cont.)*

Bit 6	R/W	**SCHEDULED WCS ACCESS/ ENABLE**: When this bit is set, the microcontroller uses the WCS Byte Ready Bit (Register 7AH, Bit 4) to access the WCS correctly.
Bit 7	R/W	**INHIBIT DATA FIELD CARRY**: When this bit is set, the carry/load of the WCS Count Field for the data transfer will be inhibited. Also, the Sector Size Counter will be reinitialized from the Sector Size Register (Register 4EH); this feature is used for large data fields. This bit is reset by the assertion of RST* (Pin 34/83) or Register 71H, Bit 5.

5.57 Register 7BH: WAM Control Register (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83).

Bits 7-0	R/W	**WRITE ADDRESS MARK CONTROL**: In Soft Sector Mode, the WAM*/AMD* Signal (Pin 33/82) will be asserted low for each bit-cell time corresponding to the bits set in this register during a Write Address Mark Operation. Output at the WAM*/AMD*/SECTOR Signal (Pin 33/82) is shifted two bits toward the MSB at the output. In Hard Sector Mode, the pin will not be asserted.

5.58 Register 7CH: AMD Control Register (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83).

Bits 7-0	R/W	**ADDRESS MARK DETECT CONTROL**: (Synchronization Byte Pattern) This register is to be compared with NRZ read data when the RG Signal (Pin 35/84) and, if in Soft Sector Mode, the WAM*/AMD*/SECTOR Signal (Pin 33/82) are asserted. A match between this register and the serial NRZ read data input will set the SYNC Detect Bit (Register 7AH, Bit 3), and will cause the bit ring to start at zero and NRZ read data to be gated into the ECC. Only those bits in this register which are enabled by the Clock Control (Register 7FH) will be used for comparison. This register is reset when the RST* (Pin 34/83) is asserted.

5.59 Register 7DH: Formatter Interrupt Status Register (Read Only)

This register is reset by the assertion of RST* (Pin 34/83), Register 71H, Bit 5, or a microcontroller read of this register.

Bit 0	R	**INDEX PAST**: This performs the same function as Register 7AH, Bit 0.
Bit 1	R	**SECTOR PAST**: This performs the same function as Register 7AH, Bit 1.
Bit 2	R	**INPUT DETECTED**: This bit will be set by the rising edge of the Input1/Output Signal (Pin 31/80). This bit will be cleared by the microcontroller reading this register.
Bit 3	R	**SEQUENCER STOPPED**: This performs the same function as Register 79H, Bit 5.
Bit 4	R	**ECC ERROR/UNCORRECTABLE ERROR**: If the Hardware Correction Enable Bit is set (Register 71H, Bit 0), this bit performs the same function as Register 79H, Bit 3. If the Hardware Correction Enable Bit is reset, this bit performs the same function as Register 79H, Bit 2.
Bit 5	R	**DATA TRANSFER STATUS**: This bit will be set by the rising (leading) edge of the Data Transfer Status Bit (Register 79H, Bit 7).
Bit 6	R	**SEQUENCER OUTPUT DETECTED**: This bit will be set by the rising (leading) edge of the Output Signal (Pin 31/80).
Bit 7	—	Not used; status indeterminate.

5.60 Register 7EH: Formatter Interrupt Enable Register (Read/Write)

This register is reset by the assertion of RST* (Pin 34/83).

Bit 0	R/W	**INDEX ENABLE**: When this bit is set, it will allow the INT* Signal to be asserted low when the Index Past Bit (Register 7DH, Bit 0) is set.
Bit 1	R/W	**SECTOR ENABLE**: When this bit is set, it will allow the INT* Signal to be asserted low when the Sector Past Bit (Register 7DH, Bit 1) is set.
Bit 2	R/W	**INPUT DETECTED ENABLE**: When this bit is set, it will allow the INT* Signal to be asserted low when the Input Detected Bit (Register 7DH, Bit 2) is set.
Bit 3	R/W	**SEQUENCER STOPPED ENABLE**: When this bit is set, it will allow the INT* Signal to be asserted low when the Sequencer Stopped Bit (Register 7DH, Bit 3) is set.
Bit 4	R/W	**ECC ERROR ENABLE**: When this bit is set, it will allow the INT* Signal to be asserted low when the ECC Error/Uncorrectable Error Bit (Register 7DH, Bit 4) is set.
Bit 5	R/W	**DATA TRANSFER DETECTED ENABLE**: When this bit is set, it will allow the INT* Signal to be asserted low when the Data Transfer Status Bit (Register 7DH, Bit 5) is set.
Bit 6	R/W	**SEQUENCER OUTPUT DETECTED ENABLE**: When this bit is set, it will allow the INT* Signal to be asserted low when the Sequencer Output Detected Bit (Register 7DH, Bit 6) is set.
Bit 7	—	Not used; status indeterminate.

5.61 Register 7FH: Clock Control Register (Write Only)

This register is reset by the assertion of RST* (Pin 34/83).

Bits 2-0	W	**SYNC COMPARE CONTROL**: These bits specify the number of bits to be used in the compare for the sync byte programmed in the AMD Control Register (Register 7CH). 000 = Only Bit 7 is compared 001 = Only Bits 7 and 6 are compared 010 = Only Bits 7, 6, and 5 are compared 011 = Only Bits 7, 6, 5, and 4 are compared 100 = Only Bits 7, 6, 5, 4, and 3 are compared 101 = Only Bits 7, 6, 5, 4, 3, and 2 are compared 110 = Only Bits 7, 6, 5, 4, 3, 2, and 1 are compared 111 = All bits are compared
Bits 4-3	R/W	**ECC CORRECTOR CLOCK SOURCE**: These two bits select the input clock to the ECC correction circuitry as follows: 00 = 1FCLK/DASP* (Pin 28/77) 01 = RRCLK (Pin 37/86) (default after RST*) 10 = BCLK (Pin 39/88) 11 = BCLK (Pin 39/88) divided by 2
Bit 5	W	**BUFFER CLOCK DISABLE**: The user ***must*** program this bit to be reset. When this bit is set, the internal clock will be disabled. It is used for test purposes only.
Bits 7-6	W	**BUFFER CLOCK DIVIDE**: These bits select the divider value that is applied to BCLK (Pin 39/88) to generate a buffer clock (BUFCLK) 00 = One buffer access cycle per four BCLK cycles 01 = One buffer access cycle per two BCLK cycles 10 = One buffer access cycle per one BCLK cycle 11 = One buffer access cycle per three BCLK cycles Bit 7 is set and Bit 6 is reset when the RST* Signal (Pin 34/83) is asserted.

5.62 Register 7FH: Top of Stack Register (Read Only)

Bits 7-0	R	**STACK**: A read of this register reads the last byte that was enabled [by the Stack Enable Bit (WCS Control Field, Bit 4)] onto the stack. The Address Pointer in 'ring' fashion moves around the 8-byte circular stack. As the byte is read, the Address Pointer moves to the previous location. The data during a read is never 'popped' from the stack; it is not lost or removed, and a continuous read of eight locations would bring one back around to the original location, reading the same data. If 10 bytes in a field were enabled to the stack, the last eight bytes would be captured, as the first two bytes would be overwritten. The first byte read from the stack would be the tenth byte enabled onto the stack. In reverse order, all of the last eight bytes could then be read continuously, in a circular manner.

6. SEQUENCER RAM FIELD DESCRIPTION

The Sequencer RAM (Addresses 80H-9EH, A0H-BEH, C0H-DEH, and E0H-FEH) may be written to or read from by the microcontroller. If the Scheduled WCS Access/WCS Access Bit (Register 7AH, Bit 6) is reset, then the microcontroller may access the WCS when there is no risk of the contents being accessed by the Sequencer. This is normally true only during data transfers or when the Sequencer is stopped. If the Scheduled WCS Access/WCS Access Bit (Register 7AH, Bit 6) is set, then the microcontroller may access the WCS in a scheduled format where there is no contention problem between microcontroller or Sequencer access. The Sequencer RAM is not initialized during any reset.

6.1 Next Address Field Register Description

6.1.1 Registers 80H-9EH Next Address Field (Read/Write)

Bits 4-0	**NEXT ADDRESS**: This is the address the Sequencer will go to after the down counter has reached zero and a branch has not been taken. There are 31 possible Next Address locations (00H-1EH). The stopped condition is established by Address 1FH.
Bits 7-5	**BRANCH COMMAND**: All branch commands are evaluated at the end of execution of the Current Sequencer Word.

NOTE: The branch address can be the Branch Address Register (78H) or the Data/Branch Field or the React Branch Register unless otherwise explicitly stated.

The following are branch commands when the Alternate Branch Command Select Bit (Bit 7) of the WCS Control Field is reset and all of the following conditions are true:

- The Process ECC/CRC Select Bit (Bit 6) of the WCS Count Field is set ***and***
- The Read Gate Signal (Pin 35/84) is asserted.

  000 = Continue — next address used
  001 = Stop on ECC error
  010 = Stop on non-equal compare
  011 = Stop on non-equal compare or ECC error
  100 = Branch on good ECC and equal compare
  101 = Branch on ECC error
  110 = Branch on non-equal compare
  111 = Branch on non-equal compare or ECC error

Branch Commands when the Alternate Branch Command Select Bit (Bit 7) of the WCS Control Field is reset, and if either of the following two conditions are true:

- The Process ECC/CRC Select Bit (Bit 6) of the Writable Control Store (WCS) Count Field is reset ***or***
- The Read Gate Signal (Pin 35/84) is deasserted.

  000 = Continue — next address used
  001 = Stop on INPUT1 (Pin 31/80) active
  010 = Stop on index or sector active
  011 = Stop on non-equal compare

6.1.1 Registers 80H-9EH Next Address Field (Read/Write) *(cont.)*

100 = Branch on Synchronization Time-out when the WCS Data Transfer is 0 (WCS Control Field, Bit 0).

101 = Branch on INPUT1/OUTPUT (Pin 31/80) active.

110 = Branch on index or sector active.

111 = Branch on non-equal compare.

The following are **branch commands** when the Alternate Branch Command Select Bit (Bit 7) of the WCS Control Field is set ***and all*** of the following conditions are true:

- The Process ECC/CRC Select Bit (Bit 6) of the WCS Count Field is set ***and***
- The Read Gate Signal (Pin 35/84) is asserted.

000 = No Branch.

001 = Stop on bad CRC.

Branch on good CRC, bad compare to retry (use the data field for the Branch Register).

On good CRC, good compare, and no Defect Bit (use the next address to process the data field).

Stop on good CRC, good compare, and the Defect Bit.

010 = Stop on bad CRC.

Branch on good CRC, bad compare to retry (use the data field for Branch Register).

On good CRC, good compare, and no Defect Bit (use the next address to process the data field).

Branch on good CRC, good compare, and the Defect Bit using React Branch Register (Register 6CH) to execute the alternate routine.

011 = Branch on bad CRC or bad compare to retry (use the data field for Branch Register).

On good CRC, good compare, and no Defect Bit (use the next address to process the data field).

Stop on good CRC, good compare, and Defect Bit.

100 = Branch on bad CRC or bad compare to retry (use the data field for the Branch Register).

On good CRC, good compare, and no Defect Bit (use the next address to process the data field).

Branch on good CRC, good compare, and Defect Bit using the React Branch Register (Register 6CH) to execute the alternate routine.

101 = Stop on Sector Count Register = 0.

Branch on the Sector Count Register not equal to zero and the End of Track Bit is reset. Increment the Sector Target Register and decrement the Sector Count Register (use the data field for the Branch Register).

Branch on the Sector Count Register not equal to zero and the End of Track Bit set. Reset the Sector Target Register to zero, and decrement the Sector Count Register (use the data field for the Branch Register).

Stop on the Uncorrectable ECC Error set for previous sector if the Hardware Correction Enable Bit (Register 71H, Bit 0) is set.

Stop on ECC Error if the Hardware Correction Enable Bit (Register 71H, Bit 0) is reset.

110 = No Branch.

111 = No Branch.

6.1.1 Registers 80H-9EH Next Address Field (Read/Write) *(cont.)*

The following are **branch commands** when the Alternate Branch Command Select Bit (Bit 7) of the WCS Control Field is set, and ***if either*** of the following two conditions are true:

- The Process ECC/CRC Select Bit (Bit 6) of the Writable Control Store (WCS) Count Field is reset ***or***
- The Read Gate Signal (Pin 35/84) is deasserted.

000 = No branch.

001 = If the Sector Remaining Counter Register (Registers 6DH-6EH) is not equal to zero, freeze ECC and read the next split of data (use the Next Address Field)

or

Branch on Sector Remaining Counter Register = 0 (use the Branch Register 78H).

010 = Sector Count Register = 0 use the Next Address Field.

Branch on the Sector Count Register not equal to zero and the End of Track Bit is reset (use the data field for Branch Register).

Branch on the Sector Count Register not equal to zero and the End of Track Bit set (use the data field for the Branch Register).

NOTE: If DRAM is used, and Buffer parity is disabled, the branch conditions above will be applied normally. If DRAM is used and Buffer parity is enabled, the previous branch code will also stop on a buffer-to-Formatter Parity Error.

011 = No branch.

100 = No branch.

101 = No branch.

110 = Branch on INPUT2/HOSTINT* (Pin 5/54) edge detected.

111 = No branch.

6.2 Count Field Register Description

6.2.1 Registers C0H-DEH Count Field (Read/Write)

Bits 3-0	**COUNT**: These bits are always used for the initial value of the Sequencer byte counter when a new state is entered. The counter is decremented on Bit Ring 7. When it reaches zero, a new instruction word will be accessed from the Formatter WCS.
Bit 4	**COUNT/SECTOR TARGET**: When the Data Transfer Bit of the Current Sequencer Word is set, this bit is a Count Bit (for an eight-bit Count Field). When the Data Transfer Bit of the Current Sequencer Word is reset, this bit indicates that the Sector Target Register should be used as the source of comparison with the incoming NRZ data in the Sector ID Byte to verify the correct sector target.
Bit 5	**COUNT/START SYNCHRONIZATION TIMER/TWO INDEX TIMER ARM**: When the Data Transfer Bit of the Current Sequencer Word is set, this is a Count Bit (for an 8-bit Count Field). **START SYNCHRONIZATION TIMER**: When this mode is selected, this bit resets and starts the Synchronization Timer. This counter is used to limit the amount of time that Format Sequencer will wait for synchronization with the NRZ Read Data. The Synchronization Byte Count Limit (Register 76H) holds a limit for the counter. If the count limit is exhausted, the current Read Operation will be aborted (the Format Sequencer stopped) and the Synchronization Time-out Error Bit (Register 4FH, Bit 0) will be set. This mode is selected when the Read Gate On Bit (Bits 6-5 of WCS Control Field) is set. **TWO INDEX TIMER**: This mode is selected when the Data Transfer Bit (WCS Control Field, Bit 0), and the Read Gate On Bit (WCS Control Field, Bit 6) are reset, and this bit is set. If Two Index pulses are detected after this circuit has been started, then the Format Sequencer will be stopped.
Bit 6	**COUNT/PROCESS ECC/CRC SELECT**: When the Data Transfer Bit of the Current Sequencer Word is set, this bit is a Count Bit (for an eight-bit Count Field). If, in the Current Sequencer Word, either the Read Gate On, or Write Gate On Bits are active, and the Data Transfer Bit is off, then this bit selects the CRC function. With this function active, setting this bit initializes the ECC function to the CRC polynomial; when this bit is cleared, the ECC function is initialized to the 88-bit ECC polynomial. When the Data Transfer Bit is off, and the Read Gate On, and Write Gate On Bits (WCS Control Field, Bits 6-5) are reset, this bit treats the incoming NRZ data (if Read Gate is active), or the outgoing NRZ data (if Write Gate is active) as an ECC field.
Bit 7	**COUNT/PROCESS AM/EXTENDED COUNT ENABLE:** When the Data Transfer Bit of the Current Sequencer Word is set, this is a Count Bit (for an 8-bit Count Field). When the Data Transfer Bit is off, and Read Gate or Write Gate is active, this bit will set the AM active latch internally to define the address mark at the beginning of the ID or data field. When the Data Transfer Bit is off, and the Read Gate or Write Gate are reset, this register becomes a 7-bit Count Field. The counter is decremented on Bit Ring 7. When it reaches zero, a new instruction word will be accessed from the Formatter WCS.

6.3 Data Field Register Description

6.3.1 Registers E0H-FEH Data Field (Read/Write)

Bits 7-0	**DATA**: This register is the source for all overhead bytes of data used by the device during Write Operations. During Read Operations, it is one of the operands to the comparison logic. When the Data Transfer Bit is on with the Write Gate asserted, the source for write data will be the external buffer. When Suppress Transfer is on with the Write Gate, the source for write data will be the content of this register. This register can also be the Branch Address source.

6.4 Control Field Register Description

6.4.1 Registers A0H-BEH Control Field (Read/Write)

Bit 0	**DATA TRANSFER/PREFETCH:** This bit is used for two functions: **DATA TRANSFER:** When this bit is set, the Count Field is used as an 8-bit counter. Each byte time that this bit is set, a byte of data will be accessed from the buffer if the Suppress Transfer Bit (Register 7AH, Bit 5) is reset. If Write Gate is active, then a byte of data is read from the buffer (if Suppress Transfer is reset) or from the Data Field (if Suppress Transfer is set); it is then serialized and sent to the NRZ Pin. During format, the ID field bytes can be written from the buffer instead of coming from the WCS Data Field (where they must be updated by the local microcontroller). This is accomplished by setting the Data Transfer Bit in the WCS Control Field. This will override the Suppress Transfer function for the ID field only. If Read Gate is active, then a byte of data is deserialized from the NRZ Pin and is written to the buffer (if Suppress Transfer is reset). **PREFETCH:** When this bit is set, the CL-SH366 starts prefetching data from the buffer memory. This mode is selected when **all** of the following conditions are true: 1) The Read Gate On code or the Write Gate On code is set. 2) The Buffer Disk R/W* Transfer Direction is reset, and 3) The Suppress Transfer Bit (Register7AH, Bit 5) is reset. For a disk write operation, PREFETCH must be set at the same time as the Write Gate On code. When performing a search operation, PREFETCH must be set at the same time as the Read Gate On code.
Bit 1	**COMPARE ENABLE**: When this bit is set and the RG Signal (Pin 35/84) is asserted, it will allow a comparison between Read Data and the WCS Data Field.
Bit 2	**OUTPUT**: This bit drives the Input/Output Signal (Pin 31/80) and is used to synchronize external logic functions to the state of the WCS.
Bit 3	**PROCESS SPLIT/FLAG**: If the Advanced Multisector/Multisector* Bit (Bit 0 of Register 4FH) is reset, this bit is used to indicate split or consecutive data field. If the Advanced Multisector/Multisector* Bit (Register 4FH, Bit 0) is set, this bit is used to specify the Flag/LS Split Count in the ID field.

6.4 Control Field Register Description *(cont.)*

6.4.1 Registers A0H-BEH Control Field (Read/Write)

Bit 4 **STACK ENABLE:** When active, read data is pushed on the 8-byte recirculating stack.

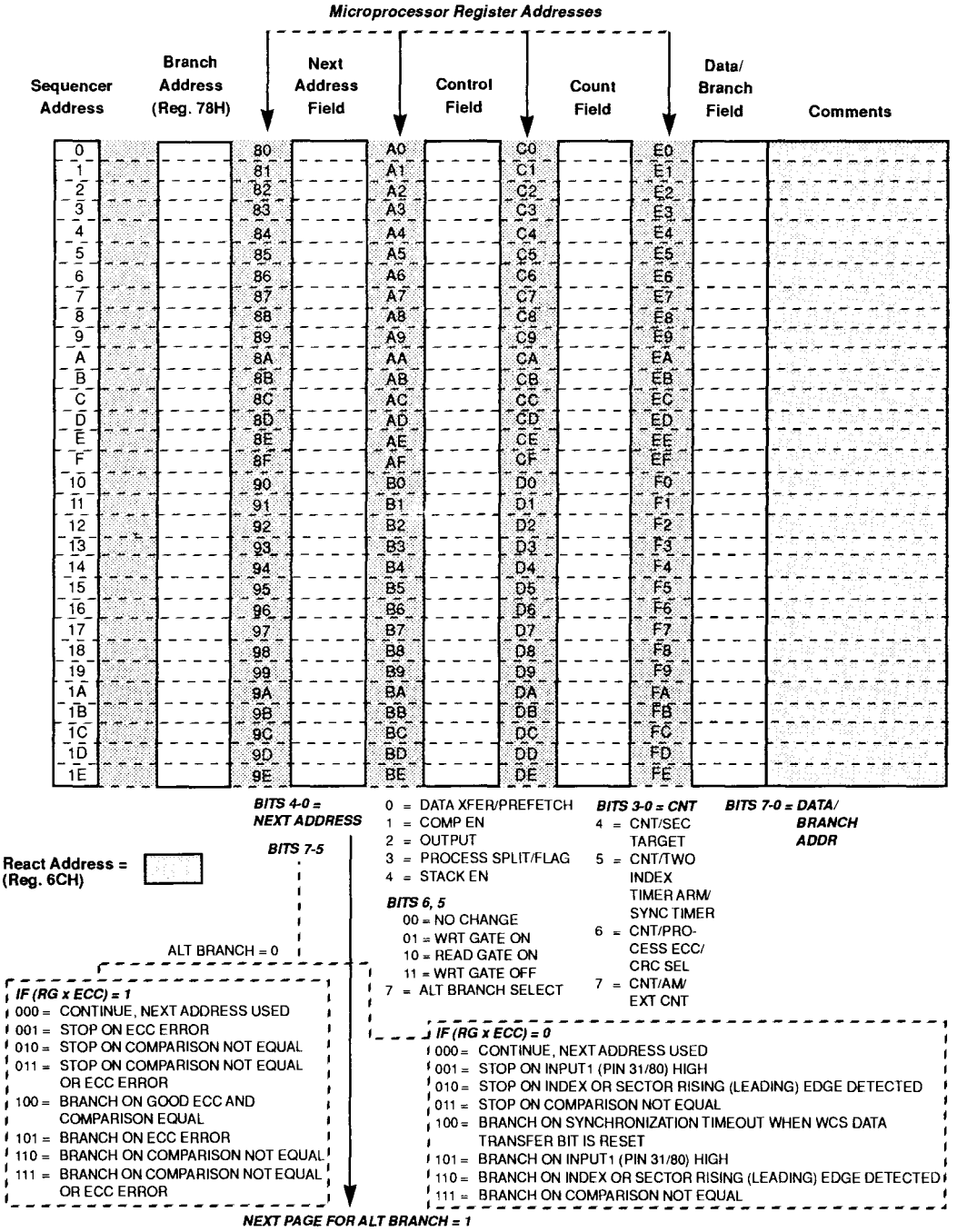
Bits 6-5 **CONTROL FIELD:** Bits 6-5 are encoded as follows:

Encoded Control Field Bits 6-5

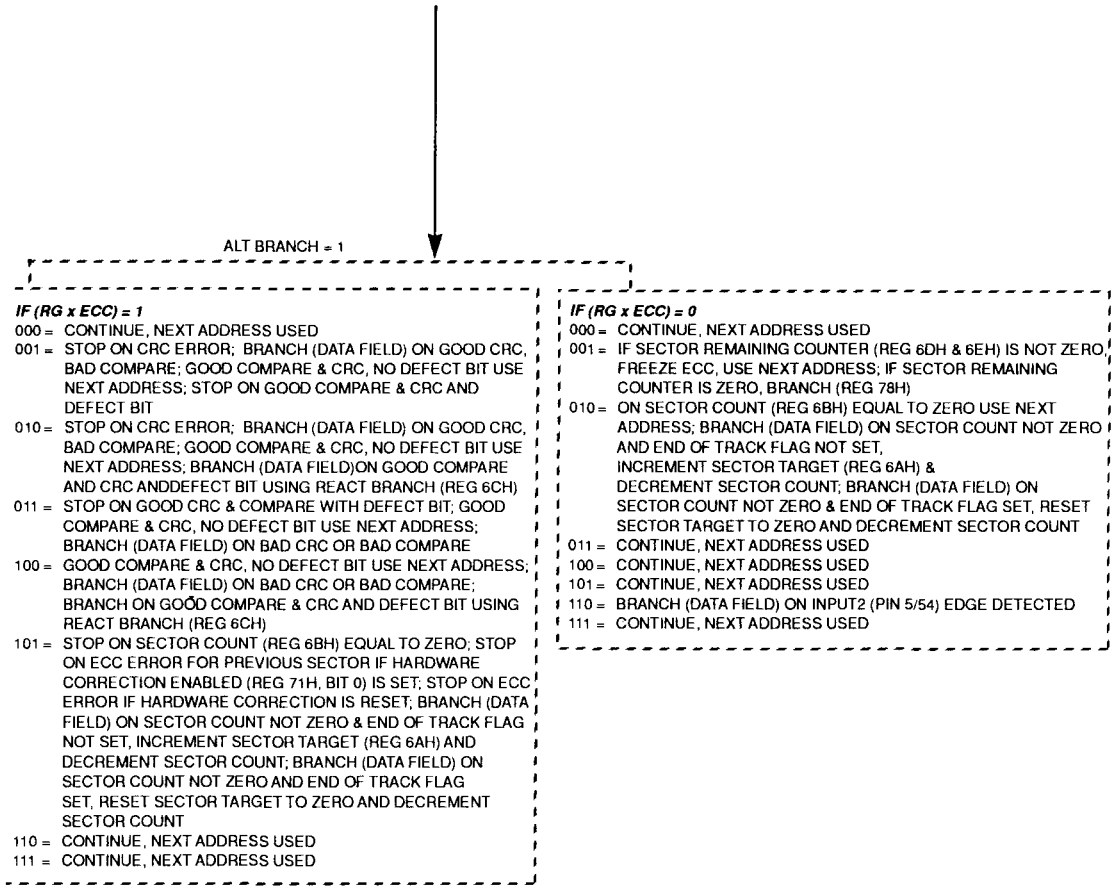
Bit 6	Bit 5	Coded As	Description
0	0	No Change	The state of the Write Gate Signal (Pin 36/85) and the Read Gate Signal (Pin 35/84) is not affected.
0	1	Write Gate 0n	This code is used to assert the Write Gate Signal (Pin 36/85). The Write Gate Signal (Pin 36/85) is asserted during the first count of execution of the Format Sequencer Word with this bit combination set. The Write Gate Signal (Pin 36/85) is not asserted if the Read Gate Signal (Pin 35/84) is already asserted when this bit combination is executed.
1	0	Read Gate On	This code is used to assert the Read Gate Signal (Pin 35/84). The Read Gate Signal is asserted during the first count of the execution of the Format Sequencer Word with this bit combination set. The Read Gate Signal (Pin 35/84) is not asserted if the Write Gate Signal (Pin 36/85) is already asserted. The Read Gate Signal is deasserted at the end of ECC processing, or when the Format Sequencer goes to the stopped state.
1	1	Write Gate Off	This code is used to deassert the Write Gate Signal (Pin 36/85). The Write Gate Signal (Pin 36/85) is cleared during the last count of the execution of the Format Sequencer Word with this bit combination set. The Write Gate Signal (Pin 36/85) is also deasserted when the Format Sequencer comes to a stopped state.

Bit 7 **ALTERNATE BRANCH COMMAND SELECT:** When this bit is set, the branch conditions in the Next Address Field are redefined, as described in Section 6.1.1.

6.5 WCS Worksheet



6.5 WCS Worksheet *(cont.)*



6.6 WCS Worksheet Example

The following map shows a format (F), read (R), and write (W) example with the following assumptions:

- Split data format, with up to two splits
- ID field contains Sync, Cylinder High, Cylinder Low, Head, Sector, Flag/Split (four bytes), and-CRC (two bytes)
- Data field contains Sync (three bytes, one for each data split), three data splits, and ECC bytes (11 bytes)
- The Sequencer start address is 0

		Microprocessor Register Addresses								
Seq. Addr.	Branch Addr. (Reg. 78H)		Next Addr. Field		Control Field		Count Field		Data/ Branch Field	Comments
0		80	C0	A0	00	C0	20	E0	01	Start; Wait for Index/Sector,Two Index Timer
1		81	02(F),03(R,W)	A1	00	C1	Delay	E1	00	Delay after Index/Sector
2		82	04	A2	20	C2	4A	E2	00	Write Gate On,Select CRC, Write PLO
3		83	04	A3	40	C3	61	E3	00	Read Gate On, Select CRC/Sync Timer, AM
4		84	05	A4	12	C4	80	E4	ID Sync	ID Field Sync, Enable Stack/Compare
5		85	06	A5	12	C5	00	E5	CYL High	Cylinder High, Enable Stack/Compare
6		86	07	A6	12	C6	00	E6	CYL Low	Cylinder Low, Enable Stack/Compare
7		87	08	A7	12	C7	00	E7	Head	Head, Enable Stack and Compare
8		88	09	A8	12	C8	10	E8	Sector	Sector Target Reg., Enable Stack/Compare
9		89	0A	A9	08	C9	00	E9	Flag/MS Split1	Upper Data Split Count 1
A		8A	0B	AA	00	CA	00	EA	LS Split1	Lower Data Split Count 1
B		8B	0C	AB	08	CB	00	EB	Flag/MS Split2	Upper Data Split Count 2
C		8C	0D	AC	00	CC	00	EC	LS Split2	Lower Data Split Count 2
D		8D	6E(R),76(W),17(F)	AD	80	CD	41	ED	00	Evaluate CRC/Write CRC
E		8E	0F	AE	00	CE	01	EE	00	Delay Past Write Splice
F		8F	10	AF	40	CF	21	EF	00	Read Gate On, Sync Timer
10		90	11	B0	12	D0	80	F0	Data Sync	Data Sync Byte, Enable Stack/Compare, AM
11	14	91	32	B1	81	D1	Don't care	F1	Data	Data Transfer
12		92	13	B2	60	D2	01	F2	00	Write Gate Off for Write/Format, Delay Read
13		93	16(F,W),0E(R)	B3	00	D3	9F	F3	00	Servo Delay, Extended Count Enable
14		94	B5	B4	80	D4	4B	F4	00	Evaluate ECC and Decision Point
15		95	5F	B5	E0	D5	02	F5	00	Write Gate Off, Stop if Sector Count Zero
16		96	10	B6	20	D6	0A	F6	00	Write Gate On, Write PLO Field
17		97	16	B7	60	D7	02	F7	00	Write Gate Off, Post ID Pad
18		98		B8		D8		F8		
19		99		B9		D9		F9		
1A		9A		BA		DA		FA		
1B		9B		BB		DB		FB		
1C		9C		BC		DC		FC		
1D		9D		BD		DD		FD		
1E		9E		BE		DE		FE		

7. LOCAL MICROCONTROLLER-HOST INTERFACE

The local microcontroller interface to the host is programmed through a set of command, status, and control registers. Many of these registers are shared for XT and AT applications. In general, these registers may be accessed at any time, except when noted. The interface is configured to XT or AT on power-up only. The host resets will not change this configuration.

7.1 XT-Local Microcontroller Interface

The Local XT Register File has eight Command/General-Purpose and three Control/Status Registers. These registers may be accessed by the local microcontroller after setting the XT/AT Mode Bit to 1 (see the PC Mode Control Register). The registers are as follows:

Address	Read	Write
40H or 60H	Command/General Byte 0	Command/General Byte 0
41H or 61H	Command/General Byte 1	Command/General Byte 1
42H or 62H	Command/General Byte 2	Command/General Byte 2
43H or 63H	Command/General Byte 3	Command/General Byte 3
44H or 64H	Command/General Byte 5	Command/General Byte 5
45H or 65H	Command/General Byte 4	Command/General Byte 4
46H or 66H	General Byte 6	General Byte 6
47H or 67H	General Byte 7	General Byte 7
55H	Mode/Status	Mode/Status
56H	Drive Type	Drive Type
57H	DRV/DMA/IRQ Status	Not Used

7.1.1 XT Registers 40H-47H (60H-67H): Command/General-Purpose (Read/Write)

The Command/General-Purpose Registers allow the local microcontroller to transfer bytes between the host and the disk controller without going through the buffer memory. These registers are used to receive the six command or configuration bytes and to send sense status or command-completion status. The local microcontroller is locked out of these registers during transfers with the host involving these registers. Host access to these registers is controlled by the local microcontroller through the XT Mode/Status Register. All the command/general-purpose registers are read/written by the local microcontroller. However, for the host access, the read/write direction is controlled by the I/O* Bit in the XT Mode/Status Register. These registers are not initialized on any reset.

7.1.2 XT Register 55H: Mode/Status (Read/Write)

The Mode/Status Register contains control and status for the XT interface. All transfers between the host and the Local Register File are controlled by this register. In addition, the local microcontroller may set or reset the state of the XT interface through this register. This register is reset by the assertion of HRST*/ HRST (Pin 53/2), RST* (Pin 34/83), or a host-programmed reset. The register contains the following bits:

Bits 2-0	R/W	**LRTC0:2**: The Local Register Transfer Count (LRTC) Bits set the number of bytes to be transferred between the host and the Local Register File. Up to eight bytes may be transferred each time. These bits contain the transfer length minus one (i.e., LRTC0:2 = 0 for transfer of 1). The Local Register File Transfer Address Pointer always starts with Register 0 and is incremented on each byte transfer. A read of these bits represents the number of bytes to be transferred.
Bit 3	R/W	**LRTRNS**: The Local Register File Transfer Request (LRTRNS) Bit generates a transfer between the host and the register file when set to 1 by the local microcontroller. This bit will be reset when the host transfer is complete. The local microcontroller should not access the Local Register File, Registers 0-7, when this bit is set. This bit may be set only when there are no active transfers between the host and buffer memory (i.e., when the BTRNS Bit [Bit 4] = 0).
Bit 4	R	**BTRNS**: The Buffer Transfer (BTRNS) Bit represents the state of host buffer memory access. When this bit is set, it indicates that transfers are active between the host and buffer memory. When set, the local microcontroller may not transfer bytes between the Local Register File and the host.
Bit 5	R/W	**I/O***: This bit determines the direction of transfer being requested when BTRNS or LRTRNS is asserted (see Table 7–1 on the following page).
Bit 6	R/W	**C/D***: This bit determines the type of information being requested — command or data (see Table 7–1 on the following page).
Bit 7	R/W	**BUSY**: The Busy Bit indicates that the controller is busy executing a command. The Busy Bit is set during the selection phase by the host; it is reset at the end of the command during the Status Phase, when the host reads the Status Byte.

Table 7–1. PC/XT I/O Bus Phases Table

BUSY	C/D*	I/O*	State of Controller	Direction of Transfer
0	X	X	Idle	
1	0	0	Data Phase	PC to Controller
1	0	1	Data Phase	Controller to PC
1	1	0	Command Phase	PC to Controller
1	1	1	Status Phase	Controller to PC

NOTE: X = Don't care.

7.1.3 XT Register 56H: Drive Type (Read/Write)

The Drive Type Register is read/write and may be accessed by the local microcontroller at any time. Generally, this register contains information required by the XT BIOS driver to configure the physical attributes of the drive (i.e., cylinders, heads, sectors/track). From the host, this register appears as a read-only register. This register is not affected by any reset. In PC/XT Master/Slave Mode, only four bits of this register are driven to the host. For the master, Bits 3-0 are driven. For the slave, Bits 7-4 are driven. If the CL-SH366 is not configured for Master/Slave Mode, then all eight bits of this register are driven to the host. This register is not affected by any reset.

7.1.4 XT Register 57H: DRV/DMA/IRQ (Read Only)

The DRV/MA/IRQ Status Register reflects the state of the DRV/DMA/IRQ Enable Register written to by the host. This read-only register can be accessed at any time. This register is reset when the HRST*/HRST (Pin 53/2) is asserted or under a host program reset.

Bit 0	R	**DMAEN**: The DMA Request Enable Bit allows driving of the host DREQ Signal during Data Mode transfers.
Bit 1	R	**IRQEN**: The Interrupt Enable Bit controls the enable for the tri-stated host signal HINT/HINT*. When the Interrupt Enable Bit is reset, no interrupts will be issued to the host processor. When set, this allows the controller to interrupt the host at the command completion phase.
Bit 2	R	**DRV**: In Master/Slave Mode, this bit enables the host to select a controller prior to issuing a command. If not in Master/Slave Mode, this bit is a don't care.
Bits 7-3	—	Not Used.

7.2 AT Local Microcontroller Interface

The Local AT Register File has eight Command and three Control/Status Registers. These registers may be accessed by the local microcontroller after setting the XT/AT Mode Bit to 0 (see the PC Mode Control Register). These registers are not initialized on any reset, except the Drive/Head Register. The registers are:

Address	Read	Write
40H or 60H	Error Status	Error Status
41H or 61H	Features	Features
42H or 62H	Sector Count	Sector Count
43H or 63H	Sector Number	Sector Number
44H or 64H	Cylinder High	Cylinder High
45H or 65H	Cylinder Low	Cylinder Low
46H or 66H	Drive/Head Number	Drive/Head Number
47H or 67H	Command	Command
55H	Control/Status	Control/Status
56H	Drive 0 Status	Drive 0 Status
57H	Drive 1 Status	Drive 1 Status

7.2.1 AT Register 40H (60H): Error Status Register (Read/Write)

The Error Status Register contains detailed error status of the last command failure. This register is also used to set controller diagnostic errors during the diagnostic command or on power-up. When an error occurs, this register is loaded and the Error Bit is set in the Control/Status Register. The Error Bit is cleared whenever the host writes to the AT Command Register.

7.2.2 AT Register 41H (61H): Features Register (Read/Write)

This register is command-specific and may be used to enable and disable features of the interface.

7.2.3 AT Register 42H (62H): Sector Count Register (Read/Write)

The Sector Count Register specifies the number of sectors to be transferred during a read/write sector command. This register is decremented by the local microcontroller as each sector is transferred. If this register is loaded with 0, then 256 sectors are transferred.

7.2.4 AT Register 43H (63H): Sector Number Register (Read/Write)

The Sector Number Register contains the starting sector number for the current read/write sector command. This register is incremented by the local microcontroller as each sector is transferred between the host and controller.

7.2.5 AT Register 44H (64H): Cylinder High Register (Read/Write)

The Cylinder High Register contains the lower eight bits of the disk cylinder address. This register, in conjunction with the Cylinder Low Register, constitutes a 16-bit cylinder address. This register is incremented by the local microcontroller as each cylinder boundary is crossed.

7.2.6 AT Register 45H (65H): Cylinder Low Register (Read/Write)

The Cylinder Low Register contains the upper eight bits of the disk cylinder address. This register, in conjunction with the Cylinder High Register, constitutes a 16-bit cylinder address. If the lower cylinder overflows, this register is incremented by the local microcontroller as each cylinder boundary is crossed.

7.2.7 AT Register 46H (66H): Drive/Head Register (Read/Write)

The Drive/Head Register contains the sector size, drive and head number. The local microcontroller increments the head address as each track boundary is crossed. This register is reset by HRST*/HRST (Pin 53/2), RST* (Pin 34/83), host-programmed reset, or a diagnostic command (90H). The format of the register is:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXT	Sector Size		DRV#	Head Number			

7.2.8 AT Register 47H (67H): Command Register (Read/Write)

The host processor issues a new command to the disk controller through this register. The controller must be 'idle' and all other registers must be set up prior to loading the Command Register. The host may abort the current data transfer and start a new command by writing to the Command Register when the data request bit is set.

7.2.9 AT Register 55H: Control/Status Register (Read/Write)

This register is reset when the RST* (Pin 34/83) or HRST*/HRST (Pin 53/2) is asserted or under host program reset, except Bits 1, 2, and 3; these are reset by HRST*/HRST (Pin 53/2) only.

Bit 0	R/W	**ERROR**: The Error Bit is set when an error occurred on the last command or power-up diagnostics. The error code is stored in the Error Status Register. This Error Bit is cleared whenever the host writes to the AT Command Register.
Bit 1	R	**INTEN***: The Interrupt Enable (INTEN) reflects Bit 1 of the AT Host Fixed Disk Register. This register is a write-only host register that the local microcontroller can monitor. When this bit is reset, the tri-state interrupt line to the host bus is enabled.
Bit 2	R	**RESET**: The Reset Bit reflects the status of Bit 2 of the AT Host Fixed Disk Register. This register is a write-only host register that the local microcontroller can monitor. When this bit is set, the host is issuing a programmed reset to the controller. This condition can be sensed by the local microcontroller through the PC Reset Detected Bit (Register 50H, Bit 4) being set after a local interrupt.
Bit 3	R	**HD3EN**: The Head 3 Enable/Reduced Write Current (HD3EN) Bit reflects Bit 3 of the Fixed Disk Register. This register is a write-only host register that the local microcontroller can monitor. When this bit is set, the controller uses the head 3 line on the control cable to the drive as a head-select bit and not the reduced write current. This condition may not be used in all controller designs, since this function is only present in the ST 506/412 Disk Interface.
Bit 4	R/W	**INT**: The Interrupt Request (INT) Bit allows the local microcontroller to set an interrupt to the host by writing a one to this bit. The read of this bit returns the status of the PC interrupt line, HINT/HINT* (Pin 41/90). If interrupt is enabled, the controller asserts the HINT/HINT* Signal to request each sector of data transfer between the host and the FIFO. HINT/HINT* is deasserted at the end of every sector transfer except the final sector. At the end of the last sector transfer, HINT/HINT* remains asserted to indicate the end of a multiple-sector transfer, until the interrupt is serviced by the host. However, if an error occurs during multiple-sector transfers, the HINT/HINT* Signal is asserted upon the error detection and stays asserted through the end of the last sector transfer.
Bit 5	R/W	**CDATA**: The Corrected Data (CDATA) Bit is set whenever a sector read from the disk had a correctable ECC error on the previous read sector transfer. The CDATA Bit is cleared whenever the host writes to AT Command Register.
Bit 6	R	**BTRNS**: The Buffer Transfer (BTRNS) Bit indicates the state of host buffer memory access. When this bit is set, it indicates that transfers are active between the host and the buffer memory. In a disk read, this bit is reset when the last data is transferred to the host. In a disk write, this bit is reset when the last data is transferred to the buffer memory.

7.2.9 AT Register 55H: Control/Status Register (Read/Write) *(cont.)*

Bit 7	R/W	**BUSY**: The Busy Bit indicates that the controller is executing a command. The Busy Bit is set by the host writing to the Command Register. The Busy Bit is automatically cleared on the last sector of a read command after the FIFO has been filled and DREQ is asserted. The definition of the last sector is: the only sector in the case of a single-sector read, the actual last sector of a multi-sector read if no errors, or the sector in error regardless of the sector count (a sector in error is indicated by the assertion of Register 55H, Bit 0). This bit is also set when a diagnostic command is issued, the host writes to the Command Register, or when RST* (Pin 34/83), HRST*/HRST (Pin 53/2), or a host-programmed reset is active.

7.2.10 AT Register 56H: Drive 0 Control/Status Register (Read/Write)

The Drive 0 Status Register contains drive-related status information that is part of the Host Control/Status Register when drive 0 is selected in the Drive Number Field of the Drive/Head Register. This may be accessed by the local microcontroller at any time. The XT/AT Mode Bit must be set to 0 for AT operation. This register is reset by assertion of RST* (Pin 34/83).

Bit 0	R/W	**SKCOMP0**: The Seek Complete (SKCOMP0) Bit reflects the state of the Seek Complete Signal from disk drive 0. When the drive is not seeking, this bit is set.
Bit 1	R/W	**FAULT0**: The Write/Fault (FAULT0) Bit reflects the state of the Write Fault Signal from disk drive 0. When this bit is set, it indicates that the drive is unsafe for access.
Bit 2	R/W	**READY0**: The Ready (READY0) Bit reflects the state of the Ready Signal from disk drive 0. When this bit is set, the drive is present but may not be ready for read/write transfers.
Bit 3	R/W	**RWC0**: The Reduced Write Current (RWC0) Bit reflects the state of the Reduced Write Current Signal from disk drive 0. When this bit is set, the current to the drive write heads has been reduced.
Bit 4	R/W	**OVERRIDE HD3EN0**: When this bit is set, the HD3EN Bit of the AT Host Fixed Disk Register for disk drive 0 is forced to logical 1.
Bits 7-5		Reserved.

7.2.11 AT Register 57H: Drive 1 Control/Status Register (Read/Write)

The Drive 1 Status Register contains drive-related status information that is part of the Host Control/Status Register when Drive 1 is selected in the Drive Number Field of the Drive/Head Register. This may be accessed by the local register at any time. The XT/AT Mode Bit must be set to 0 for AT operation. This register is reset by assertion of RST* (Pin 34/83).

Bit 0	R/W	**SKCOMP1**: The Seek Complete (SKCOMP1) Bit reflects the state of the Seek Complete Signal from disk drive 1. When the drive is not seeking, this bit is set.
Bit 1	R/W	**FAULT1**: The Write/Fault (FAULT1) Bit reflects the state of the Write Fault Signal from disk drive 1. When this bit is set, it indicates that the drive is unsafe for access.
Bit 2	R/W	**READY1**: The Ready (READY1) Bit reflects the state of the Ready Signal from disk drive 1. When this bit is set, the drive is present but may not be ready for read/write transfers.
Bit 3	R/W	**RWC1**: The Reduced Write Current (RWC1) Bit reflects the state of the Reduced Write Current Signal from disk drive 1. When this bit is set, the current to the drive write heads has been reduced.
Bit 4	R/W	**OVERRIDE HD3EN1**: When this bit is set, the HD3EN Bit of the AT Host Fixed Disk Register for disk drive 1 is forced to logical 1.
Bits 7-5	—	Reserved.

8. PC DISK CONTROLLER INTERFACE DESCRIPTION

8.1 XT Disk Controller Interface Description

The CL-SH366 supports the standard XT hardware/BIOS protocol and the additional ability to daisy-chain two embedded drives. The XT interface between the host and the disk over the IBM XT I/O channel is through a combination of I/O ports and DMA data transfers. These registers can be accessed by the XT host when the XT/AT Select Bit (Register 58H, Bit 7) is set. There are three read ports and four write ports. The ports are as follows: Read/Write Data, Status, Programmed Reset, Drive Type, and DRV/DMA/IRQ Enable.

DACK*	HCS0*	HA1	HA0	IOR* = 0	OW* = 0
0	X	X	X	Read Data	Write Data
1	0	0	0	Read Data	Write Data
1	0	0	1	Status	Program Reset
1	0	1	0	Drive Type	Select
1	0	1	1	Not Used	DRV/DMA/IRQ Enable

NOTE: X = Don't Care.

8.1.1 Read Data Register (Port 0 Read)

Data transferred from the controller to the host originates from this register. Data is defined as sector bytes, configuration, and command-completion information. This data is transferred by either programmed I/O or DMA. However, DMA data transfers may only occur if the controller is in the Data Mode (see the Status Register).

8.1.2 Write Data Register (Port 0 Write)

Data transferred from the host to the controller goes through this register. Data is defined as command, sector-byte, and configuration information. This data is transferred either by programmed I/O or DMA. However, DMA transfers may only occur if the controller is in the Data Mode (see the Status Register).

8.1.3 Status Register (Port 1 Read)

The Status Register contains information regarding the present state of the controller. This read-only register contains the following bits:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	INTRQ	DMARQ	BUSY	C/D*	I/O*	REQ

Bit 0	REQ	**REQUEST**: When this bit is set, it indicates that the controller is ready to send or receive a byte. The type and transfer direction of this byte depends on the state of the controller, as defined by the C/D* and I/O* Status Bits. The Request Bit is set and cleared for each byte transferred between the host and the controller. This bit is valid even if the data transfers are being done by DMA.
Bit 1	I/O*	**I/O***: This bit determines the requested transfer direction when the REQ Bit (Bit 0) is asserted (see Table 8–1).
Bit 2	C/D*	**C/D***: This bit determines the type of information being requested, i.e., command, data, or status (see Table 8–1).
Bit 3	BUSY	**BUSY**: This bit indicates that the controller is executing a command. When this bit is set, no new commands are accepted until the controller goes idle by resetting the Busy Bit. The Busy Bit is set during the Selection Phase and reset at the end of the command.
Bit 4	DMARQ	**DMA REQUEST**: This bit is set only during the data transfers between the host and the controller, i.e., C/D*= 0, and REQ =1. In addition, the controller must be programmed to generate DMA transfers by setting the DMAEN Bit in DMA/IRQ Enable Register. This bit is the direct image of the DREQ line on the host bus interface. This bit is set for each byte transfer and cleared by the host bus signal, DACK*.
Bit 5	INTRQ	**INTERRUPT REQUEST**: This bit indicates that an interrupt has been issued to the host. This bit directly reflects the Host Bus Signal HINT/HINT* (Pin 41/90). This bit is set during the Command Completion Phase. During this phase, the Completion Status Byte is available to the host. In order for the Interrupt Request Bit to be set, the host must set the INTEN Bit in DMA/IRQ Enable Register before the Command Completion Phase. The Interrupt Request Bit may only be cleared by the host resetting the INTEN Bit in the DMA/IRQ Enable Register.
Bits 7-6	—	Not used; will read 0.

Table 8–1. PC XT I/O Bus Phases

BUSY	C/D*	I/O*	State of Controller	Direction of Transfer
0	X	X	Idle	
1	0	0	Data Phase	PC to Controller
1	0	1	Data Phase	Controller to PC
1	1	0	Command Phase	PC to Controller
1	1	1	Status Phase	Controller to PC

NOTE: X = Don't care.

8.1.4 Reset Register (Port 1 Write)

The host may reset the controller at any time by issuing an I/O write to Port 1. This will immediately cause the controller to enter the idle state if the controller is busy.

8.1.5 Drive Type Register (Port 2 Read)

The Drive Type Register contains information used by the host to identify the drive characteristics. The information contained in this register is written by the local microcontroller. This read-only register is used by the host BIOS driver program.

8.1.6 Controller Select Register (Port 2 Write)

The controller Select Register is a write-only register that starts the command process. When the controller is idle and the host processor issues a port write to this address, the controller becomes 'busy' and enters the Command Phase. Any data can be written to this register to cause the disk controller to become busy. A write to this port when the controller is busy has no effect.

8.1.7 DRV/DMA/IRQ Enable Register (Port 3 Write)

The DRV/DMA/IRQ Enable Register allows the host to control both DMA transfers and interrupts to the host; for the embedded dual-drive configuration (optional), it allows host control of the selected drive through the DRV Bit. This write-only register can be loaded at any time. The DMAEN Bit allows the disk controller to drive the host DREQ Signal during data phase transfers. The DREQ Signal is set and cleared on each data transfer, forming an interlocked handshake. The DMA Request Enable Bit should be enabled immediately following the 'select' sequence and disabled at the Command Completion Phase. The INTEN Bit controls the enable for the tri-stated host HINT/HINT* Signal. When the INTEN Bit is reset, no interrupts will be issued to the host processor. When set, this allows the disk controller to interrupt the host at the Command Completion Phase. To reset the interrupt once it is set, the host must reset the INTEN Bit. The DRV/ DMA/IRQ Enable Register Bit definition is shown below. Bits 7-3 are don't care bits, but it is recommended that these bits to be set to logical zero.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	X	DRV	INTEN	DMAEN

NOTE: X = Don't Care.

8.2 AT Disk Controller Interface Description

The AT host processor communicates with the disk controller through a series of read/write registers. Register access is accomplished through programmed I/O or DMA (read/write data only). These registers include Data, Error Status, Features, Sector Count, Sector Number, Cylinder Address, Drive/Head Number, Controller/Drive Status, Fixed Disk, and Digital Input. All registers are eight bits, except the Read/ Write Data, which can be 8/16 bits.

Table 8–2. HCS1* Mode Disabled (Register 52H, Bit 3, is reset; Pin 46/95 is HA9)

DREQ	BUSY	HCS0*	HA9	HA2	HA1	HA0	IOR*	IOW*
1	1	0	0	0	0	0	Read Data	Write Data
X	0	0	0	0	0	1	Error Status	Features
X	0	0	0	0	1	0	Sector Count	Sector Count
X	0	0	0	0	1	1	Sector Number	Sector Number
X	0	0	0	1	0	0	Cylinder Low	Cylinder Low
X	0	0	0	1	0	1	Cylinder High	Cylinder High
X	0	0	0	1	1	0	Drive/Head Number	Drive/Head Number
X	0	0	0	1	1	1	Contr./Drive Status	Command
0	1	0	0	X	X	X	Contr./Drive Status	Not Allowed
X	X	0	1	1	1	0	Alternate Status	Fixed Disk
X	X	0	1	1	1	1	Digital Input	Not Used

Table 8–3. HCS1* Mode Enabled (Register 52H, Bit 3 is set; Pin 46/95 is HCS1*)

DREQ	BUSY	HCS0*	HCS1*	HA2	HA1	HA0	IOR*	IOW*
1	1	0	1	0	0	0	Read Data	Write Data
X	0	0	1	0	0	1	Error Status	Features
X	0	0	1	0	1	0	Sector Count	Sector Count
X	0	0	1	0	1	1	Sector Number	Sector Number
X	0	0	1	1	0	0	Cylinder Low	Cylinder Low
X	0	0	1	1	0	1	Cylinder High	Cylinder High
X	0	0	1	1	1	0	Drive/Head Number	Drive/Head Number
X	0	0	1	1	1	1	Contr./Drive Status	Command
0	1	0	1	X	X	X	Contr./Drive Status	Not Allowed
X	X	1	0	1	1	0	Alternate Status	Fixed Disk
X	X	1	0	1	1	1	Digital Input	Not Used

8.2.1 Read Data Register (Read Only)

The Read Data Register transfers sector and ECC data from the buffer to the host. This register is 16 bits wide except when transferring read ECC data, when it is eight bits. The host processor may only access this register during data transfers when the Data Request Bit (DRQ) is set (see Controller/Drive Status Register).

8.2.2 Write Data Register (Write Only)

The Write Data Register transfers sector and ECC data from the host to the buffer. This register is 16 bits wide except when transferring write ECC data, when it is eight bits. The host processor may only access this register during data transfers when the Data Request Bit (DRQ) is set (see the Controller/Drive Status Register).

8.2.3 Error Status Register (Read Only)

The local microcontroller can write detailed error status of the last command failure to this register. This register is also used to set controller diagnostic errors during the diagnostic command or on power-up. When an error occurs, this register is loaded and the Error Bit is set in the Controller/Drive Status Register (see Controller/Drive Status Register). The Error Bit is cleared whenever the host writes to the Command Register. This register may only be read when the Busy Bit is not set (see the Controller/Drive Status Register).

8.2.4 Features Register (Write Only)

The Features Register is command specific and may be used to enable or disable features of the interface. An example would be using the Set Features Command to enable and disable caching. This register was previously called the Write Precompensation Register. This register may only be written when the Busy Bit is not set (see the Controller/Drive Status Register).

8.2.5 Sector Count Register (Read/Write)

The Sector Count Register specifies the number of sectors to be transferred during a read/write sector command. This register is decremented by the local microcontroller as each sector is transferred. If this register is loaded with 0, then 256 sectors are transferred. This register may only be accessed when the Busy Bit is not set (see the Controller/Drive Status Register).

8.2.6 Sector Number Register (Read/Write)

The Sector Number Register contains the starting sector number for the current read/write sector command. This register is incremented by the local microcontroller as each sector is transferred between the host and the controller. This register may only be accessed when the Busy Bit is not set (see the Controller/Drive Status Register).

8.2.7 Cylinder Low Register (Read/Write)

The Cylinder Low Register contains the lower eight bits of the disk cylinder address. This register, in conjunction with the Cylinder High Register, constitutes a 16-bit cylinder address. This register may only be accessed when the Busy Bit is not set (see the Controller/Drive Status Register).

8.2.8 Cylinder High Register (Read/Write)

The Cylinder High Register contains the upper eight bits of the disk cylinder address. This register, in conjunction with the Cylinder Low Register, constitutes a 16-bit cylinder address. This register may only be accessed when the Busy Bit is not set (see the Controller/Drive Status Register).

8.2.9 Drive/Head Register (Read/Write)

The Drive/Head Register contains the sector size, drive and head number. This register may only be accessed when the Busy Bit is not set (see the Controller/Drive Status Register).

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EXT	Sector Size		DRV #	Head Number			

Bit 7, the Extension Bit, is used to extend the data field by up to 11 bytes when using ECC codes. CRC is not appended to data field when EXT = 1; the data field becomes 'sector size + ECC' bytes long. This register is reset when RST* (Pin 34/83) or HRST*/HRST (Pin 53/2) is asserted. It is also reset when an AT host sets Fixed Disk Register, Bit 2 or when the Diagnostic Command is issued by the host.

8.2.10 Controller/Drive Status Register (Read Only)

The Controller/Drive Status Register specifies the state of the controller/drive. This register may be accessed at any time; however, when the Busy Bit is set, no other bits in the register are valid. Also by reading this register, any pending interrupts to the host are cleared.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BUSY	READY	FAULT	SKCOMPL	DREQ	CDATA	INDEX	ERROR

Bit 0	ERROR	**ERROR BIT**: This is set when an error occurred on the last command or power-up diagnostics. The Error Bit is cleared whenever the host writes to the Command Register. The error code is stored in the Error Register.
Bit 1	INDEX	**INDEX SIGNAL**: This reflects the Index Signal from the selected disk drive. This signal goes active once per revolution of the disk. This bit will not be set if the drive is not ready (Bit 6 is reset).
Bit 2	CDATA	**CORRECTED DATA BIT**: This bit is set, whenever, on the previous read sector transfer, a sector read off the disk had a correctable ECC error. The corrected data bit is cleared whenever the host writes to the Command Register.
Bit 3	DREQ	**DATA REQUEST**: The Data Request Bit is set for data transfers to/from the sector buffer. This includes both sector and ECC data. The controller is considered busy whenever the DREQ or Busy Bits are set. Also, when the Data Request Bit is set, the host processor may read/write any of the registers, including the Command Register.
Bit 4	SKCOMPL	**SEEK COMPLETE**: The Seek Complete Bit reflects the state of the Seek Complete Signal from the selected disk drive. When the drive is not seeking, this bit is set.
Bit 5	FAULT	**WRITE FAULT**: The Write Fault Bit reflects the state of the Write Fault Signal from the selected disk drive. When this bit is set, it indicates that the drive is unsafe for read/write access.
Bit 6	READY	**READY**: The Ready Bit reflects the state of the Ready Signal from the selected disk drive. When this bit is set, the drive is present but may not be ready for read/write transfers.
Bit 7	BUSY	**BUSY**: When the Busy Bit is set, the controller is executing a command. Also, when this bit is set, the host processor may not read or write any other registers except the Controller/Drive Status, Alternate Controller/Drive Status, Fixed Disk, or Digital Input registers. This bit is set when RST* or HRST*/HRST Pin is asserted. It is also set when an AT host sets Fixed Disk Register, Bit 2, or when the Command Register is loaded by the host.

8.2.11 Command Register (Write Only)

The host processor issues a new command to the disk controller through this register. The controller must be idle and all other registers must be set up prior to loading the Command Register. The host may abort the current data transfer and start a new data command by writing to the Command Register when the Data Request Bit is set.

8.2.12 Alternate Controller/Drive Status Register (Read Only)

The Alternate Controller/Drive Status Register contains the same bit definition as the Controller/Drive Status Register. This register is used for systems that do not want to reset pending interrupts by reading the Controller/Drive Status Register. This register may be read at any time.

8.2.13 Fixed Disk Register (Write Only)

The Fixed Disk Register is a control register to select Head Mode, reset the controller, and enable interrupts and AT DMA Mode. The DMA Enable Bit (Bit 0) is an extra feature that the CL-SH366 supports for the AT that is not part of the generic AT interface. This feature allows a DMA channel to be multiplexed between multiple peripherals directly by the PC without local microcontroller intervention. To enable this feature, first the DMA Mode must be selected (Register 58H, Bit 3); second, the Enable DMA Control Bit through the Miscellaneous Control/Status Register (Register 52H, Bit 4) must be set. With these two control bits set, then the Fixed Disk Register Bit 0 controls the DMA Enable of the DMA channel. The bit definition of the Fixed Disk Register is shown below; Bits 7-4 are don't care bits, but it is recommended that the user program these bits to logical zero. This register is reset when HRST*/HRST (Pin 53/2) or RST* (Pin 34/83) is asserted.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	HD3EN	RESET	INTEN*	DMAEN

8.2.14 Digital Input Register (Read Only)

The Digital Input Register is a diagnostic loopback register that contains Write Gate, Head Select 3/Reduced Write Current, Head Select 2, Head Select 1, Head Select 0, Drive Select drive 1, and Drive Select drive 0. These bits reflect the state of signals on the disk control cable. The host may read this register at any time. When the host reads this register, only Bits 6-0 are driven; Bit 7 is tri-stated. Note that Bit 6 is not initialized by any host interface hard or soft reset. Bits 5-0 are reset in the same manner as the Drive/Head Register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HiZ	WGate*	H3/RWC*	H2*	H1*	H0*	DS1*	DS0*

NOTE: HiZ denotes high impedance.

9. ELECTRICAL SPECIFICATIONS

9.1 Absolute Maximum Ratings

Ambient temperature under bias ..... 0^{o} C to 70^{o} C

Storage temperature ..... -65^{o} C to 150^{o} C

Voltage on any pin with respect to ground ..... GND -0.5 to V_{CC} +0.5 Volts

Power dissipation ..... 0.50 Watt

Power supply voltage ..... 7 Volts

NOTE: Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9.2 DC Characteristics

Symbol	Parameter	MIN	MAX	Units	Conditions
V_{CC}	Power Supply Voltage	4.5	5.5	V	Operating
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5	V	
V_{OL}[1]	Output Low Voltage		0.4	V	I_{OL} = 2 mA[3]
V_{OL}[2]	Output Low Voltage		0.5	V	I_{OL} = 24 mA
V_{OH}	Output High Voltage	3.5		V	I_{OH} = -400 µA
I_L	Input Leakage	-10	10	uA	$0 < V_{IN} < V_{CC}$
C_{IN}	Input Capacitance		10	pF	
C_{OUT}	Output Capacitance		10	pF	

NOTES: 1) All output pins except for PC Signals.

2) PC Outputs.

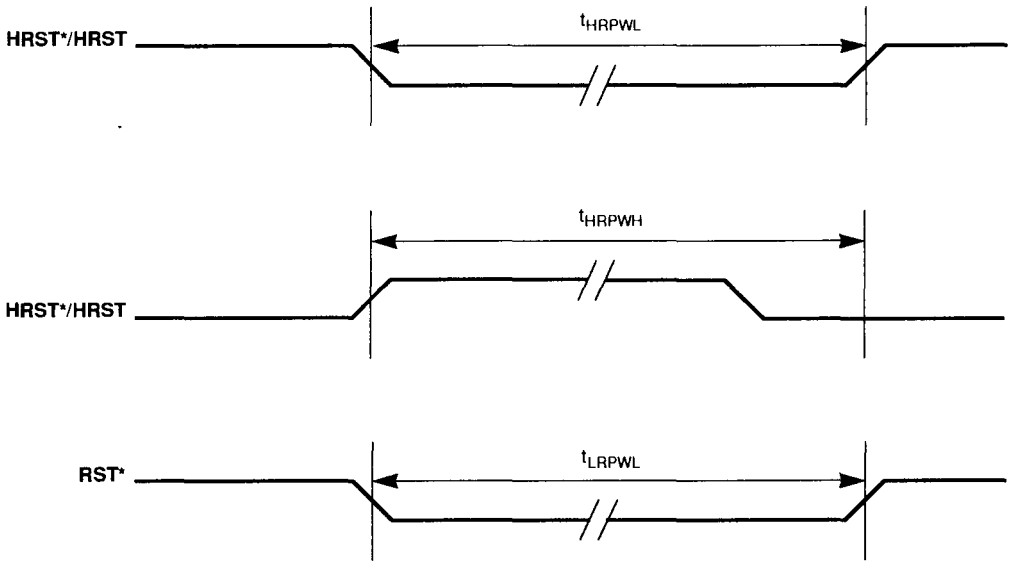
3) I_{OL} = 4 mA for RG and WG.

9.3 AC Characteristics/Timing Information

9.3.1 Index of Timing Information

Table 9–1. RESET Assertion Timing Parameters

Symbol	Parameter	MIN	MAX	Units
t_{HRPWL}	HRST*/HRST pulse width low	500		ns
t_{HRPWH}	HRST*/HRST pulse width high	500		ns
t_{LRPWL}	RST* pulse width low	10		µs



Figures 9–1a. and 9–1b. RESET Assertion Timings

Table 9–2. Microprocessor Interface Timing Parameters

Symbol	Parameter	MIN	MAX	Units
t_A	ALE Width	20		ns
t_{AR}	Address Valid to RD* ⇓ or DS ⇑	15		ns
t_R	RD* Width	60		ns
a_S	Address Valid to ALE ⇓	5		ns
a_H	ALE ⇓ to Address Invalid	5		ns
c_S	CS Valid to RD* ⇓ or DS ⇑	5		ns
c_H	RD* ⇑ or DS ⇓ to CS ⇓	0		ns
t_{DA}	RD* ⇓ or DS ⇑ to Read Data Valid		40	ns
t_{DS}	DS Width	60		ns
t_{DH}	RD* ⇑ to Read Data Invalid	0	15	ns
t_{SRW}	R/W* valid to DS ⇑	5		ns
t_{HRW}	DS ⇓ to R/W* Invalid	5		ns
t_{AL}	AD[7:0] Valid to A[7:0]		20	ns

NOTES: ⇑ indicates rising edge. ⇓ indicates falling edge.

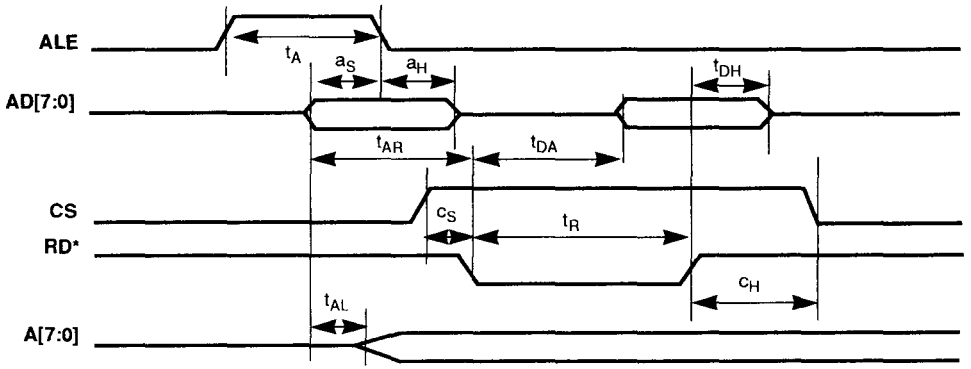


Figure 9–2a. Multiplexed Intel Register Read Timing

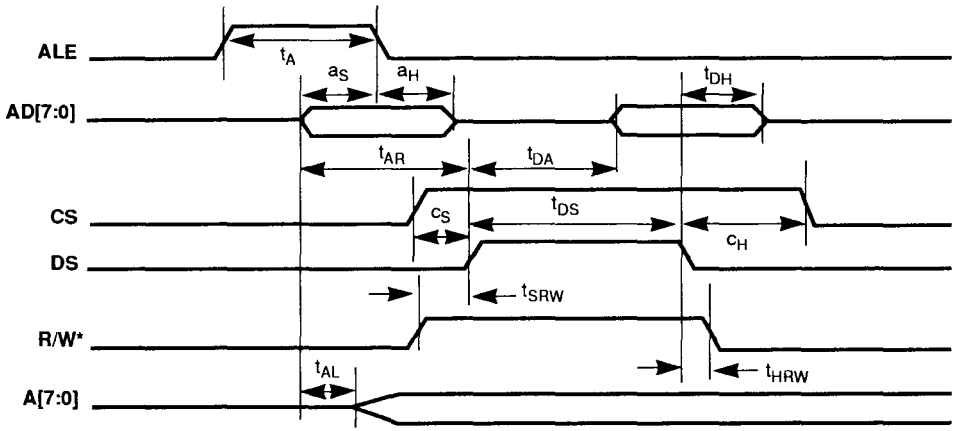


Figure 9–2b. Multiplexed Motorola Register Read Timing

Table 9–3. Microprocessor Interface Timing Parameters

Symbol	Parameter	MIN	MAX	Units
t_A	ALE Width	20		ns
t_{Aw}	Address valid to WR* ⇓ or DS ⇑	15		ns
t_w	WR* Width	50		ns
a_S	Address Valid to ALE ⇓	5		ns
a_H	ALE ⇓ to Address Invalid	5		ns
c_S	CS Valid to WR* ⇓ or DS ⇑	5		ns
c_H	WR* ⇑ or DS ⇓ to CS ⇓	0		ns
w_{DS}	Write Data Valid to WR* ⇑ or DS ⇓	20		ns
w_{DH}	WR* ⇑ or DS ⇓ to Write Data Invalid	10		ns
t_{DS}	DS width	60		ns
t_{SRW}	R/W* valid to DS ⇑	5		ns
t_{HRW}	DS ⇓ to R/W* invalid	5		ns
t_{AL}	AD[7:0] Valid to A[7:0]		20	ns

NOTES: ⇑ indicates rising edge. ⇓ indicates falling edge.

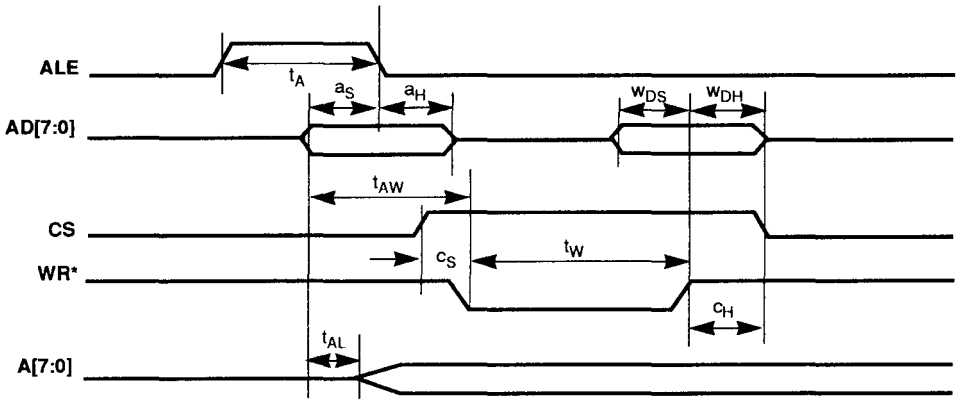


Figure 9–3a. Multiplexed Intel Register Write Timing

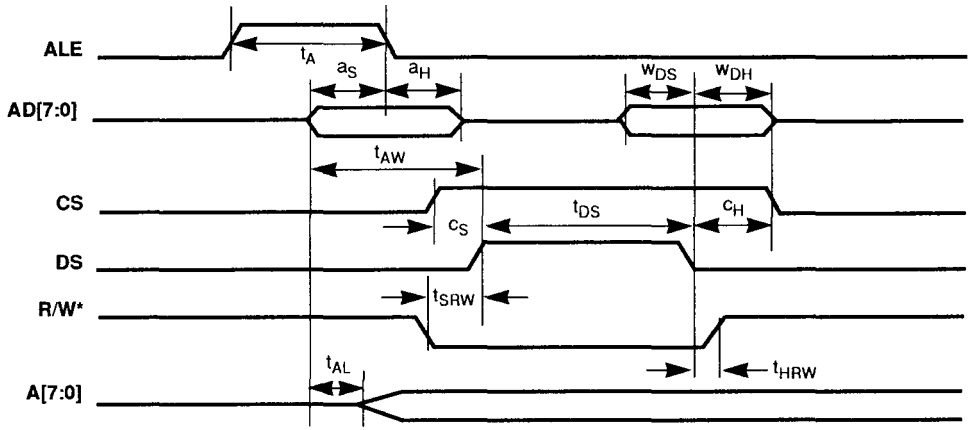


Figure 9–3b. Multiplexed Motorola Register Write Timing

Table 9–4. Microprocessor Interface Timing Parameters

Symbol	Parameter	MIN	MAX	Units
t_{DS}	DS Width	60		ns
t_{AS}	Address Valid to DS ⇑	25		ns
t_{AH}	DS ⇓ to Address Invalid	0		ns
cs_{f1}	CS ⇑ to DS ⇑	10		ns
c_H	DS ⇓ to CS ⇓	0		ns
t_{DA}	DS ⇑ to Read Data Valid		40	ns
t_{DH}	DS ⇓ to Read Data Invalid	0	25	ns
wd_S	Write Data Valid to DS ⇓	20		ns
wd_H	DS ⇓ to Write Data Invalid	10		ns
t_{SRW}	R/W* Valid to DS ⇑	5		ns
t_{HRW}	DS ⇓ to R/W* Invalid	5		ns

NOTES: ⇑ indicates rising edge. ⇓ indicates falling edge.

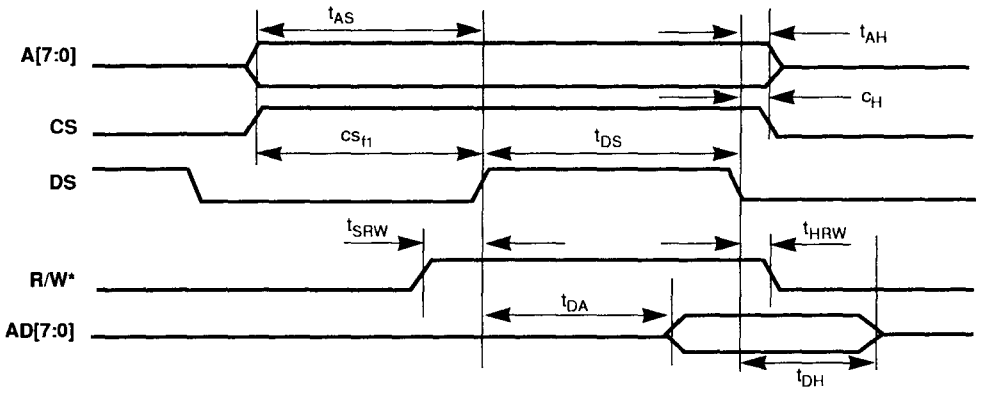


Figure 9–4a. Non-Multiplexed Register Read Timing

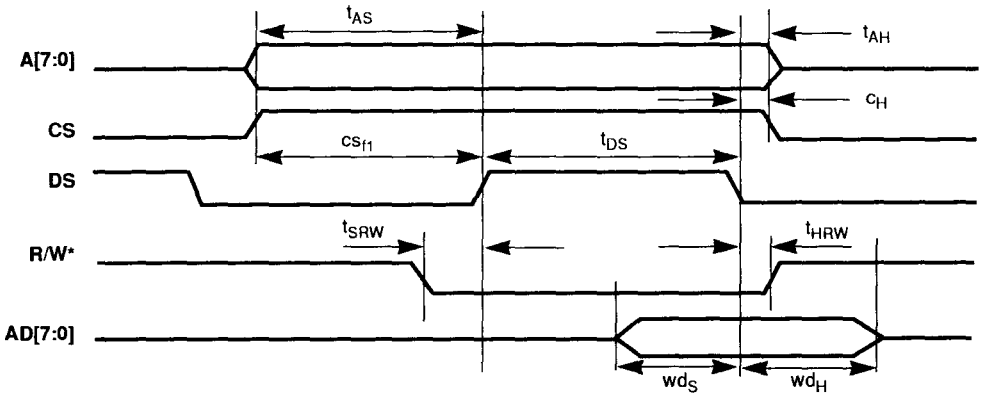


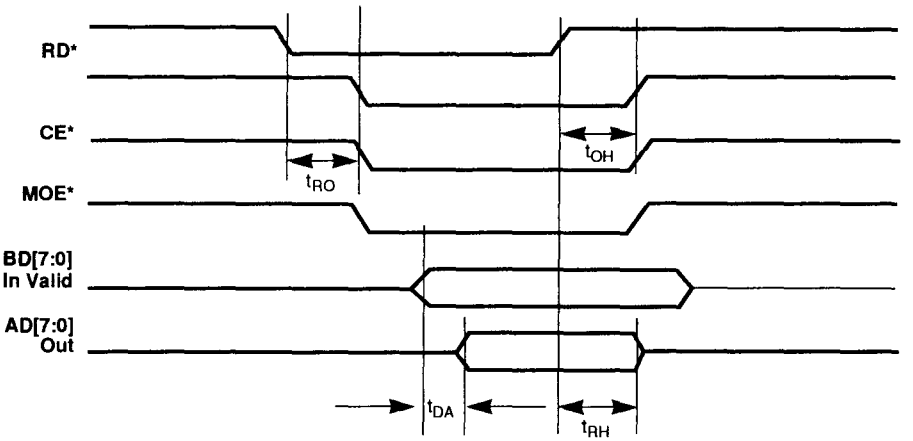
Figure 9–4b. Non-Multiplexed Register Write Timing

Table 9–5. Register 70H Access Timing Parameters

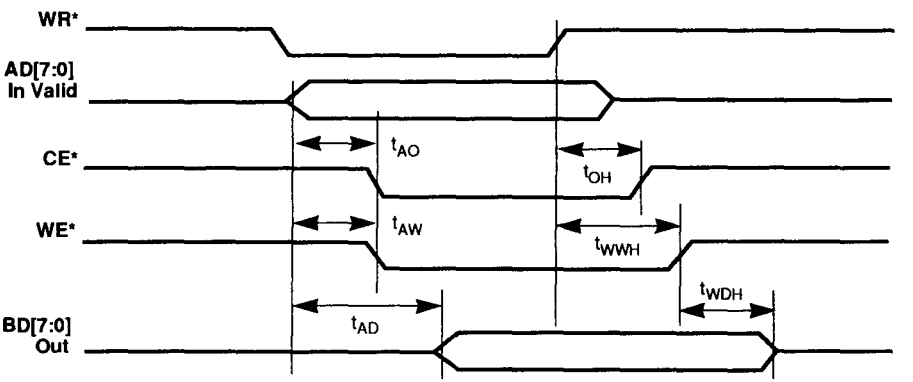
Symbol	Parameter	MIN	MAX	Units
t_{RO}	RD* ⇓ or WR* ⇓ to MOE* ⇓ or CE* ⇓		40	ns
t_{DA}	BD[7:0] In Valid to AD[7:0] Out		55	ns
t_{RH}	RD* ⇑ to AD[7:0] Invalid		50	ns
t_{OH}	RD*⇑ or WR* ⇑ to MOE*⇑ or CE* ⇑		40	ns
t_{AW}	AD[7:0] In Valid to WE* ⇓		55	ns
t_{AO}	AD[7:0] In Valid to CE* ⇓		55	ns
t_{AD}	AD[7:0] In Valid to BD[7:0] Out		55	ns
t_{WWL}	WR* ⇓ to WE*⇓		40	ns
t_{WWH}	WR* ⇑ to WE* ⇑		40	ns
t_{WDH}	WE* ⇑ to BD[7:0] Out Invalid	10		ns

NOTES: ⇑ indicates rising edge. ⇓ indicates falling edge.

Read Register 70H Timing (SRAM Mode Only)



Write Register 70H Timing (SRAM Mode Only)



Figures 9–5a. and 9–5b. Register 70H Access Timing Parameters

Table 9–6. Disk Read/Write Timing Parameters (1-Bit NRZ Interface)

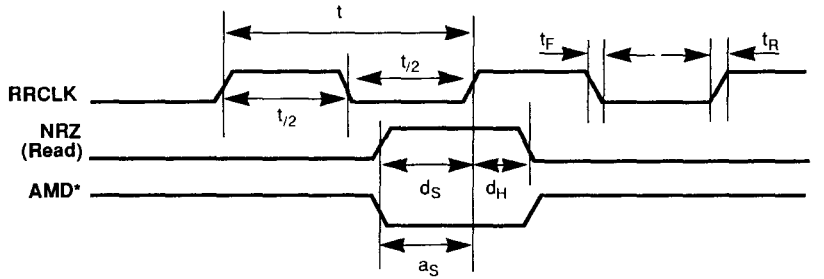
		32 MHz		
Symbol	**Parameter**	**MIN**	**MAX**	**Units**
$f_{RRCLK/1FCLK}$	RRCLK/1FCLK Frequency		32	MHz
t	RRCLK/1FCLK Period	31		ns
$t_{/2}$ (L)	RRCLK/1FCLK Low Time at 0.8V	7		ns
$t_{/2}$ (H)	RRCLK/1FCLK High Time at 2.0V	12		ns
$t_R = t_F$	RRCLK/1FCLK Rise and Fall Time		5	ns
d_S	NRZ In Valid to RRCLK ⇑	5		ns
d_H	RRCLK ⇑ to NRZ In Invalid	5		ns
a_S[1]	AMD* Valid to RRCLK ⇑	6		ns
d_V	RRCLK ⇑ to NRZ Out	6	18	ns
w_V[1]	RRCLK ⇑ to WAM* Out	6	18	ns

		40 MHz		
Symbol	**Parameter**	**MIN**	**MAX**	**Units**
$f_{RRCLK/1FCLK}$	RRCLK/1FCLK Frequency		40	MHz
t	RRCLK/1FCLK Period	25		ns
$t_{/2}$ (L)	RRCLK/1FCLK Low Time at 0.8V	7		ns
$t_{/2}$ (H)	RRCLK/1FCLK High Time at 2.0V	12		ns
$t_R = t_F$	RRCLK/1FCLK Rise and Fall Time		5	ns
d_S	NRZ In Valid to RRCLK ⇑	5		ns
d_H	RRCLK ⇑ to NRZ In Invalid	5		ns
a_S[1]	AMD* Valid to RRCLK ⇑	6		ns
d_V	RRCLK ⇑ to NRZ Out	6	18	ns
w_V[1]	RRCLK ⇑ to WAM* Out	6	18	ns

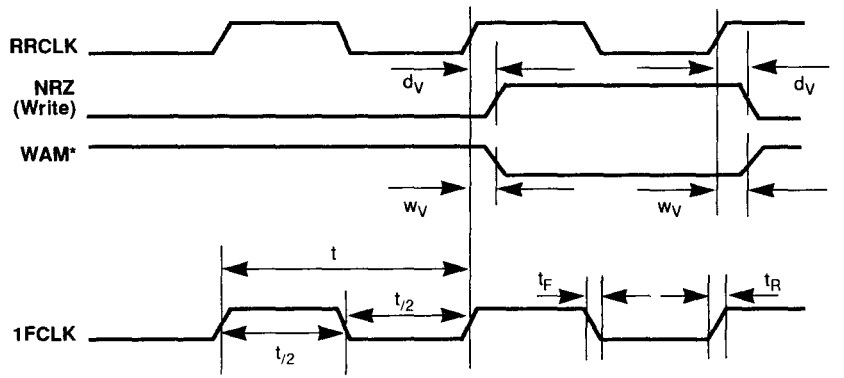
NOTES: ⇑ indicates rising edge. ⇓ indicates falling edge.

(1) These specifications are only applicable in the Soft Sector Mode.

Disk Read Timing (1-Bit NRZ Interface)



Disk Write Timing (1-Bit NRZ Interface)



Figures 9–6a. and 9–6b. Disk Read/Write Timing Parameters

Table 9–7. Disk Read/Write Timing Parameters (Parallel 2-Bit NRZ Interface)

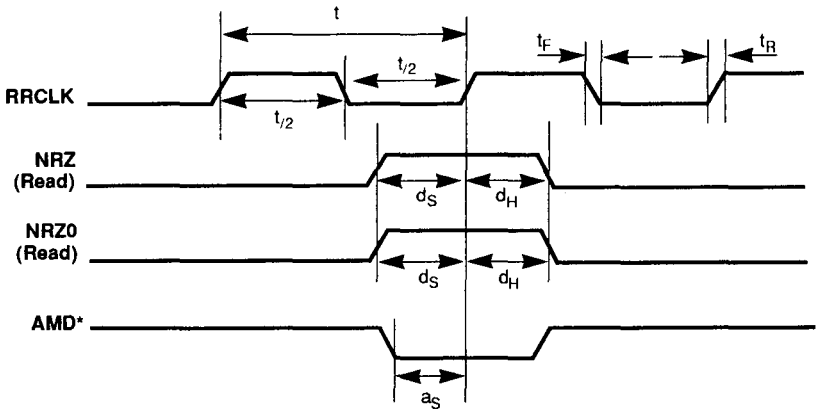
		24 MHz		
Symbol	**Parameter**	**MIN**	**MAX**	**Units**
$f_{RRCLK/1FCLK}$	RRCLK/1FCLK Frequency		24	MHz
t	RRCLK/1FCLK Period	41		ns
$t_{/2}$ (L)	RRCLK/1FCLK Low Time at 0.8V	10		ns
$t_{/2}$ (H)	RRCLK/1FCLK High Time at 2.0V	13		ns
$t_R = t_F$	RRCLK/1FCLK Rise and Fall Time		5	ns
d_S	NRZ In Valid to RRCLK ⇑	5		ns
d_H	RRCLK ⇑ to NRZ In Invalid	5		ns
a_S[1]	AMD* Valid to RRCLK ⇑	6		ns
d_V	RRCLK ⇑ to NRZ Out	6	18	ns
w_V[1]	RRCLK ⇑ to WAM* Out	6	18	ns

		32 MHz		
Symbol	**Parameter**	**MIN**	**MAX**	**Units**
$f_{RRCLK/1FCLK}$	RRCLK/1FCLK Frequency		32	MHz
t	RRCLK/1FCLK Period	31		ns
$t_{/2}$ (L)	RRCLK/1FCLK Low Time at 0.8V	10		ns
$t_{/2}$ (H)	RRCLK/1FCLK High Time at 2.0V	13		ns
$t_R = t_F$	RRCLK/1FCLK Rise and Fall Time		4	ns
d_S	NRZ In Valid to RRCLK ⇑	5		ns
d_H	RRCLK ⇑ to NRZ In Invalid	5		ns
a_S[1]	AMD* Valid to RRCLK ⇑	6		ns
d_V	RRCLK ⇑ to NRZ Out	6	18	ns
w_V[1]	RRCLK ⇑ to WAM* Out	6	18	ns

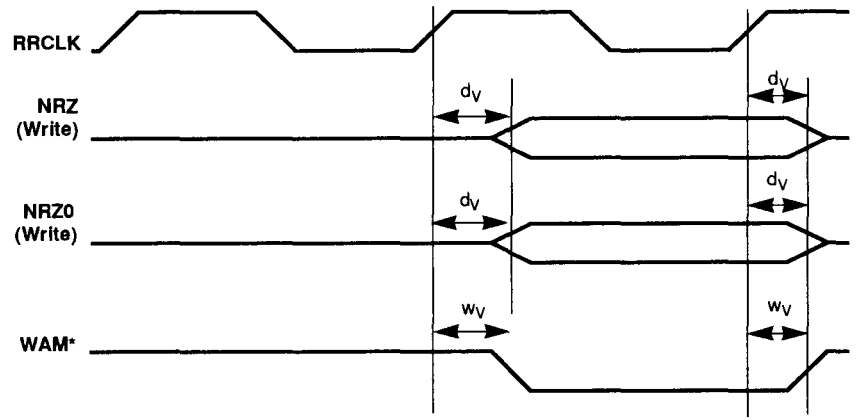
NOTES: ⇑ indicates rising edge. ⇓ indicates falling edge.

(1) These specifications are only applicable in the Soft Sector Mode.

Disk Read Timing (Parallel 2-Bit NRZ Interface)



Disk Write Timing (Parallel 2-Bit NRZ Interface)



Figures 9–7a. and 9–7b. Disk Read/Write Timing Parameters

Table 9–8. SRAM Buffer Memory Read/Write Timing Parameters

Symbol	Parameter	MIN	MAX	Units
t_B	BCLK Period	25		ns
$t_{B/2}$	BCLK Low/High Time	12		ns
$t_{BR} = t_{BF}$	BLCK Rise and Fall Time		5	ns
t_{AV}	BLCK ⇑ to Address Valid		20	ns
t_{EV}	BLCK ⇑ to MCE* ⇓		20	ns
t_{EH}	BLCK ⇑ to MCE* ⇑	28		ns
t_{MV1}	BLCK ⇑ to MOE* ⇓		20	ns
t_{MH1}	BLCK ⇑ to MOE* ⇑	28		ns
t_{WV}	BLCK ⇓ to WE* ⇓		28	ns
t_{WH}	BLCK ⇓ to WE* ⇑		28	ns
t_{DOV1}	BLCK ⇓ to Data Out Valid in SRAM		28	ns
t_{DOH1}	BLCK ⇑ to Data Out invalid in SRAM	0		ns
t_{DIS1}	Data in Valid to BLCK ⇑ in SRAM	5		ns
t_{DIH1}	BLCK ⇑ to Data Invalid in SRAM	10		ns

NOTES: ⇑ indicates rising edge. ⇓ indicates falling edge.

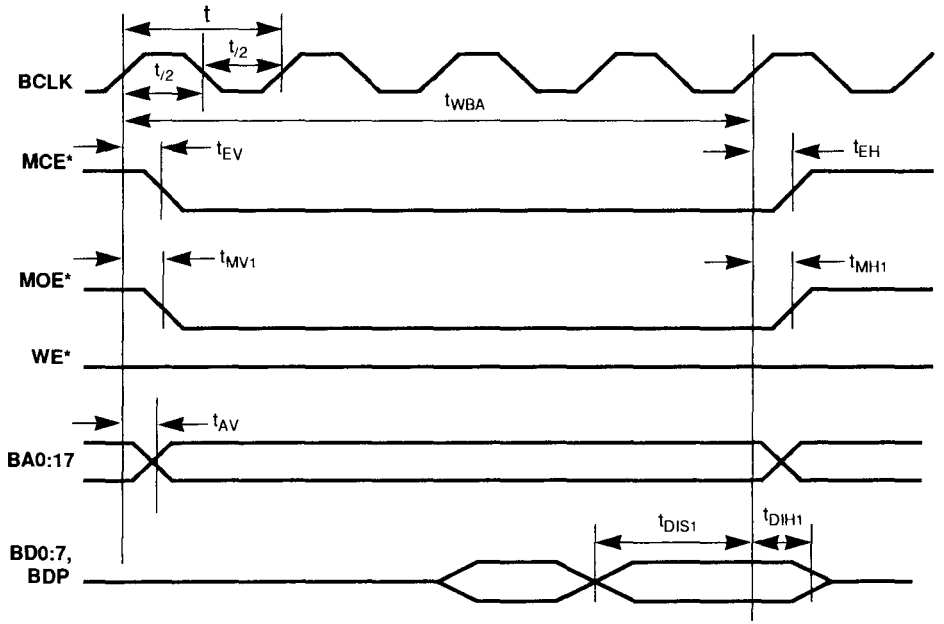


Figure 9–8a. SRAM Read Timing

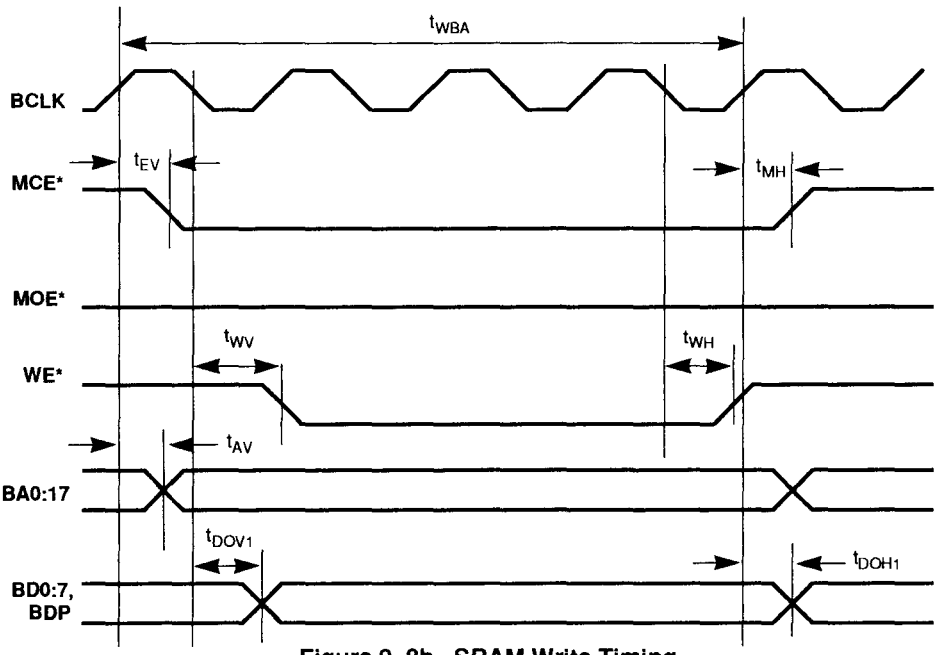
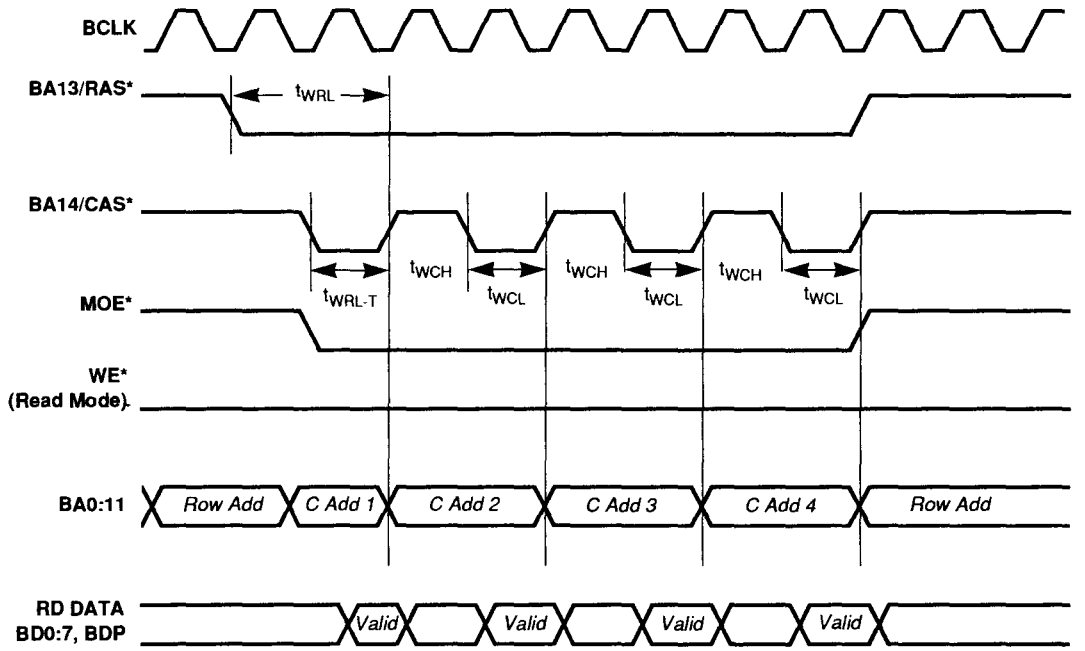


Figure 9–8b. SRAM Write Timing

Table 9–9. DRAM Buffer Memory Read/Write Timing Parameters

Symbol	Parameter	MIN	MAX	Units
t_B	BCLK Period	25		ns
$t_{B/2}$	BCLK Low/High Time	12		ns
$t_{BR} = t_{BF}$	BLCK Rise and Fall Time		5	ns
t_{RV}	BLCK ⇓ to RAS* ⇓		20	ns
t_{RH}	BLCK ⇓ to RAS* ⇑		20	ns
t_{RAV}	BLCK ⇑ to Row Address Valid		28	ns
t_{RAH}	BLCK ⇑ to Row Address Invalid		28	ns
t_{CV}	BLCK ⇓ to CAS* ⇓		28	ns
t_{CH}	BLCK ⇓ to CAS* ⇑		28	ns
t_{CAV}	BLCK ⇑ to Column Address Valid		28	ns
t_{CAH}	CAS* ⇓ to Column Address Invalid		28	ns
t_{MV}	BLCK ⇓ to MOE* ⇓		28	ns
t_{MH}	BLCK ⇓ to MOE* ⇑		28	ns
t_{DOV}	BLCK ⇑ to Data Out Valid in DRAM		28	ns
t_{DOH}	BLCK ⇑ to Data Out Invalid in DRAM	0		ns
t_{DIS}	Data In Valid to BLCK ⇓ in DRAM	5	28	ns
t_{DIH}	BLCK ⇓ to Data In Invalid in DRAM	10		ns
t_{WV}	BLCK ⇓ to WE* ⇓		28	ns
t_{WH}	BLCK ⇓ to WE* ⇑		28	ns
t_{DIS}	Data In Valid to BLCK ⇓ in DRAM	5		ns
t_{DIH}	BLCK ⇓ to Data In Invalid in DRAM	10		ns
t_{DIS}	Data in Valid to BLCK ⇑ in SRAM	5		ns
t_{DIH}	BLCK ⇑ to Data Invalid in SRAM	10		ns

NOTES: ⇑ indicates rising edge. ⇓ indicates falling edge.



NOTE: t_{WRL} and t_{WRH} are functional parameters that specify the duration of the BA13/RAS* Signal width low and width high (in BCLK periods) for a normal RAM data buffer access cycle. The value are programmed in Bits 3-0 of the Register S53H.

Figure 9–9a. DRAM Page Mode Read/Write Timing

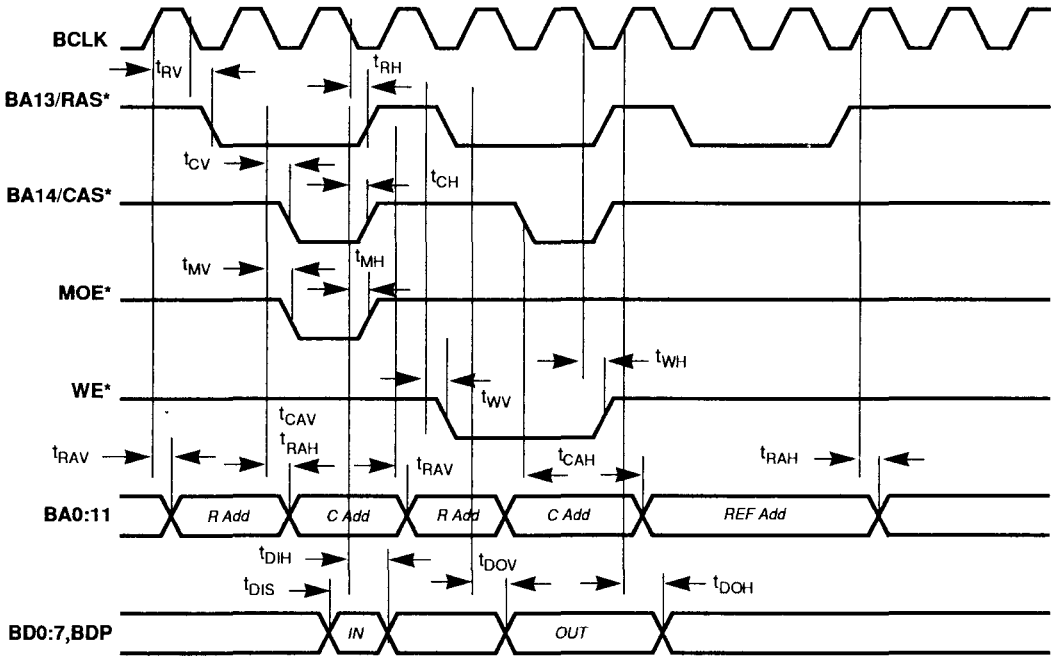


Figure 9–9b. DRAM Write/Read/Refresh Timing

Table 9–10. Host-PC-Programmed I/O Timing Parameters

Symbol	Parameter	MIN	MAX	Units
$cs16_L$	HCS0* Low, HA[2:0], HA9/HCS1* to IOCS16* Low		20	ns
adr_{SET}	HCS0*, HA[2:0], HA9/HCS1* Set-up to IOR*/IOW* Low	30		ns
adr_{HLD}	HCS0*, HA[2:0], HA9/HCS1* Hold from IOR*/IOW* High	10		ns
$ioch_L$	IOR*/IOW* Low to IOCHRDY Low		25	ns
$ioch_{TW}$	IOCHRDY Pulse Width	0	5*BUFCLK	ns
rd_{TA}	IOR* Low to HDB[15:0] Valid		60	ns
rd_{HLD}	IOR* High to HDB[15:0] Invalid	5		ns
rd_{TRI}	IOR* High to HDB[15:0] Tri-state		30	ns
wd_S	HDB[15:0] Set-up to IOW* High	40		ns
wd_{HLD}	HDB[15:0] Hold from IOW* High	10		ns
rw_{PULSE}	IOR*/IOW* Pulse Width	80		ns

NOTE: BUFCLK is the internal Buffer Clock that indicates the period of Buffer Access Cycles derived from BCLK in the appropriate Divide By Mode (Register 7FH, Bits 6 and 7). The minimum Buffer Access Cycle is 83.33 ns.

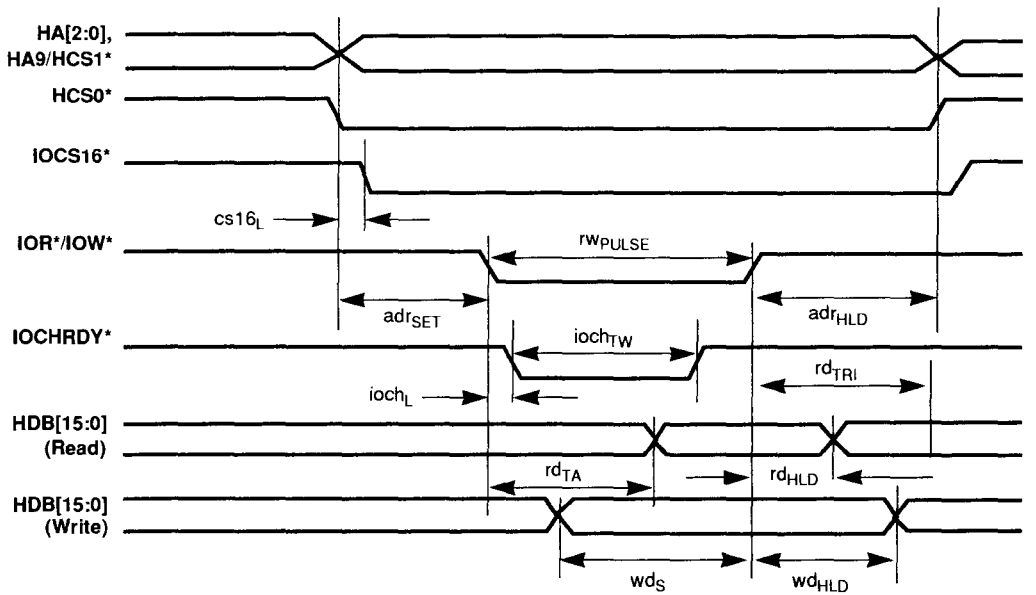


Figure 9–10. Programmed I/O, 8-/16-Bit Host Interface Timing

Table 9–11. Host DMA 8-/16-Bit Interface Timing Parameters (Single-Transfer Mode)

Symbol	Parameter	MIN	MAX	Units
$dreq_L$	DREQ Low from DACK* Low		60	ns
dma_{SET}	DACK* Low to IOR*/IOW* Low	10		ns
dma_{HLD}	DACK* Hold from IOR*/IOW* High	10		ns
rd_{TA}	IOR* Low to HDB[15:0] Valid		50	ns
rd_{HLD}	IOR* High to HDB[15:0] Invalid	5		ns
rd_{TRI}	IOR* High to HDB[15:0] Tri-state		30	ns
wd_S	HDB[15:0] Set-up to IOW* High	20		ns
wd_{HLD}	HDB[15:0] Hold from IOW* High	10		ns
rw_{PULSE}	IOR*/IOW* Pulse Width	80		ns

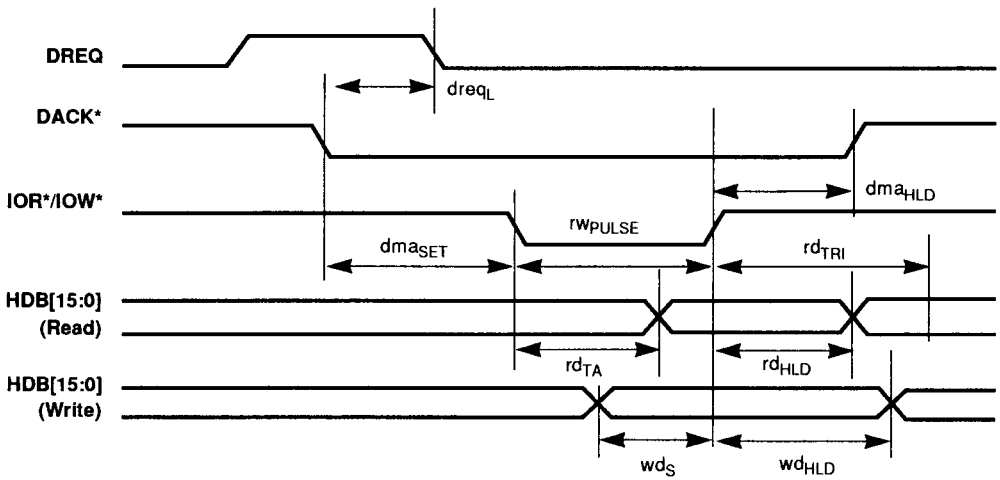


Figure 9–11. Host DMA 8-/16-Bit Interface Timing (Single-Transfer Mode)

Table 9–12. Host DMA 8-/16-Bit Interface Timing Parameters (Demand Mode)

Symbol	Parameter	MIN	MAX	Units
$dreq_L$	DREQ Low from IOR*/IOW* Low		60	ns
dma_{SET}	DACK* Low to IOR*/IOW* Low	10		ns
dma_{HLD}	DACK* Hold from IOR*/IOW* High	10		ns
rw_H	IOR*/IOW* High	50		ns
rd_{TA}	IOR* Low to HDB[15:0] Valid		50	ns
rd_{HLD}	IOR* High to HDB[15:0] Invalid	5		ns
rd_{TRI}	IOR* High to HDB[15:0] Tri-state		30	ns
wd_S	HDB[15:0] Set-up to IOW* High	20		ns
wd_{HLD}	HDB[15:0] Hold from IOW* High	10		ns
rw_{PULSE}	IOR*/IOW* Pulse Width	80		ns

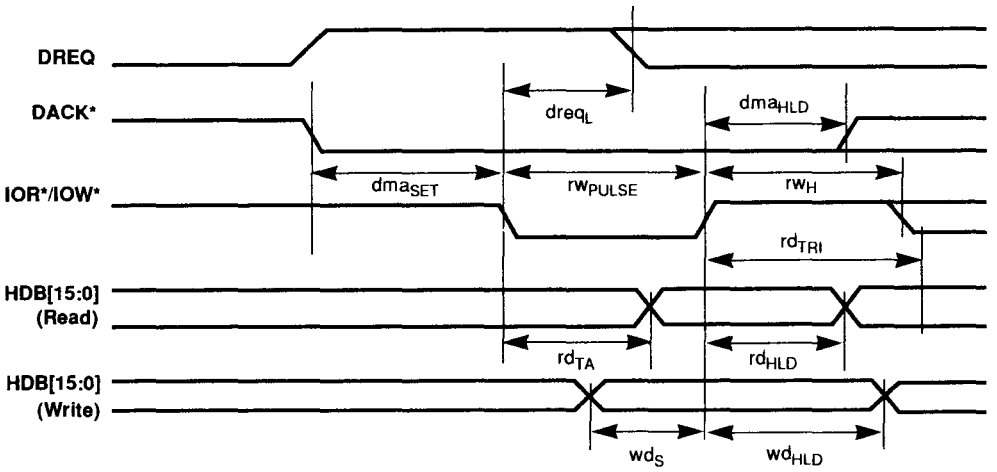
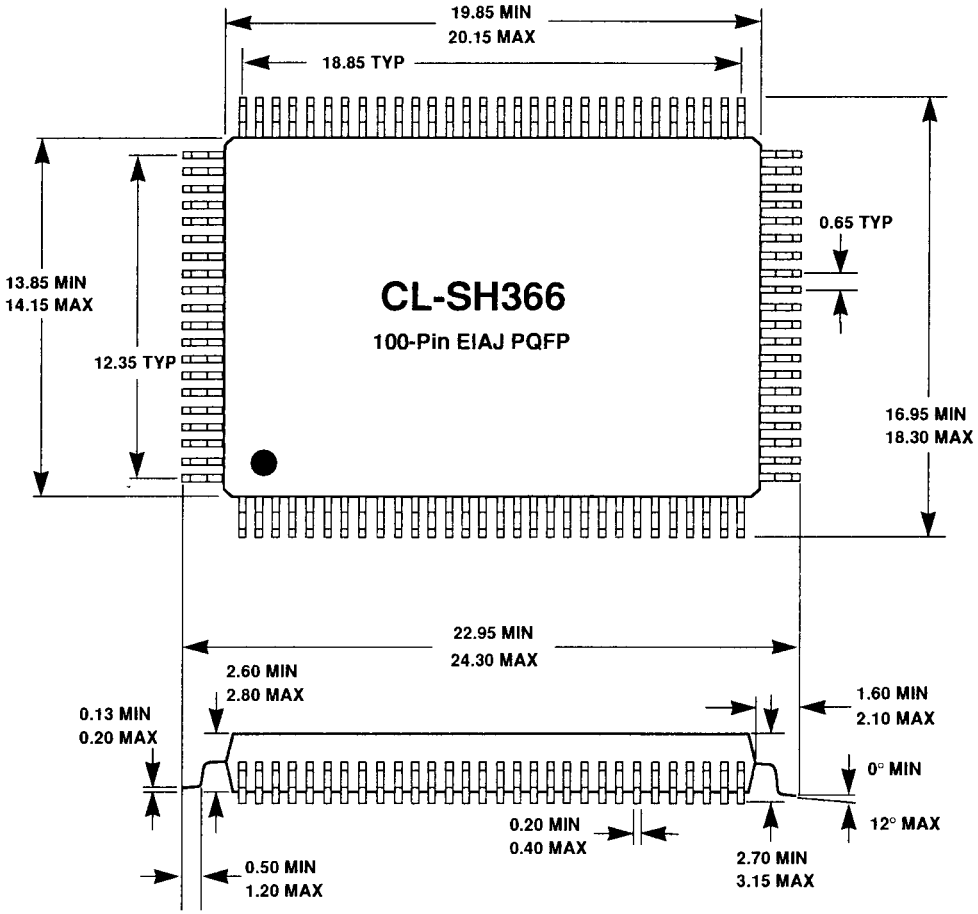


Figure 9–12. Host DMA 8-/16-Bit Interface Timing (Demand Mode)

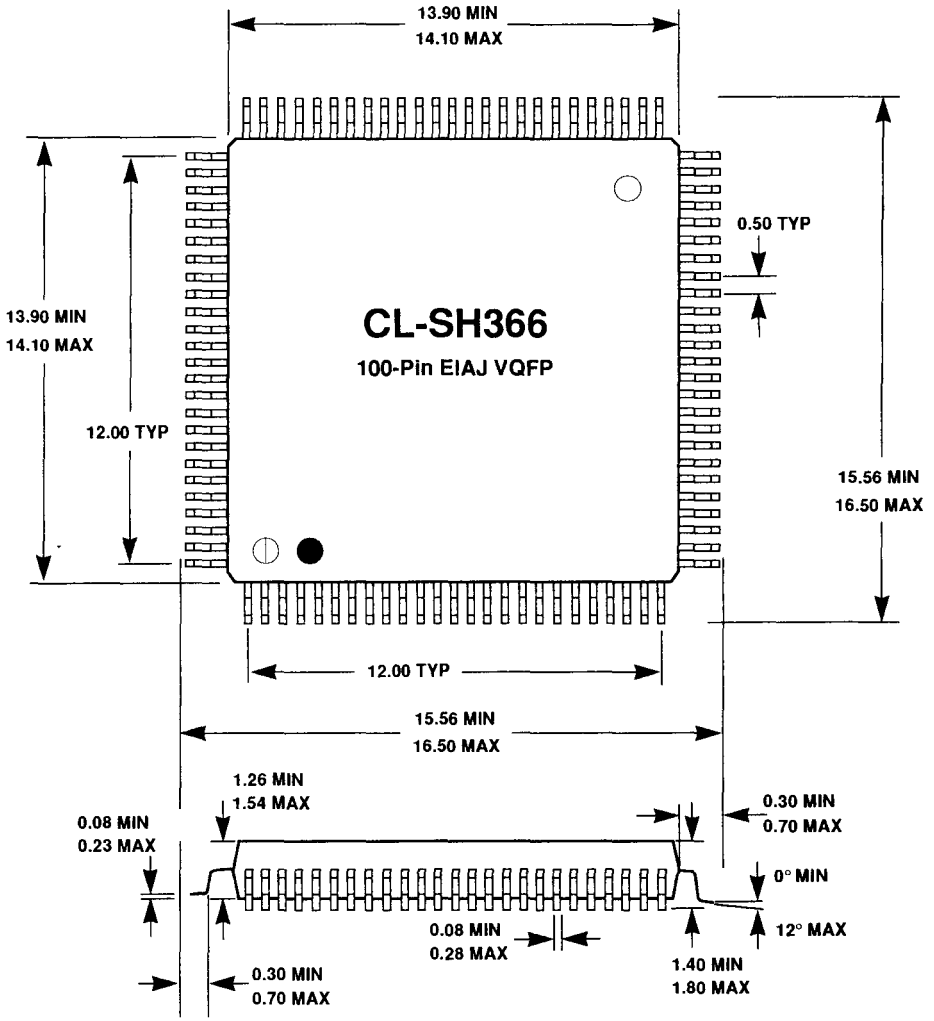
10. SAMPLE PACKAGE

10.1 100-Pin PQFP Package Dimensions (EIAJ)



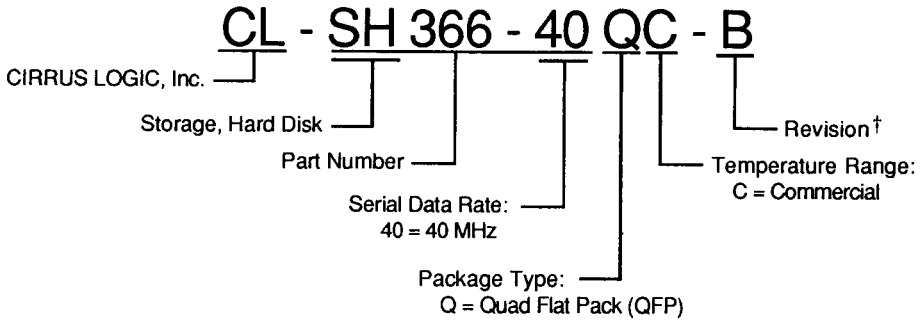
NOTE: Package dimensions are in millimeters.

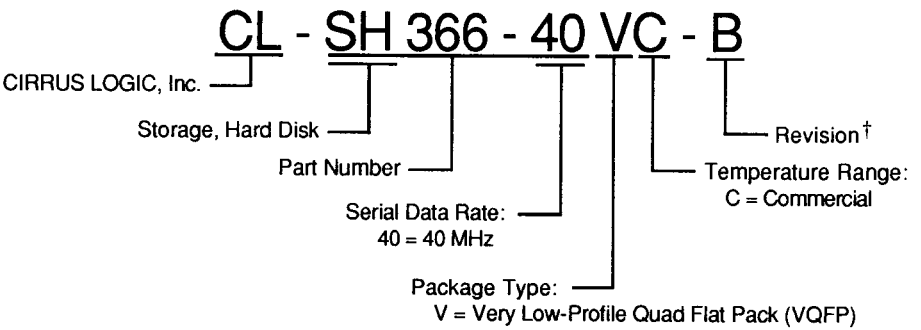
10.2 100-Pin VQFP Package Dimensions (EIAJ)



NOTE: Package dimensions are in millimeters.

11. ORDERING INFORMATION





† Contact Cirrus Logic, Inc., for up-to-date information on revisions.

NOTE: See Section 5.41, *Register 6FH: Revision Register.*

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