4.0 ELECTRICAL SPECIFICATIONS

This section provides information on electrical connections, absolute maximum ratings, recommended operationg conditions, and DC characteristics, and AC characteristics. All voltage values in Electrical Specifications are with respect to V_{SS} unless otherwise noted.

4.1 Electrical Connections

4.1.1 Power and Ground Connections and Decoupling

Testing and operating the 5x86 CPU requires the use of standard high frequency techniques to reduce parasitic effects. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the V_{CC} and GND pins.

4.1.2 Pull-Up/Pull-Down Resistors

Table 4-1 lists the input pins that are internally connected to pull-up and pull-down resistors. When unused, these inputs do not require connection to external pull-up or pull-down resistors. The SUSP# pin is unique in that it is connected to a pull-up resistor only when SUSP# is not asserted. CLKMUL should not be connected to a switching signal.

Table 4-1. Pins Connected to Internal Pull-Up and Pull-Down Resistors

SIGNAL	RESISTOR
A20M#	20-kΩ pull-up
AHOLD	20-kΩ pull-down
BOFF#	20-kΩ pull-up
BS16#	20-kΩ pull-up
BS8#	20-kΩ pull-up
BRDY#	20-kΩ pull-up
CLKMUL	20-kΩ pull-up
EADS#	20-kΩ pull-up
FLUSH#	20-kΩ pull-up
IGNNE#	20-kΩ pull-up
INVAL	20-kΩ pull-up
KEN#	20-kΩ pull-up
RDY#	20-kΩ pull-up
SUSP#	20-kΩ pull-up
UP#	20-kΩ pull-up
WM_RST	20-kΩ pull-down

It is recommended that the ADS#, LOCK# and SMI# output pins be connected to pull-up resistors, as indicated in Table 4-2. The external pull-ups guarantee that the signals remain high (inactive) during hold acknowledge states.

Table 4-2. Pins Requiring External Pull-Up Resistors

SIGNAL	EXTERNAL RESISTOR
ADS#	20-kΩ pull-up
LOCK#	20-kΩ pull-up
SMI#	20-kΩ pull-up

4.1.3 Unused Input Pins

All inputs not used by the system designer and not listed in Table 4-1 (Page 4-1) should be kept at either ground or V_{CC}. To prevent possible spurious operation, connect active-high inputs to ground through a 20-kΩ (± 10%) pull-down resistor and active-low inputs to V_{CC} through a 20-kΩ (± 10%) pull-up resistor.

4.1.4 NC Designated Pins

Pins designated NC should be left disconnected. Connecting an NC pin to a pull-up resistor, pull-down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

4.2 Absolute Maximum Ratings

Table 4-3 lists absolute maximum ratings for the 5x86 microprocessors. Stresses beyond the listed ratings may cause permanent damage to the device. Exposure to conditions beyond these limits may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings may also result in reduced useful life and reliability These are stress ratings only and do not imply that operation under any conditions other than those listed under "Recommended Operating Conditions" Table 4-4 (Page 4-3) is possible.

Table 4-3. Absolute Maximum Ratings

PARAMETER	ALL 5x86 CPUs		UNITS	NOTES
	MIN	MAX		
Operating Case Temperature	-65	110	°C	Power Applied
Storage Temperature	-65	150	°C	No Bias
Supply Voltage, V_{CC}	-0.5	4.0	V	
Voltage On Any Pin	-0.5	6.0	V	
Input Clamp Current, I_{IK}		10	mA	Power Applied
Output Clamp Current, I_{OK}		25	mA	Power Applied

4.3 Recommended Operating Conditions

Table 4-4 lists the recommended operating conditions for the 5x86 CPU.

Table 4-4. Recommended Operating Conditions

PARAMETER	ALL 5x86 CPUs		UNITS	NOTES
	MIN	MAX		
T_C Operating Case Temperature	0	85	°C	
V_{CC} Supply Voltage	3.3	3.6	V	
V_{IH} High-Level Input Voltaage	2.0	5.5	V	
V_{IL} Low-Level Input Voltage All Inputs Except CLK CLK Input Only	 -0.3 -0.3	 0.6 0.5	 V	
I_{OH} High-Level Output Current		-2.0	mA	$V_O=V_{OH(MIN)}$
I_{OL} Low-Level Output Current		5.0	mA	$V_O=V_{OL(MAX)}$

4.4 DC Characteristics

Table 4-5. DC Characteristics (at Recommended Operating Conditions)

PARAMETER	ALL 5x86 CPUs		UNITS	NOTES
	MIN	MAX		
V_{OL} Output Low Voltage		0.45	V	I_{OL} = 5 mA
V_{OH} Output High Voltage	2.4		V	I_{OH} = -2 mA
I_I Input Leakage Current for all pins except those with internal pull-ups or pull-downs		±15	µA	$0 < V_{IN} < V_{CC}$, See Table 4-1
I_{IH} Input Leakage Current for all pins with internal pull-downs.		200	µA	V_{IH} = 2.4 V, See Table 4-1
I_{IL} Input Leakage Current for all pins with internal pull-ups.		-400	µA	V_{IL} = 0.45 V, See Table 4-1
I_{CC} Active I_{CC} 5x86-100 at f_{CLK} = 100 MHz 5x86-120 at f_{CLK} = 120 MHz	 0.9 TYP 1.0 TYP	 1.2 1.4	A	Note 1
I_{CCSM} Suspend Mode I_{CC} 5x86-100 at f_{CLK} = 100 MHz 5x86-120 at f_{CLK} = 120 MHz	 20 TYP 50 TYP	 75 75	mA	Notes 1, 3
I_{CCSS} Standby I_{CC} (Suspended and CLK Stopped)	15 TYP	60	mA	f_{CLK} = 0 MHz, Note 4
C_{IN} Input Capacitance		20	pF	f = 1 MHz, Note 2
C_{OUT} Output or I/O Capacitance		20	pF	f = 1 MHz, Note 2
C_{CLK} CLK Capacitance		20	pF	f = 1 MHz, Note 2

Notes:
1. f_{CLK} ratings refer to internal clock frequency.
2. Not 100% tested.
3. All inputs are at 0.4 or V_{CC} - 0.4 (CMOS levels). All inputs held are static except clock and all outputs are unloaded (static I_{OUT} = 0 mA). This specification is also valid for UP# = 0.
4. All inputs are at 0.4 or V_{CC} - 0.4 (CMOS levels). All inputs are held static and all outputs are unloaded (static I_{OUT} = 0 mA).

4.5 AC Characteristics

Tables 4-6 through 4-12 (Pages 4-7 through 4-12) list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figure 4-1 (Page 4-6) and Figure 4-2 (Page 4-7). The rising-clock-edge reference level V_{REF}, and other reference levels are shown in Table 4-6 below. Input or output signals must cross these levels during testing.

Figure 4-1 shows output delay (A and B) and input setup and hold times (C and D). Input setup and hold times are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

Table 4-6. Drive Level and Measurement Points for Switching Characteristics

SYMBOL	VOLTAGE (Volts)
V_{REF}	1.5
V_{IHD}	2.3
V_{ILD}	0

Note: Refer to Figure 4-1.

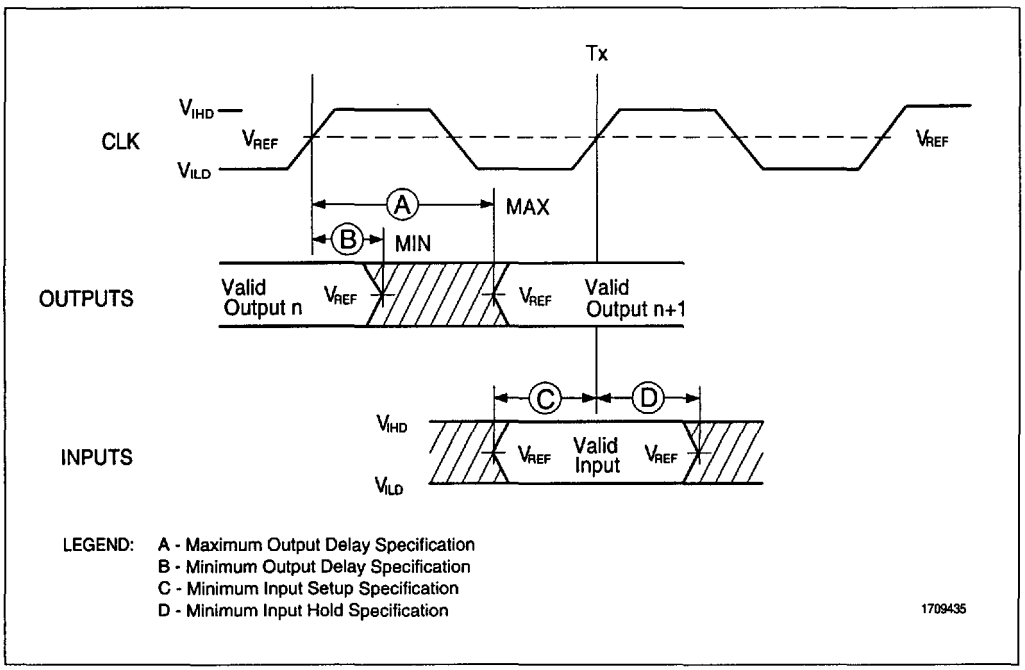

Figure 4-1. Drive Level and Measurement Points for Switching Characteristics

Table 4-7. Clock Specifications

T_{case} = 0 to 85 °C (See Figure 4-2)

	PARAMETER	5x86-100 33-MHz BUS		5x86-120 40-MHz BUS		5x86-100 50-MHz BUS		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
	CLK Frequency		33		40		50	MHz	
T1	CLK Period	30		25		20		ns	
T2	CLK Period Stability		± 250		± 250		± 250	ps	
T3	CLK High Time	11		9		7		ns	At 2 V
T4	CLK Low Time	11		9		7		ns	0.5 V
T5	CLK Fall Time		3		3		2	ns	2 to 0.5 V
T6	CLK Rise Time		3		3		2	ns	0.5 to 2 V

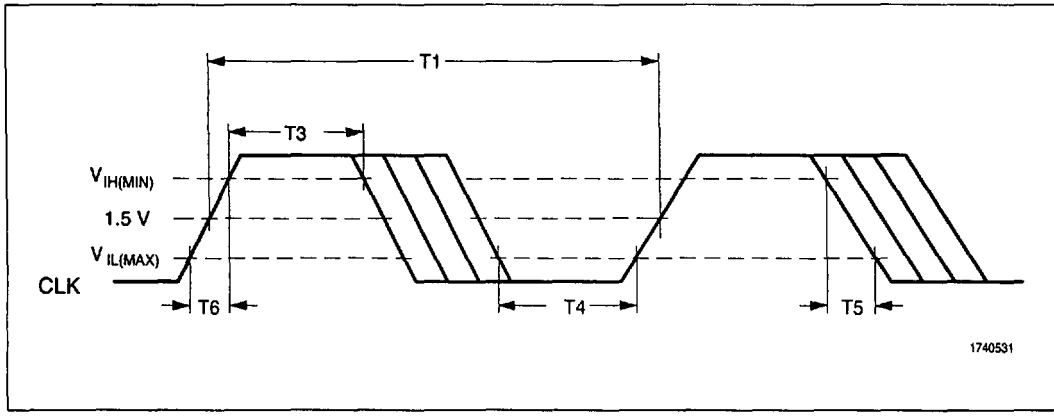

Figure 4-2. CLK Timing and Measurement Points

Table 4-8. Output Valid Delays

C_L = 50 pF, T_{case} = 0 to 85 °C (See Figure 4-3)

	PARAMETER	5x86-100 33-MHz BUS		5x86-120 40-MHz BUS		5x86-100 50-MHz BUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
T7	All output signals not listed below	3	14	3	14	2	12	ns
T7a	D31 - D0, DP3 - DP0	3	14	3	14	3	12	ns
T7b	A19 - A2	3	14	3	14	2	10.5	ns

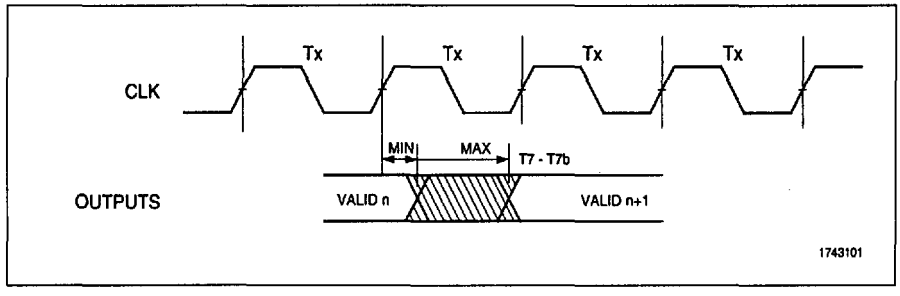

Figure 4-3. Output Valid Delay Timing

Table 4-9. Output Float Delays

C_L = 50 pF, T_{case} = 0 to 85 °C (See Figure 4-4)

	PARAMETER	5x86-100 33-MHz BUS		5x86-120 40-MHz BUS		5x86-100 50-MHz BUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
T8	All output signals.		20		19		18	ns

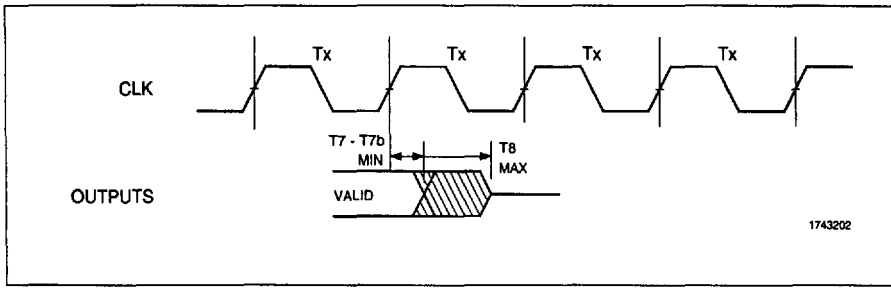

Figure 4-4. Output Float Delay Timing

Table 4-10. Input Setup Times

T_{case} = 0 to 85 °C (See Figure 4-5)

	PARAMETER	5x86-100 33-MHz BUS	5x86-120 40-MHz BUS	5x86-100 50-MHz BUS	UNITS
		MIN	MIN	MIN	
T9	All inputs not listed below	5	5	5	ns
T9a	HOLD, AHOLD	6	5	5	ns
T9b	BOFF#	7	6	5	ns
T9c	A31 - A4, D31 - D0, DP3 - DP0	5	5	4	ns

Table 4-11. Input Hold Times

T_{case} = 0 to 85 °C (See Figure 4-5)

	PARAMETER	5x86-100 33-MHz BUS	5x86-120 40 MHz-BUS	5x86-100 50-MHz BUS	UNITS
		MIN	MIN	MAX	
T10	All inputs	3	3	2	ns

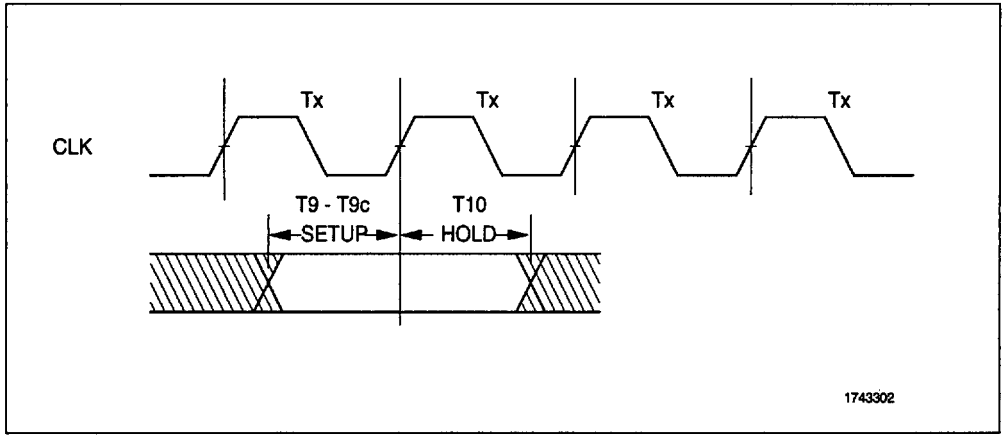

Figure 4-5. Input Setup and Hold Timing

Table 4-12. JTAG AC Specifications

SYMBOL	PARAMETER	ALL BUS FREQUENCIES		UNITS	FIGURE
		MIN	MAX		
	TCK Frequency (MHz)		25	ns	
T37	TCK Period	40		ns	4-6
T38	TCK High Time	10		ns	4-6
T39	TCK Low Time	10		ns	4-6
T40	TCK Rise Time		4	ns	4-6
T41	TCK Fall Time		4	ns	4-6
T42	TDO Valid Delay	3	25	ns	4-7
T43	Non-test Outputs Valid Delay	3	25	ns	4-7
T44	TDO Float Delay		30	ns	4-7
T45	Non-test Outputs Float Delay		36	ns	4-7
T47	TDI, TMS Setup Time	8		ns	4-7
T48	Non-test Inputs Setup Time	8		ns	4-7
T49	TDI, TMS Hold Time	7		ns	4-7
T50	Non-test Inputs Hold Time	7		ns	4-7

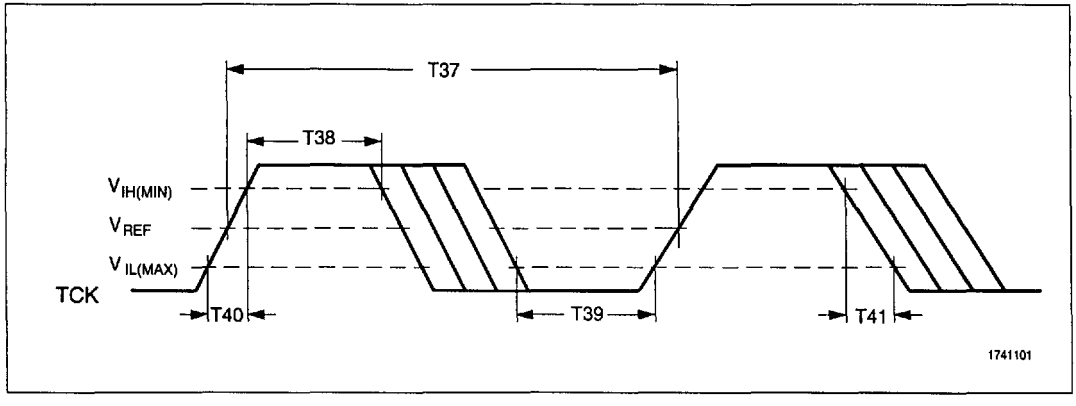

Figure 4-6. TCK Timing and Measurement Points

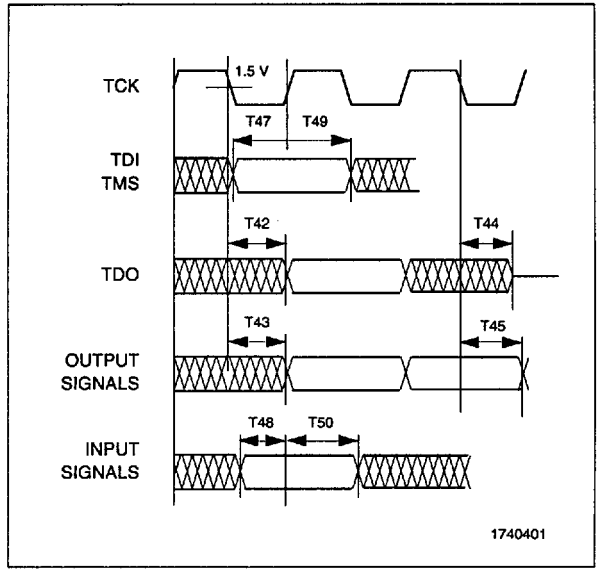

Figure 4-7. JTAG Test Timings