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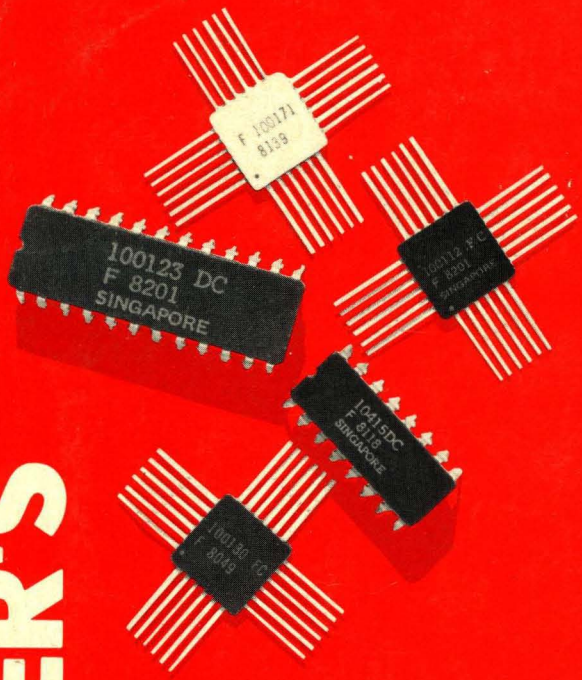

F100K ECL USER'S HANDBOOK

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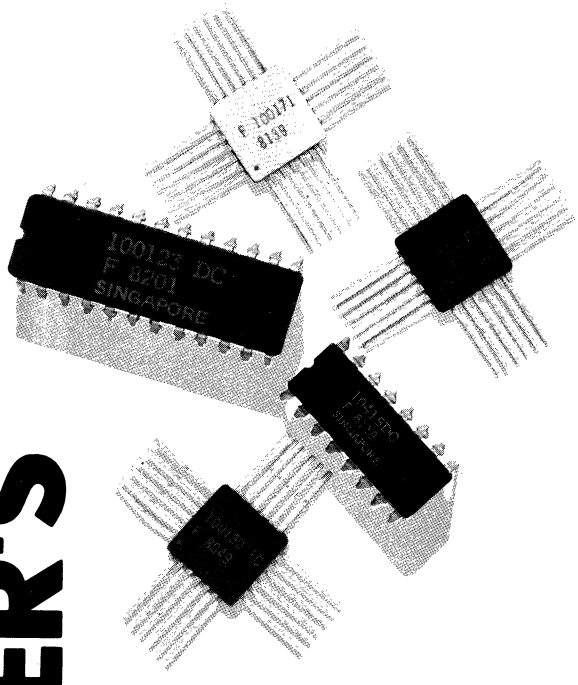
F100K ECL USER'S HANDBOOK



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Introduction

The F100K family was developed to meet the ever increasing demands of the data processing industry. After significant consultation with major segments of the data processing industry, it was determined that the faster processing rates, higher machine densities, and greater system reliability required by that industry could only be met by the use of higher speed integrated circuits with more on-chip integration and more multi-purpose logic functions; thus, F100K ECL.

In order to ensure F100K acceptance as a standard product family, major segments of the data processing industry were involved in its definition. The result is the F100K ECL product family, which provides next generation system performance and density without requiring the total use of LSI, but is still compatible with LSI approaches.

F100K gate arrays are not included in this user's handbook but will become an integral part of the F100K family. Please contact your local Fairchild sales office for information on F100K gate arrays.

Chapter 1 Family Overview
Discusses F100K design philosophy and actualization, and summarizes the key features and advantages in high-speed systems.

Chapter 2 Circuit Basics
Discusses internal circuitry and logic function formation. Also, a sample analysis of noise margins is outlined.

Chapter 3 Logic Design
Features brief applications of F100K logic arranged according to function.

Chapter 4 Transmission Line Concepts
Reviews the concepts of characteristic impedance and propagation delay and discusses termination, mismatch, reflections and associated waveforms.

Chapter 5 System Considerations
Extends the transmission line approach to the specific configurations, signal levels and parameter values of ECL. Various methods of driving and terminating signal lines are discussed.

Chapter 6 Power Distribution and Thermal Considerations
Discusses power supply, decoupling and system cooling requirements.

Chapter 7 Testing Techniques
Discusses various methods and techniques used in testing ECL devices (intended for those concerned with customer incoming inspection).

Chapter 8 Quality Assurance and Reliability
Gives an overview of the quality and reliability programs currently in use.

Chapter 9 Field Sales Offices and Distributor Locations

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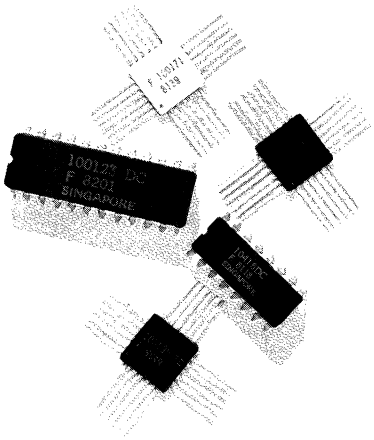


Chapter 1
Family Overview

1

- Introduction
- Design Philosophy
- Process Technology
- Compensation Network
- Characteristics
- System Aspects
- Features
- System Benefits
- Process Benefits
- Radiation Tolerance
- Packaging
- References

Introduction
Systems designers have found that Emitter Coupled Logic (ECL) circuits offer significant advantages to high-speed systems. These advantages include high switching rates with moderate power consumption, low propagation delays with moderate edge rates, and the ability to drive low impedance transmission lines.

The F100K ECL family is the realization of refinements made on ECL design to produce a family of logic components which are not only capable of providing ultimate performance for packaged SSI/MSI but which are easy to use and cost effective.

F100K ECL has been accepted as the standard subnanosecond logic family used in high-speed, next generation systems. The advance into complex LSI and gate arrays is fully supported by the F100K SSI/MSI parts.

Design Philosophy
F100K was designed to meet four key requirements: high speed at reduced power, high level of on-chip integration, flexible logic functions, and optimum I/O pin assignment.

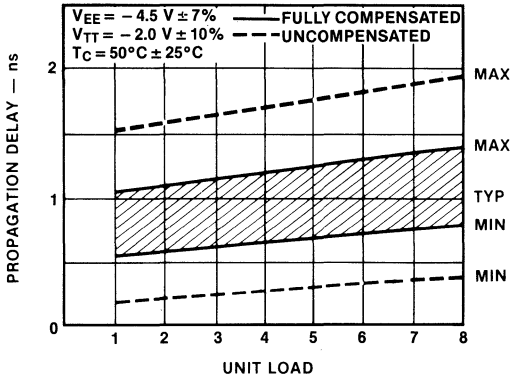
Subnanosecond Gate Delays
The subnanosecond internal gate delays of F100K are obtained by the use of ECL design techniques and the advanced Isoplanar II process. Many circuit approaches were carefully considered prior to selecting the optimum gate configuration for the F100K family. The emitter-follower current-switch (E^2CL) and current-mode logic (CML) gates were eliminated mainly because of poor capacitive drive and lack of output wired-OR capability; the CML gate has low noise margins. The 2-1/2D, EFL, DCTTL and hysteresis gates were eliminated due to the lack of simultaneous complementary outputs along with difficult temperature and voltage compensation characteristics that lead to the loss of system noise immunity.

The choice narrowed down to the current-switch emitter-follower ECL gate which offers the following characteristics:

- High fan-out capability
- Simultaneous complementary outputs
- Excellent ac characteristics
- Compatibility with existing ECL logic and memories
- Internal series gating capability
- Good noise immunity
- Amenable full compensation and extended temperature characteristics
- External wired-OR capability

In order to ease drive requirements all circuit inputs were designed to have similar loading characteristics; *i.e.,* buffers are incorporated where an input pin would normally drive more than one on-chip gate. The on-chip delay incurred by buffering is less than the system delay caused by an output which drives a capacitance of higher than three unit loads. Full compensation was selected for the F100K family to provide improved switching characteristics. Full compensation results in relatively constant signal levels and thresholds and in improved noise margins over temperature and voltage variations from chip to chip, and thus a tighter ac window in the system environment. A comparison of fully compensated ECL to conventional ECL shows a 2:1 improvement in system ac performance due solely to full compensation *(Figure 1-1).* And, the improved speed has been achieved at reduced power. This power reduction is accomplished by the use of advanced process technology that reduces parasitic capacitances and improves tolerances, by optimum circuit designs using series gating and collector and emitter dotting, and by designing for the use of a −4.5 V V_{EE} power supply. While a −5.2 V ± 10% power supply can be used to interface with 2 ns ECL families, F100K is only specified at a V_{EE} power supply of −4.2 V to −4.5 V.

Fig. 1-1 Comparison of Propagation Delays



High On-Chip Integration
Higher on-chip integration is made possible by using the 24-pin package to increase the number of signal pins by 62% over the conventional 16-pin package. The emphasis in F100K is to minimize the number of SSI functions and maximuze the use of MSI and LSI to reduce wiring delays and thus make more efficient use of the fast on-chip switching technology. Only 10 SSI functions are needed to serve the system needs presently requiring 25 functions in the ECL 10K family.

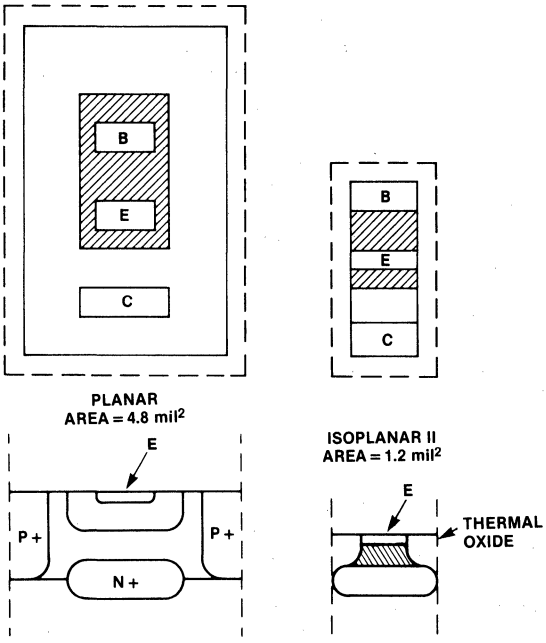
Flexibility and Pin Assignment
F100K was planned to minimize the total number of logic functions by increasing the flexibility of each function and by making use of more I/O pins. Since next-generation system performance and ease of system designs are major F100K goals, pin assignment is important and was planned to minimize crosstalk, noise coupling and feedthrough, to facilitate OR-ties and to ease power-bus routing. Some of the key considerations in selecting the F100K pin assignments were:

- Locate power pins in the center on opposite sides of the DIP package to ease system design and to provide low-inductance connections to the chip.
- Provide two V_{CC} pins, one for the internal circuit and one for the output buffers, to minimize noise coupling.
- Locate inverting outputs of logically independent gates adjacent to each other. This provides the ability to wire AND-OR-Invert functions with ease.
- Locate common pins such as common Reset and common Clock at pin number 22 and Address or control inputs at pins 19 and 20 for flatpaks. This is to maximize use of Computer Aided Design (CAD) for board layouts.
- When feasible, mode control pins are used to create multipurpose devices.

Process Technology
The F100K family is fabricated using the advanced Isoplanar II process, which provides transistors with very-high, well-controlled switching speeds, extremely small parasitic capacitances and f_T in excess of 5 GHz.

The technology can best be described by comparing the integrated circuit transistor structures of the conventional Planar process and that of the Isoplanar II process *(Figure 1-2)*. The top view shows the area needed for each structure; the dashed area is the center of the isolation area.

Fig. 1-2 Transistor Structures



In the Isoplanar process, a thick oxide is selectively grown between devices, instead of the P^+ region which is present in the Planar process. Since this oxide needs no separation from the base-collector regions, a substantial reduction in device and chip size can be realized. The base and emitter ends terminate in the oxide wall; therefore, the masks can overlap into the isolation oxide. This overlap feature means that base and emitter masking does not have to meet the extremely close tolerances that might otherwise be necessary, and standard photolithographic processes can be used.

The "walled emitter" structure allows over a 70% reduction of the transistor silicon area compared to that of a conventional Planar transistor. For a given emitter size, the collector-base area is also reduced by more than 60%. The reduced junction areas result in corresponding reductions in collector-base and collector-substrate capacitances, thereby allowing higher speeds.

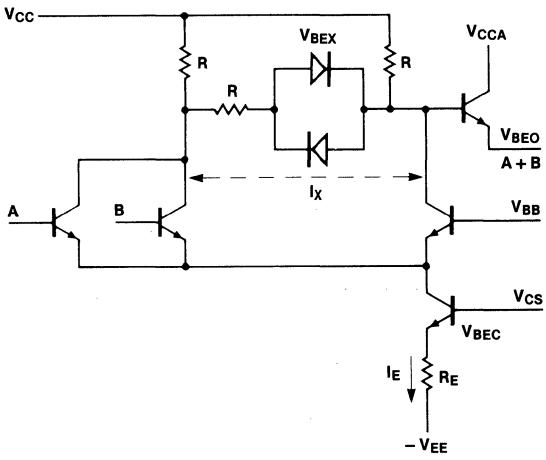
Since the active transistor area is only under the emitter, all capacitance and resistance values outside this area are reduced. Parasitic values are further reduced by taking advantage of the masking alignment latitude resulting from the self-aligning nature of the structure.

As is the case with other modern LSI processes, the shallower diffusions and thinner oxides make ECL devices more susceptible to damage from electrostatic discharge than are devices of earlier TTL families. Users should take the usual precautions when handling ECL devices: avoid placing them on non-conductive plastic surfaces or in plastic bags, make sure test equipment and fixtures are grounded, individuals should be grounded before handling the devices, etc.

Compensation Network

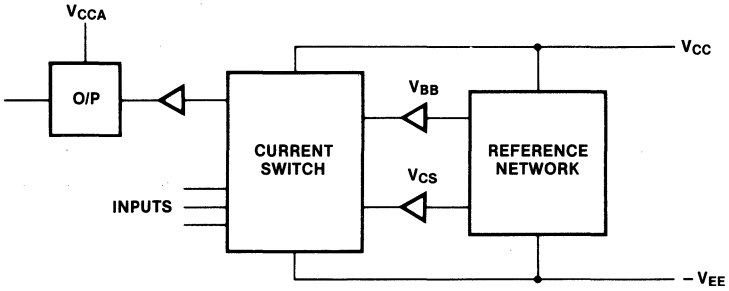
The heart of F100K is fully compensated ECL.[1] The basic gate consists of three blocks — the current switch, the output emitter-followers, and the reference or bias network *(Figure 1-3)*. The current switch allows both conjunctive and disjunctive logic. The output emitter-followers provide high drive capability through impedance transformation and allows for increased logic swing. The bias network sets dc thresholds and current-source bias voltages. Temperature compensation at the gate output is achieved by incorporating a cross-connect branch between the complementary collector nodes of the current switch and driving the current source with a temperature insensitive bias network[2] *(Figure 1-4)*.

Fig. 1-4 Temperature Compensation



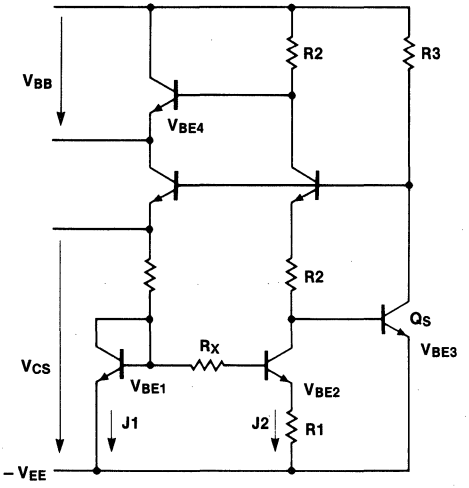
As junction temperature increases and the forward base-emitter voltage of the output emitter-follower decreases, the collector node of the current switch must become more negative. Since the current-source bias voltage, V_{CS}, is independent of temperature, the switch current increases with temperature due to the temperature dependence of V_{BEC}. The combination of temperature controlled current, I_E, and the cross-connect branch current, I_X, forces the proper temperature coefficient at the collector node of the current switch to null out the V_{BEO} tracking coefficient.[3]

Fig. 1-3 ECL Gate



The schematic for the reference network displays a V_{BE1} amplifier in the bottom left corner *(Figure 1-5)*. Two base-emitter junctions are operated at different current densities, J1 and J2. The resulting voltage difference, V_{BE1} minus V_{BE2}, appears across R1 and is amplified by the ratio R2/R1. Note that R2 is used twice, once to generate V_{CS} and once to generate V_{BB}. The different current densities, J1 and J2, result in a positive temperature tracking coefficient across R2, which cancels the negative diode-tracking coefficient of V_{BE3} and V_{BE4}. The V_{CS} and the V_{BB} thus generated are temperature insensitive at the extrapolated bandgap voltage of silicon[1,2] (approximately 1300 mV).[4] R_X in the V_{BE} amplifier compensates for process variations of β and ΔV_{BE}.[5] Voltage regulation is achieved through a shunt regulator shown at the right side of the schematic.

Fig. 1-5 Reference Network



Characteristics

F100K compatibility with existing ECL logic families and memories permits direct interface with slower logic families and ensures immediate memory availability. The typical logic swing is 800 mV *(Figure 1-6)* and all voltage levels are specified with a 50 Ω load to –2 V at all outputs to provide transmission line drive capability. However, the inherently low output impedance *(Figure 1-7)* and maximum specified output current, 50 mA, make 25 Ω drive possible at any or all outputs. Alternately, of course, higher termination impedances or other termination schemes are also useful.

Fig. 1-6 Transfer Characteristics

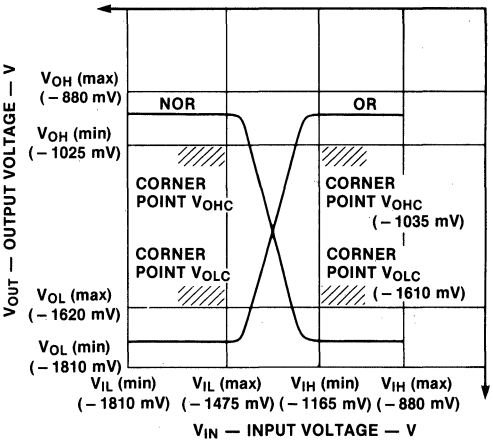
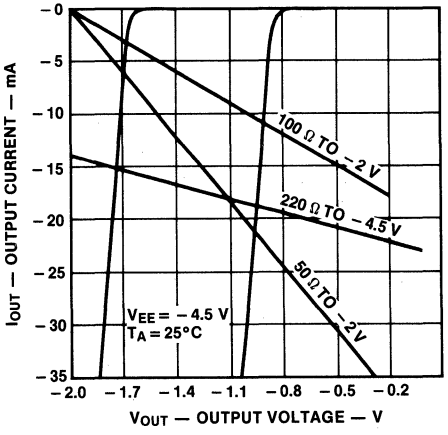
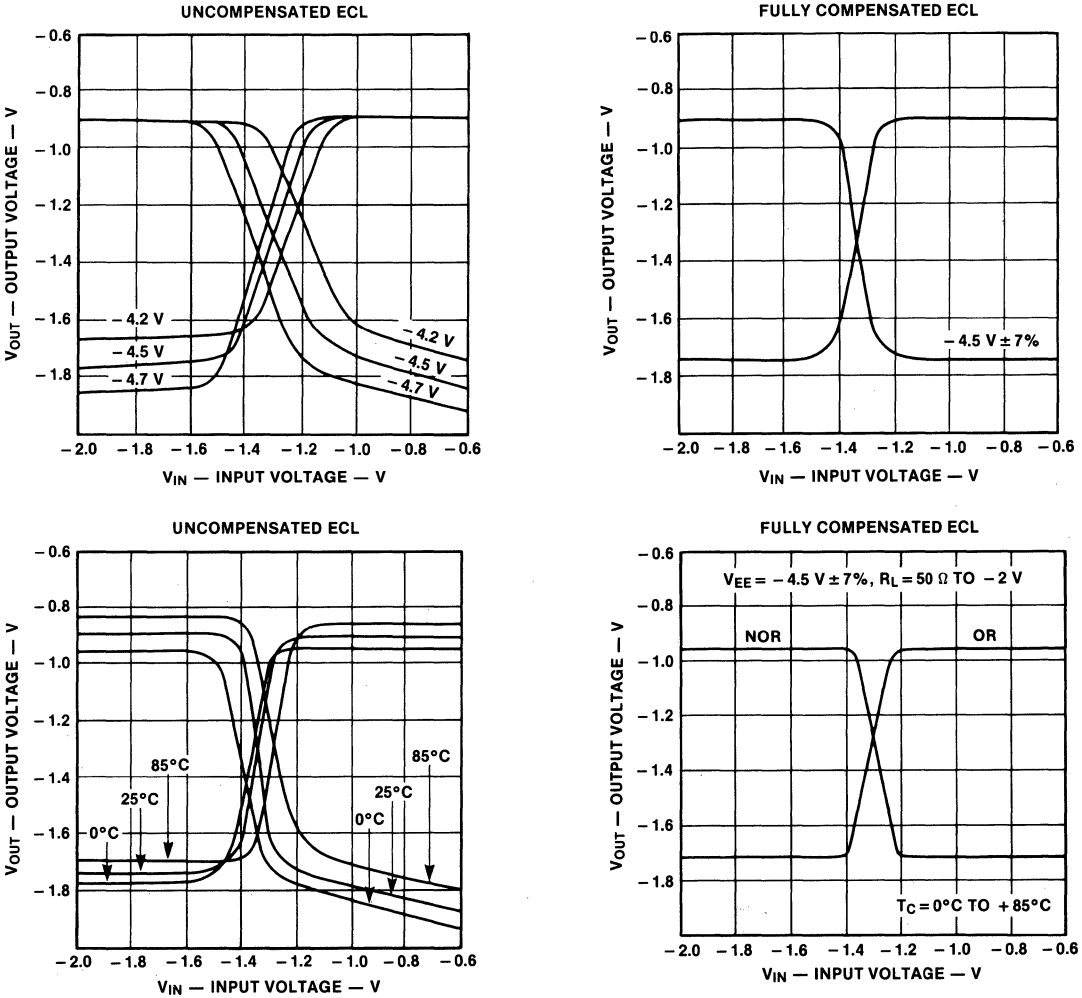


Fig. 1-7 Output Characteristic vs Output Terminations



F100K exhibits relatively constant output levels and thresholds over the 0°C to +85°C specified temperature range and –4.2 V to –4.8 V specified voltage range *(Figure 1-8)*. V_{EE} power supply current is also constant over the specified voltage range *(Figure 1-9)*; therefore:

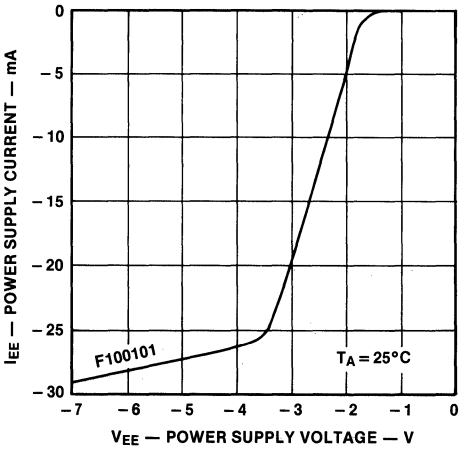
Fig. 1-8 Transfer Characteristics



- Propagation delay is relatively constant versus power supply voltage variations thus tightening the ac window.
- Power dissipation is a linear function of the supply voltage, reducing worst-case power consumption.

The typical propagation delay of an SSI gate function driving a 50 Ω transmission line is 0.75 ns, including package, with a power dissipation of 40 mW resulting in a speed-power product of 3 pJ. For optimized MSI functions, the internal gates can dissipate < 10 mW with average propagation delay of < 0.5 ns, giving a power-speed product of < 5 pJ.

Fig. 1-9 Change In I_{EE} vs Change In V_{EE}



F100K has a tighter ac window over the wide range of environmental conditions; thus, the system timing requirements are eased and maximum system clock rates are increased. At the sacrifice of ac performance, the small-signal input impedance was conservatively designed to be positive-real over the frequency range encountered by any circuit input. This provides adequate damping to insure ac stability within the system.

System Aspects

F100K provides high-density digital functions that outperform all other families on the market today. How does this increased circuit performance and higher on-chip density improve system performance?

Propagation delay and transition times vary (ac windows) when functions are operated at the extremes of the specified environmental ranges. With F100K, these variations are reduced and more predictable system timing is achieved. For synchronous machines and very high speed asynchronous systems, timing and its predictability are of utmost importance. Due to F100K constant supply current versus power supply voltage and because of nearly constant levels and thresholds with respect to temperature, voltage variations and gradients, speed skews are minimized.

Not only timing but also maximum system clock rate is affected by the tighter ac window. Thus, with F100K the system designer can use a higher speed value in his worst-case calculations. This can be translated into higher possible system clock rates. Therefore, a machine can perform at up to twice the frequency, solely due to the F100K compensation features. Noise immunity will be of utmost importance in next generation computers, since much of the noise generated within the system is inversely proportional to the switching transition time of the circuits. The F100K transition time is typically 0.7 ns as compared to 2.0 ns in other ECL families and should therefore increase system crosstalk by the same ratio.

F100K combats the increased system noise by maintaining a virtually invariant noise immunity with variations and gradients in power supply voltage, ambient and junction temperatures. The variation in junction temperatures is much larger than in earlier computer systems because of the mixture of LSI and SSI functions on the same boards.

Features

F100K ECL logic components are designed to be used in high-speed, low-noise systems and offer significant advantages over other logic families. Some of the important features and advantages are summarized below:

Low Propagation Delay

F100K ECL features gate delays which are typically 0.75 ns (750 picoseconds) with counters, registers and flip-flops operating in the 400 - 500 MHz range. When compared to other logic families such as Schottky TTL or slower ECL families, system performance can be doubled or tripled.

Moderate Edge Rates

Because of the nature of current mode switching which uses differential comparison techniques and avoids transistor storage delays, rise times can be controlled by internal time constants without sacrificing throughput delays. Slower rise times minimize ringing and reflections on interconnection wiring and simplify physical design. The typical edge rate for F100K ECL is 1 V/ns, only about 80% of the edge rate of Schottky TTL. It can be shown that for ECL circuits, the natural rise and fall times are approximately equal to the propagation delay. This relationship is considered optimum for use in high-speed systems.

Wired-OR Capability
ECL outputs can be wired together where wiring rules permit, to form the positive logic-OR function, thus achieving an extra level of gating at no parts count expense. Data bussing and party line operations are facilitated by this feature.

Complementary Outputs
A majority of F100K ECL logic elements have complementary outputs, providing numerous opportunities for reduction of package count and power consumption when mechanizing logic equations. Further, the system incurs no extra penalty in time delay since the complementary ECL outputs switch simultaneously.

A significant advantage to complementary outputs is that, since both the true and complement logic functions are available, I_{CC} imbalance can be minimized either by using both outputs in the design or merely terminating unused outputs. In this way, the constant current characteristic of ECL is not compromised and power supply noise is minimized.

Low Output Impedance, High Current Capacity
As operating speeds are increased to achieve the higher performance levels demanded of digital systems, ordinary wiring begins to exhibit distributed parameter characteristics, as opposed to a lumped capacitance nature at low speeds.

Characteristic impedances of normal wiring and printed circuit interconnections generally fall in the 50 to 250 Ω range. With these low impedance lines and fast transitions, the signals are attenuated by the voltage divider action between the circuit output impedance and the characteristic impedance of the interconnection.

Voltage mode circuits have a HIGH state output impedance of from 50 to 150 Ω and thus exhibit an output *stepped* characteristic, first reaching about 50% of final value and later reaching the final value in another *step.* F100K ECL output impedances under 10 Ω insure a complete, full valued, signal into a transmission line. Also, F100K ECL outputs are specified to drive a 50 Ω load (some devices are specified to drive a 25 Ω load). Outputs are capable of supplying 50 mA or more and can thus support the quiescent current required for passive terminations.

Convenient Data Transmission
The complementary high-current outputs of F100K ECL elements are well suited for driving twisted pair or other balanced lines in a differential mode, thereby enhancing field cancellation and minimizing crosstalk between subsystems.

High Common-Mode Noise Rejection
Differential line receivers provide common-mode noise rejection of 1 V or more for induced and ground noise. Differential receiving requires less signal swing than single ended and thus allows more reliable interpretation of low signal swings.

Constant Supply Current
The supply current drain of F100K ECL elements is governed by one or more internal constant current sources supplying operating current for differential switches and level shifting networks. Since the current drain is the same regardless of the state of the switches, F100K ECL circuits present constant current loads to power supplies *(see Complementary Outputs).*

Low Power Loss in Stray Capacitance
Energy is consumed each time a capacitor is charged or discharged so the energy loss rate, or power, goes up with switching frequency. Since the energy stored in a capacitor is proportional to the square of the voltage and F100K ECL signal swings are four to five times less than those of TTL, power loss in stray capacitance may be an order of magnitude less than that of TTL.

Low Noise Generation
In ECL systems, power supply lines are not subjected to the large current spikes common with TTL designs. Inherently, ECL is a constant current family without the totem-pole structures found in TTL circuits which generate the large current spikes. Since ECL voltage swings are much smaller than TTL, the current spikes caused by charging and discharging stray capacitances are much smaller with ECL than with TTL of comparable edge rates.

Low Crosstalk
Induced noise signals are proportional to signal swings and edge rates. The lower swing and slower edge rate of F100K ECL result in low levels of crosstalk.

System Benefits
The Fairchild F100K family offers improvements over other ECL families such as voltage and temperature compensation, higher integration levels, improved packaging, planned pinouts, lower propagation delay and more complementary outputs. These improvements cause measurable advantages to accrue to the design(er) of high-performance systems.

Easier Engineering
Designers have increased confidence that designs realized in F100K will operate with good margins over voltage and temperature variations in prototypes, production models and field installations. Less effort need be expended doing detailed voltage and temperature calculations and testing. With noncompensated ECL, noise margins cannot be guaranteed unless both the receiving and transmitting circuit operate at the same temperature and V_{EE}. This can cause a problem when attempting to transfer a breadboard or prototype system to production.

Since output swings and input thresholds remain almost constant over temperature and V_{EE} variations, complex control systems for power supply levels and more-than-adequate cooling are not necessary with F100K. This results in a more economical and better operating system.

Circuit Design
F100K ECL benefits from sound, well-engineered circuit designs. All input pins exhibit *positive/real* input impedance to eliminate system oscillations. Input buffering is used to reduce loads on lines which drive multiple internal gates.

High Performance
The regulation and control of dc and ac parameters achieved by F100K ECL assures that signal timing and propagation delays in critical paths are relatively insensitive to changes or gradients of temperature and supply voltage. Guardbands can be narrower, yet provide a higher degree of confidence due to the elimination of skew between output levels at one location and input thresholds at another.

The consistency of response and security of noise margins permit operation at higher clock rates and thus increase system performance.

Easier Debugging
With F100K, debugging of systems can proceed more rapidly than with uncompensated ECL. When a cabinet or enclosure is opened for access in debugging, the resultant change in thermal conditions has almost no effect on F100K signal swings, propagation delays, edge rates or noise margins.

Flexibility
F100K is designed to operate at −4.5 V for reduced power dissipation. If compatibility with other ECL families is a requirement, F100K will operate between −4.2 and −5.7 V due to the unique voltage compensation features. When operating at voltages other than −4.5 V, ac and dc parameters will vary slightly from specified values.

Fan-In/Fan-Out
All F100K ECL outputs are specified to drive 50 Ω transmission lines; this makes them suitable for driving very-high fan-out loads. In addition, some F100K outputs are specified to drive 25 Ω lines, which would be the case if a 50 Ω party-line bus terminated at both ends were being driven.

System Design
F100K ECL was designed to be the ultimate standard packaged IC logic family. System design constraints were considered and the F100K family was designed for overall ease of system design and use while making the maximum use of the very fast propagation delays available.

Process Benefits
F100K ECL SSI/MSI parts are made using the Isoplanar II process. This process makes possible subnanosecond logic delays and very tightly controlled switching characteristics.

Expansion of the F100K family will take place by moving into LSI functions of 500 to 4000 gates. The evolution of the Isoplanar II process will enable such growth and give much increased performance.

It is by moving into LSI that subnanosecond delays can be fully utilized and overall system performance increased with decreased power consumption and parts count.

Radiation Tolerance
F100K ECL manufactured using Isoplanar II processes is one of the most radiation-hard integrated circuit families in production. Radiation hardness can extend system lifetimes up to 50% in some applications requiring radiation tolerance. *(Reference Table 1.)*

Packaging
The initial package selected for the F100K is a 24-pin Flatpak, 0.375 inches square, with leads on 50-mil centers, 6 leads per side. This package was chosen because it offers minimum performance degradations of circuit and system and uses a somewhat conventional packaging technology. More common packaging such as the dual in-line packages, while available, do not provide optimum performance due to the loss in speed entering and leaving the package as well as a decrease in system density. With the F100K packaging technique and higher chip complexities within the family, the system density is two to three times higher than that possible with other available ECL families.

Table 1 Summary of Semiconductor Vulnerability Assessment

Radiation Environment	Bipolar Trans. & J-FET. Discretes	SCR	TTL	LSTTL	Analog IC	CMOS	NMOS	LED	ISO II ECL
Neutrons n/cm^2	10^{10}-10^{12}	10^{10}-10^{12}	10^{14}	10^{14}	10^{13}	10^{15}	10^{15}	10^{13}	> 10^{15}
Ionizing Total Dose Rads (Si)	> 10^4	10^4	10^6	10^6	5×10^4 10^5	10^3 10^4	10^3	> 10^5	10^7
Transient Dose Rate Rads (Si)/seconds (Upset or Saturation)		10^3	10^7	5×10^7	10^6	10^7	10^5		> 10^8
Transient Dose Rate Rads (Si)/seconds (Survival)	10^{10}	10^{10}	> 10^{10}	> 10^{10}	> 10^{10}	10^9	10^{10}	> 10^{10}	> 10^{11}
Dormant Total Dose (Zero Bias)	> 10^4	10^4	10^6	10^6	10^5	10^6	10^4	> 10^5	> 10^7

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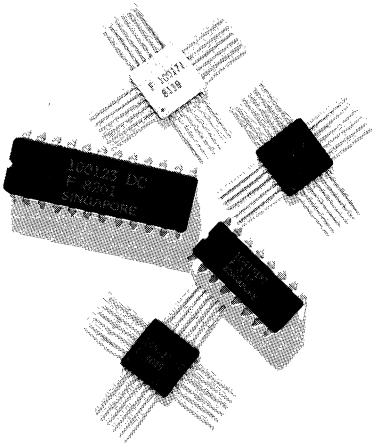


Chapter 2
Circuit Basics

Introduction

ECL circuits, except for the simplest elements, are schematically formidable and many of the specified parameters are relatively unfamiliar to system designers. The relationships between external parameters and internal circuitry are best determined by individually examining the fundamental subcircuits of a simple element. System variables such as supply voltage tolerances and temperature have predictable effects on circuit parameters, thus allowing a systematic evaluation of noise margins.

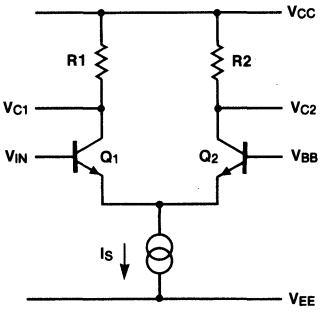
Basic ECL Switch

At the bottom of every ECL circuit, literally and figuratively, is a current source. In the basic ECL switch *(Figure 2-1)*, a logic operation consists of steering the current through either of two return paths to V_{CC}; the state of the switch can be detected from the resultant voltage drop across R1 or R2. The net voltage swing is determined by the value of the resistors and the magnitude of the current. Further, these two values are chosen to accomplish the charging and discharging of all of the parasitic capacitances at the desired switching rate.

Required Input Signal

The voltage swing required to control the state of the switch is relatively small due to the exponential change of emitter current with base-emitter voltage and to the differential mode of operation. For example, starting from a condition where the two base voltages are equal, which causes the current to divide equally between Q1 and Q2, an increase of V_{IN} by 125 mV causes essentially all of the current to flow through Q1. Conversely, decreasing V_{IN} by 125 mV causes essentially all of the current to flow through Q2. Thus the minimum signal swing required to accomplish switching is 250 mV centered about V_{BB}. The signal swing is made larger (approximately 750 mV) to provide noise immunity and to allow for differences between the V_{BB} of one circuit and the output voltage levels of another circuit driving it.

Fig. 2-1 Basic ECL Switch



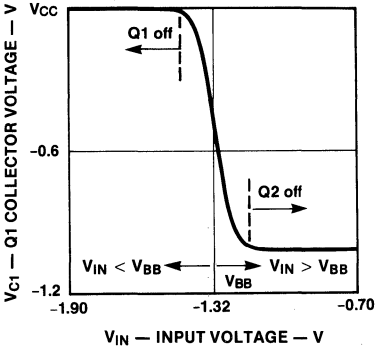
Transition Region

If the voltage at the collector of Q1 is monitored while varying V_{IN} above and below the value of V_{BB}, the relationship between V_{C1} and V_{IN} appears as shown in *Figure 2-2*. Note that the horizontal axis of the graph is centered on V_{BB}; this emphasizes the importance of V_{BB} in fixing the location of the transition region. The shape of the transition (or threshold) region is governed by the transistor characteristics and the value of current to be switched. Both of these factors are determined by the circuit designer. The shape of the transition region is essentially invariant over a broad range of conditions, due to the matching of transistor characteristics inherent with IC technology and because the transistors are at the same temperature. The inherent matching of IC resistors assures equal voltage swings at the two collectors.

Emitter-Follower Buffers

In *Figure 2-2*, V_{C1} ranges from V_{CC} (ground) when Q1 is off to approximately −0.90 V when Q1 is conducting all

Fig. 2-2 V_{C1}-V_{IN} Transition Region

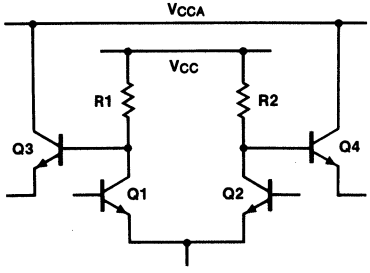


of the source current. To make these voltage levels compatible with the voltages required to drive the input of another current switch, emitter followers are added as shown in the buffered current switch *(Figure 2-3)*. In addition to translating V_{C1} and V_{C2} downward, the emitter followers also isolate the collector nodes from load capacitance and provide current gain. Since the output impedance of the emitter followers is low (approximately 7 Ω), ECL circuits can drive transmission lines—coaxial cables, twisted pairs, and etched circuits—having characteristic impedances of 50 Ω or more.

In this buffered current switch, the collectors of Q3 and Q4 return to a separate ground lead, V_{CCA}. This separation insures that any changes in load currents during switching do not cause a change in V_{CC} through the small but finite inductance of the V_{CCA} bond wire and package lead. Outside the package, the V_{CC} and V_{CCA} leads should be connected to the common V_{CC} distribution.

For internal functions of complex circuits where loading is minimal, the buffer transistors are scaled down to maintain high switching speeds with modest source currents. For service as output buffers, the emitter followers are designed for a maximum rated output current of 50 mA. For standardization of testing, detailed specifications on guaranteed min/max output levels apply when an output is loaded with 50 Ω returned to -2 V. The emitter followers have no internal pull-down resistors; consequently, there is maximum design flexibility when optimizing line terminations and using wired-OR techniques for combinatorial logic or data busing.

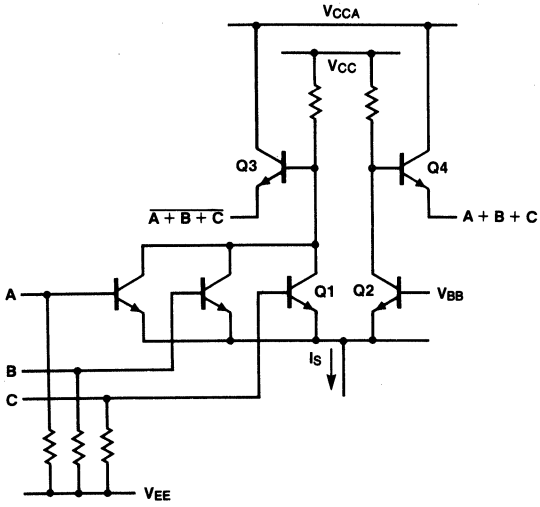
Fig. 2-3 Buffered Current Switch



Multiple Inputs

The buffered switch of *Figure 2-3* is essentially an ECL line receiver circuit with the bases of both Q1 and Q2 available for receiving differential signals. With one input connected to the V_{BB} terminal, the switch can receive a signal transmitted in a single-ended mode or it can act as a buffer or logic inverter. To perform the OR and NOR of two or more functions, additional transistors are connected in parallel with Q1 as indicated in *Figure 2-4*. When any input is HIGH, its associated transistor conducts the source current and Q2 is turned off; this causes the collector of Q1 to go LOW and the collector of Q2 to go HIGH, with the emitters of Q3 and Q4 following the collectors of Q1 and Q2 respectively. When two or more inputs are HIGH, the results are the same. Thus, with a HIGH level defined as a True or logic "1" signal, Q3 provides the NOR of the inputs while Q4 simultaneously provides the OR. In addition to the logic design flexibility afforded by the availability of both the assertion and negation, the Q3 and Q4 outputs can drive both conductors of a differential pair for data transmission. Also shown in *Figure 2-4* are the pull-down resistors, nominally 50 kΩ, connected between ECL inputs and the negative supply. These resistors serve the purpose of holding unused inputs in the LOW state by sinking I_{CBO} current and preventing the build-up of

Fig. 2-4 Input Expansion by Parallel Transistors



charge on input capacitances. Accordingly, most non-essential ECL inputs are designed to be active HIGH. When such inputs are not used, the pull-down resistors eliminate the need for external wiring to hold them LOW.

Power Conservation, Complementary Functions
Power dissipation in an ECL circuit is due in part to the output load currents and in part to the internal operating currents. Load currents depend on system design factors and are discussed in *Chapter 6*. In the basic switch *(Figure 2-1)*, power dissipation is fixed by the source current and the supply voltage, whether the circuit is in a quiescent or a transient state. There is no mechanism for causing a current spike such as occurs in TTL circuits, and thus the power dissipation is not a function of switching frequency.

A distinct advantage of the ECL switch is the ease of forming both the assertion and negation of a function without additional time delay or complexity. This is very significant in complex MSI functions, since it helps to maximize the efficiency of the internal logic while minimizing chip area and power consumption. Since most 100K ECL devices have complementary outputs, the system designer has similar opportunities to reduce package count and power consumption while enhancing logic efficiency and reducing throughput times.

Series Gating, Wired-AND
Quite often in ECL elements, the circuitry required to generate functions is much simpler than the detailed logic diagrams suggest. In addition to readily available complementary functions and the wired-OR option, other techniques providing high performance with low part count are series gating and wired collectors. These are illustrated in principle by the simplified schematics of *Figures 2-5* and *2-6*.

In *Figure 2-5*, if both A and B are HIGH, then Q1 and Q3 conduct and I_S flows through R1, making the collector of Q1 go LOW, thereby achieving the NAND of A and B. Connecting the collectors of Q2 and Q4 to the same load resistor provides the AND of A and B. If the collectors of Q3 and Q4 were interchanged, a different pair of functions of A and B would be produced. Similarly, a third functional pair is achieved by interchanging the collectors of Q1 and Q2. For Q3 and Q4 to operate at a lower voltage level than Q1 and Q2, the voltage level of B is translated downward from the normal ECL levels and V'_{BB} is similarly translated downward from the V_{BB} voltage. In the slightly more complex circuit in *Figure 2-6*, another pair of transistors is added to obtain the Exclusive-OR and Exclusive-NOR functions.

Connecting transistors in series is not limited to two levels of decision making; three levels are shown in the simplified schematic of an octal decoding tree *(Figure 2-7)*. If the three input signals are all HIGH, Q1 conducts through Q9 and Q13 to make the collector of Q1 LOW. In all, there are eight possible paths through which the source current can return to the positive supply. A LOW signal at the collector of any one of the transistors in the top row represents a unique

Fig. 2-5 Series/Parallel Gating

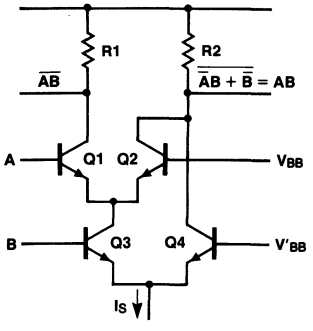
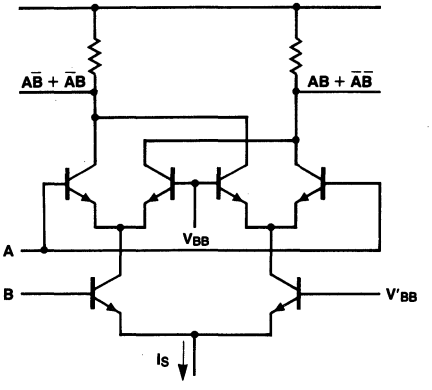


Fig. 2-6 Exclusive-OR/NOR



combination of the three input signals. This 1-of-8 decoding circuit illustrates very clearly how ECL design techniques make the most efficient use of components and power to generate complex functions. This same set of switches, with the upper collectors wired in two sets of four collectors each, generates the binary sum and its complement of the three input signals.

The Current Source, Output Regulation

All elements of the F100K circuits use a transistor current source illustrated in *Figure 2-8*. Source current is determined by an internally generated reference voltage V_{CS}, the emitter resistor R_S and the base-emitter voltage of Q5. The reference voltage is designed to remain fixed with respect to the negative supply V_{EE}, which makes I_S independent of supply voltage.

Regulating the current source (I_S) simplifies system design because output voltage and switching parameters are not sensitive to V_{EE} changes. Output voltage levels are determined primarily by the voltage drops across R1 and R2 resulting from the collector currents of Q1 and Q2. Since the collector current of the conducting transistor (Q1 or Q2) is determined by I_S and the transistor α, the voltage drop across the collector load resistor is not sensitive to V_{EE} variations. For example, a 1 V change in V_{EE} changes the output level V_{OL} by only 30 mV.

Switching parameters are affected by transistor characteristics, the collector resistor (R1 or R2), stray capacitances, and the amount of current being switched. In other forms of ECL where source currents change with V_{EE}, switching parameters are directly affected. This sensitivity is essentially eliminated in F100K circuits by regulating I_S against V_{EE} changes.

Power dissipation in an ECL switch is the product of I_S and V_{EE}. By holding I_S constant with V_{EE}, incremental changes in dissipation are linear with V_{EE} changes. In non-regulated ECL, I_S increases with V_{EE} causing switch dissipation to change more rapidly with V_{EE}.

Threshold Regulation

As previously discussed, the input threshold region of an ECL switch is centered on the internal reference V_{BB}. In F100K circuits, the on-chip bias driver holds V_{BB} constant with respect to V_{CC}, thus minimizing changes in input thresholds with V_{EE}. For a V_{EE} change of 1 V, for example, V_{BB} changes by approximately 25 mV.

With output voltage levels and input thresholds regulated, F100K circuits tolerate large differences in V_{EE} between a driving and a receiving circuit and still maintain good noise margins. For example, a driving circuit operated with -4.2 V and receiving circuit operated with -5.7 V experience a LOW state noise margin loss of only 30 to 40 mV compared to the ideal case of both circuits with V_{EE} = -4.5 V. This insensitivity to V_{EE} simplifies the design of system power distribution and regulation.

Fig. 2-7 Octal Decoding Tree

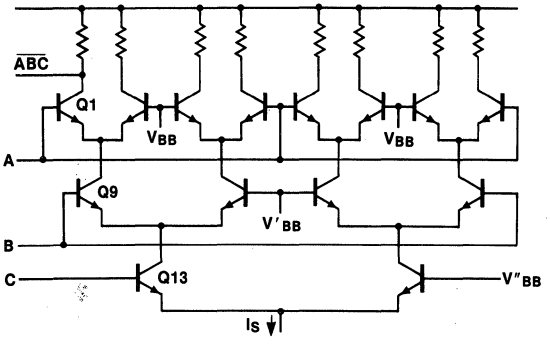
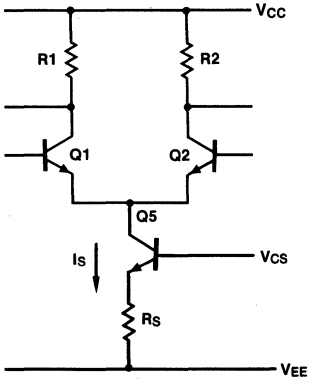


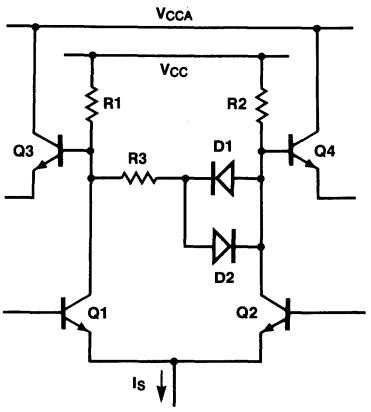
Fig. 2-8 Constant Current Source for a Switch



Temperature Compensation

In F100K circuits, input thresholds are made insensitive to temperature by regulating V_{BB}. Output voltage levels are made insensitive to temperature by a correction factor designed into the current source and by a simple network connected between the bases of the output transistors as shown in *Figure 2-9.*

Fig. 2-9 Temperature Compensation



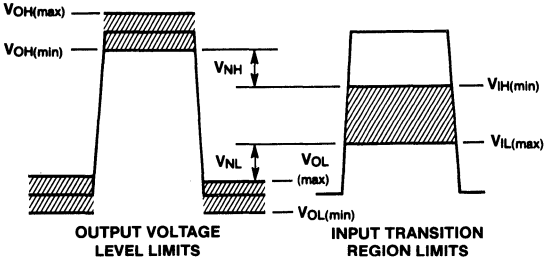
With Q1 conducting and Q2 off, most of the source current flows through R1, while a small amount flows through R2, D1 and R3. If the chip temperature increases, the source current is made to increase, causing an increase in the voltage drop of sufficient magnitude across R1 to offset the decrease in base-emitter voltage of Q3. The voltage drop across R1 increases with temperature at the rate of approximately 1.5 mV/°C, while the voltage drop across D1 decreases at the same rate. This means that there is a net voltage increase of 3 mV/°C across the series combination of R2 and R3. This increase is equally divided between the two resistors since R3 is equal to R2 (and R1); thus the voltage at the base of Q4 goes negative by 1.5 mV/°C, offsetting the decrease in the base-emitter voltage of Q4. When Q2 is on and Q1 is off, the same relationships apply except that most of the current flows through R2, and D2 conducts instead of D1. F100K change rates for V_{OH}, V_{BB}, and V_{OL} are approximately 0.06, 0.08 and 0.1 mV/°C, respectively.

The stabilization of output levels against changes in temperature provides significant advantages to both the user and manufacturer. In testing, an extended thermal stabilization period is not required, nor is an elaborate air cooling arrangement necessary to obtain correlation of test results between user and supplier. In a system, the output signal swing of a circuit does not depend on its temperature, therefore temperature differences do not cause a mismatch in signal levels between various locations. With temperature gradients thus eliminated as a system constraint, the design of the cooling system is greatly simplified.

Noise Margins

The most conservative values of ECL noise margins are based on the dc test conditions and limits listed on the data sheets. Acceptance limits on V_{OH} and V_{OL} are identified on a symbolic waveform in *Figure 2-10,* with the boundaries of the input threshold region also identified. The HIGH-state noise margin is usually defined as the difference between $V_{OH(min)}$ and $V_{IH(min)}$, with the LOW-state margin defined as the difference between $V_{OL(max)}$ and $V_{IL(max)}$. These two differences are identified as V_{NH} and V_{NL} respectively. The worst case input and output test points are also identified on the OR gate transfer function shown in *Figure 2-11.* The transition region indicated by the solid line is applicable when the internal reference V_{BB} has the design center value of -1.32 V for F100K circuits. The transition regions indicated by the dashed lines represent the lot-to-lot displacement resulting from the normal production tolerances on V_{BB}, which amount to ± 40 mV for F100K circuits. Using F100K circuit values as an example, the dashed curve on the right correlates with a V_{BB} value of -1.280 V, and the input test voltage $V_{IH(min)}$ is -1.165 V, for a net difference of 115 mV. Similarly, the dashed curve on the left applies when V_{BB} is -1.360 V with

Fig. 2-10 Identifying Specification Limits on Input and Output Voltage Levels



$V_{IL(max)}$ specified as −1.475 V, which also gives a net difference of 115 mV. The points V_{OHC} and V_{OLC} are commonly referred to as the *corner points* because of their location on the transfer function of worst case circuits.

In actual system operation, the noise margins V_{NH} and V_{NL} are quite conservative because of the way $V_{IH(min)}$ and $V_{IL(max)}$ are defined. From the transfer function of *Figure 2-11,* for example, $V_{IH(min)}$ is defined as a value of input voltage which causes a worst-case output to decrease from $V_{OH(min)}$ to V_{OHC}. This change in V_{OH} amounts to only 10 mV for F100K circuits. Thus, if a worst case OR gate has a quiescent input of $V_{OH(min)}$, a superimposed negative-going disturbance of amplitude V_{NH} causes an output change of only 10 mV, assuming that the time duration of the disturbance is sufficient for the OR gate to respond fully. In contrast, a system fault does not occur unless the superimposed noise at the OR input is of sufficient amplitude to cause the output response to extend into the threshold region(s) of the load(s) driven by the OR gate. In general, noise becomes intolerable when it propagates through a string of gates and arrives at the input of a regenerative circuit (flip-flop, counter, shift register, etc.) with sufficient amplitude to reach the V_{BB} level.

The critical requirement for propagating either a signal or noise through a string of gates is that each output must exhibit an excursion to the V_{BB} level of the next gate in the string, assuming, of course, that the time duration is sufficient to allow full response. If the excursion at the input of a particular gate either falls short or exceeds V_{BB}, the effect on its output response is magnified by the voltage gain of the gate. On the voltage transfer function of a gate, the slope in the transition region is not, strictly speaking, constant. However, for input signal excursions of about ±50 mV on either side of V_{BB}, a value of 5.5 may be used for the voltage gain. For example, if the noise (or signal) excursion at the input of a gate falls short of V_{BB} by 20 mV, the gate output response is 110 mV less. Another useful relationship is that if the input voltage of a gate is equal to V_{BB}, the output voltage is also equal to V_{BB}, within perhaps 30 mV.

To determine the combined effects of circuit and system parameters on noise propagation through a string of gates, refer to *Figure 2-12.* The voltages V_1 and V_2 represent differences in ground potential, while V_3 and V_4 are V_{EE} differences. The output of gate A is in the quiescent LOW state and V_{PL} is a positive-going disturbance voltage. Now, how large can V_{PL} be without causing propagation through gate C? For a starting point, assume all three gates are identical with typical parameters; V_{EE} is −4.5 V, the ground drops are zero, and there are no temperature gradients. Voltage parameters of F100K circuits are used. With typical

Fig. 2-11 Location of Test Points and Threshold on a Transfer Function

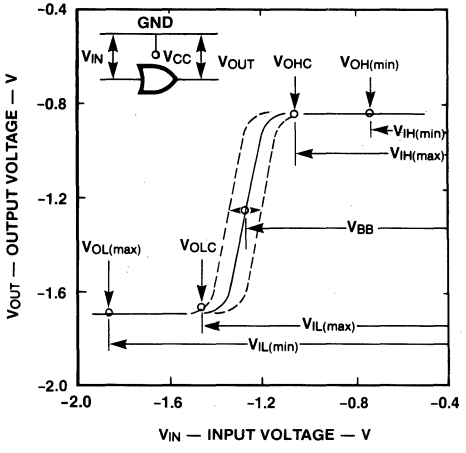
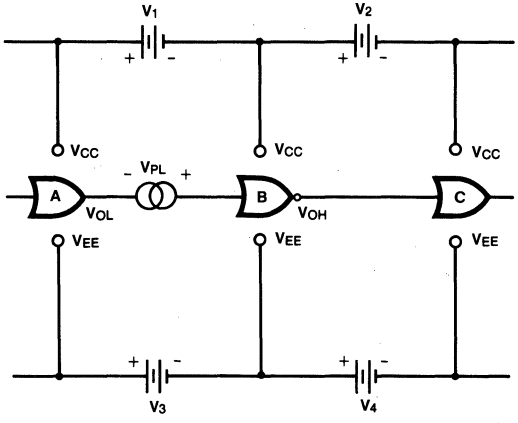


Fig. 2-12 Arrangement for Noise Propagation Analysis



circuits and the idealized environment, the maximum tolerable value of V_{PL} for propagation is the difference between the nominal V_{BB} of -1.320 V and nominal V_{OL} of -1.705 V, or 385 mV. The following steps treat each non-ideal factor separately and the required reduction in V_{PL} is calculated.

Non-typical V_{BB} of gate B. Specifications provide for V_{BB} variations of ±40 mV. If the V_{BB} of gate B is 40 mV more negative than nominal, V_{PL} must be reduced by the same amount.

$$\Delta V_{PL} = -40 \text{ mV}$$
$$V_{PL} = 385 - 40 = 345 \text{ mV}$$

Non-typical V_{OL} of gate A. V_{OL} limits are -1.620 V to -1.810 V corresponding to the $\pm 3\sigma$ points on the distribution. Statistically, this means that 98% of the circuits have V_{OL} values of -1.650 V or lower. Since this value differs from the nominal V_{OL} by 55 mV, V_{PL} must be reduced accordingly.

$$\Delta V_{PL} = -55 \text{ mV}$$
$$V_{PL} = 345 - 55 = 290 \text{ mV}$$

Difference in ground (V_{CC}) potential between gates A and B. Since the V_{CC} lead of gate B is the reference potential for input voltages, V_1 in the polarity shown effectively makes the V_{OL} of gate A more positive. Minimizing ground drops is one of the system designer's tasks *(Chapter 6)* and its effect on noise margins emphasizes its importance. For this analysis, a value of 30 mV is assumed.

$$\Delta V_{PL} = 30 \text{ mV}$$
$$V_{PL} = 290 - 30 = 260 \text{ mV}$$

Difference in V_{EE} between gates A and B. In the polarity shown, V_3 reduces the supply voltage for gate A since it is assumed that gate B has V_{EE} of -4.5 V. The indicated polarities of V_1 and V_3 seem to be in conflict if it is assumed that V_3 represents only ohmic drops along the V_{EE} bus. Since V_3 may, however, be caused by the use of different power supplies or regulators as well as by ohmic drops, the polarities may exist as indicated. In any actual situation, the designer can usually predict the directions of supply current flow by observation of the physical arrangement. As mentioned earlier, a 1 V change in V_{EE} causes a V_{OL} change 30 mV, or 3%. Assuming a value of 0.5 V for V_3 and adding the 30 mV of V_1, the net reduction in supply voltage for gate A is 0.53 V. Using 3% of this reduction as the change in V_{OL} gives a positive V_{OL} shift of 16 mV, which is a reduction of noise margin.

$$\Delta V_{PL} = -16 \text{ mV}$$
$$V_{PL} = 260 - 16 = 244 \text{ mV}$$

If the net supply voltage of gate A is assumed to be -4.5 V, then V_1 and V_3 cause gate B to have a greater supply voltage. This, in turn, causes the V_{BB} of gate B to go more negative at the rate of 25 mV/V of V_{EE} change, or 2.5%. Thus, for the same values of V_1 and V_3, the required reduction of V_{PL} is only 13 mV instead of the 16 mV computed above.

Non-typical V_{BB} of gate B. This was considered earlier for its effect at the input of gate B. It must also be considered for its effect on the excursions of the output voltage of gate B. Since the net input voltage of gate B ($V_{OL} + V_{PL}$) reaches the V_{BB} level of gate B, the output excursion also extends to the V_{BB} level and perhaps 30 mV beyond (more negative). This means that the output excursion of gate B could be 90 mV more negative than the nominal V_{BB} of gate C. This excess excursion must be divided by the voltage gain of gate B to determine exactly how much V_{PL} must be reduced as compensation.

$$\Delta V_{PL} = -90/5.5 = -16 \text{ mV}$$
$$V_{PL} = 244 - 16 = 228 \text{ mV}$$

Non-typical V_{BB} of gate C. The V_{BB} of gate C could be 40 mV more positive than the nominal value of -1.320 V. Dividing by the voltage gain of gate B gives the necessary reduction of V_{PL}.

$$\Delta V_{PL} = -40/5.5 = -7 \text{ mV}$$
$$V_{PL} = 228 - 7 = 221 \text{ mV}$$

Difference in V_{CC} potential between gates B and C. For the polarity shown, V_2 makes the net voltage at the C input more negative with respect to the V_{CC}

lead of gate C. Assume 30 mV for V_2 as was done for V_1.

$\Delta V_{PL} = -30/5.5 = -5.0\ mV$
$V_{PL} = 217 - 5 = 212\ mV$

Difference in V_{EE} between gates B and C. In the polarity shown, V_4 reduces the supply voltage for gate C, as does V_2. As previously mentioned, V_{BB} changes with V_{EE} at a rate of 25 mV/V, or 2.5%. Assuming a value of 0.5 V for V_4, as was done for V_2, adding V_2 gives a net V_{EE} reduction of 0.53 V. This makes the V_{BB} of gate C about 13 mV more positive, with respect to its own V_{CC} lead. This must be divided by the gain of gate B to determine the effect on the permissible value of V_{PL}.

$\Delta V_{PL} = -13/5.5 \simeq -2\ mV$
$V_{PL} = 212 - 2 = 210\ mV$

At this point the more conservatively defined V_{NL} *(Figure 2-10)* should be evaluated and compared with V_{PL}. Subtracting the values of $V_{OL(max)}$ and $V_{IL(max)}$, a value of 145 mV for V_{NL} is obtained.

The primary advantage of using V_{NH} and V_{NL} as the limits of tolerable noise is that they provide for simultaneous appearance of noise on inputs and outputs. Whatever the system designer's preference regarding noise margin definitions, the important factor is to recognize that the ΔV_{CC} and ΔV_{EE} between devices decrease the noise margins and therefore should be minimized.

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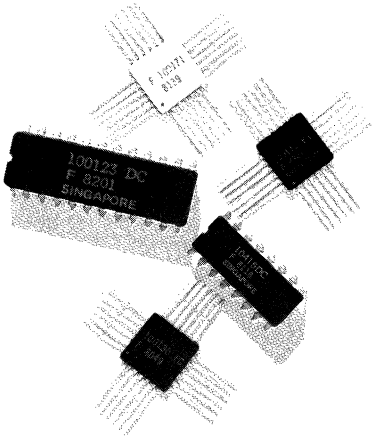


Chapter 3
Logic Design

- Introduction
- OR/NOR Gates
- Wired-OR Function
- AND Function
- OR-AND, OR-AND-Invert Gates
- Exclusive-OR/Exclusive-NOR Gate
- Flip-flops and Latches
- Counters
- Shift Registers
- Multiplexers
- Decoder
- Register File
- Comparators
- Parity Generator/Checker
- Arithmetic Logic Unit
- Multipliers
- TTL/100K Interfacing
- F10K/F100K Interfacing

Introduction

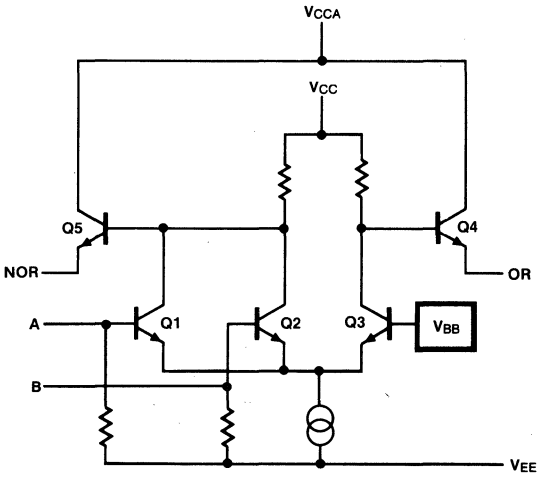
The F100K family comprises SSI, MSI, LSI, gate arrays, RAMs and PROMs. This chapter covers basic gates and flip-flops, as well as applications using MSI. Gate arrays and LSI are covered in separate publications and memory applications are included in the Bipolar Memory Data Book.

Fairchild F100K ECL logic symbols use the positive logic or "active-HIGH" option of MIL-STD-806B. Logic '1' is the more positive voltage, nearest ground (typically -0.955 V). Logic '0' or "active LOW" is the more negative level, nearest V_{EE} (typically -1.705 V).

OR/NOR Gates

The most basic F100K ECL circuit is the OR/NOR gate *(Figure 3-1)*. If the input (A or B) voltages are more negative than the reference voltage V_{BB}, Q1 and Q2 are cut off (non-conducting) and Q3 conducts, holding the collector of Q3 LOW. Since the base of Q4 is LOW, the pull-down resistor or terminator connected to its emitter makes the OR output LOW. The base of Q5 is HIGH (near ground) and its emitter pulls the NOR output HIGH. If either input is more positive than V_{BB}, Q1 or Q2 conducts and Q3 is cut off. This makes the base of Q4 HIGH, resulting in a HIGH at the OR output. At the same time, the base of Q5 is LOW and the pull-down resistors or terminator pulls the NOR output LOW. Detailed information concerning F100K ECL circuit basics may be found in *Chapter 2*.

Fig. 3-1 Basic ECL Gate



The F100K family includes two OR/NOR-gate devices. The F100101 is a triple 5-input OR/NOR and the F100102 is a quint 2-input OR/NOR with common enable. One element of the F100102 is shown in *Figure 3-2;* the corresponding truth table is *Table 3-1*.

Fig. 3-2 F100102 OR/NOR Gate

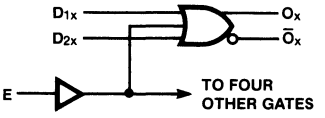


Table 3-1 F100102 Truth Table

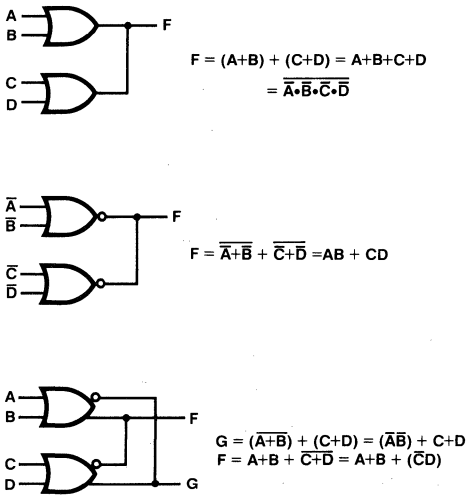
D_{1x}	D_{2x}	E	O_x	$\bar{O}_x$
L	L	L	L	H
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level

Wired-OR Function

A wired-OR function can be implemented simply by connecting the appropriate outputs external to the package (see *Figure 3-3*). Each output is buffered so that the internal logic is not affected by the wire-OR. This is a positive logic OR, not to be confused with a DTL wired- AND or the internal series gating used for some ECL functions. This wired-OR is especially useful in implementing data busses. For further information see *Chapter 5*.

Fig. 3-3 Wired-OR Function

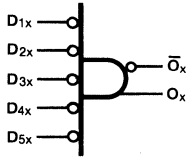


AND Function

The positive logic AND function is not directly available in F100K ECL. There are two approaches which can be taken to solve the problem of implementing an AND.

The first solution is indicated in *Figure 3-4*. A positive logic OR gate can be redrawn as a negative logic AND gate. To take advantage of this requires active-LOW input terms; but, since practically every F100K circuit provides complementary outputs, this should not be a problem.

Fig. 3-4 F100101 Redrawn as AND/NAND Gate



The second possible solution is to use devices in a manner other than that intended, at the cost of package efficiency. The F100117 may be used as a triple 3-input AND/NAND by connecting only one input on each of the OR gates. The F100179 may be used as a single 9-input AND gate by connecting the inputs to $\overline{C}_n$ and $\overline{G}_7$ through $\overline{G}_0$. The $\overline{P}_n$ inputs are left open (LOW) and the output is taken from $\overline{C}_{n+8}$.

OR-AND, OR-AND-Invert Gates

The F100117 is a triple 2-wide OR-AND, OR-AND-Invert Gate. The logic diagram and truth table for one section of the F100117 are shown in *Figure 3-5* and *Table 3-2*, respectively. The F100118 5-wide OA/OAI has OR inputs of 5, 4, 4, 4, and 2.

Fig. 3-5 F100117 OA/OAI Gate

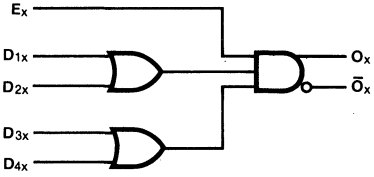


Table 3-2 F100117 Truth Table

E_x	D_{1x}	D_{2x}	D_{3x}	D_{4x}	O_x	$\overline{O}_x$
H	H	X	H	X	H	L
H	X	H	X	H	H	L
X	L	L	X	X	L	H
X	X	X	L	L	L	H
L	X	X	X	X	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Exclusive-OR/Exclusive-NOR Gate

The F100107 is a quint exclusive OR/NOR gate. In addition to providing the exclusive-OR/exclusive-NOR of the five input pairs, a comparison output is available. If the five pairs of inputs are identical, bit by bit, then the common output will be LOW.

Flip-Flops and Latches

Flip-flops and latches are treated together due to their similarity. The only difference is that latch outputs follow the inputs whenever the enable is LOW, whereas a flip-flop changes output states only on the LOW-to-HIGH clock transition.

The advantage of an edge-triggered flip-flop is that the outputs are stable except while the clock is rising; a latch has better data-to-output propagation delay while the enable is kept active.

Both latches and flip-flops are available three to a package with individual as well as common controls and six to a package with only common controls. There are a total of four parts as indicated below.

	Triple w/Individual Controls	Hex w/Common Controls
Flip-flops	F100131	F100151
Latches	F100130	F100150

Figure 3-6 shows the equivalent logic diagram of 1/3 of an F100131. The internal clock is the OR of two clock inputs, one common to the other two flip-flops. The OR clock input permits common or individual control of the three flip-flops. In addition, one input may be used as a clock input and the other as an active-LOW enable.

When the clock is LOW, the slave is held steady and the information on the D input is permitted to enter the master. The transition from LOW to HIGH locks the master in its present state making it insensitive to the D input. This transition simultaneously connects the slave to the master, causing the new information to appear at the outputs. Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master/slave changes when the clock has slow rise or fall times.

The Clear and Set Direct for each flip-flop are the OR of two inputs, one common to the other two flip-flops. The output levels of a flip-flop are unpredictable if both the Set and Clear Direct inputs are active.

The outputs of all F100K flip-flops and latches are buffered. This means that they can be OR-wired; noise appearing on the outputs cannot affect the state of the internal latches.

Table 3-3 is the truth table for the F100131 flip-flop. The truth table for the F100130 latch is similar except the enables are active LOW whereas the F100131 clocks are edge triggered.

Fig. 3-6 F100131 D Flip-flop

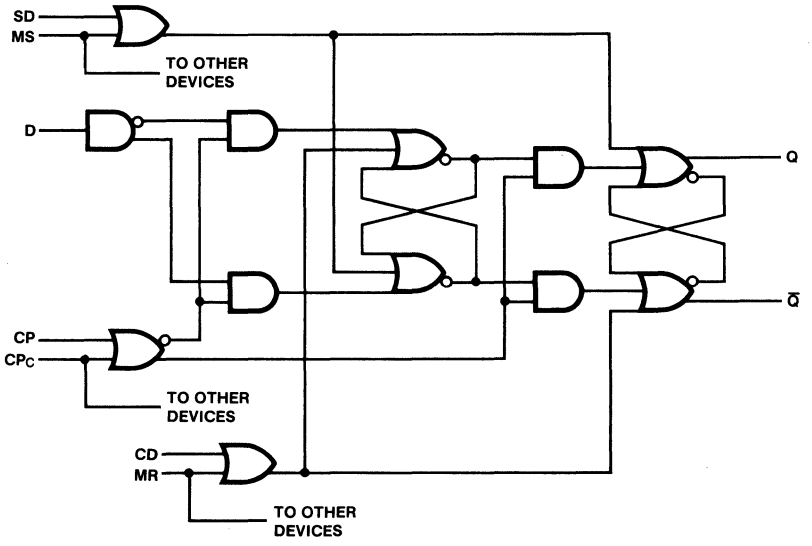


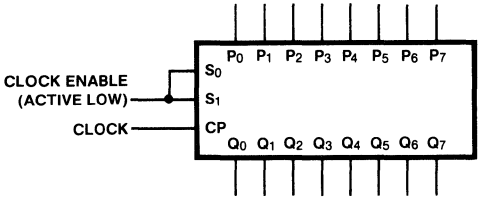
Table 3-3 F100131 Truth Table

D_n	CP_n	CP_c	MS SD_n	MR CD_n	$Q_{n(t+1)}$
L	↑	L	L	L	L
H	↑	L	L	L	H
L	L	↑	L	L	L
H	L	↑	L	L	H
X	H	X	L	L	$Q_n(t)$
X	X	H	L	L	$Q_n(t)$
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
U = Undefined
t, t + 1 = Time before and after CP positive transition

If eight flip-flops are desired, such as for pipeline register applications, the F100141 Shift Register can be used. Neither reset nor complementary outputs are available. The Select inputs may be used to mechanize a clock enable as shown in *Figure 3-7*.

Fig. 3-7 F100141 as Octal D Flip-flop



Counters

The F100136 operates either as a modulo-16 up/down counter or as a 4-bit bidirectional shift register. It has three Select inputs which determine the mode of operation as shown in *Table 3-4*. In addition, a Terminal Count output, and two Count Enables are provided for easy expansion to longer counters. A detailed truth table for the F100136 is included in the specification sheet. To achieve the highest possible speed, complementary outputs should be equally terminated, i.e., if Q_2 is used, $\overline{Q_2}$ should be equally terminated even if not used. If neither output of a particular stage is used, then both outputs can be left open.

Table 3-4 F100136 Function Select Table

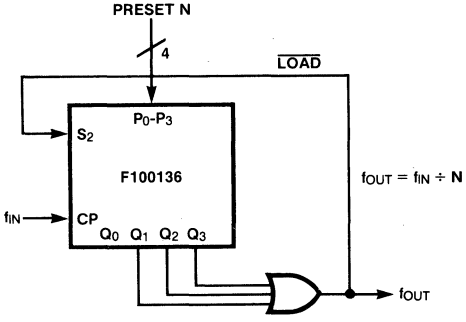
S_0	S_1	S_2	Function
L	L	L	Load
L	L	H	Count Down
L	H	L	Shift Left
L	H	H	Count Up
H	L	L	Complement
H	L	H	Clear
H	H	L	Shift Right
H	H	H	Hold

H = HIGH Voltage Level
L = LOW Voltage Level

Variable Modulus Counters

An F100136 can act as a programmable divider by presetting it via the parallel inputs, counting down to minimum and then presetting it again to start the next cycle. *Figure 3-8* shows a one-stage counter capable of dividing by 2 to 15. S_0 and S_1 are unconnected (therefore LOW) and the counter thus is in either the Count Down or Parallel Load mode, depending on whether S_2 is HIGH or LOW, respectively. $\overline{CEP}$ and $\overline{CET}$ are also LOW, enabling counting when S_2 is HIGH. Immediately after the counter is preset to N, which must be greater than one, the $\overline{LOAD}$ signal goes HIGH and the F100136 starts counting down on the next clock. When it counts down to one, the $\overline{LOAD}$ signal goes LOW and presetting will occur on the next clock rising edge. Generating the $\overline{LOAD}$ signal on the count of one, rather than zero, makes up for the clock pulse used in presetting.

Fig. 3-8 1-Stage Counter



A 3-stage programmable divider is shown in *Figure 3-9*. The $\overline{TC}$ output of the first stage enables counting in the upper stages, while the $\overline{TC}$ output of the second stage also enables counting in the third stage. The D-input signal to the flip-flop is normally HIGH and thus $\overline{Q}$ is normally LOW. When both the second and third stage counters have counted down to zero, the $\overline{TC}$ output of the third stage goes LOW. When the first stage subsequently counts down to one, the D signal goes LOW, as does $\overline{LOAD}$. Presetting thus occurs on the next clock and $\overline{Q}$ goes HIGH to end the $\overline{LOAD}$ signal and permit counting to resume on the next clock.

In *Figure 3-8*, the maximum clock frequency is determined by the sum of the propagation delays from CP to Q and the OR gate, plus the set-up time from S to CP. The maximum frequency is approximately 220 MHz for typical units or 170 MHz for worst-case units. In *Figure 3-9* the critical path is CP to Q of the first stage plus both OR gates, plus the S to CP set-up time of the counters. Typical and worst-case maximum frequencies are 190 MHz and 140 MHz respectively.

Interconnecting Counters

The terminal count and count enable connections provide an easy method of interconnecting the F100136 counter to achieve longer counts. *Figure 3-10* shows a method that uses few connections but has a drawback. The counters are fully synchronous, since the clock arrives at all devices at the same time; the only drawback is that the count enables have to "trickle" down the chain. This results in a lower maximum counting rate since it drastically increases the set-up time from enable to clock.

Figure 3-11 shows a method for partially overcoming these drawbacks. The enable to clock set-up is now one $\overline{CET}$ to $\overline{TC}$ propagation delay plus one $\overline{CEP}$ to CP set-up. The count speed is thus increased. This is best seen by assuming that all stages except the second are at terminal count. At the next clock pulse, the second counter reaches terminal count and the first stage exits terminal count. The command to suppress counting in the third and fourth (and subsequent) stages arrives very quickly (via $\overline{CEP}$). The terminal count from the second

Fig. 3-9 3-Stage Programmable Divider

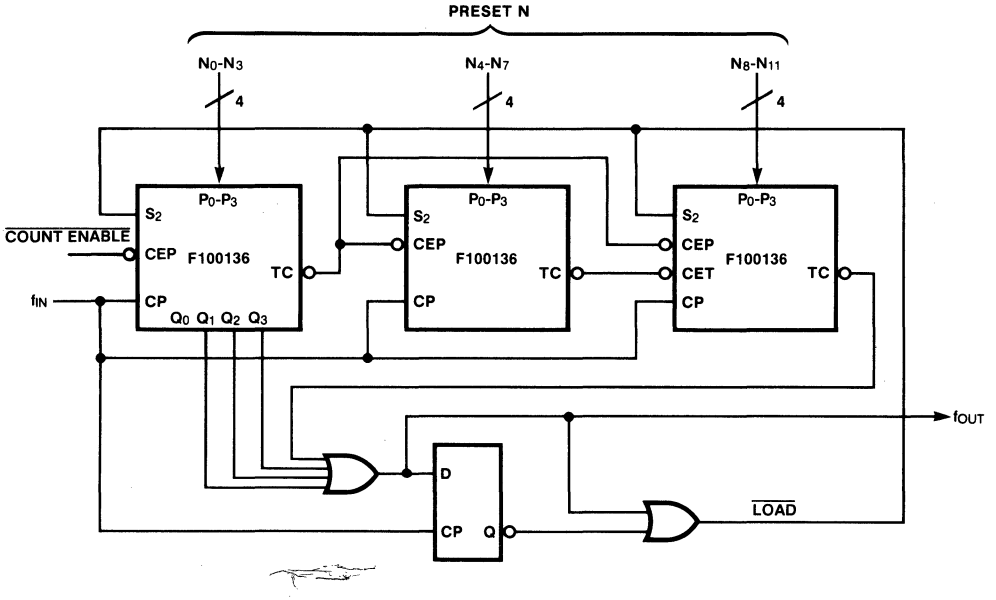


Fig. 3-10 Slow Expansion Scheme

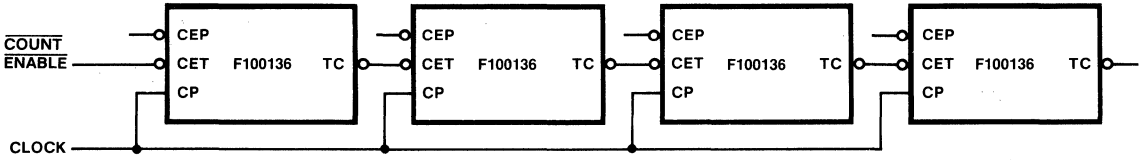
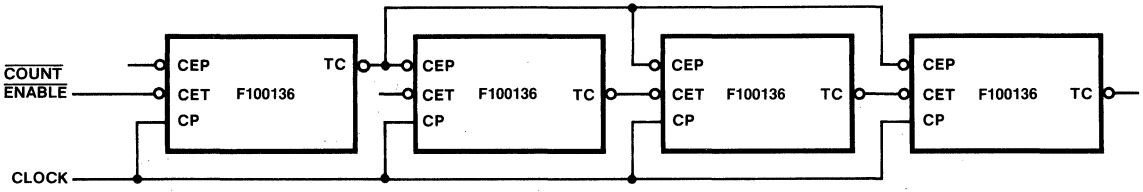


Fig. 3-11 Fast Expansion Scheme

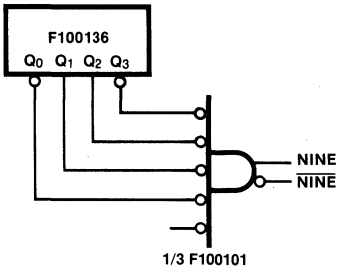


stage propagates via $\overline{TC}$ and $\overline{CEP}$ to the high order stages, but has a full 15 counts to do so.

Decoding Outputs

Since the complementary outputs from each stage are available, it is an easy matter to decode any value. (Clearly, if many values needed to be decoded one would choose a decoder chip.) *Figure 3-12* shows an F100136 and 1/3 F100101 interconnected to decode 1001 (NINE). Both complementary outputs of NINE are available and there is a spare input on the decoding gate.

Fig. 3-12 Decoding States of F100136



Shift Registers

The F100141 is an 8-bit universal shift register. It can be used for parallel-to-serial or serial-to-parallel conversion and it will shift left or right. The truth table is shown in *Table 3-5.*

Table 3-5 F100141 Truth Table

S_1	S_0	CP	Mode
L	L	⎍	Parallel Load
L	H	⎍	Shift Left ($Q_0 \rightarrow Q_7$)
H	L	⎍	Shift Right ($Q_7 \rightarrow Q_0$)
H	H	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Figure 3-13 shows the F100141 used as a 7-bit serial-to-parallel converter. When Initialize (INIT) becomes active, the next clock pulse presets the register to '10000000', and Register-Full (REG-FULL) becomes inactive. Each time a data bit becomes available, Data-Available (DATA-AVAIL) must be made active during one clock LOW-to-HIGH transition. This clocks the bit into the register and moves the flag bit closer to Q_0. When the seventh data bit is entered, the flag bit reaches Q_0 and REG-FULL becomes active. The seven data bits may be removed at this time (Q_1 to Q_7) and the conversion is complete.

Fig. 3-13 Serial-to-Parallel Conversion

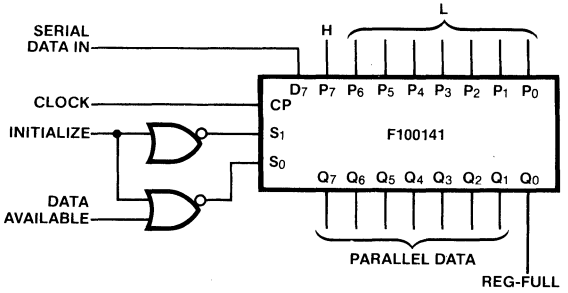


Table 3-6 summarizes the control inputs and corresponding F100141 modes for this circuit.

Table 3-6 Select Inputs Truth Table

INIT	DATA-AVAIL	S_1	S_0	Mode
L	L	H	H	Hold
L	H	H	L	Shift right
H	L	L	L	Preset
H	H	L	L	(illegal)

H = HIGH Voltage Level
L = LOW Voltage Level

Figure 3-15 shows a parallel-to-serial converter using the F100136 counter. *Figure 3-14* shows the associated timing diagram. Each time the external device has taken a bit of data, it makes the signal Serial-Data-Accept (SERIAL-DATA-ACPT) HIGH. The shift register shifts right which makes the next bit available and the counter counts up. The Serial-Data-Accept term must be synchronized with the clock. The counter counts to eight after the eighth data bit has been accepted and Parallel-Data-Request (PARALLEL-DATA-RQST) becomes active HIGH. When the device supplying data makes the next byte available, Parallel-Data-Ready (PARALLEL-DATA-RDY) goes HIGH. On the next clock pulse the shift register loads the new data byte and the counter clears to zero. *Table 3-7* shows the operating mode as a function of the control inputs.

Fig. 3-15 Parallel-to-Serial Converter

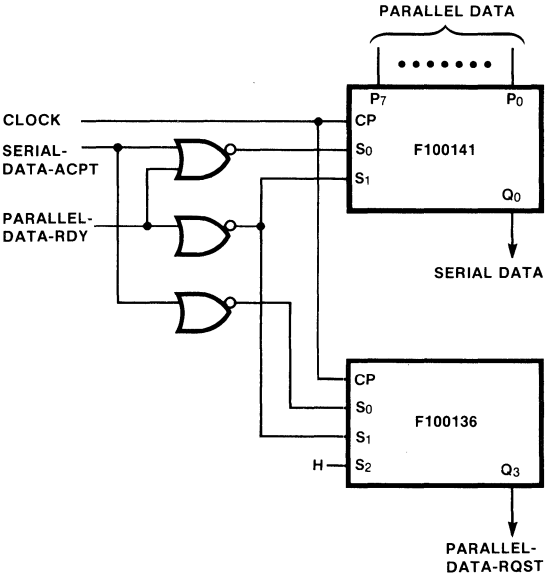


Fig. 3-14 Timing Diagram Parallel-to-Serial Converter

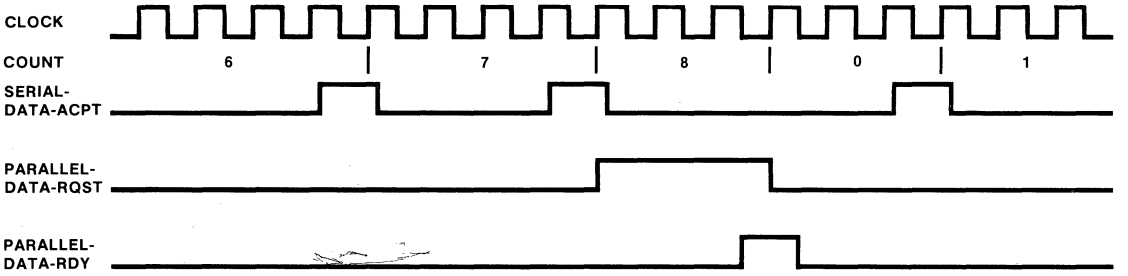


Table 3-7 Parallel-to-Serial Converter Truth Table

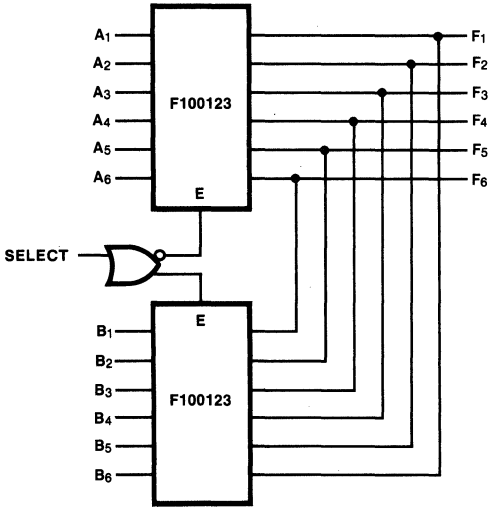
PARALLEL-DATA-RDY	SERIAL-DATA-ACPT	Shift Register			Counter			
		S_1	S_0	Mode	S_0	S_1	S_2	Mode
L	L	H	H	Hold	H	H	H	Hold
L	H	H	L	Shift Right	L	H	H	Count up
H	L	L	L	Load	H	L	H	Clear

H = HIGH Voltage Level
L = LOW Voltage Level

Multiplexers

Multiplexers send one of several inputs to a single output. The function can be implemented with standard gates or bus drivers and the wired-OR connection. *Figure 3-16* shows the F100123 Hex Bus Driver used as a wired-OR multiplexer. The F100123 devices could be in physically different parts of the system, since they can drive double-terminated busses.

Fig. 3-16 Wired-OR Multiplexer



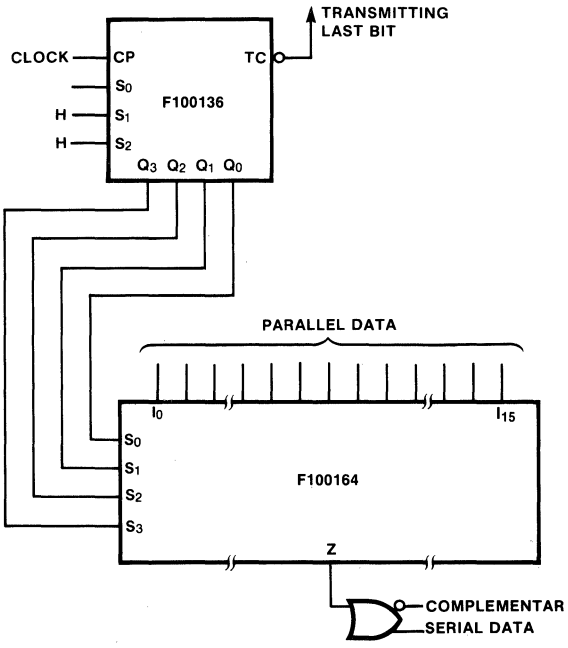
The F100155 is a quad 2-input multiplexer with transparent latches. The device has two select terms and can accept data from either, neither, or both (OR) sources.

The F100163 is a dual 8-input multiplexer with common selects. The F100164 is a single 16-input multiplexer.

The F100163 and F100164 do not feature complementary outputs or an enable for wired-ORing. The F100171 is a triple 4-input multiplexer with enable and complementary outputs.

Figure 3-17 shows an F100164 multiplexer and F100136 connected to convert 16-bit parallel data to single-bit serial data. A gate is added to provide complementary serial data. If the input data is stable, then the output

Fig. 3-17 Parallel-to-Serial Data Transmission



data is stable from 6.4 ns after a clock until 2.5 ns after the next clock. This would insure valid data 50% of the time at a clock rate of 100 MHz. Terminal Count on the counter can be used as a term to indicate the last bit is being transmitted. This can be used as a clock enable to the register containing the parallel data. The propagation delay through the register is masked by the propagation delay through the counter.

Decoder

The F100170 is a universal demultiplexer/decoder. It can function as either a dual 1-of-4 decoder or as a single 1-of-8 decoder. The outputs can be either active HIGH or active LOW.

If the M input is LOW, then the F100170 is configured as a dual 1-of-4 decoder. Both A_{2a} and H_c must be LOW. *Table 3-8* is a truth table for each half of the F100170; the two halves are completely independent. The truth table is shown for active-HIGH outputs; for active-LOW outputs, H_x is made LOW.

Table 3-8 Dual 1-of-4 Mode Truth Table

Inputs				Active-HIGH Outputs (H_a and H_b Inputs HIGH)			
$\overline{E}_{1a}$ $\overline{E}_{1b}$	$\overline{E}_{2a}$ $\overline{E}_{2b}$	A_{1a} A_{1b}	A_{0a} A_{0b}	Z_{0a} Z_{0b}	Z_{1a} Z_{1b}	Z_{2a} Z_{2b}	Z_{3a} Z_{3b}
H	X	X	X	L	L	L	L
X	H	X	X	L	L	L	L
L	L	L	L	H	L	L	L
L	L	L	H	L	H	L	L
L	L	H	L	L	L	H	L
L	L	H	H	L	L	L	H

*M = A_{2a} = H_c = LOW
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

If the M input is HIGH, then the F100170 is configured as a single 1-of-8 decoder. A_{0b}, A_{1b}, H_a, and H_b must all be LOW. *Table 3-9* is a truth table for the F100170 in single 1-of-8 mode. The truth table is shown for active-HIGH outputs; for active-LOW outputs, H_c is made LOW.

Table 3-9 Single 1-of-8 Mode Truth Table

Inputs					Active-HIGH Outputs (H_c Input HIGH)							
$\overline{E}_1$	$\overline{E}_2$	A_{2a}	A_{1a}	A_{0a}	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

M = HIGH;
A_{0b} = A_{1b} = H_a = H_b = LOW
E_1 = E_{1a} and E_{1b} wired; E_2 = E_{2a} and E_{2b} wired
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Figure 3-18 and *Table 3-10* show a universal decimal decoder and the decode table, respectively. The sense of the outputs can be easily modified. The entire decoder may be enabled with a LOW at the Function input.

Table 3-10 Output Selection

A_0-A_3 Weighted Input	Selected Output per Input Code				
	8421	5421	Excess 3	Excess 3 Gray	2421
0	0	0	3	2	0
1	1	1	4	6	1
2	2	2	5	7	2
3	3	3	6	5	3
4	4	4	7	4	4
5	5	8	8	12	11
6	6	9	9	13	12
7	7	10	10	15	13
8	8	11	11	14	14
9	9	12	12	10	15

Fig. 3-18 Universal Decimal Decoder

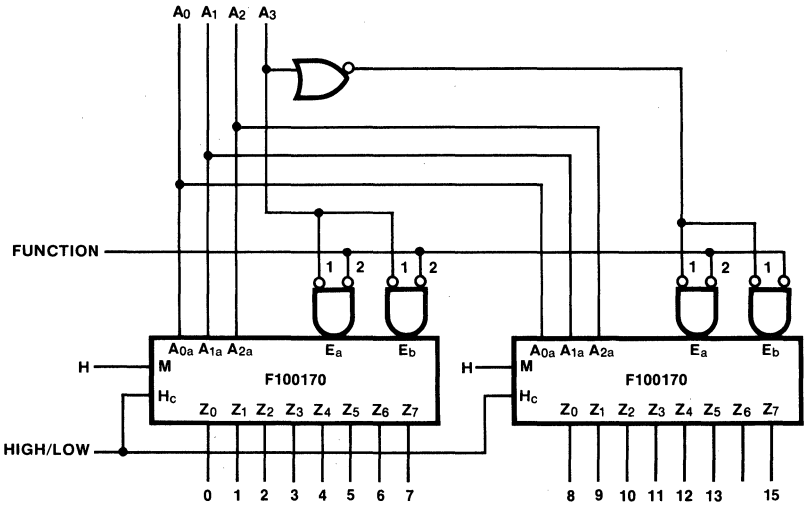


Figure 3-19 shows a scheme to decode five lines with a 1-of-32 decoder. Inputs A_0, A_1, and A_2 are connected to the address select inputs of all four decoders in parallel. Both the true and complement of the two high order addresses are formed and then ANDed together at the decoder enable inputs.

Figure 3-20 shows a 1-of-64 decoder which uses the LOW outputs of one F100170 to enable one-of-eight F100170 devices whose address inputs are connected together. The unused enable inputs may be used to enable all 64 outputs. The 64 outputs may be either active HIGH or LOW. The propagation delay from address to any output is 4.5 ns maximum.

Fig. 3-19 1-of-32 Decoder

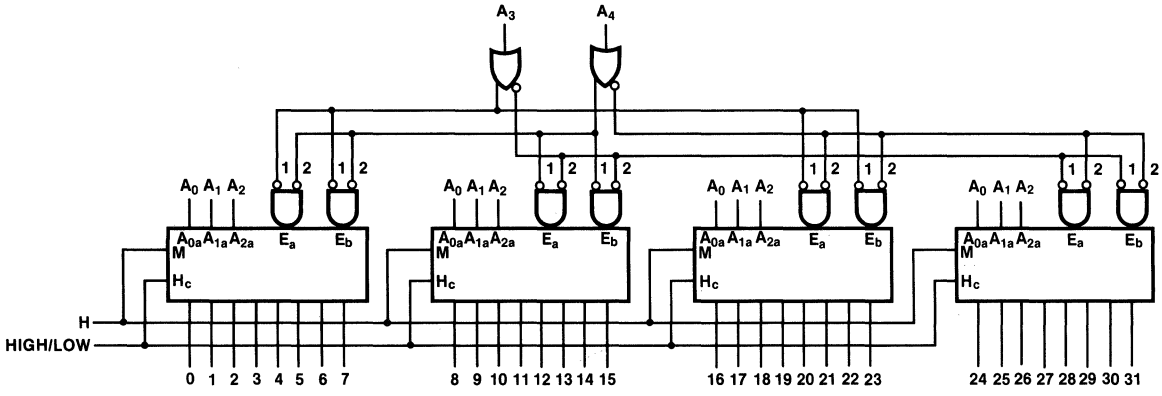
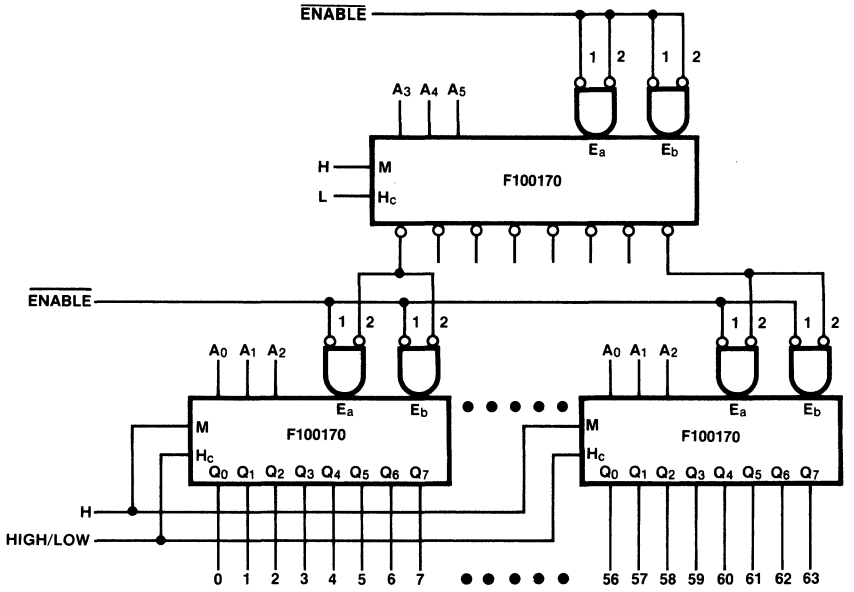


Fig. 3-20 1-of-64 Decoder



Register File

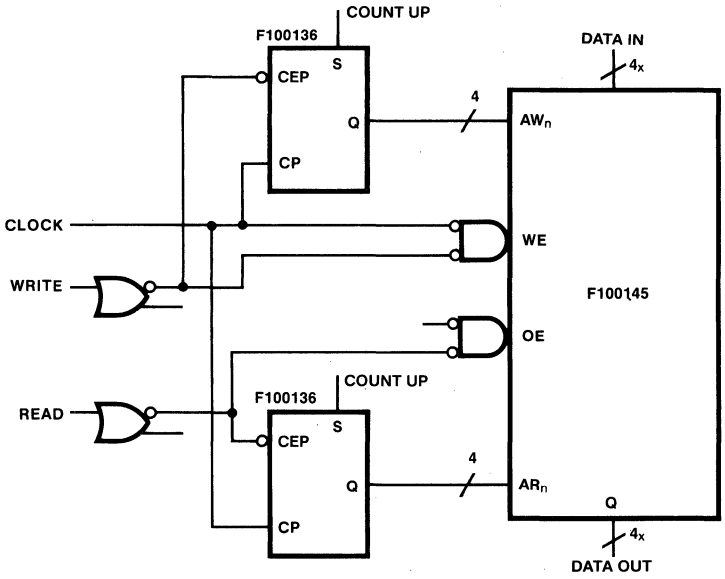
The F100145 is a 16 x 4 register file with typical Read access time of 5.5 ns. It has separate addresses for Read (AR_n) and Write (AW_n) operations. This reduces effective cycle time by allowing one address to be setting up while the other is being used.

Internal output latches are present which store data from a previous Read while a Write is in progress. Any time a Write is not in progress, the data in the latches are updated from the array.

Active-LOW output enables are available, allowing the F100145 to be OR-wired for easy expansion. A HIGH on the Master Reset (MR) input, which overrides all other inputs, resets the output latches, forces the outputs LOW, and clears all cells in the memory.

Figure 3-21 indicates a method of connecting one or more F100145 devices with F100136 devices to form a very fast FIFO. This FIFO can be expanded horizontally (to form wider words) by merely adding more register files. The inputs and outputs must be synchronized to a common clock.

Fig. 3-21 FIFO Diagram

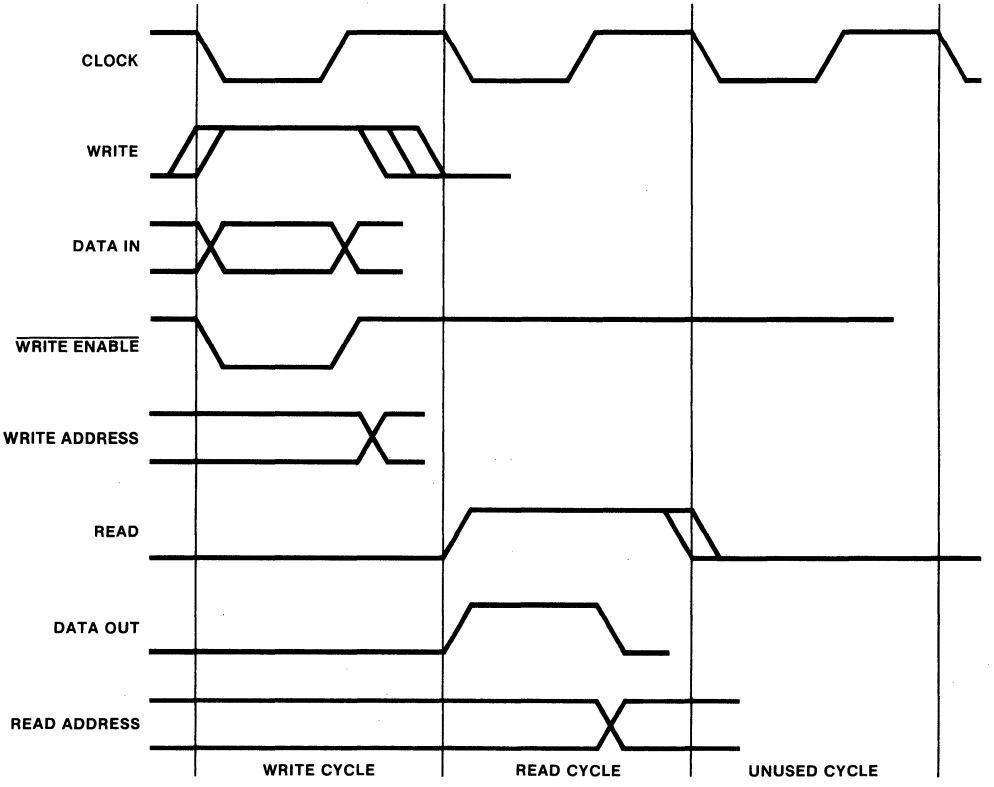


During the first half of the clock cycle, data are written into the FIFO in the case of a WRITE command, or presented on the outputs in the case of a READ command. During the second half of the cycle, either the Write or Read (or neither) address is updated. In addition, the data at the current Read address is accessed in case it will be used during the next cycle. This means that Read data is available very early in the cycle.

The FIFO timing diagram is shown in *Figure 3-22.* The minimum timing of the LOW portion of the clock may be determined as follows. The Write pulse width is 4 ns typical and the data set-up (to trailing edge of Write) is 6 ns typical. Assuming the Write data are available at the beginning of the period, the 6 ns would be the longest path.

The worst case for the HIGH portion of the clock is when a Read is followed by a Read. In this case, the counter must be incremented and the data read from a new location. This is 1.6 + 5.5 ns typical. Allowing for non-typical devices, clock skew, and interconnection delays could bring these numbers to 10 ns each, for a total (Read or Write) cycle time of 20 ns. Since a Read and a Write are required to move one piece of data through the FIFO, the actual transfer rate is 25M words/second.

Fig. 3-22 FIFO Timing



Comparators

The F100166 is a 9-bit magnitude comparator which compares the arithmetic value of two 9-bit words and indicates either A > B, A < B, or $\overline{A = B}$.

The unequal outputs are active HIGH so that expansion is simple. *Figure 3-23* indicates how two 64-bit words may be compared in 5.4 ns typical. If desired, the $\overline{A = B}$ outputs of the first rank may be OR-wired to obtain an active-LOW $\overline{A = B}$ in 2.7 ns typical.

The F100107 Quint Exclusive-OR/NOR may be used as a 5-bit identity comparator with a propagation delay of 2.0 ns typical. The F100160 Parity Checker/Generator may also be used as an identity comparator.

Fig. 3-23 64-Bit Magnitude Comparator

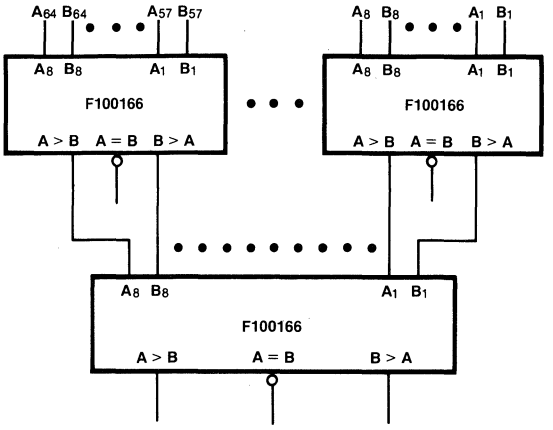
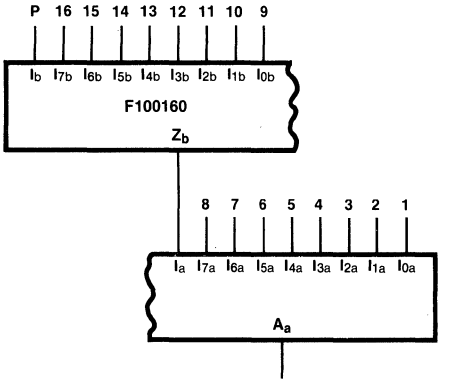


Fig. 3-24 16-Bit Parity Checker/Generator



Parity Generator/Checker

The F100160 is a dual 9-bit parity checker/generator. The output (of each section) is HIGH when an even number of inputs are HIGH. Thus, to generate odd parity on eight bits, the ninth input would be held HIGH. One of the nine inputs on each half has a shorter propagation (I_a, I_b) delay and is thus preferred for expansion.

Figure 3-24 shows how to build a 16-bit parity checker using a single F100160. The typical propagation delay from the longest input is 4.05 ns. This circuit can be turned into a parity generator by replacing "P" at input I_b with a LOW or HIGH for even or odd parity, respectively.

Arithmetic Logic Unit

The F100181 is a 4-bit binary/BCD ALU with a typical propagation delay of 4.5 ns. Output latches are provided to reduce system package count. When the latches are not required, they may be made transparent. *Table 3-11* summarizes the functions available in the F100181. *Table 3-12* is a summary of add times as a function of word width using the F100181 and, optionally, the F100179 Lookahead Carry Generator. These are calculated using maximum times from the data sheets and assume zero interconnection times. Further, it is assumed that the S (function select) inputs are available very early; their delay paths are ignored. The F100181 specification sheet indicates how the parts are interconnected.

Table 3-11 F100181 Functions

S_3	S_2	S_1	S_0	Function	Note
L	L	L	L	A plus B BCD	
L	L	L	H	A minus B BCD	
L	L	H	L	B minus A BCD	
L	L	H	H	O minus A BCD	
L	H	L	L	A plus B binary	
L	H	L	H	A minus B binary	
L	H	H	L	B minus A binary	
L	H	H	H	O minus B binary	
H	L	L	L	Identity	$F = A \bullet B + \overline{A} \bullet \overline{B}$
H	L	L	H	XOR	$F = A \bullet \overline{B} + \overline{A} \bullet B$
H	L	H	L	OR	$F = A + B$
H	L	H	H	A	$F = A$
H	H	L	L	Inverse	$F = \overline{B}$
H	H	L	H	B	$F = B$
H	H	H	L	AND	$F = A \bullet B$
H	H	H	H	Zero	F = LOW

H = HIGH Voltage Level
L = LOW Voltage Level

Table 3-12 Summary of Add times Using F100181

Bits	Ripple Carry	1 F100179 Lookahead Carry	2 F100179 Lookahead Carries
8	11.3	n/a	n/a
16	16.9	11.9	n/a
32	28.1	14.7	14.6
64	50.5	n/a	25.2

Multipliers

The F100182 Wallace Tree Adder and F100183 Recode Multiplier can be combined to build extremely fast parallel multipliers. The F100183 data sheet has detailed applications information; *Table 3-13* is a summary of delay times and package counts for various operand sizes. The times are typical and do not include interconnection delays.

Table 3-13 Multiplier Summary

Operand Size	Delay (ns)	Device Count
16 x 16	16	62
24 x 24	22	115
32 x 32	24	186
64 x 64	26	634

TTL/F100K Interfacing

The F100124 is a hex translator, designed to convert TTL logic levels to F100K ECL logic levels. A common Enable input (E_C), when LOW, holds all true outputs LOW. Complementary outputs are available on each translator, allowing the circuits to be used as inverting, non-inverting, or differential translators. The TTL inputs present the loading factors indicated in *Table 3-14*.

Table 3-14 F100124 Input Loading

Load	Current	Standard TTL Unit Loads
HIGH	50 μA	1.25
HIGH (Enable)	300 μA	7.5
LOW	-3.2 mA	2
LOW (Enable)	-16.0 mA	10

The F100125 is a hex F100K ECL-to-TTL translator. Differential inputs allow each circuit to be used as an inverting, non-inverting, or differential translator. An internal reference voltage generator provides V_{BB} for single-ended operation. The outputs of the F100125 have a fan-out of 50 standard TTL Unit Loads (U.L.) in the HIGH state and 12.5 in the LOW state.

F10K/F100K Interfacing

The problem caused by mixing F10K ECL and F100K ECL is illustrated in *Figures 3-25* and *3-26*. F10K output levels and input thresholds vary with temperature whereas F100K levels and thresholds remain essentially constant. This means that the noise margins vary with temperature, even if the temperatures of the driving and receiving circuits track. Perhaps the worst case is shown in *Figure 3-26*, which illustrates F100K driving F10K.

Fig. 3-25 10K ECL Driving 100K ECL

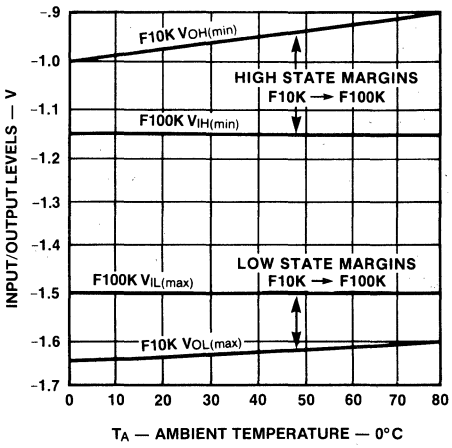
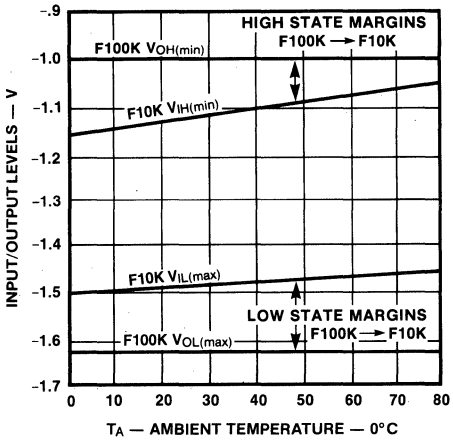


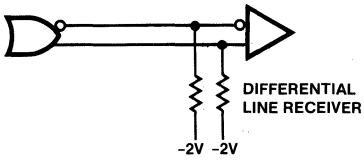
Fig. 3-26 100K ECL Driving 10K ECL

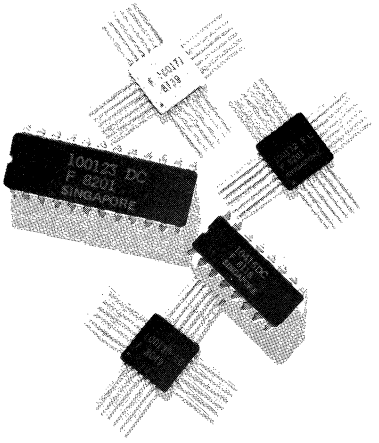


At +75°C, the high margins are seen to be less than 100 mV. Clearly this would not represent acceptable dc margins in any real system.

If the use of F10K ECL in an F100K system is unavoidable, it is recommended that all interfacing be done differentially. This is illustrated in *Figure 3-27* which is applicable for either direction.

Fig. 3-27 Interfacing 10K and 100K





Chapter 4
Transmission Line Concepts

Transmission Line Concepts

Introduction

The interactions between wiring and circuitry in high-speed systems are more easily determined by treating the interconnections as transmission lines. A brief review of basic concepts is presented and simplified methods of analysis are used to examine situations commonly encountered in digital systems. Since the principles and methods apply to any type of logic circuit, normalized pulse amplitudes are used in sample waveforms and calculations.

Simplifying Assumptions

For the great majority of interconnections in digital systems, the resistance of the conductors is much less than the input and output resistance of the circuits. Similarly, the insulating materials have very good dielectric properties. These circumstances allow such factors as attenuation, phase distortion, and bandwidth limitations to be ignored. With these simplifications, interconnections can be dealt with in terms of characteristic impedance and propagation delay.

Characteristic Impedance

The two conductors that interconnect a pair of circuits have distributed series inductance and distributed capacitance between them, and thus constitute a transmission line. For any length in which these distributed parameters are constant, the pair of conductors have a characteristic impedance Z_0. Whereas quiescent conditions on the line are determined by the circuits and terminations, Z_0 is the ratio of transient voltage to transient current passing by a point on the line when a signal charge or other electrical disturbance occurs. The relationship between transient voltage, transient current, characteristic impedance, and the distributed parameters is expressed as follows:

$$\frac{V}{I} = Z_0 = \sqrt{\frac{L_0}{C_0}} \qquad \textbf{(4-1)}$$

where L_0 = inductance per unit length, C_0 = capacitance per unit length. Z_0 is in ohms, L_0 in Henries, C_0 in Farads.

Propagation Velocity

Propagation velocity v and its reciprocal, delay per unit length δ, can also be expressed in terms of L_0 and C_0. A consistent set of units is nanoseconds, microhenries and picofarads, with a common unit of length.

$$v = \frac{1}{\sqrt{L_0 C_0}} \qquad \delta = \sqrt{L_0 C_0} \qquad \textbf{(4-2)}$$

Equations 4-1 and *4-2* provide a convenient means of determining the L_0 and C_0 of a line when delay, length and impedance are known. For a length l and delay T, δ is the ratio T/l. To determine L_0 and C_0, combine *Equations 4-1* and *4-2*.

$$L_0 = \delta Z_0 \qquad \textbf{(4-3)}$$

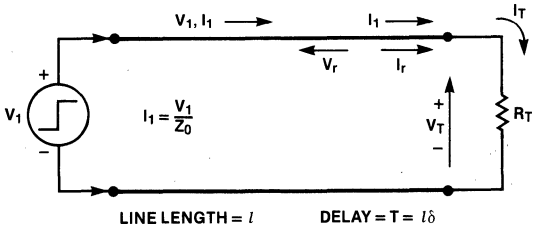
$$C_0 = \frac{\delta}{Z_0} \qquad \textbf{(4-4)}$$

More formal treatments of transmission line characteristics, including loss effects, are available from many sources.[1–3]

Termination and Reflection

A transmission line with a terminating resistor is shown in *Figure 4-1*. As indicated, a positive step function voltage travels from left to right. To keep track of reflection polarities, it is convenient to consider the lower conductor as the voltage reference and to think in terms of current flow in the top conductor only. The generator is assumed to have zero internal impedance. The initial current I_1 is determined by V_1 and Z_0.

Fig. 4-1 Assigned Polarities and Directions for Determining Reflections



If the terminating resistor matches the line impedance, the ratio of voltage to current traveling along the line is matched by the ratio of voltage to current which must, by Ohm's law, always prevail at R_T. From the viewpoint of the voltage step generator, no adjustment of output current is ever required; the situation is as though the transmission line never existed and R_T had been connected directly across the terminals of the generator.

From the R_T viewpoint, the only thing the line did was delay the arrival of the voltage step by the amount of time T.

When R_T is not equal to Z_0, the initial current starting down the line is still determined by V_1 and Z_0 but the final steady state current, after all reflections have died out, is determined by V_1 and R_T (ohmic resistance of the line is assumed to be negligible). The ratio of voltage to current in the initial wave is not equal to the ratio of voltage to current demanded by R_T. Therefore, at the instant the initial wave arrives at R_T, another voltage and current wave must be generated so that Ohm's law is satisfied at the line-load interface. This *reflected* wave, indicated, by V_r and I_r in *Figure 4-1,* starts to return toward the generator. Applying Kirchoff's laws to the end of the line at the instant the initial wave arrives, results in the following.

$$I_1 + I_r = I_T = \text{current into } R_T \qquad \textbf{(4-5)}$$

Since only one voltage can exist at the end of the line at this instant of time, the following is true:

$$V_1 + V_r = V_T$$

$$\text{thus} \qquad I_T = \frac{V_T}{R_T} = \frac{V_1 + V_r}{R_T} \qquad \textbf{(4-6)}$$

$$\text{also} \qquad I_1 = \frac{V_1}{Z_0} \text{ and } I_r = -\frac{V_r}{Z_0}$$

with the minus sign indicating that V_r is moving toward the generator.

Combining the foregoing relationships algebraically and solving for V_r yields a simplified expression in terms of V_1, Z_0 and R_T.

$$\frac{V_1}{Z_0} - \frac{V_r}{Z_0} = \frac{V_1 + V_r}{R_T} = \frac{V_1}{R_T} + \frac{V_r}{R_T}$$

$$V_1 \left(\frac{1}{Z_0} - \frac{1}{R_T}\right) = V_r \left(\frac{1}{R_T} + \frac{1}{Z_0}\right) \qquad \textbf{(4-7)}$$

$$V_r = V_1 \left(\frac{R_T - Z_0}{R_T + Z_0}\right) = \rho_L V_1$$

The term in parentheses is called the coefficient of reflection ρ. With R_T ranging between zero (shorted line) and infinity (open line), the coefficient ranges between -1 and +1 respectively. The subscript L indicates that ρ refers to the coefficient at the load end of the line.

Equation 4-7 expresses the amount of voltage sent back down the line, and since

$$V_T = V_1 + V_r$$

$$\text{then} \qquad V_T = V_1 (1 + \rho_L). \qquad \textbf{(4-8)}$$

V_T can also be determined from an expression which does not require the preliminary step of calculating ρ_L. Manipulating $(1 + \rho_L)$ results in

$$1 + \rho_L = 1 + \frac{R_T - Z_0}{R_T + Z_0} = 2\left(\frac{R_T}{R_T + Z_0}\right)$$

Substituting in *Equation 4-8* gives

$$V_T = 2\left(\frac{R_T}{R_T + Z_0}\right) V_1 \qquad \textbf{(4-9)}$$

The foregoing has the same form as a simple voltage divider involving a generator V_1 with internal impedance Z_0 driving a load R_T, except that the amplitude of V_T is doubled.

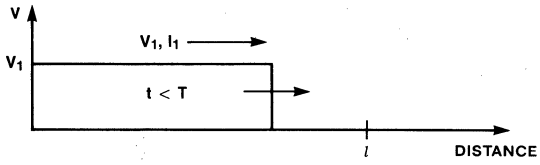
The arrow indicating the direction of V_r in *Figure 4-1*, correctly indicates the V_r direction of travel, but the direction of I_r flow depends on the V_r polarity. If V_r is positive, I_r flows toward the generator, opposing I_1. This relationship between the polarity of V_r and the direction of I_r can be deduced by noting in *Equation 4-7* that if V_r is positive it is because R_T is greater than Z_0. In turn, this means that the initial current I_r is larger than the final quiescent current, dictated by V_1 and R_T. Hence I_r must oppose I_1 to reduce the line current to the final quiescent value. Similar reasoning shows that if V_r is negative, I_r flows in the same direction as I_1.

It is sometimes easier to determine the effect of V_r on line conditions by thinking of it as an independent voltage generator in series with R_T. With this concept, the direction of I_r is immediately apparent; its magnitude, however, is the ratio of V_r to Z_0, *i.e.*, R_T is

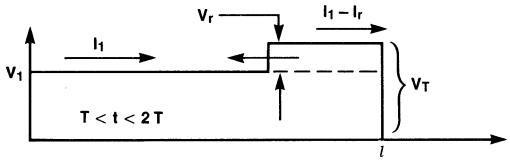
already accounted for in the magnitude of V_r. The relationships between incident and reflected signals are represented in *Figure 4-2* for both cases of mismatch between R_T and Z_0.

Fig. 4-2 Reflections for $R_T \neq Z_0$

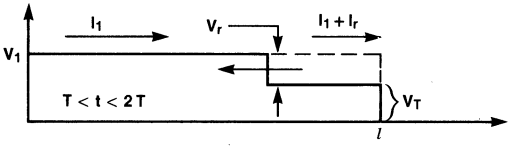
a. Incident Wave



b. Reflected Wave for $R_T > Z_0$



c. Reflected Wave for $R_T < Z_0$



The incident wave is shown in *Figure 4-2a,* before it has reached the end of the line. In *Figure 4-2b,* a positive V_r is returning to the generator. To the left of V_r the current is still I_1, flowing to the right, while to the right of V_r the net current in the line is the difference between I_1 and I_r. In *Figure 4-2c,* the reflection coefficient is negative, producing a negative V_r. This, in turn, causes an increase in the amount of current flowing to the right behind the V_r wave.

Source Impedance, Multiple Reflections

When a reflected voltage arrives back at the source (generator), the reflection coefficient at the source determines the response to V_r. The coefficient of reflection at the source is governed by Z_0 and the source resistance R_S.

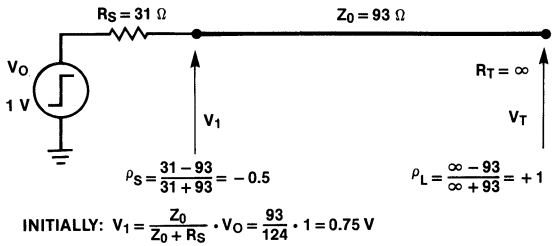
$$\rho_S = \frac{R_S - Z_0}{R_S + Z_0} \qquad \textbf{(4-10)}$$

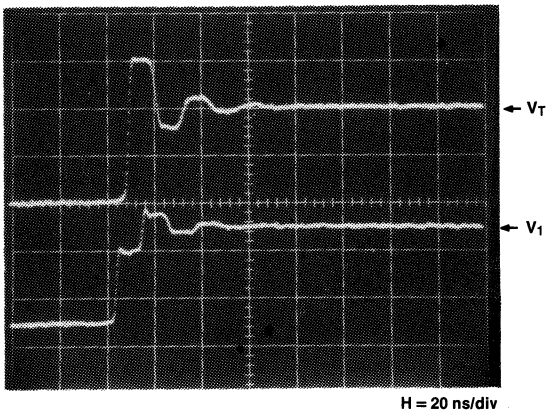
If the source impedance matches the line impedance, a reflected voltage arriving at the source is not reflected back toward the load end. Voltage and current on the line are stable with the following values.

$$V_T = V_1 + V_r \text{ and } I_T = I_1 - I_r \qquad \textbf{(4-11)}$$

If neither source impedance nor terminating impedance matches Z_0, multiple reflections occur; the voltage at each end of the line comes closer to the final steady state value with each succeeding reflection. An example of a line mismatched on both ends is shown in *Figure 4-3.* The source is a step function of 1 V ampli-

Fig. 4-3 Multiple Reflections Due to Mismatch at Load and Source





H = 20 ns/div
V = 0.5 V/div

tude occurring at time t_0. The initial value of V_1 starting down the line is 0.75 V due to the voltage divider action of Z_0 and R_S. The time scale in the photograph shows that the line delay is approximately 6 ns. Since neither end of the line is terminated in its characteristic impedance, multiple reflections occur.

The amplitude and persistence of the ringing shown in *Figure 4-3* become greater with increasing mismatch between the line impedance and source and load impedances. Reducing R_S *(Figure 4-3)* to 13 Ω increases ρ_S to −0.75, and the effects are illustrated in *Figure 4-4.* The initial value of V_T is 1.8 V with a reflection of 0.9 V from the open end. When this reflection reaches the source, a reflection of 0.9 × -0.75 V starts back toward the open end. Thus, the second increment of voltage arriving at the open end is negative going. In turn, a negative-going reflection of 0.9 × -0.75 V starts back toward the source. This negative increment is again multiplied by −0.75 at the source and returned toward the open end. It can be deduced that the difference in amplitude between the first two positive peaks observed at the open end is

$$V_T - V'_T = (1 + \rho_L)\, V_1 - (1 + \rho_L)\, V_1 \rho^2_L \rho^2_S \qquad \textbf{(4-12)}$$
$$= (1 + \rho_L)\, V_1 (1 - \rho^2_L \rho^2_S).$$

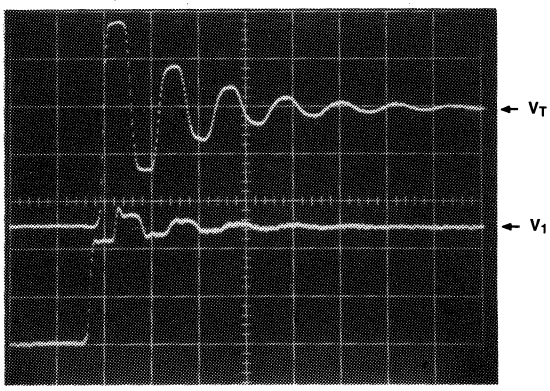
The factor $(1 - \rho^2_L \rho^2_S)$ is similar to the damping factor associated with lumped constant circuitry. It expresses the attenuation of successive positive or negative peaks of ringing.

Lattice Diagram

In the presence of multiple reflections, keeping track of the incremental waves on the line and the net voltage at the ends becomes a bookkeeping chore. A convenient and systematic method of indicating the conditions which combines magnitude, polarity and time utilizes a graphic construction called a lattice diagram.[4] A lattice diagram for the line conditions of *Figure 4-3* is shown in *Figure 4-5.*

The vertical lines symbolize discontinuity points, in this case the ends of the line. A time scale is marked off on each line in increments of 2T, starting at t_0 for V_1 and T for V_T. The diagonal lines indicate the incremental voltages traveling between the ends of the line; solid

Fig. 4-4 Extended Ringing when R_S of Figure 4-3 is Reduced to 13 Ω



H = 20 ns/div
V = 0.4 V/div

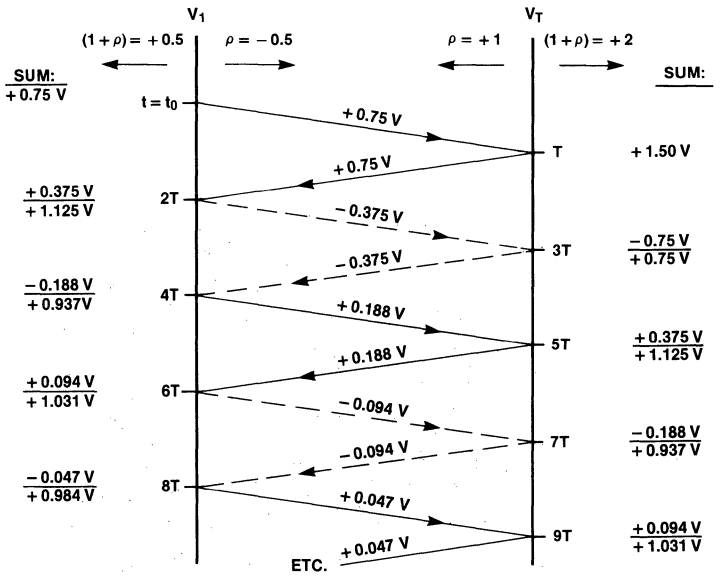
lines are used for positive voltages and dashed lines for negative. It is helpful to write the reflection and transmission multipliers ρ and $(1 + \rho)$ at each vertical line, and to tabulate the incremental and net voltages in columns alongside the vertical lines. Both the lattice diagram and the waveform photograph show that V_1 and V_T asymptotically approach 1 V, as they must with a 1 V source driving an open-ended line.

Shorted Line

The open-ended line in *Figure 4-3* has a reflection coefficient of +1 and the successive reflections tend toward the steady state conditions of zero line current and a line voltage equal to the source voltage. In contrast, a shorted line has a reflection coefficient of -1 and successive reflections must cause the line conditions to approach the steady state conditions of zero voltage and a line current determined by the source voltage and resistance.

Shorted line conditions are shown in *Figure 4-6a* with the reflection coefficient at the source end of the line also negative. A negative coefficient at both ends of the line means that any voltage approaching either end of the line is reflected in the opposite polarity. *Figure 4-6b* shows the response to an input step-function with a duration much longer than the line delay. The initial voltage starting down the line is about +0.75 V, which is

Fig. 4-5 Lattice Diagram for the Circuit of Figure 4-3



inverted at the shorted end and returned toward the source as -0.75 V. Arriving back at the source end of the line, this voltage is multiplied by $(1 + \rho_S)$, causing a -0.37 V net change in V_1. Concurrently, a reflected voltage of +0.37 V (-0.75 V times ρ_S of -0.5) starts back toward the shorted end of the line. The voltage at V_1 is reduced by 50% with each successive round trip of reflections, thus leading to the final condition of zero volts on the line.

When the duration of the input pulse is less than the delay of the line, the reflections observed at the source end of the line constitute a train of negative pulses, as shown in *Figure 4-6c.* The amplitude decreases by 50% with each successive occurrence as it did in *Figure 4-6b.*

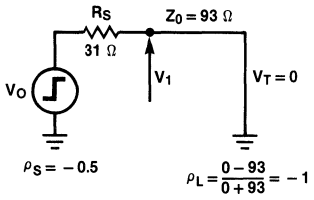
Series Termination

Driving an open-ended line through a source resistance equal to the line impedance is called series termination. It is particularly useful when transmitting signals which originate on a PC board and travel through the backplane to another board, with the attendant discontinuities, since reflections coming back to the source are absorbed and ringing thereby controlled. *Figure 4-7* shows a 93 Ω line driven from a 1 V generator through a source impedance of 93 Ω. The photograph illustrates that the amplitude of the initial signal sent down the line is only half of the generator voltage, while the voltage at the open end of the line is doubled to full amplitude $(1 + \rho_L = 2)$. The reflected voltage arriving back at the source raises V_1 to the full amplitude of the generator signal. Since the reflection coefficient at the source is zero, no further changes occur and the line voltage is equal to the generator voltage. Because the initial signal on the line is only half the normal signal swing, the loads must be connected at or near the end of the line to avoid receiving a 2-step input signal.

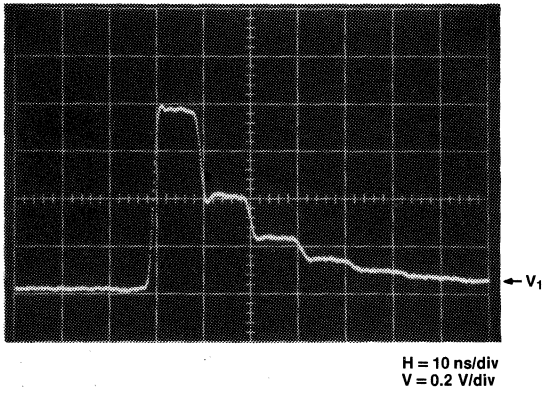
An ECL output driving a series terminated line requires a pull-down resistor to V_{EE}, as indicated in *Figure 4-8.* The resistor R_0 shown in *Figure 4-8* symbolizes the output resistance of the ECL gate. The relationships between R_0, R_S, R_E and Z_0 are discussed in *Chapter 5.*

Fig. 4-6 Reflections of Long and Short Pulses on a Shorted Line

a. Reflection Coefficients for Shorted Line



b. Input Pulse Duration >> Line Delay



c. Input Pulse Duration < Line Delay

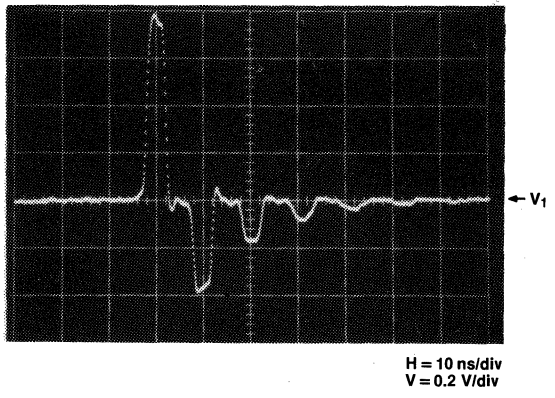


Fig. 4-7 Series Terminated Line and Waveforms

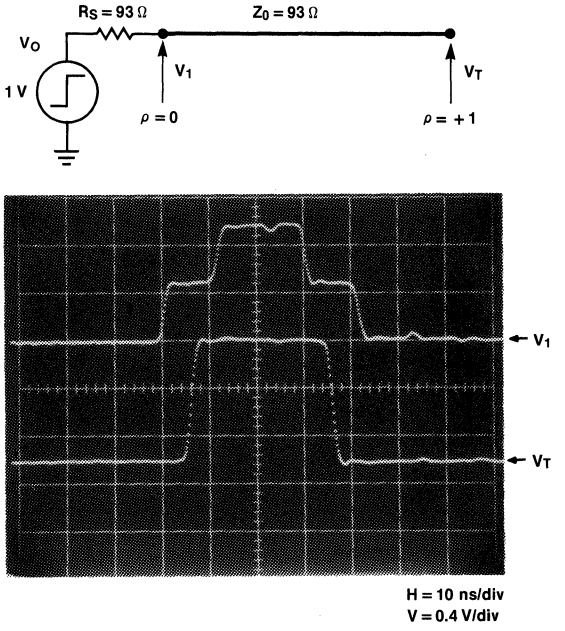
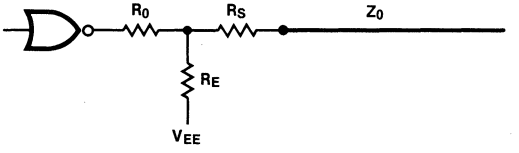


Fig. 4-8 ECL Element Driving a Series Terminated Line

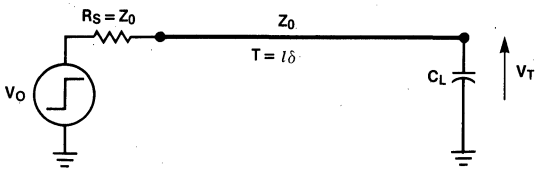


Extra Delay with Termination Capacitance

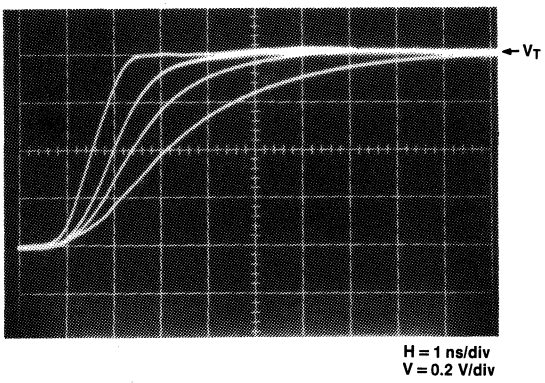
Designers should consider the effect of the load capacitance at the end of the line when using series termination. *Figure 4-9* shows how the output waveform changes with increasing load capacitance. *Figure 4-9b* shows the effect of load capacitances of 0, 12, 24, 48 pF. With no load, the delay between the 50% points of the input and output is just the line delay T. A capacitive load at the end of the line causes an extra delay ΔT due to the increase in rise time of the output signal. The midpoint of the output is used as a criterion because the propagation delay of an ECL circuit is measured between the 50% points of the input and output signals.

Fig. 4-9 Extra Delay with Termination Capacitance

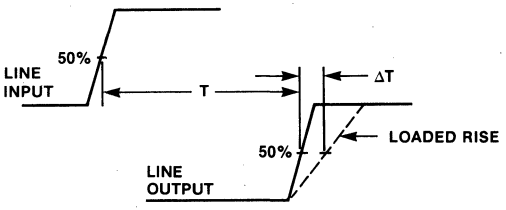
a. Series Terminated Line with Load Capacitance



b. Output Rise Time Increase with Increasing Load Capacitance



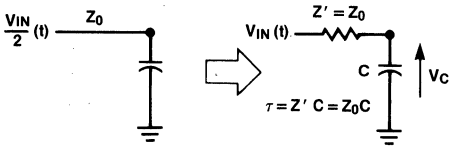
c. Extra Delay ΔT Due to Rise Time Increase



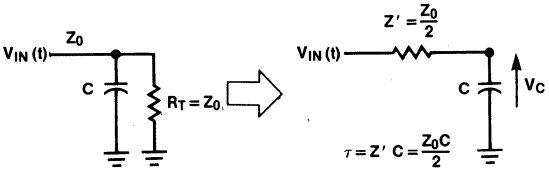
The increase in propagation delay can be calculated by using a ramp approximation for the incident voltage and characterizing the circuit as a fixed impedance in series with the load capacitance, as shown in *Figure 4-10*. One general solution serves both series and parallel termination cases by using an impedance Z′ and a time constant τ, defined in *Figure 4-10a* and *4-10b*. Calculated and observed increases in delay time to the 50% point show close agreement when τ is less than half the ramp time. At large ratios of τ/a (where a = ramp

Fig. 4-10 Determining the Effect of End-of-Line Capacitance

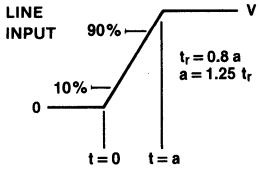
a. Thevenin Equivalent for Series Terminated Case



b. Thevenin Equivalent for Parallel Terminated Case



c. Equations for Input and Output Voltages



$$v_{in}(t) = \frac{V}{a}\,[tu(t) - (t-a)u(t-a)]$$

$$u(t) = \begin{matrix} 0 \text{ for } t < o \\ 1 \text{ for } t > o \end{matrix}$$

$$u(t-a) = \begin{matrix} 0 \text{ for } t < a, \\ 1 \text{ for } t > a \end{matrix}$$

$$V_{IN}(S) = \frac{V}{as^2}\,(1 - e^{-as})$$

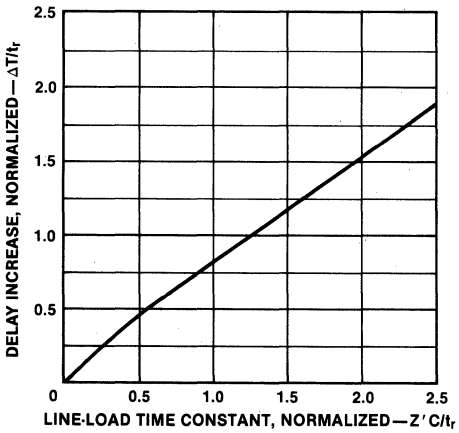
$$V_C(S) = \frac{V}{ar} \bullet \frac{1}{s^2(s + 1/\tau)}\,(1 - e^{-as})$$

$$v_c(t) = \frac{V}{a}\,[t - \tau(1 - e^{-t/\tau})]\,u(t) - \frac{V}{a}\,[(t-a) - \tau(1 - e^{-\frac{t-a}{\tau}})]\,u(t-a)$$

time), measured delays exceed calculated values by approximately 7%. *Figure 4-11,* based on measured values, shows the increase in delay to the 50% point as a function of the Z'C time constant, both normalized to the 10% to 90% rise time of the input signal. As an example of using the graph, consider a 100 Ω series terminated line with 30 pF load capacitance at the end of the line and a no-load rise time of 3 ns for the input signal. From *Figure 4-10a,* Z' is equal to 100 Ω; the ratio $Z'C/t_r$ is 1. From the graph, the ratio $\Delta T/t_r$ is 0.8. Thus the increase in the delay to the 50% point of the output waveform is 0.8 t_r, or 2.4 ns, which is then added to the no-load line delay T to determine the total delay.

Had the 100 Ω line in the foregoing example been parallel rather than series terminated at the end of the line, Z' would be 50 Ω. The added delay would be only 1.35 ns with the same 30 pF loading at the end. The added delay would be only 0.75 ns if the line were 50 Ω and parallel terminated. The various trade-offs involving type of termination, line impedance, and loading are important considerations for critical delay paths.

Fig. 4-11 Increase in 50% Point Delay Due to Capacitive Loading at the End of the Line, Normalized to T_r



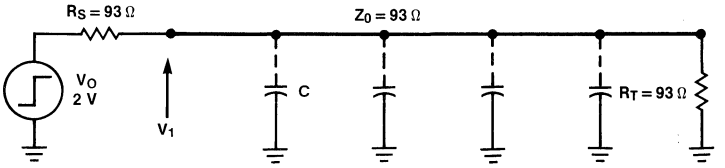
Distributed Loading Effects on Line Characteristics

When capacitive loads such as ECL inputs are connected along a transmission line, each one causes a reflection with a polarity opposite to that of the incident wave. Reflections from two adjacent loads tend to overlap if the time required for the incident wave to travel from one load to the next is equal to or less than the signal rise time.[5] *Figure 4-12a* illustrates an arrangement for observing the effects of capacitive loading, while *Figure 4-12b* shows an incident wave followed by reflections from two capacitive loads. The two capacitors causing the reflections are separated by a distance requiring a travel time of 1 ns. The two reflections return to the source 2 ns apart, since it takes 1 ns longer for the incident wave to reach the second capacitor and an additional 1 ns for the second reflection to travel back to the source. In the upper trace of *Figure 4-12b,* the input signal rise time is 1 ns and there are two distinct reflections, although the trailing edge of the first overlaps the leading edge of the second. The input rise time is longer in the middle trace, causing a greater overlap. In the lower trace, the 2 ns input rise time causes the two reflections to merge and appear as a single reflection which is relatively constant (at ≈ −10%) for half its duration. This is about the same reflection that would occur if the 93 Ω line had a middle section with an impedance reduced to 75 Ω.

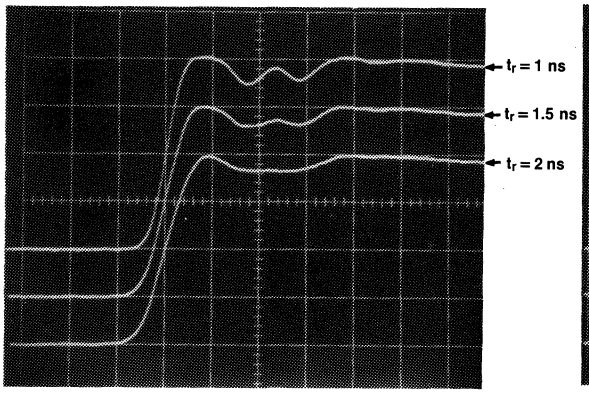
With a number of capacitors distributed all along the line of *Figure 4-12a,* the combined reflections modify the observed input waveform as shown in the top trace of *Figure 4-12c.* The reflections persist for a time equal to the 2-way line delay (15 ns), after which the line voltage attains its final value. The waveform suggests a line terminated with a resistance greater than its characteristic impedance ($R_T > Z_0$). This analogy is strengthened by observing the effect of reducing R_T from 93 Ω to 75 Ω, which leads to the middle waveform of *Figure 4-12c.* Note that the final (steady state) value of the line voltage is reduced by about the same amount as that caused by the capacitive reflections. In the lower trace of *Figure 4-12c* the source resistance R_S is reduced from 93 Ω to 75 Ω, restoring both the initial and final line voltage values to the same amplitude as the final value in the upper trace. From the standpoint of providing a desired signal voltage on the line and impedance matching at either end, the effect of distributed capacitive loading can be treated as a reduction in line impedance.

Fig. 4-12 Capacitive Reflections and Effects on Line Characteristics

a. Arrangement for Observing Capacitive Loading Effects

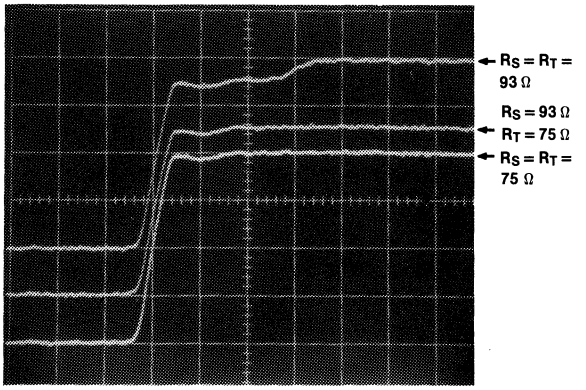


b. Capacitive Reflections Merging as Rise Time Increases



H = 2 ns/div
V = 0.25 V/div

c. Matching the Altered Impedance of a Capacitively Loaded Line



H = 5 ns/div
V = 0.25 V/div

The reduced line impedance can be calculated by considering the load capacitance C_L as an increase in the intrinsic line capacitance C_0 along that portion of the line where the loads are connected.[6] Denoting this length of line as l, the distributed value C_D of the load capacitance is as follows.

$$C_D = \frac{C_L}{l}$$

C_D is then added to C_0 in *Equation 4-1* to determine the reduced line impedance Z_0.

$$Z_0' = \sqrt{\frac{L_0}{C_0 + C_D}} = \sqrt{\frac{L_0}{C_0\left(1 + \frac{C_D}{C_0}\right)}} \qquad \textbf{(4-13)}$$

$$Z_0' + \frac{\sqrt{\frac{L_0}{C_0}}}{\sqrt{1 + \frac{C_D}{C_0}}} = \frac{Z_0}{\sqrt{1 + \frac{C_D}{C_0}}}$$

In the example of *Figure 4-12c*, the total load capacitance is 33 pF while the total intrinsic line capacitance

lC_0 is 60 pF. (Note that the ratio C_D/C_0 is the same as C_L/lC_0.) The calculated value of the reduced impedance is thus

$$Z_0' = \frac{93}{\sqrt{1 + \frac{33}{60}}} = \frac{93}{\sqrt{1.55}} = 75\ \Omega \qquad \textbf{(4-14)}$$

This correlates with the results observed in *Figure 4-12c* when R_T and R_S are reduced to 75 Ω.

The distributed load capacitance also increases the line delay, which can be calculated from *Equation 4-2.*

$$\delta' = \sqrt{L_0(C_0 + C_D)} = \sqrt{L_0 C_0}\sqrt{1 + \frac{C_D}{C_0}} \qquad \textbf{(4-15)}$$

$$= \delta\sqrt{1 + \frac{C_D}{C_0}}$$

The line used in the example of *Figure 4-12c* has an intrinsic delay of 6 ns and a loaded delay of 7.5 ns which checks with *Equation 4-15.*

$$l\delta' = l\delta\sqrt{1.55} = 6\sqrt{1.55} = 7.5\ ns \qquad \textbf{(4-16)}$$

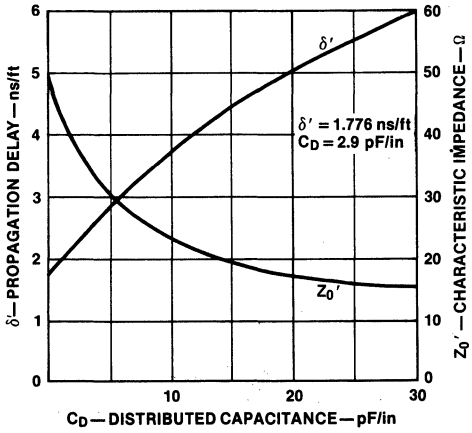
Equation 4-15 can be used to predict the delay for a given line and load. The ratio C_D/C_0 (hence the loading effect) can be minimized for a given loading by using a line with a high intrinsic capacitance C_0.

A plot of Z' and δ' for a 50 ohm line as a function of C_D is shown in *Figure 4-13.* This figure illustrates that relatively modest amounts of load capacitance will add appreciably to the propagation delay of a line. In addition, the characteristic impedance is reduced significantly.

Worst case reflections from a capacitively loaded section of transmission line can be accurately predicted by using the modified impedance of *Equation 4-9.*[6] When a signal originates on an unloaded section of line, the effective reflection coefficient is as follows.

$$\rho = \frac{Z_0' - Z_0}{Z_0' + Z_0} \qquad \textbf{(4-17)}$$

Fig. 4-13 Capacitive Loading Effects on Line Delay and Impedance



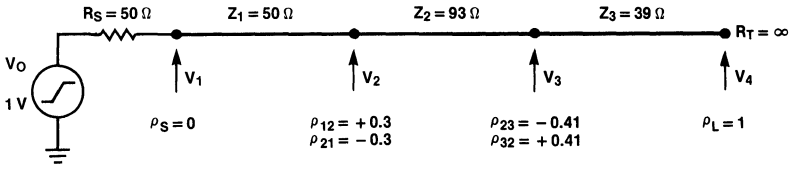
Mismatched Lines

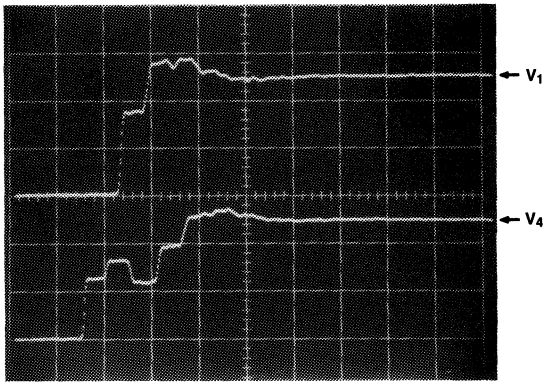
Reflections occur not only from mismatched load and source impedances but also from changes in line impedance. These changes could be caused by bends in coaxial cable, unshielded twisted-pair in contact with metal, or mismatch between PC board traces and backplane wiring. With the coax or twisted-pair, line impedance changes run about 5 to 10% and reflections are usually no problem since the percent reflection is roughly half the percent change in impedance. However, between PC board and backplane wiring, the mismatch can be 2 or 3 to 1. This is illustrated in *Figure 4-14* and analyzed in the lattice diagram of *Figure 4-15.* Line 1 is driven in the series terminated mode so that reflections coming back to the source are absorbed.

The reflection and transmission at the point where impedances differ are determined by treating the downstream line as though it were a terminating resistor. For the example of *Figure 4-14,* the reflection coefficient at the intersection of lines 1 and 2 for a signal traveling to the right is as follows.

$$\rho_{12} = \frac{Z_2 - Z_1}{Z_2 + Z_1} = \frac{93 - 50}{143} = +0.3 \qquad \textbf{(4-18)}$$

Fig. 4-14 Reflections from Mismatched Lines





H = 20 ns/div
V = 0.4 V/div

Thus the signal reflected back toward the source and the signal continuing along line 2 are, respectively, as follows.

$$V_{1r} = \rho_{12} V_1 = +0.3\ V_1 \qquad \textbf{(4-19a)}$$

$$V_2 = (1 + \rho_{12})\ V_1 = +1.3\ V_1 \qquad \textbf{(4-19b)}$$

At the intersection of lines 2 and 3, the reflection coefficient for signals traveling to the right is determined by treating Z_3 as a terminating resistor.

$$\rho_{23} = \frac{Z_3 - Z_2}{Z_3 + Z_2} = \frac{39 - 93}{132} = -0.41 \qquad \textbf{(4-20)}$$

When V_2 arrives at this point, the reflected and transmitted signals are as follows.

$$\begin{aligned} V_{2r} &= \rho_{23}\ V_2 = -0.41\ V_2 \\ &= (-0.41)\,(1.3)\ V_1 \qquad \textbf{(4-21a)} \\ &= -0.53\ V_1 \end{aligned}$$

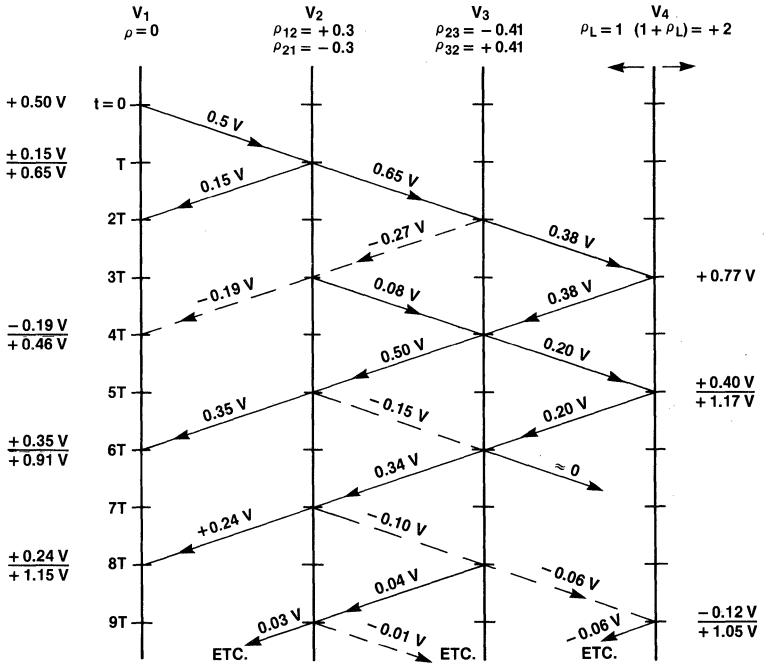
$$\begin{aligned} V_3 &= (1 + \rho_{23})\ V_2 = 0.59\ V_2 \\ &= (0.59)\,(1.3)\ V_1 \qquad \textbf{(4-21b)} \\ &= 0.77\ V_1 \end{aligned}$$

Voltage V_3 is doubled in magnitude when it arrives at the open-ended output, since ρ_L is +1. This effectively cancels the voltage divider action between R_S and Z_1.

$$\begin{aligned} V_4 &= (1 + \rho_L)\ V_3 = (1 + \rho_L)(1 + \rho_{23})\ V_2 \\ &= (1 + \rho_L)(1 + \rho_{23})(1 + \rho_{12})\ V_1 \\ &= (1 + \rho_L)(1 + \rho_{23})(1 + \rho_{12})\ \frac{V_O}{2} \qquad \textbf{(4-22)} \\ V_4 &= (1 + \rho_{23})(1 + \rho_{12})\ V_O \end{aligned}$$

Thus, *Equation 4-22* is the general expression for the initial step of output voltage for three lines when the input is series terminated and the output is open-ended.

Fig. 4-15 Lattice Diagram for the Circuit of Figure 4-14

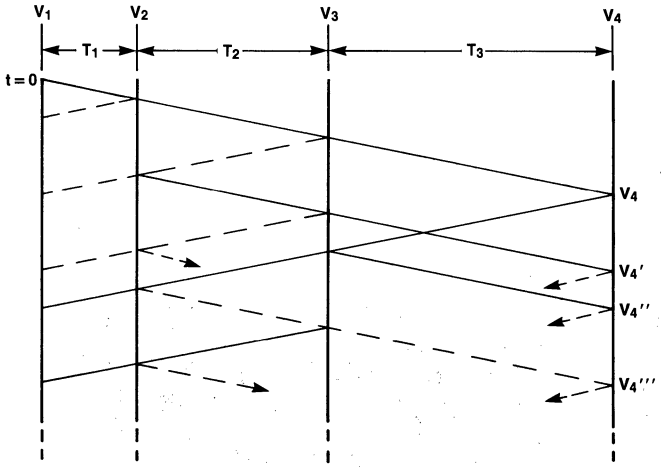


Note that the reflection coefficients at the intersections of lines 1 and 2 and lines 2 and 3 in *Figure 4-15* have reversed signs for signals traveling to the left. Thus the voltage reflected from the open output and the signal reflecting back and forth on line 2 both contribute additional increments of output voltage in the same polarity as V_O. Lines 2 and 3 have the same delay time; therefore, the two aforementioned increments arrive at the output simultaneously at time 5T on the lattice diagram *(Figure 4-15)*.

In the general case of series lines with different delay times, the vertical lines on the lattice diagram should be spaced apart in the ratio of the respective delays. *Figure 4-16* shows this for a hypothetical case with delay ratios 1:2:3. For a sequence of transmission lines with the highest impedance line in the middle, at least three output voltage increments with the same polarity as V_O occur before one can occur of opposite polarity. On the other hand, if the middle line has the lowest impedance, the polarity of the second increment of output voltage is the opposite of V_O. The third increment of output voltage has the opposite polarity, for the time delay ratios of *Figure 4-16*.

When transmitting logic signals, it is important that the initial step of line output voltage pass through the threshold region of the receiving circuit, and that the next two increments of output voltage augment the initial step. Thus in a series terminated sequence of three mismatched lines, the middle line should have the highest impedance.

Fig. 4-16 Lattice Diagram for Three Lines with Delay Ratios 1:2:3



Rise Time Versus Line Delay

When the 2-way line delay is less than the rise time of the input wave, any reflections generated at the end of the line are returned to the source before the input transition is completed. Assuming that the generator has a finite source resistance, the reflected wave adds algebraically to the input wave while it is still in transition, thereby changing the shape of the input. This effect is illustrated in *Figure 4-17,* which shows input and output voltages for several comparative values of rise time and line delay.

In *Figure 4-17b* where the rise time is much shorter than the line delay, V_1 rises to an initial value of 1 V. At time T later, V_T rises to 0.5 V, i.e., $1 + \rho_L = 0.5$. The negative reflection arrives back at the source at time 2T, causing a net change of -0.4 V, i.e., $(1 + \rho_S)(-0.5) = -0.4$.

The negative coefficient at the source changes the polarity of the other 0.1 V of the reflection and returns it to the end of the line, causing V_T to go positive by another 50 mV at time 3T. The remaining 50 mV is inverted and reflected back to the source, where its effect is barely distinguishable as a small negative change at time 4T.

In *Figure 4-17c,* the input rise time (0 to 100%) is increased to such an extent that the input ramp ends just as the negative reflection arrives back at the source end. Thus the input rise time is equal to 2T.

The input rise time is increased to 4T in *Figure 4-17d,* with the negative reflection causing a noticeable change in input slope at about its midpoint. This change in slope is more visible in the double exposure photo of *Figure 4-17e,* which shows V_1 (t_r still set for 4T) with and without the negative reflection. The reflection was eliminated by terminating the line in its characteristic impedance.

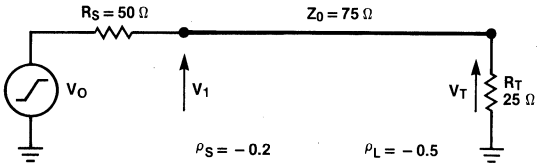
The net input voltage at any particular time is determined by adding the reflection to the otherwise unaffected input. It must be remembered that the reflection arriving back at the input at a given time is proportional to the input voltage at a time 2T earlier. The value of V_1 in *Figure 4-17d* can be calculated by starting with the 1 V input ramp.

$$V_1 = \frac{1}{t_r} \bullet t \quad \text{for } 0 \le t \le 4T \qquad \textbf{(4-23)}$$

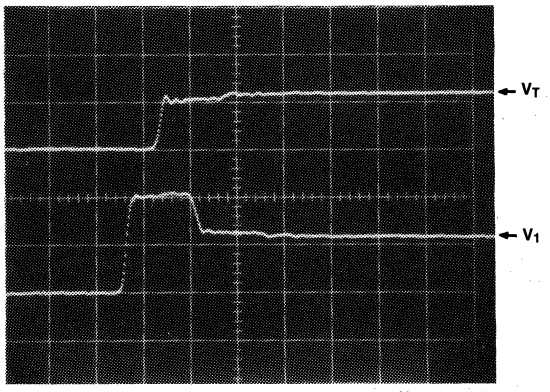
$$= 1\ V \quad \text{for } t \ge 4T$$

Fig. 4-17 Line Voltages for Various Ratios of Rise Time to Line Delay

a. Test Arrangement for Rise Time Analysis

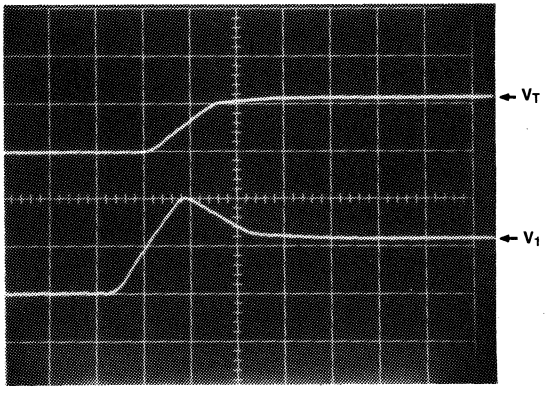


b. Line Voltages for $t_r \ll T$



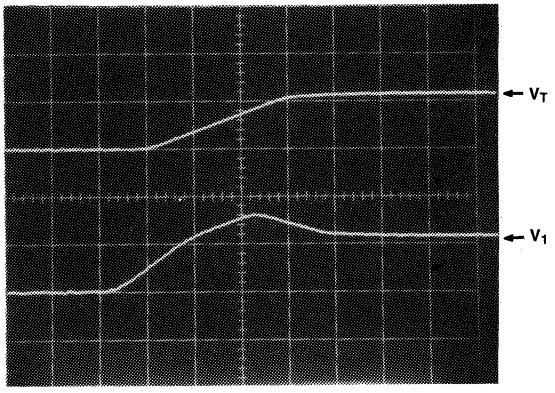
H = 10 ns/div
V = 0.5 V/div

c. Line Voltages for $t_r = 2T$



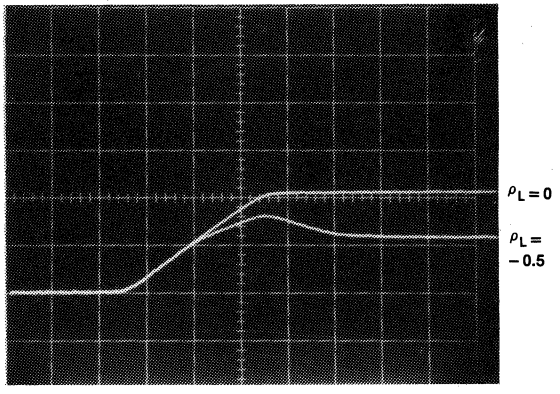
H = 10 ns/div
V = 0.5 V/div

d. Line Voltages for $t_r = 4T$



H = 10 ns/div
V = 0.5 V/div

e. Input Voltage With and Without Reflection



H = 10 ns/div
V = 0.5 V/div

The reflection from the end of the line is

$$V_r = \frac{\rho_L\,(t - 2T)}{t_r}\;; \qquad \textbf{(4-24)}$$

the portion of the reflection that appears at the input is

$$V_r' = \frac{(1 + \rho_S)\,\rho_L\,(t - 2T)}{t_r}\;; \qquad \textbf{(4-25)}$$

the net value of the input voltage is the sum.

$$V_1' = \frac{t}{t_r} + \frac{(1 + \rho_S)\,\rho_L\,(t - 2T)}{t_r} \qquad \textbf{(4-26)}$$

The peak value of the input voltage in *Figure 4-17d* is determined by substituting values and letting t equal 4T.

$$V_1' = 1 + \frac{(0.8)\,(-0.5)\,(4T - 2T)}{t_r}$$
$$= 1 - 0.4\,(0.5) = 0.8\ V \qquad \textbf{(4-27)}$$

After this peak point, the input ramp is no longer increasing but the reflection is still arriving. Hence the net value of the input voltage decreases. In this example, the later reflections are too small to be detected and the input voltage is thus stable after time 6T. For the general case of repeated reflections, the net voltage $V_{1(t)}$ seen at the driven end of the line can be expressed as follows, where the signal caused by the generator is $V_{1(t)}$.

$$V_{1(t)}' = V_{1(t)} \quad \text{for } 0 < t < 2T$$

$$V'_{1(t)} = V_{1(t)} + (1 + \rho_S)\,\rho_L\,V_{1(t-2T)} \quad \text{for } 2T < t < 4T$$

$$V_{1(t)}' = V_{1(t)} + (1 + \rho_S)\,\rho_L\,V_{1(t-2T)} + (1 + \rho_S)\,\rho_S\rho_L^2 V_{1(t-4T)} \quad \text{for } 4T < t < 6T \qquad \textbf{(4-28)}$$

$$V_{1(t)}' = V_{1(t)} + (1 + \rho_S)\,\rho_L\,V_{1(t-2T)} + (1 + \rho_S)\,\rho_S\rho_L^2 V_{1(t-4T)} + (1 + \rho_S)\,\rho_S^2\rho_L^3 V_{1(t-6T)} \quad \text{for } 6T < t < 8T, \text{ etc.}$$

The voltage at the output end of the line is expressed in a similar manner.

$$V_{T(t)} = 0 \quad \text{for } 0 < t < T$$

$$V_{T(t)} = (1 + \rho_L)\,V_{1(t-T)} \quad \text{for } T < t < 3T$$

$$V_{T(t)} = (1 + \rho_L)\,V_{1(t-T)} + (1 + \rho_L)\,\rho_S\rho_L\,V_{1(t-3T)} \quad \text{for } 3T < t < 5T \qquad \textbf{(4-29)}$$

$$V_{T(t)} = (1 + \rho_L)\,V_{1(t-T)} + (1 + \rho_L)\,\rho_S\rho_L V_{1(t-3T)} + (1 + \rho_L)\,\rho_S^2\rho_L^2\,V_{1(t-5T)} \quad \text{for } 5T < t < 7T, \text{ etc.}$$

Ringing

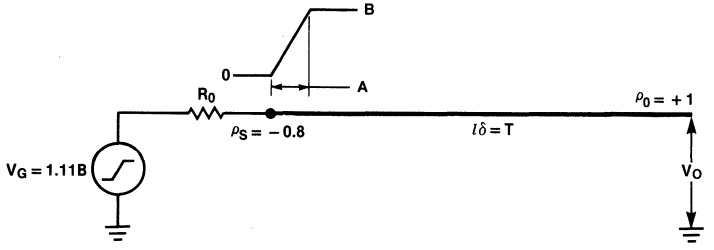
Multiple reflections occur on a transmission line when neither the signal source impedance nor the termination (load) impedance matches the line impedance. When the source reflection coefficient ρ_S and the load reflection coefficient ρ_L are of opposite polarity, the reflections alternate in polarity. This causes the signal voltage to oscillate about the final steady state value, commonly recognized as ringing.

When the signal rise time is long compared to the line delay, the signal shape is distorted because the individual reflections overlap in time. The basic relationships among rise time, line delay, overshoot and undershoot are shown in a simplified diagram, *Figure 4-18*. The incident wave is a ramp of amplitude B and rise duration A. The reflection coefficient at the open-ended line output is +1 and the source reflection coefficient is assumed to be −0.8, *i.e.*, $R_0 = Z_0/9$.

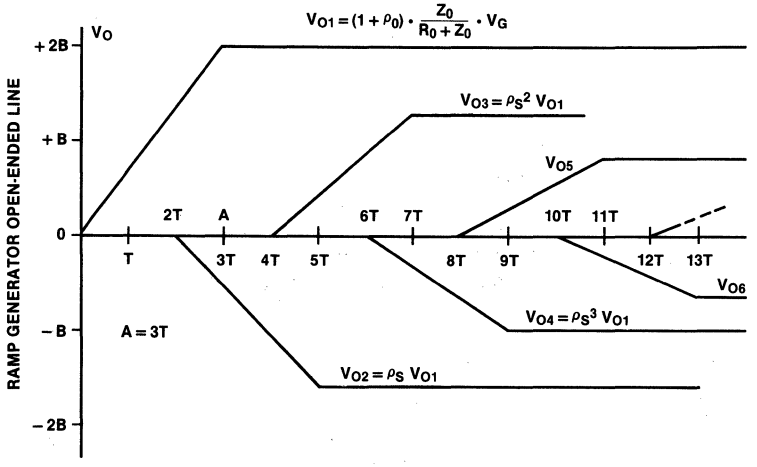
Figure 4-18b shows the individual reflections treated separately. Rise time A is assumed to be three times the line delay T. The time scale reference is the line output and the first increment of output voltage V_O rises to 2B in the time interval A. Simultaneously, a positive reflection (not shown) of amplitude B is generated and travels to the source, whereupon it is multiplied by −0.8 and

Fig. 4-18 Basic Relationships Involved in Ringing

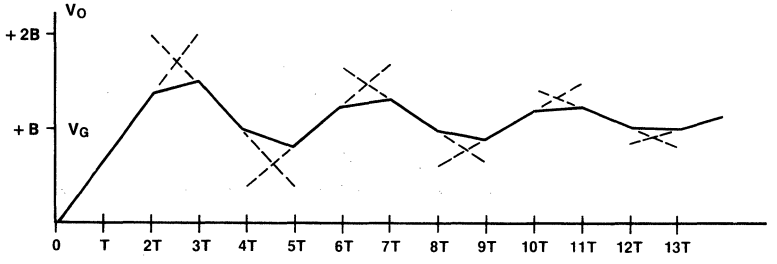
a. Ramp Generator Driving Open-ended Line



b. Increments of Output Voltage Treated Individually



c. Net Output Signal Determined by Superposition



returns toward the end of the line. This negative-going ramp starts at time 2T (twice the line delay) and doubles to -1.6B at time 2T + A.

The negative-going increment also generates a reflection of amplitude -0.8B which makes the round trip to the source and back, appearing at time 4T as a positive ramp rising to +1.28B at time 4T + A. The process of reflection and re-reflection continues, and each successive increment changes in polarity and has an amplitude of 80% of the preceding increment.

In *Figure 4-18c,* the output increments are added algebraically by superposition. The starting point of each increment is shifted upward to a voltage value equal to the algebraic sum of the quiescent levels of all the preceding increments (*i.e.,* 0, 2B, 0.4B, 1.68B, etc.). For time intervals when two ramps occur simultaneously, the two linear functions add to produce a third ramp that prevails during the overlap time of the two increments.

It is apparent from the geometric relationships, that if the ramp time A is less than twice the line delay, the first output increment has time to rise to the full 2B amplitude and the second increment reduces the net output voltage to 0.4B. Conversely, if the line delay is very short compared to the ramp time, the excursions about the final value V_G are small.

Figure 4-18c shows that the peak of each excursion is reached when the earlier of the two constituent ramps reaches its maximum value, with the result that the first peak occurs at time A. This is because the earlier ramp has a greater slope (absolute value) than the one that follows.

Actual waveforms such as produced by ECL or TTL do not have a constant slope and do not start and stop as abruptly as the ramp used in the example of *Figure 4-18.* Predicting the time at which the peaks of overshoot and undershoot occur is not as simple as with ramp excitation. A more rigorous treatment is required, including an expression for the driving waveform which closely simulates its actual shape. In the general case, a peak occurs when the sum of the slopes of the individual signal increment is zero.

Summary

The foregoing discussions are by no means an exhaustive treatment of transmission line characteristics. Rather, they are intended to focus attention on the general methods used to determine the interactions between high-speed logic circuits and their interconnections. Considering an interconnection in terms of distributed rather than lumped inductance and capacitance leads to the line impedance concept, i.e., mismatch between this characteristic impedance and the terminations causes reflections and ringing.

Series termination provides a means of absorbing reflections when it is likely that discontinuities and/or line impedance changes will be encountered. A disadvantage is that the incident wave is only one-half the signal swing, which limits load placement to the end of the line. ECL input capacitance increases the rise time at the end of the line, thus increasing the effective delay. With parallel termination, i.e., at the end of the line, loads can be distributed along the line. ECL input capacitance modifies the line characteristics and should be taken into account when determining line delay.

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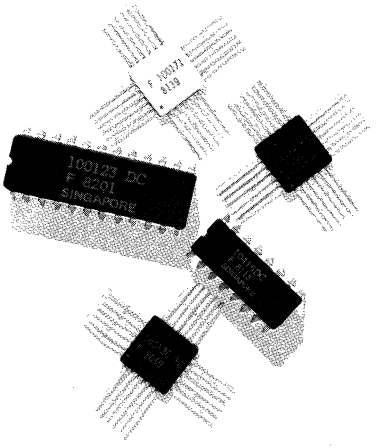


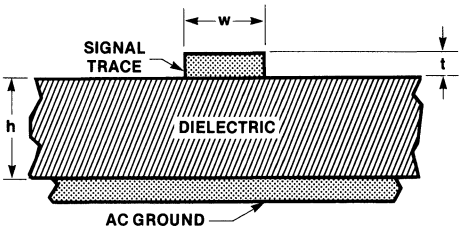
Chapter 5
System Considerations

Introduction
All of Fairchild's ECL input and output impedances are designed to accommodate various methods of driving and terminating interconnections. Controlled wiring impedance makes it possible to use simplified equivalent circuits to determine limiting conditions. Specific guidelines and recommendations are based on assumed worst-case combinations. Many of the recommendations may seem conservative, compared to typical observations, but the intent is to help the designer achieve a reliable system in a reasonable length of time with a minimum amount of redesign.

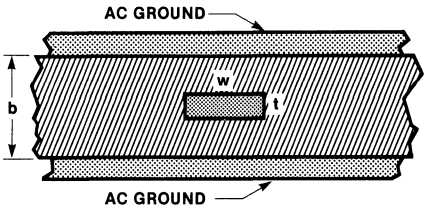
PC Board Transmission Lines
Strictly speaking, transmission lines are not always required for F100K ECL but, when used, they provide the advantages of predictable interconnect delays as well as reflection and ringing control through impedance matching. Two common types of PC board transmission lines are microstrip and stripline, *Figure 5-1*. Stripline requires multilayer construction techniques; microstrip uses ordinary double-clad boards. Other board construction techniques are wire wrap, stitch weld and discrete wired.

Fig. 5-1 Transmission Lines on Circuit Boards

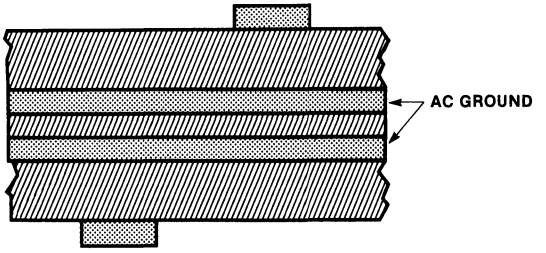
a. Microstrip



b. Stripline



c. Composite Microstrip



Stripline, *Figure 5-1b,* is used where packing density is a high priority because increasing the interconnect layers provides short signal paths. Boards with as many as 14 layers have been used in ECL systems.

Microstrip offers easier fabrication and higher propagation velocity than stripline, but the routing for a complex system may require more design effort. In *Figure 5-1a,* the ground plane can be a part of the V_{EE} distribution as long as adequate bypassing from V_{EE} to V_{CC} (ground) is provided. Also, signal routing is simplified and an extra voltage plane is obtained by bonding two microstrip structures back to back, *Figure 5-1c.*

Microstrip
Equation 5-1 relates microstrip characteristic impedance to the dielectric constant and dimensions.[1] Electric field fringing requires that the ground extend beyond each edge of the signal trace by a distance no less than the trace width.

$$Z_0 = \left(\frac{60}{\sqrt{0.475\,\epsilon_r + 0.67}}\right) \ln\left(\frac{4h}{0.67\,(0.8\,w + t)}\right)$$

$$= \left(\frac{87}{\sqrt{\epsilon_r + 1.41}}\right) \ln\left(\frac{5.98\,h}{0.8\,w + t}\right) \qquad \textbf{(5-1)}$$

where h = dielectric thickness, w = trace width, t = trace thickness, ϵ_r = board material dielectric constant relative to air.

Equation 5-1 was developed from the impedance formula for a wire over ground plane transmission line, *Equation 5-2.*

$$Z_0 = \left(\frac{60}{\sqrt{\epsilon_r}}\right) \ln \left(\frac{4h}{d}\right) \qquad \textbf{(5-2)}$$

where d = wire diameter, h = distance from ground to wire center.

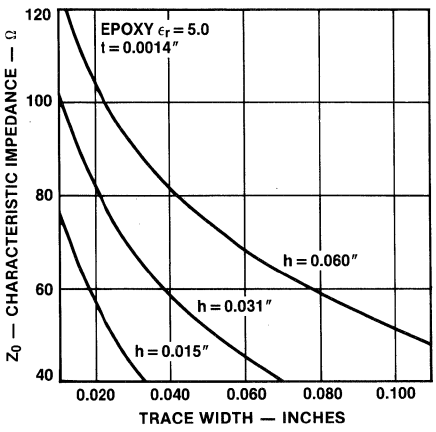
Comparing *Equation 5-1* and 5-2, the term 0.67 (0.8 w + t) shows the equivalence between a round wire and a rectangular conductor. The term 0.475 ϵ_r + 0.67 is the *effective* dielectric constant for microstrip, considering that a microstrip line has a compound dielectric consisting of the board material and air. The effective dielectric constant is determined by measuring propagation delay per unit of line length and using the following relationship.

$$\delta = 1.016 \bullet \sqrt{\epsilon_r} \quad ns/ft \qquad \textbf{(5-3)}$$

where δ = propagation delay, ns/ft.

Propagation delay is a property of the dielectric material rather than line width or spacing. The coefficient 1.016 is the reciprocal of the velocity of light in free space. Propagation delay for microstrip lines on glass-filled G-10 epoxy boards is typically 1.77 ns/ft, yielding an effective dielectric constant of 3.04.

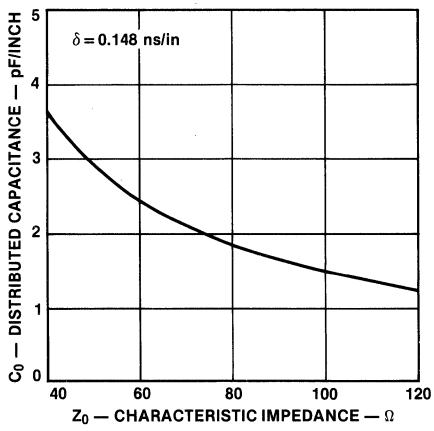
Fig. 5-2 Microstrip Impedance Versus Trace Width, G-10 Epoxy



Using ϵ_r = 5.0 in *Equation 5-1, Figure 5-2* provides microstrip line impedance as a function of width for several G-10 epoxy board thicknesses. *Figure 5-3* shows the related C_0 values, useful for determining capacitive loading effects on line characteristics, *(Equation 4-15).*

System designers should ascertain tolerances on board dimensions, dielectric constant and trace width etching in order to determine impedance variations. If conformal coating is used the effective dielectric constant of microstrip is increased, depending on the coating material and thickness.

Fig. 5-3 Microstrip Distributed Capacitance Versus Impedance, G-10 Epoxy



Stripline

Stripline conductors are totally imbedded. As a result, the board material determines the dielectric constant. G-10 epoxy boards have a typical propagation delay of 2.26 ns/ft. *Equation 5-4* is used to calculate stripline impedances.[1-2]

$$Z_0 = \left(\frac{60}{\sqrt{\epsilon_r}}\right) \ln \left(\frac{4b}{0.67\,\pi\,(0.8\,w + t)}\right) \qquad \textbf{(5-4)}$$

where b = distance between ground planes,
w = trace width, t = trace thickness,
w/(b-t) < 0.35 and t/b < 0.25.

Figure 5-4 shows stripline impedance as a function of trace width, using *Equation 5-4* and various ground plane separations for G-10 glass-filled epoxy boards. Related values of C_0 are plotted in *Figure 5-5.*

Fig. 5-4 Stripline Impedance Versus Trace Width, G-10 Epoxy

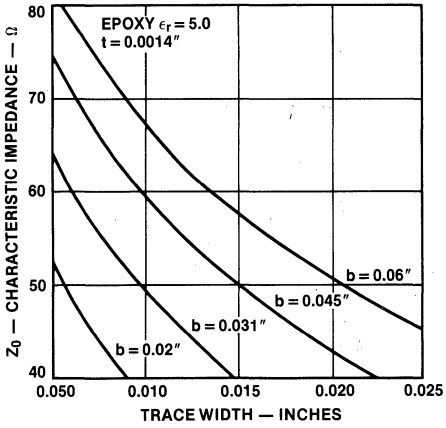
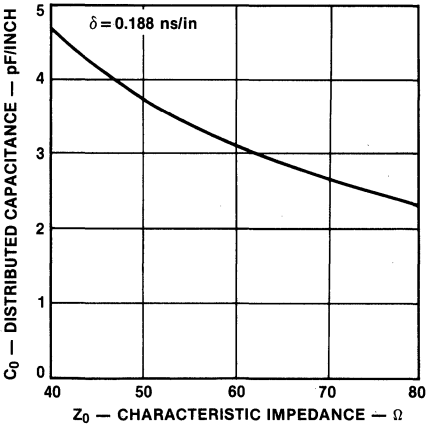


Fig. 5-5 Stripline Distributed Capacitance Versus Impedance, G-10 Epoxy



Wire Wrap

Wire-wrap boards are commercially available with three voltage planes, positions for several 24-pin Dual In-line Packages (DIP), terminating resistors, and decoupling capacitors. The devices are mounted on socket pins and interconnected with twisted pair wiring. One wire at each end of the twisted pair is wrapped around a signal pin, the other around a ground pin. The #30 insulated wire is uniformly twisted to provide a nominal 93 Ω impedance line. Positions for Single In-line Package (SIP) terminating resistors are close to the inputs to provide good termination characteristics.

Stitch Weld

Stitch-weld boards are commercially available with three voltage planes and buried resistors between planes. The devices are mounted on terminals and interconnected with insulated wires that are welded to the backside of the terminals. The insulated wires are placed on a controlled thickness over the ground plane to provide a nominal impedance of 50 Ω. The boards are available for both DIPs and flatpaks. Use of flatpaks can increase package density and provide higher system performance.

Discrete Wired

Custom Multiwire* boards are available with integral power and ground planes. Wire is placed on a controlled thickness above the ground plane to obtain a nominal impedance line of 55 Ω. Then holes are drilled through the wire and board. Copper is deposited in the drilled holes by an additive-electrolysis process which bonds each wire to the wall of the holes. Devices are soldered on the board to make connection to the wires.

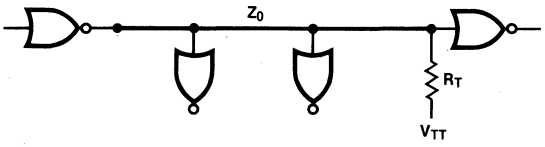
Parallel Termination

Terminating a line at the receiving end with a resistance equal to the characteristic line impedance is called parallel termination, *Figure 5-6a.* F100K circuits do not have internal pull-down resistors on outputs, so the terminating resistor must be returned to a voltage more negative than V_{OL} to establish the LOW-state output voltage from the emitter follower. A −2 V termination return supply is commonly used. This minimizes power consumption and correlates with standard test specifications for ECL circuits. A pair of resistors connected in series between ground (V_{CC}) and the V_{EE} supply can

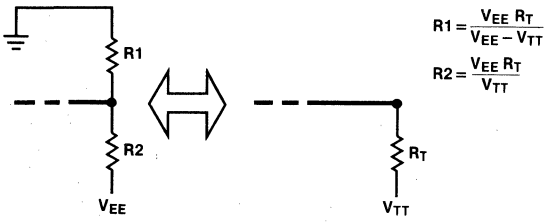
*Multiwire is a registered trademark of the Multiwire Corporation.

Fig. 5-6 Parallel Termination

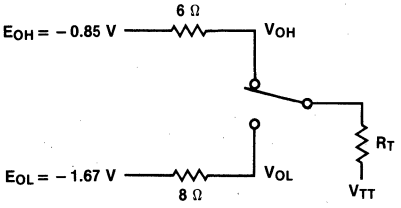
a. Parallel Termination



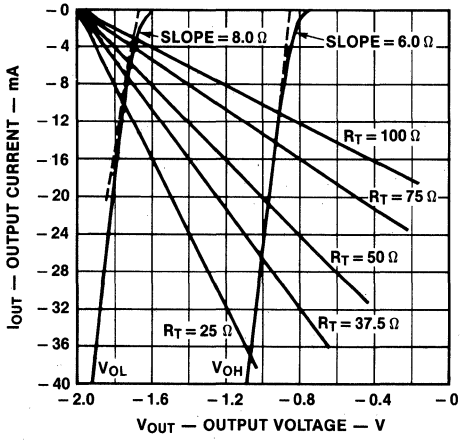
b. Thevenin Equivalent of R_T and V_{TT}



c. Equivalent Circuit for Determining Approximate V_{OH} and V_{OL} Levels



d. F100K Output Characteristic with Terminating Resistor R_T Returned to V_{TT} = −2.0 V



provide the Thevenin equivalent of a single resistor to −2 V if a separate termination supply is not available, *Figure 5-6b.* The average power dissipation in the Thevenin equivalent resistors is about 10 times the power dissipation in the single resistor returned to −2 V, as shown in *Figures 6-10* and *6-13.* For either parallel termination method, decoupling capacitors are required between the supply and ground *(Chapter 6).*

F100K output transistors are designed to drive low-impedance loads and have a maximum output current rating of 50 mA. The circuits are specified and tested with a 50 Ω load returned to −2 V. This gives nominal output levels of −0.955 V at 20.9 mA and −1.705 V at 5.9 mA. Output levels will be different with other load currents because of the transistor output resistance. This resistance is nonlinear with load current since it is due, in part, to the base-emitter voltage of the emitter follower, which is logarithmic with output current. With the standard 50 Ω load, the effective source resistance is approximately 6 Ω in the HIGH state and 8 Ω in the LOW state.

The foregoing values of output voltage, output current, and output resistance are used to estimate quiescent output levels with different loads. An equivalent circuit is shown in *Figure 5-6c.* The ECL circuit is assumed to contain two internal voltage sources E_{OH} and E_{OL} with series resistances of 6 Ω and 8 Ω respectively. The values shown for E_{OH} and E_{OL} are −0.85 V and −1.67 V respectively.

The linearized portion of the F100K output characteristic can be represented by two equations:

For V_{OH}: $V_{OUT} = -850 - 6\, I_{OUT}$

For V_{OL}: $V_{OUT} = -1670 - 8\, I_{OUT}$

where I_{OUT} is in mA, V_{OUT} is in mV.

If the range of I_{OUT} is confined between 8 mA to 40 mA for V_{OH}, and 2 mA to 16 mA for V_{OL}, the output voltage can be estimated within ± 10 mV *(Figure 5-6d).*

An ECL output can drive two or more lines in parallel, provided the maximum rated current is not exceeded. Another consideration is the effect of various loads on noise margins. For example, two parallel 75 Ω terminations to −2 V *(Figure 5-6d)* give output levels of

approximately −1.000 V and −1.716 V. Noise margins are thus 35 mV less in the HIGH state and 11 mV more in the LOW state, compared to 50 Ω load conditions. Conversely, a single 75 Ω load to −2 V causes noise margins 38 mV greater in the HIGH state and 11 mV less in the LOW state, compared to a 50 Ω load.

The magnitude of reflections from the terminated end of the line depends on how well the termination resistance R_T matches the line impedance Z_0. The ratio of the reflected voltage to the incident voltage V_i is the reflection coefficient ρ.

$$\frac{V_r}{V_i} = \rho = \frac{R_T - Z_0}{R_T + Z_0} \qquad \textbf{(5-5)}$$

The initial signal swing at the termination is the sum of the incident and reflected voltages. The ratio of termination signal to incident signal is thus:

$$\frac{V_T}{V_i} = 1 + \rho = \frac{2R_T}{R_T + Z_0} \qquad \textbf{(5-6)}$$

The degree of reflections which can be tolerated varies in different situations, but to allow for worst-case circuits, a good rule to thumb is to limit reflections to 15% to prevent excursions into the threshold region of the ECL inputs connected along the line. The range of permissible values of R_T as a function of Z_0 and the reflection coefficient limitations can be determined by rearranging *Equation 5-5.*

$$R_T = Z_0 \frac{1 + \rho}{1 - \rho} \qquad \textbf{(5-7)}$$

Using 15% reflection limits as examples, the range of the R_T/Z_0 ratio is as follows.

$$\frac{1.15}{0.85} > \frac{R_T}{Z_0} > \frac{0.85}{1.15} \qquad 1.35 > \frac{R_T}{Z_0} > 0.74 \qquad \textbf{(5-8)}$$

The permissible range of the R_T/Z_0 ratio determines the tolerance ranges for R_T and Z_0. For example, using the foregoing ratio limits, R_T tolerances of ± 10% allow Z_0 tolerance limits of +22% and −19%; R_T tolerances of ± 5% allow Z_0 tolerance limits of +28% and −23%.

An additional requirement on the maximum value of R_T is related to the value of quiescent I_{OH} current needed to insure sufficient negative-going signal swing when the ECL driver switches from the HIGH state to the LOW state. The npn emitter-follower output of the ECL circuit cannot act as a voltage source driver for negative-going transitions. When the voltage at the base of the emitter follower starts going negative as a result of an internal state change, the output current of the emitter follower starts to decrease. The transmission line responds to the decrease in current by producing a negative-going change in voltage. The ratio of the voltage change to the current change is, of course, the characteristic impedance Z_0. Since the maximum decrease in current that the line can experience is from I_{OH} to zero, the maximum negative-going transition which can be produced is the product $I_{OH} Z_0$.

If the $I_{OH} Z_0$ product is greater than the normal negative-going signal swing, the emitter follower responds by limiting the current change, thereby controlling the signal swing. If, however, the $I_{OH} Z_0$ product is too small, the emitter follower is momentarily turned off due to insufficient forward bias of its base-emitter junctions, causing a discontinuous negative-going edge such as the one shown in *Figure 5-14.* In the output-LOW state the emitter follower is essentially non-conducting for V_{OL} values more positive than about −1.55 V. Using this value as a criterion and expressing I_{OH} and V_{OH} in terms of the equivalent circuit of *Figure 5-6c,* an upper limit on the value of R_T can be developed.

$$\Delta V = I_{OH} Z_0 > 1.55 - |V_{OH}|$$

$$\left(\frac{E_{OH} - V_{TT}}{R_0 + R_T}\right) Z_0 > 1.55 - \left|\frac{V_{TT} R_0 = E_{OH} R_T}{R_0 + R_T}\right|$$

$$R_T < \frac{(E_{OH} - V_{TT}) Z_0 - (1.55 - |V_{TT}|) R_0}{1.55 - |E_{OH}|} \qquad \textbf{(5-9)}$$

For a V_{TT} of −2 V, R_0 of 6 Ω and E_{OH} of −0.85 V, *Equation 5-9* reduces to

$$R_T < 1.64 Z_0 + 3.86\ \Omega$$

For Z_0 = 50 Ω, the emitter follower cuts off during a negative-going transition if R_T exceeds 86 Ω. Changing

the voltage level criteria to −1.60 V to insure continuous conduction in the emitter follower gives an upper limit of 77 Ω for a 50 Ω line. For a line terminated at the receiving end with a resistance to −2 V, a rough rule-of-thumb is that termination resistance should not exceed line impedance by more than 50%. This insures a satisfactory negative-going signal swing to ECL inputs connected along the line. The quiescent V_{OL} level, after all reflections have damped out, is determined by R_T and the ECL output characteristic.

The input impedance of ECL circuits is predominately capacitive. A single-function input has an effective value of about 1.5 pF for F100K flatpak, as determined by its effect on reflected and transmitted signals on transmission lines. In practical calculations, a value of 2 pF should be used. Approximately one third of this capacitance is attributed to the internal circuitry and two thirds to the flatpak pin and internal bonding.

For F100K flatpak circuits, multiple input lines may appear to have up to 3 to 4 pF but never more. For example, in the F100102, an input is connected internally to all five gates, but because of the philosophy of buffering these types of inputs in the F100K family this input appears as a unit load with a capacitance of approximately 2 pF. For applications such as a data bus, with two or more outputs connected to the same line, the capacitance of a passive-LOW output can be taken as 2 pF.

Capacitive loads connected along a transmission line increase the propagation delay of a signal along the line. The modified delay can be determined by treating the load capacitance as an increase in the intrinsic distributed capacitance of the line, discussed in *Chapter 4*. The intrinsic capacitance of any stubs which connect the inputs to the line should be included in the load capacitance. The intrinsic capacitance per unit length for G-10 epoxy boards is shown in *Figures 5-3* and *5-5* for microstrip and stripline respectively. For other dielectric materials, the intrinsic capacitance C_0 can be determined by dividing the intrinsic delay δ *(Equation 5-3)* by the line impedance Z_0.

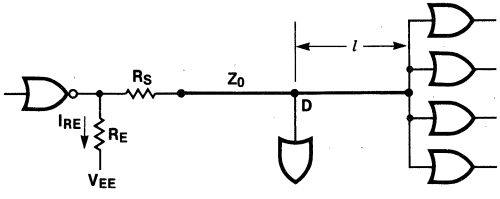
The length of a stub branching off the line to connect an input should be limited to insure that the signal continuing along the line past the stub has a continuous rise, as opposed to a rise (or fall) with several partial steps. The point where a stub branches off the line is a low impedance point. This creates a negative coefficient of reflection, which in turn reduces the amplitude of the incident wave as it continues beyond the branch point. If the stub length is short enough, however, the first reflection returning from the end of the stub adds to the attenuated incident wave while it is still rising. The sum of the attenuated incident wave and the first stub reflection provides a step-free signal, although its rise time will be longer than that of the original signal. Satisfactory signal transitions can be assured by restricting stub lengths according to the recommendations for unterminated lines *(Figure 5-10)*. The same considerations apply when the termination resistance is not connected at the end of the line; a section of line continuing beyond the termination resistance should be treated as an unterminated line and its length restricted accordingly.

Series Termination

Series termination requires a resistor between the driver and transmission line, *Figure 5-7*. The receiving end of the line has no termination resistance. The series resistor value should be selected so that when added to the driver source resistance, the total resistance equals the line impedance. The voltage divider action between the net series resistance and the line impedance causes an incident wave of half amplitude to start down the line. When the signal arrives at the unterminated end of the line, it doubles and is thus restored to a full amplitude. Any reflections returning to the source are absorbed without further reflection since the line and source impedance match. This feature, source absorption, makes series termination attractive for interconnection paths involving impedance discontinuities, such as occur in backplane wiring.

A disadvantage of series termination is that driven inputs must be near the end of the line to avoid receiving a 2-step signal. The initial signal at the driver end is half amplitude, rising to full amplitude only after the reflec-

Fig. 5-7 Series Termination



tion returns from the open end of the line. In *Figure 5-7,* one load is shown connected at point D, away from the line end. This input receives a full amplitude signal with a continuous edge if the distance *l* to the open end of the line is within recommended lengths for unterminated lines *(Figure 5-10).*

The signal at the end has a slower rise time than the incident wave because of capacitive loading. The increase in rise time to the 50% point effectively increases the line propagation delay, since the 50% point of the signal swing is the input signal timing reference point. This added delay as a function of the product of line impedance and load capacitance is discussed in *Chapter 4.*

Quiescent V_{OH} and V_{OL} levels are established by resistor R_E *(Figure 5-7),* which also acts with V_{EE} to provide the negative-going drive into R_S and Z_0 when the driver output goes to the LOW state. To determine the appropriate R_E value, the driver output can be treated as a simple mechanical switch which opens to initiate the negative-going swing. At this instant, Z_0 acts as a linear resistor returned to V_{OH}. Thus the components form a simple circuit of R_E, R_S and Z_0 in a series, connected between V_{EE} and V_{OH}. The initial current in this series circuit must be sufficient to introduce a 0.38 V transient into the line, which then doubles at the load end to give 0.75 V swing.

$$I_{RE} = \frac{V_{OH} - V_{EE}}{R_E + R_S + Z_0} \geq \frac{0.38}{Z_0} \qquad \textbf{(5-10)}$$

Any I_{OH} current flowing in the line before the switch opens helps to generate the negative swing. This current may be quite small, however, and should be ignored when calculating R_E.

Increasing the minimum signal swing into the line by 30% to 0.49 V insures sufficient pull-down current to handle reflection currents caused by impedance discontinuities and load capacitance. The appropriate R_E value is determined from the following relationship.

$$\frac{V_{OH} - V_{EE}}{R_E + R_S + Z_0} \geq \frac{0.49}{Z_0} \qquad \textbf{(5-11)}$$

For the R_E range normally used, quiescent V_{OH} averages approximately 0.955 V and $V_{EE} = -4.5$ V. The value of R_S is equal to Z_0 minus R_0 (R_0 averages 7 Ω). Inserting these values and rearranging *Equation 5-11* gives the following.

$$R_E \leq 5.23\, Z_0 + 7\ \Omega \qquad \textbf{(5-12)}$$

Power dissipation in R_E is listed in *Figure 6-14.* The power dissipation in R_E is greater than in R_T of a parallel termination to −2 V, but still less than the two resistors of the Thevenin equivalent parallel termination, see *Figures 6-10, 6-13 and 6-14.*

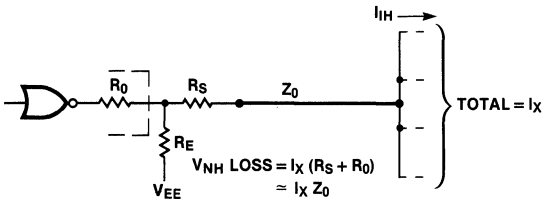
The number of driven inputs on a series terminated line is limited by the voltage drop across R_S in the quiescent HIGH state, caused by the finite input currents of the ECL loads. I_{IH} values are specified on data sheets for various types of inputs, with a worst-case value of 265 μA for simple gate inputs. The voltage drop subtracts from the HIGH-state noise margin as outlined in *Figure 5-8a.*

However, there is more HIGH-state noise margin initially, because there is less I_{OH} with the R_E load than with the standard 50 Ω load to −2 V. This makes V_{OH} more positive; the increase ranges from 43 mV for a 50 Ω line to 82 mV for a 100 Ω line. Using this V_{OH} increase as a limit on the voltage drop across R_S assures that the HIGH-state noise margin is as good as in the parallel terminated case. Dividing the V_{OH} increase by $R_S + R_0$ ($=Z_0$) gives the allowed load input current (I_X in *Figure 5-8a*). This works out to 0.86 mA for a 50 Ω line, 0.92 mA for a 75 Ω line, and 0.82 mA for a 100 Ω line. Load input current greater than these values can be tolerated at some sacrifice in noise margin. If, for example, an additional 50 mV loss is feasible, the maximum values of current become 1.86 mA, 1.59 mA, and 1.32 mA for 50 Ω, 75 Ω and 100 Ω lines respectively.

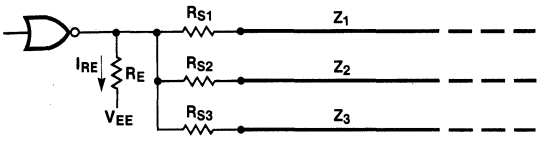
An ECL output can drive more than one series terminated line, as suggested in *Figure 5-8b,* if the maximum rated output current of 50 mA is not exceeded. Also, driving two or more lines requires a lower R_E value. This makes the quiescent I_{OH} higher and consequently V_{OH} lower, due to the voltage drop across R_0. This voltage drop decreases the HIGH-state noise margin, which may become the limiting factor (rather than the maximum rated current), depending on the particular application.

Fig. 5-8 Loading Considerations for Series Termination

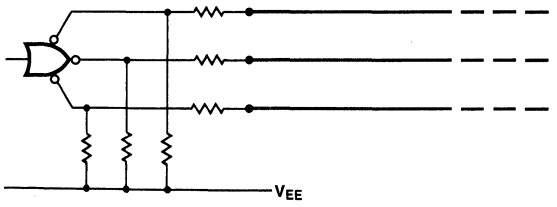
a. Noise Margin Loss Due to Load Input Current



b. Driving Several Lines from One Output



c. Using Multiple Output Element for Load Sharing



The appropriate R_E value can be determined using *Equation 5-13* for $V_{EE} = -4.5$ V.

$$\frac{1}{R_E} \geq \frac{1}{6.23\,Z_1 - R_{S1}} + \frac{1}{6.23\,Z_2 - R_{S2}} + \frac{1}{6.23\,Z_3 - R_{S3}} \qquad \textbf{(5-13)}$$

Circuits with multiple outputs (such as the F100112) provide an alternate means of driving several lines simultaneously *(Figure 5-8c)*. Note, each output should be treated individually when assigning load distribution, line impedance, and R_E value.

Unterminated Lines

Lines can be used without series or parallel termination if the line delay is short compared to the signal rise time. Ringing occurs because the reflection coefficient at the open (receiving) end of the line is positive (nominally +1) while the reflection coefficient at the driving end is negative (approximately −0.8). These opposite polarity reflection coefficients cause any change in signal voltage to be reflected back and forth, with a polarity change each time the signal is reflected from the driver. Net voltage change on the line is thus a succession of increments with alternating polarity and decreasing magnitude. The algebraic sum of these increments is the observed ringing. The general relationships among rise time, line delay, overshoot and undershoot are discussed in *Chapter 4,* using simple waveforms for clarity.

Excessive overshoot on the positive-going edge of the signal drives input transistors into saturation. Although this does not damage an ECL input, it does cause excessive recovery times and makes propagation delays unpredictable. Undershoot (following the overshoot) must also be limited to prevent signal excursions into the threshold region of the loads. Such excursions could cause exaggerated transition times at the driven circuit outputs, and could also cause multiple triggering of sequential circuits. Signal swing, exclusive of ringing, is slightly greater on unterminated lines than on parallel terminated lines; I_{OH} is less and I_{OL} is greater with the R_E load, *(Figure 5-9a)* making V_{OH} higher and V_{OL} lower.

For worst case combinations of driver output and load input characteristics, a 35% overshoot limit insures that system speed is not compromised either by saturating an input on overshoot or extending into the threshold region on the following undershoot.

For distributed loading, ringing is satisfactorily controlled if the 2-way modified line delay does not exceed the 20% to 80% rise time of the driver output. This relationship can be expressed as follows, using the symbols from *Chapter 4* and incorporating the effects of load capacitance on line delay.

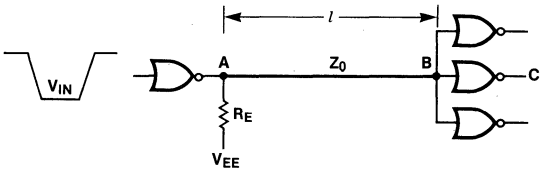
$$t_r = 2T' = 2l\delta' = 2l\delta\sqrt{1 + \frac{C_L}{lC_0}}$$

Solving this expression for the line length (l):

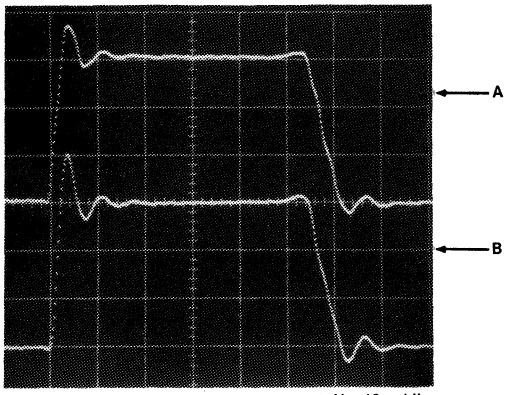
$$l_{max} = \frac{1}{2}\sqrt{\left(\frac{C_L}{C_0}\right)^2 + \left(\frac{t_r}{\delta}\right)^2} - \frac{C_L}{2C_0} \qquad \textbf{(5-14)}$$

Fig. 5-9 Effect of R_E Value on Trailing-edge Propagation

a. Unterminated Line

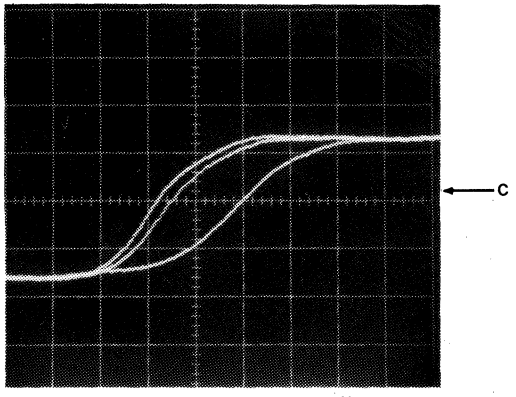


b. Line Voltages Showing Stair-step Trailing Edges



H = 10 ns/div
V = 0.3 V/div

c. Load Gate Output Showing Net Propagation Increase for Increasing Values of R_E: 330 Ω, 510 Ω, 1 kΩ



H = 1 ns/div
V = 0.3 V/div

The shorter the rise time, the shorter the permissible line length. For F100K ECL, the minimum rise time from 20% to 80% is specified as 0.5 ns. Using this rise time and 2 pF per fan-out load, calculated maximum line lengths for G-10 epoxy microstrip are listed in *Figure 5-10a.* The length (l) in the table is the distance from the terminating resistor to the input of the device(s). For F100K ECL the case described in *Figure 5-10a* is the only one calculated, since all other combinations are approximately the same. For other combinations of rise time, impedance, fan out or line characteristics (δ and C_0), maximum lengths are calculated using *Equation 5-14.* For the convenience of those who are also using F10K ECL, maximum recommended lengths of unterminated lines are listed in *Figures 5-10b* to *5-10e.*

Fig. 5-10 Maximum Worst-case Line Lengths for Unterminated Lines

a. F100K Maximum Worst-case Line Lengths for Unterminated Microstrip, Distributed Loading

	Number of Fan-out Loads		
Z_0	1	2	4
50	1.37*	1.13	0.95
62	1.33	1.07	0.87
75	1.25	0.95	0.75
90	1.18	0.85	0.52
100	1.15	0.82	0.49

*Length in inches
Unit load = 2 pF, δ = 0.148 ns/inch

5

Fig. 5-10b F10K Maximum Worst-case Line Lengths for Unterminated Microstrip, Distributed Loading

	Number of Fan-out Loads				
Z_0	2	3	4	6	8
50	4.15*	3.75	3.45	2.85	2.45
62	3.95	3.50	3.15	2.55	2.10
75	3.75	3.25	2.85	2.25	1.85
90	3.55	3.00	2.60	2.00	1.60
100	3.45	2.85	2.45	1.85	1.45

*length in inches.
Unit load = 3 pF; δ = 0.148 ns/in.,

Fig. 5-10c F10K Maximum Worst-case Line Lengths for Unterminated Microstrip, Concentrated Loading

	Number of Fan-out Loads				
Z_0	1	2	4	6	8
50	4.40*	3.65	2.60	1.90	1.40
62	4.30	3.45	2.30	1.60	1.15
75	4.20	3.20	2.05	1.40	0.95
90	4.05	2.95	1.75	1.05	0.65
100	3.90	2.80	1.60	0.90	0.50

*length in inches.
Unit load = 3 pF; δ = 0.148 ns/in.,

Fig. 5-10d F10K Maximum Worst-case Line Lengths for Unterminated Stripline, Distributed Loading

	Number of Fan-out Loads				
Z_0	2	3	4	6	8
50	3.30*	3.00	2.70	2.25	2.90
62	3.15	2.80	2.50	2.00	1.65
75	3.00	2.60	2.25	1.80	1.45
90	2.80	2.40	2.05	1.55	1.25

*length in inches.
Unit load = 3 pF; δ = 0.188 ns/in.,

Fig. 5-10e F10K Maximum Worst-case Line Lengths for Unterminated Stripline, Concentrated Loading

	Number of Fan-out Loads				
Z_0	1	2	4	6	8
50	3.45*	2.85	2.00	1.50	1.10
62	3.40	2.70	1.80	1.30	0.90
75	3.30	2.55	1.60	1.10	0.75
90	3.15	2.35	1.40	0.85	0.50
100	3.10	2.20	1.25	0.70	0.40

*length in inches.
Unit load = 3 pF; δ = 0.188 ns/in.,

A load capacitance concentrated at the end of the line restricts line length more than a distributed load does. Maximum recommended lengths for fiberglass epoxy dielectric and a 0.5 ns rise time are listed in *Figure 5-10* for microstrip. For line impedances not listed, linear interpolation can be used to determine appropriate line lengths. Appropriate line lengths for dielectric materials with a different propagation constant δ can be determined by multiplying the listed values by the fiberglass epoxy δ and then dividing by the δ of the other material. For example, a line length for a material which has a microstrip δ of 0.1 ns/inch is determined by multiplying the length given in the microstrip table (for a desired impedance and load) by 0.148 and dividing by 0.1.

Resistor R_E must provide the current for the negative-going signal at the driver output. Line input and output waveforms are noticeably affected if R_E is too large, as shown in *Figure 5-9b*. The negative-going edge of the signal falls in stair-step fashion, with three distinct steps visible at point A. The waveform at point B shows a step in the middle of the negative-going swing. The effect of different R_E values on the net propagation time through the line and the driven loads is evident in *Figure 5-9c* which shows the output signal of one driven gate in a multiple exposure photograph. The horizontal sweep (time axis) was held constant with respect to the input signal of the driver. The earliest of the three output signals occurs with an R_E value of 330 Ω. Changing R_E to 510 Ω increases the net propagation delay by 0.3 ns, the horizontal offset between the first and second signals. Changing R_E to 1 kΩ produces a much greater increase in net propagation delay, indicating that the negative-going signal at B contains several steps. In practice, a satisfactory negative-going signal results when the R_E value is chosen to give an initial

negative-going step of 0.6 V at the driving end of the line. This gives an upper limit on the value of R_E, as shown in *Equation 5-15*.

$$\text{initial step} = \Delta I \bullet Z_0 = \frac{(V_{OH} - V_{EE})\, Z_0}{R_E + Z_0} \geq 0.6$$

$$R_E = \leq 6.25\, Z_0 \qquad \textbf{(5-15)}$$

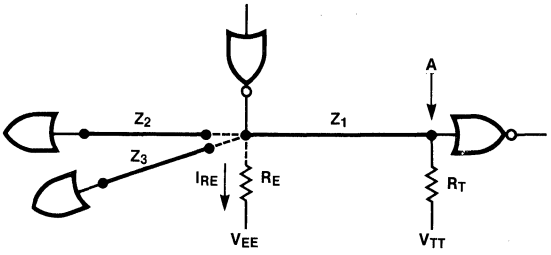
An ECL output can drive two or more unterminated lines, provided each line length and loading combination is within the recommended constraints. The appropriate R_E value is determined from *Equation 5-15,* using the parallel impedance of the two or more lines for Z_0.

An ECL output can simultaneously drive terminated and unterminated lines, although the negative-going edge of the signal shows two or more distinct steps when the stubs are long unless some extra pull-down current is provided. *Figure 5-11a* shows an ECL circuit driving a parallel terminated line, with provision for connecting two worst-case unterminated lines to the driver output. Waveforms at the termination resistor (point A) are shown in the multiple exposure photograph of *Figure 5-11b.* The upper trace shows a normal signal without stubs connected to the driver. The middle trace shows the effect of connecting one stub to the driver. The step in the negative-going edge indicates that the quiescent I_{OH} current through R_T is not sufficient to cause a full signal for both lines. The relationship between the quiescent I_{OH} current (through R_T) and the negative-going signal swing was discussed earlier in connection with parallel termination.

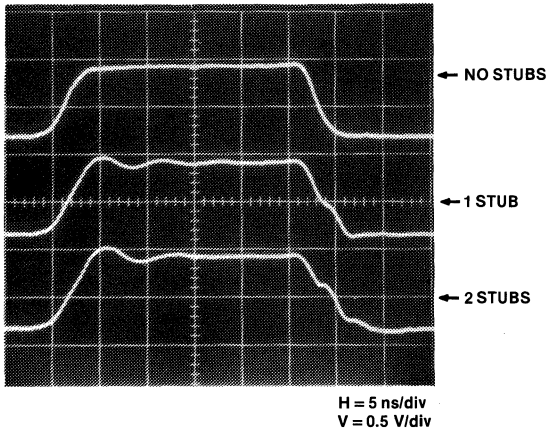
The bottom trace in *Figure 5-11* shows the effect of connecting two stubs to the driver output. The steps in the trailing edge are smaller and more pronounced. The deteriorated trailing edge of either the middle or lower waveform increases the switching time of the circuit connected to point A. If this extra delay cannot be tolerated, additional pull-down current must be provided. One method uses a resistor to V_{EE} as suggested in *Figure 5-11a.* The initial negative-going step at point A should be about 0.7 V to insure a good fall rate through the threshold region of the driven gate. The initial step at the driver output should also be 0.7 V. If the driver output is treated as a switch that opens to initiate the negative-going signal, the equivalent circuit of *Figure 5-11c* can

Fig. 5-11 Driving Terminated and Unterminated Lines in Parallel

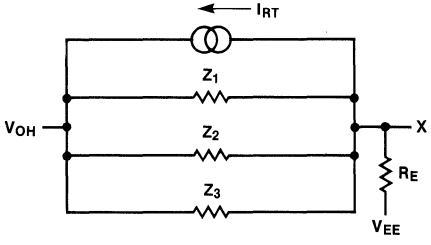
a. Multiple Lines



b. Waveforms at Termination Point A



c. Equivalent Circuit for Determining Initial Negative Voltage Step at the Driver Output



be used to determine the initial voltage step at the driver output (point X). The value of the current source I_{RT} is the quiescent I_{OH} current through R_T. Using Z′ to denote the parallel impedance of the transmission lines and ΔV for the desired voltage step at X, the appropriate value of R_E can be determined from the following equation, using absolute values to avoid polarity confusion.

$$R_E = (|V_{EE}| - |V_{OH}| - |\Delta V|) \bullet \left(\frac{Z'}{|\Delta V| - |I_{RT}|\, Z'} \right) \quad \textbf{(5-16)}$$

For a sample calculation, assume that R_T and the line impedances are each 100 Ω, V_{OH} is −0.955 V, ΔV is 0.750 V, V_{EE} is −4.5 V and V_{TT} is −2 V. I_{RT} is thus 10.45 mA and the calculated value of R_E is 232 Ω. In practice, this value is on the conservative side and can be increased to the next larger (10%) standard value with no appreciable sacrifice in propagation through the gate at point A.

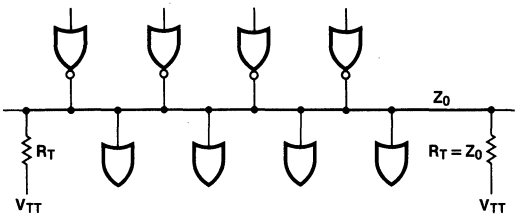
Again, the foregoing example is based on worst-case stub lengths (the longest permissible). With shorter stubs, the effects are less pronounced and a point is reached where extra pull-down current is not required because the reflection from the end of the stub arrives back at the driver while the original signal is still falling. Since the reflection is also negative going, it combines with and reinforces the falling signal at the driver, eliminating the steps. The net result is a smoothly falling signal but with increased fall time compared to the stubless condition.

The many combinations of line impedance and load make it practically impossible to define just what stub length begins to cause noticeable steps in the falling signal. A rough rule-of-thumb would be to limit the stub length to one-third of the values given in *Figure 5-10.*

Data Busing

Data busing involves connecting two or more outputs and one or more inputs to the same signal line, *(Figure 5-12).* Any one of the several drivers can be enabled and can apply data to the line. Load inputs connected to the line thus receive data from the selected source. This method of steering data from place to place simplifies wiring and tends to minimize package count. Only one of the drivers can be enabled at a given time;

Fig. 5-12 Data Bus or Party Line



all other driver outputs must be in the LOW state. Termination resistors matching the line impedance are connected to both ends of the line to prevent reflections. For calculating the modified delay of the line *(Chapter 4)* the capacitance of a LOW (unselected) driver output should be taken as 2 pF.

An output driving the line sees an impedance equal to half the line impedance. Similarly, the quiescent I_{OH} current is higher than with a single termination. For line impedance less than 100 Ω, the I_{OH} current is greater than the data sheet test value, with a consequent reduction of HIGH-state noise margin. This loss can be eliminated if necessary by using multiple output gates (F100112) and paralleling two outputs for each driver. In the quiescent LOW state, termination current is shared among all the output transistors on the line. This sharing makes V_{OL} more positive than if only one output were conducting all of the current. For example, a 100 Ω line terminated at both ends represents a net 50 Ω dc load, which is the same as the data sheet condition for V_{OL}. If one worst-case output were conducting all the current, the V_{OL} would be −1.705 V. If another output with identical dc characteristics shares the load current equally, the V_{OL} level shifts upward by about 25 mV. Connecting two additional outputs for a total of four with the same characteristics shifts V_{OL} upward another 22 mV. Connecting four more identical outputs shifts V_{OL} upward another 20 mV. Thus the V_{OL} shift for eight outputs having identical worst-case V_{OL} characteristics is approximately 67 mV. In practice, the probability of having eight circuits with worst-case V_{OL} characteristics is quite low. The output with the highest V_{OL} tends to conduct most of the current. This limits the upward shift to much less than the theoretical worst-case value. In addition, the LOW-state noise margin is specified greater than the HIGH-state margin to allow for V_{OL} shift when outputs are paralleled.

In some instances a single termination is satisfactory for a data bus, provided certain conditions are fulfilled. The single termination is connected in the middle of the line. This requires that for each half of the line, from the termination to the end, the line length and loading must comply with the same restrictions as unterminated lines to limit overshoot and undershoot to acceptable levels. The termination should be connected as near as possible to the electrical mid-point of the line, in terms of the modified line delay from the termination to either end. Another restriction is that the time between successive transitions, *i.e.*, the nominal bit time, should not be less than 15 ns. This allows time for the major reflections to damp out and limits additive reflections to a minor level.

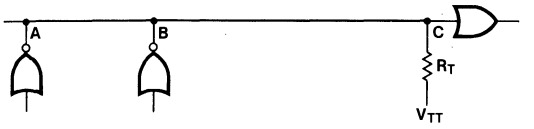
Wired-OR

In general-purpose wired-OR logic connections, where two or more driver outputs are expected to be in the HIGH state simultaneously, it is important to minimize the line length between the participating driver outputs, and to place the termination as close as possible to the mid-point between the two most widely separated sources. This minimizes the negative-going disturbances which occur when one HIGH output turns off while other outputs remain HIGH. The driver output going off represents a sudden decrease in line current, which in turn generates a negative-going voltage on the line. A finite time is required for the other driver outputs (quiescently HIGH) to supply the extra current. The net result is a "V" shaped negative glitch whose amplitude and duration depend on three factors: current that the off-going output was conducting, the line impedance, and the line length between outputs. If the separation between outputs is kept within about one inch, the transient will not propagate through the driven load circuits.

If a wired-OR connection cannot be short, it may be necessary to design the logic so that the signal on the line is not sampled for some time after the normal propagation delay (output going negative) of the element being switched. Normal propagation delay is defined as the case where the element being switched is the only one on the line in the HIGH state, resulting in the line going LOW when the element switches. In this case, the propagation delay is measured from the 50% point on the input signal of the off-going element to the 50% point of the signal at the input farthest away from the output being switched. The extra waiting time required in the case of a severe negative glitch is, in a worst-case physical arrangement, twice the line delay between the off-going output and the nearest quiescently HIGH output, plus 2 ns.

An idea of how the extra waiting time varies with physical arrangement can be obtained by qualitatively comparing the signal paths in *Figure 5-13*. With the outputs at A and B quiescently HIGH, the duration of the transient observed at C is longer if B is the off-going output than if A is the off-going element. This is because the negative-going voltage generated at B must travel to A, whereupon the corrective signal is generated, which subsequently propagates back toward C. Thus the corrective signal lags behind the initial transient, as observed at C, by twice the line delay between A and B. On the other hand, if the output at A generates the negative-going transient, the corrective response starts when the transient reaches point B. Consequently, the transient duration observed at C is shorter by twice the line delay from A to B.

Fig. 5-13 Relative to Wired-OR Propagation



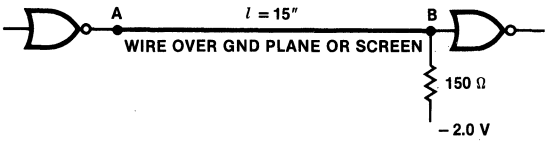
Backplane Interconnections

Several types of interconnections can be used to transmit a signal between logic boards. The factors to be considered when selecting a particular interconnection for a given application are cost, impedance discontinuities, predictability of propagation delay, noise environment, and bandwidth. Single-ended transmission over an ordinary wire is the most economical but has the least predictable impedance and propagation delay. At the opposite end of the scale, coaxial cable is the most costly but has the best electrical characteristics. Twisted pair and similar parallel wire interconnection cost and quality fall in between.

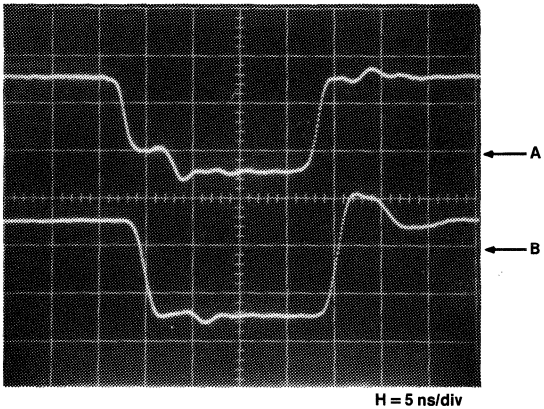
For single-wire transmission through the backplane, a ground plane or ground screen *(Chapter 6)* should be provided to establish a controlled impedance. A wire over a ground plane or screen has a typical impedance of 150 Ω with variations on the order of ±33%, depending primarily on the distance from ground and the configuration of the ground. *Figure 5-14* illustrates the

Fig. 5-14 Parallel Terminated Backplane Wire

a. Wire over Ground Plane or Screen

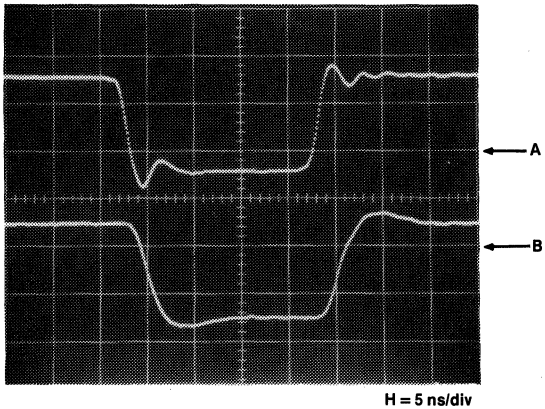


b. Wire in Contact with Ground Plane



H = 5 ns/div
V = 0.4 ns/div

c. Wire Spaced 1/8" from Ground Screen



H = 5 ns/div
V = 0.4 V/div

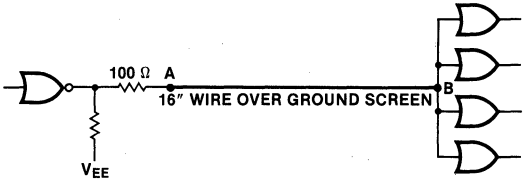
effects of impedance variations with a 15-inch wire parallel terminated with 150 Ω to –2 V. *Figure 5-14b* shows source and receiver waveforms when the wire is in contact with a continuous ground plane. The negative-going signal at the source shows an initial step of only 80% of a full signal swing. This occurs because the quiescent HIGH-state current I_{OH} (about 7 mA) multiplied by the impedance of the wire (approximately 90 Ω) is less than the normal signal swing, and this condition allows the driver emitter follower to turn off. The negative-going signal at the receiving end is greater by 25% ($1 + \rho = 1.25$). The receiving end mismatch causes a negative-going reflection which returns to the source and establishes the V_{OL} level. The positive-going signal at the source shows a normal signal swing, with the receiving end exhibiting approximately 25% overshoot.

Figure 5-14c shows waveforms for a similar arrangement, but with the wire about 1/8 inch from a ground screen. The impedance of the wire is greater than the 150 Ω termination, but small variations in impedance along the wire cause intermediate reflections which tend to lengthen the rise and fall times of the signal. As a result, the received signal does not exhibit pronounced changes in slope as would be expected if a 200 Ω constant impedance line were terminated with 150 Ω.

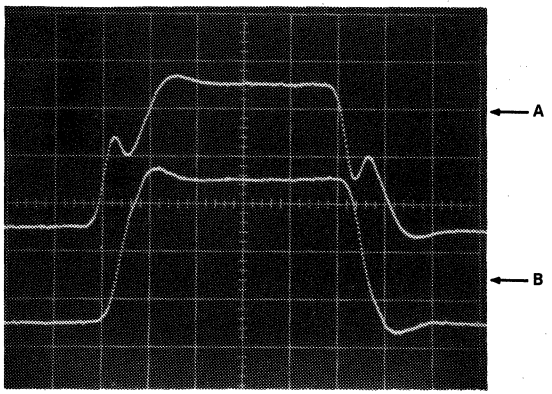
Series source resistance can also be used with single wire interconnections to absorb reflection. *Figure 5-15a* shows a 16-inch wire with a ground screen driven through a source resistance of 100 Ω. The waveforms (*Figure 5-15b*) show that although reflections are generated, they are largely absorbed by the series resistor, and the signal received at the load exhibits only slight changes and overshoot. Series termination techniques can also be used when the signal into the wire comes from the PC board transmission line. *Figure 5-16a* illustrates a 12-inch wire over a ground screen, with 12-inch microstrip lines at either end of the wire. The output is heavily loaded (fan out of 8) and the combination of impedances produces a variety of reflections at the input to the first microstrip line, shown in the upper trace of *Figure 5-16b.* The lower trace shows the final output; a comparison between the two traces shows the effectiveness of damping in maintaining an acceptable signal at the output. *Figure 5-16c* shows the signals at

Fig. 5-15. Series Terminated Backplane Wire

a. Wire over Ground Screen



b. Series Terminated Waveform



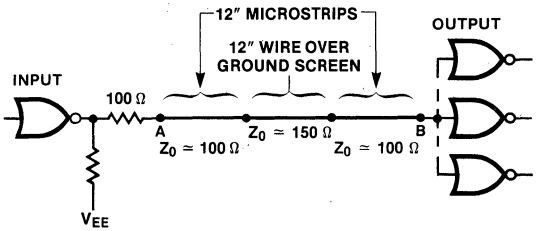
H = 10 ns/div
V = 0.3 V/div

the input to the driving gate and at the output of the load gate, with a net through-put time of 8.5 ns. The circuit in *Figure 5-16a* is a case of mismatched transmission lines, discussed in *Chapter 4*.

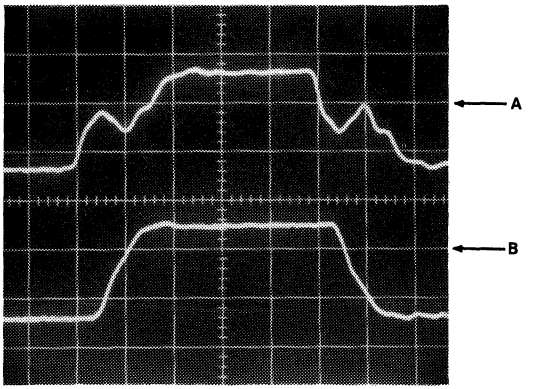
Signal propagation along a single wire tends to be fast because the dielectric medium is mostly air. However, impedance variations along a wire cause intermediate reflections which tend to increase rise and fall times, effectively increasing propagation delay. Effective propagation delays are in the range of 1.5 to 2.0 ns per foot of wire. Load capacitance at the receiving end also increases rise and fall time *(Chapter 4)*, further increasing the effective propagation delay.

Fig. 5-16 Signal Path with Sequence of Microstrip, Wire, Microstrip

a. Backplane Wire Interconnecting PC Board Lines

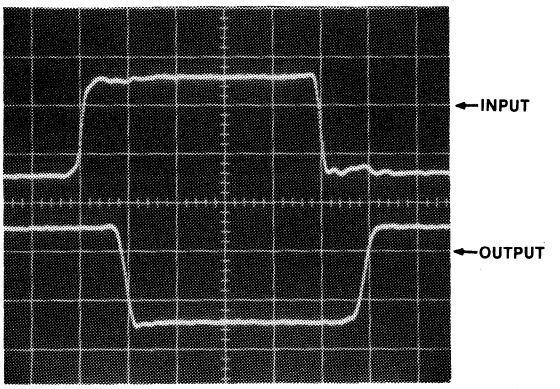


b. Signals into the First Microstrip and at the Loads



H = 10 ns/div
V = 0.4 V/div

c. Input to Driving Gate and Output of Load Gate

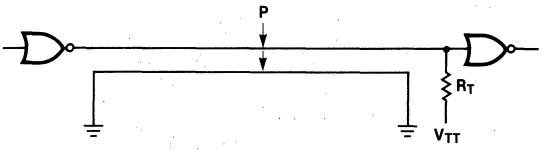


H = 10 ns/div
V = 0.4 V/div

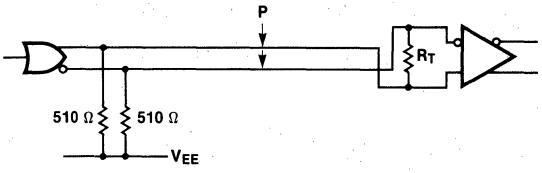
Better control of line impedance and faster propagation can be achieved with a twisted pair. A twisted pair of AWG 26 Teflon* insulated wires, two twists per inch, exhibits a propagation delay of 1.33 ns/ft and an impedance of 115 Ω. Twisted pair lines are available in a variety of sizes, impedances and multiple-pair cables. *Figure 5-17a* illustrates single-ended driving and receiving. In addition to improved propagation velocity, the magnetic fields of the two conductors tend to cancel, minimizing noise coupled into adjacent wiring.

Fig. 5-17 Twisted Pair Connections

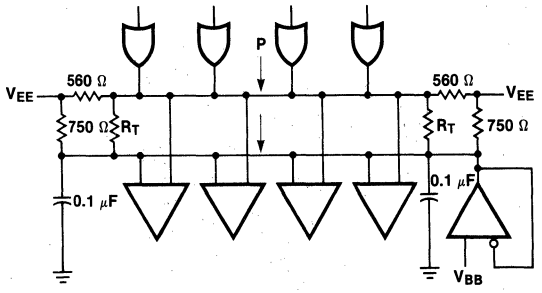
a. Single-ended Twisted Pair



b. Differential Transmission Reception



c. Backplane Data Bus



Differential line driving and receiving with complementary gates as the driver and an F100114 line receiver is illustrated in *Figure 5-17b.* Differential operation provides high noise immunity, since common mode input voltages between −0.55 V and −3.0 V are rejected. The differential mode is recommended for communication between different parts of a system, because it effectively nullifies ground voltage differences. For long runs between cabinets or near high power transients, interconnections using shielded twisted pair are recommended.

Twisted pair lines can be used to implement party line type data transfer in the backplane, as indicated in *Figure 5-17c.* Only one driver should be enabled at a given time; the other outputs must be in the V_{OL} state. The V_{BB} reference voltage is available on pin 22 of the flatpak and pin 19 of the dual-in-line package for the F100114.

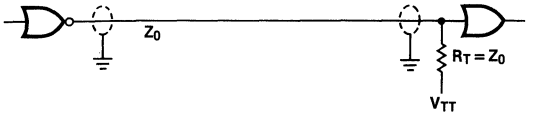
In the differential mode, a twisted pair can send high-frequency symmetrical signals, such as clock pulses, of 100 MHz over distances of 50 to 100 feet. For random data, however, bit rate capability is reduced by a factor of four or five due to line rise effects on time jitter.[3]

Coaxial cable offers the highest frequency capability. In addition, the outer conductor acts as a shield against noise, while the uniformity of characteristics simplifies the task of matching time delays between different parts of the system. In the single-ended mode, *Figure 5-18a,* 50 MHz signals can be transferred over distances of 100 feet. For 100 MHz operation, lengths should be 50 feet or less. In the differential mode, *Figures 5-18b, c,* the line receiver can recover smaller signals, allowing 100 MHz signals to be transferred up to 100 feet. The dual cable arrangement of *Figure 5-18c* provides maximum noise immunity. The delay of coaxial cables depends on the type of dielectric material, with typical delays of 1.52 ns/ft for polyethylene and 1.36 ns/ft for cellular polyethylene.

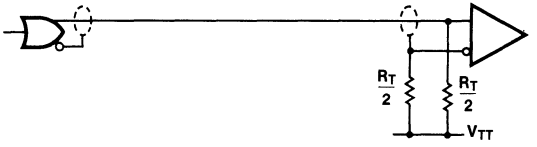
*Teflon is a registered trademark of E.I. du Pont de Nemours Company

Fig. 5-18 Coaxial Cable Connections

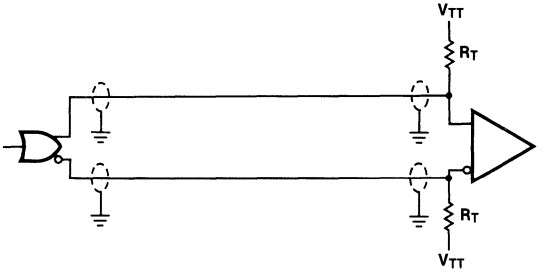
a. Single-ended Coaxial Transmission



b. Differential Coaxial Transmission



c. Differential Transmission with Grounded Shields



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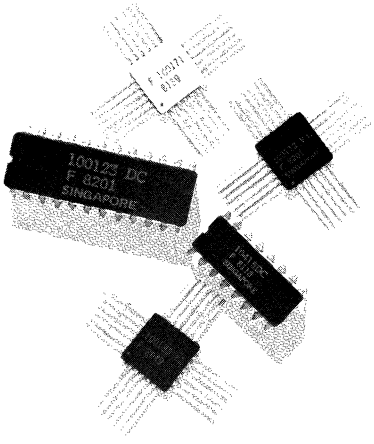
1. Kaupp, H. R., "Characteristics of Microstrip Transmission Lines," *IEEE Transaction on Electronic Computers,* Vol. EC-16 (April, 1967).

2. Harper, C. A., *Handbook of Wiring, Cabling and Interconnections for Electronics.* New York: McGraw-Hill, 1972.

3. True, K. M., "Transmission Line Interface Elements," *The TTL Applications Handbook, Chapter 14* (August, 1973), pp. 14-1 - 14-14.



Chapter 6
Power Distribution and Thermal Considerations

- Introduction
- Logic Circuit Ground, V_{CC}
- Conductor Resistances
- Temperature Coefficient
- Distribution Impedance
- Ground on PC Cards
- Backplane Construction
- Termination Supply, V_{TT}
- V_{EE} Supply
- Thermal Considerations
- Reference

6

Introduction

High-speed circuits generally consume more power than similar low-speed circuits. At the system level, this means that the power supply distribution system must handle the larger current flow; the larger power dissipation places a greater demand on the cooling system. The direct current (dc) voltage drop along ground busses affects noise margins for all types of ECL circuits. Voltage drops along V_{EE} busses have only a slight effect on F100K circuits, but they require consideration to obtain the performance available from the family.

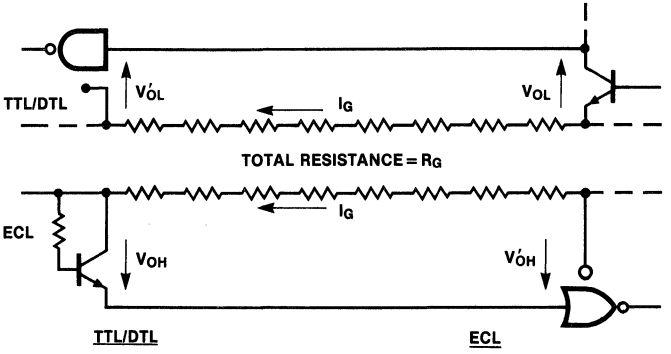
Logic Circuit Ground, V_{CC}

The positive potential V_{CC} and V_{CCA} in ECL circuits is the reference voltage for output voltages and input thresholds and should therefore be the ground potential. When two circuits are connected in a single-ended mode, any difference in ground potentials decreases the noise margins, as discussed in *Chapter 2.* This effect for TTL/DTL circuits, as well as for ECL circuits, is illustrated in *Figure 6-1.* The following analysis assumes some average value of current flowing through the distributed resistance along the ground path between two circuits. For the indicated direction of I_G, the shift in ground potential *decreases* the LOW-state noise margin of the TTL/DTL circuits and the HIGH-state noise margin of the ECL circuits. If I_G is flowing in the opposite direction, it *increases* these noise margins, but *decreases* the noise margins when the drivers are in the opposite state. For tabulation of ground currents in ECL, the designs must include termination currents as well as I_{EE} operating currents. ECL logic boards which use microstrip or stripline techniques generally have large areas of ground metal. This causes the ground resistance to be quite low and thus minimizes noise margin loss between pairs of circuits on the same board.

In practice, two communicating circuits might be located on widely separated PC cards with other PC cards in between. The net resistance then includes the incremental resistance of the ground distribution bus from card to card, while the ground current is successively increased by the contribution from each card. *Figure 6-2* illustrates a distribution bus for a row of cards with incremental resistances along the bus.

6

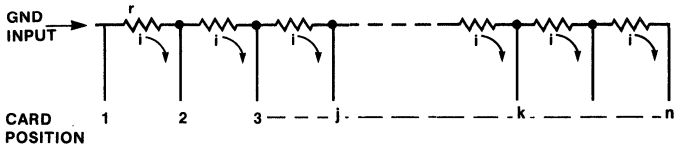
Fig. 6-1 Effect of Ground Resistance on Noise Margins



$V'_{OL} = V_{OL} + I_G R_G$ $\quad$ $V'_{OH} = V_{OH} + I_G R_G$

$I_G R_G = (V'_{OL} - V_{OL})$ = Noise Margin Decrease = $I_G R_G = (V'_{OH} - V_{OH})$

Fig. 6-2 Ground Shift Along a Row of PC Cards



r = Incremental Bus Resistance Between Positions
i = Average Ground Current per Card

The ground shift can be estimated by first determining an average value of current per card based on the number of packages, the mix of SSI and MSI, and the number and types of terminations. With n cards in the row, an average ground current (i) per card, and an incremental bus resistance (r) between card positions, the bus voltage drops between the various positions can be determined as follows:

between positions 1 and 2: $v_{1\text{-}2} = (n - 1)\ ir$

between positions 1 and 3: $v_{1\text{-}3} = (n - 1)\ ir + (n - 2)\ ir$

between positions 1 and 4: $v_{1\text{-}4} = (n - 1)\ ir + (n - 2)\ ir + (n - 3)\ ir$

between 1 and n:

$$v_{1\text{-}n} = ir\ \{(n - 1) + (n - 2) + (n - 3) + \ldots + [n - (n - 1)]\}$$

$$= ir\ [1 + 2 + 3 + \ldots + (n - 1)]$$

$$v_{1\text{-}n} = ir \sum_{1}^{n-1} n$$

For a row of 15 cards, for example, the total ground shift between positions 1 and 15 is expressed as in *Equation 6-1*.

$$v_{1\text{-}15} = ir \sum_{1}^{14} n = ir\ (1 + 2 + 3 + \ldots + 13 + 14) \qquad \textbf{(6-1)}$$

$$= 105\ ir$$

The ground shift between any two card positions j and k can be determined as follows for the general case.

$$v_{j\text{-}k} = (n - j)\ ir + [n - (j + 1)]\ ir + [n - (j + 2)]\ ir + \ldots + \{n - [j + (k\text{-}j\text{-}1)]\}\ ir$$

$$= (k - j)\ nir - ir\ \{j + (j + 1) + (j + 2) + \ldots + [j + (k\text{-}j\text{-}1)]\} \qquad \textbf{(6-2)}$$

$$v_{j\text{-}k} = (k - j)\ nir - ir \sum_{j}^{k-1} n = ir\ [(k - j)\ n - \sum_{j}^{k-1} n]$$

In a row of 15 cards, the ground shift between positions four and nine, for example, is determined as follows.

$$v_{j\text{-}k} = ir\ [(9 - 4)\ 15 - (4 + 5 + 6 + 7 + 8)] = ir\ (75 - 30) = 45\ ir \qquad \textbf{(6-3)}$$

The ground shift between the same number of positions further down the row is less because of the decreasing current along the row. Consider the ground shift between card positions 10 and 15.

$$v_{10\text{-}15} = ir\ [(15 - 10)15 - (10 + 11 + 12 + 13 + 14)] = ir\ (75 - 60) = 15\ ir \qquad \textbf{(6-4)}$$

These examples illustrate several principles the designer should consider regarding the ground distribution bus and assignment of card positions. The bus resistance should be kept as low as possible by making the cross-sectional areas as large as practical. Logic cards which represent the heaviest current drain should be located nearest the end where ground comes into the row of cards. Cards with single-ended logic wiring between them should be assigned to positions as close together as possible. Conversely, if the ground shift between two card positions represents an unacceptable loss of noise margin, then the differential transmission and reception method *i.e.,* twisted pair, should be used for logic wiring between them, thereby eliminating ground shift as a noise margin factor.

Conductor Resistances

Conductors with large cross-sectional areas are required to maintain low voltage drops along power busses. For convenience, *Figure 6-3* lists the resistance per foot and the cross-sectional area for more common sizes of annealed copper wire. Other characteristics and a complete list of sizes can be found in standard wire tables. A useful rule-of-thumb regarding resistances and, hence, areas is: as gauge numbers increase, resistance doubles with every third gauge number; *e.g.,* the resistance per foot of #10 wire is 1 mΩ, for #13 wire it is 2 mΩ. Similarly, the resistance per foot of #0 wire is 0.078 mΩ, which is half that of #2 wire.

For calculations involving conductors having rectangular cross sections, it is often convenient to work with sheet resistance, particularly for power distribution on PC

Fig. 6-3 Resistance and Cross-sectional Area of Several Sizes of Annealed Copper Wire

AWG B & S Gauge	Resistance mΩ per foot	Cross-sectional Area square inches
#2	0.156	5.213×10^{-2}
#6	0.395	2.062×10^{-2}
#10	0.999	8.155×10^{-3}
#12	1.588	5.129×10^{-3}
#18	6.385	1.276×10^{-3}
#22	16.14	5.046×10^{-4}
#26	40.81	1.996×10^{-4}
#30	103.2	7.894×10^{-5}

cards. Copper resistivity is usually given in ohm-centimeters, indicating the resistance between opposing faces of a 1 cm cube. The sheet resistance of a conductor is obtained by dividing the resistivity by the conductor thickness. These relationships follow.

$$\text{Copper resistivity} = \rho = 1.724 \times 10^{-6}\ \Omega\text{-cm @ } 20°C$$

$$\text{Resistance of a conductor} = \rho \frac{l}{A} = \rho \frac{l}{tw}$$

where: l = length t = thickness w = width

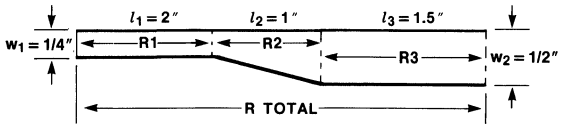
$$\text{Sheet resistance } \rho_S = \frac{\rho}{t}\ \Omega \text{ per } \frac{l}{w}$$

The length/width ratio (l/w) is dimensionless; therefore, the resistance of a length of conductor of uniform thickness can be calculated by first determining the number of "squares," then multiplying by the sheet resistance. For example, a conductor one-eighth inch wide and three inches long has 24 squares; its resistance is 24 times the sheet resistance. Since many thickness dimensions are given in inches, it is convenient to express the resistivity in ohm-inch, as follows.

$$\rho(\Omega\text{-in.}) = \rho(\Omega\text{-cm}) \div 2.54 = 6.788 \times 10^{-7}\ \Omega\text{-in.}$$

The use of sheet resistance and the "squares" concept is illustrated by calculating the resistance of the conductor shown in *Figure 6-4*. Assume the conductor is a 1 oz. copper cladding with a 0.0012 inch minimum thickness on a PC card.

Fig. 6-4 Conductor of Uniform Thickness but Non-uniform Cross Section



$$\text{Sheet resistance} = \rho_S = \frac{\rho}{t}$$

$$= 5.657 \times 10^{-4}\ \Omega \text{ per square}$$

The number of squares S for the rectangular sections are as follows.

$$S_1 = \frac{l_1}{w_1} = 8 \qquad S_3 = \frac{l_3}{w_2} = 3$$

The middle average segment of the conductor has a trapezoidal shape. The average of w_1 and w_2 can be used as the effective width, within 1% accuracy, if the w_2/w_1 ratio is 1.5 or less. Otherwise, a more exact result is obtained as follows.

$$S_2 = \frac{l_2}{w_2 - w_1} \ln\left(\frac{w_2}{w_1}\right) = 4 \ln 2 = 2.77 \text{ squares}$$

$$\text{Total } R = R_1 + R_2 + R_3 = \rho_S(S_1 + S_2 + S_3) = 7.51\ m\Omega \qquad \textbf{(6-5)}$$

As another example, assume that a 1 oz. trace must carry a 200 mA current six inches with a voltage drop less than 10 mV.

$$R_{max} = \frac{V_{max}}{1} = \frac{0.01}{0.2} = 0.05\ \Omega$$

$$0.05 = \rho_S \frac{l}{w}$$

$$\frac{w}{l} = 20\ \rho_S \qquad \textbf{(6-6)}$$

$$w = 120\ \rho_S = (120)\ 5.657 \times 10^{-4} = 67.9 \times 10^{-3}$$

$\therefore$ minimum trace width, w = 68 mils

6

At a higher current level, consider the voltage drop in a conductor 20 mils thick, 1.25 inches wide and 3 feet long carrying a 50 A current.

$$\rho_S = \frac{6.788 \times 10^{-7}}{2 \times 10^{-2}} = 3.364 \times 10^{-5}\ \Omega \text{ per square}$$

$$V = IR - (50)\ (3.364 \times 10^{-5})\ \frac{36}{1.25} \qquad \textbf{(6-7)}$$
$$= 0.0484 = 48.4\ mV$$

Sheet resistances for various copper thicknesses are listed in *Figure 6-5.* Standard thicknesses and tolerances for copper cladding are tabulated in *Figure 6-6* and resistance per foot as a function of width is shown in *Figure 6-7.*

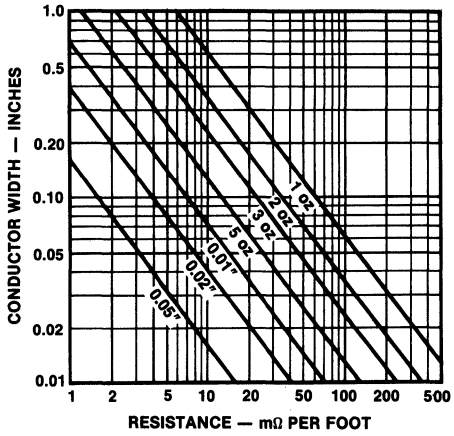
Fig. 6-5 Sheet Resistance for Various Thicknesses of Copper

Weight or Thickness	Sheet Resistance Ω per square	Thickness	Sheet Resistance Ω per square
2 oz.	2.715×10^{-4}	0.02 in.	3.364×10^{-5}
3 oz.	1.886×10^{-4}	0.05 in.	1.358×10^{-5}
5 oz.	1.077×10^{-4}	1/16 in.	1.086×10^{-5}
0.01 in.	6.788×10^{-5}	1/4 in.	2.715×10^{-6}

Fig. 6-6 Thicknesses and Tolerances for Copper Cladding

Nominal Thickness		Nominal Weight	Tolerances By	
in.	mm	oz/ft²	weight, %	in.
0.0007	0.0178	1/2	+10	+0.0002
0.0014	0.0355	1	+10	+0.0004 −0.0002
0.0028	0.0715	2	+10	+0.0007 −0.0003
0.0042	0.1065	3	+10	+0.0006
0.0056	0.1432	4	+10	+0.0006
0.0070	0.1780	5	+10	+0.0007
0.0084	0.2130	6	+10	+0.0008
0.0098	0.2460	7	+10	+0.001
0.014	0.3530	10	+10	+0.0014
0.0196	0.4920	14	+10	+0.002

Fig. 6-7 Conductor Resistance Versus Thickness and Width



Temperature Coefficient

The resistances in *Figures 6-3, 6-5,* and *6-7,* as well as those used in the sample calculations, are 20°C values. Since copper resistivity has a temperature coefficient of approximately 0.4%/°C, the resistance at a temperature (T) can be determined as follows.

$$R_T = R_{20°}\ [1 + 0.004\ (T + 20°)]$$

At 55°C: **(6-8)**

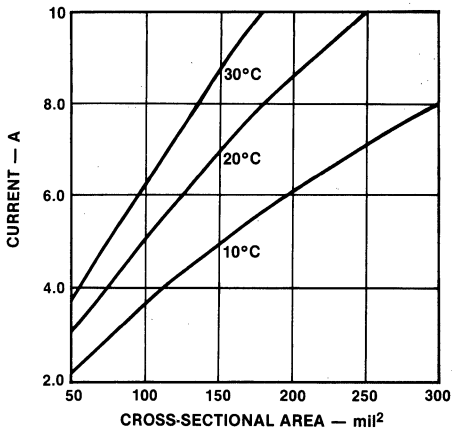
$$R = R_{20°}\ [1 + 0.004\ (55° - 20°)] = 1.14\ R_{20°}$$

When specifying power bus dimensions for PC cards containing many IC packages, designers should bear in mind that excessive current densities can cause the copper temperature to rise appreciably. *Figure 6-8* illustrates the ohmic heating effect of various current densities.[1]

Distribution Impedance

Power busses should have low ac impedance, as well as low dc resistance, to prevent propagation of extraneous disturbances along the distribution system. As far as current or voltage changes are concerned, power and ground busses appear as transmission lines; thus their impedances can be affected by shape, spacing and dielectric. The effect of geometry on impedance is illustrated in the two arrangements of *Figure 6-9.* The same cross-sectional area of copper is used, but the

Fig. 6-8 Temperature Rise with Current Density in PC Board Traces

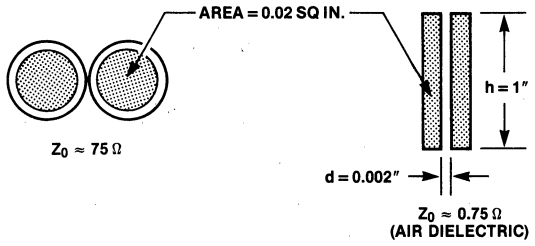


two round wires have an impedance of about 75 Ω while the flat conductors have an impedance determined as follows.

$$Z_0 = \frac{377\ d}{\sqrt{\epsilon}\ h} \quad for \quad \frac{d}{h} < 0.1$$

With a Mylar* or Teflon* dielectric ($\epsilon = 2.3$) two mils thick, impedance of the flat conductor pair is only 0.5 Ω. Power line impedance can be reduced by periodically connecting RF-type capacitors across the line.

Fig. 6-9 Effect of Geometry on Power Bus Impedance



*Mylar and Teflon are registered trademarks of E.I. du Ponte de Nemours Company.

Ground on PC Cards

It is essential to assign one layer of copper cladding almost exclusively to ground. This provides low-impedance, non-interfering return paths for the current changes which travel along signal traces when the IC outputs change state. These currents flow from the V_{CCA} pins of the IC packages, through the output transistors, then into the loads and the stray capacitances. These stray capacitances exist from an output to V_{EE}, output to ground, and to other signal lines. Thus, displacement currents through stray capacitances flow in many paths, but must ultimately return through ground to the output transistor where they originated. To reduce the length and impedance of the return path, the ground metal should cover as large an area as possible and one decoupling capacitor should be provided for every one to two IC packages. Additional capacitors may be needed for multiple output devices. These capacitors should be ceramic, monolithic or other RF types in the 0.01 to 0.1 μF range.

The load current returning to an IC package through ground metal is predictable, both in magnitude and in the return path. Since the magnetic and capacitive coupling between a signal trace and the underlying ground provides the transmission line characteristic, it follows that the load current flowing through the signal trace is accompanied by a ground return current equal in magnitude but opposite in direction. For example, in a 50 Ω terminator I_{OL} is 5.9 mA, I_{OH} is 20.9 mA. Then signal change will cause about 15 mA current change and, as this current change propagates along the signal trace, a current of −15 mA advances along the ground directly underneath the signal trace. Therefore, if there is an interruption in the ground, the return current is forced to go around it. The 15 mA current change can be reduced by terminating the complementary output of the signal. Then a signal change will direct the current from true output to the complement output reducing the Δ currents in the ground plane. When it is necessary to interrupt the ground plane, the interruptions should be kept as short as possible; every effort should be made to locate them away from overlying signal lines. When the ground plane is interrupted for short signal lines between packages, these lines should be at right angles to signal lines on the other side to minimize coupling. V_{EE} and V_{TT} distribution lines can also act as the return

side of transmission lines, as long as decoupling capacitors to ground are placed in the immediate areas where the signal return current must continue through ground.

Several connections along the edge of a PC card should be assigned to ground to accommodate backplane signal ground. These should be spaced at one-half to one inch intervals to minimize the average path length for signal return currents and to simulate a distributed connection to the backplane signal ground.

Not enough emphasis can be placed on the requirement for a good ground. All input signals are referenced to internal V_{BB} and the V_{BB} is referenced to V_{CC} (ground). Any variation from one side of the board to the other affects the noise margins. To help eliminate some of the variations a separate V_{CCA} is provided on F100K ECL circuits to power the output drivers and leave the V_{CC} going to internal circuitry unaffected.

Backplane Construction

In order to take complete advantage of the speeds inherent in F100K ECL it is desirable to construct the backplane as a multilayer printed circuit board. Generally, two internal layers are devoted to ground and V_{EE} and the signals occupy the outside layers. Where power densities are very high, it may be necessary to supplement the power layers with external busses (see Backplane Interconnections, *Chapter 5*).

If it is necessary to use wires to augment the interconnection provided by the traces, less critical signals should use the wires. The wires will exhibit an impedance which can be calculated with the wire-over-ground formula

$$Z_0 = \frac{138}{\sqrt{\epsilon}} \, Log_{10} \, \frac{4h}{d} \qquad \textbf{(6-9)}$$

where d is diameter, h is distance to ground, and ϵ is dielectric constant.

Bear in mind that if the ground plane is buried inside the board, then both h and ϵ are made up of multiple components.

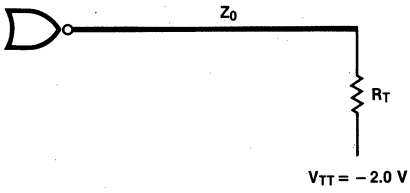
Termination Supply, V_{TT}

A separate return voltage for the termination resistors offers a way to minimize power dissipation in systems extensively using parallel termination techniques. A -2 V V_{TT} value represents an optimum speed/power trade-off, allowing sufficient termination current to discharge load capacitances while minimizing the average power consumption. *Figure 6-10* shows the average values of current, IC power dissipation and resistor power dissipation for various values of the termination resistor R_T returned to -2 V. Average values are determined by calculating the output HIGH and output LOW values, then taking the average. These 50% duty cycle values are useful in determining the current drain on the -2 V supply and the contribution to dissipation on the logic boards. Peak values of termination current are approximately 60% greater than the average values listed.

DC regulation of the -2 V supply is not critical; a variation of ± 5% causes a change in output levels of ± 12 mV for 50 Ω terminations or ± 7 mV for 100 Ω terminations.

The high frequency characteristics of the V_{TT} distribution are extremely important. Ideally, a solid voltage plane should be devoted to V_{TT}. If this is not feasible, the V_{TT} distribution should form a grid using orthogonal traces. In any case, decoupling capacitors to ground should be used to reduce the high frequency impedance.

Fig. 6-10 Average Current and Power Dissipation for Parallel Termination to −2 V



R_T Ω	I_{avg} mA	$P_{D\,(avg)}$ mW IC Output	$P_{D\,(avg)}$ mW Resistor
50	14	14	13
62	11	12	11
75	9.3	9.5	9.1
90	8.1	8.2	7.9
100	7.3	7.3	7.1
150	5.0	4.9	5.0

If the terminators used are in Single In-line Packages (SIP) or Dual In-line Packages (DIP) as opposed to discrete resistors, particular attention must be given to decoupling in order to maintain a solid V_{TT} voltage inside the package. This is necessary to avoid crosstalk due to mutual inductance to V_{TT}. SIPs have been developed which have multiple V_{TT} connections and on-board decoupling capacitors.

V_{EE} Supply

The value of V_{EE} is not critical for F100K since all circuits in the family operate over the range of -4.2 V to -5.7 V. Decoupling capacitors to ground should be used on each card, as previously discussed in connection with the ground on PC cards. In addition, each card should use 1 to 10 μF decoupling capacitors near the points where V_{EE} enters the card.

The current drain for the V_{EE} supply for each circuit type can be determined from the data sheet specifications. For V_{EE} values other than -4.5 V, the current drain varies as shown in *Figures 6-11* and *6-12* for SSI and MSI elements respectively. These graphs are made from data from the F100101 and F100179.

Fig. 6-11 Supply Current Versus Supply Voltage for F100101

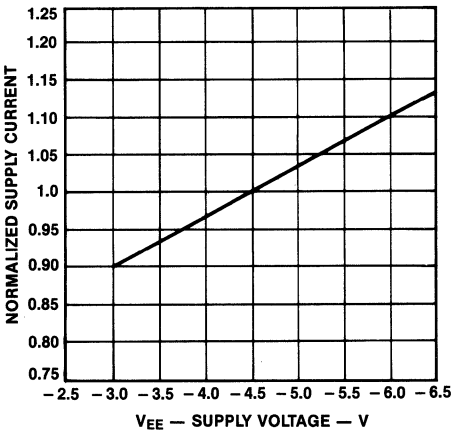
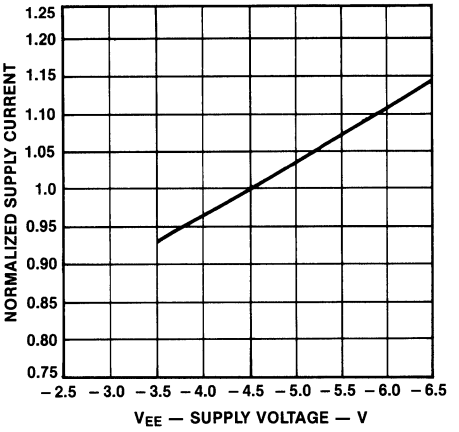


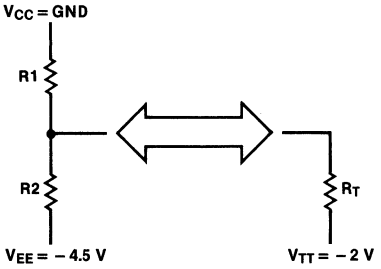
Fig. 6-12 Supply Current Versus Supply Voltage for F100179



Series dividers used to obtain Thevenin equivalent parallel terminations increase the current load on the V_{EE} supply, as do the pull-down resistors to V_{EE} used with series termination. Average V_{EE} current and resistor dissipation for Thevenin equivalent terminations are listed in *Figure 6-13* for several representative values of equivalent resistance. The average values apply for 50% duty cycle. Peak current values are approximately 11% greater. Dissipation in the IC output transistor is the same as in *Figure 6-10.* Average dissipation and I_{EE} current for several values of pull-down resistance to V_{EE} are listed in *Figure 6-14.* The R_E values are appropriate for series termination of transmission lines with impedances listed in the Z_0 column, determined from *Equation 5-12.* Peak current values are approximately 12% greater than average values.

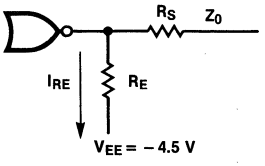
Figures 6-10, 13 and *14* show that the Thevenin equivalent parallel termination method leads to ten times as much dissipation in the resistors as in the single resistor returned to -2 V. Similarly, the dissipation in R_E for series termination is three times the dissipation in the parallel termination resistor to -2 V.

Fig. 6-13 Series Divider for Thevenin Equivalent Terminations



R_T Ω	R_1 Ω = 1.80 R_T	R_2 Ω = 2.25 R_T	$I_{EE\ (avg)}$ mA	$P_{D\ (avg)}$ mW Resistors
50	90	113	28.2	109
62	112	140	22.7	87.9
75	135	169	18.8	72.7
82	148	185	17.2	66.5
90	162	203	15.7	60.5
100	180	225	14.1	54.5
120	216	270	11.7	45.4
150	270	338	9.4	36.3

Fig. 6-14 Average Current and Power Dissipation Using Pull-down Resistor to V_{EE}



Z_0 Ω	R_E Ω	$I_{EE\ (avg)}$ mA	$P_{D\ (avg)}$ mW	
			IC Output	R_E
50	269	9.8	12.9	25.8
62	331	7.9	10.4	20.6
75	399	6.5	8.6	16.8
90	477	5.4	7.1	13.9
100	530	4.9	6.5	12.7
120	634	4.1	5.4	10.6
150	791	3.2	4.2	8.1

Thermal Considerations

System cooling requirements for ECL circuits are based on three considerations: (1) the need to minimize temperature gradients between circuits communicating in the single-ended mode, (2) the need to control the temperature environment of each circuit to assure that the parameters stay within guaranteed limits, and (3) the need to insure that the maximum rated junction temperature is not exceeded.

Temperature gradients are of no practical concern with F100K circuits since they are temperature compensated; their output voltage levels and input thresholds change very little with temperature, as discussed in *Chapter 2.* With uncompensated ECL circuits, output voltage levels and input thresholds vary with temperature. This causes a loss of noise margin when driving and receiving circuits are operating at different temperatures. Loss of HIGH-state noise margin occurs when the receiving circuit is at the higher temperature, amounting to approximately 1 mV/°C of temperature gradient. When the driving circuit is at the higher temperature, the LOW-state margin decreases by approximately 0.5 mV/°C of gradient. The system designer must consider noise margin loss, due to temperature gradients.

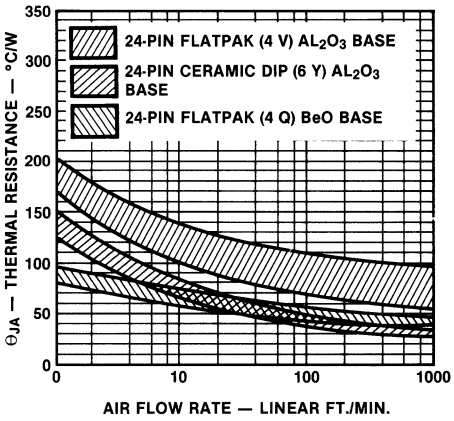
Each dc parameter limit on the F100K data sheets applies over the entire 0°C to +85°C case temperature. For uncompensated ECL circuits, parameter limits have different values for different ambient temperatures. Further, ambient temperature specifications are based on a minimum air flow rate of 400 linear feet per minute. Thermal equilibrium must be established for incoming test results of uncompensated ECL circuits to be valid. The time required to attain equilibrium can vary considerably, depending on the internal dissipation of the particular IC type and details of the thermal arrangement. Normally, an adequate waiting time is three to five minutes after power is applied.

The maximum rated junction temperature of F100K circuits is +150°C. An individual IC junction temperature can be determined by multiplying power dissipation by the junction-to-air thermal resistance θ_{JA} and adding the result to the ambient air temperature. The power dissipation is V_{EE} times I_{EE}, from the data sheet, plus the

dissipation in the output transistors from *Figure 6-10* or *6-14*. Thermal resistance is shown in *Figure 6-15* as a function of cooling air flow rate. This figure applies when the IC is mounted on a board with the air flowing in a plane parallel to the board and perpendicular to the long axis of the IC package. When air temperature, flow rate and package power dissipation are known, junction temperature is determined as follows.

$$T_J = T_A + P_D \theta_{JA} \qquad \textbf{(6-10)}$$

Fig. 6-15. Junction-to-Air Thermal Resistance Versus Air Flow Rate



Conversely, when the maximum rated junction temperature (+150°C), the package power dissipation, and the air temperature are known, the minimum flow rate can be determined by first determining the maximum thermal resistance.

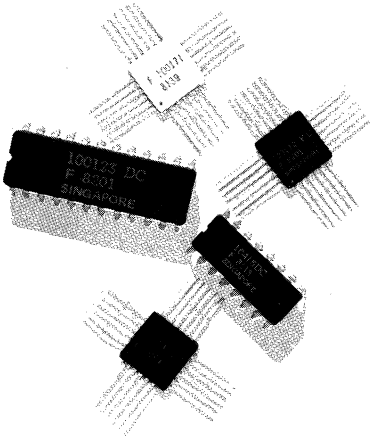
$$\text{Maximum } \theta_{JA} = \frac{(150° - T_A)}{P_D} \qquad \textbf{(6-11)}$$

For this value of θ_{JA} the minimum flow rate is determined from *Figure 6-15*.

When the system designer plans to depend on natural convection for cooling, it is recommended that thermal tests be conducted to determine actual conditions. The effectiveness of natural convection for cooling varies greatly. For instance, on a densely packed logic board in a horizontal attitude in still air, the effective ambient temperature for an IC varies with its position. An IC in the middle of the board is subjected to air that is partially heated by surrounding ICs. Additionally, the temperature of the board rises due to heat flow through the component leads. These effects can cause a much higher junction temperature than might be expected.

Reference

1. Harper, C.A., Editor, *Handbook of Wiring, Cabling and Interconnecting for Electronics,* McGraw-Hill, 1972.



Chapter 7
Testing Techniques

- Introduction
- Tester Selection
- Functional Testing
- DC Testing
- AC Testing
- AC Test Fixtures

Chapter 7
Testing Techniques

Introduction
The purpose of this chapter is assist personnel involved with incoming inspection and qualification testing, by discussing the various methods and techniques used in testing ECL devices.

Testing includes verifying functionality, checking dc parametric limits and measuring ac performance. These tasks are particularly difficult for ECL devices in light of the broad range of products: RAMs, PROMs, gate arrays, and logic circuits. Correlation between supplier and user is extremely important. Recognizing the differences between high-volume instantaneous testing, as performed by the supplier, and the user's concern for long term performance in a given operating environment, Fairchild guarantees the data sheet limits as specified, although testing may be performed by alternate methods.

Tester Selection
Although many makes and types of automatic test systems are available and in use today, not all are capable of testing ECL RAMs, PROMs, logic and gate arrays.

Logic and gate array testers require dc accuracy, subnanosecond ac test capability, and the ability to change software for each device. Software capability and the number of test pins available are major considerations in choosing a gate array tester. Functional, dc and threshold tests are successfully performed on automatic test equipment, but subnanosecond propagation delays are difficult to measure accurately.

The use of dedicated testers to perform high-volume memory testing is very common. Testers containing hardware addressing capability are usually the most efficient. Although basic dc testing is similar for any device type, RAM and PROM functional testing usually require special addressing capabilities to test for pattern sensitivity. The pattern generators and output comparators must have minimum skew to obtain maximum tester accuracy. Functional and ac tests are performed simultaneously; then, dc and threshold tests are performed.

The following considerations must be taken into account when selecting a tester.

Noise
Since the voltage swing on ECL input and output levels is only about 800 mV, it is very important that the power supplies and voltage drivers be extremely clean and free of spikes, hum, or any other type of noise.

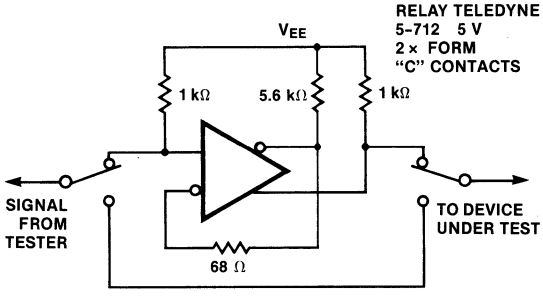
DC Resolution
The threshold measurements ($V_{IH(min)}$, $V_{IL(max)}$) require that input voltage be extremely accurate and repeatable, i.e., if the $V_{IL(max)}$ is specified as −1.475 V, a voltage source of −1.475 ± 5 mV is not adequate to accurately test the part. Ideally, the driver and the output comparators should have an accuracy of ±1 mV.

Current Capability
Since ECL is noted for high current requirements, power supplies for V_{EE} should be capable of supplying current with a 25% reserve over the highest powered parts. This reserve should be included because power supplies tend to get noisy when approaching the current clamp. Some ECL LSI parts dissipate over 4.5 W; therefore, with a V_{EE} of −4.5 V, the power supply must provide well over 1 A.

Edge Rates
When testing edge-triggered sequential logic parts such as flip-flops and shift registers, it is important that the rise and fall times of the clock pulses be fast, clean and free from overshoot. If the clock edges are not adequate, the deficiency can be overcome using a Schmitt trigger as shown in *Figure 7-1*.

The 68 Ω resistor provides hysteresis by positive feedback, thus improving the edge rates. When energized,

Fig. 7-1 Typical Schmitt Trigger Circuit



the relay provides a path to bypass the Schmitt trigger, so the input currents of the device under test can be measured.

Functional Testing
The functional operation and truth table for all device types are checked using automatic test equipment. For memory devices, pattern sensitivity and ac characteristics are also tested automatically. Functional testing is usually performed before dc testing. Logic parts are functionally tested in all modes of operation. The inputs are driven using typical V_{IH} and V_{IL} values. The outputs are compared against relaxed V_{OH} and V_{OL} limits. The V_{IH}, V_{IL}, V_{OH}, and V_{OL} limits are tested during dc testing.

DC Testing
An automatic tester is used to test all dc parameters listed on the individual data sheet for each input and output. The device may have to be preconditioned to obtain the correct output logic state. The cable length should be kept to a minimum to insure signal integrity.

Threshold Measurements
Threshold measurement on an automatic tester is probably the most difficult dc test and the test most prone to oscillation. When testing, take one input at a time to threshold; all other inputs remain at full V_{IH} or V_{IL} levels. If all inputs were at threshold simultaneously, the device would tend to oscillate. For example, to test a flip-flop, make sure the output is LOW before test, take the data pin to HIGH threshold, and apply the clock pulse. Verify that the HIGH has been transferred to the output. Next, apply LOW threshold to the data input and clock it through; use hard levels on the clock (full V_{IH} and V_{IL}). Check that the output pin goes LOW.

Bench Testing
Occasionally, it is necessary to obtain data not easily available from an automatic tester. This is accomplished by testing devices in a universal test board. The typical test circuit board is double-clad copper. All input/output pins go to single-pole, triple-throw switches so that V_{IH}, V_{IL} or a 50 Ω terminating resistor can be connected. Leadless 0.05 μF capacitors decouple all pins to V_{CC} (+2 V) at the socket pins. Access to the device under test is made via banana sockets to the X-Y plotter.

V_{IN}/V_{OUT} Plot—The input ramp supply is 0 V to −2 V varied by a multi-turn potentiometer. The input voltage (V_{IN}) versus output voltage (V_{OUT}) is plotted on an X-Y recorder using the test set-up shown in *Figure 7-2.*

V_{OUT}/I_{OUT} Plot—The output voltage (V_{OUT}) versus output current (I_{OUT}) can be plotted using the test setup shown in *Figure 7-3.*

Fig. 7-2 V_{IN}/V_{OUT} Transfer Characteristics

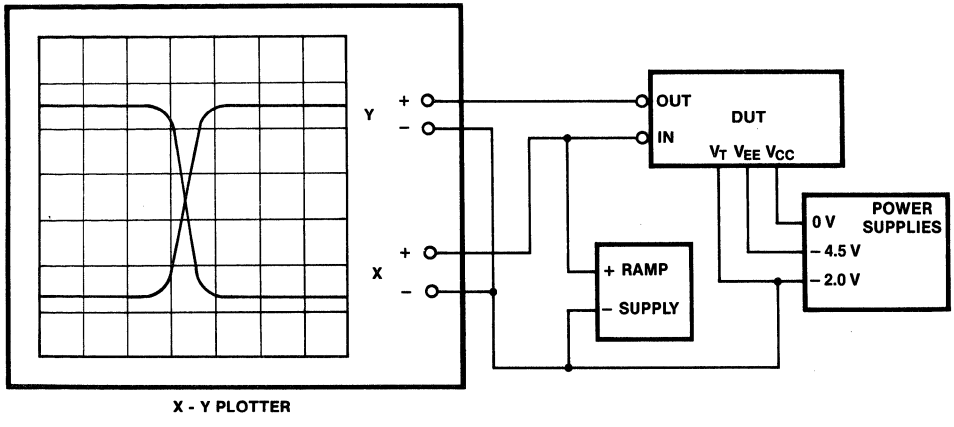
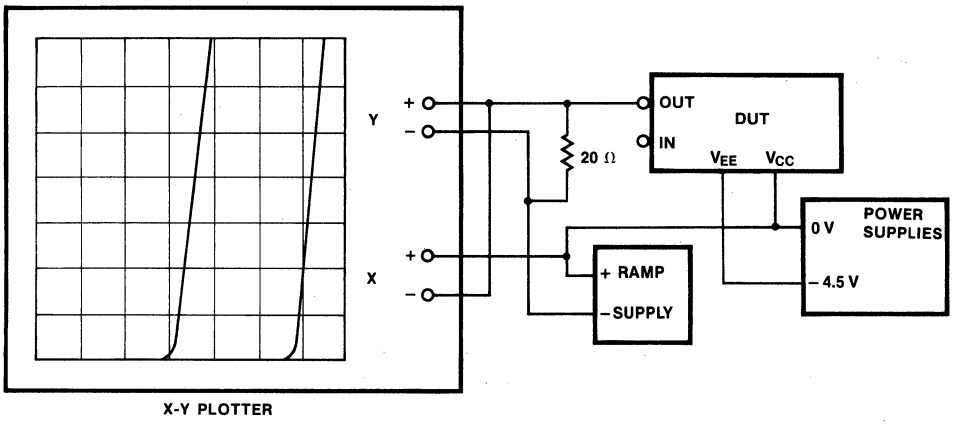


Fig. 7-3 V_{OUT}/I_{OUT} Characteristics



AC Testing
Because few automatic measurement systems have sufficient accuracy to perform subnanosecond testing, ac testing of ECL is one of the most difficult tests to accomplish. To obtain subnanosecond accuracy usually requires special test fixtures and equipment. The physical location of the test fixture, the input driver and the output comparator is very important.

Depending upon the accuracy and repeatability of the automatic tester, a bench setup may be required for correlation. Comparing an air line with known propagation delay to the test setup is recommended.

AC Test Fixtures
Test fixture design plays a pivotal role in insuring that undistorted waveforms are applied to the Device Under Test (D.U.T.) and that the device output can be monitored correctly.

Board Construction and Layout
ECL ac bench test fixtures are built on a double-clad printed circuit board or on a multilayer printed circuit board with semi-rigid coax, *Figures 7-4* and *7-5*. The power planes are shorted at the device and brought out to banana sockets with the decoupling capacitors at the device. Transmission lines of 50 Ω are maintained from soldered-on BNC or SMA connectors to the D.U.T. Sense lines from the D.U.T. output and input pins to the connectors must be of electrically equal length. For input pins, care must be taken to insure that the force and sense lines are brought directly to the point that makes contact with the D.U.T. For output pins, only the output sense lines are used to monitor the signals. The force lines are disconnected at the device to minimize signal distortion. Special care must be taken to minimize crosstalk and stray capacitance in the area of the D.U.T. For correlation, flatpaks are not tested in sockets but are clamped to the traces of a multilayer PC board. Dual in-line devices are plugged into individual pin sockets instead of normal test sockets. Due to equipment limitations and for correlation, the amplitude, offset, rise and fall time are set up with no device in the test socket.

The bench test fixture to measure toggle frequency utilizes the principles described in the preceding paragraph except that the feedback path between the output and data input is as short as possible.

Output Termination
All outputs should be terminated with 50 Ω ±1% resistors. This is especially important for complementary outputs. When bench testing, the device is offset by +2 V; V_{EE} is −2.5 V, V_{CC}, V_{CCA} is +2 V. Then the 50 Ω input impedance of the sampling oscilloscope acts as the termination resistor to 0 V. The input and output coaxial cable to the oscilloscope should be cut to exactly the same electrical length.

Decoupling
Not enough emphasis can be put on the importance of good decoupling on the D.U.T. because oscillations can give erroneous test results. A sampling scope should be used to make sure that oscillation is not occurring.

The value of capacitors used depends on the type of tester used and the frequency of test. Some testers use pulse test; in other words, for each individual test in a program, V_{EE} is powered up and down. On this type of tester, electrolytic-type (*i.e.,* large value) capacitors cannot be used because of the time constant needed to charge the capacitor.

Always start with the minimum decoupling needed to achieve good results, perhaps merely a capacitor between V_{CC} and V_{EE}. Capacitors should be placed as close as possible to the D.U.T. to eliminate as much inductance as possible. Only low-inductance capacitors should be used; leadless monolithic ceramic capacitors are very effective.

There are no rigid decoupling rules, and each device type may have it own decoupling requirements. A typical decoupling technique that works well on most F100K devices is to place 0.01 to 0.1 μF monolithic ceramic capacitors in the following locations.

- If no offset is used:
  between V_{EE} (−4.5 V) and V_{CC}, V_{CCA} (0 V)
  between V_{TT} (−2 V) and ground (0 V)
- If +2 V offset is used:
  between V_{CC}, V_{CCA} (+2 V) and ground (0 V)
  between V_{EE} (−2.5 V) and ground (0 V)
- In most cases, V_{CCA} and V_{CC} should be shorted as close to the D.U.T. as possible. However, if the V_{CCA} and V_{CC} pins are physically separated, individual decoupling capacitors may be necessary.
- For dc tests only place a 0.001 μF capacitor:
  between an input pin and V_{EE}
  between an output pin and V_{CCA}

Decoupling problems will appear mainly at threshold test. If certain outputs fail try the decoupling technique, described in the preceding paragraph, on those outputs and the associated inputs. With testers that use the power-hold method, such as the Sentry®, large electrolytics can be used in parallel with smaller (0.01 μF) disk capacitors for the high-frequency bypass.

Fig. 7-4 Multilayer Test Fixture (Top View)

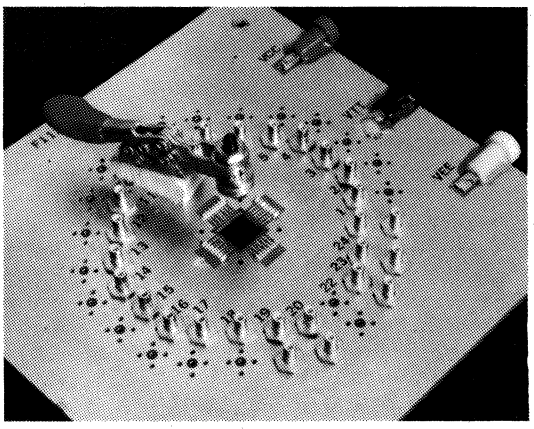
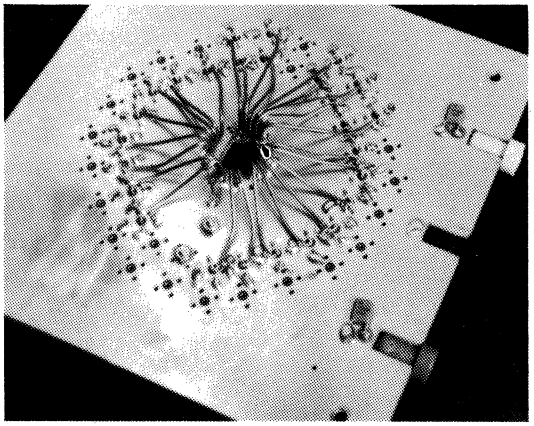
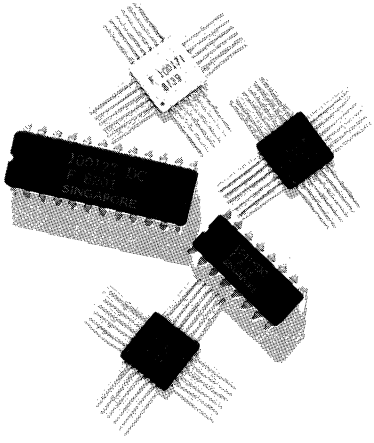


Fig. 7-5 Multilayer Test Fixture (Bottom View)





Chapter 8
Quality Assurance and Reliability

- Introduction
- Incoming Quality Inspection
- Process Quality Control
- Quality Assurance
- Reliability

8

Quality Assurance and Reliability

Introduction
F100K ECL is manufactured to strict quality and reliability standards. Product conformance to these standards is insured by careful monitoring of the following functions: (1) incoming quality inspection, (2) process quality control, (3) quality assurance, and (4) reliability.

Incoming Quality Inspection
Purchased piece parts and raw materials must conform to purchase specifications. Major monitoring programs are the inspection of package piece parts, inspection of raw silicon wafers, and inspection of bulk chemicals and materials. Two other important functions of incoming quality inspection are to provide real-time feedback to vendors and in-house engineering, and to define and initiate quality improvement programs.

Package Piece Parts Inspection
Each shipment of package piece parts is inspected and accepted or rejected based on AQL sampling plans. Inspection tests include both inherent characteristics and functional use tests. Inherent characteristics include physical dimensions, color, plating quality, material purity, and material density. Functional use tests for various package piece parts include die attach, bond pull, seal, lid torque, salt atmosphere, lead fatigue, solderability, and mechanical strength. In these tests, the piece parts are sent through process steps that simulate package assembly. The units are then destructively tested to determine whether or not they meet the required quality and reliability levels.

Silicon Wafer Inspection
Each shipment of raw silicon wafers is accepted or rejected based on AQL sampling plans. Raw silicon wafers are subjected to non-destructive and destructive tests. Included in the testing are flatness, physical dimensions, resistivity, oxygen and carbon content, and defect densities. The test results are used to accept or reject the lot.

Bulk Chemical and Material Inspection
Bulk chemicals and materials play an important role in any semiconductor process. To insure that the bulk chemicals and materials used in processing F100K wafers are the highest quality, they are stringently tested for trace impurities and particulate or organic contamination. Mixtures are also analized to verify their chemical make-up.

Incoming inspection is only the first step in determining the acceptability of bulk chemicals and materials. After acceptance, detailed documentation is maintained to correlate process results to various vendors and to any variations found in mixture consistency.

Process Quality Control
Process quality is maintained by establishing and maintaining effective controls for monitoring the wafer fabrication process, reporting the results of the monitors, and initiating valid measurement techniques for improving quality and reliability levels.

Methods of Control
The process quality control program utilizes the following methods of control: (1) process audits, (2) environmental monitors, (3) process monitors, (4) lot acceptance inspections, (5) process qualifications, and (6) process integrity audits. These methods of control, defined below, characterize visually and electrically the wafer fabrication operation.

Process Audit—Audits concerning manufacturing operator conformance to specification. These are performed on all operations critical to product quality and reliability.

Environmental Monitor-Monitors concerning the process environment, i.e., water purity, air temperature/humidity, and particulate count.

Process Monitor—Periodic inspection at designated process steps for verification of manufacturing inspection and maintenance of process average. These inspections provide both attribute and variables data.

Lot Acceptance—Lot by lot sampling. This sampling method is reserved for those operations deemed as critical and, as such, requiring special attention.

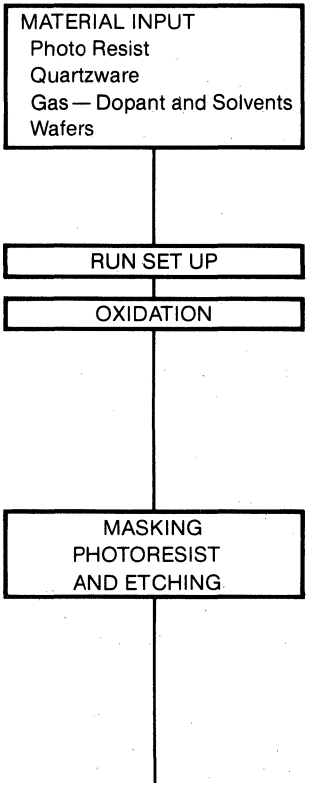
Process Qualification—Complete distributional analysis is run to specified tolerance averages and standard deviations. These qualifications are typically conducted on deposition and evaporation processes, i.e., epi, aluminum, vapox, and backside gold.

Process Integrity Audit—Special audits conducted on oxidation and metal evaporation processes (CV drift—oxidation; SEM evaluation—metal evaporation).

Data Reporting
Process quality control data is recorded on an attribute or variable basis as required; control charts are maintained on a regular basis. This data is reviewed at periodic intervals and serves as the basis for judging the acceptability of specific processes. Summary data from the various process quality control operations are relayed to cognizant line, engineering and management personnel in real time so that, if appropriate, the necessary corrective actions can be immediately taken.

Process Flow
Figure 8-1 shows the integration of the various methods of control into the wafer fabrication process flow. The process flow chart contains examples of the process quality controls and inspections utilized in the manufacturing operation.

Fig. 8-1 Process Flow Chart



Process Controls (Examples)

A. Environmental
B. Chemical supplies
C. Substrate examination (resistivity, flatness, thickness, crystal perfection, etc.)
D. Photoresist evaluation
E. Mask inspections

A. Process audit

A. Process audit/qualification
B. Environmental
C. Process monitors (thickness, pinhole and crack measurements)
E. C V Plotting
F. Calibration

A. Process audits
B. Environmental
C. Visual examinations
D. Photoresist evaluation (preparation, storage, application, baking, development and removal),
E. Etchant controls
F. Exposure controls (intensity, uniformity)

Fig. 8-1 Process Flow Chart (cont'd.)

SOLID STATE DIFFUSIONS: Buried Layer, Epitaxy, Getter, Ion Implant, Base and Emitter	A. Process audits/qualification B. Environmental C. Temperature profiling D. Quartz cleaning E. Calibration F. Electrical tests (resistivity, breakdown voltages, etc.)
THIN FILM: Metal (aluminum, nichrome, titanium-tungsten and Chemical Vapor) Deposition (silox, doped silox and nitride passivation)	A. Process audits/qualification B. Environmental C. Visual examinations D. Epitaxy controls (thickness, resistivity cleaning, visual examination) E. Metallization controls (thickness, temperature cleaning, SEM, C V plotting) F. Glassivation controls (thickness, dopant concentraton, pinhole and crack measurements)
WAFER SORT	A. Process audit B. Environmental C. Visual examinations
OUTGOING WAFER INSPECTION	A. Process audit B. Inspection
ASSEMBLY	

Quality Assurance

To assure that all product shipped meets both internal Fairchild specifications for standard product and customer specifications in the case of negotiated specs, a number of QA inspections throughout the assembly process flow (*Figure 8-2*) are required.

Many of the assembly operations follow the requirements of MIL-M-38510 (General Specification for Microcircuits). The test methods employed and listed are described in MIL-STD-883 (Test Methods and Procedures for Microelectronics). Most of the internal specifications, as a result, closely follow the procedures of the military specifications.

For ease of reference, and for clearer understanding of the operations performed, the MIL-STD-883 methods are stated when applicable. A flow, much more detailed than the one presented in *Figure 8-2*, governs the assembly of the devices and the performance of the environmental, mechanical, and electrical tests.

Fig. 8-2 Generalized Process Flow

Operation	Method
Die Forming/Scribe	
Plate	
Internal Visual (2nd OPT)	2010/B
QA—Internal Visual (2nd OPT) Optional	2010/B
Die Attach	
QA—Die Shear Strength	2019
Ultrasonic Bonding	
QA—Ultrasonic Bond Strength	2011
Internal Visual (3rd OPT)	2010
QA—Internal Visual (3rd OPT)	2010
Seal—Solder or Glass	
External Visual (4th OPT)	2009
QA—External Visual (4th OPT)	2009
High Temperature Storage	1008/C, E
Temperature Cycling	1010/C
Constant Acceleration	2001/E

Operation (cont'd.)	Method (cont'd.)
Plating (Tin/Gold) — Lead Finish	
QA—Plating Inspection/Solderability	2003
Lead Clip and Form	
Seal, Fine (Hermeticity Check)	1014 5×10^{-8} cc/sec
Seal, Gross (Hermeticity Check)	Bubble Test—Fluorocarbon
Mark and Pack	
QA—External Visual	2009
QA—Seal, Fine (Hermeticity Check)	1014 5×10^{-8} cc/sec
QA—Seal, Gross (Hermeticity Check)	Bubble Test—Fluorocarbon
Electrical Test	
Quality Conformance (Group A)	5005
QA—Plant Clearance	
Distribution Store	

Reliability
A number of programs, among them qualification testing, reliability monitoring, failure analysis, and reliability data collection and presentation, are maintained.

Qualification Programs
All products receive reliability qualification prior to the product being released for shipment. Qualification is required for (1) new product designs, (2) new fabrication processes or (3) new packages or assembly processes. Stress tests are run in accordance to test methods described in MIL-STD-883B. Test results are evaluated against existing reliability levels, and must be better than or equal to current product for the new product to receive qualification.

New Product Designs—Receive, as a minimum, +125°C operating life tests. Readouts are normally scheduled at 168 hours, 1168 hours and 2168 hours. The samples stressed are electrically good units from initial wafer runs. Additional life testing, consisting of high-temperature operating life test, 85/85 humidity bias tests and bias pressure pot (BPTH) tests, may be run as deemed necessary. Redesigns of existing device layouts are considered to be new product designs, and full qualification is necessary.

New Fabrication Processes—Qualifications are designed to evaluate the new process against the current process. Stress tests consist of operating life test, high-temperature operating life test, 85/85 humidity bias test and/or biased pressure pot (BPTH) test. In addition, package environment tests may be performed. Evaluations are performed on various products throughout the development stages of the new process. Units stressed are generally from split wafer runs. All processing is performed as a single wafer lot up to the new process steps, where the lot is split for the new and the current process steps. Then the wafers are recombined, and again processed as a single wafer lot. This allows for controlled evaluation of the new process against the standard process. Both significant modifications to existing process and transferring existing products to new fabrication plants are treated as a new process.

New Packages or Assembly Processes—Qualifications are performed for new package designs, changes to existing piece parts, changes in piece part vendors, and significant modification to assembly process methods. In general, samples from three assembly runs are stressed to a matrix in accordance to MIL-STD-883B, Method 5005, group B, group C, subgroup 2, and group D (*Table 8-1*). In addition, +100°C operating life tests, 85/85 humidity bias tests, biased pressure pot (BPTH) tests and unbiased pressure pot tests are performed.

Reliability Monitors
Reliability testing of mature products is performed to establish device failure rates, and to identify problems occuring in production. Samples are obtained on a regular basis from production. These units are stressed with operating life tests or package environmental tests. The results of these tests are summarized and reported on a monthly basis. When a problem is identified, the respective engineering group is notified, and production is stopped until corrective action is taken.

Current testing levels are in excess of 14,000 units per year stressed with operating life tests, and 23,000 units per year stressed with package environmental tests.

Failure Analysis
Failure analysis is performed on all units failing reliability stress tests. Failure analysis is offered as a service to support manufacturing and engineering, and to support customer returns and customer requested failure studies. The failure analysis procedure used has been established to provide a technique of sequential analysis. This technique is based on the premise that each step of analysis will provide information of the failure without destroying information to be obtained from subsequent steps. The ultimate purpose is to uncover all underlying failure mechanisms through complete, in-depth, defect analysis. The procedure places great emphasis on electrical analysis, both external before decapsulation, and internal micro-probing. Visual examinations with high magnification microscopes or SEM analysis are used to confirm failure mechanisms. Results of the failure analysis are recorded and, if abnormalities are found, reported to engineering and/or manufacturing.

Data Collection and Presentation
Product reliability is controlled by first stressing the product, and then feeding back results to manufacturing and engineering. This feedback takes two forms. There is a formal monthly Reliability Summary distributed to all groups. The summary shows current product failure

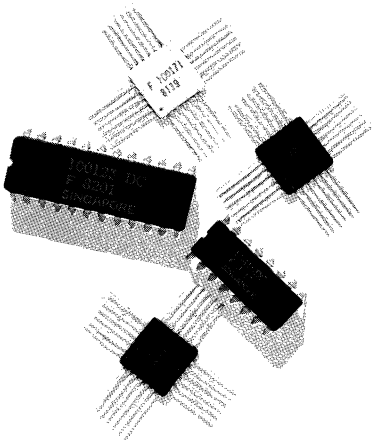
rates, highlights problem areas, and shows the status of qualification and corrective action programs. Less formal feedback is obtained by including reliability personnel at all product meetings, which gives high visibility to the reliability aspects of various products. As a customer service, product reliability data is compiled and made available upon request.

Table 8-1 Package Environmental Stress Matrix

Test	MIL-STD-883 Method	MIL-STD-883 Condition
Group B		
Subgroup 1		
Physical dimensions	2016	
Subgroup 2		
Resistance to solvents	2015	
Subgroup 3		
Solderability	2003	Soldering temperature of 260 ± 10°C
Subgroup 5		
Bond strength	2011	
(1) Thermocompression		(1) Test condition C or D
(2) Ultrasonic or wedge		(2) Test condition C or D
Group C		
Subgroup 2		
Temperature Cycling	1010	Test condition C (−65°C to +150°C)
Constant Acceleration	2001	Test condition E (30 Kg), Y_1 orientation and X_1 orientation Test condition D (20 Kg) for packages over 5 gram weight or with seal ring greater than 2 inches
Seal	1014	
(a) Fine		
(b) Gross		
Visual examination		
End-point electrical parameters		
Group D		
Subgroup 1		
Physical Dimensions	2016	
Subgroup 2		
Lead integrity	2004	Test condition B2 (lead fatigue)
Seal	1014	As applicable
(a) Fine		
(b) Gross		
Lid torque	2024	As applicable

Table 8-1 Package Environmental Stress Matrix (cont'd.)

Subgroup 3		
Thermal shock	1011	Test condition B (−55°C to +125°C) 15 cycles minimum
Temperature cycling	1010	Test condition C, (−65°C to +150°C) 100 cycles minimum.
Moisture resistance	1004	
Seal	1014	
(a) Fine		
(b) Gross		
Visual examination		
End-point electrical parameters		
Subgroup 4		
Mechanical shock	2002	Test condition B (1500g, 0.5 ms)
Vibration, variable frequency	2007	Test condition A (20 g)
Constant acceleration	2001	Same as group C, subgroup 2
Seal		
(a) Fine		
(b) Gross		
Visual examination		
End-point electrical parameters		
Subgroup 5		
Salt atmosphere	1009	Test condition A minimum (24 hours)
Seal	1014	As applicable
(a) Fine		
(b) Gross		
Visual examination		
Subgroup 6		
Internal water-vapor content	1018	
Subgroup 7		
Adhesion of lead finish	2025	



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