MB86950

FUJITSU

EtherStar™ Ethernet Controller

FACT SHEET

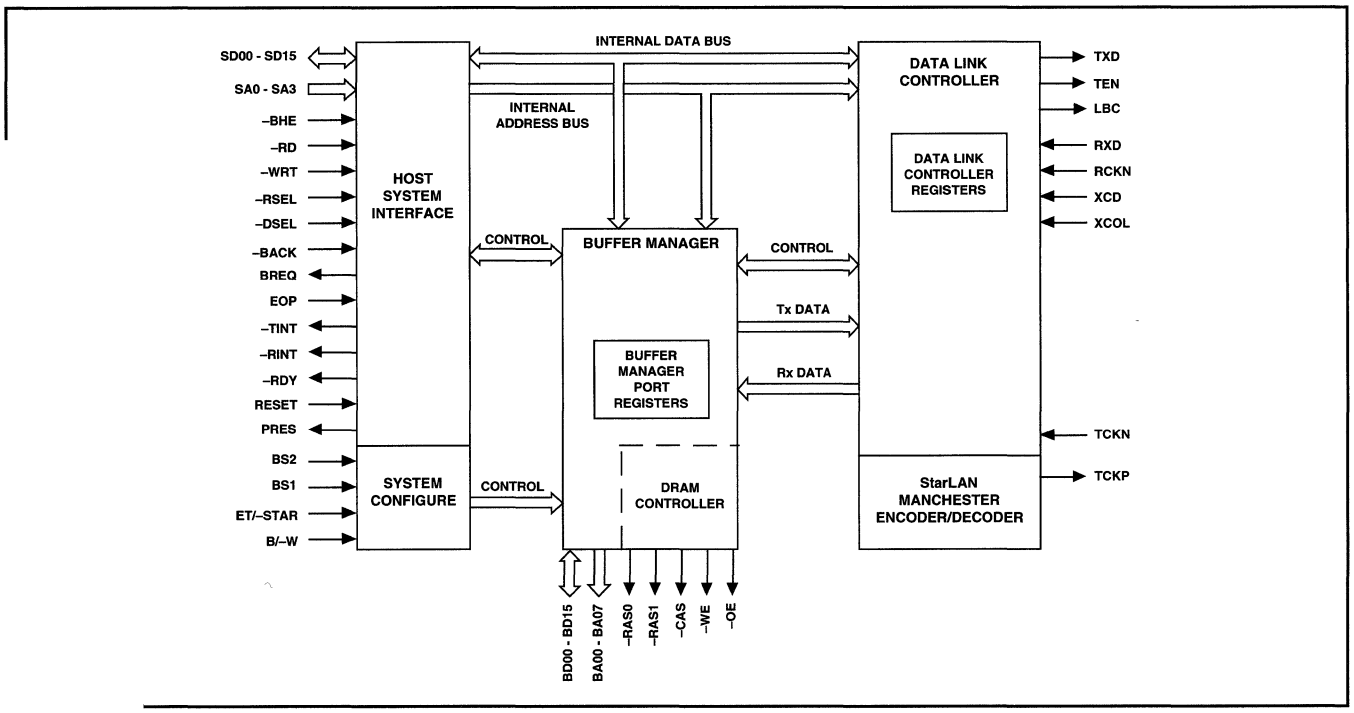
FEBRUARY 1991

FEATURES

- IEEE 802.3 CSMA/CD Ethernet/Thin-Ethernet/ 10BASE-T and StarLAN™ compatibility
- Configurable for 8-bit or 16-bit data path widths
- Unique buffer management architecture arbitrates all dedicated SRAM or DRAM memory data accesses and automatically allocates buffer memory area for incoming data frames, automatically updating pointers
- Allows automatic retransmission of data packets during collisions, thus saving bus bandwidth
- Addresses 8, 16, 32, or 64 Kbytes of dedicated SRAM or DRAM buffer memory. Dedicated buffer memory architecture allows data packet reception without using bus bandwidth
- Supports DMA transfers
- Dual metal, CMOS technology
- Available in 84-pin plastic J-bend PLCC or 80-pin PQFP package

DESCRIPTION

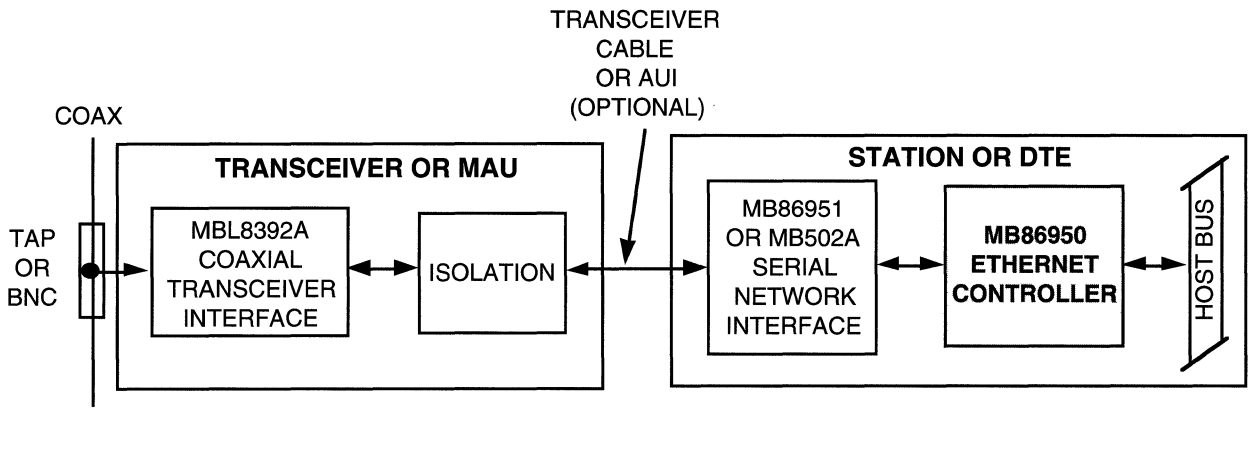
The MB86950 EtherStar Ethernet Controller is fully compliant with IEEE 802.3 10BASE5 Ethernet, 10BASE2 Thin-Ethernet/ Cheapernet and 10BASE-T twisted pair configurations. The MB86950 is part of a three-chip set available from Fujitsu which also includes the MB86951 Serial Network Interface and the MBL8392A Coaxial Transceiver or MB86962 10BASE-T Transceiver. EtherStar integrates a Data Link Controller, a Dynamic Memory Controller, a Buffer Management Unit, and a 1 Mbps Manchester encoder/decoder on a single chip. Unique to the controller is its on-chip arbitration logic or buffer manager that controls access to a dedicated SRAM or DRAM buffer memory. The dedicated buffer memory is connected directly to the controller, thus eliminating the need for a local bus. The controller manages the packet data structure by automatically updating receive and transmit pointers, and allocating space in the buffer memory. The amount of driver software code needed to handle these operations is reduced considerably. The EtherStar architecture eliminates concerns about FIFO size limitations, system timing constraints and contention on the local bus. Data packets can be received from the network into the dedicated buffer memory and data packets can be transferred to or from the controller simultaneously resulting in superior media to host transfer throughput.



EtherStar Ethernet Controller Block Diagram

MB86950
ETHERSTAR ETHERNET CONTROLLER

The diagram below shows a complete Ethernet coaxial interface implemented with the Fujitsu chip set.



Typical System Diagram

Order Information

PACKAGE STYLE	PACKAGE CODE	ORDERING CODE
80-pin Plastic Quad Flat Pack	FPT-80P-M01	MB86950BPF-G
84-pin Plastic Leaded Chip Carrier	LCC-84P-M01	MB86950BPD-G

Fujitsu supplies many components for your local area networking requirements, including controllers, bus interfaces, transceivers and a large variety of memories. For additional information, contact the Fujitsu Microelectronics sales office, sales representative or authorized distributor in your area, or contact:

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