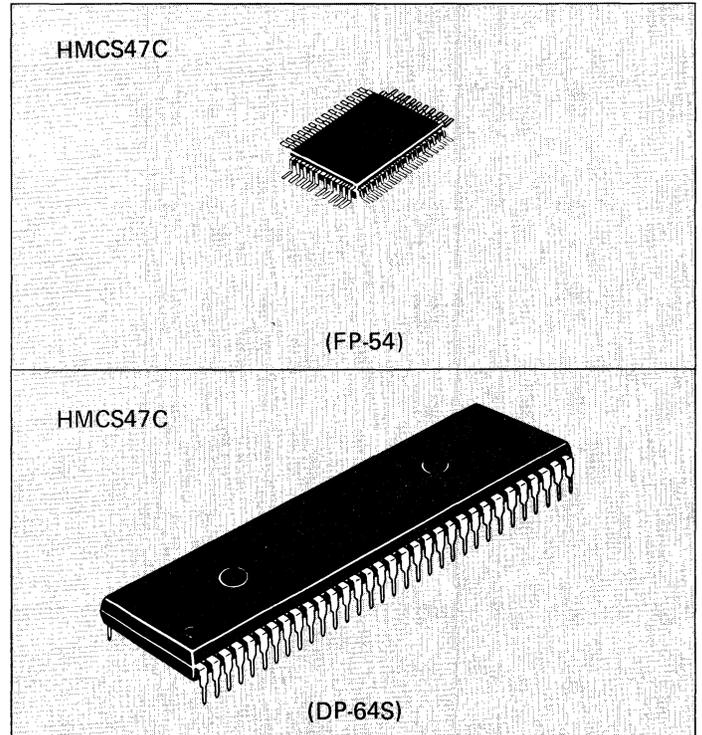# HITACHI HMCS47C
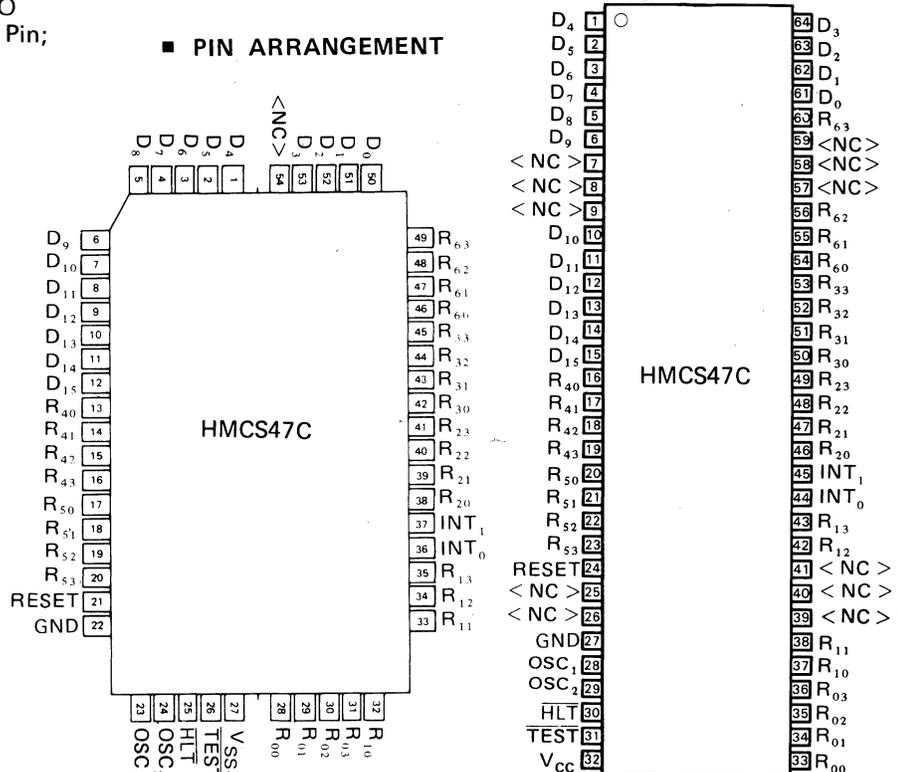# 4-BIT SINGLE-CHIP MICROCOMPUTER

**◎ HITACHI**

The HMCS47C is the CMOS 4-bit single chip microcomputer which contains ROM, RAM, I/O and Timer/Counter on single chip. The HMCS47C is designed to perform efficient controller function as well as arithmetic function for both binary and BCD data. The CMOS technology of the HMCS47C provides the flexibility of microcomputers for battery powered and battery back-up applications.

## ■ FEATURES
- 4-bit Architecture
- 4,096 Words of Program ROM and Pattern ROM (10 bits/Word)
- 256 Digits of Data RAM (4 bits/Digit)
- 44 I/O Lines and 2 External Interrupt Lines
- Timer/Counter
- 5 $\mu$sec Instruction Cycle Time
- All Instructions except One Instruction; Single Word and Single Cycle
- BCD Arithmetic Instructions
- Pattern Generation Instruction
  − Table Look Up Capability −
- Powerful Interrupt Function
  - 3 Interrupt Sources
    - ├─2 External Interrupt Lines
    - └─Timer/Counter
  - Multiple Interrupt Capability
- Bit Manipulation Instructions for Both RAM and I/O
- Option of I/O Configuration Selectable on Each Pin; With Pull up MOS or CMOS or Open Drain
- Built-in Oscillator (Resistor or Ceramic Filter)
- Built-in Power-on Reset Circuit
- Low Operating Power Dissipation; 3.3mW typ.
- Stand-by Mode (Halt Mode); 66 $\mu$W max.
- CMOS Technology
- Single, +5V Power Supply
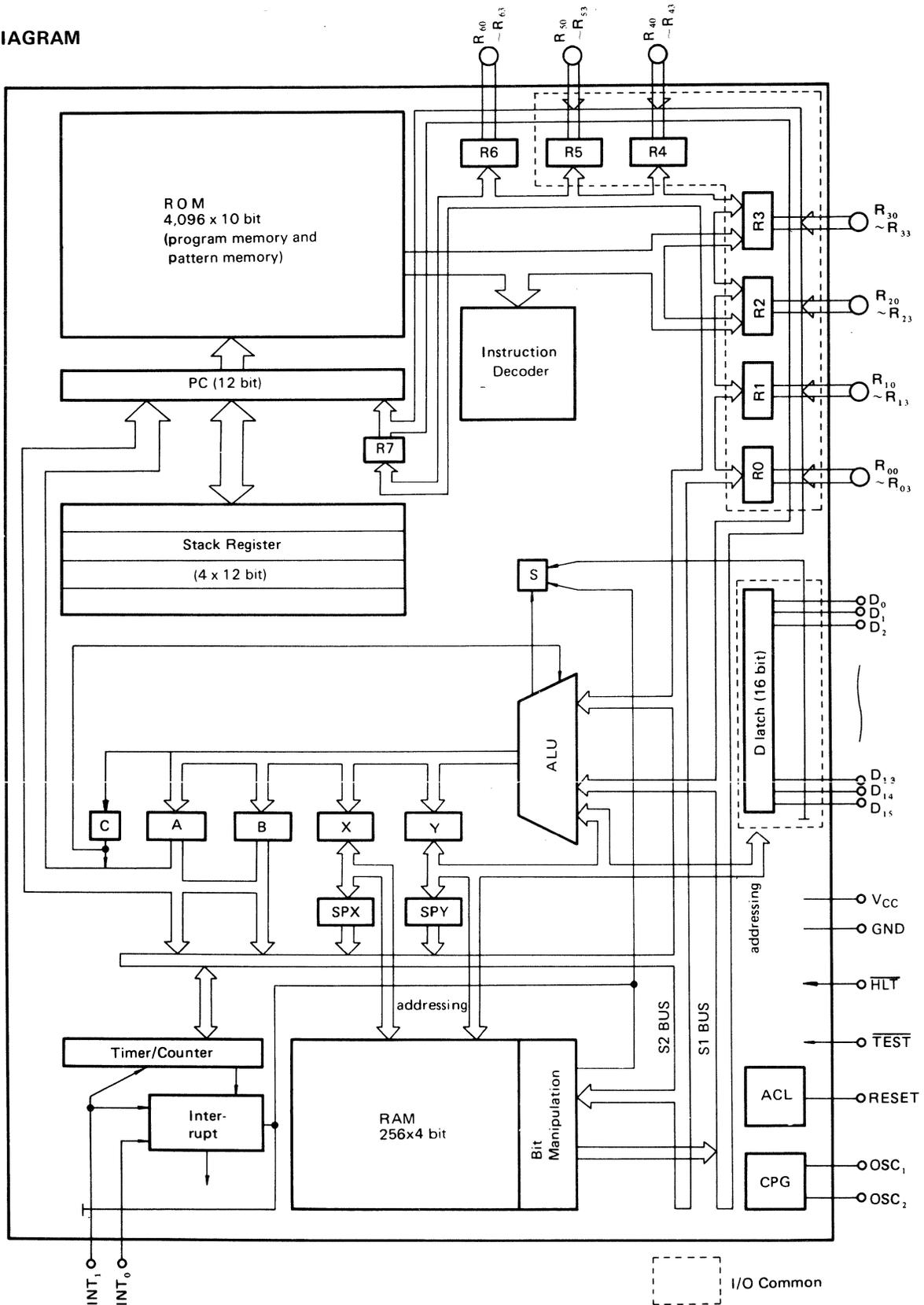- 54-pin Flat Plastic Package (FP-54) or 64-pin Dual-in-line Plastic Package (DP-64S)

HMCS47C

(FP-54)

HMCS47C

(DP-64S)

## ■ PIN ARRANGEMENT

HMCS47C

| Pin | Signal |
|---|---|
| $D_9$ | 6 |
| $D_{10}$ | 7 |
| $D_{11}$ | 8 |
| $D_{12}$ | 9 |
| $D_{13}$ | 10 |
| $D_{14}$ | 11 |
| $D_{15}$ | 12 |
| $R_{40}$ | 13 |
| $R_{41}$ | 14 |
| $R_{42}$ | 15 |
| $R_{43}$ | 16 |
| $R_{50}$ | 17 |
| $R_{51}$ | 18 |
| $R_{52}$ | 19 |
| $R_{53}$ | 20 |
| RESET | 21 |
| GND | 22 |

| 49 | $R_{63}$ |
| 48 | $R_{62}$ |
| 47 | $R_{61}$ |
| 46 | $R_{60}$ |
| 45 | $R_{33}$ |
| 44 | $R_{32}$ |
| 43 | $R_{31}$ |
| 42 | $R_{30}$ |
| 41 | $R_{23}$ |
| 40 | $R_{22}$ |
| 39 | $R_{21}$ |
| 38 | $R_{20}$ |
| 37 | $INT_1$ |
| 36 | $INT_0$ |
| 35 | $R_{13}$ |
| 34 | $R_{12}$ |
| 33 | $R_{11}$ |

Top pins: $D_8$(5) $D_7$(4) $D_6$(3) $D_5$(2) $D_4$(1) <NC>(54) $D_3$(53) $D_2$(52) $D_1$(51) $D_0$(50)

Bottom pins: OSC₁(23) OSC₂(24) HLT(25) TEST(26) $V_{SS}$(27) $R_{00}$(28) $R_{01}$(29) $R_{02}$(30) $R_{03}$(31) $R_{10}$(32)

HMCS47C (DP-64S)

| Left | | Right | |
|---|---|---|---|
| $D_4$ | 1 | 64 | $D_3$ |
| $D_5$ | 2 | 63 | $D_2$ |
| $D_6$ | 3 | 62 | $D_1$ |
| $D_7$ | 4 | 61 | $D_0$ |
| $D_8$ | 5 | 60 | $R_{63}$ |
| $D_9$ | 6 | 59 | <NC> |
| < NC > | 7 | 58 | <NC> |
| < NC > | 8 | 57 | <NC> |
| < NC > | 9 | 56 | $R_{62}$ |
| $D_{10}$ | 10 | 55 | $R_{61}$ |
| $D_{11}$ | 11 | 54 | $R_{60}$ |
| $D_{12}$ | 12 | 53 | $R_{33}$ |
| $D_{13}$ | 13 | 52 | $R_{32}$ |
| $D_{14}$ | 14 | 51 | $R_{31}$ |
| $D_{15}$ | 15 | 50 | $R_{30}$ |
| $R_{40}$ | 16 | 49 | $R_{23}$ |
| $R_{41}$ | 17 | 48 | $R_{22}$ |
| $R_{42}$ | 18 | 47 | $R_{21}$ |
| $R_{43}$ | 19 | 46 | $R_{20}$ |
| $R_{50}$ | 20 | 45 | $INT_1$ |
| $R_{51}$ | 21 | 44 | $INT_0$ |
| $R_{52}$ | 22 | 43 | $R_{13}$ |
| $R_{53}$ | 23 | 42 | $R_{12}$ |
| RESET | 24 | 41 | < NC > |
| < NC > | 25 | 40 | < NC > |
| < NC > | 26 | 39 | < NC > |
| GND | 27 | 38 | $R_{11}$ |
| $OSC_1$ | 28 | 37 | $R_{10}$ |
| $OSC_2$ | 29 | 36 | $R_{03}$ |
| $\overline{HLT}$ | 30 | 35 | $R_{02}$ |
| $\overline{TEST}$ | 31 | 34 | $R_{01}$ |
| $V_{CC}$ | 32 | 33 | $R_{00}$ |

(Top View)

## ■ BLOCK DIAGRAM

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## ■ MAXIMUM RATINGS

| Item | Symbol | Value | Unit | Remarks |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.3 to +7.0 | V | |
| Terminal Voltage (1) | $V_{T1}$ | -0.3 to $V_{CC}$ + 0.3 | V | Except for the terminals specified by $V_{T2}$ |
| Terminal Voltage (2) | $V_{T2}$ | -0.3 to +10.0 | V | Applied to the Open Drain type of Output pins and Open Drain type of I/O pins. |
| Maximum Total Output Current (1) | $-\Sigma I_{O1}$ | 45 | mA | [NOTE 3] |
| Maximum Total Output Current (2) | $\Sigma I_{O2}$ | 45 | mA | [NOTE 3] |
| Operating Temperature | $T_{opr}$ | -20 to +75 | $^\circ$C | |
| Storage Temperature | $T_{stg}$ | -55 to +125 | $^\circ$C | |

[NOTE 1]  Permanent LSI damage may occur if "Maximum Ratings" are exceeded. Normal operation should be under the conditions of "Electrical Characteristics –1, –2." If these conditions are exceeded, it could be cause of malfunction of LSI and affect reliability of LSI.

[NOTE 2]  All voltages are with respect to GND.

[NOTE 3]  The Maximum Total Output Current is total sum of output currents which can flow out (or flow in) from or into the I/O pins and Output pins simultaneously.

## ■ ELECTRICAL CHARACTERISTICS-1 ($V_{CC} = 5V \pm 10\%$, Ta = $-20°C$ to $+75°C$)

| Item | Symbol | Test Conditions | Value min | Value typ | Value max | Unit | Note |
|---|---|---|---|---|---|---|---|
| Input "Low" Voltage | $V_{IL}$ | | — | — | 1.0 | V | |
| Input "High" Voltage (1) | $V_{IH1}$ | | $V_{CC} - 1.0$ | — | $V_{CC}$ | V | 2 |
| Input "High" Voltage (2) | $V_{IH2}$ | | $V_{CC} - 1.0$ | — | 10 | V | 3 |
| Output "Low" Voltage | $V_{OL}$ | $I_{OL} = 1.6mA$ | — | — | 0.8 | V | |
| Output "High" Voltage (1) | $V_{OH1}$ | $-I_{OH} = 1.0mA$ | 2.4 | — | — | V | 4 |
| Output "High" Voltage (2) | $V_{OH2}$ | $-I_{OH} = 0.01mA$ | $V_{CC} - 0.3$ | — | — | V | 5 |
| Interrupt Input Hold Time | $t_{INT}$ | | $2 \cdot T_{inst}$ | — | — | $\mu s$ | |
| Output "High" Current | $I_{OH}$ | $V_{OH} = 10V$ | — | — | 3 | $\mu A$ | 6 |
| Input Leakage Current | $I_{IL}$ | $V_{in} = 0$ to $V_{CC}$ | — | — | 1 | $\mu A$ | 2 |
| | | $V_{in} = 0$ to 10V | — | — | 3 | | 3 |
| Pull up MOS Current | $-I_P$ | $V_{CC} = 5V$ | 60 | 125 | 250 | $\mu A$ | |
| Supply Current (1) | $I_{CC1}$ | $V_{in} = V_{CC}$, $V_{CC} = 5V$, Ceramic Filter Oscillation, ($f_{osc} = 800kHz$) | — | 1.0 | 2.0 | mA | |
| Supply Current (2) | $I_{CC2}$ | $V_{in} = V_{CC}$, $V_{CC} = 5V$ $R_f$ Oscillation, ($f_{osc} = 800kHz$) External Clock Operation ($f_{cp} = 800kHz$) | — | 0.65 | 0.85 | mA | 7 |
| Standby I/O Leakage Current | $I_{LS}$ | $\overline{HLT} = 1.0V$ $V_{in} = 0$ to $V_{CC}$ | — | — | 1 | $\mu A$ | 5, 8 |
| | | $V_{in} = 0$ to 10V | — | — | 3 | $\mu A$ | 6, 8 |
| Standby Supply Current | $I_{CCS}$ | $V_{in} = V_{CC}$, $\overline{HLT} = 0.2V$ | — | 2.0 | 12 | $\mu A$ | 9 |
| External Clock Operation | | | | | | | |
| External Clock Frequency | $f_{cp}$ | | 350 | — | 850 | kHz | |
| External Clock Duty | Duty | | 45 | 50 | 55 | % | |
| External Clock Rise Time | $t_{rcp}$ | | 0 | — | 0.2 | $\mu s$ | |
| External Clock Fall Time | $t_{fcp}$ | | 0 | — | 0.2 | $\mu s$ | |
| Instruction Cycle Time | $T_{inst}$ | $T_{inst} = 4/f_{cp}$ | 4.7 | — | 11.4 | $\mu s$ | |
| Internal Clock Operation ($R_f$ Oscillation) | | | | | | | |
| Clock Oscillation Frequency | $f_{osc}$ | $R_f = 51k\Omega \pm 2\%$ | 540 | 720 | 900 | kHz | |
| Instruction Cycle Time | $T_{inst}$ | $T_{inst} = 4/f_{osc}$ | 4.4 | 5.5 | 7.4 | $\mu s$ | |
| Internal Clock Operation (Ceramic Filter Oscillation) | | | | | | | |
| Clock Oscillation Frequency | $f_{osc}$ | Ceramic Filter Circuit | 784 | 800 | 816 | kHz | |
| Instruction Cycle Time | $T_{inst}$ | $T_{inst} = 4/f_{osc}$ | 4.9 | 5.0 | 5.1 | $\mu s$ | |

[NOTE 1]  All voltages are with respect to GND.
[NOTE 2]  This is applied to RESET, $\overline{HLT}$, $OSC_1$, $INT_0$, $INT_1$ and the With Pull up MOS or CMOS type of I/O pins.
[NOTE 3]  This is applied to the Open Drain type of I/O pins.
[NOTE 4]  This is applied to the CMOS type of I/O or Output pins.
[NOTE 5]  This is applied to the With Pull up MOS or CMOS type of I/O or Output pins.
[NOTE 6]  This is applied to the Open Drain type of I/O or Output pins.
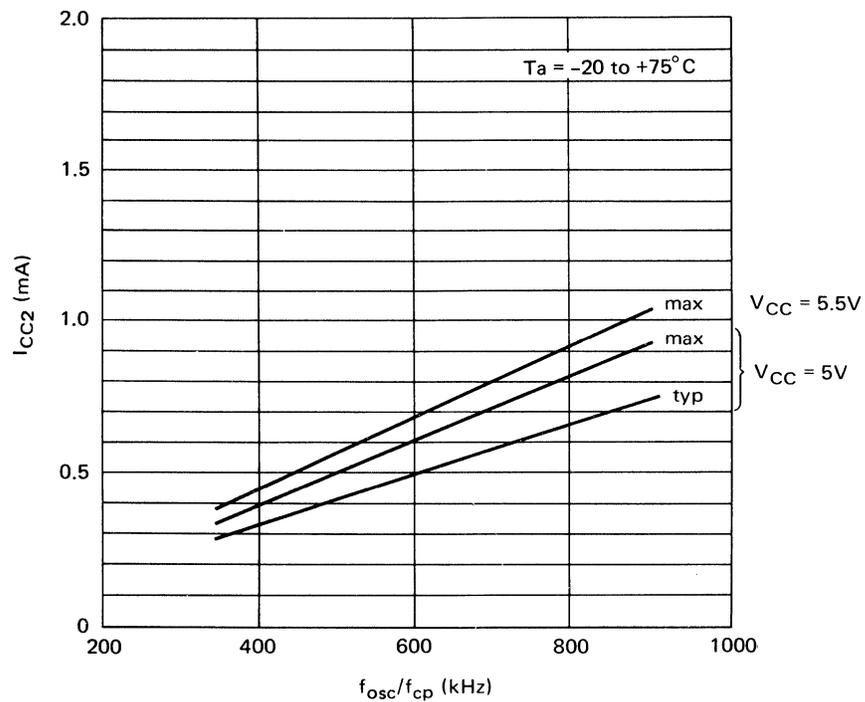[NOTE 7]  I/O current is excluded.
$I_{CC2}$ vs. $f_{osc}/f_{cp}$ and $I_{CC2}$ vs. $V_{CC}$ are shown in Figure 1.
[NOTE 8]  The Standby I/O Leakage Current is the I/O leakage current in the Halt and Disable State.
[NOTE 9]  I/O current is excluded.
The Standby Supply Current is the supply current at $V_{CC} = 5V \pm 10\%$ in the Halt State. The supply current in the case where the supply voltage falls to the Halt Duration voltage is called the Halt Current ($I_{DH}$), and it is shown in "Electrical Characteristics -2."
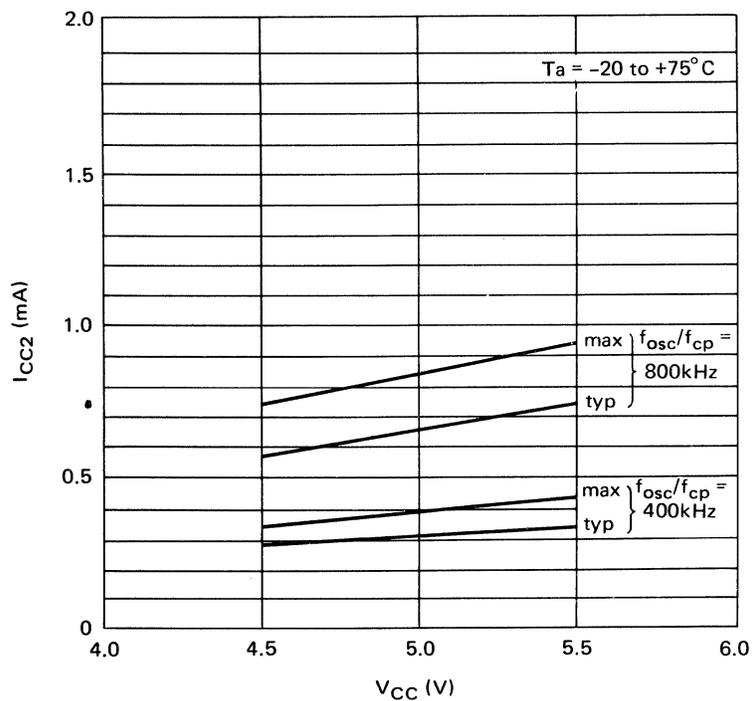
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(a)  $I_{CC2}$ vs. $f_{osc}/f_{cp}$



Ta = −20 to +75°C

$I_{CC2}$ (mA)

max    $V_{CC}$ = 5.5V

max

$V_{CC}$ = 5V

typ

$f_{osc}/f_{cp}$ (kHz)

(b)  $I_{CC2}$ vs. $V_{CC}$



Ta = −20 to +75°C

$I_{CC2}$ (mA)

max  $f_{osc}/f_{cp}$ =
     800kHz
typ

max  $f_{osc}/f_{cp}$ =
     400kHz
typ

$V_{CC}$ (V)

Figure 1  $I_{CC2}$ vs. $f_{osc}/f_{cp}$, $I_{CC2}$ vs. $V_{CC}$

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■ **ELECTRICAL CHARACTERISTICS-2** (Ta = –20°C to +75°C)

Reset and Halt

| Item | Symbol | Test Conditions | | Value | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | min | typ | max | |
| Halt Duration Voltage | $V_{DH}$ | $\overline{HLT}$ = 0.2V | | 2.3 | – | – | V |
| Halt Current | $I_{DH}$ | $V_{in} = V_{CC}$ $\overline{HLT}$ = 0.2V, $V_{DH}$ = 2.3V | | – | 2.0 | 1 2 | μA |
| Halt Delay Time | $t_{HD}$ | | | 100 | – | – | μs |
| Operation Recovery Time | $t_{RC}$ | | | 100 | – | – | μs |
| $\overline{HLT}$ Fall Time | $t_{fHLT}$ | | | – | – | 1000 | μs |
| $\overline{HLT}$ Rise Time | $t_{rHLT}$ | | | – | – | 1000 | μs |
| $\overline{HLT}$ "Low" Hold Time | $t_{HLT}$ | | | 400 | – | – | μs |
| $\overline{HLT}$ "High" Hold Time | $t_{OPR}$ | $R_f$ Oscillation, External clock operation | | 0.1 | – | – | ms |
| | | Ceramic Filter Oscillation | | 4 | – | – | |
| Power Supply Rise Time | $t_{rCC}$ | Built-in Reset $\overline{HLT}$ = $V_{CC}$ | $R_f$ Oscillation, Ceramic Filter Oscillation | 0.1 | – | 10 | ms |
| | | | External Clock Operation | 0.1 | – | 4 | |
| Power Supply OFF Time | $t_{OFF}$ | Built-in Reset $\overline{HLT}$ = $V_{CC}$ | | 1 | – | – | ms |
| RESET Pulse Width (1) | $t_{RST1}$ | External Reset $V_{CC}$ = 4.5 to 5.5V, $\overline{HLT}$ = $V_{CC}$ ($R_f$ Oscillation, External Clock Operation) | | 1 | – | – | ms |
| | | External Reset $V_{CC}$ = 4.5 to 5.5V, $\overline{HLT}$ = $V_{CC}$ (Ceramic Filter Oscillation) | | 4 | – | – | |
| RESET Pulse Width (2) | $t_{RST2}$ | External Reset $V_{CC}$ = 4.5 to 5.5V, $\overline{HLT}$ = $V_{CC}$ | | 2·Tinst | – | – | μs |

[NOTE]  All voltages are with respect to GND.

■ **SIGNAL DESCRIPTION**

The input and output signals for the HMCS47C, shown in PIN ARRANGEMENT, are described in the following paragraphs.

● **$V_{CC}$ and GND**

Power is supplied to the HMCS47C using these two pins. $V_{CC}$ is power and GND is the ground connection.

● **RESET**

This pin allows resetting of the HMCS47C at times other than the automatic resetting capability (ACL; Built-in Reset Circuit) already in the HMCS47C. The HMCS47C can be reset by pulling RESET high. Refer to RESET FUNCTION for additional information.

● **$OSC_1$ and $OSC_2$**

These pins provide control input for the built-in oscillator circuit. A resistor, ceramic filter circuit, or an external oscillator can be connected to these pins to provide a system clock with various degrees of stability/cost tradeoffs. Lead length and stray capacitance on these two pins should be minimized. Refer to OSCILLATOR for recommendations about these pins.

● **$\overline{HLT}$**

This pin is used to place the HMCS47C in the Halt State (Stand-by Mode).

The HMCS47C can be moved into the Halt State by pulling $\overline{HLT}$ low.

In the Halt State, the internal clock stops and all the internal statuses (the RAM, the registers, the Carry F/F, the Status F/F, the Program Counter, and all the internal statuses) are held.

Consequently, the power consumption is reduced. By pulling $\overline{HLT}$ high, the HMCS47C starts operation from the state just before the Halt State.

Refer to HALT FUNCTION for details of the Halt Mode.

● **TEST**

This pin is not for user application and must be connected to $V_{CC}$.

● **$INT_0$ and $INT_1$**

These pins provide the capability for asynchronously applying external interrupts to the HMCS47C.

Refer to INTERRUPTS for additional information.

● **$R_{00} - R_{03}$, $R_{10} - R_{13}$, $R_{20} - R_{23}$, $R_{30} - R_{33}$, $R_{40} - R_{43}$, $R_{50} - R_{53}$**

These 24 lines are arranged into six 4-bit Data Input/Output Common Channels.

The 4-bit registers (Data I/O Register) are attached to these channels. Each channel is directly addressed by the operand of input/output instruction. Refer to INPUT/OUTPUT for additional information.

● **$R_{60} - R_{63}$**

These 4 lines are the 4-bit Data Output Channel.

● **HITACHI**

The 4-bit register (Data I/O Register) is attached to this channel.

The channel is directly addressed by the operand of input/output instruction.

Refer to INPUT/OUTPUT for additional information.

● $D_0 - D_{15}$

These lines are 16 1-bit Discrete Input/Output Common Terminals.

The 1-bit latches are attached to these terminals. Each terminal is addressed by the Y register. The $D_0$ to $D_3$ terminals are also addressed directly by the operand of input/output instruction. Refer to INPUT/OUTPUT for additional information.

■ ROM
● ROM Address Space

ROM is used as a memory for the instructions and the patterns (constants). The instruction used in the HMCS47C consists of 10 bits. These 10 bits are called "a word", which is a unit for writing into ROM.

The ROM address has been split into two banks.

Each bank is composed of 32 pages (64 words/page).

The ROM capacity is 4,096 words (1 word = 10 bits) in all.

All addresses can contain both the instructions and the patterns (constants).

The ROM address space is shown in Figure 2.
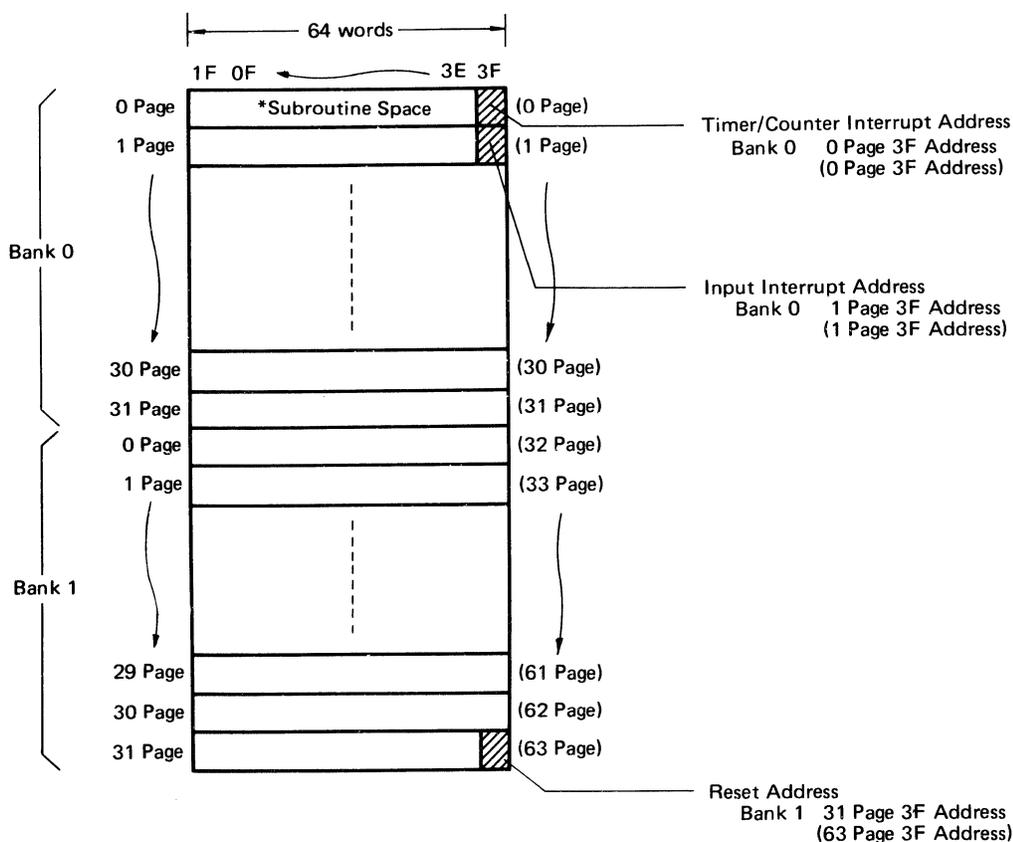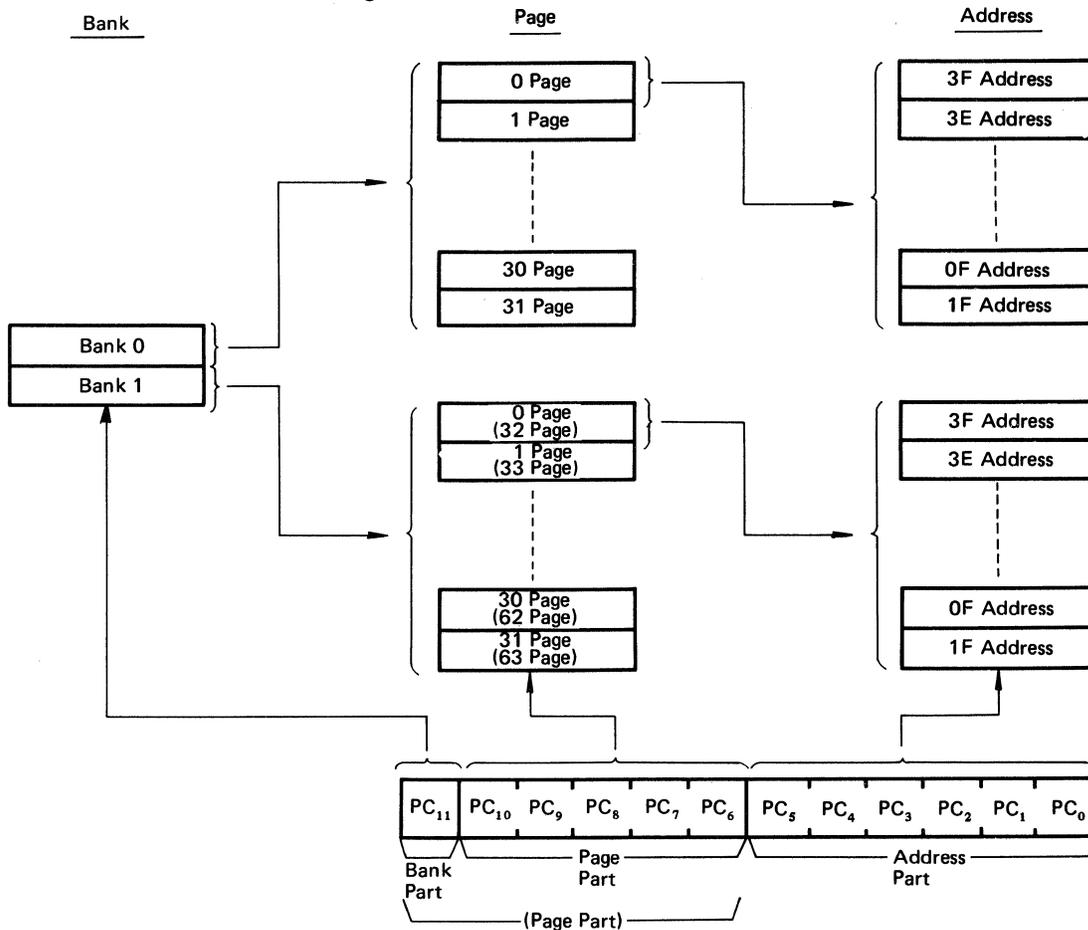


*Bank 0 0 Page (0 Page) is the Subroutine Space.

Note: The parenthesized contents are expressions of the Page, combining the bank part with the page part.

Figure 2  ROM Address Space

● **Program Counter (PC)**

The program counter is used for addressing of ROM. The program counter consists of the bank part, the page part, and the address part as show in Figure 3.



Note: The parenthesized contents are expressions of the Page, combining the bank part with the page part.

Figure 3  Configuration of Program Counter

The bank part is a 1-bit register and the page part is a 5-bit register.

Once a certain value is loaded into the bank part or the page part, the content is unchanged until other value is loaded by a program.

The settable value is "0" (the Bank 0) or "1" (the Bank 1) for the bank part, and 0 to 31 for the page part.

The address part is a 6-bit polynomial counter and counts up for each instruction cycle time. The sequence in the decimal and hexa-decimal system is shown in Table 1. This sequence is circulating and has neigher the starting nor ending point. It doesn't generate a overflow carry. Consequently, the program on a same page is executed in order unless the value of the bank part or the page part is changed.

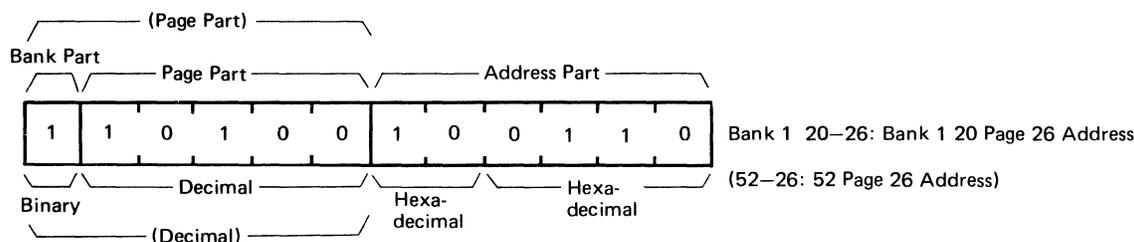Table 1  Program Counter Address Part Sequence

| Decimal | Hexa-decimal | Decimal | Hexa-decimal | Decimal | Hexa-decimal |
|---|---|---|---|---|---|
| 63 | 3F | 5 | 05 | 9 | 09 |
| 62 | 3E | 11 | 0B | 19 | 13 |
| 61 | 3D | 23 | 17 | 38 | 26 |
| 59 | 3B | 46 | 2E | 12 | 0C |
| 55 | 37 | 28 | 1C | 25 | 19 |
| 47 | 2F | 56 | 38 | 50 | 32 |
| 30 | 1E | 49 | 31 | 37 | 25 |
| 60 | 3C | 35 | 23 | 10 | 0A |
| 57 | 39 | 6 | 06 | 21 | 15 |
| 51 | 33 | 13 | 0D | 42 | 2A |
| 39 | 27 | 27 | 1B | 20 | 14 |
| 14 | 0E | 54 | 36 | 40 | 28 |
| 29 | 1D | 45 | 2D | 16 | 10 |
| 58 | 3A | 26 | 1A | 32 | 20 |
| 53 | 35 | 52 | 34 | 0 | 00 |
| 43 | 2B | 41 | 29 | 1 | 01 |
| 22 | 16 | 18 | 12 | 3 | 03 |
| 44 | 2C | 36 | 24 | 7 | 07 |
| 24 | 18 | 8 | 08 | 15 | 0F |
| 48 | 30 | 17 | 11 | 31 | 1F |
| 33 | 21 | 34 | 22 | | |
| 2 | 02 | 4 | 04 | | |

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● **Designation of ROM Address and ROM Code**

The bank part of the ROM address is shown in the binary system and the page part in the decimal system. The address part is divided into 2 bits and 4 bits, and shown in the hexa-decimal system.

It is possible to combine the bank part and the page part and show the combined part as the Page (in the decimal system).
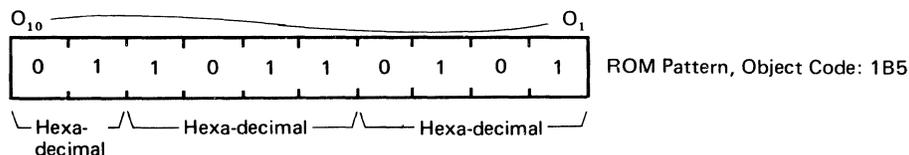
In this case, the 0 Page to the 31 Page in the Bank 1 are shown as the 32 Page to the 63 Page. The examples are shown in Figure 4.

One word (10 bits) of ROM is devided into three parts (2 bits, 4 bits and 4 bits from the most significant bit $O_{10}$ in order) shown in the hexa-decimal system. The examples are shown in Figure 4.

(a) ROM Address



Bank 1 20—26: Bank 1 20 Page 26 Address

(52—26: 52 Page 26 Address)

(b) ROM Code



ROM Pattern, Object Code: 1B5

Figure 4 Designation of ROM Address and ROM Code

■ **PATTERN GENERATION**

The pattern (constant) can be accessed by the pattern instruction (P p). The pattern can be written in any address of the ROM address space.

● **Reference**

ROM addressing for reference of the patterns is achieved by modifying the program counter with the accumulator, the B register, the Carry F/F and the operand p. Figure 5 shows how to modify the program counter. The address part is replaced with the accumulator and the lower 2 bits of B register, while the page part and the bank part are ORed with the upper 2 bits of B register, the Carry F/F and the operand p.

The value of the operand p ($p_2$, $p_1$, $p_0$) is 0 to 7 (decimal).

The bank part of the ROM address to be referenced to is determined by the logical equation: $PC_{11} + p_2$ ($p_2$ = the MSB of the operand p).

If the address where the pattern instruction exists is in the Bank 1, only the pattern of the Bank 1 can be referenced.

If the address where the pattern instruction exists is in the Bank 0, the pattern of the either Bank 1 or Bank 0 can be referenced depending on the value of $p_2$. The truth table of the bank part of the ROM address is shown in Table 2.

The value of the program counter is apparently modified and does not change actually. After execution of the pattern instruction, the program counter counts up and the next instruction is

executed.

The pattern instruction is executed in 2 instruction cycle time.

● **Generation**

The pattern of referred ROM address is generated as the following two ways:

(i) The pattern is loaded into the accumulator and B register.

(ii) The pattern is loaded into the Data I/O Registers R2 and R3.

Selection is determined by the command bits ($O_9$, $O_{10}$) in the pattern.

Mode (i) is performed when $O_9$ is "1" and mode (ii) is performed when $O_{10}$ is "1".

Mode (i) and (ii) are simultaneously performed when both of $O_9$ and $O_{10}$ are "1". The correspondence of each bit of the pattern is shown in Figure 6.

Examples of the pattern instruction is shown in Table 3.

**CAUTION**

In the program execution, the pattern can not be distinguished from the instruction. When the program is executed at the addresses into which pattern is written, the instruction corresponding to the pattern bit is executed. Take care that a pattern is not executed as an instruction.
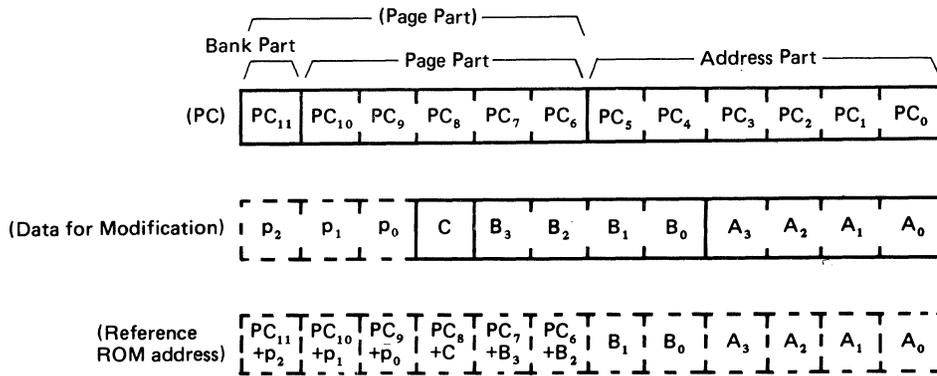
Figure 5  ROM Addressing for Pattern Generation

Table 2  Bank Part Truth Table of Pattern Generation

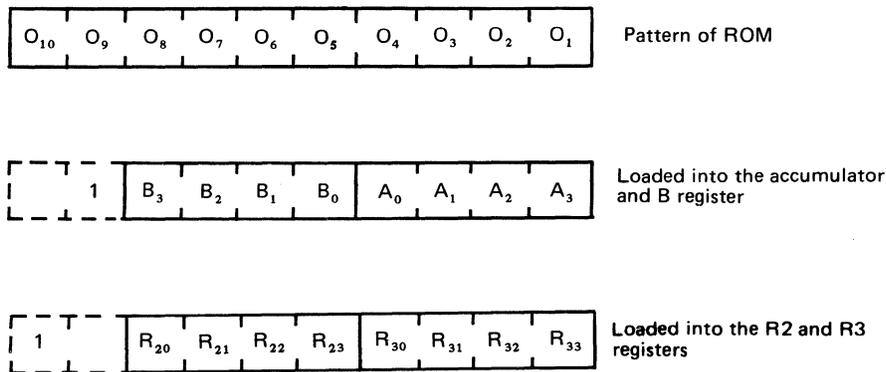| $PC_{11}$ | $P_2$ | Bank part of ROM address to be referenced to |
|---|---|---|
| 1 (Bank 1) | 1 | 1 (Bank 1) |
| | 0 | 1 (Bank 1) |
| 0 (Bank 0) | 1 | 1 (Bank 1) |
| | 0 | 0 (Bank 0) |



Figure 6  Correspondence of Each Bit of Pattern

Table 3  Example of Pattern Instructions

| Before Execution | | | | | Referred ROM Address | ROM Pattern | After Execution | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| PC | p | C | B | A | | | B | A | R2 | R3 |
| Bank 0 0-3F (0-3F) | 1 | 0 | A | 0 | Bank 0 10-20 (10-20) | 12D | 2 | B | — | —* |
| Bank 0 0-3F (0-3F) | 7 | 1 | 4 | 0 | Bank 1 29-00 (61-00) | 22D | — | — | 4 | B |
| Bank 1 30-00 (62-00) | 4 | 0/1** | 0 | 9 | Bank 1 30-09 (62-09) | 32D | 2 | B | 4 | B |
| Bank 1 30-00 (62-00) | 1 | 0/1** | F | 9 | Bank 1 31-39 (63-39) | 223 | — | — | 4 | C |

\* "—" means that the value does not change after execution of the instruction.

\*\* "0/1" means that either "0" or "1" may be selected.

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■ **BRANCH**

ROM is accessed according to the program counter sequence and the program is executed. In order to jump to any address out of the sequence, there are four ways. They are explained in the following paragraphs.

● **BR**

By BR instruction, the program branches to an address in the current page.

The lower 6 bits of ROM Object Code (operand a, $O_6$ to $O_1$) are transferred to the address part of the program counter. This instruction is a conditional instruction and executed only when the Status F/F is "1". If it is "0", the instruction is skipped and the Status F/F becomes "1". The operation is shown in Figure 7.

● **LPU**

By LPU instruction, the jump of the bank and page is performed.

The lower 5 bits of the ROM Object Code (operand u, $O_5$ to $O_1$) are transferred to the page part of the program counter with a delay of 1 instruction cycle time. At the same time, the signal $\overline{R_{70}}$ (the reversed-phase signal of the Data I/O Register $R_{70}$) is transferred to the bank part of the program counter with a delay of 1 instruction cycle time. The operation is shown in Figure 8.

Consequently, the bank and page will remain unchanged in the cycle immediately following this instruction. In the next cycle, a jump of the bank and page is achieved.

This instruction (LPU) is conditional, and is executed only when the Status F/F is "1". Even after a skip, the Status F/F will remain unchanged ("0").

LPU instruction is used in combination with BR instruction or CAL instruction as the macro instruction of BRL or CALL instruction.

● **BRL**

By BRL instruction, the program branches to an address in any bank and page.

This instruction is a macro instruction of LPU and BR instructions, which is divided into two instructions as follows.

$$\text{BRL} \quad \text{a-b} \longrightarrow \begin{array}{ll} \text{LPU} & \text{a} \\ \text{BR} & \text{b} \end{array}$$

< Jump to Bank "$\overline{R_{70}}$", a Page — b Address >

BRL instruction is a conditional instruction because of characteristics of LPU and BR instructions, and is executed only when the Status F/F is "1". If the Status F/F is "0", the instruction is skipped and the Status F/F become "1". The examples of BRL instruction are shown in Figure 9.

● **TBR (Table Branch)**

By TBR instruction, the program branches by the table.

The program counter is modified with the accumulator, the B register, the Carry F/F and the operand p.

The method for modification is shown in Figure 10.

The bank part is determined by the logical equation: $PC_{11} + p_2$, as shown in Table 4.

If the address where TBR instruction exists is in the Bank 1, a jump can be made to an address in the Bank 1 only and not to that in the Bank 0.

If the address where TBR instruction exists is in the Bank 0, a jump can be made to an address in either the Bank 1 or the Bank 0 depending on the value of the operand $p_2$.

TBR instruction is executed regardless of the Status F/F, and does not affect the Status F/F.



Figure 7  BR Operation



Figure 8  LPU Operation

Branch to Bank 0
```
• LAI    15
┌--LRA    7      R₇₀ = "1" (R̄₇₀ = "0")
└-►LPU    5  ⎫
   BR     3F ⎬  BRL 5-3F
               (Branch to Bank 0 5-3F (5-3F))

• LAI    15
  LBA
┌--LRA    7      R₇₀ = "1" (R̄₇₀ = "0")
┊ COMB
└-►LPU   31 ⎫
   BR     3F ⎬  BRL 31-3F
               (Branch to Bank 0 31-3F (31-3F))
```

Branch to Bank 1
```
• LAI     0
┌--LRA    7      R₇₀ = "0" (R̄₇₀ = "1")
└-►LPU   15 ⎫
   BR     3F ⎬  BRL 15-3F
               (Branch to Bank 1 15-3F (47-3F))

• LAI     0
  LTA
┌--LRA    7      R₇₀ = "0" (R̄₇₀ = "1")
┊ LYI     2
┊ XMA
└-►LPU   10 ⎫
   BR     2E ⎬  BRL 10-2E
               (Branch to Bank 1 10-2E (42-2E))
```

Figure 9  BRL Example

Table 4  Bank Part Truth Table of TBR Instruction

| $PC_{11}$ | $p_2$ | Bank Part of PC after TBR |
|---|---|---|
| 1 (Bank 1) | 1 | 1 (Bank 1) |
| | 0 | 1 (Bank 1) |
| 0 (Bank 0) | 1 | 1 (Bank 1) |
| | 0 | 0 (Bank 0) |

■ **SUBROUTINE JUMP**

There are two types of subroutine jumps. They are explained in the following paragraphs.

● **CAL**

By CAL instruction, subroutine jump to the Subroutine Space is performed.

The Subroutine Space is the Bank 0 0 Page (0 Page).

The address next to CAL instruction address is pushed onto the Stack ST1 and the contents of the stacks ST1, ST2 and ST3 are pushed onto the stacks ST2, ST3 and ST4 respectively as shown in Figure 11.

The bank part of the program counter becomes the Bank 0 and the page part becomes the 0 Page. The lower 6 bits (operand a, $O_6 \sim O_1$) of the ROM Object Code is transferred to the address part of the program counter.

The HMCS47C has 4 levels of stack (ST1, ST2, ST3 and ST4) which allows the programmer to use up to 4 levels of subroutine jumps (including interrupts).

CAL is a conditional instruction and executed only when the Status F/F is "1". If the Status F/F is "0", it is skipped and the Status F/F changes to "1".

● **CALL**

By CALL instruction, subroutine jump to an address in any bank and page is performed.

Subroutine jump to any address can be implemented by the subroutine jump to the page specified by LPU instruction in the bank designated by the reversed-phase signal $\bar{R}_{70}$ of the Data I/O Register $R_{70}$.

This instruction is a macro instruction of LPU and CAL instructions, which is divided into two instructions as follows

```
CALL    a-b ──────► LPU  a
                    CAL  b
```
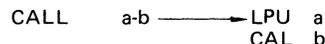
< Subroutine Jump to Bank "$\bar{R}_{70}$", a Page − b Address >

CALL instruction is conditional because of characteristic of LPU and CAL instructions and is executed when the Status F/F is "1". If the Status F/F is "0", the instruction is skipped and the Status F/F changes to "1". The examples of CALL instruction are shown in Figure 12.
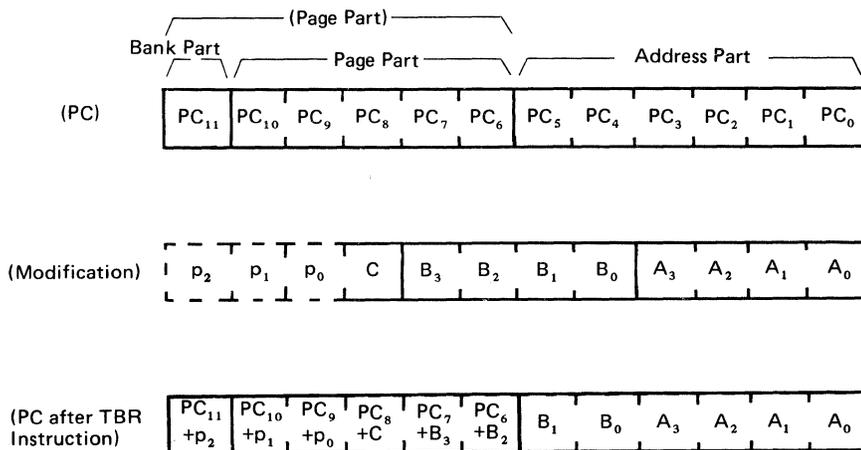


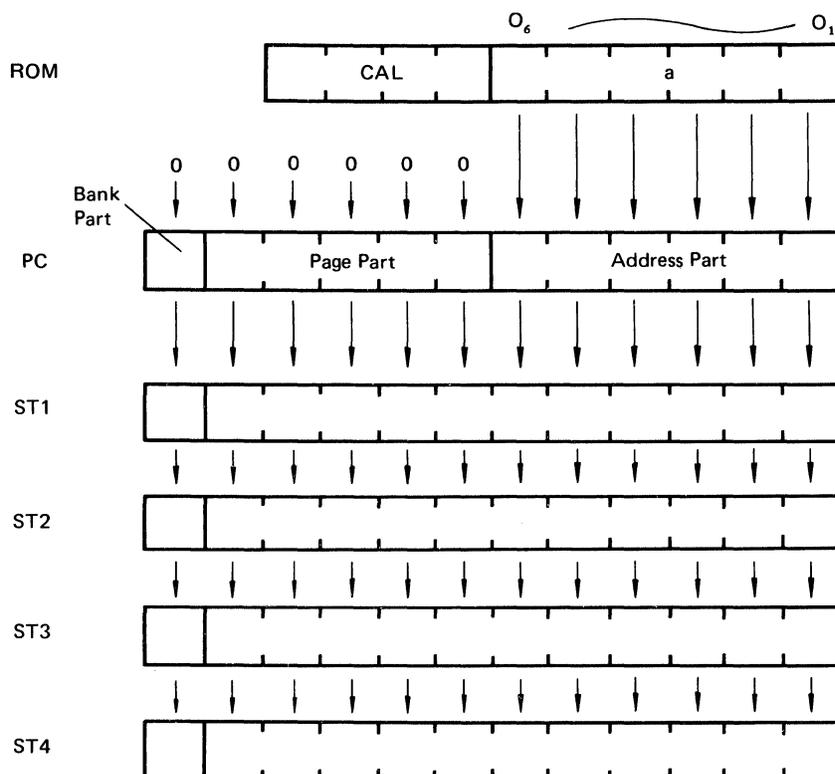Figure 10  Modification of Program Counter by TBR Instruction

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Figure 11 Subroutine Jump Stacking Order

Subroutine Jump to Bank 0
```
·  LAI    15
 ┌─LRA    7          R₇₀ = "1" (R̄₇₀ = "0")
 └►LPU    5  ⎱       CALL 5-3F
   CAL    3F ⎰       (Subroutine Jump to Bank 0 5-3F (5-3F))

·  LAI    15
   LBA
 ┌─LRA    7          R₇₀ = "1" (R̄₇₀ = "0")
 │ COMB
 └►LPU    31 ⎱       CALL 3-3F
   CAL    3F ⎰       (Subroutine Jump to Bank 0 31-3F (31-3F))
```

Subroutine Jump to Bank 1
```
·  LAI    0
 ┌─LRA    7          R₇₀ = "0" (R̄₇₀ = "1")
 └►LPU    15 ⎱       CALL 15-3F
   CAL    3F ⎰       (Subroutine Jump to Bank 1 15-3F (47-3F))

·  LAI    0
   LTA
 ┌─LRA    7          R₇₀ = "0" (R̄₇₀ = "1")
 │ LYI    3
 │ XMA
 └►LPU    10 ⎱       CALL 10-2E
   CAL    2E ⎰       (Subroutine Jump to Bank 1 10-2E (42-2E))
```

Figure 12 CALL Example

### ■ RAM

RAM is a memory used for storing data and saving the contents of the registers. Its capacity is 256 digits (1,024 bits) where one digit consists of 4 bits.

Addressing of RAM is performed by a matrix of the file No. and the digit No.

The file No. is set in the X register and the digit No. in the Y register for reading, writing or testing. Specific digits in RAM can be addressed not via the X register and Y register. These digits are called "Memory Register (MR)", 0 to 15 (16 digits in all). The memory register can be exchanged with the accumulator by XAMR m instruction.

The RAM address space is shown in Figure 13.

In an instruction in which reading from RAM and writing to RAM coexist (exchange between RAM and the register), reading precedes writing and the write data does not affect the read data.

The RAM bit manipulation instruction enables any addressed RAM bit to be set, reset or tested. The bit assignment is specified by the operand n of the instruction.

The bit test make the Status F/F "1" when the assigned bit is "1" and make it "0" when the assigned bit is "0".

Correspondence between the RAM bit and the operand n is shown in Figure 14.

|  | Y | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Y register Digit No. |
| X | f d | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| 0 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 2 | 2 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 3 | 3 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 4 | 4 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 5 | 5 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 6 | 6 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 7 | 7 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 8 | 8 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 9 | 9 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 10 | 10 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 11 | 11 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 12 | 12 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 13 | 13 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 14 | 14 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 15 | 15 | MR15 | MR14 | MR13 | MR12 | MR11 | MR10 | MR9 | MR8 | MR7 | MR6 | MR5 | MR4 | MR3 | MR2 | MR1 | MR0 |  |

X register File No.

Figure 13 RAM Address Space

Figure 14 RAM Bit and Operand n

$2^3$  $2^2$  $2^1$  $2^0$   n

0   M(0)

1   M(1)

2   M(2)

3   M(3)
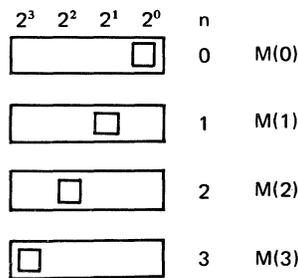
n = Bit Assignment No. (Operand)

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# ■ REGISTER

The HMCS47C has six 4-bit registers and two 1-bit registers available to the programmer. The 1-bit registers are the Carry F/F and the Status F/F. They are explained in the following paragraphs.

## ● Status F/F (S)

The Status F/F latches the result of logical or arithmetic operations (Not Zero, Overflow) and bit test operations. The Status F/F affects conditional instructions (LPU, BR and CAL instructions). These instructions are executed only when the Status F/F is "1". If it is "0", these instructions are skipped and the Status F/F becomes "1".

## ● Accumulator (A; A register) and Carry F/F (C)

The result of the Arithmetic Logic Unit (ALU) operation (4 bits) and the overflow of the ALU are loaded into the accumulator and the Carry F/F. The Carry F/F can be set, reset or tested. Combination of the accumulator and the Carry F/F can be right or left rotated. The accumulator is the main register for ALU operation and the Carry F/F is used to store the overflow generated by ALU operation when the calculation of two or more digits (4 bits/digit) is performed.

## ● B register (B)

The result of ALU operation (4 bits) is loaded into this register. The B register is used as a sub-accumulator to stack data temporarily and also used as a counter.

## ● X register (X)

The result of ALU operation (4 bits) is loaded into this register. The X register has exchangeability for the SPX register. The X register addresses the RAM file.

## ● SPX register (SPX)

The SPX register has exchangeability for the X register.

The SPX register is used to stack the X register and expand the addressing system of RAM in combination with the X register.

## ● Y register (Y)

The result of ALU operation (4 bits) is loaded into this register. The Y register has exchangeability for the SPY register. The Y register can calculate itself simultaneously with transferring data by the bus lines, which is usable for the calculation of two or more digits (4 bits/digit). The Y register addresses the RAM digit and 1-bit Discrete I/O.

## ● SPY register (SPY)

The SPY register has exchangeability for the Y register. The SPY register is used to stack the Y register and expand the addressing system of RAM and 1-bit Discrete I/O in combination with the Y register.

# ■ INPUT/OUTPUT

## ● 4-bit Data Input/Output Common Channel (R)

The HMCS47C has five 4-bit Data I/O Common Channels (R0, R1, R2, R3, R4 and R5) and one 4-bit Data Output Channel (R6).

The 4-bit registers (Data I/O Register) are attached to these channels.

Each channel is directly addressed by the operand P of input/output instruction.

The data is transferred from the accumulator and the B register to the Data I/O Registers R0 to R5 via. the bus lines. Pattern instruction enables the patterns of ROM to be loaded into the Data I/O Registers R2 and R3.

Input instruction enables the 4-bit data to be sent to the accumulator and the B register from R0 to R5. Note that, since the Data I/O Register's output is directly connected to the pin even during execution of input instruction, the input data is wired logic of the Data I/O Register's output and the pin input. Therefore, the Data I/O Register should be set to 15 (all bits of the Data I/O Register is "1") not to affect the pin input before execution of input instruction, and Open Drain or With Pull up MOS should be specified for the I/O configuration of these pins.

The block diagram is shown in Figure 15. The I/O timing is shown in Figure 16.

## ● 1-bit Discrete Input/Output Common Terminal (D)

The HMCS47C has 16 1-bit Discrete I/O Common Terminals.

The 1-bit Discrete I/O Common Terminal consists of a 1-bit latch and a I/O common pin.

The 1-bit Discrete I/O is addressed by the Y register. The addressed latch can be set or reset by output instruction and "0" and "1" level can be tested with the addressed pin by input instruction.

Note that, since the latch output is directly connected to the pin even during execution of input instruction, the input data is wired logic of the latch's output and the pin input. Therefore, the latch should be set to "1" not to affect the pin input before execution of input instruction and Open Drain or With Pull up MOS should be specified for the I/O configuration of this pin.

The $D_0$ to $D_3$ terminal are also addressed directly by the operand n of input/output instruction and can be set or reset. The block diagram is shown in Figure 17 and the I/O timing is shown in Figure 18.

## ● I/O Configuration

The I/O configuration of each pin can be specified among Open Drain, With Pull up MOS and CMOS using a mask option as shown in Figure 19.
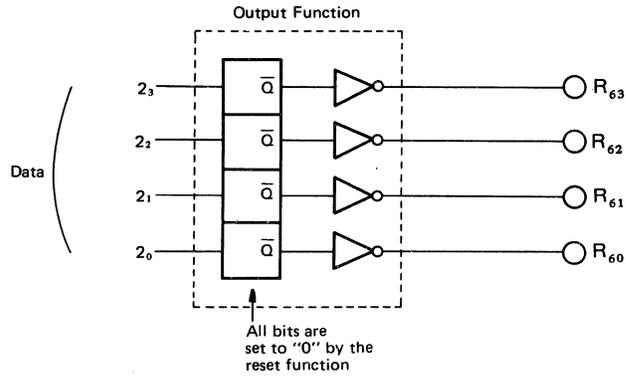
(a) R0 to R5
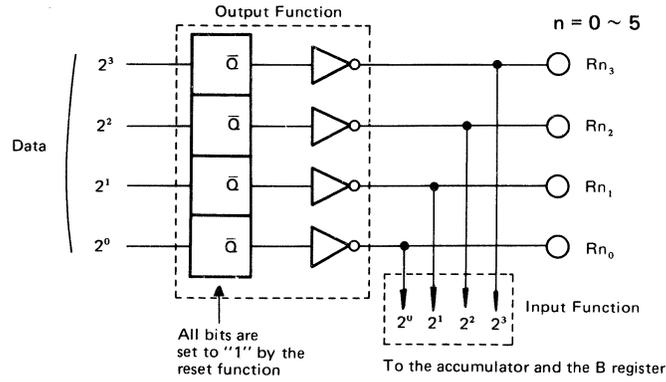


(b) R6
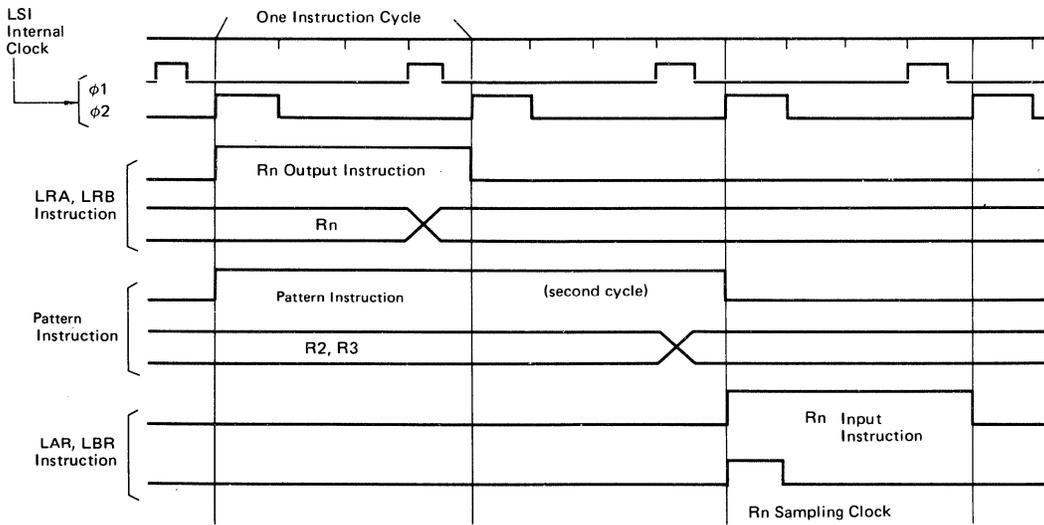


Figure 15 4-bit Data I/O Block Diagram
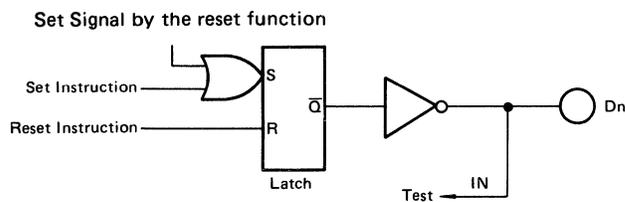


Figure 16 4-bit Data I/O Timing



Figure 17 1-bit Discrete I/O Block Diagram

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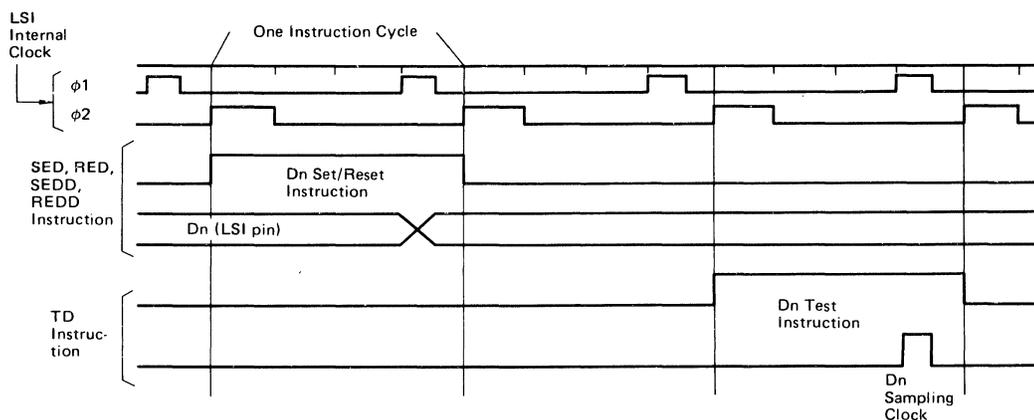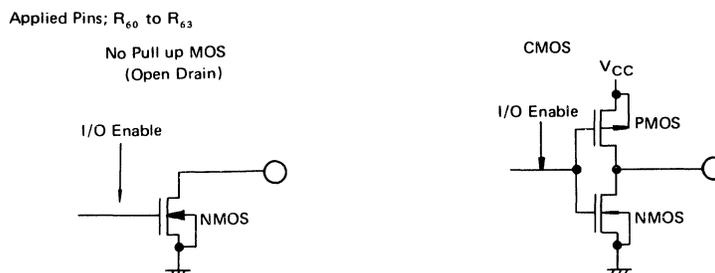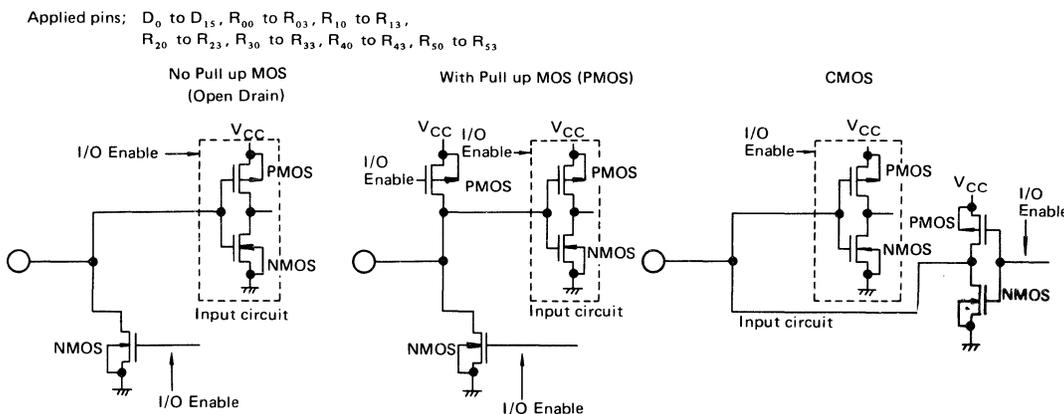Figure 18  1-bit Discrete I/O Timing

**(a)  Configuration of Output Pin**

Applied Pins; $R_{60}$ to $R_{63}$



**(b)  Configuration of I/O Pin**

Applied pins;  $D_0$ to $D_{15}$, $R_{00}$ to $R_{03}$, $R_{10}$ to $R_{13}$,
$R_{20}$ to $R_{23}$, $R_{30}$ to $R_{33}$, $R_{40}$ to $R_{43}$, $R_{50}$ to $R_{53}$



\* When "Disable" is specified for the I/O State at the Halt State,
the I/O Enable signal shown in the figure turns off the input circuit,
Pull up MOS and NMOS output and sets CMOS output to high
inpedance (PMOS, NMOS; OFF).

Figure 19  I/O Configuration

### ■ TIMER/COUNTER

The timer/counter consists of the 4-bit counter and the 6-bit prescaler as shown in Figure 20. The 4-bit counter may be loaded under program control and is incremented toward 15 by the prescaler overflow output pulse or the input pulse of $INT_1$ pin (its leading edge is counted). The clock input to the counter is selected by the CF F/F. When the CF F/F is "0", the clock input is the prescaler overflow output pulse (Timer Mode). When the CF F/F is "1", the clock input is the input pulse of $INT_1$ pin (Counter Mode). When the counter reaches zero (returns from 15 to zero), the overflow output pulse is generated and the counter continues to count ($14 \rightarrow 15 \rightarrow 0 \rightarrow 1 \rightarrow 2 \cdots$).

The TF F/F is a flip-flop which masks interrupts from the timer/counter. It can be set and reset by interrupt instruction. If the overflow output pulse of the counter is generated when the TF F/F is reset ("0"), an interrupt request occurs and the TF F/F becomes "1". If the overflow output pulse is generated when the TF F/F is set ("1"), no interrupt request occurs. The TTF instruction enables the TF F/F to be tested.

The prescaler is a 6-bit frequency divider. It divides a system clock (instruction frequency) by 64 into the overflow output pulses of "instruction frequency ÷ 64".

The prescaler is cleared when data is loaded into the counter (by LTA or LTI instruction). The frequency division is 0 when the prescaler is cleared. At the 64th clock, an overflow output

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pulse is generated from the prescaler. During operation of the LSI, the prescaler is operating and cannot be stopped. (In the Halt state, it stops.) The relation between the specified value of the counter and specified time in the Timer Mode is shown in Table 5.

The pulse width of the $INT_1$ pin in the Counter Mode must be at least 2 instruction cycle time for both "High" and "Low" levels as shown in Figure 20.

■ **INTERRUPT**

The HMCS47C can be interrupted two different ways: through the external interrupt input pins ($INT_0$, $INT_1$) and the timer/counter interrupt request. When any interrupt occurs, processing is suspended, the Status F/F is unchanged, the present program counter is pushed onto the stack ST1 and the contents of the stacks ST1, ST2 and ST3 are pushed onto the stacks ST2, ST3 and ST4 respectively, the Interrupt Enable F/F (I/E) is set, the address jumps to a fixed destination (Interrupt Address), and the interrupt routine is executed. Stacking the registers other than the program counter must be performed by the program. The interrupt routine must end with RTNI

(Return Interrupt) instruction which sets the I/E F/F simultaneously with RTN instruction.

The Interrupt Address:

Input Interrupt Address . . . . . . . . Bank 0 1 Page 3F Address
(1 Page 3F Address)

Timer/Counter Interrupt Address . . . . . . . . Bank 0 0 Page
3F Address
(0 Page 3F Address)

The input interrupt has priority over the timer/counter interrupt.

The $INT_0$ and $INT_1$ pin have an interrupt request function. Each terminal consists of a circuit which generates leading pulse and the Interrupt mask F/F (IF0, IF1). An interrupt is enabled (unmasked) when the IF0 F/F or IF1 F/F is reset. When the $INT_0$ or $INT_1$ pin changes from "0" to "1" (from "Low" level to "High" level), a leading pulse is generated to produce an interrupt request. At the same time, the IF0 F/F or IF1 F/F is set. When the IF0 F/F or IF1 F/F is set, the interrupt masking for the pin will result. (If a leading pulse is generated, no interrupt request occurs.)
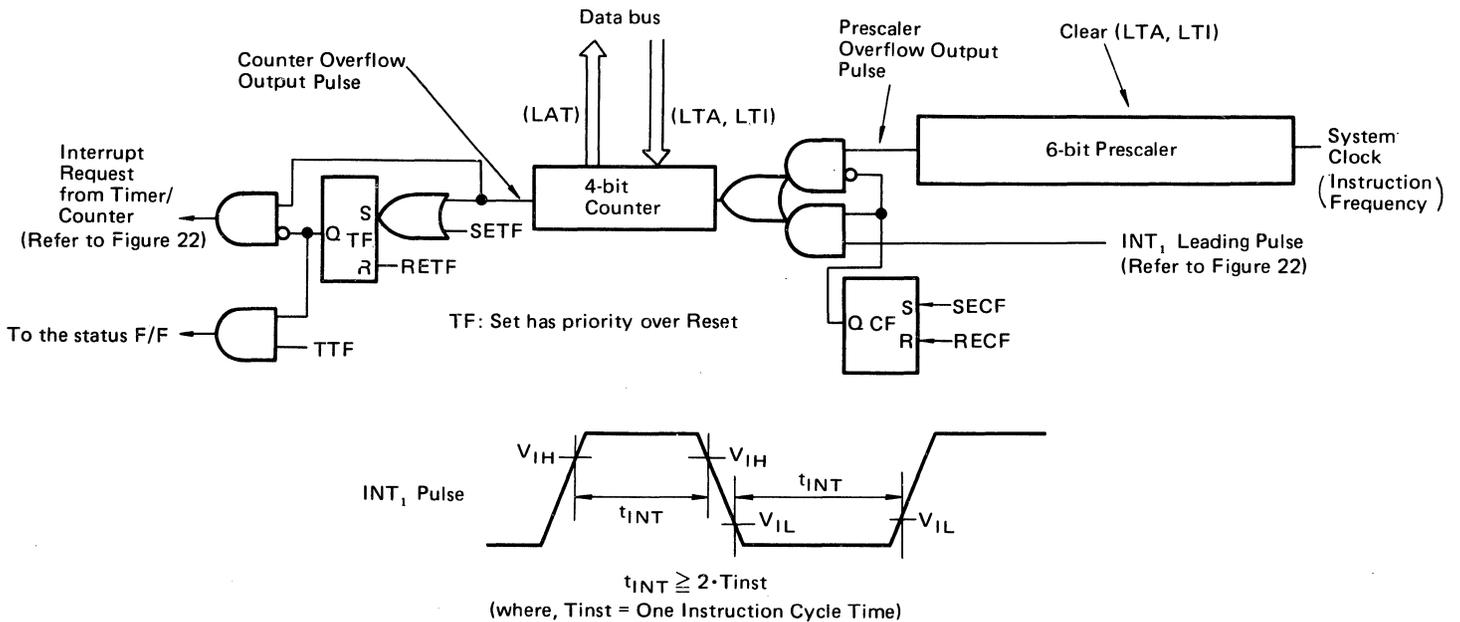
Figure 20 Timer/Counter Block Diagram

Table 5 Timer Range

| Specified Value | Number of Cycles | *Time (ms) | Specified Value | Number of Cycles | *Time (ms) |
|---|---|---|---|---|---|
| 0 | 1024 | 5.12 | 8 | 512 | 2.56 |
| 1 | 960 | 4.80 | 9 | 448 | 2.24 |
| 2 | 896 | 4.48 | 10 | 384 | 1.92 |
| 3 | 832 | 4.16 | 11 | 320 | 1.60 |
| 4 | 768 | 3.84 | 12 | 256 | 1.28 |
| 5 | 704 | 3.52 | 13 | 192 | 0.96 |
| 6 | 640 | 3.20 | 14 | 128 | 0.64 |
| 7 | 576 | 2.88 | 15 | 64 | 0.32 |

* Time is based on instruction frequency 200kHz. (One Instruction Cycle Time (Tinst) = 5μs)

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An interrupt request generated by the leading pulse is latched into the input interrupt request F/F (I/RI) on the input side. If the Interrupt Enable F/F (I/E) is "1" (Interrupt Enable State), an interrupt occurs immediately and the I/RI F/F and the I/E F/F are reset. If the I/E F/F is "0" (Interrupt Disable State), the I/RI F/F is held at "1" until the HMCS47C gets into the Interrupt Enable State.

The IF0 F/F, the IF1 F/F, the $INT_0$ pin and the $INT_1$ pin can be tested by interrupt instruction. Therefore, the $INT_0$ and the $INT_1$ can be used as additional input pins with latches.

The $INT_0$ pin and $INT_1$ pin can be provided with Pull up MOS using a mask option as shown in Figure 21.

An interrupt request from the timer/counter is latched into the timer interrupt request F/F (I/RT). The succeeding operations are same as an interrupt from the input. Only the exception is that, since an interrupt from the input precedes a timer/counter interrupt, the input interrupt occurs if both the I/RI F/F and the I/RT F/F are "1" (when the input interrupt and the timer/counter interrupts are generated simultaneously). During this processing, the I/RT F/F remains "1". The timer/counter interrupt can be implemented after the input interrupt processing is achieved.

The interrupt circuit block diagram is shown in Figure 22.
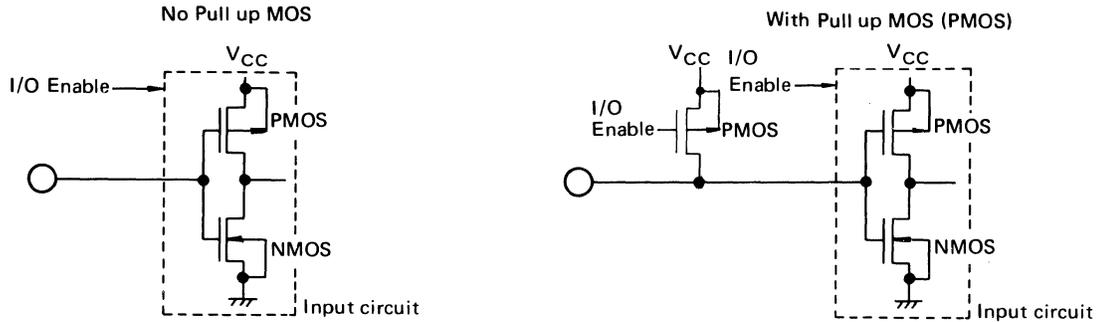


Figure 21  Configuration of $INT_0$ and $INT_1$
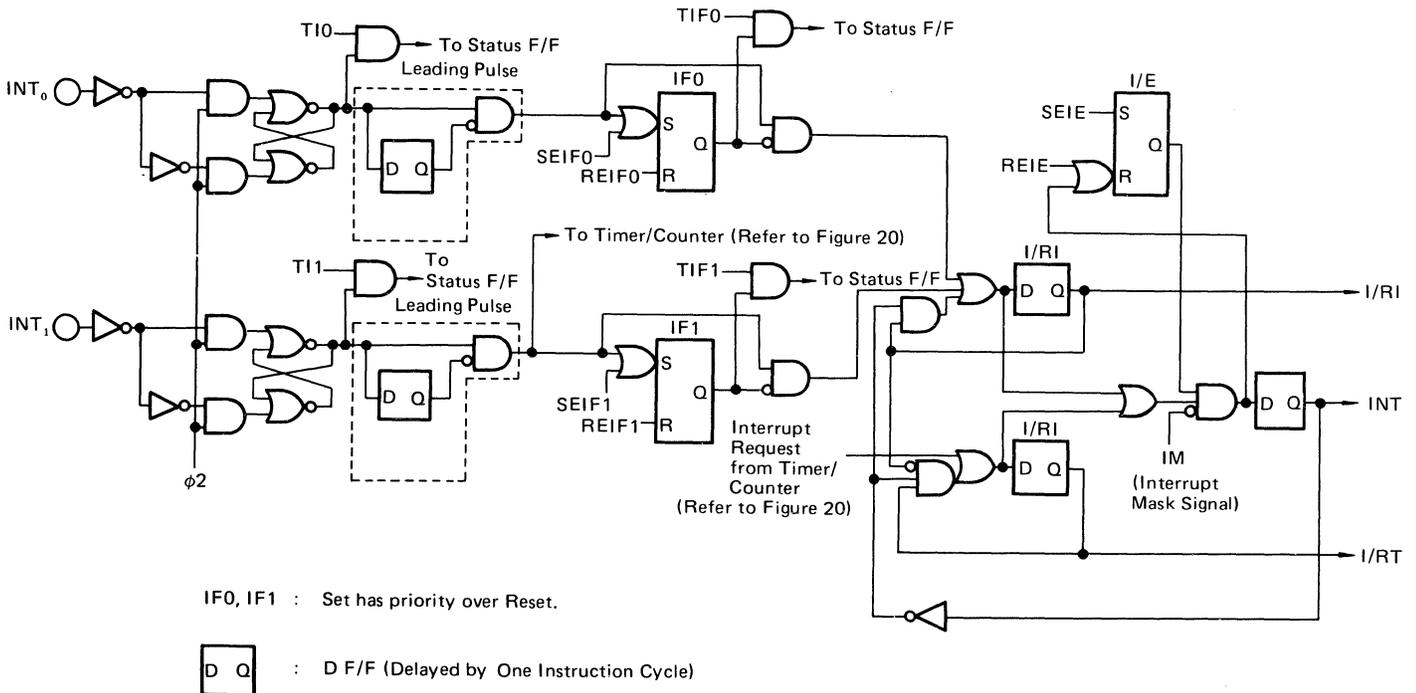


Figure 22  Interrupt Circuit Block Diagram

## ■ RESET FUNCTION

The reset is performed by setting the RESET pin to "1" ("High" level) and the HMCS47C gets into operation by setting it to "0" ("Low" level); Refer to Figure 23. Moreover, the HMCS47C has the power-on reset function (ACL; Built-in Reset Circuit). The Built-in Reset Circuit restricts the rise condition of the power supply; Refer to Figure 24. When the Built-in Reset Circuit is used, RESET should be connected to GND.

Internal state of the HMCS47C are specified as follows by the reset function.

· Program Counter (PC) is set to Bank 1 31 Page 3F Address (63 Page 3F Address).
· Data I/O Register $R_{70}$ is set to "1" (Jumps to Bank 0 by execution of LPU instruction after the reset).
· I/RI, I/RT, I/E and CF are reset to "0"
· IF0, IF1, and TF are set to "1"
· Data I/O Registers (R0 to R6) and Discrete I/O Latches ($D_0$ to $D_{15}$) are all set to "1"

> Note that all the other logic blocks (the Stack Registers, the Status F/F, the accumulator, the Carry F/F, the registers, the Timer/Counter, RAM) are not cleared by the reset function. The user should initialize these blocks by software. Because the Status F/F after the reset is not defined, set the Status F/F to "0" or "1" before the first execution of the conditional instructions (LPU, CAL and BR instructions).

## ■ HALT FUNCTION

When the HLT pin is set to "0" ("Low" level), the internal clock stops and all the internal statuses (RAM, the Registers, the Carry F/F, the Status F/F, the Program Counter, and all the internal statuses) are held. Becuase all internal logic operation stop, power consumption is reduced. There are two input/output statuses in the Halt State. The user should specify either "Enable" or "Disable" using a mask option at the time of ordering ROM.

"Enable" ─┬─ Output ....... The status before the Halt State is held.
          ├─ Pull up MOS ... ON
          └─ Input ........ Independent of the Halt State or Operating State (Input Circuit is ON)

Since Pull up MOS is ON, Pull up MOS current flows with output "0" ("Low" level) in the Halt State (NMOS: ON). When a input signal changes, transition current flows into a input circuit. Also, current flows into Pull up MOS. These



* $t_{RST1}$ includes the time required from the power ON until the operation gets into the constant state.
** $t_{RST2}$ is applied when the operation is in the constant state.

Figure 23  RESET Timing



* $t_{OFF}$ specifies the period when the power supply is OFF, when a short break of the power supply occurs and the power supply ON/OFF is repeated.
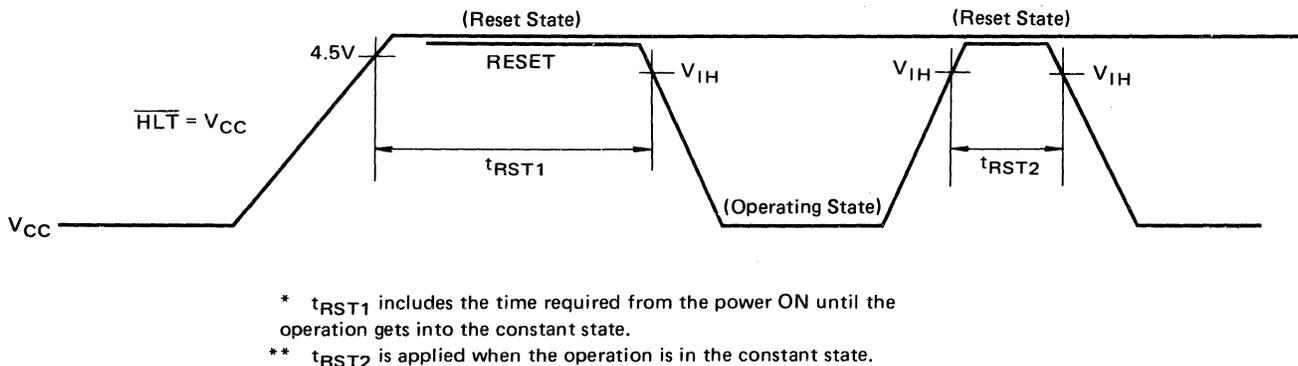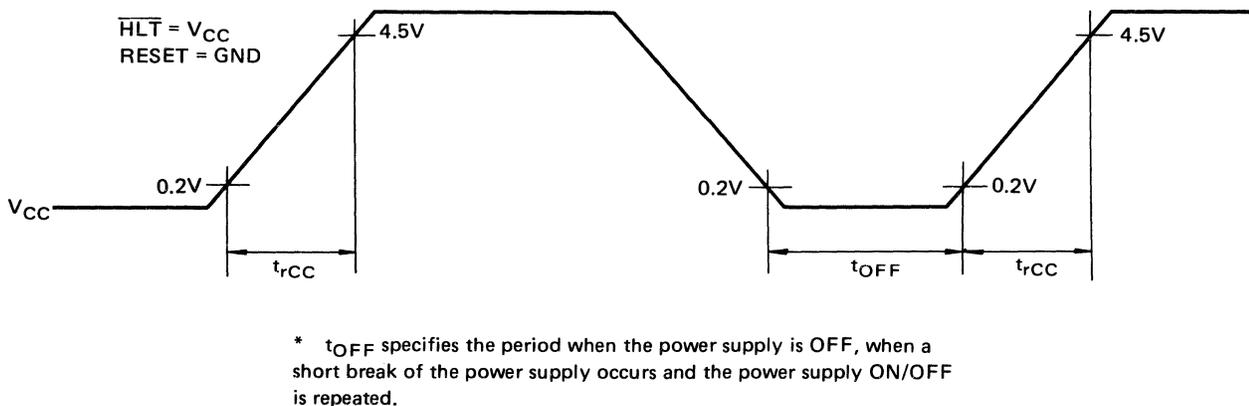
Figure 24  Power Supply Timing for Built-in Reset Circuit

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"Disable" ┬ Output ....... NMOS Output: OFF
          │                CMOS Output:
          │                  High Impedance
          │                  (NMOS, PMOS:
          │                  OFF)
          ├ Pull up MOS ... OFF
          └ Input ........ Input Circuit: OFF

currents are added to the Stand-by Supply Current (or Halt Current)

Both input and output are at high impedance state. Since a input circuit is OFF, any current other than the Stand-by Supply Current (or Halt Current) does not flow even if a input signal changes.

When the $\overline{\text{HLT}}$ pin is set to "1"("High"level), the HMCS47C gets into operation from the status just before the Halt State.

The halt timing is shown in Figure 25.

**CAUTION**

If, during the Halt State, the external reset input is applied (RESET = "1" ("High" level)), the internal status is not held.

■ **OSCILLATOR**

The HMCS47C contains its own oscillator and frequency divider (CPG). The user can obtain the desired timing for operation of the LSI by merely connecting an resistor $R_f$ or ceramic filter circuit (Internal Clock Operation). Also an external oscillator can supply a clock (External Clock Operation).

The $OSC_1$ clock frequency is internally divided by four to produce the internal system clocks.

The user may exchange the external parts for the same LSI to select either of these two operational modes as shown in Figure 26. There is no need of specifying it by using the mask option.

The typical value of clock oscillation frequency ($f_{osc}$) varies with a oscillation resistor $R_f$ as shown in Figure 27.
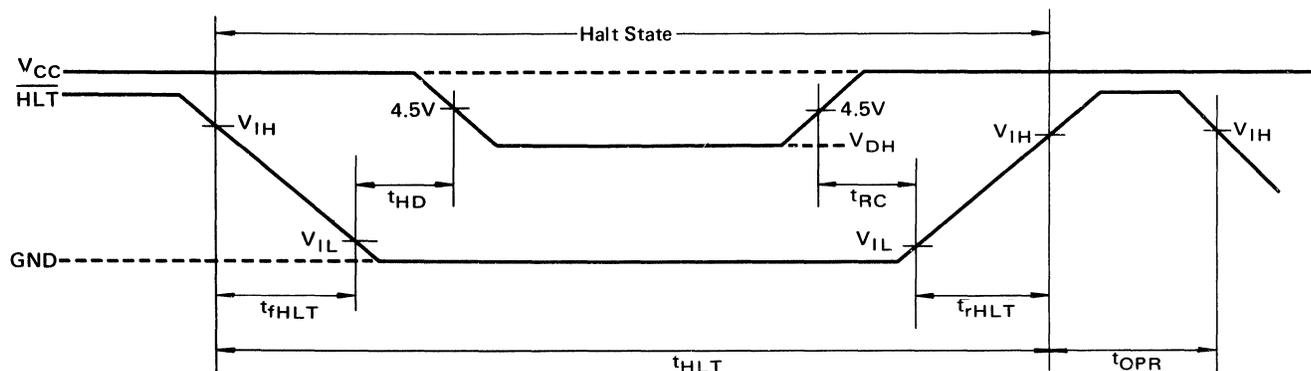


Figure 25 Halt Timing

(a) Internal Clock Operation Using Resistor $R_f$ .
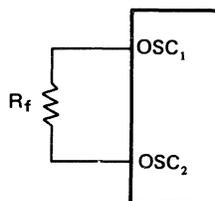


Wiring of $OSC_1$ and $OSC_2$ terminals should be as short as possible because the oscillation frequency is modified by capacitance of these terminals.

(b) Internal Clock Operation Using Ceramic Filter Circuit
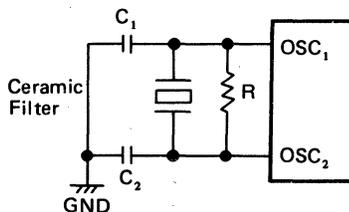


Ceramic Filter; CSB800A (MURATA)
$R_1$ ; 1MΩ ± 10%
$C_1$ ; 100pF ± 10% (Ceramic Capacitor)
$C_2$ ; 100pF ± 10% (Ceramic Capacitor)

Figure 26 Clock Operation Mode (to be continued)

(c) External Clock Operation



$$Duty = \frac{T_l}{T_h + T_l} \times 100\%$$

Figure 26  Clock Operation Mode



Figure 27  Typical Value of Oscillation Frequency vs. $R_f$

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## ■ INSTRUCTION LIST

The instructions of the HMCS47C are listed according to their functions, as shown in Table 6.

Table 6  Instruction List

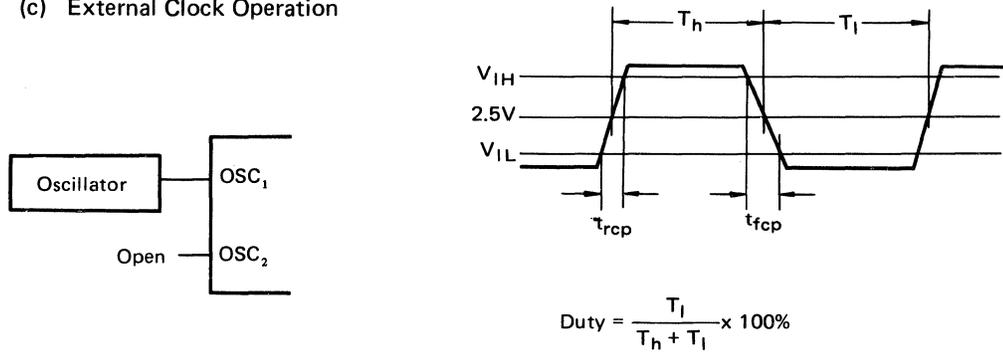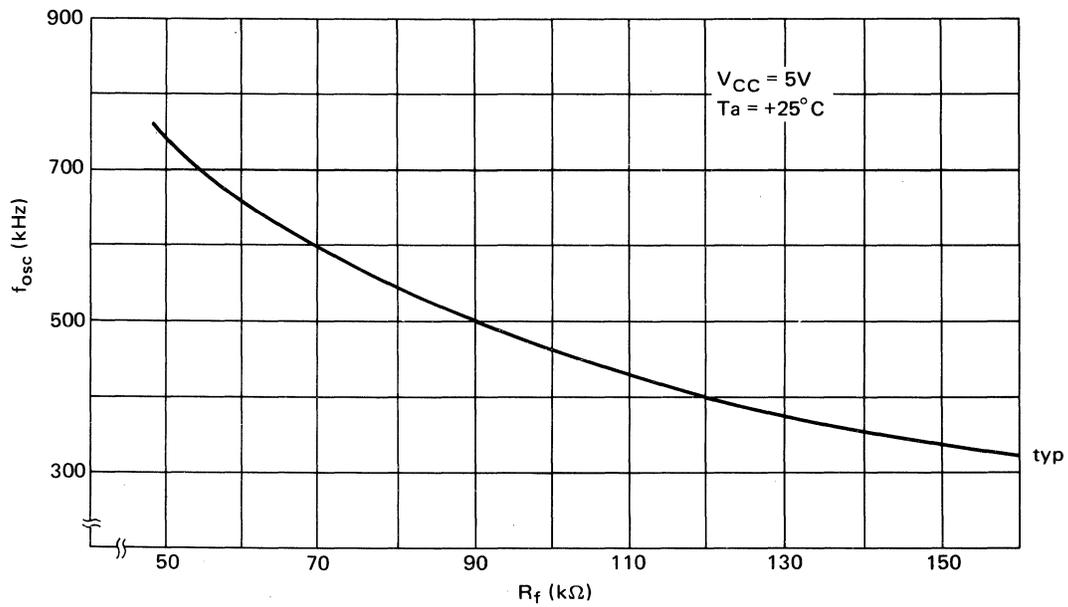| Group | Mnemonic | Function | Status |
|---|---|---|---|
| Register · Register Instruction | LAB<br>LBA<br>LAY<br>LASPX<br>LASPY<br>XAMR m | B → A<br>A → B<br>Y → A<br>SPX → A<br>SPY → A<br>A ↔ MR (m) | |
| RAM Address Register Instruction | LXA<br>LYA<br>LXI i<br>LYI i<br>IY<br>DY<br>AYY<br>SYY<br>XSPX<br>XSPY<br>XSPXY | A → X<br>A → Y<br>i → X<br>i → Y<br>Y+1 → Y<br>Y−1 → Y<br>Y+A → Y<br>Y−A → Y<br>X ↔ SPX<br>Y ↔ SPY<br>X ↔ SPX,  Y ↔ SPY | NZ<br>NB<br>C<br>NB |
| RAM · Register Instruction | LAM (XY)<br>LBM (XY)<br>XMA (XY)<br>XMB (XY)<br>LMAIY (X)<br>LMADY (X) | M → A  (XY ↔ SPXY)<br>M → B  (XY ↔ SPXY)<br>M ↔ A  (XY ↔ SPXY)<br>M ↔ B  (XY ↔ SPXY)<br>A → M, Y+1 → Y  (X ↔ SPX)<br>A → M, Y−1 → Y  (X ↔ SPX) | NZ<br>NB |
| Immediate Transfer Instruction | LMIIY i<br>LAI i<br>LBI i | i → M, Y+1 → Y<br>i → A<br>i → B | NZ |
| Arithmetic Instruction | AI i<br>IB<br>DB<br>AMC<br>SMC<br>AM<br>DAA<br>DAS<br>NEGA<br>COMB<br>SEC<br>REC<br>TC<br>ROTL<br>ROTR<br>OR | A+i → A<br>B+1 → B<br>B−1 → B<br>M+A+$\overline{\text{C}}$ (F/F) → A<br>M−A−$\overline{\text{C}}$ (F/F) → A<br>M+A → A<br>Decimal Adjustment (Addition)<br>Decimal Adjustment (Subtraction)<br>$\overline{\text{A}}$+1 → A<br>$\overline{\text{B}}$ → B<br>"1" → C (F/F)<br>"0" → C (F/F)<br>Test    C (F/F)<br>Rotation Left<br>Rotation Right<br>A ∪ B → A | C<br>NZ<br>NB<br>C<br>NB<br>C<br><br><br><br><br><br><br>C (F/F) |

| Group | Mnemonic | Function | Status |
|---|---|---|---|
| Compare Instruction | MNEI i | M $\neq$ i | NZ |
| | YNEI i | Y $\neq$ i | NZ |
| | ANEM | A $\neq$ M | NZ |
| | BNEM | B $\neq$ M | NZ |
| | ALEI i | A $\leq$ i | NB |
| | ALEM | A $\leq$ M | NB |
| | BLEM | B $\leq$ M | NB |
| RAM Bit Manipulation Instruction | SEM n | "1" $\rightarrow$ M (n) | |
| | REM n | "0" $\rightarrow$ M (n) | |
| | TM n | Test M (n) | M(n) |
| ROM Address Instruction | BR a | Branch on Status 1 | 1 |
| | CAL a | Subroutine Jump on Status 1 | 1 |
| | LPU u | Load Program Counter Upper on Status 1 | |
| | TBR p | Table Branch | |
| | RTN | Return from Subroutine | |
| Interrupt Instruction | SEIE | "1" $\rightarrow$ I/E | |
| | SEIF0 | "1" $\rightarrow$ IF0 | |
| | SEIF1 | "1" $\rightarrow$ IF1 | |
| | SETF | "1" $\rightarrow$ TF | |
| | SECF | "1" $\rightarrow$ CF | |
| | REIE | "0" $\rightarrow$ I/E | |
| | REIF0 | "0" $\rightarrow$ IF0 | |
| | REIF1 | "0" $\rightarrow$ IF1 | |
| | RETF | "0" $\rightarrow$ TF | |
| | RECF | "0" $\rightarrow$ CF | |
| | TI0 | Test $INT_0$ | $INT_0$ |
| | TI1 | Test $INT_1$ | $INT_1$ |
| | TIF0 | Test IF0 | IF0 |
| | TIF1 | Test IF1 | IF1 |
| | TTF | Test TF | TF |
| | LTI i | i $\rightarrow$ Timer/Counter | |
| | LTA | A $\rightarrow$ Timer/Counter | |
| | LAT | Timer/Counter $\rightarrow$ A | |
| | RTNI | Return Interrupt | |
| Input/Output Instruction | SED | "1" $\rightarrow$ D (Y) | |
| | RED | "0" $\rightarrow$ D (Y) | |
| | TD | Test D (Y) | D(Y) |
| | SEDD n | "1" $\rightarrow$ D (n) | |
| | REDD n | "0" $\rightarrow$ D (n) | |
| | LAR p | R (p) $\rightarrow$ A | |
| | LBR p | R (p) $\rightarrow$ B | |
| | LRA p | A $\rightarrow$ R (p) | |
| | LRB p | B $\rightarrow$ R (p) | |
| | P p | Pattern Generation | |
| | NOP | No Operation | |

[NOTE] 1. (XY) after a mnemonic code has four meanings as follows.

| | |
|---|---|
| Mnemonic only | Instruction execution only |
| Mnemonic with X | After instruction execution, X $\leftrightarrow$ SPX |
| Mnemonic with Y | After instruction execution, Y $\leftrightarrow$ SPY |
| Mnemonic with XY | After instruction execution, X $\leftrightarrow$ SPX, Y $\leftrightarrow$ SPY |

[Example] LAM M $\rightarrow$ A

LAMX M $\rightarrow$ A, X $\leftrightarrow$ SPX

LAMY M $\rightarrow$ A, Y $\leftrightarrow$ SPY

LAMXY M $\rightarrow$ A, X $\leftrightarrow$ SPX, Y $\leftrightarrow$ SPY

2. Status column shows the factor which bring the Status F/F "1" under judgement instruction or instruction accompanying the judgement.

NZ .... ALU Not Zero

C ..... ALU Overflow in Addition, that is, Carry

NB .... ALU Overflow in Subtraction, that is, No Borrow

Except above ....... Contents of the status column affects the Status F/F directly.

3. The Carry F/F (C(F/F)) is not always affected by executing the instruction which affects the Status F/F. Instruction which affect the Carry F/F are eight as follows.

| | |
|---|---|
| AMC | SEC |
| SMC | REC |
| DAA | ROTL |
| DAS | ROTR |

4. All instructions except the pattern instruction (P p) are executed in 1 instruction cycle. The pattern instruction (P p) is executed in 2 instruction cycles.

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● **HMCS47C I/O COMPOSITION TABLE**

(1) I/O Option

| LSI Type Number | HD | (To be filled by Hitachi) |
|---|---|---|
| Customer's ROM Code Name | | |
| Customer | | |

| Pin Name | I/O | I/O Option | | | Remarks |
|---|---|---|---|---|---|
| | | A | B | C | |
| $D_0$ | I/O | | | | |
| $D_1$ | I/O | | | | |
| $D_2$ | I/O | | | | |
| $D_3$ | I/O | | | | |
| $D_4$ | I/O | | | | |
| $D_5$ | I/O | | | | |
| $D_6$ | I/O | | | | |
| $D_7$ | I/O | | | | |
| $D_8$ | I/O | | | | |
| $D_9$ | I/O | | | | |
| $D_{10}$ | I/O | | | | |
| $D_{11}$ | I/O | | | | |
| $D_{12}$ | I/O | | | | |
| $D_{13}$ | I/O | | | | |
| $D_{14}$ | I/O | | | | |
| $D_{15}$ | I/O | | | | |
| $R_{00}$ | I/O | | | | |
| $R_{01}$ | I/O | | | | |
| $R_{02}$ | I/O | | | | |
| $R_{03}$ | I/O | | | | |
| $R_{10}$ | I/O | | | | |
| $R_{11}$ | I/O | | | | |
| $R_{12}$ | I/O | | | | |
| $R_{13}$ | I/O | | | | |
| $R_{20}$ | I/O | | | | |
| $R_{21}$ | I/O | | | | |
| $R_{22}$ | I/O | | | | |
| $R_{23}$ | I/O | | | | |
| $R_{30}$ | I/O | | | | |
| $R_{31}$ | I/O | | | | |
| $R_{32}$ | I/O | | | | |
| $R_{33}$ | I/O | | | | |
| $R_{40}$ | I/O | | | | |
| $R_{41}$ | I/O | | | | |
| $R_{42}$ | I/O | | | | |
| $R_{43}$ | I/O | | | | |
| $R_{50}$ | I/O | | | | |
| $R_{51}$ | I/O | | | | |
| $R_{52}$ | I/O | | | | |
| $R_{53}$ | I/O | | | | |
| $R_{60}$ | O | | ▨ | | |
| $R_{61}$ | O | | ▨ | | |
| $R_{62}$ | O | | ▨ | | |
| $R_{63}$ | O | | ▨ | | |
| $INT_0$ | I | | | ▨ | |
| $INT_1$ | I | | | ▨ | |

[NOTE] Mark a selected composition with a circle ( ○ ).

A. No Pull up MOS
B. With Pull up MOS
C. CMOS Output
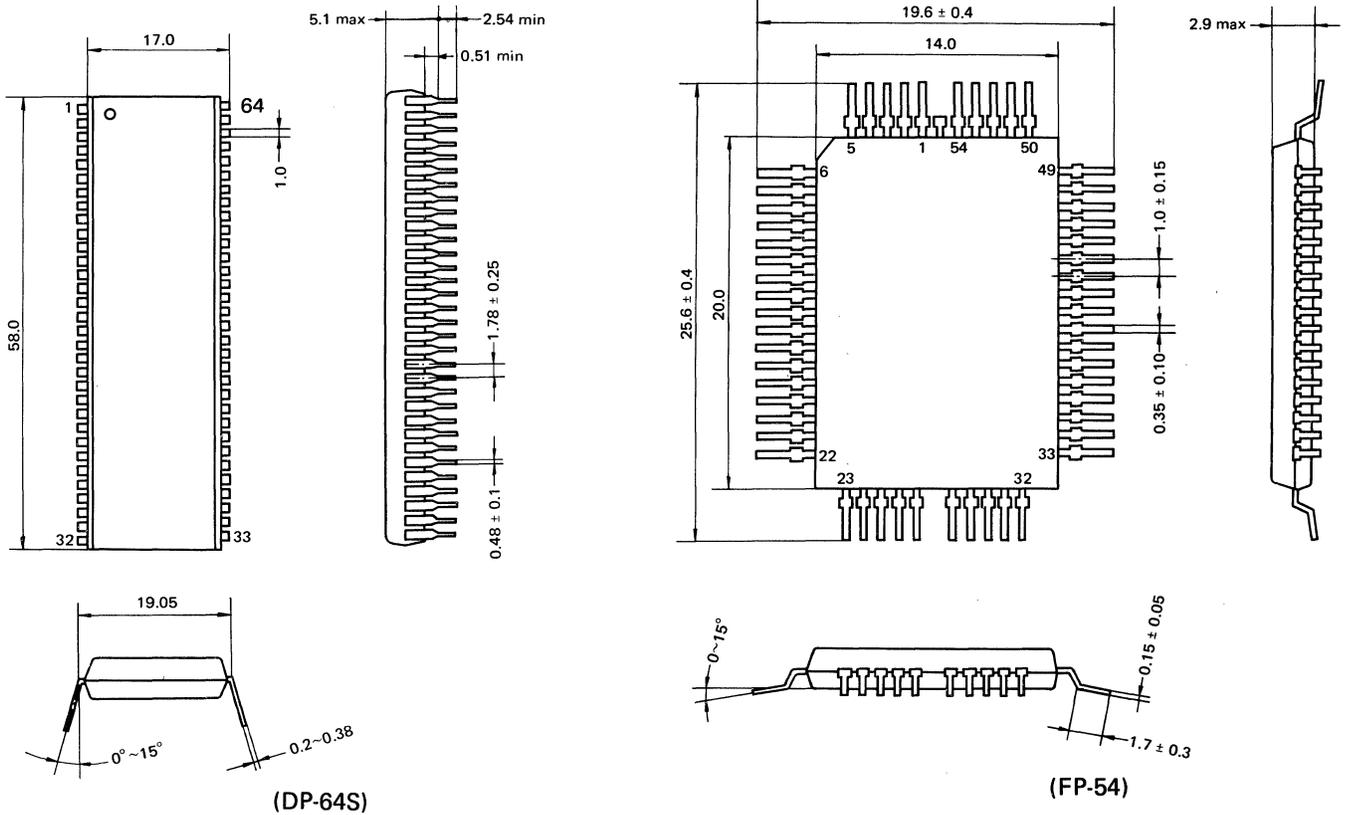
(2) I/O State at "Halt" State

| ☐ Enable | ☐ Disable |
|---|---|

[NOTE] Mark a selected I/O State with a check mark ( ✓ ).

(3) Package

| ☐ FP-54 | ☐ DP-64S |
|---|---|

[NOTE] Mark a selected package with a check mark ( ✓ ).

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■ **PACKAGE DIMENSIONS**

17.0

58.0

1

64

1.0

32

33

5.1 max

2.54 min

0.51 min

1.78 ± 0.25

0.48 ± 0.1

19.05

0° ~ 15°

0.2 ~ 0.38

**(DP-64S)**

19.6 ± 0.4

14.0

25.6 ± 0.4

20.0

5

1

54

50

6

49

22

33

23

32

1.0 ± 0.15

0.35 ± 0.10

2.9 max

0° ~ 15°

0.15 ± 0.05

1.7 ± 0.3

**(FP-54)**

(Unit: mm)

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