ICD2062B

Dual Programmable ECL/TTL Clock Generator

Single-Chip Dual Programmable Oscillator Handles All Frequency Requirements of High-Performance Graphic Systems

- 2nd Generation Dual Oscillator Graphics Clock Generator
- PECL Video Outputs: 508 KHz–165 MHz
- TTL Outputs: 508 KHz–120 MHz
- Individually Programmable Oscillators Using a Highly Reliable Manchester-Encoded 21-Bit Serial Data Word
- 2-Pin Serial Programming Interface Allows Direct Connection to Most Graphics Chip Sets with no External Hardware Required
- Programmable Video Clock Dividers Allow for Easy Interface to most RAMDACs and VRAMs
- 3-State Oscillator Control Disables Outputs for Test Purposes
- Phase-Locked Loop Oscillator Input Derived from Single 14.31818 MHz Crystal
- Sophisticated Internal Loop-Filter Requires no External Components
- Low-Power, High-Speed, 5V CMOS Technology
- Available in 20-Pin SOIC Package Configuration

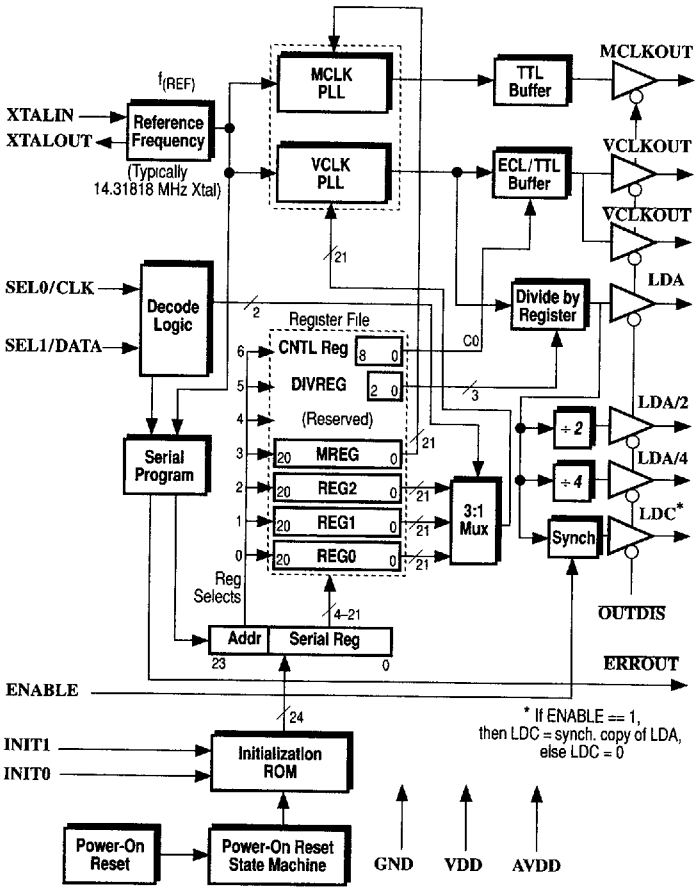

Fig. 1: ICD2062B Block Diagram

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Introduction

The ICD2062B is a clock generator for high-resolution video displays. It uses a low-frequency (and low-cost) reference crystal to produce the following: a 10 KH compatible complementary ECL oscillator signal for high-speed video RAMDACs, a high-speed TTL oscillator signal for video RAMs and system logic operation, and the requisite load, control and clock signals to control the loading of data between the CRT controller, VRAM and RAMDACs.

The ICD2062B Dual Programmable Clock Generator offers two fully user-programmable phase-locked loops in a single package. The outputs may be changed "on the fly" to any desired frequency value in the range 508 KHz to 165 MHz (VCLKOUT) and 508 KHz to 120 MHz (MCLKOUT). The ICD2062B is ideally suited for any design where multiple or varying frequencies are required, replacing more expensive metal can oscillators, particularly where the application requires expensive complementary ECL oscillators.

The Video Clock output may be programmatically divided — by 1, 2, 3, 4, 5 or 8 — in order to generate the Load Signal, which is further divided by 2 and 4 for clocking video timing logic. A second Load Signal may be synchronously gated in order to enable starting and stopping the clocking of video RAMs. The ICD2062B can also configure the pipeline delay of certain RAMDACs (such as the Bt457/458) to a fixed pipeline delay.

Being able to change the output frequency dynamically adds a new degree of freedom for the electrical engineer heretofore unavailable with existing crystal oscillator devices. Some examples of the uses for this device include: graphics board dot clocks to allow dynamic synchronization with different brands of monitors or display formats; and on-board test strategies where the ability to skew a system's desired frequency (for example: ±10%) allows worst case evaluations.

ICD2062A vs. ICD2062B

The ICD2062B revision of the ICD2062A is a complete mask redesign which includes feature enhancements as well as minor bug fixes. The following points detail the differences between the two versions:

The ICD2062B offers the following new features:

- **New VCO** — The primary difference between the A and B versions is the design of the internal VCO. The ICD2062B video VCO has been redesigned to support frequencies up to 165 MHz (see above);
- **Higher Upper Frequency Limit (VCLKOUT)** — 165 MHz;
- **New Register Initialization ROM** — A new ROM allows the ICD2062B to be initialized to higher default frequencies;
- **More Load Clock divisors** — the ICD2062B Load Clock divisors of 1, 2, 3, 4, 5 & 8.

Pin & Signal Descriptions

Fig. 2: Pin Descriptions

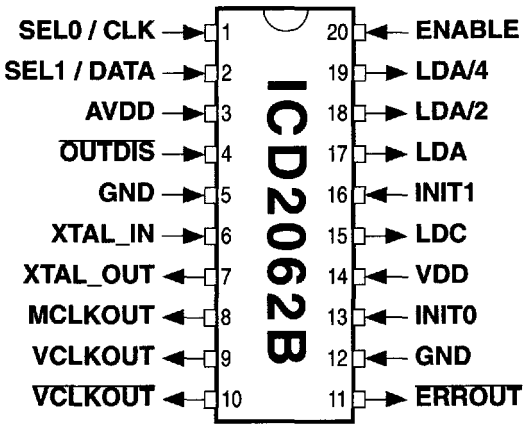

Table 1: Signal Descriptions

Pin #	Signal	Function
1	SEL0 / CLK	Bit 0 (LSB) of frequency select logic, used to select oscillator frequencies. Clock Input in serial programming mode. (Internal pull-down)
2	SEL1 / DATA	Bit 1 (MSB) of frequency select logic, used to select oscillator frequencies. Data Input in serial programming mode. (Internal pull-down)
3	AVDD	+5V to Analog Core
4	$\overline{\text{OUTDIS}}$	Output Disable (3-State Output Enable) when signal is pulled low. (Internal pull-up allows no-connect if 3-state operation not required.)
5	GND	Ground
6	XTAL_IN	Input Reference Oscillator for all Phase-Locked Loops (nominally 14.31818 MHz). An optional PC System Bus Clock signal may be used as input if available.

Table 1: Signal Descriptions (Continued)

Pin #	Signal	Function
7	XTAL_OUT	Oscillator Output to a reference Series-Resonant Crystal. For higher accuracy, a Parallel-Resonant Crystal may be used. Assume CLOAD ≈ 17pF. For more specifics on crystal requirements please refer to the IC DESIGNS Application Note *Crystal Oscillator Topics* on page 292. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.)
8	MCLKOUT	Memory Clock out
9	VCLKOUT	Differential clock output. Connect directly to RAMDAC CLOCK inputs. Can drive 4 RAMDACs.
10	$\overline{\text{VCLKOUT}}$	Output levels equivalent to 10 KH ECL circuit operating from single supply. $\overline{\text{VCLKOUT}}$ is skew-free.
11	$\overline{\text{ERROUT}}$	Error Output: a low signals an error during serial programming.
12	GND	Ground
13	INIT0	Select power-up initial conditions (LSB) (Internal pull-down)
14	VDD	+5V to I/O Ring
15	LDC	Load output (TTL compatible). When ENABLE is high, has same timing as LDA output. Can drive up to 4 capacitive loads without buffering.
16	INIT1	Select power-up initial conditions (MSB) (Internal pull-down)
17	LDA	Skew-free Load Outputs (TTL compatible). Generated by dividing VCLKOUT by Div Register (1, 2, 3, 4, 5 or 8). Each output can drive up to 4 capacitive loads without buffering.
18	LDA/2	Generated by dividing LDA by two
19	LDA/4	Generated by dividing LDA by four.
20	ENABLE	Synchronous load enable input. Internally synched to LDA, used to start/stop LDC output synchronously. If ENABLE is low, LDC is held low; when high, LDC is free-running.

Register Definitions

Register File

The Register File consists of the following registers and their selection addresses:

Table 2: Register Addressing

Address	Register	Usage
000	REG0	Video Clock Register 1
001	REG1	Video Clock Register 2
010	REG2	Video Clock Register 3
011	MREG	Memory or I/O Timing Clock
100	(Reserved)	
101	DIVREG	Load Divisor Register
110	CNTL Reg	Control Register

Register Selection

Video clock output is controlled not only by the SEL0 & SEL1 bits, but also by the $\overline{\text{OUTDIS}}$ signal, as follows:

Table 3: VCLKOUT Selection

$\overline{\text{OUTDIS}}$	SEL1	SEL0	VCLKOUT
0	X	X	High-Z
1	0	0	REG0
1	0	1	REG1
1	1	X	REG2

The Memory Clock output is controlled by the $\overline{\text{OUTDIS}}$ signal as indicated below:

Table 4: MCLKOUT Selection

$\overline{\text{OUTDIS}}$	MCLKOUT
0	High-Z
1	MREG

The Clock Select pins SEL0 & SEL1 have a dual purpose. When these pins are performing serial download, the VCLKOUT signal remains unchanged (unless the currently selected register is the one being programmed). When the pins SEL0 & SEL1 are functioning as register selects, a timeout interval is required to determine whether the user desires register select or serial programming. At the end of the timeout interval, new register selection occurs. At this point, the VCLKOUT signal will be multiplexed to the reference signal $f_{(REF)}$ for an additional timeout interval to give the VCO time to settle to its new value. (The timeout interval in both cases is approximately 5 msec — see the timeout interval spec in *Table 17: AC Characteristics* on page 189.)

When a new frequency is being set for MCLK, or if the active VCLK register is being programmed, then a glitch-free multiplexing to the Reference Frequency is performed. Once the STOP bit is sent from the MCLK or active VCLK Programming Word, the appropriate output signal will be multiplexed to the reference signal $f_{(REF)}$ for an extra timeout interval (See *Table 17: AC Characteristics* on page 189 for further details.).

Control Register Definition

The Control Register (CNTL Reg) allows the user to adjust various internal options. Most of these options are for special cases, and should have no applicability to standard graphics usage. The register word is defined as follows:

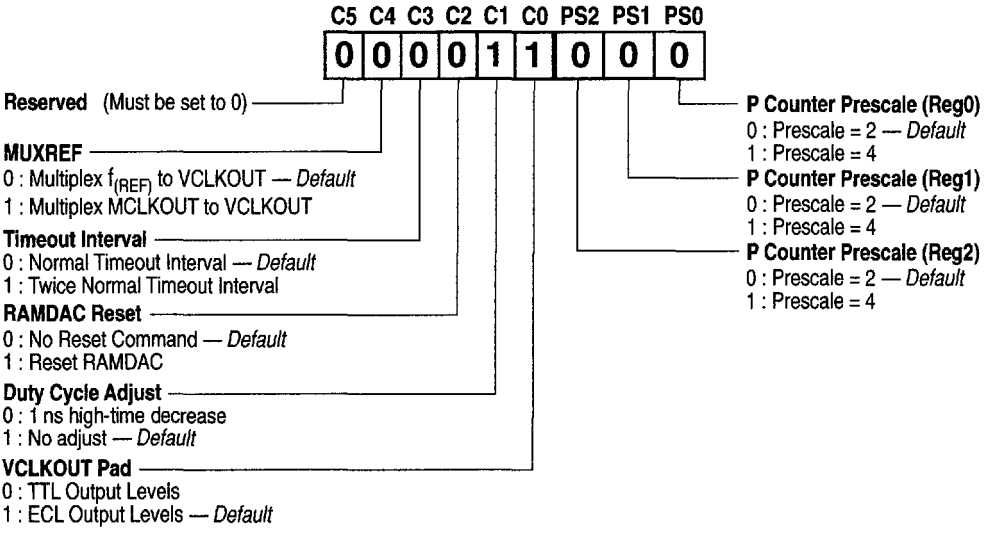

Fig. 3: Control Register

MUXREF — This control bit determines which clock is multiplexed to the VCLKOUT output during frequency changes. While the VCLK VCO changes to a different frequency, a known clock is multiplexed to the output. The default is to multiplex the $f_{(REF)}$ reference frequency, but some graphic controllers cannot run as slow as $f_{(REF)}$. This bit, when set, allows the MCLK to be used as an alternative frequency.

Timeout Interval — The Timeout Interval is normally defined as in *Table 17: AC Characteristics* on page 189. It is derived from the MCLK VCO, and if this VCO is programmed to certain extremes, the timeout may be too short. If this control bit is set, the Timeout Interval is doubled.

RAMDAC Reset — This control bit, when set, will cause the ICD2062B to issue a RAMDAC reset sequence, which is required by some specific RAMDACs (such as the Bt457/458). For more specifics on this operation, refer to the Section *Internal RESET Sequence* on page 181. NOTE: This operation will only take place the first time this bit is set.

Duty Cycle Adjust — This control bit causes a 1 ns decrease in the output waveform high time. The default is no adjustment. In situations in which the capacitive load is beyond device specifications, or where the Threshold Voltage V_{TH} is to be changed from CMOS to TTL levels, this adjustment can sometimes bring the output closer to 50% duty cycle.

VCLKOUT Pad — This control bit determines whether the VCLKOUT Pad is at ECL or TTL levels. The default is ECL levels. When in TTL mode, the VCLKOUT Pad is nonfunctional, and remains 3-stated.

P Counter Prescale (REG0, REG1, REG2) — These control bits determine whether or not to prescale the P Counter value, which allows "fine tuning" the output frequency of the respective register. Prescaling is explained in more detail elsewhere in this Datasheet.

Divide Register Definition

The output signals LDA, LDA/2, LDA/4, and LDC are all a function of the VCLK VCO value divided by the division factor stored in the Divide Register (DIVREG). The maximum LDA & LDC output is 100 MHz.

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Table 5: DIVREG Division Factors

D2	D1	D0	Division Factor	Clock Low (cycles)	Clock High (cycles)	Device Version
1	0	X	÷1	1/2	1/2	A & B
1	1	X	÷2	1	1	A & B
0	0	0	÷3	1	2	B
0	0	1	÷4	2	2	B[a]
0	1	0	÷5	2	3	B
0	1	1	÷8	4	4	B

a. Default on power-up

Register Initialization

The ICD2062B Clock Synthesizer has several of its registers in a known state upon power-up. This is implemented by the Power-On initialization circuitry. Three pixel clock registers are initialized based on the state of the INIT1 and INIT0 pins at power-up. Also, the Memory Clock is initialized based on the INIT pins.

The Power-On Reset function operates transparently to the video subsystem. It performs its initialization function and is cleared before the system Power-On Reset permits the system to begin its boot process. The INIT pins must ramp up with VDD if a 1 on either of these pins is desired. They are internally pulled down, and so will default to 0 if left unconnected.

The various registers are initialized as follows:

Table 6: Register Initialization

INIT1	INIT0	MREG	REG0	REG1	REG2
		(Frequencies in MHz)			
0	0	32.500	25.175	28.322	28.322
0	1	40.000	25.175	28.322	28.322
1	0	50.350	110.000	135.000	165.000
1	1	56.644	110.000	135.000	185.000

Serial Programming Architecture

The ICD2062B programming scheme is simple, yet impenetrable to accidental access. Because the only common denominator between most VGA and 8514 controllers is a few clock select pins, these have to perform the dual function of clock selection and serial programming. The Serial Program Block (See *Fig. 1: ICD2062B Block Diagram* on page 159) contains several components: a Serial Unlock Decoder (containing the Unlocking Mechanism and Manchester Decoder), a Watchdog Timer, the Serial Data Register (Serial Reg) and a Demultiplexer to the Register File.

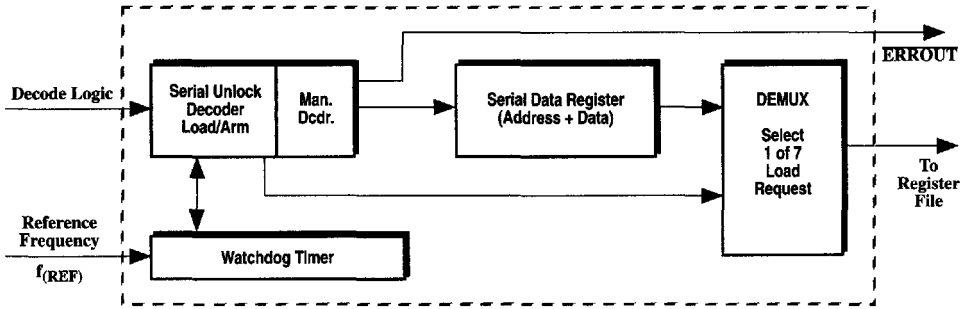


Fig. 4: Serial Program Block Diagram — Detail

Unlocking Mechanism

The Unlocking Mechanism watches for an initial break sequence detailed in the following timing diagram:

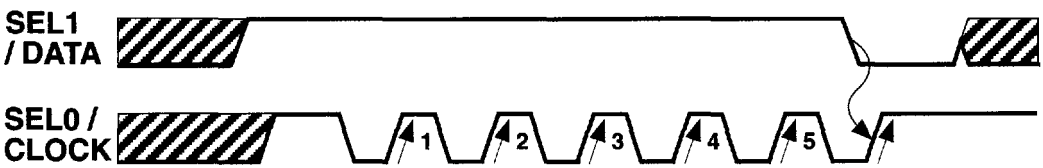


Fig. 5: Unlock Sequence

The initial unlock sequence consists of at least five low-to-high transitions of CLK with DATA high, followed immediately by a single low-to-high transition of CLK with DATA low. Following this unlock sequence, the encoded serial data is clocked into the Serial Data Register.

Watchdog Timer

Following any transition of CLK or DATA, the Watchdog Timer is reset and begins counting. Throughout the entire programming process, the Watchdog Timer ensures that there is a transition on clock or data within the timeout specification (of 2 msec — see *Table 17: AC Characteristics* on page 189). If a timeout does occur, the Lock Mechanism is rearmed and the current data in the Serial Data Register is lost.

Since the VCLK registers are selected by the SEL0 or SEL1 bits, and since any change in their state may affect the resultant output frequency, new data input on the Selection Bits is only permitted to pass through to the Decode Logic after the Watchdog Timer has timed out. This delay of SEL0 or SEL1 data permits a serial program cycle to take place without affecting the current register selection. The process of serial programming has no effect on the performance of the graphics subsystem. [Note that there is a latency amounting to the duration of the Watchdog Timer before any new VCLK register selections take effect.]

The Serial Data Register

Serial data is clocked into the Serial Data Register in the following order:

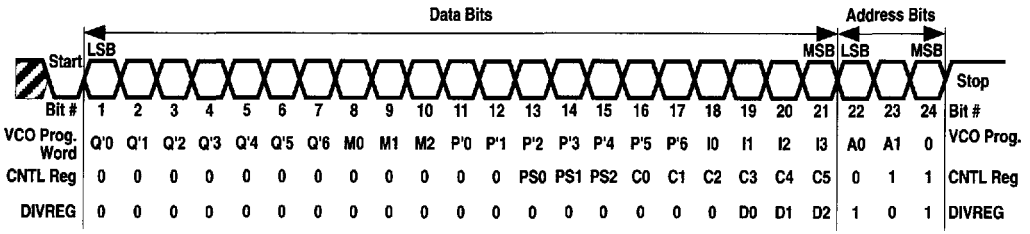


Fig. 6: Serial Data Timing

The serial data is sent using a modified Manchester encoded data format. This is defined as follows:

1 — An individual data bit is sampled on the rising edge of CLK.
2 — The complement of the data bit must be sampled on the previous falling edge of CLK.
3 — The Setup and Hold Time requirements must be met on both CLK edges.
4 — The unlock sequence, start, and stop bits are not Manchester encoded.

For specifics on timing, see *Fig. 18: Serial Programming Timing* on page 193.

The bits are shifted in this order: a start bit, 21 data bits, 3 address bits (which designate the desired register), and a stop bit (which also functions as a load strobe to transfer the data from the Serial Reg into the desired register). For the VCO registers (REG0, REG1, REG2, MREG), the data is made up of 4 fields: D[20:17] = Index; D[16:10] = P'; D[9:7] = Mux; D[6:0] = Q'. [Refer to *Programming the ICD2062B* on page 174 for more details on the VCO data word.] For the other registers having fewer

than 21 bits (DIVREG, CNTL Reg), the upper bits are used (starting with the MSB). A total of 24 bits must always be loaded into the Serial Data Register (or an error is issued). Undefined bits should be set to zero to maintain software compatibility with future enhancements.

Following the entry of the last address bit, a stop bit or Load command is issued by bringing DATA high and toggling CLK high-to-low and low-to-high. The Unlocking Mechanism then automatically rearms itself following the load. Only when the Watchdog Timer has timed out are the SEL0 & SEL1 pins permitted to return to their normal clock select function.

Note that the Serial Data Register (Serial Reg) which receives the address and data bits is exactly the correct length to accept the data being sent. The stop bit is used as a load command which passes the Serial Reg contents on to the register file location indicated by the address bits. If a stop bit is not received after the Serial Reg has been filled, but rather more valid encoded data is received, then all of the received serial data is ignored, the Unlocking Mechanism rearmed, and an error issued. The device counts the serial data clock edges to know exactly when the Serial Buffer is full, and thus to know which bit is the stop bit. Following the stop bit, the Unlocking Mechanism rearms itself. If corrupt data is detected (i.e., incorrectly Manchester-encoded data), then the Unlocking Mechanism is rearmed, the Serial Counter reset, all received data ignored, and $\overline{\text{ERROUT}}$ is asserted.

$\overline{\text{ERROUT}}$ Operation

The $\overline{\text{ERROUT}}$ signal is used to announce when a program error has been detected internally by the ICD2062B. The signal remains low until the next unlock sequence.

The following circuit shows the basic mechanism used to detect erroneous serial data:

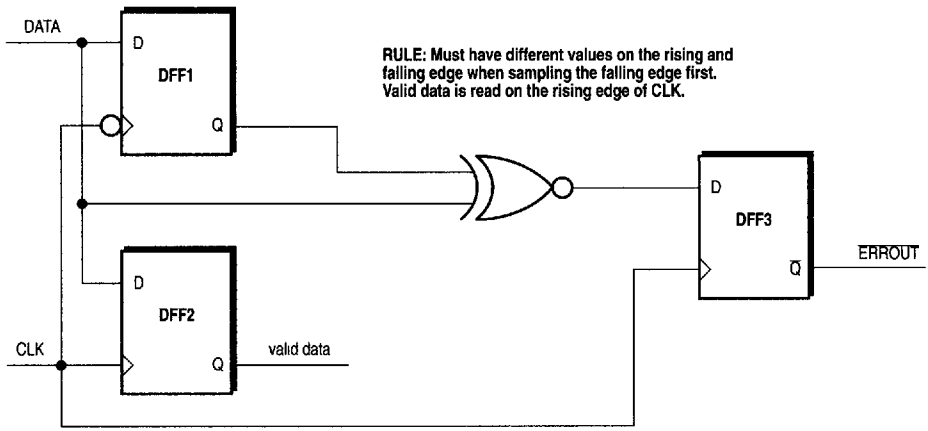


Fig. 7: Modified Manchester Decoder Circuit

The $\overline{\text{ERROUT}}$ signal is invoked for any of the following error conditions: incorrect start bit; incorrect Manchester encoding; incorrect length of data word; incorrect stop bit.

NOTE: If there is no input pin available on the target VGA controller chip to monitor $\overline{\text{ERROUT}}$, a software routine which counts VSYNC pulses to measure output frequency may be used as a determination of programming success.

Programming the ICD2062B

The desired output frequency is defined via a serial interface, with a 21–bit number shifted in. The ICD2062B has two programmable oscillators, requiring a 21-bit programming word (W) to be loaded into each channel's respective registers independently. This word contains 4 fields:

Table 7: Programming Word Bit Fields

Field	# of Bits	Notes
Index (I)	4	MSB (Most Significant Bits)
P Counter value (P')	7	
Mux (M)	3	
Q Counter Value (Q')	7	LSB (Least Significant Bits)

The frequency of the programmable oscillator $f_{(VCO)}$ is determined by these fields as follows:

$$P' = P - 3 \qquad Q' = Q - 2$$

$$f_{(VCO)} = (2 \times f_{(REF)} \times \frac{P}{Q})$$

where $f_{(REF)}$ = Reference frequency (between 1 MHz – 60 MHz; typically 14.31818 MHz).

NOTE: If a reference frequency other than 14.31818 MHz is used, then the initially loaded ROM frequencies will not be correct.

The value of $f_{(VCO)}$ must remain between a minimum and maximum frequency. These limits vary depending on the clock (MCLK or VCLK). See *Table 10: Programming Constraints* on page 177 for the actual boundary frequencies in each case. For output frequencies below the minimum, $f_{(VCO)}$ must be brought into range. To accomplish this, a post-VCO Divisor is selected by setting the values of the Mux field (M) as follows:

Table 8: Post-VCO Divisor

M	Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

The Index field (I) is used to preset the VCO to an appropriate range. The value for this field should be chosen from *Table 9: Index Field (I)* on page 176. (Note that this table is referenced to the VCO frequency, $f_{(VCO)}$, rather than to the desired output frequency.) Note that VCLK may be shut off, but that MCLK must be left running. When the Index Field is programmed to **1111**, VCLK is turned off and both channels run from the same MCLK VCO.

When the Index Field is set to **1111**, VCLK is turned off and both channels run from the same MCLK VCO. To reduce jitter, one doesn't want the two VCOs to run at integral multiples of each other; therefore, if one does want the clocks to run at 2^n (n = 0, 1, 2 .. 7) multiples of each other, this is done by turning off the VCLK VCO and multiplexing the MCLK VCO over to VCLKOUT, dividing down to the desired frequency. This will significantly reduce heterodyne jitter.

Table 9: Index Field (I)

I	VCLK f_{VCO} (MHz)	MCLK f_{VCO} (MHz)
0000	65.0 – 70.7	• Reserved •
0001	70.7 – 77.8	52.0 – 55.0
0010	77.8 – 85.6	55.0 – 60.0
0011	85.6 – 88.0	60.0 – 68.0
0100	88.0 – 94.2	68.0 – 70.0
0101	94.2 – 96.8	70.0 – 75.0
0110	96.8 – 106.5	75.0 – 80.0
0111	106.5 – 111.7	80.0 – 84.5
1000	111.7 – 117.2	84.5 – 90.0
1001	117.2 – 122.8	90.0 – 95.0
1010	122.8 – 135.1	95.0 – 100.0
1011	135.1 – 148.6	100.0 – 104.0
1100	148.6 – 160.0	104.0 – 110.0
1101	160.0 – 165.0	110.0 – 120.0
1110	Turn off VCLK	110.0 – 120.0
1111	Mux MCLK > VCLK	110.0 – 120.0

If the desired VCO frequency lies on a boundary in the table — in other words, if it is exactly the upper limit of one entry and the lower limit of the next — then either index value may be used (since both limits are tested), but we recommend using the higher one.

To assist with these calculations, IC DESIGNS provides ***BitCalc*** (Part #ICD/BCALC), a Windows™ program which automatically generates the appropriate programming words from the user's reference input and desired output frequencies, as well as assembling the program words for such things as control and power-down registers. For Macintosh or DOS environments, please ask about availability. Please specify disk size (5" or 3") when ordering ***BitCalc***.

Programming Constraints

There are five primary programming constraints the user must be aware of:

Table 10: Programming Constraints

Parameter	Minimum	Maximum
$f_{(REF)}$	1 MHz	60 MHz
$f_{(REF)} \div Q$	200 KHz	1 MHz
$f_{(VCO)}$	VCLK: 65 MHz MCLK: 52 MHz	VCLK: 165 MHz MCLK: 120 MHz
Q	3	129
P	4	130

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability, and factors affecting the loop equation. The factors are listed here for completeness' sake; however, by using the aforementioned ***BitCalc*** program, these constraints become transparent.

Programming Example — Prescaling = 2 (default)

The following is an example of the calculations ***BitCalc*** performs:

For the ICD2062B, derive the proper programming word for a 39.5 MHz VCLK output frequency, using 14.31818 MHz as the reference frequency:

Since 39.5 MHz < 52 MHz, double it to 79.0 MHz. Set M to **001**. Set I to **0010**. The result:

$$f_{(VCO)} = 79.0 = (2 \times 14.31818 \times \frac{P}{Q})$$

$$\frac{P}{Q} = 2.7857$$

Several choices of P and Q are available:

Table 11: P & Q Value Pairs

P	Q	f_{VCO} (MHz)	Error (ppm)
69	25	79.0363	460
80	29	78.9969	40
91	33	78.9669	419

Choose (P, Q) = (80,29) for best accuracy (40 ppm).

Therefore:

$$\mathbf{P' = P-3 = 80-3 = 77 = 1001101}\ (4dH)$$

$$\mathbf{Q' = Q-2 = 29-2 = 27 = 0011011}\ (1bH)$$

and the full programming word, W, is:

$$\mathbf{W = I, P', M, Q' = 0010,1001101,001,0011011 = 00101001101001011011}\ (05349bH)$$

The programming word W is then sent as a serial bit stream, LSB first. Appropriate address bits and start & stop bits must also be included as defined in the section *Serial Programming Architecture* on page 171.

Programming Example — Prescaling = 4

Assume the desired VCLKOUT frequency is 100 MHz. The table below compares the results of using the default prescaling value of 2 and the optional prescaling value of 4:

Table 12: Prescale Values

Prescale	Actual Frequency (MHz)	P	Q	Error (ppm)
2	99.84028	129	37	1600
4	99.99998	110	63	0

But this precision has its price, namely that the user now has to set and reset the Prescale Bits PS0–2 (corresponding to REG0–2) — which involves loading a Control Word (taking care to preserve the current values of the other Control Bits) — before the VCO Program Word can be loaded. Once the appropriate Prescale Bits are set, then frequency programming can proceed as before, unless and until it is desired to program a new frequency without prescaling, at which point a new Control Word must first be loaded with the proper bits set, and observing the precautions noted above.

To summarize, the sequence is:

1. Set the Prescale Bits (load a Control Word)
2. Program the VCO (load a Program Word)

Note: Care must be taken not to change the Prescale Bit of the currently active register: the results will be unpredictable at best, and it could cause the VCO to go out of lock.

RAMDAC/VRAM Interface

Interfacing to the RAMDAC

The figure below shows how to interface the ICD2062B to a RAMDAC. The part should be located as close to the RAMDAC as possible. Termination resistors are needed on the VCLKOUT outputs, and should be located as close as possible to the RAMDAC. For specific information, please refer to the IC DESIGNS Application Note *ECL Outputs* on page 289.

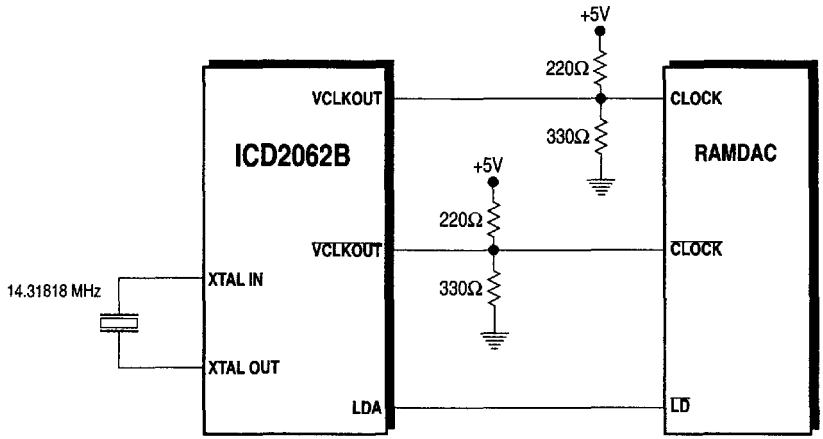


Fig. 8: ICD2062B to RAMDAC Interface Example

The ICD2062B may drive the CLOCK inputs of up to four RAMDACs, if they are located physically adjacent to each other. In this case, only 2 sets of termination resistors should be used, and these should be located nearest the farthest RAMDAC from the ICD2062B.

Typical ICD2062B Usage

The DIVREG Register holds the divisor, which can be 1, 2, 3, 4, 5 or 8, by which the pixel clock is divided to generate the load signals: LDA, LDA/2 and LDA/4.

The ENABLE input is synchronized internally to LDA; it may be used to start and stop the LDC output synchronously. When ENABLE is low, LDC is held low. When ENABLE is high, then LDC will be free-running and in phase with LDA. This allows the video DRAM shift registers to be non-clocked during the retrace intervals.

NOTE: For fanouts > 4, LDC needs to be buffered.

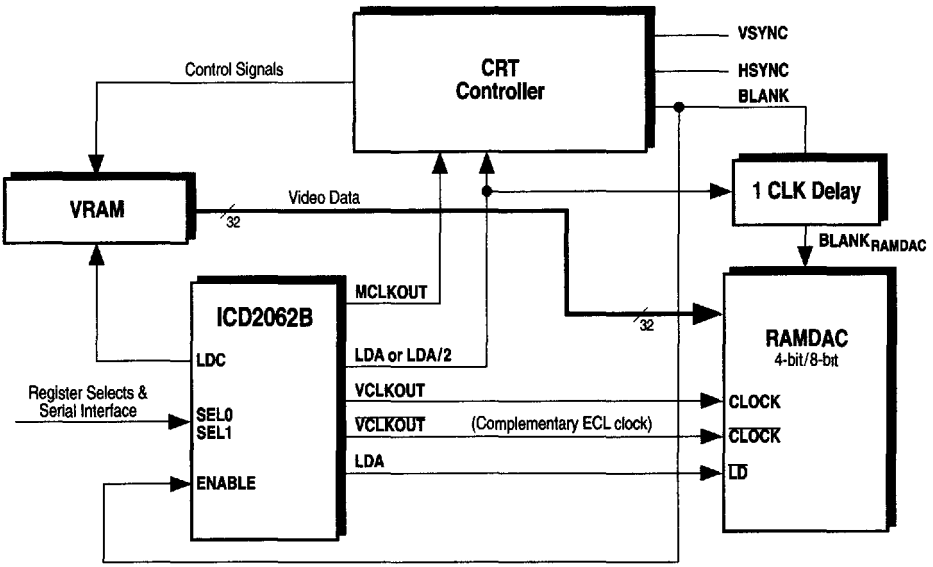


Fig. 9: ICD2062B Typical Interface Circuit

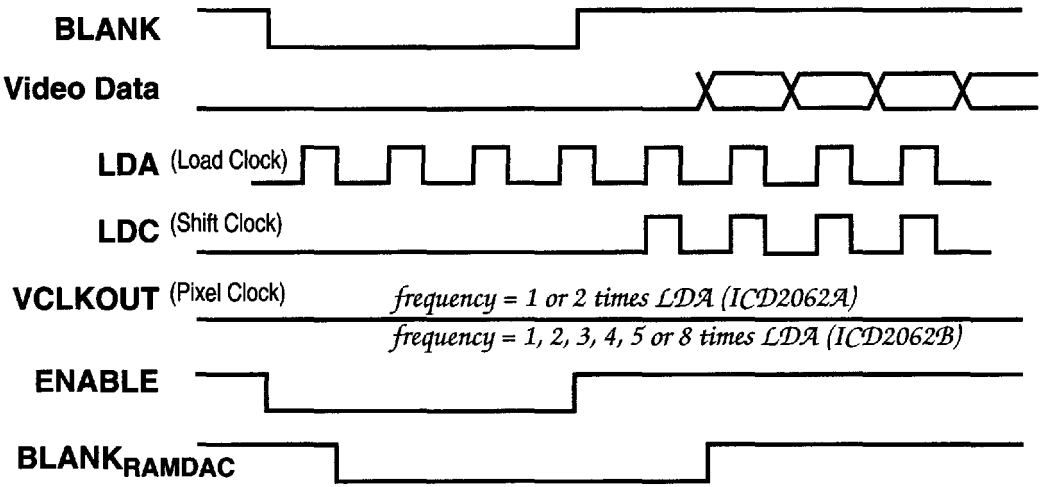


Fig. 10: Timing Diagram for Interface Circuit

Internal RESET Sequence

The internal RESET signal allows the ICD2062B to set the RAMDAC pipeline delay to a specific cycle count, depending on the RAMDAC. Reset takes place the first time the CNTL Register's Reset Bit is set. Following the rising edge of LDA/4 after the Reset Bit is set, the VCLKOUT and $\overline{\text{VCLKOUT}}$ outputs are stopped high and low, respectively; at the next rising edge of LDA/4, these outputs are again allowed to be free-running. The figure below shows the operation of the internal RESET signal:

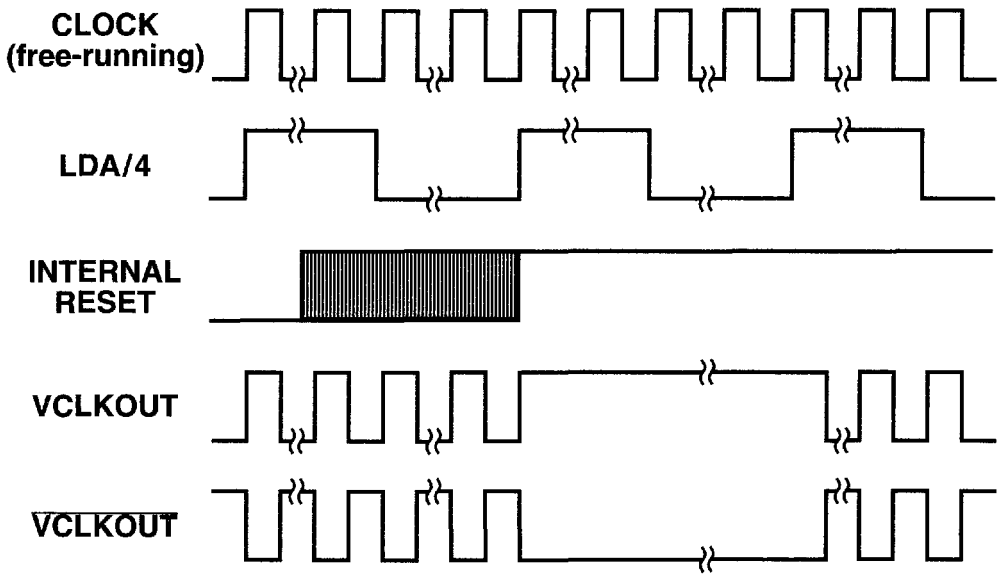


Fig. 11: Internal RESET Timing

Power Management Issues

Estimating Total Current Drain

Actual current drain is a function of frequency and of circuit loading. The operating current of a given output is given by the equation: $I = C \cdot V \cdot f$, where:

I = current,

C = load capacitance (max. 25pF),

V = output voltage (usually 5V for TTL pads, 1.5V for ECL pads), and

f = output frequency (in MHz).

To calculate total operating current, sum the following:

MCLKOUT	$\Rightarrow$	$C \cdot V \cdot f_{(MCLKOUT)}$
VCLKOUT	$\Rightarrow$	$C \cdot V \cdot f_{(VCLKOUT)}$; (ECL pad, V = 1.5V)
$\overline{\text{VCLKOUT}}$	$\Rightarrow$	$C \cdot V \cdot f_{(\overline{VCLKOUT})}$; (ECL pad, V = 1.5V)
LDA	$\Rightarrow$	$C \cdot V \cdot f_{(LDA)}$
LDA/2	$\Rightarrow$	$C \cdot V \cdot f_{(LDA/2)}$
LDA/4	$\Rightarrow$	$C \cdot V \cdot f_{(LDA/4)}$
LDC	$\Rightarrow$	$C \cdot V \cdot f_{(LDC)}$
Internal	$\Rightarrow$	12 mA

This gives an approximation of the actual operating current. For unconnected output pins, one can assume 5–10pF loading, depending on package type.

Typical values:

Table 13: Typical Current Drain Values

Frequency	Capacitive Load	Current (mA)
low	low	15
high	low	50
high	high	100

Circuit Operation

Circuit Description

The ICD2062B is designed to use an inexpensive TTL crystal and to generate the high-frequency ECL clock signals required by RAMDACs. The VCLKOUT and $\overline{\text{VCLKOUT}}$ signals interface directly with the RAMDAC CLOCK and $\overline{\text{CLOCK}}$ inputs. Output levels of the complementary ECL pads are compatible with 10 KH ECL circuitry operating from a single +5V power supply.

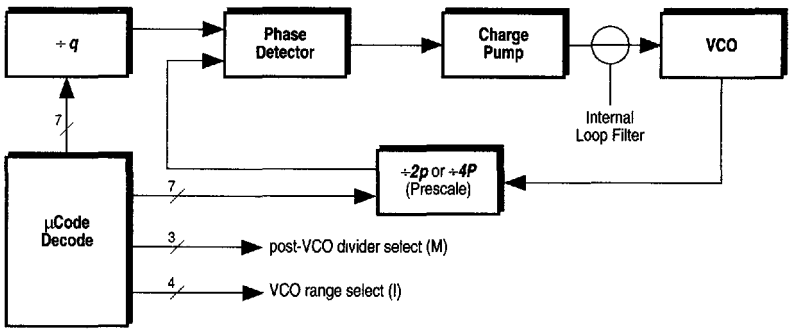


Fig. 12: Phase-Locked Loop Oscillator

Each oscillator block is a classical phase-locked loop connected as shown above. The external input frequency $f_{(REF)}$ goes into a divide-by-n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase matches the reference signal and the variable synthesized signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO either to go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up and down movement of the variable frequency will quickly lock on to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal loop filter provides stability and damping.

Stability and "Bit-Jitter"

The long-term frequency stability of the IC DESIGNS phase-locked loop frequency synthesis components is good due to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices is affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short-term stability (also called "bit-jitter") is a manifestation of the frequency synthesis process. The IC DESIGNS frequency synthesis parts have been designed with an emphasis on reduction of bit-jitter. The primary cause of this phenomenon is the "dance" of the VCO as it strives to maintain lock. Low-gain VCOs and sufficient loop filtering are design elements specifically included to minimize bit-jitter. The IC DESIGNS families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough to be acceptable for graphic designs.

Frequency Range

The frequency ranges for the video and memory clock outputs are as follows:

VCLKOUT: 508 KHz – 185 MHz

MCLKOUT: 508 KHz – 120 MHz

Output Disable

When the $\overline{\text{OUTDIS}}$ pin is asserted (active low), all the output pins except XTAL OUT and $\overline{\text{ERROUT}}$ enter a high impedance mode, to support automated board testing.

PC Board Routing Issues

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout to accommodate a single source of all clocks, particularly at frequencies above 50 MHz.

A full power and ground plane layout should be employed both under and around the IC package. For optimum noise immunity, it is highly recommended that the ICD2062B be used with a voltage regulator or Zener diode attached to the AVDD line. A less expensive (and less effective) alternative is to utilize an RC power filter as follows: the analog power pin (AVDD) is bypassed to ground with a 0.1µF multi-layer ceramic capacitor and a 2.2µF/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin. A 22Ω resistor placed between the power supply and the AVDD pin can help to filter noisy supply lines. Refer to IC DESIGNS Application Note *Power Feed and Board Layout Issues* on page 281 for more details and for illustrative schematics.

The designer should also avoid routing any of the output traces of the IC DESIGNS in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies. When designing with this device, it is best to locate the ICD2062B closest to the device requiring the highest frequency.

FCC & Noise issues

A conscious design effort was made to achieve the optimum rise & fall times at the output pads in order to produce acceptable signals at the clock destinations when operating at high frequencies. Unfortunately, the production of the squarest possible square waves can lead to the generation of high-energy odd harmonics, which can result in extraneous emissions.

For techniques on how to design with this device while taking FCC emission issues into consideration, please refer to the IC DESIGNS Application Note *Minimizing Radio Frequency Emissions* on page 285.

ECL Design Issues

Please refer to the IC DESIGNS Application Note *ECL Outputs* on page 289.

Minimized Parasitic Problems

All of the IC DESIGNS families of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, all the synthesis blocks are physically separated into discrete elements with their output oscillator pins placed on opposite sides of the die. Further, all the synthesis VCOs are separated from their digital logic. Finally, separate power and ground buses for the analog and digital circuitry are used.

Temperature and Process Sensitivity

Because of its feedback circuitry, the ICD2062B is inherently stable over temperature, voltage and manufacturing process variations. Incorporating the loop filter internal to the chip assures that the loop filter will track the same process variations as does the VCO. With the ICD2062B, no manufacturing "tweaks" to external filter components are required as is the case with external de-coupled filters.

Ordering Information

Table 14: Order Codes

Part Number	Package Type	Temperature Range	Speed Options
ICD2062B	S = 20-Pin SOIC DIP	C = Commercial[a]	–1: 135 MHz –2: 165 MHz

a. 0°C to +70°C

Example: order ICD2062BSC-2 for the ICD2062B, 20–pin plastic SOIC, commercial temperature range device with a top Video Clock frequency range of 165 MHz.

Device Specifications

Electrical Data

Table 15: Absolute Maximum Ratings

Name	Description	Min	Max	Units
V_{DD} & AV_{DD}	Supply voltage relative to GND	–0.5	7.0	Volts
V_{IN}	Input voltage with respect to GND	–0.5	V_{DD} + 0.5	Volts
T_{STOR}	Storage temperature	–65	+150	°C
T_{SOL}	Max soldering temperature (10 sec)		+260	°C
T_J	Junction temperature		+125	°C
P_{DISS}	Power dissipation		790 / 1050	mWatts

NOTE: Above the Maximum Ratings, the useful life may be impaired. For user guidelines, not tested.

OPERATING RANGE: V_{DD} & AV_{DD} = +5V ±5%; 0°C ≤ $T_{AMBIENT}$ ≤ 70°C
(This applies to all specifications below.)

Table 16: DC Characteristics

Name	Description	Min	Typ	Max	Units	Conditions
V_{IH}	High-level input voltage	2.0			Volts	
V_{IL}	Low-level input voltage			0.8	Volts	
$V_{OH(ECL)}$	ECL High-level output[a]	V_{DD} – 1.0		V_{DD} – 0.8	Volts	
$V_{OL(ECL)}$	ECL Low-level output	V_{DD} – 2.0		V_{DD} – 1.6	Volts	
$V_{OH(TTL)}$	TTL High-level output[b]	2.4			Volts	I_{OH} = –4.0 mA
$V_{OL(TTL)}$	TTL Low-level output			0.4	Volts	I_{OL} = 4.0 mA
I_{IH}	Input high current			150	µA	V_{IH} = 5.25V
I_{IL}	Input low current			–250	µA	V_{IL} = 0V
I_{OZ}	Output leakage current			10	µA	(3-state)
I_{DD}	Power supply current	15		150 / 200	mA	A / B
I_{DD-TYP}	Power supply current (typical)		45		mA	@ 60 MHz
$C_{OUT(ECL)}$	ECL Output Capacitance			10	pF	

a. ECL outputs: VCLKOUT, $\overline{\text{VCLKOUT}}$
b. TTL outputs: MCLKOUT, LDA, LDA/2, LDA/4, LDC, $\overline{\text{ERROUT}}$

Table 17: AC Characteristics

Symbol	Name	Description	Min	Typ	Max	Units
$f_{(REF)}$	reference frequency	Reference Oscillator nominal value (Note: for references of other than 14.31818 MHz, the pre-loaded ROM frequencies will not be accurate.)	1	14.318	60	MHz
$t_{(REF)}$	reference clock period	$1 \div f_{(REF)}$	16.6		1000	ns
t_1	input duty cycle	Duty cycle for the input oscillator defined as $t_1 \div t_{(REF)}$	25%	50%	75%	
t_2	output clock periods	Output oscillator values – ECL –	6.1 165 MHz		1970 508 KHz	ns
		– TTL –	8.3 120 MHz		1970 508 KHz	
t_3	output duty cycle	Duty cycle for the output oscillators (NOTE: for non-ECL outputs, the duty cycle is measured at CMOS threshold levels. At 5V, V_{TH} = 2.5V.)	40%		60%	
t_4	rise times	Rise time for the output oscillators into a 25pF load			3	ns
t_5	fall times	Fall time for the output oscillators into a 25pF load			3	ns
$t_{skew\text{-}ECL}$		Skew between the VCLKOUT complementary outputs			1	ns
t_{freq1}	freq1 output	Old frequency output				
t_{freq2}	freq2 output	New frequency output				
t_A	$f_{(REF)}$ mux time	Time clock output remains high while output muxes to reference frequency	$\frac{t_{(REF)}}{2}$		$3\frac{t_{(REF)}}{2}$	
$t_{timeout}$	timeout interval	Internal interval for serial programming and for VCO changes to settle. If the interval is too short, see the timeout interval section in the control register definition.	2	5	10	msec
t_B	t_{freq2} mux time	Time clock output remains high while output muxes to new frequency value	$\frac{t_{freq2}}{2}$		$3\frac{t_{freq2}}{2}$	
t_6	3-state	Time for the output oscillators to go into 3-state mode after $\overline{OUTDIS}$ signal assertion	0		12	ns
t_7	clk valid	Time for the output oscillators to recover from 3-state mode after $\overline{OUTDIS}$ signal goes high	0		12	ns

Table 17: AC Characteristics (Continued)

Symbol	Name	Description	Min	Typ	Max	Units
t_{LD}	Load Clock period	Maximum LDA & LDC period	10			ns
$t_{SKEW-LDA}$		VCLKOUT to LDA output skew	2		6	ns
$t_{SKEW-LDA/2}$		LDA to LDA/2 output skew	0	1	2	ns
$t_{SKEW-LDA/4}$		LDA to LDA/4 output skew	0	1	2	ns
$t_{SKEW-LDC}$		LDA to LDC output skew	0	1	2	ns
t_{EN-SU}		ENABLE setup time to LDA	12			ns
t_{EN-HD}		ENABLE hold time to LDA	0			ns
t_{serclk}		Clock period of serial clock	$2 \bullet t_{(REF)}$		2	msec
t_{HI}		Minimum high time of serial clock	$t_{(REF)}$			ns
t_{LO}		Minimum low time of serial clock	$t_{(REF)}$			ns
t_{SU}		Setup time	20			ns
t_{HD}		Hold time	10			ns
t_{ldcmd}		Load command	0		$t_1 + 30$	ns

NOTE: Input capacitance is typically 10pF, except for the crystal pads.

Timing Diagrams

Fig. 13: Rise and Fall Times

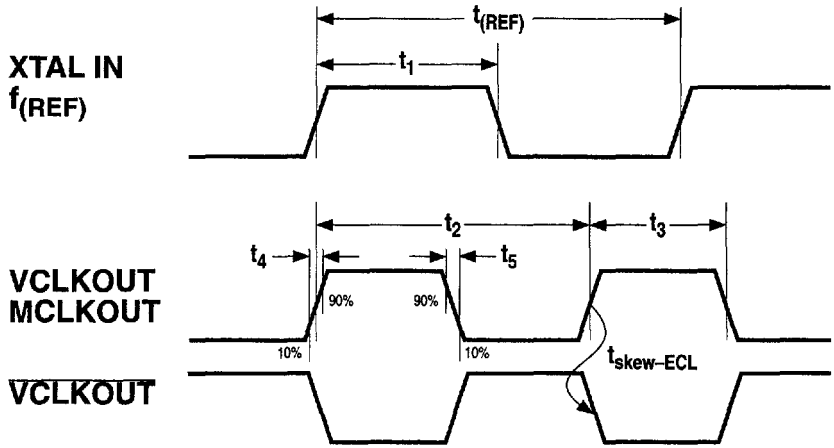


Fig. 14: 3-State Timing

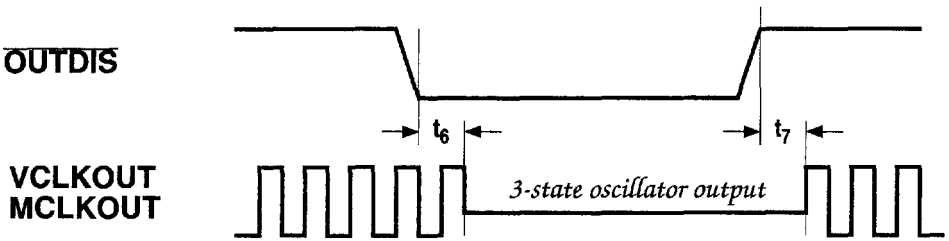


Fig. 15: Selection Timing

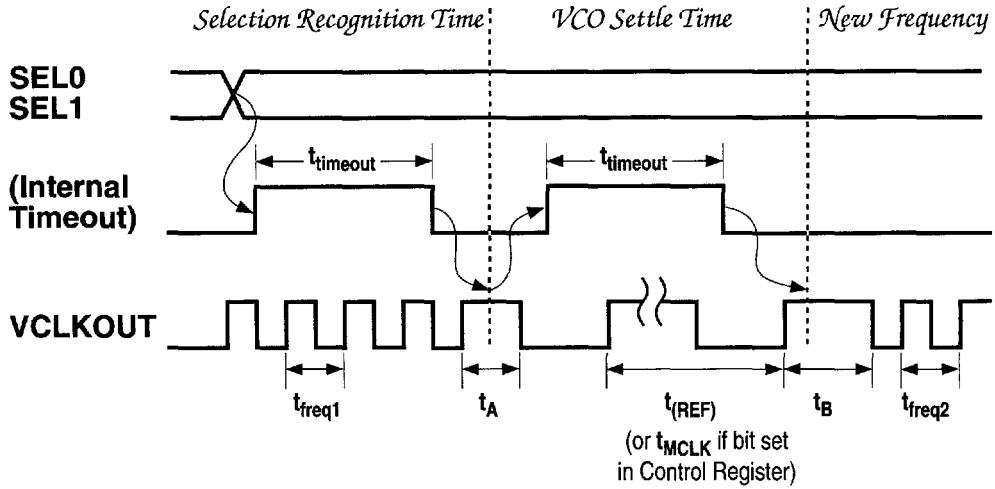


Fig. 16: MCLK & Active VCLK Register Programming Timing

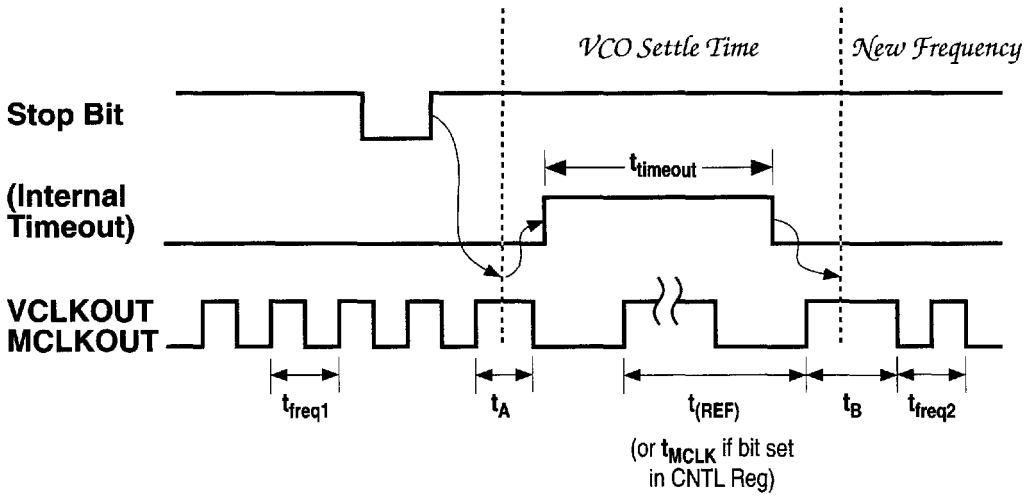


Fig. 17: RAMDAC / VRAM Interface Timing

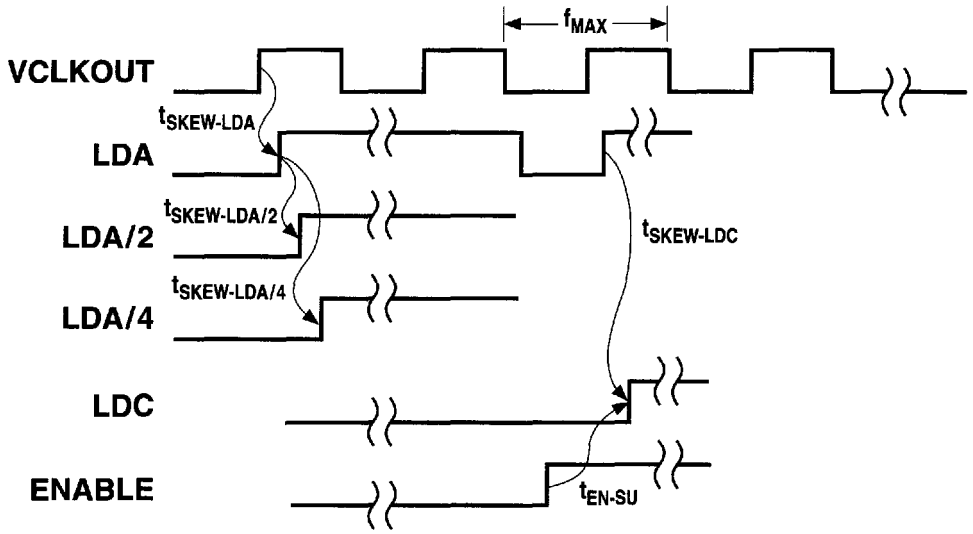
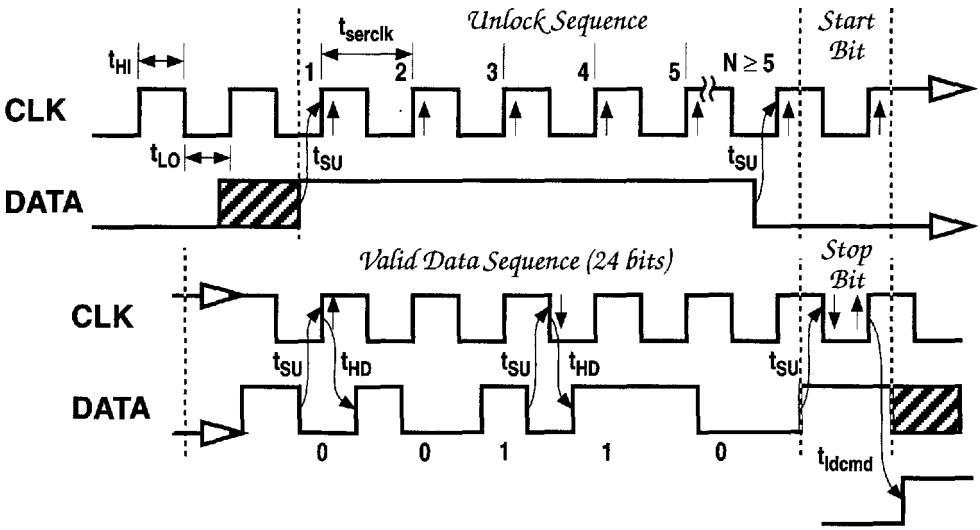


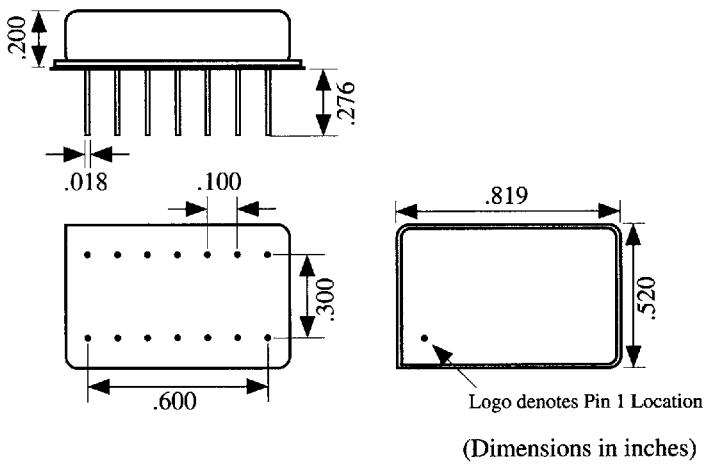
Fig. 18: Serial Programming Timing



14-Pin Packages

Table 1: 14-Pin Metal Can Outline

Package (Lead Count = 14)



(Dimensions in inches)

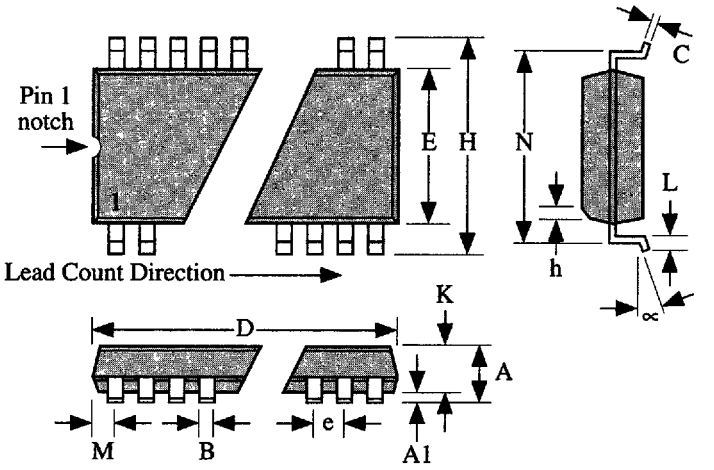
8

16-Pin Packages

Table 2: 16-Pin SOIC Outline

Symbol	MIN	MAX
A	.099	.104
A1	.004	.009
B	.014	.019
C	.010	REF
D	.405	.410
E	.294	.299
e	.050	TYP
H	.402	.419
h	.025 x	45°
L	.030	.040
∝	0°	8°
K	.088	.098
M	.020	.030
N	.335	.351

Package (Lead Count = 16)

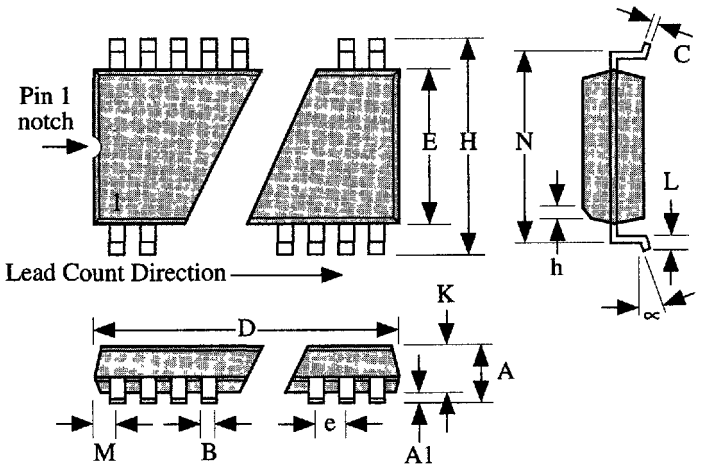


20-Pin Packages

Table 3: 20-Pin SOIC Outline

Symbol	MIN	MAX
A	.099	.104
A1	.004	.009
B	.014	.019
C	.010	REF
D	.505	.512
E	.294	.299
e	.050	TYP
H	.402	.419
h	.025 x 45°	
L	.030	.040
∝	0°	8°
K	.088	.098
M	.020	.030
N	.335	.351

Package (Lead Count = 20)



(Dimensions in inches)

8