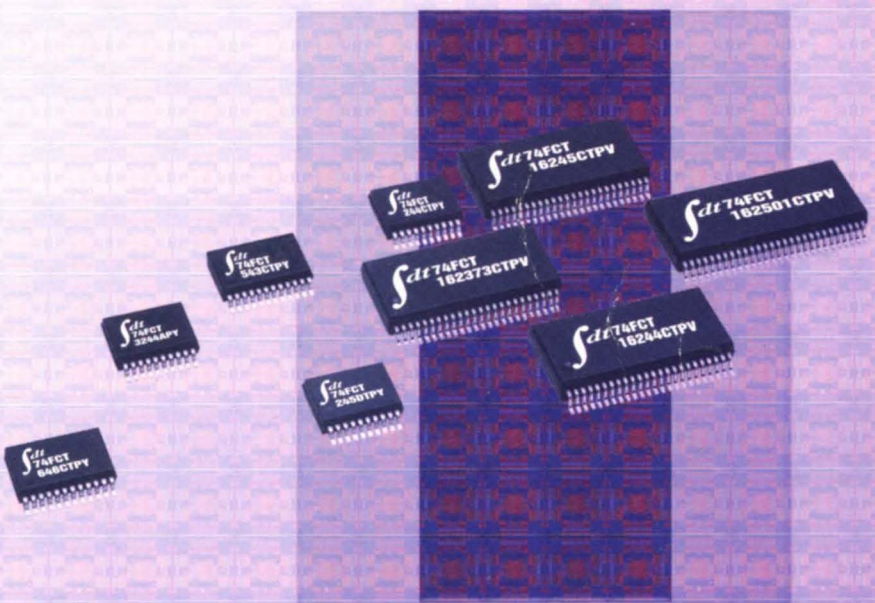
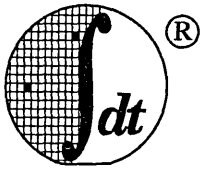
1992 DATA BOOK

HIGH-PERFORMANCE LOGIC

INCLUDES 3.3V AND DOUBLE-DENSITY LOGIC



Integrated Device Technology, Inc.



Integrated Device Technology, Inc.

1992
HIGH-PERFORMANCE
LOGIC
DATA BOOK

2975 Stender Way, Santa Clara, California 95054-3090
Telephone: (800) 345-7015 • TWX: 910-338-2070 • FAX: (408) 492-8674

CONTENTS OVERVIEW

For ease of use for our customers, Integrated Device Technology provides four separate data books: High-Performance Logic, Specialized Memories and Modules, RISC and RISC SubSystems, and Static RAM.

IDT's 1992 Logic Data Book is comprised of new and revised data sheets on Double-Density standard 5V logic, standard 5V logic, 3.3V logic, 3.3V-to-5V translators, and complex logic products. Also included is a current packaging section for the products included in this book.

The 1992 High-Performance Logic Data Book's Table of Contents contains a listing of the products contained in this data book only (in the past, we have included products that appeared in other IDT data books). The numbering scheme for the book is consistent with the 1990–91 data books. The number at the bottom center of the page denotes the section number and the sequence of the data sheet within that section, (i.e., 5.5 would be the fifth data sheet in the fifth section). The number in the lower right-hand corner is the page number for that particular data sheet.

Integrated Device Technology, Inc. is a recognized leader in high-speed CMOS technology and produces a broad line of products. This enables us to provide a complete CMOS solution to designers of high-performance digital systems. Not only do our product lines include industry standard devices, they also feature products with faster speeds, lower power, and package and/or architectural benefits that allow designers to significantly improve system performance.

To find ordering information: Ordering Information for all products in this book appears in Section 1, along with the Package Outline Index, Product Selector Guides, Ordering Information, and Standard Logic Timing Diagrams. Reference data on our Technology Capabilities and Quality Commitments is included in separate sections (2 and 3, respectively).

To find product data: Start with the Table of Contents, organized by product line (page 1.2), or with the Numeric Table of Contents (page 1.4). These indexes will direct you to the page on which the complete technical data sheet can be found. Data sheets may be of the following type:

ADVANCE INFORMATION—contain initial descriptions (subject to change) for products that are in development, including features and block diagrams.

PRELIMINARY—contain descriptions for products soon to be, or recently released to production, including features, pinouts, and block diagrams. Timing data are based on simulation or initial characterization and are subject to change upon full characterization.

FINAL—contain minimum and maximum limits specified over the complete supply and temperature range for full production devices.

New products, product performance enhancements, additional package types, and new product families are being introduced frequently. Please contact your local IDT sales representative to determine the latest device specifications, package types, and product availability.

ABOUT THE COVER

The cover features a High-Performance Double-Density wafer shown at approximately 3x magnification with a sampling of both standard, octal and Double-Density FCT-T packaged units shown at slightly larger than actual size. IDT's high-speed logic products are excellent for use in high-performance data processing systems. The new 3.3V members of the Double-Density family were specifically designed to address the low-power, low-noise requirements of battery operated systems, such as laptop and notebook computers. IDT also offers a 5V-to-3.3V translator chip that interfaces today's higher-voltage systems with next-generation low-voltage systems.

LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. **Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.**
2. **A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.**

1992 LOGIC DATA BOOK
TABLE OF CONTENTS

1

1992 LOGIC DATA BOOK (CONTINUED)

3.3V LOGIC AND 3.3V TO 5V TRANSLATORS

COMPLEX LOGIC PRODUCTS

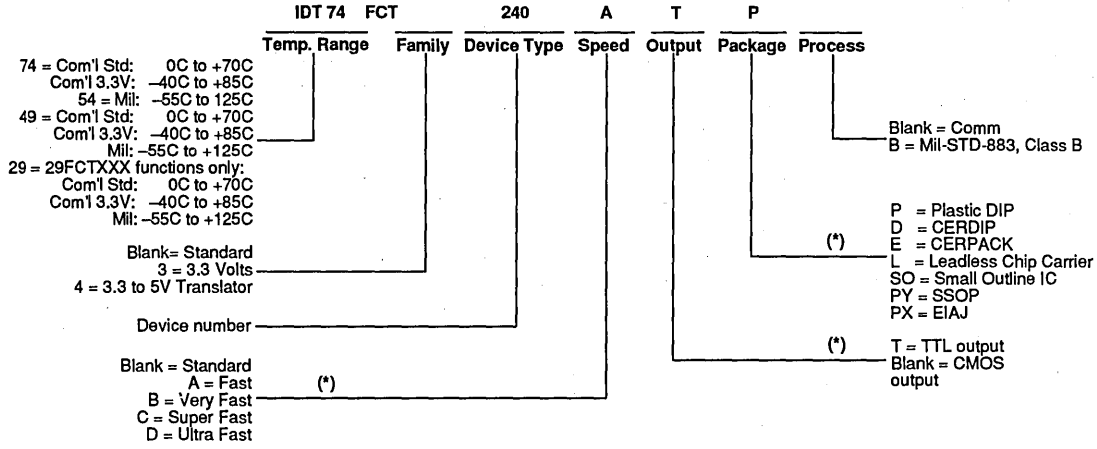
IDT SALES OFFICE, REPRESENTATIVE AND DISTRIBUTOR LOCATIONS

NUMERICAL TABLE OF CONTENTS

NUMERICAL TABLE OF CONTENTS (CONTINUED)

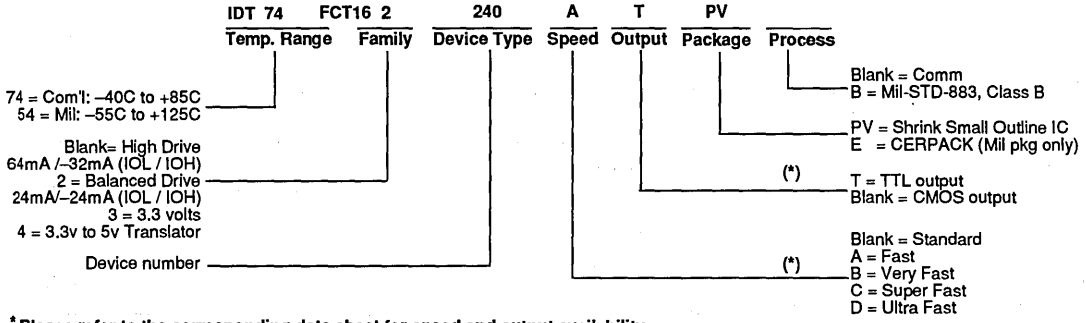
ORDERING INFORMATION

FCTXXX, FCTXXXT



*Please refer to the corresponding data sheet for speed, package and output availability

FCT16XXX, 16XXXT (Double Density)

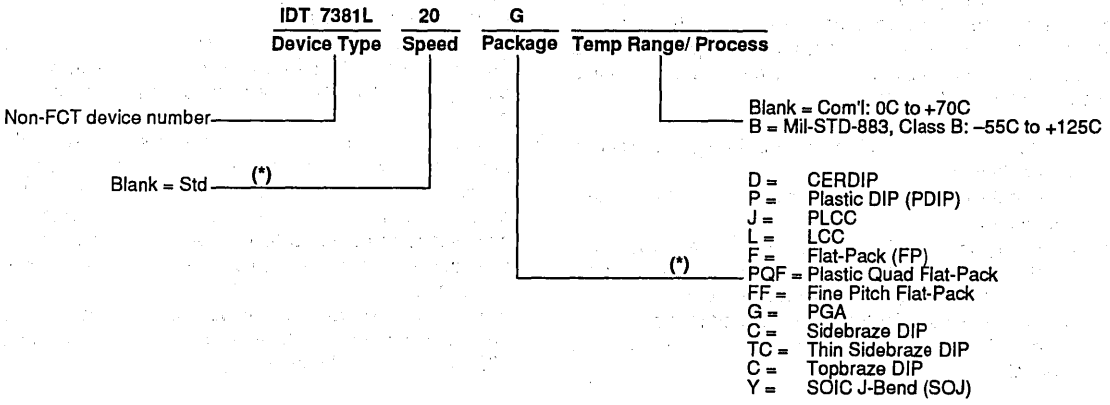


*Please refer to the corresponding data sheet for speed and output availability

ORDERING INFORMATION

1

NON-FCT DEVICES



*Please refer to table below for speed and package availability

NON-FCT DEVICE REFERENCE TABLE

Device	Speed		Package
	Commercial	Military	
39C10	B,C	B,C	CERDIP, PDIP, PLCC, LCC
39C60	Std., –1, A, B	Std., –1, A, B	FP, PLCC, PDIP, CERDIP
49C402	Std., A, B	Std., A, B	FP, PGA, PLCC
49C410	Std., A	Std., A	PDIP, SIDEBRAZE, PLCC, FP
49C460	Std., A, B, C, D	Std., A, B, C, D	FP, PGA, PLCC
49C465	Std., A	Std., A	PQF, PGA
49C466	Std.	Std.	PQF, PGA
7210L	25, 35, 45, 55, 65	30, 40, 55, 65, 75	FP, PGA, PDIP, PLCC, Topbraze
7216L	20, 25, 35, 45, 55, 65	25, 30, 40, 55, 65, 75	FP, PGA, PDIP, PLCC, Topbraze
7217L	20, 25, 35, 45, 55, 65	25, 30, 40, 55, 65, 75	FP, PGA, PDIP, PLCC, Topbraze
73200L	10, 12, 15	12, 15, 20	PDIP, PLCC, Sidebraze
73201L	10, 12, 15	12, 15, 20	PDIP, PLCC, Sidebraze
73210	Std., A, B	Std., A, B	SOJ, Thin-Sidebraze
73211	Std., A, B	Std., A, B	SOJ, Thin-Sidebraze
7381L	20, 25, 30, 40, 55	25, 30, 35, 45, 65	PLCC, PGA, FF
7383L	20, 25, 30, 40, 55	25, 30, 35, 45, 65	PLCC, PGA, FF
73720	Std.	Std.	PQF, PLCC

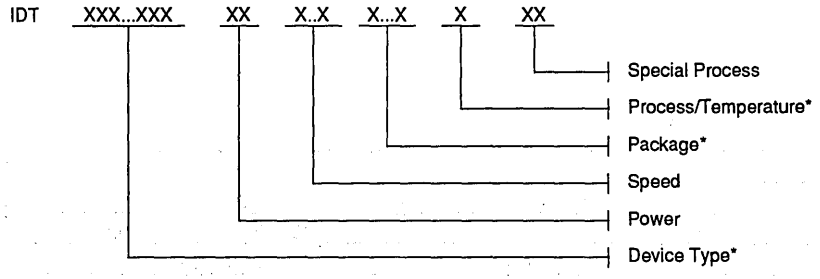
IDT PACKAGE MARKING DESCRIPTION

PART NUMBER DESCRIPTION

IDT's part number identifies the basic product, speed, power, package(s) available, operating temperature and processing grade. Each data sheet has a detailed description, using the part number, for ordering the proper product for the user's application. The part number is comprised of a series of alpha-numeric characters:

1. An "IDT" corporate identifier for Integrated Device Technology, Inc.
2. A basic device part number composed of alpha-numeric characters.
3. A device power identifier, composed of one or two alpha characters, is used to identify the power options. In most cases, the following alpha characters are used:
   "S" or "SA" is used for the standard product's power.
   "L" or "LA" is used for lower power than the standard product.
4. A device speed identifier, when applicable, is either alpha characters, such as "A" or "B", or numbers, such as 20 or 45. The speed units, depending on the product, are in nanoseconds or megahertz.
5. A package identifier, composed of one or two characters. The data sheet should be consulted to determine the packages available and the package identifiers for that particular product.
6. A temperature/process identifier. The product is available in either the commercial or military temperature range, processed to a commercial specification, or the product is available in the military temperature range with full compliance to MIL-STD-883. Many of IDT's products have burn-in included as part of the standard commercial process flow.
7. A special process identifier, composed of alpha characters, is used for products which require radiation enhancement (RE) or radiation tolerance (RT).

Example for Monolithic Devices:



* Field Identifier Applicable To All Products

2507 drw 01

ASSEMBLY LOCATION DESIGNATOR

IDT uses various locations for assembly. These are identified by an alpha character in the last letter of the date code marked on the package. Presently, the assembly location alpha character is as follows:

A = Anam, Korea
I = USA
P = Penang, Malaysia

MIL-STD-883C COMPLIANT DESIGNATOR

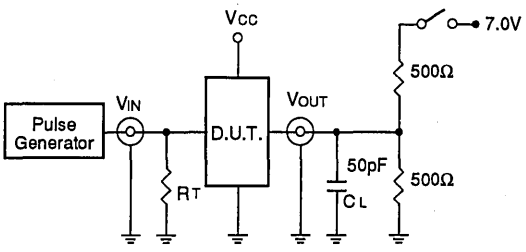
IDT ships military products which are compliant to the latest revision of MIL-STD-883C. Such products are identified by a "C" designation on the package. The location of this designator is specified by internal documentation at IDT.

EXAMPLE FOR SUBSYSTEM MODULES

See Ordering Information (section 1.4), page 2.

TEST CIRCUITS AND WAVEFORMS
FCTXXX, FCTXXXT, FCT16XXXT - 5V FAMILIES

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

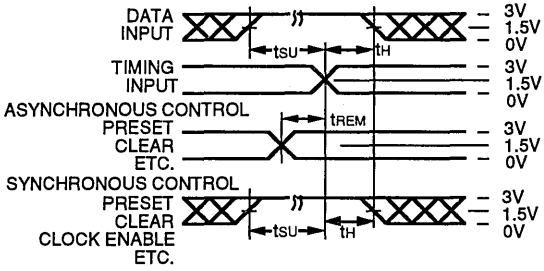
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

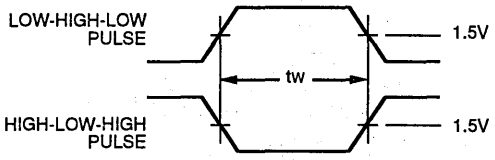
CL= Load capacitance: includes jig and probe capacitance.

RT= Termination resistance: should be equal to ZOUT of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



PULSE WIDTH



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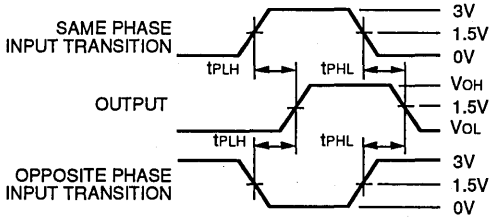
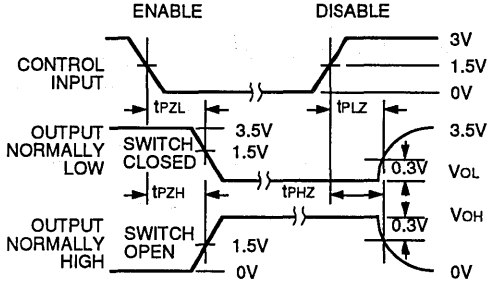
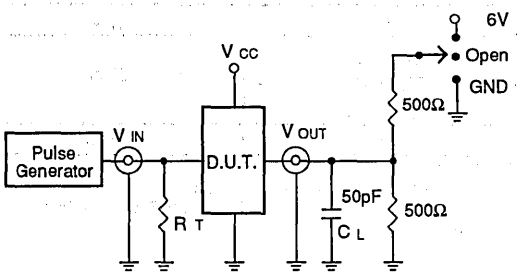


ENABLE AND DISABLE TIMES



TEST CIRCUITS AND WAVEFORMS
FCT3XXX AND FCT163XXX - 3.3V FAMILY

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

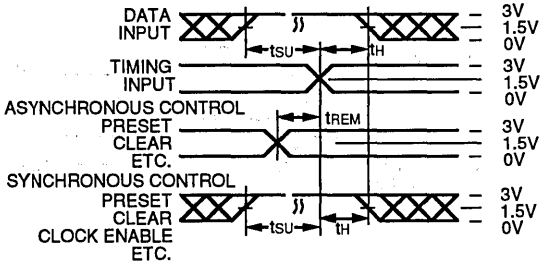
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



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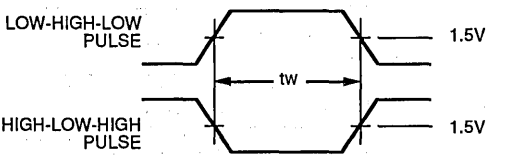
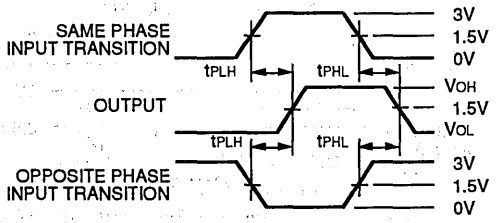
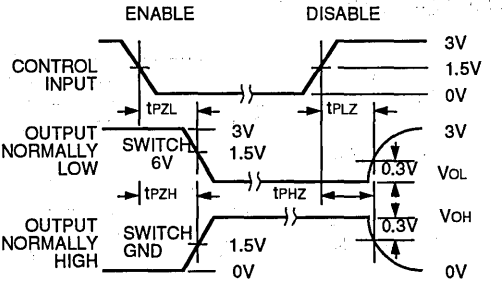


PROPAGATION DELAY



ENABLE AND DISABLE TIMES



High-Speed CEMOS Logic Products — Bus Interface Devices

- FCT and FCT-T CEMOS families are the fastest in the industry with maximum propagation delays as low as 4.1ns.
- The FCT-T family offers the lowest-power solution. No other logic family uses less dynamic power, standby power, or static high or low power.
- The FBT BiCEMOS Memory Drivers with 25Ω resistors reduce overshoot and undershoot when driving CMOS RAMs.
- The new Double-Density bus interface family offers users significant board area savings, power savings, higher speeds, guaranteed low noise, and a choice of output drive characteristics. Three configurations are available:
  1. Standard 64mA high drive device for bus and backplane interface.
  2. 24mA balanced output drive with on-chip resistors for internal bus and point to point driving.
  3. 3.3V bus interface logic for systems with 3.3V regulated supplies.
- The EDC (Error Detection and Correction) devices can detect multiple errors as fast as 10ns and correct as fast as 14ns.
- IDT features a series of read-write buffers with 8-bit bidirectional registers and 16-bit pipeline registers.
- The DSP Building Blocks are composed of 16-bit ALUs, Multipliers, and Multiplier-Accumulators with speeds as fast as 20ns.

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typ. Power (mW)	Data Book Page
DOUBLE-DENSITY FAMILY					
IDT54/74FCT16240T/AT/CT	16-Bit Buffer/Line Driver	4.7	4.3	0.01	5.1
IDT54/74FCT162240T/AT/CT					5.1
IDT54/74FCT16244T/AT/CT	16-Bit Buffer/Line Driver	4.6	4.1	0.01	5.2
IDT54/74FCT162244T/AT/CT					5.2
IDT54/74FCT163244/A	3.3V 16-Bit Buffer/Line Driver				7.1
IDT54/74FCT16245T/AT/CT	16-Bit Bidirectional Transceivers	4.5	4.1	0.01	5.3
IDT54/74FCT162245T/AT/CT					5.3
IDT54/74FCT163245/A	3.3V 16-Bit Bidirectional Transceivers				7.2
IDT54/74FCT164245T	Mixed Supply (3.3/5.0V) Translator				7.9
IDT54/74FCT16373T/AT/CT	16-Bit Transparent Latches	5.1	4.2	0.006	5.4
IDT54/74FCT162373T/AT/CT					5.4
IDT54/74FCT163373/A	3.3V 16-Bit Transparent Latches				7.3
IDT54/74FCT16374T/AT/CT	16-Bit Register (3-State)	6.2	5.2	0.006	5.5
IDT54/74FCT162374T/AT/CT					5.5
IDT54/74FCT163374/A	3.3V 16-Bit Register (3-State)				7.4
IDT54/74FCT16646T/AT/CT	16-Bit Bus Transceiver/Registers	6.0	5.4	0.006	5.9
IDT54/74FCT162646T/AT/CT	(3-State)				5.9
IDT54/74FCT163646/A	3.3V 16-Bit Bus Transceiver/Registers				7.6
IDT54/74FCT16500AT/CT	18-Bit Registered Bus Transceiver	4.6	4.6	0.006	5.6
IDT54/74FCT162500AT/CT	(3-State)				5.6
IDT54/74FCT16501AT/CT	18-bit Registered Bus Transceiver	4.6	4.6	0.006	5.7
IDT54/74FCT162501AT/CT	(3-State)				5.7
IDT54/74FCT163501/A	3.3V 18-Bit Registered Bus Transceiver				7.5
IDT54/74FCT16543T/AT/CT/DT	16-Bit Latched Transceiver	6.1	4.4	0.006	5.8
IDT54/74FCT162543T/AT/CT/DT					5.8
IDT54/74FCT16952T/AT/CT/DT	16-Bit Registered Transceivers	7.3	4.5	0.006	5.11
IDT54/74FCT162952T/AT/CT/DT					5.11
IDT54/74FCT16652T/AT/CT	16-Bit Transceiver/Registers	6.0	5.4	0.006	5.10
IDT54/74FCT162652T/AT/CT					5.10
IDT54/74FCT16823AT/BT/CT	18-Bit Bus Interface Registers	7.0	6.0	0.006	5.12
IDT54/74FCT162823AT/BT/CT					5.12
IDT54/74FCT16841AT/BT/CT	20-Bit Transparent Latch	6.3	5.5	0.006	5.14
IDT54/74FCT162841AT/BT/CT					5.14
IDT54/74FCT16827AT/BT/CT	20-Bit Buffers	5.0	4.4	0.006	5.13
IDT54/74FCT162827AT/BT/CT					5.13

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typ. Power (mW)	Data Book Page
FCT/FCT-T FAMILY					
IDT29FCT52A/B/C IDT29FCT52AT/BT/CT	Non-Inverting Octal Registered Transceiver	7.3	6.3	1.0	6.26 6.1
IDT29FCT53A/B/C IDT29FCT53AT/BT/CT	Inverting Octal Registered Transceiver	7.3	6.3	1.0	6.26 6.1
IDT29FCT520A/B/C IDT29FCT520AT/BT/CT/DT	Multilevel Pipeline Register	7.0	5.2	1.0	6.27 6.2
IDT29FCT521AT/BT/CT/DT	Octal Multilevel Pipeline Register (level 1 replaced)	7.0	5.2	1.0	6.2
IDT49FCT805/A	Clock Driver w/Guaranteed Skew	6.8	5.8	1.0	6.28
IDT49FCT806/A	Inverting Clock Driver w/Guaranteed Skew	6.8	5.8	1.0	6.28
IDT54/74FCT138/A/C IDT54/74FCT138T/AT/CT	1-of-8 Decoder	6.0	5.1	1.0	6.29 6.3
IDT54/74FCT139/A/C IDT54/74FCT139T/AT/CT	Dual 1-of-4 Decoder	6.2	5.0	1.0	6.30 6.4
IDT54/75FCT151T/AT/CT	8-Input Multiplexer	6.2	5.6	1.0	6.5
IDT54/74FCT157T/AT/CT	Quad 2-Input Multiplexer	5.0	4.3	1.0	6.6
IDT54/74FCT161/A/C IDT54/74FCT161T/AT/CT	Synchronous Binary Counter w/Synchronous Reset	6.3	5.8	1.0	6.31 6.7
IDT54/74FCT163/A/C IDT54/74FCT163T/AT/CT	Synchronous Binary Counter w/Asynchronous Master Reset	6.3	5.8	1.0	6.31 6.7
IDT54/74FCT182/A	Carry Lookahead Generator	10.7	7.0	1.0	6.32
IDT54/74FCT191/A IDT54/74FCT191T/AT	Up/Down Binary Counter	10.5	7.8	1.0	6.33 6.8
IDT54/74FCT193/A IDT54/74FCT193T/AT	Up/Down Binary Counter	6.9	6.5	1.0	6.34 6.9
IDT54/74FCT240/A/C IDT54/74FCT240T/AT/CT/DT	Inverting Octal Buffer/Line Driver	4.7	3.6	1.0	6.35 6.10
IDT54/74FCT241/A/C IDT54/74FCT241T/AT/CT/DT	Inverting Octal Buffer/Line Driver	4.6	3.6	1.0	6.35 6.10
IDT54/74FCT244/A/C IDT54/74FCT244T/AT/CT/DT IDT54/74FCT3244/A	Inverting Octal Buffer/Line Driver 3.3V Inverting Octal Buffer/Line Driver	4.6	3.6	1.0	6.35 6.10 7.7
IDT54/74FCT245/A/C IDT54/74FCT245T/AT/CT/DT IDT54/74FCT3245/A	Inverting Octal Bidirectional Transceiver 3.3V Inverting Octal Buffer Transceiver	4.5	3.8	1.0	6.36 6.11 7.8
IDT54/74FCT251T/AT/CT	8-Input Multiplexer with OE	6.2	5.6	1.0	6.5
IDT54/74FCT257T/AT/CT	Quad 2-Input Multiplexer w/OE	5.0	4.3	1.0	6.6
IDT54/74FCT273/A/C IDT54/74FCT273T/AT/CT	Octal D Flip-Flop with Reset	6.5	5.8	1.0	6.37 6.12
IDT54/74FCT299/A/C IDT54/74FCT299/AT/CT	Octal Universal Shift Register w/Common Parallel I/O Pins	7.5	6.5	1.0	6.38 6.13
IDT54/74FCT373/A/C IDT54/74FCT373T/AT/CT/DT	Octal Transparent Latch	5.1	3.8	1.0	6.39 6.14
IDT54/74FCT374/A/C IDT54/74FCT374T/AT/CT/DT	Octal D Register	6.2	4.2	1.0	6.40 6.15
IDT54/74FCT377/A/C IDT54/74FCT377T/AT/CT	Octal D Flip-Flop w/Clock Enable	5.5	5.2	1.0	6.41 6.16
IDT54/74FCT399/A/C IDT54/74FCT399T/AT/CT	Quad Dual-Port Register	6.6	6.1	7.0	6.42 6.17

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typ. Power (mW)	Data Book Page
IDT54/74FCT521/A/B/C IDT54/74FCT521T/AT/BT/CT	8-Bit Identity Comparator	5.1	4.5	1.0	6.43 6.18
IDT54/74FCT533/A/C IDT54/74FCT533T/AT/CT	Inverting Octal Transparent Latch w/3-State	5.1	4.2	1.0	6.39 6.14
IDT54/74FCT534/A/C IDT54/74FCT534T/AT/CT	Inverting Octal D Register w/3State	6.2	5.2	1.0	6.40 6.15
IDT54/74FCT540/A/C IDT54/74FCT540T/AT/CT	Inverting Octal Buffer/Line Driver	4.7	4.3	1.0	6.35 6.10
IDT54/74FCT541/A/C IDT54/74FCT541T/AT/CT	Non-Inverting Octal Buffer/Line Driver	4.7	4.3	1.0	6.35 6.10
IDT54/74FCT543/A/C IDT54/74FCT543T/AT/CT/DT	Non-Inverting Octal Latched Transceiver	6.1	4.4	1.0	6.44 6.19
IDT54/74FCT573/A/C IDT54/74FCT573T/AT/CT/DT	Octal Transparent Latch	5.1	3.8	1.0	6.39 6.14
IDT54/74FCT574/A/C IDT54/75FCT574T/AT/CT/DT	Octal D Register w/ 3-State	6.2	4.2	1.0	6.40 6.15
IDT54/74FCT620T/AT/CT	Inverting Octal Bus Transceiver w/3-State	5.1	4.5	1.0	6.21
IDT54/74FCT621T/AT	Non-Inverting Octal Bus Transceiver w/Open Drain	12.5	12.0	1.0	6.22
IDT54/74/FCT622T/AT	Inverting Octal Bus Transceiver w/Open Drain	12.5	12.0	1.0	6.22
IDT54/74FCT623T/AT/CT	Non-Inverting Octal Bus Transceiver w/3-State	5.4	4.8	1.0	6.21
IDT54/74FCT640/A/C IDT54/74FCT640T/AT/CT	Inverting Octal Transceiver	4.7	4.4	1.0	6.36 6.11
IDT54/74FCT645/A/C IDT54/74FCT645T/AT/CT/DT	Non-Inverting Bidirectional Transceiver	4.5	3.8	1.0	6.36 6.11
IDT54/74FCT646/A/C IDT54/74FCT646T/AT/CT/DT	Octal Transceiver/Register	6.0	4.4	1.0	6.45 6.20
IDT54/74FCT648T/AT/CT	Octal Transceiver/Register	6.0	5.4	1.0	6.20
IDT54/74FCT651T/AT/CT	Inverting Octal Registered Transceiver	6.0	5.4	1.0	6.20
IDT54/74FCT652T/AT/CT/DT	Non-Inverting Octal Registered Transceiver	6.0	4.4	1.0	6.20
IDT54/74FCT821A/B/C IDT54/74FCT821AT/BT/CT/DT	10-Bit Non-Inverting Register	7.0	4.2	1.0	6.46 6.23
IDT54/74FCT823A/B/C IDT54/74FCT823AT/BT/CT/DT	9-Bit Non-Inverting Register	7.0	5.0	1.0	6.46 6.23
IDT54/74FCT824A/B/C	9-Bit Inverting Register	7.0	6.0	1.0	6.46
IDT54/74FCT825A/B/C IDT54/74FCT825AT/BT/CT	8-Bit Non-Inverting Register	7.0	6.0	1.0	6.46 6.23
IDT54/74FCT826AT/BT/CT	8-Bit Inverting Register w/Multiple Enable	7.0	6.0	1.0	6.23
IDT54/74FCT827A/B/C IDT54/74FCT827AT/BT/CT/DT	10-Bit Non-Inverting Buffer	5.0	3.8	1.0	6.47 6.24
IDT54/74FCT828AT/BT/CT	10-Bit Inverting Register	5.0	4.4	1.0	6.24
IDT54/74FCT833A/B	8-Bit Transceiver w/Parity	10.0	7.0	1.0	6.48
IDT54/74FCT841A/B/C IDT54/74FCT841AT/BT/CT/DT	10-Bit Non-Inverting Latch	6.3	4.2	1.0	6.49 6.25
IDT54/74FCT843A/B/C IDT54/74FCT843AT/BT/CT	9-Bit Non-Inverting Latch	6.3	5.5	1.0	6.49 6.25

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typ. Power (mW)	Data Book Page
IDT54/74FCT844A/B/C	9-Bit Inverting Latch	6.3	5.5	1.0	6.49
IDT54/74FCT845A/B/C IDT54/74FCT845AT/BT/CT	8-Bit Non-Inverting Latch	6.3	5.5	1.0	6.49 6.25
IDT54/74FCT861A/B	10-Bit Non-Inverting Transceiver	6.5	6.0	1.0	6.50
IDT54/74FCT863A/B	9-Bit Non-Inverting Transceiver	6.5	6.0	1.0	6.50
IDT54/74FCT864A/B	9-Bit Inverting Transceiver	6.5	6.0	1.0	6.50
FBT FAMILY					
IDT54/74FBT2240/A	BiCEMOS Inv. Octal Memory Driver	5.1	4.8	1.0	6.51
IDT54/74FBT2244/A	BiCEMOS Non-Inv. Memory Driver	5.1	4.8	1.0	6.52
IDT54/74FBT2373/A	BiCEMOS Octal Transparent Latch Drivers	5.6	5.2	1.0	6.53
IDT54/74FBT2827A/B	BiCEMOS Non-Inverting 10-Bit Memory Driver	6.5	5.0	1.0	6.54
IDT54/74FBT2828A/B	BiCEMOS Inv. 10-Bit Memory Driver	6.5	5.5	1.0	6.54
IDT54/74FBT2841A/B	BiCEMOS Non-Inverting 10-Bit Latch	7.5	6.5	1.0	6.55

Part Number	Description	Max. Speed (ns) Com'l.	Typ. Power (mW)	Data Book Page
MICROSLICE™ PRODUCTS				
IDT49C402 IDT49C402A IDT49C402B	16-Bit µP Slice, quad 2901 with 8 additional destination functions and 64 x 16 register file capacity — superset of Am29C101, CY7C9101, WS159016	A,B addr to Y = 47ns A,B addr to Y = 37ns A,B addr to Y = 28ns	50	8.2
IDT39C10B IDT39C10C	12-bit Sequencer with 33-deep stack — replaces AM2910/A, CY7C910	D to Y = 20ns D to Y = 12ns	175	8.1
IDT49C410 IDT49C410A	16-bit Sequencer with 33-deep stack address up to 64K microcode	D to Y = 20ns D to Y = 12ns	175	8.3

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typ. Power (mW)	Data Book Page
DSP BUILDING BLOCKS					
IDT7381L20/25/30/40/55	16-bit Cascadable ALU (replaces Logic Devices' L4C381)	25	20	10	8.6
IDT7383L20/25/30/40/55	16-bit Cascadable ALU (32 instructions)	25	20	10	8.6
IDT7210L25/35/45/55/65	16 x 16-bit with 35-bit output, replaces TDC1010J	30	25	20	8.4
IDT7216L20/25/35/45/55/65	16 x 16-bit, replaces Am29516	25	20	20	8.5
IDT7217L20/25/35/45/55/65	16 x 16-bit with Single-Clock Architecture, replaces Am29517	25	20	20	8.5
READ-WRITE BUFFERS AND BUS MULTIPLEXERS					
73200L10/L12/L15	16-bit 8-level-deep Pipeline Register; replaces four Am29520s	12	10	10	8.7
73201L10/L12/L15	16-bit 7-level-deep Pipeline Register with pass-through mode	12	10	10	8.7
73210/A/B	8-bit Bidirectional Registers with parity; one register and one latch from B to A	7.5	6.0	0.1	8.8

Part Number	Description	Max. Speed (ns) Mil.	Com'l.	Typ. Power (mW)	Data Book Page
73211/A/B	8-bit Bidirectional Registers with parity; two latches from B to A	7.5	6.0	0.1	8.8
73720	16-Bit 3-Port Latched Bus Exchanger		7.5	1.0	8.9
ERROR DETECTION AND CORRECTION		**Detect Time**			
IDT39C60	16-bit Cascadable EDC	36	32	15	8.10
IDT39C60-1	Replaces Am2960, -1, A; N2960,	28	25		8.10
IDT39C60A	MC74F2960, -1, A	24	20		8.10
IDT39C60B		22	18		8.10
IDT49C460	32-bit Cascadable EDC	44	40	15	8.11
IDT49C460A	Replaces Am29C660.	33	30		8.11
IDT49C460B		28	25		8.11
IDT49C460C		21	16		8.11
IDT49C460D		16	12		8.11
IDT49C465/A	32-bit Flow-thruEDC™—two separate bidirectional 32-bit buses; expandable to 64-bit, 144-pin PGA.	20	15	25	8.12
IDT49C466	64-bit Flow-thruEDC—two separate bidirectional 64-bit buses; 208-pin PGA		20	15	8.13

IDT...LEADING THE CMOS FUTURE

A major revolution is taking place in the semiconductor industry today. A new technology is rapidly displacing older NMOS and bipolar technologies as the workhorse of the '80s and beyond. That technology is high-speed CMOS. Integrated Device Technology, a company totally predicated on and dedicated to implementing high-performance CMOS products, is on the leading edge of this dramatic change.

Beginning with the introduction of the industry's fastest CMOS 2K x 8 static RAM, IDT has grown into a company with multiple divisions producing a wide range of high-speed CMOS circuits that are, in almost every case, the fastest available. These advanced products are produced with IDT's proprietary CEMOS™ technology, a twin-well, dry-etched, stepper-aligned process utilizing progressively smaller dimensions.

From inception, IDT's product strategy has been to apply the advantages of its extremely fast CEMOS technology to produce the integrated circuit elements required to implement high-performance digital systems. IDT's goal is to provide the circuits necessary to create systems which are far superior to previous generations in performance, reliability, cost, weight, and size. Many of the company's innovative product designs offer higher levels of integration, advanced architectures, higher density packaging and system enhancement features that are establishing tomorrow's industry standards. The company is committed to providing its customers with an ever-expanding series of these high-speed, lower-power IC solutions to system design needs.

IDT's commitment, however, extends beyond state-of-the-art technology and advanced products to providing the highest level of customer service and satisfaction in the industry. Manufacturing products to exacting quality standards that provide excellent, long-term reliability is given the same level of importance and priority as device performance. IDT is also dedicated to delivering these high-quality advanced products on time. The company would like to be known not only for its technological capabilities, but also for providing its customers with quick, responsive, and courteous service.

IDT's product families are available in both commercial and military grades. As a bonus, commercial customers obtain the benefits of military processing disciplines, established to meet or exceed the stringent criteria of the applicable military specifications.

IDT is the leading U.S. supplier of high-speed CMOS circuits. The company's high-performance fast SRAM , FCT logic, high-density modules, FIFOs, multi-port memories, BiCEMOS™ ECL I/O memories, RISC SubSystems, and the 32- and 64-bit RISC microprocessor families complement each other to provide high-speed CMOS solutions for a wide range of applications and systems.

Dedicated to maintaining its leadership position as a state-of-the-art IC manufacturer, IDT will continue to focus on maintaining its technology edge as well as developing a broader range of innovative products. New products and speed enhancements are continuously being added to each of the existing product families, and additional product families are being introduced. Contact your IDT field representative or factory marketing engineer for information on the most current product offerings. If you're building state-of-the-art equipment, IDT wants to help you solve your design problems.

IDT MILITARY AND DESC-SMD PROGRAM

IDT is a leading supplier of military, high-speed CMOS circuits. The company's high-performance Static RAMs, FCT Logic Family, Complex Logic (CLP), FIFOs, Specialty Memories (SMP), ECL I/O BiCMOS Memories, 32-bit RISC Microprocessor, RISC Subsystems and high-density Subsystems Modules product lines complement each other to provide high-speed CMOS solutions to a wide range of military applications and systems. Most of these product lines offer Class B products which are fully compliant to the latest revision of MIL-STD-883, Paragraph 1.2.1. In addition, IDT offers Radiation Tolerant (RT), as well as Radiation Enhanced (RE), products.

IDT has an active program with the Defense Electronic Supply Center (DESC) to list all of IDT's military compliant devices on Standard Military Drawings (SMD). The SMD program allows standardization of militarized products and reduction of the proliferation of non-standard source control drawings. This program will go far toward reducing the need for each defense contractor to make separate specification control drawings for purchased parts. IDT plans to have SMDs for many of its product offerings. Presently, IDT has 88 devices which are listed or pending listing. The devices are from IDT's SRAM, FCT Logic family, Complex Logic (CLP), FIFOs and Specialty Memories (SMP) product families. IDT expects to add another 20 devices to the SMD program in the near future. Users should contact either IDT or DESC for current status of products in the SMD program.

SMD	
SRAM	**IDT**
84036/E	6116
5962-88740	6116LA
84132/B	6167
5962-86015/A	7187
5962-86859	6198/7198/7188
5962-86705/D	6168
5962-85525/B	7164
5962-88552/B	71256L
5962-88662/A	71256S
5962-88611/A	71682L
5962-88681/A	71258S
5962-88545	71258L
5962-89891	7198
5962-89892	6198
5962-89690	6116
5962-38294/B	7164
5962-89692	7188
5962-89712	71982
SMP	**IDT**
5962-86875/B	7130/7140
5962-87002/C	7132/7142
5962-88610/A	7133S/7143S
5962-88665/A	7133L/7143L
FIFO	**IDT**
5962-87531	7201LA
5962-86846/A	72404
5962-88669	7203S
5962-89568	7204L
5962-89536	7202L
5962-89863	7201S
5962-89523	72403L
5962-89666	7200L
5962-89942	72103L
5962-89943	72104L
5962-89567	7203L

SMD	
LOGIC	**IDT**
5962-87630/B	54FCT244/A
5962-87629/C	54FCT245/A
5962-86862/B	54FCT299/A
5962-87644/A	54FCT373/A
5962-87628/C	54FCT374/A
5962-87627/B	54FCT377/A
5962-87654/A	54FCT138/A
5962-87655/A	54FCT240/A
5962-87656/A	54FCT273/A
5962-89533	54FCT861A/B
5962-89506	54FCT827A/B
5962-88575	54FCT841A/B
5962-88608	54FCT821A/B
5962-88543/A	54FCT521/A
5962-88640/A	54FCT161/A
5962-88639/A	54FCT573/A
5962-88656	54FCT823A/B
5962-88657/A	54FCT163/A
5962-88674	54FCT825A/B
5962-88661	54FCT863A/B
5962-88736/A	29FCT520A/B
5962-88775	54FCT646
5962-89508	54FCT139/A
5962-89665	54FCT824A/B
5962-88651	54FCT533/A
5962-88652	54FCT182/A
5962-88653	54FCT645A/B
5962-88654	54FCT640A/B
5962-88655	54FCT534/A
5962-89767	54FCT540/A
5962-89766	54FCT541/A
5962-89733/A	54FCT191/A
5962-89732	54FCT241/A
5962-89652	54FCT399/A
5962-89513	54FCT574/A
5962-89731	54FCT833A/B
5962-88675	54FCT845A/B
5962-89730	54FCT543/A

SMD	
CLP	**IDT**
5962-87708/A	39C10B & C
5962-88533/A	49C460A/B/C
5962-88613/A	39C60A
5962-88643/A	49C410
5962-86893	7216L
5962-87686	7217L
5962-88733/A	7210L
5962-89758	54FCT843A/B/C
5962-90669	54FCT193/A
5962-90901	29FCT52A/B/C

2509 tbl 01

RADIATION HARDENED TECHNOLOGY

IDT manufactures and supplies radiation hardened products for military/aerospace applications. Utilizing special processing and starting materials, IDT's radiation hardened devices survive in hostile radiation environments. In Total Dose, Dose Rate, and environments where single event upset is of concern, IDT products are designed to continue functioning without loss of performance. IDT can supply all its products on these processes. Total Dose radiation testing is performed in-house on an ARACOR X-Ray system. External facilities are utilized for device research on gamma cell, LINAC and other radiation equipment. IDT has an on-going research and development program for improving radiation handling capabilities (See "IDT Radiation Tolerant/Enhanced Products for Radiation Environments" in Section 3) of IDT products/processes.

IDT LEADING EDGE CEMOS TECHNOLOGY

HIGH-PERFORMANCE CEMOS

From IDT's beginnings in 1980, it has had a belief in and a commitment to CMOS. The company developed a high-performance version of CMOS, called enhanced CMOS (CEMOS), that allows the design and manufacture of leading-edge components. It incorporates the best characteristics of traditional CMOS, including low power, high noise immunity and wide operating temperature range; it also achieves speed and output drive equal or superior to bipolar Schottky TTL. The last decade has seen development and production of four "generations" of IDT's CEMOS technology with process improvements which have reduced IDT's electrical effective (Leff) gate lengths by more than 50 percent from 1.3 microns (millionths of a meter) in 1981 to 0.6 microns in 1989.

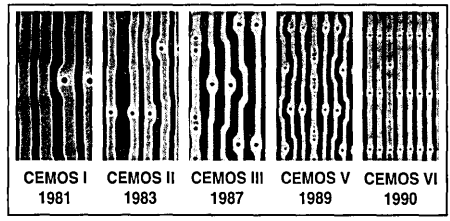
	CEMOS I	CEMOS II		CEMOS III	CEMOS V	CEMOS VI
		A	C			
Calendar Year	**1981**	**1983**	**1985**	**1987**	**1989**	**1990**
Drawn Feature Size	2.5μ	1.7μ	1.3μ	1.2μ	1.0μ	0.8μ
Leff	1.3μ	1.1μ	0.9μ	0.8μ	0.6μ	0.45μ
Basic Proces Enhancements	Dual-well, Wet Etch, Projection Aligned	Dry Etch, Stepper	Shrink, Spacer	Silicide, BPSG, BiCEMOS I	BiCEMOS II	BiCEMOS III

2514 drw 01

CEMOS IV = CEMOS III – scaled process optimized for high-speed logic.

Figure 1.

Continual advancement of CEMOS technology allows IDT to implement progressively higher levels of integration and achieve increasingly faster speeds maintaining the company's established position as the leader in high-speed CMOS integrated circuits. In addition, the fundamental process technology has been extended to add bipolar elements to the CEMOS platform. IDT's BiCEMOS process combines the ultra-high speeds of bipolar devices with the lower power and cost of CMOS, allowing us to build even faster components than straight CMOS at a slightly higher cost.



SEM photos (miniaturization)

2514 drw 02

Figure 2. Fifteen-Hundred-Power Magnification Scanning Electron Microscope (SEM) Photos of the Four Generations of IDT's CEMOS Technology

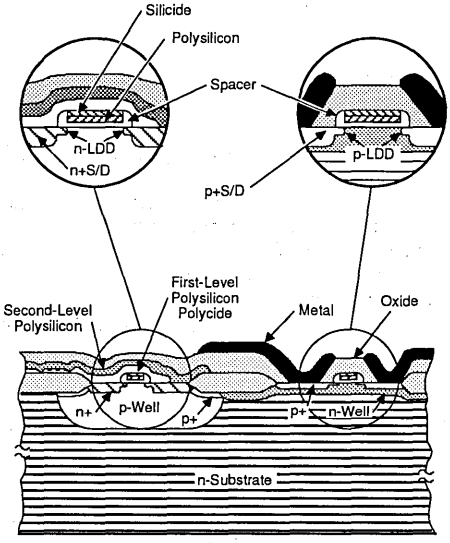


Figure 3. IDT CEMOS Device Cross Section

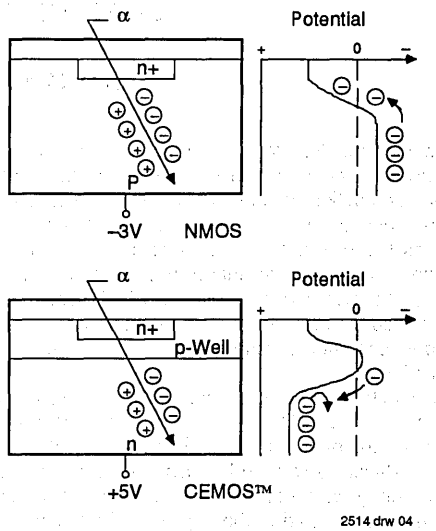


Figure 4. IDT CEMOS Built-in High Alpha Particle Immunity

ALPHA PARTICLES

Random alpha particles can cause memory cells to temporarily lose their contents or suffer a "soft error." Traveling with high energy levels, alpha particles penetrate deep into an integrated chip. As they burrow into the silicon, they leave a trail of free electron-hole pairs in their wake.

The cause of alpha particles is well documented and understood in the industry. IDT has considered various techniques to protect the cells from this hazardous occurrence. These techniques include dual-well structures (Figures 3 and 4) and a polymeric compound for die coating. Presently, a polymeric compound is used in many of IDT's SRAMs; however, the specific techniques used may vary and change from one device generation to the next as the industry and IDT improve the alpha particle protection technology.

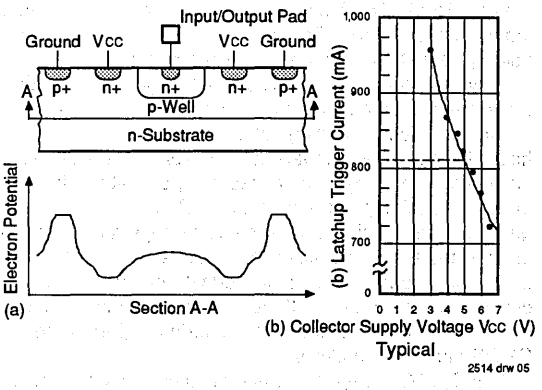


Figure 5. IDT CEMOS Latchup Suppression

LATCHUP IMMUNITY

A combination of careful design layout, selective use of guard rings and proprietary techniques have resulted in virtual elimination of latchup problems often associated with older CMOS processes (Figure 5). The use of NPN and N-channel I/O devices eliminates hole injection latchup. Double guard ring structures are utilized on all input and output circuits to absorb injected electrons. These effectively cut off the current paths into the internal circuits to essentially isolate I/O circuits. Compared to older CMOS processes which exhibit latchup characteristics with trigger currents from 10-20mA, IDT products inhibit latchup at trigger currents substantially greater than this.

SURFACE MOUNT TECHNOLOGY AND IDT'S MODULE PRODUCTS

Requirements for circuit area reduction, utilizing the most efficient and compact component placement possible and the needs of production manufacturing for electronics assemblies are the driving forces behind the advancement of circuit-board assembly technologies. These needs are closely associated with the advances being made in surface mount devices (SMD) and surface mount technology (SMT) itself. Yet, there are two major issues with SMT in production manufacturing of electronic assemblies: high capital expenditures and complexity of testing.

The capital expenditure required to convert to efficient production using SMT is still too high for the majority of electronics companies, regardless of the 20–60% increase in the board densities which SMT can bring. Because of this high barrier to entry, we will continue to see a large market segment [large even compared to the exploding SMT market] using traditional through-hole packages (i.e. DIPs, PGAs, etc) and assembly techniques. How can these types of companies take advantage of SMD and SMT? Let someone else, such as IDT, do it for them by investing time and money in SMT and then in return offer through-hole products utilizing SMT processes. Products which fit this description are multi-chip modules, consisting of SMT assembled SMDs on a through-hole type substrate. Modules enable companies to enjoy SMT density advantages and traditional package options without the expensive startup costs required to do SMT in-house.

Although subcontracting this type of work to an assembly house is an alternative, there still is the other issue of testing, an area where many contract assembly operations fall short of IDT's capability and experience. Prerequisites for adequate module testing sophisticated high-performance parametric testers, customized test fixtures, and most importantly the experience to tests today's complex electronic devices. Companies can therefore take advantage of IDT's experience in testing and manufacturing high-performance CMOS multi-chip modules.

At IDT, SMD components are electrically tested, environmentally screened, and performance selected for each IDT module. All modules are 100% tested as if they are a separate functional component and are guaranteed to meet all specified parameters at the module output without the customer having to understand the modules' internal workings.

Other added benefits companies get by using IDT's CMOS module products are:

1) a wide variety of high-performance, through-hole products utilizing SMD packaged components,
2) fast speeds compared with NMOS based products,
3) low power consumption compared with bipolar technologies, and
4) low cost manufacturability compared with GaAs-based products.

IDT has recognized the problems of SMT and began offering CMOS modules as part of its standard product portfolio. IDT modules combine the advantages of:

1) the low power characteristics of IDT's CEMOS™ and BiCEMOS™ products,
2) the density advantages of first class SMD components including those from IDT's components divisions, and
3) experience in system level design, manufacturing, and testing with its own in-house SMT operation.

IDT currently has two divisions (Subsystems and RISC Subsystems) dedicated to the development of module products ranging from simple memory modules to complex VME sized application specific modules to full system-level CPU boards. These modules have surface mount devices assembled on both sides of either a multi-layer glass filled epoxy (FR-4) or a multi-layer co-fired ceramic substrate. Assembled modules come available in industry standard through-hole packages and other space-saving module packages. Industry proven vapor-phase or IR reflow techniques are used to solder the SMDs to the substrate during the assembly process. Because of our affiliation with IDT's experienced semiconductor manufacturing divisions, we thoroughly understand and therefore test all modules to the applicable datasheet specifications and customer requirements.

Thus, IDT is able to offer today's electronic design engineers a unique solution for their "need-more-for-less" problem.modules. These high speed, high performance products offer the density advantages of SMD and SMT, the added benefit of low power CMOS technology, and through-hole packaged electronics without the high cost of doing it in-house.

STATE-OF-THE-ART FACILITIES AND CAPABILITIES

Integrated Device Technology is headquartered in Santa Clara, California—the heart of "Silicon Valley." The company's operations are housed in six facilities totaling over 500,000 square feet. These facilities house all aspects of business from research and development to design, wafer fabrication, assembly, environmental screening, test, and administration. In-house capabilities include scanning electron microscope (SEM) evaluation, particle impact noise detection (PIND), plastic and hermetic packaging, military and commercial testing, burn-in, life test, and a full complement of environmental screening equipment.

The over-200,000-square-foot corporate headquarters campus is composed of three buildings. The largest facility on this site is a 100,000 square foot, two-building complex. The first building, a 60,000-square-foot facility, is dedicated to the Standard Logic and RISC Microprocessor product lines, as well as hermetic and plastic package assembly, logic products' test, burn-in, mark, QA, and a reliability/failure analysis lab.

IDT's Packaging and Assembly Process Development teams are located here. To keep pace with the development of new products and to enhance the IDT philosophy of "innovation," these teams have ultra-modern, integrated and correspondingly sophisticated equipment and environments at their disposal. All manufacturing is completed in dedicated clean room areas (Class 10K minimum), with all preseal operations accomplished under Class 100 laminar flow hoods.

Development of assembly materials, processes and equipment is accomplished under a fully operational production environment to ensure reliability and repeatable product. The Hermetic Manufacturing and Process Development team is currently producing custom products to the strict requirements of MIL-STD-883. The fully automated plastic facility is currently producing high volumes of USA-manufactured product, while developing state-of-the-art surface-mount technology patterned after MIL-STD-883.

The second building of the complex houses sales, marketing, finance, MIS, and Northwest Area Sales.

The RISC Subsystems Division is located across from the two-building complex in a 50,000-square-foot facility. Also located at this facility are Quality Assurance and wafer fabrication services. Administrative services, Human Resources, International Planning, Shipping and Receiving departments are also housed in this facility.

IDT's largest and newest facility, opened in 1990 in San Jose, California, is a multi-purpose 150,000-square-foot, ultra-modern technology development center. This facility houses a 25,000 square foot, combined Class 1 (a maximum of one particle-per-cubic-foot of 0.2 micron or larger), sub-half-micron R&D fabrication facility and a wafer fabrication area. This fab supports both production volumes of IDT products, including some next-generation SRAMs, and the R&D efforts of the technology development staff. Technology development efforts targeted for the center include advanced silicon processing and wafer fabrication techniques. A test area to support both production and research is located on-site. The building is also the home of the FIFO, ECL, and Subsystems product lines.

IDT's second largest facility is located in Salinas, California, about an hour south of Santa Clara. This 95,000-square-foot facility, located on 14 acres, houses the Static RAM Division and Specialty Memory product line. Constructed in 1985, this facility contains an ultra-modern 25,000-square-foot high-volume wafer fabrication area measured at Class 2-to-3 (a maximum of 2 to 3 particles-per-cubic-foot of 0.2 micron or larger) clean room conditions. Careful design and construction of this fabrication area created a clean room environment far beyond the 1985 average for U.S. fab areas. This made possible the production of large volumes of high-density submicron geometry, fast static RAMs. This facility also houses shipping areas for IDT's leadership family of CMOS static RAMs. This site can expand to accommodate a 250,000-square-foot complex.

To extend our capabilities while maintaining strict control of our processes, IDT has an operational Assembly and Test facility located in Penang, Malaysia. This facility assembles product to U.S. standards, with all assemblies done under laminar flow conditions (Class 100) until the silicon is encased in its final packaging. All products in this facility are manufactured to the quality control requirements of MIL-STD-883.

All of IDT's facilities are aimed at increasing our manufacturing productivity to supply ever-larger volumes of high-performance, cost-effective, leadership CMOS products.

SUPERIOR QUALITY AND RELIABILITY

Maintaining the highest standards of quality in the industry on all products is the basis of Integrated Device Technology's manufacturing systems and procedures. From inception, quality and reliability are built into all of IDT's products. Quality is "designed in" at every stage of manufacturing – as opposed to being "tested-in" later – in order to ensure impeccable performance.

Dedicated commitment to fine workmanship, along with development of rigid controls throughout wafer fab, device assembly and electrical test, create inherently reliable products. Incoming materials are subjected to careful inspections. Quality monitors, or inspections, are performed throughout the manufacturing flow.

IDT military grade monolithic hermetic products are designed to meet or exceed the demanding Class B reliability levels of MIL-STD-883 and MIL-M-38510, as defined by Paragraph 1.2.1 of MIL-STD-883.

Product flow and test procedures for all monolithic hermetic military grade products are in accordance with the latest revision and notice of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with tight controls and inspections to ensure that products meet the requirements for 100% screening. Routine quality conformance lot testing is performed as defined in MIL-STD-883, Methods 5004 and 5005.

For IDT module products, screening of the fully assembled substrates is performed, in addition to the monolithic level screening, to assure package integrity and mechanical reliability. All modules receive 100% electrical tests (DC, functional and dynamic switching) to ensure compliance with the "subsystem" specifications.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that commercial, industrial and military grade products consistently meet customer requirements for quality, reliability and performance.

SPECIAL PROGRAMS

Class S. IDT also has all manufacturing, screening and test capabilities in-house (except X-ray and some Group D tests) to perform complete Class S processing per MIL-STD-883 on all IDT products and has supplied Class S products on several programs.

Radiation Hardened. IDT has developed and supplied several levels of radiation hardened products for military/aerospace applications to perform at various levels of dose rate, total dose, single event upset (SEU), upset and latchup. IDT products maintain nearly their same high-performance levels built to these special process requirements. The company has in-house radiation testing capability used both in process development and testing of deliverable product. IDT also has a separate group within the company dedicated to supplying products for radiation hardened applications and to continue research and development of process and products to further improve radiation hardening capabilities.

QSP–QUALITY, SERVICE AND PERFORMANCE

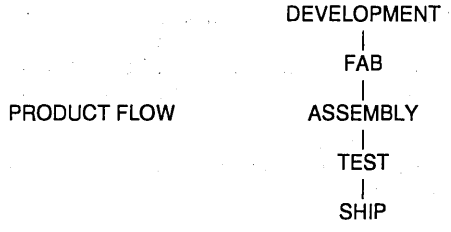
Quality from the beginning, is the foundation for IDT's commitment to supply consistently high-quality products to our customers. IDT's quality commitment is embodied in its all pervasive Continuous Quality Improvement (CQI) process. Everyone who influences the quality of the product–from the designer to the shipping clerk–is committed to constantly improving the quality of their actions.

IDT QUALITY PHILOSOPHY

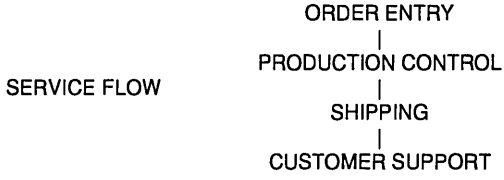
"To make quantitative constant improvement in the quality of our actions that result in the supply of leadership products in conformance to the requirements of our customers."

IDT's ASSURANCE STRATEGY FOR CQI

Measurable standards are essential to the success of CQI. All the processes contributing to the final quality of the product need to be monitored, measured and improved upon through the use of statistical tools.



Our customers receive the benefit of our optimized systems. Installed to enhance quality and reliability, these systems provide accurate and timely reporting on the effectiveness of manufacturing controls and the reliability and quality performance of IDT products and services.



These systems and controls concentrate on CQI by focusing on the following key elements:

Statistical Techniques
Using statistical techniques, including Statistical Process Control (SPC) to determine whether the product/ processes are under control.

Standardization
Implementing policies, procedures and measurement techniques that are common across different operational areas.

Documentation
Documenting and training in policies, procedures, measurement techniques and updating through characterization/ capability studies.

Productivity Improvement
Using constant improvement teams made up from employees at all levels of the organization.

Leadership
Focusing on quality as a key business parameter and strategic strength.

Total Employee Participation
Incorporating the CQI process into the IDT Corporate Culture.

Customer Service
Supporting the customer, as a partner, through performance review and pro-active problem solving.

People Excellence
Committing to growing, motivating and retaining people through training, goal setting, performance measurement and review.

PRODUCT FLOW

Product quality starts here. IDT has mechanisms and procedures in place that monitor and control the quality of our development activities. From the calibration of design capture libraries through process technology and product characterization that establish whether the performance, ratings and reliability criteria have been met. This includes failure analysis of parts that will improve the prototype product.

At the pre-production stage once again in-house qualification tests assure the quality and reliability of the product. All specifications and manufacturing flows are established and personnel trained before the product is placed into production.

Manufacturing
To accomplish CQI during the manufacturing stage, control items are determined for major manufacturing conditions. Data is gathered and statistical techniques are used to control specific manufacturing processes that affect the quality of the product.

In-process and final inspections are fed back to earlier processes to improve product quality. All product is burned-in (where applicable) before 100% inspection of electrical characteristics takes place.

Products which pass final inspection are then subject to Quality Assurance and Reliability Tests. This data is used to improve manufacturing processes and provide reliability predictions of field applications.

Inventory and Shipping

Controls in shipping focus on ensuring parts are identified and packaged correctly. Care is also taken to see that the correct paperwork is present and the product being shipped was processed correctly.

SERVICE FLOW

Quality not only applies to the product but to the quality-of-service we give our customers. Service is also constantly monitored for improvement.

Order Procedures

Checks are made at the order entry stage to ensure the correct processing of the Customer's product. After verification and data entry the Acknowledgements (sent to Customers) are again checked to ensure details are correct. As part of the CQI process, the results of these verifications are analyzed using statistical techniques and corrective actions are taken.

Production Control

Production Control (P.C.) is responsible for the flow and logistics of material as it moves through the manufacturing processes. The quality of the actions taken by P.C. greatly influences the quality of service the customer receives. Because many of our customers have implemented Just-in-Time (JIT) manufacturing practices, IDT as a supplier has adopted these same disciplines. As a result, employees receive extensive training and the performance level of key actions are kept under constant review. These key actions include:

Quotation response and accuracy.
Scheduling response and accuracy.
Response and accuracy of Expedites.
Inventory, management, and effectiveness.
On-time delivery.

Customer Support

IDT has a worldwide network of sales offices and Technical Development Centers. These provide local customer support on business transactions, and in addition, support customers on applications information, technical services, benchmarking of hardware solutions, and demonstration of various Development Workstations.

The key to CQI is the timely resolution of defects and implementation of the corrective actions. This is no more important than when product failures are found by a customer. When failures are found at the customer's incoming inspection, in the production line, or the field application, the Division Quality Assurance group is the focal point for the investigation of the cause of failure and implementation of the corrective action. IDT constantly improves the level of support we give our customers by monitoring the response time to customers who have detected a product failure. Providing the customer with an analysis of the failure, including corrective actions and the statistical analysis of defects, brings CQI full circle–full support of our customers and their designs with high-quality products.

SUMMARY

In 1990, IDT made the commitment to *"Leadership through Quality, Service, and Performance Products"*.

We believe by following this credo IDT and our customers will be successful in the coming decade. With the implementation of the CQI strategy within the company, we will satisfy our goal...

"Leadership through Quality, Service and Performance Products".

IDT QUALITY CONFORMANCE PROGRAM

A COMMITMENT TO QUALITY

Integrated Device Technology's monolithic assembly products are designed, manufactured and tested in accordance with the strict controls and procedures required by Military Standards. The documentation, design and manufacturing criteria of the Quality and Reliability Assurance Program were developed and are being maintained to the most current revisions of MIL-38510 as defined by paragraph 1.2.1 of MIL-STD-883 and MIL-STD-883 requirements.

Product flow and test procedures for all Class B *monolithic* hermetic Military Grade microcircuits are in full compliance with paragraph 1.2.1 of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with stringent controls and inspections to ensure that products meet the requirements for 100% screening and quality conformance tests as defined in MIL-STD-883, Methods 5004 and 5005.

Product flow and test procedures for all *plastic* and *commercial hermetic* products are in accordance with industry practices for producing highly reliable microcircuits to ensure that products meet the IDT requirements for 100% screening and quality conformance tests.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that our products consistently meet customer requirements for quality, reliability and performance.

SUMMARY

Monolithic Hermetic Package Processing Flow[1]

Refer to the Monolithic Hermetic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die Visual Inspection:** Wafers are cut and separated and the individual die are 100% visually inspected to strict IDT-defined internal criteria.

3. **Die Shear Monitor:** To ensure die attach integrity, product samples are routinely subjected to a shear strength test per Method 2019.

4. **Wire Bond Monitor:** Product samples are routinely subjected to a strength test per Method 2011, Condition D, to ensure the integrity of the lead bond process.

5. **Pre-Cap Visual:** Before the completed package is sealed, 100% of the product is visually inspected to Method 2010, Condition B criteria.

6. **Environmental Conditioning:** 100% of the sealed product is subjected to environmental stress tests. These thermal and mechanical tests are designed to eliminate units with marginal seal, die attach or lead bond integrity.

7. **Hermetic Testing:** 100% of the hermetic packages are subjected to fine and gross leak seal tests to eliminate marginally sealed units or units whose seals may have become defective as a result of environmental conditioning tests.

8. **Pre-Burn-In Electrical Test:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

9. **Burn-In:** 100% of the Military Grade product is burned-in under dynamic electrical conditions to the time and temperature requirements of Method 1015, Condition D. Except for the time, Commercial Grade product is burned-in as applicable to the same conditions as Military Grade devices.

10. **Post-Burn-In Electrical:** After burn-in, 100% of the Class B Military Grade product is electrically tested to IDT data sheet or customer specifications over the –55°C to +125°C temperature range. Commercial Grade products are sample tested to the applicable temperature extremes.

11. **Mark:** All product is marked with product type and lot code identifiers. MIL-STD-883 compliant Military Grade products are identified with the required compliant code letter.

12. **Quality Conformance Tests:** Samples of the Military Grade product which have been processed to the 100% screening tests of Method 5004 are routinely subjected to the quality conformance requirements of Method 5005.

NOTE:

1. For quality requirements beyond Class B levels such as SEM analysis, X-Ray inspection, Particle Impact Noise Reduction (PIND) test, Class S screening or other customer specified screening flows, please contact your Integrated Device Technology sales representative.

SUMMARY

Monolithic Plastic Package Processing Flow

Refer to the Monolithic Plastic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Topside silicon nitride passivation is all applied to all wafers for better moisture barrier characteristics.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die Visual Inspection:** Wafers are 100% visually inspected to strict IDT defined internal criteria.

3. **Die Push Test:** To ensure die attach integrity, product samples are routinely subjected to die push tests, patterned after MIL-STD-883, Method 2019.

4. **Wire Bond Monitor:** Product samples are routinely subjected to wire bond pull and ball shear tests to ensure the integrity of the wire bond process, patterned after MIL-STD-883, Method 2011, Condition D.

5. **Pre-Cap Visual:** Before encapsulation, all product lots are visually inspected (using LTPD 5 sampling plan) to criteria patterned after MIL-STD-883, Method 2010, Condition B.

6. **Post Mold Cure:** Plastic encapsulated devices are baked to ensure an optimum polymerization of the epoxy mold compound so as to enhance moisture resistance characteristics.

7. **Pre-Burn-In Electrical:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

8. **Burn-In:** Except for MSI Logic family devices where it may be obtained as an option, all Commercial Grade plastic package products are burned-in for 16 hours at +125°C minimum (or equivalent), utilizing the same burn-in conditions as the Military Grade product.

9. **Post-Burn-In Electrical:** After burn-in, 100% of the plastic product is electrically tested to IDT data sheet or customer specifications at the maximum temperature extreme. The minimum temperature extreme is tested periodically on an audit basis.

10. **Mark:** All product is marked with product type and lot code identifiers. Products are identified with the assembly and test locations.

11. **Quality Conformance Inspection:** Samples of the plastic product which have been processed to the 100% screening requirements are subjected to the Periodic Quality Conformance Inspection Program. Where indicated, the test methods are patterned after MIL-STD-883 criteria.

TABLE 1

This table defines the device class screening procedures for IDT's high reliability products in conformance with MIL-STD-883C.

Monolithic Hermetic Package Final Processing Flow

	CLASS-S		CLASS-B		CLASS-C [1]	
OPERATION	**TEST METHOD**	**RQMT**	**TEST METHOD**	**RQMT**	**TEST METHOD**	**RQMT**
BURN-IN	1015 Cond. D, 240 Hrs @ 125°C or equivalent	100%	1015 Cond. D, 160 Hrs. @ 125°C min or equivalent	100%	Per applicable device specification	100%
POST BURN-IN ELECTRICAL: Static (DC), Functional and Switching (AC)	Per applicable device specification +25, -55 and 125°C	100%	Per applicable device specification +25, -55 and 125°C	100%	Per applicable [2] device specification	100%
Group A ELECTRICAL: Static (DC), Functional and Switching (AC)	Per applicable device specification and 5005	Sample	Per applicable device specification and 5005	Sample	Per applicable [2] device specification	Sample
MARK/LEAD STRAIGHTENING	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%
FINAL ELECTRICAL TEST	Per applicable device specification +25°C	100%	Per applicable device specification +25°C	100%	Per applicable device specification +25°C	100%
FINAL VISUAL/PACK	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%
QUALITY CONFORMANCE INSPECTION	5005 Group B, C, D.	Sample	5005 Group B,C,D.	Sample	IDT Spec	Sample
QUALITY SHIPPING INSPECTION (Visual/Plant Clearance)	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%

NOTES:
1. Class-C = IDT commercial spec. for hermetic and plastic packages
2. Typical 0°C, 70°C, Extended -55°C +125°C

RADIATION TOLERANT/ENHANCED/HARDENED PRODUCTS FOR RADIATION ENVIRONMENTS

INTRODUCTION

The need for high-performance CMOS integrated circuits in military and space systems is more critical today than ever before. The low power dissipation that is achieved using CMOS technology, along with the high complexity and density levels, makes CMOS the nearly ideal component for all types of applications.

Systems designed for military or space applications are intended for environments where high levels of radiation may be encountered. The implication of a device failure within a military or space system clearly is critical. IDT has made a significant contribution toward providing reliable radiation-tolerant systems by offering integrated circuits with enhanced radiation tolerance. Radiation environments, IDT process enhancements and device tolerance levels achieved are described below.

THE RADIATION ENVIRONMENT

There are four different types of radiation environments that are of concern to builders of military and space systems. These environments and their effects on the device operation, summarized in Figure 1, are as follows:

Total Dose Accumulation refers to the total amount of accumulated gamma rays experienced by the devices in the system, and is measured in RADS (SI) for radiation units experienced at the silicon level. The physical effect of gamma rays on semiconductor devices is to cause threshold shifts (Vt shifts) of both the active transistors as well as the parasitic field transistors. Threshold voltages decrease as total dose is accumulated; at some point, the device will begin to exhibit parametric failures as the input/output and supply currents increase. At higher radiation accumulation levels, functional failures occur. In memory circuits, however, functional failures due to memory cell failure often occur first.

Burst Radiation or Dose Rate refers to the amount of radiation, usually photons or electrons, experienced by the devices in the system due to a pulse event, and is measured in RADS (Si) per second. The effect of a high dose rate or burst of radiation on CMOS integrated circuits is to cause temporary upset of logic states and/or CMOS latch-up. Latch-up can cause permanent damage to the device.

Single Event Upset (SEU) is a transient logic state change caused by high-energy ions, such as energetic cosmic rays, striking the integrated circuits. As the ion passes through the silicon, charge is either created through ionization or direct nuclear collision. If collected by a circuit node, this excess charge can cause a change in logic state of the circuit. Dynamic nodes that are not actively held at a particular logic state (dynamic RAM cells for example) are the most susceptible. These upsets are transient, but can cause system failures known as "soft errors."

Neutron Irradiation will cause structural damage to the silicon lattice which may lead to device leakage and, ultimately, functional failure.

Radiation Category	Primary Particle	Source	Effect
Total Dose	Gamma	Space or Nuclear Event	Permanent
Dose Rate	Photons	Nuclear Event	Temporary Upset of Logic State or Latch-up
SEU	Cosmic Rays	Space	Temporary Upset of Logic State
Neutron	Neutrons	Nuclear Event	Device Leakage Due to Silicon Lattice Damage

2510 drw 01

Figure 1.

DEVICE ENHANCEMENTS

Of the four radiation environments above, IDT has taken considerable data on the first two, Total Dose Accumulation and Dose Rate. IDT has developed a process that significantly improves the radiation tolerance of its devices within these environments. Prevention of SEU failures is usually accomplished by system-level considerations, such as Error Detection and Correction (EDC) circuitry, since the occurrence of SEUs is not particularly dependent on process technology. Through IDT's customer contracts, SEU has been gathered on some devices. Little is yet known about the effects of neutron-induced damage. For more information on SEU testing, contact IDT's Radiation Hardened Product Group.

Enhancements to IDT's standard process are used to create radiation enhanced and tolerant processes. Field and gate oxides are "hardened" to make the device less susceptible to radiation damage by modifying the process architecture to allow lower temperature processing. Device implants and Vts adjustments allow more Vt margin. In addition to process changes, IDT's radiation enhanced process utilizes epitaxial substrate material. The use of epi substrate material provides a lower substrate resistance environment to create latch-up free CMOS structures.

RADIATION HARDNESS CATEGORIES

Radiation Enhanced (RE) or Radiation Tolerant ('RT) versions of IDT products follow IDT's military product data sheets whenever possible (consult factory). IDT's Total Dose Test plan exposes a sample of die on a wafer to a particular Total Dose level via ARACOR X-Ray radiation. This Total Dose Test plan qualifies each 'RE or 'RT wafer to a Total Dose level. Only wafers with sampled die that pass Total Dose level tests are assembled and used for orders (consult factory for more details on Total Dose sample testing). With regard to Total Dose testing, clarifications/exceptions to MIL-STD-883,

Methods 5005 and 1019 are required. Consult factory for more details.

The 'RE and 'RT process enhancements enable IDT to offer integrated circuits with varying grades of radiation tolerance or radiation "hardness".

- Radiation Enhanced process uses Epi wafers and is able to provide devices that can be Total Dose qualified to 10K RADs (Si) or greater by IDT's ARACOR X-Ray Total Dose sample die test plan (Total Dose levels require negotiation, consult factory for more details).
- Radiation Tolerant product uses standard wafer/process material that is qualified to 10K RADs (Si) Total Dose by IDT's ARACOR X-Ray Total Dose sample die test plan.

Integrated Device Technology can provide Radiation Tolerant/Enhanced versions of all product types (some speed grades may not be available as 'RE).

Please contact your IDT sales representative or factory marketing to determine availability and price of any IDT product processed in accordance with one of these levels of radiation hardness.

CONCLUSION

There has been widespread interest within the military and space community in IDT's CMOS product line for its radiation hardness levels, as well as its high-performance and low power dissipation. To serve this growing need for CMOS circuits that must operate in a radiation environment, IDT has created a separate group within the company to concentrate on supplying products for these applications.Continuing research and development of process and products, including the use of in-house radiation testing capability, will allow Integrated Device Technology to offer continuously increasing levels of radiation-tolerant solutions.

THERMAL PERFORMANCE CALCULATIONS FOR IDT'S PACKAGES

Since most of the electrical energy consumed by microelectronic devices eventually appears as heat, poor thermal performance of the device or lack of management of this thermal energy can cause a variety of deleterious effects. This device temperature increase can exhibit itself as one of the key variables in establishing device performance and long term reliability; on the other hand, effective dissipation of internally generated thermal energy can, if properly managed, reduce the deleterious effects and improve component reliability.

A few key benefits of IDT's enhanced CEMOS™ process are: low power dissipation, high speed, increased levels of integration, wider operating temperature ranges and lower quiescent power dissipation. Because the reliability of an integrated circuit is largely dependent on the maximum temperature the device attains during operation, and as the junction stability declines with increases in junction temperature (TJ), it becomes increasingly important to maintain a low (TJ).

CMOS devices stabilize more quickly and at greatly lower temperature than bipolar devices under normal operation. The accelerated aging of an integrated circuit can be expressed as an exponential function of the junction temperature as:

$$t_A = t_o \exp\left[\frac{E_a}{k}\left(\frac{1}{T_O} - \frac{1}{T_J}\right)\right]$$

where

- t_A = lifetime at elevated junction (T_J) temperature
- t_O = normal lifetime at normal junction (T_O) temperature
- E_a = activation energy (ev)
- k = Boltzmann's constant (8.617×10^{-5}ev/k)

i.e. the lifetime of a device could be decreased by a factor of 2 for every 10°C increase temperature.

To minimize the deleterious effects associated with this potential increase, IDT has:

1. Optimized our proprietary low-power CEMOS fabrication process to ensure the active junction temperature rise is minimal.
2. Selected only packaging materials that optimize heat dissipation, which encourages a cooler running device.
3. Physically designed all package components to enhance the inherent material properties and to take full advantage of heat transfer and radiation due to case geometries.
4. Tightly controlled the assembly procedures to meet or exceed the stringent criteria of MIL-STD-883_ to ensure maximum heat transfer between die and packaging materials.

The following figures graphically illustrate the thermal values of IDT's current package families. Each envelop (shaded area) depicts a typical spread of values due to the influence of a number of factors which include: circuit size, package materials and package geometry. The following range of values are to be used as a comprehensive characterization of the major variables rather than single point of reference.

When calculating junction temperature (T_J), it is necessary to know the thermal resistance of the package (θ_{JA}) as measured in "degree celsius per watt". With the accompanying data, the following equation can be used to establish thermal performance, enhance device reliability and ultimately provide you, the user, with a continuing series of high-speed, low-power CMOS solutions to your system design needs.

$$\theta_{JA} = [T_J - T_A]/P$$
$$T_J = T_A + P[\theta_{JA}] = T_A + P[\theta_{JC} + \theta_{CA}]$$

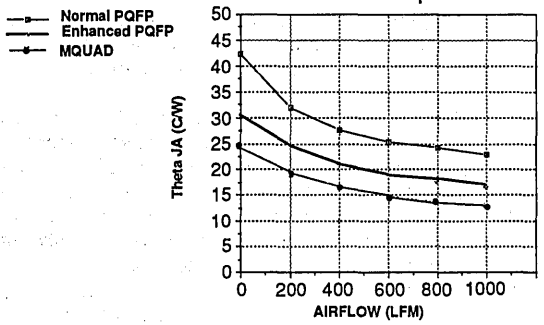
where

$$\theta_{JC} = \frac{T_J - T_C}{P} \qquad \theta_{CA} = \frac{T_C - T_A}{P}$$

- θ = Thermal resistance
- J = Junction
- P = Operational power of device (dissipated)
- T_A = Ambient temperature in degree celsius
- T_J = Temperature of the junction
- T_C = Temperature of case/package
- θ_{CA} = Case to Ambient, thermal resistance—usually a measure of the heat dissipation due to natural or forced convection, radiation and mounting techniques.
- θ_{JC} = Junction to Case, thermal resistance—usually measured with reference to the temperature at a specific point on the package (case) surface. (Dependent on the package material properties and package geometry.)
- θ_{JA} = Junction to Ambient, thermal resistance—usually measured with respect to the temperature of a specified volume of still air. (Dependent on θ_{JC} + θ_{JA} which includes the influence of area and environmental condition.)

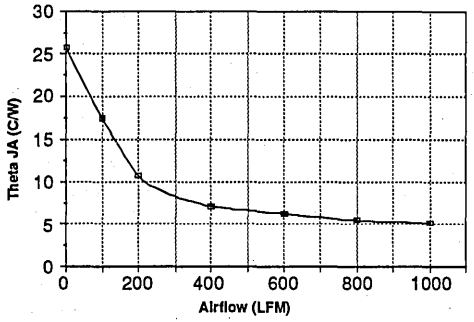
Ref. MIL-STD-883C, Method 1012.1
JEDEC ENG. Bulletin No. 20, January 1975
1986 Semi. Std., Vol. 4, Test Methods G30–86, G32–86.

Theta JA vs. Airflow
160 Pin Quad Flatpacks



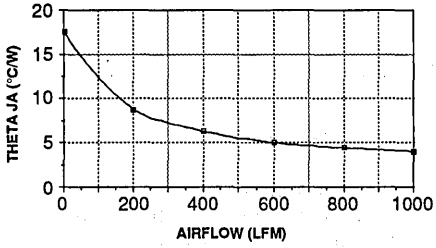
Delco Temp 09 Thermal Die (.250"sq.)
Parts mounted to standard 3" sq. test board.

Theta JA vs. Airflow
144 pin PGA - Cavity Down w/ CuW heatsink



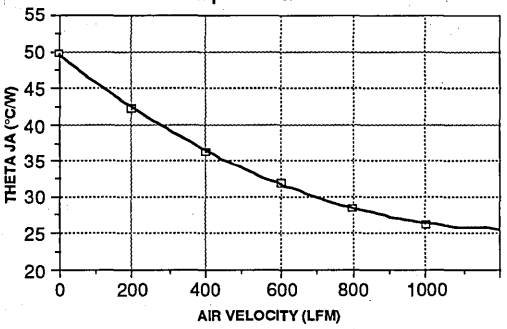
Measurements done with Delco Temp09 Thermal Die (.250"sq.)

THETA JA vs. AIRFLOW
179 PIN PGA - R4000 PACKAGE
INTEGRAL CuW HEATSINK - NO FIN ATTACHED



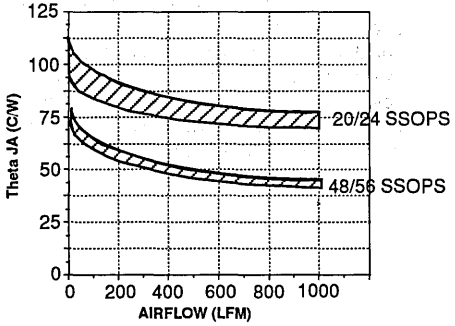
Delco Temp09 Thermal Die Array (.500"sq.)
applied power = 3W

THETA JA vs. AIR FLOW
32 pin J-bend SOIC



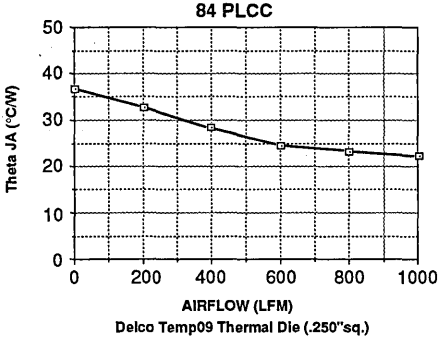
Theta JC was measured to be 17°C/W - Die size (.150"x.250")

Theta JA vs. Airflow
PLASTIC SSOP PACKAGES



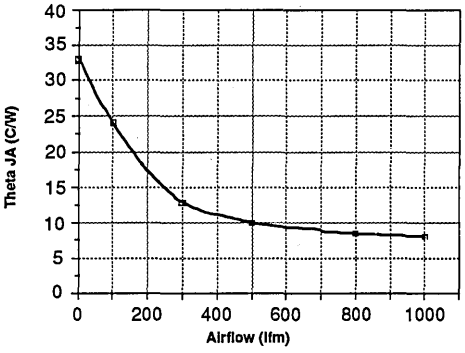
THETA JC : 20/24 PIN = 35-40 °C/W
48/56 PIN = 16-20 °C/W

THETA JA VS. AIRFLOW
84 PLCC



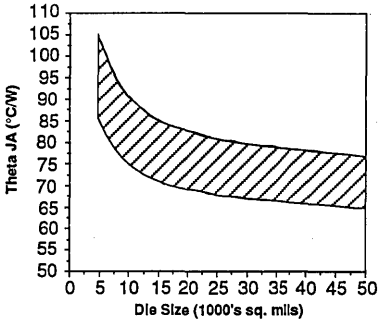
Delco Temp09 Thermal Die (.250"sq.)

Theta JA vs. Airflow
84 pin PGA - Cavity Down w/CuW heatsink

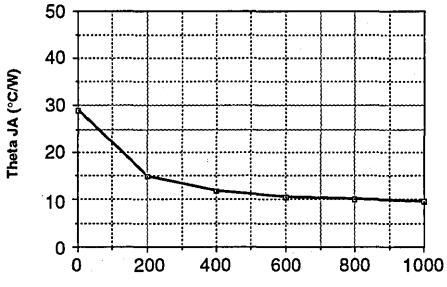


Measurements were done using Temp09 Delco Thermal Die (.250sq.)

Theta JA - Still Air 16-20 Lead Ceramic Dips

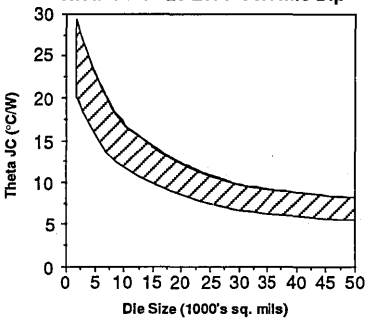


GD 208 THETA JA VS. AIRFLOW

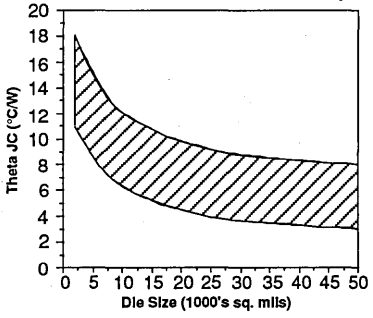


Delco Temp09 Thermal Die (.250"sq.)

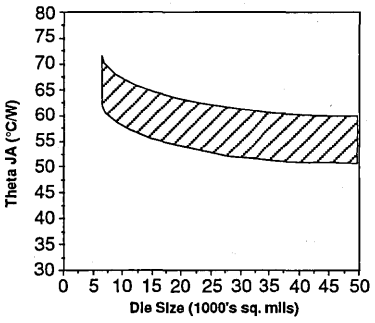
Theta JC 16-20 Lead Ceramic Dip



Theta JC 22-40 Lead Ceramic Dips

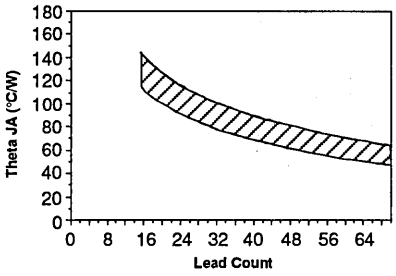


Theta JA - Still Air 22-40 Ceramic Dips

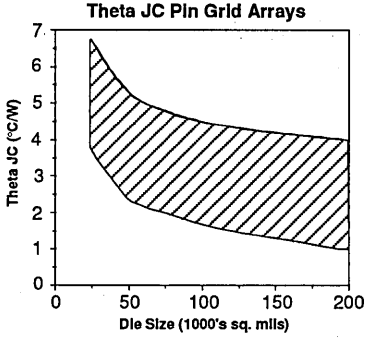


4

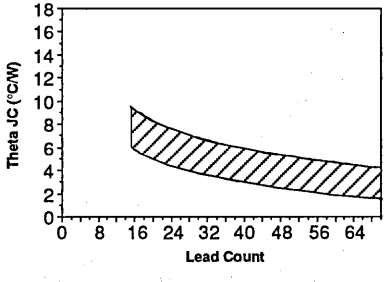
Theta JA Ceramic Flatpacks/Cerpacks



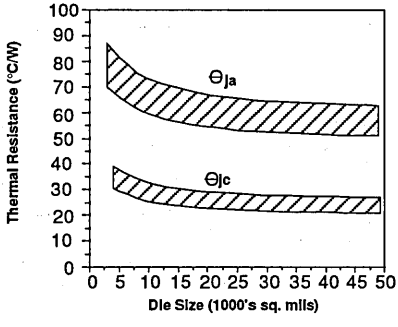
Theta JC Pin Grid Arrays



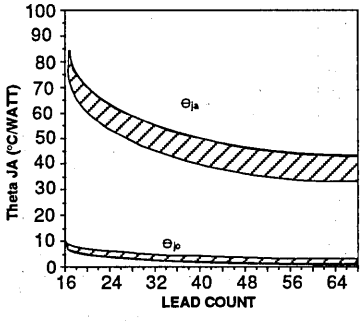
Theta JC Ceramic Flatpacks/Cerpacks



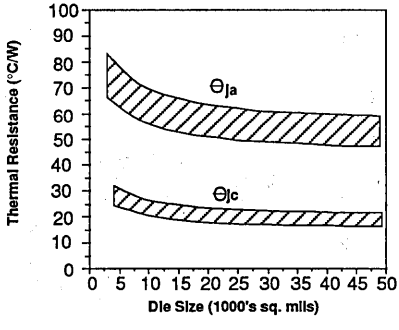
PLASTIC DIPS: 16,18 & 20 PINS



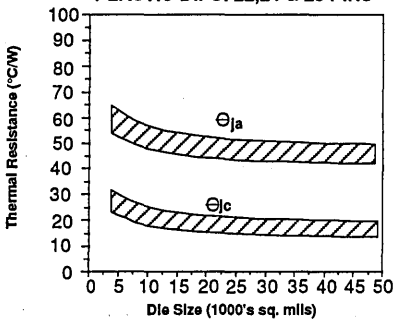
Thermal Resistance of Ceramic LCC's



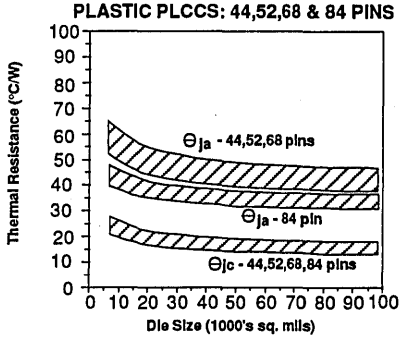
PLASTIC SOICS: 24,28 & 32 PINS



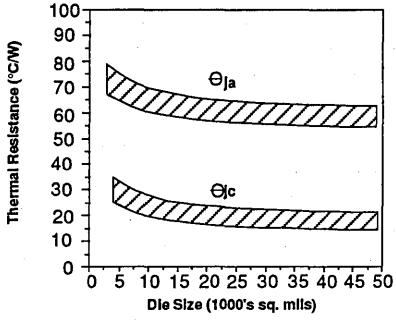
PLASTIC DIPS: 22,24 & 28 PINS



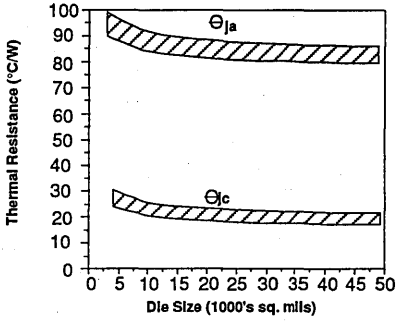
PLASTIC PLCCS: 44,52,68 & 84 PINS



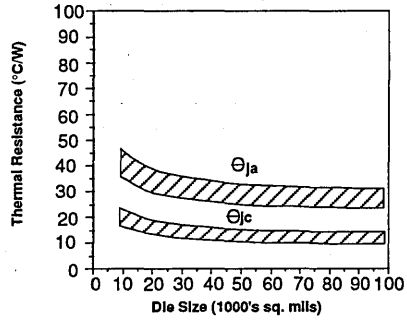
PLASTIC PLCCS: 28 & 32 PINS



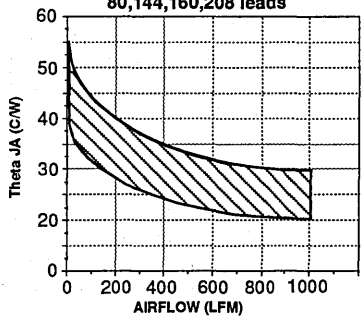
PLASTIC SOICS: 16 & 20 PINS



PLASTIC DIPS: 40,48 & 64 PINS



Theta JA vs. Airflow
Plastic Quad Flatpacks
80,144,160,208 leads



THETA JC : 15-25 °C/W

PACKAGE DIAGRAM OUTLINE INDEX

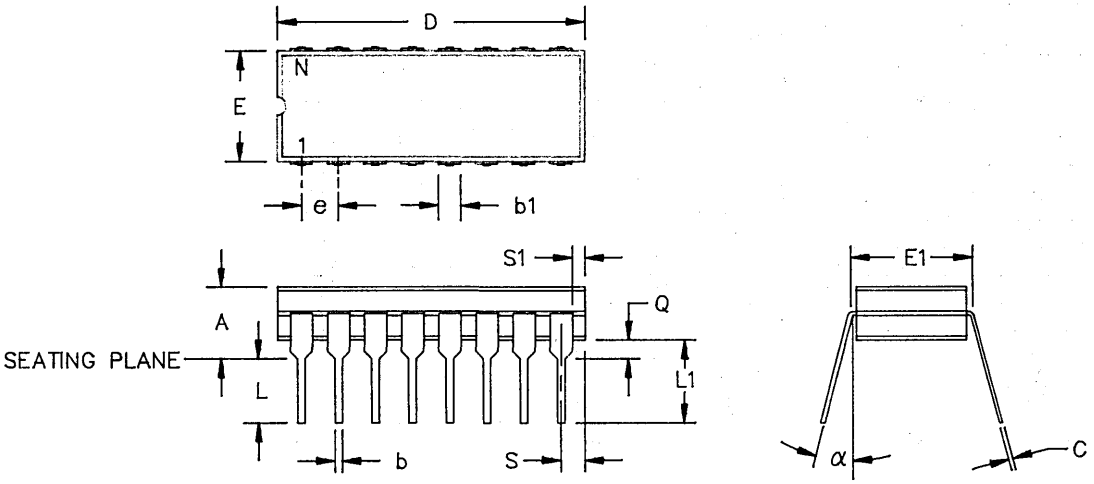
MODULE PACKAGE DIAGRAM OUTLINES

Module package diagrams are located at the back of each Subsystems data sheet.

Integrated Device Technology, Inc.

PACKAGE DIAGRAM OUTLINES

DUAL IN-LINE PACKAGES



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. THE MINIMUM LIMIT FOR DIMENSION b1 MAY BE .023 FOR CORNER LEADS.

16-28 LEAD CERDIP (300 MIL)

DWG #	D16-1		D18-1		D20-1		D22-1		D24-1		D28-3	
# OF LDS (N)	16		18		20		22		24		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.200	.140	.200	.140	.200	.140	.200	.140	.200	.140	.200
b	.015	.021	.015	.021	.015	.021	.015	.021	.015	.021	.015	.021
b1	.045	.060	.045	.060	.045	.060	.045	.060	.045	.065	.045	.065
C	.009	.012	.009	.012	.009	.012	.009	.012	.009	.014	.009	.014
D	.750	.830	.880	.930	.935	1.060	1.050	1.080	1.240	1.280	1.440	1.485
E	.285	.310	.285	.310	.285	.310	.285	.310	.285	.310	.285	.310
E1	.290	.320	.290	.320	.290	.320	.300	.320	.300	.320	.300	.320
e	.100	BSC	.100	BSC	.100	BSC	.100	BSC	.100	BSC	.100	BSC
L	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.015	.055	.015	.055	.015	.060	.015	.060	.015	.060	.015	.060
S	.020	.080	.020	.080	.020	.080	.020	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°

DUAL IN-LINE PACKAGES (Continued)

24-40 LEAD CERDIP (400 & 600 MIL)

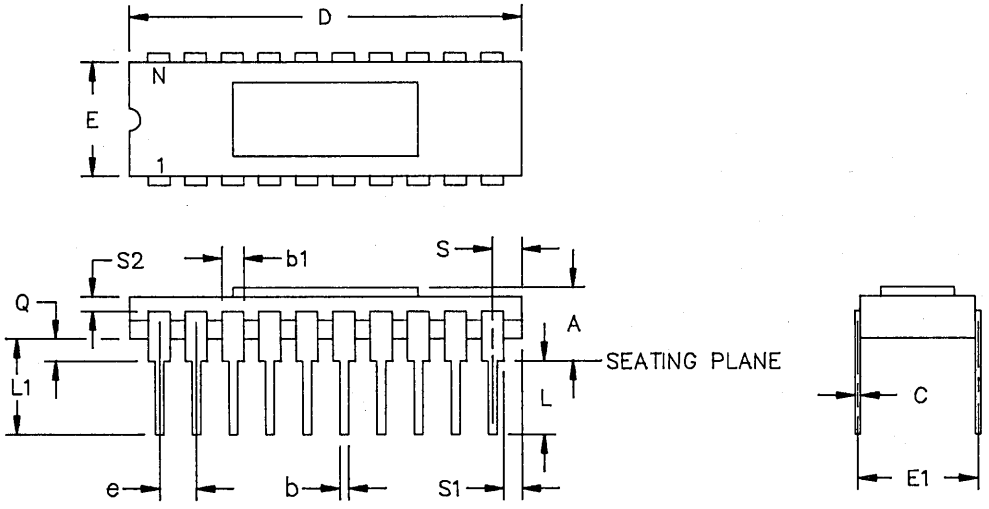
DWG #	D24-3		D24-2		D28-1		D40-1	
# OF LDS (N)	24		24		28		40	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.130	.175	.090	.190	.090	.200	.160	.220
b	.015	.021	.014	.023	.014	.023	.014	.023
b1	.045	.065	.045	.060	.045	.065	.045	.065
C	.009	.014	.008	.012	.008	.014	.008	.014
D	1.180	1.250	1.230	1.290	1.440	1.490	2.020	2.070
E	.350	.410	.500	.610	.510	.600	.510	.600
E1	.380	.420	.590	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.175	.125	.200	.125	.200	.125	.200
L1	.150	–	.150	–	.150	–	.150	–
Q	.015	.060	.015	.060	.020	.060	.020	.060
S	.030	.070	.030	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°	0°	15°

32 LEAD CERDIP (WIDE BODY)

DWG #	D32-1	
# OF LDS (N)	32	
SYMBOL	MIN	MAX
A	.120	.210
b	.014	.023
b1	.045	.065
C	.008	.014
D	1.625	1.675
E	.570	.600
E1	.590	.620
e	.100 BSC	
L	.125	.200
L1	.150	–
Q	.020	.060
S	.030	.080
S1	.005	–
α	0°	15°

DUAL IN-LINE PACKAGES (Continued)

20-32 LEAD SIDE BRAZE (300 MIL)

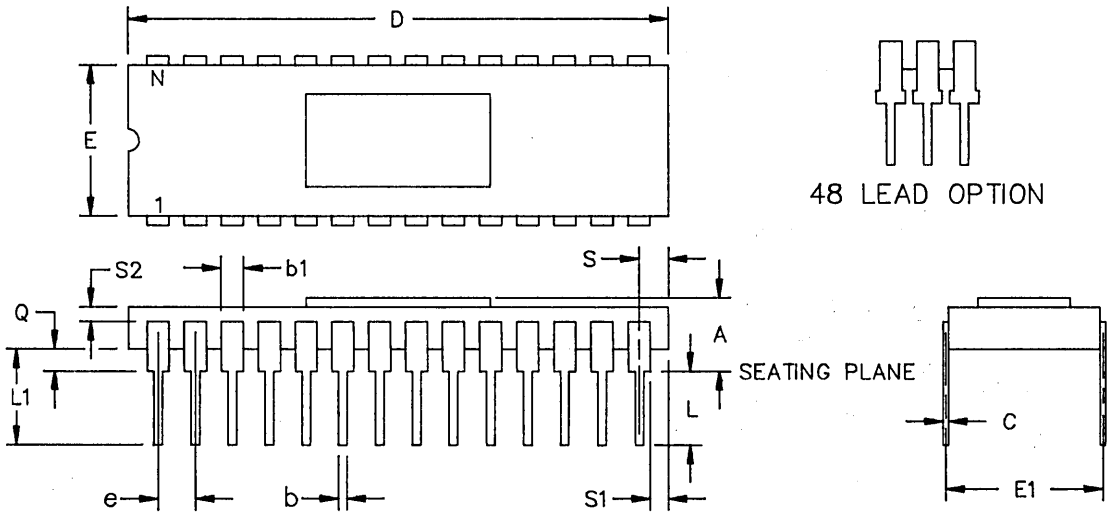


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C20-1		C22-1		C24-1		C28-1		C32-3	
# OF LDS (N)	20		22		24		28		32	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.100	.200	.090	.200	.090	.200	.090	.200
b	.014	.023	.014	.023	.015	.023	.014	.023	.014	.023
b1	.045	.060	.045	.060	.045	.060	.045	.060	.045	.060
C	.008	.015	.008	.015	.008	.015	.008	.015	.008	.014
D	.970	1.060	1.040	1.120	1.180	1.230	1.380	1.420	1.580	1.640
E	.260	.310	.260	.310	.220	.310	.220	.310	.280	.310
E1	.290	.320	.290	.320	.290	.320	.290	.320	.290	.320
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200	.125	.200	.100	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.015	.060	.015	.060	.015	.060	.015	.060	.030	.060
S	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–	.005	–	.005	–

DUAL IN-LINE PACKAGES (Continued)

28-48 LEAD SIDE BRAZE (400 MIL)

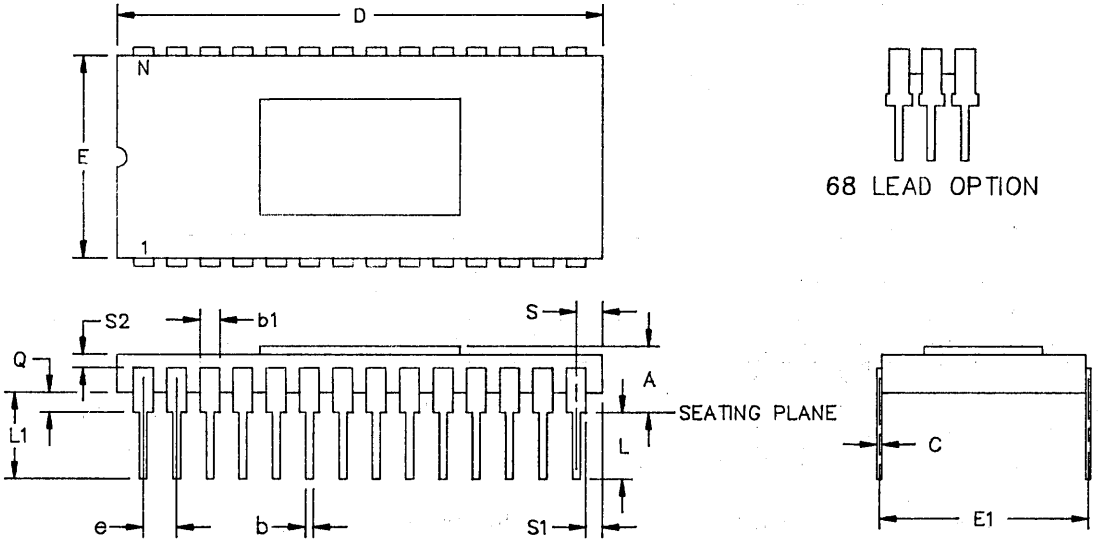


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C28-2		C32-2		C48-1	
# OF LDS (N)	28		32		48	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.090	.200	.085	.190
b	.014	.023	.014	.023	.014	.023
b1	.045	.060	.045	.060	.045	.060
C	.008	.014	.008	.014	.008	.014
D	1.380	1.420	1.580	1.640	1.690	1.730
E	.380	.420	.380	.410	.380	.410
E1	.390	.420	.390	.420	.390	.420
e	.100 BSC		.100 BSC		.070 BSC	
L	.100	.175	.100	.175	.125	.175
L1	.150	–	.150	–	.150	–
Q	.030	.060	.030	.060	.020	.070
S	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–

DUAL IN-LINE PACKAGES (Continued)

24-68 LEAD SIDE BRAZE (600 MIL)

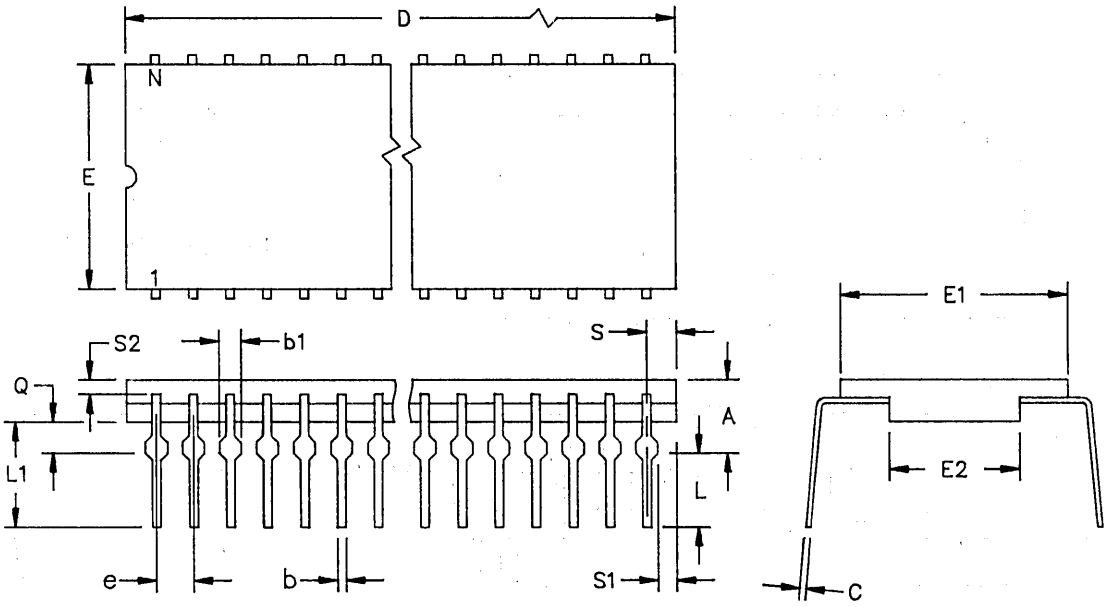


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C24-2		C28-3		C32-1		C40-1		C48-2		C68-1	
# OF LDS (N)	24		28		32		40		48		68	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.190	.085	.190	.100	.190	.085	.190	.100	.190	.085	.190
b	.015	.023	.015	.022	.015	.023	.015	.023	.015	.023	.015	.023
b1	.045	.060	.045	.060	.045	.060	.045	.060	.045	.060	.045	.060
C	.008	.012	.008	.012	.008	.014	.008	.012	.008	.012	.008	.012
D	1.180	1.220	1.380	1.430	1.580	1.640	1.980	2.030	2.370	2.430	2.380	2.440
E	.575	.610	.580	.610	.580	.610	.580	.610	.550	.610	.580	.610
E1	.595	.620	.595	.620	.590	.620	.595	.620	.595	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC		.070 BSC	
L	.125	.175	.125	.175	.100	.175	.125	.175	.125	.175	.125	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.020	.060	.020	.060	.020	.060	.020	.060	.020	.060	.020	.070
S	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–

DUAL IN-LINE PACKAGES (Continued)

64 LEAD TOP BRAZE (900 MIL)

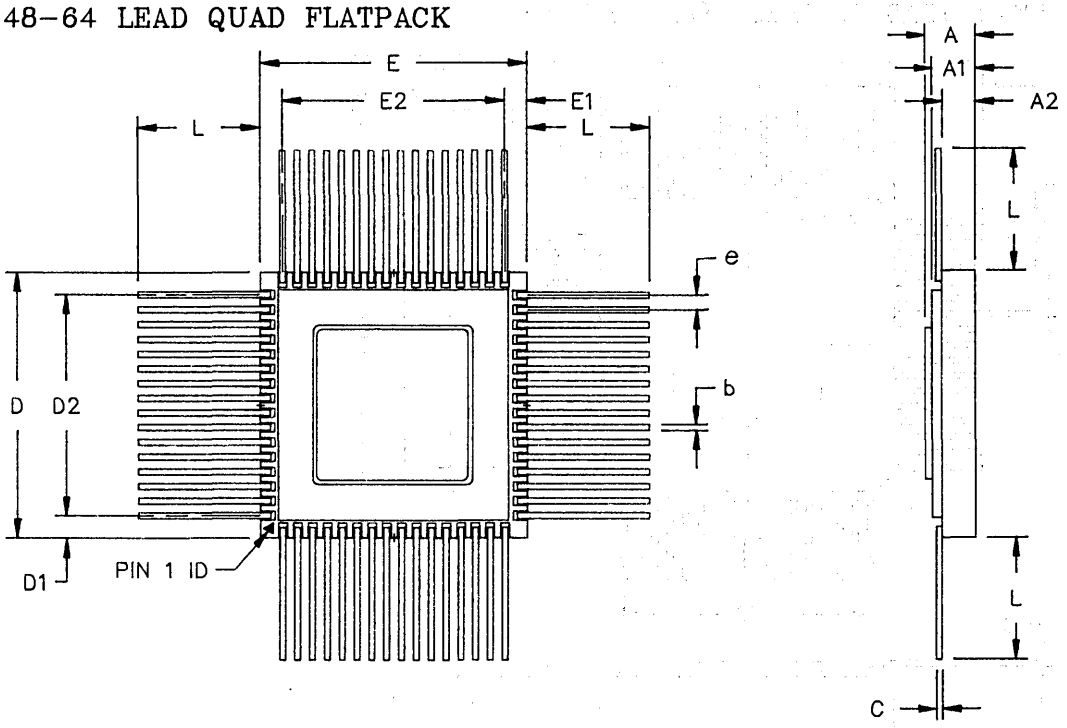


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C64-2	
# OF LDS (N)	64	
SYMBOL	MIN	MAX
A	.120	.180
b	.015	.021
b1	.045	.060
C	.009	.012
D	3.170	3.240
E	.790	.810
E1	.880	.915
E2	.640	.660
e	.100 BSC	
L	.125	.160
L1	.150	–
Q	.020	.100
S	.030	.065
S1	.005	–
S2	.005	–

FLATPACKS (Continued)

48–64 LEAD QUAD FLATPACK

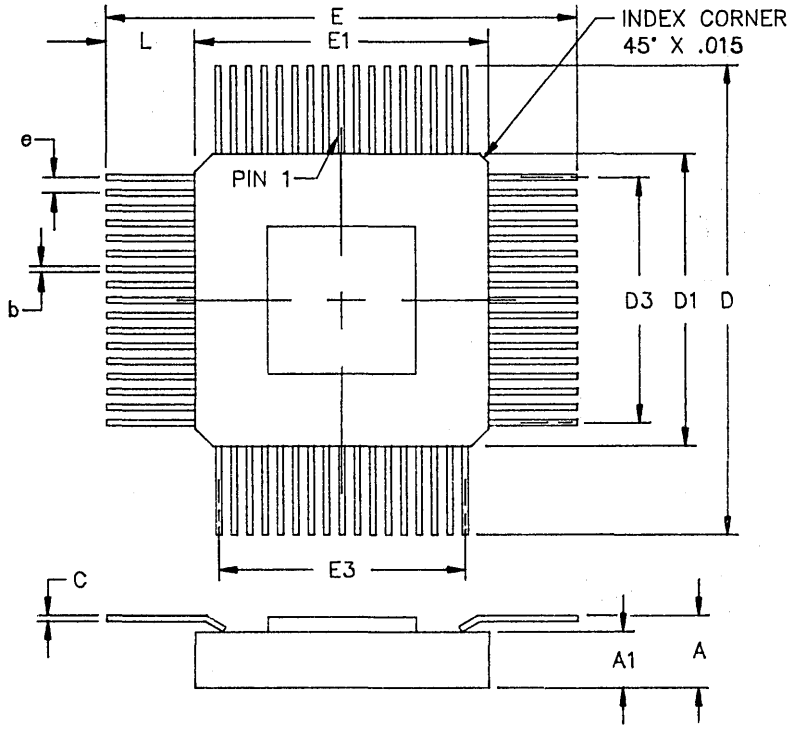


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	F48–1		F64–1	
# OF LDS (N)	48		64	
SYMBOL	MIN	MAX	MIN	MAX
A	.089	.108	.070	.090
A1	.079	.096	.060	.078
A2	.058	.073	.030	.045
b	.018	.022	.016	.020
C	.008	.010	.009	.012
D/E	–	.750	.885	.915
D1/E1	.100 REF		.075 REF	
D2/E2	.550 BSC		.750 BSC	
e	.050 BSC		.050 BSC	
L	.350	.450	.350	.450
ND/NE	12		16	

FLATPACKS (Continued)

68 LEAD QUAD FLATPACK (FINE PITCH)

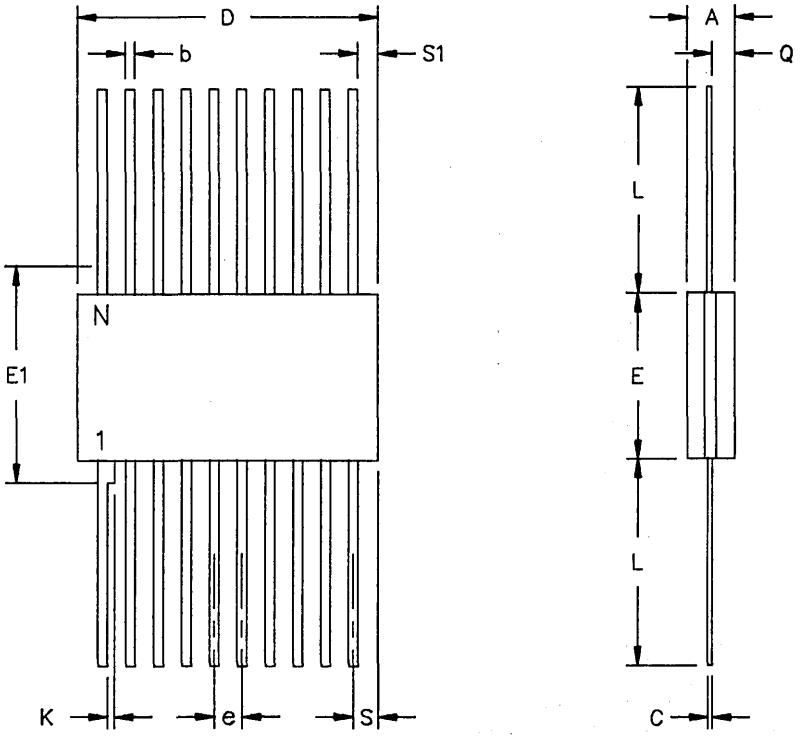


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	F68–2	
# OF LDS (N)	68	
SYMBOL	MIN	MAX
A	.064	.084
A1	.054	.070
b	.008	.013
C	.0045	.008
D/E	.860	1.100
D1/E1	.460	.500
D2/E2	.400 REF	
e	.025 BSC	
L	.200	.300
ND/NE	17	

CERPACKS

16–28 LEAD CERPACK

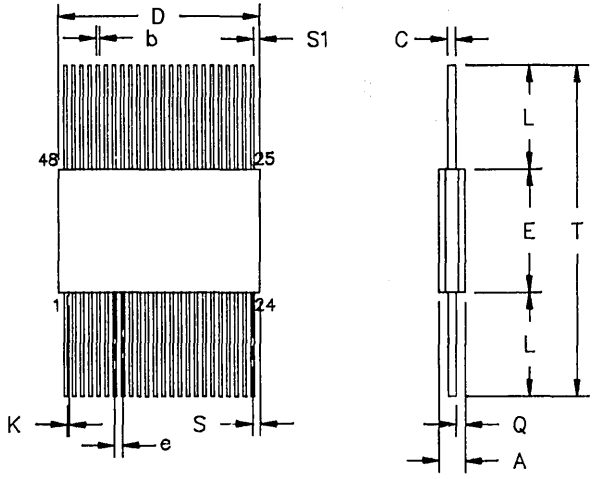


NOTES:
1. ALL DIMENSION ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	E16–1		E20–1		E24–1		E28–1		E28–2	
# OF LDS (N)	16		20		24		28		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.055	.085	.045	.092	.045	.090	.045	.115	.045	.090
b	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
C	.0045	.006	.0045	.006	.0045	.006	.0045	.006	.0045	.006
D	.370	.430	–	.540	–	.640	–	.740	–	.740
E	.245	.285	.245	.300	.300	.420	.460	.520	.340	.380
E1	–	.305	–	.305	–	.440	–	.550	–	.400
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
K	.008	.015	.008	.015	.008	.015	.008	.015	.008	.015
L	.250	.370	.250	.370	.250	.370	.250	.370	.250	.370
Q	.026	.040	.026	.040	.026	.040	.026	.045	.026	.045
S	–	.045	–	.045	–	.045	–	.045	–	.045
S1	.005	–	.005	–	.005	–	.000	–	.005	–

CERPACKS (Continued)

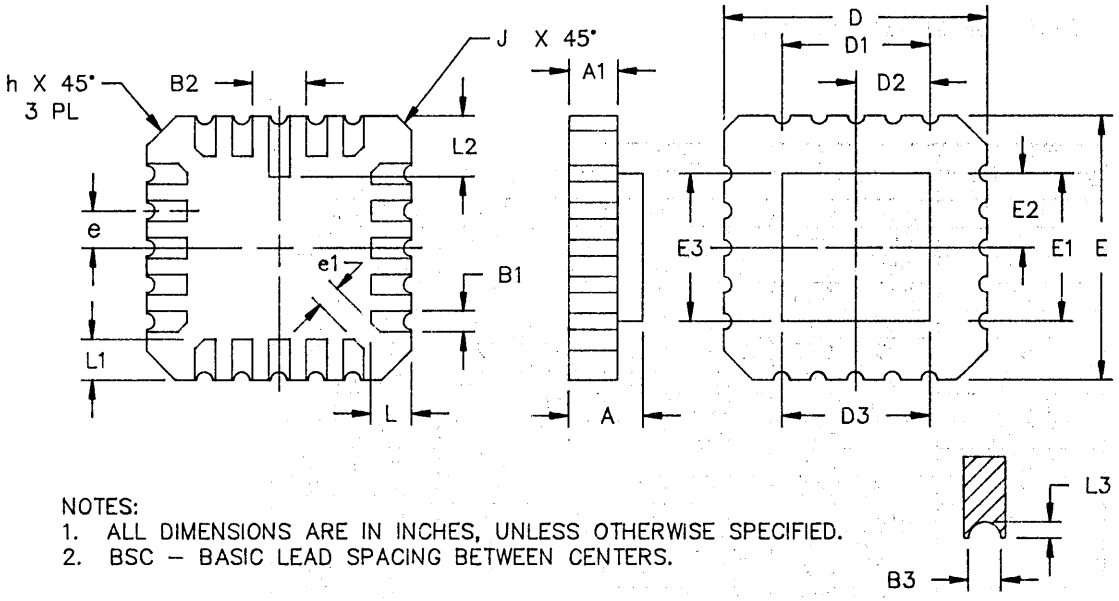
48–56 LEAD CERPACK (.025" LEAD PITCH)



NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "N" REPRESENTS THE NUMBER OF LEADS.
4. THIS DWG REPRESENTS A 48 LEAD CERPACK.

DWG #	E48–1		E56–1	
# OF LDS (N)	48		56	
SYMBOL	MIN	MAX	MIN	MAX
A	.065	.086	.065	.086
b	.008	.013	.008	.013
C	.0045	.006	.0045	.006
D	.614	.626	.713	.727
E	.370	.390	.370	.390
e	.025 BSC		.025 BSC	
K	.003	.007	.003	.007
L	.312	.405	.312	.405
Q	.035	.045	.035	.045
S	–	.045	–	.045
S1	.005	–	.005	–
T	.995	1.200	.995	1.200

LEADLESS CHIP CARRIERS



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

20–48 LEAD LCC (SQUARE)

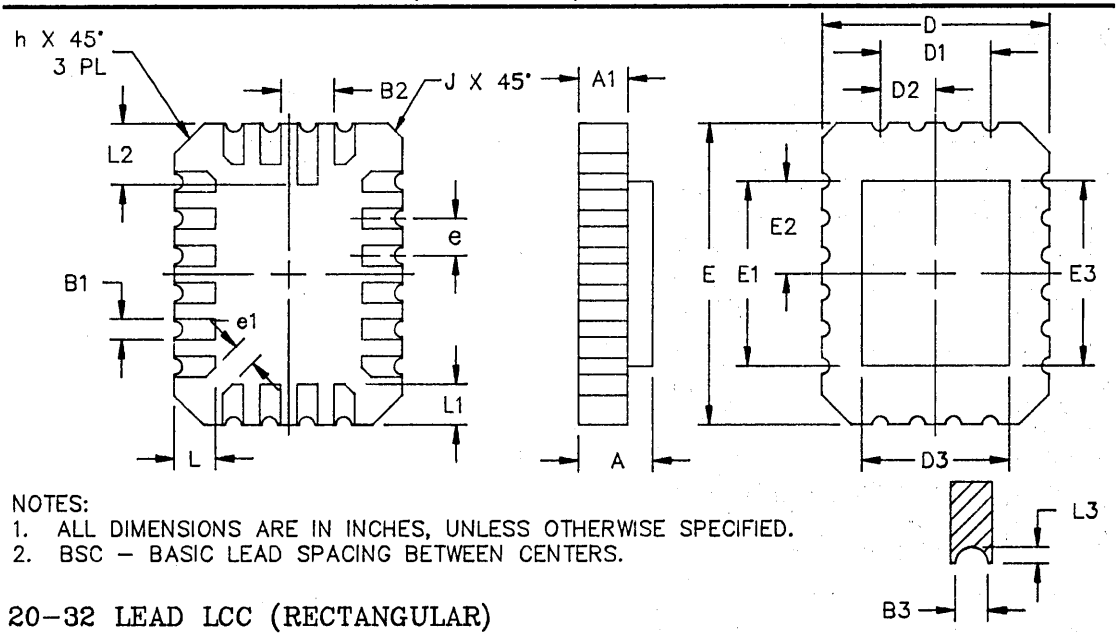
DWG #	L20–2		L28–1		L44–1		L48–1	
# OF LDS (N)	20		28		44		48	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.064	.100	.064	.100	.064	.120	.055	.120
A1	.054	.066	.050	.088	.054	.088	.045	.090
B1	.022	.028	.022	.028	.022	.028	.017	.023
B2	.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022
D/E	.342	.358	.442	.460	.640	.660	.554	.572
D1/E1	.200 BSC		.300 BSC		.500 BSC		.440 BSC	
D2/E2	.100 BSC		.150 BSC		.250 BSC		.220 BSC	
D3/E3	–	.358	–	.460	–	.560	.500	.535
e	.050 BSC		.050 BSC		.050 BSC		.040 BSC	
e1	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.040 REF		.040 REF		.012 RADIUS	
J	.020 REF		.020 REF		.020 REF		.020 REF	
L	.045	.055	.045	.055	.045	.055	.033	.047
L1	.045	.055	.045	.055	.045	.055	.033	.047
L2	.077	.093	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015
ND/NE	5		7		11		12	

LEADLESS CHIP CARRIERS (Continued)

52–68 LEAD LCC (SQUARE)

DWG #	L52–1		L52–2		L68–2		L68–1	
# OF LDS (N)	52		52		68		68	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.061	.087	.082	.120	.082	.120	.065	.120
A1	.051	.077	.072	.088	.072	.088	.055	.075
B1	.022	.028	.022	.028	.022	.028	.008	.014
B2	.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022
D/E	.739	.761	.739	.761	.938	.962	.554	.566
D1/E1	.600 BSC		.600 BSC		.800 BSC		.400 BSC	
D2/E2	.300 BSC		.300 BSC		.400 BSC		.200 BSC	
D3/E3	–	.661	–	.661	–	.862	–	.535
e	.050 BSC		.050 BSC		.050 BSC		.025 BSC	
e1	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.040 REF		.040 REF		.040 REF	
J	.020 REF		.020 REF		.020 REF		.020 REF	
L	.045	.055	.045	.055	.045	.055	.045	.055
L1	.045	.055	.045	.055	.045	.055	.045	.055
L2	.077	.093	.075	.093	.075	.095	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015
ND/NE	13		13		17		17	

LEADLESS CHIP CARRIERS (Continued)



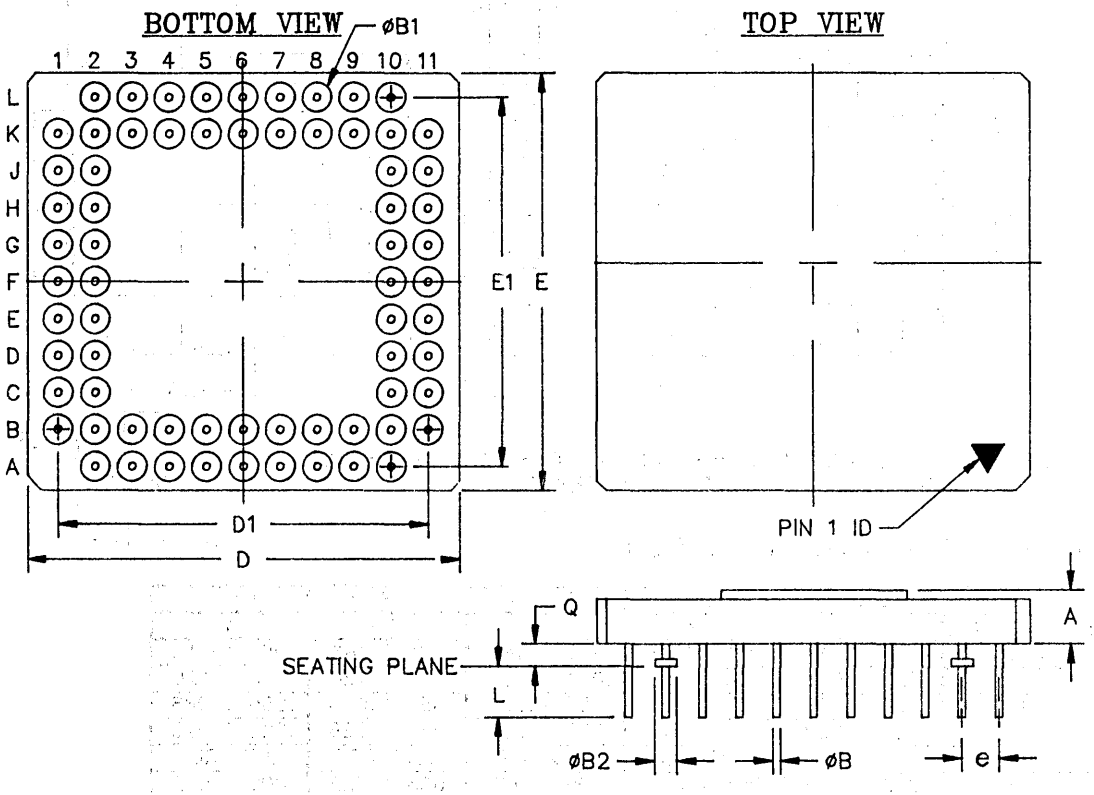
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

20–32 LEAD LCC (RECTANGULAR)

DWG #	L20–1		L22–1		L24–1		L28–2		L32–1	
# OF LDS (N)	20		22		24		28		32	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.060	.075	.064	.100	.064	.120	.060	.120	.060	.120
A1	.050	.065	.054	.063	.054	.066	.050	.088	.050	.088
B1	.022	.028	.022	.028	.022	.028	.022	.028	.022	.028
B2	.072 REF		.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022	.006	.022
D	.284	.296	.284	.296	.292	.308	.342	.358	.442	.458
D1	.150 BSC		.150 BSC		.200 BSC		.200 BSC		.300 BSC	
D2	.075 BSC		.075 BSC		.100 BSC		.100 BSC		.150 BSC	
D3	–	.280	–	.280	–	.308	–	.358	–	.458
E	.420	.435	.480	.496	.392	.408	.540	.560	.540	.560
E1	.250 BSC		.300 BSC		.300 BSC		.400 BSC		.400 BSC	
E2	.125 BSC		.150 BSC		.150 BSC		.200 BSC		.200 BSC	
E3	–	.410	–	.480	–	.408	–	.558	–	.558
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
e1	.015	–	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.012 RADIUS		.025 REF		.040 REF		.040 REF	
J	.020 REF		.012 RADIUS		.015 REF		.020 REF		.020 REF	
L	.045	.055	.039	.051	.040	.050	.045	.055	.045	.055
L1	.045	.055	.039	.051	.040	.050	.045	.055	.045	.055
L2	.080	.095	.083	.097	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015	.003	.015
ND	4		4		5		5		7	
NE	6		7		7		9		9	

PIN GRID ARRAYS

68 PIN PGA (CAVITY UP)

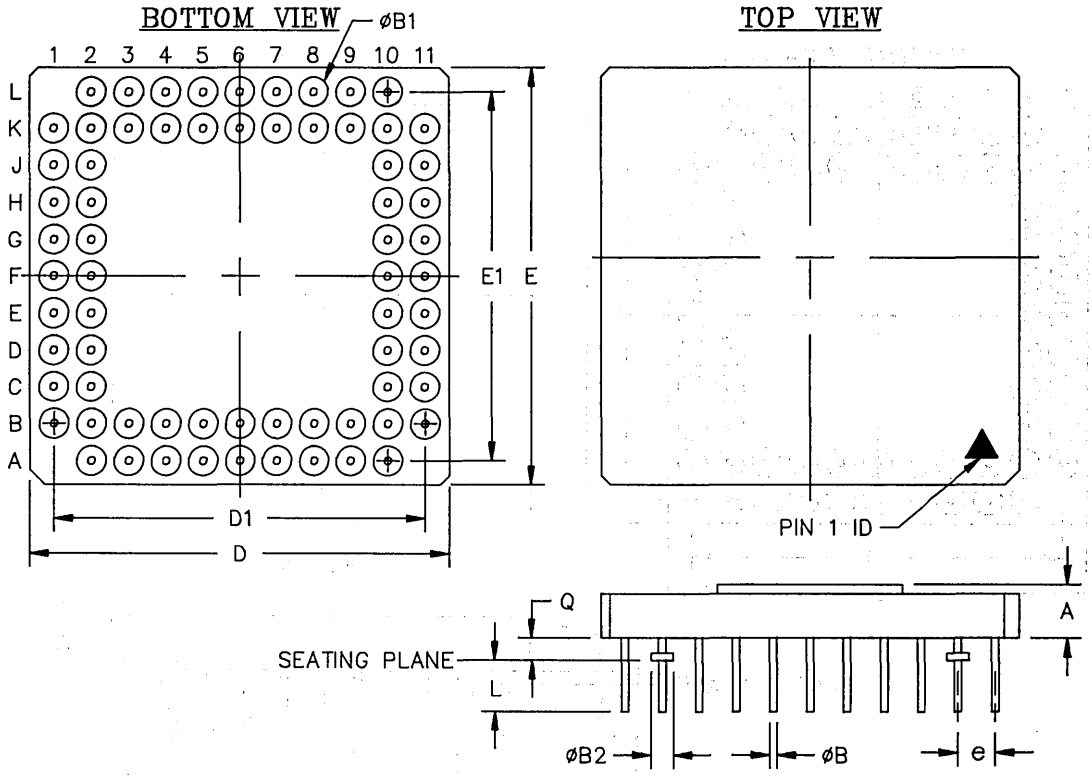


DWG #	G68-1	
# OF PINS (N)	68	
SYMBOL	MIN	MAX
A	.070	.145
ØB	.016	.020
ØB1	–	.080
ØB2	.040	.060
D/E	1.140	1.180
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

68 PIN PGA (SMALL OUTLINE – CAVITY UP)

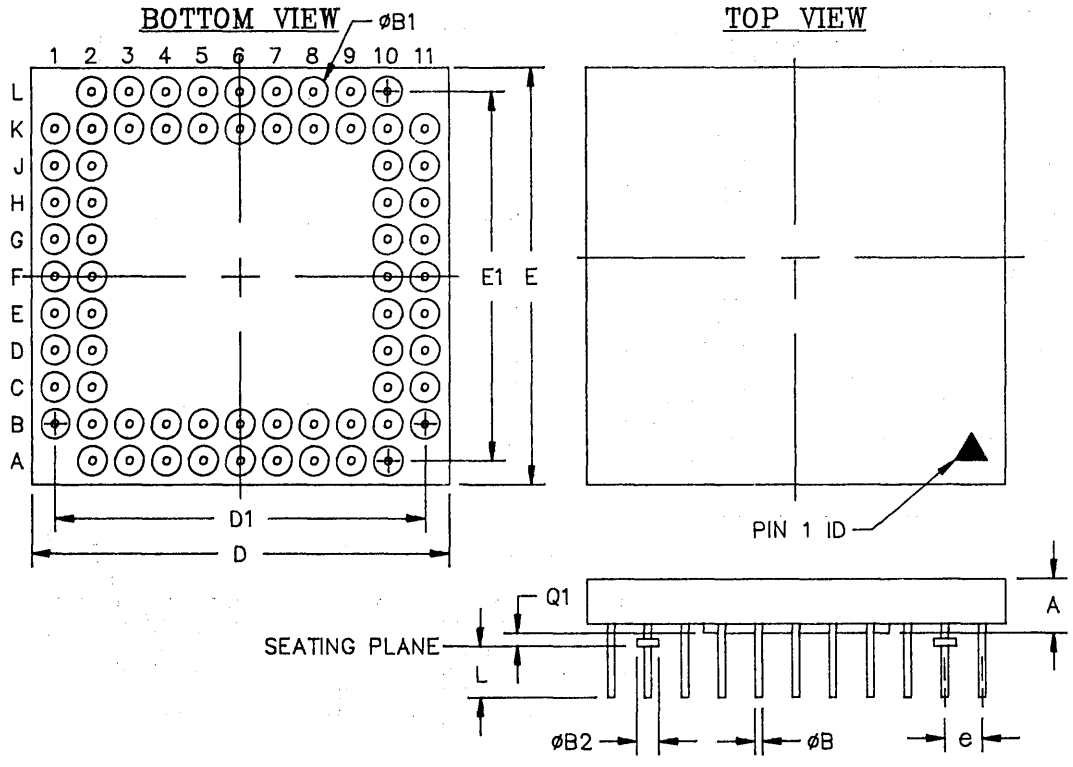


DWG #	G68-3	
# OF PINS (N)	68	
SYMBOL	MIN	MAX
A	.070	.145
ØB	.016	.020
ØB1	.040	.080
ØB2	.040	.060
D/E	1.080	1.135
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

68 PIN PGA (CAVITY DOWN)

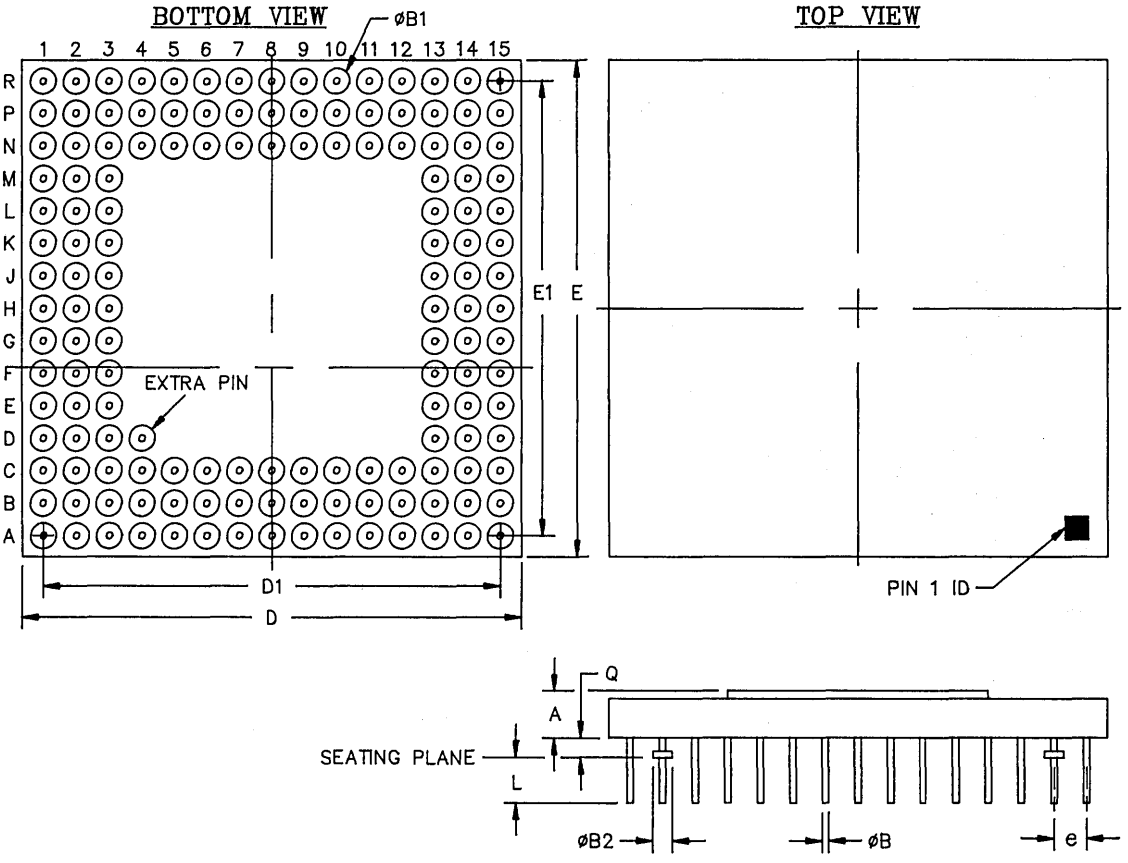


DWG #	G68-2	
# OF PINS (N)	68	
SYMBOL	MIN	MAX
A	.077	.095
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D/E	1.098	1.122
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

144 PIN PGA (CAVITY UP – R3001)

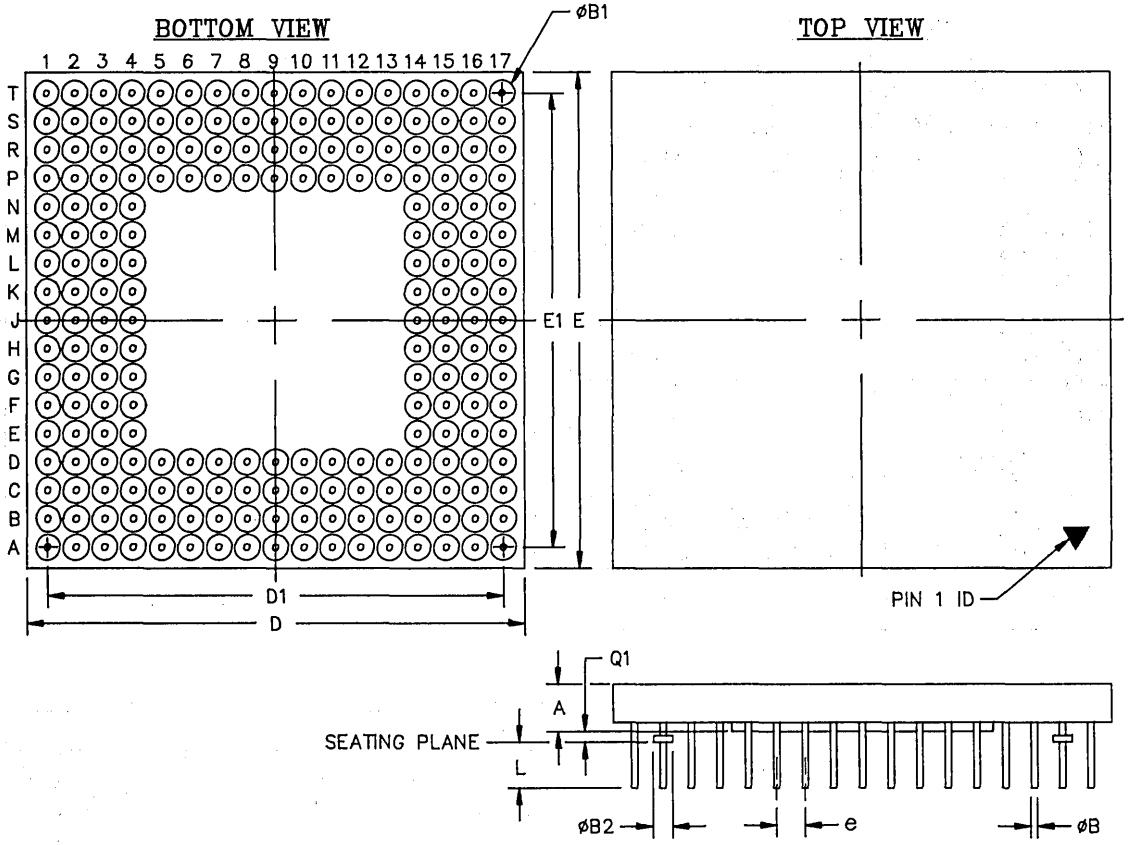


DWG #	G144–2	
# OF PINS (N)	145	
SYMBOL	MIN	MAX
A	.082	.125
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D/E	1.559	1.590
D1/E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
M	15	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.
6. EXTRA PIN (D–4) ELECTRICALLY CONNECTED TO D–3.

PIN GRID ARRAYS (Continued)

208 PIN PGA (CAVITY DOWN)

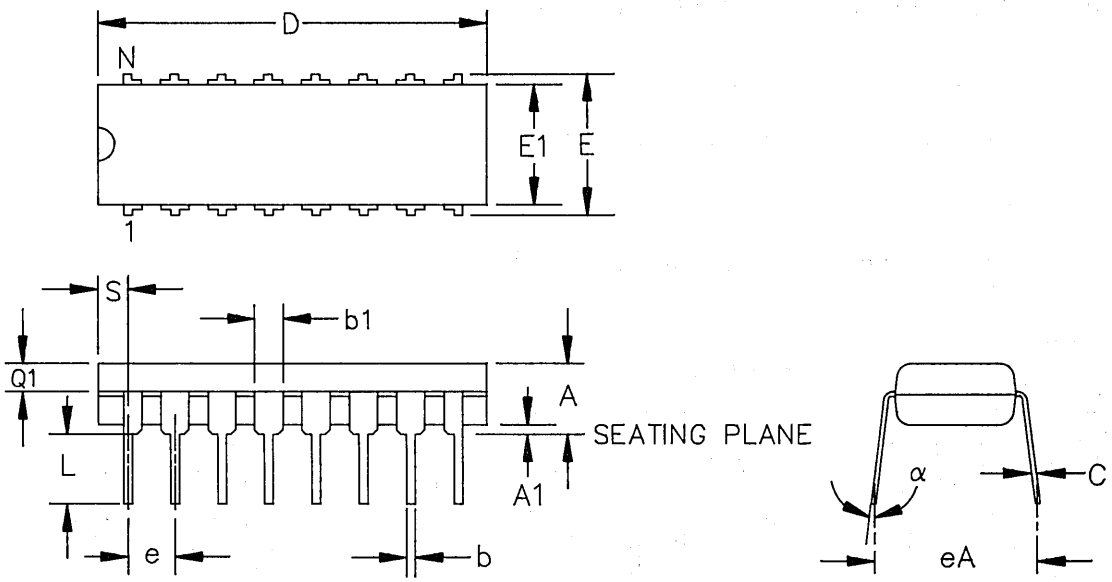


DWG #	G208-2	
# OF PINS (N)	208	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1	—	.080
øB2	.040	.060
D/E	1.732	1.780
D1/E1	1.600 BSC	
e	.100 BSC	
L	.120	.140
M	17	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PLASTIC DUAL IN-LINE PACKAGES

16-32 LEAD PLASTIC DIP (300 MIL)

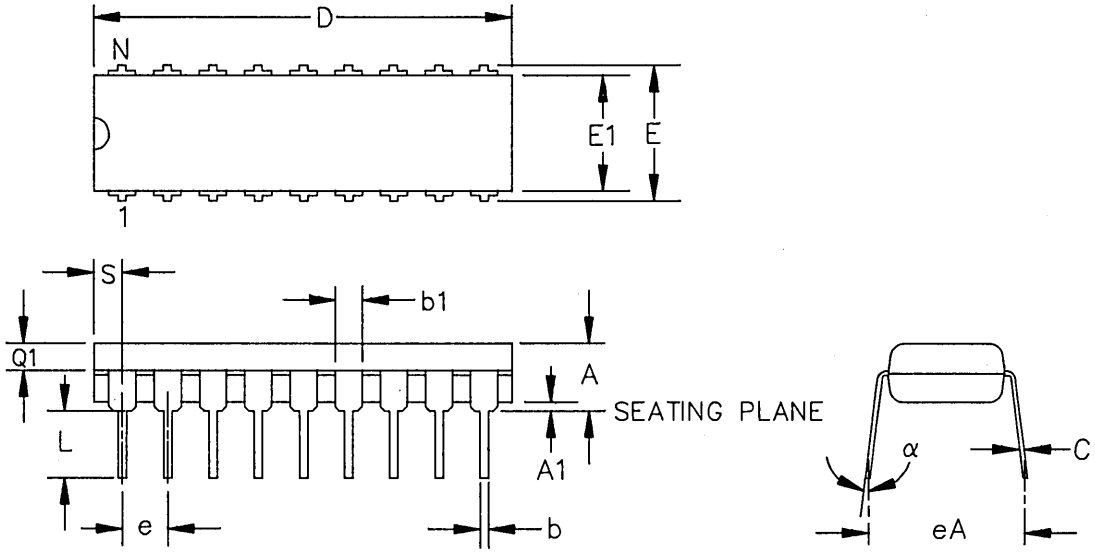


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG #	P16-1		P22-1		P28-2		P32-2	
# OF LDS (N)	16		22		28		32	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.165	.145	.165	.145	.180	.145	.180
A1	.015	.035	.015	.035	.015	.030	.015	.030
b	.015	.022	.015	.022	.015	.022	.016	.022
b1	.050	.070	.050	.065	.045	.065	.045	.060
C	.008	.012	.008	.012	.008	.015	.008	.015
D	.745	.760	1.050	1.060	1.345	1.375	1.545	1.585
E	.300	.325	.300	.320	.300	.325	.300	.325
E1	.247	.260	.240	.270	.270	.295	.275	.295
e	.090	.110	.090	.110	.090	.110	.090	.110
eA	.310	.370	.310	.370	.310	.400	.310	.400
L	.120	.150	.120	.150	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°	0°	15°
S	.015	.035	.020	.040	.020	.042	.020	.060
Q1	.050	.070	.055	.075	.055	.065	.055	.065

PLASTIC DUAL IN-LINE PACKAGES (Continued)

18-24 LEAD PLASTIC DIP (300 MIL - FULL LEAD)

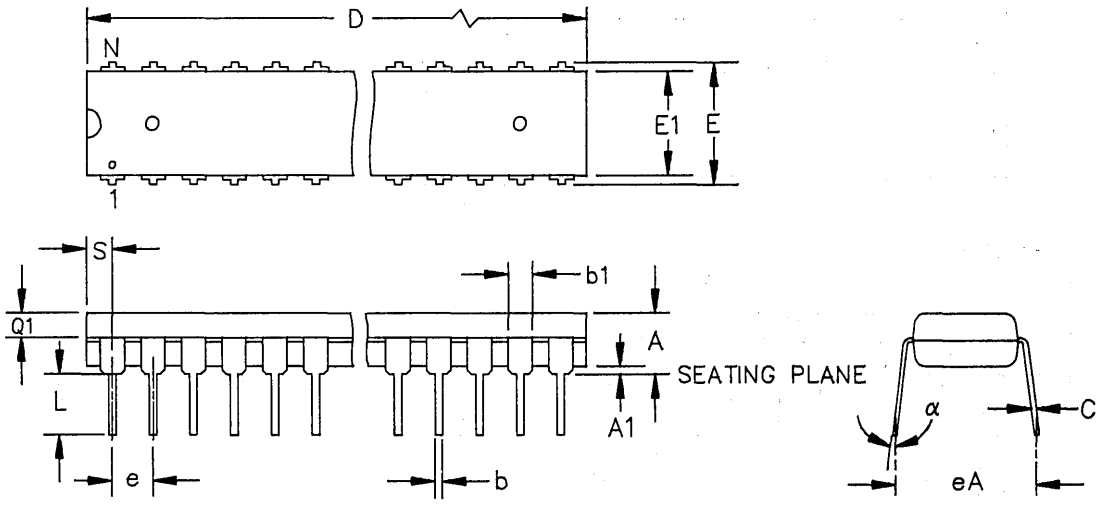


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG #	P18-1		P20-1		P24-1	
# OF LDS (N)	18		20		24	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.165	.145	.165	.145	.165
A1	.015	.035	.015	.035	.015	.035
b	.015	.020	.015	.020	.015	.020
b1	.050	.070	.050	.070	.050	.065
C	.008	.012	.008	.012	.008	.012
D	.885	.910	1.022	1.040	1.240	1.255
E	.300	.325	.300	.325	.300	.320
E1	.247	.260	.240	.280	.250	.275
e	.090	.110	.090	.110	.090	.110
eA	.310	.370	.310	.370	.310	.370
L	.120	.150	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°
S	.040	.060	.025	.070	.055	.075
Q1	.050	.070	.055	.075	.055	.070

PLASTIC DUAL IN-LINE PACKAGES (Continued)

28 & 32 LEAD PLASTIC DIP (400 MIL)

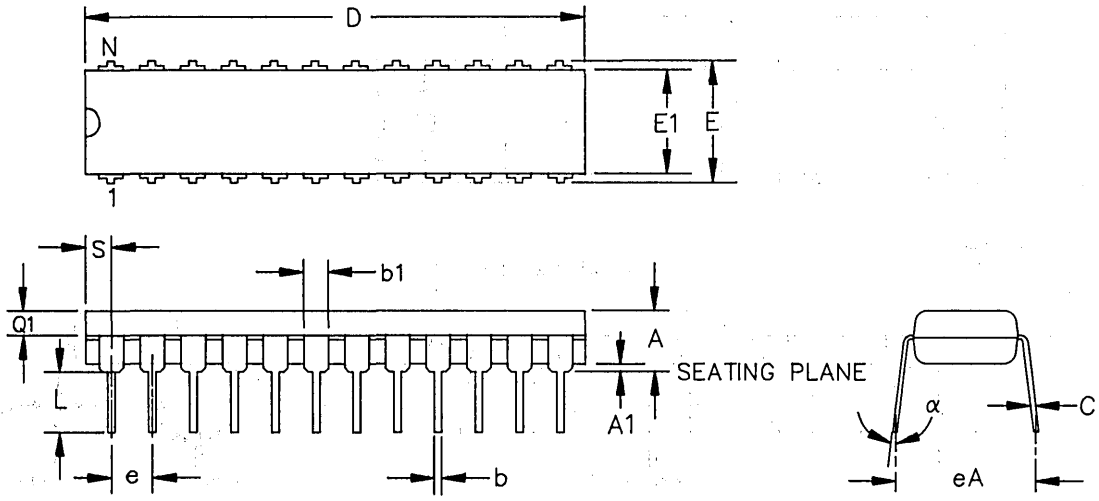


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG #	P28-3		P32-3	
# OF LEADS (N)	28		32	
SYMBOLS	MIN	MAX	MIN	MAX
A	–	.210	–	.200
A1	.015	–	.015	–
b	.014	.022	.014	.022
b1	.045	.065	.045	.065
C	.009	.015	.009	.015
D	1.380	1.420	1.610	1.620
E	.390	.425	.390	.425
E1	.340	.390	.340	.390
e	.100 BSC		.100 BSC	
eA	.400 BSC		.400 BSC	
L	.115	.160	.115	.160
α	0°	15°	0°	15°
S	.040	.070	.040	.070
Q1	.060	.090	.060	.090

PLASTIC DUAL IN-LINE PACKAGES (Continued)

24-48 LEAD PLASTIC DIP (600 MIL)

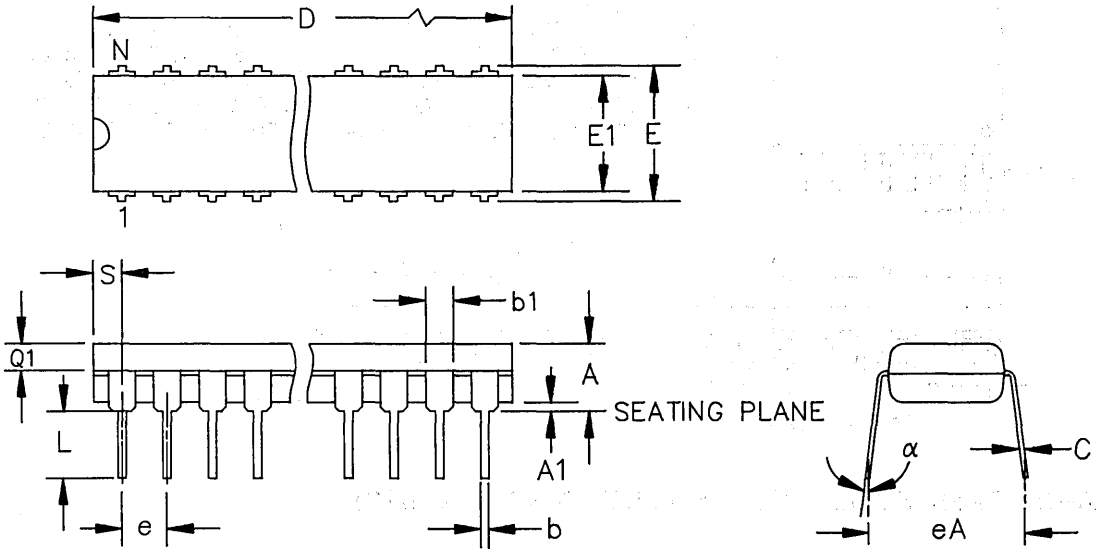


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG #	P24-2		P28-1		P32-1		P40-1		P48-1	
# OF LEADS (N)	24		28		32		40		48	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.160	.185	.160	.185	.170	.190	.160	.185	.170	.200
A1	.015	.035	.015	.035	.015	.050	.015	.035	.015	.035
b	.015	.020	.015	.020	.016	.020	.015	.020	.015	.020
b1	.050	.065	.050	.065	.045	.055	.050	.065	.050	.065
C	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	1.240	1.260	1.420	1.460	1.645	1.655	2.050	2.070	2.420	2.450
E	.600	.620	.600	.620	.600	.625	.600	.620	.600	.620
E1	.530	.550	.530	.550	.530	.550	.530	.550	.530	.560
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
eA	.610	.670	.610	.670	.610	.670	.610	.670	.610	.670
L	.120	.150	.120	.150	.125	.135	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°
S	.060	.080	.055	.080	.070	.080	.070	.085	.060	.075
Q1	.060	.080	.060	.080	.065	.075	.060	.080	.060	.080

PLASTIC DUAL IN-LINE PACKAGES (Continued)

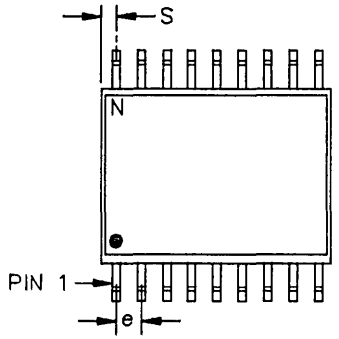
64 LEAD PLASTIC DIP (900 MIL)



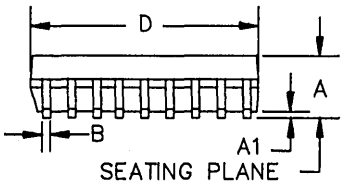
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

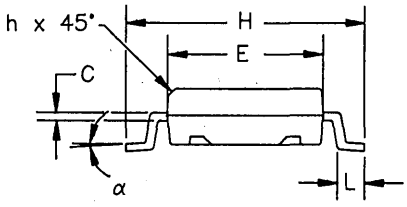
DWG #	P64-1	
# OF LEADS (N)	64	
SYMBOLS	MIN	MAX
A	.180	.230
A1	.015	.040
b	.015	.020
b1	.050	.065
C	.008	.012
D	3.200	3.220
E	.900	.925
E1	.790	.810
e	.090	.110
eA	.910	1.000
L	.120	.150
α	0°	15°
S	.045	.065
Q1	.080	.090

SMALL OUTLINE IC



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

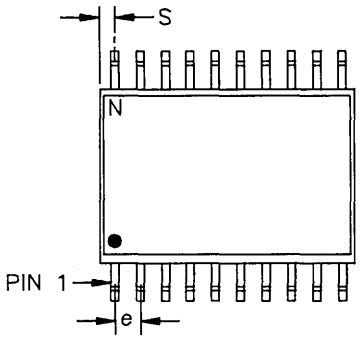




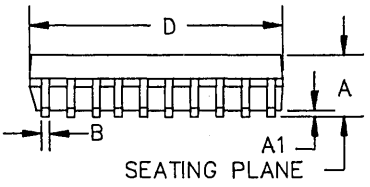
16–24 LEAD SMALL OUTLINE (GULL WING – JEDEC)

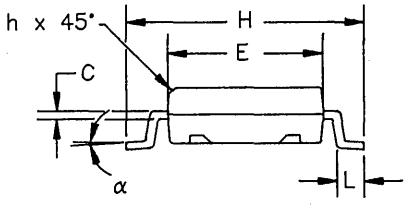
DWG #	SO16–1		SO18–1		SO20–2		SO24–2	
# OF LDS (N)	16 (.300)		18 (.300)		20 (.300")		24 (.300")	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.095	.1043	.095	.1043	.095	.1043	.095	.1043
A1	.005	.0118	.005	.0118	.005	.0118	.005	.0118
B	.014	.020	.014	.020	.014	.020	.014	.020
C	.0091	.0125	.0091	.0125	.0091	0125	.0091	.0125
D	.403	.413	.447	.462	.497	.511	.600	.614
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC	
E	.292	.2992	.292	.2992	.292	.2992	.292	.2992
h	.010	.020	.010	.020	.010	.020	.010	.020
H	.400	.419	.400	.419	.400	.419	.400	.419
L	.018	.045	.018	.045	.018	.045	.018	.045
α	0°	8°	0°	8°	0°	8°	0°	8°
S	.023	.035	.023	.035	.023	.035	.023	.035

SMALL OUTLINE IC (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.



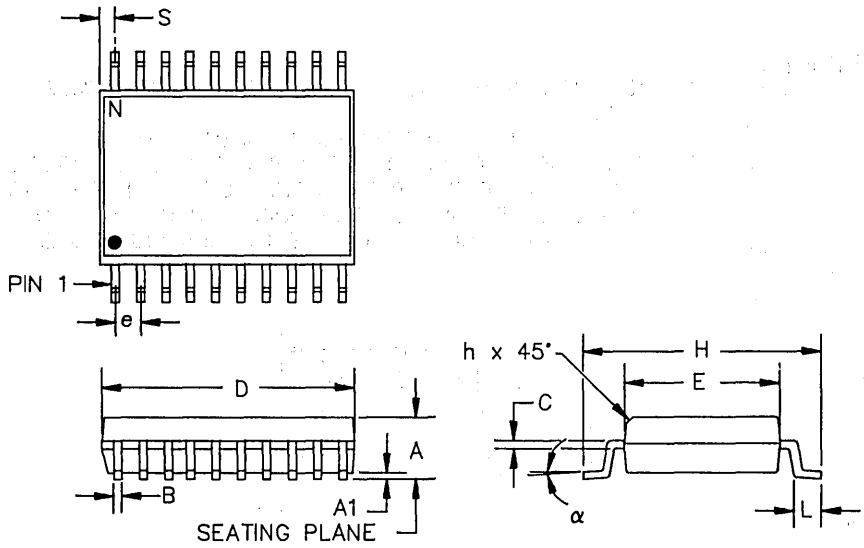


4

28 LEAD SMALL OUTLING (GULL WING – JEDEC)

DWG #	SO28-2		SO28-3	
# OF LDS (N)	28 (.300")		28 (.330")	
SYMBOL	MIN	MAX	MIN	MAX
A	.095	.1043	.110	.120
A1	.005	.0118	.005	.014
B	.014	.020	.014	.019
C	.0091	.0125	.006	.010
D	.700	.712	.718	.728
e	.050 BSC		.050 BSC	
E	.292	.2992	.340	.350
h	.010	.020	.012	.020
H	.400	.419	.462	.478
L	.018	.045	.028	.045
α	0°	8°	0°	8°
S	.023	.035	.023	.035

SMALL OUTLINE IC (Continued)

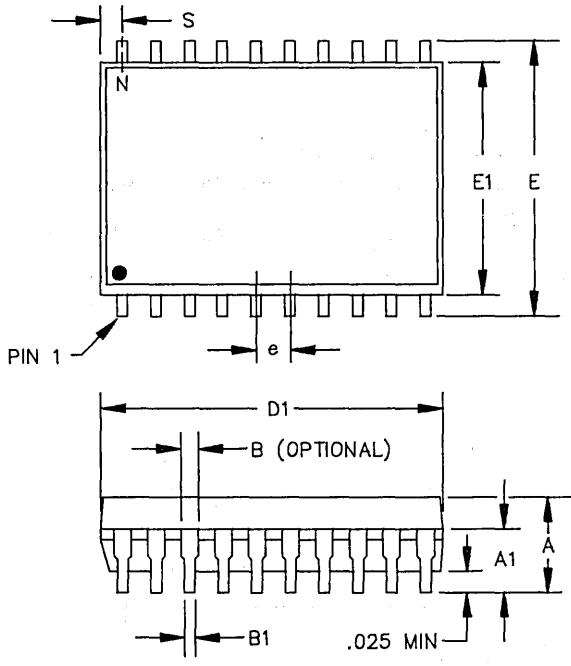


NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF THE PACKAGE.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

16–24 LEAD SSOP (EIAJ – 1.27 LEAD PITCH)

DWG #	SO16–6		SO20–6		SO24–6	
# OF LDS (N)	16		20		24	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	1.70	2.10	1.75	2.10	1.75	2.10
A1	.08	–	.05 TYP		.05 TYP	
B	.35	.45	.30	.50	.30	.50
C	.12	.18	.15	.25	.15	.25
D	10.10	10.30	12.20	12.80	14.70	15.30
E	5.00	5.60	5.20	5.60	5.20	5.60
e	1.27 BSC		1.27 BSC		1.27 BSC	
H	7.60	8.00	7.62	8.10	7.62	8.10
L	.65	.85	.25	–	.25	–
α	12° REF		0°	8°	0°	8°

SMALL OUTLINE IC (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSION AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE

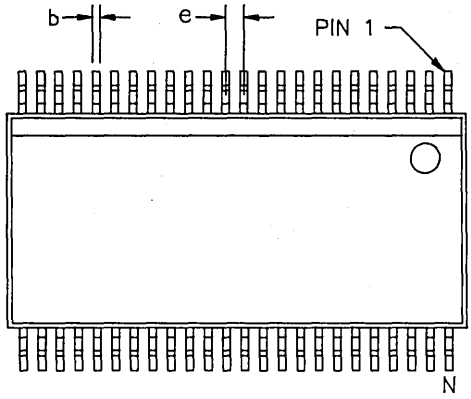
4

20–32 LEAD SMALL OUTLINE (J–BEND, 300 MIL)

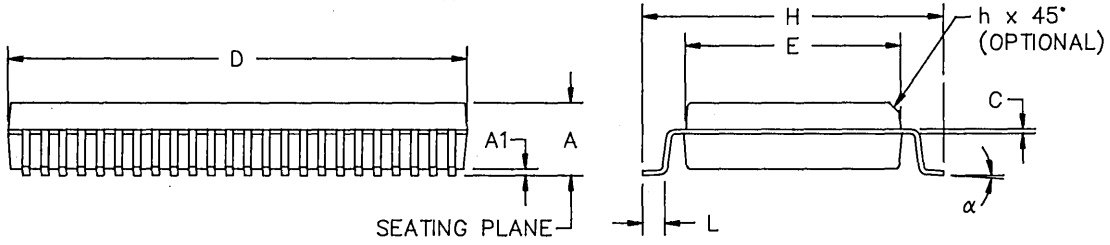
DWG #	SO20–1		SO24–4		SO24–8		SO28–5		SO32–2	
# OF LDS (N)	20		24		24		28		32	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.120	.140	.130	.148	.120	.140	.120	.140	.130	.148
A1	.078	.095	.082	.095	.078	.091	.078	.095	.082	.095
B	–	–	.026	.032	–	–	–	–	.026	.032
B1	.014	.020	.015	.020	.014	.019	.014	.020	.016	.020
C	.008	.013	.007	.011	.0091	.0125	.008	.013	.008	.013
D1	.500	.512	.620	.630	.602	.612	.700	.712	.820	.830
E	.335	.347	.335	.345	.335	.347	.335	.347	.330	.340
E1	.292	.300	.295	.305	.292	.299	.292	.300	.295	.305
E2	.262	.272	.260	.280	.262	.272	.262	.272	.260	.275
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
h	.010	.020	.010	.020	.010	.016	.012	.020	.012	.020
S	.023	.035	.032	.043	.032	.043	.023	.035	.032	.043

SMALL OUTLINE IC (Continued)

48 & 56 LEAD SSOP (JEDEC)

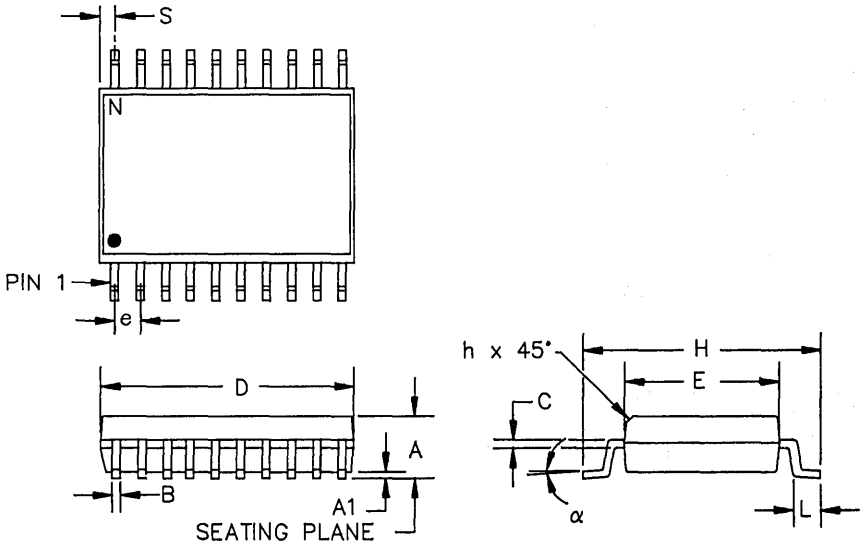


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.



DWG #	SO48–1		SO56–1	
# OF LDS (N)	48 (.300")		56 (.300")	
SYMBOL	MIN	MAX	MIN	MAX
A	.095	.110	.095	.110
A1	.008	.016	.008	.016
b	.008	.012	.008	.012
C	.005	.009	.005	.009
D	.620	.630	.720	.730
E	.291	.299	.291	.299
e	.025 BSC		.025 BSC	
H	.395	.420	.395	.420
h	.015	.025	.015	.025
L	.020	.040	.020	.040
α	0°	8°	0°	8°

SMALL OUTLINE IC (Continued)



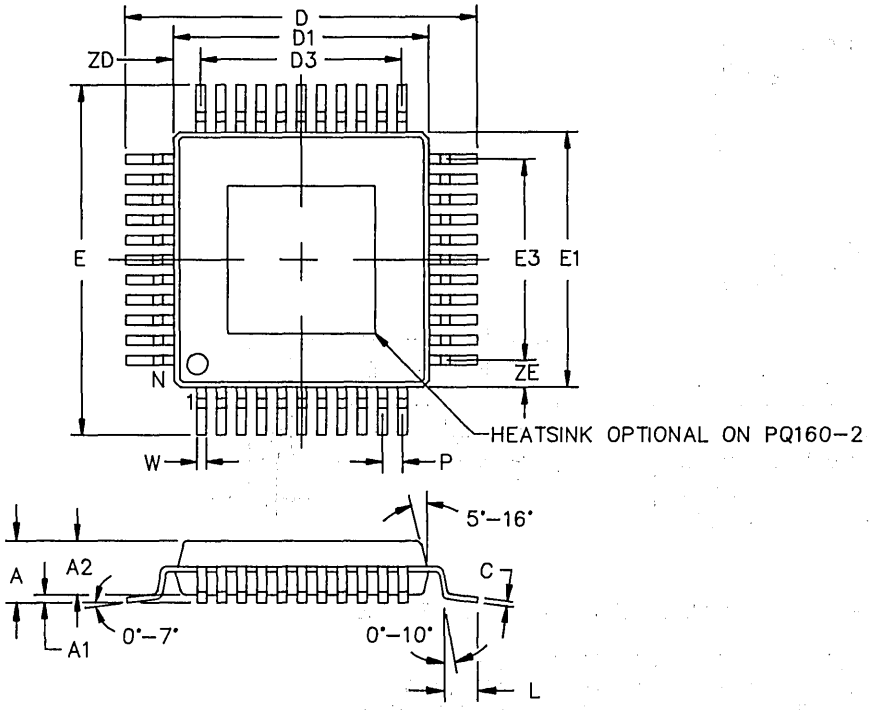
NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .10mm AT THE SEATING PLANE.

20 & 24 LEAD SSOP (EIAJ – .65 LEAD PITCH)

DWG #	SO20–7		SO24–7	
# OF LDS (N)	20		24	
SYMBOLS	MIN	MAX	MIN	MAX
A	1.73	1.99	1.73	1.99
A1	.05	.21	.05	.21
B	.25	.38	.25	.38
C	.13	.22	.13	.22
D	7.07	7.33	8.07	8.33
E	5.20	5.38	5.20	5.38
e	.65 BSC		.65 BSC	
H	7.65	7.90	7.65	7.90
L	.55	.95	.55	.95
α	0°	8°	0°	8°

PLASTIC QUAD FLATPACKS (Continued)

80–208 LEAD SQUARE PLASTIC QUAD FLATPACK (EIAJ)

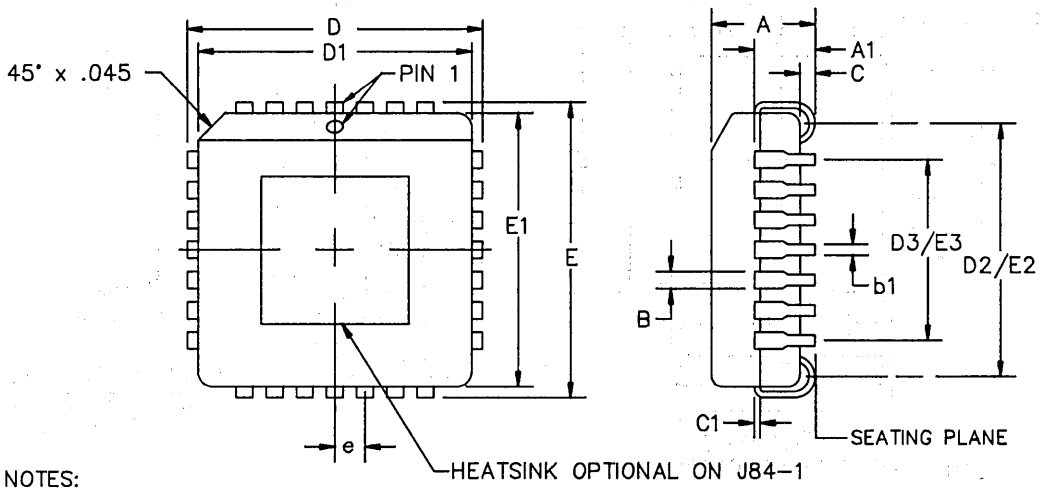


NOTES:
1. ALL DIMENSIONS ARE IN METRIC, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .254 PER SIDE.
4. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.

DWG #	PQ80–1		PQ144–2		PQ160–2		PQ208–2	
# OF LDS (N)	80		144		160		208	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	–	2.45	3.45	4.07	3.45	4.07	3.45	4.07
A1	–	.25	.25	–	.25	–	.25	–
A2	1.75	2.25	3.18	3.65	3.18	3.65	3.18	3.65
C	.13	.20	.13	.20	.13	.20	.13	.20
D/E	16.95	17.45	31.80	32.00	31.80	32.00	31.80	32.00
D1/E1	13.90	14.10	27.90	28.10	27.90	28.10	27.90	28.10
D3/E3	12.35 REF		22.75 REF		25.35 REF		25.50 REF	
L	.65	.95	.65	.95	.65	.95	.65	.95
ND/NE	20/20		36/36		40/40		52/52	
P	.65 BSC		.65 BSC		.65 BSC		.50 BSC	
W	.22	.35	.22	.35	.22	.35	.22	.35
ZD/ZE	.82		2.62		1.32		1.25	

PLASTIC LEADED CHIP CARRIERS

20–84 LEAD PLCC (SQUARE)



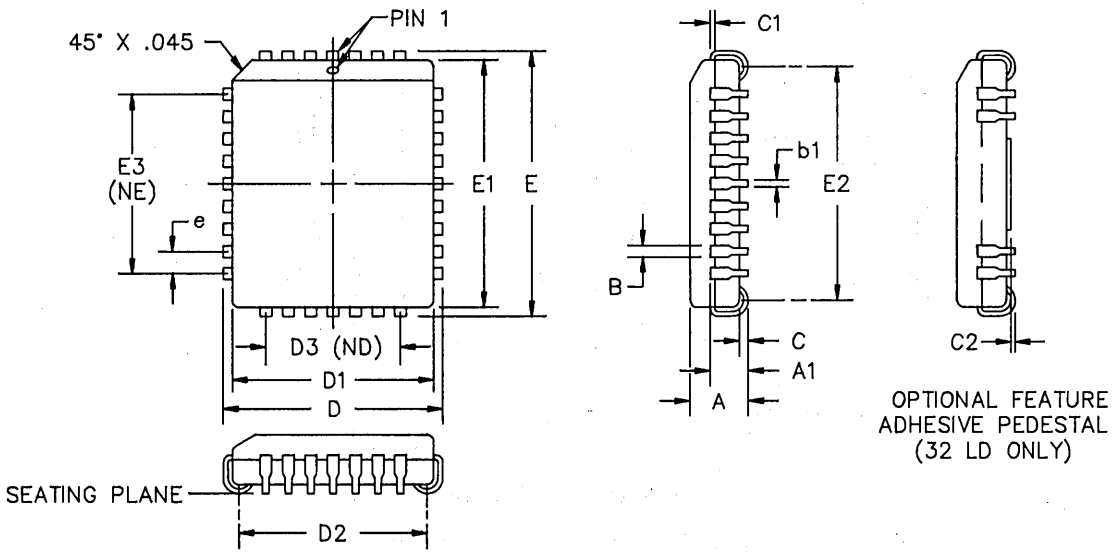
NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
5. ND & NE REPRESENT NUMBER OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
6. D1 & E1 SHOULD BE MEASURED FROM THE BOTTOM OF THE PKG.

DWG #	J20–1		J28–1		J44–1		J52–1		J68–1		J84–1	
# OF LDS	20		28		44		52		68		84	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180
A1	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115
B	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032
b1	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021
C	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040
C1	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
D1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
D2/E2	.290	.330	.390	.430	.590	.630	.690	.730	.890	.930	1.090	1.130
D3/E3	.200 REF		.300 REF		.500 REF		.600 REF		.800 REF		1.000 REF	
E	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
E1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
ND/NE	5		7		11		13		17		21	

PLASTIC LEADED CHIP CARRIERS (Continued)

18–32 LEAD PLCC (RECTANGULAR)



DWG #	J18–1		J32–1	
# OF LDS	18		32	
SYMBOL	MIN	MAX	MIN	MAX
A	.120	.140	.120	.140
A1	.075	.095	.075	.095
B	.026	.032	.026	.032
b1	.013	.021	.013	.021
C	.015	.040	.015	.040
C1	.008	.012	.008	.012
C2	–	–	.005	.015
D	.320	.335	.485	.495
D1	.289	.293	.449	.453
D2	.225	.265	.390	.430
D3	.150 REF		.300 REF	
E	.520	.535	.585	.595
E1	.489	.493	.549	.553
E2	.422	.465	.490	.530
E3	.200 REF		.400 REF	
e	.050 BSC		.050 BSC	
ND/NE	4 / 5		7 / 9	

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
5. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
6. D1 & E1 SHOULD BE MEASURED FROM THE BOTTOM OF THE PACKAGE.

DOUBLE DENSITY STANDARD 5V LOGIC PRODUCTS

The demand for higher integration and higher speed continues to push the need for high-performance, high-density logic families. IDT has recently introduced a new series of extra-quiet, high-performance, 16-, 18-, and 20-bit logic functions. This exciting new ***Double Density*** family offers users significant board area savings, power savings, higher speeds, excellent guaranteed low noise characteristics, and guaranteed low output skew. The ***Double Density*** family is the premiere octal upgrade and is considered the high-speed, low-noise replacement for all existing CMOS and BiCMOS wide bus width products. Because of increased system bus widths, these bus and backplane drivers represent the next logical step in system integration.

To better accomodate various design applications, two output drive options are available.

64mA, High Drive Outputs

The first configuration, designated *54/74FCT16XXXT*, is intended to act as a direct replacement for two high-drive octal devices. These TTL-compatible, high drive (I_{OH} = –32mA and I_{OL} = 64mA) functions were designed for use in bus and backplane applications where heavy DC loads or termination may exist. These high drive devices meet or exceed all competitive BiCMOS double-wide and IDT's octal FCT-T DC specifications.

24mA, Balanced Drive Outputs

The second configuration, designated *54/74FCT162XXXT*, has new balanced drive outputs (I_{OH} = –24mA and I_{OL} = 24mA) with on-chip resistors. The combination of high dynamic drive and reduced DC drive makes these low-noise, balanced drive parts excellent for use in internal bus or motherboard designs, where overshoot and undershoot can be a problem.

Both configurations are available in the very small 48- and 56-pin Shrink Small Outline Packages (SSOP) and ceramic flatpacks. These fine-pitch SSOPs use approximately half the board area of two standard octal SOICs. All devices have been designed with flow-through pinouts and output edge rate control circuitry, providing up to a 70% improvement in ground bounce characteristics over older FCT octal devices. Pinouts are compatible with existing CMOS and BiCMOS double-wide families making system upgrades easy.

IDT's FCT-T double density devices use 40% less dynamic power, at all operating frequencies, than any advanced BiCMOS bus interface family, and, unlike their bipolar and BiCMOS counterparts, do not use any power in high impedance or static states (I_{CCZ}, I_{CCL}, I_{CCH}).

These devices are offered in several industry standard speed grades, FCT-T, FCT-AT, FCT-CT, and FCT-DT. All speed specifications are consistent with IDT's octal FCT and low-noise FCT-T devices, and are now guaranteed over an extended temperature and voltage range.

No other technology or product family offers the performance advantages that IDT's new Double Density family does. IDT plans on expanding this family with additional Double Density functions.

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Integrated Device Technology, Inc.

FAST CMOS 16-BIT BUFFER/LINE DRIVER

IDT54/74FCT16240T/AT/CT
IDT54/74FCT162240T/AT/CT

FEATURES:

- **Common features:**
  - 0.5 MICRON CEMOS™ Technology
  - **High-speed, low-power CEMOS replacement for ABT functions**
  - **Typical tSK(o) (Output Skew) < 250ps**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages
  - Extended commercial range of -40°C to +85°C
  - Vcc = 5V ±10%
  - Speed grades same as FCT-T Octals
- **Features for FCT16240T/AT/CT:**
  - High drive outputs (-32mA IOH, 64mA IOL)
  - Power off disable outputs permit "live insertion"
  - Typical VOLP (Output Ground Bounce) < 1.0V at Vcc = 5V, TA = 25°C
- **Features for FCT162240T/AT/CT:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical VOLP (Output Ground Bounce) < 0.6V at Vcc = 5V, TA = 25°C

DESCRIPTION:

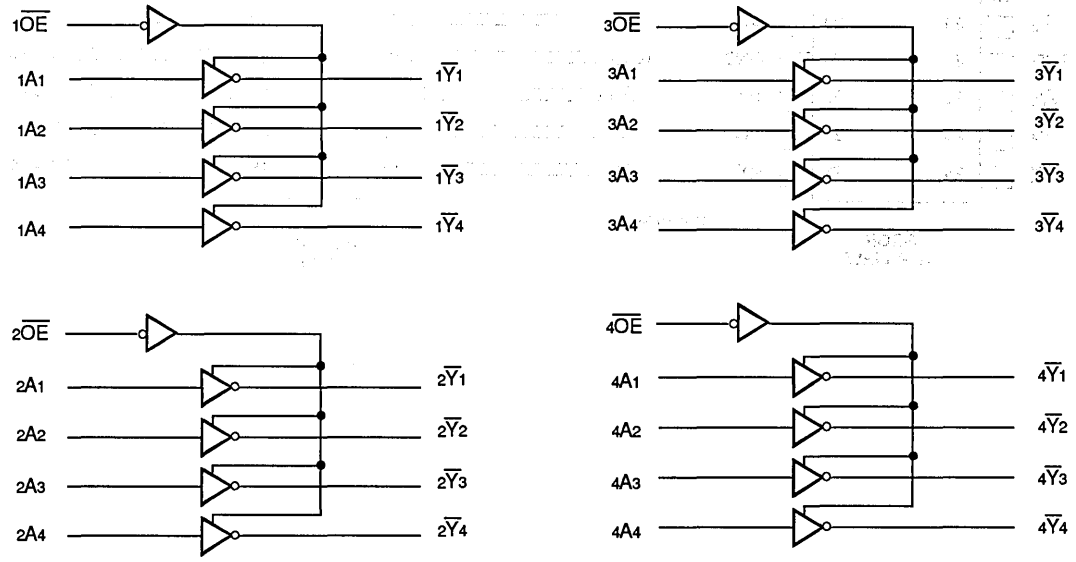
The IDT54/74FCT16240T/AT/CT and IDT54/74FCT162240T/AT/CT 16-bit buffer/line drivers are built using advanced CEMOS, dual metal CMOS technology. These high-speed, low-power devices offer bus/backplane interface capability with improved packing density. These devices have a flow-through organization for ease of board layout. The three-state controls are designed to operate these devices in a Quad-Nibble, Dual-Byte or single 16-bit word mode. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT16240T/AT/CT are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with Power-Off disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162240T/AT/CT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162240T/AT/CT are plug-in replacements for IDT54/74FCT16240T/AT/CT and 54/74ABT16240 for on-board interface applications.

5

FUNCTIONAL BLOCK DIAGRAM

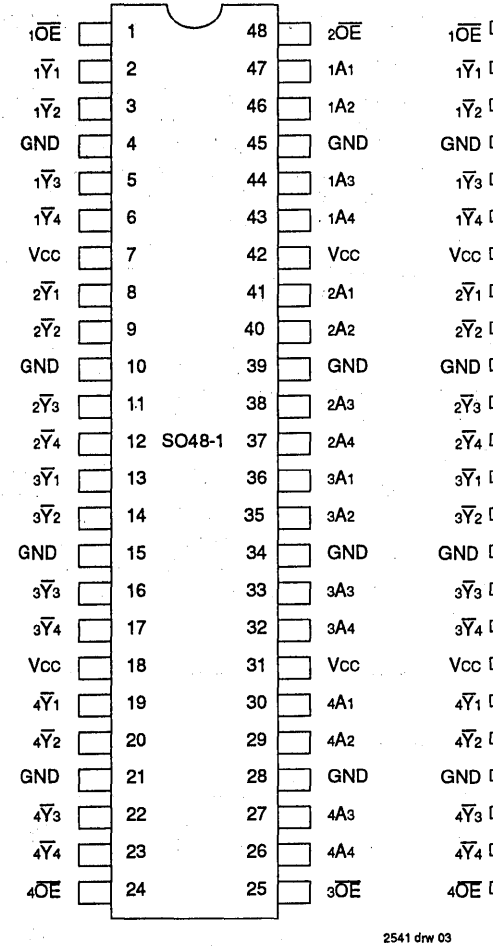


2541 drw 01

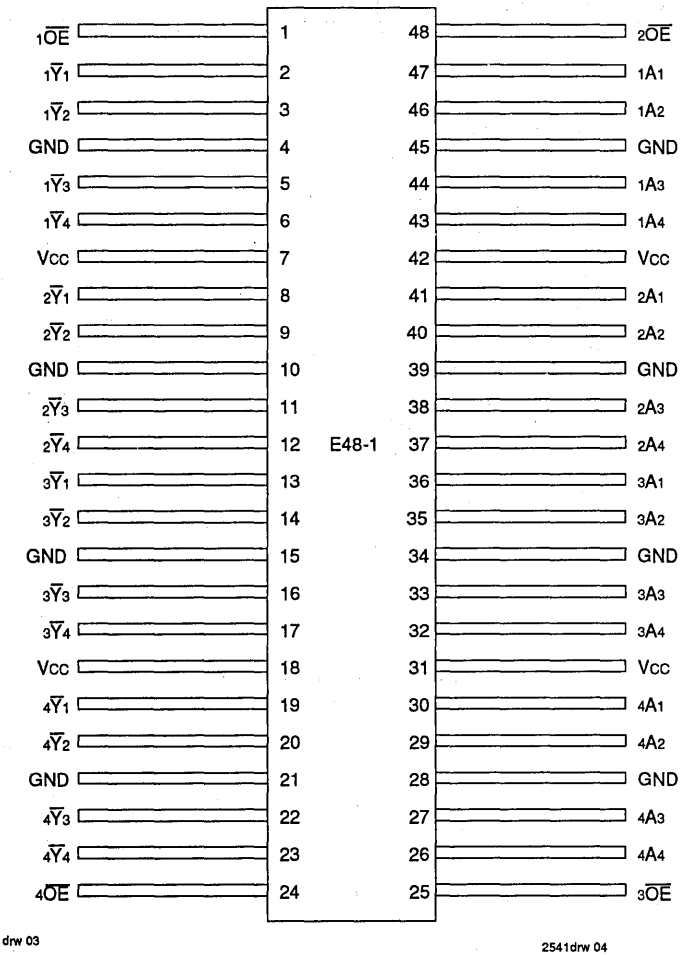
2541 drw 02

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



SSOP
TOP VIEW



CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}$	3–State Output Enable Inputs (Active LOW)
xAx	Data Inputs
$x\overline{Y}x$	3-State Outputs

2541 tbl 01

FUNCTION TABLE[1]

Inputs		Outputs
$x\overline{OE}$	xAx	$x\overline{Y}x$
L	L	H
L	H	L
H	X	Z

NOTE: 2541 tbl 02

1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2541 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2541 lnk 04

1. This parameter is measured at characterization but not tested.

5

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	±5	µA
	Input HIGH Current (I/O pins)			—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)			—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = 0.5V	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

2541 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16240T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±100	µA

2541 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162240T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2541 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.7	2.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	0.9	3.3	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = GND Sixteen Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	2.5	5.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.5	17.5[5]	

2541 tbl 08

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT16240T/162240T				FCT16240AT/162240AT				FCT16240CT/162240CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay xAx to $x\overline{Y}x$	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	1.5	4.3	1.5	4.7	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

2541 tbl 09

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Integrated Device Technology, Inc.

FAST CMOS 16-BIT BUFFER/LINE DRIVER

IDT54/74FCT16244T/AT/CT
IDT54/74FCT162244T/AT/CT

FEATURES:

- **Common features:**
  - 0.5 MICRON CEMOS™ Technology
  - **High-speed, low-power CEMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
  - Speed grades same as FCT-T Octals
- **Features for FCT16244T/AT/CT:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162244T/AT/CT:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

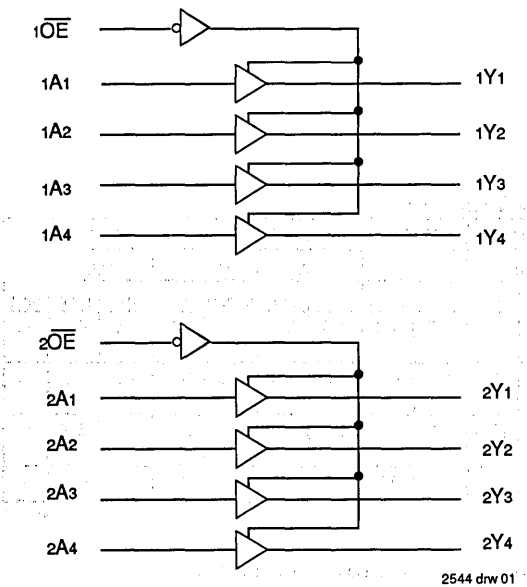
DESCRIPTION:

The IDT54/74FCT16244T/AT/CT and IDT54/74FCT162244T/AT/CT 16-bit buffer/line drivers are built using advanced CEMOS, dual metal CMOS technology. These high-speed, low-power devices offer bus/backplane interface capability with improved packing density. These devices have a flow-through organization for ease of board layout. The three-state controls are designed to operate these devices in a Quad-Nibble, Dual-Byte or single 16-bit word mode. All inputs are designed with hysteresis for improved noise margin.

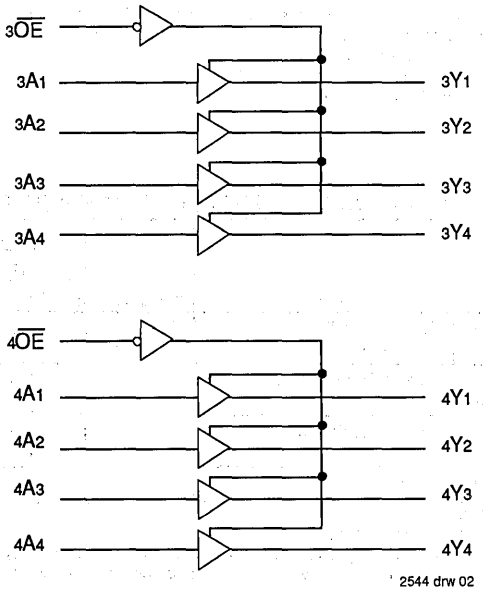
The IDT54/74FCT16244T/AT/CT are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with Power-Off disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162244T/AT/CT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162244T/AT/CT are plug-in replacements for the IDT54/74FCT16244T/AT/CT and 54/74ABT16244 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM



2544 drw 01



2544 drw 02

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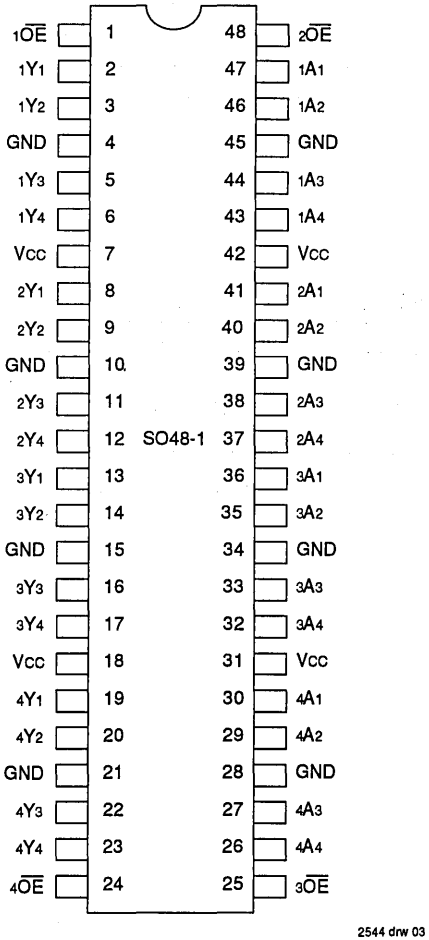
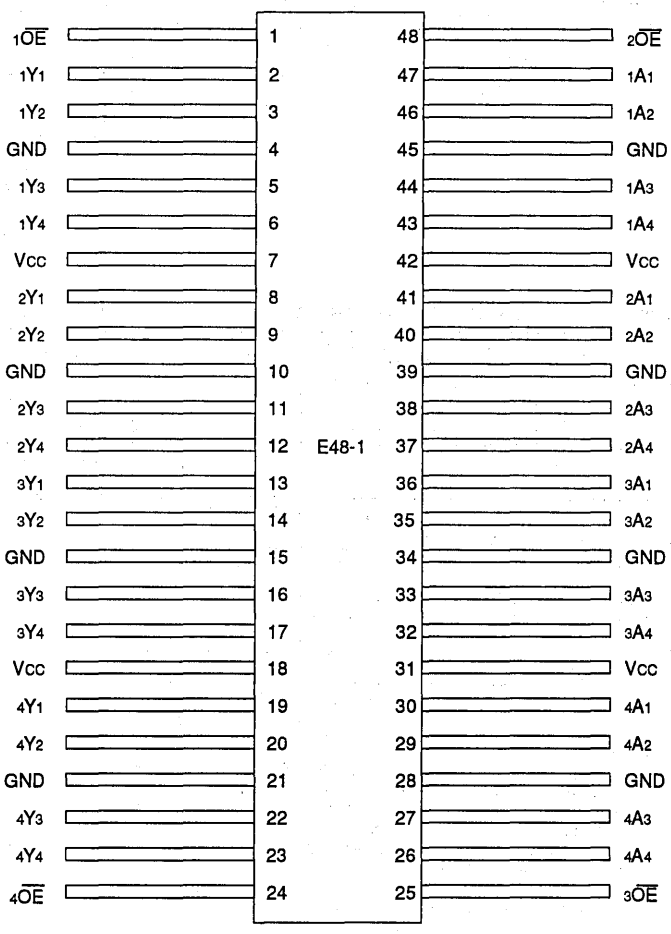
PIN CONFIGURATIONS



2544 drw 03

SSOP
TOP VIEW



2544 drw 04

CERPACK
TOP VIEW

5

PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}$	3–State Output Enable Inputs (Active LOW)
xAx	Data Inputs
xYx	3-State Outputs

2544 tbl 01

FUNCTION TABLE[1]

Inputs		Outputs
$x\overline{OE}$	xAx	xYx
L	L	L
L	H	H
H	X	Z

2544 tbl 02

NOTE:
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2544 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

2544 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	±5	µA
	Input HIGH Current (I/O pins)			—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)			—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = 0.5V	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

2544 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16244T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±100	µA

2544 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162244T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2544 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.

5

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND V_{IN} = 3.4V V_{IN} = GND	— —	0.7 0.9	2.5 3.3	mA
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = GND Sixteen Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND V_{IN} = 3.4V V_{IN} = GND	— —	2.5 6.5	5.5[5] 17.5[5]	

NOTES:
2544 tbl 08

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT16244T/162244T				FCT16244AT/162244AT				FCT16244CT/162244CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	1.5	4.1	1.5	4.6	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

NOTES:
2544 tbl 09

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Integrated Device Technology, Inc.

FAST CMOS 16-BIT BIDIRECTIONAL TRANSCEIVERS

IDT54/74FCT16245T/AT/CT
IDT54/74FCT162245T/AT/CT

FEATURES:

- **Common features:**
  - 0.5 MICRON CEMOS™ Technology
  - **High-speed, low-power CEMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
  - Speed grades same as FCT-T Octals
- **Features for FCT16245T/AT/CT:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162245T/AT/CT:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

DESCRIPTION:

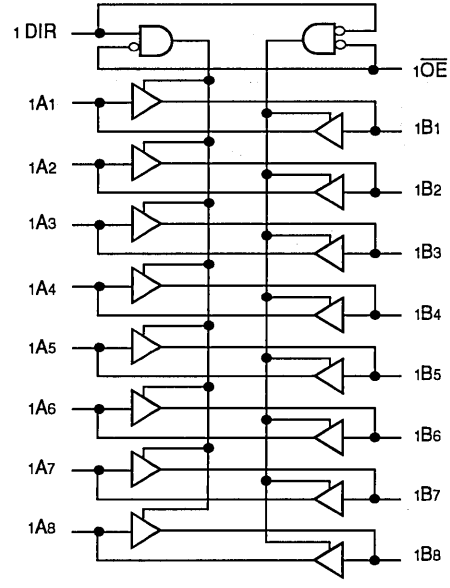
The IDT54/74FCT16245T/AT/CT and IDT54/74FCT162245T/AT/CT 16-bit transceivers are built using advanced CEMOS, dual metal CMOS technology. These high-speed, low-power transceivers are ideal for synchronous communication between two busses (A and B). The Direction and Output Enable controls are designed to operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver. The direction control pin (xDIR) controls the direction of data flow. The output enable pin ($x\overline{OE}$) overrides the direction control and disables both ports. All inputs are designed with hysteresis for improved noise margin.

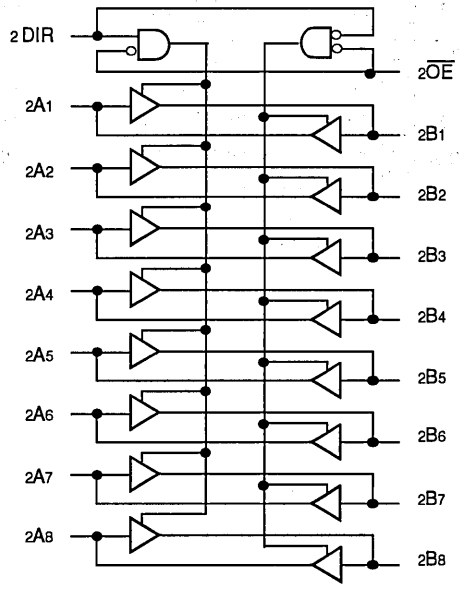
The IDT54/74FCT16245T/AT/CT are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with Power-Off Disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162245T/AT/CT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162245T/AT/CT are plug-in replacements for the IDT54/74FCT16245T/AT/CT and 54/74ABT16245 for on-board interface applications.

5

FUNCTIONAL BLOCK DIAGRAM



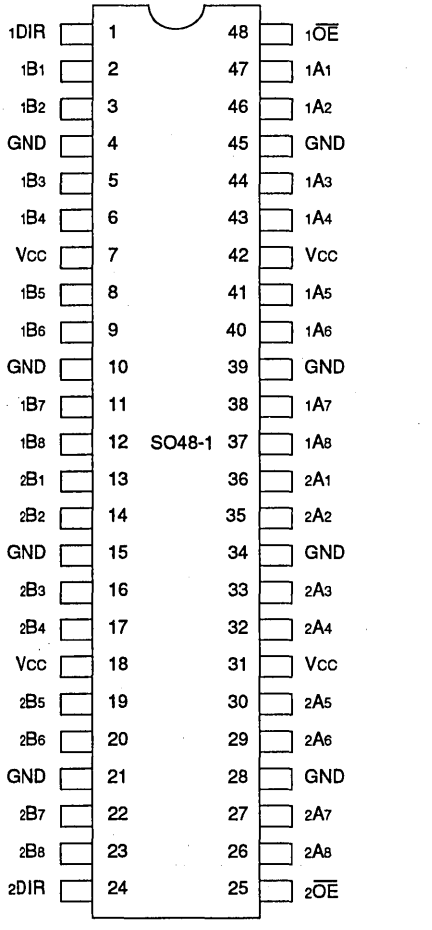


CEMOS is a trademark of Integrated Device Technology, Inc.

2545 drw 01

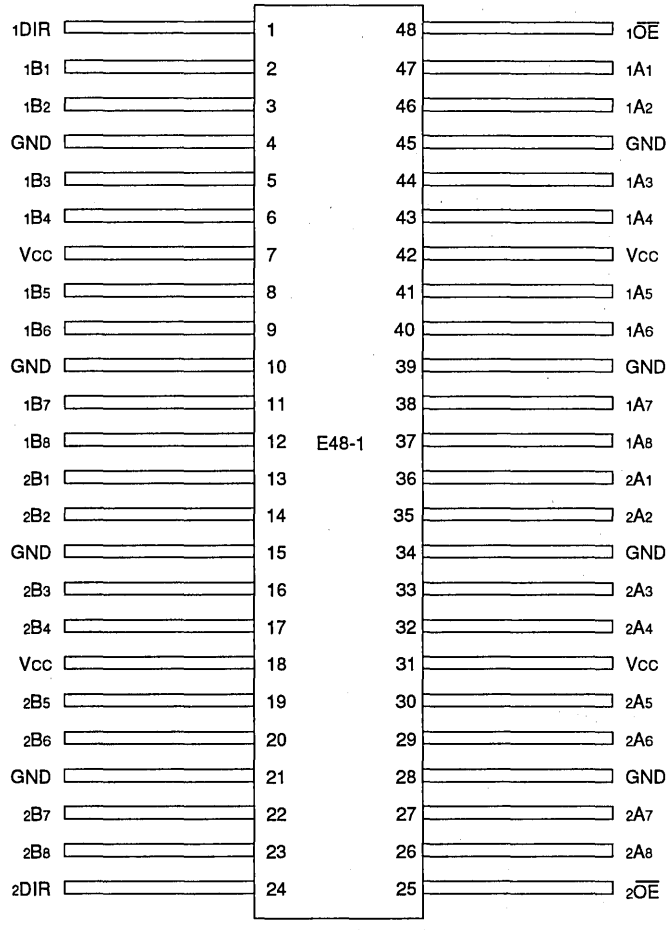
2545 drw 02

PIN CONFIGURATIONS



2545 drw 03

SSOP
TOP VIEW



2545 drw 04

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}$	Output Enable Input (Active LOW)
xDIR	Direction Control Input
xAx	Side A Inputs or 3-State Outputs
xBx	Side B Inputs or 3-State Outputs

2545 tbl 01

FUNCTION TABLE[1]

Inputs		
$x\overline{OE}$	xDIR	Outputs
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

NOTE: 2545 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2545 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2545 lnk 04

1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	±5	µA
	Input HIGH Current (I/O pins)			—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)			—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = 0.5V	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

2545 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16245T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±100	µA

2545 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162245T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2545 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = xDIR = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $x\overline{OE}$ = xDIR = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.7	2.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	0.9	3.3	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = xDIR = GND Sixteen Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	2.5	5.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.5	17.5[5]	

2545 tbl 08

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT16245T/162245T				FCT16245AT/162245AT				FCT16245CT/162245CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	7.5	1.5	4.6	1.5	4.9	1.5	4.1	1.5	4.5	ns
t_{PZH} t_{PZL}	Output Enable Time $x\overline{OE}$ to A or B		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time $x\overline{OE}$ to A or B		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns
t_{PZH} t_{PZL}	Output Enable Time xDIR to A or B[3]		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time xDIR to A or B[3]		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns
$t_{SK(o)}$	Output Skew[4]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

2545 tbl 09

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Integrated Device Technology, Inc.

FAST CMOS 16-BIT TRANSPARENT LATCHES

IDT54/74FCT16373T/AT/CT
IDT54/74FCT162373T/AT/CT

FEATURES:

- **Common features:**
  - 0.5 MICRON CEMOS™ Technology
  - **High-speed, low-power CEMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
  - Speed grades same as FCT-T Octals
- **Features for FCT16373T/AT/CT:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162373T/AT/CT:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

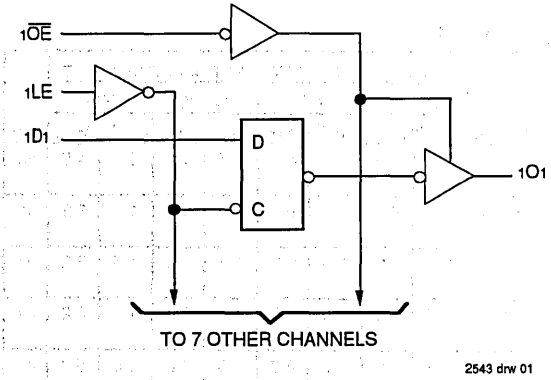
DESCRIPTION:

The IDT54/74FCT16373T/AT/CT and IDT54/74FCT162373T/AT/CT 16-bit transparent D-type latches are built using advanced CEMOS, dual metal CMOS technology. These high-speed, low-power latches are ideal for temporary storage of data. They can be used for implementing memory address latches, I/O ports, and bus drivers. The Output Enable and Latch Enable controls are organized to operate each device as two 8-bit latches or one 16-bit latch. Flow-through organization of signal pins facilitates ease of layout. All inputs are designed with hysteresis for improved noise margin.

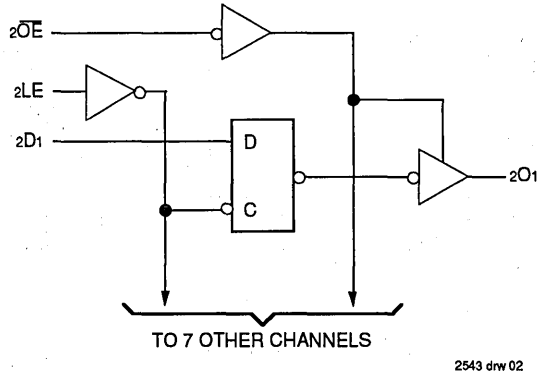
The IDT54/74FCT16373T/AT/CT are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with Power-Off Disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162373T/AT/CT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162373T/AT/CT are plug-in replacements for the IDT54/74FCT16373T/AT/CT and 54/74ABT16373 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM



2543 drw 01



2543 drw 02

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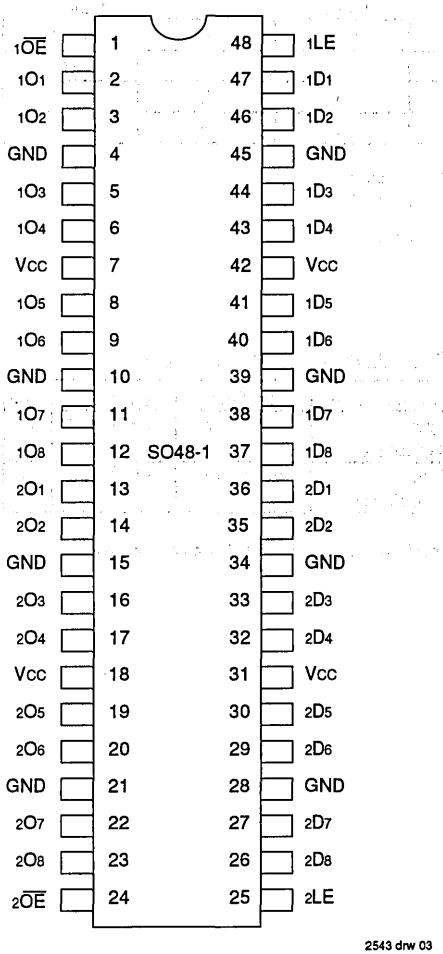
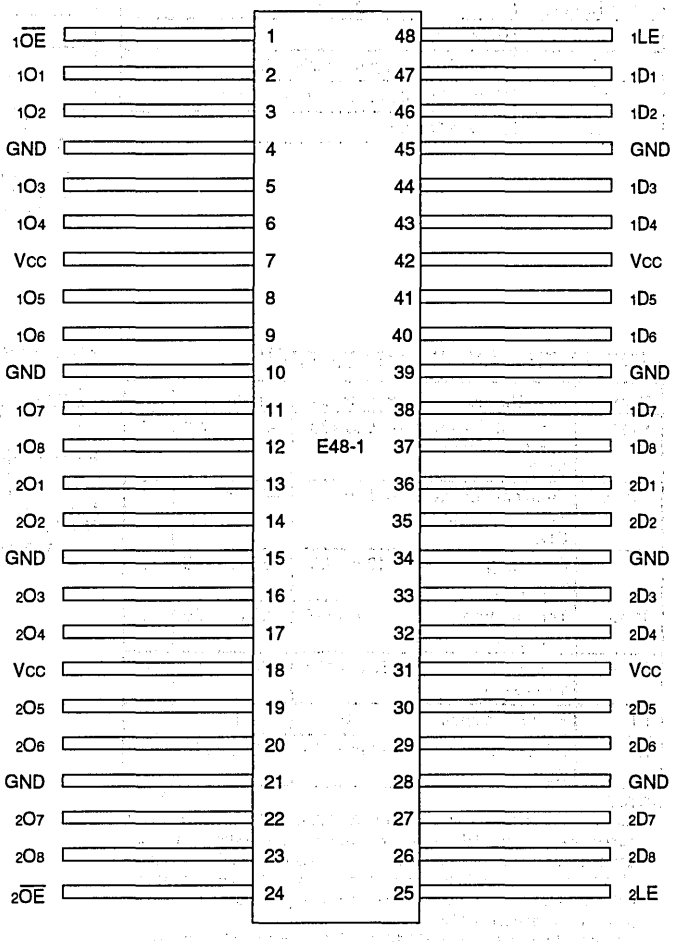
PIN CONFIGURATIONS



2543 drw 03

SSOP
TOP VIEW



2543 drw 04

CERPACK
TOP VIEW

5

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xLE	Latch Enable Inputs (Active HIGH)
$x\overline{OE}$	Output Enable Inputs (Active LOW)
xOx	3-State Outputs

2543 tbl 01

FUNCTION TABLE[1]

Inputs			Outputs
xDx	xLE	$x\overline{OE}$	xOx
H	H	L	H
L	H	L	L
X	X	H	Z

2543 tbl 02

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2543 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

2543 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	±5	µA
	Input HIGH Current (I/O pins)			—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)			—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = 0.5V	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	-140	-200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	-180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

2543 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16373T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±100	µA

2543 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162373T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2543 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi =10MHz 50% Duty Cycle $x\overline{OE}$ = GND xLE = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.7	2.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	0.9	3.3	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = GND xLE = V_{CC} Sixteen Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	2.5	5.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.5	17.5[5]	

2543 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16373T/162373T				FCT16373AT/162373AT				FCT16373CT/162373CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay xDx to xOx	CL = 50pF RL = 500Ω	1.5	8.0	1.5	8.5	1.5	5.2	1.5	5.6	1.5	4.2	1.5	5.1	ns
tPLH tPHL	Propagation Delay xLE to xOx		2.0	13.0	2.0	15.0	2.0	8.5	2.0	9.8	2.0	5.5	2.0	8.0	ns
tPZH tPZL	Output Enable Time		1.5	12.0	1.5	13.5	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns
tPHZ tPLZ	Output Disable Time		1.5	7.5	1.5	10.0	1.5	5.5	1.5	6.5	1.5	5.0	1.5	5.9	ns
tSU	Set-up Time HIGH or LOW, xDx to xLE		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, xDx to xLE		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	xLE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

NOTES:
2543 tbl 09

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

5

Integrated Device Technology, Inc.

FAST CMOS 16-BIT REGISTER (3-STATE)

IDT54/74FCT16374T/AT/CT
IDT54/74FCT162374T/AT/CT

FEATURES:

- **Common features:**
  - 0.5 MICRON CEMOS™ Technology
  - **High-speed, low-power CEMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
  - Speed grades same as FCT-T Octals
- **Features for FCT16374T/AT/CT:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162374T/AT/CT:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

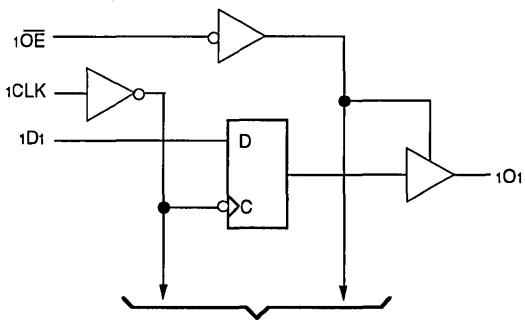
DESCRIPTION:

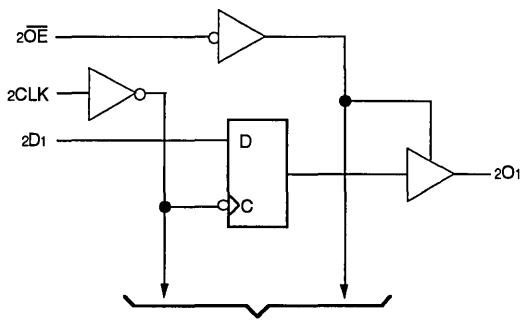
The IDT54/74FCT16374T/AT/CT and IDT54/74FCT162374T/AT/CT 16-bit edge-triggered D-type registers are built using advanced CEMOS, dual metal CMOS technology. These high-speed, low-power registers are ideal for use as buffer registers for data synchronization and storage. The Output Enable (xOE) and clock (xCLK) controls are organized to operate each device as two 8-bit registers or one 16-bit register with common clock. Flow-through organization of signal pins facilitates ease of layout. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT16374T/AT/CT are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with Power-Off Disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162374T/AT/CT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162374T/AT/CT are plug-in replacements for the IDT54/74FCT16374T/AT/CT and 54/74ABT16374 for on-board bus interface applications.

FUNCTIONAL BLOCK DIAGRAM





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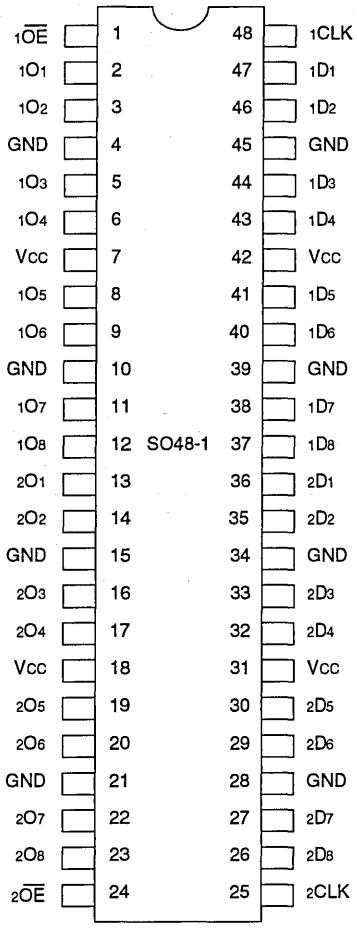
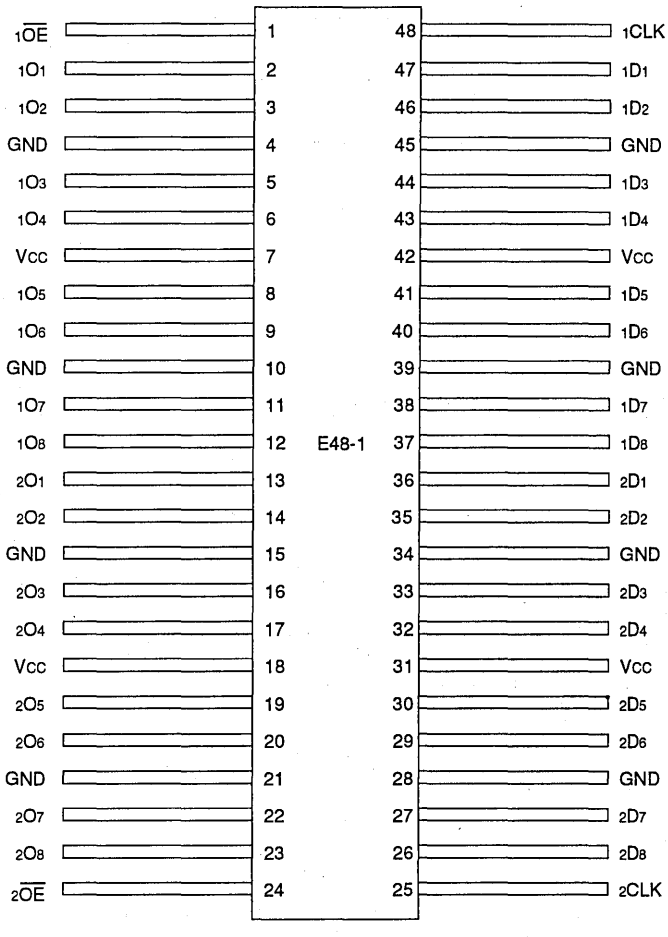
PIN CONFIGURATIONS



2542 drw 03

SSOP
TOP VIEW



2542 drw 04

CERPACK
TOP VIEW

5

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xCLK	Clock Inputs
xOx	3-State Outputs.
$\overline{xOE}$	3-State Output Enable Input (Active LOW)

2542 tbl 01

FUNCTION TABLE[1]

Function	Inputs			Outputs
	xDx	xCLK	$\overline{xOE}$	xOx
Hi-Z	X	L	H	Z
	X	H	H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

NOTE: 2542 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2542 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2542 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	±5	µA
	Input HIGH Current (I/O pins)			—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)			—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = 0.5V	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	-140	-200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	-180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

2542 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16374T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±100	µA

2542 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162374T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2542 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.

5

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $x\overline{OE}$ = GND f_i = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.7	2.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.2	4.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $x\overline{OE}$ = GND Sixteen Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.1	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	7.6	20[5]	

2542 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT16374T/162374T				FCT16374AT/162374AT				FCT16374CT/162374CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay xCLK to xOx	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	11.0	2.0	6.5	2.0	7.2	2.0	5.2	2.0	6.2	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	12.5	1.5	14.0	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	8.0	1.5	8.0	1.5	5.5	1.5	6.5	1.5	5.0	1.5	5.7	ns
t_{SU}	Set-up Time HIGH or LOW, xDx to xCLK		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, xDx to xCLK		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	xCLK Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

2542 tbl 09

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

5

Integrated Device Technology, Inc.

FAST CMOS 18-BIT REGISTERED TRANSCEIVER

IDT54/74FCT16500AT/CT
IDT54/74FCT162500AT/CT

FEATURES:

- **Common features:**
  - 0.5 MICRON CEMOS™ Technology
  - **High-speed, low-power CEMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16500AT/CT:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 0.8V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162500AT/CT:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.5V at V_{CC} = 5V, T_A = 25°C

DESCRIPTION:

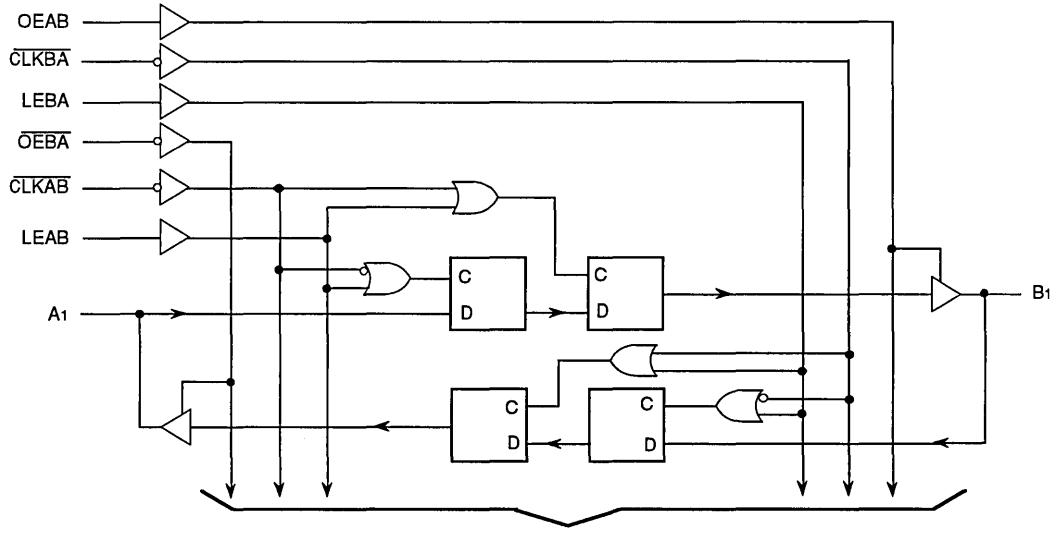
The IDT54/74FCT16500AT/CT and IDT54/74FCT162500AT/CT 18-bit registered transceivers are built using advanced CEMOS, dual metal CMOS technology.

These high-speed, low-power 18-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes. Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch enable (LEAB and LEBA) and clock ($\overline{CLKAB}$ and $\overline{CLKBA}$) inputs. For A-to-B data flow, the device operates in transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if $\overline{CLKAB}$ is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of $\overline{CLKAB}$. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar but requires using $\overline{OEBA}$, LEBA and $\overline{CLKBA}$. Flow-through organization of signal pins facilitates ease of layout. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT16500AT/CT are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with Power-Off Disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162500AT/CT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162500AT/CT are plug-in replacements for the IDT54/74FCT16500AT/CT and 54/74ABT16500 for on-board bus interface applications.

FUNCTIONAL BLOCK DIAGRAM



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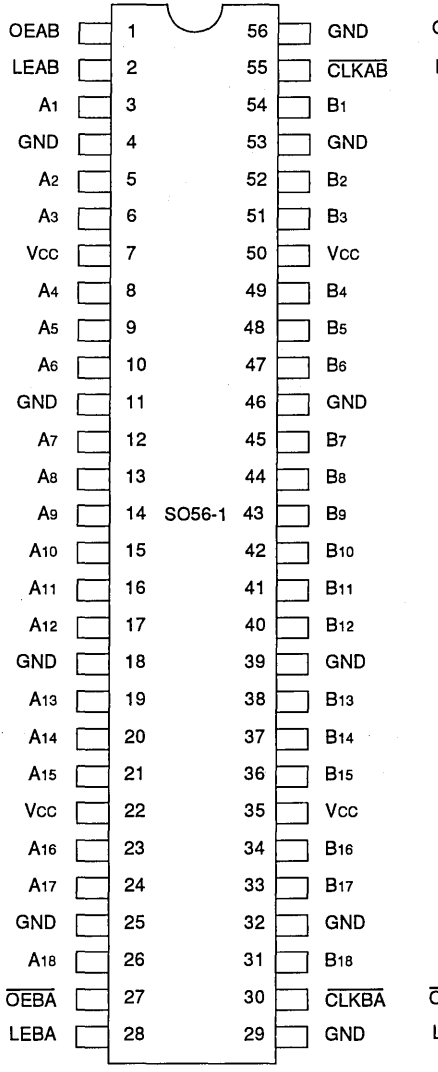
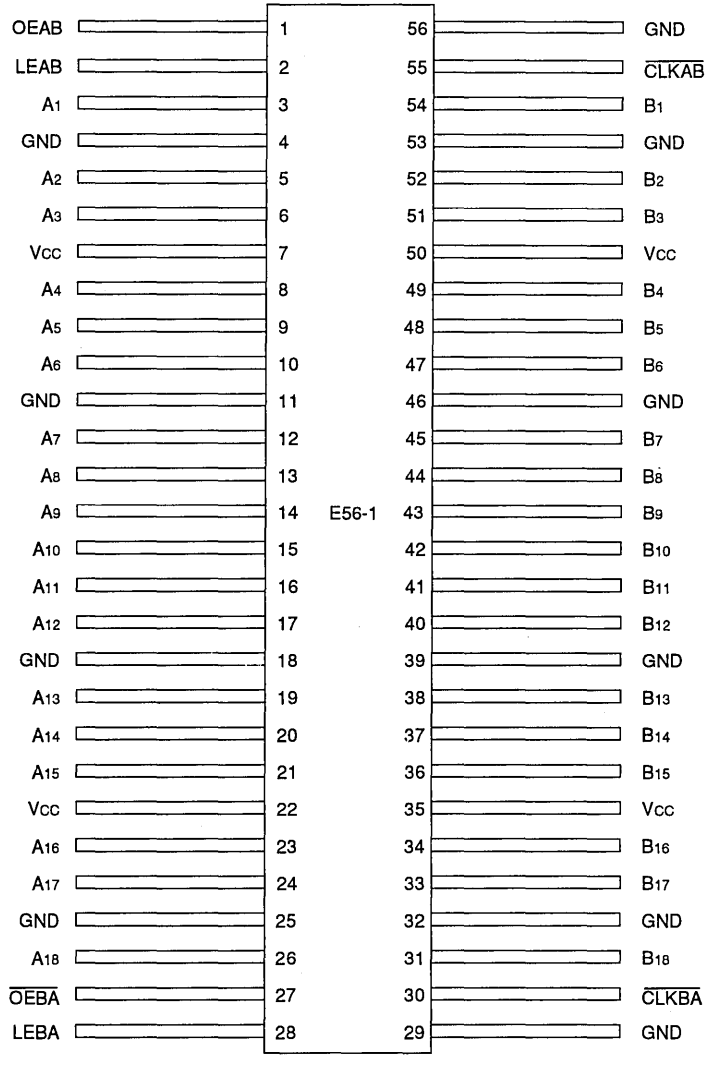
2548 drw 01

PIN CONFIGURATIONS



2548 drw 02

SSOP
TOP VIEW



2548 drw 03

CERPACK
TOP VIEW

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PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
$\overline{CLKAB}$	A-to-B Clock Input (Active LOW)
$\overline{CLKBA}$	B-to-A Clock Input (Active LOW)
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs

2548 tbl 01

FUNCTION TABLE[1,4]

Inputs				Outputs
OEAB	LEAB	$\overline{CLKAB}$	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B[2]
H	L	L	X	B[3]

NOTES: 2548 tbl 02

1. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was LOW before LEAB went LOW.
4. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   ↓ = HIGH-to-LOW Transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2548 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2548 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	±5	µA
	Input HIGH Current (I/O pins)			—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)			—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = 0.5V	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

2548 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16500T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±100	µA

2548 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162500T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2548 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open OEAB = $\overline{OEBA}$ = Vcc or GND One Input Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz ($\overline{CLKAB}$) 50% Duty Cycle OEAB = $\overline{OEBA}$ = Vcc LEAB = GND One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	0.8	2.7	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.3	4.2	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz ($\overline{CLKAB}$) 50% Duty Cycle OEAB = $\overline{OEBA}$ = Vcc LEAB = GND Eighteen Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	3.8	7.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	8.6	21.8[5]	

2548 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter		Condition[1]	FCT16500AT/162500AT				FCT16500CT/162500CT				Unit
				Com'l.		Mil.		Com'l.		Mil.		
				Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
f_{MAX}	$\overline{CLKAB}$ or $\overline{CLKBA}$ frequency[3]		C_L = 50pF	—	150	—	150	—	150	—	150	MHz
t_{PLH} t_{PHL}	Propagation Delay Ax to Bx or Bx to Ax		R_L = 500Ω	1.5	5.1	1.5	5.6	1.5	4.6	1.5	4.6	ns
t_{PLH} t_{PHL}	Propagation Delay LEBA to Ax, LEAB to Bx			1.5	5.6	1.5	6.0	1.5	5.3	1.5	5.6	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CLKBA}$ to Ax, $\overline{CLKAB}$ to Bx			1.5	5.6	1.5	6.0	1.5	5.3	1.5	5.4	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ to Ax, OEAB to Bx			1.5	6.0	1.5	6.4	1.5	5.6	1.5	6.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ to Ax, OEAB to Bx			1.5	5.6	1.5	6.0	1.5	5.2	1.5	5.6	ns
t_{SU}	Set-up Time HIGH or LOW Ax to $\overline{CLKAB}$, Bx to $\overline{CLKBA}$			3.0	—	3.0	—	3.0	—	3.0	—	ns
t_H	Hold Time HIGH or LOW Ax to $\overline{CLKAB}$, Bx to $\overline{CLKBA}$			0	—	0	—	0	—	0	—	ns
t_{SU}	Set-up Time HIGH or LOW	Clock HIGH		3.0	—	3.0	—	3.0	—	3.0	—	ns
	Ax to LEAB, Bx to LEBA	Clock LOW		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_H	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA			1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	LEAB or LEBA Pulse Width HIGH[3]			3.0	—	3.0	—	3.0	—	3.0	—	ns
t_W	$\overline{CLKAB}$ or $\overline{CLKBA}$ Pulse Width HIGH or LOW[3]			3.0	—	3.0	—	3.0	—	3.0	—	ns
$t_{SK(o)}$	Output Skew[4]			—	0.5	—	0.5	—	0.5	—	0.5	ns

NOTES:
2548 tbl 09

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

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Integrated Device Technology, Inc.

FAST CMOS 18-BIT REGISTERED TRANSCEIVER

IDT54/74FCT16501AT/CT
IDT54/74FCT162501AT/CT

FEATURES:

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  - 0.5 MICRON CEMOS™ Technology
  - **High-speed, low-power CEMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16501AT/CT:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 0.8V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162501AT/CT:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.5V at V_{CC} = 5V, T_A = 25°C

DESCRIPTION:

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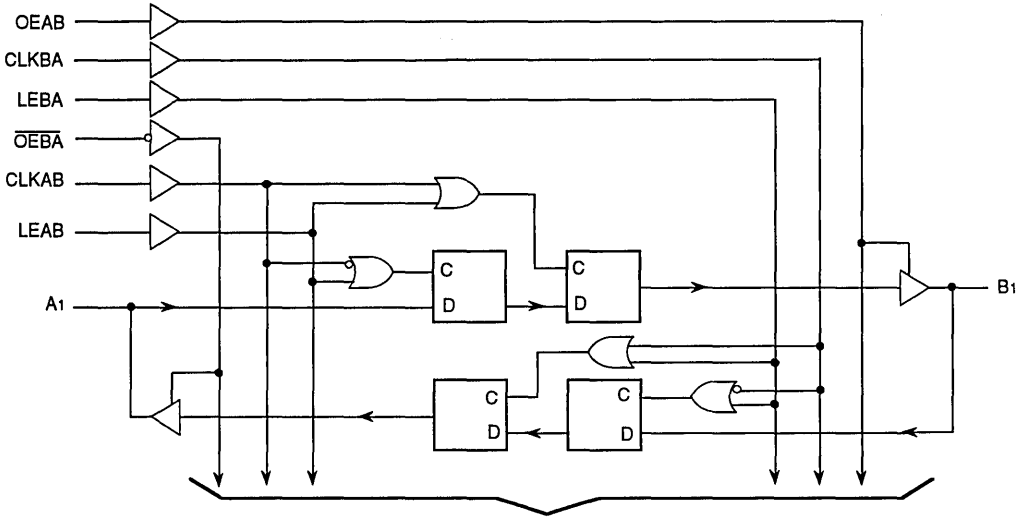
These high-speed, low-power 18-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes. Data flow in each direction is controlled by output-enable (OEAB and $\overline{OEBA}$), latch enable (LEAB and LEBA) and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in transparent mode when LEAB is HIGH. When LEAB isLOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. If LEAB isLOW, the A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar but requires using $\overline{OEBA}$, LEBA and CLKBA. Flow-through organization of signal pins facilitates ease of layout. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT16501AT/CT are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with Power-Off Disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162501AT/CT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162501AT/CT are plug-in replacements for the IDT54/74FCT16501AT/CT and 54/74ABT16501 for on-board bus interface applications.

FUNCTIONAL BLOCK DIAGRAM



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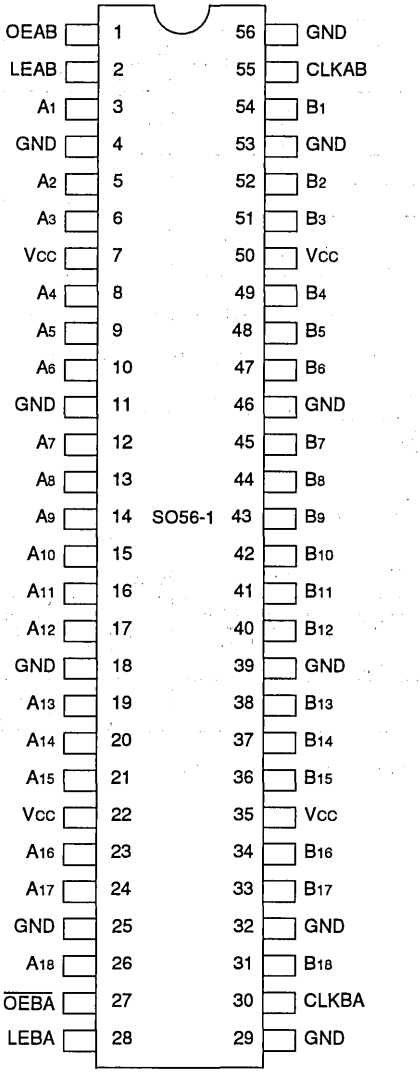
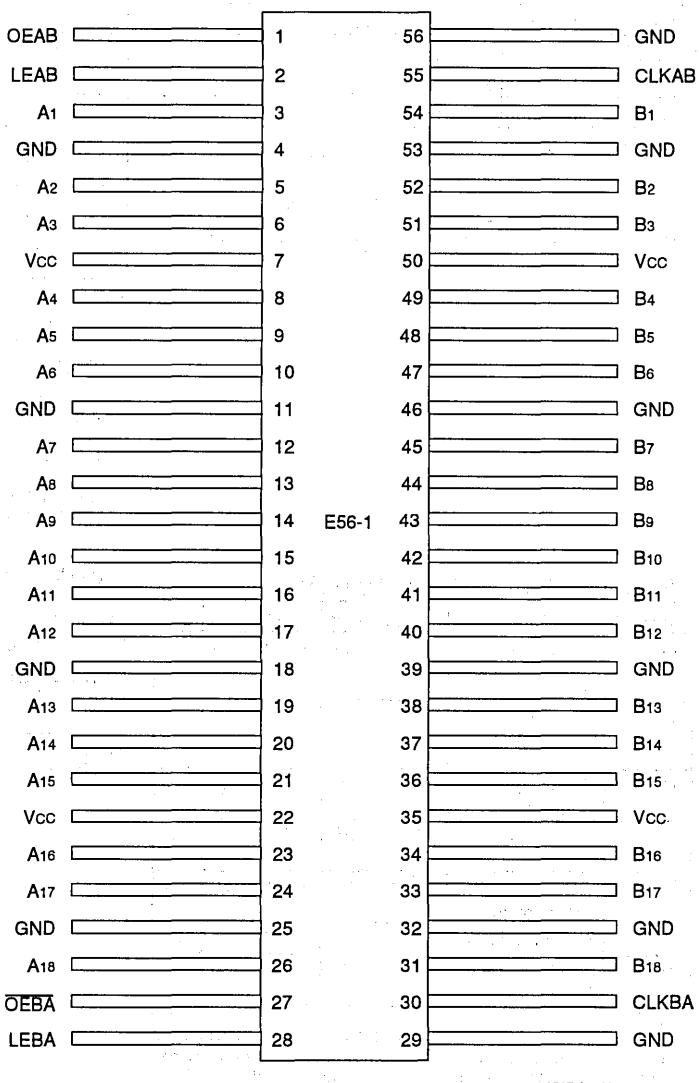
PIN CONFIGURATIONS



2547 drw 02

SSOP
TOP VIEW



2547 drw 03

CERPACK
TOP VIEW

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PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs

2547 tbl 01

FUNCTION TABLE[1,4]

Inputs				Outputs
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B[2]
H	L	H	X	B[3]

2547 tbl 02

NOTES:
1. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
4. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2547 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

2547 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	±5	µA
	Input HIGH Current (I/O pins)			—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)			—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = 0.5V	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

2547 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16501T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±100	µA

2547 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162501T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2547 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open OEAB = $\overline{OEBA}$ = V_{CC} or GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz (CLKAB) 50% Duty Cycle OEAB = $\overline{OEBA}$ = V_{CC} LEAB = GND One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	2.7	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.3	4.2	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz (CLKAB) 50% Duty Cycle OEAB = $\overline{OEBA}$ = V_{CC} LEAB = GND Eighteen Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	7.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	8.6	21.8[5]	

2547 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter		Condition[1]	FCT16501AT/162501AT				FCT16501CT/162501CT				Unit
				Com'l.		Mil.		Com'l.		Mil.		
				Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
fMAX	CLKAB or CLKBA frequency[3]			—	150	—	150	—	150	—	150	MHz
tPLH tPHL	Propagation Delay Ax to Bx or Bx to Ax		CL = 50pF RL = 500Ω	1.5	5.1	1.5	5.6	1.5	4.6	1.5	4.6	ns
tPLH tPHL	Propagation Delay LEBA to Ax, LEAB to Bx			1.5	5.6	1.5	6.0	1.5	5.3	1.5	5.6	ns
tPLH tPHL	Propagation Delay CLKBA to Ax, CLKAB to Bx			1.5	5.6	1.5	6.0	1.5	5.3	1.5	5.4	ns
tPZH tPZL	Output Enable Time $\overline{OEBA}$ to Ax, OEAB to Bx			1.5	6.0	1.5	6.4	1.5	5.6	1.5	6.0	ns
tPHZ tPLZ	Output Disable Time $\overline{OEBA}$ to Ax, OEAB to Bx			1.5	5.6	1.5	6.0	1.5	5.2	1.5	5.6	ns
tSU	Set-up Time HIGH or LOW Ax to CLKAB, Bx to CLKBA			3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA			0	—	0	—	0	—	0	—	ns
tSU	Set-up Time HIGH or LOW	Clock LOW		3.0	—	3.0	—	3.0	—	3.0	—	ns
	Ax to LEAB, Bx to LEBA	Clock HIGH		1.5	—	1.5	—	1.5	—	1.5	—	ns
tH	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA			1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	LEAB or LEBA Pulse Width HIGH[3]			3.0	—	3.0	—	3.0	—	3.0	—	ns
tW	CLKAB or CLKBA Pulse Width HIGH or LOW[3]			3.0	—	3.0	—	3.0	—	3.0	—	ns
tSK(o)	Output Skew[4]			—	0.5	—	0.5	—	0.5	—	0.5	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

2547 tbl 09

5

Integrated Device Technology, Inc.

FAST CMOS 16-BIT LATCHED TRANSCEIVER

IDT54/74FCT16543T/AT/CT/DT
IDT54/74FCT162543T/AT/CT/DT

FEATURES:

- **Common features:**
  - 0.5 MICRON CEMOS™ Technology
  - **High-speed, low-power CEMOS replacement for ABT functions**
  - **Typical tSK(o) (Output Skew) < 250ps**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages
  - Extended commercial range of -40°C to +85°C
  - Vcc = 5V ±10%
  - Speed grades same as FCT-T Octals
- **Features for FCT16543T/AT/CT/DT:**
  - High drive outputs (-32mA IOH, 64mA IOL)
  - Power off disable outputs permit "live insertion"
  - Typical VOLP (Output Ground Bounce) < 1.0V at Vcc = 5V, TA = 25°C
- **Features for FCT162543T/AT/CT/DT:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical VOLP (Output Ground Bounce) < 0.6V at Vcc = 5V, TA = 25°C

DESCRIPTION:

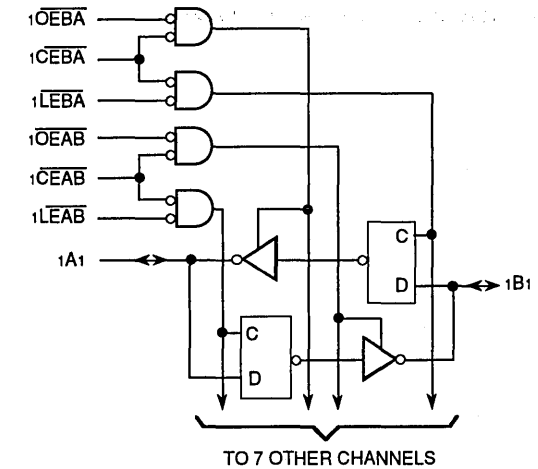
The IDT54/74FCT16543T/AT/CT/DT and IDT54/74FCT162543T/AT/CT/DT 16-bit latched transceivers are built using advanced CEMOS, dual metal CMOS technology.

These high-speed, low-power devices are organized as two independent 8-bit D-type latched transceivers with separate input and output control for each set to permit independent control of data flow in either direction. For example, the A-to-B Enable ($xCEAB$) must be LOW in order to enter data from A port or to output data from the B port. $xLEAB$ controls the latch function. When $xLEAB$ is LOW, the latches are transparent; a subsequent LOW-to-HIGH transition of $xLEAB$ signal puts the A latches in the storage mode. $xOEAB$ performs output enable function on the B port. Data flow from B port to A port is similar but requires using $xCEBA$, $xLEBA$, and $xOEBA$ inputs. Flow-through organization of signal pins facilitates ease of layout. All inputs are designed with hysteresis for improved noise margin.

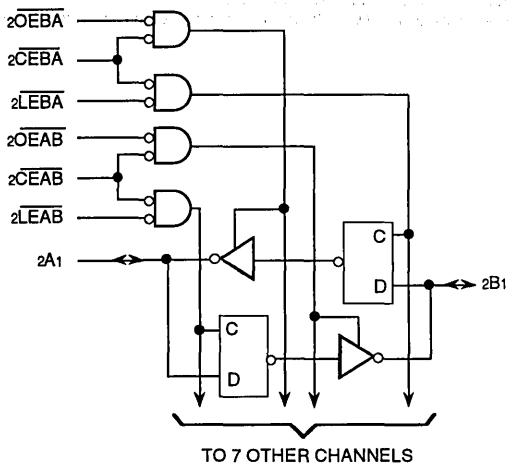
The IDT54/74FCT16543T/AT/CT/DT are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with Power-Off Disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162543T/AT/CT/DT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162543T/AT/CT/DT are plug-in replacements for the IDT54/74FCT16543T/AT/CT/DT and 54/74ABT16543 for on-board bus interface applications.

FUNCTIONAL BLOCK DIAGRAM



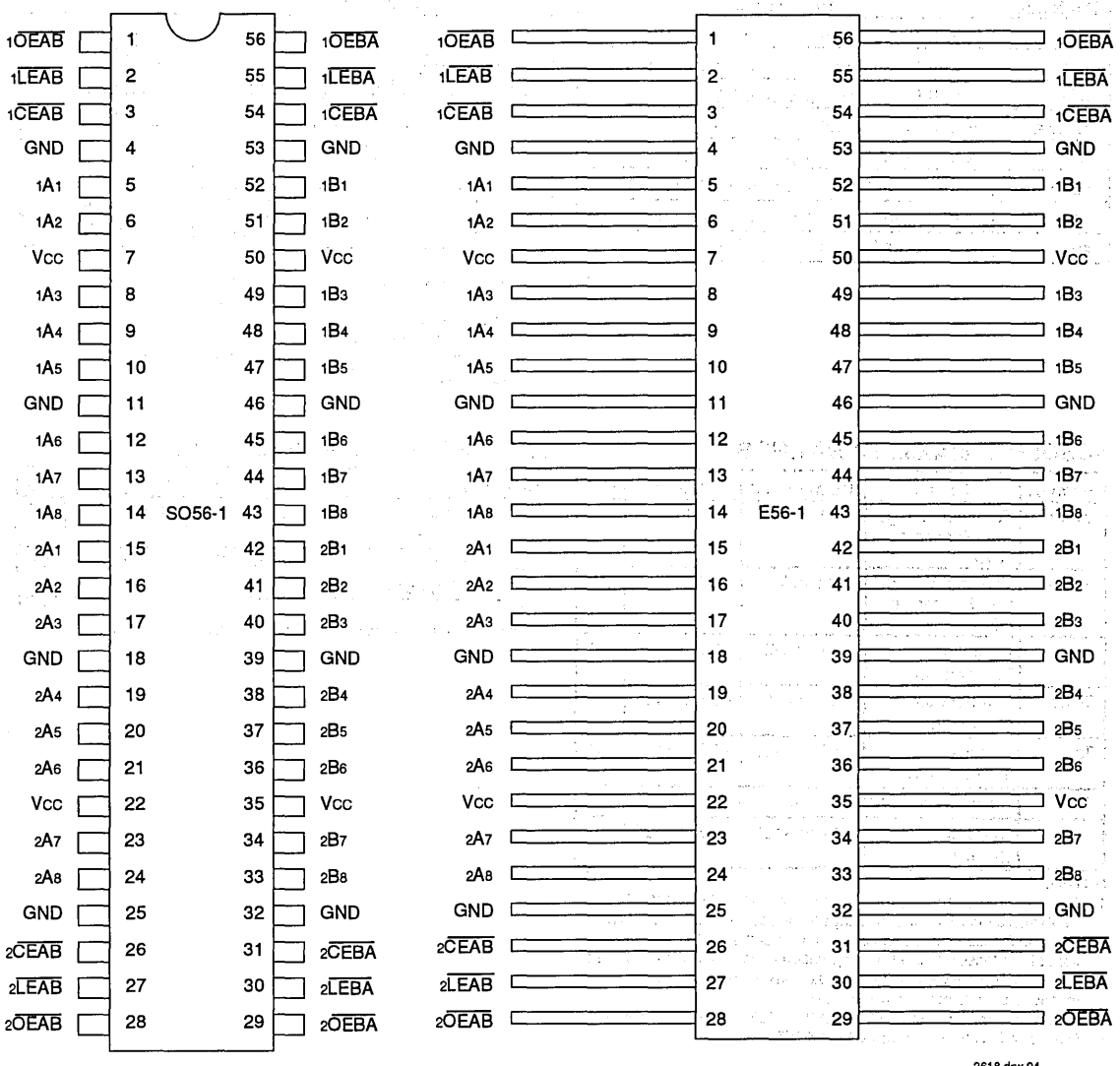
2618 drw 01



2618 drw 02

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2618 drw 03

SSOP
TOP VIEW

2618 drw 04

CERPACK
TOP VIEW

5

PIN DESCRIPTION

Pin Names	Description
$x\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$x\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$x\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$x\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$x\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$x\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs

2618 tbl 01

FUNCTION TABLE[1, 2]

For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
$x\overline{CEAB}$	$x\overline{LEAB}$	$x\overline{OEAB}$	xAx to xBx	xBx
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

NOTES: 2618 tbl 02

1. * Before $x\overline{LEAB}$ LOW-to-HIGH Transition
   H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care or Irrelevant
2. A-to-B data flow shown; B-to-A flow control is the same, except using $x\overline{CEBA}$, $x\overline{LEBA}$ and $x\overline{OEBA}$.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2618 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2618 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5.0V \pm 10\%$; Military: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	$V_I = V_{CC}$	—	—	±5	µA
	Input HIGH Current (I/O pins)			—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)			—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = 0.5V	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

2618 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16543T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		$V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \le 4.5V$		—	—	±100	µA

2618 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162543T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, $V_{IN} = V_{IH}$ or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, $V_{IN} = V_{IH}$ or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2618 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open x$\overline{CEAB}$ and x$\overline{OEAB}$ = GND x$\overline{CEBA}$ = Vcc One Input Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz 50% Duty Cycle x$\overline{LEAB}$, x$\overline{CEAB}$ and x$\overline{OEAB}$= GND x$\overline{CEBA}$ = Vcc One Bit Toggling	V_{IN} = Vcc V_{IN} = GND	—	0.7	2.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	0.9	3.3	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz 50% Duty Cycle x$\overline{LEAB}$, x$\overline{CEAB}$ and x$\overline{OEAB}$= GND x$\overline{CEBA}$ = Vcc Sixteen Bits Toggling	V_{IN} = Vcc V_{IN} = GND	—	2.5	5.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.5	17.5[5]	

2618 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16543T/162543T				FCT16543AT/162543AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	CL = 50pF RL = 500Ω	2.5	8.5	2.5	10.0	2.5	6.5	2.5	7.5	ns
tPLH tPHL	Propagation Delay $x\overline{LEBA}$ to xAx, $x\overline{LEAB}$ to xBx		2.5	12.5	2.5	14.0	2.5	8.0	2.5	9.0	ns
tPZH tPZL	Output Enable Time $x\overline{OEBA}$ or $x\overline{OEAB}$ to xAx or xBx $x\overline{CEBA}$ or $x\overline{CEAB}$ to xAx or xBx		2.0	12.0	2.0	14.0	2.0	9.0	2.0	10.0	ns
tPHZ tPLZ	Output Disable Time $x\overline{OEBA}$ or $x\overline{OEAB}$ to xAx or xBx $x\overline{CEBA}$ or $x\overline{CEAB}$ to xAx or xBx		2.0	9.0	2.0	13.0	2.0	7.5	2.0	8.5	ns
tSU	Set-up Time HIGH or LOW xAx or xBx to $x\overline{LEAB}$ or $x\overline{LEBA}$		3.0	—	3.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW xAx or xBx to $x\overline{LEAB}$ or $x\overline{LEBA}$		2.0	—	2.0	—	2.0	—	2.0	—	ns
tW	$x\overline{LEBA}$ or $x\overline{LEAB}$ Pulse Width LOW		5.0	—	5.0	—	5.0	—	5.0	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2618 tbl 09

Symbol	Parameter	Condition[1]	FCT16543CT/162543CT				FCT16543DT/162543DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	CL = 50pF RL = 500Ω	1.5	5.3	1.5	6.1	2.5	4.4	—	—	ns
tPLH tPHL	Propagation Delay $x\overline{LEBA}$ to xAx, $x\overline{LEAB}$ to xBx		1.5	7.0	1.5	8.0	2.5	5.0	—	—	ns
tPZH tPZL	Output Enable Time $x\overline{OEBA}$ or $x\overline{OEAB}$ to xAx or xBx $x\overline{CEBA}$ or $x\overline{CEAB}$ to xAx or xBx		1.5	8.0	1.5	9.0	2.0	5.4	—	—	ns
tPHZ tPLZ	Output Disable Time $x\overline{OEBA}$ or $x\overline{OEAB}$ to xAx or xBx $x\overline{CEBA}$ or $x\overline{CEAB}$ to xAx or xBx		1.5	6.5	1.5	7.5	2.0	4.3	—	—	ns
tSU	Set-up Time, HIGH or LOW xAx or xBx to $x\overline{LEBA}$ or $x\overline{LEAB}$		2.0	—	2.0	—	1.5	—	—	—	ns
tH	Hold Time HIGH or LOW xAx or xBx to $x\overline{LEBA}$ or $x\overline{LEAB}$		2.0	—	2.0	—	1.5	—	—	—	ns
tW	$x\overline{LEBA}$ or $x\overline{LEAB}$ Pulse Width LOW		5.0	—	5.0	—	3.0[4]	—	—	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

NOTES:

2618 tbl 10

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

Integrated Device Technology, Inc.

FAST CMOS 16-BIT BUS TRANSCEIVER/ REGISTERS (3-STATE)

IDT54/74FCT16646T/AT/CT
IDT54/74FCT162646T/AT/CT

FEATURES:

- **Common features:**
  - 0.5 MICRON CEMOS™ Technology
  - **High-speed, low-power CEMOS replacement for ABT functions**
  - **Typical tSK(o) (Output Skew) < 250ps**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages
  - Extended commercial range of -40°C to +85°C
  - Vcc = 5V ±10%
  - Speed grades same as FCT-T Octals
- **Features for FCT16646T/AT/CT:**
  - High drive outputs (-32mA IOH, 64mA IOL)
  - Power off disable outputs permit "live insertion"
  - Typical VOLP (Output Ground Bounce) < 1.0V at Vcc = 5V, TA = 25°C
- **Features for FCT162646T/AT/CT:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical VOLP (Output Ground Bounce) < 0.6V at Vcc = 5V, TA = 25°C

DESCRIPTION:

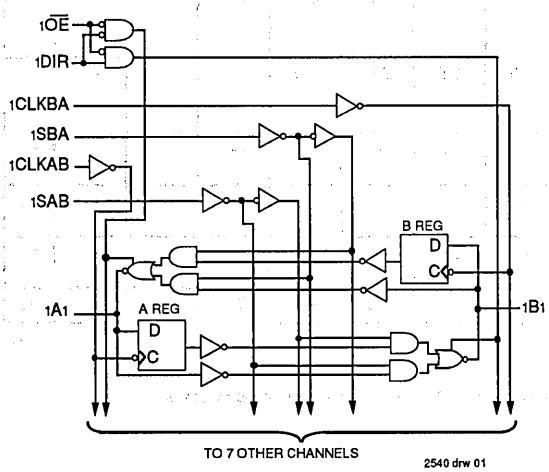
The IDT54/74FCT16646T/AT/CT and IDT54/74FCT162646T/AT/CT 16-bit registered transceivers are built using advanced CEMOS, dual metal CMOS technology.

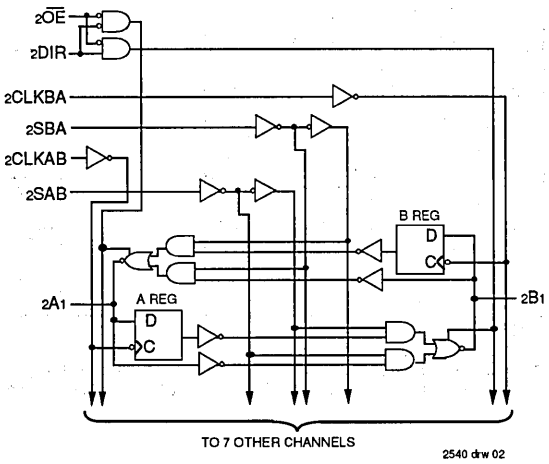
These high-speed, low-power devices are organized as two independent 8-bit bus transceivers with 3-state D-type registers. The control circuitry is organized for multiplexed transmission of data between A bus and B bus either directly or from the internal storage registers. Each 8-bit transceiver/ register features direction control (xDIR), over-riding Output Enable control ($x\overline{OE}$) and Select lines (xSAB and xSBA) to select either real-time data or stored data. Separate clock inputs are provided for A and B port registers. Data on the A or B data bus, or both, can be stored in the internal registers by the LOW-to-HIGH transitions at the appropriate clock pins. Flow-through organization of signal pins facilitates ease of layout. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT16646T/AT/CT are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with Power-Off Disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162646T/AT/CT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times– reducing the need for external series terminating resistors. The IDT54/74FCT162646T/AT/CT are plug-in replacements for the IDT54/74FCT16646T/AT/CT and 54/74ABT16646 for on-board bus interface applications.

FUNCTIONAL BLOCK DIAGRAM





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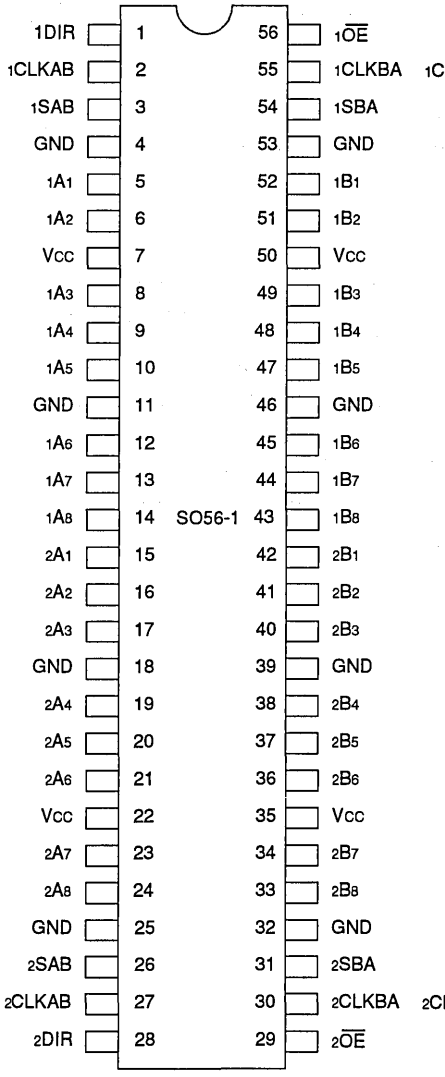
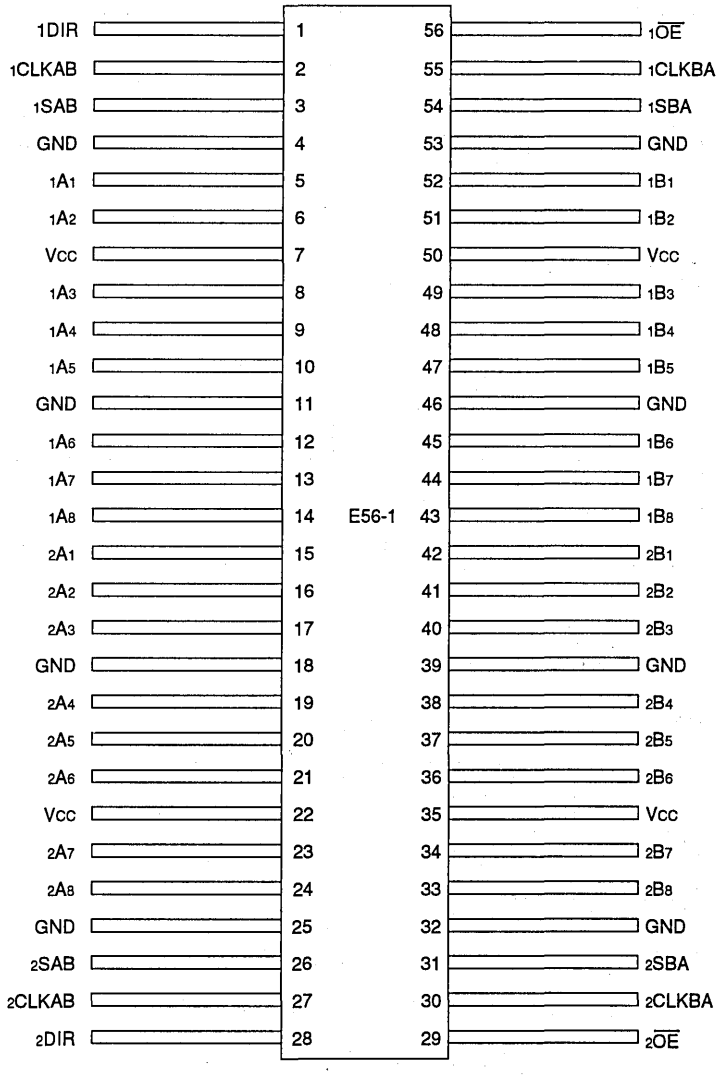
PIN CONFIGURATIONS



2540 drw 03

SSOP
TOP VIEW



2540 drw 04

CERPACK
TOP VIEW

5

PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xDIR, $x\overline{OE}$	Output Enable Inputs

2540 tbl 01

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE:
1. This parameter is measured at characterization but not tested.

2540 tbl 02

FUNCTION TABLE(2)

Inputs						Data I/O(1)		Operation or Function
$x\overline{OE}$	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

NOTES:
1. The data output functions may be enabled or disabled by various signals at the $x\overline{OE}$ or xDIR inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition

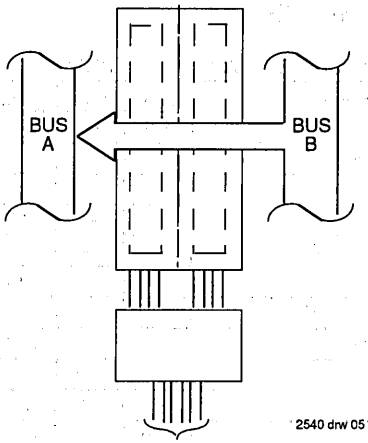
2634 tbl 03

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

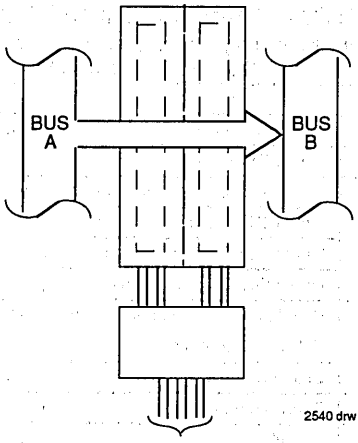
NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

2540 tbl 04



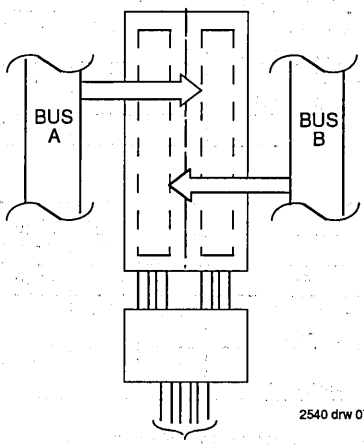
xDIR	$\overline{xOE}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO A



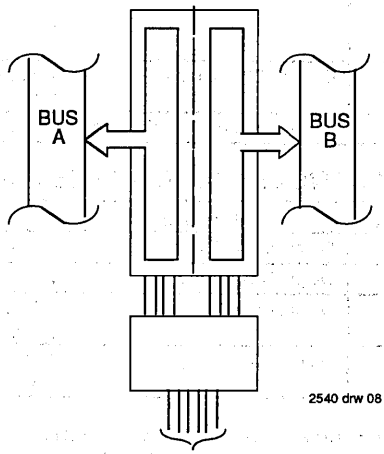
xDIR	$\overline{xOE}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	X	X	L	X

REAL-TIME TRANSFER BUS A TO B



xDIR	$\overline{xOE}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	↑	X	X	X
L	L	X	↑	X	X
X	H	↑	↑	X	X

STORAGE FROM A AND/OR B



xDIR (1)	$\overline{xOE}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

TRANSFER STORED DATA TO A AND/OR B

NOTE:
1. Cannot transfer data to A bus and B bus simultaneously.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	±5	µA
	Input HIGH Current (I/O pins)			—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)			—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = 0.5V	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

2540 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16646T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±100	µA

2540 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162646T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2540 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open xDIR = $x\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle xDIR = $x\overline{OE}$ = GND One Bit Toggling fi = 5MHz 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	0.8	2.7	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.3	4.2	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle xDIR = $x\overline{OE}$ = GND Sixteen Bits Toggling fi = 2.5MHz 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	3.8	7.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	8.3	21[5]	

2540 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

5

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT16646T/162646T				FCT16646AT/162646AT				FCT16646CT/162646CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	1.5	5.4	1.5	6.0	ns
t_{PZH} t_{PZL}	Output Enable Time xDIR or x$\overline{OE}$ to Bus		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	1.5	7.8	1.5	8.9	ns
t_{PHZ} t_{PLZ}	Output Disable Time xDIR or x$\overline{OE}$ to Bus		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	1.5	6.3	1.5	7.7	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	1.5	5.7	1.5	6.3	ns
t_{PLH} t_{PHL}	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	1.5	6.2	1.5	7.0	ns
t_{SU}	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	Clock Pulse Width HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

2540 tbl 09

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Integrated Device Technology, Inc.

FAST CMOS 16-BIT BUS TRANSCEIVER/ REGISTER

IDT54/74FCT16652T/AT/CT
IDT54/74FCT162652T/AT/CT

FEATURES:

- **Common features:**
  - 0.5 MICRON CEMOS™ Technology
  - **High-speed, low-power CEMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
  - Speed grades same as FCT-T Octals
- **Features for FCT16652T/AT/CT:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162652T/AT/CT:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

DESCRIPTION:

The IDT54/74FCT16652T/AT/CT and IDT54/74FCT162652T/AT/CT 16-bit registered transceivers are built using advanced CEMOS, dual metal CMOS technology. These high-speed, low-power devices are organized as two independant 8-bit bus transceivers with 3-state D-type registers. For example, the xOEAB and x$\overline{OEBA}$ signals control the transceiver functions.

xSAB and xSBA control pins are provided to select either real time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real time data. A LOW input level selects real-time data and a HIGH level selects stored data.

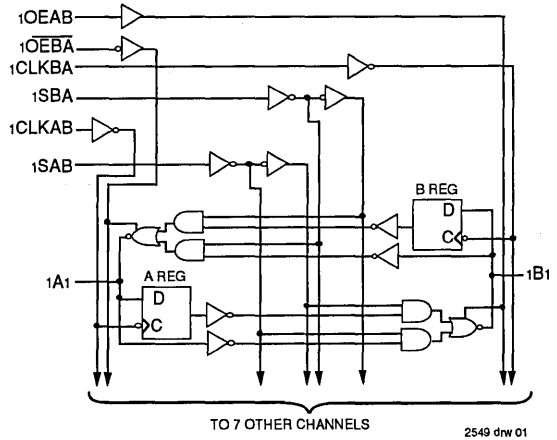
Data on the A or B data bus, or both, can be stored in the internal D-flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (xCLKAB or xCLKBA), regardless of the select or enable control pins. Flow-through organization of signal pins facilitates ease of layout. All inputs are designed with hysteresis for improved noise margin.

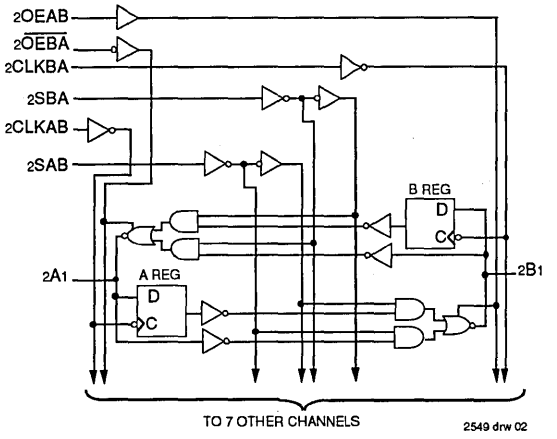
The IDT54/74FCT16652T/AT/CT are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with Power-Off Disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162652T/AT/CT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162652T/AT/CT are plug-in replacements for the IDT54/74FCT16652T/AT/CT and 54/74ABT16652 for on-board bus interface applications.

5

FUNCTIONAL BLOCK DIAGRAM





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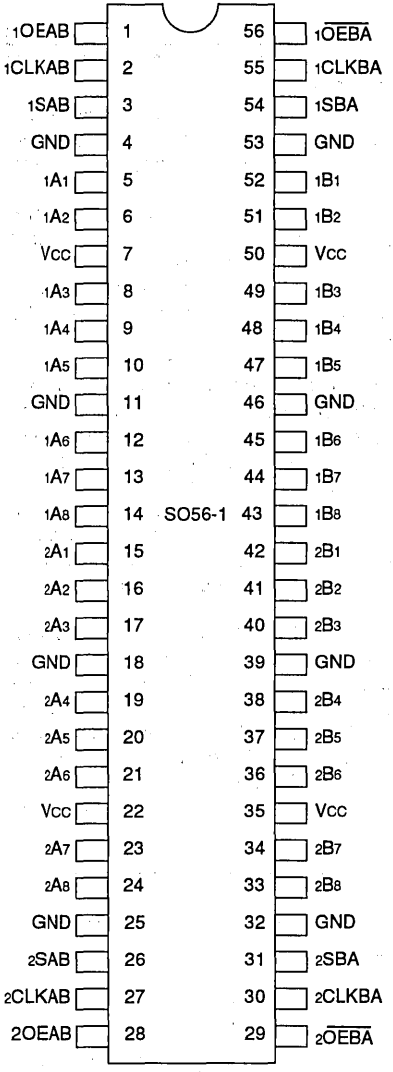
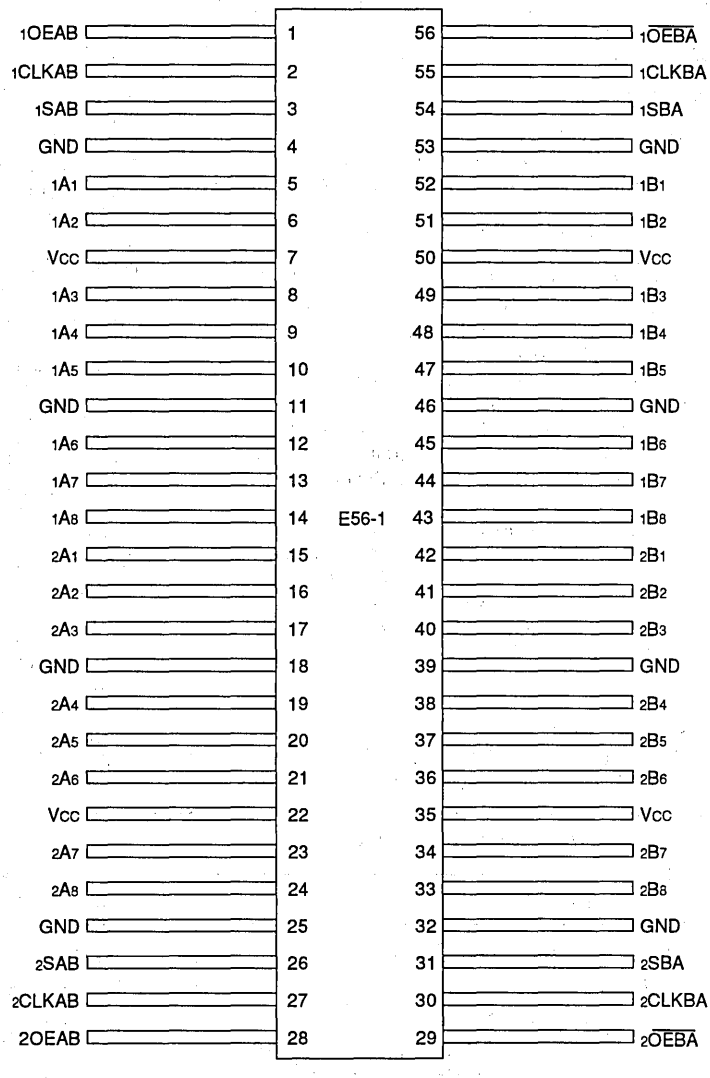
PIN CONFIGURATIONS



2549 drw 03

SSOP
TOP VIEW



2549 drw 04

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xOEAB, x$\overline{\text{OEBA}}$	Output Enable Inputs

2549 tbl 01

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2549 lnk 02
1. This parameter is measured at characterization but not tested.

FUNCTION TABLE(3)

Inputs						Data I/O(1)		Operation or Function
xOEAB	x$\overline{\text{OEBA}}$	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified(1)	Store A, Hold B
H	H	↑	↑	X(2)	X	Input	Output	Store A in Both Registers
L	X	H or L	↑	X	X	Unspecified(1)	Input	Hold A, Store B
L	L	↑	↑	X	X(2)	Output	Input	Store B in both Registers
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

NOTES: 2549 tbl 03
1. The data output functions may be enabled or disabled by various signals at the xOEAB or x$\overline{\text{OEBA}}$ inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.
3. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2549 lnk 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

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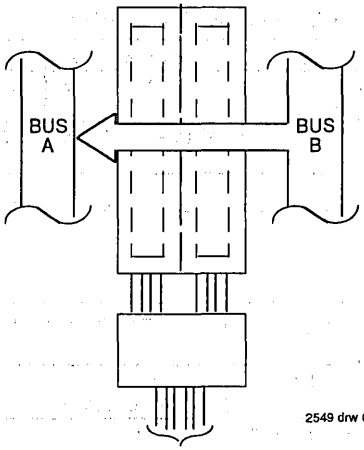
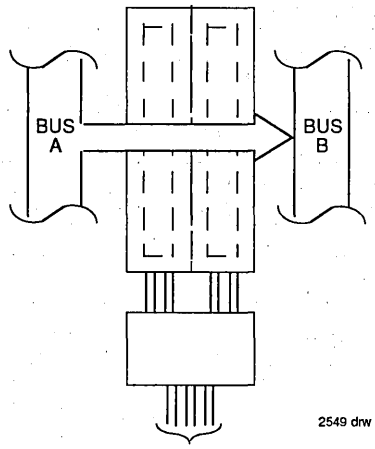


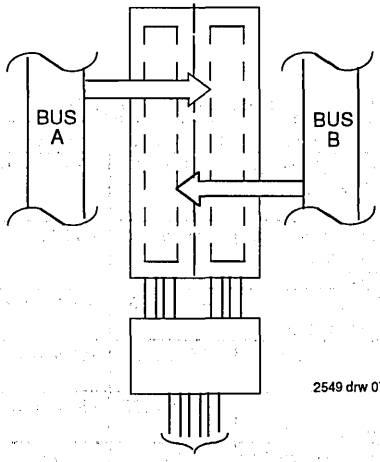
xOEAB	$\overline{\text{xOEBA}}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO A



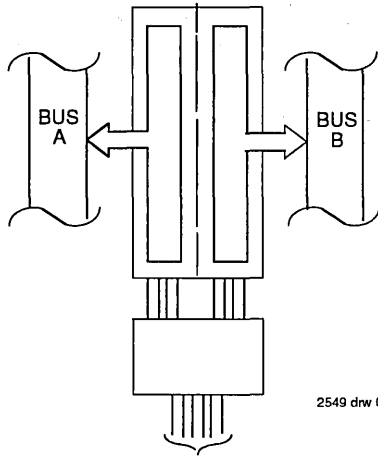
xOEAB	$\overline{\text{xOEBA}}$	xCLKAB	xCLKBA	xSAB	xSBA
H	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO B



xOEAB	$\overline{\text{xOEBA}}$	xCLKAB	xCLKBA	xSAB	xSBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM A AND/OR B



xOEAB	$\overline{\text{xOEBA}}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA TO A AND/OR B

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	±5	µA
	Input HIGH Current (I/O pins)			—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)			—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = 0.5V	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	-140	-200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	-180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

2549 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16652T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±100	µA

2549 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162652T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2549 lnk 09

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open xOEAB = $x\overline{OEBA}$=GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	2.7	mA
		xOEAB = $x\overline{OEBA}$=GND One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	1.3	4.2	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	7.5[5]	
		xOEAB = $x\overline{OEBA}$=GND Sixteen Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	8.3	21[5]	

2549 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16652T/162652T				FCT16652AT/162652AT				FCT16652CT/162652CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	1.5	5.4	1.5	6.0	ns
t_{PZH} t_{PZL}	Output Enable Time xOEAB or x$\overline{OEBA}$ to Bus		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	1.5	7.8	1.5	8.9	ns
t_{PHZ} t_{PLZ}	Output Disable Time xOEAB or x$\overline{OEBA}$ to Bus		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	1.5	6.3	1.5	7.7	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	1.5	5.7	1.5	6.3	ns
t_{PLH} t_{PHL}	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	1.5	6.2	1.5	7.0	ns
t_{SU}	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	Clock Pulse Width HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

2549 tbl 09

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

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Integrated Device Technology, Inc.

FAST CMOS 16-BIT REGISTERED TRANSCEIVER

IDT54/74FCT16952AT/BT/CT/DT
IDT54/74FCT162952AT/BT/CT/DT

FEATURES:

- **Common features:**
  - 0.5 MICRON CEMOS™ Technology
  - **High-speed, low-power CEMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
  - Speed grades same as FCT-T Octals
- **Features for FCT16952AT/BT/CT/DT:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162952AT/BT/CT/DT:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

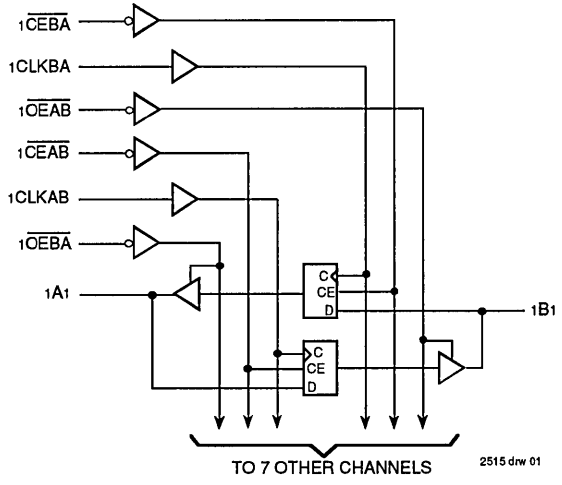
DESCRIPTION:

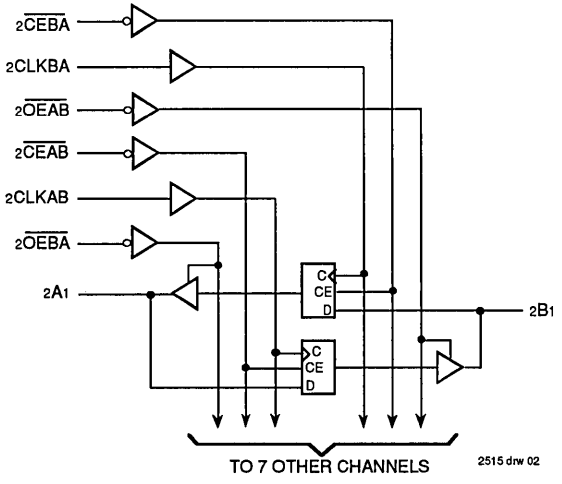
The IDT54/74FCT16952AT/BT/CT/DT and IDT54/74FCT162952AT/BT/CT/DT 16-bit registered transceivers are built using advanced CEMOS, dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type registered transceivers with separate input and output control for each set to permit independent control of data flow in either direction. For example, the A-to-B Enable ($xCEAB$) must be LOW in order to enter data from the A port. xCLKAB controls the clocking function. When xCLKAB toggles from LOW-to-HIGH, the data present on the A port will be clocked into the register. $xOEAB$ performs the output enable function on the B port. Data flow from B port to A port is similar but requires using $xCEBA$, xCLKBA, and $xOEBA$ inputs. The flow-through organization of signal pins facilitates ease of layout. Full 16-bit operation can be achieved by tying the control pins of the independent transceivers together. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT16952AT/BT/CT/DT are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with Power-Off Disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162952AT/BT/CT/DT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162952AT/BT/CT/DT are plug-in replacements for the IDT54/74FCT16952AT/BT/CT/DT and 54/74ABT16952 for on-board bus interface applications.

FUNCTIONAL BLOCK DIAGRAM





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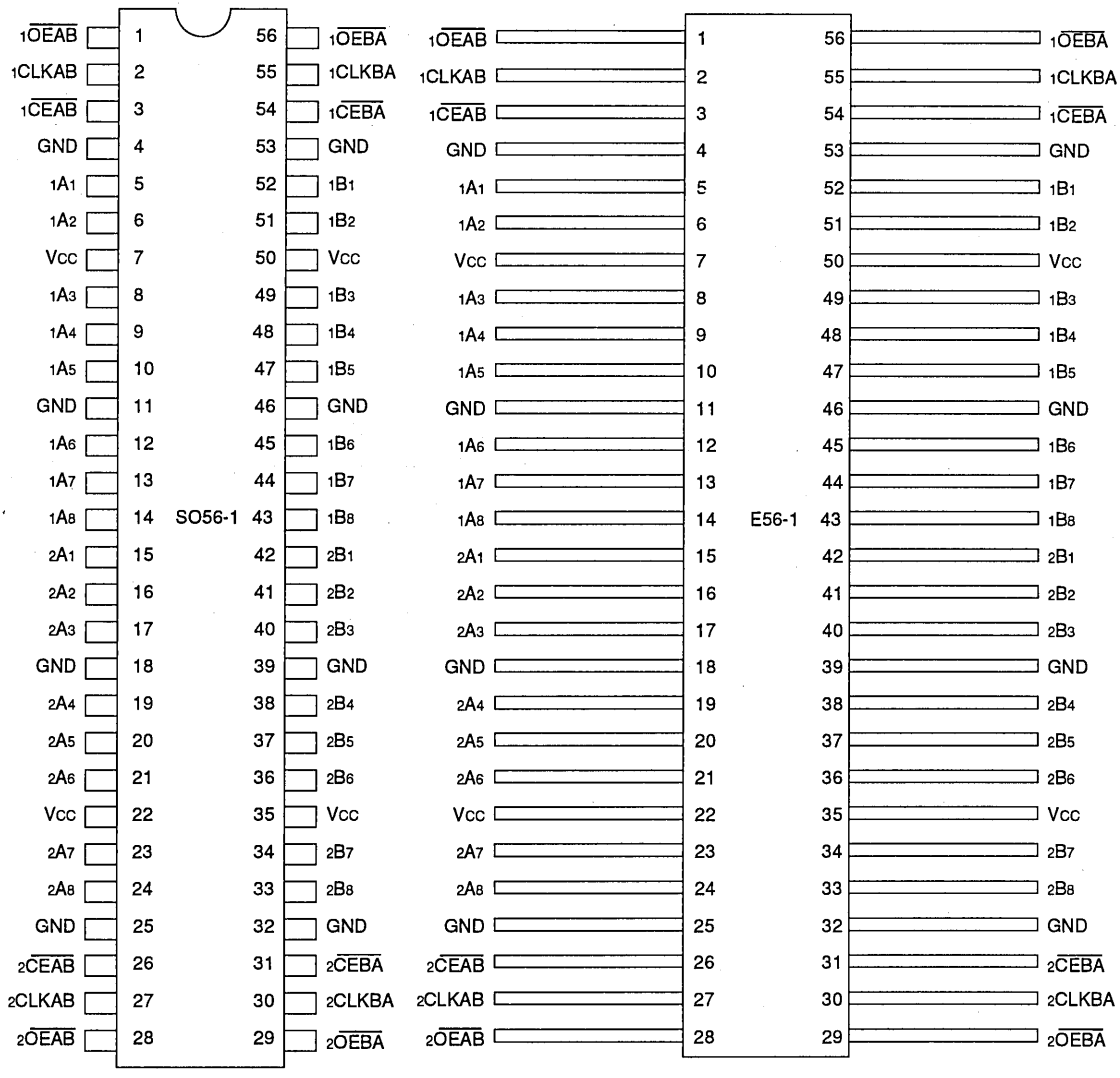
PIN CONFIGURATIONS



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PIN DESCRIPTION

Pin Names	Description
$x\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$x\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$x\overline{CEAB}$	A-to-B Clock Enable Input (Active LOW)
$x\overline{CEBA}$	B-to-A Clock Enable Input (Active LOW)
xCLKAB	A-to-B Clock Input
xCLKBA	B-to-A Clock Input
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs

2515 tbl 01

FUNCTION TABLE[1,3]

Inputs				Outputs
$x\overline{CEAB}$	xCLKAB	$x\overline{OEAB}$	xAx	xBx
H	X	L	X	B[2]
X	L	L	X	B[2]
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

NOTES: 2515 tbl 02

1. A-to-B data flow is shown: B-to-A data flow is similar but uses, $x\overline{CEBA}$, xCLKBA, and $x\overline{OEBA}$.
2. Level of B before the indicated steady-state input conditions were established.
3. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2515 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2515 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	±5	µA
	Input HIGH Current (I/O pins)			—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)			—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = 0.5V	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

2515 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16952T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±100	µA

2515 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162952T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2613 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $x\overline{OEAB}$ or $x\overline{OEBA}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz (xCLKAB) 50% Duty Cycle $x\overline{OEAB}$ = $x\overline{CEAB}$ = GND $x\overline{OEBA}$ = V_{CC} One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	2.7	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.3	4.2	
		V_{CC} = Max., Outputs Open f_{CP}= 10MHz (xCLKAB) 50% Duty Cycle $x\overline{OEAB}$ = $x\overline{CEAB}$ = GND $x\overline{OEBA}$ = V_{CC} Sixteen Bits Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	7.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	8.3	21[5]	

2515 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16952AT/162952AT				FCT16952BT/162952BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay xCLKAB, xCLKBA to xBx, xAx	CL = 50pF RL = 500Ω	2.0	10.0	2.0	11.0	2.0	7.5	2.0	8.0	ns
tPZH tPZL	Output Enable Time $x\overline{OEBA}$, $x\overline{OEAB}$ to xAx, xBx		1.5	10.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
tPHZ tPLZ	Output Disable Time $x\overline{OEBA}$, $x\overline{OEAB}$ to xAx, xBx		1.5	10.0	1.5	10.0	1.5	7.5	1.5	8.0	ns
tSU	Set-up Time, HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.5	—	2.5	—	2.5	—	2.5	—	ns
tH	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.0	—	2.0	—	1.5	—	1.5	—	ns
tSU	Set-up Time, HIGH or LOW $x\overline{CEAB}$, $x\overline{CEBA}$ to xCLKAB, xCLKBA		3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW $x\overline{CEAB}$, $x\overline{CEBA}$ to xCLKAB, xCLKBA		2.0	—	2.0	—	2.0	—	2.0	—	ns
tW	Pulse Width HIGH or LOW xCLKAB or xCLKBA[3]		3.0	—	3.0	—	3.0	—	3.0	—	ns
tSK(o)	Output Skew[4]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2515 tbl 09

Symbol	Parameter	Condition[1]	FCT16952CT/162952CT				FCT16952DT/162952DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay xCLKAB, xCLKBA to xBx, xAx	CL = 50pF RL = 500Ω	2.0	6.3	2.0	7.3	2.0	4.5	—	—	ns
tPZH tPZL	Output Enable Time $x\overline{OEBA}$, $x\overline{OEAB}$ to xAx, xBx		1.5	7.0	1.5	8.0	1.5	5.6	—	—	ns
tPHZ tPLZ	Output Disable Time $x\overline{OEBA}$, $x\overline{OEAB}$ to xAx, xBx		1.5	6.5	1.5	7.5	1.5	4.3	—	—	ns
tSU	Set-up Time, HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.5	—	2.5	—	1.5	—	—	—	ns
tH	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		1.5	—	1.5	—	1.0	—	—	—	ns
tSU	Set-up Time, HIGH or LOW $x\overline{CEAB}$, $x\overline{CEBA}$ to xCLKAB, xCLKBA		3.0	—	3.0	—	2.0	—	—	—	ns
tH	Hold Time HIGH or LOW $x\overline{CEAB}$, $x\overline{CEBA}$ to xCLKAB, xCLKBA		2.0	—	2.0	—	1.0	—	—	—	ns
tW	Pulse Width HIGH or LOW xCLKAB or xCLKBA[3]		3.0	—	3.0	—	3.0	—	—	—	ns
tSK(o)	Output Skew[4]		—	0.5	—	0.5	—	0.5	—	—	ns

2515 tbl 10

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

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Integrated Device Technology, Inc.

FAST CMOS 18-BIT REGISTER

IDT54/74FCT16823AT/BT/CT
IDT54/74FCT162823AT/BT/CT

FEATURES:

- **Common features:**
  - 0.5 MICRON CEMOS™ Technology
  - **High-speed, low-power CEMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
  - Speed grades same as FCT-T 9-bit functions
- **Features for FCT16823AT/BT/CT:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162823AT/BT/CT:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

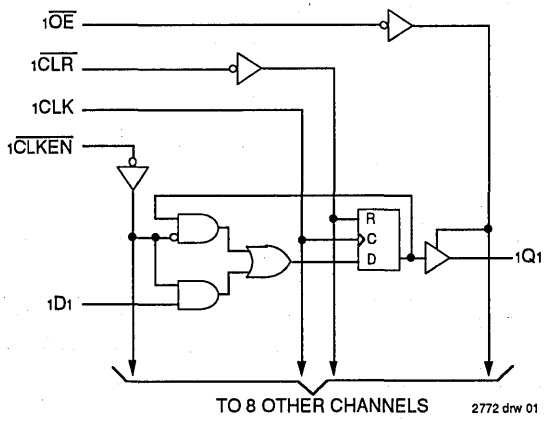
DESCRIPTION:

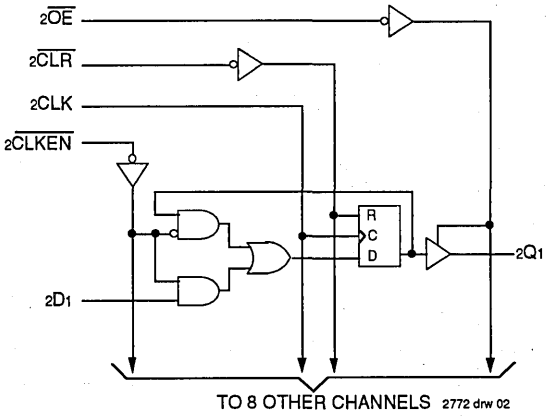
The IDT54/74FCT16823AT/BT/CT and IDT54/74FCT162823AT/BT/CT 18-bit bus interface registers are built using advanced CEMOS, dual metal CMOS technology. These high-speed, low-power registers with clock enable (x$\overline{CLKEN}$) and clear (x$\overline{CLR}$) controls are ideal for parity bus interfacing in high-performance synchronous systems. The control inputs are organized to operate the device as two 9-bit registers or one 18-bit register. Flow-through organization of signal pins facilitates ease of layout. All inputs are designed with hysteresis for improved noise margin.

The IDT54/74FCT16823AT/BT/CT are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with Power-Off Disable capability to allow "live insertion" of boards when used as backplane drivers.

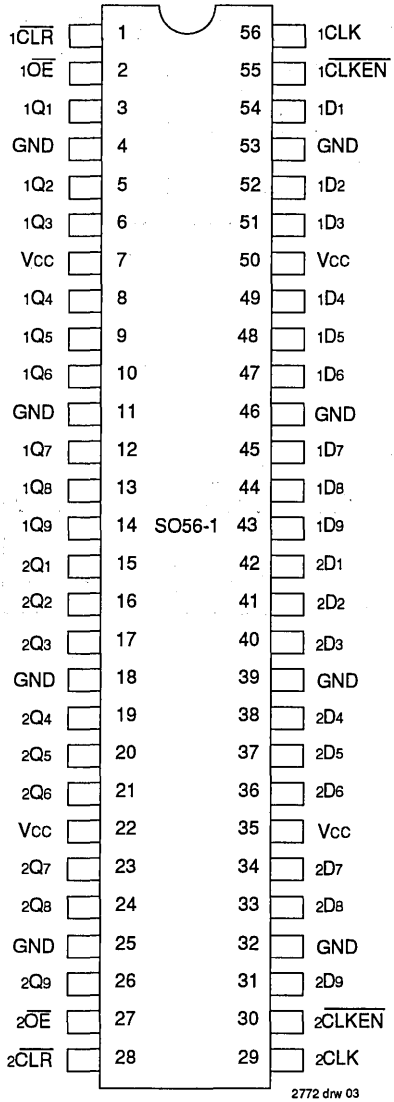
The IDT54/74FCT162823AT/BT/CT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162823AT/BT/CT are plug-in replacements for the IDT54/74FCT16823AT/BT/CT and 54/74ABT16823 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM



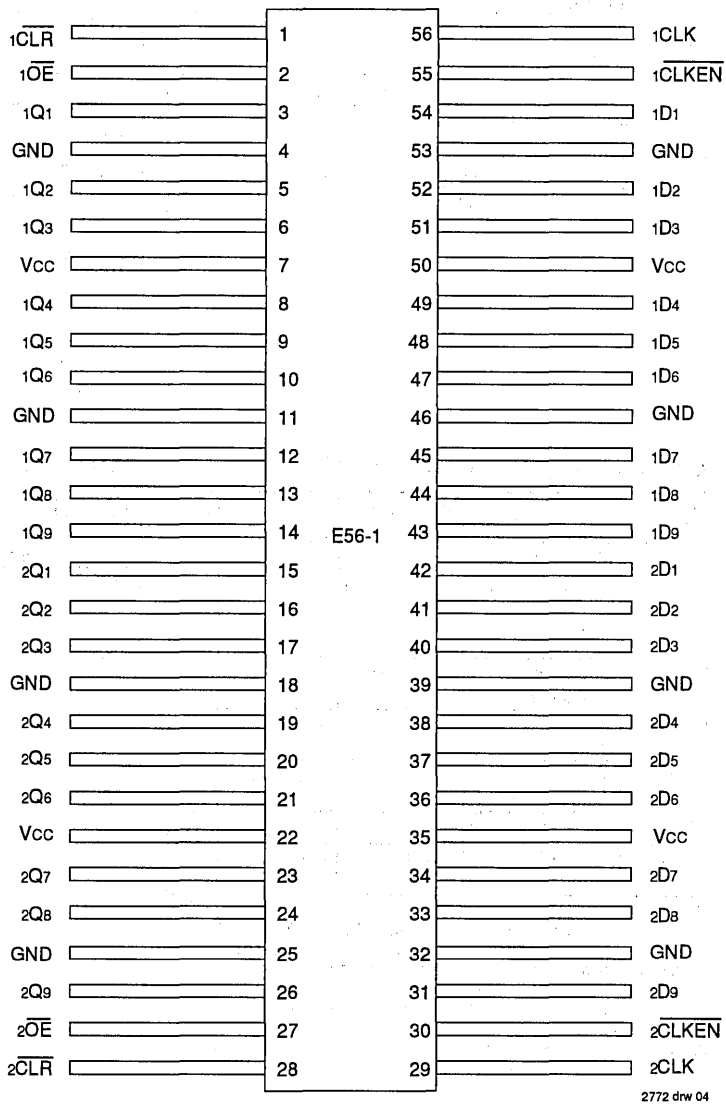


PIN CONFIGURATIONS



2772 drw 03

SSOP
TOP VIEW



2772 drw 04

CERPACK
TOP VIEW

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PIN DESCRIPTION

Pin Names	Description
xDx	Data inputs
xCLK	Clock Inputs
$x\overline{CLKEN}$	Clock Enable Inputs (Active LOW)
$x\overline{CLR}$	Asynchronous clear Inputs (Active LOW)
$x\overline{OE}$	Output Enable Inputs (Active LOW)
xQx	3-State Outputs

2772 tbl 01

FUNCTION TABLE[1]

Inputs					Outputs	
$x\overline{OE}$	$x\overline{CLR}$	$x\overline{CLKEN}$	xCLK	xDx	xQx	Function
H	X	X	X	X	Z	High Z
L	L	X	X	X	L	Clear
L	H	H	X	X	Q[2]	Hold
H	H	L	↑	L	Z	Load
H	H	L	↑	H	Z	
L	H	L	↑	L	L	
L	H	L	↑	H	H	

NOTES:
2772 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
2. Output level before indicated steady-state input conditions were established.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES:
2772 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE:
2772 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	±5	µA
	Input HIGH Current (I/O pins)			—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)			—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = 0.5V	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	-140	-200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

2772 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16823T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±100	µA

2772 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162823T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2772 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.

5

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = $x\overline{CLKEN}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	0.8	2.7	mA
		$x\overline{OE}$ = $x\overline{CLKEN}$ = GND at f_i = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	1.3	4.2	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	4.2	8.1[5]	
		$x\overline{OE}$ = $x\overline{CLKEN}$ = GND at f_i = 2.5MHz 50% Duty Cycle Eighteen Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	9.2	23.1[5]	

2772 tbl 08

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions[1]	FCT16823AT/162823AT				FCT16823BT/162823BT				FCT16823CT/162823CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay xCLK to xQx	CL = 50pF RL = 500Ω	1.5	10.0	1.5	11.5	1.5	7.5	1.5	8.5	1.5	6.0	1.5	7.0	ns
		CL = 300pF[3] RL = 500Ω	1.5	20.0	1.5	20.0	1.5	15.0	1.5	16.0	1.5	12.5	1.5	13.5	
tPHL	Propagation Delay $xCLR$ to xQx	CL = 50pF RL = 500Ω	1.5	14.0	1.5	15.0	1.5	9.0	1.5	9.5	1.5	8.0	1.5	8.5	ns
tPZH tPZL	Output Enable Time xOE to xQx	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	1.5	7.0	1.5	8.0	ns
		CL = 300pF[3] RL = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	1.5	12.5	1.5	13.5	
tPHZ tPLZ	Output Disable Time xOE to xQx	CL = 5pF[3] RL = 500Ω	1.5	7.0	1.5	8.0	1.5	6.5	1.5	7.0	1.5	6.2	1.5	6.2	ns
		CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	7.5	1.5	8.0	1.5	6.5	1.5	6.5	
tSU	Set-up Time HIGH or LOW xDx to xCLK	CL = 50pF RL = 500Ω	4.0	—	4.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW xDx to xCLK		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tSU	Set-up Time HIGH or LOW $xCLKEN$ to xCLK		4.0	—	4.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW $xCLKEN$ to xCLK		2.0	—	2.0	—	0	—	0	—	0	—	0	—	ns
tW	xCLK Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tW	$xCLR$ Pulse Width LOW		6.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tREM	Recovery Time $xCLR$ to xCLK		6.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tSK(o)	Output Skew[4]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

NOTES:
2772 tbl 09

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These conditions are guaranteed but not tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

5

Integrated Device Technology, Inc.

FAST CMOS 20-BIT BUFFERS

IDT54/74FCT16827AT/BT/CT
IDT54/74FCT162827AT/BT/CT

FEATURES:

- **Common features:**
  - 0.5 MICRON CEMOS™ Technology
  - **High-speed, low-power CEMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
  - Speed grades same as FCT-T 10-bit functions
- **Features for FCT16827AT/BT/CT:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162827AT/BT/CT:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

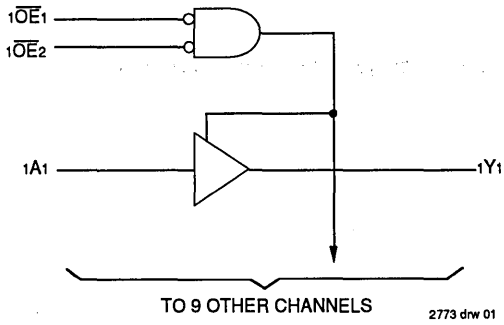
DESCRIPTION:

The IDT54/74FCT16827AT/BT/CT and IDT54/74FCT162827AT/BT/CT 20-bit buffers are built using advanced CEMOS, dual metal CMOS technology. These 20-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or busses carrying parity. Two pair of nand-ed output enable controls offer maximum control flexibility and are organized to operate the device as two 10-bit buffers or one 20-bit buffer. Flow-through organization of signal pins facilitates ease of layout. All inputs are designed with hysteresis for improved noise margin.

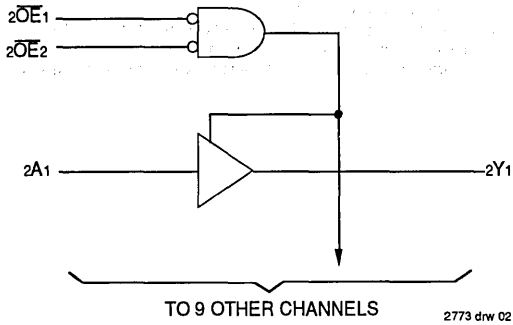
The IDT54/74FCT16827AT/BT/CT are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with Power-Off Disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162827AT/BT/CT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162827AT/BT/CT are plug-in replacements for the IDT54/74FCT16827AT/BT/CT and 54/74ABT16827 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM



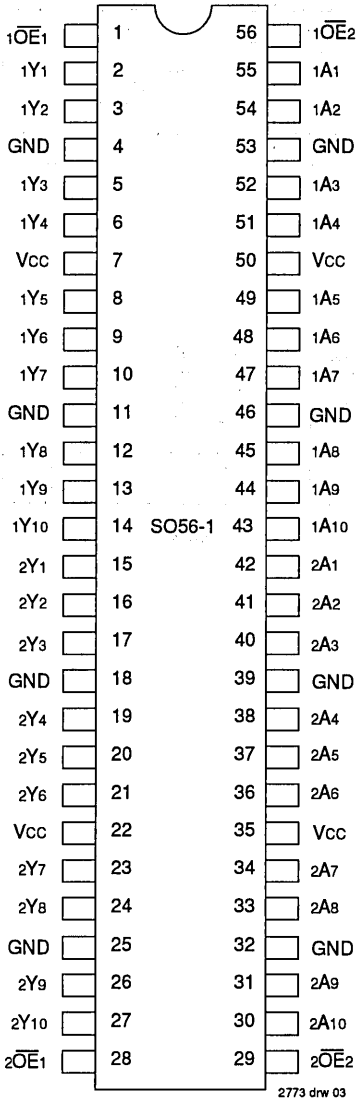
2773 drw 01



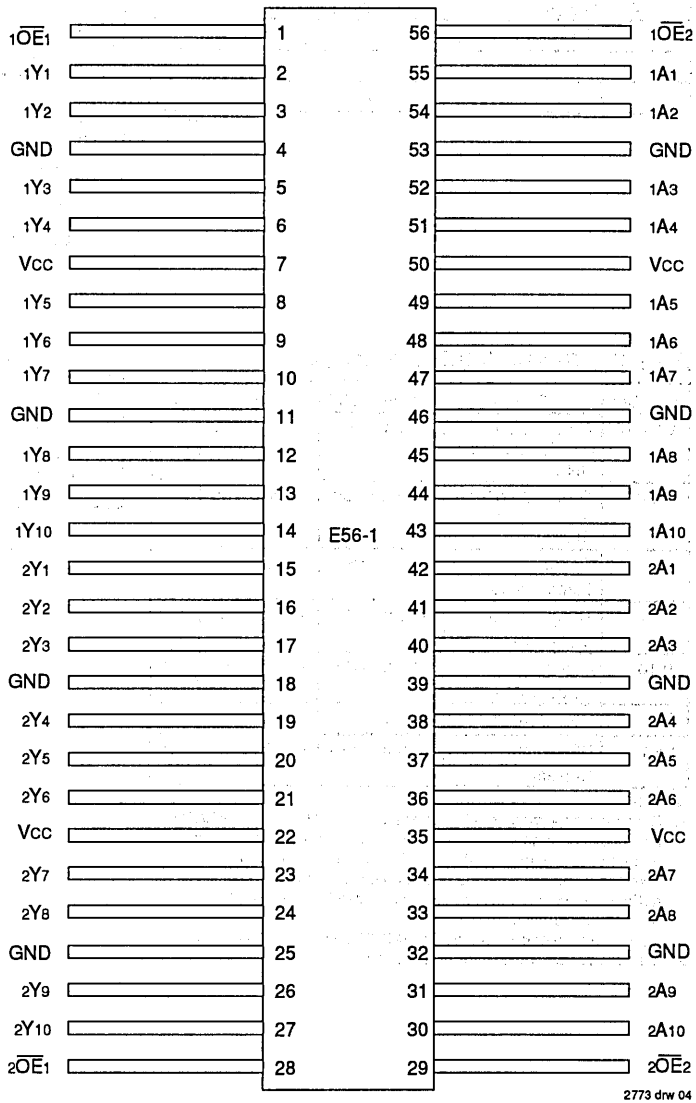
2773 drw 02

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



SSOP
TOP VIEW



CERPACK
TOP VIEW

5

PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}x$	Output Enable Inputs (Active LOW)
xAx	Data Inputs
xYx	3-State Outputs

2773 tbl 01

FUNCTION TABLE[1]

Inputs			Outputs
$x\overline{OE}_1$	$x\overline{OE}_2$	xAx	xYx
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

2773 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2773 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

2773 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	±5	µA
	Input HIGH Current (I/O pins)			—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)			—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = 0.5V	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	-0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

2773 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16827T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±100	µA

2773 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162827T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2773 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}_1$ = $x\overline{OE}_2$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	0.7	2.5	mA
		50% Duty Cycle $x\overline{OE}_1$ = $x\overline{OE}_2$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	0.9	3.3	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND	—	3.1	6.5[5]	
		50% Duty Cycle $x\overline{OE}_1$ = $x\overline{OE}_2$ = GND Twenty Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	8.1	21.5[5]	

2773 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT16827AT/162827AT				FCT16827BT/162827BT				FCT16827CT/162827CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Conditions[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	9.0	1.5	5.0	1.5	6.5	1.5	4.4	1.5	5.0	ns
		C_L = 300pF[3] R_L = 500Ω	1.5	15.0	1.5	17.0	1.5	13.0	1.5	14.0	1.5	10.0	1.5	11.0	
t_{PZH} t_{PZL}	Output Enable Time $x\overline{OE}x$ to xYx	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	1.5	7.0	1.5	8.0	ns
		C_L = 300pF[3] R_L = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	1.5	14.0	1.5	15.0	
t_{PHZ} t_{PLZ}	Output Disable Time $x\overline{OE}x$ to xYx	C_L = 5pF[3] R_L = 500Ω	1.5	9.0	1.5	9.0	1.5	6.0	1.5	7.0	1.5	5.7	1.5	6.7	ns
		C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	10.0	1.5	7.0	1.5	8.0	1.5	6.0	1.5	7.0	
$t_{SK(o)}$	Output Skew[4]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

2773 tbl 09

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These conditions are guaranteed but not tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

5

Integrated Device Technology, Inc.

FAST CMOS 20-BIT TRANSPARENT LATCHES

IDT54/74FCT16841AT/BT/CT
IDT54/74FCT162841AT/BT/CT

FEATURES:

- **Common features:**
  - 0.5 MICRON CEMOS™ Technology
  - **High-speed, low-power CEMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
  - Speed grades same as FCT-T 10-bit functions
- **Features for FCT16841AT/BT/CT:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162841AT/BT/CT:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

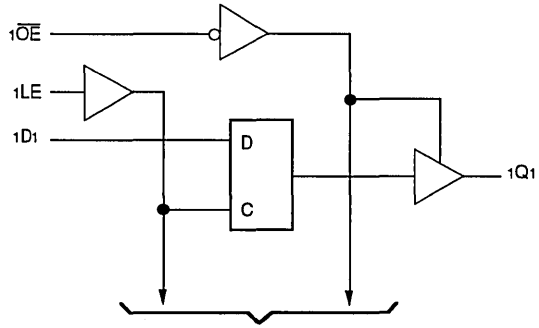
DESCRIPTION:

The IDT54/74FCT16841AT/BT/CT and IDT54/74FCT162841AT/BT/CT 20-bit transparent D-type latches are built using advanced CEMOS, dual metal CMOS technology. These high-speed, low-power latches are ideal for temporary storage of data. They can be used for implementing memory address latches, I/O ports, and bus drivers. The Output Enable and Latch Enable controls are organized to operate each device as two 10-bit latches or one 20-bit latch. Flow-through organization of signal pins facilitates ease of layout. All inputs are designed with hysteresis for improved noise margin.

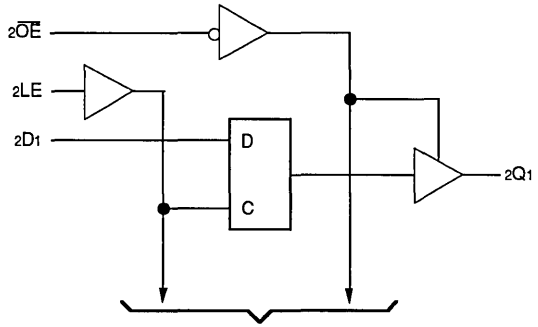
The IDT54/74FCT16841AT/BT/CT are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with Power-Off Disable capability to allow "live insertion" of boards when used as backplane drivers.

The IDT54/74FCT162841AT/BT/CT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The IDT54/74FCT162841AT/BT/CT are plug-in replacements for the IDT54/74FCT16841AT/BT/CT and 54/74ABT16841 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM



2556 drw 01



2556 drw 02

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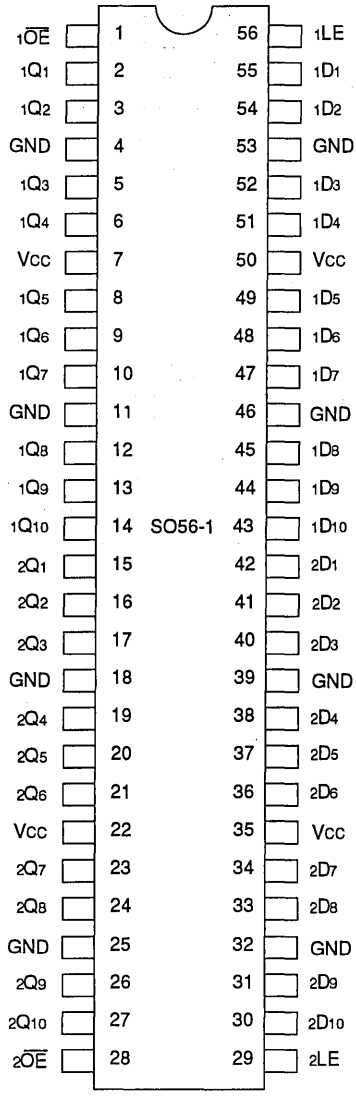
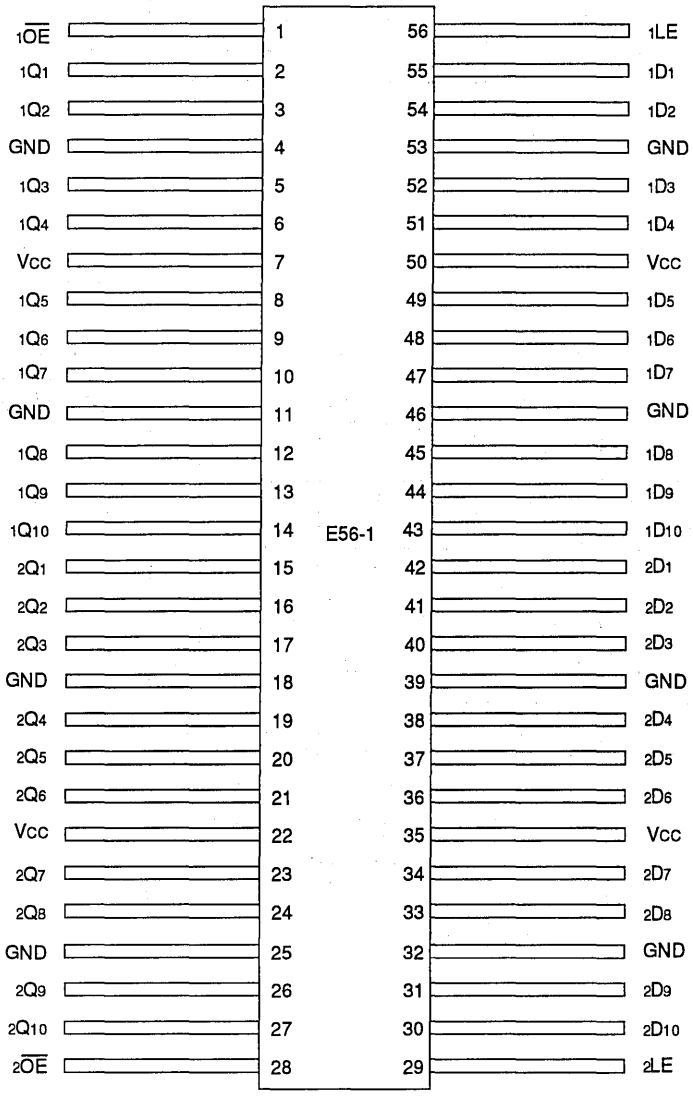
PIN CONFIGURATIONS



2556 drw 03

SSOP
TOP VIEW



2556 drw 04

CERPACK
TOP VIEW

5

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xLE	Latch Enable Input (Active HIGH)
$x\overline{OE}$	Output Enable Input (Active LOW)
xQx	3-State Outputs

2556 tbl 01

FUNCTION TABLE[1]

Inputs			Outputs
xDx	xLE	$x\overline{OE}$	xQx
H	H	L	H
L	H	L	L
X	L	L	Q[2]
X	X	H	Z

NOTES:
2556 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
2. Output level before xLE HIGH-to-LOW Transition.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES:
2556 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE:
2556 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	±5	µA
	Input HIGH Current (I/O pins)			—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)			—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = 0.5V	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	-140	-200	mA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	-180	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

2556 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16841T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±100	µA

2556 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162841T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2556 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi =10MHz 50% Duty Cycle $x\overline{OE}$ = GND xLE = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND V_{IN} = 3.4V V_{IN} = GND	— —	0.7 0.9	2.5 3.3	mA
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = GND xLE = V_{CC} Twenty Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND V_{IN} = 3.4V V_{IN} = GND	— —	3.1 8.1	6.5[5] 21.5[5]	

2556 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT16841AT/162841AT				FCT16841BT/162841BT				FCT16841CT/162841CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay xDx to xQx (LE = HIGH)	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	10.0	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	
t_{PLH} t_{PHL}	Propagation Delay xLE to xQx	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	10.5	1.5	6.4	1.5	6.8	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	16.0	1.5	20.0	1.5	15.5	1.5	18.0	1.5	15.0	1.5	16.0	
t_{PZH} t_{PZL}	Output Enable Time $x\overline{OE}$ to xQx	C_L = 50pF R_L = 500Ω	1.5	11.5	1.5	13.0	1.5	8.0	1.5	8.5	1.5	6.5	1.5	7.3	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	23.0	1.5	25.0	1.5	14.0	1.5	15.0	1.5	12.0	1.5	13.0	
t_{PHZ} t_{PLZ}	Output Disable Time $x\overline{OE}$ to xQx	C_L = 5pF[4] R_L = 500Ω	1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	1.5	5.7	1.5	6.0	ns
		C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	10.0	1.5	7.0	1.5	7.5	1.5	6.0	1.5	6.3	
t_{SU}	Set-Up Time HIGH or LOW, xDx to xLE	C_L = 50pF R_L = 500Ω	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
t_H	Hold Time HIGH or LOW, xDx to xLE		2.5	—	3.0	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
t_W	xLE Pulse Width HIGH[3]		4.0	—	5.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
$t_{SK(o)}$	Output skew[5]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.
4. These conditions are guaranteed but not tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

2556 tbl 09

5

STANDARD 5V LOGIC PRODUCTS

The demand for high-performance systems continues to push the need for fast clock frequencies that exceed the capabilities of most ASICs and older-generation logic families such as FAST™ and FACT™. The use of high-speed MSI logic building blocks in the "speed-critical" processor memory interface has allowed designers to produce the highest performance 25/33/40/50 MHz microprocessor-based systems. The use of MSI logic, with its fast speeds and low switching noise characteristics, as realized by IDT's 16-, 20-, and 24-pin FCT and FCT-T devices, has become all-pervasive in today's high-performance systems.

The FCT and Low-Noise FCT-T Logic Families

The popular FCT and FCT-T families were designed specifically for high-performance systems. These high-speed, very low-power (1mW typ.) functions have now become the industry standard for high-speed designs. The FCT-T family, with output edge rate control and input hysteresis circuitry, has 40% less ground bounce that the FCT family, eliminating the high noise once associated with high-speed CMOS logic circuits. Both the FCT and the FCT-T families are offered in several speed grades:

- FCT/FCT-T is a direct low-power replacement of FAST™ and AM29800 products.
- FCT-A products are up to 25% faster than FCT, with standard switching noise.
- FCT-AT products are equivalent to FCT-A, with low switching noise.
- FCT-C products are up to 50% faster than FCT, with standard switching noise.
- FCT-CT products are equivalent to FCT-C, with low switching noise.
- FCT-DT products are up to 60% faster than FCT, with low switching noise.

The FBT Logic Family

Several memory driver functions have been designed using IDT's advanced dual metal BiCEMOS™ process. This technology provides high-speed devices, while minimizing simultaneous switching noise and maintaining CMOS power levels. These functions include a 25Ω series resistor on the output driver that acts as a series terminator. This results in a greater ability to drive transmission lines with high-capacitance loads such as large banks of memory. The FBT family comes in two speed grades, FBT and FBT-A.

- FBT series is equivalent to BCT speeds with ultra-low switching noise
- FBT-A series is up to 30% faster than BCT speeds, with low switching noise
- CMOS power levels (1mW typical static)
- TTL-compatible input and output levels.
- High-impedance power-off state
- 25Ω series resistor outputs
- JEDEC standard pinouts

TABLE OF CONTENTS

STANDARD 5V LOGIC PRODUCTS (CONTINUED)

STANDARD 5V LOGIC MODULES (Please refer to the 1992 Specialized Memories and Modules Data Book)

6

Integrated Device Technology, Inc.

FAST CMOS OCTAL REGISTERED TRANSCEIVERS

IDT29FCT52AT/BT/CT/DT
IDT29FCT53AT/BT/CT

FEATURES:

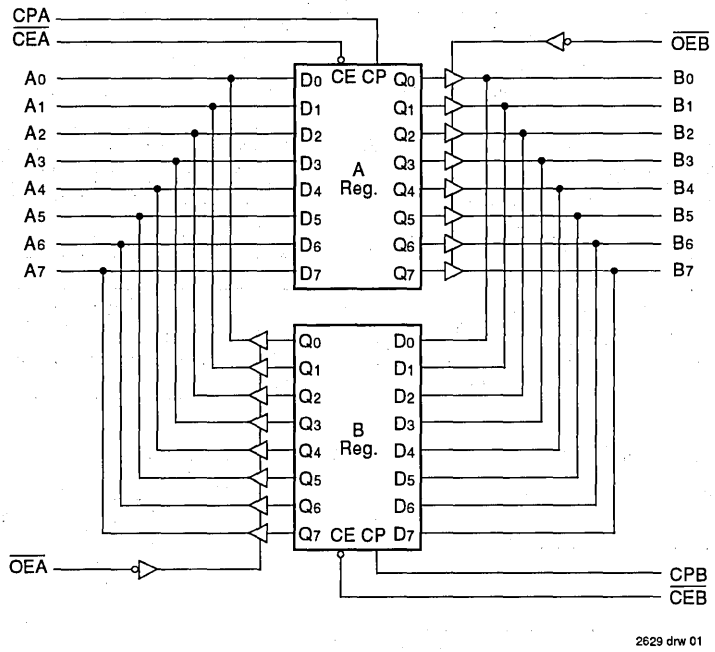
- Fastest CMOS logic family available
- A, B, C and D speed grades with 4.5ns t_{PD}
- Available in DIP, SOIC, SSOP, CERPACK and LCC packages
- Power-off disable feature allows "hot-insertion"
- CMOS power levels (2.5mW typ. static)
- TTL input and output level compatible
- I_{OFF} feature ideal for hot switching of backplane drivers
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT29FCT52AT/BT/CT/DT and IDT29FCT53AT/BT/CT are 8-bit registered transceivers manufactured using advanced CEMOS™, a dual metal CMOS technology. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-state output enable signals are provided for each register. Both A outputs and B outputs are guaranteed to sink 64mA.

The IDT29FCT52AT/BT/CT/DT is a non-inverting option of the IDT29FCT53AT/BT/CT.

FUNCTIONAL BLOCK DIAGRAM[1]

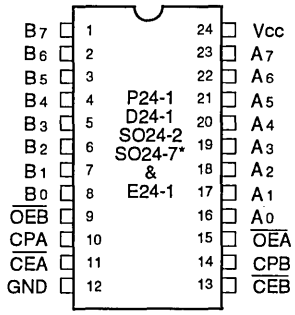


2629 drw 01

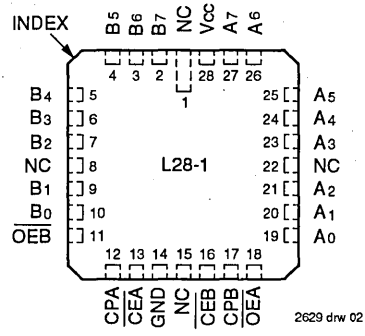
NOTE:
1. IDT29FCT52T function is shown. IDT29FCT53T is the inverting option.

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/SSOP/CERPACK
TOP VIEW



LCC
TOP VIEW

* For 29FCT52AT/BT/CT only

PIN DESCRIPTION

Name	I/O	Description
A0-7	I/O	Eight bidirectional lines carrying the A Register inputs or B Register outputs.
B0-7	I/O	Eight bidirectional lines carrying the B Register inputs or A Register outputs.
CPA	I	Clock for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal.
$\overline{CEA}$	I	Clock Enable for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal. When $\overline{CEA}$ is HIGH, the A Register holds its contents, regardless of CPA signal transitions.
$\overline{OEB}$	I	Output Enable for the A Register. When $\overline{OEB}$ is LOW, the A Register outputs are enabled onto the B0-7 lines. When $\overline{OEB}$ is HIGH, the B0-7 outputs are in the high-impedance state.
CPB	I	Clock for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal.
$\overline{CEB}$	I	Clock Enable for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal. When $\overline{CEB}$ is HIGH, the B Register holds its contents, regardless of CPB signal transitions.
$\overline{OEA}$	I	Output Enable for the B Register. When $\overline{OEA}$ is LOW, the B Register outputs are enabled onto the A0-7 lines. When $\overline{OEA}$ is HIGH, the A0-7 outputs are in the high-impedance state.

2629 tbl 05

REGISTER FUNCTION TABLE[1]
(Applies to A or B Register)

Inputs			Internal	
D	CP	$\overline{CE}$	Q	Function
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

2629 tbl 06

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   NC = No Change
   ↑ = LOW-to-HIGH Transition

OUTPUT CONTROL[1]

	Internal	Y-Outputs		
$\overline{OE}$	Q	52	53	Function
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

2629 tbl 07

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2529 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed +0.5V unless otherwise noted.
2. Inputs and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2640 tbl 02

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V	Except I/O Pins	—	—	5	µA
			I/O Pins	—	—	15	
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V	Except I/O Pins	—	—	–5	µA
			I/O Pins	—	—	–15	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	–225	mA
I_{OFF}	Power Down Disable	V_{CC} = GND, V_O = 4.5V		—	—	100	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH}= –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL.(4) I_{OL} = 64mA COM'L.	—	0.3	0.55	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.5	1.5	mA

NOTES: 2629 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously.Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE_A}$ or $\overline{OE_B}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE_A}$ or $\overline{OE_B}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	2.0	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.5	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE_A}$ or $\overline{OE_B}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.3	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.5	16.8[5]	

2629 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the ICC formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at DH
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	29FCT52AT/53AT				29FCT52BT/53BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB to An, Bn	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	11.0	2.0	7.5	2.0	8.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to An, Bn		1.5	10.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to An, Bn		1.5	10.0	1.5	10.0	1.5	7.5	1.5	8.0	ns
t_{SU}	Set-up Time, HIGH or LOW An, Bn to CPA, CPB		2.5	—	2.5	—	2.5	—	2.5	—	ns
t_H	Hold Time, HIGH or LOW An, Bn to CPA, CPB		2.0	—	2.0	—	1.5	—	1.5	—	ns
t_{SU}	Set-up Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		3.0	—	3.0	—	3.0	—	3.0	—	ns
t_H	Hold Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_W	Clock Pulse Width HIGH or LOW[3]		3.0	—	3.0	—	3.0	—	3.0	—	ns

Symbol	Parameter	Condition[1]	29FCT52CT/53CT				29FCT52DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB to An, Bn	C_L = 50pF R_L = 500Ω	2.0	6.3	2.0	7.3	2.0	4.5	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to An, Bn		1.5	7.0	1.5	8.0	1.5	5.6	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to An, Bn		1.5	6.5	1.5	7.5	1.5	4.3	—	—	ns
t_{SU}	Set-up Time, HIGH or LOW An, Bn to CPA, CPB		2.5	—	2.5	—	1.5	—	—	—	ns
t_H	Hold Time, HIGH or LOW An, Bn to CPA, CPB		1.5	—	1.5	—	1.0	—	—	—	ns
t_{SU}	Set-up Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		3.0	—	3.0	—	2.0	—	—	—	ns
t_H	Hold Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		2.0	—	2.0	—	1.0	—	—	—	ns
t_W	Clock Pulse Width HIGH or LOW[3]		3.0	—	3.0	—	3.0	—	—	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2629 tbl 08

6

Integrated Device Technology, Inc.

MULTILEVEL PIPELINE REGISTERS

IDT29FCT520AT/BT/CT/DT
IDT29FCT521AT/BT/CT/DT

FEATURES:

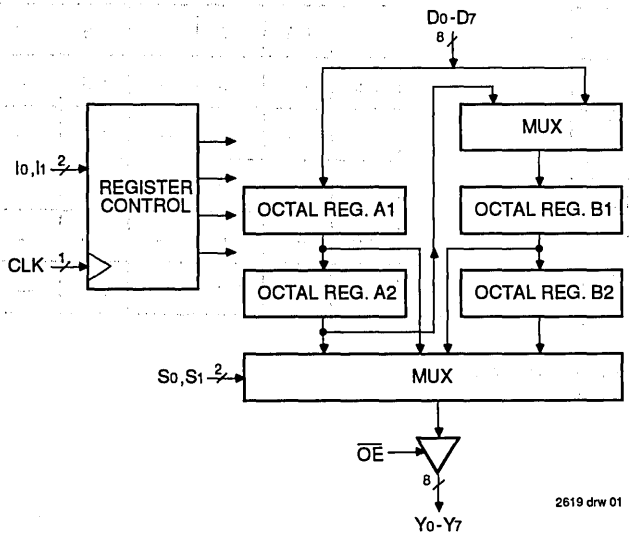
- Fastest CMOS logic family available
- A, B, C and D speed grades with 5.2ns t_{PD}
- Available in DIP, SOIC, SSOP, CERPACK and LCC packages
- Four 8-bit high-speed registers
- Dual two-level or single four-level push-only stack operation
- All registers available at multiplexed output
- Hold, transfer and load instructions
- Provides temporary address or data storage
- I_{OL} = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- Substantially lower input current levels than AMD's bipolar (5µA typ.)
- True TTL input and output levels
- Manufactured using advanced CEMOS™ processing
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT29FCT520AT/BT/CT/DT and IDT29FCT521AT/BT/CT/DT each contain four 8-bit positive edge-triggered registers. These may be operated as a dual 2-level or as a single 4-level pipeline. A single 8-bit input is provided and any of the four registers is available at the 8-bit, 3-state output.

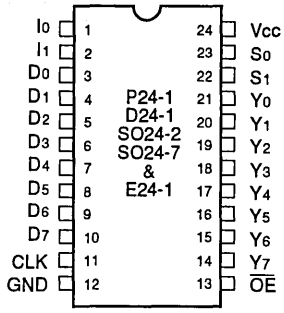
These devices differ only in the way data is loaded into and between the registers in 2-level operation. The difference is illustrated in Figure 1. In the IDT29FCT520AT/BT/CT/DT when data is entered into the first level (I = 2 or I = 1), the existing data in the first level is moved to the second level. In the IDT29FCT521AT/BT/CT/DT, these instructions simply cause the data in the first level to be overwritten. Transfer of data to the second level is achieved using the 4-level shift instruction (I = 0). This transfer also causes the first level to change. In either part I=3 is for hold.

FUNCTIONAL BLOCK DIAGRAM

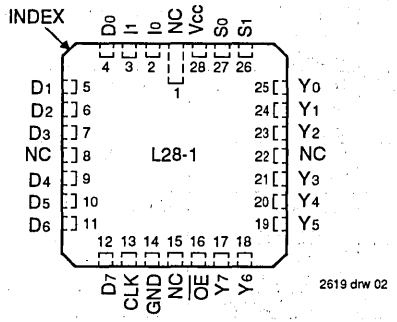


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/SOIC/SSOP/CERPACK
TOP VIEW



LCC
TOP VIEW

DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
D_n	Register input Port.
CLK	Clock input. Enter data into registers on LOW-to-HIGH transitions.
I_0, I_1	Instruction inputs. See Figure 1 and instruction Control Tables.
S_0, S_1	Multiplexer select. Inputs either register A_1, A_2, B_1 or B_2 data to be available at the output port.
$\overline{OE}$	Output enable for 3-state output port.
Y_n	Register output port.

2619 tbl 01

REGISTER SELECTION

S_1	S_0	Register
0	0	B_2
0	1	B_1
1	0	A_2
1	1	A_1

2619 tbl 02

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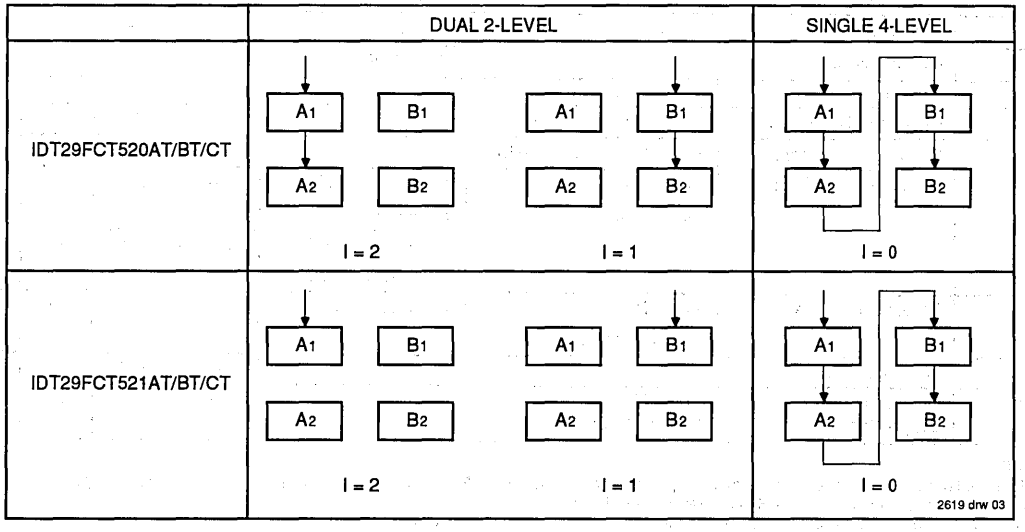

NOTE:
1. I = 3 for hold.

Figure 1. Data Loading in 2-Level Operation

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2619 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals.
3. Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2619 tbl 04

1. This parameter is measured at characterization data but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	–10	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –6mA MIL.	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA COM'L.				
			I_{OH} = –12mA MIL.	2.0	3.0	—	
			I_{OH} = –15mA COM'L.				
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 32mA MIL.	—	0.3	0.5	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA COM'L.				
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES: 2619 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current, TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	7.0	12.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	9.2	21.8[5]	

2619 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL HIgh Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT520AT/521AT				FCT520BT/521BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPHL tPLH	Propagation Delay CLK to Yn	CL = 50pF RL = 500Ω	2.0	14.0	2.0	16.0	2.0	7.5	2.0	8.0	ns
tPHL tPLH	Propagation Delay S0 or S1 to Yn		2.0	13.0	2.0	15.0	2.0	7.5	2.0	8.0	ns
tSU	Set-up Time, HIGH or LOW Dn to CLK		5.0	—	6.0	—	2.5	—	2.8	—	ns
tH	Hold Time, HIGH or LOW Dn to CLK		2.0	—	2.0	—	2.0	—	2.0	—	ns
tSU	Set-up Time, HIGH or LOW I0 or I1 to CLK		5.0	—	6.0	—	4.0	—	4.5	—	ns
tH	Hold Time, HIGH or LOW I0 or I1 to CLK		2.0	—	2.0	—	2.0	—	2.0	—	ns
tPHZ tPLZ	Output Disable Time		1.5	12.0	1.5	13.0	1.5	7.0	1.5	7.5	ns
tPZH tPZL	Output Enable Time		1.5	15.0	1.5	16.0	1.5	7.5	1.5	8.0	ns
tW	Clock Pulse Width HIGH or LOW		7.0	—	8.0	—	5.5	—	6.0	—	ns

2619 tbl 07

Symbol	Parameter	Condition[1]	FCT520CT/521CT				FCT520DT/521DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPHL tPLH	Propagation Delay CLK to Yn	CL = 50pF RL = 500Ω	2.0	6.0	2.0	7.0	2.0	5.2	—	—	ns
tPHL tPLH	Propagation Delay S0 or S1 to Yn		2.0	6.0	2.0	7.0	2.0	4.8	—	—	ns
tSU	Set-up Time, HIGH or LOW Dn to CLK		2.5	—	2.8	—	1.5	—	—	—	ns
tH	Hold Time, HIGH or LOW Dn to CLK		2.0	—	2.0	—	1.0	—	—	—	ns
tSU	Set-up Time, HIGH or LOW I0 or I1 to CLK		4.0	—	4.5	—	2.0	—	—	—	ns
tH	Hold Time, HIGH or LOW I0 or I1 to CLK		2.0	—	2.0	—	1.0	—	—	—	ns
tPHZ tPLZ	Output Disable Time		1.5	6.0	1.5	6.0	1.5	4.8	—	—	ns
tPZH tPZL	Output Enable Time		1.5	6.0	1.5	7.0	1.5	4.0	—	—	ns
tW	Clock Pulse Width HIGH or LOW[3]		5.5	—	6.0	—	3.0	—	—	—	ns

NOTES:

2619 tbl 08

1. See test circuit and waveforms.
2. Minimum units are guaranteed but not tested on Propagation Delays.

Integrated Device Technology, Inc.

FAST CMOS 1-OF-8 DECODER WITH ENABLE

IDT54/74FCT138T
IDT54/74FCT138AT
IDT54/74FCT138CT

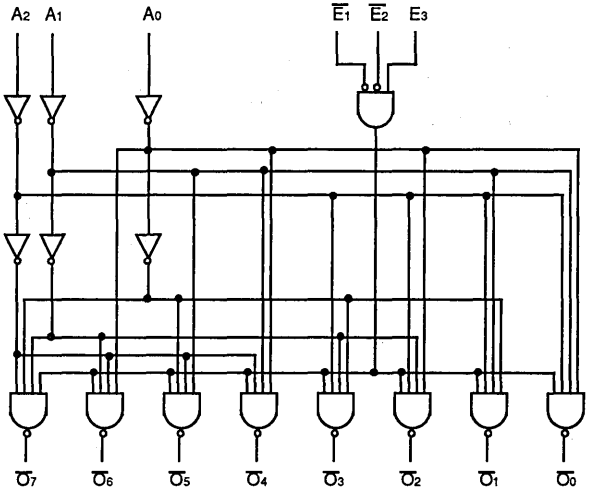
FEATURES:

- IDT54/74FCT138T equivalent to FAST™ speed
- **IDT54/74FCT138AT 35% faster than FAST**
- **IDT54/74FCT138CT 40% faster than FAST**
- Equivalent to FAST speeds and output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- True TTL input and output levels
- Substantially lower input current levels than FAST (5µA max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

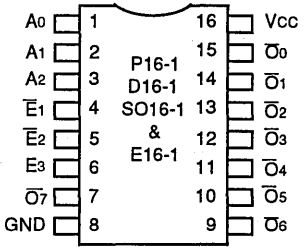
The IDT54/74FCT138T/AT/CT are 1-of-8 decoders built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT138T/AT/CT accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_7$). The IDT54/74FCT138T/AT/CT features three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four IDT54/74FCT138T/AT/CT devices and one inverter.

FUNCTIONAL BLOCK DIAGRAM



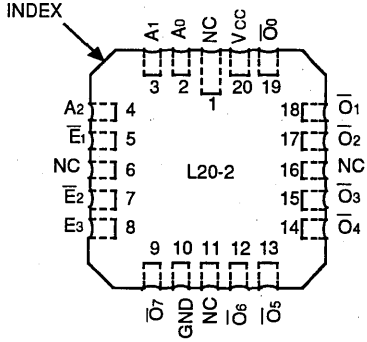
2570 cnv° 03

PIN CONFIGURATIONS



2570 drw 01

DIP/SOIC/CERPACK
TOP VIEW



2570 drw 02

LCC
TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
A_0–A_2	Address Inputs
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
$\overline{O}_0$–$\overline{O}_7$	Outputs (Active LOW)

2570 tbl 06

FUNCTION TABLE

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

2570 tbl 07

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2570 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2570 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES:

2570 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Output Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.3	mA/ MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max. Outputs Open Toggle $\overline{E_1}$, $\overline{E_2}$ or E_3	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.5	mA
		50% Duty Cycle f_O = 10MHz One Output Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.5	

NOTES:

2570 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_O N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_O = Output Frequency
   N_O = Number of Outputs at f_O
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT138T				IDT54/74FCT138AT				IDT54/74FCT138CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	12.0	1.5	5.8	1.5	7.8	1.5	5.1	1.5	6.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$		1.5	9.0	1.5	12.5	1.5	5.9	1.5	8.0	1.5	5.2	1.5	6.1	ns
t_{PLH} t_{PHL}	Propagation Delay E_3 to $\overline{O}_n$		1.5	9.0	1.5	12.5	1.5	5.9	1.5	8.0	1.5	5.2	1.5	6.1	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2570 tbl 08

Integrated Device Technology, Inc.

FAST CMOS DUAL 1-OF-4 DECODER WITH ENABLE

IDT54/74FCT139T
IDT54/74FCT139AT
IDT54/74FCT139CT

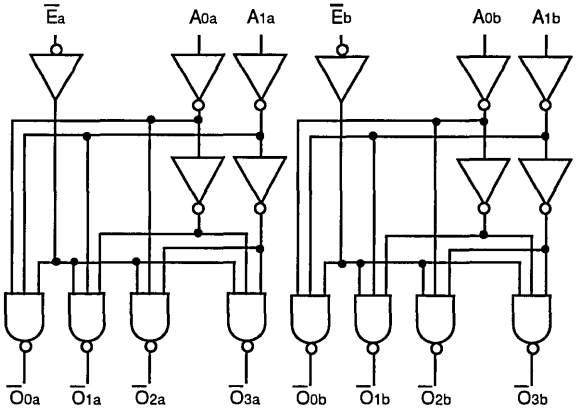
FEATURES:

- IDT54/74FCT139T equivalent to FAST™ speed
- **IDT54/74FCT139AT 35% faster than FAST**
- **IDT54/74FCT139CT 45% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- Substantially lower input current levels than FAST (5µA max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

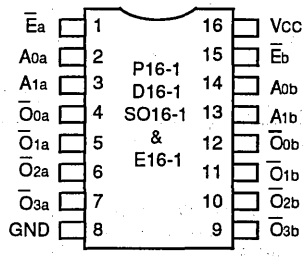
The IDT54/74FCT139T/AT/CT are dual 1-of-4 decoders built using advanced CEMOS™, a dual metal CMOS technology. These devices have two independent decoders, each of which accept two binary weighted inputs (A_0-A_1) and provide four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH, all outputs are forced HIGH.

FUNCTIONAL BLOCK DIAGRAM



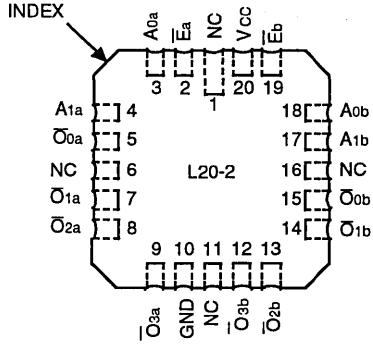
2566 cnv* 03

PIN CONFIGURATIONS



2566 cnv* 01

DIP/SOIC/CERPACK
TOP VIEW



2566 cnv* 02

LCC
TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
A_0, A_1	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
$\overline{O_0}$ - $\overline{O_3}$	Outputs (Active LOW)

2566 tbl 07

FUNCTION TABLE[1]

Inputs			Outputs			
$\overline{E}$	A_0	A_1	$\overline{O_0}$	$\overline{O_1}$	$\overline{O_2}$	$\overline{O_3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

NOTE: 2566 tbl 06

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2566 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2566 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2566 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.3	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_0 = 10MHz 50% Duty Cycle One Output Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.5	
		V_{CC} = Max. Outputs Open f_0 = 10MHz 50% Duty Cycle One Output Toggling on Each Decoder	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	7.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	3.7	9.5[5]	

NOTES:
2566 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_0 N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_0 = Output Frequency
   N_O = Number of Outputs at f_0
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FCT139T				IDT54/74FCT139AT				IDT54/74FCT139CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Parameter	Description	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay A_0 or A_1 to $\overline{O}_n$	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	12.0	1.5	5.9	1.5	7.8	1.5	5.0	1.5	6.2	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{O}_n$		1.5	8.0	1.5	9.0	1.5	5.5	1.5	7.2	1.5	4.8	1.5	5.8	ns

NOTES:
2566 tbl 08

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

Integrated Device Technology, Inc.

FAST CMOS 8-INPUT MULTIPLEXER

IDT54/74FCT151T/AT/CT
IDT54/74FCT251T/AT/CT

FEATURES:

- IDT54/74FCT151T/251T equivalent to FAST™ speed and drive
- **IDT54/74FCT151AT/251AT 25% faster than FAST**
- **IDT54/74FCT151CT/251CT 50% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- TTL input and output level compatible
  - — V_{OH} = 3.3V (typ.)
  - — V_{OL} = 0.3V (typ.)
- I_{OL} = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

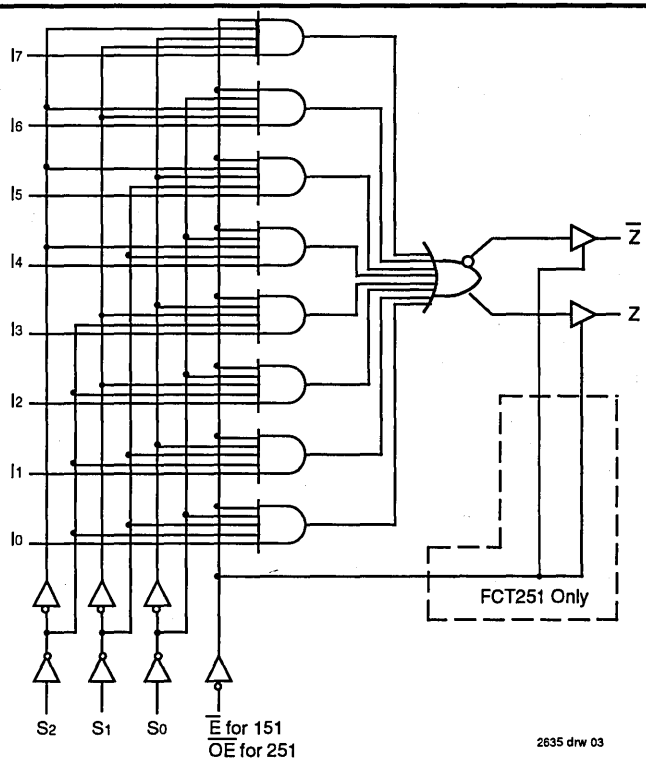
DESCRIPTION:

The IDT54/74FCT151T/AT/CT and IDT54/74FCT251T/AT/CT are high-speed 8-input multiplexers built using advanced CEMOS™, a dual metal CMOS technology. They select one bit of data from up to eight sources under the control of three select inputs. Both assertion and negation outputs are provided.

The IDT54/74FCT151T/AT/CT has a common Active-LOW enable ($\overline{E}$) input. When $\overline{E}$ is LOW, data from one of eight inputs is routed to the complementary outputs according to the 3-bit code applied to the Select (S_0-S_2) inputs. A common application of the 'FCT151 is data routing from one of eight sources.

The IDT54/74FCT251T/AT/CT has a common Active-LOW Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, data from one of eight inputs is routed to the complementary outputs. When $\overline{OE}$ is HIGH, both outputs are in the high-impedance state. This feature allows multiplexer expansion by tying several outputs together.

FUNCTIONAL BLOCK DIAGRAM



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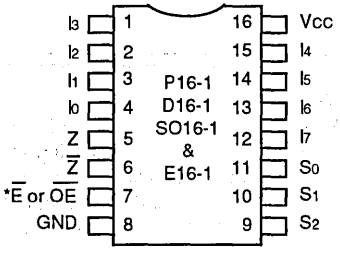
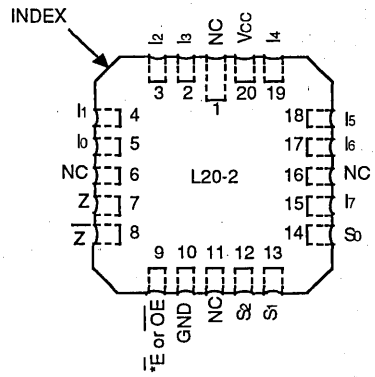
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW

2635 drw 01



2635 drw 02

LCC
TOP VIEW

*Ē for 151 only. OE for 251 only.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
VTERM(3)	Terminal Voltage with Respect to GND	–0.5 to VCC	–0.5 to VCC	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

2635 tbl 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed VCC by +0.5V unless otherwise noted.
2. Input and VCC terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

2635 tbl 04

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
I0 - I7	Data Inputs
S0 - S2	Selects Inputs
Ē	Enable Input (Active LOW)-FCT151
OE	Output Enable Input (Active LOW)-FCT251
Z	Data Output
Z̄	Inverted Data Output

2635 tbl 01

FUNCTION TABLE(2)

Inputs				Outputs	
S2	S1	S0	Ē/OE(1)	Z	Z̄
X	X	X	H	L(151)	H(151)
X	X	X	H	Z(251)	Z(251)
L	L	L	L	I0	Ī0
L	L	H	L	I1	Ī1
L	H	L	L	I2	Ī2
L	H	H	L	I3	Ī3
H	L	L	L	I4	Ī4
H	L	H	L	I5	Ī5
H	H	L	L	I6	Ī6
H	H	H	L	I7	Ī7

2635 tbl 02

NOTES:
1. Ē for 151, OE for 251.
2. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't care, Z = High Impedance.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	–10	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES:
2635 tbl 05
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	QuiescentPower Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $\overline{E}$ or $\overline{OE}$ = GND One Input Toggling	V_{IN} = V_{CC} V_{IN} = GND V_{IN} = 3.4V V_{IN} = GND	— —	3.2 3.5	6.5 7.5	mA

NOTES:
2635 tbl 06
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_O = Number of Outputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE – IDT54/74FCT151T/AT/CT

Symbol	Parameter	Condition[1]	IDT54/74FCT151T				IDT54/74FCT151AT				IDT54/74FCT151CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay SN to $\overline{Z}$	CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	6.6	1.5	7.4	1.5	5.6	1.5	6.2	ns
tPLH tPHL	Propagation Delay SN to Z		1.5	10.5	1.5	11.5	1.5	6.8	1.5	7.6	1.5	5.8	1.5	6.5	ns
tPLH tPHL	Propagation Delay $\overline{E}$ to $\overline{Z}$		1.5	7.0	1.5	7.5	1.5	5.6	1.5	6.3	1.5	4.8	1.5	5.4	ns
tPLH tPHL	Propagation Delay $\overline{E}$ to Z		1.5	9.5	1.5	11.0	1.5	5.8	1.5	6.6	1.5	5.0	1.5	5.7	ns
tPLH tPHL	Propagation Delay IN to $\overline{Z}$		1.5	6.5	1.5	7.5	1.5	5.2	1.5	5.8	1.5	4.4	1.5	4.9	ns
tPLH tPHL	Propagation Delay IN to Z		1.5	7.5	1.5	9.0	1.5	5.5	1.5	6.1	1.5	4.7	1.5	5.2	ns

2635 tbl 07

SWITCHING CHARACTERISTICS OVER OPERATING RANGE – IDT54/74FCT251T/AT/CT

Symbol	Parameter	Condition[1]	IDT54/74FCT251T				IDT54/74FCT251AT				IDT54/74FCT251CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay SN to $\overline{Z}$	CL = 50pF RL = 500Ω	1.5	9.0	1.5	9.5	1.5	6.6	1.5	7.4	1.5	5.6	1.5	6.2	ns
tPLH tPHL	Propagation Delay SN to Z		1.5	11.0	1.5	14.0	1.5	6.8	1.5	7.6	1.5	5.8	1.5	6.5	ns
tPLH tPHL	Propagation Delay IN to $\overline{Z}$		1.5	7.0	1.5	8.0	1.5	5.2	1.5	5.8	1.5	4.4	1.5	4.9	ns
tPLH tPHL	Propagation Delay IN to Z		1.5	7.0	1.5	8.0	1.5	5.5	1.5	6.1	1.5	4.7	1.5	5.2	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to $\overline{Z}$		1.5	9.0	1.5	10.0	1.5	6.7	1.5	7.4	1.5	5.7	1.5	6.3	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to $\overline{Z}$		1.5	7.5	1.5	8.5	1.5	6.0	1.5	6.4	1.5	5.0	1.5	5.4	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to Z		1.5	9.0	1.5	10.0	1.5	6.7	1.5	7.6	1.5	5.7	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to Z		1.5	7.0	1.5	7.0	1.5	6.0	1.5	6.3	1.5	5.0	1.5	5.2	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2635 tbl 08

Integrated Device Technology, Inc.

FAST CMOS QUAD 2-INPUT MULTIPLEXER

IDT54/74FCT157T/AT/CT
IDT54/74FCT257T/AT/CT

FEATURES:

- IDT54/74FCT157T/257T equivalent to FAST™ speed and drive
- **IDT54/74FCT157AT/257AT 25% faster than FAST**
- **IDT54/74FCT157CT/257CT 50% faster than FAST**
- TTL input and output level compatible
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- Product available in Radiation Tolerant and Radiation Enhanced Versions
- Military product compliant to MIL-STD-883, Class B and DESC listed

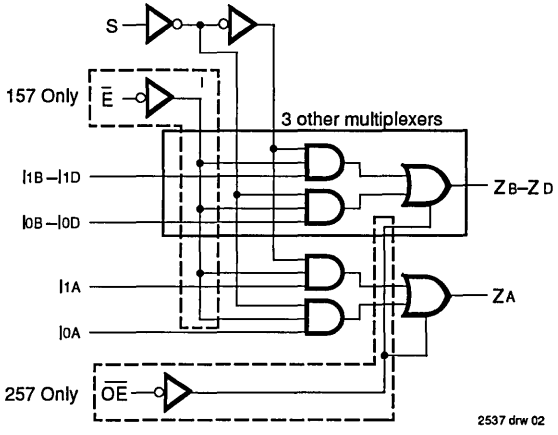
DESCRIPTION:

The IDT54/74FCT157T/AT/CT and IDT54/74FCT257T/AT/CT are high-speed quad 2-input multiplexers built using advanced CEMOS™, a dual metal CMOS technology. Four bits of data from two sources can be selected using the common select input. The four buffered outputs present the selected data in the true (non-inverting) form.

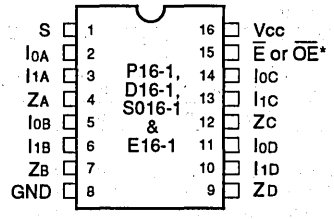
The IDT54/74FCT157T/AT/CT has a common, active-LOW, enable input. When the enable input is not active, all four outputs are held LOW. A common application of 'FCT157T is to move data from two different groups of registers to a common bus. Another application is as a function generator. The 'FCT157T can generate any four of the 16 different functions of two variables with one variable common.

The IDT54/74FCT257T/AT/CT has a common Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, all outputs are switched to a high-impedance state allowing the outputs to interface directly with bus-oriented systems.

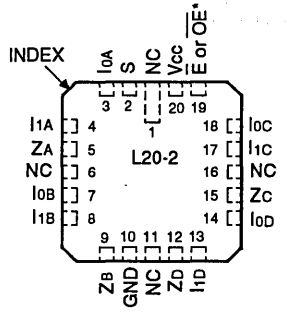
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOIC/CERPACK TOP VIEW



LCC TOP VIEW

2537 drw 01

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FAST is a trademark of National Semiconductor Co.

* $\overline{E}$ for FCT157, $\overline{OE}$ for FCT257.

PIN DESCRIPTION

Pin Names	Description
I_{0A}–I_{0D}	Source 0 Data Inputs
I_{1A}–I_{1D}	Source 1 Data Inputs
$\overline{E}$	Enable Input (Active LOW)–FCT157T
$\overline{OE}$	Output Enable (Active LOW)–FCT257T
S	Select Input
Z_A–Z_D	Outputs

2537 tbl 05

FUNCTION TABLE[1]

Inputs				Output Z_N	
$\overline{E}/\overline{OE}$	S	I_0	I_1	157	257
H	X	X	X	L	Z
L	H	X	L	L	L
L	H	X	H	H	H
L	L	L	X	L	L
L	L	H	X	H	H

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

2537 tbl 06

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

2537 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

2537 tbl 02

1. This parameter is guaranteed but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_{OZH}	High Impedance Output	V_{CC} = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}	Current		V_O = 0.5V	—	—	–10	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –6mA MIL.	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA COM'L.				
			I_{OH} = –12mA MIL.	2.0	3.0	—	V
			I_{OH} = –15mA COM'L.				
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 32mA MIL.	—	0.3	0.5	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA COM'L.				
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2537 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling	V_{IN} = Vcc V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{IN} = Vcc Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{E}$ or $\overline{OE}$ = GND Four Bits Toggling	V_{IN} = Vcc V_{IN} = GND	—	1.7	4.0[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	2.7	8.0[5]	

2537 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE – FCT157T/AT/CT

Symbol	Parameter	Condition[1]	54/74FCT157T				54/74FCT157AT				54/74FCT157CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay In to Zn	CL = 50 pF RL = 500Ω	1.5	6.0	1.5	7.0	1.5	5.0	1.5	5.8	1.5	4.3	1.5	5.0	ns
tPLH tPHL	Propagation Delay $\overline{E}$ to Zn		1.5	10.5	1.5	12.0	1.5	6.0	1.5	7.4	1.5	4.8	1.5	5.9	ns
tPLH tPHL	Propagation Delay S to Zn		1.5	10.5	1.5	12.0	1.5	7.0	1.5	8.1	1.5	5.2	1.5	6.0	ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE – FCT257T/AT/CT

Symbol	Parameter	Condition[1]	54/74FCT257T				54/74FCT257AT				54/74FCT257CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay In to Zn	CL = 50 pF RL = 500Ω	1.5	6.0	1.5	7.0	1.5	5.0	1.5	5.8	1.5	4.3	1.5	5.0	ns
tPLH tPHL	Propagation Delay S to Zn		1.5	10.5	1.5	12.0	1.5	7.0	1.5	8.1	1.5	5.2	1.5	6.0	ns
tPZH tPZL	Output Enable Time		1.5	8.5	1.5	10.0	1.5	7.0	1.5	8.0	1.5	6.0	1.5	6.8	ns
tPHZ tPLZ	Output Disable Time		1.5	6.0	1.5	8.0	1.5	5.5	1.5	5.8	1.5	5.0	1.5	5.3	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2537 tbl 07

6

Integrated Device Technology, Inc.

FAST CMOS SYNCHRONOUS PRESETTABLE BINARY COUNTERS

IDT54/74FCT161T/AT/CT
IDT54/74FCT163T/AT/CT

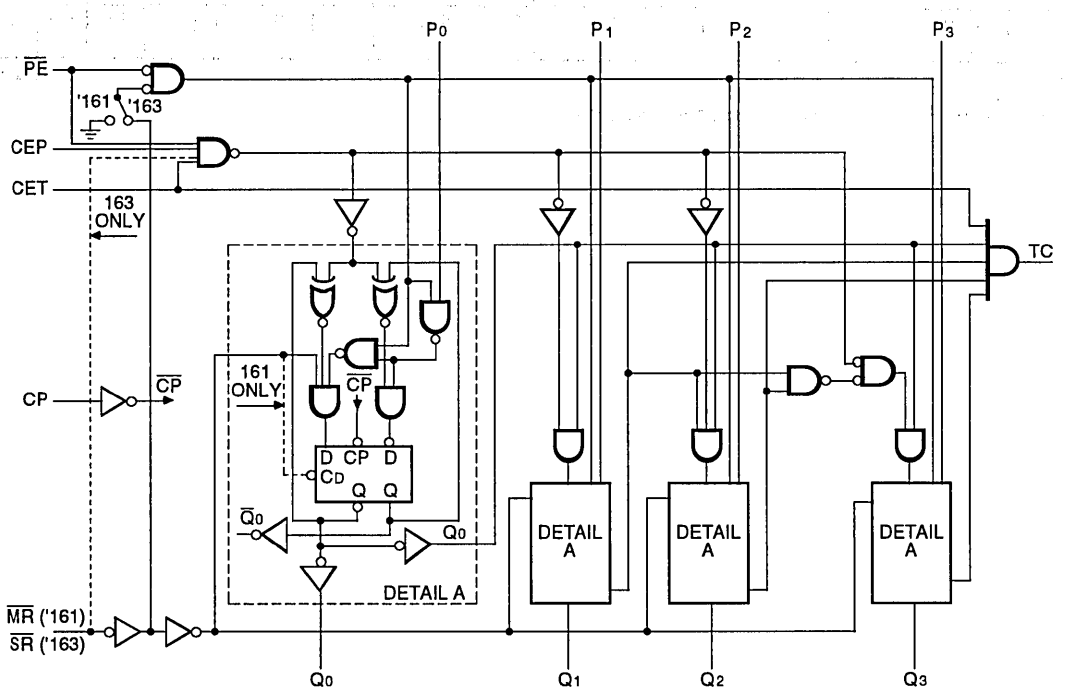
FEATURES:

- IDT54/74FCT161T/163T equivalent to FAST™ speed
- **IDT54/74FCT161AT/163AT 35% faster than FAST**
- **IDT54/74FCT161CT/163CT 45% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- IOL = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- True TTL input and output levels
- Substantially lower input current levels than FAST (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT161T/163T, IDT54/74FCT161AT/163AT and IDT54/74FCT161CT/163CT are high-speed synchronous modulo-16 binary counters built using advanced CEMOS™, a dual metal CMOS technology. They are synchronously presettable for application in programmable dividers and have two types of count enable inputs plus a terminal count output for versatility in forming synchronous multi-stage counters. The IDT54/74FCT161T/AT/CT have asynchronous Master Reset inputs that override all other inputs and force the outputs LOW. The IDT54/74FCT163T/AT/CT have Synchronous Reset inputs that override counting and parallel loading and allow the outputs to be simultaneously reset on the rising edge of the clock.

FUNCTIONAL BLOCK DIAGRAM



2611 drw 01

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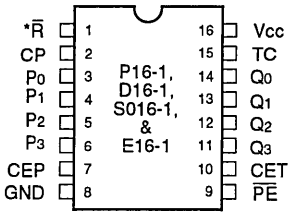
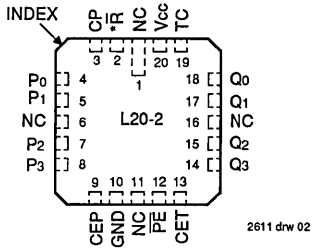
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

*$\overline{MR}$ for '161
*$\overline{SR}$ for '163

PIN DESCRIPTION

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$ ('161)	Asynchronous Master Reset Input (Active LOW)
$\overline{SR}$ ('163)	Synchronous Reset Input (Active LOW)
P0-3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q0-3	Flip-Flop Outputs
TC	Terminal Count Output

FUNCTION TABLE[2]

$\overline{SR}$[1]	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge(s)
L	X	X	X	Reset (Clear)
H	L	X	X	Load (Pn→Qn)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

NOTES: 2611 tbl 06
1. For FCT163/163A only.
2. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care.

2611 tbl 05

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
VTERM[3]	Terminal Voltage with Respect to GND	–0.5 to VCC	–0.5 to VCC	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

NOTES: 2611 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

NOTE: 2611 tbl 02
1. This parameter is guaranteed at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = –55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	COM'L[4]	2.0V	—	—	V
			MIL	2.7V	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	Vcc = Max.	V_I = 0.5V	—	—	–5	µA
I_I	Input HIGH Current	Vcc = Max., V_I = Vcc (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL}= 32mA MIL. I_{OL}= 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	Vcc = Max. V_{IN} = GND or Vcc		—	0.2	1.5	mA

2611 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Clock pin requires a minimum V_{IH} of 2.5V.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open Load Mode $\overline{CEP}$ = $\overline{CET}$ = $\overline{PE}$ = GND $\overline{MR}$ or $\overline{SR}$ = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open Load Mode f_{CP} = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
		$\overline{CEP}$ = $\overline{CET}$ = $\overline{PE}$ = GND $\overline{MR}$ or $\overline{SR}$ = V_{CC} One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max., Outputs Open Load Mode f_{CP} = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.0	7.8[5]	
		$\overline{CEP}$ = $\overline{CET}$ = $\overline{PE}$ = GND $\overline{MR}$ or $\overline{SR}$ = V_{CC} Four Bits Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	5.2	12.8[5]	

2611 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT161T IDT54/74FCT163T				IDT54/74FCT161AT IDT54/74FCT163AT				IDT54/74FCT161CT IDT54/74FCT163CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to Qn ($\overline{PE}$ Input HIGH)	CL = 50pF RL = 500Ω	2.0	11.0	2.0	11.5	2.0	7.2	2.0	7.5	2.0	5.8	2.0	6.3	ns
tPLH tPHL	Propagation Delay CP to Qn ($\overline{PE}$ Input LOW)		2.0	9.5	2.0	10.0	2.0	6.2	2.0	6.5	2.0	5.8	2.0	6.3	ns
tPLH tPHL	Propagation Delay CP to TC		2.0	15.0	2.0	16.5	2.0	9.8	2.0	10.8	2.0	7.4	2.0	8.3	ns
tPLH tPHL	Propagation Delay CET to TC		1.5	8.5	1.5	9.0	1.5	5.5	1.5	5.9	1.5	5.2	1.5	5.6	ns
tPHL	Propagation Delay $\overline{MR}$ to Qn ('161)		2.0	13.0	2.0	14.0	2.0	8.5	2.0	9.1	2.0	6.0	2.0	6.6	ns
tPHL	Propagation Delay $\overline{MR}$ to TC ('161)		2.0	11.5	2.0	12.5	2.0	7.5	2.0	8.2	2.0	7.0	2.0	7.7	ns
tSU	Set-up Time, HIGH or LOW Pn to CP		5.0	—	5.5	—	4.0	—	4.5	—	4.0	—	4.5	—	ns
tH	Hold Time, HIGH or LOW Pn to CP		1.5	—	2.0	—	1.5	—	2.0	—	1.5	—	2.0	—	ns
tSU	Set-up Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		11.5	—	13.5	—	9.5	—	11.5	—	9.5	—	11.5	—	ns
tH	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tSU	Set-up Time, HIGH or LOW CEP or CET to CP		11.5	—	13.0	—	9.5	—	11.0	—	9.5	—	11.0	—	ns
tH	Hold Time, HIGH or LOW CEP or CET to CP		0	—	0	—	0	—	0	—	0	—	0	—	ns
tW	Clock Pulse Width (Load) HIGH or LOW		5.0	—	5.0	—	4.0[3]	—	4.0[3]	—	4.0[3]	—	4.0[3]	—	ns
tW	Clock Pulse Width (Count) HIGH or LOW		7.0	—	8.0	—	6.0	—	7.0	—	6.0	—	7.0	—	ns
tW	$\overline{MR}$ Pulse Width, LOW ('161)		5.0	—	5.0	—	4.0[3]	—	4.0[3]	—	4.0[3]	—	4.0[3]	—	ns
tREM	Recovery Time $\overline{MR}$ to CP ('161)		6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This limit is guaranteed but not tested.

2611 tbl 07

Integrated Device Technology, Inc.

FAST CMOS UP/DOWN BINARY COUNTER

IDT54/74FCT191T
IDT54/74FCT191AT

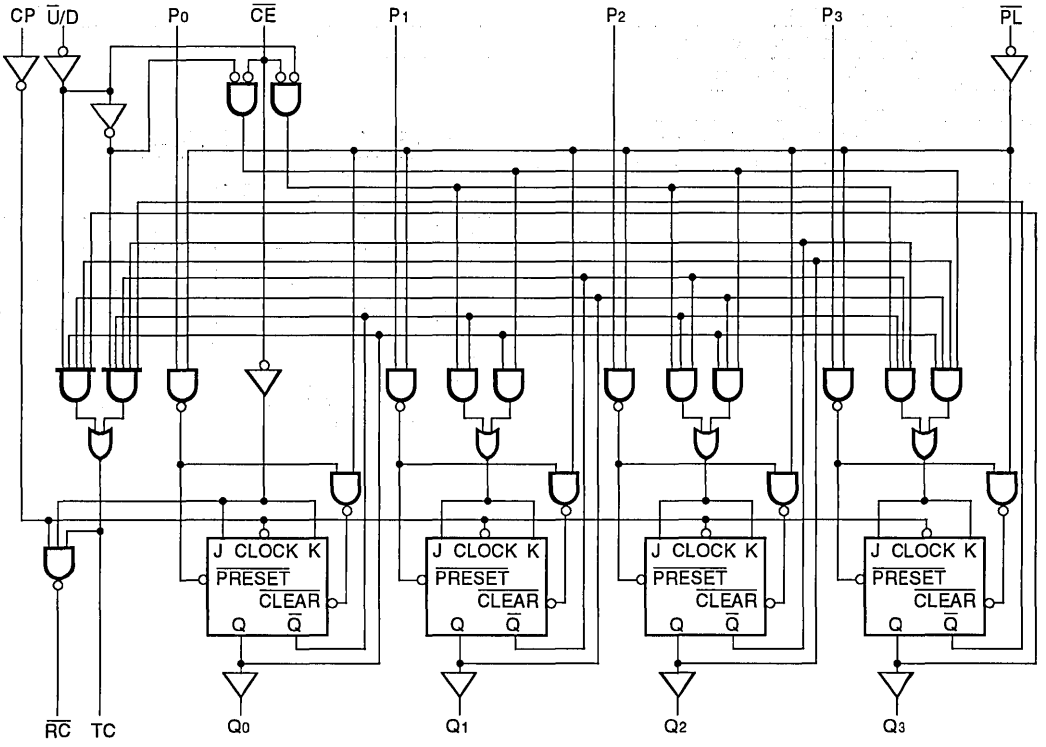
FEATURES:

- IDT54/74FCT191T equivalent to FAST™ speed
- **IDT54/74FCT191AT 35% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- True TTL input and output levels
- Substantially lower input current levels than FAST (5µA max.)
- JEDEC standard pinout for DIP, LCC and SOIC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT191T and IDT54/74FCT191AT are reversible modulo-16 binary counters, featuring synchronous counting and asynchronous presetting and are built using advanced CEMOS™, a dual metal CMOS technology. The preset feature allows the IDT54/74FCT191T and IDT54/74FCT191AT to be used in programmable dividers. The count enable input, terminal count output and ripple clock output make possible a variety of methods of implementing multiusage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

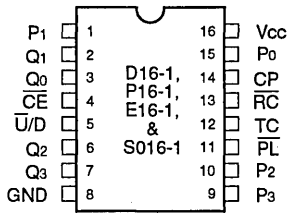
FUNCTIONAL BLOCK DIAGRAM



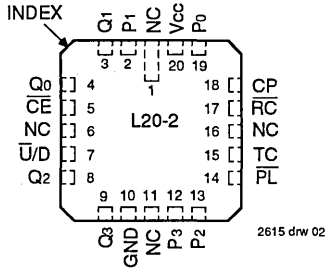
2615 drw 01

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
P0-3	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
$\overline{U}$/D	Up/Down Count Control Input
Q0-3	Flip-Flop Outputs
$\overline{RC}$	Ripple Clock Output (Active LOW)
TC	Terminal Count Output (Active HIGH)

2615 tbl 05

$\overline{RC}$ FUNCTION TABLE[2]

Inputs		Outputs	
$\overline{CE}$	CP	TC[1]	$\overline{RC}$
L	⊓	H	⊓
H	X	X	H
X	X	L	H

2615 tbl 06

MODE SELECT FUNCTION TABLE[2]

Inputs				
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	Mode
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Preset (Asynchronous)
H	H	X	X	No Change (Hold)

NOTES:
2615 tbl 07

1. TC is generated internally.
2. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, ↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2615 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Inputs and V_{CC} terminals.
3. Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2615 tbl 02

1. This parameter is guaranteed at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	COM'L(4)	2.0V	—	—	V
			MIL	2.7V	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL}= 32mA MIL. I_{OL}= 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES: 2615 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Clock pin requires a minimum V_{IH} of 2.5V.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open Preset Mode $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open Preset Mode $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.0	2.8	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.2	3.8	
		V_{CC} = Max., Outputs Open Preset Mode $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND Four Bits Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	4.2	10.5[5]	

2615 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT191T				IDT54/74FCT191AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	C_L = 50pF R_L = 500Ω	2.5	12.0	1.5	16.0	2.5	7.8	1.5	10.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC		3.0	14.0	2.0	16.0	3.0	11.8	2.0	12.2	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$		2.5	8.5	1.5	12.5	2.5	8.5	1.5	10.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$		2.0	8.0	2.0	8.5	2.0	7.2	2.0	8.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{RC}$		4.0	20.0	4.0	22.5	4.0	13.0	4.0	14.7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to TC		3.0	11.0	3.0	13.0	3.0	7.2	3.0	8.5	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		2.0	14.0	1.5	16.0	2.0	9.1	1.5	10.4	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		3.0	13.0	3.0	14.0	3.0	8.5	3.0	9.1	ns
t_{SU}	Set-up Time, HIGH or LOW P_n to $\overline{PL}$		5.0	—	6.0	—	4.0	—	5.0	—	ns
t_H	Hold Time, HIGH or LOW P_n to $\overline{PL}$		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{SU}	Set-up Time LOW $\overline{CE}$ to CP		10.0	—	10.5	—	9.0	—	9.5	—	ns
t_H	Hold Time LOW $\overline{CE}$ to CP		0	—	0	—	0	—	0	—	ns
t_{SU}	Set-up Time, HIGH or LOW $\overline{U}$/D to CP		12.0	—	12.0	—	10.0	—	10.0	—	ns
t_H	Hold Time, HIGH or LOW $\overline{U}$/D to CP		0	—	0	—	0	—	0	—	ns
t_W	$\overline{PL}$ Pulse Width LOW		6.0	—	8.5	—	5.5	—	8.0	—	ns
t_W	Clock Pulse Width HIGH or LOW		5.0	—	7.0	—	4.0[3]	—	6.0	—	ns
t_{REM}	Recovery Time $\overline{PL}$ to CP		6.0	—	7.5	—	5.0	—	6.5	—	ns

NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This limit is guaranteed but not tested.

2615 tbl 08

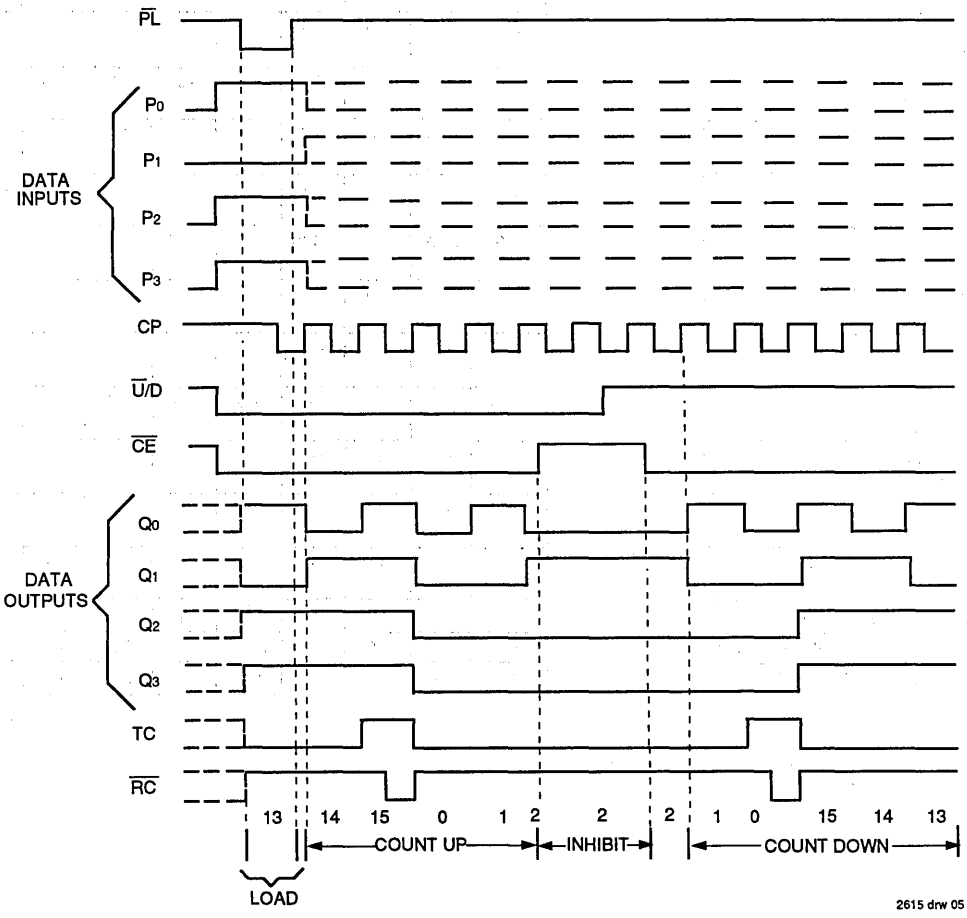
6

TIMING WAVEFORMS

Typical load, count and inhibit sequences

Illustrated below is the following sequence:

- Load (preset) to binary thirteen
- Count up to fourteen, fifteen (maximum), zero, one and two
- Inhibit
- Count down to one, zero (minimum), fifteen, fourteen and thirteen



Integrated Device Technology, Inc.

FAST CMOS UP/DOWN BINARY COUNTERS

IDT54/74FCT193T
IDT54/74FCT193AT

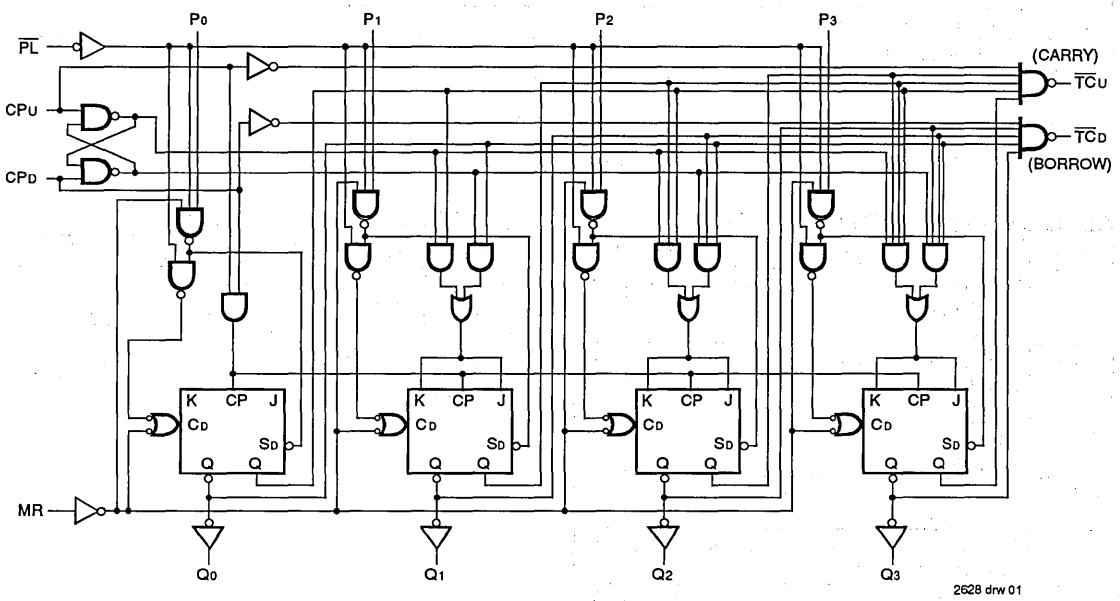
FEATURES:

- IDT54/74FCT193T equivalent to FAST™ speed
- **IDT54/74FCT193AT 35% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- Substantially lower input current levels than FAST (5µA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

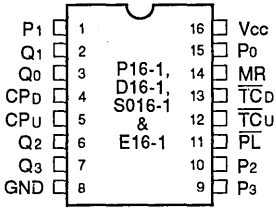
The IDT54/74FCT193T and IDT54/74FCT193AT are up/down modulo-16 binary counters built using advanced CEMOS™, a dual metal CMOS technology. Separate count-up and count-down clocks are used and, in either counting mode, the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs. Separate terminal count-up and terminal count-down outputs are provided that are used as the clocks for subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

FUNCTIONAL BLOCK DIAGRAM

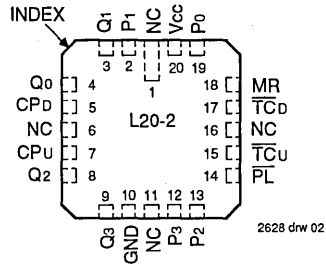


CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
CP_U	Count Up Clock Input (Active Rising Edge)
CP_D	Count Down Clock Input (Active Rising Edge)
MR	Asynchronous Master Reset (Active HIGH)
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
P_n	Parallel Data Inputs
Q_n	Flip-flop Outputs
$\overline{TC_D}$	Terminal Count Down (Borrow) Output (Active LOW)
$\overline{TC_U}$	Terminal Count Up (Carry) Output (Active LOW)

2628 tbl 05

FUNCTION TABLE[1]

MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	↑	H	Count Up
L	H	H	↑	Count Down

NOTE: 2628 tbl 06
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Clock Transition.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2628 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals.
3. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2628 tbl 02
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		COM'L[4]	2.0V	—	—	V
				MIL	2.7V	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level			—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V		—	—	–5	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)			—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA			—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND			–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.		2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.		2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL}= 32mA MIL. I_{OL}= 48mA COM'L.		—	0.3	0.5	V
V_H	Input Hysteresis	—			—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}			—	0.2	1.5	mA

2628 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Clock pin requires a minimum V_{IH} of 2.5V.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open Preset Mode $\overline{PL}$ = MR = CP_U = CP_D = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open Preset Mode $\overline{PL}$ = MR = CP_U = CP_D = GND One Bit Toggling at f_i = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open Preset Mode $\overline{PL}$ = MR = CP_U = CP_D = GND Four Bits Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	4.2	10.5[5]	

2628 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT193T				IDT54/74FCT193AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to $\overline{TC_U}$ or $\overline{TC_D}$	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	10.5	2.0	6.5	2.0	6.9	ns
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to Q_n		2.0	13.5	2.0	14.0	2.0	8.8	2.0	9.1	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		2.0	15.5	2.0	16.5	2.0	10.1	2.0	10.8	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		2.0	14.0	2.0	13.5	2.0	8.8	2.0	9.1	ns
t_{PHL}	Propagation Delay MR to Q_n		3.0	15.5	3.0	16.0	3.0	10.1	3.0	10.4	ns
t_{PLH}	Propagation Delay MR to $\overline{TC_U}$		3.0	14.5	3.0	15.0	3.0	9.4	3.0	9.8	ns
t_{PHL}	Propagation Delay MR to $\overline{TC_D}$		3.0	15.5	3.0	16.0	3.0	10.1	3.0	10.4	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to $\overline{TC_U}$ or $\overline{TC_D}$		3.0	16.5	3.0	18.5	3.0	10.8	3.0	12.0	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to $\overline{TC_U}$ or $\overline{TC_D}$		3.0	15.5	3.0	16.5	3.0	10.1	3.0	10.8	ns
t_{SU}	Set-up Time, HIGH or LOW P_n to $\overline{PL}$		5.0	—	6.0	—	4.0	—	5.0	—	ns
t_H	Hold Time, HIGH or LOW P_n to $\overline{PL}$		2.0	—	2.0	—	1.5	—	1.5	—	ns
t_W	$\overline{PL}$ Pulse Width LOW		6.0	—	7.5	—	5.0	—	6.5	—	ns
t_W	CP_U or CP_D Pulse Width HIGH or LOW		5.0	—	7.0	—	4.0[3]	—	6.0	—	ns
t_W	CP_U or CP_D Pulse Width LOW (Change of Direction)		10.0	—	12.0	—	8.0	—	10.0	—	ns
t_W	MR Pulse Width HIGH		6.0	—	6.0	—	5.0	—	5.0	—	ns
t_{REM}	Recovery Time $\overline{PL}$ to CP_U or CP_D		6.0	—	8.0	—	5.0	—	7.0	—	ns
t_{REM}	Recovery Time MR to CP_U or CP_D		4.0	—	4.5	—	3.0	—	3.5	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2628 tbl 07

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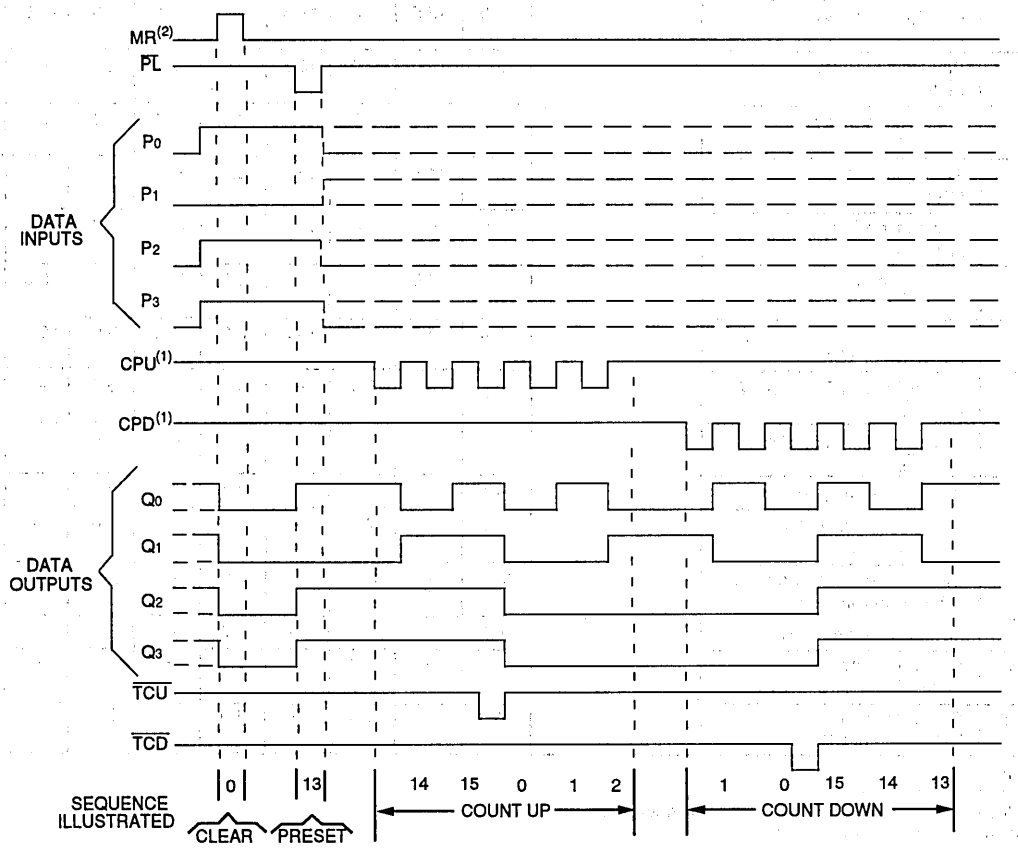
TIMING WAVEFORMS

Typical clear, load and count sequences

Illustrated below is the following sequence:

- Clear outputs to zero.
- Load (preset) to binary thirteen.
- Count up to fourteen, fifteen, carry zero, one and two.
- Count down to one, zero, borrow, fifteen, fourteen and thirteen.



2628 drw 04

NOTES:

1. MR overrrides load, data, and count inputs.
2. When counting up, CPD input must be HIGH; when counting down, CPU input must be HIGH.

Integrated Device Technology, Inc.

FAST CMOS OCTAL BUFFER/LINE DRIVERS

IDT54/74FCT240T/AT/CT/DT
IDT54/74FCT241T/AT/CT/DT
IDT54/74FCT244T/AT/CT/DT
IDT54/74FCT540T/AT/CT
IDT54/74FCT541T/AT/CT

FEATURES:

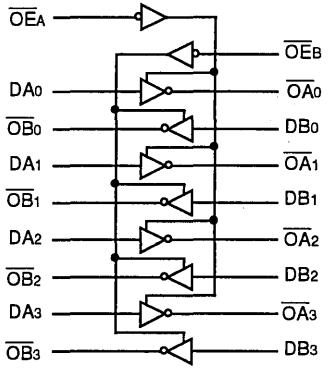
- Fastest CMOS logic family available
- Std., A, C, and D speed grades with 3.6ns t_{PD}
- Available in DIP, SOIC, SSOP, CERPACK and LCC packages
- True TTL input and output compatible
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (1mW typ. static)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Meets or exceeds JEDEC Standard 18 specifications

DESCRIPTION:

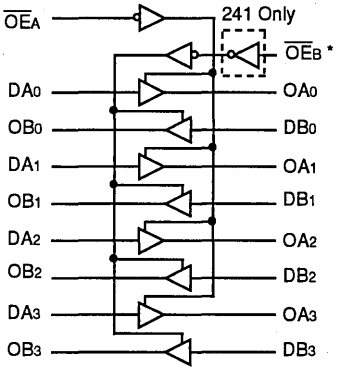
The IDT octal buffer/line drivers are built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT240T/AT/CT/DT, IDT54/74FCT241T/AT/CT/DT and IDT54/74FCT244T/AT/CT/DT are designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitter/receivers which provide improved board density.

The IDT54/74FCT540T/AT/CT and IDT54/74FCT541T/AT/CT are similar in function to the IDT54/74FCT240T/AT/CT/DT and IDT54/74FCT244T/AT/CT/DT, respectively, except that the inputs and outputs are on opposite sides of the package. This pinout arrangement makes these devices especially useful as output ports for microprocessors and as backplane drivers, allowing ease of layout and greater board density.

FUNCTIONAL BLOCK DIAGRAMS

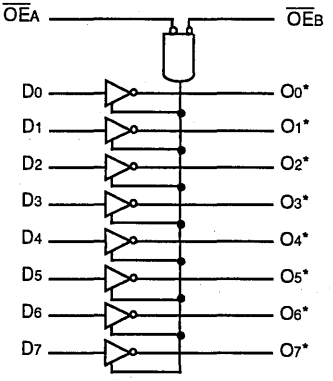


IDT54/74FCT240T



IDT54/74FCT241T/244T

* $\overline{OE}_B$ for 241T, $\overline{OE}_B$ for 244T



IDT54/74FCT540T/541T

*Logic diagram shown for 'FCT540T. 'FCT541T is the non-inverting option.

2565 cnv* 01

2565 cnv* 02

2565 cnv* 03

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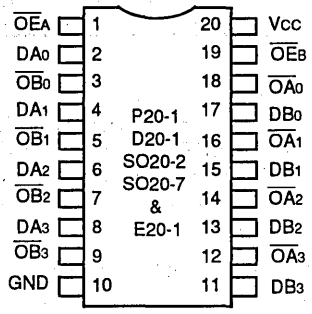
CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

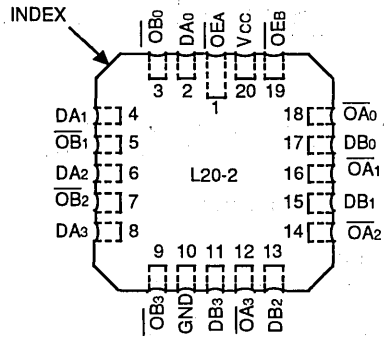
PIN CONFIGURATIONS

IDT54/74FCT240T



DIP/SOIC/SSOP/CERPACK
TOP VIEW

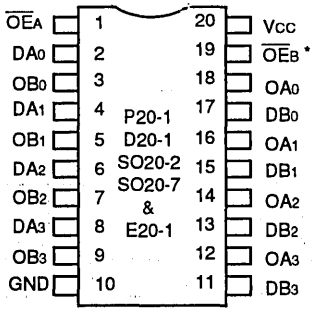
2565cnv* 04



LCC
TOP VIEW

2565cnv* 07

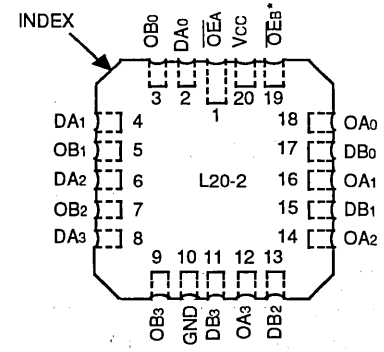
IDT54/74FCT241T/244T



DIP/SOIC/SSOP/CERPACK
TOP VIEW

*OEB for 241T, $\overline{OE_B}$ for 244T

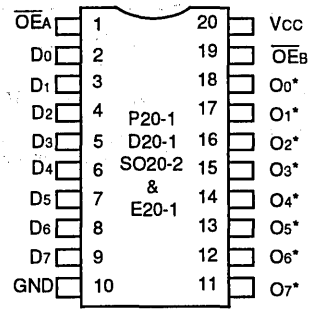
2565cnv* 05



LCC
TOP VIEW

2565cnv* 08

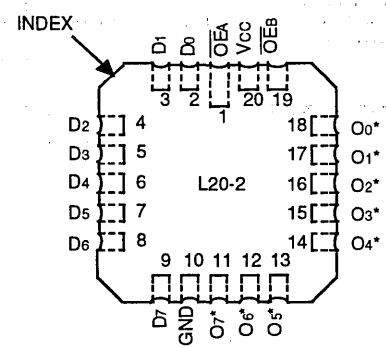
IDT54/74FCT540T/541T



DIP/SOIC/CERPACK
TOP VIEW

*$\overline{O}$x for 540T, Ox for 541T

2565cnv* 06



LCC
TOP VIEW

2565cnv* 09

PIN DESCRIPTION

Pin Names	Description
$\overline{OE_A}$, $\overline{OE_B}$	3-State Output Enable Inputs (Active LOW)
OE_B[1]	3-State Output Enable Input (Active HIGH)
Dxx	Inputs
Oxx	Outputs

NOTE: 2565 tbl 04
1. OE_B for 241 only.

FUNCTION TABLE

Inputs[1]				Outputs[1]				
$\overline{OE_A}$	$\overline{OE_B}$	OE_B[2]	D	240	241	244	540	541
L	L	H	L	H	L	L	H	L
L	L	H	H	L	H	H	L	H
H	H	L	X	Z	Z	Z	Z	Z

NOTES: 2565 tbl 05
1. H = High Voltage Level
   X = Don't Care
   L = Low Voltage Level
   Z = High Impedance
2. OE_B for 241 only.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +150	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2565 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2565 tbl 02
1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	−5	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	−10	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		—	−0.7	−1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		−60	−120	−225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −6mA MIL. I_{OH} = −8mA COM'L.	2.4	3.3	—	V
			I_{OH} = −12mA MIL. I_{OH} = −15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES:
2565 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE_A}$ = $\overline{OE_B}$ = GND or $\overline{OE_A}$ = GND, OE_B = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi =10MHz 50% Duty Cycle $\overline{OE_A}$ = $\overline{OE_B}$ = GND or $\overline{OE_A}$ = GND, OE_B = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $\overline{OE_A}$ = $\overline{OE_B}$ = GND or $\overline{OE_A}$ = GND, OE_B = V_{CC} Eight Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2565 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT240T

Symbol	Parameter	Condition[1]	54/74FCT240T				54/74FCT240AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay D_N to $\overline{O}_N$	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	ns
tPZH tPZL	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	ns

2565 tbl 07

Symbol	Parameter	Condition[1]	54/74FCT240CT				54/74FCT240DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay D_N to $\overline{O}_N$	C_L = 50pF R_L = 500Ω	1.5	4.3	1.5	4.7	1.5	3.6	—	—	ns
tPZH tPZL	Output Enable Time		1.5	5.8	1.5	6.5	1.5	4.8	—	—	ns
tPHZ tPLZ	Output Disable Time		1.5	5.2	1.5	5.7	1.5	4.0	—	—	ns

2565 tbl 08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT241T AND FCT244T

Symbol	Parameter	Condition[1]	54/74FCT241T/244T				54/74FCT241AT/244AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay D_N to O_N	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	ns
tPZH tPZL	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	ns

2565 tbl 09

Symbol	Parameter	Condition[1]	54/74FCT241CT/244CT				54/74FCT241DT/244DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay D_N to O_N	C_L = 50pF R_L = 500Ω	1.5	4.1	1.5	4.6	1.5	3.6	—	—	ns
tPZH tPZL	Output Enable Time		1.5	5.8	1.5	6.5	1.5	4.8	—	—	ns
tPHZ tPLZ	Output Disable Time		1.5	5.2	1.5	5.7	1.5	4.0	—	—	ns

2565 tbl 10

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT540T AND FCT541T

Symbol	Parameter	Condition[1]	54/74FCT540T/541T				54/74FCT540AT/541AT				54/74FCT540CT/541CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DN to ON IDT54/74FCT540T	CL = 50pF RL = 500Ω	1.5	8.5	1.5	9.5	1.5	4.8	1.5	5.1	1.5	4.3	1.5	4.7	ns
tPLH tPHL	Propagation Delay DN to ON IDT54/74FCT541T		1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	1.5	4.1	1.5	4.6	ns
tPZH tPZL	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns

2565 tbl 11

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

6

Integrated Device Technology, Inc.

FAST CMOS OCTAL BIDIRECTIONAL TRANSCEIVERS

IDT54/74FCT245T/AT/CT/DT
IDT54/74FCT640T/AT/CT
IDT54/74FCT645T/AT/CT/DT

FEATURES:

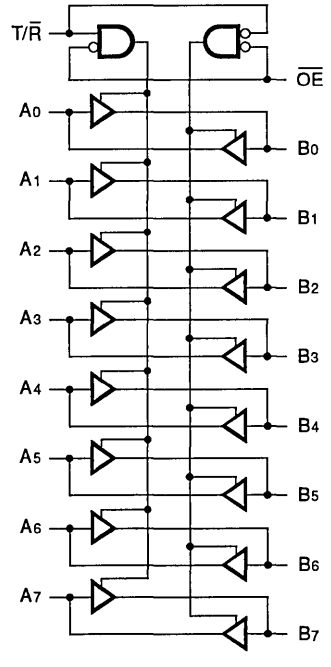
- Fastest CMOS logic family available
- Std., A, C, and D speed grades with 3.8ns t_{PD}
- Available in DIP, SOIC, SSOP, CERPACK and LCC packages
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (2.5mW typical static)
- Direction control and over-riding 3-state control
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed
- Meets or exceeds JEDEC Standard 18 specifications

DESCRIPTION:

The IDT octal bidirectional transceivers are built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT245T/AT/CT/DT, IDT54/74FCT640T/AT/CT and IDT54/74FCT645T/AT/CT/DT are designed for asynchronous two-way communication between data buses. The transmit/receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports, and receive (active LOW) from B ports to A ports. The output enable ($\overline{OE}$) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

The IDT54/74FCT245T/AT/CT/DT and IDT54/74FCT645T/AT/CT/DT transceivers have non-inverting outputs. The IDT54/74FCT640T/AT/CT has inverting outputs.

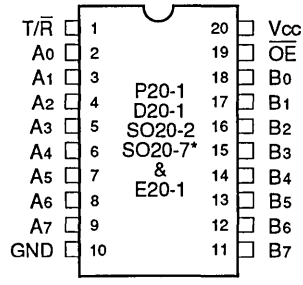
FUNCTIONAL BLOCK DIAGRAM



2539 drw 01

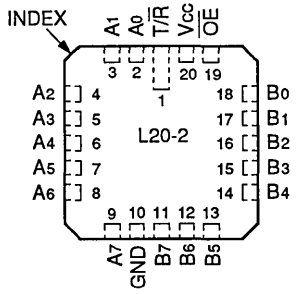
FCT245T, 645T are non-inverting options.
FCT640T is the inverting option.

PIN CONFIGURATIONS



DIP/SOIC/SSOP/CERPACK
TOP VIEW

*FCT245/645T/AT/CT/DT only.



2539 drw 02

LCC
TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or 3-State Outputs
B_0–B_7	Side B Inputs or 3-State Outputs

2539 tbl 05

FUNCTION TABLE[2]

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A[1]
L	H	Bus A Data to Bus B[1]
H	X	High Z State

NOTES: 2539 tbl 06

1. 640 is inverting from input to output.
2. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

NOTES: 2539 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2539 tbl 02

1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max	Except I/O Pins	—	—	5	µA
		V_I = 2.7V	I/O Pins	—	—	15	
I_{IL}	Input LOW Current	V_{CC} = Max	Except I/O Pins	—	—	–5	µA
		V_I = 0.5V	I/O Pins	—	—	–15	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –6mA Mil.	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA Com'l.				
			I_{OH} = –12mA Mil.	2.0	3.0	—	
			I_{OH} = –15mA Com'l.				
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 48mA Mil.	—	0.3	0.55	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA Com'l.				
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = V_{CC} or GND		—	0.5	1.5	mA

2539 tbl 03

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = T/$\overline{R}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = T/$\overline{R}$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	2.0	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.3	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = T/$\overline{R}$ = GND Eight Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.5	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.5	14.5[5]	

NOTES:

2539 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT245T

Symbol	Parameter	Conditions[1]	54/74FCT245T				54/74FCT245AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	C_L = 50 pF R_L = 500Ω	1.5	7.0	1.5	7.5	1.5	4.6	1.5	4.9	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A or B		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	ns
t_{PZH} t_{PZL}	Output Enable Time T/$\overline{R}$ to A or B[3]		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time T/$\overline{R}$ to A or B[3]		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	ns

2534 tbl 07

Symbol	Parameter	Conditions[1]	54/74FCT245CT				54/74FCT245DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	C_L = 50 pF R_L = 500Ω	1.5	4.1	1.5	4.5	1.5	3.8	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B		1.5	5.8	1.5	6.2	1.5	5.0	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A or B		1.5	4.8	1.5	5.2	1.5	4.3	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time T/$\overline{R}$ to A or B[3]		1.5	5.8	1.5	6.2	1.5	5.0	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time T/$\overline{R}$ to A or B[3]		1.5	4.8	1.5	5.2	1.5	4.3	—	—	ns

2534 tbl 08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT640T

Symbol	Parameter	Conditions[1]	54/74FCT640T				54/74FCT640AT				54/74FCT640CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	C_L = 50 pF R_L = 500Ω	2.0	7.0	2.0	8.0	1.5	5.0	1.5	5.3	1.5	4.4	1.5	4.7	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B		2.0	13.0	2.0	16.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A or B		2.0	10.0	2.0	12.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns
t_{PZH} t_{PZL}	Output Enable Time T/$\overline{R}$ to A or B[3]		2.0	13.0	2.0	16.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time T/$\overline{R}$ to A or B[3]		2.0	10.0	2.0	12.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns

2534 tbl 09

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT645T

Symbol	Parameter	Conditions[1]	54/74FCT645T				54/74FCT645AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay A to B, B to A	C_L = 50 pF R_L = 500Ω	1.5	9.5	1.5	11.0	1.5	4.6	1.5	4.9	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to A or B		1.5	11.0	1.5	12.0	1.5	6.2	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to A or B		1.5	12.0	1.5	13.0	1.5	5.0	1.5	6.0	ns
tPZH tPZL	Output Enable Time T/$\overline{R}$ to A or B[3]		1.5	11.0	1.5	12.0	1.5	6.2	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time T/$\overline{R}$ to A or B[3]		1.5	12.0	1.5	13.0	1.5	5.0	1.5	6.0	ns

2534 tbl 11

Symbol	Parameter	Conditions[1]	54/74FCT645CT				54/74FCT645DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay A to B, B to A	C_L = 50 pF R_L = 500Ω	1.5	4.1	1.5	4.5	1.5	3.8	—	—	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to A or B		1.5	5.8	1.5	6.2	1.5	5.0	—	—	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to A or B		1.5	4.8	1.5	5.2	1.5	4.3	—	—	ns
tPZH tPZL	Output Enable Time T/$\overline{R}$ to A or B[3]		1.5	5.8	1.5	6.2	1.5	5.0	—	—	ns
tPHZ tPLZ	Output Disable Time T/$\overline{R}$ to A or B[3]		1.5	4.8	1.5	5.2	1.5	4.3	—	—	ns

2534 tbl 12

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

6

Integrated Device Technology, Inc.

FAST CMOS OCTAL D FLIP-FLOP WITH MASTER RESET

IDT54/74/FCT273T
IDT54/74FCT273AT
IDT54/74FCT273CT

FEATURES:

- IDT54/74FCT273T equivalent to FAST™ speed
- **IDT54/74FCT273AT 45% faster than FAST**
- **IDT54/74FCT273CT 55% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- True TTL input and output levels
- Substantially lower input current levels than FAST (5µA max.)
- Octal D flip-flop with Master Reset
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

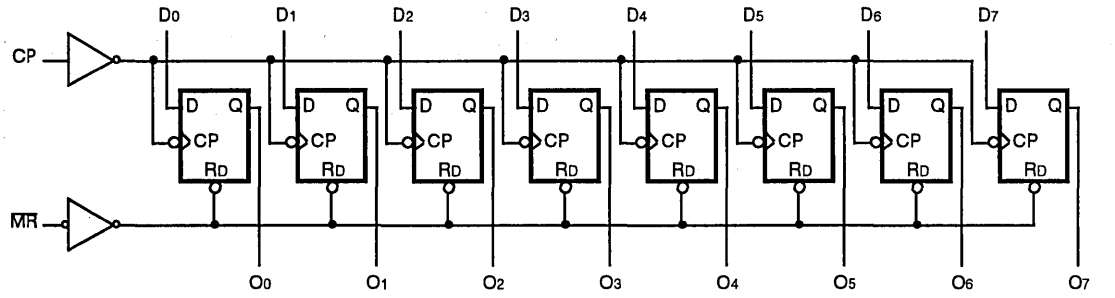
DESCRIPTION:

The IDT54/74FCT273T/AT/CT are octal D flip-flops built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT273T/AT/CT have eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output.

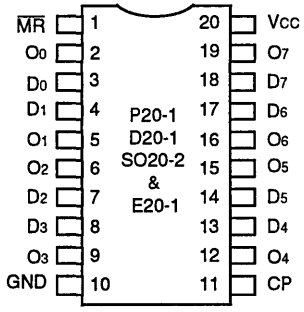
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

FUNCTIONAL BLOCK DIAGRAM



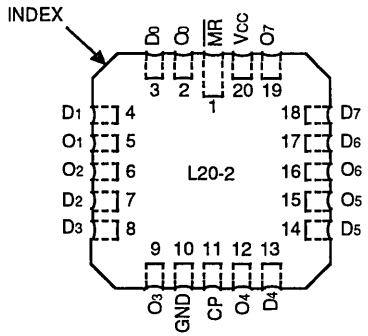
2568 cnv* 03

PIN CONFIGURATIONS



2568 cnv* 01

DIP/SOIC/CERPACK
TOP VIEW



2568 cnv* 02

LCC
TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
D_N	Data Inputs
$\overline{MR}$	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
O_N	Data Outputs

2568 tbl 05

FUNCTION TABLE[1]

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	D_N	O_N
Reset (Clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

NOTE: 2568 tbl 06

1. H = HIGH voltage level steady state
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
   L = LOW voltage level steady state
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
   X = Don't Care
   ↑ = LOW-to-HIGH Clock Transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2568 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Inputs and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2568 tbl 02

1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2568 tbl 03

NOTES:
1. For conditions shown as Max. or Min.; use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{MR}$ = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
		$\overline{MR}$ = V_{CC} One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.0	7.8[5]	
		$\overline{MR}$ = V_{CC} Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

NOTES:

2568 tbl 07

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT273T				IDT54/74FCT273AT				IDT54/74FCT273CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to On	CL = 50pF RL = 500Ω	2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	5.8	2.0	6.5	ns
tPHL	Propagation Delay $\overline{MR}$ to On		2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	6.1	2.0	6.8	ns
tSU	Set-up Time HIGH or LOW Dn to CP		3.0	—	3.5	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW Dn to CP		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tW	$\overline{MR}$ Pulse Width LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tREM	Recovery Time $\overline{MR}$ to CP		4.0	—	5.0	—	2.0	—	2.5	—	2.0	—	2.5	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2568 tbl 08

Integrated Device Technology, Inc.

FAST CMOS 8-INPUT UNIVERSAL SHIFT REGISTER

IDT54/74FCT299T
IDT54/74FCT299AT
IDT54/74FCT299CT

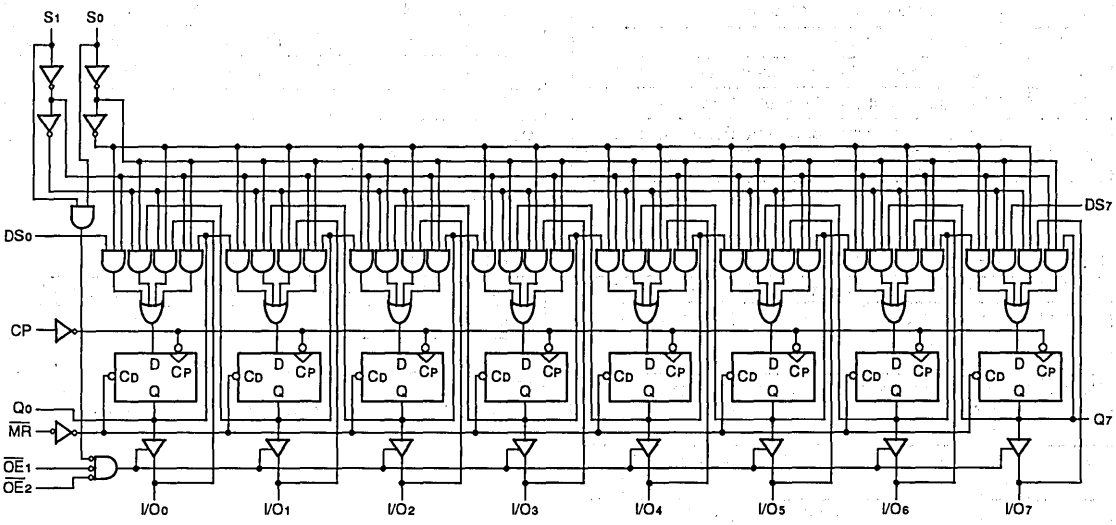
FEATURES:

- IDT54/74FCT299T equivalent to FAST™ speed
- IDT54/74FCT299AT 25% faster than FAST
- **IDT54/74FCT299CT 35% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- Substantially lower input current levels than FAST (5μA max.)
- 8-input universal shift register
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT299T and IDT54/74FCT299AT/CT are built using advanced CEMOS™, a dual-metal CMOS technology. The IDT54/74FCT299T and IDT54/74FCT299AT/CT are 8-input universal shift/storage registers with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

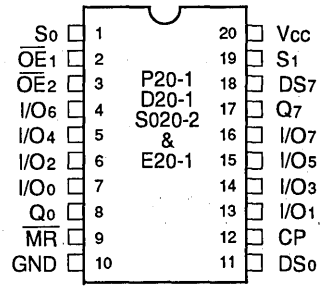
FUNCTIONAL BLOCK DIAGRAM



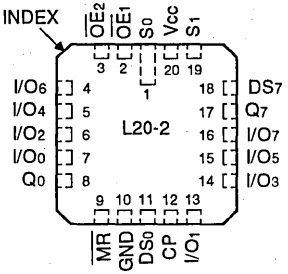
2632 drw 01

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

2532 drw 02

PIN DESCRIPTION

Pin Names	Description
CP	Clock Pulse Input (Active Edge Rising)
DS0	Serial Data Input for Right Shift
DS7	Serial Data Input for Left Shift
S0, S1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE_1}$, $\overline{OE_2}$	3-State Output Enable Inputs (Active LOW)
I/O0–I/O7	Parallel Data Inputs or 3-State Parallel Outputs
O0, O7	Serial Outputs

2632 tbl 01

FUNCTION TABLE[1]

Inputs				Response
$\overline{MR}$	S1	S0	CP	
L	X	X	X	Asynchronous Reset Q0–Q7 = LOW
H	H	H	↑	Parallel Load; I/On → Qn
H	L	H	↑	Shift Right; DS0 → Q0, Q0 → Q1, etc.
H	H	L	↑	Shift Left; DS7 → Q7, Q7→ Q6, etc.
H	L	L	X	Hold

NOTE: 2632 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
VTERM[3]	Terminal Voltage with Respect to GND	–0.5 to VCC	–0.5 to VCC	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

NOTES: 2632 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5 unless otherwise noted.
2. Inputs and Vcc terminals.
3. Outputs and I/O terminals.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
CI/O	I/O Capacitance	VOUT = 0V	8	12	pF

NOTE: 2632 tbl 04

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V	Except I/O Pins	—	—	5	µA
			I/O Pins	—	—	15	
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V	Except I/O Pins	—	—	–5	µA
			I/O Pins	—	—	–15	
I_I	Input HIGH Current	V_{CC} = Max., V_I = Vcc (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.,[3] V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH}= –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2632 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE_1}$ = $\overline{OE_2}$ = GND $\overline{MR}$ = V_{CC} S_0 = S_1 = V_{CC} DS_0 = DS_1 = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE_1}$ = $\overline{OE_2}$ = GND $\overline{MR}$ = V_{CC} S_0 = S_1 = V_{CC} DS_0 = DS_7 = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE_1}$ = $\overline{OE_2}$ = GND $\overline{MR}$ = V_{CC} S_0 = S_1 = V_{CC} DS_0 = DS_7 = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

2632 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT299T				IDT54/74FCT299AT				IDT54/74FCT299CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	14.0	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/On		2.0	12.0	2.0	12.0	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7		2.0	10.0	2.0	10.5	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/On		2.0	15.0	2.0	15.0	2.0	8.7	2.0	11.5	2.0	6.5	2.0	7.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$n to I/On		1.5	11.0	1.5	15.0	1.5	6.5	1.5	7.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$n to I/On		1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	1.5	6.0	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW S_0 or S_1 to CP		7.5	—	7.5	—	3.5	—	4.0	—	3.5	—	4.0	—	ns
t_{SU}	Set-up Time HIGH or LOW I/On, DS_0 or DS_7 to CP		5.5	—	5.5	—	4.0	—	4.5	—	4.0	—	4.5	—	ns
t_H	Hold Time HIGH or LOW S_0 or S_1 to CP		1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
t_H	Hold Time HIGH or LOW I/On, DS_0 or DS_7 to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns
t_W	$\overline{MR}$ Pulse Width LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns
t_{REM}	Recovery Time		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum units are guaranteed but not tested on Propagation Delays.

2619 tbl 07

6

Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSPARENT LATCHES

IDT54/74FCT373T/AT/CT/DT
IDT54/74FCT533T/AT/CT
IDT54/74FCT573T/AT/CT/DT

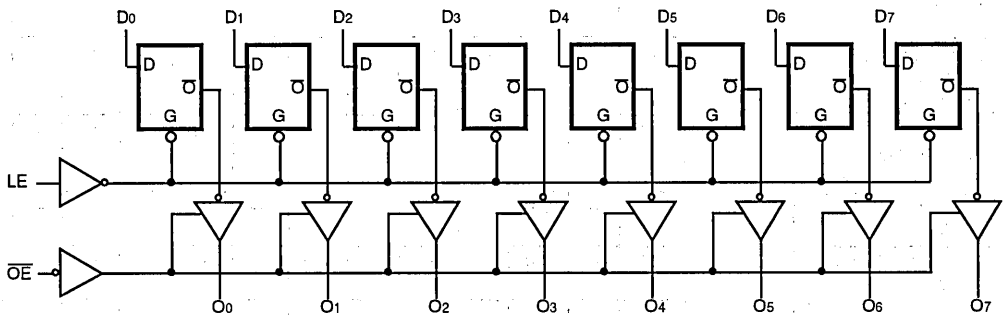
FEATURES:

- Fastest CMOS logic family available
- Std., A, C, and D speed grades with 3.8ns t_{PD}
- Available in DIP, SOIC, SSOP, CERPACK and LCC packages
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- Octal transparent latch with 3-state output control
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

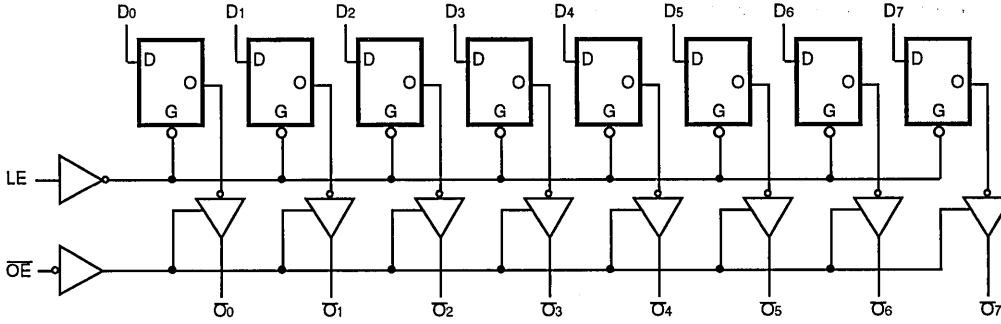
The IDT54/74FCT373T/AT/CT/DT, IDT54/74FCT533T/AT/CT and IDT54/74FCT573T/AT/CT/DT are octal transparent latches built using advanced CEMOS™, a dual metal CMOS technology. These octal latches have 3-state outputs and are intended for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high-impedance state.

FUNCTIONAL BLOCK DIAGRAM IDT54/74FCT373T AND IDT54/74FCT573T



2564 cnv* 01

FUNCTIONAL BLOCK DIAGRAM IDT54/74FCT533T

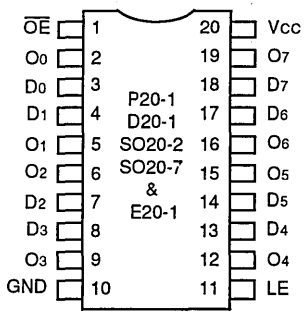


2564 cnv* 02

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is trademark of National Semiconductor Co.

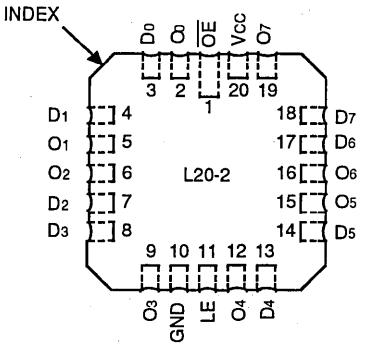
PIN CONFIGURATIONS

IDT54/74FCT373T



2564 cnv* 03

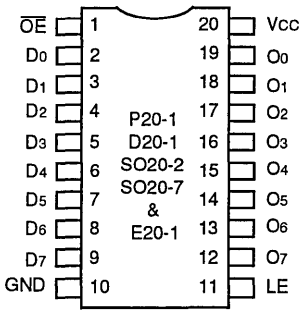
DIP/SOIC/SSOP/CERPACK
TOP VIEW



2564 cnv* 04

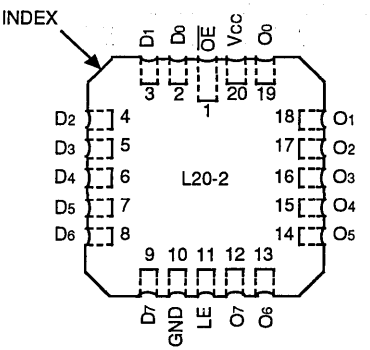
LCC
TOP VIEW

IDT54/74FCT573T



2564 cnv* 05

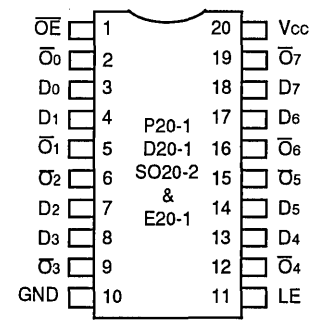
DIP/SOIC/SSOP/CERPACK
TOP VIEW



2564 cnv* 06

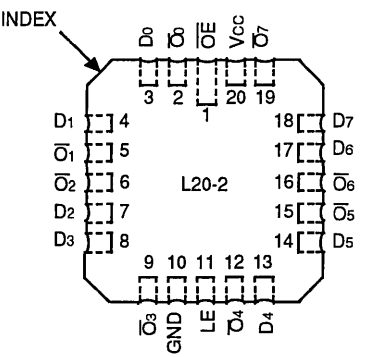
LCC
TOP VIEW

IDT54/74FCT533T



2564 cnv* 07

DIP/SOIC/CERPACK
TOP VIEW



2564 cnv* 08

LCC
TOP VIEW

6

FUNCTION TABLE (FCT533)[1]

Inputs			Outputs
D_N	LE	$\overline{OE}$	$\overline{O}_N$
H	H	L	L
L	H	L	H
X	X	H	Z

2564 tbl 05

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

FUNCTION TABLE (FCT373 and FCT573)[1]

Inputs			Outputs
D_N	LE	$\overline{OE}$	O_N
H	H	L	H
L	H	L	L
X	X	H	Z

2564 tbl 06

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
D_N	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
O_N	3-State Outputs
$\overline{O}_N$	Complementary 3-State Outputs

2564 tbl 07

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2564 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2564 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	–10	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES: 2564 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
		50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	6.5[5]	
		50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2564 tbl 04

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT373T AND FCT573T

Symbol	Parameter	Conditions[1]	FCT373T/573T				FCT373AT/573AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Dn to On	CL = 50pF RL = 500Ω	1.5	8.0	1.5	8.5	1.5	5.2	1.5	5.6	ns
tPLH tPHL	Propagation Delay LE to On		2.0	13.0	2.0	15.0	2.0	8.5	2.0	9.8	ns
tPZH tPZL	Output Enable Time		1.5	12.0	1.5	13.5	1.5	6.5	1.5	7.5	ns
tPHZ tPLZ	Output Disable Time		1.5	7.5	1.5	10.0	1.5	5.5	1.5	6.5	ns
tSU	Set-up Time HIGH or LOW, Dn to LE		2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, Dn to LE		1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	LE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	ns

2564 tbl 08

Symbol	Parameter	Conditions[1]	FCT373CT/573CT				FCT373DT/573DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Dn to On	CL = 50pF RL = 500Ω	1.5	4.2	1.5	5.1	1.5	3.8	—	—	ns
tPLH tPHL	Propagation Delay LE to On		2.0	5.5	2.0	8.0	2.0	4.0	—	—	ns
tPZH tPZL	Output Enable Time		1.5	5.5	1.5	6.3	1.5	4.8	—	—	ns
tPHZ tPLZ	Output Disable Time		1.5	5.0	1.5	5.9	1.5	4.0	—	—	ns
tSU	Set-up Time HIGH or LOW, Dn to LE		2.0	—	2.0	—	1.5	—	—	—	ns
tH	Hold Time HIGH or LOW, Dn to LE		1.5	—	1.5	—	1.0	—	—	—	ns
tW	LE Pulse Width HIGH[3]		5.0	—	6.0	—	3.0	—	—	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2564 tbl 09

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT533T

			FCT533T				FCT533AT				FCT533CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Conditions[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_N to $\overline{O}_N$	C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	12.0	1.5	5.2	1.5	5.6	1.5	4.2	1.5	5.1	ns
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_N$		2.0	13.0	2.0	14.0	2.0	8.5	2.0	9.8	2.0	5.5	2.0	8.0	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	11.0	1.5	12.5	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	1.5	8.5	1.5	5.5	1.5	6.5	1.5	5.0	1.5	5.9	ns
t_{SU}	Set-up Time HIGH or LOW, D_N to LE		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, D_N to LE		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	LE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2564 tbl 10

Integrated Device Technology, Inc.

FAST CMOS OCTAL D REGISTERS (3-STATE)

IDT54/74FCT374T/AT/CT/DT
IDT54/74FCT534T/AT/CT
IDT54/74FCT574T/AT/CT/DT

FEATURES

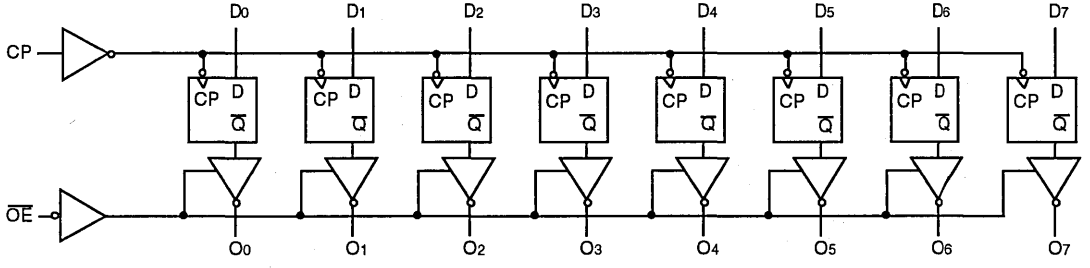
- Fastest CMOS logic family available
- Std., A, C, and D speed grades with 4.2ns t_{PD}
- Available in DIP, SOIC, SSOP, CERPACK and LCC packages
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- Edge triggered master/slave, D-type flip-flops
- Buffered common clock and buffered common three-state control
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Meets or exceeds JEDEC Standard 18 specifications

DESCRIPTION

The IDT54/74FCT374T/AT/CT/DT, IDT54/74FCT534T/AT/CT and IDT54/74FCT574T/AT/CT/DT are 8-bit registers built using advanced CEMOS™, a dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered 3-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the high-impedance state.

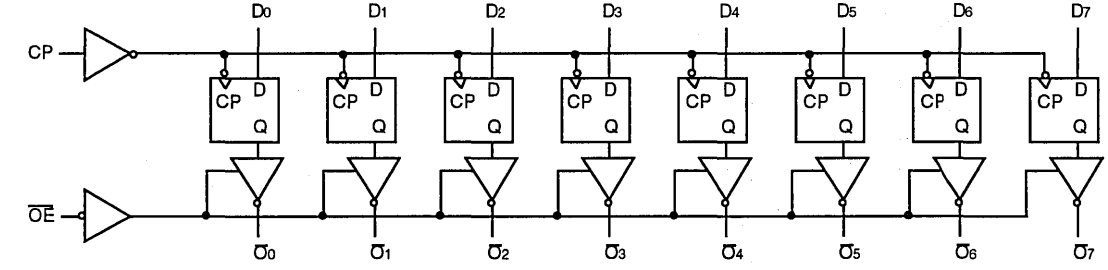
Input data meeting the set-up and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

FUNCTIONAL BLOCK DIAGRAM IDT54/74FCT374T AND IDT54/74FCT574T



2569 drw 01

FUNCTIONAL BLOCK DIAGRAM IDT54/74FCT534T

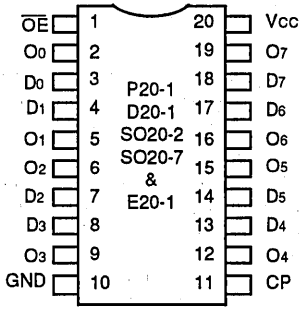


2569 drw 02

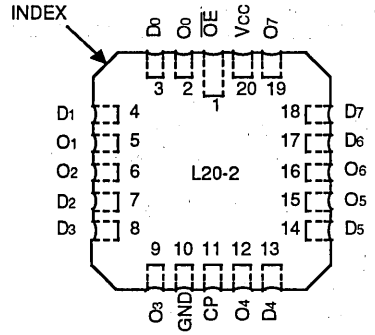
CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS

IDT54/74FCT374T



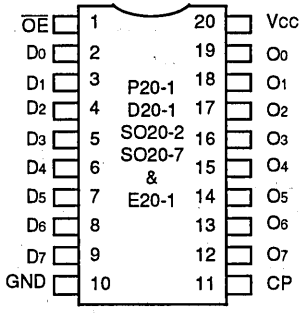
DIP/SOIC/SSOP/CERPACK
TOP VIEW



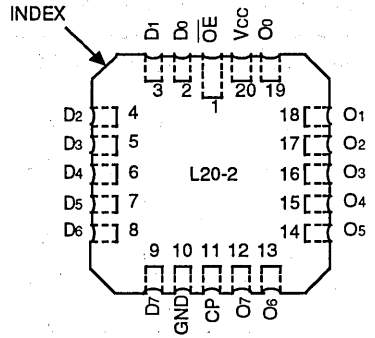
2569 drw 03

LCC
TOP VIEW

IDT54/74FCT574T



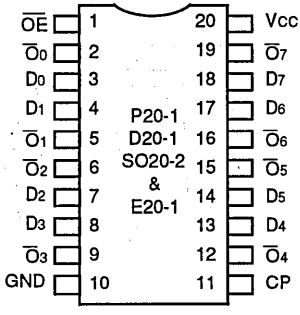
DIP/SOIC/SSOP/CERPACK
TOP VIEW



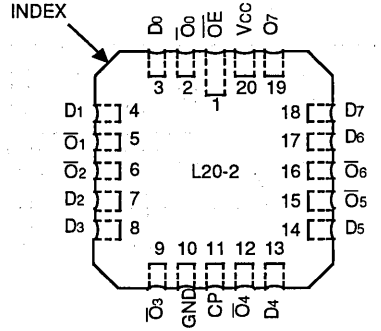
2569 drw 04

LCC
TOP VIEW

IDT54/74FCT534T



DIP/SOIC/CERPACK
TOP VIEW



2569 drw 05

LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
D_N	D flip-flop data inputs
CP	Clock Pulse for the register. Enters data on LOW-to-HIGH transition.
O_N	3-state outputs, (true)
$\overline{O}_N$	3-state outputs, (inverted)
$\overline{OE}$	Active LOW 3-state Output Enable input

2569 tbl 06

FUNCTION TABLE[1]

	Inputs			FCT534		FCT374/574	
				Outputs	Internal	Outputs	Internal
Function	$\overline{OE}$	CP	D_N	$\overline{O}_N$	Q_N	O_N	$\overline{Q}_N$
HI-Z	H	L	X	Z	NC	Z	NC
	H	H	X	Z	NC	Z	NC
LOAD REGISTER	L	↑	L	H	L	L	H
	L	↑	H	L	H	H	L
	H	↑	L	Z	L	Z	H
	H	↑	H	Z	H	Z	L

NOTE: 2569 tbl 05

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   NC = No Change
   ↑ = LOW-to-HIGH transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2569 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2569 tbl 02

1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	–10	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2569 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
		$\overline{OE}$ = GND f_i = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.0	7.8[5]	
		$\overline{OE}$ = GND Eight Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

2569 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions[1]	FCT374T/534T/574T				FCT374AT/534AT/574AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_N[3]	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	11.0	2.0	6.5	2.0	7.2	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	12.5	1.5	14.0	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	8.0	1.5	8.0	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW, D_N to CP		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, D_N to CP		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	ns

2569 tbl 07

Symbol	Parameter	Conditions[1]	FCT374CT/534CT/574CT				FCT374DT/574DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_N[3]	C_L = 50pF R_L = 500Ω	2.0	5.2	2.0	6.2	2.0	4.2	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	5.5	1.5	6.2	1.5	4.8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	5.0	1.5	5.7	1.5	4.0	—	—	ns
t_{SU}	Set-up Time HIGH or LOW, D_N to CP		2.0	—	2.0	—	2.0	—	—	—	ns
t_H	Hold Time HIGH or LOW, D_N to CP		1.5	—	1.5	—	1.0	—	—	—	ns
t_W	CP Pulse Width HIGH or LOW[4]		5.0	—	6.0	—	3.0	—	—	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. O_N for FCT374 and FCT574, $\overline{O}_N$ for FCT534.
4. This parameter is guaranteed but not tested.

2569 tbl 08

Integrated Device Technology, Inc.

FAST CMOS OCTAL D FLIP-FLOP WITH CLOCK ENABLE

IDT54/74FCT377T
IDT54/74FCT377AT
IDT54/74FCT377CT

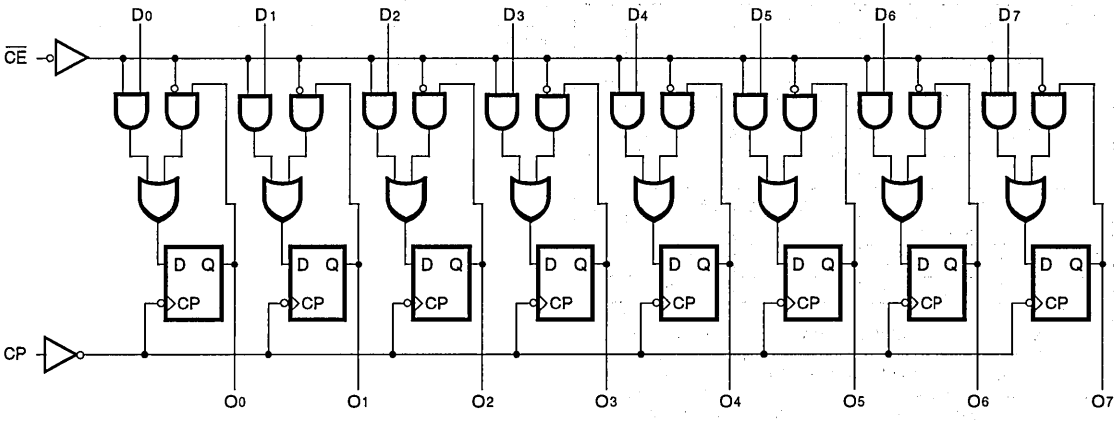
FEATURES:

- IDT54/74FCT377T equivalent to FAST™ speed
- **IDT54/74FCT377AT 25% faster than FAST**
- **IDT54/74FCT377CT 40% faster than FAST**
- True TTL input and output compatibility:
  - — V_{OH} = 3.3V (typ.)
  - — V_{OL} = 0.3V (typ.)
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- Octal D flip-flop with clock enable
- Meets or exceeds JEDEC Standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

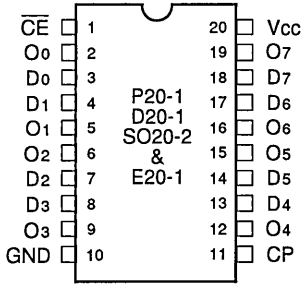
The IDT54/74FCT377T/AT/CT are octal D flip-flops built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT377T/AT/CT have eight edge-triggered, D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is LOW. The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The $\overline{CE}$ input must be stable only one set-up time prior to the LOW-to-HIGH transition for predictable operation.

FUNCTIONAL BLOCK DIAGRAM

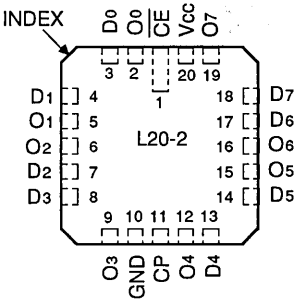


2630 drw 02

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2630 drw 01

LCC
TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
$D_0 - D_7$	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
$O_0 - O_7$	Data Outputs
CP	Clock Pulse Input

2630 tbl 05

FUNCTION TABLE[1]

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D	O
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (Do Nothing)	↑	h	X	No Change
	H	H	X	No Change

2630 tbl 06

NOTE:
1. H = HIGH Voltage Level
   h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
   L = LOW Voltage Level
   l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
   X = Immaterial
   ↑ = LOW-to-HIGH Clock Transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2630 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2630 tbl 02
1. This parameter is guaranteed but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES:
2630 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{CE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
		$\overline{CE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.0	7.8[5]	
		$\overline{CE}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

NOTES:
2630 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FCT377T				IDT54/74FCT377AT				IDT54/74FCT377CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay CP to O_n	C_L = 50pF R_L = 500Ω	2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	5.2	2.0	5.5	ns
t_{SU}	Set-up Time HIGH or LOW D_n to CP		2.5	—	3.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW D_n to CP		2.0	—	2.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{SU}	Set-up Time HIGH or LOW $\overline{CE}$ to CP		4.0	—	4.0	—	3.5	—	3.5	—	3.5	—	3.5	—	ns
t_H	Hold Time HIGH or LOW $\overline{CE}$ to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	Clock Pulse Width, HIGH or LOW		7.0	—	7.0	—	6.0	—	7.0	—	6.0	—	7.0	—	ns

NOTES:
2630 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

Integrated Device Technology, Inc.

FAST CMOS QUAD DUAL-PORT REGISTER

IDT54/74FCT399T
IDT54/74FCT399AT
IDT54/74FCT399CT

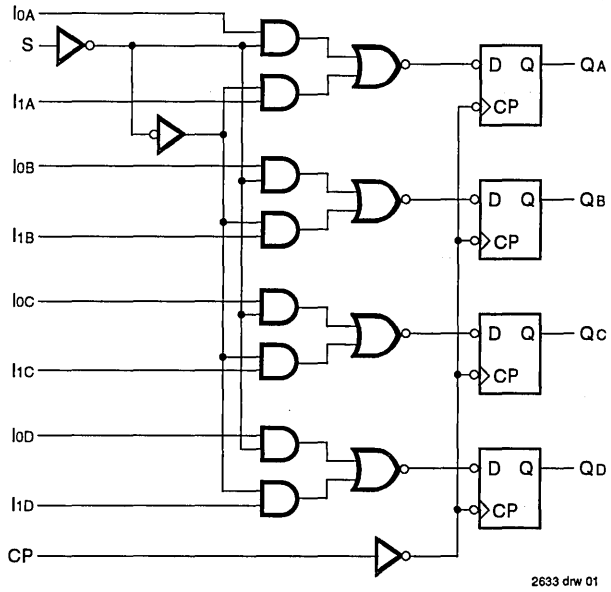
FEATURES:

- IDT54/74FCT399T equivalent to FAST™ speed
- **IDT54/74FCT399AT 30% faster than FAST**
- **IDT54/74FCT399CT 45% faster than FAST**
- Equivalent to FAST pinout/function and output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT399T/AT/CT are high-speed quad dual-port registers. They select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0X}, I_{1X}) and Select input (S) must be stable only one set-up time prior to, and hold time after, the LOW-to-HIGH transition of the Clock input for predictable operation.

FUNCTIONAL BLOCK DIAGRAM



6

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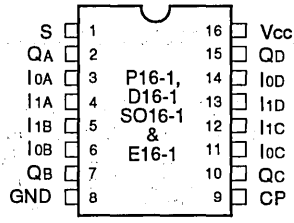
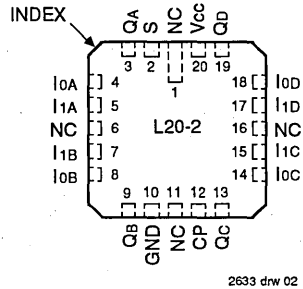
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
S	Common Select Input
CP	Clock Pulse Input (Active Rising Edge)
$I_{0A} - I_{0D}$	Data Inputs from Source 0
$I_{1A} - I_{1D}$	Data Inputs from Source 1
$Q_A - Q_D$	Register True Outputs

2633 tbl 05

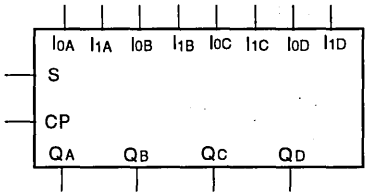
FUNCTION TABLE[1]

Inputs			Outputs
S	I_0	I_1	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

2633 tbl 06

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   h = HIGH Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
   l = LOW Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
   X = Immaterial

LOGIC SYMBOL



2633 drw 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2633 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals.
3. Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2633 tbl 02

1. This parameter is measured at characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = –55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	Vcc = Max.	V_I = 0.5V	—	—	–5	µA
I_I	Input HIGH Current	Vcc = Max., V_I = Vcc (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	Vcc = Max[3]., Vo = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	Vcc = Max. V_{IN} = GND or Vcc		—	0.2	1.5	mA

NOTES: 2633 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
		One Bit Toggling at f_i = 5MHz 50% Duty Cycle S = Steady State	V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.0	7.8[5]	
		Four Bits Toggling at f_i = 5MHz 50% Duty Cycle S = Steady State	V_{IN} = 3.4V V_{IN} = GND	—	5.2	12.8[5]	

NOTES:

2633 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT399T				IDT54/74FCT399AT				IDT54/74FCT399CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	C_L = 50pF R_L = 500Ω	3.0	10.0	3.0	11.5	2.5	7.0	2.5	7.5	2.5	6.1	2.5	6.6	ns
t_{SU}	Set-up Time HIGH or LOW I_n to CP		4.0	—	4.5	—	3.5	—	4.0	—	3.5	—	4.0	—	ns
t_H	Hold Time HIGH or LOW I_n to CP		1.0	—	1.5	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
t_{SU}	Set-up Time HIGH or LOW S to CP		9.0	—	9.5	—	8.5	—	9.0	—	8.5	—	9.0	—	ns
t_H	Hold Time HIGH or LOW S to CP		0	—	0	—	0	—	0	—	0	—	0	—	ns
t_W	CP Pulse Width HIGH or LOW		5.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2633 tbl 07

6

Integrated Device Technology, Inc.

FAST CMOS 8-BIT IDENTITY COMPARATOR

IDT54/74FCT521T
IDT54/74FCT521AT
IDT54/74FCT521BT
IDT54/74FCT521CT

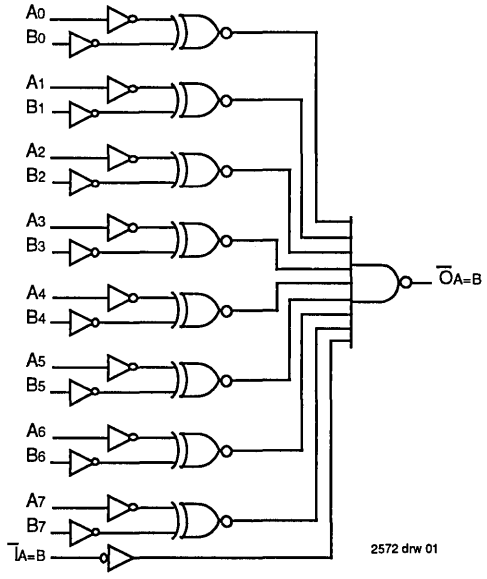
FEATURES:

- IDT54/74FCT521T equivalent to FAST™ speed
- **IDT54/74FCT521AT 35% faster than FAST**
- **IDT54/74FCT521BT 50% faster than FAST**
- **IDT54/74FCT521CT 60% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial), and 32mA (military)
- CMOS power levels (1mW typ. static)
- True TTL input and output levels
- Substantially lower input current levels than FAST (5µA max.)
- 8-bit Identitiy Comparator
- Product available in Radiation Tolerant and Radiation Enhanced versions
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT521T/AT/BT/CT are 8-bit identity comparators built using advanced CEMOS™, a dual metal CMOS technology. These devices compare two words of up to eight bits each and provide a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

FUNCTIONAL BLOCK DIAGRAM



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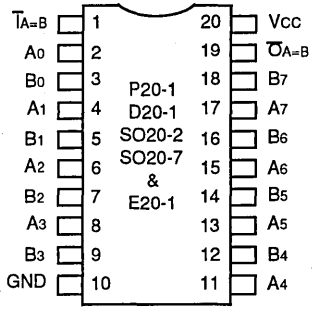
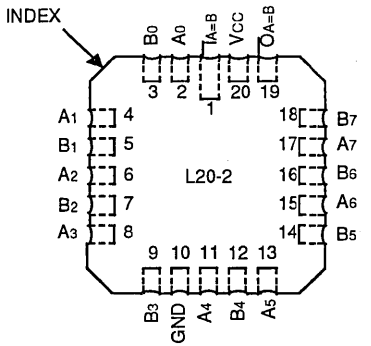
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



2572 drw 02

DIP/SOIC/SSOP/CERPACK
TOP VIEW



2572 drw 03

LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
A_0 - A_7	Word A Inputs
B_0 - B_7	Word B Inputs
$\overline{I}_{A=B}$	Expansion or Enable Input (Active LOW)
$\overline{O}_{A=B}$	Identity Output (Active LOW)

2572 tbl 05

FUNCTION TABLE(1)

Inputs		Output
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

2572 tbl 06

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   *A_0 = B_0, A_1 = B_1, A_2 = B_2, etc.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2572 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2572 tbl 02
1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES: 2572 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max. Outputs Open	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
		f_i = 10MHz One Bit Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	

NOTES: 2572 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT521T				IDT54/74FCT521AT				IDT54/74FCT521BT				IDT54/74FCT521CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay An or Bn to $\overline{O}_{A=B}$	CL = 50pF RL = 500Ω	1.5	11.0	1.5	15.0	1.5	7.2	1.5	9.5	1.5	5.5	1.5	7.3	1.5	4.5	1.5	5.1	ns
tPLH tPHL	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$		1.5	10.0	1.5	9.0	1.5	6.0	1.5	7.8	1.5	4.6	1.5	6.0	1.5	4.1	1.5	4.5	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2572 tbl 07

6

Integrated Device Technology, Inc.

FAST CMOS OCTAL LATCHED TRANSCEIVER

IDT54/74FCT543T
IDT54/74FCT543AT
IDT54/74FCT543CT
IDT54/74FCT543DT

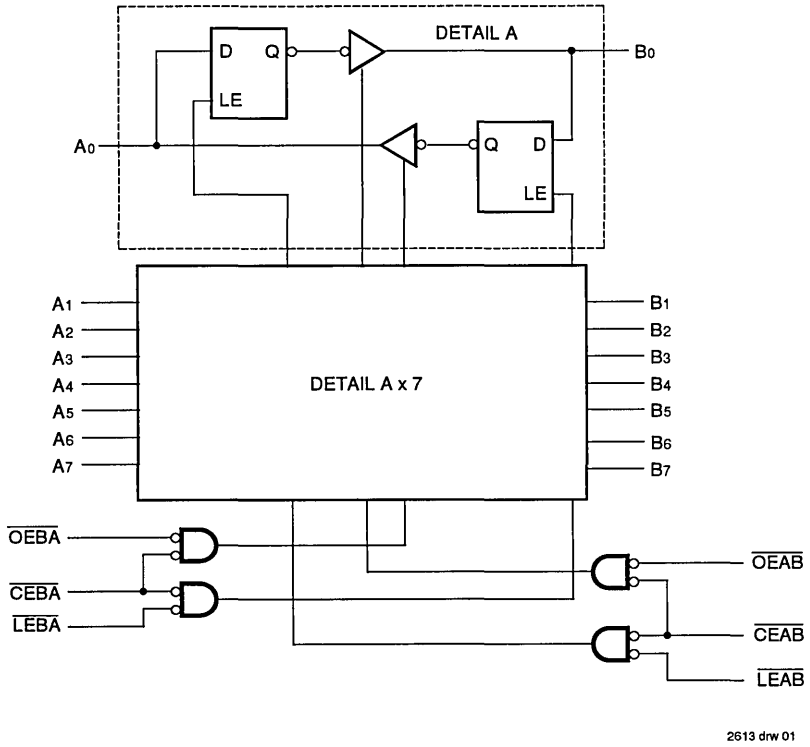
FEATURES:

- Fastest CMOS logic family available
- Std., A, C and D speed grades with 4.4ns t_{PD}
- Available in DIP, SOIC, SSOP, CERPACK and LCC packages
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial), 48mA (military)
- Separate controls for data flow in each direction
- Back-to-back latches for storage
- CMOS power levels (1mW typ. static)
- Substantially lower input current levels than FAST (5μA max.)
- True TTL input and output levels
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT543T/AT/CT/DT are non-inverting octal transceivers built using advanced CEMOS™, a dual metal CMOS technology. These devices contain two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A_0–A_7 or to take data from B_0–B_7, as indicated in the Function Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

FUNCTIONAL BLOCK DIAGRAM



2613 drw 01

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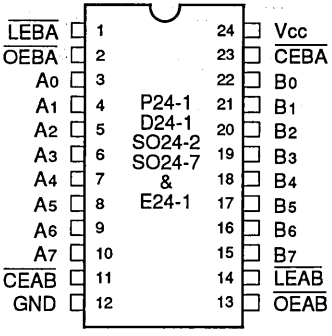
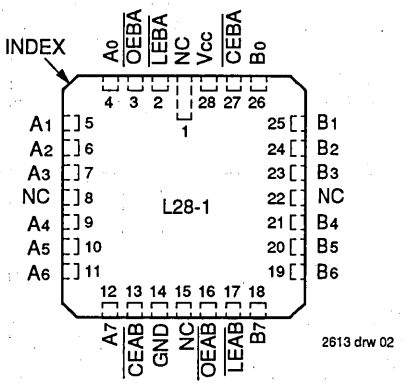
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/SSOP/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0–A_7	A-to-B Data Inputs or B-to-A 3-State Outputs
B_0–B_7	B-to-A Data Inputs or A-to-B 3-State Outputs

2613 tbl 02

FUNCTION TABLE[1, 2]

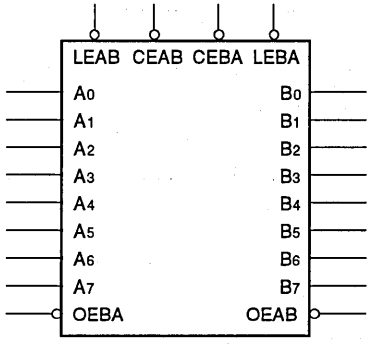
For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B	B_0–B_7
H	—	—	Storing	High Z
—	H	—	Storing	—
—	—	H	—	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

2613 tbl 01

NOTES:
1. * Before $\overline{LEAB}$ LOW-to-HIGH Transition
   H = HIGH Voltage Level
   L = LOW Voltage Level
   — = Don't Care or Irrelevant
2. A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.

LOGIC SYMBOL



2613 drw 03

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2613 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Inputs and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2613 tbl 04

1. This parameter is guaranteed by characterization and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	Except I/O Pins	—	—	5	µA
		V_I = 2.7V	I/O Pins	—	—	15	
I_{IL}	Input LOW Current	V_{CC} = Max.	Except I/O Pins	—	—	–5	µA
		V_I = 0.5V	I/O Pins	—	—	–15	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –6mA MIL.	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA COM'L.				
			I_{OH} = –12mA MIL.	2.0	3.0	—	V
			I_{OH} = –15mA COM'L.				
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 48mA MIL.(4)	—	0.3	0.55	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA COM'L.				
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES: 2613 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz ($\overline{LEAB}$) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz ($\overline{LEAB}$) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} Eight Bits Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	7.0	12.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	9.2	21.8[5]	

2613 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT543T				IDT54/74FCT543AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Transparant Mode An to Bn or Bn to An	CL = 50pF RL = 500Ω	2.5	8.5	2.5	10.0	2.5	6.5	2.5	7.5	ns
tPLH tPHL	Propagation Delay $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn		2.5	12.5	2.5	14.0	2.5	8.0	2.5	9.0	ns
tPZH tPZL	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		2.0	12.0	2.0	14.0	2.0	9.0	2.0	10.0	ns
tPHZ tPLZ	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		2.0	9.0	2.0	13.0	2.0	7.5	2.0	8.5	ns
tSU	Set-up Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$		3.0	—	3.0	—	2.0	—	2.0	—	ns
tH	Hold Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$		2.0	—	2.0	—	2.0	—	2.0	—	ns
tW	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW		5.0	—	5.0	—	5.0	—	5.0	—	ns

2513 tbl 07

Symbol	Parameter	Condition[1]	IDT54/74FCT543CT				IDT54/74FCT543DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Transparant Mode An to Bn or Bn to An	CL = 50pF RL = 500Ω	2.5	5.3	2.5	6.1	2.5	4.4	—	—	ns
tPLH tPHL	Propagation Delay $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn		2.5	7.0	2.5	8.0	2.5	5.0	—	—	ns
tPZH tPZL	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		2.0	8.0	2.0	9.0	2.0	5.4	—	—	ns
tPHZ tPLZ	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		2.0	6.5	2.0	7.5	2.0	4.3	—	—	ns
tSU	Set-up Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$		2.0	—	2.0	—	1.5	—	—	—	ns
tH	Hold Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$		2.0	—	2.0	—	1.5	—	—	—	ns
tW	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW		5.0	—	5.0	—	3.0	—	—	—	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2513 tbl 08

Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSCEIVER/ REGISTERS (3-STATE)

IDT54/74FCT646T/AT/CT/DT
IDT54/74FCT648T/AT/CT
IDT54/74FCT651T/AT/CT
IDT54/74FCT652T/AT/CT/DT

FEATURES:

- Fastest CMOS logic family available
- Std., A, C and D speed grades with 4.4ns t_{PD}
- Available in DIP, SOIC, SSOP, CERPACK and LCC packages
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of true and inverting data paths
- I_{OL} = 64mA (commercial), 48mA (military)
- CMOS power levels
- TTL input and output level compatible
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

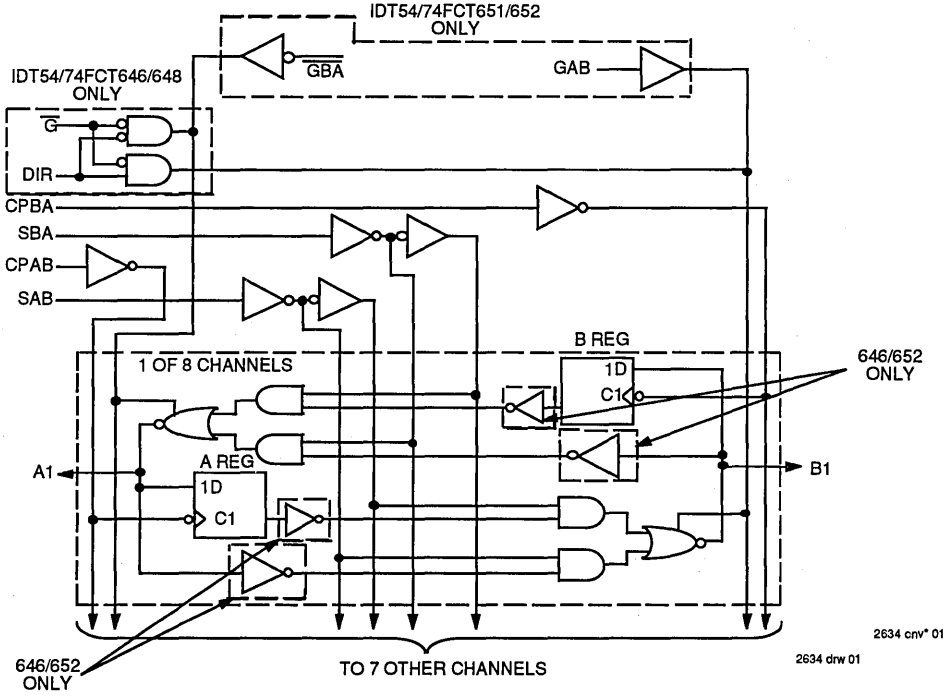
The IDT54/74FCT646/652T/AT/CT/DT and IDT54/74FCT 648/651T/AT/CT consist of a bus transceiver with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

The '651/652 utilize GAB and $\overline{GBA}$ signals to control the transceiver functions. The '646/648 utilize the enable control ($\overline{G}$) and direction (DIR) pins to control the transceiver functions.

SAB and SBA control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data and a HIGH selects stored data.

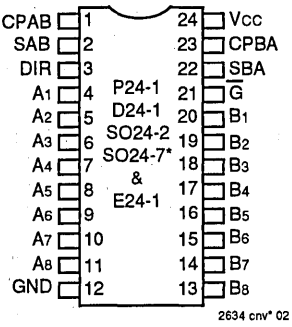
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

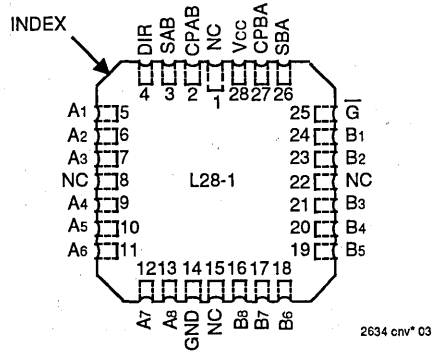
PIN CONFIGURATIONS



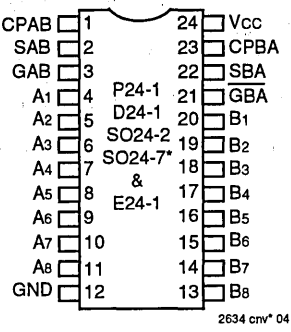
DIP/SOIC/SSOP/CERPACK
TOP VIEW

* FCT646T/AT/CT/DT only

FCT646/648T



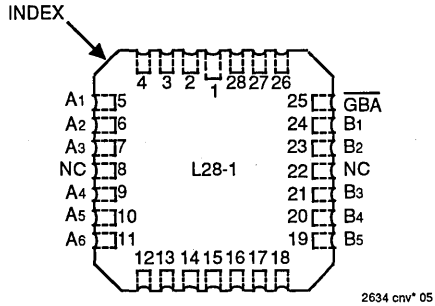
LCC
TOP VIEW



DIP/SOIC/SSOP/CERPACK
TOP VIEW

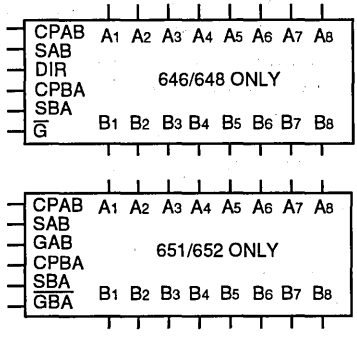
* FCT652T/AT/CT/DT only

FCT651/652T



LCC
TOP VIEW

LOGIC SYMBOLS



PIN DESCRIPTION

Pin Names	Description
A_1 - A_8	Data Register A Inputs Data Register B Outputs
B_1 - B_8	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\overline{G}$	Output Enable Inputs (646/648)
GAB, $\overline{GBA}$	Output Enable Inputs (651/652)

2634 tbl 01

FUNCTION TABLE FCT646/648T

Inputs						Data I/O(1)		Operation or Function	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_1 - A_8	B_1 - B_8	IDT54/74FCT646T	IDT54/74FCT648T
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

2634 tbl 02

FUNCTION TABLE FCT651/652T

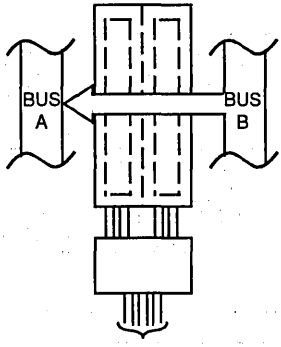
Inputs						Data I/O		Operation or Function	
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_1 - A_8	B_1 - B_8	IDT54/74FCT651T	IDT54/74FCT652T
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified(1)	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X(2)	X	Input	Output	Store A in Both Registers(3)	Store A in Both Registers
L	X	H or L	↑	X	X	Unspecified(1)	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X(2)	Output	Input	Store B in Both Registers(4)	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

2634 tbl 03

NOTES:

1. The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.
   H = HIGH, L = LOW, X = Don't Care, ≠ = LOW-to-HIGH transition.
3. $\overline{A}$ in B Register.
4. $\overline{B}$ in A Register.

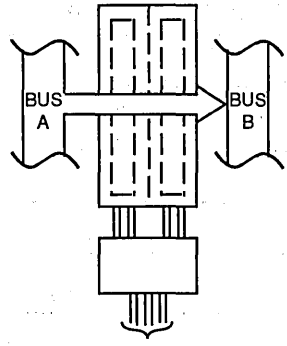
6



651/652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L
646/648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO A

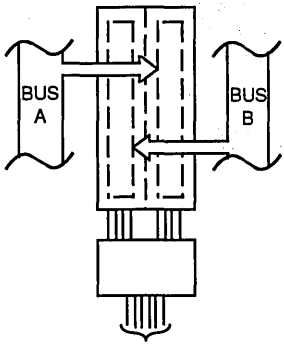
2634 cnv* 07



651/652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	H	H	X	X	L	X
646/648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	X	X	L	X

REAL-TIME TRANSFER BUS A TO B

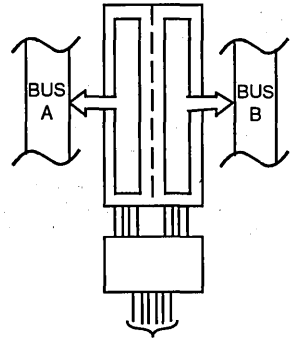
2634 cnv* 08



651/652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	X	H	↑	X	X	X
	L	X	X	↑	X	X
	L	H	↑	↑	X	X
646/648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	↑	X	X	X
	L	L	X	↑	X	X
	X	H	↑	↑	X	X

STORAGE FROM A AND/OR B

2634 cnv* 09



651/652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	H	L	H or L	H or L	H	H
646/648[1]	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	H or L	X	H
	H	L	H or L	X	H	X

TRANSFER STORES DATA TO A AND/OR B

2634 cnv* 10

NOTE:
1. 646/648 cannot transfer data to A bus and B bus simultaneously.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2634 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed VCC by +0.5V unless otherwise noted.
2. Input and VCC terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2634 tbl 05

1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	—	—	–5	µA
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = 2.7V	—	—	15	µA
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	—	—	–15	µA
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max[3], V_O = GND		–60	–120	–225	mA
I_{OFF}	Power Down Disable	V_{CC} = GND V_O = 4.5V		—	—	100	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL.	—	0.3	0.55	V
			I_{OL} = 64mA COM'L.[4]	—	0.3	0.55	
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2634 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These are maximum I_{OL} values per output for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{GAB}$ = $\overline{GBA}$ = GND or $\overline{G}$ = DIR = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{GAB}$ = $\overline{GBA}$ = GND or	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
		$\overline{G}$ = DIR = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{GAB}$ = $\overline{GBA}$ = GND or	V_{IN} = V_{CC} V_{IN} = GND	—	7.0	12.8[5]	
		$\overline{G}$ = DIR = GND Eight Bits Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	9.2	21.8[5]	

2634 tbl 07

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Outputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	646T/648T/651T/652T				646AT/648AT/651AT/652AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
t_{PZH} t_{PZL}	Output Enable Time, $\overline{G}$, DIR to Bus[3]		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time, $\overline{G}$, DIR to Bus[3]		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	ns
t_{SU}	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	ns
t_W	Clock Pulse Width, HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	ns

2634 tbl 08

Symbol	Parameter	Condition[1]	646CT/648CT/651CT/652CT				646DT/652DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	1.5	5.4	1.5	6.0	1.5	4.4	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time, $\overline{G}$, DIR to Bus[3]		1.5	7.8	1.5	8.9	1.5	5.0	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time, $\overline{G}$, DIR to Bus[3]		1.5	6.3	1.5	7.7	1.5	4.3	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		1.5	5.7	1.5	6.3	1.5	4.4	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Bus		1.5	6.2	1.5	7.0	1.5	5.0	—	—	ns
t_{SU}	Set-up Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	—	—	ns
t_H	Hold Time HIGH or LOW Bus to Clock		1.5	—	1.5	—	1.0	—	—	—	ns
t_W	Clock Pulse Width, HIGH or LOW[4]		5.0	—	5.0	—	3.0	—	—	—	ns

2634 tbl 09

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. GAB, $\overline{GBA}$ to Bus for 651, 652.
4. This parameter is guaranteed but not tested.

Integrated Device Technology, Inc.

FAST CMOS OCTAL BUS TRANSCEIVERS (3-STATE)

IDT54/74FCT620T/AT/CT
IDT54/74FCT623T/AT/CT

FEATURES

- IDT54/74FCT620T/623T equivalent to FAST™ speed
- **IDT54/74FCT620AT/623AT 25% faster than FAST**
- **IDT54/74FCT620CT/623CT 45% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (1mW typ. static)
- CMOS devices with TRUE TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- Substantially lower input current levels than FAST (5μA max.)
- Power Down Disable feature
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION

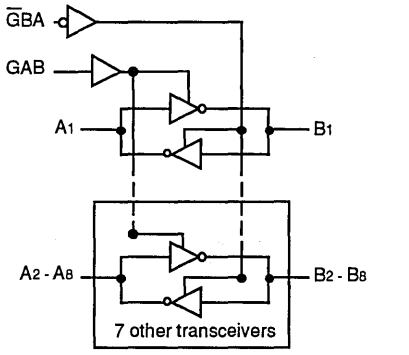
The IDT54/74FCT623T/AT/CT is a non-inverting octal transceiver with 3-state bus-driving outputs in both the send and receive directions. The B bus outputs are capable of sinking 64mA and sourcing up to 15mA, providing very good capacitive drive characteristics.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

One important feature of the IDTFCT620T/AT/CT and IDTFCT623T/AT/CT is the Power Down Disable capability. When the GAB and $\overline{GBA}$ inputs are conditioned to put the device in high-Z state, the I/O ports will maintain high impedance during power supply ramps and when Vcc = 0V. This is a desirable feature in back-plane applications where it may be necessary to perform "hot" insertion and disinsertion of cards for on-line maintenance. It is also a benefit in systems with multiple redundancy where one or more redundant cards may be powered-off.

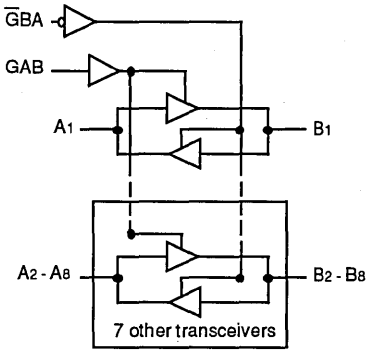
The IDTFCT620T/AT/CT is the inverting option of the IDTFCT623T/AT/CT.

FUNCTIONAL BLOCK DIAGRAMS



FCT620T/AT/CT

2563 cnv* 01



FCT623T/AT/CT

2563 cnv* 02

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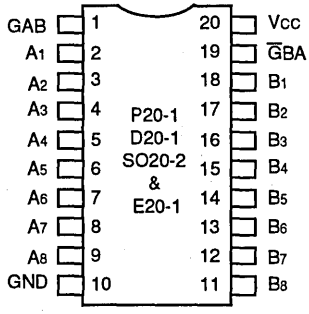
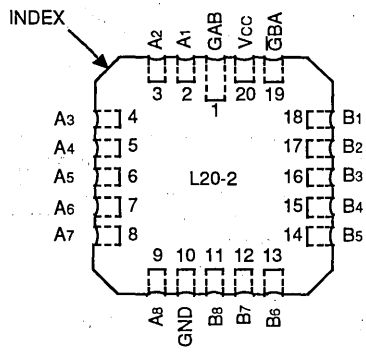
CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW

2563 cnv* 03



LCC
TOP VIEW

2563 cnv* 04

DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
$\overline{GBA}$, GAB	Enable Inputs
A_1 - A_8	A Bus Inputs or 3-State Outputs
B_1 - B_8	B Bus Inputs or 3-State Outputs

2563 tbl 01

FUNCTION TABLE[1]

Enable Inputs		Outputs	
$\overline{GBA}$	GAB	FCT620	FCT623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Z	Z
L	H	$\overline{B}$ data to A bus $\overline{A}$ data to B bus	B data to A bus A data to B bus

NOTES:
1. H = HIGH Voltage Level
2. L = LOW Volage Level
3. Z = High-Impedance (OFF) state

2563 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

2563 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

2563 tbl 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	Except I/O Pins	—	—	5	µA
		V_I = 2.7V	I/O Pins	—	—	15	
I_{IL}	Input LOW Current	V_{CC} = Max.	Except I/O Pins	—	—	–5	µA
		V_I = 0.5V	I/O Pins	—	—	–15	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
I_{OFF}	Power Down Disable	V_{CC} = GND, V_O = 4.5V		—	—	100	µA
V_{OH}	Output HIGH Voltage (A and B Bus)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage (A Bus)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.[4] I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_{OL}	Output LOW Voltage (B Bus)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL.[4] I_{OL} = 64mA COM'L.	—	0.3	0.55	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES:
2563 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{GBA}$ = GAB = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $\overline{GBA}$ = GAB = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $\overline{GBA}$ = GAB = GND Eight Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2563 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT620T/AT/CT

Symbol	Parameter	Condition[1]	54/74FCT620T				54/74FCT620AT				54/74FCT620CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay An to Bn	CL = 50pF RL = 500Ω	1.5	7.0	1.5	8.0	1.5	5.2	1.5	6.0	1.5	4.5	1.5	5.1	ns
tPLH tPHL	Propagation Delay Bn to An		1.5	7.0	1.5	8.0	1.5	5.2	1.5	6.0	1.5	4.5	1.5	5.1	ns
tPZH tPZL	Output Enable Time $\overline{GBA}$ to An		1.5	9.0	1.5	10.0	1.5	7.0	1.5	8.0	1.5	6.1	1.5	6.9	ns
tPHZ tPLZ	Output Disable Time $\overline{GBA}$ to An		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns
tPZH tPZL	Output Enable Time GAB to Bn		1.5	9.0	1.5	10.5	1.5	7.0	1.5	8.0	1.5	6.1	1.5	6.9	ns
tPHZ tPLZ	Output Disable Time GAB to Bn		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns

2563 tbl 07

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT623T/AT/CT

Symbol	Parameter	Condition[1]	54/74FCT623T				54/74FCT623AT				54/74FCT623CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay An to Bn	CL = 50pF RL = 500Ω	1.5	7.5	1.5	9.0	1.5	5.5	1.5	6.3	1.5	4.8	1.5	5.4	ns
tPLH tPHL	Propagation Delay Bn to An		1.5	7.5	1.5	9.5	1.5	5.5	1.5	6.3	1.5	4.8	1.5	5.4	ns
tPZH tPZL	Output Enable Time $\overline{GBA}$ to An		1.5	9.0	1.5	10.0	1.5	7.0	1.5	8.0	1.5	6.1	1.5	6.9	ns
tPHZ tPLZ	Output Disable Time $\overline{GBA}$ to An		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns
tPZH tPZL	Output Enable Time GAB to Bn		1.5	9.0	1.5	10.5	1.5	7.0	1.5	8.0	1.5	6.1	1.5	6.9	ns
tPHZ tPLZ	Output Disable Time GAB to Bn		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns

NOTES:

2563 tbl 08

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays

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Integrated Device Technology, Inc.

FAST CMOS OCTAL BUS TRANSCEIVER (OPEN DRAIN)

IDT54/74FCT621T/AT
IDT54/74FCT622T/AT

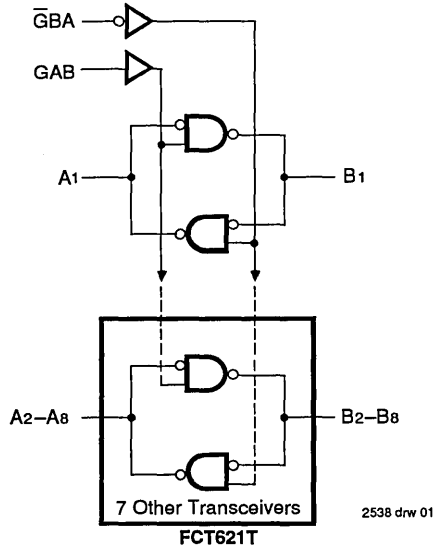
FEATURES:

- IDT54/74FCT621T/622T equivalent to FAST™ speed
- **IDT54/74FCT621AT/622AT 25% faster than FAST speed**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- Substantially lower input current levels than FAST (5µA max.)
- **Power Down Disable feature**
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT621T/AT is an octal transceiver with non-inverting Open-Drain bus compatible outputs in both send and receive directions. The B bus outputs are capable of sinking 64mA providing very good capacitive drive characteristics. These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing. The IDT54/74FCT622T/AT is the inverting option of the '621.

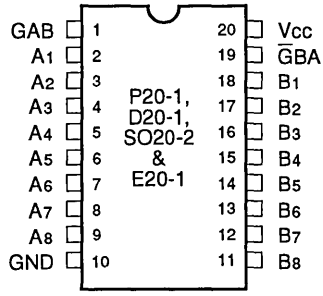
FUNCTIONAL BLOCK DIAGRAM [1]



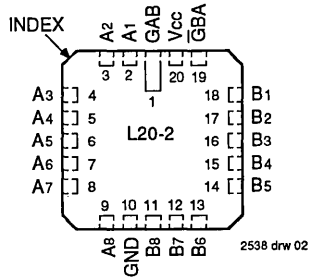
FCT621T

NOTE:
1. The FCT622T is the inverting option of FCT621T.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK TOP VIEW



LCC TOP VIEW

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FAST is a trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
$\overline{G}BA$, GAB	Enable Inputs
$A_1 - A_8$	A Inputs or Open-drain Outputs
$B_1 - B_8$	B Inputs or Open-drain Outputs

2538 tbl 05

FUNCTION TABLE[1]

Enable Inputs		Function	
$\overline{G}BA$	GAB	'FCT621T	'FCT622T
L	L	B data to A bus	$\overline{B}$ data to A bus
H	H	A data to B bus	$\overline{A}$ data to B bus
H	L	OFF	OFF
L	H	B data to A bus A data to B bus	$\overline{B}$ data to A bus $\overline{A}$ data to B bus

NOTE: 2538 tbl 06
1. H = HIGH Voltage Level.
   L = LOW Voltage Level.
   OFF = HIGH if pull-up resistor is connected to Open-Drain output.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2538 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals.
3. Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2538 tbl 04
1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max	Except I/O Pins	—	—	5	µA
		V_I = 2.7V	I/O Pins	—	—	15	
I_{IL}	Input LOW Current	V_{CC} = Max	Except I/O Pins	—	—	–5	µA
		V_I = 0.5V	I/O Pins	—	—	–15	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OFF}	Power Down Disable	V_{CC} = GND V_O = 4.5V		—	—	100	µA
I_{OH}	Output HIGH Current	V_{CC} = Max. V_{IN} = V_{IH} or V_{IL}	V_{OH} = Vcc (Max.)	—	—	20	µA
V_{OL}	Output LOW Voltage (B Bus)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL.[4] I_{OL} = 64mA COM'L.	—	0.3	0.55	V
V_{OL}	Output LOW Voltage (A Bus)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.[4] I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current[3]	V_{CC} = max., V_{IN} = GND or Vcc		—	0.2	1.5	mA

NOTES: 2538 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. This test is performed with outputs preconditioned to the LOW state. Icc with outputs preconditioned to the HIGH state is guaranteed when the outputs are forced to V_{CC} or GND.
4. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{G}BA$ = GAB = GND or V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6,7]	V_{CC} = Max. Outputs Open $\overline{G}BA$ = GAB = GND or V_{CC} One Bit Toggling at f_i =10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open $\overline{G}BA$ = GAB = GND or V_{CC} Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2538 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.
7. This test is performed with outputs tied to GND through a pull-down resistor.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE – IDT54/74FCT621T/AT

			IDT54/74FCT621T				IDT54/74FCT621AT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH}	Propagation Delay A to B	C_L = 50pF	5.5	13.0	5.5	13.5	5.5	12.0	5.5	12.5	ns
t_{PHL}		R_L = 500Ω	1.5	8.5	1.5	9.5	1.5	6.8	1.5	7.6	
t_{PLH}	Propagation Delay B to A		5.5	12.5	5.5	13.0	5.5	12.0	5.5	12.5	ns
t_{PHL}			1.5	8.0	1.5	9.0	1.5	6.4	1.5	7.2	
t_{PLH}	Propagation Delay $\overline{G}$BA to A		5.5	14.0	5.5	14.5	5.5	13.0	5.5	13.5	ns
t_{PHL}			1.5	8.5	1.5	9.5	1.5	6.8	1.5	7.6	
t_{PLH}	Propagation Delay GAB to B		5.5	14.0	5.5	14.5	5.5	13.0	5.5	13.5	ns
t_{PHL}			1.5	8.0	1.5	9.0	1.5	6.4	1.5	7.2	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE – IDT54/74FCT622T/AT

			IDT54/74FCT622T				IDT54/74FCT622AT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH}	Propagation Delay $\overline{A}$ to B	C_L = 50pF	5.5	13.5	5.5	14.0	5.5	12.0	5.5	12.5	ns
t_{PHL}		R_L = 500Ω	1.5	8.0	1.5	9.5	1.5	6.0	1.5	7.0	
t_{PLH}	Propagation Delay $\overline{B}$ toA		5.5	12.5	5.5	13.0	5.5	12.0	5.5	12.5	ns
t_{PHL}			1.5	8.0	1.5	9.5	1.5	5.5	1.5	6.5	
t_{PLH}	Propagation Delay $\overline{G}$BA to A		5.5	12.5	5.5	13.0	5.5	11.5	5.5	12.0	ns
t_{PHL}			1.5	10.0	1.5	11.5	1.5	7.0	1.5	8.5	
t_{PLH}	Propagation Delay GAB to B		6.0	12.5	6.0	13.0	6.0	11.5	6.0	12.0	ns
t_{PHL}			1.5	9.5	1.5	11.0	1.5	6.5	1.5	7.5	

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2538 tbl 07

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE REGISTERS

IDT54/74FCT821AT/BT/CT/DT
IDT54/74FCT823AT/BT/CT/DT
IDT54/74FCT825AT/BT/CT
IDT54/74FCT826AT/BT/CT

FEATURES:

- Fastest CMOS logic family available
- A, B, C and D speed grades with 4.2ns tPD
- Available in DIP, SOIC, SSOP, CERPACK and LCC packages
- High-speed parallel registers with positive edge-triggered D-type flip-flops
- Buffered common Clock Enable ($\overline{EN}$) and asynchronous Clear input ($\overline{CLR}$)
- IOL = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- True TTL input and output compatibility
  - VOH = 3.3V (typ.)
  - VOL = 0.3V (typ.)
- Substantially lower input current levels than AMD's bipolar Am29800 series (5μA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Meet or exceed JEDEC Standard 18 specifications

DESCRIPTION:

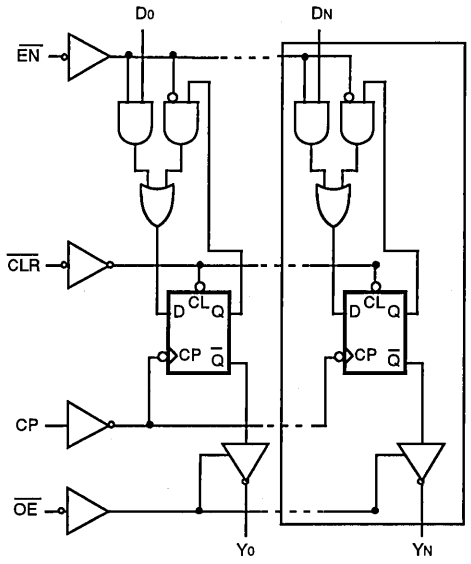
The IDT54/74FCT800 seriesis built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT820 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT821AT/BT/CT/DT are buffered, 10-bit wide versions of the popular '374 function. The IDT54/74FCT823AT/BT/CT/DT are 9-bit wide buffered registers with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high-performance microprogrammed systems. The IDT54/74FCT825AT/BT/CT and IDT54/74FCT826AT/BT/CT are 8-bit buffered registers with all the '823 controls plus multiple enables ($\overline{OE1}$, $\overline{OE2}$, $\overline{OE3}$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. They are ideal for use as an output port requiring high IOL/IOH.

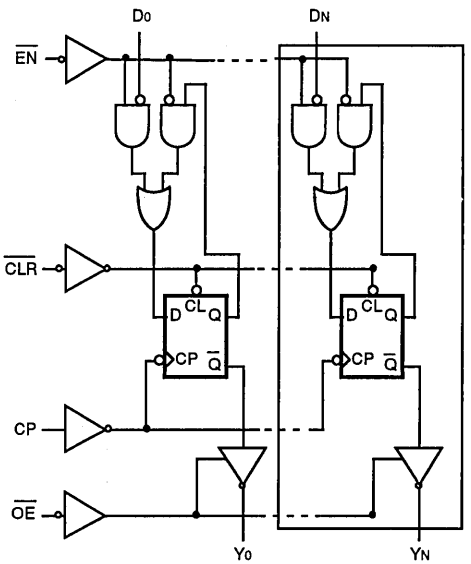
All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

FUNCTIONAL BLOCK DIAGRAM

IDT54/74FCT821/823/825T



IDT54/74FCT826T

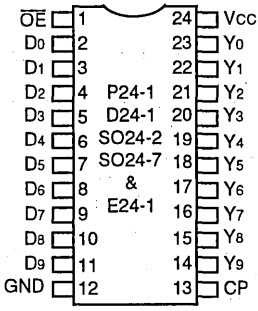


CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

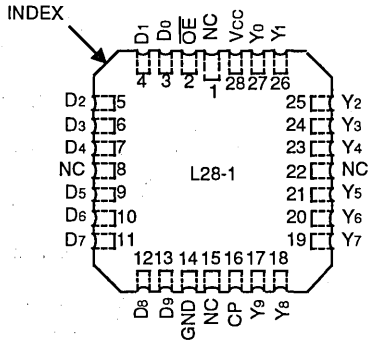
PIN CONFIGURATIONS

LOGIC SYMBOLS

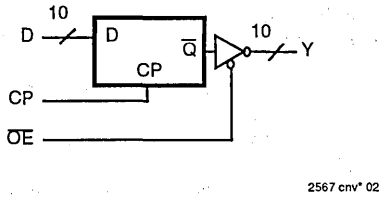
IDT54/74FCT821T 10-BIT REGISTER



DIP/SOIC/SSOP/CERPACK
TOP VIEW

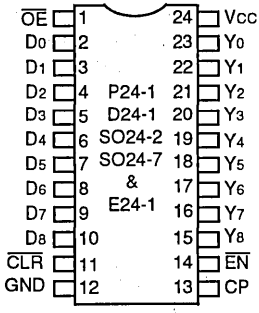


LCC
TOP VIEW

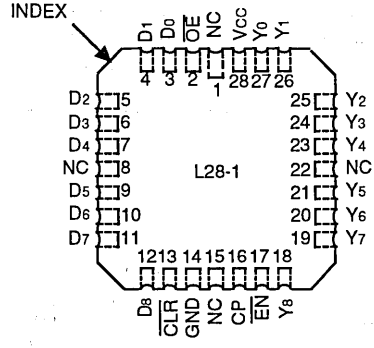


2567 cnv* 02

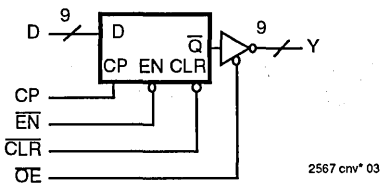
IDT54/74FCT823T 9-BIT REGISTER



DIP/SOIC/SSOP/CERPACK
TOP VIEW

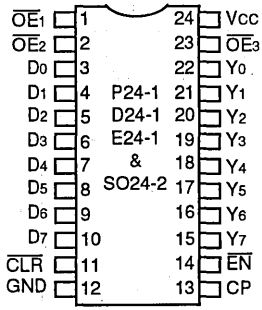


LCC
TOP VIEW

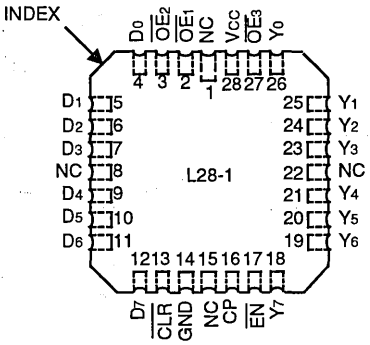


2567 cnv* 03

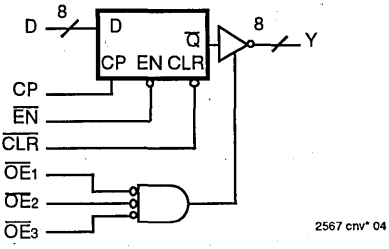
IDT54/74FCT825/826T 8-BIT REGISTER



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW



2567 cnv* 04

PRODUCT SELECTOR GUIDE

	Device		
	10-Bit	9-Bit	8-Bit
Non-inverting	FCT821AT/BT/CT/DT	FCT823AT/BT/CT/DT	FCT825AT/BT/CT
Inverting			FCT826AT/BT/CT

2567 tbl 01

PIN DESCRIPTION

Names	I/O	Description
D_I	I	The D flip-flop data inputs.
$\overline{CLR}$	I	When the clear input is LOW and $\overline{OE}$ is LOW, the Q_I outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Y_I	O	The register 3-state outputs.
$\overline{EN}$	I	Clock Enable. When the clock enable is LOW, data on the D_I input is transferred to the Q_I output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_I outputs do not change state, regardless of the data or clock input transitions.
$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y_I outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_I outputs.

2567 tbl 02

FUNCTION TABLE[1] IDT54/74FCT821/823/825T

Inputs					Internal/ Outputs		
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_I	CP	Q_I	Y_I	Function
H	H	L	L	↑	L	Z	High Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

NOTE:
1. H = HIGH
   L = LOW
   X = Don't Care
   NC = No Change
   ↑ = LOW-to-HIGH Transition
   Z = High Impedance

2567 tbl 03

FUNCTION TABLE[1] IDT54/74FCT826T

Inputs					Internal/ Outputs		
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_I	CP	Q_I	Y_I	Function
H	H	L	L	↑	H	Z	High Z
H	H	L	H	↑	L	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	H	
L	H	L	H	↑	L	L	

NOTE:
1. H = HIGH
   L = LOW
   X = Don't Care
   NC = No Change
   ↑ = LOW-to-HIGH Transition
   Z = High Impedance

2567 tbl 10

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2567 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2567 tbl 05

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = –55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	Vcc = Max.	V_I = 0.5V	—	—	–5	µA
I_{OZH}	High Impedance Output Current	Vcc = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	–10	
I_I	Input HIGH Current	Vcc = Max., V_I = Vcc (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.(3), V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	Vcc = Max. V_{IN} = GND or Vcc		—	0.2	1.5	mA

NOTES: 2567 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = $\overline{EN}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle $\overline{OE}$ = $\overline{EN}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle $\overline{OE}$ = $\overline{EN}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

NOTES:

2567 tbl 07

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT821AT-826AT				FCT821BT-826BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to Yi ($\overline{OE}$ = LOW)	CL = 50pF RL = 500Ω	1.5	10.0	1.5	11.5	1.5	7.5	1.5	8.5	ns
		CL = 300pF[4] RL = 500Ω	1.5	20.0	1.5	20.0	1.5	15.0	1.5	16.0	
tSU	Set-up Time HIGH or LOW Di to CP	CL = 50pF RL = 500Ω	4.0	—	4.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW Di to CP		2.0	—	2.0	—	1.5	—	1.5	—	ns
tSU	Set-up Time HIGH or LOW $\overline{EN}$ to CP		4.0	—	4.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW $\overline{EN}$ to CP		2.0	—	2.0	—	0	—	0	—	ns
tPHL	Propagation Delay, $\overline{CLR}$ to Yi		1.5	14.0	1.5	15.0	1.5	9.0	1.5	9.5	ns
tREM	Recovery Time $\overline{CLR}$ to CP		6.0	—	7.0	—	6.0	—	6.0	—	ns
tW	Clock Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	ns
tW	$\overline{CLR}$ Pulse Width LOW		6.0	—	7.0	—	6.0	—	6.0	—	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to Yi	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		CL = 300pF[4] RL = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to Yi	CL = 5pF[4] RL = 500Ω	1.5	7.0	1.5	8.0	1.5	6.5	1.5	7.0	ns
		CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	7.5	1.5	8.0	

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. This condition is guaranteed but not tested.

2567 tbl 08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT821CT-826CT				FCT821DT		FCT823DT		Unit
			Com'l.		Mil.		Com'l.		Com'l.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to YI ($\overline{OE}$ = LOW)	C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	7.0	1.5	4.2	1.5	5.0	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	12.5	1.5	13.5	1.5	8.0	1.5	8.5	
tSU	Set-up Time HIGH or LOW DI to CP	C_L = 50pF R_L = 500Ω	3.0	—	3.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW DI to CP		1.5	—	1.5	—	1.0	—	1.0	—	ns
tSU	Set-up Time HIGH or LOW $\overline{EN}$ to CP		3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW $\overline{EN}$ to CP		0	—	0	—	0	—	0	—	ns
tPHL	Propagation Delay, $\overline{CLR}$ to YI		1.5	8.0	1.5	8.5	1.5	5.0	1.5	5.0	ns
tREM	Recovery Time $\overline{CLR}$ to CP		6.0	—	6.0	—	3.0	—	3.0	—	ns
tW	Clock Pulse Width HIGH or LOW[3]		6.0	—	6.0	—	3.0	—	3.0	—	ns
tW	$\overline{CLR}$ Pulse Width LOW[3]		6.0	—	6.0	—	3.0	—	3.0	—	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to YI	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	8.0	1.5	4.8	1.5	4.8	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	12.5	1.5	13.5	1.5	9.0	1.5	9.0	
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to YI	C_L = 5pF[4] R_L = 500Ω	1.5	6.0	1.5	6.0	1.5	4.0	1.5	4.0	ns
		C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	6.5	1.5	4.0	1.5	4.0	

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. This condition is guaranteed but not tested.

2567 tbl 09

6

Integrated Device Technology, Inc.

FAST CMOS 10-BIT BUFFERS

IDT54/74FCT827AT/BT/CT/DT
IDT54/74FCT828AT/BT/CT

FEATURES:

- Fastest CMOS logic family available
- A, B, C and D speed grades with 3.8ns t_{PD}
- Available in DIP, SOIC, SSOP, CERPACK and LCC packages
- I_{OL} = 48mA (commercial), and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- True TTL input and output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5μA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

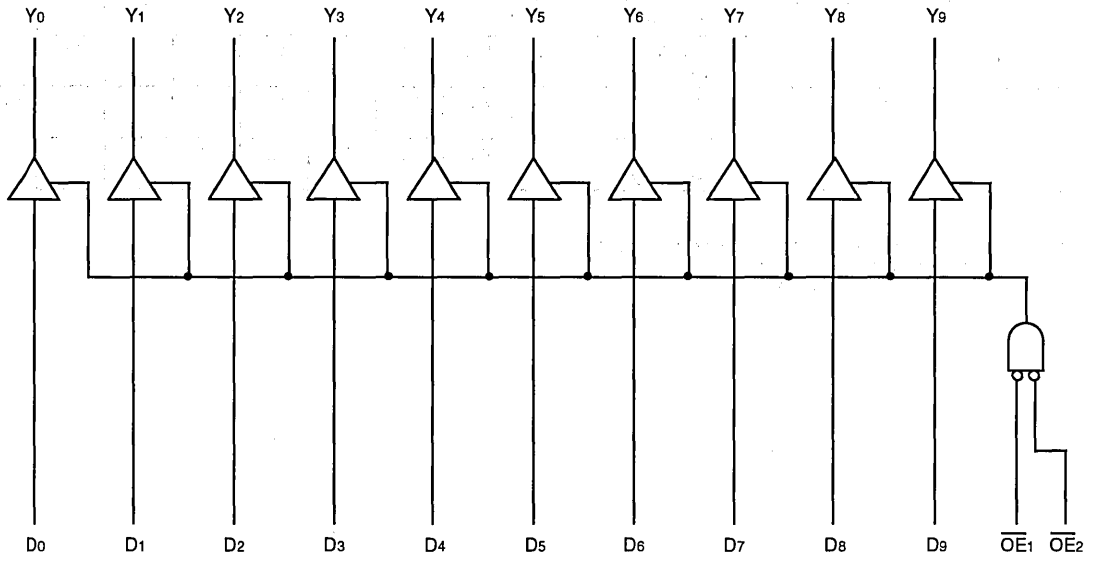
DESCRIPTION:

The IDT54/74FCT800 series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT827AT/BT/CT/DT and IDT54/74FCT828-AT/BT/CT 10-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NAND-ed output enables for maximum control flexibility.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

FUNCTIONAL BLOCK DIAGRAM



2573 cnv* 01

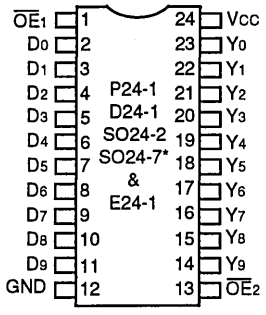
PRODUCT SELECTOR GUIDE

	10-Bit Buffer
Non-inverting	IDT54/74FCT827AT/BT/CT/DT
Inverting	IDT54/74FCT828AT/BT/CT

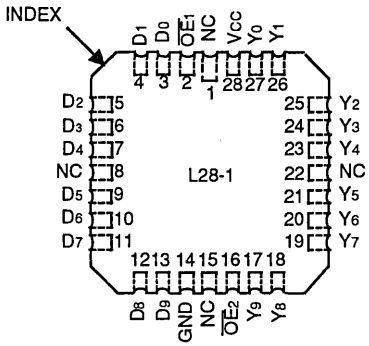
2573 tbl 01

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



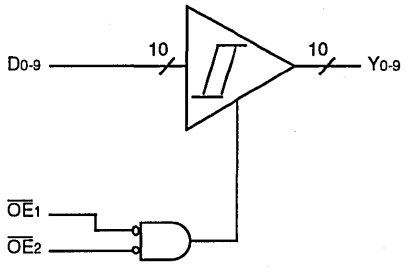
DIP/SOIC/SSOP/CERPACK
TOP VIEW



LCC
TOP VIEW

* FCT827AT/BT/CT/DT only.

LOGIC SYMBOL



2573 cnv* 02–04

PIN DESCRIPTION

Names	I/O	Description
$\overline{OE}_I$	I	When both are LOW the outputs are enabled. When either one or both are HIGH the outputs are High Z.
D_I	I	10-bit data input.
Y_I	O	10-bit data output.

2573 tbl 02

FUNCTION TABLES

IDT54/74FCT827T (NON-INVERTING)(1)

Inputs			Output	
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	Function
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	Three-State
X	H	X	Z	

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

2573 tbl 03

IDT54/74FCT828T (INVERTING)(1)

Inputs			Output	
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	Function
L	L	L	H	Transparent
L	L	H	L	
H	X	X	Z	Three-State
X	H	X	Z	

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

2573 tbl 04

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2573 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2573 tbl 06

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–5	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	–10	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES: 2573 tbl 07

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE_1}$ = $\overline{OE_2}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $\overline{OE_1}$ = $\overline{OE_2}$ = GND One Bit Toggling	V_{IN} = Vcc V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $\overline{OE_1}$ = $\overline{OE_2}$ = GND Eight Bits Toggling	V_{IN} = Vcc V_{IN} = GND	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2573 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at fi
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions[1]	54/74FCT827AT/828AT				54/74FCT827BT/828BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DI to YI	CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	5.0	1.5	6.5	ns
	IDT54/74FCT827T (Non-inverting)	CL = 300pF[3] RL = 500Ω	1.5	15.0	1.5	17.0	1.5	13.0	1.5	14.0	
tPLH tPHL	Propagation Delay DI to YI	CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	5.5	1.5	6.5	ns
	IDT54/74FCT828T (Inverting)	CL = 300pF[3] RL = 500Ω	1.5	14.0	1.5	16.0	1.5	13.0	1.5	14.0	
tPZH tPZL	Output Enable Time $\overline{OE}$I to YI	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		CL = 300pF[3] RL = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	
tPHZ tPLZ	Output Disable Time $\overline{OE}$I to YI	CL = 5pF[3] RL = 500Ω	1.5	9.0	1.5	9.0	1.5	6.0	1.5	7.0	ns
		CL = 50pF RL = 500Ω	1.5	10.0	1.5	10.0	1.5	7.0	1.5	8.0	

2573 tbl 10

Symbol	Parameter	Conditions[1]	54/74FCT827CT/828CT				54/74FCT827DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DI to YI	CL = 50pF RL = 500Ω	1.5	4.4	1.5	5.0	1.5	3.8	—	—	ns
	IDT54/74FCT827T (Non-inverting)	CL = 300pF[3] RL = 500Ω	1.5	10.0	1.5	11.0	1.5	7.5	—	—	
tPLH tPHL	Propagation Delay DI to YI	CL = 50pF RL = 500Ω	1.5	4.4	1.5	5.0	—	—	—	—	ns
	IDT54/74FCT828T (Inverting)	CL = 300pF[3] RL = 500Ω	1.5	10.0	1.5	11.0	—	—	—	—	
tPZH tPZL	Output Enable Time $\overline{OE}$I to YI	CL = 50pF RL = 500Ω	1.5	7.0	1.5	8.0	1.5	5.0	—	—	ns
		CL = 300pF[3] RL = 500Ω	1.5	14.0	1.5	15.0	1.5	9.0	—	—	
tPHZ tPLZ	Output Disable Time $\overline{OE}$I to YI	CL = 5pF[3] RL = 500Ω	1.5	5.7	1.5	6.7	1.5	4.3	—	—	ns
		CL = 50pF RL = 500Ω	1.5	6.0	1.5	7.0	1.5	4.3	—	—	

2573 tbl 11

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These conditions are guaranteed but not tested.

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE LATCHES

IDT54/74FCT841AT/BT/CT/DT
IDT54/74FCT843AT/BT/CT
IDT54/74FCT845AT/BT/CT

FEATURES:

- Fastest CMOS logic family available
- A, B, C and D speed grades with 4.2ns t_{PD}
- Available in DIP, SOIC, SSOP, CERPACK and LCC packages
- TRUE TTL input and output compatible
  - V_{OH} = 3.3V (typ)
  - V_{OL} = 0.3V (typ).
- I_{OL} = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- Substantially lower input current levels than AMD's bipolar Am29800 series (5µA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Meet or exceed JEDEC Standard 18 specifications

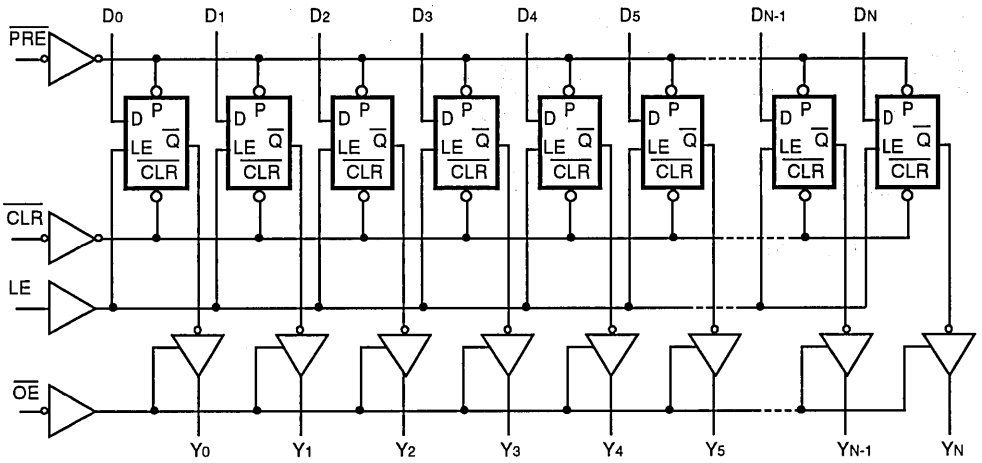
DESCRIPTION:

The IDT54/74FCT800 series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT840 Series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT841AT/BT/CT/DT are buffered, 10-bit wide versions of the popular '373 function. The IDT54/74FCT843AT/BT/CT are 9-bit wide buffered latches with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high-performance systems. The IDT54/74FCT845AT/BT/CT are 8-bit buffered latches with all the '843 controls, plus multiple enables ($\overline{OE_1}$, $\overline{OE_2}$, $\overline{OE_3}$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

FUNCTIONAL BLOCK DIAGRAM



2571 cnv* 01

PRODUCT SELECTOR GUIDE

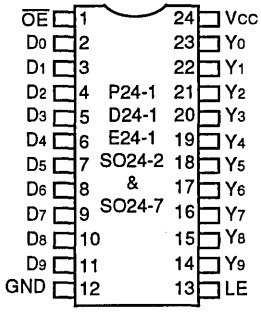
Device		
10-Bit	**9-Bit**	**8-Bit**
IDT54/74FCT841 AT/BT/CT/DT	IDT54/74FCT843 AT/BT/CT	IDT54/74FCT845 AT/BT/CT

2571 tbl 01

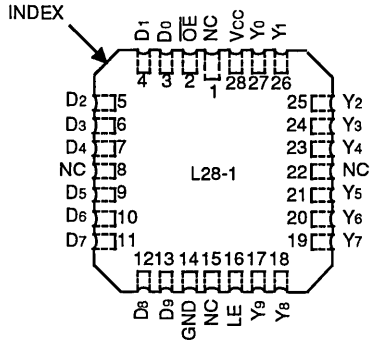
CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS

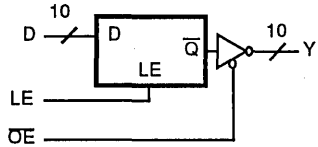
IDT54/74FCT841T 10-BIT LATCH



DIP/CERPACK/SOIC/SSOP
TOP VIEW

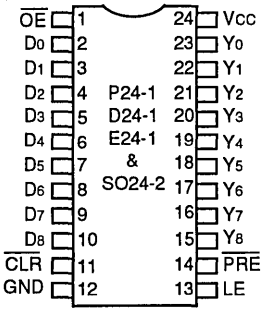


LCC
TOP VIEW

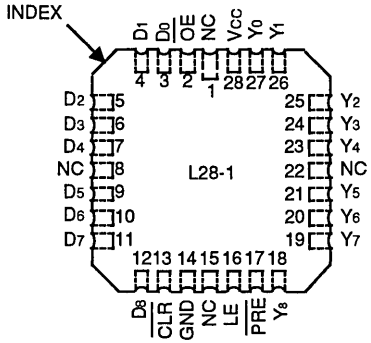


2571 cnv* 02,03,08

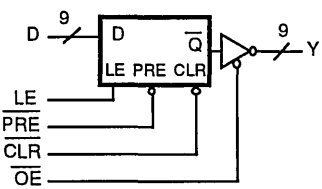
IDT54/74FCT843T 9-BIT LATCH



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW



2571 cnv* 04,05,09

IDT54/74FCT845T 8-BIT LATCH

2571 cnv* 06,07,10

PIN DESCRIPTION

Name	I/O	Description
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_I	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_I	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs V_I are in high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

2571 tbl 02

FUNCTION TABLE[1]

Inputs					Internal	Output	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_I	Q_I	Y_I	Function
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

NOTE: 2571 tbl 03
1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2571 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2571 tbl 05
1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	−5	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	10	µA
I_{OZL}			V_O = 0.5V	—	—	−10	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		—	−0.7	−1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		−60	−120	−225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −6mA MIL. I_{OH} = −8mA COM'L.	2.4	3.3	—	V
			I_{OH} = −12mA MIL. I_{OH} = −15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2571 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = Vcc One Input Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = Vcc One Bit Toggling	V_{IN} = Vcc V_{IN} = GND	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = Vcc Eight Bits Toggling	V_{IN} = Vcc V_{IN} = GND	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2571 tbl 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter		Conditions[1]	FCT841AT/843AT/845AT				FCT841BT/843BT/845BT				Unit
				Com'l.		Mil.		Com'l.		Mil.		
				Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DI to YI (LE = HIGH)		CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	6.5	1.5	7.5	ns
			CL = 300pF[4] RL = 500Ω	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	
tPLH tPHL	Propagation Delay LE to YI		CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	10.5	ns
			CL = 300pF[4] RL = 500Ω	1.5	16.0	1.5	20.0	1.5	15.5	1.5	18.0	
tPLH	Propagation Delay, $\overline{PRE}$ to YI		CL = 50pF RL = 500Ω	1.5	12.0	1.5	14.0	1.5	8.0	1.5	10.0	ns
tPHL				1.5	14.0	1.5	17.0	1.5	10.0	1.5	13.0	
tPHL	Propagation Delay, $\overline{CLR}$ to YI			1.5	13.0	1.5	14.0	1.5	10.0	1.5	11.0	ns
tPLH				1.5	14.0	1.5	17.0	1.5	10.0	1.5	10.0	
tPZH tPZL	Output Enable Time $\overline{OE}$ to YI		CL = 50pF RL = 500Ω	1.5	11.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
			CL = 300pF[4] RL = 500Ω	1.5	23.0	1.5	25.0	1.5	14.0	1.5	15.0	
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to YI		CL = 5pF[4] RL = 500Ω	1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	ns
			CL = 50pF RL = 500Ω	1.5	8.0	1.5	10.0	1.5	7.0	1.5	7.5	
tSU	Data to LE Set-up Time		CL = 50pF RL = 500Ω	2.5	—	2.5	—	2.5	—	2.5	—	ns
tH	Data to LE Hold Time			2.5	—	3.0	—	2.5	—	2.5	—	ns
tW	LE Pulse Width[3]	HIGH		4.0	—	5.0	—	4.0	—	4.0	—	ns
tW	$\overline{PRE}$ Pulse Width[3]	LOW		5.0	—	7.0	—	4.0	—	4.0	—	ns
tW	$\overline{CLR}$ Pulse Width[3]	LOW		4.0	—	5.0	—	4.0	—	4.0	—	ns
tREM	Recovery Time $\overline{PRE}$ to LE			4.0	—	4.0	—	4.0	—	4.0	—	ns
tREM	Recovery Time $\overline{CLR}$ to LE			3.0	—	3.0	—	3.0	—	3.0	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.
4. These conditions are guaranteed but not tested.

2571 tbl 08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter		Conditions[1]	FCT841CT/843CT/845CT				FCT841DT				Unit
				Com'l.		Mil.		Com'l.		Mil.		
				Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DI to YI (LE = HIGH)		CL = 50pF RL = 500Ω	1.5	5.5	1.5	6.3	1.5	4.2	—	—	ns
			CL = 300pF[4] RL = 500Ω	1.5	13.0	1.5	15.0	1.5	8.0	—	—	
tPLH tPHL	Propagation Delay LE to YI		CL = 50pF RL = 500Ω	1.5	6.4	1.5	6.8	1.5	4.0	—	—	ns
			CL = 300pF[4] RL = 500Ω	1.5	15.0	1.5	16.0	1.5	8.0	—	—	
tPLH	Propagation Delay, $\overline{PRE}$ to YI		CL = 50pF	1.5	7.0	1.5	9.0	—	—	—	—	ns
tPHL			RL = 500Ω	1.5	9.0	1.5	12.0	—	—	—	—	
tPHL	Propagation Delay, $\overline{CLR}$ to YI			1.5	9.0	1.5	10.0	—	—	—	—	ns
tPLH				1.5	9.0	1.5	9.0	—	—	—	—	
tPZH tPZL	Output Enable Time $\overline{OE}$ to YI		CL = 50pF RL = 500Ω	1.5	6.5	1.5	7.3	1.5	4.8	—	—	ns
			CL = 300pF[4] RL = 500Ω	1.5	12.0	1.5	13.0	1.5	9.0	—	—	
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to YI		CL = 5pF[4] RL = 500Ω	1.5	5.7	1.5	6.0	1.5	4.0	—	—	ns
			CL = 50pF RL = 500Ω	1.5	6.0	1.5	6.3	1.5	4.0	—	—	
tSU	Data to LE Set-up Time		CL = 50pF	2.5	—	2.5	—	1.5	—	—	—	ns
tH	Data to LE Hold Time		RL = 500Ω	2.5	—	2.5	—	1.0	—	—	—	ns
tW	LE Pulse Width[3]	HIGH		4.0	—	4.0	—	3.0	—	—	—	ns
tW	$\overline{PRE}$ Pulse Width[3]	LOW		4.0	—	4.0	—	—	—	—	—	ns
tW	$\overline{CLR}$ Pulse Width[3]	LOW		4.0	—	4.0	—	—	—	—	—	ns
tREM	Recovery Time $\overline{PRE}$ to LE			4.0	—	4.0	—	—	—	—	—	ns
tREM	Recovery Time $\overline{CLR}$ to LE			3.0	—	3.0	—	—	—	—	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.
4. These conditions are guaranteed but not tested.

2571 tbl 09

6

Integrated Device Technology, Inc.

FAST CMOS OCTAL REGISTERED TRANSCEIVERS

IDT29FCT52A/B/C
IDT29FCT53A/B/C

FEATURES:

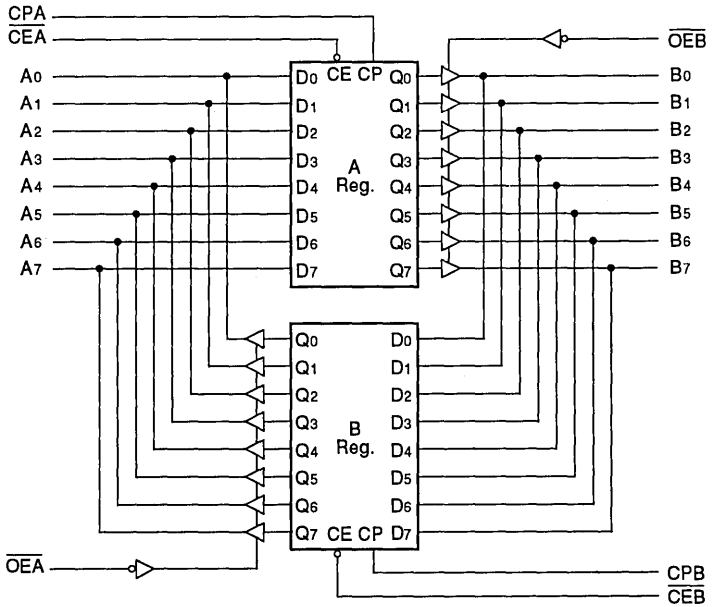
- Equivalent to AMD's Am2952/53 and National's 29F52/53 in pinout/function
- IDT29FCT52A/53A equivalent to FAST™ speed
- **IDT29FCT52B/53B 25% faster than FAST**
- **IDT29FCT52C/53C 37% faster than FAST**
- I_{OL} = 64mA (commercial) and 48mA (military)
- I_{IH} and I_{IL} only 5µA max.
- CMOS power levels (2.5mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Available in 24-pin DIP, SOIC, 28-pin LCC with JEDEC standard pinout
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT29FCT52A/B/C and IDT29FCT53A/B/C are 8-bit registered transceivers manufactured using advanced CEMOS™, a dual-metal CMOS technology. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-state output enable signals are provided for each register. Both A outputs and B outputs are guaranteed to sink 64mA.

The IDT29FCT52A/B/C is a non-inverting option of the IDT29FCT53A/B/C.

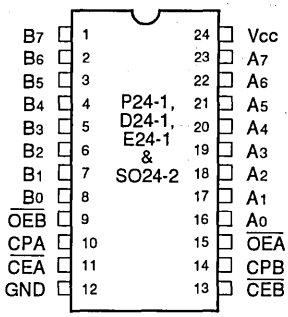
FUNCTIONAL BLOCK DIAGRAM[1]



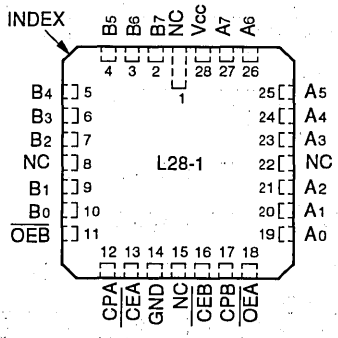
2533 drw 01

NOTE:
1. IDT29FCT52 function is shown.

PIN CONFIGURATIONS



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW

2533 drw 02

PIN DESCRIPTION

Name	I/O	Description
A0-7	I/O	Eight bidirectional lines carrying the A Register inputs or B Register outputs.
B0-7	I/O	Eight bidirectional lines carrying the B Register inputs or A Register outputs.
CPA	I	Clock for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal.
$\overline{CEA}$	I	Clock Enable for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal. When $\overline{CEA}$ is HIGH, the A Register holds its contents, regardless of CPA signal transitions.
$\overline{OEB}$	I	Output Enable for the A Register. When $\overline{OEB}$ is LOW, the A Register outputs are enabled onto the B0-7 lines. When $\overline{OEB}$ is HIGH, the B0-7 outputs are in the high-impedance state.
CPB	I	Clock for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal.
$\overline{CEB}$	I	Clock Enable for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal. When $\overline{CEB}$ is HIGH, the B Register holds its contents, regardless of CPB signal transitions.
$\overline{OEA}$	I	Output Enable for the B Register. When $\overline{OEA}$ is LOW, the B Register outputs are enabled onto the A0-7 lines. When $\overline{OEA}$ is HIGH, the A0-7 outputs are in the high-impedance state.

2533 tbl 05

REGISTER FUNCTION TABLE[1]
(Applies to A or B Register)

Inputs			Internal	
D	CP	$\overline{CE}$	Q	Function
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

2533 tbl 06

OUTPUT CONTROL[1]

	Internal	Y-Outputs		
$\overline{OE}$	Q	52	53	Function
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

2533 tbl 07

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   NC = No Change
   ↑ = LOW-to-HIGH Transition

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2533 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed +0.5V unless otherwise noted.
2. Inputs and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2533 tbl 02

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5(4)	
I_{IL}	Input LOW Current (Except I/O Pins)		V_I = 0.5V	—	—	–5(4)	
			V_I = GND	—	—	–5	
I_{IH}	Input HIGH Current (I/O Pins Only)	V_{CC} = Max.	V_I = V_{CC}	—	—	15	µA
			V_I = 2.7V	—	—	15(4)	
I_{IL}	Input LOW Current (I/O Pins Only)		V_I = 0.5V	—	—	–15(4)	
			V_I = GND	—	—	–15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
			I_{OH} = –15mA MIL.	2.4	4.0	—	
			I_{OH} = –24mA COM'L.	2.4	4.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}(4)	
			I_{OL} = 48mA MIL.(5)	—	0.3	0.55	
			I_{OL} = 64mA COM'L.(5)	—	0.3	0.55	

NOTES: 2533 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.5	1.5	µA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OEA}$ or $\overline{OEB}$= GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OEA}$ or $\overline{OEB}$= GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	2.0	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.5	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OEA}$ or $\overline{OEB}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.3	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.5	16.8[5]	

NOTES:

2533 tbl 07

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT29FCT52A/53A				IDT29FCT52B/53B				IDT29FCT52C/53C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB to A_n, B_n	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	11.0	2.0	7.5	2.0	8.0	2.0	6.3	2.0	7.3	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n		1.5	10.5	1.5	13.0	1.5	8.0	1.5	8.5	1.5	7.0	1.5	8.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n		1.5	10.0	1.5	10.0	1.5	7.5	1.5	8.0	1.5	6.5	1.5	7.5	ns
t_{SU}	Set-up Time HIGH or LOW A_n, B_n to CPA, CPB		2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
t_H	Hold Time HIGH or LOW A_n, B_n to CPA, CPB		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{SU}	Set-up Time HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
t_H	Hold Time HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_W	Pulse Width, HIGH[3] or LOW CPA or CPB		3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns

NOTES:

2533 tbl 08

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

Integrated Device Technology, Inc.

MULTILEVEL PIPELINE REGISTER

IDT29FCT520A
IDT29FCT520B
IDT29FCT520C

FEATURES:

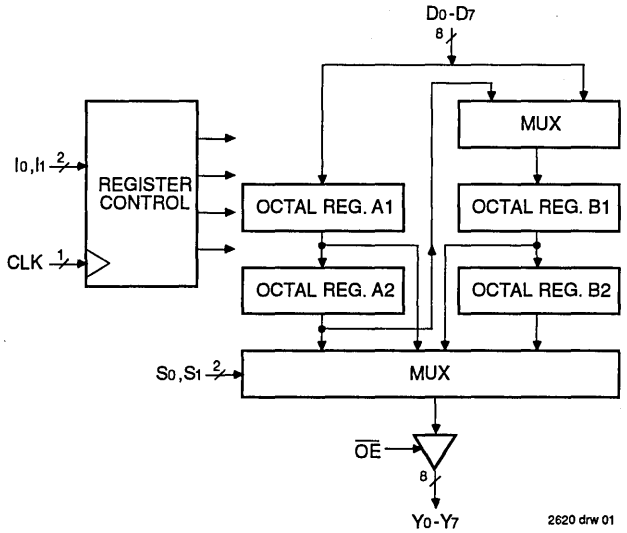
- Equivalent to AMD's Am29520 bipolar Multilevel Pipeline Register in pinout/function, speed and output drive over full temperature and voltage supply extremes
- Four 8-bit high-speed registers
- Dual two-level or single four-level push-only stack operation
- All registers available at multiplexed output
- Hold, transfer and load instructions
- Provides temporary address or data storage
- I_{OL} = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- Substantially lower input current levels than AMD's bipolar (5µA typ.)
- TTL input and output level compatible
- CMOS output level compatible
- Manufactured using advanced CEMOS™ processing
- Available in 300 mil plastic and hermetic DIP, as well as LCC, SOIC and CERPACK
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT29FCT520A/B/C contains four 8-bit positive edge-triggered registers. These may be operated as a dual 2-level or as a single 4-level pipeline. A single 8-bit input is provided and any of the four registers is available at the 8-bit, 3-state output.

In the IDT29FCT520A/B/C when data is entered into the first level (I = 2 or I = 1), the existing data in the first level is moved to the second level. Transfer of data to the second level is achieved using the 4-level shift instruction (I = 0). This transfer also causes the first level to change.

FUNCTIONAL BLOCK DIAGRAM



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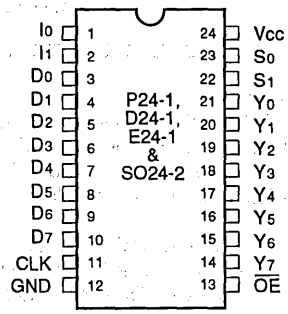
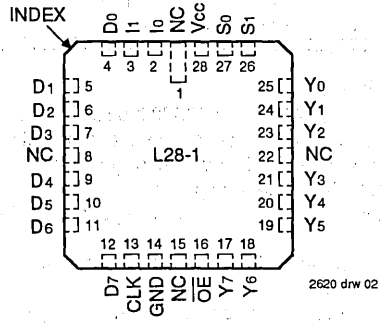
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/CERPACK/SOIC
TOP VIEW



2620 drw 02

LCC
TOP VIEW

DEFINITION OF FUNCTIONAL TERMS

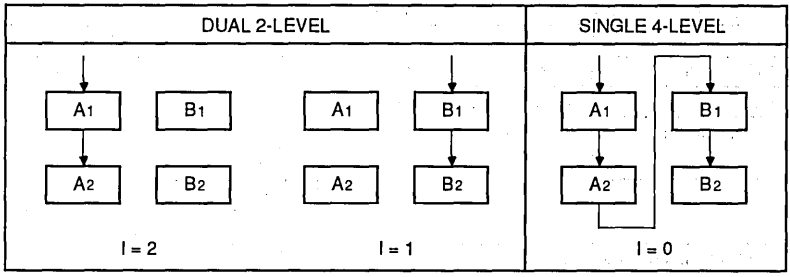
Pin Names	Description
D_n	Register input port.
CLK	Clock input. Enter data into registers on LOW-to-HIGH transitions.
I_0, I_1	Instruction inputs. See Figure 1 and Instruction Control Tables.
S_0, S_1	Multiplexer select. Inputs either register A_1, A_2, B_1 or B_2 data to be available at the output port.
$\overline{OE}$	Output enable for 3-state output port
Y_n	Register output port.

2620 tbl 01

REGISTER SELECTION

S_1	S_0	Register
0	0	B_2
0	1	B_1
1	0	A_2
1	1	A_1

2620 tbl 02



2620 drw 03

NOTE:
1. I = 3 for hold.

Figure 1. Data Loading in 2-Level Operation

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

2620 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals.
3. Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

2620 tbl 04

1. This parameter is measured at characterization data but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	10	µA
			V_O = 2.7V	—	—	10[4]	
I_{OZL}			V_O = 0.5V	—	—	–10[4]	
			V_O = GND	—	—	–10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

2620 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current, TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
		$\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz, 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	7.0	12.8[5]	
		$\overline{OE}$ = GND Eight Bits Toggling at f_i = 5MHz, 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	9.2	21.8[5]	

2620 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL HIgh Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT520A				IDT54/74FCT520B				IDT54/74FCT520C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PHL} t_{PLH}	Propagation Delay CLK to Y_n	C_L = 50pF R_L = 500Ω	2.0	14.0	2.0	16.0	2.0	7.5	2.0	8.0	2.0	6.0	2.0	7.0	ns
t_{PHL} t_{PLH}	Propagation Delay S_0 or S_1 to Y_n		2.0	13.0	2.0	15.0	2.0	7.5	2.0	8.0	2.0	6.0	2.0	7.0	ns
t_{SU}	Set-up Time HIGH or LOW D_n to CLK		5.0	—	6.0	—	2.5	—	2.8	—	2.5	—	2.8	—	ns
t_H	Hold Time HIGH or LOW D_n to CLK		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_{SU}	Set-up Time HIGH or LOW I_0 or I_1 to CLK		5.0	—	6.0	—	4.0	—	4.5	—	4.0	—	4.5	—	ns
t_H	Hold Time HIGH or LOW I_0 or I_1 to CLK		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	12.0	1.5	13.0	1.5	7.0	1.5	7.5	1.5	6.0	1.5	6.0	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	15.0	1.5	16.0	1.5	7.5	1.5	8.0	1.5	6.0	1.5	7.0	ns
t_W	Clock Pulse Width HIGH or LOW		7.0	—	8.0	—	5.5	—	6.0	—	5.5	—	6.0	—	ns

NOTES:

2620 tbl 07

1. See test circuit and waveforms.
2. Minimum units are guaranteed but not tested on Propagation Delays.

Integrated Device Technology, Inc.

FAST CMOS BUFFER/CLOCK DRIVER

IDT49FCT805/A
IDT49FCT806/A

FEATURES:

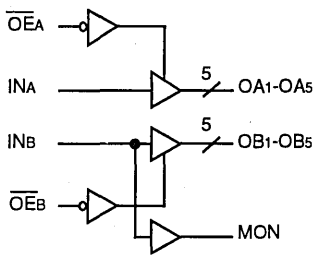
- Guaranteed low skew:
  — 0.7ns (COM)
  — 0.9ns (MIL)
- Very low duty cycle distortion
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (1mW typ. static)
- TTL compatible inputs and outputs
- Rail-to-rail output voltage swing
- Two independent groups of buffers with 3-state control
- 5:1 fanout per group
- 'Heartbeat' monitor output
- 20-pin DIP, SOIC, SSOP (805 only), CERPACK and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49FCT805/A and IDT49FCT806/A are clock drivers built using advanced CEMOS™, a dual metal CMOS technology. The IDT49FCT805/A is a non-inverting clock driver and the IDT49FCT806/A is an inverting clock driver. Each device consists of two banks of drivers. Each bank drives five output buffers from a standard TTL compatible input. The devices feature a "heartbeat" monitor for diagnostics and PLL driving. The 805/A and 806/A offer low capacitance inputs with hysteresis. Rail-to-rail output swing improves noise margin and allows easy interface with CMOS inputs.

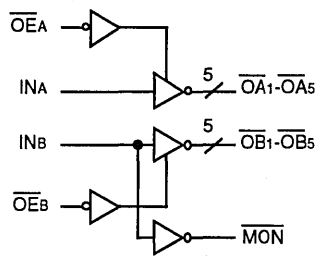
FUNCTIONAL BLOCK DIAGRAMS

IDT49FCT805



2574 drw 03

IDT49FCT806



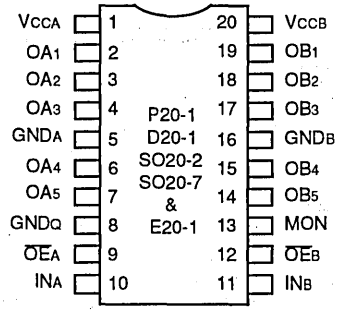
2574 drw 06

6

CEMOS is a trademark of Integrated Device Technology, Inc.

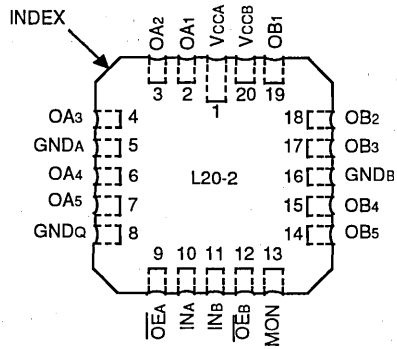
PIN CONFIGURATIONS

IDT49FCT805



DIP/SOIC/SSOP/CERPACK
TOP VIEW

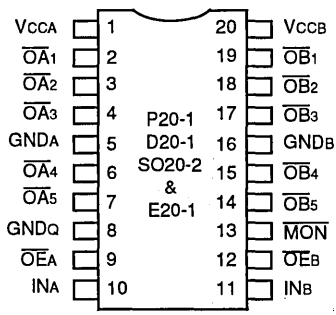
2574 drw 01



LCC
TOP VIEW

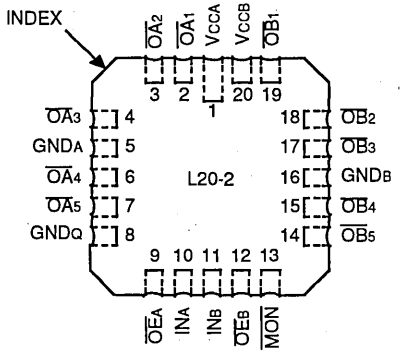
2574 drw 02

IDT49FCT806



DIP/SOIC/CERPACK
TOP VIEW

2574 drw 04



LCC
TOP VIEW

2574 drw 05

PIN DESCRIPTION

Pin Names	Description
$\overline{OE_A}$, $\overline{OE_B}$	3-State Output Enable Inputs (Active LOW)
IN_A, IN_B	Clock Inputs
O_An, O_Bn	Clock Outputs (FCT805)
$\overline{O_An}$, $\overline{O_Bn}$	Clock Outputs (FCT806)
MON	Monitor Output (FCT805)
$\overline{MON}$	Monitor Output (FCT806)

2574 tbl 05

FUNCTION TABLE[1]

Inputs		Outputs			
		49FCT805		49FCT806	
$\overline{OE_A}$, $\overline{OE_B}$	IN_A, IN_B	O_An, O_Bn	MON	$\overline{O_An}$, $\overline{O_Bn}$	$\overline{MON}$
L	L	L	L	H	H
L	H	H	H	L	L
H	L	Z	L	Z	H
H	H	Z	H	Z	L

NOTE:
1. H = HIGH, L = LOW, Z = High Impedance

2574 tbl 06

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2574 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals.
3. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2574 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V ± 5%, Military: T_A = –55°C to +125°C; V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = GND	—	—	–5	µA
I_{OZH}	Off State (High Z)	V_{CC} = Max.	V_O = V_{CC}	—	—	10	µA
I_{OZL}	Output Current		V_O = GND	—	—	–10	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	3.6	4.3	—	
			I_{OH} = –24mA MIL. I_{OH} = –24mA COM'L.	2.4	3.8	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OH} = 300µA	—	GND	V_{LC}(4)	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	
V_H	Input Hysteresis for all inputs	—		—	200	—	mV

NOTES: 2574 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	1.0	2.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE_A}$ = $\overline{OE_B}$ = GND Per Output Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.20	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $\overline{OE_A}$ = $\overline{OE_B}$ = V_{CC} Mon. Output Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	3.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	4.8	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $\overline{OE_A}$ = $\overline{OE_B}$ = GND Eleven Outputs Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	4.3	7.0[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.3	9.5[5]	

2574 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_O = Number of Outputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SKEW CHARACTERISTICS OVER OPERATING RANGE[2]

Symbol	Parameter	Condition[1]	IDT49FCT805/806				IDT49FCT805A/806A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.	Max.	Min.	Max.	Min.[2]	Max.	Min.[2]	Max.	
$t_{SK(o)}$	Skew between two outputs of same package (same transition)	C_L = 50pF R_L = 500Ω	—	0.7	—	0.9	—	0.7	—	0.9	ns
$t_{SK(p)}$	Skew between opposite transitions (t_{PHL}-t_{PLH}) of same output		—	1.0	—	1.1	—	1.0	—	1.1	ns
$t_{SK(t)}$	Skew between two outputs of different package at same power supply voltage and temperature (same transition)		—	1.5	—	1.5	—	1.5	—	1.5	ns

NOTES:
2574 tbl 07

1. See test circuit and waveforms.
2. Skew guaranteed across temperature range but measured at maximum temperature only. Skew parameters apply to propagation delays only.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[3]

Symbol	Parameter	Condition[1]	IDT49FCT805/806				IDT49FCT805A/806A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay IN_A to OA_n, IN_B to OB_n	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.5	1.5	5.8	1.5	6.8	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		1.5	8.0	1.5	8.5	1.5	8.0	1.5	8.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		1.5	7.0	1.5	7.5	1.5	7.0	1.5	7.5	ns

NOTES:
2574 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Propagation delay range indicated by Min. and Max. limit is due to Vcc, operating temperature, and process parameters. These propagation delay limits do not imply skew.

6

Integrated Device Technology, Inc.

FAST CMOS 1-OF-8 DECODER WITH ENABLE

IDT54/74FCT138
IDT54/74FCT138A
IDT54/74FCT138C

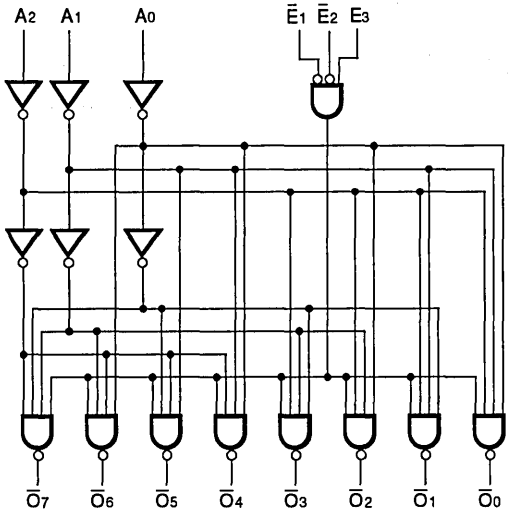
FEATURES:

- IDT54/74FCT138 equivalent to FAST™ speed
- **IDT54/74FCT138A 35% faster than FAST**
- **IDT54/74FCT138C 40% faster than FAST**
- Equivalent to FAST speeds output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST (5µA max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing # 5962-87654 is listed on this function. Refer to section 2.

DESCRIPTION:

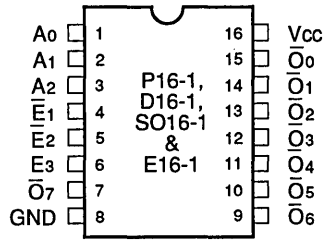
The IDT54/74FCT138/A/C are 1-of-8 decoders built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT138/A/C accept three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provide eight mutually exclusive active LOW outputs ($\overline{O}_0$ - $\overline{O}_7$). The IDT54/74FCT138/A/C feature three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four IDT54/74FCT138/A/C devices and one inverter.

FUNCTIONAL BLOCK DIAGRAM

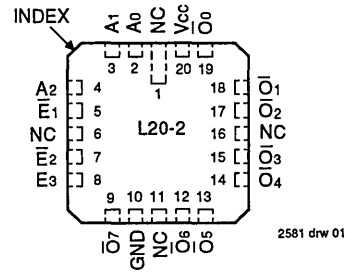


2581 drw 02

PIN CONFIGURATIONS



DIP/SOIC/CERPACK TOP VIEW



2581 drw 01

LCC TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
A_0–A_2	Address Inputs
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
$\overline{O}_0$–$\overline{O}_7$	Outputs (Active LOW)

2581 tbl 05

FUNCTION TABLE

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

2581 tbl 06

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2581 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2581 tbl 02

1. This parameter is guaranteed characterization data and not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
			I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}[4]	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES: 2581 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} ≥ V_{HC}; V_{IN} ≤ V_{LC}		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Output Toggling 50% Duty Cycle	V_{IN} ≥ V_{HC} V_{IN} ≤ V_{LC}	—	0.15	0.3	mA/MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max. Outputs Open Toggle $\overline{E}_1$, $\overline{E}_2$ or E_3	V_{IN} ≥ V_{HC} V_{IN} ≤ V_{LC} (FCT)	—	1.7	4.5	mA
		50% Duty Cycle f_O = 10MHz One Output Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.5	

NOTES: 2581 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
   I_C = I_{CC} + ΔI_{CC} $D_H N_T$ + I_{CCD} (f_{CP}/2 + f_{ONO})
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_O = Output Frequency
   N_O = Number of Outputs at f_O
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT138				IDT54/74FCT138A				IDT54/74FCT138C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay An to $\overline{O}_n$	CL = 50pF RL = 500Ω	1.5	9.0	1.5	12.0	1.5	5.8	1.5	7.8	1.5	5.1	1.5	6.0	ns
tPLH tPHL	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$		1.5	9.0	1.5	12.5	1.5	5.9	1.5	8.0	1.5	5.2	1.5	6.1	ns
tPLH tPHL	Propagation Delay E3 to $\overline{O}_n$		1.5	9.0	1.5	12.5	1.5	5.9	1.5	8.0	1.5	5.2	1.5	6.1	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2581 tbl 07

6

Integrated Device Technology, Inc.

FAST CMOS DUAL 1-OF-4 DECODER WITH ENABLE

IDT54/74FCT139
IDT54/74FCT139A
IDT54/74FCT139C

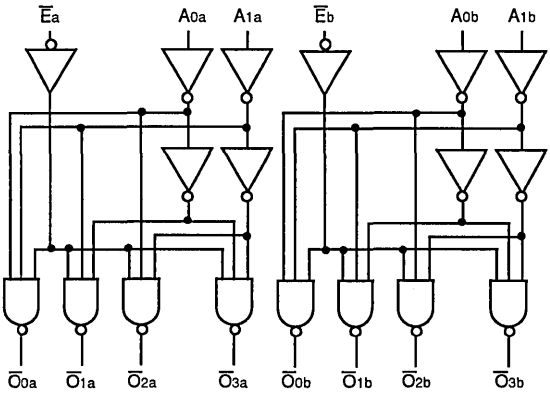
FEATURES:

- IDT54/74FCT139 equivalent to FAST™ speed
- **IDT54/74FCT139A 35% faster than FAST**
- **IDT54/74FCT139C 45% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST (5µA max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

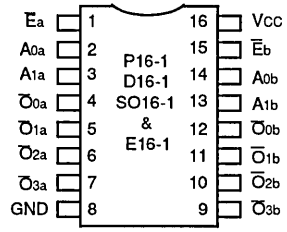
The IDT54/74FCT139/A/C are dual 1-of-4 decoders built using advanced CEMOS™, a dual metal CMOS technology. These devices have two independent decoders, each of which accept two binary weighted inputs (A_0-A_1) and provide four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH, all outputs are forced HIGH.

FUNCTIONAL BLOCK DIAGRAM



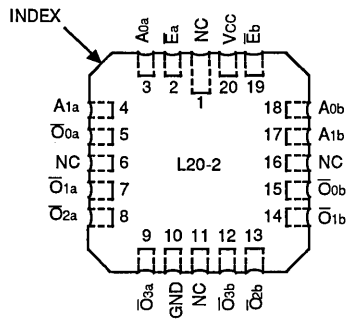
2605 cnv* 03

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW

2605 cnv* 01



LCC
TOP VIEW

2605 cnv* 02

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

TRUTH TABLE[1]

Inputs			Outputs			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

2605 tbl 05

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

PIN DESCRIPTION

Pin Names	Description
A_0, A_1	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
$\overline{O}_0$ - $\overline{O}_3$	Outputs (Active LOW)

2605 tbl 04

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

2605 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2605 tbl 02

NOTE:
1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

2605 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS $V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.3	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fo = 10MHz 50% Duty Cycle One Output Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT) V_{IN} = 3.4V V_{IN} = GND	— —	1.7 2.0	4.5 5.5	mA
		V_{CC} = Max. Outputs Open fo = 10MHz 50% Duty Cycle One Output Toggling on Each Decoder	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT) V_{IN} = 3.4V V_{IN} = GND	— —	3.2 3.7	7.5[5] 9.5[5]	

NOTES: 2605 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_o N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_o = Output Frequency
   N_O = Number of Outputs at f_o
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FCT139				IDT54/74FCT139A				IDT54/74FCT139C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Parameter	Description	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay A_0 or A_1 to $\overline{On}$	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	12.0	1.5	5.9	1.5	7.8	1.5	5.0	1.5	6.2	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{On}$		1.5	8.0	1.5	9.0	1.5	5.5	1.5	7.2	1.5	4.8	1.5	5.8	ns

NOTES: 2605 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

6

Integrated Device Technology, Inc.

FAST CMOS SYNCHRONOUS PRESETTABLE BINARY COUNTERS

IDT54/74FCT161/A/C
IDT54/74FCT163/A/C

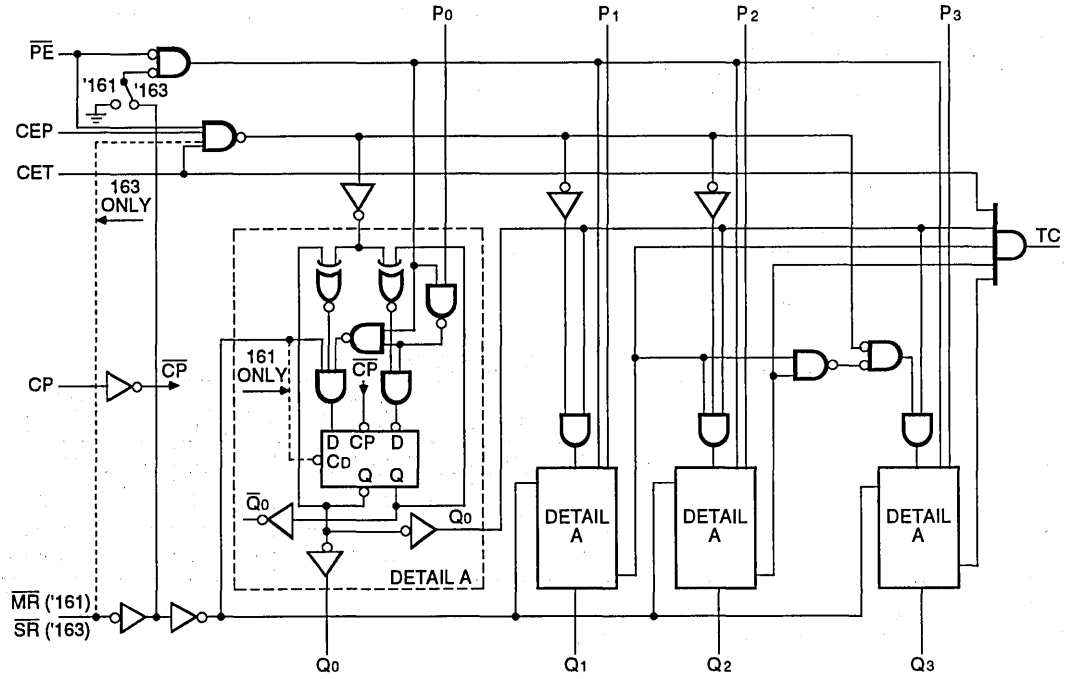
FEATURES:

- IDT54/74FCT161/163 equivalent to FAST™ speed
- **IDT54/74FCT161A/163A 35% faster than FAST**
- **IDT54/74FCT161A/163C 45% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- CMOS output level compatible
- Substantially lower input current levels than FAST (5µA max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT161/163, IDT54/74FCT161A/163A and IDT54/74FCT161C/163C are high-speed synchronous modulo-16 binary counters built using advanced CEMOS™, a dual metal CMOS technology. They are synchronously presettable for application in programmable dividers and have two types of count enable inputs plus a terminal count output for versatility in forming synchronous multistage counters. The IDT54/74FCT161/A/C have asynchronous Master Reset inputs that override all other inputs and force the outputs LOW. The IDT54/74FCT163/A/C have Synchronous Reset inputs that override counting and parallel loading and allow the outputs to be simultaneously reset on the rising edge of the clock.

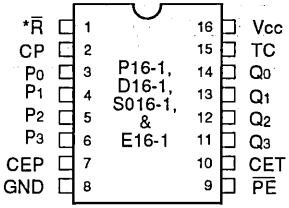
FUNCTIONAL BLOCK DIAGRAM



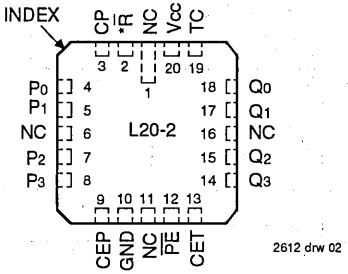
2612 drw 01

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

*$\overline{MR}$ for '161
*$\overline{SR}$ for '163

PIN DESCRIPTION

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$ ('161)	Asynchronous Master Reset Input (Active LOW)
$\overline{SR}$ ('163)	Synchronous Reset Input (Active LOW)
P_{0-3}	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q_{0-3}	Flip-Flop Outputs
TC	Terminal Count Output

2612 tbl 05

FUNCTION TABLE(2)

$\overline{SR}$(1)	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge(s)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

NOTES:
1. For FCT163/163A/163C only.
2. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care.

2612 tbl 06

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2612 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Inputs and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2612 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)			Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		COM'L(5)	2.0V	—	—	V
				MIL	3.0V	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level			—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}		—	—	5	µA
			V_I = 2.7V		—	—	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V		—	—	–5(4)	
			V_I = GND		—	—	–5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA			—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND			–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA			V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA		V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL.		2.4	4.3	—	
			I_{OH} = –15mA COM'L.		2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA			—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA		—	GND	V_{LC}(4)	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.		—	0.3	0.5	
			I_{OL} = 48mA COM'L.		—	0.3	0.5	

NOTES: 2612 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. Clock pin requires a minimum V_{IH} of 2.7V.

POWER SUPPLY CHARACTERISTICS V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max., V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open Load Mode $\overline{CEP}$ = $\overline{CET}$ = $\overline{PE}$ = GND $\overline{MR}$ or $\overline{SR}$ = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open Load Mode f_{CP} = 10MHz 50% Duty Cycle $\overline{CEP}$ = $\overline{CET}$ = $\overline{PE}$ = GND $\overline{MR}$ or $\overline{SR}$ = V_{CC} One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max., Outputs Open Load Mode f_{CP} = 10MHz 50% Duty Cycle $\overline{CEP}$ = $\overline{CET}$ = $\overline{PE}$ = GND $\overline{MR}$ or $\overline{SR}$ = V_{CC} Four Bits Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.2	12.8[5]	

2612 tbl 04

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT161/163				IDT54/74FCT161A/163A				IDT54/74FCT161C/163C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	C_L = 50pF R_L = 500Ω	2.0	11.0	2.0	11.5	2.0	7.2	2.0	7.5	2.0	5.8	2.0	6.3	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)		2.0	9.5	2.0	10.0	2.0	6.2	2.0	6.5	2.0	5.8	2.0	6.3	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC		2.0	15.0	2.0	16.5	2.0	9.8	2.0	10.8	2.0	7.4	2.0	8.3	ns
t_{PLH} t_{PHL}	Propagation Delay CET to TC		1.5	8.5	1.5	9.0	1.5	5.5	1.5	5.9	1.5	5.2	1.5	5.6	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('161)		2.0	13.0	2.0	14.0	2.0	8.5	2.0	9.1	2.0	6.0	2.0	6.6	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to TC ('161)		2.0	11.5	2.0	12.5	2.0	7.5	2.0	8.2	2.0	7.0	2.0	7.7	ns
t_{SU}	Set-up Time, HIGH or LOW P_n to CP		5.0	—	5.5	—	4.0	—	4.5	—	4.0	—	4.5	—	ns
t_H	Hold Time, HIGH or LOW P_n to CP		1.5	—	2.0	—	1.5	—	2.0	—	1.5	—	2.0	—	ns
t_{SU}	Set-up Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		11.5	—	13.5	—	9.5	—	11.5	—	9.5	—	11.5	—	ns
t_H	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{SU}	Set-up Time, HIGH or LOW CEP or CET to CP		11.5	—	13.0	—	9.5	—	11.0	—	9.5	—	11.0	—	ns
t_H	Hold Time, HIGH or LOW CEP or CET to CP		0	—	0	—	0	—	0	—	0	—	0	—	ns
t_W	Clock Pulse Width (Load) HIGH or LOW		5.0	—	5.0	—	4.0[3]	—	4.0[3]	—	4.0[3]	—	4.0[3]	—	ns
t_W	Clock Pulse Width (Count) HIGH or LOW		7.0	—	8.0	—	6.0	—	7.0	—	6.0	—	7.0	—	ns
t_W	$\overline{MR}$ Pulse Width, LOW ('161)		5.0	—	5.0	—	4.0[3]	—	4.0[3]	—	4.0[3]	—	4.0[3]	—	ns
t_{REM}	Recovery Time $\overline{MR}$ to CP ('161)		6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2612 tbl 07

Integrated Device Technology, Inc.

FAST CMOS CARRY LOOKAHEAD GENERATOR

IDT54/74FCT182
IDT54/74FCT182A

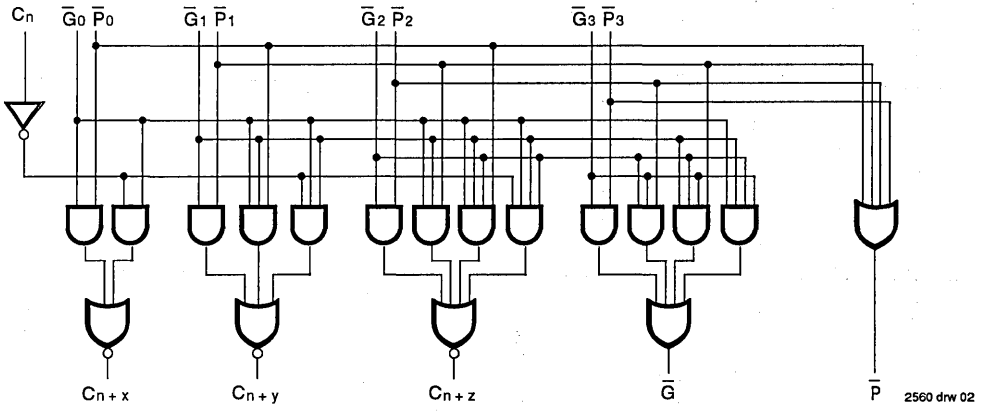
FEATURES:

- IDT54/74FCT182 equivalent to FAST™ speed;
- **IDT54/74FCT182A 30% faster than FAST**
- Equivalent to FAST speeds and output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST (5µA max.)
- Carry lookahead generator
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

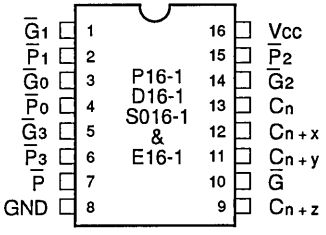
DESCRIPTION:

The IDT54/74FCT182 and IDT54/74FCT182A are high-speed carry lookahead generators built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT182 and IDT54/74FCT182A are carry lookahead generators that accept up to four pairs of active LOW Carry Propagate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$) and Carry Generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$) signals and an active HIGH carry input (C_n) and provides anticipated HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. These products also have active LOW Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of lookahead.

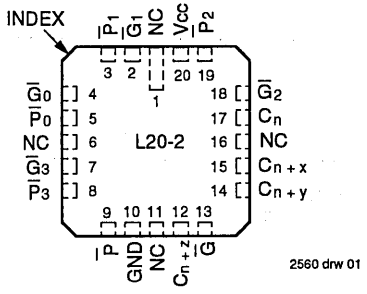
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
C_n	Carry Input
$\overline{G}_0 - \overline{G}_3$	Carry Generate Inputs (Active LOW)
$\overline{P}_0 - \overline{P}_3$	Carry Propagate Inputs (Active LOW)
$C_{n+x} - C_{n+z}$	Carry Outputs
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)

2560 tbl 05

FUNCTION TABLE[1]

Inputs									Outputs				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
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X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
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	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

2560 tbl 06

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2560 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2560 tbl 02

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES: 2560 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.3	mA/ MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.5	

NOTES:
2560 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FCT182				IDT54/74FCT182A				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Conditions[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+x}, C_{n+y}, C_{n+z}	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	16.5	2.0	7.0	2.0	10.7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P_0}$, $\overline{P_1}$, $\overline{P_2}$ to C_{n+x}, C_{n+y}, C_{n+z}		1.5	9.0	1.5	11.5	1.5	8.5	1.5	9.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{G_0}$, $\overline{G_1}$, $\overline{G_2}$ to C_{n+x}, C_{n+y}, C_{n+z}		1.5	9.5	1.5	11.5	1.5	8.5	1.5	9.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P_1}$, $\overline{P_2}$, $\overline{P_3}$ to $\overline{G}$		2.0	11.0	2.0	16.5	2.0	7.2	2.0	10.7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{G_n}$ to $\overline{G}$		2.0	11.5	2.0	16.5	2.0	7.6	2.0	10.7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P_n}$ to $\overline{P}$		1.5	8.5	1.5	12.5	1.5	6.0	1.5	7.4	ns

NOTES:
2560 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

Integrated Device Technology, Inc.

FAST CMOS UP/DOWN BINARY COUNTER

IDT54/74FCT191
IDT54/74FCT191A

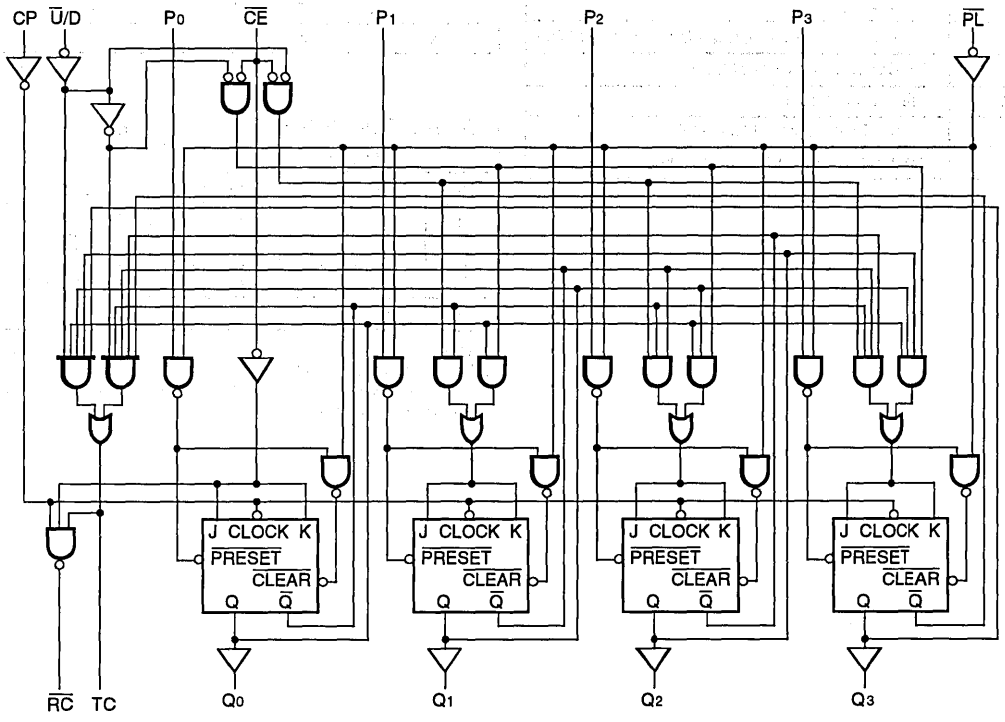
FEATURES:

- IDT54/74FCT191 equivalent to FAST™ speed
- **IDT54/74FCT191A 35% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- CMOS output level compatible
- Substantially lower input current levels than FAST (5µA max.)
- JEDEC standard pinout for DIP, LCC and SOIC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT191 and IDT54/74FCT191A are reversible modulo-16 binary counters, featuring synchronous counting and asynchronous presetting and are built using advanced CEMOS™, a dual metal CMOS technology. The preset feature allows the IDT54/74FCT191 and IDT54/74FCT191A to be used in programmable dividers. The count enable input, terminal count output and ripple clock output make possible a variety of methods of implementing multiusage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

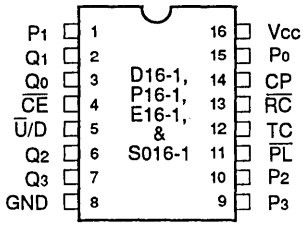
FUNCTIONAL BLOCK DIAGRAM



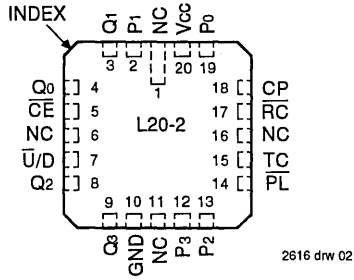
2616 drw 01

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
P_{0-3}	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
$\overline{U}/D$	Up/Down Count Control Input
Q_{0-3}	Flip-Flop Outputs
$\overline{RC}$	Ripple Clock Output (Active LOW)
TC	Terminal Count Output (Active HIGH)

2616 tbl 05

$\overline{RC}$ FUNCTION TABLE[2]

Inputs		Outputs	
$\overline{CE}$	CP	TC[1]	$\overline{RC}$
L	⊓	H	⊓
H	X	X	H
X	X	L	H

2616 tbl 06

MODE SELECT FUNCTION TABLE[2]

Inputs				
$\overline{PL}$	$\overline{CE}$	$\overline{U}/D$	CP	Mode
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Preset (Asynchronous)
H	H	X	X	No Change (Hold)

2616 tbl 07

NOTES:
1. TC is generated internally.
2. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, ↑= LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2616 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Inputs and V_{CC} terminals.
3. Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2616 tbl 02

1. This parameter is guaranteed at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military; T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	COM'L[5]	2.0V	—	—	V
			MIL	3.0V	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES: 2616 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. Clock pin requires a minimum V_{IH} of 2.7V.

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POWER SUPPLY CHARACTERISTICS V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max., V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open Preset Mode $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open Preset Mode $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.0	2.8	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.2	3.8	
		V_{CC} = Max., Outputs Open Preset Mode $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND Four Bits Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	4.2	10.5[5]	

2616 tbl 04

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT191				IDT54/74FCT191A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	C_L = 50pF R_L = 500Ω	2.5	12.0	1.5	16.0	2.5	7.8	1.5	10.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$		3.0	14.0	2.0	16.0	3.0	11.8	2.0	12.2	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$		2.5	8.5	1.5	12.5	2.5	8.5	1.5	10.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$		2.0	8.0	2.0	8.5	2.0	7.2	2.0	8.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}/D$ to $\overline{RC}$		4.0	20.0	4.0	22.5	4.0	13.0	4.0	14.7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}/D$ to $\overline{TC}$		3.0	11.0	3.0	13.0	3.0	7.2	3.0	8.5	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		2.0	14.0	1.5	16.0	2.0	9.1	1.5	10.4	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		3.0	13.0	3.0	14.0	3.0	8.5	3.0	9.1	ns
t_{SU}	Set-up Time, HIGH or LOW P_n to $\overline{PL}$		5.0	—	6.0	—	4.0	—	5.0	—	ns
t_H	Hold Time, HIGH or LOW P_n to $\overline{PL}$		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{SU}	Set-up Time LOW $\overline{CE}$ to CP		10.0	—	10.5	—	9.0	—	9.5	—	ns
t_H	Hold Time LOW $\overline{CE}$ to CP		0	—	0	—	0	—	0	—	ns
t_{SU}	Set-up Time, HIGH or LOW $\overline{U}/D$ to CP		12.0	—	12.0	—	10.0	—	10.0	—	ns
t_H	Hold Time, HIGH or LOW $\overline{U}/D$ to CP		0	—	0	—	0	—	0	—	ns
t_W	$\overline{PL}$ Pulse Width LOW		6.0	—	8.5	—	5.5	—	8.0	—	ns
t_W	CP Pulse Width HIGH or LOW		5.0	—	7.0	—	4.0[3]	—	6.0	—	ns
t_{REM}	Recovery Time $\overline{PL}$ to CP		6.0	—	7.5	—	5.0	—	6.5	—	ns

NOTES:
1. See test circuit and waveform.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2616 tbl 08

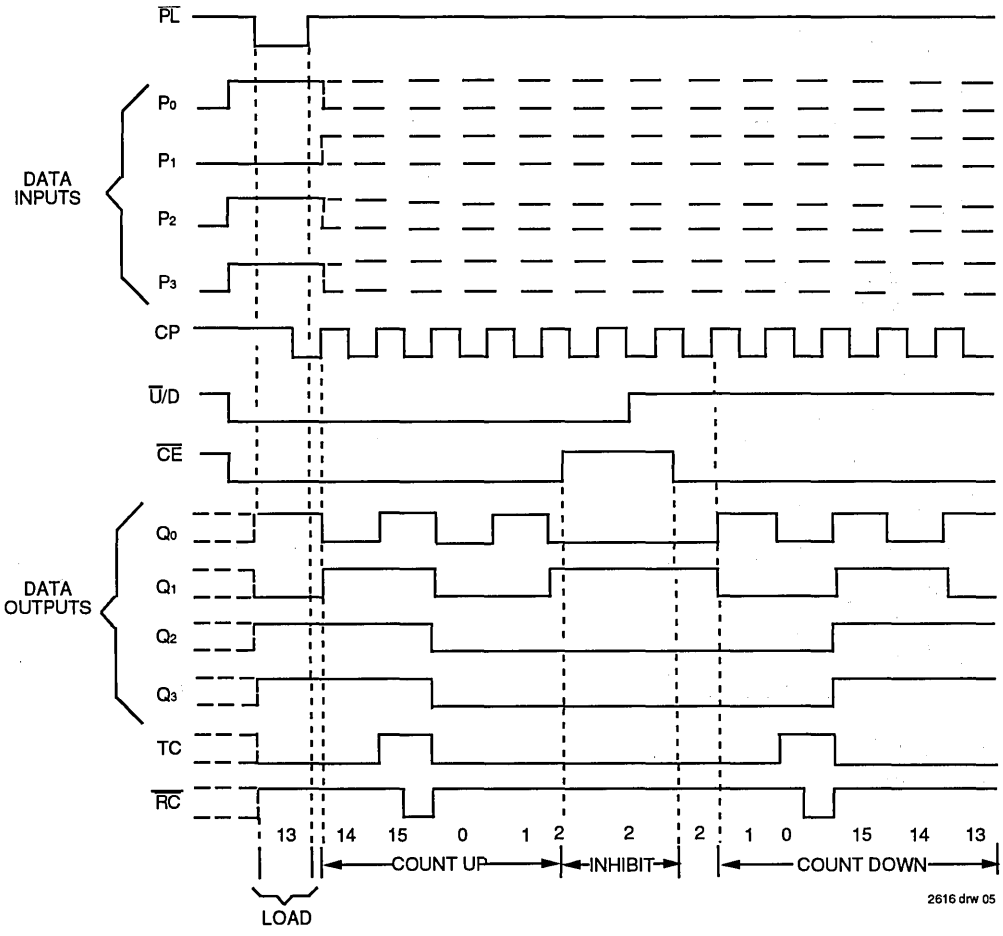
6

TIMING WAVEFORMS

Typical load, count, and inhibit sequences

Illustrated below is the following sequence:

- Load (preset) to binary thirteen
- Count up to fourteen, fifteen (maximum), zero, one and two
- Inhibit
- Count down to one, zero (minimum), fifteen, fourteen and thirteen



Integrated Device Technology, Inc.

FAST CMOS UP/DOWN BINARY COUNTER

IDT54/74FCT193
IDT54/74FCT193A

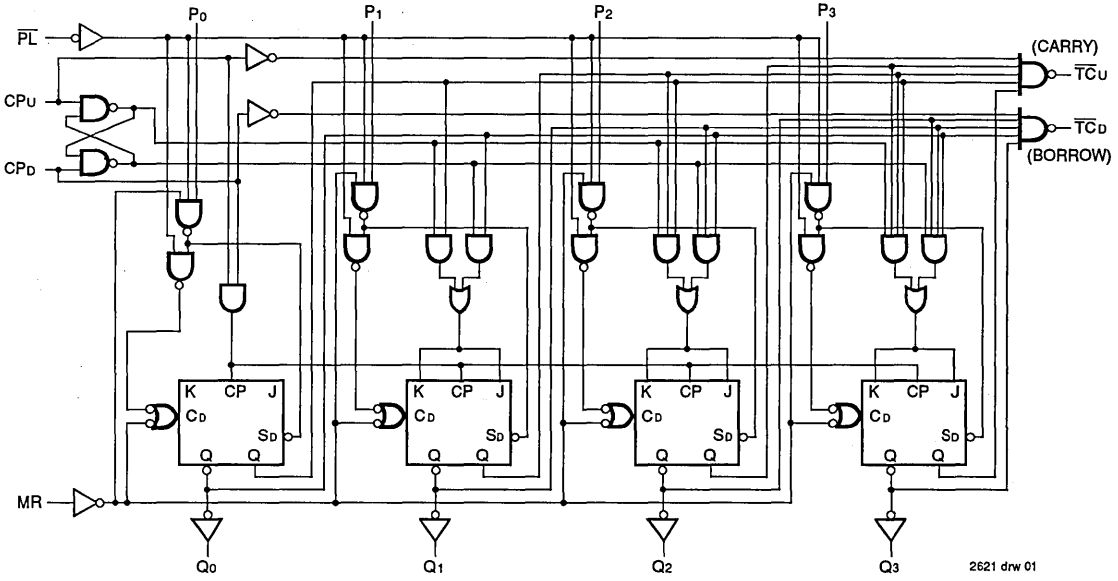
FEATURES:

- IDT54/74FCT193 equivalent to FAST™ speed
- **IDT54/74FCT193A 35% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- CMOS output level compatible
- Substantially lower input current levels than FAST (5µA max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT193 and IDT54/74FCT193A are up/down modulo-16 binary counters built using advanced CEMOS™, a dual metal CMOS technology. Separate count-up and count-down clocks are used and, in either counting mode, the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs. Separate terminal count-up and terminal count-down outputs are provided that are used as the clocks for subsequent stages without extra logic, thus simplifying multiusage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

FUNCTIONAL BLOCK DIAGRAM



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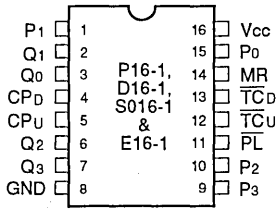
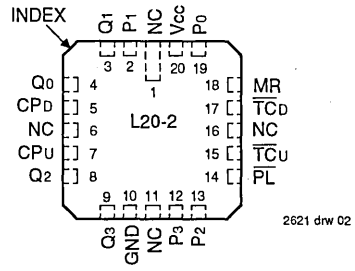
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
CPU	Count Up Clock Input (Active Rising Edge)
CPD	Count Down Clock Input (Active Rising Edge)
MR	Asynchronous Master Reset (Active HIGH)
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
Pn	Parallel Data Inputs
Qn	Flip-Flop Outputs
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)

2621 tbl 05

FUNCTION TABLE[1]

MR	$\overline{PL}$	CPU	CPD	Mode
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	↑	H	Count Up
L	H	H	↑	Count Down

NOTE: 2621 tbl 06

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Clock Transition.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
VTERM[3]	Terminal Voltage with Respect to GND	–0.5 to VCC	–0.5 to VCC	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

NOTES: 2621 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals.
3. Output and I/O terminals.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

NOTE: 2621 tbl 02

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military; T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	COM'L[5]	2.0V	—	—	V
			MIL	3.0V	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

2621 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. Clock pin requires a minimum V_{IH} of 2.7V.

6

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max., V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open Preset Mode $\overline{PL}$ = MR = CP_U = CP_D = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open Preset Mode $\overline{PL}$ = MR = CP_U = CP_D = GND One Bit Toggling at f_i = 10MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open Preset Mode $\overline{PL}$ = MR = CP_U = CP_D = GND Four Bits Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	4.2	10.5[5]	

NOTES:

2621 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT193				IDT54/74FCT193A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to $\overline{TC_U}$ or $\overline{TC_D}$	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	10.5	2.0	6.5	2.0	6.9	ns
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to Q_n		2.0	13.5	2.0	14.0	2.0	8.8	2.0	9.1	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		2.0	15.5	2.0	16.5	2.0	10.1	2.0	10.8	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		2.0	14.0	2.0	13.5	2.0	8.8	2.0	9.1	ns
t_{PHL}	Propagation Delay MR to Q_n		3.0	15.5	3.0	16.0	3.0	10.1	3.0	10.4	ns
t_{PLH}	Propagation Delay MR to $\overline{TC_U}$		3.0	14.5	3.0	15.0	3.0	9.4	3.0	9.8	ns
t_{PHL}	Propagation Delay MR to $\overline{TC_D}$		3.0	15.5	3.0	16.0	3.0	10.1	3.0	10.4	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to $\overline{TC_U}$ or $\overline{TC_D}$		3.0	16.5	3.0	18.5	3.0	10.8	3.0	12.0	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to $\overline{TC_U}$ or $\overline{TC_D}$		3.0	15.5	3.0	16.5	3.0	10.1	3.0	10.8	ns
t_{SU}	Set-up Time, HIGH or LOW P_n to $\overline{PL}$		5.0	—	6.0	—	4.0	—	5.0	—	ns
t_H	Hold Time, HIGH or LOW P_n to $\overline{PL}$		2.0	—	2.0	—	1.5	—	1.5	—	ns
t_W	$\overline{PL}$ Pulse Width, LOW		6.0	—	7.5	—	5.0	—	6.5	—	ns
t_W	CP_U or CP_D Pulse Width HIGH or LOW		5.0	—	7.0	—	4.0[3]	—	6.0	—	ns
t_W	CP_U or CP_D Pulse Width LOW (Change of Direction)		10.0	—	12.0	—	8.0	—	10.0	—	ns
t_W	MR Pulse Width HIGH		6.0	—	6.0	—	5.0	—	5.0	—	ns
t_{REM}	Recovery Time $\overline{PL}$ to CP_U or CP_D		6.0	—	8.0	—	5.0	—	7.0	—	ns
t_{REM}	Recovery Time MR to CP_U or CP_D		4.0	—	4.5	—	3.0	—	3.5	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2621 tbl 07

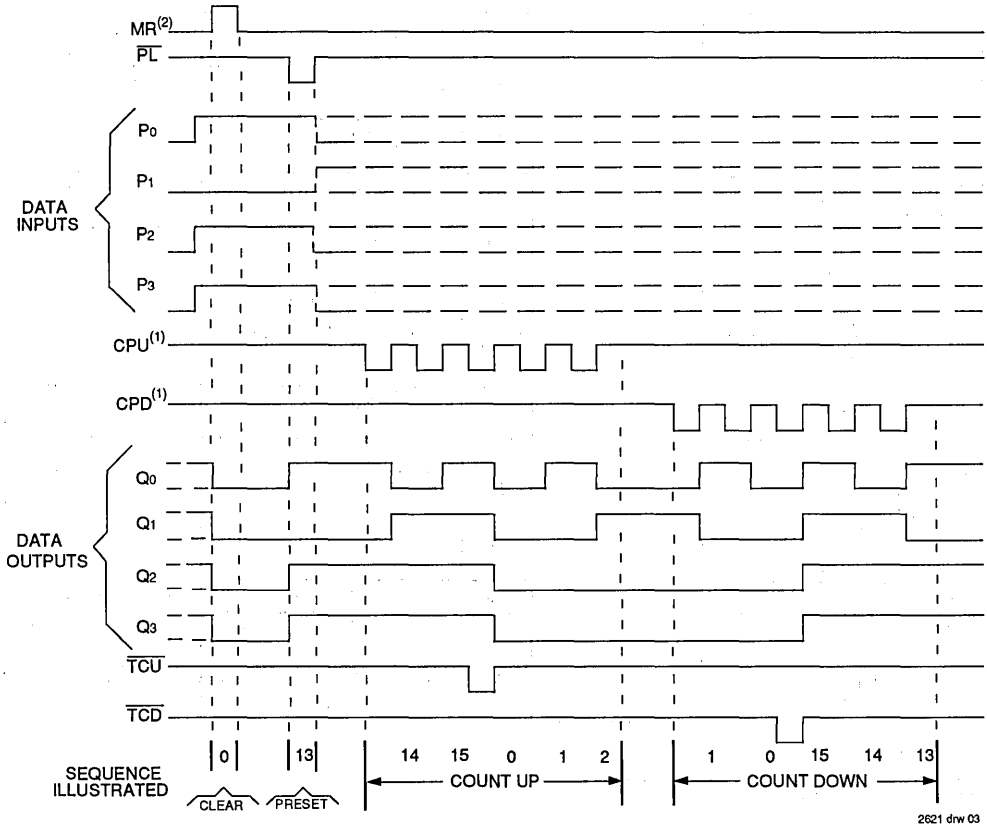
6

TIMING WAVEFORMS

Typical clear, load, and count sequences

Illustrated below is the following sequence:

- Clear outputs to zero
- Load (preset) to binary thirteen
- Count up to fourteen, fifteen, carry zero, one and two
- Count down to one, zero, borrow, fifteen, fourteen and thirteen



NOTES:

1. MR overrrides load, data, and count inputs
2. When counting up, CPD input must be HIGH; when counting down, CPU input must be HIGH.

Integrated Device Technology, Inc.

FAST CMOS OCTAL BUFFER/LINE DRIVER

IDT54/74FCT240/A/C
IDT54/74FCT241/A/C
IDT54/74FCT244/A/C
IDT54/74FCT540/A/C
IDT54/74FCT541/A/C

FEATURES:

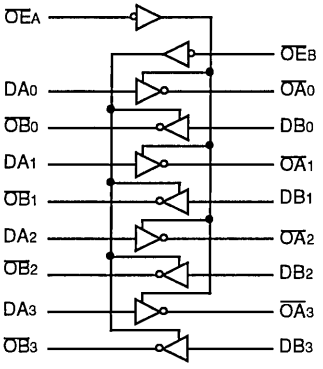
- IDT54/74FCT240/241/244/540/541 equivalent to FAST™ speed and drive
- **IDT54/74FCT240A/241A/244A/540A/541A 25% faster than FAST**
- **IDT54/74FCT240C/241C/244C/540C/541C up to 55% faster than FAST**
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (1mW typ. static)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Meets or exceeds JEDEC Standard 18 specifications

DESCRIPTION:

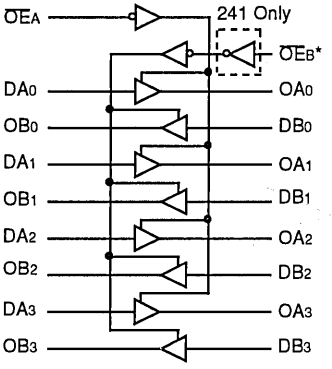
The IDT octal buffer/line drivers are built using advanced CEMOS™ a dual metal CMOS technology. The IDT54/74FCT240/A/C, IDT54/74FCT241/A/C and IDT54/74FCT244/A/C are designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitter/receivers which provide improved board density.

The IDT54/74FCT540/A/C and IDT54/74FCT541/A/C are similar in function to the IDT54/74FCT240/A/C and IDT54/74FCT244/A/C, respectively, except that the inputs and outputs are on opposite sides of the package. This pinout arrangement makes these devices especially useful as output ports for microprocessors and as backplane drivers, allowing ease of layout and greater board density.

FUNCTIONAL BLOCK DIAGRAMS

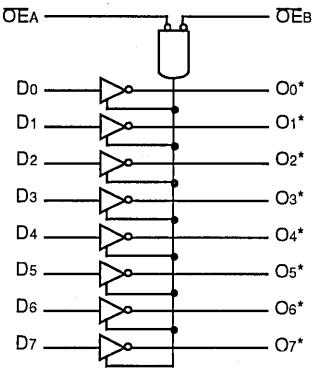


IDT54/74FCT240



IDT54/74FCT241/244

*$\overline{OE}_B$ for 241, $\overline{OE}_B$ for 244



IDT54/74FCT540/541

*Logic diagram shown for 'FCT540. 'FCT541 is the non-inverting option.

2606 dwg 01-03

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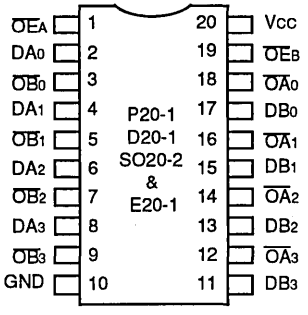
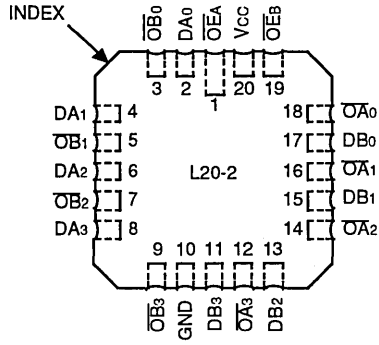
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS

IDT54/74FCT240

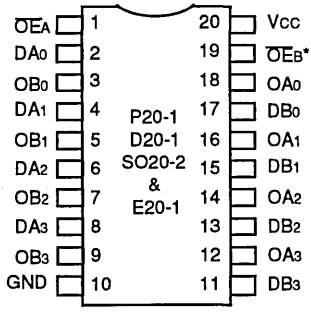


DIP/SOIC/CERPACK
TOP VIEW

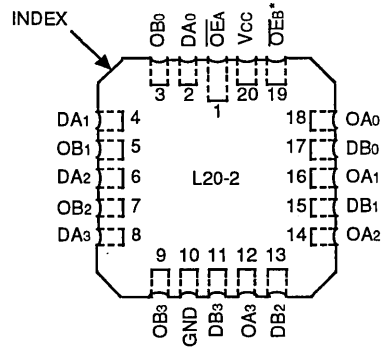


LCC
TOP VIEW

IDT54/74FCT241/244



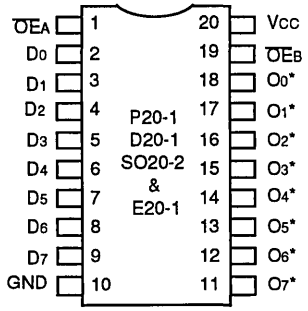
DIP/SOIC/CERPACK
TOP VIEW



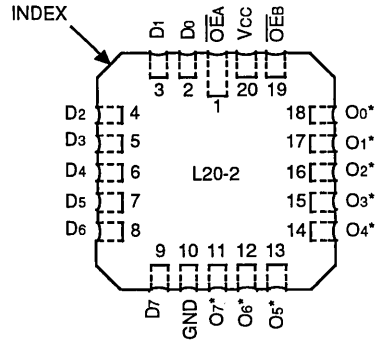
LCC
TOP VIEW

*OEB for 241, $\overline{OE_B}$ for 244

IDT54/74FCT540/541



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

*Ox for 540, Ox for 541

2606 cnv* 04-09

PIN DESCRIPTION

Pin Names	Description
$\overline{OE_A}$, $\overline{OE_B}$	3-State Output Enable Inputs (Active LOW)
OE_B[1]	3-State Output Enable Input (Active HIGH)
Dxx	Inputs
Oxx	Outputs

NOTE: 2606 tbl 04
1. OE_B for 241 only.

FUNCTION TABLE

Inputs[1]				Outputs[1]				
$\overline{OE_A}$	$\overline{OE_B}$	OE_B[2]	D	240	241	244	540	541
L	L	H	L	H	L	L	H	L
L	L	H	H	L	H	H	L	H
H	H	L	X	Z	Z	Z	Z	Z

NOTES: 2606 tbl 05
1. H = High Voltage Level
   X = Don't Care
   L = Low Voltage Level
   Z = High Impedance
2. OE_B for 241 only.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2606 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter (1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2606 tbl 02
1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	10	µA
			V_O = 2.7V	—	—	10[4]	
I_{OZL}			V_O = 0.5V	—	—	–10[4]	
			V_O = GND	—	—	–10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
			I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}[4]	
			I_{OL} = 48mA MIL.	—	0.3	0.55	
			I_{OL} = 64mA COM'L.	—	0.3	0.55	

2606 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND or $\overline{OE}_A$ = GND, OE_B = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current [6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
		$\overline{OE}_A$ = $\overline{OE}_B$ = GND or $\overline{OE}_A$ = GND, OE_B = V_{CC} One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open fi = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5[5]	
		$\overline{OE}_A$ = $\overline{OE}_B$ = GND or $\overline{OE}_A$ = GND, OE_B = V_{CC} Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2606 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT240[1,2]

Symbol	Parameter	Condition	54/74FCT240				54/74FCT240A				54/74FCT240C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay DN to ON	CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	1.5	4.3	1.5	4.7	ns
tPZH tPZL	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns

2606 tbl 07

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT241 AND FCT244[1,2]

Symbol	Parameter	Condition	54/74FCT241/244				54/74FCT241A/244A				54/74FCT241C/244C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay DN to ON	CL = 50pF RL = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	1.5	4.1	1.5	4.6	ns
tPZH tPZL	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns

2606 tbl 08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT540 AND FCT541[1,2]

Symbol	Parameter	Condition	54/74FCT540/541				54/74FCT540A/541A				54/74FCT540C/541C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay DN to ON IDT54/74FCT540	CL = 50pF RL = 500Ω	1.5	8.5	1.5	9.5	1.5	4.8	1.5	5.1	1.5	4.3	1.5	4.7	ns
tPLH tPHL	Propagation Delay DN to ON IDT54/74FCT541		1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	1.5	4.1	1.5	4.6	ns
tPZH tPZL	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2606 tbl 09

Integrated Device Technology, Inc.

FAST CMOS OCTAL BIDIRECTIONAL TRANSCEIVERS

IDT54/74FCT245/A/C
IDT54/74FCT640/A/C
IDT54/74FCT645/A/C

FEATURES:

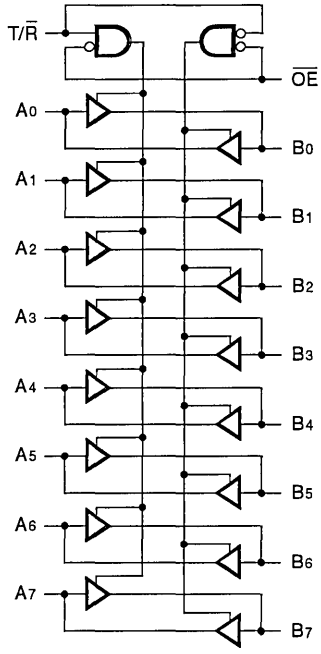
- IDT54/74FCT245/640/645 equivalent to FAST™ speed and drive
- **IDT54/74FCT245A/640A/645A 25% faster than FAST**
- **IDT54/74FCT245C/640C/645C 40% faster than FAST**
- TTL input and output level compatible
- CMOS output level compatible
- IOL = 64mA (commercial) and 48mA (military)
- Input current levels only 5µA max.
- CMOS power levels (2.5mW typical static)
- Direction control and over-riding 3-state control
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed
- Meets or exceeds JEDEC Standard 18 specifications

DESCRIPTION:

The IDT octal bidirectional transceivers are built using advanced CEMOS™, a dual-metal CMOS technology. The IDT54/74FCT245/A/C, IDT54/74FCT640/A/C and IDT54/74FCT645/A/C are designed for asynchronous two-way communication between data buses. The transmit/receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports, and receive (active LOW) from B ports to A ports. The output enable ($\overline{OE}$) input, when HIGH, disables both A and B ports by placing them in High-Z condition.

The IDT54/74FCT245/A/C and IDT54/74FCT645/A/C transceivers have non-inverting outputs. The IDT54/74FCT640/A/C has inverting outputs.

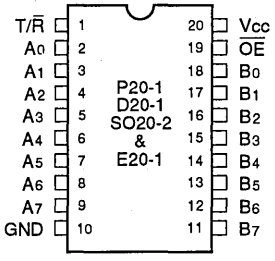
FUNCTIONAL BLOCK DIAGRAM



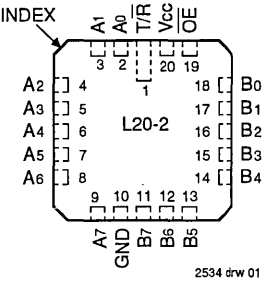
2534 drw 02

NOTES:
1. FCT245, 645 are noninverting options.
2. FCT640 is the inverting option.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2534 drw 01

LCC
TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or 3-State Outputs
B_0–B_7	Side B Inputs or 3-State Outputs

2534 tbl 05

FUNCTION TABLE[2]

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A[1]
L	H	Bus A Data to Bus B[1]
H	X	High Z State

2534 tbl 06

NOTES:
1. 640 is inverting from input to output.
2. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2534 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Inputs and V_{CC} terminals.
3. Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2534 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max	V_I = V_{CC}	—	—	15	µA
			V_I = 2.7V	—	—	15[4]	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	—	—	–15[4]	
			V_I = GND	—	—	–15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
			I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage (Port A and Port B)	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}[4]	
			I_{OL} = 48mA MIL.	—	0.3	0.55	
			I_{OL} = 64mA COM'L.	—	0.3	0.55	

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

2534 tbl 03

6

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.5	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	2.0	4.0	mA
		50% Duty Cycle T/$\overline{R}$ = $\overline{OE}$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.3	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.5	6.5[5]	
		50% Duty Cycle T/$\overline{R}$ = $\overline{OE}$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	5.5	14.5[5]	

2534 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT245/A/C

			54/74FCT245				54/74FCT245A				54/74FCT245C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
tPLH tPHL	Propagation Delay A to B, B to A	CL = 50 pF RL = 500Ω	1.5	7.0	1.5	7.5	1.5	4.6	1.5	4.9	1.5	4.1	1.5	4.5	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to A or B		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to A or B		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns
tPZH tPZL	Output EnableTime T/$\overline{R}$ to A or B[3]		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time T/$\overline{R}$ to A or B[3]		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns

2534 tbl 07

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT640/A/C

			54/74FCT640				54/74FCT640A				54/74FCT640C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
tPLH tPHL	Propagation Delay A to B, B to A	CL = 50 pF RL = 500Ω	2.0	7.0	2.0	8.0	1.5	5.0	1.5	5.3	1.5	4.4	1.5	4.7	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to A or B		2.0	13.0	2.0	16.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to A or B		2.0	10.0	2.0	12.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns
tPZH tPZL	Output Enable Time T/$\overline{R}$ to A or B[3]		2.0	13.0	2.0	16.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time T/$\overline{R}$ to A or B[3]		2.0	10.0	2.0	12.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns

2534 tbl 08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT645/A/C

			54/74FCT645				54/74FCT645A				54/74FCT645C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
tPLH tPHL	Propagation Delay A to B, B to A	CL = 50 pF RL = 500Ω	1.5	9.5	1.5	11.0	1.5	4.6	1.5	4.9	1.5	4.1	1.5	4.5	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to A or B		1.5	11.0	1.5	12.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to A or B		1.5	12.0	1.5	13.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns
tPZH tPZL	Output Enable Time T/$\overline{R}$ to A or B[3]		1.5	11.0	1.5	12.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time T/$\overline{R}$ to A or B[3]		1.5	12.0	1.5	13.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns

NOTES:

2534 tbl 09

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

6

Integrated Device Technology, Inc.

FAST CMOS OCTAL FLIP-FLOP WITH MASTER RESET

IDT54/74FCT273
IDT54/74FCT273A
IDT54/74FCT273C

FEATURES:

- IDT54/74FCT273 equivalent to FAST™ speed;
- **IDT54/74FCT273A 45% faster than FAST**
- **IDT54/74FCT273C 55% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST (5µA max.)
- Octal D flip-flop with Master Reset
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

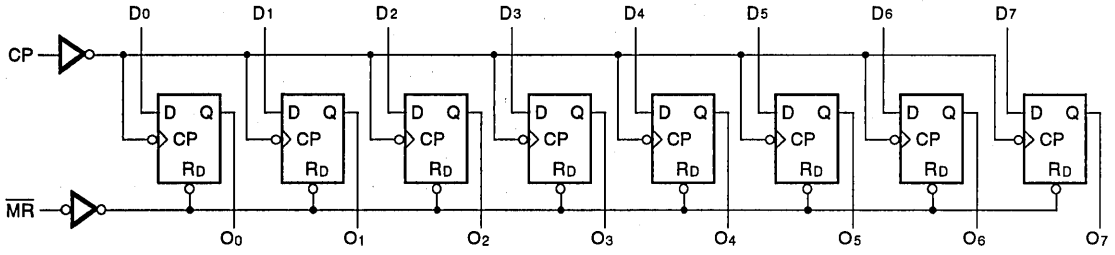
DESCRIPTION:

The IDT54/74FCT273/A/C are octal D flip-flops built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT273/A/C have eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output.

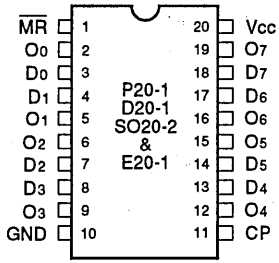
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

FUNCTIONAL BLOCK DIAGRAM

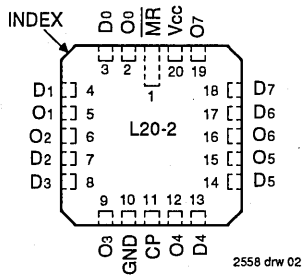


2558 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK TOP VIEW



2558 drw 02

LCC TOP VIEW

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FAST is a trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
D_N	Data Input
$\overline{MR}$	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
O_N	Data Outputs

2558 tbl 05

FUNCTION TABLE

	Inputs			Outputs
Operating Mode	$\overline{MR}$	CP	D_N	O_N
Reset (Clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

2558 tbl 06

NOTES:
H = HIGH voltage level steady-state
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level steady state
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
X = Don't care
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2558 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2558 tbl 02

1. This parameter is guaranteed by characterization data and not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

2558 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{MR}$ = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{MR}$ = V_{CC} One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{MR}$ = V_{CC} Eight Bits Toggling f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

NOTES:

2558 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT273				IDT54/74FCT273A				IDT54/74FCT273C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	C_L = 50 pF R_L = 500Ω	2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	5.8	2.0	6.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Output		2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	6.1	2.0	6.8	ns
t_{SU}	Set-up Time HIGH or LOW Data to CP		3.0	—	3.5	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW Data to CP		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	Clock Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
t_W	$\overline{MR}$ Pulse Width LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
t_{REM}	Recovery Time $\overline{MR}$ to CP		4.0	—	5.0	—	2.0	—	2.5	—	2.0	—	2.5	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2558 tbl 07

Integrated Device Technology, Inc.

FAST CMOS 8-INPUT UNIVERSAL SHIFT REGISTER

IDT54/74FCT299
IDT54/74FCT299A
IDT54/74FCT299C

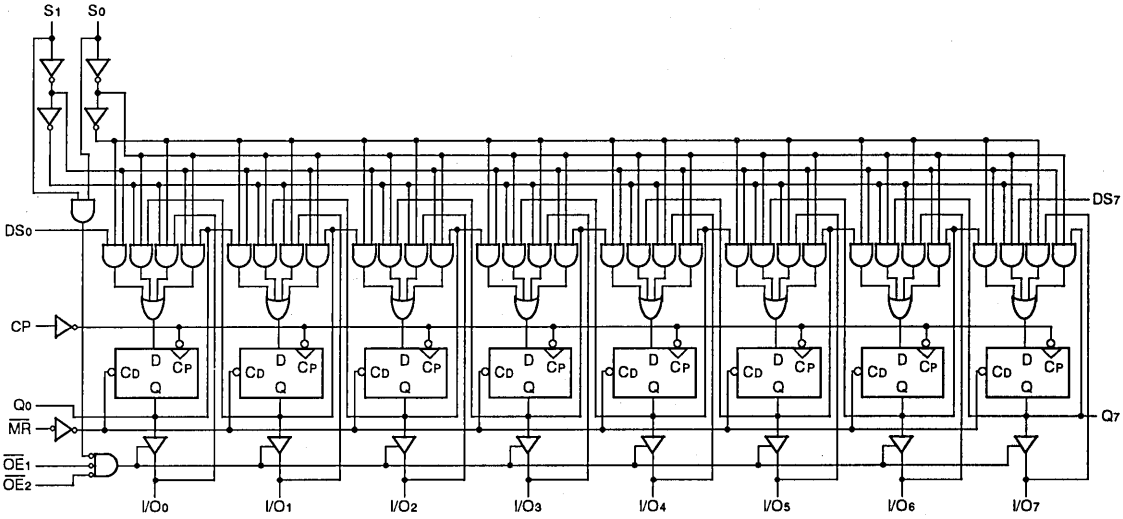
FEATURES:

- IDT54/74FCT299 equivalent to FAST™ speed
- **IDT54/74FCT299A 25% faster than FAST**
- **IDT54/74FCT299C 35% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST (5μA max.)
- 8-input universal shift register
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86862 is listed on this function. Refer to section 2.

DESCRIPTION:

The IDT54/74FCT299 and IDT54/74FCT299A/C are built using advanced CEMOS™, a dual-metal CMOS technology. The IDT54/74FCT299 and IDT54/74FCT299A/C are 8-input universal shift/storage registers with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

FUNCTIONAL BLOCK DIAGRAM



2561 drw 01

6

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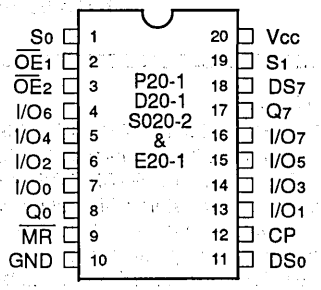
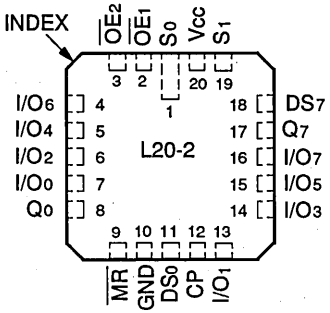
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2561 drw 02

LCC
TOP VIEW

2561 drw 02

PIN DESCRIPTION

Pin Names	Description
CP	Clock Pulse Input (Active Edge Rising)
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE_1}$, $\overline{OE_2}$	3-State Output Enable Inputs (Active LOW)
I/O_0–I/O_7	Parallel Data Inputs or 3-State Parallel Outputs
Q_0, Q_7	Serial Outputs

2561 tbl 05

FUNCTION TABLE[1]

Inputs				
$\overline{MR}$	S_1	S_0	CP	Response
L	X	X	X	Asynchronous Reset Q_0–Q_7 = LOW
H	H	H	↑	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	↑	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	↑	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH clock transition

2561 tbl 06

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:

2561 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5 unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

2561 tbl 02

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current (Except I/O Pins)		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
I_{IH}	Input HIGH Current (I/O Pins Only)	V_{CC} = Max.	V_I = V_{CC}	—	—	15	µA
			V_I = 2.7V	—	—	15[4]	
I_{IL}	Input LOW Current (I/O Pins Only)		V_I = 0.5V	—	—	–15[4]	
			V_I = GND	—	—	–15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
			I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}[4]	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

2561 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

6

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE_1}$ = $\overline{OE_2}$ = GND $\overline{MR}$ = V_{CC} S_0 = S_1 = V_{CC} DS_0 = DS_1 = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE_1}$ = $\overline{OE_2}$ = GND $\overline{MR}$ = V_{CC} S_0 = S_1 = V_{CC} DS_0 = DS_7 = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE_1}$ = $\overline{OE_2}$ = GND $\overline{MR}$ = V_{CC} S_0 = S_1 = V_{CC} DS_0 = DS_7 = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

2561 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT299				IDT54/74FCT299A				IDT54/74FCT299C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	14.0	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n		2.0	12.0	2.0	12.0	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7		2.0	10.0	2.0	10.5	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n		2.0	15.0	2.0	15.0	2.0	8.7	2.0	11.5	2.0	6.5	2.0	7.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE_n}$ to I/O_n		1.5	11.0	1.5	15.0	1.5	6.5	1.5	7.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE_n}$ to I/O_n		1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	1.5	6.0	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW S_0 or S_1 to CP		7.5	—	7.5	—	3.5	—	4.0	—	3.5	—	4.0	—	ns
t_H	Hold Time HIGH or LOW S_0 or S_1 to CP		1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
t_{SU}	Set-up Time HIGH or LOW I/O_n, DS_0 or DS_7 to CP		5.5	—	5.5	—	4.0	—	4.5	—	4.0	—	4.5	—	ns
t_H	Hold Time HIGH or LOW I/O_n, DS_0 or DS_7 to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	CP Pulse width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns
t_W	$\overline{MR}$ Pulse Width LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns
t_{REM}	Recovery Time $\overline{MR}$ to CP		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2561 tbl 07

6

Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSPARENT LATCHES

IDT54/74FCT373/A/C
IDT54/74FCT533/A/C
IDT54/74FCT573/A/C

FEATURES

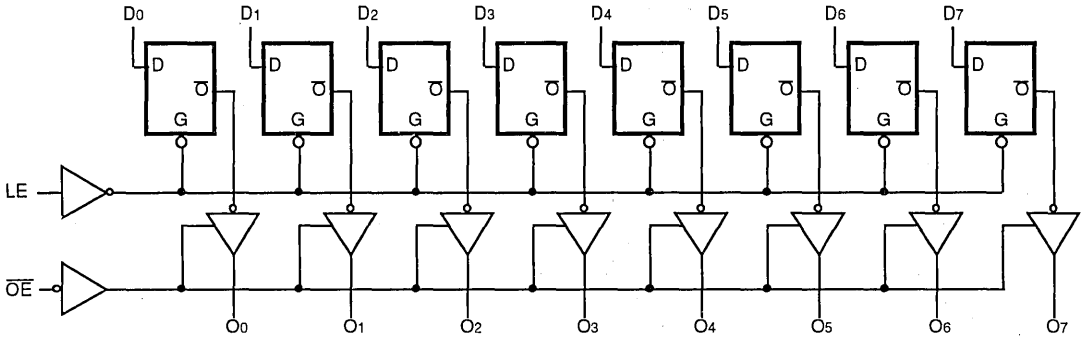
- IDT54/74FCT373/533/573 equivalent to FAST™ speed and drive
- **IDT54/74FCT373A/533A/573A up to 30% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- Octal transparent latch with 3-state output control
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION

The IDT54/74FCT373/A/C, IDT54/74FCT533/A/C and IDT54/74FCT573/A/C are octal transparent latches built using advanced CEMOS™, a dual metal CMOS technology. These octal latches have 3-state outputs and are intended for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high-impedance state.

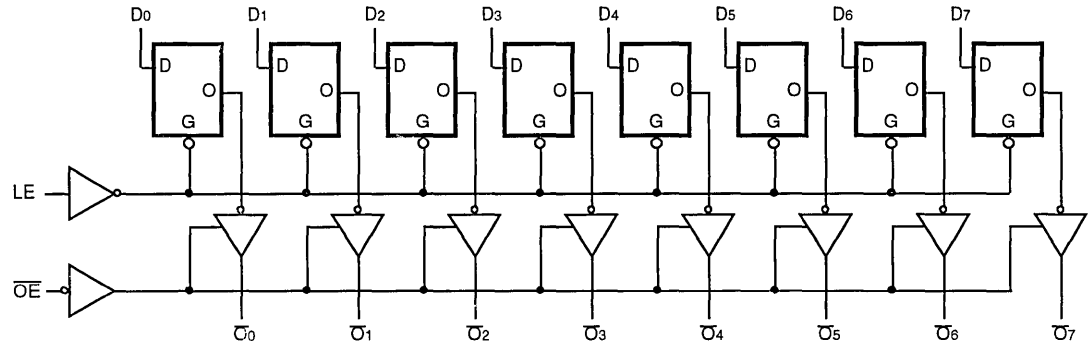
FUNCTIONAL BLOCK DIAGRAMS

IDT54/74FCT373 AND IDT54/74FCT573



2602 cnv* 01

IDT54/74FCT533



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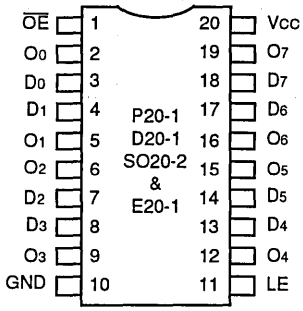
FAST is a trademark of National Semiconductor Co.

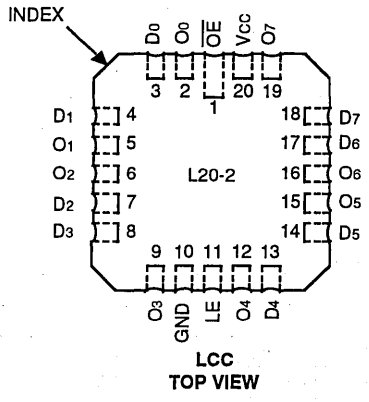
2602 cnv* 02

PIN CONFIGURATIONS

IDT54/74FCT373

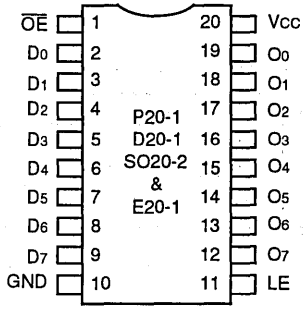


DIP/SOIC/CERPACK
TOP VIEW

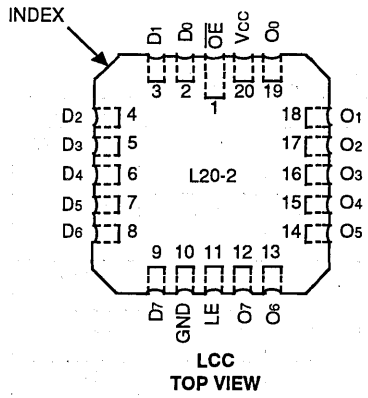


LCC
TOP VIEW

IDT54/74FCT573

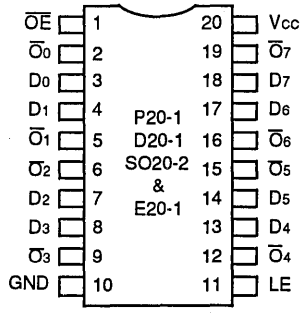


DIP/SOIC/CERPACK
TOP VIEW

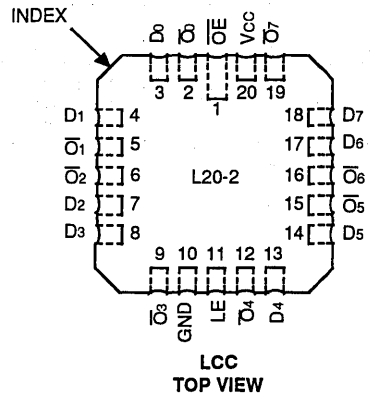


LCC
TOP VIEW

IDT54/74FCT533



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

2602 cnv* 03-08

6

FUNCTION TABLE (FCT533)[1]

Inputs			Outputs
D_N	LE	$\overline{OE}$	$\overline{O}_N$
H	H	L	L
L	H	L	H
X	X	H	Z

2602 tbl 05

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

FUNCTION TABLE (FCT373 and FCT573)[1]

Inputs			Outputs
D_N	LE	$\overline{OE}$	O_N
H	H	L	H
L	H	L	L
X	X	H	Z

2602 tbl 06

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

PIN DESCRIPTION

Pin Names	Description
D_N	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
O_N	3-State Outputs
$\overline{O}_N$	Complementary 3-State Outputs

2602 tbl 07

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

2602 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2602 tbl 02

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	10	µA
			V_O = 2.7V	—	—	10[4]	
I_{OZL}			V_O = 0.5V	—	—	–10[4]	
			V_O = GND	—	—	–10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
			I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}[4]	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

2602 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
		50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5[5]	
		50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2602 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT373/A/C/FCT573/A/C

Symbol	Parameter	Conditions[1]	FCT373/573				FCT373A/573A				FCT373C/573C				Unit
			Com'l.[2]		Mil.[2]		Com'l.[2]		Mil.[2]		Com'l.[2]		Mil.[2]		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	8.5	1.5	5.2	1.5	5.6	1.5	4.2	1.5	5.1	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_N		2.0	13.0	2.0	15.0	2.0	8.5	2.0	9.8	2.0	5.5	2.0	8.0	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	12.0	1.5	13.5	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.5	1.5	10.0	1.5	5.5	1.5	6.5	1.5	5.0	1.5	5.9	ns
t_{SU}	Set-up Time HIGH or LOW, D_N to LE		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, D_N to LE		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	LE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

2602 tbl 08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT533/A/C

Symbol	Parameter	Conditions[1]	FCT533				FCT533A				FCT533C				Unit
			Com'l.[2]		Mil.[2]		Com'l.[2]		Mil.[2]		Com'l.[2]		Mil.[2]		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay $\overline{D_N}$ to $\overline{O_N}$	C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	12.0	1.5	5.2	1.5	5.6	1.5	4.7	1.5	5.1	ns
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O_N}$		2.0	13.0	2.0	14.0	2.0	8.5	2.0	9.8	2.0	6.9	2.0	8.0	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	11.0	1.5	12.5	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	1.5	8.5	1.5	5.5	1.5	6.5	1.5	5.0	1.5	5.9	ns
t_{SU}	Set-up Time HIGH or LOW, D_N to LE		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, D_N to LE		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	LE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2602 tbl 09

6

Integrated Device Technology, Inc.

FAST CMOS OCTAL D REGISTERS (3-STATE)

IDT54/74FCT374/A/C
IDT54/74FCT534/A/C
IDT54/74FCT574/A/C

FEATURES:

- IDT54/74FCT374/534/574 equivalent to FAST™ speed and drive
- **IDT54/74FCT374A/534A/574A up to 30% faster than FAST**
- **IDT54/74FCT374C/534C/574C up to 50% faster than FAST**
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- Edge triggered master/slave, D-type flip-flops
- Buffered common clock and buffered common three-state control
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B
- Meets or exceeds JEDEC Standard 18 specifications

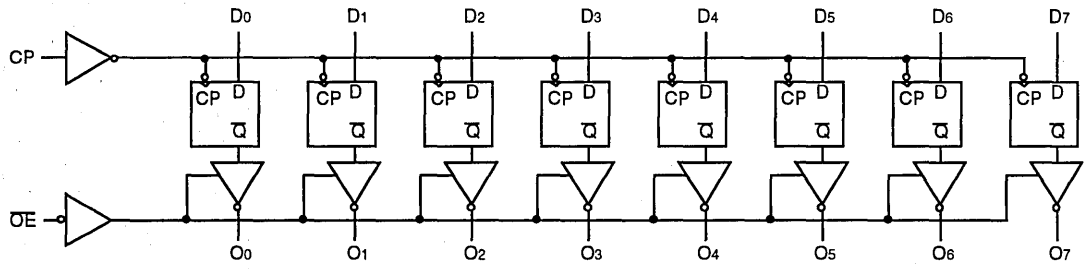
DESCRIPTION:

The IDT54/74FCT374/A/C, IDT54/74FCT534/A/C and IDT54/74FCT574/A/C are 8-bit registers built using advanced CEMOS™, a dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered 3-state output control. When the output enable ($\overline{OE}$) is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the high-impedance state.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

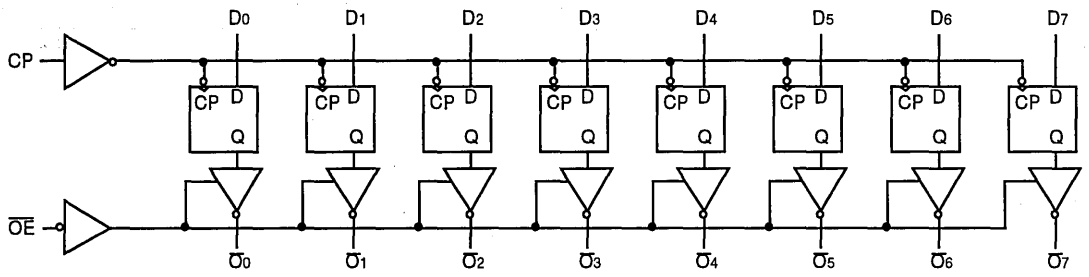
The IDT54/74FCT374/A/C and IDT54/74FCT574/A/C have non-inverting outputs with respect to the data at the D inputs. The IDT54/74FCT534/A/C have inverting outputs.

FUNCTIONAL BLOCK DIAGRAM IDT54/74FCT374 AND IDT54/74FCT574



2603 cnv* 01

FUNCTIONAL BLOCK DIAGRAM IDT54/74FCT534



2603 cnv* 02

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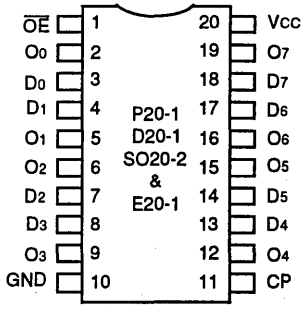
FAST is a trademark of National Semiconductor, Inc.

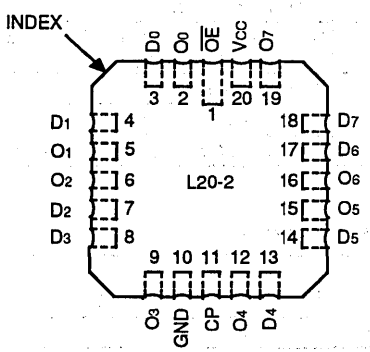
PIN CONFIGURATIONS

IDT54/74FCT374



2603 cnv* 03

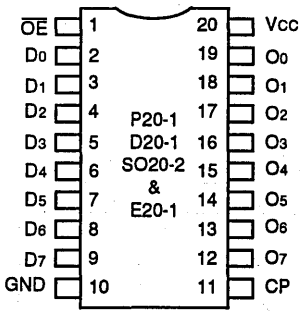
DIP/SOIC/CERPACK
TOP VIEW



2603 cnv* 04

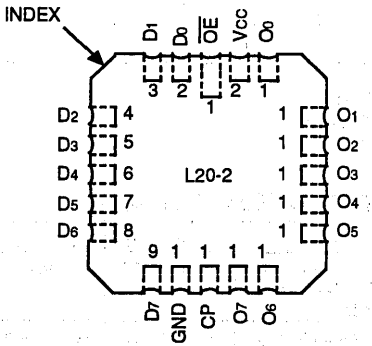
LCC
TOP VIEW

IDT54/74FCT574



2603 cnv* 05

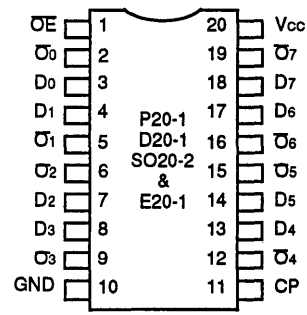
DIP/SOIC/CERPACK
TOP VIEW



2603 cnv* 06

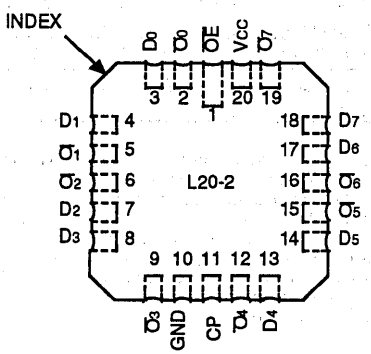
LCC
TOP VIEW

IDT54/74FCT534



2603 cnv* 07

DIP/SOIC/CERPACK
TOP VIEW



2603 cnv* 08

LCC
TOP VIEW

6

PIN DESCRIPTION

Pin Names	Description
D_N	D flip-flop data inputs.
CP	Clock Pulse for the register. Enters data on LOW-to-HIGH transition.
O_N	3-state outputs, (true).
$\overline{O_N}$	3-state outputs, (inverted).
$\overline{OE}$	Active LOW 3-state Output Enable input.

2603 tbl 06

FUNCTION TABLE[1]

Function	Inputs			FCT534 Outputs	FCT534 Internal	FCT374/574 Outputs	FCT374/574 Internal
	$\overline{OE}$	CP	D_N	$\overline{O_N}$	Q_N	O_N	$\overline{Q_N}$
Hi-Z	H	L	X	Z	NC	Z	NC
	H	H	X	Z	NC	Z	NC
Load Register	L	↑	L	H	L	L	H
	L	↑	H	L	H	H	L
	H	↑	L	Z	L	Z	H
	H	↑	H	Z	H	Z	L

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   NC = No Change
   ↑ = LOW-to-HIGH transition

2603 tbl 05

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2603 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2603 tbl 02
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	10	µA
			V_O = 2.7V	—	—	10[4]	
I_{OZL}			V_O = 0.5V	—	—	–10[4]	
			V_O = GND	—	—	–10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
			I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}[4]	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

2603 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

6

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND f_i = 5MHz 50% Duty Cycle One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

2603 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions[1]	FCT374/534/574				FCT374A/534A/574A				FCT374C/534C/574C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_N[3]	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	11.0	2.0	6.5	2.0	7.2	2.0	5.2	2.0	6.2	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	12.5	1.5	14.0	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	8.0	1.5	8.0	1.5	5.5	1.5	6.5	1.5	5.0	1.5	5.7	ns
t_{SU}	Set-up Time HIGH or LOW, D_N to CP		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, D_N to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

2603 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. O_N for FCT374 and FCT574, O_N for FCT534.

6

Integrated Device Technology, Inc.

FAST CMOS OCTAL D FLIP-FLOP WITH CLOCK ENABLE

IDT54/74FCT377
IDT54/74FCT377A
IDT54/74FCT377C

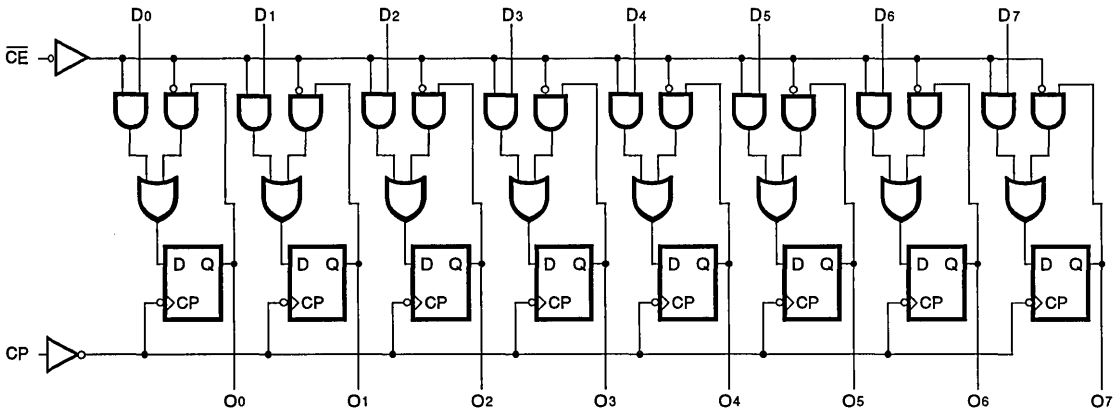
FEATURES:

- IDT54/74FCT377 equivalent to FAST™ speed
- **IDT54/74FCT377A 25% faster than FAST**
- **IDT54/74FCT377C 40% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- I_{IH} and I_{IL} only 5µA max.
- CMOS power levels (1mW typ. static)
- CMOS output level compatible
- Meets or exceeds JEDEC Standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

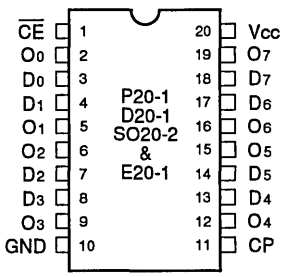
The IDT54/74FCT377/A/C is an octal D flip-flop built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT377/A/C have eight edge-triggered, D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is LOW. The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The $\overline{CE}$ input must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

FUNCTIONAL BLOCK DIAGRAM

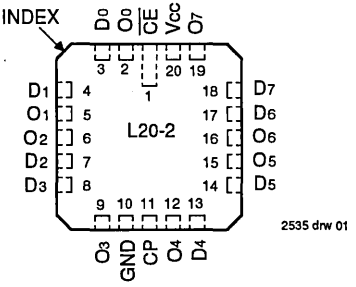


2535 drw 02

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2535 drw 01

LCC
TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
O_0–O_7	Data Outputs
CP	Clock Pulse Input

2535 tbl 05

FUNCTION TABLE[1]

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D	O
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (Do Nothing)	↑	h	X	No Change
	H	H	X	No Change

2535 tbl 06

NOTE:
1. H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH Clock Transition
   L = LOW voltage level
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH Clock transition
   X = Immaterial
   ↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

2535 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2535 tbl 02

NOTE:
1. This parameter is guaranteed but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

2535 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{CE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{CE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{CE}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

2535 tbl 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT377				IDT54/74FCT377A				IDT54/74FCT377C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to On	CL = 50pF RL = 500Ω	2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	5.2	2.0	5.5	ns
tSU	Set-up Time HIGH or LOW Dn to CP		2.5	—	3.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW Dn to CP		2.0	—	2.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tSU	Set-up Time HIGH or LOW $\overline{CE}$ to CP		4.0	—	4.0	—	3.5	—	3.5	—	3.5	—	3.5	—	ns
tH	Hold Time HIGH or LOW $\overline{CE}$ to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	Clock Pulse Width, HIGH or LOW		7.0	—	7.0	—	6.0	—	7.0	—	6.0	—	7.0	—	ns

NOTES:

2535 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

Integrated Device Technology, Inc.

FAST CMOS QUAD DUAL-PORT REGISTER

IDT54/74FCT399
IDT54/74FCT399A
IDT54/74FCT399C

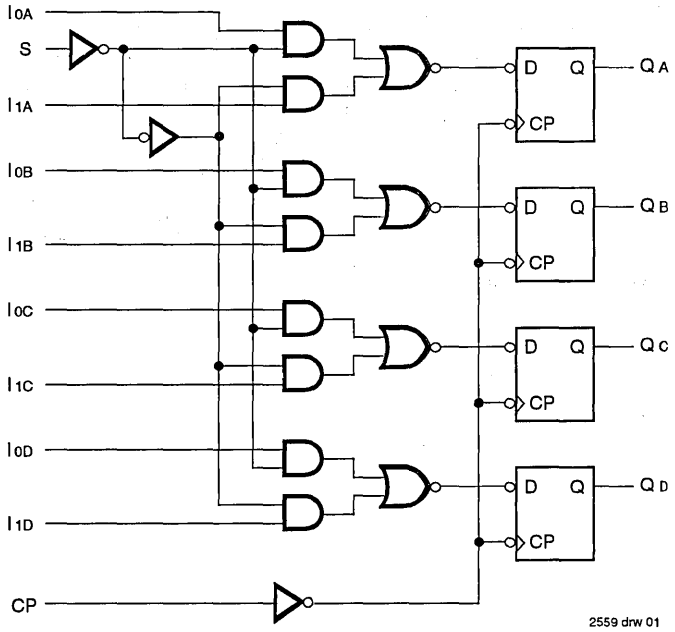
FEATURES:

- IDT54/74FCT399 equivalent to FAST™ speed
- **IDT54/74FCT399A 30% faster than FAST**
- **IDT54/74FCT399C 45% faster than FAST**
- Equivalent to FAST pinout/function and output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA (commercial) and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT399/A/C are high-speed quad dual-port registers. The register selects four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0X}, I_{1X}) and Select input (S) must be stable only one set-up time prior to, and hold time after, the LOW-to-HIGH transition of the Clock input for predictable operation.

FUNCTIONAL BLOCK DIAGRAM



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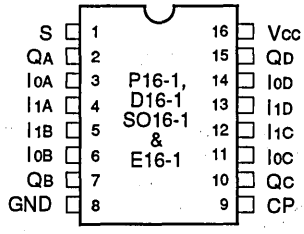
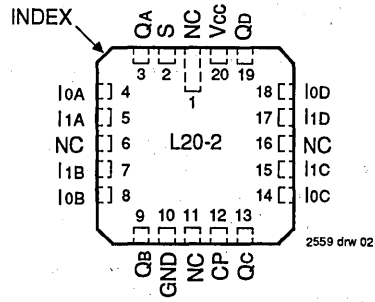
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
S	Common Select Input
CP	Clock Pulse Input (Active Rising Edge)
$I_{0A} - I_{0D}$	Data Inputs from Source 0
$I_{1A} - I_{1D}$	Data Inputs from Source 1
$Q_A - Q_D$	Register True Outputs

2559 tbl 03

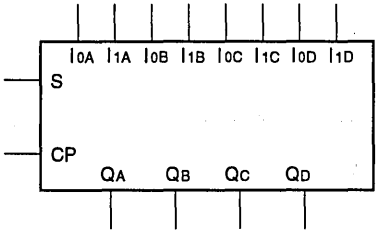
FUNCTION TABLE[1]

Inputs			Outputs
S	I_0	I_1	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

2559 tbl 04

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   h = HIGH Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
   l = LOW Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
   X = Immaterial

LOGIC SYMBOL



2559 drw 03

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2559 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2559 tbl 02
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5(4)	
			V_I = GND	—	—	–5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
			I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}(4)	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES: 2559 tbl 05
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

6

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle One Bit Toggling at f_i = 5MHz 50% Duty Cycle S = Steady State	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle Four Bits Toggling at f_i = 5MHz 50% Duty Cycle S = Steady State	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.2	12.8[5]	

2559 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FCT399				IDT54/74FCT399A				IDT54/74FCT399C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	C_L = 50pF R_L = 500Ω	3.0	10.0	3.0	11.5	2.5	7.0	2.5	7.5	2.5	6.1	2.5	6.6	ns
t_{SU}	Set-up Time HIGH or LOW I_n to CP		4.0	—	4.5	—	3.5	—	4.0	—	3.5	—	4.0	—	ns
t_H	Hold Time HIGH or LOW I_n to CP		1.0	—	1.5	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
t_{SU}	Set-up Time HIGH or LOW S to CP		9.0	—	9.5	—	8.5	—	9.0	—	8.5	—	9.0	—	ns
t_H	Hold Time HIGH or LOW S to CP		0	—	0	—	0	—	0	—	0	—	0	—	ns
t_W	CP Pulse Width HIGH or LOW		5.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

NOTES:

2559 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

6

Integrated Device Technology, Inc.

FAST CMOS 8-BIT IDENTITY COMPARATOR

IDT54/74FCT521
IDT54/74FCT521A
IDT54/74FCT521B
IDT54/74FCT521C

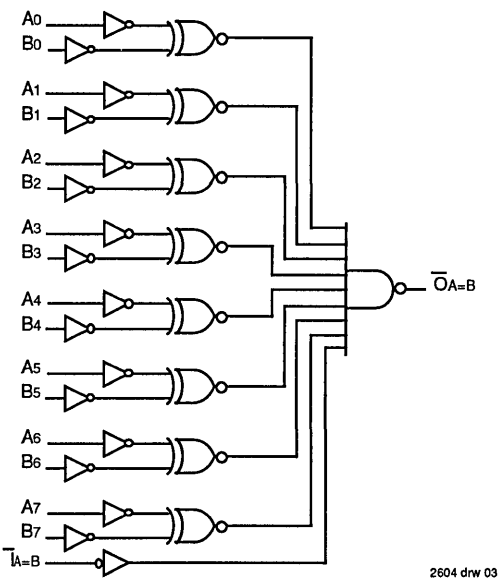
FEATURES:

- IDT54/74FCT521 equivalent to FAST™ speed
- **IDT54/74FCT521A 35% faster than FAST**
- **IDT54/74FCT521B 50% faster than FAST**
- **IDT54/74FCT521C 60% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- IOL = 48mA (commercial), and 32mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST (5µA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

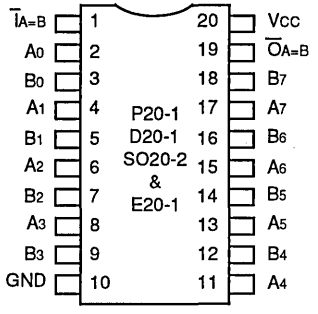
The IDT54/74FCT521/A/B/C are 8-bit identity comparators built using advanced CEMOS™, a dual metal CMOS technology. These devices compare two words of up to eight bits each and provide a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

FUNCTIONAL BLOCK DIAGRAM



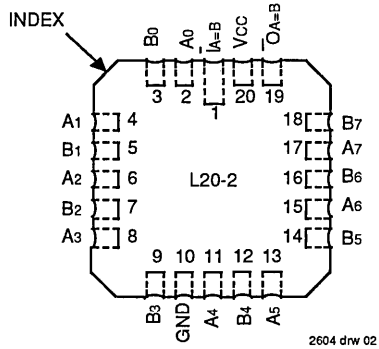
2604 drw 03

PIN CONFIGURATIONS



DIP/SOIC/CERPACK TOP VIEW

2604 drw 01



2604 drw 02

LCC TOP VIEW

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN DESCRIPTION

Pin Names	Description
A_0 - A_7	Word A Inputs
B_0 - B_7	Word B Inputs
$\overline{I}_{A=B}$	Expansion or Enable Input (Active LOW)
$\overline{O}_{A=B}$	Identity Output (Active LOW)

2604 tbl* 05

FUNCTION TABLE[1]

INPUTS		OUTPUT
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

NOTE: 2604 tbl* 06

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   *A_0 = B_0, A_1 = B_1, A_2 = B_2, etc.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2604 tbl* 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed VCC by +0.5V unless otherwise noted.
2. Input and VCC terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2604 tbl* 02

1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

2604 tbl* 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max. Outputs Open fi = 10MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	

NOTES: 2604 tbl* 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FCT521				IDT54/74FCT521A				IDT54/74FCT521B				IDT54/74FCT521C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay An or Bn to $\overline{O}_A$ = B	C_L = 50pF R_L = 500Ω	1.5	11.0	1.5	15.0	1.5	7.2	1.5	9.5	1.5	5.5	1.5	7.3	1.5	4.5	1.5	5.1	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_A$ = B to $\overline{O}_A$ = B		1.5	10.0	1.5	9.0	1.5	6.0	1.5	7.8	1.5	4.6	1.5	6.0	1.5	4.1	1.5	4.5	ns

NOTES: 2604 tbl* 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

Integrated Device Technology, Inc.

FAST CMOS OCTAL LATCHED TRANSCEIVER

IDT54/74FCT543
IDT54/74FCT543A
IDT54/74FCT543C

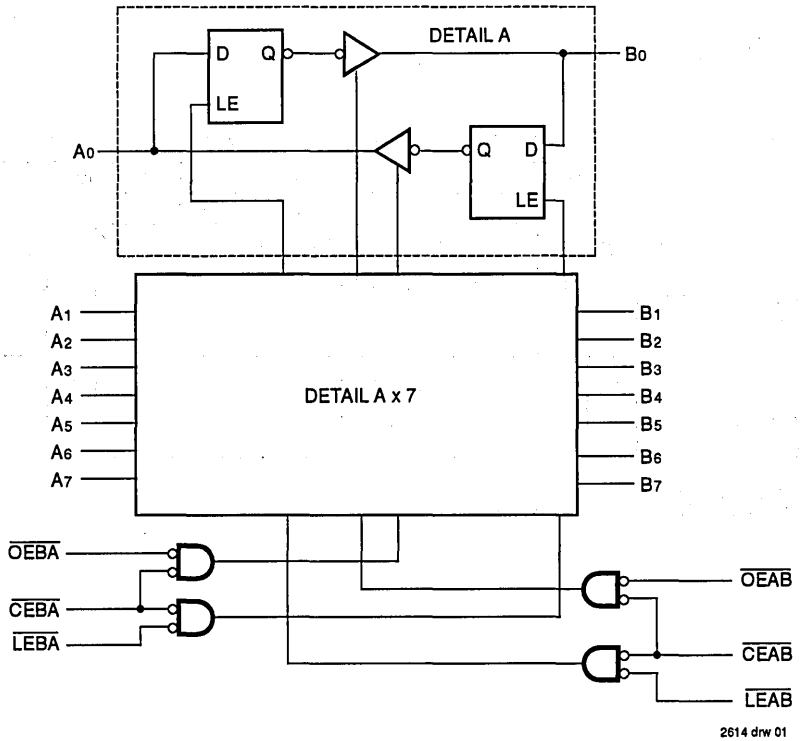
FEATURES:

- IDT54/74FCT543 equivalent to FAST™ speed
- **IDT54/74FCT543A 25% faster than FAST**
- **IDT54/74FCT543C 40% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial), 48mA (military)
- Separate controls for data flow in each direction
- Back-to-back latches for storage
- CMOS power levels (1mW typ. static)
- Substantially lower input current levels than FAST (5µA max.)
- TTL input and output level compatible
- CMOS output level compatible
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

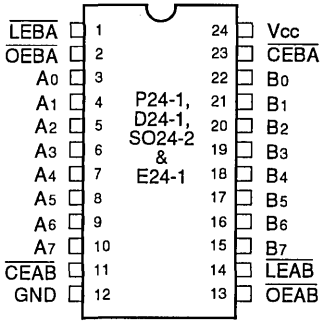
The IDT54/74FCT543/A/C is a non-inverting octal transceiver built using advanced CEMOS™, a dual metal CMOS technology. These devices contain two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A_0–A_7 or to take data from B_0–B_7, as indicated in the Function Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

FUNCTIONAL BLOCK DIAGRAM

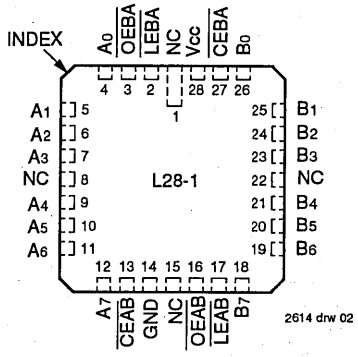


CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0–A_7	A-to-B Data Inputs or B-to-A 3-State Outputs
B_0–B_7	B-to-A Data Inputs or A-to-B 3-State Outputs

2614 tbl 02

FUNCTION TABLE (1,2)

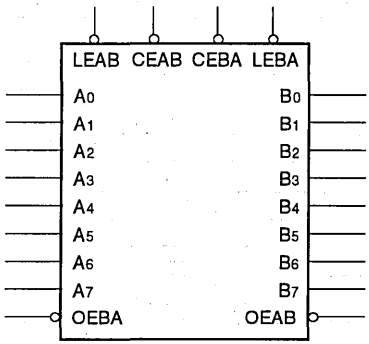
For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B	B_0–B_7
H	—	—	Storing	High Z
—	H	—	Storing	—
—	—	H	—	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

2614 tbl 01

NOTES:
1. * Before $\overline{LEAB}$ LOW-to-HIGH Transition
   H = HIGH Voltage Level
   L = LOW Voltage Level
   — = Don't Care or Irrelevant
2. A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.

LOGIC SYMBOL



2614 drw 03

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2614 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2614 tbl 04

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V, V_{HC} = Vcc – 0.2V
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = –55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	Vcc = Max.	V_I = Vcc	—	—	5	µA
			V_I = 2.7V	—	—	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	—	—	–5(4)	µA
			V_I = GND	—	—	–5	
I_{IH}	Input HIGH Current (I/O pins Only)	Vcc = Max.	V_I = Vcc	—	—	15	µA
			V_I = 2.7V	—	—	15(4)	
I_{IL}	Input LOW Current (I/O pins Only)		V_I = 0.5V	—	—	–15(4)	µA
			V_I = GND	—	—	–15	
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.(3), V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	Vcc	—	V
		Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}(4)	Vcc	—	
			I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}(4)	
			I_{OL} = 48mA MIL.(5)	—	0.3	0.55	
			I_{OL} = 64mA COM'L.(5)	—	0.3	0.55	

NOTES: 2614 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.

POWER SUPPLY CHARACTERISTICS $V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max., V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz ($\overline{LEAB}$) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz ($\overline{LEAB}$) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} Eight Bits Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	7.0	12.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	9.2	21.8[5]	

2614 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT543				IDT54/74FCT543A				IDT54/74FCT543C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Transparent Mode An to Bn or Bn to An	CL = 50pF RL = 500Ω	2.5	8.5	2.5	10.0	2.5	6.5	2.5	7.5	2.5	5.3	2.5	6.1	ns
tPLH tPHL	Propagation Delay $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn		2.5	12.5	2.5	14.0	2.5	8.0	2.5	9.0	2.5	7.0	2.5	8.0	ns
tPZH tPZL	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		2.0	12.0	2.0	14.0	2.0	9.0	2.0	10.0	2.0	8.0	2.0	9.0	ns
tPHZ tPLZ	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		2.0	9.0	2.0	13.0	2.0	7.5	2.0	8.5	2.0	6.5	2.0	7.5	ns
tSU	Set-up Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$		3.0	—	3.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tW	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW		5.0	—	5.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2513 tbl 07

Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSCEIVER/REGISTER

IDT54/74FCT646
IDT54/74FCT646A
IDT54/74FCT646C

FEATURES:

- IDT54/74FCT646 equivalent to FAST™ speed;
- **IDT54/74FCT646A 30% faster than FAST**
- **IDT54/74FCT646C 40% faster than FAST**
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- I_{OL} = 64mA (commercial) and 48mA (military)
- CMOS power levels (1mW typical static)
- TTL input and output level compatible
- CMOS output level compatible
- Available in 24-pin (300 mil) CERDIP, plastic DIP, SOIC, CERPACK and 28-pin LCC
- Product available in Radiation Tolerant and Radiation Enhanced Versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

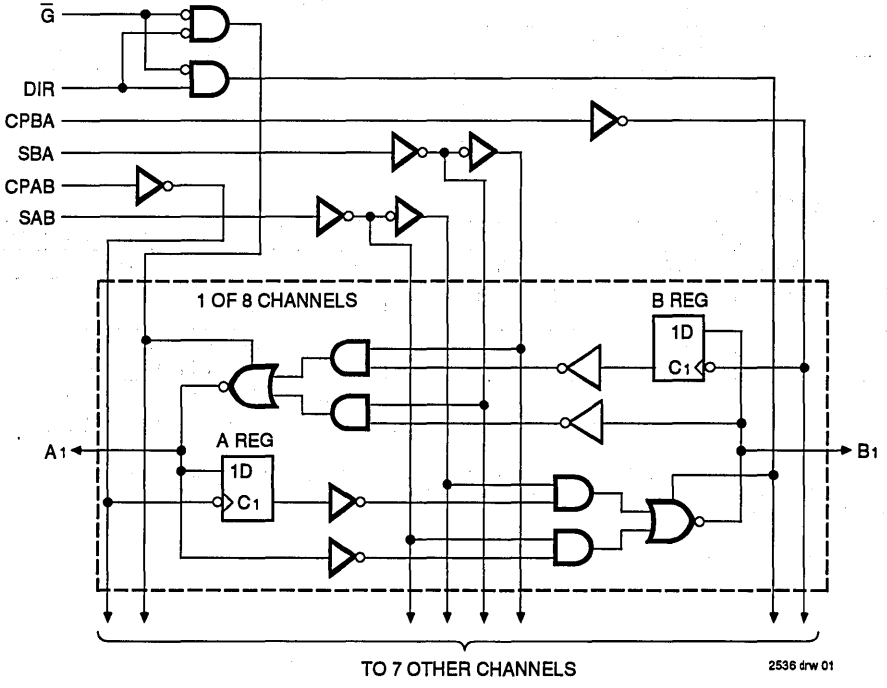
The IDT54/74FCT646/A/C consists of a bus transceiver with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

The IDT54/74FCT646/A/C utilizes the enable control ($\overline{G}$) and direction (DIR) pins to control the transceiver functions.

SAB and SBA control pins are provided to select either real time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data and a HIGH selects stored data.

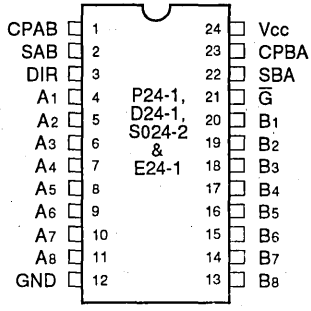
Data on the A or B data bus or both can be stored in the internal D flip flops by LOW-to-HIGH transitions at the appropriate clock pins (CPAB or CPBA) regardless of the select or enable control pins.

FUNCTIONAL BLOCK DIAGRAM

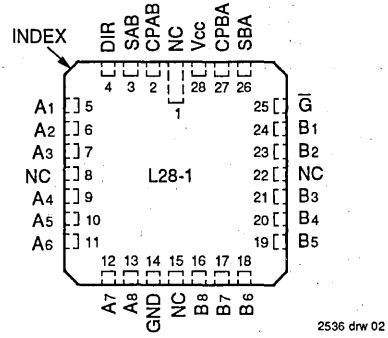


CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



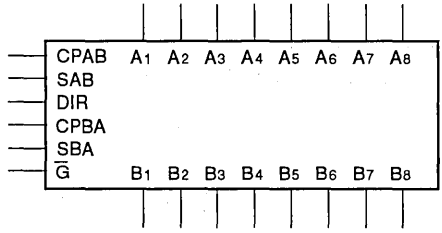
LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
A_1–A_8	Data Register A Inputs Data Register B Outputs
B_1–B_8	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\overline{G}$	Output Enable Inputs

2536 tbl 01

LOGIC SYMBOL

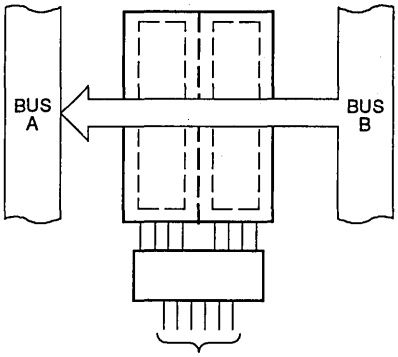


FUNCTION TABLE[2]

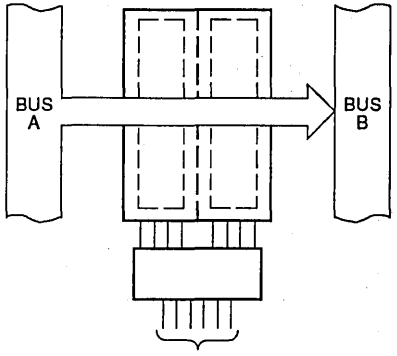
Inputs						Data I/O[1]		Operation or Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_1–A_8	B_1–B_8	IDT54/74FCT646
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

2536 tbl 02

NOTES:
1. The data output functions may be enabled or disabled by various signals at the $\overline{G}$ or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. H = HIGH, L = LOW, X = Don't Care, ↑ = LOW-to-HIGH Transition.

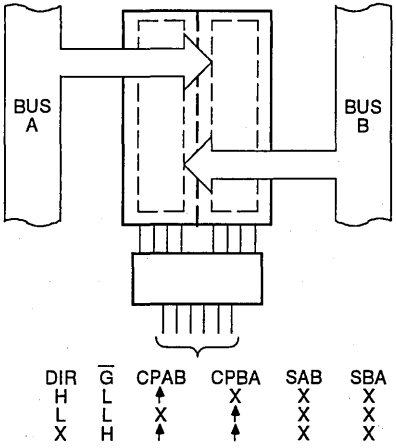


REAL–TIME TRANSFER BUS B TO BUS A

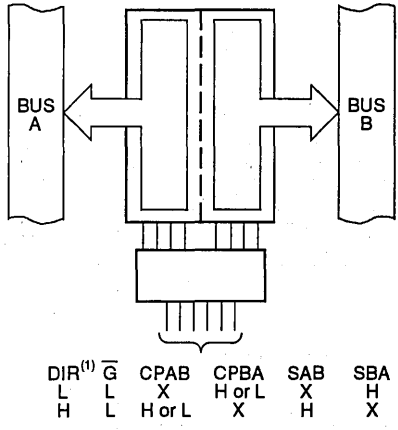


REAL–TIME TRANSFER BUS A TO BUS B

2536 drw 03



STORAGE FROM A AND/OR B



TRANSFER STORED DATA TO A AND/OR B

2536 drw 04

NOTE:
1. Cannot transfer data to A bus and B bus simultaneously.

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2536 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Inputs and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2536 tbl 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	—	—	–5(4)	
			V_I = GND	—	—	–5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	—	—	15	µA
			V_I = 2.7V	—	—	15(4)	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	—	—	–15(4)	
			V_I = GND	—	—	–15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
			I_{OH} = –12mA MIL.	2.4	4.0	—	
			I_{OH} = –15mA COM'L.	2.4	4.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}(4)	
			I_{OL} = 48mA MIL.	—	0.3	0.55	
			I_{OL} = 64mA COM'L.	—	0.3	0.55	

NOTES: 2536 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{G}$ = DIR = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{G}$ = DIR = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{G}$ = DIR = GND Eight Bits Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	7.0	12.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	9.2	21.8[5]	

2536 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	54/74FCT646				54/74FCT646A				54/74FCT646C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	C_L = 50 pF R_L = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	1.5	5.4	1.5	6.0	ns
tPZH tPZL	Output Enable Time $\overline{G}$, DIR to Bus		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	1.5	7.8	1.5	8.9	ns
tPHZ tPLZ	Output Disable Time $\overline{G}$, DIR to Bus		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	1.5	6.3	1.5	7.7	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	1.5	5.7	1.5	6.3	ns
tPLH tPHL	Propagation Delay SBA or SAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	1.5	6.2	1.5	7.0	ns
tSU	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tW	Clock Pulse Width HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2536 tbl 07

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE REGISTERS

IDT54/74FCT821A/B/C
IDT54/74FCT823A/B/C
IDT54/74FCT824A/B/C
IDT54/74FCT825A/B/C

FEATURES:

- Equivalent to AMD's Am29821-25 bipolar registers in pinout/function, speed and output drive over full temperature and voltage supply extremes
- IDT54/74FCT821A/823A/824A/825A equivalent to FAST™ speed
- **IDT54/74FCT821B/823B/824B/825B 25% faster than FAST**
- **IDT54/74FCT821C/823C/824C/825C 40% faster than FAST**
- Buffered common Clock Enable ($\overline{EN}$) and asynchronous Clear input ($\overline{CLR}$)
- I_{OL} = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output compatibility
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5μA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

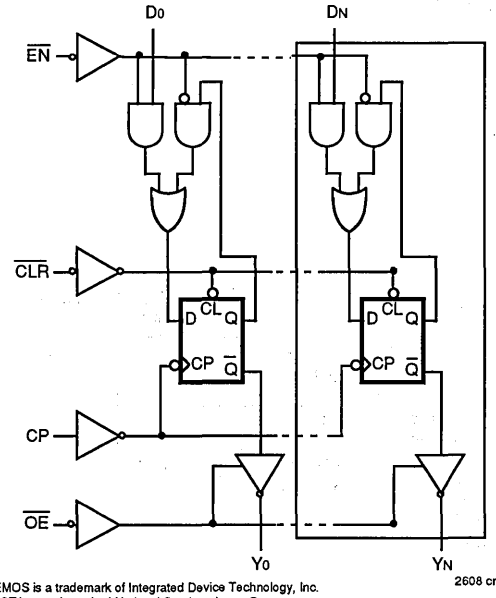
The IDT54/74FCT800 series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT820 series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT821 are buffered, 10-bit wide versions of the popular '374 function. The IDT54/74FCT823 and IDT54/74FCT824 are 9-bit wide buffered registers with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high-performance microprogrammed systems. The IDT54/74FCT825 are 8-bit buffered registers with all the '823 controls plus multiple enables ($\overline{OE_1}$, $\overline{OE_2}$, $\overline{OE_3}$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. They are ideal for use as an output port requiring HIGH I_{OL}/I_{OH}.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

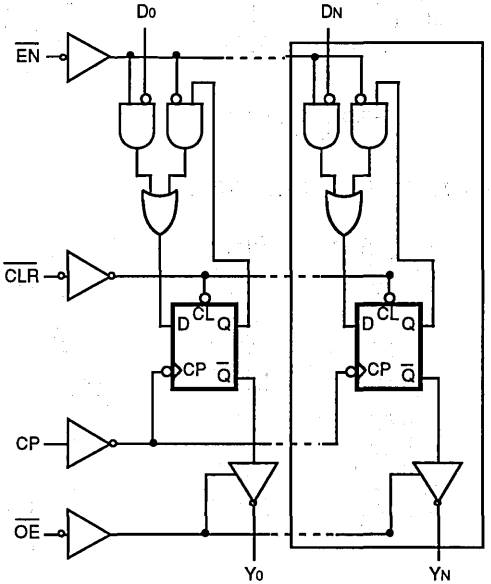
FUNCTIONAL BLOCK DIAGRAMS

IDT54/74FCT821/823/825



2608 cnv° 01

IDT54/74FCT824

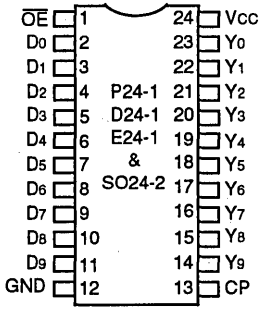


2608 cnv° 02

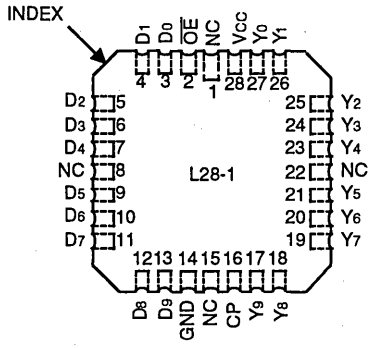
CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS

IDT54/74FCT821 10-BIT REGISTER

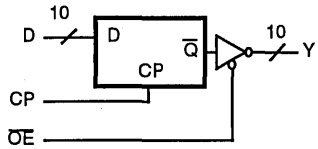


DIP/SOIC/CERPACK
TOP VIEW



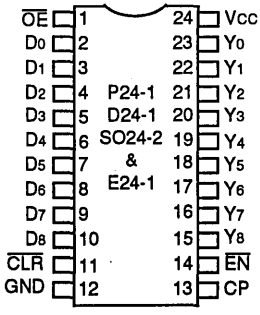
LCC
TOP VIEW

LOGIC SYMBOLS

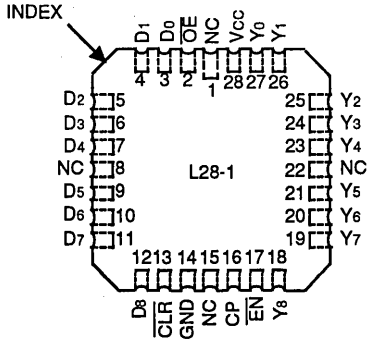


2608 cnv* 03

IDT54/74FCT823/824 9-BIT REGISTERS



DIP/SOIC/CERPACK
TOP VIEW



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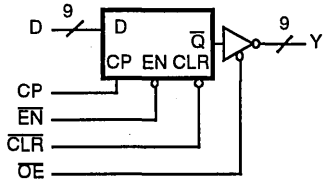
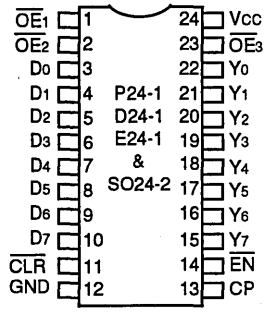
TOP VIEW

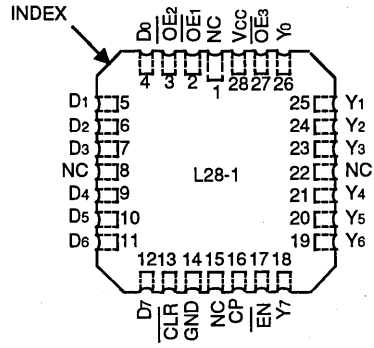


2608 cnv* 04

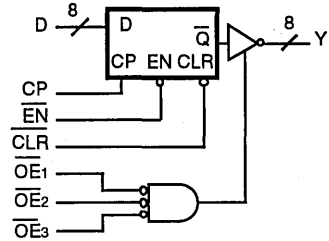
IDT54/74FCT825 8-BIT REGISTER



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW



2608 cnv* 05

PRODUCT SELECTOR GUIDE

	Device		
	10-Bit	9-Bit	8-Bit
Non-inverting	54/74FCT821A/B/C	54/74FCT823A/B/C	54/74FCT825A/B/C
Inverting		54/74FCT824A/B/C	

2608 tbl 01

PIN DESCRIPTION

Name	I/O	Description
D_I	I	The D flip-flop data inputs.
$\overline{CLR}$	I	For both inverting and non-inverting registers, when the clear input is LOW and $\overline{OE}$ is LOW, the Q_I outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Y_I, $\overline{Y_I}$	O	The register three-state outputs.
$\overline{EN}$	I	Clock Enable. When the clock enable is LOW, data on the D_I input is transferred to the Q_I output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_I outputs do not change state, regardless of the data or clock input transitions.
$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y_I outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_I outputs.

2608 tbl 01

FUNCTION TABLE[1] IDT54/74FCT821/823/825

Inputs					Internal/ Outputs		
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_I	CP	Q_I	Y_I	Function
H	H	L	L	↑	L	Z	High Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

NOTE: 2608 tbl 02
1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = High Impedance

FUNCTION TABLE[1] IDT54/74FCT824

Inputs					Internal/ Outputs		
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_I	CP	Q_I	Y_I	Function
H	H	L	L	↑	H	Z	High Z
H	H	L	H	↑	L	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	H	
L	H	L	H	↑	L	L	

NOTE: 2608 tbl 03
1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = High Impedance

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2608 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2608 tbl 05
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = Vcc – 0.2V
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = –55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	Vcc = Max.	V_I = Vcc	—	—	5	µA
			V_I = 2.7V	—	—	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5(4)	
			V_I = GND	—	—	–5	
I_{OZH}	Off State (High Impedance) Output Current	Vcc = Max.	V_O = Vcc	—	—	10	µA
			V_O = 2.7V	—	—	10(4)	
I_{OZL}			V_O = 0.5V	—	—	–10(4)	
			V_O = GND	—	—	–10	
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.(3), V_O = GND		–75	–120	—	mA
V_{OH}	Output HIGH Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	Vcc	—	V
		Vcc = Min.	I_{OH} = –300µA	V_{HC}	Vcc	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15mA MIL.	2.4	4.3	—	
			I_{OH} = –24mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	Vcc = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		Vcc = Min.	I_{OL} = 300µA	—	GND	V_{LC}(4)	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES: 2608 tbl 06
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = $\overline{EN}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = $\overline{EN}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = $\overline{EN}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

2608 tbl 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameter	Description	Test Conditions[1]	IDT54/74FCT821A/ 823A/824A/825A				IDT54/74FCT821B/ 823B/824B/825B				IDT54/74FCT821C/ 823C/824C/825C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to Y i (OE = LOW)	CL = 50pF RL = 500Ω	—	10.0	—	11.5	—	7.5	—	8.5	—	6.0	—	7.0	ns
		CL = 300pF[3] RL = 500Ω	—	20.0	—	20.0	—	15.0	—	16.0	—	12.5	—	13.5	
tSU	Set-up Time HIGH or LOW D i to CP	CL = 50pF RL = 500Ω	4.0	—	4.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW D i to CP		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tSU	Set-up Time HIGH or LOW EN to CP		4.0	—	4.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW EN to CP		2.0	—	2.0	—	0	—	0	—	0	—	0	—	ns
tPHL	Propagation Delay, CLR to Yi		—	14.0	—	15.0	—	9.0	—	9.5	—	8.0	—	8.5	ns
tREM	Recovery Time CLR to CP		6.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tW	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tW	CLR Pulse Width LOW		6.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tPZH tPZL	Output Enable Time OE to Yi	CL = 50pF RL = 500Ω	—	12.0	—	13.0	—	8.0	—	9.0	—	7.0	—	8.0	ns
		CL = 300pF[3] RL = 500Ω	—	23.0	—	25.0	—	15.0	—	16.0	—	12.5	—	13.5	
tPHZ tPLZ	Output Disable Time OE to Yi	CL = 5pF[3] RL = 500Ω	—	7.0	—	8.0	—	6.5	—	7.0	—	6.2	—	6.2	ns
		CL = 50pF RL = 500Ω	—	8.0	—	9.0	—	7.5	—	8.0	—	6.5	—	6.5	

NOTES:

2608 tbl* 08

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUFFERS

IDT54/74FCT827A
IDT54/74FCT827B
IDT54/74FCT827C

FEATURES:

- Faster than AMD's Am29827 series
- Equivalent to AMD's Am29827 bipolar buffers in pinout/ function, speed and output drive over full temperature and voltage supply extremes
- IDT54/74FCT827A equivalent to FAST™
- **IDT54/74FCT827B 35% faster than FAST**
- **IDT54/74FCT827C 45% faster than FAST**
- I_{OL} = 48mA (commercial), and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5μA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

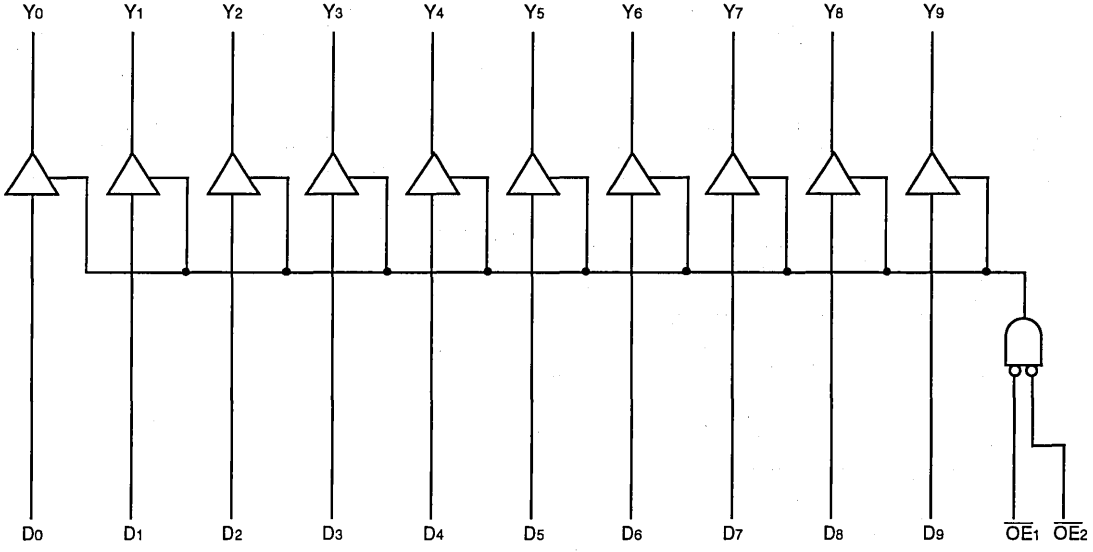
DESCRIPTION:

The IDT54/74FCT800 series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT827A/B/C 10-bit bus drivers provide high-performance bus interface buffering for wide data/ address paths or buses carrying parity. The 10-bit buffers have NAND-ed output enables for maximum control flexibility.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

FUNCTIONAL BLOCK DIAGRAM



2609 drw 01

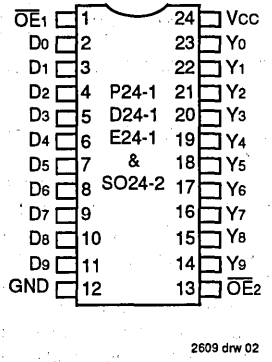
PRODUCT SELECTOR GUIDE

	10-Bit Buffer
Non-inverting	IDT54/74FCT827A/B/C

2609 tbl 01

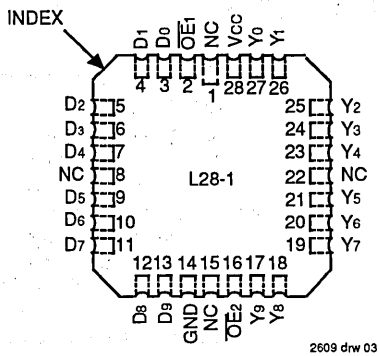
CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS



2609 drw 02

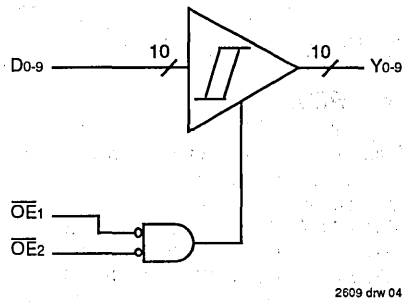
DIP/CERPACK/SOIC TOP VIEW



2609 drw 03

LCC TOP VIEW

LOGIC SYMBOL



2609 drw 04

PIN DESCRIPTION

Name	I/O	Description
$\overline{OE}_I$	I	When both are LOW, the outputs are enabled. When either one or both are HIGH, the outputs are High Z.
D_I	I	10-bit data input.
Y_I	O	10-bit data output.

2609 tbl 02

FUNCTION TABLE[1]

Inputs			Output	
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	Function
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	Three-State
X	H	X	Z	

NOTE: 2609 tbl 03

1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2609 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and VCC terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2609 tbl 05

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5[4]	
			V_I = GND	—	—	–5	
I_{OZH}	Off State (High Impedance)	V_{CC} = Max.	V_O = V_{CC}	—	—	10	µA
	Output Current		V_O = 2.7V	—	—	10[4]	
I_{OZL}			V_O = 0.5V	—	—	–10[4]	
			V_O = GND	—	—	–10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–75	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15mA MIL.	2.4	4.3	—	
			I_{OH} = –24mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}[4]	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

2609 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE_1}$ = $\overline{OE_2}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
		50% Duty Cycle $\overline{OE_1}$ = $\overline{OE_2}$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5[5]	
		50% Duty Cycle $\overline{OE_1}$ = $\overline{OE_2}$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2609 tbl 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameter	Description	Conditions[1]	IDT54/74FCT827A				IDT54/74FCT827B				IDT54/74FCT827C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Di to Yi	CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	5.0	1.5	6.5	1.5	4.4	1.5	5.0	ns
		CL = 300pF[3] RL = 500Ω	1.5	15.0	1.5	17.0	1.5	13.0	1.5	14.0	1.5	10.0	1.5	11.0	
tPZH tPZL	Output Enable Time $\overline{OE}$i to Yi	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	1.5	7.0	1.5	8.0	ns
		CL = 300pF[3] RL = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	1.5	14.0	1.5	15.0	
tPHZ tPLZ	Output Disable Time $\overline{OE}$i to Yi	CL = 5pF[3] RL = 500Ω	1.5	9.0	1.5	9.0	1.5	6.0	1.5	7.0	1.5	5.7	1.5	6.7	ns
		CL = 50pF RL = 500Ω	1.5	10.0	1.5	10.0	1.5	7.0	1.5	8.0	1.5	6.0	1.5	7.0	

2609 tbl 08

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

6

Integrated Device Technology, Inc.

FAST CMOS PARITY BUS TRANSCEIVER

IDT54/74FCT833A
IDT54/74FCT833B

FEATURES:

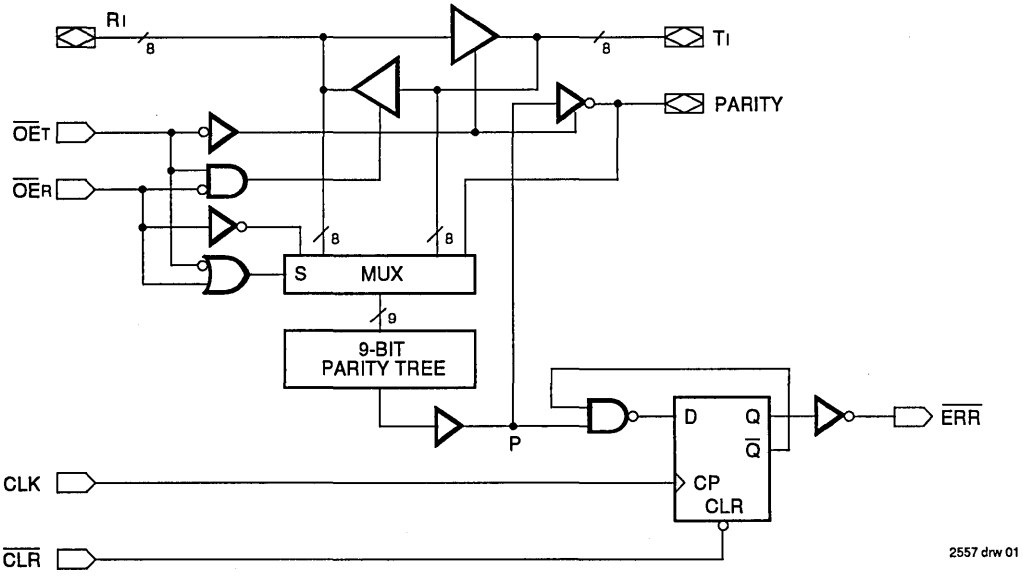
- Equivalent to AMD's Am29833 bipolar parity bus transceiver in pinout/function, speed and output drive over full temperature and voltage supply extremes
- High-speed bidirectional bus transceiver for processor-organized devices
- IDT54/74FCT833A equivalent to Am29833A speed and output drive
- **IDT54/74FCT833B 30% faster than Am29833A**
- Buffered direction and three-state controls
- Error flag with open-drain output
- I_{OL} = 48mA (commercial) and 32mA (military)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5µA max.)
- Available in plastic DIP, CERDIP, LCC and SOIC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT833s are high-performance bus transceivers designed for two-way communications. They each contain an 8-bit data path from the R (port) to the T (port), an 8-bit data path from the T (port) to the R (port), and a 9-bit parity checker/generator. The error flag can be clocked and stored in a register and read at the $\overline{ERR}$ output. The clear ($\overline{CLR}$) input is used to clear the error flag register.

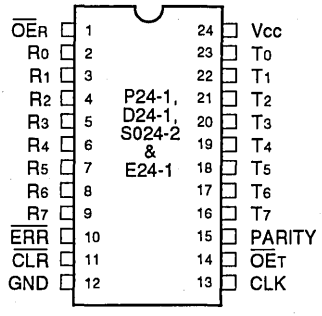
The output enables $\overline{OE_T}$ and $\overline{OE_R}$ are used to force the port outputs to the high-impedance state so that the device can drive bus lines directly. In addition, $\overline{OE_R}$ and $\overline{OE_T}$ can be used to force a parity error by enabling both lines simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability. The devices are specified at 48mA and 32mA output sink current over the commercial and military temperature ranges, respectively.

FUNCTIONAL BLOCK DIAGRAM

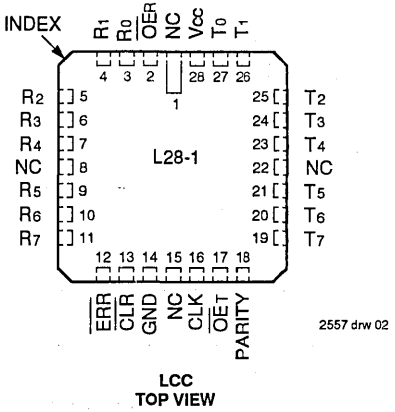


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

Pin Name	I/O	Description
$\overline{OE_R}$	I	RECEIVE enable input.
RI	I/O	8-bit RECEIVE data input/output.
$\overline{ERR}$	O	Output from fault registers. Register detection of odd parity fault on rising clock edge (CLK). A registered $\overline{ERR}$ output remains LOW until cleared. Open drain output, requires pull up resistor.
$\overline{CLR}$	I	Clears the fault register output.
TI	I/O	8-bit TRANSMIT data input/output.
PARITY	I/O	1-bit PARITY output.
$\overline{OE_T}$	I	TRANSMIT enable input.
CLK	I	External clock pulse input for fault register flag.

2557 tbl 01

ERROR FLAG OUTPUT FUNCTION TABLE(1,2)

Inputs		Internal To Device	Output Pre-State	Output	
$\overline{CLR}$	CLK	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
H	↑	H	H	H	Sample
H	↑	—	L	L	(1's
H	↑	L	—	L	Capture)
L	—	—	—	H	Clear

2557 tbl 02

NOTES:
1. $\overline{OE_T}$ is HIGH and $\overline{OE_R}$ is LOW.
2. H = HIGH
   L = LOW
   ↑ = LOW-to-HIGH transition of clock
   — = Don't Care or Irrelevant

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FUNCTION TABLE[2]

Inputs						Outputs				
$\overline{OE_T}$	$\overline{OE_R}$	$\overline{CLR}$	CLK	R_I (Σ or H's)	T_I Incl Parity (Σ of H's)	R_I	T_I	Parity	$\overline{ERR}$[1]	Function
L	H	H	↑	H (Odd)	NA	NA	H	L	H	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	H	↑	H (Even)	NA	NA	H	H	L	
L	H	H	↑	L (Odd)	NA	NA	L	L	H	
L	H	H	↑	L (Even)	NA	NA	L	H	L	
H	L	H	↑	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag: transmitting path is disabled.
H	L	H	↑	NA	H (Even)	H	NA	NA	L	
H	L	H	↑	NA	L (Odd)	L	NA	NA	H	
H	L	H	↑	NA	L (Even)	L	NA	NA	L	
—	—	L	—	—	—	NA	NA	NA	H	Clear the state of error flag register.
H	H	H	H or L	—	—	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	—	—	—	Z	Z	Z	H	
H	H	H	↑	H or L (Odd)	—	Z	Z	Z	H	
H	H	H	↑	H or L (Even)	—	Z	Z	Z	L	
L	L	H	↑	H (Odd)	NA	NA	H	H	L	Forced-error checking.
L	L	H	↑	H (Even)	NA	NA	H	L	H	
L	L	H	↑	L (Odd)	NA	NA	L	H	L	
L	L	H	↑	L (Even)	NA	NA	L	L	H	

NOTES:

2557 tbl 03

1. Output state assumes HIGH output pre-state.
2. H = HIGH
   L = LOW
   ↑ = LOW-to-HIGH transition of clock
   *No change to stored Error State
   Z = High Impedance
   NA = Not Applicable
   – = Don't Care or Irrelevant
   Odd = Odd number of logic one's
   Even = Even number of logic one's
   I = 0, 1, 2, 3, 4, 5, 6, 7

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	−0.5 to V_{CC}	−0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2557 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Inputs and V_{CC} terminals.
3. Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2557 tbl 05

1. This parameter is guaranteed by characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} − 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5(4)	
I_{IL}	Input LOW Current (Except I/O Pins)		V_I = 0.5V	—	—	−5(4)	
			V_I = GND	—	—	−5	
I_{IH}	Input HIGH Current (I/O Pins Only)	V_{CC} = Max.	V_I = V_{CC}	—	—	15	µA
			V_I = 2.7V	—	—	15(4)	
I_{IL}	Input LOW Current (I/O Pins Only)		V_I = 0.5V	—	—	−15(4)	
			V_I = GND	—	—	−15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA		—	−0.7	−1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		−60	−120	—	mA
V_{OH}	Output HIGH Voltage (Except $\overline{ERR}$)	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = −32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300µA	V_{HC}	V_{CC}	—	
			I_{OH} = −15mA MIL.	2.4	4.3	—	
			I_{OH} = −24mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	v
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	Except $\overline{ERR}$ I_{OL} = 300µA	—	GND	V_{LC}(4)	
			Except $\overline{ERR}$ I_{OL} = 32 mA MIL.	—	0.3	0.5	
			Except $\overline{ERR}$ I_{OL} = 48mA COM'L.	—	0.3	0.5	
			$\overline{ERR}$ I_{OL} = 48mA	—	0.3	0.5	

NOTES: 2557 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS $V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.; $V_{IN} \geq V_{HC}$, $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4] Outputs Open	V_{CC} = Max. $V_{IN} \leq V_{LC}$ $\overline{OE_T}$ = $\overline{OE_R}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE_T}$ = GND $\overline{OE_R}$ = V_{CC} f_i = 2.5MHz One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.4	3.4	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.9	5.4	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE_T}$ = GND f_i = 2.5MHz $\overline{OE_R}$ = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

2557 tbl 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions[1]	IDT54/74FCT833A				IDT54/74FCT833B				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH	Propagation Delay	CL = 50pF	—	10.0	—	14.0	—	7.0	—	10.0	ns
tPHL	RI to TI, TI to RI	CL = 300pF[3]	—	17.5	—	21.5	—	14.5	—	17.5	
tPLH	Propagation Delay	CL = 50pF	—	15.0	—	20.0	—	10.5	—	14.0	ns
tPHL	RI to PARITY	CL = 300pF[3]	—	22.5	—	27.5	—	18.0	—	21.5	
tPZH	Output Enable Time	CL = 50pF	—	12.0	—	16.0	—	8.5	—	11.0	ns
tPZL	$\overline{OE}_R$, $\overline{OE}_T$ to RI, TI	CL = 300pF[3]	—	19.5	—	23.5	—	16.0	—	18.5	
tPHZ	Output Disable Time	CL = 5pF[3]	—	10.7	—	14.7	—	7.2	—	9.8	ns
tPLZ	$\overline{OE}_R$, $\overline{OE}_T$ to RI, TI	CL = 50pF	—	12.0	—	16.0	—	8.5	—	11.0	
tSU	TI, PARITY to CLK Set-up Time	CL = 50pF	12.0	—	16.0	—	8.5	—	11.0	—	ns
tH	TI, PARITY to CLK Hold Time		0	—	0	—	0	—	0	—	ns
tREM	Clear Recovery Time $\overline{CLR}$ to CLK		15.0	—	20.0	—	10.5	—	14.0	—	ns
tW	Clock Pulse Width HIGH or LOW		7.0	—	9.5	—	5.5	—	7.0	—	ns
tW	Clear Pulse Width LOW		7.0	—	9.5	—	5.5	—	7.0	—	ns
tPHL	Propagation Delay CLK to $\overline{ERR}$		—	12.0	—	16.0	—	8.5	—	11.0	ns
tPLH	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$		—	16.0	—	20.0	—	15.0	—	18.0	ns
tPLH	Propagation Delay	CL = 50pF	—	15.0	—	20.0	—	10.5	—	14.0	ns
tPHL	$\overline{OE}_R$ to PARITY	CL = 300pF[3]	—	22.5	—	27.5	—	18.0	—	21.5	

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

2557 tbl 08

6

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE LATCHES

IDT54/74FCT841A/B/C
IDT54/74FCT843A/B/C
IDT54/74FCT844A/B/C
IDT54/74FCT845A/B/C

FEATURES:

- Equivalent to AMD's Am29841-46 bipolar registers in pinout/function, speed and output drive over full temperature and voltage supply extremes
- IDT54/74FCT841A/843A/844A/845A equivalent to FAST™ speed
- **IDT54/74FCT841B/843B/844B/845B 25% faster than FAST**
- **IDT54/74FCT841C/843C/844C/845C 40% faster than FAST**
- Buffered common latch enable, clear and preset inputs
- I_{OL} = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5μA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

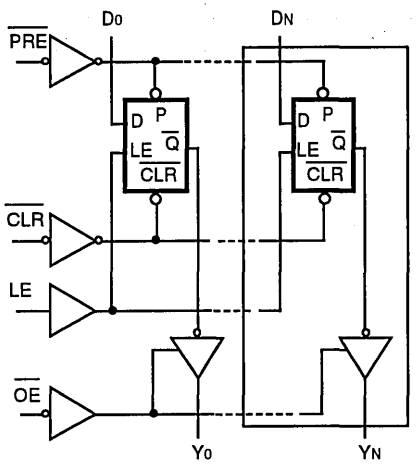
The IDT54/74FCT800 series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT840 series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT841 is a buffered, 10-bit wide version of the popular '373 function. The IDT54/74FCT843 and IDT54/74FCT844 are 9-bit wide buffered latches with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$)—ideal for parity bus interfacing in high-performance systems. The IDT54/74FCT845 is an 8-bit buffered latch with all the '843/4 controls, plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. It is ideal for use as an output port requiring high IOL/IOH.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high-impedance state.

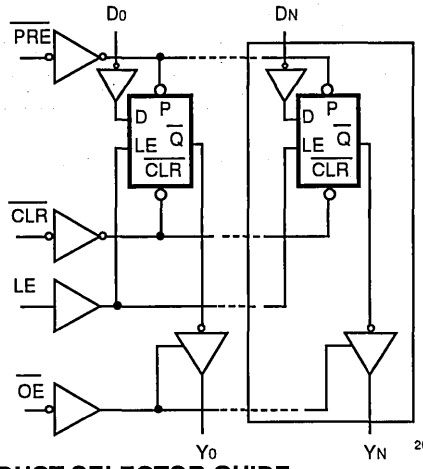
FUNCTIONAL BLOCK DIAGRAM

IDT54/74FCT841/843/845



2607 cnv* 01

IDT54/74FCT844



2607 cnv* 02

PRODUCT SELECTOR GUIDE

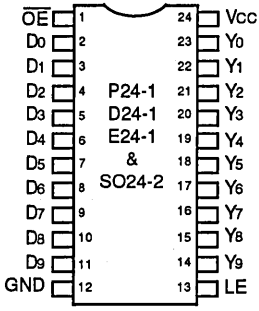
	Device		
	10-Bit	**9-Bit**	**8-Bit**
Non-Inverting	IDT54/74FCT841 A/B/C	IDT54/74FCT843 A/B/C	IDT54/74FCT845 A/B/C
Inverting		IDT54/74FCT844 A/B/C	

2607 tbl 01

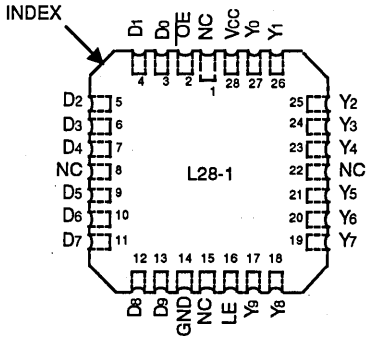
CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS

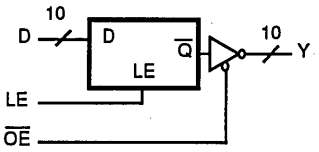
IDT54/74FCT841 10-BIT LATCH



DIP/CERPACK/SOIC
TOP VIEW

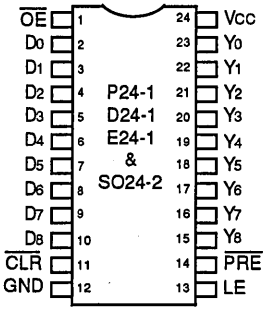


LCC
TOP VIEW

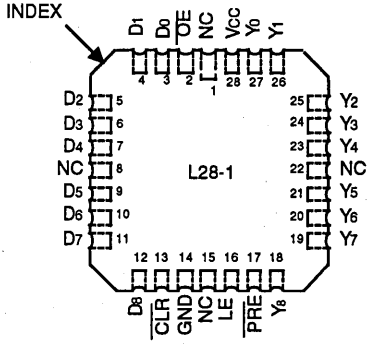


2607 cnv* 03,04,05

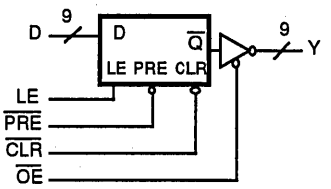
IDT54/74FCT843/844 9-BIT LATCHES



DIP/CERPACK/SOIC
TOP VIEW

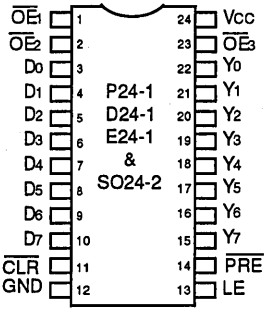


LCC
TOP VIEW

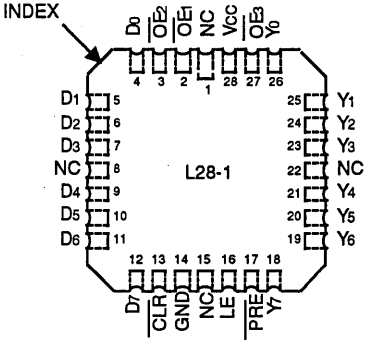


2607 cnv* 06,07,08

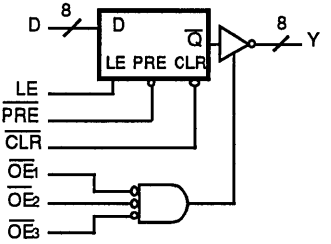
IDT54/74FCT845 8-BIT LATCH



DIP/CERPACK/SOIC
TOP VIEW



LCC
TOP VIEW



2607 cnv* 09,10,11

PIN DESCRIPTION

Name	I/O	Description
IDT54/74FCT841/843/845 (Non-Inverting)		
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_I	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_I	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs (Y_I) are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$
IDT54/74FCT844 (Inverting)		
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_I	I	The latch inverting data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_I	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs (Y_I) are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$

2607 tbl 02

FUNCTION TABLE[1]
IDT54/74FCT841/843/845

Inputs					Internal	Outputs	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_I	Q_I	Y_I	Function
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

NOTE: 2607 tbl 03
1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, Z = High Impedance

FUNCTION TABLE[1]
IDT54/74FCT844

Inputs					Inter - nal	Out - puts	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_I	Q_I	Y_I	Function
H	H	H	X	X	X	Z	High Z
H	H	H	H	H	L	Z	High Z
H	H	H	H	L	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	H	L	L	Transparent
H	H	L	H	L	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

NOTE: 2607 tbl 04
1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, Z = High Impedance

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2607 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter (1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2607 tbl 06

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5(4)	
			V_I = GND	—	—	–5	
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	10	µA
			V_O = 2.7V	—	—	10(4)	
I_{OZL}			V_O = 0.5V	—	—	–10(4)	
			V_O = GND	—	—	–10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–75	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
			I_{OH} = –15mA MIL.	2.4	4.3	—	
			I_{OH} = –24mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}(4)	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES: 2607 tbl 07

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

6

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2607 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter		Conditions[1]	FCT841A/843A-844A/845A				FCT841B/843B-844B/845B				FCT841C/843C-844C/845C				Unit
				Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
				Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
(FCT841, 843, 845) tPLH tPHL	Propagation Delay DI to YI (LE = HIGH)		CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns
			CL = 300pF[4] RL = 500Ω	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	
(FCT844) tPLH tPHL	Propagation Delay DI to YI (LE = HIGH)		CL = 50pF RL = 500Ω	1.5	10.0	1.5	12.0	1.5	8.0	1.5	9.0	1.5	7.0	1.5	8.0	ns
			CL = 300pF[4] RL = 500Ω	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	
tPLH tPHL	Propagation Delay LE to YI		CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	10.5	1.5	6.4	1.5	6.8	ns
			CL = 300pF[4] RL = 500Ω	1.5	16.0	1.5	20.0	1.5	15.5	1.5	18.0	1.5	15.0	1.5	16.0	
tPLH	Propagation Delay, $\overline{PRE}$ to YI		CL = 50pF	1.5	12.0	1.5	14.0	1.5	8.0	1.5	10.0	1.5	7.0	1.5	9.0	ns
tPHL			RL = 500Ω	1.5	14.0	1.5	17.0	1.5	10.0	1.5	13.0	1.5	9.0	1.5	12.0	
tPHL	Propagation Delay, $\overline{CLR}$ to YI			1.5	13.0	1.5	14.0	1.5	10.0	1.5	11.0	1.5	9.0	1.5	10.0	ns
tPLH				1.5	14.0	1.5	17.0	1.5	10.0	1.5	10.0	1.5	9.0	1.5	9.0	
tPZH tPZL	Output Enable Time $\overline{OE}$ to YI		CL = 50pF RL = 500Ω	1.5	11.5	1.5	13.0	1.5	8.0	1.5	8.5	1.5	6.5	1.5	7.3	ns
			CL = 300pF[4] RL = 500Ω	1.5	23.0	1.5	25.0	1.5	14.0	1.5	15.0	1.5	12.0	1.5	13.0	
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to YI		CL = 5pF[4] RL = 500Ω	1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	1.5	5.7	1.5	6.0	ns
			CL = 50pF RL = 500Ω	1.5	8.0	1.5	10.0	1.5	7.0	1.5	7.5	1.5	6.0	1.5	6.3	
tSU	Data to LE Set-up Time		CL = 50pF	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
tH	Data to LE Hold Time		RL = 500Ω	2.5	—	3.0	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
tW	LE Pulse Width[3]	HIGH		4.0	—	5.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tW	$\overline{PRE}$ Pulse Width[3]	LOW		5.0	—	7.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tW	$\overline{CLR}$ Pulse Width[3]	LOW		4.0	—	5.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tREM	Recovery Time $\overline{PRE}$ to LE			4.0	—	4.0	—	4.0	—	4.0	—	4.0	—	4.0	—	ns
tREM	Recovery Time $\overline{CLR}$ to LE			3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.
4. These conditions are guaranteed but not tested.

2607 tbl 09

6

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS TRANSCEIVERS

IDT54/74FCT861A/B
IDT54/74FCT863A/B
IDT54/74FCT864A/B

FEATURES:

- Equivalent to AMD's Am29861-64 bipolar registers in pinout/function, speed and output drive over full temperature and voltage supply extremes
- IDT54/74FCT861A/863A/864A equivalent to FAST™ speed
- **IDT54/74FCT861B/863B/864B 25% faster than FAST**
- High-speed symmetrical bidirectional transceivers
- I_{OL} = 48mA (commercial) and 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 Series (5µA max.)
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

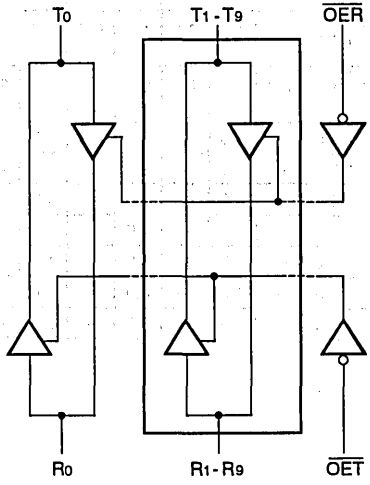
The IDT54/74FCT800 series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT860 series bus transceivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The IDT54/74FCT863/864 9-bit transceivers have NAND-ed output enables for maximum control flexibility.

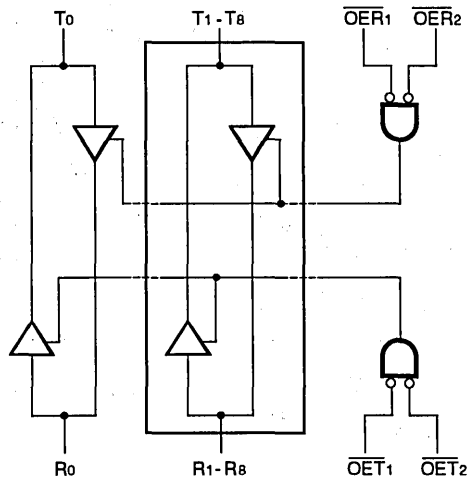
All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high-impedance state.

FUNCTIONAL BLOCK DIAGRAMS

IDT54/74FCT861



IDT54/74FCT863/864



2610 drw 01

PRODUCT SELECTOR GUIDE

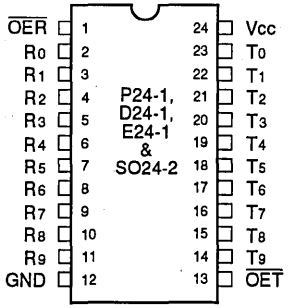
	Device	
	10-Bit	**9-Bit**
Non-inverting	IDT54/74FCT861	IDT54/74FCT863
Inverting		IDT54/74FCT864

2610 tbl 01

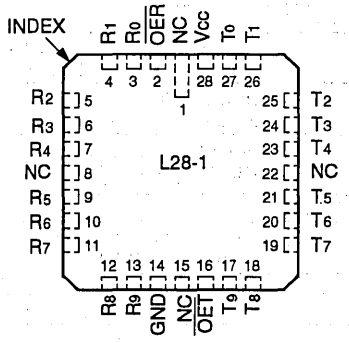
CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor Co.

PIN CONFIGURATIONS

IDT54/74FCT861 10-BIT TRANSCEIVER

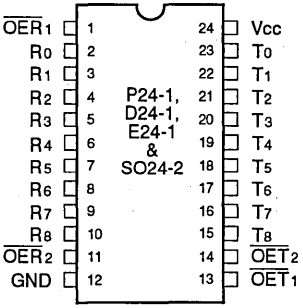


DIP/CERPACK/SOIC
TOP VIEW

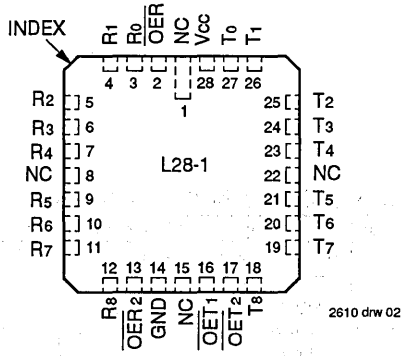


LCC
TOP VIEW

IDT54/74FCT863/864 9-BIT TRANSCEIVERS



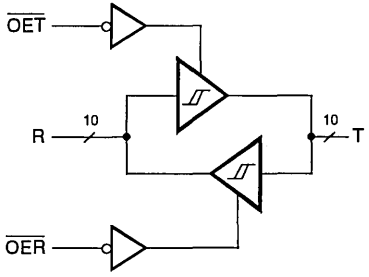
DIP/CERPACK/SOIC
TOP VIEW



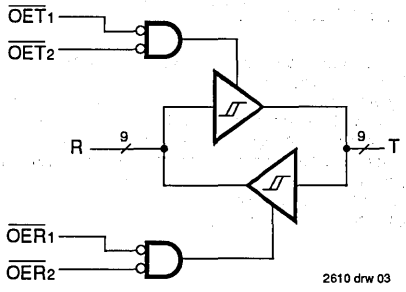
LCC
TOP VIEW

LOGIC SYMBOLS

IDT54/74FCT861



IDT54/74FCT863/864



PIN DESCRIPTION

Name	I/O	Description
IDT54/74FCT861		
$\overline{OER}$	I	When LOW in conjunction with $\overline{OET}$ HIGH activates the RECEIVE mode.
$\overline{OET}$	I	When LOW in conjunction with $\overline{OER}$ HIGH activates the TRANSMIT mode.
RI	I/O	10-bit RECEIVE input/output.
TI	I/O	10-bit TRANSMIT input/output.
IDT54/74FCT863/864		
$\overline{OER}$I	I	When LOW in conjunction with $\overline{OET}$I HIGH activates the RECEIVE mode.
$\overline{OET}$I	I	When LOW in conjunction with $\overline{OER}$I HIGH activates the TRANSMIT mode.
RI	I/O	9-bit RECEIVE input/output.
TI	I/O	9-bit TRANSMIT input/output.

2610 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2610 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

FUNCTION TABLE(1)

IDT54/74FCT861/863 (Non-inverting)

Inputs				Outputs		
$\overline{OET}$	$\overline{OER}$	RI	TI	RI	TI	Function
L	H	L	N/A	N/A	L	Transmitting
L	H	H	N/A	N/A	H	Transmitting
H	L	N/A	L	L	N/A	Receiving
H	L	N/A	H	H	N/A	Receiving
H	H	X	X	Z	Z	High Z

NOTE: 2610 tbl 03

1. H = HIGH, L = LOW, Z = High Impedance, X = Don't Care, N/A = Not Applicable.

FUNCTION TABLE(1)

IDT54/74FCT864 (Inverting)

Inputs				Outputs		
$\overline{OET}$	$\overline{OER}$	RI	TI	RI	TI	Function
L	H	L	N/A	N/A	H	Transmitting
L	H	H	N/A	N/A	L	Transmitting
H	L	N/A	L	H	N/A	Receiving
H	L	N/A	H	L	N/A	Receiving
H	H	X	X	Z	Z	High Z

NOTE: 2610 tbl 04

1. H = HIGH, L = LOW, Z = High Impedance, X = Don't Care, N/A = Not Applicable.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2610 tbl 06

1. This parameter is guaranteed by characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	—	—	–5[4]	µA
			V_I = GND	—	—	–5	
I_{IH}	Input HIGH Current (I/O pins Only)	V_{CC} = Max.	V_I = V_{CC}	—	—	15	
			V_I = 2.7V	—	—	15[4]	
I_{IL}	Input LOW Current (I/O pins Only)		V_I = 0.5V	—	—	–15[4]	
			V_I = GND	—	—	–15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–75	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
			I_{OH} = –15mA MIL.	2.4	4.3	—	
			I_{OH} = –24mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}[4]	
			I_{OL} = 32mA MIL.[5]	—	0.3	0.5	
			I_{OL} = 48mA COM'L.[5]	—	0.3	0.5	

2610 tbl 07

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. These are maximum I_{OL} values per output, for 10 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 480mA for commercial and 320mA for military. Derate I_{OL} for number of outputs exceeding 10 turned on simultaneously.

6

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OER}$ or $\overline{OET}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
		$\overline{OER}$ or $\overline{OET}$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5[5]	
		$\overline{OER}$ or $\overline{OET}$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	5.2	14.5[5]	

2610 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT861A/863A/864A				FCT861B/863B/864B				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay RI to TI or TI to RI FCT861/863	CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	6.0	1.5	6.5	ns
		CL = 300pF[3] RL = 500Ω	1.5	15.0	1.5	17.0	1.5	13.0	1.5	14.0	
tPLH tPHL	Propagation Delay RI to TI or TI to RI FCT864	CL = 50pF RL = 500Ω	1.5	7.5	1.5	9.0	1.5	5.5	1.5	6.5	ns
		CL = 300pF[3] RL = 500Ω	1.5	14.0	1.5	16.0	1.5	13.0	1.5	14.0	
tPZH tPZL	Output Enable Time $\overline{OET}$ to TI or $\overline{OER}$ to RI	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		CL = 300pF[3] RL = 500Ω	1.5	20.0	1.5	22.0	1.5	15.0	1.5	16.0	
tPHZ tPLZ	Output Disable Time $\overline{OET}$ to TI or $\overline{OER}$ to RI	CL = 5pF[3] RL = 500Ω	1.5	9.0	1.5	9.0	1.5	6.0	1.5	7.0	ns
		CL = 50pF RL = 500Ω	1.5	10.0	1.5	10.0	1.5	7.0	1.5	8.0	

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This condition guaranteed but not tested.

2610 tbl 09

6

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS MEMORY DRIVERS

PRELIMINARY
IDT54/74FBT2240
IDT54/74FBT2240A

FEATURES:

- IDT54/74FBT2240 equivalent to the 54/74BCT2240
- **IDT54/74FBT2240A 25% faster than the 2240**
- 25Ω output resistors reduce overshoot and undershoot when driving MOS RAMs
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Higher static VOH for improved noise immunity and reduced system power dissipation
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

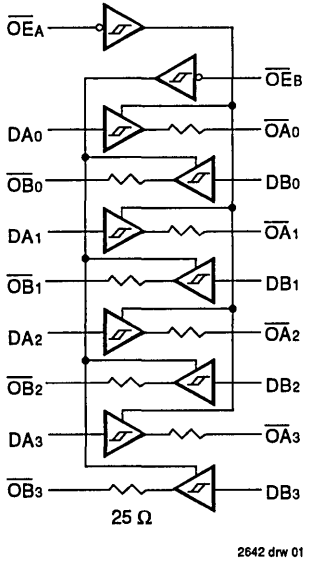
DESCRIPTION:

The FBT series of BiCMOS Memory Drivers is built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT2240 series are octal buffers/line drivers where each output is terminated with a 25Ω series resistor.

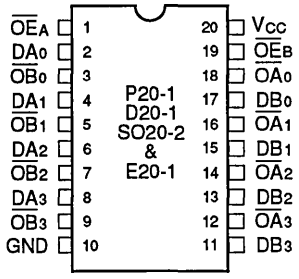
The FBT series of bus interface devices are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection. The output buffers are designed to guarantee a static VOH of 2.7V. This higher output level in the high state results in a significant reduction in overall system power dissipation and improved noise immunity when driving DRAMS and SRAMS.

FUNCTIONAL BLOCK DIAGRAM

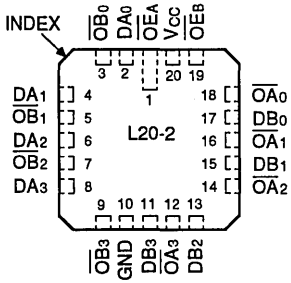


2642 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2642 drw 02

LCC
TOP VIEW

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
Dxx	Inputs
$\overline{O}$xx	Outputs

2642 tbl 01

FUNCTION TABLE[1]

Inputs		Output
$\overline{OE}_A$, $\overline{OE}_B$	Dxx	Oxx
L	L	H
L	H	L
H	X	Z

NOTE: 2642 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2642 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Type	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2642 tbl 04

1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	–10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	–50	
I_I	Input HIGH Current	V_{CC} = Max., V_{CC} (Max.)		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		–35	—	—	mA
I_{ODL}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		50	—	—	mA
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–75	—	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –300µA[4]	V_{HC}	V_{CC}	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –1mA	2.7	3.8	—	
			I_{OH} = –8mA	2.4	3.3	—	
			I_{OH} = –12mA	2.0	3.2	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 300µA[4]	—	GND	V_{LC}	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1mA	—	0.1	0.5	
			I_{OL} = 12mA	—	0.35	0.8	
V_H	Input Hysteresis	—		—	200	—	mV
I_{CCH} I_{CCZ} I_{CCL}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2642 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This condition is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.3	0.40	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	5.5	mA
		$\overline{OE}_A$ = $\overline{OE}_B$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	3.5	6.5	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	6.2	9.5[5]	
		$\overline{OE}_A$ = $\overline{OE}_B$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	8.2	17.5[5]	

NOTES: 2642 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL HIgh Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FBT2240				IDT54/74FBT2240A				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Dxx to $\overline{O}$xx	C_L = 50pF R_L = 500Ω	1.5	5.7	1.5	6.3	1.5	4.8	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	ns

NOTES: 2642 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

6

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS MEMORY DRIVERS

PRELIMINARY
IDT54/74FBT2244
IDT54/74FBT2244A

FEATURES:

- IDT54/74FBT2244 equivalent to the 54/74BCT2244
- **IDT54/74FBT2244A 25% faster than the 2244**
- 25Ω output resistors reduce overshoot and undershoot when driving MOS RAMs
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Higher static VOH for improved noise immunity and reduced system power dissipation.
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

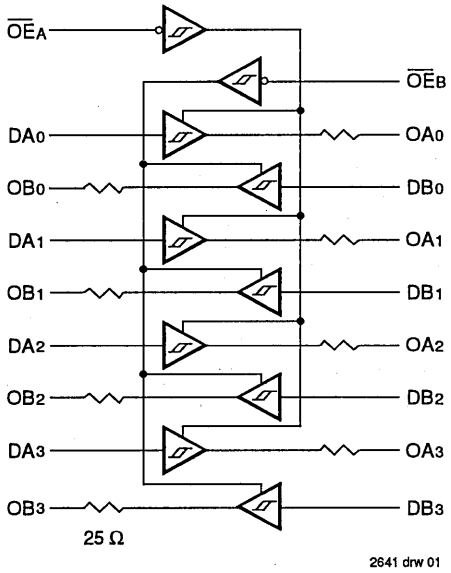
DESCRIPTION:

The FBT series of BiCMOS Memory Drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT2244 series are octal buffers/line drivers where each output is terminated with a 25Ω series resistor.

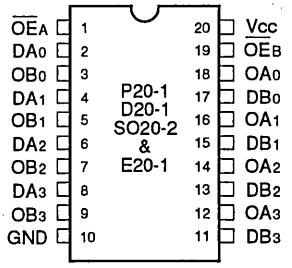
The FBT series of bus interface devices are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection. The output buffers are designed to guarantee a static VOH of 2.7V. This higher output level in the high state results in a significant reduction in overall system power dissipation and in improved noise immunity when driving DRAMS and SRAMS.

FUNCTIONAL BLOCK DIAGRAM

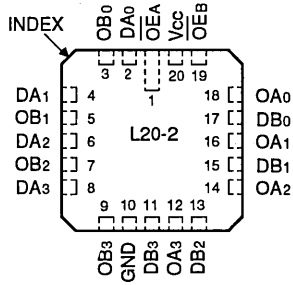


2641 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2641 drw 02

LCC
TOP VIEW

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs
Dxx	Inputs
Oxx	Outputs

2641 tbl 01

FUNCTION TABLE[1]

Inputs		Outputs
$\overline{OE}_A$, $\overline{OE}_B$	Dxx	Oxx
L	L	L
L	H	H
H	X	Z

2641 tbl 02

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2641 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Type	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2641 tbl 04

1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	–10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	–50	
I_I	Input HIGH Current	V_{CC} = Max., V_{CC} (Max.)		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		–35	—	—	mA
I_{ODL}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		50	—	—	mA
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–75	—	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –300µA[4]	V_{HC}	V_{CC}	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –1mA	2.7	3.8	—	
			I_{OH} = –8mA	2.4	3.3	—	
			I_{OH} = –12mA	2.0	3.2	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 300µA[4]	—	GND	V_{LC}	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1mA	—	0.1	0.5	
			I_{OL} = 12mA	—	0.35	0.8	
V_H	Input Hysteresis	—		—	200	—	mV
I_{CCH} I_{CCZ} I_{CCL}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES:
2641 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This condition is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.3	0.40	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	5.5	mA
		$\overline{OE}_A$ = $\overline{OE}_B$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	3.5	6.5	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	6.2	9.5[5]	
		$\overline{OE}_A$ = $\overline{OE}_B$ = GND Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	8.2	17.5[5]	

2641 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FBT2244				IDT54/74FBT2244A				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Dxx to Oxx	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	ns

2641 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

6

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS OCTAL TRANSPARENT LATCH DRIVERS

ADVANCE INFORMATION
IDT54/74FBT2373
IDT54/74FBT2373A

FEATURES:

- 25Ω output resistors reduce overshoot and undershoot when driving MOS RAMs
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Higher static VOH for improved noise immunity and reduced power dissipation.
- Low power in all three states
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

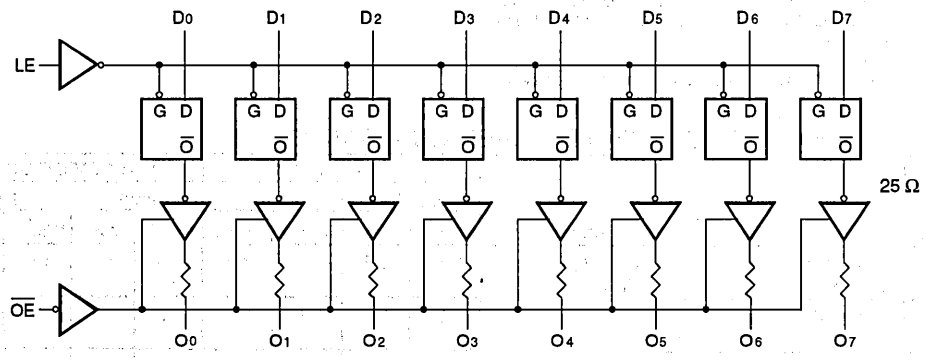
DESCRIPTION:

The FBT series of BiCMOS Latch Drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT2373 series are 3-state, 8-bit latches where each output is terminated with a 25Ω series resistor. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high-impedance state.

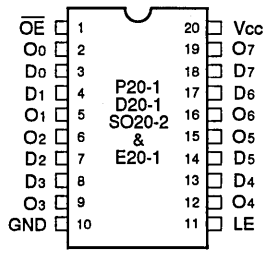
The FBT series of bus interface devices are ideal for driving large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection. The output buffers are designed to guarantee a static VOH of 2.7V. This higher output level in the high state will result in a significant reduction in overall system power dissipation and in improved noise immunity when driving DRAMS and SRAMS.

FUNCTIONAL BLOCK DIAGRAM

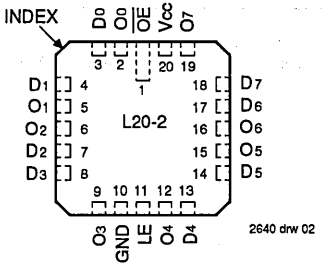


2640 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2640 drw 02

LCC
TOP VIEW

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
$D_0 - D_7$	Data Inputs
LE	Latch Enables Input (Active HIGH)
$\overline{OE}$	Output Enables Input (Active LOW)
$O_0 - O_7$	3-State Latch Outputs

2640 tbl 05

FUNCTION TABLE[1]

Inputs			Outputs
Dn	LE	$\overline{OE}$	On
H	H	L	H
L	H	L	L
X	L	L	NC
X	X	H	Z

NOTE:
2640 tbl 06

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   NC = No Change

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES:
2640 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Inputs and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Type	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
2640 tbl 02

1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	-10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_{CC} (Max.)		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		–35	—	—	mA
I_{ODL}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		50	—	—	mA
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–75	—	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –300µA[4]	V_{HC}	V_{CC}	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –1mA	2.7	3.8	—	
			I_{OH} = –8mA	2.4	3.3	—	
			I_{OH} = –12mA	2.0	3.2	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 300µA[4]	—	GND	V_{LC}	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1mA	—	0.1	0.5	
			I_{OL} = 12mA	—	0.35	0.8	
V_H	Input Hysteresis	—		—	200	—	mV
I_{CCH} I_{CCZ} I_{CCL}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2640 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This condition is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND, LE = Vcc One Input Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	0.3	0.4	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	3.2	5.5	mA
		$\overline{OE}$ = GND, LE = Vcc One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	3.5	6.5	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	6.2	9.5[5]	
		$\overline{OE}$ = GND, LE = Vcc Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	8.2	17.5[5]	

NOTES: 2640 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTLI inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FBT2373				IDT54/74FBT2373A				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	8.5	1.5	5.2	1.5	5.6	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_n		2.0	9.3	2.0	10.1	2.0	8.5	2.0	9.8	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	12.0	1.5	12.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.4	1.5	8.1	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW D_n to LE		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW D_n to LE		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	LE Pulse Width HIGH or LOW		6.0	—	6.0	—	5.0	—	6.0	—	ns

NOTES: 2640 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

Integrated Device Technology, Inc.

HIGH SPEED BiCMOS 10-BIT MEMORY DRIVERS

ADVANCE INFORMATION
IDT54/74FBT2827A/B
IDT54/74FBT2828A/B

FEATURES

- IDT54/74FBT2827A/2828A is equivalent to 54/74BCT2827A/2828A
- **IDT54/74FBT2827B/2828B is 30% faster than BCT**
- 25Ω output resistors reduce overshoot and undershoot when driving MOS RAMs
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Higher static VOH for improved noise immunity and reduced system power dissipation
- Low power in all three states
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

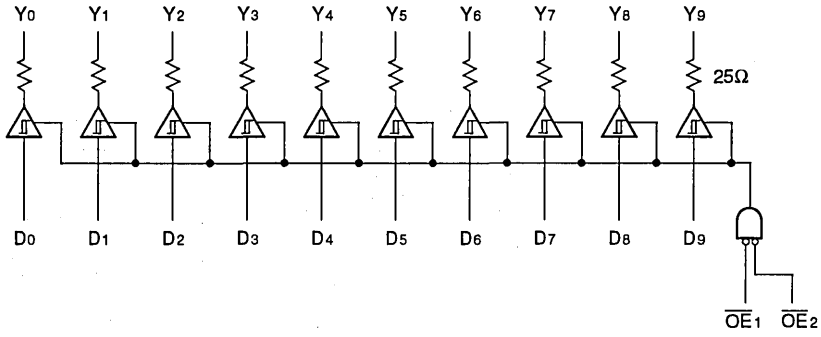
DESCRIPTION

The FBT series of BiCMOS Memory Drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT2827A/B and IDT54/74FBT2828A/B are 3-state 10-bit buffers where each output is terminated with a 25Ω series resistor. The output buffers are enabled when the two Active-LOW output enable pins are logic LOW.

The FBT series of memory line drivers are ideal for use in designs needed to drive large capacitive loads, with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection. They are also designed for rail-to-rail output switching. This higher output level in the high state will result in significant reduction in overall system power dissipation.

FUNCTIONAL BLOCK DIAGRAM



2516 drw 01

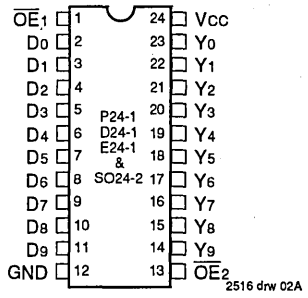
PRODUCT SELECTOR GUIDE

	10-Bit Memory Driver
Non-inverting	IDT 54/74FBT2827A/B
Inverting	IDT 54/74FBT2828A/B

2516 tbl 01

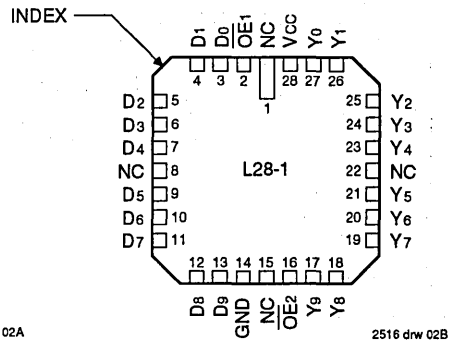
BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2516 drw 02A

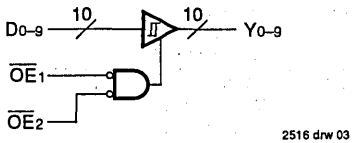
DIP/CERPACK/SOIC
TOP VIEW



2516 drw 02B

LCC
TOP VIEW

LOGIC SYMBOL



2516 drw 03

PIN DESCRIPTION

Name	I/O	Description
$\overline{OE}_1$ $\overline{OE}_2$	I	When both are LOW, the outputs are enabled. When either one or both are HIGH the outputs are High Z.
D_I	I	10-bit data input.
Y_I	O	10-bit data output.

2516 tbl 02

FUNCTION TABLES

IDT54/74FBT2827A/B (Non-Inverting)[1]

Inputs			Output	
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	Function
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	3-State
X	H	X	Z	

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

2516 tbl 03

IDT54/74FBT2828A/B (Inverting)[1]

Inputs			Output	
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	Function
L	L	L	H	Transparent
L	L	H	L	
H	X	X	Z	3-State
X	H	X	Z	

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

2516 tbl 04

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ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2516 tbl 06

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Condition	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2516 tbl 07

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 2.7V	—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_I = 0.5V	—	—	–10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	–50	
I_I	Input HIGH Current	V_{CC} = Max., V_I = 5.5V		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		–35	—	—	mA
I_{ODL}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		50	—	—	mA
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–60	—	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –300µA[4]	V_{HC}	V_{CC}	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –1mA	2.4	3.3	—	
			I_{OH} = –12mA	2.0	3.2	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 300µA[4]	—	GND	V_{LC}	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1mA	—	0.1	0.5	
			I_{OL} = 12mA	—	0.35	0.8	
V_H	Input Hysteresis	—		—	200	—	mV
I_{CCH} I_{CCZ} I_{CCL}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES: 2516 tbl 05

1. For condition shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This condition is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Condition[1]		Min.	Typ.	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE_1}$ = $\overline{OE_2}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.7	4.0	mA
		$\overline{OE_1}$ = $\overline{OE_2}$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.0	7.8[5]	
		$\overline{OE_1}$ = $\overline{OE_2}$ = GND Ten Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	6.5	17.8[5]	

NOTES: 2516 tbl 08

1. For condition shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. I_C = $I_{QUIESCENT}$ = I_{INPUTS} + $I_{DYNAMIC}$
   I_C = I_{CC} + ΔI_{CC} $D_H N_T$ + I_{CCD} (f_{CP}/2 + $f_i N_i$)
   I_{CC} = Quiescent Current
   ΔI_{CC} = Quiescent Current
   D_H = Duty Cycle for a TTL High Input (V_{IN} = 3.4V)
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in MHz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

		FBT2827A				FBT2827B			
		Commercial		Military		Commercial		Military	
Symbol	Parameter	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.
t_{PHL} t_{PLH}	Prop Delay, Di to Yi	1.5	7.0	1.5	7.5	1.5	5.0	1.5	6.5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Yi	1.5	13.0	1.5	14	1.5	8.0	1.5	9.0
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Yi	1.5	13.0	1.5	14	1.5	7.0	1.5	8.0

		FBT2828A				FBT2828B			
		Commercial		Military		Commercial		Military	
Symbol	Parameter	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.
t_{PHL} t_{PLH}	Prop Delay, Di to Yi	1.5	8.0	1.5	8.5	1.5	5.5	1.5	6.5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Yi	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Yi	1.5	14.0	1.5	15.0	1.5	7.0	1.5	8.0

NOTES: 2516 tbl 09

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

6

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS 10-BIT MEMORY LATCHES

IDT54/74FBT2841A
IDT54/74FBT2841B

FEATURES:

- 25Ω output resistors reduce overshoot and undershoot when driving MOS RAMs
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Low power in all three states
- ± 10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

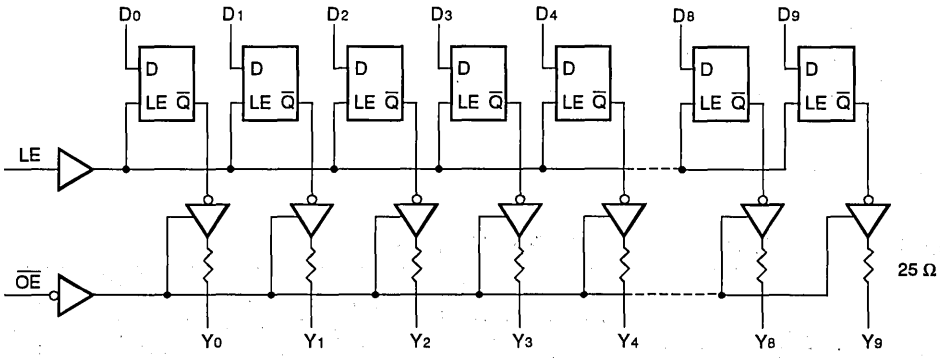
DESCRIPTION:

The FBT series of BiCMOS Memory Drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT2841 series are 3-state, 10-bit latches where each output is terminated with a 25Ω series resistor.

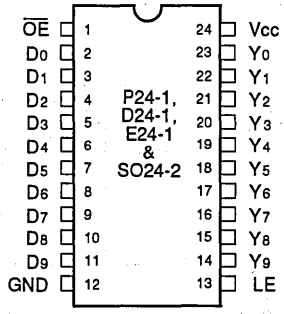
The FBT series of memory line drivers are ideal for use in designs needed to drive large capacitive loads with low static (DC) current loading. They are also designed for rail-to-rail output switching. This higher output level in the high state will result in a significant reduction in overall system power dissipation.

FUNCTIONAL BLOCK DIAGRAM

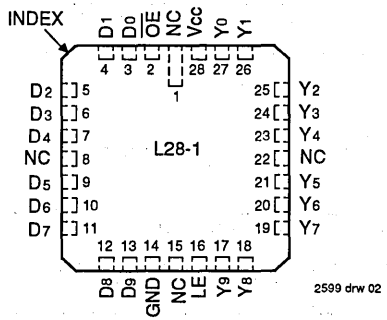


2599 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



2599 drw 02

LCC
TOP VIEW

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Name	I/O	Description
$D_0 - D_9$	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
$Y_0 - Y_9$	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_I are in the high-impedance (off) state.

2599 tbl 05

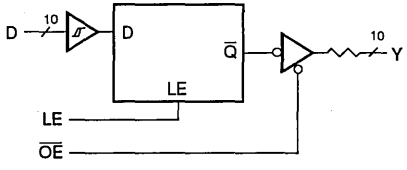
FUNCTION TABLE[1]

Inputs			Internal	Outputs	
$\overline{OE}$	LE	D_I	Q_I	Y_I	Function
H	X	X	X	Z	High Z
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched (High Z)
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched

NOTE: 2599 tbl 06

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, Z = High Impedance

LOGIC SYMBOL



2599 drw 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2599 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Inputs and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2599 tbl 02

1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	–10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	–50	
I_I	Input HIGH Current	V_{CC} = Max., V_{CC} (Max.)		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		–35	—	—	mA
I_{ODL}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		50	—	—	mA
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–75	—	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –300µA[4]	V_{HC}	V_{CC}	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –1mA	2.7	3.8	—	
			I_{OH} = –8mA	2.4	3.3	—	
			I_{OH} = –12mA	2.0	3.2	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 300µA[4]	—	GND	V_{LC}	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1mA	—	0.1	0.5	
			I_{OL} = 12mA	—	0.35	0.8	
V_H	Input Hysteresis	—		—	200	—	mV
I_{CCH} I_{CCZ} I_{CCL}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2599 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This condition is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND One Input Toggling LE = V_{CC} 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.3	0.4	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	5.5	mA
		$\overline{OE}$ = GND, LE = V_{CC} One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	3.5	6.5	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	7.7	11.5[5]	
		$\overline{OE}$ = GND, LE = V_{CC} Ten Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	10.2	21.5[5]	

NOTES:
2599 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			54/74FBT2841A				54/74FBT2841B				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_i to Y_i (LE = HIGH)	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	10.0	1.5	6.5	1.5	7.5	ns
t_{SU}	Data to LE Set-up Time		2.5	—	2.5	—	2.5	—	2.5	—	ns
t_H	Data to LE Hold Time		2.5	—	3.0	—	2.5	—	2.5	—	ns
t_{PLH} t_{PHL}	Propagation Delay LE to Y_i		1.5	12.0	1.5	13.0	1.5	8.0	1.5	10.5	ns
t_W	LE Pulse Width[3] HIGH		4.0	—	5.0	—	4.0	—	4.0	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_i		1.5	11.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Y_i		1.5	8.0	1.5	10.0	1.5	7.0	1.5	7.5	ns

NOTES:
2599 tbl 07

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed, but not tested.

3.3V LOGIC AND 5V-3.3V TRANSLATOR PRODUCTS

The demand for 3.3V logic functions is increasing dramatically. In particular, the introduction of 3.3V processors, coupled with the availability of 3.3V ASIC and RAM, has fueled a rapid growth in 3.3V portable personal computer and workstation development. IDT's new 3.3V bus interface logic devices, (*74FCT163xxx* and the *74FCT3xxx*) and 5V-to-3.3V translator (*74FCT164245T*) are designed to support the exploding demand generated by these new systems. The translator chip, in particular, solves the designer's number one problem when designing with 3.3V; how to interface 3.3V and 5V on a single bus. IDT offers 3.3V logic in both Octal and Double Density configurations. Pinouts and AC specifications of both configurations match those of available 5V functions.

3.3V Standard Logic Functions

IDT's new family of 3.3V logic devices has been developed on today's advanced sub-half-micron CEMOS process, providing low-voltage compatibility without sacrificing high performance. The 3.3V family consists of functions offered in 20-, 24-, 48-, and 56-pin new fine-pitch Shrink Small Outline Packages (SSOP). Both the Double Density and the Octal 3.3V functions have the same function and pin-outs as their 5V counterparts, making it easy to upgrade existing designs. AC specifications also match those of the 5V FCT functions. Because of the high speeds, the 3.3V logic family is the ideal choice for redesigned 5V systems, especially those that maintain clock rates above 25MHz. IDT's 3.3V products have been designed to operate from a regulated 3.3V supply and are not simply "recharacterized" or "derated" 5V CMOS products. All 3.3V products will also operate functionally with Vcc as low as 2.5V, making them an excellent choice for non-regulated, battery operated system applications.

5V-to-3.3V Bidirectional Translator

The 5V-to-3.3V translator chip was developed to complement the 3.3V-only products, providing an immediate solution to the problems incurred from interfacing 5V to 3.3V logic. It is clear that not all components required to complete a 3.3V system are immediately available. Therefore, initial systems will require some combination of 3.3V and 5V components, creating a need for logic voltage translation. In bidirectional applications, there is an inherent problem; since all 3.3V drivers have a parasitic diode to Vcc, there is a chance that a 5V signal will source current into the 3.3V device (specifically when the 5V signal is >3.3V + Vd). If maximum current ratings are exceeded, the 3.3V device can be damaged. IDT's translator can also serve as an interface between a 3.3V system and 5V peripherals.

5V-to-3.3V Unidirectional Translators

In many applications, there is a need to communicate directly from 5V components to 3.3V components. In these unidirectional applications, standard unidirectional 3.3V-only functions can operate as effective voltage translators. Because IDT's Octal and Double Density 3.3V logic has no input clamp diodes to Vcc and high breakdown voltages, the inputs can easily be driven by 5V signals without any system problems. IDT's unidirectional 3.3V devices make excellent one-way 5V-to-3.3V translators.

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Integrated Device Technology, Inc.

3.3V CMOS 16-BIT BUFFER/LINE DRIVER

PRELIMINARY
IDT54/74FCT163244/A

FEATURES:

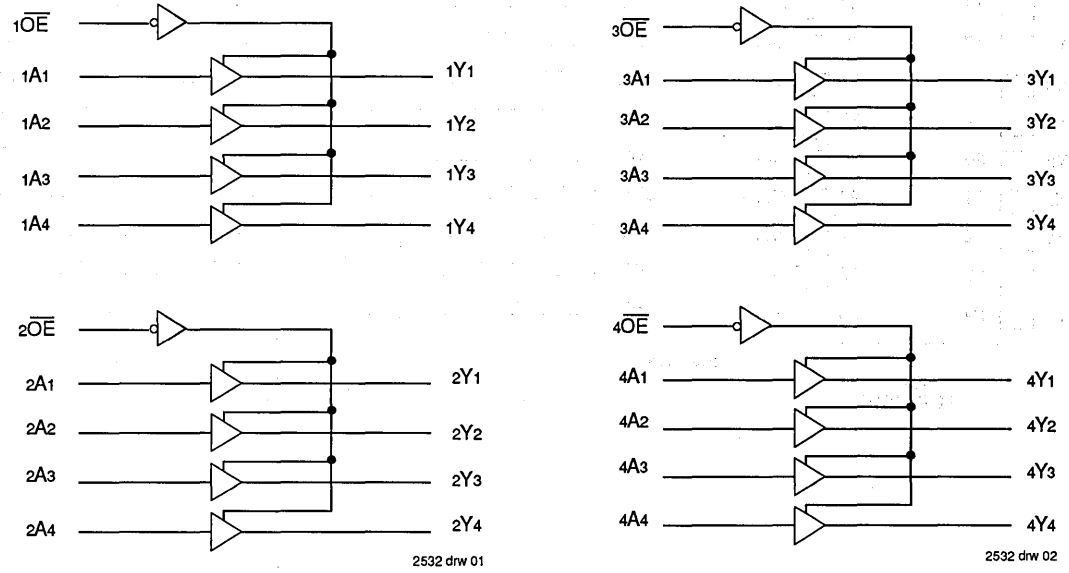
- 0.5 MICRON CEMOS™ Technology
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **Can serve as 5V to 3.3V translator**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V
- CMOS power levels (0.16mW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

DESCRIPTION:

The IDT54/74FCT163244/A 16-bit buffer/line drivers are built using advanced CEMOS, dual metal CMOS technology. These high-speed, low-power devices offer bus/backplane interface capability with improved packing density. These devices have a flow-through organization for ease of board layout. The three-state controls are designed to operate these devices in a Quad-Nibble, Dual-Byte or single 16-bit word mode. All inputs are designed with hysteresis for improved noise margin.

The inputs of IDT54/74FCT163244/A can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V supply system. Thus, the IDT54/74FCT163244/A can be used as buffers to connect 5V components to a 3.3V bus.

FUNCTIONAL BLOCK DIAGRAM



2532 drw 01

2532 drw 02

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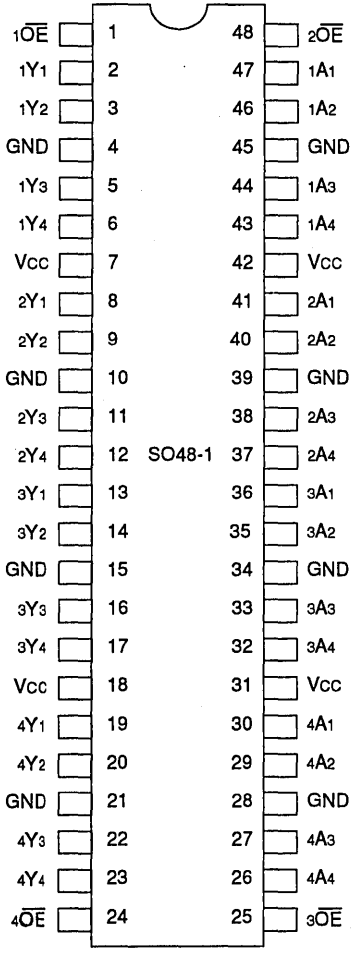
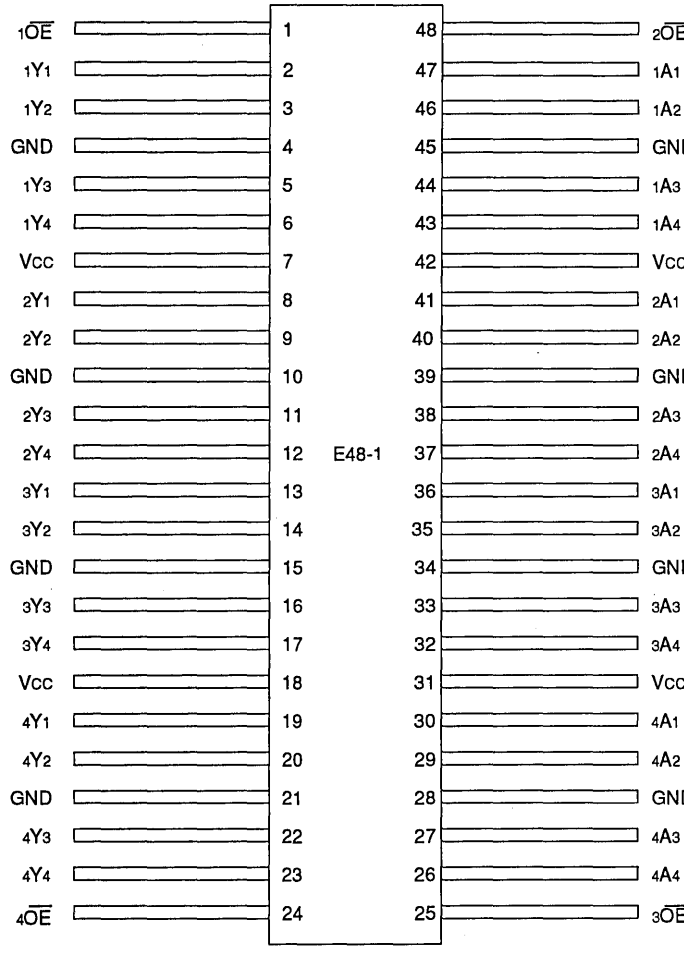
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2532 drw 03

SSOP
TOP VIEW



2532 drw 04

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}$	3–State Output Enable Inputs (Active LOW)
xAx	Data Inputs
xYx	3-State Outputs

2532 tbl 01

FUNCTION TABLE[1]

Inputs		Outputs
$x\overline{OE}$	xAx	xYx
L	L	L
L	H	H
H	X	Z

2532 tbl 02

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

NOTES: 2532 lnk 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2532 lnk 04
1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 3.3V ± 0.3V; Military: T_A = –55°C to +125°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = 5.5V	—	—	±5	µA
	Input HIGH Current (I/O pins)		V_I = V_{CC}	—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)		V_I = GND	—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.5	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

2532 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} - 0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} − 0.6V[3]	—	2.0	30	µA
			V_{IN} = 2.4V[3]	—	70	500	
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open 50% Duty Cycle $x\overline{OE}$ = GND One Input Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	50	75	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz	V_{IN} = V_{CC} − 0.6V V_{IN} = GND	—	0.6	2.3	mA
		50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	V_{IN} = 2.4V V_{IN} = GND	—	0.6	2.5	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	V_{IN} = V_{CC} − 0.6V V_{IN} = GND	—	2.1	4.7[5]	
		50% Duty Cycle $x\overline{OE}$ = GND Sixteen Bits Toggling	V_{IN} = 2.4V V_{IN} = GND	—	2.6	8.5[5]	

2532 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT163244				FCT163244A				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2532 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Integrated Device Technology, Inc.

3.3V CMOS 16-BIT BIDIRECTIONAL TRANSCEIVERS

PRELIMINARY
IDT54/74FCT163245/A

FEATURES:

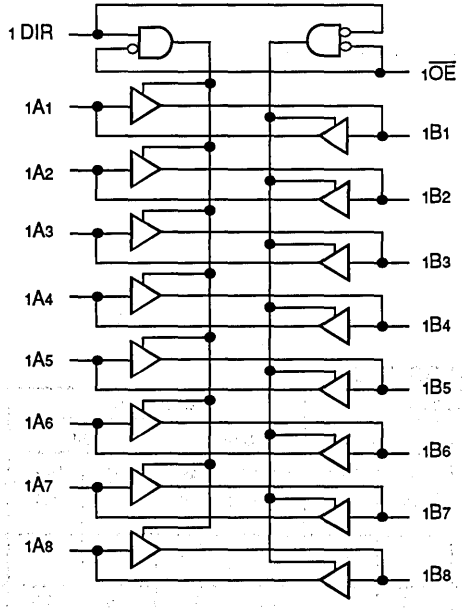
- 0.5 MICRON CEMOS™ Technology
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V
- CMOS power levels (0.16mW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

DESCRIPTION:

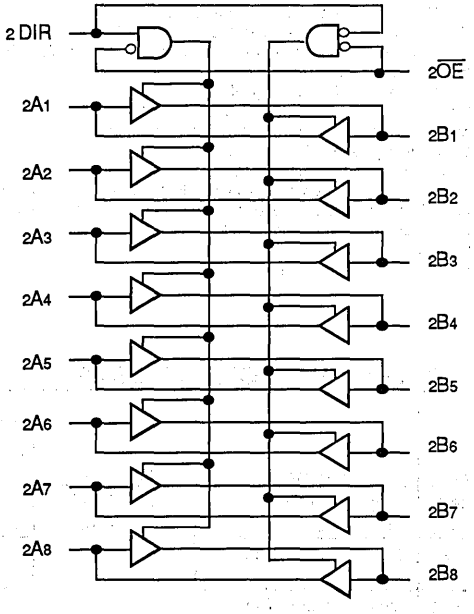
The IDT54/74FCT163245/A 16-bit transceivers are built using advanced CEMOS, dual metal CMOS technology. These high-speed, low-power transceivers are ideal for synchronous communication between two busses (A and B). The Direction and Output Enable controls are designed to operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver. The direction control pin (xDIR) controls the direction of data flow. The output enable pin ($x\overline{OE}$) overrides the direction control and disables both ports. All inputs are designed with hysteresis for improved noise margin.

The xDIR and $x\overline{OE}$ control inputs of these transceivers can be driven from either 3.3V or 5V devices. This feature allows added flexibility when used in a mixed 3.3V/5V supply environment.

FUNCTIONAL BLOCK DIAGRAM



2554 drw 01



2554 drw 02

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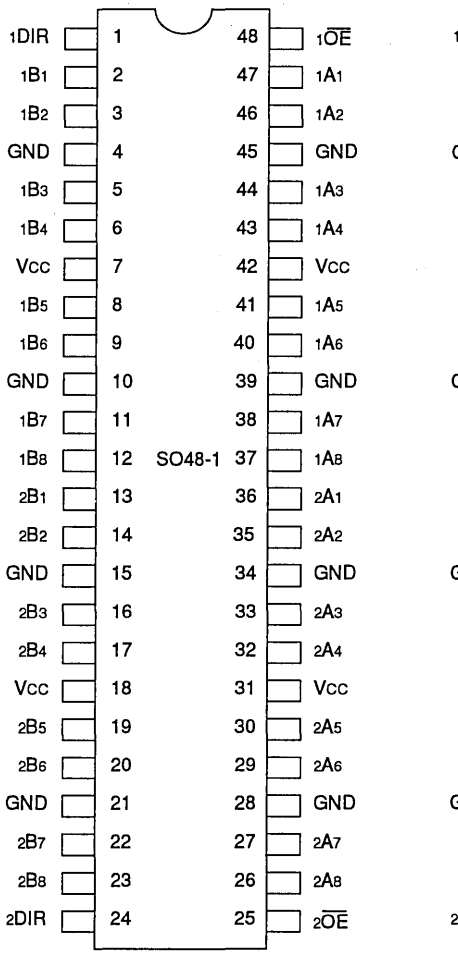
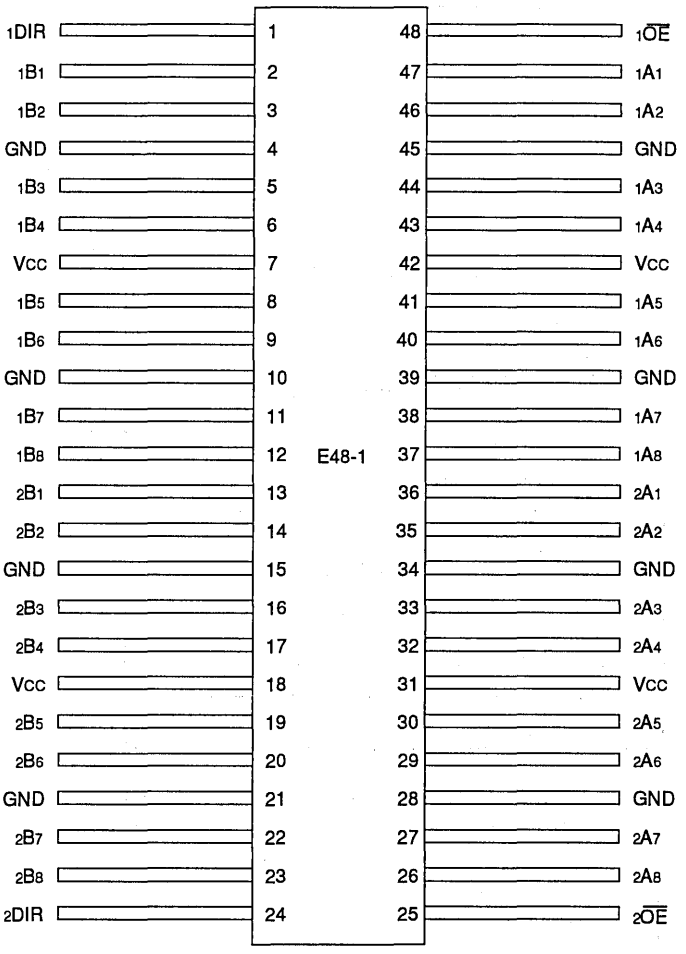
PIN CONFIGURATIONS



2554 drw 03

SSOP
TOP VIEW



2554 drw 04

CERPACK
TOP VIEW

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PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}$	Output Enable Input (Active LOW)
xDIR	Direction Control Input
xAx	Side A Inputs or 3-State Outputs
xBx	Side B Inputs or 3-State Outputs

2554 tbl 01

FUNCTION TABLE[1]

Inputs		Outputs
$x\overline{OE}$	xDIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

2554 tbl 02

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

NOTES: 2554 lnk 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2554 lnk 04
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = –40°C to +85°C, V_{CC} = 3.3V ± 0.3V; Military: T_A = –55°C to +125°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = 5.5V	—	—	±5	µA
	Input HIGH Current (I/O pins)		V_I = V_{CC}	—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)		V_I = GND	—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.5	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

2554 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} - 0.6V at rated current.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} − 0.6V[3]	—	2.0	30	µA
			V_{IN} = 2.4V[3]	—	70	500	
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = xDIR = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	50	75	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi =10MHz 50% Duty Cycle $x\overline{OE}$ = xDIR = GND One Bit Toggling	V_{IN} = V_{CC} − 0.6V V_{IN} = GND	—	0.6	2.3	mA
			V_{IN} = 2.4V V_{IN} = GND	—	0.6	2.5	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = xDIR = GND Sixteen Bits Toggling	V_{IN} = V_{CC} − 0.6V V_{IN} = GND	—	2.1	4.7[5]	
			V_{IN} = 2.4V V_{IN} = GND	—	2.6	8.5[5]	

NOTES:

2554 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT163245				FCT163245A				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	7.5	1.5	4.6	1.5	4.9	ns
t_{PZH} t_{PZL}	Output Enable Time $x\overline{OE}$ to A or B		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $x\overline{OE}$ to A or B		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	ns
t_{PZH} t_{PZL}	Output Enable Time xDIR to A or B[3]		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time xDIR to A or B[3]		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	ns
$t_{SK(o)}$	Output Skew[4]		—	0.5	—	0.5	—	0.5	—	0.5	ns

NOTES:

2554 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Integrated Device Technology, Inc.

3.3V CMOS 16-BIT TRANSPARENT LATCH

PRELIMINARY
IDT54/74FCT163373/A

FEATURES:

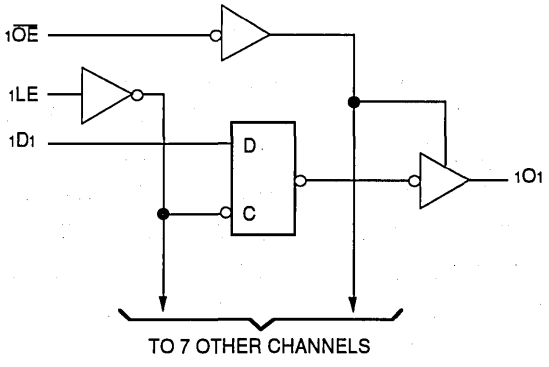
- 0.5 MICRON CEMOS™ Technology
- **Typical tsk(o) (Output Skew) < 250ps**
- **Can serve as 5V to 3.3V translator**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V
- CMOS power levels (0.16mW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

DESCRIPTION:

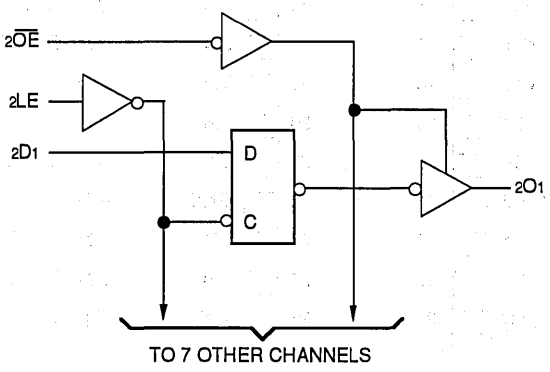
The IDT54/74FCT163373/A 16-bit transparent D-type latches are built using advanced CEMOS, dual metal CMOS technology. These high-speed, low-power latches are ideal for temporary storage of data. They can be used for implementing memory address latches, I/O ports, and bus drivers. The Output Enable and Latch Enable controls are organized to operate each device as two 8-bit latches or one 16-bit latch. Flow-through organization of signal pins facilitates ease of layout. All inputs are designed with hysteresis for improved noise margin.

The inputs of IDT54/74FCT163373/A can be driven from either 3.3V or 5V devices. This feature allows the use of these transparent latches as translators in a mixed 3.3V/5V supply system. With xLE inputs HIGH, the IDT54/74FCT163373/A can be used as buffers to connect 5V components to a 3.3V bus.

FUNCTIONAL BLOCK DIAGRAM



2601 drw 01



2601 drw 02

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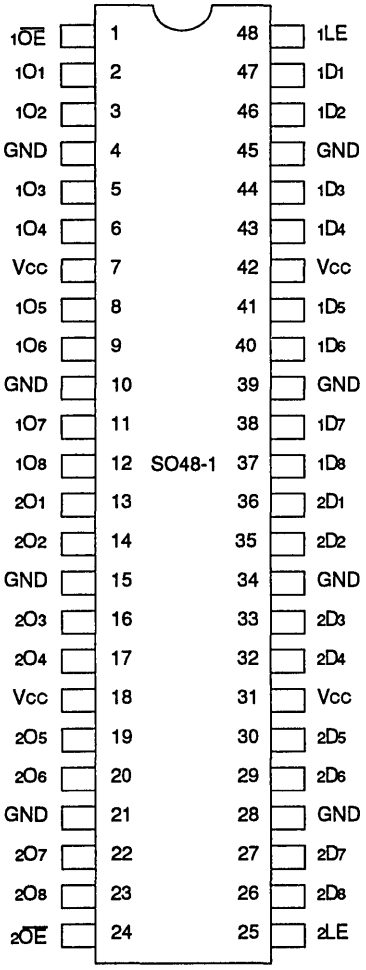
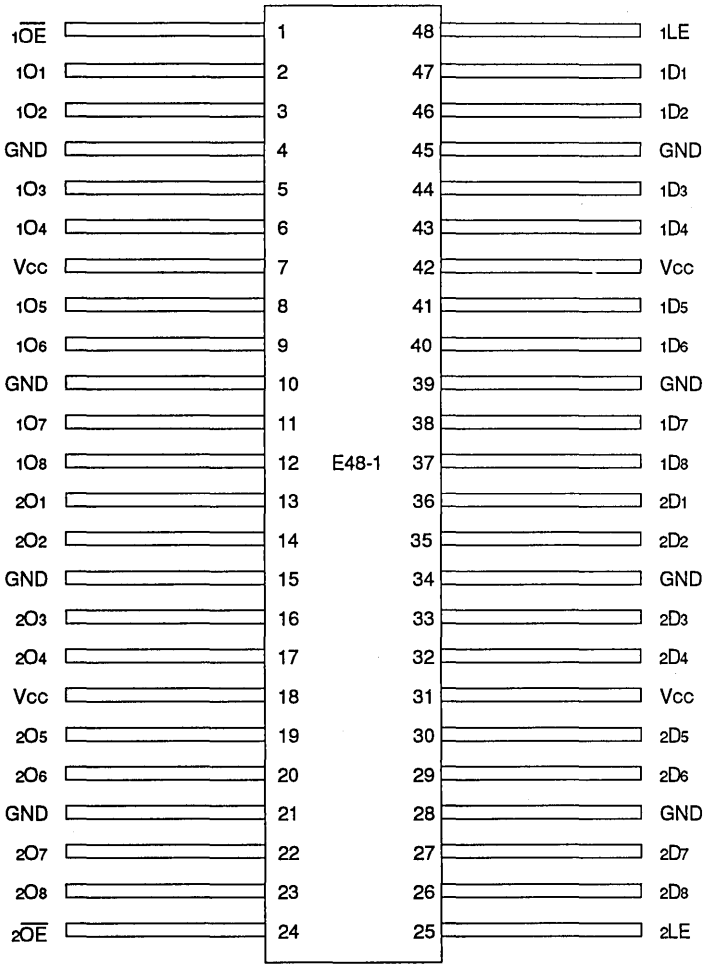
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2601 drw 03

SSOP
TOP VIEW



2601 drw 04

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xLE	Latch Enable Inputs (Active HIGH)
$x\overline{OE}$	Output Enable Inputs (Active LOW)
xOx	3-State Outputs

2601 tbl 01

FUNCTION TABLE[1]

Inputs			Outputs
xDx	xLE	$x\overline{OE}$	xOx
H	H	L	H
L	H	L	L
X	X	H	Z

NOTE: 2601 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

NOTES: 2601 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2601 lnk 04

1. This parameter is measured at characterization but not tested.

7

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 3.3V ± 0.3V; Military: T_A = –55°C to +125°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = 5.5V	—	—	±5	µA
	Input HIGH Current (I/O pins)		V_I = V_{CC}	—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)		V_I = GND	—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.5	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

NOTES:

2601 lnk 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} - 0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V[3]	—	2.0	30	µA
			V_{IN} = 2.4V[3]	—	70	500	
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	50	75	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi =10MHz 50% Duty Cycle $x\overline{OE}$ = GND xLE = V_{CC} One Bit Toggling	V_{IN} = V_{CC} – 0.6V V_{IN} = GND	—	0.6	2.3	mA
			V_{IN} = 2.4V V_{IN} = GND	—	0.6	2.5	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = GND xLE = V_{CC} Sixteen Bits Toggling	V_{IN} = V_{CC} – 0.6V V_{IN} = GND	—	2.1	4.7[5]	
			V_{IN} = 2.4V V_{IN} = GND	—	2.6	8.5[5]	

2601 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT163373				FCT163373A				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay xDx to xOx	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	8.5	1.5	5.2	1.5	5.6	ns
t_{PLH} t_{PHL}	Propagation Delay xLE to xOx		2.0	13.0	2.0	15.0	2.0	8.5	2.0	9.8	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	12.0	1.5	13.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.5	1.5	10.0	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW, xDx to xLE		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, xDx to xLE		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	xLE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2601 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Integrated Device Technology, Inc.

3.3V CMOS 16-BIT REGISTER (3-STATE)

PRELIMINARY
IDT54/74FCT163374/A

FEATURES:

- 0.5 MICRON CEMOS™ Technology
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **Can serve as 5V to 3.3V translator**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V
- CMOS power levels (0.16mW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

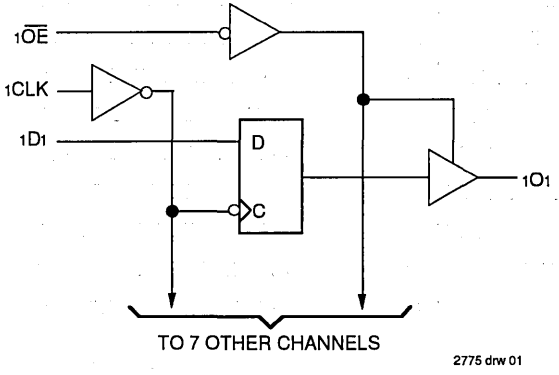
DESCRIPTION:

The IDT54/74FCT163374/A 16-bit edge-triggered D-type registers are built using advanced CEMOS, dual metal CMOS technology. These high-speed, low-power registers are ideal for use as buffer registers for data synchronization and storage. The Output Enable ($x\overline{OE}$) and clock (xCLK) controls are organized to operate each device as two 8-bit registers or one 16-bit register with common clock. Flow-through organization of signal pins facilitates ease of layout. All inputs are designed with hysteresis for improved noise margin.

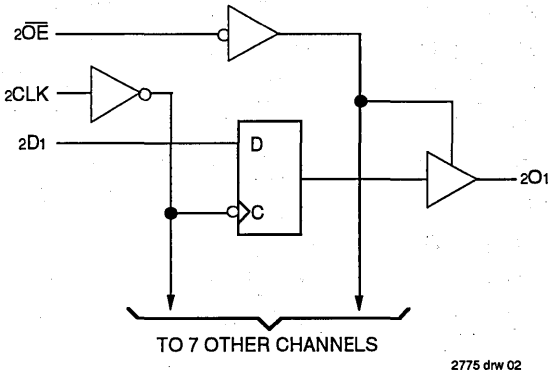
The inputs of IDT54/74FCT163374/A can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V supply system.

Thus, the IDT54/74FCT163374/A can be used as an interface between 5V components and a 3.3V bus.

FUNCTIONAL BLOCK DIAGRAM



2775 drw 01



2775 drw 02

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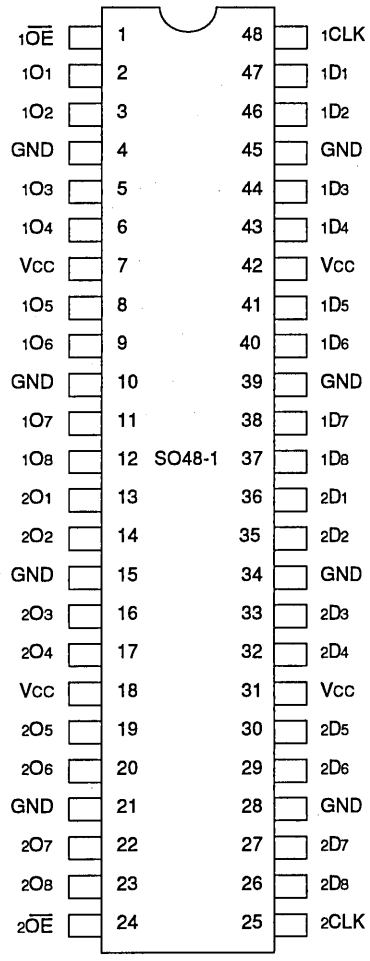
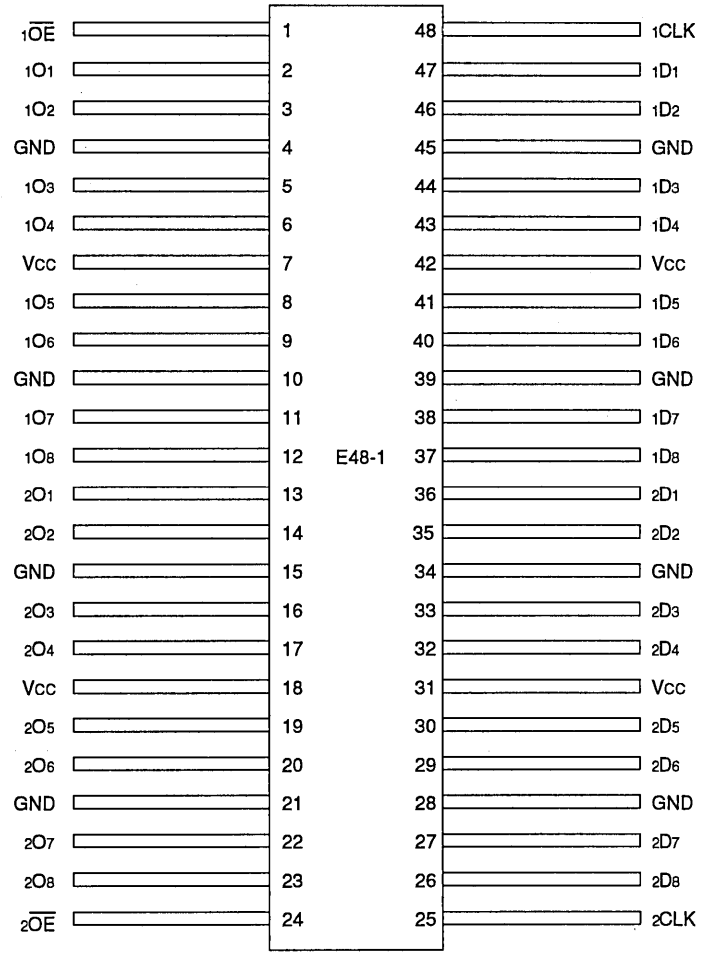
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2775 drw 03

SSOP
TOP VIEW



2775 drw 04

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xCLK	Clock Inputs
xOx	3-State Outputs.
$x\overline{OE}$	3-State Output Enable Input (Active LOW)

2775 tbl 01

FUNCTION TABLE[1]

Function	Inputs			Outputs
	xDx	xCLK	$x\overline{OE}$	xOx
Hi-Z	X	L	H	Z
	X	H	H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH transition

2775 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

2775 lnk 03

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE:
1. This parameter is measured at characterization but not tested.

2775 lnk 04

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 3.3V ± 0.3V; Military: T_A = –55°C to +125°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = 5.5V	—	—	±5	µA
	Input HIGH Current (I/O pins)		V_I = V_{CC}	—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)		V_I = GND	—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.5	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

2775 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} - 0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V[3]	—	2.0	30	µA
			V_{IN} = 2.4V[3]	—	70	500	
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = GND 50% Duty Cycle One Input Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	50	75	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $x\overline{OE}$ = GND f_i = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = V_{CC} – 0.6V V_{IN} = GND	—	0.6	2.3	mA
			V_{IN} = 2.4V V_{IN} = GND	—	0.6	2.8	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $x\overline{OE}$ = GND f_i = 2.5MHz 50% Duty Cycle Sixteen Bits Toggling	V_{IN} = V_{CC} – 0.6V V_{IN} = GND	—	2.6	5.5[5]	
			V_{IN} = 2.4V V_{IN} = GND	—	3.2	9.8[5]	

2775 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

7

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT163374				FCT163374A				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay xCLK to xOx	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	11.0	2.0	6.5	2.0	7.2	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	12.5	1.5	14.0	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	8.0	1.5	8.0	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW, xDx to xCLK		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, xDx to xCLK		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	xCLK Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

2775 tbl 07

Integrated Device Technology, Inc.

3.3V CMOS 18-BIT REGISTERED TRANSCEIVER

PRELIMINARY
IDT54/74FCT163501/A

FEATURES:

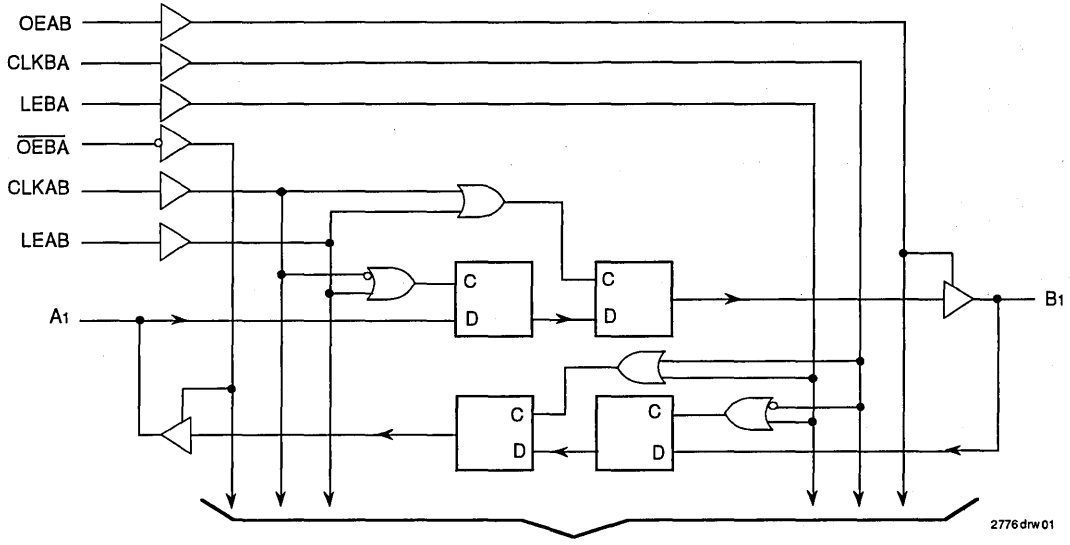
- 0.5 MICRON CEMOS™ Technology
- **Typical tsk(o) (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V
- CMOS power levels (0.16mW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

DESCRIPTION:

The IDT54/74FCT163501/A 18-bit registered transceivers are built using advanced CEMOS, dual metal CMOS technology. These high-speed, low-power 18-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes. Data flow in each direction is controlled by output-enable (OEAB and $\overline{OEBA}$), latch enable (LEAB and LEBA) and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB. OEAB performs the output enable function on the B port. Data flow from B port to A port is similiar but requires using $\overline{OEBA}$, LEBA and CLKBA. Flow-through organization of signal pins facilitates ease of layout. All inputs are designed with hysteresis for improved noise margin.

The control inputs of IDT54/74FCT163501/A can be driven from either 3.3V or 5V devices. This feature allows added flexibility when used in a mixed 3.3V/5V supply system. With LExx input HIGH, the IDT54/74FCT163501/A can be used as buffers to connect 5V components to a 3.3V bus.

FUNCTIONAL BLOCK DIAGRAM



TO 17 OTHER CHANNELS

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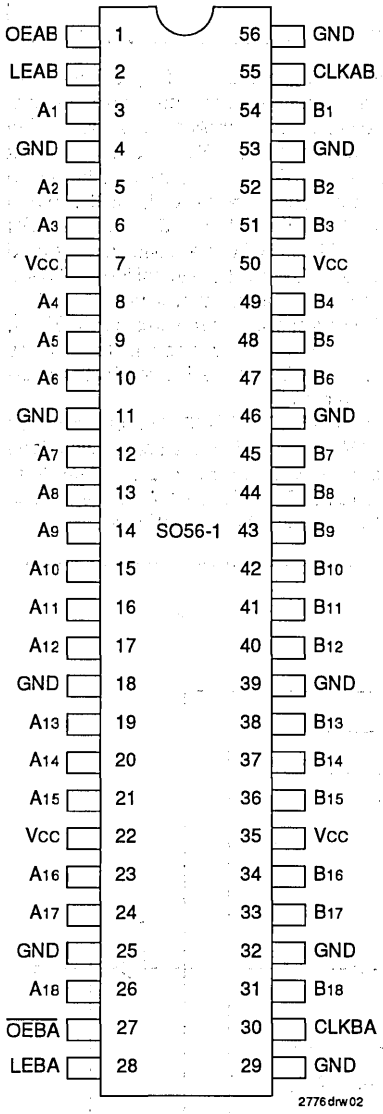
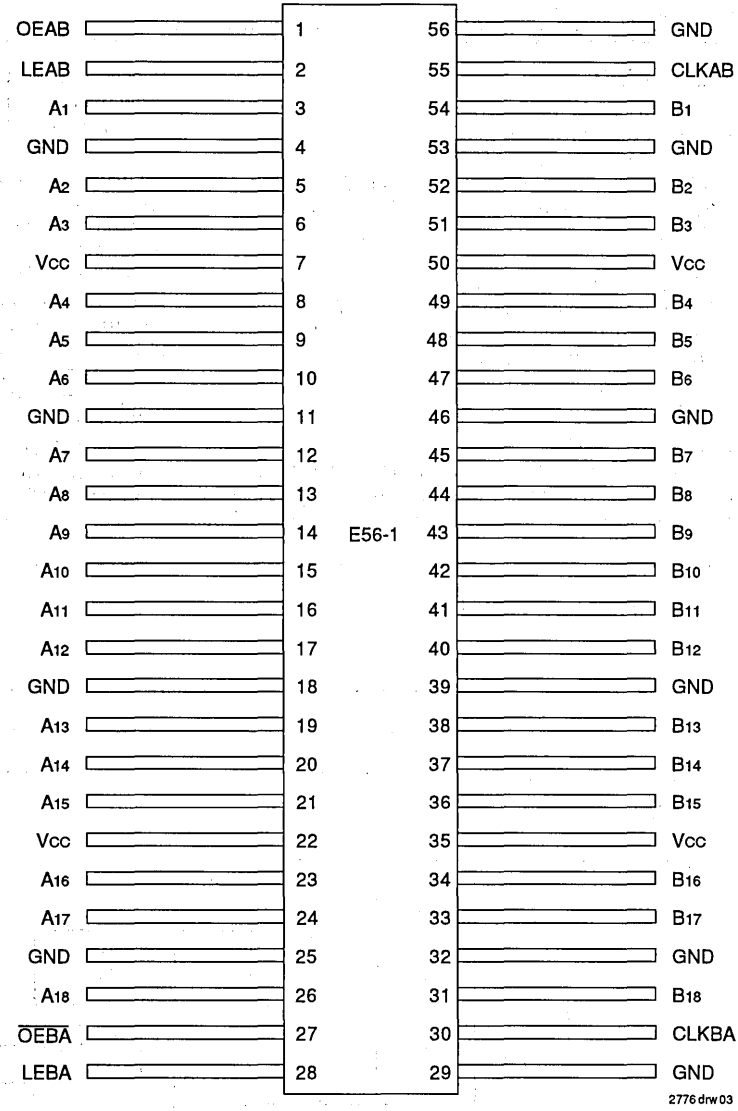
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



SSOP
TOP VIEW



CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs

2776 tbl 01

FUNCTION TABLE[1,4]

Inputs				Outputs
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B[2]
H	L	H	X	B[3]

2776 tbl 02

NOTES:
1. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
4. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

2776 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

2776 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: $T_A = -40°C$ to $+85°C$, $V_{CC} = 3.3V \pm 0.3V$; Military: $T_A = -55°C$ to $+125°C$, $V_{CC} = 3.3V \pm 0.3V$

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = 5.5V	—	—	±5	µA
	Input HIGH Current (I/O pins)		V_I = V_{CC}	—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)		V_I = GND	—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.5	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

2776 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} - 0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V[3]	—	2.0	30	µA
			V_{IN} = 2.4V[3]	—	70	500	
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open OEAB = $\overline{OEBA}$ = V_{CC} or GND 50% Duty Cycle One Input Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz (CLKAB) 50% Duty Cycle OEAB = $\overline{OEBA}$ = V_{CC}	V_{IN} = V_{CC} – 0.6V V_{IN} = GND	—	0.7	2.5	mA
		LEAB = GND f_i = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = 2.4V V_{IN} = GND	—	0.7	3.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz (CLKAB) 50% Duty Cycle OEAB = $\overline{OEBA}$ = V_{CC}	V_{IN} = V_{CC} – 0.6V V_{IN} = GND	—	3.1	6.8[5]	
		LEAB = GND f_i = 2.5MHz 50% Duty Cycle Eighteen Bits Toggling	V_{IN} = 2.4V V_{IN} = GND	—	3.7	11.3[5]	

2776 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter		Condition[1]	FCT163501 Com'l. Min.[2]	FCT163501 Com'l. Max.	FCT163501 Mil. Min.[2]	FCT163501 Mil. Max.	FCT163501A Com'l. Min.[2]	FCT163501A Com'l. Max.	FCT163501A Mil. Min.[2]	FCT163501A Mil. Max.	Unit
f_{MAX}	CLKAB or CLKBA frequency[3]		C_L = 50pF	—	100	—	100	—	150	—	150	MHz
t_{PLH} t_{PHL}	Propagation Delay Ax to Bx or Bx to Ax		R_L = 500Ω	1.5	6.5	1.5	7.5	1.5	5.1	1.5	5.6	ns
t_{PLH} t_{PHL}	Propagation Delay LEBA to Ax, LEAB to Bx			1.5	7.5	1.5	8.0	1.5	5.6	1.5	6.0	ns
t_{PLH} t_{PHL}	Propagation Delay CLKBA to Ax, CLKAB to Bx			1.5	8.0	1.5	9.0	1.5	5.6	1.5	6.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ to Ax, OEAB to Bx			1.5	8.0	1.5	9.0	1.5	6.0	1.5	6.4	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ to Ax, OEAB to Bx			1.5	7.5	1.5	8.0	1.5	5.6	1.5	6.0	ns
t_{SU}	Set-up Time HIGH or LOW Ax to CLKAB, Bx to CLKBA			4.0	—	4.0	—	3.0	—	3.0	—	ns
t_H	Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA			0	—	0	—	0	—	0	—	ns
t_{SU}	Set-up Time HIGH or LOW	Clock LOW		4.0	—	4.0	—	3.0	—	3.0	—	ns
	Ax to LEAB, Bx to LEBA	Clock HIGH		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_H	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA			1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	LEAB or LEBA Pulse Width HIGH[3]			3.0	—	3.0	—	3.0	—	3.0	—	ns
t_W	CLKAB or CLKBA Pulse Width HIGH or LOW[3]			3.0	—	3.0	—	3.0	—	3.0	—	ns
$t_{SK(o)}$	Output Skew[4]			—	0.5	—	0.5	—	0.5	—	0.5	ns

2776 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Integrated Device Technology, Inc.

3.3V CMOS 16-BIT BUS TRANSCEIVER/ REGISTERS

PRELIMINARY
IDT54/74FCT163646/A

FEATURES:

- 0.5 MICRON CEMOS™ Technology
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V
- CMOS power levels (0.16mW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

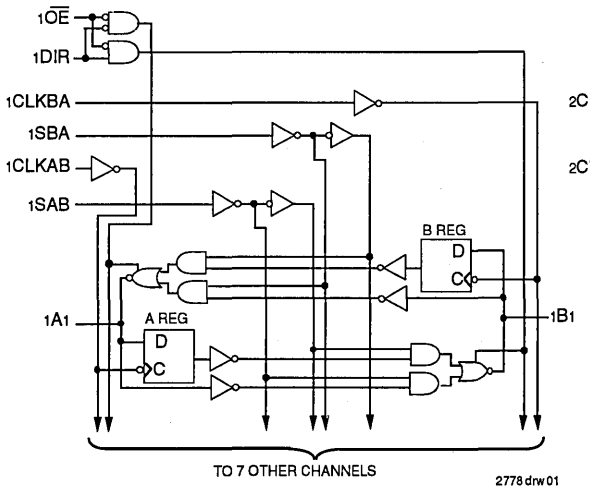
DESCRIPTION:

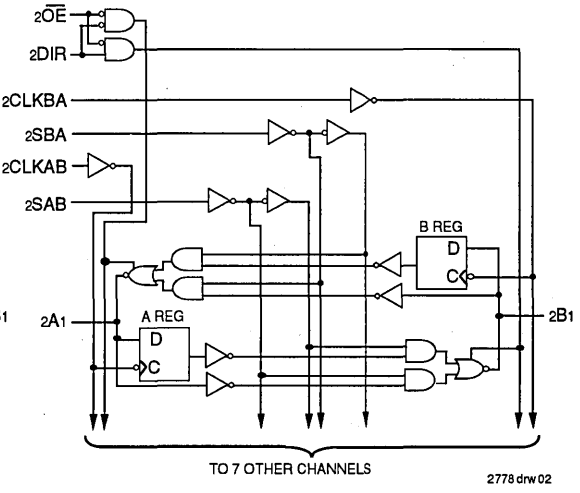
The IDT54/74FCT163646/A 16-bit registered transceivers are built using advanced CEMOS, dual metal CMOS technology.

These high-speed, low-power devices are organized as two independant 8-bit bus transceivers with 3-state D-type registers. The control circuitry is organized for multiplexed transmission of data between A bus and B bus either directly or from the internal storage registers. Each 8-bit transceiver/ register features direction control (xDIR), over-riding Output Enable control ($x\overline{OE}$) and Select lines (xSAB and xSBA) to select either real-time data or stored data. Separate clock inputs are provided for A and B port registers. Data on the A or B data bus, or both, can be stored in the internal registers by the LOW-to-HIGH transitions at the appropriate clock pins. Flow-through organization of signal pins facilitates ease of layout. All inputs are designed with hysteresis for improved noise margin.

The control inputs of IDT54/74FCT163646/A can be driven from either 3.3V or 5V devices. This feature allows added flexibility when used in a mixed 3.3V/5V supply environment.

FUNCTIONAL BLOCK DIAGRAM





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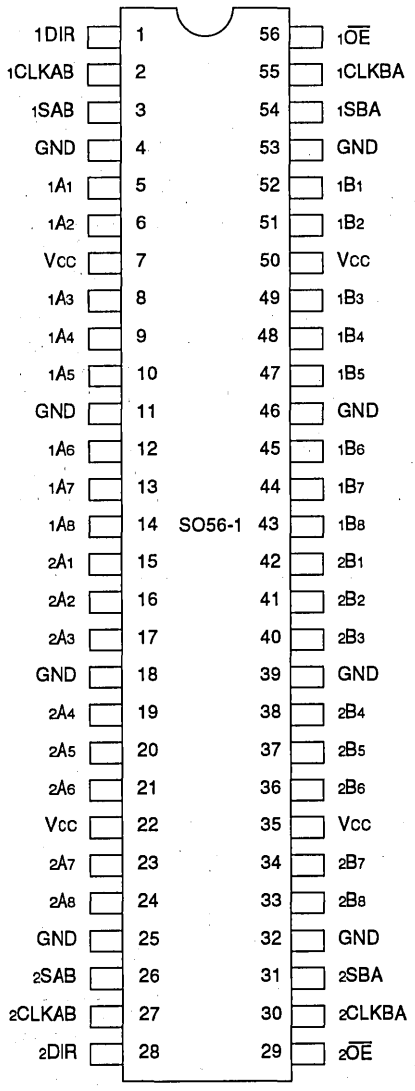
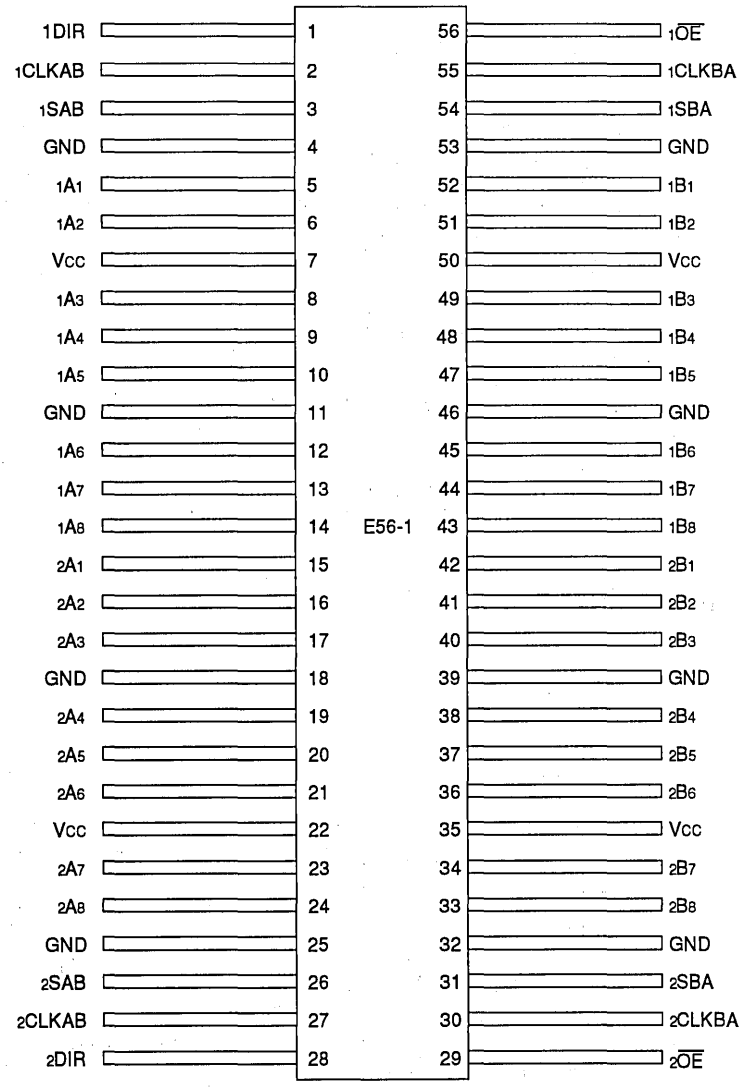
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2778 drw 03

SSOP
TOP VIEW



2778 drw 04

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xDIR, $x\overline{OE}$	Output Enable Inputs

2778 tbl 01

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2778 lnk 04
1. This parameter is measured at characterization but not tested.

FUNCTION TABLE(2)

Inputs						Data I/O(1)		Operation or Function
$x\overline{OE}$	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

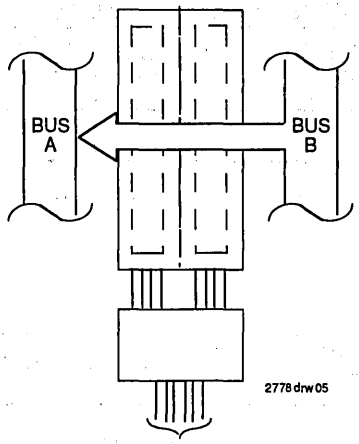
NOTE: 2778 tbl 02
1. The data output functions may be enabled or disabled by various signals at the $x\overline{OE}$ or xDIR inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ =LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(4)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

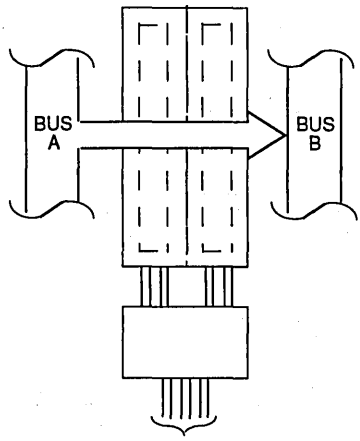
NOTES: 2778 lnk 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

7



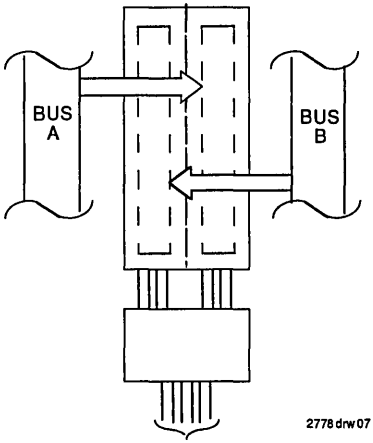
xDIR	$x\overline{OE}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO A



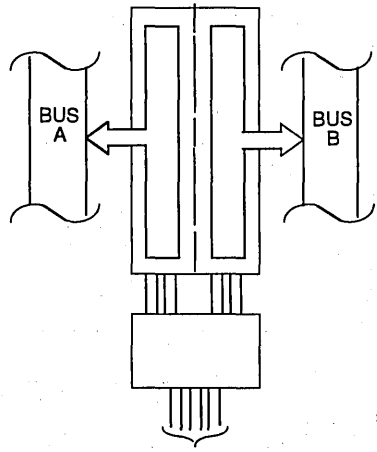
xDIR	$x\overline{OE}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	X	X	L	X

REAL-TIME TRANSFER BUS A TO B



xDIR	$x\overline{OE}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	↑	X	X	X
L	L	X	↑	X	X
X	H	↑	↑	X	X

STORAGE FROM A AND/OR B



xDIR (1)	$x\overline{OE}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

TRANSFER STORED DATA TO A AND/OR B

NOTE:
1. Cannot transfer data to A bus and B bus simultaneously.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 3.3V ± 0.3V; Military: T_A = –55°C to +125°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = 5.5V	—	—	±5	µA
	Input HIGH Current (I/O pins)		V_I = V_{CC}	—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)		V_I = GND	—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.5	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

2778 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} - 0.6V at rated current.

7

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V[3]	—	2.0	30	µA
			V_{IN} = 2.4V[3]	—	70	500	
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open xDIR = $x\overline{OE}$ = GND 50% Duty Cycle One Input Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle xDIR = $x\overline{OE}$ = GND	V_{IN} = V_{CC} – 0.6V V_{IN} = GND	—	0.7	2.5	mA
		f_i = 5MHz 50% Duty cycle One Bit Toggling	V_{IN} = 2.4V V_{IN} = GND	—	0.7	3.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle xDIR = $x\overline{OE}$ = GND	V_{IN} = V_{CC} – 0.6V V_{IN} = GND	—	3.1	6.8[5]	
		f_i = 2.5MHz 50% Duty Cycle Sixteen Bits Toggling	V_{IN} = 2.4V V_{IN} = GND	—	3.7	11[5]	

2778 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT163646				FCT163646A				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
t_{PZH} t_{PZL}	Output Enable Time xDIR or x$\overline{OE}$ to Bus		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time xDIR or x$\overline{OE}$ to Bus		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	ns
t_{PLH} t_{PHL}	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	ns
t_{SU}	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	ns
t_W	Clock Pulse Width HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2778 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

7

Integrated Device Technology, Inc.

3.3V CMOS OCTAL BUFFER/LINE DRIVER

PRELIMINARY
IDT54/74FCT3244/A

FEATURES:

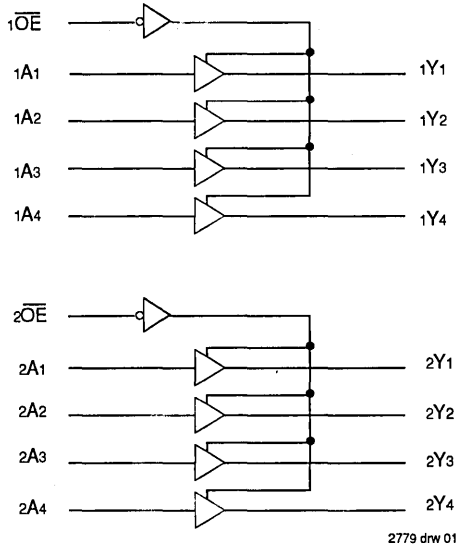
- 0.5 MICRON CEMOS™ Technology
- **Can serve as 5V to 3.3V translator**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V
- CMOS power levels (0.16mW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Inputs (except I/O) can be driven by 3.3V or 5V components

DESCRIPTION:

The IDT54/74FCT3244/A octal buffer/line drivers are built using advanced CEMOS, dual metal CMOS technology. These high-speed, low-power buffers are designed to be used as memory data and address drivers, clock drivers, and bus-oriented transmitter/receivers. The three-state controls are designed to operate these devices in a dual-nibble or single-byte mode. All inputs are designed with hysteresis for improved noise margin.

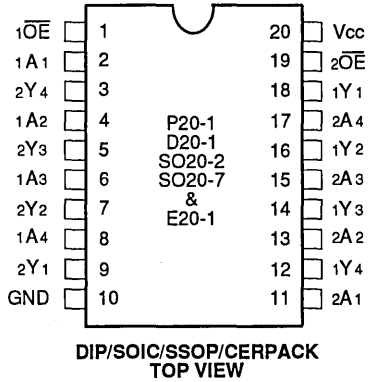
The data(xAx) and output enable ($x\overline{OE}$) inputs of these buffers can be driven from either 3.3V or 5V devices. This feature enables the IDT54/74FCT3244/A buffers to be used as 5V to 3.3V unidirectional translators in a 5V/3.3V mixed supply system.

FUNCTIONAL BLOCK DIAGRAM

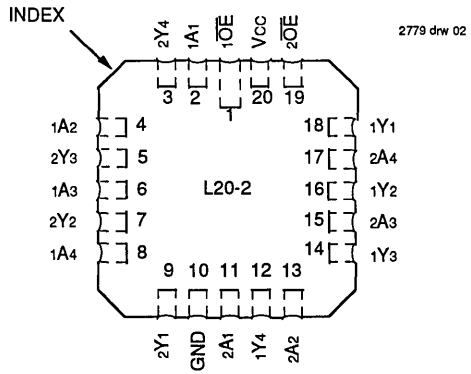


2779 drw 01

PIN CONFIGURATIONS



DIP/SOIC/SSOP/CERPACK TOP VIEW



2779 drw 02

LCC TOP VIEW

2779 drw 03

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}$	3–State Output Enable Inputs (Active LOW)
xAx	Data Inputs
xYx	3-State Outputs

2779 tbl 01

FUNCTION TABLE[1]

Inputs		Outputs
$x\overline{OE}$	xAx	xYx
L	L	L
L	H	H
H	X	Z

2779 tbl 02

NOTE:
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

2779 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

2779 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

7

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 3.3V ± 0.3V; Military: T_A = –55°C to +125°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	Vcc+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	Vcc = Max.	V_I = 5.5V	—	—	±5	µA
	Input HIGH Current (I/O pins)		V_I = Vcc	—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)		V_I = GND	—	—	±15	
I_{OZH}	High Impedance Output Current	Vcc = Max.	V_O = Vcc	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±10	
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	Vcc = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	Vcc = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	Vcc = Min.	I_{OH} = –0.1mA	Vcc–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	Vcc = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.5	
I_{OS}	Short Circuit Current[4]	Vcc = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	Vcc = Max., V_{IN} = GND or Vcc		—	0.05	1.5	mA

2779 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = Vcc -0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} − 0.6V[3]	—	2.0	30	µA
			V_{IN} = 2.4V[3]	—	70	500	
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open 50% Duty Cycle $x\overline{OE}$ = GND One Input Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	60	85	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz	V_{IN} = V_{CC} − 0.6V V_{IN} = GND	—	0.7	2.4	mA
		50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	V_{IN} = 2.4V V_{IN} = GND	—	0.7	2.6	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	V_{IN} = V_{CC} − 0.6V V_{IN} = GND	—	1.3	3.3[5]	
		50% Duty Cycle $x\overline{OE}$ = GND Eight Bits Toggling	V_{IN} = 2.4V V_{IN} = GND	—	1.5	5.2[5]	

2779 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

7

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT3244				FCT3244A				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	ns

2779 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

Integrated Device Technology, Inc.

3.3V CMOS OCTAL BIDIRECTIONAL TRANSCEIVERS

PRELIMINARY
IDT54/74FCT3245/A

FEATURES:

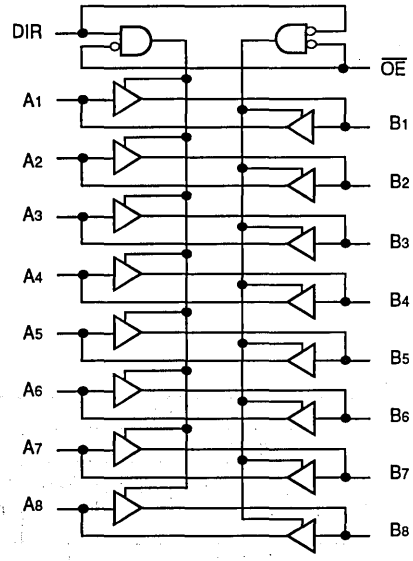
- 0.5 MICRON CEMOS™ Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V
- CMOS power levels (0.16mW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Inputs (except I/O) can be driven by 3.3V or 5V components

DESCRIPTION:

The IDT54/74FCT3245/A octal transceivers are built using advanced CEMOS, dual metal CMOS technology. These high-speed, low-power transceivers are ideal for synchronous communication between two busses (A and B). The direction control pin (DIR) controls the direction of data flow. The output enable pin ($\overline{OE}$) overrides the direction control and disables both ports. All inputs are designed with hysteresis for improved noise margin.

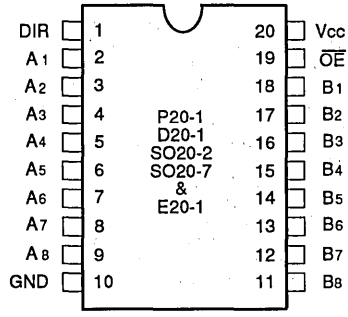
The DIR and $\overline{OE}$ control inputs of these transceivers can be driven from either 3.3V or 5V devices. This feature allows added flexibility when used in a mixed 3.3V/5V supply environment.

FUNCTIONAL BLOCK DIAGRAM

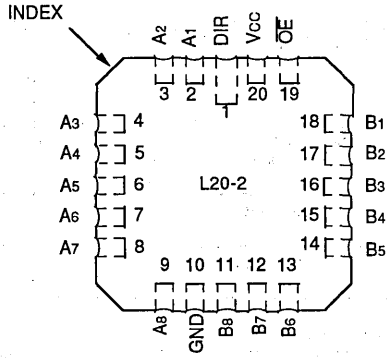


2650 drw 01

PIN CONFIGURATIONS



DIP/SOIC/SSOP/CERPACK
TOP VIEW



2650 drw 02

LCC
TOP VIEW

2650 drw 03

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
DIR	Direction Control Input
Ax	Side A Inputs or 3-State Outputs
Bx	Side B Inputs or 3-State Outputs

2650 tbl 01

FUNCTION TABLE[1]

Inputs		
$\overline{OE}$	DIR	Outputs
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

2650 tbl 02

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

2650 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

2650 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

7

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 3.3V ± 0.3V; Military: T_A = –55°C to +125°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = 5.5V	—	—	±5	µA
	Input HIGH Current (I/O pins)		V_I = V_{CC}	—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)		V_I = GND	—	—	±15	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±10	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±10	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.5	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.05	1.5	mA

2650 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} – 0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} − 0.6V[3]	—	2.0	30	µA
			V_{IN} = 2.4V[3]	—	70	500	
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = DIR = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	85	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi =10MHz	V_{IN} = V_{CC} − 0.6V V_{IN} = GND	—	0.7	2.4	mA
		50% Duty Cycle $\overline{OE}$ = DIR = GND One Bit Toggling	V_{IN} = 2.4V V_{IN} = GND	—	0.7	2.6	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	V_{IN} = V_{CC} − 0.6V V_{IN} = GND	—	1.3	3.3[5]	
		50% Duty Cycle $\overline{OE}$ = DIR = GND Eight Bits Toggling	V_{IN} = 2.4V V_{IN} = GND	—	1.5	5.2[5]	

NOTES: 2650 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT3245				FCT3245A				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	7.5	1.5	4.6	1.5	4.9	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A or B		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	ns
t_{PZH} t_{PZL}	Output Enable Time DIR to A or B[3]		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time DIR to A or B[3]		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	ns

NOTES: 2650 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

7

Integrated Device Technology, Inc.

FAST CMOS 16-BIT BIDIRECTIONAL 3.3V TO 5V TRANSLATOR

PRELIMINARY
IDT54/74FCT164245T

FEATURES:

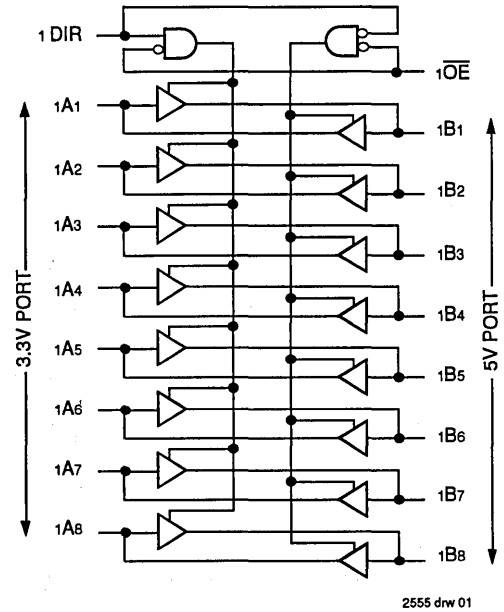
- 0.5 MICRON CEMOS™ Technology
- Bidirectional interface between 3.3V and 5V busses
- Control inputs can be driven from either 3.3V or 5V circuits
- ESD >2000V per MIL-STD-883, Method 3015; >200V using machine model (C = 200pF, R = 0)
- 25 MIL Center SSOP and Cerpack Packages
- Extended commercial range of -40°C to +85°C
- V_{CC1} = 5V ±10%, V_{CC2} = 3.3V ±0.3V
- High drive outputs (-32mA I_{OH}, 64mA I_{OL}) on 5V port
- Power-off disable on both poerts permits "live insertion"
- Typical V_{OLP} (Output Ground Bounce) < 0.9V at V_{CC1} = 5V, V_{CC2} = 3.3V, T_A = 25°C

DESCRIPTION:

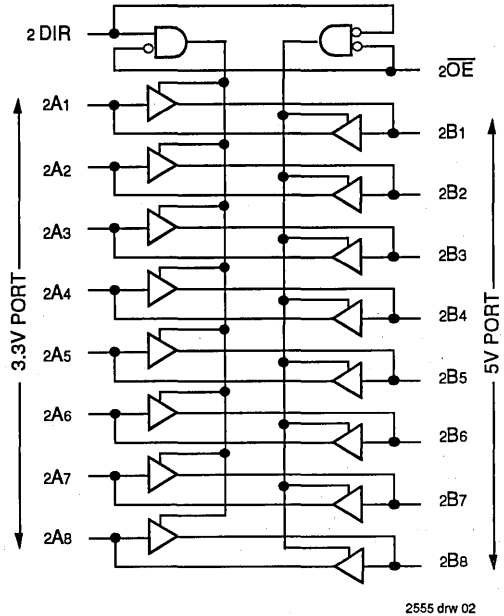
The IDT54/74FCT164245T 16-bit 3.3V-to-5V translator is built using advanced CEMOS, dual metal CMOS technology. This high-speed, low-power transceiver is designed to interface between a 3.3V bus and a 5V bus in a mixed 3.3V/5V supply environment. This enables system designers to interface TTL compatible 3.3V components with 5V components. The direction and output enable controls are designed to operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver. The A port interfaces with the 3.3V bus; the B port interfaces with the 5V bus. The direction control (xDIR) pin controls the direction of data flow. The output enable ($x\overline{OE}$) overrides the direction control and disables both ports. These control signals can be driven from either 3.3V or 5V devices.

The IDT54/74FCT164245T is ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with Power-Off Disable capability to allow "hot insertion" of boards when used as backplane drivers. They also allow interface between a mixed supply system and external 5V peripherals.

FUNCTIONAL BLOCK DIAGRAM



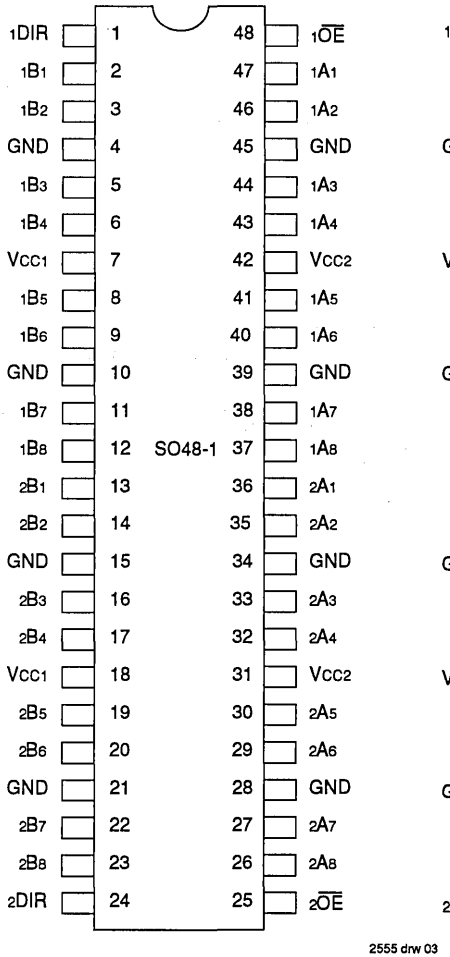
2555 drw 01



2555 drw 02

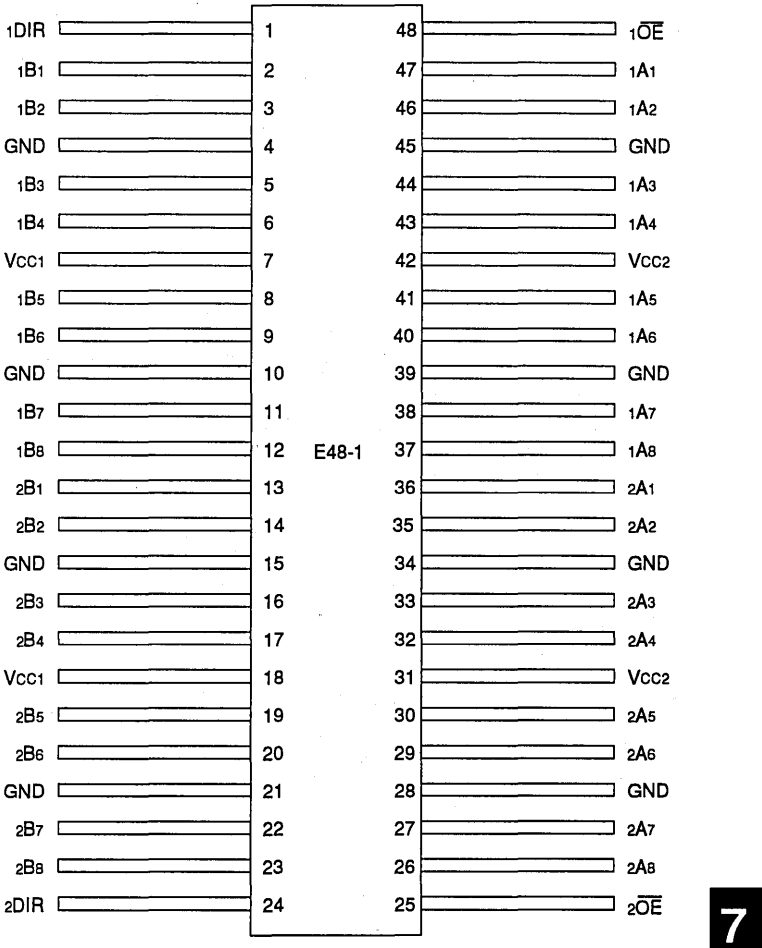
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2555 drw 03

SSOP
TOP VIEW



2555 drw 04

CERPACK
TOP VIEW

POWER SUPPLY SEQUENCING

The IDT54/74FCT164245T includes circuitry that will place both A and B ports in high impedance state if $V_{CC2} \geq V_{CC1} - 0.9$ volts. If V_{CC2} is applied first, there will be current flow from V_{CC2} to V_{CC1} that will raise V_{CC1} to $V_{CC2} - 0.6$ volts and both A and B ports will maintain high impedance state. In this condition, the user must insure that absolute maximum ratings are not violated.

PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}$	Output Enable Input (Active LOW)
xDIR	Direction Control Input
xAx	Side A Inputs or 3-State Outputs (3.3V Port)
xBx	Side B Inputs or 3-State Outputs (5V Port)

2555 tbl 01

FUNCTION TABLE(1)

Inputs		Outputs
$x\overline{OE}$	xDIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

2555 tbl 03

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2555 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

2555 tbl 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (A PORT - 3.3V)

Following Conditions Apply Unless Otherwise Specified:
V_{CC1} = 5V ± 10%, V_{CC2} = 3.3V ± 0.3V; Commercial: T_A = –40°C to +85°C, Military: T_A = –55°C to +125°C,

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input and I/O pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC1} = Max.	V_I = 5.5V	—	—	±5	µA
	Input HIGH Current (I/O pins)	V_{CC2} = Max.	V_I = V_{CC2}	—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)		V_I = GND	—	—	±15	
V_{IK}	Clamp Diode Voltage	V_{CC2} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC1} = Min.	I_{OH} = –0.1mA	V_{CC2}–0.2	—	—	V
		V_{CC2} = Min.	I_{OH} = –6mA MIL.	2.4[5]	3.0	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA COM'L.				
V_{OL}	Output LOW Voltage	V_{CC1} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{CC2} = Min.	I_{OL} = 16mA	—	0.2	0.4	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.5	
I_{OFF}	Input/Output Power Off Leakage	V_{CC1} = 0V, V_{CC2} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±100	µA
I_{OS}	Short Circuit Current[4]	V_{CC1} = Max., V_{CC2} = Max., V_O = GND[3]		—	–100	—	mA
I_O	Output Drive Current	V_{CC1} = Max., V_{CC2} = Max., V_O = 2.5V[3]		—	–60	—	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CC2L} I_{CC2H} I_{CC2Z}	Quiescent Power Supply Current	V_{CC1} = Max., V_{IN} = GND or V_{CC2} V_{CC2} = Max.		—	0.35	2.0	mA

2555 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC1} = 5.0V, V_{CC2} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC2} - 0.6V at rated current.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (B PORT - 5V)

Following Conditions Apply Unless Otherwise Specified:
V_{CC1} = 5V ± 10%, V_{CC2} = 3.3V ± 0.3V; Commercial: T_A = –40°C to +85°C, Military: T_A = –55°C to +125°C,

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input and I/O pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC1} = Max.	V_I = V_{CC1}	—	—	±5	µA
	Input HIGH Current (I/O pins)	V_{CC2} = Max.		—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)			—	—	±15	
V_{IK}	Clamp Diode Voltage	V_{CC1} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC1} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{CC2} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[5]	2.0	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC1} = Min., V_{CC2} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC1} = 0V, V_{CC2} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±100	µA
I_{OS}	Short Circuit Current[4]	V_{CC1} = Max., V_{CC2} = Max., V_O = GND[3]		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC1} = Max., V_{CC2} = Max., V_O = 2.5V[3]		–50	–75	–180	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CC1L} I_{CC1H} I_{CC1Z}	Quiescent Power Supply Current	V_{CC1} = Max., V_{IN} = GND or V_{CC2} V_{CC2} = Max.		—	0.08	1.5	mA

2555 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC1} = 5.0V, V_{CC2} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5 Duration of the condition can not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC1} = Max., V_{CC2} = Max., V_{IN} = V_{CC2} -0.6V[3]		—	12	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC1} = Max., V_{CC2} = Max. Outputs Open $x\overline{OE}$ = xDIR = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC2} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC1} = Max., V_{CC2} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $x\overline{OE}$ = xDIR = GND One Bit Toggling	V_{IN} = V_{CC2} - 0.6V V_{IN} = GND	—	1.2	4.7	mA
		V_{CC1} = Max., V_{CC2} = Max Outputs Open f_i = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = xDIR = GND Sixteen Bits Toggling	V_{IN} = V_{CC2} - 0.6V V_{IN} = GND	—	3.5	8.5[5]	

2555 tbl 07

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC1}= 5.0V, V_{CC2}= 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC1} + I_{CC2} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC1}= Quiescent Current (I_{CC1L}, I_{CC1H} and I_{CC1Z})
   I_{CC2}= Quiescent Current (I_{CC2L}, I_{CC2H} and I_{CC2Z})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	Com'l.		Mil.		Unit
			Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay A to B	C_L = 50pF R_L = 500Ω	1.5	5.0	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay B to A		1.5	5.0	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to B		1.5	6.5	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to B		1.5	6.0	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to A		1.5	6.5	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to A		1.5	6.0	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time xDIR to B[3]		1.5	6.5	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time xDIR to B[3]		1.5	6.0	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time xDIR to A[3]		1.5	6.5	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time xDIR to A[3]		1.5	6.0	—	—	ns

2555 tbl 08

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

Integrated Device Technology, Inc.

5V TO 3.3V UNIDIRECTIONAL TRANSLATORS

IDT54/74FCT3244
IDT54/74FCT163244
IDT54/74FCT163373
IDT54/74FCT163374

The following 8-bit and 16-bit, 3.3V bus interface parts serve as unidirectional translators[1]. For detailed specifications, please refer to the individual data sheets for these parts.

5V to 3.3V Unidirectional Translators

Part Number	Description
IDT54/74FCT3244	Octal 3.3V Buffer/Line Driver
IDT54/74FCT163244	16-Bit 3.3V Buffer/Line Driver
IDT54/74FCT163373	16-Bit 3.3V Transparent Latch
IDT54/74FCT163374	16-Bit 3.3V Register

5V to 3.3V Unidirectional Translators provide a one-way interface between 5V components and 3.3V components or between 5V components and 3.3V bus in a mixed 5V/3.3V supply system as shown in Figure 1.

The Unidirectional Translators accept TTL– or CMOS–compatible signals from 5V components at the inputs and provide TTL-compatible output levels. These translators avoid any problems associated with a direct interface between a 5V component and a 3.3V component or between a 5V component and a 3.3V bus.

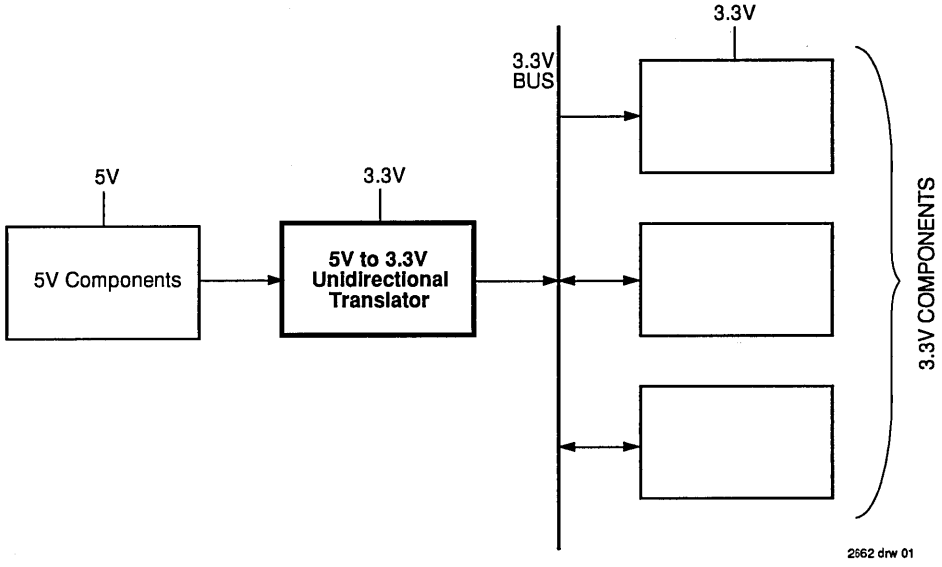

Figure 1. Mixed 5V/3.3V System

NOTE:
1. For 3.3V/5V Bidirectional Bus Translators, please refer to the IDT54/74FCT164245T data sheet.

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COMPLEX LOGIC PRODUCTS

High-performance building blocks of ever-increasing complexity are the basis for many of today's innovative design solutions. IDT's Complex Logic products address this need by combining state-of-the-art sub-micron CEMOS process with highly sophisticated design tools to produce VLSI building blocks that satisfy the most demanding system requirements. IDT's Complex Logic products are divided into three functional areas:

— Error Detection and Correction
— Read-Write buffers and Bus Multiplexers
— DSP and Microslice

Error Detection and Correction (EDC)

Today's high-performance systems are becoming increasingly DRAM intensive. IDT has developed a range of high-performance EDC devices that eliminate the performance penalties once associated with these circuits while assuring the designer continuous, error-free operation necessary in high-reliability systems. IDT's family of EDC products offers the designer a choice of 16-, 32-, or 64-bit devices with either single-bus or flow-through architectures. These devices are capable of detecting and correcting errors in as little as 20ns.

Read-Write Buffers and Bus Multiplexers

The current generation of RISC and CISC microprocessors depend on secondary cache memory for their best performance. IDT's newly released 73200 family of write buffers provides the designer with a flexible approach to meeting these requirements in his system.

The 73720, 16-bit triport bus multiplexer was designed for DRAM interleaving schemes. With separate byte controls, latches and high speeds, these bus multiplexers are the perfect solution for DRAM memory designs.

DSP and Microslice Processors

Digital signal processing applications have always demanded extremely high-performance building blocks. IDT continues to offer a selection of the world's fastest fixed-point DSP elements including multipliers, multiplier/accumulators, ALUs and microslice processors. These components enable the construction of customized, high-performance architectures and instruction sets.

TABLE OF CONTENTS

Integrated Device Technology, Inc.

12-BIT CMOS MICROPROGRAM SEQUENCER

IDT39C10B
IDT39C10C

FEATURES:

- Low-power CEMOS™
  - — Icc (max.)
    Military: 90mA
    Commercial: 75mA
- Fast
  - — IDT39C10B matches 2910A speeds
  - — IDT39C10C 30% speed upgrade
- 33-Deep stack
  - — Accommodates highly nested loops and subroutines
- 12-bit address width
- 12-bit internal loop counter
- 16 powerful microinstructions
- Three output enables control 3-way branch
- Available in 40-pin DIP and 44-pin LCC/PLCC
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-87708 is listed on this function.

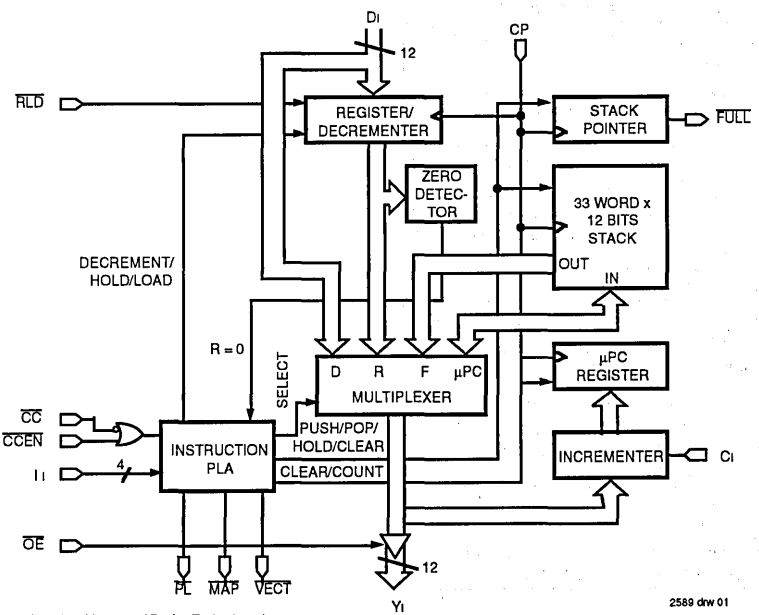
DESCRIPTION:

The IDT39C10 microprogram sequencers are designed for use in high-performance microprogram state machines. These microprogram sequencers are intended for use in controlling the sequence of microinstructions executed in the microprogram memory. The IDT39C10s provide several conditional branch instructions that allow branching to any microinstruction within the 4K microword address space. A 33-deep last-in/first-out stack provides for a very powerful microprogram subroutine return linkage and looping capability. With this depth of a microprogram return stack, the microprogrammer has maximum flexibility in nesting subroutines and loops. The counter contained in the IDT39C10s provides for microinstruction loop counts of up to 4096, in terms of total count length.

The IDT39C10s provide a 12-bit address to the microprogram memory. This microprogram sequencer selects one of four sources for the address. These are (1) the microprogram address register, (2) external direct input, (3) internal register counter and (4) the 33-deep LIFO stack. The microprogram counter usually contains an address that is one greater than the microinstruction currently being executed in the microprogram pipeline register.

The IDT39C10s are fabricated using CEMOS, a CMOS technology designed for high-performance and high-reliability. The devices are pin-compatible, performance-enhanced, functional replacements for the 2910A.

FUNCTIONAL BLOCK DIAGRAM



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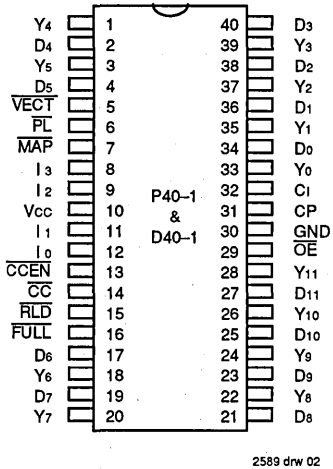
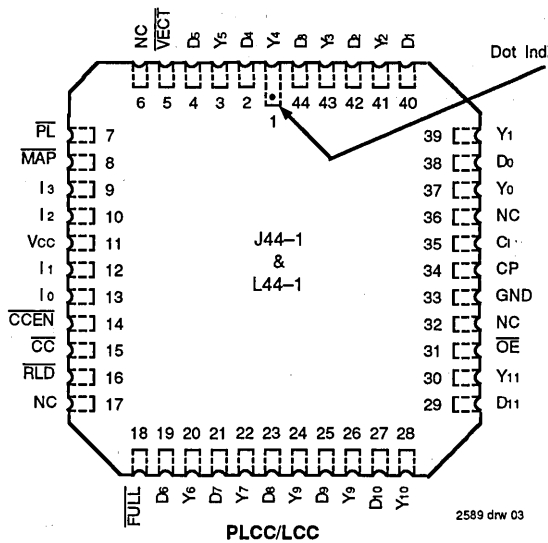
PIN CONFIGURATIONS



2589 drw 02

DIP
TOP VIEW



2589 drw 03

PLCC/LCC
TOP VIEW

PIN DESCRIPTIONS

Pin Name	I/O	Description
DI	I	Direct input to register/counter and multiplexer D0 is LSB.
II	I	Selects one-of-sixteen instructions.
$\overline{CC}$	I	Used as test criterion. A LOW on $\overline{CC}$ indicates "passed" test condition.
$\overline{CCEN}$	I	Whenever the signal is HIGH, $\overline{CC}$ is ignored and the device operates as though $\overline{CC}$ were true (LOW).
CI	I	Low order carry input to incrementer for microprogram counter.
$\overline{RLD}$	I	When LOW forces loading of register/ counter regardless of instruction or condition.
$\overline{OE}$	I	Three-state control of YI outputs.
CP	I	Triggers all internal state changes at LOW-to-HIGH edge.
YI	O	Address to microprogram memory. Y0 is LSB, Y11 is MSB.
$\overline{FULL}$	O	Indicates that 33 items are on the stack.
$\overline{PL}$	O	Can select #1 source (usually Pipeline Register) as direct input source.
$\overline{MAP}$	O	Can select #2 source (usually Mapping PROM or PLA) as direct input source.
$\overline{VECT}$	O	Can select #3 source (for example, Interrupt Starting Address) as direct input source.

2589 tbl 01

PRODUCT DESCRIPTION

The IDT39C10s are high-performance CMOS microprogram sequencers that are intended for use in very high-speed microprogrammable microprocessor applications. The sequencers allow for direct control of up to 4K words of microprogram.

The heart of the microprogram sequencers is a 4-input multiplexer that is used to select one of four address sources to select the next microprogram address. These address sources include the register/counter, the direct input, the microprogram counter or the stack as the source for the address of the next microinstruction.

The register/counter consists of twelve D-type flip-flops which can contain either an address or a count. These edge-triggered flip-flops are under the control of a common clock enable, as well as the four microinstruction control inputs. When the load control (RLD) is LOW, the data at the D inputs is loaded into this register on the LOW-to-HIGH transition of the clock. The output of the register/counter is available at the multiplexer as a possible next address source for the microcode. Also, the terminal count output associated with the register/counter is available at the internal instruction PLA to be used as condition code input for some of the microinstructions. The IDT39C10s contain a microprogram counter that usually contains the address of the next microinstruction compared to that currently being executed. The microprogram counter actually consists of a 12-bit incrementer followed by a 12-bit register. The microprogram counter will increment the address coming out of the sequencer going to the microprogram memory if the carry-in input to this counter is HIGH; otherwise, this address will be loaded into the microprogram counter. Normally, this carry-in input is set to the logic HIGH state so that the incrementer will be active. Should the carry-in input be set LOW, the same address is loaded into the microprogram counter. This is a technique that can be used to allow execution of the same microinstruction several times.

There are twelve D-inputs on the IDT39C10s that go directly to the address multiplexer. These inputs are used to provide a branch address that can come directly from the microcode or some other external source. The fourth input available to the multiplexer for next address control is the 33-deep, 12-bit wide LIFO stack. The LIFO stack provides return address linkage for subroutines and loops. The IDT39C10s contain a built-in stack pointer that always points to the last stack location written. This allows for stack reference operations, usually called loops, to be performed without popping the stack.

The stack pointer internal to the IDT39C10s is actually an up/down counter. During the execution of microinstructions one, four and five, the PUSH operation may occur depending on the state of the condition code input. This causes the stack pointer to be incremented by one and the stack to be written with the required return linkage (the value contained in the microprogram counter). On the microprogram cycle following the PUSH, this new return linkage data that was in the microprogram counter is now at the new location pointed to by the stack pointer. Thus, any time the multiplexer looks at the stack, it will see this data on the top of the stack.

During five different microinstructions, a pop operation associated with the stack may occur. If the pop occurs, the stack pointer is decremented at the next LOW-to-HIGH transition of the clock. A pop decrements the stack pointer which is the equivalent of removing the old information from the top of the stack.

The IDT39C10s are designed so that the stack pointer linkage allows any sequence of pushes, pops or stack references to be used. The depth of the stack can grow to a full 33 locations. After a depth of 33 is reached, the $\overline{\text{FULL}}$ output goes LOW. If further PUSHes are attempted when the stack is full, the stack information at the top of the stack will be destroyed but the stack pointer will not end around. It is necessary to initialize the stack pointer when power is first turned on. This is performed by executing a RESET instruction (Instruction 0). This sets the stack pointer to the stack empty position — the equivalent depth of zero. Similarly, a pop from an empty stack may place unknown data on the Y outputs, but the stack pointer is designed not to end around. Thus, the stack pointer will remain at the 0 or stack empty location if a pop is executed while the stack is already empty.

The IDT39C10s' internal 12-bit register/counter is used during microinstructions eight, nine and fifteen. During these instructions, the 12-bit counter acts as a down counter and the terminal count (count = 0) is used by the internal instruction PLA as an input to control the microinstruction branch test capability. The design of the internal counter is such that, if it is preloaded with a number N and then this counter is used in a microprogram loop, the actual sequence in the loop will be executed N + 1 times. Thus, it is possible to load the counter with a count of 0 and this will result in the microcode being executed one time. The 3-way branch microinstruction, Instruction 15, uses both the loop counter and the external condition code input to control the final source address from the Y outputs of the microprogram sequencer. This 3-way branch may result in the next address coming from the D inputs, the stack or the microprogram counter.

The IDT39C10s provide a 12-bit address at the Y outputs that are under control of the $\overline{\text{OE}}$ input. Thus, the outputs can be put in the three-state mode, allowing the writable control store to be loaded or certain types of external diagnostics to be executed.

In summary, the IDT39C10s are the most powerful microprogram sequencers currently available. They provide the deepest stack, the highest performance and the lowest power dissipation for today's microprogrammed machine design.

IDT39C10 OPERATION

The IDT39C10s are CMOS pin-compatible implementations of the Am2910 and 2910A microprogram sequencers. The IDT39C10's microprogram is functionally identical except that it provides a 33-deep stack to give the microprogrammer more capability in terms of microprogram subroutines and microprogram loops. The definition of each microprogram instruction is shown in the table of instructions. This table

shows the results of each instruction in terms of controlling the multiplexer, which determines the Y outputs, and in controlling the signals that can be used to enable various branch address sources ($\overline{PL}$, $\overline{MAP}$, $\overline{VECT}$). The operation of the register/counter and the 33-deep stack after the next LOW-to-HIGH transition of the clock. The internal multiplexer is used to select which of the internal sources is used to drive the Y outputs. The actual value loaded into the microprogram counter is either identical to the Y output or the Y output value is incremented by 1 and placed in the microprogram counter. This function is under the control of the carry inputs. For each of the microinstruction inputs, only one of the three outputs ($\overline{PL}$, $\overline{MAP}$, or $\overline{VECT}$) will be LOW. Note that this function is not determined by any of the possible condition code inputs. These outputs can be used to control the three-state selection of one of the sources for the microprogram branches.

Two inputs, $\overline{CC}$ and $\overline{CCEN}$, can be used to control the conditional instructions. These are fully defined in the table of instructions. The $\overline{RLD}$ input can be used to load the internal register/counter at any time. When this input is LOW, the data at the D inputs will be loaded into this register/counter on the LOW-to-HIGH transition of the clock. Thus, the $\overline{RLD}$ input overrides the internal hold or decrement operations specified by the various microinstructions. The $\overline{OE}$ input is normally LOW and is used as the three-state enable for the Y outputs. The internal stack in the IDT39C10s is a last-in/first-out memory that is 12-bits in width and 33 words deep. It has a stack pointer that addresses the stack and always points to the value currently on the top of the stack. When instruction 0 (RESET) is executed, the stack pointer is initialized to the top of the stack which is, by definition, the stack empty condition. Thus, the contents of the top of the stack are undefined until the forced PUSH occurs. A pop performed while the stack is empty will not change the stack pointer in any way; however, it will result in unknown data at the Y outputs.

By definition, the stack is full any time 33 more pushes than pops have occurred since the stack was last empty. When this happens, the Full Flag will go LOW. This signal first goes LOW on the microcycle after the 33 pushes occur. When this signal is LOW, no additional pushes should be attempted or the information on the top of the stack will be lost.

THE IDT39C10 INSTRUCTION SET

This data sheet contains a block diagram of the IDT39C10 microprogram sequencers. As can be seen, the devices are controlled by a 4-bit microinstruction word (I_3 - I_0). Normally, this word is supplied from one 4-bit field of the microinstruction word associated with the entire state machine system. These four bits provide for the selection of one of the sixteen powerful instructions associated with selecting the address of the next microinstruction. Unused Y outputs can be left open; however, the corresponding most significant D inputs should be tied to ground for smaller microwords. This is necessary to make sure the internal operation of the counter is proper should less than 4K of microcode be implemented. As shown in the block diagram, the internal instruction PLA uses the four instruction inputs as well as the $\overline{CC}$, $\overline{CCEN}$ and the internal counter = 0 line for controlling the sequencer. This internal instruction PLA provides all of the necessary internal control signals to control each particular part of the microprogram sequencer. The next address at the Y outputs of the IDT39C10s can be from one of four sources. These include the internal microprogram counter, the last-in/first-out stack, the register/counter and the direct inputs.

The following paragraphs will describe each instruction associated with the IDT39C10s. As a part of the discussion, an example of each instruction is shown in Figure 1. The purpose of the examples is to show microprogram flow. Thus, in each example the microinstruction currently being executed has a circle around it. That is, this microinstruction is assumed to be the contents of the pipeline register at the output of the microprogram memory. In these drawings, each of the dots refers to the time that the contents of the microprogram memory word would be in the pipeline register and is currently being executed.

INSTRUCTION 0 – JUMP 0 (JZ)

This instruction is used at power up time or at any restart sequence when the need is to reset the stack pointer and jump to the very first address in microprogram memory. The Jump 0 instruction does not change the contents of the register/counter.

INSTRUCTION 1 – CONDITIONAL JUMP TO SUBROUTINE (CJS)

The Conditional Jump to Subroutine Instruction is the one used to call microprogram subroutines. The subroutine address will be contained in the pipeline register and presented at the D inputs. If the condition code test is passed, a branch is taken to the subroutine. Referring to the flow diagram for the IDT39C10s shown in Figure 1, we see that the content of the microprogram counter is 68. This value is pushed onto the stack and the top of stack pointer is incremented. If the test is failed, this Conditional Jump to Subroutine instruction behaves as a simple continue. That is, the content of microinstruction address 68 is executed next.

INSTRUCTION 2 – JUMP MAP (JMAP)

This sequencer instruction can be used to start different microprogram routines based on the machine instruction opcode. This is typically accomplished by using a mapping PROM as an input to the D inputs on the microprogram sequencer. The JMAP instruction branches to the address appearing on the D inputs. In the flow diagram shown in Figure 1, we see that the branch actually will be the contents of microinstruction 85 and this instruction will be executed next.

INSTRUCTION 3 – CONDITIONAL JUMP PIPELINE (CJP)

The simplest branching control available in the IDT39C10 microprogram sequencers is that of conditional jump to address. In this instruction, the jump address is usually contained in the microinstruction pipeline register and presented to the D inputs. If the test is passed, the jump is

taken. If the test fails, this instruction executes as a simple continue. In the example shown in the flow diagram of Figure 1, we see that if the test is passed, the next microinstruction to be executed is the content of address 25. If the test is failed, the microcode simply continues to the contents of the next instruction.

INSTRUCTION 4 –
PUSH/CONDITIONAL LOAD COUNTER (PUSH)

With this instruction, the counter can be conditionally loaded during the same instruction that pushes the current value of the microprogram counter on to the stack. Under any condition independent of the conditional testing, the microprogram counter is pushed on to the stack. If the conditional test is passed, the counter will be loaded with the value on the D inputs to the sequencer. If the test fails, the contents of the counter will not change. The PUSH/Conditional Load Counter instruction is used in conjunction with the loop instruction (Instruction 13), the repeat file based on the counter instruction (Instruction 9) or the 3-way branch instruction (Instruction 15).

INSTRUCTION 5 –
CONDITIONAL JUMP TO SUBROUTINE R/PL (JSRP)

Subroutines may be called by a Conditional Jump Subroutine from the internal register or from the external pipeline register. In this instruction, the contents of the microprogram counter are pushed on the stack and the branch address for the subroutine call will taken from either the internal register/counter or the external pipeline register presented to the D inputs. If the conditional test is passed, the subroutine address will be taken from the pipeline register. If the conditional test fails, the branch address is taken from the internal register/counter. An example of this is shown in the flow diagram of Figure 1.

INSTRUCTION 6 –
CONDITIONAL JUMP VECTOR (CJV)

The Conditional Jump Vector instruction is similar to the Jump Map instruction in that it allows a branch operation to a microinstruction as defined from some external source, except that it is conditional. The Jump Map instruction is unconditional. If the conditional test is passed, the branch is taken to the new address on the D inputs. If the conditional test is failed, no branch is taken but rather the microcode simply continues to the next sequential microinstruction. When this instruction is executed, the $\overline{VECT}$ output is LOW unconditionally. Thus, an external 12-bit field can be enabled on to the D inputs of the microprogram sequencer.

INSTRUCTION 7 –
CONDITIONAL JUMP R/PL (JRP)

The Conditional Jump register/counter or external pipeline register always causes a branch in microcode. This jump will be to one of two different locations in the microcode address space. If the test is passed, the jump will be to the address presented on the D inputs to the microprogram sequencer. If the conditional test fails, the branch will be to the address contained in the internal register/counter.

INSTRUCTION 8 –
REPEAT LOOP COUNTER NOT EQUAL TO 0 (RFCT)

This instruction utilizes the loop counter and the stack to implement microprogrammed loops. The start address for the loop would be initialized by using the PUSH/Conditional Load Counter instruction. Then, when the repeat loop instruction is executed, if the counter is not equal to 0, the next microword address will be taken from the stack. This will cause a loop to be executed as shown in the Figure 1 flow diagram. Each time the microcode sequence goes around the loop, the counter is decremented. When the counter reaches 0, the stack will be popped and the microinstruction address will be taken from the microprogram counter. This instruction performs a timed wait or allows a single sequence to be executed the desired number of times. Remember, the actual number of loops performed is equal to the value in the counter plus 1.

INSTRUCTION 9 –
REPEAT PIPELINE COUNTER NOT EQUAL TO 0 (RPCT)

This instruction is another technique for implementing a loop using the counter. Here, the branch address for the loop is contained in the pipeline register. This instruction does not use the stack in any way as a part of its implementation. As long as the counter is not equal to 0, the next microword address will be taken from the D inputs of the microprogram sequencer. When the counter reaches 0, the internal multiplexer will select the address source from the microprogram counter, thus causing the microcode to continue on and leave the loop.

INSTRUCTION 10 –
CONDITIONAL RETURN (CRTN)

The Conditional Return instruction is used for terminating subroutines. The fact that it is conditional allows the subroutine either to be ended or to continue. If the conditional test is passed, the address of the next microinstruction will be taken from the stack and it will be popped. If the conditional test fails, the next microinstruction address will come from the internal microprogram counter. This is depicted in the flow diagram of Figure 1. It is important to remember that every subroutine call must somewhere be followed by a return from subroutine call in order to have an equal number of pushes and pops on the stack.

INSTRUCTION 11 –
CONDITIONAL JUMP PIPELINE AND POP (CJPP)

The Conditional Jump Pipeline and Pop instruction is a technique for exiting a loop from within the middle of the loop. This is depicted fully in the flow diagram for the IDT39C10s as shown in Figure 1. The conditional test input for this instruction results in a branch being taken if the test is passed. The address selected will be that on the D inputs to the microprogram sequencer and, since the loop is being terminated, the stack will be popped. Should the test be failed on the conditional test inputs, the microprogram will simply continue to the next address as taken from the microprogram counter. The stack will not be affected if the conditional test input is failed.

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INSTRUCTION 12 – LOAD COUNTER AND CONTINUE (LDCT)

The Load Counter and Continue instruction is used to place a value on the D inputs in the register/counter and continue to the next microinstruction.

INSTRUCTION 13 – TEST END OF LOOP (LOOP)

The Test End of Loop instruction is used as a last instruction in a loop associated with the stack. During this instruction, if the conditional test input is failed, the loop branch address will be that on the stack. Since we may go around the loop a number of times, the stack is not popped. If the conditional test input is passed, then the loop is terminated and the stack is popped. Notice that the loop instruction requires a PUSH to be performed at the instruction immediately prior to the loop return address. This is necessary so as to have the correct address on the stack before the loop operation. It is for this reason that the stack pointer always points to the last thing written on the stack.

INSTRUCTION 14 – CONTINUE (CONT)

Continue is a simple instruction where the address for the microinstruction is taken from the microprogram counter. This instruction simply causes sequential program flow to the next microinstruction in microcode memory.

INSTRUCTION 15 – THREE WAY BRANCH (TWB)

The Three-Way Branch instruction is used for looping while waiting for a conditional event to come true. If the event does not come true after some number of microinstructions, then a branch is taken to another microprogram sequence. This is depicted in Figure 1 showing the IDT39C10's flow diagram and is also described in full detail in the IDT39C10's instruction operational summary. Operation of the instruction is such that any time the external conditional test input is passed, the next microinstruction will be that associated with the program counter and the loop will be left. The stack is also popped. Thus, the external test input overrides the other possibilities. Should the external conditional test input not be true, the rest of the operation is controlled by the internal counter. If the counter is not equal to 0, the loop is taken by selecting the address on the top of the stack as the address out of the Y outputs of the IDT39C10s. In addition, the counter is decremented. Should the external conditional test input be failed and the counter also have counted to 0, this instruction "times out". The result is that the stack is popped and a branch is taken to the address presented to the D inputs of the IDT39C10 microprogram sequencers. This address is usually provided by the external pipeline register.

CONDITIONAL TEST

Throughout this discussion we have talked about microcode passing the conditional test. There are actually two inputs associated with the conditional test input. These include the $\overline{CCEN}$ and the $\overline{CC}$ inputs. The $\overline{CCEN}$ input is a condition code enable. Whenever the $\overline{CCEN}$ input is HIGH, the $\overline{CC}$ input is ignored and the device operates as though the $\overline{CC}$ input were true (LOW). Thus, a fail of the external test condition can defined as $\overline{CCEN}$ equals LOW and $\overline{CC}$ equals HIGH. A pass condition is defined as a $\overline{CCEN}$ equal to HIGH or a $\overline{CC}$ equal to LOW. It is important to recognize the full function of the condition code enable and the condition code inputs in order to understand when the test is passed or failed.

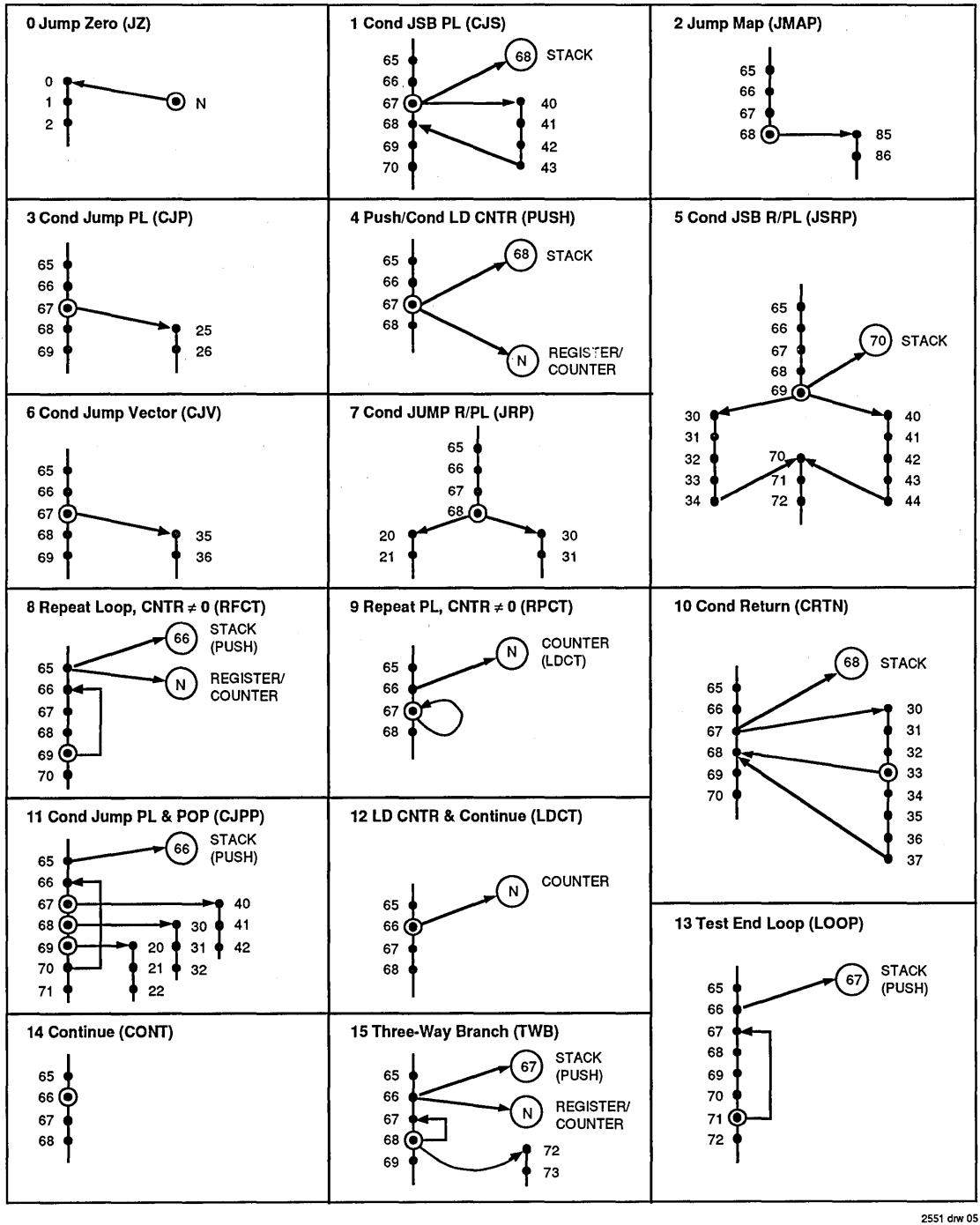
IDT39C10 INSTRUCTION OPERATIONAL SUMMARY

$I_3 - I_0$	Mnemonic	CC	Counter Test	Stack	Address Source	Register/ Counter	Enable Select
0	JZ	X	X	CLEAR	0	NC	$\overline{PL}$
1	CJS	PASS FAIL	X X	PUSH NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
2	JMAP	X	X	NC	D	NC	$\overline{MAP}$
3	CJP	PASS FAIL	X X	NC NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
4	PUSH	PASS FAIL	X X	PUSH PUSH	PC PC	LOAD NC	$\overline{PL}$ $\overline{PL}$
5	JSRP	PASS FAIL	X X	PUSH PUSH	D R	NC NC	$\overline{PL}$ $\overline{PL}$
6	CJV	PASS FAIL	X X	NC NC	D PC	NC NC	$\overline{VECT}$ $\overline{VECT}$
7	JRP	PASS FAIL	X X	NC NC	D R	NC NC	$\overline{PL}$ $\overline{PL}$
8	RFCT	X X	= 0 NOT = 0	POP NC	PC STACK	NC DEC	$\overline{PL}$ $\overline{PL}$
9	RPCT	X X	= 0 NOT = 0	NC NC	PC D	NC DEC	$\overline{PL}$ $\overline{PL}$
10	CRTN	PASS FAIL	X X	POP NC	STACK PC	NC NC	$\overline{PL}$ $\overline{PL}$
11	CJPP	PASS FAIL	X X	POP NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
12	LDCT	X	X	NC	PC	LOAD	$\overline{PL}$
13	LOOP	PASS FAIL	X X	POP NC	PC STACK	NC NC	$\overline{PL}$ $\overline{PL}$
14	CONT	X	X	NC	PC	NC	$\overline{PL}$
15	TWB	PASS PASS FAIL FAIL	= 0 NOT = 0 = 0 NOT = 0	POP POP POP NC	PC PC D STACK	NC DEC NC DEC	$\overline{PL}$ $\overline{PL}$ $\overline{PL}$ $\overline{PL}$

NC = No Change; DEC = Decrement

2589 tbl 02

8



2551 drw 05

Figure 1. IDT39C10B Flow Diagrams

IDT39C10 INSTRUCTIONS

$I_3 - I_0$	Mnemonic	Name	Reg/ Cntr Con- tents	FAIL $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH		PASS $\overline{CCEN}$ = HIGH and $\overline{CC}$ = LOW		Reg/ Cntr	Enable
				Y	Stack	Y	Stack		
0	JZ	Jump Zero	X	0	CLEAR	0	CLEAR	HOLD	$\overline{PL}$
1	CJS	Cond JSP PL	X	PC	HOLD	D	PUSH	HOLD	$\overline{PL}$
2	JMAP	Jump Map	X	D	HOLD	D	HOLD	HOLD	$\overline{MAP}$
3	CJP	Cond Jump PL	X	PC	HOLD	D	HOLD	HOLD	$\overline{PL}$
4	PUSH	PUSH/Cond Ld Cntr	X	PC	PUSH	PC	PUSH	(1)	$\overline{PL}$
5	JSRP	Cond JSB R/PL	X	R	PUSH	D	PUSH	HOLD	$\overline{PL}$
6	CJV	Cond Jump Vector	X	PC	HOLD	D	HOLD	HOLD	$\overline{VECT}$
7	JRP	Cond Jump R/PL	X	R	HOLD	D	HOLD	DEC	$\overline{PL}$
8	RFCT	Repeat Loop, CNTR ≠ 0	≠ 0	F	HOLD	F	HOLD	DEC	$\overline{PL}$
			= 0	PC	POP	PC	POP	HOLD	$\overline{PL}$
9	RPCT	Repeat PL, CNTR ≠ 0	≠ 0	D	HOLD	D	HOLD	DEC	$\overline{PL}$
			= 0	PC	HOLD	PC	HOLD	HOLD	$\overline{PL}$
10	CRTN	Cond RTN	X	PC	HOLD	F	POP	HOLD	$\overline{PL}$
11	CJPP	Cond Jump PL & POP	X	PC	HOLD	D	POP	HOLD	$\overline{PL}$
12	LDCT	LD Contr & Continue	X	PC	HOLD	PC	HOLD	LOAD	$\overline{PL}$
13	LOOP	Test End Loop	X	F	HOLD	PC	POP	HOLD	$\overline{PL}$
14	CONT	Continue	X	PC	HOLD	PC	HOLD	HOLD	$\overline{PL}$
15	TWB	Three-Way Branch	≠ 0	F	HOLD	PC	POP	DEC	$\overline{PL}$
			= 0	D	POP	PC	POP	HOLD	$\overline{PL}$

NOTE: 2589 tbl 03
1. If $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH, hold; else load. X = Don't Care.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{CC}	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	30	30	mA

NOTE: 2589 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter (1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2589 tbl 05
1. This parameter is sampled and not 100% tested.

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DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level[4]		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level[4]		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–0.1	–5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –12mA Mil.	2.4	4.3	–	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15mA Com'l.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 20mA Mil.	–	0.3	0.5	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA Com'l.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	–0.1	–10	µA
			V_O = V_{CC} (max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V [3]		–30	–	–	mA
I_{CCQH}	Quiescent Power Supply Current CP = H	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_{CP} = 0, CP = H		–	35	50	mA
I_{CCQL}	Quiescent Power Supply Current CP = L	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_{CP} = 0, CP = L		–	35	50	mA
I_{CCT}	Quiescent Input Power Supply[5] Current (per Input @ TTL High)	V_{CC} = Max., V_{IH} = 3.4V, f_{CP} = 0		–	0.3	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max.	MIL.	–	1.0	3.0	mA/
		$V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	COM'L.	–	1.0	1.5	MHz
I_{CC}	Total Power Supply Current[6]	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50 % Duty cycle $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$	MIL.	–	45	80	mA
			COM'L.	–	45	65	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50 % Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	–	50	90	
			COM'L.	–	50	75	

2589 tbl 06

NOTES:

1. For conditions shown as Max. or Min. use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, + 25°C ambient and maximum loading, not production tested.
3. Not more than one output should be shorted at one time. Duration of the circuit test should not exceed one second.
4. These input levels should only be static tested in a noise-free environment.
5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$I_{CC} = I_{CCQH}(C_{DH}) + I_{CCQL}(1 - C_{DH}) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP}/2 + f_0 N_0)$

C_{DH} = Clock duty cycle high period
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
N_T = Number of dynamic inputs driven at TTL levels
f_{CP} = Clock input frequency
f_0 = Ouput frequency
N_0 = Number of Outputs switching at f_0

CMOS TESTING CONSIDERATIONS

There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large Vcc current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscillate causing improper device operation and possible latchup.
3) Definition of input levels is very important. Since many inputs may change coincidentally, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

IDT39C10C AC ELECTRICAL CHARACTERISTICS

I. MINIMUM SET-UP AND HOLD TIMES

Inputs	t(S)		t(H)		Unit
	Com'l.	Mil.	Com'l.	Mil.	
DI → R	6	7	0	0	ns
DI → PC	13	15	0	0	ns
I0–3	23	25	0	0	ns
$\overline{CC}$	15	18	0	0	ns
$\overline{CCEN}$	15	18	0	0	ns
CI	6	7	0	0	ns
$\overline{RLD}$	11	12	0	0	ns

2589 tbl 07

II. MAXIMUM COMBINATIONAL DELAYS

Inputs	Y		$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$		$\overline{FULL}$		Unit
	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
D0–11	12	15	–	–	–	–	ns
I0–3	20	25	13	15	–	–	ns
$\overline{CC}$	16	20	–	–	–	–	ns
$\overline{CCEN}$	16	20	–	–	–	–	ns
CP	28	33	–	–	22	25	ns
$\overline{OE}$ (1)	10/10	13/13	–	–	–	–	ns

NOTE: 2589 tbl 08

1. Enable/Disable. Disable times measure to 0.5V change on output voltage level with C_L = 5pF. Tested at C_L = 50pF, correlated to 5pF.

III. CLOCK REQUIREMENTS

	Com'l.	Mil.	Unit
Minimum Clock LOW Time	18	20	ns
Minimum Clock HIGH Time	17	20	ns
Minimum Clock Period	35	40	ns

2589 tbl 09

IDT39C10B AC ELECTRICAL CHARACTERISTICS

I. MINIMUM SET-UP AND HOLD TIMES

Inputs	t(S)		t(H)		Unit
	Com'l.	Mil.	Com'l.	Mil.	
DI → R	16	16	0	0	ns
DI → PC	30	30	0	0	ns
I0–3	35	38	0	0	ns
$\overline{CC}$	24	35	0	0	ns
$\overline{CCEN}$	24	35	0	0	ns
CI	18	18	0	0	ns
$\overline{RLD}$	19	20	0	0	ns

2589 tbl 102589 tbl 07

II. MAXIMUM COMBINATIONAL DELAYS

Inputs	Y		$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$		$\overline{FULL}$		Unit
	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
D0–11	20	25	–	–	–	–	ns
I0–3	35	40	30	35	–	–	ns
$\overline{CC}$	30	36	–	–	–	–	ns
$\overline{CCEN}$	30	36	–	–	–	–	ns
CP	40	46	–	–	31	35	ns
$\overline{OE}$ (1)	25/27	25/30	–	–	–	–	ns

NOTE: 2589 tbl 11

1. Enable/Disable. Disable times measure to 0.5V change on output voltage level with C_L = 5pF. Tested at C_L = 50pF, correlated to 5pF.

III. CLOCK REQUIREMENTS

	Com'l.	Mil.	Unit
Minimum Clock LOW Time	20	25	ns
Minimum Clock HIGH Time	20	25	ns
Minimum Clock Period	50	51	ns

2589 tbl 12

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IDT39C10B INPUT/OUTPUT INTERFACE CIRCUIT

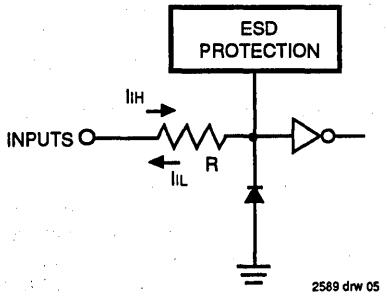


Figure 2. Input Structure

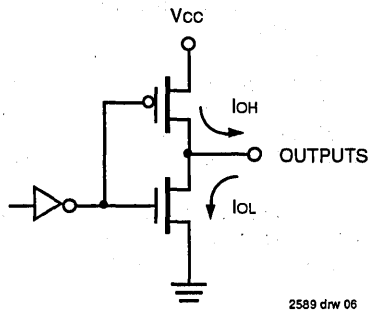


Figure 3. Output Structure

TEST LOAD CIRCUIT

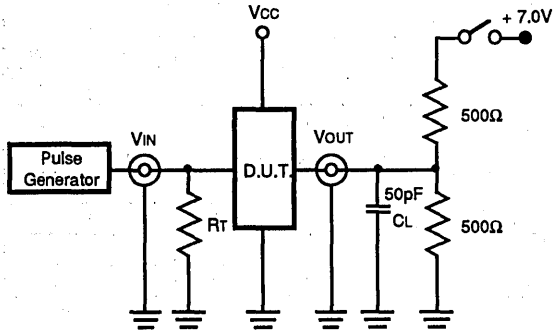


Figure 4. Switching Test Circuits

Test	Switch
Disable Low Enable Low	Closed
All other Tests	Open

2589 tbl 14

DEFINITIONS

C_L = Load capacitance: includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 4

2589 tbl 13

Integrated Device Technology, Inc.

16-BIT CMOS MICROPROCESSOR SLICE

IDT49C402
IDT49C402A
IDT49C402B

FEATURES:

- Functionally equivalent to four 2901s and one 2902
- IDT49C402B is 60% faster than four 2901Cs and one 2902A
- Expanded two-address architecture with independent, simultaneous access to two 64 x 16 register files
- Expanded destination functions with 8 new operations allowing Direct Data to be loaded directly into the dual-port RAM and Q Register
- Clamp diodes on all inputs provide noise suppression
- Fully cascadable
- 68-pin ceramic PGA, Plastic Leaded Chip Carrier (PLCC), and Ceramic Flatpack (25 mil centers)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

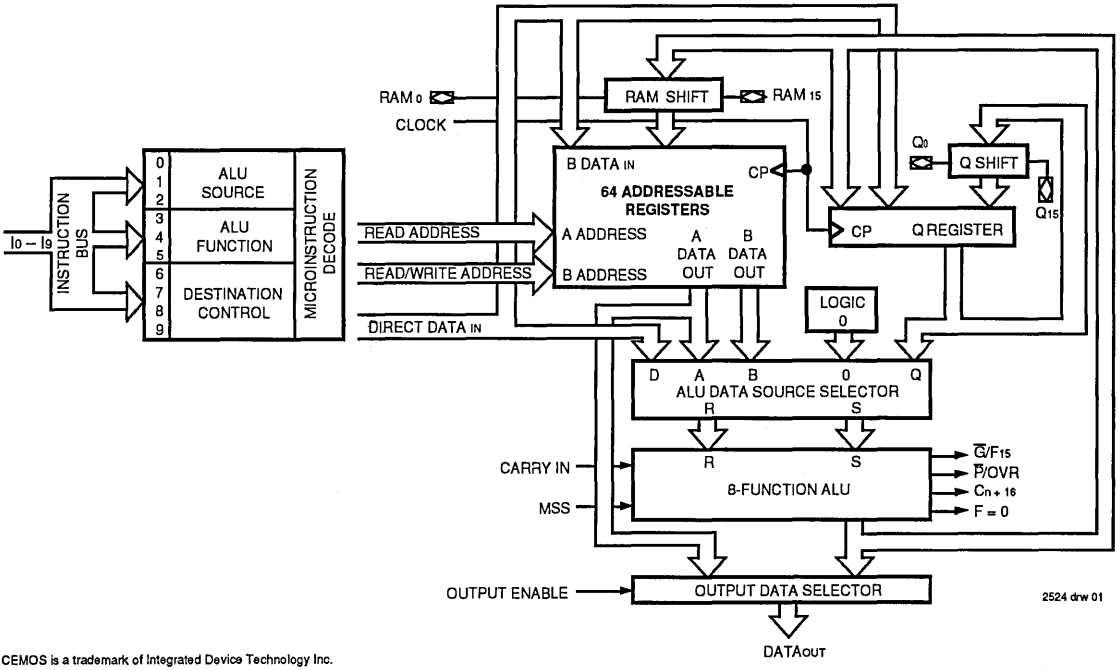
The IDT49C402s are high-speed, fully cascadable 16-bit CMOS microprocessor slice units which combine the standard functions of four 2901s and a 2902 with additional control features aimed at enhancing the performance of bit-slice microprocessor designs.

The IDT49C402s include all of the normal functions associated with standard 2901 bit-slice operation: a) a 3-bit instruction field (I_0, I_1, I_2) which controls the source operand selection for the ALU; b) a 3-bit microinstruction field (I_3, I_4, I_5) used to control the eight possible functions of the ALU; c) eight destination control functions which are selected by the microcode inputs (I_6, I_7, I_8); and d) a tenth microinstruction input, I_9, offering eight additional destination control functions. This I_9 input, in conjunction with I_6, I_7 and I_8, allows for shifting the Q Register up and down, loading the RAM or Q Register directly from the D inputs without going through the ALU, and having the RAM A data output port available at the Y output pins of the device.

Also featured is an on-chip dual-port RAM that contains 64-words-by-16 bits—four times the number of working registers in a 2901.

The IDT49C402s are fabricated using CEMOS™, a CMOS technology designed for high performance and high reliability. These performance-enhanced devices feature both bipolar speed and bipolar output drive capabilities, while maintaining exceptional microinstruction speeds at greatly reduced CMOS power levels.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology Inc.

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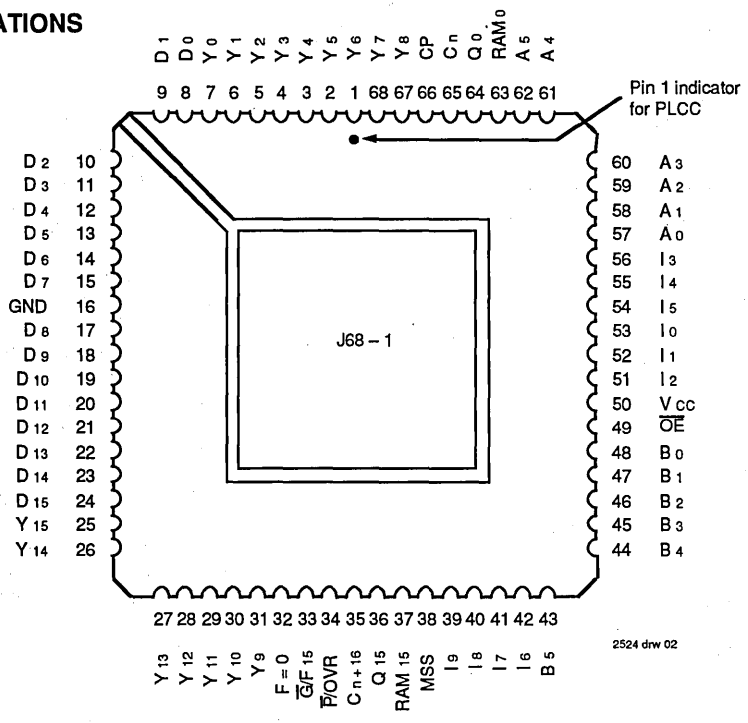
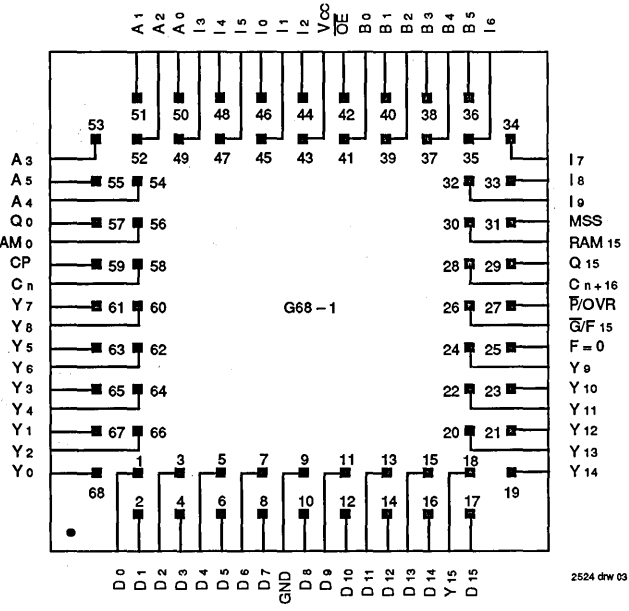
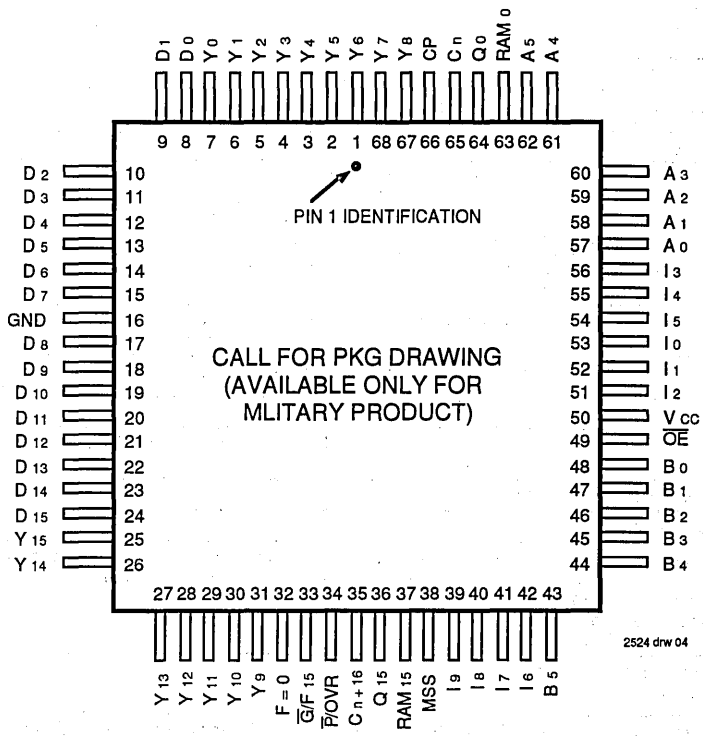
PIN CONFIGURATIONS



PLCC
TOP VIEW



PGA
TOP VIEW



FLATPACK
TOP VIEW

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PIN DESCRIPTIONS

Pin Name	I/O	Description
A_0 - A_5	I	Six address inputs to the register file which selects one register and displays its contents through the A port.
B_0 - B_5	I	Six address inputs to the register file which selects one of the registers in the file, the contents of which is displayed through the B port. It also selects the location into which new data can be written when the clock goes LOW.
I_0 - I_9	I	Ten instruction control lines which determine what data source will be applied to the ALU $I_{(0, 1, 2)}$, what function the ALU will perform $I_{(3, 4, 5)}$ and what data is to be deposited in the Q Register or the register file $I_{(6, 7, 8, 9)}$. Original 2901 destinations are selected if I_9 is disconnected in this mode, proper I_9 bias is achieved by an external pullup resistor to V_{CC} (47K ohms recommended).
D_0 - D_{15}	I	Sixteen-bit direct data inputs which are the data source for entering external data into the device ALU, Q Register or RAM. D_0 is the LSB.
Y_0 - Y_{15}	O	Sixteen three-state output lines which, when enabled, display either the sixteen outputs of the ALU or the data on the A port of the register stack. This is determined by the destination code $I_{(6, 7, 8, 9)}$.
$\overline{G}/F_{15}$	O	A multipurpose pin which indicates the carry generate ($\overline{G}$) function at the least significant and intermediate slices or as F_{15}, the most significant ALU output (sign bit). $\overline{G}/F_{15}$ selection is controlled by the MSS pin. If MSS = HIGH, F_{15} is enabled. If MSS = LOW, $\overline{G}$ is enabled.
F = 0	O	Open drain output which goes HIGH if the F_0 - F_{15} ALU outputs are all LOW. This indicates that the result of an ALU operation is zero (positive logic).
C_n	I	Carry-in to the internal ALU.
C_{n+16}	O	Carry-out of the ALU.
Q_{15} RAM_{15}	I/O	Bidirectional lines controlled by $I_{(6, 7, 8, 9)}$. Both are three-state output drivers connected to the TTL-compatible inputs. When the destination code on $I_{(6, 7, 8, 9)}$ indicates an up shift, the three-state outputs are enabled, the MSB of the Q Register is available on the Q_{15}, pin and the MSB of the ALU output is available on the RAM_{15} pin. When the destination code indicates a down shift, the pins are the data inputs to the MSB of the Q Register and the MSB of the RAM.
Q_0 RAM_0	I/O	Both bidirectional lines function identically to Q_{15} and RAM_{15} lines except they are the LSB of the Q Register and RAM.
$\overline{OE}$	I	Output enable. When pulled HIGH, the Y outputs are OFF (high impedance). When pulled LOW, the Y outputs are enabled.
$\overline{P}$/OVR	O	A multipurpose pin which indicates the carry propagate ($\overline{P}$) output for performing a carry lookahead operation or overflow (OVR) the Exclusive-OR of the carry-in and carry-out of the ALU MSB. OVR, at the most significant end of the word, indicates that the result of an arithmetic two's complement operation has overflowed into the sign bit. $\overline{P}$/OVR selection is controlled by the MSS pin. If MSS = HIGH, OVR is enabled. If MSS = LOW, $\overline{P}$ is enabled.
CP	I	The clock input LOW-to-HIGH clock transitions will change the Q Register and the register file outputs. Clock LOW time is internally the write enable time for the 64 x 16 RAM. While the clock is LOW, the slave latches on the RAM outputs are closed, storing the data previously on the RAM outputs. Synchronous MASTER-SLAVE operation of the register file is achieved by this.
MSS	I	When HIGH, enables OVR and F_{15} on the $\overline{P}$/OVR and $\overline{G}/F_{15}$ pins. When LOW, enables $\overline{G}$ and $\overline{P}$ on these pins. If left open, internal pullup resistor to Vcc provides declaration that the device is the most significant slice.

2524 tbl 01

DEVICE ARCHITECTURE

The IDT49C402 CMOS bit-slice microprocessor is configured sixteen bits wide and is cascadable to any number of bits (16, 32, 48, 64). Key elements which make up this 16-bit microprocessor slice are the 1) register file (64 x 16 dual-port RAM) with shifter; 2) ALU and 3) Q Register and shifter.

REGISTER FILE — A 16-bit data word from one of the 64 RAM registers can read from the A port as selected by the 6-bit A address field. Simultaneously, the same data word, or any other word from the 64 RAM registers, can be read from the B port as selected by the 6-bit B address field. New data is written into the RAM register location selected by the B address field during the clock (CP) LOW time. Two sixteen-bit latches hold the RAM A port and B port during the clock (CP) LOW time, eliminating any data races. During clock HIGH, these latches are transparent, reading the data selected by the A and B addresses. The RAM data input field is driven from a four-input multiplexer that selects the ALU output or the D inputs. The ALU output can be shifted up one position, down one position or not shifted. Shifting data operations involves the RAM_{15} and RAM_0 I/O pins. For a shift up operation, the RAM shifter MSB is connected to an enabled RAM_{15} I/O output, while the RAM_0 I/O input is selected as the input to the LSB. During a shift down operation, the RAM shifter LSB is connected to an enabled RAM_0 I/O output, while the RAM_{15} I/O input is selected as the input to the MSB.

ALU — The ALU can perform three binary arithmetic and five logic operations on the two 16-bit input words S and R. The S input field is driven from a 3-input multiplexer and the R input field is driven from a 2-input multiplexer, with both having a zero source operand. Both multiplexers are controlled by the $I_{(0, 1, 2)}$ inputs. This multiplexer configuration enables the user to select the various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. Microinstruction inputs $I_{(3, 4, 5)}$ are used to select the ALU function. This high-speed ALU cascades to any word length, providing carry-in (C_n), carry-out (C_{n+16}) and an open-drain (F = 0) output. When all bits of the ALU are zero, the pull-down device of F = 0 is off, allowing a wire-OR of this pin over all cascaded devices. Multipurpose pins $\overline{G}/F_{15}$ and $\overline{P}$/OVR are aimed at accelerating arithmetic operations. For intermediate and least significant slices, the MSS pin is programmed LOW, selecting the carry-generate ($\overline{G}$) and carry propagate ($\overline{P}$) output functions to be used by carry lookahead logic. For the most significant slice, MSS is programmed HIGH, selecting the sign-bit (F_{15}) and the two's complement overflow (OVR) output functions. The sign bit (F_{15}) allows the ALU sign bit to be monitored without enabling the three-state ALU outputs. The overflow (OVR) output is high when the two's complement arithmetic operation has overflowed into the sign bit, as logically determined from the Exclusive -OR of the carry-in and carry-out of the most significant bit of the ALU. The ALU data outputs are available at the three-state outputs $Y_{(0\text{-}15)}$ or as inputs to the RAM register file and Q register under control of the $I_{(6, 7, 8, 9)}$ instruction inputs.

Q REGISTER — The Q Register is a separate 16-bit file intended for multiplication and division routines and can also be used as an accumulator or holding register for other types of applications. It is driven from a 4-input multiplexer. In the no-shift mode, the multiplexer enters the ALU F output or Direct Data into the Q Register. In either the shift up or shift down mode, the multiplexer selects the Q Register data appropriately shifted up or down. The Q shifter has two ports, Q_0 and Q_{15}, which operate comparably to the RAM shifter. They are controlled by the $I_{(6, 7, 8, 9)}$ inputs.

The clock input of the IDT49C402 controls the RAM, Q Register and A and B data latches. When enabled, the data is clocked into the Q Register on the LOW- to-HIGH transition. When the clock is HIGH, the A and B latches are open and pass data that is present at the RAM outputs. When the clock is LOW, the latches are closed and retain the last data entered. When the clock is LOW and $I_{(6, 7, 8, 9)}$ define the RAM as the destination, new data will be written into the RAM file defined by the B address field.

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ALU SOURCE OPERAND CONTROL

Mnemonic	Microcode I2	I1	I0	Octal Code	ALU Source Operands R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

2524 tbl 02

ALU FUNCTION CONTROL

Mnemonic	Microcode I5	I4	I3	Octal Code	ALU Function	Symbol
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S – R
SUBS	L	H	L	2	R Minus S	R – S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
EXOR	H	H	L	6	R EX-OR S	R ∇ S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \nabla S}$

2524 tbl 04

ALU ARITHMETIC MODE FUNCTIONS

Octal I5, 4, 3	Octal I2, 1, 0	Cn = L Group	Cn = L Function	Cn = H Group	Cn = H Function
0	0	ADD	A + Q	ADD plus one	A + Q + 1
0	1		A + B		A + B + 1
0	5		D + A		D + A + 1
0	6		D + Q		D + Q + 1
0	2	PASS	Q	Increment	Q + 1
0	3		B		B + 1
0	4		A		A + 1
0	7		D		D + 1
1	2	Decrement	Q – 1	PASS	Q
1	3		B – 1		B
1	4		A – 1		A
2	7		D – 1		D
2	2	1's Comp.	–Q – 1	2's Comp. (Negate)	–Q
2	3		–B – 1		–B
2	4		–A – 1		–A
1	7		–D – 1		–D
1	0	Subtract (1's Comp)	Q – A – 1	Subtract (2's Comp)	Q – A
1	1		B – A – 1		B – A
1	5		A – D – 1		A – D
1	6		Q – D – 1		Q – D
2	0		A – Q – 1		A – Q
2	1		A – B – 1		A – B
2	5		D – A – 1		D – A
2	6		D – Q – 1		D – Q

2524 tbl 03

ALU LOGIC MODE FUNCTIONS

Octal I5, 4, 3	Octal I2, 1, 0	Group	Function
4	0	AND	A ∧ Q
4	1		A ∧ B
4	5		D ∧ A
4	6		D ∧ Q
3	0	OR	A ∨ Q
3	1		A ∨ B
3	5		D ∨ A
3	6		D ∨ Q
6	0	EX–OR	A ∇ Q
6	1		A ∇ B
6	5		D ∇ A
6	6		D ∇ Q
7	0	EX–NOR	$\overline{A \nabla Q}$
7	1		$\overline{A \nabla B}$
7	5		$\overline{D \nabla A}$
7	6		$\overline{D \nabla Q}$
7	2	INVERT	$\overline{Q}$
7	3		$\overline{B}$
7	4		$\overline{A}$
7	7		$\overline{D}$
6	2	PASS	Q
6	3		B
6	4		A
6	7		D
3	2	PASS	Q
3	3		B
3	4		A
3	7		D
4	2	"ZERO"	0
4	3		0
4	4		0
4	7		0
5	0	MASK	$\overline{A}$ ∧ Q
5	1		$\overline{A}$ ∧ B
5	5		$\overline{D}$ ∧ A
5	6		$\overline{D}$ ∧ Q

2524 tbl 05

SOURCE OPERAND AND ALU FUNCTION MATRIX (1)

Octal	ALU	I2, 1, 0 Octal							
		0	1	2	3	4	5	6	7
		ALU Source							
I5, 4, 3	Function	A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	Cn = L R Plus S Cn = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	Cn = L S Minus R Cn = H	Q – A – 1 Q – A	B – A – 1 B – A	Q – 1 Q	B – 1 B	A – 1 A	A – D – 1 A – D	Q – D – 1 Q – D	–D – 1 –D
2	Cn = L R Minus S Cn = H	A – Q – 1 A – Q	A – B – 1 A – B	–Q – 1 –Q	–B – 1 –B	–A – 1 –A	D – A – 1 D – A	D – Q – 1 D – Q	D – 1 D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ∇ Q	A ∇ B	Q	B	A	D ∇ A	D ∇ Q	D
7	R EX-NOR S	$\overline{A \nabla Q}$	$\overline{A \nabla B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \nabla A}$	$\overline{D \nabla Q}$	$\overline{D}$

2524 tbl 06

NOTE:
1. + = Plus; – = Minus; ∧ = AND; ∇ = EX-OR; ∨ = OR.

ALU DESTINATION CONTROL(1)

Mnemonic	Microcode I9	I8	I7	I6	Hex Code	RAM Function Shift	RAM Function Load	Q Register Function Shift	Q Register Function Load	Y Output	RAM Shifter RAM0	RAM Shifter RAM15	Q Shifter Q0	Q Shifter Q15	
OREG	H	L	L	L	8	X	NONE	NONE	F → Q	F	X	X	X	X	Existing 2901
NOP	H	L	L	H	9	X	NONE	X	NONE	F	X	X	X	X	Functions
RAMA	H	L	H	L	A	NONE	F → B	X	NONE	A	X	X	X	X	
RAMF	H	L	H	H	B	NONE	F → B	X	NONE	F	X	X	X	X	
RAMQD	H	H	L	L	C	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F0	IN15	Q0	IN15	
RAMD	H	H	L	H	D	DOWN	F/2 → B	X	NONE	F	F0	IN15	Q0	X	
RAMQU	H	H	H	L	E	UP	2F → B	UP	2Q → Q	F	IN0	F15	IN0	Q15	
RAMU	H	H	H	H	F	UP	2F → B	X	NONE	F	IN0	F15	X	Q15	
DFF	L	L	L	L	0	NONE	D → B	NONE	F → Q	F	X	X	X	X	New Added
DFA	L	L	L	H	1	NONE	D → B	NONE	F → Q	A	X	X	X	X	IDT49C402
FDF	L	L	H	L	2	NONE	F → B	NONE	D → Q	F	X	X	X	X	Functions
FDA	L	L	H	H	3	NONE	F → B	NONE	D → Q	A	X	X	X	X	
XQDF	L	H	L	L	4	X	NONE	DOWN	Q/2 → Q	F	X	X	Q0	IN15	
DXF	L	H	L	H	5	NONE	D → B	X	NONE	F	X	X	Q0	X	
XQUF	L	H	H	L	6	X	NONE	UP	2Q → Q	F	X	X	IN0	Q15	
XDF	L	H	H	H	7	X	NONE	NONE	D → Q	F	X	X	X	Q15	

NOTE:
2524 tbl 07
1. X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the impedance state.
   B = Register Addressed by B inputs.
   UP is toward MSB; DOWN is toward LSB.

8

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{CC}	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2524 tbl 08

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter (1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2524 tbl 09

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions (1)		Min.	Typ. (2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic High Level (4)		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level (4)		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–0.1	–5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –6mA MIL.	2.4	4.3	–	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8mA MIL.	–	0.3	0.5	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 10mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	–0.1	–10	µA
			V_O = V_{CC} (Max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V (3)		–15	–30	–70	mA

NOTES: 2524 tbl 10

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading, not production tested.
3. Not more than one output should be shorted at one time. Duration of the circuit test should not exceed one second.
4. These input levels should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQH}	Quiescent Power Supply Current	V_{CC} = Max.	MIL.	–	–	10	mA
	CP = H (CMOS Inputs)	V_{IH} = V_{CC}, V_{IL} = 0V	COM'L.	–	–	10	
		f_{CP} = 0, CP = H					
I_{CCQL}	Quiescent Power Supply Current	V_{CC} = Max.	MIL.	–	–	10	mA
	CP = L (CMOS Inputs)	V_{IH} = V_{CC}, V_{IL} = 0V	COM'L.	–	–	10	
		f_{CP} = 0, CP = L					
I_{CCT}	Quiescent Input Power Supply[6]	V_{CC} = Max., V_{IH} = 3.4V, f_{CP} = 0	MIL.	–	–	1.5	mA/
	Current (per Input @ TTL High)		COM'L.	–	–	0.85	Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max.	MIL.	–	–	7.5	mA/
		V_{IH} = V_{CC}, V_{IL} = 0V	COM'L.	–	–	4.5	MHz
		Outputs Open, $\overline{OE}$ = L					
I_{CC}	Total Power Supply Current[7]	V_{CC} = Max., f_{CP} = 10MHz	MIL.	–	–	85	mA
		Outputs Open, $\overline{OE}$ = L	COM'L.	–	–	55	
		CP = 50 % Duty cycle					
		V_{IH} = V_{CC}, V_{IL} = 0V					
		V_{CC} = Max., f_{CP} = 10MHz	MIL.	–	–	130	
		Outputs Open, $\overline{OE}$ = L	COM'L.	–	–	95	
		CP = 50 % Duty cycle					
		V_{IH} = 3.4V, V_{IL} = 0.4V					

2524 tbl 12

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading, not production tested.
3. Not more than one output should be shorted at one time. Duration of the circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.
5. Guaranteed by design, not production tested.
6. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
7. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:
   $I_{CC} = I_{CCQH} (C_{DH}) + I_{CCQL} (1 - C_{DH}) + I_{CCT} (N_T \times D_H) + I_{CCD} (f_{CP})$
   C_{DH} = Clock duty cycle high period
   D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
   N_T = Number of dynamic inputs driven at TTL levels
   f_{CP} = Clock input frequency
   I_{CCT} = Quiescent Power Supply Current for TTL level inputs
   I_{CCD} = Dynamic Power Supply Current in mA/MHz

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic testing environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.

8

AC ELECTRICAL CHARACTERISTICS IDT49C402

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C402 over the –55°C to +125°C and 0°C to +70°C temperature ranges. Vcc is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	Mil. (6)	Com'l.	Unit
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	50	48	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32)	20	21	MHz
Minimum Clock LOW Time	30	30	ns
Minimum Clock HIGH Time	20	20	ns
Minimum Clock Period	50	48	ns

2524 tbl 13

MAXIMUM COMBINATIONAL PROPAGATION DELAYS(1) C_L = 50pF

From Input	To Output: Y		(MSS = L) $\overline{G}$, $\overline{P}$		(MSS = H) F_{15}		(MSS = H) OVR		C_{n+16}		F = 0		RAM_0 RAM_{15}		Q_0 Q_{15}		Unit
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Address	52	47	47	42	52	47	47	42	38	34	52	47	44	40	–	–	ns
D	35	32	34	31	35	32	34	31	27	25	35	32	28	26	–	–	ns
C_n	29	26	–	–	29	26	27	25	20	18	29	26	23	21	–	–	ns
$I_{0,1,2}$	41	37	30	27	41	37	38	35	29	26	41	37	30	27	–	–	ns
$I_{3,4,5}$	40	36	28	26	40	36	37	34	27	25	40	36	28	26	–	–	ns
$I_{6,7,8,9}$	26	24	–	–	–	–	–	–	–	–	–	–	20	18	20	18	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	30	27	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ∫	42	38	41	37	42	38	41	37	30	27	42	38	41	37	25	23	ns

2524 tbl 14

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP: 

Input	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H		Unit
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Source Address	20	18	2 (3)	1 (3)	50 (4)	50 (4)	2	1	ns
B Destination Address	20	18	Do not change (2)				2	1	ns
D	– (1)	–	–	–	30/40 (5)	26/36 (5)	2	1	ns
C_n	–	–	–	–	35	32	0	0	ns
$I_{0,1,2}$	–	–	–	–	45	41	0	0	ns
$I_{3,4,5}$	–	–	–	–	45	41	0	0	ns
$I_{6,7,8,9}$	12	11	Do not change (2)				0	0	ns
$RAM_{0,15}$, $Q_{0,15}$	–	–	–	–	12	11	0	0	ns

2524 tbl 15

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination: i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).
6. Guaranteed by design, not production tested.

AC ELECTRICAL CHARACTERISTICS IDT49C402A

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C402A over the −55°C to +125°C and 0°C to +70°C temperature ranges. Vcc is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	Mil.(6)	Com'l.	Unit
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)(6)	23	22	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32)(6)	35	41	MHz
Minimum Clock LOW Time	13	11	ns
Minimum Clock HIGH Time	13	11	ns
Minimum Clock Period(6)	36	31	ns

2524 tbl 16

MAXIMUM COMBINATIONAL PROPAGATION DELAYS(1) C_L = 50pF

From Input	To Output: Y		(MSS = L) $\overline{G}$, $\overline{P}$		(MSS = H) F_{15}		(MSS = H) OVR		C_{n+16}		F = 0		RAM_0 RAM_{15}		Q_0 Q_{15}		Unit
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Address	41	37	39	35	41	37	41	37	37	34	41	37	40	36	–	–	ns
D	32	29	29	26	29	26	31	28	27	25	32	29	28	26	–	–	ns
C_n	28	25	–	–	26	24	25	23	20	18	29	26	23	21	–	–	ns
$I_{0,1,2}$	35	32	30	27	35	32	34	31	29	26	35	32	30	27	–	–	ns
$I_{3,4,5}$	35	32	28	26	34	31	34	31	27	25	35	32	28	26	–	–	ns
$I_{6,7,8,9}$	25	23	–	–	–	–	–	–	–	–	–	–	20	18	20	18	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	30	27	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ↓	34	31	31	28	33	30	34	31	30	27	34	31	34	31	25	23	ns

2524 tbl 17

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP: 

Input	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H		Unit
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Source Address	11	10	2 (3)	1 (3)	25 (4)	21 (4)	2	1	ns
B Destination Address	11	10	Do not change (2)				2	1	ns
D	– (1)	–	–	–	12/22 (5)	10/20 (5)	2	1	ns
C_n	–	–	–	–	17	15	0	0	ns
$I_{0,1,2}$	–	–	–	–	28	25	0	0	ns
$I_{3,4,5}$	–	–	–	–	28	25	0	0	ns
$I_{6,7,8,9}$	11	10	Do not change (2)				0	0	ns
$RAM_{0,15}$, $Q_{0,15}$	–	–	–	–	12	11	0	0	ns

2524 tbl 18

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination: i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).
6. Guaranteed by design, not production tested.

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AC ELECTRICAL CHARACTERISTICS IDT49C402B

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C402B over the −55°C to +125°C and 0°C to +70°C temperature ranges. Vcc is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	Mil.(6)	Com'l.	Unit
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)(6)	22	19	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32)(6)	52	60	MHz
Minimum Clock LOW Time	11	9	ns
Minimum Clock HIGH Time	11	9	ns
Minimum Clock Period(6)	24	20	ns

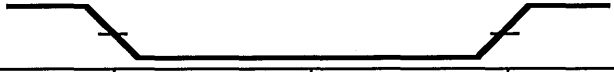
2524 tbl 19

MAXIMUM COMBINATIONAL PROPAGATION DELAYS(1) C_L = 50pF

From Input	To Output: Y		(MSS = L) $\overline{G}$, $\overline{P}$		(MSS = H) F_{15}		OVR		C_{n+16}		F = 0		RAM0 RAM15		Q0 Q15		
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Unit
A, B Address	33	28	31	26	31	28	31	28	28	26	31	28	32	29	–	–	ns
D	26	23	23	21	23	21	25	22	22	20	26	23	24	23	–	–	ns
C_n	22	20	–	–	20	18	19	17	15	14	22	20	18	17	–	–	ns
$I_{0,1,2}$	28	26	24	22	28	26	27	25	23	21	28	26	26	24	–	–	ns
$I_{3,4,5}$	28	26	22	21	27	25	27	25	22	20	28	26	25	23	–	–	ns
$I_{6,7,8,9}$	20	18	–	–	–	–	–	–	–	–	–	–	16	14	16	14	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	24	22	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ∫	27	25	25	22	26	24	27	25	–	–	27	25	27	25	–	–	ns

2524 tbl 20

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP: 

Input	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H		Unit
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Source Address	10	9	2 (3)	1 (3)	20 (4)	18 (4)	2	1	ns
B Destination Address	10	9	Do not change(2)				2	1	ns
D	– (1)	–	–	–	12/22(5)	10/20(5)	2	1	ns
C_n	–	–	–	–	16	14	0	0	ns
$I_{0,1,2}$	–	–	–	–	26	24	0	0	ns
$I_{3,4,5}$	–	–	–	–	26	24	0	0	ns
$I_{6,7,8,9}$	10	9	Do not change(2)				0	0	ns
$RAM_{0,15}$, $Q_{0,15}$	–	–	–	–	12	10	0	0	ns

2524 tbl 21

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination: i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).
6. Guaranteed by design, not production tested.

IDT49C402B
MAX. OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)
Tested at C_L = 50pF, correlated to 5pF

		Enable		Disable	
Input	Output	Mil.	Com'l.	Mil.	Com'l.
$\overline{OE}$	Y	18	16	15	13

2524 tbl 22

IDT49C402A
MAX. OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)
Tested at C_L = 50pF, correlated to 5pF

		Enable		Disable	
Input	Output	Mil.	Com'l.	Mil.	Com'l.
$\overline{OE}$	Y	22	20	20	18

2524 tbl 23

IDT49C402
MAX. OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)
Tested at C_L = 50pF, correlated to 5pF

		Enable		Disable	
Input	Output	Mil.	Com'l.	Mil.	Com'l.
$\overline{OE}$	Y	25	23	25	23

2524 tbl 24

CRITICAL SPEED PATH ANALYSIS

Critical speed paths are for the IDT49C402B versus the equivalent bipolar circuit implementation using four 2901Cs and one 2902A is shown below.

The IDT49C402B operates faster than the theoretically achievable values of the discrete bipolar implementation. Actual speed values for the discrete bipolar circuit will increase due to on-chip/off-chip circuit board delays.

TIMING COMPARISION: IDT49C402B vs 2901C w/2902A

16-Bit µP System	Data Path (Com'l.)		Data Path (Mil.)		Unit
	AB ADDR → F = 0	AB ADDR → $RAM_{0, 15}$	AB ADDR → F = 0	AB ADDR → $RAM_{0, 15}$	
Four 2901Cs + 2902A	≥ 71	≥ 71	≥ 83.5	≥ 83.5	ns
IDT49C402B	28	23	31	25	ns
Speed Savings	43	48	52	55	ns

2524 tbl 26

TIMING COMPARISION: IDT49C402A vs 2901C w/2902A

16-Bit µP System	Data Path (Com'l.)		Data Path (Mil.)		Unit
	AB ADDR → F = 0	AB ADDR → $RAM_{0, 15}$	AB ADDR → F = 0	AB ADDR → $RAM_{0, 15}$	
Four 2901Cs + 2902A	≥ 71	≥ 71	≥ 83.5	≥ 83.5	ns
IDT49C402A	37	36	41	25	ns
Speed Savings	34	35	42.5	43.5	ns

2524 tbl 27

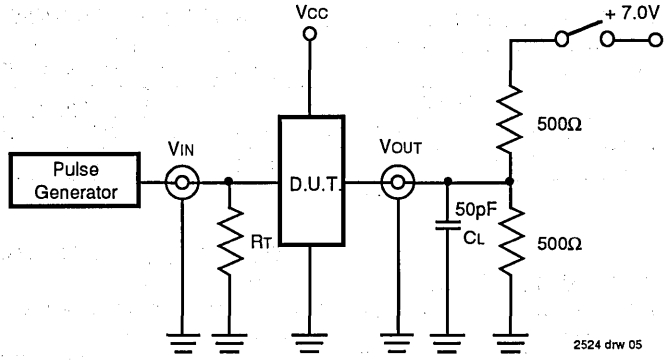
TIMING COMPARISION: IDT49C402 vs 2901C w/2902A

16-Bit µP System	Data Path (Com'l.)		Data Path (Mil.)		Unit
	AB ADDR → F = 0	AB ADDR → $RAM_{0, 15}$	AB ADDR → F = 0	AB ADDR → $RAM_{0, 15}$	
Four 2901Cs + 2902A	≥ 71	≥ 71	≥ 83.5	≥ 83.5	ns
IDT49C402A	47	40	52	44	ns
Speed Savings	24	31	31.5	39.5	ns

2524 tbl 28

8

TEST CIRCUIT LOAD



DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance
R_L = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

Figure 1. Switching Test Circuit (All Outputs)

INPUT/OUTPUT INTERFACE CIRCUIT

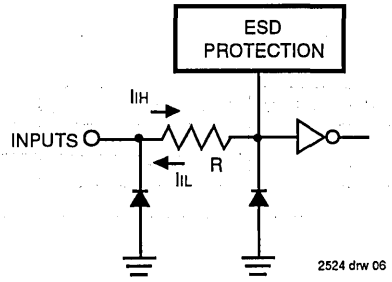


Figure 2. Input Structure (All Inputs)

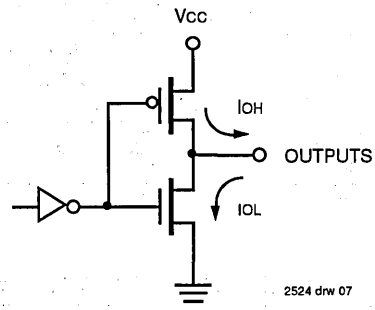


Figure 3. Outputs Structure (All Outputs Except F = 0)

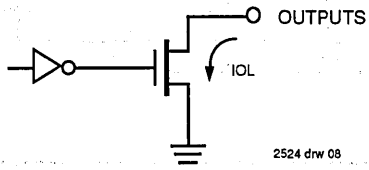


Figure 4. Outputs Structure (F = 0)

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2524 tbl 25

Test	Switch
Disable Low Enable Low	Closed
All other Tests	Open

2524 tbl 29

Integrated Device Technology, Inc.

16-BIT CMOS MICROPROGRAM SEQUENCER

IDT49C410
IDT49C410A

FEATURES:

- 16-bit wide address path
  - — Address up to 65,536 words of microprogram memory
- 16-bit loop counter
  - — Pre-settable down-counter for counting loop iterations and repeating instructions
- Low-power CEMOS™
  - — Icc (max.)
    Military: 90mA
    Commercial: 75 mA
- Fast
  - — IDT49C410 meets 2910A speeds
  - — IDT49C410A is a 30% speed upgrade
- 33-deep stack
  - — Accommodates highly nested microcode
- 16 powerful microinstructions
- Available in 48-pin, 600 mil plastic and sidebraze DIP, 52-pin PLCC and 48-pin Flatpack
- Three enables control branch address sources
- Four address sources
- 2910A instruction compatibility
- Military product available compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-88643 is listed for this function

DESCRIPTION:

The IDT49C410s are architecture and function code compatible to the 2910A with an expanded 16-bit address path, thus allowing for programs up to 65,536 words in length. They are microprogram address sequencers intended for controlling the sequence of execution of microinstructions stored in the microprogram memory. Besides the capability of sequential access, they provide conditional branching to any microinstruction within their 65,536 microword range.

The 33-deep stack provides microsubroutine return linkage and looping capability. The deep stack can be used for highly nested microcode applications. Microinstruction loop count control is provided with a count capability of 65,536.

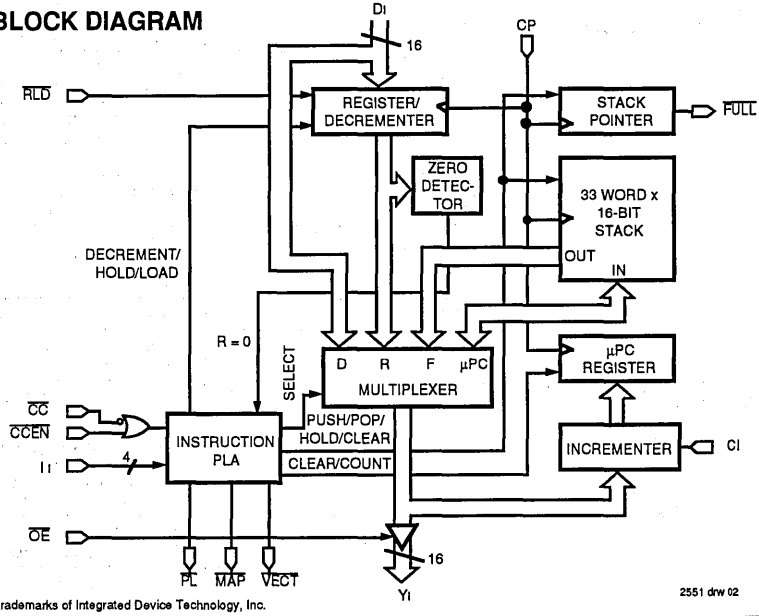
During each microinstruction, the microprogram controller provides a 16-bit address from one of four sources: 1) the microprogram address register (µPC), which usually contains an address one greater than the previous address; 2) an external (direct) input (D); 3) a register/counter (R) retaining data loaded during a previous microinstruction; or 4) a last-in/first-out stack (F).

The IDT49C10s are fabricated using CEMOS, a CMOS technology designed for high-performance and high-reliability.

The IDT49C410s are pin-compatible, performance-enhanced, easily upgradable versions of the 2910A.

The IDT49C410s are available in 48-pin DIP (600 mil x 100 mil centers), 52-pin PLCC and 48-pin flatpack.

FUNCTIONAL BLOCK DIAGRAM



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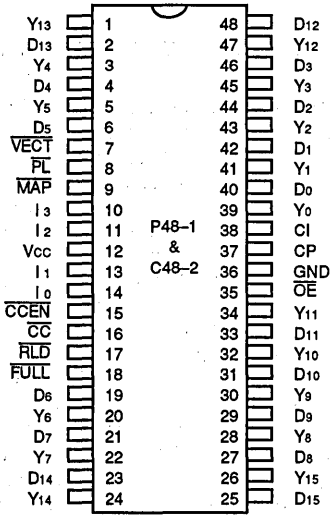
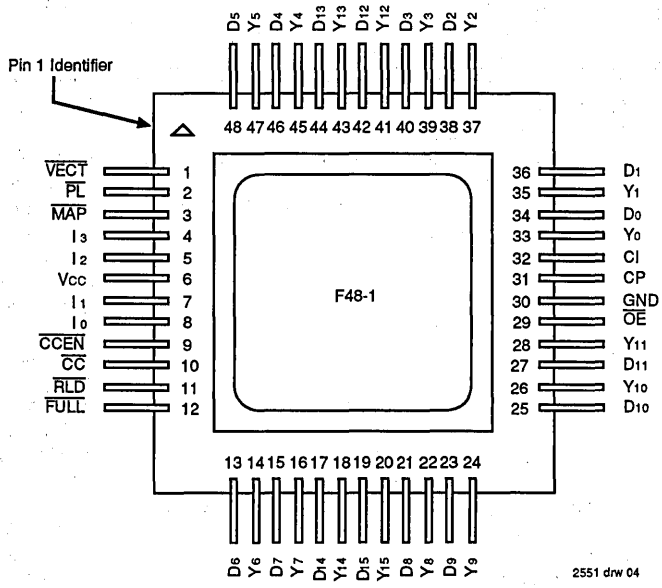
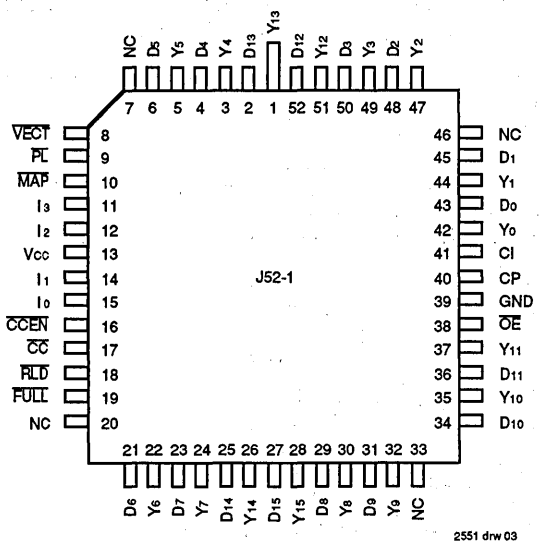
PIN CONFIGURATIONS



DIP
TOP VIEW



FLATPACK
TOP VIEW



PLCC
TOP VIEW

IDT49C410 PIN DESCRIPTIONS

Pin Name	I/O	Description
DI	I	Direct input to register/counter and multiplexer D0 is LSB.
II	I	Selects one-of-sixteen instructions.
$\overline{CC}$	I	Used as test criterion. A LOW on $\overline{CC}$ indicates "passed" test condition.
$\overline{CCEN}$	I	Whenever the signal is HIGH, $\overline{CC}$ is ignored and the device operates as though $\overline{CC}$ were true (LOW).
CI	I	Low order carry input to incrementer for microprogram counter.
$\overline{RLD}$	I	When LOW forces loading of register/ counter regardless of instruction or condition.
$\overline{OE}$	I	Three-state control of YI outputs.
CP	I	Triggers all internal state changes at LOW-to-HIGH edge.
YI	O	Address to microprogram memory. Y0 is LSB, Y15 is MSB.
$\overline{FULL}$	O	Indicates that 33 items are on the stack.
$\overline{PL}$	O	Can select #1 source (usually Pipeline Register) as direct input source.
$\overline{MAP}$	O	Can select #2 source (usually Mapping PROM or PLA) as direct input source.
$\overline{VECT}$	O	Can select #3 source (for example, Interrupt Starting Address) as direct input source.

2551 tbl 01

PRODUCT DESCRIPTION

The IDT49C410s are high-performance CMOS microprogram sequencers that are intended for use in very high-speed microprogrammable microprocessor applications. The sequencers allow for direct control of up to 64K words of microprogram.

The heart of the microprogram sequencers is a 4-input multiplexer that is used to select one of four address sources to select the next microprogram address. These address sources include the register/counter, the direct input, the microprogram counter or the stack as the source for the address of the next microinstruction.

The register/counter consists of sixteen D-type flip-flops which can contain either an address or a count. These edge-triggered flip-flops are under the control of a common clock enable, as well as the four microinstruction control inputs. When the load control ($\overline{RDL}$) is LOW, the data at the D inputs is loaded into this register on the LOW-to-HIGH transition of the clock. The output of the register/counter is available at the multiplexer as a possible next address source for the microcode. Also, the terminal count output associated with the register/counter is available at the internal instruction PLA to be used as condition code input for some of the microinstructions. The IDT49C410s contain a microprogram counter that usually contains the address of the next microinstruction compared to that currently being executed. The microprogram counter actually consists of a 16-bit incrementer followed by a 16-bit register. The microprogram counter will increment the address coming out of the sequencer going to the microprogram memory if the carry-in input to this counter is HIGH; otherwise, this address will be loaded into the microprogram counter. Normally, this carry-in input is set to the logic HIGH state so that the incrementer will be active. Should the carry-in input be set LOW, the same address is loaded into the microprogram counter. This is a technique that can be used to allow execution of the same microinstruction several times.

There are sixteen D-inputs on the IDT49C410s that go directly to the address multiplexer. These inputs are used to provide a branch address that can come directly from the microcode or some other external source. The fourth input available to the multiplexer for next address control is the 33-deep, 16-bit wide LIFO stack. The LIFO stack provides return address linkage for subroutines and loops. The IDT49C410s contain a built-in stack pointer that always points to the last stack location written. This allows for stack reference operations, usually called loops, to be performed without popping the stack.

The stack pointer internal to the IDT49C410s is actually an up/down counter. During the execution of microinstructions one, four and five, the PUSH operation may occur depending on the state of the condition code input. This causes the stack pointer to be incremented by one and the stack to be written with the required return linkage (the value contained in the microprogram counter). On the microprogram cycle following the PUSH, this new return linkage data that was in the microprogram counter is now at the new location pointed to by the stack pointer. Thus, any time the multiplexer looks at the stack, it will see this data on the top of the stack.

During five different microinstructions, a pop operation associated with the stack may occur. If the pop occurs, the stack pointer is decremented at the next LOW-to-HIGH transition of the clock. A pop decrements the stack pointer which is the equivalent of removing the old information from the top of the stack.

The IDT49C410s are designed so that the stack pointer linkage allows any sequence of pushes, pops or stack references to be used. The depth of the stack can grow to a full 33 locations. After a depth of 33 is reached, the $\overline{FULL}$ output goes LOW. If further PUSHes are attempted when the stack is full, the stack information at the top of the stack will be destroyed but the stack pointer will not end around. It is necessary to initialize the stack pointer when power is first turned on. This is performed by executing a RESET instruction (Instruction 0). This sets the stack pointer to the stack empty position — the equivalent depth of zero. Similarly, a pop from an empty stack may place unknown data on the Y outputs, but the stack pointer is designed not to end around. Thus, the stack pointer will remain at the 0 or stack empty location if a pop is executed while the stack is already empty.

The IDT49C410's internal 16-bit register/counter is used during microinstructions eight, nine and fifteen. During these instructions, the 16-bit counter acts as a down counter and the terminal count (count = 0) is used by the internal instruction PLA as an input to control the microinstruction branch test capability. The design of the internal counter is such that, if it is preloaded with a number N and then this counter is used in a microprogram loop, the actual sequence in the loop will be executed N + 1 times. Thus, it is possible to load the counter with a count of 0 and this will result in the microcode being executed one time. The 3-way branch microinstruction, instruction 15, uses both the loop counter and the external condition code input to control the final source address from the Y outputs of the microprogram sequencer. This 3-way branch may result in the next address coming from the D inputs, the stack or the microprogram counter.

The IDT49C410s provide a 16-bit address at the Y outputs that are under control of the $\overline{OE}$ input. Thus, the outputs can be put in the three-state mode, allowing the writable control store to be loaded or certain types of external diagnostics to be executed.

In summary, the IDT49C410s are the most powerful microprogram sequencers currently available. They provide the deepest stack, the highest performance and lowest power dissipation for today's microprogrammed machine design.

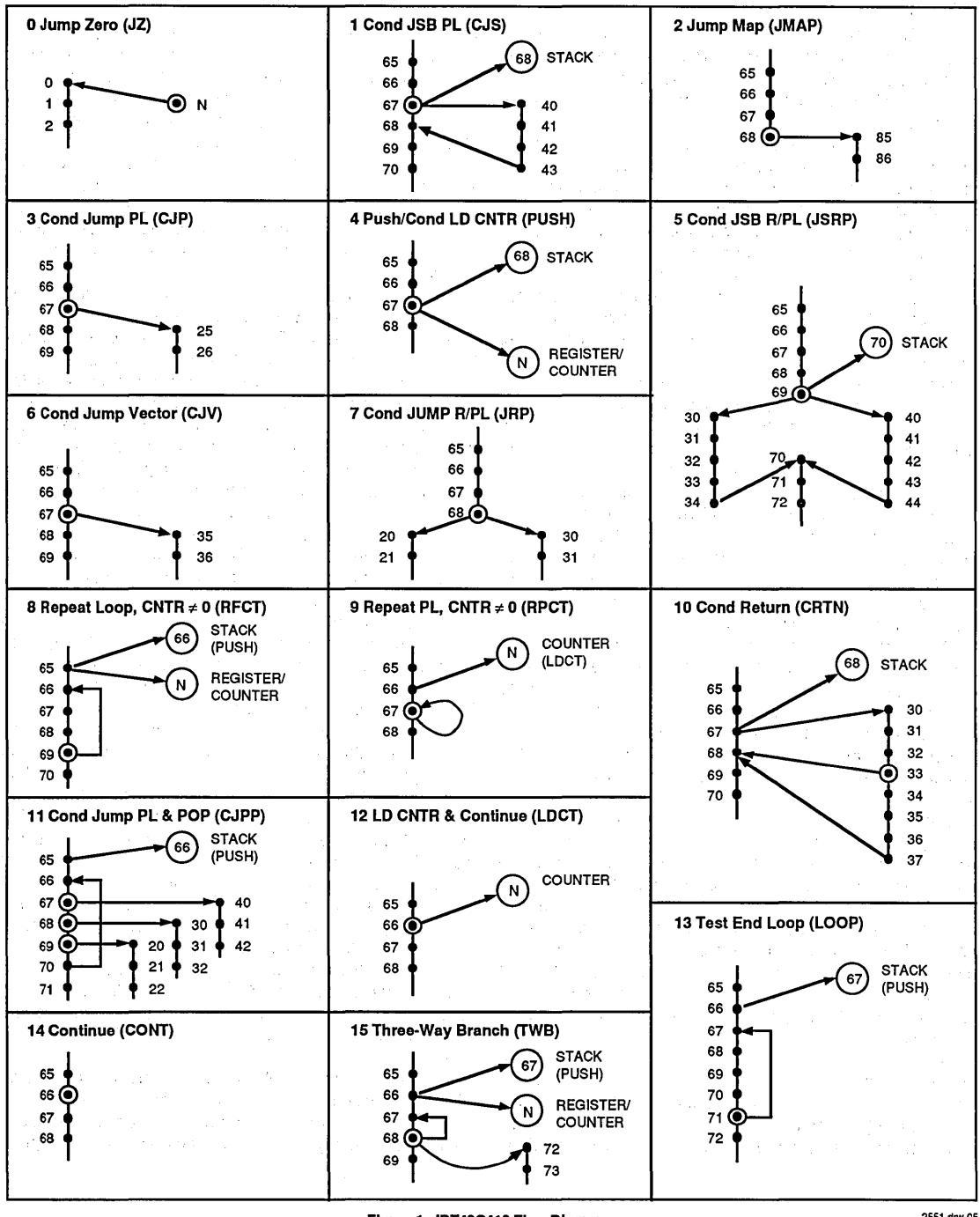


Figure 1. IDT49C410 Flow Diagrams

2551 drw 05

IDT49C410 OPERATION

The IDT49C410s are CMOS pin-compatible implementations of the Am2910 and 2910A microprogram sequencers. The IDT49C410 sequencers are functionally identical except that they are 16 bits wide and provide a 33-deep stack to give the microprogrammer more capability in terms of microprogram subroutines and microprogram loops. The definition of each microprogram instruction is shown in the table of instructions. This table shows the results of each instruction in terms of controlling the multiplexer, which determines the Y outputs, and in controlling the signals that can be used to enable various branch address sources ($\overline{PL}$, $\overline{MAP}$, $\overline{VECT}$). The operation of the register/counter and the 33-deep stack after the next LOW-to-HIGH transition of the clock are also shown. The internal multiplexer is used to select which of the internal sources is used to drive the Y outputs. The actual value loaded into the microprogram counter is either identical to the Y output or the Y output value is incremented by 1 and placed in the microprogram counter. This function is under the control of the carry inputs. For each of the microinstruction inputs, only one of the three outputs ($\overline{PL}$, $\overline{MAP}$ or $\overline{VECT}$) will be LOW. Note that this function is not determined by any of the possible condition code inputs. These outputs can be used to control the three-state selection of one of the sources for the microprogram branches.

Two inputs, $\overline{CC}$ and $\overline{CCEN}$, can be used to control the conditional instructions. These are fully defined in the table of instructions. The $\overline{RLD}$ input can be used to load the internal register/counter at any time. When this input is LOW, the data at the D inputs will be loaded into this register/counter on the LOW-to-HIGH transition of the clock. Thus, the $\overline{RLD}$ input overrides the internal hold or decrement operations specified by the various microinstructions. The $\overline{OE}$ input is normally LOW and is used as the three-state enable for the Y outputs. The internal stack in the IDT49C410s is a last-in/first-out memory that is 16-bits in width and 33 words deep. It has a stack pointer that addresses the stack and always points to the value currently on the top of the stack. When instruction 0 (RESET) is executed, the stack pointer is initialized to the top of the stack which is, by definition, the stack empty condition. Thus, the contents of the top of the stack are undefined until the forced PUSH occurs. A pop performed while the stack is empty will not change the stack pointer in any way; however, it will result in unknown data at the Y outputs.

By definition, the stack is full any time 33 more PUSHes than pops have occurred since the stack was last empty. When this happens, the $\overline{FULL}$ Flag will go LOW. This signal first goes LOW on the microcycle after the 33 pushes occur. When this signal is LOW, no additional pushes should be attempted or the information on the top of the stack will be lost.

THE IDT49C410 INSTRUCTION SET

This data sheet contains a block diagram of the IDT49C410 microprogram sequencers. As can be seen, the devices are controlled by a 4-bit microinstruction word (I3 - I0). Normally, this word is supplied from one 4-bit field of the microinstruction word associated with the entire state machine system. These four bits provide for the selection of one of the sixteen powerful instructions associated with selecting the address of the next microinstruction. Unused Y outputs can be left open; however, the corresponding most significant D inputs should be tied to ground for smaller microwords. This is necessary to make sure the internal operation of the counter is proper should less than 64K of microcode be implemented. As shown in the block diagram, the internal instruction PLA uses the four instruction inputs as well as the $\overline{CC}$, $\overline{CCEN}$ and the internal counter = 0 line for controlling the sequencer. This internal instruction PLA provides all of the necessary internal control signals to control each particular part of the microprogram sequencer. The next address at the Y outputs of the IDT49C410s can be from one of four sources. These include the internal microprogram counter, the last-in/first-out stack, the register/counter and the direct inputs.

The following paragraphs will describe each instruction associated with the IDT49C410s. As a part of the discussion, an example of each instruction is shown in Figure 1. The purpose of the examples is to show microprogram flow. Thus, in each example the microinstruction currently being executed has a circle around it. That is, this microinstruction is assumed to be the contents of the pipeline register at the output of the microprogram memory. In these drawings, each of the dots refers to the time that the contents of the microprogram memory word would be in the pipeline register and is currently being executed.

INSTRUCTION 0 – JUMP 0 (JZ)

This Conditional Jump is used at power-up time or at any restart sequence when the need is to reset the stack pointer and jump to the very first address in microprogram memory. The Jump 0 instruction does not change the contents of the register/counter.

INSTRUCTION 1 – CONDITIONAL JUMP TO SUBROUTINE (CJS)

The Conditional Jump to Subroutine instruction is the one used to call microprogram subroutines. The subroutine address will be contained in the pipeline register and presented at the D inputs. If the condition code test is passed, a branch is taken to the subroutine. Referring to the flow diagram for the IDT49C410s shown in Figure 1, we see that the content of the microprogram counter is 68. This value is pushed onto the stack and the top of stack pointer is incremented. If the test is failed, this Conditional Jump to Subroutine instruction behaves as a simple continue. That is, the content of microinstruction address 68 is executed next.

INSTRUCTION 2 – JUMP MAP (JMAP)

This sequencer instruction can be used to start different microprogram routines based on the machine instruction opcode. This is typically accomplished by using a mapping PROM as an input to the D inputs on the microprogram sequencer. The JMAP instruction branches to the address appearing on the D inputs. In the flow diagram shown in Figure 1, we see that the branch actually will be the contents of microinstruction 85 and this instruction will be executed next.

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IDT49C410 INSTRUCTION OPERATIONAL SUMMARY

$I_3 - I_0$	Mnemonic	CC	Counter Test	Stack	Address Source	Register Counter	Enable Select
0	JZ	X	X	CLEAR	0	NC	$\overline{PL}$
1	CJS	PASS FAIL	X X	PUSH NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
2	JMAP	X	X	NC	D	NC	$\overline{MAP}$
3	CJP	PASS FAIL	X X	NC NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
4	PUSH	PASS FAIL	X X	PUSH PUSH	PC PC	LOAD NC	$\overline{PL}$ $\overline{PL}$
5	JSRP	PASS FAIL	X X	PUSH PUSH	D R	NC NC	$\overline{PL}$ $\overline{PL}$
6	CJV	PASS FAIL	X X	NC NC	D PC	NC NC	$\overline{VECT}$ $\overline{VECT}$
7	JRP	PASS FAIL	X X	NC NC	D R	NC NC	$\overline{PL}$ $\overline{PL}$
8	RFCT	X X	= 0 NOT = 0	POP NC	PC STACK	NC DEC	$\overline{PL}$ $\overline{PL}$
9	RPCT	X X	= 0 NOT = 0	NC NC	PC D	NC DEC	$\overline{PL}$ $\overline{PL}$
10	CRTN	PASS FAIL	X X	POP NC	STACK PC	NC NC	$\overline{PL}$ $\overline{PL}$
11	CJPP	PASS FAIL	X X	POP NC	D PC	NC NC	$\overline{PL}$ $\overline{PL}$
12	LDCT	X	X	NC	PC	LOAD	$\overline{PL}$
13	LOOP	PASS FAIL	X X	POP NC	PC STACK	NC NC	$\overline{PL}$ $\overline{PL}$
14	CONT	X	X	NC	PC	NC	$\overline{PL}$
15	TWB	PASS PASS FAIL FAIL	= 0 NOT = 0 = 0 NOT = 0	POP POP POP NC	PC PC D STACK	NC DEC NC DEC	$\overline{PL}$ $\overline{PL}$ $\overline{PL}$ $\overline{PL}$

NC = No Change; DEC = Decrement

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INSTRUCTION 3 – CONDITIONAL JUMP PIPELINE (CJP)

The simplest branching control available in the IDT49C410 microprogram sequencers is that of conditional jump to address. In this instruction, the jump address is usually contained in the microinstruction pipeline register and presented to the D inputs. If the test is passed, the jump is taken while, if the test fails, this instruction executes as a simple continue. In the example shown in the flow diagram of Figure 1, we see that if the test is passed, the next microinstruction to be executed is the content of address 25. If the test is failed, the microcode simply continues to the contents of the next instruction.

INSTRUCTION 4 – PUSH/CONDITIONAL LOAD COUNTER (PUSH)

With this instruction, the counter can be conditionally loaded during the same instruction that pushes the current value of the microprogram counter on to the stack. Under any condition independent of the conditional testing, the microprogram counter is pushed on to the stack. If the conditional test is passed, the counter will be loaded with the value on the D inputs to the sequencer. If the test fails, the contents of the counter will not change. The PUSH/Conditional Load Counter instruction is used in conjunction with the loop instruction (Instruction 13), the repeat file based on the counter instruction (Instruction 9) or the 3-way branch instruction (Instruction 15).

INSTRUCTION 5 – CONDITIONAL JUMP TO SUBROUTINE R/PL (JSRP)

Subroutines may be called by a Conditional Jump Subroutine from the internal register or from the external pipeline register. In this instruction the contents of the microprogram counter are pushed on the stack and the branch address for the subroutine call will be taken from either the internal register/counter or the external pipeline register presented to the D inputs. If the conditional test is passed, the subroutine address will be taken from the pipeline register. If the conditional test fails, the branch address is taken from the internal register/counter. An example of this is shown in the flow diagram of Figure 1.

INSTRUCTION 6 – CONDITIONAL JUMP VECTOR (CJV)

The Conditional Jump Vector instruction is similar to the Jump Map instruction in that it allows a branch operation to a microinstruction as defined from some external source,

except that it is conditional. The Jump Map instruction is unconditional. If the conditional test is passed, the branch is taken to the new address on the D inputs. If the conditional test is failed, no branch is taken but rather the microcode simply continues to the next sequential microinstruction. When this instruction is executed, the $\overline{VECT}$ output is LOW unconditionally. Thus, an external 12-bit field can be enabled on to the D inputs of the microprogram sequencer.

INSTRUCTION 7 –
CONDITIONAL JUMP R/PL (JRP)

The Conditional Jump register/counter or external pipeline register always causes a branch in microcode. This jump will be to one of two different locations in the microcode address space. If the test is passed, the jump will be to the address presented on the D inputs to the microprogram sequencer. If the conditional test fails, the branch will be to the address contained in the internal register/counter.

INSTRUCTION 8 –
REPEAT LOOP COUNTER NOT EQUAL TO 0 (RFCT)

This instruction utilizes the loop counter and the stack to implement microprogrammed loops. The start address for the loop would be initialized by using the PUSH/Conditional Load Counter instruction. Then, when the repeat loop instruction is executed, if the counter is not equal to 0, the next microword address will be taken from the stack. This will cause a loop to be executed as shown in the Figure 1 flow diagram. Each time the microcode sequence goes around the loop, the counter is decremented. When the counter reaches 0, the stack will be popped and the microinstruction address will be taken from the microprogram counter. This instruction performs a timed wait or allows a single sequence to be executed the desired number of times. Remember, the actual number of loops performed is equal to the value in the counter plus 1.

INSTRUCTION 9 –
REPEAT PIPELINE, COUNTER NOT EQUAL TO 0 (RPCT)

This instruction is another technique for implementing a loop using the counter. Here, the branch address for the loop is contained in the pipeline register. This instruction does not use the stack in any way as a part of its implementation. As long as the counter is not equal to 0, the next microword address will be taken from the D inputs of the microprogram sequencer. When the counter reaches 0, the internal multiplexer will select the address source from the microprogram counter, thus causing the microcode to continue on and leave the loop.

INSTRUCTION 10 –
CONDITIONAL RETURN (CRTN)

The Conditional Return instruction is used for terminating subroutines. The fact that it is conditional allows the subroutine either to be ended or to continue. If the conditional test is passed, the address of the next microinstruction will be taken from the stack and it will be popped. If the conditional test fails, the next microinstruction address will come from the internal microprogram counter. This is depicted in the flow diagram of Figure 1. It is important to remember that every subroutine call must somewhere be followed by a return from subroutine call in order to have an equal number of pushes and pops on the stack.

INSTRUCTION 11 –
CONDITIONAL JUMP PIPELINE AND POP (CJPP)

The Conditional Jump Pipeline and Pop instruction is a technique for exiting a loop from within the middle of the loop. This is depicted fully in the flow diagram for the IDT49C410s, as shown in Figure 1. The conditional test input for this instruction results in a branch being taken if the test is passed. The address selected will be that on the D inputs to the microprogram sequencer and, since the loop is being terminated, the stack will popped. Should the test be failed on the conditional test inputs, the microprogram will simply continue to the next address as taken from the microprogram counter. The stack will not be affected if the conditional test input is failed.

INSTRUCTION 12 –
LOAD COUNTER AND CONTINUE (LDCT)

The Load Counter and Continue instruction is used to place a value on the D inputs in the register/counter and continue to the next microinstruction.

INSTRUCTION 13 –
TEST END OF LOOP (LOOP)

The Test End of Loop instruction is used as a last instruction in a loop associated with the stack. During this instruction, if the conditional test input is failed, the loop branch address will be that on the stack. Since we may go around the loop a number of times, the stack is not popped. If the conditional test input is passed, then the loop is terminated and the stack is popped. Notice that the loop instruction requires a PUSH to be performed at the instruction immediately prior to the loop return address. This is necessary so as to have the correct address on the stack before the loop operation. It is for this reason that the stack pointer always points to the last thing written on the stack.

INSTRUCTION 14 –
CONTINUE (CONT)

The Continue instruction is a simple instruction whereby the address for the microinstruction is taken from the microprogram counter. This instruction simply causes sequential program flow to the next microinstruction in microcode memory.

INSTRUCTION 15 –
THREE WAY BRANCH (TWB)

The Three Way Branch instruction is used for looping while waiting for a conditional event to come true. If the event does not come true after some number of microinstructions, a branch is taken to another microprogram sequence. This is depicted in Figure 1 showing the IDT49C410 flow diagrams and is also described in full detail in the IDT49C410's instruction operational summary. Operation of the instruction is such that any time the external conditional test input is passed, the next microinstruction will be that associated with the program counter and the loop will be left. The stack is also popped. Thus, the external test input overrides the other possibilities. Should the external test input not be true, the rest of the operation is controlled by the internal counter. If the counter

is not equal to 0, the loop is taken by selecting the address on the top of the stack as the address out of the Y outputs of the IDT49C410. In addition, the counter is decremented. Should the external conditional test input be failed and the counter also have counted to 0, this instruction "times out". The result is that the stack is popped and a branch is taken to the address presented to the D inputs of the IDT49C410 microprogram sequencer. This address is usually provided by the external pipeline register.

CONDITIONAL TEST

Throughout this discussion we have talked about microcode passing the conditional test. There are actually two inputs associated with the conditional test input. These include the $\overline{CCEN}$ and the $\overline{CC}$ inputs. The $\overline{CCEN}$ input is a condition code enable. Whenever the $\overline{CCEN}$ input is HIGH, the $\overline{CC}$ input is ignored and the device operates as though the $\overline{CC}$ input were true (LOW). Thus, a fail of the external test condition can be defined as $\overline{CCEN}$ equals LOW and $\overline{CC}$ equals HIGH. A pass condition is defined as a $\overline{CCEN}$ equal to HIGH or a $\overline{CC}$ equal to LOW. It is important to recognize the full function of the condition code enable and the condition code inputs in order to understand when the test is passed or failed.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{CC}	Power Supply Voltage	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	30	30	mA

NOTE: 2551 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2551 tbl 04

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to + 70°C, V_{CC} = 5.0V ± 5%; Military: T_A = – 55°C to + 125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions (1)		Min.	Typ. (2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level (4)		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level (4)		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	– 0.1	– 5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –12 mA MIL	2.4	4.3	–	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15 mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 20 mA MIL	–	0.3	0.5	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA COM'L	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	– 0.1	– 10	µA
			V_O = V_{CC} (Max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V (3)		– 30	–	–	mA

NOTES: 2551 tbl 05

1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the circuit test should not exceed one second.
4. These input levels should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS (Cont'd.)

Commercial: T_A = 0°C to + 70°C, V_{CC} = 5.0V ± 5%; Military: T_A = – 55°C to + 125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions [1]		Min.	Typ. [2]	Max.	Unit
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. V_{IN} = V_{CC} or GND f_{CP} = 0, CP = H		–	35	50	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. V_{IN} = V_{CC} or GND f_{CP} = 0, CP = L		–	35	50	mA
I_{CCT}	Quiescent Input Power Supply Current (per Input @ TTL High) [5]	V_{CC} = Max., V_{IH} = 3.4V, f_{CP} = 0		–	0.3	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. V_{IN} = V_{CC} or GND Outputs Open, $\overline{OE}$ = L	MIL COM'L	– –	1.0 1.0	3.0 1.5	mA/ MHz
I_{CC}	Total Power Supply Current [6]	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50 % Duty cycle $V_{HC} \leq V_{IH}$, $V_{IL} \leq V_{LC}$	MIL COM'L	– –	45 45	80 65	mA
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50 % Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL COM'L	– –	50 50	90 75	

NOTES:

2551 tbl 06

5. I_{CCQT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$I_{CC} = I_{CCQH} (CD_H) + I_{CCQL} (1 - CD_H) + I_{CCT} (N_T \times D_H) + I_{CCD} (f_{CP})$

CD_H = Clock duty cycle high period
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
N_T = Number of dynamic inputs driven at TTL levels
f_{CP} = Clock Input frequency

CMOS TESTING CONSIDERATIONS

There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large Vcc current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscillate causing improper device operation and possible latchup.
3) Definition of input levels is very important. Since many inputs may change coincidentally, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

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IDT49C410A
AC ELECTRICAL CHARACTERISTICS
I. SET-UP AND HOLD TIMES

Inputs	t (S)		t (H)		Unit
	Com'l.	Mil.	Com'l.	Mil.	
DI → R	6	7	0	0	ns
DI → PC	13	15	0	0	ns
I 0–3	23	25	0	0	ns
$\overline{CC}$	15	18	0	0	ns
$\overline{CCEN}$	15	18	0	0	ns
CI	6	7	0	0	ns
$\overline{RLD}$	11	12	0	0	ns

2551 tbl 07

II. COMBINATIONAL DELAYS

Inputs	Y		$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$		$\overline{FULL}$		Unit
	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
D0–11	12	15	–	–	–	–	ns
I 0–3	20	25	13	15	–	–	ns
$\overline{CC}$	16	20	–	–	–	–	ns
$\overline{CCEN}$	16	20	–	–	–	–	ns
CP	28	33	–	–	22	25	ns
$\overline{OE}$ (1)	10/10	13/13	–	–	–	–	ns

NOTE:
1. Enable/Disable. Disable times measure to 0.5V change on output voltage level with C_L = 5pF. Tested at C_L = 50pF, correlated to 5pF.

2551 tbl 08

III. CLOCK REQUIREMENTS

	Com'l.	Mil.	Unit
Minimum Clock LOW Time	18	20	ns
Minimum Clock HIGH Time	17	20	ns
Minimum Clock Period	35	40	ns

2551 tbl 09

IDT49C410
AC ELECTRICAL CHARACTERISTICS
I. SET-UP AND HOLD TIMES

Inputs	t (S)		t (H)		Unit
	Com'l.	Mil.	Com'l.	Mil.	
DI → R	16	16	0	0	ns
DI → PC	30	30	0	0	ns
I 0–3	35	38	0	0	ns
$\overline{CC}$	24	35	0	0	ns
$\overline{CCEN}$	24	35	0	0	ns
CI	18	18	0	0	ns
$\overline{RLD}$	19	20	0	0	ns

2551 tbl 10

II. COMBINATIONAL DELAYS

Inputs	Y		$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$		$\overline{FULL}$		Unit
	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
D0–11	20	25	–	–	–	–	ns
I 0–3	35	40	30	35	–	–	ns
$\overline{CC}$	30	36	–	–	–	–	ns
$\overline{CCEN}$	30	36	–	–	–	–	ns
CP	40	46	–	–	31	35	ns
$\overline{OE}$ (1)	25/27	25/30	–	–	–	–	ns

NOTE:
1. Enable/Disable. Disable times measure to 0.5V change on output voltage level with C_L = 5pF. Tested at C_L = 50pF, correlated to 5pF.

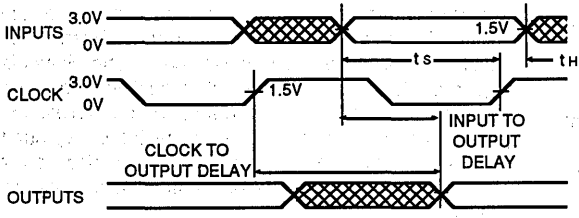
2551 tbl 11

III. CLOCK REQUIREMENTS

	Com'l.	Mil.	Unit
Minimum Clock LOW Time	20	25	ns
Minimum Clock HIGH Time	20	25	ns
Minimum Clock Period	50	51	ns

2551 tbl 12

SWITCHING WAVEFORMS



2551 drw 06

IDT49C410 INPUT/OUTPUT INTERFACE CIRCUITRY

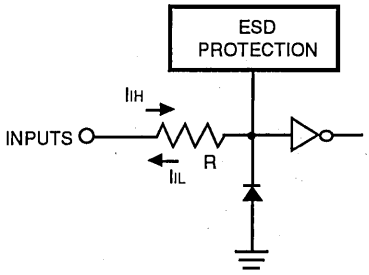


Figure 2. Input Structure

2551 drw 07

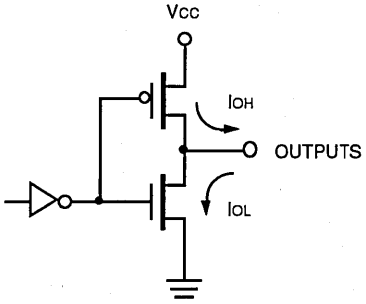
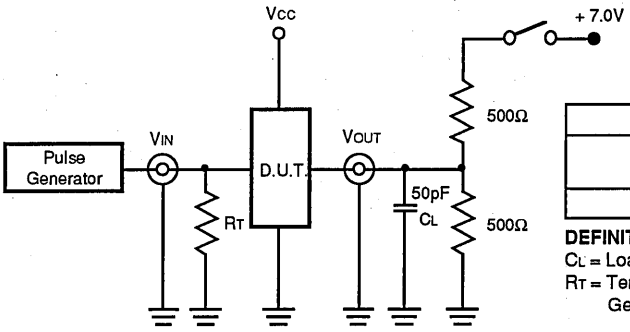


Figure 3. Output Structure

2551 drw 08

TEST LOAD CIRCUIT



Test	Switch
Disable Low Enable Low	Closed
All other Tests	Open

2551 tbl 13

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

Figure 4. Switching Test Circuits

2551 drw 09

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 3

2551 tbl 14

8

Integrated Device Technology, Inc.

16 x 16 PARALLEL CMOS MULTIPLIER-ACCUMULATOR

IDT7210L

FEATURES:

- 16 x 16 parallel multiplier-accumulator with selectable accumulation and subtraction
- High-speed: 25ns multiply-accumulate time
- IDT7210 features selectable accumulation, subtraction, rounding and preloading with 35-bit result
- IDT7210 is pin and function compatible with the TRW TDC1010J, TMC2210, Cypress CY7C510, and AMD AM29510
- Performs subtraction and double precision addition and multiplication
- Produced using advanced CEMOS™ high-performance technology
- TTL-compatible
- Available in plastic and topbraze DIP, PLCC, Flatpack and Pin Grid Array
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-88733 is listed on this function
- Speeds available:
  Commercial: L25/35/45/55/65
  Military: L30/40/55/65/75

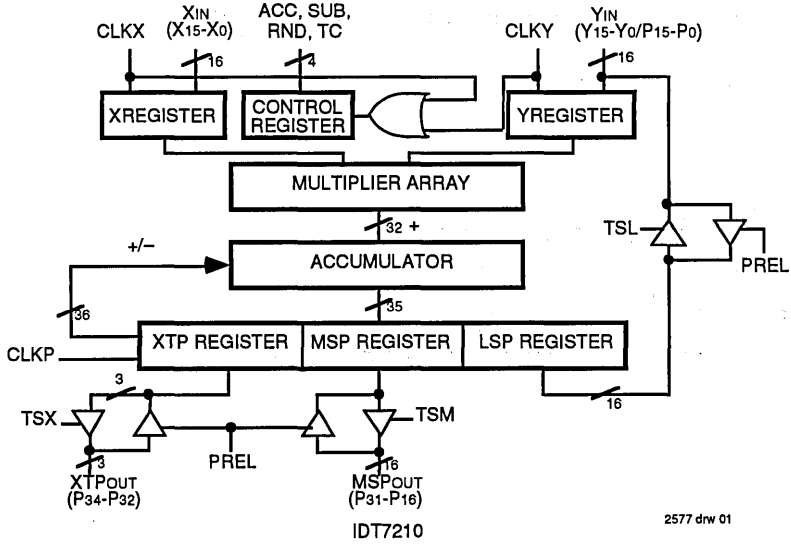
DESCRIPTION:

The IDT7210 is a high-speed, low-power 16 x 16-bit parallel multiplier-accumulator that is ideally suited for real-time digital signal processing applications. Fabricated using CEMOS silicon gate technology, this device offers a very low-power alternative to existing bipolar and NMOS counterparts, with only 1/7 to 1/10 the power dissipation and exceptional speed (25ns maximum) performance.

A pin and functional replacement for TRW's TDC1010J the IDT7210 operates from a single 5 volt supply and is compatible with standard TTL logic levels. The architecture of the IDT7210 is fairly straightforward, featuring individual input and output registers with clocked D-type flip-flop, a preload capability which enables input data to be preloaded into the output registers, individual three-state output ports for the Extended Product (XTP) and Most Significant Product (MSP) and a Least Significant Product output (LSP) which is multiplexed with the Y input.

The XIN and YIN data input registers may be specified through the use of the Two's Complement input (TC) as either a two's complement or an unsigned magnitude, yielding a full-precision 32-bit result that may be accumulated to a full 35-bit result. The three output registers – Extended Product (XTP), Most Most Significant Product (MSP) and Least Significant Product (LSP) – are controlled by the respective TSX, TSM and TSL input lines. The LSP output can be routed through YIN ports.

FUNCTIONAL BLOCK DIAGRAM

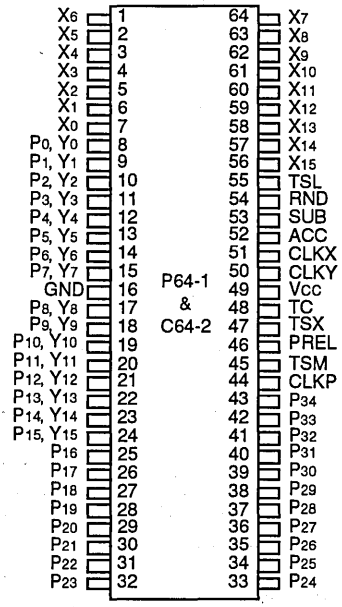


CEMOS is a trademark of Integrated Device Technology, Inc.

DESCRIPTION (Continued)

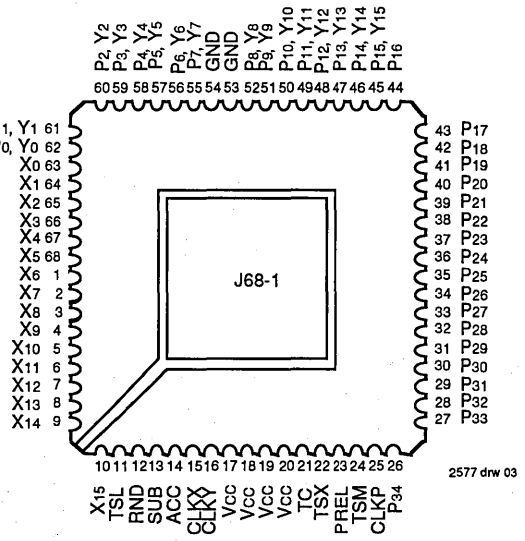
The Accumulate input (ACC) enables the device to perform either a multiply or a multiply-accumulate function. In the multiply-accumulate mode, output data can be added to or subtracted from previous results. When the Subtraction (SUB) input is active simultaneously with an active ACC, a subtraction can be performed. The double precision accumulated result is rounded down to either a single precision or single precision plus 3-bit extended result. In the multiply mode, the Extended Product output (XTP) is sign extended in the two's complement mode or set to zero in the unsigned mode. The Round (RND) control rounds up the Most Significant Product (MSP) and the 3-bit Extended Product (XTP) outputs. When Preload input (PREL) is active, all the output buffers are forced into a high-impedance state (see Preload truth table) and external data can be loaded into the output register by using the TSX, TSL and TSM signals as input controls.

PIN CONFIGURATIONS



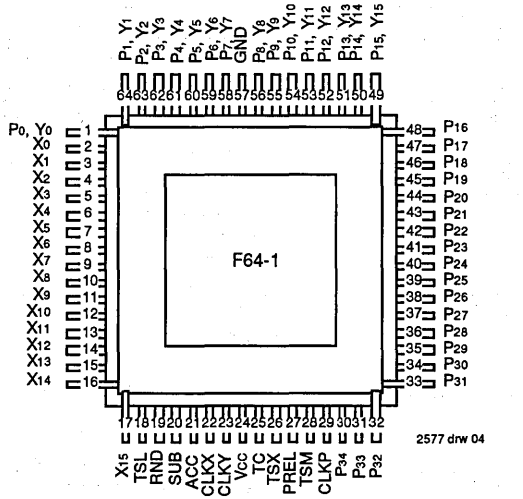
DIP
TOP VIEW

2577 drw 02



2577 drw 03

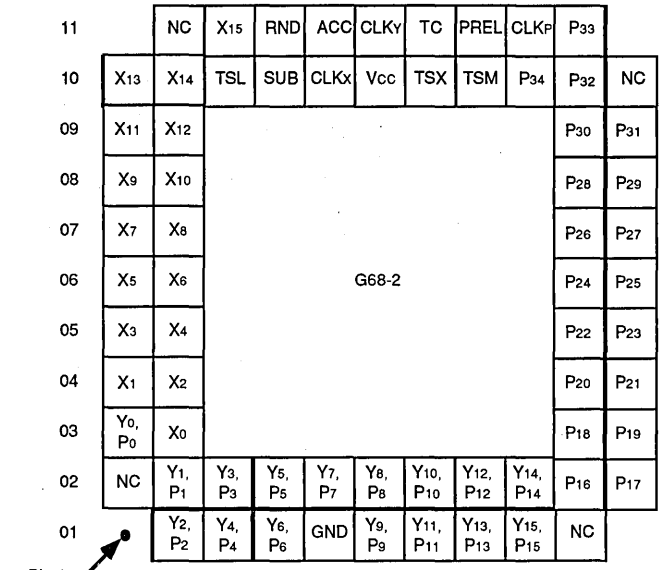
PLCC
TOP VIEW



2577 drw 04

FLATPACK
TOP VIEW

8



PIN DESCRIPTIONS

Pin Name	I/O	Description
X_{0-15}	I	Data Inputs
Y_{0-15}/ P_{0-15}	I/O	Multiplexed I/O port. Y_{0-15} are data inputs and can be used to preload LSP register on PREL = 1. P_{0-15} are LSP register outputs - enabled by TSL.
P_{16-32}	I/O	MSP register outputs - enabled by TSM. MSP register can be preloaded when PREL = 1.
P_{33-35}	I/O	XTP register outputs - enabled by TSX. XTP register can be preloaded through these inputs when PREL = 1.
CLKX	I	Input data X_{0-15} loaded in X input register on CLKX rising edge.
CLKY	I	Input data Y_{0-15} loaded in Y input register on CLKY rising edge.
CLKP	I	Output data loaded into output register on rising edge of CLKP.
TSX	I	TSX = 1 enables XTP outputs, TSX = 0 tristates P_{33-35} lines.
TSM	I	TSM = 1 enables MSP outputs, TSM = 0 tristates P_{16-32} lines.
TSL	I	TSL = 1 enables LSP outputs, TSL = 0 tristates P_{0-15} lines.
PREL	I	When PREL= 1 data is input on P_{0-15} lines. When PREL = 0, inputs on these lines are ignored.
ACC	I	This input is loaded into the control register on the rising edge of (CLKX + CLKY). When ACC = 1 and SUB = 0 an accumulate operation is performed. When ACC = 1 and SUB = 1, a subtract operation is performed. When ACC = 0, the SUB input is a don't care and the device acts as a simple multipler with no accumulation
SUB	I	This input is loaded into the control register on the rising edge of (CLKX + CLKY). This input is active only when ACC = 1. When SUB = 1 the contents of the output register are subtracted from the result and stored back in the output register. When SUB = 0 the contents of the output register are added to the result and stored back in the output register
TC	I	This input is loaded into the control register on the rising edge of (CLKX + CLKY). When TC = 1, the X and Y input are assumed to be in two's complement form. When TC = 0, X and Y inputs are assumed to be in unsigned magnitude form
RND	I	This input is loaded into the control register on the rising edge of (CLKX + CLKY). RND is inactive when low. RND = 1, adds a "1" to the most significant bit of the LSP, to round MSP and XTP data

2577 tbl 01

PRELOAD TRUTH TABLE

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Hi Z
0	0	1	0	Q	Hi Z	Q
0	0	1	1	Q	Hi Z	Hi Z
0	1	0	0	Hi Z	Q	Q
0	1	0	1	Hi Z	Q	Hi Z
0	1	1	0	Hi Z	Hi Z	Q
0	1	1	1	Hi Z	Hi Z	Hi Z
1	0	0	0	Hi Z	Hi Z	Hi Z
1	0	0	1	Hi Z	Hi Z	PL
1	0	1	0	Hi Z	PL	Hi Z
1	0	1	1	Hi Z	PL	PL
1	1	0	0	PL	Hi Z	Hi Z
1	1	0	1	PL	Hi Z	PL
1	1	1	0	PL	PL	Hi Z
1	1	1	1	PL	PL	PL

NOTES: 2577 tbl 02

Hi Z = Output buffers at high impedance (output disabled)
Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.
PL = Output buffers at high impedance or output disabled. Preload data supplied externally at output pins will be loaded into the output register at the rising edge of CLKP.

NOTES ON TWO'S COMPLEMENT FORMATS

1. In two's complement notation, the location of the binary point that signifies the separation of the fractional and integer fileds is just after the sign, between the sign bit (-2^0) and the next significant bit for the multiplier inputs. This same format is carried over to the output format, except that the extended significance of the integer filed is provided to extend the utility of the accumulator. In the case of the output rotation, the output binary point is located between the2^0 and 2^1 bit positions. The location of the binary point is arbitrary, as long as there is consistency with both the input and output formats. The number filed can be considered entirely integer with the binary point just to the right of the least significant bit for the input, product and the accumulated sum.
2. When in the non-accumulating mode, the first four bits (P_{34} to P_{31}) will all indicate the sign of the product. Additionally, the P_{30} term will also indicate the sign with one exception, when multiplying -1 x -1. With the additional bits that are available in this multiplier, the -1×-1 is a valid operation that yields a +1 product.
3. In operations that require the accumulation of single products or sum of products, there is no change in format. To allow for a valid summation beyond that available for a single multiplication product, three additional significant bits (guard bits) are provided. This is the same as if the product was accumulated off-chip in a separate 35-bit wide adder. Taking the sign at the most significant bit position will guarantee that the largest number field will be used. When the accumulated sum only occupies the right hand portion of the accumulator, the sign will be extended into the lesser significant bit positions.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{CC}	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to V_{CC} +0.5V	−0.5 to V_{CC} +0.5V	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2577 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2577 tbl 04

1. This parameter is measured at characterization and not 100%tested.

8

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C TO +125°C)

Symbol	Parameter	Test Conditions[5]	Commercial			Military			Unit
			Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.	
V_{IH}	Input High Voltage	Guaranteed Logic HIGH Level	2.0	—	—	2.0	—	—	V
V_{IL}	Input Low Voltage	Guaranteed Logic LOW Level	—	—	0.8	—	—	0.8	V
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0V to V_{CC}	—	—	10	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., Outputs Disabled V_{OUT} = 0 to V_{CC}	—	—	10	—	—	10	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0mA	2.4	—	—	2.4	—	—	V
V_{OL}[4]	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	—	0.4	—	—	0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_O GND	-20	—	-100	-20	—	-100	mA
I_{CC}[2]	Operating Power Supply Current	V_{CC} = Max., Outputs Enabled f= 10MHz[2] C_L = 50 pF	—	45	90	—	45	110	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	20	30	—	20	30	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$–0.2V, $V_{IN} \leq$ 0.2V	—	4	10	—	4	12	mA
I_{CC}/f[2,3]	Increase in Power Supply Current MHz	V_{CC} = Max., Outputs Enabled C_L = 50 pF	—	—	6	—	—	8	mA/ MHz

NOTES:
2577 tbl 05

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = 0 to 3V. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 90+ 6(f –10)mA, where f = operating frequency in MHz. For the military range, I_{CC} = 110 + 8(f –10). f = operating frequency in MHz, f = 1/t_{MA}.
3. For frequencies greater than 10MHz, guaranteed by design, not production tested.
4. I_{OL} = 4mA for t_{MA} > 55ns.
5. For conditions shown as Max. or Min., use appropriate value specified under electrical characteristics.

AC ELECTRICAL CHARACTERISTICS COMMERCIAL (V_{CC} = 5V ± 10%, T_A = 0° to +70°C)

Symbol	Parameter	7210L25		7210L35		7210L45		7210L55		7210L65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{MA}	Multiply-Accumulate Time[2]	2.0	25	2.0	35	2.0	45	2.0	55	2.0	65	ns
t_D	Output Delay[2]	2.0	20	2.0	25	2.0	25	2.0	30	2.0	35	ns
t_{ENA}	3-State Enable Time	–	20	–	25	–	25	–	30	–	30	ns
t_{DIS}	3-State Disable Time[1]	–	20	–	25	–	25	–	30	–	30	ns
t_S	Input Register Set-up Time	12	–	12	–	15	–	20	–	25	–	ns
t_H	Input Register Hold Time	3	–	3	–	3	–	3	–	3	–	ns
t_{PW}	Clock Pulse Width	10	–	10	–	15	–	20	–	25	–	ns
t_{HCL}	Relative Hold Time	0	–	0	–	0	–	0	–	0	–	ns

NOTES:
2577 tbl 06

1. Transition is measured ±500mV from steady state voltage.
2. Minimum delays guaranteed but not tested

AC ELECTRICAL CHARACTERISTICS MILITARY (V_{CC} = 5V ± 10%, T_A = –55° to +125°C)

Symbol	Parameter	7210L30		7210L40		7210L55		7210L65		7210L75		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{MA}	Multiply-Accumulate Time[2]	2.0	30	2.0	40	2.0	55	2.0	65	2.0	75	ns
t_D	Output Delay[2]	2.0	20	2.0	25	2.0	30	2.0	35	2.0	35	ns
t_{ENA}	3-State Enable Time	–	20	–	25	–	30	–	30	–	35	ns
t_{DIS}	3-State Disable Time[1]	–	20	–	25	–	25	–	30	–	30	ns
t_S	Input Register Set-up Time	12	–	15	–	20	–	25	–	25	–	ns
t_H	Input Register Hold Time	3	–	3	–	3	–	3	–	3	–	ns
t_{PW}	Clock Pulse Width	10	–	15	–	20	–	25	–	25	–	ns
t_{HCL}	Relative Hold Time	0	–	0	–	0	–	0	–	0	–	ns

NOTES:
2577 tbl 07

1. Transition is measured ±500mV from steady state voltage.
2. Minimum delays guaranteed but not tested

SWITCH POSITION

Test	Switch
Disable Low Enable Low	Closed
All Other Tests	Open

2577 tbl 09

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2577 tbl 08

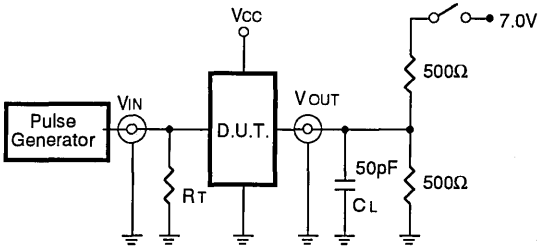


Figure 1. AC Test Load Circuit

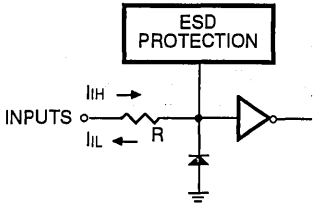


Figure 2. Input Interface Circuit

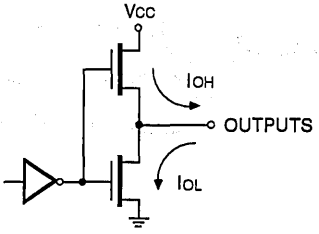


Figure 3. Output Interface Circuit

8

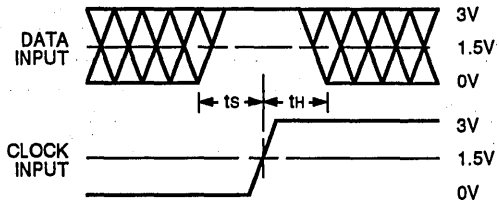


Figure 8. Set-Up and Hold Time

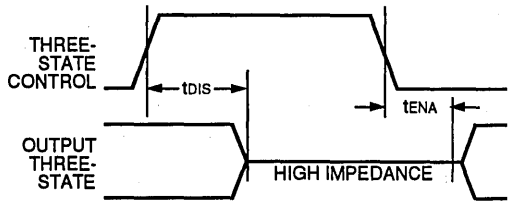


Figure 9. Three-State Control Timing Diagram

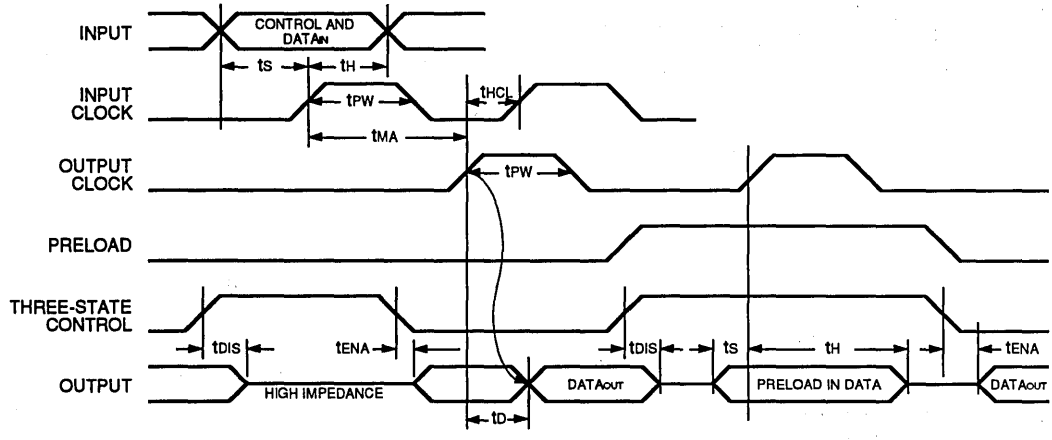


Figure 10. Timing Diagram

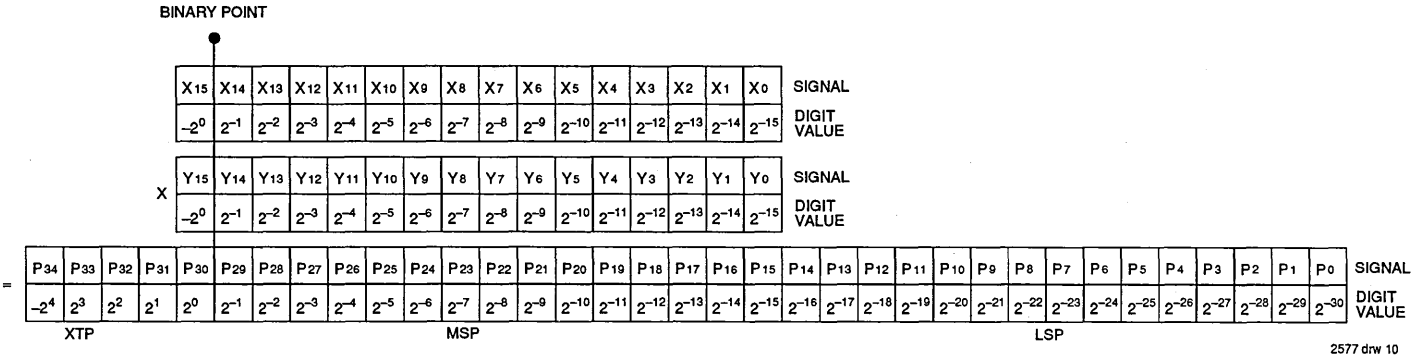


Figure 4. Fractional Two's Complement Notation.

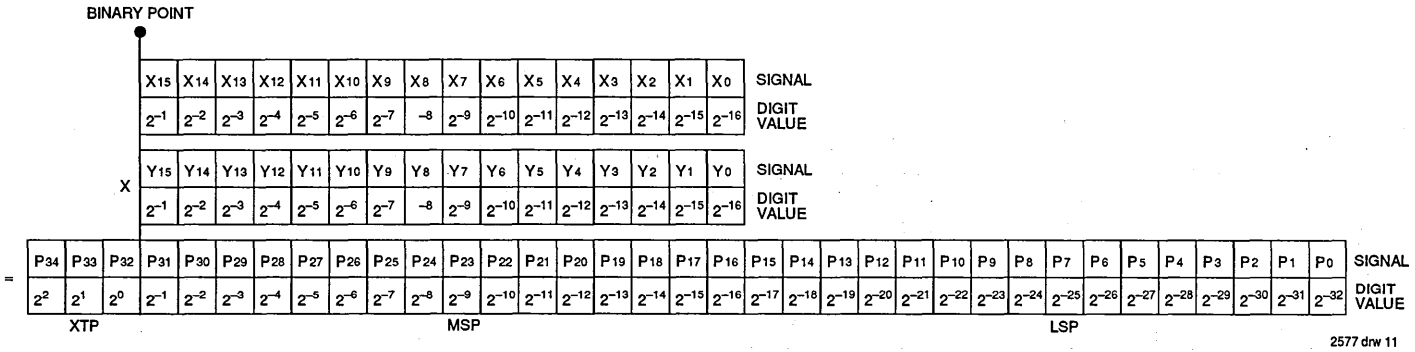


Figure 5. Fractional Unsigned Magnitude Notation

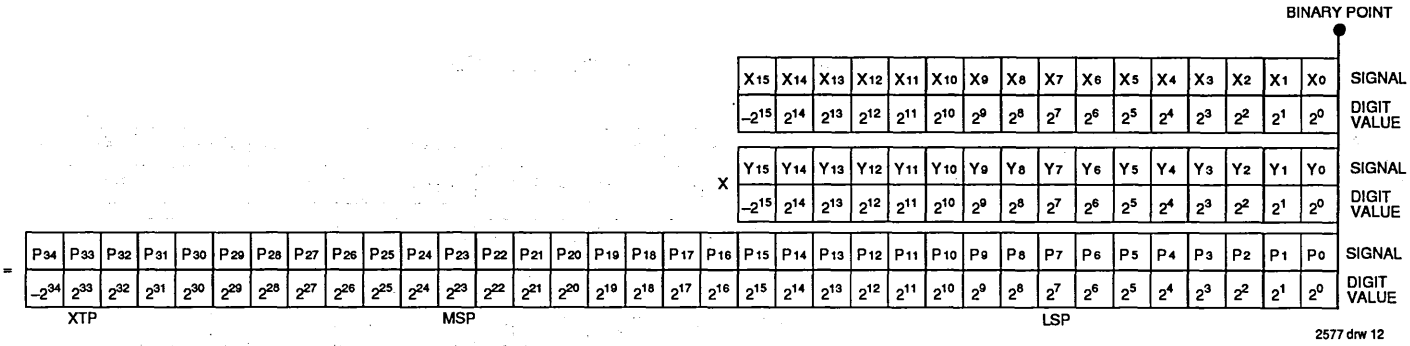


Figure 6. Integer Two's Complement Notation

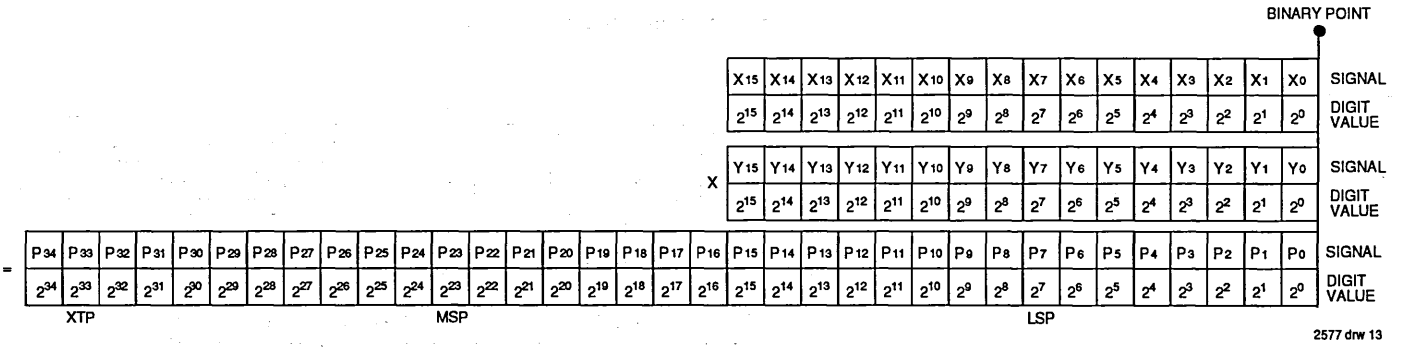


Figure 7. Integer Unsigned Magnitude Notation

Integrated Device Technology, Inc.

16 x 16 PARALLEL CMOS MULTIPLIERS

IDT7216L
IDT7217L

FEATURES:

- 16 x 16 parallel multiplier with double precision product
- 20ns clocked multiply time
- Low power consumption: 120mA
- Produced with advanced submicron CEMOS™ high performance technology
- IDT7216L is pin- and function compatible with TRW MPY016H/K and AMD Am29516
- IDT7217L requires a single clock with register enables making it pin- and function compatible with AMD Am29517
- Configured for easy array expansion
- User-controlled option for transparent output register mode
- Round control for rounding the MSP
- Input and output directly TTL-compatible
- Three-state output
- Available in plastic and Top Braze, DIP, PLCC, Flatpack and Pin Grid Array
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-86873 is listed on this function for IDT7216 and Standard Military Drawing #5962-87686 is listed for this function for IDT7217.
- Speeds available: Commercial: L20/25/35/45/55/65
  Military: L25/30/40/55/65/75

DESCRIPTION:

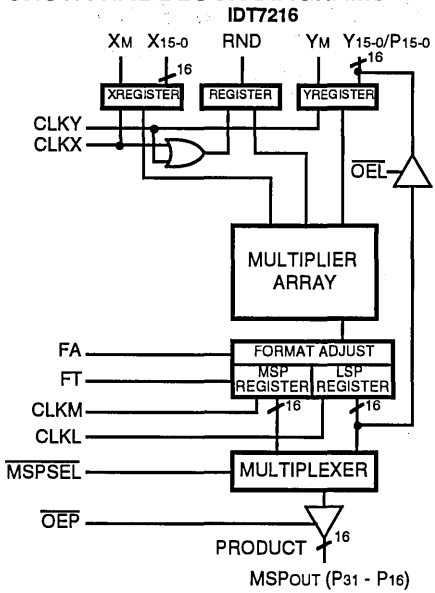
The IDT7216/IDT7217 are high-speed, low-power 16 x 16-bit multipliers ideal for fast, real time digital signal processing applications. Utilization of a modified Booths algorithm and IDT's high-performance, submicron CEMOS technology, has achieved speeds comparable to bipolar (20ns max.), at 1/10 the power consumption.

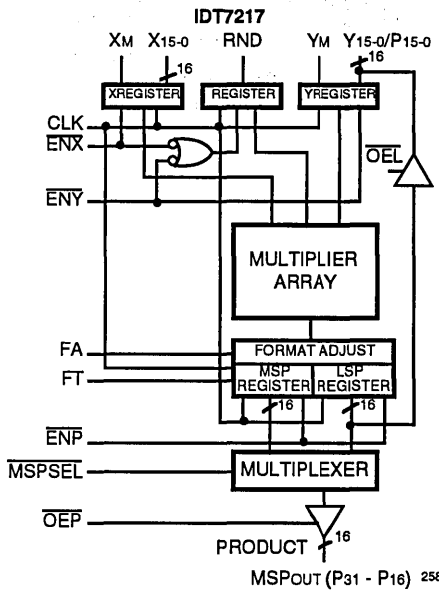
The IDT7216/IDT7217 are ideal for applications requiring high-speed multiplication such as fast Fourier transform analysis, digital filtering, graphic display systems, speech synthesis and recognition and in any system requirement where multiplication speeds of a mini/microcomputer are inadequate.

All input registers, as well as LSP and MSP output registers, use the same positive edge-triggered D-type flip-flop. In the IDT7216, there are independent clocks (CLKX, CLKY, CLKM, CLKL) associated with each of these registers. The IDT7217 has only a single clock input (CLK) and three register enables. $\overline{ENX}$ and $\overline{ENY}$ control the two input registers, while $\overline{ENP}$ controls the entire product.

The IDT7216/IDT7217 offer additional flexibility with the FA control and $\overline{MSPSEL}$ functions. The FA control formats the output for two's complement by shifting the MSP up one bit and then repeating the sign bit in the MSB of the LSP. The

FUNCTIONAL BLOCK DIAGRAMS





CEMOS is a trademark of Integrated Device Technology, Inc.

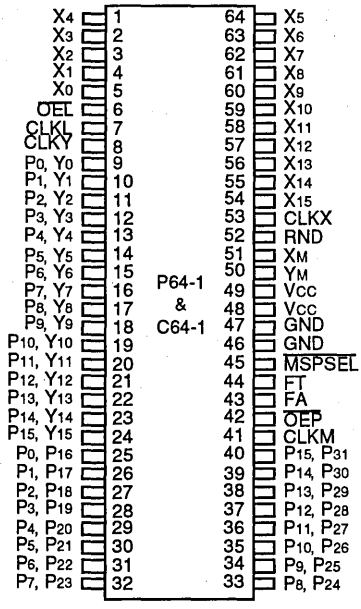
DESCRIPTION (Cont'd.)

$\overline{MSPSEL}$ low selects the MSP to be available at the product output port, while a high selects the LSP to be available. Keeping this pin low will ensure compatibility with the TRW MPY016H.

The IDT7216/IDT7217 multipliers are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS

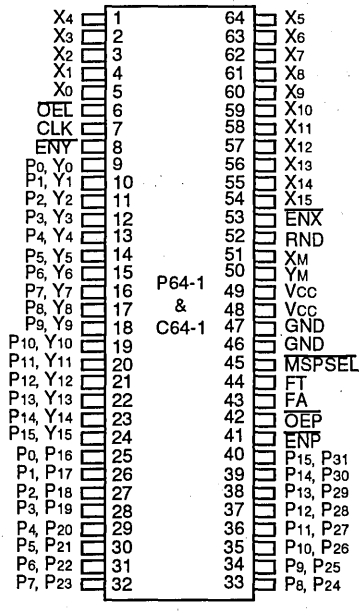
IDT7216



2580 drw 03

64-PIN DIP
TOP VIEW

IDT7217

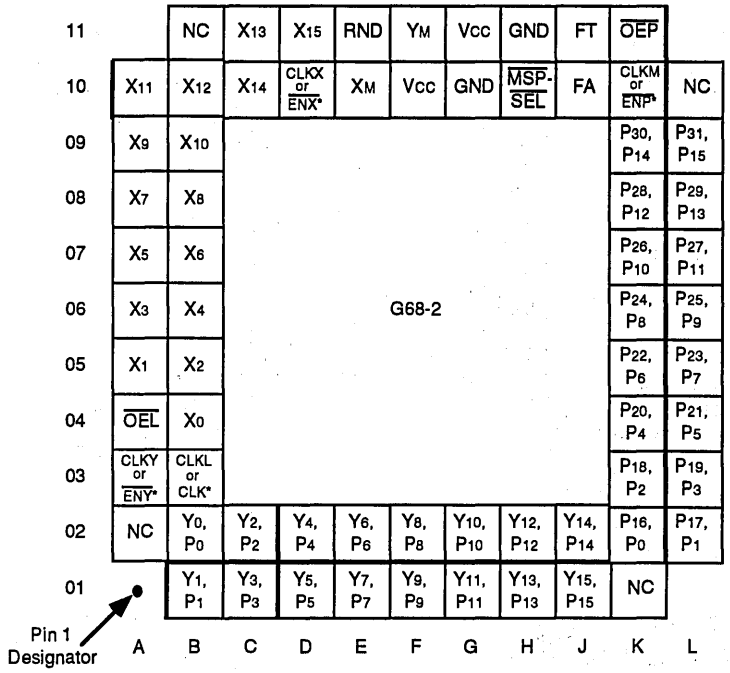


2580 drw 04

64-PIN DIP
TOP VIEW

PIN CONFIGURATIONS (Cont'd.)

IDT7216/IDT7217



*Pin designation for IDT7217

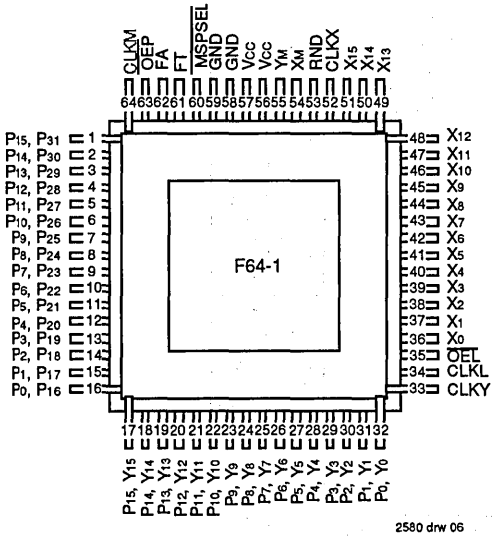
2580 drw 05

PGA
TOP VIEW

8

PIN CONFIGURATIONS (Cont'd.)

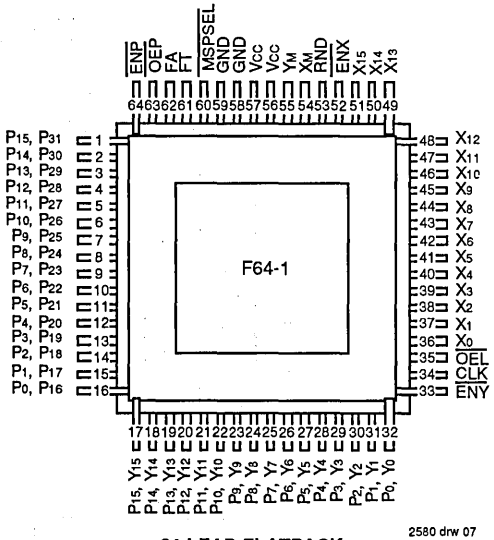
IDT7216



2580 drw 06

64-LEAD FLATPACK
TOP VIEW

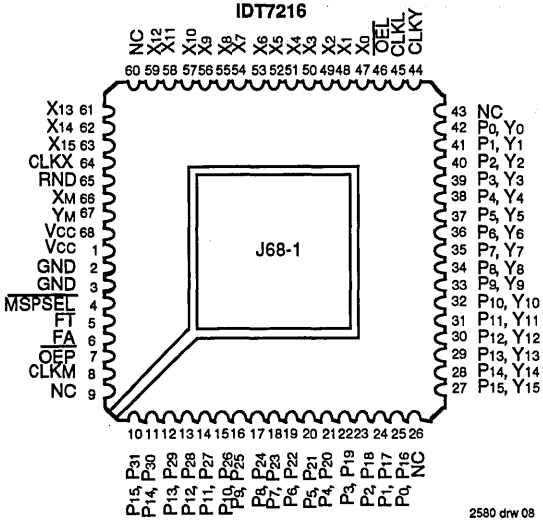
IDT7217



2580 drw 07

64-LEAD FLATPACK
TOP VIEW

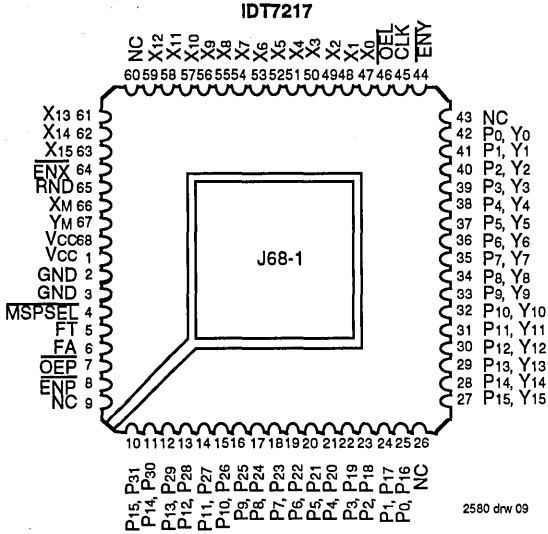
IDT7216



2580 drw 08

PLCC
TOP VIEW

IDT7217



2580 drw 09

PLCC
TOP VIEW

PIN DESCRIPTIONS

Pin Name	I/O	Description
X_0 - X_{15}	I	Data Inputs
Y_0 - Y_{15}/ P_0 - P_{15}	I/O	Y_0 - Y_{15} are data inputs P_0 - P_{15} are LSP register output, enabled when $\overline{OEL}$ = 0
P_{16} - P_{31}	O	Data Output (LSP or MSP)
$\overline{OEL}$	I	Output enable control for LSP (least significant product). When low enables P_0 - P_{15}. When high P_0 - P_{15} tristated.
$\overline{OEP}$	I	Output enable control for MSP (most significant product). When low enables P_{16} - P_{31}. When high P_{16} - P_{31} tristated.
X_M, Y_M	I	Mode control for each data word. Low designates unsigned data input and high designates two's complement.
RND	I	"Round" control for rounding of MSP. When high, 1 is added to the most significant bit of LSP. This signal is affected by the state of FA pin. When FA = 1 and RND = 1, 1 is added to the 2^{-15} bit (P_{15}). When RND = 1 and FA = 0, 1 is added to the 2^{-16} bit (P_{14}). The RND input is registered. It is clocked on the rising edge of the logical OR of CLKX and CLKY in the 7216 and on the rising edge of CLK in the 7217. Rounding always occurs in the positive direction which may introduce a systematic bias.
$\overline{MSPSEL}$	I	When low, MSP is output on P_{16} - P_{31} lines. When high, LSP is output on P_{16} - P_{31}.
FA	I	Format adjust control. When high, a full 32 bit product is selected. When low, a left shifted 31 bit product is selected with the sign bit replicated in the LSP. FA is normally high, except for certain fractional two's complement applications (see multiplier input / output formats).
$\overline{FT}$	I	Flow through control. When high, both MSP and LSP registers are by-passed.
CLK	I	7217 X, Y, RND, LSP and MSP register clock input.
CLKX	I	7216 X register clock input. Also clocks RND register.
CLKY	I	7216 Y register clock input. Also clocks RND register.
CLKL	I	7216 LSP register clock input.
CLKM	I	7216 MSP register clock input.
$\overline{ENX}$	I	7217 X register clock enable. Also enables RND register clock.
$\overline{ENY}$	I	7217 Y register clock enable. Also enables RND register clock.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{CC}	Power Supply Voltage	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to GND	V_{CC} + 0.5	V_{CC} + 0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2580 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2580 tbl 04

1. This parameter is measured at characterization and not tested.

8

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

Symbol	Parameter	Test Conditions[1]	Commercial			Military			Unit
			Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.	
V_{IH}	Input High Voltage	Guaranteed Logic High Level	2.0	—	—	2.0	—	—	V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level	—	—	0.8	—	—	0.8	V
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	10	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{OE}$ = 2.0V V_{OUT} = 0 to V_{CC}	—	—	10	—	—	10	µA
I_{CC}	Operating Power Supply Current	V_{CC} = Max., Outputs Disabled f = 10MHz[2]	—	40	80	—	40	100	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	20	40	—	20	50	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC} - 0.2V$, $V_{IN} \leq 0.2V$	—	4	20	—	4	25	mA
I_{CC}/f[2,3]	Increase in Power Supply Current	V_{CC} = Max., Outputs Disabled	—	—	4	—	—	6	mA/MHz
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0mA	2.4	—	—	2.4	—	—	V
V_{OL}[4]	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_O = GND	-20	—	-120	-20	—	-120	mA

2580 tbl 03

NOTES:

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = 0 to 3V. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 80+ 4(f –10)mA; for the military range, I_{CC} = 100 + 6(f –10). f = operating frequency in MHz, f = 1/t_{MUC} for IDT7216 and f = 1/t_{MC} for IDT7217.
3. For frequencies greater than 10MHz, guaranteed by design, not production tested.
4. I_{OL} = 4mA for t_{MC} >65ns.

AC ELECTRICAL CHARACTERISTICS COMMERCIAL (V_{CC} = 5V ± 10%, T_A = 0° to +70°C)

Symbol	Parameter	7216L20 7217L20		7216L25 7217L25		7216L35 7217L35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{MUC}	Unclocked Multiply Time[4]	2	30	2	38	2	55	ns
t_{MC}	Clocked Multiply Time[4]	2	20	2	25	2	35	ns
t_S	X, Y, RND Set-up Time	11	—	12	—	12	—	ns
t_H	X, Y, RND Hold Time	1	—	2	—	3	—	ns
t_{PWH}	Clock Pulse Width High	9	—	10	—	10	—	ns
t_{PWL}	Clock Pulse Width Low	9	—	10	—	10	—	ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out[4]	2	18	2	20	2	25	ns
t_{PDP}	Output Clock to P[4]	2	18	2	20	2	25	ns
t_{PDY}	Output Clock to Y[4]	2	18	2	20	2	25	ns
t_{ENA}	3-State Enable Time	—	18	—	20	—	25	ns
t_{DIS}	3-State Enable Time[2]	—	18	—	20	—	22	ns
t_S	Clock Enable Set-up Time (IDT7217 only)	10	—	10	—	10	—	ns
t_H	Clock Enable Hold Time (IDT7217 only)	0	—	2	—	3	—	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (IDT7216 only)[1,3]	0	—	0	—	0	—	ns

Symbol	Parameter	7216L45 7217L45		7216L55 7217L55		7216L65 7217L65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{MUC}	Unclocked Multiply Time[4]	2	65	2	75	2	85	ns
t_{MC}	Clocked Multiply Time[4]	2	45	2	55	2	65	ns
t_S	X, Y, RND Set-up Time	15	—	20	—	20	—	ns
t_H	X, Y, RND Hold Time	3	—	3	—	3	—	ns
t_{PWH}	Clock Pulse Width High	15	—	15	—	15	—	ns
t_{PWL}	Clock Pulse Width Low	15	—	20	—	20	—	ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out[4]	2	25	2	25	2	30	ns
t_{PDP}	Output Clock to P[4]	2	25	2	30	2	30	ns
t_{PDY}	Output Clock to Y[4]	2	25	2	30	2	30	ns
t_{ENA}	3-State Enable Time	—	25	—	30	—	35	ns
t_{DIS}	3-State Enable Time[2]	—	22	—	25	—	25	ns
t_S	Clock Enable Set-up Time (IDT7217 only)	10	—	10	—	10	—	ns
t_H	Clock Enable Hold Time (IDT7217 only)	3	—	3	—	3	—	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (IDT7216 only)[1,3]	0	—	0	—	0	—	ns

NOTES:

2580 tbl 06

1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured ±500mV from steady state voltage.
3. Guaranteed by design, not production tested.
4. Minimum propagation delay times are guaranteed, not production tested.

8

AC ELECTRICAL CHARACTERISTICS MILITARY (V_{CC} = 5V ± 10%, T_A = −55° to +125°C)

Symbol	Parameter	7216L25 7217L25		7216L30 7217L30		7216L40 7217L40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{MUC}	Unclocked Multiply Time[4]	2	38	2	43	2	60	ns
t_{MC}	Clocked Multiply Time[4]	2	25	2	30	2	40	ns
t_S	X, Y, RND Set-up Time	12	—	12	—	15	—	ns
t_H	X, Y, RND Hold Time	2	—	2	—	3	—	ns
t_{PWH}	Clock Pulse Width High	10	—	10	—	15	—	ns
t_{PWL}	Clock Pulse Width Low	10	—	10	—	15	—	ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out[4]	2	20	2	20	2	25	ns
t_{PDP}	Output Clock to P[4]	2	20	2	20	2	25	ns
t_{PDY}	Output Clock to Y[4]	2	20	2	20	2	25	ns
t_{ENA}	3-State Enable Time	—	20	—	20	—	25	ns
t_{DIS}	3-State Enable Time[2]	—	22	—	22	—	25	ns
t_S	Clock Enable Set-up Time (IDT7217 only)	10	—	10	—	12	—	ns
t_H	Clock Enable Hold Time (IDT7217 only)	2	—	2	—	3	—	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (IDT7216 only)[1,3]	0	—	0	—	0	—	ns

Symbol	Parameter	7216L55 7217L55		7216L65 7217L65		7216L75 7217L75		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{MUC}	Unclocked Multiply Time[4]	2	75	2	85	2	95	ns
t_{MC}	Clocked Multiply Time[4]	2	55	2	65	2	75	ns
t_S	X, Y, RND Set-up Time	20	—	25	—	25	—	ns
t_H	X, Y, RND Hold Time	3	—	3	—	3	—	ns
t_{PWH}	Clock Pulse Width High	15	—	15	—	15	—	ns
t_{PWL}	Clock Pulse Width Low	15	—	15	—	15	—	ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out[4]	2	30	2	35	2	35	ns
t_{PDP}	Output Clock to P[4]	2	30	2	30	2	35	ns
t_{PDY}	Output Clock to Y[4]	2	30	2	30	2	35	ns
t_{ENA}	3-State Enable Time	—	25	—	35	—	40	ns
t_{DIS}	3-State Enable Time[2]	—	25	—	25	—	25	ns
t_S	Clock Enable Set-up Time (IDT7217 only)	15	—	15	—	15	—	ns
t_H	Clock Enable Hold Time (IDT7217 only)	3	—	3	—	3	—	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (IDT7216 only)[1,3]	0	—	0	—	0	—	ns

NOTES:

2580 tbl 07

1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured ±500mV from steady state voltage.
3. Guaranteed by design, not production tested.
4. Minimum propagation delay times are guaranteed, not production tested.

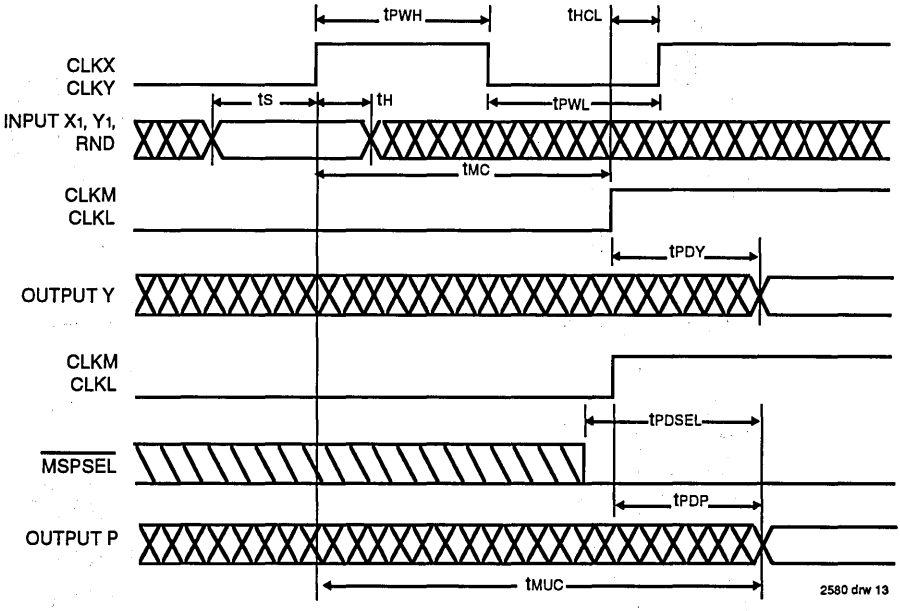


Figure 4. IDT7216 Timing Diagram

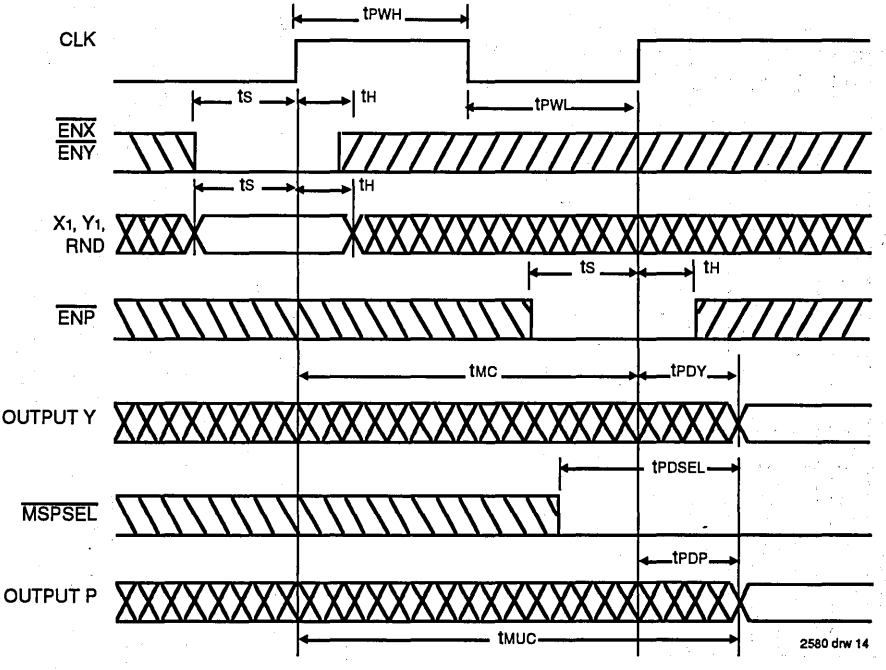


Figure 5. IDT7217 Timing Diagram

8

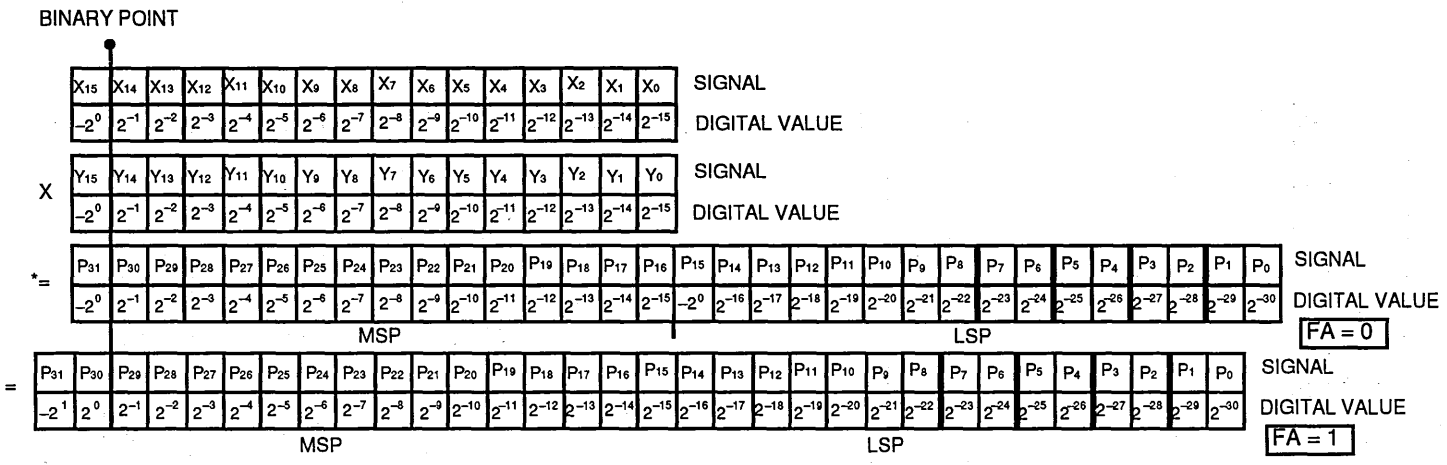


Figure 6. Fractional Two's Complement Notation

2580 drw 16

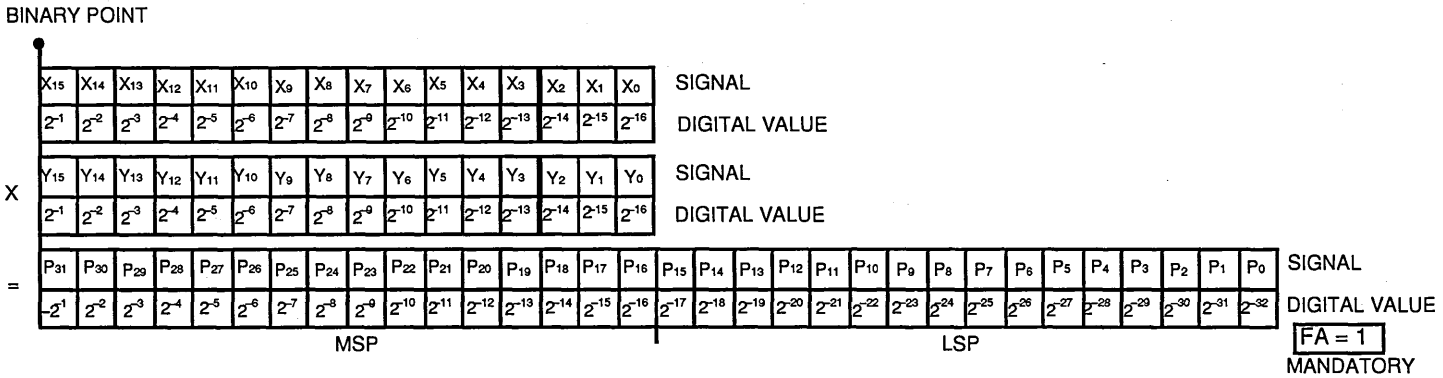


Figure 7. Fractional Unsigned Magnitude Notation

2580 drw17

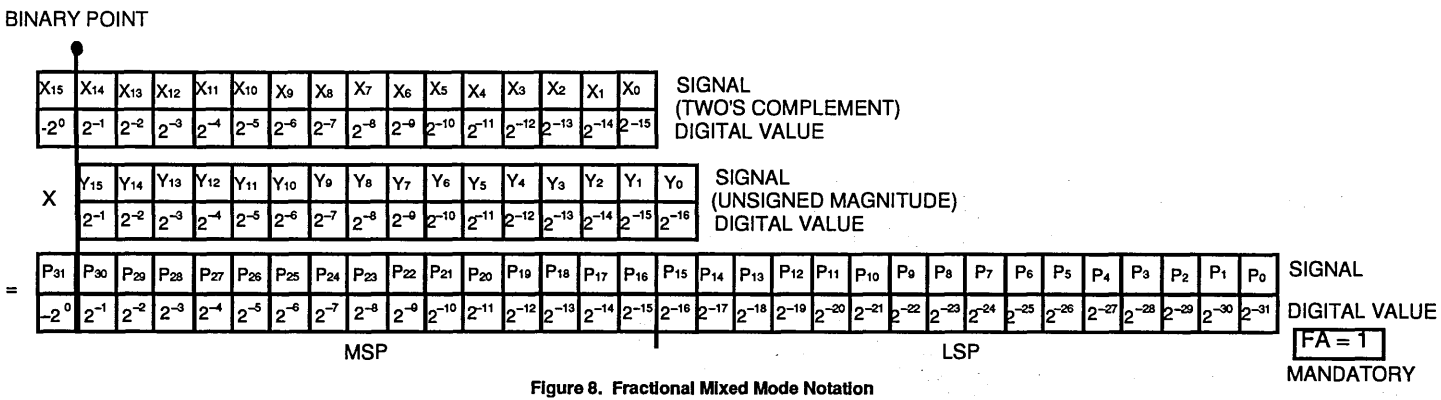


Figure 8. Fractional Mixed Mode Notation

2580 drw 18

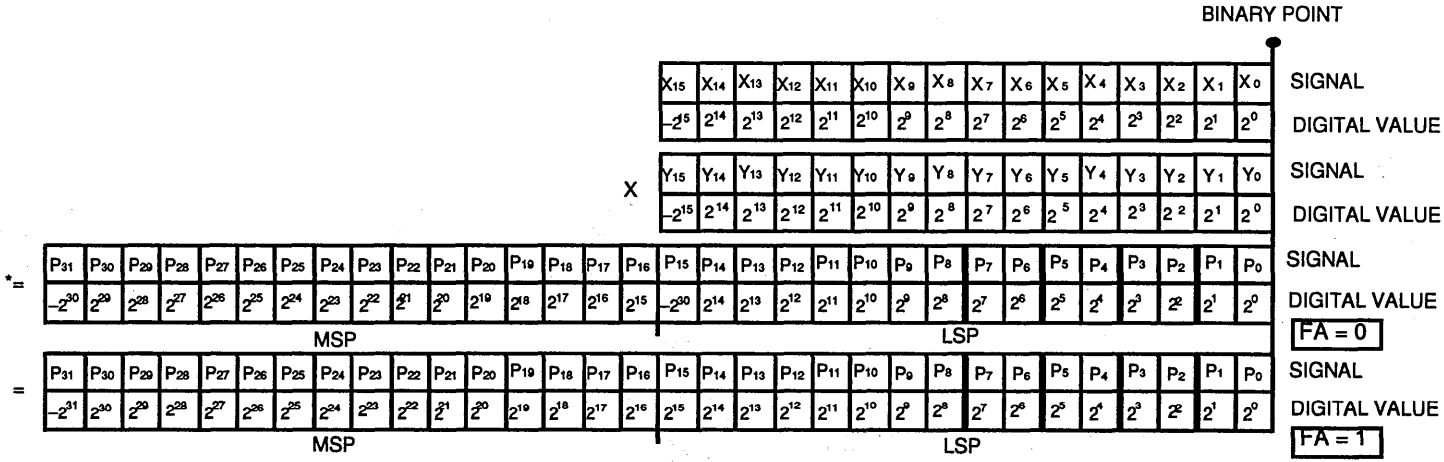


Figure 9. Integer Two's Complement Notation

2580 drw 19

* In this format an overflow occurs in the attempted multiplication of the two's complement number 1,000 . . . 0 with 1,000.0 yielding an erroneous product of –1 in the fraction case and -2^{30} in the integer case.

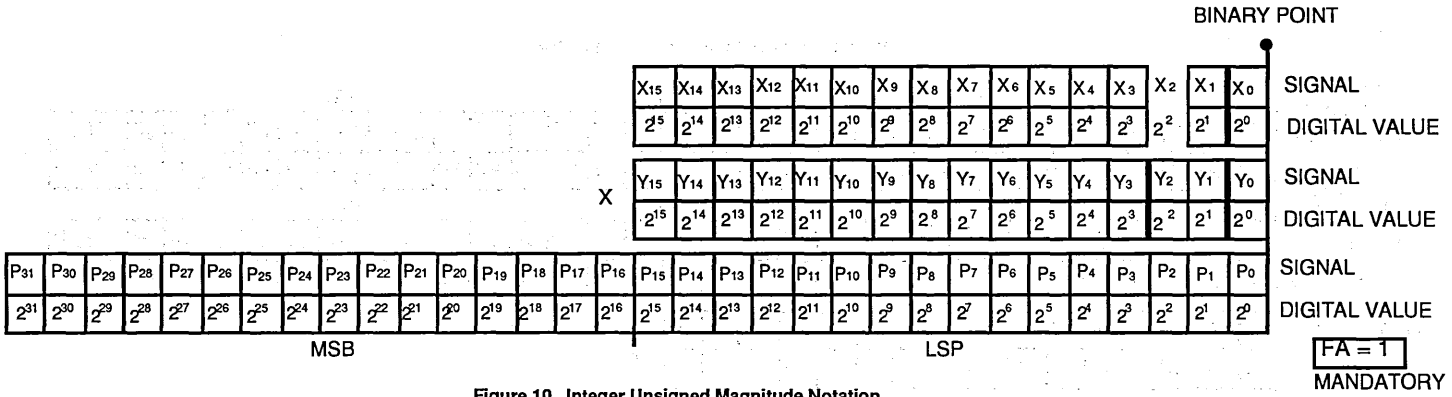


Figure 10. Integer Unsigned Magnitude Notation

2580 drw 20

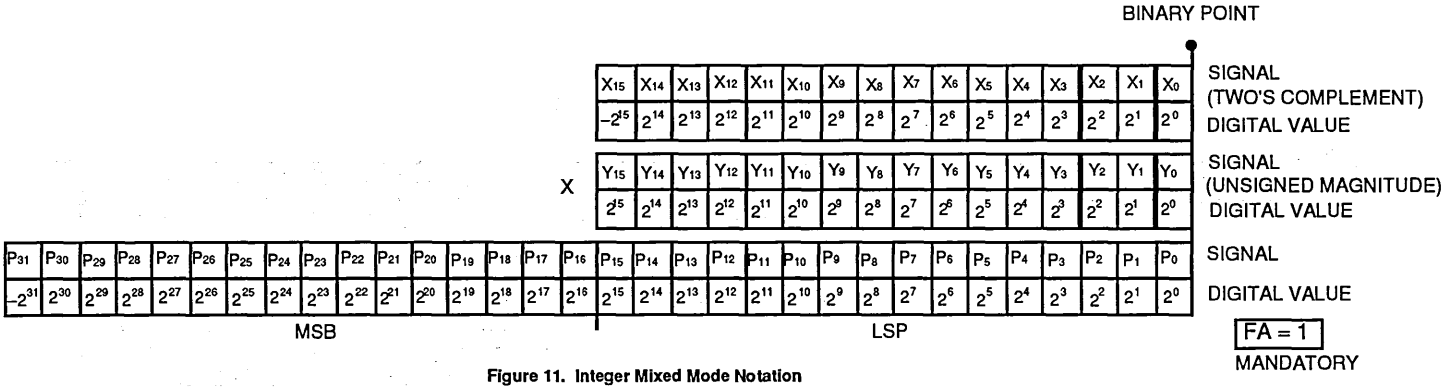


Figure 11. Integer Mixed Mode Notation

2580 drw 21

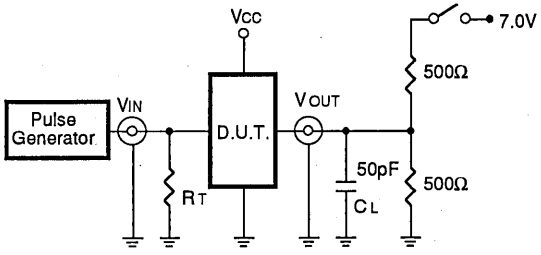


Figure 1. AC Test Load Circuit

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2580 tbl 08

SWITCH POSITION

Test	Switch
Disable Low Enable Low	Closed
All Other Tests	Open

2580 tbl 09

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

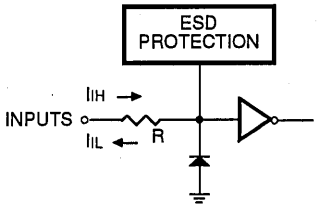


Figure 2. Input Interface Circuit

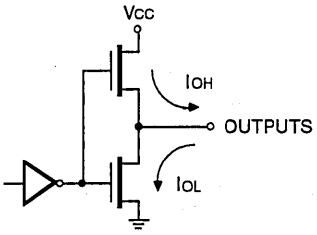


Figure 3. Output Interface Circuit

8

Integrated Device Technology, Inc.

16-BIT CMOS CASCADABLE ALU

IDT7381
IDT7383

FEATURES:

- High-performance 16-bit Arithmetic Logic Unit (ALU)
- 20ns to 55ns clocked ALU operations
- Ideal for radar, sonar or image processing applications
- IDT7381:
  - — 54/74S381 instruction set (8 functions)
  - — Replaces Gould S614381 or Logic Devices L4C381
  - — Cascadable with or without carry look-ahead
- IDT7383:
  - — 32 advanced ALU functions
  - — Cascadable without carry look-ahead
- Pipeline or flow-through modes
- Internal feedback path for accumulation
- Three-state outputs
- TTL-compatible
- Produced with advanced submicron CEMOS™ high-performance technology
- Available in 68-lead PGA, 68-pin surface mount PLCC and 68 pin fine-pitch Flatpack (7383 only)
- Military product compliant to MIL-STD-883, Class B
- Speeds available:
  Commercial: L20/25/30/40/55
  Military: L25/30/35/45/65

DESCRIPTION:

The IDT7381 and IDT7383 are high-speed cascadable Arithmetic Logic Unit (ALUs). Both three-bus devices have two input registers, ultra-fast 16-bit ALUs and 16-bit output registers. With IDT's high-performance CEMOS technology, the IDT7381/7383 can do arithmetic or logic operations in 20ns. The IDT7381 functionally replaces four 54/74S381 four-bit ALUs in a 68-pin package.

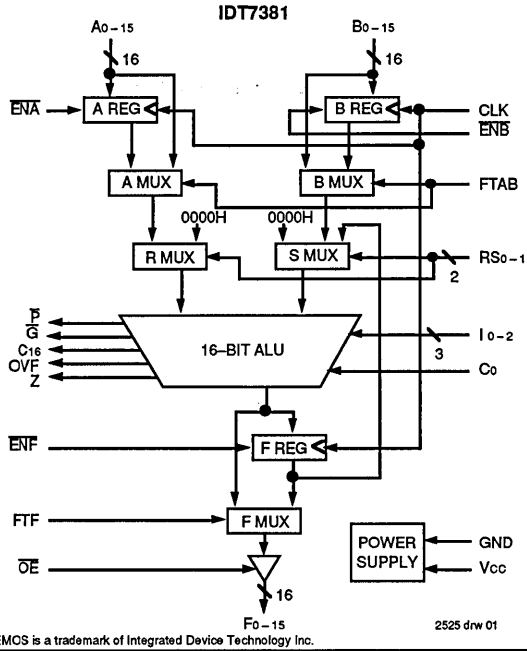
The two input operands, A and B, can be clocked or fed through for flexible pipelining. The F output can also be set into clocked or flow-through mode. An output enable is provided for three-state control of the output port on a bus.

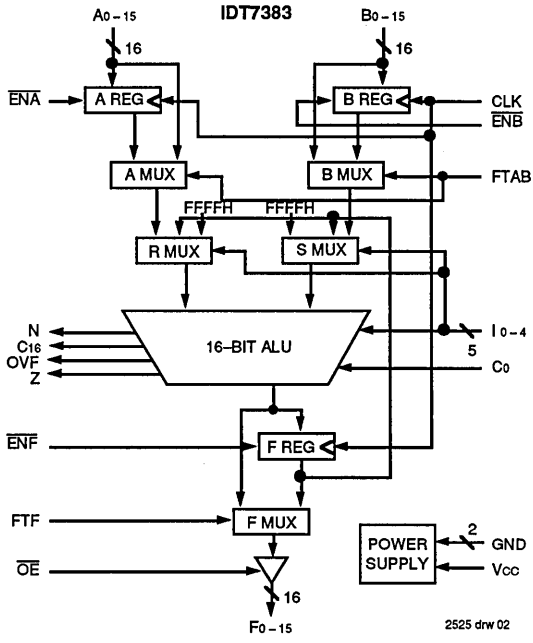
The IDT7381 has three function pins to select 1 of 8 arithmetic or logic operations. The two R and S selection pins determine whether A, B, F or 0 are fed into the ALU. This ALU has carry-out, propagate and generate outputs for cascading using carry look-ahead.

The IDT7383 has five function pins to select 1 of 32 arithmetic or logic operations. This ALU has a carry-out pin for cascading.

The IDT7381 and IDT7383 are available in 68-pin PLCC or PGA packages. Military grade product is manufactured in compliant with the latest revision of MIL-STD-883, Class B, for high reliability systems.

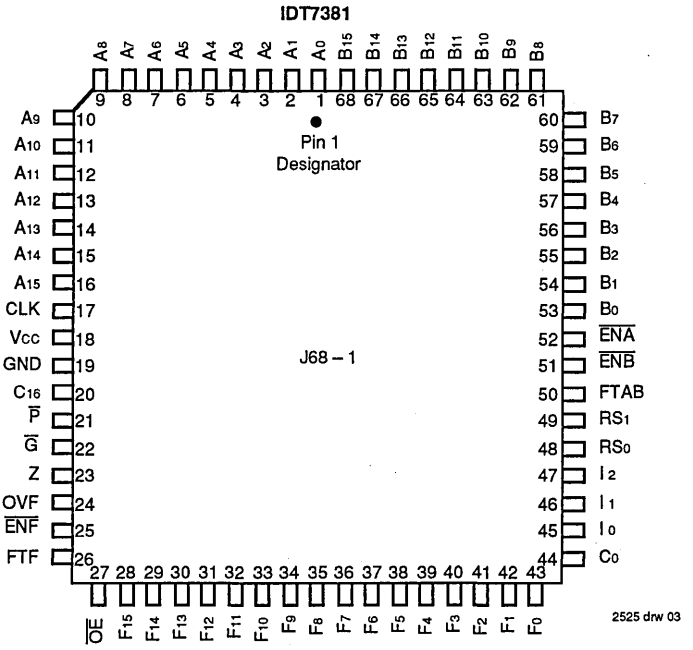
FUNCTIONAL BLOCK DIAGRAM



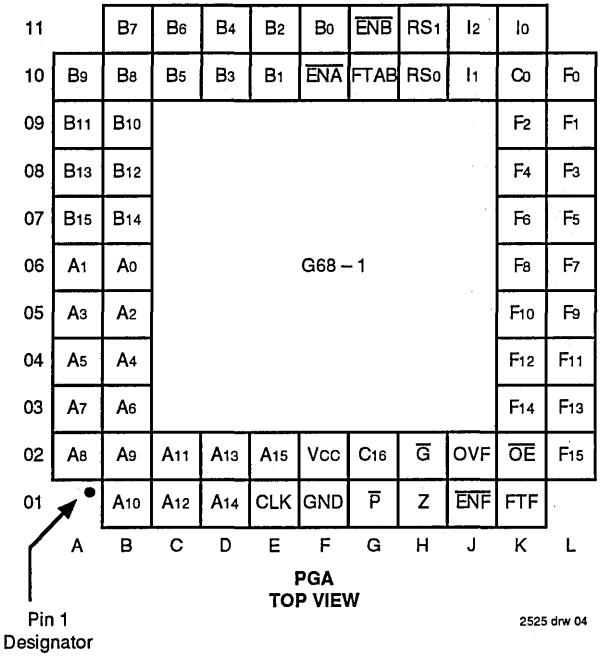


CEMOS is a trademark of Integrated Device Technology Inc.

PIN CONFIGURATION



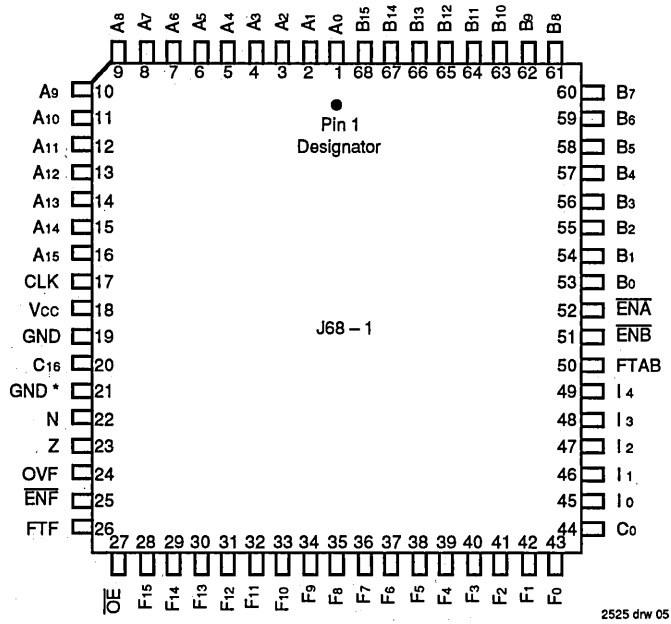
PLCC
TOP VIEW



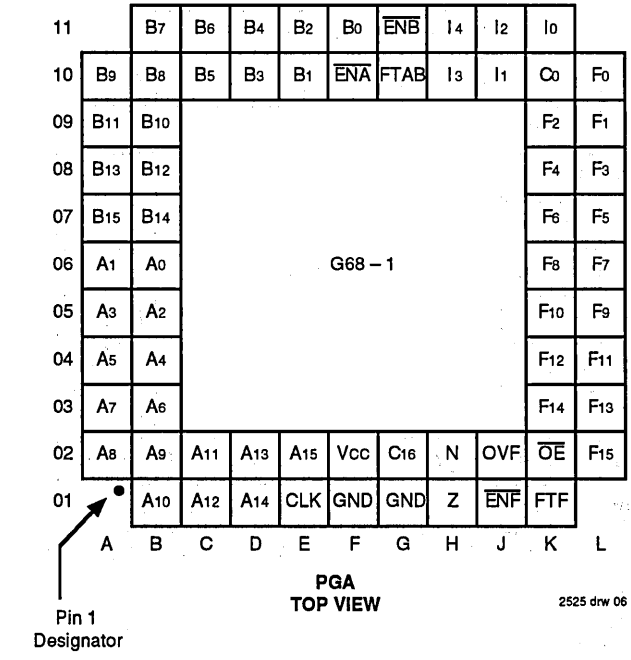
PGA
TOP VIEW

8

IDT7383

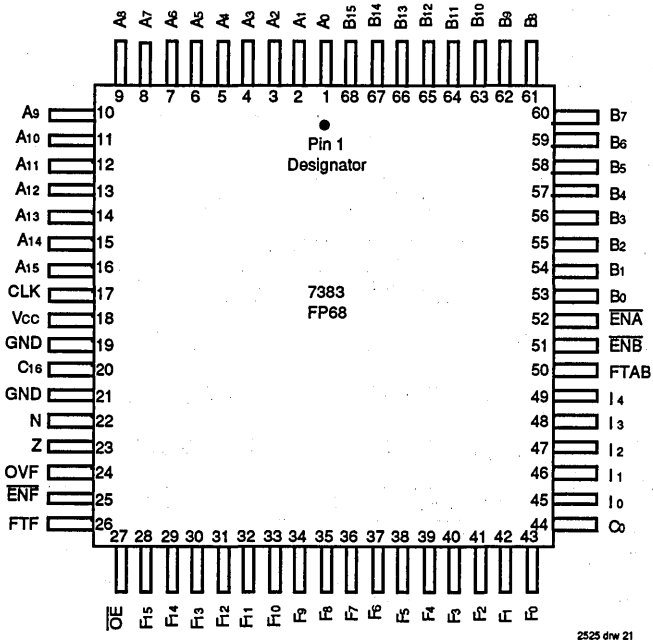


PLCC
TOP VIEW



PGA
TOP VIEW

IDT7383



FLATPACK
TOP VIEW

8

PIN DESCRIPTIONS

IDT7381 AND IDT7383 PIN DESCRIPTION

Pin Name	I/O	Description
A_0 - A_{15}	I	Sixteen–bit data input port.
B_0 - B_{15}	I	Sixteen–bit data input port.
$\overline{ENA}$	I	Register enable for the A input port; active low pin.
$\overline{ENB}$	I	Register enable for the B input port; active low pin.
FTAB	I	Flow–through control pin. When this pin is high, both register A and B are transparent.
F_0 – F_{15}	O	Sixteen–bit data output port.
$\overline{ENF}$	I	Register enable for the F output port; active low pin.
FTF	I	Flow–through control pin. When this pin is high, the F register is transparent.
CLK	I	Clock input.
$\overline{OE}$	I	Output enable control pin. When this pin is high, the output port F is in a high impedance state. When low, the output port F is active.
C_0	I	Carry input. This pin receives arithmetic carries from less significant ALU components in a cascade configuration.
C_{16}	O	Carry output. This pin produces arithmetic carries to more significant ALU components in a cascaded configuration.
OVF	O	This pin indicates a two's complement arithmetic overflow, when high.
Z	O	This pin indicates a zero output result, when high.
V_{CC}		Power supply pin, 5V.
GND		Ground pin, 0V. There are two ground pins on the IDT7383.

2525 tbl 01

IDT7381 PINS

Pin Name	I/O	Description
RS_0 – RS_1	I	Two control pins used to select input operands for the R and S multiplexers.
I_0 - I_2	I	Three control pins to select the ALU function performed.
$\overline{P}$	O	Indicates the carry propagate output state to the ALU.
$\overline{G}$	O	Indicates the carry generate output state to the ALU.

2525 tbl 02

IDT7383 PINS

Pin Name	I/O	Description
I_0 – I_4	I	Five control pins to select the ALU function performed.
N	O	The sign bit of an ALU operation.

2525 tbl 05

IDT7381 R AND S MUX TABLE

RS_1	RS_0	R Mux	S Mux
0	0	A	F
0	1	A	0
1	0	0	B
1	1	A	B

2525 tbl 03

IDT7381 ALU FUNCTION TABLE

I_2	I_1	I_0	Function
0	0	0	F = 0
0	0	1	$F = \overline{R} + S + C_0$
0	1	0	$F = R + \overline{S} + C_0$
0	1	1	$F = R + S + C_0$
1	0	0	F = R xor S
1	0	1	F = R or S
1	1	0	F = R and S
1	1	1	F = all 1's

2525 tbl 04

IDT7383 ALU FUNCTION TABLE

I_4	I_3	I_2	I_1	I_0	Function
0	0	0	0	0	F = A + B + Co
0	0	0	0	1	F = A or B
0	0	0	1	0	F = A + $\overline{B}$ + Co
0	0	0	1	1	F = $\overline{A}$ + B + Co
0	0	1	0	0	F = A + Co
0	0	1	0	1	F = $\overline{A}$ or F
0	0	1	1	0	F = A − 1 + Co
0	0	1	1	1	F = $\overline{A}$ + Co
0	1	0	0	0	F = A + F + Co
0	1	0	0	1	F = A or F
0	1	0	1	0	F = A + $\overline{F}$ + Co
0	1	0	1	1	F = $\overline{A}$ + F + Co
0	1	1	0	0	F = F + B + Co
0	1	1	0	1	F = $\overline{A}$ or B
0	1	1	1	0	F = F + $\overline{B}$ + Co
0	1	1	1	1	F = $\overline{F}$ + B + Co
1	0	0	0	0	F = A xor B
1	0	0	0	1	F = A and B
1	0	0	1	0	F = $\overline{A}$ and B
1	0	0	1	1	F = A xnor B
1	0	1	0	0	F = A xor F
1	0	1	0	1	F = A and F
1	0	1	1	0	F = $\overline{A}$ and F
1	0	1	1	1	F = all 1's + Co
1	1	0	0	0	F = B + Co
1	1	0	0	1	F = A and $\overline{B}$
1	1	0	1	0	F = $\overline{B}$ + Co
1	1	0	1	1	F = B − 1 + Co
1	1	1	0	0	F = F + Co
1	1	1	0	1	F = A or $\overline{B}$
1	1	1	1	0	F = F − 1 + Co
1	1	1	1	1	F = $\overline{F}$ + Co

2525 tbl 06

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to Ground	−0.5 to VCC + 0.5	−0.5 to VCC + 0.5	V
VCC	Power Supply Voltage	−0.5 to +7.0	−0.5 to +7.0	V
TA	Operating Temperature	0 to +70	−55 to +125	°C
TBIAS	Temperature Under Bias	−55 to +125	−65 to +135	°C
TSTG	Storage Temperature	−55 to +125	−65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE: 2525 tbl 07

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Under no circumstances should an input of an I/O Pin be greater than VCC + 0.5V.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	10	pF
COUT	Output Capacitance	VOUT = 0V	12	pF

NOTE: 2525 tbl 09

1. This parameter is sampled at initial characterization and is not production tested.

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DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.5V		—	—	–10	µA
I_{OS}[3]	Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		–20	—	–100	mA
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.5V	—	–0.1	–20	µA
			V_O = 2.7V	—	–0.1	20	
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –4mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4mA MIL.	—	—	0.5	V
			I_{OL} = 8mA COM'L.				

NOTES:

2525 tbl 08

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} =0V or V_{CC}	COM'L.	—	2	10	mA
			MIL.	—	2	15	
I_{CCQT}[3]	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V	COM'L.	—	0.5	2	mA
			MIL.	—	0.5	2.5	
I_{CCD1}	Dynamic Power Supply Current	Mode: FTAB = FTF = 1 V_{CC} = Max. Outputs Disabled f_i = 10MHz 50% Duty Cycle V_{IL} = 0V, V_{IH} = V_{CC}	COM'L.	—	10	35	mA
			MIL.	—	10	55	
I_{CCD2}	Dynamic Power Supply Current	Mode: FTAB = FTF = 1 V_{CC} = Max. Outputs Disabled f_i = 20MHz 50% Duty Cycle V_{IL} = 0V, V_{IH} = V_{CC}	COM'L.	—	30	60	mA
			MIL.	—	30	80	

NOTES:

2525 tbl 10

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

AC ELECTRICAL CHARACTERISTICS — COMMERCIAL (V_{CC} = 5V ± 5%, T_A = 0°C to +70°C)

Maximum Combinational Propagation Delays

From Input	IDT7381L20 IDT7383L20				IDT7381L25 IDT7383L25				IDT7381L30 IDT7383L30				Unit
	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	
FTAB = 0, FTF = 0													
CLK	11	20	20	20	13	22	26	22	20	28	30	28	ns
C_0	—	—	14	14	—	—	16	16	—	—	20	20	ns
I_{0-4}, RS_0, RS_1	—	18	20	18	—	22	22	22	—	28	28	28	ns
FTAB = 0, FTF = 1													
CLK	20	20	20	20	27	22	26	22	33	28	30	28	ns
C_0	18	—	14	14	22	—	16	16	28	—	20	20	ns
I_{0-4}, RS_0, RS_1 (1)	20	18	20	18	22	22	22	22	28	28	28	28	ns
FTAB = 1, FTF = 0													
A_0–A_{15}, B_0–B_{15}	—	16	20	17	—	18	25	22	—	24	30	28	ns
CLK	11	—	—	—	13	—	—	—	19	—	—	—	ns
C_0	—	—	14	14	—	—	16	16	—	—	20	20	ns
I_{0-4}, RS_0, RS_1 (1)	—	18	20	18	—	22	22	22	—	28	28	28	ns
FTAB = 1, FTF = 1													
A_0–A_{15}, B_0–B_{15}	20	16	20	17	26	18	25	22	32	24	30	28	ns
C_0	18	—	14	14	22	—	16	16	28	—	20	20	ns
I_{0-4}, RS_0, RS_1 (1)	20	18	20	18	22	22	22	22	28	28	28	28	ns

NOTE:
1. Minimum propagation delays are guaranteed to be greater than or equal to 3ns although not production tested.

2525 tb 11

Maximum Combinational Propagation Delays

From Input	IDT7381L40 IDT7383L40				IDT7381L55 IDT7383L55				Unit
	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z, OVF	C_{16}	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z, OVF	C_{16}	
FTAB = 0, FTF = 0									
CLK	26	30	44	32	32	38	53	36	ns
C_0	—	—	28	20	—	—	34	22	ns
I_{0-4}, RS_0, RS_1	—	32	34	35	—	42	42	42	ns
FTAB = 0, FTF = 1									
CLK	46	30	44	32	56	38	53	36	ns
C_0	30	—	28	20	37	—	34	22	ns
I_{0-4}, RS_0, RS_1 (1)	40	32	34	35	55	42	42	42	ns
FTAB = 1, FTF = 0									
A_0–A_{15}, B_0–B_{15}	—	30	40	32	—	36	46	37	ns
CLK	26	—	—	—	32	—	—	—	ns
C_0	—	—	28	20	—	—	34	22	ns
I_{0-4}, RS_0, RS_1 (1)	—	32	34	35	—	42	42	42	ns
FTAB = 1, FTF = 1									
A_0–A_{15}, B_0–B_{15}	40	30	40	32	55	36	46	37	ns
C_0	30	—	28	20	37	—	34	22	ns
I_{0-4}, RS_0, RS_1 (1)	40	32	34	35	55	42	42	42	ns

NOTE:
1. Minimum propagation delays are guaranteed to be greater than or equal to 3ns although not production tested.

2525 tb 12

8

AC ELECTRICAL CHARACTERISTICS — COMMERCIAL (V_{CC} = 5V ± 5%, T_A = 0°C to +70°C) - (Cont'd.)

Minimum Set-up and Hold Times Relative to Clock (CLK)

Input	IDT7381L20 IDT7383L20		IDT7381L25 IDT7383L25		IDT7381L30 IDT7383L30		IDT7381L40 IDT7383L40		IDT7381L55 IDT7383L55		Unit
	Set-up	Hold	Set-up	Hold	Set-up	Hold	Set-up	Hold	Set-up	Hold	
FTAB = 0, FTF = X											
A_0–A_{15}, B_0–B_{15}	5	0	6	0	6	0	6	0	8	0	ns
C_0 (2)	12	0	16	0	16	0	16	0	21	0	ns
I_0–$_4$, RS_0, RS_1 (1) (2)	15	0	24	0	29	0	32	0	44	0	ns
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	5	0	6	0	6	0	6	0	8	0	ns
FTAB = 1, FTF = 0											
A_0–A_{15}, B_0–B_{15}	14	0	16	0	25	0	28	0	35	0	ns
C_0	12	0	16	0	16	0	16	0	21	0	ns
I_0–$_4$, RS_0, RS_1 (1)	15	0	24	0	29	0	32	0	44	0	ns
$\overline{ENF}$	5	0	6	0	6	0	6	0	8	0	ns

2525 tbl 13

Minimum Clock Cycle Times and Pulse Widths

Parameter	IDT7381L20 IDT7383L20	IDT7381L25 IDT7383L25	IDT7381L30 IDT7383L30	IDT7381L40 IDT7383L40	IDT7381L55 IDT7383L55	Unit
Clock LOW Time	5	6	8	10	14	ns
Clock HIGH Time	5	6	8	10	14	ns
Clock Period	18	20	25	34	43	ns

2525 tbl 14

Maximum Output Enable/Disable Times

Parameter	IDT7381L20 IDT7383L20	IDT7381L25 IDT7383L25	IDT7381L30 IDT7383L30	IDT7381L40 IDT7383L40	IDT7381L55 IDT7383L55	Unit
Enable Time	8	10	15	18	20	ns
Disable Time	8	10	15	18	20	ns

2525 tbl 15

NOTES:
1. For IDT7381, pins I_0 – I_2, RS_0, RS_1 apply. For IDT7383, pins I_0 – I_4 apply.
2. Only for FTF = 0.

AC ELECTRICAL CHARACTERISTICS — MILITARY (Vcc = 5V ± 10%, TA = –55°C to +125°C)

Maximum Combinational Propagation Delays

From Input	IDT7381L25 IDT7383L25				IDT7381L30 IDT7383L30				IDT7381L35 IDT7383L35				Unit
	F_{0-15}	$\overline{P}, \overline{G}, N$	Z,OVF	C_{16}	F_{0-15}	$\overline{P}, \overline{G}, N$	Z,OVF	C_{16}	F_{0-15}	$\overline{P}, \overline{G}, N$	Z,OVF	C_{16}	
FTAB = 0, FTF = 0													
CLK	14	24	24	24	26	28	34	28	27	32	45	32	ns
C_0	—	—	18	18	—	—	22	22	—	—	30	23	ns
I_{0-4}, RS_0, RS_1 (1)	—	22	24	22	—	28	28	28	—	34	34	34	ns
FTAB = 0, FTF = 1													
CLK	25	24	24	24	34	28	34	28	45	32	40	32	ns
C_0	21	—	18	18	26	—	22	22	30	—	30	23	ns
I_{0-4}, RS_0, RS_1 (1)	25	22	24	22	30	28	28	28	40	34	34	34	ns
FTAB = 1, FTF = 0													
A_0–A_{15}, B_0–B_{15}	—	20	25	22	—	28	28	28	—	30	35	32	ns
CLK	14	—	—	—	26	—	—	—	27	—	—	—	ns
C_0	—	—	18	18	—	—	22	22	—	—	30	23	ns
I_{0-4}, RS_0, RS_1 (1)	—	22	24	22	—	28	28	28	—	34	34	34	ns
FTAB = 1, FTF = 1													
A_0–A_{15}, B_0–B_{15}	25	22	25	22	30	28	28	28	40	30	30	32	ns
C_0	21	—	18	18	26	—	22	22	30	—	30	23	ns
I_{0-4}, RS_0, RS_1 (1)	25	22	24	22	30	28	28	28	40	34	34	34	ns

NOTE:
1. Minimum propagation delays are guaranteed to be greater than or equal to 3ns although not production tested.

2525 tb 16

Maximum Combinational Propagation Delays

From Input	IDT7381L45 IDT7383L45				IDT7381L65 IDT7383L65				Unit
	F_{0-15}	$\overline{P}, \overline{G}, N$	Z, OVF	C_{16}	F_{0-15}	$\overline{P}, \overline{G}, N$	Z, OVF	C_{16}	
FTAB = 0, FTF = 0									
CLK	28	34	50	34	37	44	63	45	ns
C_0	—	—	32	23	—	—	42	25	ns
I_{0-4}, RS_0, RS_1 (1)	—	38	38	38	—	48	48	48	ns
FTAB = 0, FTF = 1									
CLK	56	34	50	34	68	44	63	45	ns
C_0	32	—	32	23	42	—	42	25	ns
I_{0-4}, RS_0, RS_1 (1)	46	38	38	38	66	48	48	48	ns
FTAB = 1, FTF = 0									
A_0–A_{15}, B_0–B_{15}	—	32	46	36	—	44	56	44	ns
CLK	28	—	—	—	37	—	—	—	ns
C_0	—	—	32	23	—	—	42	25	ns
I_{0-4}, RS_0, RS_1 (1)	—	38	38	38	—	48	48	48	ns
FTAB = 1, FTF = 1									
A_0–A_{15}, B_0–B_{15}	45	32	46	36	65	44	56	44	ns
C_0	32	—	32	23	42	—	42	25	ns
I_{0-4}, RS_0, RS_1 (1)	46	38	38	38	66	48	48	48	ns

NOTE:
1. Minimum propagation delays are guaranteed to be greater than or equal to 3ns although not production tested.

2525 tb 17

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AC ELECTRICAL CHARACTERISTICS — MILITARY (Vcc = 5V ± 10%, TA = –55°C to +125°C) - (Cont'd)

Minimum Set-up and Hold Times Relative to Clock (CLK)

Input	IDT7381L25 IDT7383L25		IDT7381L30 IDT7383L30		IDT7381L35 IDT7383L35		IDT7381L45 IDT7383L45		IDT7381L65 IDT7383L65		Unit
	Set-up	Hold	Set-up	Hold	Set-up	Hold	Set-up	Hold	Set-up	Hold	
FTAB = 0, FTF = X											
A_0–A_{15}, B_0–B_{15}	7	0	8	0	8	0	8	0	10	0	ns
C_0 (2)	14	0	18	0	19	0	20	0	25	0	ns
I_{0-4}, RS_0, RS_1 (1) (2)	19	0	30	0	32	0	36	0	50	0	ns
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	7	0	8	0	8	0	8	0	10	0	ns
FTAB = 1, FTF = 0											
A_0–A_{15}, B_0–B_{15}	14	0	27	0	30	0	33	0	43	0	ns
C_0	14	0	18	0	19	0	20	0	25	0	ns
I_{0-4}, RS_0, RS_1 (1)	19	0	30	0	34	0	36	0	50	0	ns
$\overline{ENF}$	7	0	8	0	8	0	8	0	10	0	ns

2525 tbl 18

Minimum Clock Cycle Times and Pulse Widths

Parameter	IDT7381L25 IDT7383L25	IDT7381L30 IDT7383L30	IDT7381L35 IDT7383L35	IDT7381L45 IDT7383L45	IDT7381L65 IDT7383L65	Unit
Clock LOW Time	8	12	13	15	20	ns
Clock HIGH Time	8	12	13	15	20	ns
Clock Period	20	26	30	38	52	ns

2525 tbl 19

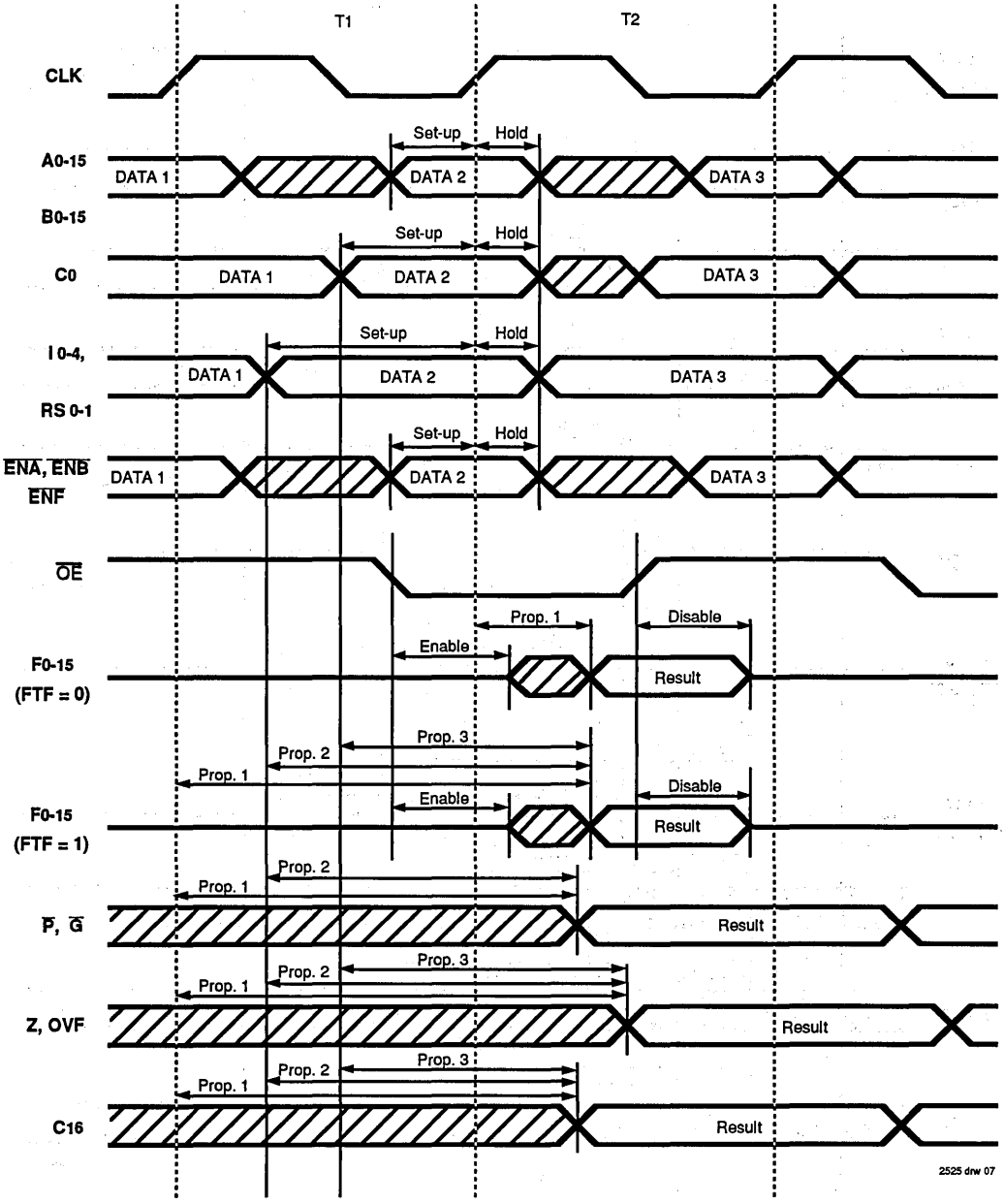
Maximum Output Enable/Disable Times

Parameter	IDT7381L25 IDT7383L25	IDT7381L30 IDT7383L30	IDT7381L35 IDT7383L35	IDT7381L45 IDT7383L45	IDT7381L65 IDT7383L65	Unit
Enable Time	14	18	19	20	22	ns
Disable Time	14	18	19	20	22	ns

2525 tbl 20

NOTES:
1. For IDT7381, pins I_0 – I_2, RS_0, RS_1 apply. For IDT7383, pins I_0 – I_4 apply.
2. Only for FTF = 0.

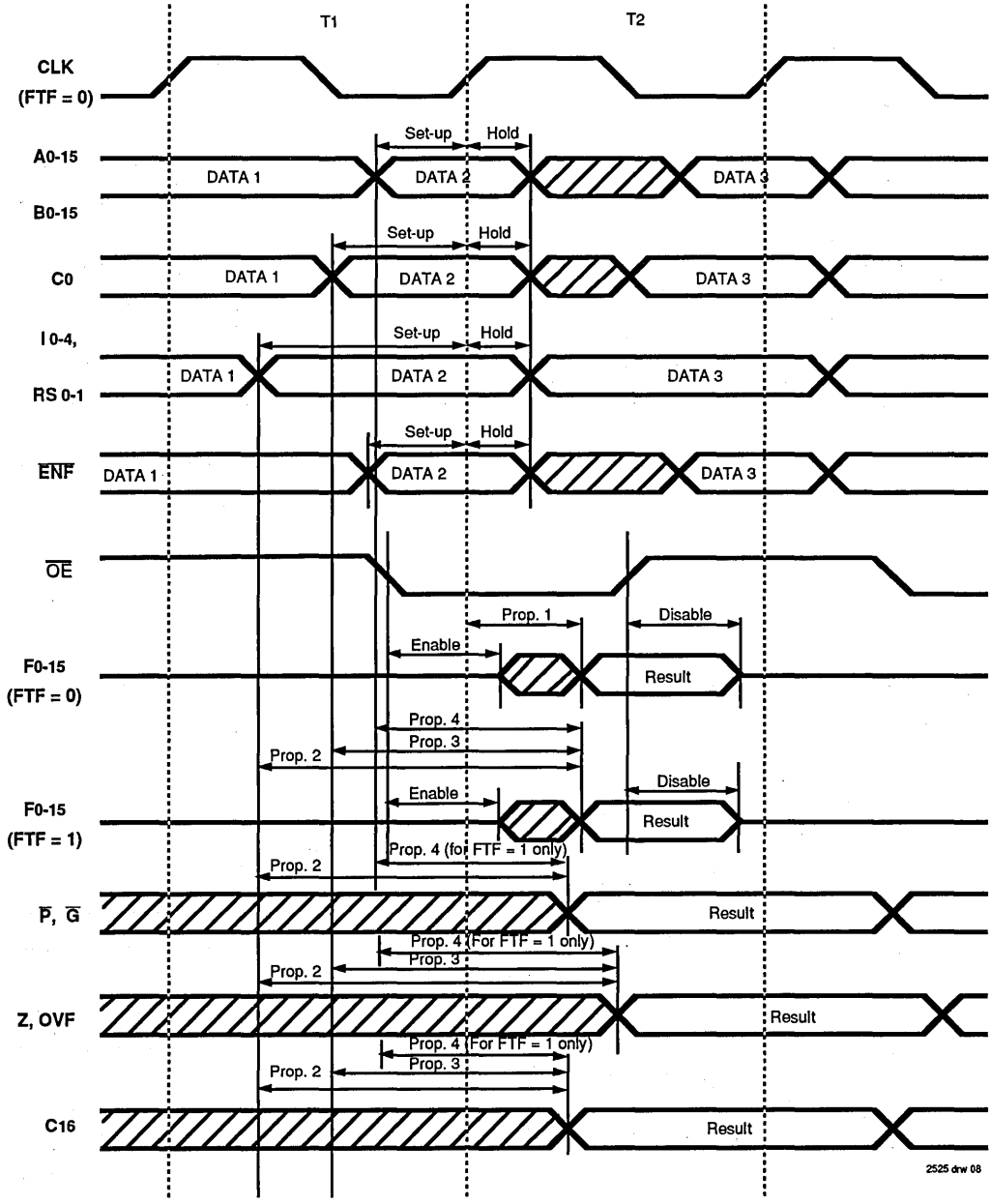
WAVEFORMS FOR FTAB = 0, FTF = X



Prop. 1: Propagation delay with respect to the CLK.
Prop. 2: Propagation delay with respect to b_{-4}, RS_{0-2}.
Prop. 3: Propagation delay with respect to C_0.

8

WAVEFORMS FOR FTAB = 1, FTF = X



Prop. 1: Propagation delay with respect to the CLK.
Prop. 2: Propagation delay with respect to b_{-4}, RS0-2.
Prop. 3: Propagation delay with respect to C_0.
Prop. 4: Propagation delay with respect to A, B.

PROPAGATION DELAY CALCULATIONS FOR TWO IDT7381/7383s

From Input	To Output		To Set PUT Time
	F_{0-15}	Flags [2]	Relative to Clock (CLK)
FTAB = 0, FTF = 0			
CLK	As in 16-bit case	(Clk → C_{16}) + (C_0 → flag)	....
C_0	....	(C_0 → C16) + (C_0 → flag)	(C_0 → C_{16}) + (C_0 set–up time)
I_{0-4}, RS_{0-1} [1]	....	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → flag)	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 set–up time)
A_{0-15}, B_{0-15}	....	....	As in 16-bit case
ENA, ENB,ENF	....	....	As in 16-bit case
FTAB = 0, FTF = 1			
CLK	(Clk → C_{16}) + (C_0 → F_{0-15})	(Clk → C_{16}) + (C_0 → flag)	....
C_0	(C_0 → C_{16}) + (C_0 → F_{0-15})	(C_0 → C_{16}) + (C_0 → flag)	(C_0 → C_{16}) + (C_0 set–up time)
I_{0-4}, RS_{0-1} [1]	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → F_{0-15})	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → flag)	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 set–up time)
A_{0-15}, B_{0-15}	....	....	As in 16-bit case
ENA, ENB,ENF	....	....	As in 16-bit case
FTAB = 1, FTF = 0			
CLK	As in 16-bit case	....	....
C_0	....	(C_0 → C_{16}) + (C_0 → flag)	(C_0 → C_{16}) + (C_0 set–up time)
I_{0-4}, RS_{0-1} [1]	....	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → flag)	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 set–up time)
A_{0-15}, B_{0-15}	....	(A_{0-15}, B_{0-15} → C_{16}) + (C_0 → flag)	As in 16-bit case
ENA, ENB,ENF	....	....	As in 16-bit case
FTAB = 0, FTF = 1			
CLK	Don't care condition	Don't care condition	....
C_0	(C_0 → C_{16}) + (C_0 → F_{0-15})	(C_0 → C_{16}) + (C_0 → flag)	....
I_{0-4}, RS_{0-1} [1]	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → F_{0-15})	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → flag)	....
A_{0-15}, B_{0-15}	(A_{0-15}, B_{0-15} → C_{16}) + (C_0 → F_{0-15})	(A_{0-15}, B_{0-15} → C_{16}) + (C_0 → flag)	....
ENA, ENB,ENF	....	....	....

2525 tbl 22

NOTES:
1. For IDT7381, pins I_{0-2}, RS_{0-2} apply. For IDT7383, pins I_{0-4} apply.
2. Flags are $\overline{P}$, $\overline{G}$, OVF, Z, C_{16} for IDT7381. Flags are N, OVF, Z C_{16} for IDT7383.

8

CASCADING THE IDT7381/3

Some applications require 32-bit or wider input operands. Cascading is the hardware solution. It provides a high speed alternative in handling more than 16-bit wide operands.

This section is divided in three parts:

1. Cascading the IDT7381
2. Cascading the IDT7383
3. Time delay considerations

1. Cascading the IDT7381

Cascading to 32-bit wide operands takes only two IDT7381s and no external hardware. However, cascading to data widths greater than 32-bit can be done in two ways: without external hardware (slow method) or by using a carry look ahead generator like FCT182 (fast method).

a) Cascading the IDT7381 without a carry-look-ahead generator: (Figures 2 and 3)

1. Connect the C_{16} output of the least significant device into the Co input of the next most significant device.
2. Common lines to all devices are: RS_{0-1}, I_{0-2}, Clk, FTF, FTAB, $\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$.
3. Take OVF, C_{16}, $\overline{P}$, $\overline{G}$ of the most significant device as valid.
4. The system's zero flag (Z) is obtained by ANDing all zero flag results.

b) Cascading three or more IDT7381s with carry-look-ahead (CLA) generator: (Figure 4)

1. Connect the $\overline{P}$ and $\overline{G}$ outputs of each device to the CLA generator's corresponding inputs.
2. Take the CLA generator outputs into the Co inputs of each device (except for the least significant one).
3. Common lines to all devices are: RS_{0-1}, I_{0-2}, Clk, FTF, FTAB, $\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$.
4. Take OVF, C_{16}, $\overline{P}$, $\overline{G}$ of the most significant device as valid.
5. Carry-in to the system should be connected to the Co input of the least significant device and also to the CLA generator.

2. Cascading the IDT7383

(Figures 5 and 6)

1. Connect the C_{16} output of the least significant device into the Co input of the next most significant device.
2. Common lines to all devices are: I_{0-4}, Clk, FTF, FTAB, $\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$.
3. Take OVF, C_{16}, N of the most significant device as valid.
4. The system's zero flag (Z) is obtained by ANDing all zero flag results.

3. Time Delay Considerations

Once cascading has taken place, time delays may become critical in high performance systems. Our main interest here is focused on "propagation delays", i.e. calculating the time required for an input signal to propagate through several cascaded devices up to a specific output in another device within the cascaded system.

Propagation Delay

The propagation delay *for two devices* between the input and output of interest (input to output delay) is done as follows:

1. Calculate delay between the input and C_{16} in the first device.
2. Calculate delay between Co and the output in the second device.
3. Add both results.

The following table is an example on how to build a propagation delay table for all inputs in a 32-bit IDT7381/3 cascaded system.

Propagation delay calculations can be extended to *n–cascaded* devices as the sum of the delays in all devices between the input and output of interest. That is:

$(Input)_1 \rightarrow (C_{16})_1 = t_1$

...

$(Co)_i \rightarrow (C_{16})_i = t_i$

$(Co)_{i+1} \rightarrow (C_{16})_{i+1} = t_{i+1}$

...

$(Co)_n \rightarrow (Output)_n = t_n$

Where the subscript i denotes the device number and the arrow (→) represents the delay in between. Notice that i + 1 is the immediate upper device from device i. Adding the delays t_i we get:

Propagation delay = $t_1 + t_2 + ... + t_i + t_{i+1} + ... + t_n$

Total Delay

As seen from Figure 11, the propagation delay is within the IDT7381/3 devices only. A complete analysis should also include the delay associated with the transmission line Li (which depends on the line length and its impedance). This line delay should then be added to the propagation delay to obtain the total delay for the cascaded system:

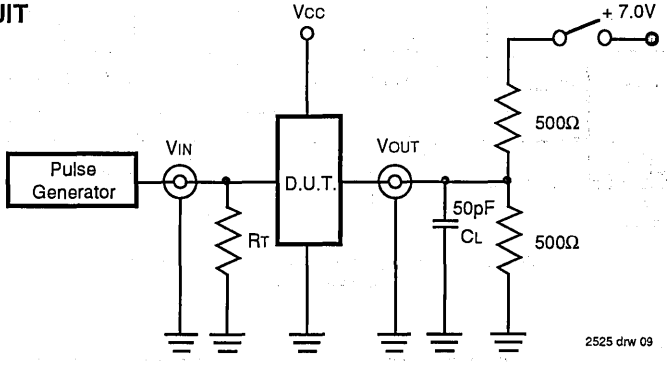
Total delay = Propagation delay + Transmission line delay

CMOS TESTING CONSIDERATIONS

There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large V_{CC} current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscillate causing improper device operation and possible latchup.
3) Definition of input levels is very important. Since many inputs may change coincidentally, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

TEST LOAD CIRCUIT



DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance
R_L = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

Figure 1. AC Test Load Circuit

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2525 tbl 21

Test	Switch
Disable Low	Closed
Enable Low	
All other Outputs	Open

2525 tbl 23

8

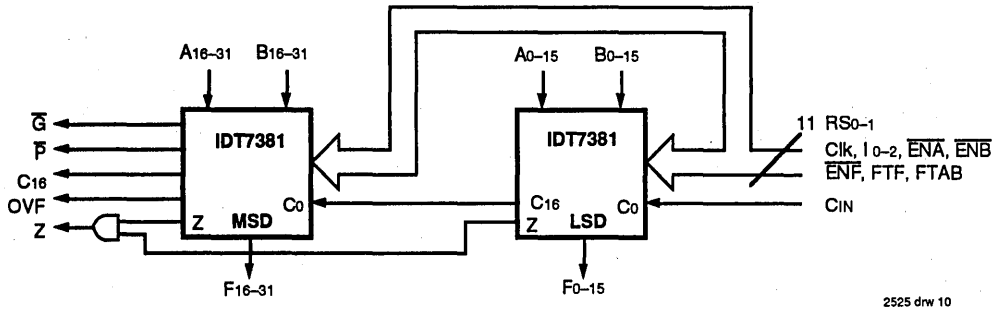


Figure 2. Cascading Two IDT7381s to 32 Bits

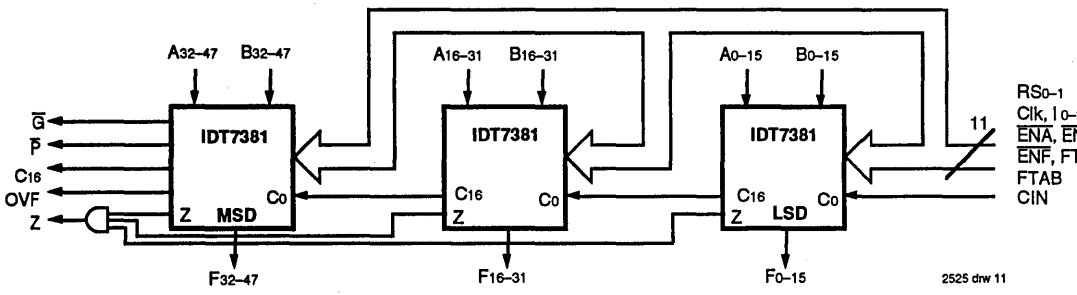


Figure 3. Cascading Three IDT7381s to 48 Bits Wide without a Carry-lookahead Generator

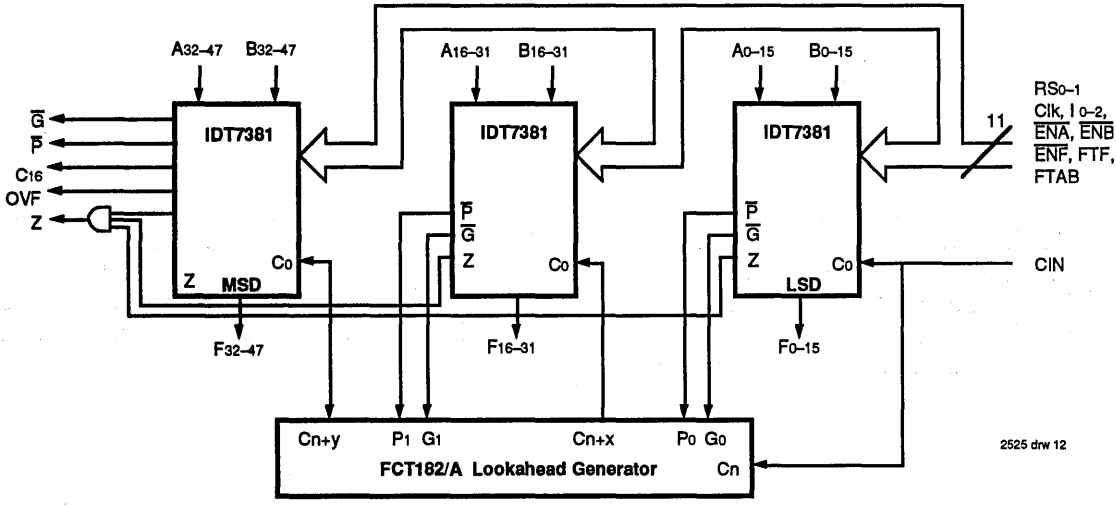


Figure 4. Cascading Three IDT7381s to 48 Bits Wide with a Carry-lookahead Generator

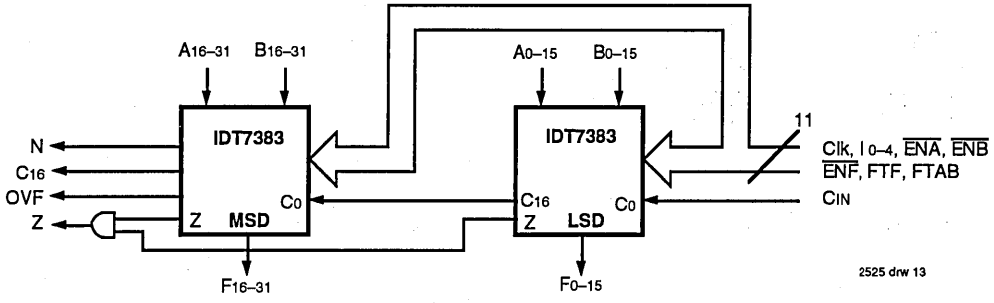


Figure 5. Cascading Two IDT7383s to 32 Bits

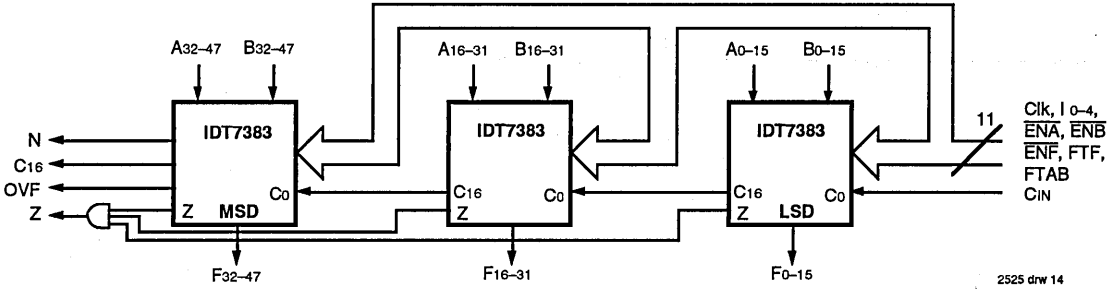


Figure 6. Cascading Three IDT7383s to 48 Bits

8

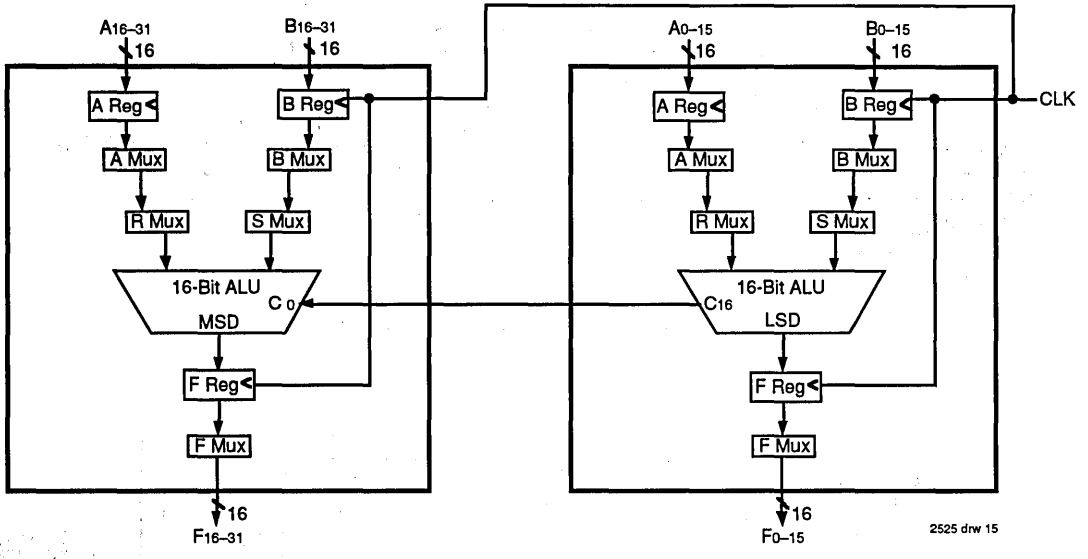


Figure 7. 32-Bit Configuration for FTAB = 0, FTF = 0

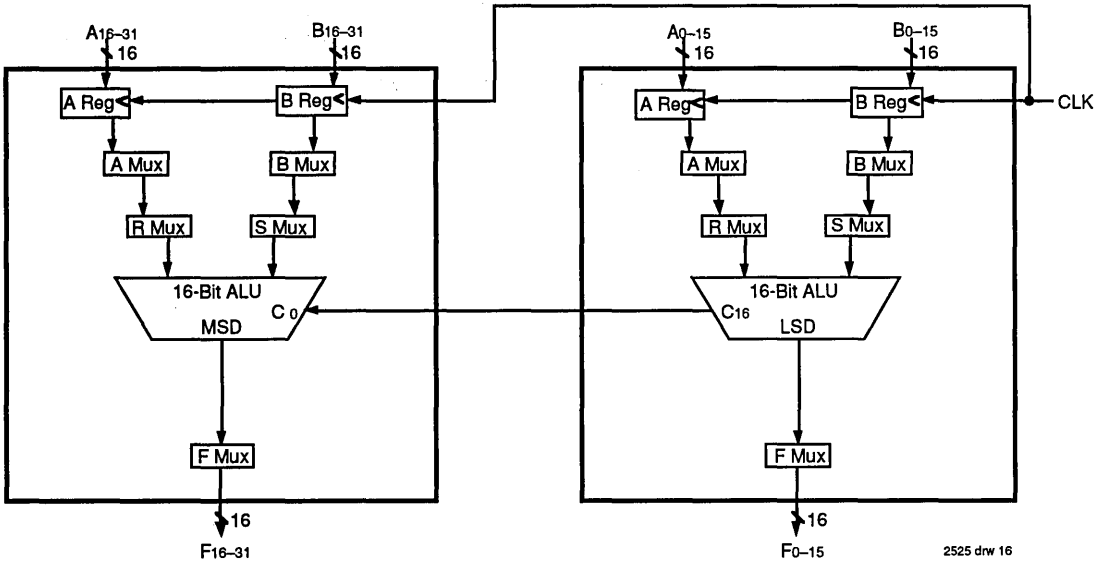


Figure 8. 32-Bit Configuration for FTAB = 0, FTF = 1

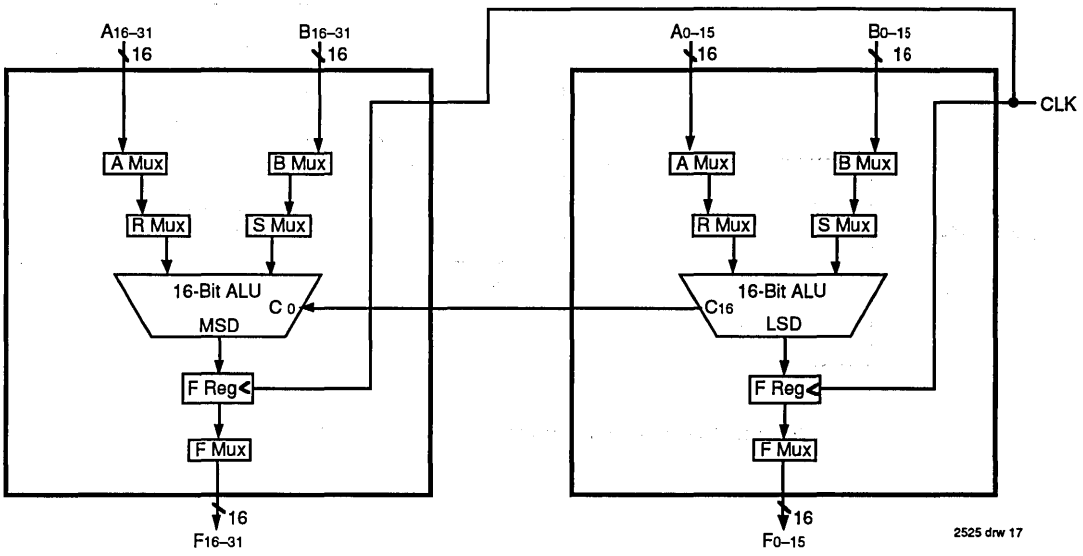


Figure 9. 32-Bit Configuration for FTAB = 1, FTF = 0

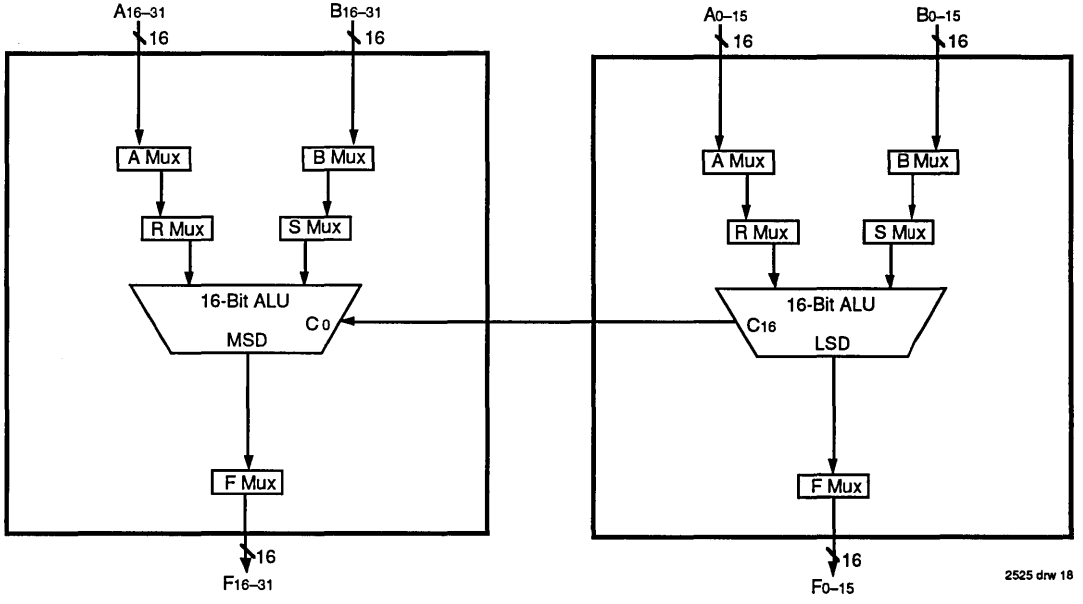


Figure 10. 32-Bit Configuration for FTAB = 1, FTF = 1

8

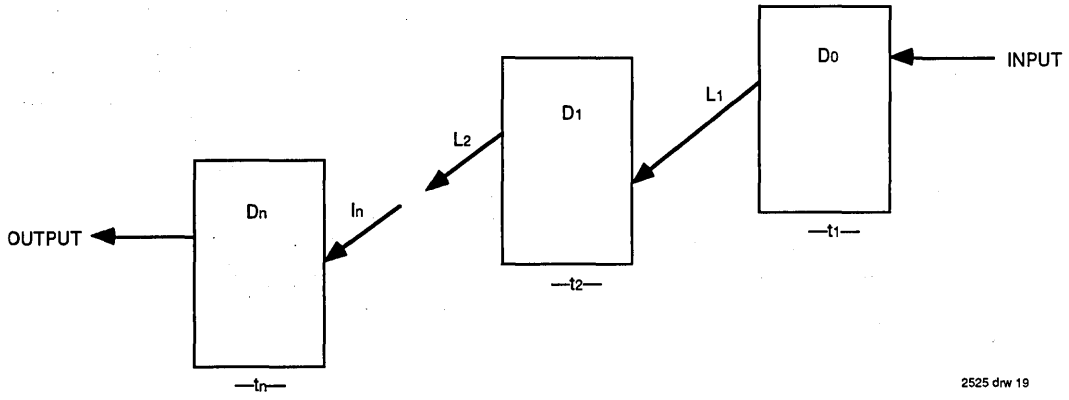


Figure 11. Propagation Delay = t1 + t2 + . . . + tn N-Cascaded Devices

Integrated Device Technology, Inc.

16-BIT CMOS MULTILEVEL PIPELINE REGISTERS

IDT73200
IDT73201

FEATURES:

- IDT73200: Eight 16-bit high-speed pipeline registers
- IDT73201: Seven 16-bit high-speed pipeline registers plus a direct feed-through path
- 10ns access time
- Programmable multilevel register configurations
- Powerful instruction set: transfer, hold, load directly
- Functionally replaces four Am29520s
- Read/Write buffer for 32-bit RISC/CISC microprocessors
- Applications as temporary address storage or programmable pipeline registers for DSP products
- Coefficient storage for FIR filters
- Three-state outputs
- TTL-compatible
- Available in 48-pin plastic and ceramic DIP and 52-pin surface mount PLCC
- Military product compliant to MIL-STD-883, Class B
- Speeds available:
  Commercial: L10/12/15
  Military: L12/15/20

DESCRIPTION:

The IDT73200 and IDT73201 are mutilevel pipeline registers. With IDT's high-performance CEMOS™ technology, the IDT73200 and IDT73201 have access times of 10ns.

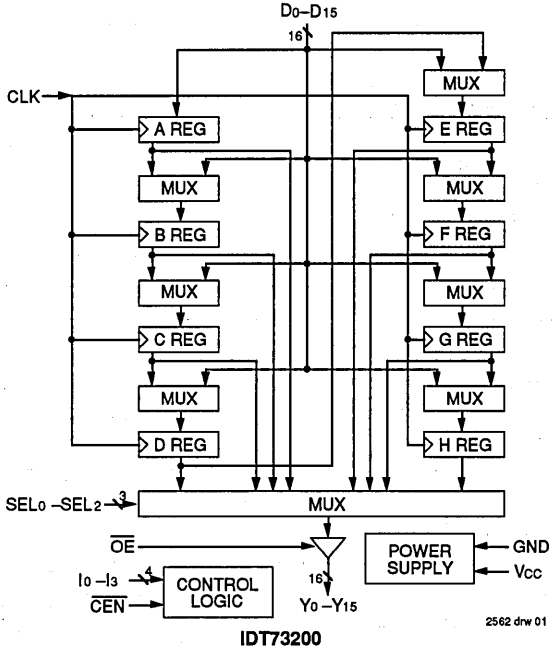
The IDT73200 contains eight 16-bit registers which can be configured as one 8-level, two 4-level, four 2-level or eight 1-level pipeline registers.

The IDT73201 contains seven 16-bit registers and a direct feed-through path. The seven registers can be configured as one 7-level, a 4-level plus a 3-level, three 2-level or seven 1-level pipeline registers.

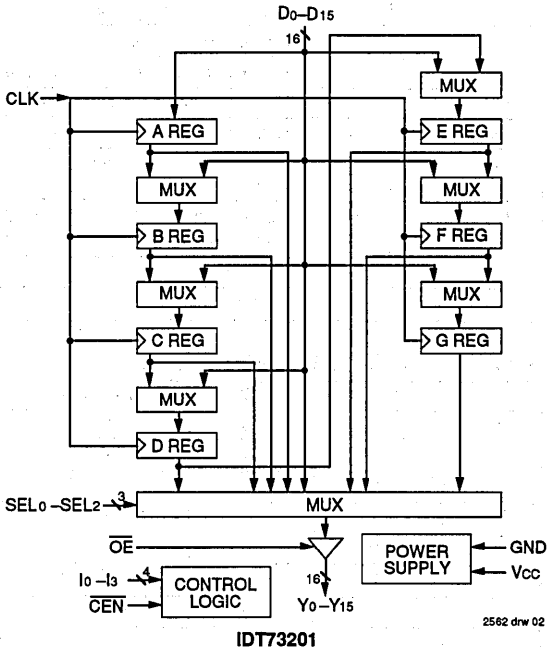
An eight-to-one output multiplexer allows data to be read from any one of the registers or from the feed-through path on the IDT73201. Three input control pins (SEL_0–SEL_2) select which of the multiplexer inputs are directed to the output (Y_0–Y_{15}).

These pipeline registers are ideal for high throughput, vector-oriented operations such as those in digital signal processing (DSP). The IDT73200 and IDT73201 can also be used as quick access scratch pad registers for general purpose computing and as Read/Write buffers for RISC/CISC Microprocessors.

FUNCTIONAL BLOCK DIAGRAMS



IDT73200

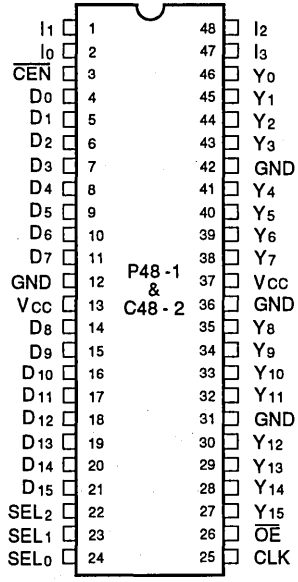


IDT73201

CEMOS is a trademark of Integrated Device Technology Inc.

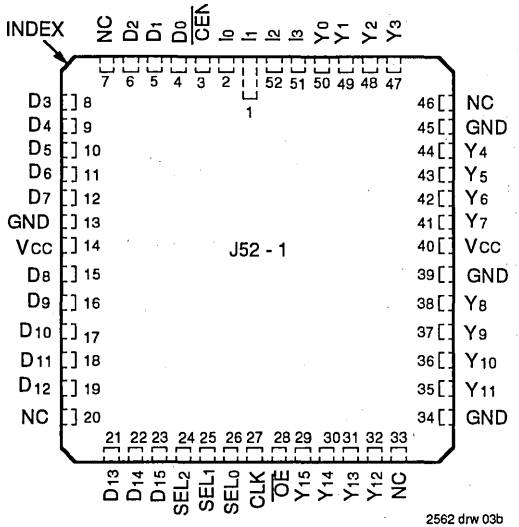
8

PIN CONFIGURATIONS



DIP
TOP VIEW

2562 drw 03a



2562 drw 03b

PLCC
TOP VIEW

PIN DESCRIPTIONS

Pin Name	I/O	Description
$D_0 - D_{15}$	I	Sixteen-bit data input port.
$Y_0 - Y_{15}$	O	Sixteen-bit data output port.
$I_0 - I_3$	I	Four control pins to select the register operation performed.
$SEL_0 - SEL_2$	I	Three control pins to select the register appearing at the output.
CLK	I	Clock input.
$\overline{CEN}$	I	Clock enable control pin. When this pin is low, the instruction I_0–I_3 is performed on the registers. When high, no register operation occurs.
$\overline{OE}$	I	Output enable control pin. When this pin is high, the output port Y is in a high impedance state. When low, the output port Y is active.
V_{CC}		Power supply pin, 5V.
GND		Ground pins, 0V.

2562 tbl 01

IDT73200 OUTPUT SELECTION

SEL_2	SEL_1	SEL_0	Y Output
0	0	0	$A \rightarrow Y_0 - Y_{15}$
0	0	1	$B \rightarrow Y_0 - Y_{15}$
0	1	0	$C \rightarrow Y_0 - Y_{15}$
0	1	1	$D \rightarrow Y_0 - Y_{15}$
1	0	0	$E \rightarrow Y_0 - Y_{15}$
1	0	1	$F \rightarrow Y_0 - Y_{15}$
1	1	0	$G \rightarrow Y_0 - Y_{15}$
1	1	1	$H \rightarrow Y_0 - Y_{15}$

2562 tbl 02

IDT73201 OUTPUT SELECTION

SEL_2	SEL_1	SEL_0	Y Output
0	0	0	$A \rightarrow Y_0 - Y_{15}$
0	0	1	$B \rightarrow Y_0 - Y_{15}$
0	1	0	$C \rightarrow Y_0 - Y_{15}$
0	1	1	$D \rightarrow Y_0 - Y_{15}$
1	0	0	$E \rightarrow Y_0 - Y_{15}$
1	0	1	$F \rightarrow Y_0 - Y_{15}$
1	1	0	$G \rightarrow Y_0 - Y_{15}$
1	1	1	$D_0 - D_{15} \rightarrow Y_0 - Y_{15}$

2562 tbl 03

IDT73200 INSTRUCTION TABLE

I_3	I_2	I_1	I_0	Mnemonic	Function	Pipeline Levels
0	0	0	0	LDA	$D_0 - D_{15} \rightarrow A$	1
0	0	0	1	LDB	$D_0 - D_{15} \rightarrow B$	1
0	0	1	0	LDC	$D_0 - D_{15} \rightarrow C$	1
0	0	1	1	LDD	$D_0 - D_{15} \rightarrow D$	1
0	1	0	0	LDE	$D_0 - D_{15} \rightarrow E$	1
0	1	0	1	LDF	$D_0 - D_{15} \rightarrow F$	1
0	1	1	0	LDG	$D_0 - D_{15} \rightarrow G$	1
0	1	1	1	LDH	$D_0 - D_{15} \rightarrow H$	1
1	0	0	0	LSHAH	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D \rightarrow E \rightarrow F \rightarrow G \rightarrow H$	8
1	0	0	1	LSHAD	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D$	4
1	0	1	0	LSHEH	$D_0 - D_{15} \rightarrow E \rightarrow F \rightarrow G \rightarrow H$	4
1	0	1	1	LSHAB	$D_0 - D_{15} \rightarrow A \rightarrow B$	2
1	1	0	0	LSHCD	$D_0 - D_{15} \rightarrow C \rightarrow D$	2
1	1	0	1	LSHEF	$D_0 - D_{15} \rightarrow E \rightarrow F$	2
1	1	1	0	LSHGH	$D_0 - D_{15} \rightarrow G \rightarrow H$	2
1	1	1	1	HOLD	Hold All Registers	—

2562 tbl 04

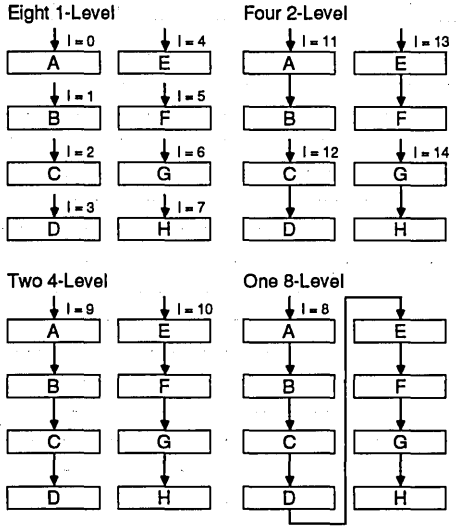
IDT73201 INSTRUCTION TABLE

I_3	I_2	I_1	I_0	Mnemonic	Function	Pipeline Levels
0	0	0	0	LDA	$D_0 - D_{15} \rightarrow A$	1
0	0	0	1	LDB	$D_0 - D_{15} \rightarrow B$	1
0	0	1	0	LDC	$D_0 - D_{15} \rightarrow C$	1
0	0	1	1	LDD	$D_0 - D_{15} \rightarrow D$	1
0	1	0	0	LDE	$D_0 - D_{15} \rightarrow E$	1
0	1	0	1	LDF	$D_0 - D_{15} \rightarrow F$	1
0	1	1	0	LDG	$D_0 - D_{15} \rightarrow G$	1
0	1	1	1	HOLD	Hold All Registers	—
1	0	0	0	LSHAG	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D \rightarrow E \rightarrow F \rightarrow G$	7
1	0	0	1	LSHAD	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D$	4
1	0	1	0	LSHEG	$D_0 - D_{15} \rightarrow E \rightarrow F \rightarrow G$	3
1	0	1	1	LSHAB	$D_0 - D_{15} \rightarrow A \rightarrow B$	2
1	1	0	0	LSHCD	$D_0 - D_{15} \rightarrow C \rightarrow D$	2
1	1	0	1	LSHEF	$D_0 - D_{15} \rightarrow E \rightarrow F$	2
1	1	1	0	LDG	$D_0 - D_{15} \rightarrow G$	1
1	1	1	1	HOLD	Hold All Registers	—

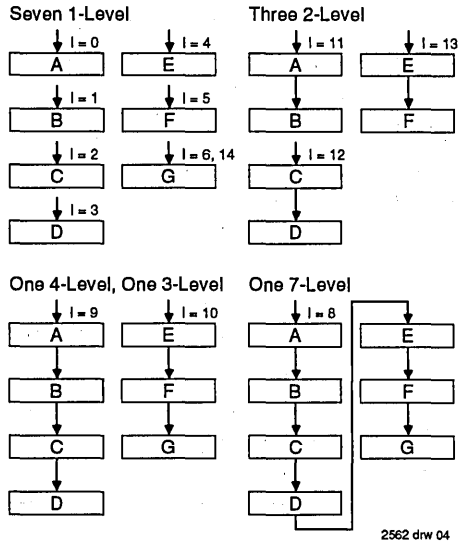
2562 tbl 05

8

IDT73200 PIPELINE CONFIGURATIONS



IDT73201 PIPELINE CONFIGURATIONS



2562 drw 04

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{CC}	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
2562 tbl 06

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
2562 tbl 07

1. This parameter is sampled at initial characterization and is not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Commercial: 0°C to +70°C, 5V ± 5%; Military: –55°C to +125°C, 5V ± 10%

Symbol	Parameter	Test Condition		Min.	Max	Unit
V_{IH}	High-Level Input Voltage	Guaranteed Logic HIGH Level		2.0	—	V
V_{IL}	Low-Level Input Voltage	Guaranteed Logic LOW Level		—	0.8	V
I_{IH}	High Level Input Current	V_{CC} = Max.	$V_I = V_{CC}$	—	1	µA
I_{IL}	Low-Level Input Current	V_{CC} = Max.	V_I = GND	—	–1	µA
V_{OH}	High-Level Output Voltage	V_{CC} = Min., I_{OH} = -8mA(COM'L.), –6mA(MIL.)		2.4	—	V
V_{OL}	Low-Level Output Voltage	V_{CC} = Min., I_{OL} = 16mA(COM'L.), 12mA(MIL.)		—	0.4	V
I_{OS}	Short Circuit Output Current[2]	V_{CC} = Max., V_O = GND $V_I = V_{CC}$ or GND		–20	–200	mA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	$V_I = V_{CC}$	—	1	µA
I_{OZL}	Low Impedance Output Current	V_{CC} = Max.	V_I = GND	—	–1	µA

NOTES:

2562 tbl 08

1. For conditions shown as Min. or Max., use appropriate value based on temperature range.
2. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed 100 milliseconds.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} = V_{CC}$ or GND		—	2	10	mA
I_{CCQT}	Quiescent Power Supply Current Inputs HIGH	V_{CC} = Max. V_I = 3.4V		—	15	45	mA
I_{CCD1}[3]	Dynamic Power Supply Current	V_{CC} = Max. Outputs Disable f_{CP} = 10MHz, 50% Duty Cycle $V_{IN} = V_{CC}$ or GND	COM'L.	—	10	30	mA
			MIL.	—	10	40	

NOTES:

2562 tbl 09

1. For conditions shown as Min. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading, not production tested.
3. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CCQC} + (I_{CCQT} \times D_H \times N_T) + I_{CCD} (f_{CP})$
   I_{CCQC} = Quiescent Current
   I_{CCQT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for each TTL Input High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Charge moved by an input transition pair (HLH or LH) mA/MHz
   f_{CP} = Clock frequency
   All currents are in milliamps and all frequencies are in megahertz.

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AC ELECTRICAL CHARACTERISTICS

Commerical: T_A = 0°C to +70°C, V_{CC} = 5V ±5%; Military: T_A = –55°C to +125°C, V_{CC} = 5V ±10%

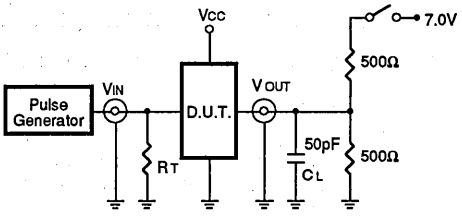
Parameter	Commercial						Military						Unit
	73200L10 73201L10		73200L12 73201L12		73200L15 73201L15		73200L12 73201L12		73200L15 73201L15		73200L20 73201L20		
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
CLK to Y_0–Y_{15} Propagation Delay[3]	2.5	10	2.5	12	2.5	15	2.5	12	2.5	15	2.5	20	ns
SEL_0–SEL_2 to Y_0–Y_{15} Propagation Delay[3]	2.5	10	2.5	12	2.5	15	2.5	12	2.5	15	2.5	20	ns
D_0–D_{15} to CLK Set-up Time	3	—	3	—	4	—	3	—	4	—	5	—	ns
D_0–D_{15} to CLK Hold Time	0	—	1	—	2	—	1	—	2	—	3	—	ns
I_0–I_3 to CLK Set-up Time	3	—	4	—	5	—	4	—	5	—	6	—	ns
I_0–I_3 to CLK Hold Time	1.5	—	2	—	2	—	2	—	2	—	3	—	ns
$\overline{CEN}$ to CLK Set-up Time	3	—	4	—	5	—	4	—	5	—	6	—	ns
$\overline{CEN}$ to CLK Hold Time	1.5	—	4	—	5	—	4	—	5	—	6	—	ns
$\overline{OE}$ Enable Time[1]	—	7	—	9	—	10	—	9	—	10	—	13	ns
$\overline{OE}$ Disable Time[1]	—	6	—	8	—	9	—	8	—	9	—	13	ns
CLK Pulse Width HIGH[4]	5	—	5	—	5	—	5	—	5	—	6	—	ns
CLK Pulse Width LOW[4]	5	—	5	—	5	—	5	—	5	—	6	—	ns
CLK Period	10	—	12	—	15	—	12	—	15	—	20	—	ns
Data In to Data Out [2,3] Flowthrough Prop. Delay	2.5	10	2.5	12	2.5	15	2.5	12	2.5	15	2.5	20	ns

NOTES:
1. Output Enable and Disable times measured to 500mV change of output voltage level.
2. 73201 only.
3. Minimum propagation delays are guaranteed, but not production tested.
4. Minimum pulse widths are guaranteed, but not production tested.

2562 tbl 11

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

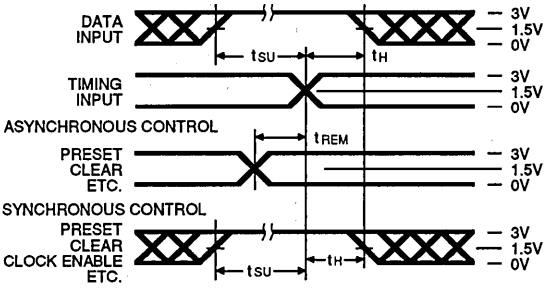
Test	Switch
Disable Low Enable Low	Closed
All Other Tests	Open

2613 tbl 08

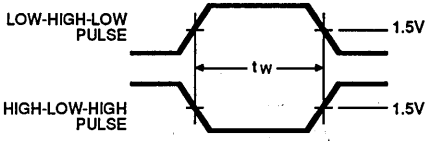
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

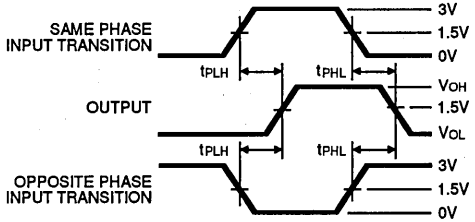
SET-UP, HOLD AND RELEASE TIMES



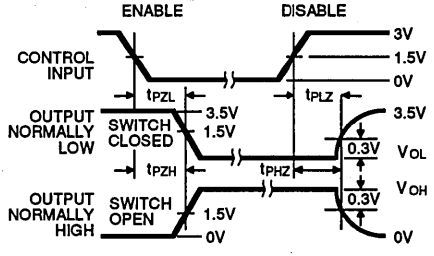
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES



NOTES

2613 drw 05

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

8

Integrated Device Technology, Inc.

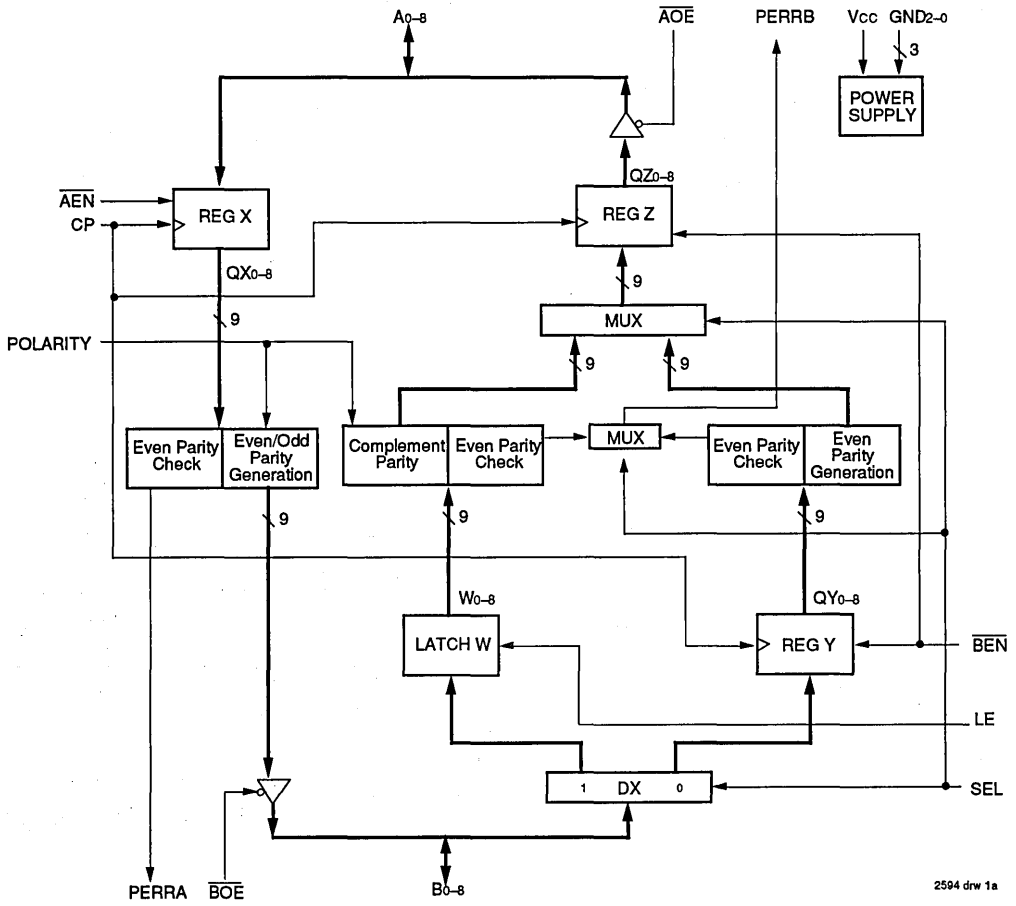
FAST CMOS OCTAL REGISTER TRANSCEIVER WITH PARITY

PRELIMINARY
IDT73210/A/B
IDT73211/A/B

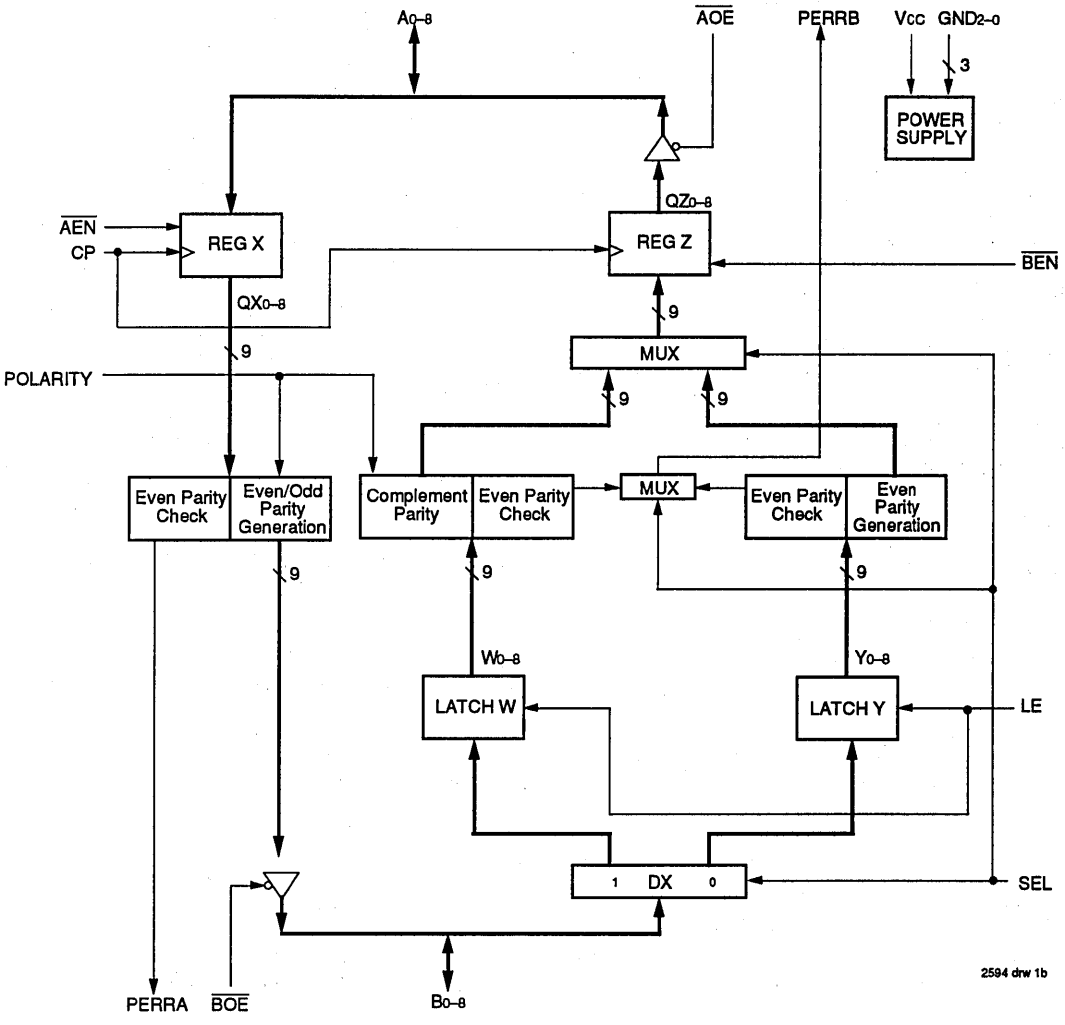
FEATURES

- Two bidirectional 9-bit I/O ports
- Available in standard, A, and B speed grades
- High output drive capability: 64mA (Com'l), 48mA (Mil)
- Low CMOS power: 0.1mW typical
- Parity Generation/Checking in both directions with polarity control for A-to-B direction
- 73210/211 Single-level pipeline register from Port A to Port B
- 73210 Two level pipeline register from Port B to Port A
- 73211 Single level pipeline register from Port B to Port A
- Military product compliant to MIL-STD-883, Class B
- Available in 32-pin sidebraze DIP and surface mount 32-pin SOJ packages

IDT73210 FUNCTIONAL BLOCK DIAGRAM



IDT73211 FUNCTIONAL BLOCK DIAGRAM



8

DESCRIPTION

The IDT73210/211 Octal Register Transceivers with parity, are designed for high performance systems requiring bidirectional data transfer between two busses with parity support. These transceivers are offered in several speed grades to support data transfer in systems with up to 40 MHz data rates. The output buffers have high drive capability for high capacitance driving and low impedence line driving.

The IDT73210/211 Register Transceivers provide Even/Odd parity generation from Port A to Port B and Even parity generation from Port B to Port A. Even parity checking with ERROR flag is provided in both directions. The Even/Odd parity and Generate/Check options can be dynamically reconfigured.

The IDT73210/211 can be used as an interface between a cache memory and the main memory in any RISC or CISC microprocessor system. The pipelining feature makes these devices ideal for use as Read/Write buffers. They can also be used as high speed general purpose registers in any parity based system. In this application, the IDT73210/211 replace the equivalent of an FCT52 Bidirectional Register and two F280 parity generator/checker devices.

DETAILED FUNCTIONAL DESCRIPTION

Port A to Port B Path (IDT73210 and IDT73211) is comprised of a register (X), an even/odd parity generator and an even parity checker. The input data is on the A_{0-8} lines. When $\overline{AEN}$ is low, A_{0-8} is latched into Register X on the low-to-high CP transition. Even parity of the latched data is checked. If PERRA goes high, a parity error has occurred. A new parity bit, B_8, is generated. The output data bus is B_{0-8} and is enabled when $\overline{BOE}$ is low.

Port B to Port A Path (IDT73210) is comprised of a latch (W), two registers (Y and Z), an even parity generator/checker and a parity bit latch complementor. The input data bus is on the B_{0-8} lines.

When SEL is high, the incoming data is latched into Latch W. When LE is high, Latch W is transparent; when LE is low, Latch W is closed. The parity bit, B_8, can be complemented by the POLARITY pin. If POLARITY is low, the parity sense remains the same. If POLARITY is high, the parity sense is complemented. Parity is not generated in this path. Even parity of latched data is checked. If PERRB goes high, a parity error has occurred. When $\overline{BEN}$ is low, W_{0-8} is latched into Register Z on the low-to-high CP transition. The previous contents are held in Register Z if $\overline{BEN}$ is high or if there is no low-to-high CP transition. The output data bus is A_{0-8} and is enabled when $\overline{AOE}$ is low. When SEL is high, there is only a one clock cycle latency.

When SEL is low, the incoming data is latched into Register Y on the low-to-high CP transition, when $\overline{BEN}$ is low. Even parity of the registered data is checked. If PERRB goes high, a parity error has occurred. Even parity (QY_8) is generated on the contents in Register Y. When $\overline{BEN}$ is low, the contents of register Y are transferred to Register Z on the low-to-high CP transition. When $\overline{BOE}$ is low, the content of Register Z is made available at output Port A. When SEL is low, there is a two clock cycle latency.

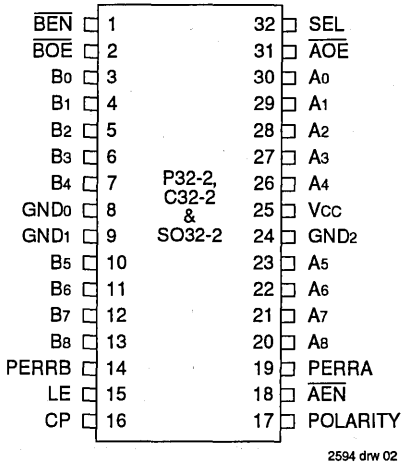
Port B to Port A Path (IDT73211) is comprised of latch (W), latch (Y), register (Z), an even parity generator/checker and a parity bit latch complementor. The input data bus is on the B_{0-8} lines.

When SEL is high, the incoming data is latched into Latch W. When LE is high, Latch W is transparent; when LE is low, Latch W is closed. The parity bit, B_8, can be complemented by the POLARITY pin. If POLARITY is low, the parity sense remains the same. If POLARITY is high, the parity sense is complemented. Parity is not generated in this path. Even parity of latched data is checked. If PERRB goes high, a parity error has occurred. When $\overline{BEN}$ is low, W_{0-8} is latched into Register Z on the low-to-high CP transition. The previous contents are held in Register Z if $\overline{BEN}$ is high or if there is no low-to-high CP transition. The output data bus is A_{0-8} and is enabled when $\overline{AOE}$ is low. When SEL is high, there is only a one clock cycle latency.

When SEL is low, the incoming data is latched into Latch Y when LE is high. Latch Y is closed when LE is low. Even parity of latched data is checked. If PERRB goes high, a parity error has occurred. Even parity (Y_8) is generated on the contents in Latch Y. When $\overline{BEN}$ is low, the contents of Latch Y are transferred to Register Z on the low-to-high CP transition. When $\overline{BOE}$ is low, the content of Register Z is made available at output Port A. When SEL is low, there is a one clock cycle latency.

The power pins are Vcc and GND_{0-2}. GND_0 is internal quiet ground, GND_1 is Port B ground and GND_2 is Port A ground.

PIN CONFIGURATIONS[1]



2594 drw 02

DIP/SOJ
TOP VIEW

NOTE:
1. GND_0 is internal quiet ground
   GND_1 is B Port ground
   GND_2 is A Port ground

PIN DESCRIPTIONS

Pin Name	I/O	Description
A_{0-8}	I/O	Data Port A.
$\overline{AEN}$	I	Clock enable (active low) for the register X.
$\overline{AOE}$	I	3-state output enable for Port A.
B_{0-8}	I/O	Data Port B.
$\overline{BEN}$	I	Clock enable (active low) for the registers Y and Z.
$\overline{BOE}$	I	3-state output enable for Port B.
LE	I	Latch enable input for Latch Y/Latch W of Port B. The Latch Y/Latch W is open when LE is high. Data is latched on the high-to-low transition of LE.
SEL	I	Input selection for Port B. SEL = 0 Register Y (73210); SEL = 1 Latch W SEL = 0 Latch Y (73211);
POLARITY	I	Polarity selection input. **Polarity** / **A to B Direction** / **B to A Direction** 0 / EVEN / Pass Parity 1 / ODD / Complement Parity
PERRA	O	Parity output error for Port A.
PERRB	O	Parity output error for Port B.
CP	I	Input clock.
VCC		+5 volts.
GND_{0-2}		Ground.

2594 tbl 01

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OPERATING MODES SUMMARY

IDT73210/11 A TO B DIRECTION, SEL = X

Input	Reg. X	PERRA	Output	
			(B_8)	B_{0-8}
A_{0-8}	$A_{0-8} \rightarrow QX_{0-8}$ ($\overline{CP}$ = Lo to Hi) ($\overline{AEN}$ = 0)	Result of even parity check	Even/odd parity bit B_8 = POLARITY XOR Even parity generate from QX_{0-7}	$QX_{0-8} \rightarrow B_{0-8}$ ($\overline{BOE}$ = 0)

2594 tbl 02

IDT73210/1 B TO A DIRECTION WHEN SEL = 1

Input	Latch W	PERRB	Reg. Z		Output	
			(QZ_8)	QZ_{0-8}	(A_8)	A_{0-8}
B_{0-8}	$B_{0-8} \rightarrow W_{0-8}$ (LE = 1)	Result of even parity check	Bit complemented by POLARITY (Even/odd parity translation)	$W_{0-8} \rightarrow QZ_{0-8}$ ($\overline{CP}$ = Lo to Hi) ($\overline{BEN}$ = 0)	A_8 = POLARITY XOR W_8	$\overline{QZ_{0-8}} \rightarrow A_{0-8}$ ($\overline{AOE}$ = 0)

2594 tbl 03

IDT73210 B TO A DIRECTION WHEN SEL = 0

Input	Reg. Y	PERRB	Reg. Z		Output	
			(QZ_8)	QZ_{0-8}	(A_8)	A_{0-8}
B_{0-8}	$B_{0-8} \rightarrow QY_{0-8}$ ($\overline{CP}$ = Lo to Hi) ($\overline{BEN}$ = 0)	Result of even parity check	Even parity generated bit	$QY_{0-8} \rightarrow QZ_{0-8}$ ($\overline{CP}$ = Lo to Hi) ($\overline{BEN}$ = 0)	A_8 = Even parity generated from QY_{0-7}	$\overline{QZ_{0-8}} \rightarrow A_{0-8}$ ($\overline{AOE}$ = 0)

2594 tbl 04

IDT73211 B TO A DIRECTION WHEN SEL = 0

Input	Latch Y	PERRB	Reg. Z		Output	
			(QZ_8)	QZ_{0-8}	(A_8)	A_{0-8}
B_{0-8}	$B_{0-8} \rightarrow Y_{0-8}$ (LE = 1)	Result of even parity check	Even parity generated bit	$Y_{0-8} \rightarrow QZ_{0-8}$ ($\overline{CP}$ = Lo to Hi) ($\overline{BEN}$ = 0)	A_8 = Even parity generated from Y_{0-7}	$\overline{QZ_{0-8}} \rightarrow A_{0-8}$ ($\overline{AOE}$ = 0)

2594 tbl 05

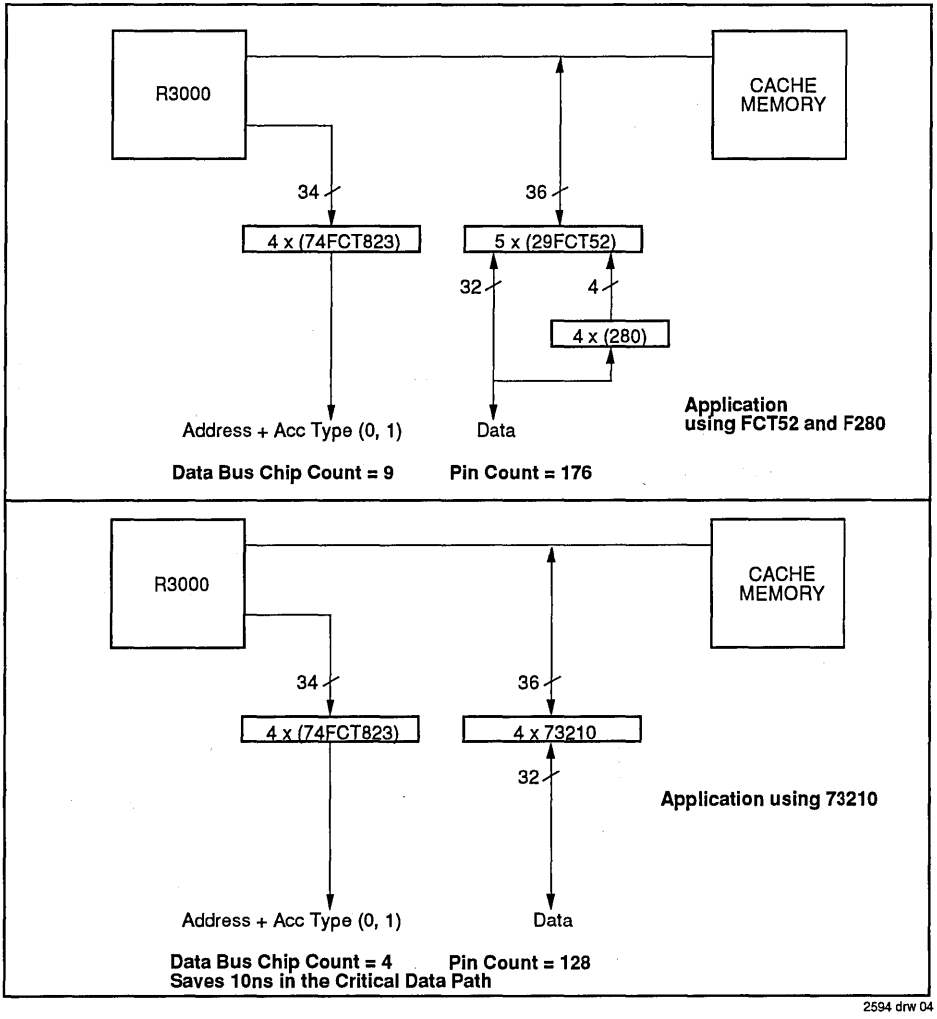

Figure 1. R3000 System with No Parity Support in Main Memory

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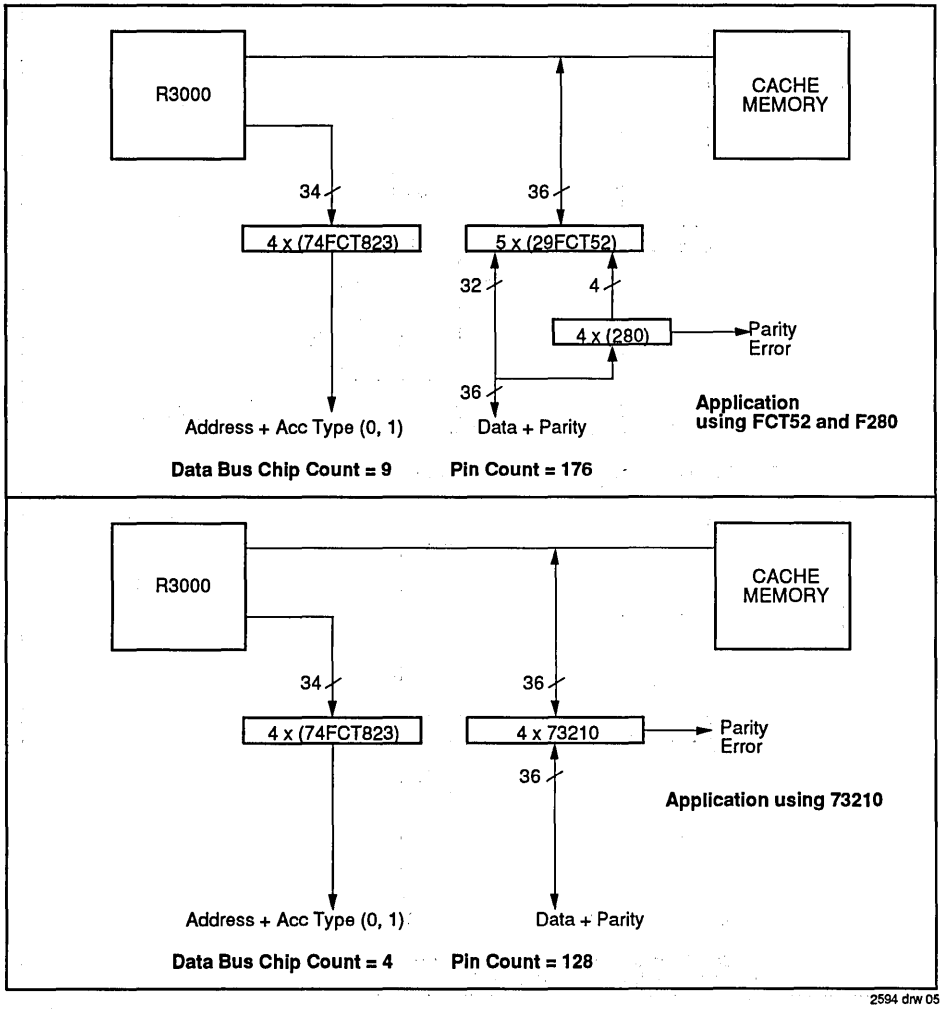


Figure 2. R3000 System with Parity Support in Main Memory

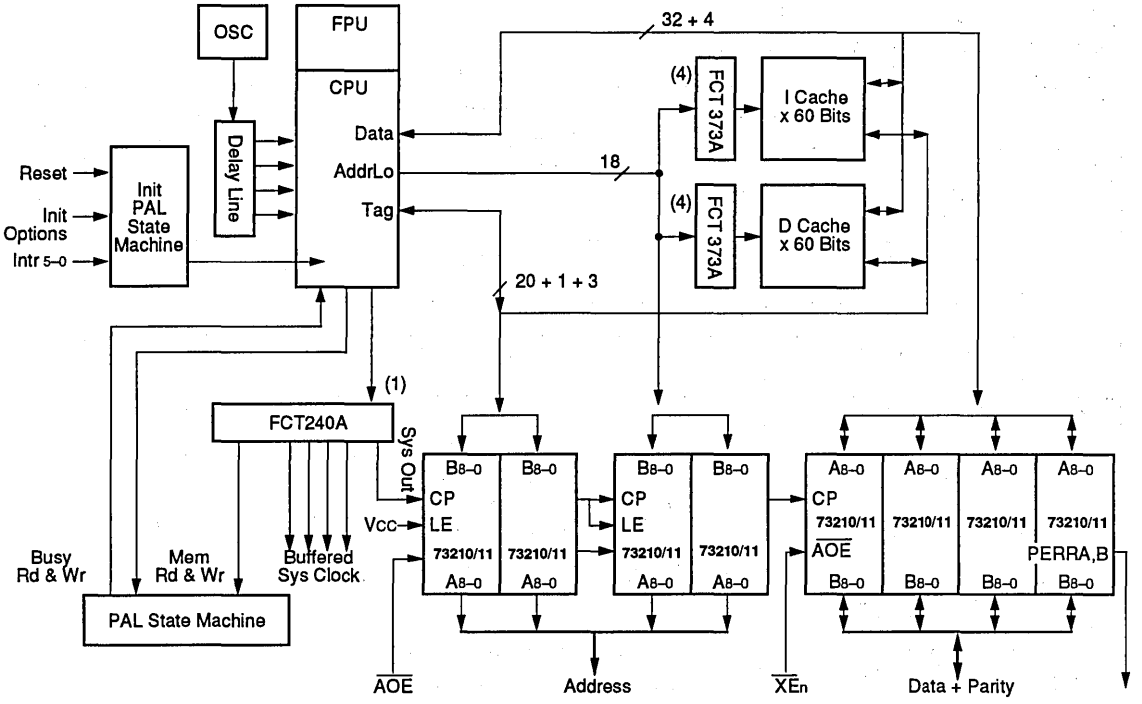


Figure 3. Read and Write Buffers Using Eight IDT73210/11

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to Ground	–0.5 to Vcc + 0.5	–0.5 to Vcc + 0.5	V
Vcc	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	1.2	1.5	W
IOUT	Total Output Current	200	250	mA

NOTE: 2594 tbl 06

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	5	pF
COUT	Output Capacitance	VOUT = 0V	7	pF
CI/O	Input – Output Capacitance	VOUT = 0V	7	pF

NOTE: 2594 tbl 07

1. This parameter is not production tested.

8

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

The following conditions apply unless otherwise specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level			2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level			—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.		Except I/O	—	—	10	µA
		V_I = 2.7V		I/O pins	—	—	20	
I_{IL}	Input LOW Current	V_{CC} = Max.		Except I/O	—	—	-10	µA
		V_I = 0.5V		I/O pins	—	—	-20	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = −18mA			—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		PERRA, PERRB	-30	—	-150	mA
				A_{0-8}, B_{0-8}	-20	—	-75	
V_{OH}	Output HIGH Voltage	V_{CC} = Min.		I_{OH} = −12mA MIL.	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}		I_{OH} = −15mA COM'L.				
V_{OL}	Output LOW Voltage	V_{CC} = Min.	A_{0-8}	I_{OL} = 48mA MIL.	—	0.3	0.55	V
		V_{IN} = V_{IH} or V_{IL}	B_{0-8}	I_{OL} = 64mA COM'L.				
		V_{CC} = Min.	PERRA	I_{OL} = 20mA MIL.				
		V_{IN} = V_{IH} or V_{IL}	PERRB	I_{OL} = 24mA COM'L.				
V_H	Input Hysteresis for CP only	V_{CC} = 5V			—	200	—	mV

NOTES: 2594 tbl 09

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, not production tested.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed 100 millisecond.

POWER SUPPLY CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.02	2.0	mA
I_{CCQT}	Quiescent Power Supply Current	V_{CC} = Max.	COM'L.	—	0.3	1.0	mA/
	TTL Inputs HIGH	V_{IN} = 3.4[3]	MIL.	—	0.3	1.5	Input
I_{CCD}	Dynamic Power Supply Current[3]	V_{CC} = Max. Outputs Disabled One input toggling 50% Duty Cycle	V_{IN} = V_{CC} or GND	—	0.25	0.50	mA/ MHz/ Input
I_C	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Disabled f_{CP} = 10 MHz 50% Duty Cycle f_i = 5 MHz	V_{IN} = V_{CC} or GND	—	18	30	mA

NOTES: 2594 tbl 08

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. This parameter is not directly testable but is derived for use in the total power supply calculation.
4. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
   I_C = I_{CCQC} + I_{CCQT} $D_H N_T$ + I_{CCD} (f_{CP}/2 + $f_i N_i$)
   I_{CCQC} = Quiescent Current
   I_{CCQT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at DH
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input frequency
   N_i = Number of Inputs at fi
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[1]

Commercial: T_A = 0°C to +70°C; V_{CC} = 5V ± 5%
Military: T_A = -55°C to +125°C; V_{CC} = 5V ± 10%,
C_L = 50pF; R_L = 500Ω

Parameter	Description	IDT73210/11				IDT73210A/11A				IDT73210B/11B				Unit
		Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PHL} t_{PLH}	Propagation Delay Clock to A_{0-8} ($\overline{AOE}$ = Low)	2.0	9.0	2.0	11.0	2.0	7.2	2.0	9.0	2.0	6.0	2.0	7.5	ns
t_{PHL} t_{PLH}	Propagation Del Clock to B_{0-8} ($\overline{BOE}$ = Low)	2.0	10.5	2.0	12.0	2.0	9.0	2.0	10.5	2.0	7.5	2.0	9.0	ns
t_{PHL} t_{PLH}	Propagation Delay CP to PERRA, PERRB	2.0	10.5	2.0	12.0	2.0	9.0	2.0	10.5	2.0	7.5	2.0	9.0	ns
t_{PHL} t_{PLH}	Propagation Delay POLARITY to B_8	2.0	9.5	2.0	11.0	2.0	8.5	2.0	9.5	2.0	7.0	2.0	8.5	ns
t_{PHL} t_{PLH}	Propagation Delay B_{0-8} to PERRB LE = High	2.0	10.0	2.0	11.5	2.0	9.0	2.0	10.0	2.0	7.5	2.0	9.0	ns
t_S	Set-up Time A_{0-8}, B_{0-8} (Reg Y-73210 only), POLARITY, SEL to CP	3.5	—	3.5	—	3.0	—	3.5	—	2.5	—	3.0	—	ns
t_H	Hold Time to CP — A_{0-8}, B_{0-8} (Reg Y-73210 only)	1.0	—	1.5	—	1.0	—	1.5	—	1.0	—	1.5	—	ns
	Hold Time to CP — POLARITY, SEL	1.5	—	2.0	—	1.5	—	2.0	—	1.5	—	2.0	—	ns
t_S	Set-up Time $\overline{AEN}$, $\overline{BEN}$ to CP	3.5	—	3.5	—	3.0	—	3.5	—	2.5	—	3.0	—	ns
t_H	Hold Time $\overline{AEN}$, $\overline{BEN}$ to CP	1.5	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_S	Set-up Time B_{0-8} to LE	3.5	—	3.5	—	3.0	—	3.5	—	2.5	—	3.0	—	ns
t_H	Hold Time B_{0-8} to LE	1.5	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_S	Set-up Time B_{0-8} to CP (Reg Z); LE = High	4.5	—	5.0	—	3.5	—	4.5	—	3.0	—	3.5	—	ns
t_H	Hold Time B_{0-8} to CP (Reg Z); LE = High	1.5	—	3.0	—	1.5	—	2.5	—	1.5	—	2.0	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{AOE}$ to A_{0-8}, $\overline{BOE}$ to B_{0-8}	2.0	8.0	2.0	10.0	2.0	7.0	2.0	8.0	2.0	6.0	2.0	7.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{AOE}$ to A_{0-8}, $\overline{BOE}$ to B_{0-8}	2.0	7.5	2.0	9.0	1.5	7.0	1.5	7.5	1.5	6.0	1.5	6.5	ns
t_{PWH}	Clock Pulse Width High[2]	5.0	—	5.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns
t_{PWL}	Clock Pulse Width Low[2]	5.0	—	5.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns

NOTES:
1. All minimum limits for propagation delays are guaranteed but not tested.
2. This parameter is guaranteed but not tested.

2594 tbl 10

8

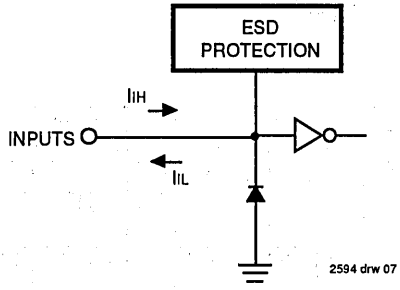


Figure 4. Input Interface Circuit

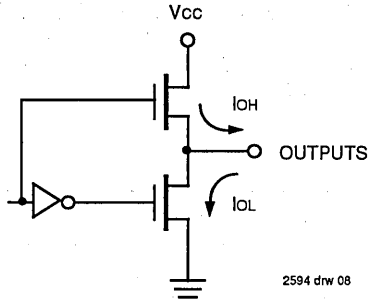
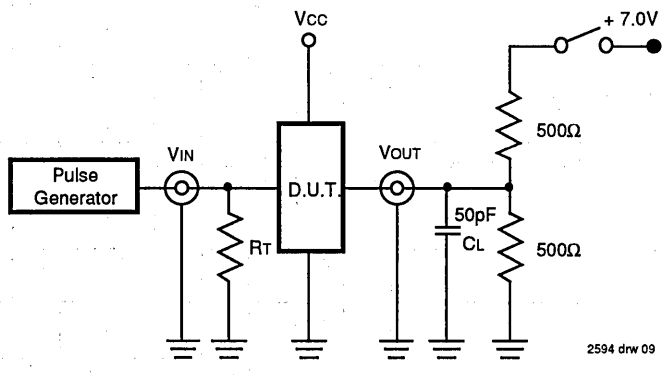


Figure 5. Output Interface Circuit



DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

Figure 6. AC Test Load Circuit

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 6

2594 tbl 12

Test	Switch
Disable Low Enable Low	Closed
All other Tests	Open

2594 tbl 13

Integrated Device Technology, Inc.

16-BIT TRI-PORT BUS EXCHANGER

IDT73720/A

FEATURES:

- High-speed 16-bit bus exchange for interbus communication in the following environments:
  - — Multi-way interleaving memory
  - — Multiplexed address and data busses
- Direct interface to R3051 family RISChipSet™
  - — R3051™ family of integrated RISController™ CPUs
  - — R3721 DRAM controller
- Data path for read and write operations
- Low noise 12mA TTL level outputs
- Bidirectional 3-bus architecture: X, Y, Z
  - — One CPU bus: X
  - — Two (interleaved or banked) memory busses:Y & Z
  - — Each bus can be independently latched
- Byte control on all three busses
- Source terminated outputs for low noise and undershoot control
- 68-pin PLCC and 80-pin PQFP package
- High-performance CEMOS™ technology.

DESCRIPTION:

The IDT73720/A Bus Exchanger is a high speed 16-bit bus exchange device intended for inter-bus communication in interleaved memory systems and high performance multiplexed address and data busses.

The Bus Exchanger is responsible for interfacing between the CPU A/D bus (CPU address/data bus) and multiple memory data busses.

The 73720/A uses a three bus architecture (X, Y, Z), with control signals suitable for simple transfer between the CPU bus (X) and either memory bus (Y or Z). The Bus Exchanger features independent read and write latches for each memory bus, thus supporting a variety of memory strategies. All three ports support byte enable to independently enable upper and lower bytes.

FUNCTIONAL BLOCK DIAGRAM

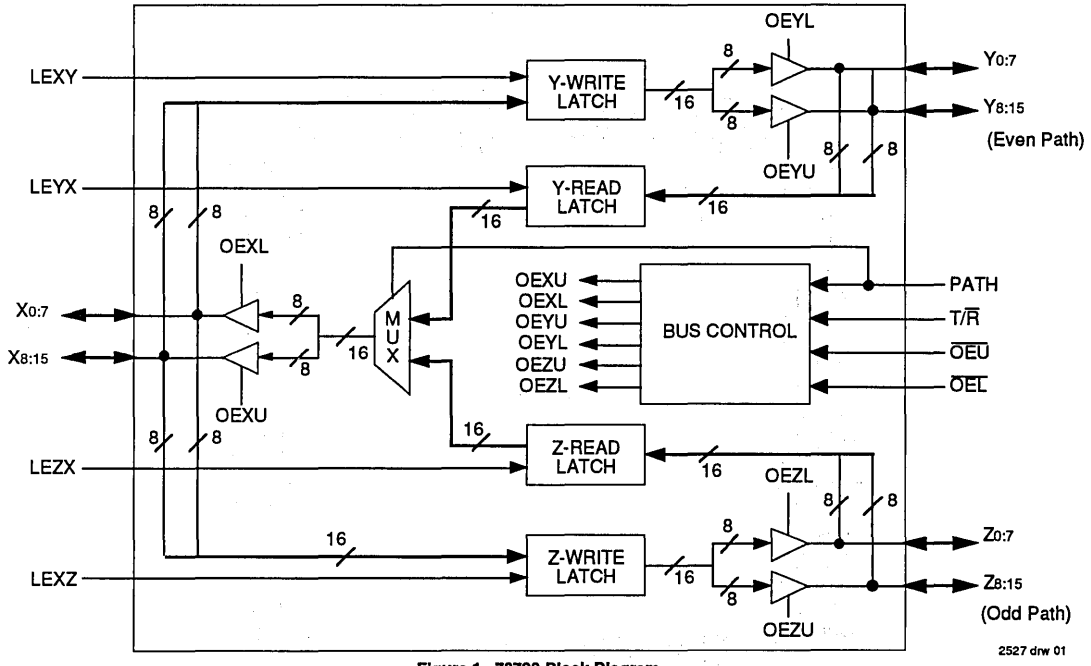


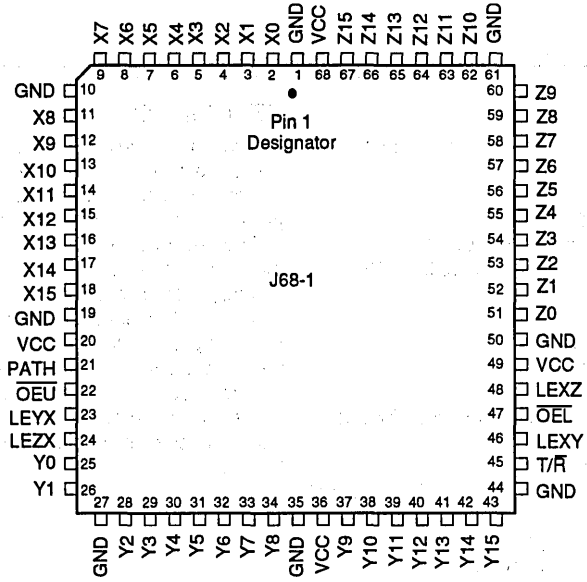
Figure 1. 73720 Block Diagram

NOTE:

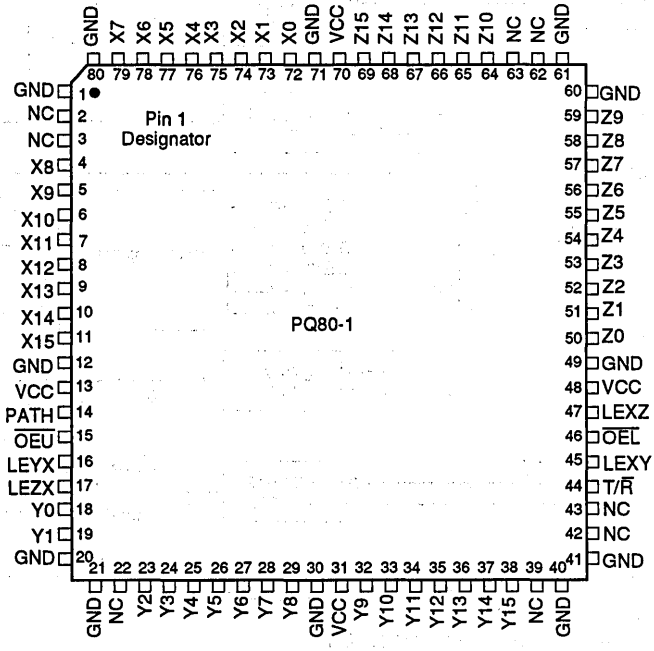
1. Logic equations for bus control:
   $OEXU = T/\overline{R}^* \cdot \overline{OEU}^*$; $OEXL = T/\overline{R}^* \cdot \overline{OEL}^*$; $OEYU = T/\overline{R} \cdot PATH \cdot \overline{OEU}^*$
   $OEYL = T/\overline{R} \cdot PATH \cdot \overline{OEL}^*$; $OEZU = T/\overline{R} \cdot PATH^* \cdot \overline{OEU}^*$; $OEZL = T/\overline{R} \cdot PATH^* \cdot \overline{OEL}^*$

CEMOS, RISChipSet, RISController, R305x, R3051, R3052 are trademarks of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



PLCC
TOP VIEW



PQFP
TOP VIEW

PIN DESCRIPTION

Signal	I/O	Description
X(0:15)	I/O	Bidirectional Data Port X. Usually connected to the CPU's A/D (Address/Data) bus.
Y(0:15)	I/O	Bidirectional Data port Y. Connected to the even path or even bank of memory.
Z(0:15)	I/O	Bidirectional Data port Z. Connected to the odd path or odd bank of memory.
LEXY	I	Latch Enable input for Y-Write Latch. The Y-Write Latch is open when LEXY is high. Data from the X-port (CPU) is latched on the high to low transition of LEXY
LEXZ	I	Latch Enable input for Z-Write Latch. The Z-Write Latch is open when LEXZ is high. Data from the X-port (CPU) is latched on the high to low transition of LEXZ.
LEYX	I	Latch Enable input for the Y-Read Latch. The Y-Read Latch is open when LEYX is high. Data from the even path Y is latched on the high to low transition of LEYX.
LEZX	I	Latch Enable input for the Z-Read Latch. The Z-Read Latch is open when LEZX is high. Data from the odd path Z is latched on the high to low transition of LEZX
PATH	I	Even/Odd Path Selection. When high, PATH enables data transfer between the X-Port and the Y-port (even path). When low, PATH enables data transfer between the X-Port and the Z-Port (odd path).
T/$\overline{R}$	I	Transmit/Receive Data. When high, Port X is an input Port and either Port Y or Z is an output Port. When low, Port X is an output Port while Ports Y & Z are input Ports
$\overline{OEU}$	I	Output Enable for Upper byte. When low, the Upper byte of data is transfered to the port specified by PATH in the direction specified by T/$\overline{R}$.
$\overline{OEL}$	I	Output Enable for Lower byte. When low, the Lower byte of data is transfered to the port specified by PATH in the direction specified by T/$\overline{R}$.

2527 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +125	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2527 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2527 tbl 04

1. This parameter is guaranteed by device characterization, but is not production tested.

TRUTH TABLE

Path	T/$\overline{R}$	$\overline{OEU}$	$\overline{OEL}$	Functionality
L	L	L	L	Z→X (16-bits)–Read Z(1)
L	H	L	L	X→Z (16 bits)–Write Z(1)
H	L	L	L	Y→X (16-bits)–Read Y(2)
H	H	L	L	X→Y (16 bits)–Write Y(2)
X	X	H	H	All output buffers are disabled
X	X	H	L	Transfer of lower 8 bits (0:7) as per PATH & T/$\overline{R}$
X	X	L	H	Transfer of upper 8 bits (8:15) as per PATH & T/$\overline{R}$

NOTES: 2527 tbl 01

1. For Z→X and X→Z transfers, Y-port output buffers are tristated.
2. For Y→X and X→Y transfers, Z-port output buffers are tristated.

8

ARCHITECTURE OVERVIEW

The Bus Exchanger is used to service both read and write operations between the CPU and the dual memory busses. It includes independent data path elements for reads from and writes to each of the memory banks (Y and Z). Data flow control is managed by a simple set of control signals, analogous to a simple transceiver. In short, the Bus Exchanger allows bidirectional communication between ports X and Y and ports X and Z as illustrated in figure 1.

The data path elements for each port include:

Read Latch: Each of the memory ports Y and Z contains a transparent latch to capture the contents of the memory bus. Each latch features an independent latch enable.

Write Latch: Each memory port Y and Z contains an independent latch to capture data from the CPU bus during writes. Each memory port write latch features an independent latch enable, allowing write data to be directed to a specific memory port without disrupting the other memory port.

Data Flow Control Signals

T/$\overline{R}$ (Transmit/$\overline{\text{Receive}}$). This signal controls the direction of data transfer. A transmit is used for CPU writes, and a receive is used for read operations.

$\overline{OEU}$, $\overline{OEL}$ are the output enable control signals to select upper or lower bytes of all three ports.

Path: The path control signal is used to select between the even memory path Y and the odd memory path Z during read or write operations. Path selects the memory port to be connected to the CPU bus (X-port), and is independent of the latch enable signals. Thus, it is possible to transfer data from one memory port to the CPU bus (X) while capturing data from the other memory port.

MEMORY READ OPERATIONS

Latch Mode

In this mode the read operation consists of two stages. During the first stage, the data present at the memory port is captured by the read latch for that memory port. During a subsequent stage, data is brought from a selected memory port to the CPU A/D port X by using output enable control.

The read operation is selected by driving T/$\overline{R}$ low. The read is managed using the Path input to select the memory port (Y or Z); the LEYX/LEZX enable the data capture into the corresponding Read Latch.

In this way, memory interleaving can be performed. While data from one bank is output onto the CPU bus, data on the other bank is captured in the other memory port. In the next cycle, the Path input is changed, enabling the next data element onto the CPU bus, while the first bank is presented with a new data element.

Transparent Mode

The Bus Exchanger may be used as a data transceiver by leaving all latches open or transparent.

Memory Write Operations

Memory write operations also consist of two distinct stages. During one stage, the write data is captured into the selected memory port write latch. During a later stage, the memory is presented on the memory port bus

The write operation is selected by driving T/$\overline{R}$ high. Writes are thus performed using the Path input to select the memory port (Y or Z). The LEXY/LEXZ capture data in the corresponding Write Latch.

Note that it is possible to utilize the bus exchanger's write resources as an additional write buffer, if desired; the CPU A/D bus can be freed up once the data has been captured by the Bus Exchanger.

APPLICATIONS

Use as Part of the R3051 Family ChipSet

Figure 2 shows the use of the Bus Exchanger in a typical R3051 based system.

In write transactions, the R3051 drives data on the CPU bus. The latch enables are held open through the entire write; thus, the bus exchanger is used like a transceiver. The appropriate LEXY/LEXZ signal is derived from ALE (Logic low- indicating that the processor is driving data) and the low order address bit. The rising edge of $\overline{Wr}$ from the CPU, ends the write operation.

During read transactions, the memory system is responsible for generating the input control signals to cause data to be captured at the memory ports. The memory controller is also responsible for acknowledging back to the CPU that the data is available, and causing the appropriate path to be selected.

The R3721 DRAM controller for the R3051 family uses the transparent latches of the read ports. The R3721 directly controls the inputs of the bus exchanger, during both reads and writes. Consult the R3721 data sheet for more information on these control signals.

Use in a general 32-bit System

Figures 3 and 4 illustrate the use of the Bus Exchanger in a 32-bit microprocessor based system. Note the reduced pin count achieved with the Bus Exchanger.

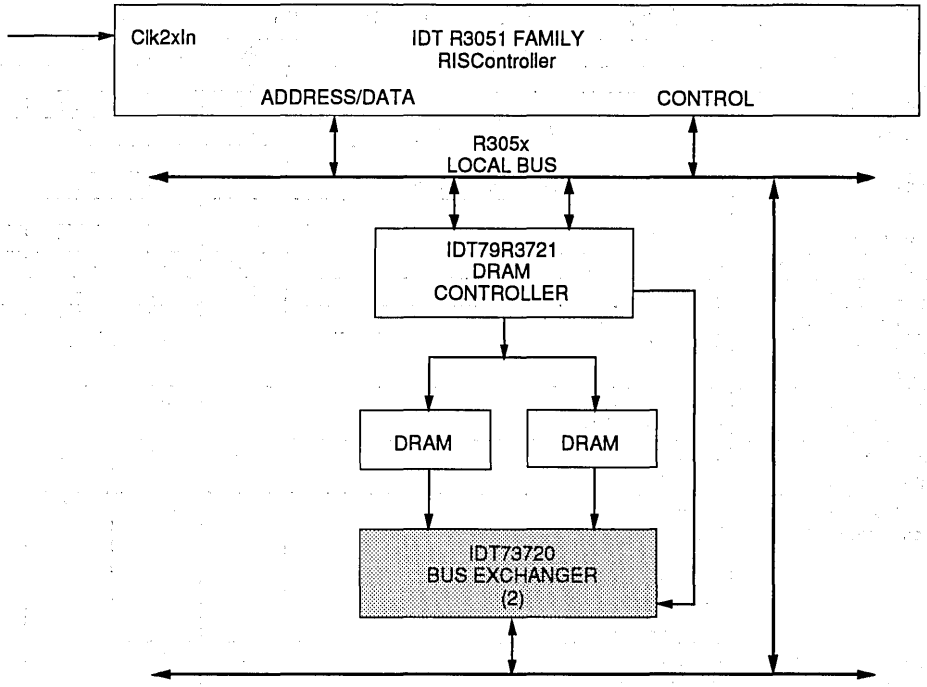
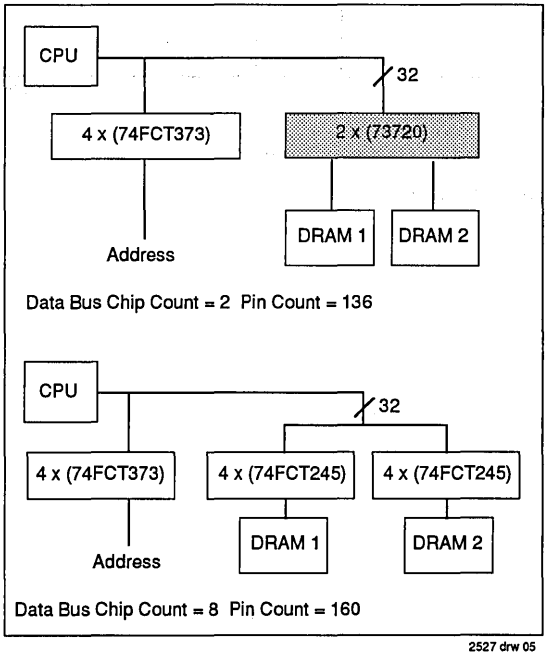


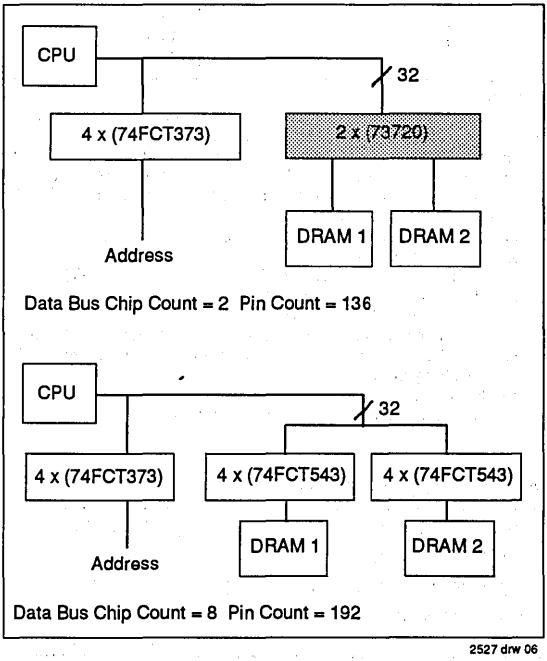
Figure 2. Bus Exchanger Used in R3051 Family System

2527 drw 04



2527 drw 05

Figure 3. CPU System with Transparent Data Path (2-way Interleaving)



2527 drw 06

Figure 4. CPU System with Latched Data Path (2-way Interleaving)

8

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level			2.0	—	—	V
V_{IL}	Input LOW Level			—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IH} = 2.7V	Inputs only	—	—	5.0	µA
			I/O pins	—	—	5.0	
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IL} = 0.5V	Inputs only	—	—	-5.0	µA
			I/O pins	—	—	-5.0	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = -18mA		—	-0.7	-1.2	V
I_{OS}[3]	Short Circuit Current	V_{CC} = Max., V_O = GND		-60.0	—	-200.0	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OH} = -12mA		2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OL} = 12mA		—	0.3	0.5	V
V_H	Input Hysteresis All inputs	V_{CC} = 5V		—	200.0	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} =3.4 V[4]		—	0.5	2.0	mA/ Input
I_{CCD}	Dynamic Power Supply Current[5]	V_{CC} = Max. V_{IN} = V_{CC} or GND Outputs Disabled $\overline{OE}$ = V_{CC} One Input Toggling 50 % Duty Cycle		—	0.25	0.5	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. V_{IN} = V_{CC} or GND Outputs Disabled 50 % Duty Cycle $\overline{OE}$ = V_{CC} fi = 10MHz One Bit Toggling		—	2.7	6.5	mA

2527 tbl 05

NOTES:

1. For conditions shown as max. or min., use appropriate V_{CC} value.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megaherz.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 5

2527 tbl 06

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0° to +70°C)

Symbol	Parameter	Test Conditions[1]	73720A		73720		Units
			Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	X to Y & X to Z Latches enabled	C_L = 50pF R_L = 500 Ohms	—	—	2.0	7.5	ns
tPLH tPHL	Y to X & Z to X Latches enabled		—	—	2.0	7.5	ns
tPLH tPHL	Latch Enable to Y & Z Port LEXY to Y LEXZ to Z		—	—	2.0	8.5	ns
tPLH tPHL	Latch Enable to X LEYX to X LEZX to X		—	—	2.0	8.5	ns
tPLH tPHL	Path to X Port Propagation Delay		—	—	2.0	8.5	ns
tHZ tLZ	Y & Z Port Disable Time (T/$\overline{R}$, PATH, $\overline{OEU}$, $\overline{OEL}$)[3]		—	—	2.0	9.5	ns
tZH tZL	Y & Z Port Enable Time (T/$\overline{R}$, PATH, $\overline{OEU}$, $\overline{OEL}$)[3]		—	—	2.0	10.5	ns
tHZ tLZ	X-Port DisableTime (T/$\overline{R}$, $\overline{OEU}$, $\overline{OEL}$)[3]		—	—	2.0	9.5	ns
tZH tZL	X-Port Enable Time (T/$\overline{R}$, $\overline{OEU}$, $\overline{OEL}$)[3]		—	—	2.0	10.5	ns
tSU	Port to LE Set-up time		—	—	2.0	—	ns
tH	Port to LE Hold time		—	—	1.5	—	ns

NOTES:
1. All timings are referenced to 1.5 V.
2. This parameter is guaranteed by design, but not tested.
3. Bus turnaround times are guaranteed by design, but not tested. (T/$\overline{R}$ enable/disable times).

2527 tbl 07

TEST CIRCUITS AND WAVEFORMS

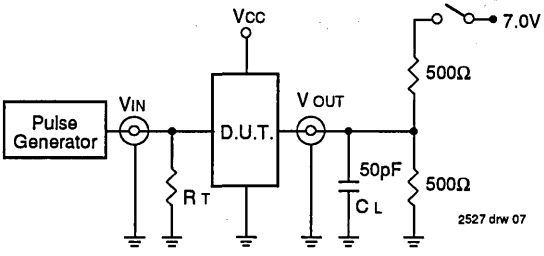


Figure 5. Test Circuit for all outputs

SWITCH POSITION

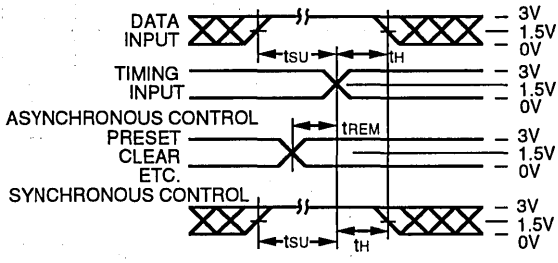
Test	Switch
Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

2527 tbl 08

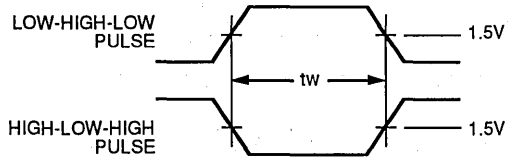
8

SET-UP, HOLD AND RELEASE TIMES



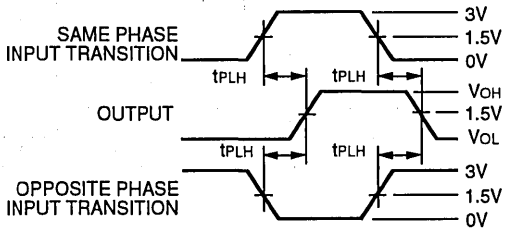
2527 drw 08

PULSE WIDTH



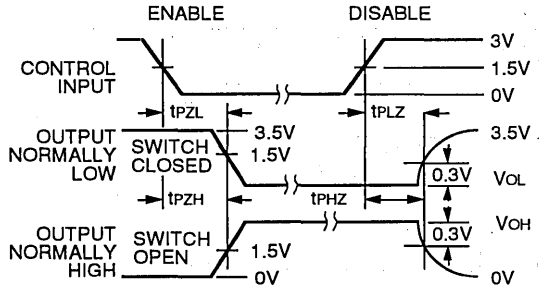
2527 drw 09

PROPAGATION DELAY



2527 drw 10

ENABLE AND DISABLE TIMES



2527 drw 11

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; ZO ≤ 50Ω; tF ≤ 2.5ns; tR ≤ 2.5ns.

Integrated Device Technology, Inc.

16-BIT CMOS ERROR DETECTION AND CORRECTION UNIT

IDT39C60
IDT39C60–1
IDT39C60A
IDT39C60B

FEATURES

- Low-power CEMOS™
  - — Military: 100mA (max.)
  - — Commercial: 85mA (max.)
- Fast
  - — Data in to Error Detect
    IDT39C60B: 18ns (max.), IDT39C60A: 20ns (max.)
    IDT39C60–1: 25ns (max.), IDT39C60: 32ns (max.)
  - — Data in to Corrected Data out
    IDT39C60B: 25ns (max.), IDT39C60A: 30ns (max.)
    IDT39C60–1: 52ns (max.), IDT39C60: 65ns (max.)
- Improves system memory reliability
  - — Corrects all single-bit errors, detects all double and some triple-bit errors
- Cascadable
  - — Data words up to 64 bits
- Built-in diagnostics
  - — Capable of verifying proper EDC operation via software control
- Simplified byte operations
  - — Fast byte writes possible with separate byte enables
- Available in 48-pin DIP, 52-pin PLCC and LCC
- Pin-compatible to all versions of the AMD2960
- Military product available compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-88613 available for this function

DESCRIPTIONS

The IDT39C60 family are high-speed, low-power, 16-bit Error Detection and Correction Units which generate check-bits on a 16-bit data field according to a modified Hamming Code and correct the data word when checkbits are supplied. When performing a read operation from memory, the IDT39C60s will correct 100% of all single bit errors, will detect all double bit errors and some triple bit errors.

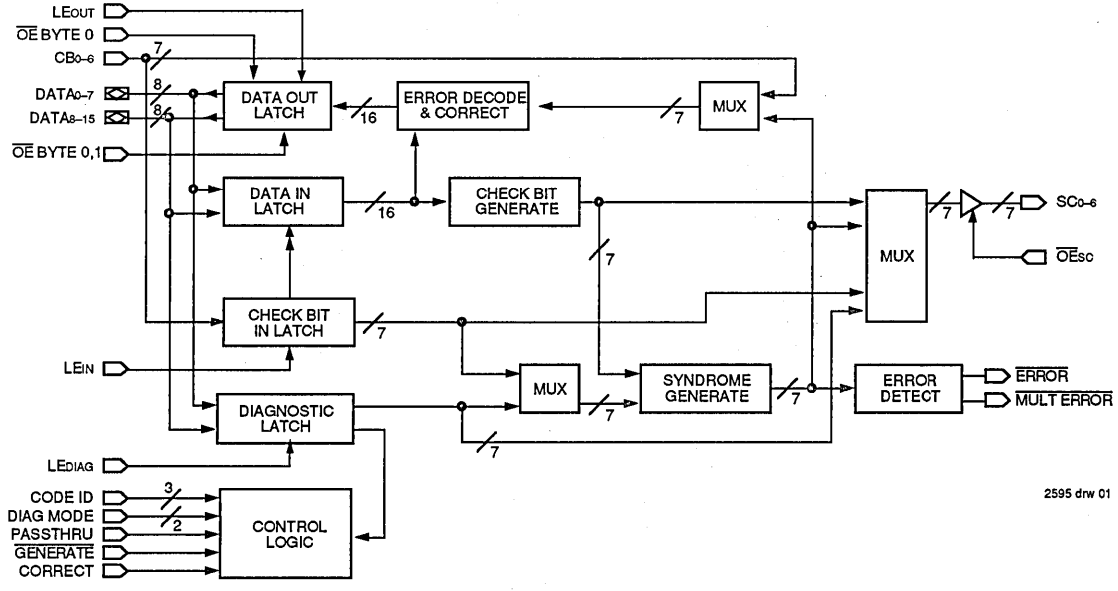
The IDT39C60s are easily cascadable from 16 bits up to 64 bits. Sixteen-bit systems use 6 check bits, 32-bit systems use 7 check bits and 64-bit systems use 8 check bits. For all three configurations, the error syndrome is made available.

All parts incorporate 2 built-in diagnostic modes. Both simplify testing by allowing for diagnostic data to be entered into the device and to execute system diagnostic functions.

The IDT39C60s are pin-compatible, performance-enhanced functional replacements for all versions of the 2960. They are fabricated using CEMOS, a CMOS technology designed for high-performance and high-reliability. The devices are packaged in either 48-pin DIPs and 52-pin PLCC and LCCs.

Military grade product is manufactured in compliance to the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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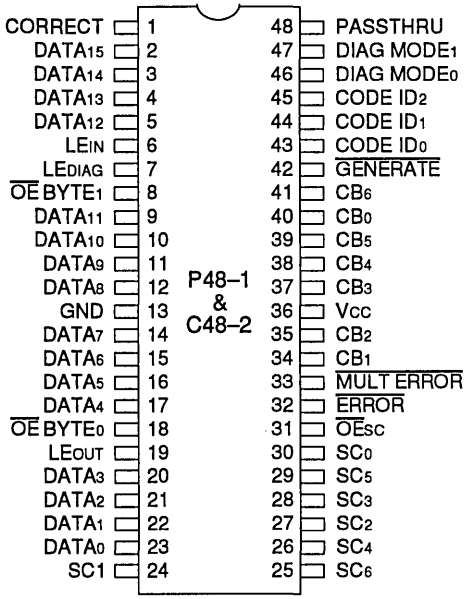
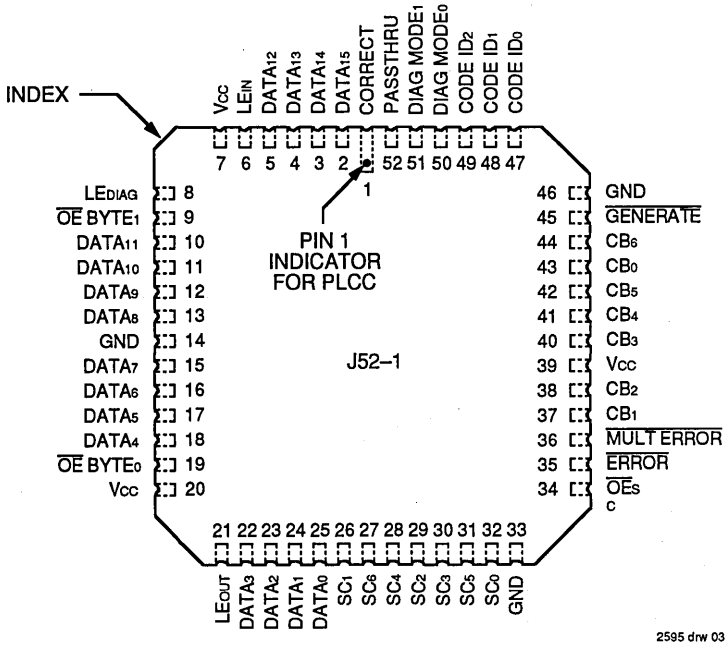
PIN CONFIGURATIONS



2595 drw 02

DIP
TOP VIEW
(600 mil x 100 mil Centers)



2595 drw 03

PLCC
TOP VIEW
(750 mil x 750 mil Centers)

PIN DESCRIPTIONS

Pin Name	I/O	Description
$DATA_{0-15}$	I/O	16 bidirectional data lines provide input to the Data Input Latch and receive output from the Data Output Latch. $DATA_0$ is the least significant bit; $DATA_{15}$ the most significant.
CB_{0-6}	I	Seven check bit input lines are used to input check bits for error detection. Also used to input syndrome bits for error correction in 32- and 64-bit configurations.
LE_{IN}	I	Latch Enable — Data Input Latch. Controls latching of the input data. When HIGH, the Data Input Latch and Check Bit Input Latch follow the input data and input check bits. When LOW, the Data Input Latch and Check Bit Input Latch are latched to their previous state.
$\overline{GENERATE}$	I	Generate Check Bits input. When this input is LOW, the EDC is in the Check Bit Generate mode. When HIGH, the EDC is in the Detect mode or Correct mode. In the Generate mode, the circuit generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs. In the Detect or Correct modes the EDC detects single and multiple errors and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In Correct mode, single-bit errors are also automatically corrected — corrected data is placed at the input of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates, in a coded form, the number of errors and the bit-in-error.
SC_{0-6}	O	Syndrome/Check Bit outputs hold the check/partial check bits when the EDC is in Generate mode and will hold the syndrome/partial syndrome bits when the device is in Detect or Correct modes. These are 3-state outputs.
$\overline{OE}_{SC}$	I	Output Enable — Syndrome/Check Bits. When LOW, the 3-state output lines SC_{0-6} are enabled. When HIGH, the SC outputs are in the high impedance state.
$\overline{ERROR}$	O	Error Detected output. When the EDC is in Detect or Correct mode, this output will go LOW if one or more syndrome bits are asserted, meaning there are one or more bit errors in the data or check bits. If no syndrome bits are asserted, there are no errors detected and the output will be HIGH. In Generate mode, $\overline{ERROR}$ is forced HIGH. (In a 64-bit configuration, $\overline{ERROR}$ must be implemented externally.)
$\overline{MULT\ ERROR}$	O	Multiple Errors Detected output. When the EDC is in Detect or Correct mode this output, if LOW, indicates that there are two or more bit errors that have been detected. If HIGH, this indicates that either one or no errors have been detected. In Generate mode, $\overline{MULT\ ERROR}$ is forced HIGH. (In a 64-bit configuration, $\overline{MULT\ ERROR}$ must be implemented externally.)
CORRECT	I	Correct input. When HIGH, this signal allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it into the Data Output Latch. When LOW, the EDC will drive data directly from the Data Input Latch to the Data Output Latch without correction.
LE_{OUT}	I	Latch Enable — Data Output Latch. Controls the latching of the Data Output Latch. When LOW, the Data Output Latch is latched to its previous state. When HIGH, the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct mode, single-bit errors are corrected by the network before loading into the Data Output Latch. In Detect mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The inputs to the Data Output Latch are disabled with its contents unchanged if the EDC is in Generate mode.
$\overline{OE}\ BYTE_0$ $\overline{OE}\ BYTE_1$	I	Output Enable — Bytes 0 and 1, Data Output Latch controls the 3-state outputs for each of the two bytes of the Data Output Latch. When LOW, these lines enable the Data Output Latch and, when HIGH, these lines force the Data Output Latch into the high impedance state. The two enable lines can be separately activated to enable only one byte of the Data Output at a time.
PASSTHRU	I	PASSTHRU input, when HIGH, forces the contents of the Check Bit Input Latch onto the Syndrome/Check Bit outputs (SC_{0-6}) and the unmodified contents of the Data Input Latch onto the inputs of the Data Output Latch.
$DIAG\ MODE_{0-1}$	I	Diagnostic Mode Select controls the initialization and diagnostic operation of the EDC.
$CODE\ ID_{0-2}$	I	Code Identification inputs identify the size of the total data word to be processed and which 16-bit slice of larger data words a particular EDC is processing. The three allowable data word sizes are 16, 32, and 64 bits and their respective modified Hamming Codes are designated 16/22, 32/39 and 64/72. Special CODE ID input 001 (ID_2, ID_1, ID_0) is also used to instruct the EDC that the signals $CODE\ ID_{0-2}$, $DIAG\ MODE_{0-1}$, CORRECT and PASSTHRU are to be taken from the diagnostic latch rather than the control lines.
LE_{DIAG}	I	Latch Enable — Diagnostic Latch. The Diagnostic Latch follows the 16-bit data on the input lines when HIGH. When LOW, the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits and internal control signals for $CODE\ ID_{0-2}$, $DIAG\ MODE_{0-1}$, CORRECT and PASSTHRU.

2595 tbl 01

8

PRODUCT DESCRIPTION

The IDT39C60 EDC Unit is a powerful 16-bit cascadable slice used for check bit generation, error detection, error correction and diagnostics. As shown in the Functional Block Diagram, the device consists of the following:

- Data Input Latch
- Data Output Latch
- Diagnostic Latch
- Check Bit Input Latch
- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic
- Error Correction Logic
- Control Logic

DATA INPUT/OUTPUT/DIAGNOSTIC LATCHES

The LE_{IN}, Latch Enable input, controls the Data Input which can load 16 bits of data from the bidirectional DATA lines. The input data is used for either check bit generation or error detection/correction.

The 16 bits of data from the DATA lines can be loaded into the Diagnostic Latch under control of the Diagnostic Latch Enable, LE_{DIAG}, giving check bit information in one byte and control information in the other byte. The Diagnostic Latch is used when in Internal Control mode or in one of the Diagnostics modes.

The Data Output Latch is split into two bytes and enabled onto the DATA lines through separate byte control lines. The Data Output Latch stores the result of an error correction operation or is loaded directly from the Data Input Latch under control of the Latch Enable Out (LE_{OUT}). The PASSTHRU control input determines which data is loaded.

CHECK BIT GENERATION LOGIC

This block of combinational logic generates 7 check bits using a modified Hamming Code from the 16 bits of data input from the Data Input Latch.

SYNDROME GENERATION LOGIC

This logic compares the check bits generated through the Check Bit Generator with either the check bits in the Check Bit Input Latch or 7 bits assigned in the Diagnostic Latch.

Syndrome bits are produced by an exclusive-OR of the two sets of bits. A match indicates no errors. If errors occur, the syndrome bits can be decoded to indicate the bit in error, whether 2 errors were detected or 3 or more errors.

ERROR DETECTION/CORRECTION LOGIC

The syndrome bits generated by the Syndrome Logic are decoded and used to control the $\overline{\text{ERROR}}$ and $\overline{\text{MULTERROR}}$ outputs. If one or more errors are detected, $\overline{\text{ERROR}}$ goes low. If two or more errors are detected, both $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ go low. Both outputs remain high when there are no errors detected.

For single bit errors, the correction logic will complement (correct) the bit in error, which can then be loaded into the Data Out Latches under the LE_{OUT} control. If check bit errors need to be corrected, then the device must be operated in the Generate mode.

CONTROL LOGIC

The control logic determines the specific mode of operation, usually from external control signals. However, the Internal Control mode allows these signals to be provided from the Diagnostic Latch.

DETAILED PRODUCT DESCRIPTION

The IDT39C60 EDC unit contains the logic necessary to generate check bits on a 16-bit data input according to a modified Hamming Code. The EDC can compare internally generated check bits against those read with the 16-bit data to allow correction of any single bit data error and detection of all double and some triple bit errors. The IDT39C60 can be used for 16-bit data words (6 check bits), 32-bit data words (7 check bits) or 64-bit data words (8 check bits).

CODE AND BYTE SELECTION

The 3 code identification pins, ID_{0-2}, are used to determine the data word size from 16, 32 or 64 bits and the byte position of each 16-bit IDT39C60 EDC device.

Code 16/22 refers to a 16-bit data field with 6 check bits.

Code 32/39 refers to a 32-bit data field with 7 check bits.

Code 64/72 refers to a 64-bit data field with 8 check bits.

The ID_{0-2} of 001 is used to place the device in the Internal Control mode as described later in this section.

Table 1 defines all possible identification codes.

CHECK AND SYNDROME BITS

The IDT39C60 provides either check bits or syndrome bits on the three-state output pins, SC_{0-6}. Check bits are generated from a combination of the Data Input bits, while syndrome bits are an Exclusive-OR of the check bits generated from read data with the read check bits stored with the data. Syndrome bits can be decoded to determine the single bit-in-error or that a double error was detected. Some triple bit errors are also detected. The check bits are labeled:

C_0, C_1, C_2, C_3, C_4	for the 8-bit configuration
$C_0, C_1, C_2, C_3, C_4, C_5$	for the 16-bit configuration
$C_0, C_1, C_2, C_3, C_4, C_5, C_6$	for the 32-bit configuration
$C_0, C_1, C_2, C_3, C_4, C_5, C_6, C_7$	for the 64-bit configuration

Syndrome bits are similarly labeled S_0 through S_7.

CONTROL MODE SELECTION

Tables 2 and 3 describe the 9 operating modes of the IDT39C60. The Diagnostic mode pins, DIAG MODE0-1, define 4 basic areas of operation, with $\overline{\text{GENERATE}}$, CORRECT and PASSTHRU, further dividing operation into 8 functions with the ID0-2 defining the ninth mode as the Internal mode.

Generate mode is used to display the check bits on the outputs SC0-6. The Diagnostic Generate mode displays check bits as stored in the Diagnostic Latch.

Detect mode provides an indication of errors or multiple errors on the outputs $\overline{\text{ERROR}}$ and $\overline{\text{MULTERROR}}$. Single bit errors are not corrected in this mode. The syndrome bits are provided on the outputs SC0-6. For the Diagnostic Detect mode, the syndrome bits are generated by comparing the internally generated check bits from the Data In Latch with check bits stored in the diagnostic latch rather than with the check bit latch contents.

Correct mode is similar to the Detect mode except that single bit errors will be complemented (corrected) and made available as input to the Data Out Latch. Again, the Diagnostic Correct mode will correct single bit errors as determined by syndrome bits generated from the Data Input and contents of the Diagnostic Latch.

The Initialize mode provides check bits for all zero bit data. Data In Latch is set and latched to a logic zero and made available as input to the Data Out Latch.

The Internal mode disables the external control pins DIAG MODE0-1, CORRECT, PASSTHRU and CODE ID to be defined by the Diagnostic Latch. When in the internal control mode, the data loaded into the diagnostic latch should have the CODE ID different from 001 as this would represent an invalid operation.

CODE ID_2	CODE ID_1	CODE ID_0	Hamming Code and Slice Selected
0	0	0	Code 16/22
0	0	1	Internal Control Mode
0	1	0	Code 32/39, Byte 0 and 1
0	1	1	Code 32/39, Byte 2 and 3
1	0	0	Code 64/72, Byte 0 and 1
1	0	1	Code 64/72, Byte 2 and 3
1	1	0	Code 64/72, Byte 4 and 5
1	1	1	Code 64/72, Byte 6 and 7

2595 tbl 02

Table 1. Hamming Code and Slice Identification

DIAG $MODE_1$	DIAG $MODE_2$	Diagnostic Mode Selected
0	0	**Non-diagnostic mode.** The EDC functions normally in all modes.
0	1	**Diagnostic Generate.** The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate mode. The EDC functions normally in the Detect or Correct modes.
1	0	**Diagnostic Detect/Correct.** In the Detect or Correct mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate mode.
1	1	**Initialize.** The outputs of the Data Input Latch are forced to zeroes and the check bits generated correspond to the all zero data. The latch is not reset, a functional difference from the Am2960.

2595 tbl 03

Table 2. Diagnostic Mode Control

8

Operating Mode	DM_1	DM_0	$\overline{GENERATE}$	CORRECT	PASS-THRU	$DATA_{OUT}$ Latch (LE_{OUT} = High)	SC_{0-6} ($\overline{OE}_{SC}$ = Low)	$\overline{ERROR}$ $\overline{MULT\ ERROR}$
Generate	0	0	0	X	0	—	Check Bits Generated from $DATA_{IN}$ Latch	High
	1	0						
Detect	0	0	1	0	0	$DATA_{IN}$ Latch	Syndrome Bits $DATA_{IN}$/ Check Bit Latch	Error Dep[1]
	0	1						
Correct	0	0	1	1	0	$DATA_{IN}$ Latch with Single Bit Correction	Syndrome Bits $DATA_{IN}$/ Check Bit Latch	Error Dep
	0	1						
PASSTHRU	0	0	X	X	1	$DATA_{IN}$ Latch	Check Bit Latch	High
	0	1						
	1	0						
Diagnostic Generate	0	1	0	X	0	—	Check Bits from Diagnostic Latch	High
Diagnostic Detect	1	0	1	0	0	$DATA_{IN}$ Latch	Syndrome Bits $DATA_{IN}$/ Diagnostic Latch	Error Dep
Diagnostic Correct	1	0	1	1	0	$DATA_{IN}$ Latch with Single Bit Correction	Syndrome Bits $DATA_{IN}$/ Diagnostic Latch	Error Dep
Initialization Mode	1	1	X	X	X	$DATA_{IN}$ Latch Set to 0000	Check Bits Generated from $DATA_{IN}$ Latch (0000)	—
Internal Mode	ID_{0-2} = 001 (Control Signals ID_{0-2}, $DIAG\ MODE_{0-1}$, CORRECT and PASSTHRU are taken from the Diagnostic Latch)							

NOTE: 2595 tbl 04

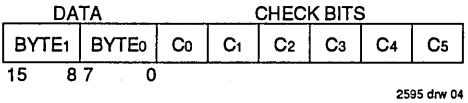
1. ERROR DEP (Error Dependent): $\overline{ERROR}$ will be low for single or multiple errors, with $\overline{MULT\ ERROR}$ low for double or multiple errors. Both signals are high for no errors.

Table 3. IDT39C60 Operating Modes

16-BIT DATA WORD CONFIGURATION

Figure 1 indicates the 22-bit data format for two bytes of data and 6 check bits.

A single IDT39C60 EDC unit, connected as shown in Figure 2, provides all the logic needed for single bit error correction and double bit error detection of a 16-bit data field. The identification code 16/22 indicates 6 check bits are required. The CB_6 pin is, therefore, a "Don't Care" and ID_2, ID_1, ID_0 = 000.



Uses Modified Hamming Code 16/22
16 Data Bits with 6 Check Bits

Figure 1. 16-Bit Data Format

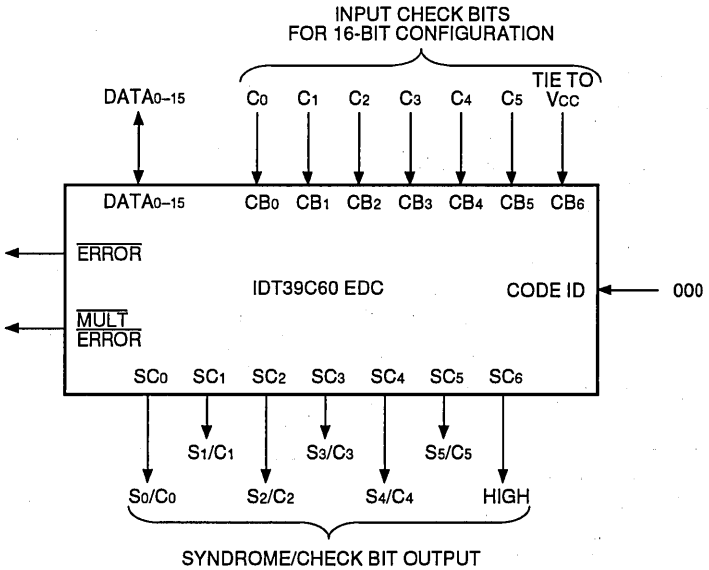


Figure 2. 16-Bit Configuration

Table 3 describes the operating modes available. The output pin SC_6, is forced high for either syndrome or check bits since only 6 check bits are used for the 16/22 code.

Table 4 indicates the data bits participating in the check bit generation. For example, check bit C_0 is the Exclusive-OR function of the 8 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization Mode. Check bits are passed as stored in the PASSTHRU or Diagnostic Generate Mode.

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example, SX is the XOR of check bits CX from those read with those generated. Table 5 indicates the decoding of the six syndrome bits to indicate the bit-in-error for a single bit error, or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Table 6 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the diagnostic check bits to determine syndrome bits or to pass as check bits to the SC_{0-5} outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

8

Generated Check Bits	Participating Data Bits[1]																
	Parity	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X

NOTE:
1. The check bit is generated as either an XOR or XNOR of the eight data bits noted by an "X" in the table.

2595 tbl 05

Table 4. 16-Bit Modified Hamming Code — Check Bit Encode Chart

					Hex	0	1	2	3
	Syndrome Bits			S_5		0	0	1	1
				S_4		0	1	0	1
Hex	S_3	S_2	S_1	S_0					
0	0	0	0	0		*	**C4**	**C5**	T
1	0	0	0	1		**C0**	T	T	**14**
2	0	0	1	0		**C1**	T	T	M
3	0	0	1	1		T	**2**	**8**	T
4	0	1	0	0		**C2**	T	T	**15**
5	0	1	0	1		T	**3**	**10**	T
6	0	1	1	0		T	**4**	**9**	T
7	0	1	1	1		M	T	T	M
8	1	0	0	0		**C3**	T	T	M
9	1	0	0	1		T	**5**	**11**	T
A	1	0	1	0		T	**6**	**12**	T
B	1	0	1	1		**1**	T	T	M
C	1	1	0	0		T	**7**	**13**	T
D	1	1	0	1		M	T	T	M
E	1	1	1	0		**0**	T	T	M
F	1	1	1	1		T	M	M	T

NOTES:
* = No errors detected
Number = The number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

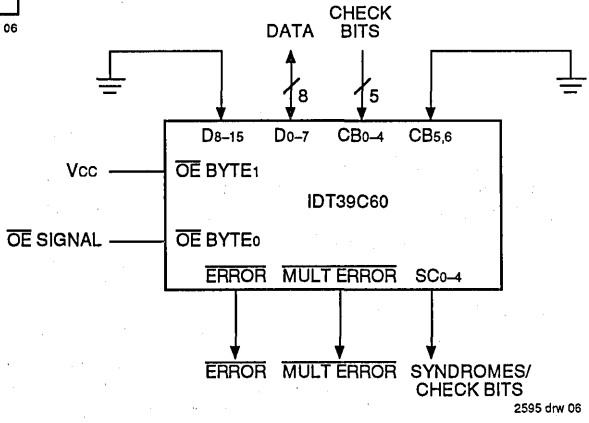
2595 tbl 06

Table 5. Syndrome Decode to Bit-In-Error (16-Bit Configuration)

Data Bit	Internal Function
0	Diagnostic Check Bit0
1	Diagnostic Check Bit1
2	Diagnostic Check Bit2
3	Diagnostic Check Bit3
4	Diagnostic Check Bit4
5	Diagnostic Check Bit5
6, 7	Don't Care
8	CODE ID0
9	CODE ID1
10	CODE ID2
11	DIAG MODE0
12	DIAG MODE1
13	CORRECT
14	PASSTHRU
15	Don't Care

2595 tbl 07

Table 6. Diagnostic Latch Loading — 16-Bit Format



2595 drw 06

Figure 3. 8-Bit Configuration

32-BIT DATA WORD CONFIGURATION

Two IDT39C60 EDC units, connected as shown in Figure 5, provide all the logic needed for single bit error correction and double bit error detection of a 32-bit data field. The identification code 32/39 indicates 7 check bits are required. Table 1 gives the ID2, ID1, ID0 values needed for distinguishing the byte 0/1 from byte 2/3. Valid syndrome, check bits and the $\overline{\text{ERROR}}$ and $\overline{\text{MULTERROR}}$ signal come from the byte 2/3 unit. Control signals not indicated are connected to both units in parallel. The $\overline{\text{OE}}$sc always enables the SC0–6 outputs of byte 0/1, but must be used to select data check bits or syndrome bits fed back from the byte 2/3 for data correction modes.

Data In bits 0 through 15 are connected to the same numbered inputs of the byte 0/1 EDC unit, while Data In bits 16 through 31 are connected to byte 2/3 Data Inputs 0 to 15, respectively.

Figure 4 indicates the 39-bit data format for 4 bytes of data and 7 check bits. Check bits are input to the byte 0/1 unit through a tri-state buffer unit such as the IDT74FCT244. Correction of single bit errors of the 32-bit configuration requires a feedback of sydrome bits from byte 2/3 into the byte 0/1 unit. The MUX shown on the functional block diagram is used to select the CB0–6 pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 describes the operating mode available for the 32/39 configuration.

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example, Sn is the XOR of check bits Cn from those read with those generated. Table 7 indicates the decoding of the seven syndrome bits to determine the bit-in-error for a single bit error, or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Performance data is provided in Table 8 in relating a single IDT39C60 EDC with the two cascaded units of Figure 5. As indicated, a summation of propagation delays is required from the cascading arrangement of EDC units.

Table 9 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic check bits to determine syndrome bits or to pass as check bits to the SC0–6 outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

Table 10 indicates the data bits participating in the check bit generation. For example, check bit C0 is the Exclusive-OR function of the 16 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization Mode. Check bits are passed as stored in the PASSTHRU or Diagnostic Generate Mode.

					Hex	0	1	2	3	4	5	6	7
					S6	0	0	0	0	1	1	1	1
	Syndrome Bits				S5	0	0	1	1	0	0	1	1
					S4	0	1	0	1	0	1	0	1
Hex	S3	S2	S1	S0									
0	0	0	0	0		*	C4	C5	T	C6	T	T	30
1	0	0	0	1		C0	T	T	14	T	M	M	T
2	0	0	1	0		C1	T	T	M	T	2	24	T
3	0	0	1	1		T	18	8	T	M	T	T	M
4	0	1	0	0		C2	T	T	15	T	3	25	T
5	0	1	0	1		T	19	9	T	M	T	T	31
6	0	1	1	0		T	20	10	T	M	T	T	M
7	0	1	1	1		M	T	T	M	T	4	26	M
8	1	0	0	0		C3	T	T	M	T	5	27	T
9	1	0	0	1		T	21	11	T	M	T	T	M
A	1	0	1	0		T	22	12	T	1	T	T	M
B	1	0	1	1		17	T	T	M	T	6	28	T
C	1	1	0	0		T	23	13	T	M	T	T	M
D	1	1	0	1		M	T	T	M	T	7	29	T
E	1	1	1	0		16	T	T	M	T	M	M	T
F	1	1	1	1		T	M	M	T	0	T	T	M

NOTES: 2595 tbl 08
* = No errors detected
Number = The number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

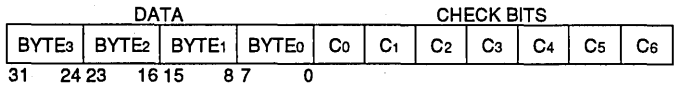
Table 7. Syndrome Decode to Bit-In-Error (32-Bit Configuration)

32-Bit Propagation Delay		Component Delay From IDT39C60
From	To	AC Specifications
DATA	Check Bits Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA	Corrected DATAOUT	(DATA to SC) + (CB to SC, CODE ID 011) + CB to DATA, CODE ID 010)
DATA	Syndromes Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA	$\overline{\text{ERROR}}$ for 32 Bits	(DATA to SC) + (CB to $\overline{\text{ERROR}}$, CODE ID011)
DATA	$\overline{\text{MULT ERROR}}$ for 32 Bits	(DATA to SC) + (CB to $\overline{\text{MULT ERROR}}$, CODE ID 011)

2595 tbl 09

Table 8. Key AC Calculations for the 32-Bit Configuration

8



Uses Modified Hamming Code 32/39
32 Data Bits with 7 Check Bits

Figure 4. 32-Bit Data Format

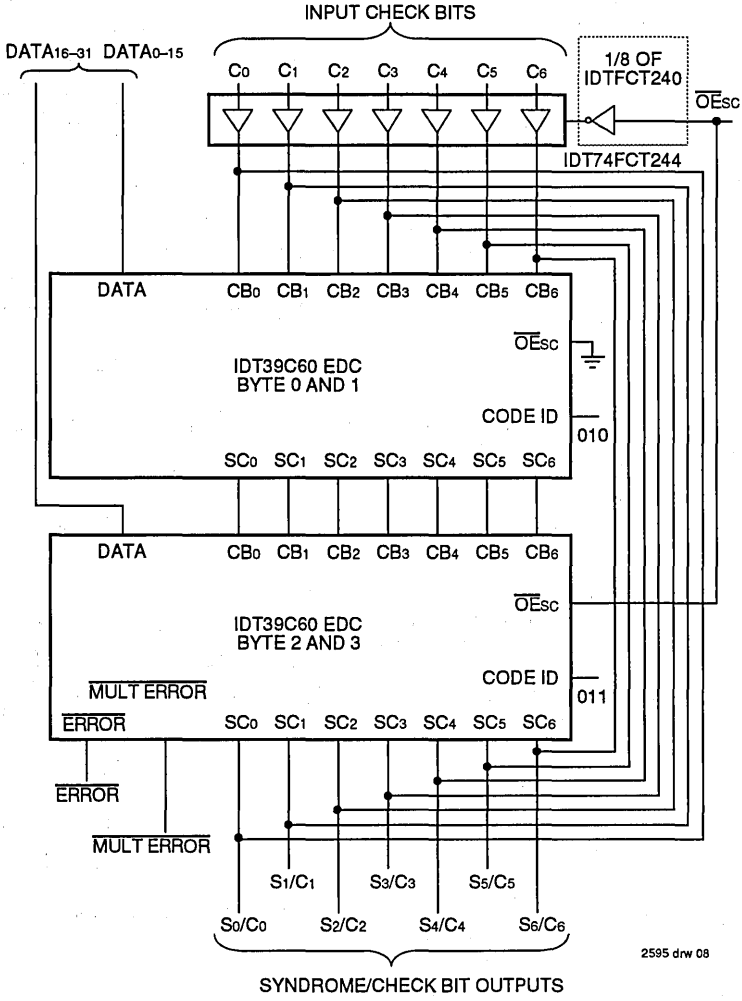


Figure 5. 32-Bit Configuration

Data Bit	Internal Function
0	Diagnostic Check Bit$_0$
1	Diagnostic Check Bit$_1$
2	Diagnostic Check Bit$_2$
3	Diagnostic Check Bit$_3$
4	Diagnostic Check Bit$_4$
5	Diagnostic Check Bit$_5$
6	Diagnostic Check Bit$_6$
7	Don't Care
8	Slice 0/1 — CODE ID$_0$
9	Slice 0/1 — CODE ID$_1$
10	Slice 0/1 — CODE ID$_2$
11	Slice 0/1 — DIAG MODE$_0$
12	Slice 0/1 — DIAG MODE$_1$
13	Slice 0/1 — CORRECT
14	Slice 0/1 — PASSTHRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 — CODE ID$_0$
25	Slice 2/3 — CODE ID$_1$
26	Slice 2/3 — CODE ID$_2$
27	Slice 2/3 — DIAG MODE$_0$
28	Slice 2/3 — DIAG MODE$_1$
29	Slice 2/3 — CORRECT
30	Slice 2/3 — PASSTHRU
31	Don't Care

2595 tbl 10

Table 9. Diagnostic Latch Loading — 32-Bit Format

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C_0	Even (XOR)	X				X		X	X	X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								

2595 tbl 11

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
C_0	Even (XOR)		X	X	X		X					X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X

2595 tbl 12

Table 10. 32-Bit Modified Hamming Code — Check Bit Encode Chart

8

64-BIT DATA WORD CONFIGURATION

The IDT39C60 EDC units connected with the MSI gates, as shown in Figure 7, provide all the logic needed for single bit error detection and double bit error detection of a 64-bit data field. The Identification code 64/72 is used, indicating 8 check bits are required. Check bits and Syndrome bits are generated external to the IDT39C60 EDC using Exclusive-OR gates. For error correction, the syndrome bits must be fed back to the CB_{0-6} inputs. Thus, external tri-state buffers are used to select between the check bits read in from memory and the syndrome bits being fed back.

The $\overline{ERROR}$ signal is low for one or more errors detected. From any of the 4 devices, $\overline{MULTERROR}$ is low for some double bit errors and for all three bit errors. Both are high otherwise. The DOUBLE ERROR signal is high only when a double bit error is detected.

Figure 6 indicates the 72-bit data format of 8 bytes of data and 8 check bits. Check bits are input to the various units through a tri-state buffer such as the IDT74FCT244. Correction of single bit errors of the 64-bit configuration requires a feedback of syndrome bits as generated external to the IDT39C60 EDC. The MUX shown on the functional block diagram is used to select the CB_{0-6} pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 describes the operating modes available for the 64/72 configuration.

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example, S_n is the XOR of check bits C_n from those read with those generated. Table 11 indicates the decoding of the 8 syndrome bits to determine the bit-in-error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

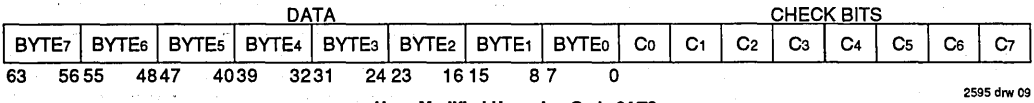
In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Performance data is provided in Table 12 in relating a single IDT39C60 EDC with the four units of Figure 7. Delay through the Exclusive-OR gates and the 3-state buffer must be included.

Table 13 indicates the Data Bits participating in the check bit generation. For example, check bit C_0 is the Exclusive-OR function of the 32 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization mode. In the PASSTHRU mode, the contents of the check bit latch are passed through the external Exclusive-OR gates and appear inverted at the outputs C_0 to C_7.

Table 14 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic Check Bits to determine syndrome bits or to pass as check bits to the SC_{0-6} outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

Some multiple errors will cause a data bit to be inverted. For example, in the 16-bit mode where bits 8 and 13 are in error, the syndrome 111100 (S_0, S_1, S_2, S_3, S_4, S_5) is produced. The bit-in-error decoder receives the syndrome 11100 (S_0, S_1, S_2, S_3, S_4) which it decodes as a single error in data bit 0 and inverts that bit. Figure 8 indicates a method for inhibiting correction when a multiple error occurs.



2595 drw 09

Uses Modified Hamming Code 64/72
32 Data Bits with 8 Check Bits

Figure 6. 64-Bit Data Format

					Hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
					S_7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
					S_6	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	1
	Syndrome Bits				S_5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
					S_4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Hex	S_3	S_2	S_1	S_0																	
0	0	0	0	0		*	C4	C5	T	C6	T	T	62	C7	T	T	46	T	M	M	T
1	0	0	0	1		C0	T	T	14	T	M	M	T	T	M	M	T	M	T	T	30
2	0	0	1	0		C1	T	T	M	T	34	56	T	T	50	40	T	M	T	T	M
3	0	0	1	1		T	18	8	T	M	T	T	M	M	T	T	M	T	2	24	T
4	0	1	0	0		C2	T	T	15	T	35	57	T	T	51	41	T	M	T	T	31
5	0	1	0	1		T	19	9	T	M	T	T	63	M	T	T	47	T	3	25	T
6	0	1	1	0		T	20	10	T	M	T	T	M	M	T	T	M	T	4	26	T
7	0	1	1	1		M	T	T	M	T	36	58	T	T	52	42	T	M	T	T	M
8	1	0	0	0		C3	T	T	M	T	37	59	T	T	53	43	T	M	T	T	M
9	1	0	0	1		T	21	11	T	M	T	T	M	M	T	T	M	T	5	27	T
A	1	0	1	0		T	22	12	T	33	T	T	M	49	T	T	M	T	6	28	T
B	1	0	1	1		17	T	T	M	T	38	60	T	T	54	44	T	1	T	T	M
C	1	1	0	0		T	23	13	T	M	T	T	M	M	T	T	M	T	7	29	T
D	1	1	0	1		M	T	T	M	T	39	61	T	T	55	45	T	M	T	T	M
E	1	1	1	0		16	T	T	M	T	M	M	T	T	M	M	T	0	T	T	M
F	1	1	1	1		T	M	M	T	32	T	T	M	48	T	T	M	T	M	M	T

NOTES:
* = No errors detected
Number = The number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

2595 tbl 13

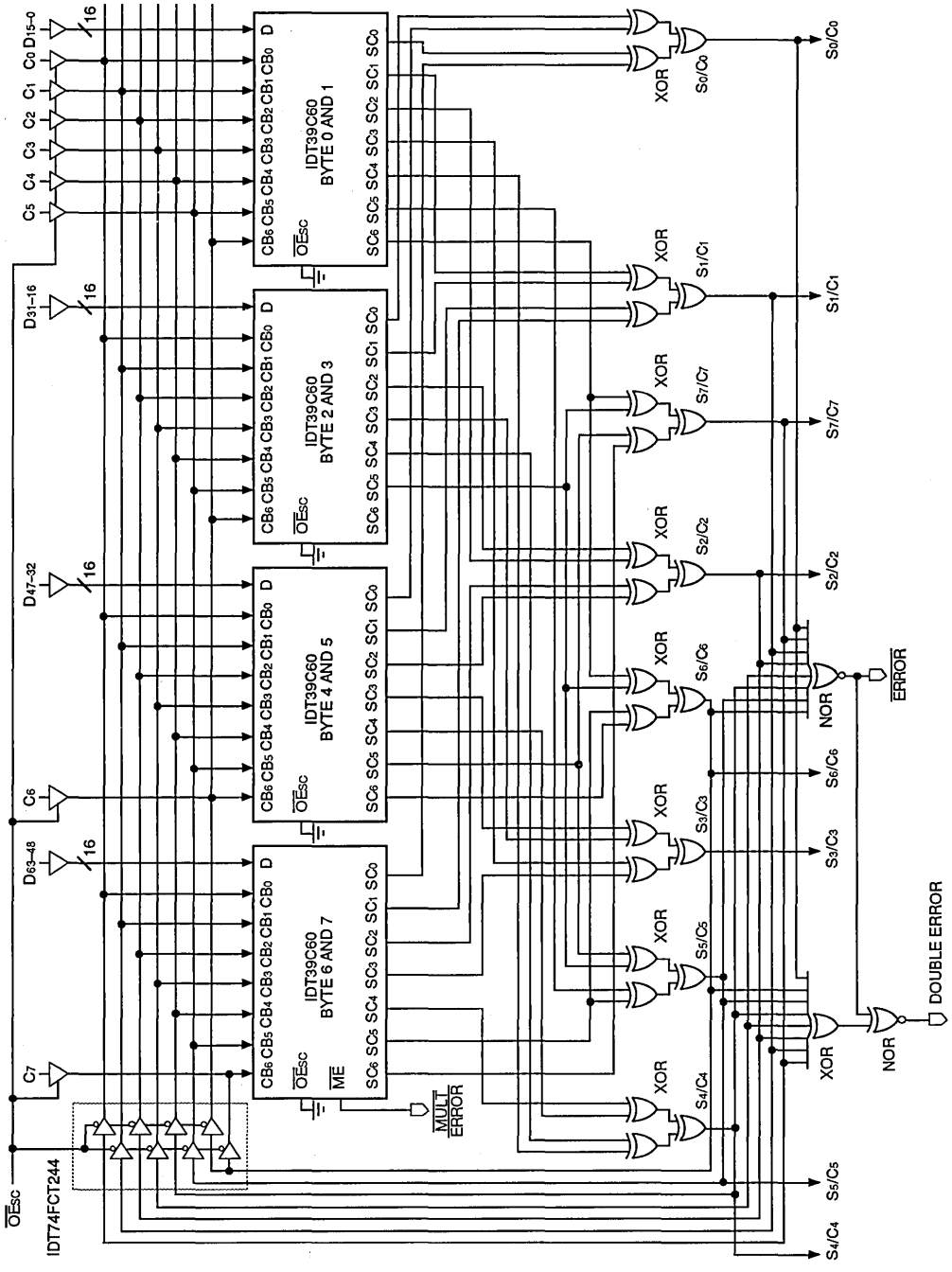
Table 11. Syndrome Decode to Bit-In-Error (64-Bit Configuration)

64-Bit Propagation Delay		Component Delay From IDT39C60
From	To	AC Specifications
DATA	Check Bits Out	(DATA to SC) + (XOR Delay)
DATA	Corrected $DATA_{OUT}$	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to DATA, CODE ID 1xx)
DATA	Syndromes	(DATA to SC) + (XOR Delay)
DATA	$\overline{ERROR}$ for 64 Bits	(DATA to SC) + (XOR Delay) + (NOR Delay)
DATA	$\overline{MULT\ ERROR}$ for 64 Bits	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to $\overline{MULT\ ERROR}$, CODE ID 1xx)
DATA	DOUBLE ERROR for 64 Bits	(DATA to SC) + (XOR Delay) + (XOR/NOR Delay)

2595 tbl 14

Table 12. Key AC Calculations for the 64-Bit Configuration

8



NOTES:
1. In PASSTHRU mode the contents of the Check Latch appears on the XOR outputs inverted.
2. In Diagnostic Generate mode the contents of the Diagnostic Latch appear on the XOR outputs inverted.

Figure 7. 64-Bit Configuration

Generated Check Bits	Parity	Participating Data Bits[1]															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								
C_7	Even (XOR)	X	X	X	X	X	X	X	X								

2595 tbl 15

Generated Check Bits	Parity	Participating Data Bits[1]															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X
C_7	Even (XOR)									X	X	X	X	X	X	X	X

2595 tbl 16

Generated Check Bits	Parity	Participating Data Bits[1]															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
C_0	Even (XOR)	X				X		X	X			X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								
C_7	Even (XOR)									X	X	X	X	X	X	X	X

2595 tbl 17

Generated Check Bits	Parity	Participating Data Bits[1]															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
C_0	Even (XOR)	X				X		X	X			X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X
C_7	Even (XOR)	X	X	X	X	X	X	X	X								

NOTE:
1. The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

2595 tbl 18

Table 13. 64-Bit Modified Hamming Code — Check Bit Encode Chart

8

Data Bit	Internal Function
0	Diagnostic Check Bit$_0$
1	Diagnostic Check Bit$_1$
2	Diagnostic Check Bit$_2$
3	Diagnostic Check Bit$_3$
4	Diagnostic Check Bit$_4$
5	Diagnostic Check Bit$_5$
6, 7	Don't Care
8	Slice 0/1 — CODE ID$_0$
9	Slice 0/1 — CODE ID$_1$
10	Slice 0/1 — CODE ID$_2$
11	Slice 0/1 — DIAG MODE$_0$
12	Slice 0/1 — DIAG MODE$_1$
13	Slice 0/1 — CORRECT
14	Slice 0/1 — PASSTHRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 — CODE ID$_0$
25	Slice 2/3 — CODE ID$_1$
26	Slice 2/3 — CODE ID$_2$
27	Slice 2/3 — DIAG MODE$_0$
28	Slice 2/3 — DIAG MODE$_1$
29	Slice 2/3 — CORRECT
30	Slice 2/3 — PASSTHRU

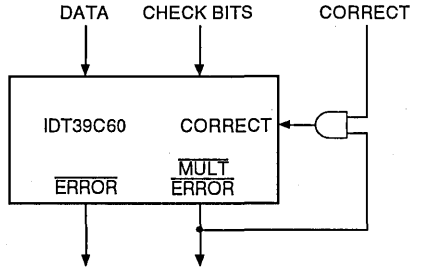
2595 tbl 19

Data Bit	Internal Function
31	Don't Care
32-37	Don't Care
38	Diagnostic Check Bit$_6$
39	Don't Care
40	Slice 4/5 — CODE ID$_0$
41	Slice 4/5 — CODE ID$_1$
42	Slice 4/5 — CODE ID$_2$
43	Slice 4/5 — DIAG MODE$_0$
44	Slice 4/5 — DIAG MODE$_1$
45	Slice 4/5 — CORRECT
46	Slice 4/5 — PASSTHRU
47	Don't Care
48-54	Don't Care
55	Diagnostic Check Bit$_7$
56	Slice 6/7 — CODE ID$_0$
57	Slice 6/7 — CODE ID$_1$
58	Slice 6/7 — CODE ID$_2$
59	Slice 6/7 — DIAG MODE$_0$
60	Slice 6/7 — DIAG MODE$_1$
61	Slice 6/7 — CORRECT
62	Slice 6/7 — PASSTHRU
63	Don't Care

2595 tbl 20

Table 14. Diagnostic Latch Loading — 64-Bit Format

Some multiple errors will cause a data bit to be inverted. For example, in the 16-bit mode where bits 8 and 13 are in error, the syndrome 111100 (S_0, S_1, S_2, S_3, S_4, S_5) is produced. The bit-in-error decoder receives the syndrome 11100 (S_0, S_1, S_2, S_3, S_4) which it decodes as a single error in data bit 0 and inverts that bit. Figure 8 indicates a method for inhibiting correction when a multiple error occurs.



2595 drw 11

Figure 8. Inhibition of Data Modification

FUNCTIONAL EQUATIONS

The following equations and tables describe in detail how the output values of the IDT39C60 EDC are determined as a function of the value of the inputs and the internal states. Be sure to carefully read the following definitions of symbols before examining the tables.

DEFINITIONS

$D_I \leftarrow$ DATAI if LE_{IN} is HIGH or the output of bit I of the Data Input Latch if LE_{IN} is LOW
$C_I \leftarrow$ CB_I if LE_{IN} is HIGH or the output of bit I of the Check Bit Latch if LE_{IN} is LOW
$DL_I \leftarrow$ Output of bit I of the Diagnostic Latch
$S_I \leftarrow$ Internally generated syndromes (same as outputs of SC_I if outputs enabled)

$PA \leftarrow D_0 \oplus D_1 \oplus D_2 \oplus D_4 \oplus D_6 \oplus D_8 \oplus D_{10} \oplus D_{12}$

$PB \leftarrow D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7$

$PC \leftarrow D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14} \oplus D_{15}$

$PD \leftarrow D_0 \oplus D_3 \oplus D_4 \oplus D_7 \oplus D_9 \oplus D_{10} \oplus D_{13} \oplus D_{15}$

$PE \leftarrow D_0 \oplus D_1 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{11} \oplus D_{12} \oplus D_{13}$

$PF \leftarrow D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_{14} \oplus D_{15} \oplus D_7$

$PG_1 \leftarrow D_0 \oplus D_4 \oplus D_6 \oplus D_7$

$PG_2 \leftarrow D_1 \oplus D_2 \oplus D_3 \oplus D_5$

$PG_3 \leftarrow D_8 \oplus D_9 \oplus D_{11} \oplus D_{14}$

$PG_4 \leftarrow D_{10} \oplus D_{12} \oplus D_{13} \oplus D_{15}$

Error Signals

$\overline{ERROR} \leftarrow (\overline{S6} \cdot (\overline{ID_1 + ID_2})) \cdot \overline{S5} \cdot \overline{S4} \cdot \overline{S3} \cdot \overline{S2} \cdot \overline{S1} \cdot \overline{S0}$ + GENERATE + INITIALIZE + PASSTHRU

$\overline{MULT\ ERROR}$:

(16 and 32-Bit Modes) $\leftarrow \overline{((S6 \cdot ID_1) \oplus S5 \oplus S4 \oplus S3 \oplus S2 \oplus S1 \oplus S0)\ (ERROR)}$ + TOME + GENERATE + PASSTHRU + INITIALIZE

$\overline{MULT\ ERROR}$: (64-Bit Modes) $\leftarrow$ $\overline{TOME}$ + GENERATE + PASSTHRU + INITIALIZE

				Hex	0		1		2		3		4		5		6		7	
				S_6	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
				S_5	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
			Syndrome[1, 2] Bits	S_4	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
				S_3	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
	Hex	S_2	S_1	S_0																
0	8	0	0	0								1		1	1		1			1
1	9	0	0	1		1			1			1	1	1	1		1		1	1
2	A	0	1	0			1				1	1	1						1	1
3	B	0	1	1	1						1	1	1						1	1
4	C	1	0	0		1						1	1	1						1
5	D	1	0	1	1	1						1	1	1						1
6	E	1	1	0	1			1		1	1	1	1			1		1	1	
7	F	1	1	1	1			1		1	1	1	1			1		1	1	1

NOTES:

2595 tbl 21

1. $S_6, S_5, \ldots S_0$ are internal syndromes except in Modes 010, 100, 101, 110, 111 (CODE ID_2, ID_1, ID_0). In these modes, the syndromes are input over the check bit lines. $S_6 \leftarrow C_6, S_5 \leftarrow C_5, \ldots S_1 \leftarrow C_1, S_0 \leftarrow C_0$.
2. The S_6 internal syndrome is always forced to 0 in CODE ID 000.

Table 15. TOME (Three or More Errors)

Generate Mode (Check Bits)	CODE ID_{0-2} 000	010	011	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_3$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	PA	PA	$PA \oplus CB_1$	PA	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD}$	$\overline{PD}$	$PD \oplus CB_2$	$\overline{PD}$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE}$	$\overline{PE}$	$PE \oplus CB_3$	$\overline{PE}$	PE	PE	PE
$SC_4 \leftarrow$	PF	PF	$PF \oplus CB_4$	PF	PF	PF	PF
$SC_5 \leftarrow$	PC	PC	$PC \oplus CB_5$	PC	PC	PC	PC
$SC_6 \leftarrow$	1	PB	$PC \oplus CB_6$	PB	PB	PB	PB

2595 tbl 22

Table 16. Generate Mode (Check Bits)

Detect and Correct Modes (Syndromes)	CODE ID_{0-2}						
	000	010	011 (1)	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3 \oplus C_0$	$PG_1 \oplus PG_3 \oplus C_0$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3 \oplus C_0$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	$PA \oplus C_1$	$PA \oplus C_1$	$PA \oplus CB_1$	$PA \oplus C_1$	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD} \oplus C_2$	$\overline{PD} \oplus C_2$	$PD \oplus CB_2$	$\overline{PD} \oplus C_2$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE} \oplus C_3$	$\overline{PE} \oplus C_3$	$PE \oplus CB_3$	$\overline{PE} \oplus C_3$	PE	PE	PE
$SC_4 \leftarrow$	$PF \oplus C_4$	$PF \oplus C_4$	$PF \oplus CB_4$	$PF \oplus C_4$	PF	PF	PF
$SC_5 \leftarrow$	$PC \oplus C_5$	$PC \oplus C_5$	$PC \oplus CB_5$	$PC \oplus C_5$	PC	PC	PC
$SC_6 \leftarrow$	1	$PB \oplus C_6$	$PC \oplus CB_6$	PB	PB	$PB \oplus C_6$	$PB \oplus C_6$

NOTE: 2595 tbl 23
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

Table 17. Detect and Correct Modes (Syndromes)

Diagnostic Detect and Correct Mode	CODE ID_{0-2}						
	000	010	011 (1)	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3 \oplus DL_0$	$PG_1 \oplus PG_3 \oplus DL_0$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3 \oplus DL_0$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	$PA \oplus DL_1$	$PA \oplus DL_1$	$PA \oplus CB_1$	$PA \oplus DL_1$	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD} \oplus DL_2$	$\overline{PD} \oplus DL_2$	$PD \oplus CB_2$	$\overline{PD} \oplus DL_2$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE} \oplus DL_3$	$\overline{PE} \oplus DL_3$	$PE \oplus CB_3$	$\overline{PE} \oplus DL_3$	PE	PE	PE
$SC_4 \leftarrow$	$PF \oplus DL_4$	$PF \oplus DL_4$	$PF \oplus CB_4$	$PF \oplus DL_4$	PF	PF	PF
$SC_5 \leftarrow$	$PDL \oplus DL_5$	$PC \oplus DL_5$	$PC \oplus CB_5$	$PC \oplus DL_5$	PC	PC	PC
$SC_6 \leftarrow$	1	$PB \oplus DL_6$	$PC \oplus CB_6$	PB	PB	$PB \oplus DL_6$	$PB \oplus DL_7$

NOTE: 2595 tbl 24
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

Table 18. Diagnostic Detect and Correct Mode

Diagnostic Generate Mode	CODE ID_{0-2}						
	000	010	011 (1)	100	101	110	111
$SC_0 \leftarrow$	DL_0	DL_0	CB_0	DL_0	1	1	1
$SC_1 \leftarrow$	DL_1	DL_1	CB_1	DL_1	1	1	1
$SC_2 \leftarrow$	DL_2	DL_2	CB_2	DL_2	1	1	1
$SC_3 \leftarrow$	DL_3	DL_3	CB_3	DL_3	1	1	1
$SC_4 \leftarrow$	DL_4	DL_4	CB_4	DL_4	1	1	1
$SC_5 \leftarrow$	DL_5	DL_5	CB_5	DL_5	1	1	1
$SC_6 \leftarrow$	1	DL_6	CB_6	1	1	DL_6	DL_7

NOTE: 2595 tbl 25
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

Table 19. Diagnostic Generate Mode

PASSTHRU Mode	CODE ID_{0-2}						
	000	010	011 (1)	100	101	110	111
$SC_0 \leftarrow$	C_0	C_0	CB_0	C_0	1	1	1
$SC_1 \leftarrow$	C_1	C_1	CB_1	C_1	1	1	1
$SC_2 \leftarrow$	C_2	C_2	CB_2	C_2	1	1	1
$SC_3 \leftarrow$	C_3	C_3	CB_3	C_3	1	1	1
$SC_4 \leftarrow$	C_4	C_4	CB_4	C_4	1	1	1
$SC_5 \leftarrow$	C_5	C_5	CB_5	C_5	1	1	1
$SC_6 \leftarrow$	1	C_6	CB_6	1	1	C_6	C_6

NOTE: 2595 tbl 26
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

Table 20. PASSTHRU Mode

		S5	0	0	0	0	1	1	1	1
		S4	0	0	1	1	0	0	1	1
S2	S1	S3	0	1	0	1	0	1	0	1
0	0		—	—	—	5	—	11	14	—
0	1		—	1	2	6	8	12	—	—
1	0		—	—	3	7	9	13	15	—
1	1		—	0	4	—	10	—	—	—

NOTE:
1. Unlisted S combinations are no correction.

2595 tbl 27

Table 21. CODE ID_{2-0} = 000

		C6	0	0	0	0	1	1	1	1
		C5	1	1	1	1	0	0	0	0
		C4	0	0	1	1	0	0	1	1
C2	C1	C3	0	1	0	1	0	1	0	1
0	0		—	11	14	—	—	—	—	5
0	1		8	12	—	—	—	1	2	6
1	0		9	13	15	—	—	—	3	7
1	1		10	—	—	—	—	0	4	—

NOTE:
1. Unlisted C_n combinations are no correction.

2595 tbl 28

Table 22. CODE ID_{2-0} = 010

		S6	0	0	0	0	1	1	1	1
		S5	0	0	0	0	1	1	1	1
		S4	0	0	1	1	0	0	1	1
S2	S1	S3	0	1	0	1	0	1	0	1
0	0		—	—	—	5	—	11	14	—
0	1		—	1	2	6	8	12	—	—
1	0		—	—	3	7	9	13	15	—
1	1		—	0	4	—	10	—	—	—

NOTE:
1. Unlisted S combinations are no correction.

2595 tbl 29

Table 23. CODE ID_{2-0} = 011

		C0	0	0	0	0	1	1	1	1
		C6	0	0	0	0	1	1	1	1
		C5	1	1	1	1	0	0	0	0
		C4	0	0	1	1	0	0	1	1
C2	C1	C3	0	1	0	1	0	1	0	1
0	0		—	11	14	—	—	—	—	5
0	1		8	12	—	—	—	1	2	6
1	0		9	13	15	—	—	—	3	7
1	1		10	—	—	—	—	0	4	—

NOTE:
1. Unlisted C_n combinations are no correction.

2595 tbl 30

Table 24. CODE ID_{2-0} = 100

		C0	0	0	0	0	1	1	1	1
		C6	0	0	0	0	1	1	1	1
		C5	0	0	0	0	1	1	1	1
		C4	0	0	1	1	0	0	1	1
C2	C1	C3	0	1	0	1	0	1	0	1
0	0		—	—	—	5	—	11	14	—
0	1		—	1	2	6	8	12	—	—
1	0		—	—	3	7	9	13	15	—
1	1		—	0	4	—	10	—	—	—

NOTE:
1. Unlisted C_n combinations are no correction.

2595 tbl 31

Table 25. CODE ID_{2-0} = 101

		C0	0	0	0	0	1	1	1	1
		C6	1	1	1	1	0	0	0	0
		C5	0	0	0	0	1	1	1	1
		C4	0	0	1	1	0	0	1	1
C2	C1	C3	0	1	0	1	0	1	0	1
0	0		—	—	—	5	—	11	14	—
0	1		—	1	2	6	8	12	—	—
1	0		—	—	3	7	9	13	15	—
1	1		—	0	4	—	10	—	—	—

NOTE:
1. Unlisted C_n combinations are no correction.

2595 tbl 32

Table 26. CODE ID_{2-0} = 110

		C0	0	0	0	0	1	1	1	1
		C6	1	1	1	1	0	0	0	0
		C5	1	1	1	1	0	0	0	0
		C4	0	0	1	1	0	0	1	1
C2	C1	C3	0	1	0	1	0	1	0	1
0	0		—	11	14	—	—	—	—	5
0	1		8	12	—	—	—	1	2	6
1	0		9	13	15	—	—	—	3	7
1	1		10	—	—	—	—	0	4	—

NOTE:
1. Unlisted C_n combinations are no correction.

2595 tbl 33

Table 27. CODE ID_{2-0} = 111

8

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
V_{CC}	Power Supply Voltage	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	30	30	mA

NOTE: 2595 tbl 34

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2595 tbl 35

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level(4)		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level(4)		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	0.1	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	–0.1	–10	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	V
			I_{OH} = –6mA MIL.	2.4	4.3	—	
			I_{OH} = –6mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}	V
			I_{OL} = 8mA MIL.	—	0.3	0.5	
			I_{OL} = 8mA COM'L.	—	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	—	–0.1	–20	µA
			V_O = V_{CC} (Max.)	—	0.1	20	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V(3)		–20	—	—	mA

NOTES: 2595 tbl 36

1. For conditions shown as Max. or Min. use appropriate value specified under DC Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels should only be static tested in a noise-free environment. Guaranteed by design.

DC ELECTRICAL CHARACTERISTICS (Cont'd.)

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%
V_{LC} = 2.0V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQ}	Quiescent Power Supply Current (CMOS) Inputs	V_{CC} = Max. V_{IN} = V_{CC} or GND f_{OP} = 0		—	3.0	5.0	mA
I_{CCT}	Quiescent Input Power Supply Current (per Input @ TTL High)[3]	V_{CC} = Max., V_{IN} = 3.4V, f_{OP} = 0		—	0.3	2.0	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. V_{IN} = V_{CC} or GND Outputs Open, $\overline{OE}$ = L	MIL.	—	5.0	8.5	mA/ MHz
			COM'L.	—	5.0	7.0	
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50% Duty Cycle V_{IN} = V_{CC} or GND	MIL.	—	53	90	mA
			COM'L.	—	53	75	
		V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50% Duty Cycle V_{IN} = 3.4V, V_{IN} = 0.4V	MIL.	—	60	100	
			COM'L.	—	60	85	

2595 tbl 37

NOTES:
1. For conditions shown as Max. or Min. use appropriate value specified under DC Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQ}, then dividing by the total number of inputs.
4. Total Supply Current is the sum of the Quiescent Current and the Dynamic Current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:
   I_{CC} = I_{CCQ} + I_{CCT} (N_T x D_H) + I_{CCD} (f_{OP})
   D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
   N_T = Number of dynamic inputs driven at TTL levels
   f_{OP} = Operating frequency

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.

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IDT 39C60B AC ELECTRICAL CHARACTERISTICS

Guaranteed Commercial Range Performance: Temperature range: 0°C to +70°C; VCC = 5.0V ± 5%
The signals switch between 0V and 3V with signal measured at 1.5V level.

MAXIMUM PROPAGATION DELAYS C_L = 50pF

From Input		To Output SC0–6	DATA0–15	ERROR	MULT ERROR	Unit
DATA0–15		18	25(1)	18	20	ns
CB0–6 (CODE ID = 000, 011)		12	22	17	20	ns
CB0–6 (CODE ID = 010, 100,101, 110, 111)		12	16	17	20	ns
GENERATE	↑	—	—	14	19	ns
	↓	15	—	—	—	
CORRECT (Not Internal Control Mode)		—	22	—	—	ns
DIAG MODE and PASSTHRU (Not Internal Control Mode)		20	22	16	19	ns
CODE ID		20	22	22	24	ns
LEIN From latched to transparent	↑	20	28	20	22	ns
LEOUT From latched to transparent	↑	—	11	—	—	ns
LEDIAG From latched to transparent	↑	20	28	20	22	ns
Internal Control Mode: LEDIAG From latched to transparent	↑	24	33	24	27	ns
Internal Control Mode: DATA0–15 Via Diagnostic Latch		24	33	24	27	ns

NOTE:
1. DATAIN to corrected DATAOUT measurement requires timing as shown below.

2595 tbl 38

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time	Hold Time	Unit
DATA0–15		↓	LEIN	5	3	ns
CB0–6 (not applic. to CODE ID = 11)		↓		5	3	ns
DATA0–15		↓	LEOUT	24	2	ns
CB0–7 (CODE ID = 000, 011)		↓		21	0	ns
CB0–7 (CODE ID = 010, 100, 101, 110, 111)		↓		21	0	ns
CORRECT	↑	↓		22	0	ns
DIAG MODE		↓		22	0	ns
PASSTHRU		↓		22	0	ns
CODE ID1, 0		↓		25	0	ns
LEIN	↑	↓		28	0	ns
DATA0–15			LEDIAG	5	3	ns

2595 tbl 39

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C_L = 5pF and measured to 0.5V change of output voltage level. Test performed with C_L = 50pF and correlated to C_L = 5pF.

From Input	Enable	Disable	To Output	Enable Max.	Disable Max.	Unit
$\overline{OE}$ Byte0, 1	↓	↑	DAT0–15	12	10	ns
$\overline{OE}$SC	↓	↑	SC0–7	12	10	ns

2595 tbl 40

MINIMUM PULSE WIDTHS

			Min.	
LEIN, LEOUT, LEDIAG	↑↓	(Positive-going pulse)	8	ns

2595 tbl 41

IDT 39C60B AC ELECTRICAL CHARACTERISTICS

Guaranteed Military Range Performance: Temperature range: –55°C to +125°C; VCC = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

MAXIMUM PROPAGATION DELAYS C_L = 50pF

From Input		To Output: SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$	Unit
$DATA_{0-15}$		22	30(1)	22	25	ns
CB_{0-6} (CODE ID = 000, 011)		14	26	20	24	ns
CB_{0-6} (CODE ID = 010, 100,101, 110, 111)		14	19	20	24	ns
$\overline{GENERATE}$	↑	—	—	14	19	ns
	↓	15	—	—	—	
CORRECT (Not Internal Control Mode)		—	20	—	—	ns
DIAG MODE and PASSTHRU (Not Internal Control Mode)		24	26	19	21	ns
CODE ID		24	29	26	29	ns
LE_{IN} From latched to transparent	↑	24	34	24	26	ns
LE_{OUT} From latched to transparent	↑	—	13	—	—	ns
Internal Control Mode: LE_{DIAG} From latched to transparent	↑	24	34	24	26	ns
LE_{DIAG} From latched to transparent	↑	29	40	29	32	ns
Internal Control Mode: $DATA_{0-15}$ Via Diagnostic Latch		29	40	29	32	ns

2595 tbl 42

NOTE:
1. $DATA_{IN}$ to corrected $DATA_{OUT}$ measurement requires timing as shown below.

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time	Hold Time	Unit
$DATA_{0-15}$	↓	LE_{IN}		6	4	ns
CB_{0-6} (not applic. to CODE ID = 11)	↓			6	4	ns
$DATA_{0-15}$	↓	LE_{OUT}		29	2	ns
CB_{0-7} (CODE ID = 000, 011)	↓			25	0	ns
CB_{0-7} (CODE ID = 010, 100, 101, 110, 111)	↓			25	0	ns
CORRECT	↑	↓		26	—	ns
DIAG MODE	↓			26	0	ns
PASSTHRU	↓			26	0	ns
$CODE\ ID_{1,0}$	↓			30	0	ns
LE_{IN}	↑	↓		34	—	ns
$DATA_{0-15}$		LE_{DIAG}		6	4	ns

2595 tbl 43

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C_L = 5pF and measured to 0.5V change of output voltage level. Test performed with C_L = 50pF and correlated to C_L = 5pF.

From Input	Enable	Disable	To Output	Enable Max.	Disable Max.	Unit
$\overline{OE}\ Byte_{0,1}$	↓	↑	DAT_{0-15}	15	12	ns
$\overline{OE}_{SC}$	↓	↑	SC_{0-7}	15	12	ns

2595 tbl 44

MINIMUM PULSE WIDTHS			Min.	
LE_{IN}, LE_{OUT}, LE_{DIAG}	↑↓	(Positive-going pulse)	10	ns

2595 tbl 45

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IDT 39C60A AC ELECTRICAL CHARACTERISTICS

Guaranteed Commercial Range Performance: Temperature range: 0°C to +70°C; V_{CC} = 5.0V ± 5%
The signals switch between 0V and 3V with signal measured at 1.5V level.

MAXIMUM PROPAGATION DELAYS C_L = 50pF

From Input		To Output: SC_{0-6}	To Output: $DATA_{0-15}$	To Output: $\overline{ERROR}$	To Output: $\overline{MULT\ ERROR}$	Unit
$DATA_{0-15}$		20	30(1)	20	23	ns
CB_{0-6} (CODE ID = 000, 011)		14	25	20	23	ns
CB_{0-6} (CODE ID = 010, 100,101, 110, 111)		14	18	20	23	ns
$\overline{GENERATE}$	↑	—	33	18	23	ns
	↓	15	—	—	—	
CORRECT (Not Internal Control Mode)		—	20	—	—	ns
DIAG MODE and PASSTHRU (Not Internal Control Mode)		22	25	18	21	ns
CODE ID		23	28	25	28	ns
LE_{IN} From latched to transparent	↑	22	32	22	25	ns
LE_{OUT} From latched to transparent	↑	—	13	—	—	ns
LE_{DIAG} From latched to transparent	↑	22	32	22	25	ns
Internal Control Mode: LE_{DIAG} From latched to transparent	↑	28	38	28	31	ns
Internal Control Mode: $DATA_{0-15}$ Via Diagnostic Latch		28	38	28	31	ns

NOTE:
1. $DATA_{IN}$ to corrected $DATA_{OUT}$ measurement requires timing as shown below.

2595 tbl 46

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time	Hold Time	Unit
$DATA_{0-15}$	↓	LE_{IN}		5	3	ns
CB_{0-6} (not applic. to CODE ID = 11)	↓			5	3	ns
$DATA_{0-15}$	↓	LE_{OUT}		24	2	ns
CB_{0-7} (CODE ID = 000, 011)	↓			21	0	ns
CB_{0-7} (CODE ID = 010, 100, 101, 110, 111)	↓			21	0	ns
CORRECT	↑	↓		22	0	ns
DIAG MODE		↓		22	0	ns
PASSTHRU		↓		22	0	ns
$CODE\ ID_{1,0}$		↓		25	0	ns
LE_{IN}	↑	↓		28	0	ns
$DATA_{0-15}$			LE_{DIAG}	5	3	ns

2595 tbl 47

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C_L = 5pF and measured to 0.5V change of output voltage level. Test performed with C_L = 50pF and correlated to C_L = 5pF.

From Input	Enable	Disable	To Output	Enable Max.	Disable Max.	Unit
$\overline{OE}\ Byte_{0,1}$	↓	↑	DAT_{0-15}	24	21	ns
$\overline{OE}_{SC}$	↓	↑	SC_{0-7}	24	21	ns

2595 tbl 48

MINIMUM PULSE WIDTHS

		Min.	
LE_{IN}, LE_{OUT}, LE_{DIAG}	(Positive-going pulse)	12	ns

2595 tbl 49

IDT 39C60A AC ELECTRICAL CHARACTERISTICS

Guaranteed Military Range Performance: Temperature range: –55°C to +125°C; Vcc = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

MAXIMUM PROPAGATION DELAYS C_L = 50pF

From Input		To Output: SC_{0-6}	To Output: $DATA_{0-15}$	To Output: $\overline{ERROR}$	To Output: $\overline{MULT\ ERROR}$	Unit
$DATA_{0-15}$		22	35(1)	24	27	ns
CB_{0-6} (CODE ID = 000, 011)		17	25	24	27	ns
CB_{0-6} (CODE ID = 010, 100,101, 110, 111)		17	20	24	27	ns
$\overline{GENERATE}$	↑	—	28	21	25	ns
	↓	20	—	—	—	
CORRECT (Not Internal Control Mode)		—	25	—	—	ns
DIAG MODE and PASSTHRU (Not Internal Control Mode)		25	28	21	24	ns
CODE ID		26	31	28	31	ns
LE_{IN} From latched to transparent	↑	24	37	26	29	ns
LE_{OUT} From latched to transparent	↑	—	16	—	—	ns
LE_{DIAG} From latched to transparent	↑	24	37	26	29	ns
Internal Control Mode: LE_{DIAG} From latched to transparent	↑	30	43	32	35	ns
Internal Control Mode: $DATA_{0-15}$ Via Diagnostic Latch		30	43	32	35	ns

NOTE:
1. $DATA_{IN}$ to corrected $DATA_{OUT}$ measurement requires timing as shown below.

2595 tbl 50

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time	Hold Time	Unit
$DATA_{0-15}$	↓	LE_{IN}		5	3	ns
CB_{0-6} (not applic. to CODE ID = 11)	↓			5	3	ns
$DATA_{0-15}$	↓	LE_{OUT}		27	2	ns
CB_{0-7} (CODE ID = 000, 011)	↓			24	0	ns
CB_{0-7} (CODE ID = 010, 100, 101, 110, 111)	↓			24	0	ns
CORRECT	↑	↓		25	0	ns
DIAG MODE		↓		25	0	ns
PASSTHRU		↓		25	0	ns
$CODE\ ID_{1,0}$		↓		28	0	ns
LE_{IN}	↑	↓		30	0	ns
$DATA_{0-15}$			LE_{DIAG}	5	3	ns

2595 tbl 51

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C_L = 5pF and measured to 0.5V change of output voltage level. Test performed with C_L = 50pF and correlated to C_L = 5pF.

From Input	Enable	Disable	To Output	Enable Max.	Disable Max.	Unit
$\overline{OE}\ Byte_{0,1}$	↓	↑	DAT_{0-15}	24	21	ns
$\overline{OE}_{SC}$	↓	↑	SC_{0-7}	24	21	ns

2595 tbl 52

MINIMUM PULSE WIDTHS

			Min.	
LE_{IN}, LE_{OUT}, LE_{DIAG}	↑↓	(Positive-going pulse)	12	ns

2595 tbl 53

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IDT 39C60-1 AC ELECTRICAL CHARACTERISTICS

Guaranteed Commercial Range Performance: Temperature range: 0°C to +70°C; Vcc = 5.0V ± 5%
The signals switch between 0V and 3V with signal measured at 1.5V level.

MAXIMUM PROPAGATION DELAYS C_L = 50pF

From Input		To Output: SC0-6	DATA0-15	ERROR	MULT ERROR	Unit
DATA0-15		28	52(1)	25	50	ns
CB0-6 (CODE ID = 000, 011)		23	50	23	47	ns
CB0-6 (CODE ID = 010, 100,101, 110, 111)		28	34	29	34	ns
$\overline{GENERATE}$	↓	—	63	36	55	ns
	↑	35	—	—	—	
CORRECT (Not Internal Control Mode)		—	45	—	—	ns
DIAG MODE(Not Internal Control Mode)		50	78	59	75	ns
PASSTHRU(Not Internal Control Mode)		36	44	29	46	ns
CODE ID		61	90	60	80	ns
LEIN From latched to transparent	↓	39	72	39	59	ns
LEOUT From latched to transparent	↓	—	31	—	—	ns
LEDIAG From latched to transparent	↓	45	78	45	65	ns
Internal Control Mode: LEDIAG From latched to transparent	↓	67	96	66	86	ns
Internal Control Mode: DATA0-15 Via Diagnostic Latch		67	96	66	86	ns

NOTE:
1. DATAIN to corrected DATAOUT measurement requires timing as shown below.

2595 tbl 54

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)	Set-up Time	Hold Time	Unit
DATA0-15	↑	LEIN	6	7	ns
CB0-6 (not applic. to CODE ID = 11)	↑		5	6	ns
DATA0-15	↑	LEOUT	34	5	ns
CB0-7 (CODE ID = 000, 011)	↑		35	0	ns
CB0-7 (CODE ID = 010, 100, 101, 110, 111)	↑		27	0	ns
CORRECT	↑		26	1	ns
DIAG MODE	↑		69	0	ns
PASSTHRU	↑		26	0	ns
CODE ID1, 0	↑		81	0	ns
LEIN	↑		51	5	ns
DATA0-15		LEDIAG	6	8	ns

2595 tbl 55

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C_L = 5pF and measured to 0.5V change of output voltage level. Test performed with C_L = 50pF and correlated to C_L = 5pF.

From Input	Enable	Disable	To Output	Enable Max.	Disable Max.	Unit
$\overline{OE}$ Byte0, 1	↑	↓	DAT0-15	30	30	ns
$\overline{OE}$SC	↑	↓	SC0-7	30	30	ns

2595 tbl 56

MINIMUM PULSE WIDTHS

		Min.	
LEIN, LEOUT, LEDIAG	↑↓ (Positive-going pulse)	15	ns

2595 tbl 57

IDT 39C60-1 AC ELECTRICAL CHARACTERISTICS

Guaranteed Military Range Performance: Temperature range: –55°C to +125°C; Vcc = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

MAXIMUM PROPAGATION DELAYS C_L = 50pF

From Input		To Output: SC_{0-6}	To Output: $DATA_{0-15}$	To Output: $\overline{ERROR}$	To Output: $\overline{MULT\ ERROR}$	Unit
$DATA_{0-15}$		31	59 (1)	28	56	ns
CB_{0-6} (CODE ID = 000, 011)		25	55	25	50	ns
CB_{0-6} (CODE ID = 010, 100,101, 110, 111)		30	38	31	37	ns
$\overline{GENERATE}$	∫	—	63	36	55	ns
	↘	38	—	—	—	
CORRECT (Not Internal Control Mode)		—	49	—	—	ns
DIAG MODE(Not Internal Control Mode)		58	89	65	90	ns
PASSTHRU(Not Internal Control Mode)		39	51	34	54	ns
CODE ID		69	100	68	90	ns
LE_{IN} From latched to transparent	∫	39	82	43	66	ns
LE_{OUT} From latched to transparent	∫	—	33	—	—	ns
LE_{DIAG} From latched to transparent	∫	50	88	49	72	ns
Internal Control Mode: LE_{DIAG} From latched to transparent	∫	75	106	74	96	ns
Internal Control Mode: $DATA_{0-15}$ Via Diagnostic Latch		75	106	74	96	ns

2595 tbl 58

NOTE:
1. $DATA_{IN}$ to corrected $DATA_{OUT}$ measurement requires timing as shown below.

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time	Hold Time	Unit
$DATA_{0-15}$	↘	LE_{IN}		7	7	ns
CB_{0-6} (not applic. to CODE ID = 11)	↘			5	7	ns
$DATA_{0-15}$	↘	LE_{OUT}		39	5	ns
CB_{0-7} (CODE ID = 000, 011)	↘			38	0	ns
CB_{0-7} (CODE ID = 010, 100, 101, 110, 111)	↘			30	0	ns
CORRECT	∫ ↘			28	1	ns
DIAG MODE	↘			84	0	ns
PASSTHRU	↘			30	0	ns
$CODE\ ID_{1,0}$	↘			89	0	ns
LE_{IN}	∫ ↘			59	5	ns
$DATA_{0-15}$		LE_{DIAG}		7	9	ns

2595 tbl 59

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C_L = 5pF and measured to 0.5V change of output voltage level. Test performed with C_L = 50pF and correlated to C_L = 5pF.

From Input	Enable	Disable	To Output	Enable Max.	Disable Max.	Unit
$\overline{OE}\ Byte_{0,1}$	↘	∫	DAT_{0-15}	35	35	ns
$\overline{OE}_{SC}$	↘	∫	SC_{0-7}	35	35	ns

2595 tbl 60

MINIMUM PULSE WIDTHS

			Min.	
LE_{IN}, LE_{OUT}, LE_{DIAG}	∫↘	(Positive-going pulse)	15	ns

2595 tbl 61

8

IDT 39C60 AC ELECTRICAL CHARACTERISTICS

Guaranteed Commercial Range Performance: Temperature range: 0°C to +70°C; V_{CC} = 5.0V ± 5%
The signals switch between 0V and 3V with signal measured at the 1.5V level.

MAXIMUM PROPAGATION DELAYS C_L = 50pF

From Input		To Output: SC0-6	DATA0-15	ERROR	MULT ERROR	Unit
DATA0-15		32	65(1)	32	50	ns
CB0-6 (CODE ID = 000, 011)		28	56	29	47	ns
CB0-6 (CODE ID = 010, 100,101, 110, 111)		28	45	29	34	ns
GENERATE	↑	—	63	36	55	ns
	↓	35	—	—	—	
CORRECT (Not Internal Control Mode)		—	45	—	—	ns
DIAG MODE(Not Internal Control Mode)		50	78	59	75	ns
PASSTHRU(Not Internal Control Mode)		36	44	29	46	ns
CODE ID		61	90	60	80	ns
LEIN From latched to transparent	↑	39	72	39	59	ns
LEOUT From latched to transparent	↑	—	31	—	—	ns
LEDIAG From latched to transparent	↑	45	78	45	65	ns
Internal Control Mode: LEDIAG From latched to transparent	↑	67	96	66	86	ns
Internal Control Mode: DATA0-15 Via Diagnostic Latch		67	96	66	86	ns

NOTE:
1. DATAIN to corrected DATAOUT measurement requires timing as shown below.

2595 tbl 62

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)	Set-up Time	Hold Time	Unit
DATA0-15	↓	LEIN	6	7	ns
CB0-6 (not applic. to CODE ID = 11)	↓		5	6	ns
DATA0-15	↓	LEOUT	44	5	ns
CB0-7 (CODE ID = 000, 011)	↓		35	0	ns
CB0-7 (CODE ID = 010, 100, 101, 110, 111)	↓		27	0	ns
CORRECT	↑		26	1	ns
DIAG MODE	↓		69	0	ns
PASSTHRU	↓		26	0	ns
CODE ID1, 0	↓		81	0	ns
LEIN	↑		51	5	ns
DATA0-15		LEDIAG	6	8	ns

2595 tbl 63

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C_L = 5pF and measured to 0.5V change of output voltage level. Test performed with C_L = 50pF and correlated to C_L = 5pF.

From Input	Enable	Disable	To Output	Enable Max.	Disable Max.	Unit
$\overline{OE}$ Byte0, 1	↓	↑	DAT0-15	30	30	ns
$\overline{OE}$SC	↓	↑	SC0-7	30	30	ns

2595 tbl 64

MINIMUM PULSE WIDTHS

			Min.	
LEIN, LEOUT, LEDIAG	↑↓	(Positive-going pulse)	15	ns

2595 tbl 65

IDT 39C60 AC ELECTRICAL CHARACTERISTICS

Guaranteed Military Range Performance: Temperature range: –55°C to +125°C; Vcc = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

MAXIMUM PROPAGATION DELAYS C_L = 50pF

From Input		To Output: SC_{0-6}	To Output: $DATA_{0-15}$	To Output: $\overline{ERROR}$	To Output: $\overline{MULT\ ERROR}$	Unit
$DATA_{0-15}$		35	73 (1)	36	56	ns
CB_{0-6} (CODE ID = 000, 011)		30	61	31	50	ns
CB_{0-6} (CODE ID = 010, 100,101, 110, 111)		30	50	31	37	ns
$\overline{GENERATE}$	∫	—	63	36	55	ns
	↘	38	—	—	—	
CORRECT (Not Internal Control Mode)		—	49	—	—	ns
DIAG MODE(Not Internal Control Mode)		58	89	65	90	ns
PASSTHRU(Not Internal Control Mode)		39	51	34	54	ns
CODE ID		69	100	68	90	ns
LE_{IN} From latched to transparent	∫	44	82	43	66	ns
LE_{OUT} From latched to transparent	∫	—	33	—	—	ns
LE_{DIAG} From latched to transparent	∫	50	88	49	72	ns
Internal Control Mode: LE_{DIAG} From latched to transparent	∫	75	106	74	96	ns
Internal Control Mode: $DATA_{0-15}$ Via Diagnostic Latch		75	106	74	96	ns

2595 tbl 66

NOTE:
1. $DATA_{IN}$ to corrected $DATA_{OUT}$ measurement requires timing as shown below.

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time	Hold Time	Unit
$DATA_{0-15}$	↘	LE_{IN}		7	7	ns
CB_{0-6} (not applic. to CODE ID = 11)	↘			5	7	ns
$DATA_{0-15}$	↘	LE_{OUT}		50	5	ns
CB_{0-7} (CODE ID = 000, 011)	↘			38	0	ns
CB_{0-7} (CODE ID = 010, 100, 101, 110, 111)	↘			30	0	ns
CORRECT	↘		∫	28	1	ns
DIAG MODE	↘			84	0	ns
PASSTHRU	↘			30	0	ns
$CODE\ ID_{1,0}$	↘			89	0	ns
LE_{IN}	↘		∫	59	5	ns
$DATA_{0-15}$		LE_{DIAG}		7	9	ns

2595 tbl 67

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C_L = 5pF and measured to 0.5V change of output voltage level. Test performed with C_L = 50pF and correlated to C_L = 5pF.

From Input	Enable	Disable	To Output	Enable Max.	Disable Max.	Unit
$\overline{OE}\ Byte_{0,1}$	↘	∫	DAT_{0-15}	35	35	ns
$\overline{OE}_{SC}$	↘	∫	SC_{0-7}	35	35	ns

2595 tbl 67

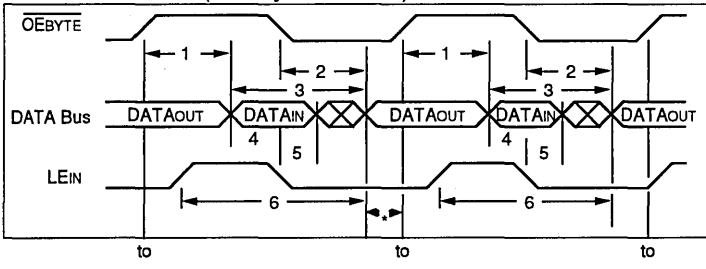
MINIMUM PULSE WIDTHS

		Min.	
LE_{IN}, LE_{OUT}, LE_{DIAG}	∫↘ (Positive-going pulse)	15	ns

2595 tbl 69

8

IDT39C60 — DATAIN TO CORRECTED DATAOUT TIMING (Two cycles shown)



NOTES:
Device Mode = "Correct"
System Type = "Correct Always"

Timing Parameter From To	Min./ Max.
1.-OEBYTE = High to DATAOUT Disabled	Max.
2.-OEBYTE = Low to DATAOUT Enabled	Max.
3.-DATAIN to Corrected DATAOUT	Max.
4.-DATAIN Set-up to LEIN = Low	Min.
5.-DATAIN Hold to LEIN = Low	Min.
6.-LEIN = High to DATAOUT	Max.
* = (Memory/System dependent)	

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 12

2595 tbl 70

Test	Switch
Disable Low Enable Low	Closed
All Other Outputs	Open

2595 tbl 71

IDT39C60 INPUT/OUTPUT INTERFACE CIRCUIT

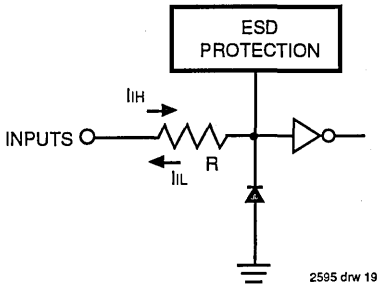


Figure 10. Input Structure (All Inputs)

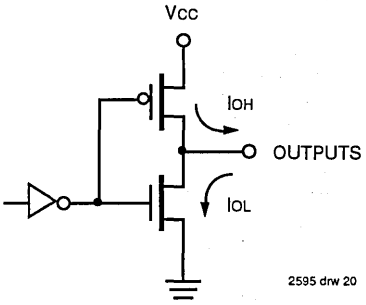
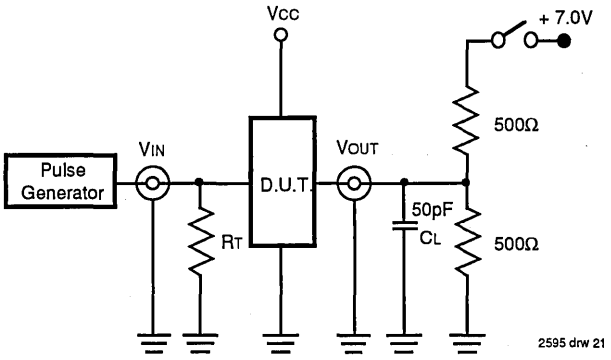


Figure 11. Output Structure

TEST CIRCUIT LOAD



DEFINITIONS:
CL = Load capacitance: includes jig and probe capacitance
RL = Termination resistance: should be equal to ZOUT of the Pulse Generator

Figure 12.

8

Integrated Device Technology, Inc.

32-BIT CMOS ERROR DETECTION AND CORRECTION UNIT

IDT49C460
IDT49C460A
IDT49C460B
IDT49C460C
IDT49C460D

FEATURES:

- Fast

	Detect	Correct
— IDT49C460D	12ns (max.)	18ns (max.)
— IDT49C460C	16ns (max.)	24ns (max.)
— IDT49C460B	25ns (max.)	30ns (max.)
— IDT49C460A	30ns (max.)	36ns (max.)
— IDT49C460	40ns (max.)	49ns (max.)

- Low-power CMOS
  - — Commercial: 95mA (max.)
  - — Military: 125mA (max.)
- Improves system memory reliability
  - — Corrects all single bit errors, detects all double and some triple-bit errors
- Cascadable
  - — Data words up to 64-bits
- Built-in diagnostics
  - — Capable of verifying proper EDC operation via software control
- Simplified byte operations
  - — Fast byte writes possible with separate byte enables
- Functional replacement for 32- and 64-bit configurations of the 2960
- Available in PGA, PLCC and Fine Pitch Flatpack
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962–88533

DESCRIPTION:

The IDT49C460s are high-speed, low-power, 32-bit Error Detection and Correction Units which generate check bits on a 32-bit data field according to a modified Hamming Code and correct the data word when check bits are supplied. The IDT49C460s are performance-enhanced functional replacements for 32-bit versions of the 2960. When performing a read operation from memory, the IDT49C460s will correct 100% of all single bit errors and will detect all double bit errors and some triple bit errors.

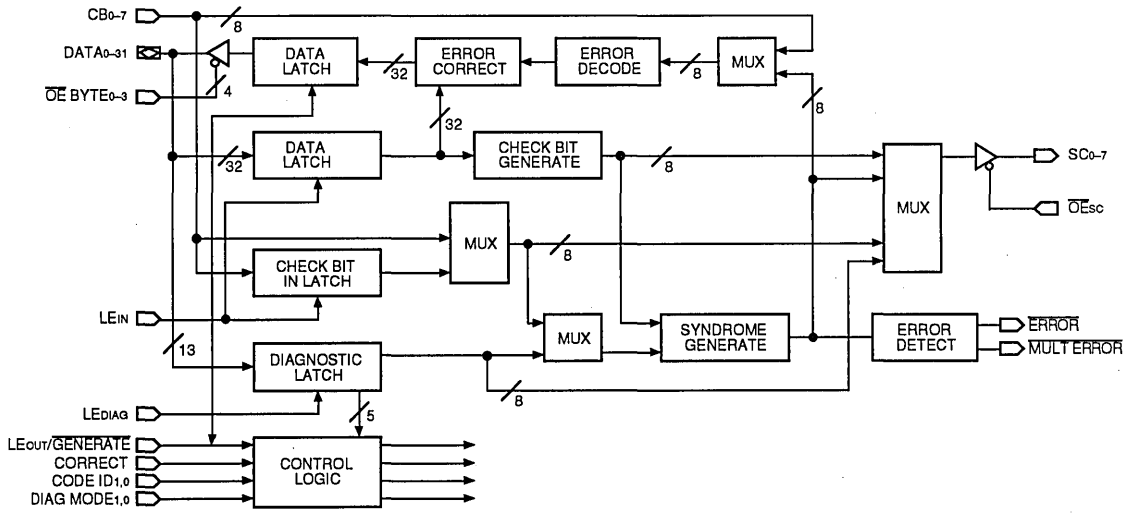
The IDT49C460s are easily cascadable to 64-bits. Thirty-two-bit systems use 7 check bits and 64-bit systems use 8 check bits. For both configurations, the error syndrome is made available.

The IDT49C460s incorporate two built-in diagnostic modes. Both simplify testing by allowing for diagnostic data to be entered into the device and to execute system diagnostics functions.

They are fabricated using CEMOS™, a CMOS technology designed for high-performance and high-reliability. The devices are packaged in a 68-pin ceramic PGA, PLCC and Ceramic Quad Flatpack.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

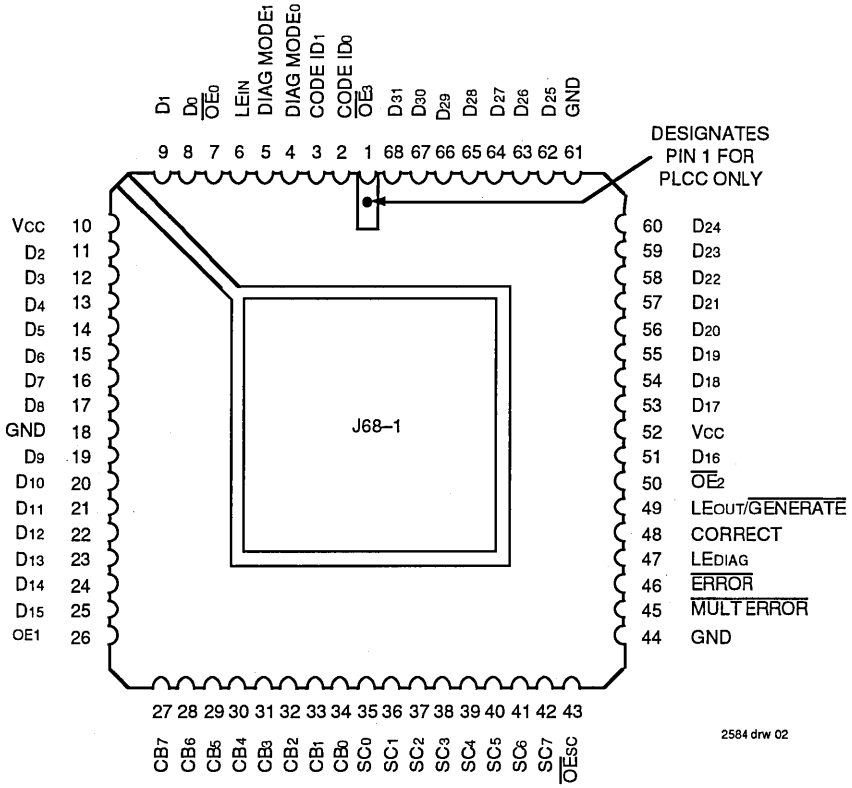
FUNCTIONAL BLOCK DIAGRAM



2584 drw 01

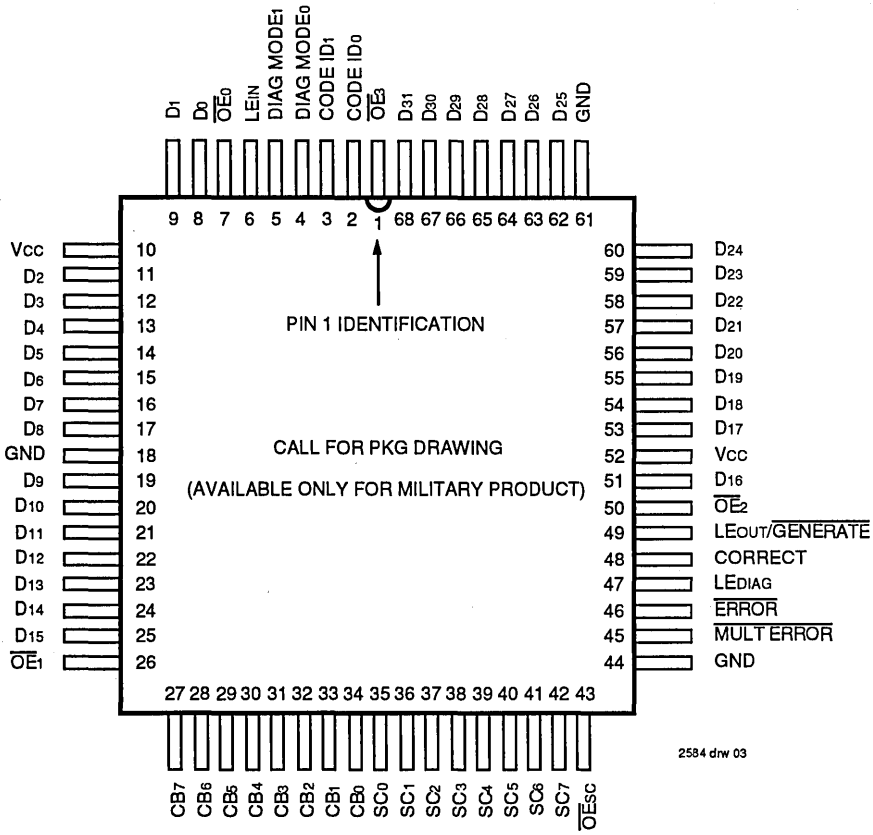
MILITARY AND COMMERCIAL TEMPERATURE RANGES **MAY 1992**

PIN CONFIGURATIONS

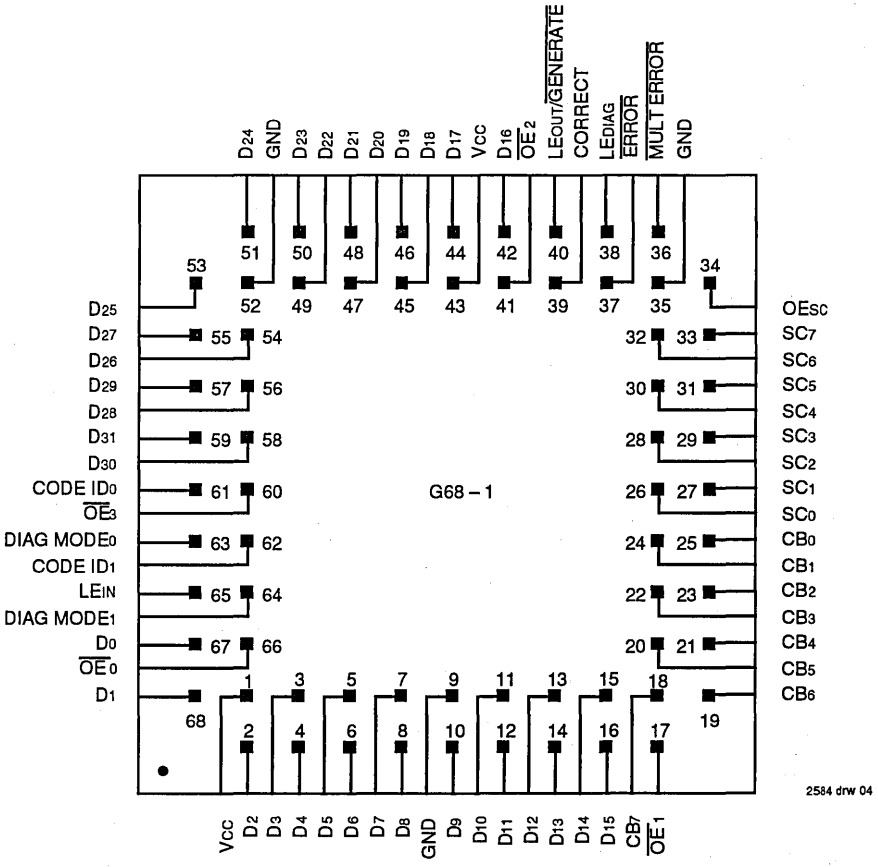


PLCC
TOPVIEW

8



FINE PITCH FLATPACK
TOPVIEW



PGA
TOPVIEW

8

PIN DESCRIPTIONS

Pin Name	I/O	Description
$DATA_{0-31}$	I/O	32 bidirectional data lines provide input to the Data Input Latch and Diagnostic Latch and also receive output from the Data Output Latch. $DATA_0$ is the LSB; $DATA_{31}$ is the MSB.
CB_{0-7}	I	Eight check bit input lines input check bits for error detection and also used to input syndrome bits for error correction in 64-bit applications.
LE_{IN}	I	Latch Enable is for the Data Input Latch. Controls latching of the input data. Data Input Latch and Check Bit Input Latch are latched to their previous state when LOW. When HIGH, the Data Input Latch and Check Bit Input Latch follow the input data and input check bits.
LE_{OUT}/ $\overline{GENERATE}$		A multifunction pin which, when LOW, is in the Check Bit Generate Mode. In this mode, the device generates the check bits or GENERATE partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs. Also, when LOW, the Data Out Latch is latched to its previous state. When HIGH, the device is in the Detect or Correct Mode. In this mode, the device detects single and multiple errors and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In the Correct Mode, single bit errors are also automatically corrected and the corrected data is placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates in a coded form the number of errors and the specific bit-in-error. When HIGH, the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct Mode, single bit errors are corrected by the network before being loaded into the Data Output Latch. In Detect Mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The Data Output Latch is disabled, with its contents unchanged, if the EDC is in the Generate Mode.
SC_{0-7}	O	Syndrome Check Bit outputs. Eight outputs which hold the check bits and partial check bits when the EDC is in the Generate Mode and will hold the syndrome/partial syndrome bits when the device is in the Detect or Correct modes. All are 3-state outputs.
$\overline{OE_{SC}}$	I	Output Enable—Syndrome Check Bits. In the HIGH condition, the SC outputs are in the high impedance state. When LOW, all SC output lines are enabled.
$\overline{ERROR}$	O	In the Detect or Correct Mode, this output will go LOW if one or more data or check bits contain an error. When HIGH, no errors have been detected. This pin is forced HIGH in the Generate Mode.
$\overline{MULT\ ERROR}$	O	In the Detect or Correct Mode, this output will go LOW if two or more bit errors have been detected. A HIGH level indicates that either one or no errors have been detected. This pin is forced HIGH in the Generate Mode.
CORRECT	I	The correct input which, when HIGH, allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it into the Data Output Latch. When LOW, the device will drive data directly from the Data Input Latch to the Data Output Latch without correction.
$\overline{OE}\ BYTE_{0-3}$	I	Output Enable—Bytes 0, 1, 2, 3. Data Output Latch. Control the three-state output buffers for each of the four bytes of the Data Output Latch. When LOW, they enable the output buffer of the Data Output Latch. When HIGH, they force the Data Output Latch buffer into the high impedance mode. One byte of the Data Output Latch is easily activated by separately selecting the four enable lines.
DIAG $MODE_{1,0}$	I	Select the proper diagnostic mode. They control the initialization, diagnostic and normal operation of the EDC.
CODE $ID_{1,0}$	I	These two code identification inputs identify the size of the total data word to be processed. The two allowable data word sizes are 32 and 64 bits and their respective modified Hamming Codes are designated 32/39 and 64/72. Special CODE $ID_{1,0}$, input 01 is also used to instruct the EDC that the signals CODE $ID_{1,0}$, DIAG $MODE_{1,0}$ and CORRECT are to be taken from the Diagnostic Latch rather than from the input control lines.
LE_{DIAG}	I	This is the Latch Enable for the Diagnostic Latch. When HIGH, the Diagnostic Latch follows the 32-bit data on the input lines. When LOW, the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits and internal control signals for CODE $ID_{1,0}$, DIAG $MODE_{1,0}$ and CORRECT.

2584 tbl 01

EDC ARCHITECTURE SUMMARY

The IDT49C460s are high-performance cascadable EDCs used for check bit generation, error detection, error correction and diagnostics. The function blocks for this 32-bit device consist of the following:

- Data Input Latch
- Check Bit Input Latch
- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic
- Error Correction Logic
- Data Output Latch
- Diagnostic Latch
- Control Logic

DATA INPUT/OUTPUT LATCH

The Latch Enable Input, LE_{IN}, controls the loading of 32 bits of data to the Data In Latch. The data from the DATA lines can be loaded in the Diagnostic Latch under control of the Diagnostic Latch Enable, LE_{DIAG}, giving check bit information in one byte and control information in another byte. The Diagnostic Latch is used in the Internal Control Mode or in one of the diagnostic modes. The Data Output Latch has buffers that place data on the DATA lines. These buffers are split into four 8-bit buffers, each having their own output enable controls. This feature facilitates byte read and byte modify operations.

CHECK BIT GENERATION LOGIC

This generates the appropriate check bits for the 32 bits of data in the Data Input Latch. The modified Hamming Code is the basis for generating the proper check bits.

SYNDROME GENERATION LOGIC

In both the Detect and Correct modes, this logic does a comparison on the check bits read from memory against the newly generated set of check bits produced for the data read in from memory. Matching sets of check bits mean no error was detected. If there is a mismatch, one or more of the data or check bits is in error. Syndrome bits are produced by an exclusive-OR of the two sets of check bits. Identical sets of check bits mean the syndrome bits will be all zeros. If an error results, the syndrome bits can be decoded to determine the number of errors and the specific bit-in-error.

ERROR DETECTION LOGIC

This part of the device decodes the syndrome bits generated by the Syndrome Generation Logic. With no errors in either the input data or check bits, both the $\overline{ERROR}$ and $\overline{MULTERROR}$ outputs are HIGH. ERROR will go low if one error is detected. $\overline{MULTERROR}$ and $\overline{ERROR}$ will both go low if two or more errors are detected.

ERROR CORRECTION LOGIC

In single error cases, this logic complements (corrects) the single data bit-in-error. This corrected data is loaded into the Data Output Latch, which can then be read onto the bidirectional data lines. If the error is resulting from one of the check bits, the correction logic does not place corrected check bits on the syndrome/check bit outputs. If the corrected check bits are needed, the EDC must be switched to the Generate Mode.

DATA OUTPUT LATCH AND OUTPUT BUFFERS

The Data Output Latch is used for storing the result of an error correction operation. The latch is loaded from the correction logic under control of the Data Output Latch Enable, LE_{OUT}. The Data Output Latch may also be directly loaded from the Data Input Latch in the PASSTHRU mode. The Data Output Latch buffer is split into 4 individual buffers which can be enabled by $\overline{OE}_{0-3}$ separately for reading onto the bidirectional data lines.

DIAGNOSTIC LATCH

The diagnostic latch is loadable under control of the Diagnostic Latch Enable, LE_{DIAG}, from the bidirectional data lines. Check bit information is contained in one byte while the other byte contains the control information. The Diagnostic Latch is used for driving the device when in the Internal Control Mode, or for supplying check bits when in one of the diagnostic modes.

CONTROL LOGIC

Specifies in which mode the device will be operating in. Normal operation is when the control logic is driven by external control inputs. In the Internal Control Mode, the control signals are read from the Diagnostic Latch. Since LE_{OUT} and $\overline{GENERATE}$ are controlled by the same pin, the latching action (LE_{OUT} from high to low) of the Data Output Latch causes the EDC to go into the Generate Mode.

8

DETAILED PRODUCT DESCRIPTION

The IDT49C460 EDC units contain the logic necessary to generate check bits on 32 bits of data input according to a modified Hamming Code. The EDC can compare internally generated check bits against those read with the 32-bit data to allow correction of any single bit data error and detection of all double (and some triple) bit errors. The IDT49C460s can be used for 32-bit data words (7 check bits) and 64-bit (8 check bits) data words.

WORD SIZE SELECTION

The two code identification pins, CODE $ID_{1,0}$, are used to determine the data word size that is 32 or 64 bits. They also select the Internal Control Mode. Table 4 defines all possible slice identification codes.

CHECK AND SYNDROME BITS

The IDT49C460s provide either check bits or syndrome bits on the three-state output pins, SC_{0-7}. Check bits are generated from a combination of the Data Input bits, while syndrome bits are an exclusive-OR of the check bits generated from read data with the read check bits stored with the data. Syndrome bits can be decoded to determine the single bit in error or that a double (some triple) error was detected. The check bits are labeled:

$C_0, C_1, C_2, C_3, C_4, C_5, C_6$ for the 32-bit configuration
$C_0, C_1, C_2, C_3, C_4, C_5, C_6, C_7$ for the 64-bit configuration

Syndrome bits are similarly labeled S_0 through S_7.

Correct	Diag Mode1	Diag Mode0	Diagnostic Mode Selected
X	0	0	**Non-diagnostic Mode.** Normal EDC function in this mode.
X	0	1	**Diagnostic Generate.** The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate Mode. The EDC functions normally in the Detect or Correct modes.
X	1	0	**Diagnostic Detect/Correct.** In either mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate Mode.
1	1	1	**Initialize.** The Data Input Latch outputs are forced to zeros and latched upon removal of Initialize Mode.
0	1	1	**PASSTHRU.**

2584 tbl 02

Table 2. Diagnostic Mode Control

Operating Mode	DM_1	DM_0	Generate	Correct	$DATA_{OUT}$ Latch	SC_{0-7} ($\overline{OE}_{SC}$ = LOW)	$\overline{ERROR}$ / $\overline{MULT\ ERROR}$
Generate	0 1	0 0	0	X	LE_{OUT} = LOW (1)	Check Bits Generated from $DATA_{IN}$ Latch	High
Detect	0 0	0 1	1	0	$DATA_{IN}$ Latch	Syndrome Bits $DATA_{IN}$/ Check Bit Latch	Error Dep (2)
Correct	0 0	0 1	1	1	$DATA_{IN}$ Latch w/ Single Bit Correction	Syndrome Bits $DATA_{IN}$/ Check Bit Latch	Error Dep
PASSTHRU	1	1	1	0	$DATA_{IN}$ Latch	Check Bit Latch	High
Diagnostic Generate	0	1	0	X	—	Check Bits from Diagnostic Latch	High
Diagnostic Detect	1	0	1	0	$DATA_{IN}$ Latch	Syndrome Bits $DATA_{IN}$/ Diagnostic Latch	Error Dep
Diagnostic Correct	1	0	1	1	$DATA_{IN}$ Latch w/ Single Bit Correction	Syndrome Bits $DATA_{IN}$/ Diagnostic Latch	Error Dep
Initialization	1	1	1	1	$DATA_{IN}$ Latch Set to 0000(3)	—	—
Internal	CODE $ID_{1,0}$ = 01 (Control Signals CODE $ID_{1,0}$, DIAG $MODE_{1,0}$ and CORRECT are taken from Diagnostic Latch.)						

NOTES: 2584 tbl 03

1. In Generate Mode, data is read into the EDC unit and the check bits are generated. The same data is written to memory along with the check bits. Since the $DATA_{OUT}$ Latch is not used in the Generate Mode, LE_{OUT} (being LOW since it is tied to Generate) does not affect the writing of check bits.
2. Error Dep (Error Dependent): $\overline{ERROR}$ will be low for single or multiple errors, with $\overline{MULT\ ERROR}$ low for double or multiple errors. Both signals are high for no errors.
3. LE_{IN} is LOW.

Table 3. IDT49C460 Operating Modes

OPERATING MODE SELECTION

Tables 2 and 3 describe the nine operating modes of the IDT49C460s. The Diagnostic Mode pins — DIAG MODE$_{0,1}$ — define four basic areas of operation. $\overline{\text{GENERATE}}$ and CORRECT further divide operation into 8 functions, with CODE ID$_{1,0}$ defining the ninth mode as the Internal Mode.

Generate Mode is used to display the check bits on the outputs SC$_{0-7}$. The Diagnostic Generate Mode displays check bits as stored in the Diagnostic Latch.

Detect Mode provides an indication of errors or multiple errors on the outputs $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$. Single bit errors are not corrected in this mode. The syndrome bits are provided on the outputs SC$_{0-7}$. For the Diagnostic Detect Mode, the syndrome bits are generated by comparing the internally generated check bits from the Data In Latch with check bits stored in the diagnostic latch rather than with the check bit latch contents.

Correct Mode is similar to the Detect Mode except that single bit errors will be complemented (corrected) and made available as input to the Data Out Latches. Again, the Diagnostic Correct Mode will correct single bit errors as determined by syndrome bits generated from the data input and contents of the diagnostic latches.

The Initialize Mode provides check bits for all zero bit data. Data Input Latches are set, latched to a logic zero and made available as input to the Data Out Latches.

The Internal Mode disables the external control pins DIAG MODE$_{0,1}$ and CORRECT to be defined by the Diagnostic Latch. Even CODE ID$_{1,0}$, although externally set to the 01 code, can be redefined from the Diagnostic Latch data.

Code ID$_1$	Code ID$_0$	Slice Selected
0	0	32-Bit
0	1	Internal Control Mode
1	0	64-Bit, Lower 32–Bit (0–31)
1	1	64-Bit, Upper 32-Bit (32–63)

2584 tbl 04

Table 4. Slice Identification

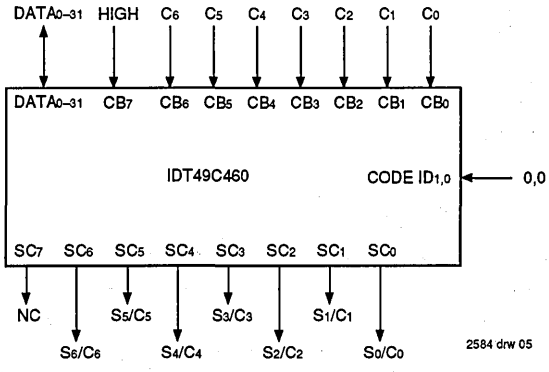


Figure 1. 32-Bit Configuration

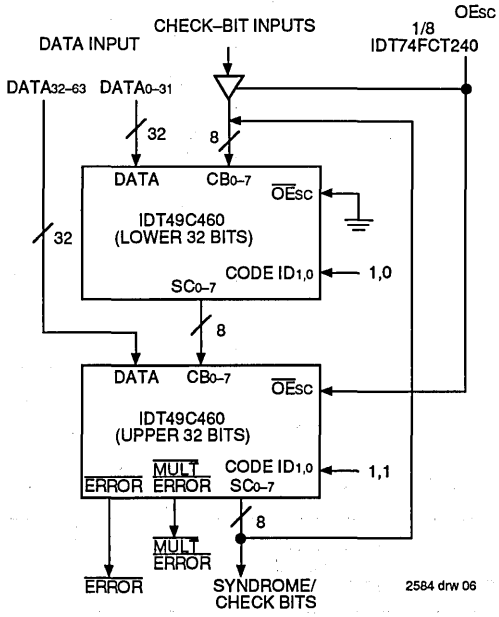


Figure 2. 64-Bit Configuration

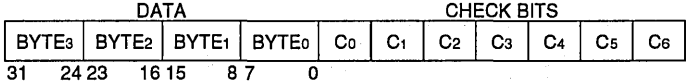


Figure 3. 32-Bit Data Format

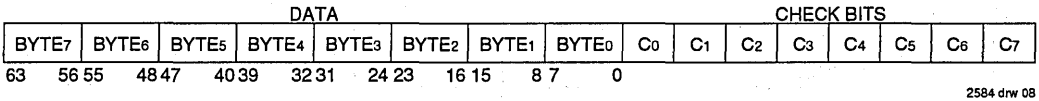


Figure 4. 64-Bit Data Format

32-BIT DATA WORD CONFIGURATION

A single IDT49C460 EDC unit, connected as shown in Figure 1, provides all the logic needed for single bit error correction and double bit error detection of a 32-bit data field. The identification code indicates 7 check bits are required. The CB_7 pin should be HIGH.

Figure 3 indicates the 39-bit data format for two bytes of data and 7 check bits. Table 3 describes the operating mode available.

Table 6 indicates the data bits participating in the check bit generation. For example, check bit C_0 is the exclusive-OR function of the 16 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization Mode. Check bits from the respective latch are passed, unchanged, in the PASSTHRU or Diagnostic Generate Mode.

Syndrome bits are generated by an exclusive-OR or the generated check bits with the read check bits. For example, S_n is the XOR of check bits C_n from those read with those generated. Table 7 indicates the decoding of the seven syndrome bits to identify the bit-in-error for a single bit error, or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Table 5 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the diagnostic check bits to determine syndrome bits or to pass as check bits to the SC_{0-7} outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

BIT 0	CB_0 DIAGNOSTIC
BIT 1	CB_1 DIAGNOSTIC
BIT 2	CB_2 DIAGNOSTIC
BIT 3	CB_3 DIAGNOSTIC
BIT 4	CB_4 DIAGNOSTIC
BIT 5	CB_5 DIAGNOSTIC
BIT 6	CB_6 DIAGNOSTIC
BIT 7	CB_7 DIAGNOSTIC
BIT 8	CODE ID_0
BIT 9	CODE ID_1
BIT 10	DIAG $MODE_0$
BIT 11	DIAG $MODE_1$
BIT 12	CORRECT
BIT 13–31	DON'T CARE

2584 drw 05

Table 5. 32-Bit Diagnostic Latch Coding Format

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C_0	Even (XOR)	X				X		X	X	X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								

2584 tbl 06

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
C_0	Even (XOR)		X	X	X		X					X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X

2584 tbl 07

Table 6. 32–Bit Modified Hamming Code–Check Bit Encode Chart

	Syndrome Bits				Hex	0	1	2	3	4	5	6	7
					S_6	0	0	0	0	1	1	1	1
					S_5	0	0	1	1	0	0	1	1
					S_4	0	1	0	1	0	1	0	1
Hex	S_3	S_2	S_1	S_0									
0	0	0	0	0		*	C4	C5	T	C6	T	T	30
1	0	0	0	1		C0	T	T	14	T	M	M	T
2	0	0	1	0		C1	T	T	M	T	2	24	T
3	0	0	1	1		T	18	8	T	M	T	T	M
4	0	1	0	0		C2	T	T	15	T	3	25	T
5	0	1	0	1		T	19	9	T	M	T	T	31
6	0	1	1	0		T	20	10	T	M	T	T	M
7	0	1	1	1		M	T	T	M	T	4	26	T
8	1	0	0	0		C3	T	T	M	T	5	27	T
9	1	0	0	1		T	21	11	T	M	T	T	M
A	1	0	1	0		T	22	12	T	1	T	T	M
B	1	0	1	1		17	T	T	M	T	6	28	T
C	1	1	0	0		T	23	13	T	M	T	T	M
D	1	1	0	1		M	T	T	M	T	7	29	T
E	1	1	1	0		16	T	T	M	T	M	M	T
F	1	1	1	1		T	M	M	T	0	T	T	M

2584 tbl 08

NOTES:
1. * = No errors detected
2. Number = The number of the single bit-in-error
3. T = Two errors detected
4. M = Three or more errors detected

Table 7. Syndrome Decode to Bit-in-Error (32-Bit)

64-BIT DATA WORD CONFIGURATION

Two IDT49C460 EDC units, connected as shown in Figure 2, provide all the logic needed for single bit error detection and double bit error detection of a 64-bit data field. Table 4 gives the CODE $ID_{1,0}$ values needed for distinguishing the upper 32 bits from the lower 32 bits. Valid syndrome, check bits and the $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ signals come from the IC with the CODE $ID_{1,0} = 11$. Control signals not indicated are connected to both units in parallel. The EDC with the CODE $ID_{1,0} = 10$ has the $\overline{OE}$sc grounded. The $\overline{OE}$sc selects the syndrome bits from the EDC with CODE $ID_{1,0} = 11$ and also controls the check bit buffers from memory.

Data In bits 0 through 31 are connected to the same numbered inputs of the EDC unit with CODE $ID_{1,0} = 10$, while Data In bits 32 through 63 are connected to Data Inputs 0 to 31, respectively, for the EDC unit with CODE $ID_{1,0} = 11$.

Figure 4 indicates the 72-bit data format of 8 bytes of data and 8 check bits. Check bits are input to the EDC unit with CODE $ID_{1,0} = 10$ through a three-state buffer unit such as the IDT74FCT244. Correction of single bit errors of the 64-bit configuration requires a feedback of syndrome bits from the upper EDC unit to the lower EDC unit. The MUX shown on the functional block diagram is used to select the CB_{0-7} pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 describes the operating modes available for the 64/72 configuration.

Table 11 indicates the data bits participating in the check bit generation. For example, check bit C_0 is the exclusive-OR function of the 32 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization modes. Check bits are passed as stored in the PASSTHRU or Diagnostic Generate modes.

Syndrome bits are generated by an exclusive-OR of the generated check bits with the read check bits. For example, S_n is the XOR of check bits C_n from those read with those generated. Table 9 indicates the decoding of the 8 syndrome bits to determine the bit in error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Tables 8A and 8B define the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic Check Bits to determine syndrome bits or to pass as check bits to the SC_{0-7} outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

Performance data is provided in Table 10, relating a single IDT49C460 EDC with the two cascaded units of Figure 2. As indicated, a summation of propagation delays is required from the cascading arrangement of EDC units.

Bit	Internal Function
0	CB_0 DIAGNOSTIC
1	CB_1 DIAGNOSTIC
2	CB_2 DIAGNOSTIC
3	CB_3 DIAGNOSTIC
4	CB_4 DIAGNOSTIC
5	CB_5 DIAGNOSTIC
6	CB_6 DIAGNOSTIC
7	CB_7 DIAGNOSTIC
8	CODE ID_0 LOWER 32-BIT
9	CODE ID_1 LOWER 32-BIT
10	DIAG $MODE_0$ LOWER 32-BIT
11	DIAG $MODE_1$ LOWER 32-BIT
12	CORRECT LOWER 32-BIT
13–31	DON'T CARE
32–39	DON'T CARE
40	CODE ID_0 UPPER 32-BIT
41	CODE ID_1 UPPER 32-BIT
42	DIAG $MODE_0$ UPPER 32-BIT
43	DIAG $MODE_1$ UPPER 32-BIT
44	CORRECT UPPER 32-BIT
45–63	DON'T CARE

2584 tbl 09

Table 8A. 64-Bit Diagnostic Latch–Coding Format (Diagnostic and Correct Mode)

8

Bit	Internal Function
0–7	DON'T CARE
8	CODE ID_0 LOWER 32-BIT
9	CODE ID_1 LOWER 32-BIT
10	DIAG $MODE_0$ LOWER 32-BIT
11	DIAG $MODE_1$ LOWER 32-BIT
12	CORRECT LOWER 32-BIT
13–31	DON'T CARE
32	CB_0 DIAGNOSTIC
33	CB_1 DIAGNOSTIC
34	CB_2 DIAGNOSTIC
35	CB_3 DIAGNOSTIC
36	CB_4 DIAGNOSTIC
37	CB_5 DIAGNOSTIC
38	CB_6 DIAGNOSTIC
39	CB_7 DIAGNOSTIC
40	CODE ID_0 UPPER 32-BIT
41	CODE ID_1 UPPER 32-BIT
42	DIAG $MODE_0$ UPPER 32-BIT
43	DIAG $MODE_1$ UPPER 32-BIT
44	CORRECT UPPER 32-BIT
45–63	DON'T CARE

2584 tbl 10

Table 8B. 64-Bit Diagnostic Latch–Coding Format (Diagnostic and Correct Mode)

					Hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
					S_7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Syndrome Bits				S_6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
					S_5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
					S_4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Hex	S_3	S_2	S_1	S_0																	
0	0	0	0	0		*	C4	C5	T	C6	T	T	62	C7	T	T	46	T	M	M	T
1	0	0	0	1		C0	T	T	14	T	M	M	T	T	M	M	T	M	T	T	30
2	0	0	1	0		C1	T	T	M	T	34	56	T	T	50	40	T	M	T	T	M
3	0	0	1	1		T	18	8	T	M	T	T	M	M	T	T	M	T	2	24	T
4	0	1	0	0		C2	T	T	15	T	35	57	T	T	51	41	T	M	T	T	31
5	0	1	0	1		T	19	9	T	M	T	T	63	M	T	T	47	T	3	25	T
6	0	1	1	0		T	20	10	T	M	T	T	M	M	T	T	M	T	4	26	T
7	0	1	1	1		M	T	T	M	T	36	58	T	T	52	42	T	M	T	T	M
8	1	0	0	0		C3	T	T	M	T	37	59	T	T	53	43	T	M	T	T	M
9	1	0	0	1		T	21	11	T	M	T	T	M	M	T	T	M	T	5	27	T
A	1	0	1	0		T	22	12	T	33	T	T	M	49	T	T	M	T	6	28	T
B	1	0	1	1		17	T	T	M	T	38	60	T	T	54	44	T	1	T	T	M
C	1	1	0	0		T	23	13	T	M	T	T	M	M	T	T	M	T	7	29	T
D	1	1	0	1		M	T	T	M	T	39	61	T	T	55	45	T	M	T	T	M
E	1	1	1	0		16	T	T	M	T	M	M	T	T	M	M	T	0	T	T	M
F	1	1	1	1		T	M	M	T	32	T	T	M	48	T	T	M	T	M	M	T

NOTES:
* = No errors detected
Number = The number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

2584 tbl 11

Table 9. Syndrome Decode to Bit–In–Error (64–Bit Configuration)

64–Bit Propagation Delay		Component Delay for IDT49C460 AC Specifications
From	To	
DATA	Check Bits Out	(DATA TO SC) + (CB TO SC, CODE ID 11)
DATA	Corrected $DATA_{OUT}$	(DATA TO SC) + (CB TO SC, CODE ID 11) + (CB TO DATA, CODE ID 10)
DATA	Syndromes Out	(DATA TO SC) + (CB TO SC, CODE ID 11)
DATA	$\overline{ERROR}$ for 64 Bits	(DATA TO SC) + (CB TO $\overline{ERROR}$, CODE ID 11)
DATA	$\overline{MULT\ ERROR}$ for 64 Bits	(DATA TO SC) + (CB TO $\overline{MULT\ ERROR}$, CODE ID 11)

2584 tbl 12

Table 10. Key Calculations for the 64–Bit Configuration

8

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								
C_7	Even (XOR)	X	X	X	X	X	X	X	X								

2584 tbl 13

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X
C_7	Even (XOR)									X	X	X	X	X	X	X	X

2584 tbl 14

Generated Check Bits	Parity	Participating Data Bits															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
C_0	Even (XOR)	X				X		X	X			X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								
C_7	Even (XOR)									X	X	X	X	X	X	X	X

2584 tbl 15

Generated Check Bits	Parity	Participating Data Bits															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
C_0	Even (XOR)	X				X		X	X			X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X
C_7	Even (XOR)	X	X	X	X	X	X	X	X								

NOTE:
1. The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

2584 tbl 16

Table 11. 64–Bit Modified Hamming Code–Check Bit Encoding

SC OUTPUTS

The tables below indicate how the SC0-7 outputs are generated in each control mode of various CODE IDs (Internal Control Mode not applicable).

Generate	CODE ID1,0		
	00	10	11
SC0 ←	PH0	PH1	PH2 ⊕ CB0
SC1 ←	PA	PA	PA ⊕ CB1
SC2 ←	PB	PB	PB ⊕ CB2
SC3 ←	PC	PC	PC ⊕ CB3
SC4 ←	PD	PD	PD ⊕ CB4
SC5 ←	PE	PE	PE ⊕ CB5
SC6 ←	PF	PF	PF ⊕ CB6
SC7 ←	—	PF	PG ⊕ CB7
	Final Check Bits	Partial Check Bits	Final Check Bits

2584 tbl 17

Correct/ Detect	CODE ID1,0		
	00	10	11
SC0 ←	PH0 ⊕ C0	PH1 ⊕ C0	PH2 ⊕ CB0
SC1 ←	PA ⊕ C1	PA ⊕ C1	PA ⊕ CB1
SC2 ←	PB ⊕ C2	PB ⊕ C2	PB ⊕ CB2
SC3 ←	PC ⊕ C3	PC ⊕ C3	PC ⊕ CB3
SC4 ←	PD ⊕ C4	PD ⊕ C4	PD ⊕ CB4
SC5 ←	PE ⊕ C5	PE ⊕ C5	PE ⊕ CB5
SC6 ←	PF ⊕ C6	PF ⊕ C6	PF ⊕ CB6
SC7 ←	—	PF ⊕ C7	PG ⊕ CB7
	Final Syndrome	Partial Syndrome	Final Syndrome

2584 tbl 19

Diagnostic Generate	CODE ID1,0		
	00	10	11
SC0 ←	DL0	DL0	DL32
SC1 ←	DL1	DL1	DL33
SC2 ←	DL2	DL2	DL34
SC3 ←	DL3	DL3	DL35
SC4 ←	DL4	DL4	DL36
SC5 ←	DL5	DL5	DL37
SC6 ←	DL6	DL6	DL38
SC7 ←	—	DL7	DL39
	Final Check Bits	Partial Check Bits	Final Check Bits

2584 tbl 18

Diagnostic Correct/ Detect	CODE ID1,0		
	00	10	11
SC0 ←	PH0 ⊕ DL0	PH1 ⊕ DL0	PH2 ⊕ CB0
SC1 ←	PA ⊕ DL1	PA ⊕ DL1	PA ⊕ CB1
SC2 ←	PB ⊕ DL2	PB ⊕ DL2	PB ⊕ CB2
SC3 ←	PC ⊕ DL3	PC ⊕ DL3	PC ⊕ CB3
SC4 ←	PD ⊕ DL4	PD ⊕ DL4	PD ⊕ CB4
SC5 ←	PE ⊕ DL5	PE ⊕ DL5	PE ⊕ CB5
SC6 ←	PF ⊕ DL6	PF ⊕ DL6	PF ⊕ CB6
SC7 ←	—	PF ⊕ DL7	PG ⊕ CB7
	Final Syndrome	Partial Syndrome	Final Syndrome

2584 tbl 20

PASSTHRU	CODE ID1,0		
	00	10	11
SC0 ←	C0	C0	CB0
SC1 ←	C1	C1	CB1
SC2 ←	C2	C2	CB2
SC3 ←	C3	C3	CB3
SC4 ←	C4	C4	CB4
SC5 ←	C5	C5	CB5
SC6 ←	C6	C6	CB6
SC7 ←	—	C7	CB7

2584 tbl 21

Table 12. SC0-7 Outputs For Different Control Modes

8

DATA CORRECTION

The tables below indicate which data output bits are corrected depending upon the syndromes and the CODE $ID_{1,0}$ position. The syndromes that determine data correction are, in some cases, syndromes input externally via the CB inputs and, in some cases, syndromes input externally by that EDC (S_i are the internal syndromes and are the same as the value of the SC_i output of that EDC if enabled).

FUNCTIONAL EQUATIONS

The equations below describe the IDT49C460 output values as defined by the value of the inputs and internal states.

DEFINITIONS

$$PA = D_0 \oplus D_1 \oplus D_2 \oplus D_4 \oplus D_6 \oplus D_8 \oplus D_{10} \oplus D_{12} \oplus D_{16} \oplus D_{17} \oplus D_{18} \oplus D_{20} \oplus D_{22} \oplus D_{24} \oplus D_{26} \oplus D_{28}$$

$$\overline{PB} = D_0 \oplus D_3 \oplus D_4 \oplus D_7 \oplus D_9 \oplus D_{10} \oplus D_{13} \oplus D_{15} \oplus D_{16} \oplus D_{19} \oplus D_{20} \oplus D_{23} \oplus D_{25} \oplus D_{26} \oplus D_{29} \oplus D_{31}$$

$$\overline{PC} = D_0 \oplus D_1 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{16} \oplus D_{17} \oplus D_{21} \oplus D_{22} \oplus D_{23} \oplus D_{27} \oplus D_{28} \oplus D_{29}$$

$$PD = D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{14} \oplus D_{15} \oplus D_{18} \oplus D_{19} \oplus D_{20} \oplus D_{21} \oplus D_{22} \oplus D_{23} \oplus D_{30} \oplus D_{31}$$

$$PE = D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14} \oplus D_{15} \oplus D_{24} \oplus D_{25} \oplus D_{26} \oplus D_{27} \oplus D_{28} \oplus D_{29} \oplus D_{30} \oplus D_{31}$$

$$PF = D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{24} \oplus D_{25} \oplus D_{26} \oplus D_{27} \oplus D_{28} \oplus D_{29} \oplus D_{30} \oplus D_{31}$$

$$PG = D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14} \oplus D_{15} \oplus D_{16} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{20} \oplus D_{21} \oplus D_{22} \oplus D_{23}$$

$$PH0 = D_0 \oplus D_4 \oplus D_6 \oplus D_7 \oplus D_8 \oplus D_9 \oplus D_{11} \oplus D_{14} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{21} \oplus D_{26} \oplus D_{28} \oplus D_{29} \oplus D_{31}$$

$$PH1 = D_1 \oplus D_2 \oplus D_3 \oplus D_5 \oplus D_8 \oplus D_9 \oplus D_{11} \oplus D_{14} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{21} \oplus D_{24} \oplus D_{25} \oplus D_{27} \oplus D_{30}$$

$$PH2 = D_0 \oplus D_4 \oplus D_6 \oplus D_7 \oplus D_{10} \oplus D_{12} \oplus D_{13} \oplus D_{15} \oplus D_{16} \oplus D_{20} \oplus D_{22} \oplus D_{23} \oplus D_{26} \oplus D_{28} \oplus D_{29} \oplus D_{31}$$

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to VCC + 0.5V	–0.5 to VCC + 0.5V	V
VCC	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	30	30	mA

NOTE: 2584 tbl 24

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = + 25°C, f = 1.0MHz)

Symbol	Parameter [1]	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	5	pF
COUT	Output Capacitance	VOUT = 0V	7	pF

NOTE: 2584 tbl 25

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = –55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions [1]		Min.	Typ. [2]	Max.	Unit
VIH	Input HIGH Level	Guaranteed Logic HIGH Level[4]		2.0	—	—	V
VIL	Input LOW Level	Guaranteed Logic LOW Level[4]		—	—	0.8	V
IIH	Input HIGH Current	Vcc = Max., VIN = Vcc		—	0.1	10.0	µA
IIL	Input LOW Current	Vcc = Max., VIN = GND		—	–0.1	–10.0	µA
VOH	Output HIGH Voltage	Vcc = Min.	IOH = 300µA	Vcc	—	—	V
			IOH = –12mA Mil.	2.4	4.3	—	
			IOH = –15mA Com'l.	2.4	4.3	—	
VOL	Output LOW Voltage	Vcc = Min.	IOL = 300µA	—	—	GND	V
			IOL = 12mA Mil.	—	0.3	0.5	
			IOL = 16mA Com'l.	—	0.3	0.5	
IOZ	Off State (High Impedance) Output Current	Vcc = Max.	VO = 0V	—	–0.1	–20.0	µA
			VO = Vcc (Max.)	—	0.1	20.0	
IOS	Output Short Circuit Current	Vcc = Max., VOUT = 0V[3]		–30.0	—	—	mA

NOTES: 2584 tbl 26

1. For conditions shown as Max. or Min. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, + 25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

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DC ELECTRICAL CHARACTERISTICS (Cont'd.)

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{CCQ}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max.; All Inputs $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{OP} = 0; Outputs Disabled		—	3.0	10	mA
I_{CCT}	Quiescent Input Power Supply Current (per Input @ TTL High) (5)	V_{CC} = Max., V_{IN} = 3.4V, f_{OP} = 0		—	0.3	0.75	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max.	MIL.	—	6	10	mA/ MHz
		$V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	COM'L.	—	6	7	
I_{CC}	Total Power Supply Current (6)	V_{CC} = Max., f_{OP} = 10MHz	MIL.	—	60	110	mA
		Outputs Open, $\overline{OE}$ = L 50 % Duty cycle $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$	COM'L.	—	60	80	
		V_{CC} = Max., f_{OP} = 10MHz	MIL.	—	70	125	
		Outputs Open, $\overline{OE}$ = L 50 % Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	COM'L.	—	70	95	

NOTES: 2584 tbl 27

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQ}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:
   $I_{CC} = I_{CCQ} + I_{CCT} (N_T \times D_H) + I_{CCD} (f_{OP})$
   D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
   N_T = Number of dynamic inputs driven at TTL levels.
   f_{OP} = Operating frequency in Megahertz.

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \le 0V$ and $V_{IH} \ge 3V$ for AC tests.

IDT49C460D AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance) Temperature range: 0°C to +70°C, Vcc = 5.0V ± 5%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS(1)

	From Input		To Output: SC0–7	To Output: DATA0–31	To Output: ERROR	To Output: MULT ERROR	Unit
	DATA0–31(3)		14	18(2)	12	15	ns
	CB0–7 (CODE ID1,0 = 00, 11)		11	16	10	12	ns
	CB0–7 (CODE ID1,0 = 10)		12	12	—	—	ns
	LEOUT/GENERATE	↑	—	9	↓ 7	↓ 8	ns
		↓	14	—	↑ 7	↑ 8	ns
	CORRECT Not Internal Control Mode		—	12	—	—	ns
	DIAG MODE Not Internal Control Mode		12	20	10	15	ns
	CODE ID1,0		14(6)	18	13	16	ns
	LEIN From latched to Transparent		17	21	14	17	ns
	LEDIAG From latched to Transparent	↑	12(6)	18	12	14	ns
Internal Control Mode	LEDIAG From latched to Transparent	↑	12(6)	17	12	14	ns
Internal Control Mode	DATA0–31 Via Diagnostic Latch	↑	12	19(2)	10	12	ns

2584 tbl 28

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)	Set-up Time Min.	Hold Time Min.	Unit
DATA0–31 (4)	↓	LEIN	3	3	ns
CB0–7 (4)	↓	LEIN	2	3	ns
DATA0–31 (4, 6)	↓	LEOUT/GENERATE	5 (15)	0	ns
CB0–7 (CODE ID 00, 11) (4, 6)	↓	LEOUT/GENERATE	11	0	ns
CB0–7 (CODE ID 10) (4, 6)	↓	LEOUT/GENERATE	6	0	ns
CORRECT (4, 6)	↑	LEOUT/GENERATE	6	0	ns
DIAG MODE (4, 6)	↓	LEOUT/GENERATE	13	0	ns
CODE ID1,0 (4, 6)	↓	LEOUT/GENERATE	8	0	ns
LEIN (4, 6)	↑	LEOUT/GENERATE	14	0	ns
DATA0–31 (4, 6)		LEDIAG	3	3	ns

NOTE: (15) above applies to correction path.

2584 tbl 29

OUTPUT ENABLE/DISABLE TIMES(5)

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
OE Byte0–3	↓	↑	DATA0–31	0	8	0	10	ns
OESC	↓	↑	SC0–7	0	8	0	10	ns

2584 tbl 30

MINIMUM PULSE WIDTHS(6)

	Min.		
LEIN, LEOUT/GENERATE, LEDIAG ↑↓ (Positive-going pulse)	5		ns

NOTES:

2584 tbl 31

1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5pF.
6. Not production tested, guaranteed by characterization.

8

IDT49C460D AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance) Temperature range: –55°C to +125°C, Vcc = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC0–7	To Output: DATA0–31	To Output: ERROR	To Output: MULT ERROR	Unit
	DATA0–31[3]		17	22 [2]	16	18	ns
	CB0–7 (CODE ID1,0 = 00, 11)		13	17	12	14	ns
	CB0–7 (CODE ID1,0 = 10)		13	14	—	—	ns
	LEOUT/GENERATE	↑	—	10	↓ 8	↓ 8	ns
		↓	15	—	↑ 8	↑ 9	ns
	CORRECT Not Internal Control Mode		—	13	—	—	ns
	DIAG MODE Not Internal Control Mode		14	22	12	17	ns
	CODE ID1,0		16 [6]	20	15	18	ns
	LEIN From latched to Transparent		18	24	16	19	ns
	LEDIAG From latched to Transparent	↑	14 [6]	20	13	16	ns
Internal Control Mode	LEDIAG From latched to Transparent	↑	14 [6]	19	14	16	ns
	DATA0–31 Via Diagnostic Latch	↑	14	22 [2]	11	14	ns

2584 tbl 32

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)	Set-up Time Min.	Hold Time Min.	Unit
DATA0–31 [4]	↓	LEIN	3	3	ns
CB0–7 [4]	↓	LEIN	2	3	ns
DATA0–31 [4, 6]	↓	LEOUT/GENERATE	6 [15]	0	ns
CB0–7 (CODE ID 00, 11) [4, 6]	↓	LEOUT/GENERATE	12	0	ns
CB0–7 (CODE ID 10) [4, 6]	↓	LEOUT/GENERATE	8	0	ns
CORRECT [4, 6]	↑ ↓	LEOUT/GENERATE	7	0	ns
DIAG MODE [4, 6]	↓	LEOUT/GENERATE	14	0	ns
CODE ID1,0 [4, 6]	↓	LEOUT/GENERATE	9	0	ns
LEIN [4, 6]	↑ ↓	LEOUT/GENERATE	16	0	ns
DATA0–31 [4, 6]		LEDIAG	3	3	ns

NOTE: (15) above applies to correction path.

2584 tbl 33

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
OE Byte0–3	↓	↑	DATA0–31	0	10	0	12	ns
OESC	↓	↑	SC0–7	0	10	0	12	ns

2584 tbl 34

MINIMUM PULSE WIDTHS[6]

	Min.		
LEIN, LEOUT/GENERATE, LEDIAG ↑↓ (Positive–going pulse)	5		ns

2584 tbl 35

NOTES:
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5F.
6. Not production tested, guaranteed by characterization.

IDT49C460C AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance) Temperature range: 0°C to +70°C, Vcc = 5.0V ± 5%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC0–7	To Output: DATA0–31	To Output: $\overline{\text{ERROR}}$	To Output: $\overline{\text{MULT ERROR}}$	Unit
	DATA0–31[3]		19	24 [2]	16	20	ns
	CB0–7 (CODE ID1,0 = 00, 11)		14	21	12	16	ns
	CB0–7 (CODE ID1,0 = 10)		14	16	—	—	ns
	LEOUT/$\overline{\text{GENERATE}}$	↑	—	12	↓ 9	↓ 11	ns
		↓	18	—	↑ 9	↑ 11	ns
	CORRECT Not Internal Control Mode		—	16	—	—	ns
	DIAG MODE Not Internal Control Mode		16	26	11	20	ns
	CODE ID1,0		18 [6]	23	17	21	ns
	LEIN From latched to Transparent		22	28 [2]	19	22	ns
	LEDIAG From latched to Transparent	↑	15 [6]	24	15	19	ns
Internal Control Mode	LEDIAG From latched to Transparent	↑	16 [6]	22	15	18	ns
Internal Control Mode	DATA0–31 Via Diagnostic Latch	↑	15	25 [2]	13	16	ns

2584 tbl 36

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
DATA0–31 [4]		↓	LEIN	3	4	ns
CB0–7 [4]		↓	LEIN	2	4	ns
DATA0–31 [4, 6]		↓	LEOUT/$\overline{\text{GENERATE}}$	6 [16]	0	ns
CB0–7 (CODE ID 00, 11) [4, 6]		↓	LEOUT/$\overline{\text{GENERATE}}$	14	0	ns
CB0–7 (CODE ID 10) [4, 6]		↓	LEOUT/$\overline{\text{GENERATE}}$	8	0	ns
CORRECT [4, 6]	↑	↓	LEOUT/$\overline{\text{GENERATE}}$	8	0	ns
DIAG MODE [4, 6]		↓	LEOUT/$\overline{\text{GENERATE}}$	17	0	ns
CODE ID1,0 [4, 6]		↓	LEOUT/$\overline{\text{GENERATE}}$	10	0	ns
LEIN [4, 6]	↑	↓	LEOUT/$\overline{\text{GENERATE}}$	19	0	ns
DATA0–31 [4, 6]			LEDIAG	3	3	ns

NOTE: (16) above applies to correction path.

2584 tbl 37

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
$\overline{\text{OE}}$ Byte0–3	↓	↑	DATA0–31	0	10	0	12	ns
$\overline{\text{OE}}$SC	↓	↑	SC0–7	0	10	0	12	ns

2584 tbl 38

MINIMUM PULSE WIDTHS[6]

	Min.		
LEIN, LEOUT/$\overline{\text{GENERATE}}$, LEDIAG ↑↓ (Positive–going pulse)	6		ns

2584 tbl 39

NOTES:
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5pF.
6. Not production tested, guaranteed by characterization.

8

IDT49C460C AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance) Temperature range: –55°C to +125°C, Vcc = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS(1)

	From Input		To Output: SC0–7	To Output: DATA0–31	To Output: ERROR	To Output: MULT ERROR	Unit
	DATA0–31 (3)		22	29 (2)	21	24	ns
	CB0–7 (CODE ID1,0 = 00, 11)		17	23	16	18	ns
	CB0–7 (CODE ID1,0 = 10)		17	18	—	—	ns
	LEOUT/GENERATE	↑	—	13	↓ 10	↓ 12	ns
		↓	20	—	↑ 10	↑ 12	ns
	CORRECT Not Internal Control Mode		—	17	—	—	ns
	DIAG MODE Not Internal Control Mode		18	29	12	23	ns
	CODE ID1,0		21 (6)	26	20	24	ns
	LEIN From latched to Transparent		24	32	21	25	ns
	LEDIAG From latched to Transparent	↑	18 (6)	27	17	21	ns
Internal Control Mode	LEDIAG From latched to Transparent	↑	19 (6)	25	18	21	ns
Internal Control Mode	DATA0–31 Via Diagnostic Latch	↑	18	29 (2)	14	18	ns

2584 tbl 40

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)	Set-up Time Min.	Hold Time Min.	Unit
DATA0–31 (4)	↓	LEIN	3	4	ns
CB0–7 (4)	↓	LEIN	2	4	ns
DATA0–31 (4, 6)	↓	LEOUT/GENERATE	7 (19)	3	ns
CB0–7 (CODE ID 00, 11) (4, 6)	↓	LEOUT/GENERATE	16	0	ns
CB0–7 (CODE ID 10) (4, 6)	↓	LEOUT/GENERATE	10	0	ns
CORRECT (4, 6)	↑ ↓	LEOUT/GENERATE	9	0	ns
DIAG MODE (4, 6)	↓	LEOUT/GENERATE	19	0	ns
CODE ID1,0 (4, 6)	↓	LEOUT/GENERATE	12	0	ns
LEIN (4, 6)	↑ ↓	LEOUT/GENERATE	21	0	ns
DATA0–31 (4, 6)		LEDIAG	3	3	ns

Note: (19) above applies to correction path.

2584 tbl 41

OUTPUT ENABLE/DISABLE TIMES(5)

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
OE Byte0–3	↓	↑	DATA0–31	0	12	0	14	ns
OESC	↓	↑	SC0–7	0	12	0	14	ns

2584 tbl 42

MINIMUM PULSE WIDTHS(6)

	Min.		
LEIN, LEOUT/GENERATE, LEDIAG ↑↓ (Positive–going pulse)	6		ns

2584 tbl 43

NOTES:
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5F.
6. Not production tested, guaranteed by characterization.

IDT49C460B AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance) Temperature range: 0°C to +70°C, Vcc = 5.0V ± 5%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC0–7	To Output: DATA0–31	To Output: ERROR		To Output: MULT ERROR		Unit
	DATA0–31 [3]		25	30 [2]	25		27		ns
	CB0–7 (CODE ID1,0 = 00, 11)		14	30	17		20		ns
	CB0–7 (CODE ID1,0 = 10)		16	18	—		—		ns
	LEOUT/GENERATE	↑	—	12	↓	23	↓	23	ns
		↓	21	—	↑	23	↑	23	ns
	CORRECT Not Internal Control Mode		—	23	—		—		ns
	DIAG MODE Not Internal Control Mode		17	26	20		24		ns
	CODE ID1,0		18 [6]	26	21		26		ns
	LEIN From latched to Transparent		27	38 [2]	30		3		ns
	LEDIAG From latched to Transparent	↑	15 [6]	29	19		22		ns
Internal Control Mode	LEDIAG From latched to Transparent	↑	16 [6]	32	19		24		ns
Internal Control Mode	DATA0–31 Via Diagnostic Latch	↑	16	32 [2]	20		25		ns

2584 tbl 44

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
DATA0–31 [4]		↓	LEIN	4	4	ns
CB0–7 [4]		↓	LEIN	4	4	ns
DATA0–31 [4, 6]		↓	LEOUT/GENERATE	19	0	ns
CB0–7 (CODE ID 00, 11) [4, 6]		↓	LEOUT/GENERATE	15	0	ns
CB0–7 (CODE ID 10) [4, 6]		↓	LEOUT/GENERATE	15	0	ns
CORRECT [4, 6]	↑	↓	LEOUT/GENERATE	11	0	ns
DIAG MODE [4, 6]		↓	LEOUT/GENERATE	17	0	ns
CODE ID1,0 [4, 6]		↓	LEOUT/GENERATE	17	0	ns
LEIN [4, 6]	↑	↓	LEOUT/GENERATE	20	0	ns
DATA0–31 [4, 6]			LEDIAG	4	3	ns

2584 tbl 45

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
OE Byte0–3	↓	↑	DATA0–31	0	12	0	14	ns
OESC	↓	↑	SC0–7	0	12	0	14	ns

2584 tbl 46

MINIMUM PULSE WIDTHS

	Min.		
LEIN, LEOUT/GENERATE, LEDIAG ↑↓ (Positive–going pulse)	9		ns

2584 tbl 47

NOTES:
1. CI = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with CI = 5pF and measured to 0.5V change of output level. Testing is performed at CI = 50pF and correlated to CI = 5pF.
6. Not production tested, guaranteed by characterization.

8

IDT49C460B AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance) Temperature range: –55°C to +125°C, Vcc = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC0–7	To Output: DATA0–31	To Output: ERROR	To Output: MULT ERROR	Unit
	DATA0–31[3]		28	33[2]	28	30	ns
	CB0–7 (CODE ID1,0 = 00, 11)		17	33	20	23	ns
	CB0–7 (CODE ID1,0 = 10)		19	23	—	—	ns
	LEOUT/GENERATE	↑	—	15	↓ 26	↓ 26	ns
		↓	24	—	↑ 26	↑ 26	ns
	CORRECT Not Internal Control Mode		—	26	—	—	ns
	DIAG MODE Not Internal Control Mode		20	29	23	27	ns
	CODE ID1,0		21	29	24	29	ns
	LEIN From latched to Transparent		30	41	33	36	ns
	LEDIAG From latched to Transparent	↑	18	32	22	25	ns
Internal Control Mode	LEDIAG From latched to Transparent	↑	19	35	22	27	ns
Internal Control Mode	DATA0–31 Via Diagnostic Latch	↑	19	35[2]	23	28	ns

2584 tbl 48

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)	Set-up Time Min.	Hold Time Min.	Unit
DATA0–31 [4]	↓	LEIN	4	4	ns
CB0–7 [4]	↓	LEIN	4	4	ns
DATA0–31 [4, 6]	↓	LEOUT/GENERATE	23	0	ns
CB0–7 (CODE ID 00, 11) [4, 6]	↓	LEOUT/GENERATE	18	0	ns
CB0–7 (CODE ID 10) [4, 6]	↓	LEOUT/GENERATE	18	0	ns
CORRECT [4, 6]	↑	LEOUT/GENERATE	14	0	ns
DIAG MODE [4, 6]	↓	LEOUT/GENERATE	20	0	ns
CODE ID1,0 [4, 6]	↓	LEOUT/GENERATE	20	0	ns
LEIN [4, 6]	↑	LEOUT/GENERATE	23	0	ns
DATA0–31 [4, 6]		LEDIAG	4	3	ns

2584 tbl 49

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
OE Byte0–3	↓	↑	DATA0–31	0	12	0	14	ns
OESC	↓	↑	SC0–7	0	12	0	14	ns

2584 tbl 50

MINIMUM PULSE WIDTHS

	Min.		
LEIN, LEOUT/GENERATE, LEDIAG ↑↓ (Positive–going pulse)	12		ns

2584 tbl 51

NOTES:
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5pF.
6. Not production tested, guaranteed by characterization.

IDT49C460A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance) Temperature range: 0°C to 70°C, Vcc = 5.0V ± 5%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC0-7	To Output: DATA0-31	To Output: ERROR	To Output: MULT ERROR	Unit
	DATA0-31[3]		27	36[2]	30	33	ns
	CB0-7 (CODE ID1,0 = 00, 11)		16	34	19	23	ns
	CB0-7 (CODE ID1,0 = 10)		16	20	—	—	ns
	LEOUT/GENERATE	↑	—	12	↓ 25	↓ 25	ns
		↓	21	—	↑ 25	↑ 25	ns
	CORRECT Not Internal Control Mode		—	23	—	—	ns
	DIAG MODE Not Internal Control Mode		17	26	20	24	ns
	CODE ID1,0		18	26	21	26	ns
	LEIN From latched to Transparent		27	38	30	33	ns
	LEDIAG From latched to Transparent	↑	15	29	19	22	ns
Internal Control Mode	LEDIAG From latched to Transparent	↑	16	32	29	24	ns
Internal Control Mode	DATA0-31 Via Diagnostic Latch	↑	16	32[2]	20	25	ns

2584 tbl 52

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
DATA0-31 [4]		↓	LEIN	5	4	ns
CB0-7 [4]		↓	LEIN	5	4	ns
DATA0-31 [4, 6]		↓	LEOUT/GENERATE	23	0	ns
CB0-7 (CODE ID 00, 11) [4, 6]		↓	LEOUT/GENERATE	15	0	ns
CB0-7 (CODE ID 10) [4, 6]		↓	LEOUT/GENERATE	15	0	ns
CORRECT [4, 6]	↑	↓	LEOUT/GENERATE	11	0	ns
DIAG MODE [4, 6]		↓	LEOUT/GENERATE	17	0	ns
CODE ID1,0 [4, 6]		↓	LEOUT/GENERATE	17	0	ns
LEIN [4, 6]	↑	↓	LEOUT/GENERATE	25	0	ns
DATA0-31 [4, 6]			LEDIAG	5	3	ns

2584 tbl 53

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
OE Byte0-3	↓	↑	DATA0-31	0	12	0	14	ns
OESC	↓	↑	SC0-7	0	12	0	14	ns

2584 tbl 54

MINIMUM PULSE WIDTHS

	Min.		
LEIN, LEOUT/GENERATE, LEDIAG ↑↓ (Positive-going pulse)	9		ns

2584 tbl 55

NOTES:
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5pF.
6. Not production tested, guaranteed by characterization.

8

IDT49C460A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance) Temperature range: –55°C to +125°C, Vcc = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC0–7	To Output: DATA0–31	To Output: $\overline{\text{ERROR}}$	To Output: $\overline{\text{MULT ERROR}}$	Unit
	DATA0–31[3]		30	39[2]	33	36	ns
	CB0–7 (CODE ID1,0 = 00, 11)		19	37	22	26	ns
	CB0–7 (CODE ID1,0 = 10)		19	23	—	—	ns
	LEOUT/$\overline{\text{GENERATE}}$	↑	—	15	↓ 28	↓ 28	ns
		↓	24	—	↑ 28	↑ 28	ns
	CORRECT Not Internal Control Mode		—	26	—	—	ns
	DIAG MODE Not Internal Control Mode		20	29	23	27	ns
	CODE ID1,0		21	29	24	29	ns
	LEIN From latched to Transparent		30	41	33	36	ns
	LEDIAG From latched to Transparent	↑	18	32	22	25	ns
Internal Control Mode	LEDIAG From latched to Transparent	↑	19	35	22	27	ns
Internal Control Mode	DATA0–31 Via Diagnostic Latch	↑	19	35[2]	23	28	ns

2584 tbl 52

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)	Set-up Time Min.	Hold Time Min.	Unit
DATA0–31 [4]	↓	LEIN	5	4	ns
CB0–7 [4]	↓	LEIN	5	4	ns
DATA0–31 [4, 6]	↓	LEOUT/$\overline{\text{GENERATE}}$	27	0	ns
CB0–7 (CODE ID 00, 11) [4, 6]	↓	LEOUT/$\overline{\text{GENERATE}}$	18	0	ns
CB0–7 (CODE ID 10) [4, 6]	↓	LEOUT/$\overline{\text{GENERATE}}$	18	0	ns
CORRECT [4, 6]	↑ ↓	LEOUT/$\overline{\text{GENERATE}}$	14	0	ns
DIAG MODE [4, 6]	↓	LEOUT/$\overline{\text{GENERATE}}$	20	0	ns
CODE ID1,0 [4, 6]	↓	LEOUT/$\overline{\text{GENERATE}}$	20	0	ns
LEIN [4, 6]	↑ ↓	LEOUT/$\overline{\text{GENERATE}}$	28	0	ns
DATA0–31 [4, 6]		LEDIAG	5	3	ns

2584 tbl 53

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
$\overline{\text{OE}}$ Byte0–3	↓	↑	DATA0–31	0	12	0	14	ns
$\overline{\text{OE}}$SC	↓	↑	SC0–7	0	12	0	14	ns

2584 tbl 54

MINIMUM PULSE WIDTHS

	Min.		
LEIN, LEOUT/$\overline{\text{GENERATE}}$, LEDIAG ↑↓ (Positive-going pulse)	12		ns

2584 tbl 31

NOTES:
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5pF.
6. Not production tested, guaranteed by characterization.

IDT49C460 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance) Temperature range: 0°C to +70°C, Vcc = 5.0V ± 5%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC0–7	To Output: DATA0–31	To Output: ERROR		To Output: MULT ERROR		Unit
	DATA0–31[3]		37	49[2]	40		45		ns
	CB0–7 (CODE ID1,0 = 00, 11)		22	46	26		31		ns
	CB0–7 (CODE ID1,0 = 10)		22	30	—		—		ns
	LEOUT/GENERATE	↑	—	17	↓	30	↓	30	ns
		↓	29	—	↑	30	↑	30	ns
	CORRECT Not Internal Control Mode		—	31	—		—		ns
	DIAG MODE Not Internal Control Mode		23	35	27		33		ns
	CODE ID1,0		25	35	29		35		ns
	LEIN From latched to Transparent		37	51	41		45		ns
	LEDIAG From latched to Transparent	↑	21	38	26		30		ns
Internal Control Mode	LEDIAG From latched to Transparent	↑	22	42	26		33		ns
Internal Control Mode	DATA0–31 Via Diagnostic Latch	↑	22	42[2]	27		34		ns

2584 tbl 60

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
DATA0–31 [4]		↓	LEIN	6	4	ns
CB0–7 [4]		↓	LEIN	5	4	ns
DATA0–31 [4, 6]		↓	LEOUT/GENERATE	30	0	ns
CB0–7 (CODE ID 00, 11) [4, 6]		↓	LEOUT/GENERATE	20	0	ns
CB0–7 (CODE ID 10) [4, 6]		↓	LEOUT/GENERATE	20	0	ns
CORRECT [4, 6]	↑	↓	LEOUT/GENERATE	16	0	ns
DIAG MODE [4, 6]		↓	LEOUT/GENERATE	23	0	ns
CODE ID1,0 [4, 6]		↓	LEOUT/GENERATE	23	0	ns
LEIN [4, 6]	↑	↓	LEOUT/GENERATE	31	0	ns
DATA0–31 [4, 6]			LEDIAG	6	3	ns

2584 tbl 61

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
OE Byte0–3	↓	↑	DATA0–31	0	15	0	17	ns
OESC	↓	↑	SC0–7	0	15	0	17	ns

MINIMUM PULSE WIDTHS

	Min.		
LEIN, LEOUT/GENERATE, LEDIAG ↑↓ (Positive-going pulse)	12		ns

2584 tbl 63

NOTES:
1. CI = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with CI = 5pF and measured to 0.5V change of output level. Testing is performed at CI = 50pF and correlated to CI = 5pF.
6. Not production tested, guaranteed by characterization.

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IDT49C460 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance) Temperature range: –55°C to +125°C, Vcc = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC0–7	To Output: DATA0–31	To Output: ERROR		To Output: MULT ERROR		Unit
	DATA0–31[3]		40	52[2]	44		48		ns
	CB0–7 (CODE ID1,0 = 00, 11)		25	49	29		34		ns
	CB0–7 (CODE ID1,0 = 10)		25	33	—		—		ns
	LEOUT/GENERATE	↑	—	20	↓	33	↓	33	ns
		↓	32	—	↑	33	↑	33	ns
	CORRECT Not Internal Control Mode		—	34	—		—		ns
	DIAG MODE Not Internal Control Mode		26	38	30		36		ns
	CODE ID1,0		28	38	32		38		ns
	LEIN From latched to Transparent		40	54	44		48		ns
	LEDIAG From latched to Transparent	↑	24	42	29		33		ns
Internal Control Mode	LEDIAG From latched to Transparent	↑	25	47[2]	29		36		ns
Internal Control Mode	DATA0–31 Via Diagnostic Latch	↑	25	47	30		37		ns

2584 tbl 64

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
DATA0–31 [4]		↓	LEIN	6	4	ns
CB0–7 [4]		↓	LEIN	5	4	ns
DATA0–31 [4, 6]		↓	LEOUT/GENERATE	36	0	ns
CB0–7 (CODE ID 00, 11) [4, 6]		↓	LEOUT/GENERATE	24	0	ns
CB0–7 (CODE ID 10) [4, 6]		↓	LEOUT/GENERATE	24	0	ns
CORRECT [4, 6]	↑	↓	LEOUT/GENERATE	20	0	ns
DIAG MODE [4, 6]		↓	LEOUT/GENERATE	28	0	ns
CODE ID1,0 [4, 6]		↓	LEOUT/GENERATE	28	0	ns
LEIN [4, 6]	↑	↓	LEOUT/GENERATE	37	0	ns
DATA0–31 [4, 6]			LEDIAG	6	3	ns

2584 tbl 66

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
OE Byte0–3	↓	↑	DATA0–31	0	15	0	17	ns
OESC	↓	↑	SC0–7	0	15	0	17	ns

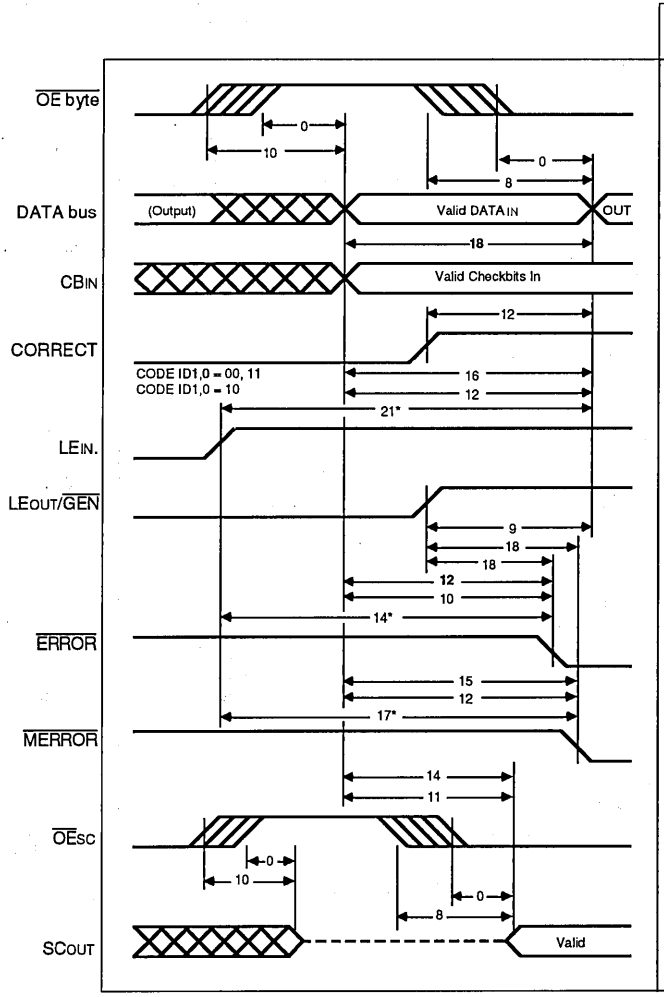
MINIMUM PULSE WIDTHS

	Min.		
LEIN, LEOUT/GENERATE, LEDIAG ↑↓ (Positive–going pulse)	15		ns

2584 tbl 67

NOTES:
1. Cl = 5pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5pF.
6. Not production tested, guaranteed by characterization.

DETECT OR CORRECTION MODE (FROM GENERATE MODE)



Propagation Delay From	To	Min./Max.
$\overline{OE}$ byte = High to DATAOUT Disabled		Min.
$\overline{OE}$ byte = High to DATAOUT Disabled		Max.
$\overline{OE}$ byte = Low to DATAOUT Enabled		Min.
$\overline{OE}$ byte = Low to DATAOUT Enabled		Max.
(Corrected DATA if Correct Mode) (DATAIN if Detect Mode)		
DATAIN	**to DATAOUT**	**Max.**
CORRECT = High to DATAOUT		Max.
CBIN	to DATAOUT	Max.
CBIN	to DATAOUT	Max.
*LEIN = High to DATAOUT		Max.
LEOUT/$\overline{GEN}$ = High to DATAOUT		Max.
LEOUT/$\overline{GEN}$ = High to $\overline{MERROR}$ = Low		Max.
LEOUT/$\overline{GEN}$ = High to $\overline{ERROR}$ = Low		Max.
DATAIN to $\overline{ERROR}$ = Low		**Max.**
CBIN to $\overline{ERROR}$ = Low		Max.
LEIN = High to $\overline{ERROR}$ = Low		Max.
(Low = Error)		
DATAIN to $\overline{MERROR}$ = Low		Max.
CBIN to $\overline{MERROR}$ = Low		Max.
LEIN = High to $\overline{MERROR}$ = Low		Max.
(Low = Error)		
DATAIN	to SCOUT	Max.
CBIN	to SCOUT	Max.
$\overline{OE}$SC = High to SCOUT Disabled		Min.
$\overline{OE}$SC = High to SCOUT Disabled		Max.
$\overline{OE}$SC = Low to SCOUT Enabled		Min.
$\overline{OE}$SC = Low to SCOUT Enabled		Max.
(Syndrome Bits Come Out)		

NOTES:
1. **BOLD** indicates critical parameters.
* Assumes "CBIN" and/or "DATAIN" are valid at least 4ns before "LEIN" goes high.

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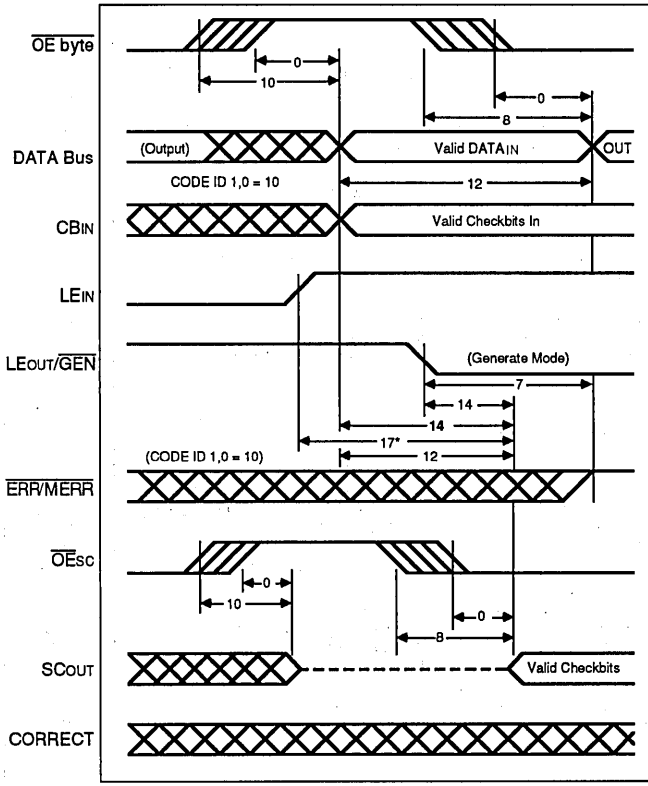
GENERATE MODE (FROM DETECT OR CORRECTION MODE)

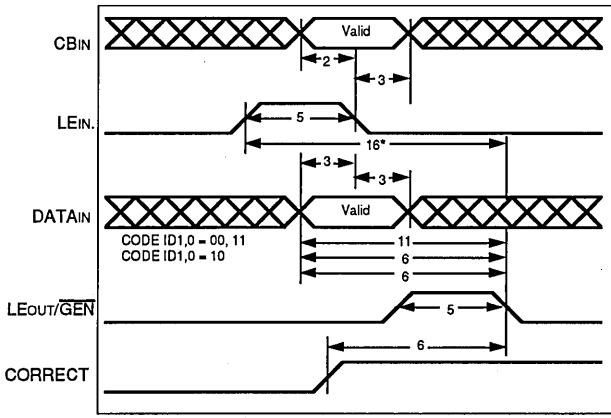


Propagation Delay From	To	Min./Max.
$\overline{OE}$ byte	= High to DATAOUT Disabled	Min.
$\overline{OE}$ byte	= High to DATAOUT Disabled	Max.
$\overline{OE}$ byte	= Low to DATAOUT Enabled	Min.
OE byte	= Low to DATAOUT Enabled	Max.
CBIN	to DATAOUT	Max.
LEOUT/$\overline{GENERATE}$	= Low to $\overline{ERROR}$ = High	Max.
LEOUT/$\overline{GENERATE}$	= Low to SCOUT	Max.
DATAIN	**to SCOUT**	**Max.**
*LEIN	= High to SCOUT*	Max.
CBIN	to SCOUT (Forced High)	Max.
$\overline{OE}$SC	= High to SCOUT Disabled	Min.
$\overline{OE}$SC	= High to SCOUT Disabled	Max.
$\overline{OE}$SC	= Low to SCOUT Enabled	Min.
$\overline{OE}$SC	= Low to SCOUT Enabled (Check Bits Exit)	Max.
CORRECT	(Don't Care)	

NOTES:
1. **BOLD** indicates critical parameters.
2. Valiid "DATA" and valid CBIN" are shown to occur simultaneously, since both buses are latched and opened by the "LEIN" input.
* Assumes DATA bus becomes input 4ns before LEIN goes high.

2584 drw 09

SET-UP AND HOLD TIMES AND MINIMUM PULSE WIDTHS



Set-up/Hold Time Of	With Respect To	Min./Max.
CBIN	Set-up to LEIN = Low	Min.
CBIN	Hold to LEIN = Low	Min.
LEIN	width	Min.
*LEIN = High	to LEOUT/GEN = Low*	Min.
DATA	Set-up to LEIN = Low	Min.
DATA	Hold to LEIN = Low	Min.
CBIN	Set-up to LEOUT/GEN = Low	Min.
CBIN	Set-up to LEOUT/GEN = Low	Min.
DATA	Set-up to LEOUT/GEN = Low	Min.
LEOUT/GENERATE	Width	Min.
CORRECT	Set-up to LEOUT/GEN = Low	Min.

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NOTES:
1. **BOLD** indicates critical parameters.
* Enable to enable timing requirement to ensure that the last DATA word applied to "DATAIN" is made available as DATAOUT"; assumes that "DATAIN" is valid at least 4ns before "LEIN" goes high.

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INPUT/OUTPUT INTERFACE CIRCUIT

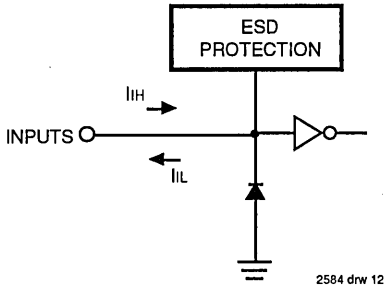


Figure 5. Input Structure (All Inputs)

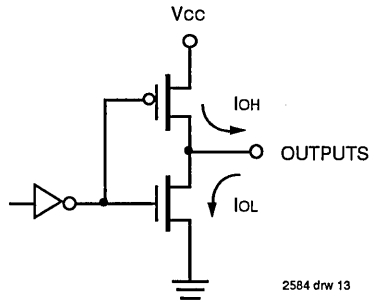
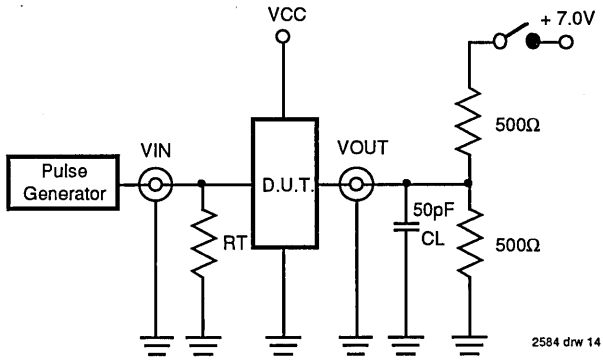


Figure 6. Out put Structure

TEST LOAD CIRCUIT



DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance
R_L = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

Figure 7.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 7

2584 tbl 69

Test	Switch
Disable Low Enable Low	Closed
All other Tests	Open

2584 tbl 68

Integrated Device Technology, Inc.

32-BIT FLOW-THRU ERROR DETECTION AND CORRECTION UNIT

PRELIMINARY
IDT49C465
IDT49C465A

FEATURES

- 32-bit wide Flow-thruEDC™ unit, cascadable to 64 bits
- Single-chip 64-bit Generate Mode
- Separate system and memory buses
- On-chip pipeline latch with external control
- Supports bi-directional and common I/O memories
- Corrects all single-bit errors
- Detects all double-bit errors, some multiple-bit errors
- Error Detection Time — 12ns
- Error Correction Time — 14ns
- On chip diagnostic registers.
- Parity generation and checking on system data bus
- Low power CMOS — 100mA typical at 20MHz
- 144-pin PGA and PQFP packages
- Military product compliant to MIL-STD 883, Class B

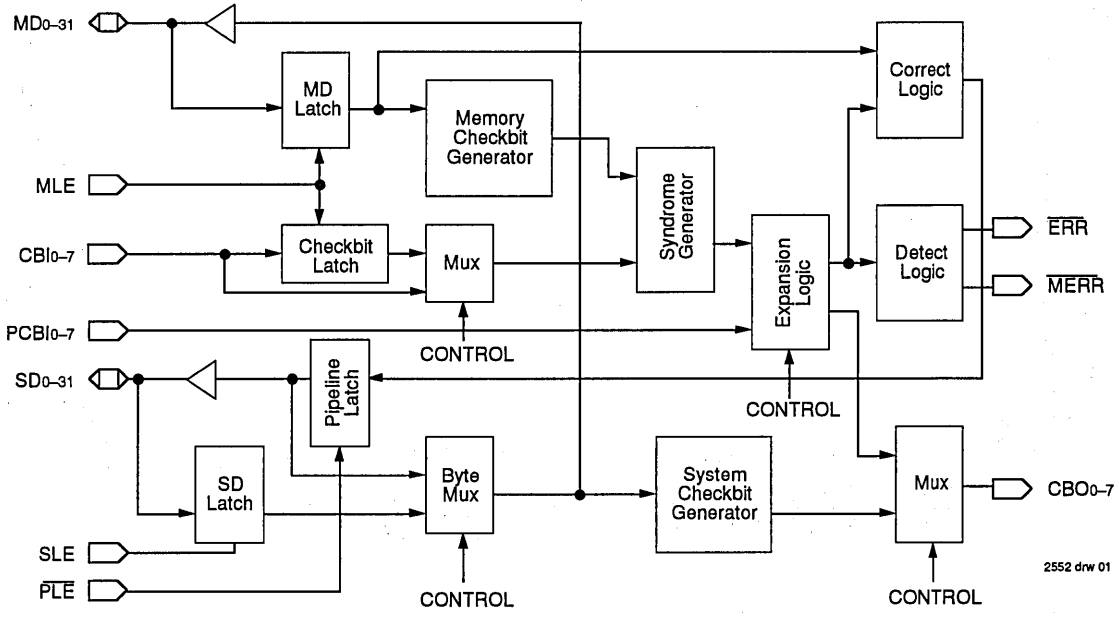
DESCRIPTION

The IDT49C465/A is a 32-bit, two-data bus, Flow-thruEDC unit. The chip provides single-error correction and two and three bit error detection of both hard and soft memory errors. It can be expanded to 64-bit widths by cascading 2 units, without the need for additional external logic. The Flow-thruEDC has been optimized for speed and simplicity of control.

The EDC unit has been designed to be used in either of two configurations in an error correcting memory system. The bi-directional configuration is most appropriate for systems using bi-directional memory buses. A second system configuration utilizes external octal buffers and is well suited for systems using memory with separate I/O buses.

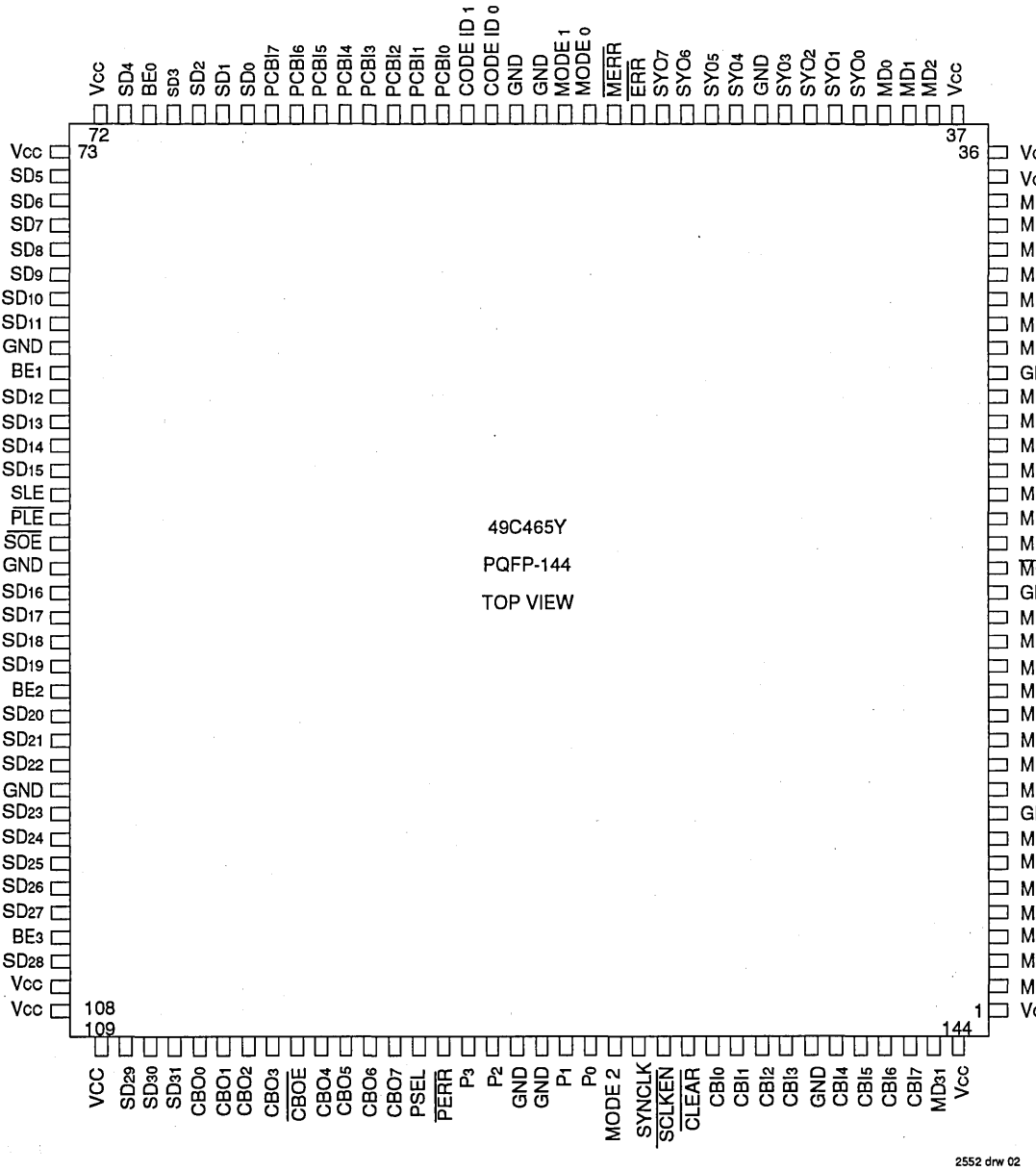
The IDT49C465/A supports partial word writes, pipelining and error diagnostics. It also provides parity protection for data on the system side.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



Flow-thruEDC is a trademark of Integrated Device Technology Inc.

PIN CONFIGURATION



2552 drw 02

PQFP
TOP VIEW

PIN CONFIGURATION

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R
15	Vcc	SD 2	PCBI 6	PCBI 5	PCBI 3	CODE ID 1	CODE ID 0	MODE 1	$\overline{\text{MERR}}$	$\overline{\text{ERR}}$	SYO 5	SYO 3	SYO 1	MD 1	Vcc
14	SD 6	SD 4	SD 1	PCBI 7	PCBI 4	PCBI 1	PCBI 0	MODE 0	SYO 6	SYO 4	SYO 2	MD 0	MD 2	Vcc	MD 5
13	SD 9	SD 5	BE 0	SD 3	SD 0	PCBI 2	GND	GND	SYO 7	GND	SYO 0	Vcc	MD 3	MD 6	MD 9
12	SD 11	SD 7	Vcc										MD 4	MD 8	GND
11	SD 12	SD 10	SD 8										MD 7	MD 10	MD 11
10	SD 15	BE 1	GND										MD 12	MD 13	MD 15
9	SLE	SD 13	SD 14										$\overline{\text{MOE}}$	MD 14	MLE
8	$\overline{\text{SOE}}$	$\overline{\text{PLE}}$	GND					G144-2					GND	MD 17	MD 16
7	SD 17	SD 19	SD 16										MD 20	MD 21	MD 18
6	SD 18	BE 2	SD 20										GND	MD 23	MD 19
5	SD 21	SD 22	SD 25										MD 27	MD 25	MD 22
4	GND	SD 24	BE 3	NC*									Vcc	MD 28	MD 24
3	SD 23	SD 26	SD 28	Vcc	CB0 0	$\overline{\text{CBOE}}$	CB0 7	GND	GND	$\overline{\text{SCLK}}$ $\overline{\text{EN}}$	GND	CB1 6	CB1 7	MD 30	MD 26
2	SD 27	Vcc	SD 29	SD 31	CB0 2	CB0 4	CB0 6	P3	MODE 2	SYN-CLK	CB1 0	CB1 3	CB1 4	MD 31	MD 29
1	Vcc	SD 30	CB0 1	CB0 3	CB0 5	PSEL	$\overline{\text{PERR}}$	P2	P1	P0	$\overline{\text{CLEAR}}$	CB1 1	CB1 2	CB1 5	Vcc

*Tied to Vcc internally

PGA (CAVITY UP)
TOP VIEW

2552 drw 03

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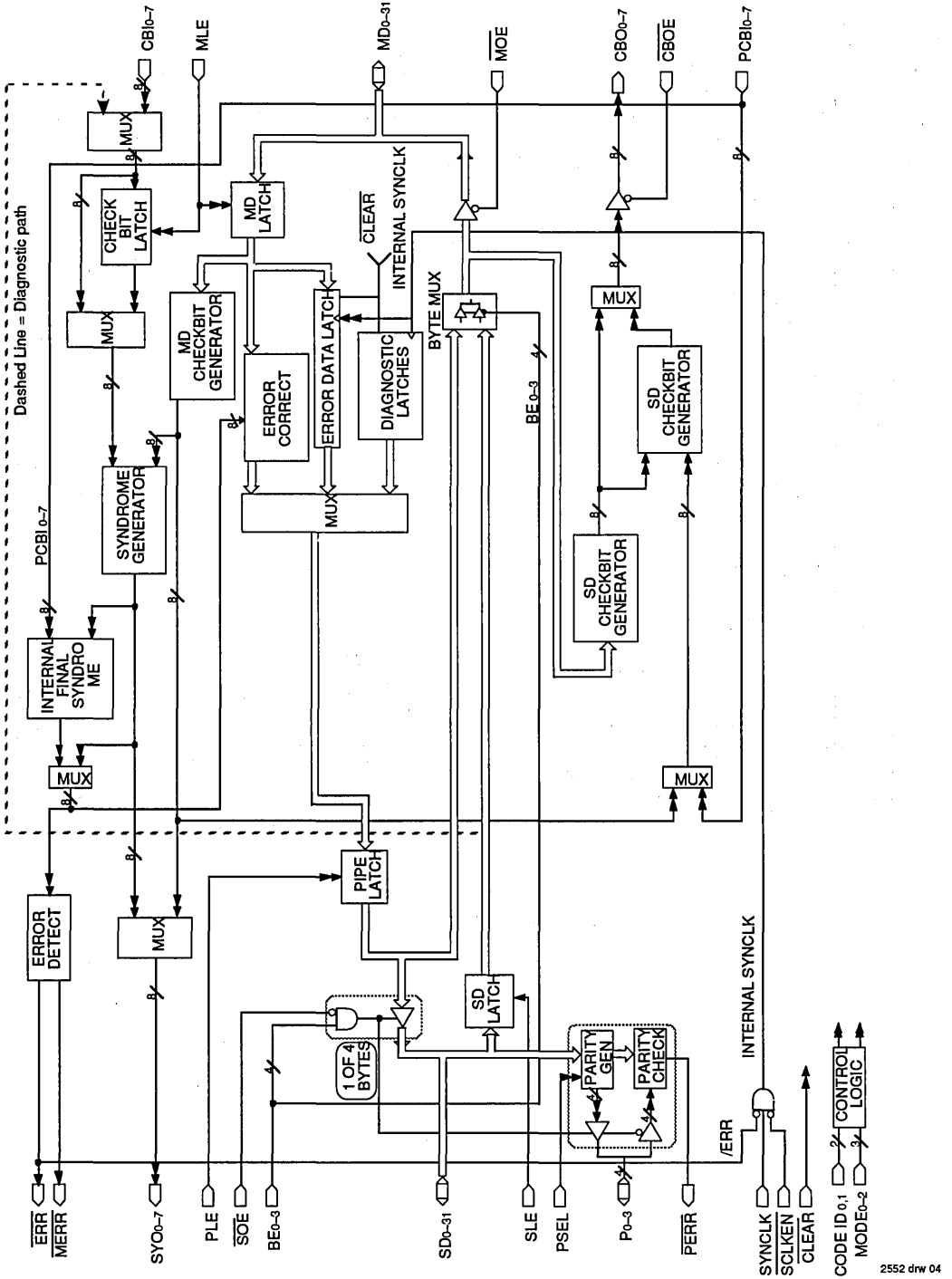
DETAILED FUNCTIONAL BLOCK DIAGRAM



SYSTEM CONFIGURATIONS

The IDT49C465 EDC unit can be used in various configurations in an EDC system. The basic configurations are shown below.

Figure 1 illustrates a bi-directional configuration, which is most appropriate for systems using bi-directional memory buses. It is the simplest configuration to understand and use. During a correction cycle, the corrected data word can be simultaneously output on both the system bus and memory bus. Logically, no other parts are required for the correction function. During partial-word-write operations, the new bytes are internally combined with the corrected old bytes for checkbit generation and writing to memory.

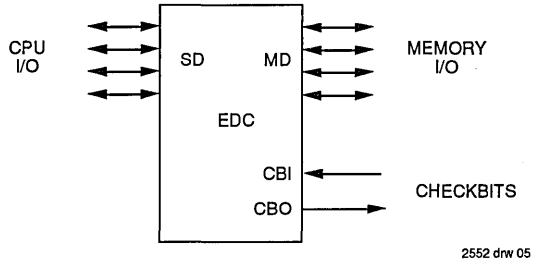


Figure 1. Common I/O Configuration

Figure 2 illustrates a separate I/O configuration. This is appropriate for systems using separate I/O memory buses. This configuration allows separate input and output memory buses to be used. Corrected data is output on the SD outputs for the system and for re-write to memory. Partial word-write bytes are combined externally for writing and checkbit generation.

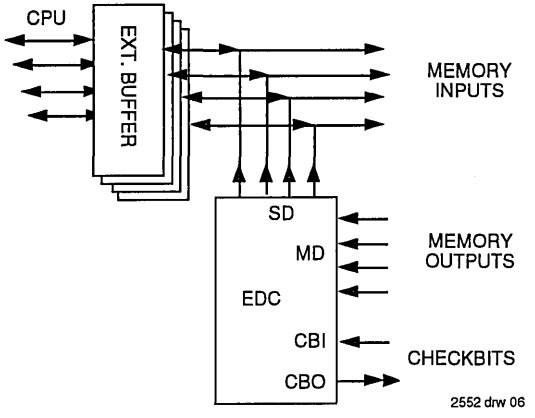


Figure 2. Separate I/O Configuration

Figure 3 illustrates a third configuration which utilizes external buffers and is also well suited for systems using memory with separate I/O buses. Since data from memory does not need to pass through the part on every cycle, the EDC system may operate in "bus-watch" mode. As in the separate I/O configuration, corrected data is output on the SD outputs.

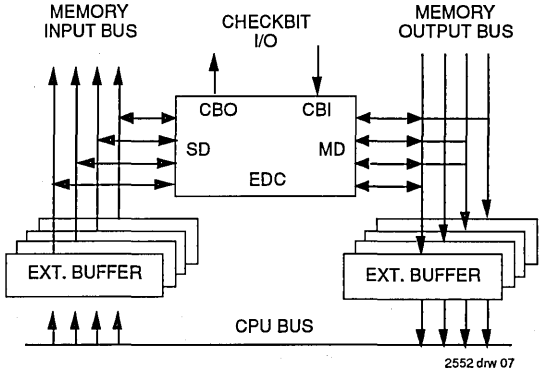


Figure 3. Bypassed Separate I/O Configuration

Figure 4 illustrates the single-chip generate-only mode for very fast 64-bit checkbit generation in systems that use separate checkbit-generate and detect-correct units. If this is not desired, 64-bit checkbit generation and correction can be done with just 2 EDC units. 64-bit correction is also straightforward, fast and requires no extra hardware for the expansion.

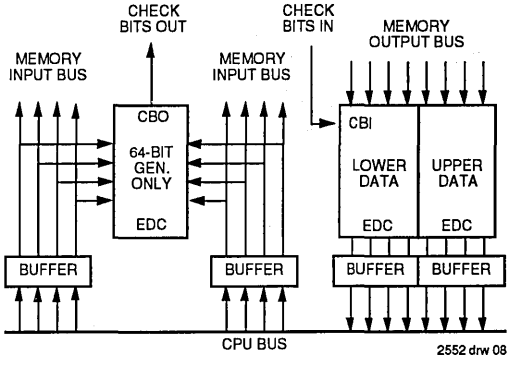


Figure 4. Separate Generate/Correction Units with 64-Bit Checkbit Generation

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FUNCTIONAL DESCRIPTION

The error detection/correction codes consist of a modified Hamming code; it is identical to that used in the IDT49C460.

32-BIT MODE (CODE ID 1,0=00)

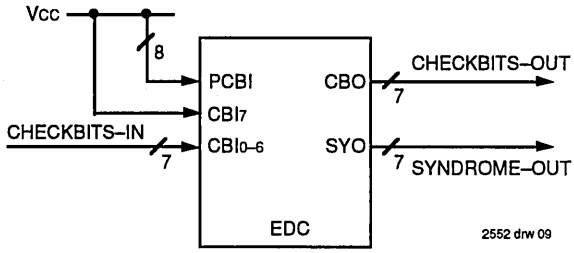

Figure 5. 32-Bit Mode

64-BIT MODE (CODE ID 1,0=10 & 11)

The expansion bus topology is shown in Figure 6. This topology allows the syndrome bits used by the correction logic to be generated simultaneously in both parts used in the expansion. During a 64-bit detection or correction operation, "Partial-Checkbit" data and "Partial-Syndrome" data is simultaneously exchanged between the two EDC units in opposite directions on dedicated expansion buses. This results in very short 64-bit detection and correction times.

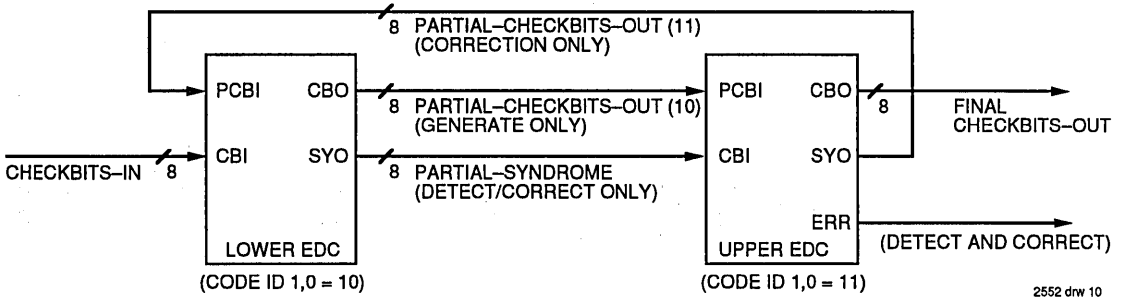

Figure 6. 64-Bit Mode — 2 Cascaded IDT49C465 Devices

64-BIT GENERATE-ONLY MODE (CODE ID 1,0=01)

If the Identity pins CODE ID 1,0 = 01, a single EDC is placed in the 64-bit "Generate-only" mode. In this mode, the lower 32 bits of the 64-bit data word enter the device on the SD0-31 inputs and the upper 32-bits of the 64 bit data word enter the device on the MD0-31 inputs. This provides the device with the full 64-bit word from memory. The resultant generated checkbits are output on the CBO0-7 outputs. The generate time is less than that resulting from using a 2-chip cascade.

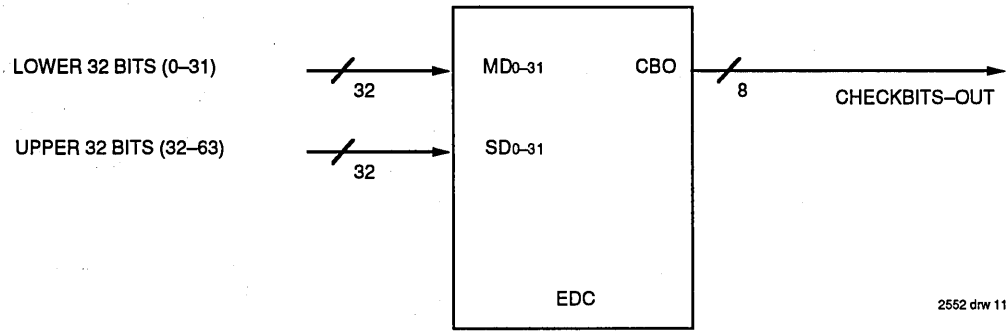

Figure 7. 64-Bit "Generate-Only" Mode (Single Chip)

PIN DESCRIPTIONS

Symbol	I/O		Name and Function
I/O Buses and Controls			
SD_{0-7} SD_{8-15} SD_{16-23} SD_{24-31}	I/O		**System Data Bus**: Data from MD_{0-31} appears at these pins corrected if MODE 2-0 = x11, or uncorrected in the other modes. The BE_n inputs must be high and the $\overline{SOE}$ pin must be low to enable the SD output buffers during a read cycle. (Also, see diagnostic section.) **Separate I/O memory systems:** In a write or partial-write cycle, the byte not-to-be-modified is output on SD_n to n+7 for re-writing to memory, if BE_n is high and $\overline{SOE}$ is low. The new bytes to be written to memory are input on the SD_n pins, for writing checkbits to memory, if BE_n is low. **Bi-directional memory systems:** In a write or partial-write cycle, the byte not-to-be-modified is re-directed to the MD I/O pins, if BE_n is high, for checkbit generation and rewriting to memory via the MD I/O pins. $\overline{SOE}$ must be high to avoid enabling the output drivers to the system bus in this mode. The new bytes to be written are input on the SD_n pins for checkbit generation and writing to memory. BE_n must be low to direct input data from the System Data bus to the MD I/O pins for checkbit generation and writing to the checkbit memory.
SLE	I		**System Latch Enable**: SLE is an input used to latch data at the SD inputs. The latch is transparent when SLE is high; the data is latched when SLE is low.
$\overline{PLE}$	I		**Pipeline Latch Enable**: $\overline{PLE}$ is an input which controls a pipeline latch, which controls data to be output on the SD bus and the MD bus during byte merges. Use of this latch is optional. The latch is transparent when $\overline{PLE}$ is low; the data is latched when $\overline{PLE}$ is high.
$\overline{SOE}$	I		**System Output Enable**: When low, enables System output drivers and Parity output drivers if corresponding Byte Enable inputs are high.
BE_{0-3}	I		**Byte Enables**: In systems using separate I/O memory buses, BE_n is used to enable the SD and Parity outputs for byte n. The BE_n pins also control the "Byte mux". When BE_n is high, the corrected or uncorrected data from the Memory Data latch is directed to the MD I/O pins and used for checkbit generation for byte n. This is used in partial-word-write operations or during correction cycles. When BE_n is low, the data from the System Data latch is directed to the MD I/O pins and used for checkbit generation for byte n. BE_0 controls SD_{0-7} BE_2 controls SD_{16-23} BE_1 controls SD_{8-15} BE_3 controls SD_{24-31}
MD_{0-31}	I/O		**Memory Data Bus:** These I/O pins accept a 32-bit data word from main memory for error detection and/or correction. They also output corrected old data or new data to be written to main memory when the EDC unit is used in a bi-directional configuration.
MLE	I		**Memory Latch Enable**: MLE is used to latch data from the MD inputs and checkbits from the CBI inputs. The latch is transparent when MLE is high; data is latched when MLE is low. When identified as the upper slice in a 64-bit cascade, the checkbit latch is bypassed.
$\overline{MOE}$	I		**Memory Output Enable**: $\overline{MOE}$ enables Memory Data Bus output drivers when low.
P_{0-3}	I/O		**Parity I/O**: The parity I/O pins for Bytes 0 to 3. These pins output the parity of their respective bytes when that byte is being output on the SD bus. These pins also serve as parity inputs and are used in generating the Parity ERRor ($\overline{PERR}$) signal under certain conditions (see Byte Enable definition). The parity is odd or even depending on the state of the Parity SELect pin (PSEL).
PSEL	I		**Parity SELect**: If the Parity SELect pin is low, the parity is even. If the Parity SELect pin is high, the parity is odd.
Inputs			
CBI_{0-7}	I		**CheckBits-In** (00) CheckBits-In-1 (10) Partial-Syndrome-In (11): In a single EDC system or in the lower slice of a cascaded EDC system, these inputs accept the checkbits from the checkbit memory. In the upper slice in a cascaded EDC system, these inputs accept the "Partial-Syndrome" from the lower slice (Detect/Correct path).
$PCBI_{0-7}$	I		**Partial-CheckBits-In** (10) Partial-CheckBits-In (11): In a single EDC system, these inputs are unused but should not be allowed to float. In a cascaded EDC system, the "Partial-Checkbits" used by the lower slice are accepted by these inputs (Correction path only). In the upper slice of a cascaded EDC system, "Partial-Checkbits" generated by the lower slice are accepted by these inputs (Generate path).
$CODE\ ID_{1,0}$	I		**CODE IDentity**: Inputs which identify the slice position/ functional mode of the IDT49C465. (00) Single 32-bit EDC unit (10) Lower slice of a 64-bit cascade (01) 64-bit "Checkbit-generate-only" unit (11) Upper slice of a 64-bit cascade

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PIN DESCRIPTIONS (Con't.)

Symbol	I/O		Name and Function
Inputs (Con't.)			
MODE 2-0	I		**MODE select:** Selects one of four operating modes.
		(x11)	**"Normal" Mode:** Normal EDC operation (Flow-thru correction and generation).
		(x10)	**"Generate-Detect" Mode:** In this mode, error correction is disabled. Error generation and detection are normal.
		(000)	**"Error-Data-Output" Mode:** Allows the uncorrected data captured from an error event by the Error-Data Register to be read by the system for diagnostic purposes. The Error-Data Register is cleared by toggling $\overline{CLEAR}$ low. The Syndrome Register and Error-Data Register record the syndrome and uncorrected data from the first error that occurs after they are reset by the $\overline{CLEAR}$ pin. The Syndrome Register and Error-Data Register are updated when there is a positive edge on SYNCLK, an error condition is indicated ($\overline{ERR}$ = low), and the Error Counter indicates zero. **All-Zero-Data Source:** In Error-Data-Output Mode, clearing the Error-Data Register provides a source of all-zero-data for hardware initialization of memory, if this desired.
		(x01)	**Diagnostic-Output Mode:** In this mode, the contents of the Syndrome Register , Error Counter and Error-Type Register are output on the SD bus. This allows the syndrome bytes for an indicated error to be read by the system for error-logging purposes. The Syndrome Register and the Error-Data Register are updated when there is a positive edge on SYNCLK, an error condition is indicated and the Error Counter indicates zero errors. Thus, the Syndrome Register saves the syndrome that was present when the first error occurred after the Error Counter was cleared. The Syndrome Register and the Error Counter are cleared by toggling $\overline{CLEAR}$ low. The Error Counter lets the system tell if more than one error has occurred since the last time the Syndrome Register or Error-Data Register was read.
		(100)	**Checkbit-Injection Mode:** In the "Checkbit-Injection" Mode, diagnostic checkbits may be input on System Data Bus bits 0-7 (see Diagnostic Features - Detailed Description).
$\overline{CLEAR}$	I		**CLEAR**: When the $\overline{CLEAR}$ pin is taken low, the Error-Data Register, the Syndrome Register, the Error Counter and the Error-Type Register are cleared.
SYNCLK	I		**SYNdrome CLocK**: If $\overline{ERR}$ is low, and the Error Counter indicates zero errors, syndrome bits are clocked into the Syndrome Register and data from the outputs of the Memory Data input latch are clocked into the Error-Data Register on the low-to-high edge of SYNCLK. If $\overline{ERR}$ is low, the Error Counter will increment on the low-to-high edge of SYNCLK, unless the Error Counter indicates fifteen errors.
$\overline{SCLKEN}$	I		**SynCLK ENable**: The $\overline{SCLKEN}$ enables the SYNCLK signal. SYNCLK is ignored if $\overline{SCLKEN}$ is high.
Outputs and Enables			
CBO0-7	O		**CheckBits-Out** (00, 01) Partial-CheckBits-Out (10) Checkbits-Out (11): In a single EDC system, the checkbits are output to the checkbit memory on these outputs. In the lower slice in a cascaded EDC system, the "Partial-checkbits" used by the upper slice are output by these outputs (Generate path only). In the upper slice in a cascade, the "Final-Checkbits" appear at these outputs (Generate path only).
$\overline{CBOE}$	I		**CheckBits Out Enable**: Enables CheckBit Output drivers when low.
SYO0-7	O		**SYndrome-Out** (00) Partial-SYndrome-Out (10) Partial-Checkbits-Out (11): In a 32-bit EDC system, the syndrome bits are output on these pins. In the lower slice in a 64-bit cascaded system, the "Partial-Syndrome" bits appear at these outputs (Detect/ Correct path). In the upper slice in a cascaded EDC system, the "Partial-Checkbits" appear at these outputs (Correct path only). In a 64-bit cascaded system, the "Final-Syndrome" may be accessed in the "Diagnostic-Output" Mode from either the lower or the upper slice since the final syndrome is contained in both.
$\overline{ERR}$	O		**ERROR**: When in "Normal" and "Detect only" modes, a low on this pin indicates that one or more errors have been detected. $\overline{ERR}$ is not gated or latched internally.
$\overline{MERR}$	O		**Multiple ERRor**: When in "Normal" and "Detect only" modes, a low on this pin indicates that two or more errors have been detected. $\overline{MERR}$ is not gated or latched internally.
$\overline{PERR}$	O		**Parity ERRor**: A low on this pin indicates a parity error which has resulted from the active bytes defined by the 4 Byte Enable pins. Parity ERRor ($\overline{PERR}$) is not gated or latched internally (see Byte Enable definition).
Power Supply Pins			
Vcc 1-10	P		+5 Volts
GND1-12	P		Ground

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DIAGNOSTIC DATA FORMAT (SYSTEM BUS)

Latched Data																Data Out (Unlatched)															
Error Type		Re-served		Error Counter				Syndrome bits								Partial Checkbits								Checkbits							
Byte 3								Byte 2								Byte 1								Byte 0							
S	M	-	-	2^3	2^2	2^1	2^0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
31	30			27			24	23							16	15							8	7							0

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DIAGNOSTIC FEATURES — DETAILED DESCRIPTION

Mode 2-0	
x11	**"NORMAL" Mode** In this mode, operation is "Normal" or non-diagnostic.
x10	**"GENERATE-DETECT" Mode** When the EDC unit is in the **"Generate-Detect" Mode**, data is not corrected or altered by the error correction network. (Also referred to as the "Detect-only" Mode.)
000	**"ERROR-DATA-OUTPUT" Mode** In this mode, the 32-bit data from the Error-Data Register is output on the SD bus. **Error Data Register**: The uncorrected data from the Memory Data bus input latch is stored in the Error-Data Register if the error counter contents indicates "0" and there is a positive transition on the SYNCLK input when the $\overline{ERR}$ signal is low. Thus, the Error-Data Register contains memory data corresponding to the first error to occur since the register was cleared. This register is cleared by pulling the $\overline{CLEAR}$ input low. The register is read via the System Data bus by entering the **"Error-Data-Output"** Mode and enabling the System Data bus output drivers. **All-Zero-Data**: The Error-Data Register can be used as an "all-zero-data" data source for memory initialization in systems where the initialization process is to be done entirely by hardware.
x01	**"DIAGNOSTIC-OUTPUT" Mode** In this mode, data from the diagnostic registers, the PCBI bus and the CBI bus is output on the SD bus. **Direct Checkbit Readback**: Internal data paths allow both the "Partial-CheckBit-Input" bus and the data in the "CheckBit-Input" latch to be read directly by the system bus for diagnostic purposes. Both the Checkbit Input Bus and the Partial Checkbit Input Bus are read via the System Data bus by entering the **"Diagnostic-Output" Mode** and enabling the System Data bus output drivers. The checkbits are output on System Data bus bits 0-7; the Partial Checkbits are output on bits 8-15. **Syndrome Register:** After an error has been detected, the syndrome bits generated are clocked into the internal Syndrome Register if the error counter contents indicates "0" and there is a positive transition on the SYNCLK input when the $\overline{ERR}$ signal is low. This register is cleared by pulling the $\overline{CLEAR}$ input low. The register is read via the System Data bus by entering the **"Diagnostic-Output" Mode** and enabling the System Data bus outputs. This data is output on SD bits 16-23. **Error Counter**: The 4-bit on-board error counter is incremented if the error counter contents do not indicate FF HEX, which corresponds to a count of 15, and there is a positive transition on the SYNCLK input when the $\overline{ERR}$ signal is low. This counter is cleared by pulling the $\overline{CLEAR}$ input low. The counter is read via the System Data bus by entering the **"Diagnostic-Output" Mode** and enabling the System Data bus output drivers. This data is output on System Data bus bits 24-27. **Test Register**: These 2 bits are reserved for factory diagnostics only and must not be used by system software. This data is output on System Data bus bits 28-29. **Error-Type Register**: The Error-Type Register, clocked by the SYNCLK input, saves 2 bits which indicate whether a recorded error was a single or a multiple-bit error. This register holds only the first error type to occur after the last Clear operation. This data is output on System Data bus bits 30-31.
100	**Direct Read-Path Checkbit Injection**: In the **"Checkbit-Injection" Mode**, bits 0-7 of the System Data input latch are presented to the inputs of the Checkbit Input latch. If MLE is strobed, the checkbit latch will be loaded with this value in place of the checkbits from memory. By inserting various checkbit values, operation of the correction function of the EDC can be verified "on-board". Except for the "Checkbit-Injection" function, operation in this mode is identical to "Normal" Mode operation.

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OPERATING MODE CHARTS

SLICE IDENTIFICATION

CODE ID 1	CODE ID 0	Slice Definition
0	0	32-bit Flow-Thru EDC
0	1	64-bit GENERATE Only EDC
1	0	64-bit EDC- Lower 32 bits (0-31)
1	1	64-bit EDC- Upper 32 bits (32-63)

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SLICE POSITION CONTROL

CODE ID	Slice Position/ Functional Operation	SOE	SD Bus	MOE	MD Bus	Checkbit Buses: PCBI Bus	CBI Bus	CBO Bus	SYO Bus	P Bus	PERR
1 0	Width =		32		32	8	8	8	8	4	1
0 0	Single 32-bit EDC unit										
	Generate(1)	1	Sys. 0–31	0	Sys. Byte Mux	—	—	CBs out	—	P in	active
	Detect/Correct(2)	0	Pipe. latch	1	MD 0–31	—	CBs in	—	Syn. out	P out	—
0 1	"64-bit Generate-only"	1	Sys. 32–63	1	Sys. 0–31	—	—	CBs out	—	—	—
1 0	Lower word, 64-bit bus										
	Generate(1)	1	Sys. 0–31	0	MD 0–31	—	—	PCBs out	—	P in	active
	Detect/Correct(2)	0	Pipe. latch	1	MD 0–31	U-SYOout	CBs in	—	Par.Synd	P out	—
1 1	Upper word, 64-bit bus										
	Generate(1)	1	Sys. 32–63	0	MD 32–63	L-CBOout	—	F.CBs out	—	P in	active
	Detect/Correct(2)	0	Pipe. latch	1	MD 32–63	—	L-SYOout	—	Par.Cbits	P out	—

NOTES:
1. Checkbits generated from the data in the SD Latch.
2. Corrected data residing in the Pipe Latch.

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FUNCTIONAL MODE CONTROL

MODE 2	MODE 1	MODE 0	Functional Mode of SD Bus	SOE	SD Bus	MOE	MD Bus	Checkbit Buses: PCBI Bus	CBI Bus	CBO Bus	SYO Bus	P Bus	PERR
			Width =		32		32	8	8	8	8	4	1
x	1	1	**"Normal"**										
			Generate	1	CPU Data	0	Pipe. latch	—	—	CB out	—	P in	active
			Correct	0	Pipe. latch	1	RAM Data	—	CB in	—	—	P out	—
x	1	0	**"Generate-Detect"**										
			Generate	1	CPU Data	0	Pipe. latch	—	—	CB out	—	P in	active
			Detect	0	Pipe. latch	1	RAM Data	—	CB in	—	—	P out	—
0	0	0	**"Error-Data-Output"**	0	Err. D. latch	—	—	—	—	—	—	—	—
x	0	1	**"Diagnostic-Output"**	0	CBin latch PCBIin bus Syn. register Err. counter Er. type reg.	—	—	PCBI in	CB in	—	—	—	—
1	0	0	**"Checkbit-Injection"**										
			Generate	1	SDin latch	0	Pipe. latch	—	—	CB out	—	P in	active
			Inject Checkbits	1	SD0–7 in	0	Pipe. latch	—	—	—	—	—	—
			Correct	0	Pipe. latch	1	RAM Data	—	CB in	—	—	P out	—

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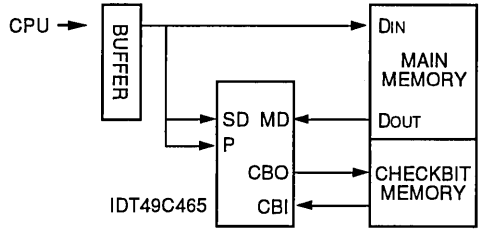
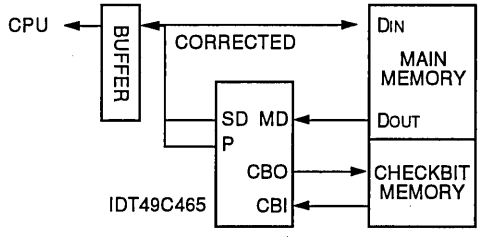
PRIMARY DATA PATH vs. MEMORY CONFIGURATION

SEPARATE I/O MEMORIES:

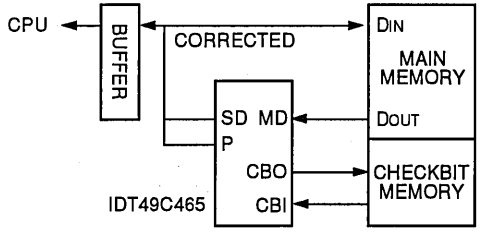
1. Checkbit Generation
Write New Word to Memory



2. Data Correction
Read Memory Word

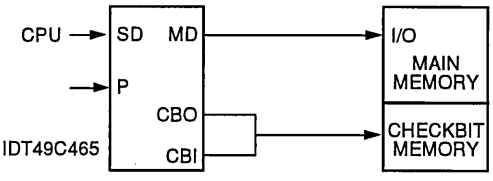


3. Memory Generation
Re-write Corrected Word to Memory

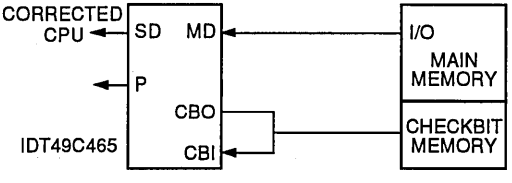


COMMON I/O MEMORIES:

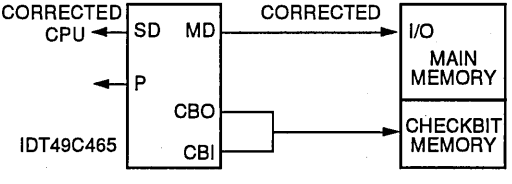
1. Checkbit Generation
Write New Word to Memory



2. Data Correction
Read Memory Word



3. Memory Generation
Re-write Corrected Word to Memory



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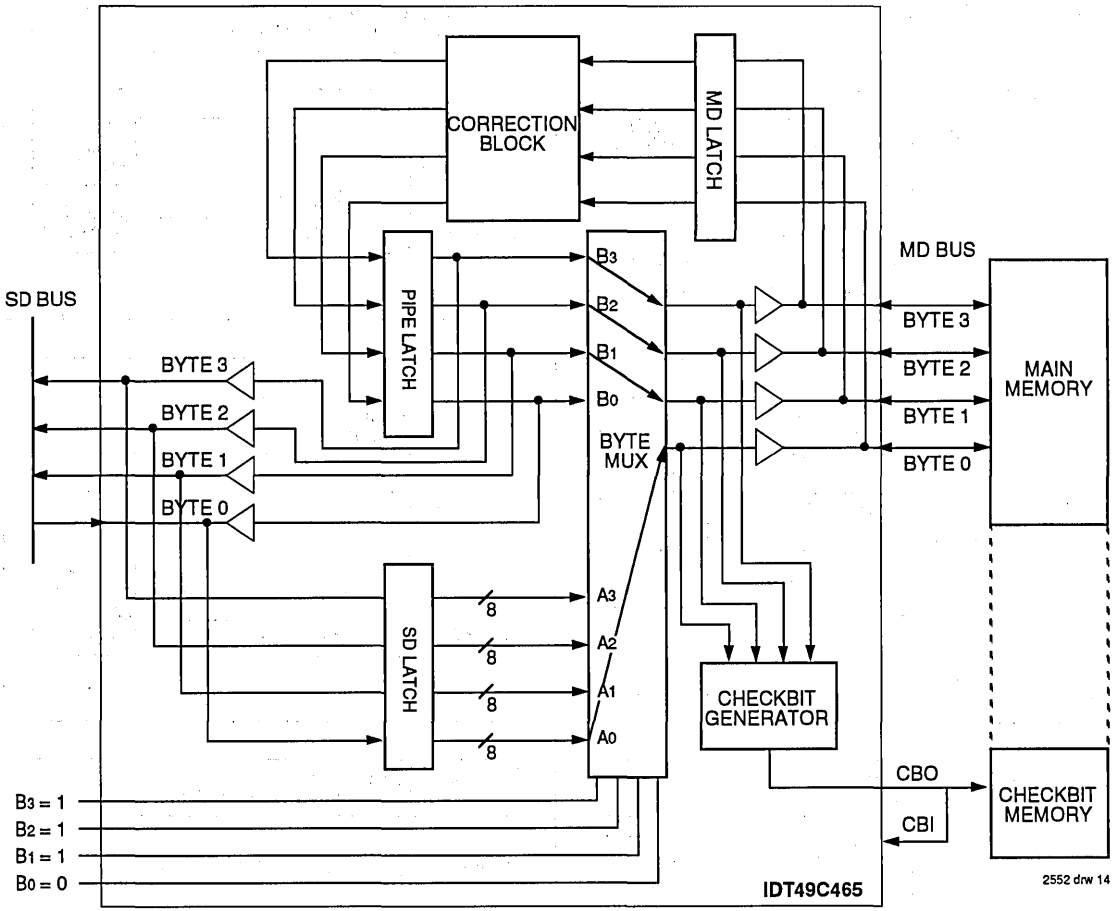
PARTIAL-WORD-WRITE OPERATIONS

FOR COMMON I/O MEMORIES:



In order to perform a partial-word-write operation, the complete word in question must be read from memory. This must be done in order to correct any error which may have occurred in the old word. Once the complete, corrected word is available, with all the bytes verified, the new word may be assembled in the byte mux and the new checkbits generated.

The example shown above illustrates the case of combining 3 bytes from an old word with a new lower order byte to form a new word. The new word, along with the new checkbits, may now be written to memory.

In the separate I/O memory configuration, the situation is similar except that the new word is output on the SD Bus instead of the MD Bus (refer to previous page).

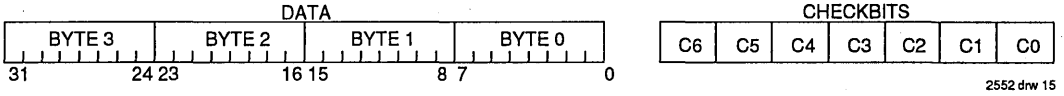
32-BIT DATA WORD CONFIGURATION

A single IDT49C465 EDC unit, connected as shown below, provides all the logic needed for single-bit error correction, and double-bit error detection, of a 32-bit data field. The identification code (00) indicates 7 checkbits are required. The CBI7 pin should be tied high.

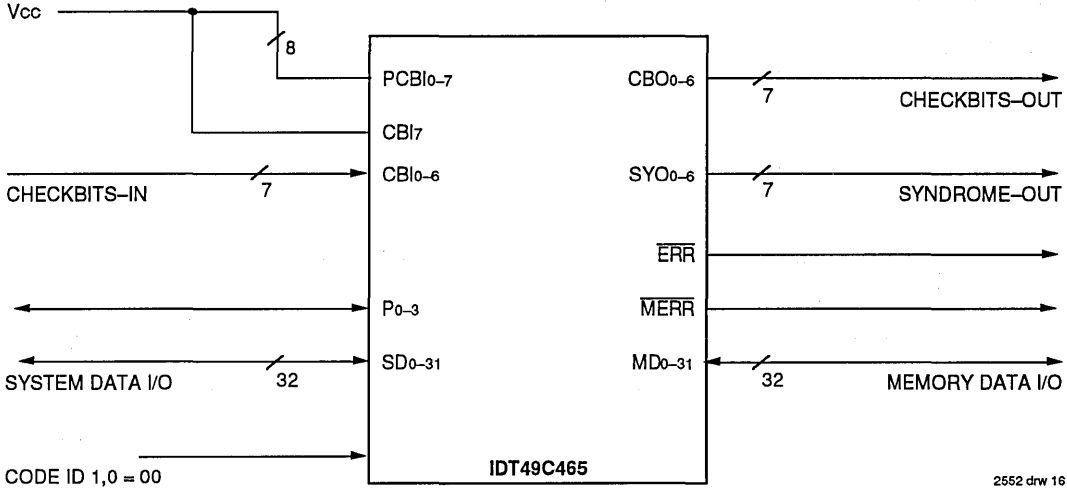
The 39-bit data format for four bytes of data and 7 checkbits is indicated below.

Syndrome bits are generated by an exclusive-OR of the generated checkbits with the checkbits read from memory. For example, Sn is the XOR of checkbits from those read with those generated. During Data Correction, the syndrome bits are used to complement (correct) single-bit errors in the data bits.

32-BIT DATA FORMAT



32-BIT HARDWARE CONFIGURATION



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64-BIT DATA WORD CONFIGURATION

Two IDT49C465 EDC units, connected as shown below, provide all the logic needed for single-bit error correction, and double-bit error detection, of a 64-bit data field. The "Slice Identification" Table gives the CODE ID1,0 values needed for distinguishing the upper 32 bits from the lower 32 bits. Final generated checkbits, $\overline{ERR}$ and $\overline{MERR}$ (indicates multiple errors) signals come from the upper slice, the IC with CODE ID1,0=11. Control signals not shown are connected to both units in parallel.

Data-In bits 0 through 31 are connected to the same numbered inputs of the EDC with CODE ID1,0=10, while Data-In bits 32 through 63 are connected to data inputs 0 to 31, respectively, for the EDC unit with CODE ID1,0=11.

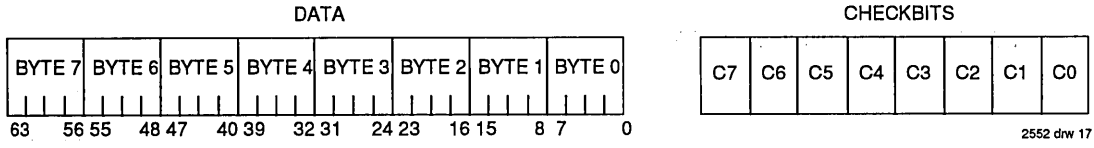
The 72-bit data format of data and checkbits is indicated below.

Correction of single-bit errors in the 64-bit configuration requires a simultaneous exchange of partial checkbits and partial syndrome bits between the upper and lower units.

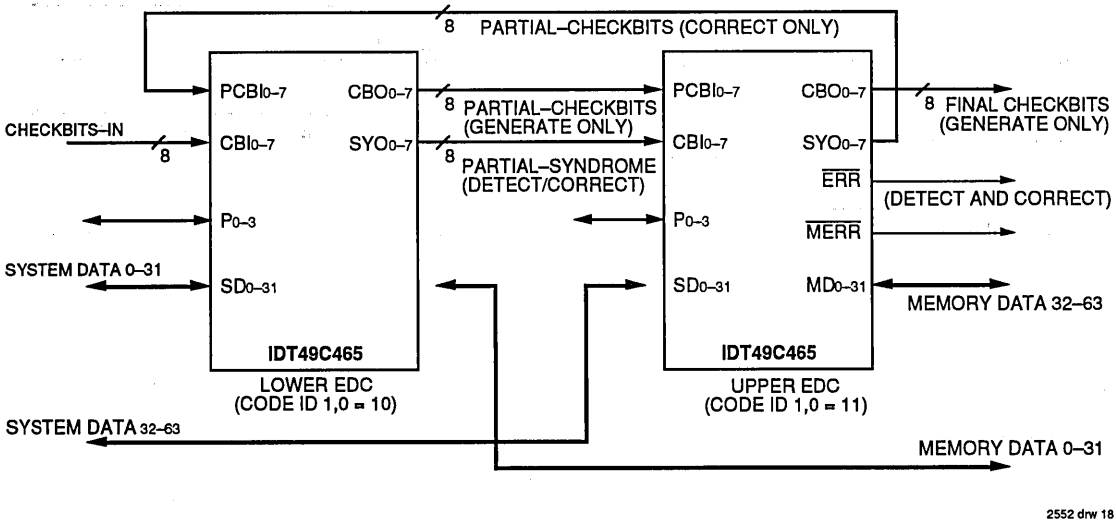
Syndrome bits are generated by an exclusive-OR of the generated checkbits with the checkbits read from memory. For example, Sn is the XOR of checkbits read and checkbits generated. During data correction, the syndrome bits are used to complement (correct) single-bit errors in the data bits. For double or multiple-bit error detection, the data available as output by the Pipeline Latch is not defined.

Critical AC performance data is provided in the Table "Key AC Calculations", which illustrates the delays that are critical to 64-bit cascaded performance. As indicated, a summation of propagation delays is required when cascading these units.

64-BIT DATA FORMAT



64-BIT HARDWARE CONFIGURATION



DEFINITIONS OF TERMS:

$D_0 - D_{31}$ = System Data and/or Memory Data Inputs
$CBI_0 - CBI_7$ = Checkbit Inputs
$PCBI_0 - PCBI_7$ = Partial Checkbit Inputs
$FS_0 - FS_7$ = Final Internal Syndrome bits

FUNCTIONAL EQUATIONS:

The equations below describe the terms used in the IDT49C465 to determine the values of the partial checkbits, checkbits, partial syndromes and final internal syndromes. NOTE: All "⊕" symbols below represent the "EXCLUSIVE-OR" function.

$PA = D_0 \oplus D_1 \oplus D_2 \oplus D_4 \oplus D_6 \oplus D_8 \oplus D_{10} \oplus D_{12} \oplus D_{16} \oplus D_{17} \oplus D_{18} \oplus D_{20} \oplus D_{22} \oplus D_{24} \oplus D_{26} \oplus D_{28}$

$PB = D_0 \oplus D_3 \oplus D_4 \oplus D_7 \oplus D_9 \oplus D_{10} \oplus D_{13} \oplus D_{15} \oplus D_{16} \oplus D_{19} \oplus D_{20} \oplus D_{23} \oplus D_{25} \oplus D_{26} \oplus D_{29} \oplus D_{31}$

$PC = D_0 \oplus D_1 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{16} \oplus D_{17} \oplus D_{21} \oplus D_{22} \oplus D_{23} \oplus D_{27} \oplus D_{28} \oplus D_{29}$

$PD = D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{14} \oplus D_{15} \oplus D_{18} \oplus D_{19} \oplus D_{20} \oplus D_{21} \oplus D_{22} \oplus D_{23} \oplus D_{30} \oplus D_{31}$

$PE = D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14} \oplus D_{15} \oplus D_{24} \oplus D_{25} \oplus D_{26} \oplus D_{27} \oplus D_{28} \oplus D_{29} \oplus D_{30} \oplus D_{31}$

$PF = D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{24} \oplus D_{25} \oplus D_{26} \oplus D_{27} \oplus D_{28} \oplus D_{29} \oplus D_{30} \oplus D_{31}$

$PG = D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14} \oplus D_{15} \oplus D_{16} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{20} \oplus D_{21} \oplus D_{22} \oplus D_{23}$

$PH_0 = D_0 \oplus D_4 \oplus D_6 \oplus D_7 \oplus D_8 \oplus D_9 \oplus D_{11} \oplus D_{14} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{21} \oplus D_{26} \oplus D_{28} \oplus D_{29} \oplus D_{31}$

$PH_1 = D_1 \oplus D_2 \oplus D_3 \oplus D_5 \oplus D_8 \oplus D_9 \oplus D_{11} \oplus D_{14} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{21} \oplus D_{24} \oplus D_{25} \oplus D_{27} \oplus D_{30}$

$PH_2 = D_0 \oplus D_4 \oplus D_6 \oplus D_7 \oplus D_{10} \oplus D_{12} \oplus D_{13} \oplus D_{15} \oplus D_{16} \oplus D_{20} \oplus D_{22} \oplus D_{23} \oplus D_{26} \oplus D_{28} \oplus D_{29} \oplus D_{31}$

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.

8

DETAILED DESCRIPTION — CHECKBIT AND SYNDROME GENERATION vs. CODE ID

LOGIC EQUATIONS FOR THE CBO OUTPUTS

Checkbit Generation	CODE ID 1,0		
	00	10	11
	Final Chkbits	Partial Checkbits	Final Checkbits
CBO_0	PH_0	PH_1	$PH_2 \oplus PCBI_0$
CBO_1	PA	PA	$PA \oplus PCBI_1$
CBO_2	$\overline{PB}$	$\overline{PB}$	$PB \oplus PCBI_2$
CBO_3	$\overline{PC}$	$\overline{PC}$	$PC \oplus PCBI_3$
CBO_4	PD	PD	$PD \oplus PCBI_4$
CBO_5	PE	PE	$PE \oplus PCBI_5$
CBO_6	PF	PF	$PF \oplus PCBI_6$
CBO_7	—	PF	$PG \oplus PCBI_7$

2552 tbl 07

LOGIC EQUATIONS FOR THE SYO OUTPUTS

Checkbit/ Syndrome Generation	CODE ID 1,0		
	00	10	11
	Final Syndrome	Partial Syndrome	Partial Checkbits
SYO0	$PH0 \oplus CBI0$	$PH1 \oplus CBI0$	PH2
SYO1	$PA \oplus CBI1$	$PA \oplus CBI1$	PA
SYO2	$\overline{PB} \oplus CBI2$	$\overline{PB} \oplus CBI2$	PB
SYO3	$\overline{PC} \oplus CBI3$	$\overline{PC} \oplus CBI3$	PC
SYO4	$PD \oplus CBI4$	$PD \oplus CBI4$	PD
SYO5	$PE \oplus CBI5$	$PE \oplus CBI5$	PE
SYO6	$PF \oplus CBI6$	$PF \oplus CBI6$	PF
SYO7	—	$PF \oplus CBI7$	PG

2552 tbl 08

LOGIC EQUATIONS FOR THE FINAL SYNDROME (FSn)

Final Syndrome Generation	CODE ID 1,0	
	00	10, 11
	Final Syndrome	Final Internal Syndrome
FS_0	$PH_0 \oplus CBI_0$	PH_1 (L) $\oplus$ PH_2 (U) $\oplus$ CBI_0
FS_1	$PA \oplus CBI_1$	PA (L) $\oplus$ PA (U) $\oplus$ CBI_1
FS_2	$\overline{PB} \oplus CBI_2$	PB (L) $\oplus$ PB (U) $\oplus$ CBI_2
FS_3	$\overline{PC} \oplus CBI_3$	PC (L) $\oplus$ PC (U) $\oplus$ CBI_3
FS_4	$PD \oplus CBI_4$	PD (L)$\oplus$ PD (U) $\oplus$ CBI_4
FS_5	$PE \oplus CBI_5$	PE (L) $\oplus$ PE (U) $\oplus$ CBI_5
FS_6	$PF \oplus CBI_6$	PF (L) $\oplus$ PF (U) $\oplus$ CBI_6
FS_7	—	PF (L) $\oplus$ PG (U)$\oplus$ CBI_7

2552 tbl 09

32-BIT SYNDROME DECODE TO BIT-IN-ERROR (1)

					HEX	0	1	2	3	4	5	6	7
					S6	0	0	0	0	1	1	1	1
				Syndrome	S5	0	0	1	1	0	0	1	1
				Bits	S4	0	1	0	1	0	1	0	1
HEX	S3	S2	S1	S0									
0	0	0	0	0		*	C4	C5	T	C6	T	T	30
1	0	0	0	1		C0	T	T	14	T	M	M	T
2	0	0	1	0		C1	T	T	M	T	2	24	T
3	0	0	1	1		T	18	8	T	M	T	T	M
4	0	1	0	0		C2	T	T	15	T	3	25	T
5	0	1	0	1		T	19	9	T	M	T	T	31
6	0	1	1	0		T	20	10	T	M	T	T	M
7	0	1	1	1		M	T	T	M	T	4	26	T
8	1	0	0	0		C3	T	T	M	T	5	27	T
9	1	0	0	1		T	21	11	T	M	T	T	M
A	1	0	1	0		T	22	12	T	1	T	T	M
B	1	0	1	1		17	T	T	M	T	6	28	T
C	1	1	0	0		T	23	13	T	M	T	T	M
D	1	1	0	1		M	T	T	M	T	7	29	T
E	1	1	1	0		16	T	T	M	T	M	M	T
F	1	1	1	1		T	M	M	T	0	T	T	M

NOTES:

2552 tbl 12

1. The table indicates the decoding of the seven syndrome bits to identify the bit-in-error for a single-bit error, or whether a double or triple-bit error was detected. The all-zero case indicates no error detected.
   * = No errors detected
   # = The number of the single bit-in-error
   T = Two errors detected
   M = Three or more errors detected

DETAILED DESCRIPTION — 32-BIT CONFIGURATION

32-BIT MODIFIED HAMMING CODE — CHECKBIT ENCODING CHART[1]

Generated Checkbits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	Even (XOR)	X				X		X	X	X	X		X			X	
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)	X	X	X	X	X	X	X	X								

2552 tbl 10

Generated Checkbits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CB0	Even (XOR)		X	X	X		X					X		X	X		X
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)									X	X	X	X	X	X	X	X

NOTE: 2552 tbl 11

1. The table indicates the data bits participating in the checkbit generation. For example, checkbit C0 is the Exclusive-OR function of the 16 data input bits marked with an X.

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DETAILED DESCRIPTION — 64-BIT CONFIGURATION

64-BIT MODIFIED HAMMING CODE - CHECKBIT ENCODING CHART[1, 2]

Generated Checkbits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	Even (XOR)		X	X	X		X			X	X		X			X	
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)	X	X	X	X	X	X	X	X								
CB7	Even (XOR)	X	X	X	X	X	X	X	X								

2552 tbl 13

Generated Checkbits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CB0	Even (XOR)		X	X	X		X			X	X		X			X	
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)									X	X	X	X	X	X	X	X
CB7	Even (XOR)									X	X	X	X	X	X	X	X

2552 tbl 14

Generated Checkbits	Parity	Participating Data Bits															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CB0	Even (XOR)	X				X		X	X			X		X	X		X
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)	X	X	X	X	X	X	X	X								
CB7	Even (XOR)									X	X	X	X	X	X	X	X

2552 tbl 15

Generated Checkbits	Parity	Participating Data Bits															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CB0	Even (XOR)	X				X		X	X			X		X	X		X
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)									X	X	X	X	X	X	X	X
CB7	Even (XOR)	X	X	X	X	X	X	X	X								

2552 tbl 16

NOTES:

1. The table indicates the data bits participating in the checkbit generation. For example, checkbit C0 is the Exclusive-OR function of the 64 data input bits marked with an X.
2. The checkbit is generated as either an XOR or an XNOR of the 64 data bits noted by an "X" in the table.

DETAILED DESCRIPTION — 64-BIT CONFIGURATION (Con't.)

64-BIT SYNDROME DECODE TO BIT-IN-ERROR(1)

				HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
				S7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
				S6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
			Syndrome	S5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
			Bits	S4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HEX	S3	S2	S1	S0																
0	0	0	0	0	*	C4	C5	T	C6	T	T	62	C7	T	T	46	T	M	M	T
1	0	0	0	1	C0	T	T	14	T	M	M	T	T	M	M	T	M	T	T	30
2	0	0	1	0	C1	T	T	M	T	34	56	T	T	50	40	T	M	T	T	M
3	0	0	1	1	T	18	8	T	M	T	T	M	M	T	T	M	T	2	24	T
4	0	1	0	0	C2	T	T	15	T	35	57	T	T	51	41	T	M	T	T	31
5	0	1	0	1	T	19	9	T	M	T	T	63	M	T	T	47	T	3	25	T
6	0	1	1	0	T	20	10	T	M	T	T	M	M	T	T	M	T	4	26	T
7	0	1	1	1	M	T	T	M	T	36	58	T	T	52	42	T	M	T	T	M
8	1	0	0	0	C3	T	T	M	T	37	59	T	T	53	43	T	M	T	T	M
9	1	0	0	1	T	21	11	T	M	T	T	M	M	T	T	M	T	5	27	T
A	1	0	1	0	T	22	12	T	33	T	T	M	49	T	T	M	T	6	28	T
B	1	0	1	1	17	T	T	M	T	38	60	T	T	54	44	T	1	T	T	M
C	1	1	0	0	T	23	13	T	M	T	T	M	M	T	T	M	T	7	29	T
D	1	1	0	1	M	T	T	M	T	39	61	T	T	55	45	T	M	T	T	M
E	1	1	1	0	16	T	T	M	T	M	M	T	T	M	M	T	0	T	T	M
F	1	1	1	1	T	M	M	T	32	T	T	M	48	T	T	M	T	M	M	T

NOTES: 2552 tbl 17

1. The table indicates the decoding of the seven syndrome bits to identify the bit-in-error for a single-bit error, or whether a double or triple-bit error was detected. The all-zero case indicates no error detected.
   * = No errors detected
   # = The number of the single bit-in-error
   T = Two errors detected
   M = Three or more detected

KEY AC CALCULATIONS — 64-BIT CASCADED CONFIGURATION

	64-Bit Propagation Delay		Total AC Delay for IDT49C465 in 64-bit Mode
Mode	From	To	(L) = Lower slice (U) = Upper slice
Generate	SD Bus	Checkbits out	SD to CBO(L) + PCBI to CBO(U) t SC(L) + t PCC(U)
Detect	MD Bus	$\overline{ERR}$ for 64-bits	MD to SYO(L) + CBI to $\overline{ERR}$ (U) t MSY(L) + t CE (U)
	MD Bus	$\overline{MERR}$ for 64-bits	MD to SYO(L) + CBI to $\overline{M\ ERR}$ t MSY(L) + t CME ($\overline{U}$)
Correct	MD Bus	Corrected data out	MD to SYO(L) + CBI to SD(U) t MSY(L) + t CS (U) (or) → MD to SYO(U) + PCBI to SD(L) t MSY(U) + t PCS(L)

NOTE: 2552 tbl 18

1. (or) = Whichever is worse.

8

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{CC}	Power Supply Voltage	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	30	30	mA

NOTE: 2552 tbl 19

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Ratings for extended periods of time may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2552 tbl 20

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

The following conditions apply unless otherwise specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)			Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level(4)	Guaranteed Logic HIGH	Normal Inputs		2.0	—	—	V
			Hysteresis Inputs		3.0	—	—	
V_{IL}	Input LOW Level(4)	Guaranteed Logic LOW			—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}			—	—	5.0	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND			—	—	–5.0	µA
I_{OZ}	Off State (Hi-Z)	V_{CC} = Max.	V_O = 0V		—	—	–10	µA
			V_O = 3V		—	—	10	
I_{OS}	Short Circuit Current	V_{CC} = Max.(3)			–20	—	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –6mA	COM'L.	2.4	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –4mA	MIL.	2.4	—	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 12mA	COM'L.	—	—	0.5	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 6mA	MIL.	—	—	0.5	
V_H	Hysteresis	$\overline{CLEAR}$, MLE, $\overline{PLE}$, SLE, $\overline{SYNCLK}$, $\overline{SCLKEN}$			—	200	—	mV

NOTES: 2552 tbl 21

1. For conditions shown as min. or max., use appropriate value specified above for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient temperature and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Con't.)

The following conditions apply unless otherwise specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQ}	Quiescent Power Supply Current CMOS Input Levels	V_{IN} = V_{CC} or GND V_{CC} = Max. All Inputs Outputs Disabled		—	—	5	mA
I_{CCQT}	Quiescent Power Supply Current TTL Input Levels	V_{IH} = 3.4V, V_{IL} = 0V V_{CC} = Max. All Inputs Outputs Disabled		—	—	1	mA/ input
I_{CCD1}	Dynamic Power Supply Current f = 10MHz	f_{CP} = 10MHz, 50% Duty Cycle V_{IH} = V_{CC}, V_{IL} = GND Read Mode, Outputs Disabled	COM'L.	—	—	100	mA
			MIL.	—	—	150	
I_{CCD2}	Dynamic Power Supply Current f = 20MHz	f_{CP} = 20MHz, 50% Duty Cycle V_{IH} = V_{CC}, V_{IL} = GND Read Mode, Outputs Disabled	COM'L.	—	—	200	mA
			MIL.	—	—	300	

2552 tbl 22

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified above for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient temperature, and maximum loading.
3. Total supply current is the sum of the Quiescent current and the dynamic current and is calculated as follows:
   $I_{CC} = I_{CCQ} + I_{CCQT} (N_T \times D_T) + I_{CCD} (f_{OP})$
   where: N_T = Total # of quiescent TTL inputs
   D_T = AC Duty cycle – % of time high (TTL)
   f_{OP} = Operating frequency

8

AC PARAMETERS - 49C465A

PROPAGATION DELAY TIMES (PRELIMINARY)

				32-bit System Standalone Slice		64-bit "Generate only" Slice		64-bit System Lower Slice		64-bit System Upper Slice			
				CODE ID=00		CODE ID=01		CODE ID=10		CODE ID=11			
Number	Parameter Name	Parameter Description From Input (edge)	To Output (edge)	Com. Max.	Mil. Max.	Com. Max.	Mil. Max.	Com. Max.	Mil. Max.	Com. Max.	Mil. Max.	Unit	Refer to Timing Diagram Figure
GENERATE (WRITE) PARAMETERS													
01	t_{BC}	BEN	CBO	15	20	—	—	15	20	15	20	ns	—
02	t_{BM}	BEN	MDOUT	15	20	—	—	15	20	15	20	ns	—
03	t_{MC}	**MDIN**	**CBO**	—	—	**15**	**18**	—	—	—	—	ns	10
04	t_{PCC}	**PCBI**	**CBO**	—	—	—	—	—	—	**12**	**18**	ns	7
05	t_{PPE}	PXIN	$\overline{PERR}$	12	18	—	—	12	18	12	18	ns	—
06	t_{SC}		**CBO**	**14**	**18**	**14**	**18**	**14**	**18**	**14**	**18**	ns	7
07	t_{SM}	**SDIN**	MDOUT	12	18	—	—	12	18	12	18	ns	7
08	t_{SPE}		$\overline{PERR}$	12	18	—	—	12	18	12	18	ns	—
DETECT (READ) PARAMETERS													
09	t_{CE}		$\overline{ERR}$ Low	14	18	—	—	—	—	**12**	**18**	ns	8,10
10	t_{CME}	**CBI**	$\overline{MERR}$ = Low	15	20	—	—	—	—	15	20	ns	8,10
11	t_{CSY}		SYO	12	18	—	—	12	18	12	18	ns	8,10
12	t_{ME}		$\overline{ERR}$	**12**	**18**	—	—	—	—	12	18	ns	8,10
13	t_{MME}	**MDIN**	$\overline{MERR}$	16	20	—	—	—	—	16	20	ns	8,10
14	t_{MSY}		**SYO**	12	18	—	—	**12**	**18**	**12**	**18**	ns	8,10
CORRECT (READ) PARAMETERS													
15	t_{CS}	**CBI**	**SDOUT**	16	20	—	—	—	—	**16**	**20**	ns	8,11
16	t_{MP}		PX	18	22	—	—	18	22	18	22	ns	8,11
17	t_{MS}	**MDIN**	**SDOUT**	**14**	**18**	—	—	—	—	—	—	ns	8,11
18	t_{MSY}		**SYO**	16	20	—	—	**12**	**18**	**12**	**18**	ns	8,11
19	t_{PCS}	**PCBI**	**SDOUT**	—	—	—	—	**13**	**18**	—	—	ns	**11**
DIAGNOSTIC PARAMETERS													
20	t_{CLR}	CLEAR = Low	SDOUT	15	20	—	—	15	20	15	20	ns	15
21	t_{MIS}	MODE ID	SDOUT	15	20	—	—	15	20	15	20	ns	15

NOTES:
1. Where "edge" is not specified, both high and low edges are implied.
2. **BOLD** indicates critical system parameters.

2552 tbl 24

AC PARAMETERS - 49C465A

PROPAGATION DELAY TIMES FROM LATCH ENABLES (PRELIMINARY)

Number	Parameter Name	Parameter Description: From Input	(edge)	To Output	(edge)	Com.'l. Max.	Mil. Max.	Unit	Refer to Timing Diagram Figure
22	t MLC			CBO	*	16	20	ns	13
23	t MLE			$\overline{ERR}$	*	13	18	ns	8, 10, 11
24	t MLME	MLE =	High	$\overline{MERR}$	*	16	20	ns	8
25	t MLP			Px	*	18	22	ns	8, 11
26	t MLS			SDOUT	*	18	22	ns	8, 10, 11
27	t MLSY			SYO	*	15	20	ns	8, 10
28	t PLS	$\overline{PLE}$ =	Low	SDOUT	*	10	12	ns	8, 11
29	t PLP	$\overline{PLE}$ =	Low	Px	*	13	18	ns	8, 11
30	t SLC	SLE =	High	CBO	*	16	20	ns	7, 9
31	t SLM	SLE =	High	MDOUT	*	12	18	ns	7, 9

NOTE: 2552 tbl 27

"*" = Both high and low edges are implied.

ENABLE AND DISABLE TIMES (PRELIMINARY)

Number	Parameter Name	Parameter Description: From Input	(edge)	To Output	(edge)	Com'l. Min.	Com'l. Max.	Mil. Min.	Mil. Max.	Unit	Refer to Timing Diagram Figure
32	t BESZx	BEN =	High	SDOUT	*	2	13	2	16	ns	8, 10, 11
33	t BESxZ		Low		Hi – Z	2	11	2	14	ns	
34	t BEPZx	BEN =	High	POUT	*	2	13	2	16	ns	8, 11
35	t BEPxZ		Low		Hi – Z	2	11	2	14	ns	
36	t CECZx	$\overline{CBOE}$ =	Low	CBO	*	2	13	2	16	ns	7, 9
37	t CECxZ		High		Hi – Z	2	11	2	14	ns	
38	t MEMZx	$\overline{MOE}$ =	Low	MDOUT	*	2	13	2	16	ns	7, 9
39	t MEMxZ		High		Hi – Z	2	11	2	14	ns	8, 10
40	t SESZx	$\overline{SOE}$ =	Low	SDOUT	*	2	13	2	16	ns	8, 10
41	t SESxZ		High		Hi – Z	2	11	2	14	ns	7, 9

NOTE: 2552 tbl 28

"*" = Delay to both edges.

8

SET-UP AND HOLD TIMES (PRELIMINARY) - 49C465A

Number	Parameter Name	Parameter Description: From Input (edge)	To Output (edge)	Com.'l. Min.	Mil. Min.	Unit	Refer to Timing Diagram Figure
42	t SSLS	SDIN Set-up *	before SLE = Low	3	4	ns	7, 9
43	t SSLH	SDIN Hold *	after SLE = Low	3	4	ns	7, 9
44	t MMLS	MDIN Set-up *	before MLE =Low	3	4	ns	8, 10, 11
45	t MMLH	MDIN Hold *	after MLE = Low	3	4	ns	8, 10, 11
46	t CMLS	CBI Set-up *	before MLE =Low	3	4	ns	8, 10, 11
47	t CMLH	CBI Hold *	after MLE = Low	3	4	ns	8, 10, 11
48	t MPLS	MDIN Set-up *	before $\overline{PLE}$ =High	10	12	ns	—
49	t MPLH	MDIN Hold *	after $\overline{PLE}$ = High	0	0	ns	—
50	t CPLS	CBI Set-up *	before $\overline{PLE}$ =High	10	12	ns	—
51	t CPLH	CBI Hold *	after $\overline{PLE}$ = High	0	0	ns	—
52	t PCPLS	PCBI Set-up *	before $\overline{PLE}$ =High	10	12	ns	—
53	t PCPLH	PCBI Hold *	after $\overline{PLE}$ = High	0	0	ns	—
DIAGNOSTIC SET-UP AND HOLD TIMES							
54	t CSCS	CBI Set-up *		10	12	ns	15
55	t MSCS	MDIN Set-up *	before SYNCLK=High	10	12	ns	15
56	t MLSCS	MLE Set-up =High		10	12	ns	15
57	t SESCS	SCLKEN Set-up =Low		3	4	ns	15
58	t SESCH	SCLKEN Hold =Low	after SYNCLK =High	3	4	ns	15

NOTE:
"*" = Where "edge" is not specified, both high and low edges are implied.

2552 tbl 32

MINIMUM PULSE WIDTH (PRELIMINARY)

Number	Parameter Name	Minimum Pulse Width: Input		Conditions	Com'l. Min.	Mil. Min.	Unit	Refer to Timing Diagram Figure
59	t CLEAR	Min. $\overline{CLEAR}$ low time	to clear diag. registers	Data = Valid	8	10	ns	14
60	t MLE	Min. MLE high time	to strobe new data	MD, CBI = Valid	5	6	ns	—
61	t PLE	Min. $\overline{PLE}$ low time	to strobe new data	SD = Valid	5	6	ns	—
62	t SLE	Min. SLE high time	to strobe new data	SD = Valid	5	6	ns	—
63	t SYNCLK	Min. SYNCLK high time	to clock in new data	SCKEN = Low	5	6	ns	14

2552 tbl 33

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 18

2552 tbl 34

AC PARAMETERS - 49C465

PROPAGATION DELAY TIMES (PRELIMINARY)

				32-bit System Standalone Slice		64-bit "Generate only" Slice		64-bit System					
								Lower Slice		Upper Slice			
				CODE ID=00		CODE ID=01		CODE ID=10		CODE ID=11			
Number	Parameter Name	Parameter Description From Input (edge)	To Output (edge)	Com. Max.	Mil. Max.	Com. Max.	Mil. Max.	Com. Max.	Mil. Max.	Com. Max.	Mil. Max.	Unit	Refer to Timing Diagram Figure
GENERATE (WRITE) PARAMETERS													
01	t_{BC}	$\overline{BE}_N$	CBO	20	25	—	—	20	25	20	25	ns	—
02	t_{BM}	$\overline{BE}_N$	MDOUT	20	25	—	—	20	25	20	25	ns	—
03	t_{MC}	**MDIN**	**CBO**	—	—	**17**	**20**	—	—	—	—	ns	10
04	t_{PCC}	**PCBI**	**CBO**	—	—	—	—	—	—	**15**	**20**	ns	7
05	t_{PPE}	PXIN	$\overline{PERR}$	15	20	—	—	15	20	15	20	ns	—
06	t_{SC}		**CBO**	**16**	**20**	**16**	**20**	**16**	**20**	**16**	**20**	ns	7
07	t_{SM}	**SDIN**	MDOUT	15	20	—	—	15	20	15	20	ns	7
08	t_{SPE}		$\overline{PERR}$	15	20	—	—	15	20	15	20	ns	—
DETECT (READ) PARAMETERS													
09	t_{CE}		$\overline{ERR}$ = Low	16	20	—	—	—	—	**15**	**20**	ns	8,10
10	t_{CME}	**CBI**	$\overline{MERR}$ = Low	20	24	—	—	—	—	20	24	ns	8,10
11	t_{CSY}		SYO	15	20	—	—	12	18	—	—	ns	8,10
12	t_{ME}		$\overline{ERR}$ = Low	**15**	**20**	—	—	—	—	—	—	ns	8,10
13	t_{MME}	**MDIN**	$\overline{MERR}$ = Low	20	24	—	—	—	—	20	24	ns	8,10
14	t_{MSY}		**SYO**	15	20	—	—	**15**	**20**	**15**	**20**	ns	8,10
CORRECT (READ) PARAMETERS													
15	t_{CS}	**CBI**	**SDOUT**	20	24	—	—	—	—	**20**	**24**	ns	8,11
16	t_{MP}		PX	20	26	—	—	20	26	20	26	ns	8,11
17	t_{MS}	**MDIN**	**SDOUT**	**16**	**20**	—	—	—	—	—	—	ns	8,11
18	t_{MSY}		**SYO**	18	22	—	—	**15**	**20**	**15**	**20**	ns	8,11
19	t_{PCS}	**PCBI**	**SDOUT**	—	—	—	—	**15**	**20**	—	—	ns	11
DIAGNOSTIC PARAMETERS													
20	t_{CLR}	CLEAR = Low	SDOUT	20	24	—	—	20	24	20	24	ns	15
21	t_{MIS}	MODE ID	SDOUT	20	24	—	—	20	24	20	24	ns	15

NOTES:
1. Where "edge" is not specified, both high and low edges are implied.
2. **BOLD** indicates critical system parameters.

2552 tbl 23

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AC PARAMETERS - 49C465

PROPAGATION DELAY TIMES FROM LATCH ENABLES (PRELIMINARY)

Number	Parameter Name	Parameter Description: From Input (edge)	Parameter Description: To Output (edge)	Com.'l. Max.	Mil. Max.	Unit	Refer to Timing Diagram Figure
22	t MLC		CBO *	20	24	ns	13
23	t MLE		$\overline{ERR}$ *	15	20	ns	8, 10, 11
24	t MLME	MLE = High	$\overline{MERR}$ *	20	24	ns	8
25	t MLP		Px *	20	25	ns	8, 11
26	t MLS		SDOUT *	20	25	ns	8, 10, 11
27	t MLSY		SYO *	18	22	ns	8, 10
28	t PLS	$\overline{PLE}$ = Low	SDOUT *	12	16	ns	8, 11
29	t PLP	$\overline{PLE}$ = Low	Px *	16	20	ns	8, 11
30	t SLC	SLE = High	CBO *	20	24	ns	7, 9
31	t SLM	SLE = High	MDOUT *	15	20	ns	7, 9

NOTE:
"*" = Both high and low edges are implied.

2552 tbl 25

ENABLE AND DISABLE TIMES (PRELIMINARY)

Number	Parameter Name	Parameter Description: From Input (edge)	Parameter Description: To Output (edge)	Com'l. Min.	Com'l. Max.	Mil. Min.	Mil. Max.	Unit	Refer to Timing Diagram Figure
32	t BESZx	BEN = High	SDOUT *	2	15	2	18	ns	8, 10, 11
33	t BESxZ	Low	Hi – Z	2	13	2	16	ns	
34	t BEPZx	BEN = High	POUT *	2	15	2	18	ns	8, 11
35	t BEPxZ	Low	Hi – Z	2	13	2	16	ns	
36	t CECZx	$\overline{CBOE}$ = Low	CBO *	2	15	2	18	ns	7, 9
37	t CECxZ	High	Hi – Z	2	13	2	16	ns	
38	t MEMZx	$\overline{MOE}$ = Low	MDOUT *	2	15	2	18	ns	7, 9
39	t MEMxZ	High	Hi – Z	2	13	2	16	ns	8, 10
40	t SESZx	$\overline{SOE}$ = Low	SDOUT *	2	15	2	18	ns	8, 10
41	t SESxZ	High	Hi – Z	2	13	2	16	ns	7, 9

NOTE:
"*" = Delay to both edges.

2552 tbl 26

SET-UP AND HOLD TIMES (PRELIMINARY) - 49C465

Number	Parameter Name	Parameter Description: From Input (edge)	To Output (edge)	Com.'l. Min.	Mil. Min.	Unit	Refer to Timing Diagram Figure
42	t SSLS	SDIN Set-up *	before SLE = Low	4	5	ns	7, 9
43	t SSLH	SDIN Hold *	after SLE = Low	4	5	ns	7, 9
44	t MMLS	MDIN Set-up *	before MLE =Low	4	5	ns	8, 10, 11
45	t MMLH	MDIN Hold *	after MLE = Low	4	5	ns	8, 10, 11
46	t CMLS	CBI Set-up *	before MLE =Low	4	5	ns	8, 10, 11
47	t CMLH	CBI Hold *	after MLE = Low	4	5	ns	8, 10, 11
48	t MPLS	MDIN Set-up *	before $\overline{PLE}$ =High	12	15	ns	—
49	t MPLH	MDIN Hold *	after $\overline{PLE}$ = High	0	0	ns	—
50	t CPLS	CBI Set-up *	before $\overline{PLE}$ =High	12	15	ns	—
51	t CPLH	CBI Hold *	after $\overline{PLE}$ = High	0	0	ns	—
52	t PCPLS	PCBI Set-up *	before $\overline{PLE}$ =High	12	15	ns	—
53	t PCPLH	PCBI Hold *	after $\overline{PLE}$ = High	0	0	ns	—
DIAGNOSTIC SET-UP AND HOLD TIMES							
54	t CSCS	CBI Set-up *		12	15	ns	15
55	t MSCS	MDIN Set-up *	before SYNCLK=High	12	15	ns	15
56	t MLSCS	MLE Set-up = High		12	15	ns	15
57	t SESCS	SCLKEN Set-up =Low		4	5	ns	15
58	t SESCH	SCLKEN Hold =Low	after SYNCLK =High	4	5	ns	15

NOTE:
"*" = Where "edge" is not specified, both high and low edges are implied.

2552 tbl 29

MINIMUM PULSE WIDTH (PRELIMINARY)

Number	Parameter Name	Minimum Pulse Width Input		Conditions	Com'l. Min.	Mil. Min.	Unit	Refer to Timing Diagram Figure
59	t CLEAR	Min. $\overline{CLEAR}$ low time	to clear diag. registers	Data = Valid	8	10	ns	14
60	t MLE	Min. MLE high time	to strobe new data	MD, CBI = Valid	5	6	ns	—
61	t PLE	Min. $\overline{PLE}$ low time	to strobe new data	SD = Valid	5	6	ns	—
62	t SLE	Min. SLE high time	to strobe new data	SD = Valid	5	6	ns	—
63	t SYNCLK	Min. SYNCLK high time	to clock in new data	SCLKEN = Low	5	6	ns	14

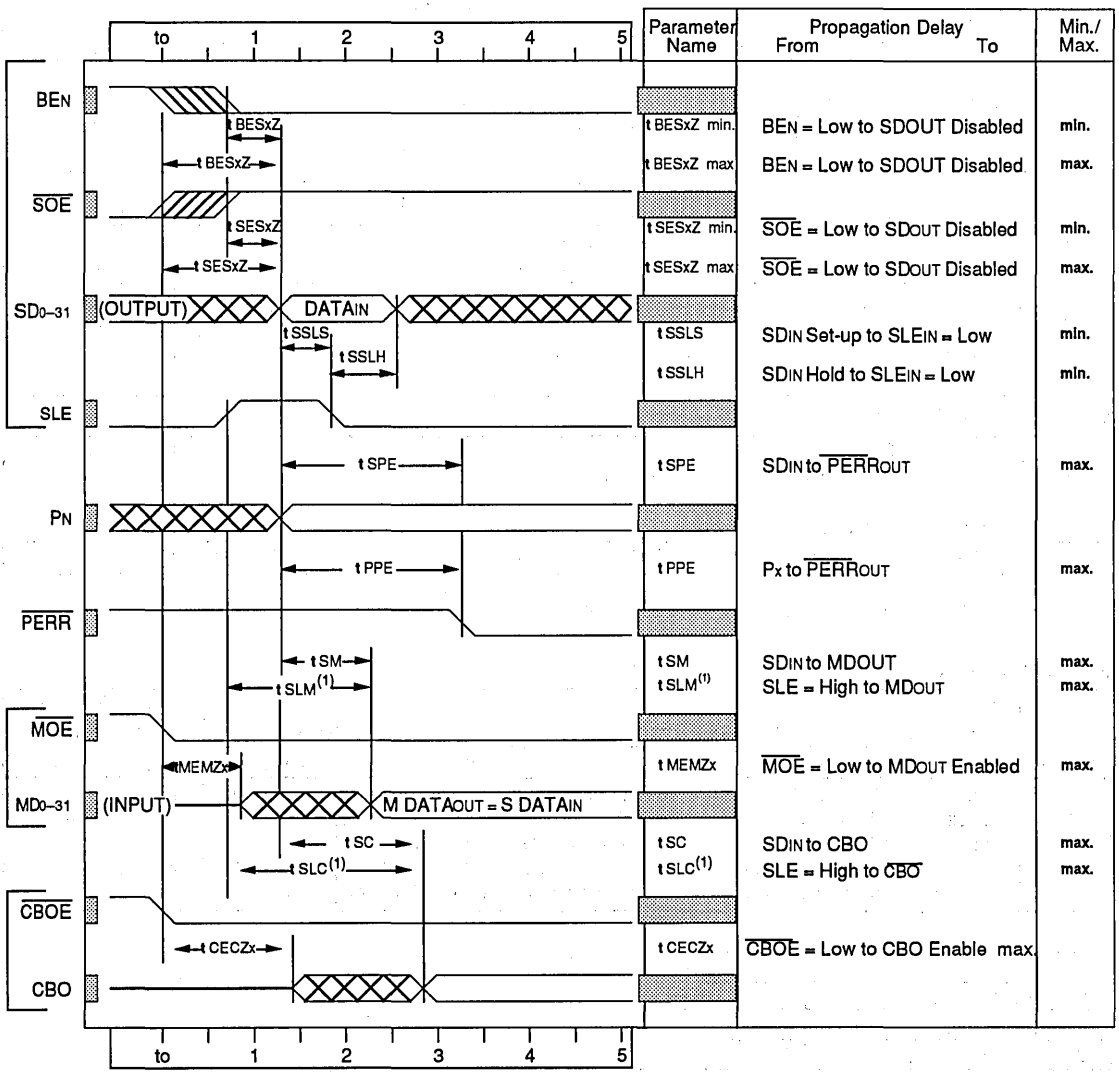
2552 tbl 30

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 18

2552 tbl 31

8

AC TIMING DIAGRAMS — 32-BIT CONFIGURATION

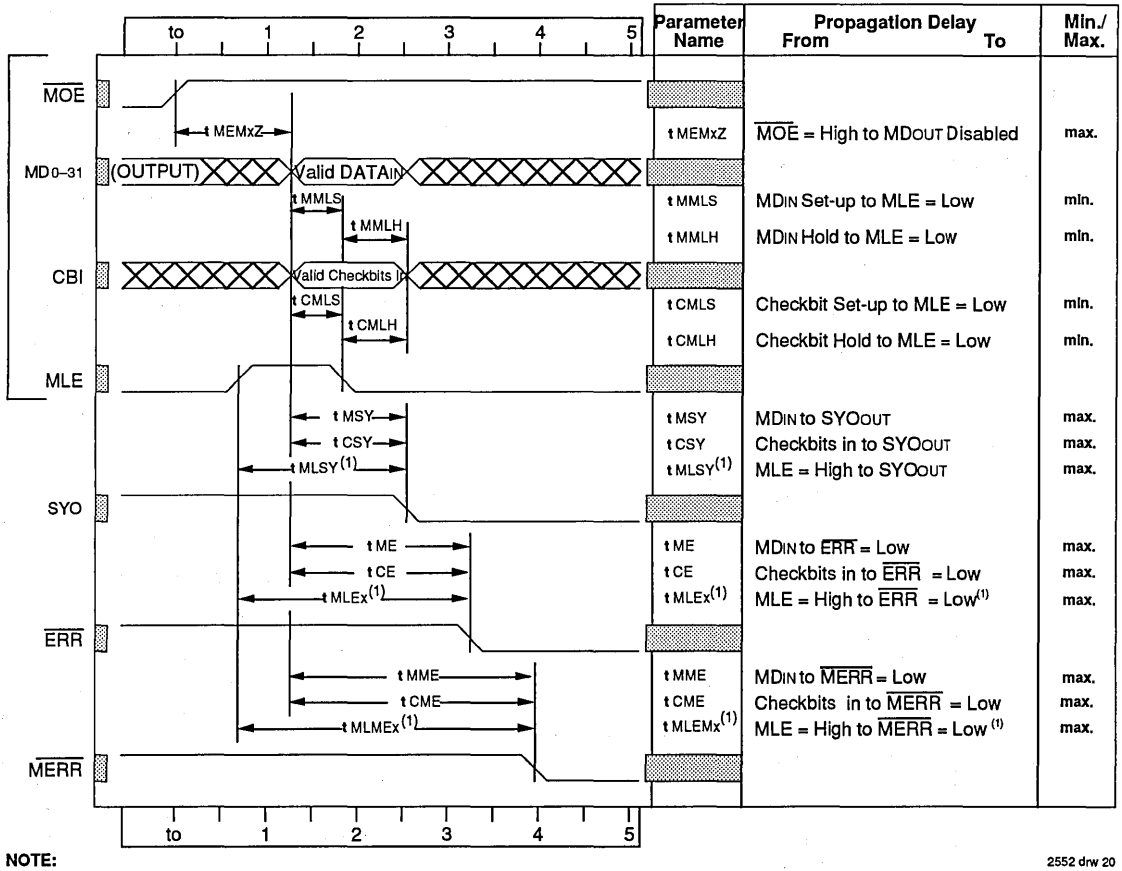


NOTE:
1. Assumes that System Data is valid at least 3ns (Com.) before SLE goes high.

2552 drw 19

Figure 7. 32-Bit Generate Timing

AC TIMING DIAGRAMS — 32-BIT CONFIGURATION



Parameter Name	Propagation Delay From To	Min./ Max.
t MEMxZ	$\overline{MOE}$ = High to MDOUT Disabled	max.
t MMLS	MDIN Set-up to MLE = Low	min.
t MMLH	MDIN Hold to MLE = Low	min.
t CMLS	Checkbit Set-up to MLE = Low	min.
t CMLH	Checkbit Hold to MLE = Low	min.
t MSY	MDIN to SYOOUT	max.
t CSY	Checkbits in to SYOOUT	max.
t MLSY(1)	MLE = High to SYOOUT	max.
t ME	MDIN to $\overline{ERR}$ = Low	max.
t CE	Checkbits in to $\overline{ERR}$ = Low	max.
t MLEx(1)	MLE = High to $\overline{ERR}$ = Low(1)	max.
t MME	MDIN to $\overline{MERR}$ = Low	max.
t CME	Checkbits in to $\overline{MERR}$ = Low	max.
t MLEMx(1)	MLE = High to $\overline{MERR}$ = Low (1)	max.

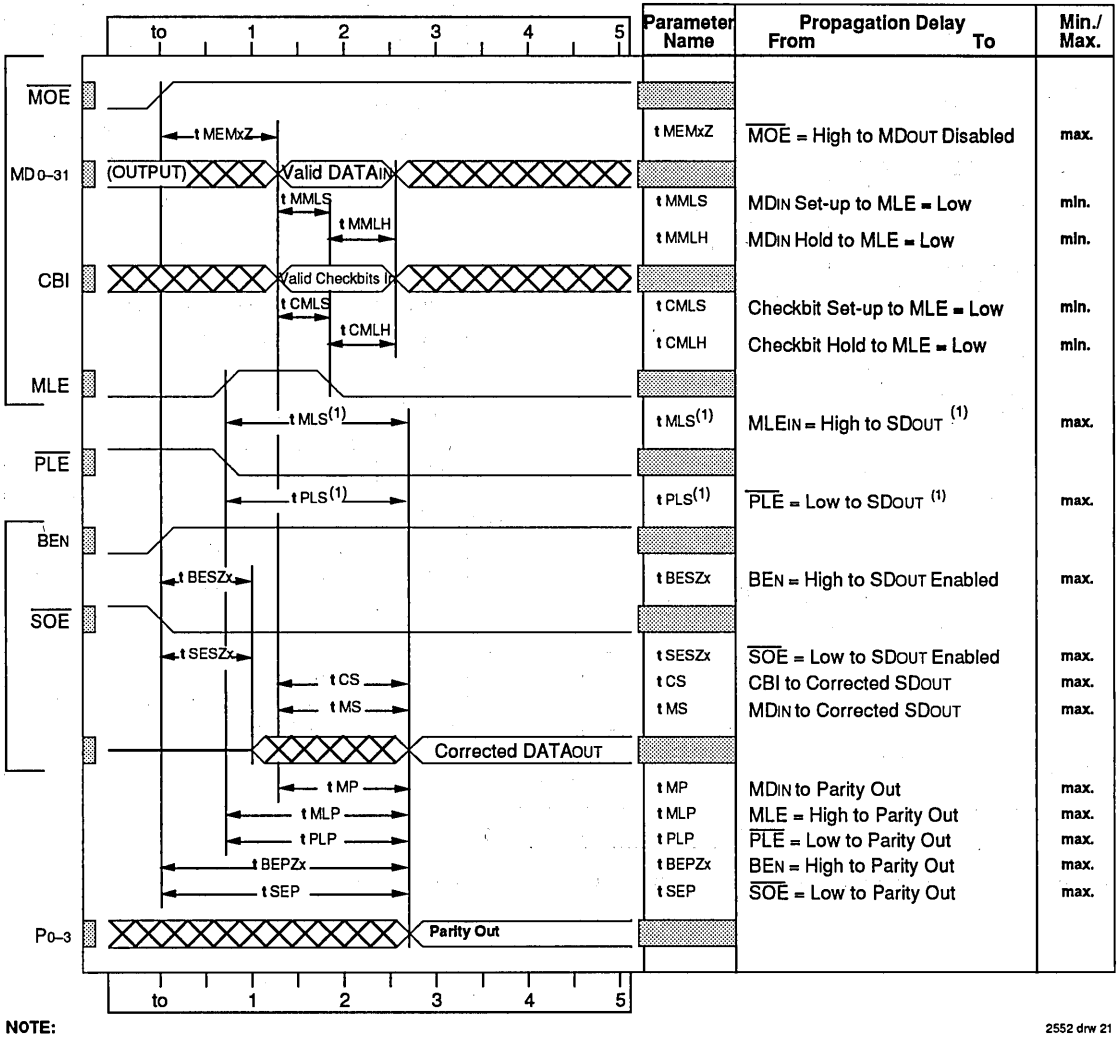
NOTE:
1. Assumes that Memory Data and Checkbits are valid at least 3ns (Com.)/4ns (Mil.) before MLE goes high.

2552 drw 20

Figure 8. 32-Bit Detect Timing

8

AC TIMING DIAGRAMS — 32-BIT CONFIGURATION

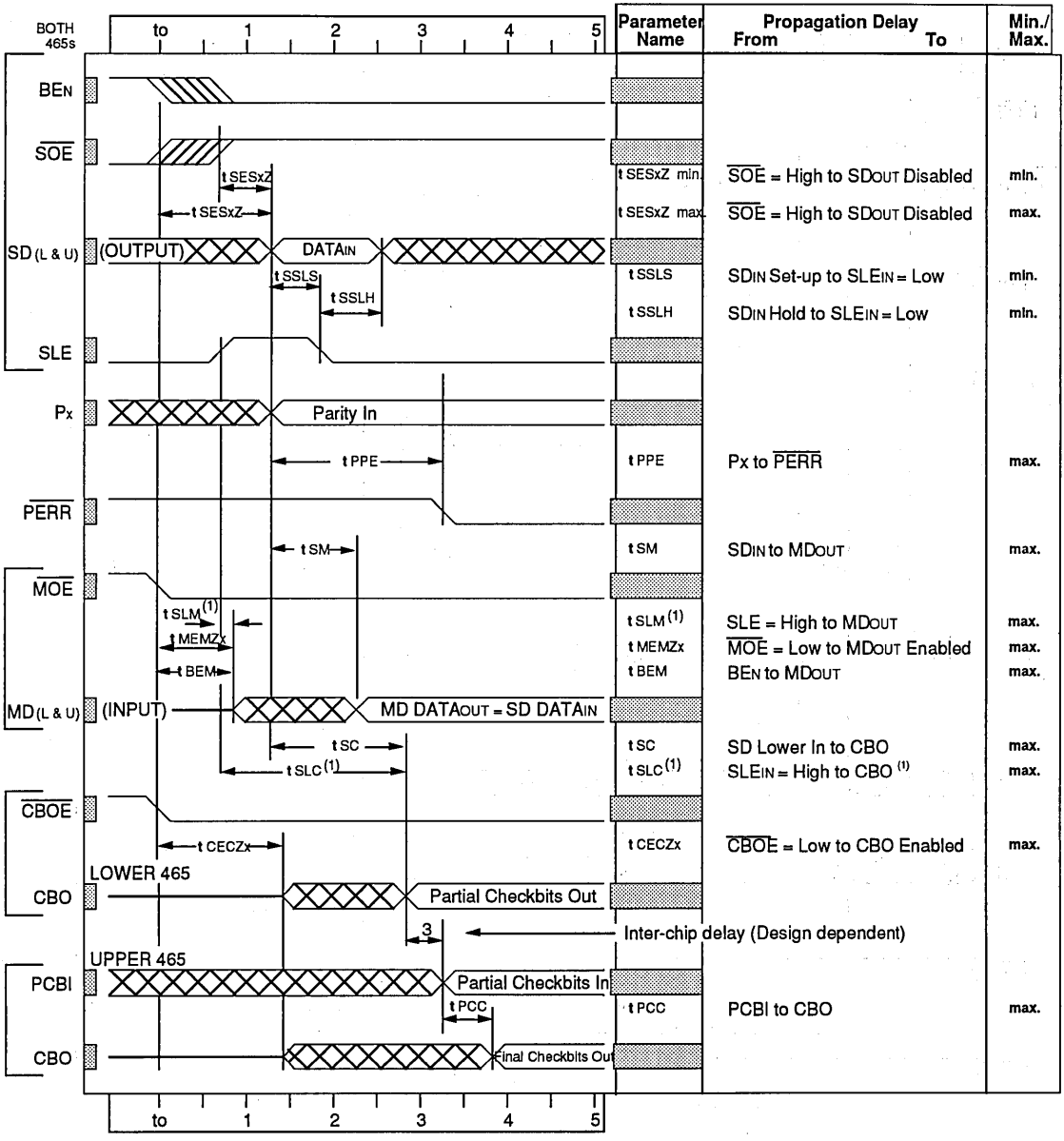


NOTE:
1. Assumes that Memory Data and Checkbits are valid at least 3ns (Com.)/4ns (Mil.) before MLE goes high.

2552 drw 21

Figure 9. 32-Bit Correct Timing

AC TIMING DIAGRAMS — 64-BIT CONFIGURATION



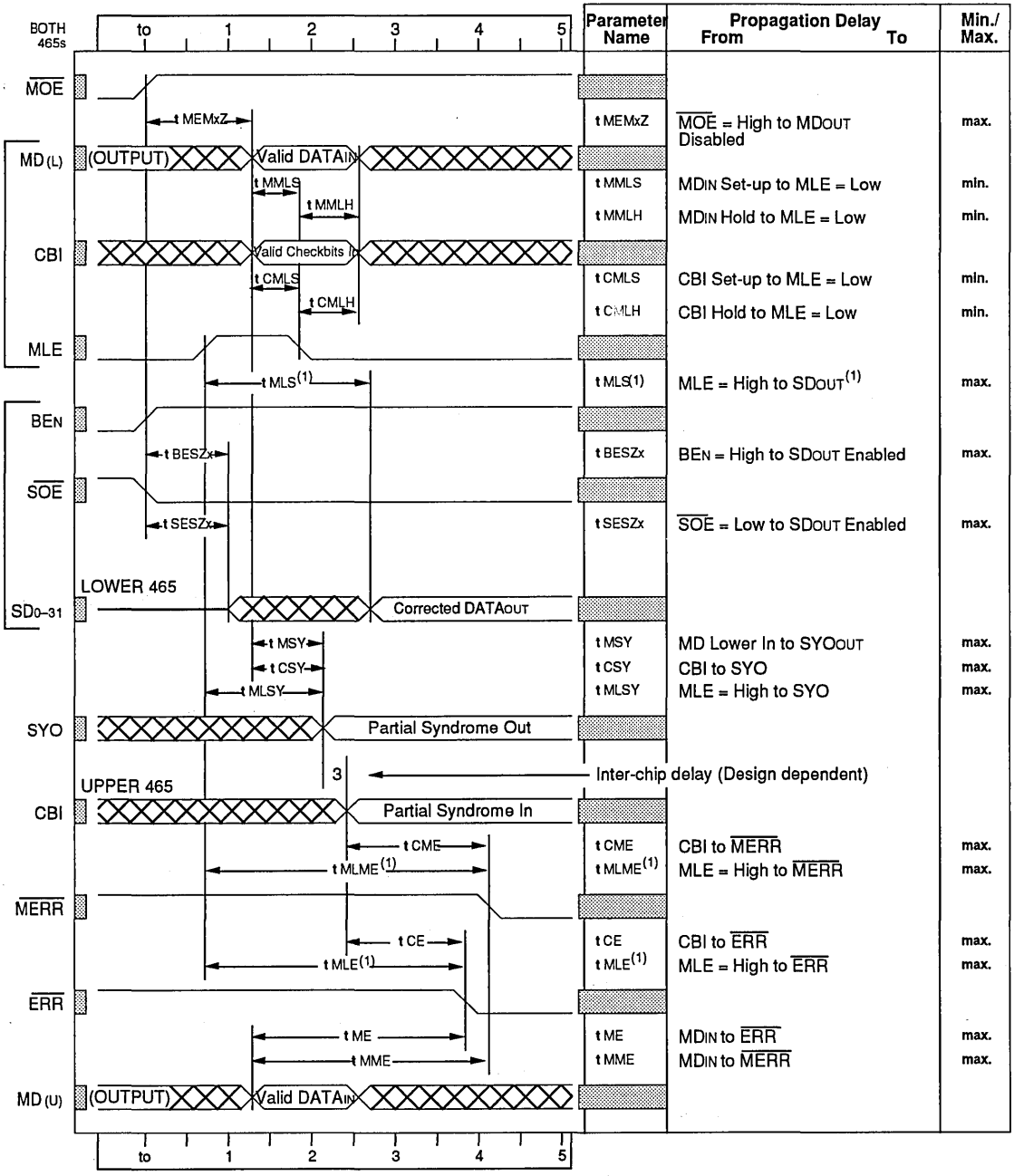
NOTE:
1. Assumes that System Data is valid at least 3ns (Com.)/4ns (Mil.) before SLE goes high.

2552 drw 22

Figure 10. 64-Bit Generate Timing — (64-Bit Cascading System)

8

AC TIMING DIAGRAMS — 64-BIT CONFIGURATION

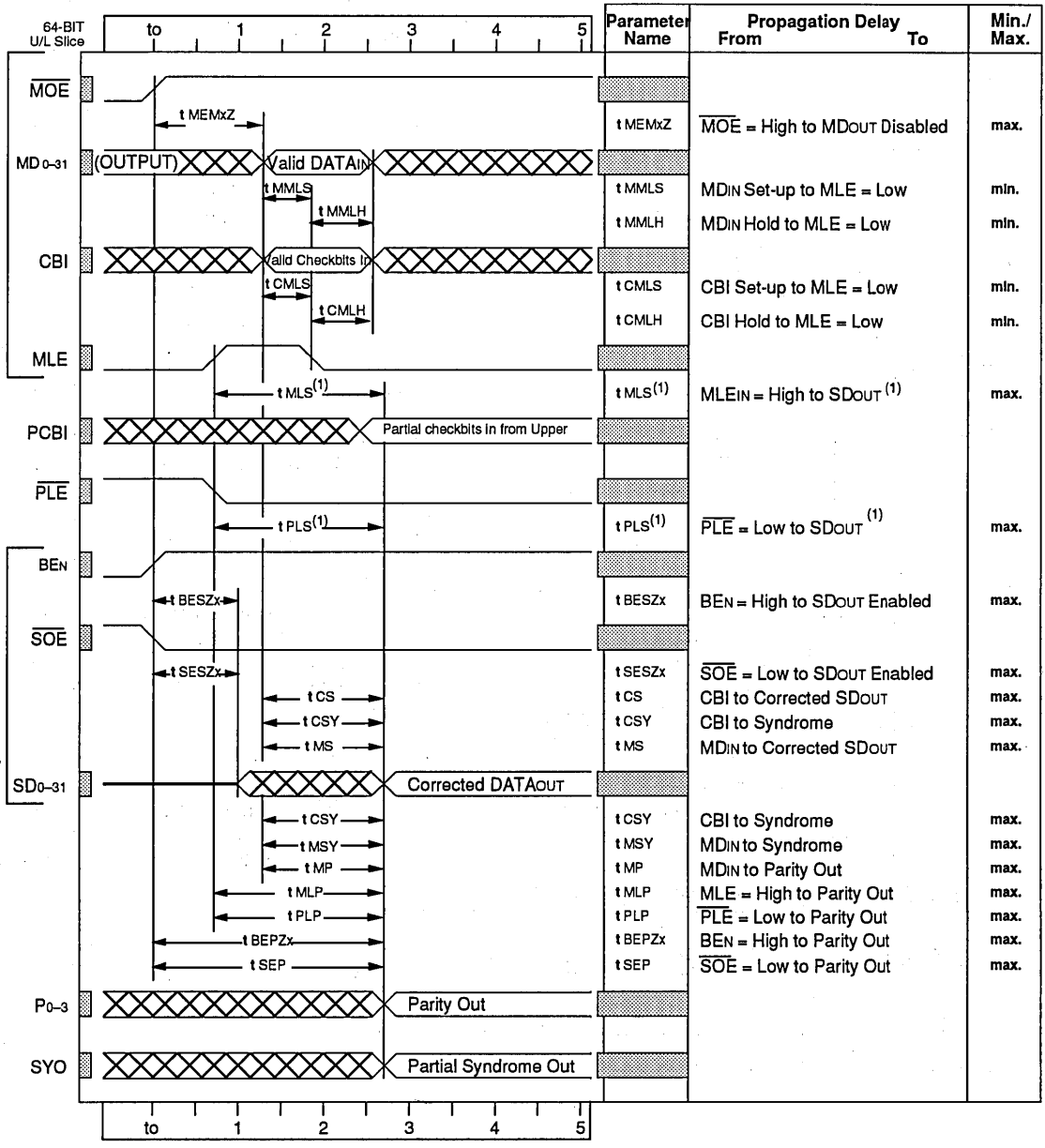


NOTE:
1. Assumes that System Data is valid at least 3ns (Com.)/4ns (Mil.) before SLE goes high.

2552 drw 23

Figure 11. 64-Bit Detect Timing

AC TIMING DIAGRAMS — 64-BIT CONFIGURATION



Parameter Name	Propagation Delay From To	Min./ Max.
t MEMxZ	$\overline{MOE}$ = High to MDOUT Disabled	max.
t MMLS	MDIN Set-up to MLE = Low	min.
t MMLH	MDIN Hold to MLE = Low	min.
t CMLS	CBI Set-up to MLE = Low	min.
t CMLH	CBI Hold to MLE = Low	min.
t MLS(1)	MLEIN = High to SDOUT (1)	max.
t PLS(1)	$\overline{PLE}$ = Low to SDOUT (1)	max.
t BESZx	BEN = High to SDOUT Enabled	max.
t SESZx	$\overline{SOE}$ = Low to SDOUT Enabled	max.
t CS	CBI to Corrected SDOUT	max.
t CSY	CBI to Syndrome	max.
t MS	MDIN to Corrected SDOUT	max.
t CSY	CBI to Syndrome	max.
t MSY	MDIN to Syndrome	max.
t MP	MDIN to Parity Out	max.
t MLP	MLE = High to Parity Out	max.
t PLP	$\overline{PLE}$ = Low to Parity Out	max.
t BEPZx	BEN = High to Parity Out	max.
t SEP	$\overline{SOE}$ = Low to Parity Out	max.

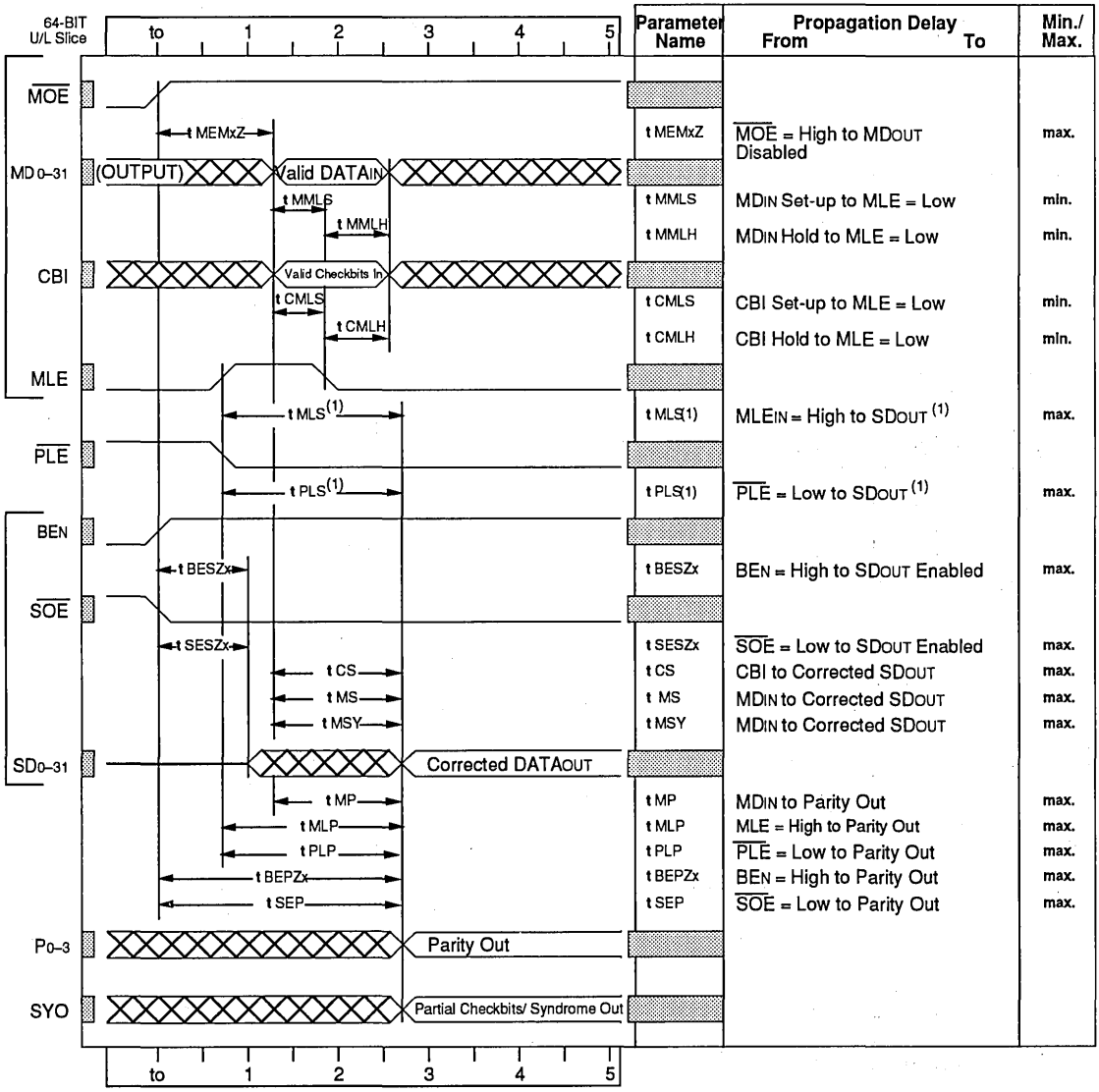
NOTE:
1. Assumes that Memory Data and Checkbits are valid at least 4ns (Com.) before MLE goes high.

2552 drw 24

Figure 12. 64-Bit Correct Timing (Lower Slice)

8

AC TIMING DIAGRAMS — 64-BIT CONFIGURATION

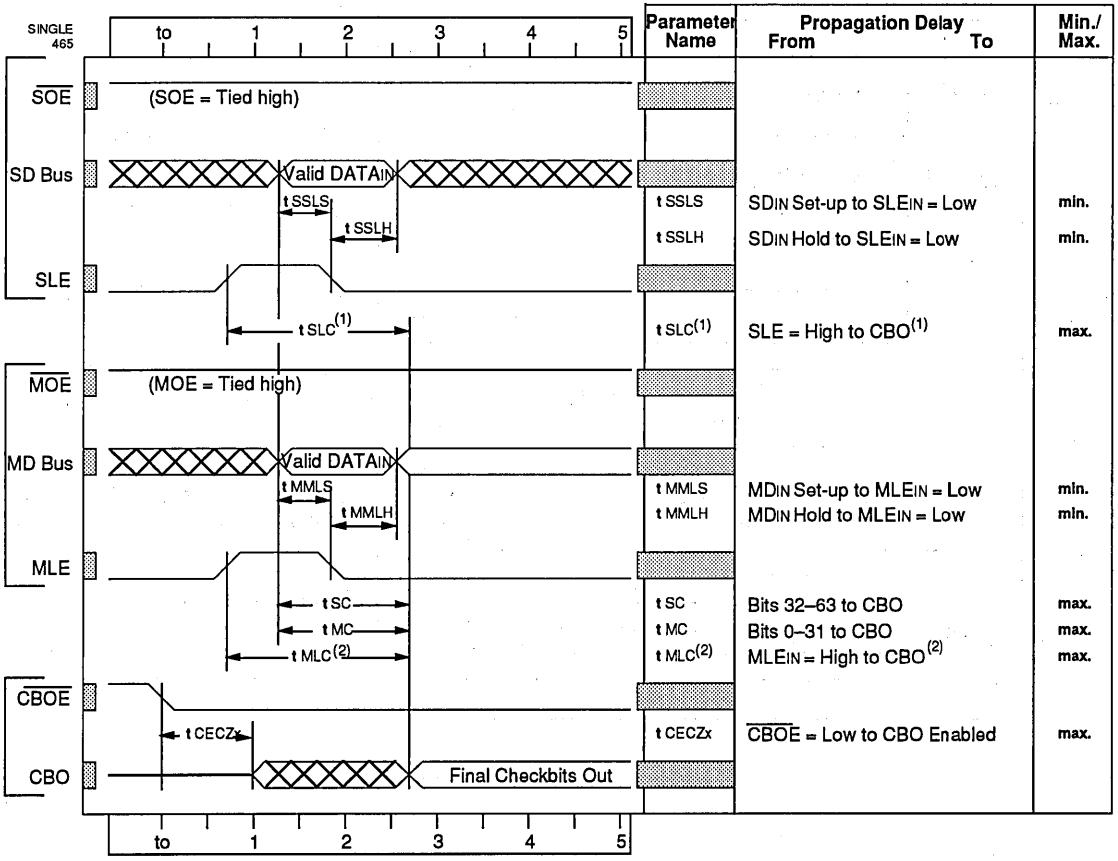


NOTE:
1. Assumes that Memory Data and Checkbits are valid at least 4ns (Com.) before MLE goes high.

2552 drw 25

Figure 13. 64-Bit Correct Timing (Upper Slice)

AC TIMING DIAGRAMS — 64-BIT CONFIGURATION



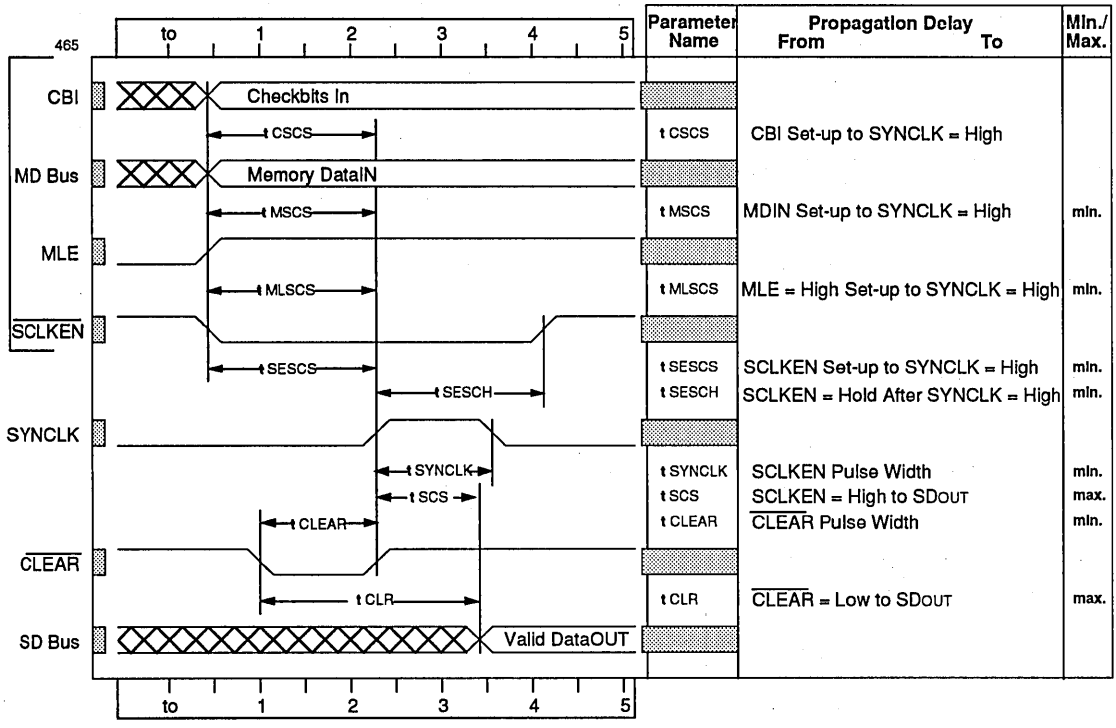
NOTE:
1. Assumes that System Data is valid at least 3ns (Com.) before SLE goes high.
2. Assumes that Memory Data is valid at least 4ns (Com.) before MLE goes high.

2552 drw 26

Figure 14. 64-Bit Single Chip "Generate Only" Timing

8

AC TIMING DIAGRAMS — DIAGNOSTIC TIMING



2552 drw 27

Figure 15. 32-Bit Diagnostic Timing

INPUT/OUTPUT INTERFACE CIRCUITS

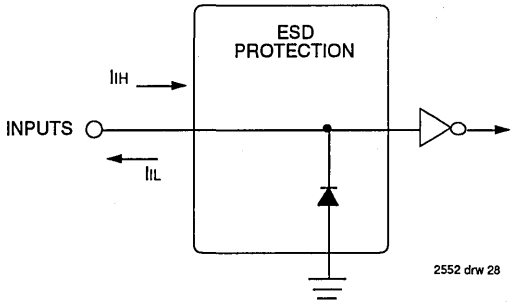


Figure 16. Input Structure (All Inputs)

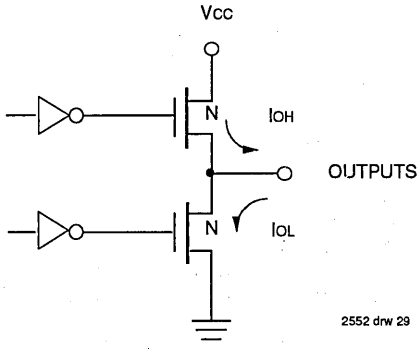


Figure 17. Output Structure

AC TEST CIRCUIT

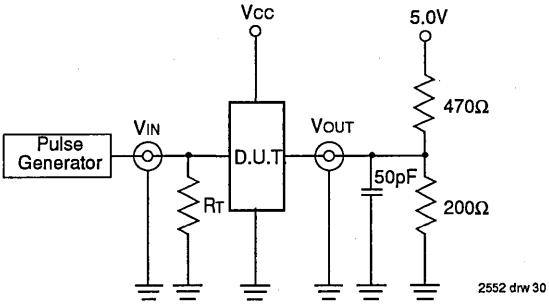


Figure 18.

Test	Switch
Disable Low Enable Low	Closed
All other tests	Open

2552 tbl 35

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

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Integrated Device Technology, Inc.

64-BIT FLOW-THRU ERROR DETECTION AND CORRECTION UNIT

PRELIMINARY
IDT49C466

FEATURES:

- 64-bit wide Flow-thruEDC™
- Separate System and Memory Data Input/Output Buses
- — Error Detect Time: 20ns
  — Error Correct Time: 22ns
- Corrects all single bit errors; Detects all double bit errors and some multiple bit errors
- Configurable 16-deep bus read/write FIFOs with flags
- Simultaneous check bit generation and correction of memory data
- Supports partial word writes on byte boundaries
- Low noise output
- Sophisticated error diagnostics and error logging
- Parity generation on system data bus
- 208-pin Pin Grid Array and Plastic Quad Flatpack

DESCRIPTION:

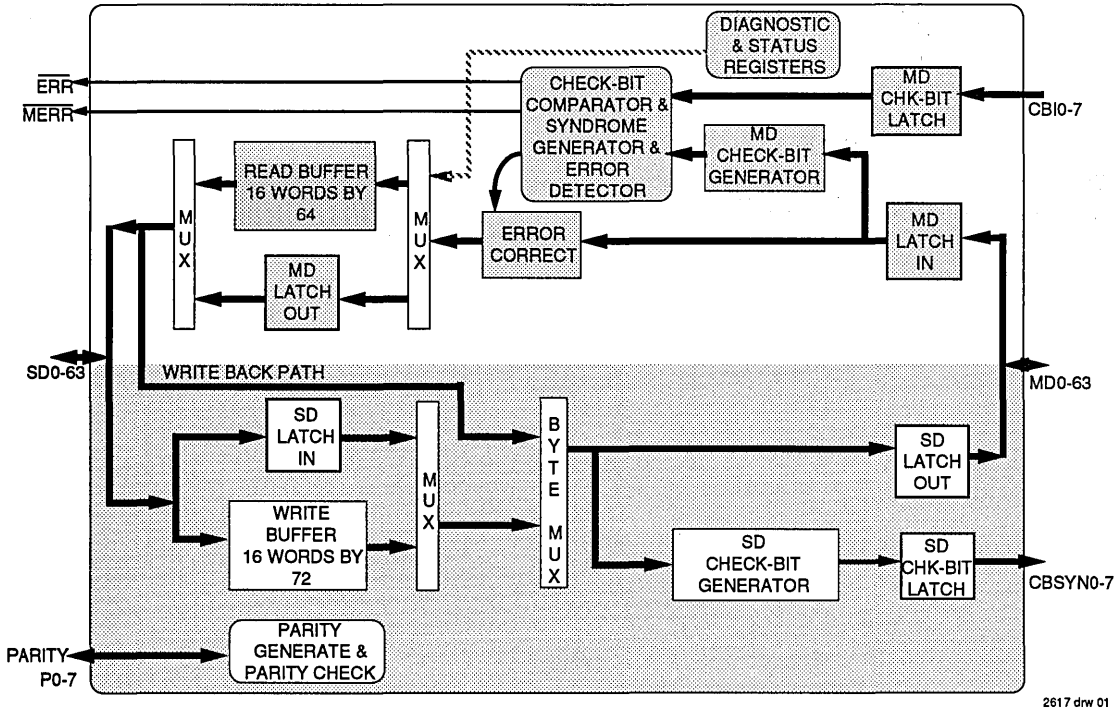
The IDT49C466 64-bit Flow-thruEDC is a high-speed error detection and correction unit that ensures data integrity in memory systems. The flow-thru architecture, with separate system and memory data buses, is ideally suited for pipelined memory systems.

Implementing a modified Hamming code, the IDT49C466 corrects all single bit hard and soft errors, and detects all double bit errors. The read/write FIFOs can store up to sixteen words. FIFO full and empty flags indicate whether additional data can be written to or read from the EDC.

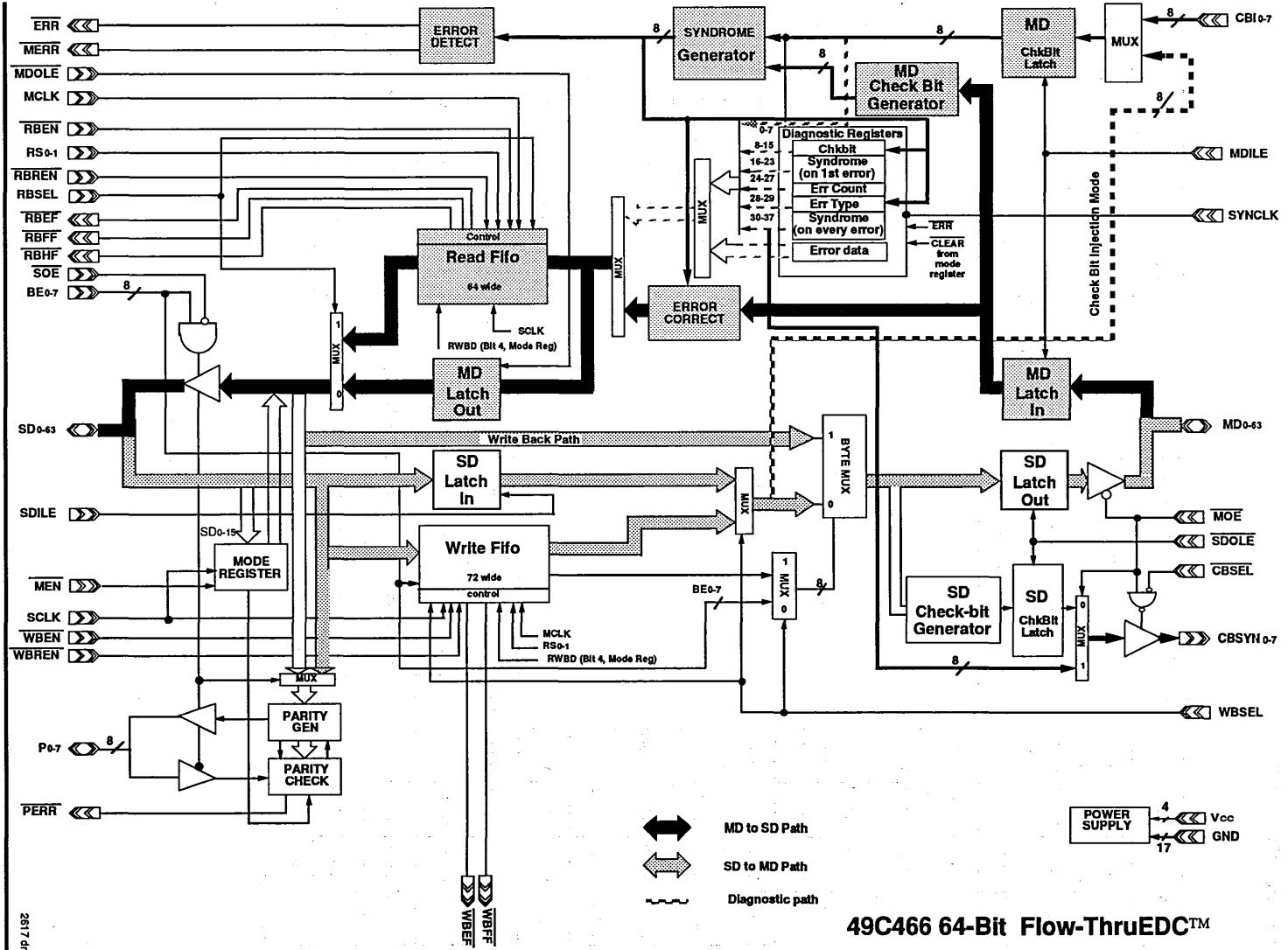
Check bit generation for partial word writes on byte boundaries is supported on the IDT49C466.

Diagnostic features include a check bit register, syndrome registers, a four bit error counter which logs up to 15 errors, and an error data register which stores the complete error data word. Parity can be generated and checked on the system bus by the IDT49C466.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



Flow-thruEDC is a trademark of Integrated Device Technology Inc.



49C466 64-Bit Flow-ThruEDC™

REV E - STANDARD DEVICE

5/8/92

PIN CONFIGURATION

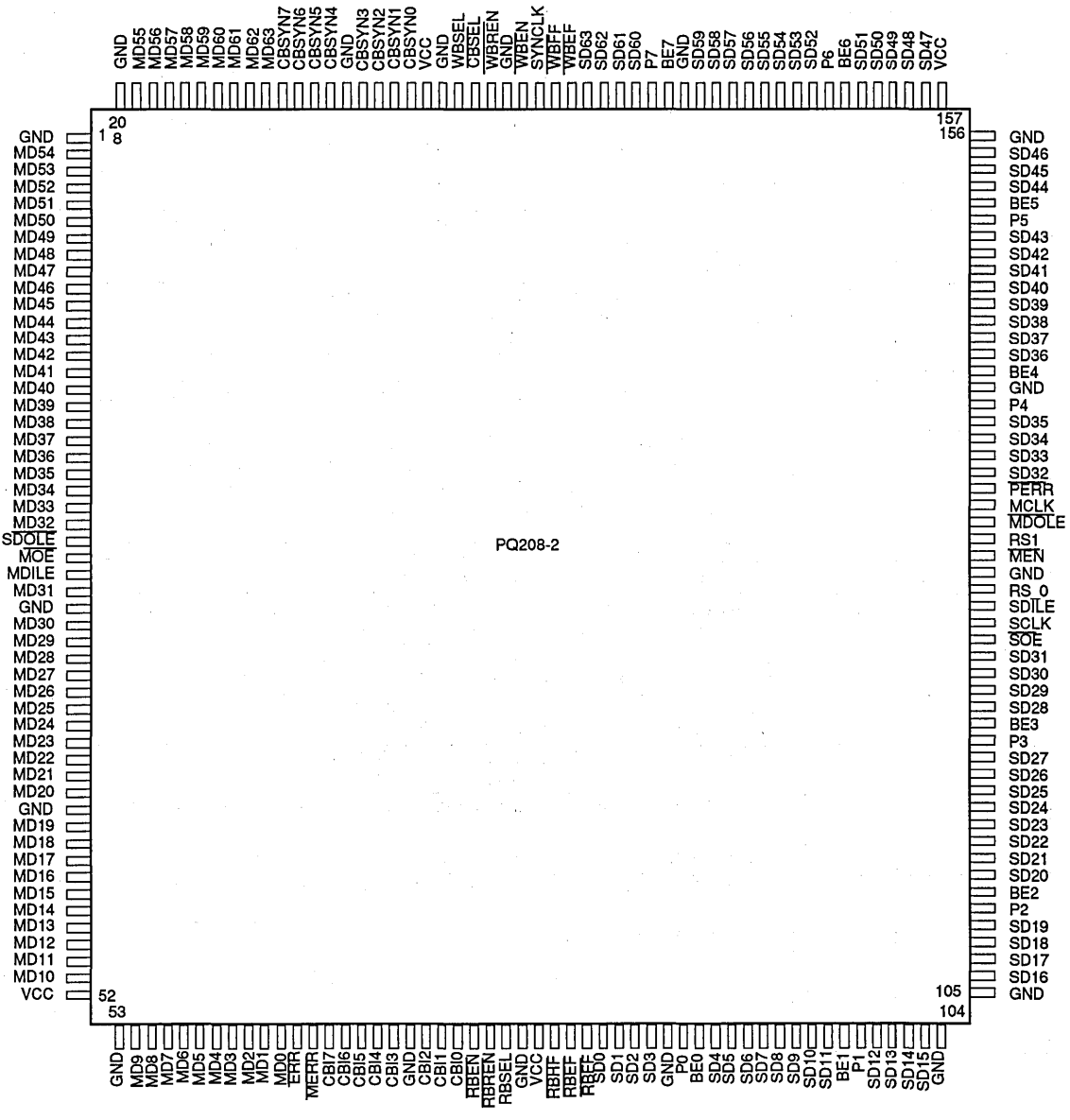
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	
17	MD_10	MD_8	MD_2	MD_1	$\overline{\text{MERR}}$	CBI_6	CBI_1	$\overline{\text{RBEN}}$	RBSEL	$\overline{\text{RBHF}}$	SD_2	SD_3	BE0	SD_9	SD_10	SD_12	SD_15	17
16	MD_13	MD_9	MD_6	MD_3	$\overline{\text{ERR}}$	CBI_3	CBI_2	$\overline{\text{RBREN}}$	$\overline{\text{RBEF}}$	$\overline{\text{RBFF}}$	SD_1	SD_4	SD_6	SD_8	SD_13	SD_16	SD_17	16
15	MD_17	MD_12	MD_11	MD_5	MD_4	CBI_7	CBI_4	CBI_0	GND	SD_0	P0	SD_7	P1	BE1	SD_14	SD_19	SD_21	15
14	MD_18	MD_19	MD_15	GND	MD_7	MD_0	CBI_5	GND	VCC	GND	SD_5	SD_11	GND	GND	P2	BE2	SD_20	14
13	MD_23	MD_20	MD_14	VCC										SD_18	SD_22	SD_24	SD_25	13
12	MD_25	MD_22	MD_21	MD_16										SD_23	SD_26	SD_28	SD_27	12
11	MD_27	MD_28	MD_24	GND										P3	BE3	SD_30	SD_29	11
10	MD_31	MD_30	MD_29	MD_26										SD_31	$\overline{\text{SOE}}$	SDILE	SCLK	10
9	$\overline{\text{SDOLE}}$	$\overline{\text{MOE}}$	MDILE	GND				G208-1						$\overline{\text{MDOLE}}$	GND	$\overline{\text{MEN}}$	RS_0	9
8	MD_33	MD_32	MD_34	MD_35										GND	SD_33	MCLK	RS_1	8
7	MD_37	MD_36	MD_39	MD_40										SD_37	SD_34	SD_32	$\overline{\text{PERR}}$	7
6	MD_41	MD_38	MD_42	MD_45										SD_42	SD_38	P4	SD_35	6
5	MD_43	MD_44	MD_46	MD_52										GND	P5	BE4	SD_36	5
4	MD_48	MD_49	MD_50	GND	GND	MD_61	CBSYN4	VCC	GND	SD_61	GND	SD_54	SD_49	VCC	SD_43	SD_39	SD_40	4
3	MD_47	MD_51	MD_56	MD_60	MD-59	CBSYN6	GND	GND	$\overline{\text{WBEN}}$	SD_62	SD_59	SD_57	SD_53	SD_51	SD_45	SD_44	SD_41	3
2	MD_53	MD_54	MD_57	CBSYN7	CBSYN5	CBSYN2	CBSYN0	WBREN	SYNCLK	$\overline{\text{WBEF}}$	SD_60	BE7	SD_55	BE6	SD_50	SD_47	BE5	2
1	MD_55	MD_58	MD_62	MD_63	CBSYN3	CBSYN1	WBSEL	$\overline{\text{CBSEL}}$	$\overline{\text{WBFF}}$	SD_63	P7	SD_58	SD_56	P6	SD_52	SD_48	SD_46	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	

Pin 1 reference

2617 drw 03

208-pin PGA Package
Top View

PIN CONFIGURATION



PQFP

Top View

2617 drw 04

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PIN DESCRIPTION

Pin Name	I/O	Description
Data Buses		
SD_{0-63}	I/O	**System Data Bus:** is a bidirectional 64-bit bus interfacing to the system or CPU. When System Output Enable, $\overline{SOE}$, is HIGH or Byte Enable, BE_{0-7}, is LOW, data can be input. When System Output Enable, $\overline{SOE}$, is LOW and Byte Enable, BE_{0-7}, is HIGH, the SD bus output drivers are enabled.
MD_{0-63}	I/O	**Memory Data Bus:** is a bidirectional 64-bit bus interfacing to the memory. During a read cycle, ($\overline{MOE}$ HIGH) memory data is input for error detection and correction. Data is output on the Memory Data Bus, when $\overline{MOE}$ is LOW.
CBI_{0-7}	I	**Check Bit Inputs:** interface to the check bit memory.
$CBSYN_{0-7}$	O	**Check Bit or Syndrome Output:** When $\overline{MOE}$ is LOW the generated check bits are output. When CBSEL is HIGH and $\overline{MOE}$ is HIGH, the syndrome bits are output. The bus is tristated when $\overline{MOE}$ = 1 and CBSEL = 0.
P_{0-7}	I/O	**Parity for bytes 0 to 7:** These pins are parity inputs when the corresponding Byte Enable (BE) is LOW or $\overline{SOE}$ is HIGH, and are used to generate the parity error signal ($\overline{PERR}$). These pins are outputs when the corresponding Byte Enable (BE) is HIGH and $\overline{SOE}$ is LOW.
Control Inputs		
$\overline{SOE}$	I	**System Output Enable:** enables system data bus output drivers if the corresponding Byte Enable (BE_{0-7}) is HIGH.
BE_{0-7}	I	**Byte Enable:** is used along with $\overline{SOE}$, to enable the System Data outputs for a particular byte. For example, if BE_1 is HIGH, the System data outputs for byte 1 (SD_{8-15}) are enabled. The BE_{0-7} pins also control the byte mux. If a particular BE is HIGH during a memory read cycle, that byte is fed back to the memory data bus. This is used during partial word write operations and writing corrected data back to memory.
$\overline{MOE}$	I	**Memory Output Enable:** when LOW, enables the output buffers of the memory data bus (MD). It also controls the check bit output buffer enable and CBSYN mux.
MDILE	I	**Memory Data Input Latch Enable:** on the HIGH-to-LOW transition, latches MD and CBI in MD input latch and MD check bit latch respectively. The latches are transparent when MDILE is HIGH.
$\overline{MDOLE}$	I	**Memory Data Output Latch Enable:** latches data in the MD output latch on the LOW-to-HIGH transition of $\overline{MDOLE}$. When $\overline{MDOLE}$ is LOW, the MD output latch is transparent.
$\overline{SDOLE}$	I	**System Data Output Latch Enable:** latches data in the SD output latch and the SD checkbit latch on the LOW-to-HIGH transition of $\overline{SDOLE}$. The latch is transparent when $\overline{SDOLE}$ is LOW.
SDILE	I	**System Data Input Latch Enable:** latches SD in the SD input latch on the HIGH-to-LOW transition. When SDILE is HIGH, the SD input latch is transparent.
WBSEL	I	**Write FIFO Select:** when HIGH, the write FIFO is selected. When WBSEL is LOW, the SD input latch is selected.
$\overline{WBEN}$	I	**Write FIFO Enable:** when LOW, allows SD data to be written to the write FIFO on the SCLK rising edge.
$\overline{WBREN}$	I	**Write FIFO Read Enable:** when LOW, allows data to be read from the the write FIFO on MCLK rising edge.
RS_{0-1}	I	**Reset and Select pins** (read and write FIFO FIFOs) RS_1 RS_0 Function 0 0 Reset 16-deep FIFO or first 8-deep FIFO 0 1 Reset second 8-deep FIFO 1 0 Select 16-deep FIFO or first 8-deep FIFO 1 1 Select second 8-deep FIFO

2617 tbl 01

PIN DESCRIPTION (Continued)

Pin Name	I/O	Description
RBSEL	I	**Read FIFO Select:** when HIGH, read FIFO is selected (data goes through read FIFO, not MD output latch). When LOW, the MD output latch is selected.
$\overline{\text{RBEN}}$	I	**Read FIFO Enable:** when LOW, allows data to be written into the read FIFO on the LOW-to-HIGH transition of the memory clock.
$\overline{\text{RBREN}}$	I	**Read FIFO Enable:** when LOW, allows data to be read from the read FIFO on the LOW-to-HIGH transition of SCLK
$\overline{\text{CBSEL}}$	I	**Checkbit Select:** Controls the CBSYN output buffer. When HIGH, the buffer is enabled. When CBSEL is LOW, $\overline{\text{MOE}}$ controls the buffer.
$\overline{\text{MEN}}$	I	**Mode Enable Input:** when LOW, data on the SD bus is loaded into the EDC mode register on the LOW-to-HIGH transition of the SCLK. This pin must be held LOW for the entire SCLK HIGH period, as shown in Figure 8.
Clock Inputs		
MCLK	I	**Memory Clock:** on the LOW-to-HIGH transition of MCLK, memory data is written to the read FIFO when $\overline{\text{RBEN}}$ is LOW. Data is read from the write FIFO when $\overline{\text{WBREN}}$ is LOW, on the LOW-to-HIGH transition of MCLK.
SCLK	I	**System Clock:** on the LOW-to-HIGH transition of the SCLK, data is read from the read FIFO when $\overline{\text{RBREN}}$ is LOW. Data on the system data bus is written into the write FIFO when $\overline{\text{WBEN}}$ is LOW on the LOW-to-HIGH transition of SCLK. Clocks data into mode register when $\overline{\text{MEN}}$ is LOW.
SYNCLK	I	**SYNdrome CLocK:** Used to load diagnostic registers. When an error occurs, Error Counter is incremented on the rising SYNCLK edge (up to 15 errors). On the first error after a diagnostic reset, SYNCLK rising edge clocks data into Check Bit, Syndrome, Error Type and Error Data registers. One of the syndrome registers has new data clocked in on every SYNCLK rising edge.
Status Outputs		
$\overline{\text{WBEF}}$	O	**Write FIFO Empty Flag:** when LOW, indicates that the write FIFO is empty. After a reset, the $\overline{\text{WBEF}}$ goes LOW.
$\overline{\text{WBFF}}$	O	**Write FIFO Full Flag:** when LOW, indicates that the write FIFO is full. After a reset, $\overline{\text{WBFF}}$ goes HIGH.
$\overline{\text{RBEF}}$	O	**Read FIFO Empty Flag:** when LOW, indicates that the read FIFO is empty. After a reset, the $\overline{\text{RBEF}}$ goes LOW.
$\overline{\text{RBHF}}$	O	**Read FIFO Half-full Flag:** when LOW, indicates that there are eight or more data words (in the 16-deep configuration) or four or more data words (in the dual 8-deep configuration) in the read FIFO. The flag will return HIGH when less than eight (or four) data words are in the FIFO.
$\overline{\text{RBFF}}$	O	**Read FIFO Full Flag:** when LOW, indicates that the read FIFO is full. After a reset, $\overline{\text{RBFF}}$ goes HIGH.
$\overline{\text{ERR}}$	O	**Error Flag:** when $\overline{\text{ERR}}$ is LOW, a data error is indicated. The $\overline{\text{ERR}}$ is not latched internally.
$\overline{\text{MERR}}$	O	**Multiple Error Flag:** when $\overline{\text{MERR}}$ is LOW, a multiple data error is indicated. The $\overline{\text{MERR}}$ is not latched internally.
$\overline{\text{PERR}}$	O	**Parity Error Flag:** when LOW, indicates a parity error on the system data bus input.
Power Supply		
Vcc	P	Power Supply Voltage, +5 volts.
GND	P	Ground.

2617 tbl 02

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DETAILED DESCRIPTION —

64-BIT MODIFIED HAMMING CODE - CHECKBIT ENCODING CHART(1, 2)

Generated Checkbits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	Even (XOR)		X	X	X		X			X	X		X			X	
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)	X	X	X	X	X	X	X	X								
CB7	Even (XOR)	X	X	X	X	X	X	X	X								

2617 tbl 03

Generated Checkbits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CB0	Even (XOR)		X	X	X		X			X	X		X			X	
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)									X	X	X	X	X	X	X	X
CB7	Even (XOR)									X	X	X	X	X	X	X	X

2617 tbl 04

Generated Checkbits	Parity	Participating Data Bits															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CB0	Even (XOR)	X				X		X	X			X		X	X		X
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)	X	X	X	X	X	X	X	X								
CB7	Even (XOR)									X	X	X	X	X	X	X	X

2617 tbl 05

Generated Checkbits	Parity	Participating Data Bits															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CB0	Even (XOR)	X				X		X	X			X		X	X		X
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)									X	X	X	X	X	X	X	X
CB7	Even (XOR)	X	X	X	X	X	X	X	X								

2617 tbl 06

NOTES:

1. The table indicates the data bits participating in the checkbit generation. For example, checkbit CB0 is the Exclusive-OR function of the 64 data input bits marked with an X.
2. The checkbit is generated as either an XOR or an XNOR of the 64 data bits noted by an "X" in the table.

DETAILED DESCRIPTION —

64-BIT SYNDROME DECODE TO BIT-IN-ERROR(1)

				HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
				S7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
				S6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
			Syndrome	S5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
			Bits	S4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HEX	S3	S2	S1	S0																
0	0	0	0	0	*	C4	C5	T	C6	T	T	62	C7	T	T	46	T	M	M	T
1	0	0	0	1	C0	T	T	14	T	M	M	T	T	M	M	T	M	T	T	30
2	0	0	1	0	C1	T	T	M	T	34	56	T	T	50	40	T	M	T	T	M
3	0	0	1	1	T	18	8	T	M	T	T	M	M	T	T	M	T	2	24	T
4	0	1	0	0	C2	T	T	15	T	35	57	T	T	51	41	T	M	T	T	31
5	0	1	0	1	T	19	9	T	M	T	T	63	M	T	T	47	T	3	25	T
6	0	1	1	0	T	20	10	T	M	T	T	M	M	T	T	M	T	4	26	T
7	0	1	1	1	M	T	T	M	T	36	58	T	T	52	42	T	M	T	T	M
8	1	0	0	0	C3	T	T	M	T	37	59	T	T	53	43	T	M	T	T	M
9	1	0	0	1	T	21	11	T	M	T	T	M	M	T	T	M	T	5	27	T
A	1	0	1	0	T	22	12	T	33	T	T	M	49	T	T	M	T	6	28	T
B	1	0	1	1	17	T	T	M	T	38	60	T	T	54	44	T	1	T	T	M
C	1	1	0	0	T	23	13	T	M	T	T	M	M	T	T	M	T	7	29	T
D	1	1	0	1	M	T	T	M	T	39	61	T	T	55	45	T	M	T	T	M
E	1	1	1	0	16	T	T	M	T	M	M	T	T	M	M	T	0	T	T	M
F	1	1	1	1	T	M	M	T	32	T	T	M	48	T	T	M	T	M	M	T

NOTES: 2617 tbl 07

1. The table indicates the decoding of the eight syndrome bits to identify the bit-in-error for a single-bit error, or whether a double or triple-bit error was detected. The all-zero case indicates no error detected.
   * = No errors detected
   # = The number of the single data bit-in-error
   T = Two errors detected
   M = Three or more detected
   C# = The number of the single checkbits in error

IDT49C466 OPERATION

The EDC is involved in two types of operation — memory reads and memory writes. With the IDT49C466, both these can be accomplished by utilizing either of two possible data paths — one incorporating the FIFO and the other without the FIFO. These operations are treated separately below.

Memory Write

The involvement of the EDC in this type of operation is relatively minimal since it does not call for any error checking. It only generates the check bits associated with each 64-bit wide data word. The EDC can be in generate-detect or normal mode for this operation.

When a write operation is performed, it must be ensured that the SD output buffer (enabled by $\overline{SOE}$ and BE_{0-7}) is disabled so that no attempt is made to simultaneously transfer read data onto the System Data (SD) Bus.

When the write FIFO is bypassed (WBSEL LOW), data passes through the SD Latch In. To latch data, the SDILE signal should be pulled LOW. The special case of a partial word write or byte merge is discussed later. Here it is assumed that all 64 bits are being written. Consequently, BE_{0-7} must all be LOW.

The data is fed to the SD Checkbit generator where appropriate checkbits are generated. Both system data and the generated checkbits can be latched by pulling the $\overline{SDOLE}$ signal HIGH. Asserting $\overline{MOE}$ enables the MD output buffer and data is output to the Memory Data (MD) bus. CBSEL (=0) and $\overline{MOE}$(=1) need to be asserted to enable the checkbit output buffer and output these on $CBSYN_{0-7}$.

When the write FIFO is selected (WBSEL = 1), instead of asserting SDILE, $\overline{WBEN}$ is asserted and data is clocked into the write FIFO on the rising edge of SCLK. The $\overline{WBFF}$ is asserted when the FIFO is full. When $\overline{WBREN}$ is asserted, data can be clocked out of the write FIFO on the rising edge of MCLK.

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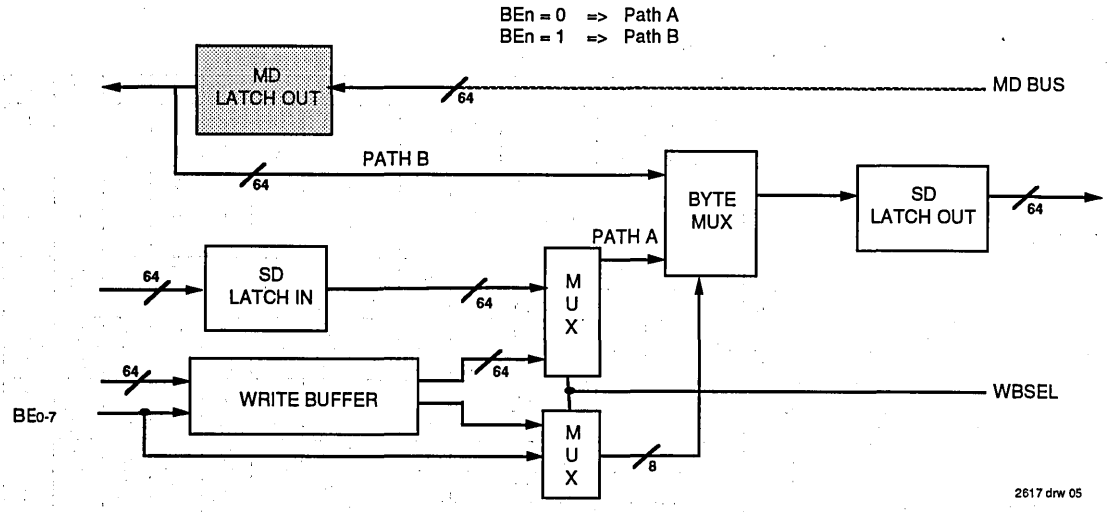

Figure 1. Byte Merge

Memory Read

During a memory read, data and the corresponding input checkbits are read from the MD bus and CBI0-7, respectively. The memory data and CBI may both be latched as they come in (MD Latch In and MD Checkbit latch) by the MDILE signal. Memory data is sent to the MD checkbit generator (where checkbits corresponding to the input data are generated) and to the error correct circuitry. The generated checkbits are X-ORed with the input checkbits to produce the syndrome word. This is sent to the error correction circuitry which generates the corrected data (normal mode). The corrected data is output to the SD bus via either of two data paths. When RBSEL is LOW, data flows through MD Latch Out. Pulling $\overline{\text{MDOLE}}$ HIGH latches this data. The output buffer is enabled by asserting $\overline{\text{SOE}}$ and BE0-7. Corrected data can be written back to memory by enabling the MD output buffer. In order to ensure selection of the write back path (Path B in figure 1) at the byte mux, BEO-7 should be all 1's while WBSEL = 0. If WBSEL = 1, buffered BEO-7 from the output of the write FIFO controls the byte mux.

If the read FIFO is selected (RBSEL HIGH), data is clocked into the FIFO (Read_FIFO Write) when $\overline{\text{RBEN}}$ is LOW, on the rising edge of MCLK. Data is clocked out of the FIFO (Read_FIFO Read) when $\overline{\text{RBREN}}$ is LOW on the rising edge of SCLK.

Clock Skew

A skew between the read and write clocks, as specified by tskew, is recommended. This specification is not a stringent one, in the manner of setup and hold times, but is important in preempting latencies at FIFO boundaries. For example – When a word is written to an empty FIFO, there is a finite delay before the FIFO is recognized as no longer being empty and hence allowing a read from the same FIFO. Similarly when a word is read from a full FIFO, there is a delay before a write can successfully be attempted. The tskew specification accounts for these cases. During cycles other than on full/empty FIFO boundaries, the clock skew is not required and the device functions correctly even when the reads and writes occur simultaneously. If the tskew specification is ignored and SCLK and MCLK were permanently tied together, there is an extra cycle latency in the cases mentioned above. One such case is illustrated in Figure 11.

FIFO Write Latency

The first data written to either of the (read or write) FIFOs, after the FIFO is reset, suffers a single clock latency. Data that is set-up with respect to the first clock is ignored and the data that is set-up with respect to the second clock edge after the reset, is stored as the first data in the FIFO. The empty-flag is deasserted after this second clock edge and 15 more data words (in a 16 deep configuration) can be written to the FIFO after this.

The latency can be reduced or eliminated by providing a "dummy" or "set-up" clock edge (as shown in figure) before the actual write to the FIFO. The dummy write clock can be provided any time after reset and before the next buffer write operation takes place. The latency described here (shown in Figure 9) occurs only after a FIFO reset. In other cases where the FIFO becomes empty there is no such latency.

Partial Word Write/Byte Merge

Writing a word shorter than 64 bits to memory is treated as a special case. The checkbits generated for a data word shorter than 64 bits and written to a particular memory location differ from the checkbits that would be generated by the entire 64-bit data word at the same location. Hence, the byte merge operation requires reading the contents of the memory location to be written to, merging the byte/bytes being written (from SD side) with the other component bytes previously at that memory location (from MD side), generating a checkbit word for this composite word and writing both the composite data word and the generated checkbits to memory. The BEn bits supplied by the user determine the bytes that come from SD and those that come from MD, as illustrated in Figure 1.

EDC Modes

The IDT49C466 has 5 modes of operation. Refer to table below for a description of the modes. The **Error Data Output** mode is useful for memory initialization. On issuing a clear, the Error Data register becomes an 'all-zero-data' source. All diagnostic registers can be cleared in this manner.

In **Checkbit Injection mode**, the MD Checkbit Latch is loaded with data from the System Bus. This serves to verify the functioning of the EDC. Any discrepancy between the injected checkbits and generated checkbits should result in assertion of the $\overline{ERR}$ or $\overline{MERR}$ signals.

These modes, and certain other features such as clear, buffer configuration, etc., can be selected by appropriately loading the Mode Register. The Mode Register can be written to by asserting $\overline{MEN}$. Then SD_{0-15} is clocked into the mode register on the rising edge of SCLK.

MODE REGISTER CONFIGURATION

15 7	6	5	4	3	2 0
UNUSED	RMODE	PSEL	RWBD	CLEAR	EDCM0-2

EDCM2	EDCM1	EDCM0	OPERATION
0	0	0	ERROR-DATA OUTPUT MODE
0	0	1	DIAGNOSTIC-OUTPUT MODE
0	1	0	GENERATE-DETECT MODE
0	1	1	NORMAL MODE
1	X	X	CHECKBIT-INJECTION MODE

RMODE	OPERATION
0	NOP
1	READ MODE REGISTER ON SD BUS

RWBD	OPERATION
0	DUAL FIFOS (8)
1	SINGLE FIFO (16)

CLEAR	OPERATION
0	NOP
1	CLEAR ALL DIAGNOSTIC REGISTERS

PSEL	OPERATION
0	EVEN PARITY
1	ODD PARITY

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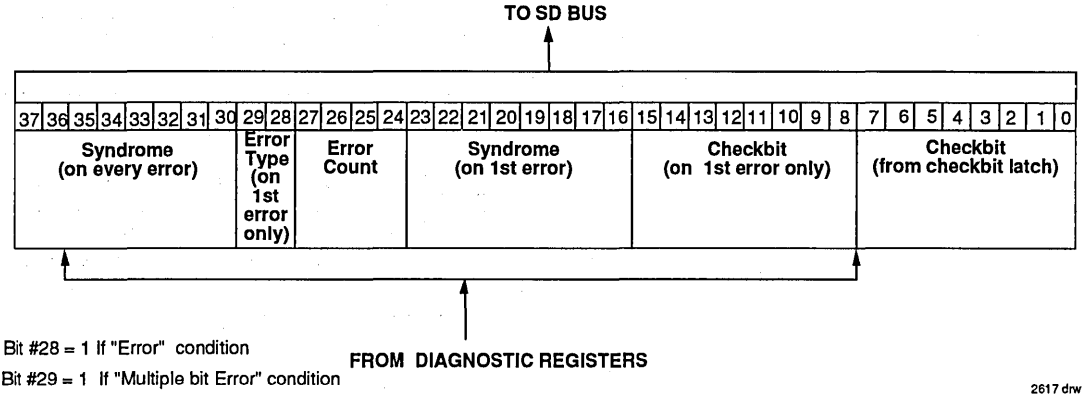
OPERATING MODE DESCRIPTION

Mode	Description
MODE 0	**Error-Data Output Mode:** This mode allows the uncorrected data captured from an error event by the Error-Data Register to be read by the system for diagnostic purposes. The Error-Data Register is cleared by setting the mode register "clear"-bit.
MODE 1	**Diagnostic-Output Mode:** In this mode, contents of latch and five internal registers are read by the system for diagnostic and error logging purposes. Internal data paths allow output from the CBI LATCH to be read directly by the system bus for diagnostic purposes. The contents of the internal diagnostic checkbit register, syndrome registers, error count register and error-type register are also output on the SD bus.
MODE 2	**Generate-Detect Mode:** (Detect-Only) The EDC performs checkbit generation during a memory write, and performs error detection only during a memory read.
MODE 3	**Normal Mode:** The EDC performs checkbit generation during memory writes and error detection and correction during memory reads.
MODE 4	**Checkbit-Injection Mode:** In this mode, the checkbit latch is loaded with desired 8-bit data from the SD bus.This eight bit data passes through SD Latch in or write FIFO to the MD check bit latch. By inserting various checkbit values, correct functioning of the EDC can be verified "on-board". The rest of the operation is similar to regular memory reads. The EDC compares the injected checkbits against the internally generated checkbits. Any discrepancy in the injected checkbits and the internally generated checkbits will cause the $\overline{ERR}$ / $\overline{MERR}$ to go LOW.

2617 tbl 08

8

DIAGNOSTIC OUTPUT DATA FORMAT



* Bit #28 = 1 If "Error" condition
Bit #29 = 1 If "Multiple bit Error" condition

2617 drw 07

Diagnostics

The diagnostic ability of the IDT49C466 rests on a set of 6 registers that provide error logging information. These include the checkbit register, error count register, error type register, 2 syndrome registers and the error data register. Data is clocked into each of these registers by SYNCLK. The error data register, checkbit register, error type register and one of the syndrome registers are reloaded only in the case of the first error after a clear. The other syndrome register and the error count register are reloaded on every error condition SYNCLK edge. The contents of the Error Data register can be read only in Error Data Output mode. The contents of the other diagnostic registers as well as the checkbit latch can be read in Diagnostic Output mode.

Parity

The IDT49C466 provides a parity check and generation facility. On a memory read the EDC generates parity bits for each data word and outputs the parity byte on the parity bus, P0-7. During a memory write, parity is checked by comparing the parity bits input on P0-7 and the parity bits generated from the input data word. A discrepancy between these two causes the $\overline{PERR}$ pin to be asserted.

DIAG. REGISTER	LOADED BY	CONDITION	OUTPUT
CHECKBIT	SYNCLK↑	ONLY ON 1st ERROR	SD8-15
SYNDROME (On 1st ERR)	SYNCLK↑	ONLY ON 1st ERROR	SD16-23
ERR CNT	SYNCLK↑	ON EVERY ERROR (Up to 15 ERRORS)	SD24-27
ERR TYPE	SYNCLK↑	ONLY ON 1st ERROR	SD28-29
SYNDROME (On every ERROR)	SYNCLK↑	ON EVERY ERROR	SD30-37

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{CC}	Power Supply Voltage	–0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to VCC + 0.5	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	30	mA

NOTE: 2617 tbl 09

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Ratings for extended periods of time may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	PGA	5	pF
			PQFP	5	
C_{OUT}	Output Capacitance	V_{OUT} = 0V	PGA	7	pF
			PQFP	7	

NOTE: 2617 tbl 10

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

The following conditions apply unless otherwise specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%;

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level[4]	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level[4]	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7V		—	0.1	5.0	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.5V		—	-0.1	–5.0	µA
I_{OZ}	Off State (Hi-Z)	V_{CC} = Max.	V_O = 0V	—	-0.1	–10	µA
	Output Current		V_O = 3V	—	0.1	10	
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT}= 0V		–20	—	–100	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –2mA	2.4	3.6	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8mA	—	0.3	0.5	V
V_H	Input Hysteresis on input control lines			—	200	—	mV

NOTES: 2617 tbl 11

1. For conditions shown as min. or max., use appropriate Vcc value.
2. Typical values are at Vcc = 5.0V, +25°C ambient temperature.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Con't)

The following conditions apply unless otherwise specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions[1]	Min.	Typ.[2]	Max.	Unit
I_{CCQC}	Quiescent Power Supply Current	V_{IN} = V_{CC}, or V_{IN} = GND V_{CC} = Max.	—	3.0	15	mA
I_{CCQT}	Quiescent Power Supply Current TTL Input Levels	V_{IN} = 3.4V V_{CC} = Max.	—	0.3	1	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{IN} = V_{CC}, or V_{IN} = GND V_{CC} = Max. f = 10MHz Correct Mode	—	—	100	mA

NOTES: 2617 tbl 12

1. For conditions shown as Min. or Max., use appropriate Vcc value.
2. Typical values are at Vcc = 5.0V, +25°C ambient temperature.

8

AC PARAMETERS
PROPAGATION DELAY TIMES

Number	Parameter	Description		Max.	Unit	Refer to Timing Diagram Figure
		From Input[1]	To Output			
GENERATE (WRITE) PARAMETERS						
Without Write FIFO:						
1	t_{BC}	BEn	CBSYN (chkbit)	20	ns	
2	t_{BM}	BEn	MDOUT	16	ns	
3	t_{PPE}	Pxin	PERR	10	ns	
4	t_{SC}	SDin	CBSYN (chkbit)	22	ns	
5	t_{SM}	SDin	MDout	22	ns	
6	t_{SPE}	SDin	$\overline{PERR}$	16	ns	
With Write FIFO:						
7	t_{MC}	MCLK (Lo-Hi)	CBSYN (chkbit)	25	ns	4
8	t_{MMD}	MCLK (Lo-Hi)	MDout	25	ns	4
9	t_{WBSEL}	WBSEL	MDout	18	ns	
DETECT (READ) PARAMETERS						
Without Read FIFO:						
10	t_{WYC}	SYNCLK (Lo-Hi)	CBSYN (syndr)	16	ns	
11	t_{ME}	MDin	$\overline{ERR}$	20	ns	
12	t_{MME}	MDin	$\overline{MERR}$	22	ns	
13	t_{CE}	CBI	$\overline{ERR}$	13	ns	
14	t_{CME}	CBI	$\overline{MERR}$	13	ns	
With Read FIFO:						
15	t_{SSD}	SCLK (Lo-Hi)	SDout	22	ns	6
16	t_{RBSEL}	RBSEL	SDout	18	ns	
CORRECT (READ) PARAMETERS						
Without Read FIFO:						
17	t_{CS}	CBI	SDout	20	ns	
18	t_{MP}	MDin	Pxout	22	ns	
19	t_{MS}	MDin	SDout	22	ns	
With Read FIFO:						
20	t_{SP}	SCLK (Lo-Hi)	Pxout	22	ns	

2617 tbl 13

NOTES:
1. (Lo-Hi) indicates LOW-to-HIGH transition and vice versa.

PROPAGATION DELAY TIMES FROM LATCH ENABLES

Number	Parameter	Description		Max.	Unit	Refer to Timing Diagram
		From Input[1]	To Output			Figure
21	tMLE	MDILE (Lo-Hi)	$\overline{ERR}$	16	ns	
22	tMLME	MDILE (Lo-Hi)	$\overline{MERR}$	18	ns	
23	tMLP	MDILE (Lo-Hi)	Px	24	ns	
24	tMLS	MDILE (Lo-Hi)	SDout	22	ns	
25	tMOLS	$\overline{MDOLE}$ (Hi-Lo)	SDout	18	ns	
26	tMOLP	$\overline{MDOLE}$ (Hi-Lo)	Px	18	ns	
27	tSLC	SDILE (Lo-Hi)	CBSYN (chkbit)	20	ns	
28	tSLM	SDILE (Lo-Hi)	MDout	20	ns	
29	tSOLC	$\overline{SDOLE}$ (Hi-Lo)	CBSYN (chkbit)	12	ns	
30	tSOLM	$\overline{SDOLE}$ (Hi-Lo)	MDout	15	ns	

NOTE: 2617 tbl 14

1. (Lo-Hi) indicates LOW-to-HIGH transition and vice versa.

R/W FIFO TIMES

Number	Parameter	Description		Min.	Max.	Unit	Refer to Timing Diagram
		From Input[1]	To Output[1]				Figure
31	tRSF	RS1 (Hi-Lo)	$\overline{EF}$ (Hi-Lo)/$\overline{FF}$ (Lo-Hi)	—	16	ns	7, 10, 11
32	tSKEW1	RCLK (Lo-Hi) (SCLK or MCLK)	WCLK (Lo-Hi) (SCLK or MCLK)	10	—	ns	3, 5
33	tSKEW2	WCLK (Lo-Hi) (SCLK or MCLK)	RCLK (Lo-Hi) (SCLK or MCLK)	10	—	ns	4, 6
34	tEF	R/WCLK (Lo-Hi) (SCLK or MCLK)	$\overline{EF}$	—	15	ns	4, 6, 10, 11
35	tFF	R/WCLK (Lo-Hi) (SCLK or MCLK)	$\overline{FF}$	—	15	ns	3, 5

NOTE: 2617 tbl 15

1. (Lo-Hi) indicates LOW-to-HIGH transition and vice versa.

8

BYTE MERGE TIMES

Number	Parameter	Description		Max.	Unit	Refer to Timing Diagram
		From[1]	To			Figure
36	t_{SCM}	SCLK (Lo-Hi)	MDout	25	ns	
37	t_{MDM}	$\overline{MDOLE}$ (Hi-Lo)	MDout	18	ns	9
38	t_{RBM}	RBSEL	MDout	23	ns	
39	t_{SDM}	SDILE (Lo-Hi))	MDout	18	ns	9

NOTES:
1. (Lo-Hi) indicates LOW-to-HIGH transition and vice versa.

2617 tbl 16

ENABLE AND DISABLE TIMES

Number	Parameter	Description				Min.	Max.	Unit	Refer to Timing Diagram
		From Input		To Output[1,2]					Figure
41	t_{BESZx}	BEN =	High	SDout	*	—	22	ns	6
42	t_{BESxZ}		Low		Hi-Z	—	22		
43	t_{BEPZx}	BEN =	High	Pout	*	—	15	ns	6
44	t_{BEPxZ}		Low		Hi-Z	—	15		
84	t_{SEPZx}	$\overline{SOE}$ =	Low	Pout	*	—	14	ns	
85	t_{SEPxZ}		High		Hi-Z	—	14		
45	t_{CECZx}	$\overline{MOE}$ =	Low	CBSYN	*	—	10	ns	4
46	t_{CECxZ}		High		Hi-Z	—	10		
47	t_{MEMZx}	$\overline{MOE}$ =	Low	MDout	*	—	32	ns	4, 9
48	t_{MEMxZ}		High		Hi-Z	—	18		
49	t_{SESZx}	$\overline{SOE}$ =	Low	SDout	*	—	16	ns	6
50	t_{SESxZ}		High		Hi-Z	—	20		

NOTES:
1. (High-Z) indicates high impedence.
2. * indicates delay to both edges.

2617 tbl 17

SET-UP AND HOLD TIMES

Number	Parameter	Description			Min.	Unit	Refer to Timing Diagram Figure
		From Input	To Input	edge[1]			
51	t_{CMLS}	CBI Set-up	before MDILE =	Hi-Lo	2	ns	5
52	t_{CMLH}	CBI Hold	after MDILE =	Hi-Lo	6	ns	5
53	t_{MMLS}	MDIN Set-up	before MDILE =	Hi-Lo	2	ns	5
54	t_{MMLH}	MDIN Hold	after MDILE =	Hi-Lo	6	ns	5
55	t_{CMOLS}	CBI Set-up	before $\overline{\text{MDOLE}}$ =	Lo-Hi	10	ns	
56	t_{CMOLH}	CBI Hold	after $\overline{\text{MDOLE}}$ =	Lo-Hi	2	ns	
57	t_{MMOLS}	MDIN Set-up	before $\overline{\text{MDOLE}}$ =	Lo-Hi	10	ns	
58	t_{MMOLH}	MDIN Hold	after $\overline{\text{MDOLE}}$ =	Lo-Hi	4	ns	
59	t_{MMCS}	MDIN Set-up	before MCLK =	Lo-Hi	10	ns	5
60	t_{MMCH}	MDIN Hold	after MCLK =	Lo-Hi	4	ns	5
61	t_{SSLS}	SDIN Set-up	before SDILE =	Hi-Lo	5	ns	
62	t_{SSLH}	SDIN Hold	after SDILE =	Hi-Lo	3	ns	
63	t_{SSCS}	SDIN Set-up	before SCLK	Lo-Hi	2	ns	3, 10, 11
64	t_{SSCH}	SDIN Hold	after SCLK	Lo-Hi	6	ns	3, 10, 11
86	t_{SSOLS}	SDIN Set-up	before $\overline{\text{SDOLE}}$ =	Lo-Hi	8	ns	
87	t_{SSOLH}	SDIN Hold	after $\overline{\text{SDOLE}}$ =	Lo-Hi	0	ns	
65	t_{SCSD}	SCLK (Lo-Hi)	before $\overline{\text{SDOLE}}$ =	Lo-Hi	14	ns	(Write back path)
89	t_{MCSD}	MCLK (Lo-Hi)	before $\overline{\text{SDOLE}}$ =	Lo-Hi	14	ns	(Write path) 4
66	t_{ENS}	R/W FIFO Enable Set-up	before S/M CLK =	Lo-Hi	4	ns	3, 4, 5, 6, 10
67	t_{ENH}	R/W FIFO Enable Hold	after S/M CLK =	Lo-Hi	4	ns	3, 4, 5, 6
70	t_{RSS}	RS1 (Lo-Hi)	R/WCLK =	Lo-Hi	6	ns	7
71	t_{MODS}	Mode Data Set-up	before SCLK =	Lo-Hi	4	ns	8
72	t_{MODH}	Mode Data Hold	after SCLK =	Lo-Hi	4	ns	8
73	t_{MENS}	Mode Enable Set-up	before SCLK =	Lo-Hi	4	ns	8
74	t_{MENH}	Mode Enable Hold	after SCLK =	Lo-Hi	4	ns	8
90	t_{MSD}	MDIN	$\overline{\text{SDOLE}}$ =	Hi-Lo	22	ns	
DIAGNOSTIC SET-UP AND HOLD TIMES							
75	t_{CSCS}	CBI Set-up	before SYNCLK =	HIGH	4	ns	
76	t_{MSCS}	MDIN Set-up			4	ns	
77	t_{MLSCS}	MDILE Set-up = Lo-Hi			12	ns	

NOTE:
1. (Lo-Hi) indicates LOW-to-HIGH transition and vice versa.

2617 tbl 18

MINIMUM PULSE WIDTH

Number	Parameter	Description			Min.	Unit	Refer to Timing Diagram Figure
		From Input		Condition			
78	t_{RS}	Min. RS1 LOW time	to reset buffers	—	6	ns	
79	t_{MLE}	Min. MDILE HIGH time	to strobe new data	MD, CBI = Valid	6	ns	
80	t_{MDOLE}	Min. $\overline{\text{MDOLE}}$ LOW time	to strobe new data	—	6	ns	
81	t_{SLE}	Min. SDILE HIGH time	to strobe new data	SD = Valid	6	ns	
82	t_{CLK}	Min. S/MCLK HIGH time	to clock in new data	EN signal LOW	6	ns	
83	t_{SYNCLK}	Min. SYNCLK HIGH time	to clock in new data	—	6	ns	
88	t_{SDOLE}	Min. $\overline{\text{SDOLE}}$ LOW time	to clock in new data	—	6	ns	

2617 tbl 19

8

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Out Load	See Figure 14

2617 tbl 21

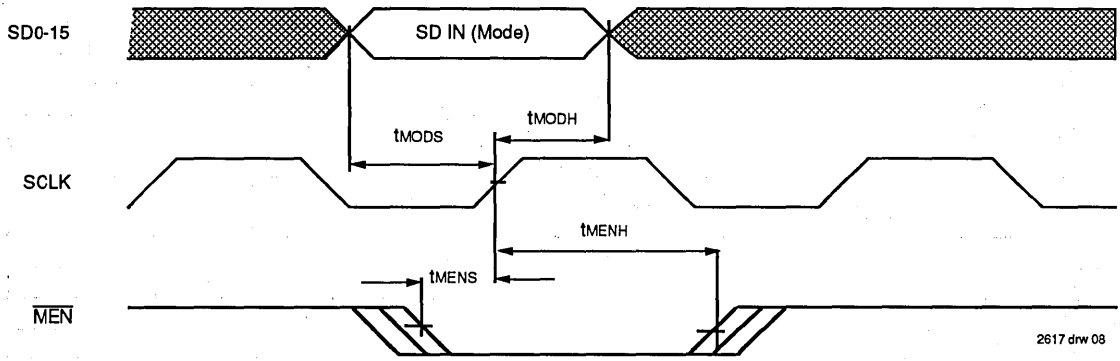


Figure 2. Mode Enable Timing

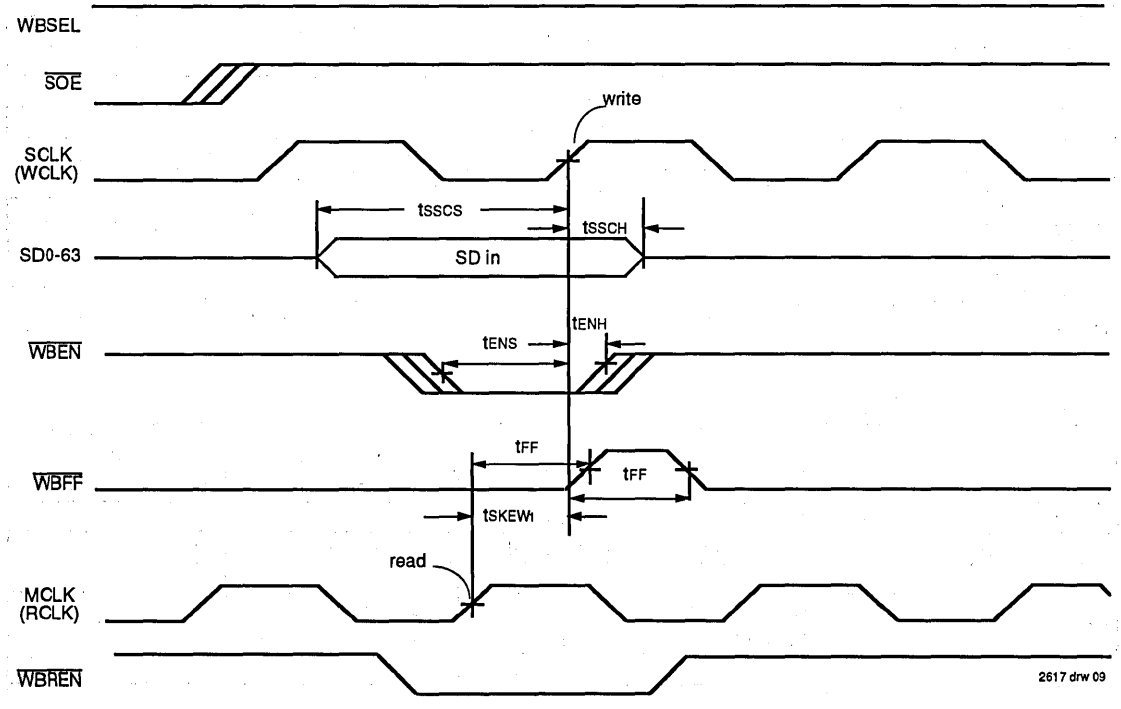


Figure 3. Write FIFO Timing Table (Write Cycle)

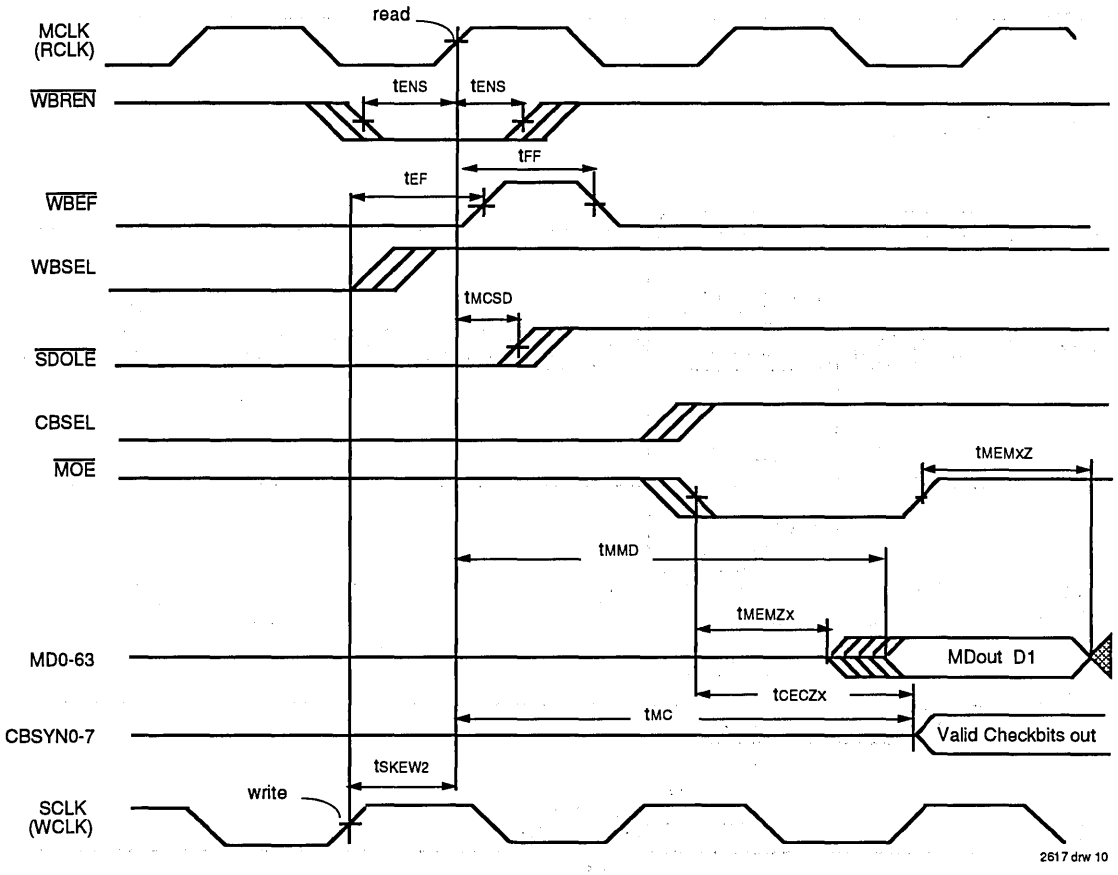


Figure 4. Write FIFO Read and Checkbit Generate Timing (Write Cycle)

8

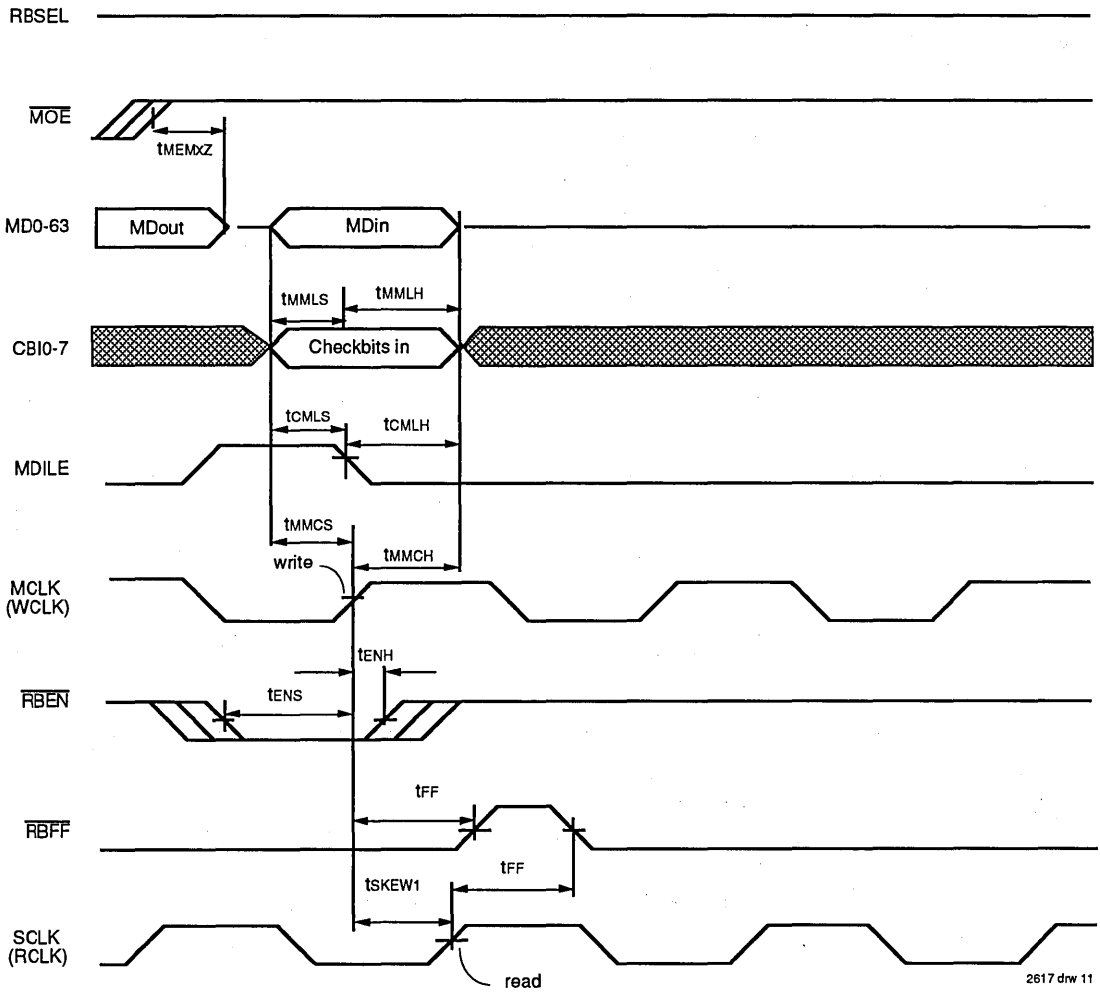


Figure 5. Read FIFO Write Timing (Read Cycle)

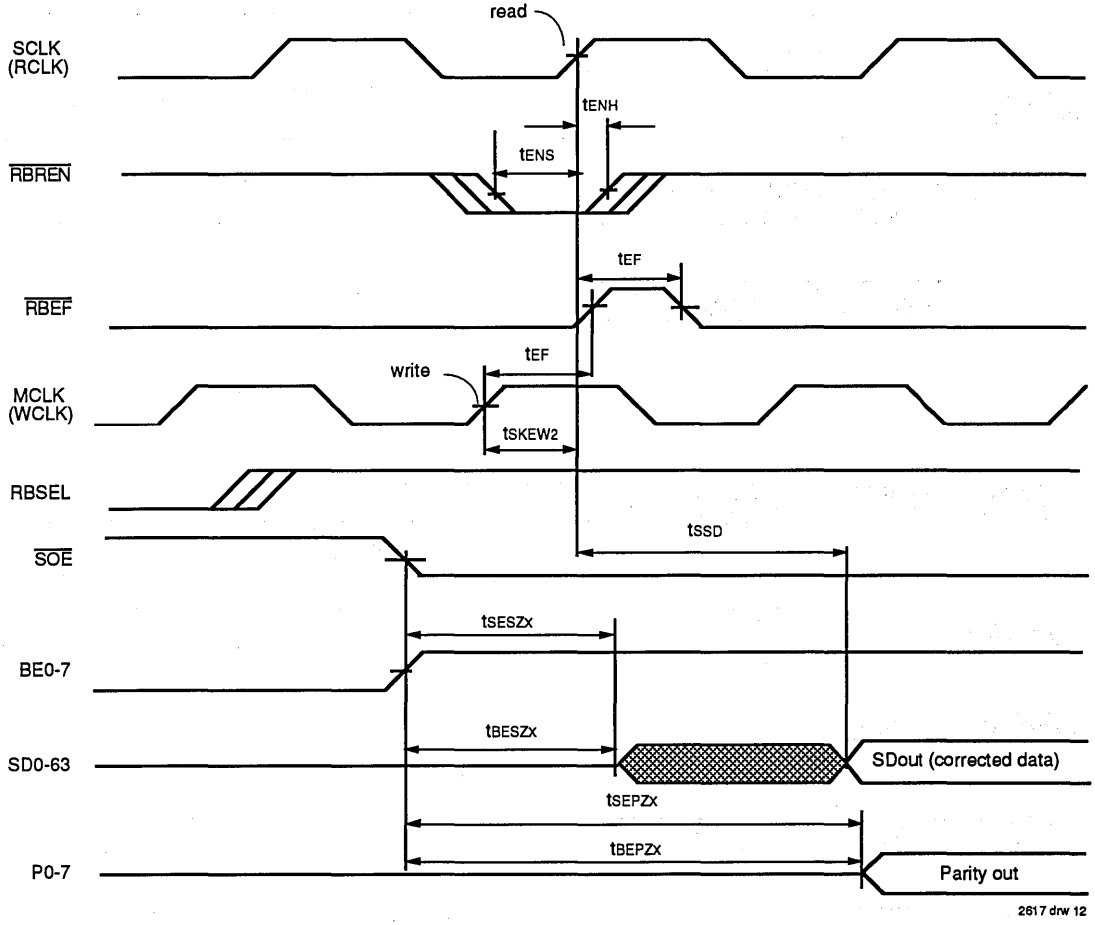


Figure 6. Read FIFO Read Timing (Read Cycle)

8

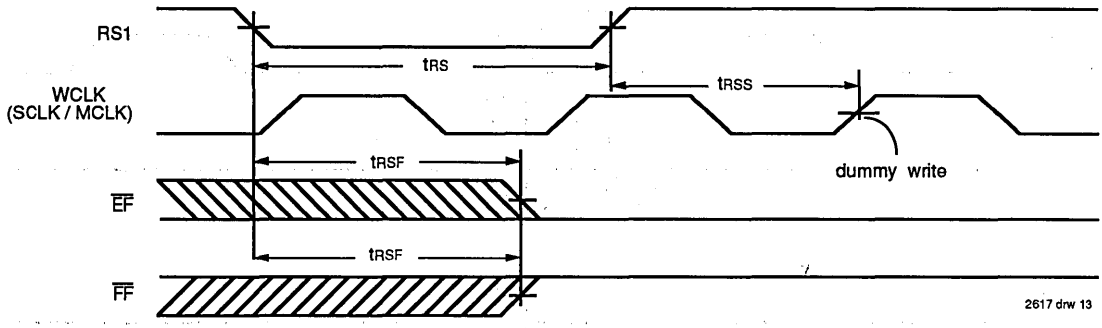


Figure 7. FIFO Reset Timing

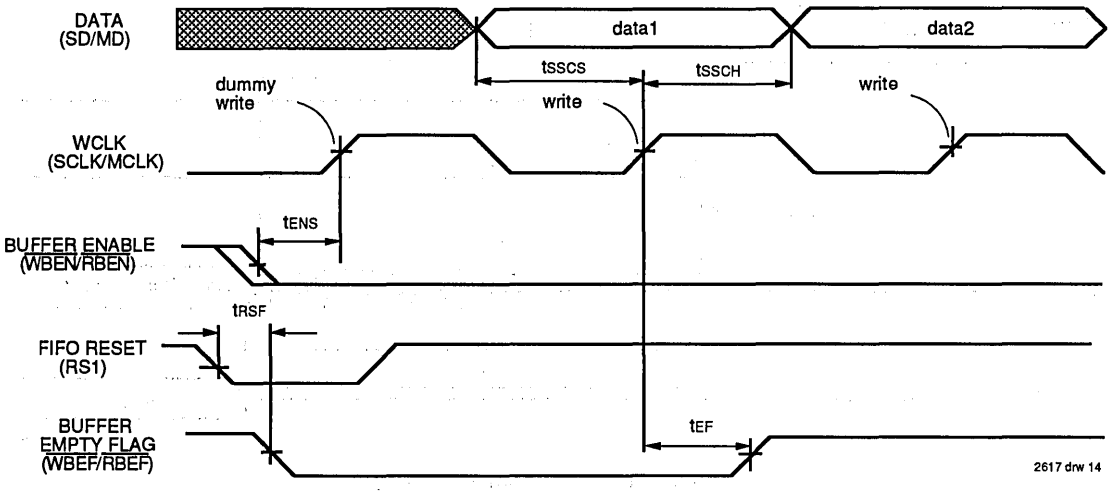


Figure 8. FIFO Write Latency Timing

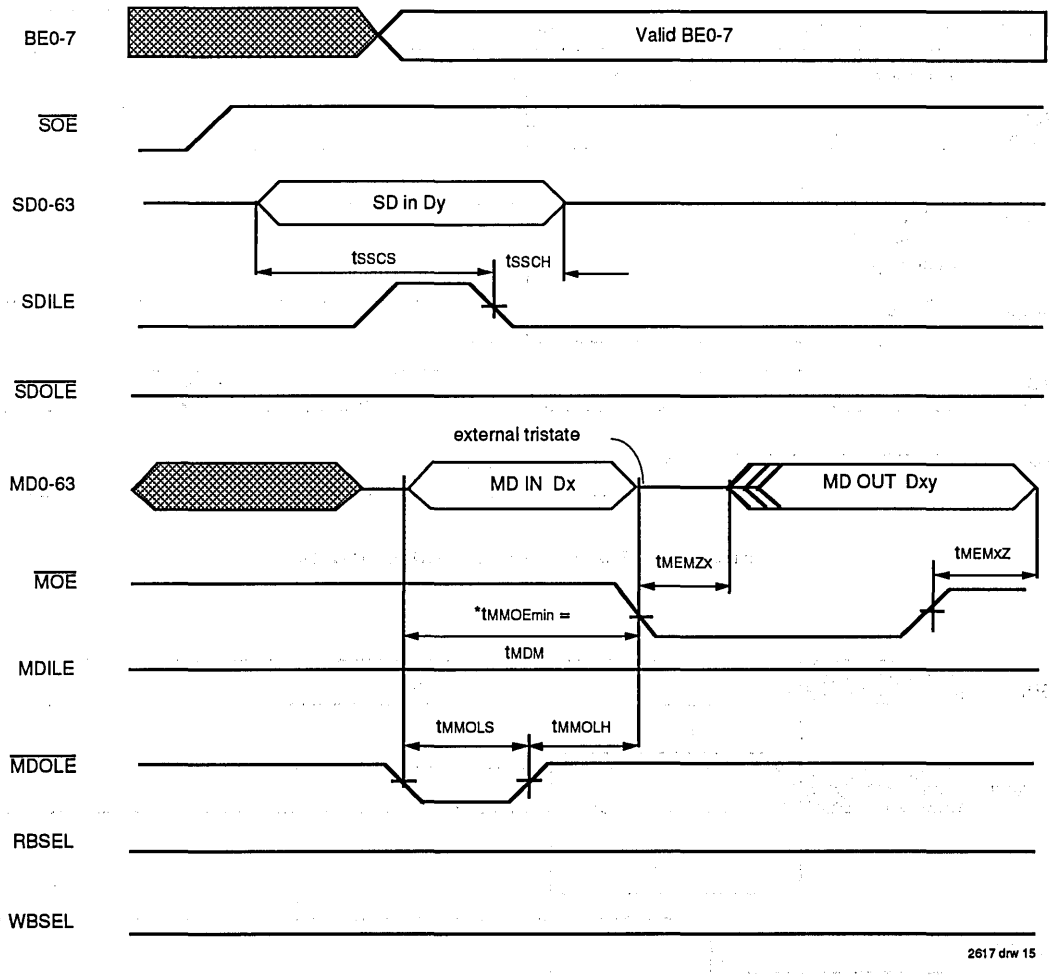


Figure 9. Partial Word Write/Byte Merge Timing

NOTE:
1. t_{MMOE} is not a propagation delay. For partial word write operations t_{MDM} may be taken as the minimum value for t_{MMOE}.

8

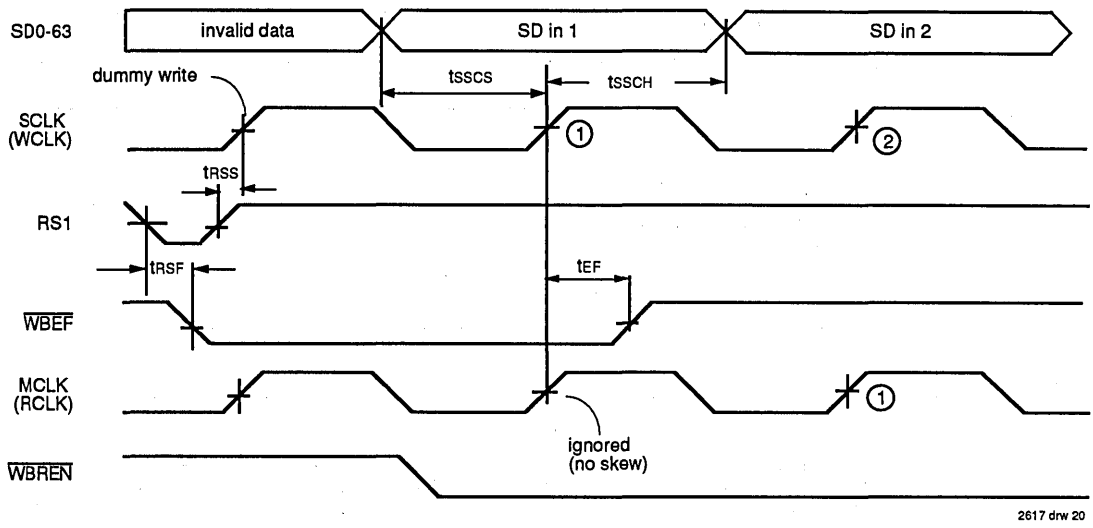


Figure 10. Write FIFO Write Timing with Clock Skew Violation

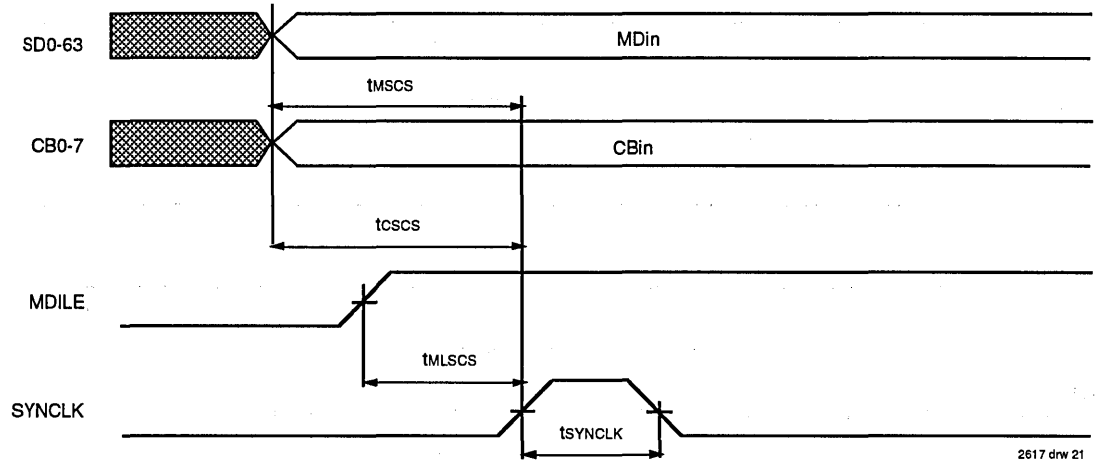


Figure 11. Diagnostic Timing

INPUT/OUTPUT INTERFACE CIRCUITS

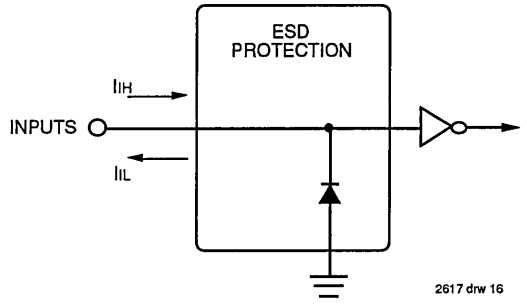


Figure 12. Input Structure (All Inputs)

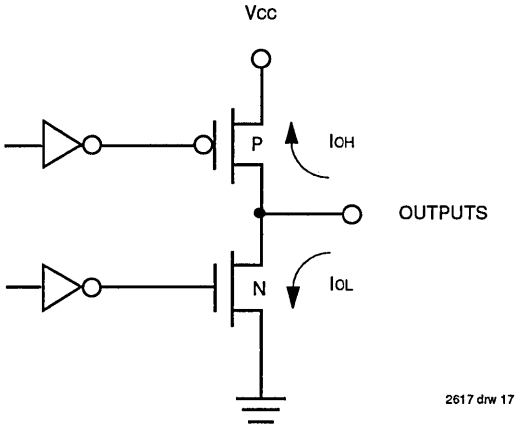
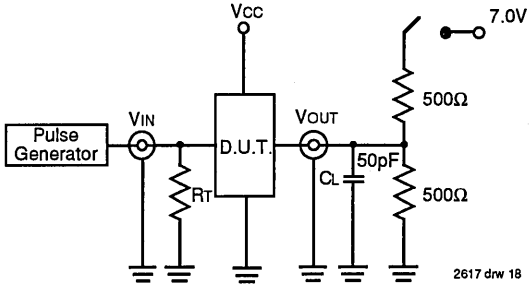


Figure 13. Output Structure



DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

Figure 14. AC Test Circuit

SWITCH POSITION

Test	Switch
Disable Low Enable Low	Closed
All Other Tests	Open

2617 tbl 20

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