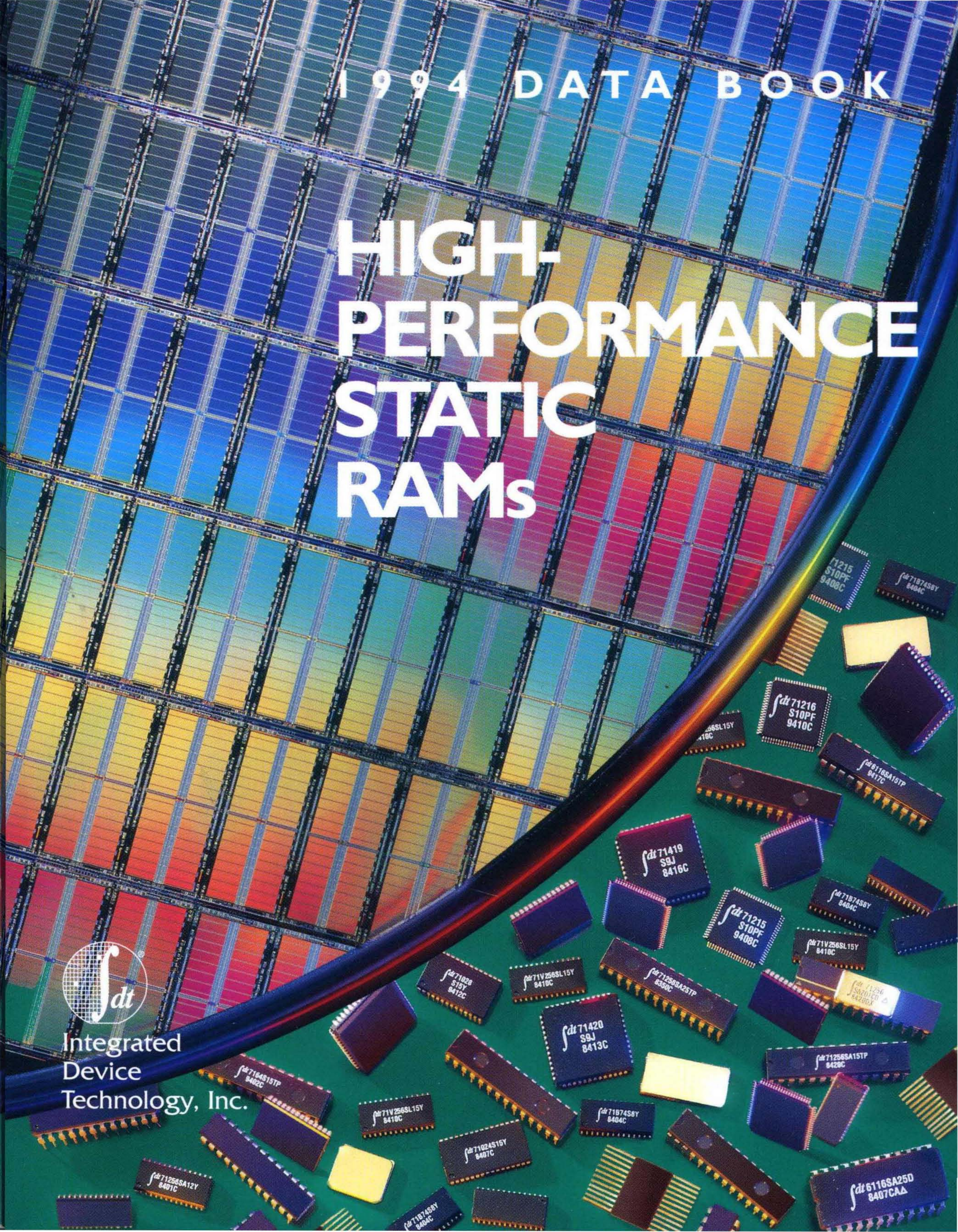
1994 DATA BOOK

HIGH-PERFORMANCE STATIC RAMs



Integrated Device Technology, Inc.

994
DATA
BOOK
HIGH-PERFORMANCE STATIC RAMs
Integrated Device Technology

Integrated Device Technology, Inc.

1994
HIGH-PERFORMANCE SRAM
DATA BOOK

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ANNOUNCING

IDT's New FAX-On-Demand Literature Request Service

Tired of waiting days or weeks for technical information you want *right now*?

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Call (408) 492-8391

For an index of current information:

Request document #1000

Individual document request numbers, product families, IDT product part numbers, descriptive titles, and page counts for each document are provided on the indices for your convenience. You may request up to 3 documents per phone call.

Integrated Device Technology, Inc.

VALUE THROUGH PERFORMANCE

CONTENTS OVERVIEW

For ease of use for our customers, Integrated Device Technology provides four separate data books: High-Performance Logic, Specialized Memories and Modules, RISC and RISC SubSystems, and High-Performance Static RAM.

IDT's 1994 High-Performance SRAM Data Book is comprised of both new product data sheets and revised data sheets on existing products. The new products include high-speed, high-density BiCMOS devices, specialty SRAM products, and true 3.3V high-performance SRAMs. The existing product data sheet revisions upgrade and correct the existing specification to more accurately reflect device improvements that have been made over time. Also included is a current packaging section for the products included in this book.

The SRAM Data Book's Table of Contents is a listing of the products contained in this data book only (in the past, we have also included products that appeared in other IDT data books). The number at the bottom center of the page denotes the section number and the sequence of the data sheet within that section, (i.e., 5.5 would be the fifth data sheet in the fifth section). The number in the lower right-hand corner is the page number for that particular data sheet.

The data sheets are organized in eight sections (16K, 64K, 256K, 1M, 3.3V, CacheRAMs, Cache Tags, and Cache Controller Product). Each section is then ordered by total number of bits (low to high), device word width (narrow to wide), and performance (slow to fast).

Integrated Device Technology, Inc. is a recognized leader in high-speed CMOS and BiCMOS technology and produces a broad line of products. This enables us to provide complete CMOS and BiCMOS solutions to designers of high-performance digital systems. Not only do our product lines include industry standard devices, they also feature products with faster speeds, lower power, and package and/or architectural benefits that allow designers to significantly improve system performance.

To find ordering information: Ordering Information for all products in this book appears in Section 1, along with the Product Selector Matrix, Package Marking Description, and Functional Cross Reference. Reference data on our Technology Capabilities, Quality Commitments, and Package Diagram Outlines is included in Sections 2, 3, and 4 respectively.

To find product data: Begin with the Table of Contents (page 1.2), Product Selector Matrix (page 1.6), or with the Numeric Table of Contents (page 1.3). The Product Selector Matrix will help you identify the device you are interested in, while the Table of Contents indexes will direct you to the page on which the complete technical data sheet can be found. Data sheets may be of the following type:

ADVANCE INFORMATION—contain initial descriptions (subject to change) for products that are in development, including features, block diagrams, and target specifications.

PRELIMINARY—contain descriptions for products soon to be or recently, released to production, including features, pinouts, and block diagrams. Timing data are based on simulation or initial characterization and are subject to change upon full characterization.

FINAL—contain minimum and maximum limits specified over the complete voltage supply and temperature range for full production devices.

New products, product performance enhancements, additional package types, and new product families are being introduced frequently. Please contact your local IDT sales representative to determine the latest device specifications, package types, and product availability.

LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. **Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.**
2. **A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.**

Note: Integrated Device Technology, Inc. reserves the right to make changes to its products or specifications at any time, without notice, in order to improve design or performance and to supply the best possible product. IDT does not assume any responsibility for use of any circuitry described other than the circuitry embodied in an IDT product. The Company makes no representations that circuitry described herein is free from patent infringement or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent, patent rights or other rights, of Integrated Device Technology, Inc.

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1994 SRAM DATA BOOK
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1M SRAM PRODUCTS

3.3V ASYNCHRONOUS SRAM PRODUCTS

CacheRAMs

Cache Tags

Cache Controller PRODUCT

IDT SALES OFFICE, REPRESENTATIVE AND DISTRIBUTOR LOCATIONS

NUMERICAL TABLE OF CONTENTS

ORDERING INFORMATION

When ordering by TWX or Telex, the following format must be used:

A. Complete Bill To.
B. Complete Ship To.
C. Purchase Order Number.
D. Certificate of Conformance. Y or N.
E. Customer Source Inspection. Y or N.
F. Government Source Inspection. Y or N
G. Government Contract Number and Rating.
H. Requested Routing.
I. IDT Part Number –
Each item ordered must use the complete part number exactly as listed in the price book.
J. SCD Number — Specification Control Document (Internal Traveller).
K. Customer Part Number/Drawing Number/Revision Level –
Specify whether part number is for reference only, mark only, or if extended processing to customer specification is required.
L. Customer General Specification Numbers/Other Referenced Drawing Numbers/Revision Levels.
M. Request Date With Exact Quantity.
N. Unit Price.
O. Special Instructions, Including Q.A. Clauses, Special Processing.

Federal Supply Code Number/Cage Number — 61772
Dun & Bradstreet Number — 03-814-2600
Federal Tax I.D. — 94-2669985
TLX# — 887766
FAX# — 408-727-3468

PART NUMBER DESCRIPTION

A = Alpha Character N = Numeric Character

IDT	XXXXX	A	X	999	AA	AA	AA
	DEVICE TYPE	**POWER**	**REVISION**	**SPEED**	**PACKAGE**	**PROCESS/ TEMP.**	**SPECIAL PROCESS**

Field	Code	Description
SPECIAL PROCESS	RE	Radiation Enhanced
	RT	Radiation Tolerant
PROCESS/TEMP.	BLANK	Commercial — 0°C to +70°C
	M*	Commercial — –55°C to +125°C
	B	Military — –55°C to +125°C (Fully compliant to MIL-STD-883, Method 5004, Class B)
PACKAGE		See Package Description Table
SPEED	SPEED	Guaranteed Minimum Performance Measured in Nanoseconds or MHz
REVISION	A	
	BLANK	
POWER	POWER	S/SA — Standard Power
		L/LA — Low Power
DEVICE TYPE	DEVICE TYPE	e.g. 6116

PACKAGE DESCRIPTION TABLE

C	Ceramic Sidebraze	PF	Plastic Quad Flatpack
D	Cerdip	PZ	TSOP Type 1
F	Flatpack	SO	Plastic Small Outline IC
J	Plastic Leaded Chip Carrier	TC	Sidebraze Thindip (300-MIL)
L	Leadless Chip Carrier	TP	Plastic Thin Dual In-Line
P	Plastic DIP	TY	Thin SOJ
Y	SOJ	XE	Cerpack (F11 Config. only)

*Consult Factory

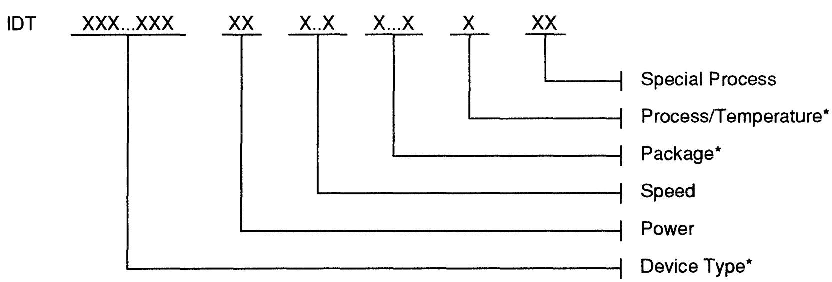
IDT PACKAGE MARKING DESCRIPTION

PART NUMBER DESCRIPTION

IDT's part number identifies the basic product, speed, power, package(s) available, operating temperature and processing grade. Each data sheet has a detailed description, using the part number, for ordering the proper product for the user's application. The part number is comprised of a series of alpha-numeric characters:

1. An "IDT" corporate identifier for Integrated Device Technology, Inc.
2. A basic device part number composed of alpha-numeric characters.
3. A device power identifier, composed of one or two alpha characters, is used to identify the power options. In most cases, the following alpha characters are used:
   "S" or "SA" is used for the standard power product.
   "L" or "LA" is used for lower power than the standard power product.
4. A device speed identifier, when applicable, is either alpha characters, such as "A" or "B", or numbers, such as 20 or 45. The speed units, depending on the product, are in nanoseconds or megahertz.
5. A package identifier, composed of one or two characters. The data sheet should be consulted to determine the packages available and the package identifiers for that particular product.
6. A temperature/process identifier. The product is available in either the commercial or military temperature range, processed to a commercial specification, or the product is available in the military temperature range with full compliance to MIL-STD-883. Many of IDT's products have burn-in included as part of the standard commercial process flow.
7. A special process identifier, composed of alpha characters, is used for products which require radiation enhancement (RE) or radiation tolerance (RT).

Example for Monolithic Devices:



* Field Identifier Applicable To All Products

2507 drw 01

ASSEMBLY LOCATION DESIGNATOR

IDT uses various locations for assembly. These are identified by an alpha character in the last letter of the date code marked on the package. Presently, the assembly location alpha character is as follows:

A = Anam, Korea
I = USA
P = Penang, Malaysia

MIL-STD-883C COMPLIANT DESIGNATOR

IDT ships military products which are compliant to the latest revision of MIL-STD-883C. Such products are identified by a "C" designation on the package. The location of this designator is specified by internal documentation at IDT.

High-Speed Standard and Specialty StaticRAMs

Integrated Device Technology, Inc.

Size/ Function	Org.	Features	Process	Part Number	Power	Speeds (ns) Commercial	Speeds (ns) Military	Commercial PDIP	SOJ	SOIC	TSOP	TQFP	PLCC	SBRZ	Military CDIP	LCC	CPAK
16K	16K x 1		CMOS	6167	SA/LA	15,20,25,35	15,20,25,35, 45,55,70,85,100	20	20	—	—	—	—	—	20	20	20
	4K x 4		CMOS	6168	SA/LA	15,20,25,35	15,20,25,35, 45,55,70,85,100	20	—	20	—	—	—	—	20	20	20
	4K x 4	Sep I/O	CMOS	71681	SA/LA	15,20,25,35,45	15,20,25,35, 45,55,70,85,100	24	—	—	—	—	—	—	24	28	24
	4K x 4	Sep I/O	CMOS	71682	SA/LA	15,20,25,35,45	12,15,20,25,35, 45,55,70,85,100	24	—	—	—	—	—	—	24	28	24
	2K x 8		CMOS	6116	SA/LA	15,20,25,35,45	20,25,35,45, 55,70,90,120,150	24	24	24	—	—	—	—	24	28/32	24
64K	64K x 1		CMOS	7187	S/L	15,20,25	20,25,35, 45,55,70,85	22	—	—	—	—	—	—	22	22/28	24
	16K x 4		CMOS	7188	S/L	20,25	20,25,35, 45,55,70,85	22	—	—	—	—	—	—	22	—	24
	16K x 4	$\overline{OE}$	CMOS	6198	S/L	15,20,25,35	20,25,35, 45,55,70,85	—	24	—	—	—	—	—	24	28	—
	16K x 4	$\overline{OE}$, $\overline{CS2}$	CMOS	7198	S/L	N/A	20,25,35, 45,55,70,85	—	—	—	—	—	—	—	24	28	24
	8K x 8		CMOS	7164	S/L	15,20,25,30	20,25,30,35, 45,55,70,85	28	28	28	—	—	—	—	28	32	28
256K	64K x 4		CMOS	61298	SA	12,15,17,20	20,25	28	28	—	—	—	—	28	—	28	—
	32K x 8		CMOS	71256	S/L	20,25,35,45	25,30,35,45, 55,70,85, 100,120,150	28	28	—	—	—	—	28	28	28/32	28
	32K x 8		CMOS	71256	SA	12,15,20,25	15,20,25	28	28	—	—	—	—	28	—	32	—
1M	256K x 4		CMOS	71028	S/L	12,15,17	15,17,20,25	28	28	—	—	—	—	—	28	28	—
	128K x 8		CMOS	71024	S/L	12,15,17,20	15,17,20,25	32	32	—	—	—	—	—	32	32	—
3.3V SRAMs	32K x 8	3.3V	3.3V CMOS	71V256	SA	20,25	N/A	—	28	—	—	—	—	—	—	—	—
	32K x 8	3.3V	3.3V CMOS	71V256	SL	15	N/A	28	28	—	28	—	—	—	—	—	—
Cache SRAMs	32K x 18	PowerPC Burst	BiCMOS	71419	S	9,10,12	N/A	—	—	—	—	—	52	—	—	—	—
	32K x 18	Intel Burst	BiCMOS	71420	S	9,10,12	N/A	—	—	—	—	—	52	—	—	—	—
	32K x 32	3.3V Intel Pipelined Burst	3.3V CMOS	71V432	S	9,10,12	N/A	—	—	—	—	100	—	—	—	—	—
Cache Tags	4K x 4	Tag	CMOS	6178	S	10,12,15,20,25	N/A	22	24	—	—	—	—	—	22	—	—
	8K x 8	Tag	BiCMOS	71B74	S	8,10,12,15,20	N/A	28	28	—	—	—	—	—	—	—	—
	16K x 15	Intel Tag	BiCMOS	71215	S	10,12	N/A	—	—	—	—	80	—	—	—	—	—
	16K x 15	PwrPC Tag	BiCMOS	71216	S	10,12	N/A	—	—	—	—	80	—	—	—	—	—
Cache Controller	16K x 10	3.3V Controller w/Tag	3.3V CMOS	71V280	S	66MHz	N/A	—	—	—	—	128	—	—	—	—	—

Integrated Device Technology, Inc.

SRAM FUNCTIONAL CROSS REFERENCE GUIDE

1

Note: This cross reference guide reflects Functional Correlation ONLY. Please refer to the individual data sheet specifications to ensure that the IDT device meets your parametric and packaging requirements.

ALLIANCE	IDT	DESCRIPTION
AS7C256	IDT71256SA	32K x 8
AS7C3256	IDT71V256SL	32K x 8 — 3.3V
AS7C3256	IDT71V256SA	32K x 8 — 3.3V
AT&T	**IDT**	**DESCRIPTION**
ATT7C167	IDT6167	16K x 1
ATT7C168	IDT6168	4K x 4
ATT7C171	IDT71681	4K x 4 Sep I/O
ATT7C172	IDT71682	4K x 4 Sep I/O
ATT7C116	IDT6116	2K x 8
ATT7C187	IDT7187	64K x 1
ATT7C164	IDT7188	16K x 4
ATT7C166	IDT6198	16K x 4 $\overline{OE}$
ATT7C165	IDT7198	16K x 4 $\overline{OE}/\overline{CS2}$
ATT7C185	IDT7164	8K x 8
ATT7C195	IDT61298SA	64K x 4 $\overline{OE}$
ATT7C199	IDT71256	32K x 8
ATT7C199	IDT71256SA	32K x 8
ATT7C106	IDT71028	256K x 4 $\overline{OE}$
ATT7C109	IDT71024	128K x 8
ATT7C180	IDT6178	4K x 4 Cache Tag
ATT7C174	IDT71B74	8K x 8 Cache Tag
CYPRESS	**IDT**	**DESCRIPTION**
CY7C167	IDT6167	16K x 1
CY7C167A	IDT6167	16K x 1
CY7C168	IDT6168	4K x 4
CY7C168A	IDT6168	4K x 4
CY7C169	IDT6168	4K x 4
CY7C169A	IDT6168	4K x 4
CY7C171	IDT71681	4K x 4 Sep I/O
CY7C171A	IDT71681	4K x 4 Sep I/O
CY7C172	IDT71682	4K x 4 Sep I/O
CY7C172A	IDT71682	4K x 4 Sep I/O
CY7C128	IDT6116	2K x 8
CY7C128A	IDT6116	2K x 8
CY7C187	IDT7187	64K x 1
CY7C187A	IDT7187	64K x 1
CY7C164	IDT7188	16K x 4
CY7C164A	IDT7188	16K x 4
CY7C166	IDT6198	16K x 4 $\overline{OE}$

CYPRESS	IDT	DESCRIPTION
CY7C166A	IDT6198	16K x 4 $\overline{OE}$
CY7C185	IDT7164	8K x 8
CY7C185A	IDT7164	8K x 8
CY7C186	IDT7164	8K x 8
CY7C186A	IDT7164	8K x 8
CY7C195	IDT61298SA	64K x 4 $\overline{OE}$
CY7B195	IDT61298SA	64K x 4 $\overline{OE}$
CY7C198	IDT71256	32K x 8
CY7C198	IDT71256SA	32K x 8
CY7C199	IDT71256	32K x 8
CY7C199	IDT71256SA	32K x 8
CY7B198	IDT71256SA	32K x 8
CY7B199	IDT71256SA	32K x 8
CYC1399	IDT71V256SL	32K x 8 — 3.3V
CYC1399	IDT71V256SA	32K x 8 — 3.3V
CY7C106	IDT71028	256K x 4 $\overline{OE}$
CY7C109	IDT71024	128K x 8
CY7C178	IDT71420	32K x 18 — Burst Pent
EDI	**IDT**	**DESCRIPTION**
EDI8164	IDT7187	64K x 1
EDI8416	IDT7188	16K x 4
EDI8417	IDT6198	16K x 4 $\overline{OE}$
EDI8808CB	IDT7164	8K x 8
EDI8466CA	IDT61298SA	64K x 4 $\overline{OE}$
EDI8466CB	IDT61298SA	64K x 4 $\overline{OE}$
EDI8833C	IDT71256	32K x 8
EDI8833C	IDT71256SA	32K x 8
EDI8833LP	IDT71256	32K x 8
EDI8833LP	IDT71256SA	32K x 8
EDI8833P	IDT71256	32K x 8
EDI8833P	IDT71256SA	32K x 8
EDI8834C	IDT71256	32K x 8
EDI8834C	IDT71256SA	32K x 8
EDI8834CA	IDT71256	32K x 8
EDI8834CA	IDT71256SA	32K x 8
EDI84256CS	IDT71028	256K x 4 $\overline{OE}$
EDI84256LPS	IDT71028	256K x 4 $\overline{OE}$
EDI84256PS	IDT71028	256K x 4 $\overline{OE}$
EDI88130C	IDT71024	128K x 8
EDI88130LP	IDT71024	128K x 8
EDI88130P	IDT71024	128K x 8
EDI88130CS	IDT71024	128K x 8
EDI88130LPS	IDT71024	128K x 8

EDI	IDT	DESCRIPTION
EDI88130PS	IDT71024	128K x 8
FUJITSU	**IDT**	**DESCRIPTION**
MB81C67	IDT6167	16K x 1
MB81C68A	IDT6168	4K x 4
MB81C69A	IDT6168	4K x 4
MB81C71	IDT7187	64K x 1
MB81C71A	IDT7187	64K x 1
MB81C74	IDT7188	16K x 4
MB81C75	IDT6198	16K x 4 $\overline{OE}$
MB81C78A	IDT7164	8K x 8
MB82B78	IDT7164	8K x 8
MB81C84A	IDT61298SA	64K x 4 $\overline{OE}$
MB82B85	IDT61298SA	64K x 4 $\overline{OE}$
MB8298	IDT71256	32K x 8
MB8298	IDT71256SA	32K x 8
MB82B88	IDT71256SA	32K x 8
MB82B005	IDT71028	256K x 4 $\overline{OE}$
MB82B008	IDT71024	128K x 8
HITACHI	**IDT**	**DESCRIPTION**
HM6267	IDT6167	16K x 1
HM6268	IDT6168	4K x 4
HM6716	IDT6116	2K x 8
HM6287	IDT7187	64K x 1
HM6287H	IDT7187	64K x 1
HM6787	IDT7187	64K x 1
HM6787H	IDT7187	64K x 1
HM6288	IDT7188	16K x 4
HM6788	IDT7188	16K x 4
HM6788H	IDT7188	16K x 4
HM6289	IDT6198	16K x 4 $\overline{OE}$
HM6789	IDT6198	16K x 4 $\overline{OE}$
HM6789H	IDT6198	16K x 4 $\overline{OE}$
HM6709A	IDT61298SA	64K x 4 $\overline{OE}$
HM62832H	IDT71256	32K x 8
HM62832H	IDT71256SA	32K x 8
HM62832UH	IDT71256SA	32K x 8
HM62832UHL	IDT71256SA	32K x 8
HM624256A	IDT71028	256K x 4 $\overline{OE}$
HM628127H	IDT71024	128K x 8
IC WORKS	**IDT**	**DESCRIPTION**
ICW73B586A	IDT71420	32K x 18 — Burst Pent
ICW73B586B	IDT71420	32K x 18 — Burst Pent
INMOS	**IDT**	**DESCRIPTION**
IMS1403	IDT6167	16K x 1
IMS1423	IDT6168	4K x 4
IMS1600	IDT7187	64K x 1
IMS1605	IDT7187	64K x 1
IMS1620	IDT7188	16K x 4

INMOS	IDT	DESCRIPTION
IMS1625	IDT7188	16K x 4
IMS1624	IDT6198	16K x 4 $\overline{OE}$
IMS1629	IDT6198	16K x 4 $\overline{OE}$
IMS1630	IDT7164	8K x 8
IMS1635	IDT7164	8K x 8
LOGIC	**IDT**	**DESCRIPTION**
L7C167	IDT6167	16K x 1
L7C168	IDT6168	4K x 4
L7C171	IDT71681	4K x 4 Sep I/O
L7C172	IDT71682	4K x 4 Sep I/O
L6116	IDT6116	2K x 8
L6116L	IDT6116	2K x 8
L7C187	IDT7187	64K x 1
L7C164	IDT7188	16K x 4
L7C166	IDT6198	16K x 4 $\overline{OE}$
L7C165	IDT7198	16K x 4 $\overline{OE}/\overline{CS2}$
L7C185	IDT7164	8K x 8
L7CL185	IDT7164	8K x 8
L7C195	IDT61298SA	64K x 4 $\overline{OE}$
L7C199	IDT71256	32K x 8
L7CL199	IDT71256	32K x 8
L7C199	IDT71256SA	32K x 8
L7CL199	IDT71256SA	32K x 8
L7C180	IDT6178	4K x 4 Cache Tag
L7C174	IDT71B74	8K x 8 Cache Tag
MICRON	**IDT**	**DESCRIPTION**
MT5C1601	IDT6167	16K x 1
MT5C1604	IDT6168	4K x 4
MT5C1606	IDT71681	4K x 4 Sep I/O
MT5C1607	IDT71682	4K x 4 Sep I/O
MT5C1608	IDT6116	2K x 8
MT5C6401	IDT7187	64K x 1
MT5C6404	IDT7188	16K x 4
MT5C6405	IDT6198	16K x 4 $\overline{OE}$
MT5C6408	IDT7164	8K x 8
MT5C2565	IDT61298SA	64K x 4 $\overline{OE}$
MT5C2568	IDT71256	32K x 8
MT5C2568	IDT71256SA	32K x 8
MT5LC2568	IDT71V256SL	32K x 8 — 3.3V
MT5LC2568	IDT71V256SA	32K x 8 — 3.3V
MT5C1005	IDT71028	256K x 4 $\overline{OE}$
MT5C1008	IDT71024	128K x 8
MITSUBISHI	**IDT**	**DESCRIPTION**
M5M21C67	IDT6167	16K x 1
M5M21C68	IDT6168	4K x 4
M5M5187A	IDT7187	64K x 1
M5M5187B	IDT7187	64K x 1
M5M5188A	IDT7188	16K x 4

MITSUBISHI	IDT	DESCRIPTION
M5M5188B	IDT7188	16K x 4
M5M5189A	IDT6198	16K x 4 $\overline{OE}$
M5M5189B	IDT6198	16K x 4 $\overline{OE}$
M5M5178	IDT7164	8K x 8
M5M5178A	IDT7164	8K x 8
M5M5178B	IDT7164	8K x 8
M5M5259B	IDT61298SA	64K x 4 $\overline{OE}$
M5M5278	IDT71256	32K x 8
M5M5278	IDT71256SA	32K x 8
M5M51004	IDT71028	256K x 4 $\overline{OE}$

MOTOROLA	IDT	DESCRIPTION
MCM6268	IDT6168	4K x 4
MCM6287B	IDT7187	64K x 1
MCM6288	IDT7188	16K x 4
MCM6288B	IDT7188	16K x 4
MCM6288C	IDT7188	16K x 4
MCM6290	IDT6198	16K x 4 $\overline{OE}$
MCM6290C	IDT6198	16K x 4 $\overline{OE}$
MCM6264C	IDT7164	8K x 8
MCM6209	IDT61298SA	64K x 4 $\overline{OE}$
MCM6209C	IDT61298SA	64K x 4 $\overline{OE}$
MCM6206	IDT71256	32K x 8
MCM6206C	IDT71256	32K x 8
MCM6206D	IDT71256	32K x 8
MCM6206	IDT71256SA	32K x 8
MCM6206C	IDT71256SA	32K x 8
MCM6206D	IDT71256SA	32K x 8
MCM62V06	IDT71V256SL	32K x 8 — 3.3V
MCM62V06	IDT71V256SA	32K x 8 — 3.3V
MCM6306D	IDT71V256SL	32K x 8 — 3.3V
MCM6360D	IDT71V256SA	32K x 8 — 3.3V
MCM6229	IDT71028	256K x 4 $\overline{OE}$
MCM6229A	IDT71028	256K x 4 $\overline{OE}$
MCM6229B	IDT71028	256K x 4 $\overline{OE}$
MCM6226	IDT71024	128K x 8
MCM6226A	IDT71024	128K x 8
MCM67B518	IDT71418	32K x 18 — Burst Pent
MCM67M518	IDT71419	32K x 18 — Burst PwrPC
MCM67H518	IDT71420	32K x 18 — Burst Pent

NEC	IDT	DESCRIPTION
uPD4311	IDT6167	16K x 1
uPD4314C	IDT6168	4K x 4
uPD4361	IDT7187	64K x 1
uPD4361B	IDT7187	64K x 1
uPD4362	IDT7188	16K x 4
uPD4362B	IDT7188	16K x 4
uPD4363	IDT6198	16K x 4 $\overline{OE}$

NEC	IDT	DESCRIPTION
uPD4368	IDT7164	8K x 8
uPD43253	IDT61298SA	64K x 4 $\overline{OE}$
uPD43258	IDT71256	32K x 8
uPD43258A	IDT71256	32K x 8
uPD43258	IDT71256SA	32K x 8
uPD43258A	IDT71256SA	32K x 8
uPD431004	IDT71028	256K x 4 $\overline{OE}$
uPD431008	IDT71024	128K x 8

PARADIGM	IDT	DESCRIPTION
PDM41298	IDT61298SA	64K x 4 $\overline{OE}$
PDM41256	IDT71256	32K x 8
PDM41256	IDT71256SA	32K x 8
PDM41028	IDT71028	256K x 4 $\overline{OE}$
PDM41024	IDT71024	128K x 8
PDM44528	IDT71420	32K x 18 — Burst Pent

PERFORMANCE	IDT	DESCRIPTION
P4C168	IDT6168	4K x 4
P4C1681	IDT71681	4K x 4 Sep I/O
P4C1682	IDT71682	4K x 4 Sep I/O
P4C116	IDT6116	2K x 8
P4C187	IDT7187	64K x 1
P4C188	IDT7188	16K x 4
P4C198	IDT6198	16K x 4 $\overline{OE}$
P4C198A	IDT7198	16K x 4 $\overline{OE}/\overline{CS2}$
P4C164	IDT7164	8K x 8
P4C1298	IDT61298SA	64K x 4 $\overline{OE}$
P4C1256	IDT71256	32K x 8
P4C1256	IDT71256SA	32K x 8

QUALITY	IDT	DESCRIPTION
QS8768	IDT6168	4K x 4
QS8761	IDT71681	4K x 4 Sep I/O
QS8762	IDT71682	4K x 4 Sep I/O
QS8888	IDT7188	16K x 4
QS8888A	IDT7188	16K x 4
QS8886	IDT6198	16K x 4 $\overline{OE}$
QS8885	IDT7198	16K x 4 $\overline{OE}/\overline{CS2}$
QS86446	IDT61298SA	64K x 4 $\overline{OE}$
QS83280	IDT71256	32K x 8
QS83280	IDT71256SA	32K x 8
QS812880	IDT71024	128K x 8
QS8780	IDT6178	4K x 4 Cache Tag
QS83291	IDT71589	32K x 9 Burst 486

SAMSUNG	IDT	DESCRIPTION
KM6165	IDT7187	64K x 1
KM6465	IDT7188	16K x 4
KM6465A	IDT7188	16K x 4
KM6465B	IDT7188	16K x 4

SAMSUNG	IDT	DESCRIPTION
KM6466	IDT6198	16K x 4 $\overline{OE}$
KM6466A	IDT6198	16K x 4 $\overline{OE}$
KM6466B	IDT6198	16K x 4 $\overline{OE}$
KM64B67	IDT7198	16K x 4 $\overline{OE}/\overline{CS2}$
KM6865	IDT7164	8K x 8
KM6865B	IDT7164	8K x 8
KM64258	IDT61298SA	64K x 4 $\overline{OE}$
KM64258B	IDT61298SA	64K x 4 $\overline{OE}$
KM68257	IDT71256	32K x 8
KM68257	IDT71256SA	32K x 8
KM68257B	IDT71256	32K x 8
KM68257B	IDT71256SA	32K x 8
KM688V257	IDT71V256SL	32K x 8 — 3.3V
KM688V257	IDT71V256SA	32K x 8 — 3.3V
KM641001	IDT71028	256K x 4 $\overline{OE}$
KM681001	IDT71024	128K x 8
SGS	**IDT**	**DESCRIPTION**
MK41H67	IDT6167	16K x 1
MK41H68	IDT6168	4K x 4
MK41H87	IDT7187	64K x 1
MK41H80	IDT6178	4K x 4 Cache Tag
MK41S80	IDT6178	4K x 4 Cache Tag
MK48S74	IDT71B74	8K x 8 Cache Tag
SHARP	**IDT**	**DESCRIPTION**
LH5267A	IDT6198	16K x 4 $\overline{OE}$
LH52253	IDT61298SA	64K x 4 $\overline{OE}$
LH52258	IDT71256	32K x 8
LH52258	IDT71256SA	32K x 8
LH52258A	IDT71256	32K x 8
LH52258A	IDT71256SA	32K x 8
LH52258B	IDT71256	32K x 8
LH52258B	IDT71256SA	32K x 8
LH521002	IDT71028	256K x 4 $\overline{OE}$
LH521007	IDT71024	128K x 8
SONY	**IDT**	**DESCRIPTION**
CXK5164	IDT7187	64K x 1
CXK5464A	IDT7188	16K x 4
CXK5466	IDT7188	16K x 4
CXK5465/7	IDT6198	16K x 4 $\overline{OE}$
CXK5863	IDT7164	8K x 8
CXK5863A	IDT7164	8K x 8
CXK58258	IDT71256	32K x 8
CXK58258	IDT71256SA	32K x 8
CXK58258B	IDT71256	32K x 8
CXK58258B	IDT71256SA	32K x 8
CXK58258A	IDT71256SA	32K x 8
CXK541000	IDT71028	256K x 4 $\overline{OE}$
CXK581120	IDT71024	128K x 8

TI	IDT	DESCRIPTION
TM6716	IDT6116	2K x 8
TM6787	IDT7187	64K x 1
TM6788	IDT7188	16K x 4
TM6789	IDT6198	16K x 4 $\overline{OE}$
TOSHIBA	**IDT**	**DESCRIPTION**
TMM2018	IDT6116	2K x 8
TC5561	IDT7187	64K x 1
TC5562	IDT7187	64K x 1
TC55416	IDT7188	16K x 4
TC55416-H	IDT7188	16K x 4
TC55417	IDT6198	16K x 4 $\overline{OE}$
TC55417-H	IDT6198	16K x 4 $\overline{OE}$
TC5588	IDT7164	8K x 8
TC55465	IDT61298SA	64K x 4 $\overline{OE}$
TC55328	IDT71256	32K x 8
TC55328	IDT71256SA	32K x 8
TC55B328	IDT71256SA	32K x 8
TC55V328	IDT71V256SA	32K x 8 — 3.3V

IDT...LEADING THE CMOS FUTURE

A major revolution is taking place in the semiconductor industry today. A new technology is rapidly displacing older NMOS and bipolar technologies as the workhorse of the '80s and beyond. That technology is high-speed CMOS. Integrated Device Technology, a company totally predicated on and dedicated to implementing high-performance CMOS products, is on the leading edge of this dramatic change.

Beginning with the introduction of the industry's fastest CMOS 2K x 8 static RAM, IDT has grown into a company with multiple divisions producing a wide range of high-speed CMOS circuits that are, in almost every case, the fastest available. These advanced products are produced with IDT's proprietary CEMOS™ technology, a twin-well, dry-etched, stepper-aligned process utilizing progressively smaller dimensions.

From inception, IDT's product strategy has been to apply the advantages of its extremely fast CEMOS technology to produce the integrated circuit elements required to implement high-performance digital systems. IDT's goal is to provide the circuits necessary to create systems which are far superior to previous generations in performance, reliability, cost, weight, and size. Many of the company's innovative product designs offer higher levels of integration, advanced architectures, higher density packaging and system enhancement features that are establishing tomorrow's industry standards. The company is committed to providing its customers with an ever-expanding series of these high-speed, lower-power IC solutions to system design needs.

IDT's commitment, however, extends beyond state-of-the-art technology and advanced products to providing the highest level of customer service and satisfaction in the industry. Manufacturing products to exacting quality standards that provide excellent, long-term reliability is given the same level of importance and priority as device performance. IDT is also dedicated to delivering these high-quality advanced products on time. The company would like to be known not only for its technological capabilities, but also for providing its customers with quick, responsive, and courteous service.

IDT's product families are available in both commercial and military grades. As a bonus, commercial customers obtain the benefits of military processing disciplines, established to meet or exceed the stringent criteria of the applicable military specifications.

IDT is the leading U.S. supplier of high-speed CMOS circuits. The company's high-performance fast SRAM , FCT logic, high-density modules, FIFOs, multi-port memories, BiCMOS ECL I/O memories, RISC SubSystems, and the 32- and 64-bit RISC microprocessor families complement each other to provide high-speed CMOS solutions for a wide range of applications and systems.

In 1993, IDT introduced its newest RISC microprocessor based on the MIPS architecture for the desktop PC, and embedded control markets. The R4600 Orion microprocessor, is the first RISC processor offering Pentium performance at a cost lower than most of Intel's 486DX line.

The R4600 is a full 64-bit implementation of the MIPS III instruction set architecture found in the popular R4000PC and R4400PC, but uses a shorter pipeline resulting in fewer stalls and, therefore, higher performance.

When compared against other processors targeted at the Windows NT market, the R4600 possesses clear advantages. The R4600 has the best performance per dollar, the best performance per watt cfonsumed, and the most efficient use of silicon for the performance attained.

Dedicated to maintaining its leadership position as a state-of-the-art IC manufacturer, IDT will continue to focus on maintaining its technology edge as well as developing a broader range of innovative products. New products and speed enhancements are continuously being added to each of the existing product families, and additional product families are being introduced. Contact your IDT field representative or factory marketing engineer for information on the most current product offerings. If you're building state-of-the-art equipment, IDT wants to help you solve your design problems.

IDT MILITARY AND DESC-SMD PROGRAM

IDT is a leading supplier of military, high-speed CMOS circuits. The company's high-performance Static RAMs, FCT Logic Family, Complex Logic (CLP), FIFOs, Specialty Memories (SMP), ECL I/O BiCMOS Memories, 32-bit RISC Microprocessor, RISC Subsystems and high-density Subsystems Modules product lines complement each other to provide high-speed CMOS solutions to a wide range of military applications and systems. Most of these product lines offer Class B products which are fully compliant to the latest revision of MIL-STD-883, Paragraph 1.2.1. In addition, IDT offers Radiation Tolerant (RT), as well as Radiation Enhanced (RE), products.

IDT has an active program with the Defense Electronic Supply Center (DESC) to list all of IDT's military compliant devices on Standard Military Drawings (SMD). The SMD program allows standardization of militarized products and reduction of the proliferation of non-standard source control drawings. This program will go far toward reducing the need for each defense contractor to make separate specification control drawings for purchased parts. IDT plans to have SMDs for many of its product offerings. Presently, IDT has 88 devices which are listed or pending listing. The devices are from IDT's SRAM, FCT Logic family, Complex Logic (CLP), FIFOs and Specialty Memories (SMP) product families. IDT expects to add another 20 devices to the SMD program in the near future. Users should contact either IDT or DESC for current status of products in the SMD program.

SMD	
SRAM	**IDT**
84036	6116
5962-88740	6116LA
84132	6167
5962-86015	7187
5962-86859	6198/7198/7188
5962-86705	6168
5962-85525	7164
5962-88552	71256L
5962-88662	71256S
5962-88611	71682L
5962-89891	7198
5962-89892	6198
5962-89690	6116
5962-38294	7164
5962-89692	7188
5962-89712	71982
5962-89790	71682
SMP	**IDT**
5962-86875	7130/7140
5962-87002	7132/7142
5962-88610	7133SA/7143SA
5962-88665	7133LA/7143LA
5962-89764	7134
5962-91508	7006
5962-91617	7025
5962-91662	7024
5962-93153	7014S
FIFO	**IDT**
5962-87531	7201LA
5962-86846	72404L
5962-88669	7203S
5962-89568	7204L
5962-89536	7202LA
5962-89863	7201SA
5962-89523	72403L
5962-89666	7200L
5962-89942	72103L
5962-89943	72104L
5962-89567	7203L
5962-90715	7204S
5962-91677	7205L

SMD	
5962-93177	7206L
5962-92069	72141L
5962-92101	72215LB
5962-93138	72220L
5962-92057	72225LB
5962-93189	72245LB
5962-91757	72200L
CLP	**IDT**
5962-87708	39C10B & C
5962-88533	49C460A/B/C
5962-88613	39C60/A
5962-88643	49C410
5962-86873	7216L
5962-87686	7217L
5962-88733	7210
5962-92122	49C465/A
LOGIC	**IDT**
5962-87630	54FCT244/A
5962-87629	54FCT245/A
5962-86862	54FCT299/A
5962-87644	54FCT373/A
5962-87628	54FCT374/A
5962-87627	54FCT377/A
5962-87654	54FCT138/A
5962-87655	54FCT240/A
5962-87656	54FCT273/A
5962-89533	54FCT861A/B
5962-89506	54FCT827A/B
5962-88575	54FCT841A/B
5962-88608	54FCT821A/B
5962-88543	54FCT521/A
5962-88640	54FCT161/A
5962-88639	54FCT573/A
5962-88656	54FCT823A/B
5962-88657	54FCT163/A
5962-88674	54FCT825A/B
5962-88661	54FCT863A/B
5962-88736	29FCT520A/B
5962-88775	54FCT646/A
5962-89508	54FCT139/A
5962-89665	54FCT824A/B
5962-88651	54FCT533/A
5962-88653	54FCT645/A

SMD	
5962-88654	54FCT640/A
5962-88655	54FCT534/A
5962-89767	54FCT540/A
5962-89766	54FCT541/A
5962-89733	54FCT191/A
5962-89732	54FCT241/A
5962-89652	54FCT399/A
5962-89513	54FCT574/A
5962-89731	54FCT833A/B
5962-89730	54FCT543/A
5962-90901	29FCT52A/B/C
5962-92205	29FCT520AT/BT/CT
5962-92157	49FCT805/A/806/A
5962-92233	54FCT138T/AT/CT
5962-92208	54FCT157T/AT/CT
5962-92209	54FCT161T/AT/CT
5962-92210	54FCT163T/AT/CT
5962-90669	54FCT193/A
5962-92213	54FCT240T/AT/CT
5962-92232	54FCT241T/AT/CT
5962-92203	54FCT244T/AT/CT
5962-92214	54FCT245T/AT/CT
5962-92211	54FCT257T/AT/CT
5962-92215	54FCT273T/AT/CT
5962-92216	54FCT299T/AT/CT
5962-92217	54FCT373T/AT/CT
5962-92218	54FCT374T/AT/CT
5962-92219	54FCT377T/AT/CT
5962-92212	54FCT399T/AT/CT
5962-92234	54FCT521T/AT/BT/CT
5962-92236	54FCT534T/AT/CT
5962-92220	54FCT540T/AT/CT
5962-92237	54FCT541T/AT/CT
5962-92221	54FCT543T/AT/CT
5962-92238	54FCT573T/AT/CT
5962-92222	54FCT574T/AT/CT
5962-92244	54FCT645T/AT/CT
5962-92223	54FCT646T/AT/CT
5962-92246	54FCT652T/AT/CT
5962-92225	54FCT821AT/BT/CT
5962-92229	54FCT823AT/BT/CT
5962-92230	54FCT825AT/BT/CT
5962-92247	54FCT827AT/BT/CT

SMD	
SRAM	**IDT**
84036	6116
5962-88740	6116LA
84132	6167
5962-86015	7187
5962-86859	6198/7198/7188
5962-86705	6168
5962-85525	7164
5962-88552	71256L
5962-88662	71256S
5962-88611	71682L
5962-89891	7198
5962-89892	6198
5962-89690	6116
5962-38294	7164
5962-89692	7188
5962-89712	71982
5962-89790	71682

SMP	IDT
5962-86875	7130/7140
5962-87002	7132/7142
5962-88610	7133SA/7143SA
5962-88665	7133LA/7143LA
5962-89764	7134
5962-91508	7006
5962-91617	7025
5962-91662	7024
5962-93153	7014S

FIFO	IDT
5962-87531	7201LA
5962-86846	72404L
5962-88669	7203S
5962-89568	7204L
5962-89536	7202LA
5962-89863	7201SA
5962-89523	72403L
5962-89666	7200L
5962-89942	72103L
5962-89943	72104L
5962-89567	7203L
5962-90715	7204S
5962-91677	7205L
5962-93177	7206L
5962-92069	72141L
5962-92101	72215LB
5962-93138	72220L
5962-92057	72225LB
5962-93189	72245LB
5962-91757	72200L

CLP	IDT
5962-87708	39C10B & C
5962-88533	49C460A/B/C
5962-88613	39C60/A
5962-88643	49C410
5962-86873	7216L
5962-87686	7217L
5962-88733	7210
5962-92122	49C465/A

LOGIC	IDT
5962-87630	54FCT244/A
5962-87629	54FCT245/A
5962-86862	54FCT299/A
5962-87644	54FCT373/A
5962-87628	54FCT374/A
5962-87627	54FCT377/A
5962-87654	54FCT138/A
5962-87655	54FCT240/A
5962-87656	54FCT273/A
5962-89533	54FCT861A/B
5962-89506	54FCT827A/B
5962-88575	54FCT841A/B
5962-88608	54FCT821A/B
5962-88543	54FCT521/A
5962-88640	54FCT161/A
5962-88639	54FCT573/A
5962-88656	54FCT823A/B
5962-88657	54FCT163/A
5962-88674	54FCT825A/B
5962-88661	54FCT863A/B
5962-88736	29FCT520A/B
5962-88775	54FCT646/A
5962-89508	54FCT139/A
5962-89665	54FCT824A/B
5962-88651	54FCT533/A
5962-88653	54FCT645/A
5962-88654	54FCT640/A
5962-88655	54FCT534/A
5962-89767	54FCT540/A
5962-89766	54FCT541/A
5962-89733	54FCT191/A
5962-89732	54FCT241/A
5962-89652	54FCT399/A
5962-89513	54FCT574/A
5962-89731	54FCT833A/B
5962-89730	54FCT543/A
5962-90901	29FCT52A/B/C
5962-92205	29FCT520AT/BT/CT
5962-92157	49FCT805/A/806/A
5962-92233	54FCT138T/AT/CT
5962-92208	54FCT157T/AT/CT
5962-92209	54FCT161T/AT/CT
5962-92210	54FCT163T/AT/CT
5962-90669	54FCT193/A
5962-92213	54FCT240T/AT/CT
5962-92232	54FCT241T/AT/CT
5962-92203	54FCT244T/AT/CT
5962-92214	54FCT245T/AT/CT
5962-92211	54FCT257T/AT/CT
5962-92215	54FCT273T/AT/CT
5962-92216	54FCT299T/AT/CT
5962-92217	54FCT373T/AT/CT
5962-92218	54FCT374T/AT/CT
5962-92219	54FCT377T/AT/CT
5962-92212	54FCT399T/AT/CT
5962-92234	54FCT521T/AT/BT/CT
5962-92236	54FCT534T/AT/CT
5962-92220	54FCT540T/AT/CT
5962-92237	54FCT541T/AT/CT
5962-92221	54FCT543T/AT/CT
5962-92238	54FCT573T/AT/CT
5962-92222	54FCT574T/AT/CT
5962-92244	54FCT645T/AT/CT
5962-92223	54FCT646T/AT/CT
5962-92246	54FCT652T/AT/CT
5962-92225	54FCT821AT/BT/CT
5962-92229	54FCT823AT/BT/CT
5962-92230	54FCT825AT/BT/CT
5962-92247	54FCT827AT/BT/CT

RADIATION HARDENED TECHNOLOGY

IDT manufactures and supplies radiation hardened products for military/aerospace applications. Utilizing special processing and starting materials, IDT's radiation hardened devices survive in hostile radiation environments. In Total Dose, Dose Rate, and environments where single event upset is of concern, IDT products are designed to continue functioning without loss of performance. IDT can supply all its products on these processes. Total Dose radiation testing is performed in-house on an ARACOR X-Ray system. External facilities are utilized for device research on gamma cell, LINAC and other radiation equipment. IDT has an on-going research and development program for improving radiation handling capabilities (See "IDT Radiation Tolerant/Enhanced Products for Radiation Environments" in Section 3) of IDT products/processes.

IDT LEADING EDGE CEMOS TECHNOLOGY

HIGH-PERFORMANCE CEMOS

From IDT's beginnings in 1980, it has had a belief in and a commitment to CMOS. The company developed a high-performance version of CMOS, called enhanced CMOS (CEMOS), that allows the design and manufacture of leading-edge components. It incorporates the best characteristics of traditional CMOS, including low power, high noise immunity and wide operating temperature range; it also achieves speed and output drive equal or superior to bipolar Schottky TTL. The last decade has seen development and production of four "generations" of IDT's CEMOS technology with process improvements which have reduced IDT's electrical effective (Leff) gate lengths by more than 60 percent from 1.3 microns (millionths of a meter) in 1981 to 0.45 microns in 1993.

	CEMOS I	CEMOS II A	CEMOS II C	CEMOS III	CEMOS V	CEMOS VI	CEMOS VII Vcc = 5V	CEMOS VII Vcc = 3.3V
Calendar Year	**1981**	**1983**	**1985**	**1987**	**1989**	**1990**	**1992**	**1993**
Drawn Feature Size	2.5μ	1.7μ	1.3μ	1.2μ	1.0μ	0.8μ	0.65μ	0.65μ
Leff	1.3μ	1.1μ	0.9μ	0.8μ	0.6μ	0.45μ	0.45μ	0.25μ
Basic Proces Enhancements	Dual-well, Wet Etch, Projection Aligned	Dry Etch, Stepper	Shrink, Spacer	Silicide, BPSG, BiCEMOS I	BiCEMOS II	BiCEMOS III	BiCEMOS IV Vcc = 5V	BiCEMOS IV Vcc = 3.3V

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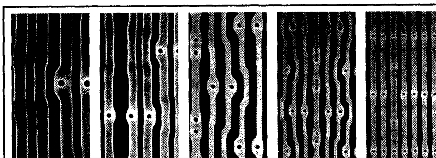
CEMOS IV = CEMOS III – scaled process optimized for high-speed logic.

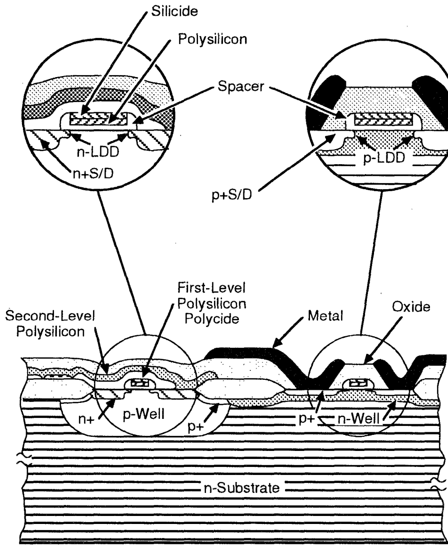
Figure 1.

Continual advancement of CEMOS technology allows IDT to implement progressively higher levels of integration and achieve increasingly faster speeds maintaining the company's established position as the leader in high-speed CMOS integrated circuits. In addition, the fundamental process technology has been extended to add bipolar elements to the CEMOS platform. IDT's BiCEMOS process combines the ultra-high speeds of bipolar devices with the lower power and cost of CMOS, allowing us to build even faster components than straight CMOS at a slightly higher cost.



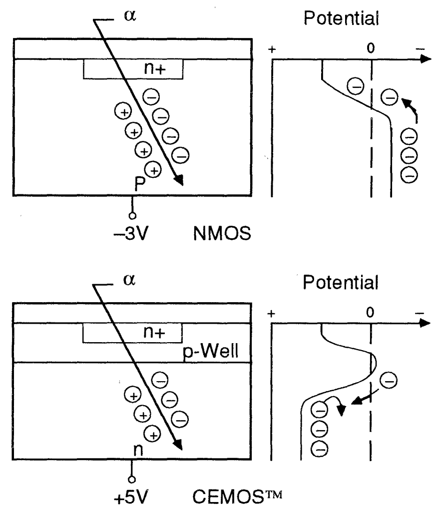
SEM photos (miniaturization) 2514 drw 02

Figure 2. Fifteen-Hundred-Power Magnification Scanning Electron Microscope (SEM) Photos of the Four Generations of IDT's CEMOS Technology



2514 drw 03

Figure 3. IDT CEMOS Device Cross Section



2514 drw 04

Figure 4. IDT CEMOS Built-In High Alpha Particle Immunity

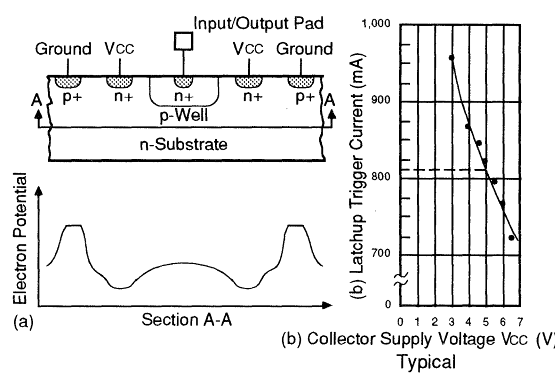
ALPHA PARTICLES

Random alpha particles can cause memory cells to temporarily lose their contents or suffer a "soft error." Traveling with high energy levels, alpha particles penetrate deep into an integrated chip. As they burrow into the silicon, they leave a trail of free electron-hole pairs in their wake.

The cause of alpha particles is well documented and understood in the industry. IDT has considered various techniques to protect the cells from this hazardous occurrence. These techniques include dual-well structures (Figures 3 and 4) and a polymeric compound for die coating. Presently, a polymeric compound is used in many of IDT's SRAMs; however, the specific techniques used may vary and change from one device generation to the next as the industry and IDT improve the alpha particle protection technology.

LATCHUP IMMUNITY

A combination of careful design layout, selective use of guard rings and proprietary techniques have resulted in virtual elimination of latchup problems often associated with older CMOS processes (Figure 5). The use of NPN and N-channel I/O devices eliminates hole injection latchup. Double guard ring structures are utilized on all input and output circuits to absorb injected electrons. These effectively cut off the current paths into the internal circuits to essentially isolate I/O circuits. Compared to older CMOS processes which exhibit latchup characteristics with trigger currents from 10-20mA, IDT products inhibit latchup at trigger currents substantially greater than this.



2514 drw 05

Figure 5. IDT CEMOS Latchup Suppression

SURFACE MOUNT TECHNOLOGY AND IDT'S MODULE PRODUCTS

Requirements for circuit area reduction, utilizing the most efficient and compact component placement possible and the needs of production manufacturing for electronics assemblies are the driving forces behind the advancement of circuit-board assembly technologies. These needs are closely associated with the advances being made in surface mount devices (SMD) and surface mount technology (SMT) itself. Yet, there are two major issues with SMT in production manufacturing of electronic assemblies: high capital expenditures and complexity of testing.

The capital expenditure required to convert to efficient production using SMT is still too high for the majority of electronics companies, regardless of the 20-60% increase in the board densities which SMT can bring. Because of this high barrier to entry, we will continue to see a large market segment [large even compared to the exploding SMT market] using traditional through-hole packages (i.e. DIPs, PGAs, etc) and assembly techniques. How can these types of companies take advantage of SMD and SMT? Let someone else, such as IDT, do it for them by investing time and money in SMT and then in return offer through-hole products utilizing SMT processes. Products which fit this description are modules, consisting of SMT assembled SMDs on a through-hole type substrate. Modules enable companies to enjoy SMT density advantages and traditional package options without the expensive startup costs required to do SMT in-house.

Although subcontracting this type of work to an assembly house is an alternative, there still is the other issue of testing, an area where many contract assembly operations fall short of IDT's capability and experience. Prerequisites for adequate module testing sophisticated high performance parametric testers, customized test fixtures, and most importantly the experience to tests today's complex electronic devices. Companies can therefore take advantage of IDT's experience in testing and manufacturing high performance modules.

At IDT, SMD components are electrically tested, environmentally screened, and performance selected for each IDT module. All modules are 100% tested as if they are a separate functional component and are guaranteed to meet all specified parameters at the module output .

IDT has recognized the problems of SMT and began offering CMOS modules as part of its standard product portfolio. IDT modules combine the advantages of:

1) the low power characteristics of IDT's CMOS and BiCMOS products,
2) the density advantages of first class SMD components including those from IDT's components divisions, and
3) experience in system level design, manufacturing, and testing with its own in-house SMT operation.

IDT currently has two divisions (Subsystems and RISC Subsystems) dedicated to the development of module products ranging from simple memory modules to complex VME sized application specific modules to full system level CPU boards. These modules have surface mount devices assembled on both sides of either a multi-layer glass filled epoxy (FR-4) or a multi-layer co-fired ceramic substrate. Assembled modules come available in industry standard through-hole packages and other space-saving module packages. Industry proven vapor-phase or IR reflow techniques are used to solder the SMDs to the substrate during the assembly process. Because of our affiliation with IDT's experienced semiconductor manufacturing divisions, we thoroughly understand and therefore test all modules to the applicable datasheet specifications and customer requirements.

Thus, IDT is able to offer today's electronic design engineers a unique solution. These high speed, high performance products offer the density advantages of SMD and SMT, the added benefit of low power CMOS technology, and through-hole packaged electronics without the high cost of doing it in-house.

STATE-OF-THE-ART FACILITIES AND CAPABILITIES

Integrated Device Technology is headquartered in Santa Clara, California—the heart of "Silicon Valley." The company's operations are housed in six facilities totaling over 500,000 square feet. These facilities house all aspects of business from research and development to design, wafer fabrication, assembly, environmental screening, test, and administration. In-house capabilities include scanning electron microscope (SEM) evaluation, particle impact noise detection (PIND), plastic and hermetic packaging, military and commercial testing, burn-in, life test, and a full complement of environmental screening equipment.

The over-200,000-square-foot corporate headquarters campus is composed of three buildings. The largest facility on this site is a 100,000 square foot, two-building complex. The first building, a 60,000-square-foot facility, is dedicated to the Standard Logic and RISC Microprocessor product lines, as well as hermetic and plastic package assembly, logic products' test, burn-in, mark, QA, and a reliability/failure analysis lab.

IDT's Packaging and Assembly Process Development teams are located here. To keep pace with the development of new products and to enhance the IDT philosophy of "innovation," these teams have ultra-modern, integrated and correspondingly sophisticated equipment and environments at their disposal. All manufacturing is completed in dedicated clean room areas (Class 10K minimum), with all preseal operations accomplished under Class 100 laminar flow hoods.

Development of assembly materials, processes and equipment is accomplished under a fully operational production environment to ensure reliability and repeatable product. The Hermetic Manufacturing and Process Development team is currently producing custom products to the strict requirements of MIL-STD-883. The fully automated plastic facility is currently producing high volumes of USA-manufactured product, while developing state-of-the-art surfac- mount technology patterned after MIL-STD-883.

The second building of the complex houses sales, marketing, finance, MIS, and Northwest Area Sales.

The RISC Subsystems Division is located across from the two-building complex in a 50,000-square-foot facility. Also located at this facility are Quality Assurance, wafer fabrication services, Administrative services, Human Resources, International Planning, and the Shipping and Receiving departments.

IDT's largest and newest facility, opened in 1990 in San Jose, California, is a multi-purpose 150,000-square-foot, ultra-modern technology development center. This facility houses a 25,000 square foot, combined Class 1 (a maximum of one particle-per-cubic-foot of 0.2 micron or larger), sub-half-micron R&D fabrication facility and a wafer fabrication area. This fab supports both production volumes of IDT products, including some next-generation SRAMs, and the R&D efforts of the technology development staff. Technology development efforts targeted for the center include advanced silicon processing and wafer fabrication techniques. A test area to support both production and research is located on-site. The building is also the home of the FIFO, ECL, and Subsystems product lines.

IDT's second largest facility is located in Salinas, California, about an hour south of Santa Clara. This 95,000-square-foot facility, located on 14 acres, houses the Static RAM Division and Specialty Memory product line. Constructed in 1985, this facility contains an ultra-modern 25,000-square-foot high-volume wafer fabrication area measured at Class 2-to-3 (a maximum of 2 to 3 particles-per-cubic-foot of 0.2 micron or larger) clean room conditions. Careful design and construction of this fabrication area created a clean room environment far beyond the 1985 average for U.S. fab areas. This made possible the production of large volumes of high-density submicron geometry, fast static RAMs. This facility also houses shipping areas for IDT's leadership family of CMOS static RAMs. This site can expand to accommodate a 250,000-square-foot complex.

To extend our capabilities while maintaining strict control of our processes, IDT has an operational Assembly and Test facility located in Penang, Malaysia. This facility assembles product to U.S. standards, with all assemblies done under laminar flow conditions (Class 100) until the silicon is encased in its final packaging. All products in this facility are manufactured to the quality control requirements of MIL-STD-883.

All of IDT's facilities are aimed at increasing our manufacturing productivity to supply ever-larger volumes of high-performance, cost-effective, leadership CMOS products.

SUPERIOR QUALITY AND RELIABILITY

Maintaining the highest standards of quality in the industry on all products is the basis of Integrated Device Technology's manufacturing systems and procedures. From inception, quality and reliability are built into all of IDT's products. Quality is "designed in" at every stage of manufacturing – as opposed to being "tested-in" later – in order to ensure impeccable performance.

Dedicated commitment to fine workmanship, along with development of rigid controls throughout wafer fab, device assembly and electrical test, create inherently reliable products. Incoming materials are subjected to careful inspections. Quality monitors, or inspections, are performed throughout the manufacturing flow.

IDT military grade monolithic hermetic products are designed to meet or exceed the demanding Class B reliability levels of MIL-STD-883, paragraph 1.2.1.

Product flow and test procedures for all monolithic hermetic military grade products are in accordance with the latest revision and notice of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with tight controls and inspections to ensure that products meet the requirements for 100% screening. Routine quality conformance lot testing is performed as defined in MIL-STD-883, Methods 5004 and 5005.

For IDT module products, screening of the fully assembled substrates is performed, in addition to the monolithic level screening, to assure package integrity and mechanical reliability. All modules receive 100% electrical tests (DC, functional and dynamic switching) to ensure compliance with the "subsystem" specifications.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that commercial, industrial and military grade products consistently meet customer requirements for quality, reliability and performance.

SPECIAL PROGRAMS

Class S. IDT also has all manufacturing, screening and test capabilities in-house (except X-ray and some Group D tests) to perform complete Class S processing per MIL-STD-883 on all IDT products and has supplied Class S products on several programs.

Radiation Hardened. IDT has developed and supplied several levels of radiation hardened products for military/aerospace applications to perform at various levels of dose rate, total dose, single event upset (SEU), upset and latchup. IDT products maintain nearly their same high-performance levels built to these special process requirements. The company has in-house radiation testing capability used both in process development and testing of deliverable product. IDT also has a separate group within the company dedicated to supplying products for radiation hardened applications and to continue research and development of process and products to further improve radiation hardening capabilities.

QSP–QUALITY, SERVICE AND PERFORMANCE

Quality from the beginning, is the foundation for IDT's commitment to supply consistently high-quality products to our customers. IDT's quality commitment is embodied in its all pervasive Total Quality Commitment (TQC) process. Everyone who influences the quality of the product–from the designer to the shipping clerk–is committed to constantly improving the quality of their actions.

IDT QUALITY PHILOSOPHY

"To make quantitative constant improvement in the quality of our actions that result in the supply of leadership products in conformance to the requirements of our customers."

IDT's ASSURANCE STRATEGY FOR TQC

Measurable standards are essential to the success of TQC. All the processes contributing to the final quality of the product need to be monitored, measured and improved upon through the use of statistical tools.

PRODUCT FLOW

DEVELOPMENT
|
FAB
|
ASSEMBLY
|
TEST
|
SHIP

Our customers receive the benefit of our optimized systems. Installed to enhance quality and reliability, these systems provide accurate and timely reporting on the effectiveness of manufacturing controls and the reliability and quality performance of IDT products and services.

SERVICE FLOW

ORDER ENTRY
|
PRODUCTION CONTROL
|
SHIPPING
|
CUSTOMER SUPPORT

These systems and controls concentrate on TQC by focusing on the following key elements:

Statistical Techniques
Using statistical techniques, including Statistical Process Control (SPC) to determine whether the product/ processes are under control.

Standardization
Implementing policies, procedures and measurement techniques that are common across different operational areas.

Documentation
Documenting and training in policies, procedures, measurement techniques and updating through characterization/ capability studies.

Productivity Improvement
Using constant improvement teams made up from employees at all levels of the organization.

Leadership
Focusing on quality as a key business parameter and strategic strength.

Total Employee Participation
Incorporating the TQC process into the IDT Corporate Culture.

Customer Service
Supporting the customer, as a partner, through performance review and pro-active problem solving.

People Excellence
Committing to growing, motivating and retaining people through training, goal setting, performance measurement and review.

PRODUCT FLOW

Product quality starts here. IDT has mechanisms and procedures in place that monitor and control the quality of our development activities. From the calibration of design capture libraries through process technology and product characterization that establish whether the performance, ratings and reliability criteria have been met. This includes failure analysis of parts that will improve the prototype product.

At the pre-production stage once again in-house qualification tests assure the quality and reliability of the product. All specifications and manufacturing flows are established and personnel trained before the product is placed into production.

Manufacturing
To accomplish continuous improvement during the manufacturing stage, control items are determined for major manufacturing conditions. Data is gathered and statistical techniques are used to control specific manufacturing processes that affect the quality of the product.

In-process and final inspections are fed back to earlier processes to improve product quality. All product is burned-in (where applicable) before 100% inspection of electrical characteristics takes place.

Products which pass final inspection are then subject to Quality Assurance and Reliability Tests. This data is used to improve manufacturing processes and provide reliability predictions of field applications.

Inventory and Shipping

Controls in shipping focus on ensuring parts are identified and packaged correctly. Care is also taken to see that the correct paperwork is present and the product being shipped was processed correctly.

SERVICE FLOW

Quality not only applies to the product but to the quality -of -service we give our customers. Services is also constantly monitored for improvement.

Order Procedures

Checks are made at the order entry stage to ensure the correct processing of the Customer's product. After verification and data entry the Acknowledgements (sent to Customers) are again checked to ensure details are correct. As part of the TQC process, the results of these verifications are analyzed using statistical techniques and corrective actions are taken.

Production Control

Production Control (P.C.) is responsible for the flow and logistics of material as it moves through the manufacturing processes. The quality of the actions taken by P.C. greatly impinges on the quality of service the customer receives. Because many of our customers have implemented Just-in-Time (JIT) manufacturing practices, IDT as a supplier also has to adopt these same disciplines. As a result, employees receive extensive training and the performance level of key actions are kept under constant review. These key actions include:

Quotation response and accuracy.
Scheduling response and accuracy.
Response and accuracy of Expedites.
Inventory, management, and effectiveness.
On time delivery.

Customer Support

IDT has a worldwide network of sales offices and Technical Development Centers. These provide local customer support on business transactions, and in addition, support customers on applications information, technical services, benchmarking of hardware solutions, and demonstration of various Development Workstations.

The key to continuous improvement is the timely resolution of defects and implementation of the corrective actions. This is no more important than when product failures are found by a customer. When failures are found at the customer's incoming inspection, in the production line, or the field application, the Division Quality Assurance group is the focal point for the investigation of the cause of failure and implementation of the corrective action. IDT constantly improves the level of support we give our customers by monitoring the response time to customers that have detected a product failure. Providing the customer with an analysis of the failure, including corrective actions and the statistical analysis of defects, brings CQI full circle–full support of our customers and their designs with high-quality products.

SUMMARY

In 1990, IDT made the commitment to *"Leadership through Quality, Service, and Performance Products".*

We believe by following that credo IDT and our cusotmers will be successful in the coming decade.With the implementation of the TQC strategy within the company, we will satisfy our goal...

"Leadership through Quality, Service and Performance Products".

IDT QUALITY CONFORMANCE PROGRAM

A COMMITMENT TO QUALITY

Integrated Device Technology's monolithic assembly products are designed, manufactured and tested in accordance with the strict controls and procedures required by Military Standards. The documentation, design and manufacturing criteria of the Quality and Reliability Assurance Program were developed and are being maintained to the most current revisions of MIL-38510 as defined by paragraph 1.2.1 of MIL-STD-883 and MIL-STD-883 requirements.

Product flow and test procedures for all Class B *monolithic* hermetic Military Grade microcircuits are in full compliance with paragraph 1.2.1 of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with stringent controls and inspections to ensure that products meet the requirements for 100% screening and quality conformance tests as defined in MIL-STD-883, Methods 5004 and 5005.

Product flow and test procedures for all *plastic* and *commercial hermetic* products are in accordance with industry practices for producing highly reliable microcircuits to ensure that products meet the IDT requirements for 100% screening and quality conformance tests.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that our products consistently meet customer requirements for quality, reliability and performance.

SUMMARY

Monolithic Hermetic Package Processing Flow[1]

Refer to the Monolithic Hermetic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die Visual Inspection:** Wafers are cut and separated and the individual die are 100% visually inspected to strict IDT-defined internal criteria.

3. **Die Shear Monitor:** To ensure die attach integrity, product samples are routinely subjected to a shear strength test per Method 2019.

4. **Wire Bond Monitor:** Product samples are routinely subjected to a strength test per Method 2011, Condition D, to ensure the integrity of the lead bond process.

5. **Pre-Cap Visual:** Before the completed package is sealed, 100% of the product is visually inspected to Method 2010, Condition B criteria.

6. **Environmental Conditioning:** 100% of the sealed product is subjected to environmental stress tests. These thermal and mechanical tests are designed to eliminate units with marginal seal, die attach or lead bond integrity.

7. **Hermetic Testing:** 100% of the hermetic packages are subjected to fine and gross leak seal tests to eliminate marginally sealed units or units whose seals may have become defective as a result of environmental conditioning tests.

8. **Pre-Burn-In Electrical Test:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

9. **Burn-In:** 100% of the Military Grade product is burned-in under dynamic electrical conditions to the time and temperature requirements of Method 1015, Condition D. Except for the time, Commercial Grade product is burned-in as applicable to the same conditions as Military Grade devices.

10. **Post-Burn-In Electrical:** After burn-in, 100% of the Class B Military Grade product is electrically tested to IDT data sheet or customer specifications over the –55°C to +125°C temperature range. Commercial Grade products are sample tested to the applicable temperature extremes.

11. **Mark:** All product is marked with product type and lot code identifiers. MIL-STD-883 compliant Military Grade products are identified with the required compliant code letter.

12. **Quality Conformance Tests:** Samples of the Military Grade product which have been processed to the 100% screening tests of Method 5004 are routinely subjected to the quality conformance requirements of Method 5005.

3

NOTE:
1. For quality requirements beyond Class B levels such as SEM analysis, X-Ray inspection, Particle Impact Noise Reduction (PIND) test, Class S screening or other customer specified screening flows, please contact your Integrated Device Technology sales representative.

SUMMARY

Monolithic Plastic Package Processing Flow

Refer to the Monolithic Plastic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Topside silicon nitride passivation is all applied to all wafers for better moisture barrier characteristics.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die Visual Inspection:** Wafers are 100% visually inspected to strict IDT defined internal criteria.

3. **Die Push Test:** To ensure die attach integrity, product samples are routinely subjected to die push tests, patterned after MIL-STD-883, Method 2019.

4. **Wire Bond Monitor:** Product samples are routinely subjected to wire bond pull and ball shear tests to ensure the integrity of the wire bond process, patterned after MIL-STD-883, Method 2011, Condition D.

5. **Pre-Cap Visual:** Before encapsulation, all product lots are visually inspected (using LTPD 5 sampling plan) to criteria patterned after MIL-STD-883, Method 2010, Condition B.

6. **Post Mold Cure:** Plastic encapsulated devices are baked to ensure an optimum polymerization of the epoxy mold compound so as to enhance moisture resistance characteristics.

7. **Pre-Burn-In Electrical:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

8. **Burn-In:** Except for MSI Logic family devices where it may be obtained as an option, all Commercial Grade plastic package products are burned-in for 16 hours at +125°C minimum (or equivalent), utilizing the same burn-in conditions as the Military Grade product.

9. **Post-Burn-In Electrical:** After burn-in, 100% of the plastic product is electrically tested to IDT data sheet or customer specifications at the maximum temperature extreme. The minimum temperature extreme is tested periodically on an audit basis.

10. **Mark:** All product is marked with product type and lot code identifiers. Products are identified with the assembly and test locations.

11. **Quality Conformance Inspection:** Samples of the plastic product which have been processed to the 100% screening requirements are subjected to the Periodic Quality Conformance Inspection Program. Where indicated, the test methods are patterned after MIL-STD-883 criteria.

TABLE 1

This table defines the device class screening procedures for IDT's high reliability products in conformance with MIL-STD-883C.

Monolithic Hermetic Package Final Processing Flow

	CLASS-S		CLASS-B		CLASS-C(1)	
OPERATION	**TEST METHOD**	**RQMT**	**TEST METHOD**	**RQMT**	**TEST METHOD**	**RQMT**
BURN-IN	1015 Cond. D, 240 Hrs @ 125°C or equivalent	100%	1015 Cond. D, 160 Hrs. @ 125°C min. or equivalent	100%	Per applicable device specification	100%
PORT BURN-IN ELECTRICAL: Static (DC), Functional and Switching (AC)	Per applicable device specification +25, –55 and 125°C	100%	Per applicable device specification +25, –55 and 125°C	100%	Per applicable (2) device specification	100%
Group A ELECTRICAL: Static (DC, Functional and Switching (AC)	Per applicable device specification and 5005	Sample	Per applicable device specification and 5005	Sample	Per applicable (2) device specification	Sample
MARK/LEAD STRAIGHTENING	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%
FINAL ELECTRICAL TEST	Per applicable device specification +25°C	100%	Per applicable device specification +25°C	100%	Per applicable device specification +25°C	100%
FINAL VISUAL/PACK	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%
QUALITY CONFORMANCE INSPECTION	5005 Group B, C, D	Sample	5005 Group B, C, D	Sample	IDT Spec	Sample
QUALITY SHIPPING INSPECTION (Visual/Plant Clearance)	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%

NOTES:
1. Class-C = IDT commercial spec. for hermetic and plastic packages
2. Typical 0°C, 70°C, Extended -55°C +125°C

3

RADIATION TOLERANT/ENHANCED/HARDENED PRODUCTS FOR RADIATION ENVIRONMENTS

INTRODUCTION

The need for high-performance CMOS integrated circuits in military and space systems is more critical today than ever before. The low power dissipation that is achieved using CMOS technology, along with the high complexity and density levels, makes CMOS the nearly ideal component for all types of applications.

Systems designed for military or space applications are intended for environments where high levels of radiation may be encountered. The implication of a device failure within a military or space system clearly is critical. IDT has made a significant contribution toward providing reliable radiation-tolerant systems by offering integrated circuits with enhanced radiation tolerance. Radiation environments, IDT process enhancements and device tolerance levels achieved are described below.

THE RADIATION ENVIRONMENT

There are four different types of radiation environments that are of concern to builders of military and space systems. These environments and their effects on the device operation, summarized in Figure 1, are as follows:

Total Dose Accumulation refers to the total amount of accumulated gamma rays experienced by the devices in the system, and is measured in RADS (SI) for radiation units experienced at the silicon level. The physical effect of gamma rays on semiconductor devices is to cause threshold shifts (Vt shifts) of both the active transistors as well as the parasitic field transistors. Threshold voltages decrease as total dose is accumulated; at some point, the device will begin to exhibit parametric failures as the input/output and supply currents increase. At higher radiation accumulation levels, functional failures occur. In memory circuits, however, functional failures due to memory cell failure often occur first.

Burst Radiation or Dose Rate refers to the amount of radiation, usually photons or electrons, experienced by the devices in the system due to a pulse event, and is measured in RADS (Si) per second. The effect of a high dose rate or burst of radiation on CMOS integrated circuits is to cause temporary upset of logic states and/or CMOS latch-up. Latch-up can cause permanent damage to the device.

Single Event Upset (SEU) is a transient logic state change caused by high-energy ions, such as energetic cosmic rays, striking the integrated circuits. As the ion passes through the silicon, charge is either created through ionization or direct nuclear collision. If collected by a circuit node, this excess charge can cause a change in logic state of the circuit. Dynamic nodes that are not actively held at a particular logic state (dynamic RAM cells for example) are the most susceptible. These upsets are transient, but can cause system failures known as "soft errors."

Neutron Irradiation will cause structural damage to the silicon lattice which may lead to device leakage and, ultimately, functional failure.

DEVICE ENHANCEMENTS

Of the four radiation environments above, IDT has taken considerable data on the first two, Total Dose Accumulation and Dose Rate. IDT has developed a process that significantly improves the radiation tolerance of its devices within these environments. Prevention of SEU failures is usually accomplished by system-level considerations, such as Error Detection and Correction (EDC) circuitry, since the occurrence of SEUs is not particularly dependent on process technology. Through IDT's customer contracts, SEU has been gathered on some devices. Little is yet known about the effects of neutron-induced damage. For more information on SEU testing, contact IDT's Radiation Hardened Product Group.

Radiation Category	Primary Particle	Source	Effect
Total Dose	Gamma	Space or Nuclear Event	Permanent
Dose Rate	Photons	Nuclear Event	Temporary Upset of Logic State or Latch-up
SEU	Cosmic Rays	Space	Temporary Upset of Logic State
Neutron	Neutrons	Nuclear Event	Device Leakage Due to Silicon Lattice Damage

2510 drw 01

Figure 1.

Enhancements to IDT's standard process are used to create radiation enhanced and tolerant processes. Field and gate oxides are "hardened" to make the device less susceptible to radiation damage by modifying the process architecture to allow lower temperature processing. Device implants and Vts adjustments allow more Vt margin. In addition to process changes, IDT's radiation enhanced process utilizes epitaxial substrate material. The use of epi substrate material provides a lower substrate resistance environment to create latch-up free CMOS structures.

RADIATION HARDNESS CATEGORIES

Radiation Enhanced (RE) or Radiation Tolerant ('RT) versions of IDT products follow IDT's military product data sheets whenever possible (consult factory). IDT's Total Dose Test plan exposes a sample of die on a wafer to a particular Total Dose level via ARACOR X-Ray radiation. This Total Dose Test plan qualifies each 'RE or 'RT wafer to a Total Dose level. Only wafers with sampled die that pass Total Dose level tests are assembled and used for orders (consult factory for more details on Total Dose sample testing). With regard to Total Dose testing, clarifications/exceptions to MIL-STD-883, Methods 5005 and 1019 are required. Consult factory for more details.

The 'RE and 'RT process enhancements enable IDT to offer integrated circuits with varying grades of radiation tolerance or radiation "hardness".

- Radiation Enhanced process uses Epi wafers and is able to provide devices that can be Total Dose qualified to 10K RADs (Si) or greater by IDT's ARACOR X-Ray Total Dose sample die test plan (Total Dose levels require negotiation, consult factory for more details).
- Radiation Tolerant product uses standard wafer/process material that is qualified to 10K RADs (Si) Total Dose by IDT's ARACOR X-Ray Total Dose sample die test plan.

Integrated Device Technology can provide Radiation Tolerant/Enhanced versions of all product types (some speed grades may not be available as 'RE).

Please contact your IDT sales representative or factory marketing to determine availability and price of any IDT product processed in accordance with one of these levels of radiation hardness.

CONCLUSION

There has been widespread interest within the military and space community in IDT's CMOS product line for its radiation hardness levels, as well as its high-performance and low power dissipation. To serve this growing need for CMOS circuits that must operate in a radiation environment, IDT has created a separate group within the company to concentrate on supplying products for these applications.Continuing research and development of process and products, including the use of in-house radiation testing capability, will allow Integrated Device Technology to offer continuously increasing levels of radiation-tolerant solutions.

THERMAL PERFORMANCE CALCULATIONS FOR IDT'S PACKAGES

Since most of the electrical energy consumed by microelectronic devices eventually appears as heat, poor thermal performance of the device or lack of management of this thermal energy can cause a variety of deleterious effects. This device temperature increase can exhibit itself as one of the key variables in establishing device performance and long term reliability; on the other hand, effective dissipation of internally generated thermal energy can, if properly managed, reduce the deleterious effects and improve component reliability.

A few key benefits of IDT's enhanced CMOS process are: low power dissipation, high speed, increased levels of integration, wider operating temperature ranges and lower quiescent power dissipation. Because the reliability of an integrated circuit is largely dependent on the maximum temperature the device attains during operation, and as the junction stability declines with increases in junction temperature (T_J), it becomes increasingly important to maintain a low (T_J).

CMOS devices stabilize more quickly and at greatly lower temperature than bipolar devices under normal operation. The accelerated aging of an integrated circuit can be expressed as an exponential function of the junction temperature as:

$$t_A = t_o \exp\left[\frac{E_a}{k}\left(\frac{1}{T_O} - \frac{1}{T_J}\right)\right]$$

where

t_A = lifetime at elevated junction (T_J) temperature
t_o = normal lifetime at normal junction (T_O) temperature
E_a = activation energy (ev)
k = Boltzmann's constant (8.617 x 10^{-5}ev/k)

i.e. the lifetime of a device could be decreased by a factor of 2 for every 10°C increase temperature.

To minimize the deleterious effects associated with this potential increase, IDT has:

1. Optimized our proprietary low-power CMOS fabrication process to ensure the active junction temperature rise is minimal.
2. Selected only packaging materials that optimize heat dissipation, which encourages a cooler running device.
3. Physically designed all package components to enhance the inherent material properties and to take full advantage of heat transfer and radiation due to case geometries.
4. Tightly controlled the assembly procedures to meet or exceed the stringent criteria of MIL-STD-883_ to ensure maximum heat transfer between die and packaging materials.

The following figures graphically illustrate the thermal values of IDT's current package families. Each envelop (shaded area) depicts a typical spread of values due to the influence of a number of factors which include: circuit size, package materials and package geometry. The following range of values are to be used as a comprehensive characterization of the major variables rather than single point of reference.

When calculating junction temperature (T_J), it is necessary to know the thermal resistance of the package (θ_{JA}) as measured in "degree celsius per watt". With the accompanying data, the following equation can be used to establish thermal performance, enhance device reliability and ultimately provide you, the user, with a continuing series of high-speed, low-power CMOS solutions to your system design needs.

$$\theta_{JA} = [T_J - T_A]/P$$
$$T_J = T_A + P[\theta_{JA}] = T_A + P[\theta_{JC} + \theta_{CA}]$$

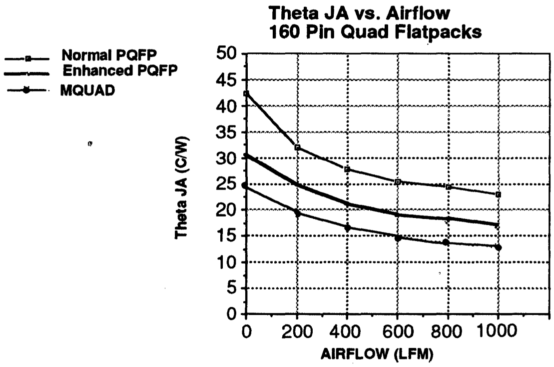
where

$$\theta_{JC} = \frac{T_J - T_C}{P} \qquad \theta_{CA} = \frac{T_C - T_A}{P}$$

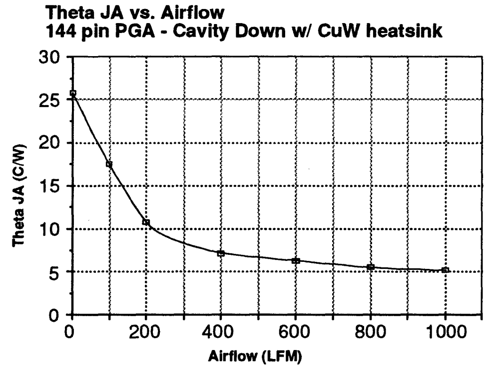
θ = Thermal resistance
J = Junction
P = Operational power of device (dissipated)
T_A = Ambient temperature in degree celsius
T_J = Temperature of the junction
T_C = Temperature of case/package
θ_{CA} = Case to Ambient, thermal resistance—usually a measure of the heat dissipation due to natural or forced convection, radiation and mounting techniques.
θ_{JC} = Junction to Case, thermal resistance—usually measured with reference to the temperature at a specific point on the package (case) surface. (Dependent on the package material properties and package geometry.)
θ_{JA} = Junction to Ambient, thermal resistance—usually measured with respect to the temperature of a specified volume of still air. (Dependent on θ_{JC} + θ_{JA} which includes the influence of area and environmental condition.)

4

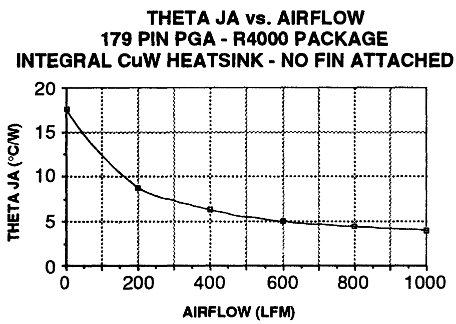
Ref. MIL-STD-883C, Method 1012.1
JEDEC ENG. Bulletin No. 20, January 1975
1986 Semi. Std., Vol. 4, Test Methods G30–86, G32–86.



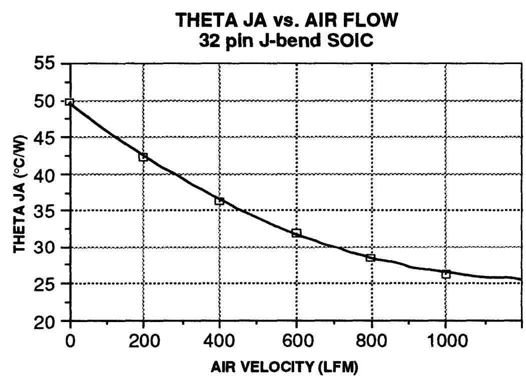
Delco Temp 09 Thermal Die (.250"sq.)
Parts mounted to standard 3" sq. test board.



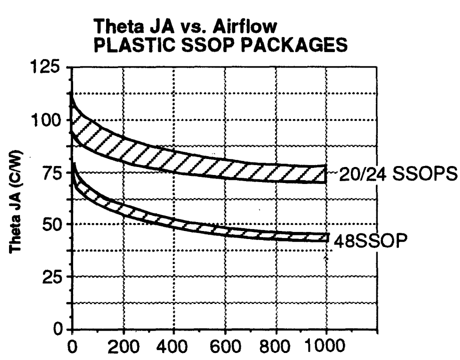
Measurements done with Delco Temp09 Thermal Die (.250"sq.)



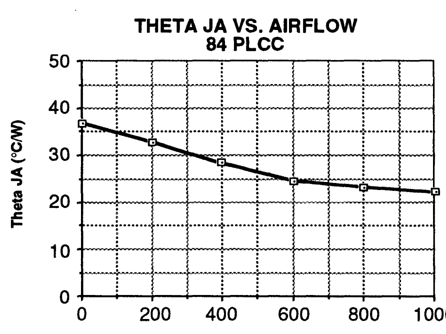
Delco Temp09 Thermal Die Array (.500"sq.)
applied power = 3W



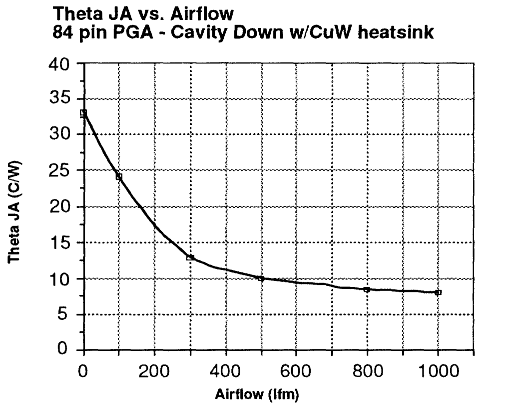
Theta JC was measured to be 17°C/W - Die size (.150"x.250")



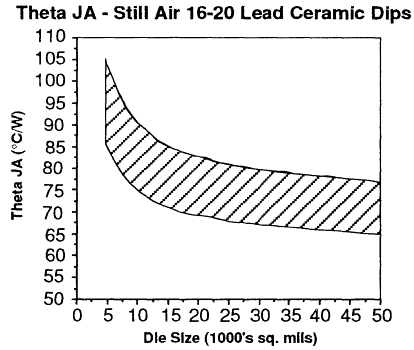
THETA JC : 20/24 PIN = 35-40 °C/W
48 PIN = 16-20 °C/W

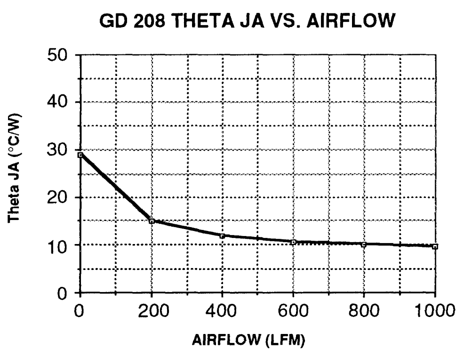


Delco Temp09 Thermal Die (.250"sq.)

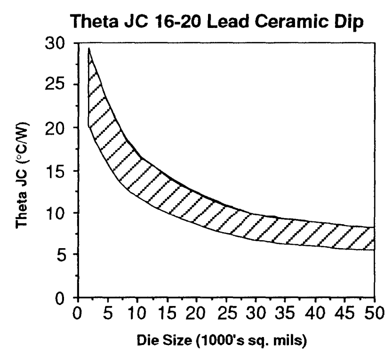


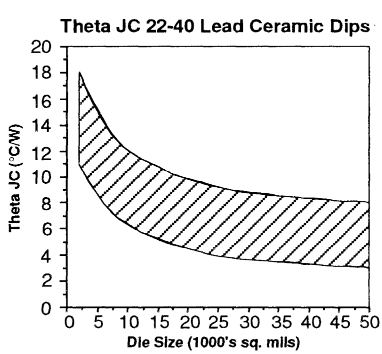
Measurements were done using Temp09 Delco Thermal Die (.250sq.)

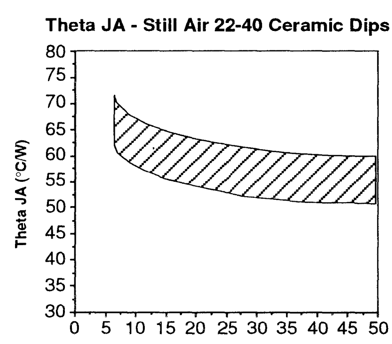




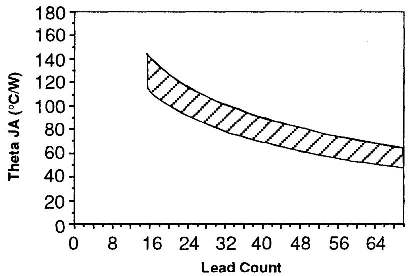
Delco Temp09 Thermal Die (.250"sq.)



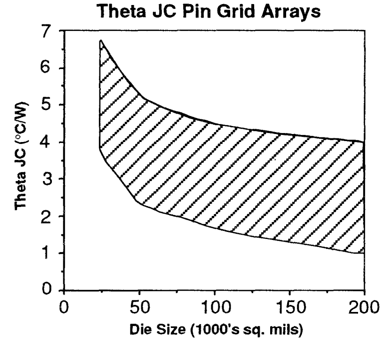




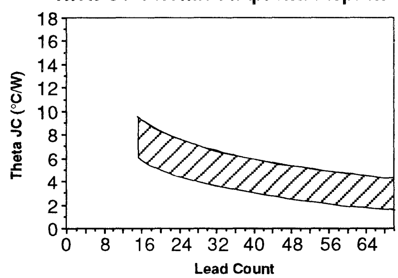
Theta JA Ceramic Flatpacks/Cerpacks



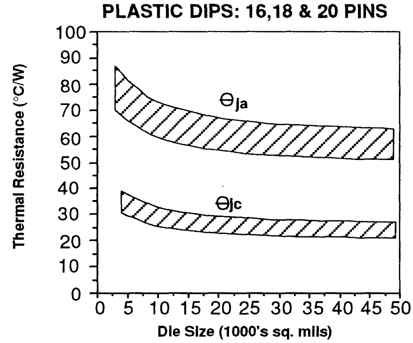
Theta JC Pin Grid Arrays



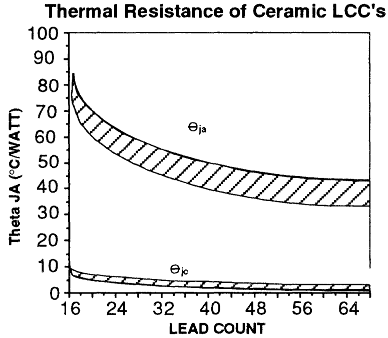
Theta JC Ceramic Flatpacks/Cerpacks



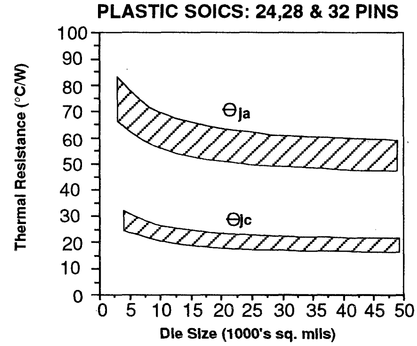
PLASTIC DIPS: 16,18 & 20 PINS

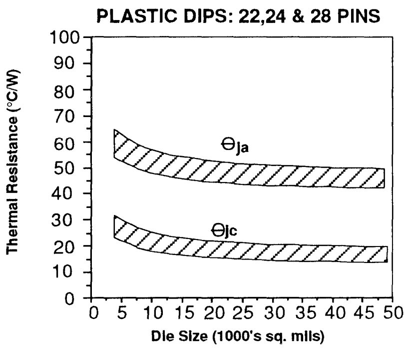


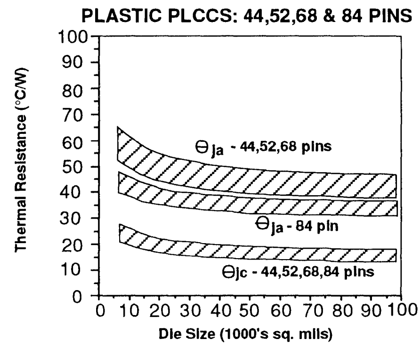
Thermal Resistance of Ceramic LCC's

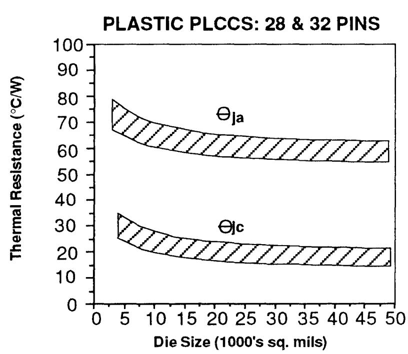


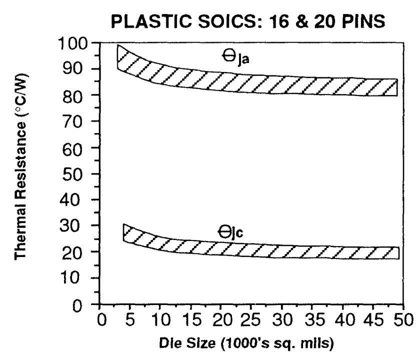
PLASTIC SOICS: 24,28 & 32 PINS

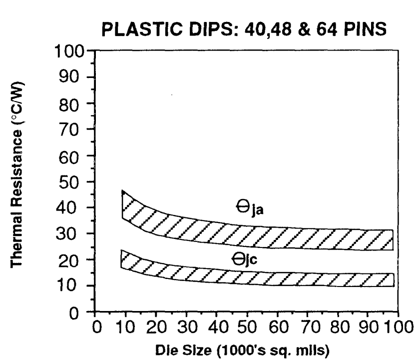


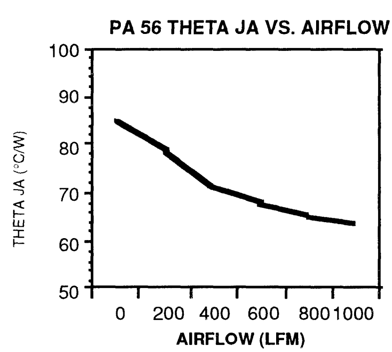

PLASTIC DIPS: 22,24 & 28 PINS
Thermal Resistance (°C/W)
Θja
Θjc
Die Size (1000's sq. mils)


PLASTIC PLCCS: 44,52,68 & 84 PINS
Thermal Resistance (°C/W)
Θja - 44,52,68 pins
Θja - 84 pin
Θjc - 44,52,68,84 pins
Die Size (1000's sq. mils)


PLASTIC PLCCS: 28 & 32 PINS
Thermal Resistance (°C/W)
Θja
Θjc
Die Size (1000's sq. mils)

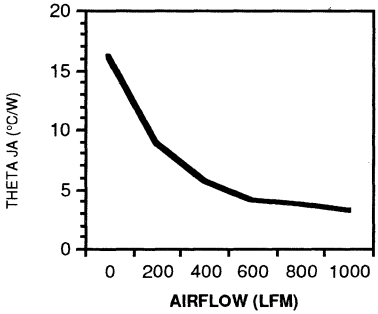

PLASTIC SOICS: 16 & 20 PINS
Thermal Resistance (°C/W)
Θja
Θjc
Die Size (1000's sq. mils)


PLASTIC DIPS: 40,48 & 64 PINS
Thermal Resistance (°C/W)
Θja
Θjc
Die Size (1000's sq. mils)

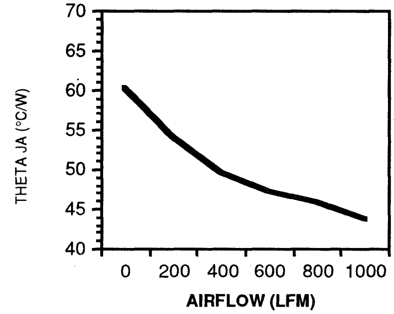

PA 56 THETA JA VS. AIRFLOW
THETA JA (°C/W)
AIRFLOW (LFM)

4

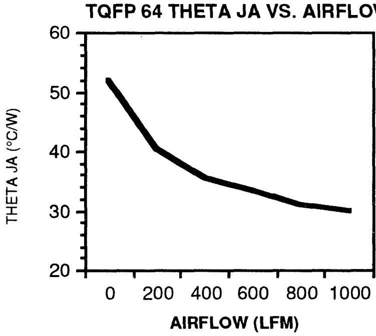
GD 447 THETA JA VS. AIRFLOW



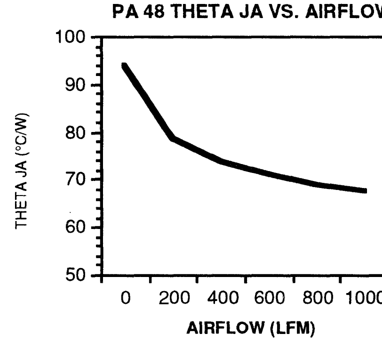
PV 56 THETA JA VS. AIRFLOW



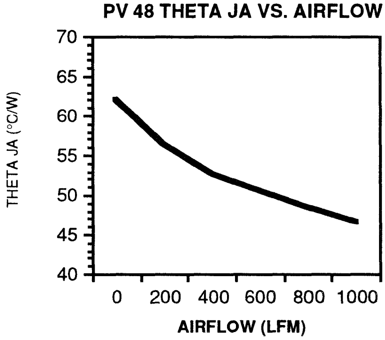
TQFP 64 THETA JA VS. AIRFLOW



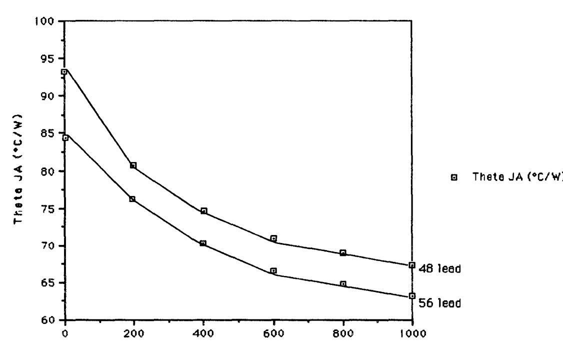
PA 48 THETA JA VS. AIRFLOW



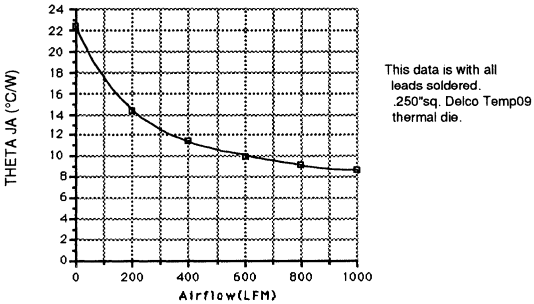
PV 48 THETA JA VS. AIRFLOW



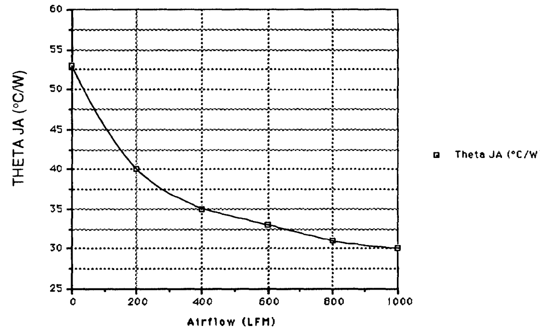
Theta JA vs. Airflow
48/56 lead (.150 body) SSOP



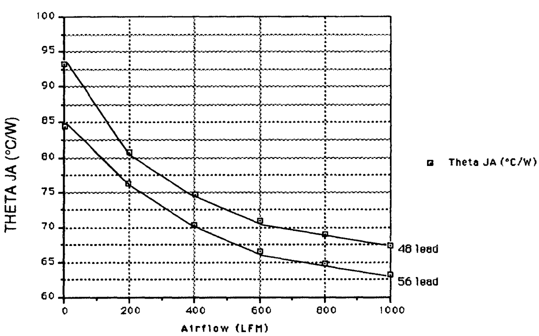
Theta JA vs. Airflow
84/160/208 lead MQUAD flatpack
28mm body



Theta JA vs. Airflow
64/80/100 lead Thin Quad Flatpack
(14mm body)

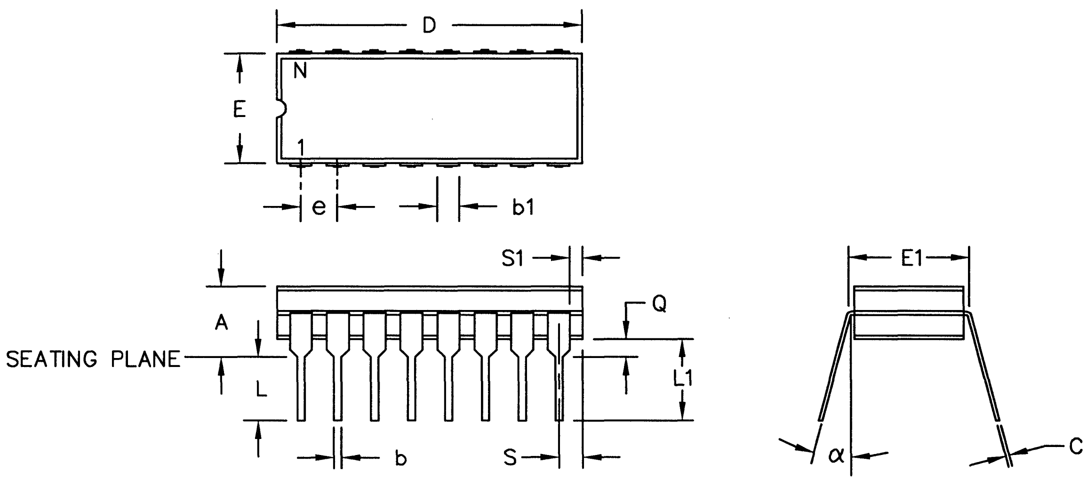


Theta JA vs. Airflow
48/56 lead (.150 body) SSOP



PACKAGE DIAGRAM OUTLINE INDEX

DUAL IN-LINE PACKAGES



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC — BASIC LEAD SPACING BETWEEN CENTERS.
3. THE MINIMUM LIMIT FOR DIMENSION b1 MAY BE .023 FOR CORNER LEADS.

16–28 LEAD CERDIP (300 MIL)

DWG #	D16–1		D18–1		D20–1		D22–1		D24–1		D28–3	
# OF LDS (N)	16		18		20		22		24		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.200	.140	.200	.140	.200	.140	.200	.140	.200	.140	.200
b	.015	.021	.015	.021	.015	.021	.015	.021	.015	.021	.015	.021
b1	.045	.060	.045	.060	.045	.060	.045	.060	.045	.065	.045	.065
C	.009	.012	.009	.012	.009	.012	.009	.012	.009	.014	.009	.014
D	.750	.830	.880	.930	.935	1.060	1.050	1.080	1.240	1.280	1.440	1.485
E	.285	.310	.285	.310	.285	.310	.285	.310	.285	.310	.285	.310
E1	.290	.320	.290	.320	.290	.320	.300	.320	.300	.320	.300	.320
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.015	.055	.015	.055	.015	.060	.015	.060	.015	.060	.015	.060
S	.020	.080	.020	.080	.020	.080	.020	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°

DUAL IN-LINE PACKAGES (Continued)

24–40 LEAD CERDIP (400 & 600 MIL)

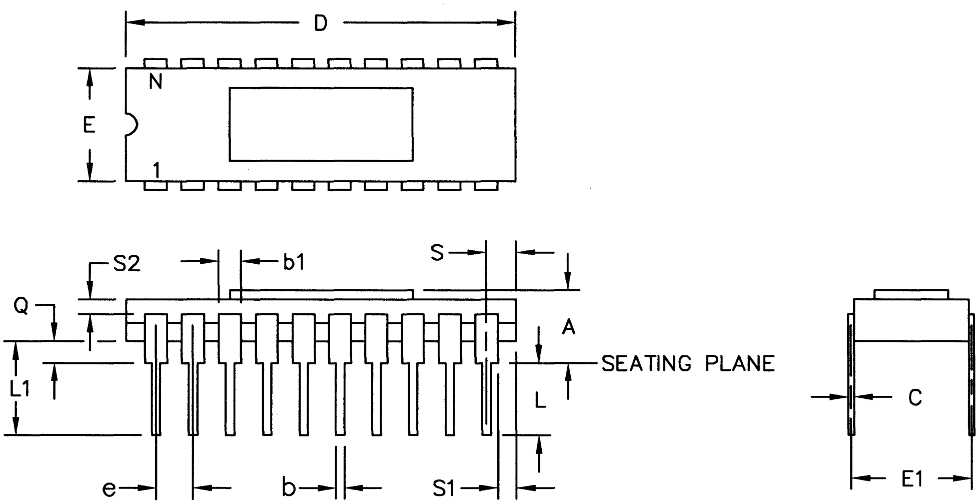
DWG #	D24–3		D24–2		D28–1		D40–1	
# OF LDS (N)	24		24		28		40	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.130	.175	.090	.190	.090	.200	.160	.220
b	.015	.021	.014	.023	.014	.023	.014	.023
b1	.045	.065	.045	.060	.045	.065	.045	.065
C	.009	.014	.008	.012	.008	.014	.008	.014
D	1.180	1.250	1.230	1.290	1.440	1.490	2.020	2.070
E	.350	.410	.500	.610	.510	.600	.510	.600
E1	.380	.420	.590	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.175	.125	.200	.125	.200	.125	.200
L1	.150	–	.150	–	.150	–	.150	–
Q	.015	.060	.015	.060	.020	.060	.020	.060
S	.030	.070	.030	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°	0°	15°

32 LEAD CERDIP (WIDE BODY)

DWG #	D32–1	
# OF LDS (N)	32	
SYMBOL	MIN	MAX
A	.120	.210
b	.014	.023
b1	.045	.065
C	.008	.014
D	1.625	1.675
E	.570	.600
E1	.590	.620
e	.100 BSC	
L	.125	.200
L1	.150	–
Q	.020	.060
S	.030	.080
S1	.005	–
α	0°	15°

DUAL IN-LINE PACKAGES (Continued)

20-32 LEAD SIDE BRAZE (300 MIL)

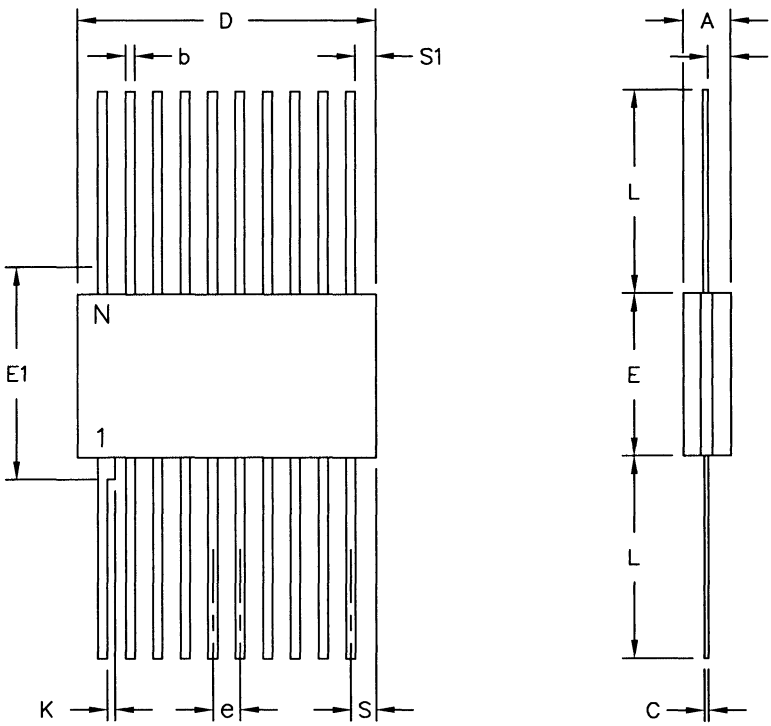


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C20-1		C22-1		C24-1		C28-1		C32-3	
# OF LDS (N)	20		22		24		28		32	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.100	.200	.090	.200	.090	.200	.090	.200
b	.014	.023	.014	.023	.015	.023	.014	.023	.014	.023
b1	.045	.060	.045	.060	.045	.060	.045	.060	.045	.060
C	.008	.015	.008	.015	.008	.015	.008	.015	.008	.014
D	.970	1.060	1.040	1.120	1.180	1.230	1.380	1.420	1.580	1.640
E	.260	.310	.260	.310	.220	.310	.220	.310	.280	.310
E1	.290	.320	.290	.320	.290	.320	.290	.320	.290	.320
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200	.125	.200	.100	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.015	.060	.015	.060	.015	.060	.015	.060	.030	.060
S	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–	.005	–	.005	–

CERPACKS

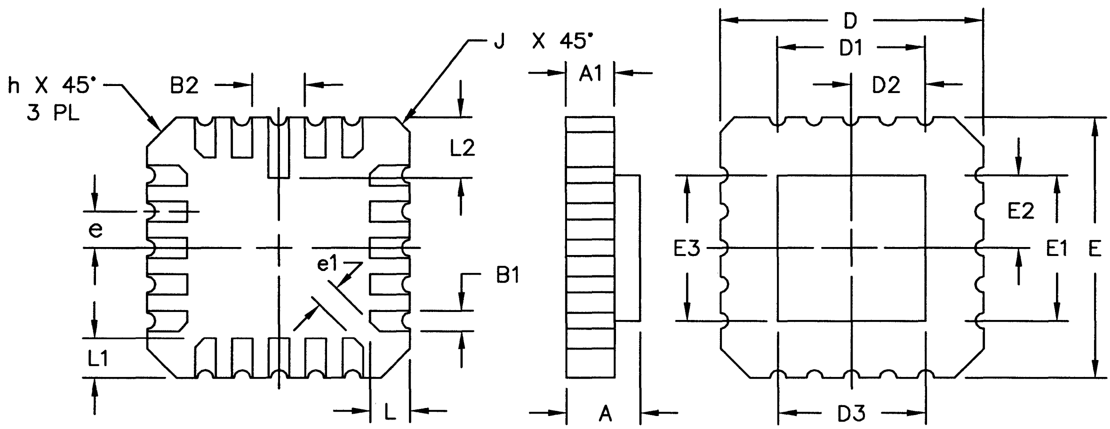
16–28 LEAD CERPACK



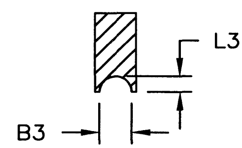
NOTES:
1. ALL DIMENSION ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	E16–1		E20–1		E24–1		E28–1		E28–2	
# OF LDS (N)	16		20		24		28		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.055	.085	.045	.092	.045	.090	.045	.115	.045	.090
b	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
C	.0045	.006	.0045	.006	.0045	.006	.0045	.006	.0045	.006
D	.370	.430	–	.540	–	.640	–	.740	–	.740
E	.245	.285	.245	.300	.300	.420	.460	.520	.340	.380
E1	–	.305	–	.305	–	.440	–	.550	–	.400
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
K	.008	.015	.008	.015	.008	.015	.008	.015	.008	.015
L	.250	.370	.250	.370	.250	.370	.250	.370	.250	.370
Q	.026	.040	.026	.040	.026	.040	.026	.045	.026	.045
S	–	.045	–	.045	–	.045	–	.045	–	.045
S1	.005	–	.005	–	.005	–	.000	–	.005	–

LEADLESS CHIP CARRIERS



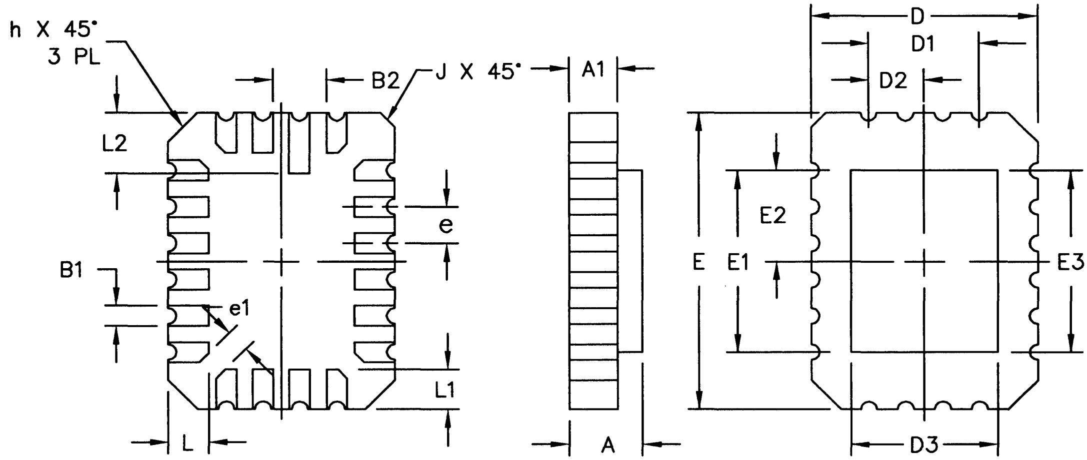
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.



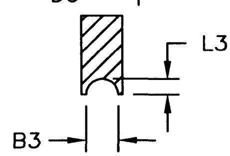
20–48 LEAD LCC (SQUARE)

DWG #	L20–2		L28–1		L44–1		L48–1	
# OF LDS (N)	20		28		44		48	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.064	.100	.064	.100	.064	.120	.055	.120
A1	.054	.066	.050	.088	.054	.088	.045	.090
B1	.022	.028	.022	.028	.022	.028	.017	.023
B2	.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022
D/E	.342	.358	.442	.460	.640	.660	.554	.572
D1/E1	.200 BSC		.300 BSC		.500 BSC		.440 BSC	
D2/E2	.100 BSC		.150 BSC		.250 BSC		.220 BSC	
D3/E3	–	.358	–	.460	–	.560	.500	.535
e	.050 BSC		.050 BSC		.050 BSC		.040 BSC	
e1	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.040 REF		.040 REF		.012 RADIUS	
J	.020 REF		.020 REF		.020 REF		.020 REF	
L	.045	.055	.045	.055	.045	.055	.033	.047
L1	.045	.055	.045	.055	.045	.055	.033	.047
L2	.077	.093	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015
ND/NE	5		7		11		12	

LEADLESS CHIP CARRIERS (Continued)



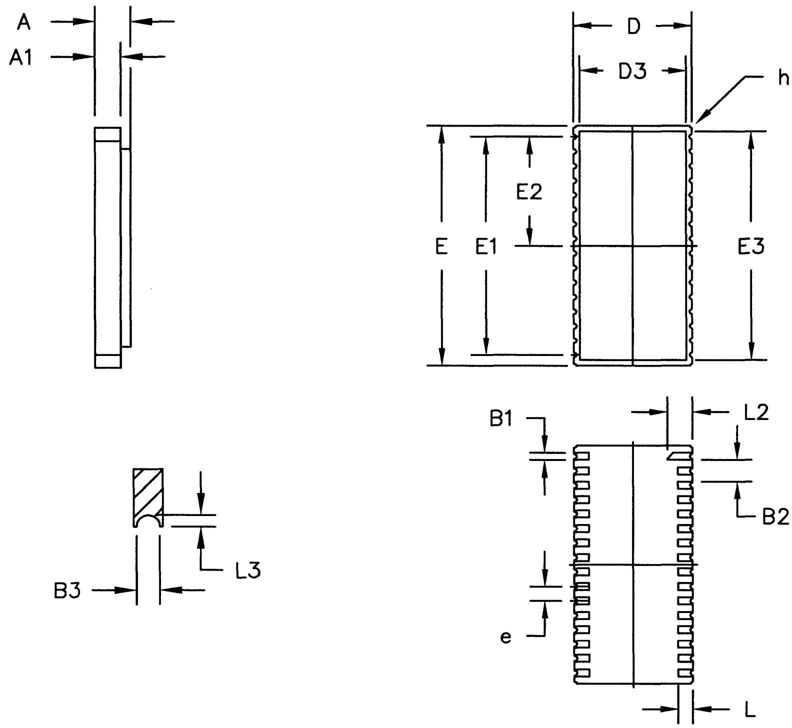
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.



20–32 LEAD LCC (RECTANGULAR)

DWG #	L20–1		L22–1		L24–1		L28–2		L32–1	
# OF LDS (N)	20		22		24		28		32	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.060	.075	.064	.100	.064	.120	.060	.120	.060	.120
A1	.050	.065	.054	.063	.054	.066	.050	.088	.050	.088
B1	.022	.028	.022	.028	.022	.028	.022	.028	.022	.028
B2	.072 REF		.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022	.006	.022
D	.284	.296	.284	.296	.292	.308	.342	.358	.442	.458
D1	.150 BSC		.150 BSC		.200 BSC		.200 BSC		.300 BSC	
D2	.075 BSC		.075 BSC		.100 BSC		.100 BSC		.150 BSC	
D3	–	.280	–	.280	–	.308	–	.358	–	.458
E	.420	.435	.480	.496	.392	.408	.540	.560	.540	.560
E1	.250 BSC		.300 BSC		.300 BSC		.400 BSC		.400 BSC	
E2	.125 BSC		.150 BSC		.150 BSC		.200 BSC		.200 BSC	
E3	–	.410	–	.480	–	.408	–	.558	–	.558
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
e1	.015	–	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.012 RADIUS		.025 REF		.040 REF		.040 REF	
J	.020 REF		.012 RADIUS		.015 REF		.020 REF		.020 REF	
L	.045	.055	.039	.051	.040	.050	.045	.055	.045	.055
L1	.045	.055	.039	.051	.040	.050	.045	.055	.045	.055
L2	.080	.095	.083	.097	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015	.003	.015
ND	4		4		5		5		7	
NE	6		7		7		9		9	

LEADLESS CHIP CARRIERS (Continued)



32 LD LCC (SMALL OUTLINE – RECTANGULAR)

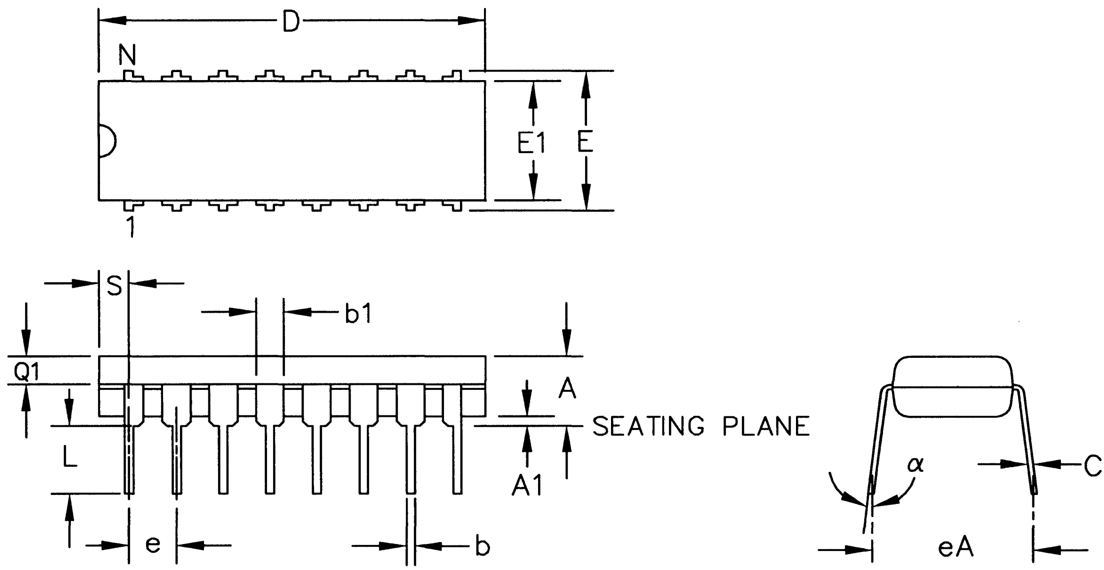
DWG #	L32–2	
# OF LDS (N)	32	
SYMBOL	MIN	MAX
A	.080	.100
A1	.060	.090
B1	.022	.028
B2	.072 REF	
B3	.006	.022
D	.392	.408
D3	–	.400
E	.800	.840
E1	.750 BSC	
E2	.375 BSC	
E3	–	.820
e	.050 BSC	
h	.008R REF	
L	.040	.060
L2	.075	.095
L3	.003	.015

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

PLASTIC DUAL IN-LINE PACKAGES

16–32 LEAD PLASTIC DIP (300 MIL)

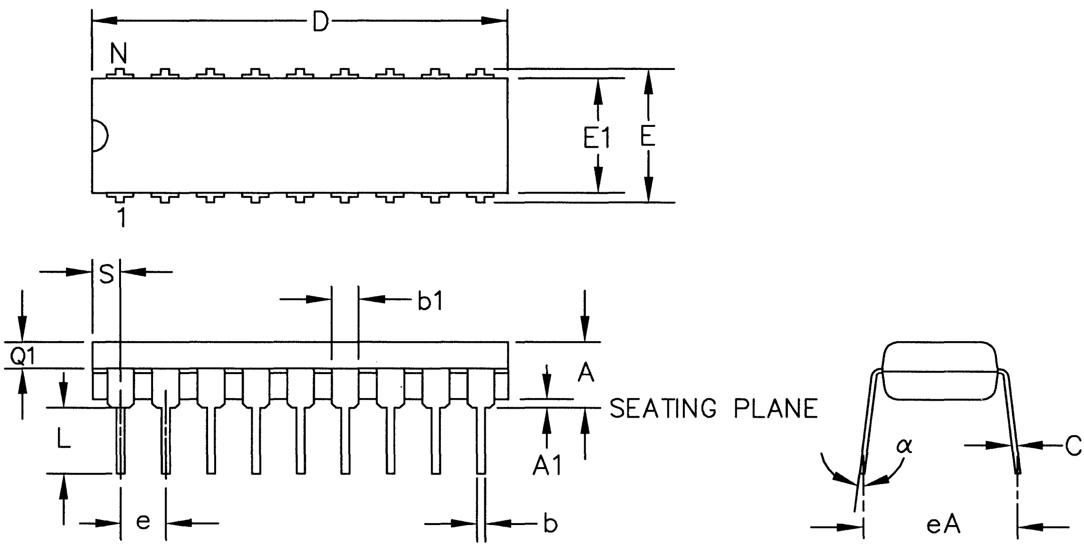


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG #	P16–1		P22–1		P28–2		P32–2	
# OF LDS (N)	16		22		28		32	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.165	.145	.165	.145	.180	.145	.180
A1	.015	.035	.015	.035	.015	.030	.015	.030
b	.015	.022	.015	.022	.015	.022	.016	.022
b1	.050	.070	.050	.065	.045	.060	.045	.060
C	.008	.012	.008	.012	.008	.015	.008	.015
D	.745	.760	1.050	1.060	1.345	1.385	1.545	1.585
E	.300	.325	.300	.320	.300	.325	.300	.325
E1	.247	.260	.240	.270	.270	.295	.275	.295
e	.090	.110	.090	.110	.090	.110	.090	.110
eA	.310	.370	.310	.370	.310	.400	.310	.400
L	.120	.150	.120	.150	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°	0°	15°
S	.015	.035	.020	.040	.020	.042	.020	.060
Q1	.050	.070	.055	.075	.055	.065	.055	.065

PLASTIC DUAL IN–LINE PACKAGES (Continued)

18–24 LEAD PLASTIC DIP (300 MIL – FULL LEAD)

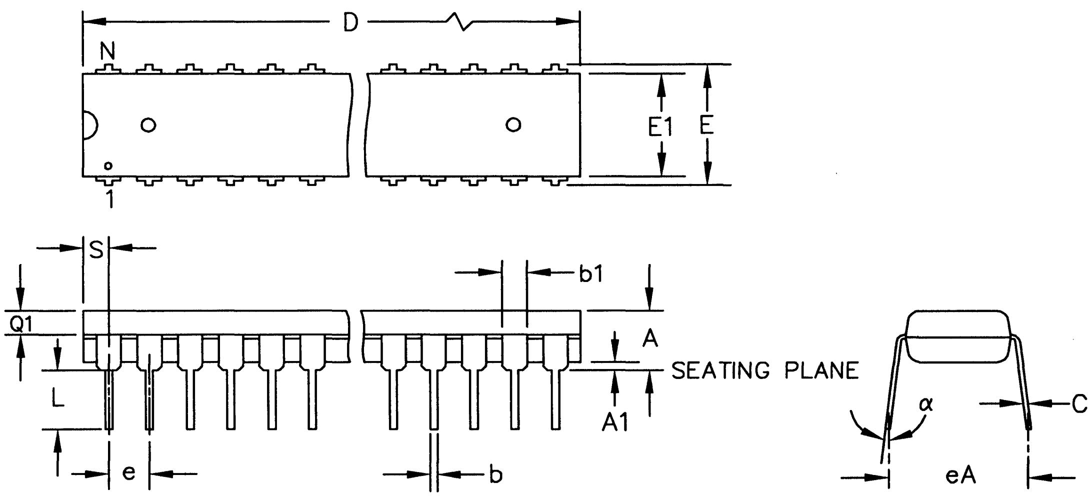


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG #	P18–1		P20–1		P24–1	
# OF LDS (N)	18		20		24	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.165	.145	.165	.145	.165
A1	.015	.035	.015	.035	.015	.035
b	.015	.020	.015	.020	.015	.020
b1	.050	.070	.050	.070	.050	.065
C	.008	.012	.008	.012	.008	.012
D	.885	.910	1.022	1.040	1.240	1.255
E	.300	.325	.300	.325	.300	.320
E1	.247	.260	.240	.280	.250	.275
e	.090	.110	.090	.110	.090	.110
eA	.310	.370	.310	.370	.310	.370
L	.120	.150	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°
S	.040	.060	.025	.070	.055	.075
Q1	.050	.070	.055	.075	.055	.070

PLASTIC DUAL IN-LINE PACKAGES (Continued)

28 & 32 LEAD PLASTIC DIP (400 MIL)

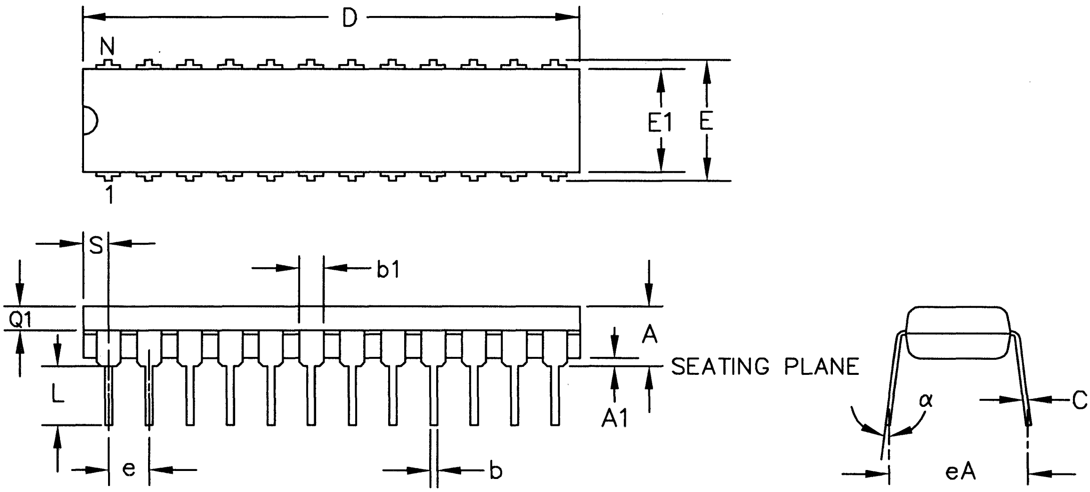


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG #	P28-3		P32-3	
# OF LEADS (N)	28		32	
SYMBOLS	MIN	MAX	MIN	MAX
A	–	.210	–	.200
A1	.015	–	.015	–
b	.014	.022	.014	.022
b1	.045	.065	.045	.065
C	.009	.015	.009	.015
D	1.380	1.420	1.610	1.620
E	.390	.425	.390	.425
E1	.340	.390	.340	.390
e	.100 BSC		.100 BSC	
eA	.400 BSC		.400 BSC	
L	.115	.160	.115	.160
α	0°	15°	0°	15°
S	.040	.070	.040	.070
Q1	.060	.090	.060	.090

PLASTIC DUAL IN–LINE PACKAGES (Continued)

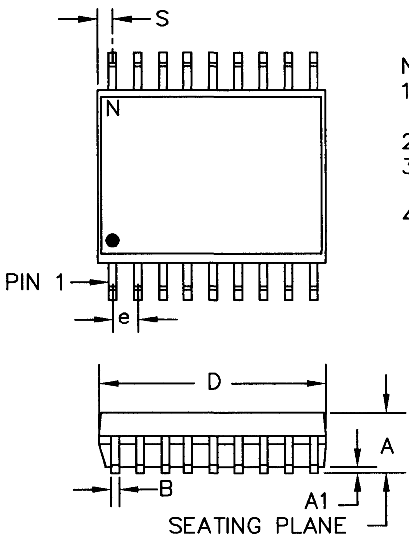
24–48 LEAD PLASTIC DIP (600 MIL)



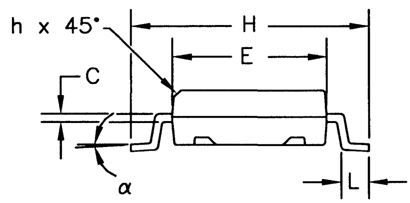
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG #	P24–2		P28–1		P32–1		P40–1		P48–1	
# OF LEADS (N)	24		28		32		40		48	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.160	.185	.160	.185	.170	.190	.160	.185	.170	.200
A1	.015	.035	.015	.035	.015	.050	.015	.035	.015	.035
b	.015	.020	.015	.020	.016	.020	.015	.020	.015	.020
b1	.050	.065	.050	.065	.045	.055	.050	.065	.050	.065
C	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	1.240	1.260	1.420	1.460	1.645	1.655	2.050	2.070	2.420	2.450
E	.600	.620	.600	.620	.600	.625	.600	.620	.600	.620
E1	.530	.550	.530	.550	.530	.550	.530	.550	.530	.560
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
eA	.610	.670	.610	.670	.610	.670	.610	.670	.610	.670
L	.120	.150	.120	.150	.125	.135	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°
S	.060	.080	.055	.080	.070	.080	.070	.085	.060	.075
Q1	.060	.080	.060	.080	.065	.075	.060	.080	.060	.080

SMALL OUTLINE IC



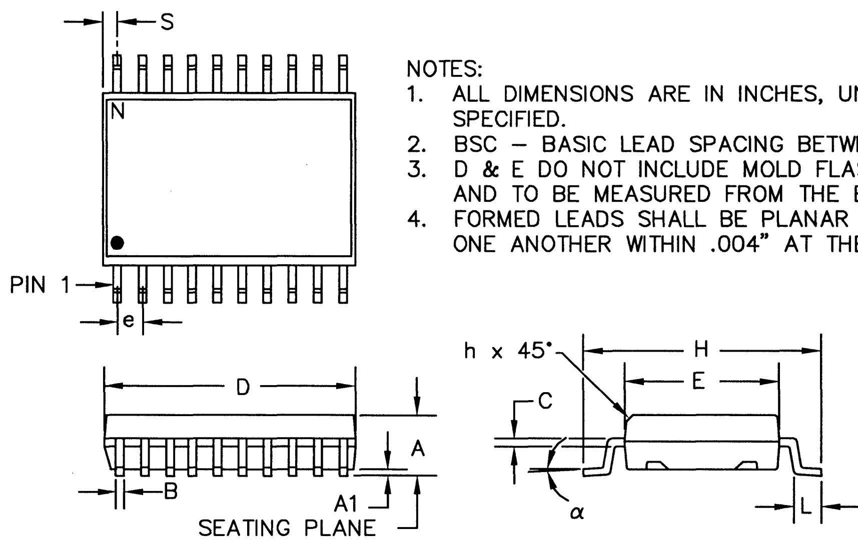
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.



16–24 LEAD SMALL OUTLINE (GULL WING – JEDEC)

DWG #	S016–1		S018–1		S020–2		S024–2	
# OF LDS (N)	16 (.300)		18 (.300)		20 (.300")		24 (.300")	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.095	.1043	.095	.1043	.095	.1043	.095	.1043
A1	.005	.0118	.005	.0118	.005	.0118	.005	.0118
B	.014	.020	.014	.020	.014	.020	.014	.020
C	.0091	.0125	.0091	.0125	.0091	.0125	.0091	.0125
D	.403	.413	.447	.462	.497	.511	.600	.614
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC	
E	.292	.2992	.292	.2992	.292	.2992	.292	.2992
h	.010	.020	.010	.020	.010	.020	.010	.020
H	.400	.419	.400	.419	.400	.419	.400	.419
L	.018	.045	.018	.045	.018	.045	.018	.045
α	0°	8°	0°	8°	0°	8°	0°	8°
S	.023	.035	.023	.035	.023	.035	.023	.035

SMALL OUTLINE IC (Continued)

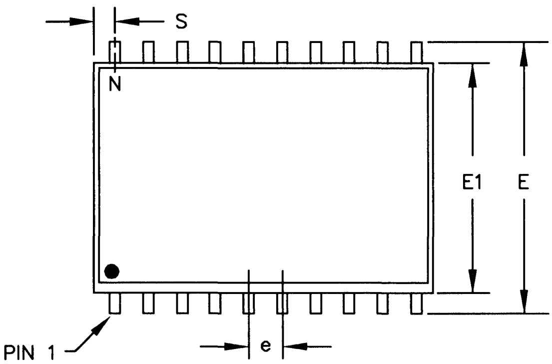


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

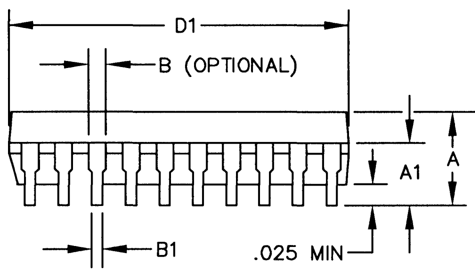
28 LEAD SMALL OUTLINE (GULL WING – JEDEC)

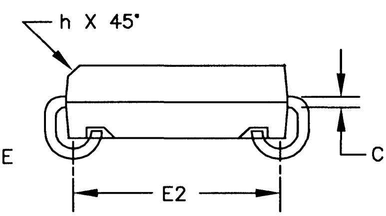
DWG #	S028–2		S028–3	
# OF LDS (N)	28 (.300")		28 (.330")	
SYMBOL	MIN	MAX	MIN	MAX
A	.095	.1043	.110	.120
A1	.005	.0118	.005	.014
B	.014	.020	.014	.019
C	.0091	.0125	.006	.010
D	.700	.712	.718	.728
e	.050 BSC		.050 BSC	
E	.292	.2992	.340	.350
h	.010	.020	.012	.020
H	.400	.419	.462	.478
L	.018	.045	.028	.045
α	0°	8°	0°	8°
S	.023	.035	.023	.035

SMALL OUTLINE IC (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSION AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE

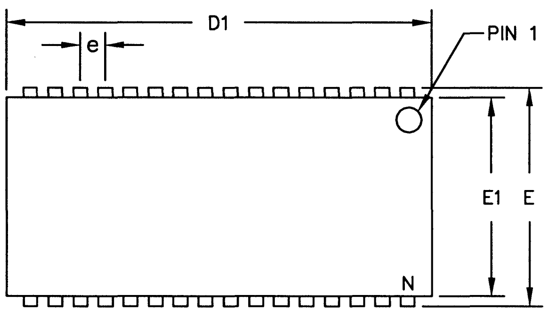




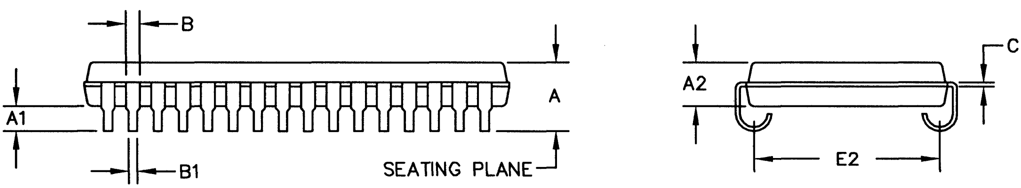
20–32 LEAD SMALL OUTLINE (J-BEND, 300 MIL)

DWG #	SO20-1		SO24-4		SO24-8		SO28-5		SO32-2	
# OF LDS (N)	20		24		24		28		32	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.120	.140	.130	.148	.120	.140	.120	.140	.130	.148
A1	.078	.095	.082	.095	.078	.091	.078	.095	.082	.095
B	–	–	.026	.032	–	–	–	–	.026	.032
B1	.014	.020	.015	.020	.014	.019	.014	.020	.016	.020
C	.008	.013	.007	.011	.0091	.0125	.008	.013	.008	.013
D1	.500	.512	.620	.630	.602	.612	.700	.712	.820	.830
E	.335	.347	.335	.345	.335	.347	.335	.347	.330	.340
E1	.292	.300	.295	.305	.292	.299	.292	.300	.295	.305
E2	.262	.272	.260	.280	.262	.272	.262	.272	.260	.275
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
h	.010	.020	.010	.020	.010	.016	.012	.020	.012	.020
S	.023	.035	.032	.043	.032	.043	.023	.035	.032	.043

SMALL OUTLINE IC (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSION AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

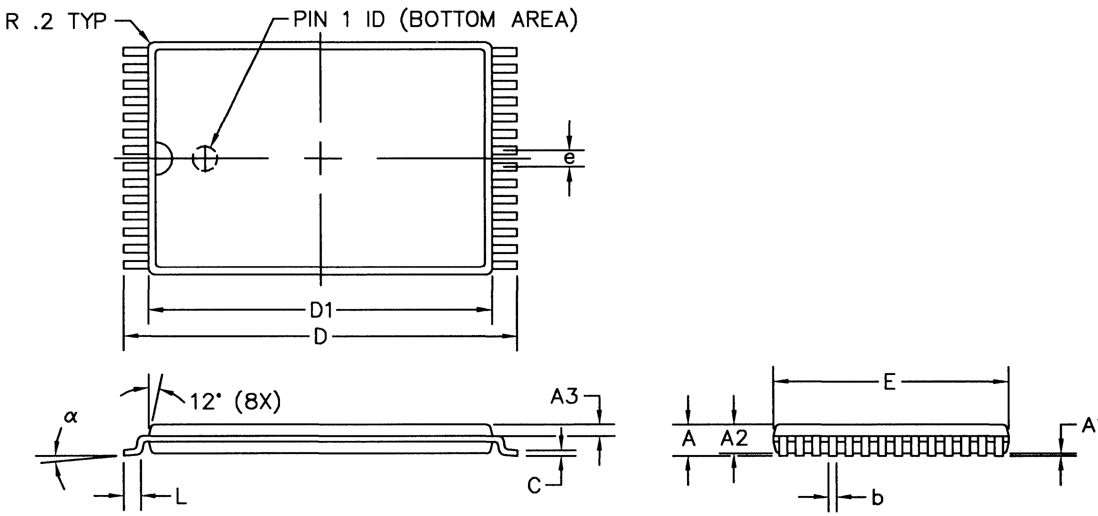


28–32 LEAD SMALL OUTLINE (J–BEND, 400 MIL)

DWG #	S028–6		S032–3	
# OF LDS (N)	28		32	
SYMBOLS	MIN	MAX	MIN	MAX
A	.131	.145	.131	.145
A1	.045	.055	.045	.055
A2	.086	.090	.086	.090
B	.026	.032	.026	.032
B1	.015	.020	.015	.020
C	.007	.0125	.007	.0125
D1	.720	.730	.820	.830
E	.435	.445	.435	.445
E1	.395	.405	.395	.405
E2	.360	.380	.360	.380
e	.050 BSC		.050 BSC	
S	.032	.043	.032	.043

TSOP

28 LEAD TSOP – TYPE I



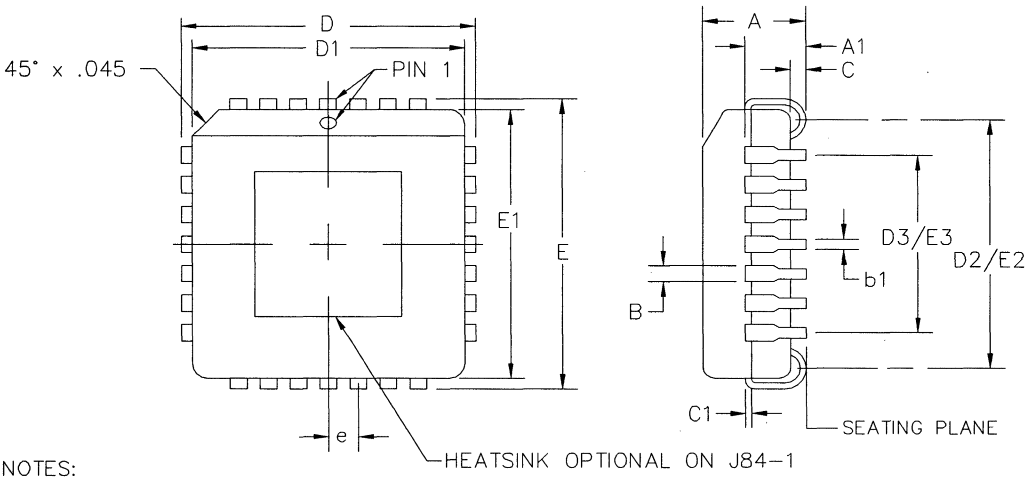
DWG #	PZ28–1	
# OF LDS	28	
SYMBOL	MIN	MAX
A	1.00	1.20
A1	.05	.20
A2	.91	1.02
A3	.37	.47
b	.18	.27
C	.15	.20
D	13.2	13.6
D1	11.7	11.9
E	7.9	8.1
e	.55 BASIC	
α	0°	5°
L	.3	.7

NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. BOTH PKG LENGTH & WIDTH DO NOT INCLUDE MOLD FLASH.
3. FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004".
4. MAX LEAD WIDTH WITH DAMBAR PROTRUSION: .30.

4

PLASTIC LEADED CHIP CARRIERS

20–84 LEAD PLCC (SQUARE)



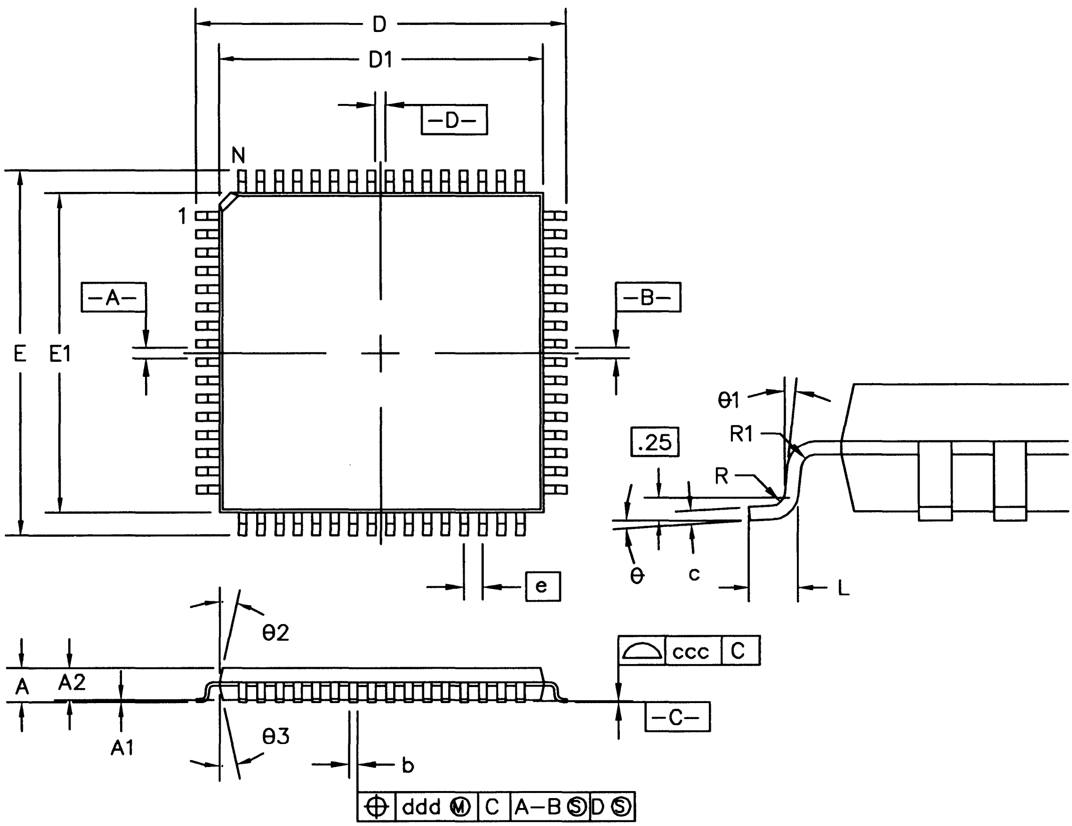
NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
5. ND & NE REPRESENT NUMBER OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
6. D1 & E1 SHOULD BE MEASURED FROM THE BOTTOM OF THE PKG.

DWG #	J20–1		J28–1		J44–1		J52–1		J68–1		J84–1	
# OF LDS	20		28		44		52		68		84	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180
A1	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115
B	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032
b1	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021
C	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040
C1	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
D1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
D2/E2	.290	.330	.390	.430	.590	.630	.690	.730	.890	.930	1.090	1.130
D3/E3	.200 REF		.300 REF		.500 REF		.600 REF		.800 REF		1.000 REF	
E	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
E1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
ND/NE	5		7		11		13		17		21	

PLASTIC QUAD FLATPACKS

TQFP



NOTES:
1. ALL DIMENSIONS ARE IN MELLIMETERS, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD PROTRUSION AND TO BE MEASURED FROM THE BOTTOM OF THE PACKAGE. ALLOWABLE PROTRUSION TO BE .254 PER SIDE.

PLASTIC QUAD FLATPACKS (Continued)

80 LEAD TQFP

DWG #	PN 80-1	
SYMBOL	MIN	MAX
A	–	1.60
A1	.05	.15
A2	1.35	1.45
D	15.75	16.25
D1	13.95	14.05
E	15.75	16.25
E1	13.95	14.05
L	.45	.70
N	80	
e	.65 BSC	
b	.25	.35
ccc	–	.10
ddd	–	.13
R	.08	.20
R1	.08	–
θ	0°	7°
θ1	2°	10°
θ2	11°	13°
θ3	11°	13°
c	.09	.16

16K SRAM PRODUCTS

IDT traces its heritage back to the first fast CMOS 2K x 8 SRAM in the industry, which was introduced at 70ns more than 10 years ago. Today, IDT's 16K family still includes many of the SRAM configurations offered during the early days of the company, now available at much higher speeds. After having been through numerous die shrinks and improvements, the 16K family is a testimonial to the long term commitments that IDT typically makes to support its customers.

The 16K family is based exclusively on CMOS technology, and is now available in speeds as fast as 12ns for commercial applications and 15ns for military applications. It is offered in a wide variety of speeds and packages, and all parts have a low power version. These low power versions offer industry-leading standby power characteristics, as well as a 2V data retention mode, which makes them ideal for portable battery-operated equipment.

Size	Organization	Features	Process	Part Number	Power	Speeds	
						Commercial	Military
16K	16K x 1		CMOS	6167	SA/LA	15,20,25,35	15,20,25,35,45,55, 70,85,100
	4K x 4		CMOS	6168	SA/LA	15,20,25,35	15,20,25,35,45,55, 70,85,100
	4K x 4	Sep I/O	CMOS	71681	SA/LA	15,20,25,35,45	15,20,25,35,45,55, 70,85,100
	4K x 4	Sep I/O	CMOS	71682	SA/LA	15,20,25,35,45	12,15,20,25,35,45, 55,70,85,100
	2K x 8		CMOS	6116	SA/LA	15,20,25,35,45	20,25,35,45,55,70,90 120,150

5

TABLE OF CONTENTS

5

CMOS STATIC RAM 16K (16K x 1-BIT)

IDT6167SA
IDT6167LA

FEATURES:

- High-speed (equal access and cycle time)
  - — Military: 15/20/25/35/45/55/70/85/100ns (max.)
  - — Commercial: 15/20/25/35ns (max.)
- Low power consumption
- Battery backup operation — 2V data retention voltage (IDT6167LA only)
- Available in 20-pin CERDIP and Plastic DIP, 20-pin CERPACK, 20-pin SOJ and 20-pin leadless chip carrier
- Produced with advanced CMOS high-performance technology
- CMOS process virtually eliminates alpha particle soft-error rates
- Separate data input and output
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT6167 is a 16,384-bit high-speed static RAM organized as 16K x 1. The part is fabricated using IDT's high-performance, high reliability CMOS technology.

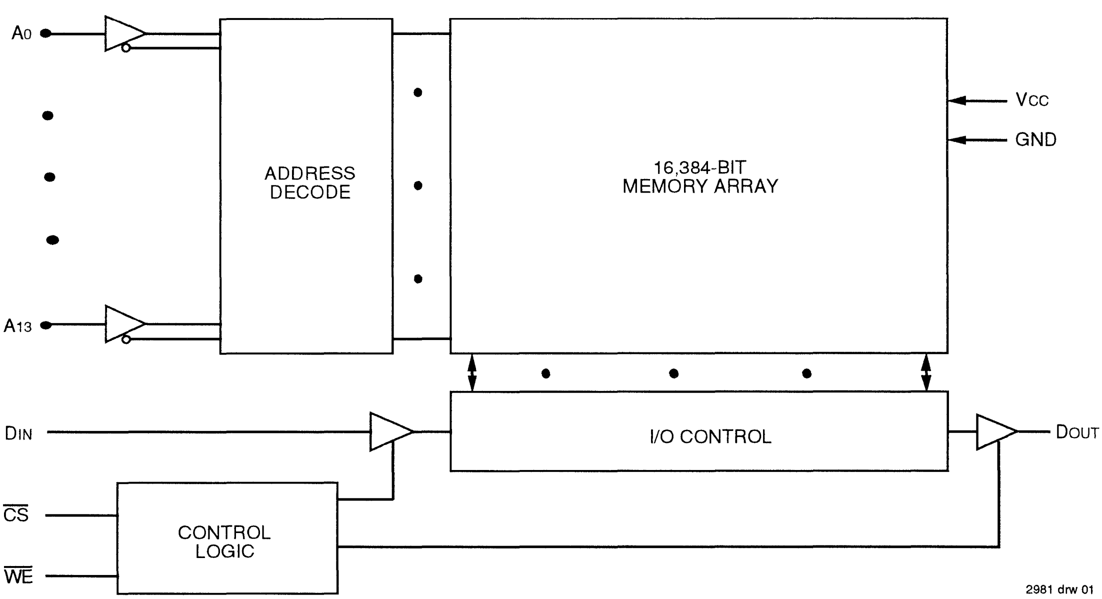
Access times as fast as 15ns are available. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains HIGH. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW operating off a 2V battery.

All inputs and the output of the IDT6167 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs.

The IDT6167 is packaged in a space-saving 20-pin, 300 mil Plastic DIP or CERDIP, Plastic 20-pin SOJ, 20-pin CERPACK and 20-pin leadless chip carrier, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



The IDT logo is a registered trademark of Integrated Device Technology, Inc.

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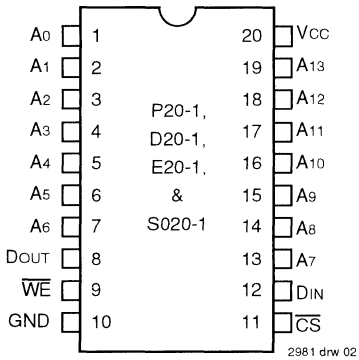
PIN CONFIGURATIONS

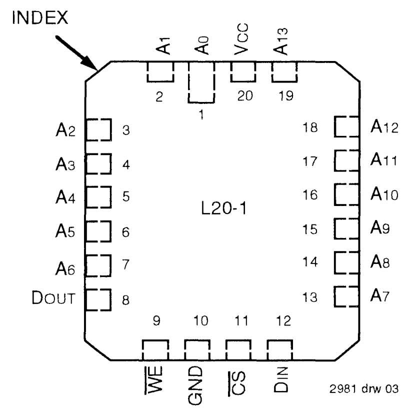


DIP/SOIC/CERPACK/SOJ
TOP VIEW

TRUTH TABLE (1)

Mode	$\overline{\text{CS}}$	$\overline{\text{WE}}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	DATAOUT	Active
Write	L	L	High-Z	Active

NOTE: 2981 tbl 02
1. H = V_{IH}, L = V_{IL}, X = Don't Care.



LCC
TOP VIEW

PIN DESCRIPTIONS

A0–A13	Address Inputs
$\overline{\text{CS}}$	Chip Select
$\overline{\text{WE}}$	Write Enable
V_{CC}	Power
DIN	DATAIN
DOUT	DATAOUT
GND	Ground

2981 tbl 01

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2981 tbl 05
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2981 tbl 06

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2981 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2981 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	Power	6167SA/LA15 Com'l.	6167SA/LA15 Mil.	6167SA/LA20 Com'l.	6167SA/LA20 Mil.	6167SA/LA25 Com'l.	6167SA/LA25 Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = 0(3)	SA	90	90	90	90	90	90	mA
		LA	55	60	55	60	55	60	
I_{CC2}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	SA	120	130	100	110	100	100	mA
		LA	100	110	80	85	70	75	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	SA	50	50	35	35	35	35	mA
		LA	35	35	30	30	25	25	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max. $V_{IN} \geq V_{HC}$ or $V_{IN} \leq V_{LC}$, f = 0(3)	SA	5	10	5	10	5	10	mA
		LA	0.9	2	0.05	2	0.05	0.9	

DC ELECTRICAL CHARACTERISTICS(1) (CONTINUED)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	Power	6167SA/LA35 Com'l.	6167SA/LA35 Mil.	6167SA/LA45(2) Com'l.	6167SA/LA45(2) Mil.	6167SA/LA55(2) Com'l.	6167SA/LA55(2) Mil.	6167SA/LA70(2) Com'l.	6167SA/LA70(2) Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = 0(3)	SA	90	90	—	90	—	90	—	90	mA
		LA	55	60	—	60	—	60	—	60	
I_{CC2}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	SA	100	100	—	100	—	100	—	100	mA
		LA	65	70	—	65	—	60	—	60	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	SA	35	35	—	35	—	35	—	35	mA
		LA	20	20	—	20	—	20	—	15	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max. $V_{IN} \geq V_{HC}$ or $V_{IN} \leq V_{LC}$, f = 0(3)	SA	5	10	—	10	—	10	—	10	mA
		LA	0.05	0.9	—	0.9	—	0.9	—	0.9	

2980 tbl 07

NOTES:
1. All values are maximum guaranteed values.
2. –55°C to +125°C temperature range only. Also available; 85ns and 100ns Military devices.
3. f_{MAX} = 1/t_{RC}, only address inputs cycling at f_{MAX}. f = 0 means no Address inputs change.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT6167SA Min.	IDT6167SA Max.	IDT6167LA Min.	IDT6167LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.,	MIL	—	10	—	5	µA
		V_{IN} = GND to V_{CC}	COM'L	—	5	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH},	MIL	—	10	—	5	µA
		V_{OUT} = GND to V_{CC}	COM'L	—	5	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	—	2.4	—	V

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

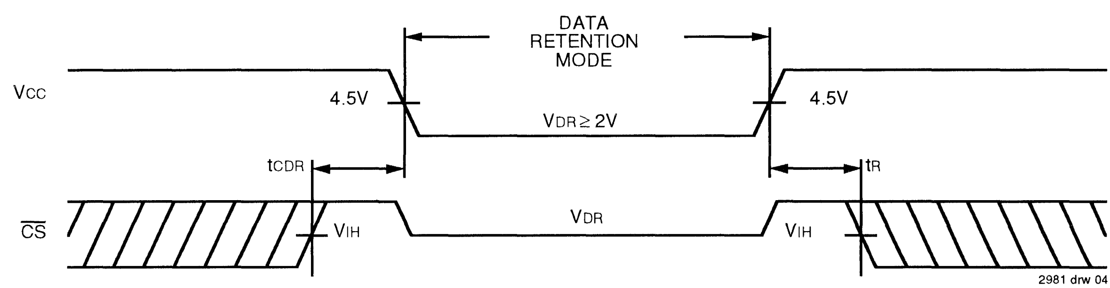
Symbol	Parameter	Test Condition		Min.	Typ.[1] Vcc @ 2.0v	Typ.[1] Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}$ ≥ V_{HC} VIN ≥ V_{HC} or ≤ V_{LC}	MIL.	—	0.5	1.0	200	300	µA
			COM'L.	—	0.5	1.0	20	30	
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns
$\|I_{LI}\|$[3]	Input Leakage Current	—		—	—	—	2	2	µA

NOTES:

2981 tbl 09

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

LOW Vcc DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2979 tbl 09

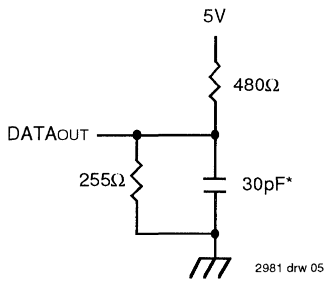


Figure 1. AC Test Load

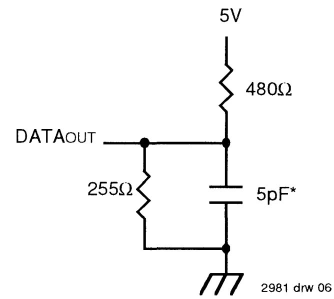


Figure 2. AC Test Load
(for t_{CLZ}, t_{CHZ}, t_{WHZ} and t_{OW})

*Includes scope and jig.

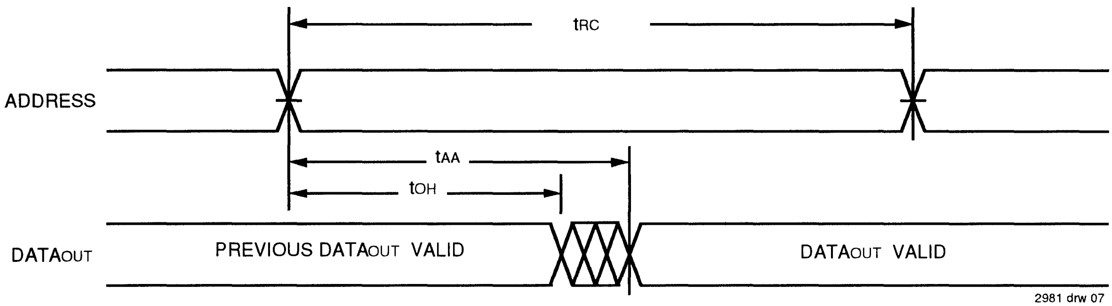
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6167SA15 6167LA15		6167SA20/25 6167LA20/25		6167SA35/45[1] 6167LA35/45[1]		6167SA55[1]/70[1] 6167LA55[1]/70[1]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	15	—	20/25	—	35/45	—	55/70	—	ns
t_{AA}	Address Access Time	—	15	—	20/25	—	35/45	—	55/70	ns
t_{ACS}	Chip Select Access Time	—	15	—	20/25	—	35/45	—	55/70	ns
t_{CLZ}[2]	Chip Deselect to Output in Low-Z	3	—	5/5	—	5/5	—	5/5	—	ns
t_{CHZ}[2]	Chip Select to Output in High-Z	—	10	—	10/10	—	15/30	—	40/40	ns
t_{OH}	Output Hold from Address Change	3	—	5/5	—	5/5	—	5/5	—	ns
t_{PU}[2]	Chip Select to Power-Up Time	0	—	0/0	—	0/0	—	0/0	—	ns
t_{PD}[2]	Chip Deselect to Power-Down Time	—	15	—	20/25	—	35/45	—	55/70	ns
Write Cycle										
t_{WC}	Write Cycle Time	15	—	20/20	—	30/45	—	55/70	—	ns
t_{CW}	Chip Select to End-of-Write	15	—	15/20	—	30/40	—	45/55	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	15/20	—	30/40	—	45/55	—	ns
t_{AS}	Address Set-up Time	0	—	0/0	—	0/0	—	0/0	—	ns
t_{WP}	Write Pulse Width	13	—	15/20	—	30/30	—	35/40	—	ns
t_{WR}	Write Recovery Time	0	—	0/0	—	0/0	—	0/0	—	ns
t_{DW}	Data Valid to End-of-Write	10	—	12/15	—	17/20	—	25/30	—	ns
t_{DH}	Data Hold Time	0	—	0/0	—	0/0	—	0/0	—	ns
t_{WHZ}[2]	Write Enable to Output in High-Z	—	7	—	8/8	—	15/30	—	40/40	ns
t_{OW}[2]	Output Active from End-of-Write	0	—	0/0	—	0/0	—	0/0	—	ns

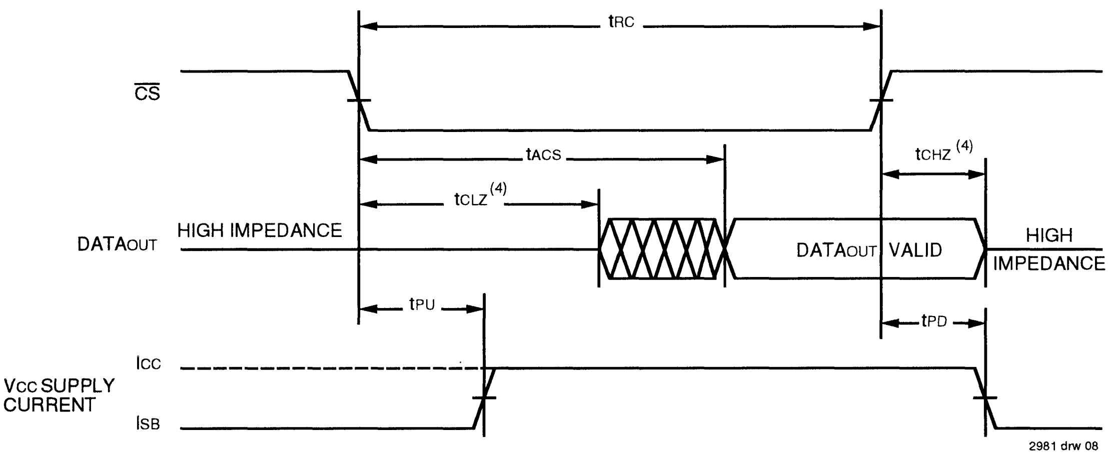
2981 tbl 11

NOTES:
1. –55°C to +125°C temperature range only. Also available: 85ns and 100ns Military devices.
2. This parameter is guaranteed with AC Load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1, 2)



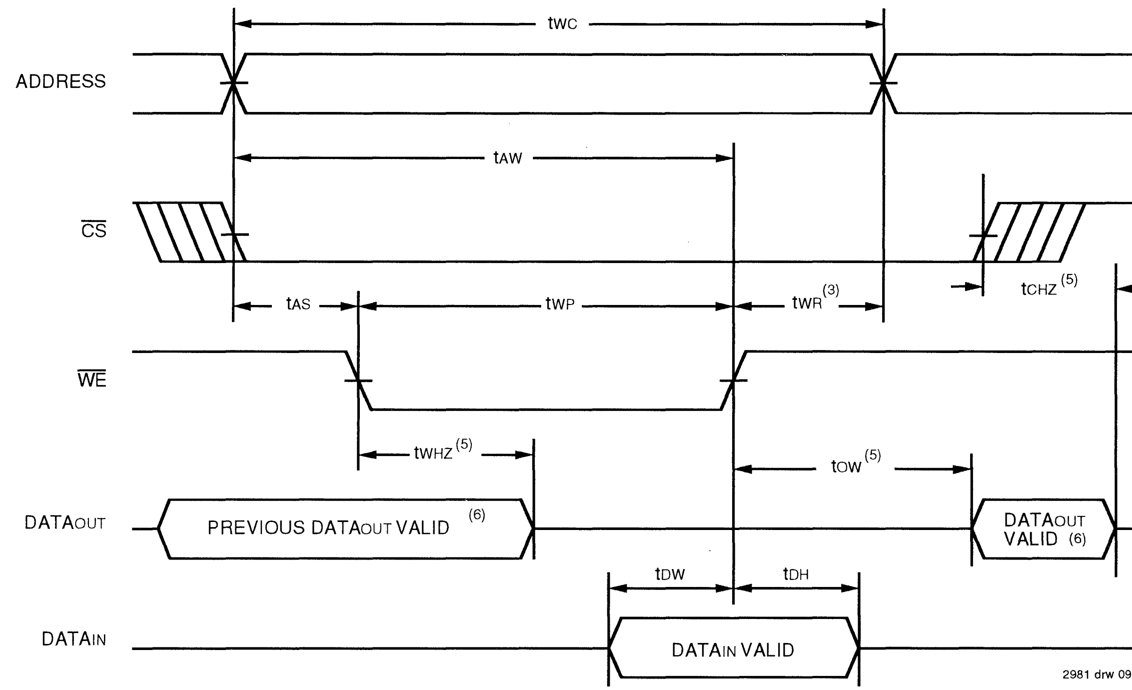
TIMING WAVEFORM OF READ CYCLE NO. 2(1, 3)



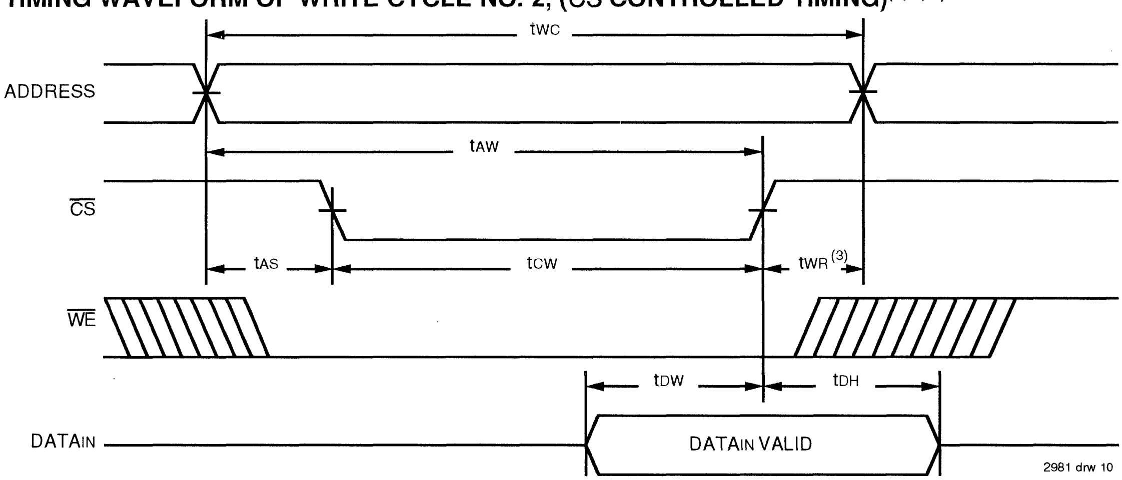
NOTES:
1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincedent with $\overline{CS}$ transition LOW.
4. Transition is measured ±200mV from steady state.

5

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 4)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 4)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be inactive during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state.
5. Transition is measured ±200mV from steady state.
6. During this period, the I/O pins are in the output state and the input signals must not be applied.

ORDERING INFORMATION

IDT	6167	XX	XXX	XX	X
	Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package

P	300MIL Plastic DIP (P20–1)
D	300MIL CERDIP (D20–1)
L	300MIL Leadless Chip Carrier (L20–1)
E	300MIL CERPACK (E20–1)
Y	300MIL SOJ (SO20–1)

Speed — Speed in nanoseconds

15	
20	
25	
35	
45	Military Only
55	Military Only
70	Military Only
85	Military Only
100	Military Only

Power

SA	Standard Power
LA	Low Power

2981 drw 11

5

Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (4K x 4-BIT)

IDT6168SA
IDT6168LA

FEATURES:

- High-speed (equal access and cycle time)
  - — Military: 15/20/25/35/45/55/70/85/100ns (max.)
  - — Commercial: 15/20/25/35ns (max.)
- Low power consumption
- Battery backup operation—2V data retention voltage (IDT6168LA only)
- Available in high-density 20-pin ceramic or plastic DIP, 20-pin SOIC, 20-pin CERPACK and 20-pin leadless chip carrier
- Produced with advanced CMOS high-performance technology
- CMOS process virtually eliminates alpha particle soft-error rates
- Bidirectional data input and output
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

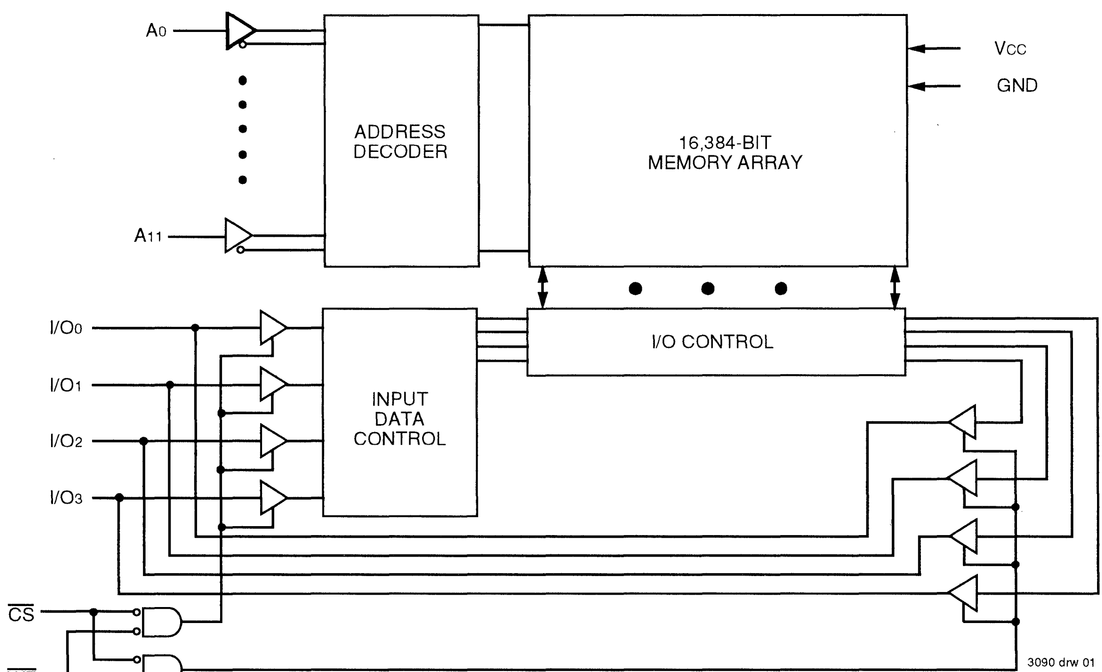
The IDT6168 is a 16,384-bit high-speed static RAM organized as 4K x 4. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective approach for high-speed memory applications.

Access times as fast 15ns are available. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains HIGH. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1μW operating off a 2V battery. All inputs and outputs of the IDT6168 are TTL-compatible and operate from a single 5V supply.

The IDT6168 is packaged in either a space saving 20-pin, 300-mil ceramic or plastic DIP, 20-pin CERPACK, 20-pin SOIC, or 20-pin leadless chip carrier, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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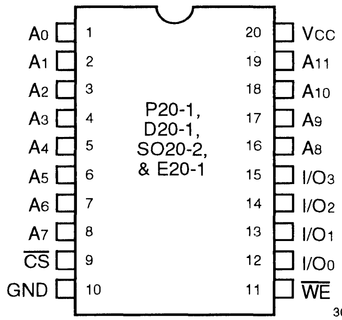
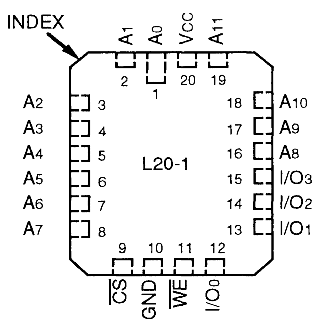
PIN CONFIGURATIONS



3090 drw 02

**DIP/SOIC/SOJ/CERPACK
TOP VIEW**



3090 drw 03

**LCC
TOP VIEW**

PIN DESCRIPTIONS

Name	Description
A_0–A_{11}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
I/O_{0-3}	Data Input/Output
V_{CC}	Power
GND	Ground

3090 tbl 01

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	7	pF

NOTE: 3090 tbl 02

1. This parameter is determined by device characterization, but is not production tested.

TRUTH TABLE(1)

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

NOTE: 3090 tbl 03

1. H = V_{IH}, L = V_{IL}, X = Don't Care

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 3090 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 3090 tbl 05

1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	VCC
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

3090 tbl 06

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6168SA15 Com'l.	6168SA15 Mil.	6168SA20 6168LA20 Com'l.	6168SA20 6168LA20 Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = 0(3)	SA	110	120	90	100	mA
		LA	—	—	70	80	
I_{CC2}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	SA	145	165	120	120	mA
		LA	—	—	100	110	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(3)	SA	55	60	45	45	mA
		LA	—	—	30	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., $V_{IN} \geq V_{HC}$ or $V_{IN} \leq V_{LC}$, f = 0(3)	SA	20	20	20	20	mA
		LA	—	—	0.5	5	

3090 tbl 07

DC ELECTRICAL CHARACTERISTICS (CONTINUED)(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6168SA25 6168LA25 Com'l.	6168SA25 6168LA25 Mil.	6168SA35 6168LA35 Com'l.	6168SA35 6168LA35 Mil.	6168SA45/55 6168LA45/55 Com'l.	6168SA45/55 6168LA45/55 Mil.	6168SA70(2) 6168LA70(2) Com'l.	6168SA70(2) 6168LA70(2) Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = 0(3)	SA	90	100	90	100	—	100	—	100	mA
		LA	70	80	70	80	—	80	—	80	
I_{CC2}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	SA	110	120	100	110	—	110	—	110	mA
		LA	90	100	80	90	—	80	—	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(3)	SA	35	45	30	35	—	35	—	35	mA
		LA	25	30	20	25	—	25/20	—	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., $V_{IN} \geq V_{HC}$ or $V_{IN} \leq V_{LC}$, f = 0(3)	SA	3	10	3	10	—	10	—	10	mA
		LA	0.5	0.3	0.5	0.3	—	0.3	—	0.3	

3090 tbl 08

NOTES:
1. All values are maximum guaranteed values.
2. Also available 85 and 100ns military devices.
3. f_{MAX} = 1/t_{RC}, only address inputs are cycling at f_{MAX}. f = 0 means no address inputs are changing.

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT6168SA Min.	IDT6168SA Max.	IDT6168LA Min.	IDT6168LA Max.	Unit
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL	—	10	—	5	µA
			COM'L	—	2	—	2	
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL	—	10	—	5	µA
			COM'L	—	2	—	2	
V_{OL}	Output LOW Voltage	I_{OL} = 10mA, V_{CC} = Min.		—	0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output HIGH Voltage	I_{OL} = –4mA, V_{CC} = Min.		2.4	—	2.4	—	V

3090 tbl 09

DATA RETENTION CHARACTERISTICS (LA Version Only)

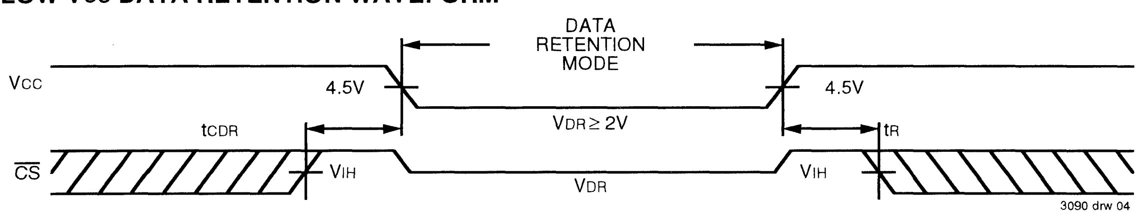
$V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Condition		IDT6168LA Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	— —	0.5[2] 1.0[3]	100[2] 150[3]	μA
			COM'L.	— —	0.5[2] 1.0[3]	20[2] 30[3]	μA
t_{CDR}[5]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[5]	Operation Recovery Time			t_{RC}[2]	—	—	ns

3090 tbl 10

NOTES:
1. $T_A = +25°C$.
2. at $V_{CC} = 2V$
3. at $V_{CC} = 3V$
4. t_{RC} = Read Cycle Time.
5. This parameter is guaranteed by device characterization, but is not production tested.

LOW Vcc DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3090 tbl 11

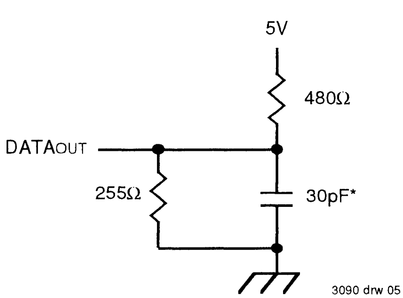


Figure 1. AC Test Load

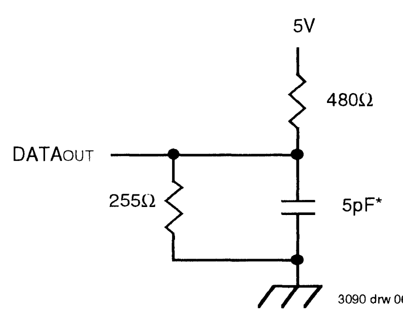


Figure 2. AC Test Load
(for t_{CHZ}, t_{CLZ}, t_{WHZ} and t_{OW})

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA15 Min.	6168SA15 Max.	6168SA20/25 6168LA20/25 Min.	6168SA20/25 6168LA20/25 Max.	Unit
Read Cycle						
tRC	Read Cycle Time	15	—	20/25	—	ns
tAA	Address Access Time	—	15	—	20/25	ns
tACS	Chip Select Access Time	—	15	—	20/25	ns
tCLZ(2)	Chip Select to Output in Low-Z	3	—	5	—	ns
tCHZ(2)	Chip Deselect to Output in High-Z	—	8	—	10	ns
tOH	Output Hold from Address Change	3	—	3	—	ns
tPU(2)	Chip Select to Power-Up Time	0	—	0	—	ns
tPD(2)	Chip Deselect to Power-Down Time	—	15	—	20/25	ns

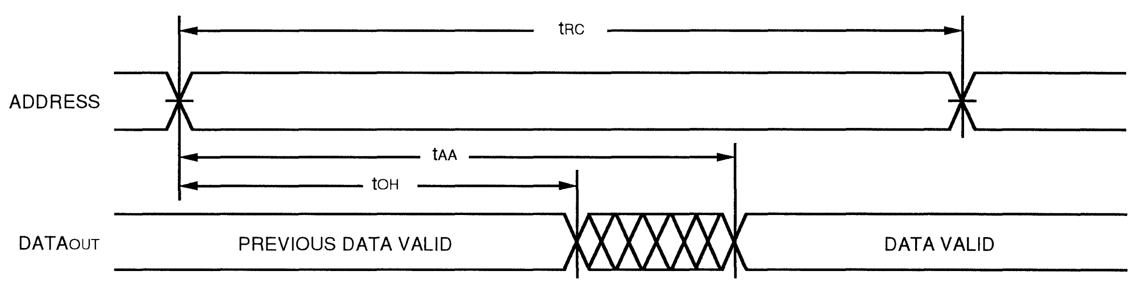
3090 drw 12

AC ELECTRICAL CHARACTERISTICS (CONTINUED) (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA35 6168LA35 Min.	6168SA35 6168LA35 Max.	6168SA45(1) 6168LA45(1) Min.	6168SA45(1) 6168LA45(1) Max.	6168SA55(1) 6168LA55(1) Min.	6168SA55(1) 6168LA55(1) Max.	6168SA70(1) 6168LA70(1) Min.	6168SA70(1) 6168LA70(1) Max.	Unit
Read Cycle										
tRC	Read Cycle Time	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	35	—	45	—	55	—	70	ns
tACS	Chip Select Access Time	—	35	—	45	—	55	—	70	ns
tCLZ(2)	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	ns
tCHZ(2)	Chip Deselect to Output in High-Z	—	15	—	25	—	25	—	30	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
tPU(2)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
tPD(2)	Chip Deselect to Power-Down Time	—	35	—	40	—	50	—	60	ns

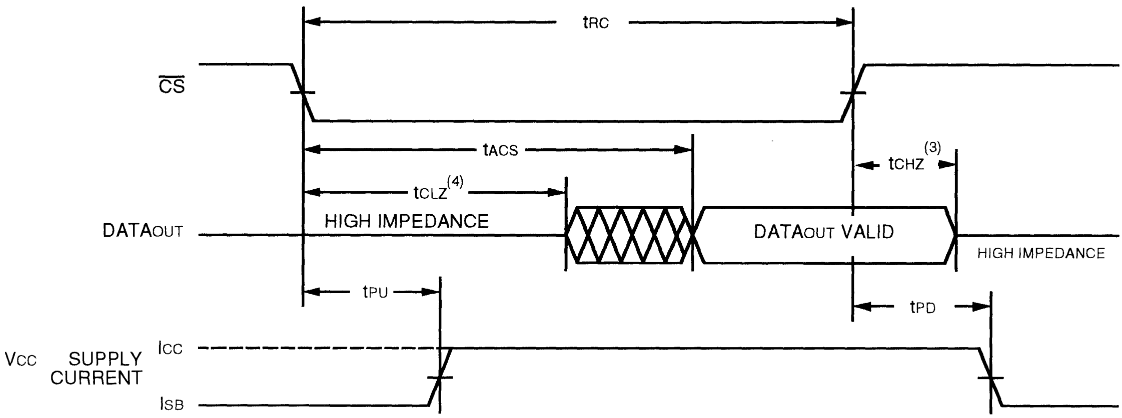
NOTES:
3090 tbl 13
1. –55°C to +125°C temperature range only. Also available 85ns and 100ns devices.
2. This parameter is guaranteed with AC Test load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1, 2)



3090 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 3)



3090 drw 08

NOTES:
1. $\overline{WE}$ is HIGH for Read cycle.
2. $\overline{CS}$ is LOW for Read cycle.
3. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. Transition is measured ±200mV from steady state.

5

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA15		6168SA20/25 6168LA20/25		Unit
		Min.	Max.	Min.	Max.	
Write Cycle						
t_{WC}	Write Cycle Time	15	—	20	—	ns
t_{CW}	Chip Select to End-of-Write	15	—	20	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	20	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	9	—	10	—	ns
t_{DH}	Data Hold Time	0	—	0	—	ns
t_{WHZ}(3)	Write Enable to Output in High-Z	—	6	—	7	ns
t_{OW}(3)	Output Active from End-of-Write	0	—	0	—	ns

3090 tbl 14

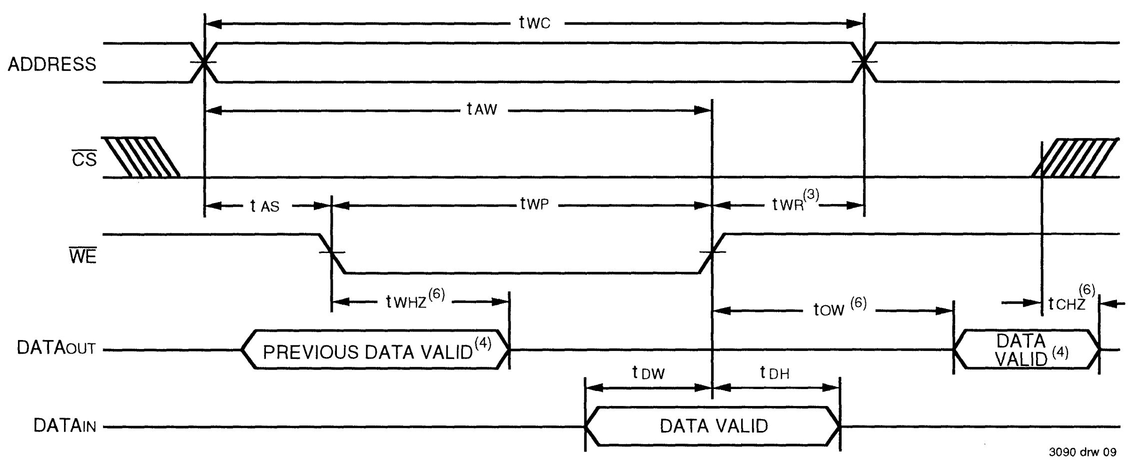
AC ELECTRICAL CHARACTERISTICS (CONTINUED) (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA35 6168LA35		6168SA45(2) 6168LA45(2)		6168SA55(2) 6168LA55(2)		6168SA70(2) 6168LA70(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
tWC	Write Cycle Time	30	—	40	—	50	—	60	—	ns
tCW	Chip Select to End-of-Write	30	—	40	—	50	—	60	—	ns
tAW	Address Valid to End-of-Write	30	—	40	—	50	—	60	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	30	—	40	—	50	—	60	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	DataValid to End-of-Write	15	—	20	—	20	—	25	—	ns
tDH	Data Hold Time	0	—	3	—	3	—	3	—	ns
tWHZ(3)	Write Enable to Output in High-Z	—	13	—	20	—	25	—	30	ns
tOW(3)	Output Active from End-of-Write	0	—	0	—	0	—	0	—	ns

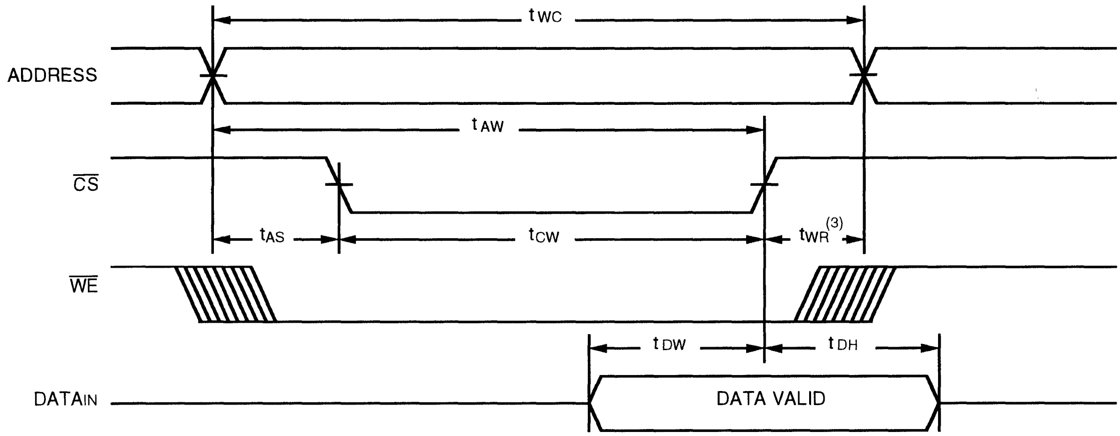
3090 tbl 15

NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only. Also available 85ns and 100ns devices.
3. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{\text{WE}}$ CONTROLLED TIMING)(1, 2, 5)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 5)



3090 drw 10

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals should not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state.

ORDERING INFORMATION

IDT 6168 XX XXX XX X

- 6168 — Device Type
- XX — Power
- XXX — Speed
- XX — Package
- X — Process/Temperature Range

Process/Temperature Range:
- Blank — Commercial (0°C to +70°C)
- B — Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:
- P — 300mil Plastic DIP (P20-1)
- D — 300mil Ceramic DIP (D20-1)
- L — Leadless Chip Carrier (L20-1)
- SO — 300mil Small Outline IC, Gull Wing (SO20-2)
- E — 300mil CERPACK (E20-1)

Speed (Speed in nanoseconds):
- 15
- 20
- 25
- 35
- 45 — Military Only
- 55 — Military Only
- 70 — Military Only
- 85 — Military Only
- 100 — Military Only

Power:
- SA — Standard Power
- LA — Low Power

3090 drw 11

5

CMOS STATIC RAMS 16K (4K x 4-BIT) Separate Data Inputs and Outputs

IDT71681SA/LA
IDT71682SA/LA

FEATURES:

- Separate data inputs and outputs
- IDT71681SA/LA: outputs track inputs during write mode
- IDT71682SA/LA: high-impedance outputs during write mode
- High speed (equal access and cycle time)
  - — Military: 15/20/25/35/45/55/70/85/100ns (max.)
  - — Commercial: 15/20/25/35/45ns (max.)
- Low power consumption
- Battery backup operation—2V data retention (LA version only)
- High-density 24-pin 300-mil Ceramic or Plastic DIP, 24-pin CERPACK, and 28-pin leadless chip carrier
- Produced with advanced CMOS high-performance technology
- CMOS process virtually eliminates alpha particle soft-error rates
- Military product compliant to MIL-STD-883, Class B

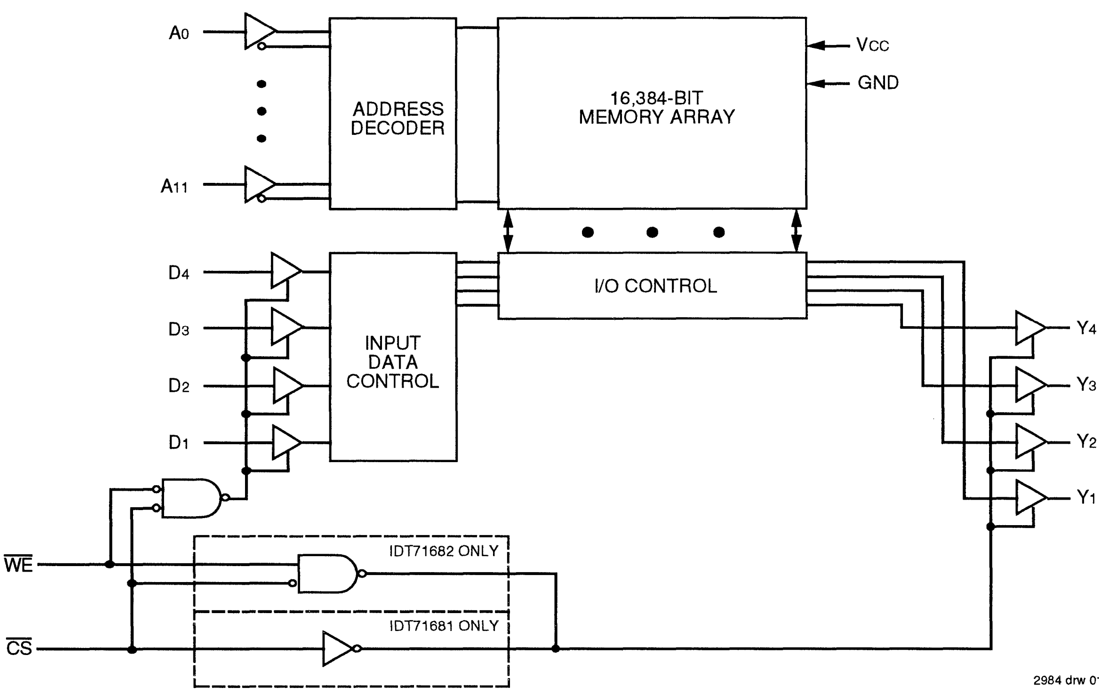
DESCRIPTION:

The IDT71681/IDT71682 are 16,384-bit high-speed static RAMs organized as 4K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective approach for high-speed memory applications.

Access times as fast as 15ns are available. These circuits also offer a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, this standby mode as long as $\overline{CS}$ remains HIGH. In the standby mode, the devices consume less than 10µW, typically. This capability provides significant system-level power and cooling savings. The low-power (LA) versions also offer a battery backup data retention capability where the circuit typically consumes only 1µW operating off a 2V battery.

All inputs and outputs of the IDT71681/IDT71682 are TTL-compatible and operate from a single 5V supply.

FUNCTIONAL BLOCK DIAGRAM



2984 drw 01

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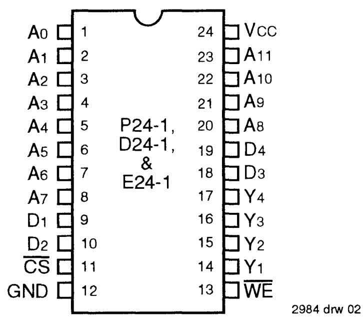
DESCRIPTION (Continued):

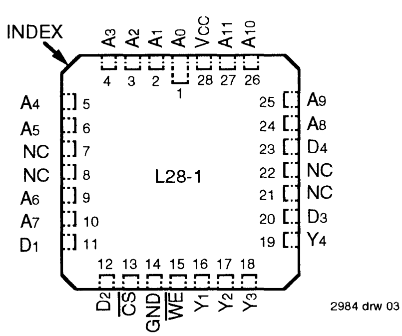
The IDT71681/IDT71682 are packaged in either space-saving 24-pin, 300-mil DIPs, CERPACKS, or 28-pin leadless chip carriers.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS



DIP/SOIC/SOJ/CERPACK TOP VIEW



LCC TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0 – A11	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
D1 – D4	DATAIN
Y1 – Y4	DATAOUT
VCC	Power
GND	Ground

2984 tbl 01

TRUTH TABLE[3]

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	DATAOUT	Active
Write[1]	L	L	DATAIN	Active
Write[2]	L	L	High-Z	Active

2984 tbl 02

NOTES:
1. For IDT71681 only.
2. For IDT71682 only.
3. H = VIH, L = VIL, X = don't care.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE: 2984 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE: 2984 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

5

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

2984 tbl 05

NOTE:
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2984 tbl 06

DATA RETENTION CHARACTERISTICS

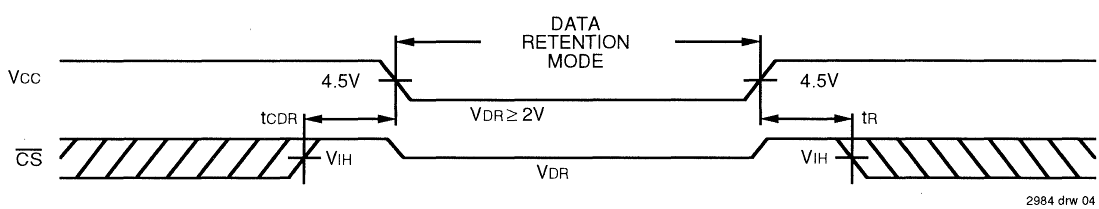
(LA Version Only; V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	Test Condition		IDT71681/2LA Min.	IDT71681/2LA Typ.[1]	IDT71681/2LA Max.	Unit
V_{DR}	Vcc for Data Retention			2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	— —	0.5[2] 1.0[3]	100[2] 150[3]	µA
			COM'L.	— —	0.5[2] 1.0[3]	20[2] 30[3]	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[5]	Operation Recovery Time			t_{RC}[4]	—	—	ns

2984 tbl 07

NOTES:
1. T_A = +25°C.
2. At V_{CC} = 2V
3. At V_{CC} = 3V
4. t_{RC} = Read Cycle Time.
5. This parameter is guaranteed by device characterization, but is not production tested.

LOW Vcc DATA RETENTION WAVEFORM



2984 drw 04

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT71681/2SA Min.	IDT71681/2SA Typ.	IDT71681/2SA Max.	IDT71681/2LA Min.	IDT71681/2LA Typ.	IDT71681/2LA Max.	Unit
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	— —	10 5	— —	— —	5 2	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	— —	10 5	— —	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.			—	0.5	—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	—	0.4	—	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

2984 tbl 08

DC ELECTRICAL CHARACTERISTICS(1,5)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71681x15 71682x15 Com'l.	71681x15 71682x15 Mil.	71681x20 71682x20 Com'l.	71681x20 71682x20 Mil.	71681x25 71682x25 Com'l.	71681x25 71682x25 Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = 0(3)	SA	110	120	90	100	90	100	mA
		LA	—	—	70	80	70	80	
I_{CC2}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = fMAX(3)	SA	145	165	120	120	110	120	mA
		LA	—	—	100	110	90	100	
I_{SB}	Standby Power SupplyCurrent (TTL Level) $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open, f = fMAX(3)	SA	55	65	45	55	35	45	mA
		LA	—	—	30	35	25	30	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, V_{CC} = Max., $V_{IN} \ge V_{HC}$ or $V_{IN} \le V_{LC}$, f = 0(3)	SA	20	20	20	20	3	10	mA
		LA	—	—	0.5	0.3	0.5	0.3	

DC ELECTRICAL CHARACTERISTICS (Continued)(1,5)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	Power	71681x35 71682x35 Com'l.	71681x35 71682x35 Mil.	71681x45 71682x45 Com'l.	71681x45 71682x45 Mil.	71681x55(4) 71682x55(4) Com'l.	71681x55(4) 71682x55(4) Mil.	71681x70(2,4) 71682x70(2,4) Com'l.	71681x70(2,4) 71682x70(2,4) Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = 0(3)	SA	90	100	90	100	—	100	—	100	mA
		LA	70	80	70	80	—	80	—	80	
I_{CC2}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = fMAX(3)	SA	100	110	100	110	—	110	—	110	mA
		LA	80	90	70	80	—	80	—	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open, f = fMAX(3)	SA	30	35	30	35	—	35	—	35	mA
		LA	20	25	20	25	—	20	—	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, V_{CC} = Max., $V_{IN} \ge V_{HC}$ or $V_{IN} \le V_{LC}$, f = 0(3)	SA	3	10	3	10	—	10	—	10	mA
		LA	0.5	0.3	0.5	0.3	—	0.3	—	0.3	

NOTES:

2984 tbl 09

1. All values are maximum guaranteed values.
2. Also available 85 and 100ns military devices.
3. fMAX = 1/tRC, only address inputs are cycling at fMAX. f = 0 means no address inputs are changing.
4. –55°C to +125°C temperature range only.
5. "x" in part numbers indicates power rating (SA or LA).

5

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2984 tbl 10

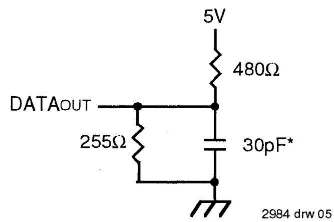


Figure 1. AC Test Load

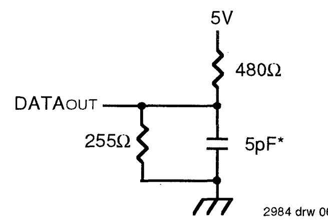


Figure 2. AC Test Load (for tCLZ, tCHZ, tWHZ, and tOW)

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS(3) (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71681x15 71682x15 Min.	Max.	71681x20 71682x20 Min.	Max.	71681x25 71682x25 Min.	Max.	Unit
Read Cycle								
tRC	Read Cycle Time	15	—	20	—	25	—	ns
tAA	Address Access Time	—	15	—	20	—	25	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tCLZ(2)	Chip Select to Output in Low-Z	5	—	5	—	5	—	ns
tCHZ(2)	Chip Select to Output in High-Z	—	7	—	9	—	10	ns
tPU(2)	Chip Select to Power Up Time	0	—	0	—	0	—	ns
tPD(2)	Chip Select to Power Down Time	—	15	—	20	—	25	ns

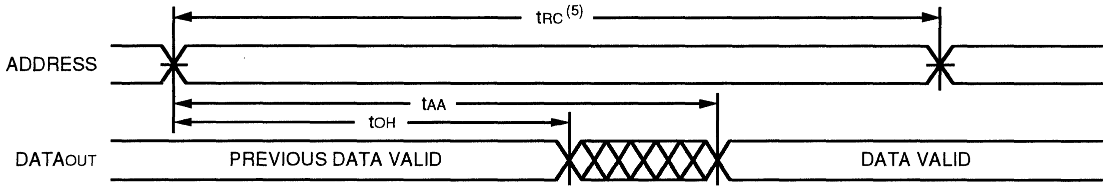
AC ELECTRICAL CHARACTERISTICS(3) (Continued) (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71681x35 71682x35 Min.	Max.	71681x45 71682x45 Min.	Max.	71681x55(1) 71682x55(1) Min.	Max.	71681x70(1) 71682x70(1) Min.	Max.	Unit
Read Cycle										
tRC	Read Cycle Time	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	35	—	45	—	55	—	70	ns
tACS	Chip Select Access Time	—	35	—	45	—	55	—	70	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
tCLZ(2)	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	ns
tCHZ(2)	Chip Select to Output in High-Z	—	15	—	20	—	25	—	30	ns
tPU(2)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
tPD(2)	Chip Select to Power-Down Time	—	35	—	40	—	50	—	60	ns

2984 tbl 11

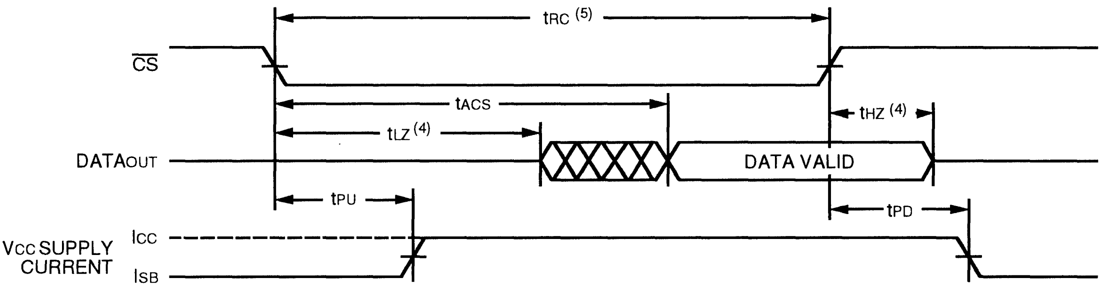
NOTES:
1. –55°C to +125°C temperature range only.
2. This parameter guaranteed with AC Load (Figure 2) by device characterization, but is not production tested.
3. "x" in part numbers indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1(1, 2)



2984 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 3)



2984 drw 08

NOTES:
1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. Transition is measured ±200mV from steady state.
5. All read cycle timings are referenced from the last valid address to the first transmitting address.

AC ELECTRICAL CHARACTERISTICS(3) (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71681x15 71682x15 Min.	Max.	71681x20 71682x20 Min.	Max.	71681x25 71682x25 Min.	Max.	Unit
Write Cycle								
t_{WC}	Write Cycle Time	15	—	20	—	20	—	ns
t_{CW}	Chip Select to End of Write	15	—	20	—	20	—	ns
t_{AW}	Address Valid to End of Write	15	—	20	—	20	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	9	—	10	—	10	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{IY}(2)	Data Valid to Output Valid (71681 only)	—	15	—	20	—	25	ns
t_{WY}(2)	Write Enable to Output Valid (71681 only)	—	15	—	20	—	25	ns
t_{WHZ}(2)	Write Enable to Output in High-Z (71682 only)	—	6	—	7	—	7	ns
t_{OW}(2)	Output Active from End of Write (71682 only)	0	—	0	—	0	—	ns

5

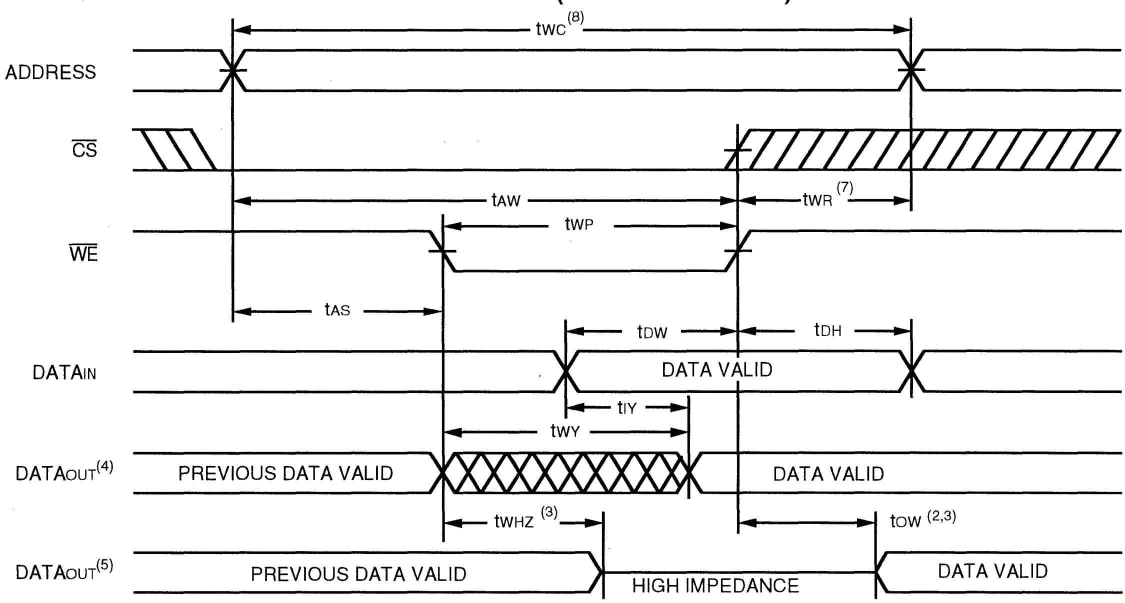
AC ELECTRICAL CHARACTERISTICS (Continued) (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71681x35 71682x35 Min.	Max.	71681x45 71682x45 Min.	Max.	71681x55(1) 71682x55(1) Min.	Max.	71681x70(1) 71682x70(1) Min.	Max.	Unit
Write Cycle										
t_{WC}	Write Cycle Time	30	—	40	—	50	—	60	—	ns
t_{CW}	Chip Select to End of Write	25	—	35	—	50	—	60	—	ns
t_{AW}	Address Valid to End of Write	25	—	35	—	50	—	60	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	35	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	15	—	20	—	20	—	25	—	ns
t_{DH}	Data Hold Time	3	—	3	—	3	—	3	—	ns
t_{IY}(2)	Data Valid to Output Valid (71681 only)	—	30	—	35	—	35	—	40	ns
t_{WY}(2)	Write Enable to Output Valid (71681 only)	—	30	—	35	—	35	—	40	ns
t_{WHZ}(2)	Write Enable to Output in High-Z (71682 only)	—	13	—	20	—	25	—	30	ns
t_{OW}(2)	Output Active from End of Write (71682 only)	0	—	0	—	0	—	0	—	ns

2984 tbl 12

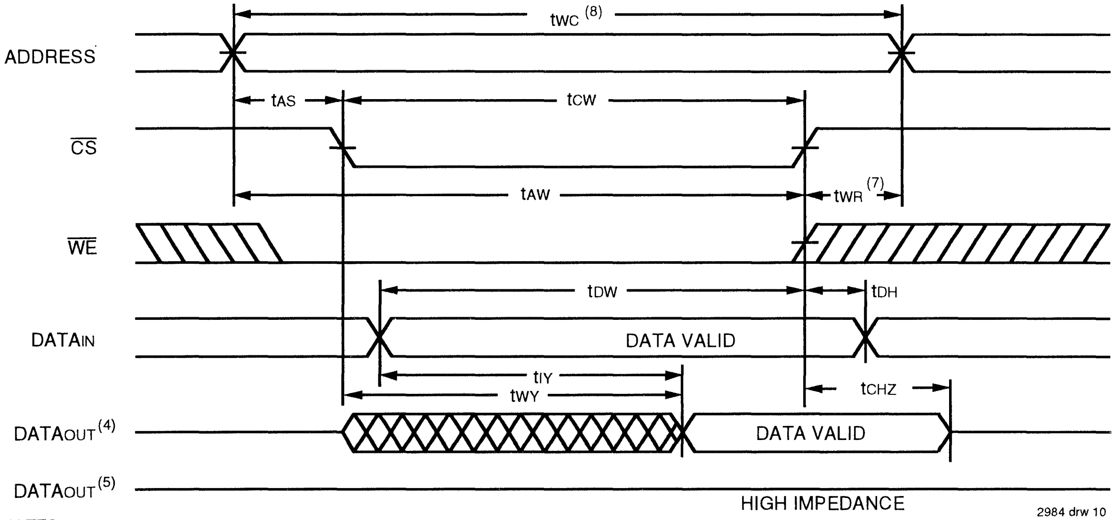
NOTES:
1. –55°C to +125°C temperature range only.
2. This parameter guaranteed with AC Load (Figure 2) by device characterization, but is not production tested.
3. "x" in part numbers indicates power rating (SA or LA).

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1,7)



2984 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1,6)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. If the $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the outputs remain in a high-impedance state.
3. Transition is measured ±200mV from steady state.
4. For IDT71681 only.
5. For IDT71682 only.
6. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
7. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
8. All write cycle timings are referenced from the last valid address to the first transitioning address.

ORDERING INFORMATION

IDT XXXXX XX XXX XX X

Device Type / Power / Speed / Package / Process/Temperature Range

Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package

P	300mil Plastic DIP (P24–1)
D	300mil Ceramic DIP (D24–1)
L	Leadless Chip Carrier (L28–1)
E	300mil CERPACK (E24-1)

Speed (Speed in nanoseconds)

15	
20	
25	
35	
45	
55	Military Only
70	Military Only
85	Military Only
100	Military Only

Power

SA	Standard Power
LA	Low Power

Device Type

71681	(4K x 4 SRAM) Outputs Follow Inputs
71682	(4K x 4 SRAM) High Impedance Outputs

2984 drw 11

Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (2K x 8 BIT)

IDT6116SA IDT6116LA

FEATURES:

- High-speed access and chip select times
  - — Military: 20/25/35/45/55/70/90/120/150ns (max.)
  - — Commercial: 15/20/25/35/45ns (max.)
- Low-power consumption
- Battery backup operation
  - — 2V data retention voltage (LA version only)
- Produced with advanced CMOS high-performance technology
- CMOS process virtually eliminates alpha particle soft-error rates
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in standard 24-pin DIP, 24-pin Thin Dip and Plastic DIP, 28- and 32-pin LCC, 24-pin SOIC, 24-lead CERPACK and 24-pin SOJ
- Military product compliant to MIL-STD-833, Class B

DESCRIPTION:

The IDT6116SA/LA is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

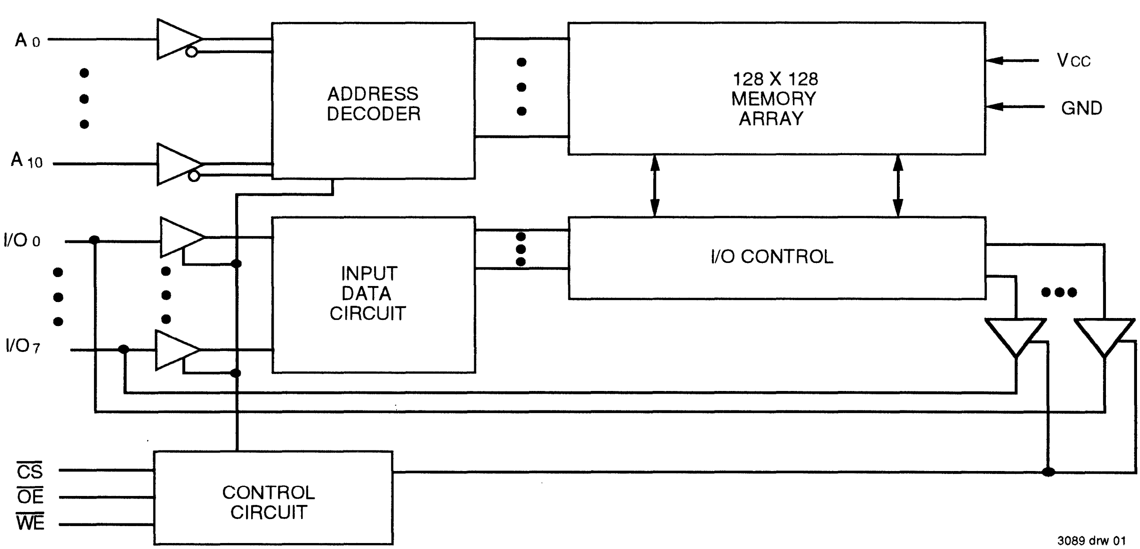
Access times as fast as 15ns are available. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, a standby power mode, as long as $\overline{CS}$ remains HIGH. This capability provides significant system level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW to 4µW operating off a 2V battery.

All inputs and outputs of the IDT6116SA/LA are TTL-compatible. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT6116SA/LA is packaged in 24-pin 600 and 300 mil plastic or ceramic DIP, 28- and 32-pin leadless chip carriers, 24-lead CERPACK, and a 24-lead gull-wing SOIC, providing high board-level packing densities.

Military grade product is manufactured in compliance to the latest version of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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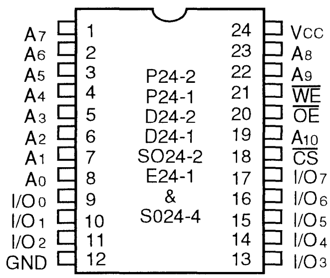
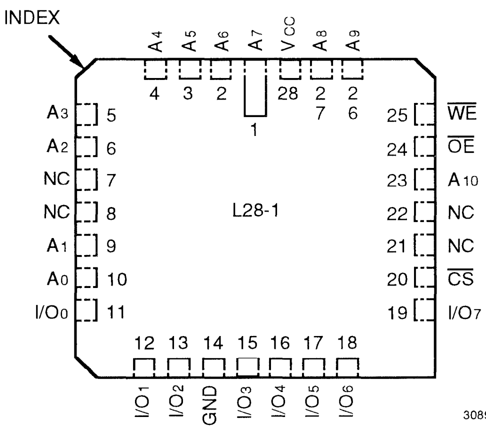
PIN CONFIGURATIONS



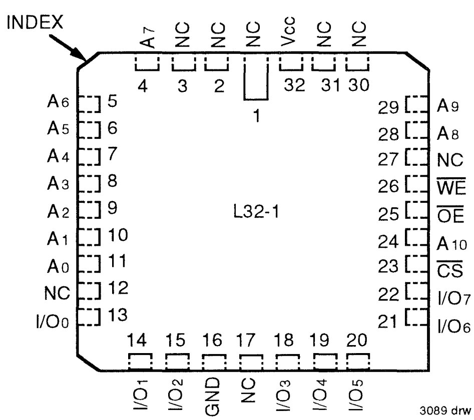
3089 drw 02

DIP/SOIC/CERPACK/SOJ TOP VIEW



3089 drw 03

28-PIN LCC TOP VIEW



3089 drw 04

32-PIN LCC TOP VIEW

PIN DESCRIPTIONS

A_0–A_{13}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground

3089 tbl 01

TRUTH TABLE[(1)]

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O
Standby	H	X	X	High-Z
Read	L	L	H	$DATA_{OUT}$
Read	L	H	H	High-Z
Write	L	X	L	$DATA_{IN}$

NOTE: 3089 tbl 02
1. H = V_{IH}, L = V_{IL}, X = Don't Care.

CAPACITANCE (T_A = +25°C, F = 1.0 MHz)

Symbol	Parameter[(1)]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	pF

NOTE: 3089 tbl 03
1. This parameter is determined by device characterization, but is not production tested.

ABSOLUTE MAXIMUM RATINGS[(1)]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[(2)]	Terminal Voltage with Respect to GND	–0.5 to + 7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to + 70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to + 125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to + 125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTES: 3089 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} +0.5V.

5

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

3089 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5(2)	V
GND	Supply Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	VCC +0.5	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTES:
3089 tbl 06
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.
2. V_{IN} must not exceed V_{CC} +0.5V.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions		IDT6116SA Min.	IDT6116SA Max.	IDT6116LA Min.	IDT6116LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	—	2.4	—	V

3089 tbl 07

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Power	6116SA15(2) 6116LA15(2) Com'l.	Mil.	6116SA20 6116LA20 Com'l.	Mil.	6116SA25 6116LA25 Com'l.	Mil.	6116SA35 6116LA35 Com'l.	Mil.	Unit
I_{CC1}	Operating Power Supply Current, $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = 0	SA	105	—	105	130	80	90	80	90	mA
		LA	95	—	95	120	75	85	75	85	
I_{CC2}	Dynamic Operating Current, $\overline{CS} \leq V_{IL}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(4)	SA	150	—	130	150	120	135	100	115	mA
		LA	140	—	120	140	110	125	95	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(4)	SA	40	—	40	50	40	45	25	35	mA
		LA	35	—	35	45	35	40	25	30	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), $\overline{CS} \geq V_{HC}$, V_{CC} = Max., $V_{IN} \geq V_{HC}$ or $V_{IN} \leq V_{LC}$, f = 0	SA	2	—	2	10	2	10	2	10	mA
		LA	0.1	—	0.1	0.9	0.1	0.9	0.1	0.9	

NOTES:
3089 tbl 08
1. All values are maximum guaranteed values.
2. 0°C to + 70°C temperature range only.
3. –55°C to + 125°C temperature range only.
4. f_{MAX} = 1/t_{RC}, only address inputs are cycling at f_{MAX}, f = 0 means address inputs are not changing.

DC ELECTRICAL CHARACTERISTICS [1] (Continued)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

			6116SA45 6116LA45		6116SA55[3] 6116LA55[3]		6116SA70[3] 6116LA70[3]		6116SA90[3] 6116LA90[3]		6116SA120[3] 6116LA120[3]		6116SA150[3] 6116LA150[3]		
Symbol	Parameter	Power	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Unit
I_{CC1}	Operating Power Supply Current, $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = 0	SA	80	90	—	90	—	90	—	90	—	90	—	90	mA
		LA	75	85	—	85	—	85	—	85	—	85	—	85	
I_{CC2}	Dynamic Operating Current, $\overline{CS} \leq V_{IL}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[4]	SA	100	100	—	100	—	100	—	100	—	100	—	90	mA
		LA	90	95	—	90	—	90	—	85	—	85	—	85	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[4]	SA	25	25	—	25	—	25	—	25	—	25	—	25	mA
		LA	20	20	—	20	—	20	—	25	—	15	—	15	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), $\overline{CS} \geq V_{HC}$, V_{CC} = Max., $V_{IN} \geq V_{HC}$ or $V_{IN} \leq V_{LC}$, f = 0	SA	2	10	—	10	—	10	—	10	—	10	—	10	mA
		LA	0.1	0.9	—	0.9	—	0.9	—	0.9	—	0.9	—	0.9	

3089 tbl 09

NOTES:
1. All values are maximum guaranteed values.
2. 0°C to + 70°C temperature range only.
3. –55°C to + 125°C temperature range only.
4. f_{MAX} = 1/t_{RC}, only address inouts are toggling at f_{MAX}, f = 0 means address inputs are not changing.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

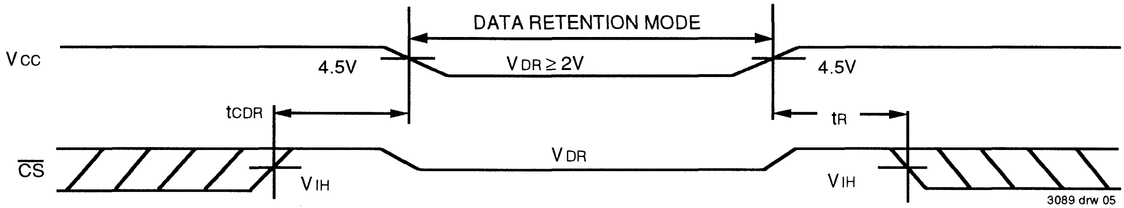
					Typ.[1] Vcc		Max. Vcc		
Symbol	Parameter	Test Conditions		Min.	2.0V	3.0V	2.0V	3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	—	0.5	1.5	200	300	µA
			COM'L.	—	0.5	1.5	20	30	
t_{CDR}[3]	Data Deselect to Data Retention Time			—	0	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns
$\lvert I_{LI} \rvert$	Input Leakage Current			—	—	—	2	2	µA

3089 tbl 10

NOTES:
1. T_A = + 25°C
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

5

LOW Vcc DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3089 tbl 11

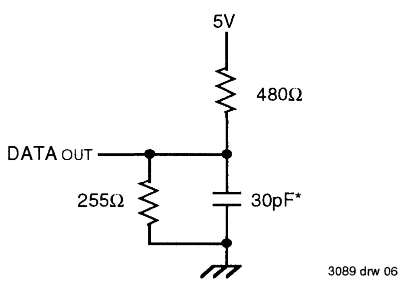


Figure 1. AC Test Load

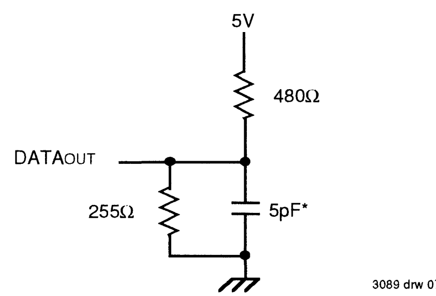


Figure 2. AC Test Load (for tOLZ, tCLZ, tOHZ, tWHZ, tCHZ & tOW)

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5V ± 10%, All Temperature Ranges)

Symbol	Parameter	6116SA15(1) 6116LA15(1) Min.	Max.	6116SA20 6116LA20 Min.	Max.	6116SA25 6116LA25 Min.	Max.	6116SA35 6116LA35 Min.	Max.	Unit
READ CYCLE										
t_{RC}	Read Cycle Time	15	—	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	15	—	19	—	25	—	35	ns
t_{ACS}	Chip Select Access Time	—	15	—	20	—	25	—	35	ns
t_{CLZ}(3)	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	10	—	10	—	13	—	20	ns
t_{OLZ}(3)	Output Enable to Output in Low-Z	0	—	0	—	5	—	5	—	ns
t_{CHZ}(3)	Chip Deselect to Output in High-Z	—	10	—	11	—	12	—	15	ns
t_{OHZ}(3)	Output Disable to Output in High-Z	—	8	—	8	—	10	—	13	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{PU}(3)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}(3)	Chip Deselect to Power-Down Time	—	15	—	20	—	25	—	35	ns

3089 tbl 12

AC ELECTRICAL CHARACTERISTICS (Vcc = 5V ± 10%, All Temperature Ranges) (Continued)

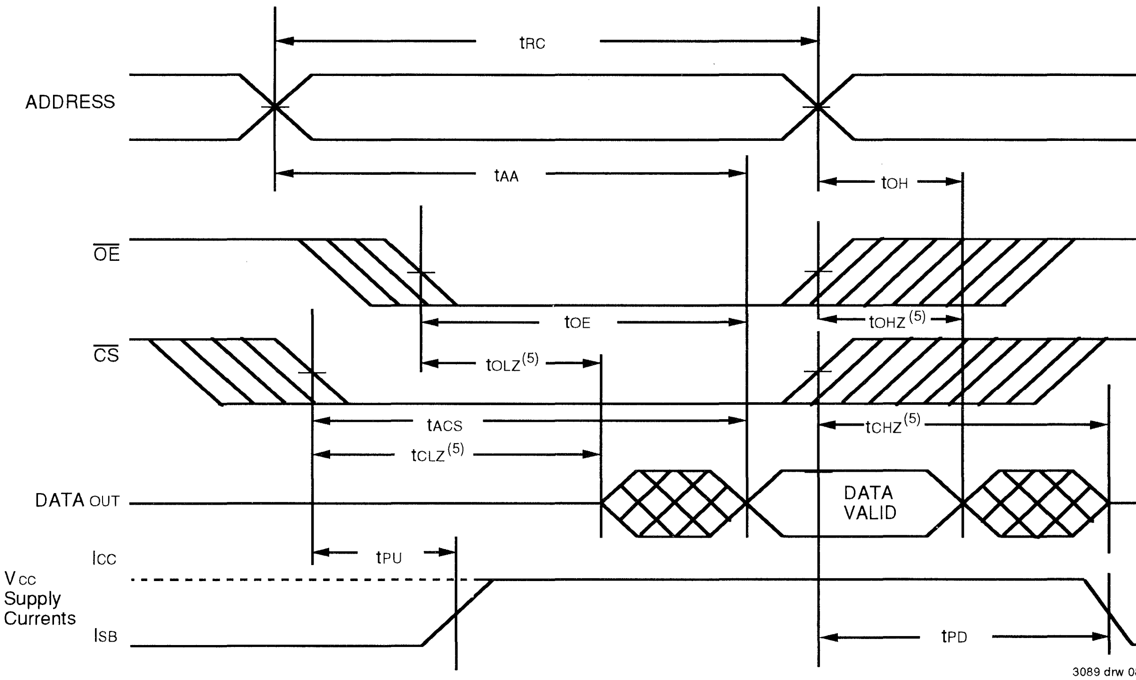
Symbol	Parameter	6116SA45 6116LA45 Min.	Max.	6116SA55(2) 6116LA55(2) Min.	Max.	6116SA70(2) 6116LA70(2) Min.	Max.	6116SA90(2) 6116LA90(2) Min.	Max.	6116SA120(2) 6116LA120(2) Min.	Max.	6116SA150(2) 6116LA150(2) Min.	Max.	Unit
READ CYCLE														
t_{RC}	Read Cycle Time	45	—	55	—	70	—	90	—	120	—	150	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	—	90	—	120	—	150	ns
t_{ACS}	Chip Select Access Time	—	45	—	50	—	65	—	90	—	120	—	150	ns
t_{CLZ}(3)	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	25	—	40	—	50	—	60	—	80	—	100	ns
t_{OLZ}(3)	Output Enable to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}(3)	Chip Deselect to Output in High-Z	—	20	—	30	—	35	—	40	—	40	—	40	ns
t_{OHZ}(3)	Output Disable to Output in High-Z	—	15	—	30	—	35	—	40	—	40	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns

3089 tbl 13

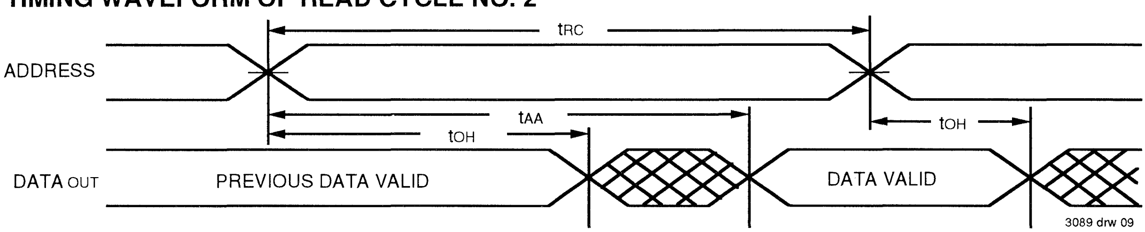
NOTES:
1. 0°C to + 70°C temperature range only.
2. –55°C to + 125°C temperature range only.
3. This parameter guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

5

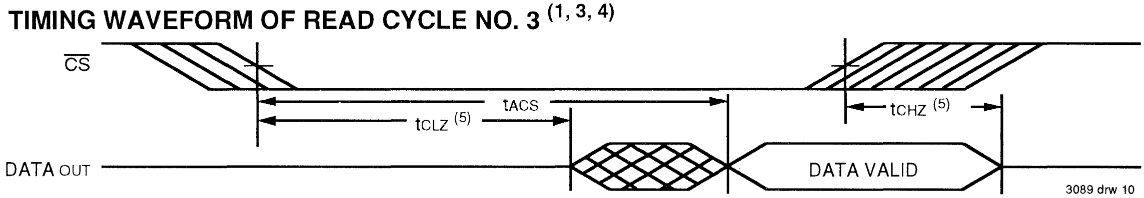
TIMING WAVEFORM OF READ CYCLE NO. 1 (1, 3)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:
1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±500mV from steady state.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5V ± 10%, All Temperature Ranges)

Symbol	Parameter	6116SA15(1) 6116LA15(1)		6116SA20 6116LA20		6116SA25 6116LA25		6116SA35 6116LA35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
tWC	Write Cycle Time	15	—	20	—	25	—	35	—	ns
tCW	Chip Select to End-of-Write	13	—	15	—	17	—	25	—	ns
tAW	Address Valid to End-of-Write	14	—	15	—	17	—	25	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12	—	12	—	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tWHZ(3)	Write to Output in High-Z	—	7	—	8	—	16	—	20	ns
tDW	Data to Write Time Overlap	12	—	12	—	13	—	15	—	ns
tDH(4)	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
tOW(3,4)	Output Active from End-of-Write	0	—	0	—	0	—	0	—	ns

3089 tbl 14

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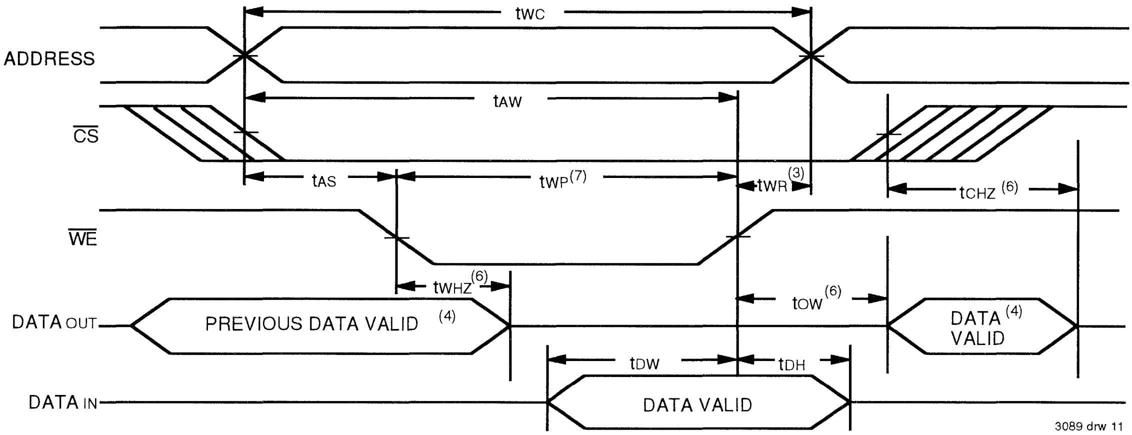
AC ELECTRICAL CHARACTERISTICS (Vcc = 5V ± 10%, All Temperature Ranges)

Symbol	Parameter	6116SA45 6116LA45		6116SA55(2) 6116LA55(2)		6116SA70(2) 6116LA70(2)		6116SA90(2) 6116LA90(2)		6116SA120(2) 6116LA120(2)		6116SA150(2) 6116LA150(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE														
tWC	Write Cycle Time	45	—	55	—	70	—	90	—	120	—	150	—	ns
tCW	Chip Select to End of Write	30	—	40	—	40	—	55	—	70	—	90	—	ns
tAW	Address Valid to End of Write	30	—	45	—	65	—	80	—	105	—	120	—	ns
tAS	Address Set-up Time	0	—	5	—	15	—	15	—	20	—	20	—	ns
tWP	Write Pulse Width	25	—	40	—	40	—	55	—	70	—	90	—	ns
tWR	Write Recovery Time	0	—	5	—	5	—	5	—	5	—	10	—	ns
tWHZ(3)	Write to Output in High-Z	—	25	—	30	—	35	—	40	—	40	—	40	ns
tDW	Data to Write Time Overlap	20	—	25	—	30	—	30	—	35	—	40	—	ns
tDH(4)	Data Hold from Write Time	0	—	5	—	5	—	5	—	5	—	10	—	ns
tOW(3,4)	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	0	—	ns

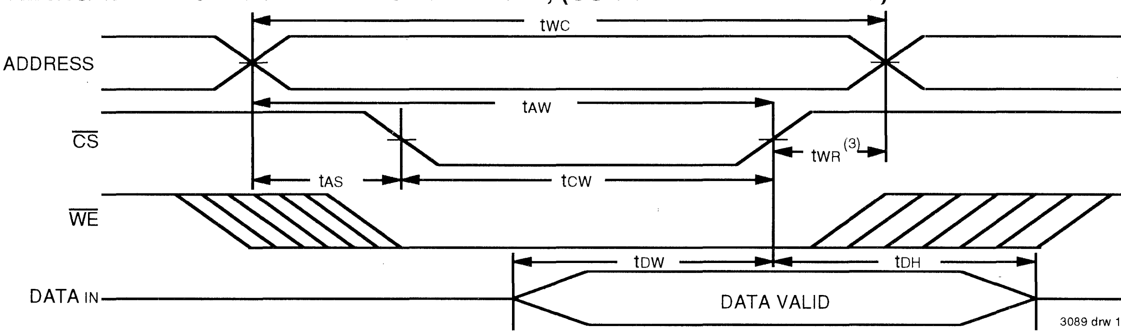
3089 tbl 15

NOTES:
1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter guaranteed with AC Load (Figure 2) by device characterization, but is not production tested.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operation conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 5, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 5, 7)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and the input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state.
6. Transition is measured ±500mV from steady state.
7. $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse is the specified tWP. For a $\overline{CS}$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to tCW.

ORDERING INFORMATION

IDT	6116	XX	XXX	X	X
	Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (-55°C to + 125°C) Compliant to MIL-STD-883, Class B

Package

TP	300 mil Plastic DIP (P24-2)
P	600 mil Plastic DIP (P24-1)
TD	300 mil CERDIP (D24-2)
D	600 mil CERDIP (D24-1)
L28	Leadless Chip Carrier (L28-1)
L32	Leadless Chip Carrier (L32-1)
SO	300 mil Small Outline IC, Gull-Wing Bend (SO24-2)
E	300 mil CERPACK (E24-1)
Y	300 mil SOJ, J-Bend (SO24-4)

Speed — Speed in nanoseconds

15	Commercial Only
20	
25	
35	
45	
55	Military Only
70	Military Only
90	Military Only
120	Military Only
150	Military Only

Power

SA	Standard Power
LA	Low Power

3089 drw 13

5

64K SRAM PRODUCTS

The 64K devices, built with state-of-the-art CMOS processing, offer unmatched capabilities in terms of standby power consumption in their low power versions, while preserving the fast speed attributes typical of IDT SRAMs. Commercial parts are available in speeds as fast as 15ns, while military devices are as fast as 20ns, both in a wide variety of speeds and packages.

The low power consumption characteristics of the "L" power versions makes them ideal for portable instruments and notebook computers, while the standard "S" power fast CMOS parts are well suited for high-performance workstations, PCs, communications, and industrial applications.

Size	Organization	Features	Process	Number	Part Power	Speeds Commercial	Speeds Military
64K	64K x 1		CMOS	7187	S/L	15,20,25	20,25,35,45,55,70,85
	16K x 4		BiCMOS	7188	S/L	20,25	20,25,35,45,55,70,85
	16K x 4	$\overline{OE}$	CMOS	6198	S/L	15,20,25,35	20,25,35,45,55,70,85
	16K x 4	$\overline{OE}$, $\overline{CS2}$	CMOS	7198	S/L	N/A	20,25,35,45,55,70,85
	8K x 8		CMOS	7164	S/L	15,20,25,30	20,25,30,35,45,55, 70,85

6

TABLE OF CONTENTS

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Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (64K x 1-BIT)

IDT7187S
IDT7187L

FEATURES:

- High speed (equal access and cycle time)
  - Military: 20/25/35/45/55/70/85ns (max.)
  - Commercial: 15/20/25ns (max.)
- Low power consumption
- Battery backup operation—2V data retention (L version only)
- JEDEC standard high-density 22-pin plastic and ceramic DIP, 22-pin and 28-pin leadless chip carrier and 24-pin CERPACK
- Produced with advanced CMOS high-performance technology
- Separate data input and output
- Input and output directly TTL-compatible
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

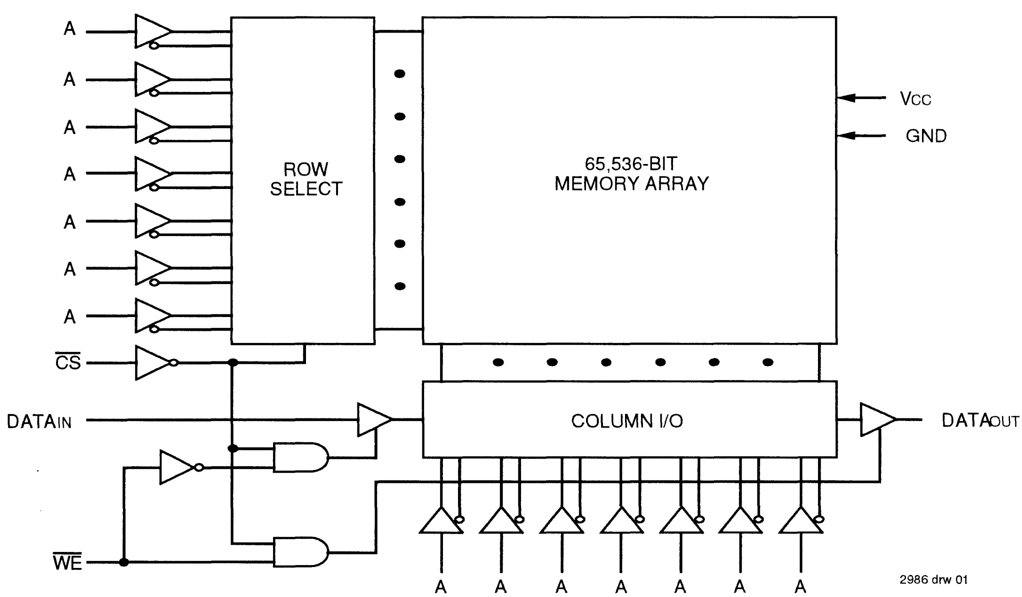
The IDT7187 is a 65,536-bit high-speed static RAM organized as 64K x 1. It is fabricated using IDT's high-performance, high-reliability CMOS technology. Access times as fast as 15ns are available.

Both the standard (S) and low-power (L) versions of the IDT7187 provide two standby modes—ISB and ISB1. ISB provides low-power operation; ISB1 provides ultra-low-power operation. The low-power (L) version also provides the capability for data retention using battery backup. When using a 2V battery, the circuit typically consumes only 30µW.

Ease of system design is achieved by the IDT7187 with full asynchronous operation, along with matching access and cycle times. The device is packaged in an industry standard 22-pin, 300 mil plastic or ceramic DIP, 22- and 28-pin leadless chip carriers, or 24-pin CERPACK.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



The IDT logo is a registered trademark of Integrated Device Technology, Inc.

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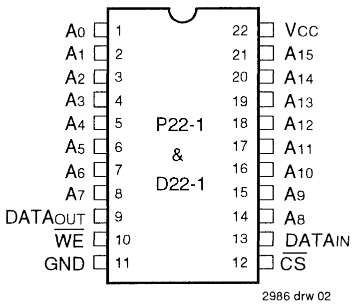
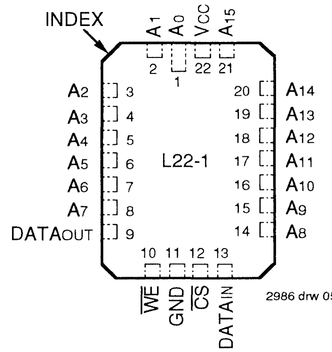
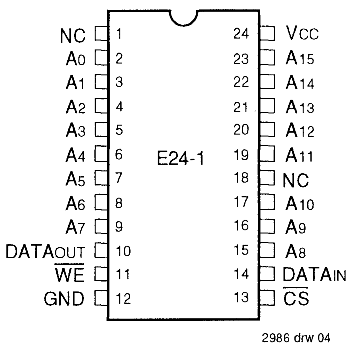
PIN CONFIGURATIONS



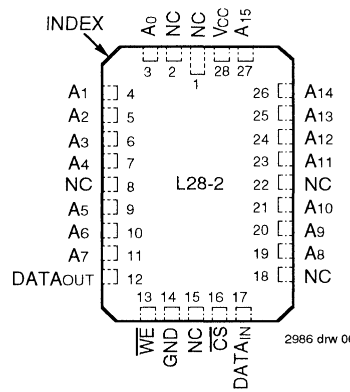
DIP
TOP VIEW



22-PIN LCC
TOP VIEW



CERPACK
TOP VIEW



28-PIN LCC
TOP VIEW

6

PIN DESCRIPTIONS

Name	Description
A_0–A_{15}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
$DATA_{IN}$	Data Input
$DATA_{OUT}$	Data Output
GND	Ground

2986 tbl 01

TRUTH TABLE[1]

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High-Z	Active

NOTE:
1. H = V_{IH}, L = V_{IL}, X = don't care.

2986 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2986 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2986 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2986 tbl 05

1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2986 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition		IDT7187S Min.	IDT7187S Max.	IDT7187L Min.	IDT7187L Max.	Unit
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.			0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2986 tbl 07

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7187S15[3]		7187S20 7187L20		7187S25 7187L25		7187S35 7187L35		7187S45 7187L45		7187S55/70 7187L55/70		7187S85 7187L85		Unit
			Com'l.	Mil.	Com'l.	Mil.[3]	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0[2]	S	100	—	90	105	90	105	—	105	—	105	—	105	—	105	mA
		L	—	—	70	85	70	85	—	85	—	85	—	85	—	85	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = f_{MAX}[2]	S	140	—	130	140	120	130	—	120	—	120	—	120	—	120	mA
		L	—	—	110	120	100	110	—	100	—	95	—	90	—	90	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}[2]	S	60	—	55	65	50	55	—	50	—	50	—	50	—	50	mA
		L	—	—	40	60	35	50	—	40	—	35	—	30/28	—	28	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC}=Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0[2]	S	20	—	15	20	15	20	—	20	—	20	—	20	—	20	mA
		L	—	—	0.3	1.5	0.3	1.5	—	1.5	—	1.5	—	1.5	—	1.5	

NOTES:
2986 tbl 06
1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.
3. These specs are preliminary.

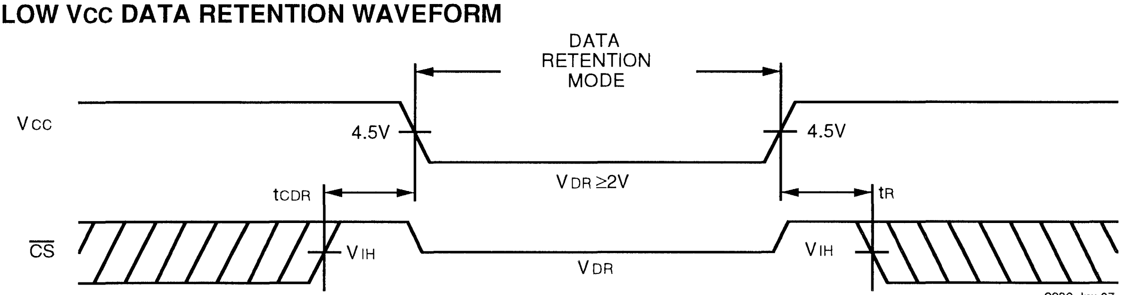
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{HC} = V_{CC} - 0.2V, V_{LC} = 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1] V_{CC} @ 2.0v	Typ.[1] V_{CC} @ 3.0V	Max. V_{CC} @ 2.0V	Max. V_{CC} @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}$ ≥ V_{HC} V_{IN} ≥ V_{HC} or ≤ V_{LC}	MIL.	—	10	15	600	900	µA
			COM'L.	—	10	15	150	225	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns
$\|I_{LI}\|$[3]	Input Leakage Current			—	—	—	2	2	µA

NOTES:
2986 tbl 09
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2986 tbl 10

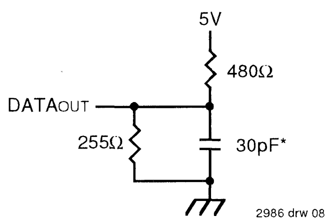


Figure 1. AC Test Load

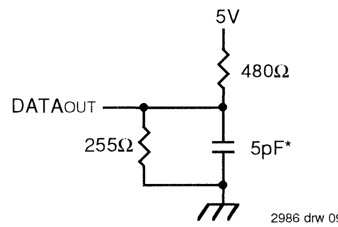


Figure 2. AC Test Load (for tHZ, tLZ, tWZ and tOW)

*Includes scope and jig capacitances

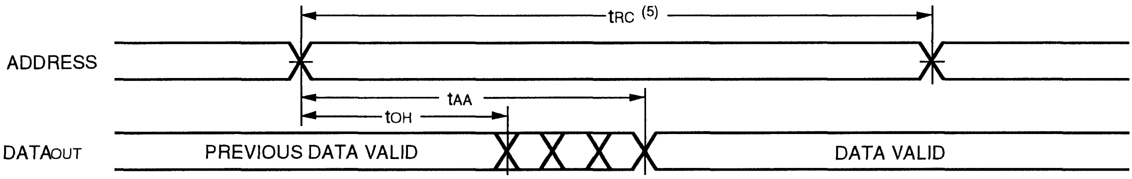
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7187S15(1)/20 7187L20		7187S25 7187L25		7187S35/45(2) 7187L35/45(2)		7187S55(2) 7187L55(2)		7187S70(2) 7187L70(2)		7187S85(2) 7187L85(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle														
tRC	Read Cycle Time	15/20	—	25	—	35/45	—	55	—	70	—	85	—	ns
tAA	Address Access Time	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns
tACS	Chip Select Access Time	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
tLZ(3)	Output Selection to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
tHZ(3)	Chip Deselect to Output in High-Z	—	6	—	12	—	17/20	—	30	—	30	—	40	ns
tPU(3)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD(3)	Chip Deselect to Power-Down Time	—	15/20	—	20	—	30/35	—	35	—	35	—	40	ns

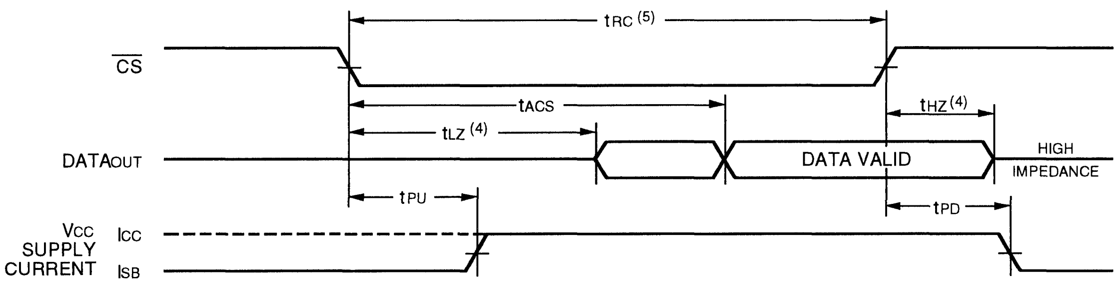
2986 tbl 11

NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1,2)



TIMING WAVEFORM OF READ CYCLE NO. 2(1,3)



NOTES:
1. WE is HIGH for Read cycle.
2. CS is LOW for Read cycle.
3. Address valid prior to or coincident with CS transition LOW.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. All Read cycle timings are referenced from the last valid address to the first transitioning address.

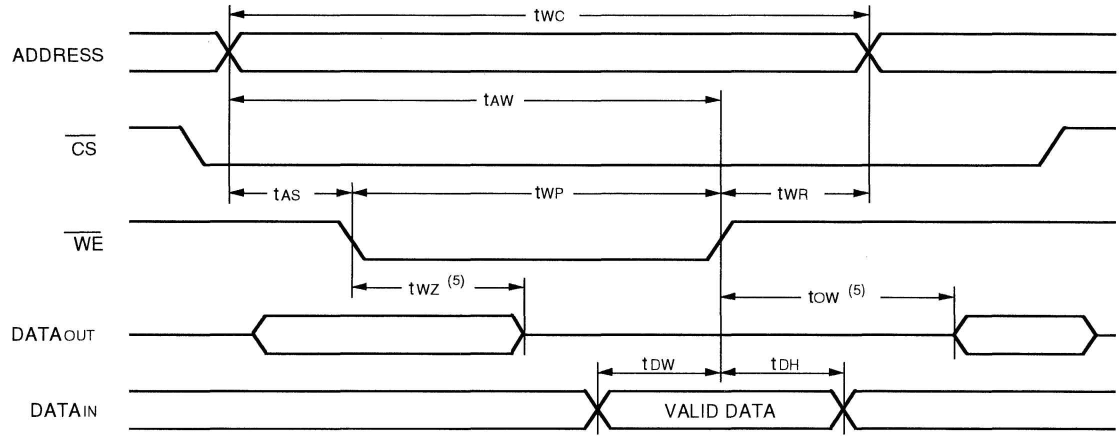
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7187S15(1)/20 7187L20		7187S25 7187L25		7187S35/45(2) 7187L35/45(2)		7187S55(2) 7187L55(2)		7187S70(2) 7187L70(2)		7187S85(2) 7187L85(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle														
tWC	Write Cycle Time	12/15	—	25	—	35/45	—	55	—	70	—	85	—	ns
tCW	Chip Select to End-of-Write	12/15	—	20	—	25/40	—	50	—	55	—	65	—	ns
tAW	Address Valid to End-of-Write	12/15	—	20	—	25/40	—	50	—	55	—	65	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12/15	—	20	—	20/25	—	35	—	40	—	45	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	8/10	—	15	—	15/25	—	25	—	30	—	35	—	ns
tDH	Data Hold Time	0	—	5	—	5	—	5	—	5	—	5	—	ns
tWZ(3)	Write Enable to Output in High-Z	—	6/8	—	12	—	15/30	—	30	—	30	—	40	ns
tOW(3)	Output Active from End-of-Write	0	—	0	—	0	—	0	—	0	—	0	—	ns

2986 tbl 12

NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

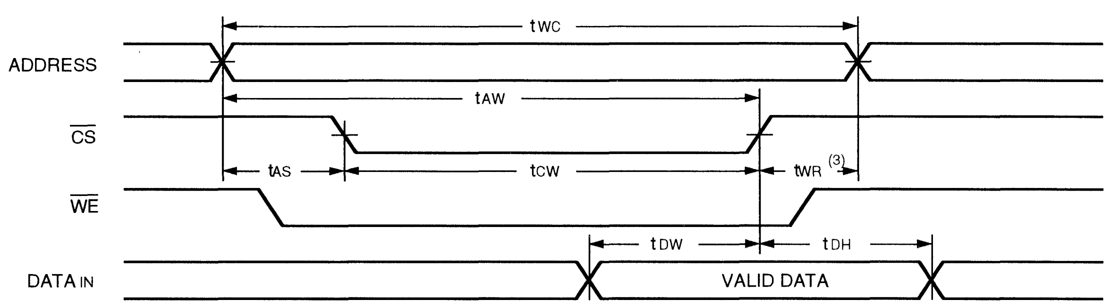
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,4)



2986 drw 12

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state.
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,4)



2986 drw 13

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state.
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

ORDERING INFORMATION

IDT	7187	X	XX	XXX	X
	Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range:

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:

D	300 mil Ceramic DIP (D22-1)
P	300 mil Plastic DIP (P22-1)
L22	Leadless Chip Carrier (L22-1)
L28	Leadless Chip Carrier (L28-2)
E	300 mil CERPACK (E24-1)

Speed (Speed in nanoseconds):

15	Commercial Only
20	
25	
35	Military Only
45	Military Only
55	Military Only
70	Military Only
85	Military Only

Power:

S	Standard Power
L	Low Power

2986 drw 14

6

Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (16K x 4-BIT)

IDT7188S
IDT7188L

FEATURES:

- High-speed (equal access and cycle times)
  - — Military: 20/25/35/45/55/70/85ns (max.)
  - — Commercial: 20/25ns (max.)
- Low power consumption
- Battery backup operation — 2V data retention (L version only)
- Available in high-density industry standard 22-pin, 300 mil ceramic and plastic DIP, and CERPACK
- Produced with advanced CMOS technology
- Inputs/outputs TTL-compatible
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

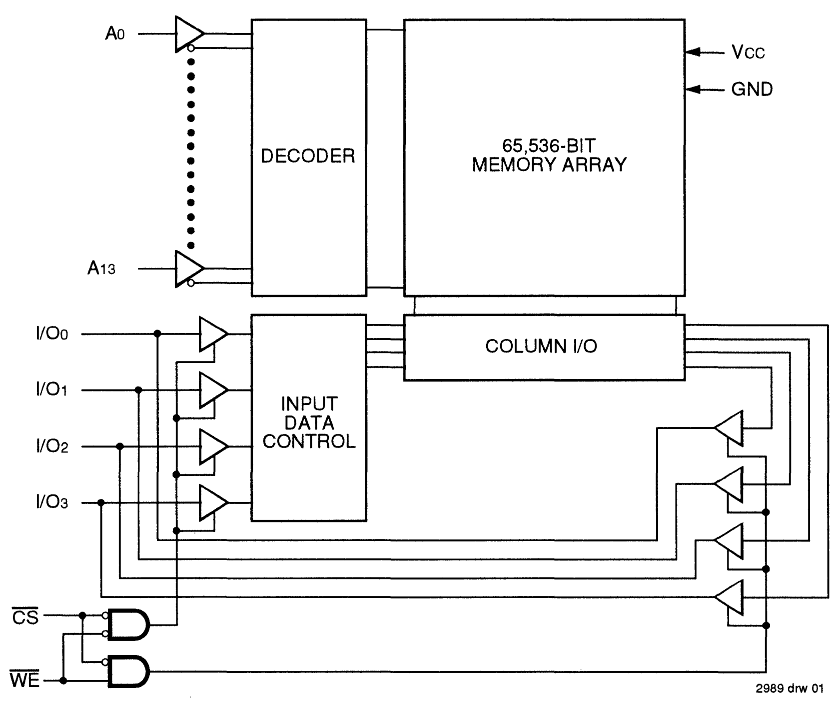
The IDT7188 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology — CMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

Access times as fast as 20ns are available. The IDT7188 offers a reduced power standby mode, ISB1, which is activated when $\overline{CS}$ goes HIGH. This capability significantly decreases power while enhancing system reliability. The low-power version (L) version also offers a battery backup data retention capability where the circuit typically consumes only 30µW operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5V supply. The IDT7188 is packaged in 22-pin, 300 mil ceramic and plastic DIPs, 24-pin CERPACKs, providing excellent board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



The IDT logo is a registered trademark of Integrated Device Technology, Inc.

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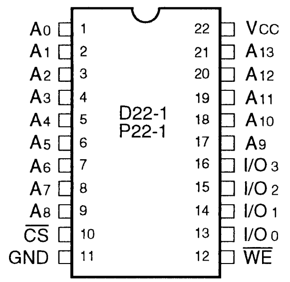
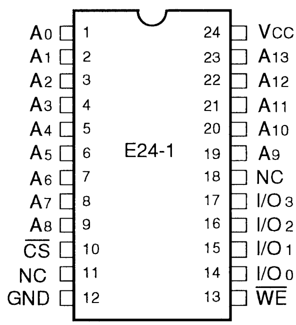
PIN CONFIGURATIONS



2989 drw 02

DIP
TOP VIEW



2989 drw 03

CERPACK/SOJ
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A_0–A_{13}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
I/O_{0-3}	Data Input/Output
V_{CC}	Power
GND	Ground

2989 tbl 01

TRUTH TABLE(1)

Mode	$\overline{CS}$	$\overline{WE}$	I/O	Power
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

NOTE: 2989 tbl 02
1. H = V_{IH}, L = V_{IL}, X = don't care.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2989 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{CC} = 0v))

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	6	pF

NOTE: 2989 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2989 tbl 05
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns,once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2989 tbl 06

6

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT7188S Min.	IDT7188S Max.	IDT7188L Min.	IDT7188L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.			0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2989 tbl 07

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7188S20 7188L20 Com'l.	7188S20 7188L20 Mil.	7188S25 7188L25 Com'l.	7188S25 7188L25 Mil.	7188S35 7188L35 Com'l.	7188S35 7188L35 Mil.	7188S45 7188L45 Com'l.	7188S45 7188L45 Mil.	7188S55/70 7188L55/70 Com'l.	7188S55/70 7188L55/70 Mil.	7188S85 7188L85 Com'l.	7188S85 7188L85 Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0(2)	S	100	105	100	105	—	105	—	105	—	105	—	105	mA
		L	70	80	70	80	—	80	—	80	—	80	—	80	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = f_{MAX}(2)	S	125	160	125	155	—	140	—	140	—	140	—	140	mA
		L	115	130	105	120	—	115	—	110	—	110	—	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	S	55	70	50	60	—	50	—	50	—	50	—	50	mA
		L	40	50	35	40	—	40	—	35	—	35	—	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC}=Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0(2)	S	15	25	15	20	—	20	—	20	—	20	—	20	mA
		L	0.5	1.5	0.5	1.5	—	1.5	—	1.5	—	1.5	—	1.5	

NOTES:

2989 tbl 06

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

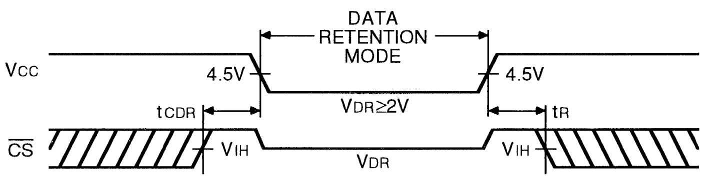
(L Version Only) $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Condition		Min.	Typ. (1) Vcc @ 2.0v	Typ. (1) Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	—	10	15	600	900	µA
			COM'L.	—	10	15	150	225	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—	—	2	2	µA

NOTES:
2989 tbl 09

1. $T_A = +25°C$.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization but is not production tested.

LOW Vcc DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2989 tbl 10

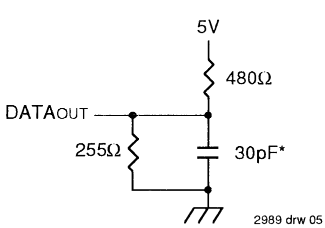


Figure 1. AC Test Load

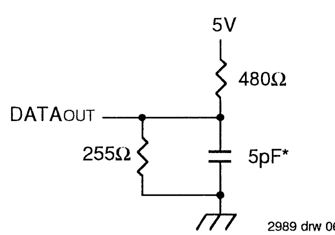


Figure 2. AC Test Load
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OHZ} and t_{OW})

*Includes scope and jig capacitances

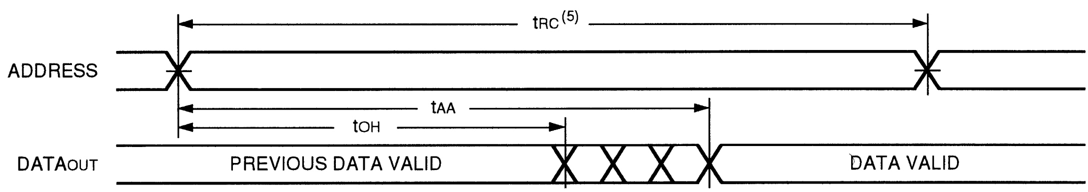
6

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7188S20 7188L20 Min.	Max.	7188S25 7188L25 Min.	Max.	7188S35/45(1) 7188L35/45(1) Min.	Max.	7188S55/70(1) 7188L55/70(1) Min.	Max.	7188S85(1) 7188L85(1) Min.	Max.	Unit
Read Cycle												
t_{RC}	Read Cycle Time	20	—	25	—	35/45	—	55/70	—	85	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35/45	—	55/70	—	85	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	35/45	—	55/70	—	85	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
$t_{LZ}^{(2)}$	Output Selection to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	ns
$t_{HZ}^{(2)}$	Chip Deselect to Output in High-Z	—	8	—	10	—	14	—	20/25	—	30	ns
$t_{PU}^{(2)}$	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
$t_{PD}^{(2)}$	Chip Deselect to Power Down Time	—	20	—	25	—	35/45	—	55/70	—	85	ns

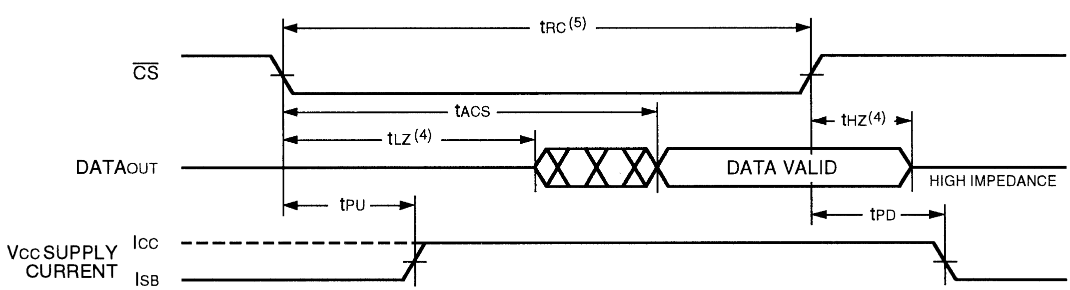
NOTES: 2989 tbl 11
1. –55°C to +125°C temperature range only.
2. This parameter is guaranteed by device characterization but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1, 2)



2989 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 3)



2989 drw 08

NOTES:
1. $\overline{WE}$ is HIGH for Read cycle.
2. $\overline{CS}$ is LOW for Read cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. Transition is measured ±200mV from steady state voltage.
5. All Read cycle timings are referenced from the last valid address to the first transitioning address.

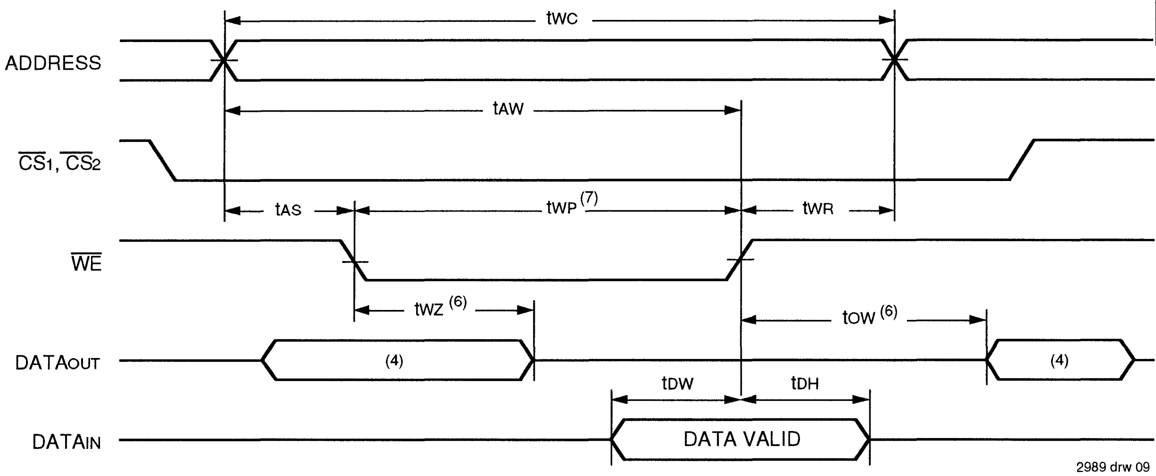
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7188S20 7188L20 Min.	Max.	7188S25 7188L25 Min.	Max.	7188S35/45(1) 7188L35/45(1) Min.	Max.	7188S55/70(1) 7188L55/70(1) Min.	Max.	7188S85(1) 7188L85(1) Min.	Max.	Unit
Write Cycle												
tWC	Write Cycle Time	17	—	20	—	30/40	—	50/60	—	75	—	ns
tCW	Chip Select to End-of-Write	17	—	20	—	25/35	—	50/60	—	75	—	ns
tAW	Address Valid to End-of-Write	17	—	20	—	25/35	—	50/60	—	75	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	17	—	20	—	25/35	—	50/60	—	75	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	10	—	13	—	15/20	—	25/30	—	35	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ(2)	Write Enable to Output in High-Z	—	6	—	7	—	10/15	—	25/30	—	40	ns
tOW(2)	Output Active from End-of-Write	5	—	5	—	5	—	5	—	5	—	ns

2989 tbl 12

NOTES:
1. –55°C to +125°C temperature range only.
2. This parameter is guaranteed by device characterization.

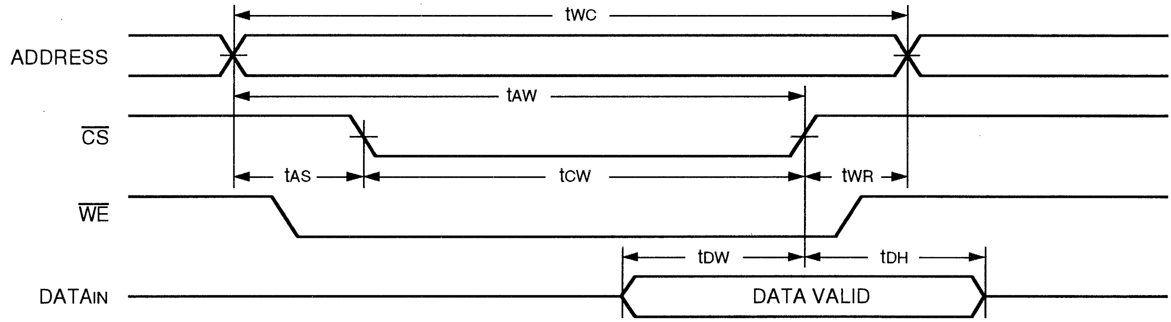
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals should not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state.
6. Transition is measured ±200mV from steady state.

6

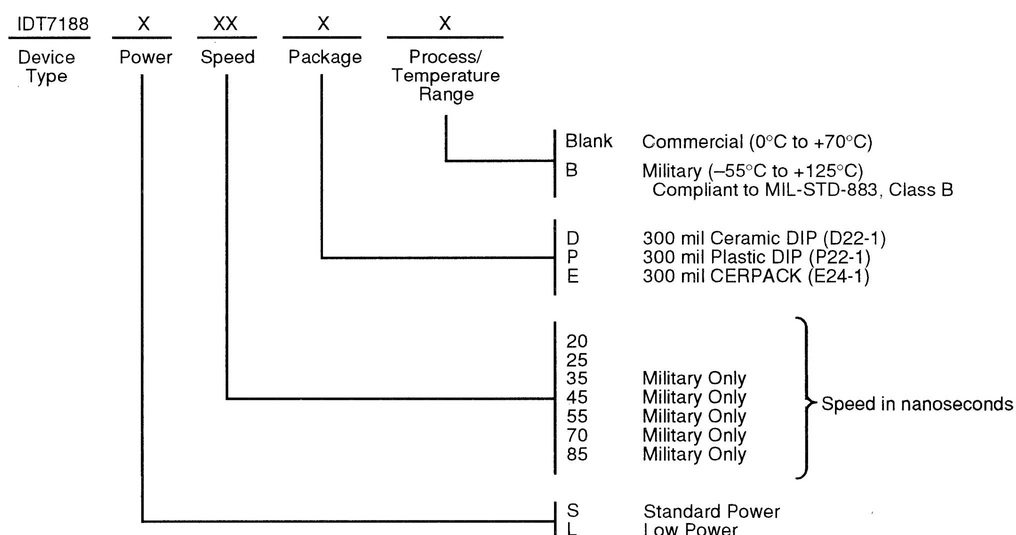
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,3,5)



2989 drw 10

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals should not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state.
6. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



2989 drw 11

CMOS STATIC RAM 64K (16K x 4-BIT) with Output Control

IDT6198S
IDT6198L

FEATURES:

- High-speed (equal access and cycle times)
  - — Military: 20/25/35/45/55/70/85ns (max.)
  - — Commercial: 15/20/25/35ns (max.)
- Output Enable ($\overline{OE}$) pin available for added system flexibility
- Low-power consumption
- JEDEC compatible pinout
- Battery back-up operation—2V data retention (L version only)
- 24-pin CERDIP, high-density 28-pin leadless chip carrier, and 24-pin SOJ
- Produced with advanced CMOS technology
- Bidirectional data inputs and outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT6198 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective approach for memory intensive applications. Timing parameters have been specified to meet the speed demands of the IDT79R3000 RISC processors.

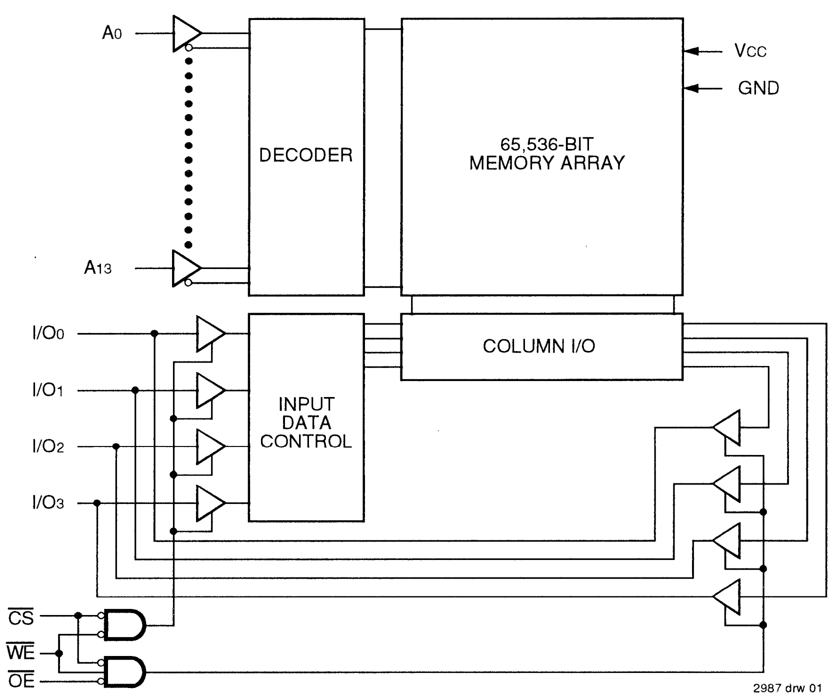
Access times as fast as 15ns are available. The IDT6198 offers a reduced power standby mode, I_{SB1}, which is activated when $\overline{CS}$ goes HIGH. This capability significantly decreases system, while enhancing system reliability. The low-power version (L) also offers a battery backup data retention capability where the circuit typically consumes only 30µW when operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5V supply.

The IDT6198 is packaged in either a 24-pin 300 mil CERDIP, 28-pin leadless chip carrier or 24-pin J-bend small outline IC.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



2987 drw 01

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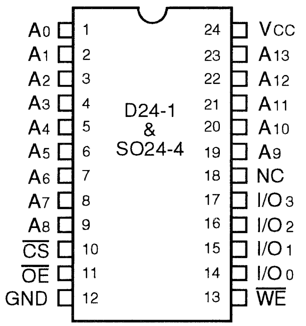
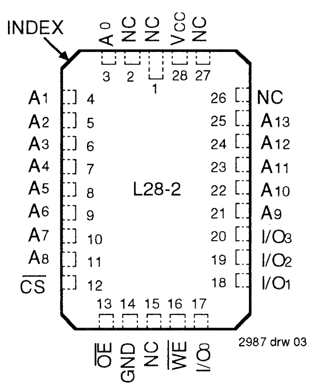
PIN CONFIGURATIONS



DIP/SOJ
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0–A13	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O0–I/O3	Data Input/Output
VCC	Power
GND	Ground

2987 tbl 01

TRUTH TABLE(1)

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Standby	H	X	X	High-Z	Standby
Read	L	H	L	DATAOUT	Active
Write	L	L	X	DATAIN	Active
Read	L	H	H	High-Z	Active

NOTE: 2987 tbl 02
1. H = VIH, L = VIL, X = Don't Care

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE: 2987 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	7	pF
CI/O	I/O Capacitance	VOUT = 0V	7	pF

NOTE: 2987 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2987 tbl 05
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2987 tbl 06

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT6198S Min.	IDT6198S Max.	IDT6198L Min.	IDT6198L Max.	Unit
|I_{LI}|	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
|I_{LO}|	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.			0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2987 tbl 07

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6198S15 6198L15 Com'l.	Mil.	6198S20 6198L20 Com'l.	Mil.	6198S25 6198L25 Com'l.	Mil.	6198S35 6198L35 Com'l.	Mil.	6198S45 6198L45 Com'l.	Mil.	6198S55/70/85 6198L55/70/85 Com'l.	Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0(2)	S	100	—	100	105	100	105	100	105	—	105	—	105	mA
		L	75	—	70	80	70	80	70	80	—	80	—	80	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = f_{MAX}(2)	S	135	—	130	160	125	155	125	140	—	140	—	140	mA
		L	125	—	115	130	105	120	105	115	—	110	—	110	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	S	60	—	55	70	50	60	45	50	—	50	—	50	mA
		L	45	—	40	50	35	40	30	35	—	35	—	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC}=Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0(2)	S	20	—	15	25	15	20	15	20	—	20	—	20	mA
		L	1.5	—	0.5	1.5	0.5	1.5	0.5	1.5	—	1.5	—	1.5	

NOTES: 2987 tbl 06
1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

6

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

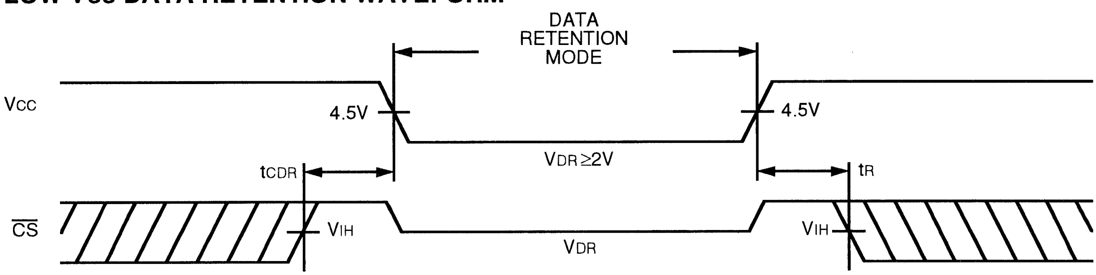
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ. (1) Vcc @ 2.0v	Typ. (1) Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL.	—	10	15	600	900	µA
			COM'L.	—	10	15	150	225	
t_{CDR}(3)	Chip Deselect to Data Retention Time	$\overline{CS} \geq V_{HC}$, $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		0	—	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—	—	2	2	µA

2987 tbl 09

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization but is not production tested.

LOW V_{CC} DATA RETENTION WAVEFORM

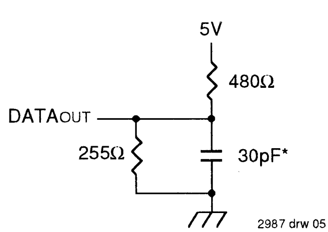


2987 drw 04

AC TEST CONDITIONS

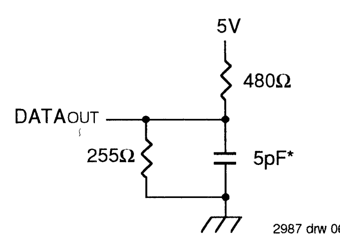
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2987 tbl 10



2987 drw 05

Figure 1. AC Test Load



2987 drw 06

Figure 2. AC Test Load
(for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{CHZ} and t_{OW})

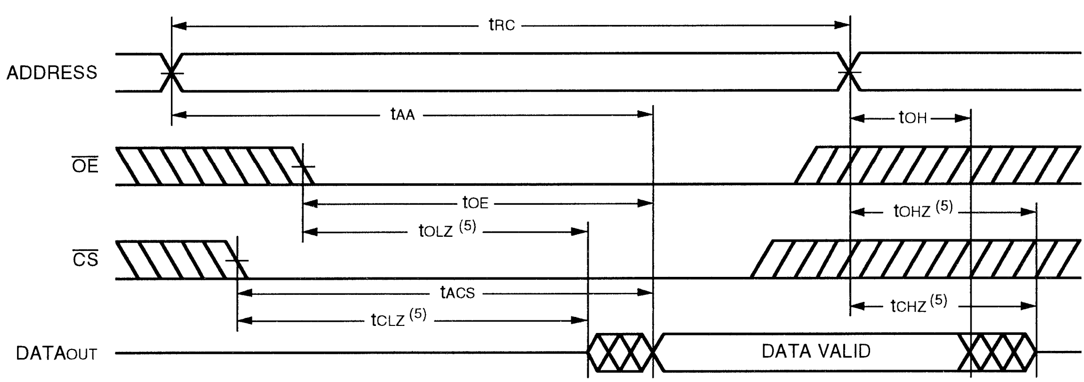
*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6198S15[1] 6198L15[1]		6198S20 6198L20		6198S25 6198L25		6198S35 6198L35		6198S45/55[2] 6198L45/55[2]		6198S70/85[2] 6198L70/85[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle														
tRC	Read Cycle Time	15	—	20	—	25	—	35	—	45/55	—	70/85	—	ns
tAA	Address Access Time	—	15	—	19	—	25	—	35	—	45/55	—	70/85	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	—	35	—	45/55	—	70/85	ns
tCLZ[3]	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	8	—	9	—	11	—	18	—	25/35	—	45/55	ns
tOLZ[3]	Output Enable to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
tCHZ[3]	Chip Select to Output in High-Z	2	7	2	8	2	10	2	14	—	15/20	—	25/30	ns
tOHZ[3]	Output Disable to Output in High-Z	2	7	2	8	2	9	2	15	—	15/20	—	25/30	ns
tOH	Output Hold from Address Change	5	—	5	—	2	—	5	—	5	—	5	—	ns
tPU[3]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD[3]	Chip Deselect to Power Down Time	—	15	—	20	—	25	—	35	—	45/55	—	70/85	ns

NOTES:
2987 tbl 11
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter is guaranteed by device characterization but is not production tested.

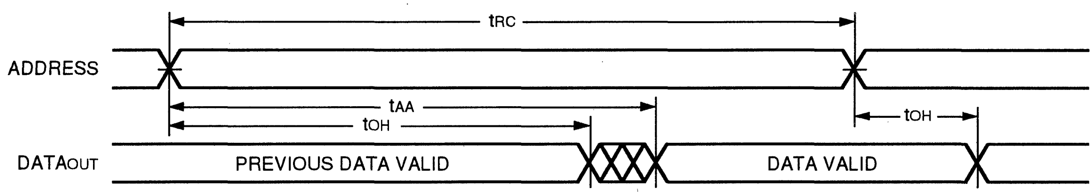
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



2987 drw 07

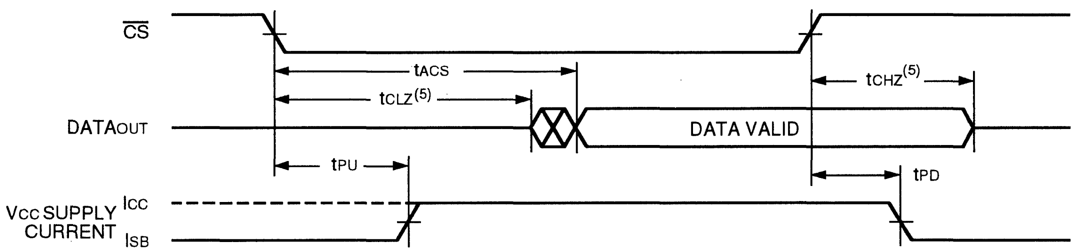
NOTES:
1. WE is HIGH for Read cycle.
2. Device is continuously selected, CS is LOW.
3. Address valid prior to or coincident with CS transition LOW.
4. OE is LOW.
5. Transition is measured ±200mV from steady state voltage.

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2987 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



2987 drw 09

NOTES:
1. WE is HIGH for Read cycle.
2. Device is continuously selected, CS is LOW.
3. Address valid prior to or coincident with CS transition LOW.
4. OE is LOW.
5. Transition is measured ±200mV from steady state voltage.

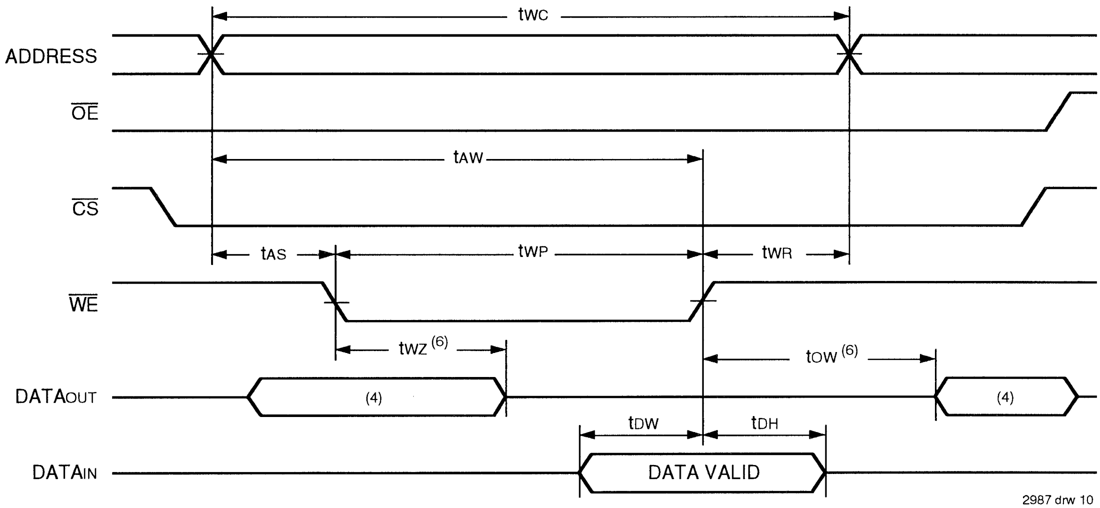
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6198S15(1) 6198L15(1) Min.	Max.	6198S20 6198L20 Min.	Max.	6198S25 6198L25 Min.	Max.	6198S35 6198L35 Min.	Max.	6198S45/55(2) 6198L45/55(2) Min.	Max.	6198S70/85(2) 6198L70/85(2) Min.	Max.	Unit
Write Cycle														
tWC	Write Cycle Time	14	—	17	—	20	—	30	—	40/50	—	60/75	—	ns
tCW	Chip Select to End-of-Write	14	—	17	—	20	—	25	—	35/50	—	60/75	—	ns
tAW	Address Valid to End-of-Write	14	—	17	—	20	—	25	—	35/50	—	60/75	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	14	—	17	—	20	—	25	—	35/50	—	60/75	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWHZ(3)	Write Enable to Output in High-Z	—	5	—	6	—	7	—	10	—	15/25	—	30/40	ns
tDW	Data Valid to End-of-Write	10	—	10	—	13	—	15	—	20/25	—	30/35	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tOW(3)	Output Active from End-of-Write	5	—	5	—	5	—	5	—	5	—	5	—	ns

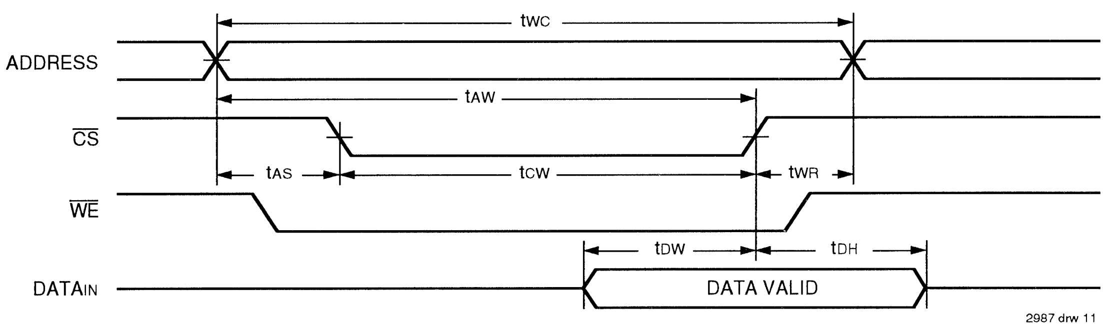
2987 tbl 12

NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter is guaranteed by device characterization, but is not production tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

6

ORDERING INFORMATION

IDT6198	X	XX	X	X
Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package

D	300 mil CERDIP (D24-1)
L	Leadless Chip Carrier (L28-2)
Y	Small Outline IC J-Bend (SO24-4)

Speed (Speed in nanoseconds)

15	Commercial Only
20	
25	
35	
45	Military Only
55	Military Only
70	Military Only
85	Military Only

Power

S	Standard Power
L	Low Power

2987 drw 12

CMOS STATIC RAMs
64K (16K x 4-BIT)
Added Chip Select and Output Controls

IDT7198S
IDT7198L

FEATURES:

- Fast Output Enable ($\overline{OE}$) pin available for added system flexibility
- Multiple Chip Selects ($\overline{CS}_1$, $\overline{CS}_2$) simplify system design and operation
- High speed (equal access and cycle times)
  — Military: 20/25/35/45/55/70/85ns (max.)
- Low power consumption
- Battery back-up operation—2V data retention (L version only)
- 24-pin CERDIP, high-density 28-pin leadless chip carrier, and 24-pin CERPACK packaging available
- Produced with advanced CMOS technology
- Bidirectional data inputs and outputs
- Inputs/outputs TTL-compatible
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7198 is a 65,536 bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

Access times as fast as 20ns are available. The IDT7198 offers a reduced power standby mode, I_{SB1}, which is activated when $\overline{CS}_1$ or $\overline{CS}_2$ goes HIGH. This capability decreases power, while enhancing system reliability. The low-power version (L) also offers a battery backup data retention capability where the circuit typically consumes only 30µW when operating from a 2V battery.

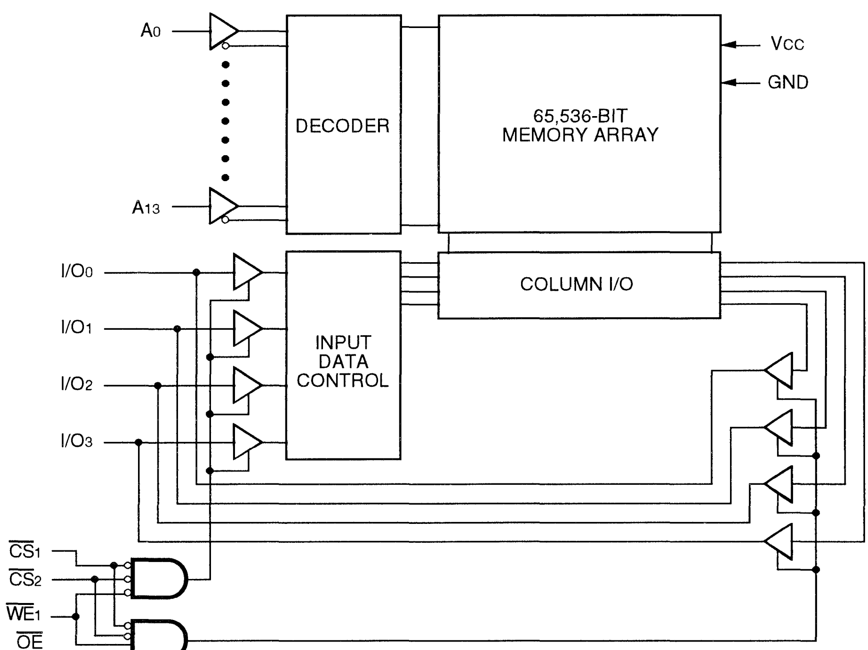
All inputs and outputs are TTL-compatible and operate from a single 5V supply.

The IDT7198 is packaged in either a 24-pin ceramic DIP, 28-pin leadless chip carrier, and 24-pin CERPACK.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

6

FUNCTIONAL BLOCK DIAGRAM



2985 drw 01

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MEMORY CONTROL

The IDT7198 64K high-speed CMOS static RAM incorporates two additional memory control features (an extra chip select and an output enable pin) which offer additional benefits in many system memory applications.

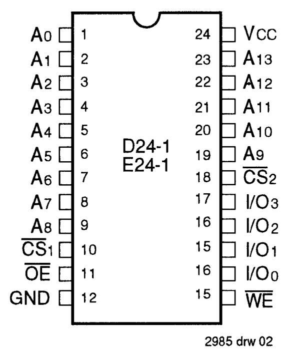
Both chip selects, Chip Select 1 ($\overline{CS_1}$) and Chip Select 2 ($\overline{CS_2}$), must be LOW to select the memory. If either chip select is pulled HIGH, the memory will be deselected and remain in the standby mode. This dual chip select feature ($\overline{CS_1}$, $\overline{CS_2}$) also brings the convenience of improved system speeds to the large memory designer by reducing the external logic required to perform decoding.

PIN DESCRIPTIONS

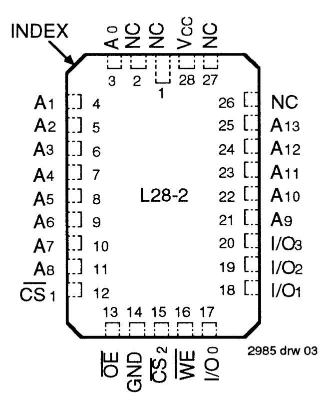
Name	Description
A_0–A_{13}	Address Inputs
$\overline{CS_1}$	Chip Select 1
$\overline{CS_2}$	Chip Select 2
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_0–I/O_3	Data I/O
VCC	Power
GND	Ground

2985 tbl 01

PIN CONFIGURATIONS



DIP/SOJ/CERPACK TOP VIEW



LCC TOP VIEW

TRUTH TABLE(1)

Mode	$\overline{CS_1}$	$\overline{CS_2}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Standby	H	X	X	X	High-Z	Standby
Standby	X	H	X	X	High-Z	Standby
Read	L	L	H	L	DOUT	Active
Write	L	L	L	X	DIN	Active
Read	L	L	H	H	High-Z	Active

NOTE: 2985 tbl 02

1. H = V_{IH}, L = V_{IL}, X = don't care.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE: 2985 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2985 tbl 05
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5V ± 10%

2985 tbl 06

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{CC} = 0V)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2985 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, Military Temperature Range Only

Symbol	Parameter	Test Condition	IDT7198S Min.	IDT7198S Max.	IDT7198L Min.	IDT7198L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.	—	0.4	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	2.4	—	V

2985 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2985 tbl 10

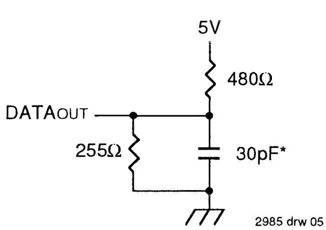


Figure 1. AC Test Load

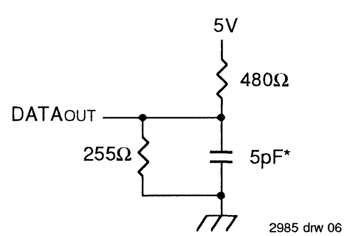


Figure 2. AC Test Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW} and t_{WHZ})

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS(1)

(VCC = 5V ± 10%, VLC = 0.2V, VHC = VCC - 0.2V)

Symbol	Parameter	Power	7198S20 7198L20 Military	7198S25 7198L25 Military	7198S35 7198L35 Military	7198S45 7198L45 Military	7198S55/70 7198L55/70 Military	7198S85 7198L85 Military	Unit
I_{CC1}	Operating Power Supply Current, $\overline{CS}_1$ and $\overline{CS}_2 \leq V_{IL}$, Outputs Open V_{CC} = Max., f = 0(2)	S	105	105	105	105	105	105	mA
		L	80	80	80	80	80	80	
I_{CC2}	Dynamic Operating Current, $\overline{CS}_1$ and $\overline{CS}_2 \leq V_{IL}$, Outputs Open V_{CC} = Max., f = f_{MAX}(2)	S	160	155	140	140	140	140	mA
		L	130	120	115	110	110	105	
I_{SB}	Standby Power Supply Current (TTL Level), $\overline{CS}_1$ or $\overline{CS}_2 \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	S	70	60	50	50	50	50	mA
		L	50	40	35	35	35	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}_1$ or $\overline{CS}_2 \geq V_{HC}$, V_{CC}= Max., $V_{IN} \geq V_{HC}$ or $V_{IN} \leq V_{LC}$, f = 0(2)	S	25	20	20	20	20	20	mA
		L	1.5	1.5	1.5	1.5	1.5	1.5	

NOTES:
2985 tbl 06
1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.

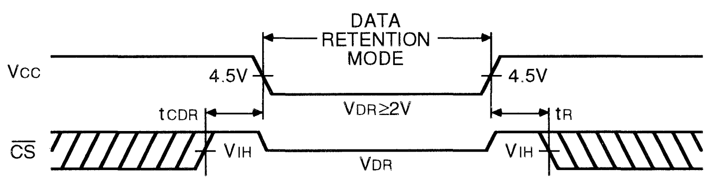
DATA RETENTION CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE

(L Version Only) VLC = 0.2V, VHC = VCC - 0.2V

Symbol	Parameter	Test Condition	Min.	Typ. (1) VCC @ 2.0v	Typ. (1) VCC @ 3.0V	Max. VCC @ 2.0V	Max. VCC @ 3.0V	Unit
V_{DR}	VCC for Data Retention	—	2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}_1$ or $\overline{CS}_2 \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	—	10	15	600	900	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time		0	—	—	—	—	ns
t_R(3)	Operation Recovery Time		t_{RC}(2)	—	—	—	—	ns
$\|I_{LI}\|$(3)	Input Leakage Current		—	—	—	2	2	µA

NOTES:
2985 tbl 09
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization but is not production tested.

LOW VCC DATA RETENTION WAVEFORM



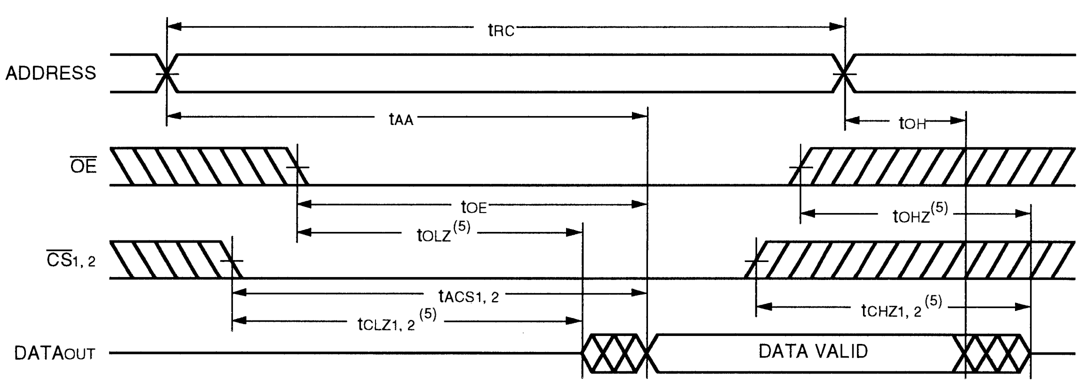
2985 drw 04

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, Military Temperature Range)

Symbol	Parameter	7198S20 7198L20 Min.	Max.	7198S25 7198L25 Min.	Max.	7198S35/45 7198L35/45 Min.	Max.	7198S55 7198L55 Min.	Max.	7198S70 7198L70 Min.	Max.	7198S85 7198L85 Min.	Max.	Unit
Read Cycle														
t_{RC}	Read Cycle Time	20	—	25	—	35/45	—	55	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	19	—	25	—	35/45	—	55	—	70	—	85	ns
$t_{ACS1,2}$[1]	Chip Select-1,2 Access Time	—	20	—	25	—	35/45	—	55	—	70	—	85	ns
$t_{CLZ1,2}$[2]	Chip Select-1,2 to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	9	—	11	—	20/25	—	35	—	45	—	55	ns
t_{OLZ}[2]	Output Enable to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
$t_{CHZ1,2}$[2]	Chip Select 1,2 to Output in High-Z	—	8	—	10	—	14	—	20	—	25	—	30	ns
t_{OHZ}[2]	Output Disable to Output in High-Z	—	8	—	9	—	15	—	20	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}[2]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[2]	Chip Deselect to Power Down Time	—	20	—	25	—	35/45	—	55	—	70	—	85	ns

NOTES: 2985 tbl 11
1. Both chip selects must be active low for the device to be selected.
2. This parameter is guaranteed by device characterization but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



2985 drw 07

NOTES:
1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continuously selected, $\overline{CS_1}$ is LOW, $\overline{CS_2}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS_1}$ and or $\overline{CS_2}$ transition LOW.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state voltage.

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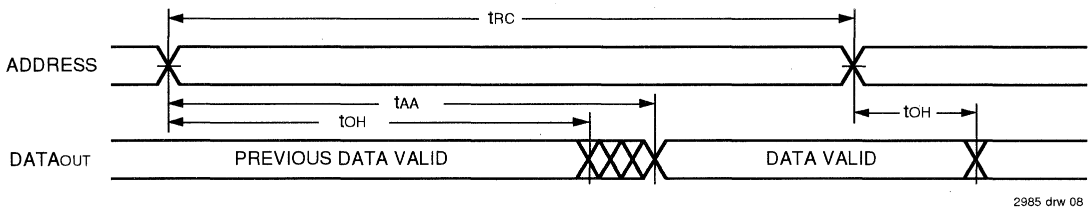
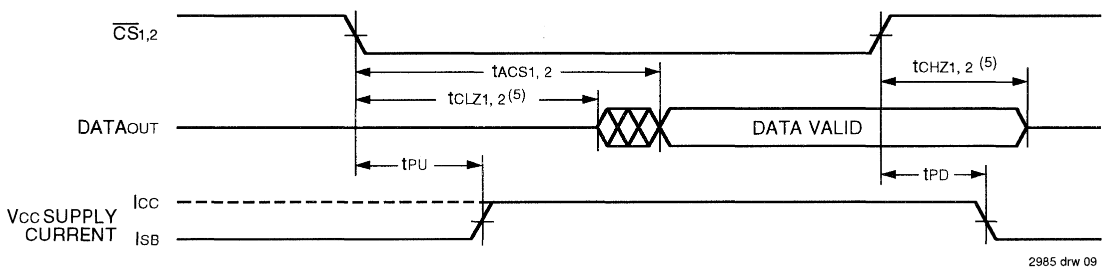
TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



NOTES:
1. WE is HIGH for Read cycle.
2. Device is continuously selected, CS1 is LOW, CS2 is LOW.
3. Address valid prior to or coincident with CS1 and or CS2 transition LOW.
4. OE is LOW.
5. Transition is measured ±200mV from steady state voltage.

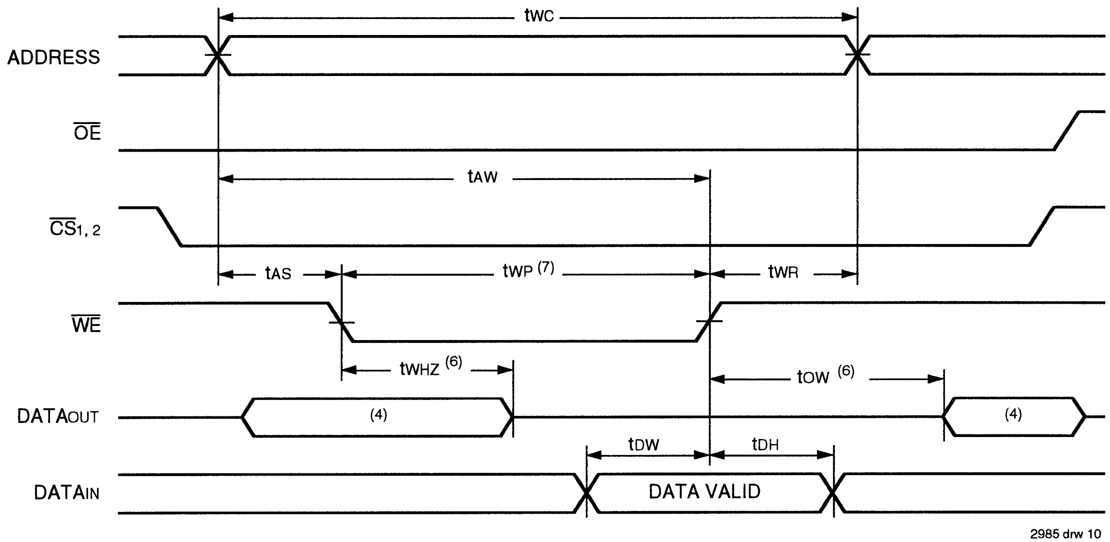
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7198S20 7198L20 Min.	Max.	7198S25 7198L25 Min.	Max.	7198S35/45 7198L35/45 Min.	Max.	7198S55 7198L55 Min.	Max.	7198S70 7198L70 Min.	Max.	7198S85 7198L85 Min.	Max.	Unit
Write Cycle														
tWC	Write Cycle Time	17	—	20	—	30/40	—	50	—	60	—	75	—	ns
tCW1,2(1)	Chip Select to End-of-Write	17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tAW	Address Valid to End-of-Write	17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tWR1,2	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWHZ(2)	Write Enable to Output in High-Z	—	5/6	—	7	—	10/15	—	25	—	30	—	40	ns
tDW	Data Valid to End-of-Write	10	—	13	—	15/20	—	25	—	30	—	35	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tOW(2)	Output Active from End-of-Write	5	—	5	—	5	—	5	—	5	—	5	—	ns

2985 tbl 12

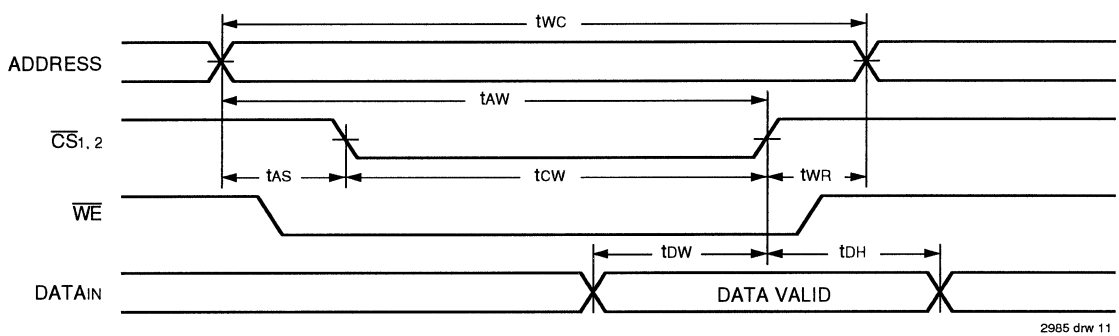
NOTES:
1. Both chip selects must be active low for the device to be selected.
2. This parameter is guaranteed by device characterization but is not production tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



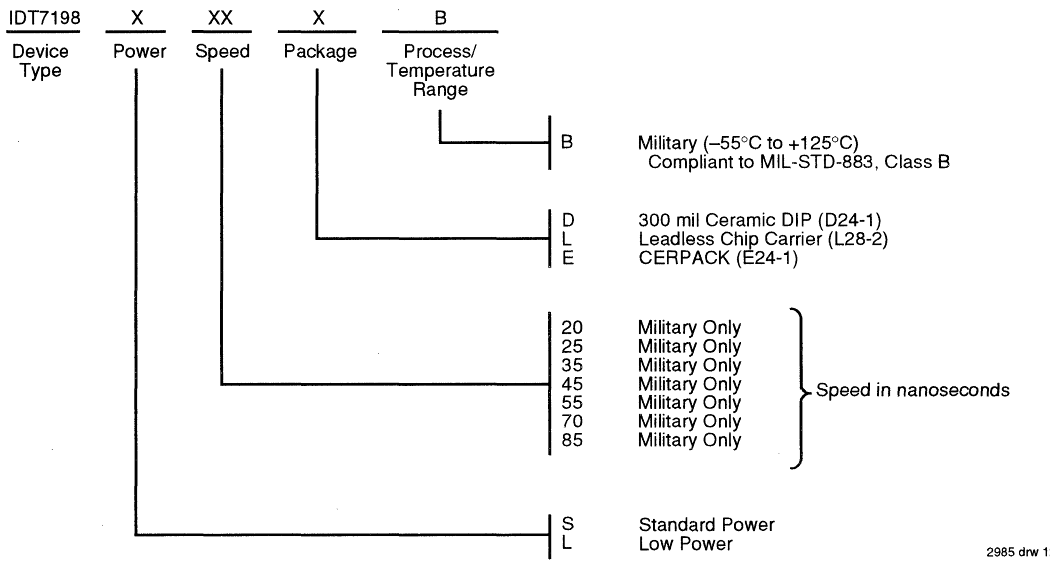
6

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1)



NOTES:
1. $\overline{WE}$, $\overline{CS_1}$ or $\overline{CS_2}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW $\overline{WE}$, a LOW $\overline{CS_1}$ and a LOW $\overline{CS_2}$.
3. t_{WR} is measured from the earlier of $\overline{CS_1}$, $\overline{CS_2}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, outputs remain in the high-impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

ORDERING INFORMATION



CMOS STATIC RAM 64K (8K x 8-BIT)

IDT7164S
IDT7164L

Integrated Device Technology, Inc.

FEATURES:

- High-speed address/chip select access time
  - — Military: 20/25/30/35/45/55/70/85ns (max.)
  - — Commercial: 15/20/25/30/35ns (max.)
- Low power consumption
- Battery backup operation — 2V data retention voltage (L Version only)
- Produced with advanced CMOS high-performance technology
- Inputs and outputs directly TTL-compatible
- Three-state outputs
- Available in:
  - — 28-pin DIP, SOIC, SOJ, and CERPACK
  - — 32-pin LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7164 is a 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

Address access times as fast as 15ns are available and the circuit offers a reduced power standby mode. When $\overline{CS_1}$ goes HIGH or CS_2 goes LOW, the circuit will automatically go to, and remain in, a low-power stand by mode. The low-power (L) version also offers a battery backup data retention capability at power supply levels as low as 2V.

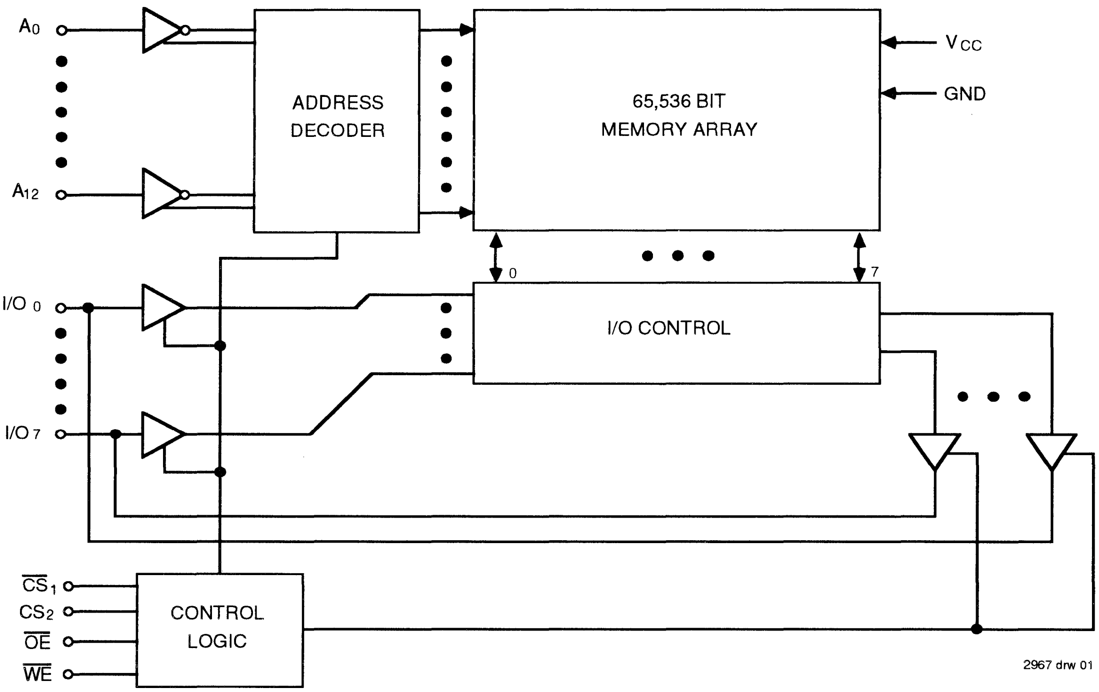
All inputs and outputs of the IDT7164 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7164 is packaged in a 28-pin 300 mil DIP and SOJ; 28-pin 330 mil SOIC; 28-pin 600 mil DIP; 32-pin LCC; and 28-pin CERPACK.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

6

FUNCTIONAL BLOCK DIAGRAM



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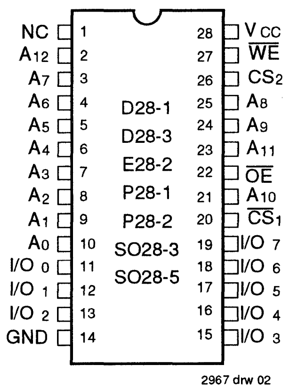
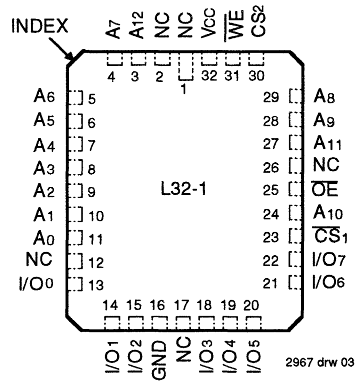
PIN CONFIGURATIONS



DIP/SOIC/SOJ/CERPACK
TOP VIEW



32-PIN LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A_0–A_{12}	Address
I/O_0–I/O_7	Data Input/Output
$\overline{CS_1}$	Chip Select
CS_2	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
VCC	Power

2967 tbl 01

TRUTH TABLE(1,2,3)

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	I/O	Function
X	H	X	X	High-Z	Deselected – Standby (I_{SB})
X	X	L	X	High-Z	Deselected – Standby (I_{SB})
X	VHC	VHC or VLC	X	High-Z	Deselected –Standby (I_{SB1})
X	X	VLC	X	High-Z	Deselected –Standby (I_{SB1})
H	L	H	H	High-Z	Output Disabled
H	L	H	L	$Data_{OUT}$	Read Data
L	L	H	X	$Data_{IN}$	Write Data

NOTES: 2967 tbl 02
1. CS_2 will power-down $\overline{CS_1}$, but $\overline{CS_1}$ will not power-down CS_2.
2. H = V_{IH}, L = V_{IL}, X = don't care.
3. V_{LC} = 0.2V, V_{HC} = Vcc - 0.2V

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTES: 2967 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed VCC + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	VCC
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2967 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input HIGH Voltage	2.2	—	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage	–0.5(1)	—	0.8	V

NOTE: 2967 tbl 06
1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

CAPACITANCE ($T_A = +25°C$, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
CI/O	I/O Capacitance	VOUT = 0V	8	pF

NOTE: 2967 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

DC ELECTRICAL CHARACTERISTICS[1]

(VCC = 5.0V ± 10%, VLC = 0.2V, VHC = VCC - 0.2V)

			7164S15 7164L15		7164S20 7164L20		7164S25 7164L25		7164S30 7164L30		
Symbol	Parameter	Power	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Unit
ICC1	Operating Power Supply Current, $\overline{CS_1}$ = VIL, CS2 = VIH, Outputs Open, VCC = Max., f = 0[3]	S	110	—	100	110	90	110	90	100	mA
		L	100	—	90	100	80	100	80	90	
ICC2	Dynamic Operating Current $\overline{CS_1}$ = VIL, CS2 = VIH, Outputs Open, VCC = Max., f = fMAX[3]	S	180	—	170	180	170	180	160	170	mA
		L	150	—	150	160	150	160	140	150	
ISB	Standby Power Supply Current (TTL Level), $\overline{CS_1}$ ≥ VIH or CS2 ≤ VIL VCC = Max., Outputs Open, f = fMAX[3]	S	20	—	20	20	20	20	20	20	mA
		L	3	—	3	5	3	5	3	5	
ISB1	Full Standby Power Supply Current (CMOS Level), f = 0[3], VCC = Max. 1. $\overline{CS1}$ ≥ VHC and CS2 ≥ VHC, or 2. CS2 ≤ VLC	S	15	—	15	20	15	20	15	20	mA
		L	0.2	—	0.2	1	0.2	1	0.2	1	

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DC ELECTRICAL CHARACTERISTICS[1] (Continued)

(VCC = 5.0V ± 10%, VLC = 0.2V, VHC = VCC - 0.2V)

			7164S35 7164L35		7164S45 7164L45		7164S55 7164L55		7164S70/85[2] 7164L70/85[2]		
Symbol	Parameter	Power	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Unit
ICC1	Operating Power Supply Current, $\overline{CS_1}$ = VIL, CS2 = VIH, Outputs Open, VCC = Max., f = 0[3]	S	90	100	—	100	—	100	—	100	mA
		L	80	90	—	90	—	90	—	90	
ICC2	Dynamic Operating Current $\overline{CS_1}$ = VIL, CS2 = VIH, Outputs Open, VCC = Max., f = fMAX[3]	S	150	160	—	160	—	160	—	160	mA
		L	130	140	—	130	—	125	—	120	
ISB	Standby Power Supply Current (TTL Level), $\overline{CS_1}$ ≥ VIH, or CS2 ≤ VIL VCC = Max., Outputs Open, f = fMAX[3]	S	20	20	—	20	—	20	—	20	mA
		L	3	5	—	5	—	5	—	5	
ISB1	Full Standby Power Supply Current (CMOS Level), f = 0[3], VCC = Max. 1. $\overline{CS1}$ ≥ VHC and CS2 ≥ VHC, or 2. CS2 ≤ VLC	S	15	20	—	20	—	20	—	20	mA
		L	0.2	1	—	1	—	1	—	1	

NOTES: 2967 tbl 07

1. All values are maximum guaranteed values.
2. Also available: 100, 120, 150 and 200ns military devices.
3. fMAX = 1/tRC (all address inputs are cycling at fMAX); f = 0 means no address input lines are changing.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition		IDT7164S Min.	IDT7164S Max.	IDT7164L Min.	IDT7164L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}_1$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.			0.4	—	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		—	0.5	—	0.5	
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	—	2.4	—	V

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) (V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Test Condition		Min.	Typ.[1] Vcc @ 2.0v	Typ.[1] Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL. COM'L.	— —	10 10	15 15	200 60	300 90	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time	1. $\overline{CS}_1 \geq V_{HC}$ $CS_2 \geq V_{HC}$, or		0	—	—	—	—	ns
t_R[3]	Operation Recovery Time	2. $CS_2 \leq V_{LC}$		t_{RC}[2]	—	—	—	—	ns
$\|I_{LI}\|$[3]	Input Leakage Current			—	—	—	2	2	µA

NOTES: 2967 tbl 10

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2967 tbl 08

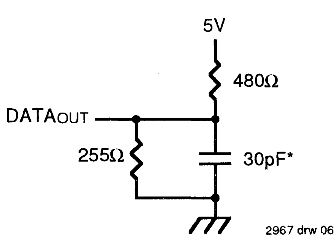

Figure 1. AC Test Load

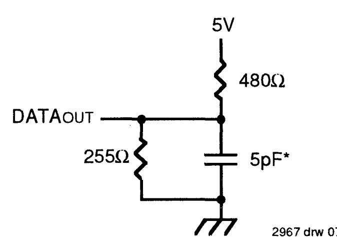

Figure 2. AC Test Load
(for t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2}, t_{OHZ}, t_{OW}, and t_{WHZ})

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

		7164S15(1) 7164L15(1)		7164S20 7164L20		7164S25 7164L25		7164S30 7164L30		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	15	—	20	—	25	—	30	—	ns
t_{AA}	Address Access Time	—	15	—	19	—	25	—	29	ns
t_{ACS1}(3)	Chip Select-1 Access Tim	—	15	—	20	—	25	—	30	ns
t_{ACS2}(3)	Chip Select-2 Access Time	—	20	—	25	—	30	—	35	ns
$t_{CLZ1,2}$(4)	Chip Select-1, 2 to Output in Low-Z	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	7	—	8	—	12	—	15	ns
t_{OLZ}(4)	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
$t_{CHZ1,2}$(4)	Chip Select-1, 2 to Output in High-Z	—	8	—	9	—	13	—	13	ns
t_{OHZ}(4)	Output Disable to Output in High-Z	—	7	—	8	—	10	—	12	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{PU}(4)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}(4)	Chip Deselect to Power Down Time	—	15	—	20	—	25	—	30	ns
Write Cycle										
t_{WC}	Write Cycle Time	15	—	20	—	25	—	30	—	ns
$t_{CW1,2}$	Chip Select to End-of-Write	14	—	15	—	18	—	22	—	ns
t_{AW}	Address Valid to End-of-Write	14	—	15	—	18	—	22	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	14	—	15	—	21	—	23	—	ns
t_{WR1}	Write Recovery Time ($\overline{CS}_1$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{WR2}	Write Recovery Time (CS_2)	5	—	5	—	5	—	5	—	ns
t_{WHZ}(4)	Write Enable to Output in High-Z	—	6	—	8	—	10	—	12	ns
t_{DW}	Data to Write Time Overlap	8	—	10	—	13	—	13	—	ns
t_{DH1}	Data Hold from Write Time ($\overline{CS}_1$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{DH2}	Data Hold from Write Time (CS_2)	5	—	5	—	5	—	5	—	ns
t_{OW}(4)	Output Active from End-of-Write	4	—	4	—	4	—	4	—	ns

2967 tbl 11

NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only. Also available: 100, 120, 150 and 200ns military devices.
3. Both chip selects must be active for the device to be selected.
4. This parameter is guaranteed by device characterization, but is not production tested.

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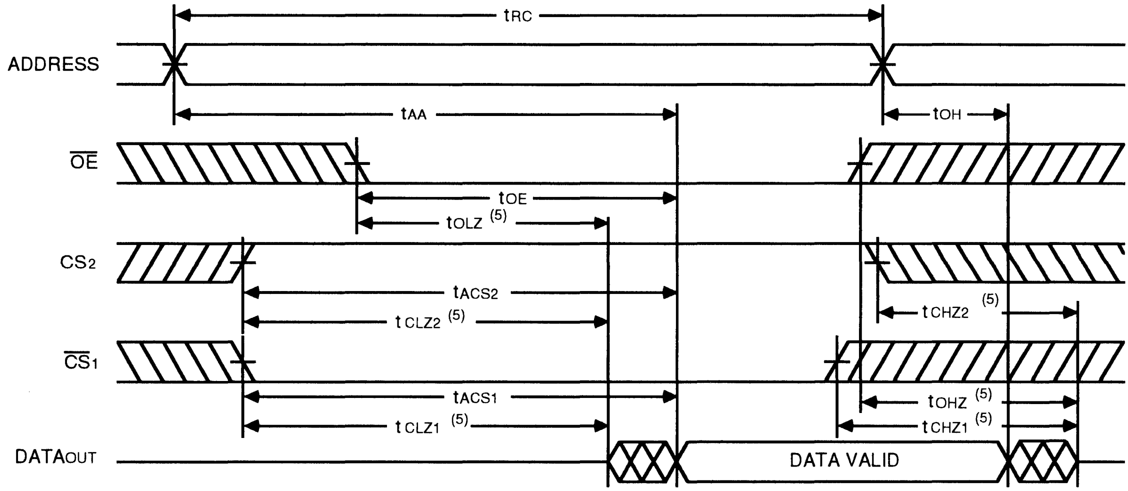
AC ELECTRICAL CHARACTERISTICS (Continued) (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7164S35 7164L35		7164S45(2) 7164L45(2)		7164S55(2) 7164L55(2)		7164S70(2)/85(2) 7164L70(2)/85(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	35	—	45	—	55	—	70/85	—	ns
t_{AA}	Address Access Time	—	35	—	45	—	55	—	70/85	ns
t_{ACS1}(3)	Chip Select-1 Access Time	—	35	—	45	—	55	—	70/85	ns
t_{ACS2}(3)	Chip Select-2 Access Time	—	40	—	45	—	55	—	70/85	ns
$t_{CLZ1,2}$(4)	Chip Select-1, 2 to Output in Low-Z	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	18	—	25	—	30	—	35/40	ns
t_{OLZ}(4)	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
$t_{CHZ1,2}$(4)	Chip Select-1, 2 to Output in High-Z	—	15	—	20	—	25	—	30/35	ns
t_{OHZ}(4)	Output Disable to Output in High-Z	—	15	—	20	—	25	—	30/35	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{PU}(4)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}(4)	Chip Deselect to Power Down Time	—	35	—	45	—	55	—	70/85	ns
Write Cycle										
t_{WC}	Write Cycle Time	35	—	45	—	55	—	70/85	—	ns
$t_{CW1,2}$	Chip Select to End-of-Write	25	—	33	—	50	—	60/75	—	ns
t_{AW}	Address Valid to End-of-Write	25	—	33	—	50	—	60/75	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	25	—	50	—	60/75	—	ns
t_{WR1}	Write Recovery Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{WR2}	Write Recovery Time (CS_2)	5	—	5	—	5	—	5	—	ns
t_{WHZ}(4)	Write Enable to Output in High-Z	—	14	—	18	—	25	—	30/35	ns
t_{DW}	Data to Write Time Overlap	15	—	20	—	25	—	30/35	—	ns
t_{DH1}	Data Hold from Write Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{DH2}	Data Hold from Write Time (CS_2)	5	—	5	—	5	—	5	—	ns
t_{OW}(4)	Output Active from End-of-Write	4	—	4	—	4	—	4	—	ns

2967 tbl 11

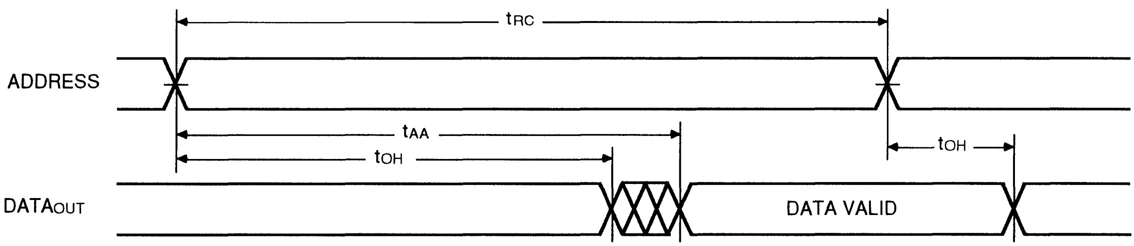
NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only. Also available: 100, 120, 150, and 200ns military devices.
3. Both chip selects must be active for the device to be selected.
4. This parameter is guaranteed by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



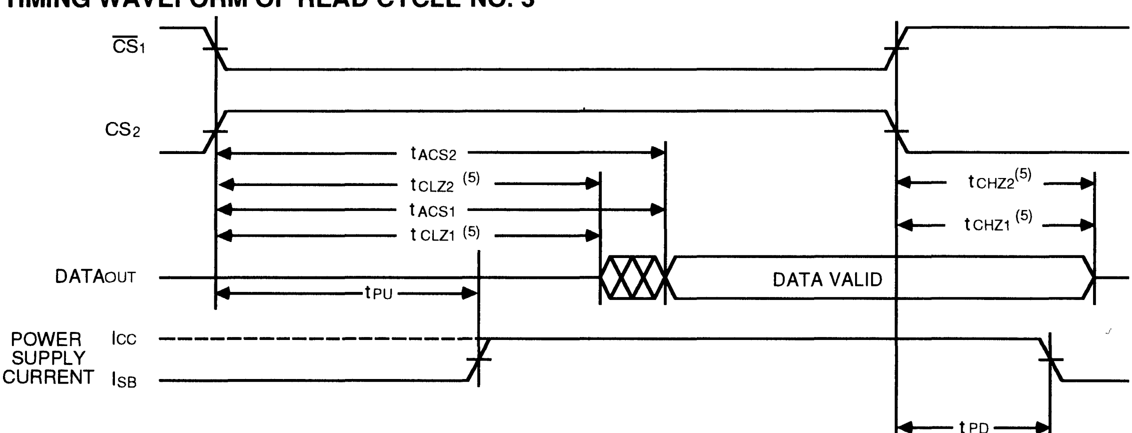
2967 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2967 drw 09

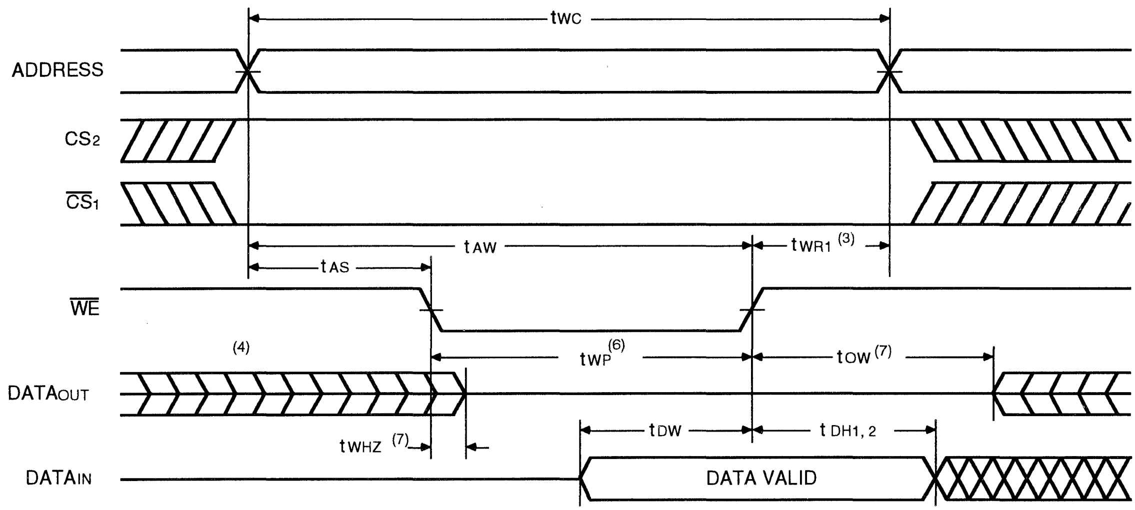
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



2967 drw 10

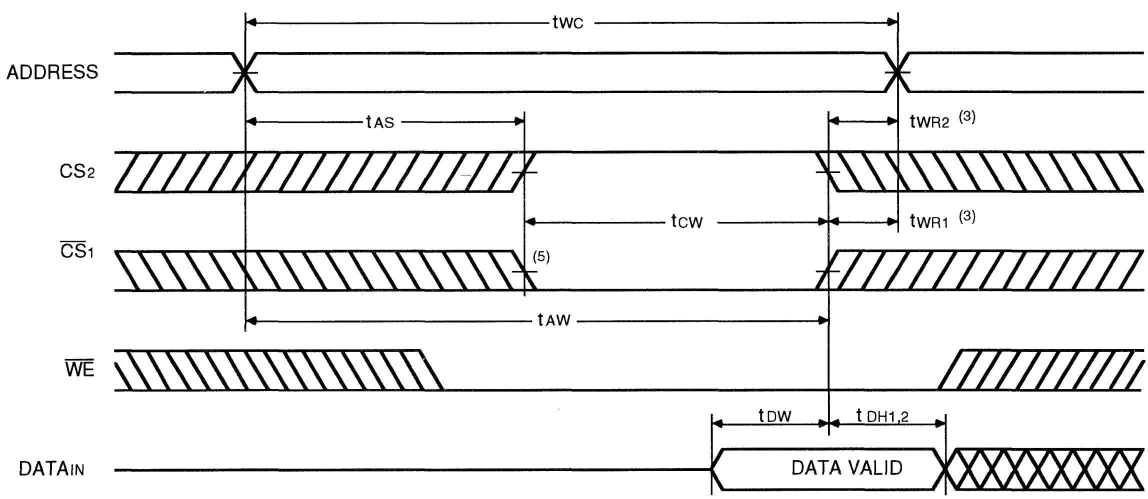
NOTES:
1. WE is HIGH for Read cycle.
2. Device is continuously selected, CS1 is LOW, CS2 is HIGH.
3. Address valid prior to or coincident with CS1 transition LOW and CS2 transition HIGH.
4. OE is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 6)



2967 drw 11

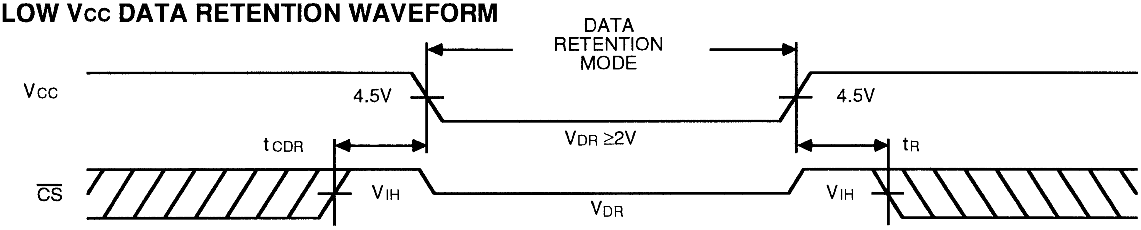
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2)



2967 drw 12

NOTES:
1. $\overline{WE}$, $\overline{CS_1}$ or CS_2 must be inactive during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{WE}$, a LOW $\overline{CS_1}$ and a HIGH CS_2.
3. $t_{WR1,2}$ is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going HIGH or CS_2 going LOW to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS_1}$ LOW transition or CS_2 HIGH transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} +t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse width is as short as the specified t_{WP}.
7. Transition is measured ±200mV from steady state.

LOW Vcc DATA RETENTION WAVEFORM



2967 drw 05

ORDERING INFORMATION

IDT 7164 X XX XXX X

Field	Code	Description
7164	Device Type	
X	Power	
XX	Speed	
XXX	Package	
X	Process/ Temperature Range	

Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package

Y	300 mil SOJ (SO28-5)
PE	330 mil SOIC (SO28-3)
TD	300 mil CERDIP (D28-3)
D	600 mil CERDIP (D28-1)
P	600 mil Plastic DIP (P28-1)
TP	300 mil Plastic DIP (P28-2)
L32	32 Leadless Chip Carrier (L32-1)
XE	CERPACK F11 (E28-2)

Speed (Speed in nanoseconds)

15	Commercial Only
20	
25	
30	
35	Military Only
45	Military Only
55	Military Only
70	Military Only
85	Military Only

Power

S	Standard Power
L	Low Power

2967 drw 13

256K SRAM PRODUCTS

The flagship 256K family of IDT SRAMs offers some of the fastest speeds in the industry in 8-bit wide and 4-bit wide configurations. IDT's world-class CMOS technology provides high-performance (as fast as 12ns) at a minimal cost in a wide array of packaging options.

The 20ns 71256 offers the best standby power consumption in the industry in its "L" version, which makes it ideally suited for battery-operated equipment like notebook computers and portable instruments.

The CMOS x8 parts are especially suitable for cache memory applications in the PC market, both as the asynchronous tag SRAM or data SRAM. The x4 parts are well suited for many workstation cache applications as well, such as R4000 cache implementations.

High-performance communications applications can also benefit from the fast speeds and surface-mount packaging options offered in this family.

Size	Organization	Process	Part Number	Power	Speeds Commercial	Speeds Military
256K	64K x 4	CMOS	61298	SA	12,15,17,20	20,25
	32K x 8	CMOS	71256	S/L	20,25,35,45	25,30,35,45,55,70, 85,100,120,150
	32K x 8	CMOS	71256	SA	12,15,20,25	15,20,25

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TABLE OF CONTENTS

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Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (64K x 4-BIT)

IDT61298SA

FEATURES:

- 64K x 4 high-speed static RAM
- Fast Output Enable ($\overline{OE}$) pin available for added system flexibility
- High speed (equal access and cycle times)
  - — Military: 20/25ns (max.)
  - — Commercial: 12/15/17/20ns (max.)
- JEDEC standard pinout
- 300 mil 28-pin DIP, 300 mil 28-pin SOJ, and 300 mil 28-pin LCC
- Produced with advanced CMOS technology
- Bidirectional data inputs and outputs
- Inputs/Outputs TTL-compatible
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

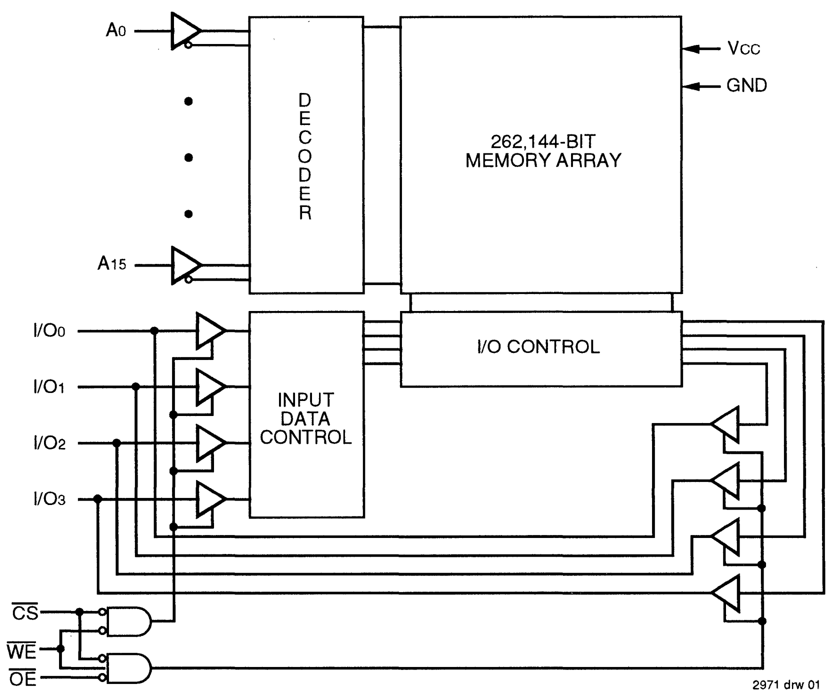
The IDT61298SA is a 262,144-bit high-speed static RAM organized as 64K x 4. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective approach for memory intensive applications.

The IDT61298SA features two memory control functions: Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$). These two functions greatly enhance the IDT61298SA's overall flexibility in high-speed memory applications.

Access times as fast as 12ns are available. The IDT61298SA offers a reduced power standby mode, I_{SB1}, which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability.

All inputs and outputs are TTL-compatible and the device operates from a single 5 volt supply. Fully static asynchronous

FUNCTIONAL BLOCK DIAGRAM



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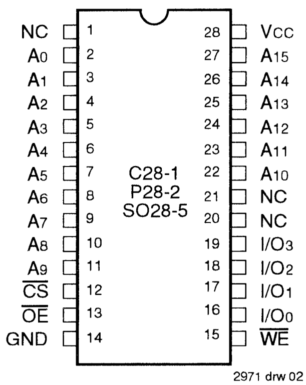
DESCRIPTION (Continued)

circuitry, along with matching access and cycle times, favor the simplified system design approach.

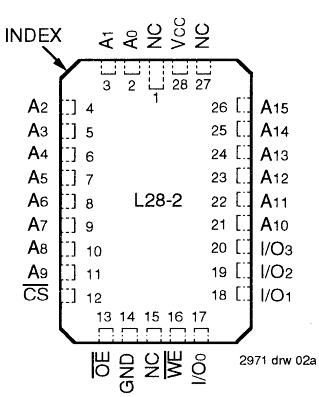
The IDT61298SA is packaged in a 28-pin Sidebraze or Plastic 300 mil DIP, an SOJ, plus an LCC, providing improved board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP/SOJ
TOP VIEW



LCC
TOP VIEW

TRUTH TABLE(1,2)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	$DATA_{OUT}$	Read Data
L	X	L	$DATA_{IN}$	Write Data
L	H	H	High-Z	Outputs Disabled
H	X	X	High-Z	Deselected - Standby (I_{SB})
V_{HC}(3)	X	X	High-Z	Deselected - Standby (I_{SB1})

NOTES: 2971 tbl 01

1. H = V_{IH}, L = V_{IL}, x = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V.
3. Other inputs $\geq V_{HC}$ or $\leq V_{LC}$.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTES: 2971 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

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CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ Package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

NOTE: 2971 tbl 03

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2971 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC} + 0.5V	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2971 tbl 05
1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

		61298SA12		61298SA15		61298SA17		61298SA20		61298SA25		
Symbol	Parameter	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Unit
I_{CC}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = f_{MAX}(2)	160	—	140	—	135	—	130	140	—	120	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	50	—	45	—	40	—	40	45	—	40	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., f = 0(2), V_{LC} ≥ V_{IN} ≥ V_{HC}	20	—	20	—	20	—	20	30	—	30	mA

NOTES: 2971 tbl 06
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2971 tbl 07

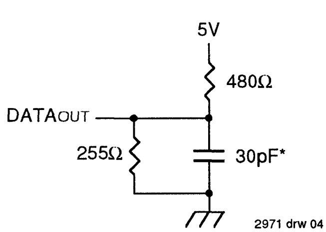


Figure 1. AC Test Load

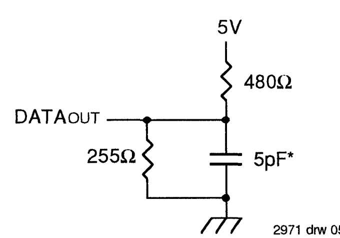


Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Condition	IDT61298SA Min.	Typ.	Max.	Unit
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	—	5	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{CC} = Max., $\overline{CS} = V_{IH}$, V_{OUT} = GND to V_{CC}	—	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min. I_{OL} = 10mA, V_{CC} = Min.	— —	— —	0.4 0.5	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	—	V

2971 tbl 09

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V \pm 10\%$, All Temperature Ranges)

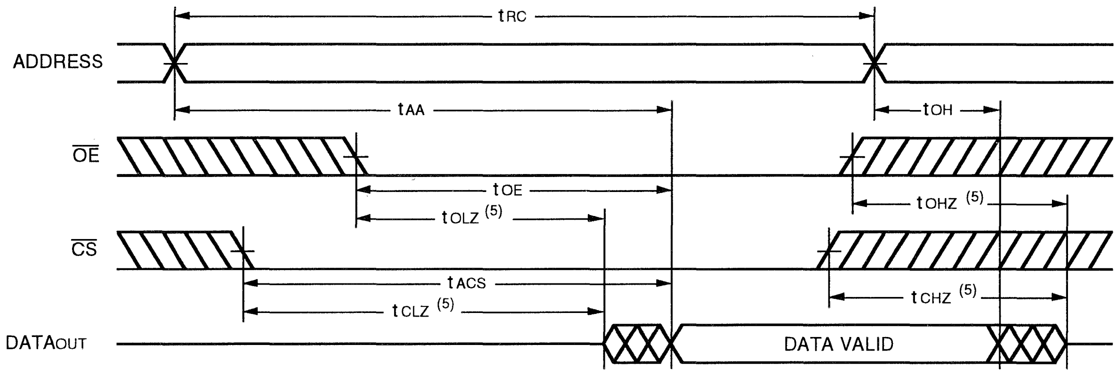
Symbol	Parameter	61298SA12(1) Min.	Max.	61298SA15(1) Min.	Max.	61298SA17(1) Min.	Max.	61298SA20 Min.	Max.	61298SA25(2) Min.	Max.	Unit
Read Cycle												
t_{RC}	Read Cycle Time	12	—	15	—	17	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	17	—	20	—	25	ns
t_{ACS}	Chip Select Access Time	—	12	—	15	—	17	—	20	—	25	ns
t_{CLZ}(3)	Chip Select to Output in Low-Z	4	—	4	—	4	—	4	—	4	—	ns
t_{CHZ}(3)	Chip Deselect to Output in High-Z	—	6	—	7	—	8	—	8	—	9	ns
t_{OE}	Output Enable to Output Valid	—	6	—	7	—	8	—	8	—	9	ns
t_{OLZ}(3)	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	0	—	ns
t_{OHZ}(3)	Output Disable to Output in High-Z	—	6	—	6	—	7	—	8	—	9	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns
t_{PU}(3)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}(3)	Chip Deselect to Power-Down Time	—	12	—	15	—	17	—	20	—	25	ns
Write Cycle												
t_{WC}	Write Cycle Time	12	—	15	—	17	—	20	—	25	—	ns
t_{CW}	Chip Select to End-of-Write	9	—	10	—	11	—	12	—	15	—	ns
t_{AW}	Address Valid to End-of-Write	9	—	10	—	11	—	12	—	15	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	9	—	10	—	11	—	12	—	15	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	6	—	7	—	8	—	8	—	10	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}(3)	Write Enable to Output in High-Z	—	6	—	6	—	7	—	8	—	9	ns
t_{OW}(3)	Output Active from End-of-Write	4	—	4	—	4	—	4	—	4	—	ns

2971 tbl 10

NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter is guaranteed with AC test load (Figure 2) by device characterization, but is not production tested.

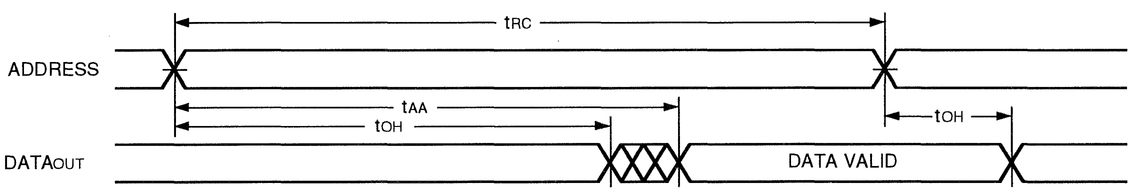
7

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



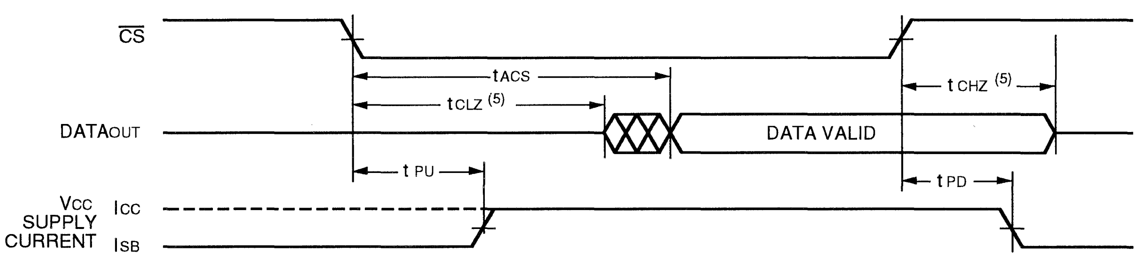
2971 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



2971 drw 07

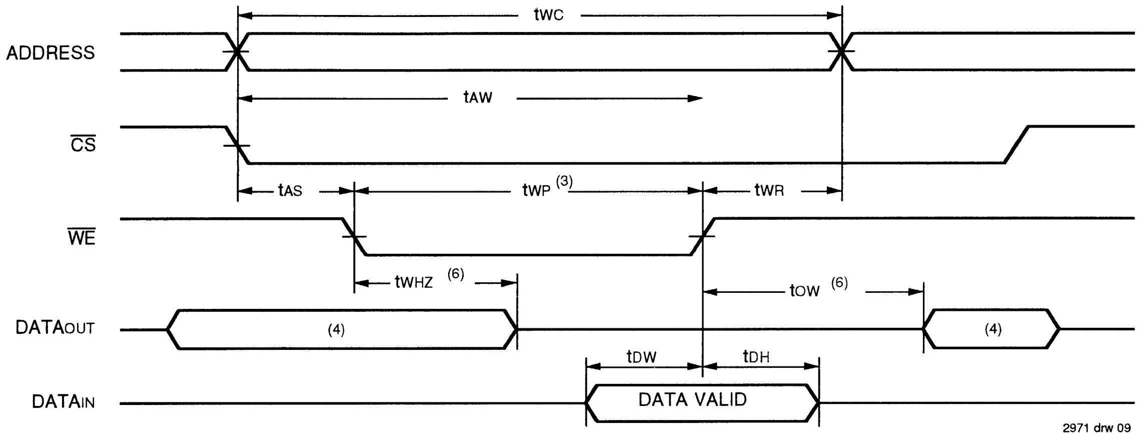
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



2971 drw 08

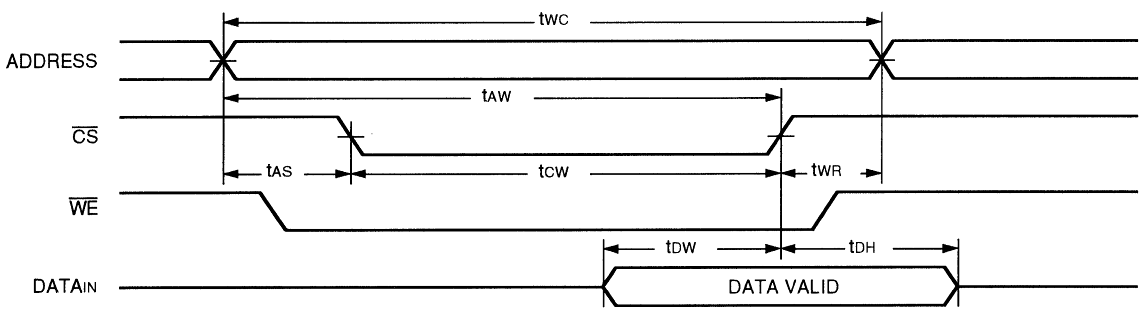
NOTES:
1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,5)



2971 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,5)



2971 drw 10

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP}.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.

7

ORDERING INFORMATION

IDT	61298	SA	XX	XX	X
	Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package

TC	300-mil Sidebraze DIP (C28-1)
TP	300-mil Plastic DIP (P28-2)
Y	300-mil SOJ (SO28-5)
L	28-pin Leadless Chip Carrier (L28-2)

Speed (Speed in nanoseconds)

12	Commercial Only
15	Commercial Only
17	Commercial Only
20	
25	Military Only

2971 drw 11

CMOS STATIC RAM 256K (32K x 8-BIT)

IDT71256S
IDT71256L

FEATURES:

- High-speed address/chip select time
  - — Military: 25/30/35/45/55/70/85/100/120/150ns (max.)
  - — Commercial: 20/25/35/45ns (max.)
- Low-power operation
- Battery Backup operation — 2V data retention
- Produced with advanced high-performance CMOS technology
- Input and output directly TTL-compatible
- Available in standard 28-pin (600 mil) CERDIP, 28-pin (300 or 600 mil) plastic DIP, 28-pin (300 mil) ceramic sidebraze DIP, 28-pin and (300 mil) SOJ, 28-pin CERPACK, 32-pin LCC, 28-pin LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

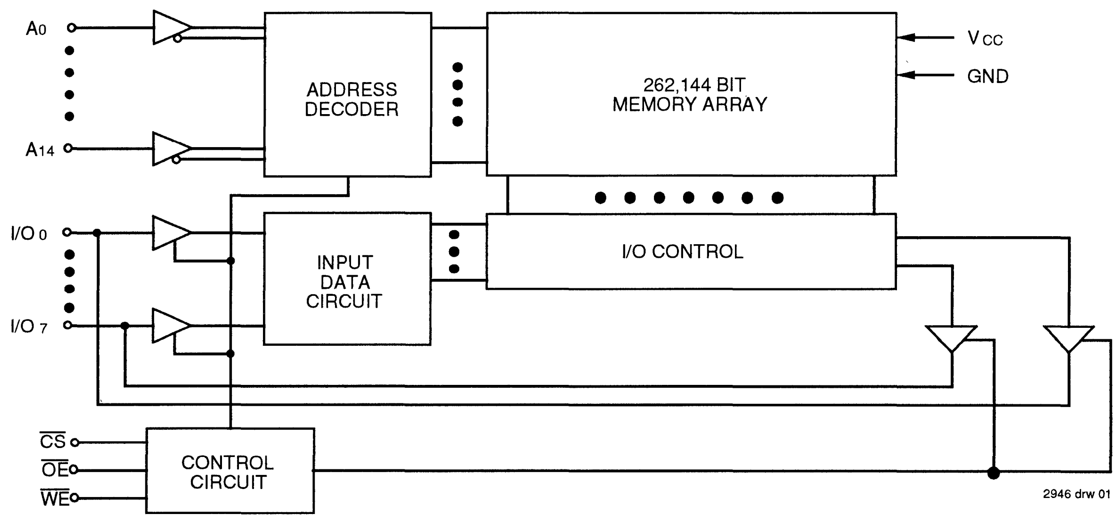
The IDT71256 is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

Address access times as fast as 20ns are available with power consumption of only 350mW (typ.). The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, a low-power standby mode as long as $\overline{CS}$ remains HIGH. In the full standby mode, the low-power device consumes less than 15µW, typically. This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 5µW when operating off a 2V battery.

The IDT71256 is packaged in a 28-pin 300 mil J-bend SOIC, a 28-pin 600 mil CERDIP, 28-pin (300 or 600 mil) plastic DIP, 28-pin (300 mil) ceramic sidebraze DIP, 28-pin CERPACK, 32-pin LCC, 28-pin LCC, providing high board-level packing densities.

The IDT71256 military RAM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



The IDT logo is a registered trademark of Integrated Device Technology, Inc.

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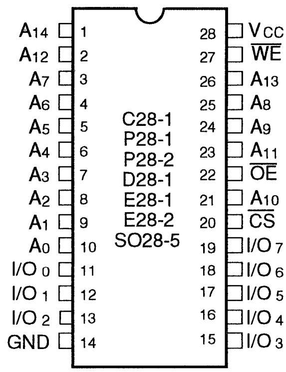
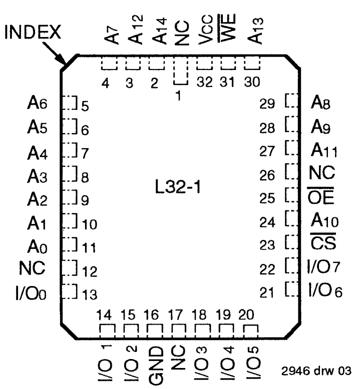
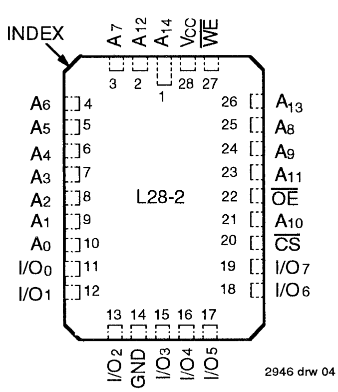
PIN CONFIGURATIONS



DIP/SOJ/SOIC
TOP VIEW



32-Pin LCC
TOP VIEW



28-Pin LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0–A14	Addresses
I/O0–I/O7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
VCC	Power

2946 tbl 01

TRUTH TABLE(1)

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
X	H	X	High-Z	Standby (ISB)
X	VHC	X	High-Z	Standby (ISB1)
H	L	H	High-Z	Output Disabled
H	L	L	DOUT	Read Data
L	L	X	DIN	Write Data

NOTE:
2946 tbl 02
1. H = VIH, L = VIL, X = Don't Care

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE:
2946 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
CI/O	I/O Capacitance	VOUT = 0V	11	pF

NOTE:
2946 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2946 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2946 tbl 06
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS(1, 2)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71256S/L20 Com'l.	71256S/L20 Mil.	71256S/L25 Com'l.	71256S/L25 Mil.	71256S/L30 Com'l.	71256S/L30 Mil.	71256S/L35 Com'l.	71256S/L35 Mil.	Unit
I_{CC}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open V_{CC} = Max., f = f_{MAX}(2)	S	155	—	145	150	—	145	135	140	mA
		L	135	—	115	130	—	125	105	120	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	S	20	—	20	20	—	20	20	20	mA
		L	3	—	3	3	—	3	3	3	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., f = 0	S	15	—	15	20	—	20	15	20	mA
		L	0.4	—	0.4	1.5	—	1.5	0.4	1.5	

Symbol	Parameter	Power	71256S/L45 Com'l.	71256S/L45 Mil.	71256S/L55 Com'l.	71256S/L55 Mil.	71256S/L70 Com'l.	71256S/L70 Mil.	71256S/L85(3) Com'l.	71256S/L85(3) Mil.	71256S/L100(3) Com'l.	71256S/L100(3) Mil.	Unit
I_{CC}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open V_{CC} = Max., f = f_{MAX}(2)	S	130	135	—	135	—	135	—	135	—	135	mA
		L	100	115	—	115	—	115	—	115	—	115	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	S	20	20	—	20	—	20	—	20	—	20	mA
		L	3	3	—	3	—	3	—	3	—	3	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., f = 0	S	15	20	—	20	—	20	—	20	—	20	mA
		L	0.4	1.5	—	1.5	—	1.5	—	1.5	—	1.5	

NOTES: 2946 tbl 07
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC}, all address inputs cycling at f_{MAX}; f = 0 means no address pins are cycling.
3. Also available: 120 and 150 ns military devices.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2946 tbl 08

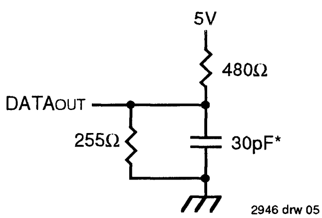


Figure 1. AC Test Load

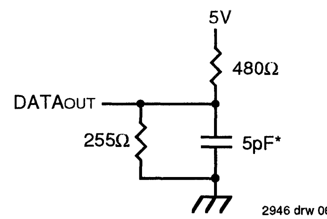


Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT71256S			IDT71256L			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	— —	10 5	— —	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	— —	10 5	— —	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.			—	0.4	—	—	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		—	—	0.5	—	—	0.5	
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

2946 tbl 09

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

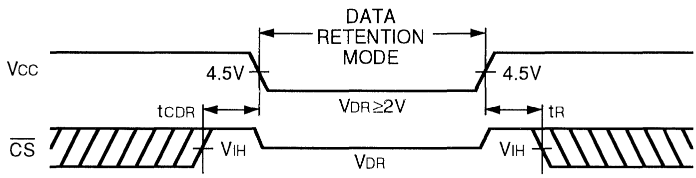
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.(1) Vcc @		Max. Vcc @		Unit
					2.0v	3.0V	2.0V	3.0V	
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL. COM'L.	— —	— —	— —	500 120	800 200	µA
t_{CDR}	Chip Deselect to Data Retention Time	$\overline{CS} \geq V_{HC}$		0	—	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns

2946 tbl 10

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71256S20[1] 71256L20[1] Min.	Max.	71256S25 71256L25 Min.	Max.	71256S30[3] 71256L30[3] Min.	Max.	71256S35 71256L35 Min.	Max.	71256S45 71256L45 Min.	Max.	Unit
Read Cycle												
t_{RC}	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	30	—	35	—	45	ns
t_{CLZ}[2]	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}[2]	Chip Deselect to Output in High-Z	—	10	—	11	—	15	—	15	—	20	ns
t_{OE}	Output Enable to Output Valid	—	10	—	11	—	13	—	15	—	20	ns
t_{OLZ}[2]	Output Enable to Output in Low-Z	2	—	2	—	2	—	2	—	0	—	ns
t_{OHZ}[2]	Output Disable to Output in High-Z	2	8	2	10	2	12	2	15	—	20	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
Write Cycle												
t_{WC}	Write Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
t_{CW}	Chip Select to End-of-Write	15	—	20	—	25	—	30	—	40	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	20	—	25	—	30	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data to Write Time Overlap	11	—	13	—	14	—	15	—	20	—	ns
t_{WHZ}[2]	Write Enable to Output in High-Z	—	10	—	11	—	15	—	15	—	20	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OW}[2]	Output Active from End-of-Write	5	—	5	—	5	—	5	—	5	—	ns

2946 tbl 11

NOTES:
1. 0° to +70°C temperature range only.
2. This parameter guaranteed by device characterization, but is not production tested.
3. –55° to +125°C temperature range only.

7

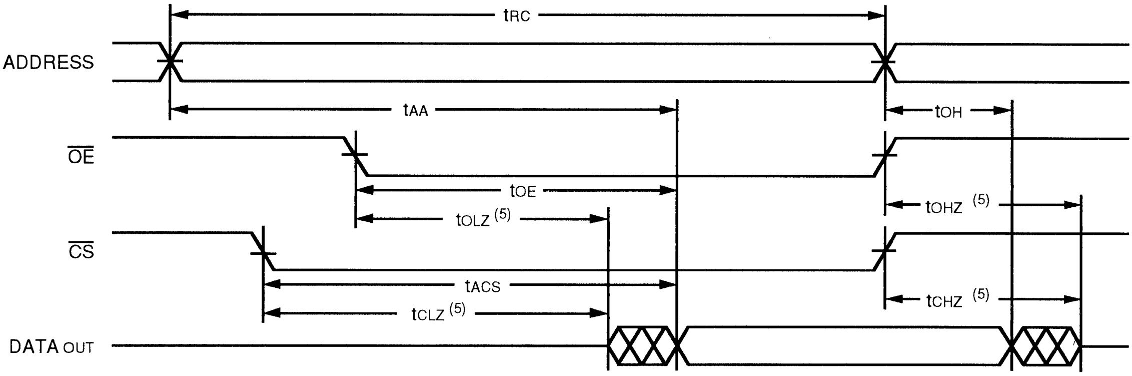
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71256S55(1) 71256L55(1)		71256S70(1) 71256L70(1)		71256S85(1) 71256L85(1)		71256S100(1,3) 71256L100(1,3)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	55	—	70	—	85	—	100	—	ns
tAA	Address Access Time	—	55	—	70	—	85	—	100	ns
tACS	Chip Select Access Time	—	55	—	70	—	85	—	100	ns
tCLZ(2)	Chip Deselect to Output in Low-Z	5	—	5	—	5	—	5	—	ns
tCHZ(2)	Output Enable to Output in Low-Z	—	25	—	30	—	35	—	40	ns
tOE	Output Enable to Output Valid	—	25	—	30	—	35	—	40	ns
tOLZ(2)	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
tOHZ(2)	Output Disable to Output in High-Z	0	25	0	30	—	35	—	40	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
Write Cycle										
tWC	Write Cycle Time	55	—	70	—	85	—	100	—	ns
tCW	Chip Select to End-of-Write	50	—	60	—	70	—	80	—	ns
tAW	Address Valid to End-of-Write	50	—	60	—	70	—	80	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	40	—	45	—	50	—	55	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	Data to Write Time Overlap	25	—	30	—	35	—	40	—	ns
tDH	Data Hold from Write Time ($\overline{WE}$)	0	—	0	—	0	—	0	—	ns
tWHZ(2)	Write Enable to Output in High-Z	—	25	—	30	—	35	—	40	ns
tOW(2)	Output Active from End-of-Write	5	—	5	—	5	—	5	—	ns

2946 tbl 11

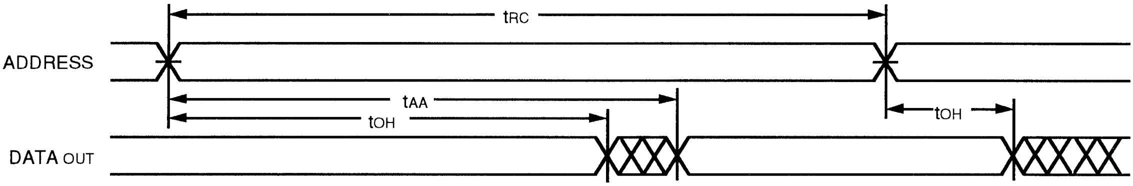
NOTES:
1. –55°C to +125°C temperature range only.
2. This parameter guaranteed by device characterization, but is not production tested.
3. Also available: 120 and 150 ns military devices.

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



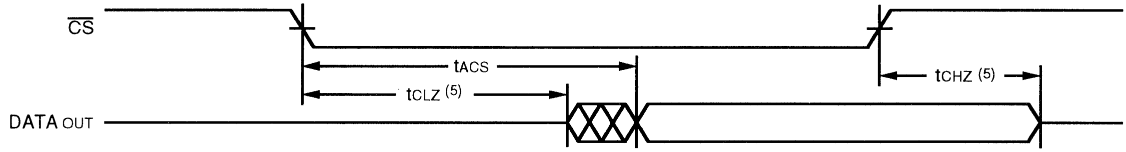
2946 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]



2946 drw 09

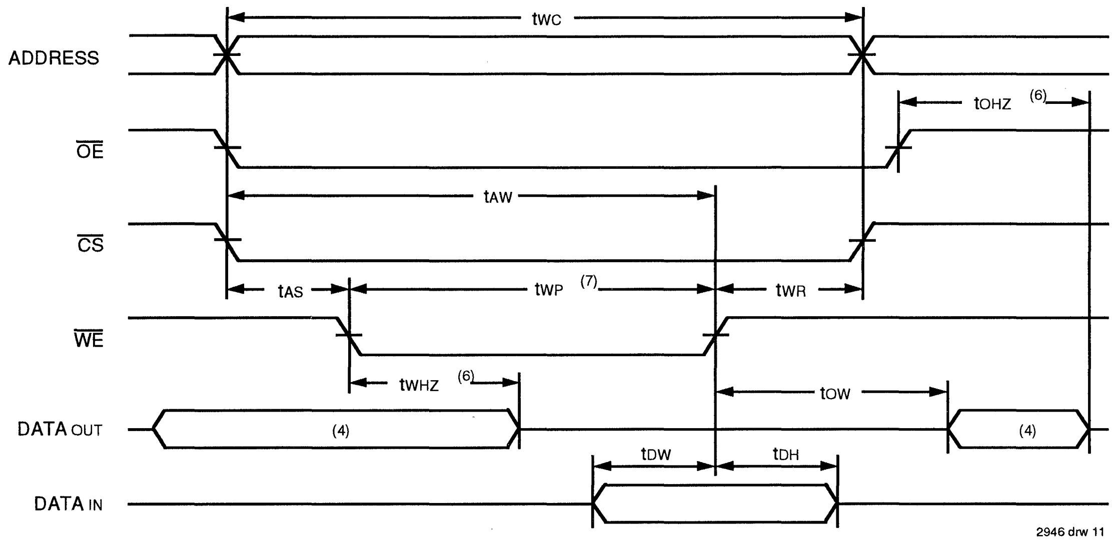
TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3, 4]



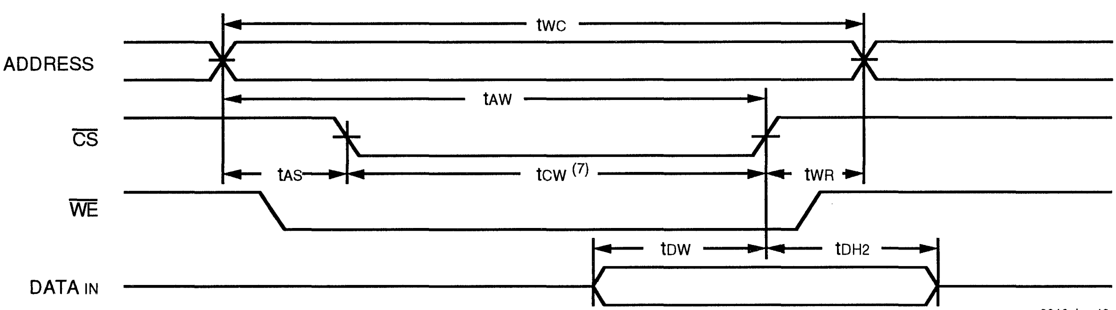
2946 drw 10

NOTES:
1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{\text{WE}}$ CONTROLLED TIMING)(1, 2, 3, 5, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{\text{CS}}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{\text{WE}}$ or $\overline{\text{CS}}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{\text{CS}}$ and a LOW $\overline{\text{WE}}$.
3. t_{WR} is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{\text{CS}}$ LOW transition occurs simultaneously with or after the $\overline{\text{WE}}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{\text{OE}}$ is LOW during a $\overline{\text{WE}}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{\text{OE}}$ is HIGH during a $\overline{\text{WE}}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the spectified t_{WP}. For a $\overline{\text{CS}}$ controlled write cycle, $\overline{\text{OE}}$ may be LOW with no degradation to t_{CW}.

ORDERING INFORMATION

IDT 71256 X XXX XXX X

71256	X	XXX	XXX	X
Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package

TC	300 mil SIDEBRAZE DIP (C28-1)
TP	300 mil Plastic DIP (P28-2)
Y	300 mil SOJ (SO28-5)
P	600 mil Plastic DIP (P28-1)
D	600 mil CERDIP (D28-1)
L28	Leadless Chip Carrier (28-pin) (L28-2)
L32	Leadless Chip Carrier (32-pin) (L32-1)
XE	Cerpack F11 (E28-2)
E	Cerpack F11A (E28-1)

Speed (Speed in nanoseconds)

20	Commercial Only
25	
30	Military Only
35	
45	
55	Military Only
70	Military Only
85	Military Only
100	Military Only
120	Military Only
150	Military Only

Power

S	Standard Power
L	Low Power

2946 drw 13

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IDT logo

Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (32K x 8-BIT)

IDT71256SA

FEATURES:

- 32K x 8 advanced high-speed CMOS static RAM
- Equal access and cycle times
  - — Military: 15/20/25ns
  - — Commercial: 12/15/20/25ns
- One Chip Select plus one Output Enable pin
- Bidirectional data inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Military product compliant to MIL-STD-883, Class B
- Available in 28-pin Sidebraze DIP, Plastic DIP, Plastic SOJ, and 32-pin LCC packages

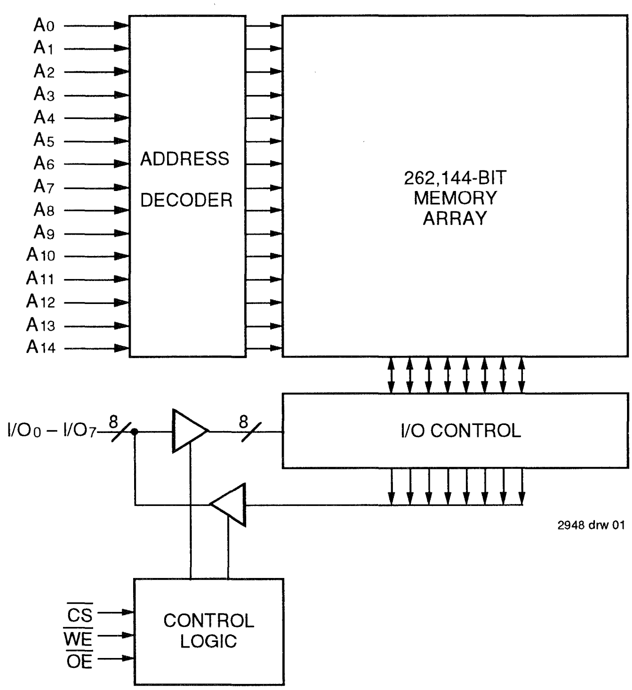
DESCRIPTION:

The ID71256SA is a 262,144-bit high-speed Static RAM organized as 32K x 8. It is fabricated using IDT's high-perfomance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71256SA has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns. All bidirectional inputs and outputs of the IDT71256SA are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71256SA is packaged in 28-pin 300 mil Sidebraze DIP, 28-pin 300 mil Plastic DIP, 28-pin 300 mil Plastic SOJ, and 32-pin Leadless Chip Carrier packages.

FUNCTIONAL BLOCK DIAGRAM



2948 drw 01

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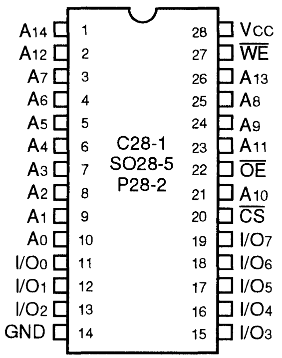
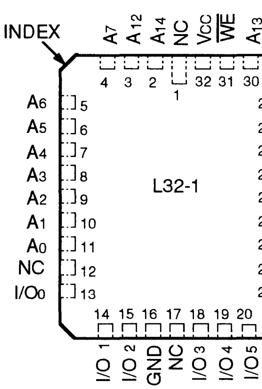
PIN CONFIGURATIONS



DIP/SOJ 2948 drw 02
TOP VIEW



2948 drw 03

LCC
TOP VIEW

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC}+0.5	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2948 tbl 04
1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTES: 2948 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	11	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	11	pF

NOTE: 2948 tbl 03
1. This parameter is guaranteed by device characterization, but not production tested.

TRUTH TABLE[1,2]

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	$DATA_{OUT}$	Read Data
L	X	L	$DATA_{IN}$	Write Data
L	H	H	High-Z	Outputs Disabled
H	X	X	High-Z	Deselected — Standby (I_{SB})
V_{HC}[3]	X	X	High-Z	Deselected — Standby (I_{SB1})

NOTES: 2948 tbl 01
1. H = V_{IH}, L = V_{IL}, x = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} –0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71256SA Min.	IDT71256SA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2948 tbl 05

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC}–0.2V)

Symbol	Parameter	71256SA12		71256SA15		71256SA20		71256SA25		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	160	—	150	170	145	150	145	150	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	50	—	40	50	40	45	40	45	mA
I_{SB1}	Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, Outputs Open, V_{CC} = Max., f = 0[2] $V_{IN} \le V_{LC}$ or $V_{IN} \ge V_{HC}$	15	—	15	30	15	30	15	30	mA

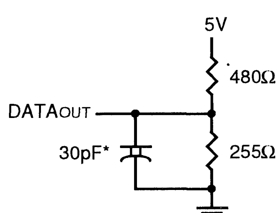
2948 tbl 06

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing .

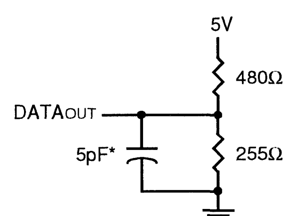
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2948 tbl 07



2948 drw 04



2948 drw 05

*Including jig and scope capacitance.

Figure 1. AC Test Load

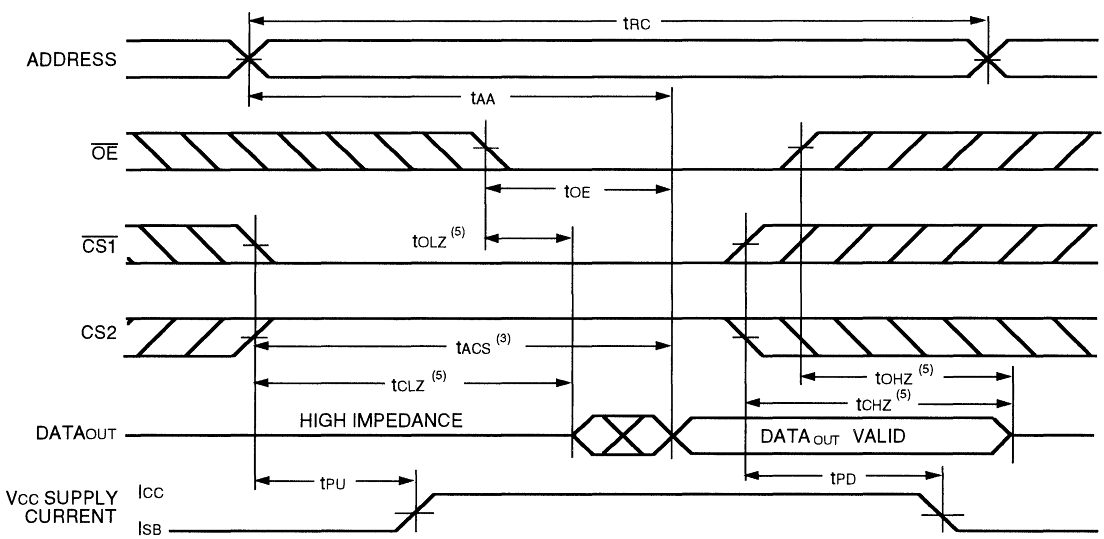
Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71256SA12(1) Min.	71256SA12(1) Max.	71256SA15 Min.	71256SA15 Max.	71256SA20 Min.	71256SA20 Max.	71256SA25 Min.	71256SA25 Max.	
Read Cycle										
t_{RC}	Read Cycle Time	12	—	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	—	25	ns
t_{ACS}	Chip Select Access Time	—	12	—	15	—	20	—	25	ns
t_{CLZ}(2)	Chip Select to Output in Low-Z	4	—	4	—	4	—	4	—	ns
t_{CHZ}(2)	Chip Deselect to Output in High-Z	0	6	0	7	0	10	0	11	ns
t_{OE}	Output Enable to Output Valid	—	6	—	7	—	10	—	11	ns
t_{OLZ}(2)	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t_{OHZ}(2)	Output Disable to Output in High-Z	0	6	0	6	0	8	0	10	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{PU}(2)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}(2)	Chip Deselect to Power Down Time	—	12	—	15	—	20	—	25	ns
Write Cycle										
t_{WC}	Write Cycle Time	12	—	15	—	20	—	25	—	ns
t_{AW}	Address Valid to End of Write	9	—	10	—	15	—	20	—	ns
t_{CW}	Chip Select to End of Write	9	—	10	—	15	—	20	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	9	—	10	—	15	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	6	—	7	—	11	—	13	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{OW}(2)	Output Active from End of Write	4	—	4	—	4	—	4	—	ns
t_{WHZ}(2)	Write Enable to Output in High-Z	0	6	0	6	0	10	0	11	ns

NOTES:
2948 tbl 08
1. 0° to +70°C temperature range only.
2. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

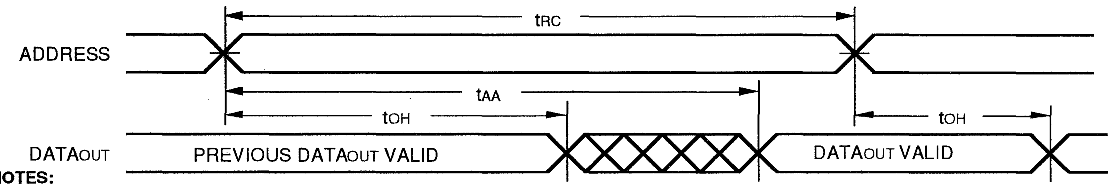
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



2948 drw 06

7

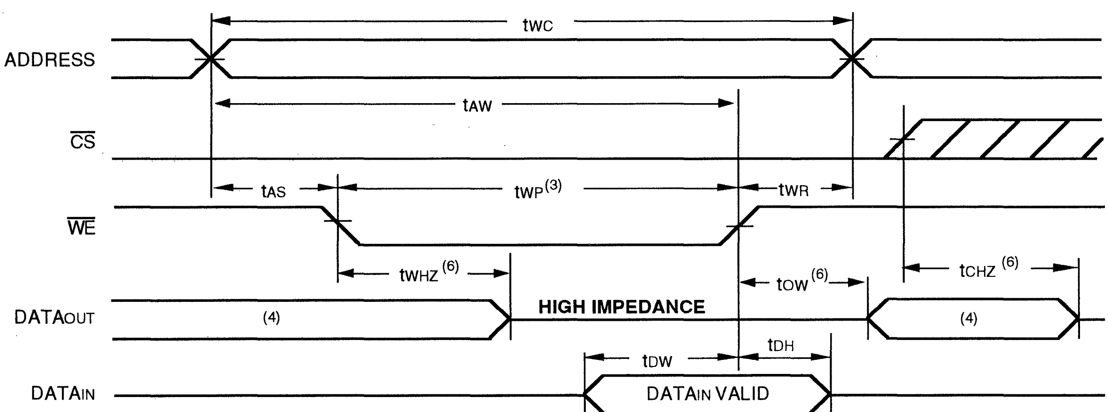
TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



2948 drw 07

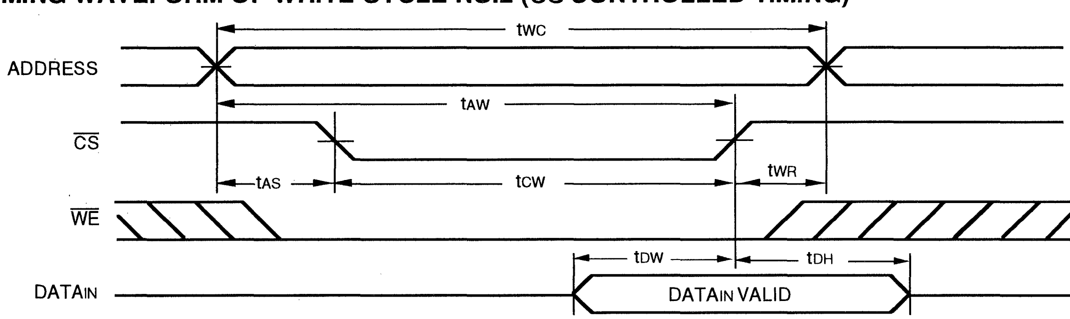
NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,5)



2948 drw 08

TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,5)



2948 drw 09

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP}.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.

ORDERING INFORMATION

IDT 71256 SA XX XXX X

71256	SA	XX	XXX	X
Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range:

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:

TC	300-mil Sidebraze DIP (C28-1)
TP	300-mil Plastic DIP (P28-2)
Y	300-mil SOJ (SO28-5)
L32	32-pin Leadless Chip Carrier (L32-1)

Speed:

$$\left.\begin{array}{ll} 12 & \text{Commercial Only} \\ 15 & \\ 20 & \\ 25 & \end{array}\right\}\ \text{Speed in nanoseconds}$$

2948 drw 10

7

1M SRAM PRODUCTS

The IDT 1M SRAM family consists of very fast, corner Power/Ground CMOS devices. IDT's state-of-the-art CMOS technology provides high-performance, affordable 1M SRAMs in multiple packaging options, including a high-density 300mil surface mount SOJ package for optimum space utilization.

Speeds as fast as 12ns are available in the CMOS commercial versions, with 15ns available in military offerings. The x8 version of these products is especially well suited for the next generation size of caches in high-end PC applications, while the x4 device is well matched to communications and workstation implementations.

Size	Organization	Process	Part Number	Power	Speeds Commercial	Speeds Military
1M	256K x 4	CMOS	71028	S/L	12,15,17	15,17,20,25
	128K x 8	CMOS	71024	S/L	12,15,17,20	15,17,20,25

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TABLE OF CONTENTS

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Integrated Device Technology, Inc.

CMOS STATIC RAM 1 MEG (256K x 4-BIT)

IDT71028

FEATURES:

- 256K x 4 advanced high-speed CMOS static RAM
- Equal access and cycle times
  - — Military: 15/17/20/25ns
  - — Commercial: 12/15/17ns
- One Chip Select plus one Output Enable pin
- Bidirectional data Inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in 28-pin Ceramic DIP, Plastic DIP, 300 mil and 400 mil Plastic SOJ, and LCC packages
- Military product compliant to MIL-STD-883, Class B

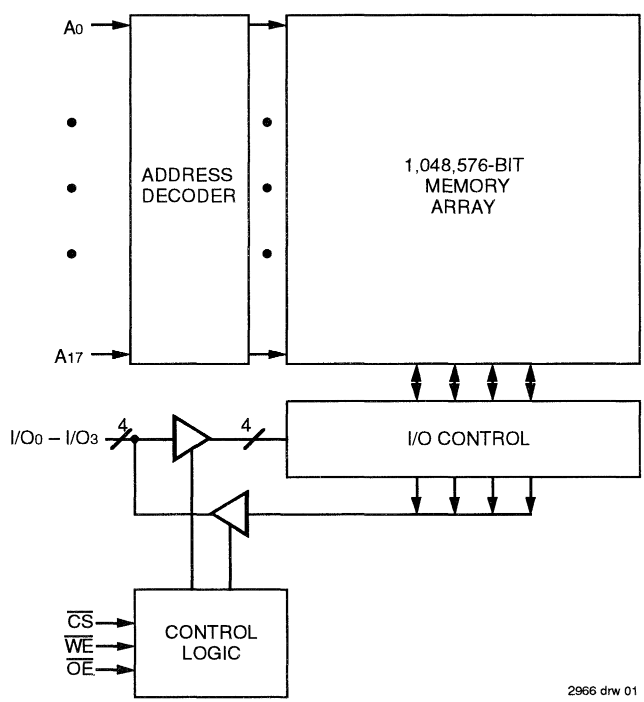
DESCRIPTION:

The IDT71028 is a 1,024,576-bit high-speed static RAM organized as 256K x 4. It is fabricated using IDT's high-perfomance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71028 has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns. All bidirectional inputs and outputs of the IDT71028 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71028 is packaged in 28-pin 400 mil Ceramic DIP, 28-pin 400 mil Plastic DIP, 28-pin 300 mil Plastic SOJ, 28-pin 400 mil Plastic SOJ, and 28-pin Leadless Chip Carrier packages.

FUNCTIONAL BLOCK DIAGRAM



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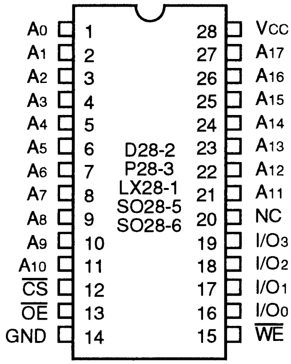
PIN CONFIGURATION



2966 drw 02

DIP/SOJ/LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.25	1.25	W
I_{OUT}	DC Output Current	50	50	mA

NOTES: 2966 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

TRUTH TABLE[1,2]

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	$DATA_{OUT}$	Read Data
L	X	L	$DATA_{IN}$	Write Data
L	H	H	High-Z	Output Disabled
H	X	X	High-Z	Deselected - Standby (I_{SB})
V_{HC}[3]	X	X	High-Z	Deselected - Standby (I_{SB1})

NOTES: 2966 tbl 01

1. H = V_{IH}, L = V_{IL}, x = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V.
3. Other inputs $\geq V_{HC}$ or $\leq V_{LC}$.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	8	pF

NOTE: 2966 tbl 03

1. This parameter is guaranteed by device characterization, but not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC}+0.5	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2966 tbl 04

1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

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DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71028 Min.	IDT71028 Max.	Unit
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2966 tbl 05

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

		71028S12(3)		71028S15		71028S17		71028S20		71028S25		
Symbol	Parameter	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Unit
I_{CC}	Dynamic Operating Current, $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	155	—	150	175	145	165	—	155	—	140	mA
I_{SB}	Standby Power Supply Current (TTL Level), $\overline{CS} \ge V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	35	—	35	45	35	40	—	40	—	35	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level), $\overline{CS} \ge V_{HC}$, Outputs Open, V_{CC} = Max., f = 0(2), $V_{IN} \le V_{LC}$ or $V_{IN} \ge V_{HC}$	10	—	10	15	10	15	—	15	—	15	mA

NOTES: 2966 tbl 06

1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.
3. 12ns specification is preliminary.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2966 tbl 07

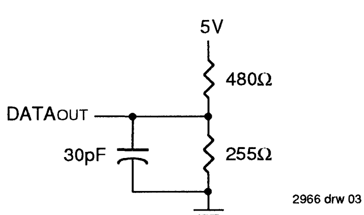
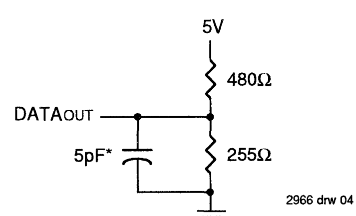


Figure 1. AC Test Load



*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

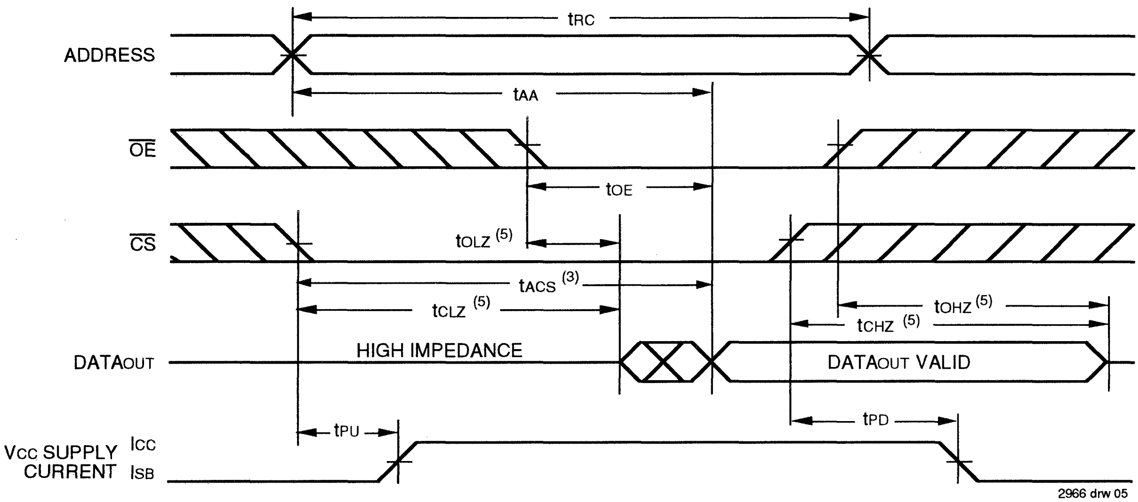
Symbol	Parameter	71028S12(1)		71028S15		71028S17		71028S20(2)		71028S25(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tRC	Read Cycle Time	12	—	15	—	17	—	20	—	25	—	ns
tAA	Address Access Time	—	12	—	15	—	17	—	20	—	25	ns
tACS	Chip Select Access Time	—	12	—	15	—	17	—	20	—	25	ns
tCLZ(3)	Chip Select to Output in Low-Z	3	—	3	—	3	—	3	—	3	—	ns
tCHZ(3)	Chip Deselect to Output in High-Z	0	6	0	7	0	8	0	8	0	10	ns
tOE	Output Enable to Output Valid	—	6	—	7	—	8	—	8	—	10	ns
tOLZ(3)	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	0	—	ns
tOHZ(3)	Output Disable to Output in High-Z	0	5	0	5	0	6	0	7	0	10	ns
tOH	Output Hold from Address Change	2	—	2	—	2	—	2	—	2	—	ns
tPU(3)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD(3)	Chip Deselect to Power Down Time	—	12	—	15	—	17	—	20	—	25	ns
Write Cycle												
tWC	Write Cycle Time	12	—	15	—	17	—	20	—	25	—	ns
tAW	Address Valid to End of Write	10	—	12	—	13	—	15	—	15	—	ns
tCW	Chip Select to End of Write	10	—	12	—	13	—	15	—	15	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	10	—	12	—	13	—	15	—	15	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	7	—	8	—	9	—	9	—	10	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tOW(3)	Output Active from End of Write	3	—	3	—	3	—	4	—	4	—	ns
tWHZ(3)	Write Enable to Output in High-Z	0	5	0	5	0	7	0	8	0	9	ns

2966 tbl 08

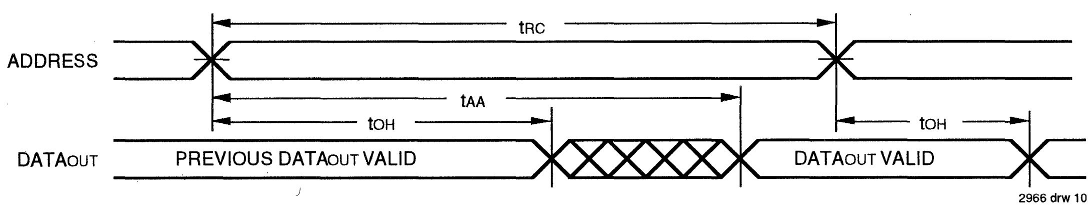
NOTES:
1. 0° to +70°C temperature range only. 12ns specification is preliminary.
2. –55°C to +125°C temperature range only.
3. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.

8

TIMING WAVEFORM OF READ CYCLE NO. 1[1]

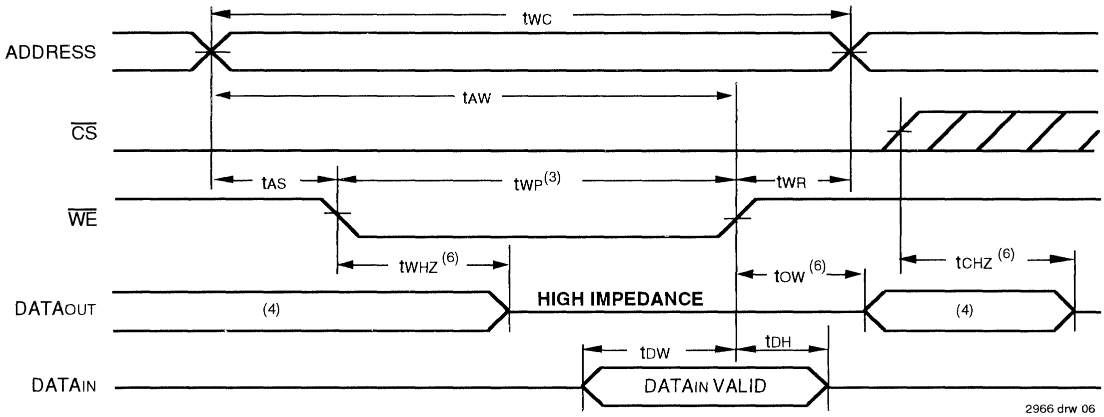


TIMING WAVEFORM OF READ CYCLE NO. 2[1,2,4]

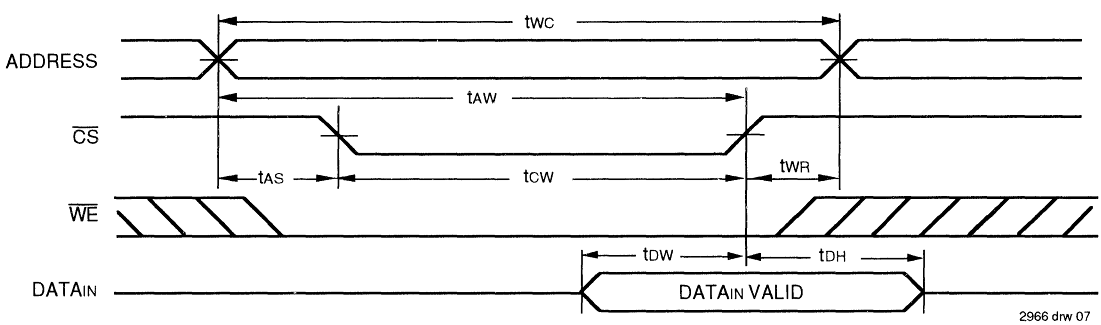


NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,5)



TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP}.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.

8

ORDERING INFORMATION

IDT 71028 S XX XX X

71028	S	XX	XX	X
Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range:

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:

L	400 x 720-mil LCC (L28-1)
C	400-mil Sidebraze DIP (D28-2)
P	400-mil Plastic DIP (P28-3)
Y	400-mil Small Outline J-Bend (SO28-6)
TY	300-mil Small Outline J-Bend (SO28-5)

Speed:

12	Commercial Only
15	
17	
20	Military Only
25	Military Only

Speed in nanoseconds

2966 drw 08

Integrated Device Technology, Inc.

CMOS STATIC RAM
1 MEG (128K x 8-BIT)

IDT71024

FEATURES:

- 128K x 8 advanced high-speed CMOS static RAM
- Equal access and cycle times
  - — Military: 15/17/20/25ns
  - — Commercial: 12/15/17/20ns
- Two Chip Selects plus one Output Enable pin
- Bidirectional inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in 32-pin Ceramic DIP, Plastic DIP, 300 and 400 mil Plastic SOJ, and LCC packages
- Military product compliant to MIL-STD-883, Class B

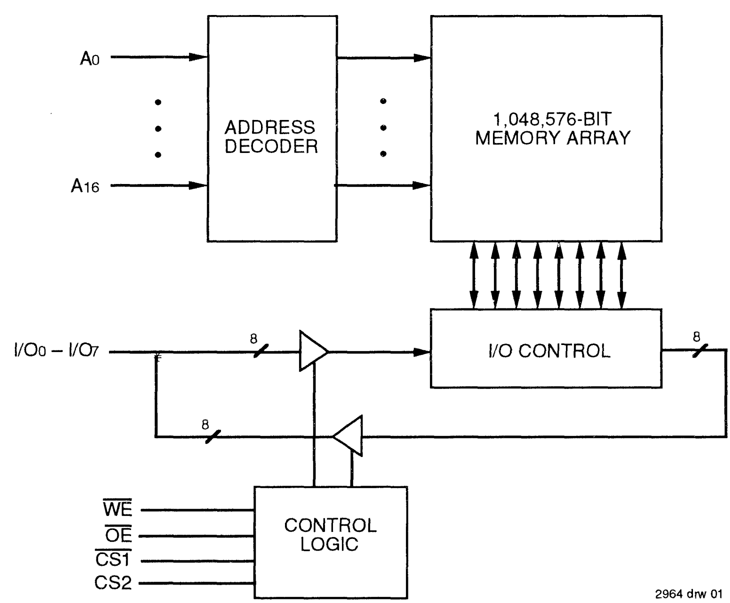
DESCRIPTION:

The IDT71024 is a 1,048,576-bit high-speed static RAM organized as 128K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71024 has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns available. All bidirectional inputs and outputs of the IDT71024 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used; no clocks or refreshes are required for operation.

The IDT71024 is packaged in 32-pin 400 mil Ceramic DIP, 32-pin 400 mil Plastic DIP, 32-pin 300 mil Plastic SOJ, 32-pin 400 mil Plastic SOJ, and 32-pin 400 x 820 mil LCC packages.

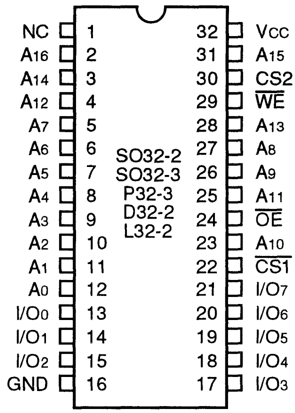
FUNCTIONAL BLOCK DIAGRAM



8

The IDT Logo is a registered trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



2964 drw 02

DIP/SOJ/LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.25	1.25	W
I_{OUT}	DC Output Current	50	50	mA

NOTES: 2964 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

TRUTH TABLE(1,2)

INPUTS					
$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	I/O	FUNCTION
X	H	X	X	High-Z	Deselected–Standby (I_{SB})
X	V_{HC}(3)	X	X	High-Z	Deselected–Standby (I_{SB1})
X	X	L	X	High-Z	Deselected–Standby (I_{SB})
X	X	V_{LC}(3)	X	High-Z	Deselected–Standby (I_{SB1})
H	L	H	H	High-Z	Outputs Disabled
H	L	H	L	DATAOUT	Read Data
L	L	H	X	DATAIN	Write Data

NOTES: 2964 tbl 01

1. H = V_{IH}, L = V_{IL}, X = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V.
3. Other inputs $\geq V_{HC}$ or $\leq V_{LC}$.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	8	pF

NOTE: 2964 tbl 03

1. This parameter is guaranteed by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	Vcc+0.5	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2964 tbl 04

1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71024 Min.	IDT71024 Max.	Unit
$\lvert I_{LI}\rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\lvert I_{LO}\rvert$	Output Leakage Current	V_{CC} = Max., $\overline{CS1}$ = V_{IH}, CS2 = V_{IL}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2964 tbl 05

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

		71024S12[3]		71024S15		71024S17		71024S20		71024S25		
Symbol	Parameter	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Unit
I_{CC}	Dynamic Operating Current, CS2 ≥ V_{IH} and CS2 ≥ V_{IH} and $\overline{CS1}$ ≤ V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	160	—	155	180	150	170	140	160	—	145	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS1}$ ≥ V_{IH} or CS2 ≤ V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	35	—	35	40	35	40	35	40	—	35	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS1}$ ≥ V_{HC}, or CS2 ≤ V_{LC} Outputs Open, V_{CC} = Max., f = 0[2], V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}	15	—	10	15	10	15	10	15	—	15	mA

2964 tbl 06

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.
3. 12ns specification is preliminary.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2964 tbl 07

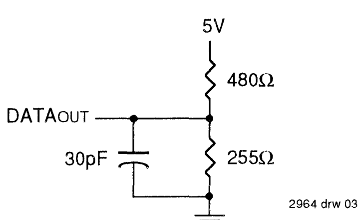
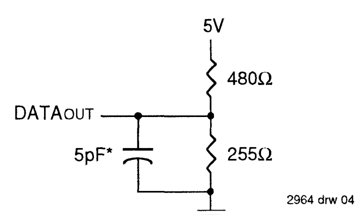


Figure 1. AC Test Load



*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

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AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

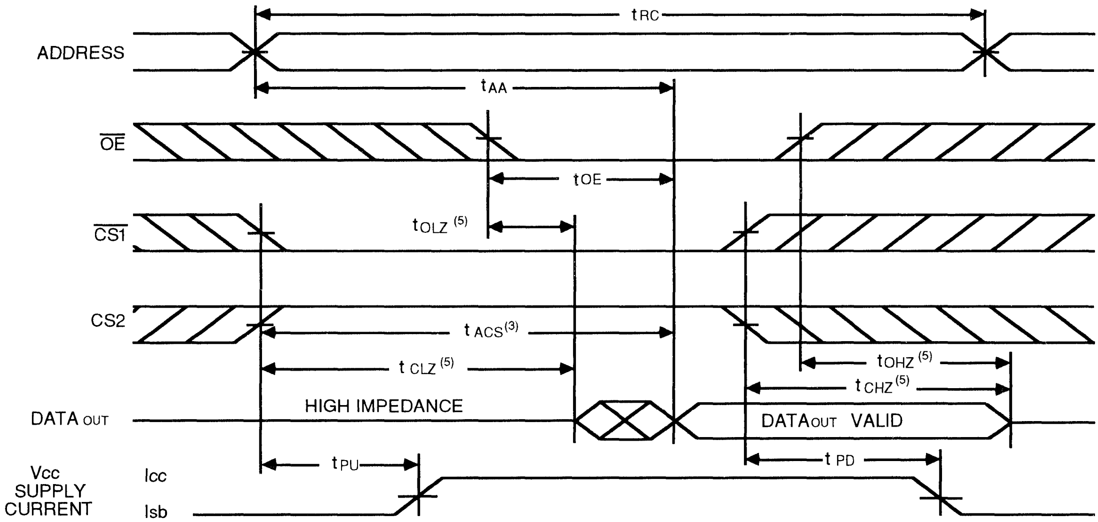
Symbol	Parameter	71024S12(1)		71024S15		71024S17		71024S20		71024S25(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	12	—	15	—	17	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	17	—	20	—	25	ns
t_{ACS}	Chip Select Access Time	—	12	—	15	—	17	—	20	—	25	ns
t_{CLZ}(3)	Chip Select to Output in Low-Z	3	—	3	—	3	—	3	—	3	—	ns
t_{CHZ}(3)	Chip Deselect to Output in High-Z	0	6	0	7	0	8	0	8	0	10	ns
t_{OE}	Output Enable to Output Valid	—	6	—	7	—	8	—	8	—	10	ns
t_{OLZ}(3)	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	0	—	ns
t_{OHZ}(3)	Output Disable to Output in High-Z	0	5	0	5	0	6	0	7	0	10	ns
t_{OH}	Output Hold from Address Change	4	—	4	—	4	—	4	—	4	—	ns
t_{PU}(3)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}(3)	Chip Deselect to Power-Down Time	—	12	—	15	—	17	—	20	—	25	ns
Write Cycle												
t_{WC}	Write Cycle Time	12	—	15	—	17	—	20	—	25	—	ns
t_{AW}	Address Valid to End-of-Write	10	—	12	—	13	—	15	—	15	—	ns
t_{CW}	Chip Select to End-of-Write	10	—	12	—	13	—	15	—	15	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	10	—	12	—	13	—	15	—	15	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	7	—	8	—	9	—	9	—	10	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OW}(3)	Output Active from End-of-Write	3	—	3	—	3	—	4	—	4	—	ns
t_{WHZ}(3)	Write Enable to Output in High-Z	0	5	0	5	0	7	0	8	0	9	ns

NOTES:

2964 tbl 08

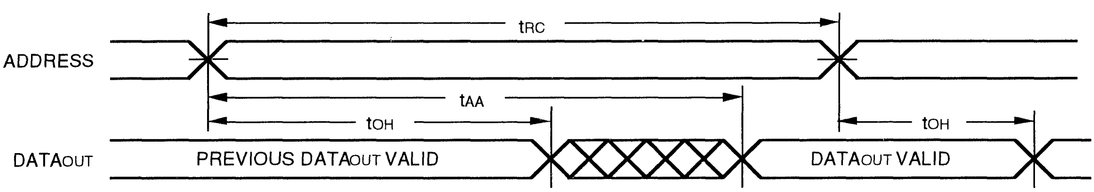
1. 0°C to +70°C temperature range only. 12ns specification is preliminary.
2. –55°C to +125°C temperature range only.
3. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



2964 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

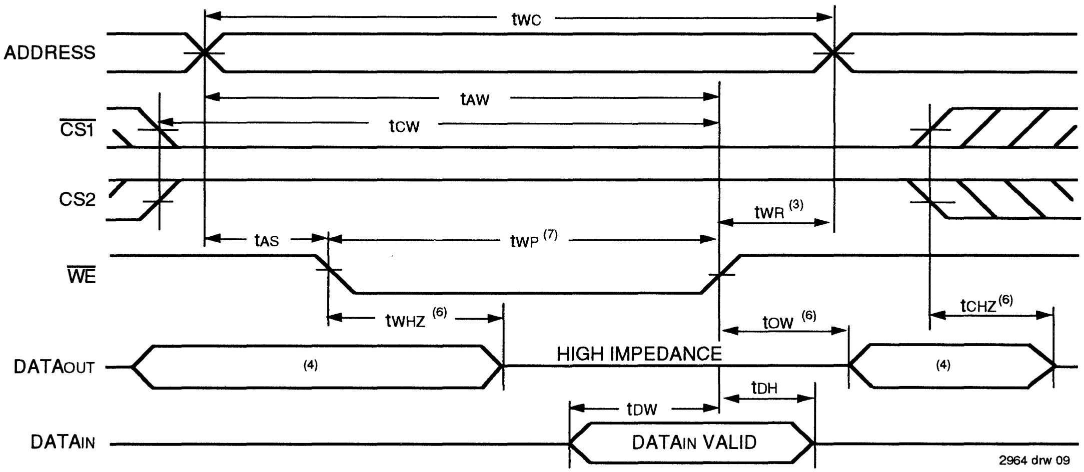


2964 drw 07

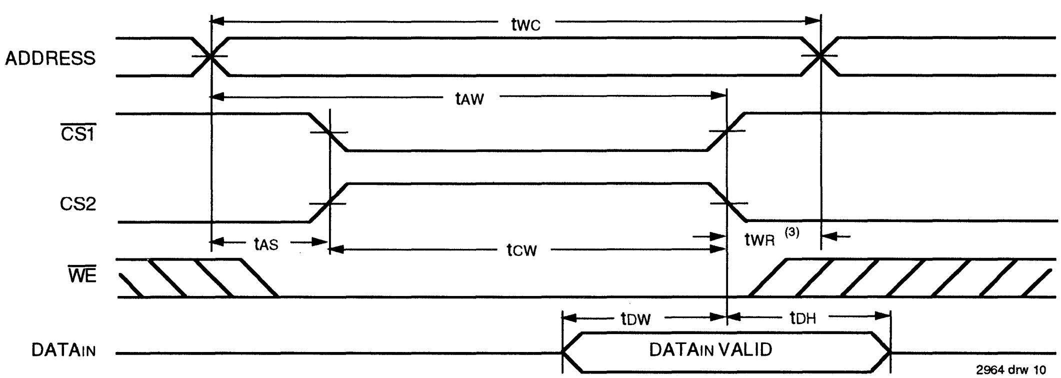
8

NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS1}$ is LOW, CS2 is HIGH.
3. Address must be valid prior to or coincident with the later of $\overline{CS1}$ transition LOW and CS2 transition HIGH; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 5, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS1}$ AND CS2 CONTROLLED TIMING)(1, 2, 5)



NOTES:
1. $\overline{WE}$ must be HIGH, $\overline{CS1}$ must be HIGH, or CS2 must be LOW during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS1}$, HIGH CS2, and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of either $\overline{CS1}$ or $\overline{WE}$ going HIGH or CS2 going LOW to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS1}$ LOW transition or the CS2 HIGH transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high impedance state. $\overline{CS1}$ and CS2 must both be active during the tCW write period.
6. Transition is measured ±200mV from steady state.
7. $\overline{OE}$ is continuously HIGH. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ LOW, tWP must be greater than or equal to tWHZ + tDW to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified tWP.

ORDERING INFORMATION

IDT	71024	S	XX	X	X
	Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package

D	400-mil Ceramic DIP (D32-2)
P	400-mil Plastic DIP (P32-3)
L	400 x 820 mil LCC package (L32-2)
TY	300-mil SOJ (SO32-2)
Y	400-mil SOJ (SO32-3)

Speed

12	Commercial Only	Speed in nanoseconds
15		
17		
20		
25	Military Only	

2964 drw 11

8

3.3V SRAM PRODUCTS

IDT introduced the first true fast 3.3V SRAM in the world in 1992, the IDT713256SL, and we have continued to optimize our processes and designs to better perform in the emerging 3.3V marketplace. By developing 3.3V-specific designs and processes, IDT's 3.3V SRAMs exhibit excellent parametric characteristics both in speed and power consumption, as well as full compliance with the JEDEC LVTTL standard.

The IDT71V256SL (32K x 8) has an access time as fast as 15ns to provide the ultimate asynchronous SRAM performance in both desktop and notebook PC's, while the IDT71V256SA provides more cost effective 20ns performance for less demanding applications.

These parts are ideal for portable equipment where both battery-life extension is essential and high-performance is necessary (<25ns speeds). The small SOJ and TSOP packages available help alleviate the typical space constraint in portable equipment.

Function	Organization	Features	Process	Part Number	Power	Speeds	
						Commercial	Military
3.3V SRAMs	32K x 8	3.3V	3.3V CMOS	71V256	SA	20,25	N/A
	32K x 8	3.3V	3.3V CMOS	71V256	SL	15	N/A

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TABLE OF CONTENTS

9

LOW POWER 3.3V CMOS FAST SRAM 256K (32K x 8-BIT)

PRELIMINARY
IDT71V256SA

Integrated Device Technology, Inc.

FEATURES

- Ideal for high-performance processor secondary cache
- Fast access times:
  — 20/25ns
- Low standby current (maximums):
  — 15mA standby
  — 500uA full standby
- Small packages for space-efficient layouts:
  — 28-pin 300 mil SOJ
- Ideal configuration for large cache sizes, with minimum space and minimum power:
  — 32K x 8
- Produced with advanced high-performance CMOS technology
- Inputs and outputs are LVTTL-compatible
- Single 3.3V(±0.3V) power supply

DESCRIPTION

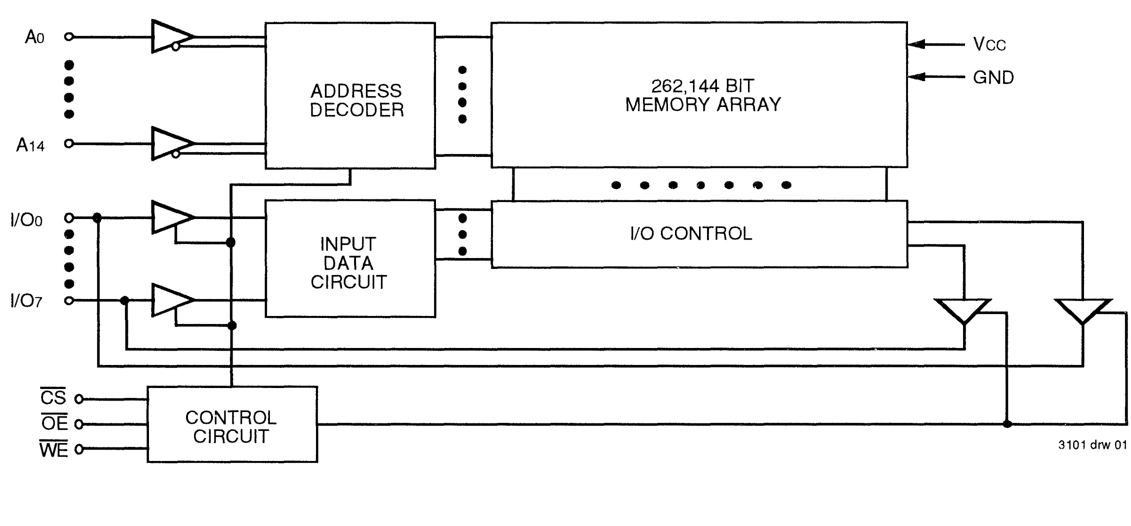
The IDT71V256SA is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

The IDT71V256SA has outstanding low power characteristics while at the same time maintaining very high performance. Address access times of 20 and 25ns are ideal for 3.3V secondary cache in 3.3V desktop designs.

When power management logic puts the IDT71V256SA in standby mode, its very low power characteristics contribute to extended battery life. By taking $\overline{CS}$ HIGH, the SRAM will automatically go to a low power standby mode and will remain in standby as long as $\overline{CS}$ remains HIGH. Furthermore, under full standby mode ($\overline{CS}$ at CMOS level, f=0), power consumption is guaranteed to always be less than 1.65mW and typically will be much smaller.

The IDT71V256SA is packaged in 28-pin 300 mil SOJ packaging.

FUNCTIONAL BLOCK DIAGRAM



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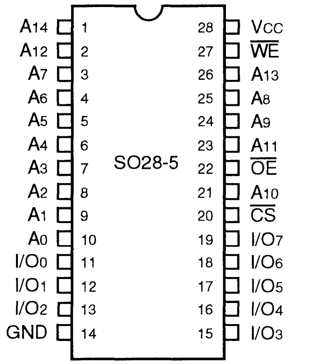
PIN CONFIGURATIONS



3101 drw 02

**SOJ
TOP VIEW**

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to VCC+0.5	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTES: 3101 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals only.
3. Input, Output, and I/O terminals; 4.6V maximum.

PIN DESCRIPTIONS

Name	Description
A_0–A_{14}	Addresses
I/O_0–I/O_7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
Vcc	Power

3101 tbl 01

TRUTH TABLE(1)

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
X	H	X	High-Z	Standby (ISB)
X	V_{HC}	X	High-Z	Standby (ISB1)
H	L	H	High-Z	Output Disable
H	L	L	D_{OUT}	Read
L	L	X	D_{IN}	Write

NOTE: 3101 tbl 02

1. H = V_{IH}, L = V_{IL}, X = Don't Care

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	7	pF

NOTE: 3101 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 0.3V

3101 tbl 05

9

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	Vcc+0.3	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 3101 tbl 06

1. V_{IL} (min.) = –1.0V for pulse width less than 5ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS(1, 2)

(V_{CC} = 3.3V ± 0.3V, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	71V256SA20 Com'l.	71V256SA25 Com'l.	Unit
I_{CC}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	105	100	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} = V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	20	20	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., f = 0	0.5	0.5	mA

3101 tbl 07

NOTES:
1. All values are maximum guaranteed values.
2. $f_{MAX} = 1/t_{RC}$, only address inputs cycling at fmax; f = 0 means that no inputs are cycling.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V± 0.3V

Symbol	Parameter	Test Condition	IDT71V256SA Min.	IDT71V256SA Typ.	IDT71V256SA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	—	2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS} = V_{IH}$, V_{OUT} = GND to V_{CC}	—	—	2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	—	V

3101 tbl 09

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3101 tbl 08

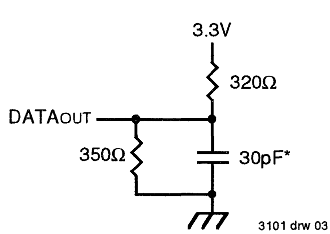


Figure 1. AC Test Load

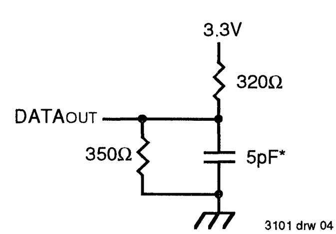


Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (Vcc = 3.3V ± 0.3V, Commercial Temperature Range)

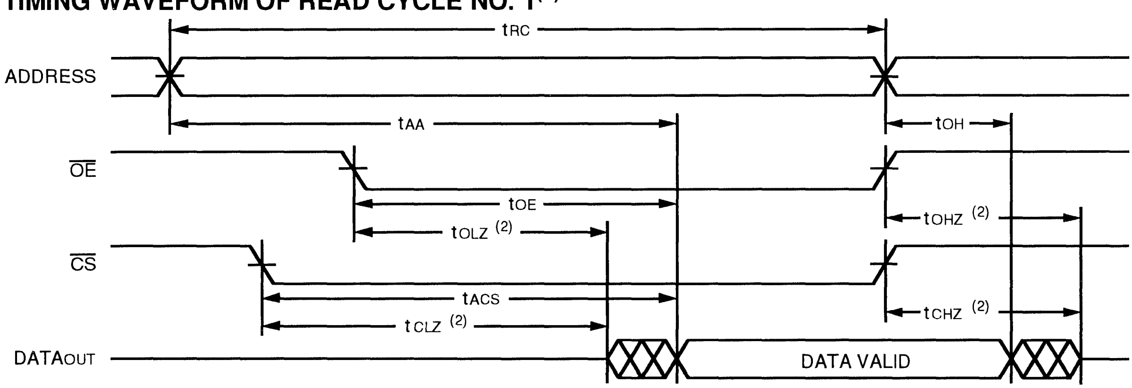
Symbol	Parameter	71V256SA20 Min.	71V256SA20 Max.	71V256SA25 Min.	71V256SA25 Max.	Unit
Read Cycle						
tRC	Read Cycle Time	20	—	25	—	ns
tAA	Address Access Time	—	20	—	25	ns
tACS	Chip Select Access Time	—	20	—	25	ns
tCLZ(1)	Chip Select to Output in Low-Z	5	—	5	—	ns
tCHZ(1)	Chip Select to Output in High-Z	0	10	0	11	ns
tOE	Output Enable to Output Valid	—	8	—	10	ns
tOLZ(1)	Output Enable to Output in Low-Z	3	—	3	—	ns
tOHZ(1)	Output Disable to Output in High-Z	2	8	2	10	ns
tOH	Output Hold from Address Change	3	—	3	—	ns
Write Cycle						
tWC	Write Cycle Time	20	—	25	—	ns
tAW	Address Valid to End-of-Write	15	—	20	—	ns
tCW	Chip Select to End-of-Write	15	—	20	—	ns
tAS	Address Set-up Time	0	—	0	—	ns
tWP	Write Pulse Width	15	—	15	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tDW	Data to Write Time Overlap	8	—	10	—	ns
tDH	Data Hold from Write Time	0	—	0	—	ns
tOW(1)	Output Active from End-of-Write	4	—	4	—	ns
tWHZ(1)	Write Enable to Output in High-Z	1	10	1	11	ns

NOTE:

3101 tbl 11

1. This parameter guaranteed with the AC test load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)

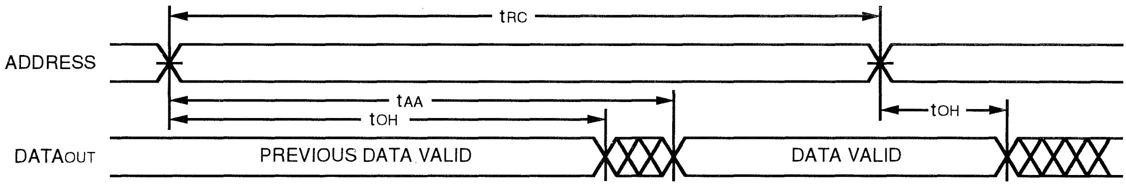


3101 drw 05

NOTES:
1. WE is HIGH for Read cycle.
2. Transition is measured ±200mV from steady state.

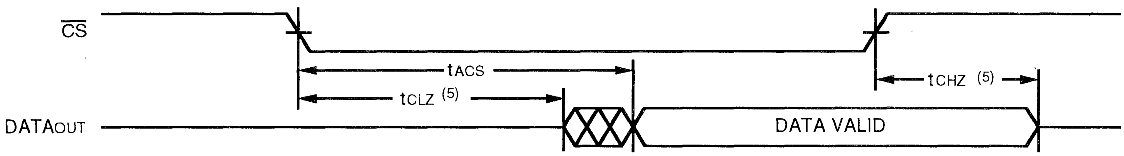
9

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



3101 drw 06

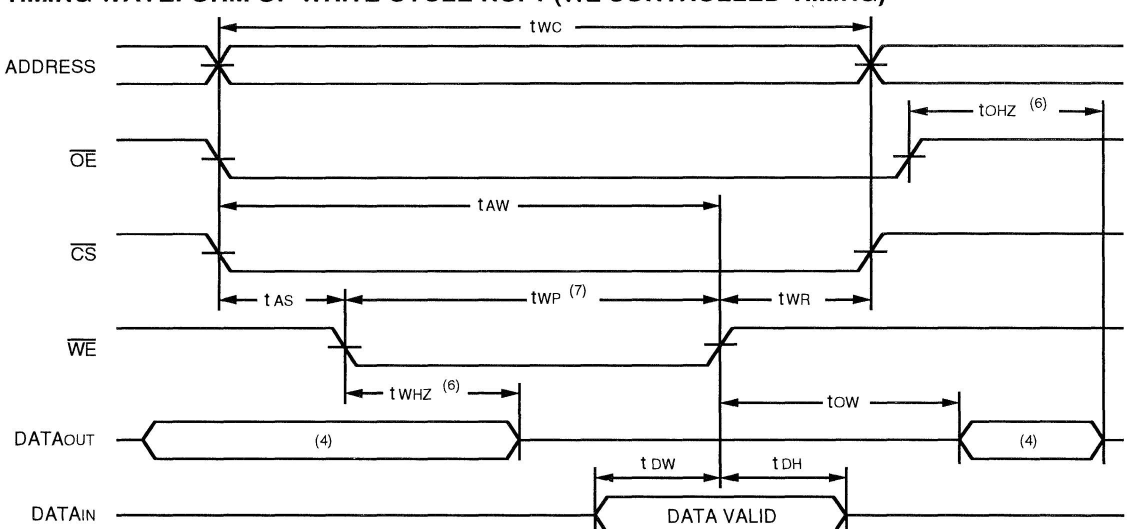
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



3101 drw 07

NOTES:
1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

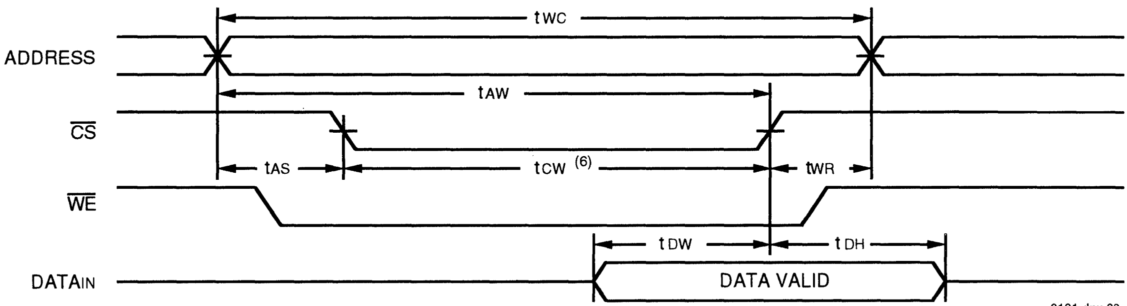
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 5, 7)



3101 drw 08

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the spectified t_{WP}.

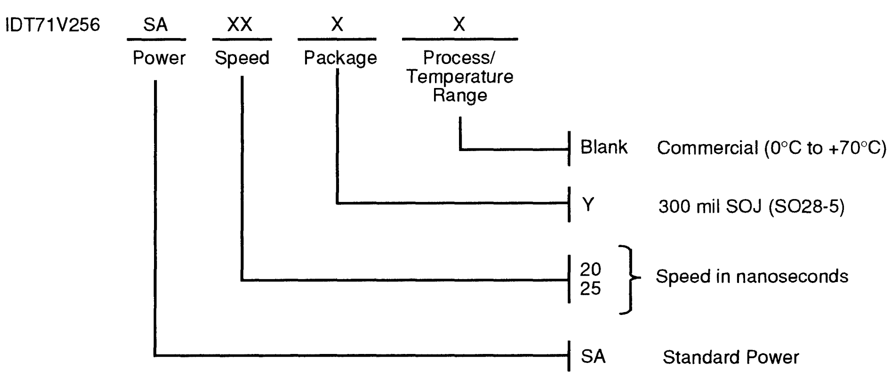
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 4)



3101 drw 09

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the spectified tWP.

ORDERING INFORMATION



3101 drw 10

9

VERY LOW POWER 3.3V CMOS FAST SRAM 256K (32K x 8-BIT)

IDT71V256SL

FEATURES

- Ideal for high-performance processor secondary cache, notebook/sub-notebook cache, and other battery-operated applications
- Fast access times:
  — 15ns
- Very low standby current (maximums):
  — 3.0mA standby
  — 500uA full standby
- Small packages for space-efficient layouts:
  — 28-pin 300 mil SOJ
  — 28-pin 300 mil plastic DIP
  — 28-pin TSOP Type I
- Ideal configuration for large cache sizes, with minimum space and minimum power:
  — 32K x 8
- Produced with advanced high-performance CMOS technology
- Inputs and outputs are LVTTL-compatible
- Single 3.3V(±0.3V) power supply

DESCRIPTION

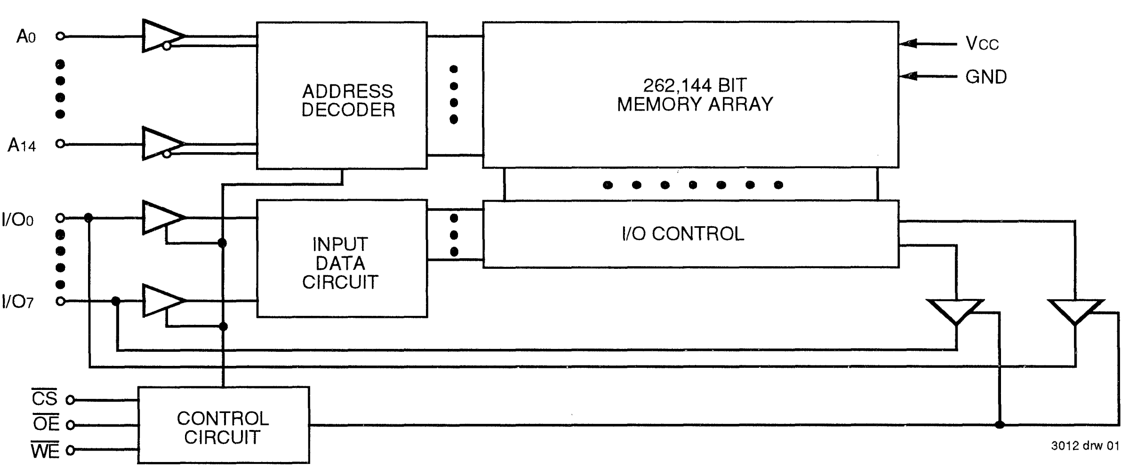
The IDT71V256SL is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

The IDT71V256SL has outstanding low power characteristics while at the same time maintaining very high performance. Address access time of 15ns is ideal for 3.3V secondary cache designs in both 3.3V desktop and notebook designs. Portable communications and test equipment also benefit from these fast speeds and low power.

When power management logic puts the IDT71V256SL in standby mode, its very low power characteristics contribute to extended battery life. By taking $\overline{CS}$ HIGH, the SRAM will automatically go to a low power standby mode and will remain in standby as long as $\overline{CS}$ remains HIGH. Furthermore, under full standby mode ($\overline{CS}$ at CMOS level, f=0), power consumption is guaranteed to always be less-than 1.65mW and typically will be much smaller.

The IDT71V256SL is packaged in 28-pin 300 mil SOJ, 28-pin 300 mil plastic DIP, and 28-pin 300mil TSOP Type I packaging which helps the designer attain the stringent space goals typical of notebooks, sub-notebooks, and battery-operated portable equipment.

FUNCTIONAL BLOCK DIAGRAM



3012 drw 01

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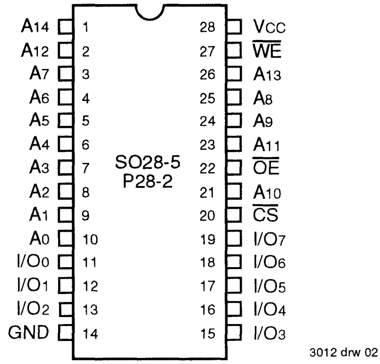
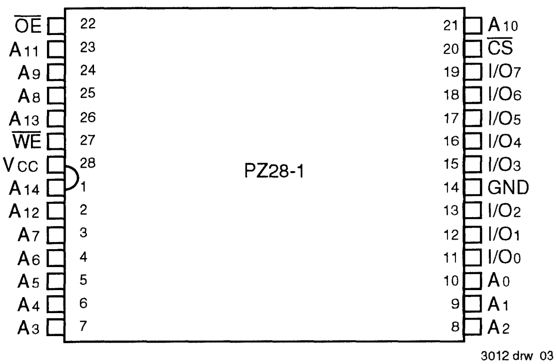
PIN CONFIGURATIONS



DIP/SOJ
TOP VIEW



TSOP
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0–A14	Addresses
I/O0–I/O7	Data Input/Output
$\overline{\text{CS}}$	Chip Select
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
GND	Ground
Vcc	Power

3012 tbl 01

TRUTH TABLE[1]

$\overline{\text{WE}}$	$\overline{\text{CS}}$	$\overline{\text{OE}}$	I/O	Function
X	H	X	High-Z	Standby (ISB)
X	VHC	X	High-Z	Standby (ISB1)
H	L	H	High-Z	Output Disable
H	L	L	DOUT	Read
L	L	X	DIN	Write

NOTE: 3012 tbl 02

1. H = VIH, L = VIL, X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Unit
VTERM[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
VTERM[3]	Terminal Voltage with Respect to GND	–0.5 to VCC+0.5	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–55 to +125	°C
TSTG	Storage Temperature	–55 to +125	°C
PT	Power Dissipation	1.0	W
IOUT	DC Output Current	50	mA

NOTES: 3012 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals only.
3. Input, Output, and I/O terminals; 4.6V maximum.

CAPACITANCE

(TA = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	5	pF
COUT	Output Capacitance	VOUT = 3dV	7	pF

NOTE: 3012 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 0.3V

3012 tbl 05

9

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.0	—	Vcc+0.3	V
VIL	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 3012 tbl 06

1. VIL (min.) = –1.0V for pulse width less than 5ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS[1, 2]

(V_{CC} = 3.3V ± 0.3V, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	71V256SL15 Com'l.	Unit
I_{CC}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	80	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} = V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[2]	3	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., f = 0	0.5	mA

3012 tbl 07

NOTES:
1. All values are maximum guaranteed values.
2. $f_{MAX} = 1/t_{RC}$, only address inputs cycling at fmax; f = 0 means that no inputs are cycling.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V± 0.3V

Symbol	Parameter	Test Condition	IDT71V256SL Min.	Typ.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	—	2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS} = V_{IH}$, V_{OUT} = GND to V_{CC}	—	—	2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	—	V

3012 tbl 09

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3012 tbl 08

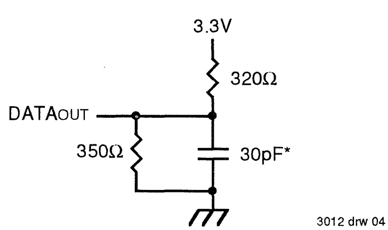


Figure 1. AC Test Load

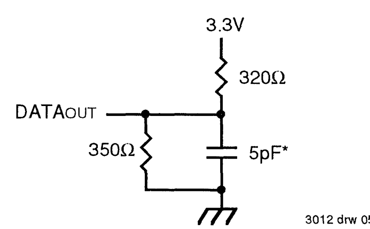


Figure 2. AC Test Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (Vcc = 3.3V ± 0.3V, Commercial Ranges)

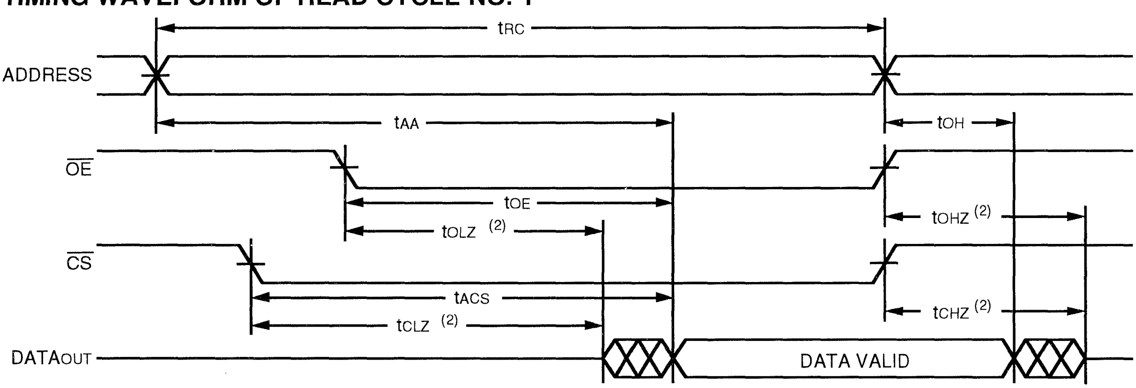
Symbol	Parameter	71V256SL15		Unit
		Min.	Max.	
Read Cycle				
t_{RC}	Read Cycle Time	15	—	ns
t_{AA}	Address Access Time	—	15	ns
t_{ACS}	Chip Select Access Time	—	15	ns
t_{CLZ}(1)	Chip Select to Output in Low-Z	5	—	ns
t_{CHZ}(1)	Chip Select to Output in High-Z	0	9	ns
t_{OE}	Output Enable to Output Valid	—	7	ns
t_{OLZ}(1)	Output Enable to Output in Low-Z	3	—	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	2	7	ns
t_{OH}	Output Hold from Address Change	3	—	ns
Write Cycle				
t_{WC}	Write Cycle Time	15	—	ns
t_{AW}	Address Valid to End-of-Write	10	—	ns
t_{CW}	Chip Select to End-of-Write	10	—	ns
t_{AS}	Address Set-up Time	0	—	ns
t_{WP}	Write Pulse Width	10	—	ns
t_{WR}	Write Recovery Time	0	—	ns
t_{DW}	Data to Write Time Overlap	7	—	ns
t_{DH}	Data Hold from Write Time	0	—	ns
t_{OW}(1)	Output Active from End-of-Write	4	—	ns
t_{WHZ}(1)	Write Enable to Output in High-Z	1	9	ns

NOTE:

3012 tbl 11

1. This parameter guaranteed with the AC test load (Figure 2) by device characterization, but is not production tested.

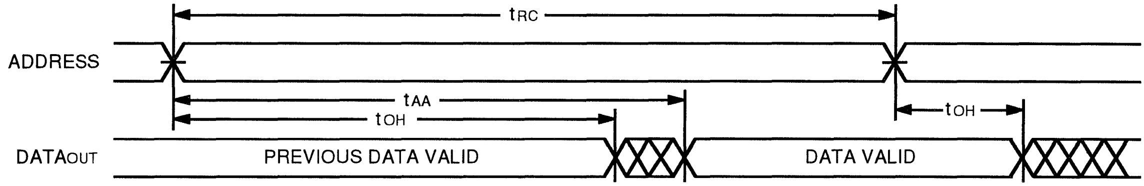
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



3012 drw 06

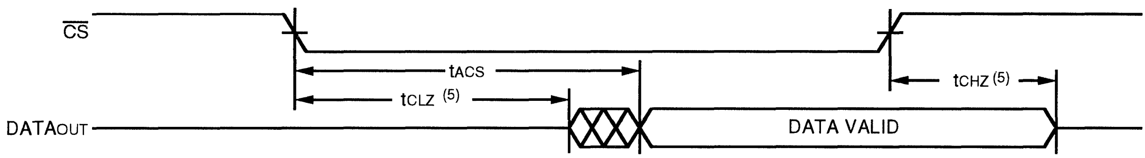
NOTES:
1. $\overline{WE}$ is HIGH for Read cycle.
2. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



3012 drw 07

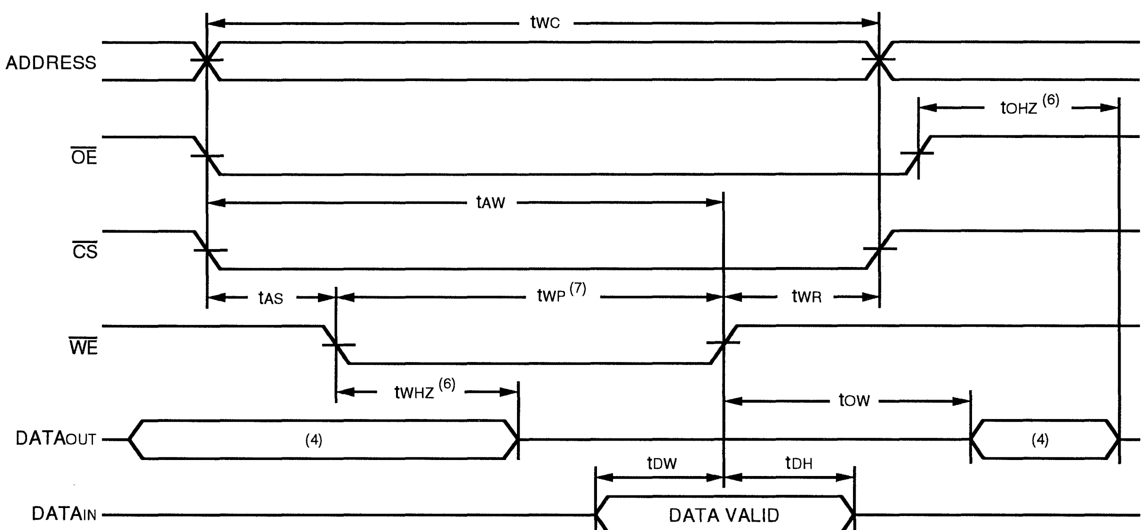
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



3012 drw 08

NOTES:
1. WE is HIGH for Read cycle.
2. Device is continuously selected, CS is LOW.
3. Address valid prior to or coincident with CS transition LOW.
4. OE is LOW.
5. Transition is measured ±200mV from steady state.

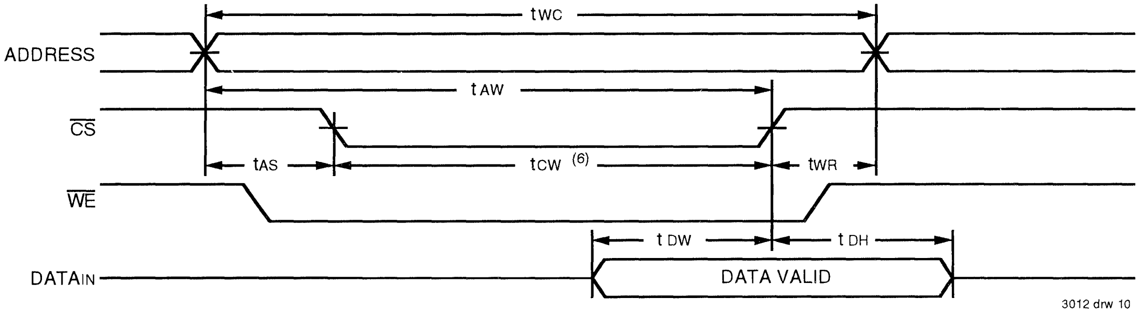
TIMING WAVEFORM OF WRITE CYCLE NO. 1 (WE CONTROLLED TIMING)(1, 2, 3, 5, 7)



3012 drw 09

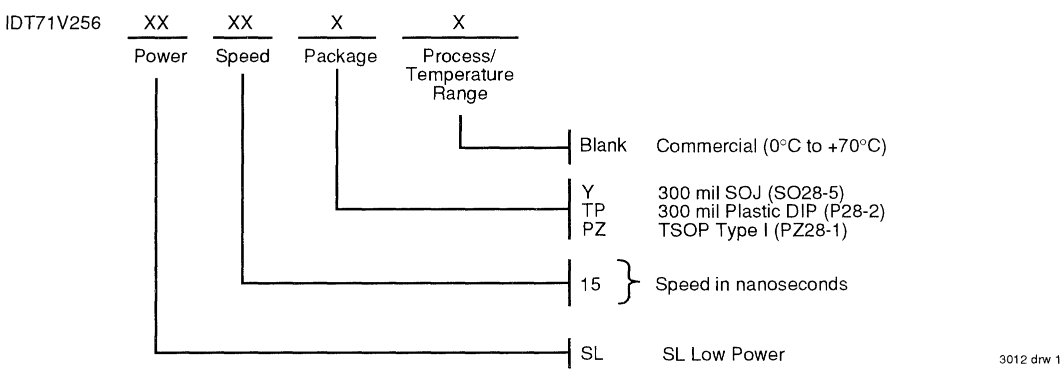
NOTES:
1. WE or CS must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW CS and a LOW WE.
3. tWR is measured from the earlier of CS or WE going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the CS LOW transition occurs simultaneously with or after the WE LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.
7. If OE is LOW during a WE controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If OE is HIGH during a WE controlled write cycle, this requirement does not apply and the write pulse can be as short as the spectified tWP.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 4)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the spectified t_{WP}.

ORDERING INFORMATION



9

CACHE SRAM PRODUCTS

IDT has been a pioneer in the area of processor specific CacheRAMs, defined and designed to meet processor secondary cache performance and configuration requirements. From the 32K x 9 Burst IDT71589 and 16K x 9 x 2 IDT71B229 to the wider configurations offered today, IDT has used technology to provide cost-effective cache data SRAMs.

Current offerings include the IDT71419 and IDT71420, which utilize BiCMOS technology to enable zero-wait state secondary cache performance at bus speeds up to 66MHz. With 3.3V bus compatibility, these devices serve the high end PC marketplace where the ultimate performance is required.

In development is a wider (x 32) device, the IDT71V432, which will provide 3.3V pipelined burst SRAM performance at an affordable cost through the use of IDT's state-of-the-art 3.3V CMOS technology.

Function	Organization	Features	Process	Part Number	Power	Speed	
						Commercial	Military
Cache SRAMs	32K x 18	PowerPC Burst	BiCMOS	71419	S	9,10,12	N/A
	32K x 18	Intel Burst	BiCMOS	71420	S	9,10,12	N/A
	32K x 32	3.3V Intel Pipelined Burst	3.3V CMOS	71V432	S	9,10,12	N/A

10

TABLE OF CONTENTS

10

Integrated Device Technology, Inc.

32K x 18 CacheRAM™ BURST COUNTER & SELF-TIMED WRITE — FOR THE PowerPC™ PROCESSOR

PRELIMINARY
IDT71419

FEATURES:

- 32K x 18 architecture
- Fast clock-to-data access times: 9, 10, 12 ns
- Internal burst read and write address counter
- Internal input registers (data and control)
- Internal address registers
- Self-timed write cycle
- Single 5V power supply
- Regulated I/Os are 3.3V LVTTL Compatible
- Complies with all timing and signals of the 68040/60 and PowerPC processor
- Packaged in a JEDEC Standard 52-pin plastic leaded chip carrier (PLCC)

DESCRIPTION:

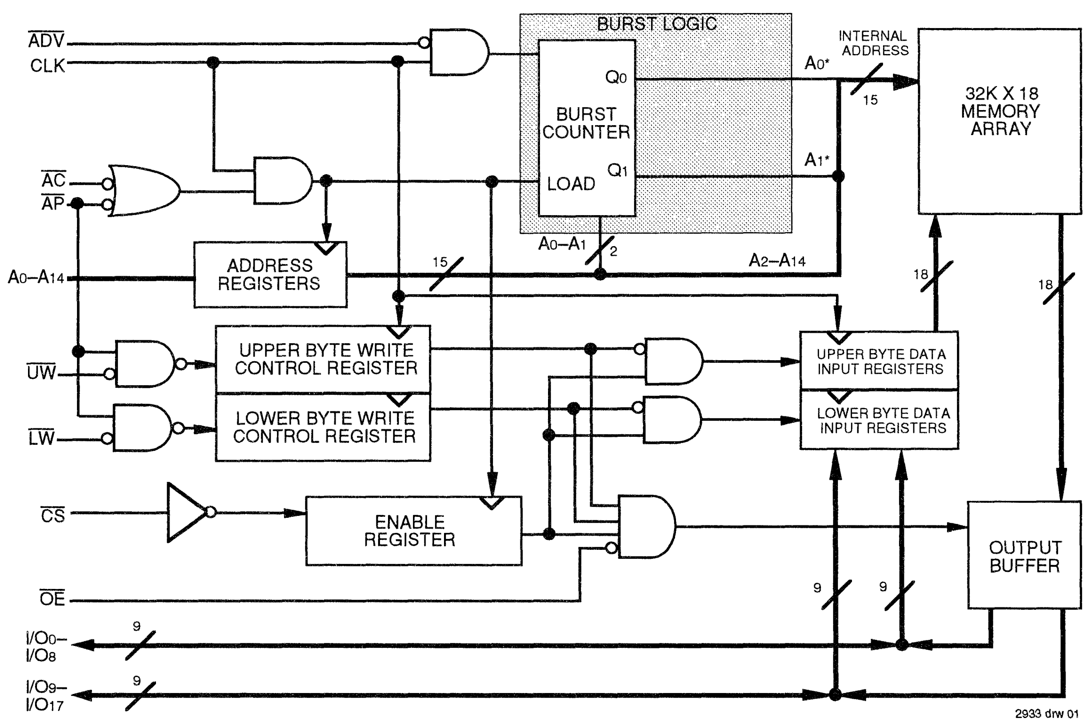
The IDT71419 is a very high-speed 32K x 18-bit static RAM with full on-chip hardware support of the PowerPC processor interface. This part is designed to facilitate the implementation of the highest performance secondary caches while using either available cache-tag SRAMs and PALs or chipsets for the PowerPC processor.

The IDT71419 CacheRAM contains a full set of write, data, address and control registers. Internal logic allows the processor to generate a self-timed write based upon a decision which can be left until the extreme end of the write cycle.

An internal burst address counter accepts the first cycle address from the processor, then cycles through the adjacent three locations using the PowerPC burst refill sequence, on appropriate rising edges of the system clock.

Fabricated using IDT's BiCMOS high-performance sub-micron technology, this device offers a maximum clock-to-data access time as fast as 9ns, while requiring an address setup of only 2.5ns.

FUNCTIONAL BLOCK DIAGRAM



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PowerPC is a trademark of International Business Machines, Inc.

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DESCRIPTION (CONTINUED)

The IDT71419 CacheRAM is packaged in a JEDEC Standard 52-pin plastic leaded chip carrier (PLCC).

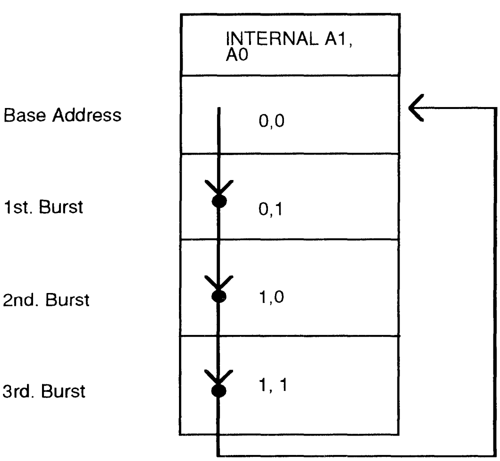
FUNCTIONALITY

The IDT71419 differs from a standard SRAM in that it's synchronous and has an internal burst counter. The synchronous functionality eases cache controller design, while the internal burst counter simplifies implementation of burst accesses.

The registered address, data-in, and write control inputs of the IDT71419 provide for synchronous write operation. All that is needed to complete a write is that the inputs be valid at rising edge of clock while meeting specified setup and hold times. This write critieria simplifies cache controller design by not requiring the write control pulse needed by asynchronous SRAMs.

A two-bit internal burst counter is used to generate the appropriate internal addresses for A0 and A1 needed for burst accesses. The burst counter starts at the base address defined by the external addresses A0 and A1. Once loaded, the internal addresses are cycled through by keeping $\overline{ADV}$ LOW at the rising edge of clock. $\overline{ADV}$ HIGH at the rising edge of clock stops the advance of the burst counter and suspends the burst sequence.

Powering up the IDT71419 is accomplished by keeping $\overline{AP}$ or $\overline{AC}$ LOW with $\overline{CS}$ LOW at the rising edge of clock. Powering down the IDT71419 is accomplished by keeping $\overline{AC}$ LOW with $\overline{CS}$ HIGH at the rising edge of clock.



Linear Burst Sequence

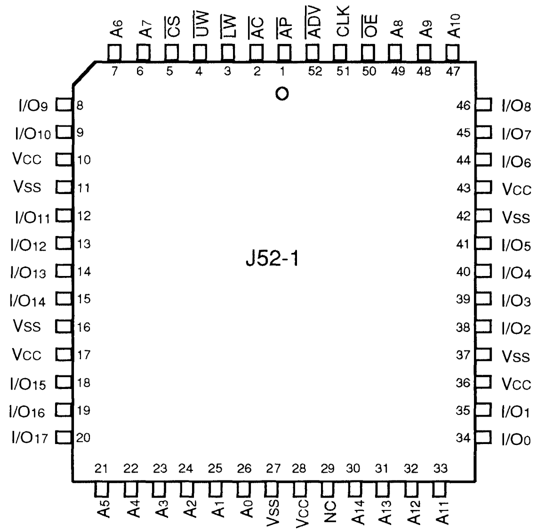
2933 drw 02

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 5%

2933 tbl 05

PIN CONFIGURATION



2933 drw 03

PLCC TOP VIEW

PIN NAMES

A0 – A14	Address Inputs
CLK	Clock
$\overline{UW}$, $\overline{LW}$	Upper, Lower Byte Write Enables
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
$\overline{ADV}$	Burst Address Advance
$\overline{AP}$, $\overline{AC}$	Burst Transfer Start (Processor & Cache Controller)
I/O0 – I/O17	Data Input/Output
Vcc	+5V Power
Vss	Ground

2933 tbl 01

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.75	5.0	5.25	V
Vss	Supply Ground	0	0	0	V
VIH	Input High Voltage	2.2	3.0	Vcc+0.5	V
VIL	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE:
2933 tbl 06

1. VIL (min.) = –1.5V for pulse width of less than 10ns, once per cycle, for I≤ 20mA.

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SYNCHRONOUS TRUTH TABLE(1, 2, 3)

$\overline{CS}$	$\overline{AP}$	$\overline{AC}$	$\overline{ADV}$	$\overline{UW}+\overline{LW}$	CLK	Address	Operation
H	L	H	X	X	↑	N/A	Deselected, Power Down
H	X	L	X	X	↑	N/A	Deselected, Power Down
L	L	X	X	X	↑	External Address	Read Cycle, Begin Burst(5)
L	H	L	X	L	↑	External Address	Write Cycle, Begin Burst(5)
L	H	L	X	H	↑	External Address	Read Cycle, Begin Burst(5)
X	H	H	L	L	↑	Next Address	Write Cycle, Continue Burst(4)
X	H	H	L	H	↑	Next Address	Read Cycle, Continue Burst(4)
X	H	H	H	L	↑	Current Address	Rewrite Cycle, Suspend Burst(4)
X	H	H	H	H	↑	Current Address	Read Cycle, Suspend Burst(4)

NOTES:
2933 tbl 02

1. L = V_{IL}, H = V_{IH}, ↑ = CLK LOW-to-HIGH transition,X = Don't Care.
2. All inputs except $\overline{OE}$ must meet setup and hold times for the LOW-to-HIGH transition of CLK; $\overline{OE}$ operates asynchronously.
3. Wait states can be inserted by suspending a burst sequence, ie. $\overline{ADV}$ = HIGH clocked in by a CLK LOW-to-HIGH transition.
4. If the device is already powered down it will remain powered down.
5. If the device is powered down it will power up.

ASYNCHRONOUS TRUTH TABLE(1, 2)

Operation	$\overline{OE}$	I/O Status
Read	L	Data Out (I/O_0 – I/O_{17})
Read	H	High-Z
Write	X	High-Z — Data In (I/O_0 – I/O_{17})
Deselected	X	High-Z

NOTES:
2933 tbl 03

1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input

CAPACITANCE

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 3dV	7	pF

NOTE:
2933 tbl 09

1. This parameter is determined by device characterization, but is not production tested.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0(2)	V
T_A	Operating Temperature	–0 to +70	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.7	W
I_{OUT}	DC Output Current	30	mA

NOTES:
2933 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.
2. V_{IN} should not exceed V_{CC}+0.5V. All pins should not exceed 7.0V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC}= Max., V_{IN} = 0V to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS} \geq V_{IH}$, $\overline{OE} \geq V_{IH}$, V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	5	µA
V_{OL}	Output Low Voltage (I/O_0–I/O_{17})	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2933 tbl 07

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1, 4) (V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Condition	71419S9 Commercial	71419S10 Commercial	71419S12 Commercial	Unit
I_{CC}	Operating Power Supply Current	$\overline{CS} \leq V_{IL}$, $\overline{OE} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	320	310	300	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$, All Inputs $\geq V_{IH}$ or $\leq V_{IL}$, V_{CC} = Max., f = f_{MAX}(3)	50	50	50	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{HC}$, All Inputs $\geq V_{HC}$ or $\leq V_{LC}$, V_{CC} = Max., f = 0(3)	30	30	30	mA

NOTES:
2933 tbl 08

1. All values are maximum guaranteed values.
2. At f = f_{MAX}, address inputs are cycling at the maximum frequency of read cycles of $1/t_{CYC}$ while $\overline{AP}$ or $\overline{AC}$ = LOW.
3. At f = f_{MAX}, address inputs are cycling at the maximum frequency of read cycles of $1/t_{CYC}$ while $\overline{AP}$, $\overline{AC}$, and $\overline{ADV}$ = HIGH. f = 0 means no address input lines change, $\overline{AP}$, $\overline{AC}$, and $\overline{ADV}$ = V_{HC}.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2933 tbl 10

AC TEST LOADS

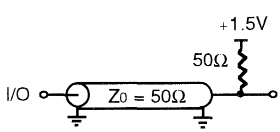


Figure 1. AC Test Load

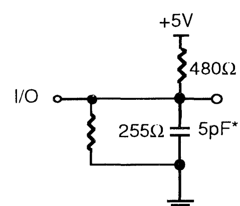


Figure 2. AC Test Load (for t_{OHZ}, t_{CHZ}, t_{OLZ}, and t_{DC1})

*** Including scope and jig**

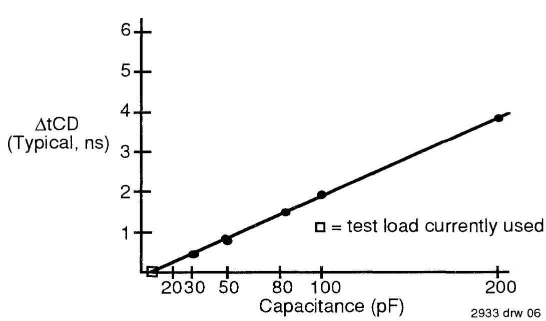


Figure 3. Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS (1, 2, 3, 6)

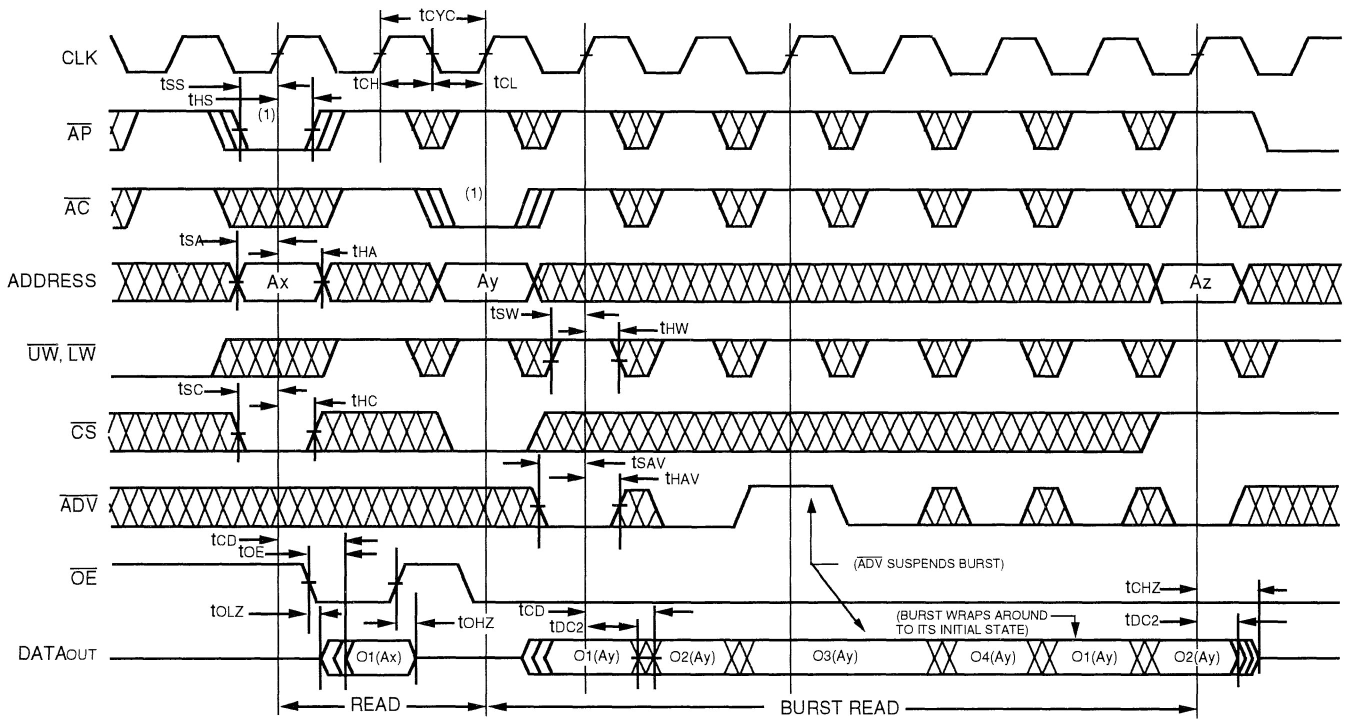
(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C)

Symbol	Parameter	IDT71419S9 Min.	IDT71419S9 Max.	IDT71419S10 Min.	IDT71419S10 Max.	IDT71419S12 Min.	IDT71419S12 Max.	Unit
t_{CYC}(4)	Cycle Time	15	—	16.6	—	20	—	ns
t_{CD}	Clock Access Time	—	9	—	10	—	12	ns
t_{OE}	Output Enable Access	—	5	—	6	—	7	ns
t_{DC1}(5)	Clock High to Output Active	3	—	3	—	3	—	ns
t_{DC2}	Clock High to Data Change	3	—	3	—	3	—	ns
t_{OLZ}(5)	Output Enable to Data Active	0	—	0	—	0	—	ns
t_{OHZ}(5)	Output Disable to Data High-Z	2	6	2	6	2	7	ns
t_{CHZ}(5)	Clock High to Data High-Z	—	6	—	6	—	6	ns
t_{CH}(7)	Clock High Pulse Width	5	—	5.5	—	6	—	ns
t_{CL}(7)	Clock Low Pulse Width	5	—	5.5	—	6	—	ns
t_{SA}(6)	Address Setup Time	2.5	—	2.5	—	3	—	ns
t_{SS}(6)	Address Status Setup Time	2.5	—	2.5	—	3	—	ns
t_{SD}(6)	Data In Setup Time	2.5	—	2.5	—	3	—	ns
t_{SW}(6)	Write Setup Time	2.5	—	2.5	—	3	—	ns
t_{SAV}(6)	Address Advance Setup Time	2.5	—	2.5	—	3	—	ns
t_{SC}(6)	Chip Select Setup Time	2.5	—	2.5	—	3	—	ns
t_{HA}(6)	Address Hold Time	2	—	2	—	2	—	ns
t_{HS}(6)	Address Status Hold Time	2	—	2	—	2	—	ns
t_{HD}(6)	Data In Hold Time	2	—	2	—	2	—	ns
t_{HW}(6)	Write Hold Time	2	—	2	—	2	—	ns
t_{HAV}(6)	Address Advance Hold Time	2	—	2	—	2	—	ns
t_{HC}(6)	Chip Select Hold Time	2	—	2	—	2	—	ns

2933 tbl 11

NOTES:
1. A read cycle is defined by both $\overline{UW}$ and $\overline{LW}$ = HIGH or $\overline{AP}$ = LOW. A write cycle is defined by either $\overline{UW}$ or $\overline{LW}$ = LOW and $\overline{AP}$ = HIGH.
2. All read and write cycle timings are referenced from CLK, or $\overline{OE}$ as it applies.
3. $\overline{OE}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ = LOW is clocked in.
4. Maximum access times are guaranteed from all possible PowerPC external bus cycles.
5. Transition is measured ±200mV from steady-state. This parameter is guaranteed by device characterization with the AC Load (Figure 2), but is not production tested.
6. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times for ALL rising edges of CLK when the chip is selected. Chip Select must be active ($\overline{CS}$ = LOW) at each rising edge of clock when $\overline{AC}$ or $\overline{AP}$ is LOW for the device to remain enabled.
7. This parameter is measured HIGH above 2.2V and LOW below 0.8V.

READ CYCLES(2)

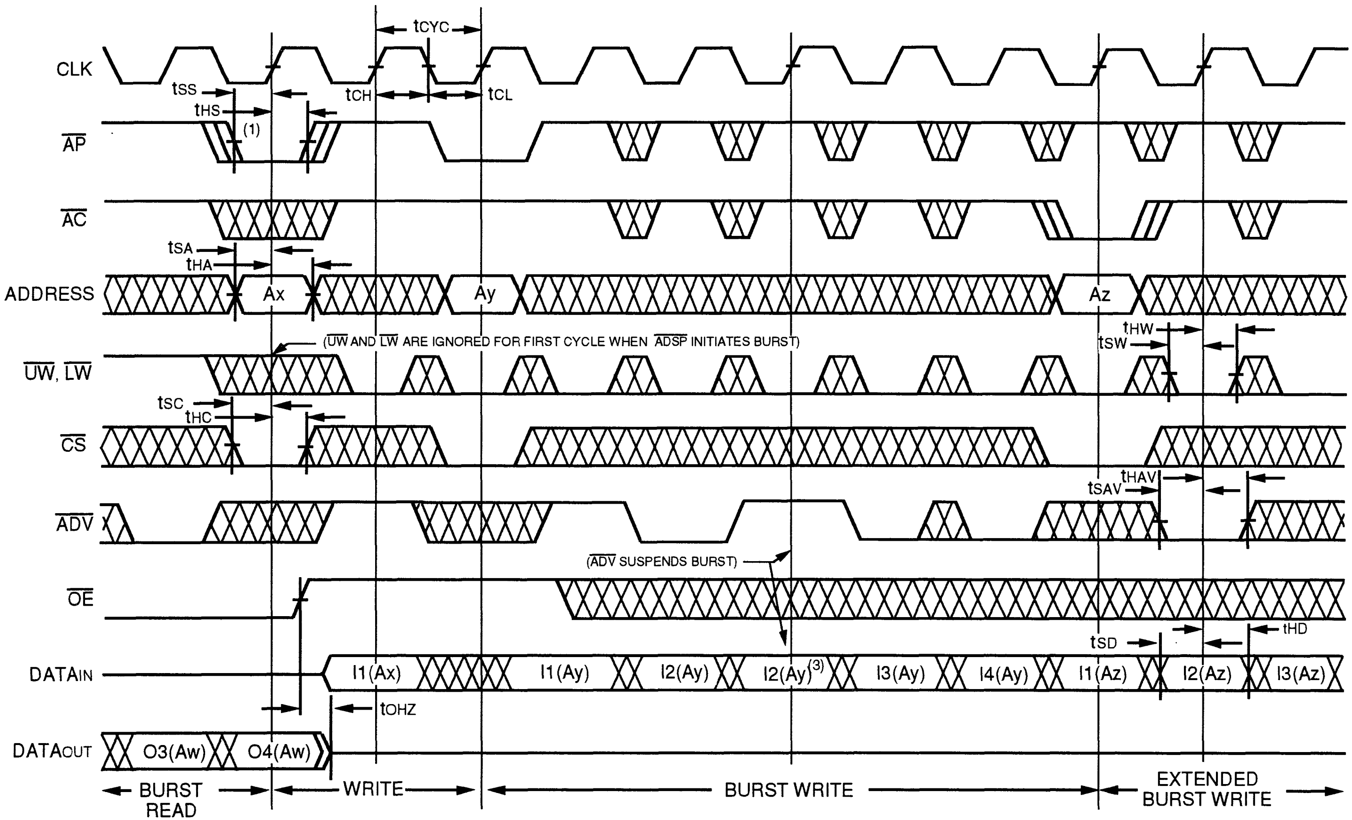


2933 drw 07

NOTES:

1. When $\overline{AP}$ and $\overline{CS}$ are LOW, the device is put into read mode. An $\overline{AP}$ and $\overline{CS}$ initiated write must include one extra clock cycle between $\overline{AP}$ sampled LOW and the first write operation. $\overline{AC}$ can initiate either a read or a write cycle without requiring an additional clock cycle between $\overline{AC}$ being sampled LOW and the first read or write operation.
2. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing sub-locally for the four word burst.

WRITE CYCLES (2)

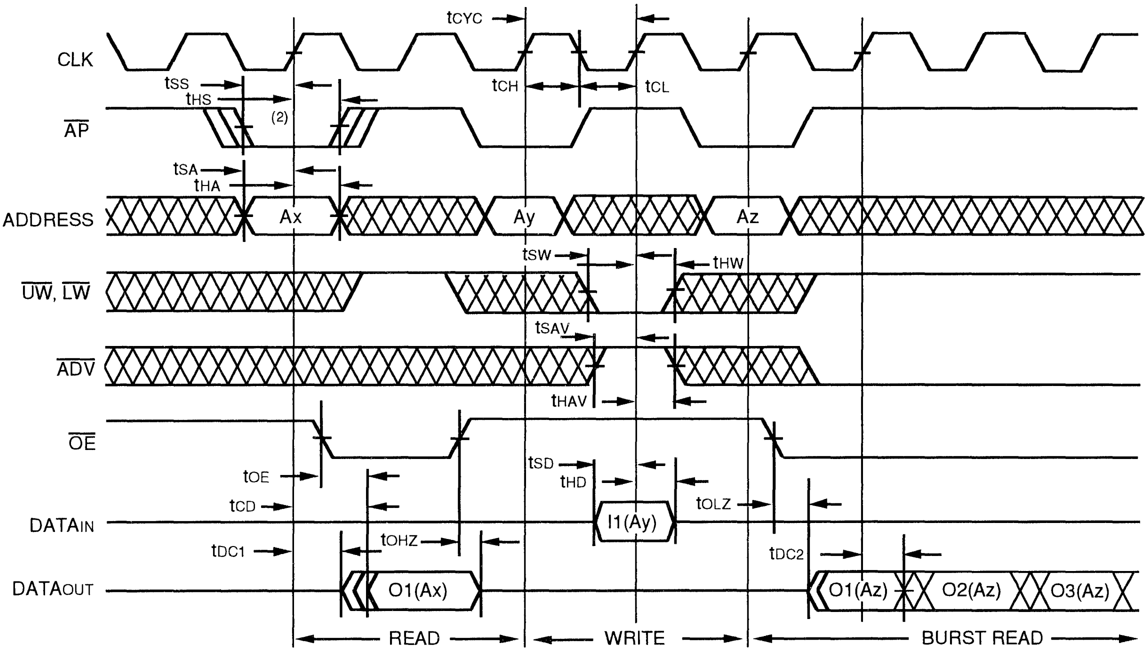


2933 drw 08

NOTES:

1. When $\overline{AP}$ and $\overline{CS}$ are LOW, the device is put into read mode. An $\overline{AP}$ and $\overline{CS}$ intiated write must include one extra clock cycle between $\overline{AP}$ sampled LOW and the first write operation. $\overline{AC}$ can initiate either a read cycle or a write cycle without requiring an additional clock cycle between $\overline{AC}$ being sampled LOW and the first read or write operation.
2. O3 (Aw) represents the third output from the external address Aw previously loaded, and O4 (Aw) represents the fourth and last of the Burst outputs from the external address Aw. I1 (Ax) represents the first input to the external address Ax. I1 (Ay) represents the first input from the external address Ay; I2 (Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing sub-locally for the four word burst.
3. $\overline{ADV}$ = HIGH on rising edge of CLK suspends the count advance which allows wait states to be added. During the wait state the previously written data may be modified (rewritten with new data).

COMBINATION READ/WRITE CYCLE (1,3)

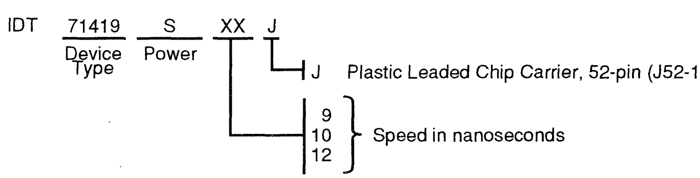


2933 drw 09

NOTES:.

1. I1 (Ay) represents the first input to the external address Ay. O1 (Az) represents the first output from the external address Az, O2 (Az) represents the next output data in the burst sequence of the base address Az.
2. $\overline{AP}$ and $\overline{AC}$ are active LOW signals which allow registering of the address bits. $\overline{AP}$ blocks the write (when either $\overline{UW}$ or $\overline{LW}$ is LOW) whereas $\overline{AC}$ does not. The first burst cycle of the back-to-back cycles requires the standard 2:1:1:1 clocking, the subsequent burst cycles may realize a 1:1:1:1 clock count using the last clock of the first burst cycle for the address status of the next burst cycle. Back-to-back read cycles may be initiated by either $\overline{AP}$ or $\overline{AC}$. Back-to-back writes may only be initiated by $\overline{AC}$.
3. $\overline{CS}$ = LOW, $\overline{AC}$ = HIGH.

ORDERING INFORMATION



2933 drw 10

10

Integrated Device Technology, Inc.

32K x 18 CacheRAM™ BURST COUNTER & SELF-TIMED WRITE — FOR THE PENTIUM™ PROCESSOR

PRELIMINARY
IDT71420

FEATURES:

- 32K x 18 architecture
- Fast clock-to-data access times: 9, 10, 12 ns
- Internal burst read and write address counter
- Processor Burst Pipelining is permitted via Chip Select gating $\overline{\text{ADSP}}$
- Internal input registers (data and control)
- Internal address registers
- Self-timed write cycle
- Single 5V power supply
- Regulated I/Os are 3.3V LVTTL Compatible
- Complies with all timing and signals of the Pentium processor
- Packaged in a JEDEC Standard 52-pin plastic leaded chip carrier (PLCC)

DESCRIPTION:

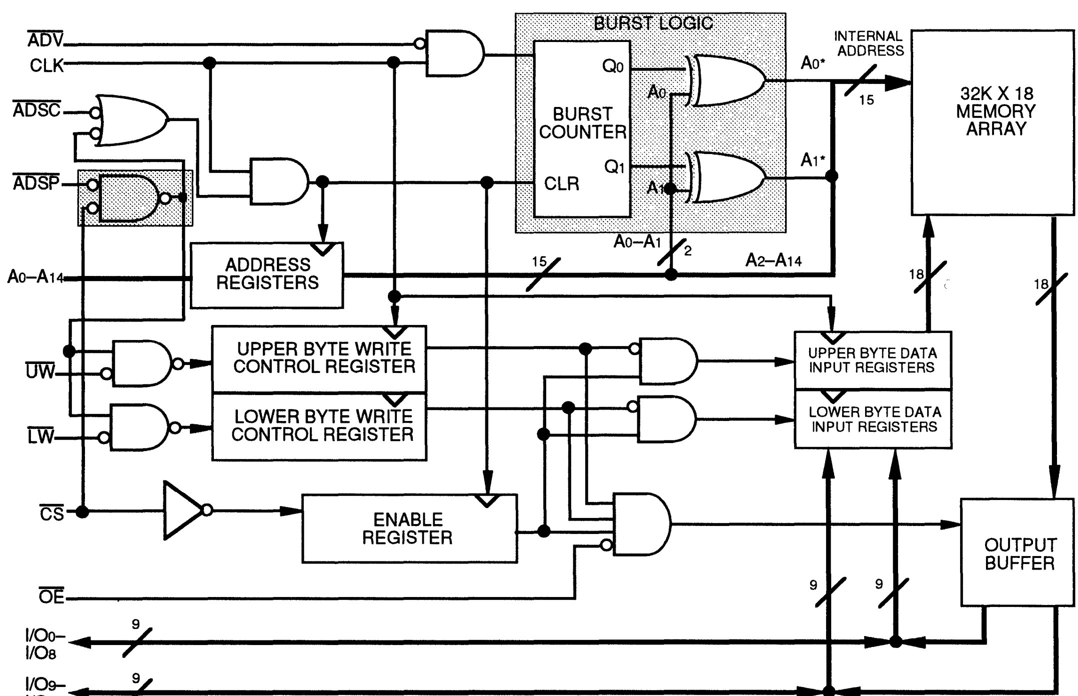
The IDT71420 is a high-speed 32K x 18-bit static RAM with full on-chip hardware support of the Pentium processor interface. This part is designed to facilitate the implementation of the highest-performance secondary caches while using either available cache-tag SRAMs and PALs or chipsets for the Pentium processor.

The IDT71420 CacheRAM contains a full set of write, data, address, and control registers. Internal logic allows the processor to generate a self-timed write based upon a decision which can be left until the extreme end of the write cycle.

An internal burst address counter accepts the first cycle address from the processor, then cycles through the adjacent three locations using the Pentium burst refill sequence, on appropriate rising edges of the system clock.

Fabricated using IDT's BiCMOS high-performance submicron technology, this device offers a maximum clock-to-data access time as fast as 9ns, while requiring an address setup of only 2.5ns.

FUNCTIONAL BLOCK DIAGRAM



2934 drw 01

The IDT logo is a registered trademark and CacheRAM is a trademark of Integrated Device Technology
Pentium is a trademark of Intel Corp.

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DESCRIPTION (CONTINUED)

The IDT71420 CacheRAM is packaged in a JEDEC Standard 52-pin plastic leaded chip carrier (PLCC).

FUNCTIONALITY

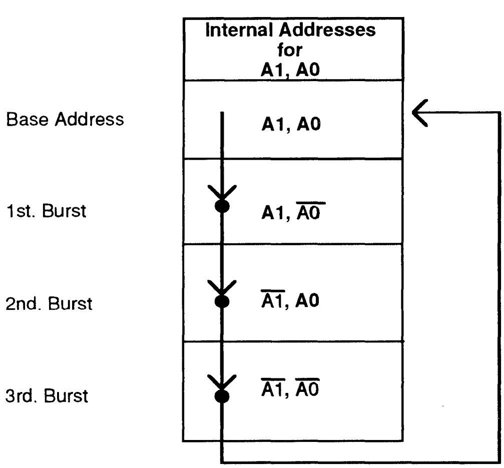
The IDT71420 is synchronous and has an internal burst counter. The synchronous functionality eases cache controller design, while the internal burst counter simplifies implementation of burst accesses.

The registered address, data-in, and write control inputs of the IDT71420 allow for synchronous write operation. To perform a write the inputs must be valid at the rising edge of clock while meeting specified setup and hold times. This write requirement simplifies cache controller design by not requiring the write control pulse needed by asynchronous SRAMs.

A two-bit internal burst counter is used to generate the appropriate internal addresses for A0 and A1 needed for burst accesses. The burst counter starts at the base address defined by the external addresses A0 and A1. Once loaded, the internal addresses are cycled through by keeping $\overline{ADV}$ LOW at the rising edge of clock. $\overline{ADV}$ HIGH at the rising edge of clock stops the advance of the burst counter and suspends the burst sequence.

Address pipelining can be achieved by using $\overline{CS}$ (a controller input to the IDT71420) to block premature assertions of $\overline{ADSP}$ (a CPU input to the IDT71420). The cache controller can request a new address from the CPU and block $\overline{ADSP}$ to the IDT71420 using $\overline{CS}$ HIGH so the new address is not loaded immediately. The controller can assert $\overline{ADSC}$ later to load in the new address at the appropriate time.

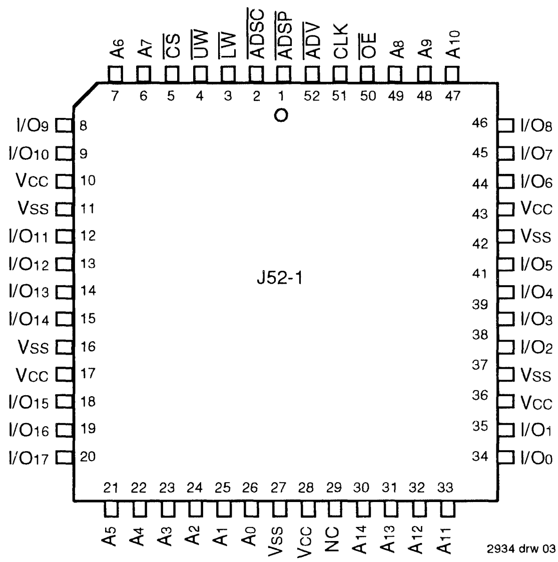
Powering up the IDT71420 is accomplished by keeping $\overline{ADSP}$ or $\overline{ADSC}$ LOW with $\overline{CS}$ LOW at rising edge of clock. Powering down the IDT71420 is accomplished by keeping $\overline{ADSC}$ LOW with $\overline{CS}$ HIGH at rising edge of clock.



Burst Sequence for Internal Burst Counter

2934 drw 02

PIN CONFIGURATION



2934 drw 03

PLCC TOP VIEW

PIN NAMES

A0 – A14	Address Inputs
CLK	Clock
$\overline{UW}$, $\overline{LW}$	Upper, Lower Byte Write Enables
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
$\overline{ADV}$	Burst Address Advance
$\overline{ADSP}$, $\overline{ADSC}$	Address Status (Processor & Cache Controller)
I/O0 – I/O17	Data Input/Output
VCC	+5V Power
VSS	Ground

2934 tbl 01

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
V_{SS}	Supply Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.0	V_{CC}+0.5	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2934 tbl 06

1. V_{IL} (min.) = –1.5V for pulse width of less than 10ns, once per cycle, for $I \leq 20mA$.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 5%

2934 tbl 05

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SYNCHRONOUS TRUTH TABLE(1, 2, 3)

$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{UW}+\overline{LW}$	CLK	Address	Operation
H	X	L	X	X	↑	N/A	Deselected, Power Down
H	L	H	X(4)	X(4)	↑	N/A	Address Input Ignored(4,5)
L	L	X	X	X	↑	External Address	Read Cycle, Begin Burst(6)
L	H	L	X	L	↑	External Address	Write Cycle, Begin Burst(6)
L	H	L	X	H	↑	External Address	Read Cycle, Begin Burst(6)
X	H	H	L	L	↑	Next Address	Write Cycle, Continue Burst(5)
X	H	H	L	H	↑	Next Address	Read Cycle, Continue Burst(5)
X	H	H	H	L	↑	Current Address	Rewrite Cycle, Suspend Burst(5)
X	H	H	H	H	↑	Current Address	Read Cycle, Suspend Burst(5)

NOTES: 2934 tbl 02
1. L = V_{IL}, H = V_{IH}, ↑ = CLK LOW-to-HIGH transition,X = Don't Care.
2. All inputs except $\overline{OE}$ must meet setup and hold times for the LOW-to-HIGH transition of CLK; $\overline{OE}$ operates asynchronously.
3. Wait states can be inserted by suspending a burst sequence, ie. $\overline{ADV}$ = HIGH clocked in by a CLK LOW-to-HIGH transition.
4. $\overline{CS}$ gates $\overline{ADSP}$ when $\overline{CS}$ = HIGH. Mode is used for address pipelining. Address input registers remain unchanged until either $\overline{ADSC}$ and $\overline{CS}$ or $\overline{ADSP}$ and $\overline{CS}$ are sampled LOW simultaneously. Other functionality of the device remains unchanged, i.e. $\overline{ADV}$ advances the burst counter, $\overline{UW}+\overline{LW}$ determines Read or Write status.
5. If the device is already powered down, it will remain powered down.
6. If the device is powered down, it will power up.

ASYNCHRONOUS TRUTH TABLE(1, 2)

Operation	$\overline{OE}$	I/O Status
Read	L	Data Out ($I/O_0 - I/O_{17}$)
Read	H	High-Z
Write	X	High-Z — Data In ($I/O_0 - I/O_{17}$)
Deselected	X	High-Z

NOTES: 2934 tbl 03
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.

CAPACITANCE

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 3dV	7	pF

NOTE: 2934 tbl 09
1. This parameter is determined by device characterization, but is not production tested.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0(2)	V
T_A	Operating Temperature	–0 to +70	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.7	W
I_{OUT}	DC Output Current	30	mA

NOTES: 2934 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.
2. V_{IN} and $V_{I/O}$ should not exceed Vcc+0.5V. All other pins should not exceed 7.0V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC}= Max., V_{IN} = 0V to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS} \geq V_{IH}$, $\overline{OE} \geq V_{IH}$, V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	5	µA
V_{OL}	Output Low Voltage (I/O_0–I/O_{17})	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage($I/O_0 - I/O_{17}$)	I_{OH} = –4mA, V_{CC} = Min.	2.4	3.3	V

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1, 4) (V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Condition	71420S9 Commercial	71420S10 Commercial	71420S12 Commercial	Unit
I_{CC}	Operating Power Supply Current	$\overline{CS} \le V_{IL}$, $\overline{OE} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	320	310	300	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \ge V_{IH}$, All Inputs $\ge V_{IH}$ or $\le V_{IL}$, V_{CC} = Max., f = f_{MAX}(3)	50	50	50	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \ge V_{HC}$, All Inputs $\ge V_{HC}$ or $\le V_{LC}$, V_{CC} = Max., f = 0(3)	30	30	30	mA

2934 tbl 08

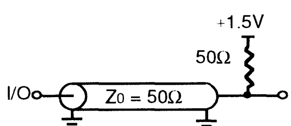
NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, address inputs are cycling at the maximum frequency of read cycles of 1/t_{CYC} while $\overline{ADSC}$ = LOW.
3. At f = f_{MAX}, address inputs are cycling at the maximum frequency of read cycles of 1/t_{CYC} while a $\overline{ADSP}$ and $\overline{ADSC}$ = HIGH and $\overline{ADV}$ = HIGH. f = 0 means no address input lines change, while $\overline{ADSP}$ and $\overline{ADSC}$ = V_{HC} and $\overline{ADV}$ = V_{HC}.
4. V_{HC} = V_{CC} - 0.2V, V_{LC} = 0.2V.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

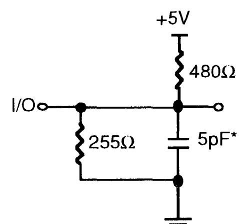
2934 tbl 10

AC TEST LOADS



2934 drw 04

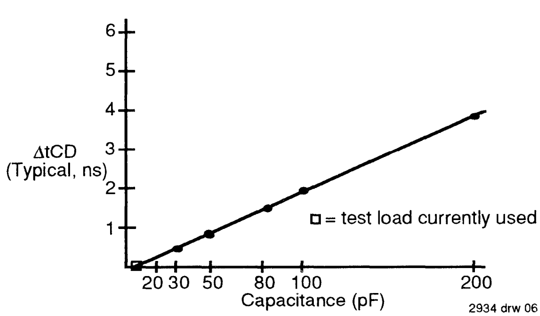
Figure 1. AC Test Load



2934 drw 05

Figure 2. AC Test Load (for t_{OHZ}, t_{CHZ}, t_{OLZ}, and t_{DC1})

* Including scope and jig



2934 drw 06

Figure 3. Lumped Capacitive Load, Typical Derating

10

AC ELECTRICAL CHARACTERISTICS (1, 2, 3, 6)

(V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C)

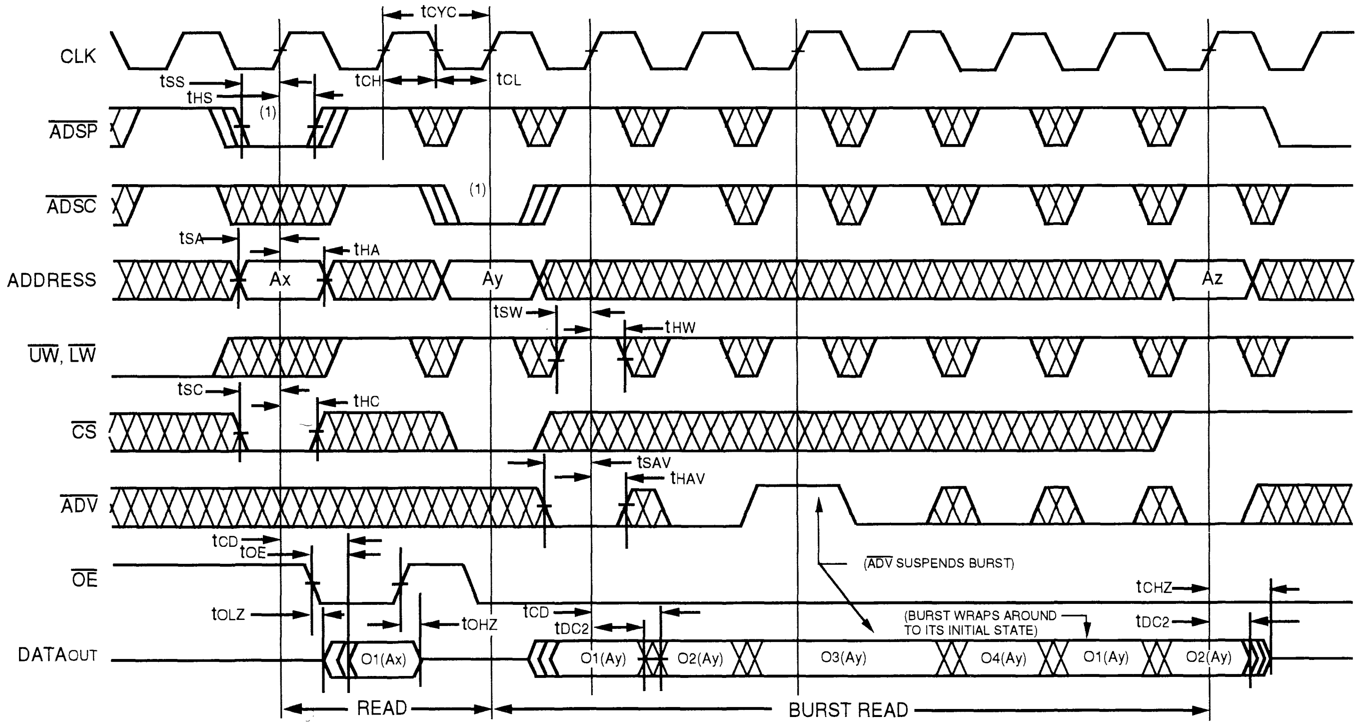
Symbol	Parameter	IDT71420S9 Min.	IDT71420S9 Max.	IDT71420S10 Min.	IDT71420S10 Max.	IDT71420S12 Min.	IDT71420S12 Max.	Unit
t_{CYC}(4)	Cycle Time	15	—	16.6	—	20	—	ns
t_{CD}	Clock Access Time	—	9	—	10	—	12	ns
t_{OE}	Output Enable Access	—	5	—	6	—	7	ns
t_{DC1}(5)	Clock High to Output Active	3	—	3	—	3	—	ns
t_{DC2}	Clock High to Data Change	3	—	3	—	3	—	ns
t_{OLZ}(5)	Output Enable to Data Active	0	—	0	—	0	—	ns
t_{OHZ}(5)	Output Disable to Data High-Z	2	6	2	6	2	7	ns
t_{CHZ}(5)	Clock High to Data High-Z	—	6	—	6	—	6	ns
t_{CH}(7)	Clock High Pulse Width	5	—	5.5	—	6	—	ns
t_{CL}(7)	Clock Low Pulse Width	5	—	5.5	—	6	—	ns
t_{SA}	Address Setup Time	2.5	—	2.5	—	3	—	ns
t_{SS}	Address Status Setup Time	2.5	—	2.5	—	3	—	ns
t_{SD}	Data In Setup Time	2.5	—	2.5	—	3	—	ns
t_{SW}	Write Setup Time	2.5	—	2.5	—	3	—	ns
t_{SAV}	Address Advance Setup Time	2.5	—	2.5	—	3	—	ns
t_{SC}	Chip Select Setup Time	2.5	—	2.5	—	3	—	ns
t_{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HS}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HD}	Data In Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HW}	Write Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HAV}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	ns
t_{HC}	Chip Select Hold Time	0.5	—	0.5	—	0.5	—	ns

2934 tbl 11

NOTES:

1. A read cycle is defined by either $\overline{UW}$ or $\overline{LW}$ = HIGH or $\overline{ADSP}$ and $\overline{CS}$ = LOW. A write cycle is defined by $\overline{CS}$ and either $\overline{UW}$ or $\overline{LW}$ = LOW and $\overline{ADSP}$ = HIGH.
2. All read and write cycle timings are referenced from CLK, or $\overline{OE}$ as it applies.
3. $\overline{OE}$ is a don't care when $\overline{UW}$ or $\overline{LW}$ = LOW is clocked in.
4. Maximum access times are guaranteed from all possible Pentium Processor external bus cycles.
5. Transition is measured ±200mV from steady-state. This parameter is guaranteed by device characterization with the AC Load (Figure 2), but is not production tested.
6. This is a synchronous device. All synchronous inputs must meet the specified setup and hold times for ALL rising edges of CLK. To enable the device, chip select must be active ($\overline{CS}$ = LOW) when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW at rising edge of CLK. The device remains enabled until chip select is inactive ($\overline{CS}$ = HIGH) and $\overline{ADSC}$ is LOW at rising edge of CLK. $\overline{ADSP}$ cannot disable the device because $\overline{CS}$ = HIGH blocks $\overline{ADSP}$ = LOW.
7. This parameter is measured as HIGH above 2.2V and LOW below 0.8V.

READ CYCLES(2)

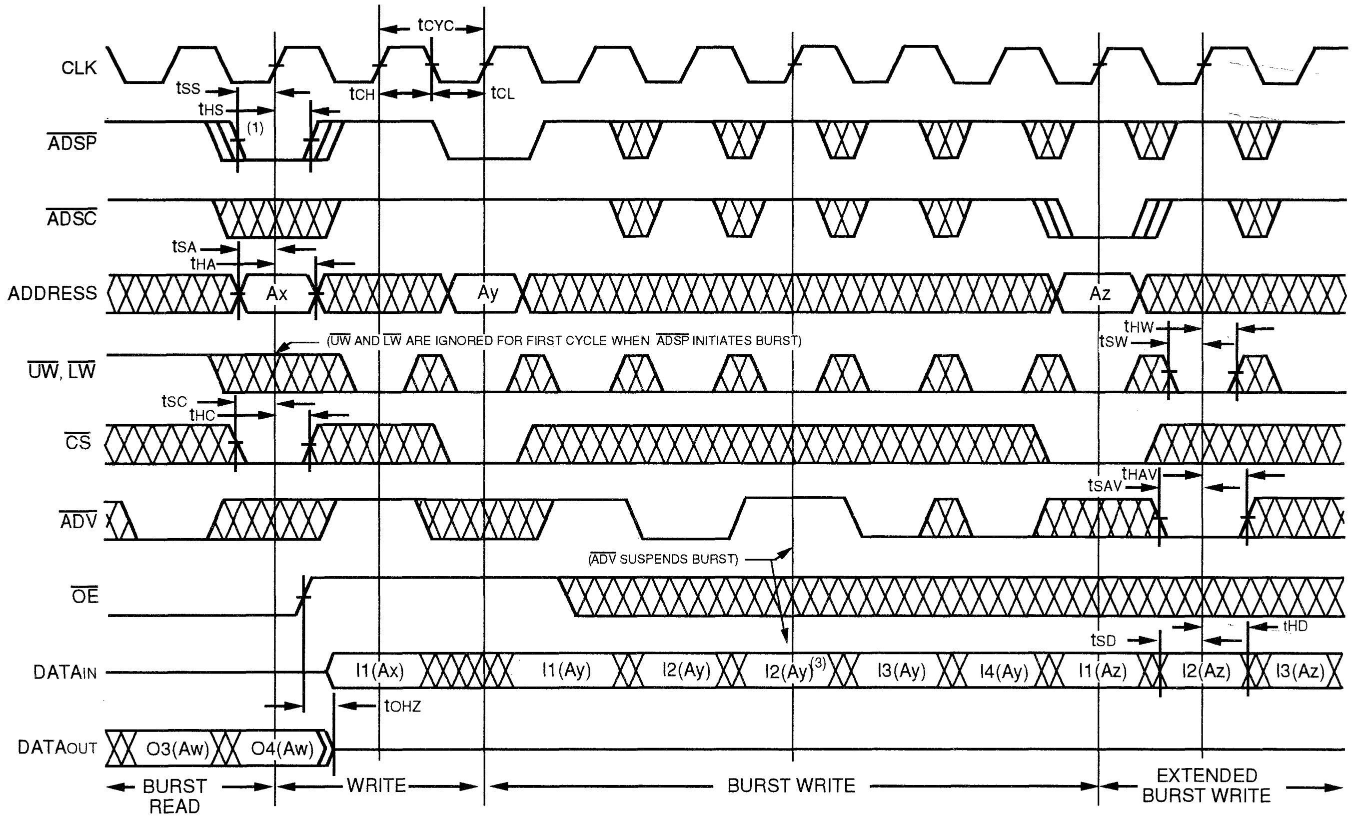


2934 drw 07

NOTES:

1. When $\overline{ADSP}$ and $\overline{CS}$ are LOW, the device is put into read cycle. An $\overline{ADSP}$ and $\overline{CS}$ initiated write must include one extra clock cycle between $\overline{ADSP}$ sampled LOW and the first write operation. $\overline{ADSC}$ can initiate either a read or a write cycle without requiring an additional clock cycle between $\overline{ADSC}$ being sampled LOW and the first read or write operation.
2. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing sub-locally for the four word burst.
3. An $\overline{ADSP}$ initiated cycle requires that both $\overline{ADSP}$ and $\overline{CS}$ be LOW during the rising edge of the clock. $\overline{ADSP}$ gated by $\overline{CS}$ allows the cache controller to block an $\overline{ADSP}$ cycle using $\overline{CS}$ and assert its own $\overline{ADSC}$ cycle.

WRITE CYCLES (2)

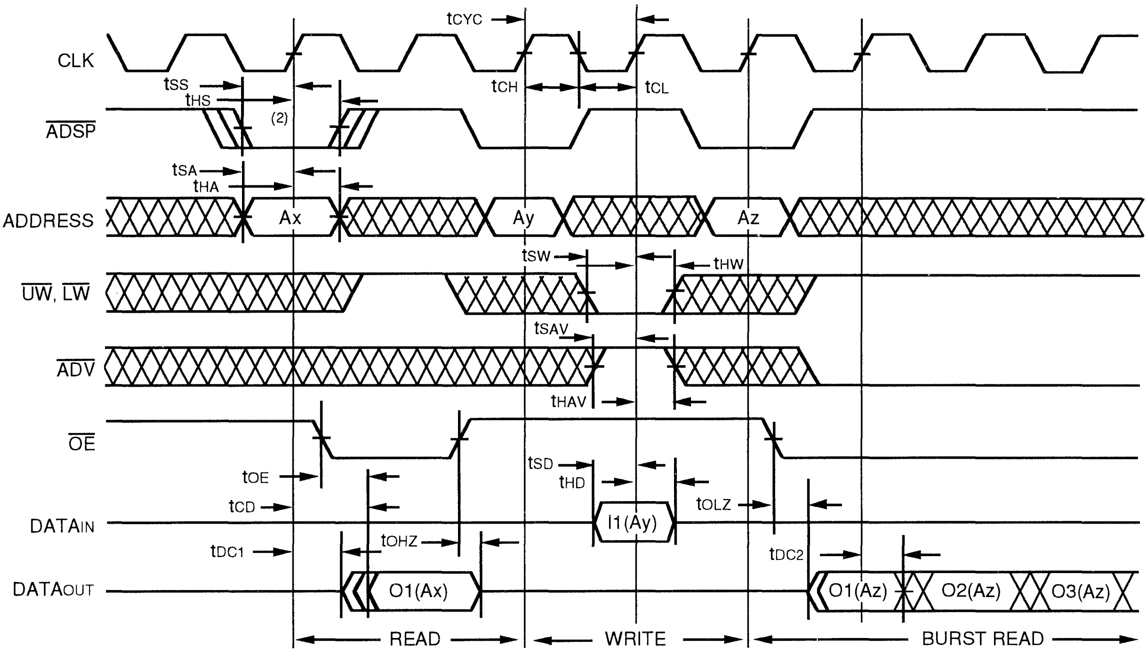


2934 drw 08

NOTES:

1. When $\overline{ADSP}$ and $\overline{CS}$ are LOW, the device is put into read mode. An $\overline{ADSP}$ and $\overline{CS}$ intiated write must include one extra clock cycle between $\overline{ADSP}$ sampled LOW and the first write operation. $\overline{ADSC}$ can initiate either a read cycle or a write cycle without requiring an additional clock cycle between $\overline{ADSC}$ being sampled LOW and the first read or write operation.
2. O3 (Aw) represents the third output from the external address Aw previously loaded, and O4 (Aw) represents the fourth and last of the Burst outputs from the external address Aw. I1 (Ax) represents the first input to the external address Ax. I1 (Ay) represents the first input from the external address Ay; I2 (Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing sub-locally for the four word burst.
3. $\overline{ADV}$ = HIGH on rising edge of CLK suspends the count advance which allows wait states to be added. During the wait state the previously written data may be modified (rewritten with new data).

COMBINATION READ/WRITE CYCLE (1,3)

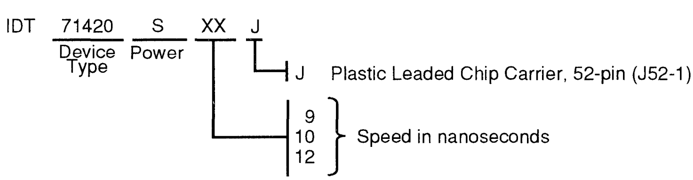


2934 drw 09

NOTES:.

1. I1 (Ay) represents the first input to the external address Ay. O1 (Az) represents the first output from the external address Az, O2 (Az) represents the next output data in the burst sequence of the base address Az.
2. $\overline{ADSP}$ and $\overline{ADSC}$ are active LOW signals which allow registering of the address bits. $\overline{ADSP}$ blocks the write (when either $\overline{UW}$ or $\overline{LW}$ is LOW) whereas $\overline{ADSC}$ does not. The first burst cycle of the back-to-back cycles requires the standard 2:1:1:1 clocking, the subsequent burst cycles may realize a 1:1:1:1 clock count by using the last clock of the first burst cycle for the address status of the next burst cycle. Back-to-back read cycles may be initiated by either $\overline{ADSP}$ or $\overline{ADSC}$. Back-to-back writes may only be initiated by $\overline{ADSC}$.
3. $\overline{CS}$ = LOW, $\overline{ADSC}$ = HIGH.

ORDERING INFORMATION



2934 drw 10

10

Integrated Device Technology, Inc.

32K x 32 CacheRAM™ PIPELINED/FLOW THROUGH OUTPUTS BURST COUNTER, & SELF-TIMED WRITE — FOR PENTIUM™/POWERPC™ PROCESSORS

ADVANCE INFORMATION
IDT71V432

FEATURES:

- 32K x 32 memory configuration
- Pipelined or Flow Through output architecture selected by $\overline{FT}$ input
- Complies with all Pentium and PowerPC timing and interface requirements
- Pentium or PowerPC burst address sequence selected by MODE input
- Self-timed write cycle with byte write, byte write enable and global write controls
- Power down controlled by ZZ input
- Single 3.3V power supply
- Packaged in a JEDEC Standard 100-pin plastic thin quad flatpack (TQFP)

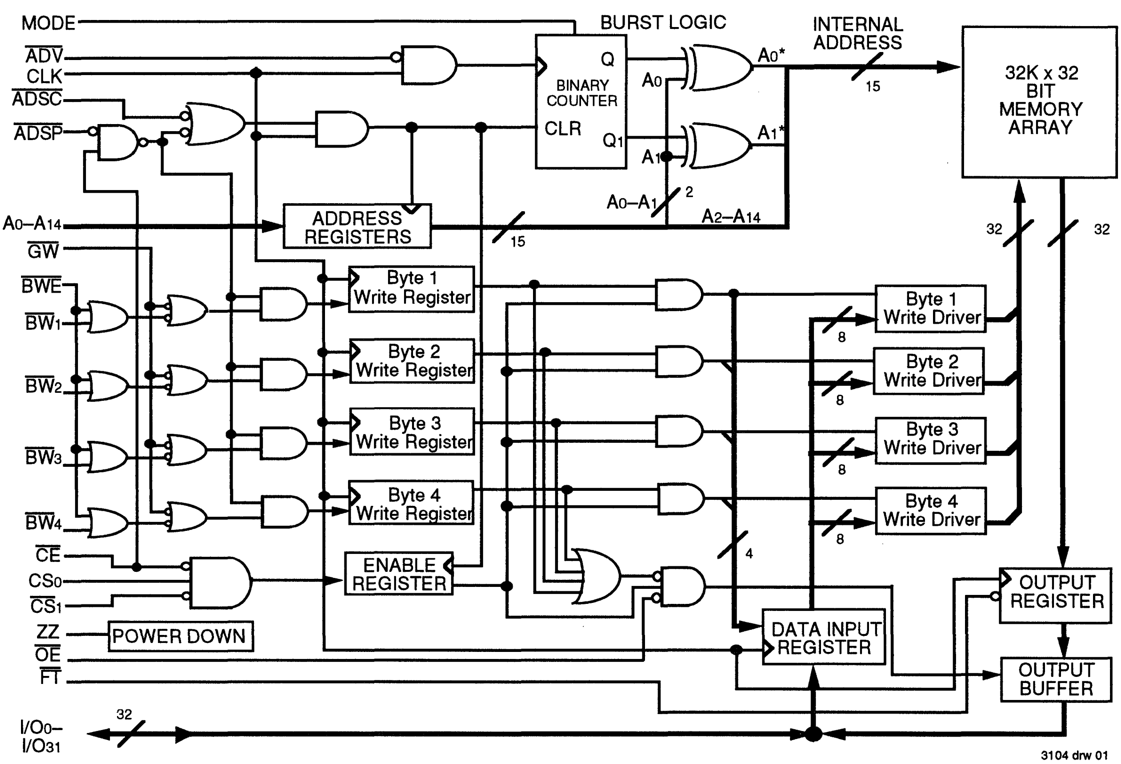
DESCRIPTION:

The IDT71V432 is a 3.3V high-speed 32K x 32-bit static RAM with full on-chip hardware support of the Pentium and PowerPC processor interfaces. The pipelined burst architecture provides cost-effective 3-1-1-1 secondary cache performance for processors up to 66MHz. The optional flow-through burst architecture provides 2-1-1-1 secondary cache performance for processors up to 50 MHz.

The IDT71V432 CacheRAM contains a full set of write, data, address, and control registers. Internal logic allows the processor to generate a self-timed write based upon a decision which can be left until the extreme end of the write cycle.

An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The IDT71V432 provides the first cycle address data and then cycles through the next three address locations.

FUNCTIONAL BLOCK DIAGRAM



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Pentium is a trademark of Intel Corp. PowerPC is a trademark of International Business Machines, Inc.

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DESCRIPTION (CONTINUED)

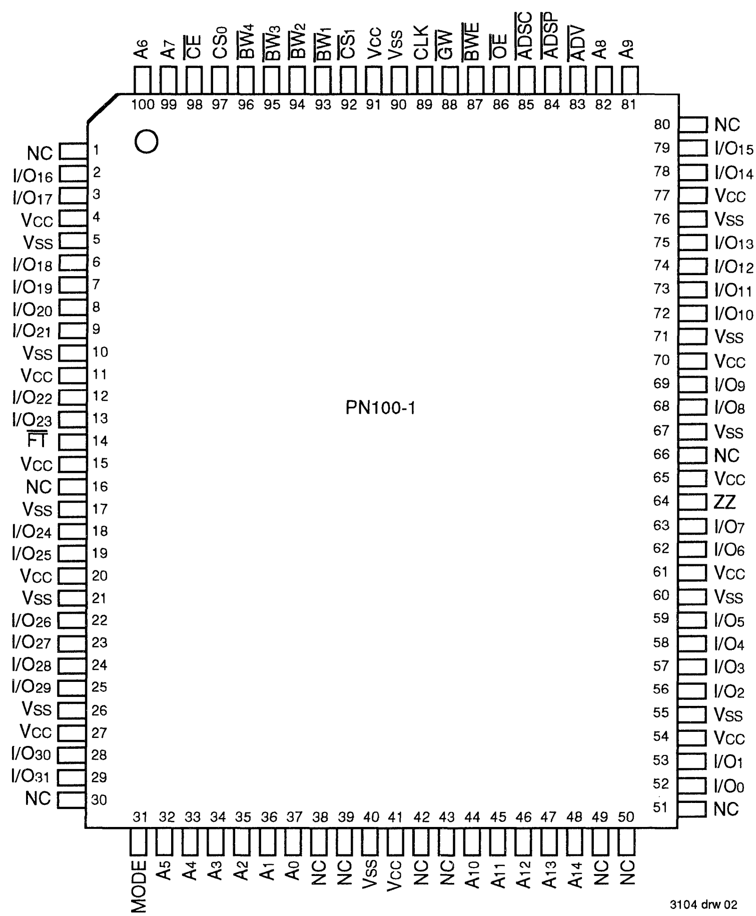
The IDT71V432 CacheRAM utilizes IDT's 3.3V CMOS process to optimize performance in 3.3V applications, and is packaged in a JEDEC Standard 100-pin thin plastic quad flatpack (TQFP) for optimum board density in both desktop and notebook applications.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 5%

3104 tbl 01

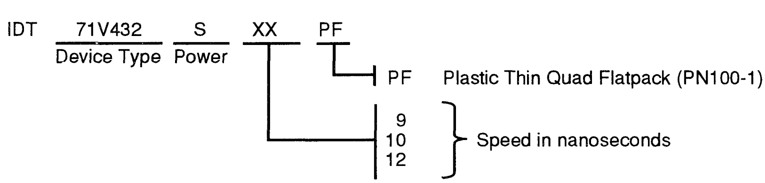
PIN CONFIGURATION



3104 drw 02

**TQFP
TOP VIEW**

ORDERING INFORMATION



3104 drw 03

10

CACHE TAG SRAM PRODUCTS

IDT has been a leader in Cache Tag SRAMs from the beginning, utilizing high-performance technology to perform the comparison function on chip to minimize the cache hit/miss decision time. Both the IDT6178, in CMOS technology, and the IDT71B74, in BiCMOS technology, have been the highest speed cache tags in the industry for their respective densities.

Continuing on with the legacy, new cache tag offerings are introducing features to make the designing of a high-speed secondary cache subsystem even easier. The IDT71215 and IDT71216 both include additional logic and features on chip to offer the designer a straight forward path to zero-wait state cache performance at bus speeds up to 66MHz.

Function	Organization	Features	Process	Part Number	Power	Speeds	
						Commercial	Military
Cache Tag SRAMs	4K x 4	Tag	CMOS	6178	S	10,12,15,20,25	N/A
	8K x 8	Tag	BiCMOS	71B74	S	8,10,12,15,20	N/A
	16K x 15	Intel Tag	BiCMOS	71215	S	10,12	N/A
	16K x 15	PowerPC Tag	BiCMOS	71216	S	10,12	N/A

TABLE OF CONTENTS

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Integrated Device Technology, Inc.

CMOS StaticRAM 16K (4K x 4-BIT) CACHE-TAG RAM

IDT6178S

FEATURES:

- High-speed Address to MATCH Valid time
  - Military: 12/15/20/25ns
  - Commercial: 10/12/15/20/25ns (max.)
- High-speed Address Access time
  - Military: 12/15/20/25ns
  - Commercial: 10/12/15/20/25ns (max.)
- Low-power consumption
  - IDT6178S

  Active: 300mW (typ.)
- Produced with advanced CMOS high-performance technology
- Input and output TTL-compatible
- Standard 22-pin Plastic or Ceramic DIP, 24-pin SOJ
- Military product 100% compliant to MIL-STD-883, Class B

DESCRIPTION:

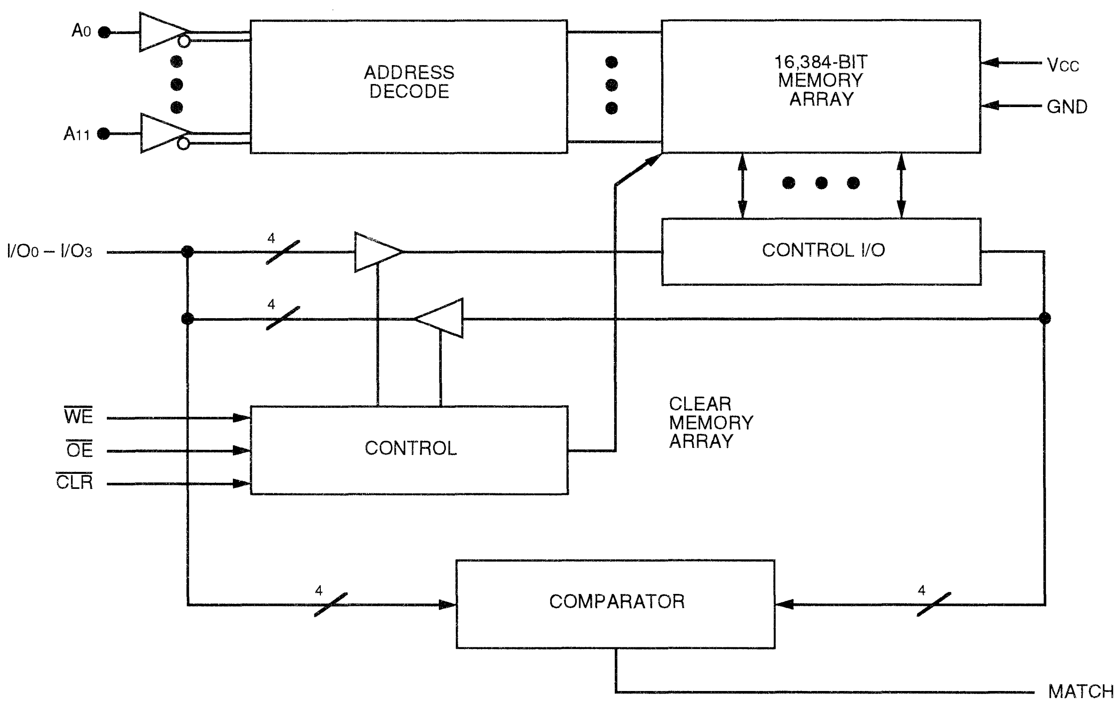
The IDT6178 is a high-speed cache address comparator sub-system consisting of a 16,384-bit StaticRAM organized as 4K x 4. Cycle Time and Address to MATCH Valid are equal. The IDT6178 features an onboard 4-bit comparator that compares RAM contents and current input data. The result is an active HIGH on the MATCH pin. The MATCH pins of several IDT6178s can be handed together to provide enabling or acknowledging signals to the data cache or processor.

The IDT6178 is fabricated using IDT's high-performance, high-reliability CMOS technology. Address to MATCH and Data to MATCH times are as fast as 10ns.

All inputs and outputs of the IDT6178 are TTL-compatible and the device operates from a single 5V supply.

The IDT6178 is packaged in either a 22-pin, 300-mil Plastic or Ceramic DIP package or 24-pin SOJ. Military grade product is manufactured in compliance with latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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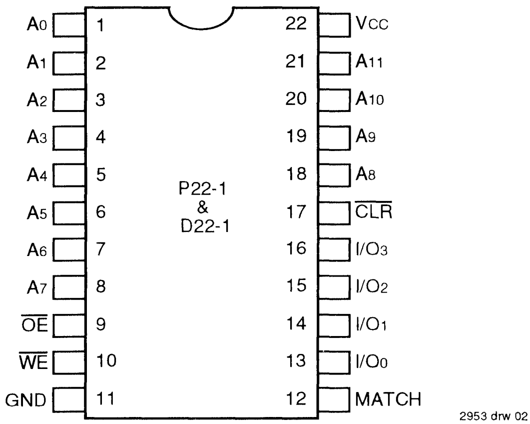
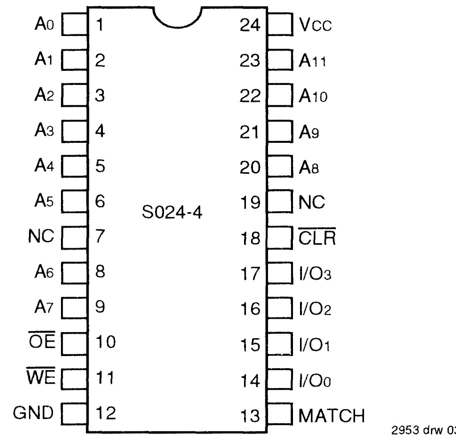
PIN CONFIGURATIONS



DIP TOP VIEW



SOJ TOP VIEW

PIN DESCRIPTIONS

A_0–A_{11}	Address Inputs
I/O_0–I/O_3	Data Input/Output
MATCH	Match
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CLR}$	Clear
V_{CC}	Power
GND	Ground

2953 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE: 2953 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Military	–55°C to +125°C	0V	5.0V ± 10%

2953 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2(2)	–	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	–	0.8	V

NOTES: 2953 tbl 05

1. V_{IL} = –3.0V for pulse width less than 20ns, once per cycle.
2. V_{IH} = 2.5V for clear pin.

TRUTH TABLES(1)

$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	MATCH	Mode
H	H	H	Valid(2)	Match Cycle
L	X	H	Invalid	Write Cycle
H	L	H	Invalid	Read Cycle
X	X	L	Invalid	Clear Cycle

NOTE: 2953 tbl 03

1. H = V_{IH}, L = V_{IL}, X = Don't care.
2. Valid Match = V_{OH}, Valid Non-Match = V_{OL}.

CAPACITANCE (T_A = 25°C, f = 1MHz)

Symbol	Parameter	Condition	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2953 tbl 06

1. This parameter is determined by device characterization, but is not production tested.

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DC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	Test Condition	6178S Min.	6178S Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{OE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA (I/O0 – I/O3)	—	0.4	V
		I_{OL} = 10mA (I/O0 – I/O3)	—	0.5	V
		I_{OL} = 16mA (Match)	—	0.4	V
		I_{OL} = 20mA (Match)	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = –4mA (I/O0 – I/O3)	2.4	—	V
		I_{OH} = –8mA (Match)	2.4	—	V

2953 tbl 07

DC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter		6178S10 Max.	6178S12(1) Max.	6178S15(1) Max.	6178S20/25 Max.	Unit
I_{CC1}	Operating Power Supply Current Outputs Open, V_{CC} = Max., f = 0(2)	COM'L.	90	90	90	90	mA
		MIL.	—	110	110	110	mA
I_{CC2}	Dynamic Operating Current Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	COM'L.	180	160	140	140	mA
		MIL.	—	180	160	160	mA

NOTES:

2953 tbl 08

1. Military values are preliminary only.
2. f_{MAX} = 1/t_{RC}, only address inputs are cycling at f_{MAX}. f = 0 means no address inputs change.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 2 and 3
AC Test Load for Match Cycle	See Figure 1

2953 tbl 09

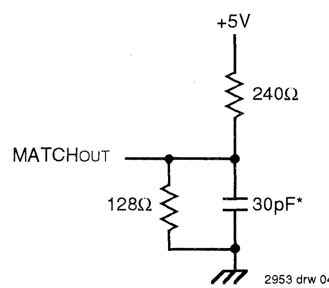


Figure 1. AC Test Load for MATCH

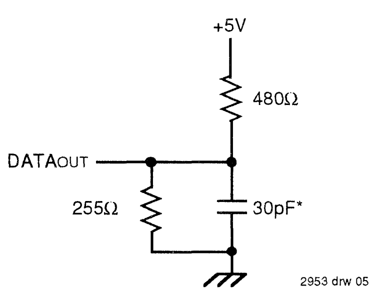


Figure 2. AC Test Load

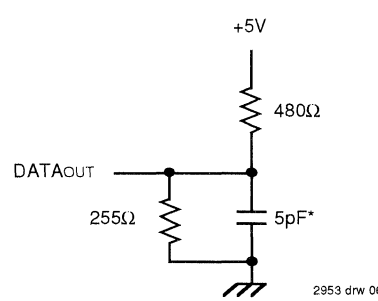


Figure 3. AC Test Load (for t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{OW})

* Including scope and jig.

CYCLE DESCRIPTION

Match Cycle: A match cycle occurs when all control signals ($\overline{OE}$, $\overline{WE}$, $\overline{CLR}$) are HIGH. At that time, data supplied to the RAM on the I/O pins is compared with the data stored at the specified address. The totem-pole match output is HIGH when there is a match at all data bits, and drives LOW if there is not a match.

Write Cycle: The write cycle is conventional, occuring when $\overline{WE}$ is LOW and $\overline{CLR}$ is HIGH. $\overline{OE}$ may be either HIGH or LOW, since it is overridden by $\overline{WE}$. The state of the Match pin is not guaranteed, but in the current implementation it continues to reflect the output of the comparator. The Match pin goes HIGH during write cycles since the data at the specified address is the same as the data (being written) at the I/Os of the RAM.

Read Cycle: When $\overline{WE}$ and $\overline{CLR}$ are HIGH and $\overline{OE}$ is LOW, the RAM is in a read cycle. The state of the Match pin is not guaranteed, but in the current implementation it continues to reflect the output of the comparator. The Match pin goes HIGH during read cycles since the data at the specified address is the same as the data (being read) at the I/Os of the RAM.

Clear Cycle: When $\overline{CLR}$ is asserted, every bit in the RAM is cleared to zero. If $\overline{OE}$ is LOW during a clear cycle, the RAM I/Os will be driven. However, this data is not necessarily zeros, even after a considerable time. The Match pin is enabled, but its state is not predicable.

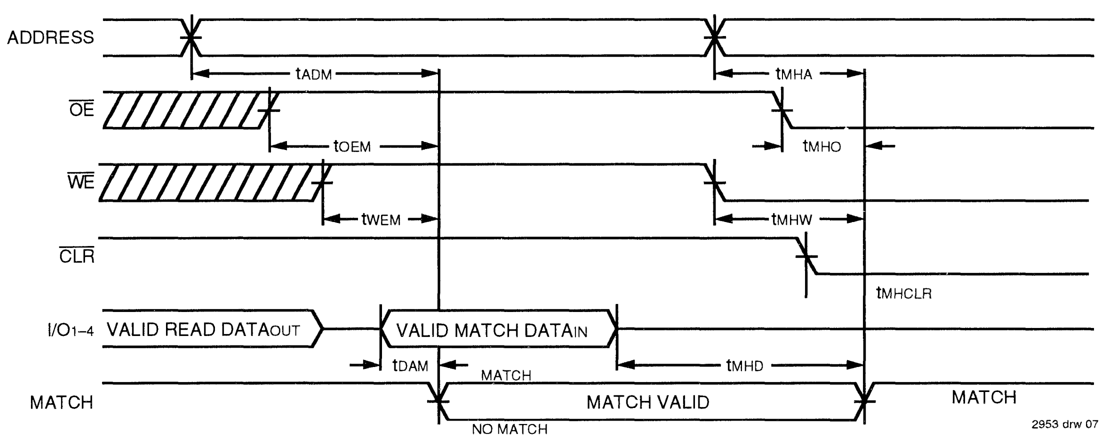
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

		6178S10(1)		6178S12		6178S15		6178S20		6178S25		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Match Cycle												
t_{ADM}	Address to Match Valid	—	10	—	12	—	15	—	20	—	25	ns
t_{DAM}	Data Input to Match Valid	—	8	—	11	—	13	—	15	—	15	ns
t_{MHO}	Match Valid Hold from $\overline{OE}$	0	—	0	—	0	—	0	—	0	—	ns
t_{OEM}	$\overline{OE}$ HIGH to Match Valid	—	10	—	12	—	15	—	20	—	20	ns
t_{MHW}	Match Valid Hold from $\overline{WE}$	0	—	0	—	0	—	0	—	0	—	ns
t_{WEM}	$\overline{WE}$ HIGH to Match Valid	—	10	—	12	—	15	—	20	—	20	ns
t_{MHCLR}	Match Valid Hold from $\overline{CLR}$	0	—	0	—	0	—	0	—	0	—	ns
t_{MHA}	Match Valid Hold from Address	3	—	3	—	3	—	3	—	3	—	ns
t_{MHD}	Match Valid Hold from Data	3	—	3	—	3	—	3	—	3	—	ns

NOTE:
1. 0°C to +70°C temperature range only.

2953 tbl 10

TIMING WAVEFORM OF MATCH CYCLE(1)



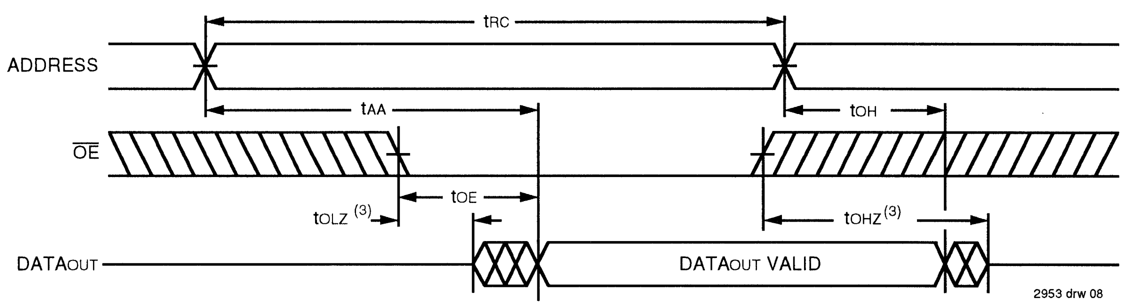
NOTE:
1. It is not recommended to let address and data input pins float while MATCH pin is active.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

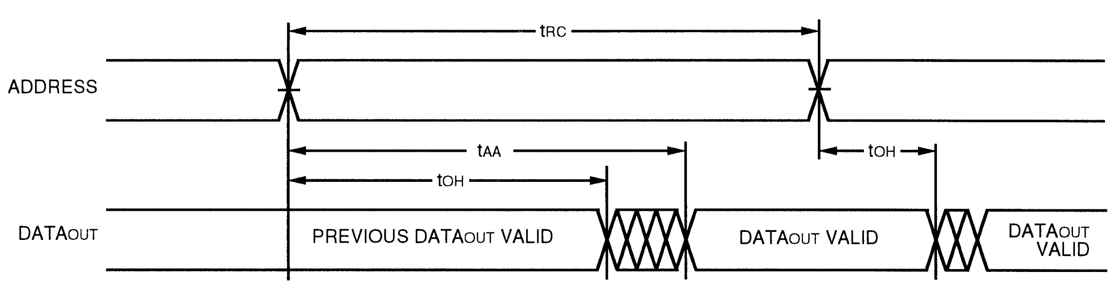
Symbol	Parameter	6178S10[1] Min.	6178S10[1] Max.	6178S12 Min.	6178S12 Max.	6178S15 Min.	6178S15 Max.	6178S20/25 Min.	6178S20/25 Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	10	—	12	—	15	—	20/25	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	20/25	ns
t_{OE}	Output Enable Access Time	—	7	—	8	—	10	—	15	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{OLZ}[2]	Output Enable to Output in Low-Z Time	2	—	2	—	2	—	2	—	ns
t_{OHZ}[2]	Output Disable to Output in High-Z Time	—	6	—	7	—	9	—	12	ns

NOTES: 2953 tbl 11
1. 0°C to +70°C temperature range only.
2. This parameter guaranteed with AC load (Figure 3) by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



TIMING WAVEFORM OF READ CYCLE NO. 2[1,2]



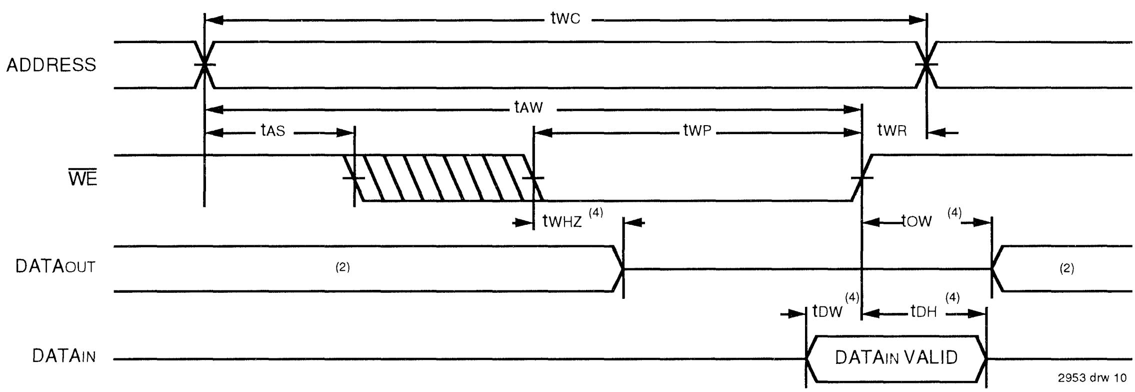
NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Output enable is continuously active, $\overline{OE}$ is LOW.
3. Transition is measured ±200V from steady state.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

		6178S10(1)		6178S12		6178S15		6178S20/25		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Write Cycle										
tWC	Write Cycle Time	10	—	12	—	15	—	20	—	ns
tAW	Address Valid to End-of-Write	8	—	10	—	12	—	14	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	8	—	10	—	12	—	14	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	6	—	8	—	10	—	12	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
tWHZ(2)	Write Enable to Output in High-Z	—	5	—	6	—	7	—	9	ns
tOW(2)	Output Active from End-of-Write	0	—	0	—	0	—	0	—	ns

NOTES: 2953 tbl 12
1. 0°C to +70°C temperature range only.
2. This parameter guaranteed with AC load (Figure 3) by device characterization, but is not production tested.

TIMING WAVEFORM OF WRITE CYCLE(1,3)



NOTES:
1. $\overline{WE}$ must be HIGH during all address transitions.
2. During this period, I/O pins are in the output state and the input signals must not be applied.
3. $\overline{OE}$ is HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the greater of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse is the specified tWP.
4. Transition is measured ±200mV from steady state.

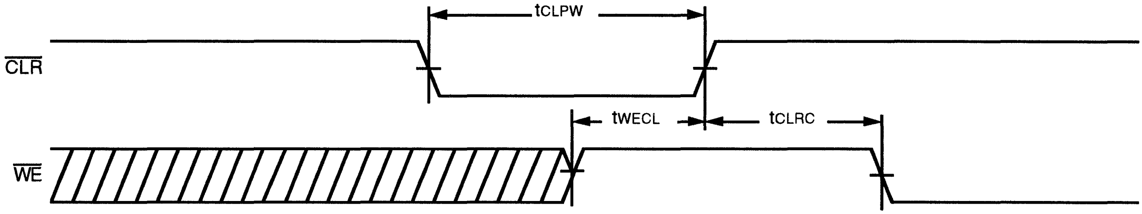
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

		6178S10(1)		6178S12		6178S15		6178S20/25		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Clear Cycle										
tCLPW(2)	$\overline{CLR}$ Pulse Width	12	—	15	—	20	—	25	—	ns
tCLRC	$\overline{CLR}$ HIGH to $\overline{WE}$ LOW	5	—	5	—	5	—	5	—	ns
tPOCL(3)	Power on Reset	50	—	60	—	80	—	100	—	ns
tWECL	$\overline{WE}$ HIGH to Clear HIGH	5	—	5	—	5	—	5	—	ns

NOTES: 2953 tbl 13
1. 0°C to +70°C temperature range only.
2. Recommended duty cycle of 10% maximum.
3. This parameter guaranteed with AC load (Figure 3) by device characterization, but is not production tested.

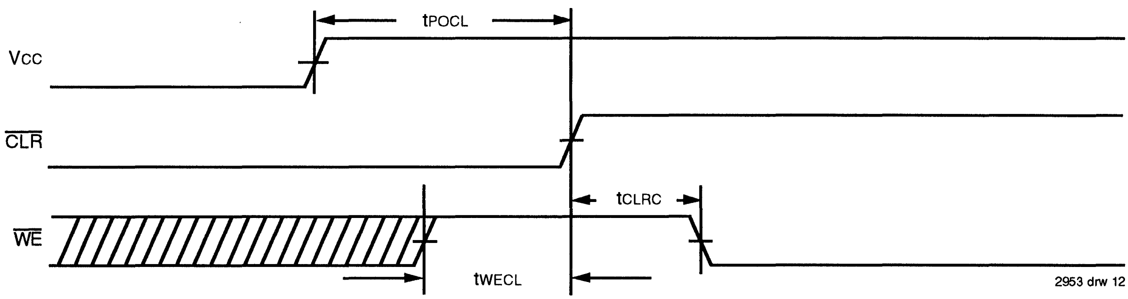
11

TIMING WAVEFORM OF CLEAR CYCLE



2953 drw 11

POWER ON RESET TIMING



2953 drw 12

ORDERING INFORMATION

IDT 6178 S XX X X

- 6178 — Device Type
- S — Power
- XX — Speed
- X — Package
- X — Process/ Temperature

Process/Temperature:
- Blank — Commercial (0°C to +70°C)
- B — Military (–55°C to +125°C, Compliant to MIL-STD-883, Class B)

Package:
- P — 300 mil Plastic DIP (P22-1)
- Y — 300 mil Small Outline, J bend (SO24-4)
- D — 300 mil Ceramic DIP (D22-1)

Speed (Speed in nanoseconds):
- 10 — Commercial only
- 12
- 15
- 20
- 25

2953 drw 13

Integrated Device Technology, Inc.

BiCMOS STATIC RAM 64K (8K x 8-BIT) CACHE-TAG RAM

IDT71B74

FEATURES:

- High-speed address to MATCH comparison time
  - Commercial: 8/10/12/15/20ns (max.)
- High-speed address access time
  - Commercial: 8/10/12/15/20ns (max.)
- High-speed chip select access time
  - Commercial: 6/7/8/10ns (max.)
- Power-ON Reset Capability
- Low power consumption
  - 830mW (typ.) for 12ns parts
  - 880mW (typ.) for 10ns parts
  - 920mW (typ.) for 8ns parts
- Produced with advanced BiCMOS high-performance technology
- Input and output directly TTL-compatible
- Standard 28-pin plastic DIP and 28-pin SOJ (300 mil)

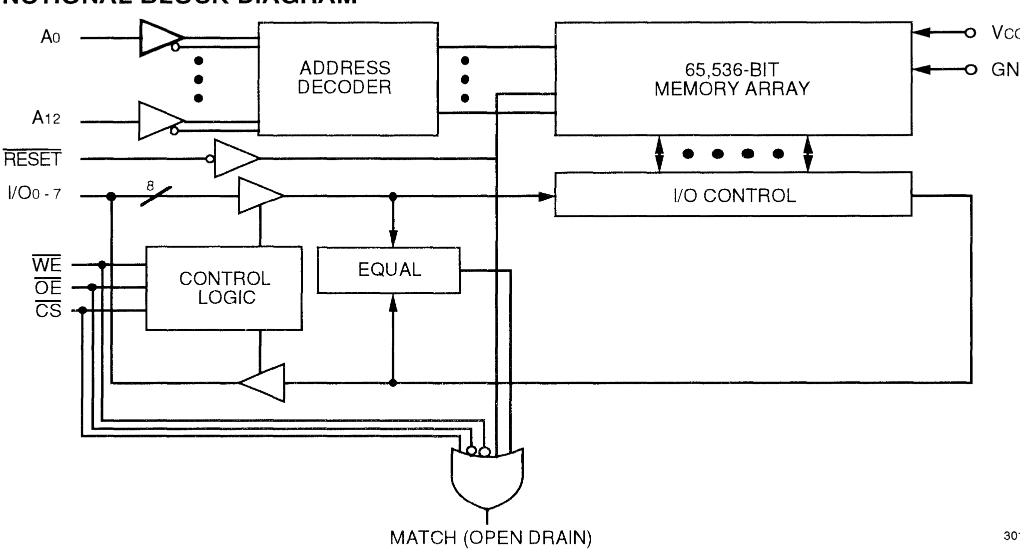
DESCRIPTION:

The IDT71B74 is a high-speed cache address comparator subsystem consisting of a 65,536-bit static RAM organized as 8K x 8 and an 8-bit comparator. A single IDT71B74 can map 8K cache words into a 2 megabyte address space by using the 21 bits of address organized with the 13 LSBs for the cache address bits and the 8 higher bits for cache data bits. Two IDT71B74s can be combined to provide 29 bits of address comparison, etc. The IDT71B74 also provides a single RAM clear control, which clears all words in the internal RAM to zero when activated. This allows the tag bits for all locations to be cleared at power-on or system-reset, a requirement for cache comparator systems. The IDT71B74 can also be used as a resettable 8K x 8 high-speed static RAM.

The IDT71B74 is fabricated using IDT's high-performance, high-reliability BiCMOS technology. Address access times as fast as 8ns, chip select times of 6ns and address-to-match times of 8ns are available.

The MATCH pin of several IDT71B74s can be wired-ORed together to provide enabling or acknowledging signals to the data cache or processor, thus eliminating logic delays and increasing system throughput.

FUNCTIONAL BLOCK DIAGRAM



3013 drw 01

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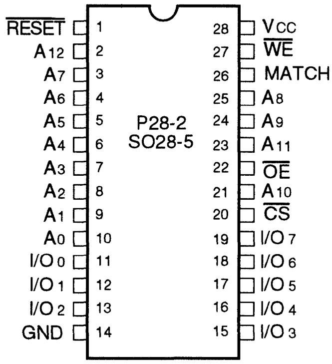
PIN CONFIGURATION



3013 drw 02

DIP/SOJ
TOP VIEW

TRUTH TABLE[1, 2]

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	$\overline{RESET}$	MATCH	I/O	Function
X	X	X	L	HIGH	—	Reset all bits to LOW
X	H	X	H	HIGH	Hi-Z	Deselect chip
H	L	H	H	LOW	D_{IN}	No MATCH
H	L	H	H	HIGH	D_{IN}	MATCH
H	L	L	H	HIGH	D_{OUT}	Read
L	L	X	H	HIGH	D_{IN}	Write

NOTES: 3013 tbl 01
1. H = V_{IH}, L = V_{IL}, X = DON'T CARE
2. HIGH = High-Z (pulled up by an external resistor), and LOW = V_{OL}.

PIN DESCRIPTIONS

Pin Names	Description
A_{0-12}	Address
I/O_{0-7}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{RESET}$	Memory Reset
MATCH	Data/Memory Match (Open Drain)
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
V_{CC}	Power

3013 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTES: 3013 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ Package)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	7	pF

NOTE: 3013 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}[1]	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input HIGH Voltage[2]	2.2	—	6.0[5]	V
V_{IHR}	$\overline{\text{RESET}}$ Input Voltage	2.5[3]	—	6.0	V
V_{IL}	Input LOW Voltage	–0.5[4]	—	0.8	V

NOTES:
3013 tbl 05

1. All speed grades except 8ns. Supply Voltage range for 8ns product is 4.75V min, 5.25V max (±5%).
2. All inputs except $\overline{\text{RESET}}$.
3. When using bipolar devices to drive the $\overline{\text{RESET}}$ input, a pullup resistor of 1kΩ–10kΩ is usually required to assure this voltage.
4. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.
5. V_{TERM} must not exceed V_{CC} + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

3013 tbl 06

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter		71B74S8	71B74S10	71B74S12	71B74S15	71B74S20	Unit
I_{CC}	Dynamic Operating Current	$\overline{\text{WE}}$ = V_{LC}	230	210	200	190	180	mA
	Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	$\overline{\text{WE}}$ = V_{HC}	210	200	170	160	150	mA

NOTES:
3013 tbl 07

1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC}, only input addresses are cycling at f_{MAX}.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	IDT71B74S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{\text{CS}}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output LOW Voltage	I_{OL} = 22mA MATCH	—	0.5	V
		I_{OL} = 18mA MATCH	—	0.4	
		I_{OL} = 10mA, V_{CC} = Min. (Except MATCH)	—	0.5	
		I_{OL} = 8mA, V_{CC} = Min. (Except MATCH)	—	0.4	
V_{OH}	Output HIGH Voltage	I_{OH} = –4mA, V_{CC} = Min. (Except MATCH)	2.4	—	V

3013 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, and 3

3013 tbl 09

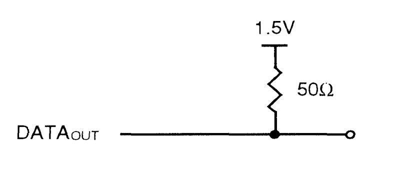


Figure 1. AC Test Load

11

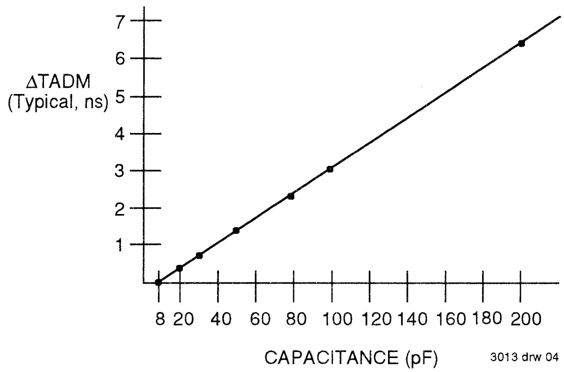
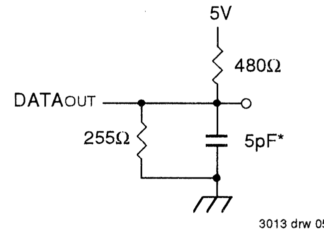


Figure 1A. Lumped Capacitive Load Typical Derating Curve



*Includes scope and jig.

Figure 2. AC Test Load (for tCLZ, tOLZ, tCHZ, tOHZ, tOW, tWHZ)

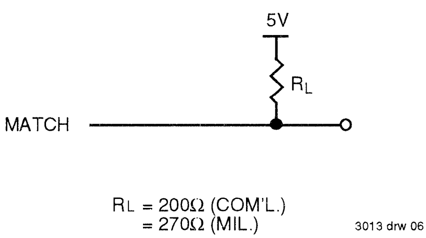


Figure 3. AC Test Load for MATCH

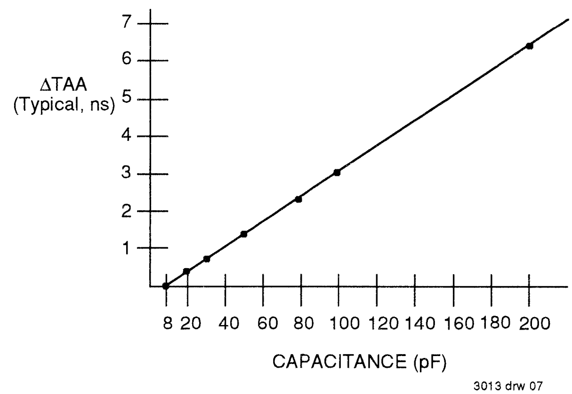
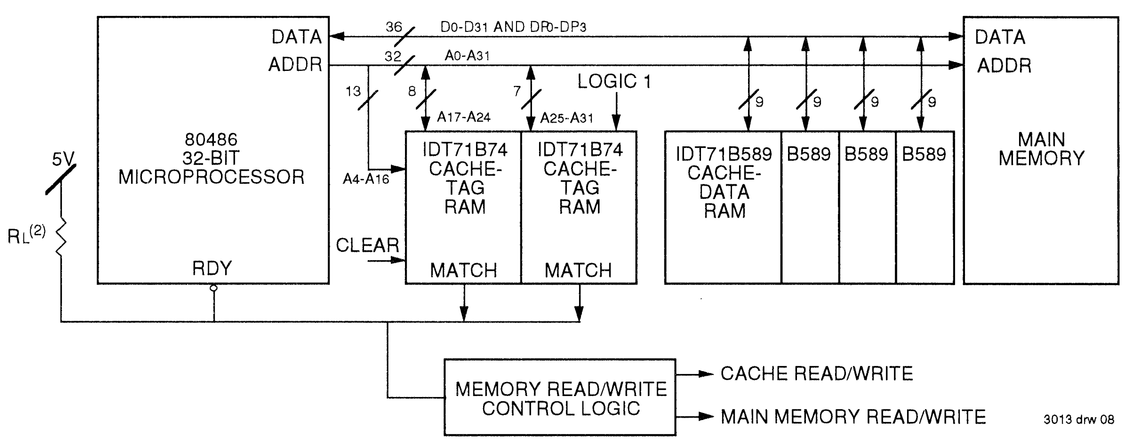


Figure 3A. Lumped Capacitive Load Typical Derating Curve



NOTES:
1. For more information refer to IDT Application Notes AN-07 and AN-78 and Technical Notes TN-11 and TN-13.
2. RL = 200Ω.

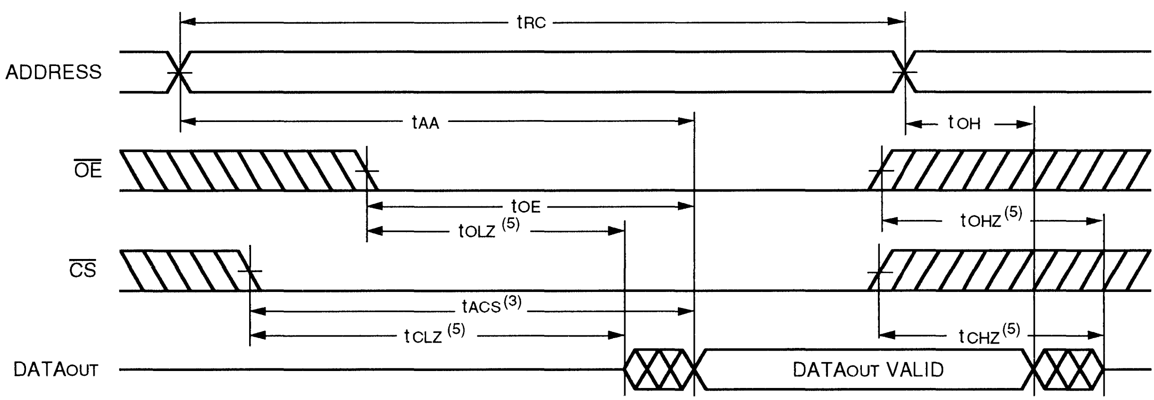
Figure 4. Example of Cache Memory System Block Diagram

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%)

Symbol	Parameter	71B74S8(2)		71B74S10		71B74S12		71B74S15		71B74S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tRC	Read Cycle Time	8	—	10	—	12	—	15	—	20	—	ns
tAA	Address Access Time	—	8	—	10	—	12	—	15	—	20	ns
tACS	Chip Select Access Time	—	6	—	7	—	8	—	8	—	10	ns
tCLZ(1)	Chip Select to Output in Low-Z	2	—	2	—	2	—	3	—	3	—	ns
tOE	Output Enable to Output Valid	—	5	—	6	—	6	—	8	—	9	ns
tOLZ(1)	Output Enable to Output in Low-Z	2	—	2	—	2	—	2	—	2	—	ns
tCHZ(1)	Chip Select to Output in High-Z	—	4	—	5	—	5	—	7	—	8	ns
tOHZ(1)	Output Disable to Output in High-Z	—	4	—	4	—	5	—	5	—	8	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns

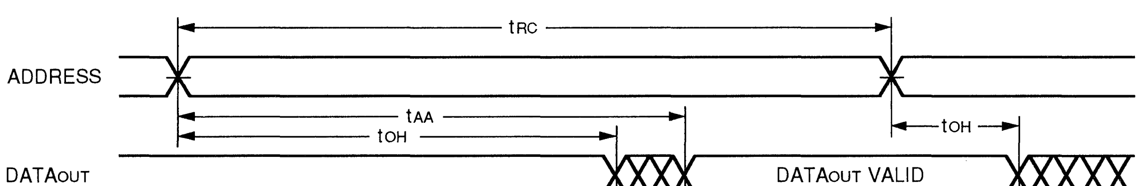
NOTES:
3013 tbl 10
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.
2. Vcc = 5.0V ± 5% for 8ns product.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



3013 drw 09

TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



NOTES:
3013 drw 10
1. WE is HIGH for Read cycle.
2. Device is continuously selected, CS is LOW.
3. Address valid prior to or coincident with CS transition LOW; otherwise tAA is the limiting parameter.
4. OE is continuously active, OE is LOW.
5. Transition is measured ±200mV from steady state.

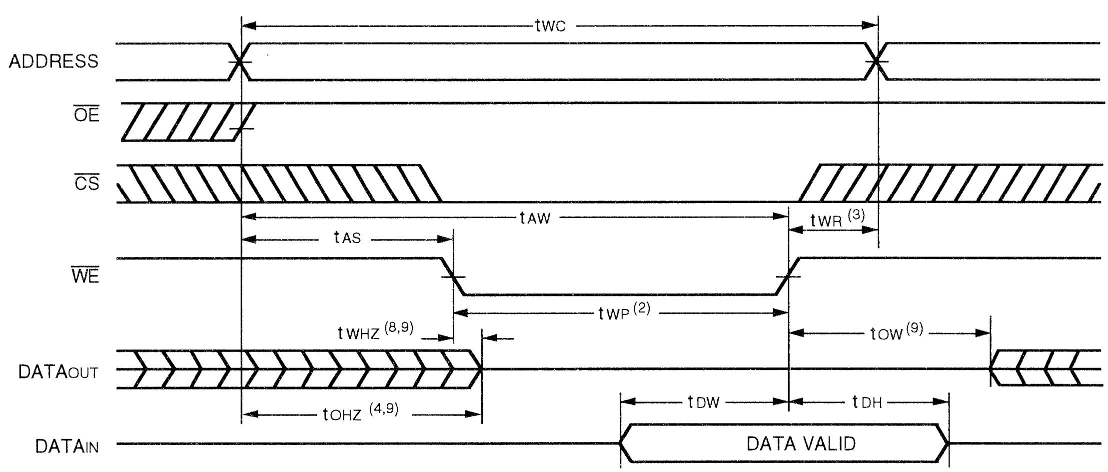
11

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%)

Symbol	Parameter	71B74S8(2)		71B74S10		71B74S12		71B74S15		71B74S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle												
tWC	Write Cycle Time	8	—	10	—	12	—	15	—	20	—	ns
tCW	Chip Select to End of Write	7	—	8	—	9	—	10	—	15	—	ns
tAW	Address Valid to End of Write	7	—	8	—	9	—	10	—	15	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	7	—	8	—	9	—	10	—	15	—	ns
tWR	Write Recovery Time (CS, WE)	0	—	0	—	0	—	0	—	0	—	ns
tWHZ(1)	Write Enable to Output in High-Z	—	5	—	5	—	5	—	5	—	5	ns
tDW	Data Valid to End of Write	5	—	5	—	6	—	8	—	10	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
tOW(1)	Output Active from End of Write	2	—	2	—	2	—	2	—	2	—	ns

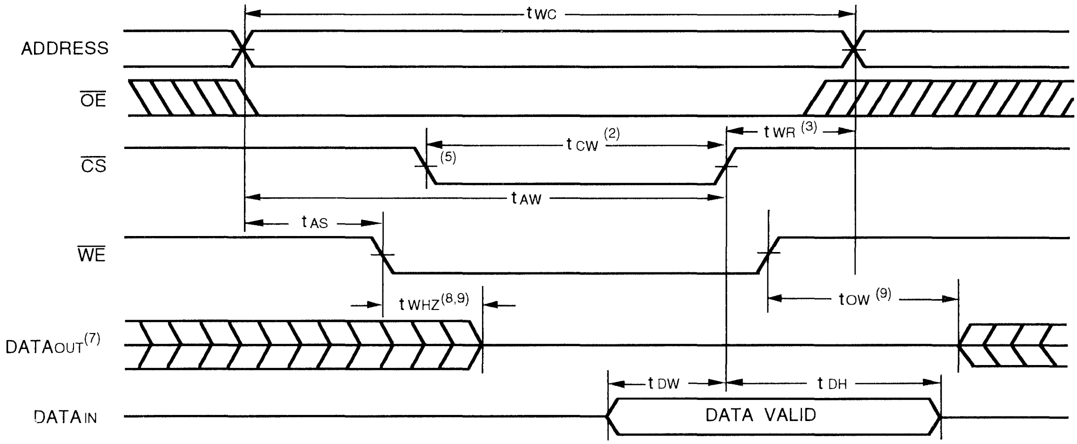
NOTES:
3013 tbl 11
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.
2. Vcc = 5.0V ± 5% for 8ns product.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (WE Controlled Timing, OE HIGH During Write)(1, 6)



3013 drw 11

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ Controlled Timing)(1, 6)



3013 drw 12

NOTES:
1. $\overline{WE}$, $\overline{CS}$ must be inactive during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{WE}$ and a LOW $\overline{CS}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. $\overline{OE}$ is continuously HIGH, $\overline{OE} \geq V_{IH}$. If during the $\overline{WE}$ controlled write cycle the $\overline{OE}$ is LOW, t_{WP} must be greater or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and the data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during the $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}. For a $\overline{CS}$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to t_{CW} timing.
7. DATAOUT is never enabled, therefore the output is in High-Z state during the entire write cycle.
8. t_{WHZ} is not included if $\overline{OE}$ remains HIGH during the write cycle. If $\overline{OE}$ is LOW during the Write Enabled write cycle then t_{WHZ} must be added to t_{WP} and t_{CW}.
9. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%)

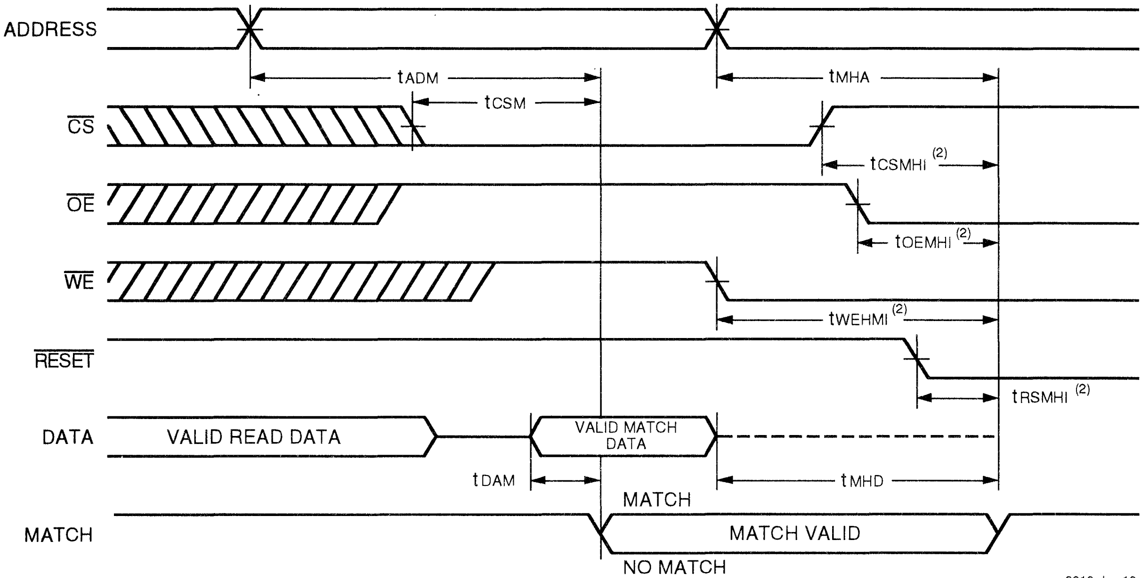
Symbol	Parameter	71B74S8(2) Min.	71B74S8(2) Max.	71B74S10 Min.	71B74S10 Max.	71B74S12 Min.	71B74S12 Max.	71B74S15 Min.	71B74S15 Max.	71B74S20 Min.	71B74S20 Max.	Unit
Match Cycle												
t_{ADM}	Address to MATCH Valid	—	8	—	10	—	12	—	15	—	20	ns
t_{CSM}	Chip Select to MATCH Valid	—	7	—	7	—	8	—	10	—	10	ns
t_{CSMHI}(1)	Chip Select to MATCH HIGH	—	7	—	8	—	8	—	8	—	8	ns
t_{DAM}	Data Input to MATCH Valid	—	7	—	8	—	10	—	12	—	12	ns
t_{OEMHI}(1)	$\overline{OE}$ LOW to MATCH HIGH	—	7	—	8	—	10	—	10	—	10	ns
t_{WEMHI}(1)	$\overline{WE}$ LOW to MATCH HIGH	—	7	—	8	—	10	—	10	—	10	ns
t_{RSMHI}(1)	$\overline{RESET}$ LOW to MATCH HIGH	—	8	—	10	—	10	—	12	—	15	ns
t_{MHA}	MATCH Valid Hold From Address	2	—	2	—	2	—	2	—	2	—	ns
t_{MHD}	MATCH Valid Hold From Data	2	—	2	—	2	—	2	—	2	—	ns

3001 tbl 12

NOTES:
1. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.
2. V_{CC} = 5.0V ± 5% for 8ns product.

11

MATCH TIMING(1)



3013 drw 13

NOTES:
1. It is not recommended to float data and address input pins while the MATCH pin is active.
2. Transition is measured at ±200mV from steady state.

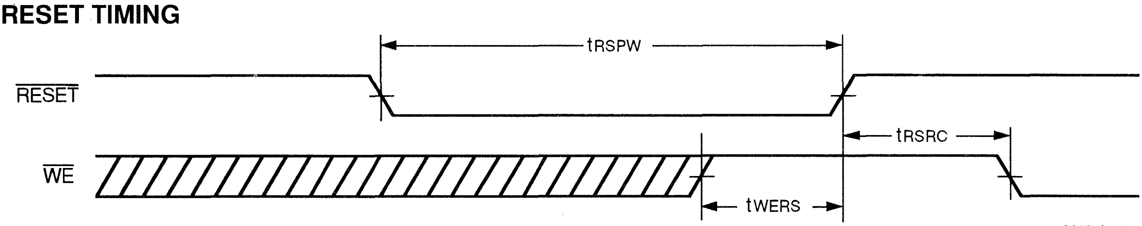
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%)

Symbol	Parameter	71B74S8(3) Min.	71B74S8(3) Max.	71B74S10 Min.	71B74S10 Max.	71B74S12 Min.	71B74S12 Max.	71B74S15 Min.	71B74S15 Max.	71B74S20 Min.	71B74S20 Max.	Unit
Read Cycle												
tRSPW(1)	Reset Pulse Width	30	—	35	—	35	—	40	—	45	—	ns
tWERS	WE HIGH to Reset HIGH	5	—	5	—	5	—	5	—	5	—	ns
tRSRC	Reset HIGH to WE LOW	25	—	25	—	25	—	30	—	30	—	ns
tPORS(2)	Power On Reset	100	—	100	—	100	—	120	—	120	—	ns

3001 tbl 13

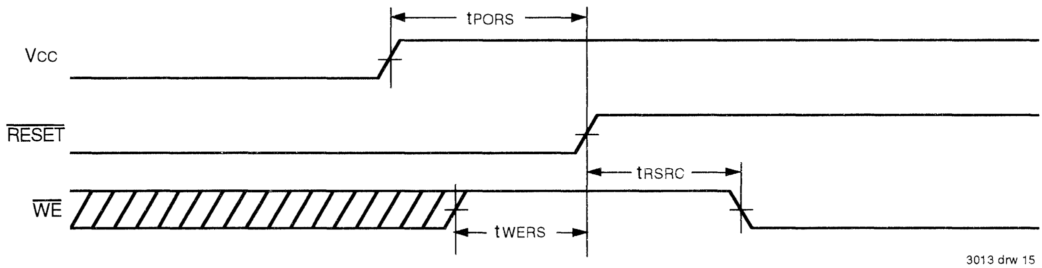
NOTES:
1. Recommended duty cycle = 10% maximum.
2. This parameter is guaranteed with the AC Load (Figure 1) by device characterization, but is not production tested.
3. Vcc = 5.0V ± 5% for 8ns product.

RESET TIMING

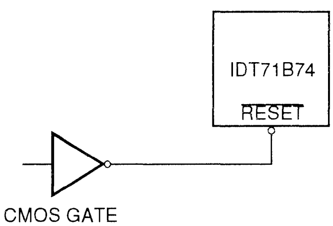


3013 drw 14

POWER ON RESET TIMING

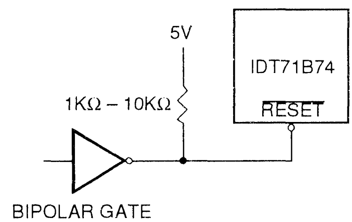


3013 drw 15



3013 drw 16

Driving the RESET pin with CMOS logic.



3013 drw 17

Driving the RESET pin with bipolar logic.

Figure 5.

ORDERING INFORMATION

IDT 71B74 S XX X X

IDT	71B74	S	XX	X	X
	Device Type	Power	Speed	Package	Process/ Temperature Range

Code	Description
Blank	Commercial (0°C to +70°C)
TP	Plastic DIP (300 mil) (P28–2)
Y	SOJ (Small Outline IC, J-bend) (SO28–5)
8	Commercial Only, SOJ Only
10	Commercial Only, SOJ Only
12	Commercial Only
15	Commercial Only
20	Commercial Only

8–20: Speed in ns

3013 drw 18

11

Integrated Device Technology, Inc.

BiCMOS StaticRAM 240K (16K x 15-BIT) CACHE-TAG RAM For the Pentium™ Processor

PRELIMINARY
IDT71215

FEATURES:

- 16K x 15 Configuration
  - 12 TAG Bits
  - 3 Separate I/O Status Bits (Valid, Dirty, Write Through)
- Match output uses Valid bit to qualify MATCH output
- High-Speed Address-to-Match comparison times
  - 10/12ns over commercial temperature range
- $\overline{\text{BRDY}}$ circuitry included inside the Cache-Tag for highest speed operation
- Asynchronous Read/Match operation with Synchronous Write and Reset operation
- Separate $\overline{\text{WE}}$ for the TAG bits and the Status bits
- Separate $\overline{\text{OE}}$ for the TAG bits, the Status bits, and $\overline{\text{BRDY}}$
- Synchronous $\overline{\text{RESET}}$ pin for invalidation of all Tag entries
- Dual Chip selects for easy depth expansion with no performance degredation
- I/O pins both 5V TTL and 3.3V LVTTL compatible with VCCQ pins
- $\overline{\text{PWRDN}}$ pin to place device in low-power mode
- Packaged in a 80-pin Thin Plastic Quad Flat Pack (TQFP)

DESCRIPTION:

The IDT71215 is a 245,760-bit Cache Tag StaticRAM, organized 16K x 15 and designed to support the Pentium and other Intel processors at bus speeds up to 66MHz. There are twelve common I/O TAG bits, with the remaining three bits used as status bits. A 12-bit comparator is on-chip to allow fast comparison of the twelve stored TAG bits and the current Tag input data. An active HIGH MATCH output is generated when these two groups of data are the same for a given address. This high-speed MATCH signal, with t_{ADM} times as fast as 10ns, provides the fastest possible enabling of secondary cache accesses.

The three separate I/O status bits (VLD, DTY, and WT) can be configured for either dedicated or generic functionality, depending on the SFUNC input pin. With SFUNC LOW, the status bits are defined and used internally by the device, allowing easier determination of the validity and use of the given Tag data. SFUNC HIGH releases the defined internal status bit usage and control, allowing the user to configure the status bit information to fit his system needs. A synchronous $\overline{\text{RESET}}$ pin, when held LOW at a rising clock edge, will reset all status bits in the array for easy invalidation of all Tag addresses.

The IDT71215 also provides the option for Burst Ready ($\overline{\text{BRDY}}$) generation within the cache tag itself, based upon MATCH, VLD bit, WT bit, and other external inputs provided by the user. This can significantly simplify cache controller logic and minimize cache decision time. Match and Read operations are both asynchronous in order to provide the fastest access times possible, while Write operations are synchronous for ease of system timing.

The IDT71215 uses a 5V power supply on Vcc and Vss, with separate VCCQ pins provided for the outputs to offer compliance with both 5.0V TTL and 3.3V LVTTL Logic levels. The $\overline{\text{PWRDN}}$ pin offers a low-power standby mode to reduce power consumption by 80%, providing significant system power savings.

The IDT71215 is fabricated using IDT's high-performance, high-reliability BiCMOS technology and is offered in a space-saving 80-pin Thin Plastic Quad Flat Pack (TQFP) package.

PIN DESCRIPTIONS

$A_0 - A_{13}$	Address Inputs	Input
$\overline{\text{CS1}}$, CS2	Chip Selects	Input
$\overline{\text{WET}}$	Write Enable - Tag Bits	Input
$\overline{\text{WES}}$	Write Enable - Status Bits	Input
$\overline{\text{OET}}$	Output Enable - Tag Bits	Input
$\overline{\text{OES}}$	Output Enable - Status Bits	Input
$\overline{\text{RESET}}$	Status Bit Reset	Input
$\overline{\text{PWRDN}}$	Powerdown Mode Control Pin	Input
SFUNC	Status Bit Function Control Pin	Input
W/$\overline{\text{R}}$	Write/Read Input from Processor	Input
VLD_{IN} / S_{1IN}	Valid Bit / S_1 Bit Input	Input
DTY_{IN} / S_{2IN}	Dirty Bit / S_2 Bit Input	Input
WT_{IN} / S_{3IN}	Write Through Bit / S_3 Bit Input	Input

CLK	System Clock	Input
BRDYH	$\overline{\text{BRDY}}$ Force High	Input
$\overline{\text{BRDYOE}}$	$\overline{\text{BRDY}}$ Output Enable	Input
$\overline{\text{BRDYIN}}$	Additional $\overline{\text{BRDY}}$ Input	Input
$\overline{\text{BRDY}}$	Burst Ready	Output
$TAG_0 - TAG_{11}$	Tag Data Input/Outputs	I/O
VLD_{OUT} / S_{1OUT}	Valid Bit / S_1 Bit Output	Output
DTY_{OUT} / S_{2OUT}	Dirty Bit / S_2 Bit Output	Output
WT_{OUT} / S_{3OUT}	Write Through Bit / S_3 Bit Output	Output
MATCH	Match	Output
VCC	+5V Power	Pwr
VCCQ	Output Buffer Power	QPwr
VSS	Ground	Gnd

3075 tbl 01

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Pentium is a trademark of Intel Corporation

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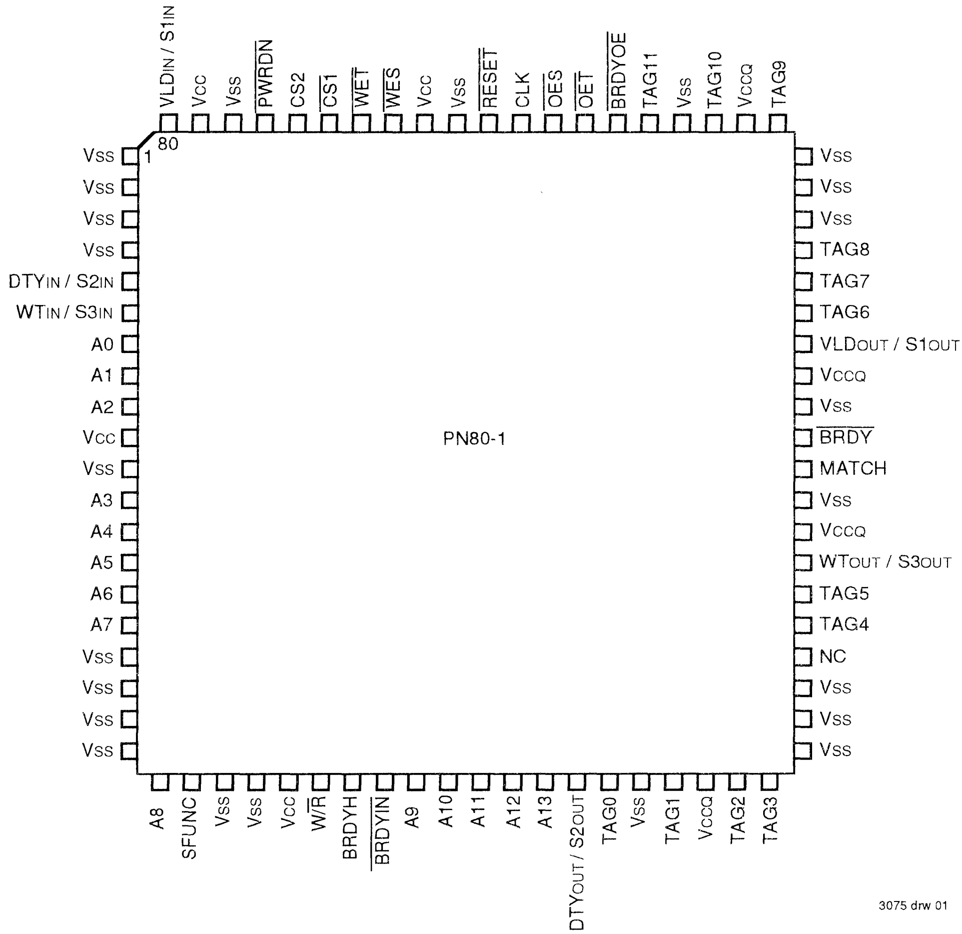
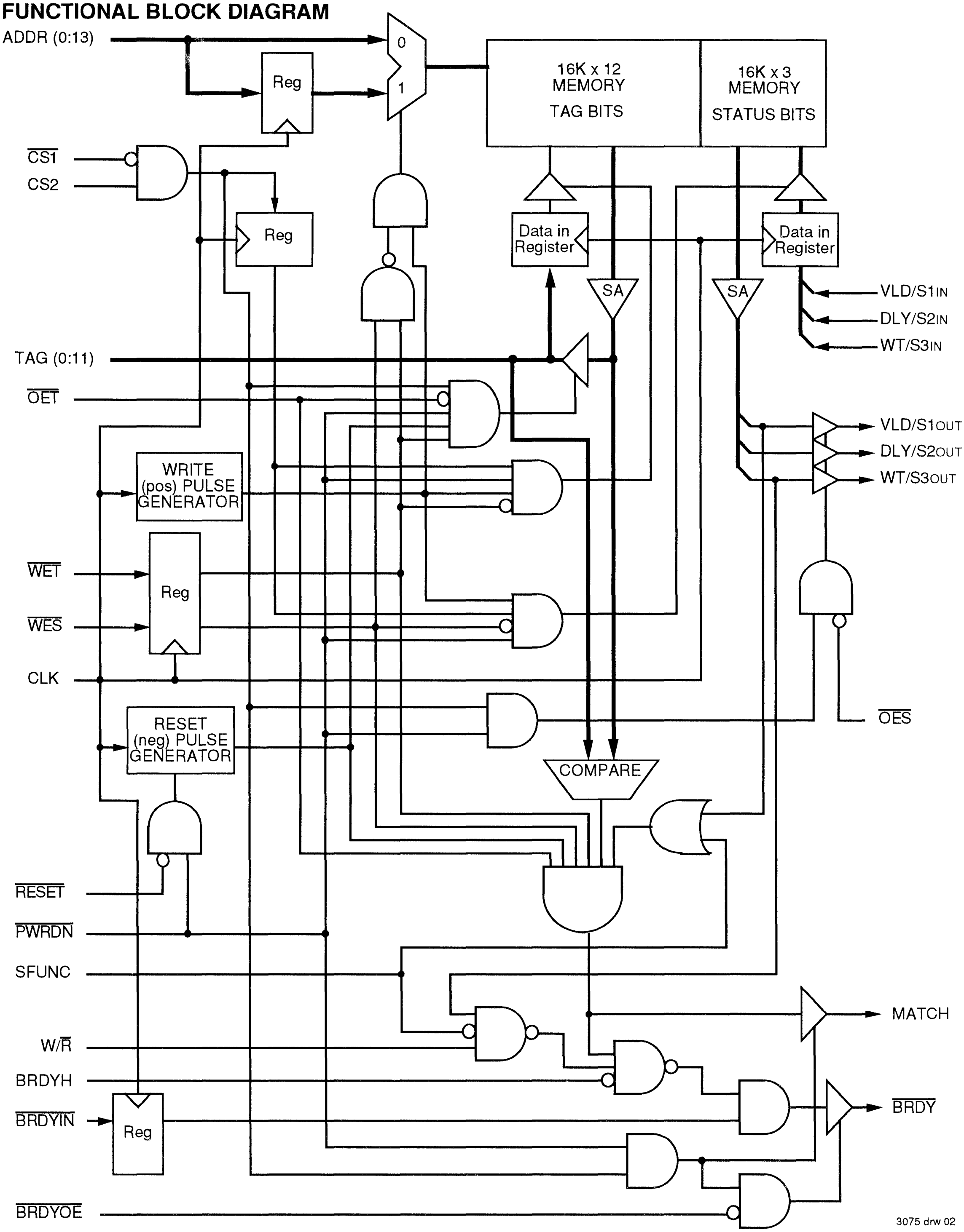
PIN CONFIGURATION



TQFP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLES

CHIP SELECT, RESET, AND POWER-DOWN FUNCTIONS[1, 2]

$\overline{CS1}$	CS2	$\overline{RESET}$	$\overline{PWRDN}$	CLK	$\overline{WET}$	$\overline{WES}$	$\overline{BRDYOE}$	TAG	VLDOUT	DTYOUT	WTOUT	MATCH	$\overline{BRDY}$	OPERATION	POWER
CHIP SELECT FUNCTION															
H	X	X	H	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Deselected	Active
X	L	X	H	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Deselected	Active
L	H	X	H	X	X	X	X	–	–	–	–	–	–	Selected	Active
RESET FUNCTION															
L	H	L	H	↑	H	H	L	Hi-Z	L[3]	L[3]	L[3]	L[3]	H	Reset Status	Active
L	H	L	H	↑	H	H	H	Hi-Z	L[3]	L[3]	L[3]	L[3]	Hi-Z	Reset Status	Active
H	X	L	H	↑	H	H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Reset Status	Active
X	L	L	H	↑	H	H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Reset Status	Active
X	X	L	H	↑	L	X	X	–	–	–	–	–	–	Not Allowed	–
X	X	L	H	↑	X	L	X	–	–	–	–	–	–	Not Allowed	–
POWER-DOWN FUNCTION															
X	X	X	L	X	H	H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power-down	Standby

NOTES: 3075 tbl 02
1. "H" = V_{IH}, "L" = V_{IL}, "X" = don't care, "–" = unrelated.
2. $\overline{OET}$, $\overline{OES}$, W/$\overline{R}$, BRDYH, $\overline{BRDYIN}$ and SFUNC are "X" for this table.
3. $\overline{OES}$ is LOW.

READ AND WRITE FUNCTIONS[1, 2]

$\overline{OET}$	$\overline{OES}$	$\overline{WET}$	$\overline{WES}$	CLK	W/$\overline{R}$	TAG	VLDIN	DTYIN	WTIN	VLDOUT	DTYOUT	WTOUT	MATCH	OPERATION
READ FUNCTION														
L	X	H	X	X	X	DOUT	–	–	–	–	–	–	DOUT	Read TAG I/O
X	L	X	X	X	X	–	–	–	–	DOUT	DOUT	DOUT	DOUT	Read Status Bits
H	X	X	X	X	X	Hi-Z	–	–	–	–	–	–	–	TAG I/O Disable
X	H	X	X	X	X	–	–	–	–	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Status Disabled
WRITE FUNCTION														
H	X	L	X	↑	X	DIN	–	–	–	DOUT	DOUT	DOUT	L	Write TAG I/O
L	X	L	X	↑	X	–	–	–	–	–	–	–	–	Not Allowed
X	L	X	L	↑	X	–	DIN	DIN	DIN	DOUT[3]	DOUT[3]	DOUT[3]	L	Write Status Bits
X	H	X	L	↑	X	–	DIN	DIN	DIN	Hi-Z	Hi-Z	Hi-Z	L	Write Status Bits

NOTES: 3075 tbl 03
1. "H" = V_{IH}, "L" = V_{IL}, "X" = don't care, "–" = unrelated.
2. This table applies when $\overline{CS1}$ is LOW and CS2, $\overline{RESET}$, and $\overline{PWRDN}$ are HIGH. $\overline{BRDYOE}$, BRDYH, $\overline{BRDYIN}$ and SFUNC are "X" for this table.
3. DOUT in this case is the same as DIN; that is, the input data is written through to the outputs during the write operation.

TRUTH TABLES (CONT.)

MATCH FUNCTION(1, 2, 3)

$\overline{\text{CS1}}$	CS2	SFUNC	$\overline{\text{OET}}$	$\overline{\text{WET}}$	$\overline{\text{WES}}$	TAG	VLD(4)	DTY(4)	WT(4)	MATCH	OPERATION
H	X	X	X	X	X	Hi-Z	–	–	–	Hi-Z	Deselected
X	L	X	X	X	X	Hi-Z	–	–	–	Hi-Z	Deselected
L	H	X	X	X	X	–	–	–	–	DOUT	Selected
L	H	X	L	H	X	DOUT	–	–	–	L	Read Tag I/O
L	H	X	H	L	X	DIN	–	–	–	L	Write Tag I/O
L	H	X	X	X	L	–	DIN	DIN	DIN	L	Write Status Bits
L	H	L	H	H	H	TAGIN	L	–	–	L	Invalid Data - Dedicated Status Bits
L	H	L	H	H	H	TAGIN	H	–	–	M	Match - Dedicated Status Bits
L	H	H	H	H	H	TAGIN	X	–	–	M	Match - Generic Status Bits

3075 tbl 04

NOTES:
1. "H" = VIH, "L" = VIL, "X" = don't care, "–" = unrelated.
2. M = HIGH if TAGIN equals the memory contents at that address; M = LOW if TAGIN does not equal the memory contents at that address.
3. $\overline{\text{PWRDN}}$ and $\overline{\text{RESET}}$ are HIGH for this table. W/$\overline{\text{R}}$, BRDYH, $\overline{\text{BRDYOE}}$, $\overline{\text{BRDYIN}}$, $\overline{\text{OES}}$, and CLK are "X".
4. This column represents the stored memory cell data for the given Status bit at the selected address.

$\overline{\text{BRDY}}$ FUNCTION(1, 2, 3, 5)

$\overline{\text{BRDYOE}}$	$\overline{\text{BRDYIN}}$(6)	$\overline{\text{OET}}$	$\overline{\text{WET}}$	$\overline{\text{WES}}$	BRDYH	W/$\overline{\text{R}}$	SFUNC	VLD(4)	DTY(4)	WT(4)	TAG	MATCH	$\overline{\text{BRDY}}$	OPERATION
H	X	X	X	X	X	X	X	X	–	X	–	–	Hi-Z	$\overline{\text{BRDY}}$ Disabled
L	L	X	X	X	X	X	X	X	–	X	–	X	L	Ext $\overline{\text{BRDY}}$ Input (7)
L	H	L	X	X	X	X	X	X	–	X	DOUT	L	H	Read TAG
L	H	X	L	X	X	X	X	X	–	X	DIN	L	H	Write TAG
L	H	X	X	L	X	X	X	DIN	DIN	DIN	–	L	H	Write Status
L	H	X	X	X	H	X	X	X	–	X	–	X	H	Force $\overline{\text{BRDY}}$ HIGH
L	H	X	X	X	X	X	L	L	–	X	–	L	H	Invalid TAG
L	H	X	X	X	X	H	L	X	–	H	–	X	H	Write Through
L	H	H	H	H	L	X	L	H	–	L	TAGIN	M	$\overline{\text{M}}$	Compare
L	H	H	H	H	L	L	L	H	–	X	TAGIN	M	$\overline{\text{M}}$	Compare
L	H	H	H	H	L	X	L	H	–	X	TAGIN	M	$\overline{\text{M}}$	Compare
L	H	H	H	H	L	X	H	X	–	X	TAGIN	M	$\overline{\text{M}}$	Compare

3075 tbl 05

NOTES:
1. "H" = VIH, "L" = VIL, "X" = don't care, "–" = unrelated.
2. M = HIGH if TAGIN equals the memory contents at that address; M = LOW if TAGIN does not equal the memory contents at that address.
3. $\overline{\text{PWRDN}}$ and $\overline{\text{RESET}}$ are HIGH for this table. CLK and $\overline{\text{OES}}$ are "X".
4. This column represents the stored memory cell data for the given Status bit at the selected address.
5. $\overline{\text{CS1}}$ is LOW, CS2 is HIGH for this table.
6. $\overline{\text{BRDYIN}}$ is a synchronous input; thus the inputs noted in the table must be applied during a rising CLK edge.
7. $\overline{\text{BRDYIN}}$ will be a factor in determining the $\overline{\text{BRDY}}$ output in all cases except when BRDYH is HIGH and there is a valid MATCH. In that case, $\overline{\text{BRDY}}$ will be LOW(Valid).

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
V_{CCQ}	5V Output Buffers	4.75	5.0	5.25	V
V_{CCQ}	3.3V Output Buffers	3.0	3.3	3.6	V
V_{SS}	Supply Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.0	V_{CC}+0.3	V
V_{IHQ}	I/O High Voltage	2.2	3.0	V_{CCQ}+0.3	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 3075 tbl 06
1. V_{IL} (min.) = –1.5V for pulse width of less than 10ns, once per cycle.

CAPACITANCE

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{TAG}	TAG Input/Output Capacitance	$V_{I/O}$ = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 3075 tbl 07
1. This parameter is determined by device characterization but is not production tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0[2]	V
T_A	Operating Temperature	–0 to +70	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.7	W
I_{OUT}	DC Output Current	20	mA

NOTES: 3075 tbl 08
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.
2. V_{IN} should not exceed V_{CC}+0.5V. All pins should not exceed 7.0V. V_{CCQ} should never exceed V_{CC}, and V_{CC} should never exceed V_{CCQ} + 4.0V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

(V_{CC} = 5.0V ± 5%, V_{CCQ} = 5.0V ± 5% OR 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0V to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS1} \geq V_{IH}$, CS2 ≤ V_{IL}, $\overline{OE} \geq V_{IH}$, V_{CC} = Max. V_{OUT} = 0V to V_{CCQ}, V_{CCQ} = Max.	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

3075 tbl 09

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1, 2] (V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Condition	71215S10 Com'l.	71215S10 Mil.	71215S12 Com'l.	71215S12 Mil.	Unit
I_{CC}	Operating Power Supply Current	$\overline{PWRDN} \geq V_{IH}$ Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	320	—	310	—	mA
I_{SB}	Standby Power Supply Current	$\overline{PWRDN} \leq V_{IL}$, $V_{IN} \geq V_{IH}$ **or** ≤ V_{IL} V_{CC} = Max., f = f_{MAX}[3]	50	—	50	—	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{PWRDN} \leq V_{IL}$, $V_{IN} \geq V_{HC}$ **or** ≤ V_{LC}[4] V_{CC} = Max., f = 0[3]	30	—	30	—	mA

NOTES: 3075 tbl 10
1. All values are maximum guaranteed values.
2. $\overline{CS1} \leq V_{IL}$, CS2 ≥ V_{IH}.
3. f_{MAX} =1/t_{CYC} (all address inputs are cycling at f_{MAX}). f = 0 means no address input lines are changing.
4. V_{HC} = V_{CC} - 0.2V, V_{LC} = 0.2V

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, V_{CCQ} = 5.0V ± 5% OR 3.3V ± 0.3V, T_A = 0 to 70°C)

Symbol	Parameter	IDT71215S10		IDT71215S12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{AAT}	Address Access Time Tag Bits	—	12	—	14	ns
t_{ACST}	Chip Select Access Time Tag Bits	—	10	—	12	ns
t_{CLZ}[1]	Chip Select to Tag and Status Bits in Low-Z	1	—	1	—	ns
t_{CHZ}[1]	Chip Select to Tag and Status Bits in High-Z	1	6	1	7	ns
t_{OET}	Output Enable to Tag Bits Valid	—	8	—	9	ns
t_{OTLZ}[1]	Output Enable to Tag Bits in Low-Z	0	—	0	—	ns
t_{OTHZ}[1]	Output Enable to Tag Bits in High-Z	1	6	1	7	ns
t_{TOH}	Tag Bit Hold from Address Change	3	—	3	—	ns
t_{OES}	Output Enable to Status Bits Valid	—	8	—	9	ns
t_{OSLZ}[1]	Output Enable to Status Bits in Low-Z	0	—	0	—	ns
t_{OSHZ}[1]	Output Enable to Status Bits in High-Z	1	6	1	7	ns
t_{AAS}	Address Access Time Status Bits	—	10	—	12	ns
t_{ACSS}	Chip Select Access Time Status Bits	—	9	—	11	ns
t_{SOH}	Status Bit Hold from Address Change	3	—	3	—	ns

NOTE: 3075 tbl 11

1. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.

AC ELECTRICAL CHARACTERISTICS (1)

(V_{CC} = 5.0V ± 5%, V_{CCQ} = 5.0V ± 5% OR 3.3V ± 0.3V, T_A = 0 to 70°C)

Symbol	Parameter	IDT71215S10		IDT71215S12		Unit
		Min.	Max.	Min.	Max.	
Reset and Power Down Cycles						
t_{SR}	$\overline{\text{RESET}}$ Set-up Time	4	—	4	—	ns
t_{HR}	$\overline{\text{RESET}}$ Hold Time	1	—	1	—	ns
t_{SRST}	Status Bit Reset Time	—	60	—	70	ns
t_{SHRS}	Status Bit Hold from $\overline{\text{RESET}}$ LOW	2	—	2	—	ns
t_{RSMI}	$\overline{\text{RESET}}$ LOW to MATCH and $\overline{\text{BRDY}}$ Invalid	—	10	—	12	ns
t_{RSMV}	$\overline{\text{RESET}}$ HIGH to MATCH and $\overline{\text{BRDY}}$ Valid	—	100	—	110	ns
t_{RSHZ}[2]	$\overline{\text{RESET}}$ LOW to TAG High-Z	—	10	—	12	ns
t_{RSLZ}[2]	$\overline{\text{RESET}}$ HIGH to TAG Low-Z	—	100	—	110	ns
t_{PDSR}	$\overline{\text{PWRDN}}$ Set-up to $\overline{\text{RESET}}$ LOW	30	—	30	—	ns
t_{RHWL}	$\overline{\text{RESET}}$ HIGH to $\overline{\text{WET}}$ and $\overline{\text{WES}}$ LOW	80	—	90	—	ns
t_{PD}[2]	$\overline{\text{PWRDN}}$ LOW to Low Power Mode	—	50	—	50	ns
t_{PU}[2]	$\overline{\text{PWRDN}}$ HIGH to Active Power Mode	0	—	0	—	ns
t_{PDHZ}[2]	$\overline{\text{PWRDN}}$ LOW to Outputs in High-Z	—	10	—	12	ns
t_{PDLZ}[2]	$\overline{\text{PWRDN}}$ HIGH to Outputs in Low-Z	0	—	0	—	ns
t_{PUV}	$\overline{\text{PWRDN}}$ HIGH to Outputs Valid	—	50	—	50	ns
t_{WHPL}[2]	$\overline{\text{WET}}$ and $\overline{\text{WES}}$ HIGH to $\overline{\text{PWRDN}}$ LOW	5	—	5	—	ns
t_{PUWL}	$\overline{\text{PWRDN}}$ HIGH to $\overline{\text{WET}}$ and $\overline{\text{WES}}$ Active	50	—	50	—	ns

NOTES: 3075 tbl 12

1. Power-down mode is intended to be used during extended time periods of device inactivity.
2. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.

AC ELECTRICAL CHARACTERISTICS (1)

(V_{CC} = 5.0V ± 5%, V_{CCQ} = 5.0V ± 5% OR 3.3V ± 0.3V, T_A = 0 to 70°C)

Symbol	Parameter	IDT71215S10 Min.	IDT71215S10 Max.	IDT71215S12 Min.	IDT71215S12 Max.	Unit
Write Cycle and Clock Parameters						
t_{CYC}	Clock Cycle Time	15	—	16.6	—	ns
t_{CH}(2, 3)	Clock Pulse HIGH	4.5	—	5	—	ns
t_{CL}(2, 3)	Clock Pulse LOW	4.5	—	5	—	ns
t_S	$\overline{WET}$, $\overline{WES}$, Chip Select, and Input Data Set-up Time	3	—	3	—	ns
t_H	$\overline{WET}$, $\overline{WES}$, Chip Select, and Input Data Hold Time	1.5	—	1.5	—	ns
t_{SA}	Address Set-up Time	3	—	3	—	ns
t_{HA}	Address Hold Time	1.5	—	1.5	—	ns
t_{WMI}	CLK HIGH Write to MATCH and $\overline{BRDY}$ Invalid	—	7	—	8	ns
t_{CKLZ}(3)	CLK HIGH Read to Outputs in Low-Z	1.5	—	1.5	—	ns
t_{CTV}(4)	CLK HIGH Read to Tag Bits Valid	—	10	—	12	ns
t_{CSV}(4)	CLK HIGH Write to Status Outputs Valid	—	9	—	10	ns
t_{CSH}(3)	Status Output Hold from CLK HIGH Write	0	—	0	—	ns
t_{WHPL}	$\overline{WET}$ and $\overline{WES}$ HIGH to $\overline{PWRDN}$ LOW	5	—	5	—	ns
t_{PUWL}	$\overline{PWRDN}$ HIGH to $\overline{WET}$ and $\overline{WES}$ Active	50	—	50	—	ns

3075 tbl 14

NOTES:
1. All Write cycles are synchronous and referenced from rising CLK.
2. This parameter is measured as a HIGH time above 2.0V and a LOW time below 0.8V.
3. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.
4. Addresses are stable prior to CLK transition HIGH.

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, V_{CCQ} = 5.0V ± 5% OR 3.3V ± 0.3V, T_A = 0 to 70°C)

Symbol	Parameter	IDT71215S10		IDT71215S12		Unit
		Min.	Max.	Min.	Max.	
MATCH and $\overline{\text{BRDY}}$ Cycles						
t_{ADM}	Address to MATCH Valid	—	10	—	12	ns
t_{DAM}	Data Input to MATCH Valid	—	10	—	12	ns
t_{CSM}	Chip Select to MATCH Valid	—	10	—	12	ns
t_{CMLZ}[1]	Chip Select to MATCH in Low-Z	1	—	1	—	ns
t_{CMHZ}[1]	Chip Select to MATCH in High-Z	1	6	1	7	ns
t_{MHA}	MATCH Valid Hold from Address	2	—	2	—	ns
t_{MHD}	MATCH Valid Hold from Data	2	—	2	—	ns
t_{BHA}	$\overline{\text{BRDY}}$ Valid Hold from Address	2	—	2	—	ns
t_{BHD}	$\overline{\text{BRDY}}$ Valid Hold from Data	2	—	2	—	ns
t_{ADB}	Address to $\overline{\text{BRDY}}$ Valid	—	11	—	13	ns
t_{DAB}	Data Input to $\overline{\text{BRDY}}$ Valid	—	11	—	13	ns
t_{CSB}	Chip Select LOW to $\overline{\text{BRDY}}$ Valid	—	11	—	13	ns
t_{OEBV}	$\overline{\text{BRDYOE}}$ LOW to $\overline{\text{BRDY}}$ Valid	—	7	—	8	ns
t_{OBLZ}[1]	$\overline{\text{BRDYOE}}$ LOW to $\overline{\text{BRDY}}$ in Low-Z	0	—	0	—	ns
t_{OBHZ}[1]	$\overline{\text{BRDYOE}}$ HIGH to $\overline{\text{BRDY}}$ in High-Z	1	6	1	7	ns
t_{BYFH}	BRDYH HIGH to Force $\overline{\text{BRDY}}$ HIGH	—	5	—	6	ns
t_{BYHV}	BRDYH LOW to $\overline{\text{BRDY}}$ Valid	—	5	—	6	ns
t_{SB}	$\overline{\text{BRDYIN}}$ Set-up Time	4	—	4	—	ns
t_{HB}	$\overline{\text{BRDYIN}}$ Hold Time	1.5	—	1.5	—	ns
t_{BIBL}	CLK HIGH $\overline{\text{BRDYIN}}$ LOW to $\overline{\text{BRDY}}$ LOW	—	7	—	8	ns
t_{BIBV}	CLK HIGH $\overline{\text{BRDYIN}}$ HIGH to $\overline{\text{BRDY}}$ Valid	—	7	—	8	ns
t_{OEMI}	$\overline{\text{OET}}$ LOW to MATCH and $\overline{\text{BRDY}}$ Invalid	—	7	—	8	ns
t_{OEMV}	$\overline{\text{OET}}$ HIGH to MATCH and $\overline{\text{BRDY}}$ Valid	—	8	—	10	ns
t_{WRBH}[2]	W/$\overline{\text{R}}$ HIGH to $\overline{\text{BRDY}}$ HIGH	—	7	—	8	ns
t_{WRBV}[2]	W/$\overline{\text{R}}$ LOW to $\overline{\text{BRDY}}$ Valid	—	7	—	8	ns
t_{WMI}	CLK HIGH Write to MATCH and $\overline{\text{BRDY}}$ Invalid	—	7	—	8	ns
t_{WMV}[3]	CLK HIGH Read to MATCH and $\overline{\text{BRDY}}$ Valid	—	10	—	12	ns

3075 tbl 15

NOTES:

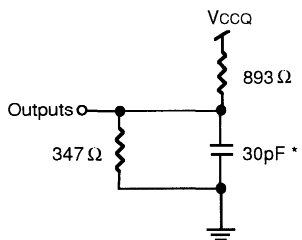
1. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.
2. These parameters only apply when SFUNC is LOW and the internal WT bit is HIGH.
3. t_{ADM}, t_{DAM}, t_{CSM} and t_{ADB}, t_{DAB}, t_{CSB} must also be satisfied.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figs. 1, 2, 3, & 4

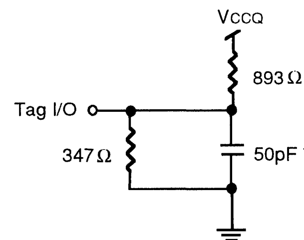
3075 tbl 16

AC TEST LOADS



3075 drw 03

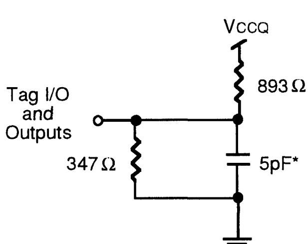
Figure 1. AC Test Load



3075 drw 04

Figure 2. Tag I/O AC Test Load

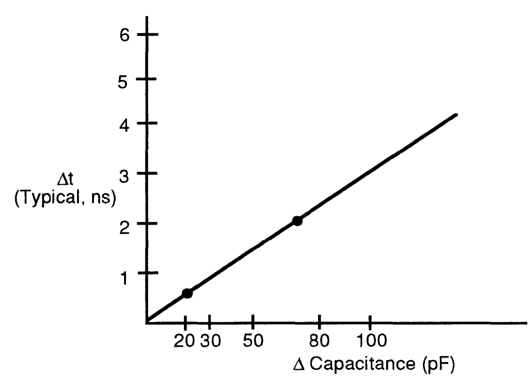
* Including scope and jig capacitance



3075 drw 05

Figure 3. AC Test Load (for tHZ and tLZ parameters)

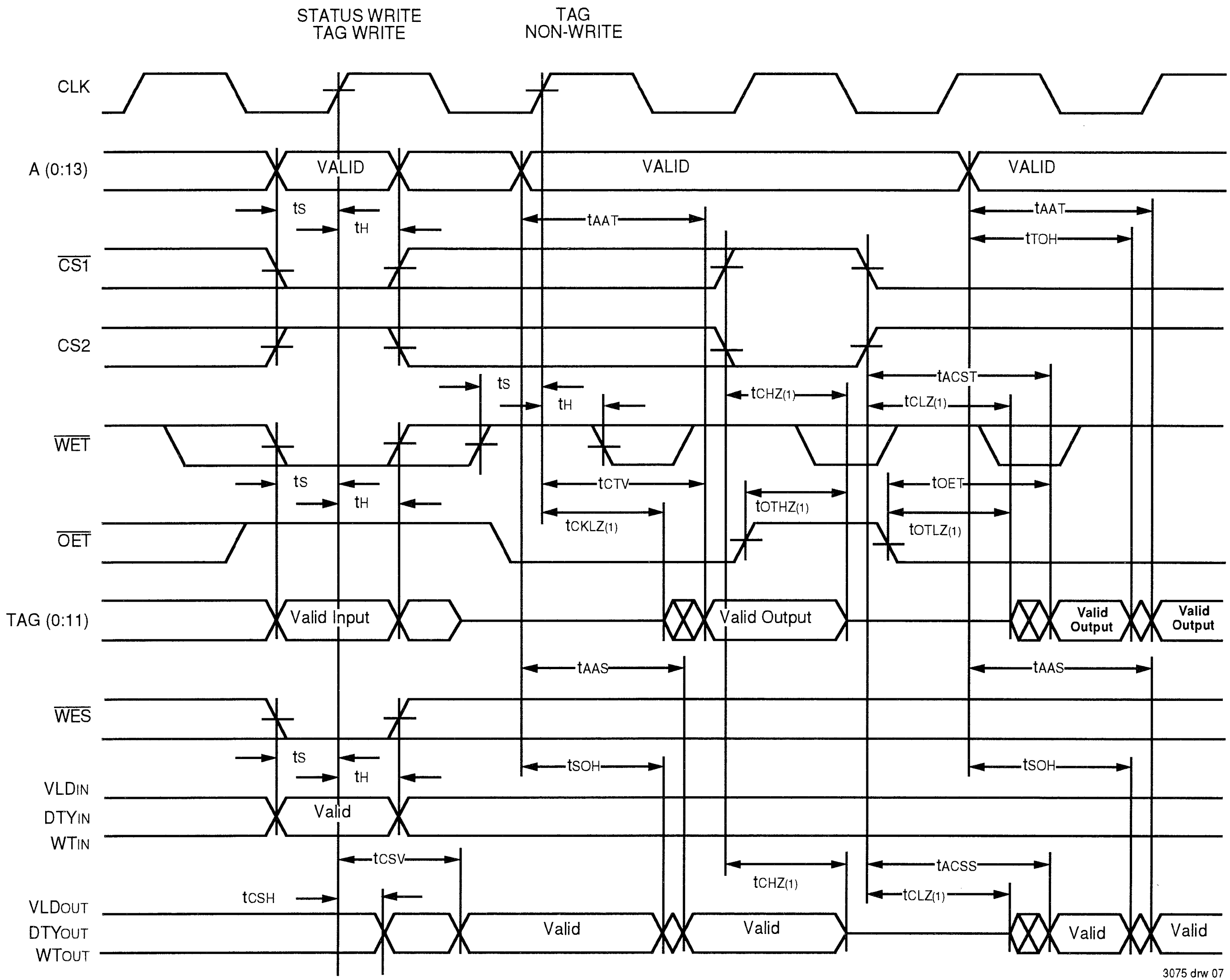
* Including scope and jig capacitance



3075 drw 06

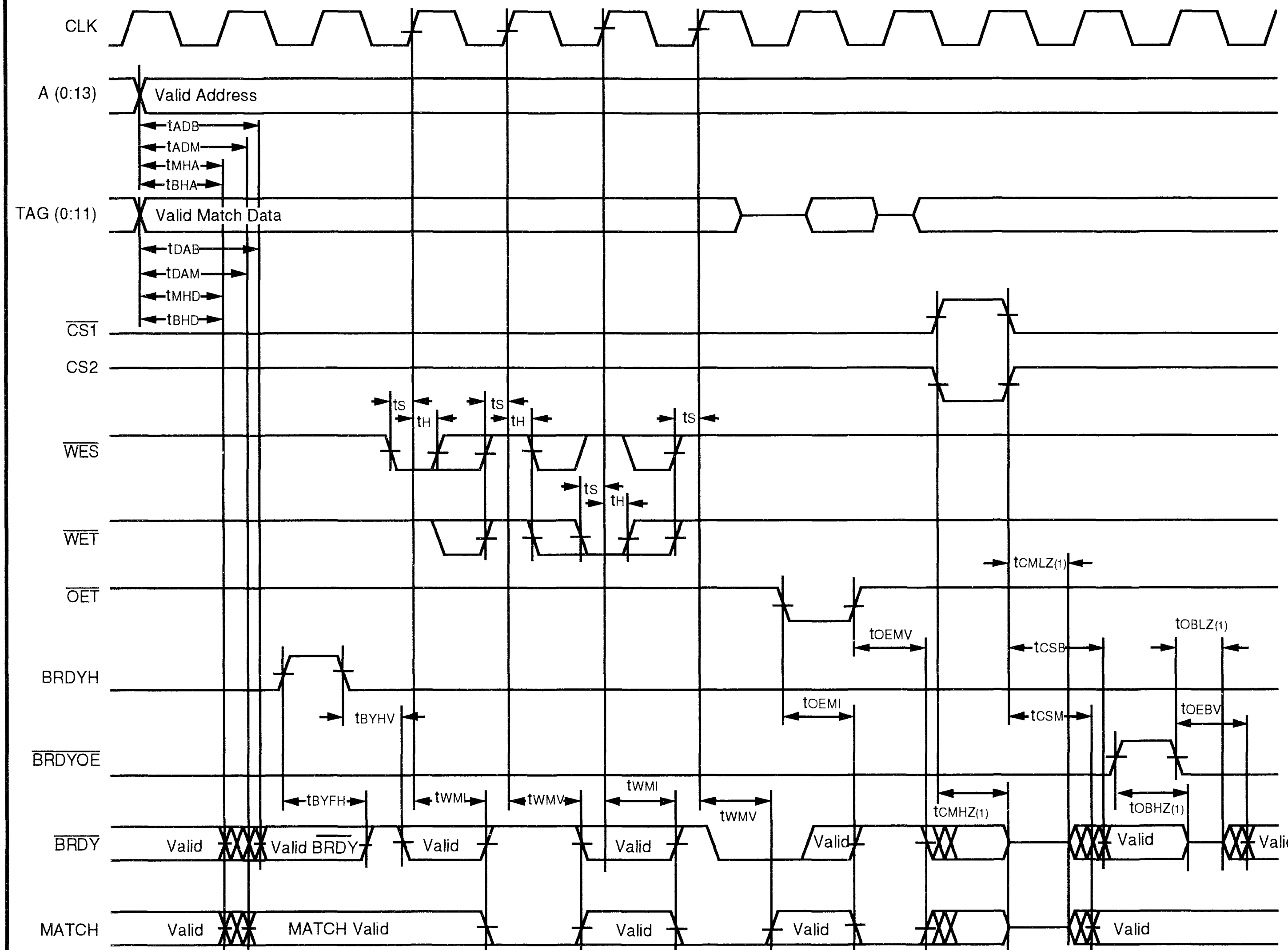
Figure 4. Lumped Capacitance Load, Typical Derating

TIMING WAVEFORMS OF WRITE AND READ CYCLES



NOTE:
1. Transition is measured ±200mV from steady state.

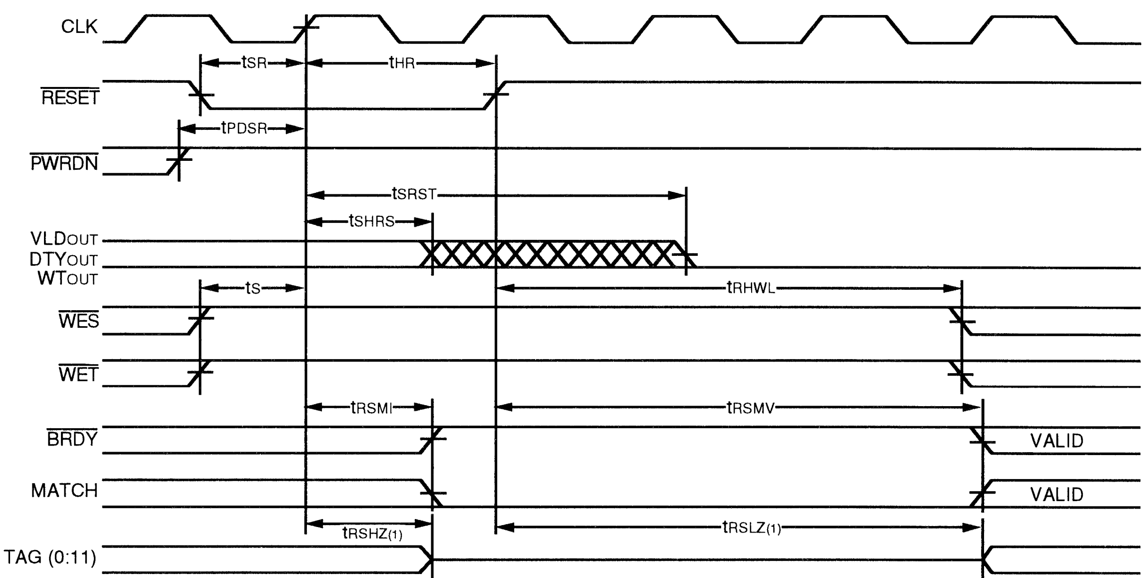
TIMING WAVEFORMS OF MATCH AND $\overline{\text{BRDY}}$ FUNCTIONS



3075 drw 08

NOTE:
1. Transition is measured ±200mV from steady state.

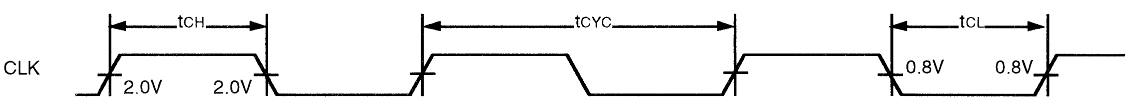
TIMING WAVEFORMS OF $\overline{\text{RESET}}$ FUNCTION



3075 drw 09

NOTE:
1. Transition is measured ±200mV from steady state.

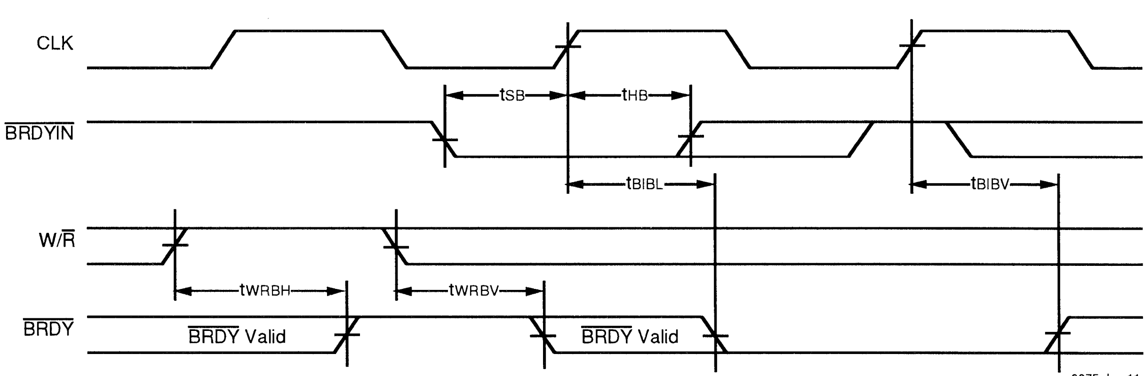
SYSTEM CLOCK TIMING WAVEFORM



3075 drw 10

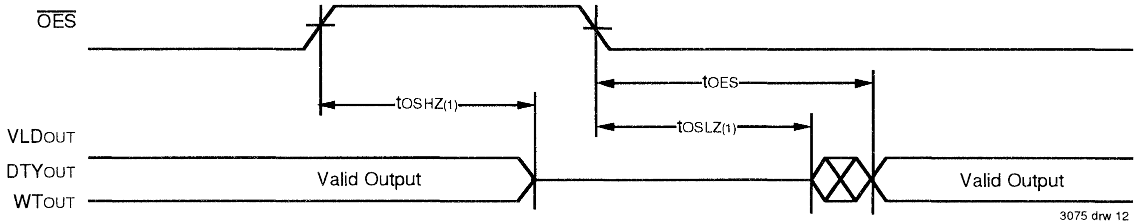
TIMING WAVEFORMS OF $\overline{\text{BRDY}}$ AND W/$\overline{\text{R}}$ SIGNAL

Applies when SFUNC is LOW, and the internal WT bit is HIGH



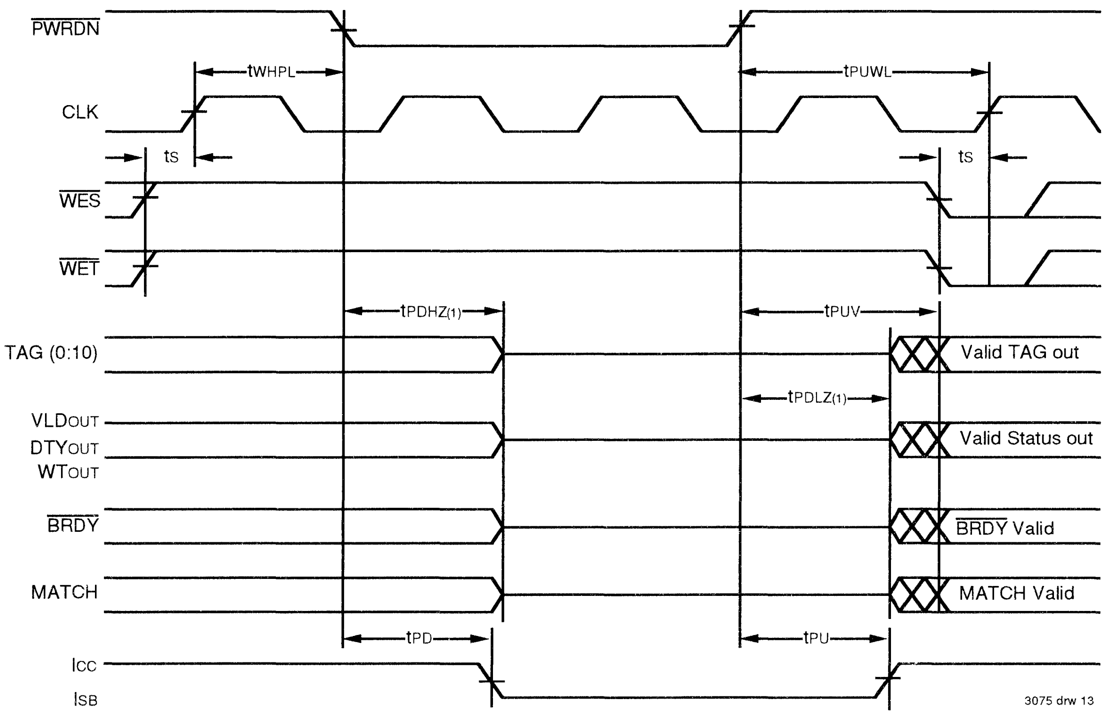
3075 drw 11

TIMING WAVEFORMS OF $\overline{OES}$ FUNCTION



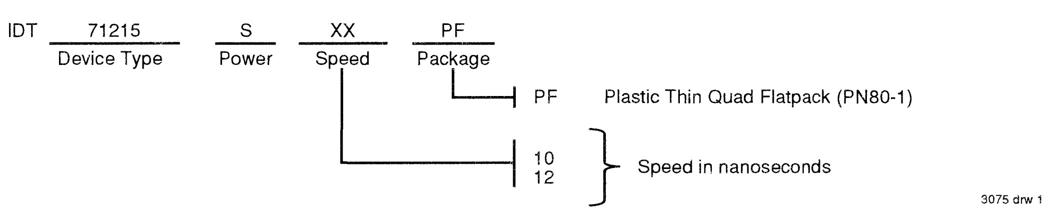
NOTE:
1. Transition is measured ±200mV from steady state.

TIMING WAVEFORMS OF POWER DOWN FUNCTION



NOTE:
1. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



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Integrated Device Technology, Inc.

BiCMOS StaticRAM 240K (16Kx15-BIT) CACHE-TAG RAM For PowerPC™ and RISC Processors

PRELIMINARY
IDT71216

FEATURES:

- 16K x 15 Configuration
  - 12 TAG Bits
  - 3 Separate I/O Status Bits (Valid, Dirty, Write Through)
- Match output uses Valid bit to qualify MATCH output
- High-Speed Address-to-Match comparison times
  - 10/12ns over commercial temperature range
- $\overline{TA}$ circuitry included inside the Cache-Tag for highest speed operation
- Asynchronous Read/Match operation with Synchronous Write and Reset operation
- Separate $\overline{WE}$ for the TAG bits and the Status bits
- Separate $\overline{OE}$ for the TAG bits, the Status bits, and $\overline{TA}$
- Synchronous $\overline{RESET}$ pin for invalidation of all Tag entries
- Dual Chip selects for easy depth expansion with no performance degredation
- I/O pins both 5V TTL and 3.3V LVTTL compatible with VCCQ pins
- $\overline{PWRDN}$ pin to place device in low-power mode
- Packaged in a 80-pin Thin Plastic Quad Flat Pack (TQFP)

DESCRIPTION:

The IDT71216 is a 245,760-bit Cache Tag StaticRAM, organized 16K x 15 and designed to support PowerPC and other RISC processors at bus speeds up to 66MHz. There are twelve common I/O TAG bits, with the remaining three bits used as status bits. A 12-bit comparator is on-chip to allow fast comparison of the twelve stored TAG bits and the current Tag input data. An active HIGH MATCH output is generated when these two groups of data are the same for a given address. This high-speed MATCH signal, with t_{ADM} times as fast as 10ns, provides the fastest possible enabling of secondary cache accesses.

The three separate I/O status bits (VLD, DTY, and WT) can be configured for either dedicated or generic functionality, depending on the SFUNC input pin. With SFUNC LOW, the status bits are defined and used internally by the device, allowing easier determination of the validity and use of the given Tag data. SFUNC HIGH releases the defined internal status bit usage and control, allowing the user to configure the status bit information to fit his system needs. A synchronous $\overline{RESET}$ pin, when held LOW at a rising clock edge, will reset all status bits in the array for easy invalidation of all Tag addresses.

The IDT71216 also provides the option for Transfer Acknowledge ($\overline{TA}$) generation within the cache tag itself, based upon MATCH, VLD bit, WT bit, and other external inputs provided by the user. This can significantly simplify cache controller logic and minimize cache decision time. Match and Read operations are both asynchronous in order to provide the fastest access times possible, while Write operations are synchronous for ease of system timing.

The IDT71216 uses a 5V power supply on Vcc and Vss, with separate VCCQ pins provided for the outputs to offer compliance with both 5.0V TTL and 3.3V LVTTL Logic levels. The $\overline{PWRDN}$ pin offers a low-power standby mode to reduce power consumption by 80%, providing significant system power savings.

The IDT71216 is fabricated using IDT's high-performance, high-reliability BiCMOS technology and is offered in a space-saving 80-pin Thin Plastic Quad Flat Pack (TQFP) package.

PIN DESCRIPTIONS

$A_0 - A_{13}$	Address Inputs	Input
$\overline{CS1}$, CS2	Chip Selects	Input
$\overline{WET}$	Write Enable - Tag Bits	Input
$\overline{WES}$	Write Enable - Status Bits	Input
$\overline{OET}$	Output Enable - Tag Bits	Input
$\overline{OES}$	Output Enable - Status Bits	Input
$\overline{RESET}$	Status Bit Reset	Input
$\overline{PWRDN}$	Powerdown Mode Control Pin	Input
SFUNC	Status Bit Function Control Pin	Input
TT1	Read/Write Input from Processor	Input
VLD_{IN} / S_{1IN}	Valid Bit / S_1 Bit Input	Input
DTY_{IN} / S_{2IN}	Dirty Bit / S_2 Bit Input	Input
WT_{IN} / S_{3IN}	Write Through Bit / S_3 Bit Input	Input

CLK	System Clock	Input
TAH	$\overline{TA}$ Force High	Input
$\overline{TAOE}$	$\overline{TA}$ Output Enable	Input
$\overline{TAIN}$	Additional $\overline{TA}$ Input	Input
$\overline{TA}$	Transfer Acknowledge	Output
$TAG_0 - TAG_{11}$	Tag Data Input/Outputs	I/O
VLD_{OUT} / S_{1OUT}	Valid Bit / S_1 Bit Output	Output
DTY_{OUT} / S_{2OUT}	Dirty Bit / S_2 Bit Output	Output
WT_{OUT} / S_{3OUT}	Write Through Bit / S_3 Bit Output	Output
MATCH	Match	Output
V_{CC}	+5V Power	Pwr
V_{CCQ}	Output Buffer Power	QPwr
V_{SS}	Ground	Gnd

3067 tbl 01

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PowerPC is a trademark of International Business Machines, Inc.

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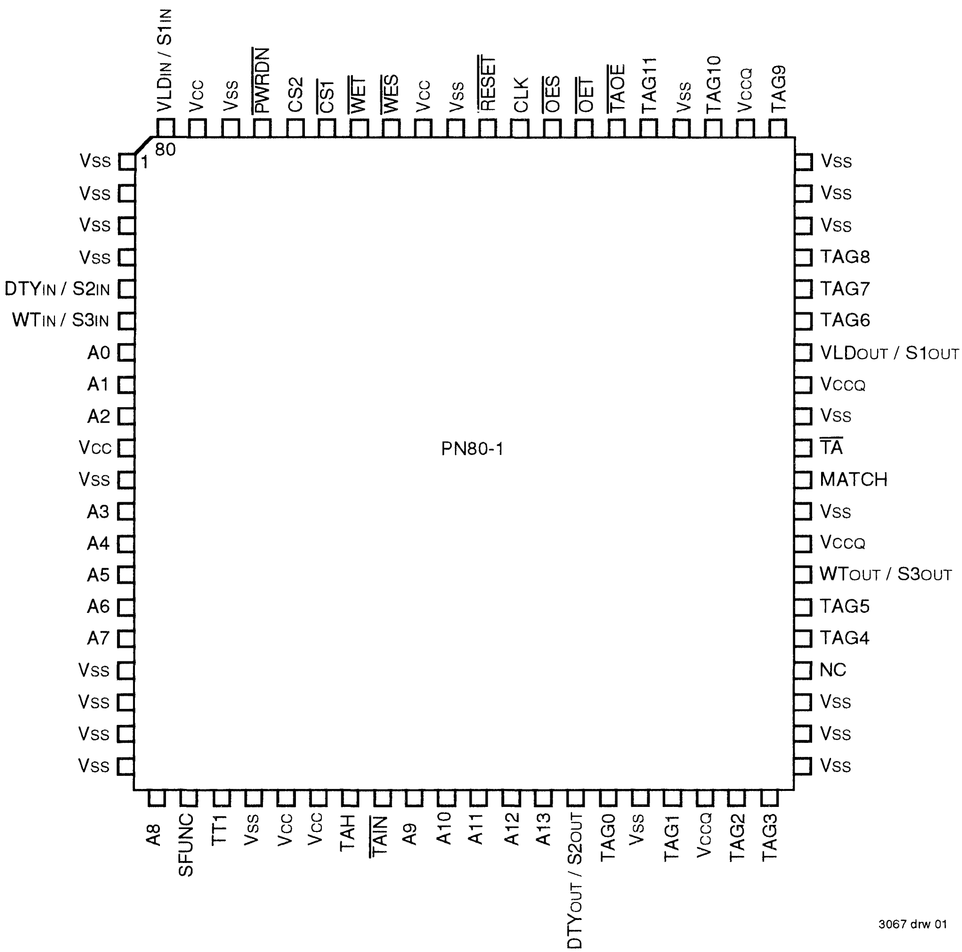
PIN CONFIGURATION



TQFP
TOP VIEW

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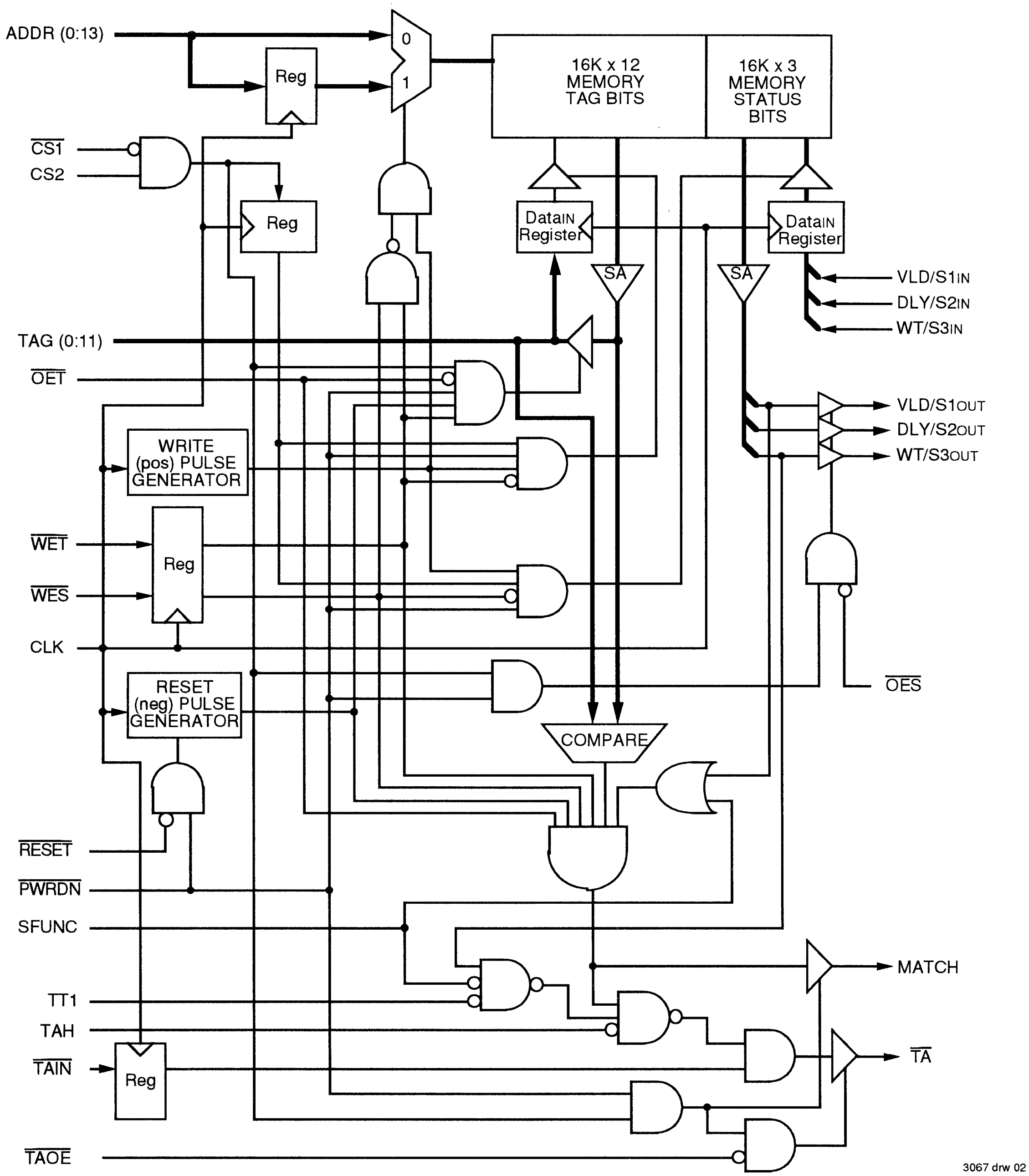
FUNCTIONAL BLOCK DIAGRAM



3067 drw 02

TRUTH TABLES

CHIP SELECT, RESET, AND POWER-DOWN FUNCTIONS(1, 2)

$\overline{CS1}$	CS2	$\overline{RESET}$	$\overline{PWRDN}$	CLK	$\overline{WET}$	$\overline{WES}$	$\overline{TAOE}$	TAG	VLDOUT	DTYOUT	WTOUT	MATCH	$\overline{TA}$	OPERATION	POWER
CHIP SELECT FUNCTION															
H	X	X	H	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Deselected	Active
X	L	X	H	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Deselected	Active
L	H	X	H	X	X	X	X	–	–	–	–	–	–	Selected	Active
RESET FUNCTION															
L	H	L	H	↑	H	H	L	Hi-Z	L(3)	L(3)	L(3)	L(3)	H	Reset Status	Active
L	H	L	H	↑	H	H	H	Hi-Z	L(3)	L(3)	L(3)	L(3)	Hi-Z	Reset Status	Active
H	X	L	H	↑	H	H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Reset Status	Active
X	L	L	H	↑	H	H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Reset Status	Active
X	X	L	H	↑	L	X	X	–	–	–	–	–	–	Not Allowed	–
X	X	L	H	↑	X	L	X	–	–	–	–	–	–	Not Allowed	–
POWER-DOWN FUNCTION															
X	X	X	L	X	H	H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power-down	Standby

NOTES: 3067 tbl 02

1. "H" = V_{IH}, "L" = V_{IL}, "X" = don't care, "–" = unrelated.
2. $\overline{OET}$, $\overline{OES}$, TT1, TAH, $\overline{TAIN}$ and SFUNC are "X" for this table.
3. $\overline{OES}$ is LOW.

READ AND WRITE FUNCTIONS(1, 2)

$\overline{OET}$	$\overline{OES}$	$\overline{WET}$	$\overline{WES}$	CLK	TT1	TAG	VLDIN	DTYIN	WTIN	VLDOUT	DTYOUT	WTOUT	MATCH	OPERATION
READ FUNCTION														
L	X	H	X	X	X	DOUT	–	–	–	–	–	–	DOUT	Read TAG I/O
X	L	X	X	X	X	–	–	–	–	DOUT	DOUT	DOUT	DOUT	Read Status Bits
H	X	X	X	X	X	Hi-Z	–	–	–	–	–	–	–	TAG I/O Disable
X	H	X	X	X	X	–	–	–	–	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Status Disabled
WRITE FUNCTION														
H	X	L	X	↑	X	DIN	–	–	–	DOUT	DOUT	DOUT	L	Write TAG I/O
L	X	L	X	↑	X	–	–	–	–	–	–	–	–	Not Allowed
X	L	X	L	↑	X	–	DIN	DIN	DIN	DOUT(3)	DOUT(3)	DOUT(3)	L	Write Status Bits
X	H	X	L	↑	X	–	DIN	DIN	DIN	Hi-Z	Hi-Z	Hi-Z	L	Write Status Bits

NOTES: 3067 tbl 03

1. "H" = V_{IH}, "L" = V_{IL}, "X" = don't care, "–" = unrelated.
2. This table applies when $\overline{CS1}$ is LOW and CS2, $\overline{RESET}$, and $\overline{PWRDN}$ are HIGH. $\overline{TAOE}$, TAH, $\overline{TAIN}$ and SFUNC are "X" for this table.
3. DOUT in this case is the same as DIN; that is, the input data is written through to the outputs during the write operation.

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TRUTH TABLES (CONT.)

MATCH FUNCTION(1, 2, 3)

$\overline{\text{CS1}}$	CS2	SFUNC	$\overline{\text{OET}}$	$\overline{\text{WET}}$	$\overline{\text{WES}}$	TAG	VLD(4)	DTY(4)	WT(4)	MATCH	OPERATION
H	X	X	X	X	X	Hi-Z	–	–	–	Hi-Z	Deselected
X	L	X	X	X	X	Hi-Z	–	–	–	Hi-Z	Deselected
L	H	X	X	X	X	–	–	–	–	D_{OUT}	Selected
L	H	X	L	H	X	D_{OUT}	–	–	–	L	Read Tag I/O
L	H	X	H	L	X	D_{IN}	–	–	–	L	Write Tag I/O
L	H	X	X	X	L	–	D_{IN}	D_{IN}	D_{IN}	L	Write Status Bits
L	H	L	H	H	H	TAG_{IN}	L	–	–	L	Invalid Data - Dedicated Status Bits
L	H	L	H	H	H	TAG_{IN}	H	–	–	M	Match - Dedicated Status Bits
L	H	H	H	H	H	TAG_{IN}	X	–	–	M	Match - Generic Status Bits

NOTES:
3067 tbl 04

1. "H" = V_{IH}, "L" = V_{IL}, "X" = don't care, "–" = unrelated.
2. M = HIGH if TAG_{IN} equals the memory contents at that address; M = LOW if TAG_{IN} does not equal the memory contents at that address.
3. $\overline{\text{PWRDN}}$ and $\overline{\text{RESET}}$ are HIGH for this table. TT1, TAH, $\overline{\text{TAOE}}$, $\overline{\text{TAIN}}$, $\overline{\text{OES}}$, and CLK are "X".
4. This column represents the stored memory cell data for the given Status bit at the selected address.

$\overline{\text{TA}}$ FUNCTION(1, 2, 3, 5)

$\overline{\text{TAOE}}$	$\overline{\text{TAIN}}$(6)	$\overline{\text{OET}}$	$\overline{\text{WET}}$	$\overline{\text{WES}}$	TAH	TT1	SFUNC	VLD(4)	DTY(4)	WT(4)	TAG	MATCH	$\overline{\text{TA}}$	OPERATION
H	X	X	X	X	X	X	X	X	–	X	–	–	Hi-Z	$\overline{\text{TA}}$ Disabled
L	L	X	X	X	X	X	X	X	–	X	–	X	L	External $\overline{\text{TA}}$ Input (7)
L	H	L	X	X	X	X	X	X	–	X	D_{OUT}	L	H	Read TAG
L	H	X	L	X	X	X	X	X	–	X	D_{IN}	L	H	Write TAG
L	H	X	X	L	X	X	X	D_{IN}	D_{IN}	D_{IN}	–	L	H	Write Status
L	H	X	X	X	H	X	X	X	–	X	–	X	H	Force $\overline{\text{TA}}$ HIGH
L	H	X	X	X	X	X	L	L	–	X	–	L	H	Invalid TAG
L	H	X	X	X	X	L	L	X	–	H	–	X	H	Write Through
L	H	H	H	H	L	X	L	H	–	L	TAG_{IN}	M	$\overline{\text{M}}$	Compare
L	H	H	H	H	L	H	L	H	–	X	TAG_{IN}	M	$\overline{\text{M}}$	Compare
L	H	H	H	H	L	X	L	H	–	X	TAG_{IN}	M	$\overline{\text{M}}$	Compare
L	H	H	H	H	L	X	H	X	–	X	TAG_{IN}	M	$\overline{\text{M}}$	Compare

NOTES:
3067 tbl 05

1. "H" = V_{IH}, "L" = V_{IL}, "X" = don't care, "–" = unrelated.
2. M = HIGH if TAG_{IN} equals the memory contents at that address; M = LOW if TAG_{IN} does not equal the memory contents at that address.
3. $\overline{\text{PWRDN}}$ and $\overline{\text{RESET}}$ are HIGH for this table. CLK and $\overline{\text{OES}}$ are "X".
4. This column represents the stored memory cell data for the given Status bit at the selected address.
5. $\overline{\text{CS1}}$ is LOW, CS2 is HIGH for this table.
6. $\overline{\text{TAIN}}$ is a synchronous input; thus the inputs noted in the table must be applied during a rising CLK edge.
7. $\overline{\text{TAIN}}$ will be a factor in determining the $\overline{\text{TA}}$ output in all cases except when TAH is HIGH and there is a valid MATCH. In that case, $\overline{\text{TA}}$ will be LOW(Valid).

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
V_{CCQ}	5V Output Buffers	4.75	5.0	5.25	V
V_{CCQ}	3.3V Output Buffers	3.0	3.3	3.6	V
V_{SS}	Supply Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.0	V_{CC}+0.3	V
V_{IHQ}	I/O High Voltage	2.2	3.0	V_{CCQ}+0.3	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 3067 tbl 06
1. V_{IL} (min.) = –1.5V for pulse width of less than 10ns, once per cycle.

CAPACITANCE

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{TAG}	TAG Input/Output Capacitance	$V_{I/O}$ = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 3067 tbl 07
1. This parameter is determined by device characterization but is not production tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0[2]	V
T_A	Operating Temperature	–0 to +70	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.7	W
I_{OUT}	DC Output Current	20	mA

NOTES: 3067 tbl 08
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.
2. V_{IN} should not exceed V_{CC}+0.5V. All pins should not exceed 7.0V. V_{CCQ} should never exceed V_{CC}, and V_{CC} should never exceed V_{CCQ} + 4.0V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

(V_{CC} = 5.0V ± 5%, V_{CCQ} = 5.0V ± 5% OR 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0V to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS1} \geq V_{IH}$, CS2 ≤ V_{IL}, $\overline{OE} \geq V_{IH}$, V_{CC} = Max. V_{OUT} = 0V to V_{CCQ}, V_{CCQ} = Max.	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

3067 tbl 09

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1, 2] (V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Condition	71216S10 Com'l.	71216S10 Mil.	71216S12 Com'l.	71216S12 Mil.	Unit
I_{CC}	Operating Power Supply Current	$\overline{PWRDN} \geq V_{IH}$ Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	320	—	310	—	mA
I_{SB}	Standby Power Supply Current	$\overline{PWRDN} \leq V_{IL}$, $V_{IN} \geq V_{IH}$ **or** ≤ V_{IL} V_{CC} = Max., f = f_{MAX}[3]	50	—	50	—	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{PWRDN} \leq V_{IL}$, $V_{IN} \geq V_{HC}$ **or** ≤ V_{LC}[4] V_{CC} = Max., f = 0[3]	30	—	30	—	mA

NOTES: 3067 tbl 10
1. All values are maximum guaranteed values.
2. $\overline{CS1} \leq V_{IL}$, CS2 ≥ V_{IH}.
3. f_{MAX} =1/t_{CYC} (all address inputs are cycling at f_{MAX}). f = 0 means no address input lines are changing.
4. V_{HC} = V_{CC} - 0.2V, V_{LC} = 0.2V

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, V_{CCQ} = 5.0V ± 5% OR 3.3V ± 0.3V, T_A = 0 to 70°C)

Symbol	Parameter	IDT71216S10 Min.	IDT71216S10 Max.	IDT71216S12 Min.	IDT71216S12 Max.	Unit
Read Cycle						
t_{AAT}	Address Access Time Tag Bits	—	12	—	14	ns
t_{ACST}	Chip Select Access Time Tag Bits	—	10	—	12	ns
t_{CLZ}(1)	Chip Select to Tag and Status Bits in Low-Z	1	—	1	—	ns
t_{CHZ}(1)	Chip Select to Tag and Status Bits in High-Z	1	6	1	7	ns
t_{OET}	Output Enable to Tag Bits Valid	—	8	—	9	ns
t_{OTLZ}(1)	Output Enable to Tag Bits in Low-Z	0	—	0	—	ns
t_{OTHZ}(1)	Output Enable to Tag Bits in High-Z	1	6	1	7	ns
t_{TOH}	Tag Bit Hold from Address Change	3	—	3	—	ns
t_{OES}	Output Enable to Status Bits Valid	—	8	—	9	ns
t_{OSLZ}(1)	Output Enable to Status Bits in Low-Z	0	—	0	—	ns
t_{OSHZ}(1)	Output Enable to Status Bits in High-Z	1	6	1	7	ns
t_{AAS}	Address Access Time Status Bits	—	10	—	12	ns
t_{ACSS}	Chip Select Access Time Status Bits	—	9	—	11	ns
t_{SOH}	Status Bit Hold from Address Change	3	—	3	—	ns

NOTE:
1. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.

3067 tbl 11

AC ELECTRICAL CHARACTERISTICS (1)

(V_{CC} = 5.0V ± 5%, V_{CCQ} = 5.0V ± 5% OR 3.3V ± 0.3V, T_A = 0 to 70°C)

Symbol	Parameter	IDT71216S10 Min.	IDT71216S10 Max.	IDT71216S12 Min.	IDT71216S12 Max.	Unit
Reset and Power Down Cycles						
t_{SR}	$\overline{RESET}$ Set-up Time	4	—	4	—	ns
t_{HR}	$\overline{RESET}$ Hold Time	1	—	1	—	ns
t_{SRST}	Status Bit Reset Time	—	60	—	70	ns
t_{SHRS}	Status Bit Hold from $\overline{RESET}$ LOW	2	—	2	—	ns
t_{RSMI}	$\overline{RESET}$ LOW to MATCH and $\overline{TA}$ Invalid	—	10	—	12	ns
t_{RSMV}	$\overline{RESET}$ HIGH to MATCH and $\overline{TA}$ Valid	—	100	—	110	ns
t_{RSHZ}(2)	$\overline{RESET}$ LOW to TAG High-Z	—	10	—	12	ns
t_{RSLZ}(2)	$\overline{RESET}$ HIGH to TAG Low-Z	—	100	—	110	ns
t_{PDSR}	$\overline{PWRDN}$ Set-up to $\overline{RESET}$ LOW	30	—	30	—	ns
t_{RHWL}	$\overline{RESET}$ HIGH to $\overline{WET}$ and $\overline{WES}$ LOW	80	—	90	—	ns
t_{PD}(2)	$\overline{PWRDN}$ LOW to Low Power Mode	—	50	—	50	ns
t_{PU}(2)	$\overline{PWRDN}$ HIGH to Active Power Mode	0	—	0	—	ns
t_{PDHZ}(2)	$\overline{PWRDN}$ LOW to Outputs in High-Z	—	10	—	12	ns
t_{PDLZ}(2)	$\overline{PWRDN}$ HIGH to Outputs in Low-Z	0	—	0	—	ns
t_{PUV}	$\overline{PWRDN}$ HIGH to Outputs Valid	—	50	—	50	ns
t_{WHPL}(2)	$\overline{WET}$ and $\overline{WES}$ HIGH to $\overline{PWRDN}$ LOW	5	—	5	—	ns
t_{PUWL}	$\overline{PWRDN}$ HIGH to $\overline{WET}$ and $\overline{WES}$ Active	50	—	50	—	ns

NOTES:
1. Power-down mode is intended to be used during extended time periods of device inactivity.
2. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.

3067 tbl 12

AC ELECTRICAL CHARACTERISTICS (1)

(V_{CC} = 5.0V ± 5%, V_{CCQ} = 5.0V ± 5% OR 3.3V ± 0.3V, T_A = 0 to 70°C)

Symbol	Parameter	IDT71216S10 Min.	IDT71216S10 Max.	IDT71216S12 Min.	IDT71216S12 Max.	Unit
Write Cycle and Clock Parameters						
t_{CYC}	Clock Cycle Time	15	—	16.6	—	ns
t_{CH}(2, 3)	Clock Pulse HIGH	4.5	—	5	—	ns
t_{CL}(2, 3)	Clock Pulse LOW	4.5	—	5	—	ns
t_S	$\overline{WET}$, $\overline{WES}$, Chip Select, and Input Data Set-up Time	3	—	3	—	ns
t_H	$\overline{WET}$, $\overline{WES}$, Chip Select, and Input Data Hold Time	1.5	—	1.5	—	ns
t_{SA}	Address Set-up Time	3	—	3	—	ns
t_{HA}	Address Hold Time	1.5	—	1.5	—	ns
t_{WMI}	CLK HIGH Write to MATCH and $\overline{TA}$ Invalid	—	7	—	8	ns
t_{CKLZ}(3)	CLK HIGH Read to Outputs in Low-Z	1.5	—	1.5	—	ns
t_{CTV}(4)	CLK HIGH Read to Tag Bits Valid	—	10	—	12	ns
t_{CSV}(4)	CLK HIGH Write to Status Outputs Valid	—	9	—	10	ns
t_{CSH}(3)	Status Output Hold from CLK HIGH Write	0	—	0	—	ns
t_{WHPL}	$\overline{WET}$ and $\overline{WES}$ HIGH to $\overline{PWRDN}$ LOW	5	—	5	—	ns
t_{PUWL}	$\overline{PWRDN}$ HIGH to $\overline{WET}$ and $\overline{WES}$ Active	50	—	50	—	ns

3067 tbl 14

NOTES:
1. All Write cycles are synchronous and referenced from rising CLK.
2. This parameter is measured as a HIGH time above 2.0V and a LOW time below 0.8V.
3. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.
4. Addresses are stable prior to CLK transition HIGH.

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, V_{CCQ} = 5.0V ± 5% OR 3.3V ± 0.3V, T_A = 0 to 70°C)

Symbol	Parameter	IDT71216S10 Min.	IDT71216S10 Max.	IDT71216S12 Min.	IDT71216S12 Max.	Unit
MATCH and $\overline{TA}$ Cycles						
t_{ADM}	Address to MATCH Valid	—	10	—	12	ns
t_{DAM}	Data Input to MATCH Valid	—	10	—	12	ns
t_{CSM}	Chip Select to MATCH Valid	—	10	—	12	ns
t_{CMLZ}(1)	Chip Select to MATCH in Low-Z	1	—	1	—	ns
t_{CMHZ}(1)	Chip Select to MATCH in High-Z	1	6	1	7	ns
t_{MHA}	MATCH Valid Hold from Address	2	—	2	—	ns
t_{MHD}	MATCH Valid Hold from Data	2	—	2	—	ns
t_{THA}	$\overline{TA}$ Valid Hold from Address	2	—	2	—	ns
t_{THD}	$\overline{TA}$ Valid Hold from Data	2	—	2	—	ns
t_{ADT}	Address to $\overline{TA}$ Valid	—	11	—	13	ns
t_{DAT}	Data Input to $\overline{TA}$ Valid	—	11	—	13	ns
t_{CST}	Chip Select LOW to $\overline{TA}$ Valid	—	11	—	13	ns
t_{OETV}	$\overline{TAOE}$ LOW to $\overline{TA}$ Valid	—	7	—	8	ns
t_{OTLZ}(1)	$\overline{TAOE}$ LOW to $\overline{TA}$ in Low-Z	0	—	0	—	ns
t_{OTHZ}(1)	$\overline{TAOE}$ HIGH to $\overline{TA}$ in High-Z	1	6	1	7	ns
t_{TAFH}	TAH HIGH to Force $\overline{TA}$ HIGH	—	5	—	6	ns
t_{TAHV}	TAH LOW to $\overline{TA}$ Valid	—	5	—	6	ns
t_{STI}	$\overline{TAIN}$ Set-up Time	4	—	4	—	ns
t_{HTI}	$\overline{TAIN}$ Hold Time	1.5	—	1.5	—	ns
t_{TITL}	CLK HIGH $\overline{TAIN}$ LOW to $\overline{TA}$ LOW	—	7	—	8	ns
t_{TITV}	CLK HIGH $\overline{TAIN}$ HIGH to $\overline{TA}$ Valid	—	7	—	8	ns
t_{OEMI}	$\overline{OET}$ LOW to MATCH and $\overline{TA}$ Invalid	—	7	—	8	ns
t_{OEMV}	$\overline{OET}$ HIGH to MATCH and $\overline{TA}$ Valid	—	8	—	10	ns
t_{THTL}(2)	TT1 LOW to $\overline{TA}$ HIGH	—	7	—	8	ns
t_{THTV}(2)	TT1 HIGH to $\overline{TA}$ Valid	—	7	—	8	ns
t_{WMI}	CLK HIGH Write to MATCH and $\overline{TA}$ Invalid	—	7	—	8	ns
t_{WMV}(3)	CLK HIGH Read to MATCH and $\overline{TA}$ Valid	—	10	—	12	ns

3067 tbl 15

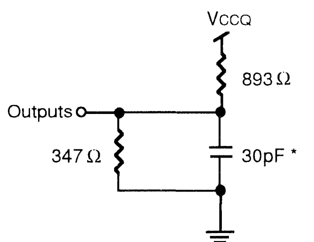
NOTES:
1. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.
2. These parameters only apply when SFUNC is LOW and the internal WT bit is HIGH.
3. t_{ADM}, t_{DAM}, t_{CSM} and t_{ADB}, t_{DAB}, t_{CSB} must also be satisfied.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figs. 1, 2, 3, & 4

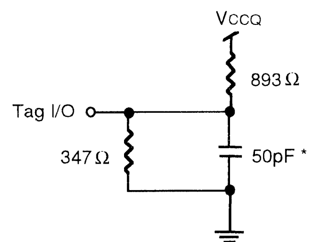
3067 tbl 16

AC TEST LOADS



3067 drw 03

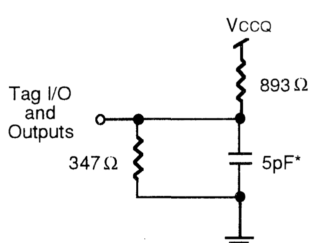
Figure 1. AC Test Load



3067 drw 04

Figure 2. Tag I/O AC Test Load

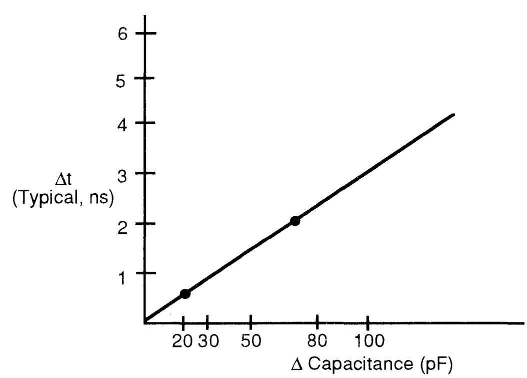
* Including scope and jig capacitance



3067 drw 05

Figure 3. AC Test Load (for tHZ and tLZ parameters)

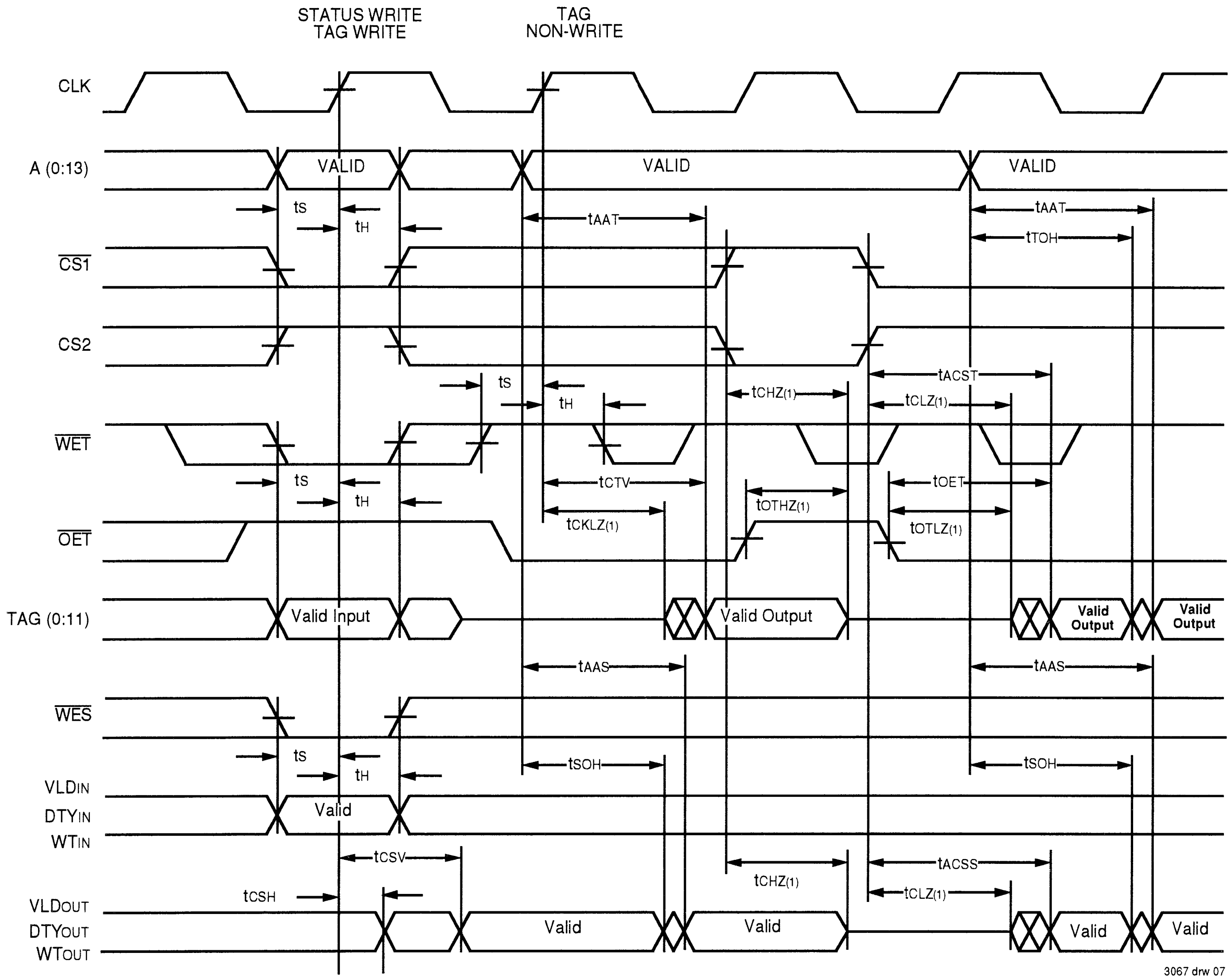
* Including scope and jig capacitance



3067 drw 06

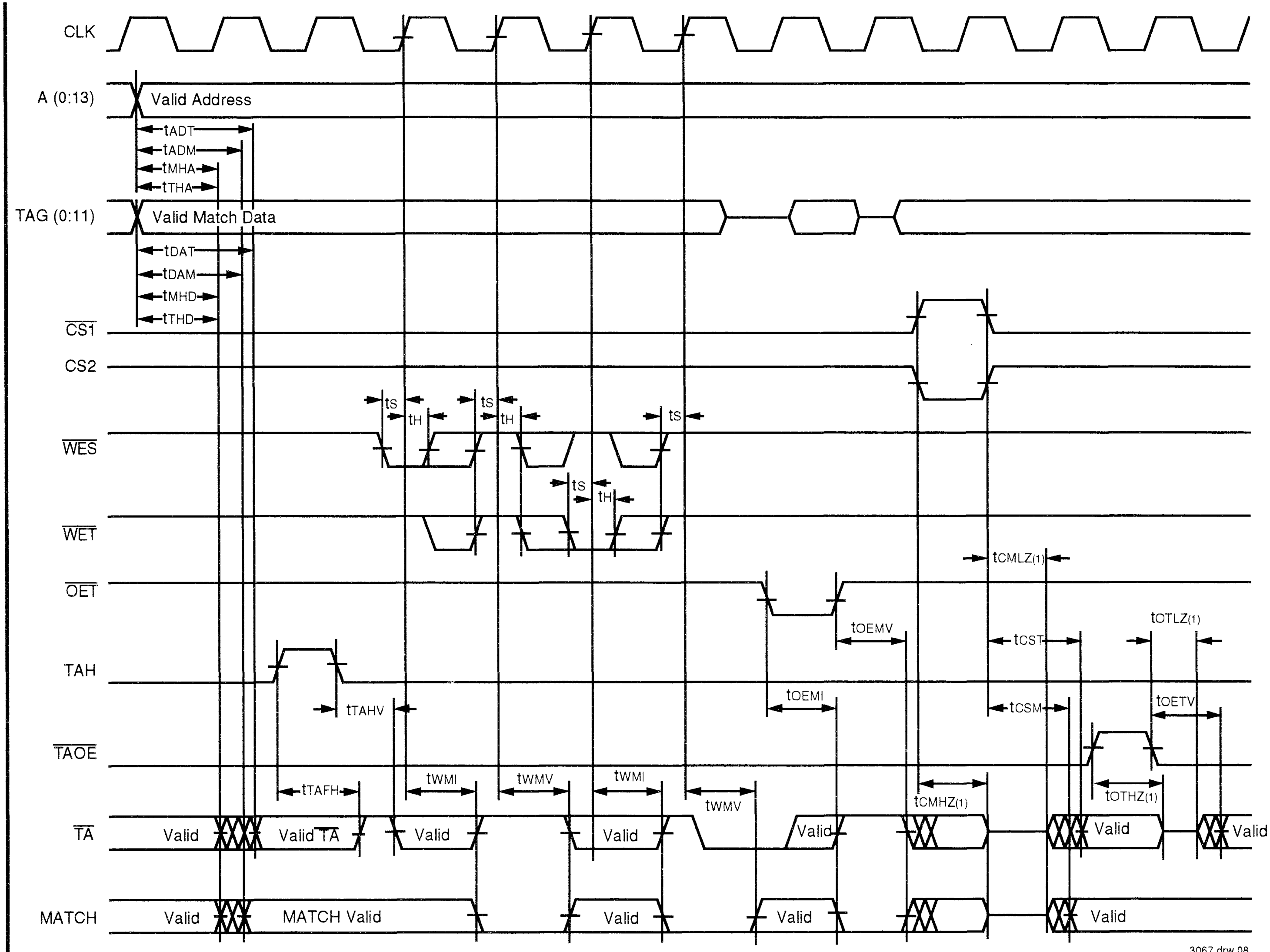
Figure 4. Lumped Capacitance Load, Typical Derating

TIMING WAVEFORMS OF WRITE AND READ CYCLES



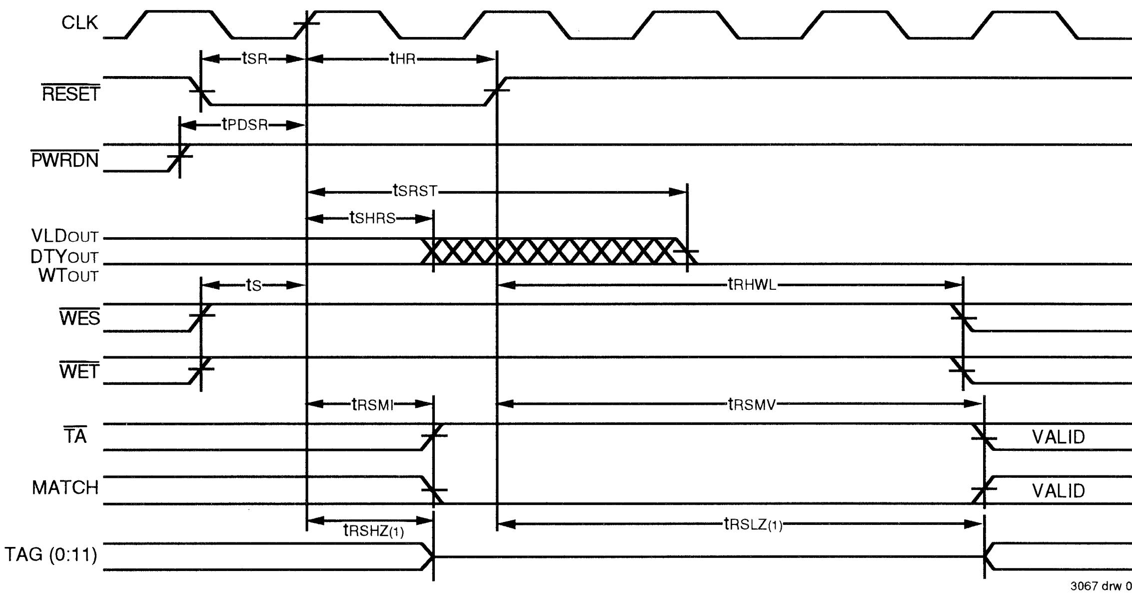
NOTE:
1. Transition is measured ±200mV from steady state.

TIMING WAVEFORMS OF MATCH AND $\overline{TA}$ FUNCTIONS



NOTE:
1. Transition is measured ±200mV from steady state.

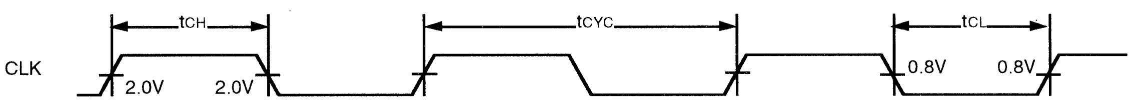
TIMING WAVEFORMS OF $\overline{\text{RESET}}$ FUNCTION



3067 drw 09

NOTE:
1. Transition is measured ±200mV from steady state.

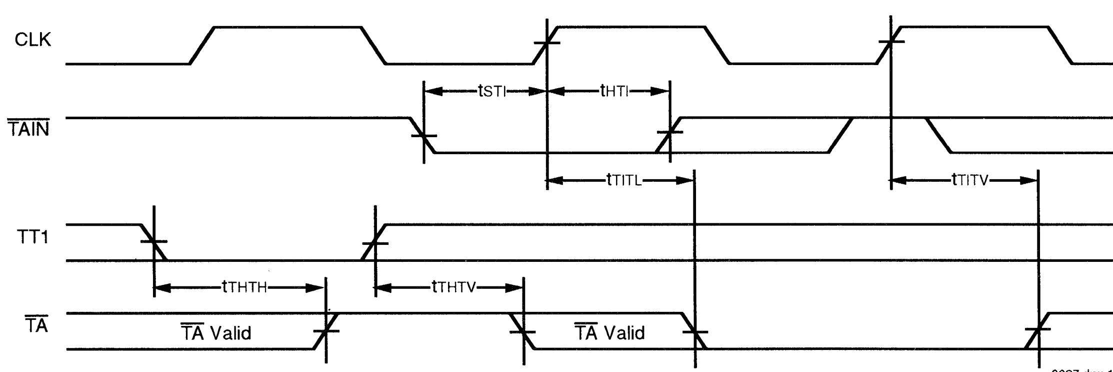
SYSTEM CLOCK TIMING WAVEFORM



3067 drw 10

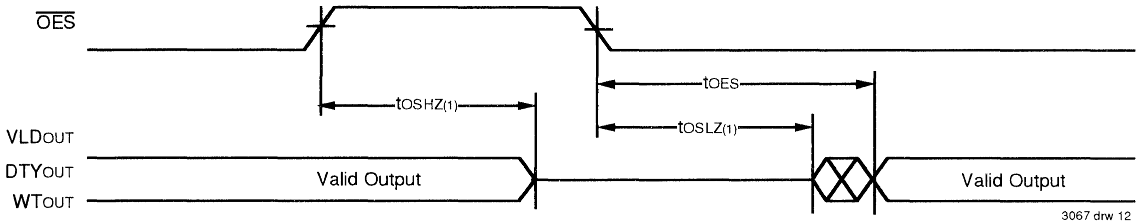
TIMING WAVEFORMS OF $\overline{\text{TA}}$ AND TT1 SIGNAL

Applies when SFUNC is LOW, and the internal WT bit is HIGH



3067 drw 11

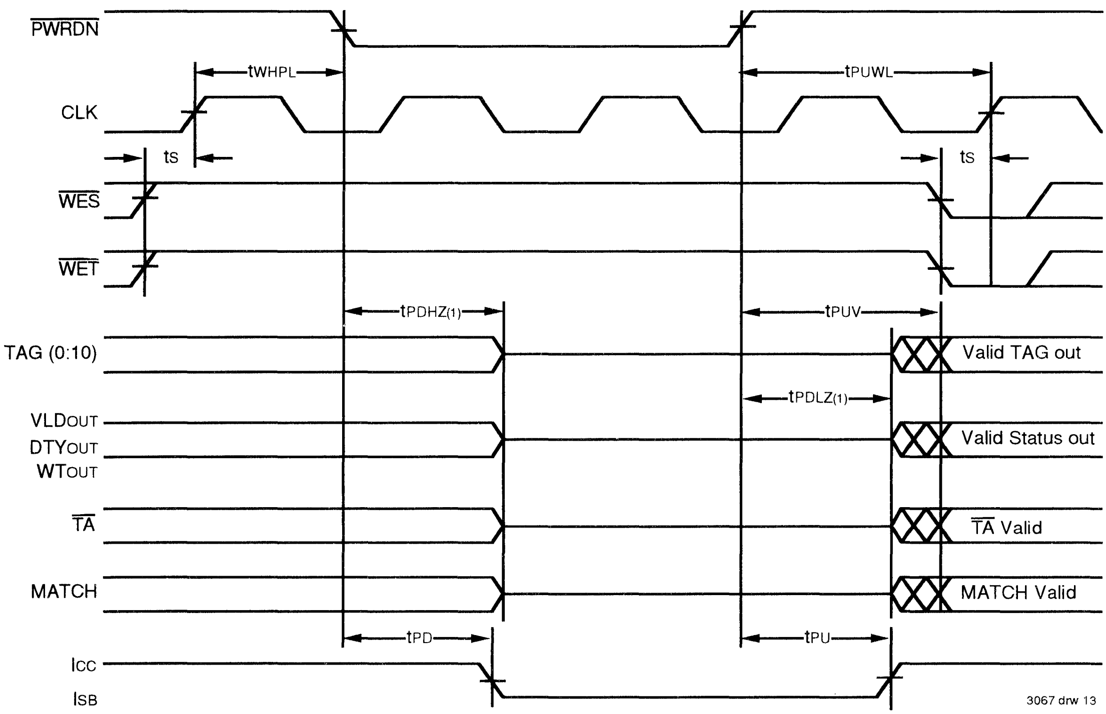
TIMING WAVEFORMS OF $\overline{\text{OES}}$ FUNCTION



3067 drw 12

NOTE:
1. Transition is measured ±200mV from steady state.

TIMING WAVEFORMS OF POWER DOWN FUNCTION



3067 drw 13

NOTE:
1. Transition is measured ±200mV from steady state.

ORDERING INFORMATION

IDT 71216 (Device Type) S (Power) XX (Speed) PF (Package)

Package:
- PF — Plastic Thin Quad Flatpack (PN80-1)

Speed:
- 10, 12 — Speed in nanoseconds

3067 drw 14

CACHE CONTROLLER PRODUCTS

Expanding further on its cache tag and cache design experience, IDT is developing products that will offer improved secondary cache performance at a lower cost to the user. The product concept will combine both the cache tag SRAM and all of the cache controller logic on a single chip to minimize on-and-off chip delays in this critical path.

The first device, the IDT71V280, utilizes IDT's state-of-the-art 3.3V CMOS technology to provide superior cache performance with either burst or asynchronous SRAMs. This device, when utilized with application specific core logic, will provide all control signals for the secondary cache data SRAMs as well as the hit/miss decision back to the processor itself.

Function	Organization	Features	Process	Part Number	Power	Speeds	
						Commercial	Military
Cache Controller	16K x 10	3.3V Controller with Tag	3.3V CMOS	71V280	S	66MHz	N/A

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TABLE OF CONTENTS

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Integrated Device Technology, Inc.

CMOS CACHE CONTROLLER WITH TAG FOR INTEL® PENTIUM™ PROCESSORS

ADVANCE INFORMATION
IDT71V280

FEATURES

- Provides the Cache Tag, Status Bits, CPU interface control and Data SRAM control for Pentium CPU-based systems
- Supports 2-1-1-1 zero-wait state reads and writes for 50MHz Pentium CPU-based systems
- Offers 3-1-1-1 burst performance for 66MHz Pentium CPU-based systems
- Supports a write-back, look aside cache architecture
- 10-bit tag field for up to 512MB cacheable address space using four words per line
- Provides Pentium address pipelining support for optimum burst performance
- Supports cache sizes of 256KB, 512KB, and 1MB
- 2 status bits offer four encoded combinations:
  - Invalid
  - Shared (valid clean, write-through)
  - Exclusive (valid clean, write-back)
  - Modified (valid dirty)
- Supports asynchronous and burst data SRAMs
- 3.3V (±5%) power supply voltage
- Packaged in a 128-lead TQFP for optimum board density

DESCRIPTION

The IDT71V280 provides the Cache Tag SRAM, Status Bits, CPU interface control, and Data SRAM control for a Pentium secondary cache implementation. Combining these elements in a single, cost-effective CMOS chip provides the system designer with greatly enhanced cache performance by reducing cache-subsystem delays. The IDT71V280 provides 2-1-1-1 zero-wait state secondary cache performance at frequencies up to 50MHz and 3-1-1-1 performance at 60 and 66MHz in Pentium applications.

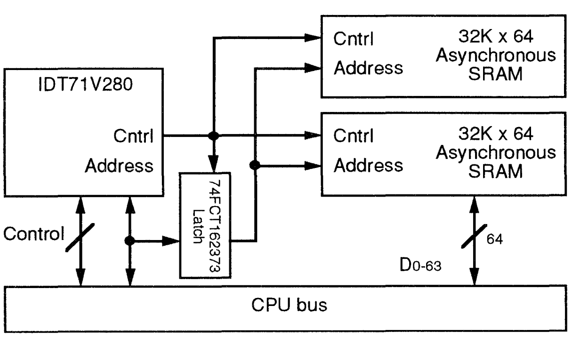
The IDT71V280 supports a number of different system configurations and performance levels. Cache size, cache wait-state performance, Data SRAM type, and Data SRAM size offer the system designer a wide range of cache choices to optimize the cache configuration to his exact system needs. Four mode pins determine the cache subsystem configuration and performance levels, with both asynchronous and burst data SRAM support options offered.

The IDT71V280 uses a single 3.3V power supply to provide full JEDEC LVTTL compatibility in 3.3V applications. Multiple GND pins provide excellent noise immunity at high frequencies, and the space saving 14mm x 20mm 128-pin Thin Quad Flat Pack offers a small board footprint and profile for maximum packing density.

TYPICAL CACHE SUBSYSTEM CONFIGURATIONS

FUNCTIONAL BLOCK DIAGRAM

1. Aynchronous SRAM—Interleaved



FUNCTIONAL DESCRIPTION

When used with two interleaved banks of asynchronous data SRAMs, the IDT71V280 supports zero wait-state bursts on read and write cycles for 50MHz systems and one wait-state bursts at 66MHz. All control for the SRAMs, including separate least significant address bits, are provided by the IDT71V280 to support this configuration.

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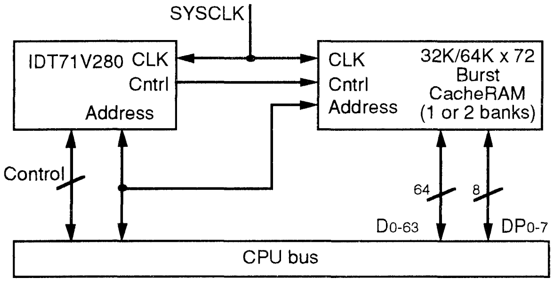
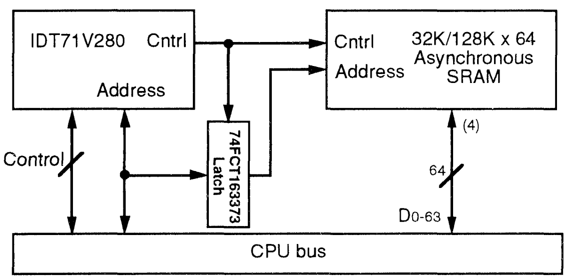
FUNCTIONAL BLOCK DIAGRAM

2. Burst SRAM



3100 drw 02

3. Asynchronous SRAM—Single Bank



3100 drw 03

FUNCTIONAL DESCRIPTION

The IDT71V280 can also be used with Burst CacheRAMs. The IDT71V280 provides all control signals necessary for up to 128K depth of data SRAM, using either one or two banks of data SRAMs. Therefore, all standard burst SRAM configurations may be used including 32K x 18, 32K x 36 and 64K x 18. For 50MHz, 2-1-1-1 zero wait-state operation can be achieved with 12ns burst SRAMs; for 66MHz, the IDT71V280 will operate with Pipelined Burst RAMs providing 3-1-1-1 performance.

The IDT71V280 will support a single bank of asynchronous SRAMs, allowing a minimum cost cache solution. With 15ns SRAMs this configuration provides 2-2-2-2 performance at 50MHz and 3-2-2-2 performance at 66MHz. This configuration will be especially useful for systems requring a minimum part count solution based on power and space constraints.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.15	3.3	3.45	V
GND	Supply Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.0	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 3100 tbl 01
1. V_{IL} (min.) = –1.5V for pulse width of less than 10ns, once per cycle.

CAPACITANCE(1) (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Condition	IDT71V280	Unit
C_{IN}	Input Capacitance (Address, Control)	V_{IN} = 0V	5	pF
C_{IN}	Input Capacitance (CLK)	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance (Control)	V_{IN} = 0V	7	pF
$C_{I/O}$	Data I/O Capacitance	V_{OUT} = 0V	7	pF

NOTE: 3100 tbl 02
1. These parameters are maximum values and guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.5	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to +V_{CC}+0.5	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

NOTES: 3100 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.
2. Vcc terminal only.
3. Input, Output, and I/O terminals; 4.5V maximum.

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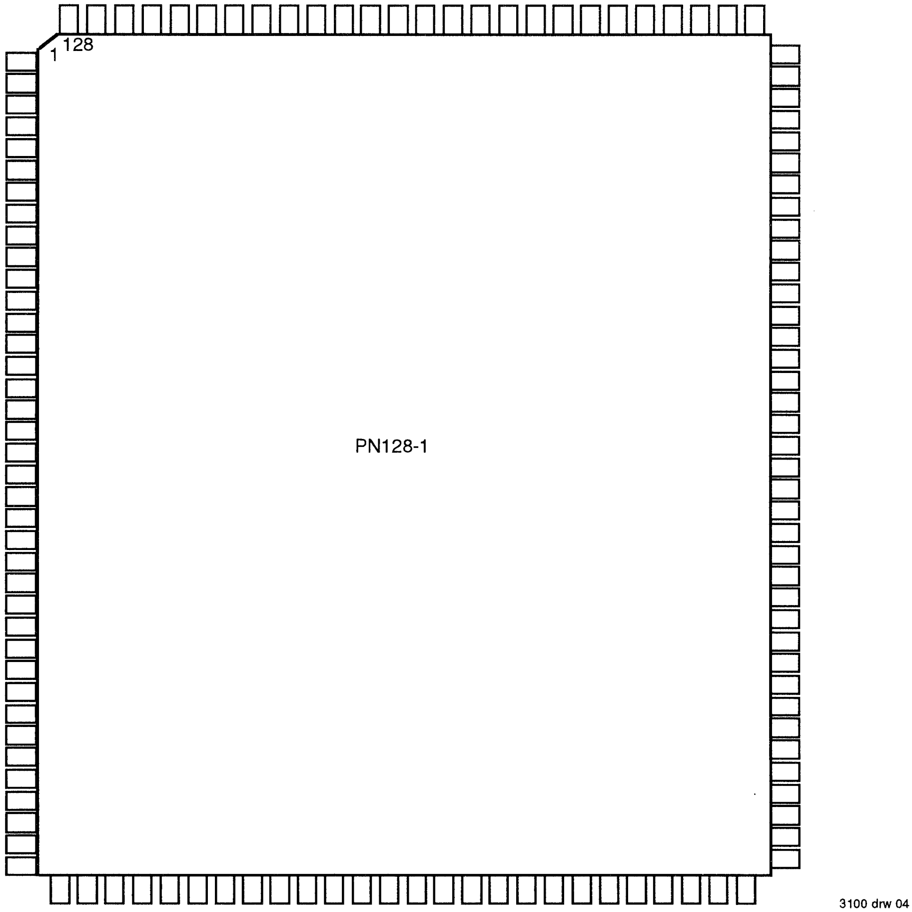
PIN CONFIGURATION



TQFP
TOP VIEW

MODE AND CONFIGURATION TABLE

M3	M2	M1	M0	Performance			Cache Size (B)	SRAM Type[(1)]	Number of Banks	Notes
				Read Hit	Write/BurstWrite	Line Fill				
0	0	0	0	2-2-2-2	2/2-2-2-2	4-2-2-2	256K	32K x 8 A	1	
0	0	0	1	3-2-2-2	3/3-2-2-2	4-2-2-2	256K	32K x 8 A	1	
0	0	1	0	2-1-1-1	2/2-1-1-1	4-1-1-1	512K	32K x 8 A	2	Interleaved
0	0	1	1	3-2-2-2	3/3-2-2-2	4-2-2-2	512K	32K x 8 A	2	Interleaved
0	1	0	0	2-1-1-1	2/2-1-1-1	4-1-1-1	256K	Burst	1	32K deep Burst SRAMs
0	1	0	1	3-1-1-1	3/3-1-1-1	4-1-1-1	256K	Pipe-Burst	1	32K deep Pipelined Burst SRAMs
0	1	1	0	2-1-1-1	2/2-1-1-1	4-1-1-1	512K	Burst	1	64K deep Burst SRAMs
0	1	1	1	3-1-1-1	3/3-1-1-1	4-1-1-1	512K	Pipe-Burst	1	64K deep Pipelined Burst SRAMs
1	0	0	0	2-2-2-2	2/2-2-2-2	4-2-2-2	1M	128K x 8 A	1	
1	0	0	1	3-2-2-2	3/3-2-2-2	4-2-2-2	1M	128K x 8 A	1	
1	0	1	0	2-1-1-1	2/2-1-1-1	4-1-1-1	1M	Burst	2	2 banks of 64K deep Burst SRAMs
1	0	1	1	3-1-1-1	3/3-1-1-1	4-1-1-1	1M	Burst	2	2 banks of 64K deep Pipelined Burst SRAMs
1	1	0	0	—	—	—	—	—	—	Reserved
1	1	0	1	—	—	—	—	—	—	Reserved
1	1	1	0	—	—	—	—	—	—	Reserved
1	1	1	1	—	—	—	—	—	—	Reserved

NOTE:
1. A = Asynchronous.

3100 tbl 04

PIN DEFINITION

Symbol	Pin Function	I/O	Level	Description
CLK	Clock	I	N/A	This is the clock input to the IDT71V280. All timing references for the cache are made with respect to this input. If the clock input is to be disabled, PWRDN# must first be asserted.
PLL	PLL Output	O	N/A	This pin is a free running output that should be loaded the same as the WE# pins and is used to adjust the phase of the internal clock.
RESET	Reset	I	HIGH	If RESET is sampled HIGH by the IDT71V280, the control logic is reset to a known state. In addition, when RESET is sampled HIGH, the resettable status bits are forced to INVALID.
FLUSH#	Flush	I	LOW	When the FLUSH# input is sampled LOW, the IDT71V280 control logic is placed into a flush pending state. While the IDT71V280 is in a flush pending state, it does not alter how it handles CPU bus cycles. The IDT71V280 initiates a cache flush when it detects a CPU Flush Acknowledge special bus cycle.
SBOFF#	System Backoff	I	LOW	This input forces the IDT71V280 off of the CPU address and data buses. When SBOFF# is asserted, the IDT71V280 will only recognize invalidation and snoop cycles; however, the cache will not provide the data and address for an invalidation/snoop hit to a dirty line until SBOFF# is deasserted. When SBOFF# is sampled asserted, it causes the IDT71V280 to assert CBOFF# synchronously.
CBOFF#	Cache Backoff	O	LOW	This output is asserted by the cache to force the CPU off the bus when the IDT71V280 detects that a dirty line must be evicted from the IDT71V280. The IDT71V280 also asserts CBOFF# when its SBOFF# input is sampled asserted.
EADS#	External Address Strobe	I	LOW	This input is used by external devices to perform a snoop to a cache line in the IDT71V280. The IDT71V280 recognizes the initiation of a snoop access when EADS# is sampled LOW. The IDT71V280 ignores ADS# if it is sampled LOW concurrent with sampling EADS# LOW.
INV	Invalidate	I	HIGH	This input is used in conjunction with EADS# to snoop, or invalidate, a cache line. If INV is HIGH, the IDT71V280 will consider the access as an invalidation. If INV is LOW when EADS# is asserted the IDT71V280 will consider the access as a snoop.

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PIN DEFINITION (CONTINUED)

Symbol	Pin Function	I/O	Level	Description
ADS#	Address Strobe	I/O	LOW	This pin is used by external devices to inform the IDT71V280 that a valid address is present on the input of the cache. This pin is driven by the IDT71V280, while the IDT71V280 is asserting CBOFF#, to evict a dirty line from the cache or to supply dirty data for a snoop hit.
NA#	Next Address	I/O	LOW	This pin is driven LOW for one clock cycle by the IDT71V280 during burst read hits to pipeline the next CPU bus cycle into the current one. This pin is an input when the memory controller is servicing the memory cycle.
M/IO#	Memory/I/O	I/O	N/A	This pin is used by external devices to inform the IDT71V280 that a memory access is being made when this pin is HIGH, or that an I/O access is being made when this pin is LOW. I/O cycles are not considered cacheable. This pin is driven HIGH by the IDT71V280, while the IDT71V280 is asserting CBOFF#, to evict a dirty line from the cache or to supply dirty data for a snoop hit.
W/R#	Write/Read	I/O	N/A	This pin is used by external devices to inform the cache that either a write is being performed when this pin is HIGH, or that a read is being performed if this pin is LOW. This pin is driven HIGH by the IDT71V280, while the IDT71V280 is asserting CBOFF#, to evict a dirty line from the cache, or to supply dirty data for a snoop hit.
WRPT#	Write Pass Through	I	LOW	This input from the system is sampled concurrent with the beginning of a CPU bus cycle. If it is sampled LOW, the IDT71V280 passes control of servicing the write cycle to the system controller.
D/C#	Data/Control	I/O	N/A	This pin is used by the IDT71V280 in conjunction with the M/IO#, W/R#, BE_7#-BE_0# to determine when a special bus cycle is being executed, and the type of special bus cycle being executed. This pin is driven HIGH by the IDT71V280, while the IDT71V280 is asserting CBOFF#, to evict a dirty line from the cache or to supply dirty data for a snoop hit.
START#	Memory Start	O	LOW	This output is driven LOW by the IDT71V280 to inform the system that it must service the current memory cycle. START# is also driven LOW when the IDT71V280 is writing back a dirty line from the cache.
CBRDY#	Burst Ready Output	O	LOW	The IDT71V280 drives this signal to the CPU BRDY# at all times. It is driven LOW to indicate the successful transfer of data. CBRDY# is a combination of the internally generated logic (for read hits, and write hits that are not write through), and the SBRDY# input (all cache misses, non-cacheable and write through cycles). There is a register delay in the SBRDY# to CBRDY# path.
SBRDY#	Burst Ready Input	I	LOW	The system drives this signal into the IDT71V280 at all times. It is driven LOW to indicate the successful transfer of data to or from the system. CBRDY# is driven LOW in response to SBRDY# being sampled LOW. The IDT71V280 delays SBRDY# (through CBRDY#) to the CPU by one cycle.
CACHE#	Cacheability	I/O	LOW	This pin is sampled by the IDT71V280 at the beginning of a bus cycle to determine the length and cacheability of the cycle. If CACHE# is LOW at the beginning of a read cycle, the read is cacheable and contains four data words. If CACHE# is HIGH at the beginning of a read cycle, the cycle consists of a single data word. If CACHE# is LOW at the beginning of a write cycle, the CPU will execute a four word write back. If CACHE# is HIGH at the beginning of a write cycle, the CPU will write out a single word. When the IDT71V280 executes a write back to evict a dirty line this pin is driven LOW at the same time that CBOFF# is asserted. This pin is driven LOW when the IDT71V280 is performing a write cycle for either a line eviction, or to supply dirty data for a snoop hit.
A_{31}-A_3	Address	I/O	N/A	These are the CPU address bus lines. They are inputs to the IDT71V280, except when the IDT71V280 is performing a write cycle for either a line eviction or to supply dirty data for a snoop hit.
BE_7#-BE_0#	Byte Enable	I/O	LOW	These are the byte enable inputs to the IDT71V280. These inputs are sampled during write cycles to control byte writes, and they are used in conjunction with M/IO#, W/R#, and D/C# to determine when a special bus cycle is being executed. These pins are driven LOW when the IDT71V280 is performing a write cycle for either a line eviction, or to supply dirty data for a snoop hit.

PIN DEFINITION (CONTINUED)

Symbol	Pin Function	I/O	Level	Description
CS#	Cache Select	I	LOW	This input is used to disable the IDT71V280 from responding to any memory or snoop cycles. The IDT71V280 will not respond to a memory, or snoop, cycle unless it samples CS# LOW the clock cycle prior to and the clock concurrent with sampling either ADS# or EADS# LOW.
CWB/WT#	Write Back/Write Write Cache	O	N/A	Output from the IDT71V280 to the CPU. It is driven to reflect whether data being accessed during a cache hit is write back or write through in nature. CWB/WT# is also driven LOW when SWB/WT# is sampled LOW.
SWB/WT#	Write Back/Write Through System	I	N/A	Input to the IDT71V280 when a line of data is loaded into the cache. If PWT is sampled HIGH at the beginning of a read cycle that results in a cache miss, the value of this pin is ignored and the line returned is considered write through. If PWT is sampled LOW at the beginning of a read cycle, and SWB/WT# is sampled HIGH during the first work transfer of a line fill, the line is marked as write back. If PWT is sampled LOW at the beginning of a read cycle, and SWB/WT# is sampled LOW during the first work transfer of a line fill, the line is marked as write through. If the line is marked as write back, the cache will update its memory contents without passing the cycle on to other devices during a memory write cycle. If the line is marked as write through, the cache will update its memory contents when the write cycle is serviced by the system. When SWB/WT# is sampled LOW, it forces CWB/WT# LOW synchronously.
HITM#	Hit-Modified Input	I	LOW	This input is used to indicate to the IDT71V280 that a dirty line is hit in the CPU level 1 cache during inquire (snoop or invalidate) cycles. When HITM# is sampled asserted, it causes the IDT71V280 to assert CHITM# synchronously.
CHITM#	Hit-Modified Output	O	LOW	IDT71V280 asserted output to indicate that an inquire (snoop or invalidate) cycle hits a dirty line in the cache. The IDT71V280 also asserts CHITM# when its HITM# input is asserted.
MOD#	Modified Line	O	LOW	Output asserted by the IDT71V280 to indicate that a dirty line is being accessed during a memory read or write bus cycle. MOD# does not depend on hit or miss status.
SKEN#	Cacheable Data Input	I	LOW	This pin is sampled by the IDT71V280 to determine whether the data being returned during a read miss is cacheable. SKEN# must be sampled LOW at least one cycle before the first word is transferred to the cache. During Reset, SKEN# is used to indicate to the IDT71V280 whether write allocation is enabled or disabled. If asserted, write alloction is enabled.
PWT	Page Write Through	I/O	HIGH	This input is sampled by the IDT71V280 at the initiation of memory read and write cycles. If PWT is sampled HIGH at the initiation of a memory read that results in a cache miss, the line returned is automatically considered write through. If PWT is sampled HIGH at the initiation of memory write cycle, the cache ignores the value of its internal write back/write through flag, and it is forced to treat the write cycle as write through. The IDT71V280 drives this pin LOW, while CBOFF# is asserted, when the IDT71V280 executes a write cycle to evict a dirty line from the cache or to supply dirty data for a snoop hit.
HLDA	Bus Hold Acknowledge	I	HIGH	Connects to the HLDA output pin from the CPU, which is used to acknowledge a bus hold request from HOLD. Except when the IDT71V280 is performing a write back operation, HLDA will propagate through to CHLDA with a one cycle delay. When the IDT71V280 is performing a write back operation, it will block the propagation of HLDA until it has released control of the bus.
CHLDA	Bus Hold Acknowledge	O	HIGH	Typically reflects HLDA input delayed by one clock cycle. However, the IDT71V280 will force CHLDA LOW while it is performing a write back operation. Once the IDT71V280 has released SBOFF#, it will allow CHLDA to be asserted.
LOCK#	Lock	I/O	LOW	If LOCK# is sampled LOW at the beginning of a read cycle and the data in the cache is not dirty, the read cycle is treated as a non-cacheable read miss. If the cache contains dirty data at the address location requested by the locked read cycle, the IDT71V280 first evicts the dirty line, then the read cycle is treated as a non-cacheable read miss. If LOCK# is sampled LOW at the beginning of a write cycle, the IDT71V280 ignores its internal write back/write through flag, and treats the write cycle as write through. The IDT71V280 drives

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PIN DEFINITION (CONTINUED)

Symbol	Pin Function	I/O	Level	Description
				this pin HIGH, while CBOFF# is asserted, when it executes a write cycle to evict a dirty line from the cache or to supply dirty data for a snoop hit.
OEA#(0:1), OEB#(0:1)	Data RAM Output Enable	O	LOW	These pins are used to assert output enable of the data SRAMs, two for each bank of SRAMs.
WE7#- WE0#	Data RAM Write Enable	O	LOW	These pins are used to assert Write Enable of the data SRAMs, one for each byte.
CEA#(0:1), CEB#(0:1)	Data RAM Chip Enable	O	LOW	These pins are used to assert Chip Enable of the data SRAMs, one for each bank of SRAMs.
ADV#	Data RAM Adv	O	LOW	This pin is used with burst SRAMs to advance the internal address counter
AD3/4A(0:1), AD4/4B(0:1)	Data RAM Address	O	N/A	These pins are the least significant two address lines of the data AD4/4B(0:1) SRAMs when asynchronous SRAMs are used. When one bank of SRAMs is used these pins are AD3 and AD4. If two banks of interleaved SRAM are used these pins are AD4A and AD4B; that is, the least significant address of the odd bank and the even bank.
ALE/ ADSC#	Address LE/ Controller ADS#	O	LOW	This pin is used to latch the CPU address into external latch(es) for the asynchronous data SRAMs, and is ADSC# when a burst SRAM implementation is used.
MODE (0:3)	Mode Select	I	N/A	These pins are used to select the mode in which the IDT71V280 operates and are not allowed to change once the IDT71V280 is powered up.
PWRDN#	Power Down	I	LOW	This pin is used to force the IDT71V280 into a Low Power Mode while retaining data. As long as this input is asserted the IDT71V280 will not initiate any new activity. After this input is negated, the IDT71V280 will respond normally within 1ms.
Vcc	Power	N/A	N/A	Power supply inputs for the IDT71V280.
GND	Ground	N/A	N/A	Ground pins of the IDT71V280.

3100 tbl 05

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