intel. ®

82443BX Host Bridge/Controller Electrical and Thermal Specification

Timing Specification

Product Features

Datasheet Addendum

- Processor/host bus support
  - Optimized for Pentium® II processor at 100 MHz system bus frequency; Support for 66 MHz
  - Supports full symmetric Multiprocessor (SMP) Protocol for up to two processors; I/O APIC related buffer management support (WSC# signal)
  - In-order transaction and dynamic deferred transaction support
  - Desktop optimized GTL+ bus driver technology (gated GTL+ receivers for reduced power)
- Integrated DRAM controller
  - 8 to 512 Mbytes or 1 G (with registered DIMMs)
  - Supports up to 4 double-sided DIMMs (8 rows memory)
  - 64-bit data interface with ECC support (SDRAM only)
  - Unbuffered and Registered SDRAM (Synchronous) DRAM Support (x-1-1-1 access at 66 MHz, x-1-1-1 access at 100 MHz)
  - Enhanced SDRAM Open Page Architecture Support for 16- and 64-Mbit DRAM devices with 2-, 4- and 8-Kbyte page sizes
- PCI bus interface
  - PCI Rev. 2.1, 3.3 V and 5 V, 33 MHz interface compliant
  - PCI Parity Generation Support
  - Data streaming support from PCI to DRAM
  - Delayed Transaction support for PCI-DRAM Reads
  - Supports concurrent CPU, AGP and PCI transactions to main memory

- AGP interface
  - Supports single AGP compliant device (AGP-66/133 MHz 3.3 V device)
  - AGP Specification Rev 1.0 compliant
  - AGP-data/transaction flow optimized arbitration mechanism
  - AGP side-band interface for efficient request pipelining without interfering with the data streams
  - AGP-specific data buffering
  - Supports concurrent CPU, AGP and PCI transactions to main memory
  - AGP high-priority transactions ("expedite") support
- Power Management Functions
  - Stop Clock Grant and Halt special cycle translation (host to PCI Bus)
  - Mobile and "Deep Green" Desktop support for system suspend/resume (i.e., DRAM and power-on suspend)
  - Dynamic power down of idle DRAM rows
  - SDRAM self-refresh power down support in suspend mode
  - Independent, internal dynamic clock gating reduces average power dissipation
  - Static STOP CLOCK support
  - Power-on Suspend mode
  - Suspend to DRAM
  - ACPI compliant power management
- Packaging/Voltage
  - 492 Pin BGA
  - 3.3 V core and mixed 3.3 V and GTL I/O
- Supporting I/O Bridge
  - System Management Bus (SMB) with support for DIMM Serial Presence Detect (SPD)
  - PCI-ISA Bridge (PIIX4E)
  - Power Management Support
  - 3.3 V core and mixed 5 V, 3.3 V I/O and interface to the 2.5 V CPU signals via open-drain output buffers

intel®

Datasheet Addendum

Contents

Figures

Tables

Revision History

Revision	Date	Notes
001	December 1998	First release of this document.

1.0   Introduction

This document contains the Electrical and Thermal Specifications (ETS) for the Intel® 440BX AGPset. Specifically, this document refers to the 440BX PCI Accelerated Graphics Port (AGP)-Compliant Controller (82443BX). The 440BX AGPset is designed to provide a high performance memory, AGP, and I/O subsystem for the Deschutes processor-based systems.

1.1   Related Documents

Table 1.   Related Intel Documents

Document	Order Number
Intel® 440BX AGPset Desktop Design Guide	290634
Intel® 440BX AGPset Design Guide Update	290641
CK97 Clock Synthesizer Design Guidelines	243867
100 MHz GTL+ Layout Guidelines for the Pentium® II Processor and Intel® 440BX AGPset Application Note	243735
Intel® 440BX AGPset: 82443BX Host Bridge/Controller datasheet	290633

2.0   Electrical Characteristics

The system bus introduces a variation of the low voltage Gunning Transceiver Logic (GTL) for signaling. For further information, refer to the *100 MHz GTL+ Layout Guidelines for the Pentium® II Processor and Intel® 440BX AGPset* Application Note (order number 243735).

For reliable operation, unused input pins must be tied to an appropriate signal level. Ensure that GTL+ inputs are connected to VTT. Unused active low 3.3 V tolerant inputs should be connected to 3.3 V. Unused active high inputs should be connected to ground (VSS).

2.1 Absolute Maximum Ratings

Table 2. Absolute Maximum DC Ratings

Parameter	Maximum Rating
Case Temperature under Bias	0°C to +105°C (no heat sink)
Storage Temperature	-55°C to +150°C
Voltage on GTL+ Tolerant Pins with Respect to Ground	-0.3 to VTT + 0.3 V
Voltage on 3.3 V Tolerant Pins with Respect to Ground	-0.3 to VCC + 0.3 V
Voltage on PCI and 5.0 V Tolerant Pins with Respect to Ground	-0.3 to VCC$_{PCI}$ + 0.3 V
3.3 V Supply Voltage with Respect to Vss (Vcc)	-0.3 to + 4.3 V
5.0 V Supply Voltage with Respect to Vss (5V_BIAS)	-0.5 to + 6.5 V

NOTES:
1. VCCPCI is the voltage level on the PCI bus. PCI AC characteristics conform to the PCI specification.
2. VCCAGP is the voltage level on the AGP bus. AGP operating conditions conform to the AGP specification.

Warning: *Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. These are stress ratings only. Operation beyond the Operating Conditions is not recommended and extended exposure beyond the Operating Conditions may affect device reliability.*

2.2 Thermal Characteristics

The 82443BX is designed for operation at case temperatures between 0°C and 105°C. The thermal resistance of the package is given in Table 3.

Table 3. 82443BX Package Thermal Resistance

Parameter	Air Flow Meters/Second (Linear Feet per Minute)	
	0 (0)	1.0 (196.9)
θ_{jc} (°C/W)[1]	7.5	N/A
ψ_{jt} (°C/W)[2]	1.1	1.7
θ_{ja} (°C/W)[2]	17.5	15.0

NOTES:
1. Typical value measured using single infinite heat sink method.
2. Typical value measured in accordance with EIA/JESD 51-2 testing standard.

2.3 Power Characteristics

Table 4. 82443BX DC Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
P_{BX}	82443BX Maximum Power Dissipation	4.8	7.3	W	1
I_{LEAK}	5.0 V to 3.3 V Power Supply Leakage Current		20	µA	2
I_{DDQ}	82443BX Quiescent Power Supply Current		20	mA	3
I_{Vtt-BX}	82443BX Maximum V_{tt} Supply Current		6.6	A	4
I_{CC-BX}	82443BX Maximum Power Supply Current		4	A	5

NOTES:
1. This specification is a combination of core power (I_{CC}) and power dissipated in the GTL+ outputs and I/O. The maximum power dissipation is a function of the microprocessor used and DRAM loading. For more information, contact your Intel Field Sales Representative.
2. This parameter is specified at V_{CC5} (5 V_BIAS) – $V_{CC3} \leq 2.25$ V.
3. This is the maximum supply current consumption when all interfaces are idle and the clock inputs are turned off.
4. The I_{VTT} specification is the maximum V_{tt} supply current consumption when all GTL+ signals are low.
5. The I_{CC} specification does not include the GTL+ output current to ground.

2.4 Signal Groups

To ease discussion of the AC and DC characteristics, the signals on the 82443BX have been combined into groups with similar characteristics. These signal groups are referenced throughout this document.

Table 5. 82443BX Signal Groups (Sheet 1 of 2)

Signal Group	Signal Type	Signals
(a)	GTL+I/O	HA[31:3]#, KD[63:0]#, ADS#, BNR#, DBSY#, DRDY#, HIT#, HITM#, HREQ[4:0]#, HTRDY#, RS[2:0]#
(b)	GTL+Output	CPURST#, BPRI#, DEFER#, BREQ0#
(c)	GTL+Input	HLOCK#
(d)	CMOS Input	PCLKIN
(e)	CMOS (2.5V) Input	HCLKIN
(f)	CMOS I/O	RASA[5:0]#/CSA[5:0]#, RASB[5:0]#/CSB[5:0]#, CKE[3:2]/CSA[7:6]#, CKE[5:4]/CSB[7:6]#, CASA[7:0]#/DQMA[7:0], CASB[1,5]#/DQMB[1,5], SRAS[B:A]#, SCAS[B:A]#, MAA[13:0], MAB[13;11,9:0]#, MAB10, WE[B:A]#, CKE0/FENA, CKE1/GCKE, PCIRST#, TESTIN#, SUSCLK, SUSTAT#, MD[63:0], MECC[7:0], WSC#, BXPWROK, CRESET#
(g)	CMOS Output	DCLKO, GCLKO
(h)	PCI Output	PHLDA#, PGNT[4:1]#, PGNT0#/IOREQ#
(i)	PCI I/O 5.0 V Tolerant	AD[31:0], DEVSEL#, FRMAE#, IRDY#, C/BE[3:0]#, PAR, PLOCK#, TRDY#, STOP#
(j)	PCI Input 5.0 V Tolerant	PHOLD#, PREQ[4:1]#, PREQ0#/IOREQ#
(k)	GTL Reference	GTL_REF[B:A]
(l)	AGP Input	PIPE#, SBA[7:0], SB_STB, G_REQ#

Table 5.   82443BX Signal Groups (Sheet 2 of 2)

Signal Group	Signal Type	Signals
(m)	AGP Output	ST[2:0], G_GNT#
(n)	AGP I/O	G_AD[31:0], G_DEVSEL#, G_FRAME#, G_IRDY#, G_TRDY#, G_C/BE[3:0]#, G_PAR, G_STOP#, AD_STB[B:A]
(o)	AGP Reference	AGPREF
(p)	GTL+Termination Voltage	VTT[B:A]
(q)	PCI 5 V Reference	REFVCC5
(r)	PCI Open Drain (3.3 V)	CLKRUN#, SERR#
(s)	CMOS Input	GCLKIN, DCLKWR

2.5   DC Characteristics

Table 6.   82433BX DC Characteristics (Sheet 1 of 3)

Functional Operating Range (V_{CC} = 3.3 V $\pm$5%, T_{CASE} = 0° C to +105° C[4])

Symbol	Signal Group	Parameter	Min	Max	Unit	Notes
V_{IL1}	(d),(e),(f),(s)	CMOS Input Low Voltage	-0.3	0.8	V	1
V_{IH1}	(d),(f),(s)	CMOS Input High Voltage	2.0	V_{CC} + 0.3	V	1
V_{IL2}	(i),(j)	PCI Input Low Voltage	-0.3	0.8	V	1
V_{IH2}	(i),(j)	PCI Input High Voltage	2.0	V_{CC} + 0.3	V	1
V_{IL3}	(a),(c)	GTL+ Input Low Voltage	-0.3	V_{REF} - 0.2	V	2
V_{IH3}	(a),(c)	GTL+ Input High Voltage	V_{REF} + 0.2	1.835	V	2
V_{IL4}	(n),(l)	AGP Input Low Voltage	-0.5	$0.3V_{CC}$	V	1
V_{IH4}	(n),(l)	AGP Input High Voltage	$0.5V_{CC}$	V_{CC} + 0.5	V	1
V_{IL5}	(r)	PCI (3.3 V) Open Drain Input Low Voltage	-0.3	0.8	V	1
V_{IH5}	(r)	PCI (3.3 V) Open Drain Input High Voltage	2.0	V_{CC} + 0.3	V	1
AGPREF	(o)	AGP Reference Voltage	1.18	1.45	V	
GTL_REFd	(k)	GTL+ Reference Voltage (desktop)	$2/3V_{TT}$ - 2%	$2/3V_{TT}$ + 2%	V	
GTL_REFm	(k)	GTL+ Reference Voltage (mobile)	$5/9V_{TT}$ - 2%	$5/9V_{TT}$ + 2%	V	
VTTd	(p)	GTL+Termination Voltage (desktop)	1.365	1.635	V	

NOTES:
1. During transitions, the inputs may overshoot beyond max VCC or undershoot below VSS by 0.8V for 7.0 ns on the 440BX inputs, with a maximum instantaneous overshoot/undershoot of ±1.6V.
2. During transitions, the inputs may overshoot/undershoot beyond VTTmax or below VSS by ±0.3 V (violating the overshoot/undershoot guideline is ok, but it will make satisfying the ringback specification very difficult). Maximum rising edge ringback is 1.12 V. Maximum falling edge ringback is 0.88 V.
3. Parameter correlated into a 120 ohm resistor.
4. Tcase = 0° C to 105° C is without a heat sink.

Table 6.   82433BX DC Characteristics (Sheet 2 of 3)

Functional Operating Range (V_{CC} = 3.3 V $\pm$5%, T_{CASE} = 0° C to +105° C[(4)])

Symbol	Signal Group	Parameter	Min	Max	Unit	Notes
VTTm	(p)	GTL+Termination Voltage (mobile)	1.465	1.835	V	
REFVCC5	(q)	5 V Reference	4.5	5.5	V	
VOL1	(f),(g)	CMOS Output Low Voltage		0.4	V	
VOH1	(f),(g)	CMOS Output High Voltage	2.4		V	
VOL2	(h),(i)	PCI Output Low Voltage		0.4	V	
VOH2	(h),(i)	PCI Output High Voltage	2.4		V	
VOL3d	(a),(b)	GTL+ Output Low Voltage (desktop)		0.6	V	
VOL3m	(a),(b)	GTL+ Output Low Voltage (mobile)		0.6	V	3
VOL4	(m),(n)	AGP Output Low Voltage		$0.1V_{CC}$	V	
VOH4	(m),(n)	AGP Output High Voltage	$0.9V_{CC}$		V	
VOL5	(r)	PCI Open Drain Output Low Voltage		0.4	V	
IOL1	(f),(g)	CMOS Output Low Current		3	mA	
IOH1	(f),(g)	CMOS Output High Current	-2		mA	
IOL2	(h),(i)	PCI Output Low Current		3	mA	
IOH2	(h),(i)	PCI Output High Current	-2		mA	
IOL3d	(a),(b)	GTL+ Output Low Current (desktop)		36	mA	
IOL3m	(a),(b)	GTL+ Output Low Current (mobile)		22	mA	
IIL1	(d),(i),(j),(s)	Input Leakage Low Current		-10	µA	
IIH1	(d),(i),(j),(s)	Input Leakage High Current		+10	µA	
IIL2	(l)	AGP Input Low Leakage Current		±10	µA	$0<V_{IN}<V_{CC}$
IIH2	(l)	AGP Input High Leakage Current		70	µA	V_{IN}=2.7 V
CIN1	(j),(l)	Input Capacitance		4	pF	F_C = 1 MHz
CIN2	(e)	HCLKIN	6.4	9.8	pF	F_C = 1 MHz
CIN3		GCLKIN	6.3	9.6	pF	F_C = 1 MHz

NOTES:
1. During transitions, the inputs may overshoot beyond max VCC or undershoot below VSS by 0.8V for 7.0 ns on the 440BX inputs, with a maximum instantaneous overshoot/undershoot of ±1.6V.
2. During transitions, the inputs may overshoot/undershoot beyond VTTmax or below VSS by ±0.3 V (violating the overshoot/undershoot guideline is ok, but it will make satisfying the ringback specification very difficult). Maximum rising edge ringback is 1.12 V. Maximum falling edge ringback is 0.88 V.
3. Parameter correlated into a 120 ohm resistor.
4. Tcase = 0° C to 105° C is without a heat sink.

Table 6.   82433BX DC Characteristics (Sheet 3 of 3)

Functional Operating Range (V$_{CC}$ = 3.3 V ±5%, T$_{CASE}$ = 0° C to +105° C$^{(4)}$)

Symbol	Signal Group	Parameter	Min	Max	Unit	Notes
CIN4		DCLKWR	7.4	11.1	pF	F$_C$ = 1 MHz
CIN5	(f)	MD[63:0]	6.5	10.6	pF	F$_C$ = 1 MHz
CIN6		PCLKIN	7.7	11.6	pF	F$_C$ = 1 MHz
COUT	(f)	Output Capacitance	6.6	11.3	pF	F$_C$ = 1 MHz
COUT		DCLKO	6.6	10.1	pF	F$_C$ = 1 MHz
CI/O	(i)	I/O Capacitance	6.7	10.3	pF	F$_C$ = 1 MHz
CI/O	(n)	I/O Capacitance	6.5	10.5	pF	F$_C$ = 1 MHz
CI/O	(a)	I/O Capacitance	3.5	7.0	pF	F$_C$ = 1 MHz

NOTES:
1. During transitions, the inputs may overshoot beyond max VCC or undershoot below VSS by 0.8V for 7.0 ns on the 440BX inputs, with a maximum instantaneous overshoot/undershoot of ±1.6V.
2. During transitions, the inputs may overshoot/undershoot beyond VTTmax or below VSS by ±0.3 V (violating the overshoot/undershoot guideline is ok, but it will make satisfying the ringback specification very difficult). Maximum rising edge ringback is 1.12 V. Maximum falling edge ringback is 0.88 V.
3. Parameter correlated into a 120 ohm resistor.
4. Tcase = 0° C to 105° C is without a heat sink.

2.6   AC Characteristics

All timings are in nanoseconds (ns), unless otherwise specified. In addition, all clock-to-output values are specified at a 0 pF load unless otherwise specified.

Table 7.   Host Clock Timing; 66 MHz and 100 MHz (Sheet 1 of 2)

Symbol	Parameter	66 MHz		100 MHz		Fig.	Unit	Notes
		Min	Max	Min	Max			
HCLKIN								
t1a	HCLKIN Period	15	15.5	10	10.5	1	ns	
t1b	HCLKIN Period Stability		±300		±250	1	ps	
t1c	HCLKIN High Time	5.3		3.1		1	ns	measured at 1.7 V for 66 MHz and 100 MHz
t1d	HCLKIN Low Time	5.3		2.8		1	ns	measured at 0.7 V for 66 MHz and 100 MHz

NOTES:
1. AC specifications are measured at the 440BX.
2. Not 100% tested. Specified by design characterization as a clock driver requirement.

intel®

Table 7.   Host Clock Timing; 66 MHz and 100 MHz (Sheet 2 of 2)

Symbol	Parameter	66 MHz		100 MHz		Fig.	Unit	Notes
		Min	Max	Min	Max			
t1e	HCLKIN Rise Time	0.25	1.25	0.25	1	1	ns	0.7 V – 1.7 V for 66 MHz and 100 MHz (2)
t1f	HCLKIN Fall Time	0.25	1.25	0.25	1	1	ns	1.7 V – 0.7 V for 66 MHz and 100 MHz (2)
DCLKO								
t2a	DCLKO Period	15	15.5	10	10.5	2	ns	
t2b	DCLKO Period Stability		±350		±350		ps	
t2c	DCLKO High Time	7.1		4.6		2	ns	
t2d	DCLKO Low Time	6.8		4.2		2	ns	
t2e	DCLKO Slew Rate	2	6	2	6	2	V/ns	
DCLKWR								
t3a	DCLKWR Period	15	15.5	10	10.5	2	ns	
t3b	DCLKWR Period Stability		±550		±550		ps	
t3c	DCLKWR High Time	6		3		2	ns	
t3d	DCLKWR Low Time	6		3		2	ns	
t3e	DCLKWR Slew Time	0.8	4	0.8	4.0	2	V/ns	
t3g	DCLKWR Duty Cycle	40%	60%	40%	60%	3		
GCLKO								
t4a	GCLKO Period	15	15.5	NA	NA	2	ns	
t4b	GCLKO Period Stability		±350		NA		ps	
t4c	GCLKO High Time	7.1		NA		2	ns	
t4d	GCLKO Low Time	6.8		NA		2	ns	
t4d	GCLKO Slew Rate	2	6	NA	NA	2	V/ns	
GCLKIN								
t5a	GCLKIN Period	15	15.5	NA	NA	2	ns	
t5b	GCLKIN Period Stability		±350		NA		ps	
t5c	GCLKIN High Time	6		NA		2	ns	
t5d	GCLKIN Low Time	6		NA		2	ns	
t5e	GCLKIN Slew Rate	1	5	NA	NA	2	V/ns	
t5g	GCLKIN Lead Time to GCLKIN	0.5	3.0	NA	NA		ns	

NOTES:
1. AC specifications are measured at the 440BX.
2. Not 100% tested. Specified by design characterization as a clock driver requirement.

Table 8.   CPU Interface Timing; 60 MHz and 100 MHz

Functional Operating Range (V_{TT} = 1.5 V $\pm$9%, V_{CC} = 3.3 V $\pm$5%; T_{CASE} = 0° C to +105[(4)]° C)

Symbol	Parameter	66 MHz (mobile)		100 MHz (mobile)		100 MHz (desktop)		Fig.	Unit	Notes
		Min	Max	Min	Max	Min	Max			
t7	Valid Delay from HCLKIN Rising (tco)	1.10	10	0.9	4.45	0.9	4.45	4	ns	1, 2, 3
t8	Input Setup Time to HCLKIN Rising (tsu)	3.0		3.0		3.0		5	ns	1, 2, 3
t9	Input Hold Time from HCLKIN Rising (thld)	-100		-100		-100		5	ps	

NOTES:
1. Mobile valid delays are specified into a 120 ohm resistor which is tied to VTT = 1.7 V.
2. Desktop valid delays are spedified into a 25 ohm resistor which is tied to VTT = 1.5 V.
3. Mobile valid delays are specified into a 56 ohm resistor which is tied to VTT = 1.5 V.
4. T_{CASE} = 0° C to + 105° C is without a heat sink.

Table 9.   100 MHz Memory Interface Timing (Sheet 1 of 2)

Functional Operating Range (V_{CC} = 3.3 V $\pm$5%, T_{CASE} = 0° C to +105° C[(7)], C_L = 0 pF)

Symbol	Parameter	1x Buffer		2x Buffer		3x Buffer		Fig.	Notes
		Min	Max	Min	Max	Min	Max		
t10a	WE[B:A]# Valid Delay from DCLKWR (for the first chip select)	1.25	18.31	1.19	18.18	1.19	18.13	4	1,3,4,5,6
t11a	WE[B:A]# Valid Delay from DCLKWR Rising (for the subsequent chip selects)	1.25	8.51	1.19	8.38	1.19	8.33	4	2,3,4,5,6
t12a	MAA[13:0], MAB[13;11,9:0]#, MAB10 Valid Delay from DCLKWR (first chip select of an access)	1.25	18.31	1.19	18.18	1.50	18.13	4	1,3,4,5,6
t13a	MAA[13:0], MAB[13;11,9:0]#, MAB10 Valid Delay from DCLKWR Rising, SDRAM Read/Write cycles (for the subsequent chip selects)	1.25	8.51	1.19	8.38	1.9	8.33	4	2,3,4,5,6
t14a	SRAS[B:A]# Valid Delay from DCLKWR (first chip select of an access)	1.25	18.31	1.19	18.18	1.50	18.13	4	1,3,4,5,6
t15a	SRAS[B:A]# Valid Delay from DCLKWR Rising (subsequent chip selects)	1.25	8.51	1.19	8.38	1.9	8.33	4	2,3,4,5,6

NOTES:
1. Symbols t10a, t12a, t14a, and t16a are based on a 3-clock cycle valid delay.
2. Symbols t11a, t13a, t15a, and t17a are based on a 2-clock cycle valid delay.
3. Two valid delays apply to these command singals. The longer valid delay applies to command signals setup to the first chip select of an access. The second valid delay applies command signals setup to subsequent chip selects in the access. However, in a pipelined access, the shorter valid delay applies to command signals setup to the first chip select.
4. All measurements are in ns, unless otherwise specified.
5. The choice of 100 MHz or 66 MHz buffers is independent of bus frequency. It is possible to select a 100 MHz memory buffer even though the bus frequency is 66 MHz (and vise versa) depending on memory signal integrity analysis.
6. Applies to rising and falling edges.
7. T_{CASE} = 0° C to + 105° C is without a heat sink.

Table 9. 100 MHz Memory Interface Timing (Sheet 2 of 2)

Functional Operating Range (V_{CC} = 3.3 V ±5%, T_{CASE} = 0° C to +105° C[7], C_L = 0 pF)

Symbol	Parameter	1x Buffer		2x Buffer		3x Buffer		Fig.	Notes
		Min	Max	Min	Max	Min	Max		
t16a	SCAS[B:A]# Valid Delay from DCLKWR (for the first chip select)	1.25	18.31	1.19	18.18	1.50	18.13	4	1,3,4,5,6
t17a	SCAS[B:A]# Valid Delay from DCLKWR Rising (subsequent chip selects)	1.25	8.51	1.19	8.38	1.9	8.33	4	2,3,4,5,6
t18a	CSA[5:0], CSB[5:0] Valid Delay from DCLKWR Rising	1.08 1.13	4.15 3.88	0.90 1.05	2.80 3.50	NA NA	NA NA	4	Rising Falling
t19a	CKE[3:2]/CSA[7:6]#, CKE[5:4]/CSB[7:6]#, CKE0/ FENA#, CKE1/GCKE, Valid Delay from DCLKWR Rising	1.04 1.07	3.87 3.76	0.90 1.03	3.55 3.68	0.87 1.03	3.11 3.46	4	Rising Falling
t20a	DQMA[7:0], Valid Delay from DCLKWR Rising	1.12 1.13	3.87 3.61	0.92 1.14	2.80 2.80	0.83 0.93	3.11 3.52	4	Rising Falling
t21a	DQMB[1,5], Valid Delay from DCLKWR Rising	1.12 1.13	3.87 3.61	0.92 1.14	2.80 2.80	0.83 0.93	3.11 3.52	4	Rising Falling
t22a	MD[63:0], MECC[7:0] Valid Delay from DCLKWR Rising	1.17 1.14	3.20 3.20	0.96 0.93	2.70 2.70	0.88 0.83	2.50 3.25	4	Rising Falling
t23a	MD[63:0], MECC[7:0] Setup Time to DCLKRD Rising	0.47		0.47		0.6 0.47		5	4,6
t24a	MD[63:0], MECC[7:0] Hold Time from DCLKRD Rising	1.5		1.5		1.5		5	4,6

NOTES:
1. Symbols t10a, t12a, t14a, and t16a are based on a 3-clock cycle valid delay.
2. Symbols t11a, t13a, t15a, and t17a are based on a 2-clock cycle valid delay.
3. Two valid delays apply to these command singals. The longer valid delay applies to command signals setup to the first chip select of an access. The second valid delay applies command signals setup to subsequent chip selects in the access. However, in a pipelined access, the shorter valid delay applies to command signals setup to the first chip select.
4. All measurements are in ns, unless otherwise specified.
5. The choice of 100 MHz or 66 MHz buffers is independent of bus frequency. It is possible to select a 100 MHz memory buffer even though the bus frequency is 66 MHz (and vise versa) depending on memory signal integrity analysis.
6. Applies to rising and falling edges.
7. T_{CASE} = 0° C to + 105° C is without a heat sink.

Table 10. 66 MHz Memory Interface Timing (Sheet 1 of 2)

Symbol	Parameter	1x Buffer		2x Buffer		3x Buffer		Fig.	Notes
		Min	Max	Min	Max	Min	Max		
t10b	WE[B:A]# Valid Delay from DCLKWR (for the first chip select) (SDRAM/EDO Modes)	1.61 1.54	17.98 18.13	1.61 1.55	17.95 18.07	1.61 1.55	17.93 18.04	4	Rising Falling 1,2,3,4
t11b	WE[B:A]# Valid Delay from DCLKWR Rising (for the subsequent chip selects) (SDRAM/EDO Modes)	1.61 1.54	8.18 8.33	1.61 1.55	8.15 8.27	1.61 1.55	8.14 8.24	4	Rising Falling 1,2,3,4
t12b	MAA[13:0], MAB[13;11,9:0]#, MAB10 Valid Delay from DCLKWR (first chip select of an access) (SDRAM/EDO Modes)	1.61 1.54	17.98 18.13	1.61 1.55	17.95 18.07	1.61 1.55	17.93 18.04	4	Rising Falling 1,2,3,4
t13b	MAA[13:0], MAB[13;11,9:0]#, MAB10 Valid Delay from DCLKWR Rising, SDRAM Read/Write cycles (for the subsequent chip selects) (SDRAM/EDO Modes)	1.61 1.54	8.18 8.33	1.61 1.55	8.15 8.27	1.61 1.55	8.14 8.24	4	Rising Falling 1,2,3,4
t14b	SRAS[B:A]# Valid Delay from DCLKWR (first chip select of an access) (SDRAM Mode)	1.61 1.54	17.98 18.13	1.61 1.55	17.95 18.07	1.61 1.55	17.93 18.04	4	Rising Falling 1,2,3,4
t15b	SRAS[B:A]# Valid Delay from DCLKWR Rising (subsequent chip selects) (SDRAM Mode)	1.61 1.54	8.18 8.33	1.61 1.55	8.15 8.27	1.61 1.55	8.14 8.24	4	Rising Falling 1,2,3,4
t16b	SCAS[B:A]# Valid Delay from DCLKWR (for the first chip select) (SDRAM Mode)	1.61 1.54	17.98 18.13	1.61 1.55	17.95 18.07	1.61 1.55	17.93 18.04	4	Rising Falling 1,2,3,4
t17b	SCAS[B:A]# Valid Delay from DCLKWR Rising (subsequent chip selects) (SDRAM Mode)	1.61 1.54	8.18 8.33	1.61 1.55	8.15 8.27	1.61 1.55	8.14 8.24	4	Rising Falling 1,2,3,4
t18b	CSA[5:0]#/RASA[5:0]#, CSB[5:0]#/RASB[5:0]#, Valid Delay from DCLKWR Rising (SDRAM/EDO Modes)	1.72 1.56	5.87 5.54	1.56 1.56	5.85 5.67	NA	NA	4	Rising Falling 1,2,3,4
t19b	CKE[3:2]/CSA[7:6]#, CKE[5:4]/CSB[7:6]#, CKE0/FENA#, CKE1/GCKE, Valid Delay from DCLKWR Rising (SDRAM/EDO Modes)	1.53 1.65	6.2 6.2	1.53 1.63	6.07 6.07	1.54 1.62	6.2 6.2	4	Rising Falling 1,2,3,4
t20b	DQMA[7:6,4:2,0]/CASA[7:6,4:2,0]#, Valid Delay from DCLKWR Rising (SDRAM/EDO Modes)	1.53 1.69	5.74 5.69	1.52 1.59	5.72 5.65	1.52 1.58	5.72 5.70	4	Rising Falling 1,2,3,4

NOTES:
1. Two valid delays apply to these command singals. The longer valid delay applies to command signals setup to the first chip select of an access. The second valid delay applies command signals setup to subsequent chip selects in the access. However, in a pipelined access, the shorter valid delay applies to command signals setup to the first chip select.
2. All measurements are in ns, unless otherwise specified.
3. The choice of 100 MHz or 66 MHz buffers is independent of bus frequency. It is possible to select a 100 MHz memory buffer even though the bus frequency is 66 MHz (and vise versa) depending on memory signal integrity analysis.
4. Applies to rising and falling edges.

Table 10. 66 MHz Memory Interface Timing (Sheet 2 of 2)

Symbol	Parameter	1x Buffer		2x Buffer		3x Buffer		Fig.	Notes
		Min	Max	Min	Max	Min	Max		
t21b	DQMA[5,1]/CASA[5,1]#, DQMB[5,1]/CASB[5,1]#, Valid Delay from DCLKWR Rising (SDRAM/EDO Modes)	1.57 1.70	5.78 5.74	1.51 1.61	5.69 5.63	1.51 1.59	5.63 5.63	4	Rising Falling 1,2,3,4
t22b	MD[63:0], MECC[7:0] Valid Delay from DCLKWR Rising (SDRAM/EDO Modes)	1.59 1.73	5.54 5.75	1.58 1.63	5.56 5.65	NA	NA	4	Rising Falling 1,2,3,4
t23b	MD[63:0], MECC[7:0] Setup Time to DCLKWR Rising (SDRAM Mode Only)	0.47		0.47		0.47		5	1,2,3,4
t24b	MD[63:0], MECC[7:0] Hold Time from DCLKWR Rising (SDRAM Mode Only)	1.5		1.5		1.5		5	1,2,3,4
t25b	MD[63:0], MECC[7:0] Setup Time to DCLKWR Rising (EDO Mode Only)	2.2		2.2		2.2		5	1,2,3,4
t26b	MD[63:0], MECC[7:0] hold Time to DCLKWR Rising (EDO Mode Only)	6		6		6		5	1,2,3,4

NOTES:
1. Two valid delays apply to these command singals. The longer valid delay applies to command signals setup to the first chip select of an access. The second valid delay applies command signals setup to subsequent chip selects in the access. However, in a pipelined access, the shorter valid delay applies to command signals setup to the first chip select.
2. All measurements are in ns, unless otherwise specified.
3. The choice of 100 MHz or 66 MHz buffers is independent of bus frequency. It is possible to select a 100 MHz memory buffer even though the bus frequency is 66 MHz (and vise versa) depending on memory signal integrity analysis.
4. Applies to rising and falling edges.

Table 11. PCI Clock Timing; 33 MHz

Functional Operating Range (V$_{CC}$ = 3.3 V ±5%; T$_{CASE}$ = 0° C to +105$^{(2)}$° C)

Symbol	Parameter	Min	Max	Figure	Notes
t30	PCLKIN Period	30		2	ns
t31	PCLKIN Cycle-to-Cycle Jitter		500		ps
t32	PCLKIN High Time	12		2	ns
t33	PCLKIN Low Time	12		2	ns
t34	HCLKIN Lead Time to PCLKIN	1.5	5		ns
t35	PCLKIN Rise Time		3	2	ns
t36	PCLKIN Fall Time		3	2	ns

NOTES:
1. Times are measured at the 440BX.
2. T$_{CASE}$ = 0° C to + 105° C is without a heat sink.

Table 12. PCI Interface Timing; 33 MHz

Functional Operating Range (V$_{CC}$ = 3.3 V ±5%; T$_{CASE}$ = 0° C to +105$^{(1)}$° C)

Symbol	Parameter	Min	Max	Figure	Notes
t37	AD[31:0] Valid Delay from PCLKIN Rising	2	11	4	Min: 0 pF Max: 50 pF
t38	AD[31:0] Setup Time to PCLKIN Rising	7		5	
t39	AD[31:0] Hold Time from PCLKIN	0		5	
t40	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, DEVSEL#, SERR#, Valid Delay from PCLKIN Rising	2	11	4	Min: 0 pF Max: 50 pF
t41	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, DEVSEL#, SERR#, Output Enable Delay from PCLKIN Rising	2	11		
t42	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, DEVSEL#, SERR#, Float Delay from PCLKIN Rising	2	28	6	
t43	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, DEVSEL#, SERR#, Setup Time to PCLKIN Rising	7		5	
t44	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, DEVSEL#, SERR#, Hold Time from PCLKIN Rising	0		5	
t45	PHLDA# Valid Delay from PCLKIN Rising	2	12	4	Min: 0 pF Max: 50 pF
t46	PHOLD# Setup Time to PCLKIN Rising	12		5	
t47	PHOLD# Hold Time from PCLKIN Rising	0		5	
t48	PGNT[4:1]#, GNT0#/IOGNT# Valid Delay from PCLKIN Rising	2	12	4	Min: 0 pF Max: 50 pF
t49	PREQ[4:1]#, PREQ0#/IOREQ0# Setup Time to PCLKIN Rising	12		5	
t50	PREQ[4:1]#, PREQ0#/IOREQ0# Hold Time from PCLKIN Rising	0		5	
t51	PCIRST# Low Pulse Width	1		7	ms

NOTE:
1. T$_{CASE}$ = 0° C to + 105° C is without a heat sink.

Table 13. AGP Interface Timing; 66 MHz (Sheet 1 of 2)

Functional Operating Range (Vcc = 3.3 V ±5%, T$_{CASE}$ = 0° C to +105$^{(1)}$° C)

Symbol	Parameter	Min	Max	Figure	Unit
t53	G_AD[31:0], G_C/BE#[3:0] Valid Delay from GCLKIN Rising	1	6	4	ns
t54	G_AD[31:0], G_C/BE#[3:0], SBA[7:0] Setup Time to GCLKIN Rising	5.5		5	ns
t55	G_AD[31:0], G_C/BE#[3:0], SBA[7:0] Hold Time from GCLKIN	0		5	ns

Table 13. AGP Interface Timing; 66 MHz (Sheet 2 of 2)

Functional Operating Range (Vcc = 3.3 V $\pm$5%, T_{CASE} = 0° C to +105[(1)]° C)

Symbol	Parameter	Min	Max	Figure	Unit
t56	G_FRAME#, G_TRDY#, G_IRDY#, G_STOP#, G_PAR, G_DEVSEL#, G_GNT#, ST[2:0] Valid Delay from GCLKIN Rising	1	5.5	4	ns
t57	G_FRAME#, G_TRDY#, G_IRDY#, G_STOP#, G_PAR, G_DEVSEL#, PIPE#, RBF#, G_REQ#, G_GNT#, ST[2:0] Float Delay from GCLKIN Rising	1	14	6	ns
t58	G_FRAME#, G_TRDY#, G_IRDY#, G_STOP#, G_PAR, G_DEVSEL#, PIPE#, RBF#, G_REQ# Setup Time to GCLKIN Rising	6		5	ns
t59	G_FRAME#, G_TRDY#, G_IRDY#, G_STOP#, G_PAR, G_DEVSEL#, PIPE#, RBF#, G_REQ# Hold Time from GCLKIN Rising	0		5	ns

NOTE:
1. T_{CASE} = 0° C to +105[1]° C is with no heat sink.

Table 14. AGP Interface Timing; 133 MHz (Sheet 1 of 2)

Functional Operating Range (Vcc = 3.3 V $\pm$5%, T_{CASE} = 0° C to +105[(1)]° C)

Symbol	Parameter	Min	Max	Figure	Note
t60	AD_STB[B:A] falling Valid Delay at transmitter from GCLKIN rising	2	12	9	tTSf, Figure 8
t61	AD_STB[B:A] rising Valid Delay at transmitter from GCLKIN rising		20	9	tTSr, Figure 8
t62	G_AD[31:0],G_C/BE[3:0]# Valid Delay before AD_STB[B:A] Rise/Fall	1.7		9	tDvb, Figure 8
t63	G_AD[31:0] G_C/BE[3:0]# Valid Delay after AD_STB[B:A] Rise/Fall	1.7		9	tDva, Figure 8
t64	G_AD[31:0] G_C/BE[3:0]# Float to Active Delay from GCLKIN rising	-1	9	8	tOND, Figure 8
t65	G_AD[31:0], G_C/BE[3:0]# Active to Float Delay from GCLKIN rising	1	12	8	tOFFD, Figure 8
t66	AD_STB[B:A] rising Delay Time at transmitter to AD_STB[B:A] floating	6	10	8	tOFFS, Figure 8
t67	AD_STB[B:A] active Setup Time at transmitter to AD_STB[B:A] falling	6	10	8	tONS, Figure 8
t68	AD_STB[B:A] rising Setup Time at receiver to GCLKIN rising	6		9	tRSsu, Figure 8
t69	AD_STB[B:A] falling Hold Time at receiver to GCLKIN rising	1		9	tRSsh, Figure 8
t70	G_AD[31:0],G_C/BE[3:0]# Setup Time to AD_STB[B:A] Rise/Fall	1		9	tDsu, Figure 8
t71	G_AD[31:0] G_C/BE[3:0]# Hold Time from AD_STB[B:A] Rise/Fall	1		9	tDh, Figure 8

NOTE:
1. T_{CASE} = 0° C to +105[1]° C is with no heat sink.

Table 14. AGP Interface Timing; 133 MHz (Sheet 2 of 2)

Functional Operating Range (Vcc = 3.3 V ±5%, T$_{CASE}$ = 0° C to +105$^{(1)°}$ C)

Symbol	Parameter	Min	Max	Figure	Note
t72	SBSTB rising Setup Time at receiver to GCLKIN rising	6		9	tRSsu, Figure 8
t73	SBSTB falling Hold Time at receiver to GCLKIN rising	1		9	tRSh, Figure 8
t74	SBA[7:0] Setup Time at receiver to SBSTB Rise/Fall	1		9	tDsu, Figure 8
t75	SBA[7:0] Hold Time at receiver from SBSTB Rise/Fall	1		9	tDh, Figure 8

NOTE:
1. T$_{CASE}$ = 0° C to +105$^{1°}$ C is with no heat sink.

Table 15. Miscellaneous Signal Timings

Symbol	Parameter	Min	Max	Fig.	Notes
t76	CRESET# Inactive (rising) edge Valid Delay time from HCLKIN Rising	0.2	7	4	0 pF
t77	WSC# Valid Delay from PCLKIN Rising	2	12	4	Min: 0 pF Max: 50 pF

Table 16. VT$_{CLOCK}$ and VT$_{SIGNAL}$ Reference Points

Signal Group	VT$_{CLOCK}$	VT$_{SIGNAL}$
GTL	1.25 V	1.0 V
DRAM	1.4 V	1.4 V
PCI (3.3 V)	1.5 V	0.285 V$_{CC}$ (R) 0.615 V$_{CC}$ (F)
AGP	0.4 V$_{CC}$	0.4 V$_{CC}$

Figure 1. 2.5 V Clocking Interface

A6315-01
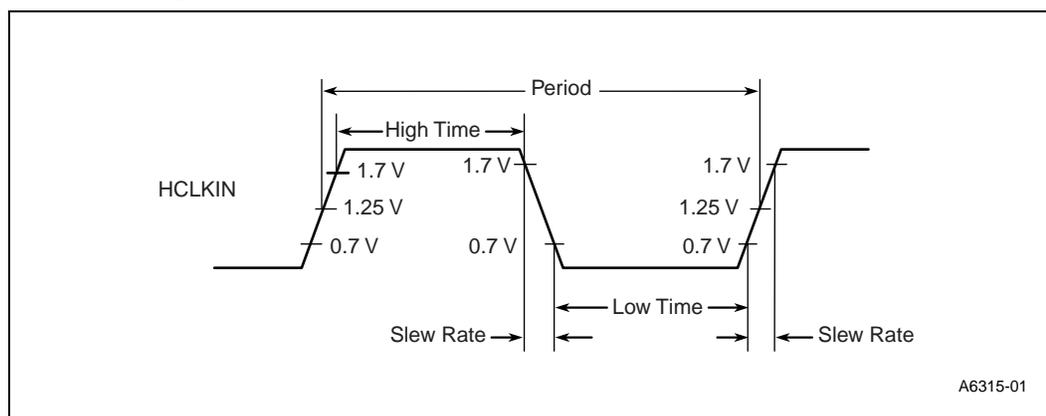
Figure 2. 3.3 V Clocking Interface
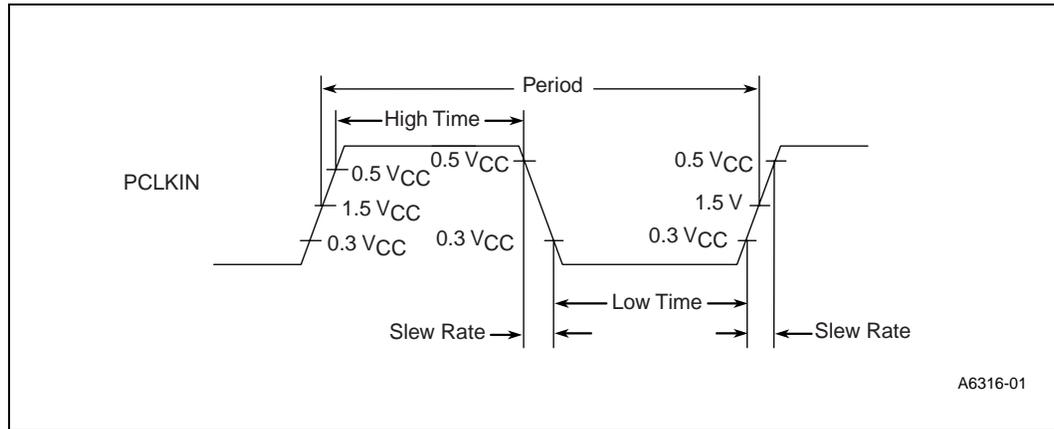
**Figure 3. 3.3 V Clock Duty Cycle**
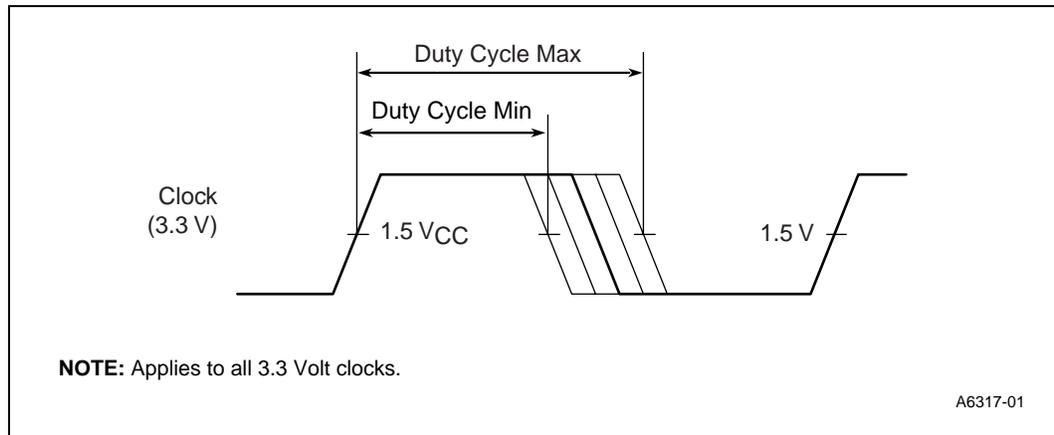

Figure 4. Valid Delay from Rising Clock Edge
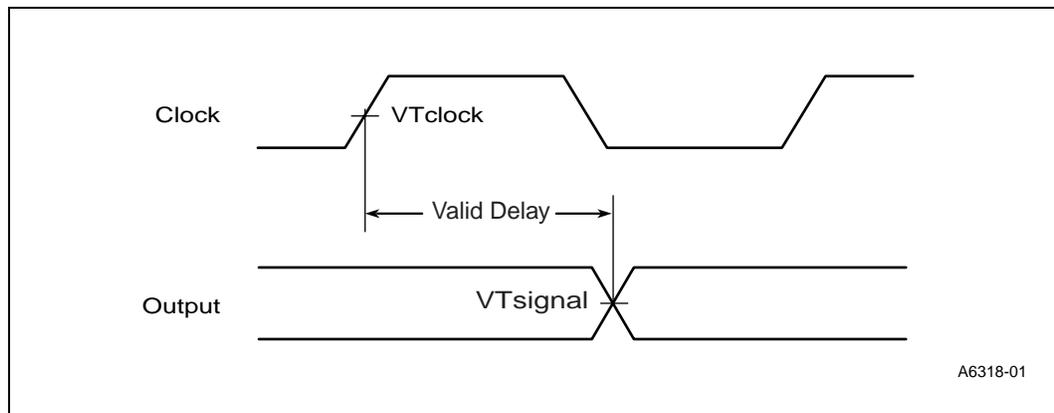
Figure 5. Setup and Hold Time to Clock
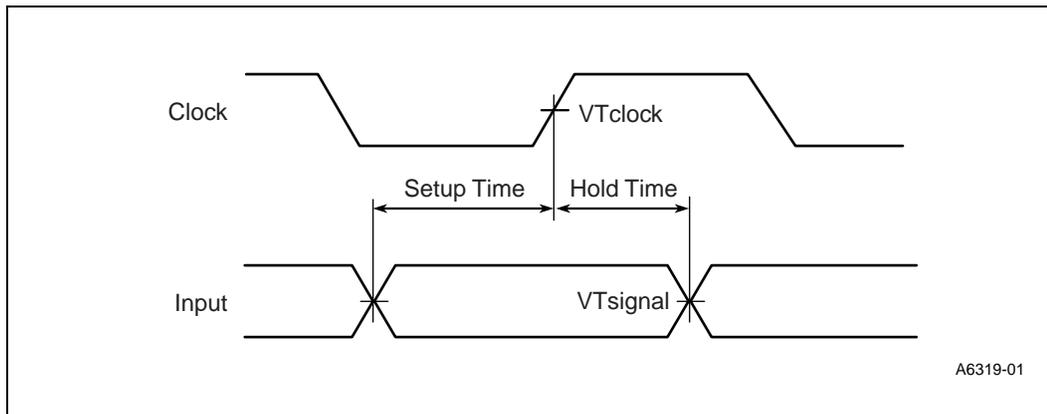
Figure 6. Float Delay
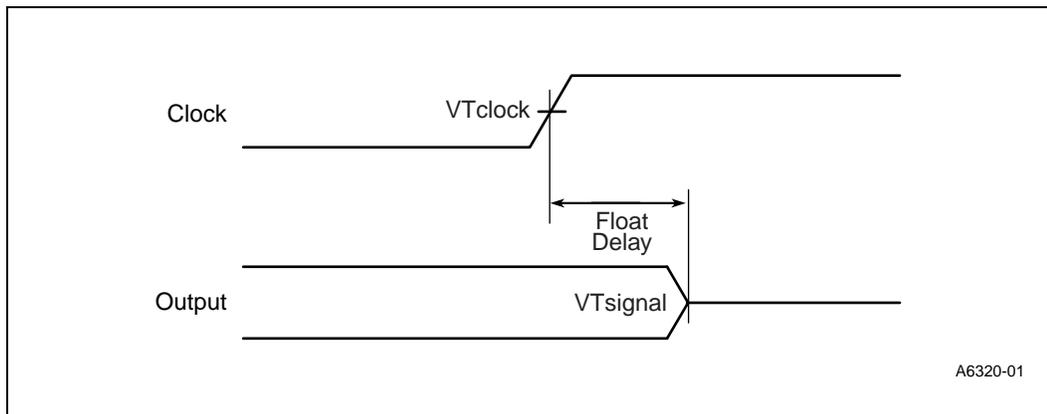

**Figure 7. Pulse Width**

Datasheet Addendum
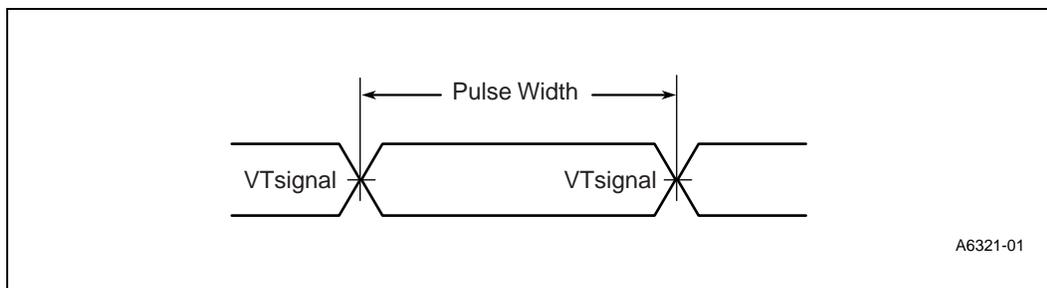
Figure 8. Strobe/Data Turnaround Timings
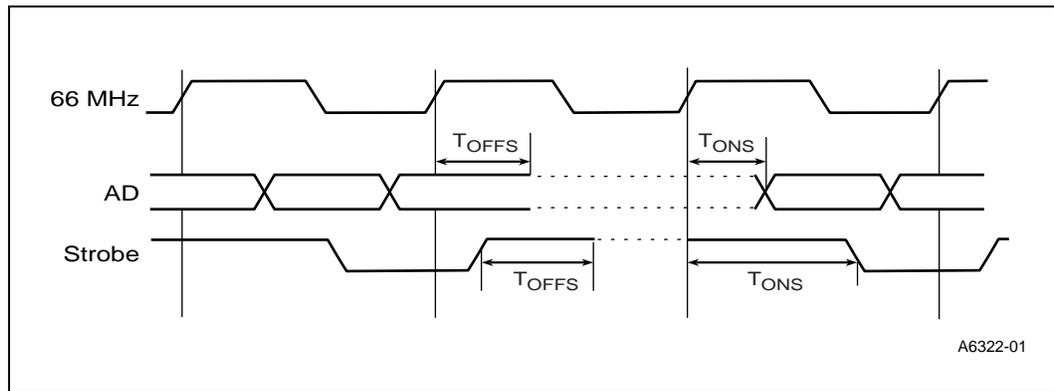
Figure 9. AGP 133 Timing Diagram