ISP Synario Starter 3.0 Release Notes

This unique software package supports both ispLSI and pLSI high-density devices and low-density ispGAL and GAL devices from Lattice Semiconductor. The product consists of a fully functional Synario-Entry and Functional Simulation package for both high- and low-density logic definition. For ispGAL and GAL device designs, this version of the Synario-Entry toolset directly generates the standard JEDEC file required for device programming. For ispLSI and pLSI device designs, the Synario-Entry tool is tightly integrated with the Lattice ISP Synario Starter Fitter for the 1016 and 2032 device families.

A license file and software security key are not required to enable this package.

These release notes provide additional information for version 3.0 of the Lattice ISP Synario Starter design solution and are intended as a supplement to the CD-ROM documents included with the package. The following topics are discussed:

- Installing the New Software
- 1016 and 2032 Device Family Support
- Low-Density Device Support
- Synario Design Attribute Restrictions in Hierarchical Designs
- Common Issues and Solutions

Installing the New Software

You must have a 486 (or higher) PC with 25 megabytes of free disk, running Windows 3.1.x or Windows95, to successfully install and use this software. Load the ISP Synario Starter Entry/Sim software and ISP Synario Starter Fitter in succession. Once that is completed, you can add the ISP Daisy Chain Download to your PDSPLUS directory. See the *ISP Synario System User Manual* for information on installing the ISP Synario Entry/Sim and ISP Synario Starter Fitter software.

Note: The pDS+ Timing Analyzer is not supported in the ISP Synario Starter software.

1016 and 2032 Device Family Support

The Device Numbers listed in the following tables are the device part numbers you enter when using the ISP Synario Starter software. It is important that you keep this list as a reference when using the ISP Synario Starter software. Refer to the *Lattice Semiconductor Data Book 1996* for the part numbers to order devices.

Table 1. 1016 Device Family Part Numbers

Device Part Number	Speed	Package	Pins	Grade
ispLSI 1016 Family				
ispLSI1016E-125LT44	125 MHz	TQFP	44	Commercial
ispLSI1016E-100LT44	100 MHz	TQFP	44	Commercial
ispLSI1016E-80LT44	80 MHz	TQFP	44	Commercial
ispLSI1016E-125LJ44	125 MHz	PLCC	44	Commercial
ispLSI1016E-100LJ44	100 MHz	PLCC	44	Commercial
ispLSI1016E-80LJ44	80 MHz	PLCC	44	Commercial
ispLSI1016-90LT44	90 MHz	TQFP	44	Commercial
ispLSI1016-80LT44	80 MHz	TQFP	44	Commercial
ispLSI1016-60LT44	60 MHz	TQFP	44	Commercial
ispLSI1016-60LT44I	60 MHz	TQFP	44	Industrial
ispLSI1016-110LJ44 *****	110 MHz	PLCC	44	Commercial
ispLSI1016-90LJ44	90 MHz	PLCC	44	Commercial
ispLSI1016-80LJ44	80 MHz	PLCC	44	Commercial
ispLSI1016-60LJ44	60 MHz	PLCC	44	Commercial
ispLSI1016-60LJ44I	60 MHz	PLCC	44	Industrial
ispLSI1016-60LH44/883	60 MHz	JLCC	44	Military/SMD

***** Not recommended for new designs. Use “E” series device instead.

Table 1. 1016 Device Family Part Numbers (Continued)

Device Part Number	Speed	Package	Pins	Grade
pLSI 1016 Family				
pLSI1016E-125LJ44	125 MHz	PLCC	44	Commercial
pLSI1016E-100LJ44	100 MHz	PLCC	44	Commercial
pLSI1016E-80LJ44	80 MHz	PLCC	44	Commercial
pLSI1016-90LT44	90 MHz	TQFP	44	Commercial
pLSI1016-80LT44	80 MHz	TQFP	44	Commercial
pLSI1016-60LT44	60 MHz	TQFP	44	Commercial
pLSI1016-110LJ44 *****	110 MHz	PLCC	44	Commercial
pLSI1016-90LJ44	90 MHz	PLCC	44	Commercial
pLSI1016-80LJ44	80 MHz	PLCC	44	Commercial
pLSI1016-60LJ44	60 MHz	PLCC	44	Commercial
pLSI1016-60LJ44I	60 MHz	PLCC	44	Industrial
pLSI1016-60LH44/883	60 MHz	JLCC	44	Military/SMD

***** Not recommended for new designs. Use “E” series device instead.

Table 2. 2032 Device Family Part Numbers

Device Part Number	Speed	Package	Pins	Grade
ispLSI 2032 Family				
ispLSI2032-180LT48	180 MHz	TQFP	48	Commercial
ispLSI2032-150LT48	150 MHz	TQFP	48	Commercial
ispLSI2032-135LT48	135 MHz	TQFP	48	Commercial
ispLSI2032-110LT48	110 MHz	TQFP	48	Commercial
ispLSI2032-80LT48	80 MHz	TQFP	48	Commercial
ispLSI2032-80LT48I	80 MHz	TQFP	48	Industrial
ispLSI2032-180LT44	180 MHz	TQFP	44	Commercial
ispLSI2032-150LT44	150 MHz	TQFP	44	Commercial
ispLSI2032-135LT44	135 MHz	TQFP	44	Commercial
ispLSI2032-110LT44	110 MHz	TQFP	44	Commercial
ispLSI2032-80LT44	80 MHz	TQFP	44	Commercial
ispLSI2032-80LT44I	80 MHz	TQFP	44	Industrial
ispLSI2032-180LJ44	180 MHz	PLCC	44	Commercial
ispLSI2032-150LJ44	150 MHz	PLCC	44	Commercial
ispLSI2032-135LJ44	135 MHz	PLCC	44	Commercial
ispLSI2032-110LJ44	110 MHz	PLCC	44	Commercial
ispLSI2032-80LJ44	80 MHz	PLCC	44	Commercial
ispLSI2032-80LJ44I	80 MHz	PLCC	44	Industrial
ispLSI2032LV-80LT44	80 MHz	TQFP	44	Commercial
ispLSI2032LV-60LT44	60 MHz	TQFP	44	Commercial
ispLSI2032LV-60LT44I	60 MHz	TQFP	44	Industrial
ispLSI2032LV-80LJ44	80 MHz	PLCC	44	Commercial
ispLSI2032LV-60LJ44	60 MHz	PLCC	44	Commercial
ispLSI2032LV-60LJ44I	60 MHz	PLCC	44	Industrial
ispLSI2032V-100LT44	100 MHz	TQFP	44	Commercial
ispLSI2032V-100LJ44	100 MHz	PLCC	44	Commercial

Table 2. 2032 Device Family Part Numbers (Continued)

Device Part Number	Speed	Package	Pins	Grade
pLSI 2032 Family				
pLSI2032-150LT44	150 MHz	TQFP	44	Commercial
pLSI2032-135LT44	135 MHz	TQFP	44	Commercial
pLSI2032-110LT44	110 MHz	TQFP	44	Commercial
pLSI2032-80LT44	80 MHz	TQFP	44	Commercial
pLSI2032-180LJ44	180 MHz	PLCC	44	Commercial
pLSI2032-150LJ44	150 MHz	PLCC	44	Commercial
pLSI2032-135LJ44	135 MHz	PLCC	44	Commercial
pLSI2032-110LJ44	110 MHz	PLCC	44	Commercial
pLSI2032-80LJ44	80 MHz	PLCC	44	Commercial
pLSI2032LV-80LJ44	80 MHz	PLCC	44	Commercial
pLSI2032LV-60LJ44	60 MHz	PLCC	44	Commercial
pLSI2032V-100LJ44	100 MHz	PLCC	44	Commercial

Low-Density Device Support

In addition to supporting the ispLSI and pLSI 1016 and 2032 high-density device families, the ISP Synario Starter also supports the following Lattice Semiconductor low-density devices

- GAL16V8
- GAL16V8Z
- GAL16LV8
- GAL16VP8
- GAL16LV8ZD
- GAL18V10
- GAL20LV8ZD
- GAL20RA10
- GAL20V8
- GAL20V8Z
- GAL20VP8
- GAL20XV10
- GAL22LV10
- GAL22V10
- ispGAL22V10
- GAL26CV12
- GAL6001
- GAL6002

The ispGDS Compiler supports the following Lattice Semiconductor ispGDS devices:

- ispGDS14
- ispGDS18
- ispGDS22

Synario Design Attribute Restrictions in Hierarchical Designs

The current version of Synario by Data I/O does not properly process Lattice Semiconductor Design Attributes in the lower-level modules of hierarchical designs. We strongly recommend that you place Design Attributes and Fitter Control Options in the top-level of your design. See the *Data I/O and pDS+ Design and Simulation Environment User Manual* for further details.

Common Issues and Solutions

Issue: If you use a dot extension in a pLSI property statement, a warning message appears which states that "Signals in pins or nodes cannot have dot extensions." This restriction is imposed by Data I/O Synario. An example of a dot extension in a pLSI property statement is shown below.

```
pLSI property 'PRESERVE QB0.Q';
```

Solution: Manually edit the *design*.abl file to remove the dot extension and attach the attribute to the pin or node itself. To preserve the data, clock, or reset input of a register, you must define an intermediate node and preserve it. An example of an edited pLSI property statement is shown below:

```
pLSI property 'PRESERVE QB0';
```

Issue: Some Help files that are part of the full Synario product are not required in the ISP Synario Starter. If you select a topic that does not have an associated Help file, the following message displays:

<path>/file_name.[htm|hlp] not found

Solution: Click **OK** in the dialog box displaying the message to continue.

Issue: When you select **Help** ⇒ **Manuals**, you may receive a message indicating the path to the online manuals is not found.

Solution: Click **Yes** in the dialog box displaying the message to be able set the path to the ISP Synario Starter directory called "`manuals`" where the Acrobat format .pdf files are located.