THE
JIM WILLIAMS
PAPERS

Filters and oscillators

Filters get rid of a signal's unwanted frequency components. Oscillators create signals at predictable frequencies. As you might imagine, the two types of circuits have more than a little in common.

Jim Williams, *Linear Technology Corp*

Filters and oscillators share a common point of view—they deal with signals in the frequency domain. You can define a filter's function as rejecting frequencies you don't want (the job of a band-reject filter, for example) or including only the frequencies you want (what a bandpass filter does). If you reorient your thinking slightly, though, you realize that all filters reject unwanted frequencies. (The bandpass filter rejects frequencies outside the band of interest.) When you view filters in this way, you see that any filter's function is the inverse of an oscillator's; oscillators synthesize individual frequencies or ranges of frequencies. Although there are more kinds of filters and oscillators than any magazine article of reasonable length can hope to touch on, herein are a few types of circuits that can meet a range of needs.

Fig 1a shows a highly selective bandpass filter using a resonant ceramic element and a single amplifier. Except at its resonant frequency, (in this case, 400 kHz) the ceramic element looks like a high impedance. For off-resonance inputs, IC_1 produces no output; it acts as a follower whose input is grounded. At resonance,

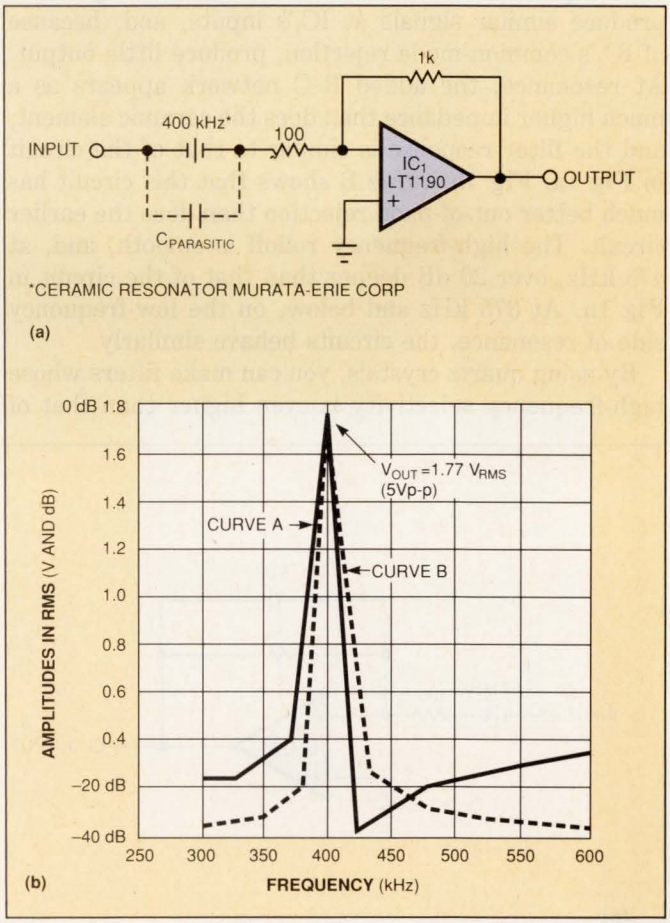

Fig 1—One amplifier and a ceramic resonator *create a bandpass filter* ***(a)****. The solid curve of* ***b*** *shows the filter's frequency response. Note the dip to −40 dB on the high side of resonance. The dip is the result of the resonator's parasitic capacitance.*

the ceramic element has a low impedance, and IC_1 behaves as an inverter with gain. The 100Ω resistor isolates IC_1's summing point from the ceramic element's capacitance. This capacitance is quite substantial and limits the circuit's out-of-band rejection. **Fig 1b**, curve A shows this effect. This plot shows very steep rejection, with IC_1's output down almost 20 dB at 300 kHz and 40 dB at 425 kHz. The device's stray parasitic capacitance causes the gentle rise in the output at higher frequencies and also sets the −20-dB floor at 300 kHz.

Fig 2 shows how to use a nulling technique to partially correct problems caused by the ceramic element's parasitic capacitance. This circuit is similar to the previous one, except that a portion of the input goes to IC_1's positive input. The R-C network at that input has an impedance close to the ceramic resonator's off-null impedance. Therefore, out-of-band components produce similar signals at IC_1's inputs, and, because of IC_1's common-mode rejection, produce little output. At resonance, the added R-C network appears as a much higher impedance than does the ceramic element, and the filter response is similar to that of the circuit in **Fig 1a**. **Fig 1b**, curve B shows that this circuit has much better out-of-band rejection than does the earlier circuit. The high-frequency rolloff is smooth, and, at 475 kHz, over 20 dB deeper than that of the circuit in **Fig 1a**. At 375 kHz and below, on the low-frequency side of resonance, the circuits behave similarly.

By using quartz crystals, you can make filters whose high-frequency selectivity is even higher than that of

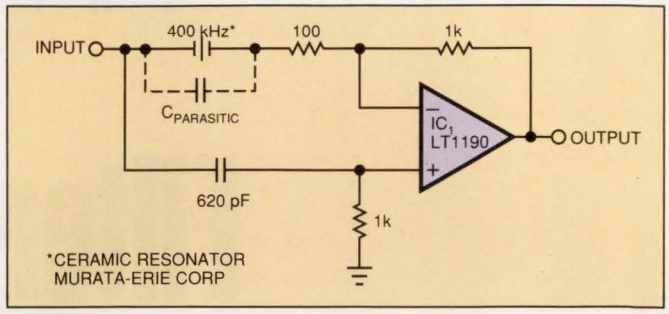

***Fig 2—A slight modification** of the circuit in **Fig 1a** allows you to cancel out the effects of the resonator's parasitic capacitance. The dashed curve of **Fig 1b** shows the effects on the filter response. Below resonance, the modified circuit attenuates by an extra 20 dB. Above approximately 525 kHz, the improvement is even more dramatic.*

filters based on ceramic resonators. **Fig 3a** replaces **Fig 1a**'s ceramic element with a 3.57-MHz quartz crystal. **Fig 3b** shows almost 30 dB of attenuation only a few kHz on either side of resonance! The differential nulling technique used with the ceramic elements is less effective with quartz crystals. Crystals have significantly lower parasitic capacitance, making the cancellation less effective.

Oscillators use crystals and resonators

The circuit in **Fig 4** places a crystal within the amplifier's feedback path, creating an oscillator. With the crystal removed, the circuit is a familiar noninverting amplifier with a grounded input. The impedance ratio of the elements associated with IC_1's negative input sets the gain. Inserting the crystal closes a positive

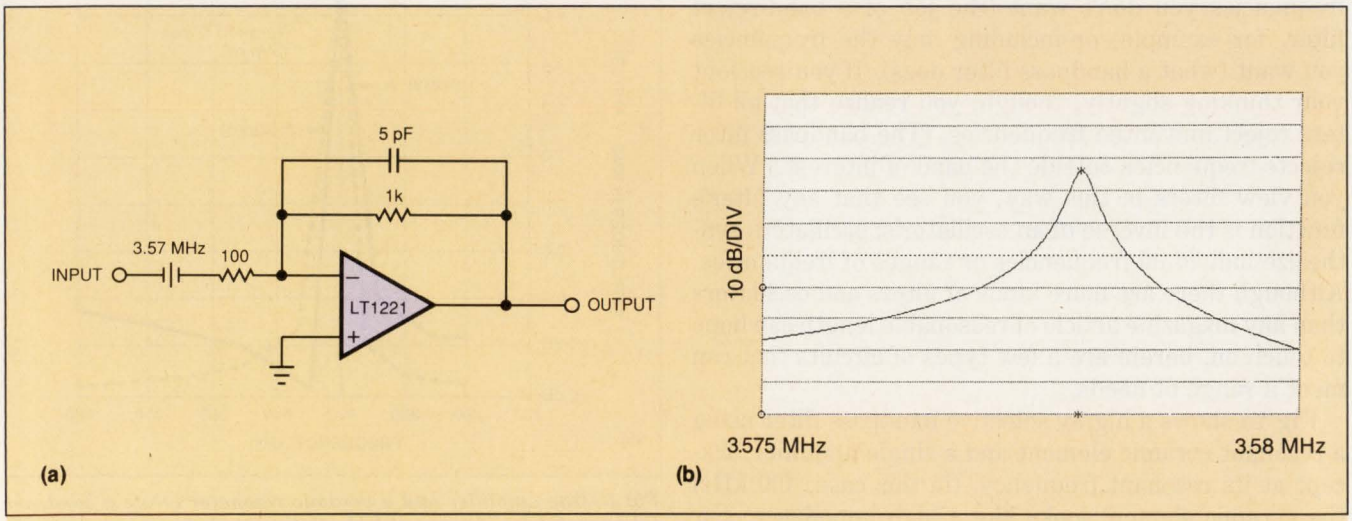

***Fig 3—Replacing the ceramic resonator** of **Fig 1a** with a 3.57-MHz crystal is the most significant change that leads to this crystal filter (**a**). You can see the crystal filter's response in **b**.*

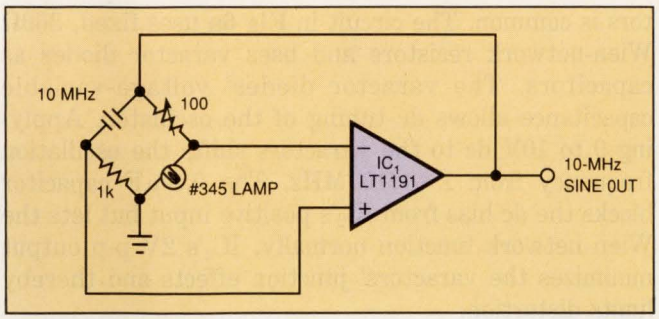

***Fig 4—An incandescent lamp's** current-dependent resistance stabilizes the oscillation amplitude of this 10-MHz crystal oscillator.*

feedback path at the crystal's resonant frequency, and oscillations commence.

In any oscillator, you must control the gain as well as the phase shift at the frequency of interest. If the gain is too low, oscillation will not occur. Conversely, too much gain produces saturation limiting. In this circuit, gain control comes from the positive temperature coefficient of the lamp at IC_1's negative input. When you first apply power, the lamp's resistance is low, the gain is high, and the oscillation amplitude increases. As the amplitude builds, the lamp current increases and causes heating, which raises the lamp resistance. The increased resistance reduces the amplifier gain and the circuit finds a stable operating point. This circuit's sine-wave output has all of the stability advantages associated with quartz crystals. Although shown with a 10-MHz crystal, the circuit works well with a variety of crystal types from 100 kHz to 20 MHz. Using a lamp to control the amplifier gain is a classic technique, first described by Meacham in 1938. Electronic gain control, though more complex, offers more precise control of amplitude.

Fig 5a's quartz stabilized oscillator replaces the lamp with an electronic amplitude-stabilization loop. IC_2 compares the IC_1 oscillator's positive output peaks with a dc reference. The diode in the dc-reference path compensates for the rectifier diode's temperature dependence. IC_2 biases Q_1, controlling the FET's channel resistance and influencing the loop gain. The amplitude of the oscillator's output is a reflection of the loop gain. Loop closure around IC_1 stabilizes the amplitude of the oscillator's output; the 1-μF capacitor compensates the gain-control loop.

The dc-reference network provides optimum temperature compensation for the rectifier diode, which sees IC_1's 2V p-p, 20-MHz output waveform. IC_1's small output swing minimizes the distortion attributable to channel-resistance modulation in Q_1. To use this circuit, adjust the 50Ω trimmer until 2V p-p oscillations appear at IC_1's output.

Fig 5b is a spectrum analysis of the oscillator's output. The fundamental is at 20 MHz; the second harmonic, at 40 MHz, is 47 dB down. The third harmonic,

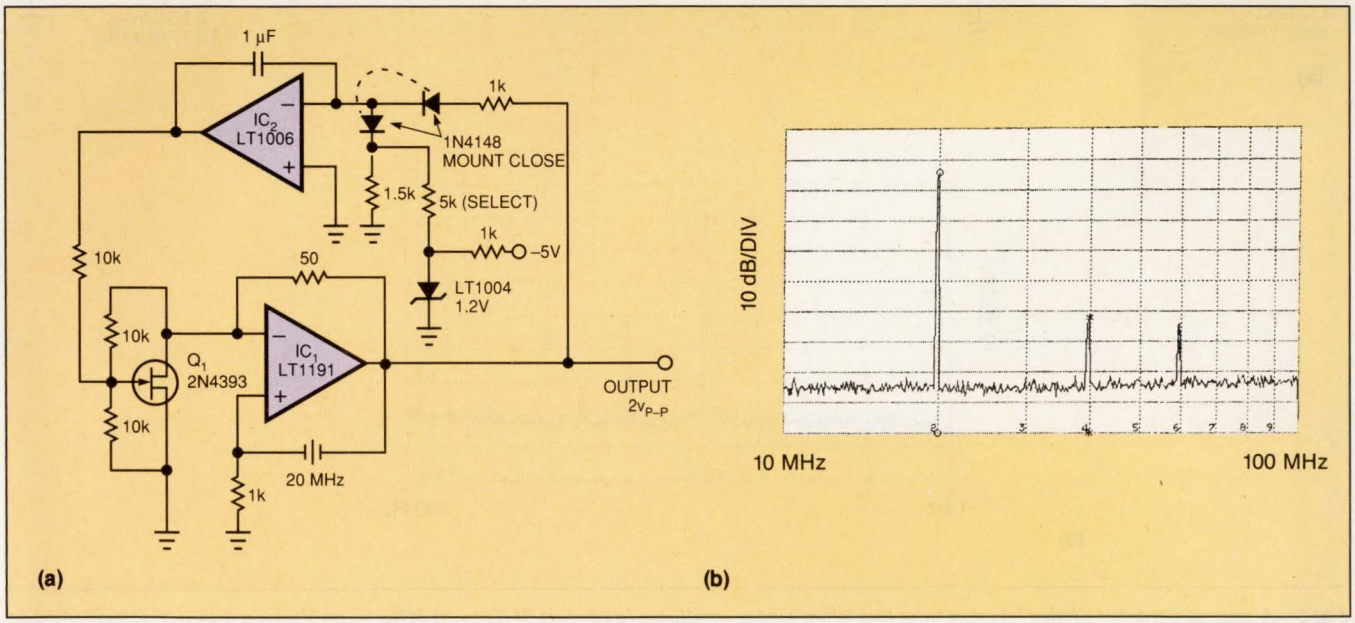

***Fig 5—An electronic gain-control circuit** that uses the voltage-controlled on-resistance of a FET stabilizes the output amplitude of this 20-MHz crystal oscillator **(a)**. In **b**, you see that the output's harmonics are at least 47 dB below the fundamental.*

50 dB down, occurs at 60 MHz. Resolution bandwidth for the spectrum analysis is 1 kHz.

The circuit in **Fig 6a** replaces the quartz crystal with a Wien network at IC_2's positive input. IC_1 controls Q_1 to stabilize the amplitude of IC_2's oscillations. The operation is identical to that of the circuit in the previous figure. Although the Wien network is not nearly as stable as a quartz crystal, it has the advantage of a variable-frequency output. Normally, you vary the frequency by varying either R or C or both. The use of manually adjustable elements, such as dual potentiometers and 2-section variable capacitors is common. The circuit in **Fig 6a** uses fixed, 360Ω Wien-network resistors and uses varactor diodes as capacitors. The varactor diodes' voltage-variable capacitance allows dc tuning of the oscillator. Applying 0 to 10V dc to the varactors shifts the oscillation frequency from 1 to 10 MHz. The 0.1-μF capacitor blocks the dc bias from IC_2's positive input but lets the Wien network function normally. IC_2's 2V p-p output minimizes the varactors' junction effects and thereby limits distortion.

This 5V-powered circuit requires a voltage step-up to develop adequate varactor drive. IC_3 and the

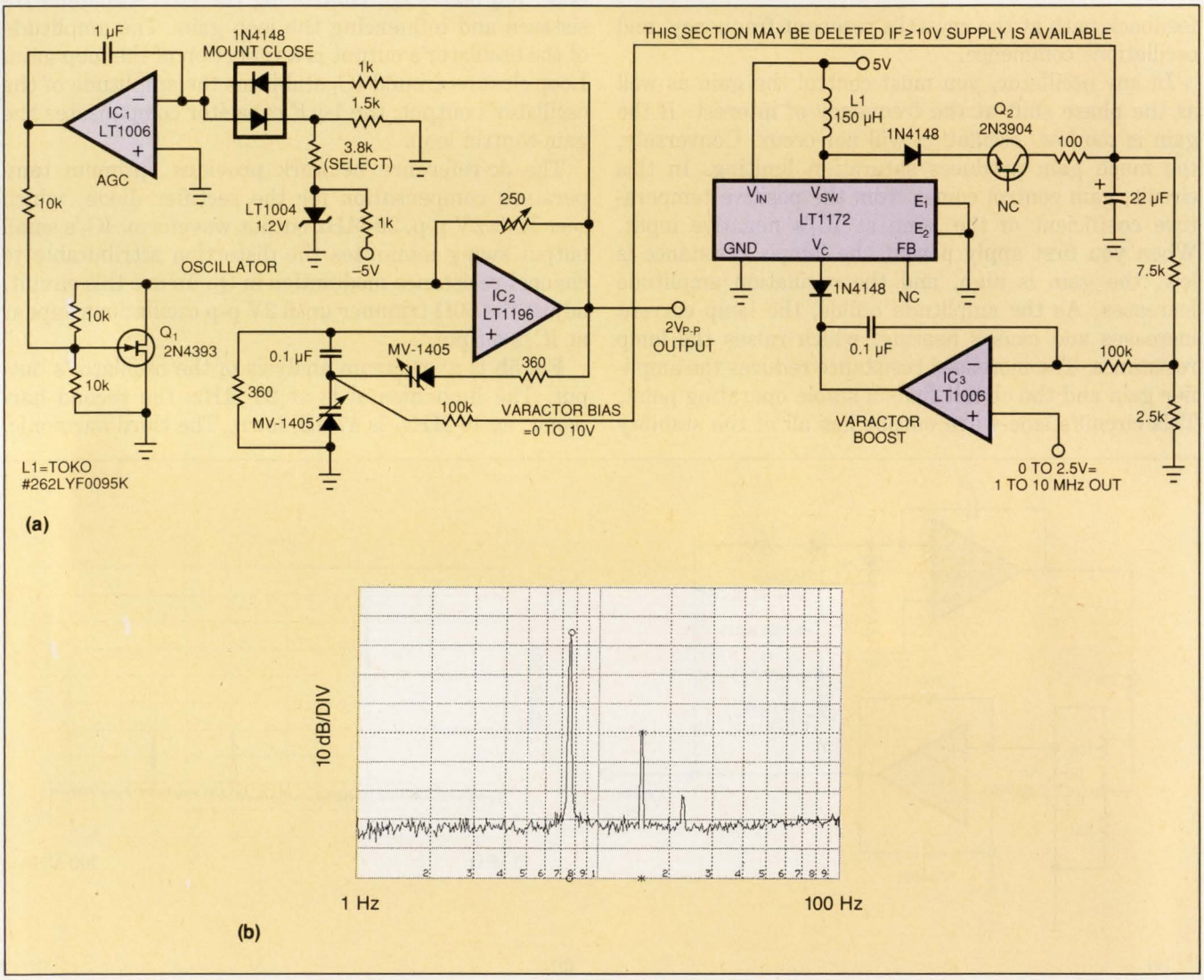

Fig 6—A pair of varactor diodes *lets you tune this Wien-bridge oscillator* ***(a)*** *from 1 MHz to 10 MHz by applying a 0 to 10V signal. Adding the components in the right half of the schematic lets you operate the circuit from a 5V supply and permits controlling the frequency with a 0 to 2.5V signal. The spectrum analysis in* ***b*** *shows that the sinusoidal output is quite clean.*

LT1172 switching regulator form a simple voltage step-up regulator. IC_3 controls the LT1172 to produce whatever output voltage is required to close a loop at IC_3's negative input. The 22-μF output capacitor stores L_1's high-voltage inductive-flyback pulses after they have been rectified by the diode-and-zener-connected Q_2. The 7.5-kΩ/2.5-kΩ divider closes the loop by providing a sample of the output value to IC_3's negative input. The 0.1-μF capacitor stabilizes this feedback action. IC_2's zener drop allows the circuit to produce controlled outputs at voltages as small as zero. This arrangement permits a 0 to 2.5V input at IC_3 to produce a corresponding 0 to 10V varactor bias. **Fig 6b**, a spectral plot of the circuit running at 7.6 MHz, shows the second harmonic down 35 dB and the third harmonic down almost 60 dB. The resolution bandwidth is 3 kHz.

Fig 7a shows the schematic of an AM radio station—complete from microphone to antenna, but lacking a Federal Communications Commission license. IC_1, set up as a quartz-stabilized oscillator similar to the one in **Fig 4**, generates the carrier. IC_1's output feeds IC_2, which functions as a modulated RF power-output stage. The bias applied to offset pins 1 and 8 restricts IC_2's input-signal range. (See the LT1194 data sheet for details.) IC_3, a microphone amplifier, supplies bias to the offset pins, resulting in an amplitude-modulated RF carrier at IC_2's output. The dc voltage summed with the microphone output biases IC_3's output to the appropriate level for good quality modulation characteristics. Calibrating this circuit involves trimming the 100Ω potentiometer in the oscillator for a stable 1V p-p 1-MHz output from IC_1.

Fig 7a does not show on-air personalities—or, in keeping with current trends in AM radio—a means of providing any kind of program other than a talk show. There is no phonograph pickup or connection to the output of a compact-disc player. Nevertheless, you can connect such a music source to the microphone input. **Fig 7b** shows a typical AM carrier output at the antenna. In a throw-back to the days when top-40 formats reigned on the AM band, the modulating signal is Mr Chuck Berry singing the rock-'n'-roll classic "Johnny B. Goode."

Start with a triangle; end up with a sine

The oscillators presented to this point have limited tuning-frequency range. Although the circuit in **Fig 8a** is not a true oscillator, it produces a synthesized sine-wave output over a wide dynamic range. Many applications such as audio, shaker-table driving, and automatic test equipment require voltage-controlled oscillators (VCOs) that have sine-wave outputs. This circuit meets this need, spanning a range of 1 Hz to 1 MHz (equal to 6 decades or 120 dB) for a 0 to 10V input. The circuit maintains 0.25% frequency linearity and 0.40% distortion.

To understand the circuit, assume Q_5 is on and its collector (**Fig 8b**, trace A,) is at −15V, cutting off Q_1. IC_3, which inverts the positive input voltage and biases the summing node of integrator IC_1 through the 3.6-kΩ

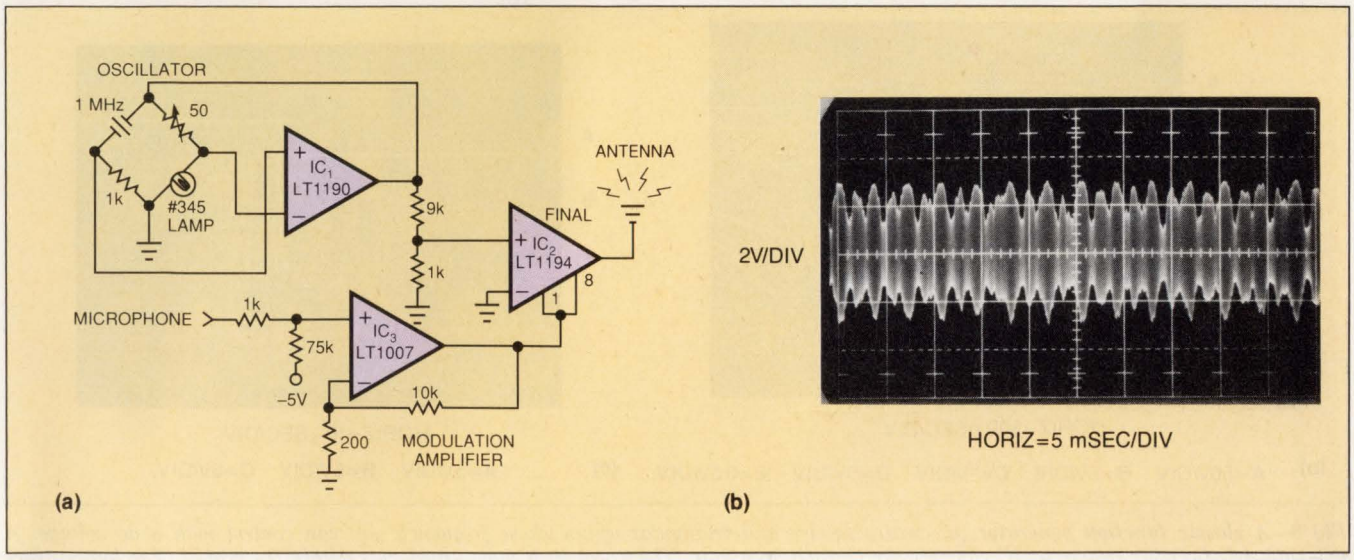

***Fig 7—Though perhaps not worthy of Wolfman Jack** or Dick Biondi, the circuit of **a** is still a complete AM radio station. When Chuck Berry picks his guitar and belts out "Johnny B. Goode," the modulated output looks like what you see in **b**.*

resistor and the self-biased FET's, pulls a current, −I, from the summing point. IC_2, a precision op amp, provides dc stabilization of IC_1. IC_1's output, (trace B,) ramps positive until IC_5's input, (trace C,) crosses zero and causes IC_5's inverting output to go negative. The Q_4/Q_5 level shifter then turns off, and Q_5's collector goes to +15V, allowing Q_1 to come on. The values of the resistors in Q_1's path result in a current, +2I, exactly twice the absolute magnitude of the current, −I, that flows out of the summing node. As a result, the net current into the junction becomes +I, and IC_1 integrates negatively at the same rate it did during its positive-going excursion.

When IC_1 integrates far enough in the negative di-

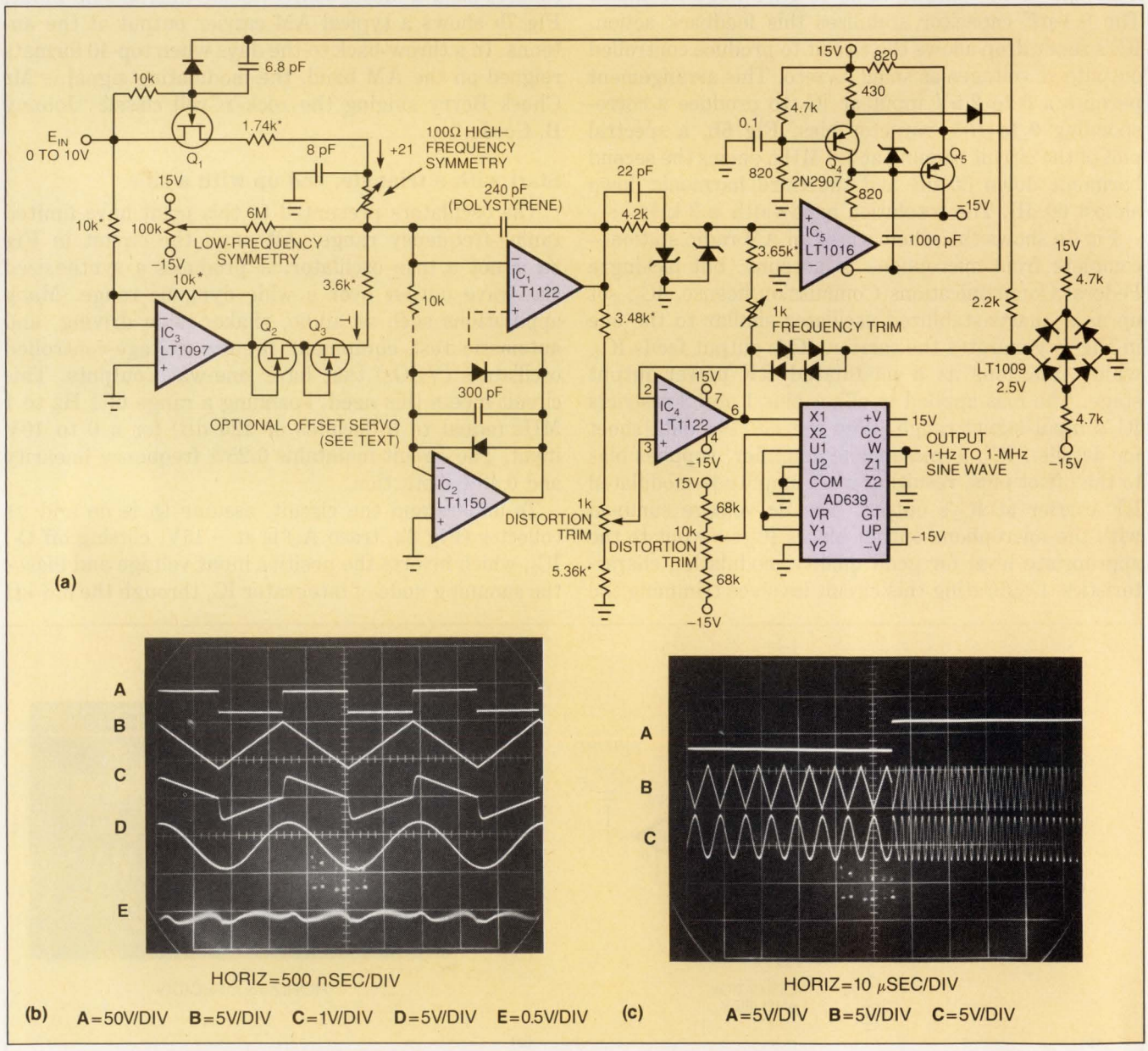

*Fig 8—**A classic function generator, a,** creates square and triangular waves whose frequency you can control with a dc voltage. A trigonometric-function generator IC converts the triangle to a sine. The traces in **b** show waveforms within the circuit. The lowest trace shows the residual distortion after you remove the output's fundamental-frequency component. In **c,** you see the circuit's quick and clean response to a command to change frequency.*

rection, IC_5's + input crosses zero and the circuit's two outputs change state. The state change switches the Q_4/Q_5 level shifter's state, causing Q_1 to go off and the entire cycle to repeat. The result is a triangular waveform at IC_1's output. The frequency of this triangle depends on the circuit's input voltage and varies from 1 Hz to 1 MHz with a 0 to 10V input. The LT1009 diode bridge and the series-parallel diodes provide a stable bipolar reference that always opposes the sign of IC_1's output ramp. The Schottky diodes bound IC_5's + input, ensuring its clean recovery from overdrive.

Sine of the times

The AD639 trigonometric function generator, biased via IC_4, converts IC_1's triangular output into a sine wave, (trace D). To avoid output distortion, you must supply the AD639 with a triangular wave that does not vary in amplitude. At higher frequencies, delays in the IC_1-integrator switching loop result in late turn-on and turn-off of Q_1. Unless you minimize these delays, the triangle amplitude will increase with frequency and cause the distortion level to increase. IC_5, the Q_4/Q_5 level shifter, and Q_1 generate a total delay of 14 nsec. This small delay, combined with the 22-pF feed-forward network at IC_5's input, keeps distortion to just 0.40% over the entire 1-MHz range. At 100 kHz, the distortion is typically less than 0.2%. The 8-pF capacitor in Q_1's source line minimizes the effects of gate-source charge transfer, which occurs whenever Q_1 switches. Without this capacitor, a sharp spike would occur at the triangle peaks, increasing distortion. FETs Q_2 and Q_3 compensate for the temperature-dependent on-resistance of Q_1 and keep the $+2I/-I$ relationship constant with temperature.

This circuit responds very rapidly to input changes—something most sine-wave generators cannot do. **Fig 8c** shows what happens when the input switches between two levels, (trace A). IC_1's triangle output (trace B), shifts frequency immediately, with no glitches or poor dynamics. The sine output, (trace C), reflecting this action, is similarly clean. To adjust this circuit, apply 10.00V and trim the 100Ω potentiometer for a symmetrical triangle output at IC_1. Next, apply 100 μV and trim the 100-kΩ potentiometer for triangle symmetry. Then, apply 10.00V again and trim the 1-kΩ frequency-trim adjustment for a 1-MHz output frequency. Finally, adjust the distortion-trim potentiometers for minimum distortion as measured on a distortion analyzer (**Fig 8b**, trace E). You may have to readjust the other potentiometers slightly to achieve the lowest possible distortion. If you won't operate the circuit below 100 Hz, you can delete the IC_2-based dc-stabilization stage. If you make this change, you should ground IC_1's positive input.

Many of the filter and oscillator circuits presented here are simple as well as useful. Their simplicity shows that clever circuit designers often take a minimalist approach. When you speak or write, you are more likely to get your point across if you use short words that are familiar to your audience. So it is with circuits. The simplest design that does the job usually costs the least and operates more reliably than complex alternatives. EDN

Author's biography

For more information on this article's author, turn to pg 163 in the October 10, 1991, issue.

Article Interest Quotient (Circle One)
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High-speed data-conversion circuits

The variety of circuits that prove useful in high-speed data conversion is almost limitless. Here is a collection of circuits that can turn out to be lifesavers in several situations.

Jim Williams, *Linear Technology Corp*

Any reasonably complete listing of the types of circuits that you can use in data conversion and analog/digital data acquisition would be long indeed. Although books have been written just on D/A and A/D converters, such circuits are hardly the only ones that prove useful in acquiring fast-changing analog signals. You almost can't mention ADCs without also bringing up sample and hold (S/H) circuits. Voltage-to-frequency converters offer a very attractive alternative to more conventional ADCs, especially where you need signal isolation or outstanding linearity. Comparators are the heart of any analog-to-digital conversion scheme. Trigger circuits let you view and capture waveforms that recur at intervals that aren't perfectly periodic. Time-to-voltage converters let you see how pulse widths and time intervals vary as a function of time, and rms-to-dc converters extract an important property of ac signals—their heating value. There is a measure of commonality among the techniques you use to design such circuits. Here for your entertainment and edification is a potpourri of useful circuits that perform diverse functions.

In **Fig 1a**, the LT1016 comparator and the LT1122 high-speed FET amplifier combine to form a high-speed V/F converter. A variety of circuit techniques yields a 1-Hz to 10-MHz output. The circuit continues to function with a 20% overrange ($V_{IN}=12V$; $f_{OUT}=12$ MHz). This circuit has a wider dynamic range (140 dB, or seven decades) than any unit available commercially. The 10-MHz full-scale frequency is 10× as high as that of currently available monolithic V/F converters.

The theory of operation depends on the identity $Q=CV$. Each time the circuit produces an output pulse, it feeds back a fixed quantity of charge (Q) to a summing node (7). The circuit's input furnishes a comparison current at the summing node and a monitoring amplifier's feedback capacitor integrates the difference signal. The amplifier controls the circuit's output-pulse generator, completing a feedback loop around the integrating amplifier. To maintain the summing node at zero, the pulse generator runs at a frequency at which the pumped charge just offsets the current produced by the input signal. Thus, the output frequency is linearly proportional to the input voltage.

IC_1 is the integrating amplifier. Stabilizing IC_1 with IC_2, a chopper-stabilized op amp, produces 0.05 μV/°C of offset drift. IC_2 measures the dc value of the negative input, compares it with ground, and forces the positive input to maintain the offset balance in IC_1.

Note that IC_2 is an integrator that cannot see high-frequency signals. It functions only at dc and low frequencies.

Integrator IC_1 has a 68-pF feedback capacitor. When you apply a positive voltage to the input, IC_1's output integrates in a negative direction (**Fig 1b,** trace A). During this period, IC_5's inverting output is low. The paralleled HCMOS inverters form a reference-voltage switch. The LT1034s (driven by the LM134 current source and the Q_3/Q_4 combination) establish the reference voltage; a small input-voltage-related term adds to the reference, improving overall circuit linearity.

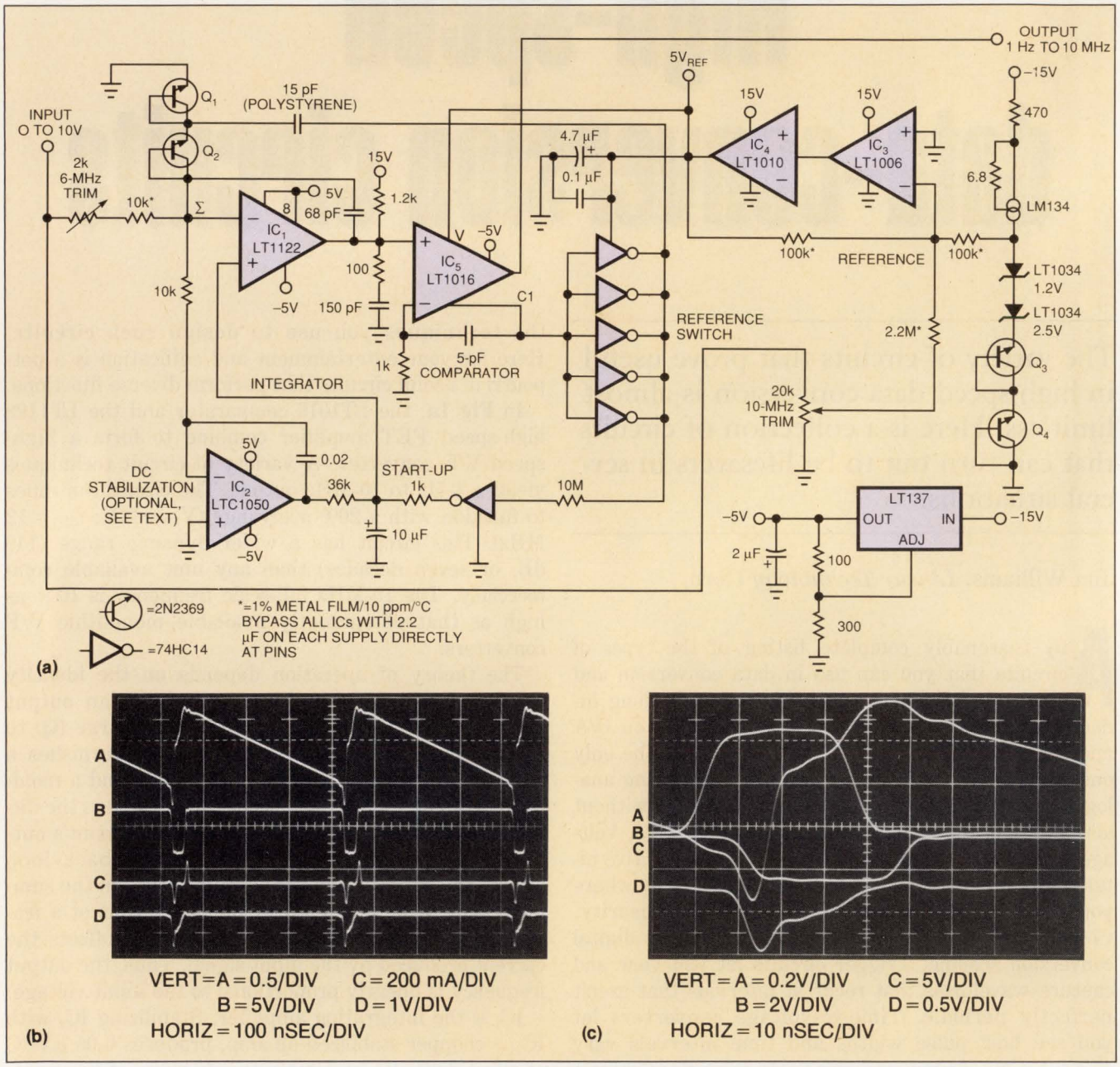


Fig 1—A voltage-to-frequency converter *with a maximum output frequency of 10 MHz and a 140-dB dynamic range is only moderately complex (**a**). In **b**, you see the circuit waveforms; **c** is an expanded view of the discharge-reset sequence upon which the circuit performance depends.*

an integrator, is the actual hold amplifier. Its output feeds back to the switching bridge's input, forming a summing point with IC_1's output resistor. This feedback loop enhances accuracy by placing the bridge within a loop.

Driving the S/H input line switches the bridge. Q_1 and Q_2 drive L_1's primary. L_1's secondaries provide complementary drive to the bridge with negligible time skew.

Fig 2b shows the circuit acquiring a full-scale step. Trace A is the input command; trace B is IC_2's output. The aberration (that is, the "hold step") visible in IC_2's output when the circuit switches into the hold mode is the result of minute residual ac imbalances in the bridge. **Fig 2c** illustrates this effect in high-resolution detail, with the "hold-step trim" deliberately disconnected. After IC_2's output nominally settles at final value, the circuit switches into the hold mode. The bridge imbalance dumps a small parasitic charge into IC_2's summing point, in this case causing IC_2 to step 10 mV higher. Properly connected and adjusted, the trim supplies a small compensatory charge during switching. **Fig 2d** shows the effect of this compensation on the output. The settled hold-mode output is the same as the acquired input voltage. To trim this circuit, ground the input while pulsing the S/H control line. Next, adjust the trim for a minimal amplitude step between the S/H states.

In contrast to low-frequency S/H circuits, this circuit, if left in the sample mode, cannot pass a signal. The transformers' inherent ac coupling prevents the circuit from providing a dc output. Moreover, extending the sample-mode duration beyond 500 nsec will saturate the transformers, causing erroneous outputs and excessive dissipation in Q_1 and Q_2. If the control input can remain in the high state for extended periods, you should ac-couple the control signal.

Compare currents in 15 nsec

Fig 3a shows a way to build a high-speed current comparator with resolution in the 12-bit range. Comparing currents, which is the fastest way to compare DAC outputs with analog values, is a common technique in high-speed instrumentation, especially in high-speed A/D converters. IC_1 is a Schottky-bounded amplifier. The bounding diodes hold down the response time by preventing summing-point overdrive from causing IC_1 to saturate. Select the capacitor—it compensates for the DAC output capacitance—for the best amplifier damping; the 3-pF value shown is typical. The feedback resistor maximizes the circuit's gain-bandwidth product; the 10-kΩ value shown is also typical. Voltage gains of 4 to 10 are common.

Fig 3b shows the circuit's performance. Trace A, a test input, causes IC_1's output (trace B) to slew through zero (the screen's center horizontal line). When IC_1 crosses zero, IC_2's input goes negative and IC_2 responds 10 nsec later with a TTL output (trace C). The total time from when the test input reaches the TTL high threshold until the comparator output level becomes a TTL high is <15 nsec.

Fig 4a is an extremely versatile trigger circuit. Designing a fast, stable trigger is not easy, and often entails a considerable number of discrete components.

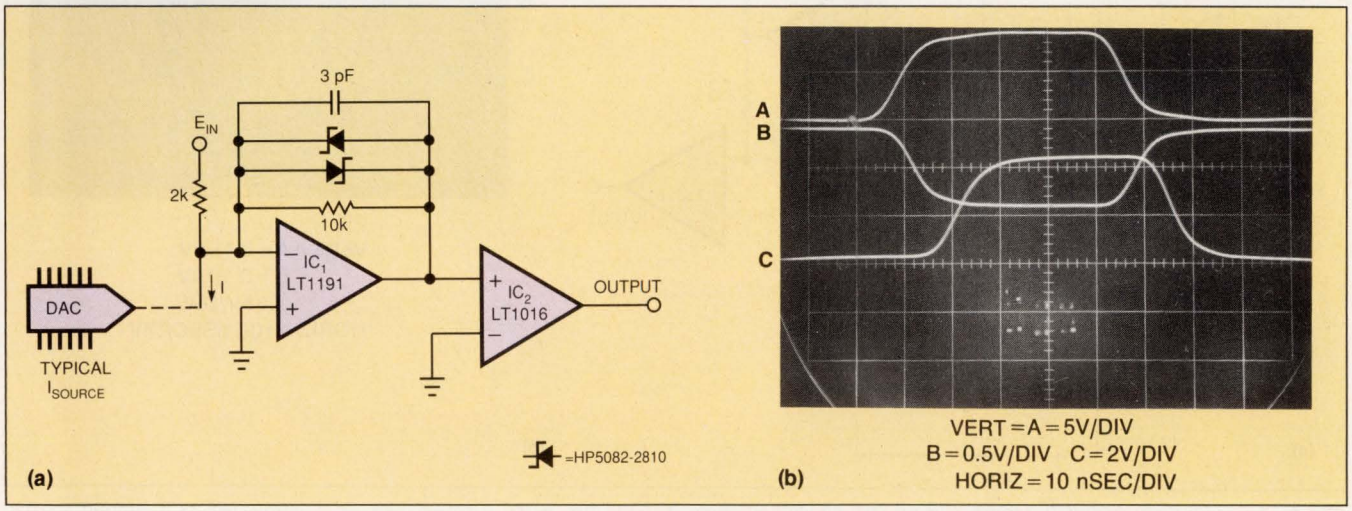


***Fig 3—Only two ICs yield a fast** summing comparator **(a)**. In **b**, you can observe key waveforms as the circuit operates.*

This circuit, without level adjustment, triggers reliably from dc to 50 MHz over a 2 to 300-mV input range.

IC_1, a gain-of-10 preamplifier, feeds an adaptive trigger configuration that maintains the output comparator's (IC_3's) trip point at one-half the input-signal amplitude, regardless of the signal's magnitude. The self-adjusting trip point ensures reliable automatic triggering over a wide input-amplitude range, even for very low-level inputs. As an option, the network (shown in dashed lines in **Fig 4a**) permits changing the trip threshold. The adjustment lets you select any point on the input-waveform edge as the trigger point.

Fig 4b shows the performance for a 40-MHz input sine wave (trace A). At IC_1's output (trace B), the input signal has received voltage gain with little or no phase shift. Comparator IC_3 gives a clean logic output (trace C). At the highest frequencies, bandwidth limiting can occur in IC_1, but it is irrelevant; the adaptive trigger threshold will simply vary in proportion to the input to maintain the circuit output.

The circuit of **Fig 5a** lets you determine very short pulse widths (in this case, 250 nsec full scale) with a typical error of 1%. Digital methods of achieving similar results dictate GHz clock speeds, and thus result in cumbersome implementations. In addition, processor-based approaches that use averaging techniques require repetitive pulses; this circuit does not. Circuits of the type shown in **Fig 5a** frequently appear in automatic test equipment and nuclear and high-energy physics work, where measuring the width of short pulses is a common requirement.

The circuit functions by charging a capacitor for the duration of the pulse. When the pulse ends, the charging ceases, and the voltage across the capacitor is proportional to the width of the pulse.

The pulse whose width is to be measured (**Fig 5b**, trace A) simultaneously biases the 74C221 dual one-shot and Q_3. Q_3, aided by Baker clamping, feed-forward capacitance, and optimized dc base biasing, turns off in a few nsec. Current source Q_2's emitter becomes forward biased, and Q_2 supplies constant current to the 100-pF integrating capacitor. Q_1 supplies temperature compensation for Q_2 and the 2.5V LT1009 provides the current-source reference. The 100-pF capacitor at Q_2's collector charges in ramp fashion (trace B). IC_1 supplies a buffered output (trace C). When the input

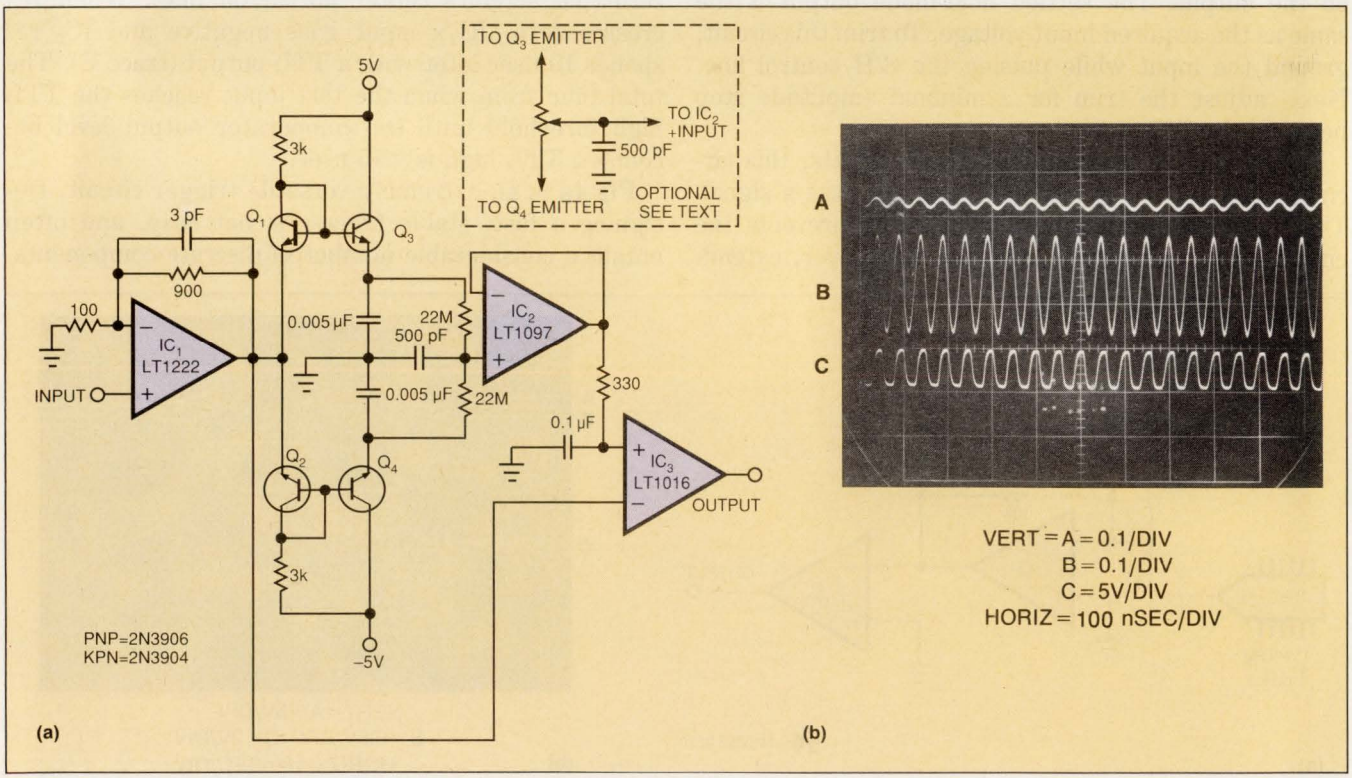


Fig 4—An extremely versatile trigger *circuit (**a**) consists of three ICs and two pairs of transistors, each connected as a current source. The circuit adjusts its threshold as the amplitude of the incoming signal varies. In **b**, you see waveforms during circuit operation.*

IC_3 and IC_4 provide low-drift buffering and present a low-impedance reference to the supply pins of the paralleled inverters. The HCMOS outputs give essentially error-free low-resistance switching. The reference switch's output charges the 15-pF capacitor via the path that includes Q_1.

When IC_1's output crosses zero, IC_5's inverting output goes high and the reference switch (trace B) goes to ground, causing the 15-pF capacitor to dispense charge into the summing node via Q_2's base-emitter junction. The amount of charge dispensed is a direct function of the voltage that had existed across the 15-pF capacitor ($Q=CV$). Q_3 and Q_4 in the reference string provide temperature compensation for Q_1 and Q_2. The current that flows through the 15-pF capacitor (trace C) reflects the charge-pumping action. Removing current from IC_1's summing junction (trace D) drives the junction negative very quickly. The initial negative-going 15-nsec transient at IC_1's output results from amplifier delay.

The input signal feeds directly through the feedback capacitor and appears at the output. When the amplifier finally responds, its output (trace A) slew limits as the amplifier attempts to regain control of the summing node. The 1.2-kΩ pull-up resistor and the RC damper at IC_1's output enhance the amplifier's recovery from slewing. The amount of time the reference switch remains at ground depends on the 5-pF/1000Ω hysteresis network at IC_5 and on how long IC_1 takes to recover. A 60-nsec interval is long enough for the 15-pF capacitor to fully discharge. After the discharge, IC_5 changes state, the reference switch swings positive, the capacitor recharges, and the entire cycle repeats. The frequency at which this oscillation occurs is directly proportional to the current into the summing junction, and, in turn, to the input voltage. Any input current will dictate an oscillation frequency that holds the summing point at an average value of zero.

At MHz frequencies, maintaining a linear relationship between the input voltage and the output frequency places severe restrictions on the circuit timing. The key to achieving a 10-MHz full-scale operating frequency is the ability to transmit information around the loop very quickly. The discharge-reset sequence detailed in **Fig 1c** is particularly critical.

Fig 1c, trace A is the output of integrator IC_1. Its ramp output crosses zero at the first vertical graticule division on the left. A few nsec later, IC_5's inverting output begins to rise (trace B), switching the reference switch to ground (trace C). The reference switch begins to head towards ground about 16 nsec after IC_1's output crosses zero. Two nanoseconds later, the summing point (trace D) begins to go negative as current flows from it through the 15-pF capacitor. At 25 nsec, IC_5's inverting output is fully positive, the reference switch is at ground, and the summing point is at its negative extreme. Now, IC_1 begins to take control. Its output (trace A) slews rapidly in the positive direction, restoring the summing point. At 60 nsec, IC_1 is in control of the summing node and the integration ramp begins again.

Come on, get going

Start-up and overdrive conditions could force IC_1's output to go to the negative rail and stay there. The ac-coupled nature of the charge-dispensing loop can preclude normal operation and cause the circuit to latch. The remaining HCMOS inverter provides a "watchdog" function for this condition. If IC_1's output goes to the negative rail, the reference switch tries to stay at ground. The remaining inverter goes high, lifting IC_1's positive input, causing IC_1's output to slew positive, and thus initiating normal circuit action. The 1-kΩ/10-μF combination and the 10-MΩ resistor in series with the inverter input limit the loop bandwidth during start-up, preventing unwanted outputs.

The LM134 current source that drives the reference string has a built-in 0.33%/°C thermal coefficient, causing a slight voltage modulation in the Q_3/Q_4 pair over temperature. This small change (~+120 ppm/°C) opposes the −120 ppm/°C drift in the 15-pF polystyrene capacitor and reduces the temperature coefficient of the complete circuit.

Acroynms used in this article

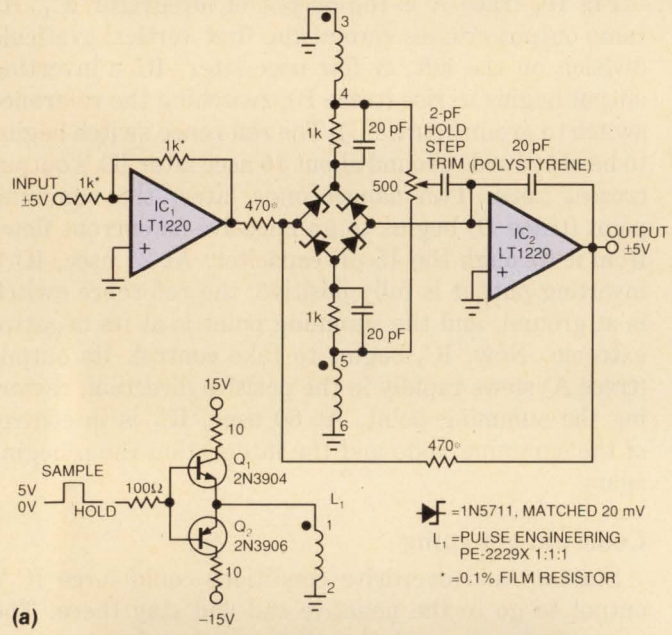
ac—Alternating current
A/D—Analog-to-digital
ADC—Analog-to-digital converter
D/A—Digital-to-analog
DAC—Digital-to-analog converter
dc—Direct current
FET—Field-effect transistor
LSB—Least-significant bit
RC—Resistance-capacitance
rms—Root-mean-square
S/H—Sample and hold
TTL—Transistor-transistor logic
V/F—Voltage to frequency
VFC—Voltage-to-frequency converter

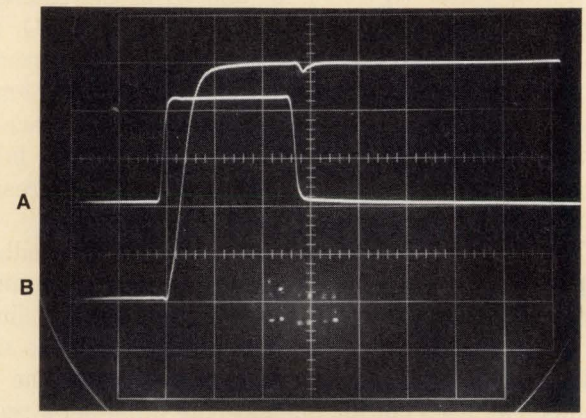
To trim this circuit, apply exactly 6V at the input and adjust the 2-kΩ potentiometer for 6.000-MHz output. Next, put in exactly 10V and trim the 20-kΩ potentiometer for a 10.000-MHz output. Repeat these adjustments until both points stay fixed. IC_2's low drift eliminates a zero adjustment. If operation below 600 Hz is not required, you can delete IC_2 and its associated components.

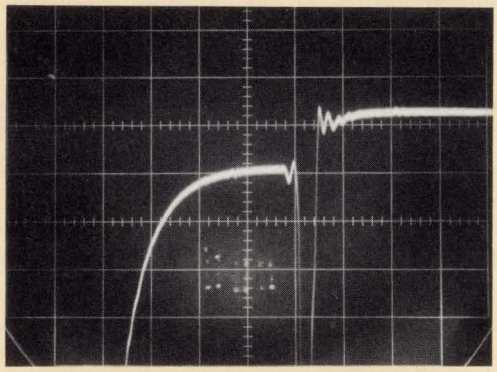
Nonlinearity of this circuit is 0.03% and full-scale drift is 50 ppm/°C. Zero-point error, controlled by IC_2, is 0.05 Hz/°C.

Fig 2a shows a simple, very fast S/H circuit. This circuit will acquire a 5V input to 8-bit accuracy in 100 nsec. The hold step amplitude is less than ¼ LSB, and hold settling time is less than 25 nsec. The aperture time is 4 nsec, and the droop rate is about ½ LSB in 1 μsec.

Inverting buffer IC_1 feeds the input to a Schottky switching bridge. The Schottky bridge, which is similar to types used in sampling oscilloscopes, switches in 1 nsec and eliminates the charge pump-through that an FET switch would contribute. The switching bridge's output feeds output-amplifier IC_2. IC_2, configured as







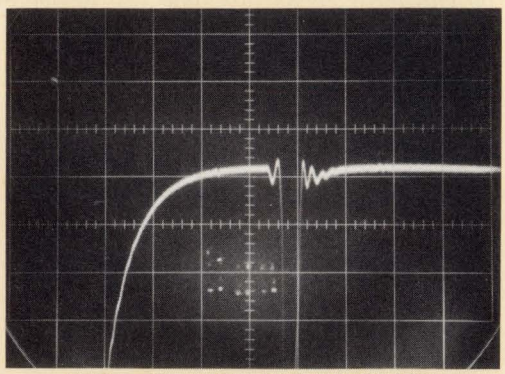


Fig 2—This very fast S/H circuit (a), *acquires signals to 8-bit accuracy in 100 nsec. In* **b** *you see the waveforms within the circuit. Accurate operation depends on cancellation of the switching signals that feed through the bridge. In* **c**, *the compensation is disconnected. In* **d**, *you can see the effect of the compensation.*

pulse ends, Q_3 turns on rapidly, reverse-biasing Q_2's emitter and turning off the current source. IC_1's voltage is directly proportional to the input pulse width. A monitoring A/D converter can acquire this data.

After an interval set by the 74C221's delay (a resistor and a capacitor set the delay), a pulse appears at the circuit's Q_2 output (trace D). This pulse turns on Q_4, discharging the 100-pF capacitor to zero and readying the circuit for the next input pulse.

This circuit's accuracy and resolution depend strongly on keeping the delay in switching the Q_1/Q_2 current source very short. **Fig 5c** provides amplitude and time-expanded versions of critical circuit waveforms. Trace A is the input pulse and trace B is IC_1's input, showing the beginning of the ramp's ascent. Trace C, IC_1's output, shows a delay of about 13 nsec from IC_1's input. Traces D and E, also IC_1's input and output, record similar delays introduced by IC_1 at the ramp turn-off. The photo reflects the extremely fast current-source switching; IC_1 causes most of the delay. IC_1's delay is far less critical than the current-source-switching delays. IC_1 will always settle to the correct

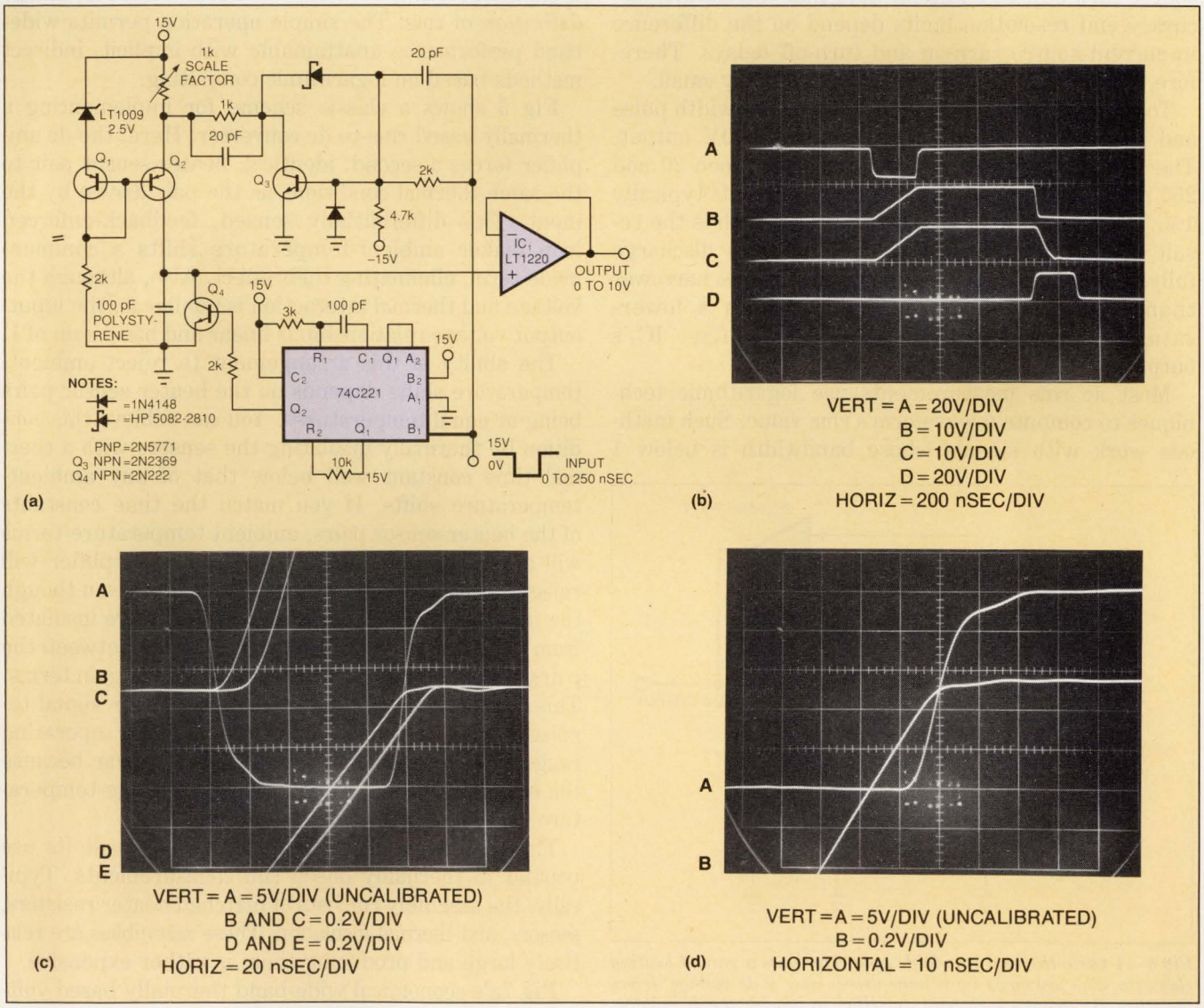


Fig 5—Changing pulse widths to voltages *provides a convenient way to monitor changes in time intervals that occur as a function of time. The circuit in* **a** *performs this function. In* **b** *you see circuit waveforms. These waveforms appear in expanded form in* **c**. *The current-source turn-off appears in* **d**.

value well before the one-shot resets the circuit. In practice, you should not trigger a monitoring A/D converter until about 50 nsec after the circuit's input pulse has ceased. This delay gives IC_1 plenty of time to catch up to the 100-pF capacitor's settled value.

As mentioned, fast current-source switching is essential for good results. **Fig 5d** details the current-source turn-off. Trace A is the circuit's input-pulse rising edge, and trace B shows the "top" of the ramp. Turn-off occurs in a few nanoseconds. Similar speed is characteristic of the input's falling edge (current-source turn-on). In addition, note that the circuit's accuracy and resolution limits depend on the difference in current-source turn-on and turn-off delays. Therefore, the effective overall delay is extremely small.

To calibrate this circuit, apply a 250-nsec-width pulse and trim the 1-kΩ potentiometer for a 10V output. The circuit will convert pulse widths between 20 and 250 nsec to voltages with an accuracy that is typically 1%. The 20-nsec minimum-measurable width is the result of the 100-pF capacitor's inability to discharge fully. If you must measure the width of pulses narrower than 20 nsec, you can replace Q_4 with a lower-saturation-voltage device or you can offset IC_1's output.

Most ac rms measurements use logarithmic techniques to compute a waveform's rms value. Such methods work with signals whose bandwidth is below 1 MHz and whose crest factor is less than about 10. Practically speaking, a waveform's ability to heat a resistive load defines its rms value. Specialized instruments employ thermally based assemblies that compute the rms values of input signals. Compared with logarithmically based converters, thermal methods work over a substantially wider bandwidth and produce accurate results with signals that have much higher crest factors (ratio of peak to rms voltage).

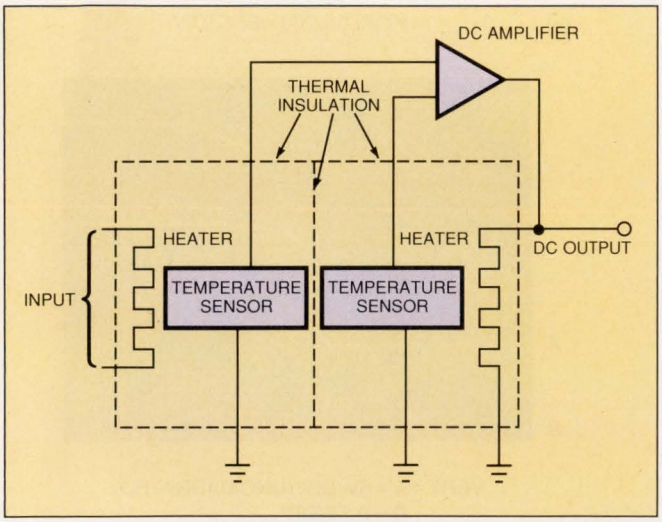


Fig 6—A basic thermal rms-to-dc converter *uses a pair of heating elements. The unknown ac voltage drives one; a dc voltage drives the other. By using a high-gain amplifier to provide the dc voltage, you force the heating effect of the dc to equal that of the ac. Hence the rms value of the dc and ac are equal. Thus, when you measure the dc voltage, you are measuring the rms ac voltage.*

Thermal rms-to-dc converters are direct acting, thermoelectronic analog computers. The thermal technique is explicit, relying on "first principles"—that is, on the *definition* of rms. The simple operation permits wideband performance unattainable with implicit, indirect methods based on logarithmic computing.

Fig 6 shows a classic scheme for implementing a thermally based rms-to-dc converter. Here, the dc amplifier forces a second, identical, heater-sensor pair to the same thermal conditions as the pair driven by the input. This differentially sensed, feedback-enforced loop makes ambient-temperature shifts a common-mode term, eliminating their effect. Also, although the voltage and thermal interaction is nonlinear, the input-output voltage relationship is linear and has a gain of 1.

The ability of this arrangement to reject ambient-temperature shifts depends on the heater-sensor pairs being at equal temperatures. You can achieve this condition by thermally insulating the sensors with a thermal time constant well below that of any ambient-temperature shifts. If you match the time constants of the heater-sensor pairs, ambient temperature-terms will affect the pairs equally and the dc amplifier will reject this common-mode term. Note that, even though the pairs are at equal temperatures, they are insulated from each other. Any thermal interaction between the pairs reduces the system's thermally based gain terms. This interaction would cause unfavorable signal-to-noise performance and limit the dynamic operating range. The output of **Fig 6**'s circuit is linear because the matched thermal pairs' nonlinear voltage-temperature relationships cancel each other.

The advantages of this approach have made its use popular in thermally based rms measurements. Typically, the assembly consists of matched heater resistors, sensors, and thermal insulation. These assemblies are relatively large and producing them is rather expensive.

Fig 7a's economical wide-band thermally based voltmeter uses a monolithic thermal converter. The LT1223 amplifier provides gain and drives the LT1088 rms-to-dc thermal converter. The supply biases the

LT1088's temperature-sensing diodes. IC_1, set up as a differential servo amplifier with a gain of 9000, extracts the diode's difference signal and biases Q_1. Q_1 drives one of the LT1088's heaters, completing a loop. The 3300-pF capacitor gives a stable roll-off. The 1.5-MΩ/0.0225-μF combination improves settling by reducing the gain during output slewing. The LT1088's square-law thermal gain makes the overall loop gain lower for small inputs. Normally, the low gain would cause slow settling for values below about 10 to 20% of full scale. The LT1004 1-kΩ/3-kΩ network provides a simple breakpoint that boosts the amplifier gain at low signal levels to improve settling. IC_2, a gain-trimmable output stage, compensates for gain variations in the two sides of the LT1088.

To trim the circuit, apply a dc signal of about 10% of full scale (that is, 0.05V) and adjust the "zero trim" so that $V_{OUT} = V_{IN}$. Next, apply a full-scale dc input and set the full-scale trim for a full-scale output. Repeat the trims until both errors are well below 1% of full-scale. An alternate trimming scheme involves applying no input, grounding Q_1's base, and adjusting the zero trim until IC_1's output is active. Then you disconnect Q_1's base from ground, apply a full-scale input, and trim the full-scale adjustment to produce a full-scale output.

Fig 7b is a plot of the circuit's error vs input fre-

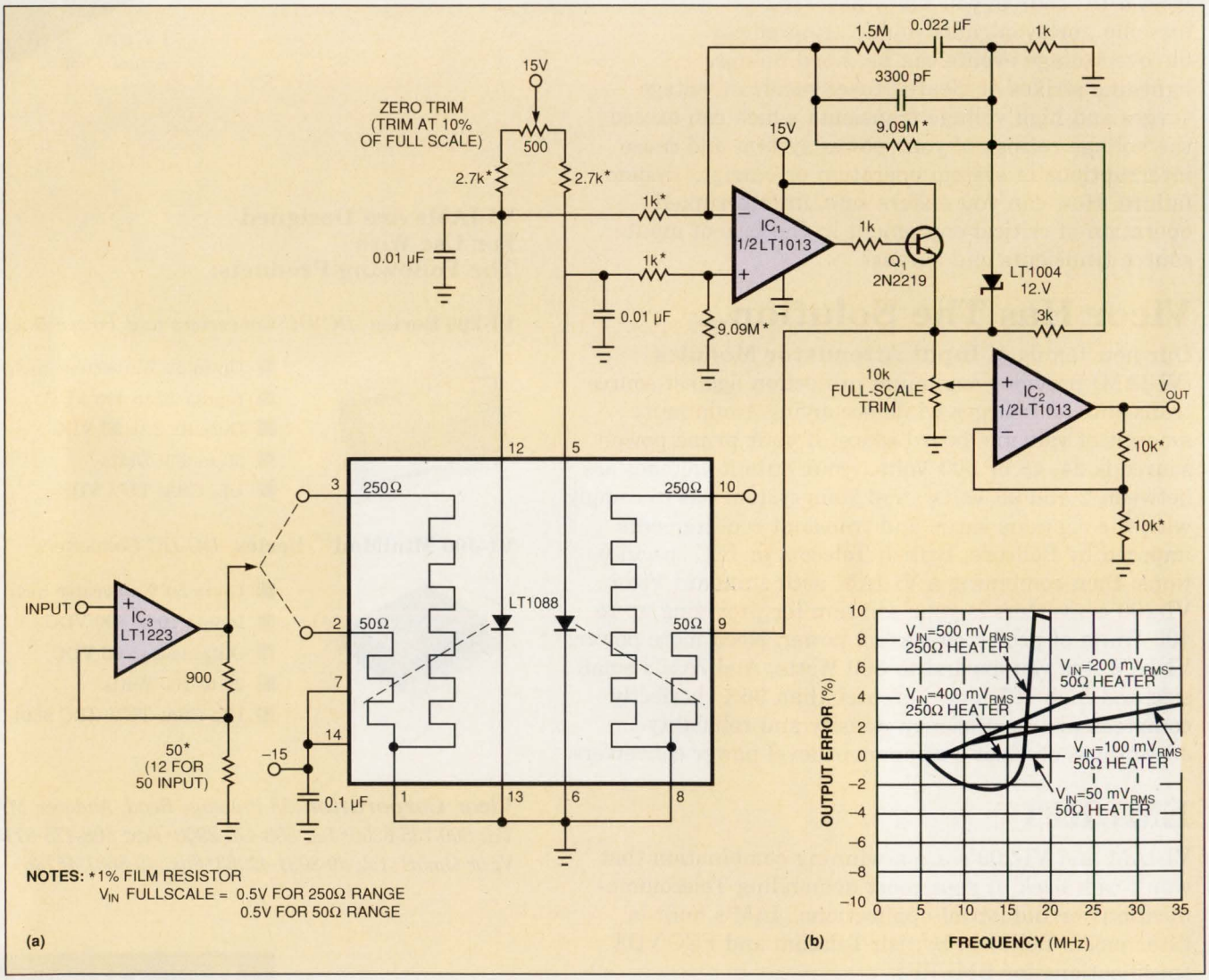


Fig 7—A functioning rms-to-dc converter *appears in* ***a****. In* ***b****, you see the circuit's error vs frequency for several input-signal amplitudes and for two values of heater resistance.*

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quency. When you apply your input to one of the 50Ω heaters, the LT1088's error spec is 2% to 100 MHz; using a 250Ω heater, the spec is 1% to 20 MHz. Most of the error shown results from bandwidth restrictions in IC_3, but the performance is still impressive. The plots include data taken at various input levels into both a high and a low-resistance heater. The error in the response to a 500-mV input into the 250Ω heater rises to 1% at 8 MHz, and 2.5% at 14 MHz before peaking badly beyond 17 MHz. This input level forces a 9.5V-rms output at IC_3, and introduces large-signal bandwidth limitations. The 400-mV input to the 250Ω heater produces essentially flat response to 20 MHz, the LT1088's 250Ω-heater specification limit.

The 50Ω heater provides significantly wider bandwidth, although in the circuit of **Fig 7a**, IC_3's 50-mA output limits the maximum input to about 100-mV rms (1.76V rms at the LT1088).

As you can see, the circuits discussed here are useful in their own right. They are also thought provoking. You can combine and modify them virtually without limit, and in so doing, produce new circuits that perform many other useful functions. EDN

Author's biography

For more information on this article's author, turn to pg 163 in the October 10, 1991 issue.

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High-speed communications circuits

High-frequency communications signals need wideband analog circuits. High-speed monolithic amplifiers let you build simple, effective circuits to meet this need for both optical and RF transmission.

Jim Williams, *Linear Technology Corp*

Megahertz-range data transmission and communications requires wideband linear circuitry. By designing around a monolithic high-speed amplifier, you can easily implement a variety of standard high-performance communications circuits. The following circuits detail several such designs for both optical and RF transmission. All have been carefully worked out and can serve as good idea sources.

Amplifying fast photodiode signals over a wide range of optical intensity is one common optical-communications requirement. **Fig 1a**'s fast FET amplifier gives wideband operation for 5 decades of photocurrent. You set up the photodiode in the conventional manner and use a −15V bias to aid diode response. Photocurrent feeds directly to IC_1's summing point, which causes IC_1's output signal to move to whatever level is required to maintain virtual ground at the negative input pin. **Fig 1b** details the circuit's operating characteristics when using the HP5082-4204 photodiode.

You must use care when frequency-compensating this circuit. The diode has approximately 2 pF of parasitic capacitance, which creates a significant lag at IC_1's summing point. Without a feedback capacitor, the circuit's high-speed dynamics are poor. **Fig 1c** illustrates this point by showing the circuit's response to a photocurrent input pulse (trace A) when the 3-pF feedback capacitor is removed. IC_1's output voltage (trace B) overshoots and saturates before finally ringing down to its final value. Replacing the feedback capacitor gives **Fig 1d**'s results. The same input pulse (trace A) produces a cleanly damped output voltage (trace B). The capacitor, however, imposes a 50% speed penalty (note that the horizontal scale of **Fig 1d** is faster than that of **Fig 1c**). This penalty is unavoidable because suppressing the parasitic ringing's relatively low frequency mandates significant roll-off.

Basic amplifier has many uses

You can use the basic photodiode amplifier as the foundation for a variety of measurement and communications circuits. One such measurement circuit is **Fig 2a**'s photointegrator. The output voltage represents the integral of the diode's photocurrent over a time period defined by the control line. This circuit is par-

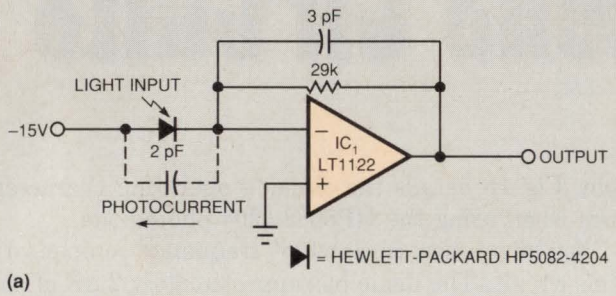
ticularly useful for measuring the total energy in a light pulse or pulses. The circuit is a fast integrator and uses IC_{2A} as a reset switch. IC_{2B}, which the control input signal switches simultaneously with IC_{2A}, compensates for IC_{2A}'s charge-injection error.

When the control input line is low (**Fig 2b,** trace A) and no photocurrent is present, IC_{2A} is closed and IC_1 acts as a grounded follower. Under these conditions, IC_1's output signal (trace C) sits at 0V. When the control input line goes high, IC_1 becomes an integrator as soon as IC_{2A} opens. Due to the switch delay, IC_2 opens approximately 150 nsec after the control input line goes high.

When IC_{2A} opens, it delivers some parasitic charge to IC_1's summing point. IC_{2B} provides a compensatory charge-based pulse at IC_1's positive terminal to cancel the effects of IC_{2A}'s charge error. The combined effect of the two charge pulses shows up as a fast, small amplitude event in IC_1's output, which settles rapidly back to 0V. You can see this event on trace C near the 400-nsec mark.

Once the switches have opened, the integrator is ready to receive and record a light pulse. When a light pulse (trace B) falls on the photodiode, IC_1 responds by integrating (trace C). With the circuit as shown in **Fig 2a,** IC_1 integrates rapidly until the light pulse ceases. IC_1's voltage after the light event is over is related to the total energy the photodiode sees during the event. In typical operation, the control line then returns low, which resets IC_1 for the next light event.

When the circuit has only 10 pF of integration capacitance, its output droop rate is about 0.2V/μsec. You

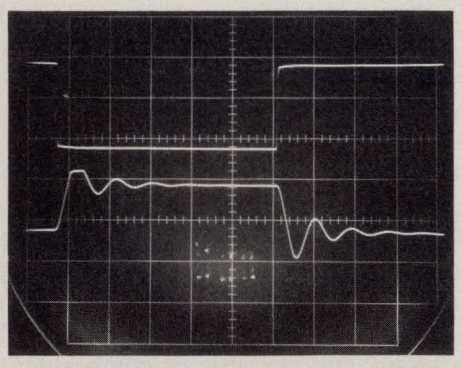


(a)

RESPONSE DATA

LIGHT (900 nm)	DIODE CURRENT	CIRCUIT OUTPUT
1 mW	350 μA	10.0V
100 μW	35 μA	1V
10 μW	3.5 μA	0.1V
1 μW	350 nA	0.01V
100 nW	35 nA	0.001V

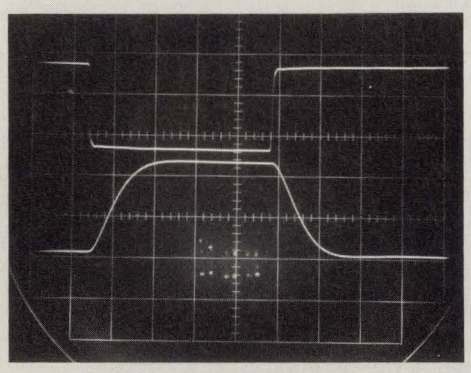
(b)



HORIZONTAL SCALE=500 nSEC/DIV

TRACE	VERTICAL SCALE
A	175 μA/DIV
B	10V/DIV

(c)



HORIZONTAL SCALE=200 nSEC/DIV

TRACE	VERTICAL SCALE
A	175 μA/DIV
B	5V/DIV

(d)

Fig 1—This basic photodiode amplifier circuit (a) *handles 5 decades of light intensity. The table* ***(b)*** *details the circuit's operating characteristics with the HP5082-4204 diode. Parts* ***c*** *and* ***d*** *show the circuit's response (trace B) to an input signal (trace A) without and with compensation, respectively.*

can increase the capacitance, but the integration speed will suffer accordingly. As shown, the circuit accommodates integration times of nanoseconds to milliseconds and photocurrents ranging from nanoamperes to hundreds of microamperes. Thus, light pulses with optical-power intensities spanning microwatts to milliwatts over wide ranges of duration are practical input signals.

The primary factors restricting the circuit's accuracy are IC_1's 75-pA bias current and 12V output swing and the effectiveness of the charge-cancellation network. Typically, the circuit can achieve full-scale accuracy within several percent if you trim the charge-cancellation network. To trim the network, make sure that no light falls on the diode while you repetitively pulse the control line. Adjust the trimmer capacitor to achieve a 0V output at IC_1 immediately after the disturbance associated with the IC_{2A}-IC_{2B} switching settles.

A communications circuit that relies on the basic photodiode amplifier is the simple fiber-optic receiver in **Fig 3a.** IC_1, a photocurrent-to-voltage converter similar to **Fig 1a,** feeds comparator IC_2. IC_2 compares IC_1's output voltage to a dc level established by the

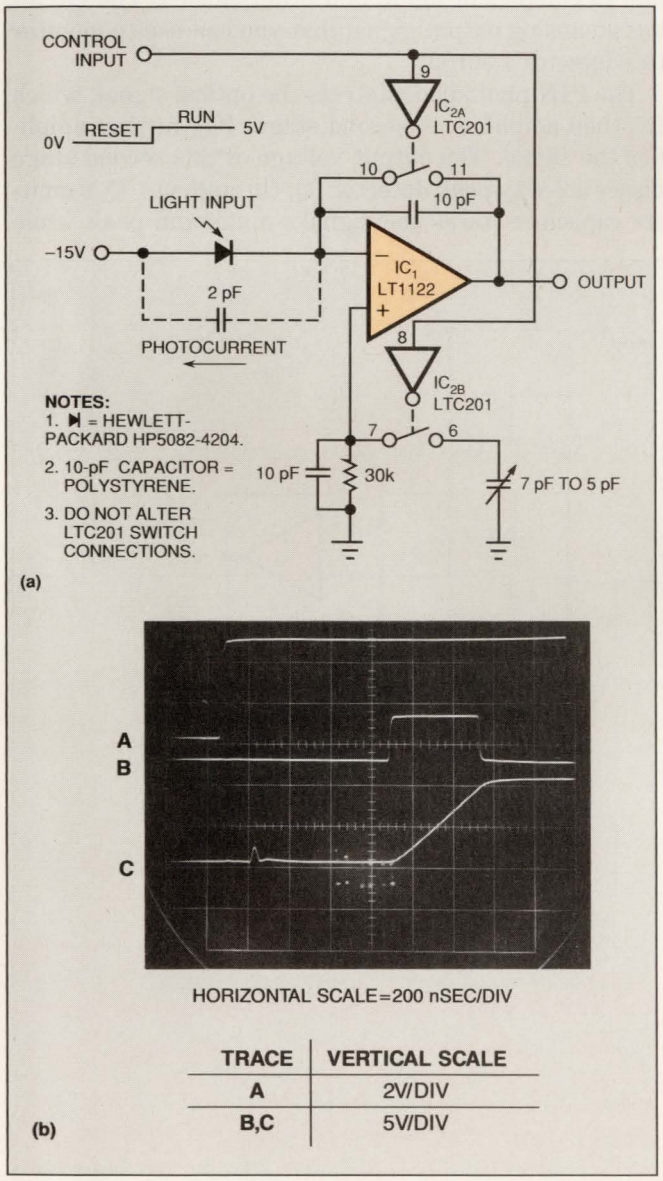


Fig 2—The basic photodiode amplifier is the basis for this integrator, *which has a resettable output* ***(a).*** *When the control line is high* ***(b,*** *trace A), the circuit integrates (trace C) the incoming signal (trace B).*

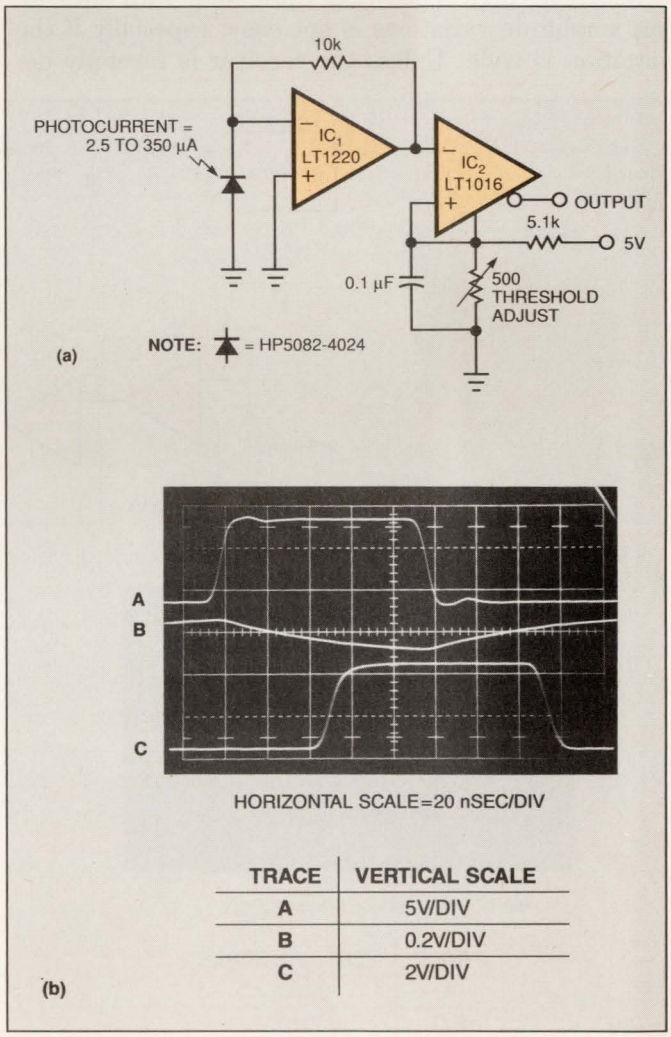
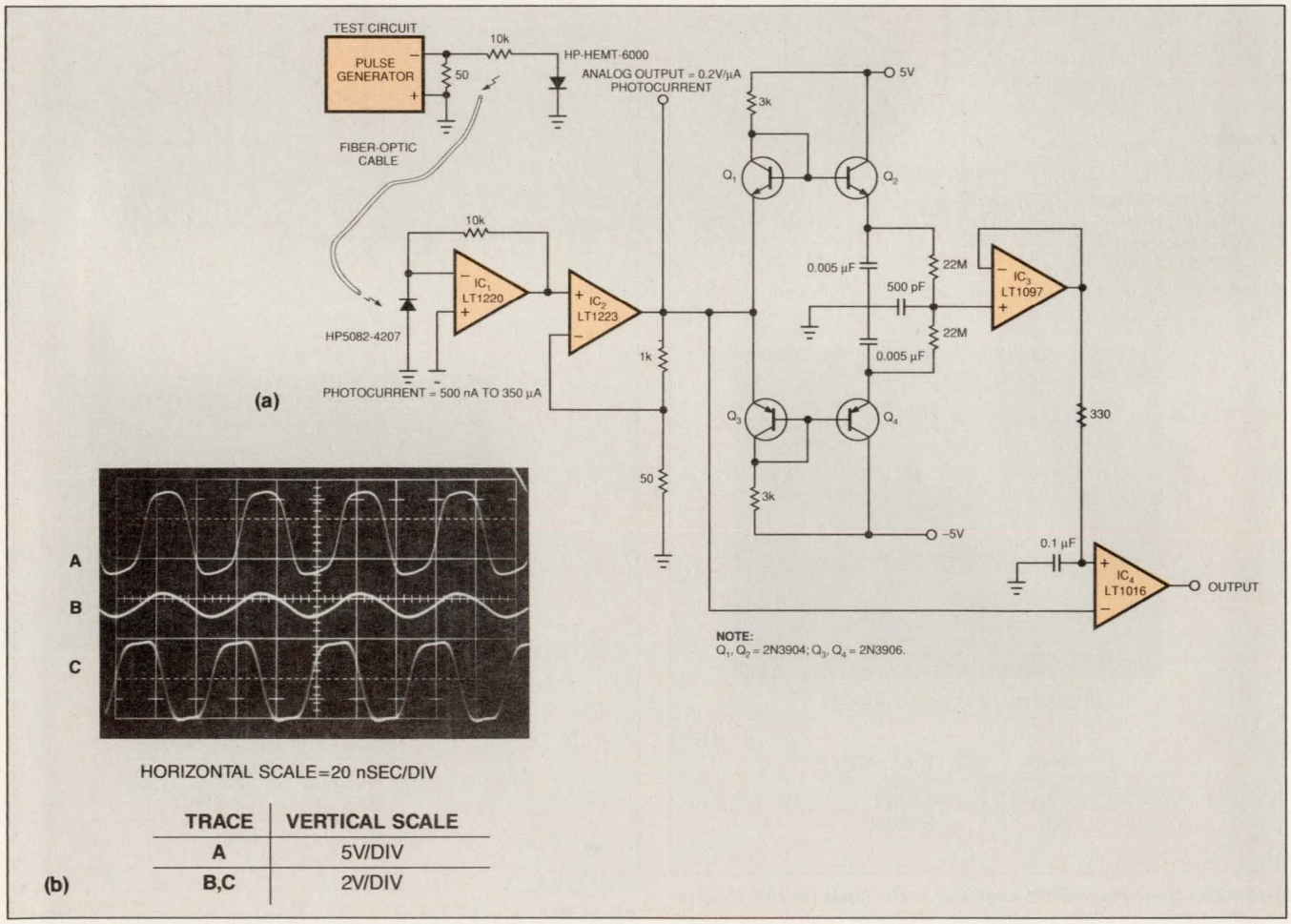


Fig 3—This simple optical receiver (a) *has a fixed signal threshold. The outputs of IC_1 (**b,** trace B) and IC_2 (trace C) lag the input signal (trace A).*

threshold-adjust potentiometer, thus producing a logic-compatible output signal. **Fig 3b** shows this circuit's typical waveforms. Trace A is a pulse associated with a light input signal. Trace B is IC_1's response, and trace C is IC_2's output signal. The phase shift between the photocurrent input signal and IC_2's output signal is due to IC_1's delay in reaching the threshold level. Reducing the threshold level will help reduce the shift but moves the circuit's operation closer to the noise floor. Additionally, the fixed threshold level cannot account for response changes in the emitter and detector diodes and the fiber-optic line over time and temperature. These response changes manifest as changes in the apparent amplitude of the signal.

Receiving high-speed fiber-optic data with such input amplitude variations is not easy, especially if the variation is wide. Unless the receiver is carefully designed, the high-speed data and uncertain intensity of the light level can cause erroneous results. **Fig 4a** addresses the previous circuit's fixed-threshold limitation and offers significant performance advantages. This receiver reliably conditions fiber-optic input signals as fast as 40 MHz. The peak-to-peak amplitude of input signal can vary by as much as 40 dB. The circuit's digital output stage has an adaptive threshold trigger that accommodates signal intensity variations due to component aging and other causes. The circuit has an analog output signal that you can use to monitor the detector's output.

The PIN photodiode detects the optical signal, which IC_1 then amplifies. A second stage, IC_2, further amplifies the signal. The output voltage of this second stage biases a 2-way peak detector (Q_1 through Q_4). Q_2's emitter capacitor stores the signal's maximum peak while



TRACE	VERTICAL SCALE
A	5V/DIV
B,C	2V/DIV

Fig 4—A self-adapting threshold *is the hallmark of this optical receiver* ***(a)****. Driven by a test signal* ***(b****, trace A), the circuit lets you monitor the detector's current (trace B) in addition to producing a final output (trace C).*

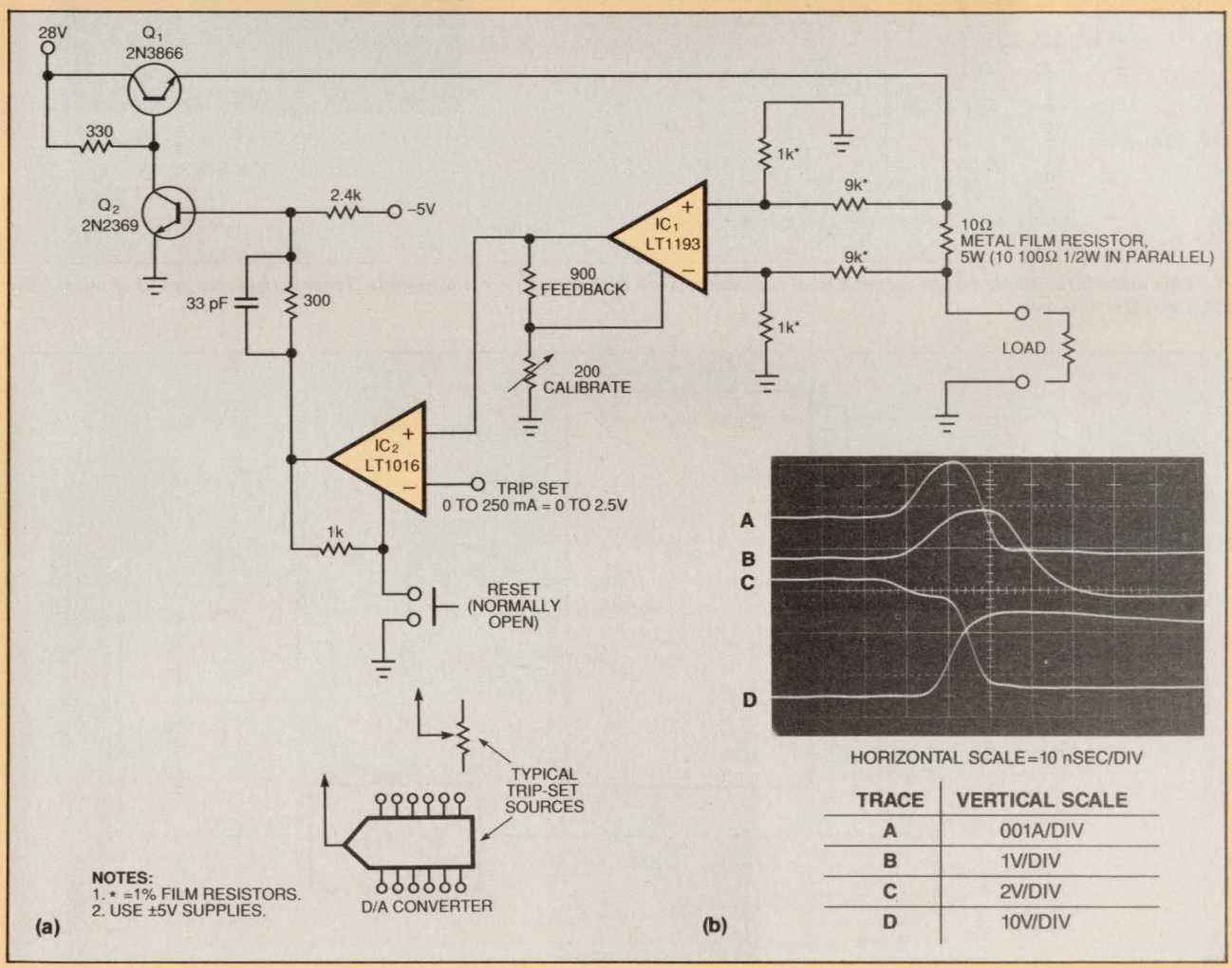
Protective circuit can save you a load

Some type of fuse or circuit breaker helps protect integrated circuits during developmental probing and expensive loads during trimming and calibration. **Fig Aa** shows a simple circuit that will turn off current in a load 18 nsec after that current exceeds a preset value. The circuit is especially versatile because one side of the load is grounded.

Under normal conditions, Q_1's emitter is biased on and supplying power to the load via the 10Ω current shunt. Differential amplifier IC_1's output signal resides below comparator IC_2's voltage-programmed trip point, and Q_2 is off.

When an overload occurs, Q_1's emitter current begins to increase (**Fig Ab,** trace A, just prior to the third vertical division). IC_1's output voltage (trace B) begins to rise as it tracks the increase in voltage across the 10Ω shunt. The 9-kΩ, 1-kΩ voltage dividers keep IC_1's input pins within their common-mode range. Q_1's emitter voltage (trace C) begins to drop as the transistor beta-limits. When IC_1's version of the load current exceeds IC_2's trip point, IC_2 goes high (trace D), which turns on Q_2. (Local positive feedback at IC_2's latch pin causes IC_2 to latch in this off state.) Q_2 steals Q_1's base drive, thus turning off the load current.

Once you've cleared the load fault, you can use the push button to reset the circuit. The delay from the onset of excessive load current to complete circuit shutdown is less than 18 nsec. (When interpreting the **Fig Ab** waveforms, note that trace A's current probe has a 4-nsec delay.) To calibrate the circuit, ground Q_2's base and install a 250-mA load. Adjust the 200Ω trim for a 2.5V output signal at IC_1. Next, remove the load, unground Q_2's base, and press the reset button. Finally, set the desired trip voltage, and the circuit is ready for use.



TRACE	VERTICAL SCALE
A	001A/DIV
B	1V/DIV
C	2V/DIV
D	10V/DIV

***Fig A—This circuit breaker (a) trips** in as little as 18 nsec. The circuit shuts down the load (**b,** trace C) when the load current (trace A) exceeds the trip point. Trace B represents IC_1's output voltage; trace D represents IC_2's output voltage.*

Q_4's emitter capacitor retains the minimum excursion. The dc value of the midpoint of IC_2's output signal appears at the junction of the 500-pF capacitor and the 22-MΩ resistors. This point will always be midway between the signal's excursions, regardless of the signal's absolute amplitude. The low-bias LT1097 op amp (IC_3) buffers this signal-adaptive voltage to set the trigger voltage at IC_4's positive input pin. IC_4's negative input pin is biased directly from IC_2's output.

Fig 4b shows the results of using the test circuit of **Fig 4a**. The pulse generator's output signal is trace A; IC_2's analog output voltage is trace B. IC_4's output signal is trace C. The waveforms were recorded using a 5-μA photocurrent at about 20 MHz as the test signal.

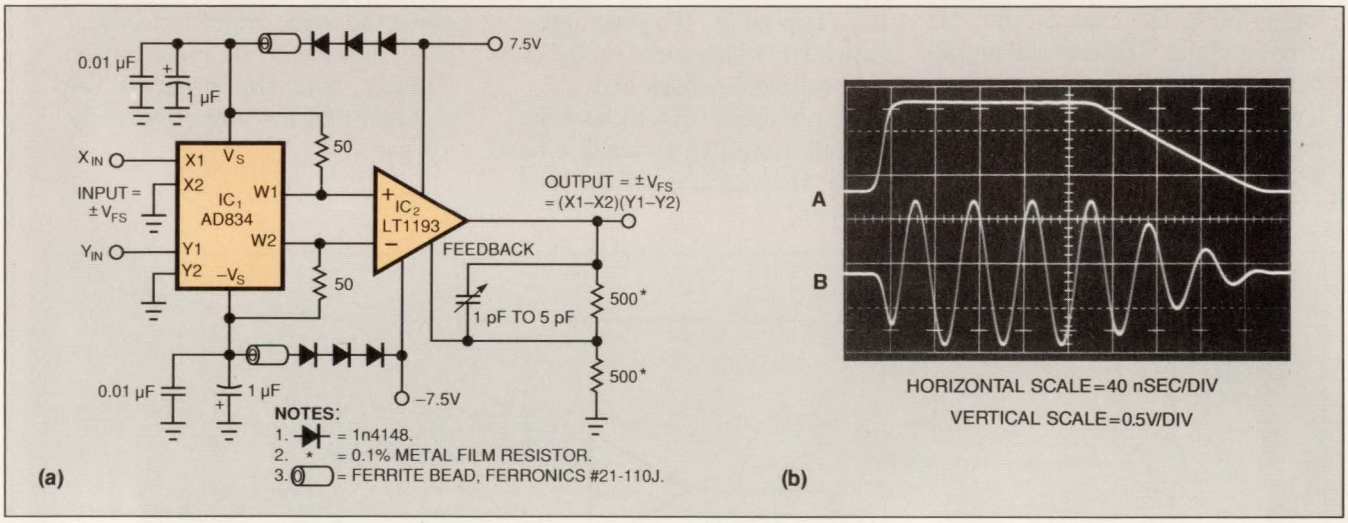


***Fig 5—This mixer's (a) single-ended output signal** is easier to work with than differential signals. Trace B **(b)** is the result of mixing trace A with a 20-MHz sine wave.*

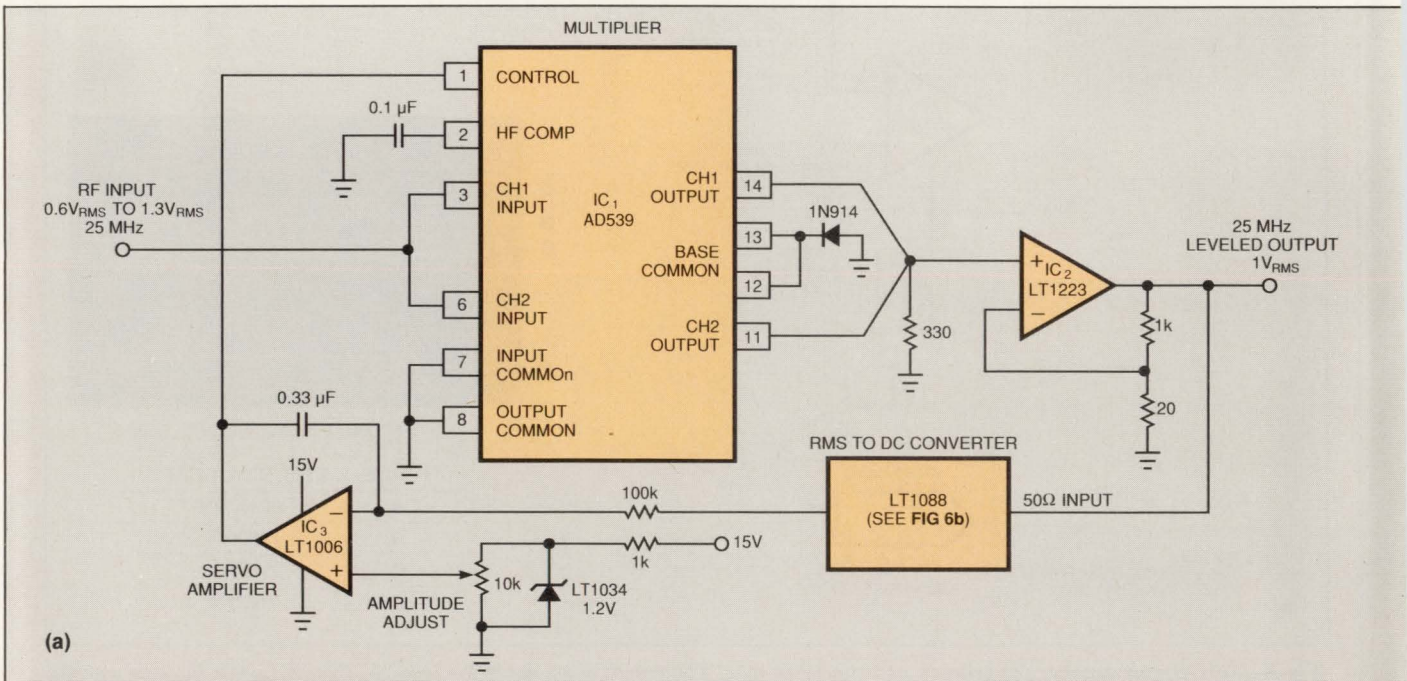


***Fig 6—A servo loop enables this circuit to stabilize** RF signals. The loop circuit **(a)** uses an rms-to-dc converter **(b)**.*

Note that IC_4's output transitions (trace C) correspond with the midpoint (plus IC_4's 10-nsec propagation delay) of IC_2's output signal (trace B), in accordance with the adaptive-trigger circuit's operation.

Mixer yields single-ended signal

Another common communications requirement, particularly for RF work, is mixing signals for modulation or heterodyning. Analog multipliers can mix signals, but they have a drawback; their output signals take a differential form. These differential signals, which have substantial common-mode content, are frequently inconvenient to work with. You can use RF transformers to convert them to single-ended signals, but you lose dc and low-frequency information in the process. **Fig 5a** illustrates a better approach. The circuit uses the LT1193 differential amplifier (IC_2) to accomplish the differential-to-single-ended transition. Set up IC_1 in the configuration **Ref 1** recommends. The LT1193 takes the differential signal from IC_1's 50Ω-terminated output lines and provides a single-ended output signal. The amplifier's gain of 2 yields an 11V output signal at full scale.

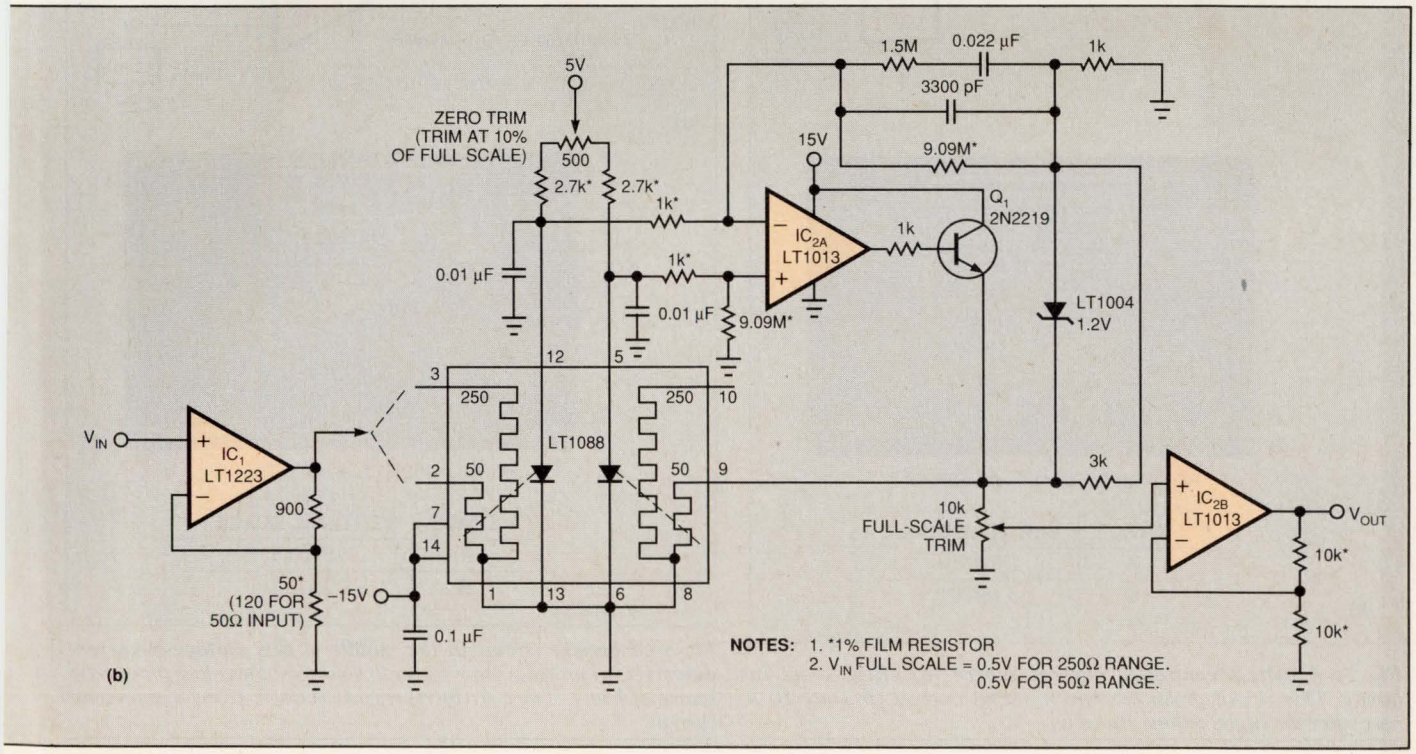
IC_1's output signals ride on a common-mode level quite close to the device's positive supply. This common-mode level falls outside IC_2's input common-mode range. The diodes in the 7.5V supply rails drop the supply voltage to IC_1, which biases IC_1's output signals within IC_2's input range. This scheme avoids the attenuation and matching problems you'd get if you placed a level shift between the multiplier and amplifier. The impedance of the ferrite beads combine with the diodes' impedance to ensure adequate bypassing for the multiplier.

This circuit's performance is quite impressive. Error remains within 2% over dc to 50 MHz, and feedthrough is less than −50 dB. Trimming the circuit involves adjusting the variable capacitor at the amplifier for minimal output square-wave peaking. **Fig 5b** shows the circuit's performance when multiplying a 20-MHz sine wave by trace A's waveform. The output signal (trace B) is a singularly clean instantaneous representation of the X and Y input products.

Often in RF communications you will want to stabilize the amplitude of a waveform against variations in

Acronyms used in this article

FET—Field-effect transistor
RF—Radio frequency
rms—Root mean square



input signal strength over time and temperature. Instruments and transmitters must often provide this function, which is not easy if the instruments must also maintain waveform purity. **Fig 6a** shows a circuit that stabilizes waveform amplitudes while maintaining waveform purity.

You apply the RF input signal to the AD539 wideband multiplier (IC_1), which drives IC_2. An LT1088-based rms-to-dc converter (**Fig 6b**) turns IC_2's output to dc. A servo amplifier (IC_3) compares that dc output signal with a settable dc reference and biases the multiplier's control channel, thus completing a loop. The 0.33-μF capacitor provides frequency compensation by rolling off gain at a frequency well below the response of the LT1088 servo amplifier. The loop maintains the output's 25-MHz rms amplitude at the dc reference's value; it rejects changes in load, input-signal strength, power-supply voltage, and other variables.

All of the previous circuits have a voltage-based output signal. Sometimes, however, you'll want your output in current form. **Fig 7a** shows a voltage-controlled current source that has both the load and control voltage referenced to ground. This simple, powerful circuit produces output current in accordance with the sign

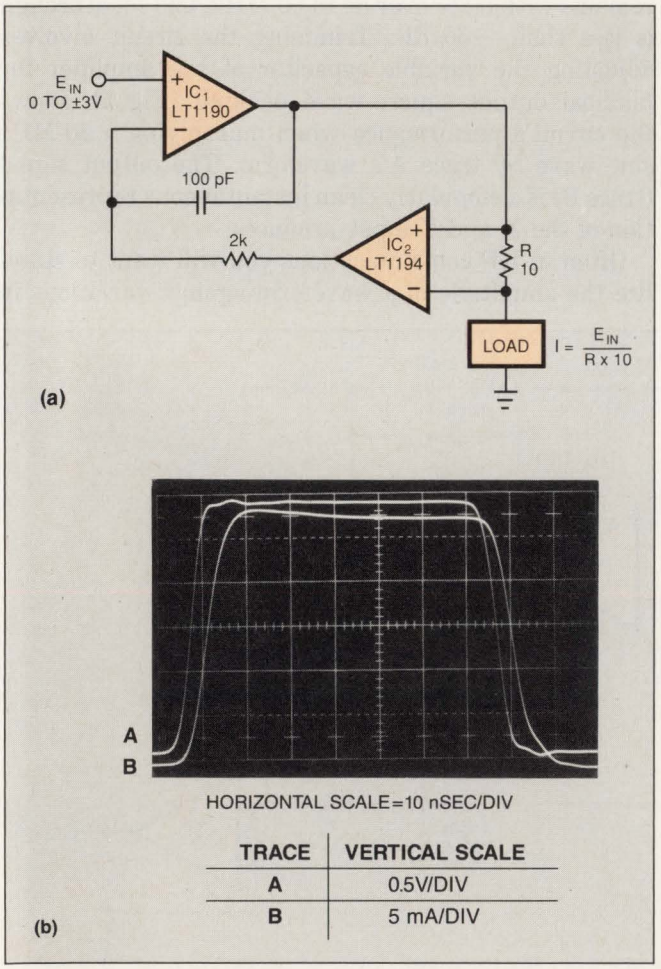


*Fig 7—**A voltage-controlled current source (a)** often comes in handy. This circuit produces a clean output current (**b**, trace B) 4 nsec after the input voltage (trace A).*

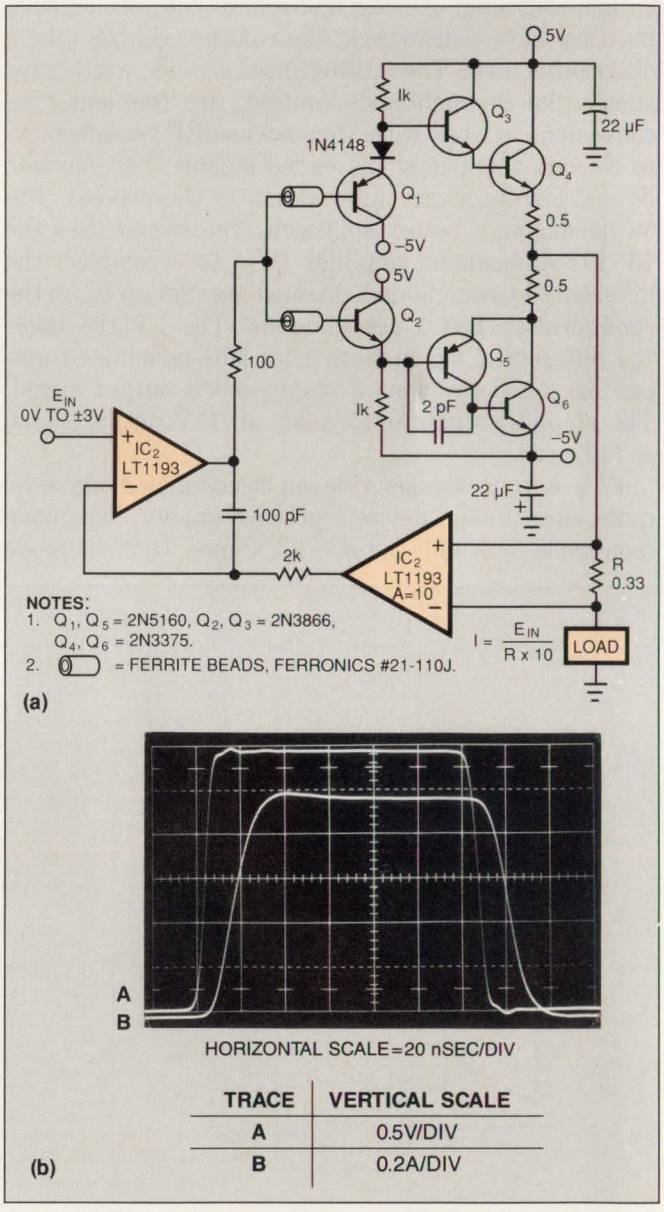


*Fig 8—**A booster circuit in the middle of this voltage-to-current converter (a)** provides more power to your load than does the current source of **Fig 7**. Trace A **(b)** represents voltage; trace B represents current.*

and magnitude of the control voltage. Resistor R sets the circuit's scale factor.

IC_1, biased by E_{IN}, drives current through R (in this case 10Ω) and the load. IC_2, sensing the differential voltage across R, closes a loop back to IC_1. The load current is constant because IC_1's loop forces a fixed voltage across R. The 2-kΩ, 100-pF combination sets roll-off, and the configuration is stable. **Fig 7b** shows the circuit's dynamic response. Trace A is the control input voltage, E_{IN}; trace B is the output current. The response has a delay of 5 nsec and no slew residue or aberrations.

Fig 8a is **Fig 7a**'s basic current source plus a 1A booster stage to increase output power. Including the booster inside IC_1's feedback loop eliminates the booster's dc errors. Note that the booster needs no current-limiting features because of the circuit's inherent current-limiting operation. **Fig 8b** shows that the circuit's response is as clean as that of the lower-power version, although its delay is about 20 nsec slower. The loop stability considerations involved in placing IC_2 and the booster in IC_1's feedback path are significant. This type of circuit receives detailed treatment in **Ref 2.** EDN

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Author's biography

For more information on this article's author, turn to pg 163 in the October 10, 1991 issue.

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