88F3710 and 88F3720

ARMADA® 3700 Family

Single/Dual CPU System-on-Chip

Hardware Specifications

Doc. No. MV-S110707-U0, Rev. B
September 4, 2019

Document Conventions

	**Note:** Provides related information or information of special importance.
	**Caution:** Indicates potential damage to hardware or software, or loss of data.
	**Warning:** Indicates a risk of personal injury.

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PRODUCT OVERVIEW

The Marvell® ARMADA® 3700 Family of devices delivers comprehensive System-on-Chip (SoC) solutions powered by the dual Cortex-A53 ARMv8 high-performance CPU technology.

The ARMADA® 3700 Family includes:

- 88F3710: Single core CPU
- 88F3720: Dual core CPU

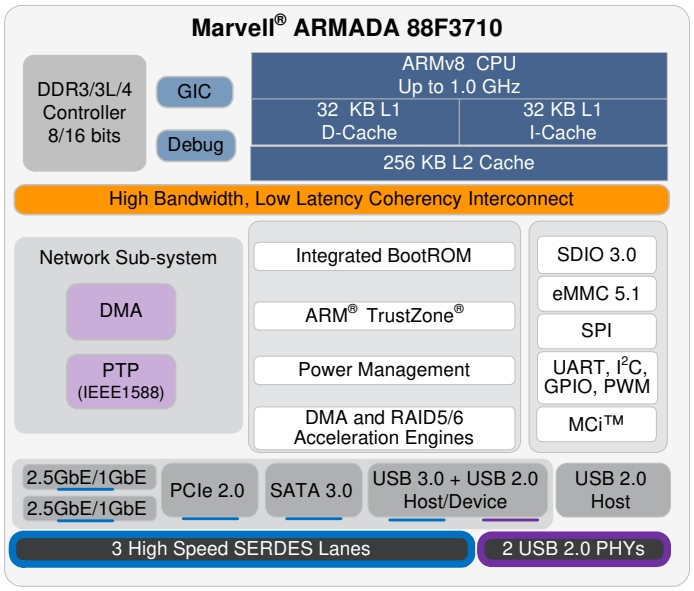
The devices incorporate rich and diversified high-speed I/Os, such as USB 3.0, SATA 3.0, PCI-Express 2.0, and 2.5 GbE (NBASE-T). In addition, the devices incorporate a wide set of security and data acceleration engines suitable for innovative networking, storage, and compute applications.

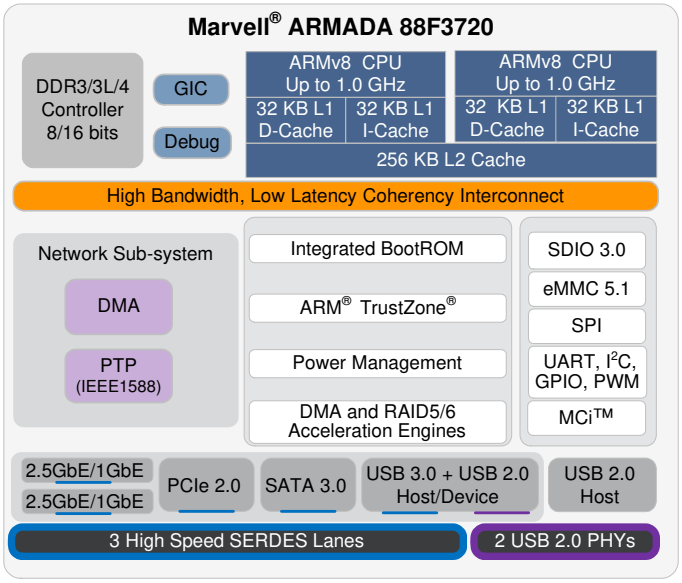
The ARMADA® 3700 Family innovative and unique architecture delivers unprecedented performance-to-power and performance-to-cost index in the embedded market.

TARGET APPLICATIONS

- Enterprise AP routers/repeaters for 802.11ac/n
- Consumer Network-Attached-Storage (NAS)
- Storage Ethernet-Drive (E-Drive)
- Multi-protocol IoT gateways
- Industrial, Factory and Building automation
- Smart energy
- Management Processor

BLOCK DIAGRAM





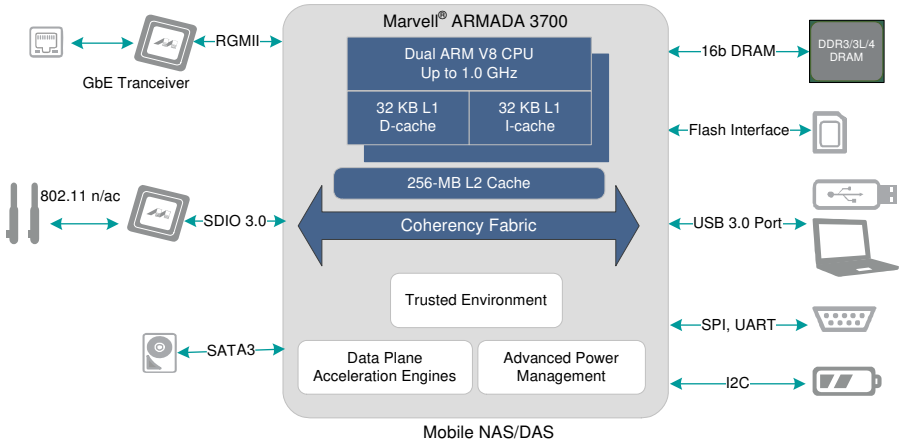
KEY FEATURES

- CPU
  - Single/Dual core ARMv8 Cortex-A53 CPU
  - CPU core operating speed of up to 1.0 GHz
  - 32 KB-Instruction / Data (4-way) set associative L1 cache with Parity/ECC protection
- Coherent Interconnect
  - High-bandwidth, low-latency IO Cache Coherency
- Memory Interface
  - High-speed 8/16-bit DDR3/3L/DDR4 DRAM memory controller
- Security
  - Hardware compliance with ARM Trustzone® architecture for DRM
- Networking Interface
  - 2 x Gigabit Ethernet 1Gbps / 2.5Gbps
  - SGMII / HS-SGMII / RGMII
  - Compatible with Marvell NBASE-T Transceivers
- USB
  - USB 3.0 Host/Device compatible with xHCI v1.0
  - USB 2.0 Host
- PCI Express (PCIe) 2.0 (RC or EP)
- SATA 3.0
- DMA, 2 x high-bandwidth DMA/XOR/CRC channels
- Flash and Peripheral I/Os, including 2 x SDIO 3.0, SPI, UART, GPIOs
- Power Management
  - Adaptive Voltage and Frequency Scaling
  - Integrated power switches for dynamic shut-down of CPU cores and unused functions
- Package and Thermals
  - 271B TFBGA 10.5 x 11.5 mm with 0.5 mm ball pitch green-compliant package
  - 28 nm low-power process
- Software and Ecosystem:
  - Complete SDK including U-Boot, Mainline Linux BSP
  - OpenWrt, Yocto Support
  - KVM and Containers support

APPLICATIONS

MOBILE (NAS/DAS)

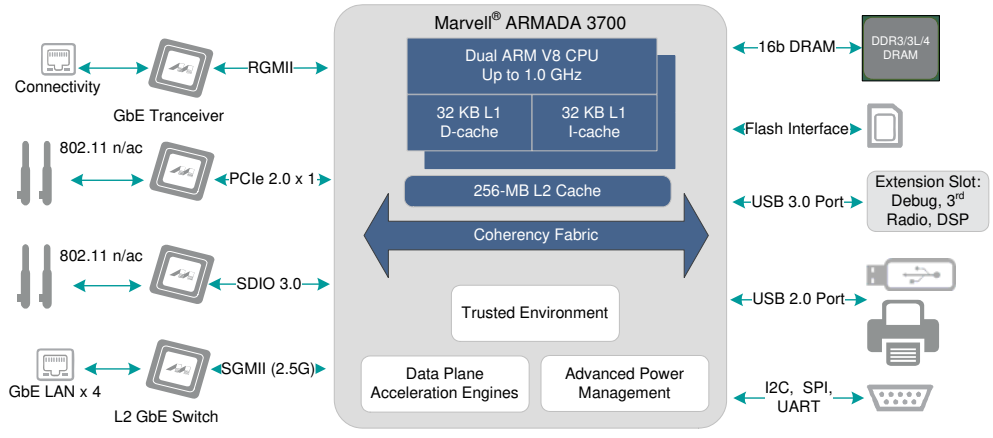
The ARMADA® 3700 Family low-power, high-performance architecture enables a new set of applications, such as battery supplied, mobile NAS and DAS all in one appliance. For example, when directly attached to a USB host, the device can operate on the USB source power and function as an external mass-storage device (DAS). When the device is battery operated, it serves as a wireless Access-Point (AP) capable of streaming media content from the attached storage device over the air. When an Ethernet connection is available, the device provides NAS services over the air or through the Ethernet ports.



Mobile NAS/DAS

RETAIL WIRELESS ROUTER

Connected to the Marvell industry-leading wireless and wired networking solutions, the ARMADA® 3700 Family is perfectly suited for dual-band 802.11 Retail Gateway or SOHO Access Point applications. The high-performance processors and hardware data-plane acceleration functions deliver the right balance between the performance, power, and price for wireless applications.



Retail Wireless Router

Revision History

Revision	Date	Description
Rev. A	13-Nov-17	Initial Release
Rev. B	4-Sep-19	Update Release
1. Updated Section 2.2.2, Adaptive Voltage Scaling (AVS) Interface, to add the following note to pin AVS_VDDFB: **NOTE:** If AVS is not applied, the maximum CPU frequency is limited to 600 MHz.		
2. Updated Table 74, MMC High-Speed Host (HS400) AC Timing Table, to add timing relative to Data Strobe.		
3. Updated Section 2.2.20, Miscellaneous Signals, pin type for RESET_N from CMOS to OD.		

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Preface

About This Document

This document provides the hardware specifications for the Marvell® ARMADA® 3700 Family devices. The hardware specifications include detailed pin information, configuration settings, electrical characteristics, and physical specifications.

This document is intended to be the basic source of information for designers of new systems.

Relevant Devices

- 88F3710
- 88F3720

In this document, the 88F3710/88F3720 devices are often referred to as the “device”.

Related Documents

The following documents contain additional information related to the 88F3710/88F3720. For the latest documentation revisions, contact a Marvell representative or see the Marvell Extranet website.

Title	Document Number
88F3710/88F3720 Marvell® ARMADA® 3700 Family *Hardware Design Guide*	MV-S302527-00
Marvell® ARMADA® 3700 Family *Functional Specifications*	MV-S110895-00
External standards	
ARM Architecture Reference Manual, Second Edition	ARM DDI 0500F
ARM Cortex-M3 Technical Reference Manual	ARM DDI 0337G
ARM Embedded Trace Macrocell Architecture Specification, ETMv4	ARM IHI 0064
Cortex-A53 Technical Reference Manual	
Corelink™ Level 2 Cache Controller L2C-310 Technical Reference Manual	
CoreSight Components Technical Reference Manual (ARM DDI 0314F)	
USB-HS High-Speed Controller Core Reference	
CoreSight Components Technical Reference Manual (ARM DDI 0314F)	

Document Conventions

Signal Range	A signal name followed by a range enclosed in brackets represents a range of logically related signals. The first number in the range indicates the most significant bit (MSb) and the last number indicates the least significant bit (LSb). Example: DB_Addr[12:0]
Active Low Signals #	An n letter at the end of a signal name indicates that the signal's active state occurs when voltage is low. Example: INTn
State Names	State names are indicated in *italic* font. Example: *linkfail*
Register Naming Conventions	Register field names may be indicated by angle brackets. Example: <RegInit> Register field bits are enclosed in brackets. Example: Field [1:0] Register addresses are represented in hexadecimal format. Example: 0x0 Reserved: The contents of the register are reserved for internal use only or for future use. A lowercase <n> in angle brackets in a register indicates that there are multiple registers with this name. Example: Multicast Configuration Register<n>
Reset Values	Reset values have the following meanings: 0 = Bit clear 1 = Bit set
Abbreviations	Kb: kilobit KB: kilobyte Mb: megabit MB: megabyte Gb: gigabit GB: gigabyte
Numbering Conventions	Unless otherwise indicated, all numbers in this document are decimal (base 10). An 0x prefix indicates a hexadecimal number. An 0b prefix indicates a binary number.

1 Detailed Features List

CPU

The Cortex™-A53 dual-core supports the following features:

- ARMv8 single/dual-core architecture with support for AArch64 and AArch32 Execution states at Exception levels EL0-EL3
- ARMv8 advanced SIMD and floating-point extensions (NEON)
- ARMv8 cryptographic extensions
- Trustzone security extension
- ARMv8 debug
- ETMv4 instruction trace
- GICv5 CPU Interface
- 32 KB L1 instruction and data caches
- L1 instruction cache parity protection, L1 data cache ECC protection
- 256 KB unified L2 cache with ECC protection
- L2 subsystem with snoop coherency unit
- 256 KB 16-way associative L2 cache with coherency
- MESI cache coherence
- ARMVv8 compliant VMSAv7 MMU
- 10-entry fully associative µITLB and µDTLB
- 512-entry 4-way SA unified main TLB
- AMBA 4 ACE bus interface
- AXI Coherency Extensions (ACE)
- SMP and cache coherency

The CPU subsystem includes the following features:

- Programmable Window AXI fabric running at half CPU speed
- ARMv8 debug via DAP Coresight™ to allow JTAG Interface
- Trace Support via Program Trace Macrocell (PTM)
- PMU for ARMv8 compliant performance monitors

SDRAM Controller

- 128-bit internal bus
- Supports DDR3, DDR3L, and DDR4 with up to 800 MHz SDRAM clock
- Runs on SDRAM clock asynchronous to the CPU clock
- Out-of-order request completion with coherent write buffer
- Up to 2 SDRAM ranks (chip selects)
- Supports x8 and x16 memory devices

Gigabit Ethernet (GbE) Ports

- 2 GbE ports (0 and 1)
- 2 x SGMII at 1 Gbps or 2.5 Gbps
- 1 x RGMII or 1 x MII at 10/100/1000 Mbps
- Serial Management Interface (SMI)
- Full-wire speed receive and transmit of short packets
- Support for IEEE 1588v2 (PTP)
- DA filtering
- Priority queuing on receive based on DA, VLAN tag, IP-TOS
- Strict priority/WRR arbitration between 8 transmit queues with rate limiting
- Per queue egress rate shaping
- Support for queuing based on Marvell DSA tag
- Support for jumbo frames (up to 10K) on both receive and transmit
- TCP/IP acceleration
- Support for IEEE 802.3az (Energy-Efficient Ethernet)
- Support for Wake-On-LAN (WOL), with an option to use an external clock and turn off the internal PLL
- TCP Segmentation Off Load

PCI Express (PCIe) Interface

- PCIe Gen 1 at 2.5 Gbps, Gen 2.0 at 5 Gbps
- Supports Root Complex and Endpoint modes
- 64-bit PCIe address and system address space for outbound transactions
- Support for outbound read and write transactions up to 512 bytes, and for inbound read and write transactions with payloads up to 512 bytes
- Maximum read request size of 4 KB
- Dual mode (Root Complex and Endpoint) operation
- Support for outbound configuration read and write transactions
- Support for MSI and MSI-X
- Support for legacy interrupts
- Programmable I/O mode for outbound 32-bit I/O, configuration and memory read and write transactions
- Support for unaligned AXI transfers
- One physical function (no VFs)
- Support for ECRC checking and generation
- Support for Latency Tolerance Reporting

USB Controllers

- 1 USB 3.0 Host or Device controller with PHYs

  Includes a USB 3.0 PHY and a USB 2.0 PHY. The USB 2.0 PHY supports VBUS, ID, and charger detection circuit.
- As a Host
  - Extensible Host Controller interface (xHCI) compatible
  - Supports direct connection to all device types (SS, HS, FS, LS)
  - Maximum number of device slots is 4
  - Maximum number of endpoints is 16
- As a Device
  - Supports 2 IN endpoints and 2 OUT endpoints plus a control endpoint (EP0) (a total of 5 independent endpoints) for both USB3.0 and USB2.0.
  - Supports SuperSpeed (SS), High Speed (HS), Full Speed (FS), and Low Speed (LS) features
- 1 USB 2.0 Host controller with PHY

NOTE:

An endpoint is a uniquely addressable portion of a USB device that is the source or sink in an information flow between the USB host and device.

An IN endpoint is a source through which the device sends data to the host, and an OUT endpoint is a sink through which the device receives data from the host.

Every USB device must provide at least one control endpoint at address 0, called the default endpoint or Endpoint0. This endpoint is bi-directional. This means the host can send data to the endpoint and receive data from it within one transfer. One of the main uses of control transfers is for device enumeration when the device is attached to the host. Other purposes of a control transfer are to enable the host to obtain device information, configure the device, or perform control operations that are unique to the device.

88F3700 is configured to have 2 IN and 2 OUT endpoints in order to support UASP (USB Attached SCSI Protocol) for mass storage applications.

SATA 3.0 AHCI Host Controller

- One SATA port compliant with Serial ATA Specification 3.0
- Supports communication speeds of 1.5 Gbps, 3.0 Gbps, and 6.0 Gbps
- Supports Gen 1x, Gen 2x, and Gen 3
- Supports programmable transmitter signal levels
- Supports Native Command Queuing (NCQ) and First Party DMA (FPDMA)
  - In-order data delivery
  - 32 outstanding commands
- Supports vendor-unique commands
- Supports AHCI 1.0 programming interface
- Supports Partial and Slumber power management states
- Supports an internal 8 KB buffer for SATA Data FIS

Internet Security

- IPsec
  - IPsec ESP and AH Packet Transform
  - Support for latest Ipsec RFCs (3566, 430x, 4434, 4543, 4868)
  - Extended Sequence Number Support
  - Replay protection
  - Full header and trailer processing
  - IPv4/IPv6 support (RFC-4301) and header updates
- MACsec
  - Header insertion and removal
  - Integrity only and integrity and confidentiality modes
  - Confidentiality offset
- SSL/TLS/DTLS
  - SSL 3.0, (Secure Sockets Layer, App Layer), TLS and DTLS, (Layer 4), transform (RFC-4346, 4347)
  - Full header processing

DMA Engine

- 2-channel general purpose DMA controller
- Memory copy (DMA) acceleration for the following transfers:
  - DDR to DDR
  - DDR to SPI with write threshold of 8, 16, or 32 bytes
  - SPI to DDR with read threshold of 8, 16, or 32 bytes
  - DDR to UART2 with write threshold of 8, 16, or 32 bytes
  - UART2 to DDR with read threshold of 8, 16, or 32 bytes
  - DDR to PCIe
  - PCIe to DDR
- Memory initialization function
- iSCSI CRC32 calculation mode
- Memory ECC error cleanup mode

SPI Port

- SPI with single, dual and quad mode, and up to 4 chip selects
- Supports external SPI flash memory of up to 80 MHz

SD / SDIO / MMC

- 1 x SDIO 3.0 Host Controller
  - 1-bit or 4-bit
  - Supports the following specifications:
    - SD Physical Layer Spec 3.01
    - SDIO Spec 3.0
    - SD Host Controller Spec 3.0
- 1 x SDIO 3.0 and eMMC 5.0 Host Controller
  - 1-bit, 4-bit, or 8-bit
  - Supports the following specifications:
    - SD Physical Layer Spec 3.01
    - SDIO Spec 3.0
    - SD Host Controller Spec 3.0
    - JEDEC MMC/eMMC Spec 4.41 (sequential commands are not supported)
    - JEDEC eMMC 5.0 (sequential commands are not supported)
    - JEDEC eMMC 5.1 Command Queuing Interface

UART Interfaces

- UART 1 Interface
  - 1-byte internal transfer size
  - 32-byte Tx FIFO
  - 64-byte Rx FIFO
  - Baud rate generator supports fractional divisor
- UART 2 Interface
  - 4-byte or 1-byte internal transfer size
  - 128-byte Tx FIFO
  - 128-byte Rx FIFO
  - Baud rate generator supports fractional divisor
  - Supports RTS and CTS control
  - Supports transfer count for RX/TX, with transfer finish status and RTS signal control

Advanced Power Management

- CPU Idle based on WFI
- CPU frequency step down function
- Dynamic frequency and adaptive voltage scaling (AVS)
  - PMIC interface through AVS, GPIO or I2C
- SOC level power management with the following options:
  - Internal VDD-off options for two power islands
  - SDRAM auto-refresh
  - Global clock gating, with free-running option for SOC timers
  - PLL and OSC disable modes
  - Internal SRAM and I/O leakage control
  - Interface to PMIC using either AVS, GPIO, or I2C for fast VDD control
  - Wake-up from any external event, interrupt, and internal timer
- Support for A53 CPU power-off during USB-SATA Bridge mode.

I^2C Interfaces

- 2 x I^2C TWSI bus interface units for sensors, real-time clock (RTC), and DC-DC
- Compliance with the *TWSI Bus Specification Version 2.1* with the exception of support for 10-bit slave addressing, CBUS compatibility, and the hardware general call
- Multi-master and arbitration support
- Standard mode operation up to 100 KHz
- Fast mode operation up to 400 KHz
- Fast-mode plus (Fm+) operation up to 1 MHz
- High-speed mode (HS mode) operation up to 3.4 MHz

1-Wire Serial Interface

- 1-Wire bus master interface controller for battery, sensors, and RTC
- SDI mode to transmit up to 128 bits at a desired clock frequency
- Control of the 1-Wire bus through 8-bit commands
- Registers for command loading, reading and writing data, and interrupt control

Integrated BootROM

- 25 MHz or 40 MHz crystal mode
- Download boot loader or program code from any of the following:
  - SPI flash (NOR flash, serial NAND)
  - eMMC memory
  - SATA AHCI interface
  - UART interface

Multi-Purpose Pins (MPP)

- North Bridge MPP1[19:0] (GPIO1) pins with maskable interrupts and programmable polarity
- South Bridge MPP2[23:0] (GPIO2) pins with maskable interrupts and programmable polarity

Clock Generation	■ Internal generation of CPU clock, core clock, SDRAM clock, RGMII/MII clock, and external reference clock from a single 25 MHz or 40 MHz reference clock ■ Supports internal generation of spread-spectrum clocking on all internal clocks
Interrupts	ARM compliant Generic Interrupt Controller (GIC500)
Timers/Counters and Watchdog Timers	Integrated programmable 64-bit timers/counters and watchdog timers
LED Drivers and PWM	4 open drain LED pads with PWM functionality
Peripheral eFuse OTP Memory	■ 69 bits in North Bridge for manufacturing purposes ■ 97 bits in South Bridge for manufacturing purposes
Package	271B-ball TFBGA 11.5 x10.5 mm, 0.5mm ball pitch package

2 Pin Information

This section provides the pin logic diagram for the 88F3710/88F3720 devices and a detailed description of the pin assignments and their functionality.

2.1 Pin Logic

Figure 1: 88F3710/88F3720 Pin Logic Diagram (Top)

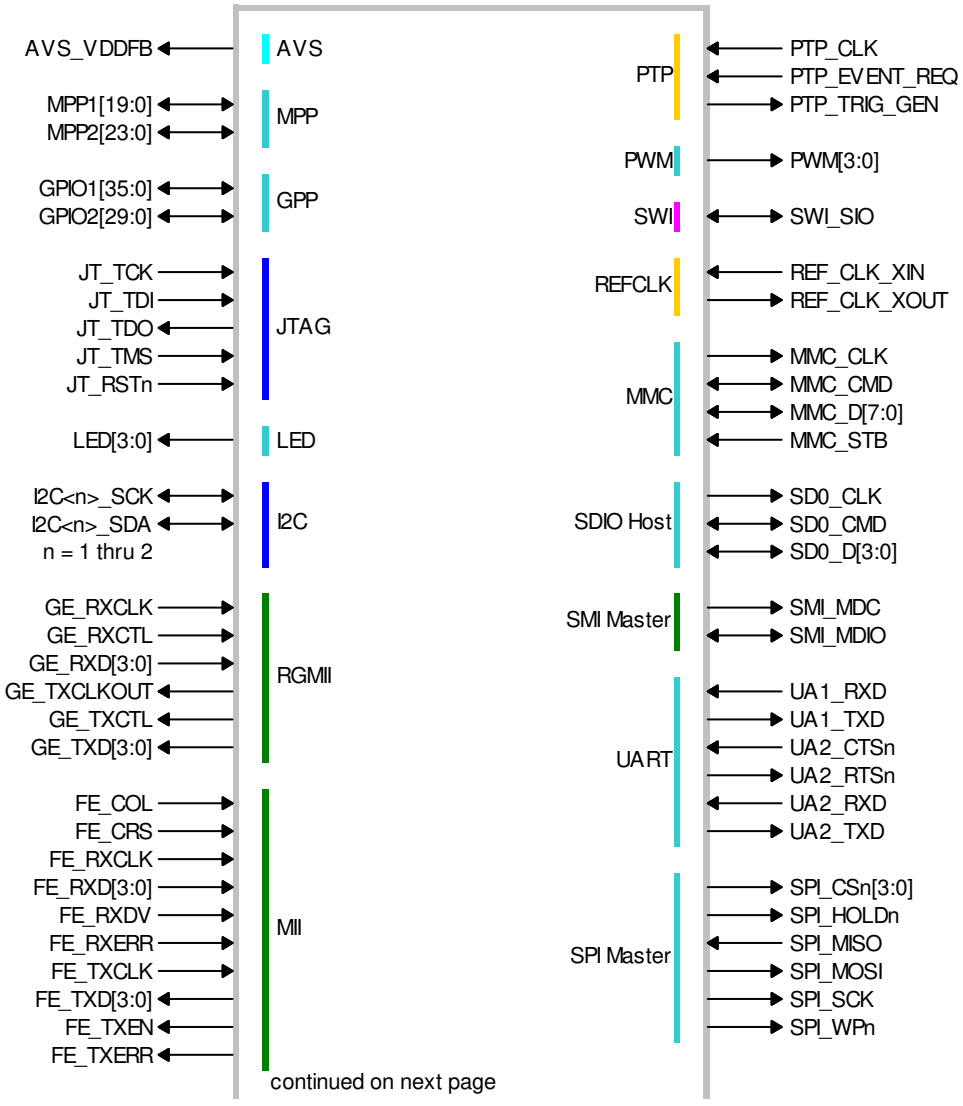
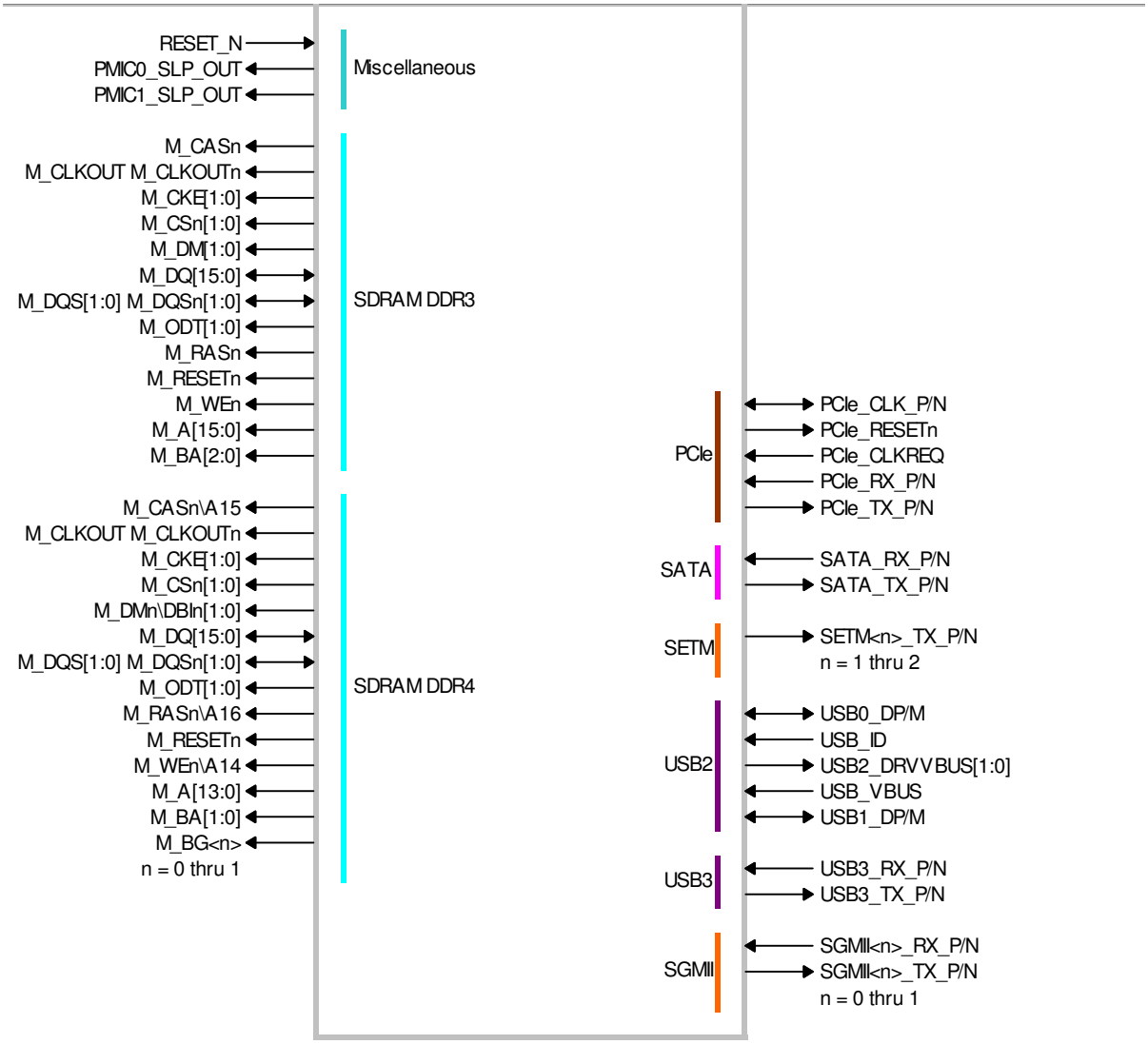


Figure 2: 88F3710/88F3720 Pin Logic Diagram (Continued)



2.2 Pin Descriptions

This section details all the pins for the different interfaces providing a functional description of each pin and pin attributes.

Note

For a description of the unused pins, refer to Section 3, Unused Interface Strapping, on page 58.

Table 1 defines the abbreviations and acronyms used in the pin description tables.

Table 1: Pin Functions and Assignments Table Key

Term	Definition
<n>	Represents port number when there are more than one ports
Analog	Analog Driver/Receiver or Power Supply
Calib	Calibration pad type
CML	Current Mode Logic
CMOS	Complementary Metal-Oxide-Semiconductor
DDR	Double Data Rate
GND	Ground Supply
HCSL	High-speed Current Steering Logic
I	Input
I/O	Input/Output
O	Output
OD	Open Drain pin The pin allows multiple drivers simultaneously (wire-OR connection). A pull-up is required to sustain the inactive value.
POD	Pseudo Open Drain
Power	Power Supply
SDR	Single Data Rate
SSTL	Stub Series Terminated Logic
XXXn	n - Suffix represents an Active Low Signal

2.2.1 Power Pins

Table 2: Power Pins Pin Description

Pin Name	Pin Type	Description
VDD	Power	Core and CPU voltage.
MCI_AVDD12	Analog Power	MoChi MCi Interconnect PHY 1.2V quiet power supply. **NOTE:** See the Design Guide for power supply filtering recommendations.
MCI_AVDD12D	Analog Power	MoChi MCi Interconnect PHY 1.2V digital quiet power supply. **NOTE:** See the Design Guide for power supply filtering recommendations.
PLL_AVDD18	Analog Power	PLL 1.8V quiet power supply. **NOTE:** See the Design Guide for power supply filtering recommendations.
SRD1_AVDD18	Analog Power	SATA and SETM PHYs 1.8V quiet power supply. Also used by USB3 interface when the USB3 is connected **NOTE:** See the Design Guide for power supply filtering recommendations.
SRD2_AVDD18	Analog Power	Crystal, SGMII, PCIe and USB 3.0 PHYs 1.8V quiet power supply. **NOTE:** See the Design Guide for power supply filtering recommendations.
USB_AVDD33	Analog Power	USB 2.0 PHY 3.3V quiet power supply. **NOTE:** See the Design Guide for power supply filtering recommendations.
USB_AVDD18	Analog Power	USB 2.0 PHY 1.8V quiet power supply. **NOTE:** See the Design Guide for power supply filtering recommendations.
VDDO_M	Power	I/O supply voltage for the SDRAM interface.
VDDO_MMC	Power	I/O supply voltage for the eMMC/SDIO1 interface. **NOTE:** For more details on the MPP multiplexing options, see Section 5.1, GPIO and DDR Pin Multiplexing, on page 61.
VDDO_GIO	Power	I/O supply voltage for the Ethernet interface. **NOTE:** For more details on the MPP multiplexing options, see Section 5.1, GPIO and DDR Pin Multiplexing, on page 61.
VDDO_JIO	Power	I/O supply voltage for the JTAG and UART interfaces. **NOTE:** For more details on the MPP multiplexing options, see Section 5.1, GPIO and DDR Pin Multiplexing, on page 61.
VDDO_PIO	Power	I/O supply voltage for the I2C, PWM, LED, SPI, UART2 interfaces. **NOTE:** For more details on the MPP multiplexing options, see Section 5.1, GPIO and DDR Pin Multiplexing, on page 61.
VSS	Ground	Main Ground
VDDIO_SD	Power	I/O supply voltage for the SDIO/eMMC interface. **NOTE:** For more details on the MPP multiplexing options, see Section 5.1, GPIO and DDR Pin Multiplexing, on page 61.

2.2.2 Adaptive Voltage Scaling (AVS) Interface

AVS external interface to Power Management unit on board

Table 3: Adaptive Voltage Scaling (AVS) Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
AVS_VDDFB	O	Analog	PLL_AVDD18	AVS Feedback Signal. Feedback to the external power regulator to adjust the voltage level. **NOTE:** When acting in slave mode as SLAVE_VOLTAGE_UP_OUT, this pin becomes Output CMOS type. **NOTE:** If AVS is not applied, the maximum CPU frequency is limited to 600 MHz.

2.2.3 Multi Purpose Pins (MPP)

When not in use, program interface to GPIOs and set GPIOs as output.

Table 4: Multi Purpose Pins (MPP) Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
MPP1[19:0]	I/O	CMOS	VDDO_PIO	Multi Purpose Pins (MPP) Refer to Section 5.1, GPIO and DDR Pin Multiplexing, on page 61, for additional information for available functionalities.
MPP2[23:0]	I/O	CMOS	VDDO_GIO	Multi Purpose Pins (MPP) Refer to Section 5.1, GPIO and DDR Pin Multiplexing, on page 61, for additional information for available functionalities.

2.2.4 General Purpose Pins (GPP)

Each individual pin can be defined as an input, output, or edge-sensitive interrupt input.

These pins can be used for indications retrieval or for peripherals control.

When not in use, set GPIOs as output.

Note

These pins are implemented on the Multi-Purpose Pin interface.

Table 5: General Purpose Pins (GPP) Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
GPIO1[19:0]	I/O	CMOS	VDDO_PIO	General Purpose Pin(s)
GPIO1[26:20]	I/O	CMOS	VDDO_JIO	General Purpose Pin(s)
GPIO1[35:27]	I/O	CMOS	VDDO_MMC	General Purpose Pin(s)
GPIO2[23:0]	I/O	CMOS	VDDO_GIO	General Purpose Pin(s)
GPIO2[29:24]	I/O	CMOS	VDDIO_SD	General Purpose Pin(s)

2.2.5 JTAG Interface

The device supports a JTAG interface and is compliant with the IEEE 1149.1 standard.

It supports mandatory and optional boundary scan instructions.

Note These pins are implemented on the Multi-Purpose Pin interface.

Table 6: JTAG Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
JT_TCK	I	CMOS	VDDO_JIO	JTAG Test Clock JT_TDI, JT_TDO, JT_TMS are referenced to this clock. **NOTE:** When unused, can be pulled down.
JT_TDI	I	CMOS SDR	VDDO_JIO	JTAG Test Data Input Sampled on JT_TCK rising edge. **NOTE:** When unused, can be pulled up to a power rail.
JT_TDO	O	CMOS SDR	VDDO_JIO	JTAG Test Data Output Driven on JT_TCK falling edge. **NOTE:** When unused, can be left unconnected.
JT_TMS	I	CMOS SDR	VDDO_JIO	JTAG Test Mode Select Sampled on JT_TCK rising edge. TMS signal for CORE. **NOTE:** When unused, can be pulled up to a power rail.
JT_RSTn	I	CMOS	VDDO_JIO	JTAG Test Asynchronous Reset **NOTE:** This pin can be pulled down to GND.

2.2.6 LED Display Interface

Table 7: LED Display Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
LED[3:0]	O	OD	VDDO_PIO	LED Output Display signals

2.2.7 Inter-Integrated Circuit (I2C) Interface

I2C and Two-Wire Serial Interface (TWSI) both refer to the same interface. Either name can be used in this document.

Note These pins are implemented on the Multi-Purpose Pin interface.

Table 8: Inter-Integrated Circuit (I2C) Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
Where <n> represents numbers 1 thru 2				
I2C<n>_SCK	I/O	CMOS	VDDO_PIO	I2C Serial Clock Serves as output when acting as an I2C master. Serves as input when acting as an I2C slave. **NOTE:** Must be pulled up to a power rail.
I2C<n>_SDA	I/O	CMOS SDR	VDDO_PIO	I2C Serial Data/Address Address or write data driven by the I2C master or read response data driven by the I2C slave. **NOTE:** Must be pulled up to a power rail.

2.2.8 Reduced Gigabit Media Independent Interface (RGMII)

Note These pins are implemented on the Multi-Purpose Pin interface.

Table 9: Reduced Gigabit Media Independent Interface (RGMII) Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
GE_RXCLK	I	CMOS	VDDO_GIO	RGMII Receive Clock Receives 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, and 2.5 MHz for 10 Mbps. All RGMII input pins are referenced to GE_RXCLK.
GE_RXCTL	I	CMOS DDR	VDDO_GIO	RGMII Receive Control A logical derivative of receive data valid (RXDV) on GE_ RXCLK rising edge, and data error (RXERR) on GE_ RXCLK falling edge.
GE_RXD[3:0]	I	CMOS DDR	VDDO_GIO	RGMII Receive Data Contains the receive data nibble inputs that run at double data rate. Bits [3:0] are presented on the rising edge of GE_RXCLK, and bits [7:4] are presented on the falling edge of GE_ RXCLK.
GE_TXCLKOUT	O	CMOS	VDDO_GIO	RGMII Transmit Clock Provides 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, and 2.5 MHz for 10 Mbps. All RGMII output pins are referenced to GE_TXCLKOUT.
GE_TXCTL	O	CMOS DDR	VDDO_GIO	RGMII Transmit Control A logical derivative of transmit data enable (TXEN) on GE_TXCLKOUT rising edge, and data error (TXERR) on GE_TXCLKOUT falling edge.
GE_TXD[3:0]	O	CMOS DDR	VDDO_GIO	RGMII Transmit Data Contains the transmit data nibble outputs that run at double data rate. Bits [3:0] are presented on the rising edge of GE_ TXCLKOUT, and bits [7:4] are presented on the falling edge of GE_TXCLKOUT.

2.2.9 Media Independent Interface (MII)

Note These pins are implemented on the Multi-Purpose Pin interface.

Table 10: Media Independent Interface (MII) Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
FE_COL	I	CMOS	VDDO_GIO	MII Collision Indication This signal is relevant for half-duplex mode only. This signal is asynchronous.
FE_CRS	I	CMOS	VDDO_GIO	MII Carrier Sense Indication This signal is relevant for half-duplex mode only. This signal is asynchronous.
FE_RXCLK	I	CMOS	VDDO_GIO	MII Receive Clock FE_RXD[3:0], FE_RXDV, and FE_RXERR pins are referenced to FE_RXCLK.
FE_RXD[3:0]	I	CMOS SDR	VDDO_GIO	MII Receive Data This bus is referenced to FE_RXCLK.
FE_RXDV	I	CMOS SDR	VDDO_GIO	MII Receive Data Valid This pin is referenced to FE_RXCLK.
FE_RXERR	I	CMOS SDR	VDDO_GIO	MII Receive Error This pin is referenced to FE_RXCLK.
FE_TXCLK	I	CMOS	VDDO_GIO	MII Transmit Reference Clock This clock is provided by an external PHY device connected to the MAC. All MII output pins are referenced to FE_TXCLK.
FE_TXD[3:0]	O	CMOS SDR	VDDO_GIO	MII Transmit Data This bus is referenced to FE_TXCLK.
FE_TXEN	O	CMOS SDR	VDDO_GIO	MII Transmit Enable Indicates that the packet is being transmitted on the data lines. This pin is referenced to FE_TXCLK.
FE_TXERR	O	CMOS SDR	VDDO_GIO	MII Transmit Error This pin is referenced to FE_TXCLK.

2.2.10 Precision Timing Protocol (PTP) Interface

Note

These pins are implemented on the Multi-Purpose Pin interface.

Table 11: Precision Timing Protocol (PTP) Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
PTP_CLK	I	CMOS	VDDO_GIO	PTP reference clock for time stamping.
PTP_EVENT_REQ	I	CMOS	VDDO_GIO	PTP capturing event time.
PTP_TRIG_GEN	O	CMOS	VDDO_GIO	PTP pulse signal.

2.2.11 Pulse Width Modulation (PWM) Interface

Note These pins are implemented on the Multi-Purpose Pin interface.

Table 12: Pulse Width Modulation (PWM) Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
PWM[3:0]	O	OD	VDDO_PIO	Programmable Pulse Width Signal Generation.

2.2.12 Single (One) Wire Serial Interface

Note

These pins are implemented on the Multi-Purpose Pin interface.

Table 13: Single (One) Wire Serial Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
SWI_SIO	I/O OD	CMOS	VDDO_PIO	Serial Input / Output Pin. The SWI_SIO pin is an open-drain, bi-directional input/output pin used to serially transfer data to and from the device. The SWI_SIO pin must be pulled-high using an external pull-up resistor (not to exceed 4KOhm in value) and may be wire-ORed with any number of other open-drain or open-collector pins from other devices on the same bus.

2.2.13 Reference Clock

Table 14: Reference Clock Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
REF_CLK_XIN	I	Analog	SRD2_AVDD18	Crystal Clock Input
REF_CLK_XOUT	O	Analog	SRD2_AVDD18	Crystal Clock Output (feedback)

2.2.14 Multi Media Card (MMC) Interface

Table 15: Multi Media Card (MMC) Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
MMC_CLK	O	CMOS	VDDO_MMC	MMC Clock Output MMC_CMD and MMC_D[7:0] signals are referenced to this clock.
MMC_CMD	I/O	CMOS SDR	VDDO_MMC	MMC Command/Response This signal is referenced to MMC_CLK. **NOTE:** This pin must be pulled up to a power rail through 10 kilohm resistor.
MMC_D[7:0]	I/O	CMOS SDR	VDDO_MMC	MMC Data Bus This bus is referenced to MMC_CLK. **NOTE:** This bus must be pulled up to a power rail through 10 kilohm resistor.

2.2.15 Multi Media Card (MMC) High Speed DDR / 400MBps Interface

Table 16: Multi Media Card (MMC) High Speed DDR / 400MBps Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
MMC_CLK	O	CMOS	VDDO_MMC	MMC Clock Output MMC_CMD and MMC_D[7:0] signals are referenced to this clock.
MMC_CMD	I/O	CMOS SDR	VDDO_MMC	MMC Command/Response This signal is referenced to MMC_CLK. **NOTE:** This pin must be pulled up to a power rail through 10 kilohm resistor.
MMC_D[7:0]	I/O	CMOS DDR	VDDO_MMC	MMC Data Bus This bus is referenced to MMC_CLK during write and to MMC_STB during read. **NOTE:** This bus must be pulled up to a power rail through 10 kilohm resistor.
MMC_STB	I	CMOS	VDDO_MMC	MMC Data Strobe MMC_D[7:0] signals are referenced to this clock during read. **NOTE:** This pin must be pulled down to a ground through 10 kilohm resistor. **NOTE:** This signal is only relevant for the High Speed 400MBps (HS400) interface.

2.2.16 Secure Digital Input/Output (SDIO) Interface

Table 17: Secure Digital Input/Output (SDIO) Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
MMC_CLK	O	CMOS	VDDO_MMC	**SD1_CLK in SDIO DDR Host mode.** SDIO Clock Output SD1_CMD and SD1_D[3:0] signals are referenced to this clock.
MMC_CMD	I/O	CMOS SDR	VDDO_MMC	**SD1_CMD in SDIO DDR Host mode.** SDIO Command/Response This signal is referenced to SD1_CLK. **NOTE:** This pin must be pulled up to a power rail through 10 kilohm resistor.
MMC_D[3:0]	I/O	CMOS DDR	VDDO_MMC	**SD1_D[3:0] in SDIO DDR Host mode.** SDIO Data Bus This bus is referenced to SD1_CLK. **NOTE:** This bus must be pulled up to a power rail through 10 kilohm resistor.
SD0_CLK	O	CMOS	VDDIO_SD	**SD0_CLK in SDIO Host mode.** SDIO Clock Output SD0_CMD and SD0_D[3:0] signals are referenced to this clock.
				SD0_CLK in SDIO DDR Host mode. SDIO Clock Output SD0_CMD and SD0_D[3:0] signals are referenced to this clock.
SD0_CMD	I/O	CMOS SDR	VDDIO_SD	**SD0_CMD in SDIO Host mode.** SDIO Command/Response This signal is referenced to SD0_CLK. **NOTE:** This pin must be pulled up to a power rail through 10 kilohm resistor.
				SD0_CMD in SDIO DDR Host mode. SDIO Command/Response This signal is referenced to SD0_CLK. **NOTE:** This pin must be pulled up to a power rail through 10 kilohm resistor.
SD0_D[3:0]	I/O	CMOS SDR	VDDIO_SD	**SD0_D[3:0] in SDIO Host mode.** SDIO Data Bus This bus is referenced to SD0_CLK. **NOTE:** This bus must be pulled up to a power rail through 10 kilohm resistor.
		CMOS DDR		**SD0_D[3:0] in SDIO DDR Host mode.** SDIO Data Bus This bus is referenced to SD0_CLK. **NOTE:** This bus must be pulled up to a power rail through 10 kilohm resistor.

2.2.17 Master Serial Management Interface (SMI)

Note These pins are implemented on the Multi-Purpose Pin interface.

Table 18: Master Serial Management Interface (SMI) Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
SMI_MDC	O	CMOS	VDDO_GIO	Serial Management Interface Data Clock Provides the timing reference for the transfer of the SMI_ MDIO signal. **NOTE:** When not used, can be left NC.
SMI_MDIO	I/O	CMOS SDR	VDDO_GIO	Serial Management Interface Data Input/Output **NOTE:** When connected through a connector/module, must be pulled up to the interface power rail using a 2.0 kilohm resistor.

2.2.18 Universal Asynchronous Receiver Transmitter (UART) Interface

Note

These pins are implemented on the Multi-Purpose Pin interface.

Table 19: Universal Asynchronous Receiver Transmitter (UART) Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
UA1_RXD	I	CMOS	VDDO_JIO	UART Receive Data
UA1_TXD	O	CMOS	VDDO_JIO	UART Transmit Data
UA2_CTSn	I	CMOS	VDDO_PIO	UART Clear To Send
UA2_RTSn	O	CMOS	VDDO_PIO	UART Request To Send
UA2_RXD	I	CMOS	VDDO_PIO	UART Receive Data
UA2_TXD	O	CMOS	VDDO_PIO	UART Transmit Data

2.2.19 Serial Peripheral Interface (SPI)

Table 20: Serial Peripheral Interface (SPI) Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
SPI_CSn[3:0]	O	CMOS SDR	VDDO_PIO	SPI Chip-Select This signal is referenced to SPI_SCK. **NOTE:** This pin must be pulled up to a power rail. **NOTE:** SPI_CSn[3:1] pins are multiplexed on the MPP pin interface, as described in Section 5.1, GPIO and DDR Pin Multiplexing, on page 61.
SPI_HOLDn	O	CMOS	VDDO_PIO	SPI Hold signal. The Hold (HOLDn) signal is used to pause any serial communications with the device without de-selecting the device. **NOTE:** This pin is multiplexed on the MPP pin interface, as described in Section 5.1, GPIO and DDR Pin Multiplexing, on page 61.
SPI_MISO	I	CMOS SDR	VDDO_PIO	SPI Data In (Master In / Slave Out) This signal is referenced to SPI_SCK.
SPI_MOSI	O	CMOS SDR	VDDO_PIO	SPI Data Out (Master Out / Slave In) This signal is referenced to SPI_SCK.
SPI_SCK	O	CMOS	VDDO_PIO	SPI Clock Output All SPI signals are referenced to this clock.
SPI_WPn	O	CMOS	VDDO_PIO	SPI Write-Protect (WPn) signal. The main purpose of this signal is to freeze the size of the area of memory that is protected against program or erase instructions.

2.2.20 Miscellaneous Signals

Table 21: Miscellaneous Signals Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
RESET_N	I	OD	VDDO_JIO	System Reset Main reset signal of the device. Used to reset all units to their initial state.
TEST_MODE	I	CMOS	VDDO_JIO	Test Mode Used for internal testing purposes. **NOTE:** This pin must be tied to VSS for functional mode.
PMIC0_SLP_OUT	O	CMOS	VDDO_PIO	Power Management Integrated Circuits (PMIC) Sleep. When asserted, power down the regulator. **NOTE:** These pins are implemented on the Multi-Purpose Pin interface.
PMIC1_SLP_OUT	O	CMOS	VDDO_PIO	Power Management Integrated Circuits (PMIC) Sleep. When asserted, power down the regulator. **NOTE:** These pins are implemented on the Multi-Purpose Pin interface.
M_CAL	I	Calib		SDRAM DDR Calibration Pin. Connect 120 ohm to VSS.
M_VREF	I	SSTL		SDRAM Reference Voltage when internal VREF is not used.
ISET	I	Calib	SRD2_AVDD18	Analog reference current. This pin must be tied to a 6.04 kilohm +/-1% pull-down resistor.

2.2.21 SDRAM DDR3 Interface

Table 22: SDRAM DDR3 Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
M_CASn	O	SSTL SDR	VDDO_M	DRAM Column Address Strobe Asserted to indicate an active column address driven on the address lines. This signal is referenced to M_CLKOUT and M_CLKOUTn.
M_CLKOUT M_CLKOUTn	O	SSTL	VDDO_M	DRAM Differential Clock Output All address and control output signals are clocked on the crossing of the positive edge of M_CLKOUT and negative edge of M_CLKOUTn. The M_DQS[1:0]/M_DQSn[1:0] output (during the WRITE data phase) is referenced to the crossings of M_CLKOUT and M_CLKOUTn (both directions of crossing).
M_CKE[1:0]	O	SSTL SDR	VDDO_M	DRAM Clock Enable Control Driven high to enable DRAM clock. Driven low when setting the DRAM in self Refresh Mode or Power Down mode. All M_CKE[1:0] pins are driven together (no separate self refresh or power down mode per each DRAM bank). This signal is referenced to M_CLKOUT and M_CLKOUTn.
M_CSn[1:0]	O	SSTL SDR	VDDO_M	DRAM Chip Select Control Asserted to select a specific DRAM physical bank. This signal is referenced to M_CLKOUT and M_CLKOUTn.
M_DM[1:0]	O	SSTL DDR	VDDO_M	DRAM Data Mask Driven during writes to the DRAM to mask the corresponding group of M_DQ[15:0] and M_DQS[1:0]/M_DQSn[1:0] pins. This signal is referenced to M_DQS[1:0] and M_DQSn[1:0].
M_DQ[15:0]	I/O	SSTL DDR	VDDO_M	DRAM Data Bus Driven during writes to the DRAM. Driven by the DRAM during reads. These signals are referenced to M_DQS[1:0] and M_DQSn[1:0].
M_DQS[1:0] M_DQSn[1:0]	I/O	SSTL DDR	VDDO_M	DRAM Data Strobe Data strobe for input and output data. Driven during writes to the DRAM. Driven by the DRAM during reads.
M_ODT[1:0]	O	SSTL SDR	VDDO_M	DRAM On-Die Termination Control Driven to the DRAM to turn on/off the DRAM on-die termination resistor. This signal is referenced to M_CLKOUT and M_CLKOUTn.

Table 22: SDRAM DDR3 Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
M_RASn	O	SSTL SDR	VDDO_M	DRAM Row Address Strobe Asserted to indicate an active row address driven on the address lines. This signal is referenced to M_CLKOUT and M_ CLKOUTn.
M_RESETn	O	CMOS	VDDO_M	DRAM active low asynchronous reset.
M_WEn	O	SSTL SDR	VDDO_M	DRAM Write Enable Command Active low. Asserted to indicate a WRITE command to the DRAM. This signal is referenced to M_CLKOUT and M_ CLKOUTn.
M_A[15:0]	O	SSTL SDR	VDDO_M	DRAM Address Outputs Provides the row address for ACTIVE commands (M_ RASn), the column address, Auto Precharge bit (A[10]) and Burst Chop (A[12]) information for READ/WRITE commands (M_CASn), to determine, with the bank address bits (M_BA[2:0]), the DRAM address. These signals are referenced to M_CLKOUT and M_ CLKOUTn.
M_BA[2:0]	O	SSTL SDR	VDDO_M	DRAM Bank Address Outputs Selects one of the eight virtual banks during an ACTIVE (M_RASn), READ/WRITE (M_CASn), or PRECHARGE command. These signals are referenced to M_CLKOUT and M_ CLKOUTn.

2.2.22 SDRAM DDR4 Interface

Table 23: SDRAM DDR4 Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
M_CASn\A15	O	SSTL SDR	VDDO_M	DRAM Column Address Strobe / Address 15 Asserted to indicate an active column address driven on the address lines. This pin has multi function together with pin. This signal is referenced to M_CLKOUT and M_ CLKOUTn.
M_CLKOUT M_CLKOUTn	O	SSTL	VDDO_M	DRAM Differential Clock Output All address and control output signals are clocked on the crossing of the positive edge of M_CLKOUT and negative edge of M_CLKOUTn. The M_DQS[1:0]/M_DQSn[1:0] output (during the WRITE data phase) is referenced to the crossings of M_CLKOUT and M_CLKOUTn (both directions of crossing).
M_CKE[1:0]	O	SSTL SDR	VDDO_M	DRAM Clock Enable Control Driven high to enable DRAM clock. Driven low when setting the DRAM in self Refresh Mode or Power Down mode. All M_CKE[1:0] pins are driven together (no separate self refresh or power down mode per each DRAM bank). This signal is referenced to M_CLKOUT and M_ CLKOUTn.
M_CSn[1:0]	O	SSTL SDR	VDDO_M	DRAM Chip Select Control Asserted to select a specific DRAM physical bank. This signal is referenced to M_CLKOUT and M_ CLKOUTn.
M_DMn\DBIn[1:0]	O	POD DDR	VDDO_M	DRAM Data Mask Driven during writes to the DRAM to mask the corresponding group of M_DQ[15:0] and M_DQS[1:0]/M_ DQSn[1:0] pins. This signal is referenced to M_DQS[1:0] and M_ DQSn[1:0]. DRAM Data Bus Inversion Identifies whether to store/output the true or inverted data. Driven during writes to/from the DRAM to the corresponding group of DQ and DQS/DQSn pins. This signal is multiplexed on DMn pin. This signal is referenced to DQS and DQSn.
M_DQ[15:0]	I/O	POD DDR	VDDO_M	DRAM Data Bus Driven during writes to the DRAM. Driven by the DRAM during reads. These signals are referenced to M_DQS[1:0] and M_ DQSn[1:0].
M_DQS[1:0] M_DQSn[1:0]	I/O	POD DDR	VDDO_M	DRAM Data Strobe Data strobe for input and output data. Driven during writes to the DRAM. Driven by the DRAM during reads.

Table 23: SDRAM DDR4 Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
M_ODT[1:0]	O	SSTL SDR	VDDO_M	DRAM On-Die Termination Control Driven to the DRAM to turn on/off the DRAM on-die termination resistor. This signal is referenced to M_CLKOUT and M_ CLKOUTn.
M_RASn\A16	O	SSTL SDR	VDDO_M	DRAM Row Address Strobe / Address 16 Asserted to indicate an active row address driven on the address lines. This pin has multi function together with pin. This signal is referenced to M_CLKOUT and M_ CLKOUTn.
M_RESETn	O	CMOS	VDDO_M	DRAM active low asynchronous reset.
M_WEn\A14	O	SSTL SDR	VDDO_M	DRAM Write Enable Command / Address 14 Asserted to indicate a WRITE command to the DRAM. This pin has multi function together with pin. This signal is referenced to M_CLKOUT and M_ CLKOUTn.
M_A[13:0]	O	SSTL SDR	VDDO_M	DRAM Address Outputs Provides the row address for ACTIVE commands (M_ RASn/A16), the column address, Auto Precharge bit (A[10]) and Burst Chop (A[12]) information for READ/WRITE commands (M_CASn/A15), to determine, with the bank address bits (M_BA[1:0]), the DRAM address. These signals are referenced to M_CLKOUT and M_ CLKOUTn. The address outputs also provide the opcode during the LOAD MODE command. M_A[14], M_A[15], M_A[16] are multiplexed on other pins (M_WEn, M_CASn, M_RASn).
M_BA[1:0]	O	SSTL SDR	VDDO_M	DRAM Bank Address Outputs Selects one of the eight virtual banks during an ACTIVE (), READ/WRITE (), or PRECHARGE command. These signals are referenced to M_CLKOUT and M_ CLKOUTn.
Where <n> represents numbers 0 thru 1				
M_BG<n>	O	SSTL SDR	VDDO_M	DRAM Bank Group Outputs Defines to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during an MRS cycle. These signals are referenced to M_CLKOUT and M_ CLKOUTn.

2.2.23 PCI Express (PCIe) Interface

Note These signals are multiplexed on the SERDES Lane 1. Refer to Section 5.2, High-Speed SERDES Multiplexing, on page 62.

Table 24: PCI Express (PCIe) Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
PCIE_CLK_P/N	I/O	HCSL	SRD2_AVDD18	PCI Express Reference Clock 100 MHz Differential pair. When functions as output, each pin must be pulled down through an internal termination or external 49.9 Ohm 1% resistor.
PCIE_RESETn	O	CMOS	VDDO_GIO	Endpoint external triggered reset. For further details, refer to the RESET section. **NOTE:** This pin is multiplexed on the MPP interface, as described in Section 5.1, GPIO and DDR Pin Multiplexing, on page 61.
PCIE_CLKREQ	I	CMOS	VDDO_GIO	Endpoint request to enable/disable the reference clock. **NOTE:** This pin is multiplexed on the MPP interface, as described in Section 5.1, GPIO and DDR Pin Multiplexing, on page 61.
PCIE_RX_P/N	I	CML	SRD2_AVDD18	Receive Lane Differential pair of PCI Express.
PCIE_TX_P/N	O	CML	SRD2_AVDD18	Transmit Lane Differential pair of PCI Express.

2.2.24 Serial-ATA (SATA) Interface

Note

These signals are multiplexed on the SERDES Lane 2. Refer to Section 5.2, High-Speed SERDES Multiplexing, on page 62.

Table 25: Serial-ATA (SATA) Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
SATA_RX_P/N	I	CML	SRD1_AVDD18	Receive Lane Differential pair of SATA.
SATA_TX_P/N	O	CML	SRD1_AVDD18	Transmit Lane Differential pair of SATA.

2.2.25 Serial Embedded Trace Macrocell (sETM) Interface

Embedded Trace Module (ETM) for enhanced real time debug capabilities.

Table 26: Serial Embedded Trace Macrocell (sETM) Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
Where <n> represents numbers 1 thru 2				
SETM<n>_TX_P/N	O	CML	SRD1_AVDD18	sETM interface output from a dedicated SERDES.

2.2.26 Universal Serial Bus (USB) 2.0 Interface

Table 27: Universal Serial Bus (USB) 2.0 Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
USB0_DP/M	I/O	CML	USB_AVDD33	USB 2.0 Data Differential Pair.
USB_ID	I	Analog	USB_AVDD33	Identification pin for USB mode **NOTE:** This pin is internally pulled up to 1.8V. Input voltage range 0-1.9V
USB2_DRV/VBUS[1:0]	O	CMOS	VDDO_GIO	Current Limiter enable for VBUS power delivery to device. **NOTE:** These pins are multiplexed on the MPP interface, as described in Section 5.1, GPIO and DDR Pin Multiplexing, on page 61.
USB_VBUS	I	Analog	USB_AVDD33	In USB 2.0 and USB 3.0 device mode, sensing the existence of a USB connection. **NOTE:** This pin is internally pulled down to VSS. Input voltage range 0-5.5V
USB1_DP/M	I/O	CML	USB_AVDD33	USB 2.0 Data Differential Pair.

Refer to Section 5.3, Multiplexing USB 3.0 and USB 2.0 on the Same Connector, on page 62.

2.2.27 Universal Serial Bus (USB) 3.0 Interface

Note

These signals are multiplexed on the SERDES Lane 0 or 2. Refer to Section 5.2, High-Speed SERDES Multiplexing, on page 62.

Table 28: Universal Serial Bus (USB) 3.0 Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
USB3_RX_P/N	I	CML	SRD2_AVDD18	Receive Lane Differential pair of USB3. In the case where USB3 is used on Lane 2, the power rail is SRD1_AVDD18.
USB3_TX_P/N	O	CML	SRD2_AVDD18	Transmit Lane Differential pair of USB3. In the case where USB3 is used on Lane 2, the power rail is SRD1_AVDD18.

2.2.28 Serial Gigabit Media Independent Interface (SGMII)

The High Speed Gigabit Ethernet port can operate at 2.5 Gbps through an HS-SGMII interface.

The 2.5 Gigabit Ethernet port supports chip-to-chip connectivity.

The 1-Gigabit Ethernet port supports direct connection to Gigabit PHYs for 10/100/1000 Mbps using Auto-Negotiation capabilities.

In addition, this interface can be directly connected to SFP for 1000BASE-X.

Note

These signals are multiplexed on the SERDES Lanes 0 and 1. Refer to Section 5.2, High-Speed SERDES Multiplexing, on page 62.

Table 29: Serial Gigabit Media Independent Interface (SGMII) Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
Where <n> represents numbers 0 thru 1				
SGMII<n>_RX_P/N	I	CML	SRD2_AVDD18	SGMII / 1000BASE-X interface input to one 1.25/3.125 Gbps SERDES lane.
SGMII<n>_TX_P/N	O	CML	SRD2_AVDD18	SGMII / 1000BASE-X interface output from one 1.25/3.125 Gbps SERDES lane.

2.3 Reserved and Not Connected (NC)

Table 30: Reserved and Not Connected (NC) Pin Description

Pin Name	Description
NC	No Connect. Pin is floating and is not connected internally to any active circuitry nor have any electrical continuity to any other pin.
TEST	Test point for analyzing internal analog circuits. The test point must be connected to a full via. The TEST via must be enabled for probing from either the print or component side of PCB.

2.4 Internal Pull-up and Pull-down Pins

Table 31 lists the pins of the device package that are connected to internal pull-up and pull-down resistors. When these pins are not connected (NC) on the system board, these resistors set the default value for input and sample at reset configuration pins.

The internal pull-up and pull-down resistor value is between 20–70 kOhm. An external resistor with a lower value can override this internal resistor.

For the pin location, see the attached Excel files in Section 4, 88F3710/88F3720 Pin Map and Pin List, on page 60.

Table 31: Internal Pull-up and Pull-down Pins

Pin#	Pin	Pull Up/Down	Pin#	Pin	Pull Up/Down
G01	MPP1[0]	PU	A06	MPP2[2]	PU
H02	MPP1[1]	PU	B06	MPP2[3]	PU
H01	MPP1[2]	PU	A05	MPP2[4]	PU
J02	MPP1[3]	PU	B05	MPP2[5]	PU
L03	MPP1[4]	PU	A08	MPP2[6]	PD
K01	MPP1[5]	PU	C11	MPP2[12]	PD
K02	MPP1[6]	PU	D13	MPP2[13]	PD
J04	MPP1[7]	PU	E03	JT_RSTn	PU
M05	MPP1[8]	PU	E04	JT_TCK	PU
L01	MPP1[9]	PU	D05	JT_TDI	PD
F02	MPP1[11]	PD	C03	JT_TMS	PU
G02	MPP1[12]	PD	Y16	M_A[1]	PD
J03	MPP1[13]	PD	W14	M_BA[1]	PD
G04	MPP1[14]	PD	Y11	M_CKE[0]	PD
D02	MPP1[15]	PU	W11	M_CKE[1]	PD
G03	MPP1[16]	PU	C02	SPI_CSn[0]	PU
D01	MPP1[17]	PU	B02	SPI_MISO	PD
E02	MPP1[18]	PU	B01	SPI_MOSI	PD
E01	MPP1[19]	PU	A02	SPI_SCK	PU
D07	MPP2[0]	PD	B04	UA1_RXD	PU
C07	MPP2[1]	PD			

3 Unused Interface Strapping

Table 32 lists the signal strapping for systems in which some of the 88F3710/88F3720 interfaces are unused.

Table 32: Unused Interface Strapping

Unused Interface	Strapping
SDRAM	If there are unused clock pairs: • Leave the unused pair unconnected. • In the DDR Controller Control (Low) register (Offset: 0x1404), set <Clk1Drv> (bit[12]),<Clk2Drv> (bit[13]), or <Clk3Drv> (bit[15]) to 0 (high-Z). **NOTE:** M_CLKOUT[0] and M_CLKOUTn[0] cannot be disabled and are always driven. The following SDRAM signals can be left unconnected when unused: • M_A • M_BA • M_DM • M_DQ • M_DQS/DQSn • M_CSn • M_ODT • M_CKE • M_RESET
Ethernet SMI	Unused SMI_MDIO must be pulled up with a 1.0–4.7 kohm resistor to VDDO_GIO. Unused SMI_MDC can be left unconnected.
I^2C	Unused I2C<n>_SDA and I2C<n>_SCK signals must be pulled up with a 1.0–4.7 kohm resistor to VDDO_PIO.
UART	Unused UA<n>_RXD signals must be pulled up with a 1.0–4.7 kohm resistor to VDDO_JIO. Unused UA<n>_TXD signals can be left unconnected.
MPP	Configure unused signals as GPIO inputs. No external pullups are required. Leave the power rail driving the unused MPPs connected as follows: Leave VDDO_ GIO/PIO connected
USB 2.0	Unused USB<n>_DP and USB<n>_DM signals can be left unconnected. Power down any unused USB ports. Refer to the USB Host And Device Switching chapter and the USB32 Initialization Sequences chapter of the Functional Specifications. •
SERDES Lanes	Unused SERDES RX/TX P/N signals can be left unconnected. • Power down any unused SERDES port via register configuration.
PCIe Clocks	Unused signals can be left unconnected.

Table 32: Unused Interface Strapping (Continued)

Unused Interface	Strapping
MCi	Unused signals for this interface can be left unconnected. Leave MCI_AVDD12 and MCI_AVDD12D power rails unconnected
SDIO0	Unused signals for this interface can be left unconnected. Leave VDDIO_SD power rail unconnected
eMMC	Unused signals for this interface can be left unconnected. Leave VDDIO_MMC power rail unconnected

4 88F3710/88F3720 Pin Map and Pin List

The pin information files are provided as Excel file attachments. The Excel contains the pin list, pin map, and trace lengths.

Note The SDRAM pins in the pin list refer to the DDR3 interface. For details about DDR4, refer to Section 5.1, GPIO and DDR Pin Multiplexing, on page 61.

To open the attached Excel pin list files, double-click the pin icons below:

88F3710/88F3720 Pin Map and Pin List

Note File attachments are only supported by Adobe Reader 6.0 and above.

To download the latest version of free Adobe Reader go to http://www.adobe.com.

5 GPIO, PHY, and DDR Pin Multiplexing and Control

This section provides information on the functionality available by configuring the device's GPIO pins, and the interfaces supported by the high-speed SERDES PHYs.

5.1 GPIO and DDR Pin Multiplexing

The device contains GPIOs. Each GPIO pin can be assigned to a different functionality.

The attached Excel file lists each GPIO pins' functionality.

To open the attached Excel files, double-click the pin icons below.

88F3710/88F3720 Pin Muxing

88F3710/88F3720 DDR Pin Muxing

Note

File attachments are only supported by Adobe Reader 6.0 and above.

To download the latest version of free Adobe Reader go to http://www.adobe.com.

5.2 High-Speed SERDES Multiplexing

The 88F3710/88F3720 device integrates multiple SERDES PHY blocks.

Table 33 lists the different interfaces available.

Table 33: 88F3710/88F3720 PHY Mode Options

Interface	Lane 0 (USB3)	Lane 1 (PCIe)	Lane 2 (SATA)
PCIe		PCIe RC/EP	
SATA			SATA
SGMII	SGMII 1	SGMII 0	
USB 3	USB 3.0 (Host)[1] USB 3.0 (Device)[1]		USB 3.0 (Host)[1] USB 3.0 (Device)[1]

1. Only one USB 3.0 port can be used from Lane 0 or Lane 2.

5.3 Multiplexing USB 3.0 and USB 2.0 on the Same Connector

USB 3.0 and USB 2.0 must be routed to the same connector and only the USB 3.0 with USB 2.0 Port0 option is valid.

6 Clocking

6.1 Clock Domain

The 88F3710/88F3720 devices have multiple clock domains:

CPU Clock:	ARM Cortex CPU clocks—up to 1.0 GHz
Crystal Clock:	25 MHz or 40 MHz crystal mode
Timer Clock:	Up to 250 MHz
AXI Clock:	The Coherent Fabric clock, also used as the L2 cache clock—up to 500 MHz
DDR Controller Clock:	The SDRAM controller internal clock—up to 400 MHz for DDR3/DDR4 respectively
DDR Interface Clock:	The SDRAM interface clock—up to 800 MHz for DDR3/DDR4 respectively
PCIe Internal Clock Domains:	■ Runs at 250 MHz when configured to Gen 1.1 ■ Runs at 500 MHz when configured to Gen 2.0
GbE Ports Clock:	■ 312.5 MHz for 2500 Mbps ■ 125 MHz for 1000 Mbps ■ 25 MHz for 100 Mbps ■ 2.5 MHz for 10 Mbps
GbE Core Clock:	125 MHz or 250 MHz
SMI Clock:	Up to (GbE Core Clock)/8
SATA Clock:	Runs at 200 MHz
USB2 Clock:	Up to 40 MHz (High Speed mode)
USB3 Clock:	Up to 125 MHz (Super Speed mode)
UART Clock:	Up to 100 MHz
SPI Clock:	Up to 80 MHz
I^2C Clock:	Up to 3.4 MHz
SDIO and SDIO/eMMC Clocks:	Up to 200 MHz
JTAG Clock:	Up to 10 MHz
Security Processor Clock:	Up to 200 MHz
Internet Security Engine Clock:	Up to 500 MHz

Note For clock diagrams, refer to the Clock Topology section of the Design Guide.

6.2 Spread Spectrum Clock Generator (SSCG)

The SSCG (Spread Spectrum Clock Generator) can be used to generate the spread spectrum clock for the PLL input.

The SSCG block can be configured to perform up-spread, down-spread, and center-spread (refer to the SSCG Configuration register in the device Functional Specifications).

Both PLL support SSC operation and they are configured independently.

7 Reset and Initialization

This section details the device's reset sequence and initialization procedure.

7.1 Power Up/Down Sequence

7.1.1 Power-Up Sequence

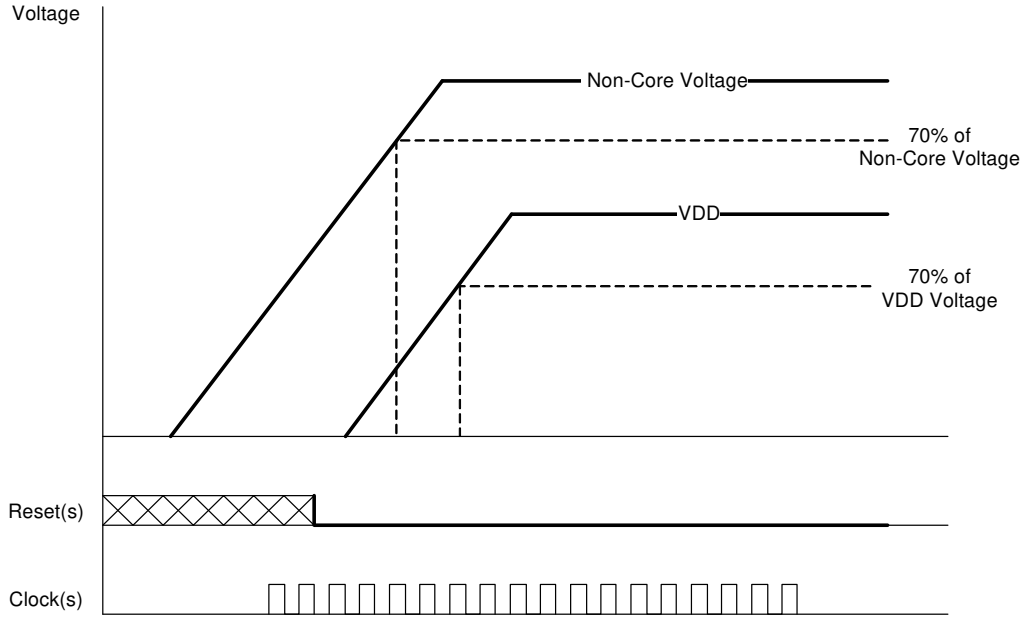
The following requirements must be applied to meet the device power-up sequence (see Figure 3).

- The Non-Core voltages (I/O and Analog) as listed in Table 34 must reach 70% of their voltage level before the Core voltages reach 70%.
  The order of the power up sequence between the Non-Core voltages is unimportant. The only requirement is for the Non-Core voltages power up before the Core voltages reach 70% of their voltage level.
- The reset signal(s) must be asserted before the Core voltages reach 70% of their voltage level.
- Each reference clock input must toggle with its respective voltage level before the first Core voltage reaches 70% of their voltage level. If a crystal oscillator is used, the system can rely on the oscillator wake-up mechanism.

Table 34: Non-Core and Core Voltages

Non-Core Voltages		Core Voltages
I/O Voltages	**Analog Power Supplies**	
VDDO_JIO (JTAG, UART) VDDO_PIO (GPIO1) VDDO_GIO (GPIO2) VDDO_MMC (eMMC) VDDO_M (DDR) VDDIO_SD (SDIO)	SRD1_AVDD18 (SETM, SATA, USB3) SRD2_AVDD18 (SGMII, USB3, PCIe, SGMII, Crystal (Xtal)) USB_AVDD18 (USB2) USB_AVDD33 (USB2) MCI_AVDD12, MCI_AVDD12D (MCi) PLL_AVDD18 (PLL)	VDD

Figure 3: Power Up Sequence Example



Note

- It is the system designer's responsibility to verify that the power sequencing requirements of other components are also met.
- Although the Non-Core voltages can be powered up any time before the Core voltages, allow a reasonable time limit (for example 100 ms) between the **first** Non-Core voltage power-up and the **last** Core voltage power-up.

7.1.2 Power-Down Sequence

Allow a reasonable time limit (for example 100 ms) between the **first** and **last** voltage power-down.

7.2 Adaptive Voltage Scaling (AVS)

The device integrates a single Adaptive Voltage Scaling (AVS) unit that controls the core voltage (VDD) via the AVS_VDDFB signal.

The AVS unit optimizes the performance and power consumption of the device by adjusting the external power regulator output voltage according to the pre-defined voltage range. The target voltage range is set during the manufacturing stage for optimal power consumption in a given CPU frequency range.

The AVS unit samples the controlled on-die voltage level at runtime and controls the power regulator supply output using the AVS_FB feedback pin, until the system achieves the desired on-die voltage.

The initial regulator output setting is specified in Section 9.2, Recommended Operating Conditions.

Upon hardware reset assertion, the AVS unit samples the on-die voltage levels and adjusts the regulator voltage output according to the pre-configured voltage range setting.

When the desired levels are achieved, the AVS unit releases the internal hardware reset signal, and the device continues with the power up sequence.

7.3 Hardware Reset

The device has one reset input pin: RESET_N.

When asserted, the entire chip is placed in its initial state.

RESET_N is open drain and can be driven by the SoC to reset the board.

7.4 PCIe Reset

As a Root Complex, the device can generate a Hot Reset to the PCIe port. Upon CPU setting of the PCIe Control register's <ConMstrHot Reset> bit, the PCIe unit sends a Hot Reset indication to the Endpoint (see the PCIe Interface section in the device's Functional Specifications).

When the device works as an Endpoint, and a Hot Reset packet is received:

- A maskable interrupt is asserted.
- If the PCIe Debug Control register's <DisHotResetRegRst> is cleared, the device also resets the PCIe register file to its default values.
- The device triggers an internal reset, if not masked by PCIe Debug Control register's <ConfMskHotReset> bit.

Link failure is detected if the PCIe link was up (LTTSSM L0 state) and dropped back to an inactive state (LTSSM Detect state). When Link failure is detected:

- A maskable interrupt is asserted
- If the PCIe Debug Control register's <DisLinkFailRegRst> is cleared, the device also resets the PCIe register file to its default values.
- The device triggers an internal reset, if not masked by PCIe Debug Control register's <ConfMskLinkFail> bit.

Whether initiated by a hot reset or link failure, this internal reset indication can be routed to the PCIe_RSTOUTn signal (multiplexed on MPPs) to reset components on the board without resetting the entire device (e.g reset only the endpoint card).

7.5 Reset Configuration

The rising edge of RESET_N, the global reset de-assertion, is used to latch the GPIO pins: GPIO1, in an internal latch (xD0013808 and xD001380C), and GPIO2, in an internal latch (0xD0018808). The latched values are preserved after RESET_N de-assertion.

Weak pull-up or pull-down resistors can be used to set any of these pin values, but only GPIO1[9:5]pins are used to configure the SOC.

7.6 Boot Modes

The pins GPIO1[9:5] are used to configure the SoC.

The Boot ROM uses pins GPIO1[7:5] as bootstrap pins to determine the boot option. GPIO1[8] must have a pull-down resistor.

In the normal mode, each of the GPIO1[15:0] pins can be programmed to output different monitor signals from different blocks inside the SoC. These signals need to be brought out to probe points on the PCB.

For all boot modes, the initial clock frequencies are as follows:

- DDR_WCK = 1.2 GHz (Clock used by the DDR PHY)
- DDR_MCK = 300 MHz (Clock used by the DDR Memory Controller)
- DDR_FCLK = 100 MHz (A slow clock used by the memory controller DDR_MC logic that doesn't require high speed)
  DDR_WCK is 4 x DDR_MCK.

  The clock out to the DDR chip is 2x DDR_MCK.
- TBG-A = 1200 MHz
- TBG-B = 800 MHz
- AP CPU = 400 MHz
- AXI = 200 MHz
- SPI = 160 MHz
- SATA = 160 MHz
- eMMC = 50 MHz (200 MHz from clock gen)

Table 35: Crystal Modes

GPIO1[9]	Crystal Mode
0	25 MHz
1	40 MHz

Table 36: Test Mode

GPIO1[8]	Mode
0	Normal mode
1	Test mode

Table 37: Normal Operation Boot Modes

GPIO1[7:5]	Boot Mode Description
001b	Serial NOR Flash Download Mode. Download boot loader or program code from Serial NOR flash into CM3 or A53.
010b	eMMC Download Mode. Download boot loader or program code from eMMC flash into CM3 or A53. Requires full initialization and command sequence.
011b	eMMC Alternate Download Mode. Download boot loader or program code from eMMC flash into CM3 or A53. For cases when the eMMC Device is pre-programmed to support eMMC Alternate Boot Mode.
100b	SATA Download Mode. Download boot loader or program code from AHCI interface into CM3 or A53.
101b	Serial NAND Flash Download Mode. Download boot loader or program code from SPI flash into CM3 or A53.
110b	UART Mode. • Download boot loader or program code from UART interface (WTPTP) into CM3 or A53. • Simple UART monitor code is executed within the Boot ROM, allowing internal registers for read/write through external UART terminal.
111b	Reserved

8 JTAG Interface

To enable board testing, the device supports a test mode operation through its JTAG boundary scan interface.

The JTAG interface is IEEE 1149.1 standard compliant. It supports mandatory and optional boundary scan instructions.

8.1 TAP Controller

The Test Access Port (TAP) is constructed with a 5-pin interface and a 16-state Finite State Machine (FSM), as defined by IEEE JTAG standard 1149.1.

To place the device in a functional mode, reset the JTAG state machine to disable the JTAG interface.

According to the IEEE 1149.1 standard, the JTAG state machine is not reset when the 88F3710/88F3720 RESET_N is asserted. The JTAG state machine can only be reset by one of the following methods:

- Asserting JT_RSTn.
- Setting JT_TMS for at least five JT_CLK cycles.

To place the device in one of the boundary scan test mode, the JTAG state machine must be moved to its control states. JT_TMS and JT_TDI inputs control the state transitions of the JTAG state machine, as specified in the IEEE 1149.1 standard. The JTAG state machine will shift instructions into the Instruction register while in *SHIFT-IR* state and shift data into and from the various data registers when in *SHIFT-DR* state.

8.2 Instruction Register

The Instruction register (IR) is a 4-bit, two-stage register. It contains the command that is shifted in when the DAP FSM is in the *Shift-IR* state. When the DAP FSM is in the *Capture-IR* state, the IR outputs all four bits in parallel.

Table 38 lists the instructions supported by the device.

Table 38: Supported JTAG Instructions

Instruction	Code	Description
HIGH-Z	00011	Select the single bit Bypass register between TDI and TDO. Sets the device output pins to high-impedance state.
IDCODE	00010	Selects the Identification register between TDI and TDO. This 32-bit register is used to identify the device.
EXTEST	00000	Selects the Boundary Scan register between TDI and TDO. Outputs the boundary scan register cells to drive the output pins of the device. Inputs the boundary scan register cell to sample the input pin of the device.

Table 38: Supported JTAG Instructions (Continued)

Instruction	Code	Description
SAMPLE/ PRELOAD	00001	Selects the Boundary Scan register between TDI and TDO. Samples input pins of the device to input boundary scan register cells. Preloads the output boundary scan register cells with the Boundary Scan register value.
BYPASS	11111	Selects the single bit Bypass register between TDI and TDO. This allows for rapid data movement through an untested device.

8.3 Bypass Register

The Bypass register (BR) is a single bit serial shift register that connects TDI to TDO, when the IR holds the Bypass command, and the TAP FSM is in *Shift-DR* state. Data that is driven on the TDI input pin is shifted out one cycle later on the TDO output pin. The Bypass register is loaded with 0 when the TAP FSM is in the *Capture-DR* state.

8.4 JTAG Scan Chain

The JTAG Scan Chain is a serial shift register used to sample and drive all of the device pins during the JTAG tests. It is a 2-bit per pin shift register in the device, thereby allowing the shift register to sequentially access all of the data pins both for driving and strobing data. For further details, refer to the BSDL Description file for the device.

8.5 ID Register

The ID register is a 32-bit deep serial shift register. The ID register is loaded with vendor and device information when the DAP FSM is in the *Capture-DR* state. The Identification code format of the ID register is shown in Table 39, which describes the various ID Code fields.

Table 39: IDCODE Register Map

Bits	Value	Description
31:28	0x2	Version
27:12	0x200	Part number
11:1	0x1E9	Manufacturer ID
0	0x1	Mandatory—This bit must be set to 0x1.

9 Electrical Specifications

9.1 Absolute Maximum Ratings

Table 40: Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
VDD	-0.5	1.4	V	Core voltage
PLL_AVDD18	-0.5	2.2	V	Analog supply for the PLLs, AVS, and VHV for the eFuse
MCI_AVDD12	-0.5	1.5	V	I/O voltage for MCi interface
MCI_AVDD12D	-0.5	1.5	V	I/O voltage for MCi interface
SRD1_AVDD18	-0.5	2.2	V	I/O voltage for SATA and SETM interfaces
SRD2_AVDD18	-0.5	2.2	V	I/O voltage for Crystal, SGMII, PCIe, SERDES common, and USB3 interfaces
USB_AVDD18	-0.5	2.2	V	I/O voltage for USB 2.0 @ 1.8V
USB_AVDD33	-0.5	4	V	I/O voltage for USB 2.0 interface @ 3.3V
VDDO_GIO	-0.5	3.2	V	I/O voltage for MPP2[23:0]
VDDO_JIO	-0.5	3.2	V	I/O voltage for JTAG and UART1 interface
VDDO_M	-0.5	1.9	V	I/O voltage for DDR3, DDR3L, and and DDR4 SDRAM interface
VDDO_MMC	-0.5	4	V	I/O voltage for SDIO1/eMMC interface
VDDO_PIO	-0.5	3.2	V	I/O voltage for MPP1[19:0] (I2C1, I2C2, SWI, UART2, SPI, and PWM/LED interfaces)
VDDIO_SD	-0.5	4	V	I/O voltage for SDIO interface
TC	-40	125	° C	Case temperature
TSTG	-40	125	° C	Storage temperature

Caution

- Exposure to conditions at or beyond the maximum rating can damage the device.
- Operation beyond the recommended operating conditions (Table 41) is neither recommended nor guaranteed.

9.2 Recommended Operating Conditions

Table 41: Recommended Operating Conditions

Parameter	Min	Typ	Max	Units	Comments
VDD (Regulator Setting)	1.0	1.05	1.1	V	Core voltage.
VDD (Actual)	1.05	1.1	1.2	V	Core voltage for 800 MHz (at device ball target controlled by AVS). Core voltage for 1000 MHz should be increased by 50mV. **NOTE:** If AVS is not applied, the maximum CPU frequency is limited to 600 MHz.
PLL_AVDD18	1.7	1.8	1.9	V	Analog supply for the PLLs, AVS, and VHV for the eFuse
MCI_AVDD12	1.14	1.2	1.26	V	I/O voltage for MCi interface
MCI_AVDD12D	1.14	1.2	1.26	V	I/O voltage for MCi interface
SRD1_AVDD18	1.7	1.8	1.9	V	I/O voltage for SATA and SETM interfaces
SRD2_AVDD18	1.7	1.8	1.9	V	I/O voltage for Crystal, SGMII, PCIe, SERDES common, and USB3 interfaces
USB_AVDD18	1.7	1.8	1.9	V	I/O voltage for USB 2.0 interface at 1.8V
USB_AVDD33	3.15	3.3	3.45	V	I/O voltage for USB 2.0 interface at 3.3V
VDDO_GIO	2.375	2.5	2.625	V	I/O voltage for MPP2[23:0]
	1.7	1.8	1.9	V	
VDDO_JIO	2.375	2.5	2.625	V	I/O voltage for JTAG and UART1 interface
	1.7	1.8	1.9	V	
VDDO_M	1.425	1.5	1.575	V	I/O voltage for DDR3 SDRAM interface
	1.283	1.35	1.45	V	I/O voltage for DDR3L SDRAM interface
	1.14	1.2	1.26	V	I/O voltage for DDR4 SDRAM interfaces
VDDO_MMC	3.15	3.3	3.45	V	I/O voltage for SDIO1/eMMC interface
	1.7	1.8	1.9	V	
VDDO_PIO	2.375	2.5	2.625	V	I/O voltage for MPP1[19:0] (I2C1, I2C2, SWI, UART2, SPI, and PWM/LED interfaces)
	1.7	1.8	1.9	V	
VDDIO_SD	3.15	3.3	3.45	V	I/O voltage for SDIO interface
	1.7	1.8	1.9	V	
T_A	0		70	° C	Ambient Operating Temperature Commercial
	-40		85	° C	Ambient Operating Temperature Industrial

Table 41: Recommended Operating Conditions (Continued)

Parameter	Min	Typ	Max	Units	Comments
T_J			115	° C	Maximum Junction Temperature

Caution Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

9.3 Current Consumption

Table 42: Current Consumption

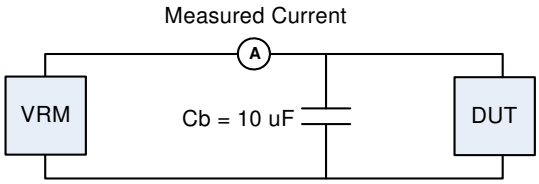
Interface	Symbol	Test Conditions	Current[2] (Max)	Units
Core and CPU[1]				
Single Embedded CPU Core, 256MB L2 cache and SoC logic	I_{PVDD}	CPU Core running at 600 MHz, VDD=1.05V, Tj=105°C	1450	mA
		CPU Core running at 800 MHz, VDD=1.1V, Tj=105°C	1735	mA
		CPU Core running at 1000 MHz, VDD=1.15V, Tj=105°C	2060	mA
Dual Embedded CPU Cores, 256MB L2 cache and SoC logic	I_{PVDD}	CPU Core running at 600 MHz, VDD=1.05V, Tj=105°C	1640	mA
		CPU Core running at 800 MHz, VDD=1.1V, Tj=105°C	1970	mA
		CPU Core running at 1000 MHz, VDD=1.15V, Tj=105°C	2340	mA
DDR3/DDR3L 16-bit Interface				
DDR3L interface (16-bit, 600 MHz, 1.35V)	I_{VDDO_M}	M_CLKOUT = 600 MHz, 1 DRAM rank, Termination: 60 Ohm internal, 60 Ohm DRAM	270	mA
DDR3L interface (16-bit, 800 MHz, 1.35V)		M_CLKOUT = 800 MHz, 1 DRAM rank, Termination: 60 Ohm internal, 60 Ohm DRAM	310	mA
DDR3 interface (16-bit, 600 MHz, 1.5V)		M_CLKOUT = 600 MHz, 1 DRAM rank, Termination: 60 Ohm internal, 60 Ohm DRAM	270	mA
DDR3 interface (16-bit, 800 MHz, 1.5V)		M_CLKOUT = 800 MHz, 1 DRAM rank, Termination: 60 Ohm internal, 60 Ohm DRAM	310	mA
DDR4 Interface 16-bit				
DDR4 interface (16-bit, 800 MHz, 1.2V)	I_{VDDO_M}	1 DRAM rank	260	mA
Miscellaneous				
Miscellaneous interface	I_{MISC}	JTAG, UART, I2C, SPI, and reset signals	50	mA
MII interface	I_{MII}	Single Port, VDDO = 2.5V	10	mA
RGMII interface	I_{RGMII}	Single Port, VDDO = 1.8V	40	mA
		Single Port, VDDO = 2.5V	50	mA
SERDES interface	I_{SRD_AVDD}	Single SERDES Port = 1.25 Gbps	50	mA
		Single SERDES Port = 2.5 Gbps	65	mA
		Single SERDES Port = 3.125 Gbps	70	mA
		Single SERDES Port = 5.0 Gbps	80	mA
		Single SERDES Port = 6.25 Gbps	85	mA
USB 2.0 interface	I_{USB_AVDD33}	USB 2.0 Ports USB_AVDD33	3	mA
	I_{USB_AVDD18}	USB 2.0 Ports USB_AVDD18	30	mA
PLL, AVS	I_{PLL_AVDD18}	1.8V CPU PLL, SSCG, and AVS blocks	50	mA

NOTES:

1. A Dhrystone test was used to estimate the embedded CPU power values

2. Current in mA is calculated using maximum recommended VDDIO specification for each power rail.
3. All output clocks toggling at their specified rate.
4. Maximum drawn current from the power supply.
5. SRD_AVDD can be SRD1_AVDD18 or SRD2_AVDD18 depending on the interface– SGMII, USB3.0, SATA, PCIe.

Figure 4: Test Setup for Core/CPU Current Specifications



9.4 DC Electrical Specifications

Note For internal pullup/pulldown information, see Section 2.2, Pin Descriptions.

9.4.1 Generic CMOS 3.3V DC Electrical Specifications

The DC electrical specifications in Table 43 are applicable for the following interfaces and signals:

- MMC
- SDIO

Note VDDIO can refer to the VDDO_MMC / VDDIO_SD pins, depending on the interface/pin (see Table 2, Power Pins Pin Description, on page 26).

Table 43: Generic CMOS 3.3V Interface DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.8	V	-
Input high level	VIH		2.0		VDDIO+0.3	V	-
Output low level	VOL	IOL = 8 mA	-		0.6	V	-
Output high level	VOH	IOH = -8 mA	2.2		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

9.4.2 Generic CMOS 2.5V (CMOS) DC Electrical Specifications

The DC electrical specifications in Table 44 are applicable for the following interfaces and signals:

- RGMII
- MII
- SMI
- JTAG
- UART
- I^2C
- SPI

Note VDDIO can refer to the VDDO_GIO, VDDO_JIO, VDDIO_SD, or VDDO_PIO pins, depending ton the interface/pin (see Table 2, Power Pins Pin Description, on page 26).

Table 44: Generic CMOS 2.5V Interface DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.7	V	-
Input high level	VIH		1.7		VDDIO+0.3	V	-
Output low level	VOL	IOL = 8 mA	-		0.6	V	-
Output high level	VOH	IOH = -8 mA	1.8		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

9.4.3 Generic CMOS 1.8V DC Electrical Specifications

The DC electrical specifications in Table 45 are applicable for the following interfaces and signals:

- RGMII
- MII
- SMI
- SDIO
- MMC
- JTAG
- SPI
- I^2C

Note VDDIO can refer to the VDDO_GIO, VDDO_PIO, VDDIO_SD, VDDO_MMC, VDDO_JIO pins, depending on the interface/pin (see Table 2, Power Pins Pin Description, on page 26).

Table 45: Generic CMOS 1.8V Interface DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.35*VDDIO	V	-
Input high level	VIH		0.65*VDDIO		VDDIO+0.3	V	-
Output low level	VOL	IOL = 8 mA	-		0.45	V	-
Output high level	VOH	IOH = -8 mA	VDDIO-0.45		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

Table 46: Open Drain 1.8/2.5V Interface DC Electrical Specifications (Applicable Only to MPP1[14:11])

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
IO supply voltage	VDDO	-	2.25	2.5	2.75	V	
			1.62	1.8	1.98	V	
Input low level	VIL		-0.4		0.7	V	
Input high level	VIH		1.7		5.5V	V	
Hysteresis of input voltage	Vhys	-	300	400	-	mV	
Output current	Iol @ 0.4V		15	30	-	mA	
Input capacitance	-	Exclude bond wire & lead	-	-	5	pF	
Input leakage 1	-	VDDO is ON 0<V(PAD)<5.5V	-	-	30	uA	
Input leakage 2	-	VDDO is OFF, 0<V(PAD)<5.5V	-	-	30	uA	

9.4.4 SDRAM DDR3 Interface DC Electrical Specifications

Note In Table 47, VDDIO represents the VDDO_M pin.

Table 47: SDRAM DDR3 Interface DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Single ended input low level	VIL		-0.3		VDDIO/2 - 0.100	V	-
Single ended input high level	VIH		VDDIO/2 + 0.100		VDDIO + 0.3	V	-
Differential input low level	VDIL		Note 6		-0.2	V	6
Differential input high level	VDIH		0.2		Note 6	V	6
Output low level	VOL	IOL = 8 mA			0.2*VDDIO	V	7
Output high level	VOH	IOH = -8 mA	0.8*VDDIO			V	7
Rtt effective impedance value	RTT	See note 2	50	60	70	ohm	1 , 2
Deviation of VM with respect to VDDIO/2	dVm	See note 3	-5		5	%	3
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	4, 5
Pin capacitance	Cpin	-		5		pF	-

Notes:

1. See SDRAM functional description section for ODT configuration.
2. Measurement definition for RTT: Apply (VDDIO/2) +/- 0.15 to input pin separately, then measure current $I_{(VDDIO/2+0.15)}$ and $I_{(VDDIO/2-0.15)}$ respectively.

$$RTT = \frac{0.30}{I_{(\frac{VDDIO}{2}+0.15)} - I_{(\frac{VDDIO}{2}-0.15)}}$$

3. Measurement definition for VM: Measured voltage (VM) at input pin (midpoint) with no load.

$$dVM = \left(\frac{2 \times Vm}{VDDIO} - 1\right) \times 100\,\%$$

4. While I/O is in High-Z.
5. This current does not include the current flowing through the pullup/pulldown resistor.
6. Limitations are same as for single ended signals.
7. Defined when driver impedance is calibrated to 35 ohms.

9.4.5 SDRAM DDR3L Interface DC Electrical Specifications

Note

In Table 48, VDDIO represents the VDDO_M pin.

Table 48: SDRAM DDR3L Interface DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Single ended input low level	VIL		-0.3		VDDIO/2 - 0.09	V	-
Single ended input high level	VIH		VDDIO/2 + 0.09		VDDIO + 0.3	V	-
Differential input low level	VDIL		Note 6		-0.16	V	6
Differential input high level	VDIH		0.16		Note 6	V	6
Output low level	VOL	IOL = 7 mA			0.2*VDDIO	V	7
Output high level	VOH	IOH = -7 mA	0.8*VDDIO			V	7
Rtt effective impedance value	RTT	See note 2	50	60	70	ohm	1 , 2
Deviation of VM with respect to VDDIO/2	dVm	See note 3	-5		5	%	3
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	4, 5
Pin capacitance	Cpin	-		5		pF	-

Notes:

1. See SDRAM functional description section for ODT configuration.
2. Measurement definition for RTT: Apply (VDDIO/2) +/- 0.15 to input pin separately, then measure current $I_{(VDDIO/2+0.15)}$ and $I_{(VDDIO/2-0.15)}$ respectively.

$$RTT = \frac{0.30}{I_{(\frac{VDDIO}{2}+0.15)} - I_{(\frac{VDDIO}{2}-0.15)}}$$

3. Measurement definition for VM: Measured voltage (VM) at input pin (midpoint) with no load.

$$dVM = \left(\frac{2 \times Vm}{VDDIO} - 1\right) \times 100\,\%$$

4. While I/O is in High-Z.
5. This current does not include the current flowing through the pullup/pulldown resistor.
6. Limitations are same as for single ended signals.
7. Defined when driver impedance is calibrated to 35 ohms.

9.4.6 SDRAM DDR4 Interface DC Electrical Specifications

Note In Table 49, VDDIO represents the VDDO_M pin.

Table 49: SDRAM DDR4 Interface DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
IO Supply	VDDQ		1.14	1.2	1.26	V	
Single ended input low level	VIL	-0.3	-0.3		VREF-0.100	V	
Single ended input high level	VIH	VREF+0.100			VDDIO+0.3	V	
Differential input low level	VDIL				-0.2	V	
Differential input high level	VDIH	0.2				V	
Output low level	VOL				0.2*VDDQ	V	1
Output high level	VOH	0.8*VDDQ				V	1
Rtt effective impedance value	RTT	48	60		72	ohm	
Pin capacitance	Cpin		3		4	pF	

Notes:
1. Specified at max drive strength

9.4.7 I²C Interface (TWSI) 2.5V DC Electrical Specifications

In Table 50, VDDIO represents the VDDO_PIO pin.

Table 50: I²C Interface 2.5V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.7	V	-
Input high level	VIH		1.7		VDDIO+0.3	V	-
Output low level	VOL	IOL = 1 mA	-		0.4	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

9.4.8 Adaptive Voltage Scaling (AVS) DC Electrical Specification

Table 51: AVS DC Electrical Specification

Parameter	Symbol	Min	Max	Units	Notes
Output voltage level	VOUT	VDD - 200	VDD + 200	mV	1
Output current drive/sink	IOUT	-1	1	mA	2
Allowed load capacitance	CLOAD		100	pF	3

Notes:

1. VDD is the actual voltage supplied to the device.
2. Actual current is determined by the external resistor (RAVS) and the output voltage.
3. This load includes board routing and regulator capacitance.

9.5 AC Electrical Specifications

For differential interface specifications, see Section 9.6, Differential Interface Electrical Characteristics, on page 125.

9.5.1 Reference Clock and Reset AC Timing Specifications

Table 52: Reference Clock and Reset AC Timing Specifications

Description	Symbol	Min	Max	Units	Notes
Core/CPU Reference Clock					
Frequency	$F_{REF\_CLK\_XIN}$	25		MHz	
Accuracy	$PPM_{REF\_CLK\_XIN}$	-100	+100	ppm	
Clock duty cycle	$DC_{REF\_CLK\_XIN}$	45	55	%	
Slew rate	$SR_{REF\_CLK\_XIN}$	0.5		V/ns	1
		0.7		V/ns	1, 2
Pk-Pk jitter	$JR_{REF\_CLK\_XIN}$		120	ps	2, 3
			200	ps	
Core/CPU Reference Clock					
Frequency	$F_{REF\_CLK\_XIN}$	40		MHz	
Accuracy	$PPM_{REF\_CLK\_XIN}$	-100	+100	ppm	
Clock duty cycle	$DC_{REF\_CLK\_XIN}$	45	55	%	
Slew rate	$SR_{REF\_CLK\_XIN}$	0.5		V/ns	1
		0.7		V/ns	1, 2
Pk-Pk jitter	$JR_{REF\_CLK\_XIN}$		120	ps	2, 3
			200	ps	
Core/CPU Reference Clock Spread Spectrum Requirement					
Modulation Frequency	$Fmod_{REF\_CLK\_XIN}$	0	33	kHz	4
Modulation Index	$Fspread_{REF\_CLK\_XIN}$	-0.5	0	%	4
Ethernet Interface (MII MAC Mode)					
Frequency	F_{FE_TXCLK}	2.5	50	MHz	
	F_{FE_RXCLK}				
Accuracy	PPM_{FE_TXCLK}	-100	100	PPM	
	PPM_{FE_RXCLK}				

Table 52: Reference Clock and Reset AC Timing Specifications (Continued)

Description	Symbol	Min	Max	Units	Notes
Duty cycle	DC_{FE_TXCLK}	35	65	%	
	DC_{FE_RXCLK}				
Slew rate	SR_{FE_TXCLK}	0.5		V/ns	1
	SR_{FE_RXCLK}				
SDIO / MMC Interface					
Frequency (MMC mode)	F_{MMC_CLK}		50	MHz	
Frequency (MMC HS200 mode)	$F_{MMCHS200\_CLK}$		200	MHz	
Frequency (MMC HS400 mode)	$F_{MMCHS400\_CLK}$		200	MHz	
Frequency (SDIO SDR mode)	F_{SD_CLK}		200	MHz	
Frequency (SDIO DDR mode)	F_{SD_CLK}		50	MHz	
SMI Reference Clock					
SMI output MDC clock	F_{SMI_MDC}	GbE Core Clock/128	GbE Core Clock/8	MHz	
I^2C Master Mode Reference Clock					
SCK output clock	F_{I2C1_SCK}		100	kHz	6
	F_{I2C2_SCK}		100	kHz	6
PTP Reference Clock					
Frequency	F_{PTP_CLK}		125	MHz	
Accuracy	PPM_{PTP_CLK}	-100	100	ppm	
Duty cycle	DC_{PTP_CLK}	40	60	%	
Slew rate	SR_{PTP_CLK}	0.7		V/ns	1
Pk-Pk jitter	JR_{PTP_CLK}		100	ps	
SPI Output Clock					
Frequency	$F_{SPI<n>\_SCK}$ <n> = 0 thru 1		80	MHz	5
JTAG Reference Clock					
Frequency	F_{JT_CLK}		10	MHz	

Notes:

1. Slew rate is defined from 20% to 80% of the reference clock signal.
2. This value is required when using the internal PLL to drive the SERDES.

3. This value is assumed to contain above 95% random components characterized by 1/f behavior, defined with a BER = 1e-12.
4. Defined on linear sweep or “Hershey’s Kiss” (US Patent 5,631,920) modulations.
5. For additional information regarding configuring this clock, see the SPI Interface Configuration Register in the device’s Functional Specification.
6. For additional information, see Section 9.5.9, Inter-integrated Circuit Interface (I2C) AC Timing, on page 114.

9.5.2 Reduced Gigabit Media Independent Interface (RGMII) AC Timing

9.5.2.1 RGMII AC Timing Table

Table 53: RGMII AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Clock frequency	fCK	125.0		MHz	-
Data to Clock output skew	TskewT	-0.50	0.50	ns	2
Data to Clock input skew	TskewR	1.00	2.60	ns	-
Clock cycle duration	Tcyc	7.20	8.80	ns	1 , 2
Duty cycle for Gigabit	Duty_G	0.45	0.55	tCK	2
Duty cycle for 10/100 Megabit	Duty_T	0.40	0.60	tCK	2

Notes:

General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

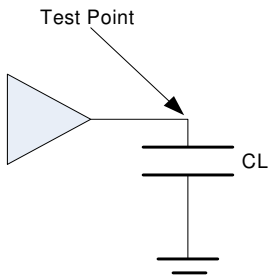
General comment: tCK = 1/fCK.

General comment: If the PHY does not support internal-delay mode, the PC board design requires routing clocks so that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal.
For 10/100 Mbps RGMII, the Max value is unspecified.

1. For RGMII at 10 Mbps and 100 Mbps, Tcyc will scale to 400 ns +/-40 ns and 40 ns +/-4 ns, respectively.
2. For all signals, the load is CL = 5 pF.

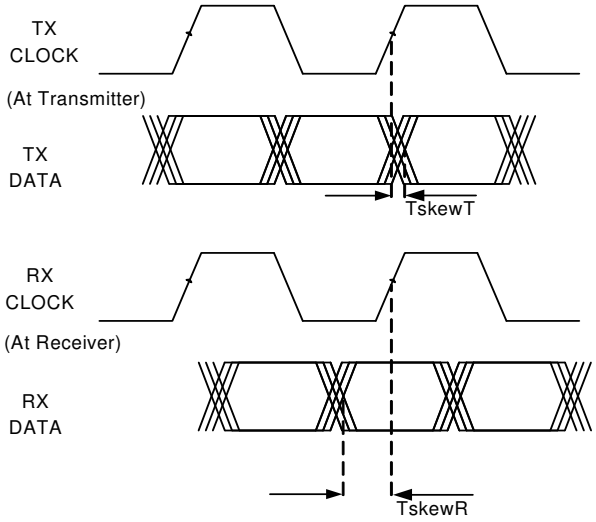
9.5.2.2 RGMII Test Circuit

Figure 5: RGMII Test Circuit



9.5.2.3 RGMII AC Timing Diagram

Figure 6: RGMII AC Timing Diagram



9.5.3 Media Independent Interface (MII) AC Timing

9.5.3.1 MII MAC Mode AC Timing Table

Table 54: MII MAC Mode AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Data input setup relative to RX_CLK rising edge	tSU	3.5	-	ns	-
Data input hold relative to RX_CLK rising edge	tHD	2.0	-	ns	-
Data output delay relative to MII_TX_CLK rising edge	tOV	0.0	10.0	ns	1

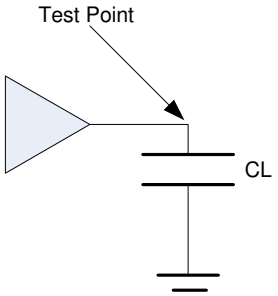
Notes:

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

1. For all signals, the load is CL = 5 pF.

9.5.3.2 MII MAC Mode Test Circuit

Figure 7: MII MAC Mode Test Circuit



9.5.3.3 MII MAC Mode AC Timing Diagrams

Figure 8: MII MAC Mode Output Delay AC Timing Diagram

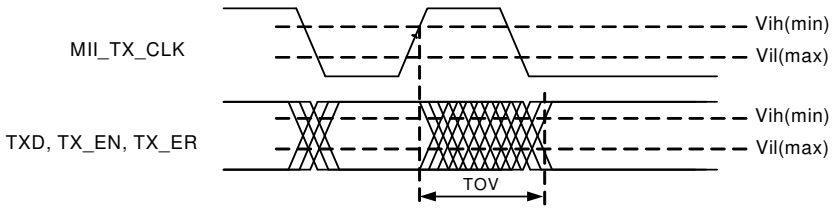
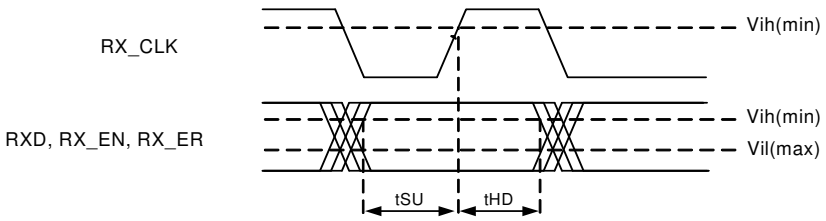


Figure 9: MII MAC Mode Input AC Timing Diagram



9.5.4 Serial Management Interface (SMI) AC Timing

9.5.4.1 SMI AC Timing Table

Table 55: SMI AC Timing Table

Description	Symbol	Min	Max	Units	Notes
MDC clock frequency	fCK	See note 2		MHz	2
MDC clock duty cycle	tDC	0.4	0.6	tCK	-
MDIO input setup time relative to MDC rise time	tSU	12.0	-	ns	-
MDIO input hold time relative to MDC rise time	tHO	0.0	-	ns	3
MDIO output valid before MDC rise time	tOVB	12.0	-	ns	1
MDIO output valid after MDC rise time	tOVA	12.0	-	ns	1

Notes:

General comment: All timing values were measured from VIL(max) and VIH(min) levels, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For all signals, the load is CL = 10 pF.
2. See "Reference Clocks" table for more details.
3. For this parameter, the load is CL = 2 pF.

9.5.4.2 SMI Test Circuit

Figure 10: MDIO Master Mode Test Circuit

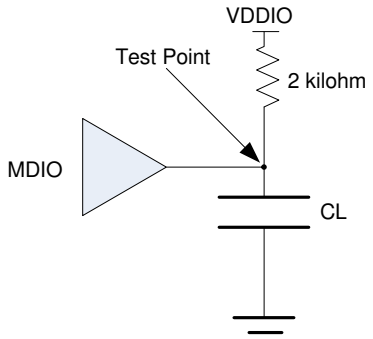
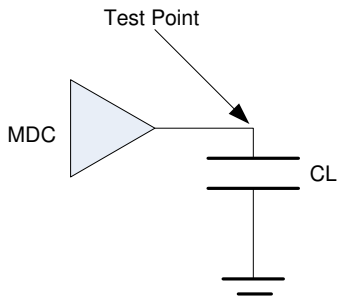


Figure 11: MDC Test Circuit



9.5.4.3 SMI AC Timing Diagrams

Figure 12: SMI Output AC Timing Diagram

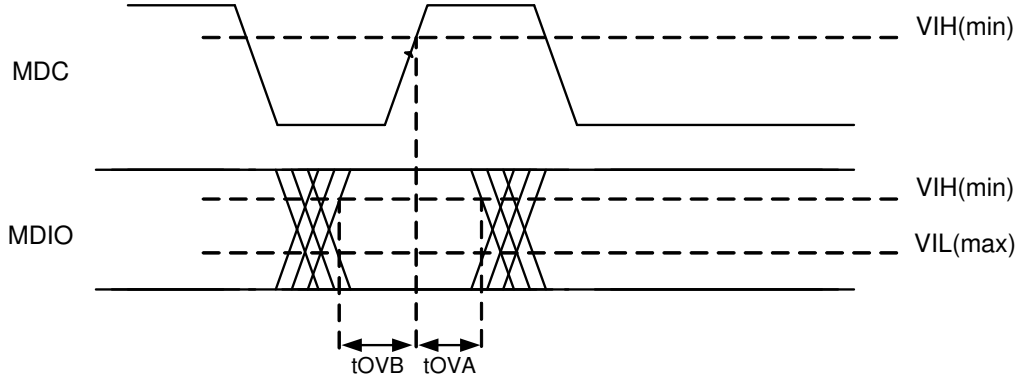
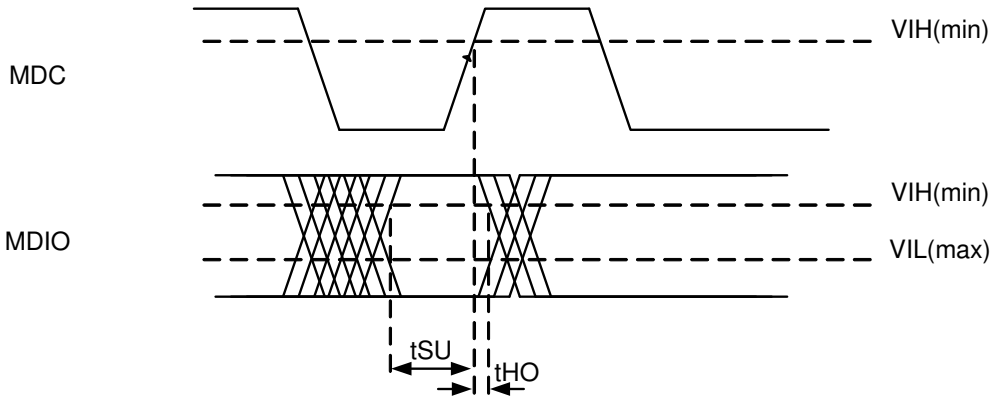


Figure 13: SMI Input AC Timing Diagram



9.5.5 SDRAM DDR3 Interface AC Timing

Note

- The timing values in the following table are based on a tuning algorithm that runs automatically during device initialization. For more information, contact your local Marvell® representative.
- In Table 56, VDDIO represents the VDDO_M pin.

9.5.5.1 SDRAM DDR3 Interface Timing Tables

Table 56: SDRAM DDR3 (800 MHz) Interface AC Timing Table (Represents 2 Banks)

Description	Symbol	800 MHz		Units	Notes
		Min	Max		
Clock frequency	fCK	800		MHz	-
DQ and DM valid output window relative to DQS transition	tDOVW	355	-	ps	-
CLK-CLKn Period Jitter	tJIT(per)	-70	70	ps	1
DQS falling edge setup time to CLK-CLKn rising edge	tDSS	0.32	-	tCK(avg)	-
DQS falling edge hold time from CLK-CLKn rising edge	tDSH	0.32	-	tCK(avg)	-
DQS latching rising transitions to associated clock edges	tDQSS	-0.13	0.13	tCK(avg)	-
Address and Control valid output time before CLK-CLKn rising edge	tAOVB	420	-	ps	2
Address and Control valid output time after CLK-CLKn rising edge	tAOVA	320	-	ps	2
DQ input window time relative to DQS in transition	tDWI	170	-	ps	3, 4

Notes:

General comment: All timing values are defined from VDDIO/2 to VDDIO/2, unless otherwise specified.

General comment: All timing parameters with DQS signal are defined on DQS-DQSn crossing point.

General comment: All timing parameters with CLK signal are defined on CLK-CLKn crossing point.

General comment: For all signals, the load is 50 ohm termination to VDDIO/2.

General comment: tCK = 1/fCK.

1. tJIT(per) = Min/max of {tCKi - tCK where i = 1 to 200}.
2. This timing value is defined when Address and Control signals are configured to output on CLK-CLKn falling edge.
3. All input timing values are defined on silicon I/O cells.
4. Minimum input window mask height is defined as VDDIO/2 +/- 150 mV.

Table 57: Pulse Width Table

Description	Symbol	Min	Max	Units	Notes
DQ and DM output pulse width	tDIPW	0.30	-	tCK(avg)	-
DQS output high pulse width	tDQSH	0.45	0.55	tCK(avg)	-
DQS output low pulse width	tDQSL	0.45	0.55	tCK(avg)	-
DQS write preamble	tWPRE	0.90	-	tCK(avg)	-
DQS write postamble	tWPST	0.30	-	tCK(avg)	-
Address and control output pulse width	tIPW	0.60	-	tCK(avg)	-

Notes:

General comment: All timing values are defined from VREF to VREF, unless otherwise specified.

General comment: tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window.

General comment: All timing parameters with DQS signal are defined on DQS-DQSn crossing point.

Table 58: SDRAM DDR3 Clock Specifications (800 MHz only)

Description	Symbol	Min	Max	Units	Notes
Clock period jitter	tJIT(per)	-70	70	ps	1
Clock perior jitter during DLL locking period	tJIT(per,lck)	-60	60	ps	2
Cycle to cycle clock period jitter	tJIT(cc)	140		ps	3
Cycle to cycle clock period jitter during DLL locking period	tJIT(cc,lck)	120		ps	4
Cumulative error across 2 cycles	tERR(2per)	-103	103	ps	5
Cumulative error across 3 cycles	tERR(3per)	-122	122	ps	5
Cumulative error across 4 cycles	tERR(4per)	-136	136	ps	5
Cumulative error across 5 cycles	tERR(5per)	-147	147	ps	5
Cumulative error across 6 cycles	tERR(6per)	-155	155	ps	5
Cumulative error across 7 cycles	tERR(7per)	-163	163	ps	5
Cumulative error across 8 cycles	tERR(8per)	-169	169	ps	5
Cumulative error across 9 cycles	tERR(9per)	-175	175	ps	5
Cumulative error across 10 cycles	tERR(10per)	-180	180	ps	5
Cumulative error across 11 cycles	tERR(11per)	-184	184	ps	5
Cumulative error across 12 cycles	tERR(12per)	-188	188	ps	5
Cumulative error across n cycles, n=13…50, inclusive	tERR(13-50per)	See note 7		ps	7
Absolute clock period	tCK(abs)	See note 6		ps	6
Absolute clock high pulse width	tCH(abs)	0.43	-	tCK(avg)	-
Absolute clock low pulse width	tCL(abs)	0.43	-	tCK(avg)	-

Notes:

General comment: All timing values are defined on CLK-CLKn crossing point, unless otherwise specified.

1. tJIT(per) is defined as the largest deviation of any single tCK from tCK(avg).
   tJIT(per) = Min/max of {tCKi- tCK(avg) where i=1 to 200}.
   tJIT(per) defines the single period jitter when the DLL is already locked.
2. tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.
3. tJIT(cc) is defined as the difference in clock period between two consecutive clock cycles: tJIT(cc) = Max of |tCKi+1 – tCKi|.
   tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.
4. tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.
5. tERR(nper) is defined as the cumulative error across multiple consecutive cycles from tCK(avg).
   Refer to JEDEC Standard No. 79-3 (DDR3 SDRAM Specification) for more information.
6. tCK(abs),min = tCK(avg),min + tJIT(per),min; tCK(abs),max = tCK(avg),max + tJIT(per),max.
7. tERR(nper),min = (1+0.68ln(n))*tJIT(per)min; tERR(nper),max = (1+0.68ln(n))*tJIT(per)max.

Table 59: SDRAM DDR3 (667 MHz) Interface AC Timing Table (Represents 2 Banks)

Description	Symbol	667 MHz		Units	Notes
		Min	Max		
Clock frequency	fCK	667.0		MHz	-
DQ and DM valid output time before DQS transition	tDOVB	205	-	ps	-
DQ and DM valid output time after DQS transition	tDOVA	190	-	ps	-
CLK-CLKn Period Jitter	tJIT(per)	-80	80	ps	1
DQS falling edge setup time to CLK-CLKn rising edge	tDSS	0.34	-	tCK(avg)	-
DQS falling edge hold time from CLK-CLKn rising edge	tDSH	0.34	-	tCK(avg)	-
DQS latching rising transitions to associated clock edges	tDQSS	-0.11	0.11	tCK(avg)	-
Address and Control valid output time before CLK-CLKn rising edge	tAOVB	440	-	ps	2
Address and Control valid output time after CLK-CLKn rising edge	tAOVA	340	-	ps	2
DQ input setup time relative to DQS in transition	tDSI	-150	-	ps	-
DQ input hold time relative to DQS in transition	tDHI	465	-	ps	-

Notes:

General comment: All timing values are defined from VREF to VREF, unless otherwise specified.

General comment: All input timing values assume a minimum slew rate of 1 V/ns (slew rate defined from VREF +/-100 mV).

General comment: All timing parameters with DQS signal are defined on the DQS-DQSn crossing point.

General comment: All timing parameters with CLK signal are defined on the CLK-CLKn crossing point.

General comment: For all signals, the load is CL = 4 pF.

General comment: tCK = 1/fCK.

1. tJIT(per) = Min/max of {tCKi - tCK where i = 1 to 200}.

2. This timing value is defined when Address and Control signals are output on the CLK-CLKn falling edge.

Table 60: SDRAM DDR3 Clock Specifications (667 MHz only)

Description	Symbol	Min	Max	Units	Notes
Clock period jitter	tJIT(per)	-80	80	ps	1
Clock perior jitter during DLL locking period	tJIT(per,lck)	-70	70	ps	2
Cycle to cycle clock period jitter	tJIT(cc)	160		ps	3
Cycle to cycle clock period jitter during DLL locking period	tJIT(cc,lck)	140		ps	4
Cumulative error across 2 cycles	tERR(2per)	-118	118	ps	5
Cumulative error across 3 cycles	tERR(3per)	-140	140	ps	5
Cumulative error across 4 cycles	tERR(4per)	-155	155	ps	5
Cumulative error across 5 cycles	tERR(5per)	-168	168	ps	5
Cumulative error across 6 cycles	tERR(6per)	-177	177	ps	5
Cumulative error across 7 cycles	tERR(7per)	-186	186	ps	5
Cumulative error across 8 cycles	tERR(8per)	-193	193	ps	5
Cumulative error across 9 cycles	tERR(9per)	-200	200	ps	5
Cumulative error across 10 cycles	tERR(10per)	-205	205	ps	5
Cumulative error across 11 cycles	tERR(11per)	-210	210	ps	5
Cumulative error across 12 cycles	tERR(12per)	-215	215	ps	5
Cumulative error across n cycles, n=13…50, inclusive	tERR(13-50per)	See note 7		ps	7
Absolute clock period	tCK(abs)	See note 6		ps	6
Absolute clock high pulse w idth	tCH(abs)	0.43	-	tCK(avg)	-
Absolute clock low pulse w idth	tCL(abs)	0.43	-	tCK(avg)	-

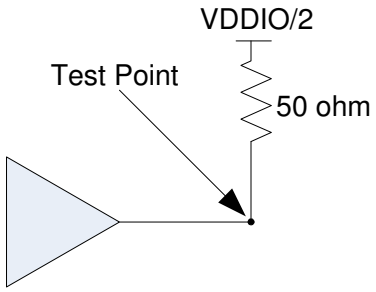
Notes:

General comment: All timing values are defined on CLK-CLKn crossing point, unless otherw ise specified.

1. tJIT(per) is defined as the largest deviation of any single tCK from tCK(avg).
   tJIT(per) = Min/max of {tCKi- tCK(avg) w here i=1 to 200}.
   tJIT(per) defines the single period jitter w hen the DLL is already locked.
2. tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.
3. tJIT(cc) is defined as the difference in clock period betw een tw o consecutive clock cycles: tJIT(cc) = Max of |tCKi+1 – tCKi|.
   tJIT(cc) defines the cycle to cycle jitter w hen the DLL is already locked.
4. tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.
5. tERR(nper) is defined as the cumulative error across multiple consecutive cycles from tCK(avg).
   Refer to JEDEC Standard No. 79-3 (DDR3 SDRAM Specification) for more information.
6. tCK(abs),min = tCK(avg),min + tJIT(per),min; tCK(abs),max = tCK(avg),max + tJIT(per),max.
7. tERR(nper),min = (1+0.68ln(n))*tJIT(per)min; tERR(nper),max = (1+0.68ln(n))*tJIT(per)max.

9.5.5.2 SDRAM DDR3 Interface Test Circuit

Figure 14: SDRAM DDR3 Interface Test Circuit



9.5.5.3 SDRAM DDR3 Interface AC Timing Diagrams

Figure 15: SDRAM DDR3 Interface Write AC Timing Diagram

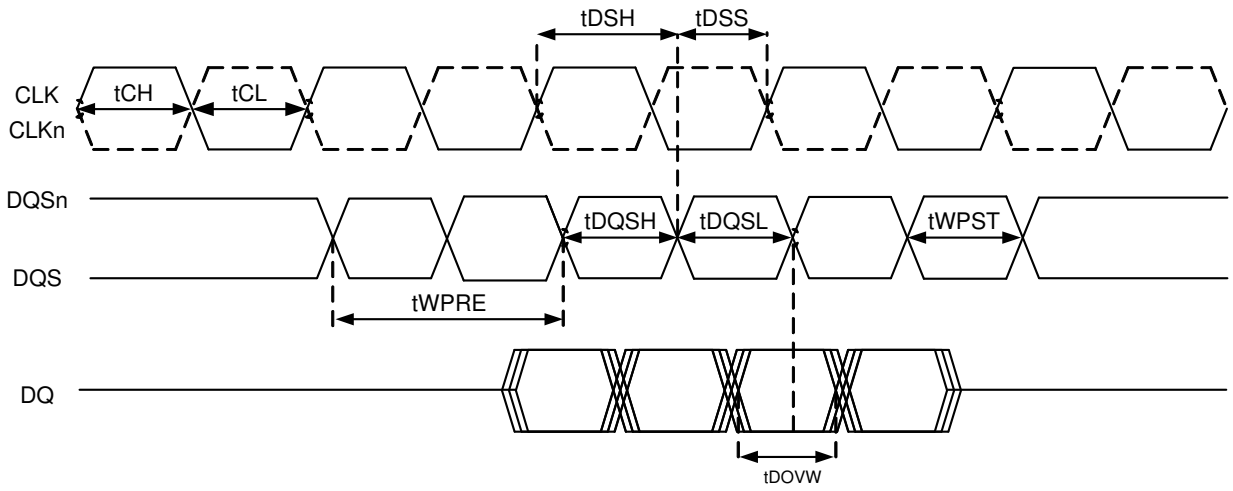


Figure 16: SDRAM DDR3 Interface Write AC Timing Diagram

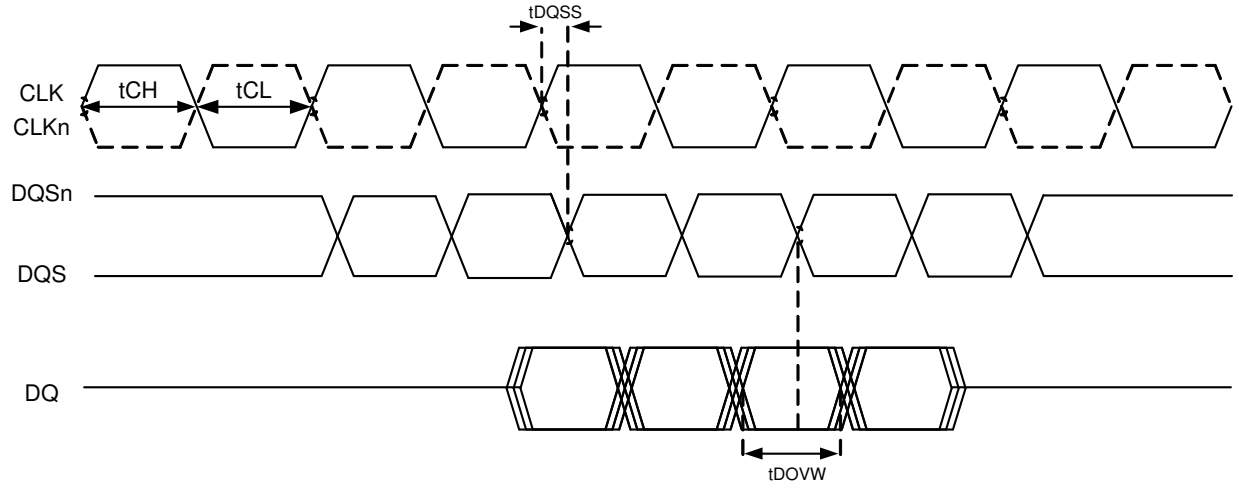


Figure 17: SDRAM DDR3 Interface Address and Control AC Timing Diagram

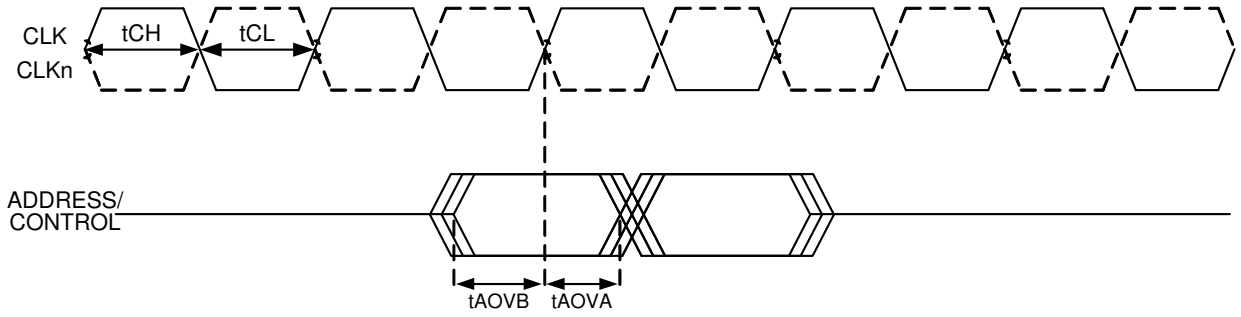
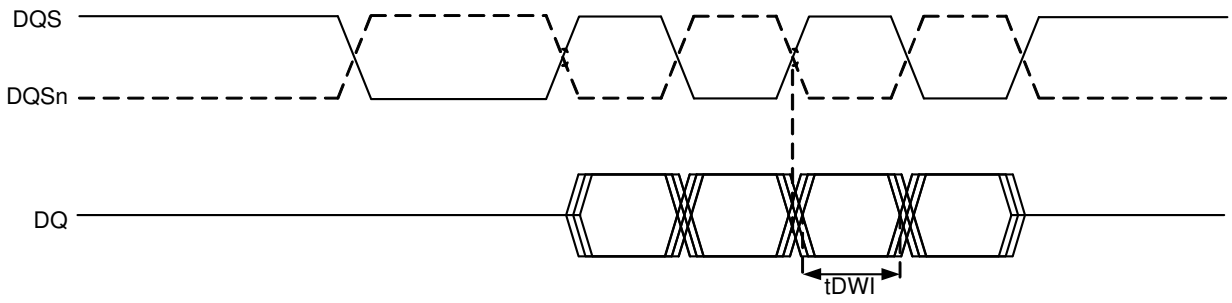


Figure 18: SDRAM DDR3 Interface Read AC Timing Diagram



9.5.6 SDRAM DDR4 Interface AC Timing (Preliminary)

Note

- The timing values in the following table are based on a tuning algorithm that runs automatically during device initialization. For more information, contact your local Marvell® representative.
- In Table 61, VDDIO represents the VDDO_M pin.

9.5.6.1 SDRAM DDR4 Interface Timing Tables

Table 61: SDRAM DDR4 Interface AC Timing Table

Description	Symbol	800 MHz		Units	Notes
		Min	Max		
Clock frequency	fCK	800		MHz	-
DQ and DM valid output window relative to DQS transition	tDOVW	0.5	-	UI	-
DQS falling edge setup time to CLK-CLKn rising edge	tDSS	0.32	-	tCK(avg)	-
DQS falling edge hold time from CLK-CLKn rising edge	tDSH	0.32	-	tCK(avg)	-
DQS latching rising transitions to associated clock edges	tDQSS	-0.13	0.13	tCK(avg)	-
Address and Control valid output time before CLK-CLKn rising edge	tAOVB	315	-	ps	1
Address and Control valid output time after CLK-CLKn rising edge	tAOVA	315	-	ps	1
DQ input window valid time relative to DQS in transition	tDWI	0.3	-	UI	2, 3

Notes:

General comment: All DQ timing values are defined on Vref(avg), unless otherwise specified.

General comment: All CA timing values are defined on VDDIO/2, unless otherwise specified.

General comment: All timing parameters with DQS signal are defined on DQS-DQSn crossing point.

General comment: All timing parameters with CLK signal are defined on CLK-CLKn crossing point.

General comment: For DQ/DQS signals, the load is 50 ohm termination to VDDIO.

General comment: For CA/CLK signals, the load is 50 ohm termination to VDDIO/2.

General comment: tCK = 1/fCK.

General comment: UI = tCK/2.

1. This timing value is defined when Address and Control signals are configured to output on CLK-CLKn falling edge.
2. All input timing values are defined on silicon I/O cells.
3. Minimum input window mask height is defined as 186 mV.

9.5.6.2 SDRAM DDR4 Interface Test Circuit

Figure 19: SDRAM DDR4 Command/Address and Clock Interface Test Circuit

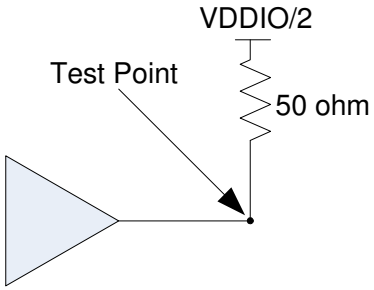
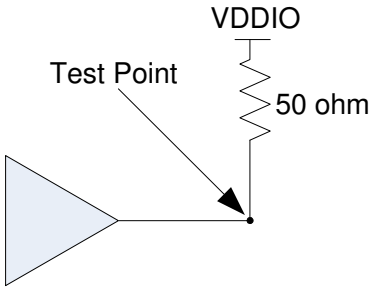


Figure 20: SDRAM DDR4 DQ and DQS Interface Test Circuit



9.5.6.3 SDRAM DDR4 Interface AC Timing Diagrams

Figure 21: SDRAM DDR4 Interface Write AC Timing Diagram

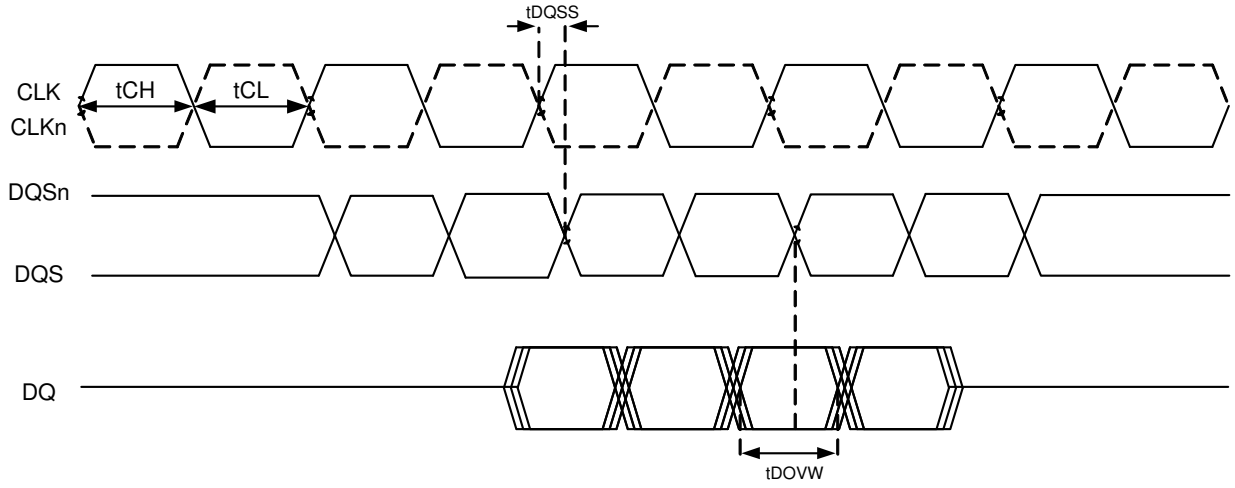


Figure 22: SDRAM DDR4 Interface Address and Control AC Timing Diagram

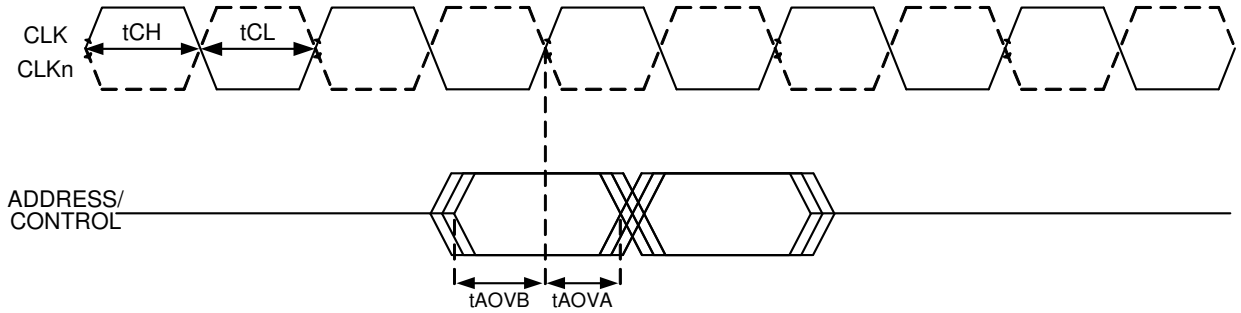
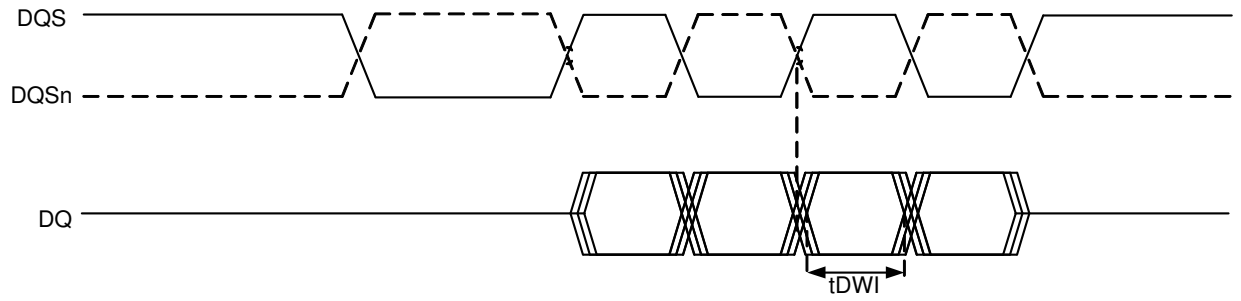


Figure 23: SDRAM DDR4 Interface Read AC Timing Diagram



9.5.7 Secure Digital Input/Output (SDIO) Interface AC Timing

Note

In Table 62, VDDIO represents the VDDIO_SD or VDDO_MMC pins.

9.5.7.1 Secure Digital Input/Output (SDIO) Host AC Timing Table

Table 62: SDIO Host SDR25 AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Clock frequency in Data Transfer Mode	fCK	0	50	MHz	-
Clock high/low level pulse width	tWL/tWH	0.35	-	tCK	1, 3
Clock rise/fall time	tTLH/tTHL	-	3	ns	1, 3
CMD, DAT output valid before CLK rising edge	tDOVB	6.5	-	ns	2, 3
CMD, DAT output valid after CLK rising edge	tDOVA	2.5	-	ns	2, 3
CMD, DAT input setup relative to CLK rising edge	tISU	6	-	ns	2
CMD, DAT input hold relative to CLK rising edge	tIHD	0.0	-	ns	2, 4

Notes:

General comment: tCK = 1/fCK.

1. Defined on VIL(max) and VIH(min) levels.
2. Defined on VDDIO/2 for Clock signal, and VIL(max) / VIH(min) for CMD and DAT signals.
3. For all signals, the load is CL = 10 pF.
4. For this parameter, the load is CL = 2 pF.

Table 63: SDIO Host SDR50 Mode AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Clock frequency in Data Transfer Mode	fCK	0	100	MHz	-
Clock high/low level pulse width	tWL/tWH	0.3	0.7	tCK	1, 3
Clock rise/fall time	tTLH/tTHL	-	0.2	tCK	1, 3
CMD, DAT output valid before CLK rising edge	tDOVB	3.5	-	ns	2, 3
CMD, DAT output valid after CLK rising edge	tDOVA	1.3	-	ns	2, 3
CMD, DAT input setup relative to CLK rising edge	tISU	tCK - 8.3	-	ns	2
CMD, DAT input hold relative to CLK rising edge	tIHD	1.5	-	ns	2, 4

Notes:

General comment: tCK = 1/fCK.

1. Defined on VIL(max) and VIH(min) levels.
2. Defined on VDDIO/2 for Clock signal, and VIL(max) / VIH(min) for CMD and DAT signals.
3. For all signals, the load is CL = 10 pF.
4. For this parameter, the load is CL = 2 pF.

Table 64: SDIO Host SDR12.5 Mode AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Clock frequency in Data Transfer Mode	fCK	0	25	MHz	-
Clock high/low level pulse width	tWL/tWH	0.35	-	tCK	1, 3
Clock rise/fall time	tTLH/tTHL	-	10	ns	1, 3
CMD, DAT output valid before CLK rising edge	tDOVB	6	-	ns	2, 3
CMD, DAT output valid after CLK rising edge	tDOVA	6	-	ns	2, 3
CMD, DAT input setup relative to CLK rising edge	tISU	6	-	ns	2
CMD, DAT input hold relative to CLK rising edge	tIHD	0.0	-	ns	2, 4

Notes:

General comment: tCK = 1/fCK.

1. Defined on VIL(max) and VIH(min) levels.
2. tDOVB & tISU are defined on VIL(max) for Clock signal, and tDOVA & tIHD are defined on VIH(min) for Clock signa
3. For all signals, the load is CL = 10 pF.
4. For this parameter, the load is CL = 2 pF.

Table 65: SDIO Host DDR50 Mode AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Clock frequency in Data Transfer mode	fCK	See note 4		MHz	4
Clock high/low level pulse width	tWL/tWH	0.45	0.55	tCK	1, 2
Clock rise/fall time	tCR/tCF	-	0.2	tCK	1, 2
DAT output valid before CLK transition	tDOVB	3.5	-	ns	1, 2
DAT output valid after CLK transition	tDOVA	1.3	-	ns	1, 2
CMD output valid before CLK rising edge	tCOVB	6.5	-	ns	1, 2
CMD output valid after CLK rising edge	tCOVA	1.3	-	ns	1, 2
DAT input setup relative to CLK transition	tISU	0.45tCK - 7.8	-	ns	1, 2
DAT input hold relative to CLK transition	tIHD	1.5	-	ns	1, 3
CMD input setup relative to CLK rising edge	tICSU	6	-	ns	1, 2
CMD input hold relative to CLK rising edge	tICHD	1.5	-	ns	1, 3

Notes:

General comment: tCK = 1/fCK.

1. Defined on VDDIO/2 for Clock signal, and VIL(max) / VIH(min) for CMD and DAT signals.
2. For all signals, the load is CL = 10 pF.
3. For this parameter, the load is CL = 2 pF.
4. See "Reference Clocks" table for more details.

Table 66: SDIO Host SDR104 Mode AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Clock frequency in Data Transfer Mode	fCK	0	208	MHz	-
Clock high/low level pulse width	tWL/tWH	0.3	0.7	tCK	1, 3
Clock rise/fall time	tTLH/tTHL	-	0.2	tCK	1, 3
CMD, DAT output valid before CLK rising edge	tDOVB	1.9	-	ns	2, 3
CMD, DAT output valid after CLK rising edge	tDOVA	1.3	-	ns	2, 3
CMD, DAT input window relative to CLK rising edge	tIDW	0.54	-	UI	4

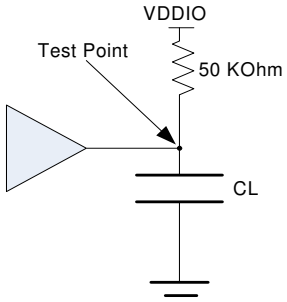
Notes:

General comment: tCK = 1/fCK.

1. Defined on VIL(max) and VIH(min) levels.
2. Defined on VDDIO/2 for Clock signal, and VIL(max) / VIH(min) for CMD and DAT signals.
3. For all signals, the load is CL = 10 pF.
4. Defined after tuning algorithm passed successfully.

9.5.7.2 Secure Digital Input/Output (SDIO) Host Test Circuit

Figure 24: Secure Digital Input/Output (SDIO) Host Test Circuit



9.5.7.3 Secure Digital Input/Output (SDIO) Host AC Timing Diagrams

Figure 25: SDIO Host SDR25/50 Mode Output AC Timing Diagram

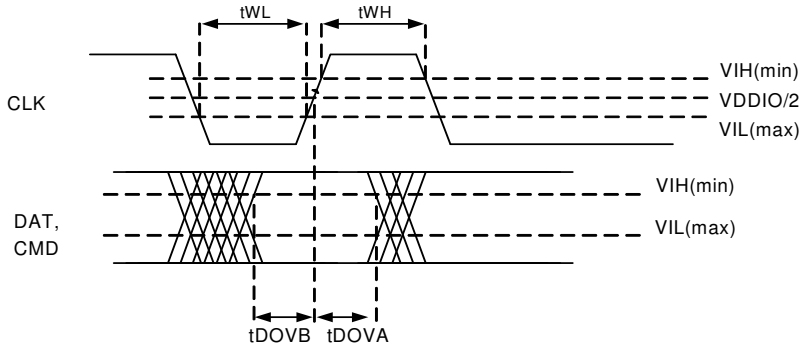


Figure 26: SDIO Host SDR25/50 Mode Input AC Timing Diagram

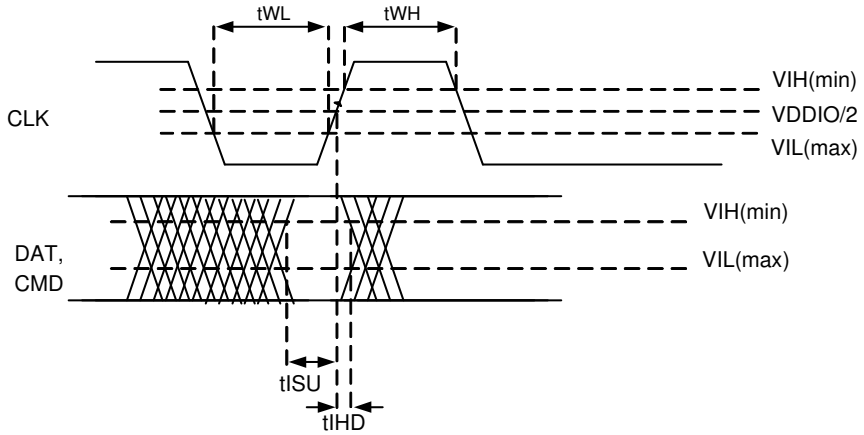


Figure 27: SDIO Host SDR12.5 Mode Output AC Timing Diagram

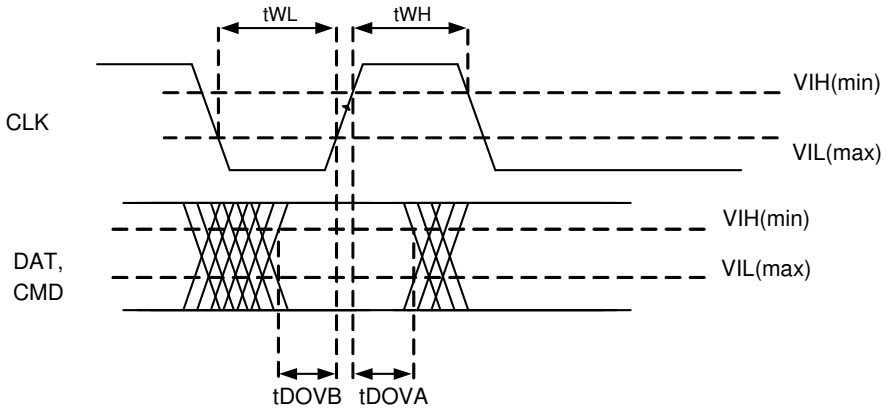


Figure 28: SDIO Host SDR12.5 Mode Input AC Timing Diagram

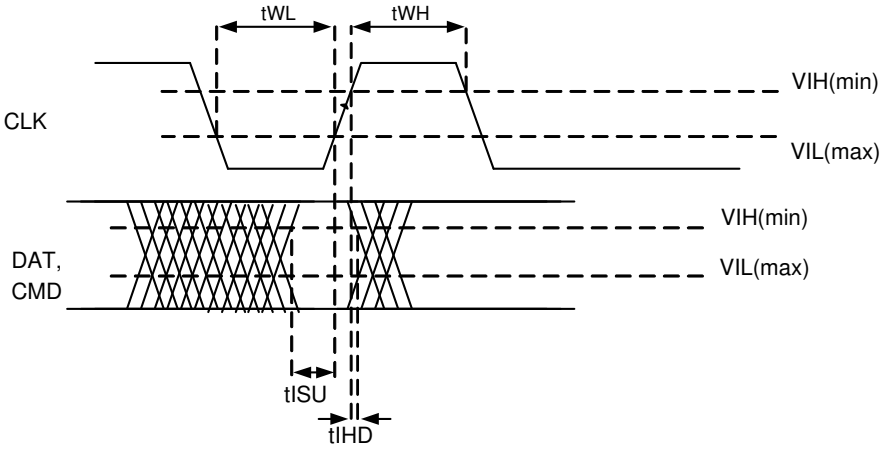


Figure 29: SDIO Host DDR50 Output AC Timing Diagram

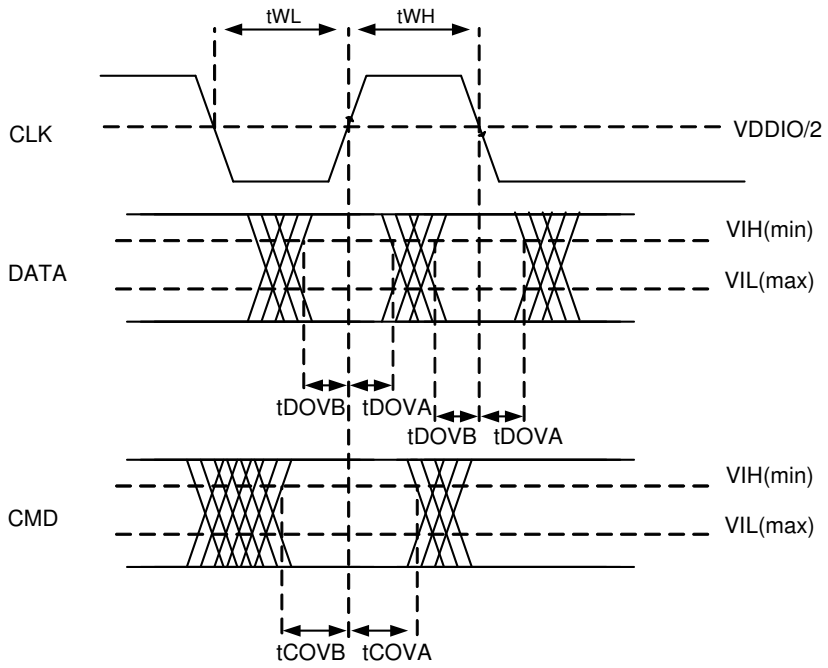


Figure 30: SDIO Host DDR50 Input AC Timing Diagram

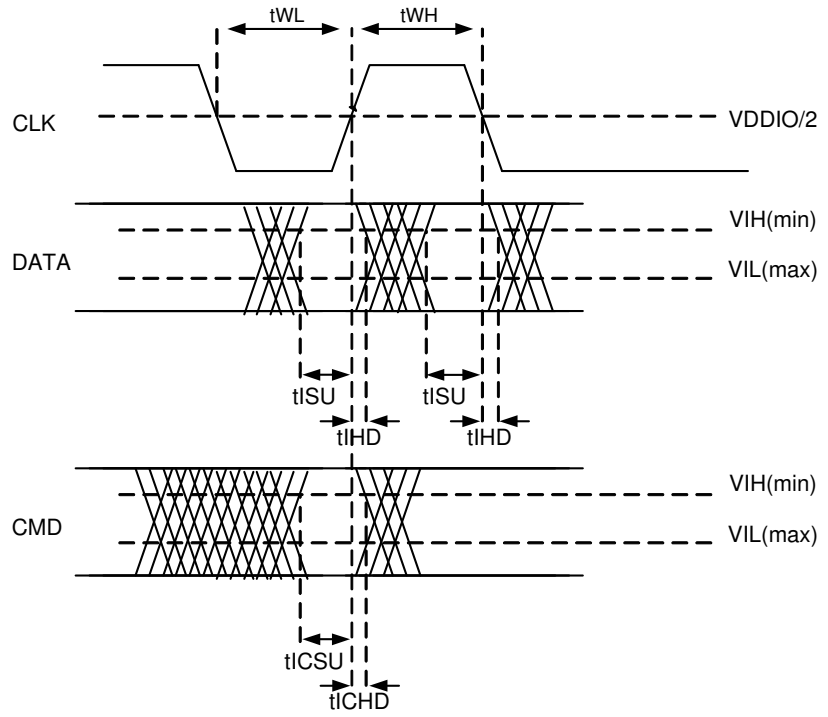
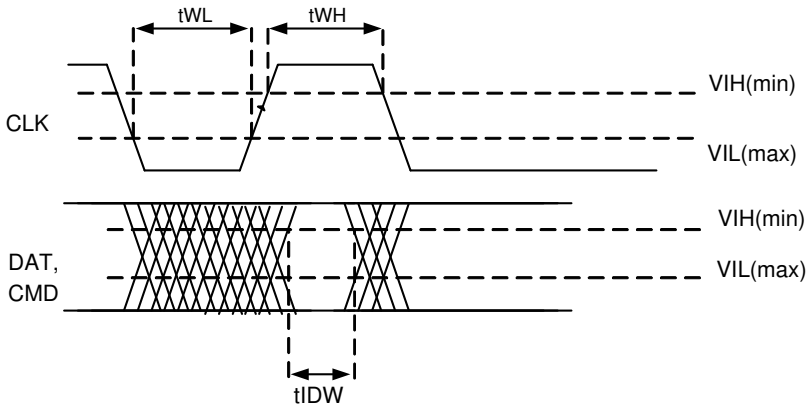


Figure 31: SDIO Host SDR104 Mode Input AC Timing Diagram



9.5.8 Serial Peripheral Interface (SPI) AC Timing

Note

In Table 67, VDDIO represents the VDDO_PIO pins.

9.5.8.1 SPI AC Timing Table

Table 67: SPI AC Timing Table

Description	Symbol	SPI		Units	Notes
		Min	Max		
SCLK clock frequency	fCK	See Note 3		MHz	3
SCLK high time	tCH	0.46	-	tCK	1, 2
SCLK low time	tCL	0.46	-	tCK	1, 2
SCLK slew rate	tSR	0.5	-	V/ns	1
Data out valid relative to SCLK falling edge	tDOV	-2.5	2.5	ns	1
CS active before first SCLK rising edge	tCSB	0.4	-	tCK	1, 4
CS not active after SCLK rising edge	tCSA	0.4	-	tCK	1, 4
Data in setup time relative to SCLK rising edge	tSU	0.2	-	tCK	2
Data in hold time relative to SCLK rising edge	tHD	5.0	-	ns	2

Notes:

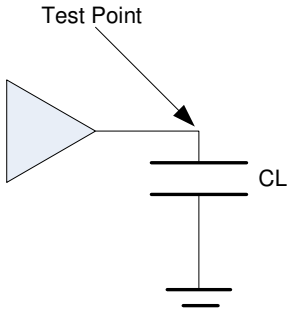
General comment: All values were measured from 0.3*vddio to 0.7*vddio, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For all signals, the load is CL = 10 pF.
2. Defined from vddio/2 to vddio/2.
3. See "Reference Clocks" table for more details.
4. When working with CPOL=1 mode, the CS is relative to first SCLK falling edge.

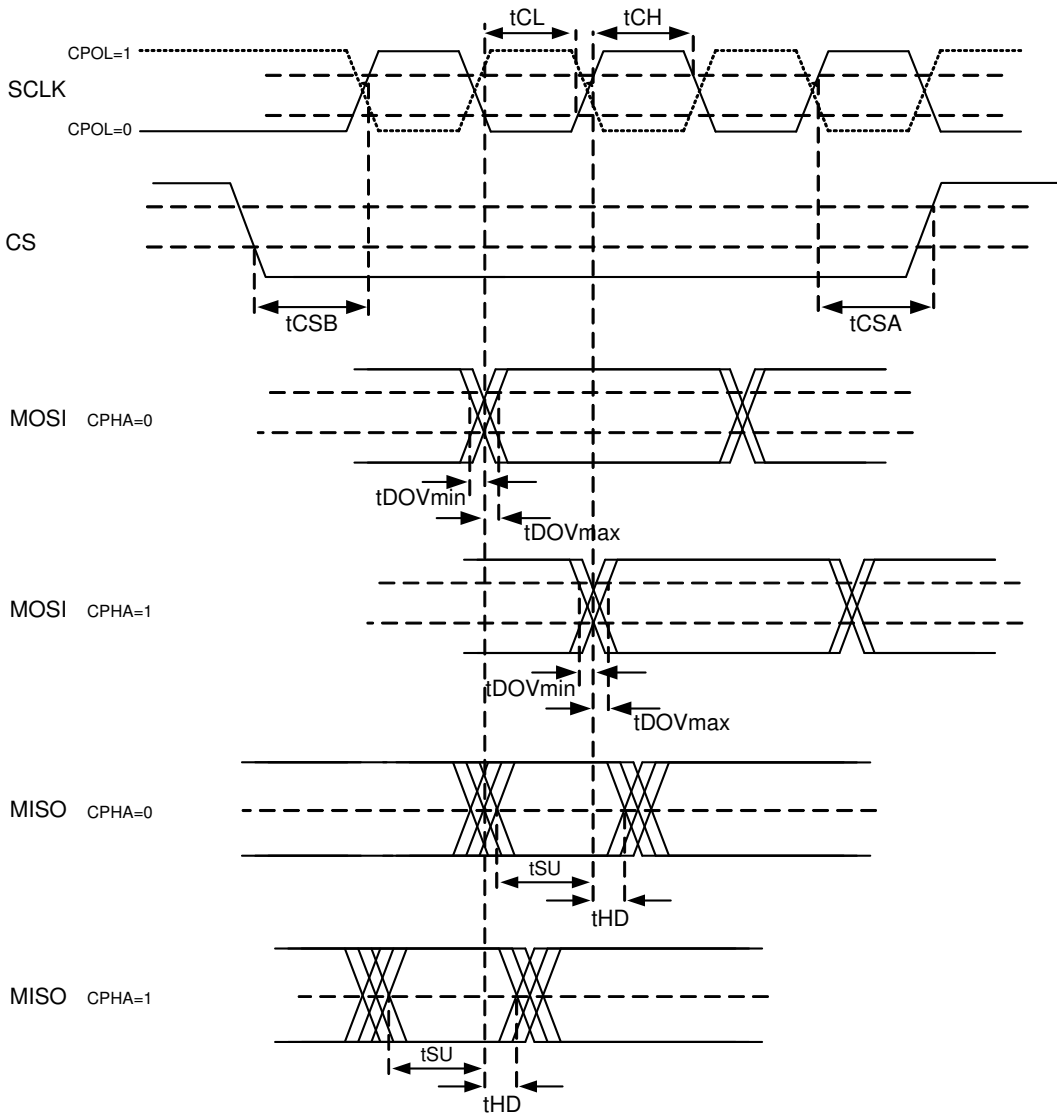
9.5.8.2 SPI (Master Mode) Test Circuit

Figure 32: SPI (Master Mode) Test Circuit



9.5.8.3 SPI (Master Mode) Timing Diagrams

Figure 33: SPI (Master Mode) AC Timing Diagram



9.5.9 Inter-integrated Circuit Interface (I^2C) AC Timing

9.5.9.1 I^2C AC Timing Table

Note The symbol tSU refers to tSU;DA. The symbol tHD refers to tHD;DAT.

Table 68: I^2C Master AC Timing Table Standard Mode (100 kHz)

Description	Symbol	Min	Max	Units	Notes
SCK clock frequency	fCK	See note 1		kHz	1
SCK minimum low level width	tLOW	0.47	-	tCK	2
SCK minimum high level width	tHIGH	0.40	-	tCK	2
SDA input setup time relative to SCK rising edge	tSU	250.0	-	ns	-
SDA input hold time relative to SCK falling edge	tHD	0.0	-	ns	4
SDA and SCK rise time	tr	-	1000	ns	2, 3
SDA and SCK fall time	tf	-	300	ns	2, 3
SDA output delay relative to SCK falling edge	tOV	0.0	0.4	tCK	2

Notes:

General comment: All values referred to VIH(min) and VIL(max) levels, unless otherwise specified.

General comment: tCK = 1/fCK.

1. See "Reference Clocks" table for more details.
2. For all signals, the load is CL = 100 pF, and RL value can be 500 ohm to 8 kilohm.
3. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).
4. For this parameter, the load is CL = 10 pF.

Table 69: I²C Slave AC Timing Table Standard Mode (100 kHz)

Description	Symbol	100 kHz (Max)		Units	Notes
		Min	Max		
SCK minimum low level width	tLOW	4.7	-	us	1
SCK minimum high level width	tHIGH	4.0	-	us	1
SDA input setup time relative to SCK rising edge	tSU	250.0	-	ns	-
SDA input hold time relative to SCK falling edge	tHD	0.0	-	ns	-
SDA and SCK rise time	tr	-	1000.0	ns	1, 2
SDA and SCK fall time	tf	-	300.0	ns	1, 2
SDA output delay relative to SCK falling edge	tOV	0.0	4.0	us	1

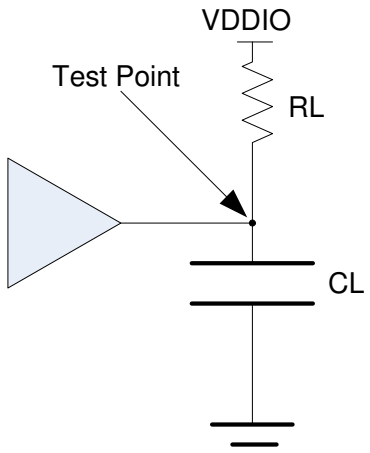
Notes:

General comment: All values referred to VIH(min) and VIL(max) levels, unless otherwise specified.

1. For all signals, the load is CL = 100 pF, and RL value can be 500 ohm to 8 kilohm.
2. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).

9.5.9.2 I²C Test Circuit

Figure 34: I²C Test Circuit



9.5.9.3 I²C AC Timing Diagrams

Figure 35: I²C Output Delay AC Timing Diagram

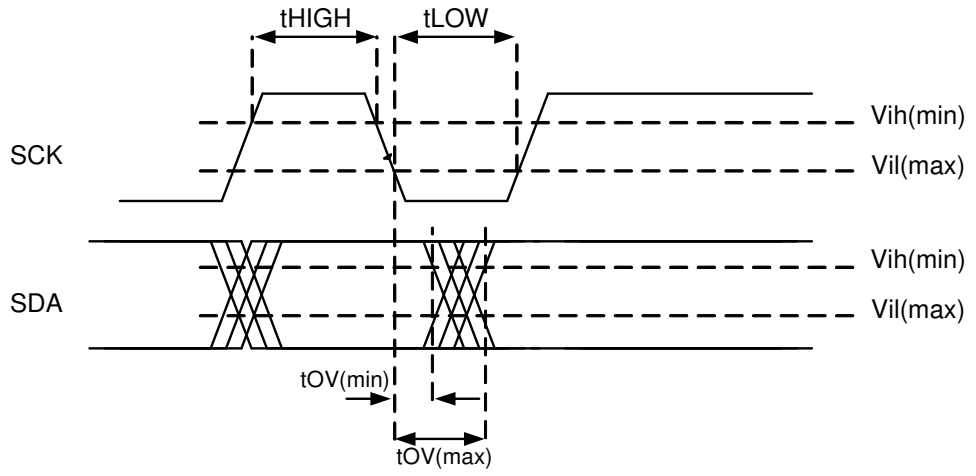
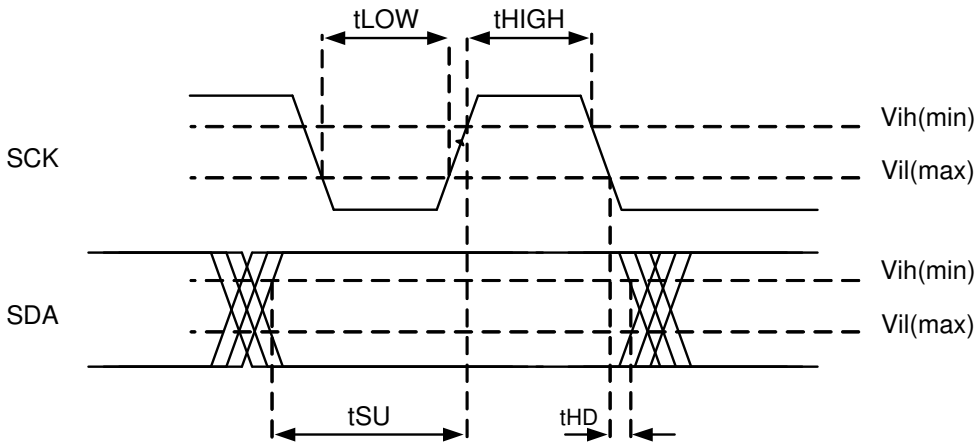


Figure 36: I²C Input AC Timing Diagram



9.5.10 JTAG Interface AC Timing

Note

In Table 70, VDDIO represents the VDDO_JIO pins.

9.5.10.1 JTAG Interface AC Timing Table

Table 70: JTAG Interface AC Timing Table

Description	Symbol	Min	Max	Units	Notes
JTClk frequency	fCK	See Note 3		MHz	-
JTClk minimum pulse width	Tpw	0.45	0.55	tCK	-
JTClk rise/fall slew rate	Sr/Sf	0.5	-	V/ns	2
JTRSTn active time	Trst	1.0	-	ms	-
TMS, TDI input setup relative to JTClk rising edge	Tsetup	0.2*tCK	-	ns	-
TMS, TDI input hold relative to JTClk rising edge	Thold	0.4*tCK	-	ns	-
JTClk falling edge to TDO output delay	Tprop	1.0	0.25*tCK	ns	1

Notes:

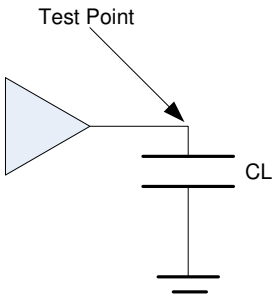
General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For TDO signal, the load is CL = 10 pF.
2. Defined from VIL to VIH for rise time, and from VIH to VIL for fall time.
3. See "Reference Clocks" table for more details.

9.5.10.2 JTAG Interface Test Circuit

Figure 37: JTAG Interface Test Circuit



9.5.10.3 JTAG Interface AC Timing Diagrams

Figure 38: JTAG Interface Output Delay AC Timing Diagram

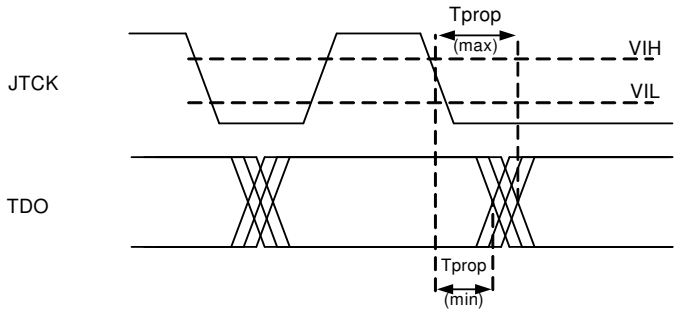
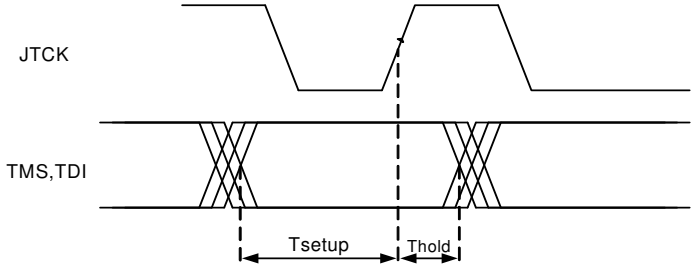


Figure 39: JTAG Interface Input AC Timing Diagram



9.5.11 Multi Media Card (MMC) Interface AC Timing

Note

In Table 71, VDDIO represents the VDDO_MMC pins.

9.5.11.1 MMC AC Timing Table

Table 71: MMC High-Speed Host AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Clock frequency in Data Transfer mode	fCK	See note 5		MHz	5
Clock high/low level pulse width	tWL/tWH	0.34	-	tCK	1, 3
Clock rise/fall time	tTLH/tTHL	-	3.0	ns	1, 3
CMD, DAT output valid before CLK rising edge	tDOVB	3.5	-	ns	2, 3
CMD, DAT output valid after CLK rising edge	tDOVA	3.5	-	ns	2, 3
CMD, DAT input setup relative to CLK rising edge	tISU	6.5	-	ns	2
CMD, DAT input hold relative to CLK rising edge	tIHD	0.0	-	ns	2, 4

Notes:

General comment: tCK = 1/fCK.

1. Defined on VIL(max) and VIH(min) levels.
2. Defined on VDDIO/2 for Clock signal, and VIL(max) / VIH(min) for CMD and DAT signals.
3. For all signals, the load is CL = 10 pF.
4. For this parameter, the load is CL = 2 pF.
5. See "Reference Clocks" table for more details.

Table 72: MMC DDR Host AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Clock frequency in Data Transfer mode	fCK	See note 4		MHz	4
Clock high/low level pulse width	tWL/tWH	0.45	0.55	tCK	1, 2, 5
DAT output valid before CLK transition	tDOVB	3.0	-	ns	1, 2
DAT output valid after CLK transition	tDOVA	3.0	-	ns	1, 2
CMD output valid before CLK rising edge	tCOVB	3.5	-	ns	1, 2
CMD output valid after CLK rising edge	tCOVA	3.5	-	ns	1, 2
DAT input setup relative to CLK transition	tISU	0.45tCK - 7.8	-	ns	1, 2
DAT input hold relative to CLK transition	tIHD	1.5	-	ns	1, 3
CMD input setup relative to CLK rising edge	tICSU	6.5	-	ns	1, 2
CMD input hold relative to CLK rising edge	tICHD	0.5	-	ns	1, 3

Notes:

General comment: tCK = 1/fCK.

1. Defined on VDDIO/2 for Clock signal, and VIL(max) / VIH(min) for CMD and DAT signals.
2. For all signals, the load is CL = 10 pF.
3. For this parameter, the clock load is CL = 2 pF.
4. See "Reference Clocks" table for more details.

Table 73: MMC High-Speed 200 (HS200) Host AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Clock frequency in Data Transfer mode	fCK	See note 5		MHz	5
Clock high/low level pulse width	tWL/tWH	0.3	-	tCK	1, 3
Clock rise/fall time	tTLH/tTHL	-	0.2*tCK	ns	1, 3
CMD, DAT output valid before CLK rising edge	tDOVB	1.9	-	ns	2, 3
CMD, DAT output valid after CLK rising edge	tDOVA	1.3	-	ns	2, 3
CMD, DAT input window relative to CLK rising edge	tIDW	0.517	-	tCK	2, 4

Notes:

General comment: tCK = 1/fCK.

1. Defined on VIL(max) and VIH(min) levels.
2. Defined on VDDIO/2 for Clock signal, and VIL(max) / VIH(min) for CMD and DAT signals.
3. For all signals, the load is CL = 10 pF.
4. For this parameter, the load is CL = 2 pF.
5. See "Reference Clocks" table for more details.

Table 74: MMC High-Speed Host (HS400) AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Clock frequency in Data Transfer mode	fCK	See note 4		MHz	4
Clock high/low level pulse width	tWL/tWH	0.46	0.54	tCK	1, 2, 3
DAT output valid before CLK transition	tDOVB	0.5	-	ns	1, 2
DAT output valid after CLK transition	tDOVA	0.5	-	ns	1, 2
CMD output valid before CLK rising edge	tCOVB	1.9	-	ns	1, 2
CMD output valid after CLK rising edge	tCOVA	1.3	-	ns	1, 2
DAT input setup relative to Data Strobe transition	tISU	-0.7	-	ns	1
DAT input hold relative to Data Strobe transition	tIHD	1.3	-	ns	1
CMD input setup relative to Data Strobe rising edge	tICSU	-1.2	-	ns	1
CMD input hold relative to Data Strobe rising edge	tICHD	3.8	-	ns	1

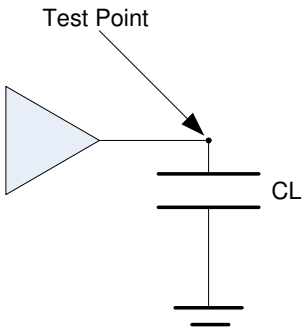
Notes:

General comment: tCK = 1/fCK.

1. Defined on VDDIO/2 for Clock signal, and VIL(max) / VIH(min) for CMD and DAT signals.
2. For all signals, the load is CL = 5 pF.
3. This parameter includes jitter and phase noise.
4. See "Reference Clocks" table for more details.

9.5.11.2 MMC Test Circuit

Figure 40: MMC Test Circuit



9.5.11.3 MMC AC Timing Diagrams

Figure 41: MMC High-Speed Host Output AC Timing Diagram

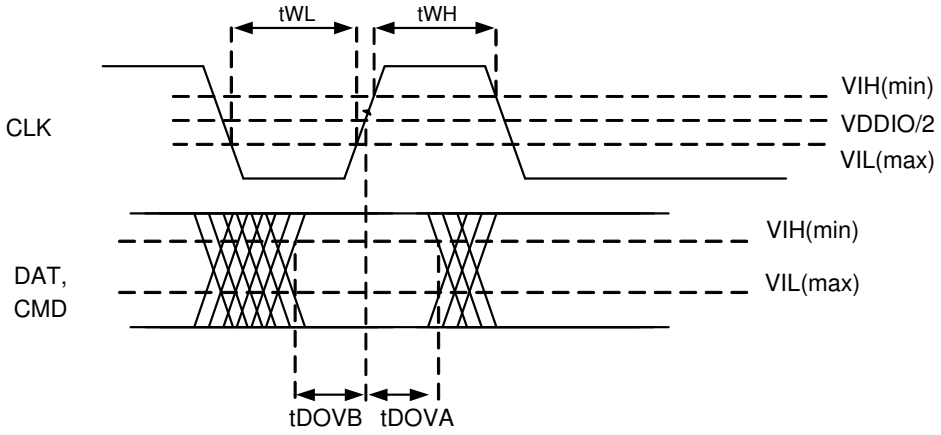


Figure 42: MMC High-Speed Host Input AC Timing Diagram

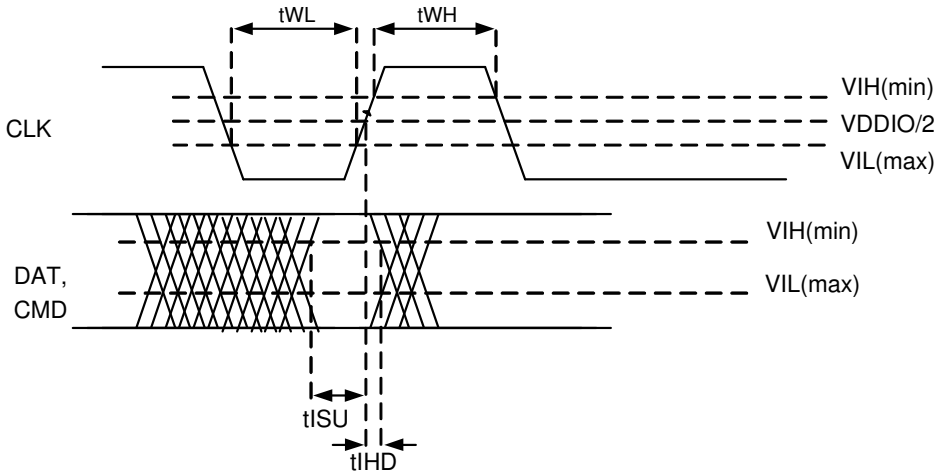


Figure 43: MMC DDR Host Output AC Timing Diagram

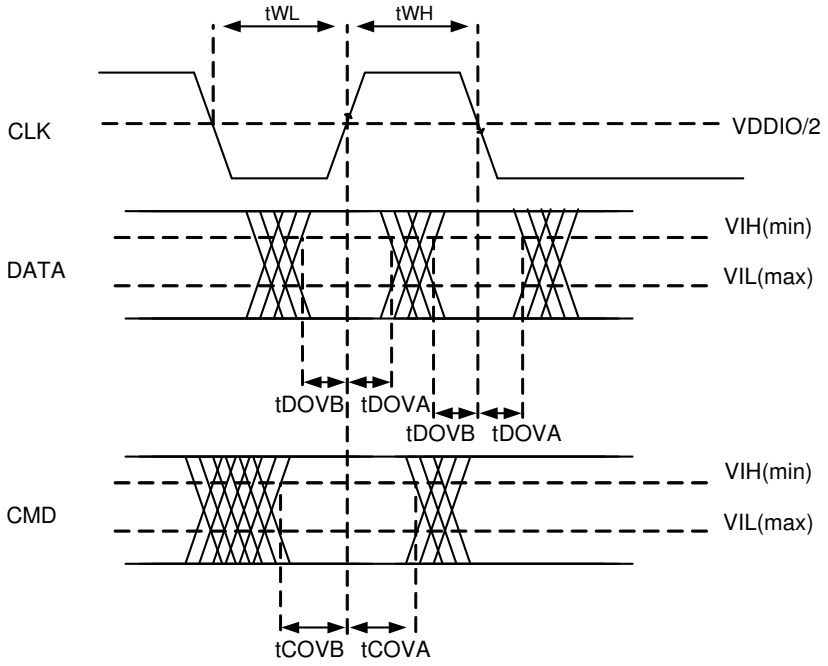
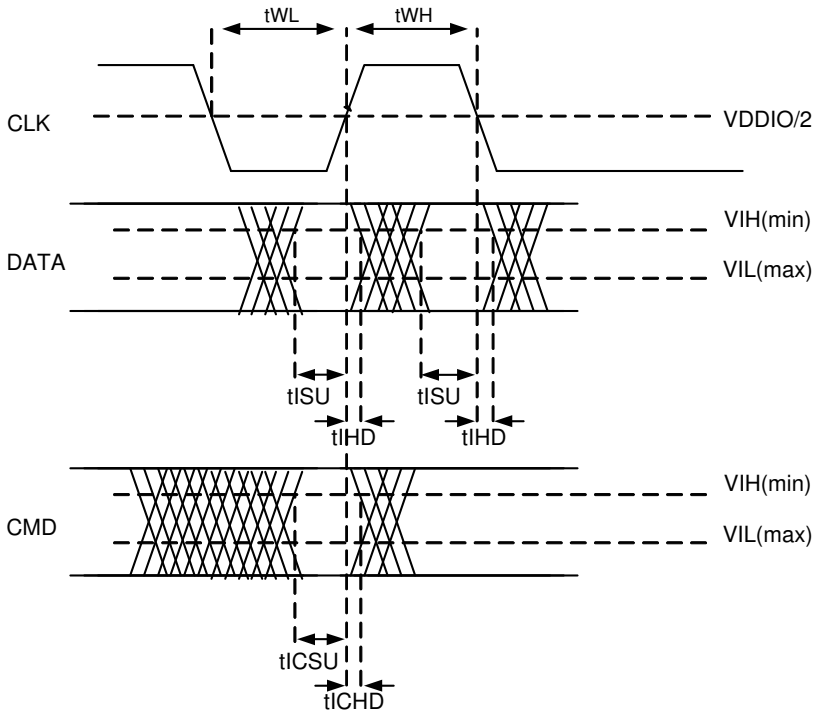


Figure 44: MMC DDR Host Input AC Timing Diagram



9.6 Differential Interface Electrical Characteristics

This section provides the reference clock, AC, and DC characteristics for the differential interfaces:

Note The Tx and Rx timing parameters are defined with the relevant reference clock specifications as specified in the Hardware Specifications.

9.6.1 Differential Reference Clock Characteristics

9.6.1.1 PCIe Interface Differential Reference Clock Characteristics

Note

- Table 75 is relevant to PCIe_CLK_P/N.
- The maximum allowed single ended voltage in the input mode must not be above the SRD2_AVDD18 power rail.

Table 75: PCIe Interface Differential Reference Clock Characteristics

Description	Symbol	Min	Max	Units	Notes
Clock frequency	fCK	100		MHz	-
Clock duty cycle	DCrefclk	0.4	0.6	tCK	-
Differential rising/falling slew rate	SRrefclk	0.6	4	V/ns	3
Differential high voltage	VIHrefclk	150	-	mV	-
Differential low voltage	VILrefclk	-	-150	mV	-
Absolute crossing point voltage	Vcross	250	550	mV	1
Variation of Vcross over all rising clock edges	Vcrs_dlta	-	140	mV	1
Rise-Fall matching	dTRrefclk	-	20	%	1
Average differential clock period accuracy	Tperavg	-300	2800	ppm	4
Absolute differential clock period	Tperabs	9.8	10.2	ns	2
Differential clock cycle-to-cycle jitter	Tccjit	-	150	ps	-
Clock high frequency RMS jitter	Thfrms	-	3.1	ps RMS	5
Clock low frequency RMS jitter	Tlfrms	-	3	ps RMS	5

Notes:

General Comment: The reference clock timings are based on 100 ohm test circuit.

General Comment: Refer to the PCI Express Card Electromechanical Specification, Revision 2.0, April 2007, section 2.1.3 for more information.

1. Defined on a single-ended signal.
2. Including jitter and spread spectrum.
3. Defined from -150 mV to +150 mV on the differential waveform.
4. Max value is defined with SSC. Without SSC the value is 300 ppm.
5. Defined according to section 4.3.7 "Reference Clock Specification" in PCI Express Base Specification Revision 2.1 standard.

PCIe Interface Spread Spectrum Requirements

Table 76: PCIe Interface Spread Spectrum Requirements

Symbol	Min	Max	Units	Notes
Fmod	0.0	33.0	kHz	1
Fspread	-0.5	0.0	%	1

Notes:
1. Defined on linear sweep or “Hershey’s Kiss” (US Patent 5,631,920) modulations.

9.6.2 High Speed SGMII (HS-SGMII) Electrical Characteristics

9.6.2.1 HS-SGMII Short Reach (SR) Driver and Receiver Characteristics

Table 77: HS-SGMII Short Reach (SR) Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud Rate	BR	3.125		Gbps	-
Baud rate tolerance	Bppm	-100	100	ppm	1
Unit Interval	UI	320		ps	-
Driver parameters					
Output differential minimum eye opening	Vodppe	800	-	mV	-
Output differential maximum peak-to-peak	Vodpp	-	1600	mV	-
Absolute output limits	Vos	-0.4	2.3	V	-
Output differential skew	Tosk	-	15	ps	2
Output differential transition time	Tr/Tf	-	130	ps	3
Return loss differential output	RLOD	10	-	dB	4
Output jitter - Deterministic, peak-to-peak	Jttx	-	0.17	UI	-
Output jitter - Total, peak-to-peak	Jttxpp	-	0.35	UI	5, 8
Receiver parameters					
Input differential sensitivity	Vidpps	200	-	mV	9
Input differential voltage	Vidpp	-	1600	mV	9
Input differential skew	Tisk	-	75	ps	6
Return loss differential input	RLID	10	-	dB	7
Return loss common mode input	RLIC	6	-	dB	7
Input jitter - Deterministic, peak-to-peak	Jtrx	-	0.47	UI	10
Input jitter - Sinusoidal, low frequency	Jtrlsx	-	8.5	UI	11
Input jitter - Sinusoidal, high frequency	Jtrsx	-	0.1	UI	12
Input jitter - Total, peak-to-peak	Jtrxpp	-	0.65	UI	5, 8

Notes:

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

1. Defines the allowable reference clock difference from nominal.
2. This is a single ended parameter and is defined at the 50% point on the signal swing.
3. Defined from 20% to 80% of the signal's voltage levels.
4. Defined from 312.5 MHz to 625 MHz.
5. Defined with a BER of 10^-12.
6. This value assumes total eye jitter budget is still maintained.
7. Relative to 100 ohm differential and 25 ohm common mode. Defined from 100 MHz to 2.5 GHz.
   Return loss includes contributions from on-chip circuitry, chip packaging,
   and off-chip optimized components related to the driver/receiver breakout.
8. Total jitter is composed of both deterministic and random components.
   The allowed random jitter equals the allowed total jitter minus the actual deterministic at that point.
9. Vidpps refers to the internal eye opening while Vidpp refers to the peak-to-peak.
10. Deterministic jitter includes sinusoidal, high frequency (Jtrsx), component.
11. Defined below 22.1 kHz.
12. Defined from 1.875 MHz to 20 MHz.

9.6.2.2 HS-SGMII Driver Output Waveforms

Table 78: HS-SGMII/XAUI Settings and Configuration

Parameter	Setting/Configuration
Vodppe	The Vodppe is the output differential minimum eye opening.
NOTE: For further information, refer to the Functional Specifications.	

Figure 45: HS-SGMII Driver Output Voltage Limits and Definitions

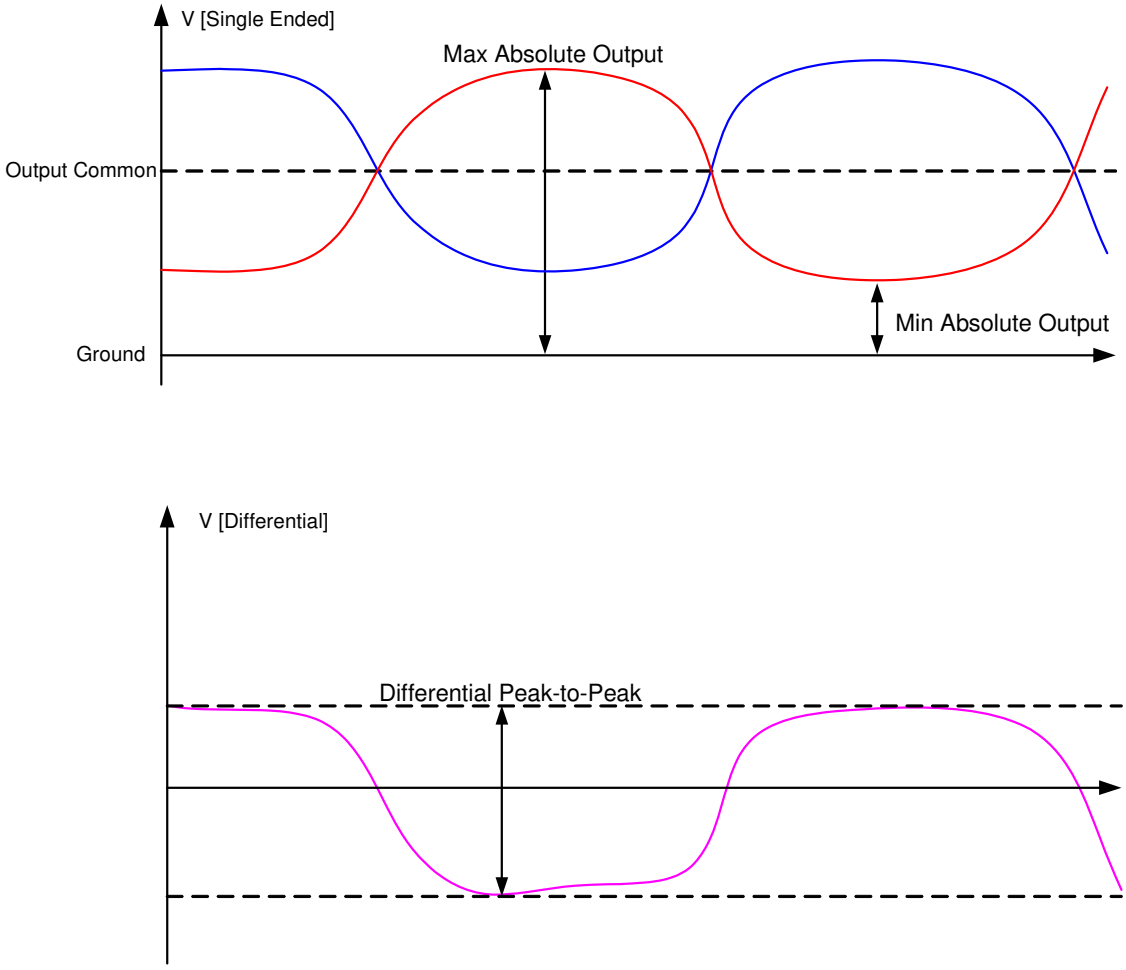


Figure 46: HS-SGMII Driver Output Differential Voltage under Pre-emphasis

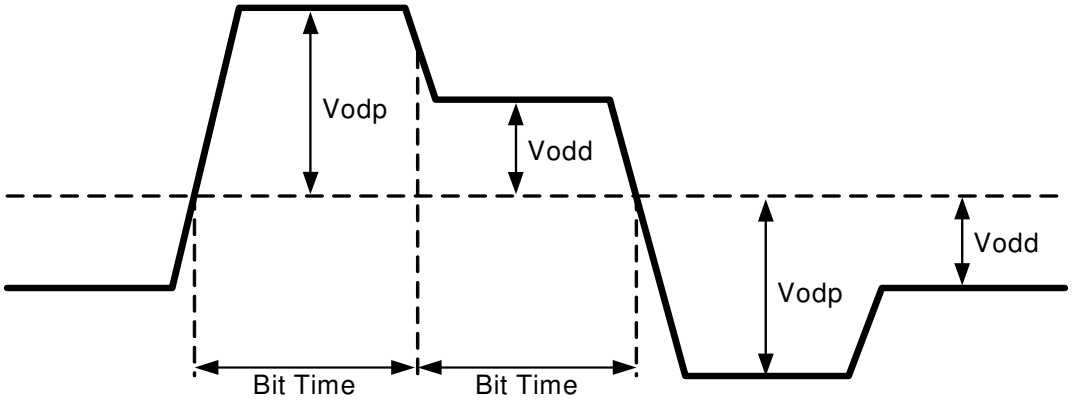
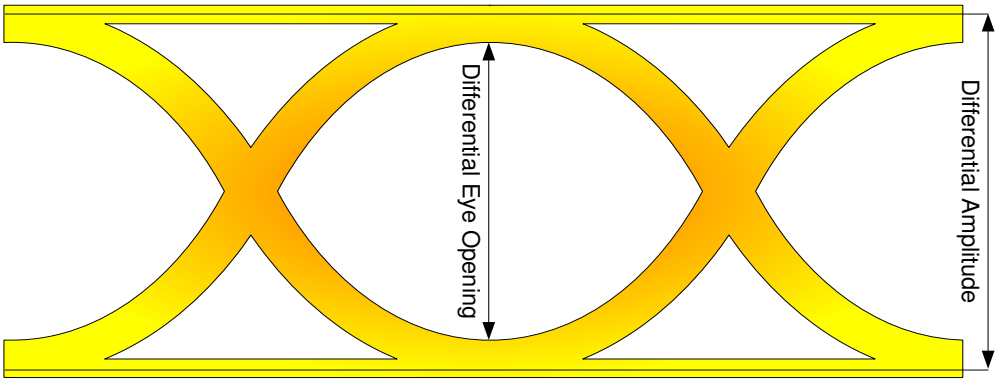


Figure 47: HS-SGMII Driver Output Differential Amplitude and Eye Opening



9.6.3 SGMII Interface Electrical Characteristics

9.6.3.1 SGMII Driver and Receiver Characteristics

Table 79: SGMII Interface Driver and Receiver Characteristics (1000BASE-X)

Description	Symbol	Min	Max	Units	Notes
Baud rate	BR	1.25		Gbps	-
Baud rate tolerance	Bppm	-100	100	ppm	1
Unit interval	UI	800		ps	-
Driver parameters for 1000BASE-X Backplane Mode					
Output differential minimum eye opening	Vodppe	850	-	mV	-
Output differential maximum peak-to-peak	Vodpp	-	1350	mV	-
Absolute output limits	Vos	-0.4	1.6	V	-
Output differential skew	Tosk	-	20	ps	2
Return loss differential output	RLOD	10	-	dB	3, 9
Output jitter - deterministic, peak-to-peak	Jttx	-	0.1	UI	4
Output jitter - total, peak-to-peak	Jttxpp	-	0.24	UI	6
Receiver parameters for 1000BASE-X Backplane Mode					
Input differential sensitivity	Vidppe	180	-	mV	8
Input differential voltage	Vidpp	-	2000	mV	8
Input differential skew	Tisk	-	180	ps	5
Return loss differential input	RLID	10	-	dB	3, 9
Return loss common mode input	RLIC	6	-	dB	7, 9
Input jitter - deterministic, peak-to-peak	Jtrx	-	0.462	UI	4
Input jitter - total, peak-to-peak	Jtrxpp	-	0.749	UI	6

Notes:

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

1. Defines the allowable reference clock difference from nominal.
2. This is a single ended parameter and is defined at the 50% point on the signal swing.
3. Defined from 50 MHz to 625 MHz.
   For 650 MHz - 1.25 GHz: -10dB+10log(Freq/625) (Freq defined in MHz).
4. Jitter specifications include all but 10^-12 of the jitter population.
5. This value assumes total eye jitter budget is still maintained.
6. Total jitter is composed of both deterministic and random components.
   The allowed random jitter equals the allowed total jitter minus the actual deterministic at that point.
7. Defined from 50 MHz to 625 MHz.
   For 650 MHz - 1.25 GHz: -6dB+10log(Freq/625) (Freq defined in MHz).
8. Vidppe refers to the internal eye opening while Vidpp refers to the peak-to-peak.
9. Return loss includes contributions from on-chip circuitry, chip packaging,
   and off-chip optimized components related to the driver/receiver breakout.

9.6.3.2 SGMII Interface Driver Waveforms

Figure 48: SGMII Interface Driver Output Voltage Limits And Definitions

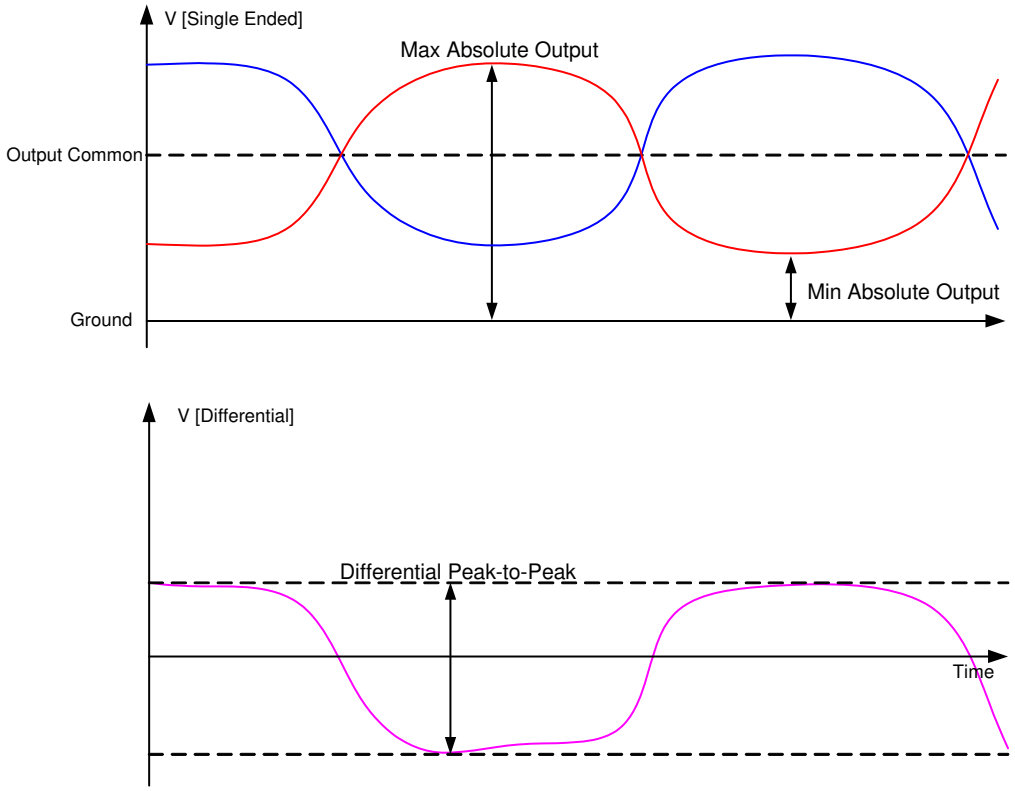
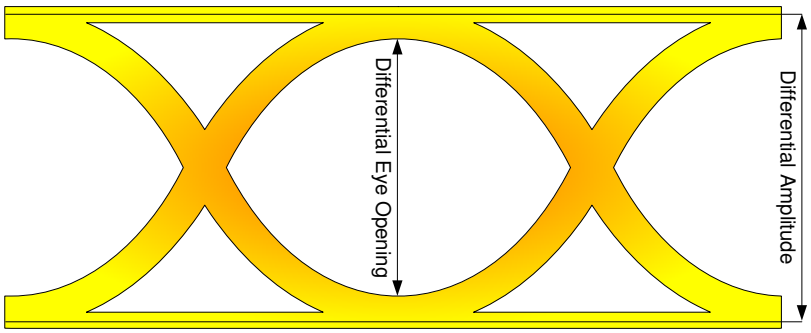


Figure 49: Driver Output Differential Amplitude and Eye Opening



9.6.4 PCIe Interface Electrical Characteristics

9.6.4.1 PCIe Interface Driver and Receiver Characteristics

Table 80: PCIe 1.1 Interface Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud rate	BR	2.5		Gbps	-
Unit interval	UI	400		ps	-
Baud rate tolerance	Bppm	-300	300	ppm	2
Driver parameters					
Differential peak to peak output voltage	VTXpp	0.8	1.2	V	-
Minimum TX eye width	TTXeye	0.75	-	UI	-
Differential return loss	TRLdiff	10	-	dB	1
Common mode return loss	TRLcm	6	-	dB	1
DC differential TX impedance	ZTXdiff	80	120	Ohm	-
Receiver parameters					
Differential input peak to peak voltage	VRXpp	0.175	1.2	V	-
Minimum receiver eye width	TRXeye	0.4	-	UI	-
Differential return loss	RRLdiff	10	-	dB	1
Common mode return loss	RRLcm	6	-	dB	1
DC differential RX impedance	ZRXdiff	80	120	Ohm	-
DC single-ended input impedance	ZRXcm	40	60	Ohm	-

Notes:

General Comment: For more information, refer to the PCI Express Base Specification, Revision 1.1, March, 2005.

1. Defined from 50 MHz to 1.25 GHz.
   Return loss includes contributions from on-chip circuitry, chip packaging,
   and off-chip optimized components related to the driver/receiver breakout.
2. Does not account for SSC dictated variations.

Table 81: PCIe 2.0 Interface Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud rate	BR	5		Gbps	-
Unit interval	UI	200		ps	-
Baud rate tolerance	Bppm	-300	300	ppm	1
Driver parameters					
Differential peak to peak output voltage	VTXpp	0.8	1.2	V	-
Differential peak to peak low power output voltage	VTXpplp	0.4	1.2	V	-
Tx 3.5 dB de-emphasis level ratio	Demph1	3	4	dB	-
Tx 6 dB de-emphasis level ratio	Demph2	5.5	6.5	dB	-
Minimum TX eye width	TTXeye	0.75	-	UI	-
Differential return loss [50 MHz to 1.25 GHz]	TRLdiff	10	-	dB	-
Differential return loss [1.25 GHz to 2.5 GHz]	TRLdiff	8	-	dB	-
Common mode return loss	TRLcm	6	-	dB	2
DC differential TX impedance	ZTXdiff	-	120	Ohm	-
Receiver parameters					
Differential input peak to peak voltage	VRXpp	0.1	1.2	V	-
Minimum receiver eye width	TRXeye	0.4	-	UI	-
Differential return loss [50 MHz to 1.25 GHz]	RRLdiff	10	-	dB	-
Differential return loss [1.25 GHz to 2.5 GHz]	RRLdiff	8	-	dB	-
Common mode return loss	RRLcm	6	-	dB	2
DC single-ended input impedance	ZRXcm	40	60	Ohm	-

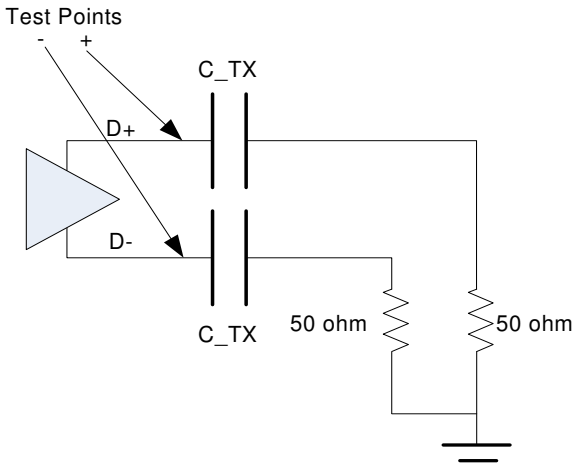
Notes:

General Comment: For more information, refer to the PCI Express Base Specification, Revision 2.1, March 2009.

1. Does not account for SSC dictated variations.
2. Defined from 50 MHz to 2.5 GHz.
   Return loss includes contributions from on-chip circuitry, chip packaging,
   and off-chip optimized components related to the driver/receiver breakout.

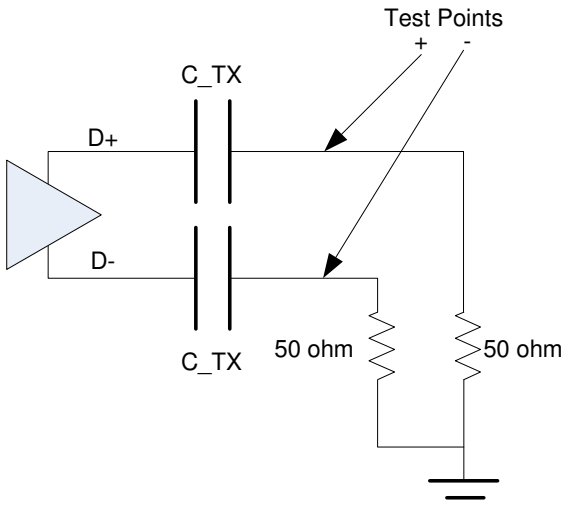
9.6.4.2 PCIe Interface Test Circuit

Figure 50: PCIe 1.1 Interface Test Circuit



When measuring Transmitter output parameters, C_TX is an optional portion of the Test/Measurement load. When used, the value of C_TX must be in the range of 75 nF to 200 nF. C_TX must not be used when the Test/Measurement load is placed in the Receiver package reference plane.

Figure 51: PCIe 2.0 Interface Test Circuit



When measuring Transmitter output parameters, C_TX is an optional portion of the Test/Measurement load. When used, the value of C_TX must be in the range of 75 nF to 200 nF. C_TX must not be used when the Test/Measurement load is placed in the Receiver package reference plane.

9.6.5 SATA Interface Electrical Characteristics

Note

The tables in this section specify the SATA electrical characteristics at the SATA connector. Refer to the device Design Guide for connectivity and layout guidelines of the SATA interface.

9.6.5.1 SATA I Interface Gen1 Mode Driver and Receiver Characteristics

Table 82: SATA I Interface Gen1i Mode Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud Rate	BR	1.5		Gbps	-
Baud rate tolerance	Bppm	-350.0	350.0	ppm	-
Spread spectrum modulation frequency	Fssc	30.0	33.0	kHz	-
Spread spectrum modulation Deviation	SSCtol	-5000.0	0.0	ppm	-
Unit Interval	UI	666.67		ps	-
Driver Parameters					
Differential impedance	Zdifftx	85.0	115.0	Ohm	-
Single ended impedance	Zsetx	40.0	-	Ohm	-
Differential return loss (75 MHz-150 MHz)	RLOD	14.0	-	dB	-
Differential return loss (150 MHz-300 MHz)	RLOD	8.0	-	dB	-
Differential return loss (300 MHz-1.2 GHz)	RLOD	6.0	-	dB	-
Differential return loss (1.2 GHz-2.4 GHz)	RLOD	3.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLOD	1.0	-	dB	-
Output differential voltage	Vdifftx	400.0	600.0	mV	2
Total jitter at connector data-data, 5UI	TJ5	-	0.355	UI	1, 3
Deterministic jitter at connector data-data, 5UI	DJ5	-	0.175	UI	3
Total jitter at connector data-data, 250UI	TJ250	-	0.470	UI	1, 3
Deterministic jitter at connector data-data, 250UI	DJ250	-	0.220	UI	3
Receiver Parameters					
Differential impedance	Zdiffrx	85.0	115.0	Ohm	-
Single ended impedance	Zsetx	40.0	-	Ohm	-
Differential return loss (75 MHz-150 MHz)	RLID	18.0	-	dB	-
Differential return loss (150 MHz-300 MHz)	RLID	14.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLID	10.0	-	dB	-
Differential return loss (600 MHz-1.2 GHz)	RLID	8.0	-	dB	-
Differential return loss (1.2 GHz-2.4 GHz)	RLID	3.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLID	1.0	-	dB	-
Input differential voltage	Vdiffrx	325.0	600.0	mV	-
Total jitter at connector data-data, 5UI	TJ5	-	0.430	UI	1, 3
Deterministic jitter at connector data-data, 5UI	DJ5	-	0.250	UI	3
Total jitter at connector data-data, 250UI	TJ250	-	0.600	UI	1, 3
Deterministic jitter at connector data-data, 250UI	DJ250	-	0.350	UI	3

Notes:

General Comment: For more information, refer to SATA II Revision 2.6 Specification, February, 2007.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Total jitter is defined as TJ = (14 * RJσ) + DJ where Rjσ is random jitter.
2. Output Differential Amplitude and Pre-Emphasis are configurabile. See the functional register description for more details.
3. The value is informative only, and it can be achieved by using a proper board layout. Refer to the hardware design guidelines for more information.

Table 83: SATA I Interface Gen1m Mode Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud Rate	BR	1.5		Gbps	-
Baud rate tolerance	Bppm	-350.0	350.0	ppm	-
Spread spectrum modulation frequency	Fssc	30.0	33.0	kHz	-
Spread spectrum modulation Deviation	SSCtol	-5000.0	0.0	ppm	-
Unit Interval	UI	666.67		ps	-
Driver Parameters					
Differential impedance	Zdifftx	85.0	115.0	Ohm	-
Single ended impedance	Zsetx	40.0	-	Ohm	-
Differential return loss (75 MHz-150 MHz)	RLOD	14.0	-	dB	-
Differential return loss (150 MHz-300 MHz)	RLOD	8.0	-	dB	-
Differential return loss (300 MHz-1.2 GHz)	RLOD	6.0	-	dB	-
Differential return loss (1.2 GHz-2.4 GHz)	RLOD	3.0	-	dB	-
Output differential voltage	Vdifftx	400.0	600.0	mV	2
Total jitter at connector data-data, 5UI	TJ5	-	0.355	UI	1, 3
Deterministic jitter at connector data-data, 5UI	DJ5	-	0.175	UI	3
Total jitter at connector data-data, 250UI	TJ250	-	0.470	UI	1, 3
Deterministic jitter at connector data-data, 250UI	DJ250	-	0.220	UI	3
Receiver Parameters					
Differential impedance	Zdiffrx	85.0	115.0	Ohm	-
Single ended impedance	Zsetx	40.0	-	Ohm	-
Differential return loss (75 MHz-150 MHz)	RLID	18.0	-	dB	-
Differential return loss (150 MHz-300 MHz)	RLID	14.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLID	10.0	-	dB	-
Differential return loss (600 MHz-1.2 GHz)	RLID	8.0	-	dB	-
Differential return loss (1.2 GHz-2.4 GHz)	RLID	3.0	-	dB	-
Input differential voltage	Vdiffrx	240.0	600.0	mV	-
Total jitter at connector data-data, 5UI	TJ5	-	0.430	UI	1, 3
Deterministic jitter at connector data-data, 5UI	DJ5	-	0.250	UI	3
Total jitter at connector data-data, 250UI	TJ250	-	0.600	UI	1, 3
Deterministic jitter at connector data-data, 250UI	DJ250	-	0.350	UI	3

Notes:

General Comment: For more information, refer to SATA II Revision 2.6 Specification, February, 2007.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Total jitter is defined as TJ = (14 * RJσ) + DJ where Rjσ is random jitter.
2. Output Differential Amplitude and Pre-Emphasis are configurabile. See the functional register description for more details.
3. The value is informative only, and it can be achieved by using a proper board layout. Refer to the hardware design guidelines for more information.

9.6.5.2 SATA II Interface Gen2 Mode Driver and Receiver Characteristics

Table 84: SATA II Interface Gen2i Mode Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud Rate	BR	3.0		Gbps	-
Baud rate tolerance	Bppm	-350.0	350.0	ppm	-
Spread spectrum modulation frequency	Fssc	30.0	33.0	kHz	-
Spread spectrum modulation deviation	SSCtol	-5000.0	0.0	ppm	-
Unit Interval	UI	333.33		ps	-
Driver Parameters					
Output differential voltage	Vdifftx	400.0	700.0	mV	1 , 2
Differential return loss (150 MHz-300 MHz)	RLOD	14.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLOD	8.0	-	dB	-
Differential return loss (600 MHz-2.4 GHz)	RLOD	6.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLOD	3.0	-	dB	-
Differential return loss (3.0 GHz-5.0 GHz)	RLOD	1.0	-	dB	-
Total jitter at connector clock-data	TJ	-	0.37	UI	4, 5
Deterministic jitter at connector clock-data	DJ	-	0.19	UI	5
Receiver Parameters					
Input differential voltage	Vdiffrx	275.0	750.0	mV	3
Differential return loss (150 MHz-300 MHz)	RLID	18.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLID	14.0	-	dB	-
Differential return loss (600 MHz-1.2 GHz)	RLID	10.0	-	dB	-
Differential return loss (1.2 GHz-2.4 GHz)	RLID	8.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLID	3.0	-	dB	-
Differential return loss (3.0 GHz-5.0 GHz)	RLID	1.0	-	dB	-
Total jitter at connector clock-data	TJ	-	0.60	UI	4, 5
Deterministic jitter at connector clock-data	DJ	-	0.42	UI	5

Notes:

General Comment: For more information, refer to SATA II Revision 2.6 Specification, February, 2007.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. 0.45-0.55 UI is the range where the signal meets the minimum level.
2. Output Differential Amplitude and Pre-Emphasis are configurabile. See the functional register description for more details.
3. 0.5 UI is the point where the signal meets the minimum level.
4. The jitter is defined using a recovered clock with characteristics that meet the desired Jitter Transfer Function (JTF). The JTF is the ratio between the jitter defined using the recovered clock and the jitter defined using an ideal clock. It should have a high pass function with the following characteristics:
   - The -3 dB corner frequency of the JTF shall be 2.1 MHz +/- 1 MHz.
   - The magnitude peaking of the JTF shall be 3.5 dB maximum.
   - The attenuation at 30 kHz +/- 1% shall be 72 dB +/- 3 dB.
5. The value is informative only, and it can be achieved by using a proper board layout. Refer to the hardware design guidelines for more information.

Table 85: SATA II Interface Gen2m Mode Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud Rate	BR	3.0		Gbps	-
Baud rate tolerance	Bppm	-350.0	350.0	ppm	-
Spread spectrum modulation frequency	Fssc	30.0	33.0	kHz	-
Spread spectrum modulation deviation	SSCtol	-5000.0	0.0	ppm	-
Unit Interval	UI	333.33		ps	-
Driver Parameters					
Output differential voltage	Vdifftx	400.0	700.0	mV	1 , 2
Differential return loss (150 MHz-300 MHz)	RLOD	14.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLOD	8.0	-	dB	-
Differential return loss (600 MHz-2.4 GHz)	RLOD	6.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLOD	3.0	-	dB	-
Total jitter at connector clock-data	TJ	-	0.37	UI	4, 5
Deterministic jitter at connector clock-data	DJ	-	0.19	UI	5
Receiver Parameters					
Input differential voltage	Vdiffrx	240.0	750.0	mV	3
Differential return loss (150 MHz-300 MHz)	RLID	18.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLID	14.0	-	dB	-
Differential return loss (600 MHz-1.2 GHz)	RLID	10.0	-	dB	-
Differential return loss (1.2 GHz-2.4 GHz)	RLID	8.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLID	3.0	-	dB	-
Total jitter at connector clock-data	TJ	-	0.60	UI	4, 5
Deterministic jitter at connector clock-data	DJ	-	0.42	UI	5

Notes:

General Comment: For more information, refer to SATA II Revision 2.6 Specification, February, 2007.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. 0.45-0.55 UI is the range where the signal meets the minimum level.
2. Output Differential Amplitude and Pre-Emphasis are configurabile. See the functional register description for more details.
3. 0.5 UI is the point where the signal meets the minimum level.
4. The jitter is defined using a recovered clock with characteristics that meet the desired Jitter Transfer Function (JTF). The JTF is the ratio between the jitter defined using the recovered clock and the jitter defined using an ideal clock. It should have a high pass function with the following characteristics:
   - The -3 dB corner frequency of the JTF shall be 2.1 MHz +/- 1 MHz.
   - The magnitude peaking of the JTF shall be 3.5 dB maximum.
   - The attenuation at 30 kHz +/- 1% shall be 72 dB +/- 3 dB.
5. The value is informative only, and it can be achieved by using a proper board layout. Refer to the hardware design guidelines for more information.

9.6.5.3 SATA III Interface Gen3 Mode Driver and Receiver Characteristics

Table 86: SATA III Interface Gen3i Mode Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud Rate	BR	6		Gbps	-
Baud rate tolerance	Bppm	-350	350	ppm	-
Spread spectrum modulation frequency	Fssc	30	33	kHz	-
Spread spectrum modulation Deviation	SSCtol	-5350	350	ppm	-
Unit Interval	UI	166.667		ps	-
Driver Parameters					
Output differential voltage in device mode	Vdifftx	240	900	mV	1 , 2
Output differential voltage in host mode	Vdifftx	200	900	mV	1 , 2
Output single-ended rise/fall time	Tr/Tf	0.2	0.48	UI	3
Output differential skew	Tskew	-	20	ps	-
Differential return loss (300 MHz)	RLOD	14	-	dB	5
Differential return loss (3 GHz)	RLOD	1	-	dB	5
Differential return loss slope	RLODs	13	-	dB/dec	-
Total jitter at connector clock-data	TJtx	-	0.52	UI	4, 6, 7
Receiver Parameters					
Input differential voltage in device mode	Vdiffrx	240	1000	mV	1
Input differential voltage in host mode	Vdiffrx	200	1000	mV	1
Input differential skew	Tskew	-	30	ps	-
Differential return loss (300 MHz)	RLID	18	-	dB	5
Differential return loss (6 GHz)	RLID	1.09	-	dB	5
Differential return loss slope	RLIDs	13	-	dB/dec	-
Total jitter at connector clock-data	TJrx	-	0.6	UI	4, 6, 7
Deterministic jitter at connector clock-data	DJrx	-	0.42	UI	4, 7

Notes:

General Comment: For more information, refer to SATA III Revision 3.1 Specification, July, 2011.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. 0.5 UI is the point where the signal meets the minimum level.
2. Output Differential Amplitude and Pre-Emphasis are configurabile. See the functional register description for more details.
3. Defined from 20% to 80% of the signal for Tr, and from 80% to 20% for Tf.
4. The value is informative only, and it can be achieved by using a proper board layout. Refer to the hardware design guidelines for more information.
5. The two points are connected linearly on a logarithmic scale.
6. Defined with a Bit Error Rate (BER) of 10^-12.
7. The jitter is defined using a recovered clock with characteristics that meet the desired Jitter Transfer Function (JTF). The JTF is the ratio between the jitter defined using the recovered clock and the jitter defined using an ideal clock. It should have a high pass function with the following characteristics:
   - The -3 dB corner frequency of the JTF shall be 4.2 MHz +/- 2 MHz.
   - The magnitude peaking of the JTF shall be 3.5 dB maximum.
   - The attenuation at 420 kHz +/- 1% shall be 38.2 dB +/- 3 dB.

9.6.6 USB Electrical Characteristics

9.6.6.1 USB Driver and Receiver Characteristics

Table 87: USB Low Speed Driver and Receiver Characteristics

Description	Symbol	Low Speed		Units	Notes
		Min	Max		
Baud Rate	BR	1.5		Mbps	-
Baud rate tolerance	Bppm	-15000.0	15000.0	ppm	-
Driver Parameters					
Ouput single ended high	VOH	2.8	3.6	V	1
Ouput single ended low	VOL	0.0	0.3	V	2
Output signal crossover voltage	VCRS	1.3	2.0	V	3
Data fall time	TLR	75.0	300.0	ns	3, 4
Data rise time	TLF	75.0	300.0	ns	3, 4
Rise and fall time matching	TLRFM	80.0	125.0	%	-
Source jitter total: to next transition	TUDJ1	-95.0	95.0	ns	5
Source jitter total: for paired transitions	TUDJ2	-150.0	150.0	ns	5
Receiver Parameters					
Input single ended high	VIH	2.0	-	V	-
Input single ended low	VIL	-	0.8	V	-
Differential input sensitivity	VDI	0.2	-	V	-

Notes:

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Defined with 1.425 kilohm pull-up resistor to 3.6V.
2. Defined with 14.25 kilohm pull-down resistor to ground.
3. See "Data Signal Rise and Fall Time" waveform.
4. Defined from 10% to 90% for rise time and 90% to 10% for fall time.
5. Including frequency tolerance. Timing difference between the differential data signals.

   Defined at crossover point of differential data signals.

Table 88: USB Full Speed Driver and Receiver Characteristics

Description	Symbol	Full Speed		Units	Notes
		Min	Max		
Baud Rate	BR	12.0		Mbps	-
Baud rate tolerance	Bppm	-2500.0	2500.0	ppm	-
Driver Parameters					
Ouput single ended high	VOH	2.8	3.6	V	1
Ouput single ended low	VOL	0.0	0.3	V	2
Output signal crossover voltage	VCRS	1.3	2.0	V	4
Output rise time	TFR	4.0	20.0	ns	3, 4
Output fall time	TFL	4.0	20.0	ns	3, 4
Source jitter total: to next transition	TDJ1	-3.5	3.5	ns	5, 6
Source jitter total: for paired transitions	TDJ2	-4.0	4.0	ns	5, 6
Source jitter for differential transition to SE0 transition	TFDEOP	-2.0	5.0	ns	6
Receiver Parameters					
Input single ended high	VIH	2.0	-	V	-
Input single ended low	VIL	-	0.8	V	-
Differential input sensitivity	VDI	0.2	-	V	-
Receiver jitter : to next transition	tJR1	-18.5	18.5	ns	6
Receiver jitter: for paired transitions	tJR2	-9.0	9.0	ns	6

Notes:

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Defined with 1.425 kilohm pull-up resistor to 3.6V.
2. Defined with 14.25 kilohm pull-down resistor to ground.
3. Defined from 10% to 90% for rise time and 90% to 10% for fall time.
4. See "Data Signal Rise and Fall Time" waveform.
5. Including frequency tolerance. Timing difference between the differential data signals.
6. Defined at crossover point of differential data signals.

Table 89: USB High Speed Driver and Receiver Characteristics

Description	Symbol	High Speed		Units	Notes
		Min	Max		
Baud Rate	BR	480.0		Mbps	-
Baud rate tolerance	Bppm	-500.0	500.0	ppm	-
Driver Parameters					
Data signaling high	VHSOH	360.0	440.0	mV	-
Data signaling low	VHSOL	-10.0	10.0	mV	-
Data rise time	THSR	500.0	-	ps	1
Data fall time	THSF	500.0	-	ps	1
Data source jitter		See note 2			2
Receiver Parameters					
Differential input signaling levels		See note 3			3
Data signaling common mode voltage range	VHSCM	-50.0	500.0	mV	-
Receiver jitter tolerance		See note 3			3

Notes:

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Defined from 10% to 90% for rise time and 90% to 10% for fall time.
2. Source jitter specified by the "TX eye diagram pattern template" figure.
3. Receiver jitter specified by the "RX eye diagram pattern template" figure.

Table 90: USB SuperSpeed Gen 1 Driver and Receiver Characteristics

Description	Symbol	Super Speed		Units	Notes
		Min	Max		
Baud Rate	BR	5		Gbps	-
Baud rate tolerance	Bppm	-300	300	ppm	-
Spread spectrum modulation frequency	Fssc	30	33	kHz	-
Spread spectrum modulation deviation	SSCtol	-5000	0.0	ppm	2
Unit interval	UI	200		ps	-
Driver Parameters					
Output differential minimum eye opening	Vodppe	800	-	mV	-
Output differential minimum eye opening	Vodlppe	400	-	mV	3
Output differential maximum peak-to-peak	Vodpp	-	1200	mV	-
Output AC common mode voltage active peak-to-peak	Vtxaccm	-	100	mV	-
Output emphasis	Emph	3	4	dB	-
Output differential resistance	Rdo	72	120	Ohm	-
Output DC common mode impedance	Tx-dc	18	30	Ohm	8
Output frequency slew rate	Cdr_slew	-	10	ms/s	11
Output jitter - Deterministic, delta-delta	Jdtx	-	0.205	UI	6
Output jitter - Total, peak-to-peak	Jtpptx	-	0.375	UI	4, 5, 7
Receiver Parameters					
Input differential sensitivity	Vidpps	30	-	mV	1, 9
Input differential voltage	Vidpp	-	1200	mV	1
Low Frequency Periodic Signaling (LFPS) detect threshold	Vrxdetpp	100	300	mV	-
Input differential resistance	Rdi	72	120	Ohm	-
Input common resistance	Rci	18	30	Ohm	-
Input jitter - Deterministic, peak-to-peak	Jtrx	-	0.715	UI	10
Input jitter - Total, peak-to-peak	Jtrxpp	-	0.55	UI	4, 5, 9

Notes:

General Comment: For more information, refer to Universal Serial Bus 3.1 Specification, Revision 1.0, July 2013.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Vidpps refers to the internal eye opening while Vidpp refers to the peak-to-peak.
2. Defined below 2 MHz only.
3. When TX driver is configured to work in Low-Power-Swing mode.
4. Defined with a Bit Error Rate (BER) of 10^-12.
5. Total jitter is composed of both deterministic and random components.
   The allowed random jitter equals the allowed total jitter minus the actual deterministic jitter at that point.
6. Driver jitter does not include correlated bounded jitter created by the driver emphasis.
7. The output TX jitter is defined when applying the effect of a single-pole high-pass filter on the jitter.
   The high-pass filter 3 dB point is located at 4.9 MHz.
8. Defined with respect to AC ground over a voltage of 0-500 mV.
9. Defined after applying reference receiver CTLE function according to section 6.8.2 "Informative Receiver CTLE Function" in USB 3.1 specification.
10. Defined without applying reference receiver CTLE function.
11. This value includes all SSC and jitter sources. Refer to section 6.5.4 "Normative Slew Rate Limit" in the USB 3.1 specification.

9.6.6.2 USB Interface Driver Waveforms

Figure 52: Low/Full Speed Data Signal Rise and Fall Time

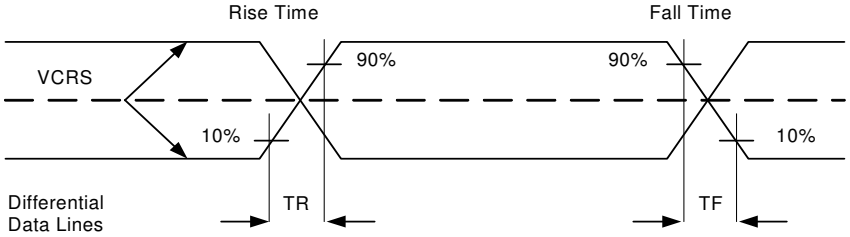


Figure 53: High Speed TX Eye Diagram Pattern Template

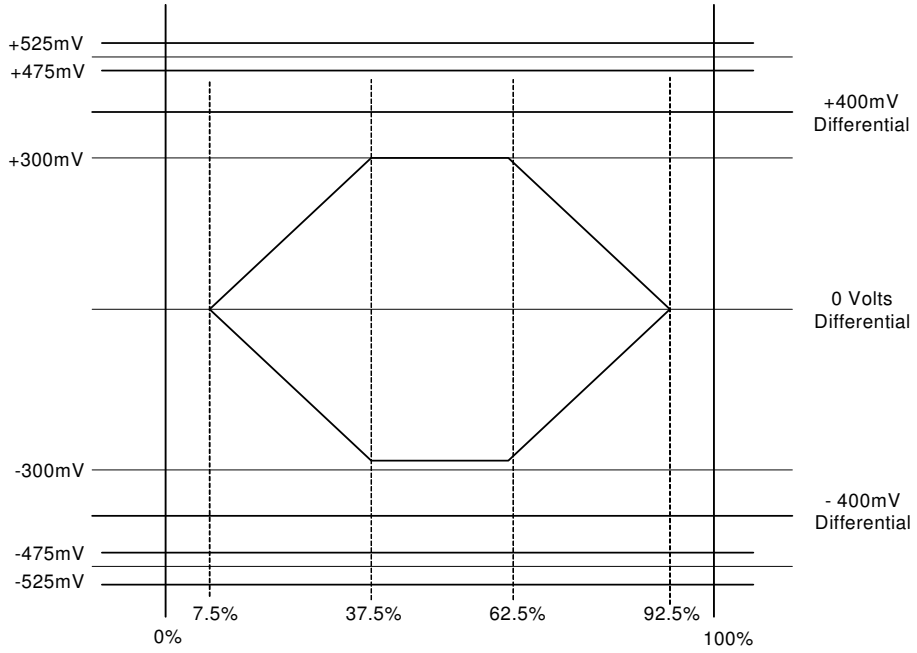
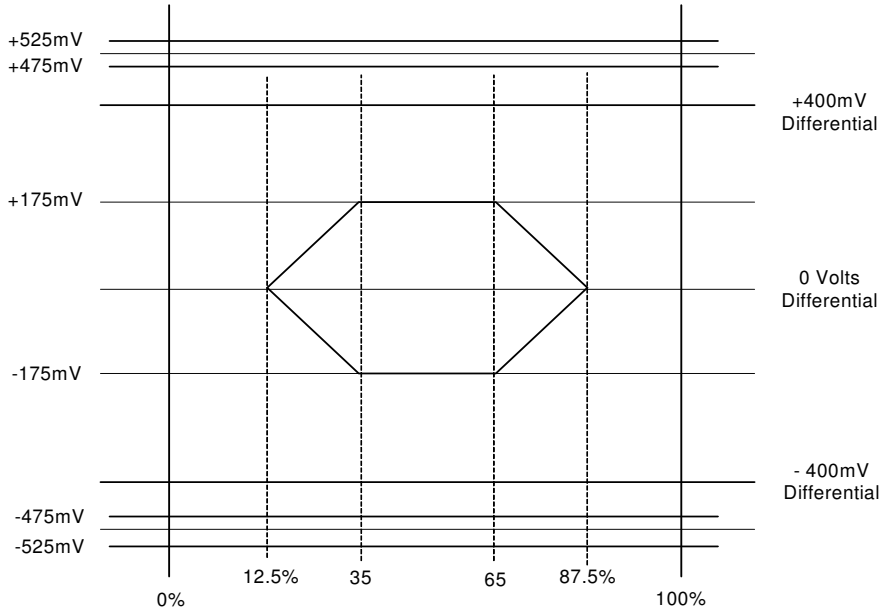


Figure 54: High Speed RX Eye Diagram Pattern Template



10 Thermal Data

Table 91 provides the package thermal data for the devices. This data is derived from simulations that were run according to the JEDEC standard.

Note The thermal parameters are preliminary and subject to change.

The documents listed below provide a basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products. Before designing a system it is recommended to refer to these documents:

- Application Note, *AN-63 Thermal Management for Selected Marvell® Products,* Document Number MV-S300281-00
- White Paper, *ThetaJC, ThetaJA, and Temperature Calculations,* Document Number MV-S700019-00.

Table 91: Devices Thermal Data

Symbol	Definition	Airflow Value (°C/W)
		0[m/s]
θ_{JA}	Thermal resistance: junction to ambient	21.87
Ψ_{JT}	Thermal characterization parameter: junction to top center	0.09
Ψ_{JB}	Thermal characterization parameter: junction to board	9.65
θ_{JC}	Thermal resistance: junction to case (not air-flow dependent)	5.62
θ_{JB}	Thermal resistance: junction to board (not air-flow dependent)	9.71

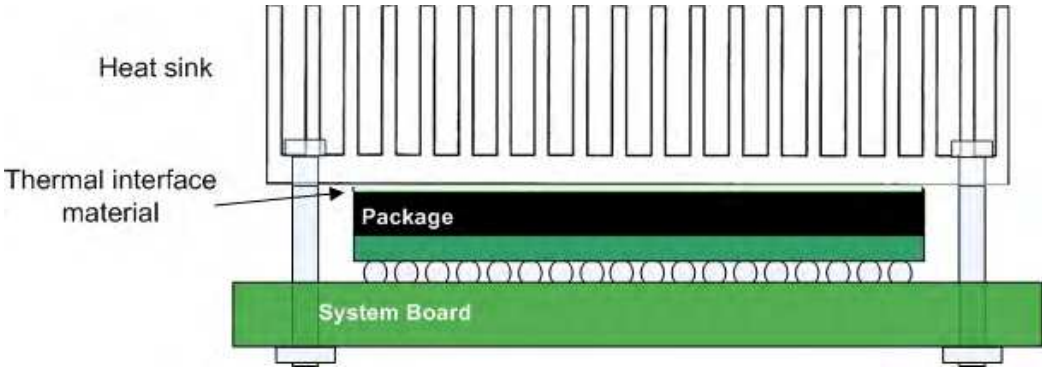
10.1 Heat Sink Mounting Guidelines

- The maximum static load should not exceed 100 Newton.
- The load must be applied uniformly and distributed perpendicularly to the package top surface.
- The applied load should meet the thermal solution and thermal interface material specifications.

Note The heat sink option is used for applications that are not able to meet the specified device junction temperature.

Figure 55 shows an illustration of the heat sink attachment for the device.

Figure 55: Heat Sink Attachment Illustration



11 Package

The 88F3710/88F3720 uses a TFBGA 11.5 x10.5 mm 271B package with a 0.5 mm ball pitch.

Figure 56: TFBGA 11.5 x 10.5 mm 271B Package

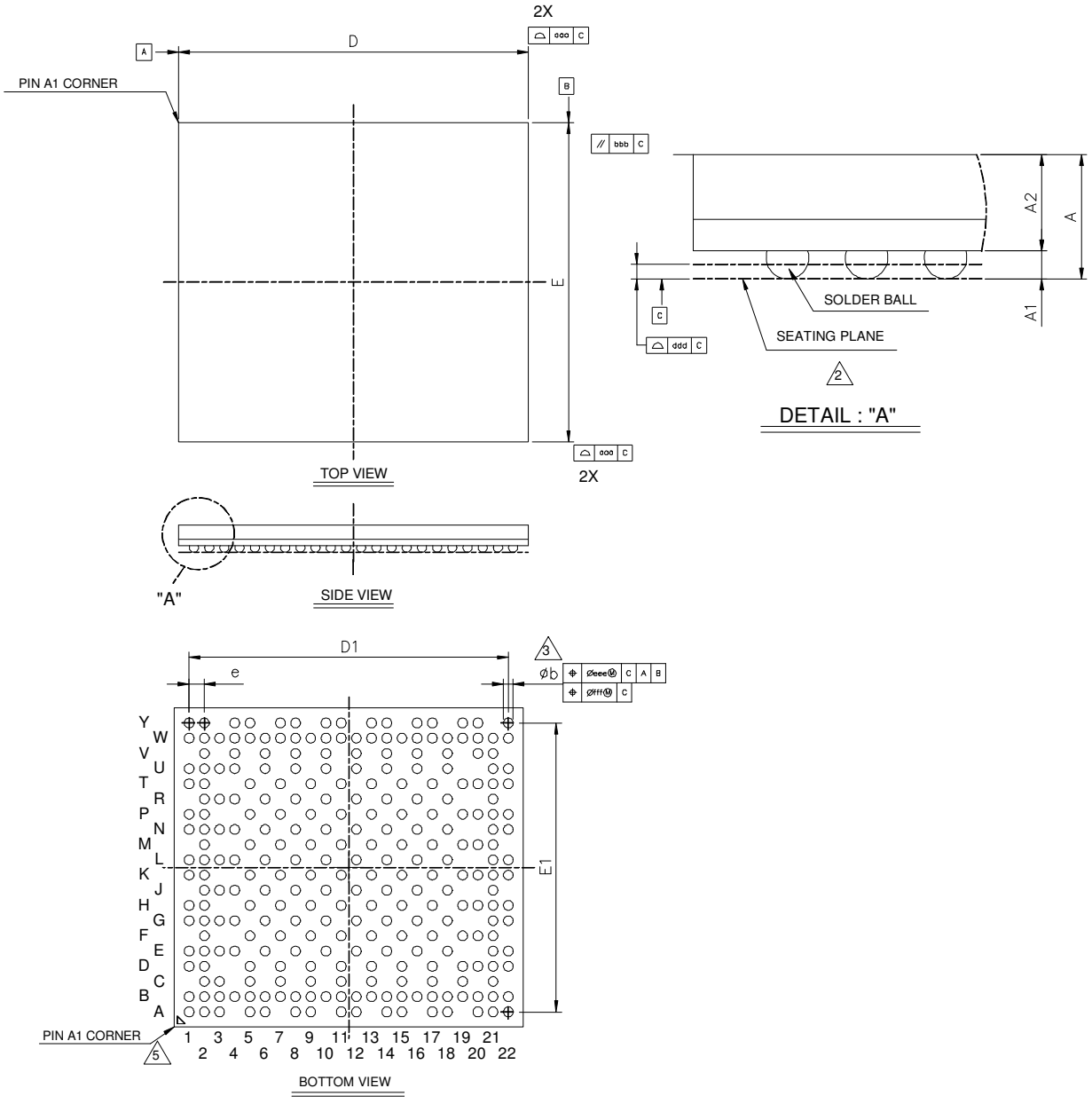


Figure 57: TFBGA 11.5 x 10.5 mm 271B Package Dimensions

Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.79	0.88	0.97
A1	0.16	0.21	0.26
A2	0.62	0.67	0.72
D	11.40	11.50	11.60
E	10.40	10.50	10.60
D1	---	10.50	---
E1	---	9.50	---
e	---	0.50	---
b	0.27	0.32	0.37
aaa	0.15		
bbb	0.10		
ddd	0.10		
eee	0.15		
fff	0.08		
MD/ME	22/20		

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: bbb , ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .

12 Part Order Numbering/Package Marking

12.1 Part Order Numbering

Figure 58 shows the part order numbering scheme for the 88F3710/88F3720. Refer to Marvell Field Application Engineers (FAEs) or representatives for further information when ordering parts.

Figure 58: Sample Part Number

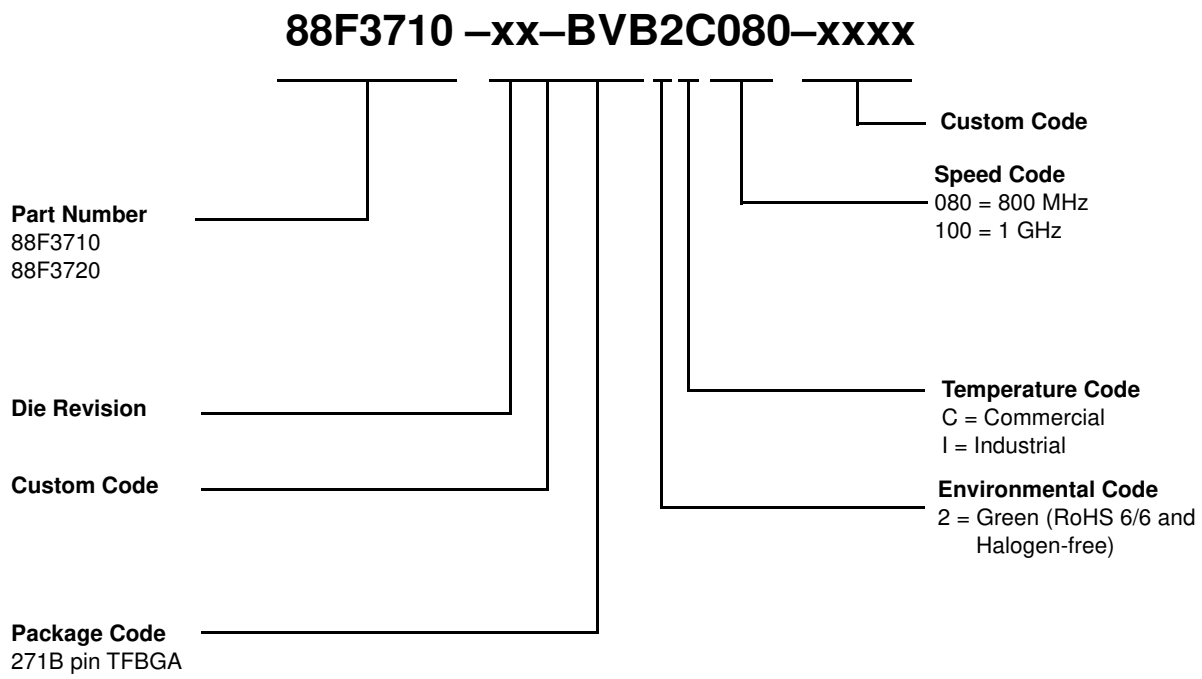


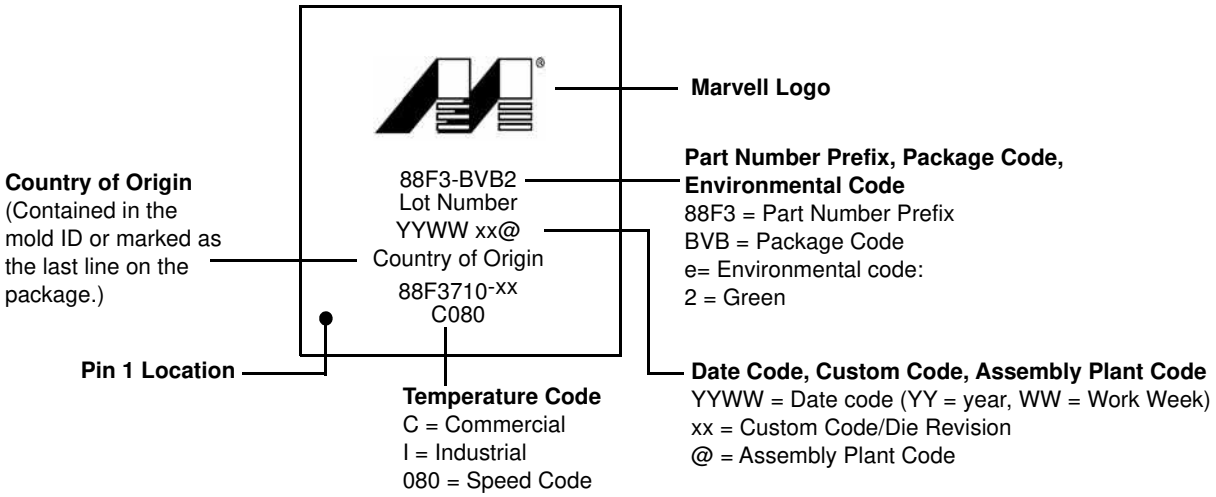
Table 92: 88F3710/88F3720 Part Order Options

Package Type	Part Order Number
TFBGA	88F3710-xx-–BVB2C080-P123 800 MHz part (Green, RoHS 6/6 and Halogen-free package)
	88F3710-xx-–BVB2C100-P123 1 GHz part (Green, RoHS 6/6, Halogen-free package)
	88F3710-xx-–BVB2I080-P123 800 MHz part (Green, RoHS 6/6, Halogen-free package)
	88F3710-xx-–BVB2I100-P123 1 GHz part (Green, RoHS 6/6, Halogen-free package)
	88F3720-xx-–BVB2C080-P123 800 MHz part (Green, RoHS 6/6, Halogen-free package)
	88F3720-xx-–BVB2C100-P123 1 GHz part (Green, RoHS 6/6, Halogen-free package)
	88F3720-xx-–BVB2I080-P123 800 MHz part (Green, RoHS 6/6, Halogen-free package)
	88F3720-xx-–BVB2I100-P123 1 GHz part (Green, RoHS 6/6, Halogen-free package)

12.2 Package Marking

Figure 59 shows a sample Commercial and Industrial package marking and pin 1 location on the 88F3710/88F3720 devices.

Figure 59: Sample Commercial Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

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