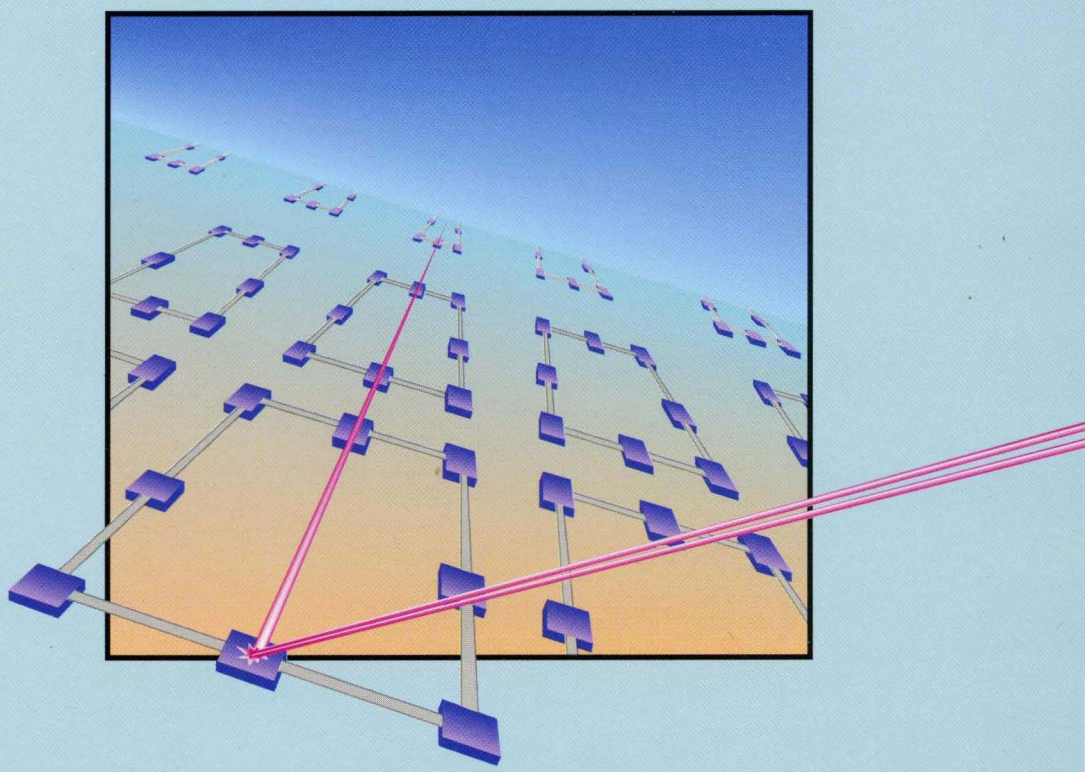
MC68837UM/AD

FDDI



Fiber Distributed Data Interface
User's Manual

MC68837

MOTOROLA

MOTOROLA

MC68837

Elasticity Buffer and Link Management User's Manual

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

Section 4
Signal Description

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Concluded)

LIST OF FIGURES

LIST OF TABLES

MC68837 ACRONYM LIST

ANSI—American National Standards Institute

BIST—built-in self-test

CMOS—complementary metal-oxide semiconductor

CMT—connection management

ELM—elasticity buffer and link management

FCG—FDDI clock generator

FCS—frame check sequence

FDDI—fiber-distributed data interface

LAN—local area network

LEM—link error monitor

LM—link management

MAC—media access controller

MUX—multiplexer

NPA—node processor address bus

NPD—node processor data bus

NPI—node processor interface

PCI—physical connection insertion

PCM—physical connection management

PHY—physical layer

SMT—station management and submanagement of FDDI standard

TNE—timer, noise events

TPC—timer, physical connection

SECTION 1
INTRODUCTION

1

The MC68837 elasticity buffer and link management (ELM) chip implements the PHY functions of the FDDI standard including data framing, elasticity buffer, encoding, decoding, smoothing, line state detection, and repeat filter. The ELM also contains the following SMT functions: CMT, PCM, PCI, and LEM.

The FDDI is a 125-Mbit/sec, fiber-optic-based, token-ring LAN standard designed to accommodate rings with up to 1000 stations, with 2 km between stations and 200 km total ring length (see Figure 1-1). Users are encouraged to refer to the pertinent ANSI standard documents for further information.

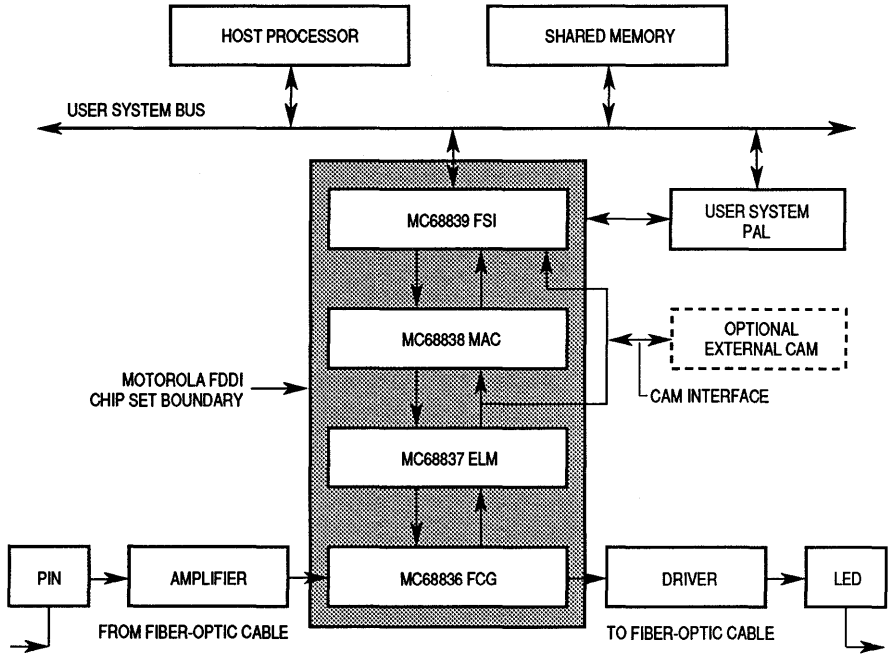


Figure 1-1. FDDI Architecture

The following list contains the ELM chip features:

- Implements ANSI FDDI PHY Standard
- 4B/5B Encoding and Decoding, Elasticity Buffer, and Smoother Functions
- Data Framing and Alignment to Byte Boundaries
- Hardware Assist for PCM State Machine Reduces Load on SMT Processing
- Contains Line State Detector and Repeat Filter
- Link Error Monitor Detection and Counting On Chip
- Performs Scrubbing and Provides for Nonconcatenation of Frames
- Contains an Interface to an Optional Communications Processor
- Data Paths Can Easily Be Multiplexed To Support Different Configurations
- BIST and Boundary Scan
- Full-Duplex Operation
- High-Speed CMOS Technology

SECTION 2
FUNCTIONAL DESCRIPTION

Figure 2-1 shows a diagram of the ELM functional blocks and data paths. This section contains detailed descriptions of the function of the various blocks in the chip.

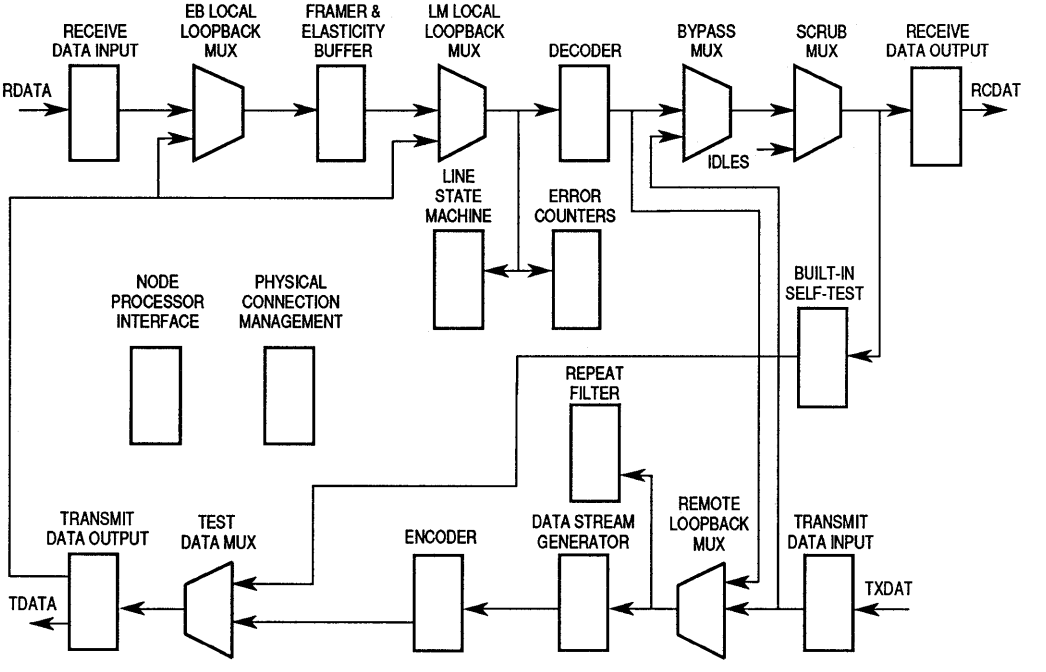


Figure 2-1. ELM High-Level Functional Block Diagram

2.1 FRAMER

The framer accepts 5-bit-wide parallel data as well as the RSCLK from the MC68836 FCG chip. Generally, data coming into the framer is not framed into proper FDDI symbols. The framer is used to align the incoming data to form proper symbols before the data is passed to the elasticity buffer. A starting delimiter used at the beginning of each frame is detected by the framer and used to determine proper symbol boundaries for the data. The framer has been designed so that the starting delimiter (the JK-symbol pair) is detected independently of previous framing.

2.2 ELASTICITY BUFFER

The elasticity buffer performs the necessary buffering to allow data to pass between different FDDI stations with independent station clocks. The elasticity buffer consists of an 80-bit buffer and some control circuitry. The buffer is used to compensate for the differences in the transmit and receive clock frequencies in the station. Data is clocked into the buffer by the RSCLK and clocked out of the buffer by the local clock. The RSCLK is also used to drive all the input circuitry including the input controller and input pointer. The local clock is also used to drive the output circuitry including the output pointer, the output controller, the overflow/underflow detection circuitry, and the output buffer. Note that the elasticity buffer uses a different version of the local byte clock than the reset of the ELM chip. This version is generated on chip from SYMCLK.

2.3 DATA PATH MULTIPLEXERS

The receive data path and transmit data path of the ELM include six multiplexers for the purpose of altering the normal flow of data through the chip (see Figure 2-1). Altering the data paths may be necessary for physical connection insertion and removal and for testing and diagnostics. All receive and transmit paths internal to the ELM are 10 bits (two symbols) wide.

2.3.1 Elasticity Buffer Local Loopback MUX

In normal operating mode, the elasticity buffer local loopback MUX puts data held in the RDATAx latch onto the receive data path of the ELM.

When the EB_LOC_LOOP bit in control register A is set or when BIST is running, the MUX loops back the data in the TDATAx latch onto the receive data path. This creates a path whereby data from the MAC can traverse the entire transmit and receive data paths of the ELM and be returned to the MAC. BIST uses this loopback along with the remote loopback MUX to create a loop that covers the entire transmit and receive data paths.

Note that when this loopback mode is in effect, the BYTCLK is switched so that it is the same as the local byte clock.

2.3.2 Link Management Local Loopback MUX

In normal operating mode, the LM local loopback MUX receives data from the elasticity buffer and passes it through the receive data path at a point before the decoder.

When the ELM_LOC_LOOP bit in control register A is set, this MUX loops back the data in the TDATAx latch onto the receive data path. This MUX provides a method for testing most ELM circuitry without the influence of the framer or elasticity buffer.

2.3.3 Bypass MUX

In normal operating mode, the bypass MUX sends the data output provided by the decoder to the scrub MUX.

For single attach slave stations, the MUX can be controlled with the CLASS_S bit in control register B. For other station types, when the SC_BYPASS bit in control register A is set while the PCM is in the MAINT state or the CONFIG_CNTRL bit in control register B is set, or when the PCI is in the REMOVED, INSERT_SCRUB or REMOVE_SCRUB state, the data in the TXDATx latch is put onto the receive path to the scrub MUX. On power-up, this bypass path will be in effect. The delay through a bypassed ELM is 80 ns.

2.3.4 Scrub MUX

The scrub MUX selects its input from either constant idle symbol pairs or the output of the bypass MUX.

When the REQ_SCRUB bit in control register A is set while the PCM is in the MAINT state or the CONFIG_CNTRL bit in control register B is set, or when the PCI is in the INSERT_SCRUB or REMOVE_SCRUB state, the output of the scrub MUX is idle symbols. Otherwise, the output of the bypass MUX is placed onto the RCDATx bus.

This MUX is used during physical connection insertion and removal to output idle symbols on RCDATx when scrubbing the ring.

2.3.5 Remote Loopback MUX

In normal operating mode, the remote loopback MUX puts the data held in the TXDATx latch onto the transmit data path of the ELM.

When the REM_LOOP bit in control register A is set, a remote loopback path is set (the EB_LOC_LOOP and ELM_LOC_LOOP bits are not set), or when BIST is running, this MUX loops back the data from the decoder onto the transmit data path. This loopback creates a path on which data from the FCG can traverse the entire data path of the ELM and be transmitted to the FCG. BIST uses this loopback along with the elasticity buffer local loopback MUX to create a loop that covers the entire receive and transmit data paths.

2.3.6 Test Data MUX

In normal operating mode, the test data MUX sends the data output by the encoder to the TDATAx latch.

When BIST is running, the test data MUX selects the input from the BIST block. Test data is returned to the BIST block at the output of the scrub MUX.

2.4 DECODER

The decoder performs the 4B/5B decoding of received data symbols. The five bits of aligned data are decoded into four bits of data and one control bit, with the high-order bit being the control bit. The decoded symbol pairs are then sent to the MAC. Although the decoder operates on symbol pairs, each symbol is decoded independently of the other.

Until the PCM has completed establishing a connection for the physical link, the physical layer invalid (PI) symbol is returned to the MAC on both RCDAT9–RCDAT5 and RCDAT4–RCDAT0. In addition, a violation (V) symbol is generated when an input error condition has been detected, such as an elasticity buffer error (buffer overflow or underflow). PI takes precedence over V; therefore, if an elasticity buffer error occurs while the current line state is Quiet, Halt, Master, or Noise, PI is given to the MAC. Table 2-1 lists the RDATAx and RCDATx decoding.

The decoder can be disabled via the ENCOFF pin.

Table 2-1. 4B/5B Decoding of Data

Symbol	RDATA(9–5)(4–0)	RCDAT(9–5)(4–0)
Q	00000	10000
I	11111	10111
H1	00100	10100
J	11000	11100
K	10001	10011
T	01101	11101
R	00111	10001
S	11001	11001
H5	00001	10100
H4	00010	10100
V1	00011	11000
V2	00101	11000
V3	00110	11000
H3	01000	10100
V4	01100	11000
H2	10000	10100
PI	XXXXX[1]	00011
0	11110	00000
1	01001	00001
2	10100	00010
3	10101	00011
4	01010	00100
5	01011	00101
6	01110	00110
7	01111	00111
8	10010	01000
9	10011	01001
A	10110	01010
B	10111	01011
C	11010	01100
D	11011	01101
E	11100	01110
F	11101	01111

NOTE 1: X = Don't care; a PI of 00011 is returned on the elasticity buffer overflow.

2.5 ENCODER

The encoder performs the 4B/5B encoding of data symbols to be transmitted over the physical medium. The four bits of data and one control bit from the MAC are encoded into a unique 5-bit symbol that is sent to the FCG circuitry. Although the encoder operates on symbol pairs, each symbol is encoded independently of the other. When the GOBBLE_BYTE signal is asserted by the repeat filter, the input data symbols are ignored, and the encoder outputs an idle (I) symbol pair. This facility is used to strip frame fragments from the FDDI ring.

A parity error on the TXDATx bus sets the ELM's internal bus to a pair of INVALID symbols (1100011000). If the RF_DISABLE bit in ELM control register A is clear, the repeat filter changes these INVALID symbols to I-symbols. Parity detection can be enabled or disabled with the ENA_PARITY_CHK bit in ELM control register A.

The encoder can be disabled via the ENCOFF pin.

The 4-bit to 5-bit symbol assignments are defined in Table 2-2.

Table 2-2. 4B/5B Encoding of Data

Symbol	TXDAT(9–5)(4–0)	TDATA(9–5)(4–0)
Q	10000	00000
I	10111	11111
H	10100	00100
J	11100	11000
K	10011	10001
T	11101	01101
R	10001	00111
S	11001	11001
INVALID	11110	11111
INVALID	10010	11111
INVALID	10101	11111
INVALID	10110	11111
INVALID	11111	11111
INVALID	11000	11111
INVALID	11010	11111
INVALID	11011	11111
0	00000	11110
1	00001	01001
2	00010	10100
3	00011	10101
4	00100	01010
5	00101	01011
6	00110	01110
7	00111	01111
8	01000	10010
9	01001	10011
A	01010	10110
B	01011	10111
C	01100	11010
D	01101	11011
E	01110	11100
F	01111	11101

2.6 REPEAT FILTER

The repeat filter operates on the symbol stream at the output of the remote loopback MUX. Only Idle and Active Line States are allowed to propagate through the station. Invalid Line States will be turned into an I-symbol stream. Also, if the repeat filter detects a corrupted frame, it truncates the frame by transmitting four halt (H) symbols and then I. The H-symbols cause the next MAC entity in the logical ring to count the frame as a lost frame.

Another function of the repeat filter is called the GOBBLE_BYTE. When the repeat filter detects a fragment (i.e., a frame in which an I-symbol appears before the ending delimiter), it instructs the encoder to change the previous symbol pair to I-symbols. After passing through repeat filters in other stations, the fragment will eventually be converted to I-symbols.

The repeat filter is defined in the ANSI FDDI PHY document. The ELM is a byte-wide implementation.

2.7 DATA I/O PORTS

The ELM contains four ports for the input and output of network data: RDATAx, RCDATx, TXDATx, and TDATAx. The signal timing for these ports is shown in **Section 8 Electrical Characteristics**.

2.7.1 Receive Data Input

RDATAx is a 5-bit (symbol wide) data bus coming from the FCG to the ELM. Data is clocked in synchronously with the RSCLK. RSCLK is also used to clock the data through the framer and into the elasticity buffer.

2.7.2 Receive Data Output

RCDATx is a 10-bit (symbol-pair wide) data bus going from the ELM to the MAC or, in a concentrator, to another ELM. Data is latched inside the ELM on each rising edge of BYTCLK and is available to the MAC.

2.7.3 Transmit Data Input

TXDATx is a 10-bit (symbol-pair wide) data bus coming from the MAC to the ELM or, in a concentrator, from another ELM to the ELM. Although the data on this bus must be latched on each rising edge of BYTCLK for use internal to the ELM, the short hold time provided by the MAC relative to BYTCLK requires some additional clocking circuitry. The data is initially latched into the ELM by each falling edge of SYMCLK. The data latched by the falling edge of SYMCLK that precedes the rising edge of BYTCLK is then latched again by that rising edge of BYTCLK. Having no skew between SYMCLK and BYTCLK effectively adds 20 ns to the hold time provided on TXDATx. Any amount by which BYTCLK trails SYMCLK will subtract from the hold time provided.

2.7.4 Transmit Data Output

TDATAx is a 5-bit (symbol wide) data bus going from the ELM to the FCG. The 10-bit internal data bus is latched initially by the ELM on each rising edge of BYTCLK. Bits 9–5 are then latched by the rising edge of SYMCLK following the rising edge of BYTCLK. Bits 4–0 are then latched by the next rising edge of SYMCLK, which follows the falling edge of BYTCLK. Data is available to the FCG after each rising edge of SYMCLK.

2.8 CMT LOGIC

The following three logic blocks implement facilities to provide for physical connection management and link monitoring. These blocks implement helpful time-critical state machines and monitoring logic for use by SMT and CMT pseudocode.

2.8.1 Line State Machine

In FDDI networks, a special group of symbols called "line state symbols" (Q–quiet, H–halt, I–idle, and the JK symbol pair) are transmitted to establish the physical connection between neighboring stations. These line state symbols are unique in that they can be recognized independently of symbol boundaries. Line states are comprised of consecutive line state symbols as defined in **Section 3 Register Description.**

2.8.2 Link Error Monitor

The LEM provides an indication of the inbound link quality to the PCM. The PCM uses this information to determine if the Link Confidence Test passes to establish a new connection. Once a link is active, the PCM continually runs an LEM test to detect and isolate links having an inadequate bit error rate.

2.8.3 Data Stream Generator

The data stream generator uses a multiplexer for the purpose of generating a symbol pair at the request of the PCM or external control when the PCM is in MAINT. The symbol pair can be requested by the PCM state machine, the repeat filter, or the node processor while in MAINT as selected by the MAINT_LS bit in control register B. The user can only control the generation of the symbol pairs while in the maintenance mode. Both the repeat filter and the PCM state machine can be turned off, but while operating, they generate symbol pairs according to their internal algorithms.

2.8.4 Physical Connection Management

CMT defines the operation of PHY layer insertion and removal and the connection of PHY entities to the MAC entities. PCM, a subset of CMT, is the management of a physical connection between the PHY being managed and another PHY.

PCM consists of two entities: the state machine and the pseudocode. The ELM chip implements the PCM state machine; whereas, the pseudocode is implemented by driver software.

The PCI state machine works in conjunction with the PCM state machine. The PCI controls ring scrubbing and the insertion and removal of a station on the ring.

SECTION 3
REGISTER DESCRIPTION

The ELM contains 26 16-bit control and status registers addressed from 00 to 34 (hex). The register set is listed in Table 3-1.

Table 3-1. ELM Register Set

Address	Name	Mnemonic	Type
00	Control Register A	ELM_CNTRL_A	Read/Write
01	Control Register B	ELM_CNTRL_B	Read/Write
02	Interrupt Mask Register	INTR_MASK	Read/Write
03	Transmit Vector Register	XMIT_VECTOR	Read/Write
04	Transmit Vector Length Register	VECTOR_LENGTH	Read/Write
05	Link Error Event Threshold Register	LE_THRESHOLD	Read/Write
06	Maximum PHY Acquisition Time Register	A_MAX	Read/Write
07	Maximum Line State Change Time Register	LS_MAX	Read/Write
08	Minimum Break Time Register	TB_MIN	Read/Write
09	Signaling Time Out Register	T_OUT	Read/Write
0B	Short Link Confidence Test Time Register	LC_SHORT	Read/Write
0C	Scrub Time Register	T_SCRUB	Read/Write
0D	Noise Time Register	NS_MAX	Read/Write
0E	TPC Load Value Register	TPC_LOAD_VALUE	Write-Only
0F	TNE Load Value Register	TNE_LOAD_VALUE	Write-Only
10	Status Register A	ELM_STATUS_A	Read-Only
11	Status Register B	ELM_STATUS_B	Read-Only
12	TPC Timer Register	TPC	Read-Only
13	TNE Timer Register	TNE	Read-Only
14	Clock Divider Register	CLK_DIV	Read-Only
15	BIST Signature Register	BIST_SIGNATURE	Read-Only
16	Receive Vector Length Register	RCV_VECTOR	Read-Only
17	Interrupt Event Register	INTR_EVENT	Read-Only
18	Violation Symbol Counter Register	VIOL_SYM_CTR	Read-Only
19	Minimum Idle Counter Register	MIN_IDLE_CTR	Read-Only
1A	Link Error Event Counter Register	LINK_ERR_CTR	Read-Only

3.1 CONTROL AND STATUS REGISTERS

The ELM control and status information is contained in four registers: control register A, control register B, status register A, and status register B.

3.1.1 Control Register A (ELM_CNTRL_A)

Control register A is a read/write register. All bits of this register are cleared with the assertion of $\overline{\text{PWRUP}}$. Control register A is used for the following functions:

- Timer Configuration
- PCM MAINT State Options Specification
- Counter Interrupt Frequency Selection
- ELM Data Path Configuration
- ELM BIST Execution
- Physical Layer Media Dependent Control

Note that several bits of this register can only be set or cleared if the PCM is in the OFF or MAINT state. If this register is written when the PCM is in any other state, these bits will remain unchanged.

15	14	13	12	11	10	9	8
0	NOISE_ TIMER	TNE_16BIT	TPC_16BIT	REQ_SCRUB	ENA_PAR_ CHK	VSYM_CTR_ INTRS	MINI_CTR_ INTRS
7	6	5	4	3	2	1	0
FCG_LOOP_ CNTRL	FOT_OFF	EB_LOC_ LOOP	ELM_LOC_ LOOP	SC_BYPASS	REM_LOOP	RF_DISABLE	RUN_BIST

Bit 15—Reserved

This bit is reserved and should be set to zero.

NOISE_TIMER—Noise Timer

The NOISE_TIMER bit allows the noise timing function of the PCM to be used when the PCM is in the MAINT state. This function causes the TNE timer to be loaded with the value in the noise time register whenever the line state machine transitions from Idle Line State to Noise Line State, Active Line State, or Unknown Line State. If the timer expires before Idle Line State is recognized, the TNE_EXPIRED bit in the interrupt event register is set.

TNE_16BIT—TNE 16-Bit Timer

When TNE_16BIT is set, it causes the TNE timer to operate as a 16-bit timer. In this mode, the two bits of the TNE clock divider are bypassed, and the TNE timer is incremented every 80 ns. TNE_16BIT can only be written if the PCM is in the OFF or MAINT state.

TPC_16BIT—TPC 16-Bit Timer

When TPC_16BIT is set, it causes the TPC timer to operate as a 16-bit timer. In this mode, the eight bits of the TPC clock divider are bypassed, and the TPC timer is incremented every 80 ns. TPC_16BIT can only be written if the PCM is in the OFF or MAINT state.

REQ_SCRUB—Request Scrub

The REQ_SCRUB bit allows limited access to the scrub capability of the ELM chip. If the PCM is in the MAINT state or if the CONFIG_CNTRL bit is set in control register B, then REQ_SCRUB controls the scrub MUX. If REQ_SCRUB is set, then I-symbols are sourced at the RCDATx port. The output at the TDATAx port is controlled separately by the MAINT_LS field in control register B. This bit may be written at any time, but only takes effect when the PCM is in the MAINT or OFF state.

ENA_PAR_CHK—Enable Parity Check

0 = Parity checking is disabled.
1 = Parity checking is enabled.

This bit is initialized to zero on power-up reset.

VSYM_CTR_INTRS—Violation Symbol Counter Interrupt

The VSYM_CTR_INTRS bit controls when the VSYM_CTR interrupt bit in the interrupt event register is set. When VSYM_CTR_INTRS is set, the interrupt is generated only when the violation symbol counter register overflows (reaches 256). When VSYM_CTR__INTRS is cleared, the interrupt is generated every time the violation symbol counter register is incremented whenever a V-symbol pair is detected.

MINI_CTR_INTRS—Minimum Idle Counter Interrupt

The MINI_CTR_INTRS bit partially controls the MINI_CTR interrupt bit in the interrupt event register.

0 = The interrupt is generated every time the counter is incremented (whenever a minimum length idle gap is detected). This bit does not affect interrupts caused by the idle counter minimum detector portion (bits 6–4) of the minimum idle counter register.
1 = The interrupt is generated when the minimum idle gap counter portion (bits 3–0) of the minimum idle counter register overflows (reaches 16).

FCG_LOOP_CNTRL—FCG Loopback Control

When FCG_LOOP_CNTRL is set, it causes the LOOPBACK output pin to be asserted low, which, in turn, causes data to be looped back from the output of the FCG to the input of the FCG.

FOT_OFF—Fiber-Optic Transmitter Off

Setting FOT_OFF is one of several conditions will cause the assertion of the ELM $\overline{\text{FOTOFF}}$ output pin.

EB_LOC_LOOP— Elasticity Buffer Local Loopback

When EB_LOC_LOOP is set, a loopback path is set up in the ELM chip just prior to the ELM-to-FCG interface. Data from TXDATx is passed through the ELM transmit path and looped back to the input of the framer at the elasticity buffer local loopback MUX. Note that this bit also controls which clock the framer and elasticity buffer use. When it is not set, the RSCLK is used. Thus, when this bit is set, a clock glitch could be created, causing receive data to be indeterminate for a clock cycle or causing spurious interrupts and unknown values in the even counters. EB_LOC_LOOP can only be set or cleared if the PCM is in the OFF or MAINT state.

ELM_LOC_LOOP—ELM Local Loopback

When ELM_LOC_LOOP is set, a loopback path is set up in the ELM so that data from TXDATx is passed through the transmit path and looped back to the input of the receive path at the LM local loopback MUX. ELM_LOC_LOOP can only be set or cleared if the PCM is in the OFF or MAINT state.

SC_BYPASS—Scrub/Bypass

The SC_BYPASS bit provides limited control over the data path by furnishing a physical bypass of the ELM. If the PCM is in the MAINT state or if the CONFIG_CNTRL bit in control register B is set, the SC_BYPASS bit controls the bypass MUX. If both SC_BYPASS and REQ_SCRUB are set, then RCDATx is driven with I-symbols. If SC_BYPASS is set and REQ_SCRUB is cleared, then RCDATx is driven by the data entering the ELM at the TXDATx input. Otherwise, RCDATx is driven by the data entering the ELM at the RDATAx input. If the CONFIG_CNTRL bit is set and the PCM is not in the MAINT state, the REQ_SCRUB bit has no effect, and only SC_BYPASS controls the data output on RCDATx. This bit may be set or cleared at any time, but only takes effect when the PCM is in the MAINT state or if the CONFIG_CNTRL bit in control register B is set.

SC_BYPASS	REQ_SCRUB	RCDATx
0	0	RDATAx
0	1	RDATAx
1	0	TXDATx
1	1	I-Symbols

When used in concentrator applications, the SC_BYPASS bit provides for isolation of the PHYs. The data is latched only once; therefore, there is only a 1-byte clock delay through a bypased ELM.

REM_LOOP—Remote Loopback

When REM_LOOP is set, a remote loopback path is set up inside the ELM whereby symbols from the receive data path are looped back onto the transmit data path, traversing both paths except for the scrub MUX, bypass MUX, RCDATx latch, and the TXDATx latch. If the PCM is in the MAINT state or if the CONFIG_CNTRL bit in control register B is set, the REM_LOOP bit controls the remote loopback MUX. The PCM uses

this loopback to control the configuration during normal operation. This bit has no effect if the ELM_LOC_LOOP bit is set. This bit may be set or cleared at any time, but only takes effect when the PCM is in the MAINT state or if the CONFIG_CNTRL bit in control register B is set.

RF_DISABLE—Repeat Filter Disable

When RF_DISABLE is set, it disables the ELM repeat filter state machine.

RUN_BIST—Run Built-In Self-Test

When RUN_BIST is set, it causes the ELM to begin running BIST. The completion of BIST is indicated via an interrupt. BIST can be stopped before completion by clearing this bit. Once BIST has completed, this bit must be cleared and set again before BIST will restart.

3.1.2 Control Register B (ELM_CNTRL_B)

Control register B is a read/write register. All bits of this register are cleared with the assertion of $\overline{\text{PWRUP}}$. Control register B contains signals and requests to direct the PCM process. It is also used to control the line state match interrupt.

15	14			11	10		8
CONFIG_ CNTRL	MATCH_LS				MAINT_LS		
7	6	5	4	3	2	1	0
CLASS_S	PC_LOOP		PC_JOIN	LONG	PC_MAINT	PCM_CNTRL	

CONFIG_CNTRL—Configuration Control

The CONFIG_CNTRL bit allows control over the bypass MUX and remote loopback MUX while the PCM is in normal operation.

0 = The SC_BYPASS and REM_LOOP bits only have an effect if the PCM is in the MAINT state.

1 = The SC_BYPASS and REM_LOOP bits in control register A have an effect regardless of the state of the PCM.

MATCH_LS—Match Line State

The MATCH_LS field specifies the line state to be compared with the currently detected line state (defined by LINE_ST in status register A). When a match occurs, the LS_MATCH bit in the interrupt event register is set. Each bit of MATCH_LS corresponds to a line state. If more than one bit is set, the interrupt is signaled if any of the line states match the current line state. If no bits are set, the interrupt is signaled on any change in the LINE_ST field or the UNKN_LINE_ST bit. MATCH_LS is further defined as follows:

0000 = Interrupt on Change in LINE_ST or UNKN_LINE_ST
1XXX = Interrupt on Quiet Line State
X1XX = Interrupt on Master Line State
XX1X = Interrupt on Halt Line State
XXX1 = Interrupt on Idle Line State

In the above list, X means don't care. Also, Idle Line State refers to ILS16, which is signaled only after 16 I-symbols (eight I-bytes) have been received.

MAINT_LS—MAINT Line State

The MAINT_LS field defines the line state the PCM will source while in the MAINT state. The PCM enters the MAINT state from the OFF state if the PC_MAINT bit is set. MAINT _LS is further defined as follows:

000 = Transmit_Quiet Line State
001 = Transmit_Idle Line State
010 = Transmit_Halt Line State
011 = Transmit_Master Line State
100 = Transmit_Quiet Line State
101 = Transmit_Quiet Line State
110 = Transmit_PDR (Transmit PHY_DATA request. The symbol pair at TXDATx is transmitted.)
111 = Transmit_Quiet Line State

CLASS_S—Class Slave

When CLASS_S is set during configuration (i.e., PHY is a single attach station and PCM is not yet in ACTIVE state), the station will be not be bypassed—i.e., data coming from the MAC to the ELM will not be looped back to the MAC. Normally, this bit would not be set for A, B, and M type PHYs, in which case the ELM will be bypassed anytime the PCM is not in the ACTIVE or TRACE state. This bit has an effect when the PCM is in normal operation. When the PCM is in the MAINT state, the REQ_SCRUB and SC_BYPASS bits in control register A control the scrubbing and bypass operation. This bit can only be changed when the PCM is in the OFF state. If this register is set or cleared when the PC is in any other state, this bit will remain unchanged.

PC_LOOP—Physical Connection Loopback

PC_LOOP controls the loopback used in the Link Confidence Test. When it is set to a value other than zero and the PCM is in the NEXT state, the PCM will set the TDF flag and perform the Link Confidence Test in one of three ways. The action taken according to the value of these two bits is defined as follows:

00 = No Link Confidence Test is performed.
01 = The PCM sets Transmit_PDR, which assumes that protocol data units will be input at TXDATx.
10 = The PCM sets Transmit_Idle, which causes the ELM to source I-symbols.
11 = The PCM sets Transmit_PDR and sets up a remote loopback path in the ELM.

PC_LOOP should only be set or cleared after the PCM_CODE interrupt has been generated. If the PCM is not in the NEXT state or if PCM_SIGNALING is set, then any value written to the field is ignored. Once PC_LOOP has been written, it must be cleared and written again to perform another Link Confidence Test.

PC_JOIN—Physical Connection Join

When PC_JOIN is set and the PCM is in the NEXT state, the PCM will transition to the JOIN state and the PCM join sequence will be started. PC_JOIN should only be written after the PCM_CODE interrupt has been generated. If the PCM is not in the NEXT state or if PCM_SIGNALING is set, then any value written to this bit is ignored. After this bit has been set, it must be cleared and then set again to cause another transition from the NEXT state to the JOIN state. Note that if PC_JOIN is set after the Link Confidence Test has been started but before it has completed, the test will be aborted and the PCM join sequence will be initiated.

LONG—Long Link Confidence Test

When LONG is set, the PCM will perform a long Link Confidence Test—that is, it will continue the test until the processor issues a PC_SIGNAL, PC_JOIN, or other command. Otherwise, it will perform a short Link Confidence Test—that is, it will stop the test after the length of time indicated in the LC_SHORT time parameter. The Link Confidence Test will halt whenever Master Line State or Halt Line State are recognized, which indicates that the neighbor PHY has completed its Link Confidence Test.

PC_MAINT—PCM MAINT State

When PC_MAINT is set, the PCM state machine transitions to the MAINT state if it is currently in the OFF state. If the PCM is not in the OFF state when this bit is set, it will immediately transition to the MAINT state when the OFF state is reached.

PCM_CNTRL—PCM Control

PCM_CNTRL controls the PCM state machine. When this bit is set to a value other than zero, it causes the PCM to immediately transition to the BREAK, TRACE, or OFF state. The transition to the BREAK or OFF state occurs regardless of the PCM state at the time. The transition to the TRACE state only occurs if the PCM is in the ACTIVE state; otherwise, PCM_CNTRL is ignored. This field must first be cleared and then written with another value to cause another transition. The following action is taken according to the value of these two bits:

00 = The PCM state is not affected.
01 = The PCM goes to BREAK state (PC_Start).
10 = The PCM goes to the TRACE state (PC_Trace).
11 = The PCM goes to the OFF state (PC_Stop).

Note that if the PCM goes to the BREAK state for a reason other than writing PCM_CNTRL (e.g., Quiet Line State is received or a time-out occurs), the PCM will not go to the CONNECT state and will remain in the BREAK state until PCM_CNTRL is written with the PC_Start value. If the PCM goes from the ACTIVE state to the BREAK state, it will scrub the ring before leaving the BREAK state. If the PC_Start value is written to PCM_CNTRL while scrubbing is being performed, the scrubbing will complete before the PCM goes to the CONNECT state.

3.1.3 Status Register A (ELM_STATUS_A)

Status register A, which is read-only, is used to report status information about the line state machine through the node processor.

15	14	13 … 11	10	9 … 8
0	0	ELM_REV_NO	SIGNAL_ DETECT	PREV_LINE_ST

7 … 5	4	3	2 … 0
LINE_ST	LSM_STATE	UNKN_LINE _ST	SYM_PR_CTR

Bits 15–14—Reserved

These bits are reserved and are set to zero.

ELM_REV_NO—ELM Revision Number

000= ELM Revision A
001= ELM Revision B

SIGNAL_DETECT—Signal Detect Value

This bit contains the value on the SD input pin.

PREV_LINE_ST—Previous Line State

This field contains the value of the previous line state whenever line state changes from Quiet, Master, Halt, or Idle (ILS16, where ILS16 is achieved after 16 I-symbols) to another line state occur. When the line state changes from anything else, this field is not updated. These two bits are defined as follows:

00 = Quiet Line State
01 = Master Line State
10 = Halt Line State
11 = Idle Line State (ISL16 achieved after 16 I-symbols)

LINE_ST—Current Line State

This field contains the most recently recognized line state by the line state machine. LINE_ST is further defined as follows:

000 = Noise Line State
001 = Active Line State
010 = Reserved
011 = Idle Line State (ILS4 achieved after 4 I-symbols)
100 = Quiet Line State
101 = Master Line State
110 = Halt Line State
111 = Idle Line State (ILS16 achieved after 16 I-symbols)

LSM_STATE—Line State Machine State

This field contains the state bit of the line state machine.

0 = Not Active Line State
1 = Active Line State

UNKN_LINE_ST—Unknown Line State

This bit is the Unknown Line State indication.

0 = Line State Known
1 = Line State Unknown

SYM_PR_CTR—Symbol Pairs Counter

This field contains the line state machine symbol pairs counter. When the count reaches seven, indicating eight consecutive like symbol pairs, then LINE_ST is set with the new line state, and the UNKN_LINE_ST bit is reset. Note that Idle Line State is reached after just two I-symbol pairs.

3.1.4 Status Register B (ELM_STATUS_B)

Status register B, which is read-only, contains signals and status from the repeat filter and PCM state machine.

15	14	13	12	11	10	8
RF_STATE		PCI_STATE		PCI_SCRUB	PCM_STATE	

7	6	5	4	3	2	0
PCM_STATE	PCM_ SIGNALING	LSF	RCF	TCF	BREAK_REASON	

RF_STATE—Repeat Filter State

This field contains the state bits of the repeat filter state machine. The states are defined as follows:

00 = REPEAT
01 = IDLE
10 = HALT1
11 = HALT2

PCI_STATE—Physical Connection Insertion State

This field contains the state bits of the PCI state machine. The states are defined as follows:

00 = REMOVED
01 = INSERT_SCRUB
10 = REMOVE_SCRUB
11 = INSERTED

PCI_SCRUB—Physical Connection Insertion Scrub

This flag indicates that the scrubbing function is operating—that is, I-symbol pairs are being sourced on the RCDATx output pins.

PCM_STATE—Physical Connection Management State

This field contains the state bits of the PCM state machine. The states are defined as follows:

0000 = PC0 (OFF)
0001 = PC1 (BREAK)
0010 = PC2 (TRACE)
0011 = PC3 (CONNECT)
0100 = PC4 (NEXT)
0101 = PC5 (SIGNAL)
0110 = PC6 (JOIN)
0111 = PC7 (VERIFY)
1000 = PC8 (ACTIVE)
1001 = PC9 (MAINT)
1010–0111 = Reserved

PCM_SIGNALING—Physical Connection Management Signaling

This PCM flag indicates that the transmit vector register has been written and the PCM is in the process of transmitting these bits to its neighboring PCM. The transmit vector register cannot be written when this flag is set.

LSF—Line State Flag

The PCM uses this bit to indicate that a given line state has been received since entering the current state. It is cleared on every change of PCM state.

RCF—Receive Code Flag

The PCM uses this bit to indicate that the receive logic has started execution. This flag is used to prevent the receive station management PCM code from being started multiple times while in the NEXT state.

TCF—Transmit Code Flag

The PCM uses this flag to indicate that the transmit logic has started execution. This flag is used to prevent the transmit station management PCM code from being started multiple times while in the NEXT state.

BREAK_REASON—Break Reason

This field, which indicates the reason for the PCM state machine's last transition to the BREAK state, is defined as follows:

000 = The PCM state machine has not gone to the BREAK state
001 = PC_START Issued
010 = TPC Timer Expired after T_OUT
011 = TNE_Timer Expired after NS_MAX
100 = Quiet Line State Detected
101 = Idle Line State Detected
110 = Halt Line State Detected
111 = Reserved

3.2 PCM TIMERS

The PCM utilizes two timers, TPC_TIMER and TNE_TIMER, to track PCM timing parameters. Both timers have a clock divider circuit to reduce the frequency at which they are incremented.

3.2.1 TPC Timer

In normal operation, the TPC timer is in 16-bit mode and is read-only by the node processor. The TPC timer value is read at address 12 (hex). When the PCM is in the MAINT state and the PCI_SCRUB bit in status register B is cleared, a value can be written to the TPC load value register at address 0E. The TPC timer is incremented by the output of an 8-bit clock divider circuit and is therefore incremented every 20.48 μs, (2^8 x 80 ns). The instantaneous value in the TPC clock divider is contained in bits 7–0 of the CLK_DIV register, which can be read at address 14 (hex).

The TPC timer is used to ensure that state transitions proceed at the desired rate while the PCM is attempting to establish a physical connection with a neighboring PCM.

The timer is loaded with a twos complement value and counts up until it reaches zero. In normal operation, the timer is loaded by the PCM from the relevant timing parameter register, which contains the twos complement of the time value in 20.48-μs units. At the same time the TPC timer is loaded with each parameter, the TPC clock divider is initialized to zero.

By using the AUTO_SCRUB bit in control register A, the TPC timer can be used to time the scrub function when the PCM is in the MAINT state without the timer having to be explicitly loaded by the node processor. When the AUTO_SCRUB function is in use, the node processor should not attempt to load the TPC timer while the PCI_SCRUB bit in status register B is set. If this condition is violated, the NP_ERR bit in the interrupt event register will be set, and the timer will not be loaded.

For test purposes, the timer can also be used in 16-bit mode, in which the TPC clock divider is bypassed and the timer is incremented every 80 ns when in operation. In this mode, the value loaded into the timer is the twos complement of the remaining time in 80-ns units. This feature is controlled by TPC_16BIT in control register A.

3.2.2 TNE Timer

In normal operation, the TNE timer is in 16-bit mode and is read-only by the node processor. The value of the TNE timer can be read at address 13 (hex). When the PCM is in the MAINT state and the NOISE_TIMER bit in control register A is not set, a value can be written to the TNE register by writing TNE load value register at address 0F. The TNE timer, which is incremented by the output of a 2-bit clock divider circuit, is incremented every 0.32 μs (2^2 x 80 ns). The instantaneous value in the TNE clock divider is contained in bits 9 and 8 of the CLK_DIV register, which can be read at address 14 (hex).

The TNE timer is used to time the length of (potential) noise while the PCM is in the ACTIVE state. The TNE timer is started whenever the line state machine transitions from Idle Line State to Noise Line State, Active Line State, or Unknown Line State. If the timer expires before the PCM line state machine recognizes Idle Line State again, the PCM transitions to the BREAK state.

The timer is loaded with a twos complement value and counts up until it reaches zero. In normal operation, the timer is loaded by the PCM from the noise time register timing parameter register, which contains the twos complement of the time value in 0.32-μs units, whenever the line state machine leaves Idle Line State. At the same time the TPC timer is loaded, the TNE clock divider is initialized to zero.

When the PCM is in the MAINT state and the NOISE_TIMER bit in control register A is not set, the TNE timer can be loaded directly with a 16-bit value from the node processor (the TNE clock divider is still loaded with zero). If the PCM is not in the MAINT state when

a write is attempted, the NP_ERR bit in the interrupt event register will be set, and the timer will not be loaded.

For testing purposes, the timer can also be used in 16-bit mode, in which the TNE clock divider is bypassed and the timer is incremented every 80 ns when in operation. In this mode, the value loaded into the timer is the twos complement of the remaining time in 80-ns units. This feature is controlled by TNE_16BIT in control register A.

3.3 PCM TIMING PARAMETER REGISTERS

The PCM uses a number of different timing parameter registers when forming a physical connection. These registers, which are readable at any time, are programmable and must be written by the node processor. TPC-based timing parameter registers hold the twos complement of the time in 20.48-μs (2^8 x 80 ns) units. They can have a maximum value of about 1.34 sec (2^{16} x 20.48 μs).

In addition to the TPC timing parameters, there is one timing parameter used by the TNE timer noise time register, which holds the twos complement of the time in 0.32-μs (2^2 x 80 ns) units. It can have a maximum value of about 20.97 ms (2^{16} x 0.32 μs).

3.3.1 Maximum PHY Acquisition Time Register (A_MAX)

The maximum PHY acquisition time register value represents the maximum time required to achieve signal acquisition. This register is used for timing the length of time to remain in the Connect State to ensure correct timing with the neighboring PCM (C_MIN). For an example value of 0.2 ms, the register would be set to FFF6.

3.3.2 Maximum Line State Change Time Register (LS_MAX)

The maximum line state change time register value is the maximum time required for line state recognition. This register is used to set the time required to transmit a given line state before advancing to the next PCM state (TL_MIN). For an example value of 0.02 ms, the register would be set to FFFF.

3.3.3 Minimum Break Time Register (TB_MIN)

The minimum break time register holds the allowable length of time for the PCM to be in the BREAK state before a response is seen on the inbound physical link. This time allows for the possibility of a bypass failure mode in this station or a neighboring station that could cause four PHYs to be connected in a loop and produce an invalid response to the break. In this case, the minimum break time guarantees that the response to the break will propagate around the loop and be seen on the inbound link. For an example with a value of 20 ms, the register would be set to FC2F.

3.3.4 Signaling Time-Out Register (T_OUT)

The signaling time-out register allows for a response reception from a neighboring PCM. When a response is expected and no transition is made in signaling time-out register

time, a transition is made to the BREAK state. For an example value of 100 ms, the register would be set to ECED.

3.3.5 Short Link Confidence Test Time Register (LC_SHORT)

The short Link Confidence Test time register specifies the time duration of the Link Confidence Test. It limits the loopback to prevent deadlock. For an example value of 50 ms, the register would be set to F676.

3.3.6 Scrub Time Register (T_SCRUB)

The scrub time register is used in the PCI process (see **Section 2 Functional Description**). For an example value of 3 ms, the register would be set to FF6D. T_SCRUB is the same as the MAC TVX time.

3.3.7 Noise Time Register (NS_MAX)

The noise time register holds the maximum length of time that noise is tolerated before a connection is broken down. For an example value of 2 ms, the register would be set to E796.

Table 3-2 summarizes calculated value examples for the timing parameter registers. The ANSI FDDI SMT document contains a set of values for these parameters.

Table 3-2. Register Values

Parameter	Recommended Value (ms)	Register Value (Twos Comp/Hex)	Timer
A_MAX	0.2	FFF6	TPC
LS_MAX	0.02	FFFF	TPC
TB_MIN	20	FC2F	TPC
T_OUT	100	ECED	TPC
LC_SHORT	50	F676	TPC
T_SCRUB	3	FF6D	TPC
NS_MAX	2	E796	TNE

3.4 PCM BIT SIGNALING REGISTERS

The ELM contains three registers used by the PCM to perform bit signaling. Bit signaling is the mechanism the PCM uses to transfer information to the PCM in the neighboring station.

3.4.1 Transmit Vector Register (XMIT_VECTOR)

All bits of the read/write transmit vector register are cleared with the assertion of $\overline{\text{PWRUP}}$. The transmit vector register is writable only when the PCM_SIGNALING bit in status

register B is cleared; otherwise, the register will not be written and the NP_ERR bit in the interrupt event register will be set. This register is readable at any time.

The transmit vector register contains from 1 to 16 bits of data to be transmitted from the PCM to its neighboring PCM. Bits are transmitted one at a time by the bit signaling mechanism. A one is represented by the transmission of Halt Line State and a zero by the transmission of Master Line State. Bit 0 of this register is the first bit to be transmitted, then bit 1, etc., up to the number of bits specified in the transmit vector length register.

The transmit vector length register should be written before this register is written. When a write is made to this register, the transmit vector length register is sampled to determine the number of bits to transmit.

3.4.2 Transmit Vector Length Register (VECTOR_LENGTH)

The transmit vector length register is cleared with the assertion of $\overline{\text{PWRUP}}$. This register is sampled when the transmit vector register is written. Thus, although this register is writable at any time, only the last value written before the transmit vector register is written will affect the operation of the PCM.

Bits 15–4 are unused and will always be read as zeros. Any value written to these bits will be ignored.

Bits 3–0 contain the number of bits to be transmitted. The value in this field (0 to 15) is actually one less than the number of bits to transmit (1 to 16).

3.4.3 Receive Vector Register (RCV_VECTOR)

The read-only receive vector register contains from 1 to 16 bits of data received from the neighboring PCM. Bits are received at the same time bits are being transmitted. As bit n is received, it is placed in the receive vector register. If Halt Line State is received, bit n is a one; if Master Line State is received, bit n is a zero. Bit 0 of this register is the first bit received, then bit 1, etc., up to the number of bits specified in the transmit vector length register.

Although this register is readable at any time, if PCM_SIGNALING is asserted when this register is read, the data may be incomplete.

3.5 EVENT COUNTERS

The ELM contains three event counter registers and one threshold value register used for gathering information about errors occurring on its associated physical link and for monitoring I-symbol gaps between packets.

3.5.1 Violation Symbol Counter (VIOL_SYM_CTR)

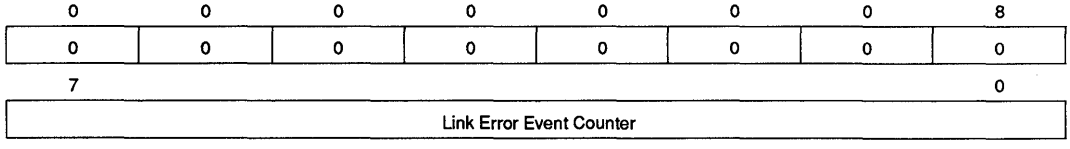
The violation symbol counter has address 18 (hex). It is read-only and is cleared whenever it is read as well as when $\overline{\text{PWRUP}}$ is asserted. The high-order 8 bits always read as zeros; the low-order 8 bits contain the counter value. The VSYM_CTR bit in the

interrupt event register is set whenever the counter increments or whenever the counter overflows (reaches 256), depending on the setting of the VSYM_CTR_INTRS bit in control register A. When the counter overflows (reaches 256), it wraps to zero and continues to count.

The violation symbol counter is incremented whenever the 4B/5B decoder in the ELM decodes a V-symbol. See Table 2-1 for the symbols considered to be V-symbols by the decoder.

3.5.2 Link Error Event Counter (LINK_ERR_CTR)

The link error event counter has address 1A (hex). It is read-only and is cleared whenever it is read as well as when $\overline{\text{PWRUP}}$ is asserted. An 8-bit counter is contained in bits 7–0. Bits 15–8 of the register always read as zeros. The LE_CTR bit in the interrupt event register is set whenever the counter reaches the value contained in the link error event threshold register. The counter will continue to count past this point. When the counter overflows (reaches 256), it wraps to zero and continues to count.



Before the PCM is active, the link error event counter is used by the internal PCM hardware to perform the Link Confidence Test. The number of errors that the user wants the Link Confidence Test to accept should be initialized into the link error event threshold register. If the Link Confidence Test is performed and the link error event threshold is not reached, then the test passed. The test result is given to the software, which then makes the decision as to the next step.

The link error event counter is part of the LEM. The LEM monitors the bit error rate of an active link and detects and isolates physical links having an inadequate bit error rate, possibly due to a marginal link quality, link degradation, or connector unplugging.

In addition to the counter, the ELM also contains logic to detect link error events. Link error events are defined as:

- Transitions from Idle Line State to Unknown Line State or Noise Line State.
- Transitions from Active Line State to Unknown Line State or Noise Line State with the duration of Unknown Line State or Noise Line State exceeding eight symbol times (320 ns).

The link error event counter is only incremented by the LEM when a link error occurs and the PCM state machine is in NEXT or ACTIVE state.

3.5.3 Link Error Event Threshold Register (LE_THRESHOLD)

The read/write link error event threshold register is cleared when $\overline{\text{PWRUP}}$ is asserted. Bits 7–0 of this register contain a value that controls when the LE_CTR bit in the interrupt event register is set. Whenever the value in the link error event counter reaches the value contained in this register, the LE_CTR bit is set. Bits 15–8 always read as zeros.

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0

7	0
Link Error Event Threshold Value	

3.5.4 Minimum Idle Counter (MIN_IDLE_CTR)

The read-only minimum idle counter is cleared whenever it is read as well as when $\overline{\text{PWRUP}}$ is asserted. The high-order 9 bits of the register always read as zeros.

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0

7	6	4	3	0
0	Idle Counter Minimum Detector		Minimum Idle Gap Counter	

Bits 6–4 of the counter contain the value in the idle counter minimum detector. This is the minimum number of interpacket I-symbol pairs seen since the counter was last reset. It gets reset to 7. Whenever the value changes to a lower value, the MINI_CTR bit in the interrupt event register is set. The counter is a gray code counter. The I-symbol pair count definitions are given in Table 3-3.

Table 3-3. I-Symbol Pair Count

MIN_IDLE_CTR (6–4)	I-Symbol Pair Count
100	7 or more
101	6
111	5
110	4
010	3
011	2
001	1
000	0

Bits 3–0 of the counter contain the value in the minimum idle gap counter. This is the number of times the minimum number of interpacket idles has been seen since the last reset. It gets reset to zero. The MINI_CTR bit in the interrupt event register is set whenever the counter increments or whenever the counter overflows (reaches 16), depending on the setting of the MINI_CTR_INTRS bit in the control register A. When the counter overflows, it remains at 16. The minimum idle occurrence count definitions are given in Table 3-4.

Table 3-4. Minimum Idle Occurrence Count

MIN_IDLE_CTR (3–0)	Minimum Idle Occurrence Count
0000	1
1000	2
1100	3
0100	4
0101	5
0111	6
1111	7
1110	8
1010	9
0010	10
0011	11
0001	12
1001	13
1101	14
0110	15
1011	16

This counter can be used to monitor the activity of the smoother. The number of idles should not go below 7. If they do, it may be desirable to monitor this counter.

3.6 INTERRUPT REGISTERS

The ELM has two interrupt registers that correspond to each other on a bit-for-bit basis. One register contains bits set by interrupting events, and the other register contains a mask that enables or disables $\overline{\text{ELMINT}}$ caused by that interrupting event.

3.6.1 Interrupt Event Register (INTR_EVENT)

The read-only interrupt event register is cleared whenever it is read as well as when $\overline{\text{PWRUP}}$ is asserted. The ELM uses this register to report individual events to the node processor. When an interrupt is generated via the $\overline{\text{ELMINT}}$ pin, the node processor should read this register to find the source(s) of the interrupt.

While the RUN_BIST bit in control register A is set, all interrupts are masked except BIST_DONE. Since BIST_DONE is the only interrupt that can occur in this situation, BIST_DONE does not have a bit in the interrupt event register. This interrupt is cleared by clearing the RUN_BIST bit in control register A.

15	14	13	12	11	10	9	8
NP_ERR	LSD	LE_CTR	MINI_CTR	VSYM_CTR	PHYINV	EBUF_ERR	TNE_ EXPIRED
7	6	5	4	3	2	1	0
TPC_ EXPIRED	PCM_ ENABLED	PCM_ BREAK	SELF_TEST	TRACE_ PROP	PCM_CODE	LS_MATCH	PARITY_ ERR

NP_ERR—Node Processor Error

This bit indicates that the node processor has requested a read or write to an invalid register. These cases include a write to a read-only register (such as this register), a write to a PCM timing parameter register while the PCM is not in the OFF state, a write to the TPC timer register while the PCM is not in the MAINT state or while PCI_SCRUB is set, and a write to the TNE timer register while the PCM is not in the MAINT state or while NOISE_TIMER is set.

LSD—Loss of Signal Detect

This bit indicates the loss of signal detect—that is, the SD input pin has been negated.

LE_CTR—Link Error Counter

This bit indicates that the link error event counter has reached the value contained in the link error event threshold register.

MINI_CTR—Minimum Counter

This bit indicates that either event or both events have occurred in the minimum idle counter register: the idle counter minimum detector has changed to a lower value or the minimum idle gap counter has incremented or overflowed (depending on the MINI_CTR_INTRS bit in control register A).

VSYM_CTR—Violation Symbol Counter

This bit indicates that the violation symbol counter has incremented or overflowed (depending on the VSYM_CTR_INTRS bit in control register A).

PHYINV—Physical Layer Invalid

This bit indicates that the physical layer invalid signal has been asserted by the PCM.

EBUF_ERR—Elasticity Buffer Error

This bit indicates that the elasticity buffer has experienced an overflow or an underflow. EBUF_ERR is only reset after recognition of Idle or Active Line States. This bit is usually masked during PCM operation.

TNE_EXPIRED—TNE Timer Expired

This bit indicates that the TNE timer has expired—i.e., reached zero.

TPC_EXPIRED—TPC Timer Expired

TPC_EXPIRED indicates that the TPC timer has expired—i.e., reached zero.

PCM_ENABLED—Physical Connection Management Enabled

PCM_ENABLED indicates that the PCM has asserted CF_JOIN (ANSI state transition PC(88b)), has completed scrubbing (for class M, A, or B stations), and is in the ACTIVE state.

PCM_BREAK—Physical Connection Management Break

This bit indicates that the PCM has entered the BREAK state.

SELF_TEST—Self-Test

This bit indicates that a Quiet or Halt Line State has been received while the PCM is in the TRACE state.

TRACE_PROP—Trace Propagate

This bit indicates that a Master Line State has been received while the PCM is in the ACTIVE or TRACE state.

PCM_CODE—Physical Connection Management Code

PCM_CODE indicates that the PCM has completed transmitting the last bit in the vector written to the transmit vector register and has received the corresponding bit of the receive vector length register or that the Link Confidence Test has been completed.

LS_MATCH—Line State Match

This bit indicates that the line state detected equals the line state in the MATCH_LS field of control register B.

PARITY_ERR—Parity Error

This bit indicates that a parity error has been detected on the TXDATx input pins. The parity feature was designed for ELMs implemented in a concentrator. Since there is no parity feature between the MAC and the ELM, this bit should be masked when the ELM is used in an end station. The frame data is protected by the FCS field when the data path is between the ELM and the MAC.

3.6.2 Interrupt Mask Register (INTR_MASK)

The read/write interrupt mask register is cleared with the assertion of $\overline{\text{PWRUP}}$. It allows the disabling of interrupts caused by specific events. The interrupt mask register contains a bit that corresponds to each bit of the interrupt event register that, when cleared, prohibits that condition from causing an interrupt to the node processor. For each bit set, the setting of the corresponding bit in the interrupt event register will generate an interrupt to the node processor via the $\overline{\text{ELMINT}}$ pin. Note, however, that the operation of a bit in the interrupt event register remains unchanged by the state of the corresponding bit in the interrupt mask register.

3.7 BUILT-IN SELF-TEST SIGNATURE REGISTER (BIST_SIGNATURE)

In addition to a bit in the ELM control register and a bit in each interrupt register, BIST requires one register, the BIST signature register. This 16-bit read-only register contains the resultant signature after execution of the chip's self-test. Refer to **Section 7 Test Operation** for further details.

SECTION 4
SIGNAL DESCRIPTION

The ELM contains 76 signal pins and 44 power and ground pins. A functional pinout diagram is shown in Figure 4-1. A description of each pin is given in the following paragraphs. Note that all outputs are CMOS level and are compatible with TTL inputs.

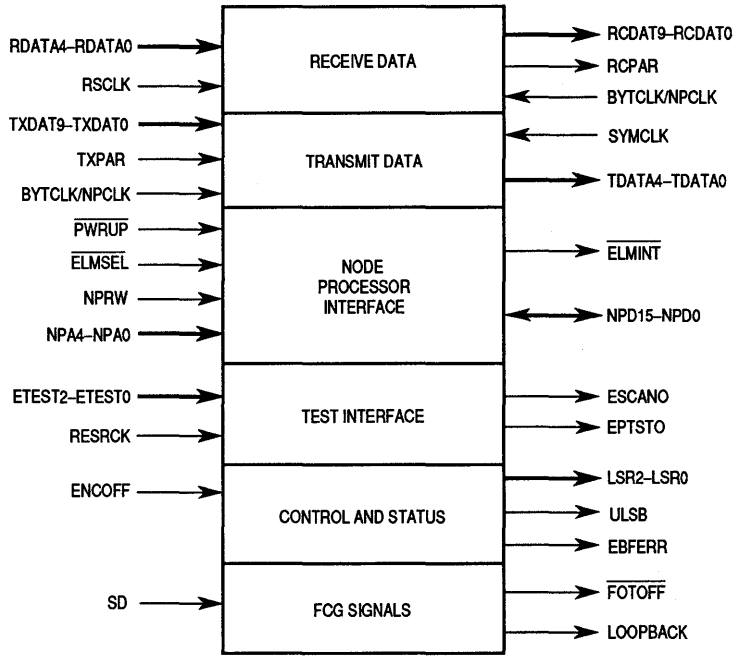


Figure 4-1. ELM Functional Pinout

4.1 CLOCK SIGNALS

The ELM contains the following clock signals.

Recovered Symbol Clock (RSCLK)

RSCLK is a 25-MHz TTL-level input signal driven from a clock recovery circuit or chip. RSCLK is used to latch data received on RDATAx and to operate the elasticity buffer.

Symbol Clock (SYMCLK)

SYMCLK is a 25-MHz TTL-level input signal used to clock TDATAx. It is used along with BYTCLK to latch data received on TXDATx.

Byte Clock (BYTCLK)

BYTCLK is a 12.5-MHz TTL-level input signal used to clock most internal operations and to provide synchronization for data framing. It is used along with SYMCLK to latch data received on TXDATx.

Node Processor Clock (NPCLK)

This TTL-level input signal is used to latch node processor inputs, run the NPI state machine, and clock output signals to the node processor. It is separated from the BYTCLK for test and diagnostic purposes only. By running the BYTCLK at a much slower rate than the NPCLK, several node processor byte transactions can occur while the ELM is essentially halted. For normal operation, BYTCLK and NPCLK **must** be tied together. A small amount of skew (see **Section 5 Bus Operation)** can be tolerated between these two clocks, both in normal operating mode and in test/diagnostic mode.

4.2 RECEIVE DATA SIGNALS

The ELM contains the following receive data signals.

Ring Receive Data Bus (RDATAx)

This TTL-level parallel input bus receives unframed data from the FCG receiver section synchronously with the rise of RSCLK.

Receive Data Bus (RCDATx)

This CMOS-level output bus is used to transfer symbol pairs to the MAC or, in the case of a concentrator, from one ELM to another ELM. The 10 bits are clocked to the MAC on the rising edge of BYTCLK. Bits 9–5 of the bus contain the first symbol (i.e., the symbol read following the rising edge of BYTCLK), and bits 4–0 contain the second symbol.

Receive Data Parity (RCPAR)

This CMOS-level output signal is the odd parity of the RCDATx bus.

4.3 TRANSMIT DATA SIGNALS

The ELM contains the following transmit data signals.

Ring Transmit Data Bus (TDATAx)

This CMOS-level parallel output bus transmits data to the FCG transmitter section.

Transmit Data Bus (TXDATx)

This CMOS-level input bus is used to transfer symbol pairs from the MAC or, in the case of a concentrator, from one ELM to another ELM. The 10 bits are first latched by the ELM on the falling edge of SYMCLK; they are then latched by the rising edge of BYTCLK for use inside the ELM. This double latching is performed to provide adequate hold time for the data relative to BYTCLK. Bits 9–5 of the bus contain the first symbol to be transmitted, and bits 4–0 contain the second symbol.

Transmit Data Parity (TXPAR)

This CMOS-level input signal is the odd parity of the TXDATx bus.

4.4 NODE PROCESSOR INTERFACE SIGNALS

The ELM contains the following NPI signals.

ELM Select ($\overline{\text{ELMSEL}}$)

This input signal selects the ELM for the current NPI bus cycle. This TTL-level signal is asserted low.

Node Processor Read/Write (NPRW)

This TTL-level input signal indicates whether the current bus cycle is a read (NPRW = 1) or a write (NPRW = 0).

Node Processor Address Bus (NPA4–NPA0)

This TTL-level input bus is used to select one of the ELM registers for a read or write cycle.

Power-Up Reset ($\overline{\text{PWRUP}}$)

This TTL-level input signal provides a means of initializing the ELM on power-up. When this signal is negated, the ELM is ready to begin normal operation. When this signal is asserted, it causes the following actions:

- The NPI, PCI, and BIST state machines are initialized to their idle state.
- All writable registers and all registers cleared on a read are cleared.
- The $\overline{\text{FOTOFF}}$ signal is asserted, Q-symbols are transmitted on TDATAx, and TXDATx is looped back onto RCDATx.

$\overline{\text{PWRUP}}$ is asserted low to the ELM. Once asserted, it must remain asserted for at least 10 NPCLK cycles. Assertion and negation are asynchronous, although a warm reset ($\overline{\text{PWRUP}}$ assertion after the chip is operational) will cause unpredictable chip outputs for a few clock cycles until the chip is initialized.

Node Processor Data Bus (NPD15–NPD0)

This TTL-level, 16-bit, bidirectional, three-state data bus is used to exchange data between the ELM and the node processor.

ELM Interrupt ($\overline{\text{ELMINT}}$)

This output signal indicates an interrupt request from the ELM. This CMOS-level signal is asserted low.

4.5 TEST SIGNALS

The ELM contains the following test signals.

ELM Test Mode (ETESTx)

This TTL-level signal is used to select between normal operating mode and three different test modes. See **Section 7 Test Operation** for a detailed discussion of test features.

ELM Scan Output (ESCANO)

This CMOS-level signal is used as an output of the scan chain when the ELM is in boundary scan serial test mode. The signal is otherwise undefined.

4

ELM Parametric Test Output (EPTSTO)

This CMOS-level signal is the output of the NAND tree and 100 inverters required for parametric testing of the chip and for monitoring process variation between chips.

Reset RSCLK (RESRCK)

This signal is used to reset the divide-by-two flip-flop that generates the RSCLK. It is needed for simulation and test purposes only. In actual use, this pin should be tied to ground.

4.6 CONTROL AND STATUS SIGNALS

The ELM contains the following control and status signals.

Line State Register (LSR2–LSR0)

These CMOS-level output signals reflect the state of the status register A LINE_ST field to ring test and monitor equipment.

Unknown Line State Bit (ULSB)

This CMOS-level output signal reflects the state of the status register A UNKN_LINE_ST field to ring test and monitor equipment.

Elasticity Buffer Error Indication (EBFERR)

This CMOS-level output signal is asserted high whenever an underflow or overflow condition is detected. EBFERR is synchronous with the rising edge of BYTCLK.

Encoder Off (ENCOFF)

This input signal controls the encoding/decoding function of the ELM. When ENCOFF is asserted, the encoder and the decoder are disabled, allowing for the transmission of any symbols, including INVALID symbols, for diagnostic purposes. This TTL-level signal is asserted high.

4.7 CLOCK RECOVERY SIGNALS

The ELM contains the following clock recovery signals.

Fiber-Optic Transmitter Off ($\overline{\text{FOTOFF}}$)

$\overline{\text{FOTOFF}}$ is a CMOS-level output signal used to control the fiber-optic transmitter. When asserted low, this signal causes the FCG transmitter to turn off (no light output) the fiber-optic transmitter. This signal is asserted if any of the following conditions occur:

- Either the FOT_OFF bit, the FCG_LOOP_CONTROL bit , or the ELM_LOC_LOOP bit is set in control register A, or
- The MAINT_LS field = Transmit_QUIET and PC_MAINT = ON in control register B, or
- The PCM logic has set LS_REQUEST = Transmit_QUIET, or
- BIST is active.

Signal Detect (SD)

This input signal is an indication from the FCG receiver of the presence of a signal on the media. The value of this signal is held in status register A, and the interrupt event register LSD bit is set whenever SD is asserted. This TTL-level signal is asserted high.

FCG Control Output (LOOPBACK)

This CMOS-level output signal controls the receive symbol multiplexer in the FCG. If LOOPBACK = 0, the MUX selects its input from the FCG transmitter. If LOOPBACK = 1, the MUX selects its input from the fiber-optic receiver.

SECTION 5
BUS OPERATION

The following paragraphs explain the bus operation of the MC68837 ELM.

5.1 NODE PROCESSOR INTERFACE OPERATION

The NPI serves as the interface between an external processor and the control and status registers internal to the ELM. The interface is general purpose in that it is not specific to a processor or family of processors.

The NPI operation is controlled by NPCLK. In normal operation, this clock is the same as the BYTCLK. The two clocks are separate for the purpose of diagnostics and testing; chip operation can be halted by stopping BYTCLK while allowing register reads via NPCLK. All signals in the NPI must be synchronous with the NPCLK—that is, they must be stable a setup time before and a hold time after the rising edge of this clock. **Section 8 Electrical Specifications** lists the definition and value of all timing parameters.

The NPI supports two types of bus transactions: a read cycle and a write cycle. A read or write transaction can occur every two NPCLK cycles (160 ns) although it is possible for the node processor to extend the transaction. Read or write transactions to nonexistent registers, writes to read-only registers, and reads of write-only registers are considered programming errors, and the ELM will ignore the transaction (not drive the data bus on a read or accept data on a write) and set the NP_ERR bit in the interrupt event register. Note that some registers can only be written under certain conditions. If a write is attempted to a register that cannot be written at that time, the NP_ERR bit will be set.

5.2 READ CYCLE

A read cycle is used by the node processor to read data from an ELM register. Some registers are cleared when read.

A read of one of the ELM registers is initiated by the assertion of the $\overline{\text{ELMSEL}}$ signal. The $\overline{\text{ELMSEL}}$ line is sampled by the rising edge of NPCLK (see Figure 5-1). $\overline{\text{ELMSEL}}$ must be asserted a setup time before and must remain asserted for a hold time after this clock edge. The $\overline{\text{ELMSEL}}$ signal may be asserted by the host bus logic to introduce as many wait states as necessary. Once the $\overline{\text{ELMSEL}}$ line is sampled and determined to be asserted, the NPA bus and NPRW line are sampled (NPRW should be high for a read). These signals must also satisfy setup and hold times relative to this same rising edge of NPCLK. At least 40 ns after this clock edge, the ELM will begin to drive the NPD bus. The ELM waits at least 40 ns before driving the bus to allow the chip driving the bus in the previous read or write cycle time to three-state the bus.

After the next rising edge of the NPCLK (the second rising edge after the assertion of $\overline{\text{ELMSEL}}$), the data on the NPD bus will be valid. It will remain valid until after the second rising edge of NPCLK following the negation of $\overline{\text{ELMSEL}}$ The ELM will three-state the NPD bus within 40 ns after this clock edge.

The timing described allows a read cycle to occur every 160 ns. However, if the node processor needs to extend the cycle and have the NPD bus valid longer than one clock cycle, it can delay the negation of $\overline{\text{ELMSEL}}$. For a minimum-length read cycle, the node processor must negate $\overline{\text{ELMSEL}}$ a setup time before the second rising edge of NPCLK following the assertion of $\overline{\text{ELMSEL}}$. If $\overline{\text{ELMSEL}}$ remains asserted for a hold time after the second rising edge of NPCLK, the ELM will continue to drive the NPD bus with valid data. The node processor can extend the read cycle indefinitely by maintaining the assertion of $\overline{\text{ELMSEL}}$.

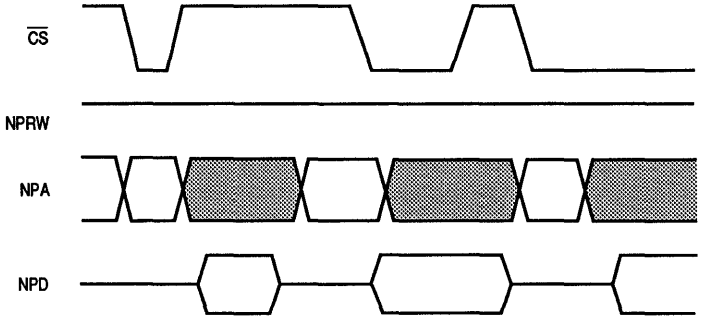


Figure 5-1. Node Processor Bus Read Cycle

5.3 WRITE CYCLE

A write cycle is used by the node processor to write data into an ELM register. It is very similar to the read cycle described above (see Figure 5-2). The principal differences are that (a) the NPRW line must be low a setup time before and a hold time after the first rising edge of NPCLK following the assertion of $\overline{\text{ELMSEL}}$ and (b) the data to be written must be valid a setup time before and a hold time after the second rising edge of NPCLK following the assertion of $\overline{\text{ELMSEL}}$. The host bus logic may assert $\overline{\text{ELMSEL}}$ to introduce as many wait states as necessary. Both the node processor and the ELM must three-state the NPD bus within 40 ns after the second rising edge of NPCLK following the negation of $\overline{\text{ELMSEL}}$. If the node processor delays the negation of $\overline{\text{ELMSEL}}$, the node processor can extend the time it has to three-state the NPD bus. The negation of $\overline{\text{ELMSEL}}$ has no effect on the ELM in a write cycle.

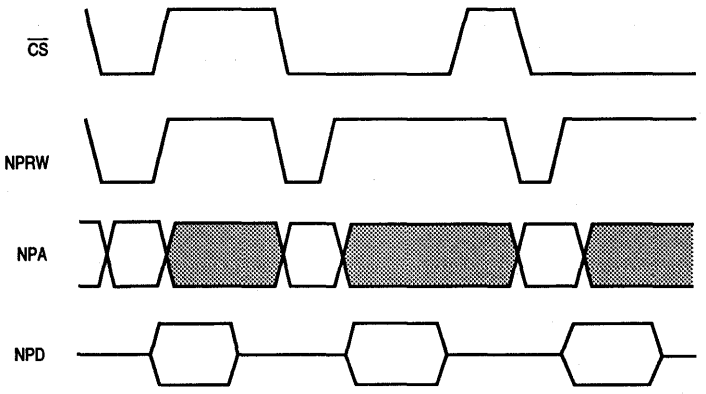


Figure 5-2. Node Processor Bus Write Cycle

5

SECTION 6
LINK MANAGEMENT OPERATION

The ELM provides facilities for CMT and link status indications as set forth in the ANSI FDDI SMT document. CMT defines the operation of PHY insertion and removal, and the connection of PHY entities to the MAC entities. PCM, a subset of CMT, is the management of a physical connection between the PHY being managed and another PHY.

The logic blocks implementing these features are the line states machine, the link error monitor, the data stream generator, and the PCM block. These logic block are discussed in this section.

6.1 LINE STATE MACHINE OPERATION

The line state machine constantly monitors incoming aligned symbol pairs. The current symbol pair is encoded and compared to the encoded value of the previous symbol pair. The symbol pairs are counted until a line state is reached. Once a line state is reached, the counter is stopped, the new line state is stored, and the UNKN_LINE_ST bit is reset to zero. Any time a noise (N) symbol is received, the line state is set to Noise Line State, and the UNKN_LINE_ST bit is reset to zero.

The recognition of these line states is reported to the PCM, which uses this information for either insertion or removal of the station from the ring, ring recovery, or maintenance. The line state machine has no reset. After power-up into any state, it will attain a valid state by satisfying the conditions for attaining a particular line state as given in Table 6-1.

Table 6-1. Line State Machine Line States

Line State Name	Condition
Noise Line State	Any Line State Not Defined
Active line State	JK Symbol Pair
Idle Line State 4	4 I-Symbols
Quiet Line State	16 Q-Symbols
Master Line State	8 Pairs of H/Q- or Q/H-Symbols
Halt Line State	16 I-Symbols

6.2 LINE STATE INDICATION

Encoded line states are presented on the output pins LINE_ST2–LINE_ST0. Table 6-2 lists the encoding of the current line state.

Table 6-2. Current Line States

LINE_ST (2–0)	Mnemonic	Name
000	NLS	Noise Line State
001	ALS	Active Line State
010	—	Reserved
011	ILS4	Idle Line State 4
100	QLS	Quiet Line State
101	MLS	Master Line State
110	HLS	Halt line State
111	ILS16	Idle Line State 16

6.3 LINK ERROR MONITOR OPERATION

The LEM hardware consists of a detector, accumulator, and threshold element. The detector is a state machine that constantly monitors incoming symbol pairs on the receive data path. When link error events are detected, they are counted by the 8-bit link error event counter. When the link error event counter matches the count written to the link error event threshold register, the LE_CTR bit in the interrupt event register is set.

6.4 DATA STREAM GENERATOR

The data stream generator block uses a multiplexer for the purpose of generating a symbol pair at the request of the PCM (or external control when the PCM is in the MAINT state) via LS_REQUESTx, the repeat filter via RF_CNTRLx, or by transmitting the symbol pair from TXDATx. Table 6-3 summarizes the operation of this block.

Table 6-3. Data Stream Generator Output

LS_REQUEST (2–0)	RF_CNTRL (1–0)	DATA_STRM (9–0)
000	XX	Q-Symbol Pair
001	XX	I-Symbol Pair
010	XX	H-Symbol Pair
011	XX	M-Symbol Pair
100	XX	Q-Symbol Pair
101	XX	Q-Symbol Pair
110	00	Symbol Pair from TXDATx
110	01	I-Symbol Pair
110	10	H-Symbol Pair
110	11	I-Symbol Pair
111	XX	Q-Symbol Pair

X = Don't care

6.5 PHYSICAL CONNECTION MANAGEMENT

The ELM chip implements CMT through a PCM state machine as specified in the ANSI FDDI SMT standard. Once a connection has been established, the ELM also performs PCI. The implementation of the PCM and PCI state machines and their functions within CMT are described in the following subsections.

CMT defines the rules that govern the allowable topologies in an FDDI ring. Fundamental to this task is the management of a connection between two PHYs in adjacent stations. It is the task of the PCM state machines in both stations to cooperate in forming a connection between the two PHYs within the rules established by CMT. The allowable types of attachment as defined by the MIC connector are as follows:

A Primary Ring In/Secondary Ring Out

B Secondary Ring In/Primary Ring Out

S Single Attachment End Station

M Concentrator Attachment of an End Station

In addition, CMT defines the type of physical connection between two physical attachments to be determined by the PHY types at each end of the connection. The characteristics of a type of connection determine if that connection will be allowed, if the SMT will be notified of possible connection problems, and the connection mode that will be established. Table 6-4 from the ANSI FDDI SMT document lists the connection rules, and Figure 6-1 illustrates some possible station interconnections to graphically show the types of stations as implemented with concentrators and end stations.

Table 6-4. Connection Rules

		Other PHY			
		A	B	S	M
This PHY	A	V, N	V	V, N	V<P
	B	V	V,N	V, N	V<P
	S	V, N	V, N	V	V
	M	V	V	V	X

NOTE:
V = Indicates a valid connection
X = Indicates an illegal connection
N = Indicates that notification to SMT is required
P = Indicates, if active, prevent THRU in CFM and PHY B takes precedence

More details of FDDI network topology can be found in the ANSI FDDI SMT document.

6.5.1 PCM State Machine

CMT secures a deterministic ring topology, independent of the sequence of station power-up, etc., by allowing only a specific set of connection types. The primary purpose of PCM is to enforce these allowable connections. The PCM announces its attachment type to the remote PCM and listens for the type of attachment from the remote PCM. If they are compatible, the PCM accepts the connection and reports the type of connection to the station configurator. Once the connection type has been established, the two PCMs share in testing the pair of physical links between them. If this test is successful, the link can then be inserted into the ring. Note that PCM operates between two cooperating PHY entities to determine the viability of the link between them, regardless of the actual ring operation. This fact can be observed by reference to the upper pair of concentrators in Figure 6-1 in which the various PHYs are connected to an input on one ring and an output on the other ring. During power-up, the PHYs will determine the viability of the connection; once both connections are valid, multiplexing between the ELMs and MACs (if any in the concentrator) will establish the topology of the ring or rings.

The architectural model for the PCM consists of ten states: OFF, BREAK, TRACE, CONNECT, NEXT, SIGNAL, JOIN, VERIFY, ACTIVE, and MAINT for both the ANSI standard and the hardware realization. The ELM PCM state machine accomplishes all of the transitions in the ANSI FDDI SMT standard, although transitions between some states are enabled by software in certain situations. Interrupts are provided to furnish indications when actions have been completed that require software to specify actions for continuing the PCM state transitions. It is also possible to accomplish non-ANSI-specified action by operating in the MAINT state. The following PCM machine descriptions, along with the ANSI FDDI SMT standard, can be used to produce ANSI-compliant SMT software.

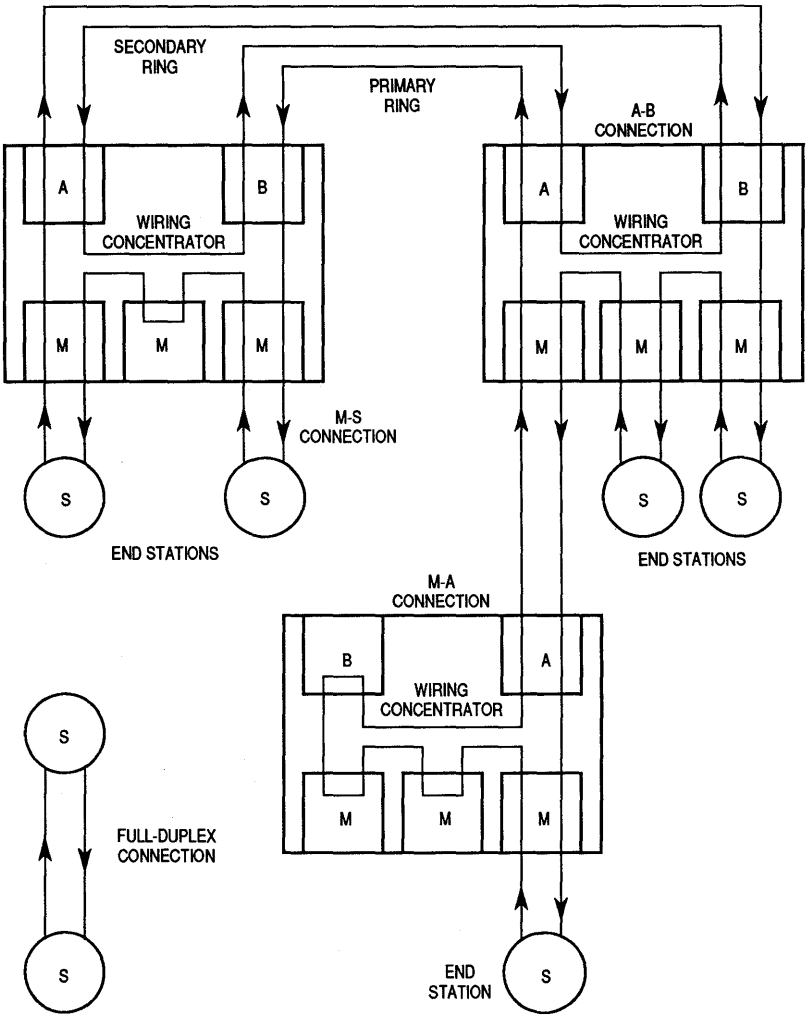


Figure 6-1. Sample FDDI PHY Connections

6.5.1.1 BIT SIGNALING MECHANISM. The signaling protocol is implemented to reduce the software processing overhead and to allow enough flexibility to change the actual pseudocode without affecting the silicon implementation.

When the PCM is in the OFF state, all parameter registers and the configuration registers are loaded with the appropriate values. The transmit vector length register is written with the value n–1 (n = the number of bits to be transmitted). The transmit vector register is written with the bit pattern to be transmitted. PC_START is then written into the control register. The PCM then transitions through the BREAK, CONNECT, and NEXT states. It then transitions back and forth between the NEXT state and the SIGNAL state until all bits in the transmit vector register are transmitted. While the PCM is transmitting all the bits, it also receives the corresponding bits from a remote station and forms a receive

vector that is stored in the receive vector length register. When all bits are received for the transmitted bits, the PCM_CODE interrupt bit is set. The node processor can then read the receive vector length register. Note that the PCM is still in the NEXT state.

If for any reason (other than PC_START) the PCM transitions to the BREAK state, then a PC_START has to be issued before the connection process can begin again. This allows the transmit vector length register and the transmit vector register to be reinitialized. Also, any transition to the BREAK state sets the PCM_BREAK interrupt bit and writes the reason for the transition in the status register B BREAK_REASON field .

If the node processor wants to do a loopback function for the purpose of a Link Confidence Test, it can do so by setting the PC_LOOP bits in control register B. If the PCM is not in the NEXT state or if it is in the NEXT state but PCM_SIGNALING is set, then setting the PC_LOOP bits will have no effect on the state machine. Normally, these bits should be set after the PCM_CODE interrupt bit is set. The node processor can set the station to do a transmit_PDR function or transmit_idle function or a remote loopback function. If the LONG bit is not set in control register B, the Link Confidence Test will last for LC_SHORT (a writable parameter) period of time, after which the PCM_CODE interrupt bit is set. If the LONG bit is set, then the ELM will be in Link Confidence Test mode continuously until the software interrupts it by giving one of the control commands (e.g., write vector, pc_start, etc.). When PC_LOOP is set, the PCM sets the TDF flag internally.

After the Link Confidence Test is completed (i.e., after LC_SHORT or after Halt or Master Line State is received), the PCM_CODE interrupt bit is set. If the node processor decides to transmit more signaling bits, it should load the transmit vector length register with a new value of *n* and then load the transmit vector register with the bit pattern to be transmitted. The PCM again starts transmitting these bits and alternates between the NEXT and SIGNAL states until all bits have been transmitted, as indicated when the PCM_CODE interrupt bit is set again.

This sequence continues until all the bits have been transmitted and the node processor writes PC_JOIN in control register B. The PCM then leaves the NEXT state and enters the JOIN state. Setting PC_JOIN has no effect when the PCM is not in the NEXT state or when PCM_SIGNALING is set. However, if PC_JOIN is set when the Link Confidence Test is in progress, then the Link Confidence Test will be aborted and the PCM join sequence will be initiated.

6.5.1.2 NOISE DETECTION MECHANISM. The TNE timer in the PCM times the period between Idle Line State receptions. This timer is loaded with the noise time register parameter when the line state machine leaves the Idle Line State. The TNE timer keeps counting noise until Idle Line State is again detected. If this timer expires while in the ACTIVE state, then the PCM will break the link and transition to the BREAK state. In the ACTIVE state, the TNE timer starts counting noise only after the line state flag is set. If PC_TRACE is received and the TNE timer expires in the same cycle, then the transition to the TRACE state is taken. This timer is ignored in all PCM states except the ACTIVE state.

6.5.1.3 NOISE IN MAINT STATE. If the NOISE_TIMER bit in control register A is cleared, then the node processor can write to the TNE timer if the PCM is in MAINT state. If the NOISE_TIMER bit is set, the TNE timer is used in the MAINT state to time the noise as previously described. If the TNE timer expires, then the TNE_EXPIRED interrupt bit is set.

6.5.1.4 OPERATION IN TRACE STATE. If the trace propagation (transition 88c) is detected in the ACTIVE state, then the TRACE_PROP interrupt bit is set. In the ACTIVE state, if PC_TRACE is received and a transition is made to the TRACE state, the station remains inserted, Master Line State is sourced on the TDATAx port, and no scrubbing is performed. If Master Line State is detected in the ACTIVE state, the TRACE_PROP interrupt bit is set. If Quiet Line State or Halt Line State is detected (transition 22a), then the SELF_TEST interrupt bit is set.

6.5.2 Physical Connection Insertion

The ELM implements PCI to intelligently bring a new connection into a ring and to remove an existing connection from a ring. The PCI state machine works in conjunction with the PCM state machine to control the data paths of the ELM chip on the MAC side, the RCDATx and TXDATx paths.

There are three primary functions of the PCI state machine:

1. Provide a bypass path between TXDATx and RCDATx.
2. Provide a scrubbing function upon the insertion and removal of a station from the ring.
3. Provide a direct data path between the fiber and the MAC.

The operation of the PCI state machine depends on whether the CLASS_S bit in control register B is set and whether the PCM state machine is in the MAINT state.

6.5.2.1 PCI OPERATION FOR NON-CLASS-S TYPE STATION. After a reset, the PCI state machine will be in the REMOVED state. If the station is not a class-S type, the ELM will be in the bypass mode whereby data input on TXDATx is directly output on RCDATx.

When the PCM state machine enters the ACTIVE state and asserts the SC_JOIN flag, the PCI state machine enters the INSERT_SCRUB state and I-symbol pairs are sourced on RCDATx. At the same time, the PCM state machine causes I-symbols to be output on TDATAx.

The PCI state machine remains in the INSERT_SCRUB state for T_SCRUB length of time, after which it enters the INSERTED state. Upon entering the INSERTED state, the PCM_ENABLED interrupt bit is asserted. In this state, a direct path exists from TXDATx to TDATAx.

If the connection is broken and the PCM state machine enters the BREAK state, the PCI state machine enters the REMOVE_SCRUB state, and I-symbol pairs are sourced on RCDATx). Because the PCM state machine is in the BREAK state, Q-symbols are sourced on TDATAx. While scrubbing is being performed, the PCM state machine will not restart the connection process. The PCI state machine remains in the REMOVE_SCRUB state for T_SCRUB length of time and then enters the REMOVED state.

6.5.2.2 PCI OPERATION FOR CLASS-S TYPE STATION. For a class-S type station single attach, the PCI operation is identical to the non-class-S type with one exception—whenever the PCI state machine would normally be in the REMOVED state, it will be in the INSERTED state. Thus, before entering INSERT_SCRUB or after leaving REMOVE_SCRUB, rather than putting the ELM in the bypass mode, PHY_INVALID is output on RCDATx.

6.5.2.3 PCI OPERATION IN MAINT STATE. When the PCM state machine is in the MAINT state, the PCI state machine does not control the previously mentioned functions. In the MAINT state, all data paths are under the control of software via several control bits in control register A. Software can also override the PCI functions when the PCM state machine is not in the MAINT state by setting the CONFIG_CNTRL bit in control register B.

SECTION 7
TEST OPERATION

The ELM test features remain passive during normal chip operation.

7.1 BIST OPERATION

BIST tests the ELM by circulating pseudorandom data throughout the chip. The various subcircuits within the chip are observed as they respond to the data, and a signature based upon their behavior is generated. This signature may be checked against a correct signature to verify chip functioning. A fault in the chip (within the coverage of BIST) will cause a different signature to be generated.

BIST is activated by setting the RUN_BIST bit in control register A. Upon activation, the data path linear feedback shift register and signature generator are enabled, and the test proceeds.

When BIST has completed, the signature is frozen and may be read through the NPI. The test concludes when a value of zero is reached in the linear feedback shift register. Using a 16-bit linear feedback shift register clocked by the 80-ns BYTCLK, it takes approximately 5.24 ms to circulate 65535 test patterns through the chip. An interrupt to the node processor after RUN_BIST has been set signifies the completion of the ELM self-test. This interrupt is cleared by clearing the RUN_BIST bit in control register A (**not** by reading the interrupt event register). BIST is aborted if the RUN_BIST bit is cleared before the test completes. The procedure for running the BIST is as follows:

- Perform a power-up reset.
- Set the EB_LOC_LOOP bit in control register A.
- Read the violation symbol counter register.
- Read the link error symbol counter register.
- Set the RUN_ BIST bit in control register A.
- Verify that the EB_LOC_LOOP bit in control register A is set during the above.
- Get an interrupt (if enabled) when BIST has finished running.
- Read the BIST signature register; if the test was successful, it will have a value of 6ECD (hex) for ELM revision A, RCB and FCB versions.
- Perform a software reset. Note that if the test fails and the PCM_STATE is in the NEXT state, a PC_STOP must be issued before a software reset can be done.

7.2 COUNTER SEGMENTATION TEST MODE

The ELM counters (including all timers) are designed in such a way that, under counter segmentation test mode, they break apart into several 4-bit counters. For example, in counter segmentation test mode, a 16-bit counter becomes four 4-bit counters. These 4-bit counters count in parallel, allowing automated test equipment to test the counters in $2^4 = 16$ cycles, as opposed to $2^{16} = 65536$ cycles for a 16-bit counter.

Since this test requires the ability to control the BYTCLK, this test is a part of a chip manufacturing test run by automated test equipment.

7.3 BOUNDARY SCAN TEST MODE

In boundary scan test mode, the RCDATx, RDATAx, and TXDATx latches are linked together to form a scan chain. Although this test complements BIST, which does not test these latches, the main purpose of this test mode is for board testing. In this mode, the I/O latches of the various chips on the board are linked into a large scan chain. By serially shifting data into the scan chain (boundary scan serial test mode), then clocking the data in parallel (normal or boundary scan parallel test mode), and finally serially shifting the data out, the I/O latches and interconnections between the various chips can be tested on a PC board.

The different modes, designated by ETESTx are listed in Table 7-1.

Table 7-1. ETESTx Modes

ETEST2	ETEST1	ETEST0	Mode
0	0	0	Normal Operating Mode
0	0	1	Chip-Specific Test Mode
0	1	0	Normal Operating Mode
0	1	1	Normal Operating Mode
1	0	Scan In	Boundary Scan Serial Test Mode
1	1	0	Boundary Scan Parallel Test Mode
1	1	1	Forces All Outputs to High Impedance

In chip-specific test mode, all counters and timers in the chip are divided into segments of four bits that are incremented with each clock tick. This test mode is also used to enhance the test coverage of other logic in the chip.

In boundary scan serial test mode, the input and output latches of the ELM data path signals are connected to form a scan chain, and data is transferred serially through the latches. ETEST0 is the input to the scan chain, and ESCANO is the output.

In boundary scan parallel test mode, the NPD15–NPD0 pins are enabled (all other pins are always enabled).

When the ETESTx pins are all ones, all output pins except EPTSTO are forced into a high-impedance state, which is used for PC board testing.

The ELM scan chain for scan path testing can be input through ETEST0 and output through ESCANO. The scan chain is clocked on the rising edge of BYTCLK and consists of the following signals, which are read in order from left to right and top to bottom.

ETEST0	RDATA0	RDATA1	RDATA2	RDATA3	RDATA4
FOTOFF	TDATA4	TDATA3	TDATA2	TDATA1	TDATA0
TXDAT0	TXDAT1	TXDAT2	TXDAT3	TXDAT4	TXDAT5
TXDAT6	TXDAT7	TXDAT8	TXDAT9	TXPAR	RCPAR
RCDAT9	RCDAT8	RCDAT7	RCDAT6	RCDAT5	RCDAT4
RCDAT3	RCDAT2	RCDAT1	RCDAT0	NPD15	NPD14
NPD13	NPD12	NPD11	NPD10	NPD9	NPD8
NPD7	NPD6	NPD5	NPD4	NPD3	NPD2
NPD1	NPD0	ESCANO			

Note that ETEST0 and ESCANO are not latched pins but represent the input and output of the scan chain, respectively.

SECTION 8
ELECTRICAL CHARACTERISTICS

8.1 ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	− 0.5 to + 7.0	V
DC Input Voltage	V_{in}	− 1.5 to V_{CC} + 1.5	V
DC Output Voltage	V_{out}	− 0.5 to V_{CC} + 0.5	V
DC Current Drain Per Pin	I	25	mA
DC Current Drain V_{CC} and GND Pins	I	75	mA
Storage Temperature	T_{stg}	− 65 to + 150	°C
Lead Temperature, Soldering (10 sec)	T_L	300	°C

The device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, normal precautions should be taken to avoid application of voltages higher than maximum-rated voltages to these high-impedance circuits. Tying unused inputs to the appropriate logic voltage level (e.g., either GND or V_{CC}) enhances reliability of operation.

8.2 RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	4.75 to 5.25	V
Input and Output Voltage	V_{in}, V_{out}	0.0 to V_{CC}	V
Ambient Temperature	T_A	0 to 70	°C

8

8.3 AC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
CMOS, Minimum High-Level Input, V_{out} = 0.1 V or V_{CC} – 0.1 V; I_{out} = 20 µA; V_{CC} = 4.5 V	V_{IH}	3.15	—	Vdc
V_{CC} = 5.5 V	V_{IH}	3.85	—	Vdc
TTL, Minimum High-Level Input, V_{out} = 0.1 V or V_{CC} – 0.1 V; I_{out} = 20 µA; V_{CC} = 4.5 V	V_{IH}	2.0	—	Vdc
V_{CC} = 5.5 V	V_{IH}	2.0	—	Vdc
CMOS, Maximum Low-Level Input, V_{out} = 0.1 V or V_{CC} – 0.1 V; I_{out} = 20 µA; V_{CC} = 4.5 V	V_{IL}	—	1.35	Vdc
V_{CC} = 5.5 V	V_{IL}	—	1.35	Vdc
TTL, Maximum Low-Level Input, V_{out} = 0.1 V or V_{CC} – 0.1 V; I_{out} = 20 µA; V_{CC} = 4.5 V	V_{IL}	—	0.8	Vdc
V_{CC} = 5.5 V	V_{IL}	—	0.8	Vdc
Minimum Low-Level Output Current, V_{OL} = 0.4 V, V_{CC} = 4.5 V	I_{OL}	5.8		mA
Maximum Output Leakage, Three-State, Output = High-Z, V_{out} = V_{CC} or GND, V_{CC} = 5.5 V	I_{OZ}	—	±4.4	µA
Maximum Input Capacitance, V_{CC} = 5.0 V	C_{in}	10.0	—	pF
Maximum Output Capacitance, Output High-Z, V_{CC} = 5.0 V	C_{out}	12.5	—	pF
Maximum I/O Capacitance, Configured as Input, V_{CC} = 5.0 V	$C_{I/O}$	15.0	—	pF

NOTE: All AC timings assume a capacitive loading of ≤ 50 pF.

8.4 NODE PROCESSOR INTERFACE TIMING (see Figure 8-1)

Num	Characteristic	Min	Max	Unit
1	$\overline{\text{ELMSEL}}$ Setup Time	10	—	ns
2	$\overline{\text{ELMSEL}}$ Hold Time	10	—	ns
3	NPRW Setup Time	5	—	ns
4	NPRW Hold Time	20	—	ns
5	NPA Setup Time	5	—	ns
6	NPA Hold Time	20	—	ns
7	Time to NPD High Impedance	—	30	ns
8	Time to NPD Driven (Read) (see Note 2)	2	—	ns
9	Time to NPD Valid (Read) (see Note 3)	—	30	ns
10	Time to NPD Invalid (Read)	2	—	ns
11	NPD Setup Time (Write) (see Notes1 and 4)	30	—	ns
12	NPD Hold Time (Write)	20	—	ns
13	Time to $\overline{\text{ELMINT}}$ Asserted (see Note 1)	—	40	ns
14	Time to $\overline{\text{ELMINT}}$ Negated (see Note 1)	—	40	ns

NOTES:
1. Relative to the rising edge of BYTCLK.
2. Relative to the falling edge of BYTCLK.
3. Data is valid on the second rising edge of NPCLK following assertion of $\overline{\text{ELMSEL}}$, regardless of how long $\overline{\text{ELMSEL}}$ is held asserted.
4. Data is sampled by the ELM on the first rising edge of NPCLK following assertion of $\overline{\text{ELMSEL}}$, regardless of how long $\overline{\text{ELMSEL}}$ is held asserted.

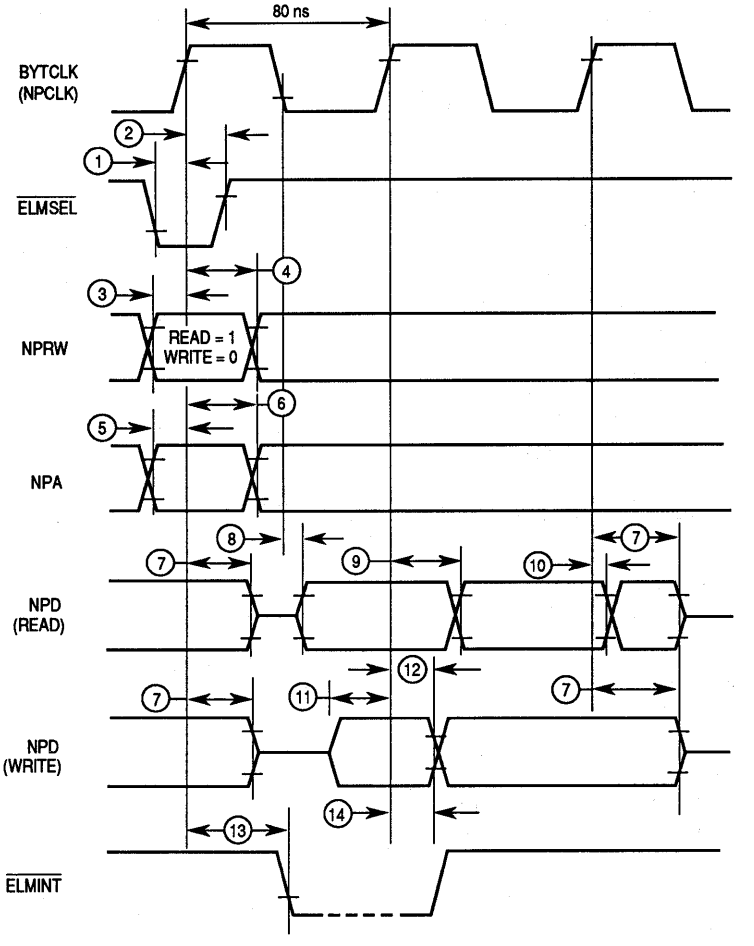


Figure 8-1. Node Processor Interface Timing Diagram

8.5 DATA I/O PORT TIMING (see Figure 8-2)

Num	Characteristic	Min	Max	Unit
15	Skew, SYMCLK to BYTCLK	0	10	ns
16	RSCLK Time Low	15	25	ns
17	RSCLK Time High	15	25	ns
18	Time to RCDATx Invalid	2	—	ns
19	Time to RCDATx, RPAR Valid	—	30	ns
20	RDATA Setup Time (see Note 1)	5	—	ns
21	RDATA Hold Time (see Note 1)	8	—	ns
22	TXDAT, TPAR Setup Time (see Note 2)	5	—	ns
23	TXDAT, TPAR Hold Time (see Note 2)	7	—	ns
24	Time to TDATA Valid	—	25	ns
25	Time to TDATA Invalid	2	—	ns
26	Time to LSR2–LSR0 Invalid	2	—	ns
27	Time to LSR2–LSR0 Valid	—	27	ns

NOTE:
1. Times are relative to the rising edge of RSCLK.
2. Times are relative to the falling edge of SYMCLK when BYTCLK is low. All other times are relative to the rising edge of BYTCLK or SYMCLK as shown.

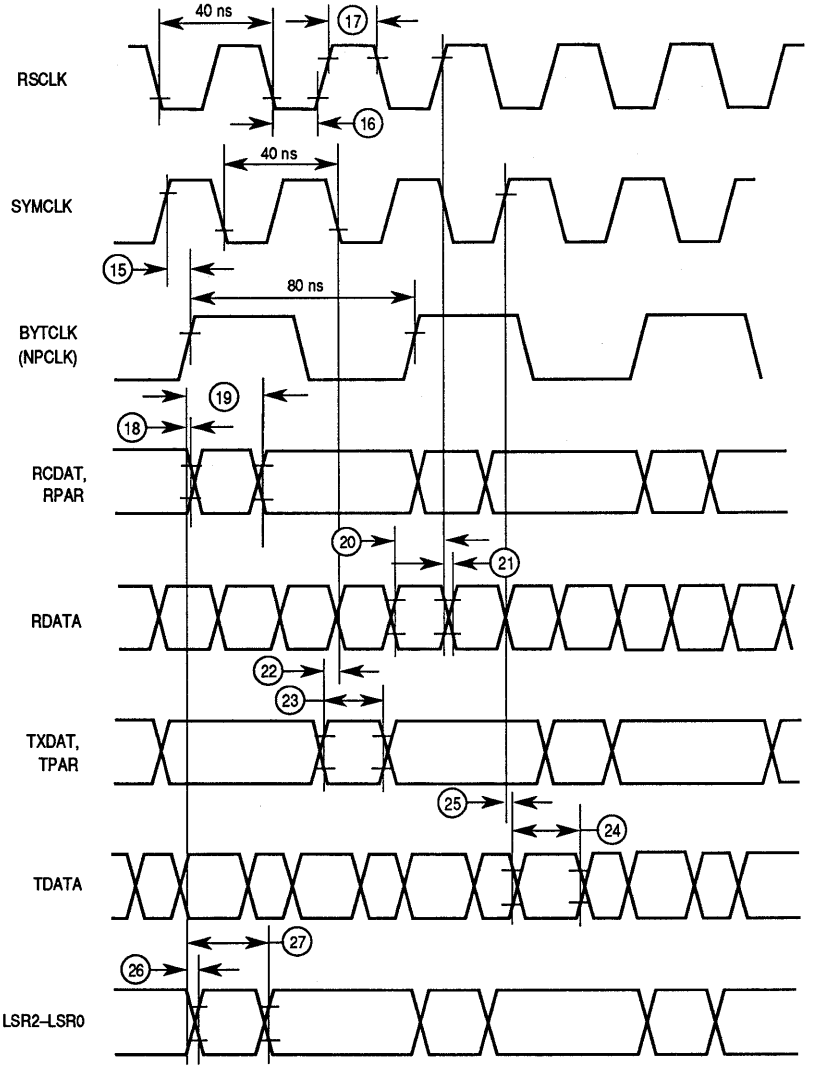


Figure 8-2. Data I/O Port Timing

8.6 MISCELLANEOUS SIGNALS TIMING (see Figure 8-3)

Num	Characteristic	Min	Max	Unit
30	EPTSTO Hold Time	10	—	ns
31	EPTSTO Setup Time	10	—	ns
32	SD Setup Time	5	—	ns
33	SD Hold Time	20	—	ns
34	LOOPBACK, $\overline{\text{FOTOFF}}$, ESCANO, ULSB, EBFERR Invalid	2	—	ns
35	LOOPBACK, $\overline{\text{FOTOFF}}$, ESCANO, ULSB, EBFERR Valid	—	25	ns
36	ENCOFF Setup Time	10	—	ns
37	ENCOFF Hold Time	10	—	ns

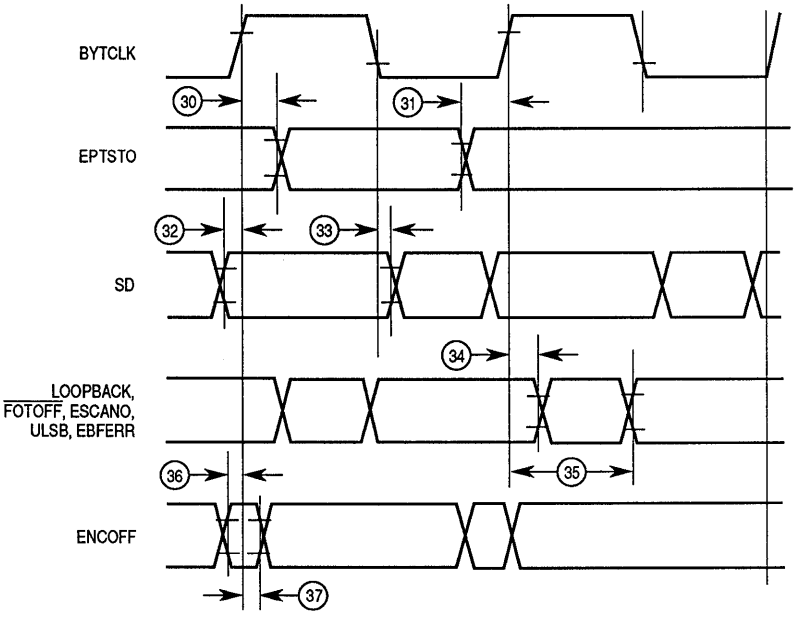


Figure 8-3. Miscellaneous Signals Timing

SECTION 9
ORDERING INFORMATION AND MECHANICAL DATA

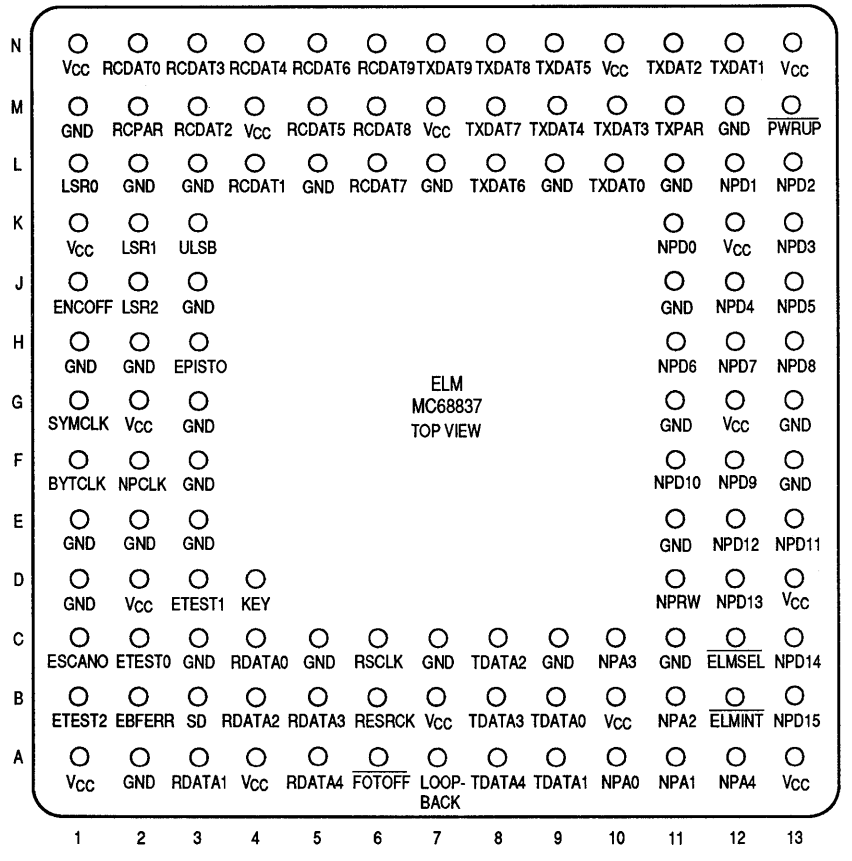
This section contains the ordering information, pin assignments, and package dimensions for the MC68837 ELM chip.

9.1 STANDARD ORDERING INFORMATION

Package Type	Frequency (MHz)	Temperature	Order Number
Pin Grid Array (RC Suffix)	25	0°C to 70°C	MC68837RCB
Quad Flat Pack (FC Suffix)	25	0°C to 70°C	MC68837FCB

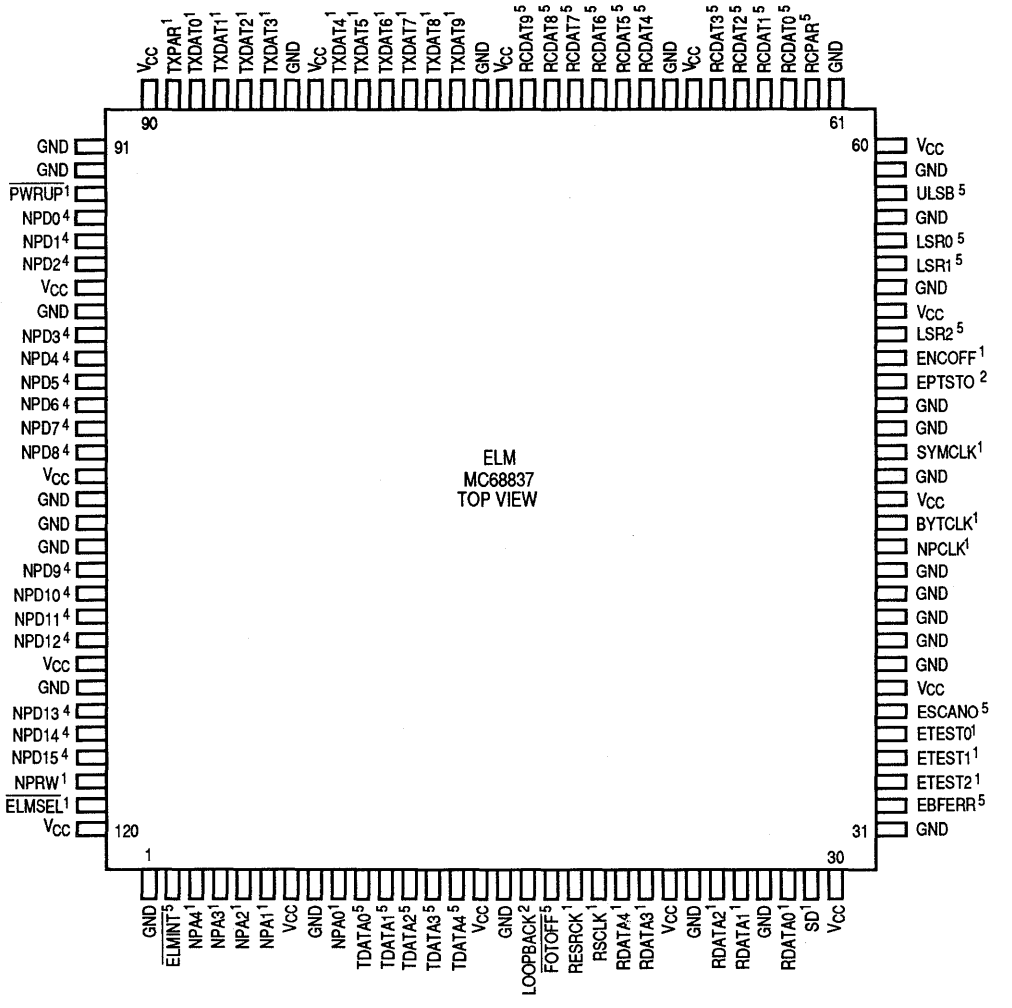
9.2 PIN ASSIGNMENTS

9.2.1 120-Lead Pin Grid Array



9

9.2.2 120-Lead Quad Flat Package



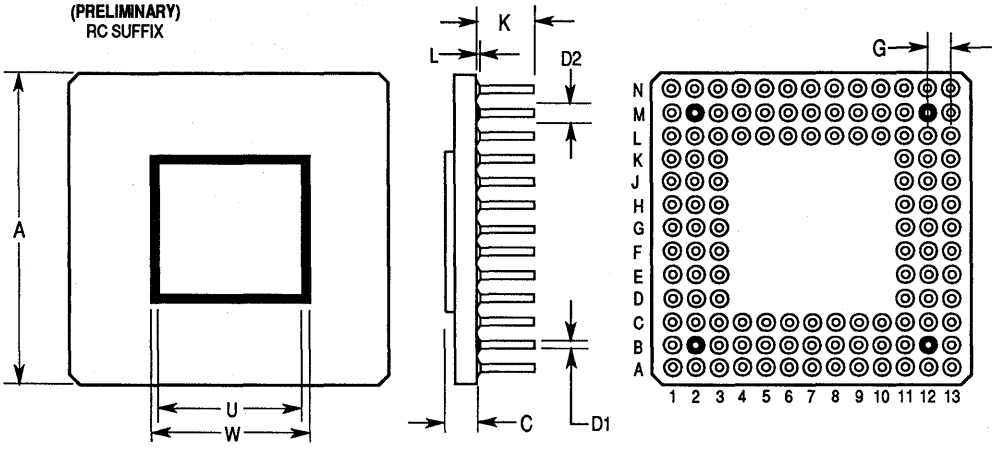
LEGEND:

1. TTL input.
2. CMOS output.
3. CMOS input. (The ELM does not utilize any CMOS inputs.)
4. Three-state CMOS input/output.
5. Three-state CMOS output.

9

9.3 PACKAGE DIMENSIONS

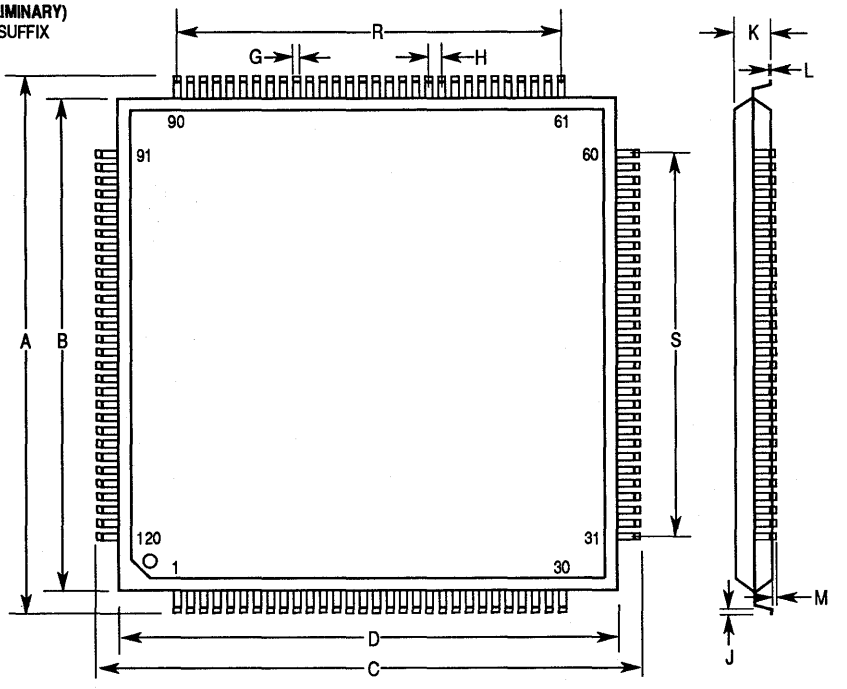
120-LEAD CERAMIC PGA
(PRELIMINARY)
RC SUFFIX



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	34.29 SQ	34.80 SQ	1.350 SQ	1.370 SQ
C	2.21	2.49	0.087	0.098
D1	0.46 (120X)		0.018 (120X)	
D2	1.27 (4X)		0.050 (4X)	
G	2.54 BSC		0.100 BSC	
K	43.18	48.26	1.70	0.190
L	1.143	1.38	0.045	0.055
U	16.383	16.891	0.645	0.665
W	16.891	17.145	0.665	0.675

9

120-LEAD
PLASTIC QUAD FLAT PACK
(PRELIMINARY)
FC SUFFIX



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.10	31.37	1.224	1.235
B	27.90	28.10	1.098	1.106
C	31.10	31.37	1.224	1.235
D	27.90	28.10	1.098	1.106
G	0.360	0.510	0.014	0.020
H	.800 TYP.		0.031 TYP.	
J	0.75	0.92	0.030	0.036
K	3.45	3.85	0.136	0.152
L	0.10	0.18	0.004	0.007
M	0.25	0.35	0.010	0.012
R	23.20 REF.		0.913 REF.	
S	23.20 REF.		0.913 REF.	

DIMENSIONS FOR MOTOROLA CHANDLER
MANUFACTURING SITE
(FOR ALL NEW DESIGNS)

REV. 2.3 1/15/90

9

INDEX

I

I

-U-

-V-

-X-

I

MOTOROLA

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.

EUROPE: Motorola Ltd.; European Literature Center; 88Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.

JAPAN: Nippon Motorola Ltd.; 4-32-1,Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.

ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

A31018 PRINTED IN USA 12/91 IMPERIAL LITHO 82996 15,000 MFU YGABAA