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TECHNICAL UPDATE
DEVELOPMENT TOOLS

M68HC705J2PGMR

Technical Update contains updates to documented information appearing in other Motorola technical documents as well as new information not covered elsewhere.

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M68HC705J2PGMR

Revision History

Date	Revision	Description
4/24/95	1.00	Original release. Includes tracker numbers HC705J2PGMR.001, HC705J2PGMR.003, HC705J2PGMR.004, HC705J2PGMR.005, and HC705J2PGMR.006

HC705J2PGMR ECN No. A001

Reference Document: Application Note HC705JPPGMR/AN1

Tracker Number: HC705J2PGMR.001   **Revision: 1.00**

Listed below is engineering change notice (ECN) No. A001 for the HC705J2PGMR. This ECN was issued July 13, 1992. The problem found with the PGMR was a race condition between the V_{DD} and V_{PP} power pins. Refer to page 1-7 in the Application Note, document number HC705JPPGMR, accompanying the PGMR.

If R12 is on your board, proceed with the following changes:

1. Remove R12. This resistor is used to shunt V_{DD} to ground when the power switch is in the off position. Removing R12 delays the fall time of the V_{DD} line when the board is powered down, allowing the V_{PP} line to fall to an acceptable level before V_{DD} drops to 0 V.

2. Change C2 from 47 μF to 4.7 μF. This will reduce the fall time of V_{PP} when powering down, but will achieve a quick enough rise time when the board is powered up.

3. Replace power switch S1 (currently a 3 position switch) with a 2 position switch. This change eliminates the middle position of the switch that floated the V_{DD} and the V_{PP} pins. The recommended type is ALCO MHS-222.

Programming Operation Example

Reference Document: HC705JPPGMR/AN1, page number not applicable

Tracker Number: HC705J2PGMR.003   Revision: 1.00

Listed below are the programming steps for the HC705J2 on the HC705J2/P9 PGMR board. A simple square wave routine will be programmed into the HC705J2. The program outputs a 7.5 µsec, 60 percent duty cycle, square wave on the HC705J2's port A. The program is:

```
****************************************
* J2TEST.ASM
* For MC68HC705J2
* 9/15/93
* Assembled with IASM05 V 3.02 m from P&E Microcomputer Systems
****************************************
* Description: Toggles all pins of portA. Given a 4.000-MHz crystal, the
frequency *of oscillation is 7.5 µs. Duty cycle is 60 percent.
****************************************
        ORG     $0700      ;beginning of EPROM of J2

Start   lda     #$ff       ;set PortA as output
        sta     $04

Loop    lda     #$00       ;set PortA low
        sta     $00
        lda     #$ff       ;set PortA high
        sta     $00
        bra     Loop       ;infinite loop


        ORG     $0FF8
TIMER   FDB     Start      ;Set all vectors to
IRQ     FDB     Start      ; beginning of code
SWI     FDB     Start
RESET   FDB     Start
```

For this example, the P&E's IASM05 assembler and a device for programming a 27C64-type EPROM will be used. It is assumed the reader has sufficient knowledge of the assembler and the programmer to accomplish this task.

The M68HC705J2/P9 PGMR board has undergone a change on R12. If R12 is not populated, then the change has been made on your board. If R12 is populated, see tracker number HC705J2PGMR.001 for instructions on changing your board.

NOTE: The HC705J2 window must be covered with an opaque covering except
when erasing the part.

1. Make sure that the HC705J2 is erased. If it is not erased or you are
unsure, uncover the window and place it under a UV eraser for at least
40 minutes. The quartz window's small size results in a very long erase
time for this part.

2. Assemble the above program.

3. Using an EPROM programmer, program a 27C64-type EPROM with
the code.
   - Program the unused space in the EPROM to $00, which will
     make the programming operation on the PGMR board faster.
     This can be done on many programmers by clearing the
     contents of programmer memory to $00 before reading in the
     .S19 or .HEX file.

   - After programming, make sure that correct addresses have been
     used. This can be done on many programmers by erasing the
     memory of the programmer and reading the EPROM contents
     back. Check that the EPROM has the same data as the .LST file.

NOTE: The J2 and the 27C64 EPROM have a one-to-one mapping of
addresses. The PGMR board does no translation of the addresses.

4. Apply +5 V V_{DD} to the PGMR board

5. Apply +16.5 V V_{PP} to the PGMR board

6. Set POWER switch to OFF.

7. Place the EPROM into socket U2 labeled 27C64.

8. Place the MC68HC705J2 in socket U4 labeled MC68HC705J2.

9. Set RESET switch to IN.

10. Set POWER to ON.

11. Set the DIP switch S3 to OFF,ON,ON,OFF. This selects J2 program
and verify.

12. Set RESET switch to OUT.

13. The PROGRAM light will come on as the device programs itself.

14. The VERIFY light will come on if the device verifies correctly against the
EPROM. If the VERIFY light does not come on, the data read from the
device is not the same as the data read from the EPROM.
   - If the device does not verify, the device possibly was not erased
     completely.

- It is possible for the device to verify if code was written outside the J2's EPROM space. This can happen if data is written to the ports, for example. The port logic may read back the data that was written to it, but that data will not be available for execution after a power- on reset. Make sure that the EPROM contains data only within the code space of the J2.

15. Set RESET switch to IN.

16. Set POWER switch to OFF.

17. Remove the J2 part from the PGMR board.

To see the results of the square wave routine that was programmed, test the output of port A by constructing a simple circuit with the HC705J2 on a protoboard. The circuit should have a 4-MHz crystal or oscillator, an MC34064 or similar low-voltage reset circuit on RESET, and a pullup on IRQ.

Programming Example for HC705J2 as HC05J1

Reference Document: HC705JPPGMR/AN1, page number not applicable

Tracker Number: HC705J2PGMR.004   Revision: 1.00

Listed here are the steps to program an HC705J2 as an HC05J1 on the HC705J2/P8 PGMR board.

The MC68HC705J2 has the ability to emulate the MC68HC05J1. This mode is enabled by programming the J1 bit (bit 2) of the mask option register to a logic one. In this mode, the memory map of the MC68HC705J2 is identical to that of the MC68HC05J1 with two exceptions: the MOR is present at $0700 and $07F1-$07F7 is EPROM instead of unused. The map is detailed on page 9-2 of MC68HC705J2/D.

A simple square wave routine will be programmed into the HC705J2. The program outputs a 7.5 µsec, 60 percent duty cycle, square wave on the HC705J2's port A. The program is:

```
****************************************
* J1EMUL.ASM
* For MC68HC705J2
* 9/15/93
* Assembled with IASM05 V 3.02 m from P&E Microcoputer Systems
****************************************
* Description:
*   All code is written in the memory map of the J1. Programming bit 2 of MOR
*selects this emulation mode.
```

```
*   Toggles all pins of portA. Given a 4.0000-MHz crystal, the frequency of
*oscillation is 7.5 µs. Duty cycle is 60 percent.
****************************************
        org     $0700     ;Address of MOR
MOR     db      $04       ;activate J1 Emulation

        ORG     $0300     ;Address of EPROM in J1 map

Start   lda     #$ff      ;Set Port A as output
        sta     $04

Loop    lda     #$00      ;Set Port A to low
        sta     $00
        lda     #$ff      ;Set Port A to high
        sta     $00
        bra     Loop      ;Infinite Loop



        ORG     $07F8     ;Address of vectors
TIMER   FDB     Start     ;Set all vectors to
IRQ     FDB     Start     ;beginning of code
SWI     FDB     Start
RESET   FDB     Start
```

For this example, the P&E's IASM05 assembler and a device for programming a 27C64-type EPROM are used. It is assumed the reader has sufficient knowledge of the assembler and the programmer to execute the instructions.

The M68HC705J2/P9 PGMR board has undergone a change on R12. If R12 is not populated, then the change has been made on your board. If R12 is populated, see tracker number HC705J2PGMR.001 for instructions on changing your board.

NOTE: The HC705J2 window must be covered with an opaque covering except when erasing the part.

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1. Make sure that the HC705J2 is erased. If it is not erased or you are unsure, uncover the window and place it under a UV eraser for at least 40 minutes. The quartz window's small size results in a very long erase time for this part.

2. Assemble the above program.

3. Using an EPROM programmer, program a 27C64-type EPROM with the code.
   • Program unused space in the EPROM to $00 to make the programming operation on the PGMR board faster. This can be done on many programmers by clearing the contents of programmer memory to $00 before reading in the .S19 or .HEX file.

- After programming, make sure that correct addresses have been used. This can be done on many programmers by erasing the memory of the programmer and reading the EPROM contents back. Check that the EPROM has the same data as the .LST file.

NOTE: The J2 and the 27C64 EPROM have a one-to-one mapping of addresses. The PGMR board does no translation of the addresses.

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4. Apply +5 V V_{DD} to the PGMR board.

5. Apply +16.5 V V_{PP} to the PGMR board.

6. Set POWER switch to OFF.

7. Place the EPROM into socket U2 labeled 27C64.

8. Place the MC68HC705J2 into socket U4 labeled MC68HC705J2.

9. Set RESET switch to IN.

10. Set POWER to ON.

11. Set the DIP switch S3 to ON,OFF,ON,OFF. This selects J1 program and verify.

12. Set RESET switch to OUT.

13. The PROGRAM light will come on as the device programs itself.

14. The VERIFY light will come on if the device verifies correctly against the EPROM. If the VERIFY light does not come on, the data read from the device is not the same as the data read from the EPROM.
   - If the device does not verify, one possibile problem is that the device was not erased completely.

   - It is possible for the device to verify if code was written outside the J2's EPROM space. This can happen if data is written to the ports, for example.

   - The port logic may read back the data that was written to it, but that data will not be available for execution after a power-on reset. Check that the EPROM contains data only within the code space of the J2.

15. Set RESET switch to IN.

16. Set POWER switch to OFF.

17. Remove the J2 part from the PGMR board.

To see the results of the square wave routine that was programmed, test the output of port A by constructing a simple circuit with the HC705J2 on a protoboard. The circuit should have a 4-MHz crystal or oscillator, an MC34064 or similar low-voltage reset circuit on RESET, and a pullup on IRQ.

Programming Operation — Bootloader Mode Enable

Reference Document: M68HC705JPPGMR2/AN1, page 1-5

Tracker Number: HC705J2PGMR.005   Revision: 1.00

To program or verify MCU parts on the PGMR, the MCU must be put into bootloader mode. This is done on the M68HC705J2/P9PGMR by applying V_{PP} to the board. This is necessary even if only for verifying the MCU contents.

Programming the HC705J3

Reference Document: Not applicable

Tracker Number: HC705J2PGMR.006   Revision: 1.00

The HC705J3 can be programmed in the J2/P9 programmer without any hardware modifications to the board.

The switch configurations for programming this device are:

Function	SW1	SW2	SW3	SW4
Program and Verify	On	Off	On	Off
Verify Only	On	Off	Off	On