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Application Note

BIPOLAR CHOPPER TRANSISTORS AND CIRCUITS

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Bipolar transistor chopper circuits are used in many applications for low-drift amplification of dc and low-frequency ac signals. This note discusses the characteristics of transistors used as choppers and the circuits in which they can be used.

MOTOROLA Semiconductor Products Inc.

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INTRODUCTION

Many analog data systems require a capability for amplifying dc or slow-time-varying signals. Low-level signals from transducers are specific examples. At first thought, a direct-coupled amplifier would seem suitable. However, such an amplifier is susceptible to drift error; that is, drift within the amplifier itself, whether due to component aging or to temperature variation, would be amplified and presented at the output. At this point it would be difficult, if not impossible, to distinguish such drift error from actual signal. Two approaches exist to reduce or eliminate this problem:

The first approach is to design the dc amplifier with components very resistant to changes due to age and temperature. Environmental control can be added to obtain an extremely stable amplifier, but its cost would be prohibitive for most applications.

The alternative approach to stability, and generally a more desirable solution, is to use a chopper-stabilized amplifier. Such an amplifier is not actually stabilized by a chopper; rather a chopper enables the utilization of a stable ac amplifier for amplifying dc signals. The amplified ac output signal can then be restored by synchronous demodulation. Thus, the *system* is, in effect, *stabilized*.

Early chopper-stabilized amplifiers used mechanical choppers, such as the relay shown in Figure 1. These circuits were characterized by near ideal contact performance; i.e., extremely high impedance when open, and near-zero impedance when closed. However, these advantages were compromised by several disadvantages. Relays have short lifetimes, slow switching speeds, contact bounce, and, generally, large size. Any electrical overstress might also result in an increase in contact resistance.

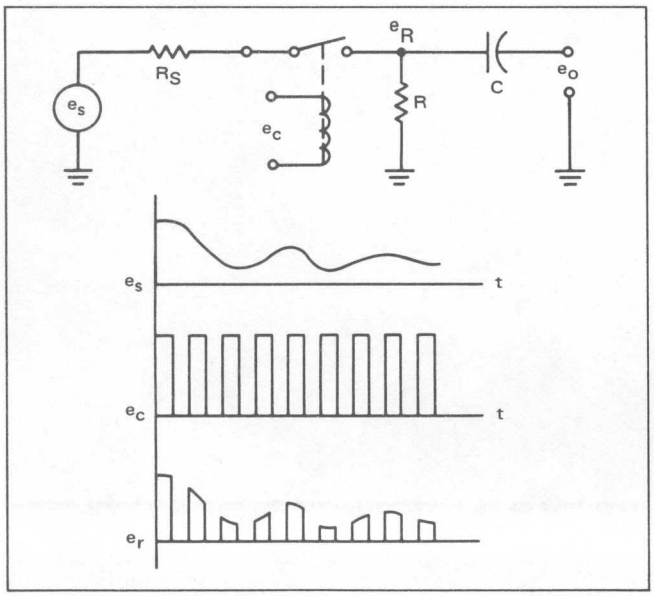

FIGURE 1 – Electro-Mechanical-Chopper Circuit and Waveforms

The disadvantages of relays in choppers are eliminated by bipolar chopper transistors, but not without introducing new disadvantages. A transistor cannot match the near-ideal switching characteristics of a relay, but the principal shortcomings of transistors, offset voltage and offset current, can be minimized through proper circuit design.

ANALYSIS OF BIPOLAR CHOPPER TRANSISTORS

If a common-emitter transistor switch is in the ON state, but the collector current is zero, the collector-emitter voltage will not be zero. It is this offset voltage that most seriously limits the performance of bipolar transistors in chopper circuits. The following amplifier will not be able to distinguish between the offset voltage and signal levels of comparable magnitude. In the OFF state, the transistor will not be an ideal open circuit, but will appear as a current source. This offset current can induce a voltage in the load, again masking signal levels of comparable level. The design problem then is quite simply one of eliminating, or more realistically, reducing, the offset voltage and offset current. The most popular technique is to use common-collector, or inverted, operation, rather than common-emitter. Justification for this is based on the work of Ebers and Moll. They have shown that the offset voltages are given by[1]

Common Emitter

$$V_{CE} = (\pm)\frac{kT}{q}\ln\left\{\alpha_I \frac{1 - \frac{I_C}{I_B}\frac{1-\alpha_N}{\alpha_N}}{1 + \frac{I_C}{I_B}(1-\alpha_I)}\right\} \quad ; \qquad (1A)$$

Common Collector

$$V_{EC} = (\pm)\frac{kT}{q}\ln\left\{\alpha_N \frac{1 - \frac{I_E}{I_B}\frac{1-\alpha_I}{\alpha_I}}{1 + \frac{I_E}{I_B}(1-\alpha_N)}\right\} \quad , \qquad (1B)$$

where

$\frac{kT}{q}$ = 0.026 volts at room temperature,

α_I = common base current gain, inverted connection*,

α_N = common base current gain, normal connection,

I_C = collector terminal current,

I_E = emitter terminal current,

I_B = base terminal current, and

$(\pm)$ = (+) for PNP, (–) for NPN.

*By inverted connection is meant that the control signal is applied between base and collector instead of between base and emitter as normal.

In choppers, the drive current, I_B, is usually much greater than the signal current (I_c for common emitter, I_e for common collector). Using this and the fact that

$$a_I < a_N < 1 \tag{2}$$

the offset voltages can be seen to be

$$V_{CE} \approx 0.026 \ell n\, a_I \tag{3A}$$

$$V_{EC} \approx 0.026 \ell n\, a_N \tag{3B}$$

Now since a_N generally approaches "1" in magnitude, $\ell n\, a_N$ is near "0." However $\ell n\, a_I$ has a larger magnitude since $a_I < a_N < 1$.

Therefore,

$$V_{CE} > V_{EC}, \tag{4}$$

or the common collector, or inverted mode of operation yields a lower offset voltage.

As an example, consider the MM4052 bilateral switching transistor. From the data sheet it is found that $h_{FE(min)}$ = 15 at 150 mA, and $h_{FE(inv)}$ (min) = 3 at 150 mA.

Using the relationship

$$a = \frac{h_{FE}}{1 + h_{FE}} \tag{5}$$

it is found that a_N = 0.937 and a_I = 0.75, therefore V_{CE} = 0.026 ℓn (0.75) and V_{EC} = 0.026 ℓn (0.937), or V_{CE} = −7.5 mV and V_{EC} = −1.7 mV.

It is seen that the inverted operation results in lower offset voltage. The choice of the bilateral device as an example gives less dramatic results than a conventional transistor; a device with a_N closer to unity will, in general, result in an offset-voltage differential greater than an order of magnitude.

In analyzing the OFF state of a transistor, Ebers and Moll have given the following expressions for current flow through the emitter-base and collector-base junctions when they are both reverse biased[2]

$$I_E = \frac{I_{EO}(1 - a_N)}{1 - a_I a_N}; \tag{6}$$

$$I_C = \frac{I_{CO}(1 - a_I)}{1 - a_N a_I}, \tag{7}$$

The above equations are based only upon the analysis of diffusion current. The total reverse current through a PN junction is the sum of three components:

$$I_R = I_D + I_G + I_S, \tag{8}$$

where

I_D = bulk diffusion current,

I_G = charge generation current, and

I_S = surface leakage current.

For germanium at room temperature the diffusion current dominates and the above equations apply. For silicon at room temperature, however, I_D is small and charge-generation current due to impurity ions in the depletion layer dominates. I_G is given by[3]

$$I_G = K_V K_1 \sqrt[n]{V} \tag{9}$$

where

K_V = an empirical factor which approaches "1" for voltages greater than 0.1 volt,

K_1 = a proportionality constant determined primarily by geometry, resistivity, and the impurities in the depletion layer,

V = applied voltage, and

n = exponent describing depletion layer behavior

In chopper applications, these currents are called offset currents. Equation (6) applies for the diffusion part of the offset current in the inverted connection. If a_N has a reasonably high value (≈1), equation (7) will reduce to

$$I_C \approx I_{CO}. \tag{10}$$

Using the relationship

$$a_I I_{CO} = a_N I_{EO}, \tag{11}$$

equation (6) becomes

$$I_E = \frac{a_I}{a_N} \frac{1 - a_N}{1 - a_N a_I} I_{CO}, \tag{12}$$

For typical values of a_I and a_N,

$$I_E \ll I_{CO}. \tag{13}$$

Therefore, if a germanium transistor is used as a shunt chopper (Figure 2) in the inverted mode, the offset error current will be I_E.

In analyzing the OFF condition in an inverted transistor using "0" OFF bias, Chaplin and Owens have shown that the emitter-collector circuit appears to be a simple resistance[4]

$$r_o \approx \frac{0.026\ V}{I_{CO}}. \tag{14}$$

For the 2N2944 chopper transistor at 25°C this would be

$$r_o \approx \frac{0.026}{0.1} \times 10^9 = 260\ M\Omega.$$

Thus it is seen that a silicon chopper transistor utilizing "0" OFF bias offers a near-ideal open circuit for reasonable load impedances.

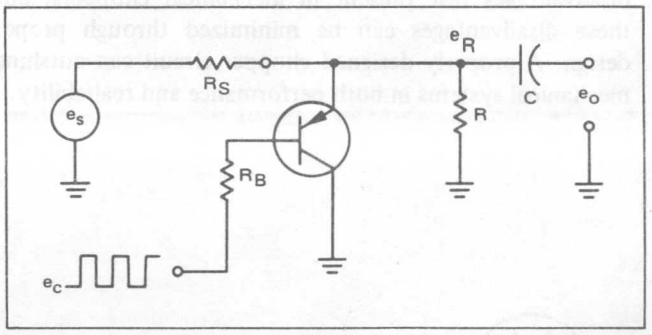

FIGURE 2 – Shunt-Transistor Chopper Circuit

Using the inverted mode of operation, a series chopper circuit and its equivalent ON and OFF representations are shown in Figure 3. The pulse transformer is required to avoid biasing the output signal with the chopping signal. The electrostatic shield reduces capacitive coupling of switching transients through the transformer to the load.

Consider now the equivalent ON state in Figure 3B. V_{EC} is as given in equation (3B), r_{ec} is the dynamic ON series resistance, r_c is the collector bulk resistance (typically about 0.5 ohm for Motorola silicon Annular* transistors), and I_B is the collector-base bias current. It is clear that in the ON state, the voltage appearing across the transistor is not "0"; it represents a minimum limit for the size of the signal (e_S) that can be supplied to the load.

Figure 3C gives the equivalent OFF state for the chopper. The transistor appears as a current source, I_E, shunted by the leakage resistance across the emitter junction. It is the flow of I_E through the load, R_L, that gives an offset during the OFF state.

The equivalent circuits of Figure 3 provide fairly accurate views of the two major states of the chopper. However, the transient states between the ON and OFF conditions are also worth considering. The transistor base is coupled to the emitter and collector by junction capacitance. Assume, for example, that the OFF bias from collector to base is 6 volts. (Chopping signal is 12 volts P-P at transformer.) According to the data sheet for the 2N2944, the output capacitance for common base, C_{ob}, is typically 3.2 pF. When the chopping signal suddenly swings 12 volts to the −6 volt ON value, the junction capacitance tries to pass this 12 volt transient. The actual value of the transient that appears at the collector will be a function of current limiting in the circuit, but there still will be a significant transient. A similar situation appears during the turn-off switching time.

It is now advisable to analyze the circuit in terms of its disadvantages and to consider methods to eliminate, or reduce, these disadvantages. The disadvantages are, quite simply, (1) offset voltage, (2) offset current, and (3) transient feedthrough.

PRACTICAL CHOPPER CIRCUITS

While the series chopper of Figure 3 might be satisfactory in some noncritical applications, the demands of more sophisticated systems require reduction of offset errors. The series-pair chopper circuit of Figure 4 is designed for this reduction.

As the equivalent ON circuit shown, each transistor contributes an offset voltage, but they are of opposite polarities and tend to cancel. If a very tightly matched pair is used, the effective offset voltage will be almost "0." That is, for an input voltage, e_S, of "0", the output, e_O, will be "0."

The OFF equivalent in Figure 4C shows that the offset currents are opposing. Therefore, the net offset current through the load will be the difference between I_E, and

*Annular semiconductors patented by Motorola Inc.

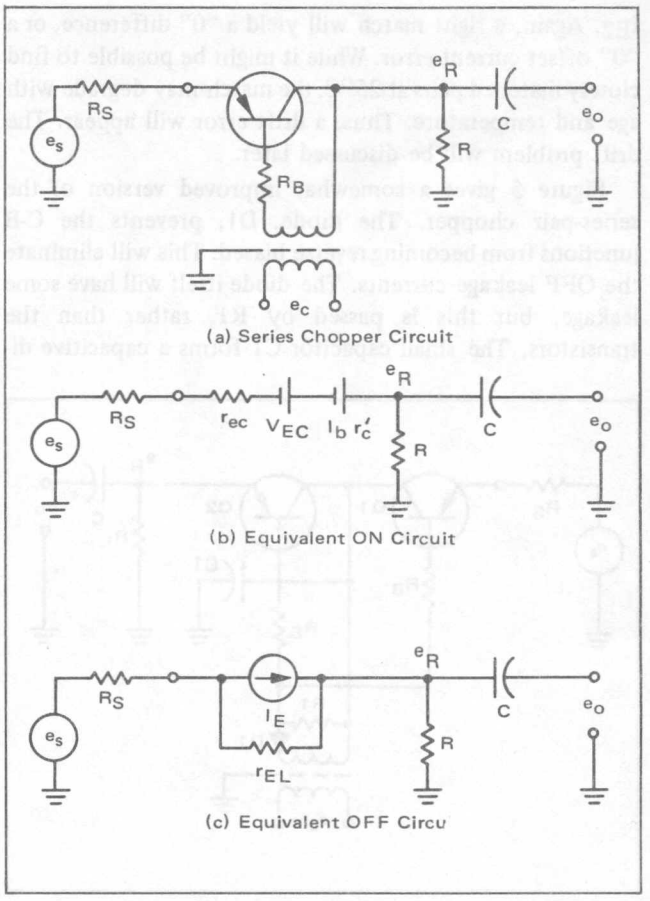

FIGURE 3 – Series Chopper Circuit

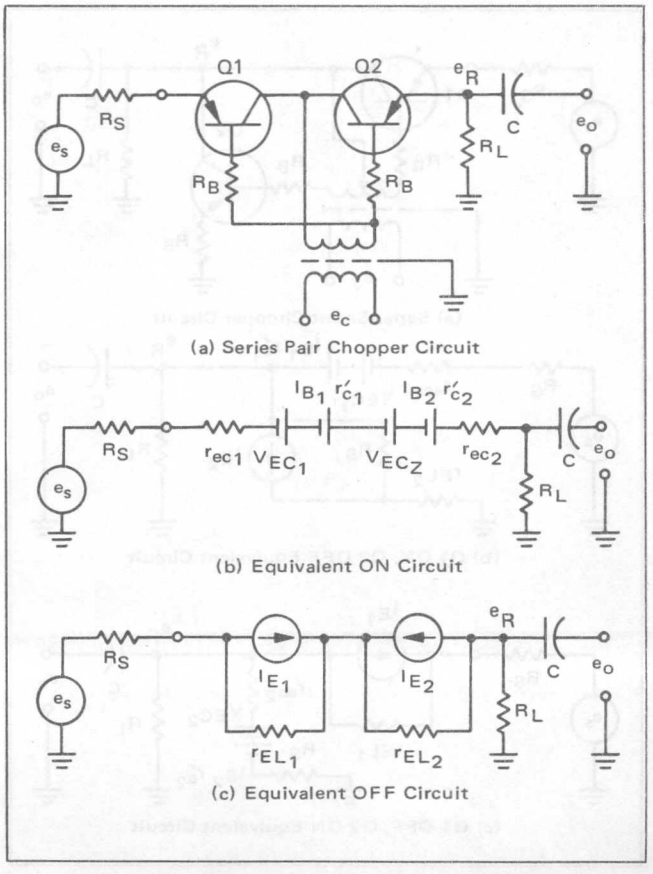

FIGURE 4 – Series-Pair Chopper Circuit

I_{E2}. Again, a tight match will yield a "0" difference, or a "0" offset current error. While it might be possible to find closely matched pairs at 25°C, the match may degrade with age and temperature. Thus, a drift error will appear. The drift problem will be discussed later.

Figure 5 gives a somewhat improved version of the series-pair chopper. The diode, D1, prevents the C-B junctions from becoming reverse biased. This will eliminate the OFF leakage currents. The diode itself will have some leakage, but this is passed by R1, rather than the transistors. The small capacitor C1 forms a capacitive divider with the transistor junction capacitance. This helps suppress feedthrough transients.

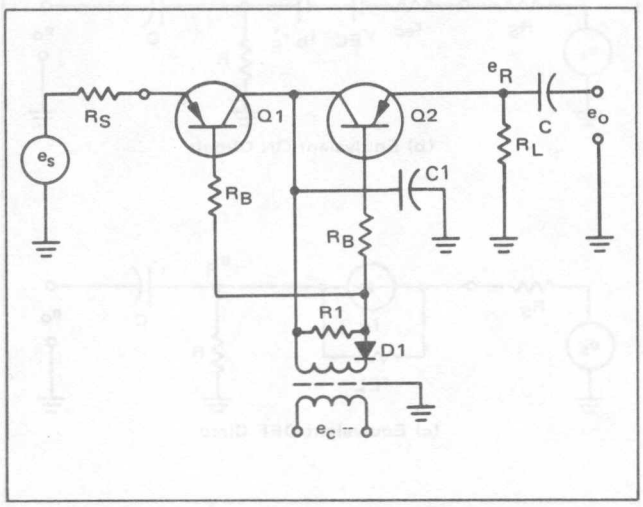

FIGURE 5 – Modified Series-Pair Chopper Circuit

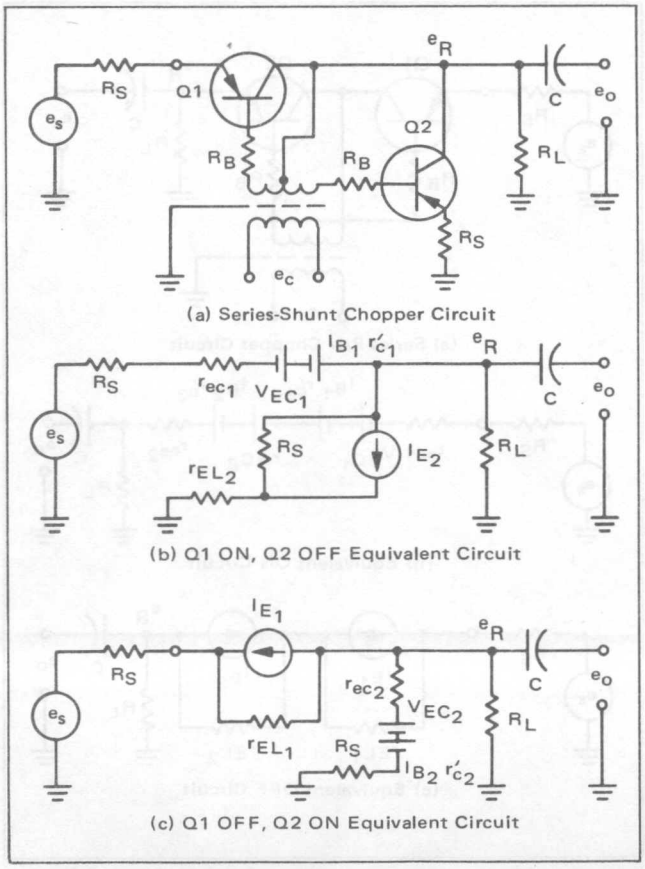

FIGURE 6 – Series-Shunt Chopper Circuit

The improvements in Figure 5 are not without disadvantages. The "0" off-bias mode and capacitive divider circuits will both tend to increase switching times. A tradeoff between speed, leakage, and feedthrough must be made.

Another circuit designed to reduce the effects of offsets is the series-shunt chopper shown in Figure 6. The chopping signal is so coupled that while the series device is ON, the shunt device is OFF and vice-versa. These two states are shown in the equivalent circuits of Figures 6B and 6C.

Consider the state shown in Figure 6B. The series device is turned ON, while the shunt device is OFF. Assume the signal e_s is at "0". The voltage across R_L is

$$e_R(1) = V_{EC1} + I_{B1}\, r_{c1} - I_{E2}\,(R_S + r_{ec1}) \qquad (15)$$

if

$$R_L \gg R_S + r_{ec1}, \qquad (16A)$$

and r_{EL2} is very large.

Now, for "0" input, the voltage across R_L in Figure 6C is

$$e_R(2) = V_{EC2} + I_{B2}\, r_{c2} - I_{E1}\,(R_S + r_{ec2}) \qquad (17)$$

if

$$R_L \gg R_S + r_{ec2}, \qquad (16B)$$

and r_{EL1} is very large.

If the devices are tightly matched, the voltage across R_L (exclusive of signal voltage) will be constant. Therefore, the capacitive coupling of this voltage will result in no offset appearing at e_o. Again, a loss of match due to age or temperature drift can result in some offset appearing at e_o.

A control of drift offset and feedthrough of transients is achieved by lowering R_L. However, the condition imposed by equations (16) must be observed.

In the circuits discussed so far, it has generally been assumed that the impedance of the signal source, R_S, was low. Under this assumption, any offset voltage due to leakage current flowing through the source impedance was also low. There are instances, though, when the source impedance will be high. Under this condition, the leakage current-source impedance product may become intolerable.

By using a shunt chopper with "0" OFF bias, the $I_E R_S$ product can be eliminated. Figure 7 shows such a circuit. During the OFF time, the transistor looks like a pure resistance of high value. Thus, no leakage flows. However, the presence of the offset voltage during the ON time will result in an offset error in e_o. This can be removed by introducing a complementary offset later in the system, or by one of the two techniques in Figure 8.

In Figure 8A, diode D2 is ON during the OFF time of the transistor. The potentiometer can be used to introduce a small voltage equal to the offset voltage during the transistor ON time. The average dc voltage at the emitter (exclusive of signal voltage) is, therefore, constant.

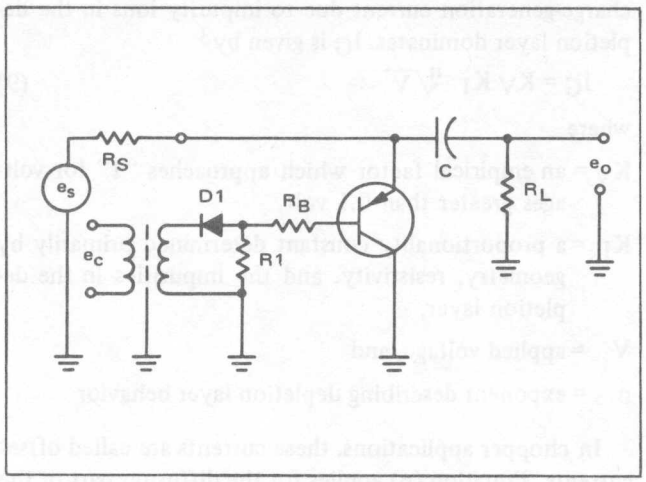

FIGURE 7 – Shunt Chopper Circuit

In Figure 8B, diode D2 conducts at the same time as the transistor. In this case it feeds a small reverse current through the transistor. The voltage drop caused by this current opposes the offset voltage. By properly adjusting the potentiometer, enough current can be introduced to cancel the offset.

DRIFT IN CHOPPERS

That the offset errors in a given chopper circuit have been adequately compensated does not guarantee that they will remain so as time passes and temperature changes. However, the effects of drift can also be minimized. When matched devices are being used for complementary compensation, it is reasonable to assume that device processing controls are tight enough that device matching with aging will be adequate.

Drift with temperature can be minimized by proper design. The degree of drift will, in general, be a function of temperature and drive. By testing the device over the desired operating temperature range for several levels of drive, the drive current for minimum temperature coefficient of offsets at the reference temperature can be determined. Then by designing the chopper drive circuitry to match the optimum drive level, minimum temperature drift for the device being used is obtained.

CONCLUSION

Bipolar chopper transistors provide attractive alternatives to mechanical choppers. Chopper transistors have disadvantages not present in mechanical choppers, but these disadvantages can be minimized through proper design. A properly designed chopper circuit can outshine mechanical systems in both performance and realiability.

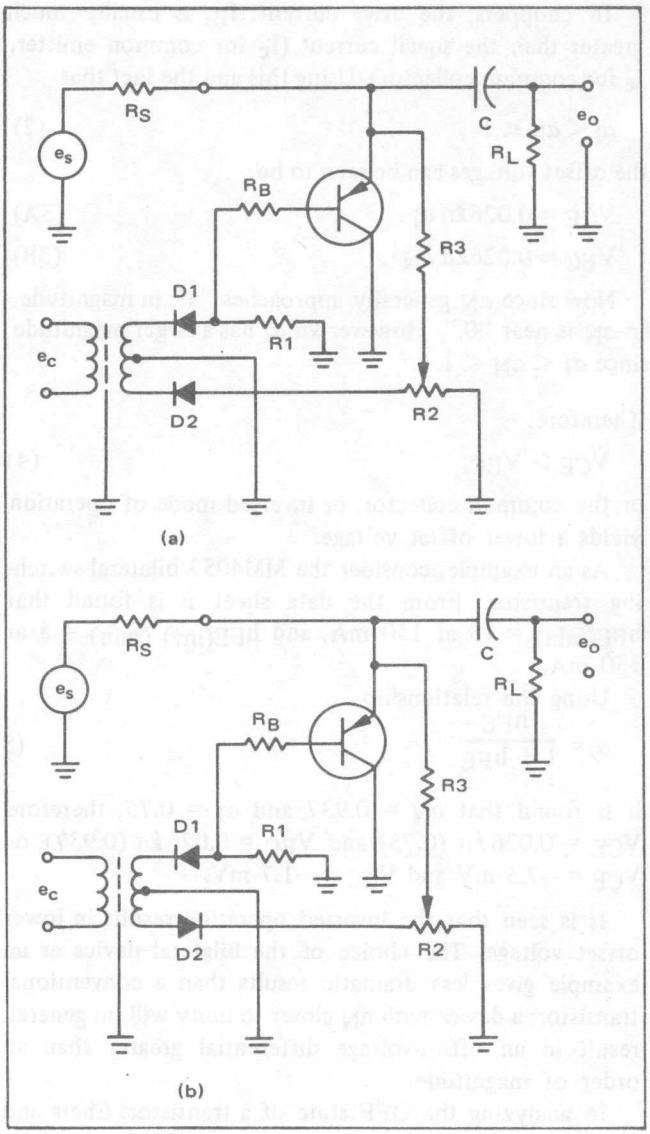

FIGURE 8 – Shunt Chopper Circuits with Offset Voltage Compensation

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