



MOTOROLA
Semiconductor Products

AN806A
Application Note

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OPERATION OF THE MC14469

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The MC14469 is an addressable asynchronous receiver transmitter that finds applications in control of remote devices, transfer of data to and from remote locations on a shared wire and as an interface from remote sensors to a central processor.

OPERATION OF THE MC14469

The MC14469 is an asynchronous receiver/transmitter fabricated in metal-gate CMOS technology. The asynchronous data format consists of a serial stream of data bits, preceded by a start bit and followed by one or more stop bits. The asynchronous data format is used to eliminate the need to transmit the system clock along with the data bit stream. The fact that the MC14469 is made in CMOS technology means that it offers the high noise immunity and low power consumption characteristic of this technology.

The MC14469 can receive one or two eleven-bit words in a serial data stream. The first received word contains a seven-bit address and if it matches the programmed address of the receiver, the transmitter can be enabled to transmit its two data words. The 7 bits of the received address word must correlate bit by bit with the 7 address pins of the MC14469. A second word may optionally be received for data or control use. This word will contain seven data bits which will be latched onto the command data outputs if it has a valid command format. With 7 address lines, 2^7 or 128 separate units may be interconnected for simplex or full duplex data transmission. The MC14469 is capable of operation at data rates in excess of 30,000 baud controlled by an on chip oscillator. Applications include transmitting data from remote A/D converters, temperature sensors, or remote digital transducers as well as single line control of remote devices such as motors, lights or security devices.

DEVICE OPERATION

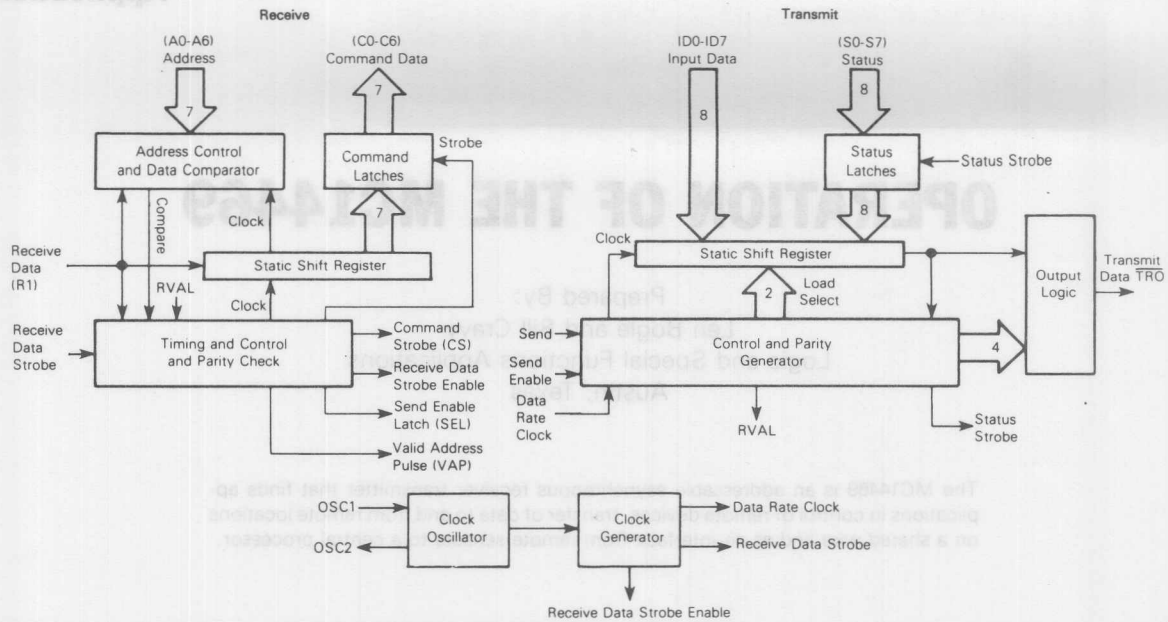
As shown in the block diagram of Figure 1, the MC14469 consists of three different sections: the receiver, the transmitter, and the oscillator. The receiver must receive (at least) a valid address on its receive data input (pin 19) in order to set up the necessary internal conditions to allow the transmitter to transmit its two data words. The address word consists of

a start bit, seven address bits, the address identifier, an even parity bit and a stop bit. The address will be valid only if: a) the seven address bits match the address that is programmed on input pins A0 through A6, b) if the address identifier is high, and c) if the state of the parity bit causes the total number of ones in the address word, including the address identifier and parity bit, to be even. After reception of a valid address, the MC14469 can optionally receive a command word. Similar to the address word, the command consists of a start bit, seven data bits, a command identifier, an even parity bit and a stop bit. The command will be valid if the command identifier is low and the total number of ones, including the parity bit, is even. The reception of either a valid address or both valid address and a valid command can be used to set up the necessary internal conditions for transmission. The format of address and command words is shown in Figure 2.

Upon receipt of a valid address data stream, the MC14469 generates a valid address pulse (VAP) which in turn sets the internal valid address latch (VAL) and the internal send enable latch (SEL). See Figure 3 for a timing diagram. SEL remains high for eight data bit times or until the send input (pin 30) is taken high. If SEL is allowed to time out and a valid command word is subsequently received, a command strobe (CS) is generated which sets SEL high again. It again remains high for eight data bit times after being set. However, once the valid address latch (VAL) is set high, it will remain high until SEND goes high and resets it.

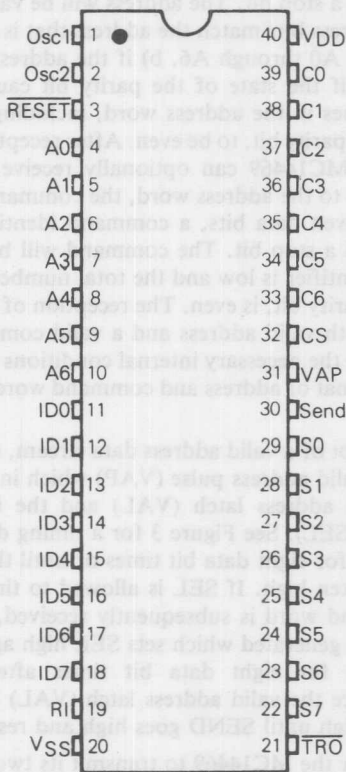
In order for the MC14469 to transmit its two data words, SEND must receive a rising edge while the valid address latch and send enable latch are both set high. Therefore, a send input must occur within eight bit times after the generation of either a valid address pulse or a command strobe, depending on the system configuration. After eight bit times, SEL will time out and transmission will be inhibited.

Figure 1A. MC14469 Block Diagram



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Figure 1B. Pin Assignments



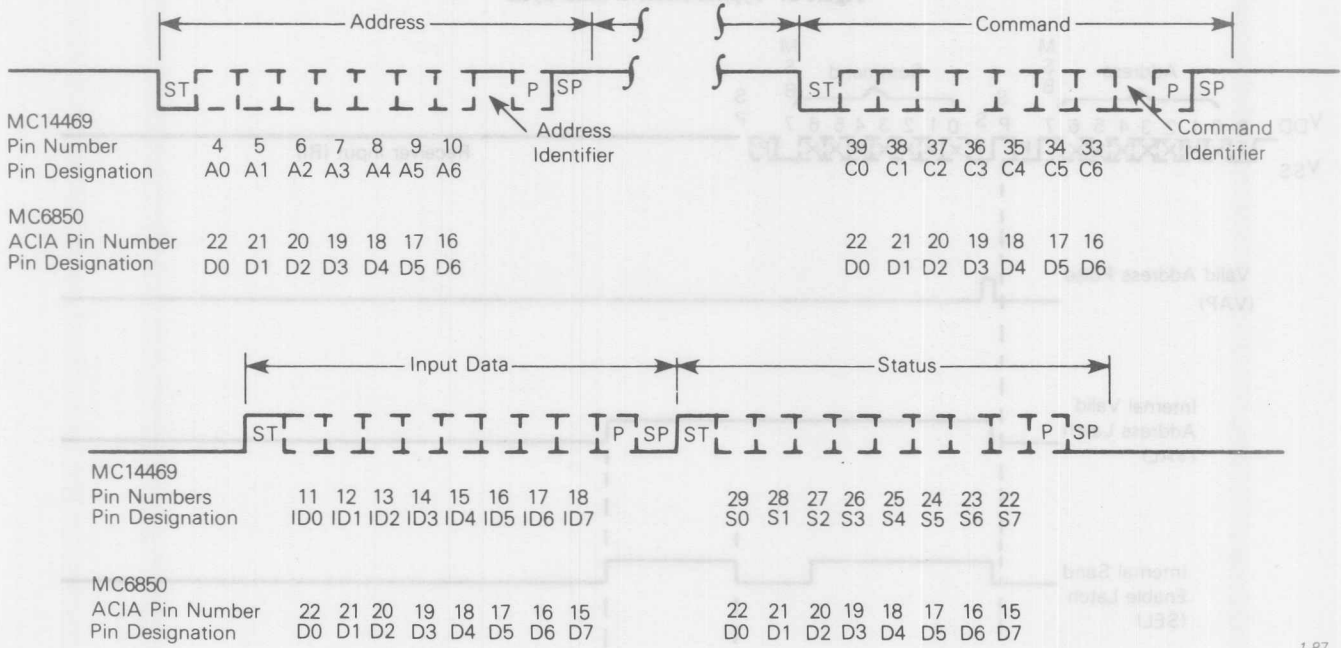
SEND going high resets VAL and SEL, and initiates the transmission of the data defined by input pins 11-18 and the status word defined by input pins 22-29. The transmitted words each contain a start bit, eight data bits, an even parity bit and a stop bit, all in UART compatible format. The transmitted data has the format shown in Figure 3. Note that the transmitted data must be inverted before being presented to the receiving device. This is usually accomplished by the line driver or transistor used to drive the common transmit wire.

OSCILLATOR OPERATION

The oscillator can be controlled by a ceramic resonator, a crystal or by an externally generated clock, and will typically operate at frequencies up to 2 MHz at a VDD of 12 V. The oscillator frequency is divided by 64 to derive the receive data strobe and the data rate clock. Thus, the data bit period is 64 times the oscillator period. To allow for maximum phase jitter, the receive data strobe is centered at the middle of each data bit. The receipt of a start bit initiates the receive data strobe and synchronizes the strobe to the receive data bit stream.

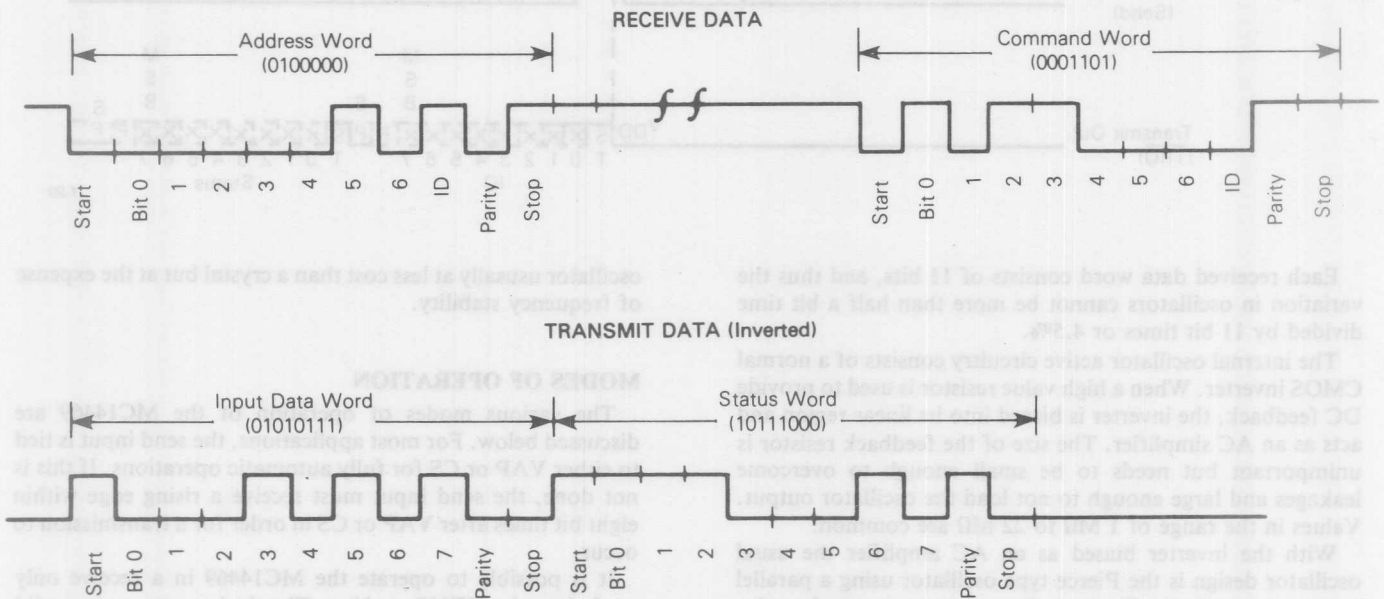
Since data is sent asynchronously, the transmit oscillator and receive oscillator must be the same frequency to ensure that the receive data strobe occurs at the middle of the bit period. The maximum permissible variation in oscillator frequency between a transmitting unit and a receiving unit can be such that over the entire receive data word time the total error is plus or minus one-half data bit period.

Figure 2A. Data Format



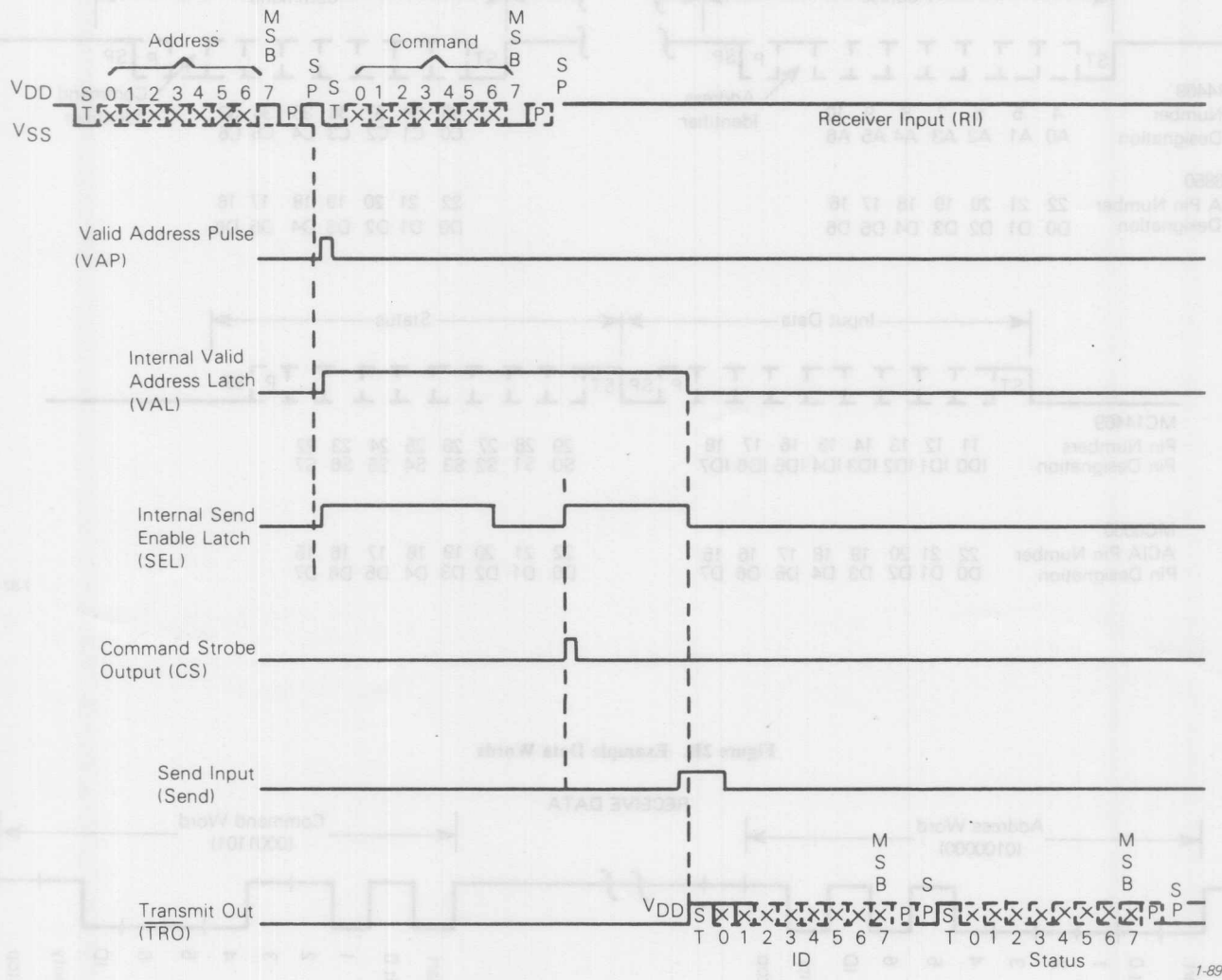
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Figure 2B. Example Data Words



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Figure 3. Typical Receive/Send Cycle



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Each received data word consists of 11 bits, and thus the variation in oscillators cannot be more than half a bit time divided by 11 bit times or 4.5%.

The internal oscillator active circuitry consists of a normal CMOS inverter. When a high value resistor is used to provide DC feedback, the inverter is biased into its linear region and acts as an AC simplifier. The size of the feedback resistor is unimportant but needs to be small enough to overcome leakages and large enough to not load the oscillator output. Values in the range of 1 MΩ to 22 MΩ are common.

With the inverter biased as an AC amplifier the usual oscillator design is the Pierce type oscillator using a parallel resonant crystal. See Figure 4. Two capacitors, one from input to ground and one from output to ground, present the required capacitive load to the crystal. The series connection of the capacitors through ground avoids feedback of signal through the parallel capacitive path. An inductor or ceramic resonator can be substituted for the crystal to form a Colpitts

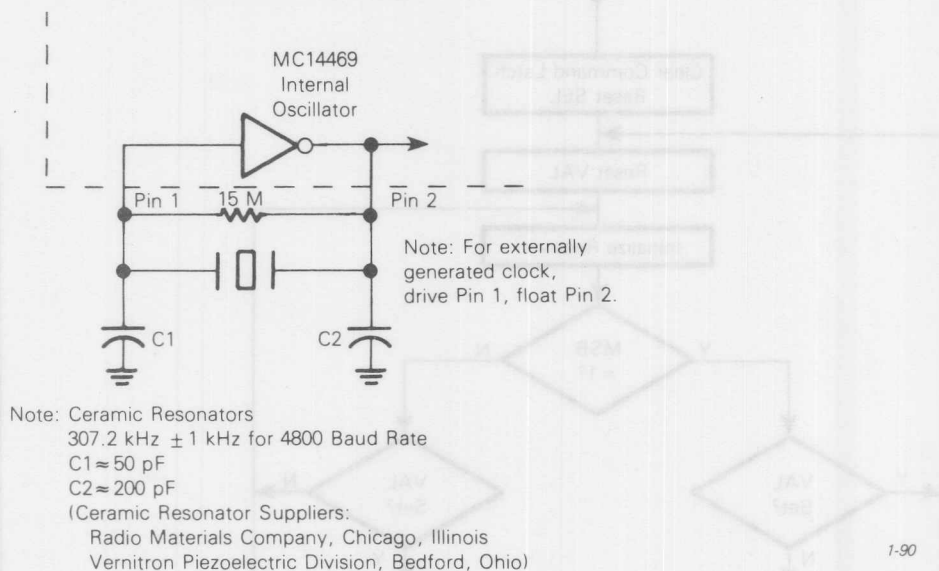
oscillator usually at less cost than a crystal but at the expense of frequency stability.

MODES OF OPERATION

The various modes of operation of the MC14469 are discussed below. For most applications, the send input is tied to either VAP or CS for fully automatic operations. If this is not done, the send input must receive a rising edge within eight bit times after VAP or CS in order for a transmission to occur.

It is possible to operate the MC14469 in a receive only mode by tying SEND to VSS. The device can receive valid address words only or both address and command words. Three different modes of operation of the MC14469 are possible depending on the signal used to drive the SEND input. These are RECEIVE ONLY MODE, SEND EQUALS VAP and SEND EQUALS CS.

Figure 4. Oscillator Circuit



RECEIVE ONLY MODE

If the MC14469 is in the receive only mode (i.e., if SEND is tied to VSS) and if it is receiving valid address words only, it will respond with a valid address pulse after every other valid address. The intervening addresses will cause no output. The reason for this can be seen by examining the flow chart (Figure 5).

Assume the MC14469 has been reset, the receiver is initialized and is ready to be addressed. If the MSB of the first word received is a one (signifying an address), the device checks to see if the valid address and send enable latches are set. If neither is set, and if the word is a valid address, VAL and SEL are set and a valid address pulse is generated. If SEND is not taken high within eight bit times, SEL is reset and the device is re-initialized and ready to receive a command. If the next word received is an address rather than a command, the MC14469 will find that VAL is still set. It will then reset VAL, initialize the receiver, and wait for another address to be sent. As a result, the second consecutive address to be received will not result in the generation of a VAP. This problem does not arise when the device is enabled to transmit every time it is addressed, since VAL is reset during the transmission cycle. Notice that once VAL has been set by the reception of a valid address, the only way it can be reset without rejecting an address is by going through the transmission cycle.

A similar situation arises when the MC14469 is in the receive only mode and valid addresses and valid commands are alternately received. On the reception of the first valid address, VAL and SEL are set and a VAP is generated. After eight bit times, SEL is reset and the receiver is re-initialized. If the next received word is a command, the MSB will be zero, and when the device checks the valid address latch, it will find that it is set. If the command word has a valid format, it will be latched onto the command data outputs (C0-C6). A command strobe will be generated and the send enable latch will be set. Once again SEL will be reset after eight bit times and the receiver will be re-initialized. Thus, the reception of the first valid address and command words

will result in the generation of a valid address pulse and a command strobe respectively, as expected. However, since data has not been transmitted, the next incoming address word will be rejected because the valid address latch has not been reset. The MC14469 will then reset VAL and re-initialize the receiver. The following word is a command word and because the valid address latch is not set, the command is also rejected and the receiver is re-initialized.

The next address and command words received will result in the generation of a VAP and CS. Thus, in the receive only mode, every other address and command words will be rejected.

SEND EQUALS VAP

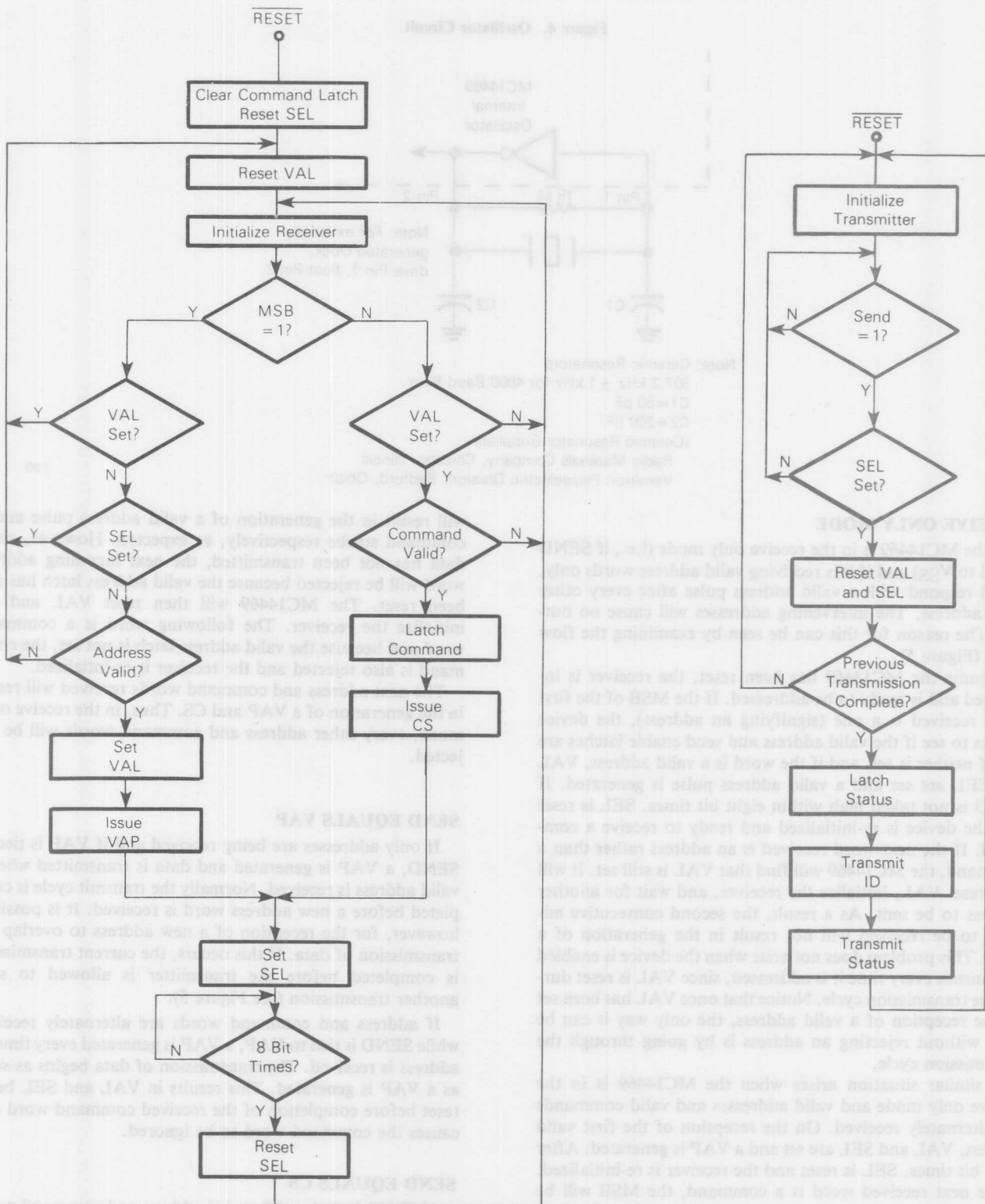
If only addresses are being received and if VAP is tied to SEND, a VAP is generated and data is transmitted when a valid address is received. Normally the transmit cycle is completed before a new address word is received. It is possible, however, for the reception of a new address to overlap the transmission of data. If this occurs, the current transmission is completed before the transmitter is allowed to start another transmission (see Figure 5).

If address and command words are alternately received while SEND is tied to VAP, a VAP is generated every time an address is received. The transmission of data begins as soon as a VAP is generated. This results in VAL and SEL being reset before completion of the received command word and causes the command word to be ignored.

SEND EQUALS CS

If SEND is tied to CS and if address and command words are alternately received, a VAP and CS are generated every time an address and command are received. Data is transmitted every time a CS is generated. Once again, data transmission can overlap the reception of a new address and command word. However, the current transmission will be allowed to finish transmitting (see Figure 5).

Figure 5. Flow Chart of MC14469 Operation



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THE MC14469 AS A MASTER TRANSMITTER

The MC14469 can transmit only after it has received a valid address. For this reason it is usually considered to be a remote or slave device controlled by a UART, MPU or similar control system. However, it is possible to use the MC14469 as a master transmitter by giving it a start pulse on its receive input that has the format of a valid address. The idea is to set the address of the MC14469 that is to be used as a master transmitter in such a way that a valid address will consist of a single pulse which goes low for a certain number of bit times and then goes back high and remains high. This will allow the use of a one-shot or RC network to generate a start pulse which will look like a valid address to the MC14469. On receiving the start pulse, the MC14469 will

generate a valid address pulse which can be tied to the SEND input in order to initiate a transmission.

As shown in Figure 2B, if the address of the MC14469 has an even number of ones, the parity bit will be high. The address identifier and stop bit are also high. Therefore, if the address begins with any odd number of zeros and ends with an even number of ones, the address word (start pulse) will need to go low for the start bit, stay low for an odd number of address bits, go high for the rest of the address bits, the address identifier, parity and stop bits. For example, if the address of the MC14469 is set to hex 00, a valid address will consist of a signal which goes low for eight bit times and then goes back high (see Figures 6 and 7). The other addresses for which the scheme will work are hex 60, hex 78 and hex 7E.

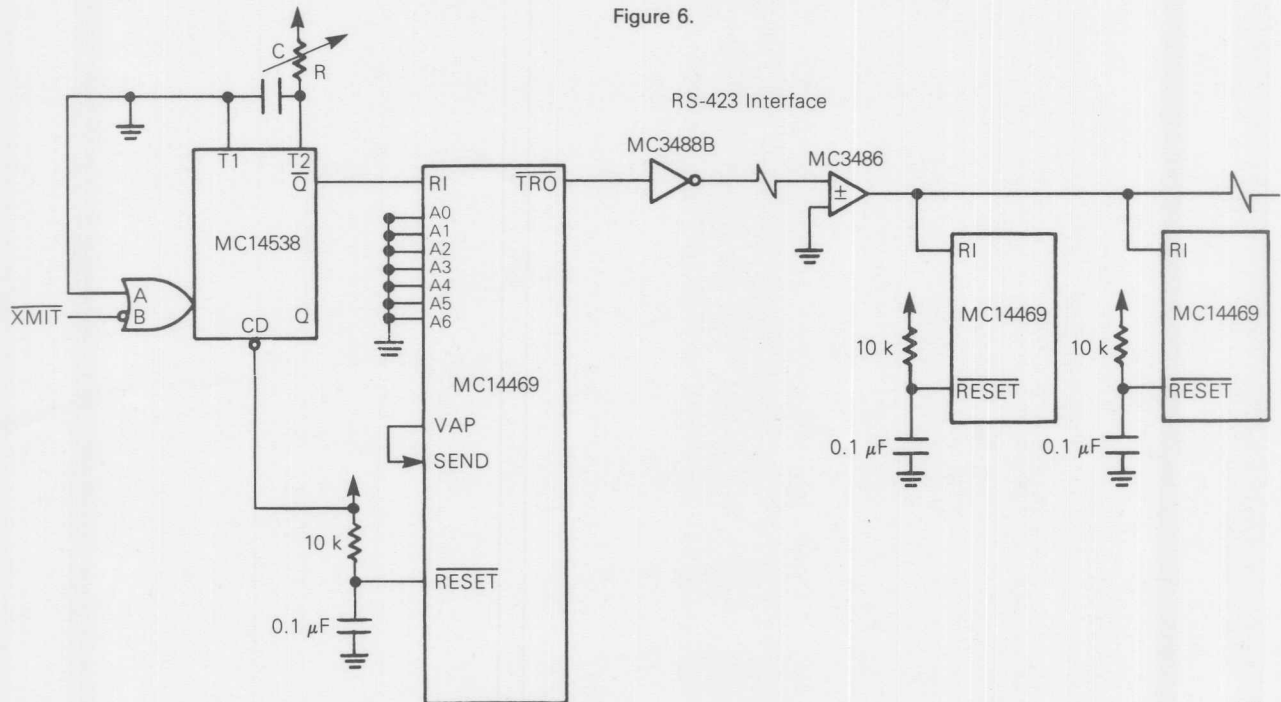


Figure 6.

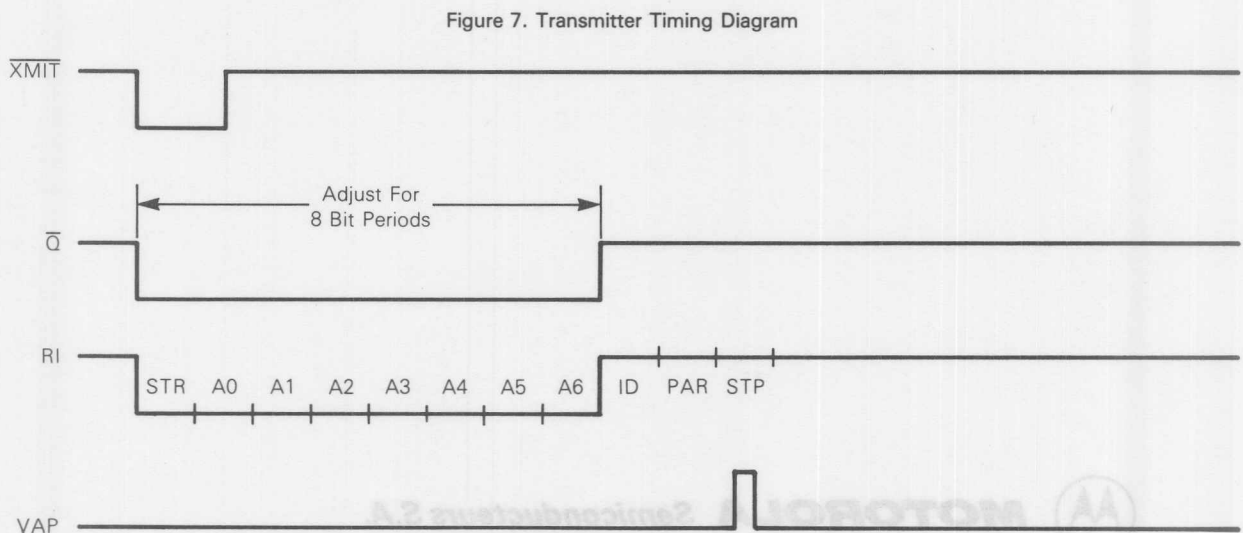


Figure 7. Transmitter Timing Diagram

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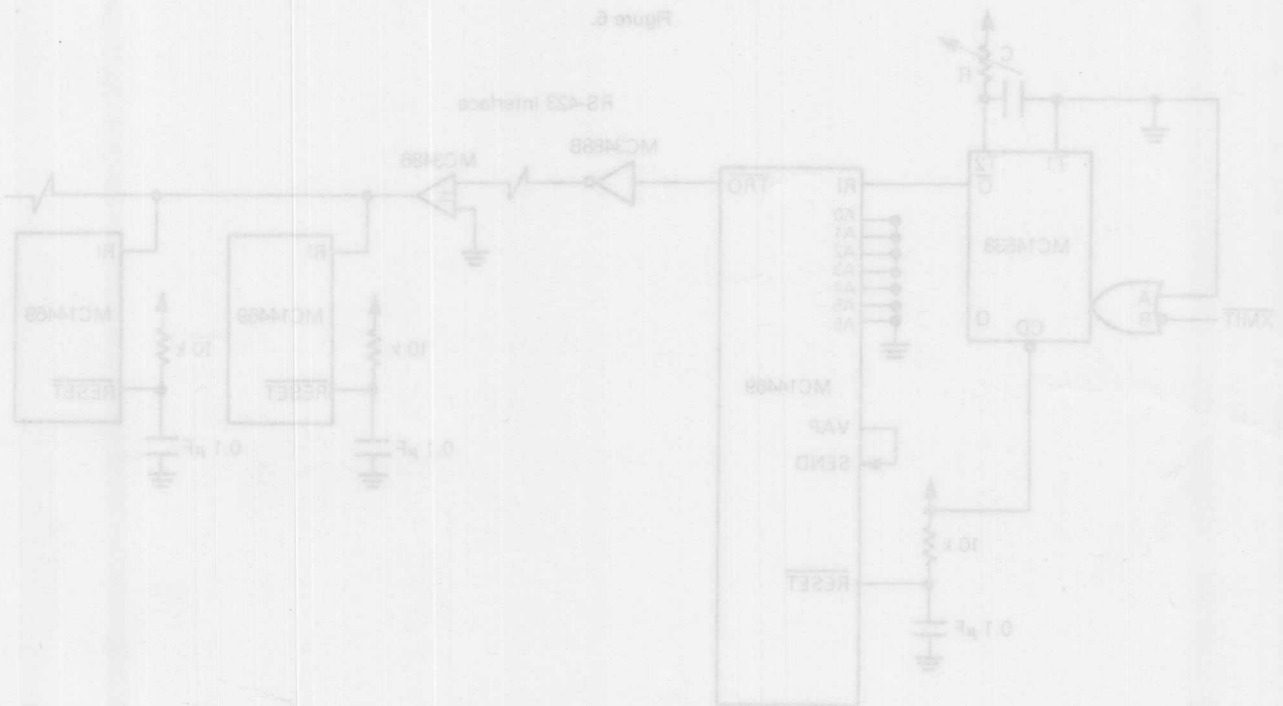


Figure 6

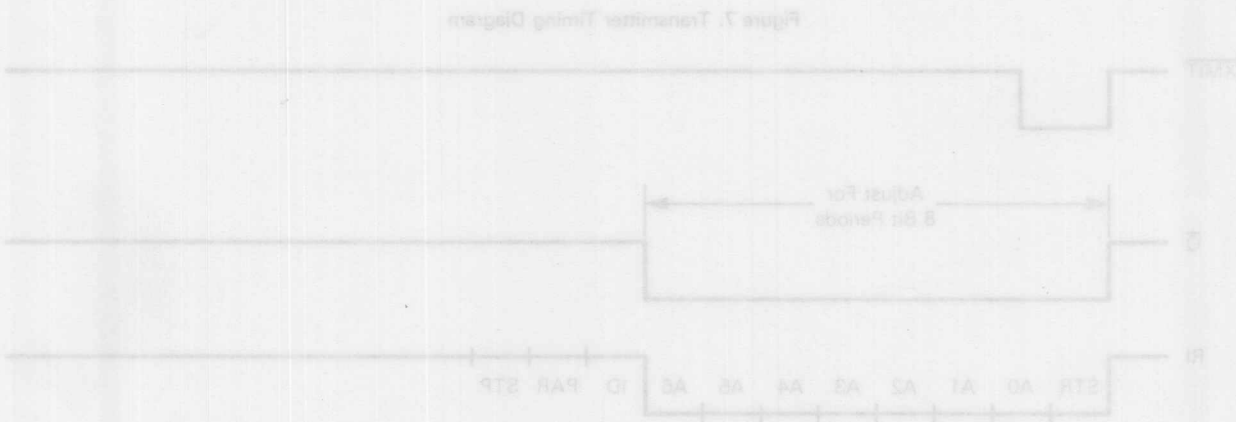


Figure 7. Transmitter Timing Diagram



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