NS8050U MICROWIRE PLUS™ Interface

National Semiconductor
Application Note 358
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INTRODUCTION

MICROWIRE™ is a serial communications interface from National Semiconductor. Originally devised to allow the COPS™ Microcontrollers to effectively communicate with peripheral devices, it has now been extended to the 8-bit 8048 microcontroller family. This extension is known as MICROWIRE PLUS.

The NS8050 from National Semiconductor, slated shortly for release, incorporates MICROWIRE PLUS. Its existence is entirely transparent to normal 8050 operation and is only activated upon execution of a new MICROWIRE PLUS instruction. This application note describes the features of the extension and presents programming examples to illustrate how to use MICROWIRE PLUS.

MICROWIRE PLUS

The MICROWIRE PLUS protocol utilizes a 3-wire interface working in conjunction with a clocked eight bit input/output shift register, *Figure 1*. The shift register is referred to as the Serial Input/Output (SIO) register. The three interface signals are Serial Output (SO), Serial Input (SI), and Serial Clock (SK). The contents of the accumulator may be exchanged with the SIO register thus providing us a means of performing the parallel to serial data conversion. Data waiting to be transmitted in the SIO register is clocked out on the SO pin on the falling SK clock edge. Serial data is received on the SI pin and clocked into the SIO register on the rising SK clock edge.

On reset the NS8050 comes up in the normal mode of operation. The MICROWIRE mode of operation may be invoked by executing one of two new instructions, XCHM or XCHS. Both instructions cause the Accumulator and SIO register to exchange data, with the differences being in the SK clock generation. In Master mode, set by XCHM, the SK clock is generated internally and output to other devices. In Slave mode, set by XCHS, the SK clock is input into the chip from a master source. Once the MICROWIRE mode has been selected it remains in effect until a system reset restores the normal mode of operation. The only practical difference

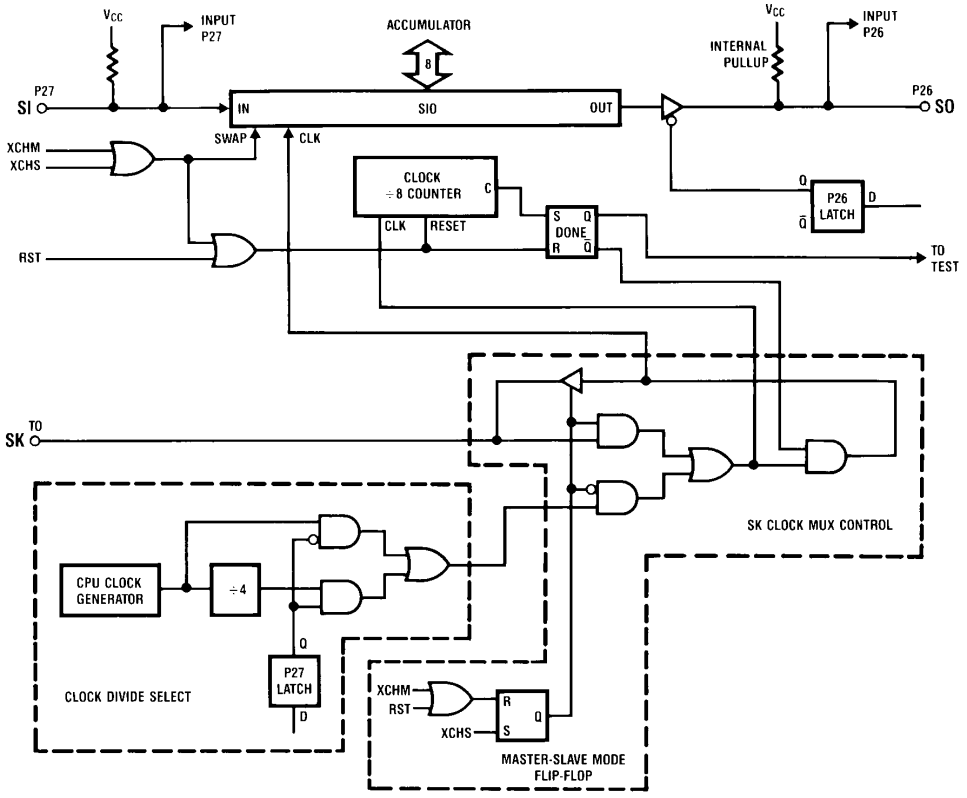

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FIGURE 1. Microwire Mode Functional Configuration

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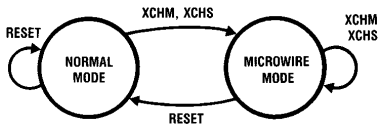
between the 2 operating modes are the dedication of 3 I/O pins to MICROWIRE operation. However, once in MICROWIRE mode, the chip may switch between Master and Slave operation at will.



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The 2 new instructions and their associated operations are as follows:

Mnenomic	Opcode	Operation
XCHM	C0	A < = > SIO. Reset DONE flip-flop, Clock counter. SK designated as an output. MICROWIRE mode selected.
XCHS	C1	A < = > SIO. Reset DONE flip-flop, Clock counter. SK designated as an input. MICROWIRE mode selected.

For MICROWIRE PLUS applications, one NS8050 must be designated as the Master. The Master supplies the SK clock for the system and initiates all data transfers between itself and one of the Slave devices. A Slave may be any of the standard MICROWIRE peripheral chips or another MICROWIRE PLUS NS8050 operating in Slave mode. In a typical system the Serial Clock (SK) is tied together on all the chips. The Serial Out (SO) from the Master is tied to the Serial In (SI) on all the Slaves. Similiarly, the Serial in (SI) pin on the Master is tied to the Serial Out (SO) on all the Slaves. General purpose outputs on the Master are used to chip select various Slave devices onto the MICROWIRE PLUS bus.

Among the various standard MICROWIRE peripherals available are display drivers (LCD, VF, LED), memories (RAM, EEROM), A/D converters, and frequency generators/timers.

NS8050 HARDWARE MODIFICATIONS

Three of the general purpose I/O pins on the NS8050 become dedicated signals when operating in MICROWIRE mode as follows:

NS8050 Pin	Function Under MICROWIRE PLUS	
T0	Serial Clock Input or Output	(SK)
P26	Serial Data Output	(SO)
P27	Serial Data Input	(SI)

In addition, upon entering MICROWIRE mode the port latches associated with P26 and P27 are disconnected from the port and used instead as configuration registers. They are still loaded by using the NS8050 port instructions with the following MICROWIRE PLUS functions selectable:

- P36 latch is used to Enable/Disable the TRI-STATE SO output.
  - 1 = Disabled
  - 0 = Enabled
- P27 latch is used to select the SK output frequency.
  - 1 = Instruction cycle clock divided by 4 (crystal freq/60)
  - 0 = Instruction cycle clock divided by 1 (crystal freq/15)

As in other chips in the 8048 family, RESET causes the latches associated with Ports 1 and 2 to set to a ''1''. Consequently if the P26 and P27 latches are not otherwise initialized, upon entering MICROWIRE mode the SO output will be disabled and divide by 4 selected for SK generation. However P26 and P27 may be modified at any time, even when in MICROWIRE mode.

When in MICROWIRE mode, port pins P26 and P27 may still be read in using the IN A, P2 instruction and will reflect the state of the SO and SI pins respectively. Note however that these pins also have internal pullup devices connected to them as shown.

To facilitate data transfers a DONE flip-flop has been included in the MICROWIRE circuitry. It and the clock counter are Reset upon every exchange between the Accumulator and the SIO register. When the clock counter reaches a count of 8, indicating that the SIO has completely shifted out, DONE is set. The DONE F/F is connected internally to the T0 sense line upon entering the MICROWIRE mode, thus allowing it to be tested by the JT0 and JNT0 instructions. Because of this any of the other T0 functions such as clock generation are precluded from operation while in MICROWIRE mode. It should be noted that the SK clock may only be shut down by the DONE F/F which in turn is driven by the Clock Counter. The Clock Counter may only be preset by 0 by an XCHM or XCHS instruction after which it will immediately start counting clock pulses.

APPLICATION NOTES

MICROWIRE PLUS may be effectively used for Local Area Networks (LANs) and Small Area Networks (SANs). Possible applications range from setting up a communications network within an automobile to home security systems. With the ability to switch between a MICROWIRE Master and Slave device at will, a multi-master NS8050 bus network may be implemented.

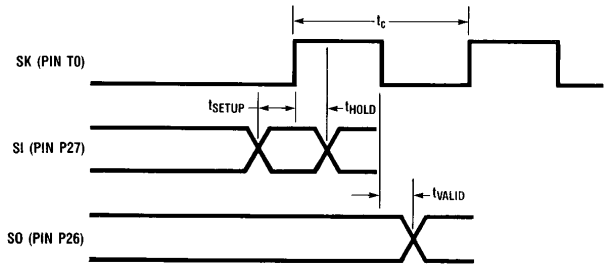
In NS8050 only systems MICROWIRE data may be transferred at the instruction cycle time of 1.36 μs (733 kHz). When using standard MICROWIRE peripherals data transfers must generally be restricted to 4 μs (250 kHz) as shown in *Figure 2a*. Also shown are typical MICROWIRE setup and hold times on the data lines relative to the SK clock. *Figure 2b* illustrates SIO bit shifting relative to instruction execution. When counting out instructions the XCH should be placed so that the last bit will be shifted in and out while the instruction is being read in as shown in *Figure 2b*.

For both divide by 1 and divide by 4 clock generation modes the rising SK clock edge is approximately coincident with the rising ALE edge as shown in *Figure 3*. For divide by 1 SK clock generation the duty cycle is 40% while for divide by 4 it is 50% (the ALE duty cycle is approximately 23%).

Since the same drive circuits are used for both normal and MICROWIRE modes of operation, the DC electrical characteristics are the same for the 3 I/O pins in either mode.

ON THE MICROWIRE 8050 THE CRYSTAL OSCILLATOR PINS ARE REVERSED FROM ORDINARY 8050s.

To facilitate 8050 MICROWIRE usage with standard COPS peripherals, a macro based I/O Driver Software Package is available. Written in 8048 assembly, it may be used directly or studied as an example of 8050 MICROWIRE peripheral interfacing.



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Parameter	Typical	Units
t_{SETUP}	200	ns
t_{HOLD}	200	ns
t_{VALID}	50	ns
t_C	4	ns

FIGURE 2a. Microwire Interface Timing

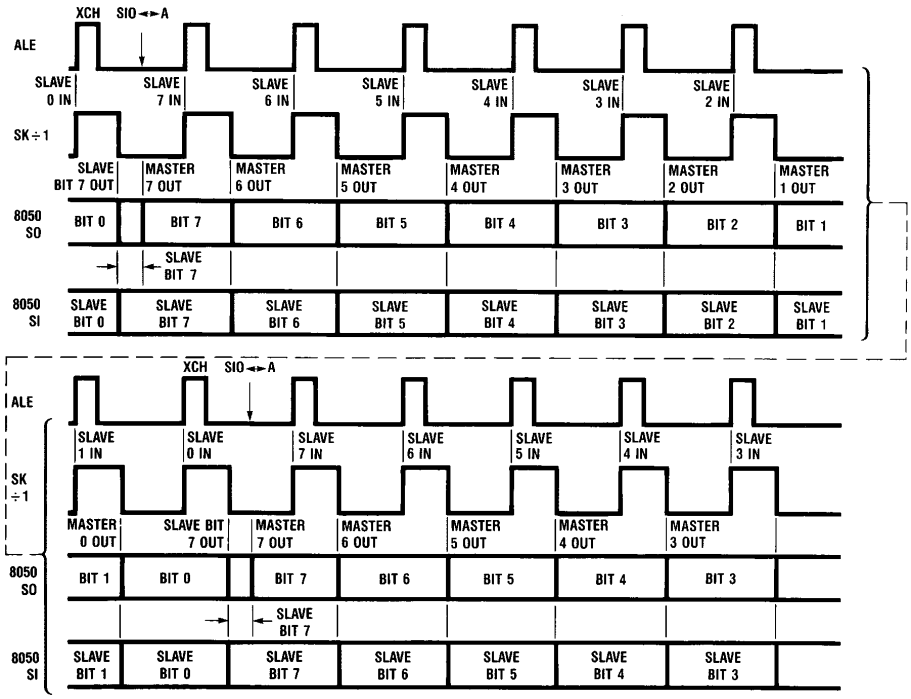

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FIGURE 2b. 8050 Microwire Serial Sequence

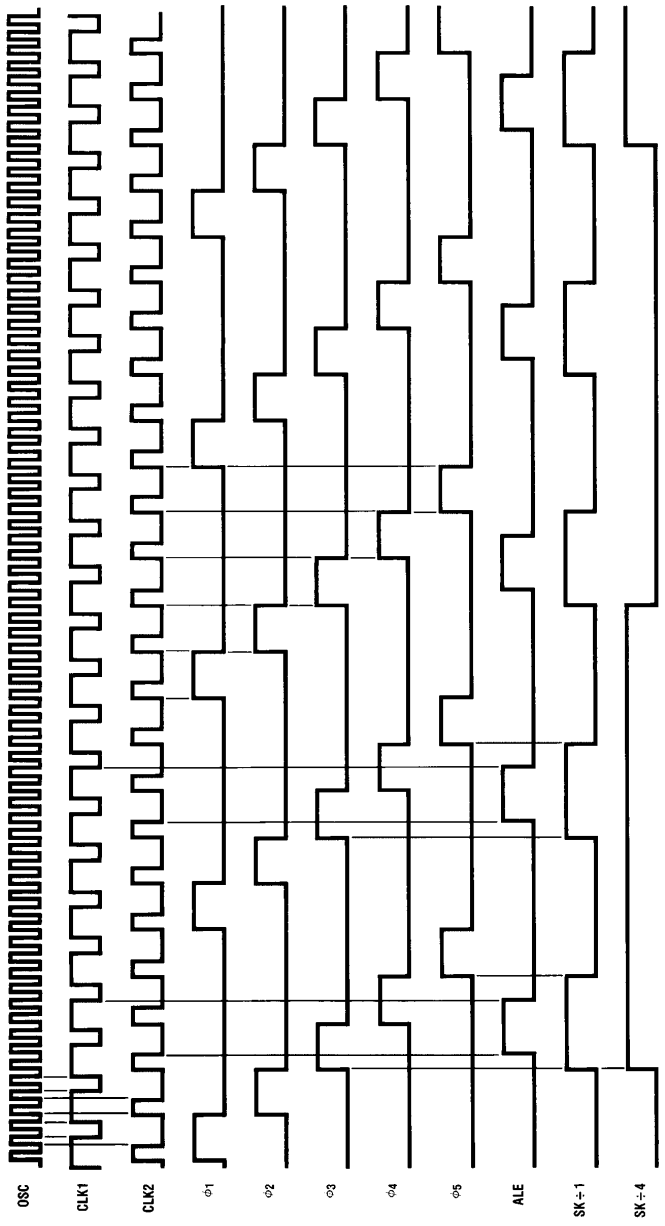

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FIGURE 3. NS8050 Microwire Clock Generation

MASTER-SLAVE PROTOCOL EXAMPLE

A number of handshake protocols are possible between a Master and Slave NS8050 in a MICROWIRE PLUS system. The following example illustrates one possible method and discusses the timing holds and restrictions on each device.

The hardware configuration for our example is shown in *Figure 4* and described as follows:

- Slave SO connected to Master SI
- Slave SI connected to Master SO
- Slave SK connected to Master SK
- Master pin P24 used to chip select slave, connected to Slave interrupt input
- Slave pin 25 connected to Master pin P25, used by slave as a BUSY output indicator
- Master and Slave have the same crystal frequencies to simplify things

Before starting our example we will also assume the following initial conditions:

- Master DONE flip-flop set causing SK clock generation to be shut down
- Master Clock divide by 4 selected (P27 latch set), SO enabled (P26 latch reset)
- Master P24 (Slave chip select) is high (inactive)
- Slave BUSY output (P25) is high (active)
- Slave DONE flip-flop is indeterminate

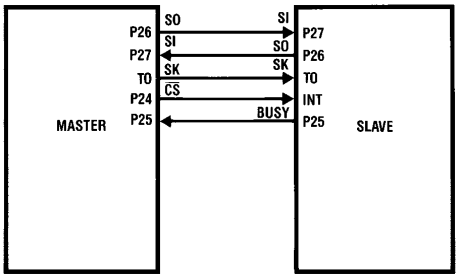

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FIGURE 4. Example Master-Slave Hardware Configuration

In our example of *Figure 5* the Master is performing a 2-byte write and read from the Slave. The following is a step by step description of the key steps in code execution.

1. Master wishes to send and/or receive data from Slave. He starts by activating the Slave chip select.
2. Slave chip select causes an interrupt service call where Slave loads his first data byte into the SIO, enables SO and resets BUSY. The SIO load also clears out the clock counter and DONE flip-flop.
3. All this time the Master was checking and waiting for BUSY to go away, thus signifying that the Slave has reorganized the chip select interrupt. The chip select is turned off and the Master loads his first data byte into the SIO thus commencing transmission.
4. Both Master and Slave now wait for 8 data bits to be transmitted as indicated by the DONE flip-flop.
5. Upon seeing that DONE is set, the Slave immediately turns BUSY back on. The Slave then saves the just received data byte, disables SO and returns from interrupt service.
6. After seeing that DONE is set, Master delays enough to ensure that the Slave has turned BUSY back on. Master delay might also want to be put in to allow the Slave time to return from subroutine and utilize the just received data byte or update pointers in preparation for the next interrupt service. Alternatively the Slave could disable interrupts until housekeeping had been performed.
7. The Master wants to send another data byte so he activates the Slave chip select once again. The sequence for the Slave is the same as before. In the Master the XCHM to load the second Master data byte into the SIO also brings in the first Slave data byte. It is stored and after the current transmission is through the second Slave data byte may be brought in. The first Slave data byte could have been brought in after the first Master WAIT sequence with an XCHM, but that would have initiated another 8 SK Clock sequence which we would have had to wait out since SK must be shut down before initiating another transfer.
8. Rather than use straight line code, memory pointers and loop counters could easily be incorporated if the handshake restrictions described above are accounted for.

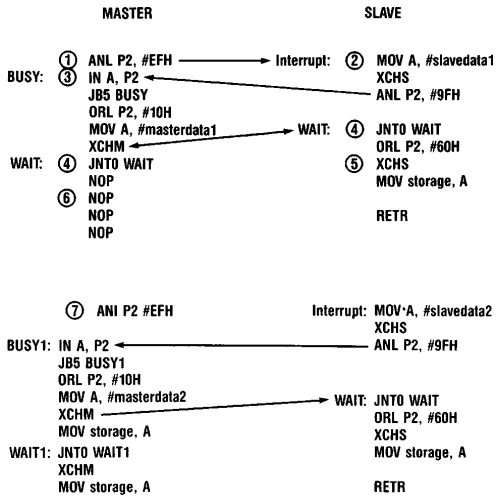

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FIGURE 5. Master-Slave Handshake Execution

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