A Novel Process for Vacuum Fluorescent (VF) Display Drivers

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Introduction

The recent introduction of Vacuum Fluorescent (VF) displays has provoked a great deal of interest in the market place in general, and in particular for use in automotive dashboard applications. Consequently, this attention has spread to the wide range of display drivers presently available. To take advantage of these displays, a new form of high voltage driver was required, at a lower cost than the previously available integrated circuit.

The Vacuum Fluorescent (VF) Display

The operation of a VF display is based upon that of a standard valve, where electrons are emitted from the cathode and are accelerated through the grid on to the anode. Initially, a filament element heats the electrons at the cathode, providing the electrons with the necessary energy for emission. If both the grid and the anode are at a positive potential with respect to the cathode, then the emitted electrons pass through the grid and onto the anode. In a VF display, the anode terminal is coated with a fluorescent material, which will emit light when bombarded by electrons. The general structure of such a display is shown in *Figure 1*. The anode areas correspond to individual segments of the display, and the grid is used to switch on and off whole digits, facilitating the option of multiplexed anodes. The brightness of the display varies directly with the voltage difference between cathode and grid/anode, and this has resulted in the need for high voltage drivers.

The type of display selected for an automotive dashboard is a critical decision, and there is a wide range from which to choose. Light emitting diode (LED) displays are commonly used in electronic dashboards at present, although they have the serious disadvantage of high power dissipation and a low level of brightness. Given the wide range of applications found for liquid crystal displays (LCD) in recent years, one might expect to find this technique applied to dashboards. However, LCD has the inherent disadvantage of a limited operating temperature range and the low temperature operation demanded in automotive applications results in difficulties when using present LCD technology as a substitute for LED. More modern display techniques, such as gas discharge or plasma, may provide a viable alternative in the future, but the technology has not been sufficiently proven at this stage. A VF display, on the other hand, is well suited to automotive applications because of its high brightness level, relatively low power consumption, and wide operating temperature range. Further, due to the recent introduction of thick and thin film techniques into display device manufacturing processes, it is with relative ease that high volumes of customer designed VF displays can be produced.

The application of VF displays to automotive dashboards demands additional requirements, because of the wide range of environmental conditions under which it must operate efficiently. In particular, it is imperative that the display characters are easily distinguishable in extreme light conditions. The visual recognition of the display information can be optimised readily by means of suitable filtering, and it is also desirable that the character brightness is variable. The latter could be achieved by altering the display voltage in proportion to signals from a light sensor mounted alongside the display on the dashboard.

High Voltage Display Drivers

EXISTING HIGH VOLTAGE DISPLAY DRIVERS

The most common, and indeed the most publicized type of display driver utilizes a mixture of MOS and bipolar technologies. While the logical areas of these devices operate as standard MOS 5V logic, each display output consists of a high voltage (up to 150V) Bipolar buffer. These output structures result from well known npn and pnp design techniques, e.g. emitter follower, Darlington pair, etc., where high output source currents (up to 100 mA) are the aim. These high current circuits appear to be the legacy from high power LED display drivers and, although capable of driving VF displays, such devices have several drawbacks. First and foremost they are expensive, mainly due to the inherent low density of Bipolar technology which, if many display outputs are included in the circuit, can significantly increase die size and hence cost. For certain desired output structures it may be necessary to include extra masking steps to the basic MOS process, e.g. to form an epitaxial layer, and this again will inevitably lead to increased costs. Further, the high current outputs result in very high power consumption on chip which, depending on the package used, may cause problems due to excessive die temperatures. Difficulties associated with power dissipation may lead to a reduction in the number of display outputs per chip, or at least a limitation on the number of segments illuminated simultaneously.

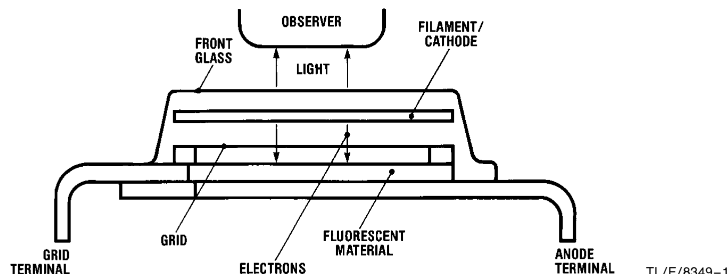

FIGURE 1. Cross-Section of a Vacuum Fluorescent (VF) Display

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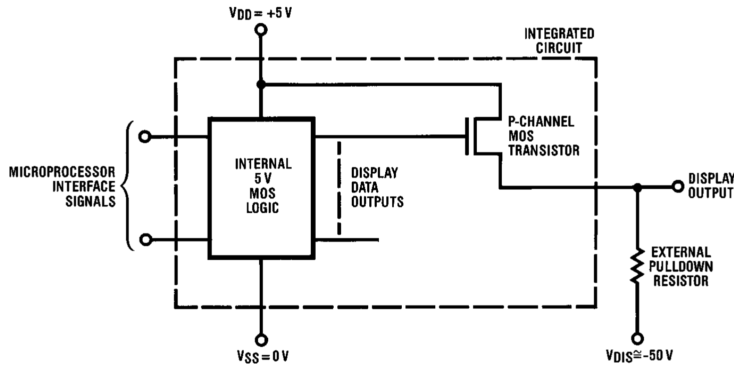

FIGURE 2. Example of a High Voltage MOS Open Drain Structure

Another readily available type of high voltage display driver is fabricated using MOS techniques only. Such devices use PMOS technology, and the high voltage output swings are achieved by means of open drain p-channel output transistors, as shown in *Figure 2*. Significant reductions in chip size can be achieved in this way, although such devices require one external pulldown resistor per display output. Consequently the board component count, and hence the system cost, will increase.

Surveying the literature, several points of interest emerge. First, there is a trend towards including far more decoding and control logic on chip, and it is likely that this has occurred due to the increasing use of high voltage displays in word processor applications. Thus, there is a demand for decoding of both ASCII character display data and ASCII control codes direct from the keyboard. In addition, it appears to be relatively rare to find display drivers with direct TTL data and clock inputs. Some devices cater for RS232 or other standard interface requirements, but many devices require some level shifting circuitry between the data source and display driver inputs.

THE 'IDEAL' VF DISPLAY DRIVER

As has already been stated, the operation of a VF display is similar to that of a valve and hence is a voltage controlled device. In addition, the nature of the fluorescent material is such that the amount of light emerging from the display is directly proportional to both the number of, and the speed at which the electrons arrive at the anode. The number of electrons emitted from the cathode is a function of the current in the filament and as such, has a limit. The acceleration of the electrons, on the other hand, is directly proportional to the voltage between the cathode and the grid/anode. Thus, one major requirement of the VF driver is that it is capable of large output voltage swings between the on and off conditions. At present, typical VF displays operate at a maximum cathode to grid/anode voltage of 50 volts, and so it is essential that the driver can produce output swings of at least 50V.

Coupled with the discussion on output voltage capabilities, an examination of the display output current requirements should be undertaken. The previous conclusion, that the VF display is a voltage controlled device, suggests that high current outputs are not required (typically 5 mA for a segment and 10 mA for a digit). The driver output must charge and discharge the display capacitance in such a time as to avoid visible flickering or ghosting effects. Given that most VF displays now have multiplexed anodes, and that the refresh rate must be greater than 100 Hz to prevent the above effects, then it can be seen that charge/discharge times in excess of 100 μsecs can be tolerated. A typical VF display has a capacitance of 20 pF and if the output off resistance is 200 KΩ, then a discharge time constant of 4 μsecs can be anticipated, more than adequate for the demands of the human eye.

Another desirable characteristic of the VF driver is that it has internal pulldown resistors on each of its display outputs. Thus, the complete structure shown in *Figure 2* can be incorporated on to the integrated circuit, and this will reduce component count and hence cost. The value of this resistor is critical in terms of both output voltage swing and standby power consumption, and as such is a parameter which must be closely defined. In addition, because low power consumption is desirable, the 5V logic on chip should dissipate as little power as possible and for this reason complementary MOS (CMOS) is the optimum processing technology to be used.

The cost of the finished product is closely related to the complexity of the fabrication process used and so the most proven of the available CMOS processes should be chosen. Thus, metal gate CMOS will be the process used.

Standard Metal Gate CMOS Processing

Examining the requirements outlined in the previous section, it is clear that metal gate CMOS design techniques can provide low power 5V internal logic and TTL microprocessor interface inputs with relative ease, using existing methods. Hence, it is the other requirements, namely high voltage outputs and on chip pulldown resistors, which demand closer attention.

OPERATING VOLTAGE LIMITATIONS

The electrical parameters which accompany the CMOS metal gate design rules state that 18V is the maximum voltage of operation of any circuit designed according to those rules. In order to contemplate possible ways by means of which this limitation can be overcome, the mechanisms which cause it must be examined.

In general, it is the phenomenon of breakdown which determines the maximum operating voltage, and there are several methods by which this can occur. One such instance is junction breakdown, where the reverse biased pn diffusion diodes inherent in the process exhibit either avalanche or zener breakdown mechanisms, as described by Bar-lev (1). Under these conditions, the diodes begin to conduct in the reverse direction and clearly this will prevent the circuit from operating as designed. In practice, however, this does not

occur until junction voltages in excess of 80V are applied and hence it is not a limiting factor on the VF driver circuit envisaged.

Another breakdown method is punchthrough, of which there are two types. The first, known as vertical punchthrough, occurs only in CMOS transistors which are situated in their own diffusion wells. For the metal gate CMOS process considered in this paper, the substrate is n-type material, and so it is the n-channel transistors which are formed within p−wells. At high voltages (18V), where the potential between the drain (n+material) and the well (p−) is large, the depletion region associated with the drain diffusion can extend until it reaches the substrate (n−), at which point a current path is formed. In this way, vertical punchthrough can occur as shown in *Figure 3*.

The second punchthrough mechanism is horizontal punchthrough, and this normally occurs between drain and source of both n- and p-channel devices. As stated by Hamilton and Howard (2), the threshold voltage of the basic MOS transistor is the voltage required to cause field inversion in bulk material and hence form a drain source channel, the conductive properties of which are controlled by the gate voltage. As before, at high drain voltages (30–35V), a depletion region extends out from the drain diffusion. If the drain (p+ or n+) to bulk (n− or p−) potential is high enough the drain depletion region will reach the source diffusion (p+ or n+) and an uncontrolled drain source channel is formed, causing the transistor to act as a short circuit. Consequently, horizontal drain source punchthrough, as shown in *Figure 4*, is a phenomenon which must be pondered carefully in connection with high voltage applications.

The final breakdown mechanism is known as surface avalanche breakdown, and this occurs due to an accumulation of charge at the bulk material surface. If the drain voltage is again large with respect to both the gate and the source (30–35V), then the equipotential lines shown in *Figure 5* will lead to an area of high electric field at the surface of the drain to bulk junction. Under the above conditions, and because the depletion region is relatively narrow at this point, surface avalanche breakdown can occur as described by Grove (3).

It is true to say, therefore, that there are several breakdown mechanisms which contribute to the aforementioned operating voltage limit. Referring to the on chip structure outlined in *Figure 2*, it is clear that only high voltage p-channel transistors are required, and so vertical punchthrough need not be considered in this case. In addition, junction breakdown will only occur at voltages above those envisaged in this application, and hence horizontal punchthrough and surface avalanche breakdown are the phenomena which must be overcome to facilitate a successful design.

ON CHIP RESISTORS

Due to the nature of CMOS, i.e. because the technology produces both pull-up and pull-down transistors, it is relatively rare to find resistors in such circuits. A further reason for the rare appearance of resistors is that the tolerances on MOS diffusion resistors are so large as to make them unac-

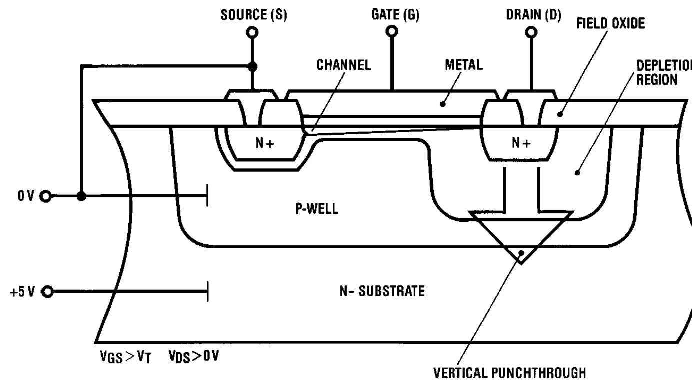

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FIGURE 3. Vertical Punchthrough in a CMOS N-Channel Transistor

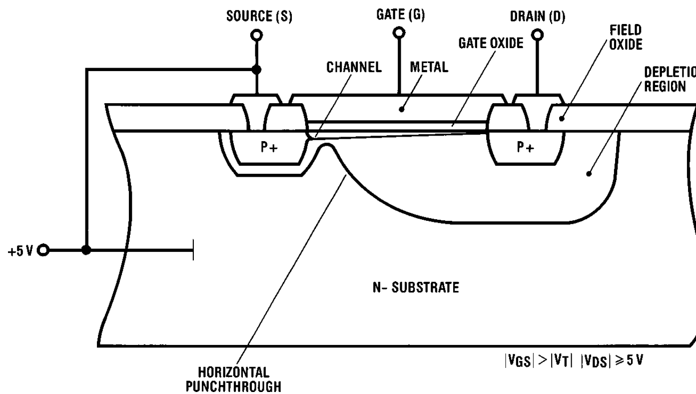

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FIGURE 4. Horizontal Punchthrough in a CMOS P-Channel Transistor

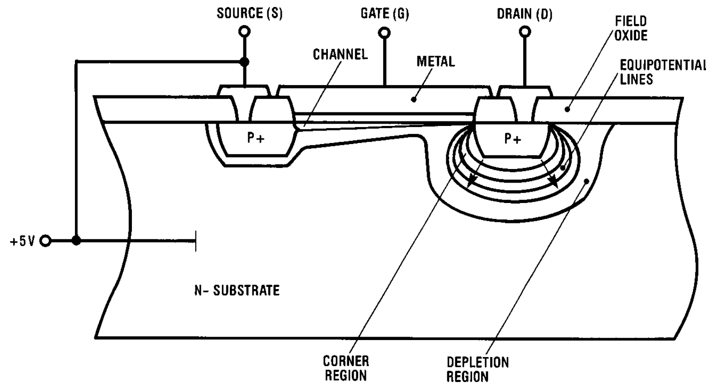

FIGURE 5. Surface Avalanche Breakdown in a CMOS P-Channel Transistor

ceptable in normal applications. One occasion where such resistors are used is where it is only the ratio between the resistors which is important, and not their precise values, for instance in a voltage divider. Under these circumstances, any change in the nominal resistance value will be reflected in all the resistors and hence the divider will operate as designed.

As was pointed out above, such resistors are normally formed by making use of the sheet resistance of diffusion. In particular, the diffusion with the highest value of sheet resistance is used, and this is p-material. Hence, the structure shown in *Figure 6*, known as a pinched p− resistor, is common, and it is clear that this device is in fact a p-channel junction field effect transistor (JFET). The theory of JFET operation is described by Glaser and Subak-Sharpe (4), and because the p− diffusion process is followed by n+ diffusion it can be seen that the JFET gate completely surrounds the p-type channel region in the form of n+ and n− (substrate) material, which is tied to 5 volts. For this reason, the pinch-off voltage is very low (typically 10V) and so these pinched resistors are widely used in low voltage applications. Further, p− diffusion sheet resistance is a parameter which has a wide process spread, i.e. 4.5–7.0 kΩ per square, and although the pinched resistor technique increases this nominal resistance value due to depletion effects, such resistors are difficult to specify in advance.

If the large changes in resistance value are not tolerable then p+ diffusion resistors in the n− substrate are a viable alternative, for two reasons. First, because of the doping profile of p+ diffusion, the JFET depletion effects are reduced, and consequently such resistors have a much higher pinch-off voltage. Second, the nominal resistance of p+ diffusion is much more stable over the process range, although its value is far lower (40–80Ω per square). For this latter reason, p+ resistors occupy large areas for relatively small values.

High Voltage CMOS

Referring to the 'Ideal' VF Driver section, one of the principal aims of this design is that a standard fabrication process be used. Bearing that in mind then, there follows a study of possible ways by which the original VF display driver specification could be realised or even enhanced.

HIGH VOLTAGE TRANSISTORS

The simpler of the two operating voltage limitation factors to overcome is horizontal punchthrough. From *Figure 5*, it is clear that in order to increase the drain source voltage at which the depletion regions combine the distance between the drain and source must be increased. This has the effect of lengthening the transistor channel, and the consequences of such action should be considered. The basic equations which describe the mode of operation of the MOS transistor are derived by A.M.I. (5), and from these, increasing the channel length (L) will result in lower drain source current (I_{DS}), lower gain factor (β), and higher threshold voltage (V_T). All of these effects will degrade the transistor performance, although it is worth noting that the aspect ratio (W/L), i.e. the ratio of channel width (W) to its length, is a major component of the transistor equations. Hence, some performance can be salvaged by increasing the channel width to return the aspect ratio to its original value. Unfortunately, this approach increases gate area and hence parasitic capacitances, and so the resulting high voltage transistor is still inferior to its low voltage equivalent.

The other mechanism which leads to high voltage breakdown in MOS transistors is surface avalanche breakdown, and this phenomenon can only be overcome at a cost. As was explained previously in reference 3, this avalanche effect is caused by a region of high electric field which can lead to electrons with energy levels high enough to start a chain reaction of collisions within the silicon lattice. The electric field at the corner (ξcorner) determines whether this phenomenon will occur and reference 3 points out that ξcorner is inversely proportional to gate oxide thickness (t_{ox}). Armed with this information, initial experiments were carried out with long channel devices having t_{ox} values ranging from the standard process value of 1000Å up to a maximum possible value of 2300Å. In practice, the oxidation cycle had to be altered to allow these different oxide thicknesses to be fabricated without affecting other process parameters. As a result of these experiments, it was found that surface avalanche breakdown occurred at approximately 40V with t_{ox} = 2300Å. An alternative experiment involved making use of the oxide which isolates the silicon from the metal inter-connect, that known as field oxide. Field oxide is typically 8800Å thick, and hence it was felt that using this as gate oxide on long channel devices could provide the desired high voltage performance. However, field oxide MOS transistors were found to have breakdown voltages in excess of 70V, and for this reason it was decided that the VF driver outputs would be designed for a maximum voltage swing of 60V. The high breakdown voltage, however, is achieved at a cost in terms of performance. Using the basic MOS transistor equations of reference 5, and noting that increasing t_{ox} will decrease gate capacitance (C_{ox}), it is clear that low values of gain factor ($\beta \cong 1\ \mu A/V^2$), and high

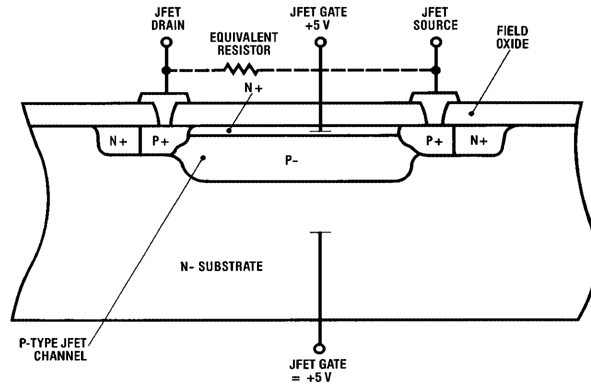

FIGURE 6. P-Pinched Resistor

values of threshold voltage ($V_T \cong -6V$) are expected. If these performance limitations are taken into account at the design stage, then high voltage p-channel MOS transistors are feasible.

The high voltage transistors outlined above are an ideal solution to the display output problem, as their fabrication requires no additional processing stages.

HIGH VOLTAGE PULLDOWN RESISTORS

Before looking at ways in which the high voltage pulldown resistors may be realised, a definitive value for this resistor should be assigned. It is essential that the resistor value is low enough that any leakage current from the p-channel transistor does not cause the output voltage, when the output is in the off state, to be significantly higher than the display voltage. If maximum values of expected leakage current are of the order of 10 μA and if the maximum output off voltage to display voltage difference is 2 volts, then the maximum resistance value is 200 kΩ. In addition it is desirable to minimise the current taken on chip when the output is in the on state. Given that approximately 60V will appear across the resistor under these circumstances and if the maximum desired on current is 600 μA per output, then the minimum resistance value is 100 kΩ. Clearly, there is a trade off in performance between the above two requirements, and if the design is centered about a resistance value of 150 kΩ then any variation due to process spread should not cause this value to drop below 100 kΩ or rise above 200 kΩ.

Having established the value of the resistor to be designed, it only remains to decide the method by which this is to be achieved. Unfortunately, neither of the two methods outlined previously can be applied in this case. P+ diffusion resistors are not practical because the nominal resistance per square of such material is too low, typically 60Ω per square, making such resistors occupy excessive amounts of die area. A p− pinched resistor, on the other hand, will pinch-off at voltages in excess of 10V, and hence such a technique is not applicable.

Given the size of the resistor required, and in order that the die area be minimised, a technique using the p− diffusion should be sought. The problem is to ensure that a resistor of this type does not pinch-off at the voltages anticipated, and hence a method whereby the channel depletion effects may be minimised must be found. The first way in which these effects can be reduced is to increase the width of the p− resistor region. This results in an increase in the voltage required to pinch-off the channel, although in the case of pinched p− resistors an intolerably large increase in area is required to allow high voltage (in excess of 50V) operation. If, however, the n+ diffusion layer shown in *Figure 6* is removed, then the JFET channel is only depleted from three, instead of four sides. Experiments showed that if the p− was simply diffused into the native n-type substrate without an n+ covering, and if the channel was sufficiently wide, then p− resistors with pinch-off voltages in excess of 60V could be fabricated. Secondary tests showed that the p− sheet resistance doubled in this mode from its unbiased value, although this parameter is closely dependent on the drain to substrate potential.

Hence, the objective of high voltage on chip pulldown resistors has been realized with no alterations to the standard fabrication process.

DISPLAY DRIVER IMPLEMENTATION

As discussed previously, the microprocessor interface inputs are TTL compatible and the internal data handling CMOS logic operates from a 5 volt supply. The display data emerges from this logic and enters a bank of level shifters, which convert the 0 $\rightarrow$ 5V waveforms into −10 $\rightarrow$ 5V levels. In this way, a p-channel field oxide transistor can be driven. The output section is in the form of a pre-buffer followed by a display output driver and a schematic of the whole circuit is shown in *Figure 7*.

Examining the schematic in more detail, it is clear that the −10V supply to the level shifting stage (V_{ee}) is derived by means of a p− resistor ladder between V_{SS} (0V) and V_{dis} (−55V). The sizes of both the p-channel field device and the p− resistor in the pre-buffer stage are non-critical, as they merely drive the next stage, except to state that the p-channel is 16 μm long and the p-resistor is 10 μm wide. In fact, it is desirable that the p-resistor has a high resistance value as this minimises the circuit current when the display outputs are in the off state (pre-buffer is on). The output driver stage, on the other hand, demands a more structured approach. Using the design figure of 10 kΩ per square, a p− resistor size of 16 squares was used, i.e. a region of p− diffusion which was 15 μm by 240 μm. The p-channel field transistor was selected to have an output on impedance of 1.5 - 2.0 kΩ, and to achieve this a size of 300 μm by 16 μm was chosen. The low VF display currents result in this high output on impedance being accepted.

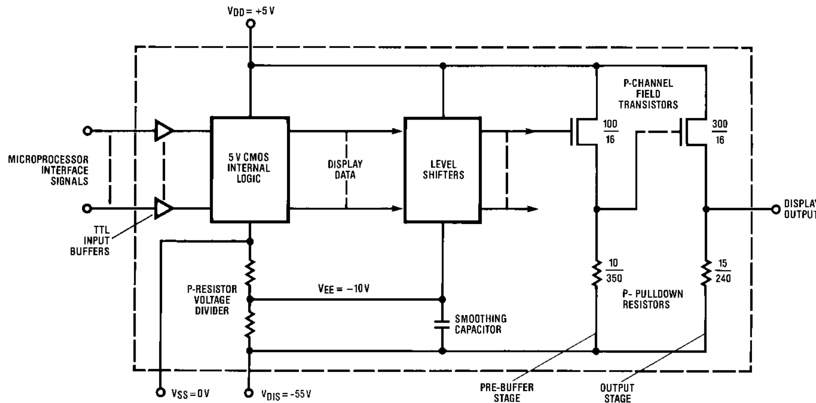

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FIGURE 7. VF Display Driver Circuit Schematic

The Future

Clearly, the future for VF display drivers is highly dependent upon the way in which such displays progress over the next few years. Further experiments with high voltage p-channel transistors suggest that voltages in excess of 100V can be sustained, although this work is at present only at the initial evaluation stage. Hence, if future VF displays demand operating voltages of this order, compatible drivers should be feasible.

At present, there is considerable interest in Front Luminous VF Displays (FLVD), and it is claimed they provide better visual character recognition and a wider viewing angle. This is achieved by reversing the order of the component parts of the VF display shown in *Figure 1*. Hence, the luminous material is directly beneath the front glass, and so the light is unimpeded as it is emitted from the display. Fortunately, however, the driving requirements of FLVD are similar to those of the present VF display, and so the display drivers outlined in this paper appear adequately to meet the needs of the VF displays of today.

Conclusions

The display drivers described in this application note have demonstrated how a fabrication process, thought only to be applicable to low voltage designs, can be extended to produce high voltage circuits. This suggests that the standard processes of today may also be stretched in other directions. If closer attention is given to the mechanisms behind the circuit and process limitations, then it is possible, as in this case, that they can be overcome. Clearly, if this is achieved the rewards of a wider range of products from the same fabrication process will follow.

References

1. Bar-lev, A., 1979, *'Semiconductors And Electronic Devices'*, Prentice-Hall International, Inc., London, pp. 124–131.
2. Hamilton, D.J., Howard, W.G., 1975, *'Basic Integrated Circuit Engineering'*, McGraw-Hill Kogakusha Ltd., Tokyo, pp. 193–198.
3. Grove, A.S., 1967, *'Physics And Technology Of Semiconductor Devices'*, John Wiley And Sons, Inc., New York, pp. 311–315.
4. Glaser, A.B., Subak-Sharpe, G.E., 1977, *'Integrated Circuit Engineering'*, Addison-Wesley Publishing Co., Reading, Mass., pp. 71–80.
5. American Micro-Systems, Inc., 1972, *'MOS Integrated Circuits'*, Van Nostrand Reinhold Co., New York, pp. 60–72.
6. "This article was first published on pp. 113–120 of the proceedings of the *IEE Fourth International Conference On Automotive Electronics*, November 1983."

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