Reliability Of Small Outline (S.O.) Surface Mount Packages

National Semiconductor
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ABSTRACT

New space efficient packages for integrated circuits have been developed. These include the Plastic Chip Carrier (P.C.C.) and Small Outline (S.O.) packages. Design considerations and reliability tests for the S.O. package were compared to the standard plastic Dual-in-Line Package (DIP). The S.O. package was found to be equal to the DIP in reliability tests performed.

INTRODUCTION

There has always been two basic trends in electronics: Make assemblies smaller and less costly. The new surface mount packages were developed to meet these on-going challenges. Two types—the Plastic Chip Carrier (P.C.C.) and the Small Outline (S.O.) have emerged to become the dominant styles of surface mount plastic packages in use today. Of these two, the smaller S.O. package has been the subject of controversy in the area of reliability.

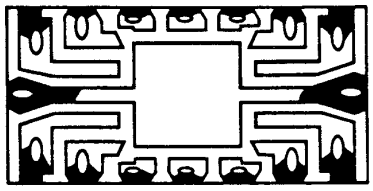
RELIABILITY BY DESIGN

As with any new product, how good one designs the package ultimately determines how good the reliability will be. Because the S.O. package is small, it affords less plastic protection for the die when compared to the traditional dual-in-line (DIP) package. This could lead to earlier failures in environmental testing compared to the dual-in-line, specifically if both are made out of the same materials. Test data has verified this possibility. To reduce this chance of failure, a re-design of the S.O. package was necessary. Among the items evaluated were: Leadframe design, leadframe plating, leadframe composition, semiconductor molding compound, and die passivation.

LEADFRAME DESIGN

The design of the leadframe must be optimum to allow for minimum moisture penetration but maximum electrical and thermal properties. One design possibility to reduce moisture penetration is to place holes in the internal lead tips. These locking holes provide a barrier to moisture traveling up the leads between the leadframe-molding compound interface. *Figure 1* shows results of a dye moisture pene-

National SO-14



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Competitor SO-14

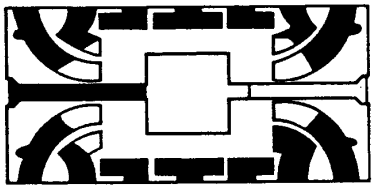

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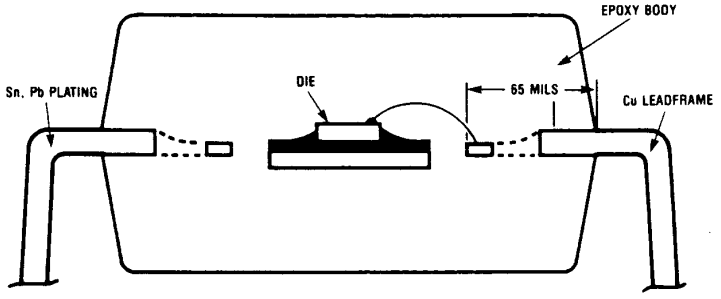
FIGURE 1. Dye Penetration Test

DIP-14



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SO-14

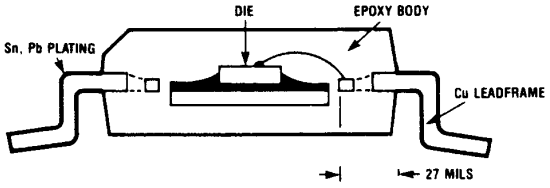

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FIGURE 2

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tration test between frames with and without locking holes. The results of this bias moisture test clearly show the advantage of leadframes with ''holes.''

Leadframe plating is also crucial to package design, as it serves as a metallurgical interface between the bare leadframe and the functional chip. As *Figure 2* illustrates, the distance from the edge of the package to the die is approximately two and a half times greater in the dual-in-line package than in the small outline package. This would lead us to conclude that moisture traveling along a leadframe/plastic interface would reach the die earlier in a small outline package.

To reduce moisture penetration along this interface, the path length (edge-to-die) must be similar to the DIP. To increase this distance, various plating techniques were evaluated, with the idea being to increase the surface area path length at which the moisture must travel. A unique plating process was developed which, by its rough surface characteristics, effectively makes the S.O. plated surface area comparable to a typical plated DIP. This plating is compared in *Figure 3*, where (A) is the new plating process that yields increased surface area, and (B) is the traditional plating.

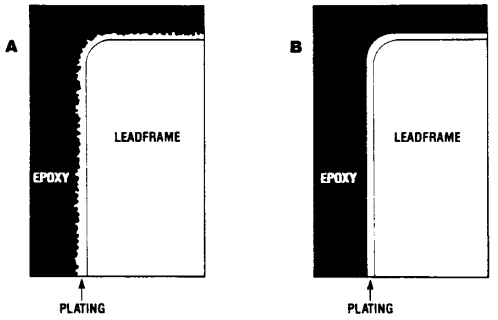

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FIGURE 3. Plating Process

Leadframe composition is an area where change has resulted in improved performance. Traditionally Alloy 42, a nickel-steel composition, has been used as a leadframe material in the dual-in-line by many manufacturers for years. However, in designing a smaller package such as the S.O., thermal properties now become a more critical factor. A high strength, modified copper alloy composition was developed which lowers the thermal resistance of the S.O. package over that produced with Alloy 42 material. In fact, *Figure 4* shows that the θJA (Junction-to-Ambient temperature of thermal resistance) of a 14 lead S.O. package using copper as a leadframe material is less than a conventional Alloy 42 fourteen (14) lead dual-in-line package.

Copper also has expansion properties which improve thermal cycle characteristics. *Figure 5* compares the linear coefficient of thermal expansion (designated as α) of Alloy 42, copper, and a semiconductor molding compound. Notice that the copper more closely matches the molding compound expansion rate. Less of a thermal mismatch is created at the copper-epoxy interface compared to that of the Alloy 42-epoxy.

Thermal Resistance S.O. vs DIP

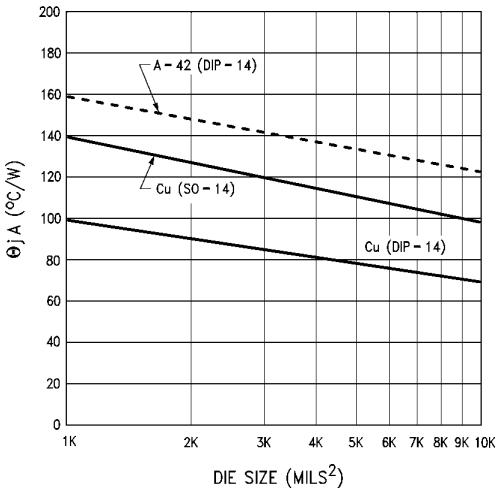

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FIGURE 4. Thermal Resistance

Thermal Expansion and Glass Transition Temperature:

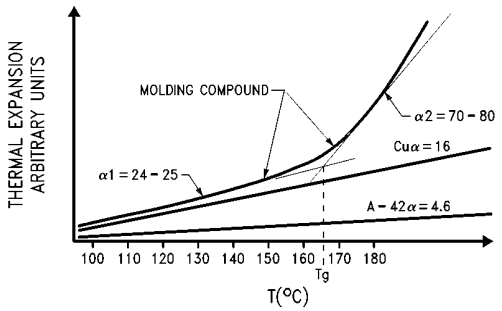

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FIGURE 5

MATERIAL CONSIDERATIONS

Semiconductor molding compounds have also helped to improve the reliability of the Small Outline package. Reduced contaminants, specifically sodium and chloride ions have resulted in less corrosive species available to cause failures in bias-temperature-humidity tests. In addition, lower internal stress producing encapsulants reduce failures due to package warping and cracking during the assembly process. Properties of these new proprietary high purity, low stress compounds are listed in Table I.

TABLE I. ''High Purity'' Semiconductor Molding Compound Chemical Properties

Na ion	$<$ 5 ppm
Cl ion	$<$ 10 ppm
pH	4.1
Extracted Conductivity	40 $\mu\Omega$/cm
Hydrolizable Chloride	45 ppm

Die passivation has always been critical in ensuring reliability. Most manufacturers use a silicon-nitride passivation to help protect the die. Some use a polyimide to enhance moisture protection. Most effective, especially on small packages, is a ''multi-layer passivation system.'' In this system, a 10,000 A thick layer of silicon oxide is formed during wafer fabrication. This is followed by a second nitride passivation layer. These two overlapped passivation techniques essentially eliminate defects, since it is unlikely that both masks will have imperfections in exactly the same spot.

RELIABILITY TEST RESULTS

Upon completion of these design improvements as described for the S.O. package, reliability tests were performed on various linear devices in the Small Outline and molded dual-in-line package configuration. Package variety included 8, 14, and 20 leads. The test categories and conditions evaluated are listed in Table II. Tables III and IV indicate that a reliability performance in products assembled in National Semiconductor Small Outline package is excellent and compares favorably to the reliability performance of products assembled in the standard dual-in-line package.

Additional detailed reliability information can be found in a report entitled ''Reliability Report: The S.O. Package'' (Lit. # 980045).

TABLE II. Test Descriptions

High Temperature Bias	— Continuous operation at rated supply voltage, $T_A = 150°C$
Temperature Humidity Bias	— Continuous operation at rated supply voltage, 85°C and 85% RH.
Autoclave	— Unbiased at 100% humidity, 15 psi and 121°C.
Storage Life	— Storage at $T_A = 150°C$ without bias.
Temperature Cycle	— $T_A = -65°C$ to $+150°C$, 20 minutes per cycle.
Thermal Shock	— $-65°C$ to $+150°C$ liquid, 5 minutes immersion, 5 seconds transfer time.

CONCLUSIONS

The Small Outline package has been shown to be reliable. Criteria to ensure reliability include enhancement and controls on (but not limited to):

- Leadframe Design
- Leadframe Plating Composition
- Leadframe Plating Texture
- Leadframe Materials
- Epoxy Molding Compound
- Die Passivation

TABLE III. Autoclave

Humidity-Temperature Storage 121°C 15 pal

Package	Time Points		
	168 Hrs.	500 Hrs.	1000 Hrs.
DIP	0/757	0/757	0/392
SO	0/1357	0/1357	0/739

Storage Life, $T_A = 150°C$

Package	Time Points		
	168 Hrs.	500 Hrs.	1000 Hrs.
DIP	0/20	0/20	0/20
SO	0/233	0/233	0/233

Thermal Shock Liquid-to-Liquid $-65°C$ to $+150°C$

Package	Time Points				
	15	30	50	100	200 Cycles
DIP	2/225	0/224	0/224	0/224	0/175
SO	0/525	0/524	0/524	0/524	0/175

TABLE IV

Accelerated Bias Moisture Test(A)

Package	85% RH/85°C Equivalent Hours Time Points			
	2000 Hrs.	4000 Hrs.	6000 Hrs.	8000 Hrs.
DIP	2/334	2/285	1/128	—
SO	1/1046	1/414	2/250	1/64

High Temperature Bias Test(A)

Package	Time Points		
	168 Hrs.	336 Hrs.	500 Hrs.
DIP	0/545	1/545	0/544
SO	1/761	0/760	0/760

Temperature Cycle $-65°C$ to $+150°C$(A)

Package	Time Points	
	1000 Cycles	2000 Cycles
DIP	0/213	0/213
SO	0/360	0/360

(A) All (S.O. Package) parts mounted on printed circuit boards using vapor phase soldering.

(B) All results expressed in # failures/units tested.

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