A 40 MHz Programmable Video Op Amp

National Semiconductor
Application Note 480
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Conventional high speed operational amplifiers, with bandwidths in excess of 40 MHz, introduce problems that are not usually encountered in slower amplifiers such as LF356, LM308, LM741, etc. Many designers experience difficulties realizing the enhanced performance. Proven design techniques for medium performance device do not translate well to high frequency operation. High speed amplifiers are sensitive to PC board layout, requiring careful placement of decoupling capacitors, a ground plane, and very short signal paths to minimize stray capacitances. Few high speed operational amplifiers can provide the output current required to drive the capacitive cables which often interface the circuit with the outside world. These applications usually demand a two chip solution which includes a line buffer placed inside an operational amplifier's feedback loop. This type of compound circuit is typically very difficult to compensate and very sensitive to layout topolgy.

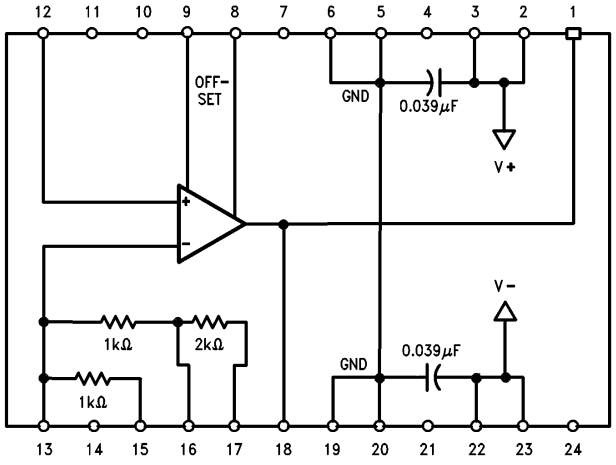
The LH4101 was designed to address these issues, making it simple to construct stable circuits without compromising performance. Its unique implementation results in a device that is not susceptible to common circuit sensitivities. The LH4101 is a wideband FET input operational amplifier exhibiting 250 V/μS slew rate and 100 mA output current capability. The high output current enables the operational amplifier to drive 50Ω loads or terminated lines directly, eliminating the need for a current booster or buffer.

The LH4101 is internally compensated for unity gain stability, and gain set resistors are provided inside the package. This amplifier can be configured to gains of $+1$, $+2$, $+3$, $+4$, -1, -2, and -3 without any external components.

Figure 1 shows a block diagram of the device and its pin identifications. Table I summarizes the typical performance data of the LH4101. Additional information and guaranteed min/max limits can be obtained from the datasheet.

TABLE I. Typical Performance Characteristics at 25°C Ambient, $\pm$15V Supply

Parameter	Condition	Value
Output Current		100 mA
Input Offset Voltage		15 mV
Input Bias Current		500 pA
Input Offset Current		200 pA
Input Resistance		$10^{12}\Omega$
Open Loop Voltage Gain	$R_L = 50\Omega$	60 dB
Output Voltage Swing	$R_L = 1\ K\Omega$ $R_L = 100\Omega$ $R_L = 50\Omega$	$\pm$13.5V $\pm$10.0V $\pm$5.0V
Slew Rate	$A_V = +1$	250 V/μs
Small Signal Rise Time	$A_V = +1$ $R_L = 50\Omega$	15 ns
Small Signal Settling Time to 0.1%	$V_{IN} = 5V$ $A_V = +1$	300 ns
Small Signal Bandwidth	$A_V = +1$ $R_L = 50\Omega$	45 MHz



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Dual-In-Line Package

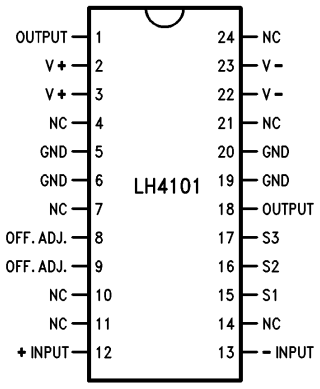

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FIGURE 1. Block Diagram and Connection Diagram of LH4101

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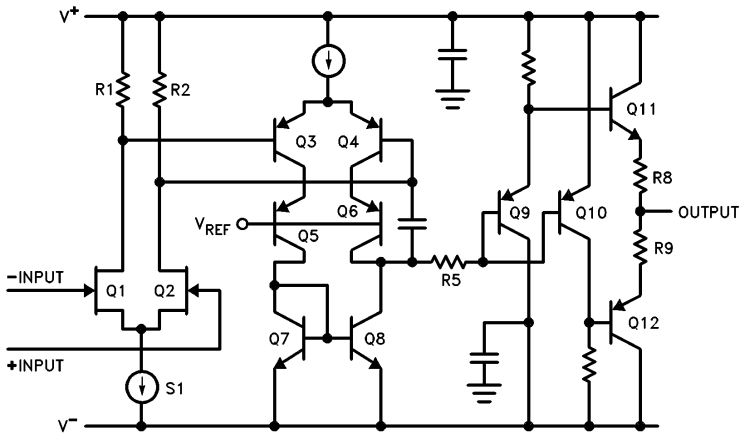

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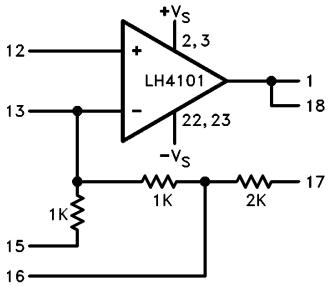
FIGURE 2. Simplified Schematic of LH4101

CIRCUIT TOPOLOGY

Figure 2 shows a simplified schematic of the amplifier. For clarity, the gain set resistors are not shown. The LH4101 is implemented using a classical op amp topology with a differential front end, followed by a differential gain stage and a Class AB output stage. The differential front end uses a pair of monolithic dual JFET to provide matched DC tracking and good common mode input characteristics. First stage operating current is set at 6 mA by the current source S1, and the first stage voltage gain is approximately 1.4. The second stage consists of two identical pairs of differential PNP transistors in a cascode configuration. Each side is biased to draw approximately 5 mA. The differential amplifier Q3 and Q4 feeds the common base pair Q5 and Q6 with the base voltage fixed at V_{REF}. Therefore, the collectors of differential pairs Q3 and Q4 are held at one V_{BE} more positive than the reference voltage. Any signal amplified by the differential stage produces only a very small change in Q3 and Q4 collector voltages. Consequently, the Miller effect on Q3 and Q4 (base to collector capacitance) is virtually eliminated. The voltage gain of the cascode second stage is approximately 1400. Note that the full differential gain is realized with the use of the current mirror Q7 and Q8, which also provides active load resistance to the PNP cascode pair, resulting in high amplifier gain. The output stage is a push pull pair biased by two emitter followers. This establishes a class AB bias in the output stage so that there is no class B type crossover distortion in the output. Resistors R8 and R9 limit the potential for thermal runaway of the output stage.

Gain Configurations

The LH4101 can be configured with gains of $+1$, $+2$, $+3$, $+4$, -1, -2, and -3 by using the internal gain set resistors. *Figure 3* illustrates how the LH4101 can be used in non-inverting configurations. *Figure 4* shows the connection diagram for inverting configurations. In this mode, pin 15 is V_{IN} and pin 12 should be tied to ground. The internal gain set resistors are trimmed and matched to insure gain error to less than 1%. The LH4101 can operate at other gain settings, but the user must supply external gain set resistors.



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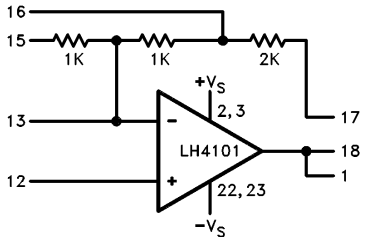
For non-inverting configuration, pin 12 is V_{IN}.

Pins 5, 6, 19, 20 are ground pins and are all internally connected.

Closed Loop Gain A_V	Connections
$+1$	Connect Pins 15, 16, 18.
$+2$	Connect Pin 15 to Pin 19, Pin 16 to Pin 18.
$+3$	Connect Pin 15 to Pin 19, Pin 16 to Pin 13, Pin 17 to Pin 18.
$+4$	Connect Pin 15 to Pin 19, Pin 17 to Pin 18.

FIGURE 3. Non Inverting Configurations



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For inverting gains, input is pin 15. Pin 12 should be connected to ground.

Pins 5, 6, 19, 20 are ground pins and are all internally connected.

Closed Loop Gain A_V	Connections
−1	Connect Pin 16 to 18.
−2	Connect Pin 16 to 13. Pin 17 to 18.
−3	Connect Pin 17 to 18.

FIGURE 4. Inverting Configurations

POWER SUPPLY BYPASSING

The LH4101 will perform well in most circuit boards even without external supply bypassing; however, it is recommended that some bulk bypassing be provided. A 1 μF capacitor on each supply is recommended. Proximity to the device pins is not critical, but the bypass will be most effective if located within an inch of the device.

A PRECISION BUFFER

Most high speed buffers which are used to drive 50Ω and 75Ω coaxial cables attain high speed and quick settling at the sacrifice of gain accuracy. Old standards such as the LH0033 have gain accuracy as low as 0.92 when driving 50Ω loads. In many precision applications such as flash A/D buffering, DAC output amplifiers, and high resolution video display drivers, low gain accuracy is unacceptable. The LH4101 fills this niche as a voltage follower with 0.99 gain accuracy into 50Ω, while maintaining a 140 nS settling time to 1%. *Figure 5a* shows the circuit connection for the precision buffer. *Figure 5b* shows a video distribution amplifier for a double terminated system.

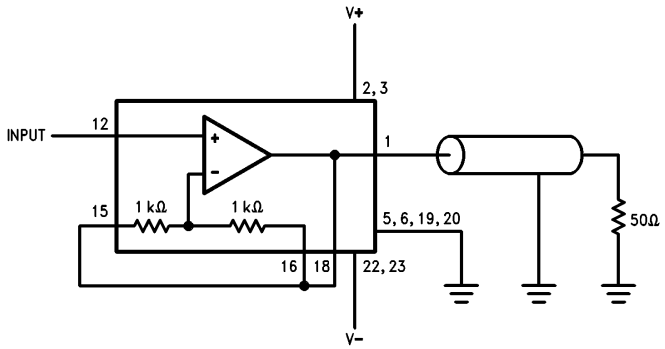

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FIGURE 5A. A Precision Non-Inverting Buffer

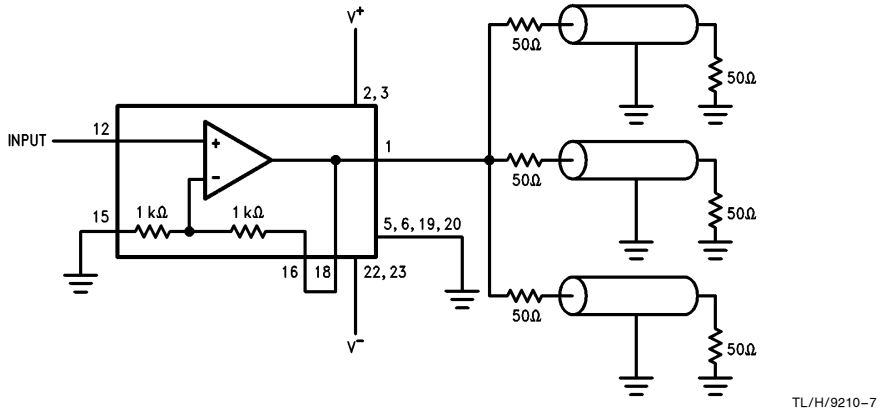

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FIGURE 5B. Video Distribution Amplifier

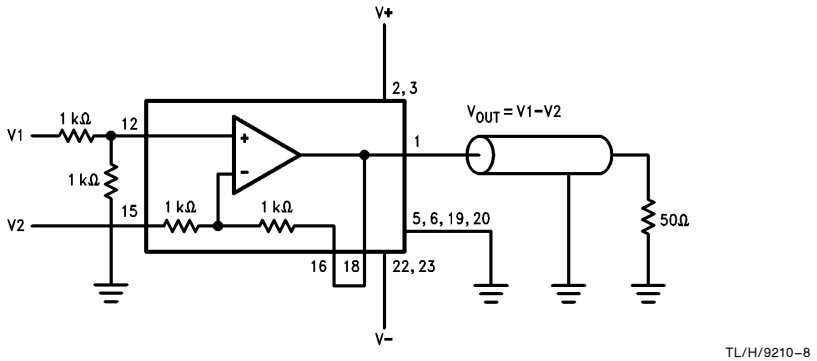

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FIGURE 6. Differential Amplifier

DIFFERENTIAL AMPLIFIER

The LH4101 can also be used as a high frequency differential amplifier. Two external 1 KΩ resistors are required. *Figure 6* shows the circuit configuration where $V_0 = V_1 - V_2$. The gain accuracy is dependent upon the relative matching of the additional 1 KΩ resistors with the internal 1 KΩ resistors.

SUMMING AMPLIFIER

Figure 7 shows the LH4101 being used as a summing amplifier where $V_0 = -(V_1 + V_2)$. One point that is often overlooked in such a configuration is the effect multiple inputs have on the usable bandwidth of the amplifier. LH4101 as an inverter (single input) exhibits a small signal bandwidth of 28 MHz, but a summing (two inputs) amplifier exhibits only 14 MHz; the resultant bandwidth is halved. One easy way to explain this is to consider the Thevenin equivalent looking back into the source resistances from the virtual ground terminal. Thevenin's R in this case is R1 in parallel with R2 = 1 KΩ//1 KΩ = 500Ω. The effective gain of the amplifier is actually −2 and not −1.

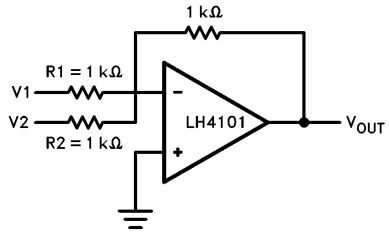

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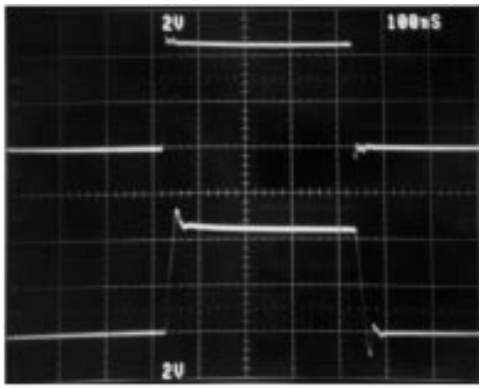
FIGURE 7. Summing Amplifier

Demonstrating Transient Performance

The photographs in *Figure 8* show the pulse response of the LH4101 under various values of gain and input conditions. *Figure 9* shows the closed loop bandwidth of the LH4101 at different gain settings and *Figure 10* shows the open loop bode plot of the device.



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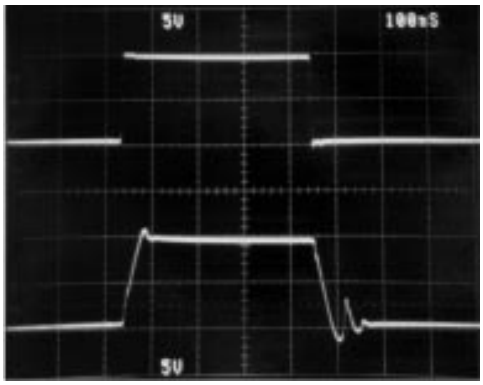
$V_{CC} = \pm 15V$ $A_V = +1$
$R_L = 50\Omega$ $V_{OUT} = \pm 2V$



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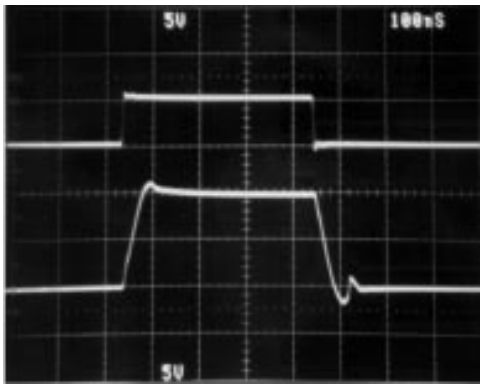
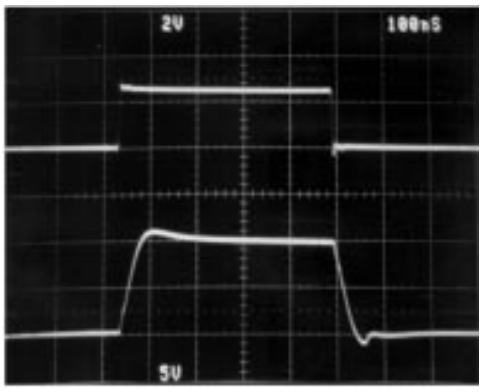
$V_{CC} = \pm 15V$ $A_V = +1$
$R_L = 50\Omega$ $V_{OUT} = \pm 5V$

FIGURE 8



V_{CC} = ±15V A_V = +2 TL/H/9210–12
R_L = 50Ω V_{OUT} = ±5V



V_{CC} = ±15V A_V = +4 TL/H/9210–13
R_L = 50Ω V_{OUT} = ±5V

FIGURE 8 (Continued)

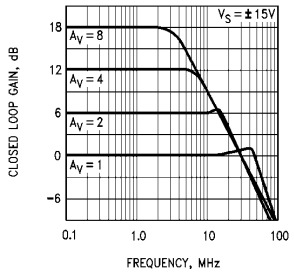


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FIGURE 9. Closed Loop Frequency Response, V_S = ±15V Bode Plot (Open Loop)

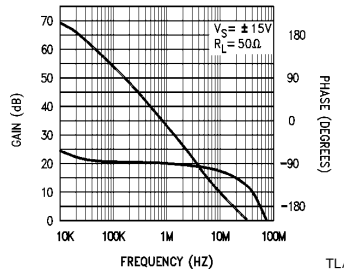

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FIGURE 10. Bode Plot of LH4101, V_S = ±15V

Driving Capacitance

Capacitive loads cause increased phase shift such that the phase margin decreases toward an unstable state and oscillation may result. *Figure 11a* shows the square wave response of the LH4101 driving a 220 pF capacitive load. This value is similar to the input capacitance of most high speed flash A/D. The circuit used is given in *Figure 12*. The series R1 = 8Ω limits the current through the output stage and also limits the added phase shift seen by the feedback loop, thus maintaining stability. To reduce the ringing and improve the settling time, changing R1 to 50Ω as seen in *Figure 11b* will substantially improve settling time by further reducing the phase delay introduced into the feedback loop.

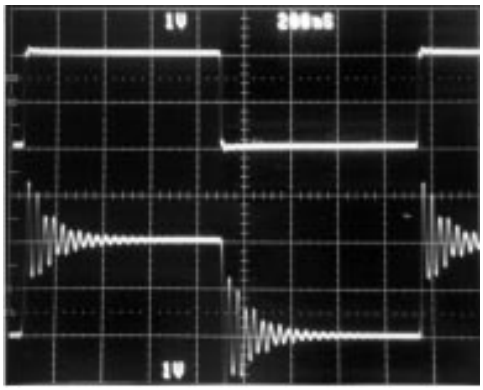

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FIGURE 11A. Pulse Response of LH4101 Driving a 220 pF Load with R1 = 8Ω

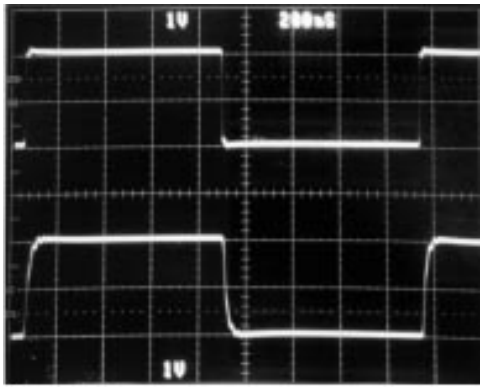

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FIGURE 11B. With R1 = 50Ω

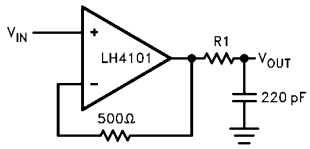

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FIGURE 12. Compensation for Capacitive Load

LH4101 Operation at $V_S = \pm 5V$

Although the LH4101 is designed for normal operation with $V_S = \pm 15V$, it can operate at similar performance levels with $\pm 5V$ supply voltage. *Figure 13* shows the closed loop frequency response at various gain settings.

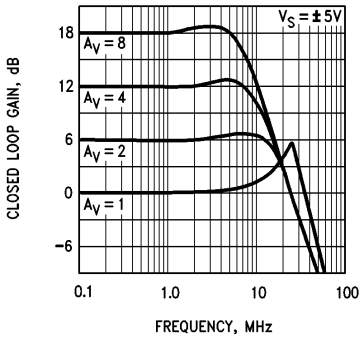

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FIGURE 13. Closed Loop Frequency Response, $V_S = \pm 5V$

DIFFERENTIAL GAIN AND DIFFERENTIAL PHASE

The LH4101 exhibits very low differential gain and differential phase and is suitable for use as precision buffers. Differential gain and phase at 3.58 MHz is less than 0.1% and 0.1 degrees. Differential gain and phase at 20 MHz with delta V_{IN} of 4 volts is 0.3% and 0.4 degrees.

MIL TEMP OPERATION

The quiescent power with V_S of $\pm 15V$ is 1.2W, whereas the package is only rated to 750 mW (without a heatsink) at 125°C. (See *Figure 14* for power dissipation graph). Therefore, to keep the junction temperature from exceeding 150°C, some form of heatsinking or forced air cooling is required when the LH4101 is operated at elevated temperature. Alternatively, the quiescent power dissipation can be reduced by using lower supply voltages to such as $\pm 10V$ or $\pm 5V$.

Maximum Power Dissipation

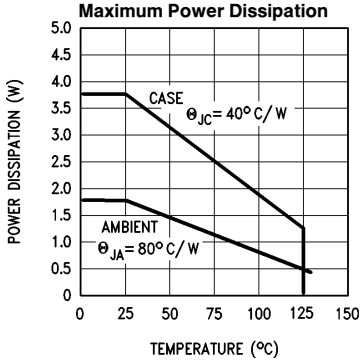

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FIGURE 14. Power Dissipation

Adjustment of Offset Voltage

The offset voltage can be reduced or nulled as shown in *Figure 15.* The 100Ω series resistor prevents any adverse oscillation or malfunction when the potentiometer is shorted to either end of the adjustment range. This type of adjustment is adequate for most applications. In applications where extremely low DC offset is required, an auto zero chip (LMC 669) can be added to correct for DC errors. *Figure 16* shows the circuit implementation of such a scheme. The LMC669 measures the D.C. voltage at the inverting input of the LH4101 and compares this value to a reference ground (INREF). The non-inverting input of the LH4101 is driven by the output of the LMC669 (through an attenuating and low pass filtering network), rather than being connected directly to ground as in a standard inverting op amp circuit. The LMC669 adjusts its output voltage until it senses that the inverting input node of the LH4101 is sufficiently close to ground. Thus the op amp's intrinsic input offset voltage has little effect on the circuit's operation. The resulting offset is determined by the offset voltage of the LMC669's internal comparator. The 2000 pF capacitor integrates the output of the LMC669. Two 0.1 μF capacitors are used to form low pass filters to block the pickup of high frequency noise at the op amp inputs.

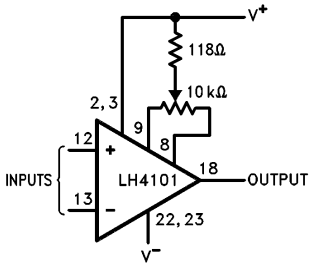

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FIGURE 15. Simple Offset Adjust

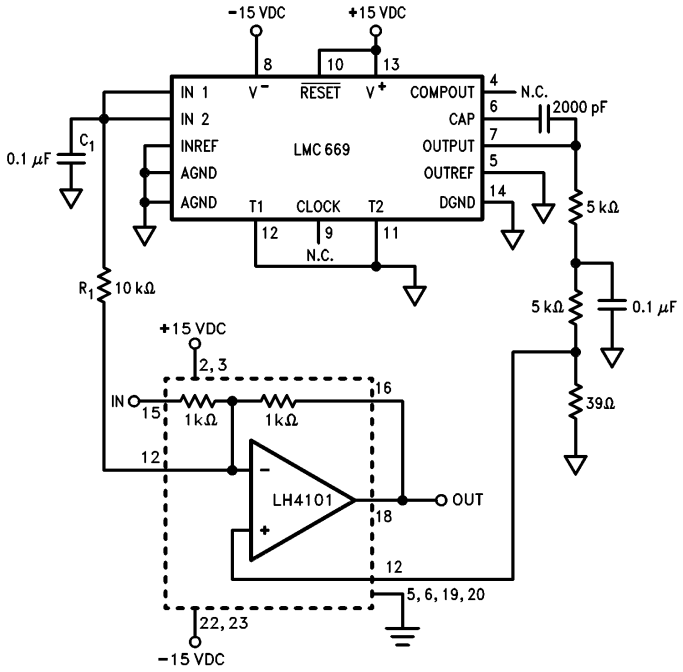

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FIGURE 16. Chopper Stabilization Dramatically Reduces the Input Offset Voltage Over a Wide Temperature Range without Trimming

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