Flexible Timers on the DP8570A and DP8571A

National Semiconductor
Application Note 595
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December 1988

1.0 INTRODUCTION

The DP8570A/71A/72A/73A family are Real Time Clock devices for use in microprocessor based systems. They are fast access low power devices with power fail protection, standby battery operation, multiple interrupts and RAM. In addition, the DP8570A and DP8571A "Timer Clock Peripherals" have two independent 16-bit binary countdown timers.

This application note deals primarily with using the timers on the DP8570A. It has dedicated timer pins; an external clock pin with up to 10 MHz operation, a hardware gate/hold pin per timer and a timer output pin. Further information is given on the DP8571A which does not have these pins, hence reducing the pin-count, but has the additional feature of being able to cascade the timers. This gives use of a timer of up to 32 bits.

The timers of both Timer Clock Peripherals have four modes of operation, seven crystal derived internal clock frequencies, programmable output/interrupts and standby operation.

2.0 DP8570A TIMERS *(Figure 1)*

Each timer, T0 and T1, has two 8-bit registers (MSB/LSB) accessed in page 0 of the DP8570A internal memory. The number in these registers is loaded into a 16-bit counter when the timer is started and the counter is decremented by the selected input clock, hence controlling the timer output. Resetting the timer start/$\overline{\text{stop}}$ bit stops the timer and puts its output into its inactive state (high or low depending on how the output is programmed). Every time the start/$\overline{\text{stop}}$ bit is set the initial value in the MSB/LSB registers is reloaded by the next selected timer input clock. A gate signal, however, is also required in mode3 before loading occurs.

Normally when accessing the data at the address of the MSB/LSB registers, only the initial load value will be read. However, if the timer read bit is set, the MSB/LSB of the counter itself will be read. This allows the user to read the counters *on-the-fly*, without disturbing timing.

The user might encounter a problem when the timer read bit is set just as the counter is reloading. In this case there is a possibility of erroneously reading a value FFhex. The user should choose initial register values other than FFhex, reject any FFhex read on-the-fly and try the read operation again.

The T0 and T1 timer start/$\overline{\text{stop}}$ bit and timer read bit are in their respective timer control registers. Each timer control register contains the following bits:

D0 Timer Start/Stop
D1 Mode Select M0
D2 Mode Select M1
D3 Input Clock Select C0
D4 Input Clock Select C1
D5 Input Clock Select C2
D6 Timer Read
D7 Count Hold/Gate

The programming of this and other timer related registers is described in Section 3.0.

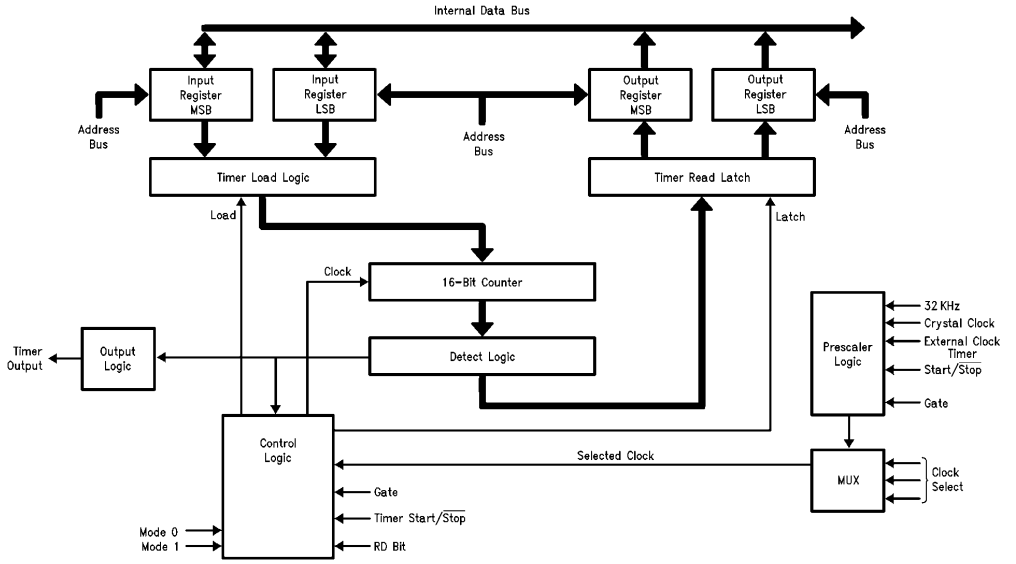

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FIGURE 1. DP8570A Timer

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3.0 USING DP8570A TIMERS

The following steps should be considered when using the DP8570A timers.

a) Mode selection to give desired output waveform.

b) Input and frequency selections to give countdown rate of timer.

c) Output and interrupt selections.

d) Standby conditions (if backed up).

3.1 Mode Selection

Four output waveforms are obtainable from the DP8570A, selected by two bits in the timer control registers (Table I).

TABLE I. Timer Control Registers Mode Bits D2, D1

M1	M0	Mode
0	0	0
0	1	1
1	0	2
1	1	3

3.1.1 MODE 0: Single Pulse Generator *(Figure 2)*

In this mode, a timer output will become active and its counter will decrement once its start/$\overline{\text{stop}}$ bit is set. As soon as the count reaches zero, the start/$\overline{\text{stop}}$ bit is automatically reset and the output returns to its inactive state. Hence the active time (pulse width) is

Timer Clock Period $\times$ Number in Counter.

The pulse width can be increased by temporarily stopping the clock in two ways. One is to set the timer count hold/gate bit and the other is to put the respective G Input pin to a logic one state. The count-down is resumed once the count hold/gate bit is reset or G input is returned to logic zero.

3.1.2 MODE 1: Rate Generator *(Figure 3)*

In this mode, a timer output will become active and its counter will decrement once its start/$\overline{\text{stop}}$ bit is set. When the count reaches zero, the output goes inactive for one timer clock period. The counter is reloaded with the number in the registers. On the next clock the output goes active again and the sequence continues until the start/$\overline{\text{stop}}$ bit is reset. The period is

Timer Clock Period $\times$ (Number In Counter + 1)

and the (inactive) pulse width is the timer clock period. As in mode 0, the count-down can be suspended by setting the count hold/gate bit or using the G input pin.

3.1.3 MODE 2: Square Wave generator *(Figure 4)*

In this mode, a timer output will become active and its counter will decrement once its start/$\overline{\text{stop}}$ bit is set. On the clock after the count reaches zero, the output goes inactive. The counter is reloaded with the number in the registers and the counter will decrement to zero again before returning to the active state. The sequence continues until the start/$\overline{\text{stop}}$ bit is reset. The period is

2 $\times$ Timer Clock Period $\times$ (Number In Counter + 1)

with a 50% duty cycle. As in mode 0, the count-down can be suspended by setting the count hold/gate bit or using the G input pin.

3.1.4 MODE 3: Retriggerable One Shot *(Figure 5)*

In mode 3, a timer output will not become active as soon as its start/$\overline{\text{stop}}$ bit is set. A trigger is also required to start a pulse. The trigger is either setting the count hold/gate bit or the rising edge of a pulse on the respective G input pin. (A trigger pulse as short as 25 ns can be used.) This trigger puts the timer output in the active state and initiates the timer count-down sequence. When the count reaches zero, the output goes inactive until another trigger is given. The pulse width is

Timer Clock Period $\times$ Number in Counter.

If another trigger is given while the timer is still decrementing, the initial number from the timer registers is reloaded thus extending the pulse. The DP8570A remains operational in this mode until the start/$\overline{\text{stop}}$ bit is reset.

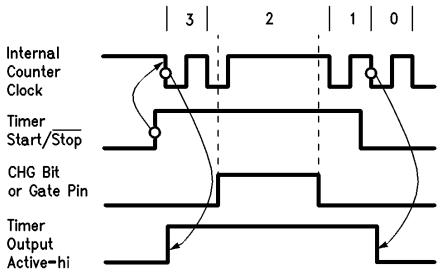

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FIGURE 2. Mode 0—Single Pulse Generator

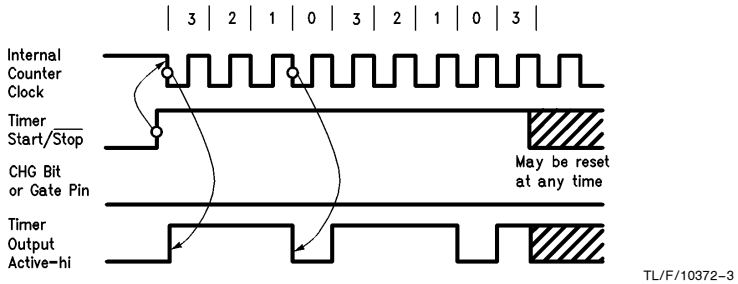

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FIGURE 3. Mode 1—Rate Generator

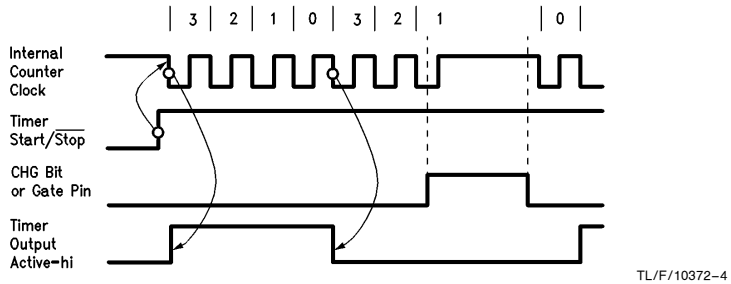

FIGURE 4. Mode 2—Square Wave Generator

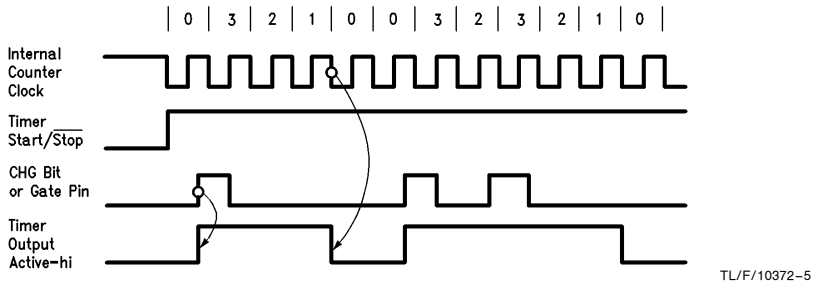

FIGURE 5. Mode 3—Retriggerable One Shot

3.2 Input and Frequency Selection

The DP8570A has a real time clock which can operate from any of four different crystal frequencies. The crystal frequency is selected in the real time mode register (Table II).

TABLE II. Real Time Mode Register
Crystal Select Bits, D7, D6

XT1	XT0	Crystal Frequency
0	0	32.768 kHz
0	1	4.194304 MHz
1	0	4.9152 MHz
1	1	32.000 kHz

This crystal frequency or a lower frequency derived from it can be used to clock the timers by programming the C2, 1, 0 bits in the timer control registers (Table III) to values 001 to 111 inclusive.

TABLE III. Timer Control Registers
Input Select Bits, D5, D4, D3

C2	C1	C0	Timer Clock
0	0	0	External
0	0	1	Crystal Frequency
0	1	0	(Crystal/Freq.)/4
0	1	1	93.5 μs (10.7 kHz)
1	0	0	1 ms (1 kHz)
1	0	1	10 ms (100 Hz)
1	1	0	0.1s (10 Hz)
1	1	1	1s (1 Hz)

Alternatively, the DP8570A timers can be clocked externally via the TCK pin by writing 000 to these input clock select bits. Falling edges of a 50% duty cycle input on the TCK pin clock the timer(s) at up to 10 MHz.

The other DP8570A timer input pins are G0 and G1 for timers T0 and T1 respectively. Their action depends on the mode selected and is described above.

3.3 Output and Interrupt Selections

The T1 pin on the DP8570A is a dedicated output from timer 1, whereas the MFO pin can be configured as the timer 0 output by programming the output mode register (Table IV).

TABLE IV. Output Mode Register
Output Pin Configurations

D7	D6	MFO
0	0	INTR
0	1	T0
1	X	OSC

MFO	D7	0 (For Timer/INTR Output)
	D6	T0/$\overline{\text{2nd-INTR}}$
MFO	D5	Push-Pull/$\overline{\text{Open-Drain}}$
	D4	Active-Hi/$\overline{\text{Active-Lo}}$
INTR	D3	Push-Pull/$\overline{\text{Open-Drain}}$
	D2	Active-Hi/$\overline{\text{Active-Lo}}$
T1	D1	Push-Pull/$\overline{\text{Open-Drain}}$
	D0	Active-Hi/$\overline{\text{Active-Lo}}$

The output mode register also sets up the T1, MFO and INTR pins as active high or low, push-pull or open-drain outputs individually. Care should be taken not to connect an open drain output to a voltage above the supply voltage in use at the time (i.e., normally V_{DD}, but V_{BB} in standby).

Whenever a timer goes to its inactive state (except when the start/$\overline{\text{stop}}$ bit is reset), it generates an interrupt, setting a bit in the main status register *(Figure 6)*. Interrupt control register 0 includes one bit for each timer (D6, 7 for T0, 1 respectively) to enable the interrupt at an output. The interrupt routing register has one bit per timer (D3, 4 for T0, 1 respectively) to route the interrupt to either the INTR pin or MFO pin (if programmed as a second interrupt pin). The interrupt status bit (D0 of the main status register) is also set when an interrupt (timer, alarm, powerfail or periodic) is pending at an output pin. Writing 1's to the main status register resets interrupts.

3.4 Standby Operation

The DP8570A power supply mode should be programmed on initial power-up by writing to bit D6 of the periodic flag register. Write 1 for single supply mode (hence no standby features) or 0 for battery backed-up mode. If thus configured, the device will enter "standby" mode if $V_{BB} > V_{DD}$. (See datasheet for hardware configurations.)

In standby the timers are still operational if bit D5 of the real time mode register is set, and if so, timer (and other) interrupts can be operational in standby if bit D4 is set. The TCK and G input pins, however, are locked out. In standby, MFO, INTR and T1 outputs are automatically configured in as open-drain outputs. When power is restored ($V_{DD} > V_{BB}$) they return to the output mode register configuration.

3.5 Power-Fall Operation

If a low going power loss signal is detected at the $\overline{\text{PFAIL}}$ pin, timer operation is unaffected, but the databus will be locked out.

4.0 PROGRAMMING STEPS

The following steps are recommended for setting-up DP8570A timer(s) after initial power-up.

a) **Main Status Register:** PS = 0, RS = 1.

b) **Real Time Mode Register:** Set crystal bits (Table II) and standby operation bits.

c) **Main Status Register:** PS = 0, RS = 0.

d) **Periodic Flag Register:** Set bit D6 for single-supply mode or reset it for backed-up mode and reset D7 so that the device is not in test mode.

e) **T0 and/or T1 Control Register:** Reset start/$\overline{\text{stop}}$ bit (D7) to ensure timers are not running.

f) **Interrupt Routing Register:** Route T0/1 interrupts (0 to INTR, 1 to MFO) if required.

g) **Main Status Register:** PS = 0, RS = 1.

h) **Output Mode Register:** Configure T1, INTR and MFO Outputs (Table IV).

i) **Interrupt Control Register 0:** Set T0/1 interrupt enable bits if required.

j) **MSB/LSB T0/1 Registers:** Load values for timer counter(s).

k) **READ:** main status register to clear old interrupts.

l) **Main Status Register:** PS = 0, RS = 0.

m) **T0 and/or T1 Control Registers:** start timer(s) with bits set for mode (Table I) and input clock (Table III).

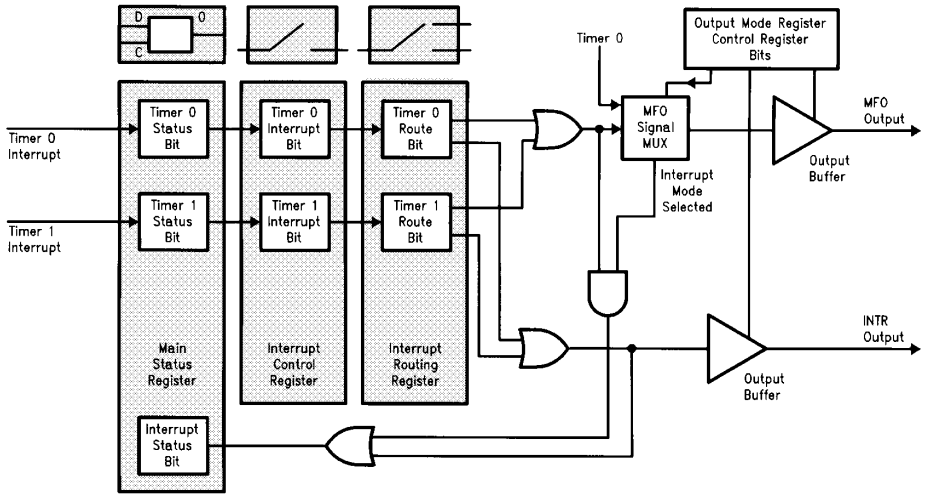

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FIGURE 6. DP8570A Timer Interrupts

If operating timers in a device already powered-up and in a known state, the above order need not be adhered to. Table V gives an example of programming a DP8570A which is already powered-up and operating correctly as a real time clock from some crystal frequency, with power supply configured and not in test mode. This example produces a 10 ms high pulse output (push-pull) every one minute using timer 1.

TABLE V. Programming Example

Write D7–0	Addr.	Reg.	Action
00000000	00000	MSR	PS = RS = 0
00000000	00010	TCR1	T1 Stopped
00000010	00000	MSR	RS = 1
0xxxxxxx	00011	ICR0	Disable T1 Intr.
00010111	10010	MSB1	} Timer
01101111	10001	LSB1	} Counter = 5999
xxxxxx10	00010	OMR	T1 = p–p, act.hi
00000000	00000	MSR	RS = 0
00101011	00010	TCR1	Start T1: Mode 1, 10 ms Input Clock

(x = Don't care in this example, but may affect other DP8570A operations.)

5.0 SYNCHRONIZATION ERRORS

As the operation of starting and stopping timers is normally asynchronous to the timer input clock, an error of up to one timer input clock period may occur. Similarly, when using the G input pins or count hold/gate bits, the following synchronization errors can occur depending on timer input clock selected:

External (TCK) + Up to One External Clock Period.

Crystal or Crystal/4 + Up to One Crystal Clock Period.

Other Selections + 0 to 32 μs.

6.0 DP8571A

The DP8571A differs from the DP8570A in the following ways.

a) It has no G0 or G1 input pins. The count hold/gate bits are fully functional however.

b) It has no T1 timer output pin. The T1 timer read bit can be used as in the DP8570A to read the value in the timer counter and interrupts are fully functional also.

c) The T1 bits in the output mode register (D1, 0) are RAM bits.

d) It has no TCK input pin.

e) An added feature of the DP8571A is it cascade mode, activated by programming T0 control register C2–0 input clock select bits to 000.

The C2–0 bits in the T1 control register are programmed to select its input clock (000 is not allowed).

6.1 DP8571A Cascade Operation

In the cascade mode, the output of timer T1 is the input clock for T0 *(Figure 7)*. The T1 bits in the output mode register have no effect on T1 and in this mode T1 output should be considered as active-low with falling edges clocking T0.

This mode gives the DP8571A 32-bit counter capability, raising the maximum counter value from 65,535 to 4,294,967,295 (Table VI). If used, for example, as a large hundredths of seconds countdown timer (with 10 ms input clock selected for T1), full range is increased from about 10.9 minutes to over 71 weeks. Also a larger variety of output waveforms can be realised by varying the values in the counters.

TABLE VI. Some Powers of 2 for Reference

Power of 2	Decimal Value
0	1
4	16
8	256
12	4,096
16	65,536
20	1,048,576
24	16,777,216
28	268,435,456
32	4,294,967,296

In cascade mode, timers cannot count down in binary from numbers greater than 65,535 if T1 contains any number other than FFFFhex. This is because T1's MSB/LSB register values are reloaded instead of FFFF when T1's count reaches 0000. The following example shows one way of working around this problem.

For countdown from 65,540 (00010004 hex) with cascaded timers:

a) Reset Timer Control Registers.

b) Write 00hex to T0 MSB, 01hex to T0 LSB registers and 00hex to T1 MSB, 04hex to T1 LSB registers.

c) Setup operating conditions for timers (outputs, interrupts, etc.).

d) Start T0 cascaded from T1, in mode 0–3 as required.

e) Start T1 with required input, in mode 1–3 as required.

f) After first T1 input clock (which loads T1 counter) and before the T1 count decrements to 0000hex, write FFhex to both LSB and MSB T1 registers.

The cascaded counters will continue to count down in effect as a single binary counter.

However, in modes 1 and 2, when T0 and T1 both reach 0000hex, the last values written to their LSB/MSB registers will be loaded (i.e. T0 = 0001hex, T1 = FFFFhex) unless action is taken to restore T1's original values (0004hex in this case) beforehand. One method would be for T0 to generate an interrupt on reaching 0000hex, which initiates a software routine to write the required values to T1 LSB/MSB registers before T1 decrements to 0000.

7.0 TEST MODES

Several features are available on the DP8570A/71A to ease testing by setting the test mode enable bit (D7) of the periodic flag register and programming the test register in page 0 as follows.

a) Set the enable MSB clock bit (D2): allows the two MSB halves of the timer counters to be clocked instead of the LSB halves (LSB must be 00).

b) Set signal route bits 0 and 1 (D3, 4): routes the T0 and T1 selected input clock signal (inverted) to the output and interrupt logic of the device instead of the timer outputs.

The DP8571A, timer 1 signal route bit does not affect the output of T1 clocking T0, but allows T1 interrupt logic to be driven from its (inverted) clock instead of its output.

c) Set crystal route bits 0 and 1 (D5, 6): The timer input clocks 10.7 kHz to 1 Hz inclusive (Table III) come from prescalers driven from an internal 32 kHz signal. If the crystal route bit is set for a timer, then its prescaler is instead driven directly by the crystal oscillator. Hence, an external signal generator faster than 32 kHz can be used to speed up testing of the timer. Real time mode register crystal select bits should be set to 32 kHz or 32.768 kHz in this case.

(Test modes are featured in detail on National Semiconductor Application Note 589.)

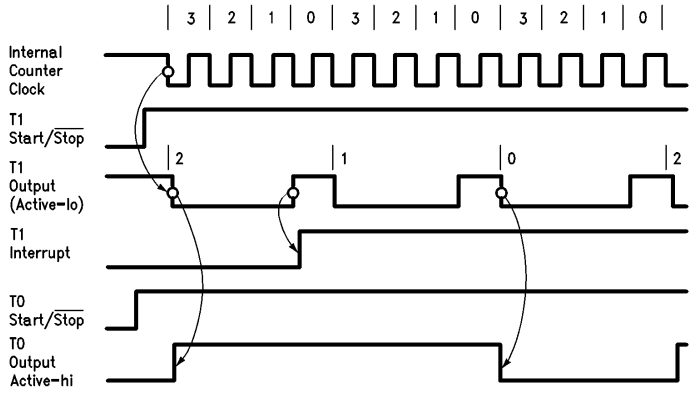

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FIGURE 7. DP8571A Cascade Mode, T0 Mode = T1 Mode = 1, Value in Counters: T1 = 3, T0 = 2

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