DP8459 Zoned Bit Recording

National Semiconductor
Application Note 599
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Driven by current progress in micro-processors, small information processing machines with mainframe-like power are rapidly moving toward storage intensive areas such as sophisticated file servers, photorealistic graphics systems, and engineering work stations. Disk drive makers are constantly trying to keep up with the increasing demand for higher capacity modules. The quest to store more and more data within the same hard disk assembly form factor has reached a point where advances in head and disk technology alone are not adequate to raise the areal density as quickly and economically as the industry wants.

Most of the high performance 5¼ in. Winchester drives today employ up to 15 Mb/s data transfer rates (RLL codes) and some even use ultra high resolution head/media in order to achieve a 700+ Mbytes capacity. Nevertheless, disk drive makers continue to seek out new ways and viable techniques to reach even higher capacity storage modules. While new methods of recording and higher performance recording components are being researched, other means of improvement using current disk technology are being investigated. One of these schemes is zoned-bit recording (ZBR) which is showing very respectible results. This method allows for packing more data on a disk surface using conventional head/disk components. The following discussion reviews the basis of ZBR and presents a design application using the DP8459 data synchronizer to simplify ZBR implementation.

ZBR BOOSTS DENSITY BY RECAPTURING VAST DISK AREA INEFFICIENTLY UTILIZED

ZBR came from an earlier idea called constant (linear) density recording, or (CDR) which pioneers of the disk community had toyed with nearly two decades ago. Conventional 5½ in. Winchesters usually employ a single data transfer rate such as 5 Mb/s, 10 Mb/s, 15 Mb/s, etc. The linear density of a given design is dictated by the maximum number of flux transitions that can be placed end-to-end on the inner-most data track of the disk surface. Since the circumferencial length of any track is proportional to its radius, the outer tracks become increasingly more loosely packed with data bits. As a result, a large portion (over 90%) of the disk surface in typical drives is not effectively utilized; i.e., valuable areal density is wasted.

The goal of CDR was to write the same linear bit density (constant flux change per unit length) to every track on the disk data surface. The reading and writing of data occur at frequencies which increase as a function of the diameter of the disk. This requires that multiple data rates be used, with each track operating at a different transfer rate, the outer tracks employing higher data rates than the inner ones. True CDR implementation can bear a substantial design/manufacturing overhead, e.g., sophisticated sector management is required since the number of sectors are different in each track, also non-conventional servo data is needed to accommodate the different data rate used for each track. Such a system demands additional firmware and software design. And because there are as many data rates used as the number of tracks employed in the disk drive, more elaborate tests are involved during manufacturing. Furthermore, the minute gain in recording capacity for using slightly different data rates in adjacent tracks might not be practical from a system's point of view. System overhead for a CDR drive thus might not be cost effective for current disk drive systems.

Zoned Bit Recording, on the other hand, is an engineering compromise to CDR. By adopting a more conservative approach, the ZBR method divides the disk data surface into a number of concentric bands called zones, with each one consisting of several tens to hundreds of tracks. The drive thus writes more data in zones on the outer edge of the disk (employing higher data rates) than in zones toward the spindle center. This is a design compromise where a substantial gain in areal density can be achieved with a much lower design and manufacturing overhead. Please refer to *Figure 1a* and *1b* which depict the bit distribution from a pre-recorded periodic pattern over different tracks.

The reemergence of CDR or ZBR was facilitated by current advances in the LSI read channel electronics. In particular, the monolithic data synchronizer/data separator integrated circuits have been a significant driving factor. About five years ago such a function (for 5 Mb/s data rate only) would have typically occupied a good portion of the electronic card cage in a drive system. Today many chip design houses can produce the core of the data synchronizer function in a single chip. However, few commercially available devices could meet the needs for high performance CDR and ZBR implementations. The DP8459 data synchronizer stands out with unique features specially designed to address this application.

DP8459 INCORPORATES FEATURES FOR ZBR

The key features of the DP8459 which make it ideal for multiple data rate operation reside in the Timing Extractor and VCO sections of the chip. They enable a broad range of data rate operation, plus the external support components require minimal programming. (Please refer to *Figure 2*.)

Conventional synchronizer chips may require a passive delay line to perform the task of window alignment. For ZBR designs that means many delay modules are needed to be multiplexed for operation requiring different data rates. Furthermore, they may have to be custom made to obtain those precise and non-standard delay values. For higher performance data synchronizer circuits and particularly for applications involving higher data rates, some PLL chipmakers use external resistors to control duty cycle of the VCO waveform. This approach utilizes the opposite (rising and falling) edges of the VCO output as a delay line. But, such chips may still require the trimming of an external resistor to attain optimum duty cycle symmetry for the desired delay time. Moreover, they would invariably require the switching of an external bank of precision resistors in ZBR.

The timing extractor block of the DP8459 represents a second PLL operating in tandem with the main PLL of the device. It is an accurate variable active delay line whose function is to establish synchronization window alignment so that the expected data bit is optimally centered about its decode window. The resultant delay is nominally equivalent to one half of the period of the reference clock.

The DP8459's built-in tracking silicon delay line completely obviates the need to switch external components. It takes

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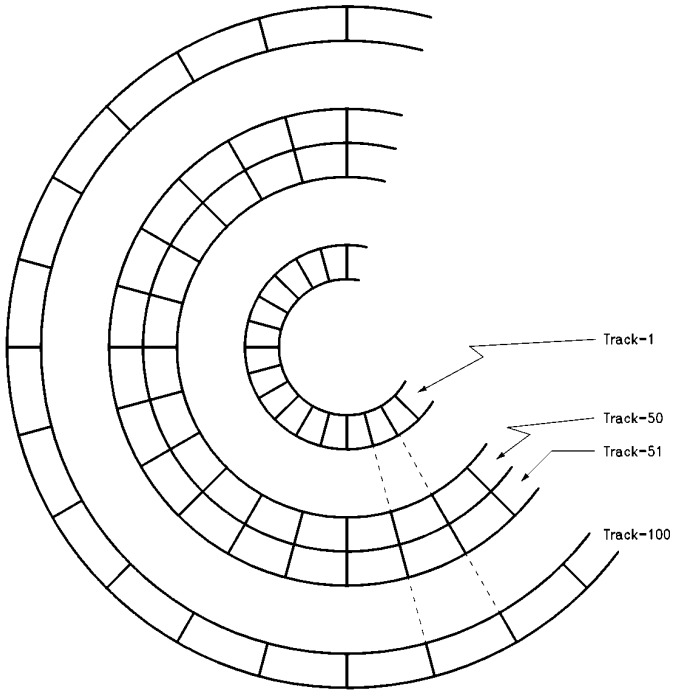

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FIGURE 1a. Single Data Rate

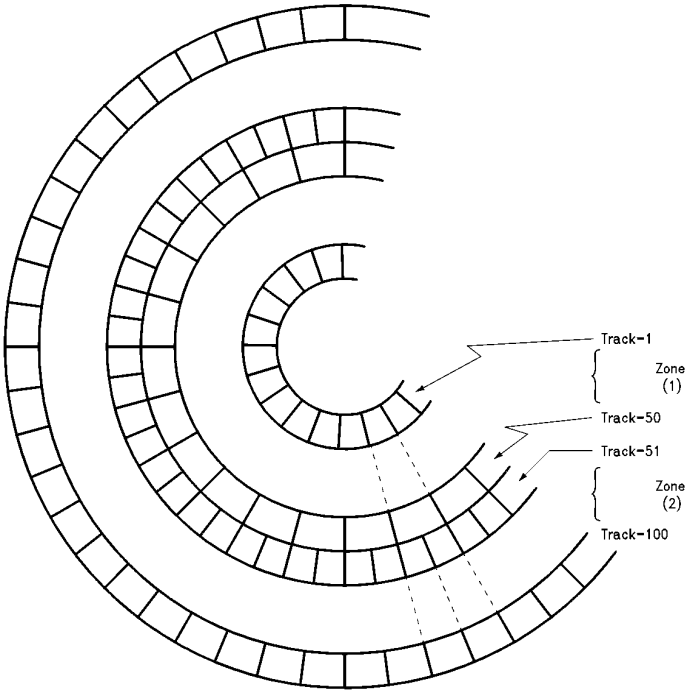

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FIGURE 1b. Multiple Data Rates

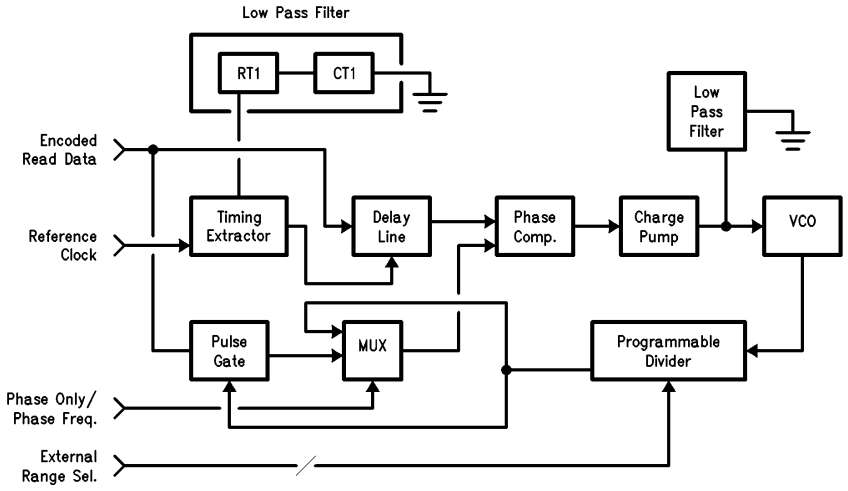

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FIGURE 2. Simplified Block Diagram of the DP8459 PLL

full advantage of the stable timing relationship from the reference clock input. The reference clock can be a crystal oscillator, a closed loop servo clock, or a programmable clock generator chip such as National Semiconductor's DP8531. The resistor-capacitor (Timing Extractor Filter) shown in *Figure 2* is employed for stabilizing the secondary PLL. The delay line performance is strictly a function of the reference clock accuracy, and is insensitive to the external components associated with the extractor as well as to supply voltage, temperature and IC process variations. Furthermore, the Time Extractor Filter (RT1 and CT1) components need not be changed for different data rates in ZBR. Simply choose the manufacturer's suggested values associated with the lowest data rate employed.

The DP8459's unique ''auto ranging VCO'' design provides another important advantage for ZBR. The reference clock frequency also sets the ''center frequency'' of the VCO automatically for the selected data rate, thus, no external components are needed for the VCO. The VCO section of the synchronizer consists of a high frequency oscillator and a programmable modulus divider. This arrangement provides a continuous range of VCO operating frequencies from 500 kHz to 50 MHz (range selection is via a 3-bit word input). The data rate range extends from 250 Kb/s to 25 Mb/s with MFM, [2, 7], and [1, 7] codes and from 250 Kb/s to 10 Mb/s for GCR codes. The DP8459 again simplifies multiple data rate applications as it requires no adjustment of any external VCO resistor/capacitor, LRC tank, or separate VCO circuitry. This not only facilitates design and testing of products, it also reduces unwanted noise from coupling to sensitive nodes. In addition, with ZBR designs operating over a 2:1 VCO frequency range, users may not need to change the range select control word, which further simplifies the design.

ZBR DESIGN CONSIDERATIONS

Unlike the controller section of a ZBR design, whose firmware and software can become more complex in order to handle a different system of sectoring, the DP8459 PLL bears practically no additional overhead. Whether one wishes to produce a system with 8 zones or 64 zones, it is important to recognize that the DP8459 synchronizer eases drive system designs by reducing the number of external components required and eliminating the need for trimming and switching critical components. ZBR implementation is simple with the DP8459, as is shown by the system block diagram in *Figure 3*. For ZBR operation, the Reference Clock input frequency must be changed whenever a different data rate (zone) is used. This can be accomplished with a crystal based programmable clock chip, such as National's DP8531. If the input is derived from a PLO (closed loop servo clock) the Reference Clock frequency would automatically update to the proper frequency as the servo head positions to a different zone.

In general it is not necessary to employ different loop filter components for every zone, especially if the adjacent zones are designed to operate over a small range of data rates. A single (compromised) 2nd order low pass loop filter should deliver acceptable performance margins, even when operating with a 2:1 ratio of data rates, for most of the drive designs. Of course there might be some designers who prefer to use more exotic filter configurations and/or to switch several loop filters to optimize system performance. If one requires switching filters, the following discussion is presented for consideration.

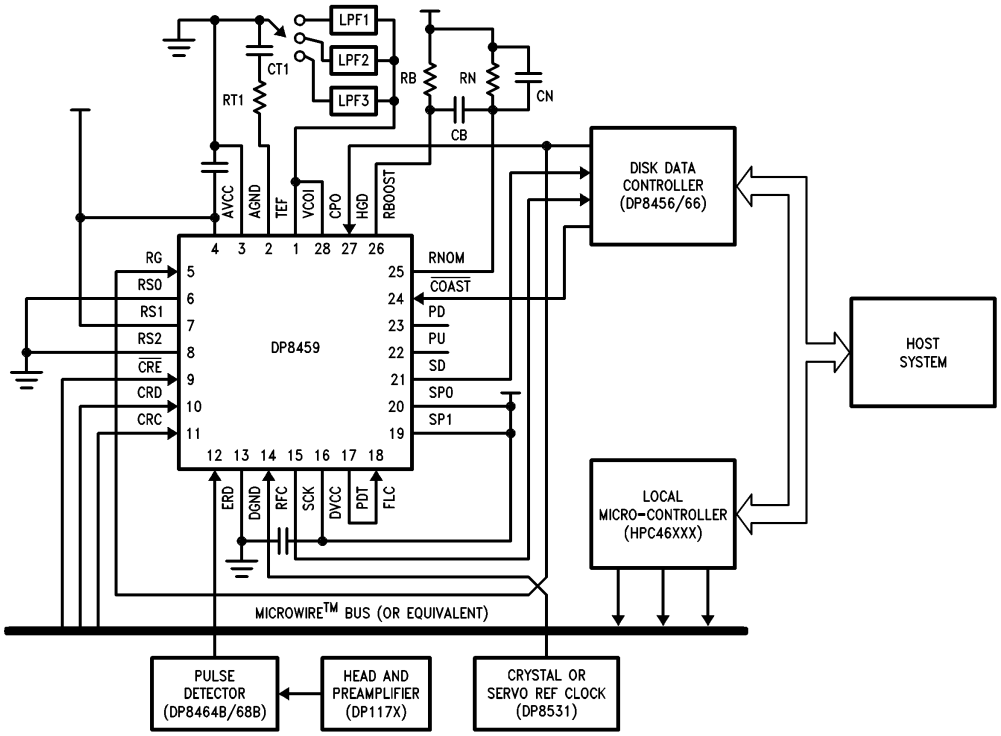

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FIGURE 3. Sample ZBR Drive System Employing the DP8459

Figure 4a shows multiplexing 3 complete sets of simple loop filter components via a switch. Alternatively one can modify the loop filter's characteristic BW or damping by changing only one of its resistor or capacitor values (see *Figure 4b*). Such a configuration can also produce an effective compromised loop filter which can handle a large number of data rates. (This scheme can help trim cost and minimize circuit board real estate.)

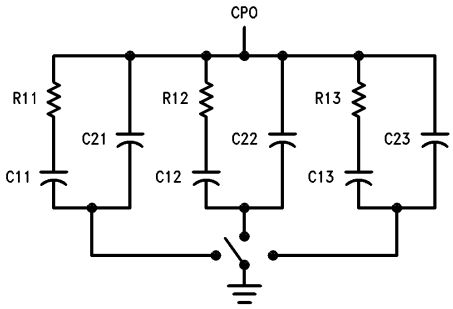

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FIGURE 4a. Switching of 3 Complete Lead-Lag Loop Filters

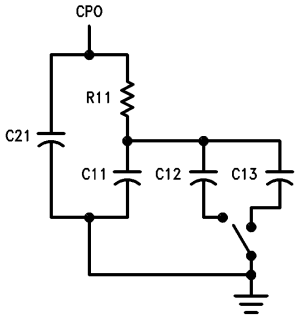

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FIGURE 4b. Modifying a Simple Filter with a Capacitor

Multiplexing several loop filters may be accomplished to advantage with micro-miniature mechanical relays. This is due to their superior isolation, lower leakage, and lower contact resistance compared to electronic switches. However, these advantages must be weighed against their slower response time and the need to suppress the relay coil's back EMF. Although ''wet'' contact relays are speedier and provide debouncing action, they can cost up to 10 times over conventional types. Analog (FET) switches have certain merits that make them suitable for switching of loop filters; these include long term reliability, fast response time, and high contact density per device. Furthermore, they lack the

back EMF hazards and do not consume much power to maintain closed ''contacts''. These features make them good candidates for multiplexing a large number of filter networks as in a ZBR application. However, some important device specifications must be examined before making a device selection. Commercial grade analog switches have a typical on-resistance of less than 40Ω, a terminal parasitic capacitance of 20 pF or less, and a leakage current of less than one nano-amp (but this spec can increase up to 50 times at high temperatures!). Nevertheless, they may offer acceptable performance as signal switches. The important issue is to determine the switch's performance under actual drive operating conditions and that typical loop filter characteristics can be maintained in the presence of parasitic elements. Another point to be aware of is that analog switches generally require bipolar power supplies, which may be unavailable in most drive systems. There are some instrumentation solid state relays which offer superior specs with attributes resembling those of mechanical relays, but their cost and contact density per device may not be cost effective for most present drive designs.

Since the DP8459 has provisions for a dual-port PLL filter network, higher order filters and active filter designs may also be used. This provides a third means to alter the loop filter characteristics conveniently via active filter implementation.

ZBR AND SINGLE DATA RATE DESIGN COMPARISON

Presently, high performance 5¼ in. Winchester companies are actively trying, with advanced head/media, to push recording densities to over 30k bit/in., track densities to over 1600 tracks/in., and are employing higher data transfer rates from 20 Mb/s to 24 Mb/s to achieve a Giga-byte capacity drive. It can be shown that without resorting to radically different technology and future generation recording components, this goal can be met by using ZBR techniques with conventional head/media.

The following design example compares a ZBR drive system and one using a single data rate; both assume moderate design parameters that are within current-generation disk technology:

The data rates and number of tracks used in each of the 9 zones for the ZBR design example above is listed below:

Zone	Tracks	Data Rate	Loop Filters
1	71	15.000 Mb/s	LPF1
2	71	15.600 Mb/s	LPF1
3	77	16.224 Mb/s	LPF1
4	80	16.873 Mb/s	LPF2
5	84	17.547 Mb/s	LPF2
6	87	18.249 Mb/s	LPF2
7	91	18.779 Mb/s	LPF3
8	94	19.738 Mb/s	LPF3
9	869	20.528 Mb/s	LPF3

Compared to the 15 Mb/s single data rate design, the ZBR design operating between 15 Mb/s and 20 Mb/s offers approximately a 30% increase in capacity. Operating the same system at a uniform data rate of 20 Mb/s is not feasible because the selected head/media characteristics (resolution limitations) would not have yielded acceptable performance over 40% of the inner tracks. At this increased data rate, higher grade head/media must be used to raise the drive's storage capacity. Although this ZBR design example needs to use higher data rates, the required read channel electronics to handle it are available and bear a lower system overhead compared to choosing the higher cost, grade, and less available (high bit density) media and (higher resolution and lower flying height) recording heads of today to support greater than 15 Mb/s single data rate Winchester disk drives.

Zoned-Bit Recording	RLL Codes	Single Data Rate Design (RLL)
Linear Density	20,404 Bits/In.	20,404 Bits/In. (Max)
Track Density	1,400 Tracks/In.	1,400 Tracks/In.
Data Surfaces	15	15
Data Rates	15 Mb/s to 20 Mb/s	15 Mb/s
Data Rate Spread	4% on Adjacent Zones	Not Applicable
No. of Zones	9 Zones	1 Zone
Loop Filters	3 Sets	1
Unformatted Capacity	1,016.3 Mbytes	721.5 Mbytes

CONCLUSION

The Zone-bit Recording concept is rapidly gaining popularity for the next generation of high capacity disk drive designs. The DP8459 high performance data synchronizer chip is truly designed to address the special needs of ZBR applications. It eases ZBR designs by eliminating cumbersome adjustment and switching of critical resistor/capacitor components for the VCO and delay line sections of the data synchronizer circuit. The combination of using the DP8459 device and ZBR techniques provides an economic and reliable solution to enhance the value and performance of disk drives, making them more cost effective to manufacture. This design methodology can achieve a significant increase in storage capacity while using existing disk technology. The DP8459 can be used in the manufacture of high performance, high capacity, multiple data rate flexible disk, optical disk, and giga-byte capacity 5¼ in. Winchester drives.

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