TP3420A S Interface Device (SID) User's Guide

National Semiconductor
Application Note 665
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July 1994

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RELATED MATERIAL

This manual assumes that the user is familiar with the ISDN Basic Rate Interface and its applications.

Other applicable documents include:

- TP3420A "S" Interface Device (SID) Data Sheet
- TP3076 COMBO II™ Data Sheet
- HPC16400E Communications Controller Data Sheet
- HPC16400E User's Manual
- CCITT I.430 Basic Access User-Network Interface — Layer 1 Specification
- ANSI T1.605 Specification
- TP3420A Line Interface Circuit Considerations, AN-872
- Interconnecting NSC TP3420A SID to Motorola SCP/HDLC Device, AN-931

1.0 INTRODUCTION

The TP3420A SID (S Interface Device) is a complete monolithic transceiver for data transmission on twisted pair subscriber loops. All functions specified in CCITT recommendation I.430 for ISDN basic access at the "S" and "T" interfaces are provided, and the device can be configured to operate either in a TE (Terminal Equipment), in an NT-1 or NT-2 (Network Termination) or as PABX line-card device.

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As specified in I.430, full-duplex transmission at 192 kb/s is provided on separate transmit and receive twisted pair wires using Alternate Mark Inversion (AMI) line coding. Various channels are combined to form the 192 kb/s aggregate rate, including 2 “B” channels, each of 64 kb/s, and 1 “D” channel at 16 kb/s. In addition, the 800 b/s multiframe channels for layer 1 maintenance is provided.

All I.430 wiring configurations are supported by the SID, including the “Passive Bus” for up to 8 TE’s distributed within 200 meters of low capacitance cable, and point-to-point connections up to at least 1500 meters. Adaptive signal processing enables the device to operate with low bit error rates on any of the standard types of cable pairs commonly found in premise wiring installations.

This user’s guide is intended to complement the device data sheets and is primarily aimed at ISDN TE, NT1, NT2 and TA designs that incorporate SID S/T transceivers. The user should refer to the TP3420A, TP3076 ISDN COMBO and HPC16400E data sheets for specific functions supported by these devices.

2.0 LINE INTERFACE AND TRANSMISSION PERFORMANCE

The components that are integral parts of the system design around the S/T interface and work in conjunction with the SID are dealt with in this section. Choice of the appropriate components will lead to reliable equipment design and superior performance.

2.1 Master Clock Source

The clock source for TP3420A may be provided with a commercially available crystal or an external clock source meeting the frequency requirements as explained in the following sections.

2.1.1 Crystal Oscillator

The SID clock source may be either a quartz crystal operating in parallel mode or an external signal source at 15.36 MHz. The complete oscillator (crystal plus the oscillator circuit) must meet a frequency tolerance specification of ±100 ppm total to comply with the CCITT I.430 specification for TE applications. The frequency tolerance limits span the conditions of full operating temperature range (commercial or industrial) and effects due to aging and part-to-part parameter variations.

The crystal is connected between pin 5 (MCLK/XTAL) and pin 6 (XTAL2), with a 33 pF total capacitance from each pin to ground as shown in *Figure 1*. The external capacitors must be mica or high-Q ceramic type. The use of NP0 (Negative-Positive Zero coefficient) capacitors is highly recommended to ensure tight tolerance over the operating temperature range. The 33 pF capacitance includes the external capacitor plus any trace and lead capacitance on the board.

Crystal Requirements:

Nominal frequency of 15.360 MHz, frequency tolerance (accuracy, temperature and aging) less than ±60 ppm, with R_S < 150Ω, C_L = 20 pF, parallel mode, CO (shunt capacitance) < 7 pF.

An external circuit may be driven directly from the pin XTAL2 (pin 6) provided that the load presented is greater than 50 kΩ shunted by a total of 33 pF of capacitance.

Crystal oscillator board layout is critical and should be designed with short traces that do not run parallel when in close proximity (to minimize coupling between adjacent pins). On multi-layered boards a ground layer should be used to prevent coupling from signals on adjacent board layers. Ground traces on either side of the high frequency trace also helps isolate the noise pickup.

2.1.2 External Oscillator Configuration

An external 5V drive clock source may be connected to the MCLK (pin 5) input pin of the SID as shown in *Figure 1*. The nominal frequency should be 15.36 MHz with a tolerance of ±80 ppm. The SID provides a load of about 7 pF at the MCLK input pin.

2.1.3 List of Recommended Crystal Manufacturers

Monitor Products Co., Inc.

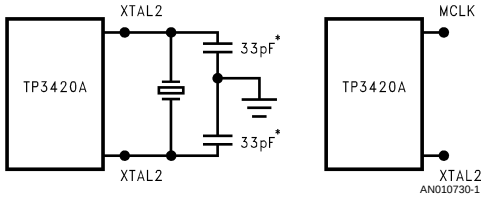
502 Via Del Monte

Oceanside, CA 92504

(619) 433-4510

Part No. MM-38A 15.36 MHz N

Freq. Tolerance (Total) ±60 ppm



*This includes the trace and lead capacitance on the board

FIGURE 1. Clock Circuits

2.2 Line Transformer Requirements

The electrical characteristics of the pulse transformer for the ISDN “S” interface are defined to meet the output and input signal and the line impedance characteristics as defined in CCITT recommendation I.430. The transformer provides isolation for the line card or terminal from the line; it also provides a means to transfer power to the terminal over the S-loop via the “phantom” circuit created by center-tapping the line side windings. A transformer is used both at the transmit and the receive end of the loop. These notes specify the tolerances of a transformer that is employed with the SID to meet the CCITT recommendation on output pulse mask and impedance requirements.

2.2.1 Line Transformer Ratio

The transmit amplifier if a 1:2 (N_p:N_S) transformer. Its primary is connected to the S loop while the secondary is connected to the device. The same transformer or optionally a 1:1 transformer can be used for the receive side. However, the 2:1 transformer is highly recommended per AN-872 to obtain the best longitudinal performance. The primary is connected to the S loop while the secondary is connected to the device with the SID pin Li-connected to the center tap.

2.2.2 Line Transformer Electrical Parameters

The tolerance on the electrical parameters of the 1:2 line transformer are tabulated in *Table 1* below.

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TABLE 1. Line Transformer Electrical Parameters

Parameter	Min	Typ	Max	Units
Ns/Np	1.98	2	2.02	—
Lp	22	30	37.5	mH
Ls	80	120	150	mH
Rp			4	Ω
Rs			5	Ω
LLp			16	µH
LLs			32	µH

The parameter mnemonics and their significance are explained in the paragraphs below.
The total capacitance looking into the primary winding when the secondary is open circuit should be ≤ 220 pF.

Line Transformer Winding Inductance (Lp, Ls)

The total inductance looking into the terminal from the "S" loop should be greater than 22 mH (> 2.5 kΩ between 20 kHz and 80 kHz). This is necessary to meet the low frequency output impedance specification in I.430 of > 2500Ω for frequencies ≥ 20 kHz. The primary winding of the transformer (the main component of inductance) should therefore have greater than 22 mH of inductance (Lp). The secondary winding inductance (Ls) is generally 4 Lp for the 1:2 transformer and Ls = Lp for the 1:1 transformer.

Total Capacitance at the Terminal End

I.430 specifies that the impedance into the Transmitter and Receiver must be > 2500Ω for frequencies < 80 kHz in a TE. The capacitance dominates this impedance, and must be limited to < 795 pF.

There are various contributors to this output capacitance:

— The TE cord, 300 pF (for the 7m length) capacitance or 350 pF (for the 10m length).

— the device driver pins, 10 pF–25 pF.

— The over-voltage protection circuit consisting of shunting diodes (8 pF).

The 1:2 transformer multiplies the capacitance on its secondary connections by 4 when observed from the line side. An allowable maximum for other distributed stray capacitances; Cd, is given by:

7m Cord Case: (25 + 8) x 4 + Cd + 300 ≤ 800 pF

which gives Cd ≤ 368 pF

10m Cord Case: (25 + 8) x 4 + Cd + 350 ≤ 800 pF

which gives Cd ≤ 316 pF

This is the most stringent case and determines the maximum allowable distributed capacitance Cd for the transformer and other miscellaneous capacitances.

Total Capacitance at the Network End

At the network end, there is no cord specified but the 2500Ω minimum impedance limit extends up to 106 kHz. The total capacitance must therefore be < 600 pF, hence:

(25 + 8) x 4 + Cd ≤ 600 pF

which gives Cd ≤ 468 pF

By restricting the Cd for the transformer to be ≤ 220 pF, sufficient margin is allowed for miscellaneous capacitances and flexibility in the protection circuit arrangement.

Line Transformer Winding Resistance Rp and Rs

Since the device output driver is a voltage-limited current source type, the value of the DC resistance of the transformer secondary is not critical.

The DC resistance of the primary side of the transformer does affect the load seen by the current source driver and hence needs to be constrained in order to meet the overall specification of ±10% maximum variation of the output pulse height when terminated into 50Ω.

Line Transformer Leakage Inductance

Unlike competing devices the TP3420A controls the output pulse transition times, and hence the leakage inductance is not critical. Overshoot and ringing are within the pulse mask for values in excess of 50 µH.

Longitudinal Balance

The longitudinal balance specification is as follows:

10 kHz to 300 kHz: ≥ 54 dB

300 kHz to 1 MHz: Value decreasing at 20 dB per decade.

Bifilar windings on the line side are necessary to meet these requirements. The transformer must connect to the TP3420A as shown in AN-872.

2.2.3 Printed Circuit Board Layout Considerations

Taking care of the pcb layout in the following ways will help prevent noise injection into the receiver front-end and maximize the transmission performance:

place the transformer and TP3420A on the same ground plane;

keep short connections between the transformer and TP3420A;

keep short connections from the transmission lines to the transformer;

minimize crosstalk between the transmit and receive pairs;

minimize crosstalk from the crystal into the transmit and receive pairs.

2.2.4 Line Transformer Manufacturers

Pulse Engineering	Phone number: 619-674-8130		
	Part number: PE64995 (2:1 single transformer package)		
	Part number: PE65495 (2:1 dual transformer package)		
Valor	Phone number: 619-537-2500		
	Part number: PT-5055 (2:1 dual transformer package)		
	Part number: PT-5001 (2:1 single transformer package)		
MID-COM	Phone number: 800-643-2661		
	Part number: 671-6322		
Vernitron:	Phone number: 813-347-2181		
	Part number: 328-0044		
VAC	Phone number:	Germany	(49) 6181-38-2544
		USA	908-4494-3530
	Part number:	ZKB402	
		ZKB409	

Note: Surface mount transformer are also available from Pulse Engineering and Valor

2.3 External Protection Circuitry

Precautions are to be taken to ensure that the TP3420A is protected against electrical surges and other interferences due to electromagnetic fields, power line faults and lightning discharges that may occur in the transmission medium. Protection circuits that are external to the device are recommended on both the primary and secondary sides of the line transformer. *Figure 2* provides a full protection circuit for the SID in TE mode. The diode stacks at the Lo and Li pins of the device are primarily provided to offer low impedance paths to electrical surges. On the transmit side in a TE they also avoid the clamping of the signals from other TE's and ensure that the minimum output impedance requirements are met even if V_{CC} is lost. In NT/LT applications only a single diode from each Lo pin to V_{CC} is required. External resistors in the receive path of the SID limit the surge current through the diodes and also form part of the low pass noise limiting input filter. This circuit can withstand at least 1000V pulses on the S interface. All the diodes in this circuit are of the type 1N4004. Low capacitance diodes are necessary to avoid exceeding the maximum allowed capacitance for the complete connecting cord and circuit impedance.

For surge protection on exposed wiring interfaces, a low capacitance gas discharge tube should be added across the terminals as shown in *Figure 2*. In addition to surge protection, the transformer must be protected against power line faults by the addition of fuses or low value ($<10\Omega$) fusible resistors. The series resistance of the protection must however, be taken into account when specifying the resistance of the transformer windings, to ensure that the transmit pulse mask requirements are met.

2.3.1 DC Bias Capacitors for Analog Reference

Two decoupling capacitors (0.1 µF mica) and 10 µF (electrolytic) are connected between pin 19 of the device and its ground connection. These capacitors decouple the midpoint of a two-resistor potential divider (inside the device) and provide an internally buffered reference for the analog circuitry.

2.4 Transmission Performance

The TP3420A SID is designed with the goal of substantially exceeding the transmission performance requirements as specified in the I.430. This is made possible in the design by employing complex signal-processing techniques in the receiver front end design. For example, in the receive path, an analog prefilter removes >200 kHz noise signals, which is then followed by an adaptive line equalizer to correct for the attenuation of loops in excess of 1.5 km in length with superior performance. A continuously tracking adaptive threshold circuit optimizes the slicing levels in the detection circuits for correct detection of received data even on long lossy loops. Finally a digital filter discriminates against in-band noise. This architecture results in longer range error-free transmission in point-to-point applications, and greater spread of terminals in extended passive bus applications than simpler first-generation tranceivers.

The SID transmission performance was measured on 24 AWG PIC cable which has approximately 90 nF/km capacitance and 180 Ω/km resistance. This cable has a loss of 7.8 dB/km at 96 kHz. Performance was measured with three different configurations, namely:

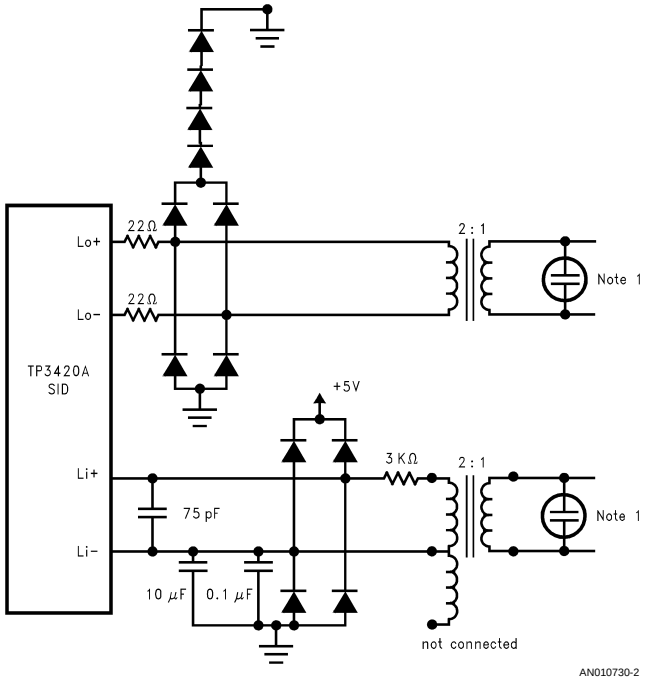
1. Point-to-Point;
2. Short Passive Bus;
3. Extended Passive Bus.

In all these tests, noise sources recommended by the I.430/ANSI standard per Section 8.6.2.1 were complied with. The setups are shown in *Figures 3, 4* and *Figure 5*, along with the tables showing the actual range measured versus the I.430 recommended range. Noise sources were located close to the NT receiver and injected via two 1 kΩ resistors to avoid affecting the loop impedance significantly. Activation and error-free transmission could be accomplished on either end of the S interface in the case of the point-to-point configuration and from any one of the TEs in the case of both passive bus configurations. The error-rate was measured in a B channel in these tests.

The TEs and NT in all these configurations used TP3420A SIDs. The NT device in the point-to-point and extended passive bus cases was in NTA mode while the short passive bus used NTF mode. The results tabulated show that the SID exceeds the I.430 and ANSI range requirements.

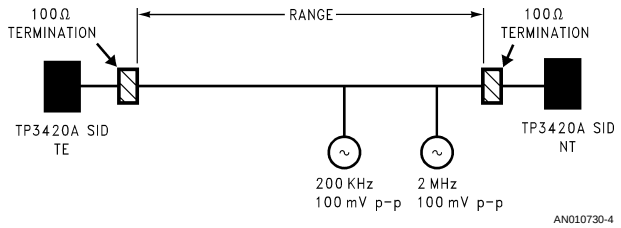
Pulse Shape and Impedance Templates

As shown in *Figure 6* and *Figure 7*, the TP3420A SID transmitter output pulse shape and amplitude comply with the specified pulse masks for both the 50Ω and 400Ω test load impedance cases. Plots in *Figure 8* and *Figure 9* show the receiver input impedance and output impedance. These tests were done with the recommended Pulse Engineering transformers. The SID output drivers are specifically designed with controlled rising and falling transitions for minimal pulse overshoot and undershoot with a wide range of transformer designs. Furthermore, the following figures show the transmit and receive impedance templates are met with the specified cable connected and the protection networks shown in Section 2.3. The device has been successfully tested for pulse shape and impedance with various other manufacturers' transformers.



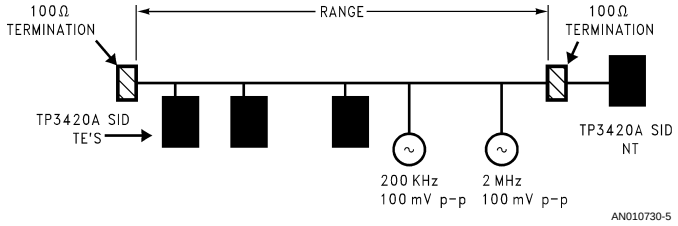
Not normally required if TE is used only on internal wiring.

FIGURE 2. External Protection Circuit — TE Application



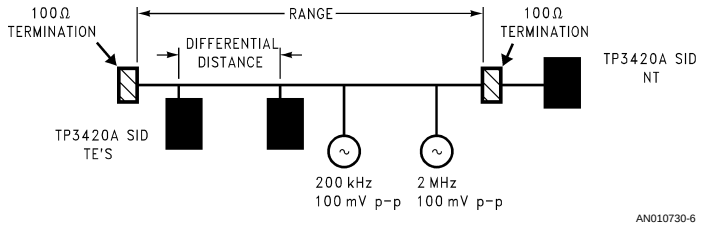
TP3420 SID	I.430 Specification
1800m	1000m

FIGURE 3. SID Point-to-Point Range Measurement



TP3420 SID	I.430 Specification
200m	100m–200m

FIGURE 4. SID Short Passive Bus Range Measurement



TP3420 SID		I.430 Specification	
Range Meters	Differential Distance Meters	Range Meters	Differential Distance Meters
675	275	500	25 to 50
1075	275		
1250	250		
1500	100		
1650	50		

FIGURE 5. SID Extended Passive Bus Range Measurement

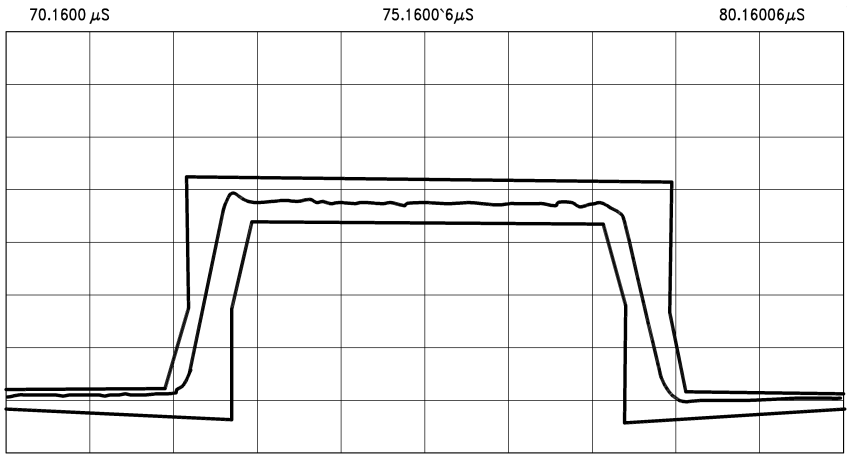


FIGURE 6. SID Output Pulse Shape and Amplitude vs Mask (50Ω)

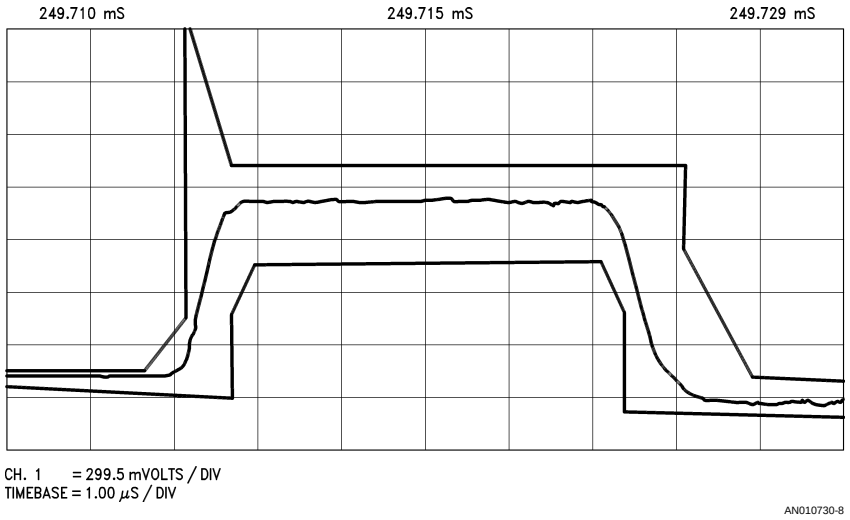


FIGURE 7. SID Output Pulse Shape and Amplitude vs Mask (400Ω)

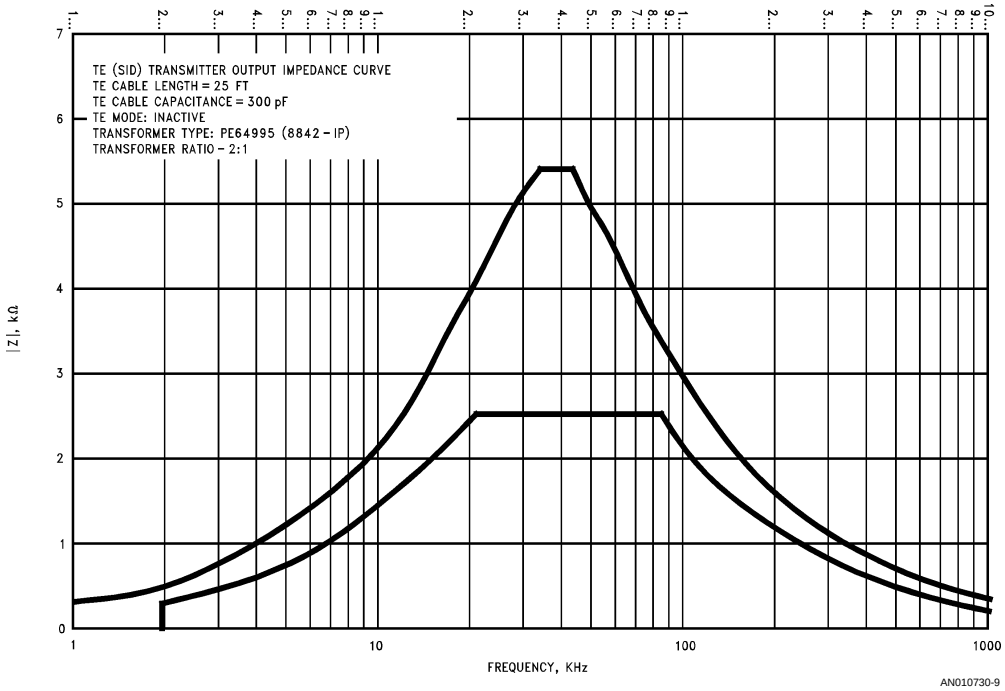


FIGURE 8. SID Receiver Input Impedance Curve

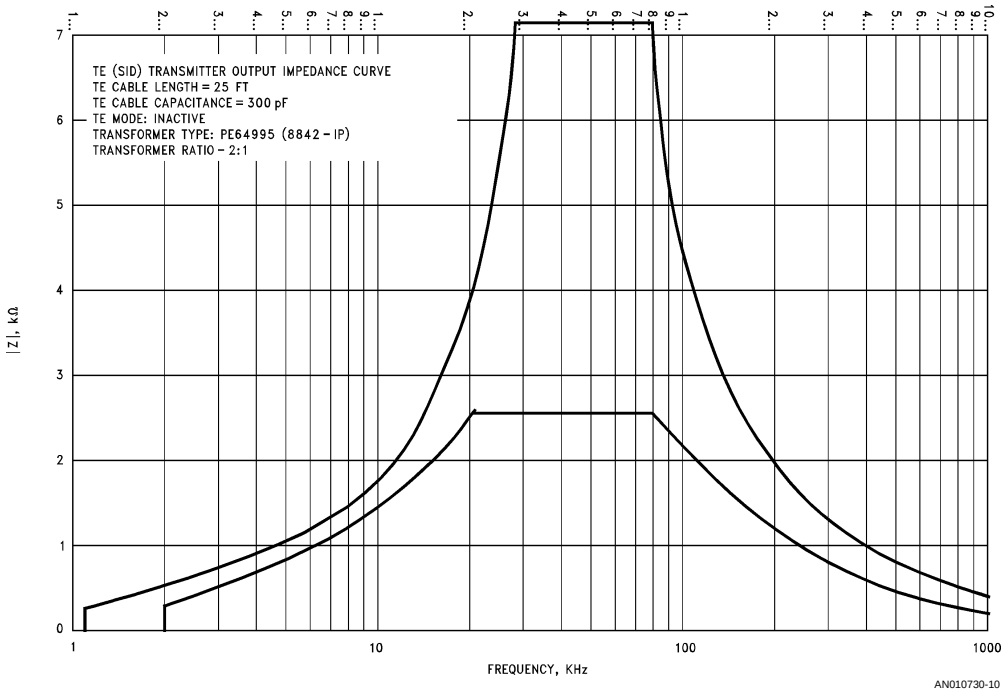


FIGURE 9. SID Transmitter Output Impedance Curve

3.0 TP3420 DIGITAL INTERFACE

To retain the flexibility of interfacing the TP3420A with a variety of other products, two digital interfaces are provided on this device. The first interface is called the Digital System Interface (DSI) and is for synchronous transfer of B and D channel information in one of the several popular schemes which encompass proprietary frame structures such as COMBO, IOM, SLD and IDL. The second interface is National's popular MICROWIRE/PLUS interface which provides a means for synchronous serial data transfer between a microcontroller and one or more peripheral devices and is used for device mode control purposes. This interface can work in the ALTERNATE MICROWIRE mode which is compatible with the Motorola SCP. See TP3420A Data Sheet for details.

3.1 Digital System Interface Formats

The Digital System Interface (DSI) combines B1, B2 and D channel data onto common pins Br and Bx to provide maximum flexibility. At this interface, phase skew between transmit and receive directions may be accommodated at the line card or NT-1/2 end since separate frame sync inputs FSa and FSb are provided. Each of these synchronizes a counter which gates the transfer of B1 and B2 channels in consecutive time-slots across the digital interface. The serial shift rate is determined by the BCLK input and may be any frequency from 256 kHz to 4.096 MHz. Thus, for applications on a PABX line card (in NT mode), the B1, B2 and D channel slots can be interfaced to a TDM bus and assigned to a time slot.

At the TE end, FSa is an output indicating the start of both the transmit and receive B channel data transfers. BCLK is also an output at the serial data shift rate, which is dependent on the DSI format selected. *Figure 10* illustrates the directions of BCLK, FSa and FSb clocks depending on the device mode TEM and TES or NT mode respectively.

Four multiplexed formats of B1, B2 and D channel data are supported by TP3420A SID and selection of these formats is via the control register.

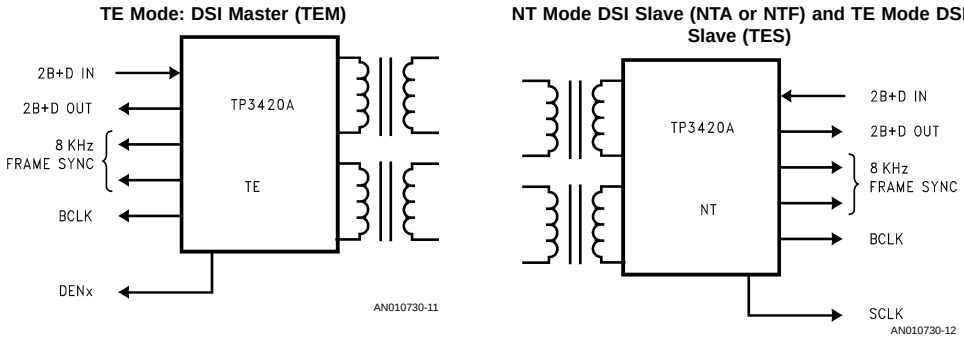
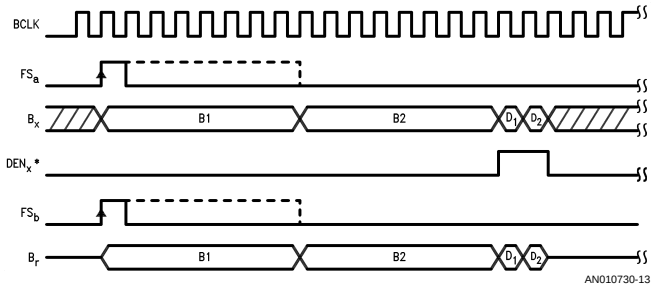
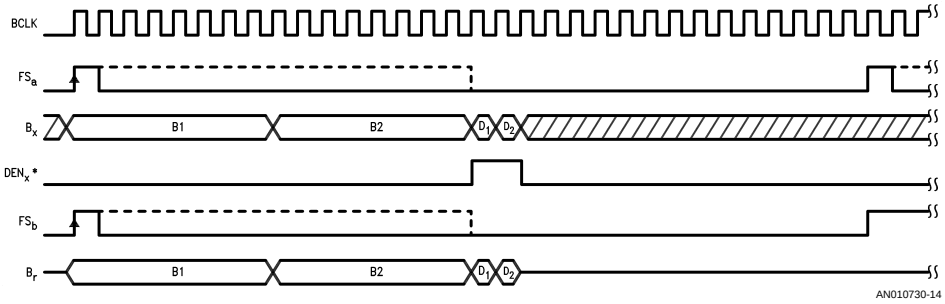


FIGURE 10. TP3420 SID Digital System Interface

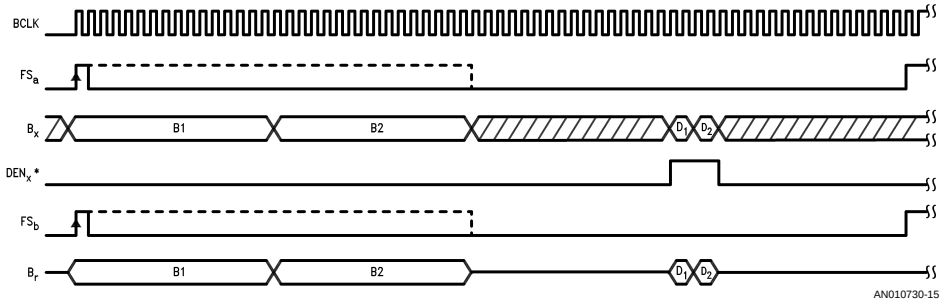
Format 1



Format 2



Format 3



Format 4

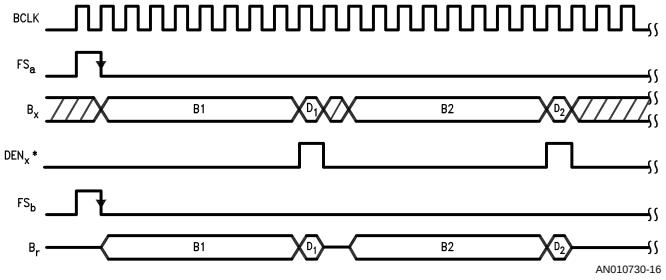
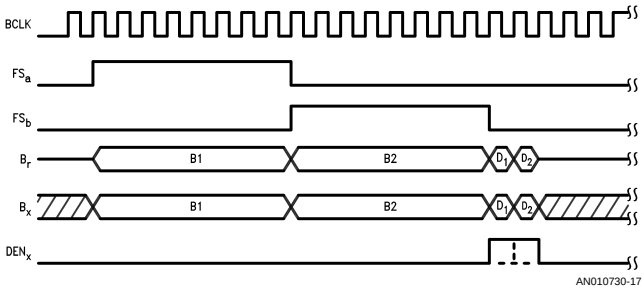


FIGURE 11. Digital System Interface Formats in NT and TES Modes

Format 1



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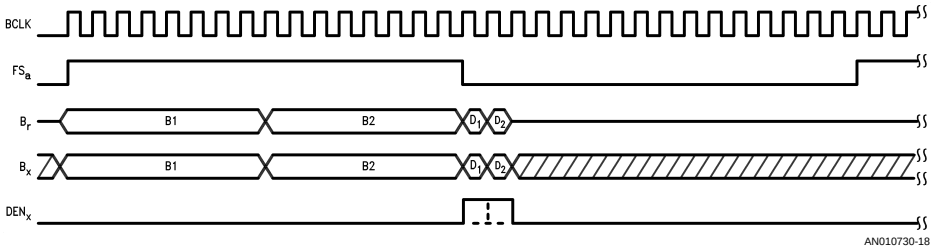
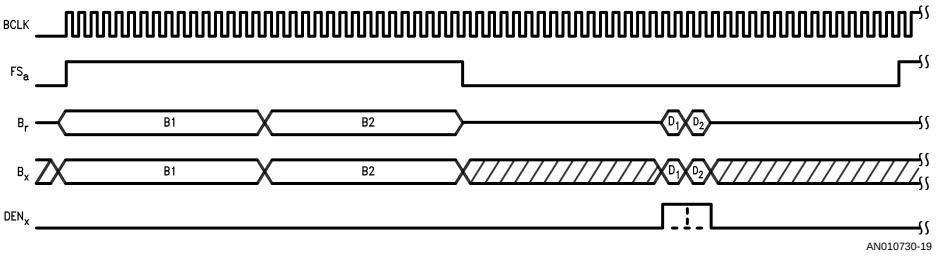


Format 3



Format 4

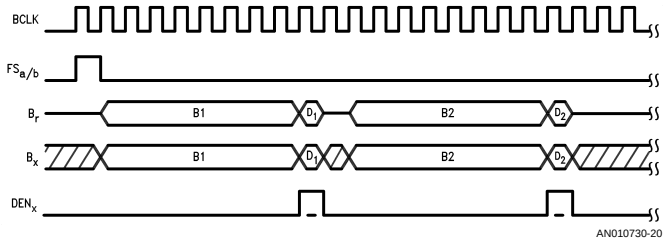


FIGURE 12. Digital System Interface Formats in TEM Mode

Figure 11 illustrates the four Digital Interface Formats for the NT and TES modes of the SID device and *Figure 12* show these formats for the TEM mode. *Table 2* presents the BCLK rates of the four DIF formats in both the Master and Slave modes.

TABLE 2. DSI Format Rates

Format	BCLK as DSI Master	BCLK as DSI Slave
1	2.048 MHz	2.56 kHz–4.096 MHz
2	256 kHz	"
3	512 kHz	"
4	2.56 MHz	"

3.2 TP3420A SID Digital System Interface and HPC16400E Connection

TP3420A SID can be used with a number of popular HDLC devices. These are MC68302, MC145488, Zilog/AMD 85C30, NSC HPC16400E please see TP3420A data sheet and AN-931 (Interconnecting NSC TP3420A SID to Motorola SCP/HDLC devices) for more information.

TP3420A SID, when used with National's HPC16400E Microcontroller, provides an elegant ISDN solution for TE and Line-card architectures. While the SID implements all the S interface functions, Layer 2 and 3 signaling and protocol layer procedures may be implemented in the HPC16400E by connecting the D-channel to HDLC#1 via the Digital System Interface. At the same time, one of the B channels may be routed to HDLC#2 on the HPC16400E for data protocol implementations.

The Serial Decoder block of the HPC16400E provides a means of flexible configuration of the device for various applications. *Figure 3* illustrates a simple block diagram functional description of the serial decoder and the various signals associated with it. The serial decoder is controlled by the contents of the SERDEC register of the HPC16400E.

Because the TP3420A has four different formats for multiplexing B and D channels on its Digital System Interface, it is important to setup the HPC16400E in the correct mode for compatibility with the chosen digital interface format from the TP3420A as shown in *Table 3* below:

TABLE 3. Relationship between the HPC Serial Mode and the SID DIF Format

HPC Serial Mode	SID DIF Format
4	1
4	2
3	3
7	4

This is done by the upper 3 bits of the SERDEC register in the HPC16400E.

The serial decoder of the HPC16400E in conjunction with the ENABLE SELECT logic provides the enable signal for data multiplexing. The serial decoder services the 2 HDLC channels (for a detailed discussion on the Serial decoder please refer to the HPC16400E data sheet). For each HDLC channel, there are two ENABLE SIGNALS, one for the Receiver and one for the TRANSMITTER. Each HDLC channel ENABLE signal can be connected to the EXTERNAL RECEIVER/TRANSMITTER ENABLE (REN1, TEN1, REN2 and TEN2) or the Internally Generated Enable strobe signals (B1, B2 and D) or can be used for ANDing of the EXTERNAL ENABLE and INTERNAL channel strobe signal. The HDLC Channel Enable Signals are selected by setting the 5 lower SERDEC register bits as shown in *Table 4* and *Table 5*:

TABLE 4. HDLC Enable Signals for Channel #1

Case	SERDEC Bit			TX1	RX1
	2	1	0		
1	x	0	0	D & TEN1	D
2	x	0	0	TEN1	D
3	1	1	0	B1	B1
4	1	1	1	B2	B2
5	0	1	1	TEN1	REN1
6	0	1	1	TEN1	B1

TABLE 5. HDLC Enable Signals for Channel #2

Case	SERDEC Reg Bit			TX2	RX2
	4	3	2		
1	0	0	0	B1	B1
2	0	0	1	B2	B2
3	0	1	0	TEN2 & B1	REN2 & B1
4	0	1	1	TEN2 & B2	REN2 & B2
5	1	0	x	1	1
6	1	1	x	TEN2	REN2

3.2.1 TP3420A SID and HPC16400E Connection for D-Channel

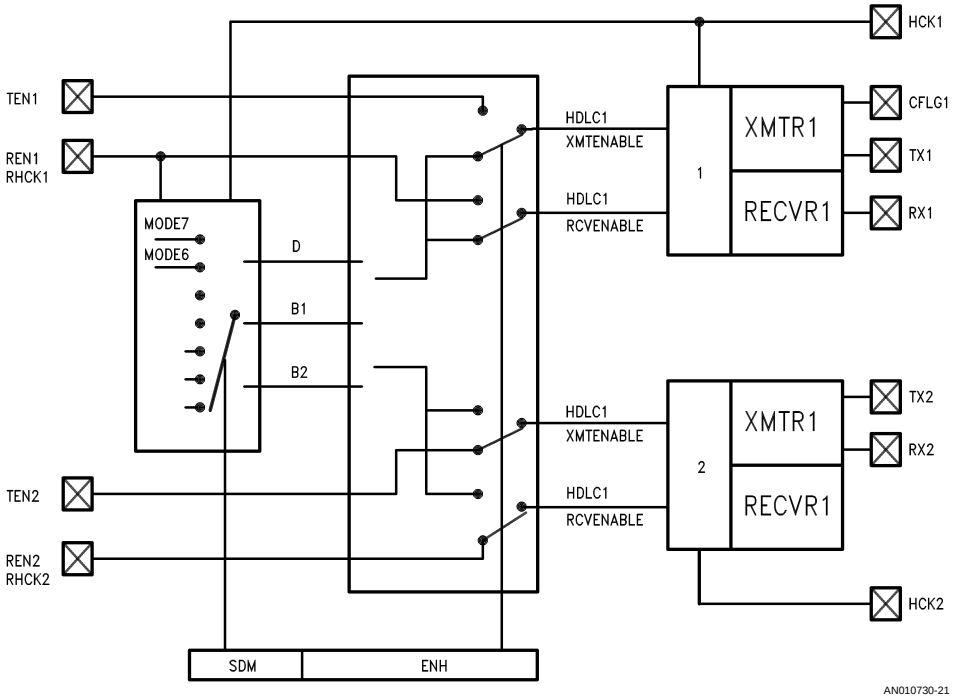
Figure 14 shows the connection of TP3420A SID's Digital System Interface signals to the HPC16400E serial decoder and HDLC Controllers 1 and 2 for the D-channel and B-channel respectively. For D-channel selection into the HDLC#1, the FSa signal on the DSI has to be connected to the REN1 (pin D0) signal on the serial decoder/HDLC #1. In this application Case 1 of HDLC enable signals for channel #1 in *Table 4* is used.

3.2.2 TP3420A SID and HPC16400E Connection for B-Channel

For B-channel selection into the HDLC#2, Case 1 or Case 2 of the HDLC enable signals for channel #2 for B1 or B2 channel respectively is used from *Table 5*.

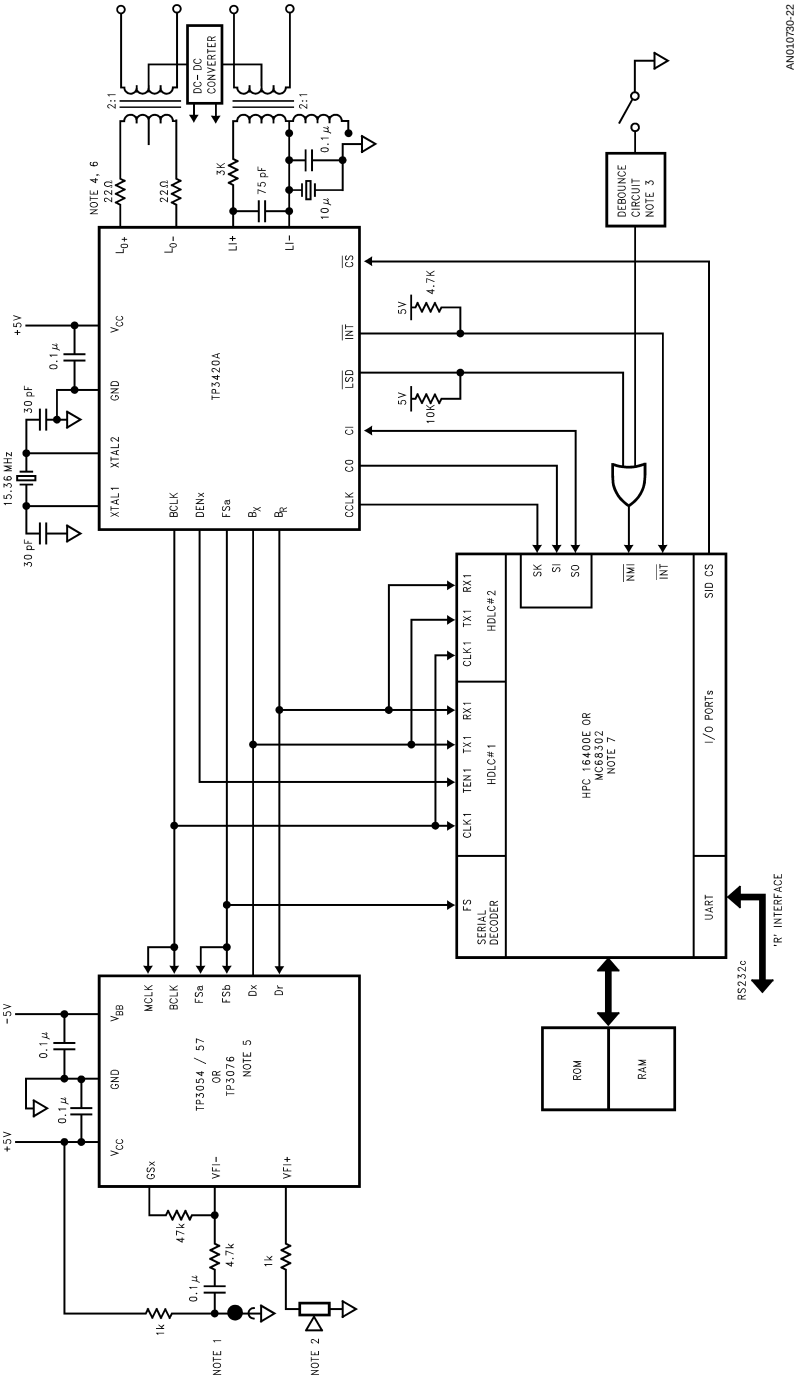
3.3 TP3420A SID Digital System Interface and TP3076 COMBO Connection

When one of the B channels in the ISDN stream is PCM coded voice, an ideal solution is to connect this B channel to a TP3076, National's PCM CODEC/filter for ISDN. The TP3076 is second generation combined PCM CODEC and filter devices optimized for digital telephone applications. The device is A-law and µ-law programmable and employ a conventional serial PCM interface capable of being clocked up to 4.096 MHz. A number of programmable functions, including the transmit and receive gains, may be controlled via a serial control port. Please refer to TP3076 data sheet for more details.



Note: All switches are independent. This diagram does not show ANDing of internal and external enables.

FIGURE 13. HPC16400E Serial Decoder Block



Note 2: Primo type EM80-PMI2 or similar
Note 3: Primo type DH31 or similar
Note 4: Only necessary if a mechanical switch is connected to the NMI input of the HPC
Note 5: See Line Interface Protection circuit section.
Note 6: When using TP3076, connect the MICROWIRE bus to the part.
Note 7: R = 22Ω when using a PEB4995 transmit transformer and a connecting cord. See AN-872 (TP3420A Line Interface Circuit Considerations) for more details.
Note 8: See AN-931 (Interconnecting NSC TP3420A SID to Motorola SCP/HDLC devices) for detailed connections to MC68302.
Note 9: When using X86 or 680XX microprocessors, use TP3465 to generate MICROWIRE port.

FIGURE 14. Typical Application in a TE and/or TA

The diagram of *Figure 14* shows the connection between the TP3420A and TP3076 in the implementation of an ISDN phone. TP3420A SID is programmed for DIF1 format at the DSI in this application. Besides, the voice channel should always be in B1 slot of the DIF FORMAT1 for this setup to work. If the network assigns the B2 channel to a voice call, it

has to be switched into the B1 slot in the DSI frame format using the command BEX in the TP3420A control register. The FSx, FSr pins on the TP3076 are connected to the Fs pin on the TP3420A. MCLK, BCLK on the TP3076 are connected to BCLK on the TP3420A, and Dx, DR signals on the TP3076 are connected to Bx and Br signals respectively on the TP3420A SID. Under these conditions, and assuming µ-law is chosen, for proper operation the control register on the TP3076 is programmed as follows:

TP3076 Control Register Contents

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

In this case, the TP3076 is in non-delayed timing mode and the time slot always begins with the leading edge of frame sync input FSx, FSr.

3.4 NT-2 Synchronization (TP3420A)

The NT-2, typically a PBX, has a number of S interfaces on the customer's side and, if it uses Basic Access to the network, each trunk is a T interface to an NT-1 as shown in *Figure 15*. Functionally the S and T interfaces are identical, i.e. both conform to I.430. Thus, the SID can operate on the S interface side, with NT more selected (either fixed or adaptive receive sampling as appropriate for the wiring), and on the T interface side the SID operates like a terminal, in TE mode. However, the complete NT-2 must have all its clocking and data interfaces synchronized to the network. This requires a system clock, at typically 2.048 MHz, to be phase-locked to one of the T interfaces. The SID includes this PLL, with an SCLK output on the DENx pin, when used in TE mode DSI Slave (TES) only. Any one of the SID's can provide this clock, but all will take their BCLK and Fs timing from the same one, i.e. they are slaved to the network clock and synchronized to each other. In this way, clocking is synchronized all the way from the network to the terminal.

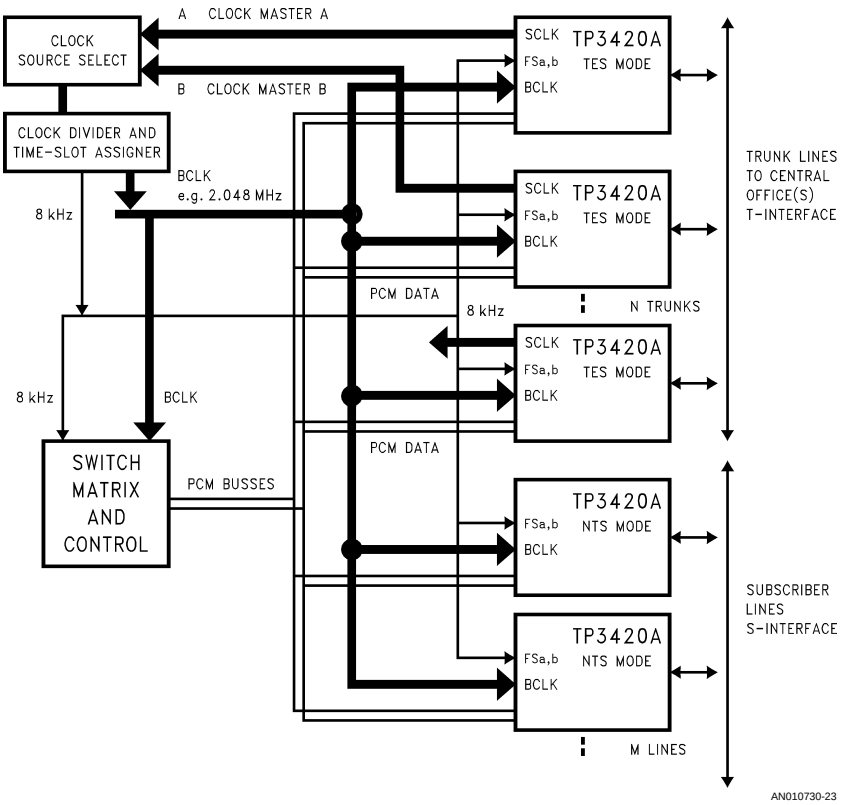
3.5 Slave-Slave Mode and Elastic Buffers (TP3420A)

When SID is used in TE mode (TES), it is a timing slave to the network, but the digital interface is also in a slave mode, i.e., Fs and BCLK are inputs and is referred to as "slave-slave" mode. A typical slave-slave application is on the network side of an NT-2, or PBX, at the T interface. Not only does this application require the device to cope with arbitrary phase relationships between the I.430 receive frame and the 8 kHz Fs, but also the possibility of "slips" arises. A slip may occur when the frame phase relationships across the device are not fixed, but jitter sufficiently to cause loss of data and frame sync. At frequencies below 10 Hz this form of jitter is called "wander", and CCITT specification Q.502 shows that wander up to 18 µs peak-peak may arise over a 24 Hour period. An elastic store is included in both the transmit and receive paths of the SID for two reasons:

1. To allow complete flexibility for any time-slot to be assigned at the digital interface, regardless of the phase of the receive I.430 frame. In addition, separate FS inputs for transmit and receive allow them to have independent frame and time slot alignments.
2. To absorb wander between the frame phases across the device up to the limits specified in Q.502.

Each elastic store, in conjunction with some control circuitry, is used to adjust the output timing requirements gradually for error free transmission performance. *Figure 16* shows the general mechanism supported by the SID in either direction which utilizes a serial-to-parallel converter, a buffer and a parallel-to-serial converter. The incoming data (2B + D) is transferred into the register as each word is accumulated in the serial-to-parallel converter. Some time later, data in the buffer is transferred to the output parallel-to-serial converter as a complete word is shifted out. The wander detector circuit controls the transfers to the parallel-to-serial converter in such a way as to absorb wander by varying delays through the elastic store. The SID is designed to absorb the CCITT wander specified over 24 hours, which can be up to 18 µs peak-to-peak.

TP3420A will optionally generate a Slip interrupt to indicate clock slip condition in the Tx or Rx directions. Please see TP3420 Data Sheet for more information.



Note 10: FSa, b to each device are offset to indicate the time slot to be used.
Note 11: SCLK frequency is set by selecting DIF format (e.g., Format 1, SCLK = 2.048 MHz).

FIGURE 15. TP3420A Showing NT-2 Synchronization

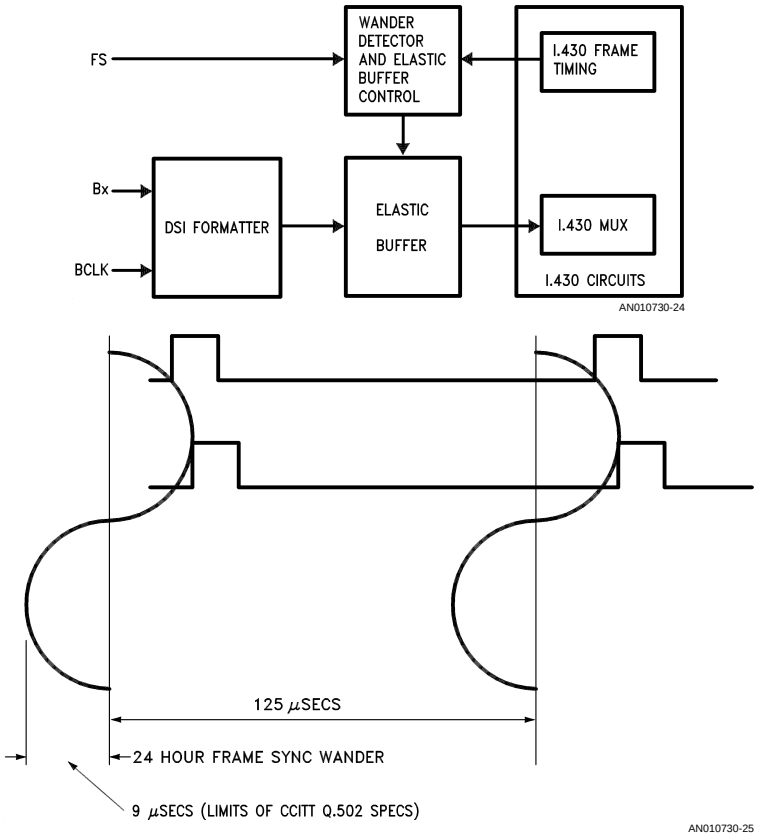


FIGURE 16. TP3420A Slave-Slave Mode and Elastic Buffer (TX Side)

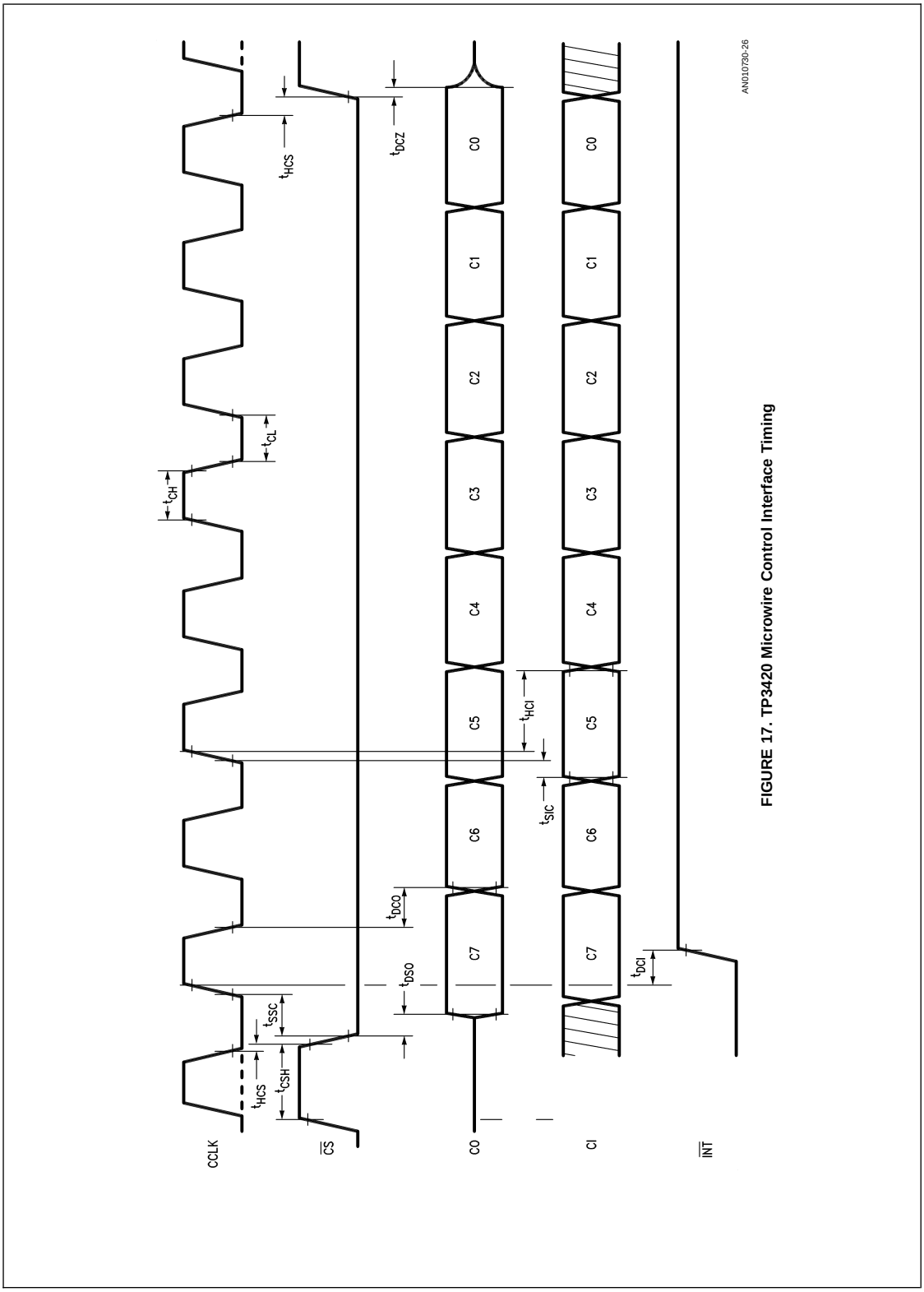


FIGURE 17. TP3420 Microwire Control Interface Timing

4.0 DIGITAL CONTROL INTERFACE

The digital control interface for the TP3420A SID is compatible with National's industry standard MICROWIRE/PLUS™ interface. This approach provides easy integration into already existing microcontroller applications.

4.1 The MICROWIRE Bus

The MICROWIRE compatible interface on the TP3420A is provided for microprocessor control of various functions in the device. MICROWIRE is used for slow speed control and status data, while all the real time user data in B and D-channels is routed via the DSI so that speed of response to interrupts is not a critical issue.

In the MICROWIRE control interface implementation in the TP3420A, with reference to the control interface timing shown in *Figure 17*, the following actions take place:

Data transfers consist of a single byte shifted into the control register of SID via the CI pin while a single byte is shifted out from the status register of SID via the CO pin.

$\overline{CS}$ is to be pulled low for 8 clock cycles of CCLK.

Data waiting to be received into CI is clocked on rising edge of CLK.

Data waiting to be transmitted out of CO is clocked out on the falling edge of CCLK.

$\overline{INT}$ goes low to alert the microprocessor when changes in the status register occur. $\overline{INT}$ returns to the high impedance state on the rising edge of CCLK after $\overline{CS}$ goes low.

The TP3420A will revert to the ALTERNATE MICROWIRE mode to communicate with the Motorola SCP master devices. Please see TP3420A Data Sheet and AN-931 (Interconnecting NSC TP3420A SID to Motorola SCP/HDLC Devices) for more details.

Note: When reading an interrupt from SID, a NOP (hex FF) must be loaded into CI.

4.2 TP3420A SID to HPC16400E MICROWIRE Connection

The MICROWIRE/PLUS interface on HPC16400E has an 8-bit parallel loaded, serial shift register using SI as the input and SO as output. SK is the clock for the serial shift register (SIO). SK clock can be provided from an internal HPC timer or from an external source, and the internal clock is programmable by the DIVBY register. A DONE flag indicates when the 8-bit data shift is completed.

The HPC16400E should be configured in the Master mode for operations in this case. A control bit in the IRCD register determines whether the HPC16400E is in master or slave mode for MICROWIRE/PLUS applications. *Figure 14* illustrates the use of HPC™ MICROWIRE/PLUS in controlling the TP3420A MICROWIRE interface.

4.3 TP3420A SID COMMAND and STATUS Bytes

The control commands and status indication functions supported by the TP3420A allow it to be flexibly used in various system applications with relative ease. The command controls are in distinct groups of functions, and in most of these, only one function my be active from each group at a time. Listed below are some various control functions and status indication functions. Please refer to the TP3420A SID Data Sheet for additional commands and indications.

Activation/Deactivation

Command	Status
PDN	LSD
PUP	AP
AR	EI
DR	DI
FI2	
MMA	

Device Modes

Command	Status
NTA	
NTF	
TEM	
TES	

Digital Interface Formats

Command	Status
DIF1	
DIF2	
DIF3	
DIF4	

B1/B2 Channel Control

Command	Status
B1E	
B2E	
B1D	
B2D	
BDIR	
BEX	

D-Channel Access

Command	Status
DREQ1	CON
DREQ2	EOM

End of Message Interrupt

Command	Status
EIE	
EID	

Multiframe

Command	Status
MFT	MFR
MIE	
MID	

Loopback Tests

Command	Status
LBS	
LBL1	
LBL2	
LBB1	
LBB2	
CAL	

4.4 TP3420A Receive Timing Recovery

The TP3420A has two receive clock timing options available in its system implementations as shown in the conceptual diagram of *Figure 18*.

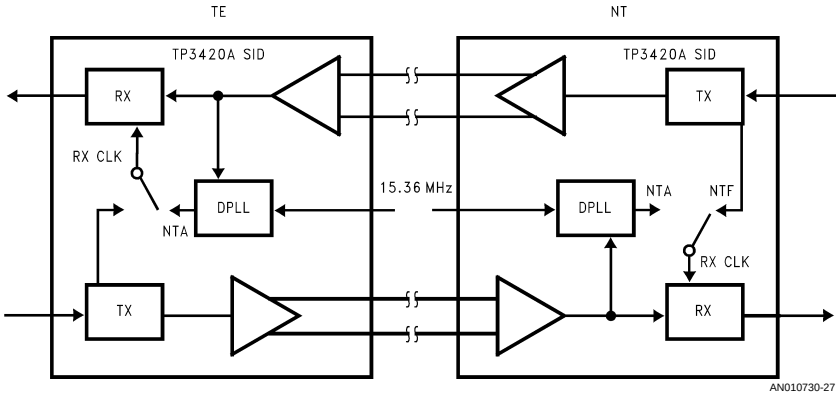
In adaptive timing mode, the DPLL is locked to timing in the received bit stream. This mode is used in TE applications for both point-to-point, short and extended passive bus configurations, whereas in NT mode this is used for point-to-point and extended passive bus configurations only.

For application in the NT of a short passive bus only, the multiple TE's with different round trip delays cause wide variations in the zero crossings so that a DPLL cannot generate a clean clock reliably. Therefore the receive sampling DPLL is bypassed in this mode by selecting the NTF command. In Fixed timing mode, the DPLL is locked to TXCLK and phased at 4 µs with respect to the leading edge of the derived clock. Also, in the fixed timing mode, the equalizer is disabled.

4.5 TP3420A Line Signal Detect (LSD) and Wake-Up Signal for µP

The Line Signal Detect circuit in the SID is active when the device is in the power down state. Upon detecting a valid signal, the $\overline{\text{LSD}}$ pin on the device is pulled low from its normally high impedance state, and also the $\overline{\text{LSD}}$ bit in the Status Register is set. The $\overline{\text{LSD}}$ pin may be used for waking up a local microprocessor from a low power idle mode and subsequently powering up SID itself. The $\overline{\text{LSD}}$ pin goes into the high impedance state upon powering up (PUP) the SID and the LSD circuit in the device is disabled in powered-up mode.

Figure 19 shows a simple concept of using the $\overline{\text{LSD}}$ pin on the TP3420A SID in waking up HPC16400E, the local microcontroller. The LSD signal is tied to the NMI pin of the HPC16400E. When a remote activation request is sensed by the SID, it pulls the $\overline{\text{LSD}}$ pin low and the NMI pin detects the inverted LSD signal to wake-up the HPC16400E. The $\overline{\text{INT}}$ signal on the TP3420A SID may also be used for these wake-up procedures because the LSD bit in the status register may be read upon the $\overline{\text{INT}}$ signal going low.



TP3420A SID has 2 RX CLK Timing Options:

1. DPLL Adaptive timing, locked to RX data
   - Used in TE mode always
   - Used in NT mode for point-point only
2. Fixed Timing, locked to TX CLK and phased at 4 µs after TX edges
   - Used in NT mode for passive bus only

The NT/TE bits select both the timing mode and the state machines for activation control.

FIGURE 18. TP3420A Receive Timing Circuitry

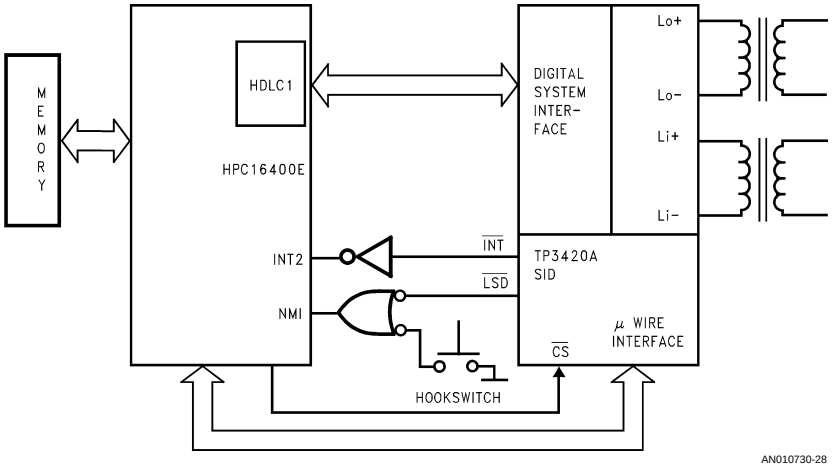


FIGURE 19. TP3420A SID, Line Signal Detect Circuit Connection to HPC16400E

5.0 ACTIVATION AND DEACTIVATION USING TP3420A SID AND HPC16400E

TP3420A SID and HPC16400E combination makes an ideal system solution for ISDN terminals (TE's). When this hardware combination is used in a system, implementing CCITT recommended activation and deactivation procedures is simplified considerably. Assuming both the TE and NT ends of the system employ the TP3420A and HPC16400E combination, the activation/deactivation procedures for specific cases are explained below.

5.1 S Interface Loop Activation Initiated from the TE End

Figure 20 illustrates various commands and status indications and the resultant INFO signals for a successful activation of the S interface for the case when a TE has initiated the activation procedure. This discussion, however, does not indicate the timers that are required in an activation procedure (see Section 6). The following sequence of events must take place for the TE initiated activation of the S interface:

TE SIDE: TP3420A SID is first powered up and then the AR command is sent. This forces INFO1 pattern onto the S interface towards the NT.

NT SIDE: The TP3420A on the NT side senses the INFO1, and issues an LSD interrupt to the local controller. On powering up the SID, the AP byte in the status register is set and the local HPC must respond by sending the AR command. This causes the NT SID to send INFO2 frames on the S interface.

The TE SID, upon recognition of INFO2 frames, sends INFO3 frames on the S interface.

NT SIDE: Upon recognizing INFO3 frames, the NT SID issues an AI interrupt to the processor to indicate pending activation. Now the HPC repeats the AR command in the TP3420A control register and SID sends INFO4 frames on the S interface.

TE SIDE: The TE SID now receives INFO4 frames and issues an AI indication to the local processor.

NT SIDE: The SID issues an AI indication to the local processor.

At this point the S interface is activated.

5.2 S Interface Loop Activation Initiated from the NT End

Figure 21 illustrates various commands and status indications and resultant INFO signals for a successful activation of the S interface for the case when a NT has initiated activation procedure. This discussion however does not indicate the timers that are required in an activation procedure (see Section 6). The following sequence of events must take place for the NT initiated activation of the S interface:

NT SIDE: TP3420A SID is first powered up and then the AR byte in the command register is sent to initiate the S interface activation procedure. This causes the NT SID to send INFO2 frames on the S interface.

TE SIDE: Upon detecting the received signals across the S interface, the TE SID issues an interrupt to the local HPC indicating LSD. The HPC16400E powers up the TP3420A, which then detects valid INFO2 frames and issues AP status indication to the HPC16400E. HP16400E responds to this by issuing an AR command, causing the TP3420A SID to send INFO3 frames on the S interface.

NT SIDE: Upon detecting the INFO3 pattern on the S interface, the NT SID alerts the local processor by setting the AP interrupt. The NT side processor responds by issuing an AR command, causing the NT SID to send INFO4 frames on the S interface. Also, at this time SID indicates a successful activation of the S interface by issuing an AI status to the local HPC16400E.

TE SIDE: The TE SID, upon recognizing the INFO4 frames, indicates to the local HPC the state of successful activation via the AI interrupt.

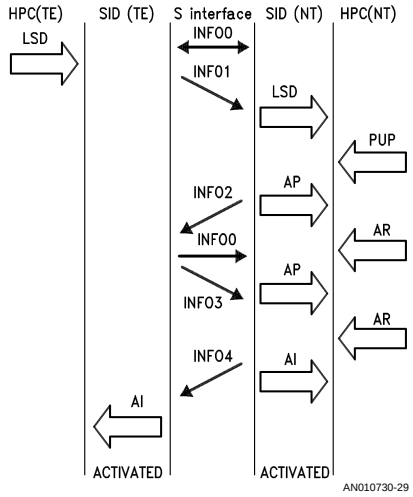


FIGURE 20. Activation Initiated by TE

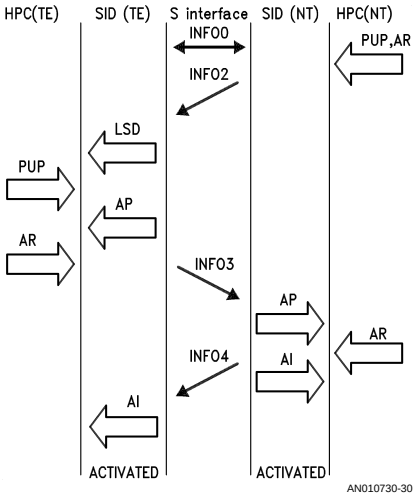


FIGURE 21. Activation Initiated by NT

5.3 S Interface Loop Deactivation Initiated from the NT Side

An activated S interface may be deactivated by generating a DR command in the NT as shown in *Figure 22*. This will force the transmitter of the TP3420A to send INFO0 on the line. The SID in the TE side of the loop detects INFO0 and supplies DI status to the local management entity and also forces INFO0 on its transmitter output. The SID on the NT side will detect the INFO0 and informs the local management entity via DI status. The local controllers on both TE and NT may optionally power down the SID to save power.

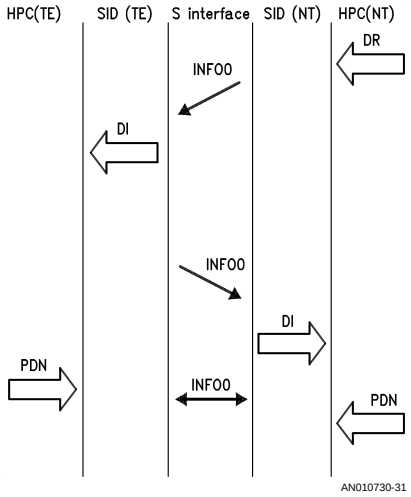


FIGURE 22. Deactivation Initiated by NT

5.4 D-Channel Request and Flow Control (TP3420A)

On the S interface, no TE can use a B channel until it is assigned by the network via the D channel. Therefore there is never a contention problem in a B channel. The D channel, however, carries multiple logical links to and from multiple physical end points (TE's). Therefore packets from different TE's may contend for the use of the D channel towards the network. This multiple access contention is resolved on the S interface by making use of the layer 2 HDLC framing rules (*Figure 23*). TP3420A implements the D channel access control via a collision detection mechanism as described in I.430 Section 6.1 for both TE and NT modes (*Figure 24*).

D channel flow control refers to the way the µP transfers a layer 2 frame or packet to the SID transmit buffer, and from there onto the S interface in a terminal. When the layer 2 wants to transmit a packet, it does not know if another TE is already occupying the D channel, since all D channel monitoring and contention resolution is done by the SID. To transmit its packet, the following sequence of events takes place:

the HDLC controller primes its transmit buffer, ready to send byte 1;

the µP sends a DREQ (D channel request) over MICROWIRE to the TP3420A DREQ messages must also indicate if the pending packet is high priority for signaling (use DREQ1) or low priority for other types of data (use DREQ2).

SID starts pulsing DENx to the HDLC; DENx is gated with the BCLK in the HPC16400E, so 2 D channel bits are

clocked from the HDLC into SID's transmit buffer every 125 µs across the DSI. No D channel bits are transmitted on the S interface yet;

SID senses when the opening flag (01111110) from the HPC is in its buffer. It then stops pulsing DENx.

SID now tests to see if the D-channel towards the NT is in use by another TE, by checking the number of consecutive 1's counted in the D echo channel. When the access algorithm allows, SID starts transmitting D-channel bits from its buffer, beginning with the opening flag.

The SID also now restarts pulsing DENx to fetch further D-channel bits from the HDLC to the SID transmit buffer, always 2 bits per 125 µs frame.

D-channel data now flows from the HDLC through SID onto the S interface until either:

SID detects that it has lost a collision with another TE, so it stops pulsing DENx, transmits 1's in the following D bit positions on the S interface, and interrupts the µP with a CON message;

or the SID detects the closing flag passing through onto the S interface, forces 1's into the D-channel after the closing flag, stops pulsing DENx and sends an EOM interrupt to the µP.

Note that the µP cannot follow immediately with another packet because the successful TE must now decrement its priority and check that no other TE starts using the D-channel (the SID does this automatically). Thus TE's waiting to send signaling packets all succeed in order first, and data packets are only sent when no TE has a signaling packet pending.

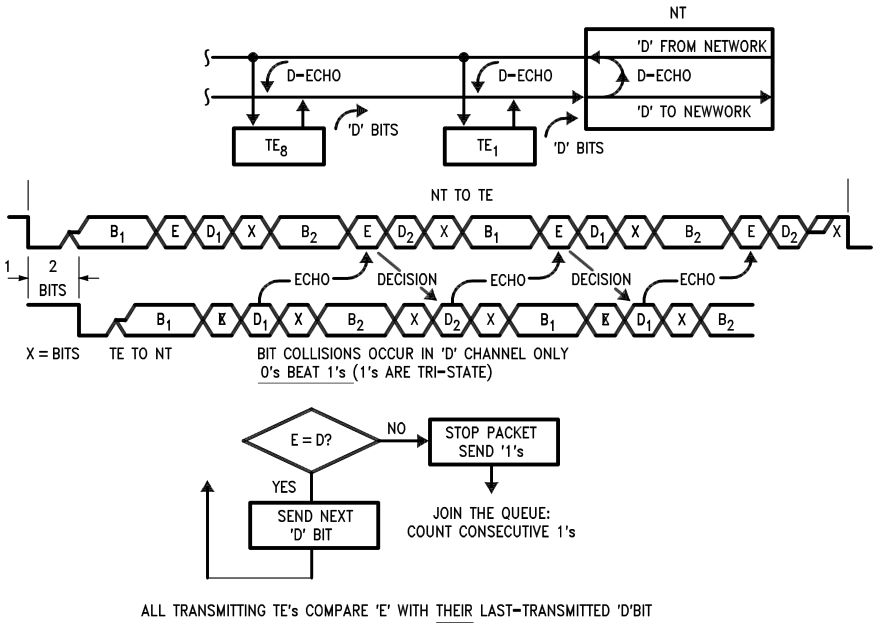


FIGURE 23. D-Channel/Access Control

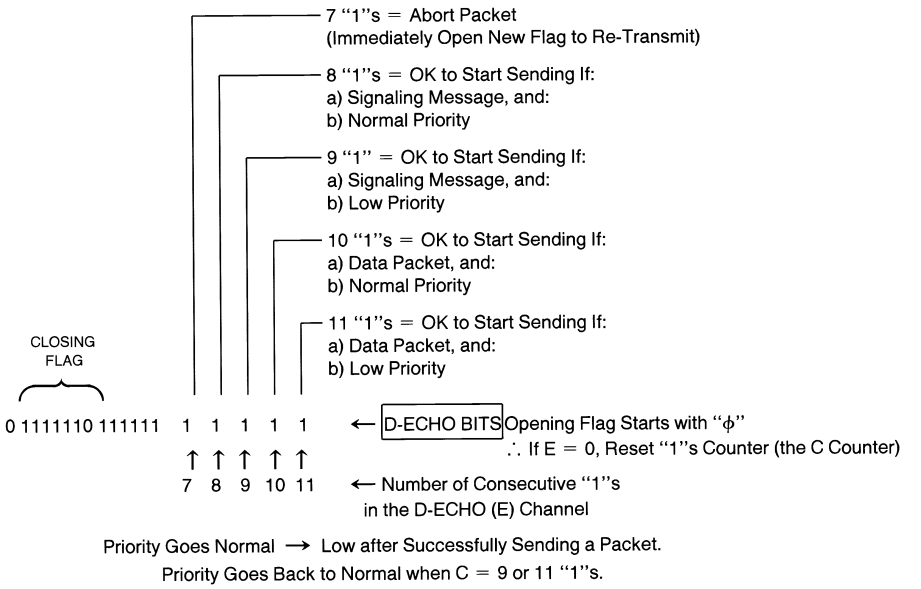


FIGURE 24. D-Channel Flow Control Via Priority Counting

5.5 Software Driver Considerations for the TP3420A

The following paragraphs discuss the software driver implementation for the TP3420A in both NT mode and TE mode. The software driver functions include Activation/Deactivation Procedure, D-Channel Access, and Multiframe Channel Data Access.

"S" Loop Activation and Deactivation. The software driver guides the SID through the activation process to suit a variety of applications. These applications could be for a Terminal Equipment, and NT1, a Linecard, a trunk card or a combination of above. The SID handles all the critical activation functions, and the software needs to simply respond to status change interrupts with activation control commands in collaboration with maintenance times appropriate for the application.

SID Command Status Servicing. The TP3420A is controlled by a local microprocessor via the MICROWIRE port. A TP3465 can be used to convert the parallel data from a micro-processor bus to the MICROWIRE serial format for up to 8 TP3420A devices if that micro-processor does not support such compatible serial interface (see TP3465 data sheet for this application). The microprocessor sends one-byte commands to the SID via the CI pin. At the same time, the SID sends a one-byte status back to the microprocessor via the CO pin. A returned byte of 00 indicates that the SID status has not changed. Otherwise, it returns the updated status.

The SID requests an interrupt service from the microprocessor by pulling the INT pin low. The microprocessor can access the changed status in the SID by sending NOP command (FFHex). In some applications, interrupt handling may not be available, then a periodic polling method for the SID status (by sending a NOP command) can also be implemented. It is possible that while the software driver is sending a normal command to SID, a SID interrupt occurs (but is ignored because it may have been masked off temporarily). In this case, the SID will send the updated status byte in exchange for the Command it receives (and the INT condition by pulling the pin back to tri-state). The software driver must always look at the received status byte and if it is not "00" hex it may decide to take appropriate action.

D-Channel Access. The layer 2 (HDLC) driver communicates with the layer 1 driver when D-Channel packets are to be transmitted in the TE mode by means of the DREQ1 (Signaling packet) and DREQ2 (Data packet) commands. The EOM or CON status must be communicated to the layer 2 for either successful or failed transfer of the packet. In the NT mode the D-Channel packets are transferred to SID without interacting with a layer 1 driver. In all modes, the receive D-Channel packets are passed straight to the layer 2 driver without interaction with the layer 1 driver.

Multiframe Channel Date. Multiframe maintenance channel received data interrupt (MFRxxxx) and transmit data command (MTFxxxx) are transferred directly to the Management Entity task to process, and take appropriate action.

6.0 TERMINAL EQUIPMENT (TE) SOFTWARE DRIVER CONSIDERATIONS

Topics are covered as the followings:

- TE F States
- The I.430 Activation/Deactivation Requirements for TE
- Suggested Flowchart to Implement Activation/ Deactivation Procedure for NT

- TP3420A Internal State Machine

6.1 TE F States

CCITT defines states that a TE would go through during the process of Activation and Deactivation on the S Interface. These are known as the F states. The software drivers recommended for the TP3420A implement additional internal states as described below:

F1: Power supply is turned off (TE not plugged into the power source).

F2: The power supply is ON, however, the receiver has not yet processed the signal received (TE Connected).

F3: Deactivated state.

F4: The activation of layer 1 was initiated by the TE (INFO1); The TE waits for an INFO2 (Awaiting Signal).

F5: Once the signal is received, the TE stops transmitting INFO1 and processes the receive signal (INFO2 or INFO4) Synchronizing.

F6: The TE recognized receipt of an INFO2 and waits for INFO4 (Synchronized).

F7: Activated State of the TE (Activated).

F8: The TE lost the frame synchronization and is trying to resynchronize itself (Lost Framing).

Additional States for SID:

INITIALIZE: TP3420 SID initialization.

POWER DOWN: TP3420A SID in Power Down mode. In this mode, the SID will detect the present of a signal on the line, but not be able to identify it. This state is also called state F2.1 in this document.

6.2 I.430 Activation/Deactivation Requirements for TE

The Activation/Deactivation procedure for TE is defined in the I.430 document. It is summarized in a Finite State Matrix Table. A modified version of this is shown in *Table 1* where the internal commands/states of the TP3420A are superimposed in the table where appropriate to relate to the I.430 states and primitives. They are located in the lower part of the boxes. The TP3420A commands and status have the prefix “SID-” after which the SID command is enclosed in a pair of brackets to distinguish it from its returned status (not enclosed by brackets). For example, SID-[AR] is the TP3420A Activation Request command whereas SID-LSD in the Signal Line Detection interrupt. The SID returned status and the applied commands should occur in such the writing order. In addition, there are a few timers associated with this table, and are described in the footnotes below the table.

TABLE 6. I.430 Activation/Deactivation Layer 1 Finite State Matrix for TEs Powered from Power Source 1 and 2

Event	TP3420A Status Indication	SID-DI (PUP State)					SID-AP	SID-AI	SID-EI
	State Name	Inactive	Sensing	Deactivated	Awaiting Signal	Identifying Input	Synchronized	Activated	Lost Framing
	State Number	F1	F2	F3	F4 (Note 4)	F5	F6	F7	F8
	INFO Sent	INFO0	INFO0	INFO0	INFO1	INFO0	INFO3	INFO3	INFO0
Power on and Detection of Power Source S (Notes 1, 2)		F2	—	—	—	—	—	—	—
Disappearance of Power Source S (Notes 1, 2)		—	F1	MPH-II(d), F1	MPH-II(d), MPH-DI, PH-DI, F1	MPH-II(d), MPH-DI, PH-DI, F1	MPH-II(d), MPH-DI, PH-DI, F1	MPH-II(d), MPH-DI, PH-DI, F1	MPH-II(d), MPH-DI, PH-DI, F1
PH-Act Request		/	|	ST:T3; F4 *SID-[AR]*	|	|	—	|	—
Expiry T3 (Note 7)		/	/	—	MPH-DI, PH-DI, F3 *SID-[DR], SID-DI*	MPH-DI, PH-DI, F3 *SID-[DR], SID-DI*	MPH-DI, PH-DI, F3(Note 8) *SID-[SR], SID-DI*	/	MPH-DI, PH-DI, F3
Receiving INFO0 (Notes 5, 6)		/	MPH-II(c), F3 *SID-[PUP]*	—	—	—	MPH-DI, PH-DI, F3 *SID-DI*	MPH-DI, PH-DI, F3 *SID-DI*	MPH-DI, PH-DI, MPH-EI2, F3 *SID-DI*
Receiving Any Signal (Note 3)		/	—	—	F5	—	/	/	—
Receiving INFO 2		/	MPH-II(c), F6 *SID-LSD, SID-[PUP], SID-AP, SID-[AR]*	F6 *SID-AP, SID-[AR]*	F6 (Note 4)	F6	—	MPH-EI1, F6 *SID-AP*	MPH-EI2, F6 *SID-AP*
Receiving INFO 4		/	MPH-II(c), PH-AI, MPH-AI, F7 *SID-LSD, SID-[PUP], SID-AP, SID-[AR], SID-AI*	PH-AI, MPH-AI, S/R T3, F7 *SID-AP, SID-[AR], SID-AI*	PH-AI, MPH-AI, S/R T3, F7 (Note 4) *SID-AI*	PH-AI, MPH-AI, S/R T3, F7 *SID-AI*	PH-AI, MPH-EI2, S/R T3, F7 *SID-AI*	—	PH-AI, MPH-AI, MPH-EI2, S/R T3, F7 *SID-AI*
Lost Framing		/	/	/	/	/	MPH-EI1, F8 *SID-EI*	MPH-EI1, F8 SID-EI	—

NOTATIONS:

"SID-[command]"	8-bit command sent to the TP3420A. These command can be found in the TP3420A Data Sheet
"SID-interrupt"	Internal interrupt of the TP3420A. They can be found in the TP3420A Data Sheet.
"—"	No change, no action
"|"	Impossible by the definition of layer-1 service
"/"	Impossible situation
"a,b,Fn"	Issue primitives "a" and the go to state "Fn"
"PH-AI"	Primitive PH-Activation Indication
"PH-DI"	Primitive PH-Deactivation Indication
"MPH-AI"	Primitive MPH-Activation Indication
"MPH-DI"	Primitive MPH-Deactivation Indication
"MPH-EI1"	Primitive MPH-Error Indication reporting error
"MPH-EI2"	Primitive MPH-Error Indication reporting recovery from error
"MPH-II(c)"	Primitive MPH-Information Indication (connected)
"MPH-II(d)"	Primitive MPH-Information Indication (disconnected)
"ST.T3"	Start time T3

Primitives are signals in a conceptual queue and will be cleared on recognition, while the INFO signals are continuous signals that are available all the time

Note 1: The term "power" could be the full operational power or backup power. Backup power is defined such that it is enough to hold the TEI value in memory and maintain the capability of receiving and transmitting lay-2 frames associated with TEI procedures.

Note 2: The procedures described in this table require the provision of power source 1 and power source 2 to enable their complete operation. A TE that determines it is connected to an NT not providing power source 1 or 2 should default to the procedures described in Table C-1/I.430.

Note 3: This event reflects the case where a signal is received and the TE has not (yet) determined whether it is INFO2 or INFO4.

Note 4: If INFO2 or INFO4 is not recognized within 5 ms after the appearance of a signal, TE shall go to F5. TO assure that a TE will go to state F5 when receiving a signal to which it can not synchronize, operation of TEs should be verified where the received signal is any bit pattern (containing at least three ZEROs in each frame interval) to which TEs conforming to 7.3.1.2 are not able to synchronize.

Note 5: INFO0 shall not be detected until at least 48 continuous binary ONEs have been received, and the TE shall perform the actions specified in this table. For conformance test purposes, when in the states F6 and F7 with a sinusodial signal having a voltage of 100 mV peak-to-peak superimposed on the received signal, the TE shall react to INFO0 by transmitting INFO0 within a period of time 250 µs to 25 ms. It is recognized that the action in states F2 and F8 is the passing of primitives and that this can not be observed or verified at the interface. (Note: A provision for the immediate reaction to INFO0 following the reciept of 48 continuous ONEs may cause the release of ongoing communications in response to spurious interface signal interruptions. A persistence check should be considered to minimized such a possibility, but the total reaction time shall not exceed 25 ms).

Note 6: To avoid disruption of on-going communication caused by spurious effects, a timer may be started when leaving the state F7 or F8 upon reception of INFO0. The corresponding PH-DI will be delivered to layer 2 only if layer 1 does not re-enter state F7 before expiry of this timer. The value of this timer may be in the range of 500 ms to 10000 ms.

Note 7: Timer 3 (T3) is a supervisory timer which has to take into account for the overall time to activate. This time includes the time it takes to activate both the ET-NT and the NT-TE portion of the customer access.

Note 8: Terminal may momentarily enter state F3 at this point and return to state F6 if INFO2 is still being received (the term "momentarily" means up to a maximum of 5 frames.

6.3 Suggested Software Flowchart to Implement Activation/Deactivation Procedure for TE

The layer 1 Task software can be divided in 4 parts: Initialization subroutine to bring up the SID in the desired ready state; the Interrupt Service Subroutine to response to interrupts issued by the SID, read the status of the SID and then set appropriate software flags; the Main ( ) Subroutine to check the status of these flags to control the state flow of the SID so as to adhere to the I.430 Layer-1 Activation/Deactivation Requirements; and the Local Activation Subroutine to detect a hook switch state, or a Activation Request from the upper layers to start a local activation. A delay of 2 ms is recommended after the device is powered up by the PUP command. Doing this allows the SID internal circuitry to have enough time to settle down.

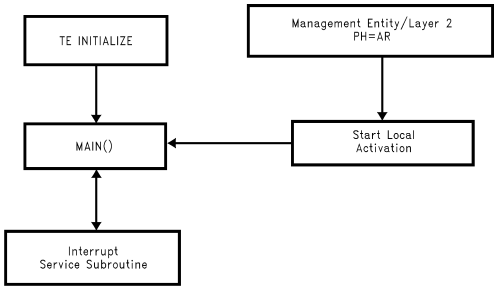


FIGURE 25. Software Driver Flowchart for TE

6.3.1 Initialization Subroutine

This is the first to run in the Layer-1 driver software upon a system power-up or a system reset. It configures the SID to be in either TEM or TES mode. The Digital Interface format must be selected for the intended target system. The TP3420A will enter state F2.1 from state F2 after the application of the PDN command. State F2.1 is the SID Low Power mode. Please consult TP3420A Data Sheet for a complete list of commands.

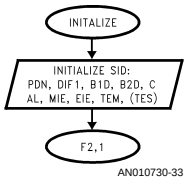


FIGURE 26. Initialization Subroutine for TE

6.3.2 Interrupt Service Subroutine

This is called whenever a SID interrupt occurs. In this subroutine, the local microprocessor sends NOP (FF'H.) to the SID to read its status, and sets the flags accordingly. These flags are Activation Pending (AP), Deactivation Indication (DI), Activation Indications (AI), Error Indication (EI).

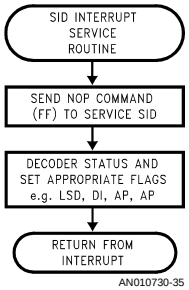


FIGURE 27. Interrupt Service Subroutine Flowchart for TE

6.3.3 Main( ) Subroutine

This is used to process the flags set by the Interrupt Service Subroutines and performs appropriate actions such as passing primitive indications to the upper layers, or sending commands to the TP3420A as needed to follow the I.430 Activation/Deactivation procedure for TE. The Flowchart for this is shown in *Figure 28.* Loop start-up either from the remote end or the local end is handled in this routine by simply responding to status change interrupts from the SID with appropriate commands back to the SID.

Transient such as lightening surge across the telephone line may cause false triggering of the Line Signal Detect (LSD) interrupt in the SID during the idle period, which would cause unexpected loop activation. Software routines can be developed to filter out such transient triggers. An example of this is described below:

After a wait of 5 ms on the first occurrence of the LSD interrupt, the tLSD timer is activated, and the LSD__ FILTERED flag is set (this flag must be reset on system power-up or system reset condition). These are followed by a PDN command. If this is a true Remote Activation Request from the far-end NT, a second LSD interrupt will occur right after this PDN command. In this case, the set condition of the LSD__FILTERED flag indicates that there is a continuous INFO signal on the line. Otherwise, the expiration of the tLSD timer signifies that this is a false alarm. The value of t_{LSD} timer can be from 5 ms to 10 ms.

There are a few timers associated with the I.430 Activation/ Deactivation Recommendation and are described in the notes below the *Table 1*. Two of these MUST be implemented in the firmware while others are already taken care of in the TP3420A.

1. $t_{SPURIOUS}$ timer (Note 6 of the I.430 *Table 5*): is needed to avoid disruption of an on-going communication caused by spurious effects. This timer is activated upon entering F2 state (Deactivation Indication). Primitive PH-DI will be delivered to layer-2 only upon the expiration of this timer. The value of this timer may vary from 500 ms to 1000 ms.
2. TE Supervisory Timer T3 (Note 7 of the I.430 *Table 5*): Supervisory timer T3 is usually 15 seconds for applications where a TE is connected via an NT-1 to the Central Office over an S Interface loop followed by a U Interface loop.

If this timer expires and if the SID is in state F4 or F5 (indicating that the U-link failed to activate), the local microprocessor must send a DR command to bring the SID to state F3 (Deactivated). However, if the TE is in state F6 (indicating that U-interface is synchronized but is not transparent to data), the SID should remain in state F6 (or is allowed to momentarily go to F3 and return to F6 within 5 frames). This is specified by Note 8 in the I.430 Activation/Deactivation Table. The suggested technique is this: At the expiry of the T3 timer, the local microprocessor can acquire the SID internal state machine status by sending ENST command followed by DISST command, and then decoding the status byte (according to the table given in the TP3420A data sheet). If the status indicates the F6, state do nothing, however, if the state is still F4 or F5, write a DR command to SID to abort the activation attempt.

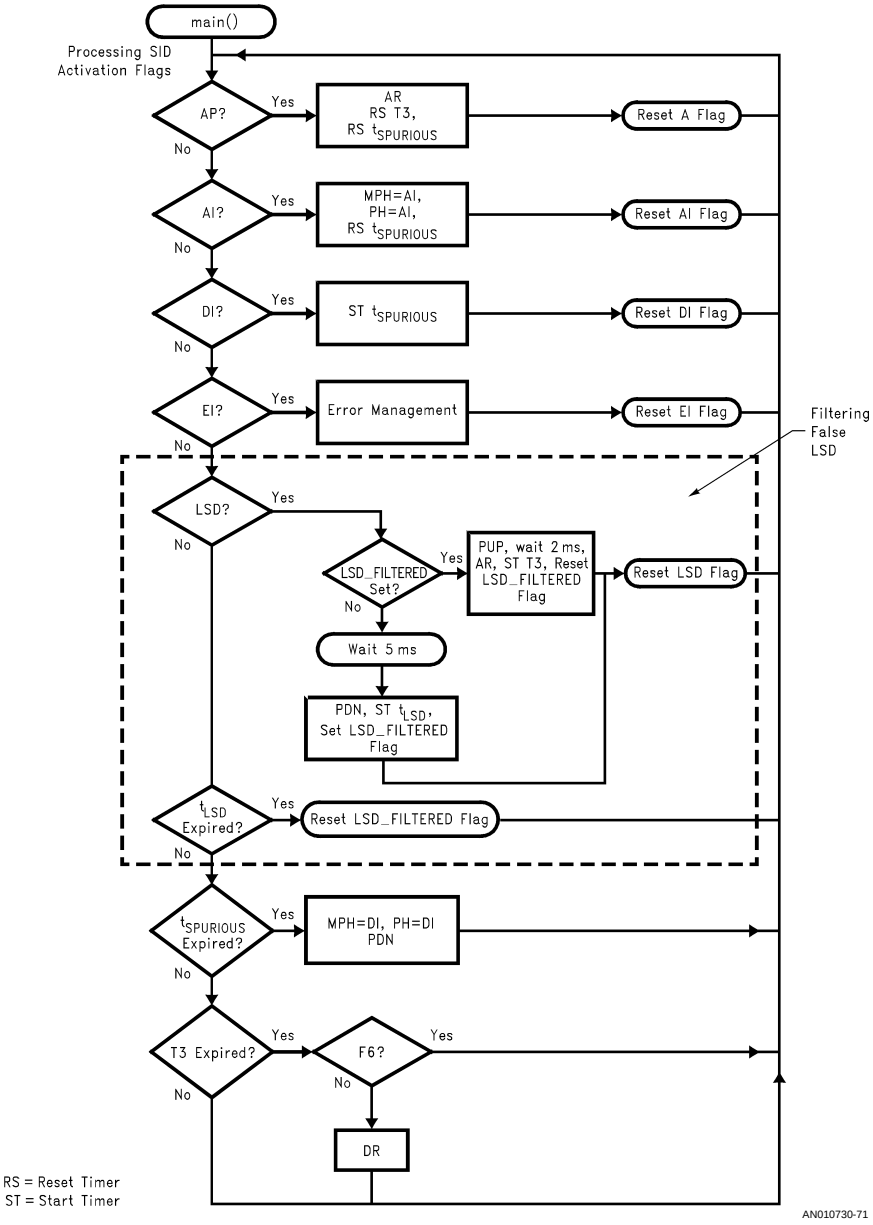


FIGURE 28. Main Task for the Software Driver

6.3.4 Local Activation Subroutine

Management Entity or Layer 2 can request a local activation by issuing a MPH-AR, or PH-AR, while the SID is in state F3 (Deactivated). This assumes the SID has been powered up at least 2 ms so that the internal circuitry has enough time to settle down. The software driver then sends an AR command to bring the SID to state F4 (Awaiting signal), and at the same time, start the timer T3. The SID waits for either INFO2 to bring it to state F6 (Identifying Input) or INFO4 to directly bring it to state F7 (Activated). Suggested actions after T3 expiry are indicated above.

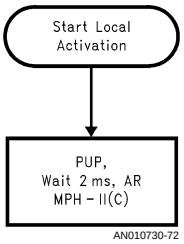


FIGURE 29. Local Activation Subroutine

6.4 TP3420A Internal F State Machine Diagram

Figure 30 is the internal F State Machine in the TP3420A when the device is programmed to be in TEM or TES mode. Each box corresponds to an equivalent of an I.430 F state, F1 to F8. There is an extra internal state, F2.1 not to be found in I.430 F states. This is the Low Power mode.

Most of the state transitions take 250 µs, and are represented by the thin lines. The other three transitions take 2 ms, and represented by the thick lines. A specified stimulus that causes a state jump is written in the transition line before the (/) or by itself. The returned status is written after the slash (/). Not every transition has a returned status.

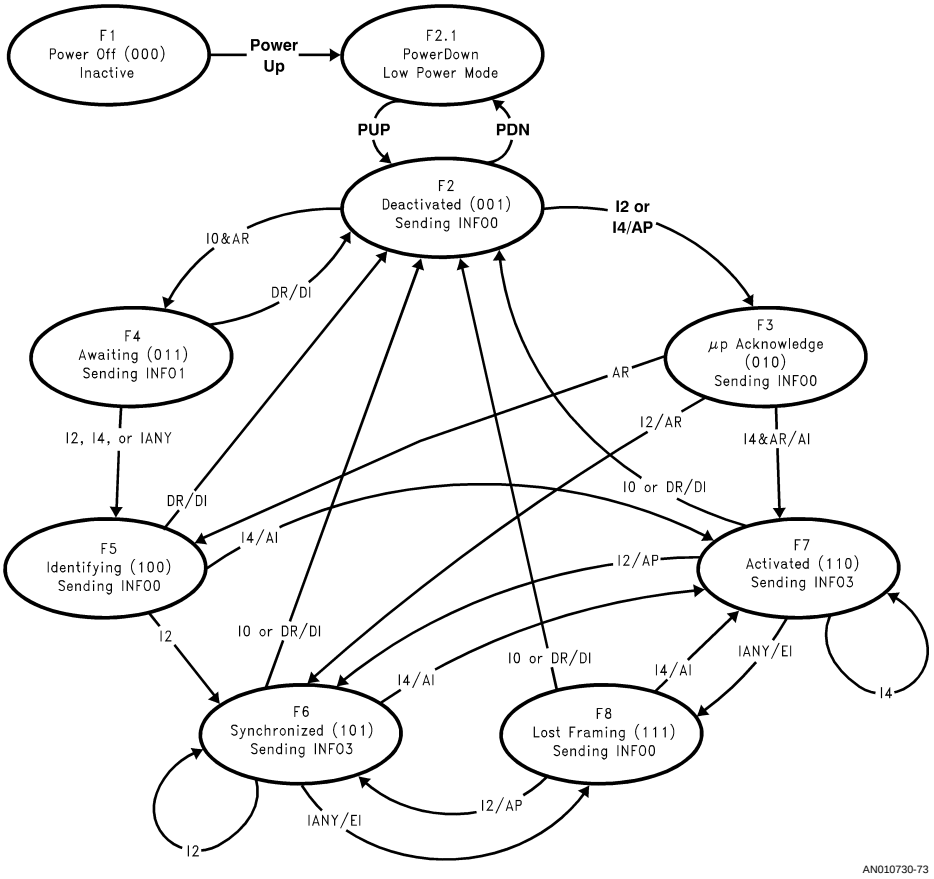


FIGURE 30. Internal F State Machine Diagram

7.0 NETWORK TERMINATION (NT) SOFTWARE DRIVER CONSIDERATIONS

Topics are covered as the following:

- NT G States
- The I.430 Activation/Deactivation Requirements for NT
- Suggested flowchart to implement Activation/ Deactivation procedure for NT
- TP3420A Internal State Machine

7.1 The G States

The G States are defined in CCITT recommendation I.430 as the state that an NT would go through to Activate/ Deactive the S interface loop. The software driver may need additional internal states as described below:

G1: Deactivated condition. Idle state, i.e., layer 1 is not ready to transmit data.

G2: The activation of layer 1 was initiated by TE or NT; the NT is waiting for INFO3 from a TE (Pending Activation).

G3: Active state of NT, (Activated)

G4: When the NT wishes to deactivate, it may wait for a timer to expire before returning to the deactivated state (G1) to prevent unintentional reactivation. I.430 (in Note 2 of NT Activation/Deactivation) also specifies that the value of this timer, namely, T2 can be 0 seconds if the NT is able to unambiguously recognize INFO1. The TP3420A in NT mode satisfies this condition, hence, state G4 is equivalent to state G1.

Additional State for SID:

INITIALIZE: SID initialization for NT mode

POWER DOWN: TP3420A is in Power Down mode. In this mode, the SID will detect the present of a signal on the line, but not be able to identify it.

7.2 I.430 Activation/Deactivation Requirements for NTs

The Activation/Deactivation procedure for NT is defined by the I.430 document. It is summarized in a Finite State Matrix Table. *Table 7* is a modified version where the internal commands/states of the TP3420A are superimposed in the table where appropriate to relate to the I.430 states and primitives. They are located in the lower part of the boxes. The TP3420A commands and status have the prefix “SID-” after which the SID command is enclosed in a pair of brackets to distinguish from its returned status (not enclosed by brackets). For example, SID-[AR] is the TP3420A Activation

Request command whereas SID-LSD is the Signal Line Detection interurpt. The SID returned status and the applied commands should occur in the order indicated. In addition, there are a few timers associated with this table, and are described in the notes below the table.

The TP3420A can uniquely identify an INFO1 signal, hence T2 timer is not needed. This implies that state G4 can be ignored or is replaced with state G1. In this case, a MPH-Deactivate Request would cause a direct transition from state G2 or G3 to state G1.

TABLE 7. Finite State Matrix for NTs to Reflect the Requirements for Layer-1 Activation/Deactivation

Event	State Name	Deactivated	Pending Activation	Active	Pending Deactivation
	State Number	**G1**	**G2**	**G3**	**G4** (Note 13)
	INFO Sent	**INFO0**	**INFO2**	**INFO4**	**INFO0**
PH-Act Request (Note 13)		Start Timer T1 G2 *SID-[PUP], SID-[AR]*	|	|	Start Timer T1 (G2) *SID-[AR]*
MPH-Deact Request (Note 13)		|	Start Timer T2 PH-DI; G4 (Note 10) *SID-[DR], SID-DI*	Start Timer T2 PH-DI; G4 (Note 10) *SID-[DR], SID-DI*	|
Expiry T1 (Note 9)		—	Start Timer T2 PH-DI; G4 (Note 10) *SID-[DR], SID-DI*	/	—
Expiry T2 (Notes 9, 13)		—	—	—	G1
Receiving INFO0 (Note 13)		—	—	MPH-DI, MPH-EI; G2 (Note 11) *SID-EI*	G1
Receiving INFO1		Start Timer T1 G2 *SID-LSD, SID-[PUP], SID-AP, SID-[AR]*	—	/	—
Receiving INFO3		/	Stop Timer T1 PH-AI, MPH-AI; G3 (Note 12) *SID-AP, SID-[AR], SID-AI*	—	—
Lost Framing		/	/	MPH-DI, MPH-EI; 2 (Note 11) *SID-EI*	—

NOTATIONS:

"—"	No state change
"/"	Impossible by the definition of peer to peer physical layer procedures or system internal reasons
"|"	Impossible by the definition of physical layer service
"a,b;Gn"	Issue primitives "a" and "b" then go to state "Gn"
"PH-AI"	Primitive PH-Active Indication
"PH-DI"	Primitive PH-Deactivate Indication
"MPH-AI"	Primitive MPH-Activation Indication
"MPH-DI"	Primitive MPH-Deactivate Indication
"MPH-EI"	Primitive MPH-Error Indication

"SID-[command]" 8-bit command sent to the TP3420A. They can be found in the TP3420A Data Sheet

"SID-interrupt" TP3420A internal interrupt. They can be found in the TP3420A Data Sheet

Note: Primitives are signals in a conceptual queue and will be cleared on recognition, while the INFO signals are continuous signals that are available all the time.

Note 9: Timer 1 (T1) is a supervisory timer that has to take into account the overall time to activate. This time includes the time it takes to activate both the ET-NT and the NT-TE portion of the customer access. ET is the exchange termination.

Note 10: Timer (T2) prevents unintentional reactivation. Its value is greater than 25 ms and smaller than 100 ms. This implies that a TE has to recognize INFO0 and to react on it within 25 ms. If the NT is able to unambiguously recognize INFO1, then the value of timer 2 may be 0, and an MPH-Deactivate Request would cause a direct transition from state G2 or G3 to state G1. It should be noted that unambiguous detection of INFO1 may not be possible in passive bus configurations, considering all possible TE implementations.

Note 11: These notifications (MPH-DI, MPH-EI) need not be transferred to management entity at the NT.

Note 12: As an implementation option, to avoid premature transmission of information (i.e., INFO4), layer 1 may not initiate transmission of INFO4 or send the primitives PH-Activate Indication and MPH-Activate Indication (to layer 2 and management, respectively) until a period of 100 ms has elapsed since the receipt of INFO3. Such delay should be noted in ET if required.

Note 13: INFO0 shall not be detected until at least 48 continuous binary ONEs have been received, and the NT shall perform the actions specified in this table. For conformance test purposes, when in the state G3 with a sinusoidal signal having a voltage of 100 mV peak-to-peak superimposed on the received signal, the NT shall react to INFO0 by transmitting INFO2 after a period of time equal to or greater than 250 µs. It is recognized that the action in state G4 can not be observed or verified at the interface.

7.3 Suggested Software Flowchart to Implement Activation/Deactivation Procedure for NT

The layer 1 Task software can be divided in 4 parts: Initialization subroutine to configure the SID in a desired ready state; the Interrupt Service Subroutine to response to interrupts issued by the SID, read the status of the SID and then set appropriate software flags; the Main( ) Subroutine to check the status of these flags to control the state flow of the SID so as to adhere to the 1.430 Layer-I Activation/Deactivation Requirements; and the Local Activation Subroutine to detect a hook switch state, or a Activation/Deactivation Request from the upper layers to start a local activation. A delay of 2 ms is recommended after the device is powered up by the PUP command. Doing this allows the SID internal circuitry to have enough time to settle down.

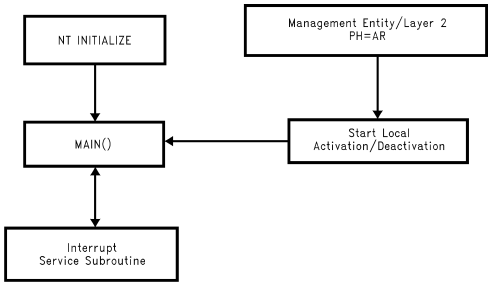


FIGURE 31. Software Driver Flowchart for NT

7.3.1 Initialization Subroutine

This software routine is the first to run in the layer 1 driver software upon a system power-up or a system reset. It configures the SID to be in either NTA or NTF mode. Typically, NTA mode is used for point to point applications and NTF mode is used for passive bus applications where up to 8 TEs can connect to the same S bus. It sets the SID in low power mode by the PDN command. The Digital Interface format must be selected for the intended target system.

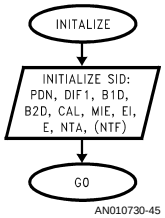


FIGURE 32. Initialization Subroutine for NT

7.3.2 Interrupt Service Subroutine

This is called whenever a SID interrupt occurs. In this subroutine, the local microprocessor sends NOP (FF'H.) to the SID to read its status, and sets the flags accordingly. These flags are Activation Pending (AP), Deactivation Indication (DI), Activation Indications (AI), Error Indication (EI) etc.

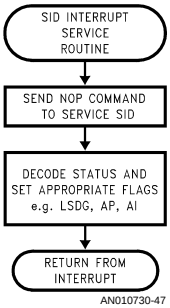


FIGURE 33. Interrupt Service Subroutine for NT

7.3.3 Local Activation/Deactivation Subroutine

Management Entity or Layer 2 can request a Local activation by issuing a MPH-AR, or PH-AR, while the SID is in state F3 (Deactivated). This assumes the SID has been powered up at least 2 ms so that the internal circuitry has enough time to settle down. The software driver then sends an AR command to bring the SID to state G2, at the same time, starts the timer T1, and waits for INFO3. The SID generates AP interrupt once it detects INFO3 from the far end TE. Another AR command sent to the SID will bring it to fully activated state (state G3). If the timer TI is expired during the local activation process, the software driver sends a DR command to the SID to bring it back to state G2. Notice that there is no state G4 involved in this activation process for the reason mentioned above. Otherwise, the timer TI is reset in state G3.

The S bus can only be deactivated by the NT. The software driver simply sends a DR command to perform this task.

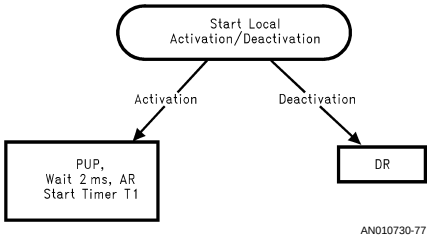


FIGURE 34. Software Driver Flowchart for NT

7.3.4 Main( ) Subroutine

This software module is used to process the flags set by the interrupt Service Routines and performs appropriate actions such as passing primitive indications to the upper layers, or send commands to the TP3420A as needed to follow the I.430 Activation/Deactivation procedure for NT. The Flowchart for this is shown in *Figure 36*. Loop start-up either from the remote end or the local end is handled in this routine by simply responding to status change interrupts from the SID with appropriate commands back to the SID.

Transient noise such as lightening surge across the telephone line may cause false triggering of the Line Signal Detect (LSD) interrupt in the SID during the idle period, which would cause unexpected loop activation. Software routines can be developed to filter out such transient triggers. An example of this is described below:

After a wait of 5 ms on the first occurrence of the LSD interrupt, the tLSD timer is activated, and the LSD — FILTERED flag is set (this flag must be reset on system power-up or system reset condition). These are followed by a PDN command. If this is a true Remote Activation Request from the far-end NT, a second LSD interrupt will occur right after this PDN command. In this case, the set condition of the LSD — FILTERED flag indicates that there is a continuous INFO signal on the line. Otherwise, the expiration of the tLSD timer signifies that this is a false alarm. The value of tLSD timer can be from 5 ms to 10 ms.

There are a few timers associated with the I.430 Activation/Deactivation Recommendation for NT and are described in the notes below the *Table 7*. Two of these MUST be implemented in the firmware while others are already taken care of in the TP3420A.

1. T1 timer (Note 1 of the I.430 *Table 7*): can be as long as 15 seconds for applications where a TE is connected to NT-1 device to the Central Office via a U interface loop. This timer is started after an occurrence of the LSD interrupt, or at the beginning of a local activation procedure. If this timer is expired before the Activation Pending interrupt, the micro-controller should send a Deactivation Request (DR) command followed by a Power Down (PDN) command to bring the SID to the Low Power mode.
2. t_{INFO4} (Note 4 of the I.430 *Table 7*): is used to delay the transmission of INFO4 after the NT reaches Activation Pending state (G2) upon the reception of INFO3 from the TE. This timer is started once the NT reaches state G2. Upon the expiration of this timer, layer-1 driver sends an AR command to bring the SID to state G3. The following AI interrupt indicates that the SID's been sending out INFO4, and Layer-1 now can send PH-AI, MPH-AI to the upper layers. This is to allow the U interface loop to acquire synchronization. Please also see the TP3410 user's manual for additional signal flow diagrams for NTI application. The value of this timer is 100 ms.

7.4 TP3420A Internal G State Machine Diagram

Figure 35 is the internal G State Machine in the TP3420A when the device is programmed to be in NTA or NTF mode. There are 3 I.430 equivalent states, namely G1, G2, and G3, and other intermediate states. Stated G0 is the low power mode. A specified stimulus that causes a state jump is written in the transition line before the slash (/) or by itself. The returned status is written after the slash (/). Not every transition has a returned status.

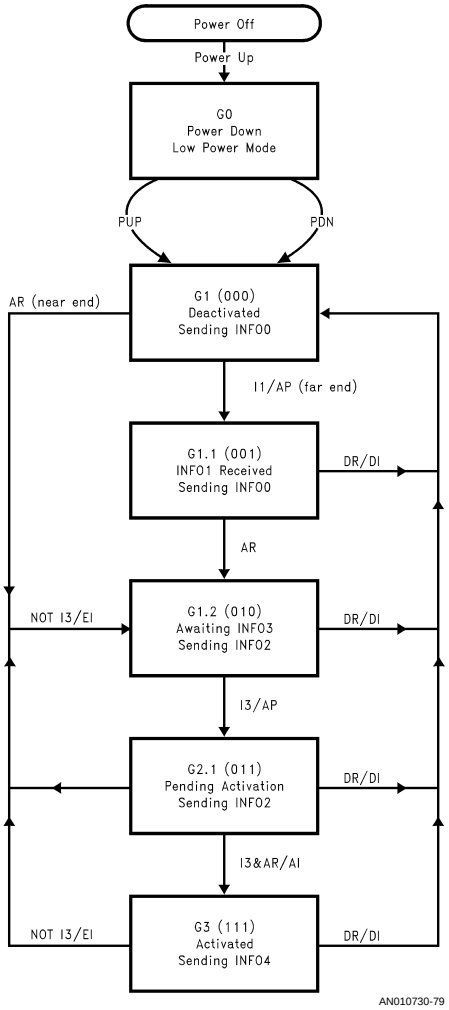


FIGURE 35. Internal G State Machine Diagram

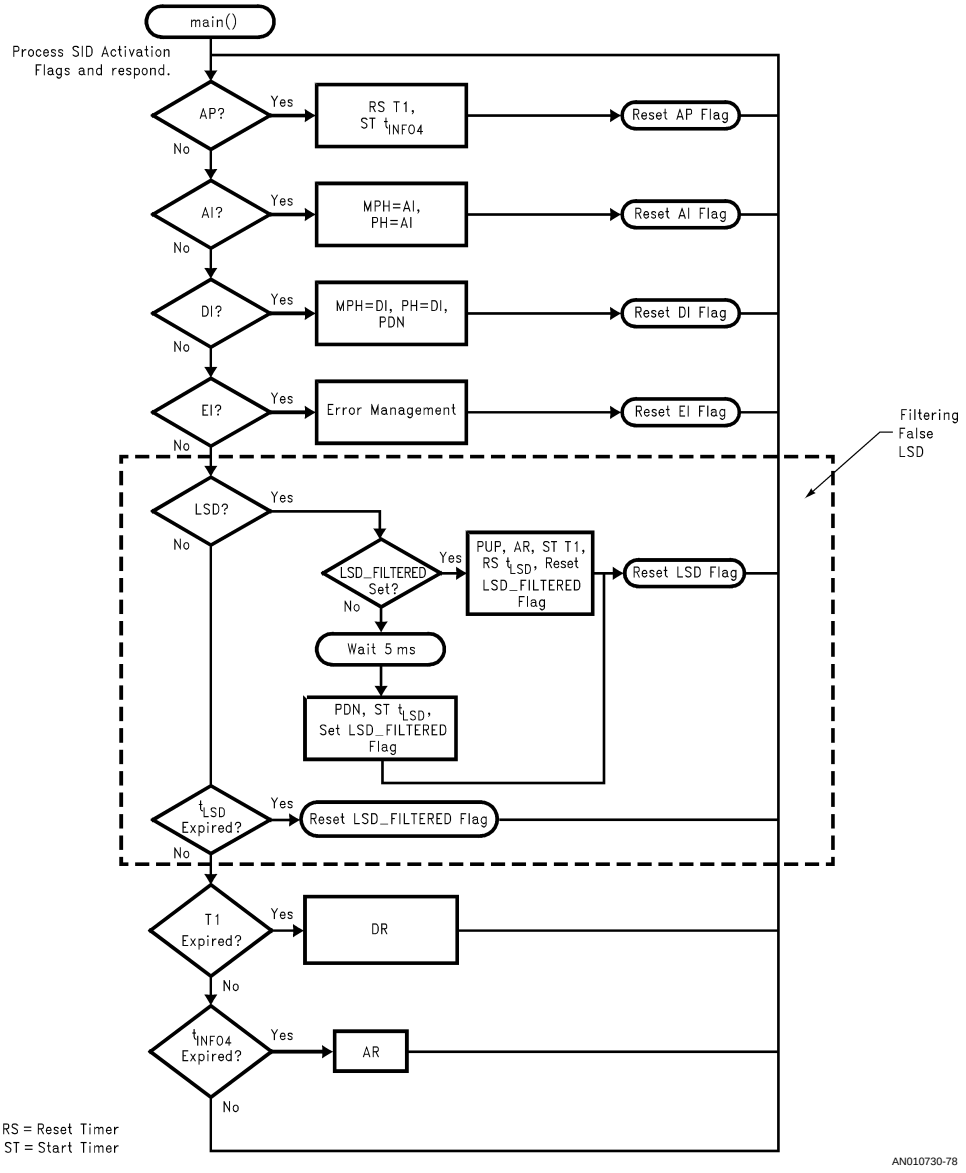


FIGURE 36. Main Task for the Software Driver

8.0 SID TEST LOOPBACK MODES

The TP3420 and TP3421 provide three classes of loopback modes, namely:

Full 2B+D loopback at the system interface (LBS);

Individual B channel loopback at the line interface (LBL1/ LBL2);

Individual B channel loopback at the system interface (LBB1/ LBB2).

These loopbacks may be activated via MICROWIRE commands into TP3420 or Monitor Channel commands in the TP3421. Using the loopback modes provided in the device, various system loopbacks recommended in the CCITT I.430 may be implemented.

In order to use SID loopback modes effectively in implementing the I.430 loopbacks, an explanation of each test loopback mode is in order here. In the explanation below, we refer to the B1, B2 and D **Tx** and **Rx** slots and B1, B2 and D slots as shown in *Figure 37*.

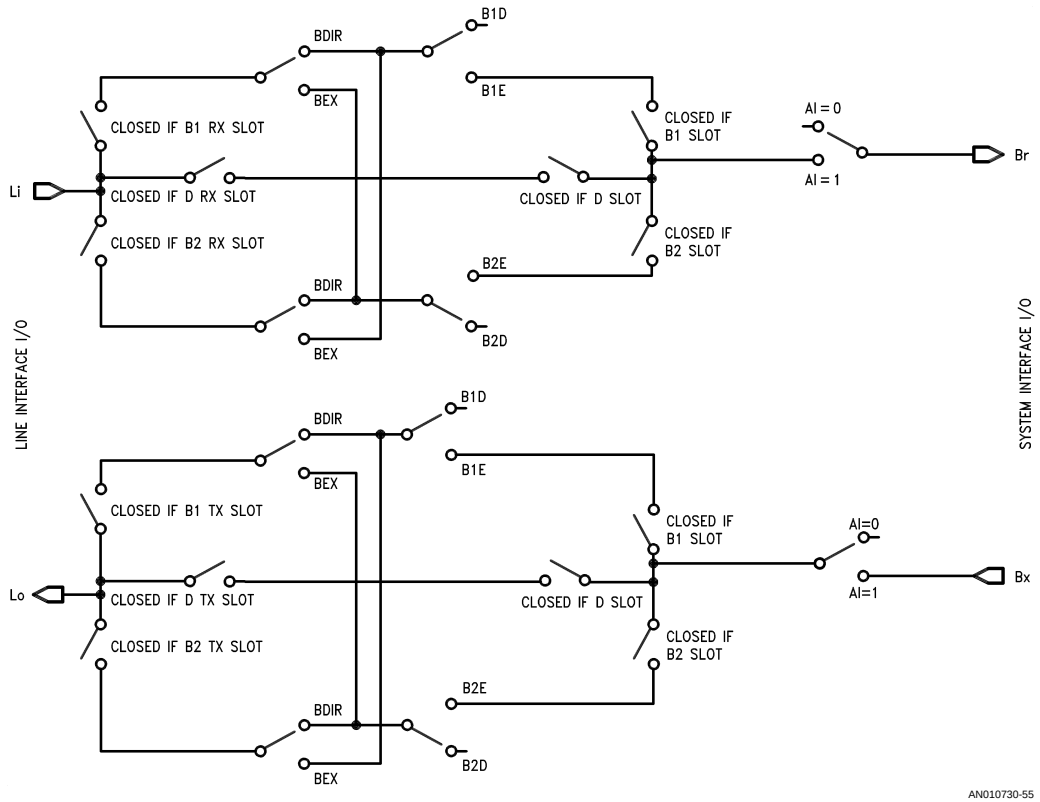
8.1 Normal Data Mode (No Loopbacks)

SID is powered up with clear all loopbacks (CAL) mode. In this mode, the function diagram of the device is as illustrated in *Figure 37*. This shows normal data paths when no test loopbacks are in effect. The switches are positioned according to the state of the device selected through commands.

8.2 System Loopback Mode LBS

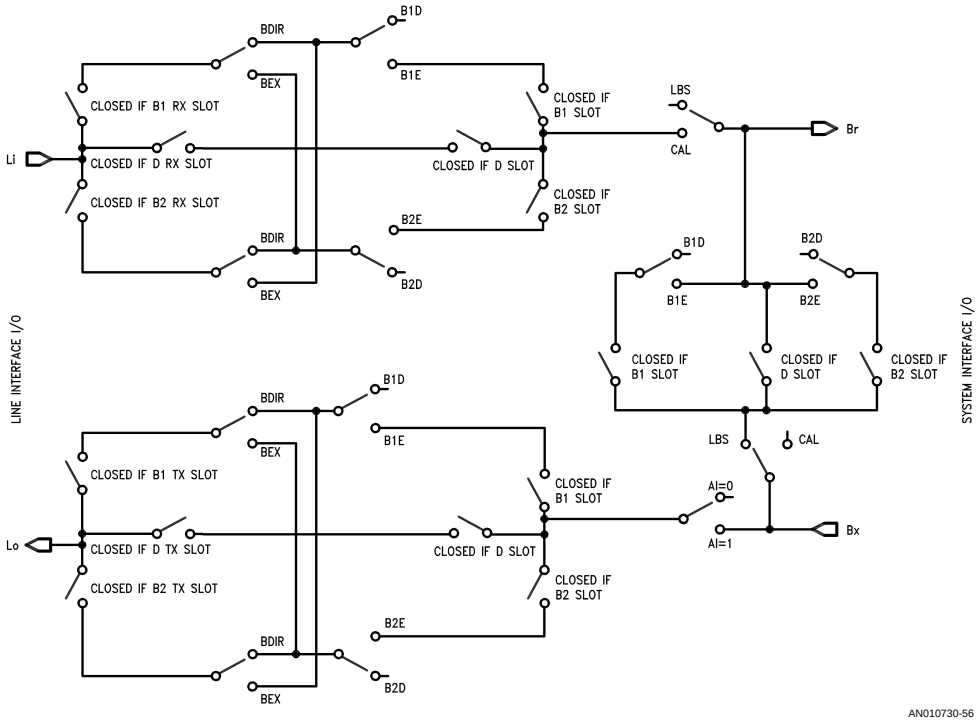
Figure 38 shows a schematic diagram illustrating the system loopback function (LBS). Upon writing the LBS command into the command register, various internal switches are positioned as in *Figure 38* if B1 and B2 channels are enabled. Bx data may be output onto the Lo pins of the line interface at the valid slots of the B1, D and B2 data periods on the Digital System Interface pin Bx and Br for the Format selected.

If the DENx Signal is used to strobe the D-Channel transient data, it is necessary to force the DENx to pulse every 8 kHz. This can be done by writing the DACCD while in TEM or TES mode.



Internal Control Signals
B1 Tx/Rx Slot:
B2 Tx/Rx Slot: Referenced to I.430 Line Interface Lo/Li time slot
D Tx/Rx Slot:
B1 Slot:
B2 Slot: Referenced to Digital System Interface Bx/Br time slot
D Slot:
External Command/Status
BDIR: B-CH mapped direct, B1 to B1, B2 to B2
BCX: B-CH exchanged, B1 to B2, B2 to B1
B1C: B1-CH enabled B2C: B2-CH enabled
B1D: B1-CH disabled B2D: B2-CH disabled
AI: Activation Indication

FIGURE 37. Normal Data Paths Diagram (No Loopbacks)



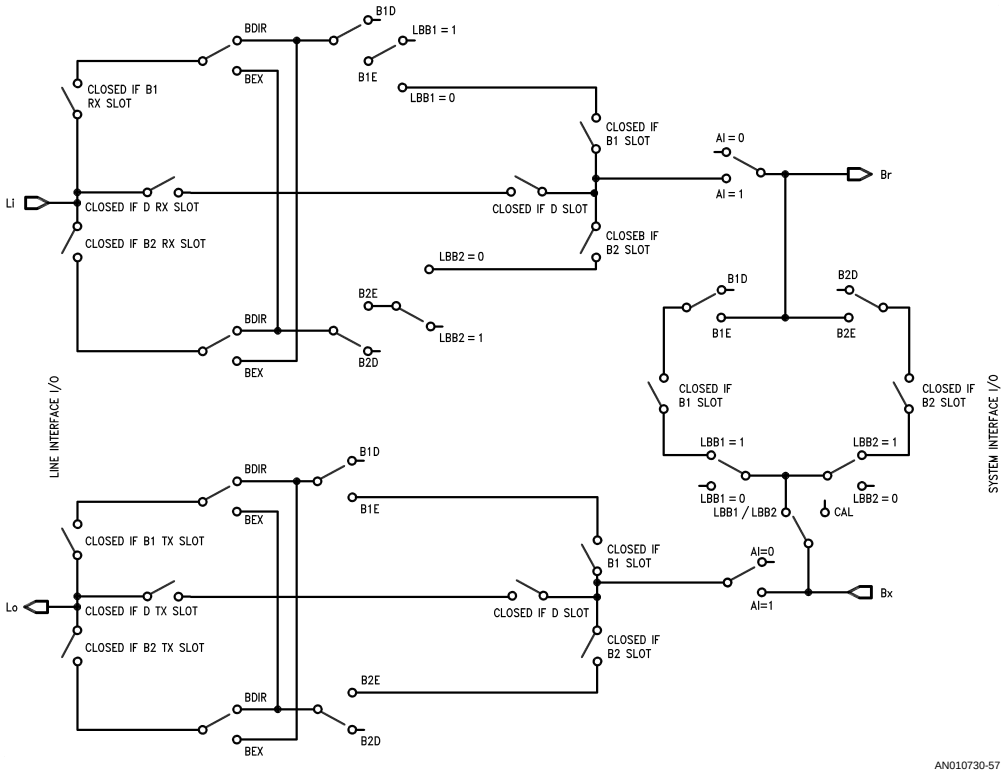
Internal Control Signals
B1 Tx/Rx Slot:
B2 Tx/Rx Slot: Referenced to I.430 line interface Lo/Li time slot
D Tx/Rx Slot:
B1 Slot:
B2 Slot: Referenced to Digital System Interface Bx/Br time slot
D Slot:
(**Note:** For NT/TES modes, FSa and FSb inputs have to be same phase)
External MICROWIRE Command/Status
LBS: Loopback 2B+D towards system interface
CAL: Clear all loopbacks
BDIR: B-CH mapped direct, B1 to B1, B2 to B2
BEX: B-CH exchanged, B1 to B2, B2 to B1
B1E: B1-CH enabled B2E: B2-CH enabled
B1D: B1-CH disabled B2D: B2-CH disabled
AI: Activation indication

FIGURE 38. TP3420A System Loopback Function Diagram (LBS)

8.3 System Loopback Mode LBB1, LBB2

Figure 39 shows a schematic diagram when LBB1 or LBB2 system loopbacks are used. LBB1 and LBB2 loopback modes may be chosen independently when B1 and/or B2 respectively are to be looped back to the system interface (from Bx to Br), while at the same time B1, B2 and D data to the line interface (Bx to Lo) may be allowed. Also, at the same time, B2 or B1 and D channel data may be allowed from the line interface to the system interface (Li to Br). Data transfers across line interface and system interface are possible only when SID is in the activated state (AI = 1).

For example, in *Figure 39* when LBB1 is enabled, the B1 channel from the system interface is looped back (assuming B1 is enabled). At this time B1, B2 and D channels may be transferred across the interfaces if AI is true; also, B2 and D channels may be transferred from Li to Br.



Internal Control Signals
B1 Tx/Rx Slot:
B2 Tx/Rx Slot: Referenced to I.430 line interface Lo/Li time slot
D Tx/Rx Slot:
B1 Slot:
B2 Slot: Referenced Digital System Interface Bx/Br time slot
D Slot:
Note: For NT/TES modes, FSa and FSb inputs have to be same phase
Note: No B-CH data loopback from Bx to Br
External Command/Status
LBB1: Loopback B1 towards system interface if LBB1 = 1
LBB2: Loopback B2 towards system interface if LBB2 = 1
CAL: Clear all loopbacks
BDIR: B-CH mapped direct, B1 to B1, B2 to B2
BEX: B-CH exchanged, B1 to B2, B2 to B1
B1E: B1-CH enabled B2E: -CH enabled
B1D: B1-CH disabled B2D: B2-CH disabled
AI: Activation Indication

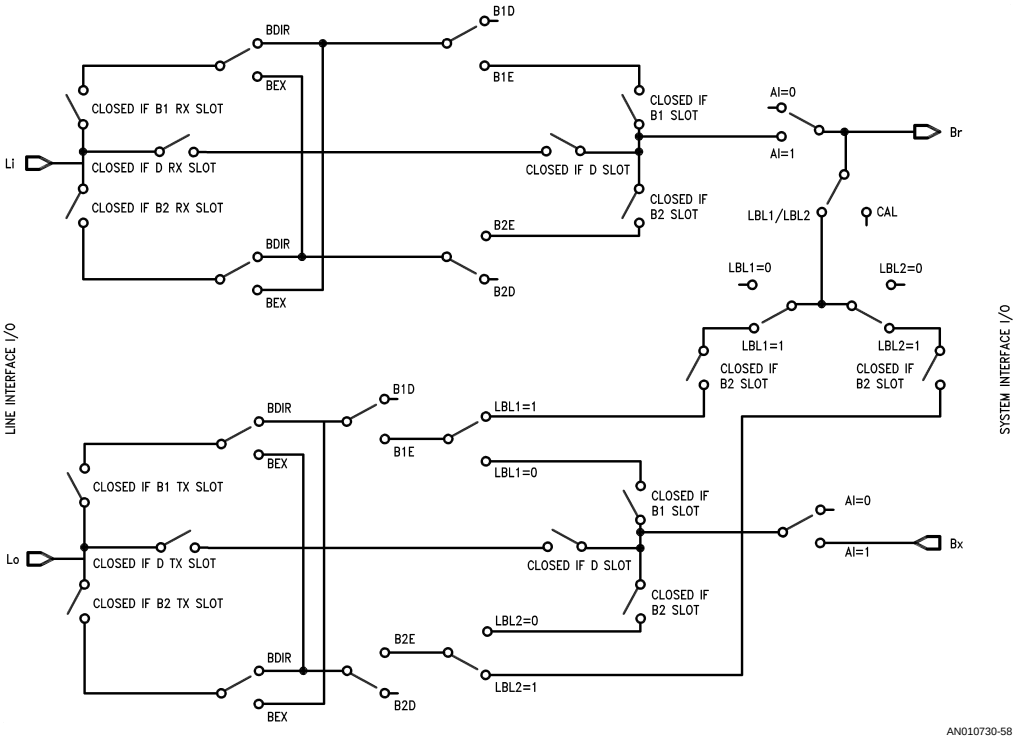
FIGURE 39. TP3420A System Loopback Function Diagram (LBB1, LBB2)

8.4 Line Loopack Mode LBL1, LBL2

LBL1 and LBL2 commands are used independently to select line loopback mode as shown in the function diagram of *Figure 40* when B1 and/or B2 are to be looped back to the line interface (from Li to Lo), while at the same time B1, B2 and D data to the system interface (Li to Br) may be allowed. Also, at the same time B2 or B1 and D channel data may be allowed from the system interface to the line interface (Bx to Lo). Of course, once again the transfers across the interfaces are conditional upon AI = 1 and the appropriate channels being enabled.

For example, when LBL1 is chosen, the B1 channel from the line interface is looped back. Notice at the same time B1, B2 and D channels are transferred to the Br pin of the system interface and also B2 and D channels from the system interface are transferred to the Lo pin of the line interface.

Figure 41 illustrates the simplified loopback functions that the device can be configured into.



Internal Control Signals
B1 Tx/Rx Slot:
B2 Tx/Rx Slot : Referenced to I.430 Line Interface Lo/Li time slot
D Tx/Rx Slot:
B1 Slot:
B2 Slot: Referenced to Digital System Interface Bx/Br time slot
D Slot:
Note: For NT/TES modes, FSa to FSb inputs have to be same phase
Note: No D-CH data loopback from Li to Lo
External Command/Status
LBL1: Loopback B1 towards line interface if LBL1 = 1
LBL2: Loopback B2 towards line interface if LBL2 = 1
CAL: Clear all loopbacks
BDIR: B-CH mapped direct, B1 to B1, B2 to B2
BEX: B-CH exchanged, B1 to B2, B2 to B1
B1E: B1-CH enabled B2E: B2-CH enabled
B1D: B1-CH disabled B2D: B2-CH disabled
AI: Activation Indication

FIGURE 40. TP3420A System Loopback Function Diagram (LBL1, LBL2)

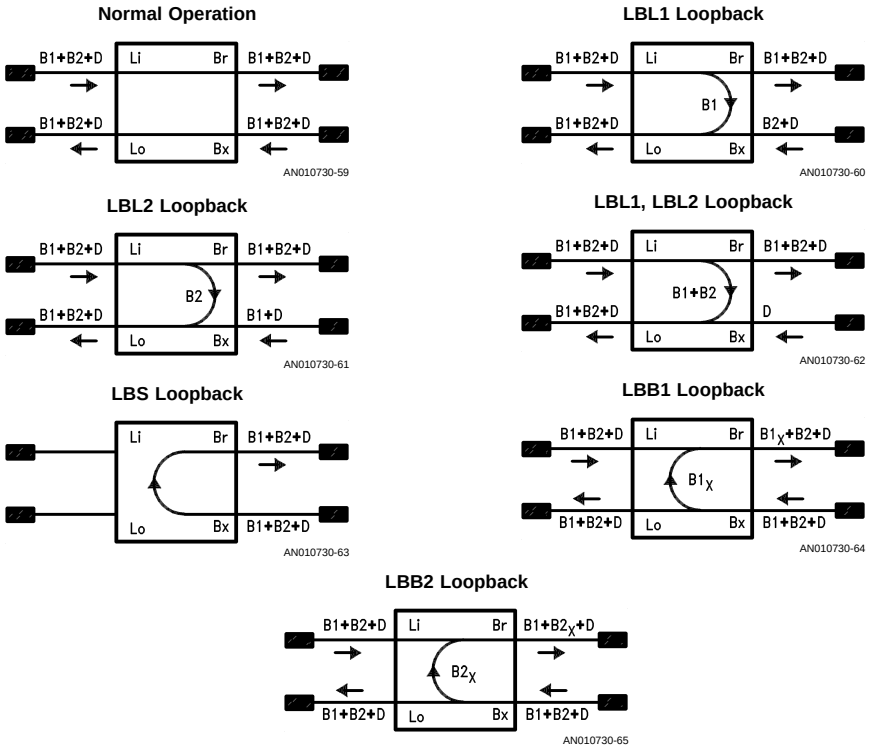


FIGURE 41. TP3420A Test Loopback Summary

9.0 ADDITIONAL TEST FEATURES

The TP3420A SID devices also include several system features intended for system test and system instrumentation purposes, namely the external local analog loopback and monitor mode activation as explained below.

9.1 External Local Analog Loopback

External local analog loopback is physically accomplished by connecting the line output signals after the transmit transformer to the line input signals before the receive transformer as shown in *Figure 42*. The SID is set in NTA or NTF mode and the local loop is activated with the following command sequence:

NTA (or NTF), PUP, AR. Receive status AP, AR, receive status AI.

The B channels are enabled (B1E, B2E) to transfer data on the B channels. Data can be sent or received on the D channel at 16 kbps. B and D channel data, fed in at the Bx input, is returned on the Br output after being looped at the external line interface. BCLK and FS signals need to be supplied to the SID operating in NT mode.

9.2 Monitor Mode Activation

The SID device may be configured for applications where D and/or B channels may be monitored in the upstream direction on an S interface pair as shown in *Figure 43*. The SID is to be first configured into TEM mode for this application and then MMA is written into the command register. This puts the TP3420A into a psuedo-NT mode in which it receives and activates on the incoming INFO3 frames. Note that in this application of the device, only the receiver section is actively connected to the S interface. This feature is targetted at applications where B and D channels are monitored for network analysis, as in protocol analyzers and line testers. Line monitoring in the downstream direction requires another device operating normally in TE Mode.

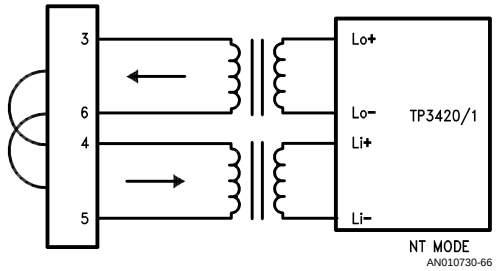


FIGURE 42. External Loopback Activation

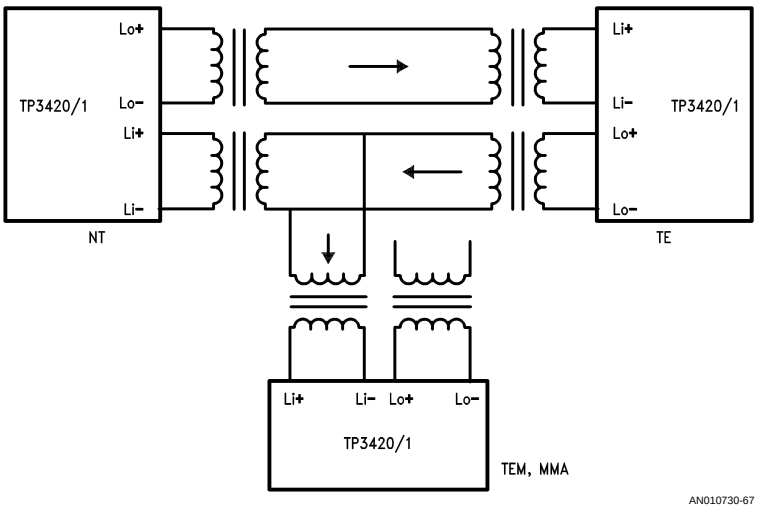


FIGURE 43. Monitor Mode Application

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