Layout Recommendations for a System Using National's FDDI Chip Set

National Semiconductor
Application Note 674
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This application note covers basic PCB layout recommendations and design techniques for high speed signal distribution in National's FDDI system. Due to the high signal speeds in FDDI, proper layout is critical. Many digital designers are not aware of problems that can arise in a high speed system from improper routing, incorrect termination, and poor power and ground layout.

ROUTING

Line reflections are a reflection of the signal waveform in a transmission line. They are caused by a difference in impedance between the transmission line and the load at the end of the line. If the line propagation delay is small compared to the rise time of the signal, the reflection is hidden during the rise time and is not seen as overshoot or ringing. However with the fast edge rates of the signals in a FDDI system, the line length becomes critical. The distortion that results from reflections can give false triggering or data errors. The signals most susceptible to reflections in a FDDI system are the differential ECL signals. In National's FDDI chip set these include the following:

- 125 MHz and 12.5 MHz ECL clocks from the DP83241 (CDD™ device)
- Receive Data and Receive Clock from the DP83231 (CRD™ device)
- Data to and from the fiber optic transceiver, and
- Loopback data from the DP83251/55 (PLAYER™ device)

It is imperative that these signal lines be kept as short as possible. To achieve this, the DP83241 should be placed close to the DP83251/55, the DP83231 should be placed close to the fiber optic receiver and the DP83251/55, and the fiber optic transmitter should be placed close to the DP83251/55 (*Figures 1* and *2*). The pinout of the PLAYER device determines the placement of the CDD and CRD devices. All the ECL signals that travel between these devices line up perfectly. To keep the ECL signals traveling between these three devices as short as possible, the CDD and CRD devices should be oriented with pin 1 facing the

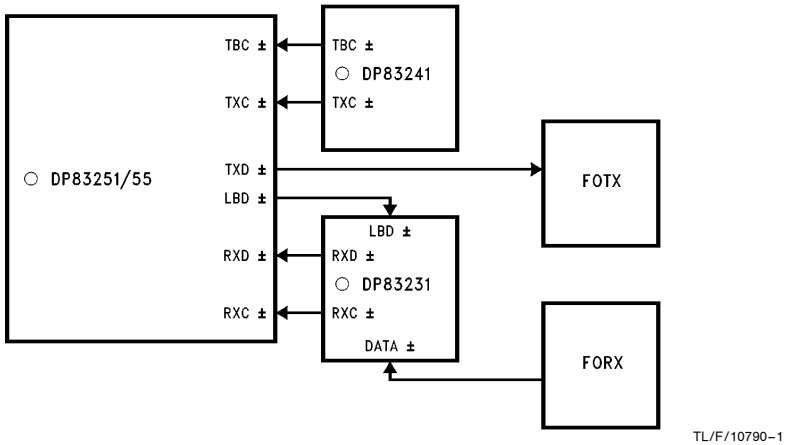

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FIGURE 1. Recommended Component Placement for a Single Attach Station (SAS)

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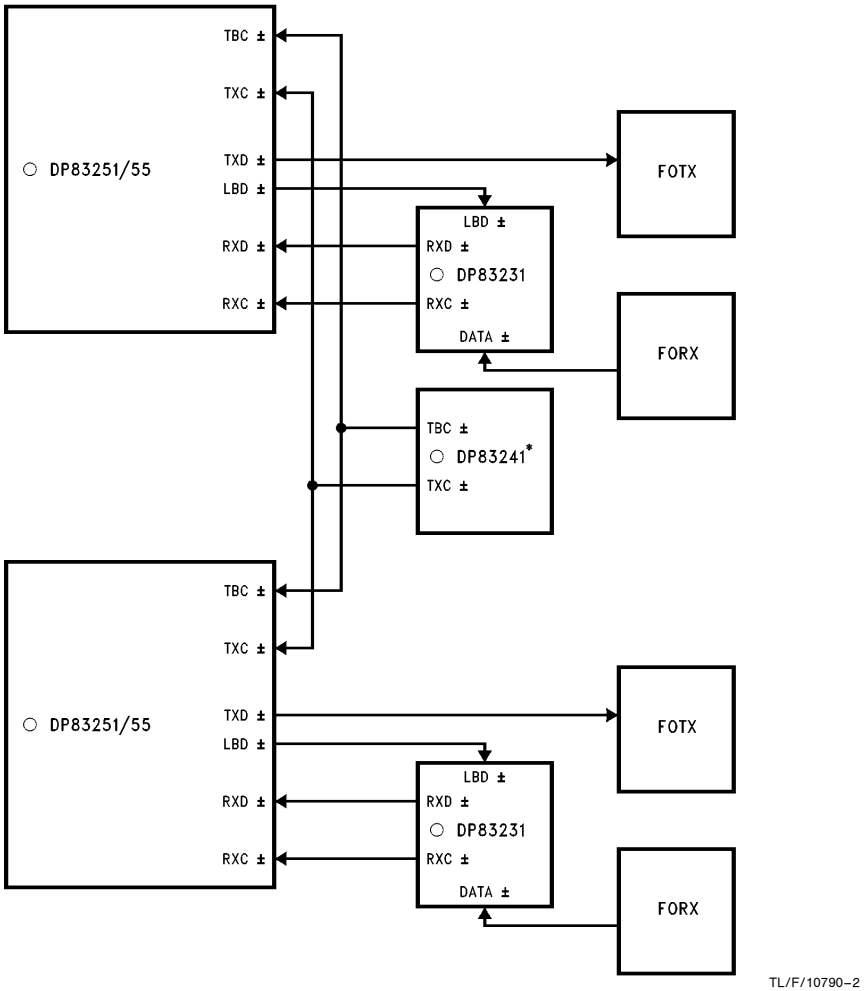

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*See DP83241 Datasheet for driving multiple DP83251/55 devices.

FIGURE 2. Recommended Component Placement for a Dual Attach Station (DAS)

PLAYER device. In addition, the PLAYER device must have its ECL signals facing toward the fiber optic transceiver.

A Single Attach Station (SAS) in an AT form factor was chosen to demonstrate recommended chip placement and signal routing. *Figures 3* through *7* show the basic connections between National's FDDI chips in a Single Attach Station. The silkscreen showing chip and component placement is shown in *Figure 8* and the actual signal traces are shown in *Figure 9*. The FOTX and FORX placement is set by the PMD specification. The CDD, CRD and PLAYER devices should be placed as described in the previous paragraph. However, due to the constraints of the AT form factor, it is necessary to rotate the CDD device and its external components 90 degrees counter clockwise. The only remaining chip to be placed was the DP83261, BMAC™ device. Once again the form factor determined the placement, but the orientation was chosen to allow an easy connection to the system interface, the control logic and the PLAYER device. Since the system interface logic is on the end of the board opposite the fiber optic transceiver, it was logical to have these signals facing that end of the board. It also allowed the control signals of the BMAC device to be near the control signals of the PLAYER device. All the TTL signals in this design can be autorouted. However, none of these signals should pass through the CDD or CRD device circuitry areas to avoid the possibility of noise due to crosstalk. In a Dual Attach Station (DAS) or a Concentrator design, the CRD device should still be placed as close as possible to the PLAYER device but the one CDD device responsible for clocking all the PLAYER and BMAC devices should be placed so as to minimize the skews between each PHY layer. More information regarding the CDD device driving multiple PLAYER devices can be found in the DP83241 datasheet.

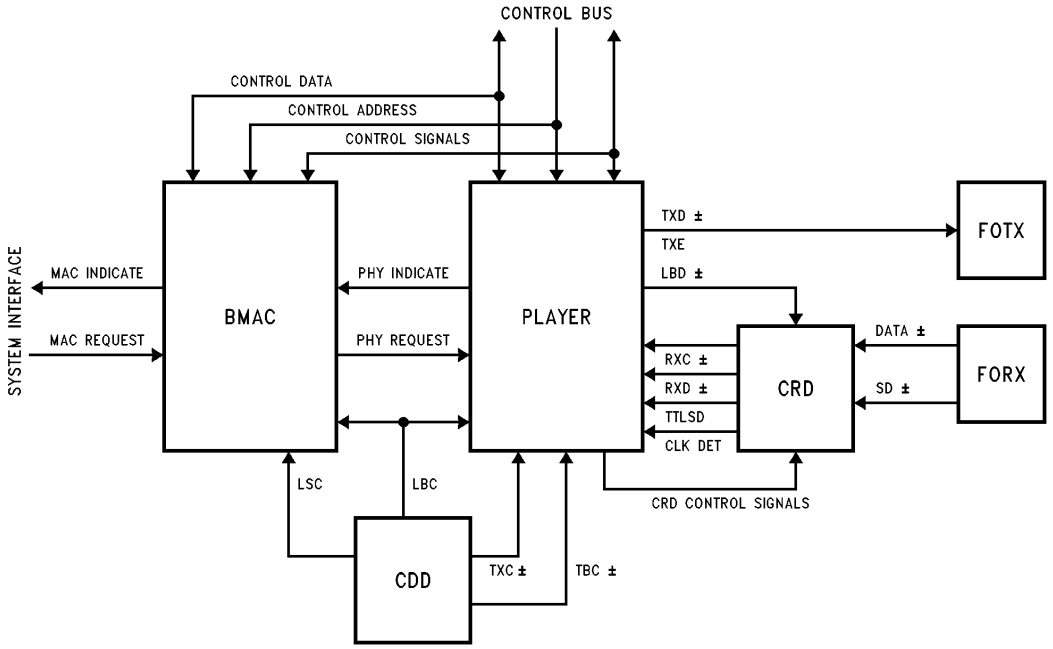

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FIGURE 3. Basic Block Diagram of a Single Attach Station Using National's FDDI Chips

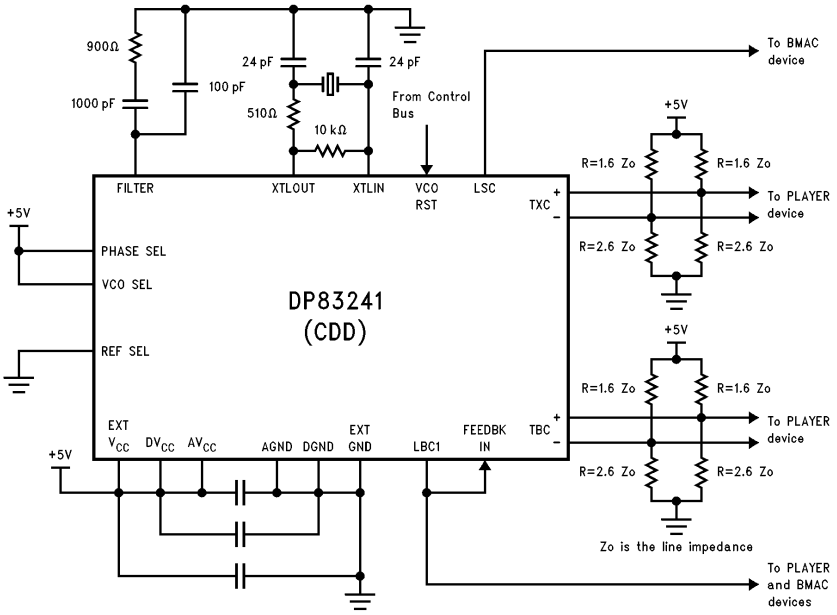

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FIGURE 4. Basic DP83241 Connections in a Single Attach Station (SAS)

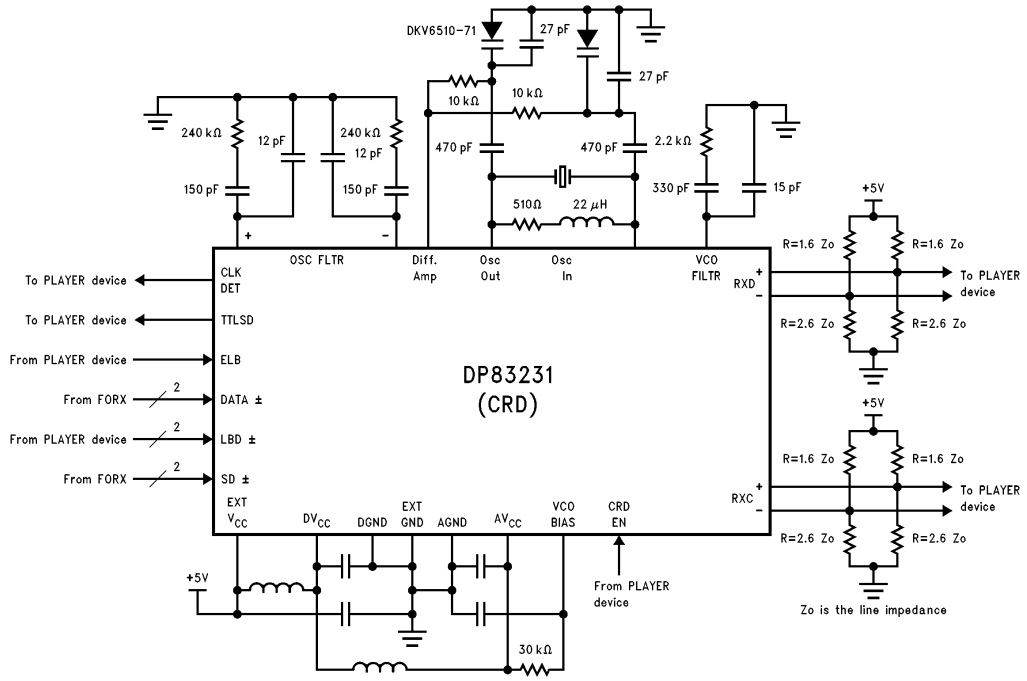

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FIGURE 5. Basic DP83231 Connections in a Single Attach Station (SAS)

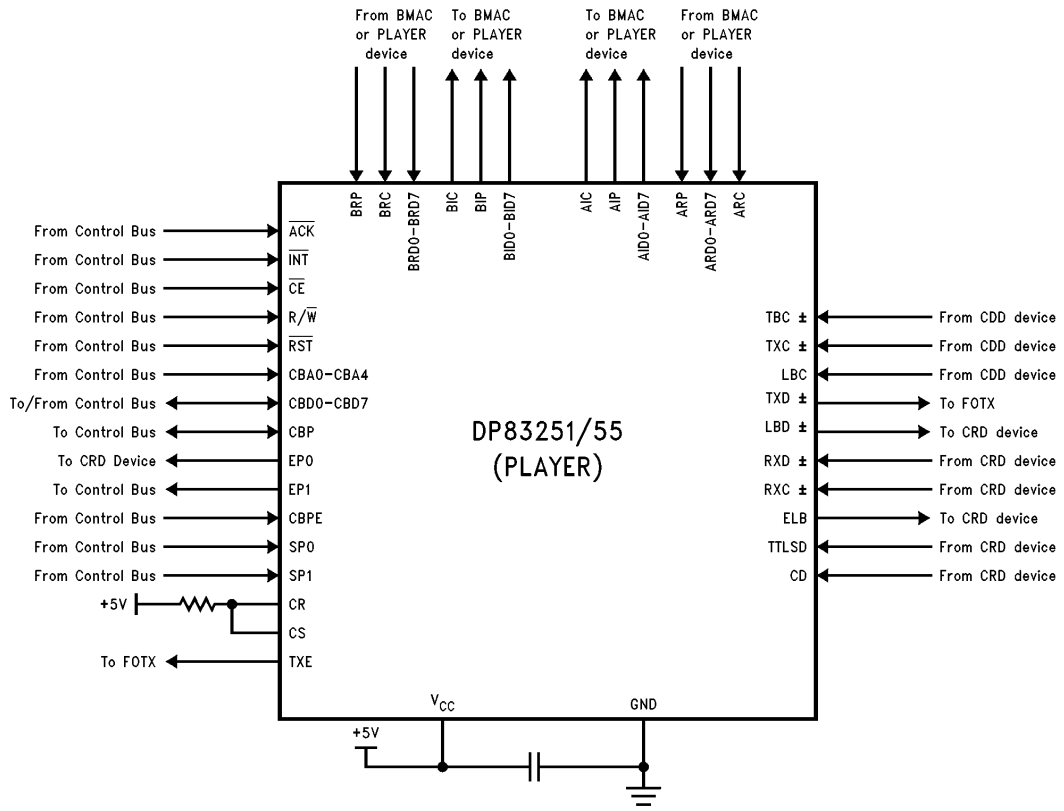

FIGURE 6. Basic DP83251/55 Connections for either an SAS or DAS

TERMINATION

In addition to keeping the ECL signal traces as short as possible to avoid reflections, it is necessary to properly terminate all of the ECL signal traces. If the ECL signals are not properly terminated, line reflections will occur. There are several methods for terminating signal traces but it is recommended that a Thevenin equivalent of the proper parallel termination be used. This method has the advantages of using a single power supply voltage and providing a pull-down resistor for the driver circuit.

Reflections occur not only from mismatched load and source impedances but also from changes in line impedance. The impedance of a signal trace can be set to a fairly accurate degree by setting the trace width to a particular value. The equation in Appendix B, System Considerations, shows how the line impedance is determined by the dielectric constant of the PCB, the thickness of the trace, the width of the trace and the distance of the trace from the ground plane. The dielectric constant will vary depending on the board manufacturer that is being used, so it is advisable to get this information from the board manufacturer before the ECL signals are routed. In an attempt to prevent line reflections, sharp bends (changes in the characteristic impedance) in the signal line should be avoided. It is recommended that all bends in high speed signal traces be forty-five degrees or less. More information on reflections and termination schemes can be found in Appendix A, Transmission Line Concepts, and Appendix B, System Considerations.

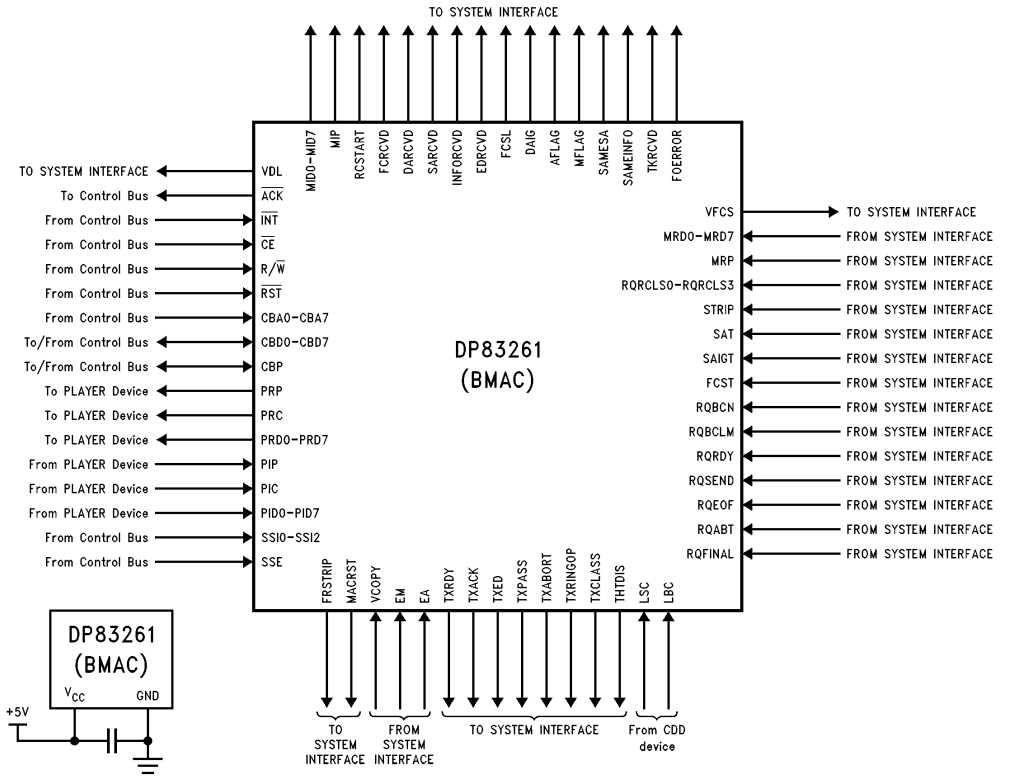

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FIGURE 7. Basic DP83261 Connections

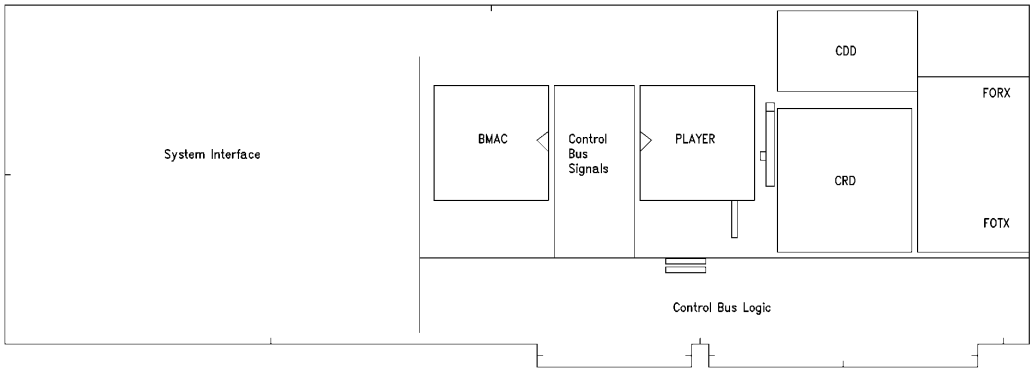

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FIGURE 8. Silkscreen Showing Placement of National's FDDI Chip Set in an SAS for an AT Form Factor

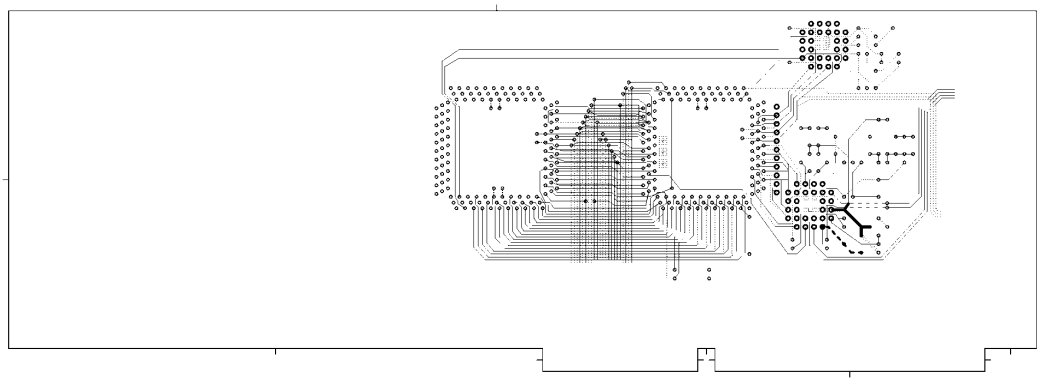

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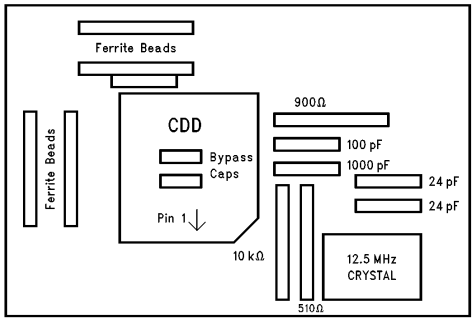
FIGURE 9. Signal Traces Connecting National's FDDI Chip Set in an SAS for an AT Form Factor



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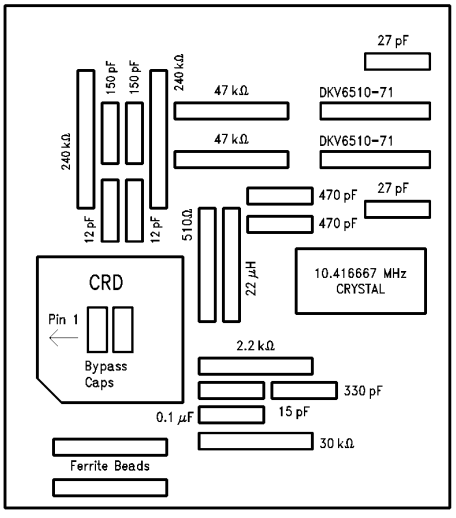

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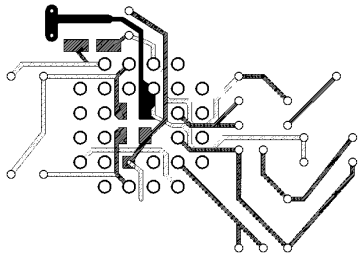
FIGURE 8a. Close Up of Silkscreen for CDD and CRD Portion of *Figure 8*



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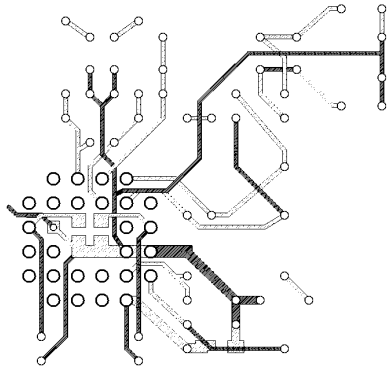

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FIGURE 9a. Close Up of Signal Traces for CDD and CRD Portion of *Figure 9.* Black traces represent the component side signal layer and the shaded traces represent the solder side signal layer.

POWER AND GROUND

In the design of a system, most people concern themselves with the layout of the signal lines and components and not with the ground and power layout. In high speed design, the shortest ground return path and the least inductive ground help maintain large signal noise margins. A common technique used to reduce ground noise is to create separate ground islands that are connected at only one point on the board. This point, at which the ground islands should connect is where the ground enters the PCB. The goal of this technique is to separate the noise on the ground plane, due to high current switching devices, from the parts which are susceptible to noise. Since voltage is equal to the inductance multiplied by the change in current divided by the change in time, a high current switching device will affect the noise margin of a signal. It is not necessay to create different ground islands for each part but only to create a separate ground island for the high current switching devices such as line or bus drivers. In the Single Attach Station design example described earlier in this application note there was a ground plane with no islands. The only exceptions to this involved some ground pins on the CDD and CRD devices. These connections are explained in the recommended layout sections of their datasheets.

The ground return path should be kept as short as possible by keeping the ground for an output device and the load (termination) on the same ground island. High speed signals should not be routed across different ground islands since a change in impedance will occur from the break in the ground planes. Ground should be routed on signal layers between signals that run parallel to each other for long distances.

Proper power supply bypassing is also recommended so that V_{CC} levels are not reduced when a sudden switch in current occurs. This reduction of V_{CC} will not be global, but instead localized and could affect the noise margin of a signal.

Remember that in ECL design, V_{CC} is connected to a logic ground but is actually the highest voltage level. The V_{EE} supply level should be treated as the ground and V_{CC} as the power supply when using National's FDDI chip set since it uses positive referenced ECL signals rather than negative.

More information on power and ground can be found in Appendix C, Power Distribution and Thermal Considerations.

APPENDIX A
ECL DESIGN GUIDE: TRANSMISSION LINE CONCEPTS

INTRODUCTION

The interactions between wiring and circuitry in high-speed systems are more easily determined by treating the interconnections as transmission lines. A brief review of basic concepts is presented and simplified methods of analysis are used to examine situations commonly encountered in digital systems. Since the principles and methods apply to any type of logic circuit, normalized pulse amplitudes are used in sample waveforms and calculations.

SIMPLIFYING ASSUMPTIONS

For the great majority of interconnections in digital systems, the resistance of the conductors is much less than the input and output resistance of the circuits. Similarly, the insulating materials have very good dielectric properties. These circumstances allow such factors as attenuation, phase distortion, and bandwidth limitations to be ignored. With these simplifications, interconnections can be dealt with in terms of characteristic impedance and propagation delay.

CHARACTERISTIC IMPEDANCE

The two conductors that interconnect a pair of circuits have distributed series inductance and distributed capacitance between them, and thus constitute a transmission line. For any length in which these distributed parameters are constant, the pair of conductors have a characteristic impedance Z_0. Whereas quiescent conditions on the line are determined by the circuits and terminations, Z_0 is the ratio of transient voltage to transient current passing by a point on the line when a signal charge or other electrical disturbance occurs. The relationship between transient voltage, transient current, characteristic impedance, and the distributed parameters is expressed as follows:

$$\frac{V}{I} = Z_0 = \sqrt{\frac{L_0}{C_0}} \qquad \text{(eq. 1)}$$

where L_0 = inductance per unit length, C_0 = capacitance per unit length. Z_0 is in ohms, L_0 in Henries, C_0 in Farads.

PROPAGATION VELOCITY

Propagation velocity ν and its reciprocal, delay per unit length δ, can also be expressed in terms of L_0 and C_0. A consistent set of units is nanoseconds, microhenries and picofarads, with a common unit of length.

$$\nu = \frac{1}{\sqrt{L_0 C_0}} \qquad \delta = \sqrt{L_0 C_0} \qquad \text{(eq. 2)}$$

Equations 1 and *2* provide a convenient means of determining the L_0 and C_0, of a line when delay, length and impedance are known. For a length *l* and delay T, δ is the ratio T/*l*. To determine L_0 and C_0, combine *Equations 1* and *2*.

$$L_0 = \delta Z_0 \qquad \text{(eq. 3)}$$

$$C_0 = \frac{\delta}{Z_0} \qquad \text{(eq. 4)}$$

More formal treatments of transmission line characteristics, including loss effects, are available from many sources.[1–3]

TERMINATION AND REFLECTION

A transmission line with a terminating resistor is shown in *Figure 1*. As indicated, a positive step function voltage travels from left to right. To keep track of reflection polarities, it is convenient to consider the lower conductor as the voltage reference and to think in terms of current flow in the top conductor only. The generator is assumed to have zero internal impedance. The initial current I_1 is determined by V_1 and Z_0.

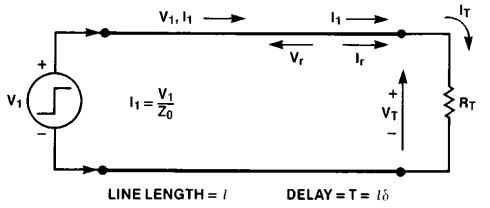

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FIGURE 1. Assigned Polarities and Directions for Determining Reflections

If the terminating resistor matches the line impedance, the ratio of voltage to current traveling along the line is matched by the ratio of voltage to current which must, by Ohm's law, always prevail at R_T. From the viewpoint of the voltage step generator, no adjustment of output current is ever required; the situation is as though the transmission line never existed and R_T had been connected directly across the terminals of the generator. From the R_T viewpoint, the only thing the line did was delay the arrival of the voltage step by the amount of time T.

When R_T is not equal to Z_0, the initial current starting down the line is still determined by V_1 and Z_0 but the final steady state current, after all reflections have died out, is determined by V_1 and R_T (ohmic resistance of the line is assumed to be negligible). The ratio of voltage to current in the initial wave is not equal to the ratio of voltage to current demanded by R_T. Therefore, at the instant the initial wave arrives at R_T, another voltage and current wave must be generated so that Ohm's law is satisfied at the line-load interface. This *reflected* wave, indicated by V_r and I_r in *Figure 1*, starts to return toward the generator. Applying

Kirchoff's laws to the end of the line at the instant the initial wave arrives, results in the following.

$I_1 + I_r = I_T =$ current into R_T (eq. 5)

Since only one voltage can exist at the end of the line at this instant of time, the following is true:

$$V_1 + V_r = V_T$$

thus $$I_T = \frac{V_T}{R_T} = \frac{V_1 + V_r}{R_T} \quad \text{(eq. 6)}$$

also $$I_1 = \frac{V_1}{Z_0} \text{ and } I_r = -\frac{V_r}{Z_0}$$

with the minus sign indicating that V_r is moving toward the generator.

Combining the foregoing relationships algebraically and solving for V_r yields a simplified expression in terms of V_1, Z_0 and R_T.

$$\frac{V_1}{Z_0} - \frac{V_r}{Z_0} = \frac{V_1 + V_r}{R_T} = \frac{V_1}{R_T} + \frac{V_r}{R_T}$$

$$V_1\left(\frac{1}{Z_0} - \frac{1}{R_T}\right) = V_r\left(\frac{1}{R_T} + \frac{1}{Z_0}\right) \quad \text{(eq. 7)}$$

$$V_r = V_1\left(\frac{R_T - Z_0}{R_T + Z_0}\right) = \rho_L V_1$$

The term in parenthesis is called the coefficient of reflection ρ. With R_T ranging between zero (shorted line) and infinity (open line), the coefficient ranges between -1 and $+1$ respectively. The subscript L indicates that ρ refers to the coefficient at the load end of the line.

Equation 7 expresses the amount of voltage sent back down the line, and since

$$V_T = V_1 + V_r \quad \text{(eq. 8)}$$

then $V_T = V_1 (1 + \rho_L)$.

V_T can also be determined from an expression which does not require the preliminary step of calculating ρ_L. Manipulating $(1 + \rho_L)$ results in

$$1 + \rho_L = 1 + \frac{R_T - Z_0}{R_T + Z_0} = 2\left(\frac{R_T}{R_T + Z_0}\right)$$

Substituting in *Equation 8* gives

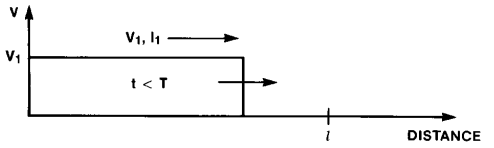
$$V_T = 2\left(\frac{R_T}{R_T + Z_0}\right) V_1 \quad \text{(eq. 9)}$$

The foregoing has the same form as a simple voltage divider involving a generator V_1 with internal impedance Z_0 driving a load R_T, except that the amplitude of V_T is doubled.

The arrow indicating the direction of V_r in *Figure 1* correctly indicates the V_r direction of travel, but the direction of I_r flow depends on the V_r polarity. If V_r is positive, I_r flows toward the generator, opposing I_1. This relationship between the polarity of V_r and the direction of I_r can be deduced by noting in *Equation 7* that if V_r is positive it is because R_T is greater than Z_0. In turn, this means that the initial current I_r is larger than the final quiescent current, dictated by V_1 and R_T. Hence, I_r must oppose I_1 to reduce the line current to the final quiescent value. Similar reasoning shows that if V_r is negative, I_r flows in the same direction as I_1.

It is sometimes easier to determine the effect of V_r on line conditions by thinking of it as an independent voltage generator in series with R_T. With this concept, the direction of I_r is immediately apparent; its magnitude, however, is the ratio of V_r to Z_0, i.e., R_T is already accounted for in the magnitude of V_r. The relationships between incident and reflected signals are represented in *Figure 2* for both cases of mismatch between R_T and Z_0.

The incident wave is shown in *Figure 2a*, before it has reached the end of the line. In *Figure 2b*, a positive V_r is returning to the generator. To the left of V_r the current is still I_1, flowing to the right, while to the right of V_r the net current in the line is the difference between I_1 and I_r. In *Figure 2c*, the reflection coefficient is negative, producing a negative V_r. This, in turn, causes an increase in the amount of current flowing to the right behind the V_r wave.



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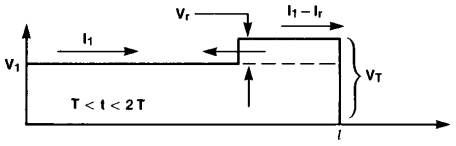
a. Incident Wave



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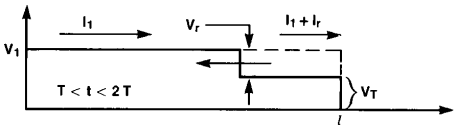
b. Reflected Wave for $R_T > Z_0$



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c. Reflected Wave for $R_T < Z_0$

FIGURE 2. Reflections for $R_T \neq Z_0$

SOURCE IMPEDANCE, MULTIPLE REFLECTIONS

When a reflected voltage arrives back at the source (generator), the reflection coefficient at the source determines the response to V_r. The coefficient of reflection at the source is governed by Z_0 and the source resistance R_S.

$$\rho_S = \frac{R_S - Z_0}{R_S + Z_0} \qquad \text{(eq. 10)}$$

If the source impedance matches the line impedance, a reflected voltage arriving at the source is not reflected back toward the load end. Voltage and current on the line are stable with the following values.

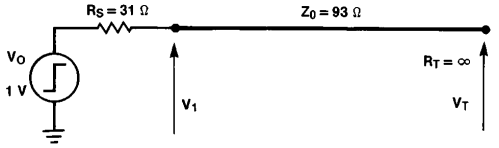
$$V_T = V_1 + V_r \text{ and } I_T = I_1 - I_r \qquad \text{(eq. 11)}$$

If neither source impedance nor terminating impedance matches Z_0, multiple reflections occur; the voltage at each end of the line comes closer to the final steady state value with each succeeding reflection. An example of a line mismatched on both ends is shown in *Figure 3*. The source is a step function of 1V amplitude occurring at time t_0. The initial value of V_1 starting down the line is 0.75V due to the voltage divider action of Z_0 and R_S. The time scale in the photograph shows that the line delay is approximately 6 ns. Since neither end of the line is terminated in its characteristic impedance, multiple reflections occur.

The amplitude and persistence of the ringing shown in *Figure 3* become greater with increasing mismatch between the line impedance and source and load impedances. Reducing R_S *(Figure 3)* to 13Ω increases ρ_S to −0.75V, and the effects are illustrated in *Figure 4*. The initial value of V_T is 1.8V with a reflection of 0.9V from the open end. When this reflection reaches the source, a reflection of 0.9V × −0.75V starts back toward the open end. Thus, the second increment of voltage arriving at the open end is negative going. In turn, a negative-going reflection of 0.9V × −0.75V starts back toward the source. This negative increment is again multiplied by −0.75 at the source and returned toward the open end. It can be deduced that the difference in amplitude between the first two positive peaks observed at the open end is

$$V_T - V'_T = (1 + \rho_L)\, V_1 - (1 + \rho_L)\, V_1\, \rho^2_L\, \rho^2_S = (1 + \rho_L)\, V_1\, (1 - \rho^2_L\, \rho^2_S). \qquad \text{(eq. 12)}$$

The factor $(1 - \rho^2_L\, \rho^2_S)$ is similar to the damping factor associated with lumped constant circuitry. It expresses the attenuation of successive positive or negative peaks of ringing.



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$$\rho_S = \frac{31 - 93}{31 + 93} = -0.5 \qquad \rho_L = \frac{\infty - 93}{\infty + 93} = +1$$

$$\text{Initially: } V_1 = \frac{Z_0}{Z_0 + R_S} \bullet V_0 = \frac{93}{124} \bullet 1 = 0.75\text{V}$$

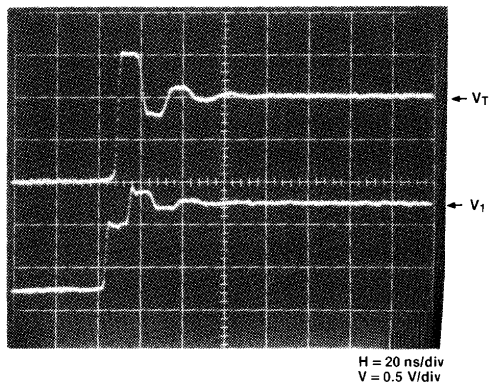

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FIGURE 3. Multiple Reflections Due to Mismatch at Load and Source

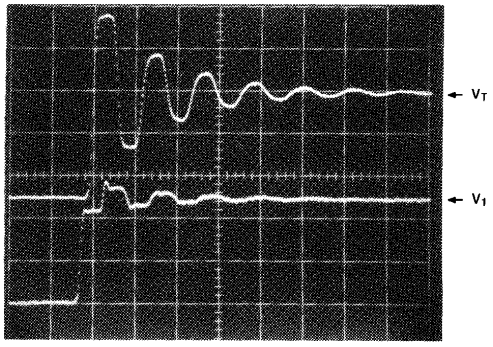

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FIGURE 4. Extended Ringing when R_S of *Figure 3* is Reduced to 13Ω

LATTICE DIAGRAM

In the presence of multiple reflections, keeping track of the incremental waves on the line and the net voltage at the ends becomes a bookkeeping chore. A convenient and systematic method of indicating the conditions which combines magnitude, polarity and time utilizes a graphic construction called a lattice diagram.[4] A lattice diagram for the line conditions of *Figure 3* is shown in *Figure 5*.

The vertical lines symbolize discontinuity points, in this case the ends of the line. A time scale is marked off on each line in increments of 2T, starting at t_0 for V_1 and T for V_T. The diagonal lines indicate the incremental voltages traveling between the ends of the line; solid lines are used for positive voltages and dashed lines for negative. It is helpful to write the reflection and transmission multipliers ρ and (1 + ρ) at each vertical line, and to tabulate the incremental and net voltages in columns alongside the vertical lines. Both the lattice diagram and the waveform photograph show that V_1 and V_T asymptotically approach 1V, as they must with a 1V source driving an open-ended line.

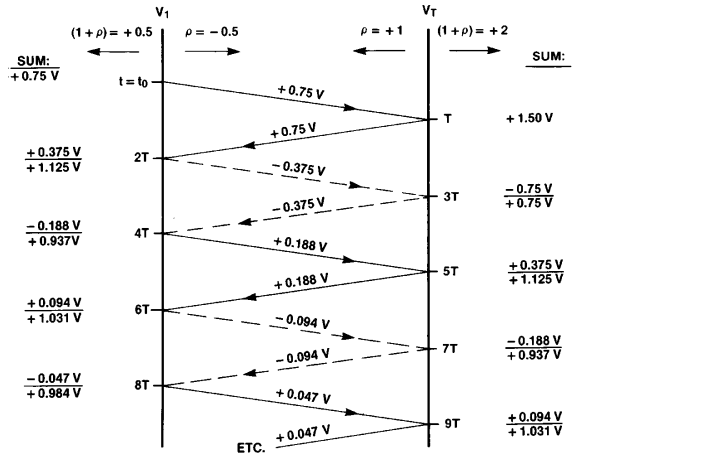

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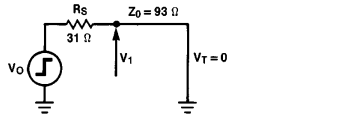
FIGURE 5. Lattice Diagram for the Circuit of *Figure 3*

SHORTED LINE

The open-ended line in *Figure 3* has a reflection coefficient of +1 and the successive reflections tend toward the steady state conditions of zero line current and a line voltage equal to the source voltage. In contrast, a shorted line has a reflection coefficient of −1 and successive reflections must cause the line conditions to approach the steady state conditions of zero voltage and a line current determined by the source voltage and resistance.

Shorted line conditions are shown in *Figure 6a* with the reflection coefficient at the source end of the line also negative. A negative coefficient at both ends of the line means that any voltage approaching either end of the line is reflected in the opposite polarity. *Figure 6b* shows the response to an input step-function with a duration much longer than the line delay. The initial voltage starting down the line is about +0.75V, which is inverted at the shorted end and returned toward the source as −0.75V. Arriving back at the source end of the line, this voltage is multiplied by (1 + ρ_S), causing a −0.37V net change in V_1. Concurrently, a reflected voltage of +0.37V (−0.75V times ρ_S of −0.5) starts back toward the shorted end of the line. The voltage at V_1 is reduced by 50% with each successive round trip of reflections, thus leading to the final condition of zero volts on the line.

When the duration of the input pulse is less than the delay of the line, the reflections observed at the source end of the line constitute a train of negative pulses, as shown in *Figure 6c*. The amplitude decreases by 50% with each successive occurrence as it did in *Figure 6b*.



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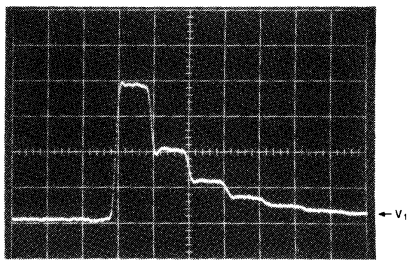
$\rho_S = -0.5$ $\quad \rho_L = \frac{0 - 93}{0 + 93} = -1$

a. Reflection Coefficients for Shorted Line



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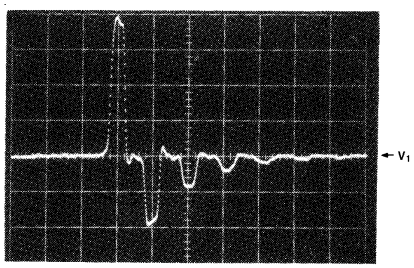
b. Input Pulse Duration ≫ Line Delay



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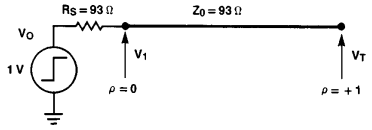
c. Input Pulse Duration < Line Delay

FIGURE 6. Reflections of Long and Short Pulses on a Shorted Line

SERIES TERMINATION

Driving an open-ended line through a source resistance equal to the line impedance is called series termination. It is particularly useful when transmitting signals which originate on a PC board and travel through the backplane to another board, with the attendant discontinuities, since reflections coming back to the source are absorbed and ringing thereby controlled. *Figure 7* shows a 93Ω line driven from a 1V generator through a source impedance of 93Ω. The photograph illustrates that the amplitude of the initial signal sent down the line is only half of the generator voltage, while the voltage at the open end of the line is doubled to full amplitude ($1 + \rho_L = 2$). The reflected voltage arriving back at the source raises V_1 to the full amplitude of the generator signal. Since the reflection coefficient at the source is zero, no further changes occur and the line voltage is equal to the generator voltage. Because the initial signal on the line is only half the normal signal swing, the loads must be connected at or near the end of the line to avoid receiving a 2-step input signal.

An ECL output driving a series terminated line requires a pull-down resistor to V_{EE}, as indicated in *Figure 8*. The resistor R_0 shown in *Figure 8* symbolizes the output resistance of the ECL gate. The relationships between R_0, R_S, R_E and Z_0 are discussed in Appendix B.



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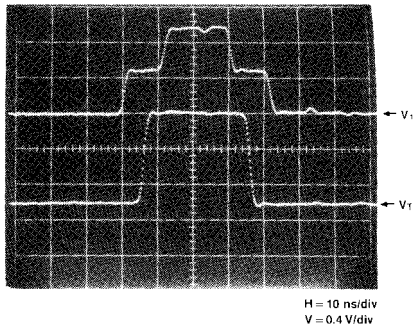

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FIGURE 7. Series Terminated Line and Waveforms

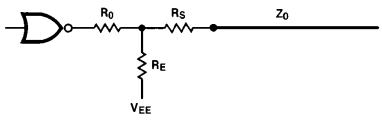

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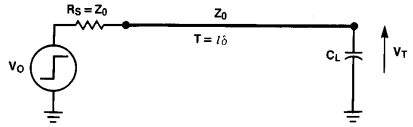
FIGURE 8. ECL Element Driving a Series Terminated Line

EXTRA DELAY WITH TERMINATION CAPACITANCE

Designers should consider the effect of the load capacitance at the end of the line when using series termination. *Figure 9* shows how the output waveform changes with increasing load capacitance. *Figure 9b* shows the effect of load capacitances of 0, 12, 24, 48 pF. With no load, the delay between the 50% points of the input and output is just the line delay T. A capacitive load at the end of the line causes an extra delay ΔT due to the increase in rise time of the output signal. The midpoint of the output is used as a criterion because the propagation delay of an ECL circuit is measured between the 50% points of the input and output signals.



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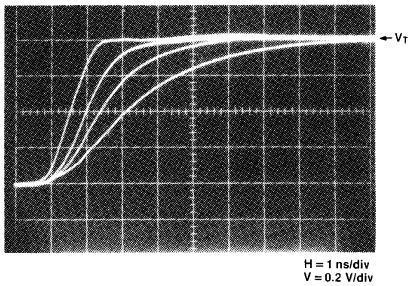
a. Series Terminated Line with Load Capacitance



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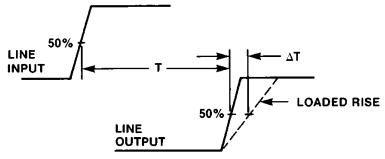
b. Output Rise Time Increase with Increasing Load Capacitance



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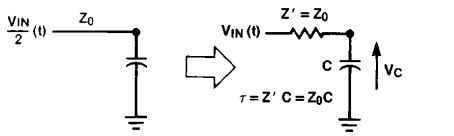
c. Extra Delay ΔT Due to Rise Time Increase

FIGURE 9. Extra Delay with Termination Capacitance



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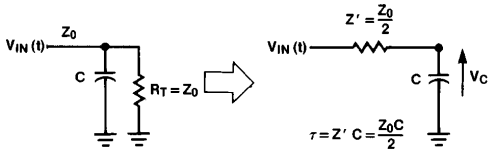
a. Thevenin Equivalent for Series Terminated Case



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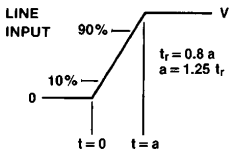
b. Thevenin Equivalent for Parallel Terminated Case



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$$\nu_{in}(t) = \frac{V}{a}\,[\,tu(t) - (t-a)u\,(t-a)]$$

$$u(t) = \frac{0 \text{ for } t < O}{1 \text{ for } t > O}$$

$$u(t-a) = \begin{matrix} 0 \text{ for } t < a, \\ 1 \text{ for } t > a \end{matrix}$$

$$V_{IN}(S) = \frac{V}{as^2}\,(1 - e^{-as})$$

$$V_C(S) = \frac{V}{ar} \bullet \frac{1}{s^2\,(s + 1/\tau)}\,(1 - e^{-as})$$

$$\nu_c(t) = \frac{V}{a}\,[t - \tau(1 - e^{-t/\tau})]\,u(t)$$

$$-\frac{V}{a}\,[(t-a)$$

$$-\tau(1 - e^{-\frac{t-a}{\tau}})]\,u\,(t-a)$$

c. Equations for Input and Output Voltages

FIGURE 10. Determining the Effect of End-of-Line Capacitance

The increase in propagation delay can be calculated by using a ramp approximation for the incident voltage and characterizing the circuit as a fixed impedance in series with the load capacitance, as shown in *Figure 10*. One general solution serves both series and parallel termination cases by using an impedance Z′ and a time constant τ, defined in *Figure 10a* and *10b*. Calculated and observed increases in delay time to the 50% point show close agreement when τ is less than half the ramp time. At large ratios of τ/a (where a = ramp time), measured delays exceed calculated values by approximately 7%. *Figure 11*, based on measured values, shows the increase in delay to the 50% point as a function of the Z′C time constant, both normalized to the 10% to 90% rise time of the input signal. As an example of using the graph, consider a 100Ω series terminated line with 30 pF load capacitance at the end of the line and a no-load rise time of 3 ns for the input signal. From *Figure 10a*, Z′ is equal to 100Ω; the ratio $Z'C/t_r$ is 1. From the graph, the ratio $\Delta T/t_r$ is 0.8. Thus the increase in the delay to the 50% point of the output waveform is 0.8 t_r, or 2.4 ns, which is then added to the no-load line delay T to determine the total delay.

Had the 100Ω line in the foregoing example been parallel rather than series terminated at the end of the line, Z′ would be 50Ω. The added delay would be only 1.35 ns with the same 30 pF loading at the end. The added delay would be only 0.75 ns if the line were 50Ω and parallel terminated. The various trade-offs involving type of termination, line impedance, and loading are important considerations for critical delay paths.

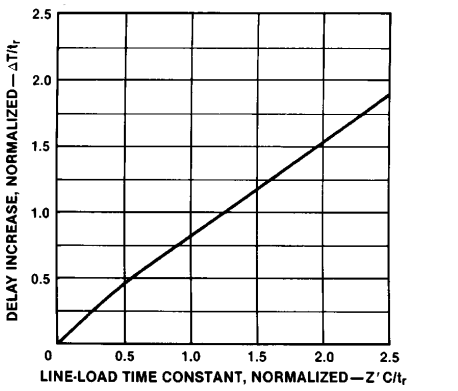

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FIGURE 11. Increase in 50% Point Delay Due to Capacitive Loading at the End of the Line, Normalized to T_r

DISTRIBUTED LOADING EFFECTS ON LINE CHARACTERISTICS

When capacitive loads such as ECL inputs are connected along a transmission line, each one causes a reflection with a polarity opposite to that of the incident wave. Reflections from two adjacent loads tend to overlap if the time required for the incident wave to travel from one load to the next is equal to or less than the signal rise time.[5] *Figure 12a* illustrates an arrangement for observing the effects of capacitive loading, while *Figure 12b* shows an incident wave followed by reflections from two capacitive loads. The two capacitors causing the reflections are separated by a distance requiring a travel time of 1 ns. The two reflections return to the source 2 ns apart, since it takes 1 ns longer for the incident wave to reach the second capacitor and an additional 1 ns for the second reflection to travel back to the source. In the upper trace of *Figure 12b*, the input signal rise time is 1 ns and there are two distinct reflections, although the trailing edge of the first overlaps the leading edge of the second. The input rise time is longer in the middle trace, causing a greater overlap. In the lower trace, the 2 ns input rise time causes the two reflections to merge and appear as a single reflection which is relatively constant (at $\approx -10\%$) for half its duration. This is about the same reflection that would occur if the 93Ω line had a middle section with an impedance reduced to 75Ω.

With a number of capacitors distributed all along the line of *Figure 12a*, the combined reflections modify the observed input waveform as shown in the top trace of *Figure 12c*. The reflections persist for a time equal to the 2-way line delay (15 ns), after which the line voltage attains its final value. The waveform suggests a line terminated with a resistance greater than its characteristic impedance ($R_T > Z_0$). This analogy is strengthened by observing the effect of reducing R_T from 93Ω to 75Ω, which leads to the middle waveform of *Figure 12c*. Note that the final (steady state) value of the line voltage is reduced by about the same amount as that caused by the capacitive reflections. In the lower trace of *Figure 12c* the source resistance R_S is reduced from 93Ω to 75Ω, restoring both the initial and final line voltage values to the same amplitude as the final value in the upper trace. From the standpoint of providing a desired signal voltage on the line and impedance matching at either end, the effect of distributed capacitive loading can be treated as a reduction in line impedance.

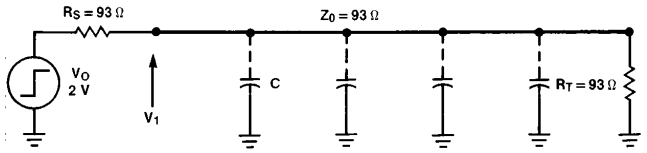
The reduced line impedance can be calculated by considering the load capacitance C_L as an increase in the intrinsic line capacitance C_0 along that portion of the line where the loads are connected.[6] Denoting this length of line as *l*, the distributed value C_D of the load capacitance is as follows.

$$C_D = \frac{C_L}{l}$$

C_D is then added to C_0 in *Equation 1* to determine the reduced line impedance Z_0.

$$Z'_0 = \sqrt{\frac{L_0}{C_0 + C_D}} = \sqrt{\frac{L_0}{C_0\left(1 + \frac{C_D}{C_0}\right)}} \qquad \text{(eq. 13)}$$

$$Z'_0 + \frac{\sqrt{\frac{L_0}{C_0}}}{\sqrt{1 + \frac{C_D}{C_0}}} = \frac{Z_0}{\sqrt{1 + \frac{C_D}{C_0}}}$$



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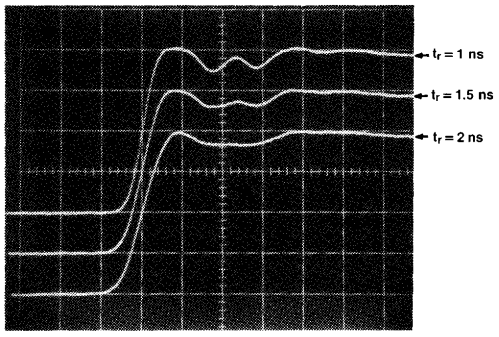
a. Arrangement for Observing Capacitive Loading Effects



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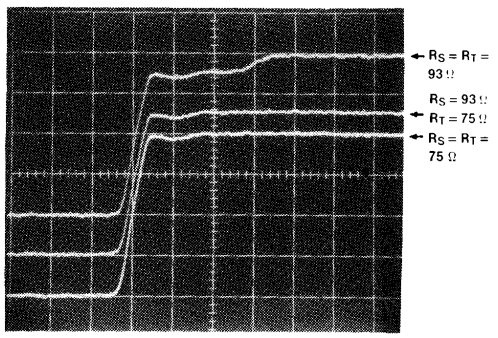
b. Capacitive Reflections Merging as Rise Time Increases



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c. Matching the Altered Impedance of a Capacitively Loaded Line

FIGURE 12. Capacitive Reflections and Effects on Line Characteristics

In the example of *Figure 12c*, the total load capacitance is 33 pF while the total intrinsic line capacitance /C_0 is 60 pF. (Note that the ratio C_D/C_0 is the same as $C_L//C_0$.) The calculated value of the reduced impedance is thus

$$Z'_0 = \frac{93}{\sqrt{1 + \frac{33}{60}}} = \frac{93}{\sqrt{1.55}} = 75\Omega \qquad \text{(eq. 14)}$$

This correlates with the results observed in *Figure 12c* when R_T and R_S are reduced to 75Ω.

The distributed load capacitance also increases the line delay, which can be calculated from *Equation 2*.

$$\delta' = \sqrt{L_0 (C_0 + C_D)} = \sqrt{L_0 C_0}\sqrt{1 + \frac{C_D}{C_0}} = \delta\sqrt{1 + \frac{C_D}{C_0}} \qquad \text{(eq. 15)}$$

The line used in the example of *Figure 12c* has an intrinsic delay of 6 ns and a loaded delay of 7.5 ns which checks with *Equation 15*.

$$/\delta' = /\delta\sqrt{1.55} = 6\sqrt{1.55} = 7.5 \text{ ns} \qquad \text{(eq. 16)}$$

Equation 15 can be used to predict the delay for a given line and load. The ratio C_D/C_0 (hence the loading effect) can be minimized for a given loading by using a line with a high intrinsic capacitance C_0.

A plot of Z' and δ' for a 50Ω line as a function of C_D is shown in *Figure 13*. This figure illustrates that relatively modest amounts of load capacitance will add appreciably to the propagation delay of a line. In addition, the characteristic impedance is reduced significantly.

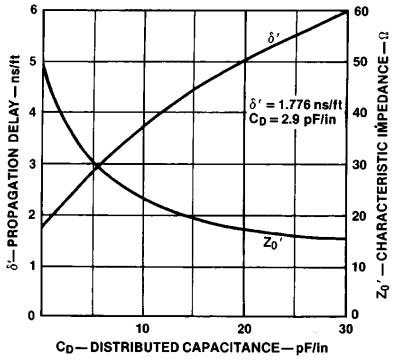

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FIGURE 13. Capacitive Loading Effects on Line Delay and Impedance

Worst case reflections from a capacitively loaded section of transmission line can be accurately predicted by using the modified impedance of *Equation 9*.[6] When a signal originates on an unloaded section of line, the effective reflection coefficient is as follows.

$$\rho = \frac{Z'_0 - Z_0}{Z'_0 + Z_0} \qquad \text{(eq. 17)}$$

MISMATCHED LINES

Reflections occur not only from mismatched load and source impedances but also from changes in line impedance. These changes could be caused by bends in coaxial cable, unshielded twisted-pair in contact with metal, or mismatch between PC board traces and backplane wiring. With the coax or twisted-pair, line impedance changes run about 5% to 10% and reflections are usually no problem since the percent reflection is roughly half the percent change in impedance. However, between PC board and backplane wiring, the mismatch can be 2 or 3 to 1. This is illustrated in *Figure 14* and analyzed in the lattice diagram of *Figure 15*. Line 1 is driven in the series terminated mode so that reflections coming back to the source are absorbed.

The reflection and transmission at the point where impedances differ are determined by treating the downstream line as though it were a terminating resistor. For the example of *Figure 14*, the reflection coefficient at the intersection of lines 1 and 2 for a signal traveling to the right is as follows.

$$\rho_{12} = \frac{Z_2 - Z_1}{Z_2 + Z_1} = \frac{93 - 50}{143} = +0.3 \qquad \text{(eq. 18)}$$

Thus the signal reflected back toward the source and the signal continuing along line 2 are, respectively, as follows.

$$V_{1r} = \rho_{12} V_1 = +0.3V_1 \qquad \text{(eq. 19a)}$$

$$V_2 = (1 + \rho_{12}) V_1 = +1.3 V_1 \qquad \text{(eq. 19b)}$$

At the intersection of lines 2 and 3, the reflection coefficient for signals traveling to the right is determined by treating Z_3 as a terminating resistor.

$$\rho_{23} = \frac{Z_3 - Z_2}{Z_3 + Z_2} = \frac{39 - 93}{132} = -0.41 \qquad \text{(eq. 20)}$$

When V_2 arrives at this point, the reflected and transmitted signals are as follows.

$$V_{2r} = \rho_{23} V_2 = -0.41 V_2 = (-0.41)(1.3) V_1 = -0.53 V_1 \qquad \text{(eq. 21a)}$$

$$V_3 = (1 + \rho_{23}) V_2 = 0.59 V_2 = (0.59)(1.3) V_1 = 0.77 V_1 \qquad \text{(eq. 21b)}$$

Voltage V_3 is doubled in magnitude when it arrives at the open-ended output, since ρ_L is +1. This effectively cancels the voltage divider action between R_S and Z_1.

$$V_4 = (1 + \rho_L) V_3 = (1 + \rho_L)(1 + \rho_{23}) V_2 = (1 + \rho_L)(1 + \rho_{23})(1 + \rho_{12}) V_1 = (1 + \rho_L)(1 + \rho_{23})(1 + \rho_{12})\frac{V_0}{2} \qquad \text{(eq. 22)}$$

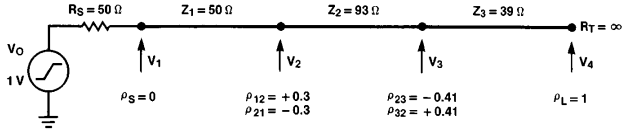
$$V_4 = (1 + \rho_{23})(1 + \rho_{12}) V_O$$

Thus, *Equation 22* is the general expression for the initial step of output voltage for three lines when the input is series terminated and the output is open-ended.

Note that the reflection coefficients at the intersections of lines 1 and 2 and lines 2 and 3 in *Figure 15* have reversed signs for signals traveling to the left. Thus the voltage reflected from the open output and the signal reflecting back and forth on line 2 both contribute additional increments of output voltage in the same polarity as V_O. Lines 2 and 3 have the same delay time; therefore, the two aforementioned increments arrive at the output simultaneously at time 5T on the lattice diagram *(Figure 15)*.

In the general case of series lines with different delay times, the vertical lines on the lattice diagram should be spaced apart in the ratio of the respective delays. *Figure 16* shows this for a hypothetical case with delay ratios 1:2:3. For a sequence of transmission lines with the highest impedance line in the middle, at least three output voltage increments with the same polarity as V_O occur before one can occur of opposite polarity. On the other hand, if the middle line has the lowest impedance, the polarity of the second increment of output voltage is the opposite of V_O. The third increment of output voltage has the opposite polarity, for the time delay ratios of *Figure 16*.

When transmitting logic signals, it is important that the initial step of line output voltage pass through the threshold region of the receiving circuit, and that the next two increments of output voltage augment the initial step. Thus in a series terminated sequence of three mismatched lines, the middle line should have the highest impedance.



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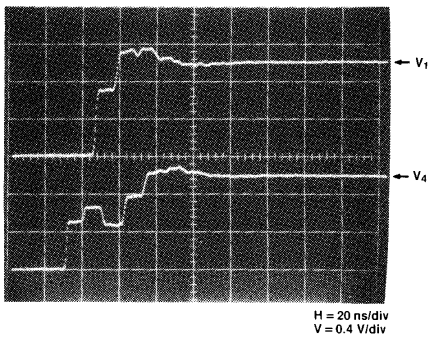

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FIGURE 14. Reflections from Mismatched Lines

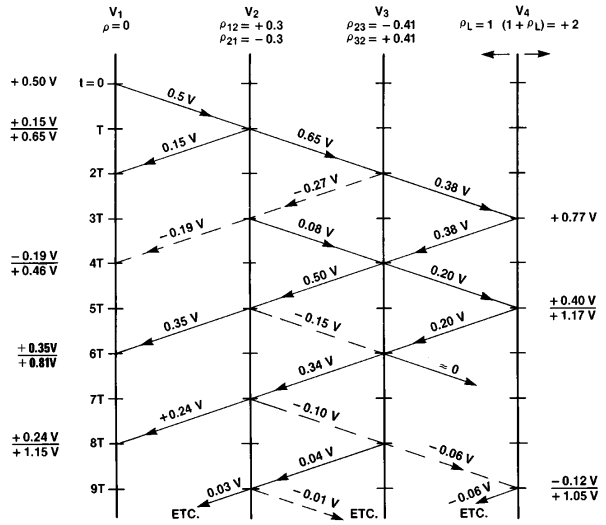

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FIGURE 15. Lattice Diagram for the Circuit of *Figure 14*

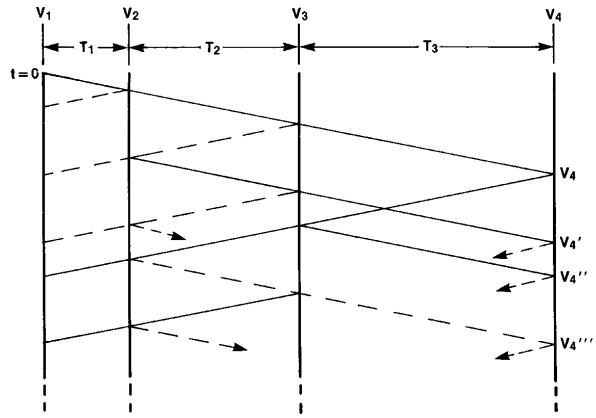

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FIGURE 16. Lattice Diagram for Three Lines with Delay Ratios 1:2:3

RISE TIME VERSUS LINE DELAY

When the 2-way line delay is less than the rise time of the input wave, any reflections generated at the end of the line are returned to the source before the input transition is completed. Assuming that the generator has a finite source resistance, the reflected wave adds algebraically to the input wave while it is still in transition, thereby changing the shape of the input. This effect is illustrated in *Figure 17*, which shows input and output voltages for several comparative values of rise time and line delay.

In *Figure 17b* where the rise time is much shorter than the line delay, V_1 rises to an initial value of 1V. At time T later, V_T rises to 0.5V, i.e., $1 + \rho_L = 0.5$. The negative reflection arrives back at the source at time 2T, causing a net change of -0.4V, i.e., $(1 + \rho_S)(-0.5) = -0.4$.

The negative coefficient at the source changes the polarity of the other 0.1V of the reflection and returns it to the end of the line, causing V_T to go positive by another 50 mV at time 3T. The remaining 50 mV is inverted and reflected back to the source, where its effect is barely distinguishable as a small negative change at time 4T.

In *Figure 17c*, the input rise time (0% to 100%) is increased to such an extent that the input ramp ends just as the negative reflection arrives back at the source end. Thus the input rise time is equal to 2T.

The input rise time is increased to 4T in *Figure 17d*, with the negative reflection causing a noticeable change in input slope at about its midpoint. This change in slope is more visible in the double exposure photo of *Figure 17e*, which shows V_1 (t_r still set for 4T) with and without the negative reflection. The reflection was eliminated by terminating the line in its characteristic impedance.

The net input voltage at any particular time is determined by adding the reflection to the otherwise unaffected input. It must be remembered that the reflection arriving back at the input at a given time is proportional to the input voltage at a time 2T earlier. The value of V_1 in *Figure 17d* can be calculated by starting with the 1V input ramp.

$$V_1 = \frac{1}{t_r} \bullet t \quad \text{for } 0 \le t \le 4T \qquad \text{(eq. 23)}$$

$$= 1V \quad \text{for } t \ge 4T$$

The reflection from the end of the line is

$$V_r = \frac{\rho_L (t - 2T)}{t_r}; \qquad \text{(eq. 24)}$$

the portion of the reflection that appears at the input is

$$V'_r = \frac{(1 + \rho_S)\,\rho_L (t - 2T)}{t_r}; \qquad \text{(eq. 25)}$$

the net value of the input voltage is the sum.

$$V'_1 = \frac{t}{t_r} + \frac{(1 + \rho_S) + \rho_L (t - 2T)}{t_r} \qquad \text{(eq. 26)}$$

The peak value of the input voltage in *Figure 17d* is determined by substituting values and letting t equal 4T.

$$V'_1 = 1 + \frac{(0.8)(-0.5)(4T - 2T)}{t_r} \qquad \text{(eq. 27)}$$

$$= 1 - 0.4\,(0.5) = 0.8V$$

After this peak point, the input ramp is no longer increasing but the reflection is still arriving. Hence the net value of the input voltage decreases. In this example, the later reflections are too small to be detected and the input voltage is thus stable after time 6T. For the general case of repeated reflections, the net voltage $V_{1(t)}$ seen at the driven end of the line can be expressed as follows, where the signal caused by the generator is $V_{1(t)}$.

$$V'_{1(t)} = V_{1(t)} \quad \text{for } 0 < t < 2T$$

$$V'_{1(t)} = V_{1(t)} + (1 + \rho_S)\,\rho_L\,V_{1(t-2T)} \quad \text{for } 2T < t < 4T$$

$$V'_{1(t)} = V_{1(t)} + (1 + \rho_S)\,\rho_L\,V_{1(t-2T)} + (1 + \rho_S)\,\rho_S\rho_L^2\,V_{1(t-4T)} \quad \text{for } 4T < t < 6T \qquad \text{(eq. 28)}$$

$$V'_{1(t)} = V_{1(t)} + (1 + \rho_S)\,\rho_L\,V_{1(t-2T)} + (1 + \rho_S)\,\rho_S\rho_L^2\,V_{1(t-4T)} + (1 + \rho_S)\,\rho_S^2\rho_L^3\,V_{1(t-6T)} \quad \text{for } 6T < t < 8T, \text{ etc.}$$

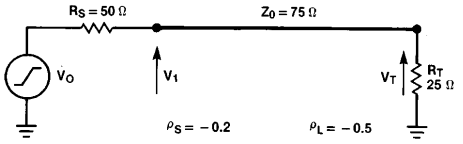
The voltage at the output end of the line is expressed in a similar manner.

$$V_{T(t)} = 0 \quad \text{for } 0 < t < T$$

$$V_{T(t)} = (1 + \rho_L)\,V_{1(t-T)} \quad \text{for } T < t < 3T$$

$$V_{T(t)} = (1 + \rho_L)\,V_{1(t-T)} + (1 + \rho_L)\,\rho_S\rho_L\,V_{1(t-3T)} \quad \text{for } 3T < t < 5T \qquad \text{(eq. 29)}$$

$$V_{T(t)} = (1 + \rho_L)\,V_{1(t-T)} + (1 + \rho_L)\,\rho_S\rho_L V_{1(t-3T)} + (1 + \rho_L)\,\rho_S^2\rho_L^2\,V_{1(t-5T)} \quad \text{for } 5T < t < 7T, \text{ etc.}$$



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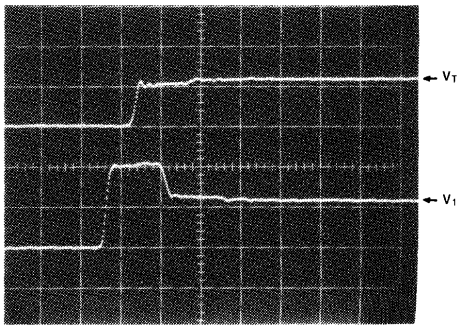
a. Test Arrangement for Rise Time Analysis



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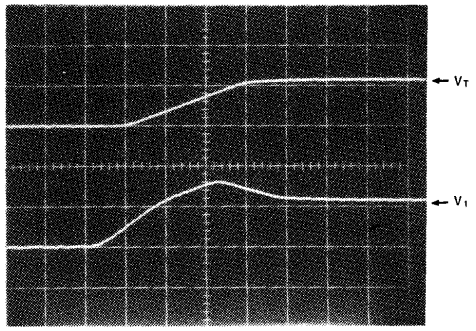
b. Line Voltages for $t_r \ll T$



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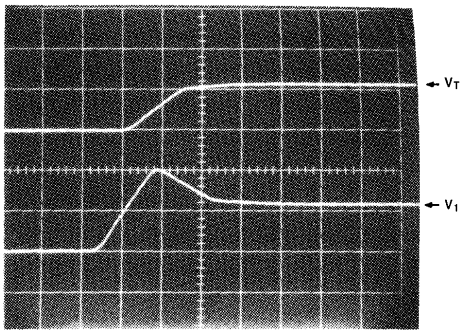
d. Line Voltages for $t_r = 4T$



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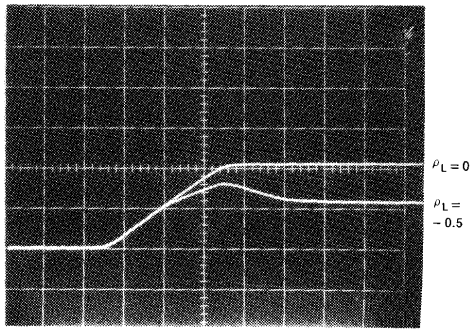
c. Line Voltages for $t_r = 2T$



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e. Input Voltage with and without Reflection

FIGURE 17. Line Voltages for Various Ratios of Rise Time to Line Delay

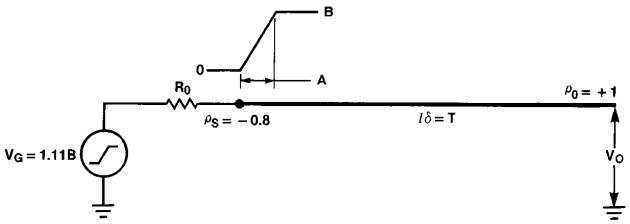
RINGING

Multiple reflections occur on a transmission line when neither the signal source impedance nor the termination (load) impedance matches the line impedance. When the source reflection coefficient ρ_S and the load reflection coefficient ρ_L are of opposite polarity, the reflections alternate in polarity. This causes the signal voltage to oscillate about the final steady state value, commonly recognized as ringing.

When the signal rise time is long compared to the line delay, the signal shape is distorted because the individual reflections overlap in time. The basic relationships among rise time, line delay, overshoot and undershoot are shown in a simplified diagram, *Figure 18*. The incident wave is a ramp of amplitude B and rise duration A. The reflection coefficient at the open-ended line output is $+1$ and the source reflection coefficient is assumed to be -0.8, i.e., $R_0 = Z_0/9$.

Figure 18b shows the individual reflections treated separately. Rise time A is assumed to be three times the line delay T. The time scale reference is the line output and the first increment of output voltage V_O rises to 2B in the time interval A. Simultaneously, a positive reflection (not shown) of amplitude B is generated and travels to the source, whereupon it is multiplied by -0.8 and returns toward the end of the line. This negative-going ramp starts at time 2T (twice the line delay) and doubles to -1.6B at time 2T + A.

The negative-going increment also generates a reflection of amplitude -0.8B which makes the round trip to the source and back, appearing at time 4T as a positive ramp rising to $+1.28$B at time 4T + A. The process of reflection and re-reflection continues, and each successive increment changes in polarity and has an amplitude of 80% of the preceding increment.



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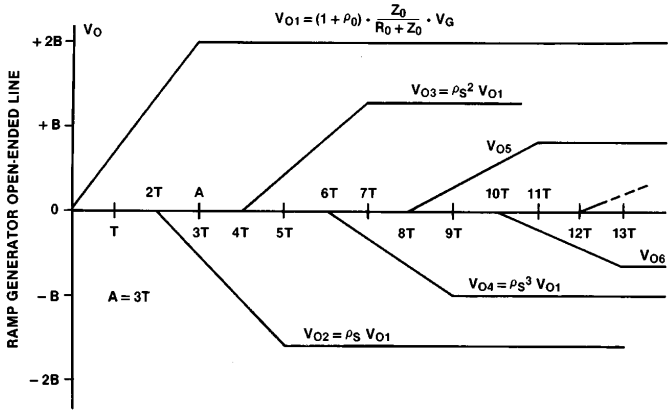
a. Ramp Generator Driving Open-Ended Line



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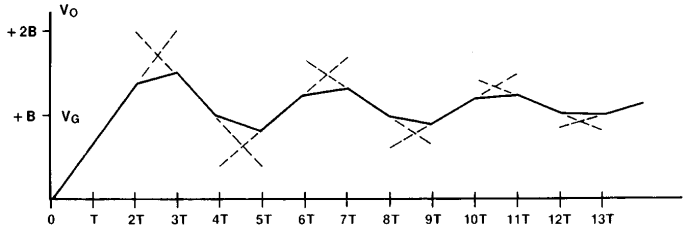
b. Increments of Output Voltage Treated Individually



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c. Net Output Signal Determined by Superposition

FIGURE 18. Basic Relationships Involved in Ringing

In *Figure 18c*, the output increments are added algebraically by superposition. The starting point of each increment is shifted upward to a voltage value equal to the algebraic sum of the quiescent levels of all the preceding increments (i.e., 0, 2B, 0.4B, 1.68B, etc.). For time intervals when two ramps occur simultaneously, the two linear functions add to produce a third ramp that prevails during the overlap time of the two increments.

It is apparent from the geometric relationships, that if the ramp time A is less than twice the line delay, the first output increment has time to rise to the full 2B amplitude and the second increment reduces the net output voltage to 0.4B. Conversely, if the line delay is very short compared to the ramp time, the excursions about the final value V_G are small.

Figure 18c shows that the peak of each excursion is reached when the earlier of the two constituent ramps reaches its maximum value, with the result that the first peak occurs at time A. This is because the earlier ramp has a greater slope (absolute value) than the one that follows.

Actual waveforms such as produced by ECL or TTL do not have a constant slope and do not start and stop as abruptly as the ramp used in the example of *Figure 18*. Predicting the time at which the peaks of overshoot and undershoot occur is not as simple as with ramp excitation. A more rigorous treatment is required, including an expression for the driving waveform which closely simulates its actual shape. In the general case, a peak occurs when the sum of the slopes of the individual signal increment is zero.

SUMMARY

The foregoing discussions are by no means an exhaustive treatment of transmission line characteristics. Rather, they are intended to focus attention on the general methods used to determine the interactions between high-speed logic circuits and their interconnections. Considering an interconnection in terms of distributed rather than lumped inductance and capacitance leads to the line impedance concept, i.e., mismatch between this characteristic impedance and the terminations causes reflections and ringing.

Series termination provides a means of absorbing reflections when it is likely that discontinuities and/or line impedance changes will be encountered. A disadvantage is that the incident wave is only one-half the signal swing, which limits load placement to the end of the line. ECL input capacitance increases the rise time at the end of the line, thus increasing the effective delay. With parallel termination, i.e., at the end of the line, loads can be distributed along the line. ECL input capacitance modifies the line characteristics and should be taken into account when determining line delay.

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2. Skilling, H., *Electric Transmission Lines*, McGraw-Hill, (1951).
3. Matick, R., *Transmission Lines for Digital and Communication Networks*, McGraw-Hill, (1969).
4. Millman, J. and Taub, H., *Pulse Digital and Switching Waveforms*, McGraw-Hill, (1965).
5. ''Time Domain Reflectometry'', *Hewlett-Packard Journal*, Vol. 15, No. 6, (February 1964).
6. Feller, A., Kaupp H., and Digiacoma, J., ''Crosstalk and Reflections in High-Speed Digital Systems'', *Proceedings, Fall Joint Computer Conference*, (1965).

APPENDIX B
ECL DESIGN GUIDE: SYSTEM CONSIDERATIONS

INTRODUCTION

All of National's ECL input and output impedances are designed to accommodate various methods of driving and terminating interconnections. Controlled wiring impedance makes it possible to use simplified equivalent circuits to determine limiting conditions. Specific guidelines and recommendations are based on assumed worst-case combinations. Many of the recommendations may seem conservative, compared to typical observations, but the intent is to help the designer achieve a reliable system in a reasonable length of time with a minimum amount of redesign.

PC BOARD TRANSMISSION LINES

Strictly speaking, transmission lines are not always required for F100K ECL but, when used, they provide the advantages of predictable interconnect delays as well as reflection and ringing control through impedance matching. Two common types of PC board transmission lines are microstrip and stripline, *Figure 1*. Stripline requires multilayer construction techniques; microstrip uses ordinary double-clad boards. Other board construction techniques are wire wrap, stitch weld and discrete wired.

Stripline, *Figure 1b*, is used where packing density is a high priority because increasing the interconnect layers provides short signal paths. Boards with as many as 14 layers have been used in ECL systems.

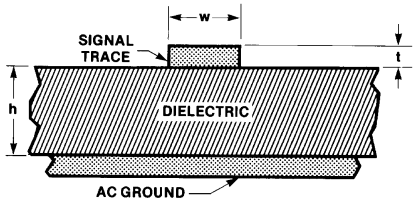
Microstrip offers easier fabrication and higher propagation velocity than stripline, but the routing for a complex system may require more design effort. In *Figure 1a*, the ground plane can be a part of the V_{EE} distribution as long as adequate bypassing from V_{EE} to V_{CC} (ground) is provided. Also, signal routing is simplified and an extra voltage plane is obtained by bonding two microstrip structures back to back, *Figure 1c*.

Microstrip

Equation 1 relates microstrip characteristic impedance to the dielectric constant and dimensions.[1] Electric field fringing requires that the ground extend beyond each edge of the signal trace by a distance no less than the trace width.

$$Z_0 = \left(\frac{60}{\sqrt{0.475\,\epsilon_r + 0.67}}\right) \ln\left(\frac{4h}{0.67\,(0.8\,w + t)}\right) = \left(\frac{87}{\sqrt{\epsilon_r + 1.41}}\right) \ln\left(\frac{5.98\,h}{0.8\,w + t}\right) \quad \text{(eq. 1)}$$

where h = dielectric thickness, w = trace width, t = trace thickness, ϵ_r = board material dielectric constant relative to air.



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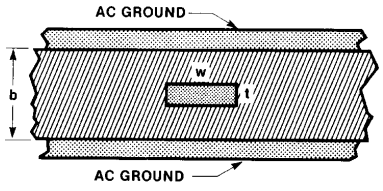
a. Microstrip



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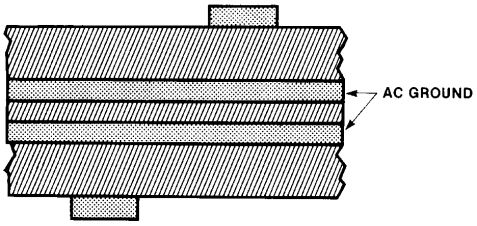
b. Stripline



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c. Composite Microstrip

FIGURE 1. Transmission Lines on Circuit Boards

Equation 1 was developed from the impedance formula for a wire over ground plane transmission line, Equation 2.

$$Z_0 = \left(\frac{60}{\sqrt{\epsilon_r}}\right) \ln\left(\frac{4h}{d}\right) \quad \text{(eq. 2)}$$

where d = wire diameter, h = distance from ground to wire center.

Comparing Equation 1 and 2, the term 0.67 (0.8 w + t) shows the equivalence between a round wire and a rectangular conductor. The term 0.475 ϵ_r + 0.67 is the *effective* dielectric constant for microstrip ϵ_e, considering that a microstrip line has a compound dielectric consisting of the board material and air. The effective dielectric constant is determined by measuring propagation delay per unit of line length and using the following relationship.

$$\delta = 1.016 \bullet \sqrt{\epsilon_e}\ \text{ns/ft} \quad \text{(eq. 3)}$$

where δ = propagation delay, ns/ft.

Propagation delay is a property of the dielectric material rather than line width or spacing. The coefficient 1.016 is the reciprocal of the velocity of light in free space. Propagation delay for microstrip lines on glass-filled G-10 epoxy boards is typically 1.77 ns/ft, yielding an effective dielectric constant of 3.04.

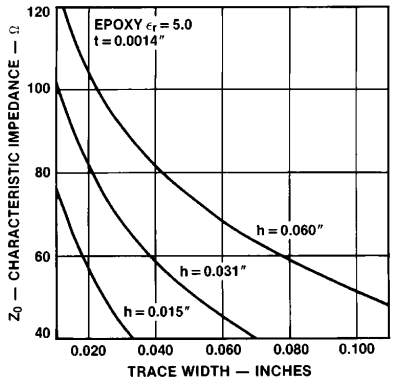

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FIGURE 2. Microstrip Impedance Versus Trace Width, G-10 Epoxy

Using ϵ_r = 5.0 in Equation 1, *Figure 2* provides microstrip line impedance as a function of width for several G-10 epoxy board thicknesses. *Figure 3* shows the related C_0 values, useful for determining capacitive loading effects on line characteristics, (Equation 15).

System designers should ascertain tolerances on board dimensions, dielectric constant and trace width etching in order to determine impedance variations. If conformal coating is used the effective dielectric constant of microstrip is increased, depending on the coating material and thickness.

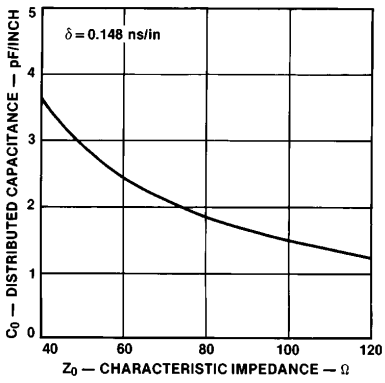

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FIGURE 3. Microstrip Distributed Capacitance Versus Impedance, G-10 Epoxy

Stripline

Stripline conductors are totally embedded. As a result, the board material determines the dielectric constant. G-10 epoxy boards have a typical propagation delay of 2.26 ns/ft. Equation 4 is used to calculate stripline impedances.[1,2]

$$Z_0 = \left(\frac{60}{\sqrt{\epsilon_r}}\right) \ln\left(\frac{4b}{0.67\,\pi\,(0.8\,w + t)}\right) \quad \text{(eq. 4)}$$

where b = distance between ground planes, w = trace width, t = trace thickness, w/(b-t) < 0.35 and t/b < 0.25.

Figure 4 shows stripline impedance as a function of trace width, using Equation 4 and various ground plane separations for G-10 glass-filled epoxy boards. Related values of C_0 are plotted in *Figure 5*.

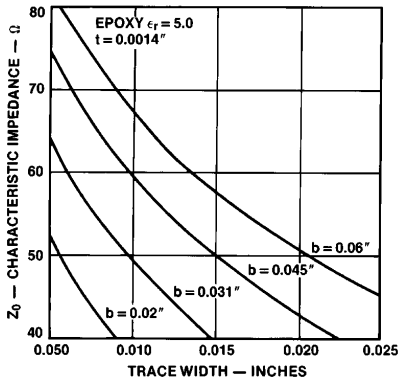

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FIGURE 4. Stripline Impedance Versus Trace Width, G-10 Epoxy

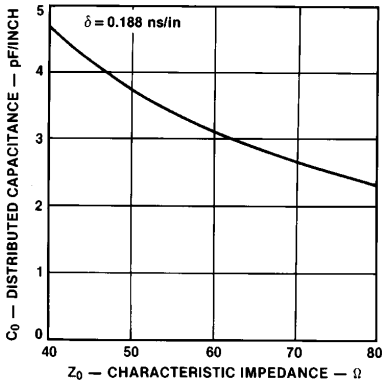

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FIGURE 5. Stripline Distributed Capacitance Versus Impedance, G-10 Epoxy

Wire Wrap

Wire-wrap boards are commercially available with three voltage planes, positions for several 24-pin Dual-In-Line Packages (DIP), terminating resistors, and decoupling capacitors. The devices are mounted on socket pins and interconnected with twisted pair wiring. One wire at each end of the twisted pair is wrapped around a signal pin, the other around a ground pin. The #30 insulated wire is uniformly twisted to provide a nominal 93Ω impedance line. Positions for Single-In-Line Package (SIP) terminating resistors are close to the inputs to provide good termination characteristics.

Stitch Weld

Stitch-weld boards are commercially available with three voltage planes and buried resistors between planes. The devices are mounted on terminals and interconnected with insulated wires that are welded to the backside of the terminals. The insulated wires are placed on a controlled thickness over the ground plane to provide a nominal impedance of 50Ω. The boards are available for both DIPs and flatpaks. Use of flatpaks can increase package density and provide higher system performance.

Discrete Wired

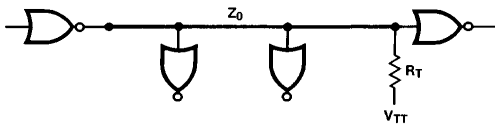
Custom Multiwire* boards are available with integral power and ground planes. Wire is placed on a controlled thickness above the ground plane to obtain a nominal impedance line of 55Ω. Then holes are drilled through the wire and board. Copper is deposited in the drilled holes by an additive-electrolysis process which bonds each wire to the wall of the holes. Devices are soldered on the board to make connection to the wires.

*Multiwire is a registered trademark of the Multiwire Corporation.

Parallel Termination

Terminating a line at the receiving end with a resistance equal to the characteristic line impedance is called parallel termination, *Figure 6a.* F100K circuits do not have internal pull-down resistors on outputs, so the terminating resistor must be returned to a voltage more negative than V_{OL} to establish the LOW-state output voltage from the emitter follower. A −2V termination return supply is commonly used. This minimizes power consumption and correlates with standard test specifications for ECL circuits. A pair of resistors connected in series between ground (V_{CC}) and the V_{EE} supply can provide the Thevenin equivalent of a single resistor to −2V if a separate termination supply is not available, *Figure 6b*. The average power dissipation in the Thevenin equivalent resistors is about 10 times the power dissipation in the single resistor returned to −2V, as shown in *Figures 10* and *13*. For either parallel termination method, decoupling capacitors are required between the supply and ground (Chapter 6).

a. Parallel Termination



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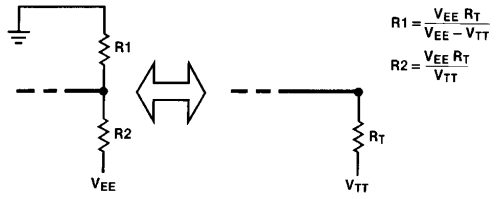
b. Thevenin Equivalent of R_T and V_{TT}



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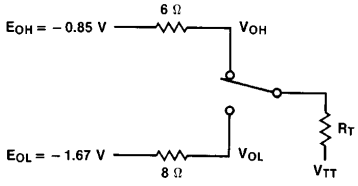
c. Equivalent Circuit for Determining Approximate V_{OH} and V_{OL} Levels



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d. F100K Output Characteristic with Terminating Resistor R_T Returned to V_{TT} = −2.0V

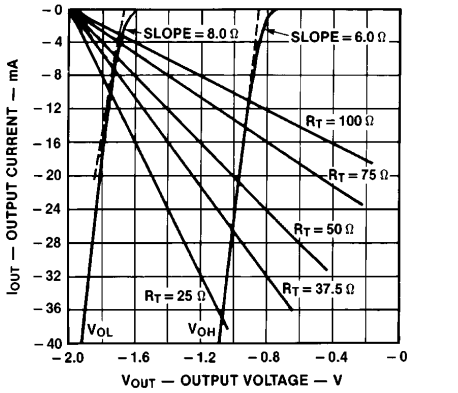

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FIGURE 6. Parallel Termination

F100K output transistors are designed to drive low-impedance loads and have a maximum output current rating of 50 mA. The circuits are specified and tested with a 50Ω load returned to −2V. This gives nominal output levels of −0.955V at 20.9 mA and −1.705V at 5.9 mA. Output levels will be different with other load currents because of the transistor output resistance. This resistance is nonlinear with load current since it is due, in part, to the base-emitter voltage of the emitter follower, which is logarithmic with output current. With the standard 50Ω load, the effective source resistance is approximately 6Ω in the HIGH state and 8Ω in the LOW state.

The foregoing values of output voltage, output current, and output resistance are used to estimate quiescent output levels with different loads. An equivalent circuit is shown in *Figure 6c*. The ECL circuit is assumed to contain two internal voltage sources E_{OH} and E_{OL} with series resistances of 6Ω and 8Ω respectively. The values shown for E_{OH} and E_{OL} are −0.85V and −1.67V respectively.

The linearized portion of the F100K output characteristic can be represented by two equations:

For V_{OH}: $V_{OUT} = -850 - 6\ I_{OUT}$
For V_{OL}: $V_{OUT} = -1670 - 8\ I_{OUT}$

where I_{OUT} is in mA, V_{OUT} is in mV.

If the range of I_{OUT} is confined between 8 mA to 40 mA for V_{OH}, and 2 mA to 16 mA for V_{OL}, the output voltage can be estimated within ±10 mV *(Figure 6d)*.

An ECL output can drive two or more lines in parallel, provided the maximum rated current is not exceeded. Another consideration is the effect of various loads on noise margins. For example, two parallel 75Ω terminations to −2V *(Figure 6d)* give output levels of approximately −1.000V and −1.716V. Noise margins are thus 35 mV less in the HIGH state and 11 mV more in the LOW state, compared to 50Ω load conditions. Conversely, a single 75Ω load to −2V causes noise margins 38 mV greater in the HIGH state and 11 mV less in the Low state, compared to a 50Ω load.

The magnitude of reflections from the terminated end of the line depends on how well the termination resistance R_T matches the line impedance Z_O. The ratio of the reflected voltage to the incident voltage V_i is the reflection coefficient ρ.

$$\frac{V_r}{V_i} = \rho = \frac{R_T - Z_0}{R_T + Z_0} \qquad \text{(eq. 5)}$$

The initial signal swing at the termination is the sum of the incident and reflected voltages. The ratio of termination signal to incident signal is thus:

$$\frac{V_T}{V_i} = 1 + \rho = \frac{2R_T}{R_T + Z_0} \qquad \text{(eq. 6)}$$

The degree of reflections which can be tolerated varies in different situations, but to allow for worst-case circuits, a good rule of thumb is to limit reflections to 15% to prevent excursions into the threshold region of the ECL inputs connected along the line. The range of permissible values of R_T as a function of Z_0 and the reflection coefficient limitations can be determined by rearranging Equation 5.

$$R_T = Z_0 \frac{1 + \rho}{1 - \rho} \qquad \text{(eq. 7)}$$

Using 15% reflection limits as examples, the range of the R_T/Z_0 ratio is as follows.

$$\frac{1.15}{0.85} > \frac{R_T}{Z_0} > \frac{0.85}{1.15} \quad 1.35 > \frac{R_T}{Z_0} > 0.74 \qquad \text{(eq. 8)}$$

The permissible range of the R_T/Z_0 ratio determines the tolerance ranges for R_T and Z_0. For example, using the foregoing ratio limits, R_T tolerances of ±10% allow Z_0 tolerance limits of +22% and −19%; R_T tolerances of ±5% allow Z_0 tolerance limits of +28% and −23%.

An additional requirement on the maximum value of R_T is related to the value of quiescent I_{OH} current needed to insure sufficient negative-going signal swing when the ECL driver switches from the HIGH state to the LOW state. The npn emitter-follower output of the ECL circuit cannot act as a voltage source driver for negative-going transitions. When the voltage at the base of the emitter follower starts going negative as a result of an internal state change, the output current of the emitter follower starts to decrease. The transmission line responds to the decrease in current by producing a negative-going change in voltage. The ratio of the voltage change to the current change is, of course, the characteristic impedance Z_0. Since the maximum decrease in current that the line can experience is from I_{OH} to zero, the maximum negative-going transition which can be produced is the product $I_{OH}\ Z_0$.

If the $I_{OH}\ Z_0$ product is greater than the normal negative-going signal swing, the emitter follower responds by limiting the current change, thereby controlling the signal swing. If, however, the $I_{OH}\ Z_0$ product is too small, the emitter follower is momentarily turned off due to insufficient forward bias of its base-emitter junctions, causing a discontinuous negative-going edge such as the one shown in *Figure 14*. In the output-LOW state the emitter follower is essentially nonconducting for V_{OL} values more positive than about −1.55V. Using this value as a criterion and expressing I_{OH} and V_{OH} in terms of the equivalent circuit of *Figure 6c*, an upper limit on the value of R_T can be developed.

$$\Delta V = I_{OH} Z_0 > 1.55 - |V_{OH}|$$

$$\left(\frac{E_{OH} - V_{TT}}{R_0 + R_T}\right) Z_0 > 1.55 - \left|\frac{V_{TT}\ R_0 = E_{OH} R_T}{R_0 + R_T}\right|$$

$$R_T < \frac{(E_{OH} - V_{TT})\ Z_0 - (1.55 - |V_{TT}|)\ R_0}{1.55 - |E_{OH}|} \qquad \text{(eq. 9)}$$

For a V_{TT} of −2V, R_0 of 6Ω and E_{OH} of −0.85V, Equation 4-9 reduces to

$R_T < 1.64\ Z_0 + 3.86\Omega$

For $Z_0 = 50\Omega$, the emitter follower cuts off during a negative-going transition if R_T exceeds 86Ω. Changing the voltage level criteria to −1.60V to insure continuous conduction in the emitter follower gives an upper limit of 77Ω for a 50Ω line. For a line terminated at the receiving end with a resistance to −2V, a rough rule-of-thumb is that termination resistance should not exceed line impedance by more than 50%. This insures a satisfactory negative-going signal swing to ECL inputs connected along the line. The quiescent V_{OL} level, after all reflections have damped out, is determined by R_T and the ECL output characteristic.

INPUT IMPEDANCE

The input impedance of ECL circuits is predominately capacitive. A single-function input has an effective value of about 1.5 pF for F100K flatpak, as determined by its effect on reflected and transmitted signals on transmission lines.

In practical calculations, a value of 2 pF should be used. Approximately one third of this capacitance is attributed to the internal circuitry and two thirds to the flatpak pin and internal bonding.

For F100K flatpak circuits, multiple input lines may appear to have up to 3 pF to 4 pF but never more. For example, in the F100102, an input is connected internally to all five gates, but because of the philosophy of buffering these types of inputs in the F100K family this input appears as a unit load with a capacitance of approximately 2 pF. For applications such as a data bus, with two or more outputs connected to the same line, the capacitance of a passive-LOW output can be taken as 2 pF.

Capacitive loads connected along a transmission line increase the propagation delay of a signal along the line. The modified delay can be determined by treating the load capacitance as an increase in the intrinsic distributed capacitance of the line, discussed in Chapter 3. The intrinsic capacitance of any stubs which connect the inputs to the line should be included in the load capacitance. The intrinsic capacitance per unit length for G-10 epoxy boards is shown in *Figure 3* and *5* for microstrip and stripline respectively. For other dielectric materials, the intrinsic capacitance C_0 can be determined by dividing the intrinsic delay δ (Equation 3) by the line impedance Z_0.

The length of a stub branching off the line to connect an input should be limited to insure that the signal continuing along the line past the stub has a continuous rise, as opposed to a rise (or fall) with several partial steps. The point where a stub branches off the line is a low impedance point. This creates a negative coefficient of reflection, which in turn reduces the amplitude of the incident wave as it continues beyond the branch point. If the stub length is short enough, however, the first reflection returning from the end of the stub adds to the attenuated incident wave while it is still rising. The sum of the attenuated incident wave and the first stub reflection provides a step-free signal, although its rise time will be longer than that of the original signal. Satisfactory signal transitions can be assured by restricting stub lengths according to the recommendations for unterminated lines *(Figure 10)*. The same considerations apply when the termination resistance is not connected at the end of the line; a section of line continuing beyond the termination resistance should be treated as an unterminated line and its length restricted accordingly.

SERIES TERMINATION

Series termination requires a resistor between the driver and transmission line, *Figure 7*. The receiving end of the line has no termination resistance. The series resistor value should be selected so that when added to the driver source resistance, the total resistance equals the line impedance. The voltage divider action between the net series resistance and the line impedance causes an incident wave of half amplitude to start down the line. When the signal arrives at the unterminated end of the line, it doubles and is thus restored to a full amplitude. Any reflections returning to the source are absorbed without further reflection since the line and source impedance match. This feature, source absorption, makes series termination attractive for interconnection paths involving impedance discontinuities, such as occur in backplane wiring.

A disadvantage of series termination is that driven inputs must be near the end of the line to avoid receiving a 2-step signal. The initial signal at the driver end is half amplitude, rising to full amplitude only after the reflection returns from the open end of the line. In *Figure 7*, one load is shown connected at point D, aways from the line end. This input receives a full amplitude signal with a continuous edge if the distance l to the open end of the line is within recommended lengths for unterminated line *(Figure 10)*.

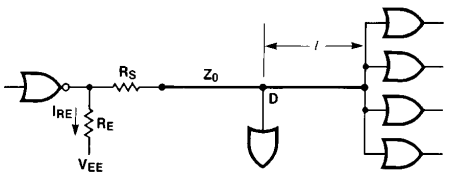

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FIGURE 7. Series Termination

The signal at the end has a slower rise time that the incident wave because of capacitive loading. The increase in rise time to the 50% point effectively increases the line propagation delay, since the 50% point of the signal swing is the input signal timing reference point. This added delay as a function of the product line impedance and load capacitance is discussed in Chapter 3.

Quiescent V_{OH} and V_{OL} levels are established by resistor R_E *(Figure 7)*, which also acts with V_{EE} to provide the negative-going drive into R_S and Z_0 when the driver output goes to the LOW state. To determine the appropriate R_E value, the driver output can be treated as a simple mechanical switch which opens to initiate the negative-going swing. At this instant, Z_O acts as a linear resistor returned to V_{OH}. Thus the components form a simple circuit of R_E, R_S and Z_0 in a series, connected between V_{EE} and V_{OH}. The initial current in this series circuit must be sufficient to introduce a 0.38V transient into the line, which then doubles at the load end to give 0.75V swing.

$$I_{RE} = \frac{V_{OH} - V_{EE}}{R_E + P_S + Z_0} \geq \frac{0.38}{Z_0} \qquad \text{(eq. 10)}$$

Any I_{OH} current flowing in the line before the switch opens helps to generate the negative swing. This current may be quite small, however, and should be ignored when calculating R_E.

Increasing the minimum signal swing into the line by 30% to 0.49V insures sufficient pull-down current to handle reflection currents caused by impedance discontinuities and load capacitance. The appropriate R_E value is determined from the following relationship.

$$\frac{V_{OH} - V_{EE}}{R_E + R_S + Z_0} \geq \frac{0.49}{Z_0} \qquad \text{(eq. 11)}$$

For the R_E range normally used, quiescent V_{OH} averages approximately 0.955V and $V_{EE} = -4.5$V. The value of R_S is equal to Z_0 minus R_0 (R_0 averages 7Ω). Inserting these values and rearranging Equation 11 gives the following.

$$R_E \leq 5.23\, Z_0 + 7\Omega \qquad \text{(eq. 12)}$$

Power dissipation in R_E is listed in *Figure 14*. The power dissipation in R_E is greater than in R_T of a parallel termination to -2V, but still less than the two resistors of the Thevenin equivalent parallel termination, see *Figure 10, 13* and *14*.

The number of driven inputs on a series terminated line is limited by the voltage drop across R_S in the quiescent HIGH state, caused by the finite input currents of the ECL loads. I_{IH} values are specified on data sheets for various types of

inputs, with a worst-case value of 265 μA for simple gate inputs. The voltage drop subtracts from the HIGH-state noise margin as outlined in *Figure 8a*.

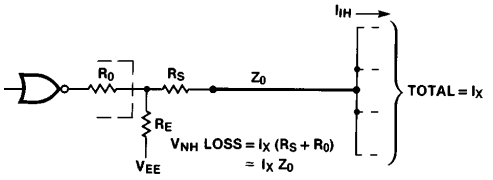
However, there is more HIGH-state noise margin initially, because there is less I_{OH} with the R_E load than with the standard 50Ω load to -2V. This makes V_{OH} more positive; the increase ranges from 43 mV for a 50Ω line to 82 mV for a 100Ω line. Using this V_{OH} increase as a limit on the voltage drop across R_S assures that the HIGH-state noise margin is as good as in the parallel terminated case. Dividing the V_{OH} increase by $R_S + R_0$ ($=Z_0$) gives the allowed load input current (Ix in *Figure 8a*). This works out to 0.86 mA for a 50Ω line, 0.92 mA for a 75Ω line and 0.82 mA for a 100Ω line. Load input current greater than these values can be tolerated at some sacrifice in noise margin. If, for example, an additional 50 mV loss is feasible, the maximum values of current become 1.86 mA, 1.59 mA and 1.32 mA for 50Ω, 75Ω and 100Ω lines respectively.

An ECL output can drive more than one series terminated line, as suggested in *Figure 8b*, if the maximum rated output current of 50 mA is not exceeded. Also, driving two or more lines requires a lower R_E value. This makes the quiescent I_{OH} higher and consequently V_{OH} lower, due to the voltage drop across R_0. This voltage drop decreases the HIGH-state noise margin, which may become the limiting factor (rather than the maximum rated current), depending on the particular application.

The appropriate R_E value can be determined using Equation 13 for $V_{EE} = -4.5$V.

$$\frac{1}{R_E} \geq \frac{1}{6.23\,Z_1 - R_{S1}} + \frac{1}{6.23\,Z_2 - R_{S2}} + \frac{1}{6.23\,Z_3 - T_{S3}} \qquad \text{(eq. 13)}$$

Circuits with multiple outputs (such as the F100112) provide an alternate means of driving several lines simultaneous *(Figure 8c)*. Note, each output should be treated individually when assiging load distribution, line impedance, and R_E value.



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a. Noise Margin Loss Due to Load Input Current

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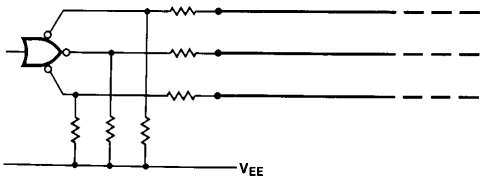
b. Driving Several Lines from one Output



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c. Using Multiple Output Element for Load Sharing

FIGURE 8. Loading Considerations for Series Termination

UNTERMINATED LINES

Lines can be used without series or parallel termination if the line delay is short compared to the signal rise time. Ringing occurs because the reflection coefficient at the open (receiving) end of the line is positive (nominally $+1$) while the reflection coefficient at the driving end is negative (approximately -0.8). These opposite polarity reflection coefficients cause any change in signal voltage to be reflected back and forth, with a polarity change each time the signal is reflected from the driver. Net voltage change on the line is thus a succession of increments with alternating polarity and decreasing magnitude. The algebraic sum of these increments if the observed ringing. The general relationships among rise time, line delay, overshoot and undershoot are discussed in Chapter 3, using simple waveforms for clarity.

Excessive overshoot on the positive-going edge of the signal drives input transistors into saturation. Although this does not damage an ECL input, it does cause excessive recovery times and makes propagation delays unpredictable. Undershoot (following the overshoot) must also be limited to prevent signal excursions into the threshold region of the loads. Such excursions could cause exaggerated transition times at the driven circuit outputs, and could also cause multiple triggering of sequential circuits. Signal swing, exclusive of ringing, is slightly greater on unterminated lines that on parallel terminated lines; I_{OH} is less and I_{OL} is greater with the R_E load, *(Figure 9a)* making V_{OH} higher and V_{OL} lower.

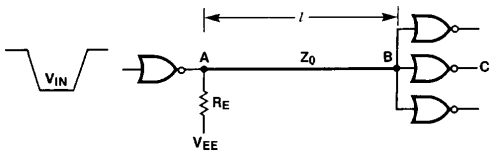
For worst case combinations of driver output and load input characteristics, a 35% overshoot limit insures that system speed is not compromised either by saturating an input on overshoot or extending into the threshold region on the following undershoot.

For distributed loading, ringing is satisfactorily controlled if the 2-way modified line delay does not exceed the 20% to 80% rise time of the driver output. This relationship can be expressed as follows, using the symbols from Chapter 3 and incorporating the effects of load capacitance on line delay.

$$t_r = 2T' = 2\ell\delta' = 2\ell\delta\sqrt{1 + \frac{C_L}{\ell C_0}}$$

Solving this expression for the line length (ℓ):

$$\ell_{max} = \frac{1}{2}\sqrt{\left(\frac{C_L}{C_0}\right)^2 + \left(\frac{t_r}{\delta}\right)^2} - \frac{C_L}{2C_0} \qquad \text{(eq. 14)}$$



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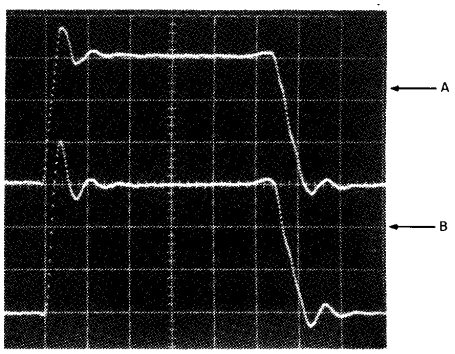
a. Unterminated Line



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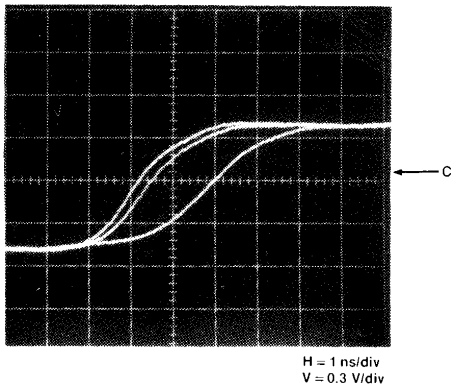
b. Line Voltages Showing Stair-step Trailing Edges



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c. Load Gate Output Showing Net Propagation Increase for Increasing Values of R_E: 330Ω, 510Ω, 1 kΩ

FIGURE 9. Effect on R_E Value on Trailing-Edge Propagation

The shorter the rise time, the shorter the premissible line length. For F100K ECL, the minimum rise time from 20% to 80% is specified as 0.5 ns. Using this rise time and 2 pF per fan-out load, calculated maximum line lengths for G-10 epoxy microstrip are listed in *Figure 10a*. The length (ℓ) in the table is the distance from the terminating resistor to the input of the device(s). For F100K ECL the case described in *Figure 10a* is the only one calculated, since all other combinations are approximately the same. For other combinations of rise time, impedance, fan-out or line characteristics (δ and C_0), maximum lengths are calculated using Equation 14. For the convenience of those who are also using 10K ECL, maximum recommended lengths of unterminated lines are listed in *Figure 10b* to *10e*.

Z_0	Number of Fan-Out Loads			
	1	2	3	4
50	1.37*	1.13	0.95	0.81
62	1.33	1.07	0.87	0.70
75	1.25	0.95	0.75	0.61
90	1.18	0.85	0.66	0.53
100	1.15	0.82	0.61	0.49

*Length in inches.
Unit load = 2 pF, δ = 0.148 ns/inch

FIGURE 10a. F100K Maximum Worst-Case Line Lengths for Unterminated Microstrip, Distributed Loading

Z_0	Number of Fan-Out Loads				
	2	3	4	6	8
50	4.15*	3.75	3.45	2.85	2.45
62	3.95	3.50	3.15	2.55	2.10
75	3.75	3.25	2.85	2.25	1.85
90	3.55	3.00	2.60	2.00	1.60
100	3.45	2.85	2.45	1.85	1.45

*Length in inches.
Unit load = 3 pF, δ = 0.148 ns/in.

FIGURE 10b. 10K Maximum Worst-Case Line Lengths for Unterminated Microstrip, Distributed Loading

Z_0	Number of Fan-Out Loads				
	1	2	4	6	8
50	4.40*	3.65	2.60	1.90	1.40
62	4.30	3.45	2.30	1.60	1.15
75	4.20	3.20	2.05	1.40	0.95
90	4.05	2.95	1.75	1.05	0.65
100	3.90	2.80	1.60	0.90	0.50

*Length in inches.
Unit load = 3 pF, δ = 0.148 ns/in.

FIGURE 10c. 10K Maximum Worst-Case Line Lengths for Unterminated Microstrip, Concentrated Loading

Z_0	Number of Fan-Out Loads				
	2	3	4	6	8
50	3.30*	3.00	2.70	2.25	2.90
62	3.15	2.80	2.50	2.00	1.65
75	3.00	2.60	2.25	1.80	1.45
90	2.80	2.40	2.05	1.55	1.25

*Length in inches.
Unit load = 3 pF, δ = 0.188 ns/in.

FIGURE 10d. 10K Maximum Worst-Case Line Lengths for Unterminated Stripline, Distributed Loading

Z_0	Number of Fan-Out Loads				
	1	2	4	6	8
50	3.45*	2.85	2.00	1.50	1.10
62	3.40	2.70	1.80	1.30	0.90
75	3.30	2.55	1.60	1.10	0.75
90	3.15	2.35	1.40	0.85	0.50
100	3.10	2.20	1.25	0.70	0.40

*Length in inches.
Unit load = 3 pF, δ = 0.188 ns/in.

FIGURE 10e. 10K Maximum Worst-Case Line Lengths for Unterminated Stripline, Concentrated Loading

A load capacitance concentrated at the end of the line restricts line length more than a distributed load does. Maximum recommended lengths for fiberglass epoxy dielectric and a 0.5 ns rise time are listed in *Figure 10* for microstrip. For line impedances not listed, linear interpolation can be used to determine appropriate line lengths. Appropriate line lengths for dielectric materials with a different propagation constant δ can be determined by multiplying the listed values by the fiberglass epoxy δ and then dividing by the δ of the other material. For example, a line length for a material which has a microstrip δ of 0.1 ns/inch is determined by multiplying the length given in the microstrip table (for a desired impedance and load) by 0.148 and dividing by 0.1.

Resistor R_E must provide the current for the negative-going signal at the driver output. Line input and output waveforms are noticeably affected if R_E is too large, as shown in *Figure 9b*. The negative-going edge of the signal falls in stair-step fashion, with three distinct steps visible at point A. The waveform at point B shows a step in the middle of the negative-going swing. The effect of different R_E values on the net propagation time through the line and the driven loads is evident in *Figure 9c* which shows the output signal of one driven gate in a multiple exposure photograph. The horizontal sweep (time axis) was held constant with respect to the input signal of the driver. The earliest of the three output signals occurs with an R_E value of 330Ω. Changing R_E to 510Ω increases the net propagation delay by 0.3 ns, the horizontal offset between the first and second signals. Changing R_E to 1 kΩ produces a much greater increase in net propagation delay, indicating that the negative-going signal at B contains several steps. In practice, a satisfactory negative-going signal results when the R_E value is chosen to give an initial negative-going step of 0.6V at the driving end of the line. This gives an upper limit on the value of R_E, as shown in Equation 15.

$$\text{initial step} = \Delta \ell \bullet Z_0 = \frac{(V_{OH} - V_{EE})\, Z_0}{R_E + Z_0} \geq 0.6$$

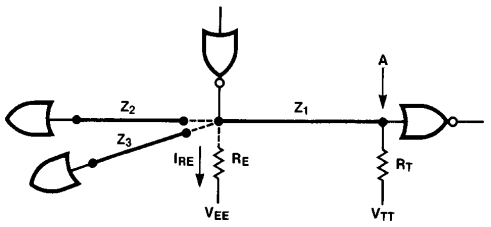
$$R_E = \leq 6.25\, Z_0 \qquad \text{(eq. 15)}$$

An ECL output can drive two or more unterminated lines, provided each line length and loading combination is within the recommended constraints. The appropriate R_E value is determined from Equation 15, using the parallel impedance of the two or more lines for Z_0.

An ECL output can simultaneously drive terminated and unterminated lines, although the negative-going edge of the signal shows two or more distinct steps when the stubs are long unless some extra pull-down current is provided. *Figure 11a* shows an ECL circuit driving a parallel terminated line, with provision for connecting two worst-case unterminated lines to the driver output. Waveforms at the termination resistor (point A) are shown in the multiple exposure photograph of *Figure 11b*. The upper trace shows a normal signal without stubs connected to the driver. The middle trace shows the effect of connecting one stub to the driver. The step in the negative-going edge indicates that the quiescent I_{OH} current through R_T is not sufficient to cause a full signal for both lines. The relationship between the quiescent I_{OH} current through R_T and the negative-going signal swing was discussed earlier in connection with parallel termination.

The bottom trace in *Figure 11* shows the effect of connecting two stubs to the driver output. The steps in trailing edge are smaller and more pronounced. The deteriorated trailing edge of either the middle or lower waveform increas-

a. Multiple Lines



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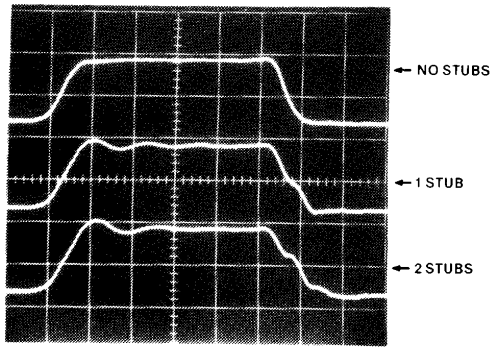
b. Waveforms at Termination Point A



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c. Equivalent Circuit for Determining Initial Negative Voltage Step at the Driver Output

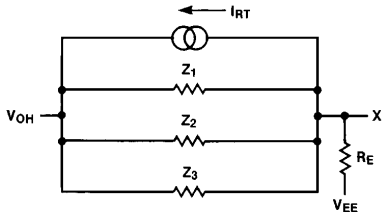

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FIGURE 11. Driving Terminated and Unterminated Lines in Parallel

es the switching time of the cirucit connected to point A. If this extra delay cannot be tolerated, additional pull-down current must be provided. One method uses a resistor to V_{EE} as suggested in *Figure 11a*. The initial negative-going step at point A should be about 0.7V to insure a good fall rate through the threshold region of the driven gate. The initial step at the driver output should also be 0.7V. If the driver output is treated as a switch that opens to initiate the negative-going signal, the equivalent circuit of *Figure 11c* can be used to determine the initial voltage step at the driver output (point X). The value of the current source I_{RT} is the quiescent I_{OH} current through R_T. Using Z' to denote the parallel impedance of the transmission lines and ΔV for the desired voltage step at X, the appropriate value of R_E can be determined from the following equation, using absolute values to avoid polarity confusion.

$$R_E = \left(|V_{EE}| - |V_{OH}| - \Delta V|\right) \bullet \left(\frac{Z'}{|\Delta V| - |I_{RT}|Z'}\right)$$

For a sample calculation, assume that R_T and the line impedances are each 100Ω, V_{OH} is −0.955V, ΔV is 0.750V, V_{EE} is −4.5V and V_{TT} is −2V. I_{RT} is thus 10.45 mA and the calculated value of R_E is 232Ω. In practice, this value is on the conservative side and can be increased to the next larger (10%) standard value with no appreciable sacrifice in propagation through the gate at point A.

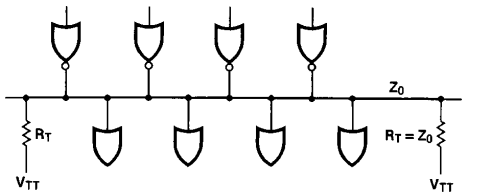
Again, the foregoing example is based on worst-case stub lengths (the longest permissible). With shorter stubs, the effects are less pronounced and a point is reached where extra pull-down current is not required because the reflection from the end of the stub arrives back at the driver while the original signal is still falling. Since the reflection is also negative going, it combines with and reinforces the falling signal at the driver, eliminating the steps. The net result is a smoothly falling signal but with increased fall time compared to the stubless condition.

The many combinations of line impedance and load make it practically impossible to define just with stub length begins to cause noticeable steps in the falling signal. A rough rule-of-thumb would be to limit the stub length to one-third of the values given in *Figure 10*.

DATA BUSSING

Data bussing involves connecting two or more outputs and one or more inputs to the same signal line, *(Figure 12)*. Any one of the several drivers can be enabled and can apply data to the line. Load inputs connected to the line thus receive data from the selected source. This method of steering data from place to place simplifies wiring and tends to minimize package count. Only one of the drivers can be enabled at a given time; all other driver outputs must be in the LOW state. Termination resistors matching the line impedance are connected to both ends of the line to prevent reflections. *For calculating the modified delay of the line (Chapter 3) the capacitance of a LOW (unselected) driver output should be taken as 2 pF.*

An output driving the line sees an impedance equal to half the line impedance. Similarly, the quiescent I_{OH} current is higher than with a single termination. For line impedance less than 100Ω, the I_{OH} current is greater than the data sheet test value, with a consequent reduction of HIGH-state noise margin. This loss can be eliminated if necessary by



TL/F/10790–71

FIGURE 12. Data Bus or Party Line

using multiple output gates (F100112) and paralleling two outputs for each driver. In the quiescent LOW state, termination current is shared among all the output transistors on the line. This sharing makes V_{OL} more positive than if only one output were conducting all of the current. For example, a 100Ω line terminated at both ends represents a net 50Ω DC load, which is the same as the data sheet condition for V_{OL}. If one worst-case output were conducting all the current, the V_{OL} would be −1.705V. If another output with identical DC characteristics shares the load current equally, the V_{OL} level shifts upward by about 25 mV. Connecting two additional outputs for a total of four with the same characteristics shifts V_{OL} upward another 22 mV. Connecting four more identical outputs shifts V_{OL} upward another 20 mV. Thus the V_{OL} shift for eight outputs having identical worst-case V_{OL} characteristics is approximately 67 mV. In practice, the probability of having eight circuits with worst-case V_{OL} characteristics is quite low. The output with the highest V_{OL} tends to conduct most of the current. This limits the upward shift to much less than the theoretical worst-case value. In addition, the LOW-state noise margin is specified greater than the HIGH-state margin to allow for V_{OL} shift when outputs are paralleled.

In some instances a single termination is satisfactory for a data bus, provided certain conditions are fulfilled. The single termination is connected in the middle of the line. This requires that for each half of the line, from the termination to the end, the line length and loading must comply with the same restrictions as unterminated lines to limit overshoot and undershoot to acceptable levels. The termination should be connected as near as possible to the electrical mid-point of the line, in terms of the modified line delay from the termination to either end. Another restriction is that the time between successive transitions, i.e., the nominal bit time, should not be less than 15 ns. This allows time for the major reflections to damp out and limits additive reflections to a minor level.

WIRED-OR

In general-purpose wired-OR logic connections, where two or more driver outputs are expected to be in the HIGH state simultaneously, it is important to minimize the line length between the participating driver outputs, and to place the termination as close as possible to the mid-point between the two most widely separated sources. This minimizes the negative-going disturbances which occur when one HIGH output turns off while other outputs remain HIGH. The driver output going off represents a sudden decrease in line current, which in turn generates a negative-going voltage on the line. A finite time is required for the other driver outputs (quiescently HIGH) to supply the extra current. The net re-

sult is a ''V'' shaped negative glitch whose amplitude and duration depend on three factors: current that the off-going output was conducting, the line impedance, and the line length between outputs. If the separation between outputs is kept within about one inch, the transient will not propagate through the driven load circuits.

If a wired-OR connection cannot be short, it may be necessary to design the logic so that the signal on the line is not sampled for some time after the normal propagation delay (output going negative) of the element being switched. Normal propagation delay is defined as the case where the element being switched is the only one on the line in the HIGH state, resulting in the line going LOW when the element switches. In this case, the propagation delay is measured from the 50% point on the input signal of the off-going element to the 50% point of the signal at the input farthest away from the output being switched. The extra wiring time required in the case of a severe negative glitch is, in a worst-case physical arrangement, twice the line delay between the off-going output and the nearest quiescently HIGH output, plus 2 ns.

An idea of how the extra waiting time varies with physical arrangement can be obtained by qualitatively comparing the signal paths in *Figure 13*. With the outputs at A and B quiescently HIGH, the duration of the transient observed at C is longer if B is the off-going output than if A is the off-going element. This is because the negative-going voltage generated at B must travel to A, whereupon the corrective signal is generated, which subsequently propagates back toward C. Thus the corrective signal lags behind the initial transient, as observed at C, by twice the line delay between A and B. On the other hand, if the output at A generates the negative-going transient, the corrective response starts when the transient reaches point B. Consequently, the transient duration observed at C is shorter by twice the line delay from A to B.

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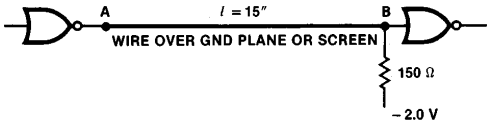
FIGURE 13. Relative to Wired-OR Propagation

BACKPLANE INTERCONNECTIONS

Several types of interconnections can be used to transmit a signal between logic boards. The factors to be considered when selecting a particular interconnection for a given application are cost, impedance discontinuities, predictability of propagation delay, noise environment, and bandwidth. Single-ended transmission over an ordinary wire is the most economical but has the least predictable impedance and propagation delay. At the opposite end of the scale, coaxial cable is the most costly but has the best electrical characteristics. Twisted pair and similar parallel wire interconnection cost and quality fall in between.

For single-wire transmission through the backplane, a ground plane or ground screen (Chapter 5) should be provided to establish a controlled impedance. A wire over a ground plane or screen has a typical impedance of 150Ω with variations on the order of ±33%, depending primarily on the distance from ground and the configuration of the ground. *Figure 14* illustrates the effects of impedance variations with a 15-inch wire parallel terminated with 150Ω to −2V. *Figure 14b* shows source and receiver waveforms when the wire is in contact with a continuous ground plane.



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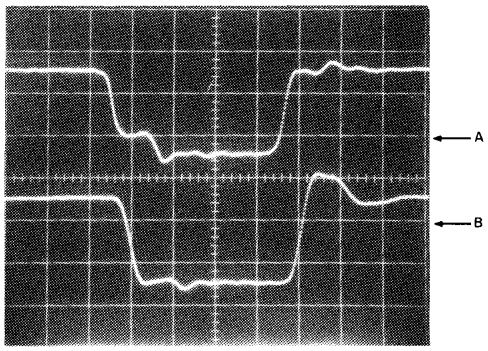
a. Wire over Ground Plane or Screen



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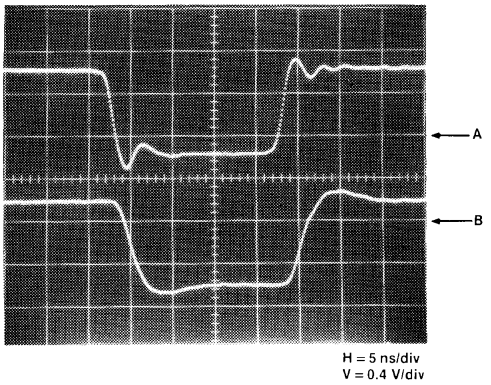
b. Wire in Contact with Ground Plane



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c. Wire Spaced 1⁄8″ from Ground Screen

FIGURE 14. Parallel Terminated Backplane Wire

The negative-going signal at the source shows an initial step of only 80% of a full signal swing. This occurs because the quiescent HIGH-state current I_{OH} (about 7 mA) multiplied by the impedance of the wire (approximately 90Ω) is less than the normal signal swing, and this condition allows the driver emitter follower to turn off. The negative-going signal at the receiving end is greater by 25% ($1 + \rho = 1.25$). The receiving end mismatch causes a negative-going reflection which returns to the source and establishes the V_{OL} level. The positive-going signal at the source shows a normal signal swing, with the receiving end exhibiting approximately 25% overshoot.

Figure 14c shows waveforms for a similar arrangement, but with the wire about ⅛ inch from a ground screen. The impedance of the wire is greater than 150Ω termination, but small variations in impedance along the wire cause intermediate reflections which tend to lengthen the rise and fall times of the signal. As a result, the received signal does not exhibit pronounced changes in slope as would be expected if a 200Ω constant impedance line were terminated with 150Ω.

Series source resistance can also be used with single wire interconnections to absorb reflection. *Figure 15a* shows a 16-inch wire with a ground screen driven through a source resistance of 100Ω. The waveforms *(Figure 15b)* show that although reflections are generated, they are largely absorbed by the series resistor, and the signal received at the load exhibits only slight changes and overshoot. Series termination techniques can also be used when the signal into the wire comes from the PC board transmission line. *Figure 16a* illustrates a 12-inch wire over a ground screen, with 12-inch microstrip lines at either end of the wire. The output is heavily loaded (fan-out of 8) and the combination of impedances produces a variety of reflections at the input to the first microstrip line, shown in the upper trace of *Figure 16b*. The lower trace shows the final output; a comparison between the two traces shows the effectiveness of damping in maintaining an acceptable signal at the output. *Figure 16c* shows the signals at the input to the driving gate and at the output of the load gate, with a net through-put time of 8.5 ns. The circuit in *Figure 16a* is a case of mismatched transmission lines, discussed in Appendix A.

Signal propagation along a single wire tends to be fast because the dielectric medium is mostly air. However, impedance variations along a wire cause intermediate reflections which tend to increase rise and fall times, effectively increasing propagation delay. Effective propagation delays are in the range of 1.5 to 2.0 ns per foot of wire. Load capacitance at the receiving end also increases rise and fall time (Appendix A), further increasing the effective propagation delay.

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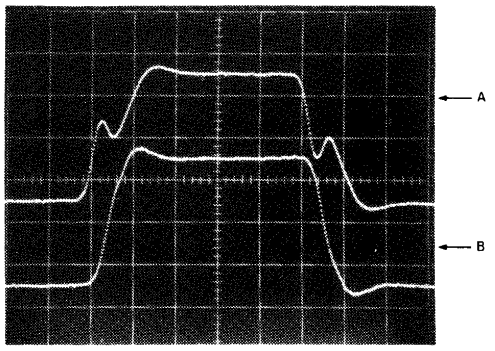
a. Wire over Ground Screen



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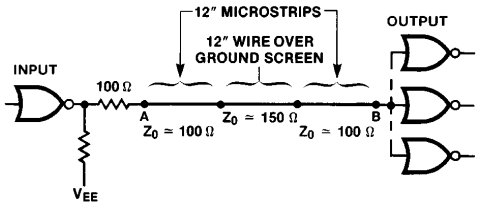
b. Series Terminated Waveform

FIGURE 15. Series Terminated Backplane Wire



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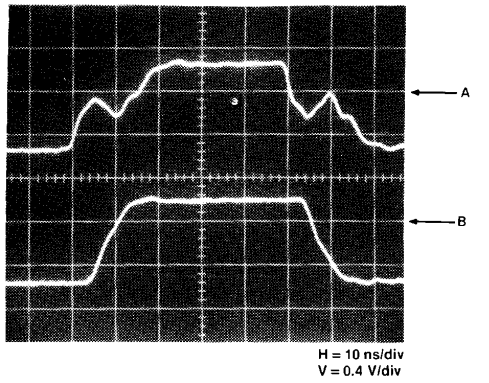
a. Backplane Wire Interconnecting PC Board Lines



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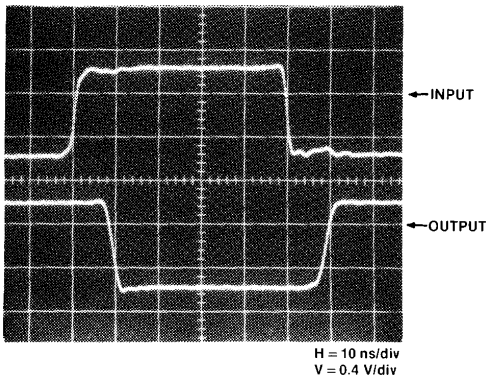
b. Signals into the First Microstrip and at the Loads



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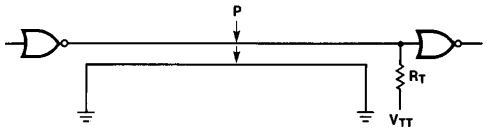
c. Input to Driving Gate and Output of Load Gate

FIGURE 4-16. Signal Path with Sequence of Microstrip, Wire, Microstrip

Better control of line impedance and faster propagation can be achieved with a twisted pair. A twisted pair of AWG 26 Teflon* insulated wires, two twists per inch, exhibits a propagation delay of 1.33 ns/ft and an impedance of 115Ω. Twisted pair lines are available in a variety of sizes, impedances and multiple-pair cables. *Figure 4-17a* illustrates single-ended driving and receiving. In addition to improved propagation velocity, the magnetic fields of the two conductors tend to cancel, minimizing noise coupled into adjacent wiring.

*Teflon is a registered trademark of E.I. du Pont de Nemours Conpany.



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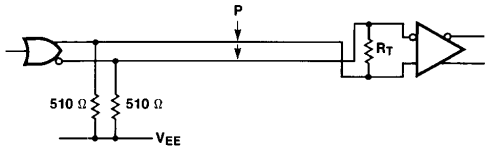
a. Single-ended Twisted Pair



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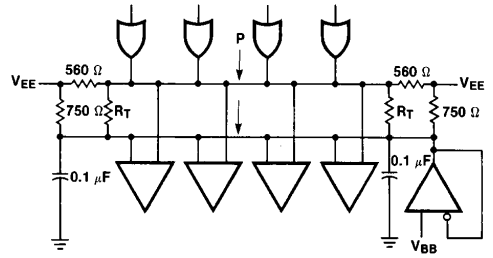
b. Differential Transmission Reception



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c. Backplane Data Bus

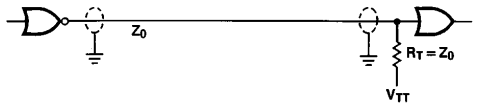
FIGURE 4-17. Twisted Pair Connections

Differential line driving and receiving complementary gates as the driver and an F100114 line receiver is illustrated in *Figure 4-17b*. Differential operation provides high noise immunity, since common mode input voltages between −0.55V and −3.0V are rejected. The differential mode is recommended for communication between different parts of a system, because it effectively nullifies ground voltage differences. For long runs between cabinets or near high power transients, interconnections using shielded twisted pair are recommended.

Twisted pair lines can be used to implement party line type data transfer in the backplane, as indicated in *Figure 4-17c*. Only one driver should be enabled at a given time; the other outputs must be in the V_{OL} state. The V_{BB} reference voltage is available on pin 22 of the flatpak and pin 19 of the dual-in-line package for the F100114.

In the differential mode, a twisted pair can send high-frequency symmetrical signals, such as clock pulses, of 100 MHz over distances of 50 to 100 feet. For random data, however, bit rate capability is reduced by a factor of four or five due to line rise effects on time jitter.[3]

Coaxial cable offers the highest frequency capability. In addition, the outer conductor acts as a shield against noise, while the uniformity of characteristics simplifies the task of matching time delays between different parts of the system. In the single-ended mode, *Figure 4-18a,* 50 MHz signals can be transferred over distances of 100 feet. For 100 MHz operation, lengths should be 50 feet or less. In the differential mode, *Figures 4-18b, c,* the line receiver can recover smaller signals, allowing 100 MHz signals to be transferred up to 100 feet. The dual cable arrangement of *Figure 4-18c* provides maximum noise immunity. The delay of coaxial cables depends on the type of dielectric material, with typical delays of 1.52 ns/ft for polyethylene and 1.36 ns/ft for cellular polyethylene.



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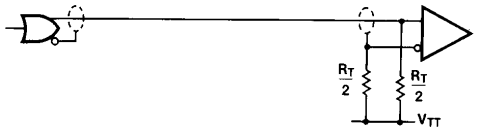
a. Single-Ended Coaxial Transmission



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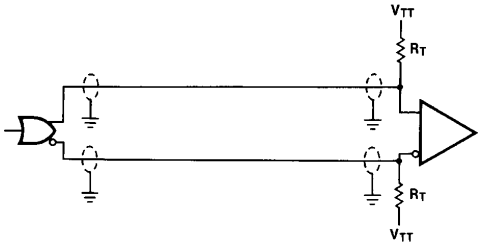
b. Differential Coaxial Transmission



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c. Differential Transmission with Grounded Shields

FIGURE 4-18. Coaxial Cable Connections

REFERENCES

1. Kaupp, H. R., ''Characteristics of Microstrip Transmission Lines,'' *IEEE Transaction on Electronic Computers*, Vol. EC-16 (April, 1967).
2. Harper, C. A., *Handbook of Wiring, Cabling and Interconnections for Electronics*. New York: McGraw-Hill, 1972.
3. True, K. M., ''Transmission Line Interface Elements,'' *The TTL Applications Handbook,* Chapter 14 (August 1973), pp. 14-1–14-14.

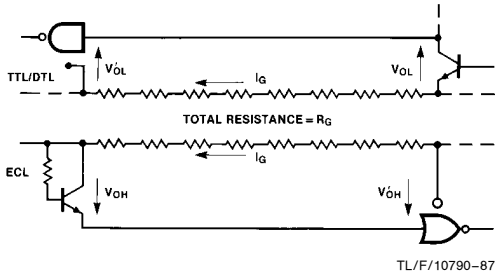
APPENDIX C
ECL DESIGN GUIDE:
POWER DISTRIBUTION AND THERMAL CONSIDERATIONS

INTRODUCTION

High-speed circuits generally consume more power than similar low-speed circuits. At the system level, this means that the power supply distribution system must handle the larger current flow; the larger power dissipation places a greater demand on the cooling system. The direct current (DC) voltage drop along ground busses affects noise margins for all types of ECL circuits. Voltage drops along V_{EE} busses have only a slight effect on F100K circuits, but they require consideration to obtain the performance available from the family.

LOGIC CIRCUIT GROUND, V_{CC}

The positive potential V_{CC} and V_{CCA} in ECL circuits is the reference voltage for output voltages and input thresholds and should therefore be the ground potential. When two circuits are connected in a single-ended mode, any difference in ground potentials decreases the noise margins, as discussed in *Chapter 1*. This effect for TTL/DTL circuits, as well as for ECL circuits, is illustrated in *Figure 1*. The following analysis assumes some average value of current flowing through the distributed resistance along the ground path between two circuits. For the indicated direction of I_G, the shift in ground potential *decreases* the LOW-state noise margin of the TTL/DTL circuits and the HIGH-state noise margin of the ECL circuits. If I_G is flowing in the opposite direction, it *increases* these noise margins, but *decreases* the noise margins when the drivers are in the opposite state. For tabulation of ground currents in ECL, the designs must include termination currents as well as I_{EE} operating currents. ECL logic boards which use microstrip or stripline techniques generally have large areas of ground metal. This causes the ground resistance to be quite low and thus minimizes noise margin loss between pairs of circuits on the same board.



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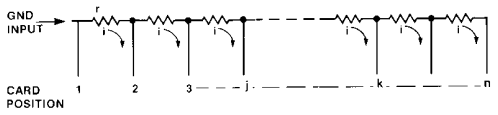
TTL/DTL $V'_{OL} = V_{OL} = +I_G R_G$

ECL $V'_{OH} = V_{OH} + I_G R_G$

$I_G R_G = (V'_{OL} - V_{OL})$ = Noise Margin Decrease $= I_G R_G = (V'_{OH} - V_{OH})$

FIGURE 1. Effect of Ground Resistance on Noise Margins

In practice, two communicating circuits might be located on widely separated PC cards with other PC cards in between. The net resistance then includes the incremental resistance of the ground distribution bus from card to card, while the ground current is successively increased by the contribution from each card. *Figure 2* illustrates a distribution bus for a row of cards with incremental resistances along the bus.



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r = Incremental Bus Resistance between Positions
i = Average Ground Current per Card

FIGURE 2. Ground Shift Along a Row of PC Cards

The ground shift can be estimated by first determining an average value of current per card based on the number of packages, the mix of SSI and MSI, and the number and types of terminations. With n cards in the row, an average ground current (i) per card, and an incremental bus resistance (r) between card positions, the bus voltage drops between the various positions can be determined as follows:

between positions 1 and 2: $v_{1-2} = (n-1)\,ir$

between positions 1 and 3: $v_{1-3} = (n-1)\,ir + (n-2)\,ir$

between positions 1 and 4: $v_{1-4} = (n-1)\,ir + (n-2)\,ir + (n-3)\,ir$

between 1 and n:

$$v_{1-n} = ir\{(n-1) + (n-2) + (n-3) + \ldots + [n-(n-1)]\}$$
$$= ir\,[1 + 2 + 3 + \ldots + (n-1)]$$
$$v_{1-n} = ir \sum_{1}^{n-1} n$$

For a row of 15 cards, for example, the total ground shift between positions 1 and 15 is expressed as in Equation 1.

$$v_{1-15} = ir \sum_{1}^{14} n = ir\,(1 + 2 + 3 + \ldots + 13 + 14) \quad \text{(eq. 1)}$$
$$= 105\,ir$$

The ground shift between any two card positions j and k can be determined as follows for the general case.

$$v_{j-k} = (n - j)\,ir + [n - (j + 1)]\,ir + [n - (j + 2)]\,ir + \ldots + \{n - [j + (k\text{-}j\text{-}1)]\}\,ir$$

$$= (k - j)\,nir - ir\{j + (j + 1) + (j + 2) + \ldots + [j + (k\text{-}j\text{-}1)]\} \quad \text{(eq. 2)}$$

$$v_{j-k} = (k - j)\,nir - ir \sum_{j}^{k-1} n = ir\,[(k - j)\,n - \sum_{j}^{k-1} n]$$

In a row of 15 cards, the ground shift between positions four and nine, for example, is determined as follows.

$$v_{j-k} = ir\,[(9 - 4)\,15 - (4 + 5 + 6 + 7 + 8)] \quad \text{(eq. 3)}$$
$$= ir\,(75 - 30) = 45\,ir$$

The ground shift between the same number of positions further down the row is less because of the decreasing current along the row. Consider the ground shift between card positions 10 and 15.

$$v_{10-15} = ir\,[(15 - 10)15 - (10 + 11 + 12 + 13 + 14)] \quad \text{(eq. 4)}$$
$$= ir\,(75 - 60) = 15\,ir$$

These examples illustrate several principles the designer should consider regarding the ground distribution bus and assignment of card positions. The bus resistance should be kept as low as possible by making the cross-sectional areas as large as practical. Logic cards which represent the heaviest current drain should be located nearest the end where ground comes into the row of cards. Cards with single-ended logic wiring between them should be assigned to positions as close together as possible. Conversely, if the ground shift between two card positions represents an unacceptable loss of noise margin, then the differential transmission and reception method i.e., twisted pair, should be used for logic wiring between them, thereby eliminating ground shift as a noise margin factor.

CONDUCTOR RESISTANCES

Conductors with large cross-sectional areas are required to maintain low voltage drops along power busses. For convenience, *Figure 3* lists the resistance per foot and the cross-sectional area for more common sizes of annealed copper wire. Other characteristics and a complete list of sizes can be found in standard wire tables. A useful rule-of-thumb regarding resistances and, hence, areas is: as gauge numbers increase, resistance doubles with every third gauge number; e.g., the resistance per foot of #10 wire is 1 mΩ, for #13 wire it is 2 mΩ. Similarly, the resistance per foot of #0 wire is 0.078 mΩ, which is half that of #2 wire.

For calculations involving conductors having rectangular cross sections, it is often convenient to work with sheet resistance, particularly for power distribution on PC cards. Copper resistivity is usually given in ohm-centimeters, indicating the resistance between opposing faces of a 1 cm cube. The sheet resistance of a conductor is obtained by dividing the resistivity by the conductor thickness. These relationships follow.

AWG B & S Gauge	Resistance mΩ Per Foot	Cross-Sectional Area Square Inches
#2	0.156	5.213×10^{-2}
#6	0.395	2.062×10^{-2}
#10	0.999	8.155×10^{-3}
#12	1.588	5.129×10^{-3}
#18	6.385	1.276×10^{-3}
#22	16.14	5.046×10^{-4}
#26	40.81	1.996×10^{-4}
#30	103.2	7.894×10^{-5}

FIGURE 3. Resistance and Cross-Sectional Area of Several Sizes of Annealed Copper Wire

Copper resistivity $= \rho = 1.724 \times 10^{-6}\ \Omega$cm @ 20°C

Resistance of a conductor $= \rho \frac{l}{A} = \rho \frac{l}{tw}$

where: l = length t = thickness w = width

Sheet resistance $\rho_S = \frac{\rho}{t}\ \Omega$ per $\frac{l}{w}$

The length/width ratio (l/w) is dimensionless; therefore, the resistance of a length of conductor of uniform thickness can be calculated by first determining the number of ''squares,'' then multiplying by the sheet resistance. For example, a conductor one-eighth inch wide and three inches long has 24 squares; its resistance is 24 times the sheet resistance. Since many thickness dimensions are given in inches, it is convenient to express the resistivity in ohm-inch, as follows.

$\rho(\Omega\text{in.}) = \rho(\Omega\text{cm}) \div 2.54 = 6.788 \times 10^{-7}\ \Omega$in.

The use of sheet resistance and the ''squares'' concept is illustrated by calculating the resistance of the conductor shown in *Figure 4*. Assume the conductor is a 1 oz. copper cladding with a 0.0012 inch minimum thickness on a PC card.

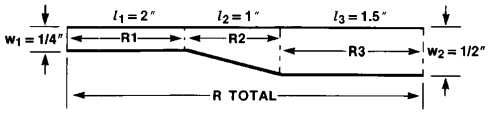

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FIGURE 4. Conductor of Uniform Thickness but Non-Uniform Cross Section

Sheet resistance $= \rho_S = \frac{\rho}{t}$

$= 5.657 \times 10^{-4}\ \Omega$ per square

The number of squares S for the rectangular sections are as follows.

$$S1 = \frac{l_1}{w_1} = 8 \qquad S_3 = \frac{l_3}{w_2} = 3$$

The middle average segment of the conductor has a trapeziodal shape. The average of w_1 and w_2 can be used as the effective width, within 1% accuracy, if the w_2/w_1 ratio is 1.5 or less. Otherwise, a more exact result is obtained as follows.

$$S_2 = \frac{l_2}{w_2 - w_1} \ln\left(\frac{w_2}{w_1}\right) = 4 \ln 2 = 2.77 \text{ squares} \quad \text{(eq. 5)}$$

$$\text{Total } R = R_1 + R_2 + R_3 = \rho_s(S_1 + S_2 + S_3)$$
$$= 7.51\ \text{m}\Omega$$

As another example, assume that a 1 oz. trace must carry a 200 mA current six inches with a voltage drop less than 10 mV.

$$R_{max} = \frac{V_{max}}{I} = \frac{0.01}{0.2} = 0.05\Omega$$

$$0.05 = \rho_s \frac{l}{w} \qquad \text{(eq. 6)}$$

$$\frac{w}{l} = 20\ \rho_s$$

$$w = 120\ \rho_s = (120)\ 5.657 \times 10^{-4} = 67.9 \times 10^{-3}$$

$\therefore$ minimum trace width, w = 68 mils

At a higher current level, consider the voltage drop in a conductor 20 mils thick, 1.25 inches wide and 3 feet long carrying a 50A current.

$$\rho_s = \frac{6.788 \times 10^{-7}}{2 \times 10^{-2}} = 3.364 \times 10^{-5}\ \Omega \text{ per square}$$

$$V = IR - (50)\ (3.364 \times 10^{-5}) \frac{36}{1.25} \qquad \text{(eq. 7)}$$

$$= 0.0484 = 48.4 \text{ mV}$$

Sheet resistances for various copper thicknesses are listed in *Figure 5*. Standard thicknesses and tolerances for copper cladding are tabulated in *Figure 6* and resistance per foot as a function of width is shown in *Figure 7*.

Weight or Thickness	Sheet Resistance Ω per Square	Thickness	Sheet Resistance Ω per Square
2 oz.	2.715×10^{-4}	0.02 in.	3.364×10^{-5}
3 oz.	1.886×10^{-4}	0.05 in.	1.358×10^{-5}
5 oz.	1.077×10^{-4}	1/16 in.	1.086×10^{-5}
0.01 in.	6.788×10^{-5}	1/4 in.	2.715×10^{-6}

FIGURE 5. Sheet Resistance for Various Thicknesses of Copper

Nominal Thickness		Nominal Weight	Tolerances By	
in.	mm	oz/ft²	Weight, %	in.
0.0007	0.0178	½	+10	+0.0002
0.0014	0.0355	1	+10	+0.0004 −0.0002
0.0028	0.0715	2	+10	+0.0007 −0.0003
0.0042	0.1065	3	+10	+0.0006
0.0056	0.1432	4	+10	+0.0006
0.0070	0.1780	5	+10	+0.0007
0.0084	0.2130	6	+10	+0.0008
0.0098	0.2460	7	+10	+0.001
0.014	0.3530	10	+10	+0.0014
0.0196	0.4920	14	+10	+0.002

FIGURE 6. Thickness and Tolerances for Copper Cladding

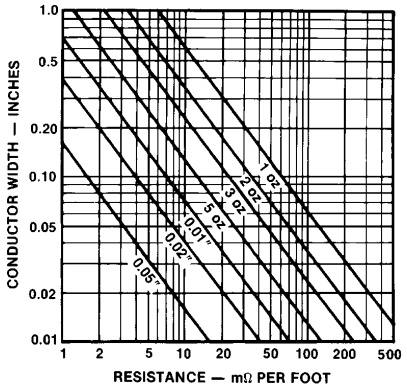

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FIGURE 7. Conductor Resistance vs Thickness and Width

TEMPERATURE COEFFICIENT

The resistances in *Figures 3, 5,* and *7*, as well as those used in the sample calculations, are 20°C values. Since copper resistivity has a temperature coefficient of approximately 0.4%/°C, the resistance at a temperature (T) can be determined as follows.

$$R_T = R_{20°C}\ [1 + 0.004\ (T + 20°C)]$$

At 55°C: (eq. 8)

$$R = R_{20°C}\ [1 + 0.004\ (55°C - 20°C)] = 1.14\ R_{20°C}$$

When specifying power bus dimensions for PC cards containing many IC packages, designers should bear in mind that excessive current densities can cause the copper temperature to rise appreciably. *Figure 8* illustrates the ohmic heating effect of various current densities.[1]

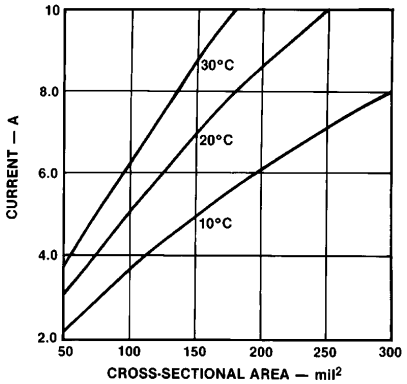

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FIGURE 8. Temperature Rise with Current Density in PC Board Traces

DISTRIBUTION IMPEDANCE

Power busses should have low AC impedance, as well as low DC resistance, to prevent propagation of extraneous disturbances along the distribution system. As far as current or voltage changes are concerned, power and ground busses appear as transmission lines; thus their impedances can be affected by shape, spacing and dielectric. The effect of geometry on impedance is illustrated in the two arrangements of *Figure 9*. The same cross-sectional area of copper is used, but the two round wires have an impedance of about 75Ω while the flat conductors have an impedance determined as follows.

$$Z_0 = \frac{377\ d}{\sqrt{\epsilon}\ h} \text{ for } \frac{d}{h} < 0.1$$

With a Mylar®* or Teflon®* dielectric ($\epsilon = 2.3$) two mils thick, impedance of the flat conductor pair is only 0.5Ω. Power line impedance can be reduced by periodically connecting RF-type capacitors across the line.

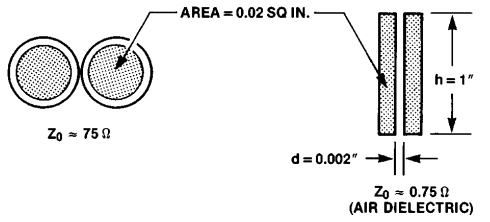

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FIGURE 9. Effect of Geometry on Power Bus Impedance

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GROUND ON PC CARDS

It is essential to assign one layer of copper cladding almost exclusively to ground. This provides low-impedance, non-interfering return paths for the current changes which travel along signal traces when the IC outputs change state. These currents flow from the V_{CCA} pins of the IC packages, through the output transistors, then into the loads and the stray capacitances. These stray capacitances exist from an output to V_{EE}, output to ground, and to other signal lines. Thus, displacement currents through stray capacitances flow in many paths, but must ultimately return through ground to the output transistor where they originated. To reduce the length and impedance of the return path, the ground metal should cover as large an area as possible and one decoupling capacitor should be provided for every one to two IC packages. Additional capacitors may be needed for multiple output devices. These capacitors should be ceramic, monolithic or other RF types in the 0.01 μF to 0.1 μF range.

The load current returning to an IC package through ground metal is predictable, both in magnitude and in the return path. Since the magnetic and capacitive coupling between a signal trace and the underlying ground provides the transmission line characteristic, it follows that the load current flowing through the signal trace is accompanied by a ground return current equal in magnitude but opposite in direction. For example, in a 50Ω terminator I_{OL} is 5.9 mA, I_{OH} is 20.9 mA. Then signal change will cause about 15 mA current change and, as this current change propagates along the signal trace, a current of −15 mA advances along the ground directly underneath the signal trace. Therefore, if there is an interruption in the ground, the return current is forced to go around it. The 15 mA current change can be reduced by terminating the complementary output of the signal. Then a signal change will direct the current from true output to the complement output reducing the Δ currents in the ground plane. When it is necessary to interrupt the ground plane, the interruptions should be kept as short as possible; every effort should be made to locate them away from overlying signal lines. When the ground plane is interrupted for short signal lines between packages, these lines should be at right angles to signal lines on the other side to minimize coupling. V_{EE} and V_{TT} distribution lines can also act as the return side of transmission lines, as long as decoupling capacitors to ground are placed in the immediate areas where the signal return current must continue through ground.

Several connections along the edge of a PC card should be assigned to ground to accommodate backplane signal ground. These should be spaced at one-half to one inch intervals to minimize the average path length for signal return currents and to simulate a distributed connection to the backplane signal ground.

Not enough emphasis can be placed on the requirement for a good ground. All input signals are referenced to internal V_{BB} and the V_{BB} is referenced to V_{CC} (ground). Any variation from one side of the board to the other affects the noise margins. To help eliminate some of the variations a separate V_{CCA} is provided on F100K ECL circuits to power the output drivers and leave the V_{CC} going to internal circuitry unaffected.

BACKPLANE CONSTRUCTION

In order to take complete advantage of the speeds inherent in F100K ECL it is desirable to construct the backplane as a multilayer printed circuit board. Generally, two internal layers are devoted to ground and V_{EE} and the signals occupy the outside layers. Where power densities are very high, it may be necessary to supplement the power layers with external busses (see Backplane Interconnections, *Chapter 4*).

If it is necessary to use wires to augment the interconnection provided by the traces, less critical signals should use the wires. The wires will exhibit an impedance which can be calculated with the wire-over-ground formula

$$Z_0 = \frac{138}{\sqrt{\epsilon}} \text{Log}_{10} \frac{4h}{d} \qquad \text{(eq. 9)}$$

where d is diameter, h is distance to ground, and ϵ is dielectric constant.

Bear in mind that if the ground plane is buried inside the board, then both h and ϵ are made up of multiple components.

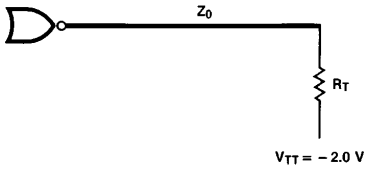
TERMINATION SUPPLY, V_{TT}

A separate return voltage for the termination resistors offers a way to minimize power dissipation in systems extensively using parallel termination techniques. A −2V V_{TT} value represents an optimum speed/power trade-off, allowing sufficient termination current to discharge load capacitances while minimizing the average power consumption. *Figure 10* shows the average values of current, IC power dissipation and resistor power dissipation for various values of the termination resistor R_T returned to −2V. Average values are determined by calculating the output HIGH and output LOW values, then taking the average. These 50% duty cycle

values are useful in determining the current drain on the −2V supply and the contribution to dissipation on the logic boards. Peak values of termination current are approximately 60% greater than the average values listed.

DC regulation of the −2V supply is not critical; a variation of ±5% causes a change in output levels of ±12 mV for 50Ω terminations or ±7 mV for 100Ω terminations.

The high frequency characteristics of the V_{TT} distribution are extremely important. Ideally, a solid voltage plane should be devoted to V_{TT}. If this is not feasible, the V_{TT} distribution should form a grid using orthogonal traces. In any case, decoupling capacitors to ground should be used to reduce the high frequency impedance.



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R_T Ω	I_{avg} mA	$P_{D\ (avg)}$ mW	
		IC Output	Resistor
50	14	14	13
62	11	12	11
75	9.3	9.5	9.1
90	8.1	8.2	7.9
100	7.3	7.3	7.1
150	5.0	4.9	5.0

FIGURE 10. Average Current and Power Dissipation for Parallel Termination to −2V

If the terminators used are in Single In-line Packages (SIP) or Dual-In-line Packages (DIP) as opposed to discrete resistors, particular attention must be given to decoupling in order to maintain a solid V_{TT} voltage inside the package. This is necessary to avoid crosstalk due to mutual inductance to V_{TT}. SIPs have been developed which have multiple V_{TT} connections and on-board decoupling capacitors.

V_{EE} SUPPLY

The value of V_{EE} is not critical for F100K since all circuits in the family operate over the range of −4.2V to −5.7V. Decoupling capacitors to ground should be used on each card, as previously discussed in connection with the ground on PC cards. In addition, each card should used 1 μF to 10 μF decoupling capacitors near the points where V_{EE} enters the card.

The current drain for the V_{EE} supply for each circuit type can be determined from the data sheet specifications. For V_{EE} values other than −4.5V, the current drain varies as shown in *Figure 11* and *12* for SSI and MSI elements respectively. These graphs are made from data from the F100101 and F100179.

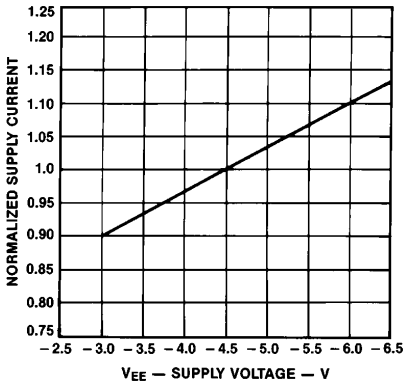

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FIGURE 11. Supply Current vs Supply Voltage for F100101

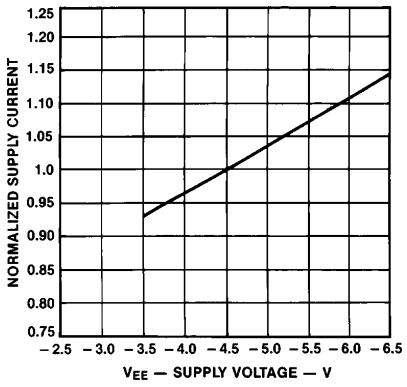

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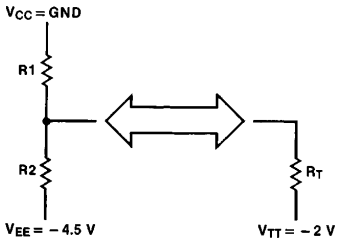
FIGURE 12. Supply Current vs Supply Voltage for F100179

Series dividers used to obtain Thevenin equivalent parallel terminations increase the current load on the V_{EE} supply, as do the pull-down resistors to V_{EE} used with series termination. Average V_{EE} current and resistor dissipation for Thevenin equivalent terminations are listed in *Figure 13* for several representative values of equivalent resistance. The average values apply for 50% duty cycle. Peak current values are approximately 11% greater. Dissipation in the IC output transistor is the same as in *Figure 10*. Average dissipation and I_{EE} current for several values of pull-down resistance to V_{EE} are listed in *Figure 14*. The R_E values are appropriate for series termination of transmission lines with impedances listed in the Z_0 column, determined from Equation 12. Peak current values are approximately 12% greater than average values.

Figures 10, 13 and *14* show that the Thevenin equivalent parallel termination method leads to ten times as much dissipation in the resistors as in the single resistor returned to −2V. Similarly, the dissipation in R_E for series termination is three times the dissipation in the parallel termination resistor to −2V.



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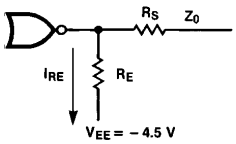
R_T Ω	$R_{1\Omega}$ = 1.80 R_T	$R_{2\Omega}$ = 2.25 R_T	I_{EE} (avg) mA	P_D (avg) mW Resistors
50	90	113	28.2	109
62	112	140	22.7	87.9
75	135	169	18.8	72.7
82	148	185	17.2	66.5
90	162	203	15.7	60.5
100	180	225	14.1	54.5
120	216	270	11.7	45.4
150	270	338	9.4	36.3

FIGURE 13. Series Divider for Thevenin Equivalent Terminations



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Z_0 Ω	R_E Ω	I_{EE} (avg) mA	P_D (avg) mW	
			IC Output	R_E
50	269	9.8	12.9	25.8
62	331	7.9	10.4	20.6
75	399	6.5	8.6	16.8
90	477	5.4	7.1	13.9
100	530	4.9	6.5	12.7
120	634	4.1	5.4	10.6
150	791	3.2	4.2	8.1

FIGURE 14. Average Current and Power Dissipation Using Pull-Down Resistor to V_{EE}

THERMAL CONSIDERATIONS

System cooling requirements for ECL circuits are based on three considerations: (1) the need to minimize temperature gradients between circuits communicating in the single-ended mode, (2) the need to control the temperature environment of each circuit to assure that the parameters stay within guaranteed limits, and (3) the need to insure that the maximum rated junction temperature is not exceeded.

Temperature gradients are of no practical concern with F100K circuits since they are temperature compensated; their output voltage levels and input thresholds change very little with temperature, as discussed in *Chapter 1*. With uncompensated ECL circuits, output voltage levels and input thresholds vary with temperature. This causes a loss of noise margin when driving and receiving circuits are operating at different temperatures. Loss of HIGH-state noise margin occurs when the receiving circuit is at the higher temperature, amounting to approximately 1 mV/°C of temperature gradient. When the driving circuit is at the higher temperature, the LOW-state margin decreases by approximately 0.5 mV/°C of gradient. The system designer must consider noise margin loss, due to temperature gradients.

Each DC parameter limit on the F100K data sheets applies over the entire 0°C to +85°C case temperature. For uncompensated ECL circuits, parameter limits have different values for different ambient temperatures. Further, ambient temperature specifications are based on a minimum air flow rate of 400 linear feet per minute. Thermal equilibrium must be established for incoming test results of uncompensated ECL circuits to be valid. The time required to attain equilibrium can vary considerably, depending on the internal dissipation of the particular IC type and details of the thermal arrangement. Normally, an adequate waiting time is three to five minutes after power is applied.

The maximum rated junction temperature of F100K circuits is +150°C. An individual IC junction temperature can be determined by multiplying power dissipation by the junction-to-air thermal resistance θ_{JA} and adding the result to the ambient air temperature. The power dissipation is V_{EE} times I_{EE}, from the data sheet, plus the dissipation in the output transistors from *Figure 10* or *14*. Thermal resistance is shown in *Figure 15* as a function of cooling air flow rate. This figure applies when the IC is mounted on a board with the air flowing in a plane parallel to the board and perpendicular to the long axis of the IC package. When air temperature, flow rate and package power dissipation are known, junction temperature is determined as follows.

$$T_J = T_A + P_D\theta_{JA} \qquad \text{(eq. 10)}$$

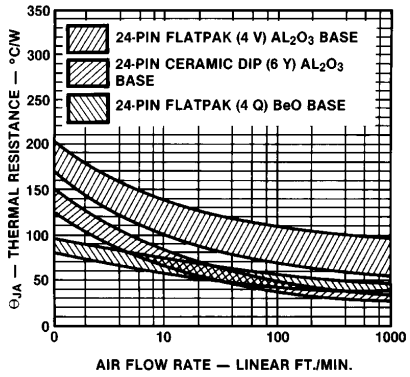

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FIGURE 15. Junction-to-Air Thermal Resistance vs Air Flow Rate

Conversely, when the maximum rate junction temperature (+150°C), the package power dissipation, and the air temperature are known, the minimum flow rate can be determined by first determining the maximum thermal resistance.

$$\text{Maximum } \theta_{JA} = \frac{(150^\circ - T_A)}{P_D} \qquad \text{(eq. 11)}$$

For this value of θ_{JA} the minimum flow rate is determined from *Figure 15*.

When the system designer plans to depend on natural convection for cooling, it is recommended that thermal tests be conducted to determine actual conditions. The effectiveness of natural convection for cooling varies greatly. For instance, on a densely packed logic board in a horizontal attitude in still air, the effective ambient temperature for an IC varies with its position. An IC in the middle of the board is subjected to air that is partially heated by surrounding ICs. Additionally, the temperature of the board rises due to heat flow through the component leads. These effects can cause a much higher junction temperature than might be expected.

REFERENCE

1. Harper, C.A., Editor, *Handbook of Wiring, Cabling and Interconnecting for Electronics*, McGraw-Hill, 1972.

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