Variable Range PWM A/D for COP820CJ

National Semiconductor
Application Note 815
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This application note is an extension of AN-607. The basic difference between the previous version and this new approach (patent pending) is that the microcontroller can vary the computing range as required by the signal being measured. This can be done totally in software without any additional hardware.

Microcontrollers such as the COP820CJ that have an on board comparator allow for a very cost effective A/D (refer to *Figure 1*). Note that there are two back to back diodes in the circuit diagram in addition to the input resistor and R/C network. The diodes provide a speed up path that assists in initializing the capacitor to equal the unknown input voltage prior to a conversion.

Since the on board comparator has an input limitation of 0.4V to $V_{CC} - 1.5V$, time and resolution would be wasted if the R/C network was driven with a PWM signal that was either at GND or V_{CC} the entire sample time. The waveforms *(Figure 2)* used in this example, have a duty cycle for the high and low pulses. High pulses consist of 8 instruction cycles at ground and 16 cycles at V_{CC}. Thus providing an upper range of 16/24 (V_{CC}) or 3.30V for full counts with $V_{CC} = 5V$. Low pulses consist of 5 cycles at V_{CC} and 19 cycles at ground. Thus providing a lower range 5/24 (V_{CC}) or 1.041V for zero counts. Equation 1 below illustrates various measurements:

Let:

$V_L = V_{CC}$ (low pulse duty cycle) ;average voltage

$V_H = V_{CC}$ (high pulse duty cycle) ;average voltage

EQU. 1:

$$V_{IN} = V_L + (V_H - V_L) \times (\text{Ton counts/Total counts})$$

The flow chart *(Figure 3)* and code listing *(Figure 4)* uses 100 counts over an input range of 1.0V to 3.30V for 23 mV per count resolution. Many variations of this technique are possible to meet almost any range or speed desired. Simply change the number of counts or the high and low duty cycles. For example, with a known input range of 1.25V–2.5V the low pulse would consist of 6 cycles high and 18 cycles low. High pulses would consist of 12 cycles high and 12 cycles low. Another alternative could involve a rough measurement to determine the approximate range of the input. Following this, duty cycles with an average voltage just below (low pulse) and just above (high pulse) the initial measurement can be used to give a high resolution result relatively fast.

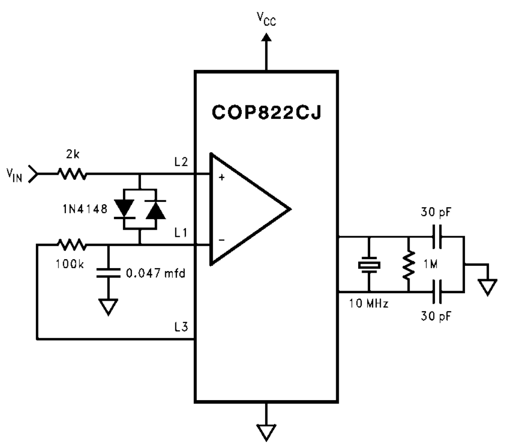

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FIGURE 1. Basic Circuit

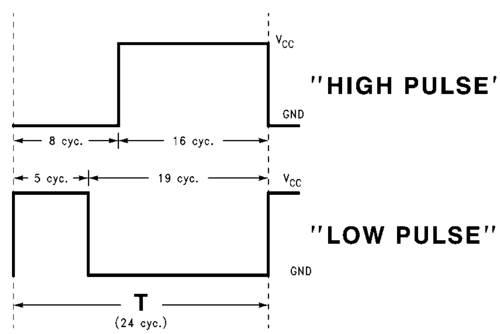

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FIGURE 2. Pulse Waveforms

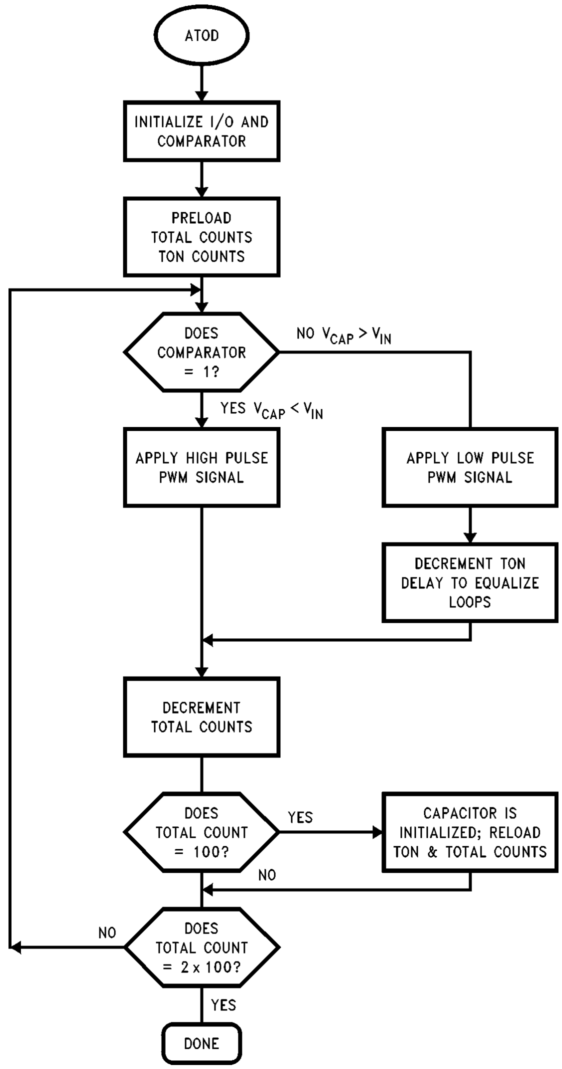

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FIGURE 3. PWM Flow Diagram

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;FILE VARPWM.TXT, COP822CJ, KEVIN DAUGHERTY 3-30-92
;THIS ROUTINE PROVIDES FOR LIMITED RANGE ON THE INPUT TO AN
;ONBOARD COMPARATOR .
;THE INPUT RANGE FOR THE A/D IS 1V
;TO 3.25V.  THIS REQUIRES A HIGH PULSE DUTY CYCLE = 8 LOW
;AND 16 HIGH CYCLES, AND A LOW PULSE DUTY CYCLE = 5 HIGH
;AND 19 LOW CYCLES.  L1=(-) COMPARATOR INPUT CONNECTED TO
;R/C NETWORK, L2=(+) INPUT FOR Vin, L3 DRIVES R/C.
;100 COUNTS OF RESOLUTION ARE STORED IN RAM LOCATION 00.
;ZERO COUNTS EQUALS 1V AND 100 COUNTS EQUALS 3.25V
;@Vcc=4.75V.  WITH THE RANGE PROPORTIONAL TO THE SUPPLY
;VOLTAGE.
.CHIP 820
CNTRL2=0CC
LDATA=0D0
CMPSL=0B7
LCONF=0D1
TON=0F2
TOTAL=0F0
;
          SBIT 4,CNTRL2 ;SET COMPARATOR ENABLE BIT
          LD LCONF,#00  ;SETUP L1&2 AS INPUTS
          LD LDATA,#00  ;TRISTATE L INPUTS
CONV:     LD A,#02      ;USE FOR COUNTING TOTAL LOOPS
          LD 0F1,#02  ;TOTAL LOOP COUNTER
          LD TOTAL,#064 ;PRELOAD TOTAL =100 COUNTS
          LD TON,#064 ;PRELOAD TON =100 COUNTS
          LD 0FE,#0D0 ;INIT. B REG TO POINT TO Ldata REG
          SBIT 3,LDATA  ; L3=HIGH
          SBIT 3,LCONF  ; L3=OUTPUT
LOOP:     IFBIT 3,CNTRL2 ;TEST COMPARATOR OUTPUT BIT
          JP HIGH     ;JUMP IF COMPARATOR= HIGH
          NOP
          NOP          ;EQUALIZE TIME FOR SET AND RESET
          SBIT 3,[B]   ;DRIVE L3 HIGH 5 PULSES
          DRSZ TON     ;DECREMENT Ton WHEN APPLYING NEG. REF.
          NOP
          RBIT 3,[B]   ;DRIVE L3 LOW WHEN COMPARATOR IS LOW.
          NOP          ;EQUALIZE HIGH AND LOW LOOP CYCLES
          NOP
          JP COUNT     ;JUMP TO COUNT UNLESS TON REACHES ZERO
HIGH:     RBIT 3,[B]   ;RESET L3 FOR TOTAL OF 8 CYCLES
          NOP
          NOP
          NOP
          NOP
          NOP
          NOP
          NOP
          SBIT 3,[B]   ;DRIVE L3 HIGH FOR TOTAL OF 16 CYCLES
          NOP
          NOP
COUNT:    DRSZ TOTAL   ;DEC. TOTAL COUNTS EACH LOOP
          JP LOOP      ;JUMP UNLESS TOTAL CNTS.=0
          RBIT 3,LCONF ;TRISTATE L3 TO MINIMIZE ERROR
          RBIT 3,[B]    ; "                          "
          IFEQ A,0F1    ;CHECK FOR 2nd CONVERSION COMPLETE
          JP RELOAD     ;IF TRUE
          JP DEC        ;OTHERWISE JUMP TO DEC
RELOAD:   LD TON,#064   ;RELOAD TON FOR START OF NEXT CONV.
          LD TOTAL,#064 ;SYNC TON AND TOTAL COUNTS
DEC:      SBIT 3,[B]    ;SET L3 HIGH
          SBIT 3,LCONF ;RESTORE L3 AS OUTPUT
          DRSZ 0F1     ;DECREMENT TOTAL LOOP UNTIL ZERO.
          JMP LOOP     ;DONE WHEN 0F1 IS ZERO.
          LD A,TON     ;LOAD A WITH Ton RESULT
          X A,00       ;STORE RESULTS IN RAM 00
.END
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FIGURE 4. Code Listing

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