Dose Rate Response of Advanced CMOS Products

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This paper investigates the dose rate radiation response of an Advanced CMOS product: the FACT™ (Fairchild Advanced CMOS Technology) 54AC299, 8-Input Universal Shift/Storage Register with Common Parallel I/O pins. Data demonstrates:

- The latchup-free capability of this FACT device type
- Its dose rate upset threshold level

As radiation hardness requirements increase, Advanced CMOS technologies, such as National Semiconductor's FACT logic, must meet these demands.

One assurance requirement in a dose rate environment is device latchup immunity. By utilizing FACT radiation latchup-free product, system designers improve their system's electrical performance, reduce power consumption, increase usable board area, and decrease user cost while improving the radiation hardness of the total system.

Associated with this gamma dot environment is dose rate upset threshold level. Knowledge of this threshold level enables system designers to determine the circumvention scheme that will prevent data loss. The upset threshold level varies with each Advanced CMOS process, layout (design rules), and device-circuit design. This is generally one to two orders of magnitude lower than the latchup level.

FABRICATION OF FACT LOGIC

National's FACT 54AC299 device utilizes a CMOS-EPI (epitaxial silicon) in its fabrication. This process features a P-well design using N+ <100> substrate and N-type <100> EPI starting material. The EPI material has a thickness of less than 8 μm.

Isolation between MOSFETs is accomplished through the LOCOS unhardened field oxide. Gate oxide thickness is less than 250 μm. The typical effective length value of this single polysilicon self-aligned gate process is 1.3 μm for both P- and N-channel MOSFETs.

Two low temperature oxides are employed for interlayer dielectrics. Planarization is accomplished through a sputter etch method. The dual-layer metalization process uses sputtered AL-1.5% Si metal which is plasma etched. The final passivation is PECVD silicon nitride. *Figure 1* shows the final cross section of this process.

The topography of the FACT CMOS-EPI process features 2 μm geometries and spacings, a 4.5 μm Metal 1 pitch, and 0.5 μm alignment. Nine mask steps are employed, based on FACT design rules. Vias and contact design rules are 2.0 μm square. Metal 1 has a designed width of 2.5 μm while the Metal 2 designed width is 3.5 μm. Tables I and II provide a summary of the process.

54AC299 CIRCUIT DESCRIPTION

The FACT 54AC299 device under test (DUT) is an 8-bit universal shift/storage register with common parallel I/O pins *(Figure 2)*.

Like all of National's FACT products, the 54AC299 is guaranteed to have MIL Class 2 ESD immunity.

Common paralleled I/O pins reduce pin count. Each I/O pin connects to both an input and an output and can be viewed as having three states: input, output, and output disabled. The 54AC299 device has four operating modes: shift left, shift right, store, and load. The circuit utilizes eight positive edge-triggered D-type flip-flops and the interstage logic to perform various synchronous operating modes. The type of operation is selected by SO and SI pins.

All flip-flop outputs are brought out through TRI-STATE® buffers. These outputs and parallel load inputs are multiplexed to reduce the total number of package pins. Additional output pins are provided for flip-flops. 00, 07 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register. This LOW signal on MR overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either OE1 or OE2 disables the TRI-STATE buffers and puts the I/O pins in the HIGH impedance state. In this condition, shift, hold, load, and reset operations may still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S0 and S1 in preparation for a parallel load operation.

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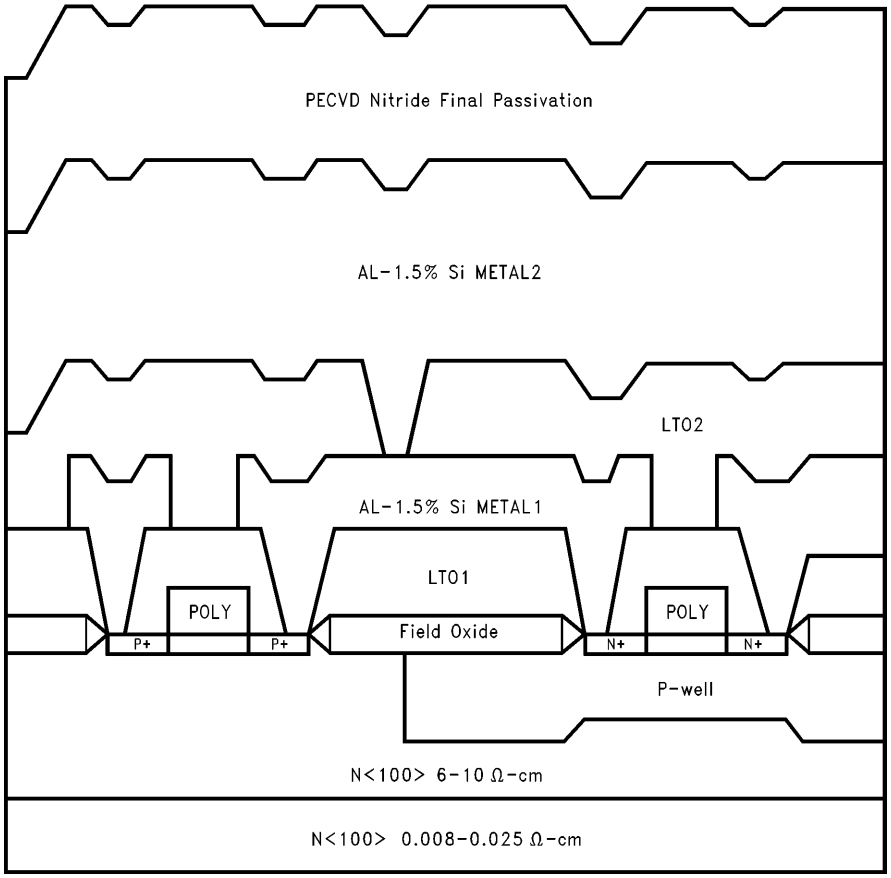

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FIGURE 1

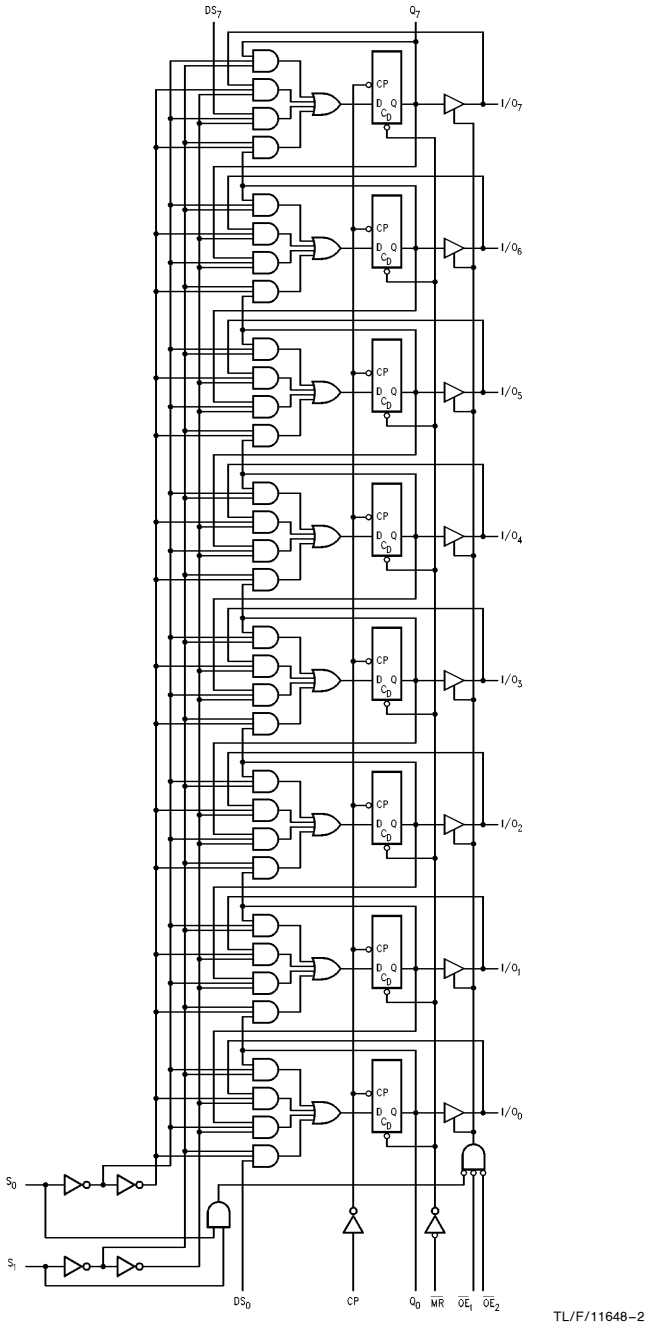

FIGURE 2. Logic Diagram

DOSE RATE TEST METHODOLOGY

To obtain a full understanding of the dose rate response of the DUT, a thorough test flow diagram was developed and implemented. Testing occurred at Boeing Radiation Effects Laboratory (BREL) in Seattle, Washington, utilizing a LINAC.

The 54AC299 was characterized for dose rate upset threshold levels, latchup windows, latchup levels, and survivability. Each irradiated device underwent a preradiation electrical test to establish its initial value. This was followed by different dose rate testings. To diminish instrumentation timing readjustments for each pulse width, 50 ns upset latchup testing was performed prior to widening the radiation pulse to 1 μs.

Dose rate upset testing was performed to determine the ''worst case'' threshold level for output transient upset both in the enabled and disabled conditions. The device was also tested for itnernal data loss (stored data data) resulting from the prompt gamma dose rate level.

Static conditions were irradiated first, establishing a reference point for internal upset and transient-output upset. Once these conditions were met, the short pulse radiation was applied and any transients on the output pins were recorded. Within 50 μs after the irradiation pulse, a functional test determined if internally-stored data was upset by the irradiation pulse.

The upset level was determined by successive approximation methodology, first at the lowest V_{CC} value. The lowest upset level was established at 4.0V DC; the next step increased V_{CC} to 5.0V DC, repeating the test without changing the dose rate level.

Dynamic testing determined if upset threshold levels changed at a lower dose rate when the DUT was clocked, compared with static condition results. In addition, the $+25°$ latchup test determined if latchup occurs at a lower dose rate when dynamic conditions are employed.

Several contributing factors can cause upset during dynamic operation when performing transient irradiation:

- Shift operating mode
- Stored data pattern when the radiation pulse occurs
- Radiation pulse width
- The relative position of the radiation pulse with respect to the clock's transition edge

For 50 ns testing, the radiation pulse was adjusted to occur at different times during the clock duty cycle. For 1 μs testing, the radiation pulse width was adjusted to encompass the entire clock pulse. If dynamic testing failed at lower upset levels than static conditions, this represented the final ''worst case'' upset threshold.

The objectives of dose rate latchup and survivability tests were:

- Determination of the device's susceptibility to latchup
- Determination of ''worse case'' conditions (temperature, V_{CC}) for producing latchup
- Recovery time measurements as a function of dose rate if latchup does not occur
- Survivability evaluation and degradation analysis when the device is subjected to high dose rate and prompt dose levels

Latchup tests began with the static conditions. Successive approximation methodology determined exact latchup levels. Various combinations of V_{CC} and temperature established the ''worst case'' condition.

An investigation was also performed to determine if latchup windows existed. The dose rate was slowly increased while observing the sample response for latchup. Four dose rate levels per decade using 1-2-4-8 sequence were employed at the maximum temperture ($+117°C$).

In addition, reliability tests were performed to:

- Demonstrate latchup survivability as a function of increasing number of exposures
- Investigate any total-dose-induced degradation resulting from cumulative ionizing dose delivered in the form of short duration, high intensity pulses

Electrical characterization before and after exposure to prompt radiation pulses during the reliability study determined if any parameter degradation has occurred. Failure of test items can result from device parameters which exceed specification limits as well as from functional failure.

DISCUSSION OF DOSE RATE TESTING: 54AC299

Several additional observations resulting from the dose rate testing and characterization are discussed here.

The first observation regards upset threshold levels. Rather than reflect the actual upset level of the device, upset levels were lower.

During the 50 ns pulse dose rate testing, observation suggested that apparent upset threshold levels resulted from transient spikes on power and/or ground pins. The test circuit was evaluated relative to the magnitude of inductance contained in the combination of device and test circuitry. Modifications were made to the test circuitry to improve and optimize the dose rate fixturing. This significantly improve testing accuracy.

As a result, series inductance must be considered a major detractor in establishing the true upset threshold level for a device, whether in a system design or in characterization testing. Care must be taken to minimize internal device inductance as well as the inductance occurring on the circuit board or in the overall system. This impacts the choice of device package, board design, and power supply design.

Utilizing the capacitor improve the 50 ns pulse dose rate upset threshold level by a factor of 1.53 to 2.05. Less improvement was observed for the 1 μs pulse dose rate upset threshold level (factor between 1.1 and 1.43). The 1 μs data is less affected due to the rise and fall times of the 1 μs radiation pulse being slower than the 50 ns pulse. Therefore, inductive effects are reduced for the wider pulse. Further investigation will determine if this apparent upset threshold level is a function of dose rate edge effect λ.

As a second observation, the lowest threshold was observed for HIGH state (HIGH to LOW transition) on the registers' outputs. A small change in dose rate caused an output to go from ''no upset'' to an ''upset'' condition. This was an extremely sharp response. In the majority of cases, all eight outputs changed from HIGH to LOW state; in some cases only one or a few outputs changed. But with a small increase in dose rate, all otuputs changed. Variances in upset threshold levels between different outputs were insignificant and in most cases could not be accurately measured. It was noted that the surge current at dose rate levels was significantly high, with a peak range between 300 mA–1.0A.

As a third observation, the dose rate pulse impacted the upset threshold level when the device outputs were in the disable (high impedence) state. Internally stored data in the disabled condition was upset at the same dose rate level when in the active mode. However, the output voltage in the disabled state is affected by both the radiation pulse and the load connected to the disabled output.

If the amplitude of these transient voltages on the disabled outputs is of sufficient magnitude, then the interface circuitry would interpret it as a change in logic state. It was observed that the magnitude and duration of radiation-induced transient voltages on the I/O pins is a function of the output loading. Additionally, the transient pulse in every case was positive-going with the transient pulse's amplitude increasing with increased dose rate. Therefore, transient upset in the disabled state is dependent upon circuit application, output loading, and the upset definition of criteria. Recovery time is also dependent upon output loading. Disabled state recovery time is fast when using low impedance output load with minimum capacitive loading on the I/O.

Finally, extensive dose rate testing of the same device samples are avoided in order to reduce any impact of total ionization damage. The 50 ns pulse contained a total dose value of 500 rad(Si) while the 1 μs pulse contained 5000 rad(Si). The inability to load and shift new data patterns was another and test condition that was utilized to indicate that a latchup condition has occurred.

Upon completion of all dose rate testing, all irradiated units and control units were retested and electrically characterized at $+25°C$ to assure that each device met the specification limits. This ensured that all previous testing was completely performed and that these functional parts were not significantly degraded by total dose radiation or electrical overstress.

When testing FACT products, any inductance in the test circuit impacts the measured radiation upset levels of the DUT. Therefore, it is very important to minimize or negate any inductance. Otherwise, the peak surge current value interferes with the accurate measurement of the upset level by as much as 50% change.

CONCLUSION

Analysis of the FACT 54AC299 upset test data indicates that minimum upset threshold levels occurred under the worst case conditions or a wide pulse (1 μs), lowest V_{CC} voltage (4.0V DC), and the DUT in the dynamic operating mode. Measured minimum upset levels were 1.90 to 2.22 x 10^9 rad (Si)/sec for these test conditions.

Static operation, using the same set of test conditions, showed a range of minimum upset levels rom 2.56 to 2.80 x 10^9 rad(Si)/sec. *Figures 3* and *4* are representative of upset results.

Narrow pulse (50 ns) data demonstrated radiation upset levels from 4.40 to 5.66 x 10^9 rad(Si)/sec under dynamic operation.

In addition, these factors also affected upset level sensitivity:

- The output states of the device
- The relative position between the occurrence of the radiation pulse and the device's clock pulse

The lowest threshold, for transient output as well as for internal upset, occurred with the outputs in the HIGH state and the radiation pulse occurring on the rising clock edge. Associated with these radiation upset levels were power supply surge currents. Peak surge current values ranged between 300 mA and 1.0A. Table III shows data for narrow pulse and wide pulse upset testing. While considerable effort was made to reduce and eliminate inductance, the final upset threshold levels may still be partially due to inductive effects, both internal and external to the 54AC299 device.

Upset threshold levels in the high impedance (disabled) state of the DUT consist of:

- A state change in the internal storage elements
- Transient voltages at the I/O pins which could be falsely detected by interfacing circuitry as a change in logic state

The magnitude and duration of the transient voltages on the I/O pins in the disabled state were very dependent on the output loading on these pins. Transient response was always positive-going with its amplitude rising with increasing dose rate. These tests results demonstrate that the transient characterization of the disabled state are complex without specific loading conditions and/or upset criteria being defined.

Using more resistive loading rather than reactive loading on I/O pin reduces the disabled state recovery time. Disabled state testing also showed that the internal upset level was unaffected whether the output pin was active or disabled.

Upon completion of radiation upset testing, latchup and survivability tests were performed at $+25°C$, $+80°C$, $+100°C$, and 116°C for $V_{CC} = 4.5V$ DC, 5.0V DC, and 5.5V DC. Test results indicated no latchup occurred for either narrow pulse (50 ns) or wide pulse (1 μs) radiation. The radiation test level for narrow pulse was 10^{10} rad(Si)/sec at $+25°C$. Due to the heating circuit of the tester, the highest radiation level was limited at $+117°C$ to 7.5 x 10^9 rad(Si)/sec. *Figures 5* and *6* are examples of latchup test results. After completion of latchup and survivability tests, verification of latchup windows was performed. Test results indicate no existence of latchup windows or burnout under worst case conditions for narrow and wide pulse radiation.

Observations showed that the peak surge current is linear with dose rate for both 50 ns and 1 μs pulse widths. The wide pulse surge current indicated both prompt and delayed components. The delayed component had a 1 μs fall time. Both the narrow and wide pulse widths for these latchup tests had surge current recovery times at the highest levels of 2 μs or less. Table IV shows the latchup test results.

Table V is the reliability study summary. Results show that no significant degradation occurred from performing multiple exposures of 500 rad(Si) while biased at maximum $V_{CC} = 5.5V$ DC. The total dose levels were 1, 2, 4, 6, 8, and 10 krad(Si). In addition to these reliability study results, other samples received total dose level between 25 to 70 krad(Si). Post irradiation electrical parameter measurements indicated that only I_{CC} shows any significant change as a result of radiation testing; the maximum change in I_{CC} was less than 1.5 μA.

Overall results of this comprehensive dose rate testing indicate that products built on the FACT process, such as the 54AC299, are latchup immune with an upset level greater than 10^9 rad(Si)/sec. FACT products offer system and circuit designers a cost effective solution for radiation hardness in both tactical and space environments.

TABLE I. FACT CMOS Process

PROCESS FEATURES

- P-well
- EPI starting material
- Stepper-based lithography
- Positive resist
- Dry etch
- Oxide isolation
- 250A gate oxide
- Single polysilicon
- 1.3 micron typical Leff (N and P)
- 1 ns typical gate delay (5V V_{CC}, room temperature, fanout-3)
- Sputtered dual-layer A1-Si metal
- Sputter etch planarizations
- Silicon nitride passivation

TOPOGRAPHY FEATURES

- 2 micron geometries and spacings
- 4.5 micron metal 1 pitch
- 0.5 micron alignment

TABLE II. FACT CMOS Process

Mask	Name	Description
1	Active	Defines Active areas
2	P-well	Defines P-well areas
3	Polysilicon	Defines poly gates and interconnects
4	N+ implant	Defines N+ areas for implant
5	Contact	Defines Metal 1 contacts to N+, P+, and Polysilicon
6	Metal 1	Defines Metal 1 interconnect
7	Via	Defines Metal 2 contacts to Metal 1
8	Metal 2	Defines Metal 2 interconnect
9	Passivation	Opens bond pads

TABLE III. 54AC299 Dose Rate Upset Summary, Active Outputs

V_{CC} S/N	Static Conditions		Dynamic Conditions	
	4.0V [E9] rad(Si)	5.0V [E9] rad(Si)	4.0V [E9] rad(Si)	5.0V [E9] rad(Si)
	50 ns Upset Thresholds			
11	6.11	8.44	5.66	
12	6.54	8.50	4.65	
13	6.26	7.99	4.74	
14	6.39	8.02	5.34	
15	5.69	8.26	4.65	
16	5.42	8.11	4.85	
17	6.35	8.13	4.87	
18	6.11	8.10	4.79	
19	5.99	7.84	4.40	
20	6.29	7.68	4.94	
Minimum:	5.42	7.68	4.40	
Maximum:	6.54	8.50	5.66	
Mean:	6.11	8.11	4.89	
	1 μs Upset Thresholds			
21			1.90	2.27
22			1.93	2.46
23			1.99	2.40
24			2.08	2.66
25			2.10	2.57
26			1.94	2.66
27			1.99	2.64
28			2.11	2.42
29			2.11	2.32
30			2.22	2.44
Minimum:			1.90	2.27
Maximum:			2.22	2.66
Mean:			2.04	2.48

TABLE IV. Latchup Test Results: Static Condition

Rad Pulse Width	Temperature			
	+25°C	+80°C	+100°C	+117°C
50 ns	No Latchup	No Latchup	No Latchup	No Latchup
1 μs	No Latchup	No Latchup	No Latchup	No Latchup

TEST CONDITIONS

Pulse Width: 50 (+4) ns
V_{CC} Voltage: +5.50V_{DC}
Temperature: +25°C
Test No.: 5 (active outputs, 01010101 pattern)

TABLE V. 54AC299 Reliability Study Summary

S/N	Shot No.	Dose Rate x IE10 [rad(Si)]	Dose Rate Shot [rad(Si)]	Total Dose [rad(Si)]	I_{CC}		Current Delta I_{CC} (mA)	Normalized [mA PER IE9] [rad(Si)]
					Pre (mA)	Post (mA)		
6	1	1.02	520		2.37	3.15	1,028	101
	2	1.04	533	1,053	2.36	3.16	1,048	101
7	1	1.04	521		2.51	3.20	1,000	96
	3	1.02	505		2.49	3.19	988	97
	3	1.05	513		2.40	3.19	995	95
	4	1.06	528	2,067	2.49	3.19	1,006	95
8	1	1.06	530		2.45	3.18	1,019	96
	2	1.05	528		2.43	3.17	1,020	97
	3	1.03	521		2.43	3.17	1,031	100
	4	1.05	518		2.42	3.16	1,022	97
	5	1.04	524		2.41	3.17	1,011	97
	6	1.06	526	3,147	2.43	3.16	1,008	95
9	1	1.07	546		2.47	3.17	990	93
	2	1.04	527		2.46	3.17	995	96
	3	1.06	538		2.45	3.19	994	94
	4	1.03	521		2.46	3.16	998	97
	5	1.06	518		2.45	3.17	986	93
	6	1.08	538		2.43	3.17	997	92
	7	1.05	543		2.43	3.17	998	95
	8	1.03	521	4,252	2.43	3.17	995	97
10	1	1.08	540		2.37	3.17	1,016	94
	2	1.07	534		2.38	3.17	1,006	94
	3	1.03	520		2.37	3.15	1,011	98
	4	1.03	538		2.37	3.15	1,019	99
	5	1.06	540		2.37	3.16	1,013	96
	6	1.06	533		2.36	3.15	1,011	95
	7	1.05	537		2.36	3.15	1,013	96
	8	1.03	529		2.36	3.16	1,014	99
	9	1.05	537		2.36	3.15	1,003	96
	10	1.05	539	5,353	2.36	3.16	1,002	95
Minimum:		1.02	505		2.36	3.15	986	92
Maximum:		1.08	546		2.51	3.20	1,048	101
Mean:		1.05	529		2.42	3.17	1,008	96

Notes: All outputs in the HIGH state upset to the LOW state on each radiation pulse.
All samples successfully passed post-exposure functional test without removing V_{CC}.

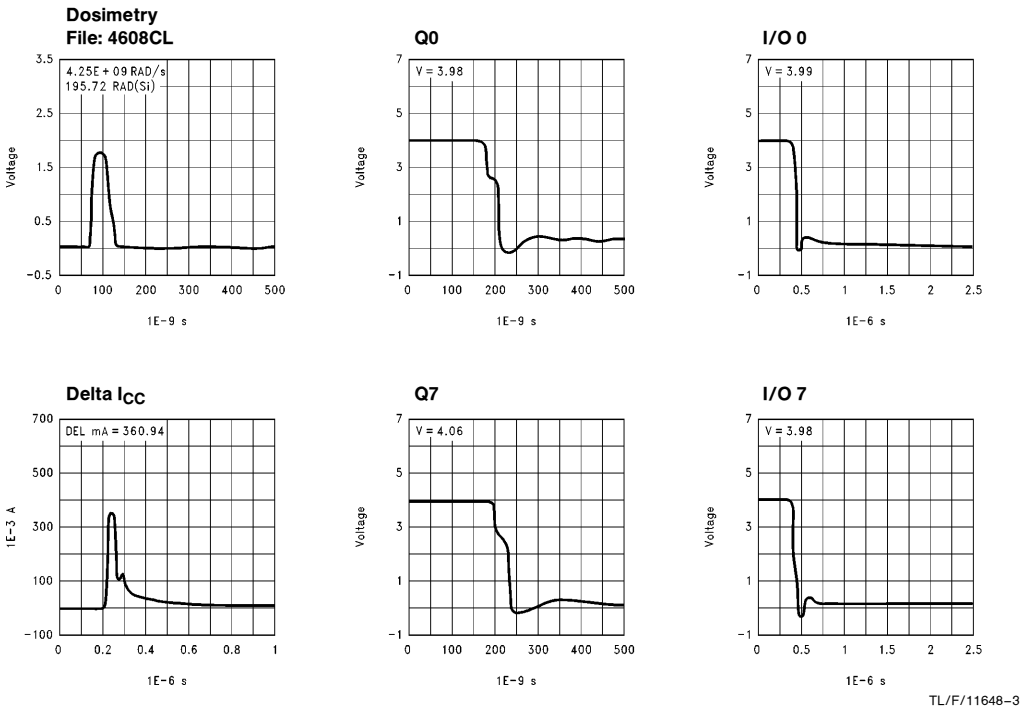

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FIGURE 3. 54AC299 Dose Rate Characterization Upset Threshold Test, +25°C

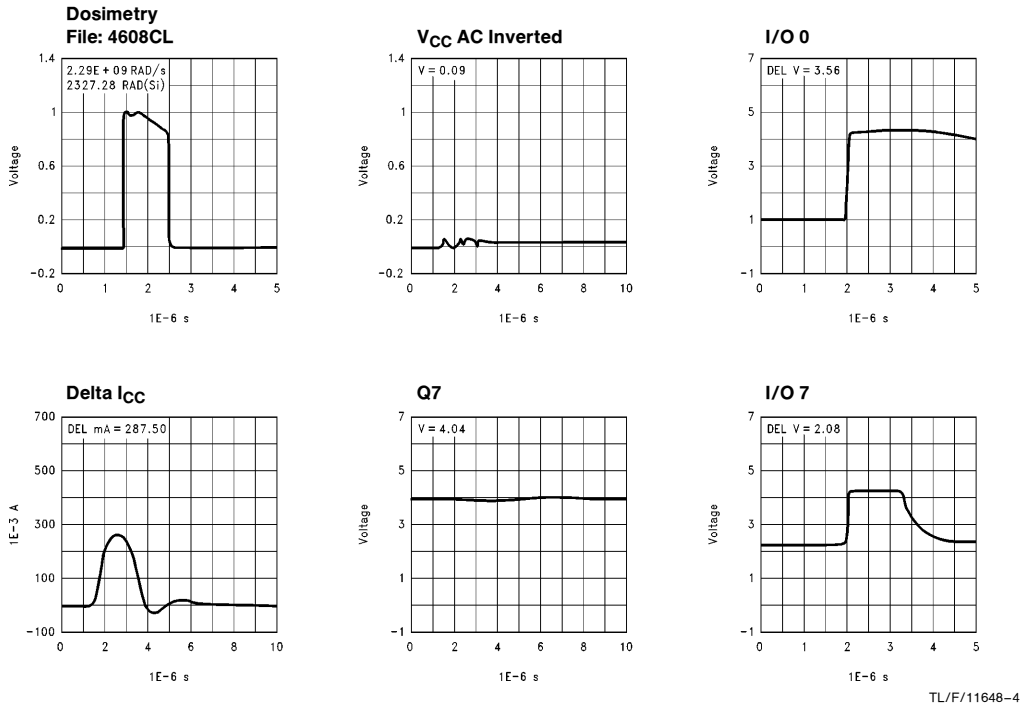

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FIGURE 4. 54AC299 Dose Rate Characterization Upset Threshold Test, +25°C

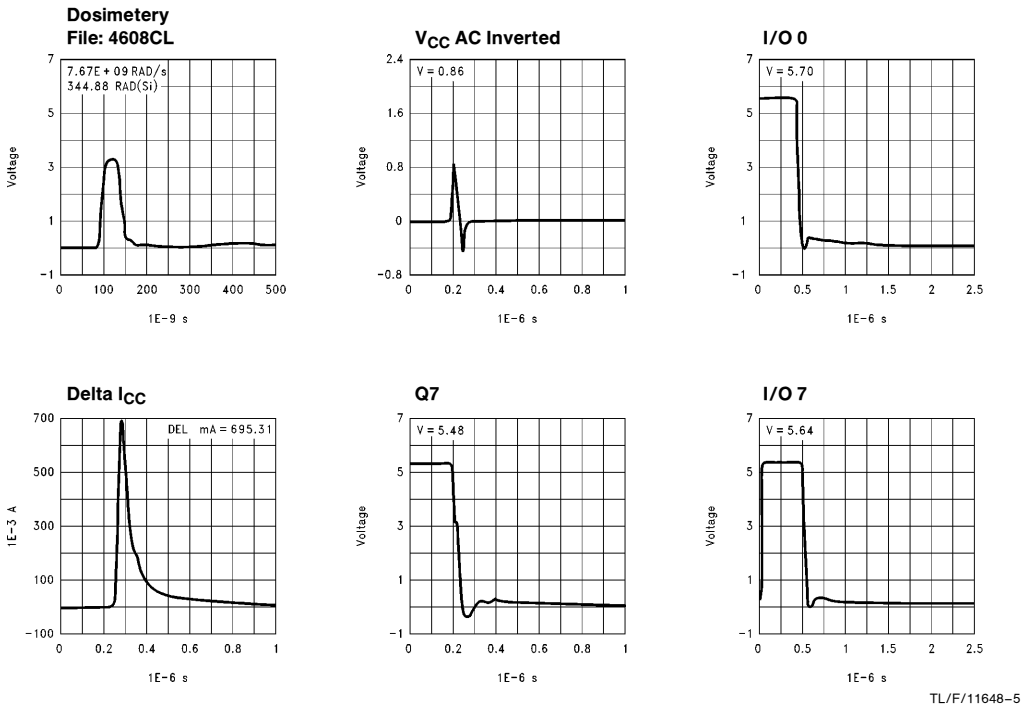

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FIGURE 5. 54AC299 Dose Rate Characterization Latchup/Survivability Test, + 117°C

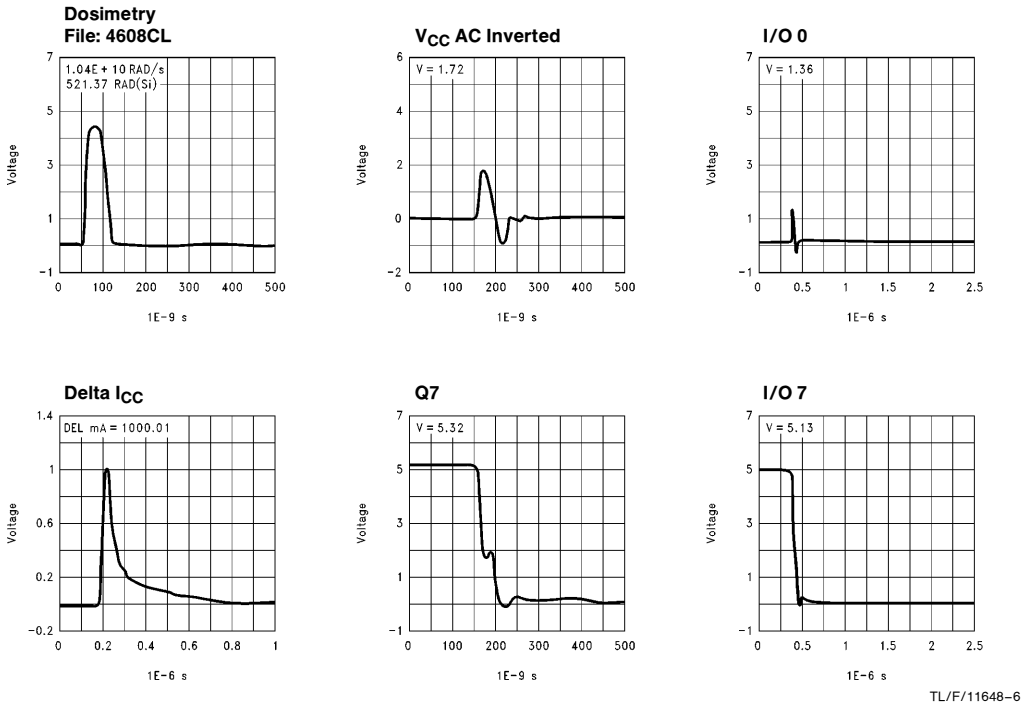

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FIGURE 6. Dose Rate Characterization Latchup/Survivability Test, + 25°C

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