Loopback Diagnostics Using the DP8390/ 901/902/905

National Semiconductor
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Bonnie Wilson
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1.0 OVERVIEW

Loopback capabilities are provided on the DP8390/901/902/905 to perform certain tests in order to validate operation of the device prior to transmission and reception of packets on a live network. Typically these tests may be performed during power up and initialization of a node.

This document describes the different loopback modes and their operation in the DP8390/901/902/905. There are several restrictions during loopback that are also discussed. Detailed instructions on how to generate different loopback tests are given, as well as the actual code that generates the tests (Appendix A). This document also discusses variations in loopback results caused by several common configuration errors.

Throughout this document, the term NIC refers to the controller, SNI refers to the ENDEC, CTI refers to the Coaxial Transceiver Interface, and TPI refers to the Twisted Pair Interface. These devices comprise the NIC chip set. The NIC family consists of the DP8390, DP83901, DP83902, and DP83905.

The loopback diagnostics verify:

1. The integrity of the data path through each block; received data is checked against transmitted data.
2. The CRC logic's capability to generate good CRC on transmit.
3. The CRC checking capability of the NIC on receive.
4. The address recognition logic's ability to accept packets that have a matching address and reject packets that fail to match an address.

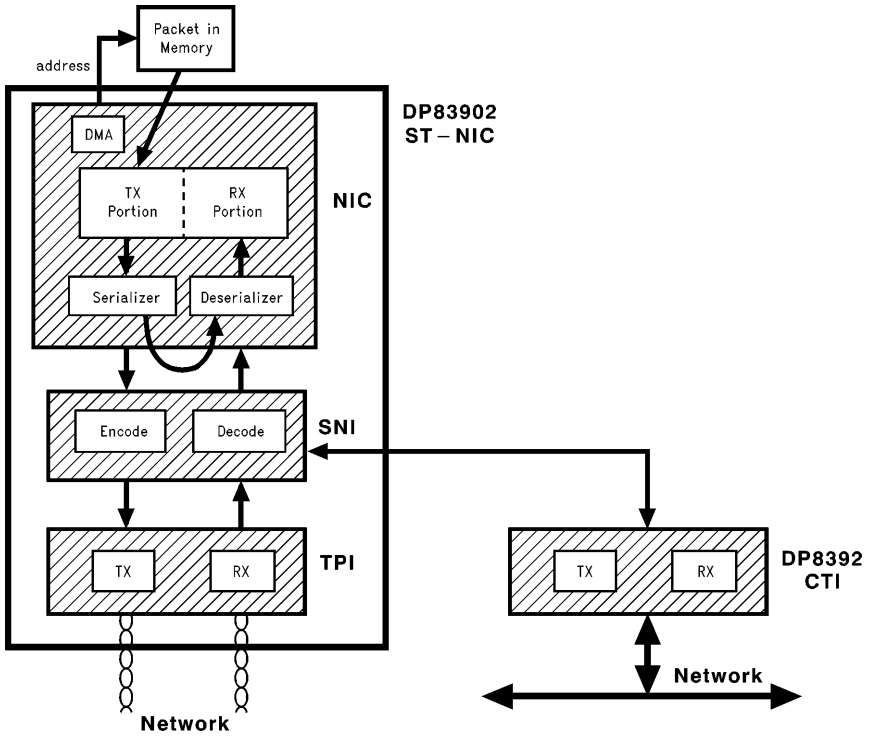

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FIGURE 1. Loopback Mode 1: Through the Controller Module

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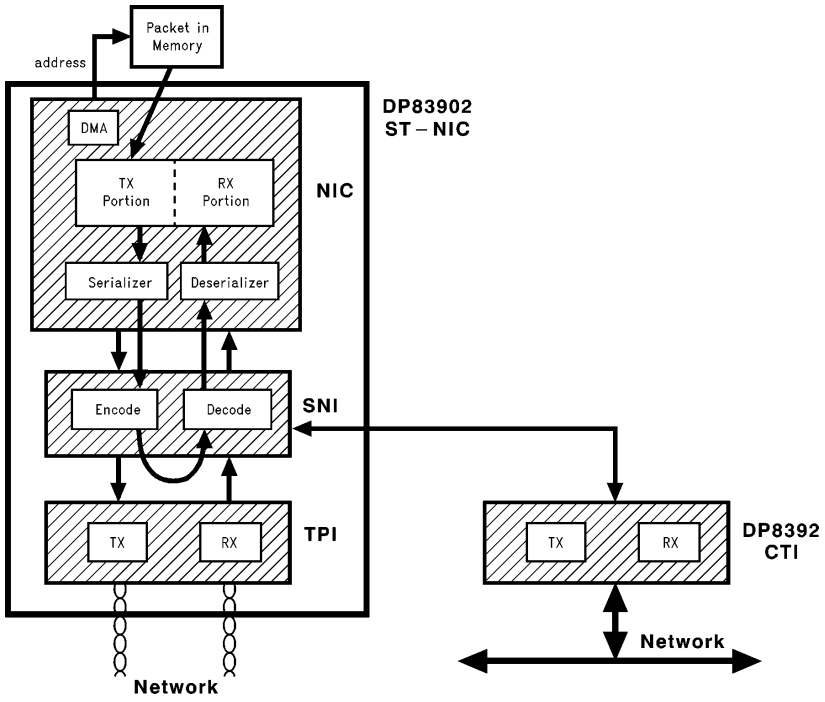

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FIGURE 2. Loopback Mode 2: Through the Encoder/Decoder

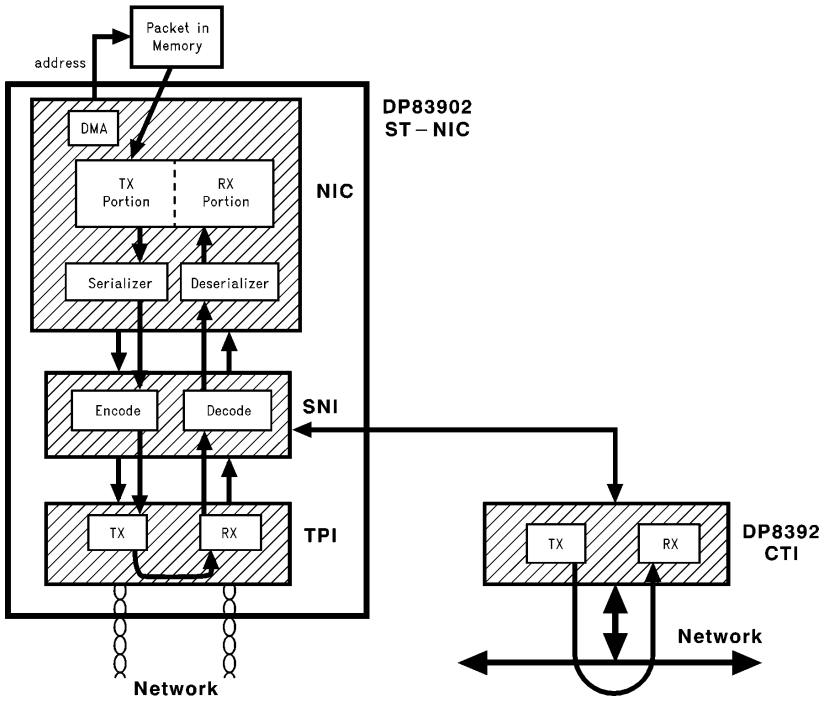

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FIGURE 3. Loopback Mode 3: Through the TPI or CTI

2.0 LOOPBACK MODES

Loopback modes are selected by programming bits LB0 and LB1 in the Transmit Configuration Register. *Figures 1, 2,* and *3* illustrate the loopback paths using the DP83902 as an example. The NIC family supports three modes of loopback:

MODE 1 (LB1 = 0, LB2 = 1): Internal loopback through the Controller Module only *(Figure 1)*. The Controller Module's serializer is connected to the deserializer.

MODE 2 (LB1 = 1, LB2 = 0): Internal loopback through the ENDEC Module *(Figure 2)*. The NIC provides a control (LPBK) that forces the ENDEC module or the DP8391 SNI to loop back all signals.

MODE 3 (LB1 = 1, LB2 = 1): External loopback through the TPI or DP8392 CTI *(Figure 3)*. For coaxial cable, packets are transmitted to the cable to check all of the transmit and receive paths and the cable itself. For twisted pair cable, packets are looped internal to the TPI.

3.0 LOOPBACK OPERATION IN THE NIC

To initiate a loopback test, a packet must first be assembled and transferred into the NIC buffer memory. Next, the Transmit Page Start Register, Transmit Byte Count Registers, Transmit Configuration Register, and Data Configuration Register must be programmed. Finally, the transmit command is issued to the Command Register, causing the following operations to occur:

3.1 Transmitter Actions

1. Data is transferred from memory by local DMA until the FIFO is filled. Subsequent burst transfers to refill the FIFO are initiated when the number of bytes in the FIFO drops below the programmed threshold. During the transfers the Transmit Byte Count Registers (TBCR0 and TBCR1) are decremented.
2. The NIC generates 56 bits of preamble followed by an 8-bit Start of Frame Delimiter.
3. Data is transferred from the FIFO to the serializer.
4. If the Inhibit CRC bit is set in the Transmit Configuration Register, no CRC is calculated by the NIC. In this case, a software CRC can be appended after the data field in buffer memory. If the Inhibit CRC bit is not set, the NIC calculates and appends four bytes of CRC to the end of the data field.
5. At the end of transmission, the Packet Transmitted bit is set in the Interrupt Status Register.

3.2 Receiver Actions

1. After the preamble and Start of Frame Delimiter have been decoded, the incoming packet starts filling the FIFO. See Section 5.0 for a description of the packet storage in the FIFO. The packet is not stored in buffer memory.
2. The receive byte count is incremented for each incoming byte.
3. If the Inhibit CRC bit is set in the Transmit Configuration Register, the receiver checks the incoming packet for CRC errors. If the Inhibit CRC bit is not set in the Transmit Configuration Register, the receiver does not check for CRC errors and the CRC error bit is set in the Receive Status Register.
4. At the end of receive, the receive byte count is written into the FIFO and the Receive Status Register is updated. The Packet Received Intact bit is typically set in the Receive Status Register even if the address does not match. If CRC errors are forced, the packet's destination address must match the address filters in order for the CRC error bit in the Receive Status Register to be set.

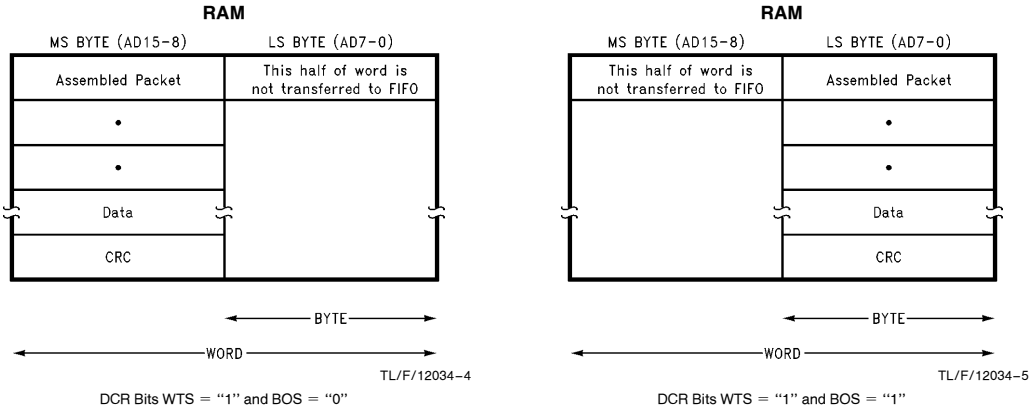

FIGURE 4. Packet Assembly for Loopback Word Wide Transfers

4.0 RESTRICTIONS USING LOOPBACK

Since the NIC is a half-duplex device, several compromises were required for the implementation of loopback diagnostics. The restrictions placed on the use of loopback diagnostics are as follows:

1. The FIFO is split into two halves to allow some buffering of incoming data. The NIC transmits through one half of the FIFO and receives through the second half. Only the last five bytes of a packet can be examined in the FIFO (see Section 5) since the DMA does not store the loopback packet in memory. Thus loopback can be considered a modified form of transmission.
2. Splitting of the FIFO has some bus latency implications. The FIFO depth is halved, thus reducing the amount of allowed bus latency. The Loopback Select bit (D3) in the Data Configuration Register should be set to allow all local DMA transfers to continue until the FIFO is filled. In cases where the latency constraints cannot be accommodated, small 7 byte packets can be transmitted. In addition, the FIFO must only be read (by successfully reading port 06h) during loopback mode; reading the FIFO in other modes will result in the NIC's failing to issue the ACK signal properly.
3. The receiver and the transmitter share the CRC logic, thus the NIC cannot generate and check the CRC simultaneously. That is, if the Inhibit CRC bit is not set in the Transmit Configuration Register, the NIC will generate and append the CRC. Software must then be used to verify the CRC by comparing the CRC from the FIFO with a previously calculated CRC. On the other hand, if the Inhibit CRC bit is set in the Transmit Configuration Register, the NIC receiver will verify the CRC appended by software.
4. Address recognition logic must be checked indirectly through a small series of tests (for further explanation see Group III Loopback Tests: Address Recognition).
5. Between consecutive transmissions in loopback mode, the NIC must be reset to guarantee alignment of the FIFO pointers when data is read from the FIFO. The following series of steps must be taken to reset the NIC and realign the FIFO pointers:
   a) Set the Transmit Configuration Register to 00h.
   b) Reset the Command Register to 21h, followed by a wait state of at least 1.5 ms for the NIC to reset.
   c) Program the desired loopback mode into the Transmit Configuration Register.
6. Loopback only operates with byte wide transfers, thus special considerations must be made with word wide transfers. Since the FIFO is split, only half of each word is transferred into the transmit portion of the FIFO. The Byte Order Select bit in the Data Configuration Register can be used to select which half of the word is written into the FIFO (see *Figure 4*). Although a word is transferred to the NIC, only a byte is transmitted in the loopback packet. To properly transfer all the bytes in the loopback packet, the byte count must be 2 times the actual number of bytes assembled in the loopback packet.
7. During heavily loaded network conditions, external loopback through the TPI or CTI could fail due to interference from the network.

5.0 ALIGNMENT OF DATA IN THE FIFO

During loopback, eight bytes of the FIFO are used for transmission and eight bytes are used for reception. Reception of the packet begins at location zero, and after the pointer reaches the last location in the receive portion of the FIFO, the pointer wraps back to location zero, overwriting the previously received data (see *Figure 5*). The pointer continues to circulate through the FIFO until the last byte is received. The NIC then appends the lower receive byte count and two copies of the upper receive byte count into the next three locations in the FIFO. Thus, only the last five bytes of the received packet may be retrieved.

Note: Although the size limit of a loopback packet is 64 Kbytes, the byte counter rolls over at 2048 bytes.

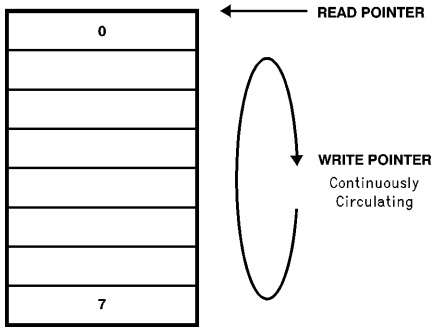

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FIGURE 5. Continuously Circulating FIFO Write Pointer during Loopback

To achieve the packet alignment shown in *Figure 6* below, the packet length should be (N*8)+5 bytes (i.e. 13, 21, etc.). If the CRC is appended, the second through fifth byte will be the CRC appended by the NIC. This allows the CRC to be extracted from the NIC and compared to a previously calculated value for verification.

FIFO LOCATION	FIFO CONTENTS	
0	Byte (N*8)+1	First Byte Read
1	Byte (N*8)+2 (CRC 1)	Second Byte Read
2	Byte (N*8)+3 (CRC 2)	•
3	Byte (N*8)+4 (CRC 3)	•
4	Byte (N*8)+5 (CRC 4)	•
5	Lower Byte Count	•
6	Upper Byte Count	•
7	Upper Byte Count	Last Byte Read

FIGURE 6. Alignment of Packet in FIFO Following Loopback

6.0 LOOPBACK TESTS

Three types of loopback tests may be performed to verify the data path through the DP8390/901/902/905. The tests are as follows:

1. Group I tests verify the CRC generation capability of the NIC. In this case, the NIC generates and appends a CRC to the loopback packet, and software is used to verify a matching CRC.
2. Group II tests verify the CRC recognition capability of the NIC. Here, the NIC verifies a software generated CRC.
3. Group III tests verify the address recognition logic of the NIC.

The loopback tests which follow were performed on the DP83902EB-AT PC-AT Compatible DP83902 ST-NIC Ethernet Evaluation Board. During each of the loopback tests, the Data Configuration Register was programmed to 41h, which selects loopback mode and word transfers. Refer to Appendix A for the actual source code necessary to perform Group I loopback.

6.1 Group I Loopback Tests: CRC Generation

The basic steps necessary to perform the Group I loopback tests (in which the CRC is appended by the NIC) are as follows:

1. Set Command Register to 21h (page 0).
2. Initialize Data Configuration Register to 41h (loopback mode and word transfers).
3. Initialize Receive Configuration Register to 1Fh (promiscuous mode).
4. Initialize Transmit Byte Count Registers and Transmit Page Start Register.
5. Set Command Register to 22h (start mode).
6. Create loopback packet and transfer into NIC buffer memory.
7. Transmit dummy packet to check for unterminated or unconnected cable by performing the following steps:
   a) Set Transmit Configuration Register to 00h (normal operation).
   b) Write FFh to Interrupt Status Register to reset.
   c) Set Command Register to 26h (transmit). Note that the Command Register must first be in start mode (22h) before transmitting (26h).
   d) Loop until the Packet Transmitted bit is set in the Interrupt Status Register. If the time-out loop completes and this bit is not set, the transmit has timed out, and the cable may not be connected.
   e) Check Interrupt Status Register for 08h (Transmit Error). If the Transmit Error bit is set, excessive collisions have occurred, and the cable may not be terminated.
8. Start loopback mode 1 test (TCR = 02h) by performing the following steps:
   a) Reset Transmit Configuration Register to 00h.
   b) Reset Command Register to 21h. If the NIC is currently receiving a packet, it will wait for the reception of the current packet to complete before it will reset. Thus, a wait state of at least 1.5 ms is necessary to insure that the NIC will completely reset.
   c) Program the Transmit Configuration Register to the appropriate loopback mode, in this case mode 1 loopback (TCR = 02h).
   d) Write FFh to Interrupt Status Register to reset.
   e) Set Command Register to 22h (start mode).
   f) Set Command Register to 26h (transmit).
   g) Wait for transmit to complete (Command Register = 22h).
   h) Check Interrupt Status Register for 06h (good transmission).
   i) Read FIFO and compare CRC with previously calculated CRC.
9. Start loopback mode 2 test (TCR = 04h): See step 8.
10. Transmit a dummy packet to change the contents of the FIFO. This step must be taken to ensure that the cable is connected. If the cable is not connected, the NIC does not receive anything into its FIFO during external loopback; therefore if the contents of the FIFO have not been changed, the disconnected cable is not detected. See step 7.
11. Start loopback mode 3 test (TCR = 06h): See step 8.
12. If mode 3 loopback fails, transmission may have been aborted due to excessive collisions (check the Transmit Status Register). In this case network traffic has interfered, but the CTI or TPI may still be operational.

GROUP I RESULTS

The following examples show what results can be expected from a properly operating NIC during Group I loopback operations. The restrictions and results of each loopback mode are listed for reference.

Internal Loopback through the NIC

Loopback Path	TCR	RCR	TSR	RSR	ISR
Mode 1 (NIC)	02H	1FH	51H	02H	06H

TSR: Before transmission of the loopback packet, Carrier Sense and Collision inputs are monitored (as required by CSMA/CD protocol). Once the NIC gains access to the network for transmission, the Carrier Sense and Collision Detect inputs are ignored. Thus, the Carrier Sense Lost and CD Heartbeat bits are always set in the Transmit Status Register.

RSR: CRC errors are always indicated by the receiver if the CRC is appended by the transmitter.

ISR: Only the Packet Transmitted and Receive Error bits in the Interrupt Status Register are set; the Packet Received bit is set only if status is written to memory. In loopback this action does not occur, hence the Packet Received bit remains 0 for all loopback modes.

Internal Loopback through the SNI

Loopback Path	TCR	RCR	TSR	RSR	ISR
Mode 2 (SNI)	04H	1FH	41H	02H	06H

TSR: CD Heartbeat is set in the Transmit Status Register; Carrier Sense Lost is not set since it is generated by the external encoder/decoder.

External Loopback through the TPI or CTI

Loopback Path	TCR	RCR	TSR	RSR	ISR
Mode 3 (TPI or CTI)	06H	1FH	01H	02H	06H

TSR: CD Heartbeat and Carrier Sense Lost should not be set. The Transmit Status Register could, however, also contain 01h, 03h, 07h, or a variety of other values depending on whether collisions were encountered or the packet was deferred.

ISR: The Interrupt Status Register will contain 08H if the packet is not transmittable.

General. During external loopback the NIC is now exposed to network traffic. It is therefore possible for the contents of both the receive portion of the FIFO and the Receive Status Register to be corrupted by any other packet on the network. Thus, in a live network, the contents of the FIFO and Receive Status Register should not be depended upon. The NIC will still abide by the standard CSMA/CD protocol in external loopback mode (the network will not be disturbed by the loopback packet).

6.2 GROUP II LOOPBACK TESTS : CRC RECOGNITION

The basic steps necessary to perform the Group II loopback tests (in which a software CRC is appended to the packet) are similar to those outlined previously for the Group I tests, with the following exceptions:

1. The loopback packet created must have a software appended CRC.
2. When programming the Transmit Configuration Register to the desired loopback mode, the Inhibit CRC bit must be set.
3. After the loopback packet has been transmitted, check the Interrupt Status Register and/or the Receive Status Register for CRC errors. If a CRC error has occurred, the loopback test has failed.

GROUP II RESULTS

The following examples show what results can be expected from a properly operating NIC during Group II loopback operations. The restrictions and results of each loopback mode are listed for reference.

Internal Loopback through the NIC

Loopback Path	TCR	RCR	TSR	RSR	ISR
Mode 1 (NIC)	03H	1FH	51H	01H	02H

TSR: Before transmission of the loopback packet, Carrier Sense and Collision inputs are monitored (as required by CSMA/CD protocol). Once the NIC gains access to the network for transmission, the Carrier Sense and Collision Detect inputs are ignored. Thus, the Carrier Sense Lost and CD Heartbeat bits are always set in the Transmit Status Register.

ISR: Only the Packet Transmitted bit in the Interrupt Status Register is set. The packet received bit is set only if status is written to memory. In loopback this action does not occur, hence the Packet Received bit remains 0 for all loopback modes.

Internal Loopback through the SNI

Loopback Path	TCR	RCR	TSR	RSR	ISR
Mode 2 (SNI)	05H	1FH	41H	01H	02H

TSR: CD Heartbeat is set in the Transmit Status register; Carrier Sense Lost is not set since it is generated by the external encoder/decoder.

External Loopback through the CTI

Loopback Path	TCR	RCR	TSR	RSR	ISR
Mode 3 (TPI or CTI)	07H	1FH	01H	01H	02H

TSR: CD Heartbeat and Carrier Sense Lost should not be set. The Transmit Status Register could, however, also contain 01h, 03h, 07h, or a variety of other values depending on whether collisions were encountered or the packet was deferred.

ISR: The Interrupt Status Register will contain 08H if the packet is not transmittable.

General. During external loopback the NIC is now exposed to network traffic. It is therefore possible for the contents of both the receive portion of the FIFO and the Receive Status Register to be corrupted by any other packet on the network. Thus, in a live network, the contents of the FIFO and Receive Status Register should not be depended upon. The NIC will still abide by the standard CSMA/CD protocol in external loopback mode (the network will not be disturbed by the loopback packet).

6.3 Group III Loopback Tests: Address Recognition

The address recognition logic cannot be directly tested. However, the CRC Error and Frame Alignment Error bits in the Receive Status Register are set only if the address of the packet matches the address filters. Thus, if errors are expected to be set and they are not set, the packet has been rejected on the basis of an address mismatch.

One method of testing the address recognition logic is to transmit two loopback packets, one with a matching physical address, and one with a non-matching address and compare the results. The basic steps necessary to perform the Group III loopback tests are similar to those outlined previously for the Group I tests, with the following exceptions:

1. RCR must be programmed to 00H. (The physical address of the node must match the station address programmed in PAR0-PAR5.)
2. Two loopback packets must be setup, one with a non-matching physical address and one with a matching physical address.
3. Both packets must have a CRC appended by the NIC.

GROUP III RESULTS

The following examples show what results can be expected from a properly operating NIC during Group III loopback operations. The restrictions and results of matching and non-matching addresses are listed for reference.

Internal Loopback through the NIC: Matching Physical Address

Loopback Path	TCR	RCR	TSR	RSR	ISR
Mode 1 (NIC)	02H	00H	51H	02H	06H

TSR: Before transmission of the loopback packet, Carrier Sense and Collision inputs are monitored (as required by CSMA/CD protocol). Once the NIC gains access to the network for transmission, the Carrier Sense and Collision Detect inputs are ignored. Thus, the Carrier Sense Lost and CD Heartbeat bits are always set in the Transmit Status Register.

RSR: CRC errors should be seen in both the Receive Status Register and the Interrupt Status Register for an address matching packet.

ISR: Only the Packet Transmitted and Receive Error bits in the Interrupt Status Register are set; the Packet Received bit is set only if status is written to memory. In loopback this action does not occur, hence the Packet Received bit remains 0 for all loopback modes.

Internal Loopback through the NIC : Non-Matching Physical Address

Loopback Path	TCR	RCR	TSR	RSR	ISR
Mode 1 (NIC)	02H	00H	51H	01H	02H

TSR: Before transmission of the loopback packet, Carrier Sense and Collision inputs are monitored (as required by CSMA/CD protocol). Once the NIC gains access to the network for transmission, the Carrier Sense and Collision Detect inputs are ignored. Thus, the Carrier Sense Lost and CD Heartbeat bits are always set in the Transmit Status Register.

RSR: CRC errors should not be detected for a non-matching physical address.

ISR: Only the Packet Transmitted bit in the Interrupt Status Register is set. The packet received bit is set only if status is written to memory. In loopback this action does not occur, hence the Packet Received bit remains 0 for all loopback modes.

7.0 COMMON LOOPBACK CONDITIONS AND CORRESPONDING RESULTS

This section identifies some common variations in the loopback results from Section 6.0 which occur when the loopback tests or hardware are not configured properly.

7.1 Group I Loopback

If the coax cable is not terminated, the results will differ from those listed in Section 6.1 as follows:

Loopback Path	TCR	RCR	TSR	RSR	ISR
Mode 3 (CTI)	06H	1FH	0CH	02H	08H

If the coax cable is disconnected, the results will differ from those listed in Section 6.1 as follows:

Loopback Path	TCR	RCR	TSR	RSR	ISR
Mode 1 (NIC)	02H	1FH	40H	02H	00H
Mode 2 (SNI)	04H	1FH	40H	02H	00H
Mode 3 (CTI)	06H	1FH	00H	82H	00H

If the twisted pair cable is not connected and good link is enabled, the results will differ from those listed in Section 6.1 as follows:

Loopback Path	TCR	RCR	TSR	RSR	ISR
Mode 2 (SNI)	04H	1FH	51H	02H	02H
Mode 3 (TPI)	06H	1FH	51H	02H	02H

If the twisted pair cable is not connected, and good link is disabled, the results do not differ from those listed in Section 6.1.

If the packet has a non-matching physical address and promiscuous physical mode is not chosen in the Receive Configuration Register, the results will differ from those listed in 6.1 as follows:

Loopback Path	TCR	RCR	TSR	RSR	ISR
Mode 1 (NIC)	02H	00H	51H	01H	02H
Mode 2 (SNI)	04H	00H	41H	01H	02H
Mode 3 (TPI or CTI)	06H	00H	01H	01H	02H

7.2 Group II Loopback

If the coax cable is not terminated, the results will differ from those listed in Section 6.2 as follows:

Loopback Path	TCR	RCR	TSR	RSR	ISR
Mode 3 (CTI)	07H	1FH	0CH	01H	08H

If the coax cable is disconnected, the results will differ from those listed in Section 6.2 as follows:

Loopback Path	TCR	RCR	TSR	RSR	ISR
Mode 1 (NIC)	03H	1FH	40H	01H	00H
Mode 2 (SNI)	05H	1FH	40H	01H	00H
Mode 3 (CTI)	07H	1FH	00H	81H	00H

If the twisted pair cable is not connected and good link is enabled, the results will differ from those listed in Section 6.2 as follows:

Loopback Path	TCR	RCR	TSR	RSR	ISR
Mode 2 (SNI)	05H	1FH	51H	01H	02H
Mode 3 (TPI)	07H	1FH	51H	01H	02H

If the twisted pair cable is not connected, and good link is disabled, the results do not differ from those listed in Section 6.2.

7.3 Group III Loopback

If the coax cable is not terminated, the results do not differ from those listed in Section 6.3.

If the coax cable is disconnected, the results will differ from those listed in Section 6.3 as follows:

Packet Contents	TCR	RCR	TSR	RSR	ISR
Matching Physical Address	02H	00H	40H	01H	00H
Non-Matching Physical Address	02H	00H	40H	01H	00H

If the twisted pair cable is not connected, regardless of good link pin's state, the results do not differ from those listed in Section 6.3.

APPENDIX A: LOOPBACK CODE

The code below will execute the Group I loopback tests, following the description in Section 6.1. When executed, the FIFO and register contents are printed to an output file (output.txt unless specified differently). Refer to AN-874, Writing Drivers for the DP8390 NIC Family of Ethernet Controllers, for a description of the PCtoNIC routine used in this program.

```
#include <stdio.h>
#include <stdlib.h>
#include <string.h>
#include <sys/timeb.h>
#include "nic.hpp"

void stepEight(int TCRValue);
void HardReset(void);
void doDelay(int DelayTime);
int pktTransmit(void);

char DummyCRC[] = {0x53,0x58,0x7a,0xba};        /*DummyPacket's CRC Value*/
char PacketCRC[] = {0x85,0x62,0x9e,0xb6};       /*Packet's CRC Value*/

FILE *TheFile = NULL;                           /*Output file*/

void main(int argc,char *argv[])
{
int x;                              /*counter*/
char Packet[128];                   /*Packet to be transmitted*/
char DummyPacket[128];              /*Another packet to be transmitted*/
char FileName[11] = "output.txt";   /*Output File*/
      HardReset();                  /*Perform a hardware reset on the NIC*/

/*The following code sets up the output file.*/

      if (argc == 2)
            strncpy(FileName,argv[1],11);
      TheFile = fopen(FileName,"w");
      if (TheFile == NULL)
      {
            printf("Error opening file!\n");
            exit(1);
      }

/*The following code creates the packets. Since the NIC will be in word mode,  */
/*the byte count is 2 times the actual number of bytes assemble and only every */
/*other byte is written to.                                                     */

      for (int x = 0; x < 128; x+=2)
            Packet[x + 1] = x;
      for (x = 0; x < 128; x+=2)
            DummyPacket[x + 1] =2*x;

      setReg(0x00,0x21);      /*1. Set Command Register to 21h (page 0).*/
      doDelay(2);             /*   Wait at least 1.5ms to insure the NIC resets*/
      setReg(0x0E,0x41);      /*2. Initialize Data Configuration Register to*/
                              /*   40h.*/
      setReg(0x0c,0x1f);      /*3. Initialize Receiver Configuration Register*/
                              /*   to 1Fh (promiscuous mode).*/
```

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```
        setReg(0x05,120);       /*4. Initialize Transmit Byte Count Register 0 to*/
                                /*   120.*/
        setReg(0x06,0);         /*4. Initialize Transmit Byte Count Register 1 to*/
                                /*   0.*/
        setReg(0x04,0x40);      /*4. Initialize Transmit Page Start Address to*/
                                /*   40h.*/
        setReg(0x00,0x22);      /*5. Set Command Register to 22h (start mode).*/
        PCtoNIC(Packet,120,0x4000,0); /*6. Transfer loopback packet into NIC*/
                                      /*   buffer memory.*/
        setReg(0x0d,00);  /*7a. Set Transmit Configuration Register to 00h*/
                          /*    (normal operation).*/
        setReg(0x07,0xff);      /*7b. Write FFh to Interrupt Status Register to*/
                                /*    reset.*/
        setReg(0x00,0x26);      /*7c. Set Command Register to 26h (transmit).*/

  /*7d. Loop until the Packet Transmitted bit is set in the Interrupt Status*/
  /*    Register or until it's determined that a timeout has occurred.      */
  /*    If the timeout loop completes, the transmit has timed out.          */

        if (!pktTransmit)
        {
              /*7e. If the Interrupt Status Register equals 08h (Transmit Error),*/
              /*    excessive collisions have occurred and the cable may not be*/
              /*    terminated.*/
              if (readReg(0x07) == 8)
                    printf("Transmit error bit set. Cable may not be
                    terminated.\n");
              /*If the Interrupt Status Register does not equal 08h, the cable*/
              /*may not be connected.*/
              else printf("Transmit timed out. Cable may not be connected.\n");
              fclose(TheFile);
              exit(1);
        }
        fprintf (TheFile,"Group I Loopback Tests: CRC Generation\n\n");
        fprintf(TheFile,"Mode 1 Loopback (TCR = 02)\n\n");
        stepEight(2);     /*8. Start loopback mode 1 test.*/
        fprintf(TheFile,"\nMode 2 Loopback (TCR = 04)\n\n");
        stepEight(4);     /*Start loopback mode 2 test.*/

        PCtoNIC(DummyPacket,120,0x4000,0);  /*Transfer different packet into NIC*/
                                            /*buffer memory for mode 3 looopback.*/

        fprintf(TheFile,"\nMode 3 Loopback (TCR = 06)\n\n");
        stepEight(6);     /*Start loopback mode 3 test.*/
        fclose(TheFile);
  }

  /*************************************************************************/
  /*stepEight:      Given the appropriate TCR value for loopback, this procedure*/
  /*                performs loopback.                                          */
  /*input:          TCRValue, the Transmit Configuration Register value         */
  /*************************************************************************/

  void stepEight(int TCRValue)
  {
  int x;  /*counter*/
```

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```
      setReg(0x0d,0);         /*8a. Reset Transmit Configuration Register to */
                              /*    00h.*/
      setReg(0x00,0x21);      /*8b. Reset Command Register to 21h.*/
      doDelay(2);             /* Wait at least 1.5ms to insure the NIC resets*/
      setReg(0x0d,TCRValue);  /*8c. Program the Transmit Configuration Register*/
                              /*    to the given loopback mode.*/
      setReg(0x07,0xff);      /*8d. Write FFh to Interrupt Status Register to*/
                              /*    reset.*/
      setReg(0x00,0x22);      /*8e. Set Command Register to 22h (start mode).*/
      setReg(0x00,0x26);      /*8f. Set Command Register to 26h (transmit).*/
      /*8g. Loop until transmit is complete*/
      while (readReg(0x00) != 0x22)
            ;
      /*8h. Check Interrupt Status Register for 06h (good transmission).*/
      if (readReg(0x07) != 0x06)
      {
            printf("Bad Transmission.  Interrupt status register\n");
            printf("does not equal 0x06\n");
      }
      /*8i. Read FIFO and compare CRC with previously calculated CRC.*/
      for (x = 0; x < 8; x++)
            fprintf(TheFile,"FIFO %d: %02X\n",x,readReg(FIFO));
      setReg(0x00,0xa2);      /*Set Command Register to A2h (page 2).*/
      fprintf(TheFile,"TCR: %02X\n",readReg(0x0d) & 0x1f);    /*Read TCR*/
      fprintf(TheFile,"RCR: %02X\n",readReg(0x0c) & 0x3f);    /*Read RCR*/
      setReg(0x00,0x22);      /*Set Command Register to 22h (page 0).*/
      fprintf(TheFile,"TSR: %02X\n",readReg(0x04) & 0xfd);    /*Read TSR*/
      fprintf(TheFile,"RSR: %02X\n",readReg(0x0c));           /*Read RSR*/
      fprintf(TheFile,"ISR: %02X\n",readReg(0x07));           /*Read ISR*/
}

/*****************************************************************************/
/*HardReset:      Performs a hardware reset on the NIC.                      */
/*****************************************************************************/

void HardReset(void)
{
      readReg(0x1f);
      setReg(0x1f,1);
      doDelay(2);
}

/*****************************************************************************/
/*doDelay:  A function that will wait a given amount of milliseconds and then */
/*          return                                                           */
/*input:    time in milliseconds                                             */
/*output:   none                                                             */
/*****************************************************************************/

void doDelay(int DelayTime)
{
struct timeb Start, Current;
short Start2, Current2;
      ftime(&Start);
      Start2 = (Start.millitm + (1000*(Start.time & 0x0f)));
      do
      {
            ftime(&Current);
```

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```
            Current2 = (Current.millitm + (1000*(Current.time & 0x0f)));
      } while ((Current2 - Start2) < DelayTime);
}

/*****************************************************************************/
/*pktTranmsit:    A function that loops until the Packet Transmitted bit is   */
/*                set in the Interrupt Status Register or a timeout has       */
/*                occurred (waits one second)                                 */
/*input:          none                                                        */
/*output:         Returns 1 if Packet Transmitted bit is set                  */
/*                Returns 0 if a timeout occurs                               */
/*****************************************************************************/

int pktTransmit(void)
{
struct timeb Start, Current;
short Start2, Current2;
      ftime(&Start);
      Start2 = (Start.millitm + (1000*(Start.time & 0x0f)));
      do
      {
            if ((readReg(0x07) & 2) !=0)
                  return 1;
            ftime(&Current);
            Current2 = (Current.millitm + (1000*(Current.time & 0x0f)));
      } while ((Current2 - Start2) < DelayTime);
      return 0;
}
```

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998