SERIES 8000 MICROPROCESSOR FAMILY HANDBOOK

NATIONAL SEMICONDUCTOR

1978

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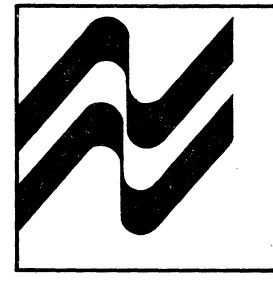

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Preface

This handbook replaces the N8080 System Design Manual. The Series 8000 Microprocessor Family encompasses not only the INS8080A, but also many peripheral control components as well. The title change reflects this increased emphasis on peripherals. This handbook provides design information pertaining to the National Semiconductor Series 8000 Microprocessor Family. The material contained in this handbook is presented at a level-of-detail sufficient for use in the design and development of microprocessor systems using the proven INS8080A CPU and support components. The material is up-to-date at the time of publication and is subject to change without notice.

Copies of this publication and other National Semiconductor publications may be obtained from the National Semiconductor sales office or distributor serving your locality.

Available data sheets are included in appendix D.
Related National Semiconductor Publications:

- National's 8080A Microprocessor Family Quick Reference
- Pace Resident Macro Assemblers Manual (for UDS - based 8080 cross assembler)
- Universal Development System Users Manual
- Universal Development System Editor Users Manual
- Universal Development System PROM Programmer Users Manual
- LLL Basic Interpreter Users Manual
- Microprocessor Family Product Guide
- National's Spectrum of IC Components for Terminals
- Microprocessor System Design Training
- Microprocessor Applications in Business, Science and Industry

Data Sheet Index

The Series 8000 Microprocessor Family Data Sheets available at time of publication are listed below and included in appendix D in the order shown (for memory data sheets refer to National's Memory Databook):

D.1 CPU GROUP

D.2 DIGITAL I/O COMPONENTS

D.3 PERIPHERAL CONTROL COMPONENTS

D.4 COMMUNICATIONS COMPONENTS

***NOTE:** For the following devices, contact National's Microprocessor Marketing regarding availability of devices and data sheets:

INS9298E	LLL BASIC Interpreter
INS8316	(same as MM52116) 16K bit (2K x 8) ROM
INS8332	(same as MM52132) 32K bit (4K x 8) ROM
INS8364	(same as MM52164) 64K bit (8K x 8) ROM

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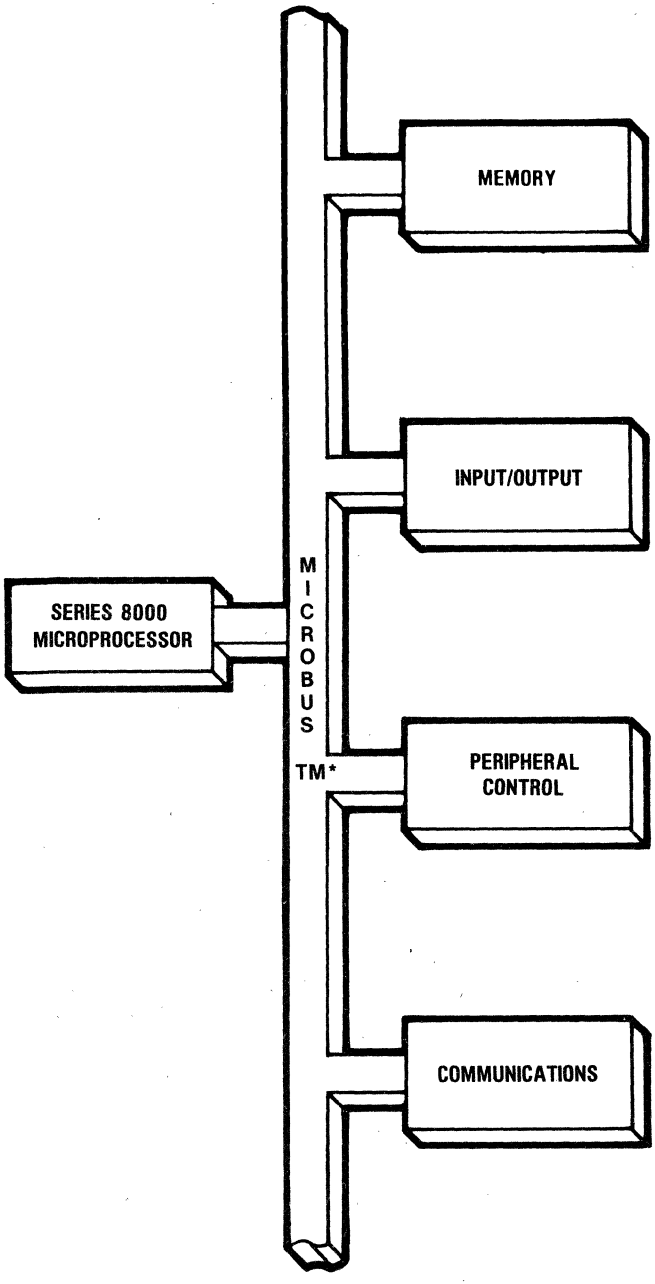

Chapter 1
Introduction

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Introduction

1.1 GENERAL DESCRIPTION

The National Semiconductor Series 8000 Microprocessor Family covers the broad general-purpose segment of microprocessor applications (see figure 1-1 for INS8080A example). Included in the Series 8000 Microprocessor Family are the proven INS8080A CPU and components of proprietary designs as well as a wide range of multiple source devices. The Series 8000 microprocessor family finds use in 8-bit microprocessor system designs ranging from complex controls to highly sophisticated communications applications. Some of the user benefits are listed below:

- Family approach to system design
- Complete CPU group
- Programmable input/output concepts
- Multiple source availability
- Complete line of support components
- Total product support

Most components of the Series 8000 Microprocessor Family are shown in figure 1-2. (For a more nearly complete list, see chapter 10 references and specific publications such as National's Memory Databook). Components are discussed by type (see 1.2). Representative of the type of CPU that can be used with the Series 8000 Microprocessor Family is the INS8080A, an 8-bit CPU chip that may be used interchangeably with the Intel 8080A. The Series 8000 Microprocessor Family can be used in systems that range from a few family components to designs that utilize the extensive capabilities available. The INS8080A falls between the cost-effective 8-bit INS8060 chip and the highly versatile 16-bit INS8900 chip in National Semiconductor's microprocessor spectrum. Any of these three microprocessors can be used with Series 8000 peripheral components.

The designer can satisfy memory requirements

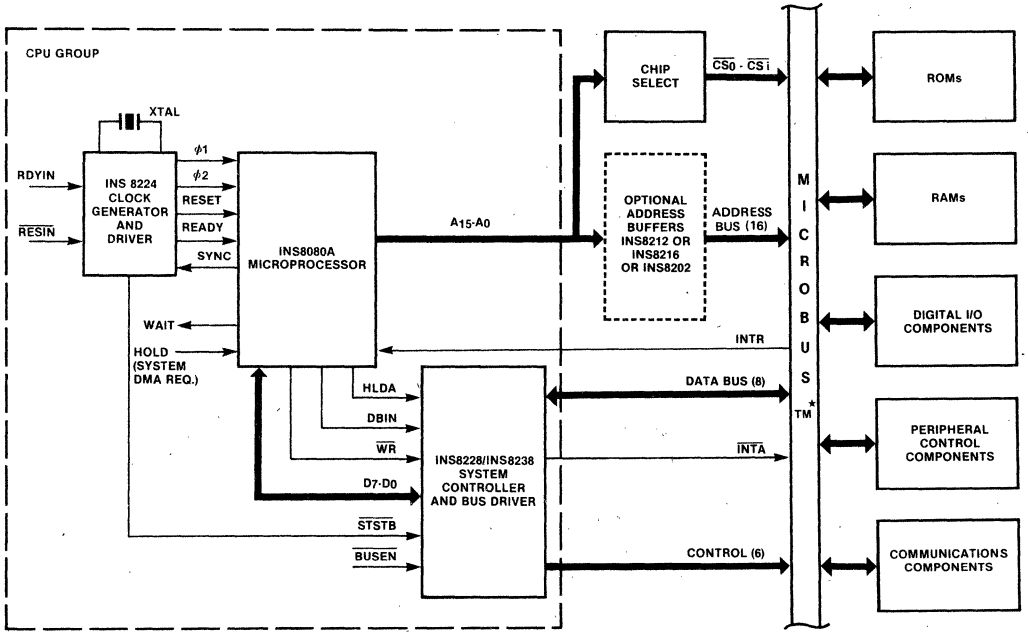
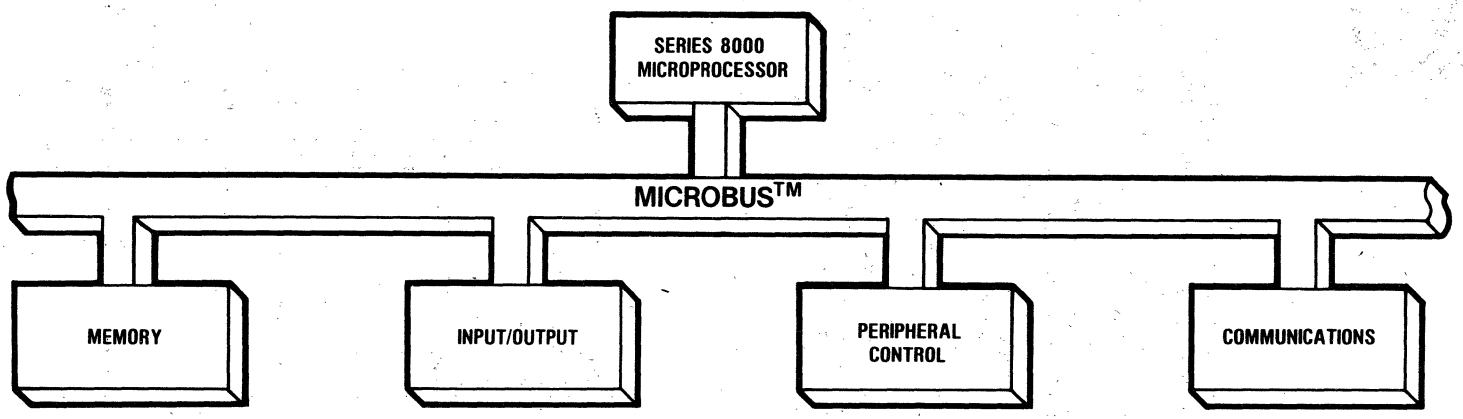


Figure 1-1. National Semiconductor Series 8000 Microprocessor Family Basic System Model (Example using INS8080A CPU Group)



PART NUMBER	DESCRIPTION
INS8101A-4	256 x 4 Static RAM with Separate I/O
INS8102A	1024 x 1 Static RAM
INS8111A-4	256 x 4 Static RAM with Common I/O
INS8154	128 x 8 Static RAM with Common I/O
INS8298E	8080A LLL Basic Interpreter
INS8316A/E	2048 x 8 MOS Mask ROM (2708 Compatible)
INS8332E	4096 x 8 MOS ROM (2708 Compatible)
INS8364/ 8364E	8192 x 8 MOS Mask ROM (E has 2708 Compatibility)
INS8704	512 x 8 EPROM
INS8708A	1024 x 8 EPROM
MM1702A	256 x 8 EPROM
MM2114	1024 x 4 Static RAM
MM5204	512 x 8 EPROM
MM5242	1024 x 8 ROM
MM5257	4K x 1 Static RAM
MM5281	4096 x 1 Dynamic RAM
MM5290	16K Dynamic RAM

PART NUMBER	DESCRIPTION
INS8202	Tri State 8 Bit Bus Driver
INS8203	Tri State 8 Bit Bus Driver (Inverting)
INS82LS05	1 of 8 Binary Decoder
INS8208B	8 Bit Bidirectional Bus Driver
INS8212	8 Bit I/O Port
INS8216	4 Bit Bidirectional Bus Driver
INS8226	4 Bit Bidirectional Bus Driver (Inverting)
INS8253	Programmable Timer
INS8255	Programmable Peripheral Interface
INS8257	Programmable DMA Controller
INS8259	Programmable Interrupt Controller

PART NUMBER	DESCRIPTION
DP8350	Series Programmable CRT Controller
INS1771-1	Floppy Disk Controller
INS1791	Dual Density Floppy Disk Controller
INS8244	90 Key Keyboard Encoder
INS8245	16 Key Keyboard Encoder
INS8246	20 Key Keyboard Encoder
INS8247	4 Digit Display Controller
INS8248	6 Digit Display Controller
INS8254	Programmable 16 Bit Addressable Peripheral Interface
INS8277	Programmable CRT Controller
INS8285	Character Generator
INS8292	8 Bit A/D Converter with 16 Channel Analog MUX
INS8294	3¾ Digit DVM with Multiplexed BCD Output

PART NUMBER	DESCRIPTION
INS1671	ASTRO Communications Interface
INS8250	Asynchronous Communications Element (ACE)
INS8251	Programmable Communications Interface

Figure 1-2. Series 8000 Microprocessor Family

from the wide range of National Semiconductor's RAM, ROM, PROM, and MAXI-ROM™* components. Programmable input/output and peripheral functions enable the system designer to configure and adapt interface lines to his own requirements. Data communications may be accomplished by using a variety of Series 8000 Communications Peripherals.

The Series 8000 Microprocessor Family is supported by industry standard design kits, easy-to-use development systems, and a full complement of cross and resident assemblers. Various components and software also are available to support the Series 8000 Microprocessor family from experimentation to final production (see chapter 10, Development Support).

1.2 HANDBOOK ORGANIZATION

The major portions of the Series 8000 Microprocessor Family Handbook are as follows:

- Introduction
- The MICROBUS
- The Series 8000 Microprocessor Family CPU Group
- Designing Series 8000 Microprocessor Family Systems
- Memory Components
- MAXI-ROMs
- Input/Output Components
- Peripheral Control Components
- Communications Components
- Development Support
- Programming
- Appendices

The handbook takes the approach of introducing the system concept of the MICROBUS first, since this is the System Bus used to interconnect the various Component Device Groups.An example of a CPU group is discussed next to form a base for discussing the various sizes of systems that follow. With this base of information, the chapter on designing Series 8000 Microprocessor Family Systems is presented next followed by detailed discussion of other device types, so that the designer can pick the chapters of interest that follow and skip the rest. Chapters 5 and 6 discuss memory components including MAXI-ROMs, and their use in storing large programs in ROM. Having covered the various memory options, it is possible to examine how Input/Output is included in the system. This is treated in two chapters (7 and 8) so that individual Input/Output Components can be selected more easily.

The communications components allow data transfer to remote locations, and are covered in chapter 9. We next turn our attention to Development Support, covering how the designer is aided, and then programming. Appendices are included next which give reference data such as MICROBUS specifications, additional sources of information and complete the manual with the available Data Sheets for the devices referenced.

1.2.1. Introduction

Chapter 1, Introduction, gives a general view of the Series 8000 Microprocessor Family and discusses the plan of the Handbook. It identifies the key concepts that are used throughout the Handbook such as the MICROBUS, and discusses the relationship of the various chapters to each other.

1.2.2 The MICROBUS

The MICROBUS chapter describes the use of the system bus and its conventions. The bus concept is developed, indicating bus usage for various size systems, recognizing that most systems will not need the entire MICROBUS capability.

1.2.3 The Series 8000 Microprocessor Family CPU Group

The discussion of the CPU Group includes as an example, the INS8080A Microprocessor, the INS8224 Clock Generator and Driver and the INS8228/INS8238 System Controller and Bus Driver. The architecture of the INS8080A is discussed along with the operating cycle, data and instruction representation. Other key topics such as addressing capabilities, Input/Output operation and control, and interrupts are examined in this chapter and then referenced in following chapters. In particular the next chapter on Designing Series 8000 Microprocessor Family Systems relies heavily on an understanding of the CPU Group as discussed in this chapter.

1.2.4 Designing Series 8000 Microprocessor Family Systems

The handbook is organized so that a designer might start with this chapter and refer to each of the other chapters as needed, while considering the design requirements of the system being designed for a particular application. For example, a particular system might need powerful input/output capability and therefore chapters 7 and 8 might be reviewed while considering approaches for the design of a system with that capability.

1.2.5 Memory Components

The diversity of Memory options range from small RAM to the mask programmable MAXI-ROM.

1.2.6 MAXI-ROMs

Mask programmable MAXI-ROMs may contain complete programs. As an example of the possibilities, the 8298 LLL (Lawrence Livermore Laboratory) BASIC interpreter for the INS8080A is discussed. This program resides in an INS-8298E, (65,536 bit) static mask-programmable ROM.

1.2.7 Input/Output Components

These devices receive a somewhat lighter discussion than the Peripheral Control Components because of their simplicity. The devices of a more complex nature (i.e. Peripheral Control Components), are given a more extensive treatment to make it easier for a designer to feel comfortable in designing with the devices. It is assumed that the designer has considerable background in the use of similar I/O devices and other Component Groups of concern in his design. The next two chapters are companions to this one and are intended to be used with it.

1.2.8 Peripheral Control Components

The discussion of these devices is somewhat grouped because of their typical use together, although no rigid division is implied by chapter divisions or order of discussion of devices. The statement that the only limitation is the imagination of the designer applies perhaps stronger with the I/O, than any other area of design, for here is the interface capability to other devices, equipment, and systems in the outside world. The treatment in the two Input/Output chapters (7 and 8) and the communications chapter (9), is intended to get the imagination going, and emphasize the range of devices available, rather than give cook book solutions to particular problems. (See appendix C for additional information sources.)

1.2.9 Communication Components

Various communications devices are covered in this chapter.

1.2.10 Development Support

This chapter identifies items of general support, such as the 8080 cross assembler, PROM Programmer and the Universal Development System (UDS), training and technical support. (Also see appendix C for additional information sources.)

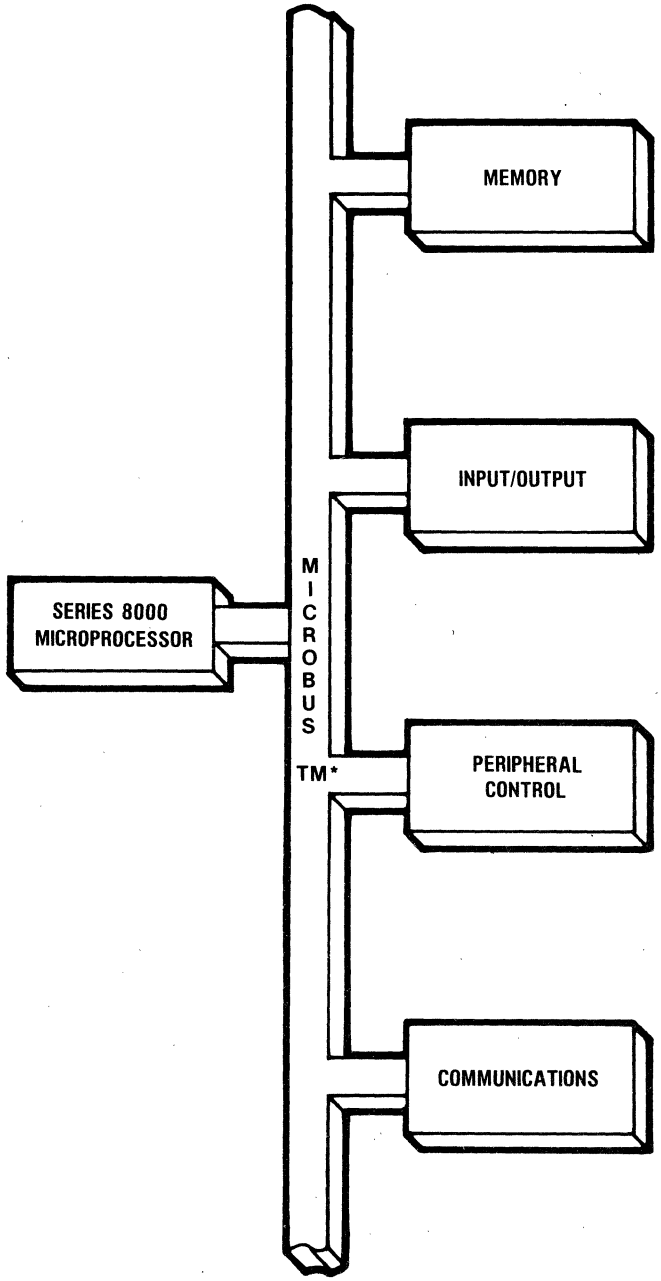
1.2.11 Programming

In this chapter, programming topics are covered from machine language through high level languages. Reference is also made to related programmable devices, such as Programmable Peripheral Control Components.

1.2.12 Appendices

In addition to general reference data, additional information sources are identified in appendix C.

Available data sheets for the referenced devices are grouped in Appendix D. Notice that they are grouped by area of concern (i.e., CPU group, Memory components, Digital I/O Components, Peripheral Control Components, and Communication Components).



Chapter 2
MICROBUS™

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2.1 INTRODUCTION

MICROBUS, the National Semiconductor Standard for Microprocessor Interfaces, deals with systems that use 8-bit parallel means to transfer digital data between MOS/LSI microprocessor CPUs and interfacing devices. The interface system described herein allows proximate components to communicate over a unified bus system.

This standard applies to relatively small systems representative of users' end products. Typically, these are systems where fewer than ten integrated circuits are interconnected to a common system bus, with buffering kept to a minimum.

Application of this standard will provide the user with a broad line of support devices which can be effectively "plugged" into systems without regard to complex timing or electrical analysis, thereby making interfacing easy for the system designer.

2.2 GENERAL DESCRIPTION

This standard applies to interface systems used to interconnect electronic devices with MOS/LSI microprocessor systems. Devices should have the following characteristics:

- Data exchanged among the interconnecting devices is digital (as distinct from analog).
- Total transmission path among interconnecting devices is electrically short. That is, transmission line considerations are negligible.
- Number of devices interconnected on the system bus is small (ten or fewer).

This standard defines the most general system. The large majority of interfacing devices employ only a subset of the signals. Signal Lines are described in table 2-1. For details contact National Semiconductor.

2.2.1 Basic MICROBUS Interface

The following paragraphs define the Basic MICROBUS Interface Signals. Figures 2-1 and 2-2 illustrate the fundamental read and write cycle timing.

The Basic MICROBUS Interface defines generalized read and write strobes - $\overline{RD}$ and $\overline{WR}$. In actual systems there may be both memory strobes and peripheral device (I/O) strobes. Because it is actually the option of the system designer whether he implements both sets of strobes, only the generalized strobes are discussed in detail. The mnemonics to be used for the memory strobes are $\overline{MEMR}$ and $\overline{MEMW}$. The mnemonics for peripheral strobes are $\overline{I/OR}$ and $\overline{I/OW}$. (Refer to Section 4.3 for discussion of mapping peripherals in memory vs. I/O addressing space.)

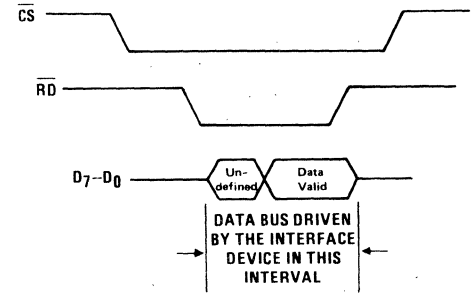


Figure 2-1. Read Cycle - Fundamental Timing Relationships

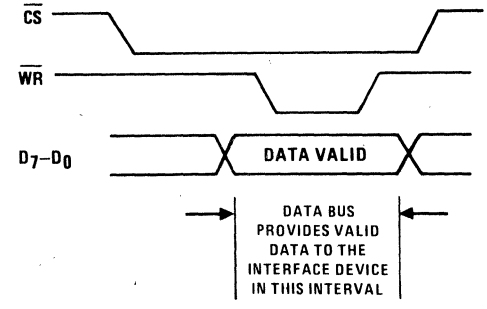


Figure 2-2. Write Cycle - Fundamental Timing Relationships

2.2.1.1 Data Bus (D_7-D_0)

These signal lines carry bit-parallel data information, typically, implemented as eight TRI-STATE input/output lines. In such a typical application status, control and data information is transferred. In most applications, eight bits are implemented.

Table 2-1. SIGNAL LINES (Referenced to the Interface Device)

FUNCTION	MNEMONIC	NUMBER	TYPE
Data	D_7-D_0	8	Bidirectional
Generalized Read Strobe	$\overline{RD}$	1	Input
Generalized Write Strobe	$\overline{WR}$	1	Input
Memory Read Strobe	$\overline{MEMR}$	1	Input
Memory Write Strobe	$\overline{MEMW}$	1	Input
I/O Read Strobe	$\overline{I/OR}$	1	Input
I/O Write Strobe	$\overline{I/OW}$	1	Input
Device (Chip) Select	$\overline{CS}$	1	Input
Reset	$\overline{RESET}$	1	Input
Ground	GND	1	Power Supply
Address	A_{15}-A_0	16	Input
Interrupt	INTR	—	Output
DMA Request	DRQ	—	Output
DMA Acknowledge	$\overline{DACK}$	—	Input
Terminal Count	TC	1	Input
Ready	READY	1	O.C. Output
Early Write Strobe	$\overline{EWR}$	1	Input
Data Buffer Enable	$\overline{DBE}$	1	Output
Data Buffer Out	DBO	1	Output
Address Buffer Enable	$\overline{ABE}$	1	Output
Address Buffer Out	ABO	1	Output

In simpler, dedicated, interface applications, these signal lines may be unidirectional. Examples are, simple interface latches, keyboard controllers, and display controllers.

2.2.1.2 Chip Select ($\overline{CS}$)

This input pin enables communication between the interface device and the system. This signal is a combinational active low state indicator that the device is being addressed by the system. The user/designer must accommodate transients on this signal during changes in the address bus. Therefore, this signal should be used as a combinational enable function, i.e., level sensitive applications are O.K., edge sensitive are not.

In a data transfer, the $\overline{CS}$ signal will envelope the $\overline{RD}$ or $\overline{WR}$ signals.

2.2.1.3 Read Strobe ($\overline{RD}$)

A low state on this input pin enables the interface device to send information to the system via the data bus. This signal is the indicator to the interface device to provide data to the MICROBUS whenever $\overline{CS}$ is also active (low). Otherwise, the interface device data bus drivers should be in the high impedance state.

2.2.1.4 Write Strobe ($\overline{WR}$)

A low on this input signal in combination with a low on the $\overline{CS}$ input signal enables the transfer of information from the MICROBUS to the interface device.

The data bus (D_7-D_0) will be valid to the interface device before the high to low transition of $\overline{WR}$ and will remain valid until after the low to high transition of $\overline{WR}$.

Designers of new interface devices should not rely upon data being valid on the leading edge of the write strobe because some existing and future microprocessors do not provide data valid at this time.

2.2.1.5 Reset ($\overline{RESET}$)

The $\overline{RESET}$ signal is supplied by the system to all interfacing devices at power on time and typically by a manual (pushbutton) operation. Devices are to be reset whenever the $\overline{RESET}$ signal is in the low voltage state.

The reset signal should place all interfacing devices into a known initial state. It is desirable that every sequential storage element within an interface device be initialized by this signal. For example, when a floppy disk interface device is reset, it should restore the head to track zero. A mag tape device, however, should terminate tape movement operations. Each electromechanical device must be considered separately when determining what effect the $\overline{RESET}$ input will have on its controlling states.

Whenever the $\overline{RESET}$ signal is applied, the interface device shall place its data bus and other TRI-STATE system outputs into the high impedance state. The device designer may assume that the $\overline{RESET}$ input will be low for a minimum of 100 μsec.

Many MOS/LSI interface devices require an active high voltage RESET signal while most existing TTL devices use $\overline{RESET}$. For this reason, most systems will require both RESET and $\overline{RESET}$. Either reset signal is acceptable for this standard. Future interface devices should standardize on the $\overline{RESET}$ convention.

2.2.1.6 Ground (GND)

This signal provides 0v reference to the interface device. All signals and voltages are referenced to GND.

2.2.2 Addressing Techniques

The first extension of complexity beyond the Basic MICROBUS is the addition of addressing capability. The addition of address signals to the interface device provides a binary encoded selection of device internal registers or memory locations.

2.2.2.1 Input Case

These input signals, in conjunction with the $\overline{CS}$ and $\overline{RD}$ or $\overline{WR}$ inputs, control the selection of data, control, or status information transfer between the MICROBUS and the interfacing device.

A common example is the 8255 Programmable Peripheral Interface. This device has two address inputs (A_1 and A_0). Internal to the device, there are three data ports - A, B, and C; a status register; and a control register. The A, B, and C data ports may be read or written and are specified by the address inputs during the time $\overline{RD}$ or $\overline{WR}$ is low. In this case, port A, B, or C is specified when the A_1A_0 inputs are 00, 01, or 10 respectively. When the address inputs are 11 and a read operation is performed, the 8255 provides information from its status register to the data bus. When the address inputs are 11 and a write is performed, the 8255 command register is loaded from the data bus.

In this example, a write only and a read only register share a common address. This is not a preferred practice as it adds complexity to the controlling software. Data written to write only control or data registers must often be duplicated in RAM when independent bit operations are to be performed on the register.

2.2.2.2 Address/Chip Select Relationship

It is implied that the chip select signal, $\overline{CS}$ (2.2.2) is a combinational function of the system address bus. Because of this relationship, transitions of $\overline{CS}$ are delayed from changes in the address bus. The timing specifications for the $\overline{CS}$ signal are derived from the typical implementation presented in appendix B.

2.2.2.3 Bidirectional Addresses

In the future, interface devices will provide their own address information during direct memory access (DMA) transfers. In this class of interface device the address lines are outputs during DMA transfers and inputs during conventional, programmed I/O transfers as described in section 4.3. Special control signals are required to control external TRI-STATE address buffers and latches needed for this type of device. These signals control the direction of data through the TRI-STATE buffer and the TRI-STATE enable. They are named Address Buffer Out (ABO) and Address Buffer Enable ($\overline{ABE}$) respectively.

2.2.3 Interrupt Convention

Interface devices often provide interrupts to the system to request the initiation or indicate the completion of a task.

In the standard bus environment, interface devices may provide one or more interrupt signals. In the singular case, this signal is named INTR. It is an active high signal that is asserted in the high voltage state to request a Program interruption.

Once asserted high by the interface device, the interrupt signal must remain high until it is serviced by the system. Typically, interrupts may be serviced by the system taking action to either identify or service the condition which caused the interrupt. In all cases, this must be implemented by a programmed I/O transfer between the system and the device. The particular protocol for removal of the interrupt is dependent upon the type of device producing it.

The interrupt signal may be asserted asynchronously with respect to other signals in the system. See figure 2-3. It must be removed by the completion of the appropriate $\overline{RD}$ or $\overline{WR}$ strobe when the $\overline{CS}$ and address inputs are active.

An example of implementation is an A/D converter designed to interface to the MICROBUS. The device designer who wishes to make his A/D converter compatible with the MICROBUS will modify the classical control and timing logic to replace the END OF CONVERSION signal with an interrupt output (INTR). The START CONVERSION input is replaced or supplemented by a programmed I/O operation.

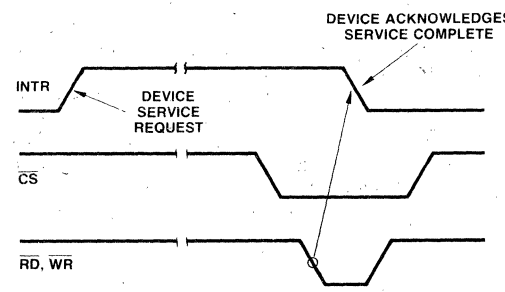


Figure 2-3. Interrupt Service - Interface Device Waveforms

In the simplest case, the INTR output is set high at END OF CONVERSION. The system responds to the interrupt by reading the A/D output buffer which sets the INTR low and simultaneously starts a new conversion. The reader will notice that the START CONVERSION input is not required. In practice it is desirable to implement control and status registers to allow the system to select how the interrupt and start conversion systems will function.

In an 8080 system, the interrupt feature may be implemented by adding an 8259. The interrupt controller is added to the CPU group to provide the MICROBUS interrupt inputs for interfacing devices.

2.2.4 Direct Memory Access (DMA) Transfers

Systems that provide DMA capability interface to devices via two dedicated and one common signal. Each DMA device controls its own DMA request signal (DRQ). The system responds to DRQ with a dedicated DMA acknowledge signal ($\overline{DACK}$). The third special signal for DMA is the terminal count (TC) indicator provided by the system to the device to indicate that the present DMA cycle should be the last cycle for this data block.

Figure 2-4 illustrates a typical DMA cycle in which the device is providing data to the system. In this type of DMA channel, a simultaneous read peripheral ($\overline{I/OR}$) and write memory operation ($\overline{MEMR}$) is performed.

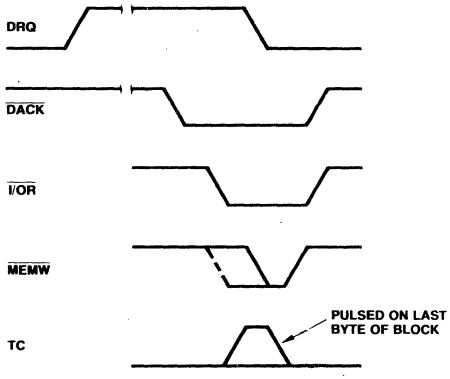


Figure 2-4. Single Cycle DMA Transfer from an Interface Device to Memory.

The interface device designer should consider the DACK signal to be equivalent to a special chip select signal with equivalent timing relationships to the read and write strobes and TRI-STATE enables of the MICROBUS.

Refer to manufacturer's literature for the standard 8257 DMA Controller for further detailed discussion of the various modes and relationships possible for DMA interface devices.

In an 8080 system, DMA capability may be implemented by adding an 8257 DMA controller and an 8212-8-Bit I/O Latch to the basic system model.

From a device designer's viewpoint, this addition may be implied as part of the MICROBUS.

2.2.5 Ready Signal

The READY signal is used to extend the period of a RD or WR strobe. It is a system input that may be driven by any number of interfacing devices. Interfacing devices that cannot otherwise meet the access time requirements of the system should provide a READY output to the system. This output should not have an active or passive connection to V_{CC}(+5V). It should be open-collector (open drain if n-channel). The system will provide a common resistive pull-up device for the READY signal.

Typically, use of the READY signal requires complex electrical design and timing analysis.

Figure 2-5 illustrates timing relationships for the READY signal. In this example, the system initiates a read or write cycle to the device by activating its RD or WR and CS inputs. If the interface device cannot respond within the system access time requirements, it may assert the READY signal low indefinitely until it has had time to stabilize the data bus in a read operation or accept the data in a write operation.

The device designer is cautioned to use the READY feature only for access time extension and not for synchronization because it may severely impact system throughout.

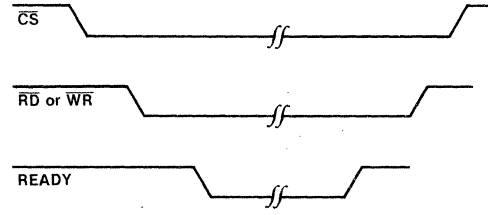


Figure 2-5. Relationship of READY to CS, WR, and RD.

2.2.6 The Basic Interface Model

The specific implementation and model for the Basic MICROBUS Interface (Class 1) is the combination of the INS8080A CPU, 8224 Clock Generator, 8228 System Bus Controller, and Chip Select Logic. This system model is depicted in Figure 2-7. The expanded CPU Group is shown in Figure 2-8. Note the use of the INS8259 at the bottom of the figure to expand interrupts. See section 4.7 for expansion using INS8259.

Class 1 devices will also interface directly with the INS8060 (SC/MP II) microprocessor system model depicted in Figure 2-9. INS8070 system model is shown in Figure 2-10.

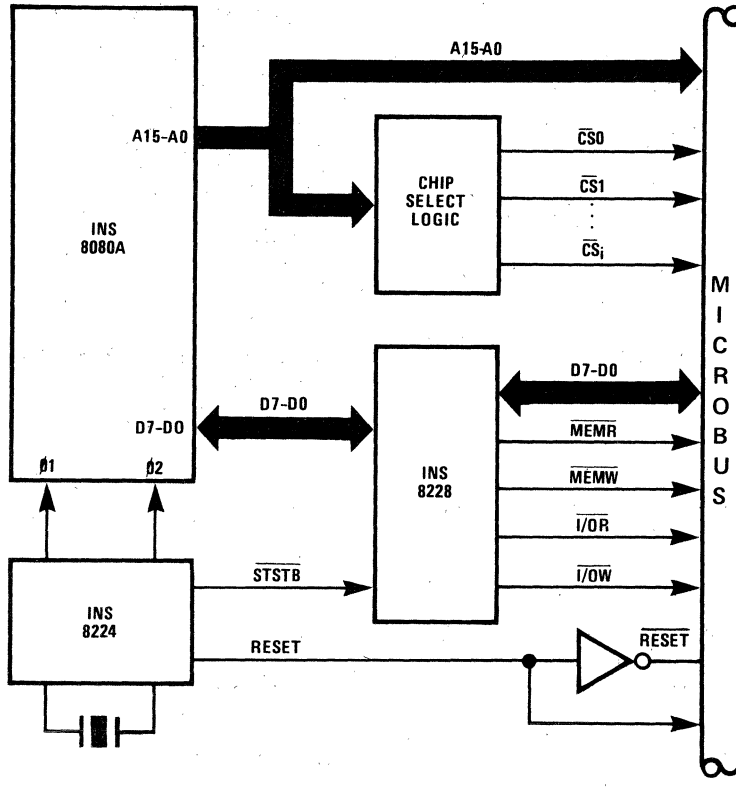


Figure 2-6. INS8080A System Model for the Basic MICROBUS Interface

For purposes of clarification:

- Class 0 devices are those which may require special conditioning of their interface to successfully function with microprocessor systems.
- Class 1 devices perform with the following microprocessor CPUs when other bus loading is within the D.C. and capacitive load limits: INS8060, INS8070, INS8080A.
- Class 2 devices are tailored for next-generation microprocessors. The specification will be available in the future.

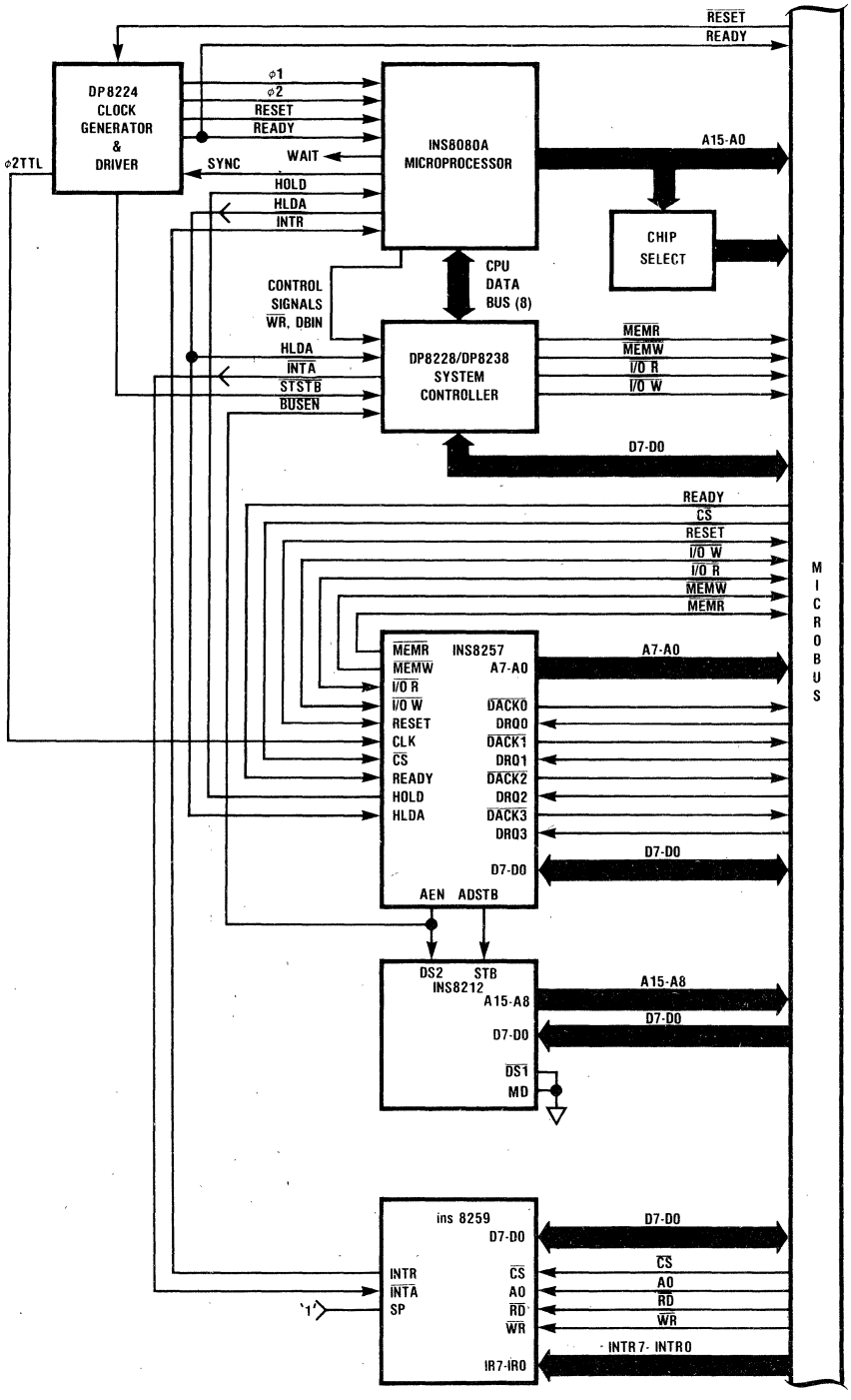


Figure 2-7. INS8080 Family CPU Group to MICROBUS Configuration

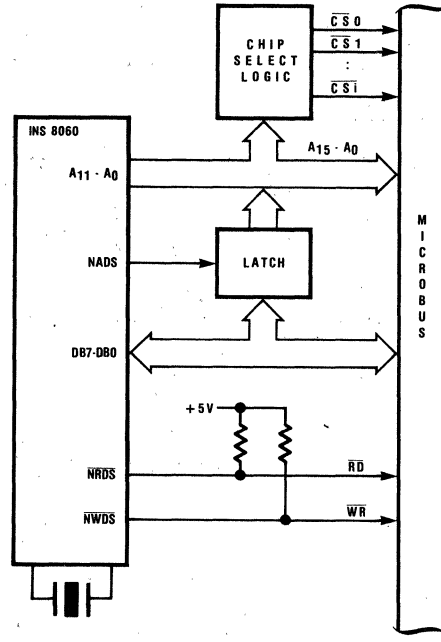


Figure 2-8. INS8060 System Model

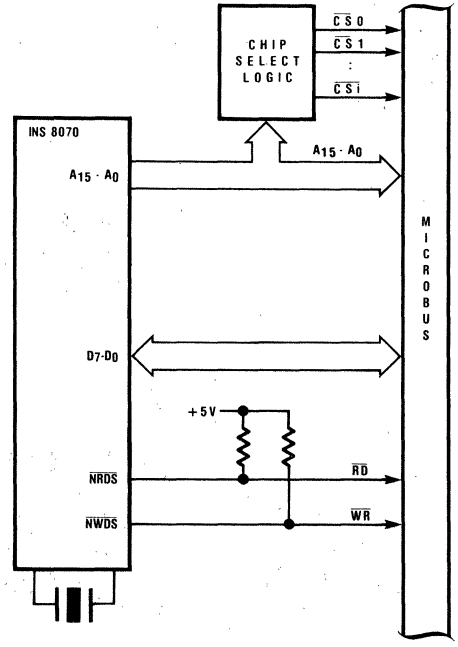
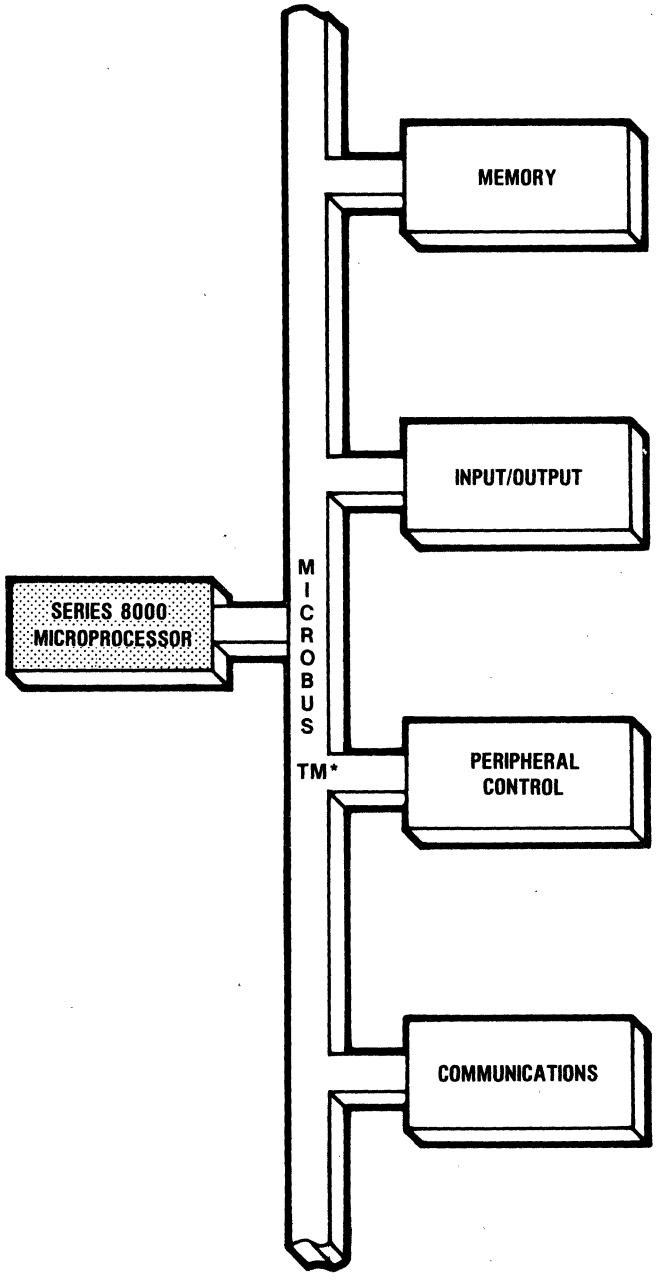


Figure 2-9. INS8070 Family System Model



Chapter 3
The Series 8000 Microprocessor Family CPU Group

INS 8080A
MICROPROCESSOR FAMILY

Part Number/Description

INS8080A
8 Bit CPU (2μs)
INS8080A-1
8 Bit CPU (1.3μs)
INS8080A-2
8 Bit CPU (1.5μs)
INS8080ADI
8 Bit CPU (2μs)
−40°C to +85°C
INS8080ADI/883
8 Bit CPU (2μs)
−40°C to +85°C/883B
INS8224
Clock Generator & Driver
INS8228
System Controller & Bus Driver
INS8238
System Controller & Bus Driver
(Advanced Timing)
INS8257
Programmable DMA Controller
INS8259
Programmable Interrupt Controller

* Trademark, National Semiconductor Corporation

The Series 8000 Microprocessor Family CPU Group

3.1 INTRODUCTION

This chapter provides detailed information on the Series 8000 Microprocessor family of support chips that comprise the INS8080A CPU Group. The information within this chapter is intended to assist the Series 8000 designer by providing both descriptions of the operating characteristics of the devices and typical interconnection diagrams. Detailed parametric information on each of the CPU Group devices is contained in appendix D, Device Data Sheets.

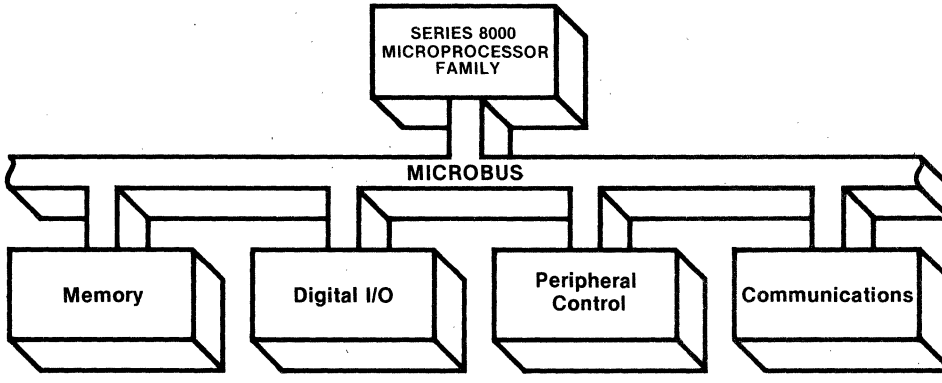
National Semiconductor offers the broadest line of microprocessors of any semiconductor manufacturer in the world. National has expanded its microprocessor base so any microprocessor application can be designed and produced using its products. From the simplest electronic toy or control mechanism to large control arrays, point-of-sale systems, and large data-processing systems, National can supply your needs. Some of the features and benefits of dealing with National follow.

- Micro-Plus - testing, special reliability and quality program
- Full development system support - all the way from the high-powered PACE development system (with numerous software packages and a DOS) to low-cost development systems (for PACE and SC/MP) to do-it-yourself PACE and SC/MP kits

National Semiconductor also offers the most extensive line of CPU-to-peripheral support products - for digital input/output, communications, peripheral control, and memory. And National Semiconductor is expanding the support lines, so you can expect to see even more!

National's INS8080A Family

Positioned between the cost-effective INS8060 and the highly versatile 16-bit INS8900, National's INS8080A can be used in systems which range from a few family components to designs which utilize its full capabilities. National offers the broadest line of peripheral circuits and memories to complement the basic INS8080A CPU. National's INS8080A features and benefits:



- Cost effectiveness - because of our variety, our microprocessors afford designs that can be tailored to a multitude of applications
- Broad product family of microprocessors and peripherals
- 16-Bit COMPUTATION microprocessors for precision control functions
- 8-Bit BYTE HANDLING microprocessors for terminals
- 4/8-Bit LOW-COST CONTROL microprocessors for industrial controllers
- Second sourced families
- Ready availability - off-the-shelf shopping

- Family approach to system design
- Complete CPU group
- Programmable input/output concepts
- Multiple source availability
- Complete line of support components
- Total product support

National's INS8080A family is supported by industry-standard design kits, easy-to-use development systems, and a full complement of cross and resident assemblers. Various components and software also are available to support the INS8080A family from experimentation to final production.

3.2 INS8080A MICROPROCESSOR

The basic INS8080A CPU Group consists of three components:

- The INS8080A Microprocessor
- The INS8224 Clock Generator and Driver
- The INS8228 System Controller

The INS8080A is an 8-bit microprocessor housed in a standard 40-pin dual in-line package. The chip is fabricated using N-channel silicon-gate technology. The INS8080A has a 16-bit address bus capable of addressing up to 65k bytes of memory, 256 input/output devices. Data is transmitted on a separate bidirectional 8-bit TRI-STATE bus. The INS8080A directly provides signals to control the interface to memory and I/O ports. The INS8080A has:

- 74 Instructions - Variable Length
- 6 General Purpose Registers plus an accumulator
- Variable Length Stack
- Addresses 256 Input and 256 Output Ports
- Multiple Addressing Modes

The INS8080A is an 8-bit CPU chip that may be used interchangeably with the Intel 8080A. It can be used in systems that range from a few family components to designs that utilize its full capabilities.

Detailed descriptions of both the INS8080A Instruction Set and the INS8080A parametric information is contained in the INS8080A Data Sheet in appendix D.

3.2.1 Architecture of the INS8080A

Figure 3-1 illustrates CPU architecture and the pinouts of the chip. (Refer to table 3-1 for descriptions of the INS8080A chip pinouts.) The INS8080A consists of the following major functional units: (1) Register Array and Address Logic, (2) Arithmetic and Logic Unit (ALU) and Registers, (3) Instruction Register and Decoder, (4) Timing and Control, and (5) Data Bus Buffer/Latch. Each of the major functional units and its logic units are briefly discussed below.

3.2.1.1 Register Array and Address Logic

This functional section of the CPU chip comprises a static RAM Register array, and Incrementer/Decrementer, an Address Latch, and a Register-Select Multiplexer. The Register array is organized into six 16-bit registers as follows.

- A Program Counter
- A Stack Pointer
- Three register pairs (BC, DE, and HL) composed of six 8-bit general-purpose registers.
- A register pair (W and Z) composed of two 8-bit temporary registers.

The Program Counter (PC) is a special-purpose register that contains the address of the instruction being executed; the PC is incremented during each instruction fetch. The Stack Pointer (SP) is also a special-purpose register and contains the address of the next available stack location in the external read/write memory (RAM). Using the SP register, any area of the external memory may be reserved as a last-in-first-out (LIFO) external stack. The stack is used primarily for temporary storage of the contents of the PC and all general-purpose registers (including the Accumulator) during subroutine execution and Interrupt Service Routine execution. The Stack Pointer is decremented when data are "pushed" onto the stack and incremented when data are "popped" off the stack. In other words, the stack is filled from top to bottom.

General-purpose registers B, C, D, E, H, and L can be used by the programmer as either single 8-bit secondary accumulators or as 16-bit register pairs that function as data counters. The HL register pair is the primary data counter and provides the indirect memory address for most memory-reference instructions (refer to 3.2.5). The BC and DE register pairs are used as data counters for a limited number of memory-reference instructions (for example: STAX B, STAX D, LDAX B, AND LDAX D). Temporary registers W and Z, which are not under software control, are only used as a 16-bit register pair for the internal execution of instructions.

The Register-Select Multiplexer enables 8-bit data transfers between the Internal Data Bus and the Register Array. Sixteen-bit transfers occur between the Register Array and either the Address Latch or the Incrementer/Decrementer. Any of the three register pairs (BC, DE, or HL) routes its 16-bit data output to the Address Latch, which in turn drives both the 16-bit A_{15}-A_0 Address Bus (via the associated 16-bit unidirectional TRI-STATE Address Buffer) and the Incrementer/Decrementer. The data output of the Incrementer/Decrementer is routed to the Register Array. The 16-bit data may be either incremented, decremented, or merely transferred between registers.

3.2.1.2 ALU and Registers

This functional section of the CPU chip includes the Arithmetic Logic Unit (ALU), an 8-bit

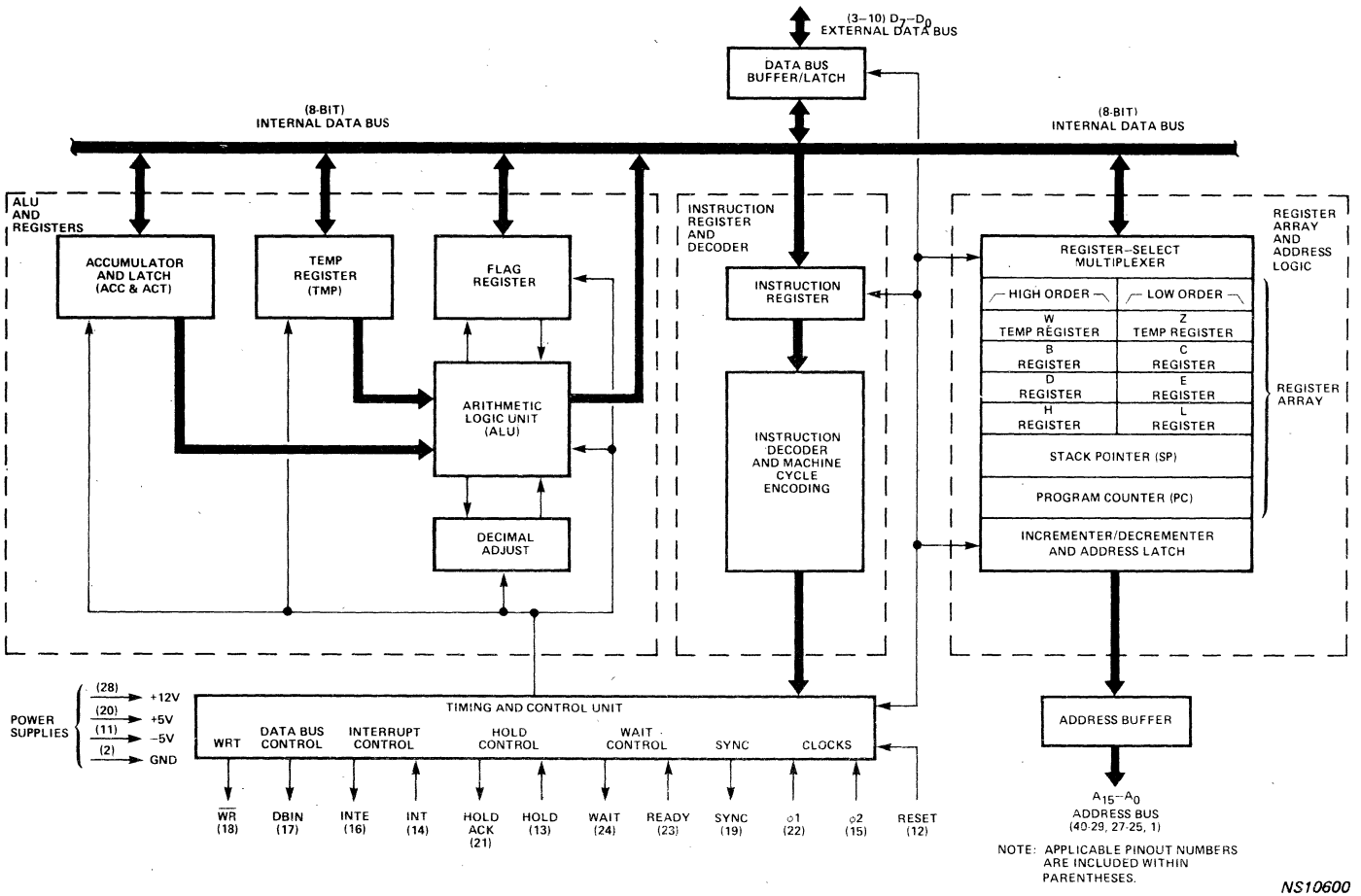


Figure 3-1. CPU Architecture and Pinouts of INS8080A

Table 3-1. Input/Output Signal Descriptions

SIGNAL MNEMONIC/ PIN DESIGNATION	FUNCTIONAL NAME	DESCRIPTION
READY (Input)	Memory or I/O Synchronization	When high (logic 1), indicates that valid memory or input data are available to the CPU on the INS8080A External Data Bus. The READY signal is used to synchronize the CPU with slower memory or input/output devices. If the INS8080A does not receive a high READY input after sending out an address to memory or an input/output device, the INS8080A enters a WAIT mode for as long as the READY input remains low (logic 0). The CPU may also be single stepped by the use of the READY signal.
HOLD (Input)	Hold or DMA Operations	When high, requests that the CPU enter the HOLD mode. When the CPU is in HOLD mode, the CPU address and data buses both are in the high-impedance state. The HOLD mode allows an external device to gain control of the INS8080A address and data buses immediately following the completion of the current machine cycle by the CPU. The CPU acknowledges the HOLD mode via the HOLD ACKNOWLEDGE (HLDA) output line. The HOLD request is recognized under the following conditions: • The CPU is in the HALT mode. • The READY signal is active and the CPU is in the T_2 or T_W state.
INT (Input)	Interrupt Request	When high, the CPU recognizes an interrupt request on this line after completing the current instruction or while in the HALT mode. An interrupt request is not honored if the CPU is in the HOLD mode (HLDA = logic 1) or the Interrupt Enable Flip-flop is reset (INTE = logic 0).
RESET (Input)	Reset	When activated (high) for a minimum of three clock periods, the content of the Program Counter is cleared and the internal Interrupt Enable and Hold Acknowledge Flip-flops are reset. Following a RESET, program execution starts at memory location 0. It should be noted that the Status Flags, Accumulator, Stack Pointer, and other registers are not cleared during the RESET sequence.
SYNC (Output)	Synchronizing Signal	When activated (high), the beginning of a new machine cycle is indicated and the status word information is outputted on the External Data Bus.
WAIT (Output)	Wait Mode	When high, acknowedges that the CPU is in the WAIT mode.
$\overline{WR}$ (Output)	Write	When low, the data on the External Data Bus are stable for WRITE memory or OUTPUT operation.

Table 3-1. Input/Output Signal Descriptions (Continued)

SIGNAL MNEMONIC/ PIN DESIGNATION	FUNCTIONAL NAME	DESCRIPTION
HLDA (Output)	Hold Acknowledge	Goes high in response to a logic 1 on the HOLD line and indicates that the data and address buses will go to the high-impedance state. The HLDA begins at one of the following times: • The T_3 state of a READ memory input operation. • The clock period following the T_3 state of a WRITE memory output operation. In both cases, the HLDA signal starts after the rising edge of the $\phi 1$ clock, and high impedance occurs after the rising edge of the $\phi 2$ clock.
INTE (Output)	Interrupt Enable	Indicates the content of the internal Interrupt Enable Flip-flop. The Enable and Disable Interrupt (EI and DI) Instructions cause the Interrupt Enable Flip-flop to be set and reset, respectively. When the flip-flop is reset (INTE = logic 0), it inhibits interrupts from being accepted by the CPU. In addition, the internal interrupt Enable Flip-flop is automatically reset (thereby disabling further interrupts) at the T_1 state of the instruction fetch cycle, when an interrupt is accepted; it is also reset by the RESET Signal.
DBIN (Output)	Data Bus In	When high, indicates to external circuits that the External Data Bus is in the input mode. The DBIN Signal should be used to gate data from memory or an input/output device onto the External Data Bus.
A_{15}-A_0 (Output)	Address Bus	This bus comprises 16 TRI-STATE® output lines. The bus provides the address to memory (up to 65k bytes) or denotes the input/output device number for up to 256 input and 256 output peripherals.
D_7-D_0 (Input/Output)	Data Bus	This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communication between the CPU, memory, and input/output devices for instructions and data transfers. A status word (which describes the current machine cycle) is also outputted on the External Data Bus during the first state of each machine cycle (SYNC = logic 1).
$\phi 1$ and $\phi 2$ (Inputs)	Clock Inputs	Two non-TTL compatible clock phases that provide nonoverlapping timing references for internal storage elements and logic circuits of the CPU.
+12V (Input)		V_{DD} Supply
+5V (Input)		V_{CC} Supply
-5V (Input)		V_{BB} Supply
GND	Ground	V_{SS} (0 volt) reference

Accumulator (ACC), an 8-bit Temporary Accumulator (ACT), a 5-bit Flag Register, and an 8-bit Temporary Register (TMP). The ALU performs arithmetic, logical, and rotate operations. It is fed by the ACC, the ACT, and the Carry Flip-flop of the 5-bit Flag Register. The results of the ALU operation are transferred to either the Internal Data Bus or the Accumulator. In addition, the ALU feeds the Flag Register. This register contains flip-flops which provide storage for the five condition flags (Zero, Carry, Sign, Parity, and Auxiliary Carry) associated with the execution of instructions in the INS8080A. The Carry Flag may be set or complemented by execution of the Set Carry or the Complement Carry Instruction (refer to 8080 Data Sheet), respectively. The 8-bit Temporary Register is loaded via the Internal Data Bus and routes all or portions of its data to the ALU, the Flag Register, and/or the Internal Data Bus. The Accumulator serves as a link between the external memory and all other software-controlled registers. The Accumulator is used in performing arithmetic and logic operations and for storing the results of these operations. Immediate instructions, data transfers, shifts, and rotates also use the Accumulator. The Accumulator receives data from the ALU and the Internal Data Bus and routes data to the Temporary Accumulator and the Internal Data Bus. During the execution of the Decimal Adjust Accumulator Instruction, the contents of the Accumulator and the Auxiliary Carry Flip-flop may be tested for decimal correction (utilizing the Decimal Adjust logic).

3.2.1.3 Instruction Register and Decoder

This functional section includes an 8-bit Instruction Register and an Instruction Decoder. The Instruction Register stores byte 1 of the instruction during the execution cycle. This byte, which contains the operation code, is transferred to the Instruction Register via the Internal Data Bus. The succeeding Instruction Decoder and control logic circuits then generate the required signals to control the internal data transfers and the timing of the new instruction, which may require from one to five machine cycles for execution (refer to 3.2.2.1).

3.2.1.4 Timing and Control Unit

The Timing and Control Unit generates the state and cycle timing signals, and maintains the proper sequences of events required for any processing task. Two nonoverlapping external clock inputs ($\phi 1$ and $\phi 2$) are accepted by the Timing and Control circuits to furnish the timing references for all microprocessor actions. In addition, the output of the Instruction Decoder is combined with various timing signals and external control inputs at the Timing and Control circuits to provide the control and gating signals required by other functional units (both internal and external to the CPU) for execution of the specified operation.

3.2.1.5 Data Bus Buffer/Latch

This major functional unit includes an 8-bit Data Buffer and an 8-bit Latch. The 8-bit Data Buffer is a bidirectional TRI-STATE interface that provides isolation between the Internal Data Bus and the D_7-D_0 External Data Bus. In the output mode, data or internal status information on the Internal Data Bus initially is loaded into the 8-bit Latch. The outputs of the Latch are then transferred to the External Data Bus via the output Data Bus Buffer, which is in the high-impedance state during input or nontransfer operations. In the input mode, external data are transfered to the Internal Data Bus via the input Data Bus Buffer, which is in the high-impedance state during output or nontransfer (DMA) operations. With the exception of the T3 state of a machine cycle (refer to 3.2.2.1), the Internal Data Bus is precharged at the start of each internal state.

3.2.2 Operating Cycle

3.2.2.1 Instruction Cycle and Related Timing

An instruction cycle of the INS8080A consists of fetching an instruction from the program stored in external memory and executing the operation specified by the instruction. The fetch routine first causes the instruction address to be transferred from the Program Counter to the Address Bus via the output Address Latch. Next, an input data transfer (fetch from memory) is initiated. When the selected instruction (which may be one, two, or three bytes in length) is subsequently placed on the External Data Bus, the operation code byte is loaded into Instruction Register. If the instruction consists of more than one byte, additional states are required to fetch each byte of the instruction. In this case, the subsequent bytes are placed in temporary storage registers.

After the complete instruction is present in the INS8080A, the Program Counter is incremented and the instruction is then executed in the remaining states of the instruction cycle. The instruction may call for a memory-read, a memory-write, or an internal CPU operation such as a register-to-register transfer or an add-registers operation.

The basic instruction cycle (see figure 3-2) contains from one to five machine cycles, which are referred to as M1, M2, M3, M4, and M5. Each machine cycle, in turn, contains from three to five states, which are referred to as T1, T2, T3, T4, and T5. The duration of a T state is determined by the interval between two successive positive-going transitions of the $\phi 1$ clock pulse. Depending on the type of instruction being ex-

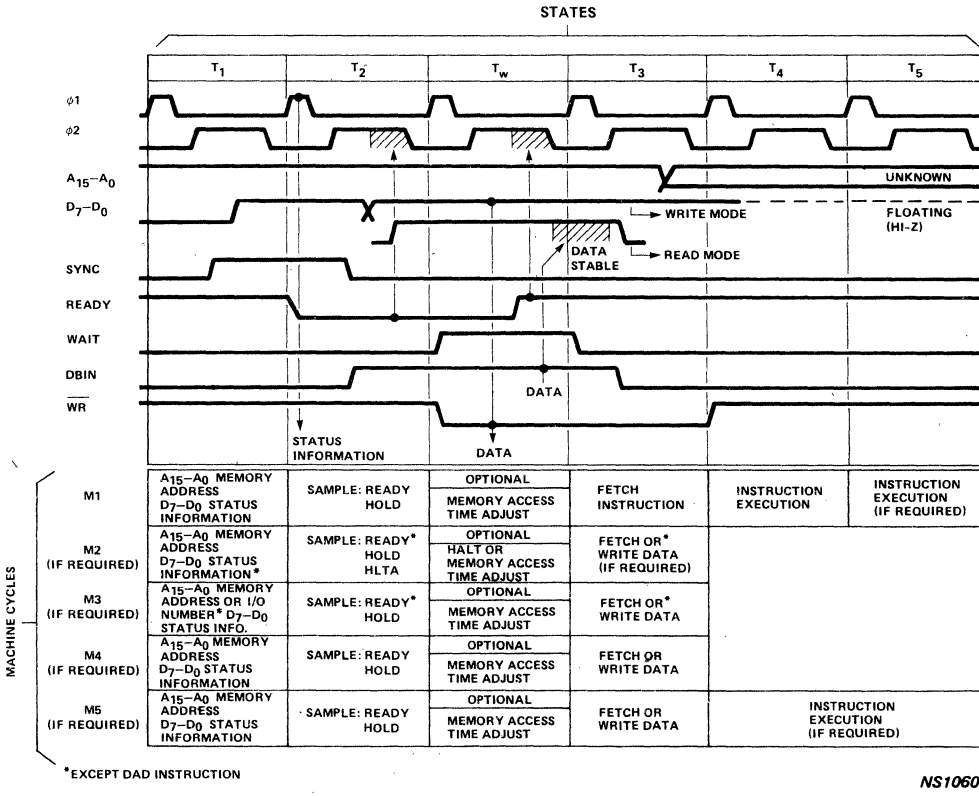


Figure 3-2. Basic Instruction Cycle

ecuted, a total of from 4 to 18 T states are required for a full instruction cycle.

Machine cycle M1 is always the operation-code fetch cycle and lasts from four to five T states. The duration of machine cycle M2, M3, M4, or M5 is normally three T states. During state T1 of a machine cycle, the following occur: the content of the Program Counter is placed on the A_{15}-A_0 Address Bus; the SYNC Signal (related to the leading edge of the $\phi 2$ clock) is activated (high); and status information pertaining to the current machine cycle (refer to 3.2.4) is outputted onto the External Data Bus. State T1 is always followed by T2, during which time the conditions of the READY and HOLD Signals are tested. In order to proceed to the T3 state, the READY Signal must be high (logic 1). If this signal is low (logic 0), the INS8080A enters the wait state (T_W) and remains there until the READY Signal goes high.

The type of machine cycle in progress determines the events that take place during the T3 state. During a FETCH machine cycle, the INS8080A inputs an instruction byte from the External Data Bus. During a MEMORY READ, STACK READ, or INPUT machine cycle, the INS8080A inputs a data byte from the External Data Bus. In an INTERRUPT machine cycle, an interrupt instruction of up to three bytes is jammed onto the External Data Bus and is routed to the CPU. The INS8080A outputs a data byte onto the External Data Bus during a MEMORY WRITE, STACK WRITE, or OUTPUT machine cycle.

States T4 and T5 are available if required for execution of a particular instruction. If the instruction being executed does not require either of these states, the CPU proceeds from the T3 state of a machine cycle directly to the T1 state of the next machine cycle. The T4 and T5 states are only used for internal processor operations.

3.2.2.2 State Transition Sequence

Figure 3-3 illustrates in flowchart form how the INS8080A proceeds from the T1 through T5

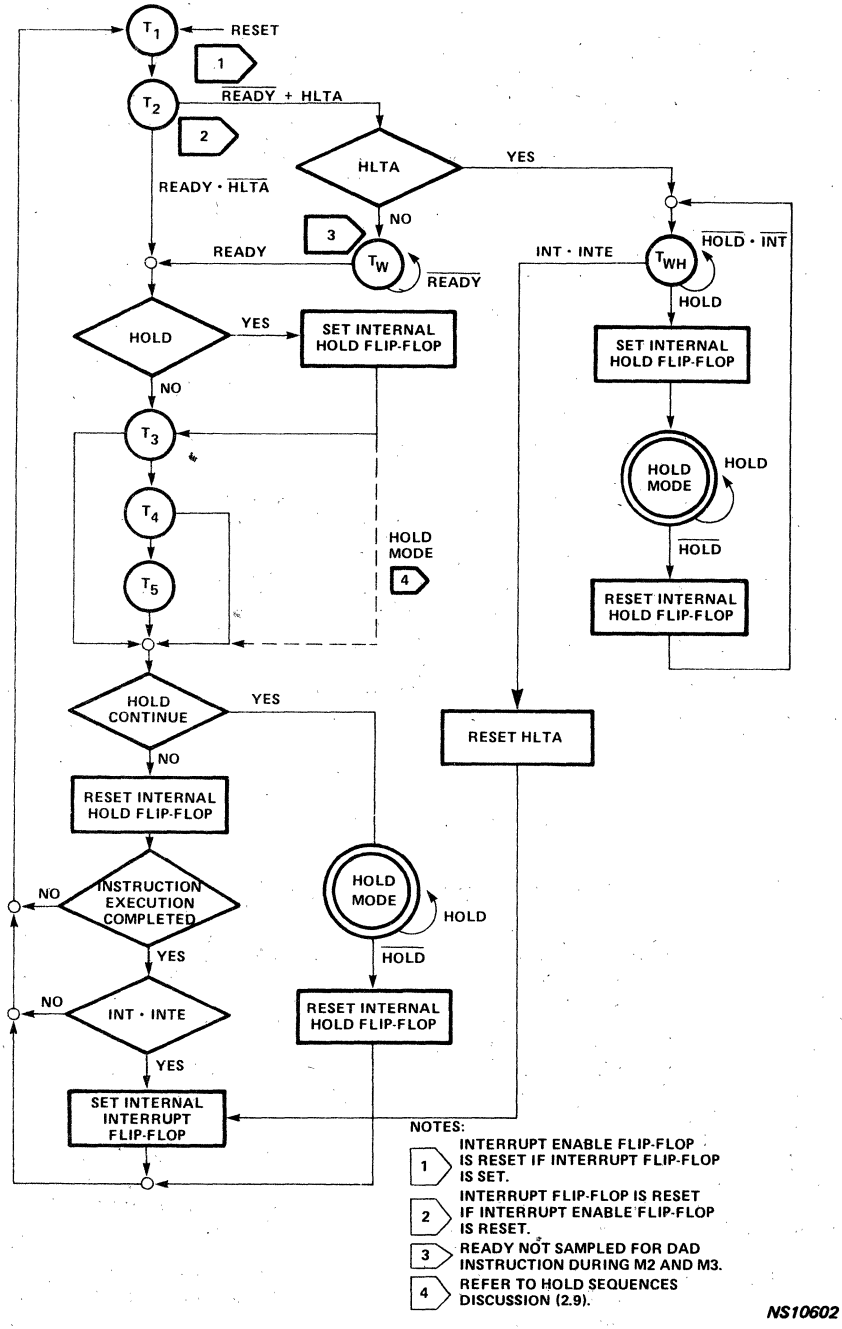


Figure 3-3. INS8080A CPU State Transition Flowchart

states of a machine cycle during the execution of an instruction. The actual number of states involved in a machine cycle depends on the instruction being executed and on the particular machine cycle of the instruction. The flow diagram also shows how the READY, HOLD, and INT lines are sampled during the machine cycle, and how the conditions on these lines affect the basic transition sequence. Only the basic sequence and the WAIT sequence are discussed below. The HOLD and INTERRUPT sequences are discussed later in this chapter.

In the basic sequence, the INS8080A does not wait for memory, does not hold, and is not halted. During this sequence, the READY input is held high, the HOLD input is held low, and the HALT Instruction is not executed. The INS8080A enters the WAIT sequence as a result of sampling a low READY Signal during the T2 state of every machine cycle, except for DAD (add Register Pair to H and L Registers) Instructions. (When executing DAD Instructions, the READY input is only sampled during the M1 machine cycle.) The WAIT sequence enables the INS8080A to adjust its processing cycle time to match the slower access time of the memory which requested the WAIT state. Beginning at T2, the memory must hold the READY line low for a number of clock cycles equal to the number to T_W states to be inserted in the machine cycle. The actual number of T_W states to be inserted is determined by external logic that is user-designed. The INS8080A does not furnish a control output during each state to directly indicate its internal state. Instead the microprocessor indicates the internal state by supplying INTE, HLDA, DBIN, $\overline{WR}$, and WAIT control signals to the external circuits.

3.2.3 Data and Instruction Representation

An 8-bit binary word or byte (see figure 3-4) is used to represent data in the INS8080A. Bit D_0 is the least significant bit (LSB) of the data word. The INS8080A instruction repertoire includes 1-byte, 2-byte, and 3-byte instructions (see figure 3-5). The exact instruction format depends on the particular operation to be executed. The first byte of an instruction contains the operation code. The second or third (if applicable) byte of a multiple-byte instruction contains either data or addressing information. Multiple-byte instructions must be stored in consecutive memory locations. For a multiple-byte instruction, the address of the first byte is used as the address of the instruction.

3.2.4 Status Information

The INS8080A outputs an 8-bit status word onto the D_7-D_0 External Data Bus during the first state (SYNC interval) of each machine cycle to identify the machine cycle in progress. A latch circuit for storing the status word for control of external circuits is illustrated in figure 3-6. (A similar latch is included in the INS8228/INS8238 System Controller and Bus Driver.) Table 3-2 defines the status information and indicates how this information is distributed on the External Data Bus. Table 3-3 lists the status bit outputs for each type of machine cycle.

3.2.5 Addressing Capabilities

The INS8080A chip has a 16-bit address capability, thus allowing any one of 65,536 memory locations to be uniquely specified. Data to be operated on are often stored in memory. When multi-byte numeric data are used, the data must be stored in consecutive memory locations. In this case, the least significant byte is stored first, followed by progressively more significant bytes.

Either the Program Counter, the Stack Pointer, or one of the 16-bit register pairs (BC, DE, and HL) is used in each memory-reference instruction. The Program Counter is always used to specify the addresses of program instructions (or data); it provides for the increasingly sequential execution of instructions, except when an interrupt or a branch instruction is effected. The Stack Pointer and the register pairs are used for other address/data requirements. The INS8080A has four different modes for addressing data stored in memory or in registers: these are immediate, direct, register, and register indirect. Each of the addressing modes is discussed below.

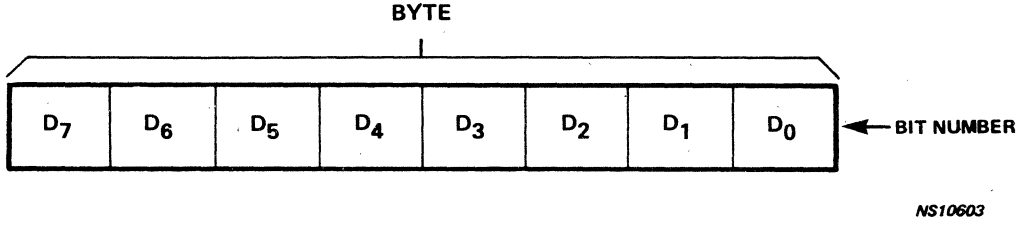
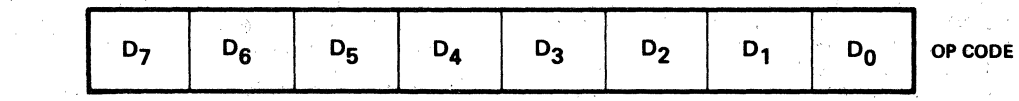
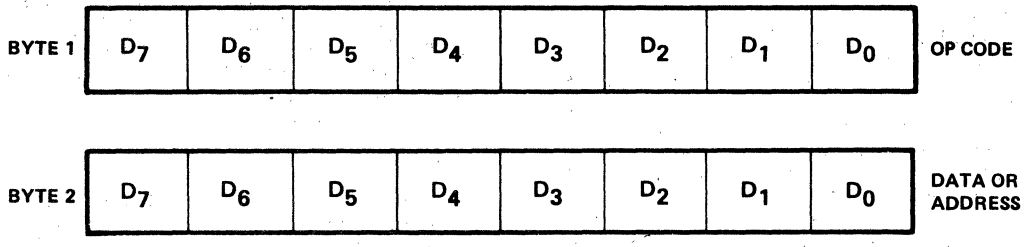


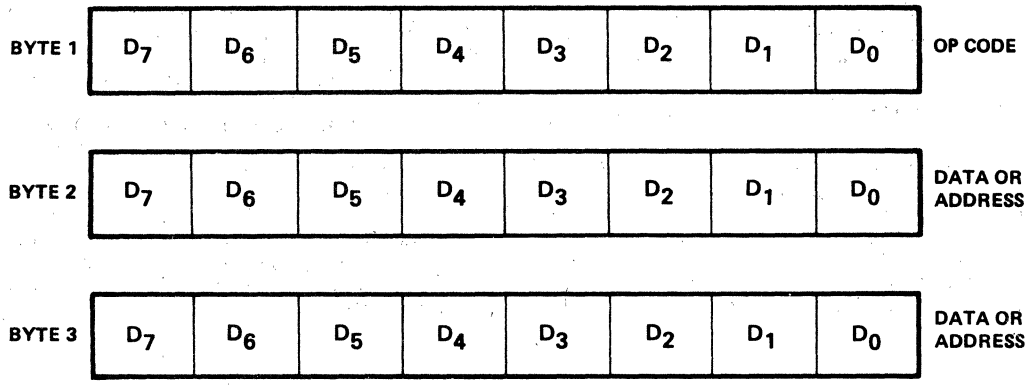
Figure 3-4. Data Word Format



A. One–Byte Instruction



B. Two–Byte Instruction



C. Three–Byte Instruction

NS10604

Figure 3-5. Instruction Formats

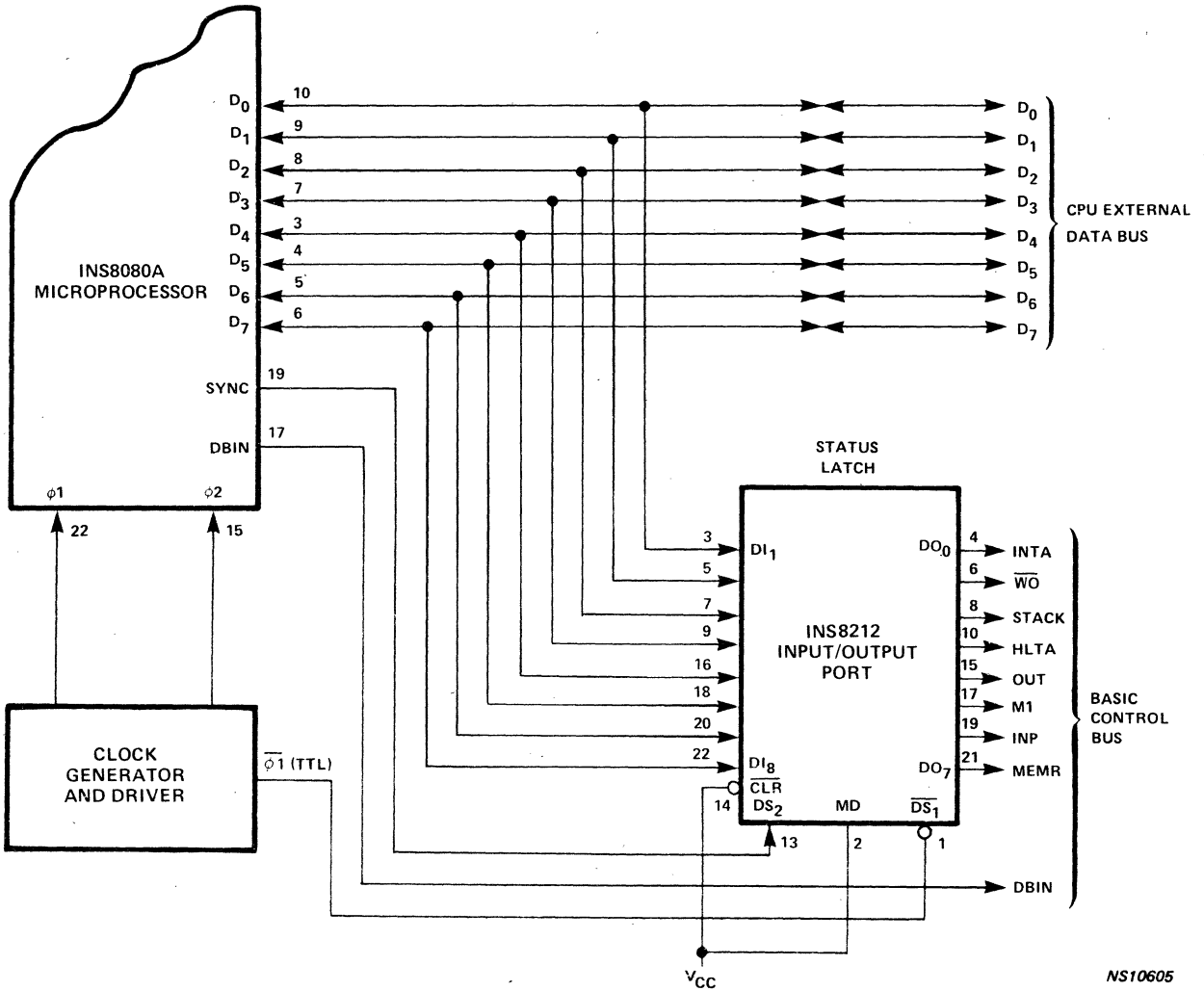


Figure 3-6. INS8080A Status Latch Circuit

Table 3-2. Status Information Distribution and Definition

SIGNAL MNEMONIC	DATA BUS BIT NUMBER	DEFINITION
INTA	D_0	Acknowledge signal for an Interrupt Request. When DBIN signal is high, the INTA signal should be used to gate an instruction (for example, Restart or Jump to Interrupt Service Routine) of up to three bytes onto the D_7-D_0 Data Bus. The INTA signal can also be used to control the flow of data onto the External Data Bus.
$\overline{WO}$	D_1	When low, indicates that the current machine cycle will be either a WRITE memory or OUTPUT operation. When high, a READ memory or INPUT operation will be executed.
STACK	D_2	When high, indicates that the A_{15}-A_0 Address Bus contains the pushdown stack address from the Stack Pointer (SP).
HLTA	D_3	Goes high to acknowledge a Halt Instruction.
OUT	D_4	When high, indicates that the A_{15}-A_0 Address Bus contains the address of an output device and that the External Data Bus will contain the output data when the $\overline{WR}$ is low.
M_1	D_5	Goes high to indicate that the INS8080A is in the fetch cycle for the first byte of an instruction.
INP	D_6	When high, indicates that the A_{15}-A_0 Address Bus contains the address of an input device and that the Data Bus will contain the input data when the DBIN signal is high. The INP signal can also be used to control the flow of data onto the Data Bus.
MEMR	D_7	When high, indicates that the Data Bus will be used for READ memory data. The MEMR signal can also be used to control the flow of data onto the Data Bus.

Table 3-3. Status Bit Outputs For Each Type of Machine Cycle

TYPES OF MACHINE CYCLES	STATUS WORD TYPE	DATA BUS BITS							
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction Fetch	1	1	0	1	0	0	0	1	0
Memory Read	2	1	0	0	0	0	0	1	0
Memory Write	3	0	0	0	0	0	0	0	0
Stack Read	4	1	0	0	0	0	1	1	0
Stack Write	5	0	0	0	0	0	1	0	0
Input Read	6	0	1	0	0	0	0	1	0
Output Write	7	0	0	0	1	0	0	0	0
Interrupt Acknowledge	8	0	0	1	0	0	0	1	1
Halt Acknowledge	9	1	0	0	0	1	0	1	0
Interrupt Acknowledge While Halt	10	0	0	1	0	1	0	1	1

3.2.5.1 Immediate Addressing

In this mode, the instruction contains the required data in either the second byte (8-bit data quantity) or the second and the third bytes (16-bit data quantity). When the data represent a 16-bit quantity, the least significant byte is first, followed by the most significant byte. The immediate addressing mode is relatively fast because an additional data address is not formed, nor is an additional memory access required to fetch data.

3.2.5.2 Direct Addressing

In this mode, the instruction contains the exact memory address of the required data or instruction in the second and third bytes. Byte 2 contains the lower-order bits of the memory address and byte 3 contains the higher-order bits. Jump and Branch Instructions are executed via the direct addressing mode. It is also used for a limited number of memory-reference instructions.

3.2.5.3 Register Addressing

The register addressing mode is conceptually identical to the direct addressing mode. In the register addressing mode, a one-byte instruction is used to specify the register or the register pair in which the required data are located.

3.2.5.4 Register Indirect Addressing

In this mode, a 1-byte instruction specifies a register pair (or Stack Pointer) that contains the exact memory location of the required data or instruction. The high-order bits of the memory address are in the first 8-bit register (B, D, or H) of the specified register-pair and the low-order bits of the address are in the second 8-bit register (C, E, or L).

3.2.6 Input/Output Operation and Control

High-speed data transfers between the microprocessor, memory, and input/output peripheral devices are made in parallel. The data and address ports of the INS8080A chip are connected to memory or other peripherals via an 8-bit bidirectional External Data Bus and a 16-bit unidirectional Address Bus, respectively. Various timing and control signals (for example, SYNC, DBIN, and so forth) and status information are generated during the data transfers.

3.2.6.1 Data Input Operations

The input cycle consists of reading data from either a specified memory location or from an input peripheral device. Timing is shown in figure 3-7 for a data-input operation. As shown, status information is initially transferred onto the D_7-D_0 External Data Bus during the SYNC signal interval. The low-to-high transition of the $\phi 2$ clock during state T2 clears the status information from the External Data Bus, preparing the bus for the receipt of incoming data. At this time, the A_{15}-A_0 Address Bus contains a valid address and any one of 65,536 memory locations or 256 input peripheral devices may be selected. Data subsequently placed on the D_7-D_0 Data Bus by memory or an input peripheral device then are sampled during the T3 state of a machine cycle. During the inputting of data to the microprocessor, the INS8080A generates a high DBIN signal which is used externally to enable the data transfer. The DBIN signal is initiated by the leading edge of the $\phi 2$ clock during state T2 and is terminated by the leading edge of the $\phi 2$ clock during state

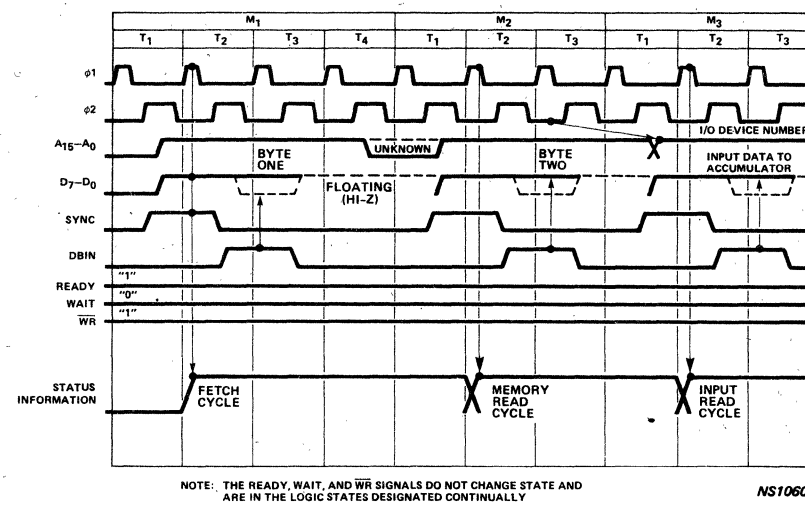


Figure 3-7. Data Input Operation Timing

T3. (During the WAIT sequence, the DBIN signal is extended one or more clock periods by any T_W states intervening between states T2 and T3.) Machine cycles during which the DBIN signal is generated include FETCH, MEMORY READ, STACK READ, and INTERRUPT.

3.2.6.2 Data Output Operations

The output cycle consists of writing data into either a specified memory location or to an output peripheral device. Figure 3-8 shows the timing for a data-output operation. The outputting of status information onto the D_7-D_0 Bus and address information onto the A_{15}-A_0 Bus is as described above for data-input operations. The rising edge of $\phi 2$ within state T2 clears status information from the D_7-D_0 Data Bus and loads in the data that are destined for memory or for peripherals. Note that a high READY signal is also required during an output cycle. If a high READY signal is not present, the microprocessor enters the T_W state following the T2 state. In this case, data on the D_7-D_0 lines remain stable during the wait state, and the processing cycle will not proceed until the READY goes high. During the outputting of data from the microprocessor (MEMORY WRITE, STACK WRITE, and OUTPUT machine cycles), the INS8080A generates a low $\overline{WR}$ output for synchronization of external transfers. The $\overline{WR}$ is initiated by the leading edge of the first $\phi 1$ clock following T2 and is terminated by the leading edge of the $\phi 1$ clock during the state following T3. During the WAIT sequence, the $\overline{WR}$ output is extended one or more clock periods by any T_W states intervening between states T2 and T3.

3.2.7 Interrupts

Figure 3-9 illustrates the timing for an interrupt. A peripheral device requests an interrupt by raising the microprocessor's INT line high. The INS8080A acknowledges the asynchronous interrupt request at the completion of the instruction in progress, providing interrupts have not been disabled either by an interrupt service not followed by a new Enable Interrupts Instruction or by a Disable Interrupts Instruction. During the first clock period (SYNC interval) of the INTERRUPT machine cycle, the microprocessor outputs a high INTA status bit (D_0) to indicate acknowledgement of the external request.

The asynchronous interrupt request is reclocked by internal logic to establish a proper relationship with the $\phi 2$ clock. As shown, an interrupt request that is made when the INTE line is high (enabled), causes the internal interrupt flip-flop to be set by the $\phi 2$ clock pulse during the last state of the instruction cycle in progress. This action ensures the completion of any instruction being executed before the processing of the interrupt. The INTERRUPT machine cycle that follows an enabled interrupt request is similar to a FETCH machine cycle, except that the Program Counter is not incremented during the acceptance of the interrupt instruction and the contents of the Program Counter and status information are pushed onto the external stack. In this way, the correct pre-interrupt instruction address is maintained in the external stack during the interrupt machine cycle.

The interrupting device identifies its required service routine by jamming an instruction of up

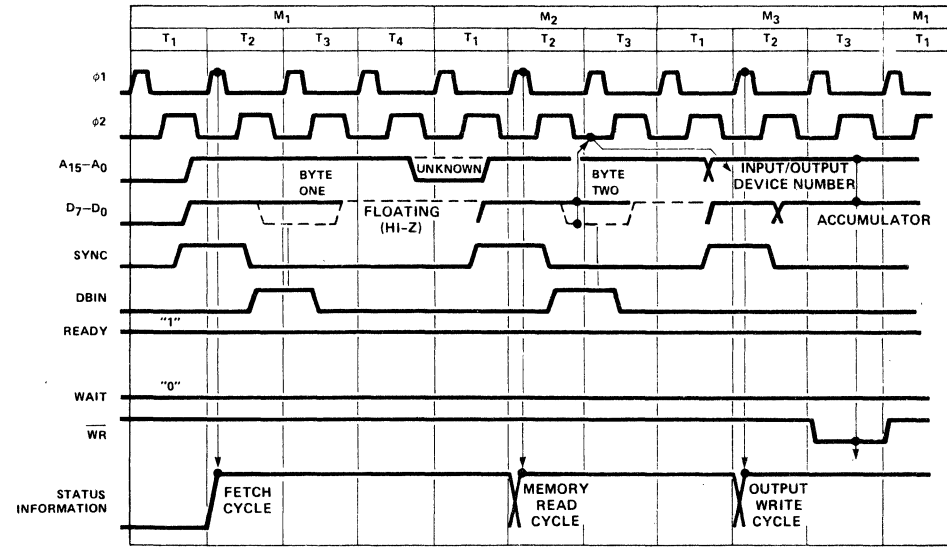


Figure 3-8. Data Output Operation Timing

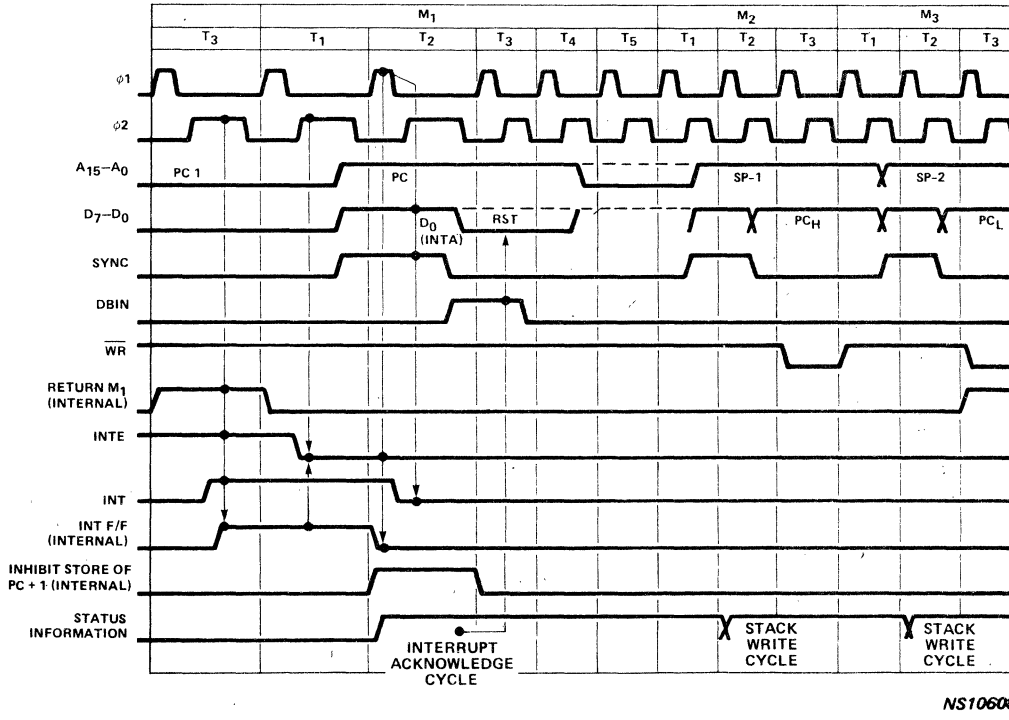


Figure 3-9. Interrupt Timing

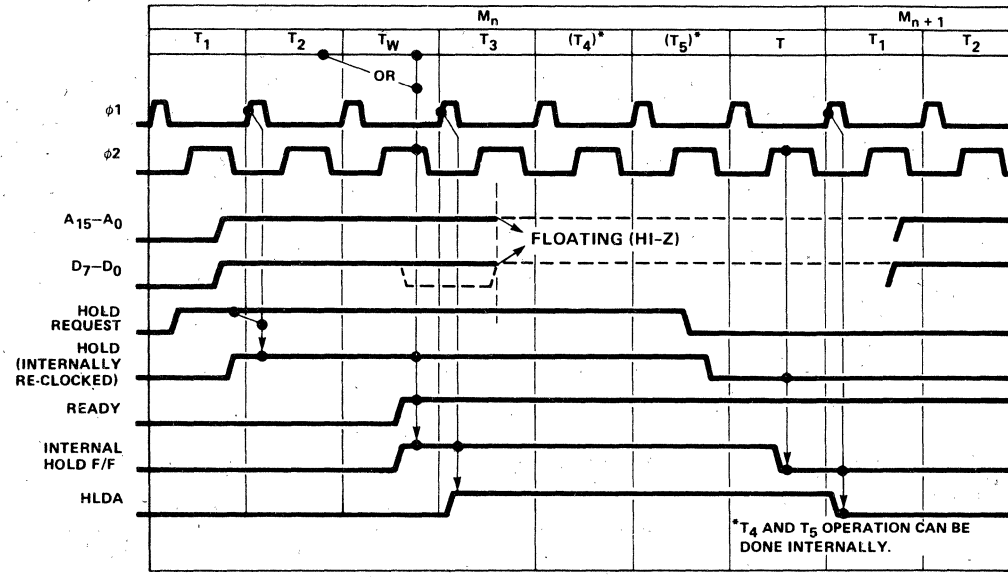
to three bytes onto the D_7-D_0 External Data Bus during state T3, when the DBIN signal is high (for example, a Call Conditional, a Jump Conditional, or a Restart Instruction). During this time, memory and other peripherals are temporarily in the high-impedance state, thereby allowing the interrupting device to control the External Data Bus. The Restart Instruction, for instance, includes a 3-bit variable field that is used to call a routine in one of eight memory locations with the following hexadecimal addresses: 0000, 0008, 0010, 0018, 0020, 0028, 0030, and 0038. Any of these addresses may be used to store the first instruction of a service routine for the requesting device.

3.2.8 Hold Operations

Direct Memory Access (DMA) is a method frequently used to effect data transfers between peripherals and memory. Using this technique, data transfers can be directly implemented without involving the microprocessor. In the INS8080A, provisions are included for DMA transfers. A peripheral requests a DMA transfer by placing a high level on the HOLD line of the INS8080A. This, in turn, may cause the microprocessor to suspend temporarily its operations and the address and data buses to go to the high-impedance state (float). The INS8080A acknowledges the asynchronous HOLD request by placing a high on the HLDA line. When its HOLD request is acknowledged, the related peripheral device takes control of the address and data buses, thereby allowing the device to effect direct data transfers to memory.

Figure 3-10 shows the timing of a HOLD operation for a READ MEMORY or INPUT machine cycle, and figure 3-11 shows the timing of a HOLD operation for a WRITE MEMORY or OUTPUT machine cycle. Note that in both cases, the asynchronous HOLD request is re-clocked by internal logic to establish the proper relationship with the $\phi 2$ clock. As shown, a HOLD request that is made when the READY line is high, causes the internal hold flip-flop to be set by the $\phi 2$ clock pulse. With the flip-flop set, the subsequent leading edge of the $\phi 1$ clock pulse causes the HLDA output to go high at either the T3 state for a READ MEMORY or INPUT cycle or at the clock period following the T3 state for a WRITE MEMORY or OUTPUT cycle. In either case, the A_{15}-A_0 Address Bus and D_7-D_0 External Data Bus are floated (high-impedance state) after the leading edge of the next $\phi 2$ clock pulse.

Once the address and data buses of the INS8080A are floated, the microprocessor usually suspends its operations. However, if the HOLD request was acknowledged at the T3 state and if a particular machine cycle requires the T4 and T5 states, the microprocessor continues these operations internally. Thus, the internal processing activities do not end until the machine cycle is terminated.



NS10609

Figure 3-10. Hold Operation Timing for MEMORY READ or INPUT Cycle

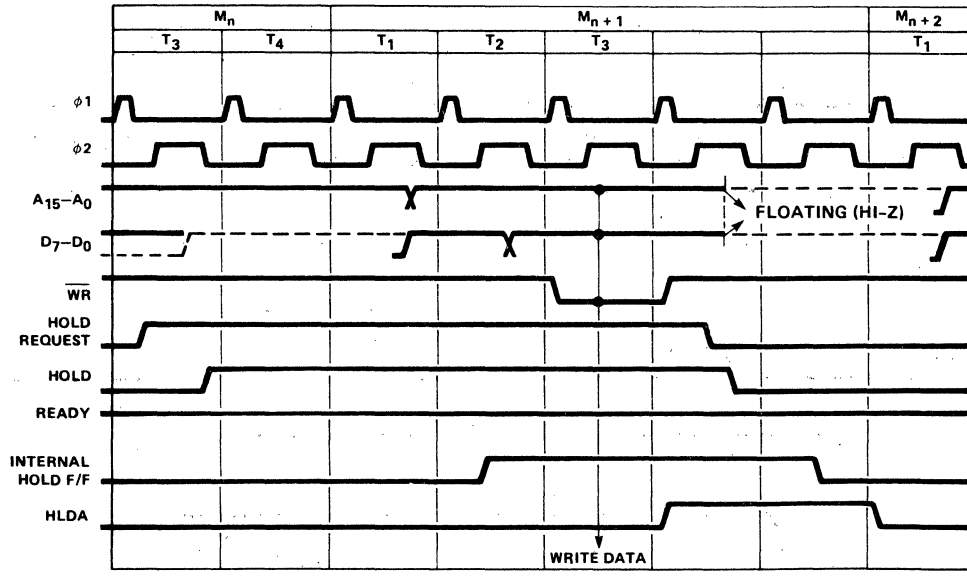


Figure 3-11. Hold Operation Timing for MEMORY WRITE or OUTPUT Cycle

When the peripheral device has completed the DMA transfer, it places a low level on the HOLD line of INS8080A. This low level causes the microprocessor to leave the HOLD state through a sequence similar to that by which it entered. Following the leading edge of the next $\phi 1$ clock pulse, the HLDA output returns to a low level. Normal processing then resumes with the machine cycle following the last cycle that was executed.

3.2.9 Microprocessor Halt

The Halt (HLT) Instruction is used to effect a programmed halt condition. When the HLT Instruction is executed, the INS8080A enters the halt state (T_{WH}) after state T2 of the next machine cycle as shown in figure 3-12. The microprocessor can exit the halt state in only the following three ways, which are shown in the Halt Sequence Flowchart of figure 3-13.

1. A high level on the microprocessor's RESET line resets the INS8080A to state T1, and clears the Program Counter as described in 3.2.10.
2. A high level on the HOLD line causes the microprocessor to enter the HOLD state as described in 3.2.8. When the HOLD line is subsequently driven low, the INS8080A reenters the halt state at the leading edge of the next $\phi 1$ clock pulse (see figure 3-14).
3. A high level on the INT line, while the INTE output line is high, causes the INS8080A to exit the halt state and enter state T1 on the leading edge of the next $\phi 1$ clock pulse (see figure 3-14).

3.2.10 Initialization

When power is first appplied to the INS8080A, an external high-level signal of at least three clock periods in duration is placed on the RESET line to clear the Program Counter (see figure 3-15). Thus, the first instruction is always fetched from memory location 0000_{16} after the power-up initialization cycle. The Status Flag Register, the Stack Pointer, and other working registers (Accumulator, B Register, C Register, and so forth) are unaffected by the active RESET signal. Instead, these registers are initialized by related instructions within the program.

3.3 INS8224 CLOCK GENERATOR AND DRIVER

The INS8224 is a single-chip crystal controlled clock generator and driver for the INS8080A.

Figure 3-16 is a functional block diagram of the INS8224 chip. The INS8224 provides $\phi 1$ and $\phi 2$ MOS clocks, a power-on RESET Signal, and a synchronized READY Signal for the INS8080A. In addition, the INS8224 provides a Status Strobe ($\overline{STSTB}$) for the INS8228/INS8238 System Controller and Bus Driver, and a $\phi 2$ TTL

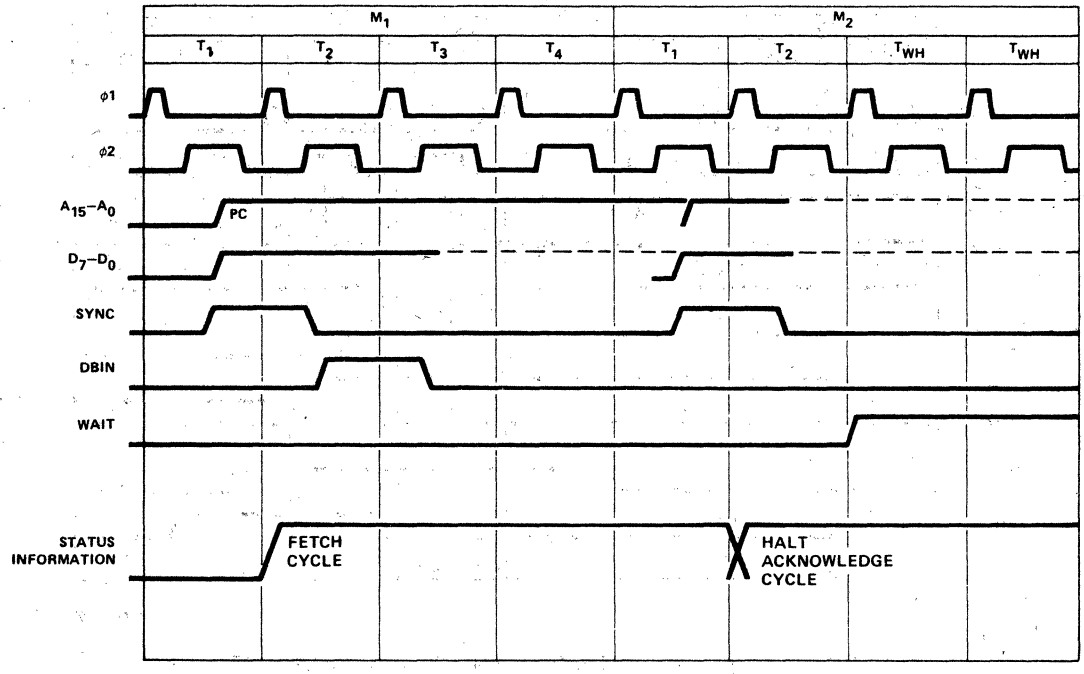


Figure 3-12. Halt Timing

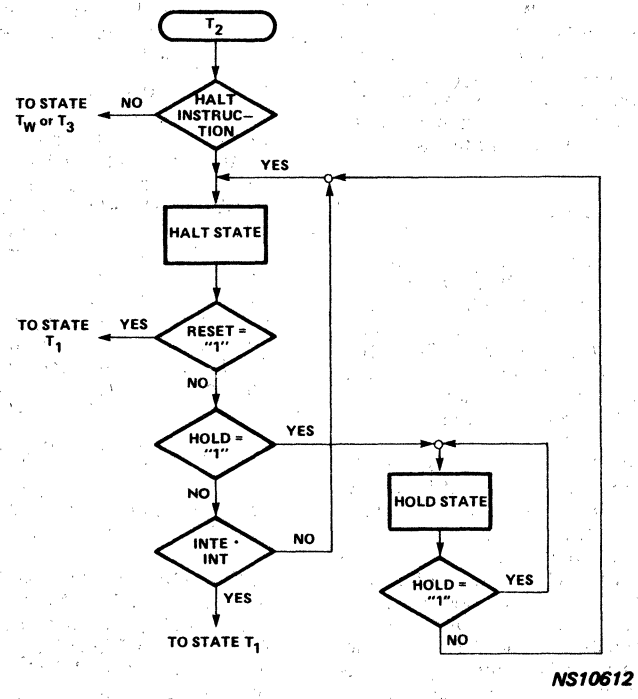


Figure 3-13. Halt Sequence Flowchart

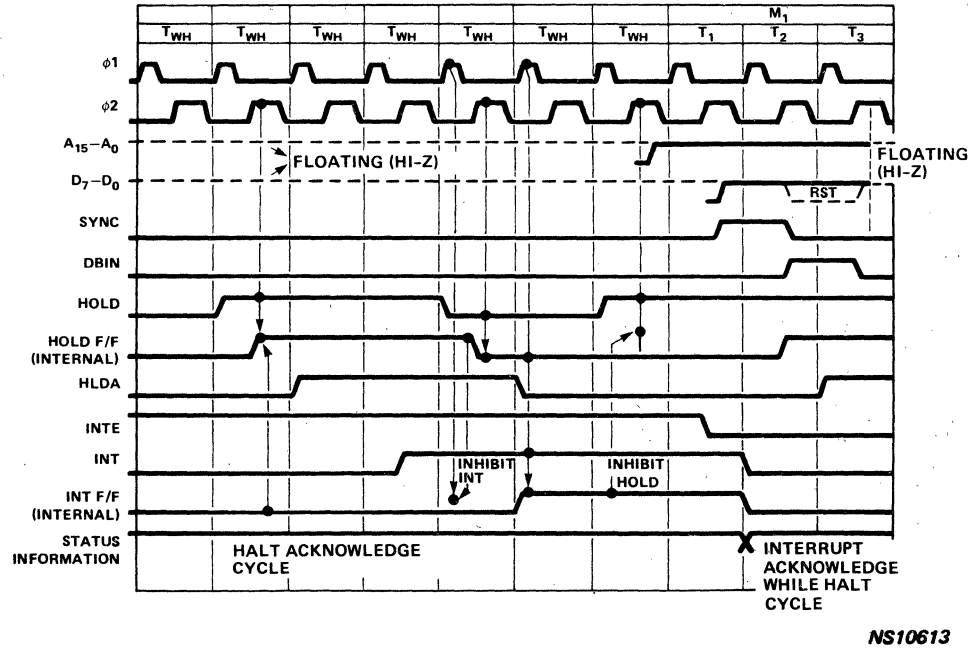


Figure 3-14. Relation Between HOLD and INT in the HALT State

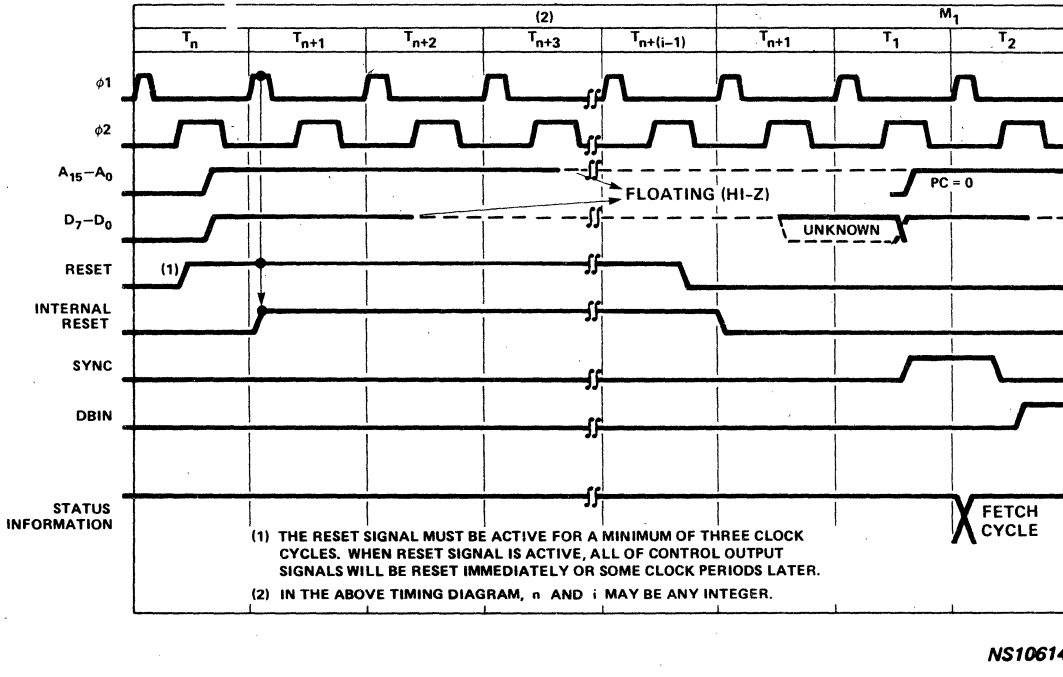


Figure 3-15. Initialization Timing

Clock, and an Oscillator (OSC) Signal to accommodate user requirements.

The INS8224:

- Has Crystal-Controlled Oscillator for Stable Operation
- Provides Status Strobe for INS8228
- Provides Power-On Reset for INS8080A

An external, series-resonant crystal provides frequency control for the oscillator circuit as shown in figure 3-16. Normally, a fundamental mode crystal is used to determine the basic operating frequency of the oscillator. However, an overtone mode crystal (which generally has a lower gain) may also be used. When an overtone mode crystal is used, the TANK input of the chip is connected to a parallel LC network (AC coupled to ground) to offset the lower gain of the overtone mode crystal. Regardless of the type of crystal used, the crystal frequency is nine times the desired microprocessor speed (crystal frequency = 1/tCY × 9). When the crystal frequency is above 10 megahertz, a selected capacitor of from 3 to 10 picofarads may have to be connected in series with the crystal to produce the exact desired frequency. The stable, crystal-controlled oscillator output is routed to the OSC chip pinout via a buffer for external timing purposes, and to the clock generator circuit.

The clock generator circuit comprises a divide-by-nine counter and the associated decode gating logic. The circuit generates the $\phi 1$ and $\phi 2$ clocks (see figure 3-17) and internal timing signals. All of the nonoverlapping waveforms generated follow a simple 2-5-2 pattern. Two of the clock generator outputs are routed to high-level drivers, which convert the TTL$\phi 1$ and $\phi 2$ clocks to MOS level clocks. A third output of the clock generator is routed to the $\phi 2$ (TTL) chip pinout for external timing purposes.

The $\overline{\text{STSTB}}$ Signal is generated by gating a high-level SYNC input from the INS8080A with the $\phi 1$A internal timing signal from the clock generator circuit. The $\overline{\text{STSTB}}$ Signal is used to clock status information onto the status latch of the INS8228/INS8238 System Controller and Bus Driver.

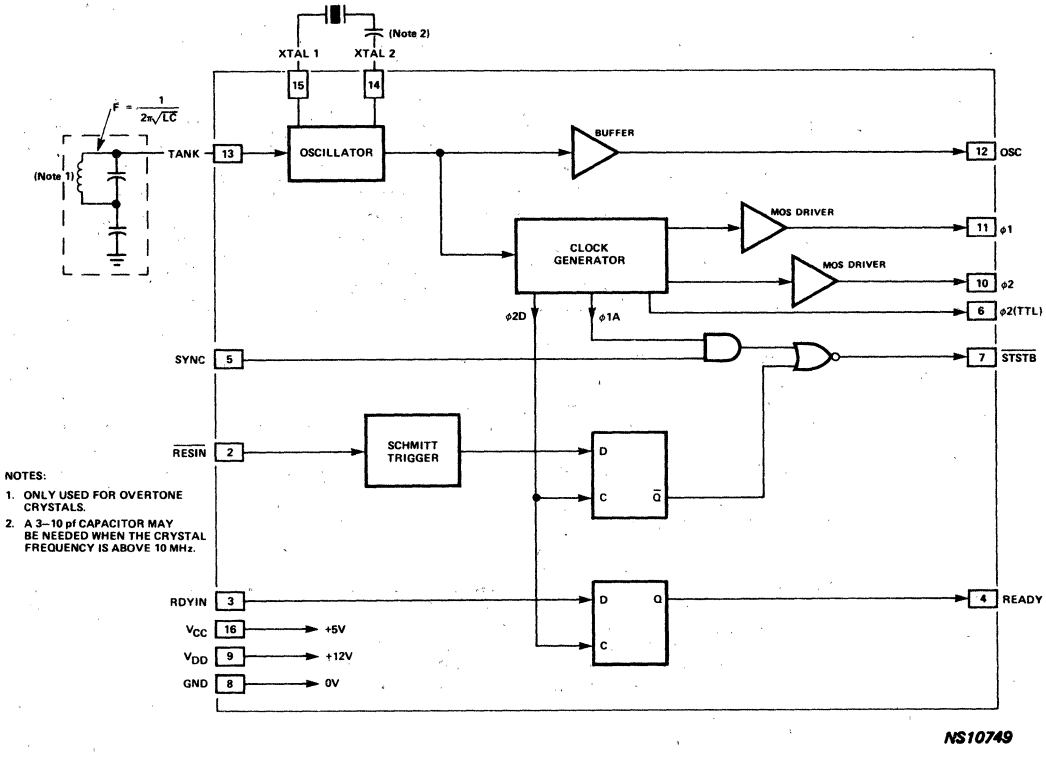
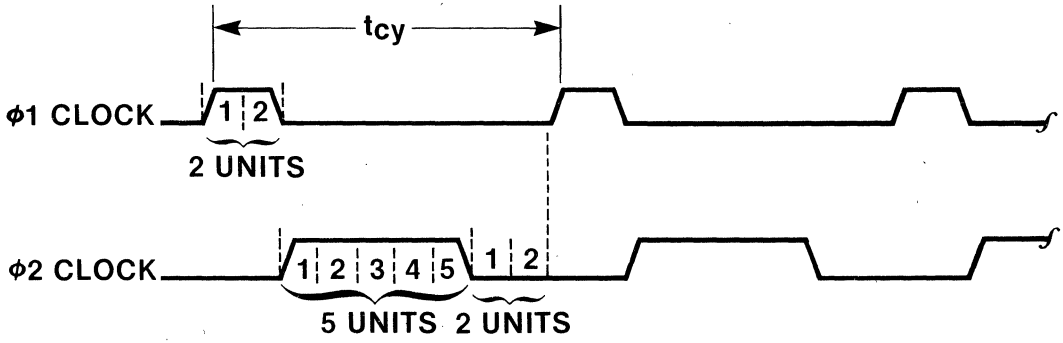


Figure 3-16. INS8224 Functional Block Diagram



$$1 \text{ UNIT} = \frac{1}{f_{osc}}$$

Figure 3-17. Relative Timing of INS8224 Clock Output Waveforms

A Schmitt Trigger circuit is used in conjunction with a D-type flip-flop to provide an automatic system reset and startup upon application of power as follows. The $\overline{\text{RESIN}}$ input, which is obtained from the junction of an external RC network that is connected between V_{CC} and ground, is routed to the internal Schmitt Trigger circuit. This circuit converts the slow transition of the power supply rise into a sharp, clean edge when its input reaches a predetermined value. When this occurs, the succeeding D-type flip-flop is synchronously reset, thereby providing the RESET output signal. For manual system reset, a momentary contact switch that provides a low (ground) when closed, is also connected to the $\overline{\text{RESIN}}$ input.

The synchronized READY signal is generated by a D-type flip-flop, which is clocked by the ϕ2D internal timing signal output of the clock generator. The D-type flip-flop re-clocks an asynchronous Ready Input (RYDIN) signal to provide the synchronous READY Signal to the INS8080A.

A typical INS8224-to-INS8080A interconnection is shown in figure 3-18.

3.4 INS8228/INS8238 SYSTEM CONTROLLER AND BUS DRIVER

The INS8228/INS8238 generates all the read and write control signals required to directly interface the memory and input/output components of the N8080 family. The INS8228/INS8238 also provides drive and isolation for the bidirectional data bus of the INS8080A Microprocessor, a user-selected single-level interrupt vector (RST7) for use in the interrupt structure of small systems that require only one basic vector, and an Interrupt Acknowledge Signal ($\overline{\text{INTA}}$) for each byte of a multibyte CALL Instructon. Advanced I/O Write ($\overline{\text{I/O W}}$) and Memory Write ($\overline{\text{MEM W}}$) Signals are provided only by the INS8238 chip for large-system timing control. Figure 3-19 is a functional block diagram of the INS8228/INS8238 chip.

The bidirectional bus driver is a parallel 8-bit, TRI-STATE circuit that buffers the INS8080A D_7-D_0 External Data Bus from memory and input/output devices. The bus driver circuit also assures that the input/output requirements of the CPU data bus (3.3 volts minimum input and 1.9 milliamperes maximum drive output) are exceeded, thereby enhancing noise immunity. In addition, the bus driver circuit has sufficient output drive capability (up to 10 milliamperes) for directly connecting a large number of memory and input/output devices to the system data bus. The chip gating array (figure 3-20) controls the operation of the bidirectional bus driver so that proper bus flow is maintained, and so that the driver circuit is driven into the high-impedance state during a DMA data transfer.

The status latch uses the low-level Status Strobe ($\overline{\text{STSTB}}$) from the INS8224 Clock Generator and Driver to store the status word that is outputted onto the CPU data bus by the INS8080A at the start of each machine cycle. The latched outputs of the status latch are, in turn, routed to the chip gating array.

The gating array generates read and write control signals by gating the status latch outputs with various control signals from the INS8080A

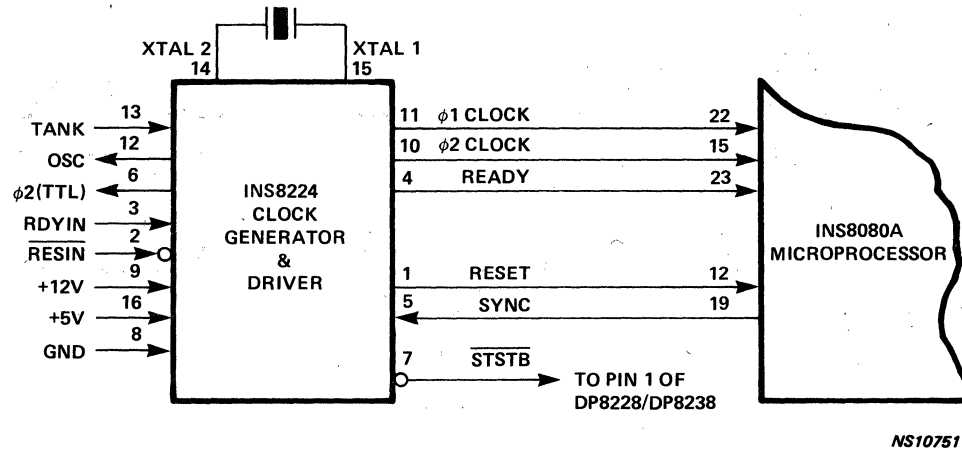


Figure 3-18. INS8224 to INS8080A Interconnection

Microprocessor. The read control signals (MEMR, I/OR, and INTA) are obtained by gating the appropriate status latch bit(s) with a high-level DBIN signal from the INS8080A. Similarly, the write control signals (MEMW and I/OW) are obtained by gating the appropriate status latch bit(s) with a low level WR signal from the INS8080A. During a DMA data transfer, the gating array and bidirectional bus driver are driven to the high-impedance state by high-level BUSEN and HLDA inputs. When using a multibyte CALL as an Interrupt Instruction, the INS8228/INS8238 generates an INTA pulse for each of the three bytes of the instruction, when an interrupt is acknowledged by the INS8080A.

The INS8228/INS8238 can be used to insert a single-level interrupt vector (RST 7) onto the CPU data bus with a high-level DBIN signal, when an interrupt is acknowledged by the INS8080A. To use this feature of the chip, the INTA output (pin 23) must be connected to an external 12-volt power supply via a 1-kilohm resistor. A typical INS8228/INS8238-to-INS8080A interconnection is shown in figure 3-20.

3.5 CPU CHIP SET

The INS8080A and its two CPU Group support devices, the INS8224 and the INS8228/INS8238, constitute the minimum components to implement the MICROBUS. The minimum CPU Group is sufficient for implementing a minimal system with only a linear select addressing capability.

An illustration of a minimal CPU Group is shown in figure 3-21. For expanded CPU Group see figure 2-8, INS8080 family CPU group to MICROBUS Configuration. Refer to appendix A.8 for System Timing Diagram.

For descriptions of the devices required to expand the minimal CPU Group into one with an expanded capability refer to the sections listed below:

- Expanded chip selects (see section 4.4)
- Interrupt expansion (see section 4.7)
- Address expansion (see section 4.3)

For INS8080A instruction set, see chapter 11.

3.5.1 DM8131 6-Bit Unified Bus Comparator

The DM8131 compares two 6-bit binary words and indicates equality by the output going low. The application shown utilizes the DM8131 to select a 2K block of memory/peripheral space with the INS82LS05 selecting 8 blocks of 256 each, within the 2K block.

Features:

- Low Bus Current Input
- High Bus Noise Immunity
- TTL Output

3.5.2 INS82LS05 One-of-Eight Binary Decoder

The INS82LS05 decodes one of eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. It is designed to be used in high-performance memory-decoding or data-routing application, requiring very short propagation delay times.

Features:

- Three enable inputs simplify cascading
- Schottky clamped for high speed

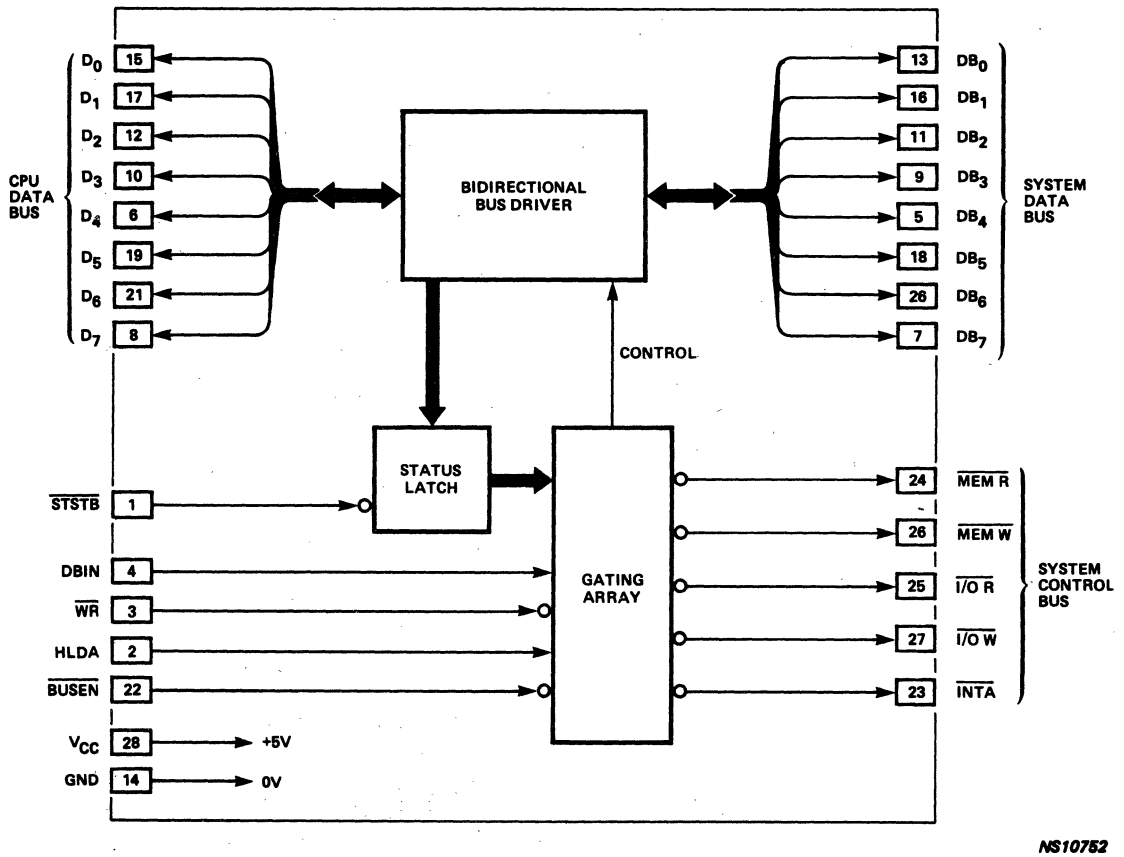


Figure 3-19. INS8228/INS8238 Functional Block Diagram

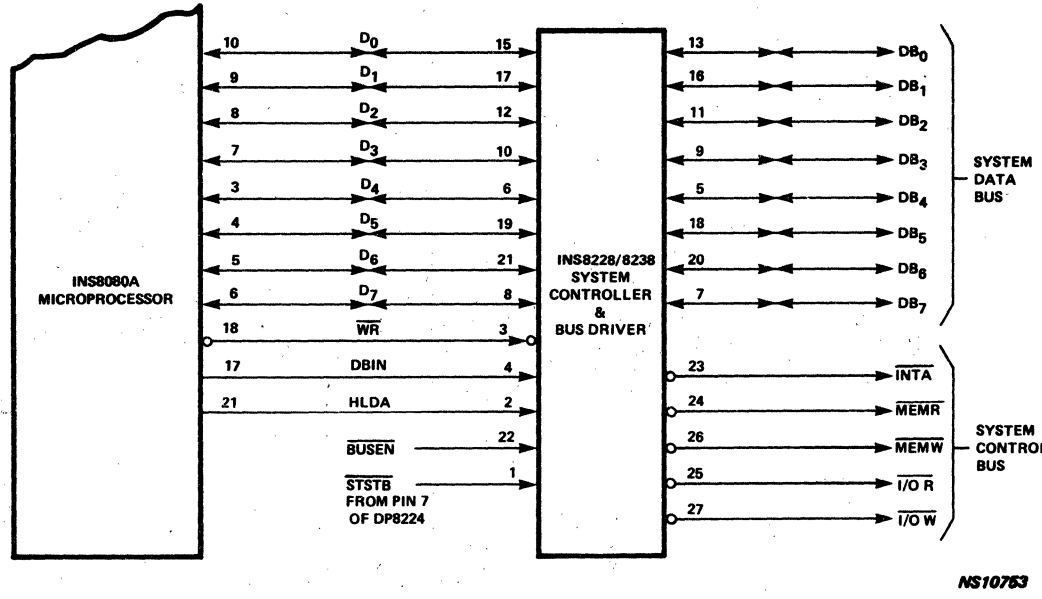


Figure 3-20. INS8228/INS8238 to INS8080A Interconnection

3.5.3 INS8257 Programmable DMA Controller

The INS8257 is a four-channel Direct Memory Access (DMA) controller that generates sequential memory addresses which allow the peripherals to read or write data directly from or to memory. Peripheral interrupt requests are prioritized internal to the INS8257 and are issued as a composite bus request signal to the CPU. Each channel contains a cycle counter that allows the INS8257 to maintain control of the number of memory locations accessed by the peripherals. Additional input controls enable sectored data transfers and expansion of the DMA capabilities.

Features:

- Four-Channel DMA Control
- Priority DMA Request Logic
- Channel Inhibit Logic
- Auto Load Mode

3.5.4 INS8259 Programmable Interupt Controller

The INS8259 handles multilevel priority interrupts in a variety of modes, and requires no clock input. The chip functions as an 8-level priority interrupt controller, expandable to 64 levels.

Features:

- Programmable Interrupt Modes
- Expandable 8-level Interrupt Controller
- Individual Request Mask Capability
- Static Operation

See also Section 4.7, Expanding Interrupts, and figure 2-8, INS8080 Family CPU Group to MICROBUS Configuraton.

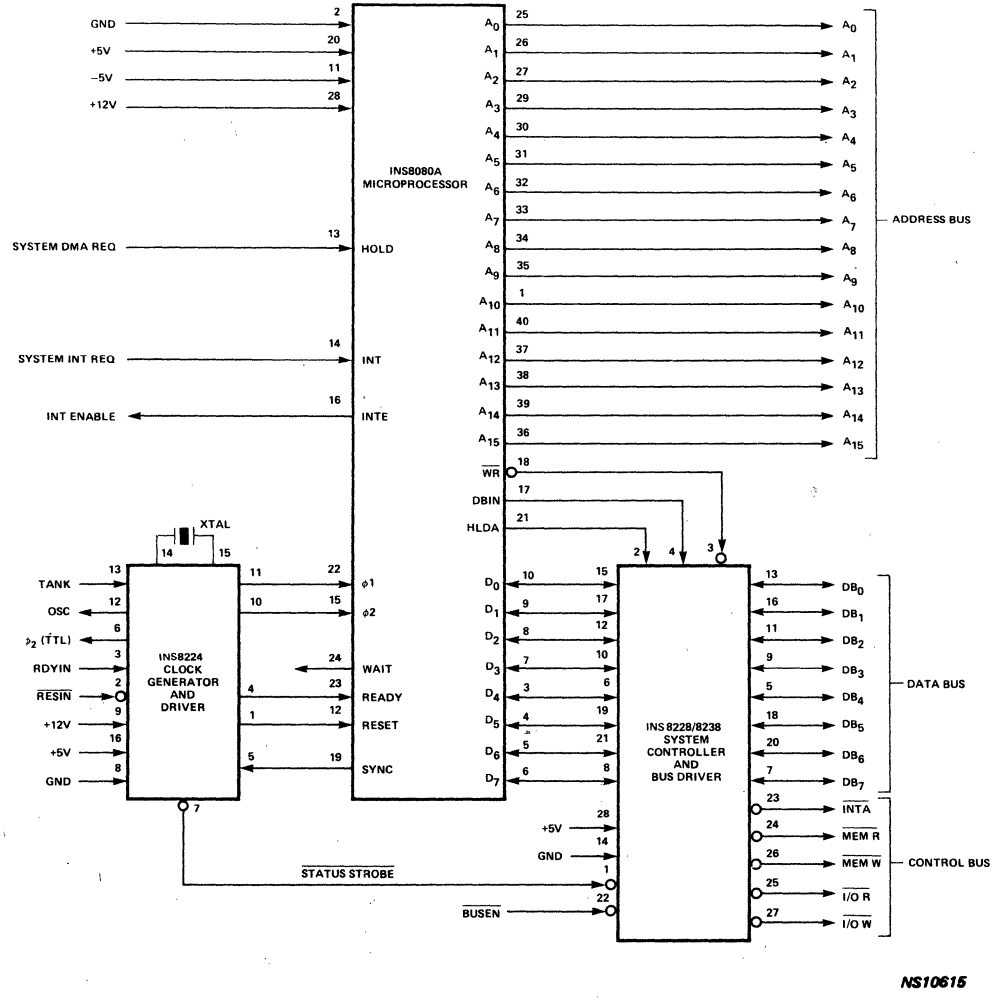
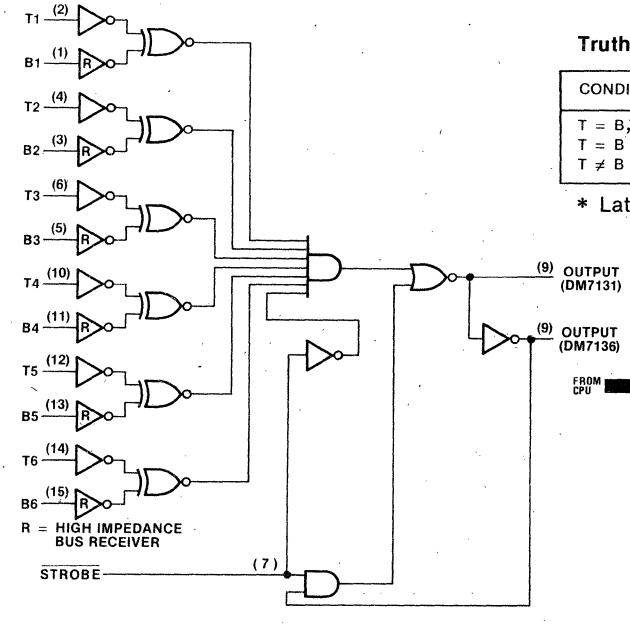


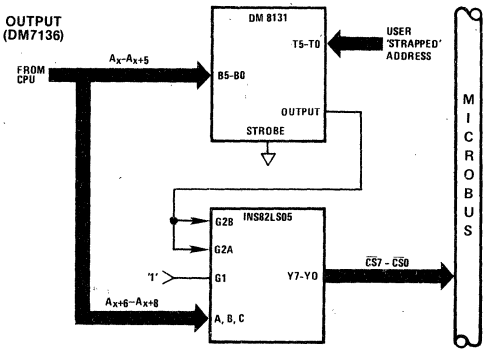
Figure 3-21. Preferred Method of CPU Group Implementation



Truth Table

CONDITION	$\overline{\text{STROBE}}$	OUTPUT	
		DM71/8131	DM71/8136
T = B, T ≠ B	H	O_{N-1}*	O_{N-1}*
T = B	L	L	H
T ≠ B	L	H	L

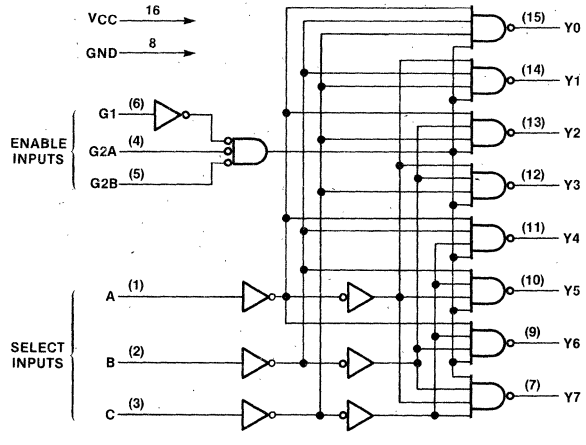
* Latched in previous state

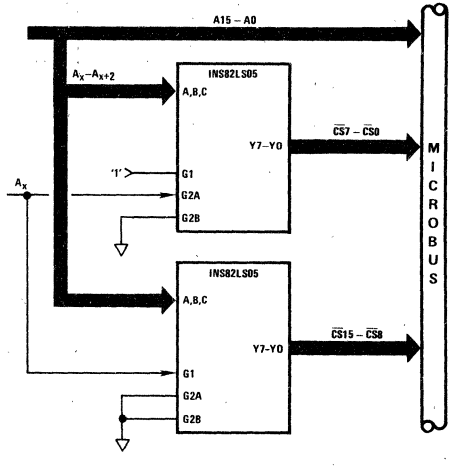


Internal Block Diagram

Typical MICROBUS Interface

Figure 3-22. DM8131 6-bit Unified Bus Comparator

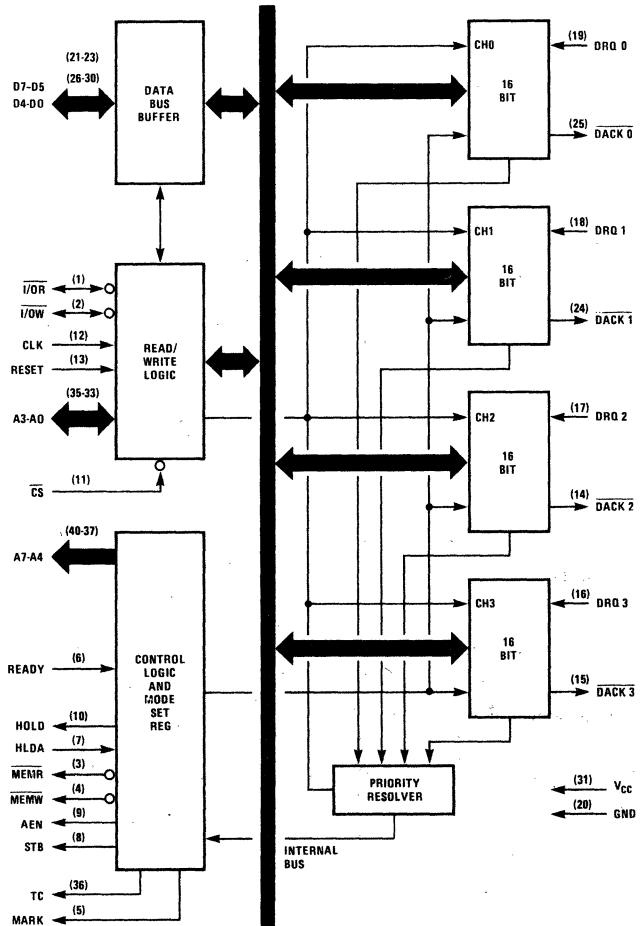




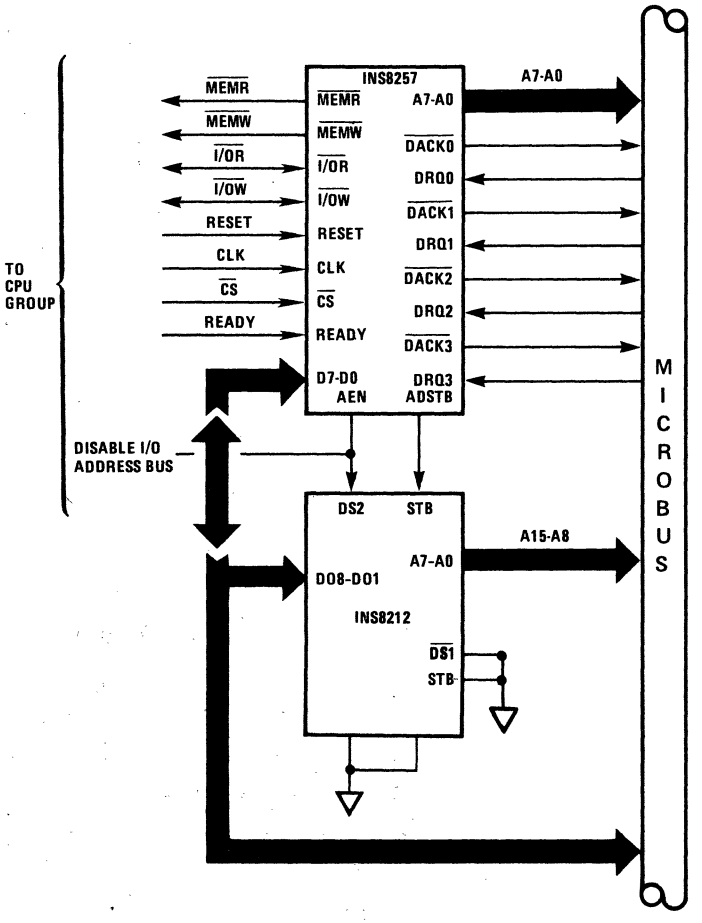
Internal Block Diagram

Typical MICROBUS Interface

Figure 3-23. INS82LS05 One-of-Eight Binary Decoder

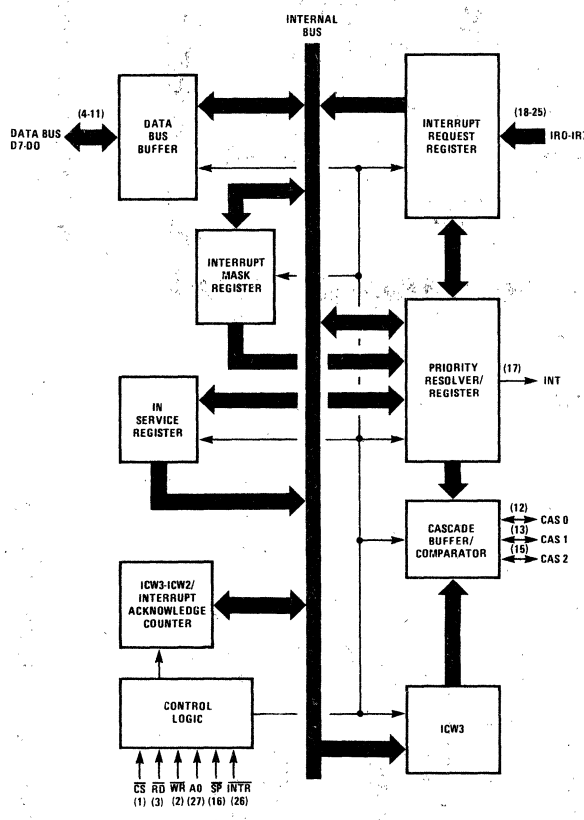


Internal Block Diagram

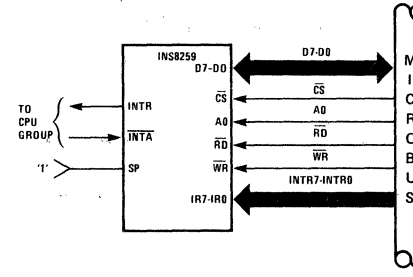


Typical MICROBUS Interface

Figure 3-24. INS8257 Programmable DMA Controller

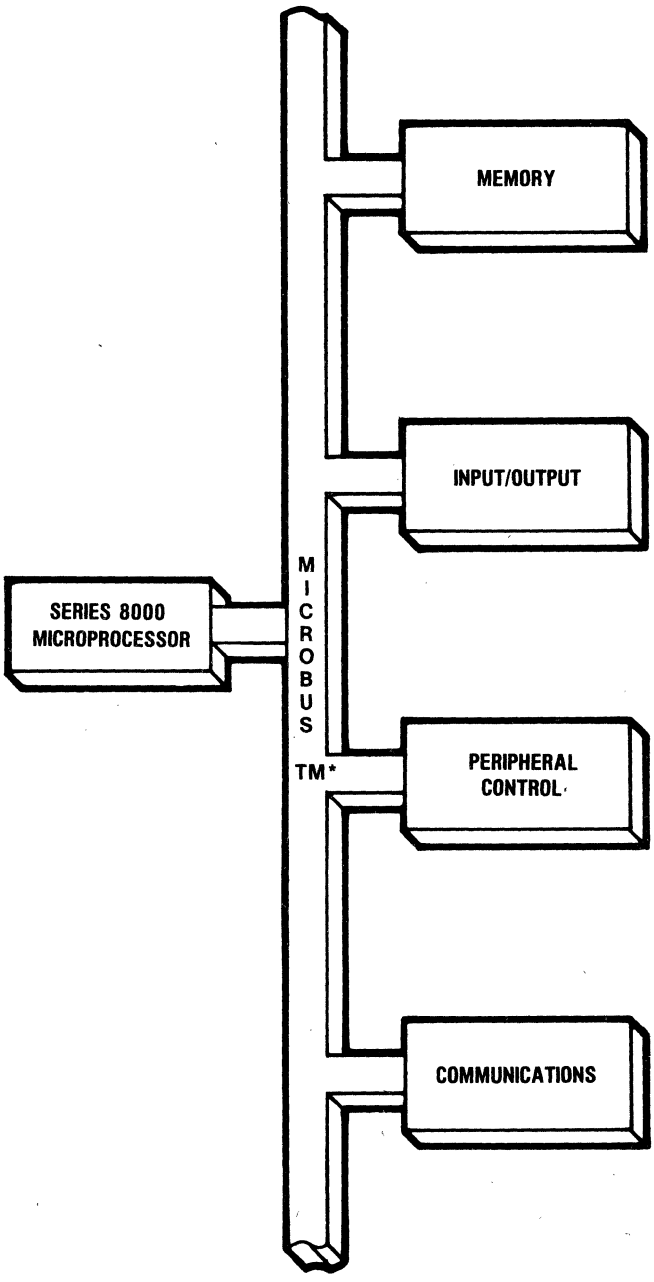


Internal Block Diagram



Single Device Configuration

Figure 3-25. INS8259 Programmable Interrupt Controller



Chapter 4

Designing Series 8000 Microprocessor Family Systems

* Trademark, National Semiconductor Corporation

Designing Series 8000 Microprocessor Family Systems

4.1 INTRODUCTION

This chapter provides detailed information to aid the system designer in the design of INS8080A microcomputer systems. Included in the chapter are the following: CPU group design, details on interfacing to memory and peripheral devices, techniques for expanding interrupts, and a method of implementing a simple control panel.

4.2 CPU GROUP DESIGN

The preferred design approach for the CPU group is to use the INS8080A Microprocessor with the INS8224 Clock Generator and Driver and the INS8228/INS8238 System Controller and Bus Driver as shown in figure 4-1. The use of this approach yields significant benefits in system timing and decreased component count. An alternative design approach, which uses standard TTL components and National Semiconductor general-purpose peripheral devices to implement the basic functions of circuits of the two supporting chips is described below. This design approach achieves operational characteristics that closely approximate those of the INS8224 and INS8228/INS8238 chips.

4.2.1 Clock Generator and Driver Design

Figure 4-2 shows the design of the Clock Generator and Driver using discrete components. The circuits generate two non-overlapping timing references (ϕ1 and ϕ2 clocks) for the internal storage elements and logic circuits of the INS8080A Microprocessor. (Refer to the INS8080A Data Sheet for the levels and timing relationships of the two reference clocks.) The circuits also provide auxiliary functions such as the synchronization of external requests and the generation of the status word strobe.

The Clock Generator comprises a 20-megahertz crystal-controlled oscillator, a 4-bit presettable binary counter, and associated gating circuits (two Exclusive-OR gates and three NAND gates). The oscillator provides a 20-megahertz TTL signal to the CLK input of the 4-bit counter, which is preset to a binary count of 3 by strapping the D_A and D_B inputs to V_{CC} supply (+5V) and the D_C and D_D inputs to ground. The resulting Q_A through Q_D outputs of the counter are then decoded by the standard TTL gates to provide proper timing for the ϕ1 and ϕ2 clock outputs. These TTL clock outputs are in turn capacitively coupled to the clock driver circuit.

The Clock Driver is a two-phase interface circuit that converts the TTL $\overline{\phi 1}$ and $\overline{\phi 2}$ clocks to MOS level ϕ1 and ϕ2 clocks. The MOS clocks have a voltage swing of from 0.6 to 11 volts, and rise and fall times typically less than 10 nanoseconds into a 20-picofarad capacitive load. To obtain the required output voltage swing, the clock driver is biased from the V_{BB} supply (−5V) and the V_{DD} supply (+12V) via a simple resistive divider. A low-resistance series network is included between each driver output and the INS8080A to eliminate any pulse overshoot.

The 20-megahertz oscillator also provides its TTL output to the CLK input of a D-type flip-flop of the Auxiliary Functions circuits. This flip-flop, in turn, generates an advanced timing signal (ϕ1A) that is used to clock two D-type flip-flops associated with the external WAIT and DMA REQUEST signals, thereby synchronizing the HOLD and READY signals to the INS8080A. The ϕ1A timing signal is also gated with the SYNC signal from the INS8080A to generate a low-level status strobe ($\overline{\text{STSTB}}$) output. This output can be used as the latching signal for the status word that is outputted onto the D_7-D_0 External Data Bus by the INS8080A at the first state of each machine cycle.

4.2.2 System Controller and Bus Driver Design

Figure 4-3 shows the design of the System Controller and Bus Driver using discrete components. The circuits generate the read and write control signals for memory and input/output devices, and provide buffering of the D_7-D_0 External Data Bus.

The System Controller comprises an eight-bit latch and associated gating circuits (four NAND gates and an inverter). The latch uses the status strobe ($\overline{\text{STSTB}}$), which occurs at the start of each machine cycle, as the latching signal to store the status word that is outputted onto the D_7-D_0 External Data Bus by the INS8080A. Four of the latch outputs (INTA, INP, MEMR, and OUT) then are gated with either the Data Bus In (DBIN) or Write ($\overline{\text{WR}}$) outputs of the INS8080A to generate the low-level read control signals ($\overline{\text{MEM R}}$, $\overline{\text{I/O R}}$, and $\overline{\text{INTA}}$) or low-level write control signals ($\overline{\text{MEM W}}$ and $\overline{\text{I/O W}}$), respectively.

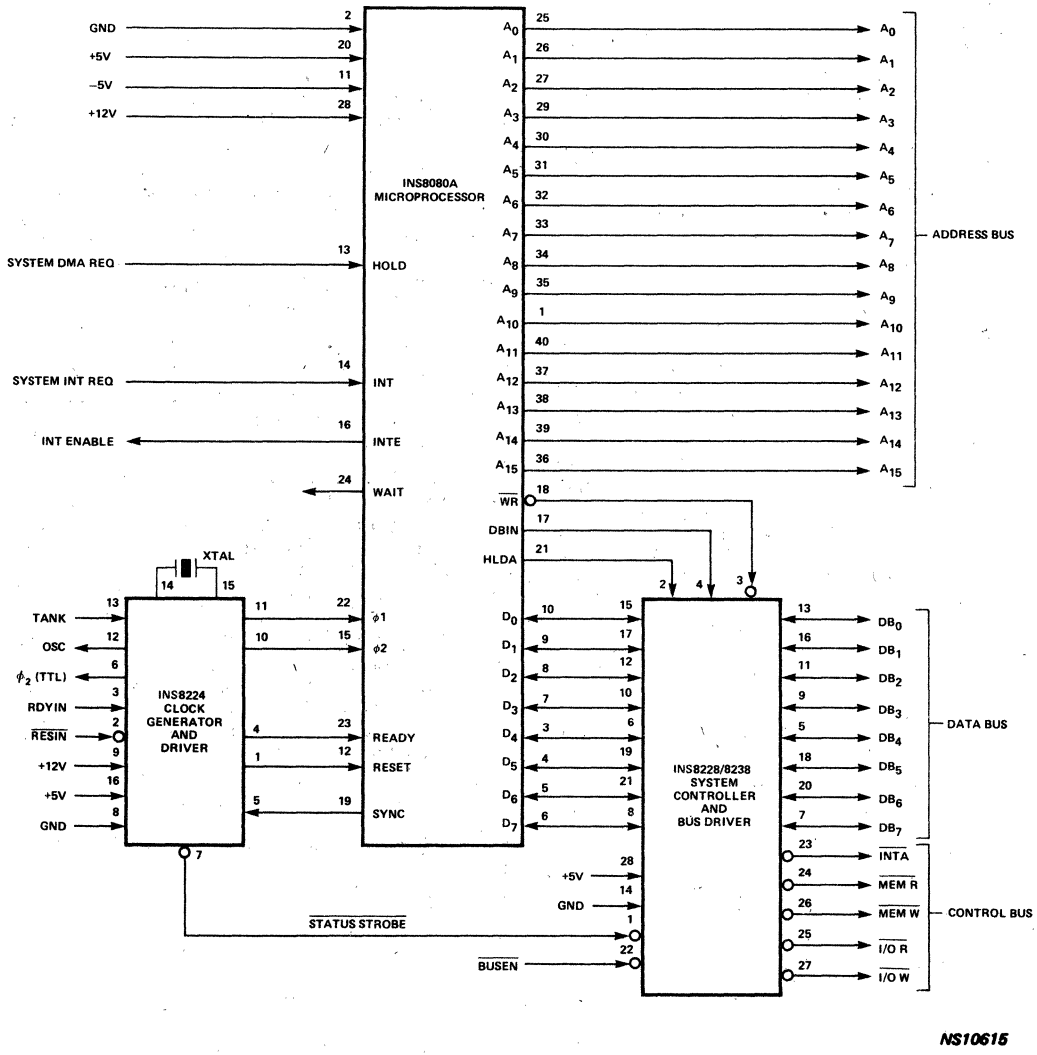


Figure 4-1. Preferred Method of CPU Group Implementation

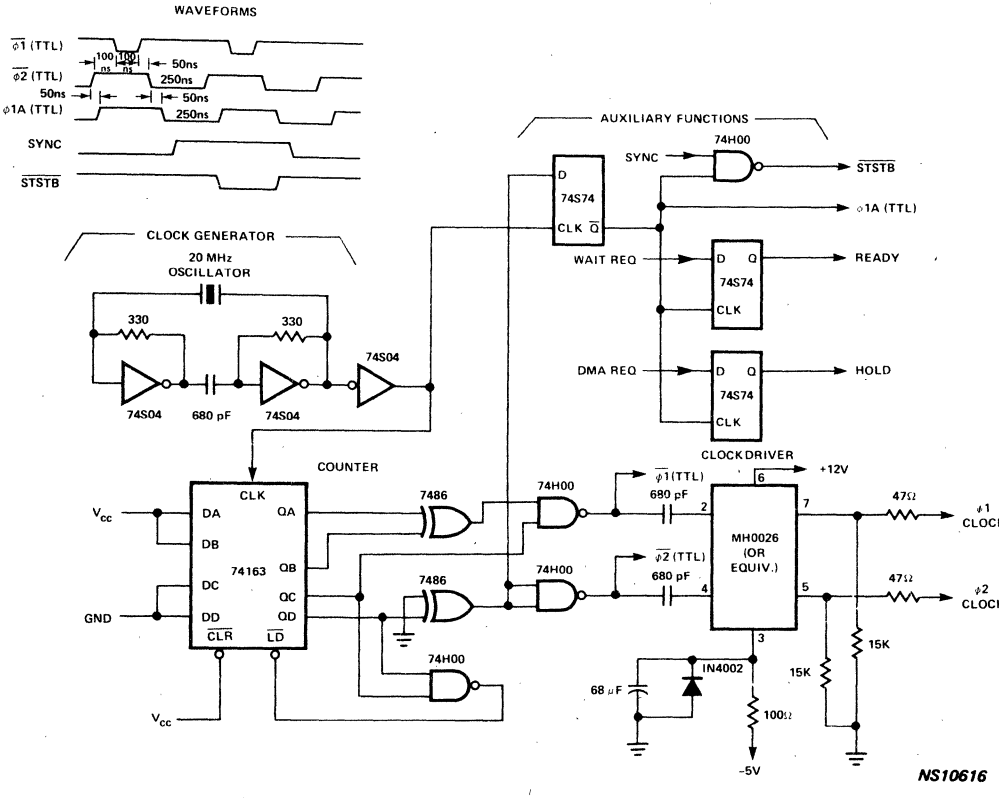


Figure 4-2. System Clock Generator and Driver Using Discrete Components

These control signals are directly interfaced to the memory and input/output devices.

The Bus Driver comprises two 4-bit, parallel bidirectional IC components that buffer the INS8080A D_7-D_0 External Data Bus from memory and input/output devices. The INS8080A data bus has an input requirement of 3.3 volts(minimum)and output drive capacity of 1.9 milliamperes (maximum). The bus driver ensures that these requirements are not only met but exceeded for enhanced noise immunity. In small systems with minimum memory and input/output requirements, buffering of the D_7-D_0 External Data Bus may not be required.

As shown in figure 4-3, the Direction Control ($\overline{DIEN}$) and Chip Select ($\overline{CS}$) inputs of the Bus Driver are connected to the DBIN output of the INS8080A and the system Bus Enable ($\overline{BUSEN}$), respectively. The DBIN signal ensures that the proper data flow is maintained on the data bus. The $\overline{BUSEN}$ is an asynchronous signal that allows other devices to gain access of the data bus during a DMA data transfer($\overline{BUSEN}$ = logic 1) by forcing the outputs of each 4-bit bidirectional IC of the bus driver to the high-impedance state.

4.3 ADDRESSING CONSIDERATIONS AND TECHNIQUES

The INS8080A has a 16-bit address bus that is capable of addressing up to 65K bytes of memory and up to 256 input and 256 output devices. In small systems with minimum memory and input/output requirements, buffering of the A_{15}-A_0 Address Bus may not be required. However, as memory and input/output device requirements increase, buffering is required for the bus. This address buffering function can be implemented by using two National Semiconductor INS8202 TRI-STATE Octal Buffers as shown in figure 4-4. Note that the system Bus Enable ($\overline{BUSEN}$) signal is connected to the buffers so that they are forced into their high-impedance state during a DMA data transfer ($\overline{BUSEN}$ = logic 1) or any other time that bus access is desired, thereby allowing other devices to gain access of the address

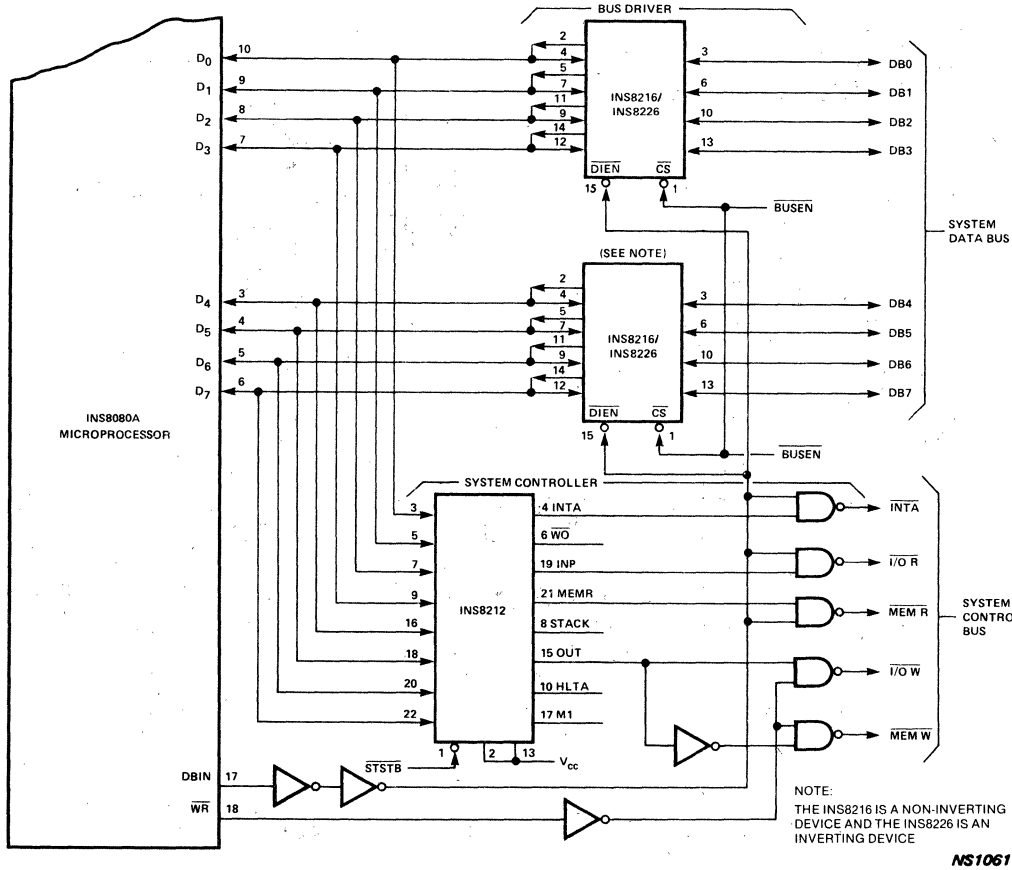


Figure 4-3. System Controller and Bus Driver Using Discrete Components

bus. As mentioned above, up to 65K bytes of memory and up to 256 input and 256 output devices can be directly addressed via the A_{15}-A_0 Address Bus of the INS8080A. The INS8080A microcomputer system can be configured so that memory and input/output devices are either treated separately (isolated input/output) or as a single memory array (memory mapped input/output) as described below. The mapping for the isolated input/output and memory mapped input/output addressing techniques is shown in figure 4-5. With both of these addressing techniques, the most common method of addressing memory or input/output devices is to decode some of the address bus bits as "chip selects" (using a device such as the National Semiconductor INS82LS05 to enable the addressed memory or the input/output device). The linear select method (refer to 4.5.1) is another way of addressing the input/output devices using either of the addressing techniques. In linear select, a singular address bus bit is assigned as the exclusive enable for a specified input/output device. Using this method limits the number of input/output devices that can be addressed but eliminates the need for extra decoders. In small system design, this is an important consideration.

When the INS8080A system is configured for isolated input/output addressing, the memory address space is separated from the input/output devices address space by using system control signals for the input/output architecture as shown in figure 4-6. Also, with isolated input/output addressing, the input/output devices communicate only with the Accumulator using the IN and OUT Instructions. Thus, since the memory address space is not affected by input/output device addressing, the full address space of 65K bytes is available for memory.

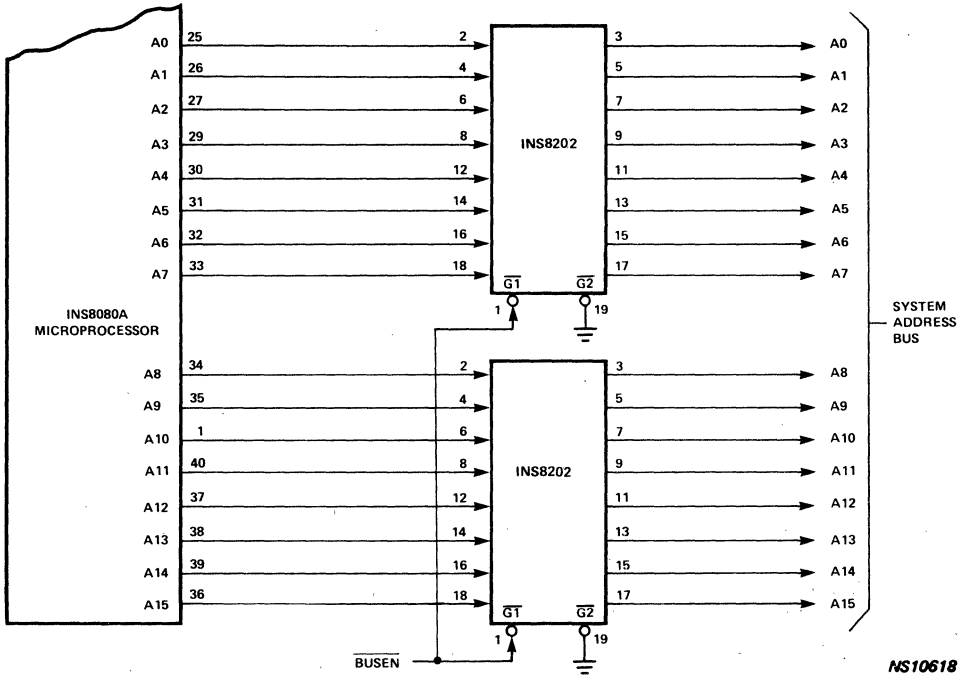


Figure 4-4. Address Buffer Design Using INS8202 Devices

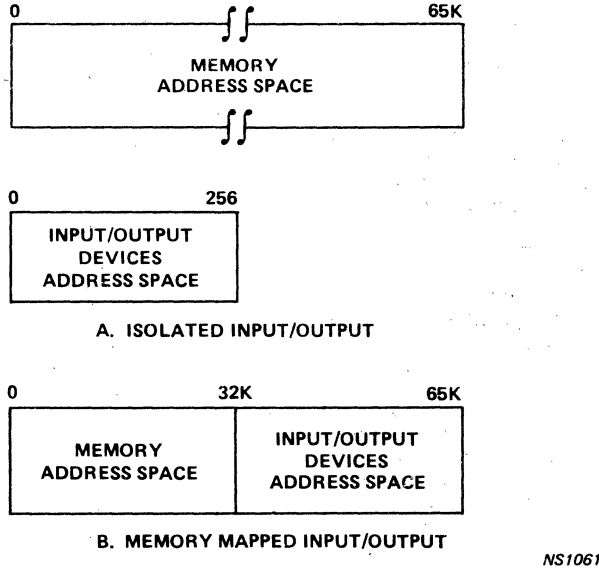


Figure 4-5. Mapping for Isolated Input/Output and Memory Mapped Input/Output Techniques

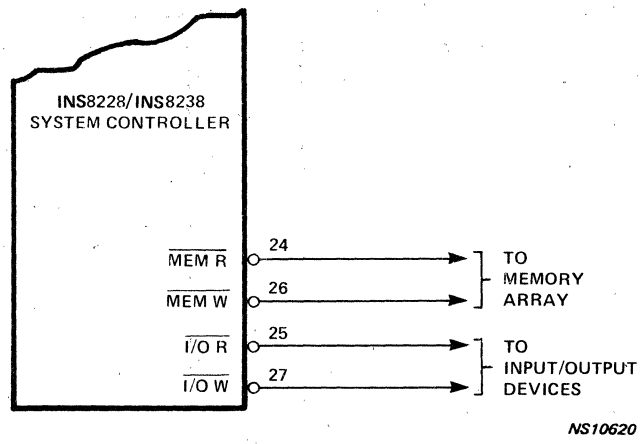


Figure 4-6. System Control Signals for Isolated Input/Output Addressing

When the INS8080A system is configured for memory mapped input/output addressing, an area of the memory array is assigned to the input/output devices by using system control signals for the input/output architecture as shown in figure 4-7. In this configuration, new input/output control signals ($\overline{I/O\ R}$ ($\overline{MM}$) and $\overline{I/O\ W}$ ($\overline{MM}$)) are generated by gating the $\overline{MEMR}$ and $\overline{MEMW}$ signals with most significant address bit A_{15}. (Since these new input/output signals connect in exactly the same manner as the corresponding signals of the isolated input/output configuration, the system bus characteristics are unaltered). Address bit A_{15} is used because it allows up to 32K bytes of memory addressing, and because it is easier to control with software. However, any other address bit may be used for this gating function. When bit A_{15} is low, the memory address space is active and when bit A_{15} is high, the input/output devices address space is active.

With memory mapped input/output addressing, all of the instructions that can be used to manipulate memory locations (for example, MOV M, r; LDA; STA; LHLD; et cetera) can also be used for the input/output devices. These devices are still considered addressed "PORTS" but instead of the Accumulator being the only data transfer medium for the peripherals, any of the internal registers of the INS8080A can also be used for this purpose. Thus, memory mapped input/output addressing is suited for small systems that require high throughput and have less than 32K bytes of memory.

4.4 INTERFACING TO MEMORY

The CPU group of the INS8080A microprocessor family interfaces with standard semiconductor memory components (and input/output devices) via the MICROBUS. A typical interface to a memory array having 6K bytes of ROM storage and 512 bytes of RAM storage is shown in figure 4-8. This typical memory interface is suitable for almost any size of memory array.However, in larger systems, buffers may be required for driving the three buses and decoders may be required for generating the chip select signals for the memory array (and input/output devices).

As shown in figure 4-8, the interfacing to the three National Semiconductor INS8316 ROMs is quite straightforward. The D_0-D_7output lines of the ROMs are connected to the bidirectional Data Bus; the A_0-A_{10} address inputs are connected to corresponding bits of the Address Bus; the CS2 and CS3 chip select inputs are connected to the A_{11} and A_{12} bits (most significant) of the Address Bus; and the CS1 chip select input of the ROMs is connected to the inverted $\overline{MEM\ R}$ signal of the Control Bus. During a FETCH or MEMORY READ machine cycle, the CPU group may output an address in the ROM address space of the memory array. When this occurs, the data stored at the addressed ROM location are then gated onto the External Data Bus with the $\overline{MEM\ R}$ signal. In this way, data are read from the ROMs in the INS8080A microprocessor system.

The interfacing to the four National Semiconductor INS8111A-4 static RAMs is also straightforward. The I/O_1-I/O_4 common input/output lines of the RAMs are connected to corresponding bits of the bidirectional Data Bus; the A_0-A_7 address bits are connected to corresponding bits of the Address Bus; and the R/W and OD in-

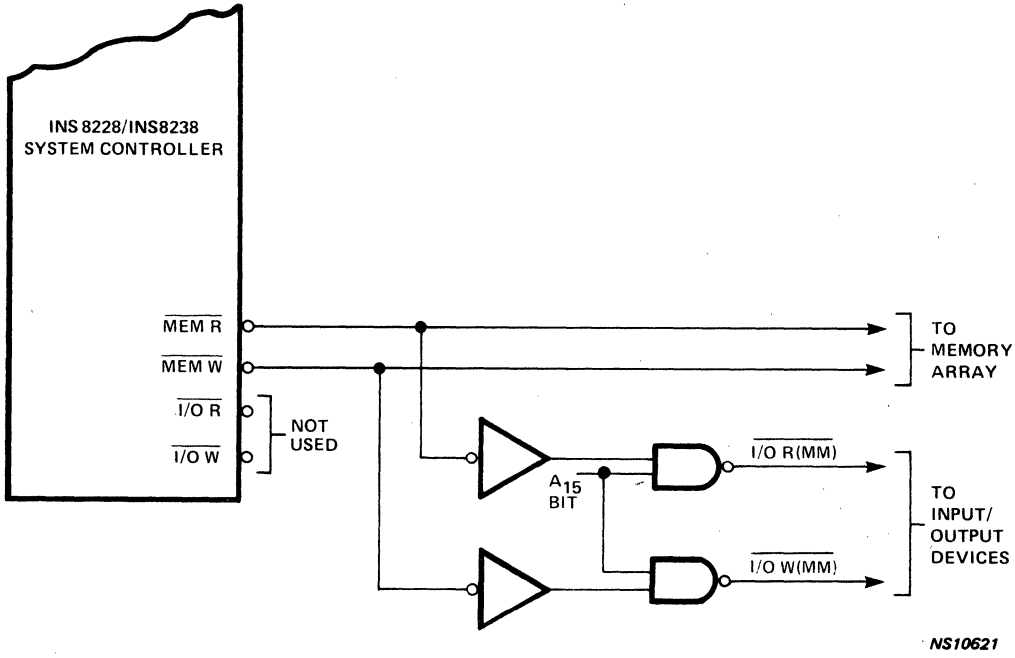


Figure 4-7. System Control Signals for Memory Mapped Input/Output Addressing

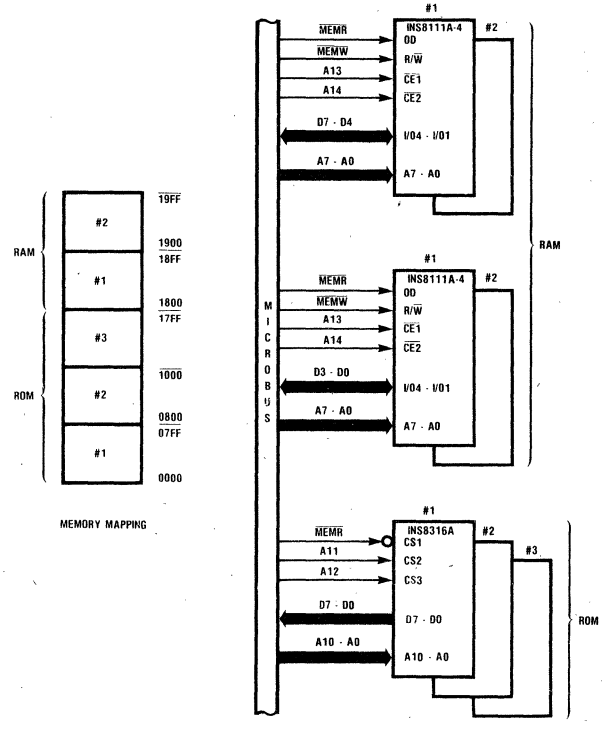


Figure 4-8. Typical Memory Interface

puts of the RAMs are connected to the $\overline{\text{MEM W}}$ and $\overline{\text{MEM R}}$ (or DBIN) signals, respectively, of the Control Bus. During a FETCH, MEMORY READ, or STACK READ machine cycle, the CPU group reads data from the RAMs in exactly the same manner as described above for the ROMs. During a MEMORY WRITE or STACK WRITE machine cycle, the CPU group outputs an address in the RAM address space of the memory array. When this occurs, the data to be written into memory are then strobed into the addressed RAM location with a low-level $\overline{\text{MEM W}}$ signal. In these ways, data are read from and written into RAMs in the INS8080A microprocessor system.

The memory array of figure 4-8 includes ROMs (INS8316A) and RAMs (INS8111A-4) that have an access time of 450 nanoseconds (maximum). When the INS8080A microprocessor is operated from a clock generator with a tCY of 500 nanoseconds, the required memory access time is from 450 to 550 nanoseconds. Therefore, when slower memory components are used in the system, the INS8080A Microprocessor must contain a synchronization provision to allow the memory components to request the wait state (T_W). (The actual number of T_W states to be inserted is determined by external logic that is user designed.) This provision can be implemented for any slow memory (RAM or ROM) by a simple logic control of the READY input of the INS8080A as follows. When the addressed slower memory receives a $\overline{\text{MEM R}}$ or $\overline{\text{MEM W}}$ signal, it places a low-level on the READY line of the microprocessor, causing the INS8080A to enter the WAIT sequence (refer to 3.2.2.2). After the slower memory has had time to respond, it places a high-level on the READY line, thereby allowing completion of the instruction cycle.

4.5 DYNAMIC MEMORY

4.5.1 Introduction

Many new memory system designs are using dynamic RAMs, particularly in large memory systems due to the availability of 16K RAM chips.

The key to success in a dynamic RAM system, or any other system for that matter, is margin. A system designed to maximize power supply and timing margins will be reliable and easy to manufacture.

In this section we shall discuss RAM chip characteristics, power supply and control signal distribution on PC boards, and control logic implementation suggestions.

4.5.2 Ram Chip Characteristics

For reference we shall compare dynamic and static RAMs at the chip level. Then we shall describe the unique characteristics of dynamic RAMs which must be considered in a memory system design.

Dynamic RAMs versus Static RAMs

The basic difference between dynamic and static RAMs is the way they store data. The static RAM uses a flip-flop to store a bit, while the dynamic RAM uses a capacitor to store a bit. (See figure 4-9.)

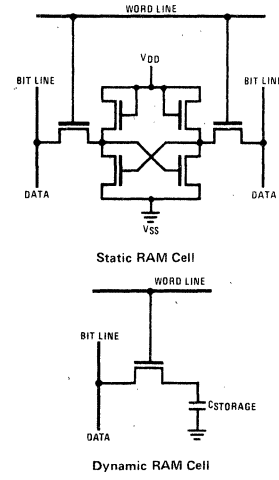


Figure 4-9. Cell Comparison

It is their respective cell designs that give each RAM its advantages over the other. Let's compare the RAMs for ease of use, power dissipation, die size, and price.

Ease of Use: The static RAM is easier to use because no refresh logic is required. In addition, static RAM control signals tend to be easier to generate because cycling is usually unnecessary.

Power Dissipation: The dynamic RAM draws less power. The static RAM draws power continuously to sustain its flip-flops, while the dynamic RAM draws minimal power (1 to 2mA) between cycles. With continuous cycling, the dynamic RAM draws about as much power as the static. However, in a large memory system, dynamic RAMs save total system power since only one bank of RAMs is ever accessed during a memory cycle. All other banks draw minimal current except during refresh cycles. The duty cycle for refresh is approximately 1½ to 3%.

Die Size: Dynamic RAMs tend to be smaller. Due to the difference in cell designs, the die size of the dynamic RAM is often at least 20% smaller than that of a comparable static RAM from the same manufacturer.

Price: Because of smaller die sizes and much larger production runs, dynamic RAMs should always remain considerably cheaper than comparable static RAMs. In addition, dynamic RAMs save money in larger systems. Less chip power means smaller and cheaper power supplies. Smaller supplies mean a further saving in reduced cooling requirements. In general, the larger the memory system, the greater the savings by using dynamics.

Dynamic RAMs

Refresh: Since charge leaks off the storage capacitors, it must be replenished periodically in order for a dynamic RAM chip to retain its data. The charge in any one cell is replenished, or refreshed, every time that cell is accessed for a read or a write. At the same time, all the other cells in the same row are also refreshed. For that reason the entire RAM chip can be refreshed by doing only 64 cycles for 4K RAM, (a 16K RAM needs 128 cycles) in 2ms while sequencing through all the row addresses. The bit pattern presented to the column addresses does not matter. However, the setup and hold times must still be met. Unstable column addresses during refresh will cause data loss.

The hardware required for refresh amounts to a 6 or 7-bit counter for the refresh addresses, some way to multiplex the counter onto the RAM row address lines, a timer to signal when a refresh should be done, and the miscellaneous gating needed to couple into the usual read/write logic.

In some systems no extra refresh logic is needed: For example, in CRT systems normal operation sequences through all the row addresses in less than a 2ms refresh period. This will be true only if the row address bits on the RAM chip are driven from the least significant address bits of the system. As a rule, this is good practice in all systems. By placing the most active system address bits on the RAM row addresses, normal system operation will automatically refresh the bulk of the RAM.

Cycling: One of the key functional differences between static and dynamic RAMs is the fact that dynamic RAMs must run through a cycle in order to read or write. Aborting the cycle by removing the chip enable too early or by trying to start a second cycle too soon after the first will probably cause data loss. Minimum chip enable on and off times must be observed.

Summary

Static RAMs are easier to use. Dynamic RAMs are cheaper, use less power, must be refreshed, and must be cycled.

4.5.3 Memory Subsystem Design Considerations

Some memory board designs are easy to manufacture, while others, functionally identical, have low manufacturing yields seemingly due to the many "bad" chips. The difference between them is usually the amount of margin designed into each system. Power supply and timing margins are both critical, and as the margins go to zero or negative, the amount of "soft" errors goes up. (A chip has a "hard" error if a location consistently cannot be written and read back properly. It has a "soft" error if it only occasionally fails.)

On careful analysis, "soft" errors usually occur during a memory cycle in which some system parameter has gone out of spec. Since the RAM chips themselves have variations in their margins, replacing the offending RAM with one that has a greater margin in the out-of-spec parameter seems to cure the problem. This results in a large pile of "bad" RAMs. However, the real solution to this type of problem is in a careful system design and board layout in the beginning.

Power Distribution

By far the single most important aspect of a successful RAM system is good power distribution consisting of carefully designed decoupling and power gridding. The importance of good power distribution cannot be overemphasized.

Figure 4-10 shows CE, I_{DD} current waveform for a typical dynamic RAM chip during a memory cycle.

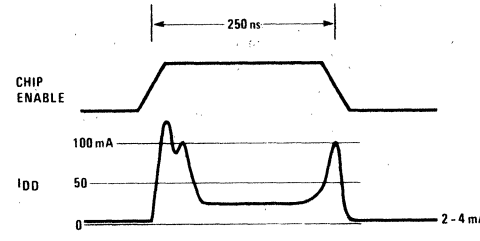


Figure 4-10. I_{DD} Current Waveform

At the beginning and end of chip enable, each RAM chip draws 50 to 100mA current spikes with rise times of 20ns. In additon, each RAM package draws a 20 to 40mA DC current lasting for the duration of chip enable. The power distribution system must supply these currents while the voltages at the RAMs remain constant. If there are a number of rows of RAMs, all power supply traces to all RAMs should be run both vertically and horizontally throughout the array. Providing multiple paths through the array reduces the effective inductance of the power distribution system.

Power Distribution Rules:

1. It is the single most important aspect of a good RAM board layout.
2. Use plenty of decoupling. The decoupling caps not only reduce voltage spikes, but also provide most of the RAM power during the cycling. Lay out the board for a 0.1μF capacitor per power supply per RAM chip (up to three capacitors per chip). As production history accumulates, it may be possible to omit half the capacitors. However, lay out the board for one per supply per chip. Use 50 to 200μF of bulk decoupling +12V. On +5V and −5V use 20 to 100μF.
3. The decoupling capacitors should have the shortest possible traces back to their respective RAM power supply and ground pins. To reduce inductance further, these traces should be as wide as room will allow.
4. Traces running the power supply voltages throughout the array should be as wide as possible. However, with good decoupling design, even minimum trace widths will probably be acceptable. If some power supply traces can be wider than others, make V_{SS} (Ground) wider first, V_{DD} next, V_{BB} next, and finally V_{CC}. Ground is the key. Grid the supplies even if the traces are heavy in one direction and light in the other.
5. Multilayer boards tend to simplify power distribution problems, but the types of problems that must be solved are the same. Only the magnitudes have been somewhat reduced. Almost everything that has been said up to now is still applicable to multilayer boards.

Data and Control Signal Distribution

The second most important aspect of the successful RAM system is address, data, and control signal distribution.

Let's discuss the chip enables first. This is the most important signal to the RAM and all timing is referenced to it. There are two types of chip enables in common use today: 12 volt and TTL level swings.

First, place the actual driver chip near the RAM array it is driving, making the chip enable run short and direct. Second, put a damping resistor near the driver. Do this for either TTL level or 12 volt chip enables. Select the value of this resistor to give the best clock waveform at the RAM chips. Its value will probably be between 10 and 51Ω. Figure 4-11 shows the commonly used arrangements.

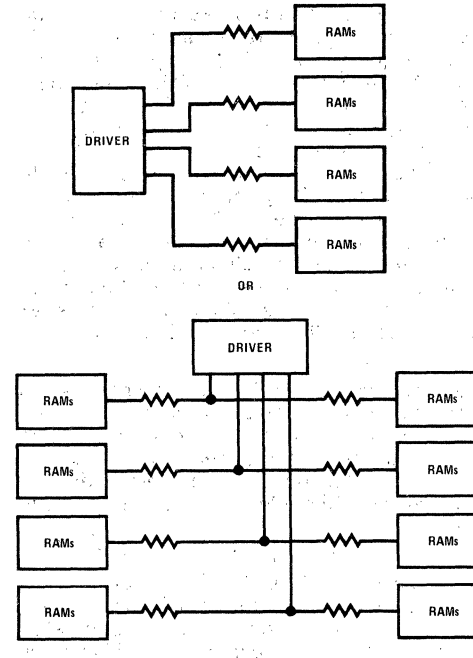


Figure 4-11. Damping Resistor Placement

The reasons for these two recommendations stem from the fact that, at the frequencies encountered here, the clock lines are, in fact, transmission lines.

Long clock lines can cause ringing because the open circuit at the far end of the line causes the reflection from the end of the line to return to the driver after the end of the rise time.

In long unloaded clock lines the reflection from the junction of the unloaded and loaded sections of the line (due to the mismatch) cause glitches in the clock transitions.

To minimize crosstalk from chip enable to other signals, try to run chip enable at 90° to other signals. This is usually hard to do in an actual layout. As an alternative, leave as much room as possible between chip enable and adjacent traces as it runs through the array. Typically, signals in the array are on 50 mil centers. Moving the two adjacent signals more than 50 mils away from chip enable will help some in reducing crosstalk. However, as stated earlier, there seem to be very few problems associated with chip enable. Neither CE itself nor crosstalk to other signals will be troublesome if the above guidelines are observed.

Address, data, and control signals such as read/write (or equivalent) should be run as directly as possible. Their layouts tend to be non-critical. The critical thing is timing. The control logic should be designed to maximize setup and hold times with respect to chip enable. Again, high production yield is related to margins. As an example, consider a RAM board that was built for an 8080 system. The chip used was MM5271 4K RAM which has a low true TTL level clock input. The signal that controls read, write, and refresh is called TSP. When doing a refresh, TSP must be low at the beginning of chip enable. Although the MM5271 data sheet says that the setup time for TSP is zero ns with respect to the leading edge of chip enable, about 50ns of setup time gives extra margin to avoid error.

In high-speed systems where it is hard to design in extra margin, use damping resistors in address, data, and control lines to help control their waveshapes. A resistor in every address, data, and control line allows these waveforms to be optimized, which gives the system improved margin over an undamped design. Use damping resistors only where necessary. Leave them out of signals that have time to settle down before they are needed.

Summarizing the use of damping resistors: always put them in chip enable lines, whether they are TTL levels or 12V levels. Use them as necessary in those address, data, and control lines whose timings are approaching the limits of the RAM chip data sheet. Design in margin first. Tune it in when it can't be designed in.

Most microprocessors have predictable periods of time when they will not access the RAM board. Usually it takes little effort to insert refresh cycles in these times, thereby making refresh transparent to the CPU. When the CPU is very fast and is using the bus almost continuously, the refresh will have to hold up the processor. Even then, some clever design will minimize the time spent doing non-transparent refresh.

4.5.4 Summary

Refresh requirements make dynamic RAMs slightly harder to use than static RAMs. However, they pay the designer back for his efforts by reducing overall system cost in three ways. First, dynamic RAMs tend to be cheaper than static RAMs of the same size. This is primarily due to smaller chip sizes and higher production volumes than comparable static RAMs. Second, dynamic RAMs use less power. When a dynamic RAM is not being accessed it draws much less current than a static RAM. During access, dynamic and static RAMs draw similar amounts of power. However, in a large array, only that bank being accessed draws full power. All others still draw standby currents so that the total system power is lower than for a comparable static system. Because of the reduced power requirements, power supplies are cheaper. And, third, due to lower power dissipation, cooling requirements are reduced, allowing a further saving.

There are three things the system designer can do to maximize RAM board yields during manufacture. First, design proper power supply decoupling. This is probably the single most important consideration for the designer. A good high frequency 0.1μF capacitor per supply per memory chip is recommended. A capacitor per supply per two chips is probably okay, but the board should be laid out for one capacitor per supply per chip and then capacitors can be left out as yield data become available. For bulk decoupling use about 50 to 200μF per board on +12V, less on +5V and −5V.

Second, design in as much margin as possible in all control signal timing. Use damping resistors where necessary. If timing is designed right to the minimum specs, periodically the right combination of data pattern, power supply noise, temperature, cosmic radiation, etc., causes the system to fail. The combined worst case parameters push a signal beyond specification and the memory fails.

Third, never allow spurious, shortened memory cycles to occur. Shortened or aborted memory cycles are guaranteed to destroy all the data in the row that was addressed during the aborted cycle.

Any designer who uses reasonable care can successfully design dynamic memory systems which will be easy to manufacture and very reliable in the field.

For a full discussion - refer to:
"Dynamic RAM Board Design Made Easy," by Stephen Calebotta, National Semiconductor, Memory Application, November 1977.

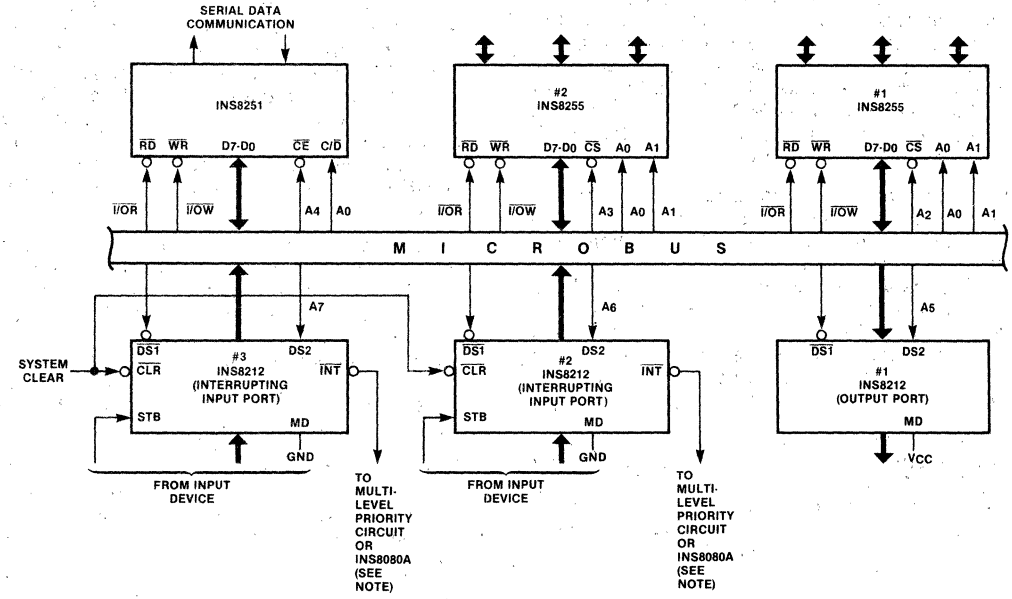
4.6 INTERFACING TO INPUT/OUTPUT DEVICES

The input/output devices use the same 3-bus

architecture for interfacing to the CPU group as the semiconductor memory components. A typical input/output interface is shown in figure 4-12. This interface enables the INS8080A Microprocessor to communicate with peripheral devices or structures such as keyboards, paper tape, floppy disks, printers, displays, data communication interfaces, sensors, relays and motor controls as described in the following paragraphs.

4.6.1 Input/Output Addressing

Depending on the system input/output environment, the input/output devices of the typical interface (figure 4-12) may be addressed using either the isolated input/output or memory mapped input/output technique and linear select.Thus, no decoders are required for generating chip select signals and each device has an exclusive enable bit. Figure 4-13 shows an example of how to address six National Semiconductor INS8255 Programmable Peripheral Interface devices using the isolated input/output addressing technique and linear select. In this example, the addressing format shown is the second byte of an IN or an OUT Instruction.Similarly, figure 4-14 shows an example of how to address 13 INS8255 devices using the memory mapped input/output addressing technique and linear select. In this example, the addressing format shown could be second and third bytes of any memory reference instruction that is used for the input/output devices (for example, MVI M, LDA, STA, SHLD, ADD M, ANA M, et cetera).



NOTE: IF ONLY ONE INS8212 INTERRUPTING INPUT DEVICE IS USED, THE $\overline{INT}$ SIGNAL SHOULD BE CONNECTED TO THE INT PINOUT OF THE INS8080A VIA AN INVERTER. IN THIS WAY, A USER SELECTED SINGLE LEVEL INTERRUPT (RST 7) IS GATED ONTO THE INS8080A DATA BUS WITH A HIGH-LEVEL DBIN SIGNAL, WHEN THE INTERRUPT REQUEST IS ACKNOWLEDGED.

Figure 4-12. Typical Input/Output Interface

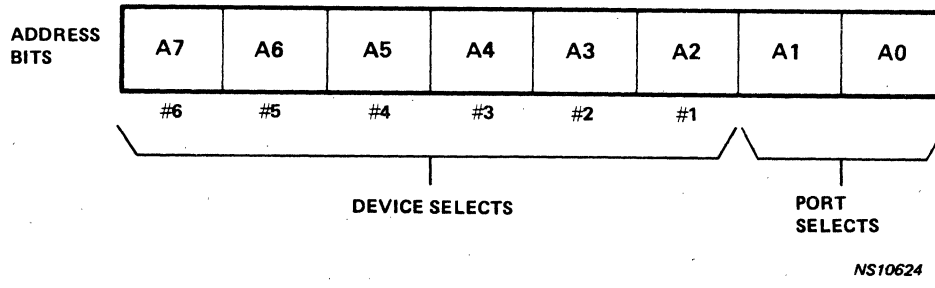


Figure 4-13. Example of Addressing INS8255 Devices Using Isolated Input/Output Technique and Linear Select

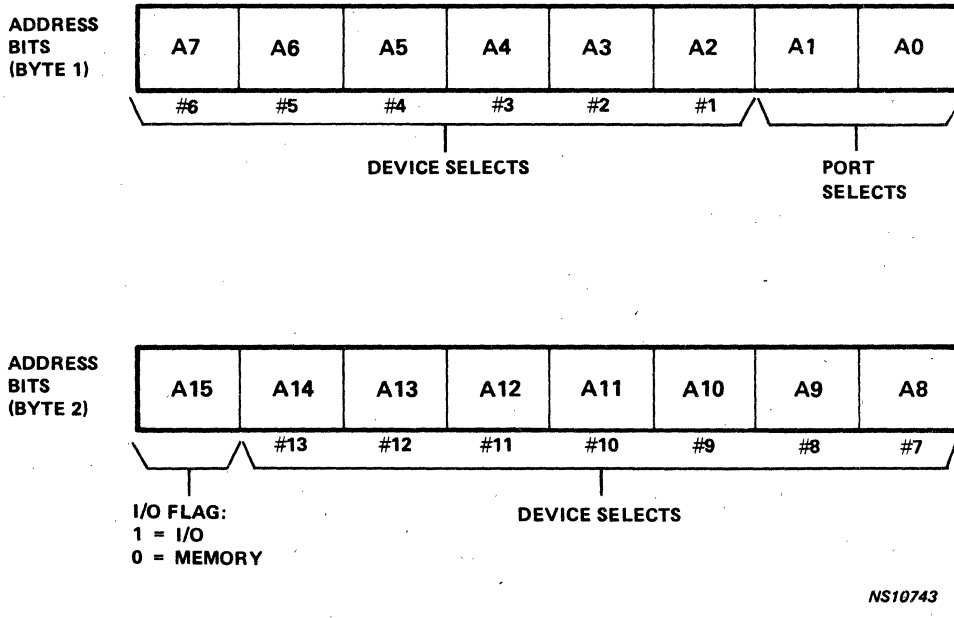


Figure 4-14. Example of Addressing INS8255 Devices Using Memory Mapped Input/Output Technique and Linear Select

4.6.2 Interfacing 8-Bit Peripherals

As shown in the typical input/output interface of figure 4-12, two National Semiconductor INS8255 Programmable Peripheral Interface devices and three National Semiconductor INS8212 Input/Output Port devices are provided for interfacing 8-bit peripherals (keyboards, sensors, paper tape, displays, et cetera) to the system. Since each INS8255 has three ports, up to 24 bits of programmable input/output data and control signals are provided by each device. Note that the $\overline{I/O\ W}$ and $\overline{I/O\ R}$ signals from the Control Bus are used as write and read command signals for the transfer of data (D_7-D_0) to and from the INS8255 devices. Also, note that the $\overline{I/O\ W}$ signal is used in conjunction with the A_5 address bit to select the INS8212 device that functions as an output port; and that the $\overline{I/O\ R}$ signal is used in conjunction with either the A_6 or the A_7 address bit to select one of two INS8212 devices that function as interrupting input ports. The addressing formats for the INS8255 and INS8212 devices are shown in figure 4-15.

4.6.3 Interfacing Serial Devices

As shown in the typical interface of figure 4-12, one National Semiconductor INS8251 Programmable Communication Interface device is provided for interfacing serial data devices (MODEMs, communications links, et cetera) to the system. Note that the $\overline{I/O\ W}$ and $\overline{I/O\ R}$ signals are also used as write and read command signals for the transfer of data to and from the INS8251 device. The addressing format for the INS8251 is shown in figure 4-16.

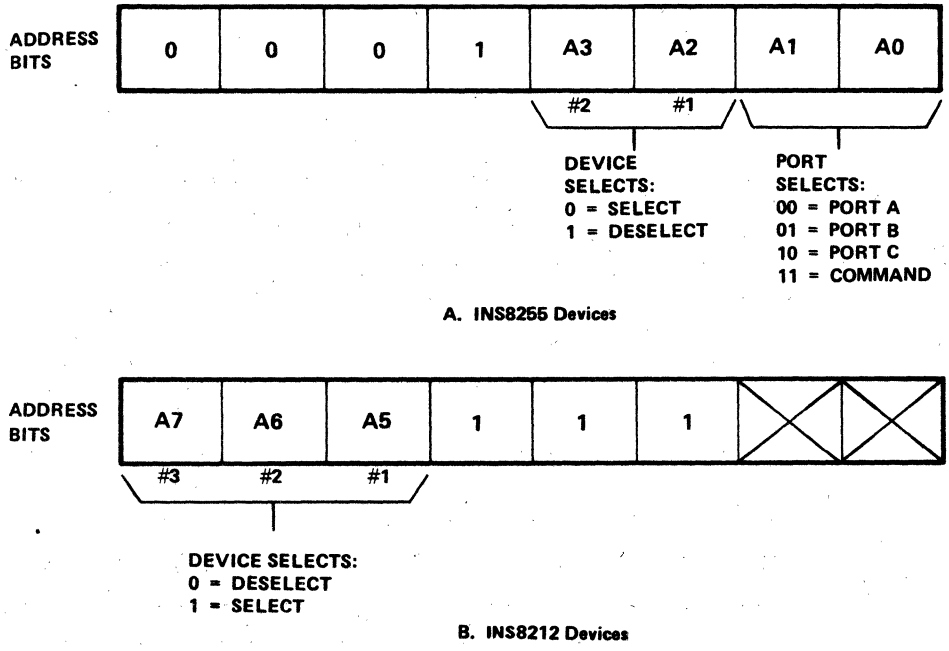


Figure 4-15. Addressing Format for INS8255 and INS8212 Devices

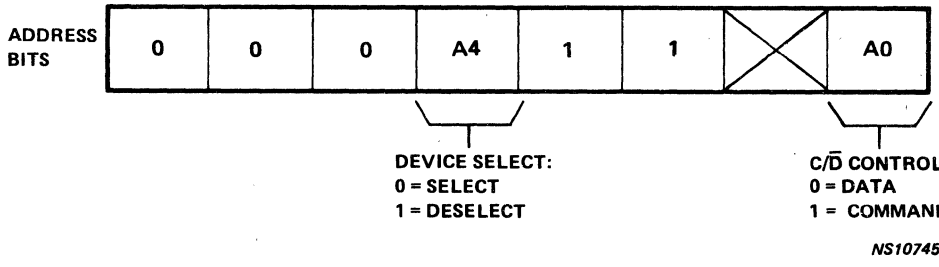


Figure 4-16. Addressing Format for INS8251 Device

4.7 EXPANDING INTERRUPTS

For many applications the single interrupt provided by the INS8080A is insufficient. The INS8259 provides a multi-level priority-encoded interrupt controller for the 8080A CPU group.

The INS8259 is a programmable interrupt controller containing eight priority-encoded vectored interrupts, cascadable to create up to 64 priority-encoded vectored interrupts without any additional circuitry. Operation of the device is static, requires no clocks, and is programmable via the system software allowing the programmer complete control over system operation at all times. There are a number of operational modes, permitting optimization for diverse system requirements.

Interrupts to the controller are via interrupt inputs IR7-IR0, and are stored in the Interrupt Request Register while the In-Service Register stores all interrupt levels currently being serviced. The Priority Resolver Register determines the priority of the interrupts stored in the Interrupt Request Register and controls the sequence in which they are loaded into the In-Service Register. The sequence in which the interrupt priorities are stored can be controlled via software allowing the interrupt priorities to be rearranged as desired by the programmer.

The INS8259 can also be cascaded with up to eight other devices to create 64 vectored interrupts. In such applications, one device is the 'master' and the others are the 'slaves'. The 'master' will store the identification of all other devices in the interrupt structure thus allowing the 'master' to maintain the appropriate priority encoding.

The INS8259, connected to the MICROBUS to implement the system interrupt controller is illustrated in figure 4-17.

Refer to Figure 2-8 INS8080 Family CPU Group to MICROBUS Configuration. The INS8259 shown is for the single configuration. See Figure 4-18 for method of Expanding up to 64 interrupts. For proper ordering of interrupts start assigning of connections to master interrupt #7. Assign interrupt request 0 only after all of the other positions are used.

4.8 USE OF INS8080A SUPPORT CHIPS

This section provides detailed information on the N8080 family support chips for the INS8080A Microprocessor. Parametric information for the support chips is contained in the related data sheets.

The INS8080A and its two CPU Group support devices, the INS8224 and the INS8228/INS8238, constitute the minimum components to implement the MICROBUS. The minimum CPU Group is sufficient for implementing a minimal system with only a linear select addressing capability.

An illustration of a minimal CPU Group is shown in figure 4-1.

For descriptions of the devices required to expand the minimal CPU Group into one with an expanded capability, refer to the sections listed below.

- Expanded chip selects (see section 4.4)
- Interrupt expansion (see section 4.7)
- Address expansion (see section 4.3)

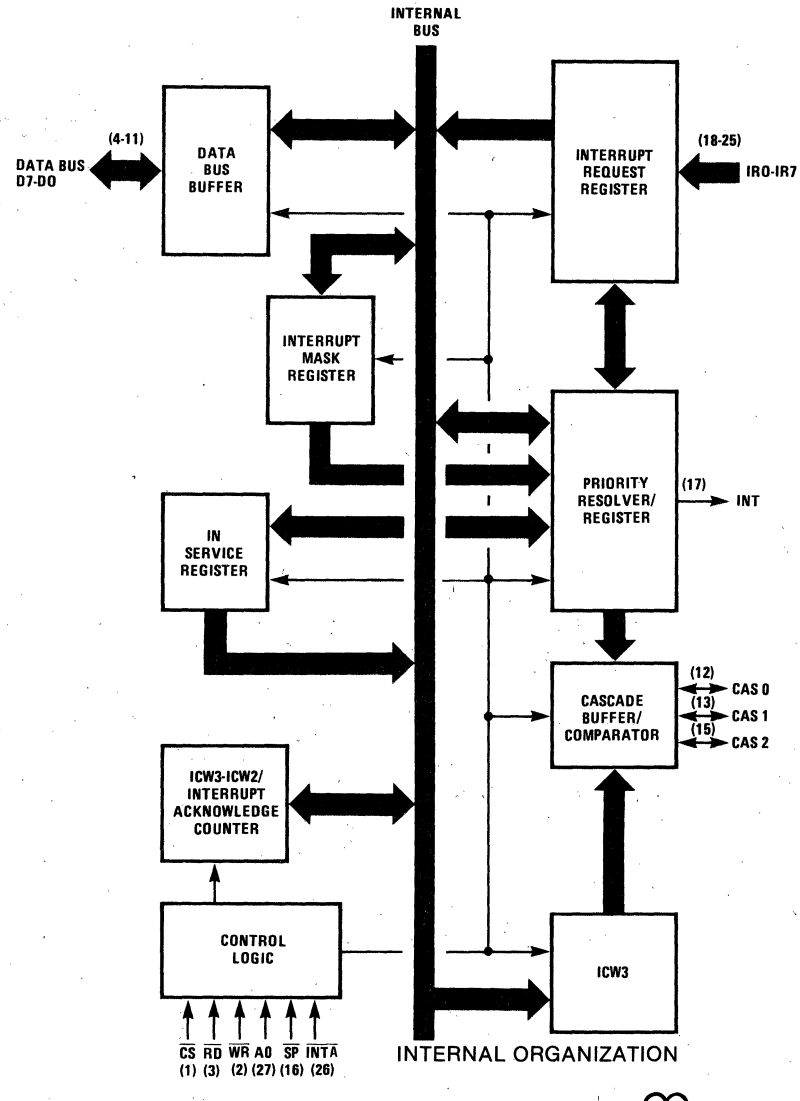


Figure 4-17. INS8259 Programmable Interrupt Controller

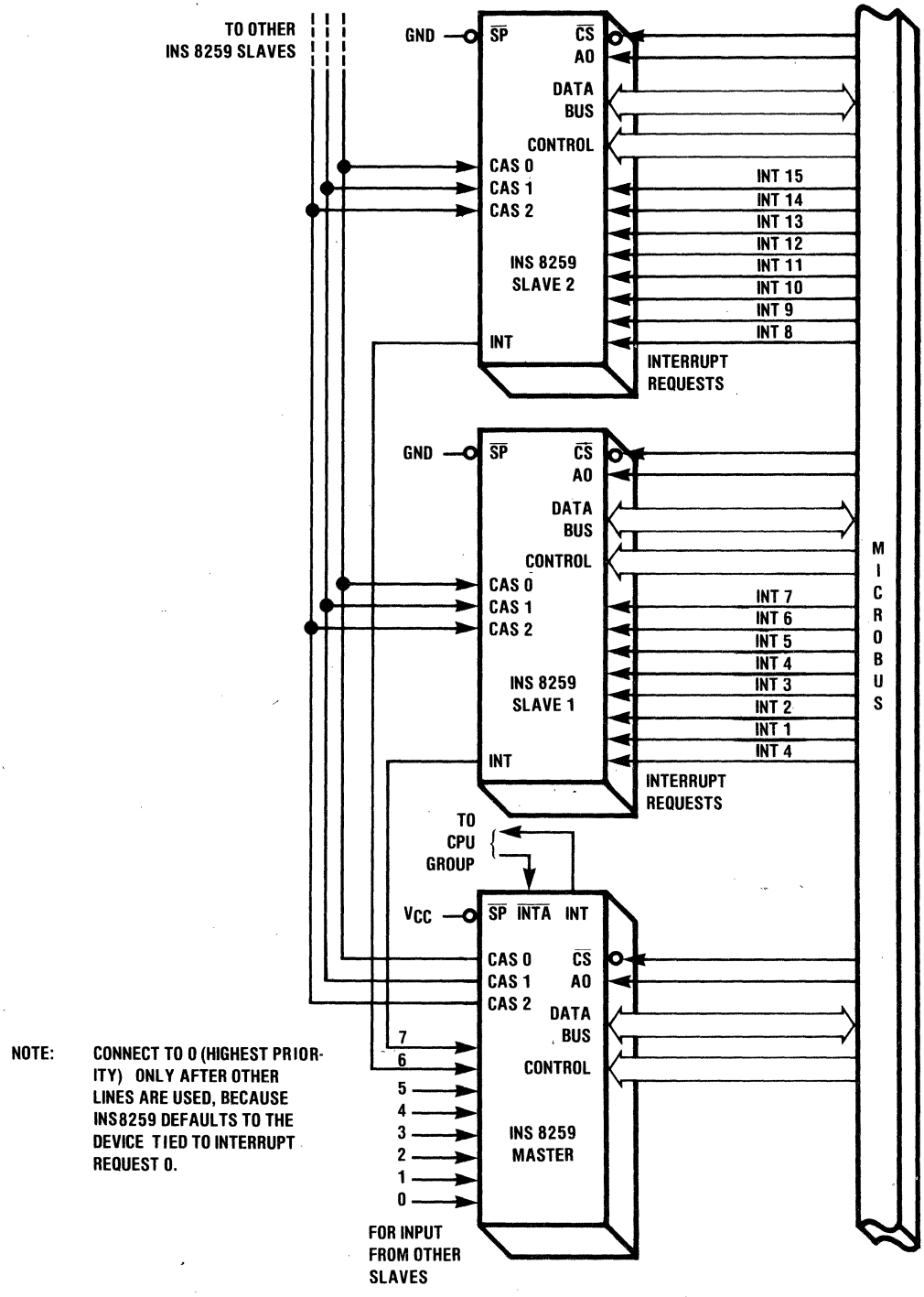
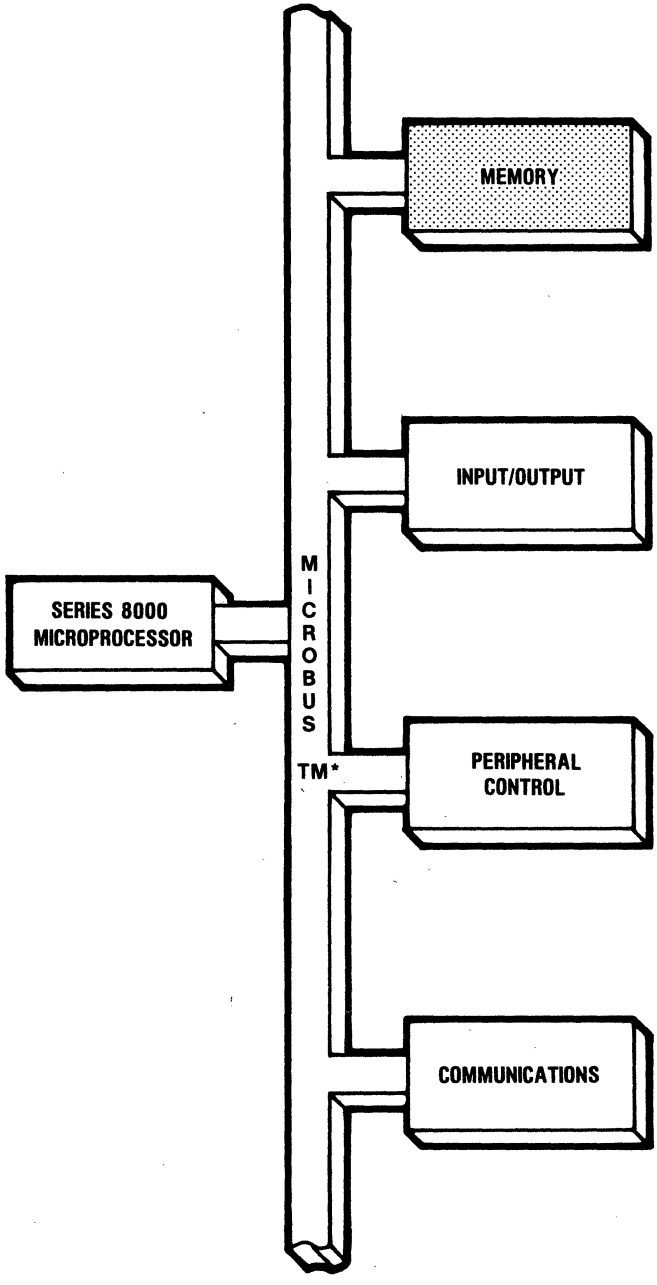


Figure 4-18. INS8259 Interrupt Expansion



Chapter 5
Memory Components

MEMORY

Type/Part Number/Description

RAM

- **Static**

  INS8101A-4
  256 x 4 Static RAM with Separate I/O
  INS8102A
  1024 x 1 Static RAM
  INS8111A-4
  256 x 4 Static RAM with Common I/O
  MM2114
  1024 x 4 Static RAM
  MM5257
  4K x 1 Static RAM

- **Dynamic**

  MM5281
  4096 x 1 Dynamic RAM
  MM5290
  16K Dynamic RAM

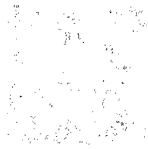
EPROM

MM1702A
256 x 8 EPROM
MM4204/MM5204
512 x 8 EPROM
INS8704
512 x 8 EPROM
INS 8708A
1024 x 8 EPROM

ROM

MM4242/MM5242
1024 x 8 ROM
INS8316 A/E
2048 x 8 MOS Mask ROM
(2708 Compatible)
INS8332E
4096 x 8 MOS ROM (2708 Compatible)
INS8364/8364E
8192 x 8 MOS Mask ROM
(E has 2708 Compatibility)

* Trademark, National Semiconductor Corporation



Memory Components

5.1 GENERAL DESCRIPTION

Using the INS8080A family, the designer can satisfy system requirements from the wide range of National Semiconductor's RAM, PROM, and ROM components. For program storage, the flexible PROM is matched by direct replacement ROMs. For random access storage, the designer can choose from one of the industry's broadest lines of RAMs, fabricated using bipolar, MOS, and CMOS technologies.

5.2 ADDRESSING CONSIDERATIONS

The INS8080A has a 16-bit address bus that is capable of addressing up to 65K bytes of memory. In small systems with minimum memory, buffering of the A_{15}-A_0 Address Bus may not be required. However, as memory requirements increase, buffering is required for the bus. This address buffering function can be implemented by using two National Semiconductor INS8202 TRI-STATE Octal Buffers as shown in figure 5.1. Note that the system Bus Enable ($\overline{BUSEN}$) signal is connected to the buffers so that they are forced into their high-impedance state during a DMA data transfer ($\overline{BUSEN}$ = logic 1) or any other time that bus access is desired, thereby allowing other devices to gain access of the address bus. As mentioned above, up to 65K bytes of memory can be directly addressed via the A_{15}-A_0 Address Bus of the INS8080A. The INS8080A microprocessor system can be configured so that memory and input/output devices are either treated separately (isolated input/output) or as a single memory array (memory mapped input/output) as described below. The mapping for the isolated input/output and memory mapped input/output addressing techniques is shown in figure 5-2. With both of these addressing techniques, the most common method of addressing memory or input/output devices is to decode some of the address bus bits as "chip selects" (using a device such as the National Semiconductor INS82LS05 to enable the addressed memory or the input/output device.

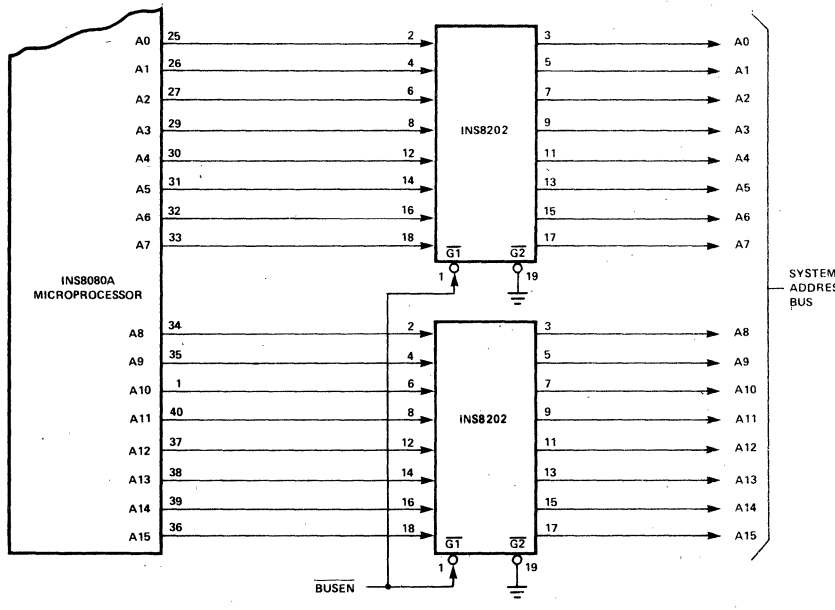


Figure 5-1. Address Buffer Design Using INS8202 Devices

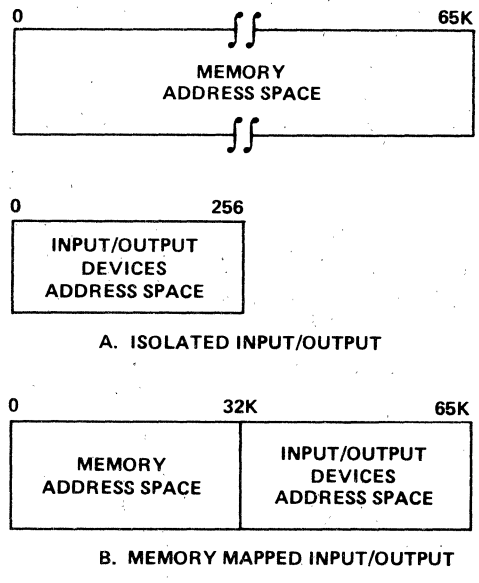


Figure 5-2. Mapping for Isolated Input/Output and Memory Mapped Input/Output Techniques

When the INS8080A system is configured for isolated input/output addressing, the memory address space is separated from the input/output devices address space by using system control signals for the input/output architecture as shown in figure 5-3. Also, with isolated input/output addressing, the input/output devices communicate only with the Accumulator using the IN and OUT Instructions. Thus, since the memory address space is not affected by input/output device addressing, the full address space of 65K bytes is available for memory.

When the INS8080A system is configured for memory mapped input/output addressing, an area of the memory array is assigned to the input/output devices by using system control signals for the input/output architecture as shown in figure 5-4. In this configuration, new input/output control signals $\overline{I/O}$ R ($\overline{MM}$) and $\overline{I/O}$ W ($\overline{MM}$) are generated by gating the $\overline{MEMR}$ and $\overline{MEMW}$ signals with most significant address bit A_{15}. (Since these new input/output signals connect in exactly the same manner as the corresponding signals of the isolated input/output configuration, the system bus characteristics are unaltered). Address bit A_{15} is used because it allows up to 32K bytes of memory addressing, and because it is easier to control with software. However, any other address bit may be used for this gating function. When bit A_{15} is low, the memory address space is active and when bit A_{15} is high, the input/output devices address space is active.

With memory mapped input/output addressing, all of the instructions that can be used to manipulate memory locations (for example, MOV M, r; LDA; STA; LHLD; et cetera) can also be used for the input/output devices. These devices are still considered addressed "PORTS" but instead of the Accumulator being the only data transfer medium for the peripherals, any of the internal registers of the INS8080A can also be used for this purpose. Thus, memory mapped input/output addressing is suited for small systems that require high throughput and have less than 32K bytes of memory.

5.3 INTERFACING TO MEMORY

The CPU group of the INS8080A microprocessor family interfaces with standard semiconductor memory components (and input/output devices) via the MICROBUS. A typical interface to a memory array having 6K bytes of ROM storage and 512 bytes of RAM storage is shown in figure 5-5. This typical memory interface is suitable for almost any size of memory array. However, in larger systems, buffers may be required for driving the three buses and decoders may be required for generating the chip select signals for the memory array (and input/output devices).

As shown in figure 5-5, the interfacing to the three National Semiconductor INS8316 ROMs is quite straightforward. The D_0-D_7 output lines

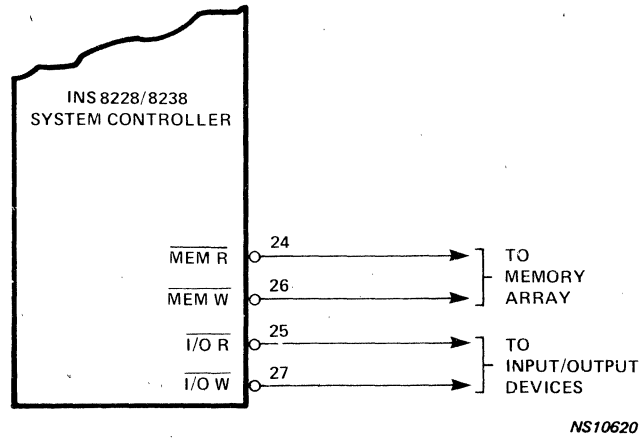


Figure 5-3. System Control Signals for Isolated Input/Output Addressing

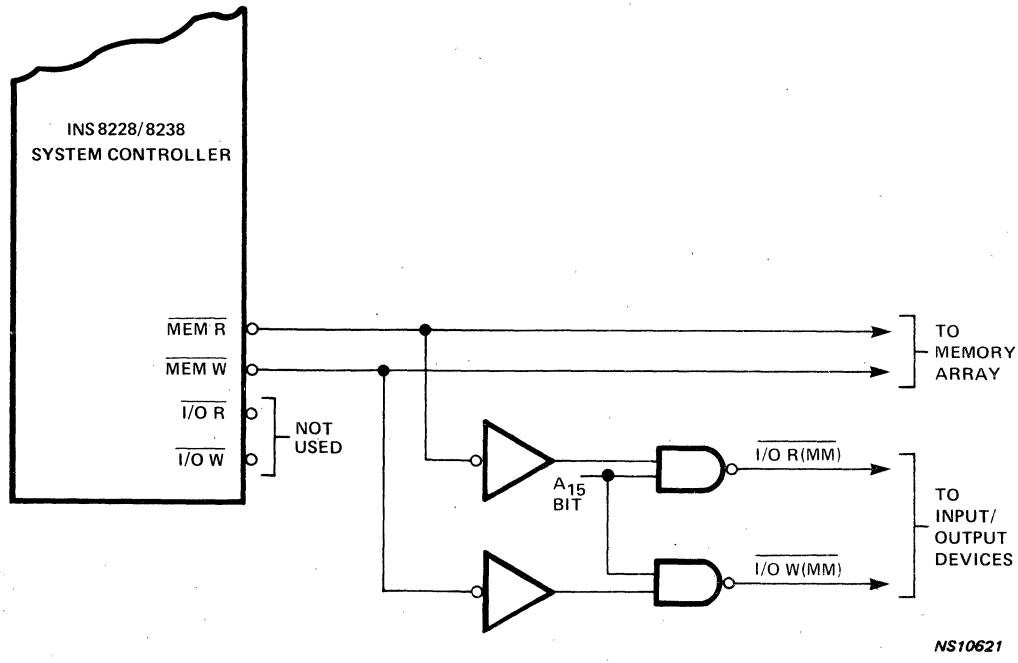


Figure 5-4. System Control Signals for Memory Mapped Input/Output Addressing

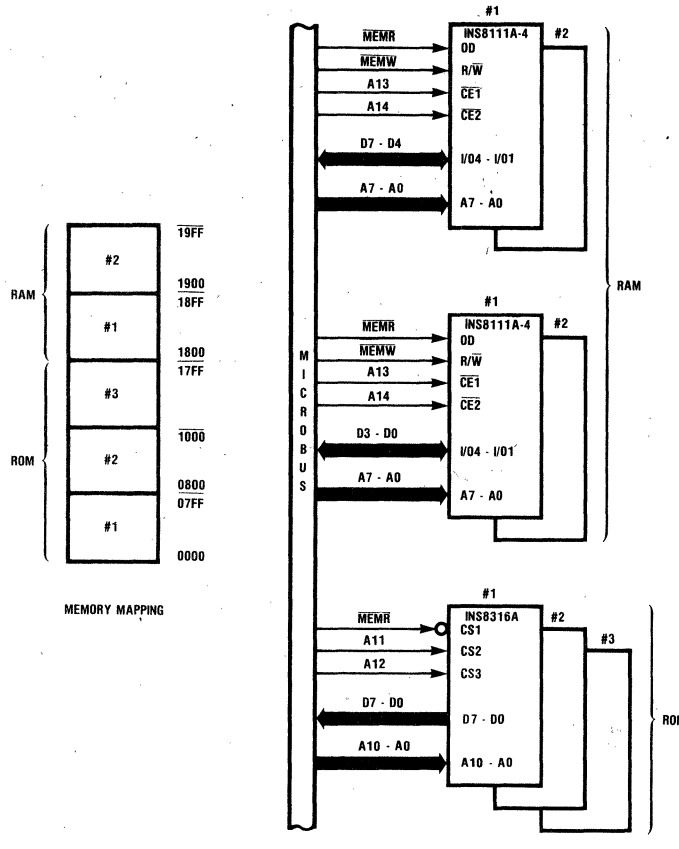


Figure 5-5. Typical Memory Interface

of the ROMs are connected to the bidirectional Data Bus; the A_0-A_{10} address inputs are connected to corresponding bits of the Address Bus; the CS2 and CS3 chip select inputs are connected to the A_{11} and A_{12} bits (most significant) of the Address Bus; and the CS1 chip select input of the ROMs is connected to the inverted $\overline{\text{MEM R}}$ signal of the Control Bus. During a FETCH or MEMORY READ machine cycle, the CPU group may output an address in the ROM address space of the memory array. When this occurs, the data stored at the addressed ROM location are then gated onto the External Data Bus with the $\overline{\text{MEM R}}$ signal. In this way, data are read from the ROMs in the INS8080A microprocessor system.

The interfacing to the four National Semiconductor INS8111A-4 static RAMs is also straightforward. The I/O_1-I/O_4 common input/output lines of the RAMs are connected to corresponding bits of the bidirectional Data Bus; the A_0-A_7 address bits are connected to corresponding bits of the Address Bus; and the R/W and OD inputs of the RAMs are connected to the $\overline{\text{MEM W}}$ and $\overline{\text{MEM R}}$ (or DBIN) signals, respectively, of the Control Bus. During a FETCH, MEMORY READ, or STACK READ machine cycle, the CPU group reads data from the RAMs in exactly the same manner as described above for the ROMs. During a MEMORY WRITE or STACK WRITE machine cycle, the CPU group outputs an address in the RAM address space of the memory array. When this occurs, the data to be written into memory are then strobed into the addressed RAM location with a low-level $\overline{\text{MEM W}}$ signal. In these, ways, data are read from and written into RAMs in the INS8080A microcomputer system.

The memory array of figure 5-5 includes ROMs (INS8316A) and RAMs (INS8111A-4) that have an access time of 450 nanoseconds (maximum). When the INS8080A microprocessor is operated from a clock generator with a tCY of 500 nanoseconds, the required memory access time is from 450 to 550 nanoseconds. Therefore, when slower memory components are used in the system, the INS8080A Microprocessor must contain a synchroniza-

tion provision to allow the memory components to request the wait state (T_W). (The actual number of T_W states to be inserted is determined by external logic that is user designed.) This provision can be implemented for any slow memory (RAM or ROM) by a simple logic control of the READY input of the INS8080A as follows. When the addressed slower memory receives a MEM R or MEM W signal, it places a low-level on the READY line of the microprocessor, causing the INS8080A to enter the WAIT sequence (refer to 3.2.2.2). After the slower memory has had time to respond, it places a high-level on the READY line, thereby allowing completion of the instruction cycle.

5.4 DYNAMIC MEMORY

Many new memory system designs are using dynamic RAMs, particulary in large memory systems, or systems using dedicated memory such as CRT displays.

Refresh requirements make dynamic RAMs slightly harder to use than static RAMs. The designer is paid back for his efforts however, by reduced overall system cost using dynamic RAMs in three ways:

- Dynamic RAMs tend to be cheaper than static RAMs of the same size.
- Dynamic RAMs use less power, especially in a large array.
- Power supplies are cheaper, because of the reduced power requirements and therefore cooling requirements are reduced, allowing a further saving.

A sample of dynamic memory devices available is referenced in section 5.6.6 and 5.6.7. (See section 4.5 for discussion covering the design of memory systems).

5.5 INS8154 128-BY-8-BIT RAM I/O

The INS8154 provides two 8-bit peripheral interface input/output ports and 1024 bits of RAM, organized as 128 x 8 bits of read/write memory for data storage.

The I/O portion consists of two peripheral ports of eight bits each. Each port may be read or written in a parallel (8-bit byte) mode.

In addition to basic I/O, one of the ports, port A, may be programmed to operate in several types of strobed mode with handshake. Strobed mode together with optional interrupt operation permit both high speed parallel data transfers and interface to a wide variety of peripherals with no external logic.

Each bit of each port may be defined as an input or an output and each bit may be set, cleared, or read with a single instruction.

The INS8154 is an N-channel silicon gate device packaged in a 40-pin dual-in-line package. It operates with a single 5-volt power supply and is fully TTL compatible. (See figure 5-6 for block diagram.)

Features

- 128 x 8 RAM
- Single +5-volt power supply
- Low Power Dissipation
- Fully static operation
- Completely TTL compatible
- Two 8-bit programmable I/O ports
- I/O port has TRI-STATE capability
- Handshake controls for strobed mode of operation
- Single bit I/O operations with single instruction
- Reduces system package count
- Independent operation of RAM and I/O
- MICROBUS™Compatible (see figure 5-7 for MICROBUS connection)

5.6 OTHER MEMORY COMPONENTS

This section describes other memory components. (Refer to appendix D for the data sheets.)

5.6.1 INS8101A-4 IK (256 x 4) Static RAM With Separate I/O

General Description

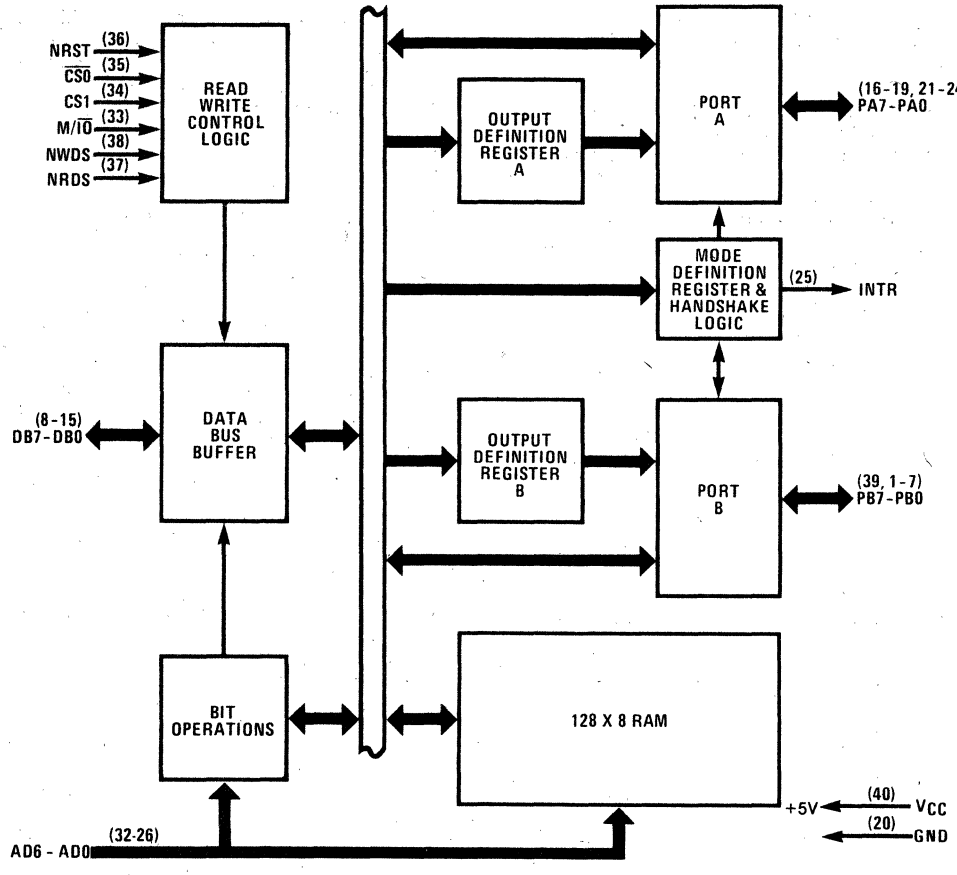
The National INS8101A-4 is a 256 word by 4-bit static random acess memory element fabricated using N-channel enhancement mode Silicon Gate technology. Static storage cells eliminate the need for refresh and the additional peripheral circuitry associated with refresh. The data is read out nondestructively and has the same polarity as the input data.

The INS8101A-4 is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. The features of this memory device can be combined to make a low cost, high performance, and easy to manufacture memory system.

National's silicon gate technology also provides protection against contamination, and permits the use of low cost Epoxy B packaging.

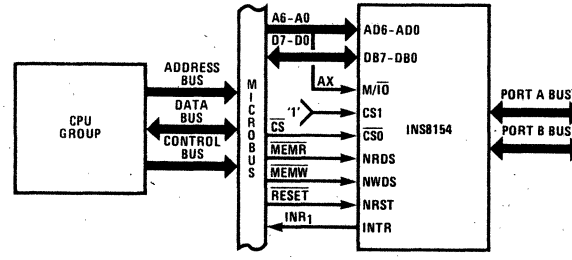
Features

- Organization 256 Words by 4 Bits
- Access time - 0.5 to 1.0μs Max.
- Single +5V Supply Voltage
- Directly TTL Compatible - All inputs and Outputs



NOTE: APPLICABLE PINOUT NUMBERS ARE INCLUDED WITHIN PARENTHESES.

Figure 5-6. INS8154 Block Diagram



NOTE

The INTR signal becomes active only in the strobed mode when a data transaction has occurred.

Figure 5-7. INS8154 MICROBUS Connection

- Static MOS - No Clocks or Refreshing Required
- Simple Memory Expansion - Chip Enable Input
- Low Cost Packaging - 22 Pin Epoxy B Dual-In-Line Configuration
- Low Power - Typically 150 mW
- Tri-State® Output - OR-Tie Capability
- Output Disable Provided for Ease of Use in Common Data Bus Systems

5.6.2 INS8111A-4 1K (256 x 4) RAM With Common I/O

General Description

The National INS8111A-4 is a 256 by 4 static random access memory element fabricated using N-channel enhancement mode Silicon Gate technology. Static storage cells eliminate the need for refresh and the peripheral circuitry associated with refresh. The data is read out nondestructively and has the same polarity as the input data. Common Data Input/Output pins are provided.

The INS8111A-4 is directly TTL in all respects: inputs, outputs, and a single +5V supply. The two Chip-enables allow easy selection of an individual package when out-puts are OR-tied. The features of this memory device can be combined to make a low cost, high performance, and easy to manufacture memory system.

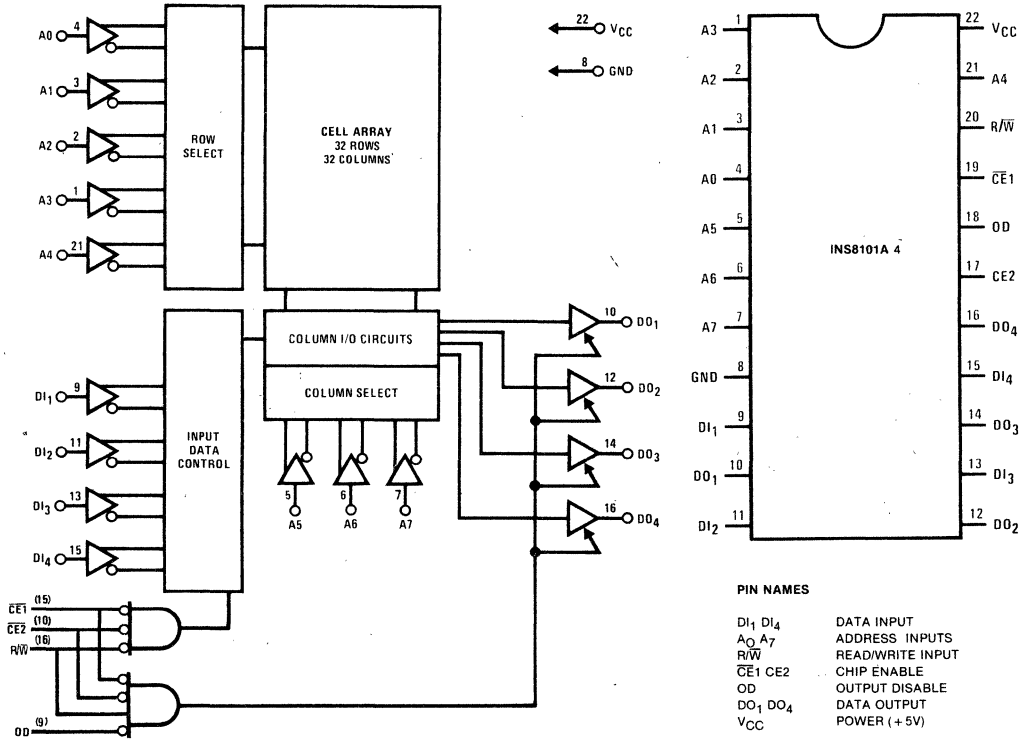
National's silicon gate technology provides excellent protection against contamination and permits the use of low cost Epoxy B packaging.

Features

- Organization 256 Words by 4 Bits
- Common Data Input and Output
- Single +5V Supply Voltage
- Directly TTL Compatible - All Inputs and Outputs
- Static MOS - No Clocks or Refreshing Required
- Access Time - 0.5 to 1.0μs Max.
- Simple Memory Expansion - Chip Enable Input
- Low Cost Packaging - 18 Pin Epoxy B Dual-In-Line Configuration
- Low Power - Typically 150 mW
- Tri-State® Output - OR-Tie Capability

5

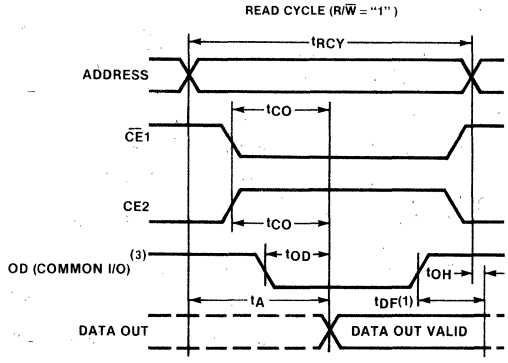
Block and Connection Diagrams (INS8101A-4)

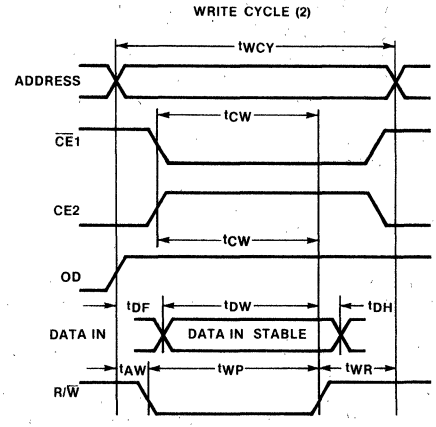


PIN NAMES

DI_1 DI_4	DATA INPUT
A_0 A_7	ADDRESS INPUTS
R/W	READ/WRITE INPUT
CE1 CE2	CHIP ENABLE
OD	OUTPUT DISABLE
DO_1 DO_4	DATA OUTPUT
V_{CC}	POWER (+5V)

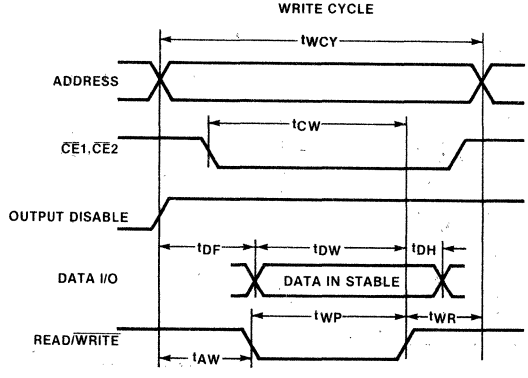
Switching Time Waveforms (INS8101A-4)

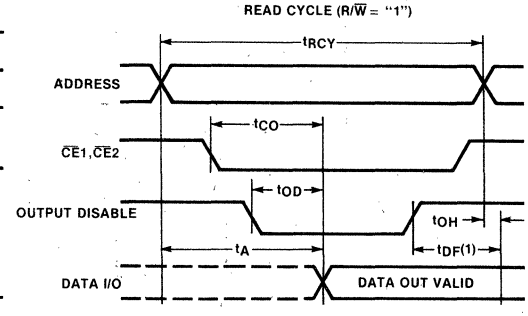




Note 1: t_{DF} is with respect to the trailing edge of $\overline{CE}1$, CE2, or OD, whichever occurs first.
Note 2: During the write cycle, OD is a logical 1 for common I/O and "don't care" for separate I/O operation.
Note 3: OD should be tied low for separate I/O operation.

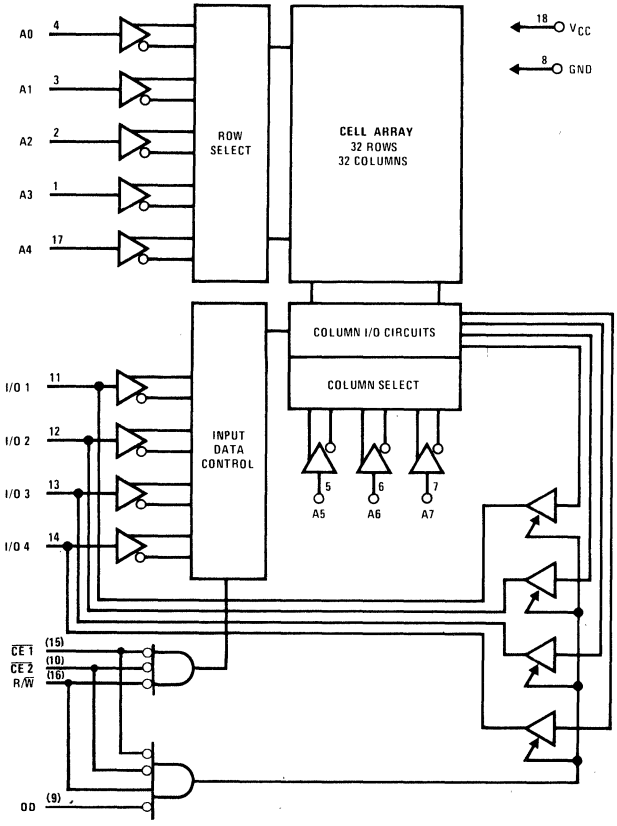
Switching Time Waveforms (INS8111A-4)

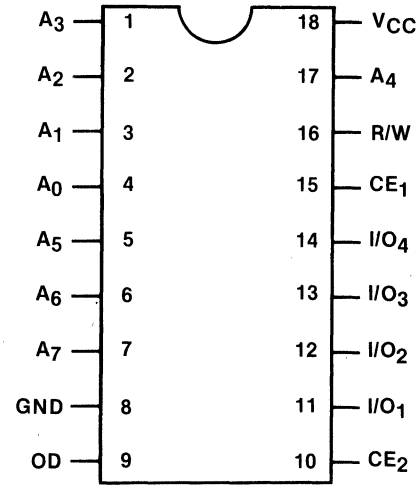




Note 1: t_{DF} is with respect to the trailing edge of $\overline{CE}1$, $\overline{CE}2$, or OD, whichever occurs first.

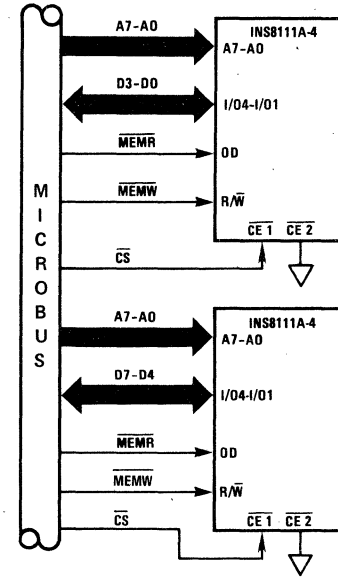
Block and Connection Diagrams (INS8111A-4)





PIN NAMES

A_0A_7	ADDRESS INPUTS
OD	OUTPUT DISABLE
$R/\overline{W}$	READ/WRITE INPUT
$\overline{CE}1$	CHIP ENABLE 1
$\overline{CE}2$	CHIP ENABLE 2
$I/O_1I/O_4$	DATA INPUT/OUTPUT



Truth Table

OD	$\overline{CE1}$	$\overline{CE2}$	$R/\overline{W}$	D_{IN}	D_{OUT}	MODE
X	X	H	X	X	Hi-Z	Not selected
X	L	L	L	L	L	Write "0"
X	L	L	L	H	H	Write "1"
L	L	L	H	X	D_{OUT}	Read
X	H	X	X	X	Hi-Z	
H	X	X	X	X	Hi-Z	

5

5.6.3 The INS8102A 1K (1024 x 1) Static RAM

General Description

The INS8102A family of high speed 1024 x 1-bit static random access read/write memories are manufactured using N-channel depletion-mode silicon gate technology. Static storage cells eliminate the need for clocks or refresh circuitry and the resultant cost associated with them.

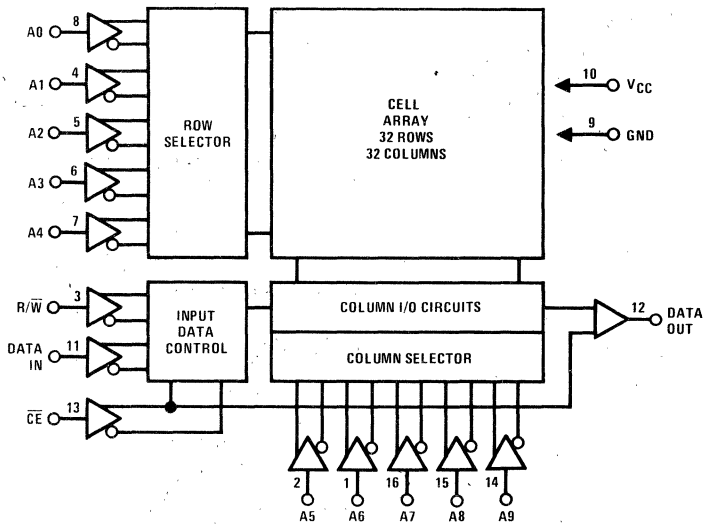
Low threshold silicon gate N-channel technology allows complete DTL/TTL compatibility of all inputs and outputs as well as a single 5V supply. The separate chip enable input ($\overline{CE}$) controlling the TRI-STATE® output allows easy memory expansion by OR-tying individual devices to a data bus. Data in and data out have the same polarity.

In addition to the INS8102A, a low power version, the INS8102AL, is also available. This selection offers a maximum operating current of 33 mA and a guaranteed standby mode down to a power supply voltage of 1.5V.

Features

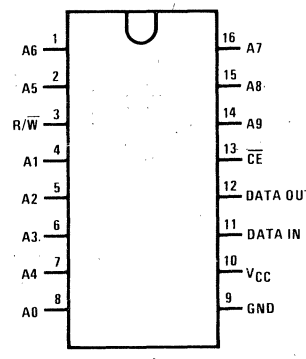
- Single 5V Supply
- All Inputs and Outputs Directly DTL/TTL Compatible
- Static Operation - No Clocks or Refresh
- TRI-STATE Output for Bus Interface
- All Inputs Protected Against Static Charge
- Access Time Down to 250 ns

Block Diagram



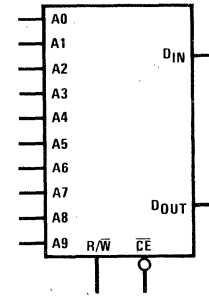
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Symbol



Truth Table

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	Hi-Z	Not selected
L	L	L	L	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{OUT}	Read

Switching Time Waveforms

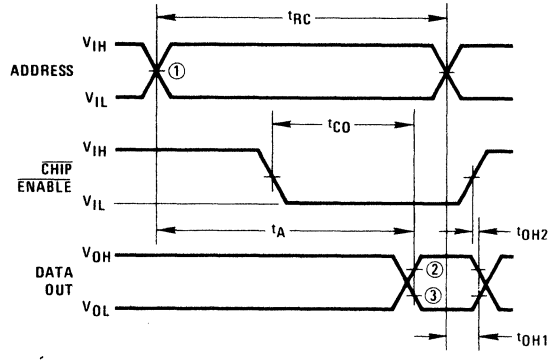


FIGURE 1. Read Cycle

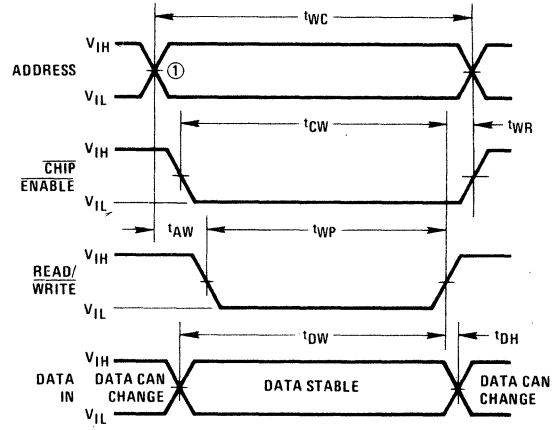
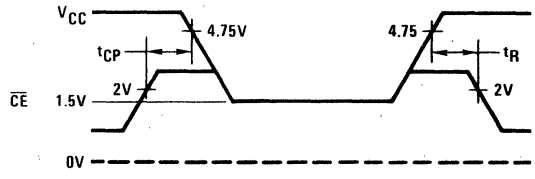


FIGURE 2. Write Cycle

Note ①: Input reference level for timing is 1.5V.
Note ②: V_{OH} = 2V is reference level for output high.
Note ③: V_{OL} = 0.8V is reference level for output low.
Note ④: Input rise and fall times are 10 ns.

Standby Waveforms (INS8102AL)



$1.5V \leq V_{PD} \leq 4.75V$
$1.5V \leq V_{PD} \leq \overline{CE} \leq 2V$
When: $2V \leq V_{PD} \leq V_{CC}$ MAX
$\overline{CE}$ must be 2V minimum.

5.6.4 MM2114 4K (1024 x 4) Static RAM

General Description

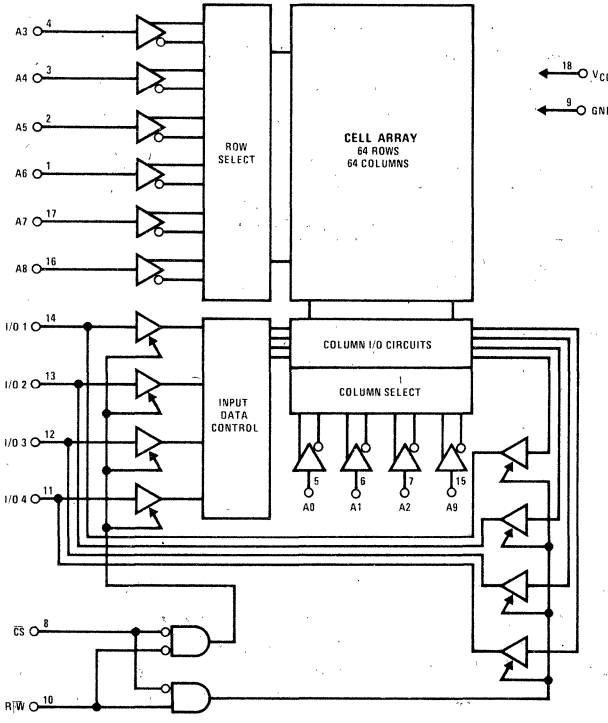
The National MM2114 is a 1024 by 4 static random access memory element fabricated using N-channel enhancement mode Silicon Gate technology. Static storage cells eliminate the need for refresh and the peripheral circuitry associated with refresh. The data is read out nondestructively and has the same polarity as the input data. Common Data Input/Output pins are provided. No address setup times are required.

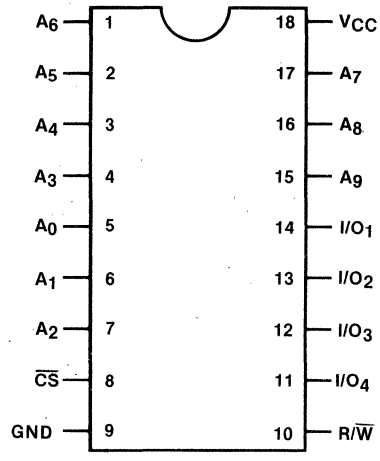
The 2114 is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The Chip select allows easy selection of an individual package when outputs are OR-tied. The features of this memory device can be combined to make a low cost, high performance and easy to manufacture memory system.

National's silicon gate technology provides excellent protection against contamination and permits the use of low cost Epoxy B packaging.

Features

- Organization 1024 Words by 4 Bits
- Common Data Input and Output
- Single +5V Supply Voltage
- Directly TTL Compatible - All Inputs and Outputs
- Static MOS - No Clocks or Refreshing Required
- Identical Cycle and Access Time
- Simple Memory Expansion - Chip Select Input
- Low Cost Packaging - 18 Pin Epoxy B Dual-In-Line Configuration
- Tri-State Output - OR-Tie Capability



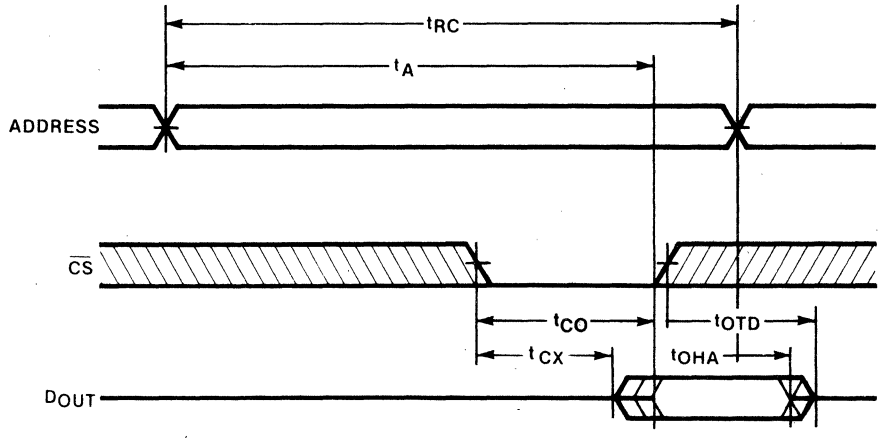


PIN NAMES

A_0-A_9	ADDRESS INPUTS
R/$\overline{W}$	READ/WRITE INPUT
$\overline{CS}$	CHIP SELECT
I/O_1-I/O_4	DATA INPUT/OUTPUT

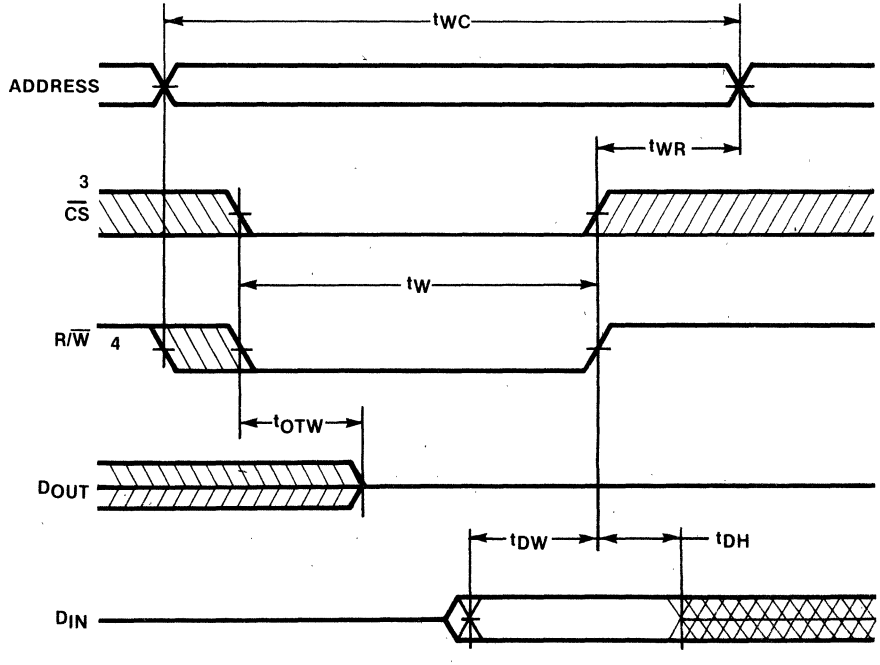
Switching Time Waveforms

READ CYCLE (R/$\overline{W}$ = "1")



NOTES:
1. A Read occurs during the overlap of a low $\overline{CS}$ and a high R/$\overline{W}$
2. A Write occurs during the overlap of a low $\overline{CS}$ and a low R/$\overline{W}$
3. If the $\overline{CS}$ low transition occurs simultaneously with the R/$\overline{W}$ Low transition, the output buffers remain in a high impedance state.
4. R/$\overline{W}$ must be high during all address transitions.

WRITE CYCLE



5.6.5 MM5257 4096 x 1 Static Random Access Memory

General Description

The MM5257 is a 4096 word by 1-bit static random access memory fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data.

The separate chip enable input ($\overline{CE}$) controlling the TRI-STATE® output allows easy memory expansion by OR-tying individual devices to a data bus.

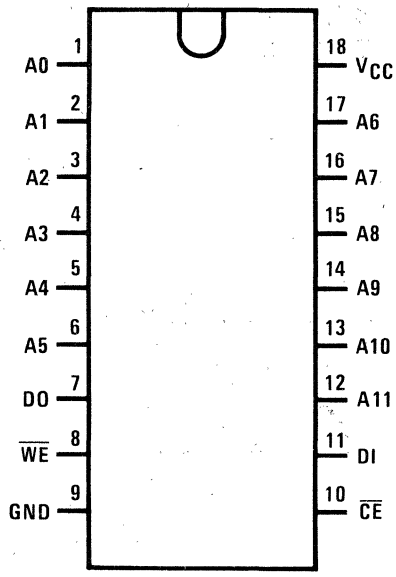
The output is held in a high impedance state during write to simplify common I/O applications.

Features

- All Inputs and Outputs Directly TTL Compatible
- Static Operation - No Clocks or Refreshing Required
- Low Power - 200 mW Typical
- High Speed - 250 ns Typical
- TRI-STATE Output for Bus Interface
- Separate Data In and Data Out Pins
- Single +5V Supply
- Standard 18-Pin Dual-In-Line Package

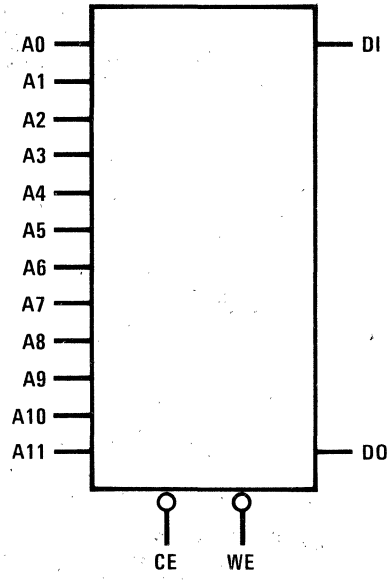
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Symbol



Truth Table

$\overline{CE}$	$\overline{WE}$	DI	D_{OUT}	MODE
H	X	X	Hi-Z	Not Selected
L	L	H	Hi-Z	Write 1
L	L	L	Hi-Z	Write 0
L	H	X	D_{OUT}	Read

Functional Description

Two pins control the operation of the MM5257. Chip Enable ($\overline{CE}$) enables write and read operations and controls TRI-STATING of the data-output buffer. Write Enable ($\overline{WE}$) chooses between READ and WRITE modes and also control output TRI-STATING. The truth table details the states produced by combinations of the $\overline{CE}$ and $\overline{WE}$ controls.

READ-cycle timing is shown in the section on Switching Time Waveforms. $\overline{WE}$ is kept high. Independent of $\overline{CE}$, any change in address code causes new data to be fetched and brought to the output buffer. $\overline{CE}$ must be low, however, for the output buffer to be enabled and transfer the data to the output pin.

Address access time, t_A, is the time required for an address change to produce new data at the output pin, assuming $\overline{CE}$ has enabled the output buffer prior to data arrival. Chip Enable-to-output delay, t_{CO}, is the time required for $\overline{CE}$ to enable the output buffer and transfer previously fetched data to the output pin. Operation with $\overline{CE}$ continously held low is permissible.

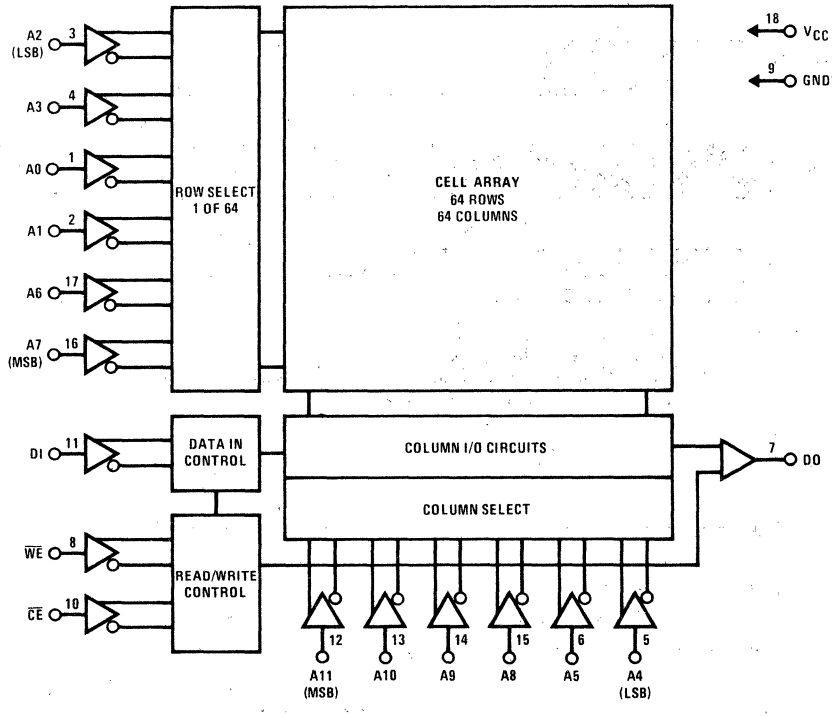
WRITE-cycle timing is shown in the section on Switching Time Waveforms. Writing occurs only during the time both $\overline{CE}$ and $\overline{WE}$ are low. Minimum write-pulse width, t_{WP}, refers to this simultaneous low region. Data set-up and hold times are measured with respect to whichever control first rises. Successive write operations may be performed with $\overline{CE}$ continously held low. $\overline{WE}$ then is used to terminate WRITE between address changes. Alternatively, $\overline{WE}$ may be held low for successive WRITES and $\overline{CE}$ used for WRITE interruption between address change.

In any event, either $\overline{WE}$ or $\overline{CE}$ (or both) must be high during address transitions to prevent erroneous WRITE.

Stand-by operation allows data to be maintained with approximately 50% less operating current. The 2 requirements to guarantee data retention are: a) the power supply voltage must meet the condition $V_{CC} \geq 1.5V$, and b) $\overline{CE}$ must be controlled; to disable the chip prior to reducing V_{CC}, to keep it disabled during the time V_{CC} is reduced, and to maintain the disabled state long enough after V_{CC} is increased to normal for the chip to recover. These requirements are shown by the stand-by waveforms and characteristics.

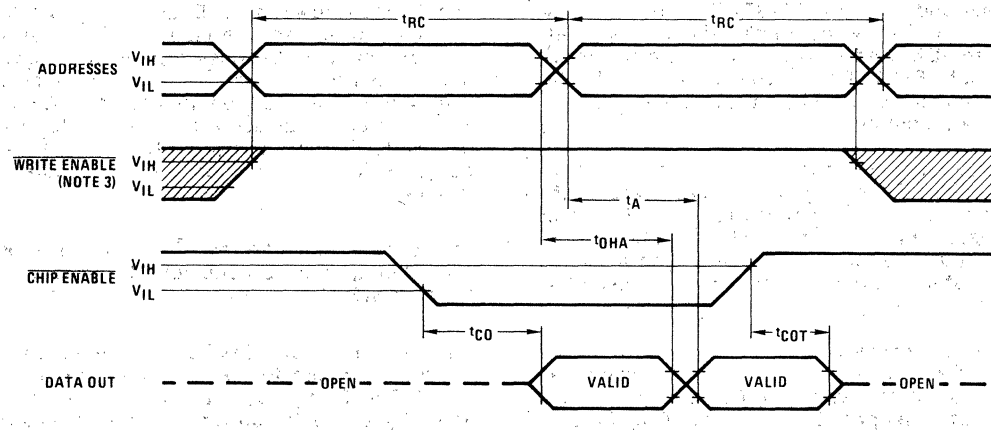
5

Block Diagram

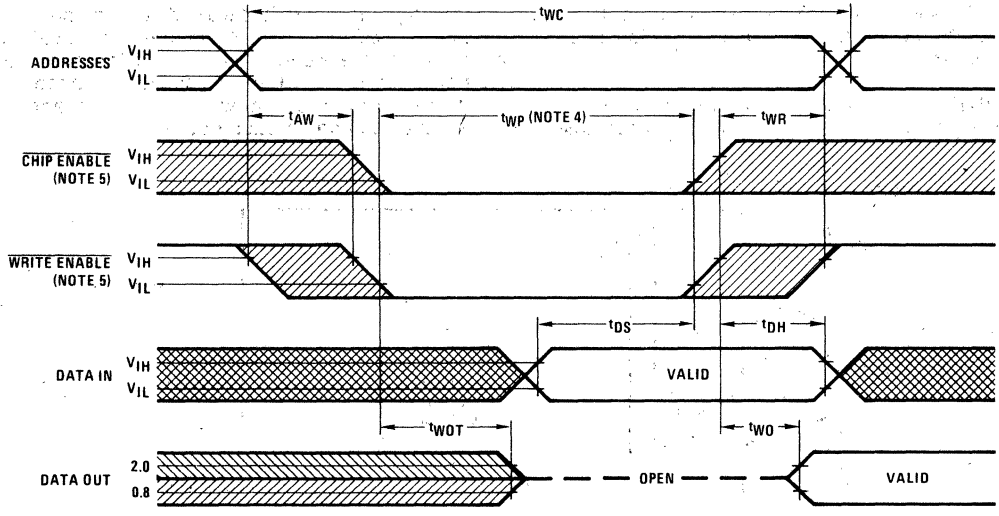


Switching Time Waveforms

Read Cycle



Write Cycle

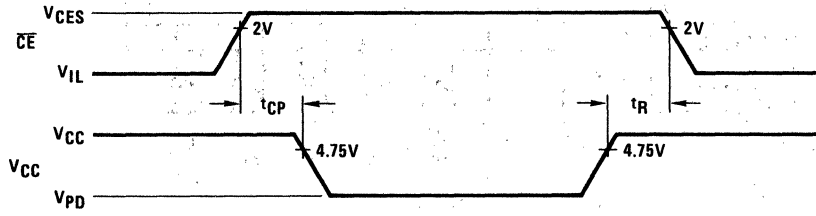


Note 3: $\overline{WE}$ is high during a read cycle ($\overline{WE} \geq V_{IH(MIN)}$).

Note 4: t_{WP} defines the period when both $\overline{CE}$ and $\overline{WE}$ are low. t_{AW} is referenced to the later of $\overline{CE}$ or $\overline{WE}$ going low while t_{DS}, t_{DH} and t_{WR} are referenced to the earlier of $\overline{CE}$ or $\overline{WE}$ going high. t_{WOT} and t_{WO} are referenced to $\overline{WE}$ with $\overline{CE}$ low.

Note 5: Either $\overline{WE}$ or $\overline{CE}$ (or both) must be high during address transitions to prevent erroneous write.

Standby Waveforms



5.6.6 MM5281 4096-BIT Fully TTL Compatible Dynamic RAM

General Description

National's MM5281 is a 4096 word by 1 bit fully TTL compatible dynamic RAM. It incorporates the latest memory design features and can be used in a wide variety of applications, from those which require very high speed to ones where low cost and large bit capacity are the prime criteria.

The MM5281 must be refreshed every two ms. This can be accomplished by performing a READ cycle at each of the 64 row addresses (A_0-A_5). The chip select input can be either high or low for refresh.

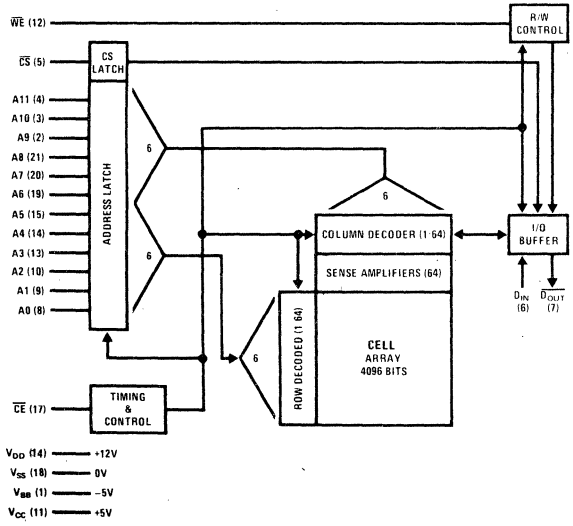
The MM5281 has been designed with minimum production costs as a prime criterion. It is fabricated using N-channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits. The MM5281 uses a single transistor cell to minimize the device area. The single device cell, along with unique design features in the on-chip peripheral circuits, yields a high performance memory device.

Features

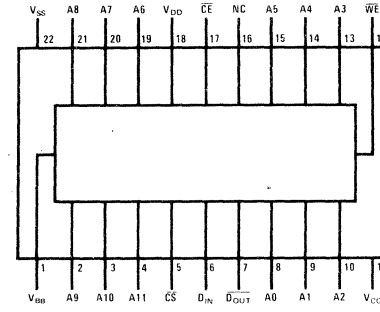
- Organization: 4096 x 1
- Access Time 250 ns Maximum
- Cycle Time 400 ns Minimum
- TTL Compatible
- Address Registers On-Chip
- TRI-STATE® Output
- Simple Read-Modify-Write Operation
- Industry Standard Pin Configuration

5

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5281D

Pin Names

A0–A11	Address Inputs*	V_{BB}	Power (−5V)
$\overline{CE}$	Chip Enable	V_{CC}	Power (+5V)
$\overline{CS}$	Chip Select	V_{DD}	Power (+12V)
D_{IN}	Data Input	V_{SS}	Ground
$\overline{D_{OUT}}$	Data Output	$\overline{WE}$	Write Enable
NC	Not Connected		

*Refresh Address A0–A5

5.6.7 MM5290 16,384 x 1 Bit Dynamic RAM

General Description

The MM5290 is a 16,384 x 1 bit dynamic RAM. It features a multiplexed address input with separate row and column strobes. This added flexibility allows the MM5290 to be used in page mode operation.

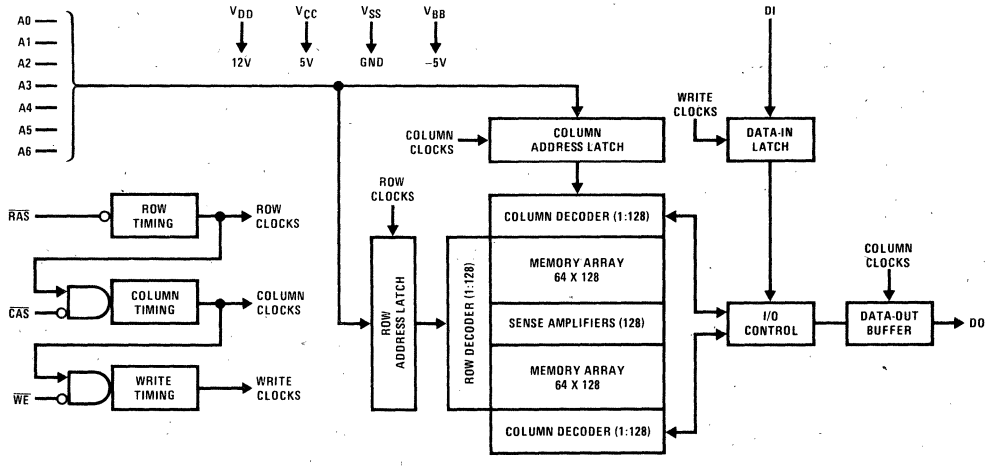
The MM5290 must be refreshed every 2 ms. This can be accomplished by performing any cycle which brings the Row Address Strobe active including an RAS-only cycle at each of the 128 row addresses.

N-channel double-poly silicon gate technology, developed by National, is used in the manufacture of the MM5290. This process combines high density and performance with reliability. Greater system densities are achievable by the use of a 16-pin dual-in-line package for the MM5290.

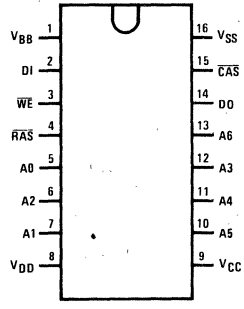
Features

- Access Times: 150 ns, 200 ns, 300 ns
- Low Power: 462 mW Max
- TTL Compatible: All Inputs and Output
- Gated CAS - Noncritical Timing
- Read, Write, Read-Modify-Write and RAS-only Refresh Cycles
- Page Mode Operation
- Industry Standard 16-pin Configuraton

Block and Connection Diagrams



Dual-In-Line Package



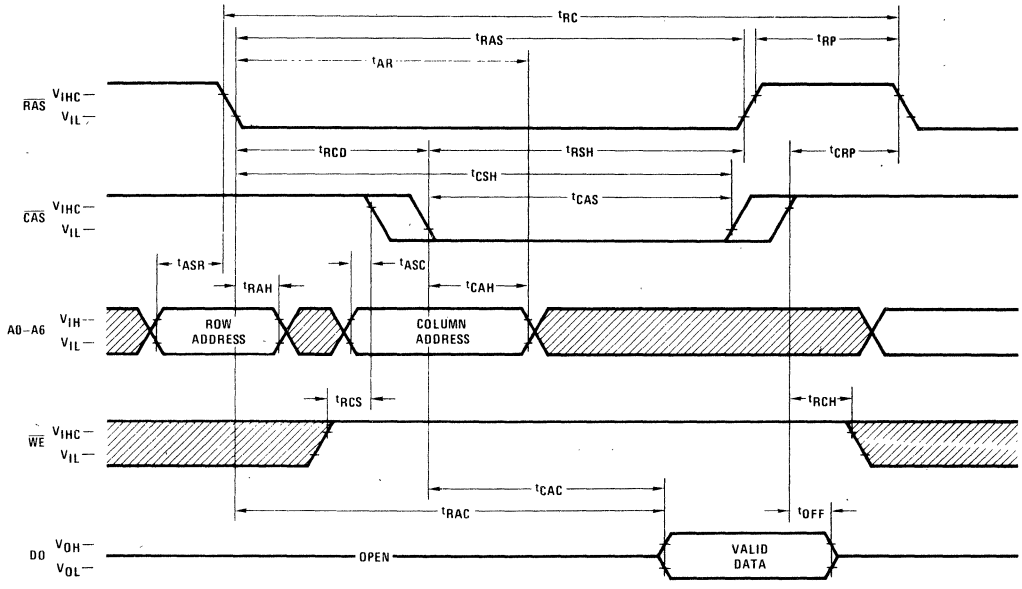
TOP VIEW

Pin Names

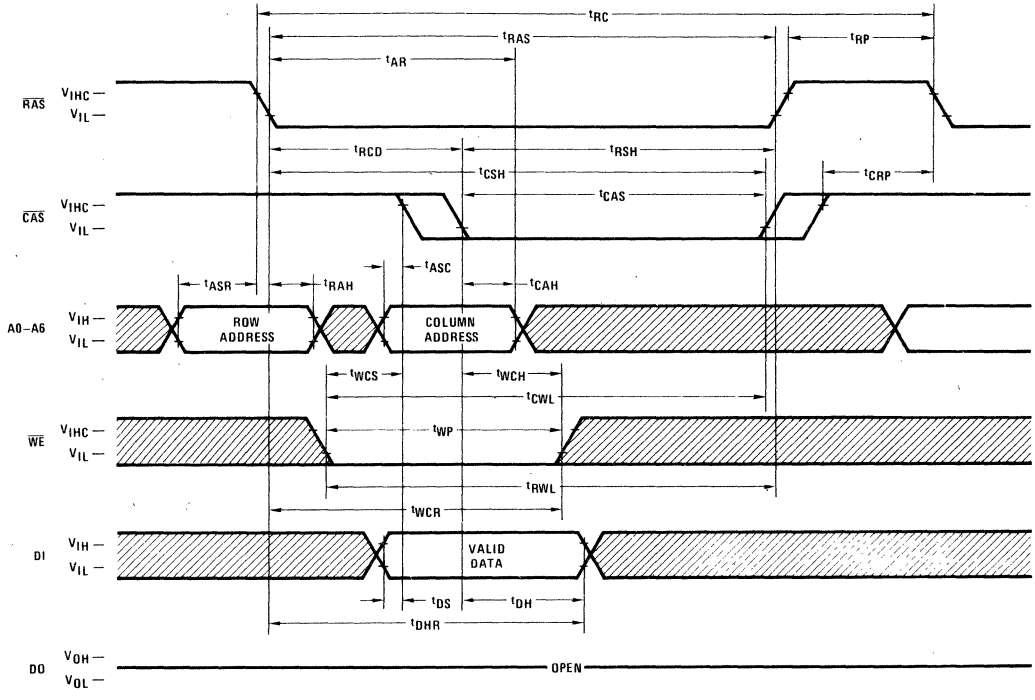
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0–A6	Address Inputs
DI	Data Input
DO	Data Output
V_{DD}	Power (12V)
V_{CC}	Power (5V)
V_{SS}	Ground
V_{BB}	Power (−5V)

Switching Time Waveforms

Read Cycle

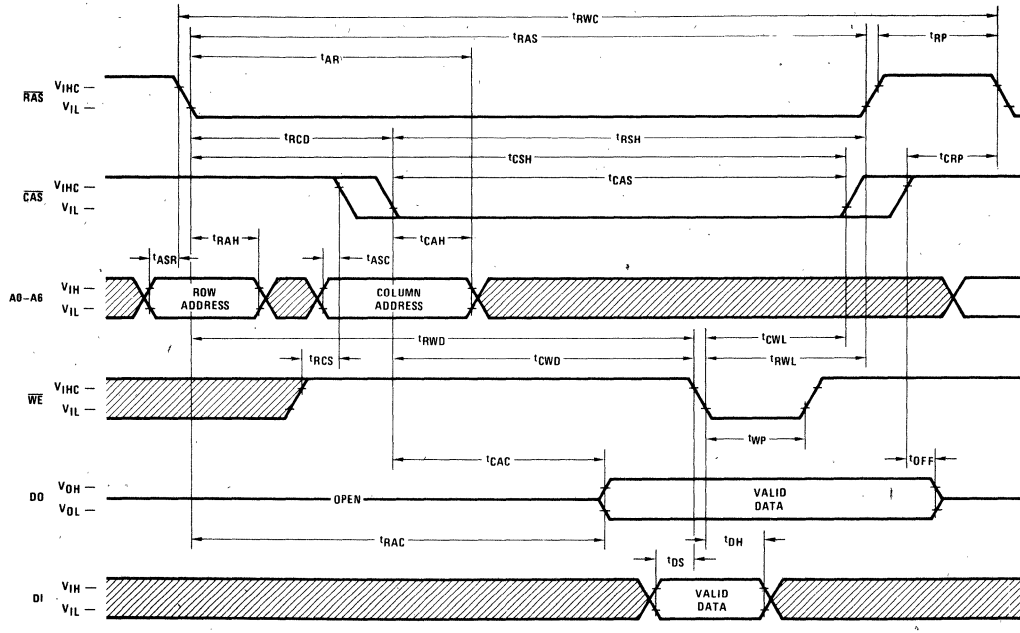


Write Cycle (Early Write)

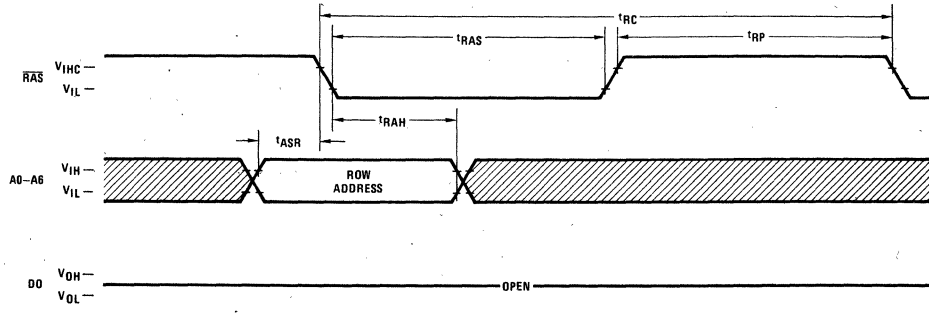


5

Read-Write Cycle, Read-Modify-Write Cycle



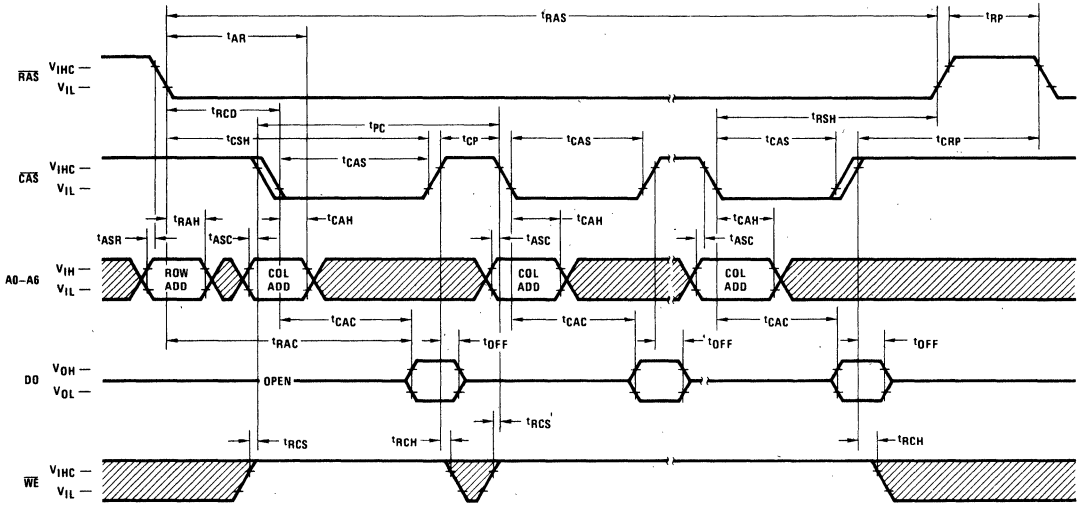
RAS-Only Refresh Cycle



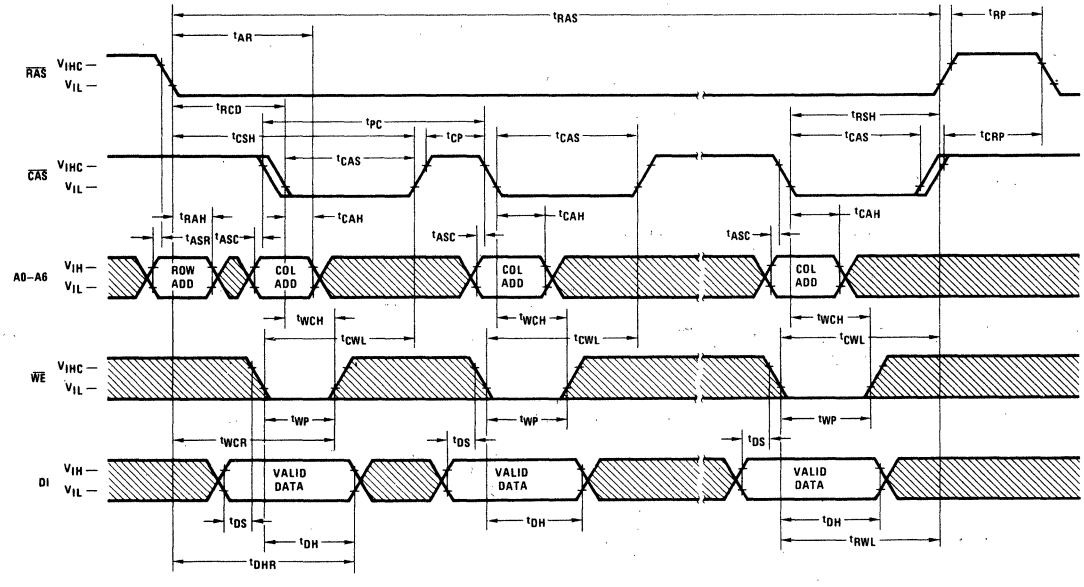
Note. $\overline{CAS}$ = V_{IHC}, $\overline{WE}$ = don't care

Switching Time Waveforms (Continued)

Page Mode Read Cycle

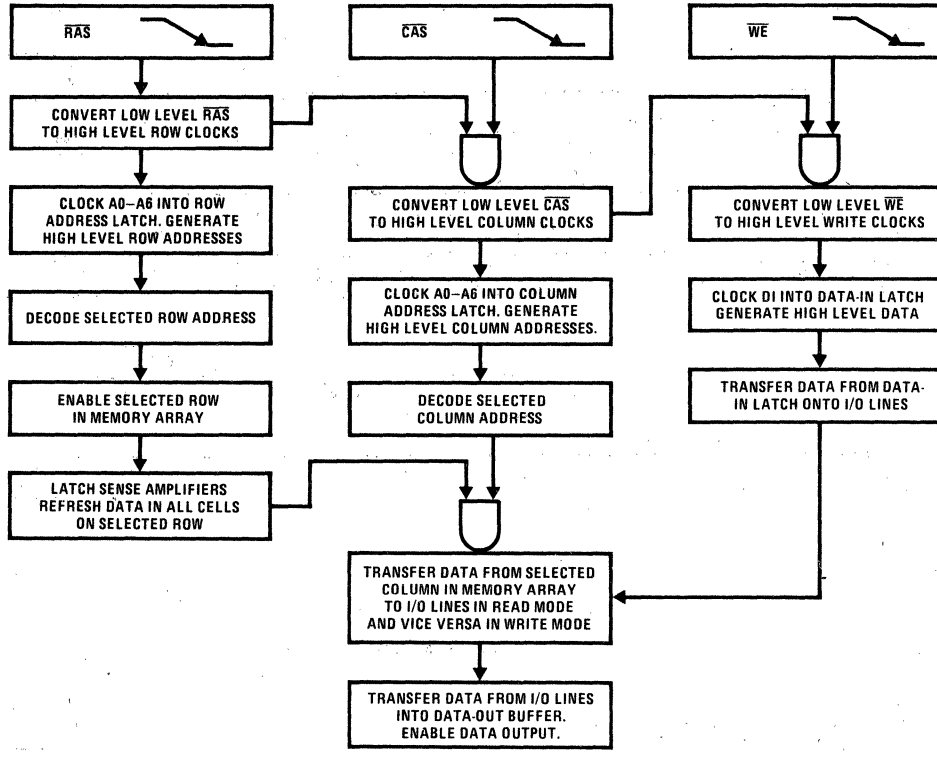


Page Mode Write Cycle

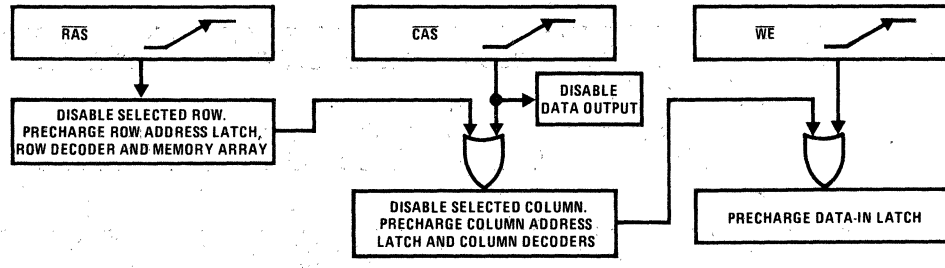


Timing Flow Chart

ACTIVE



PRECHARGE



5.6.8 MM1702A 2048-Bit Electrically Programmable ROM

General Description

The MM1702A is a 256 word by 8-bit electrically programmable ROM ideally suited for uses where fast turn-around and pattern experimentation are important. The MM1702A undergoes complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.

The MM1702AQ is packaged in a 24-pin dual-in-line package with a transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device. The MM1702AD is packaged in a 24-pin dual-in-line package with a metal lid and is not erasable.

The circuitry of the MM1702A is entirely static; no clocks are required.

A pin-for-pin metal mask programmed ROM, the MM1302 is ideal for large volume production runs of systems initially using the MM1702A.

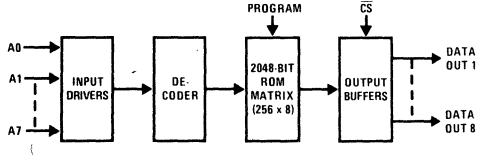
The MM1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

Features

- Fast Programming - 30 Seconds for all 2048 Bits
- All 2048 Bits Guaranteed Programmable -100% Factory Tested
- Fully Decoded, 256 x 8 organization
- Static MOS - No Clocks Required
- Inputs and Outputs DTL and TTL Compatible
- TRI-STATE® Output - OR-tie Capability
- Simple Memory Expansion - Chip Select Input Lead
- Direct Replacement for the Intel 1702A

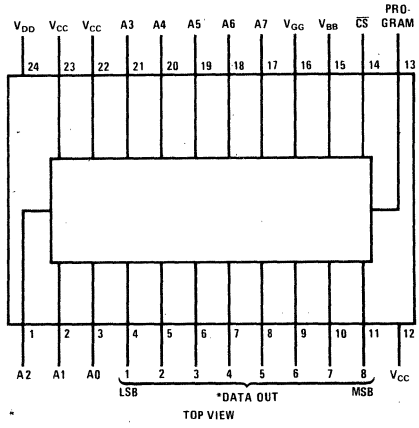
5

Block and Connection Diagrams



Note: In the read mode a logic "1" at the address inputs and data outputs is a high and logic "0" is a low.

Dual-In-Line Package



*This pin is the data input lead during programming.

Order Number MM1702AD
Order Number MM1702AQ

Pin Names

A0–A7	Address Inputs
$\overline{CS}$	Chip Select Input
$D_{OUT\,1} - D_{OUT\,8}$	Data Outputs

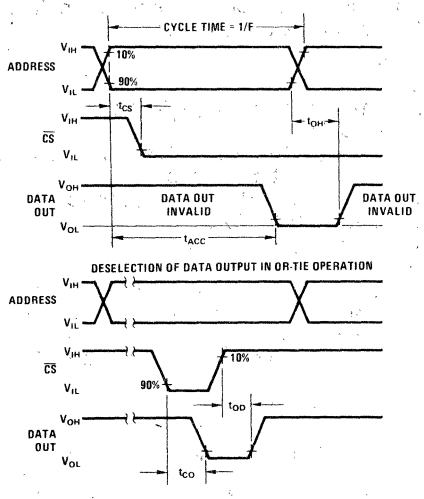
Pin Connections*

MODE/PIN	12 (V_{CC})	13 (PROGRAM)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG} (V_{IL4P})	GND	GND

*The external lead connections to the MM1702A differ, depending on whether the device is being programmed or used in read mode. (See following table.) In the programming mode, the data inputs 1–8 are pins 4–11 respectively.

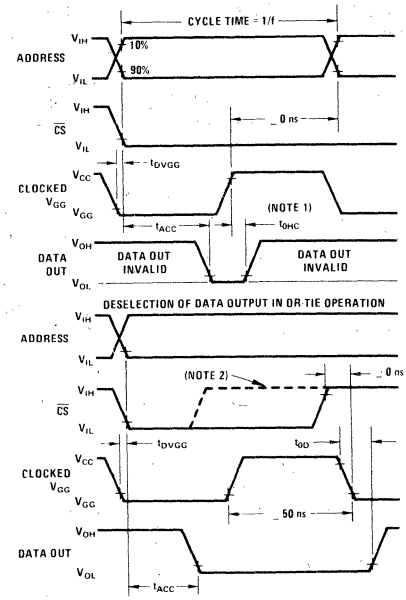
Read Operation Switching Time Waveforms

(a) Constant V_{GG} Operation



Conditions of Test:
Input pulse amplitudes: 0–4V, t_r, $t_f \leq 50$ ns. Output load is 1 TTL gate, measurements made at output of TTL gate ($t_{PD} \leq 15$ ns), $C_L = 15$ pF.

(b) Power-Down Option (Note 1)



Note 1. The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

Note 2: If $\overline{CS}$ makes a transition from V_{IL} to V_{IH} while clocked V_{GG} is at V_{GG}, then deselection of output occurs at t_{OD} as shown in static operation with constant V_{GG}.

Operation of the MM1702A in Program Mode

Initially, all 2048 bits of the ROM are in the "0" state (output low). Information is introduced by selectively programming "1's" (output high) in the proper bit locations.

Word address selection is done by the same decoding circuitry used in the READ mode (see table for logic levels.) All 8 address bits must be in the binary complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses must be held in their binary complement state for a minimum of 25μs after V_{DD} and V_{GG} have moved to their negative levels. The addresses must then make the transition to their true state a minimum of 10μs before the program pulse is applied. The addresses should be programmed in the sequence 0-255 for a minimum of 32 times. The eight output terminals are used as data inputs to determine the information pattern in the eight bits of each word. A low data input level (−48V) will program a "1" and a high data input level (ground) will leave a "0". All eight bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals.

During the programming, V_{GG}, V_{DD}, and the Program Pulse are pulsed signals.

MM1702A Erasing Procedure

The MM1702A may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose (i.e. UV intensity × exposure time) is 6W sec/cm^2. Examples of ultraviolet sources which can erase the MM1702A in 10 to 20 minutes are the Model UVS-54 and Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters, and the MM1702A to be erased should be placed about one inch away from the lamp tubes. There exists no absolute rule for erase time. Establish a worst case time required with the equipment. Then over-erase by a factor of 2, i.e., if the device appears erased after 8 minutes, continue exposure for an additional 16 minutes for a total of 24 minutes. (May be expressed as x + 2x.)

5.6.9 MM4204/MM5204 Electrically Programmable 4096-Bit Read Only Memory (EPROM)

General Description

The MM4204/MM5204 is a 4096-bit static Read Only Memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as 512 words by 8 bits per word. Programming of the memory is accomplished by storing a charge in a cell location by applying a −50V pulse. A logic input, "Power Saver," is provided which gives a 5:1 decrease in power when the memory is not being accessed.

Features

- Field Programmable
- Fast Program Time: Ten Seconds Typical for 4096-Bits
- Fast Access Time
  - MM4204 1.25μs
  - MM5204 1μs
- DTL/TTL Compatibility
- Standard Power Supplies 5.0V, −12V
- Static Operation - No Clock Required
- Easy Memory Expansion - TRI-STATE® Output Chip Select Input ($\overline{CS}$)
- "Q" Quartz Lid Version Erasable with Short Wave Ultraviolet light (i.e., 253.7 nm)
- Low Power Dissipation
- "Power Saver" Control for Low Power Applications

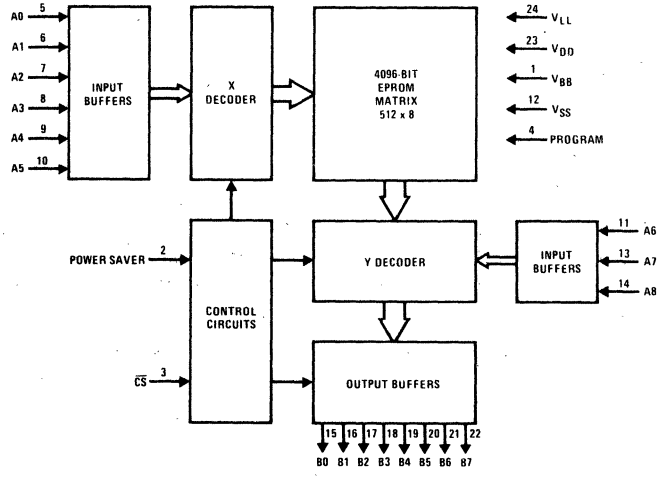
Applications

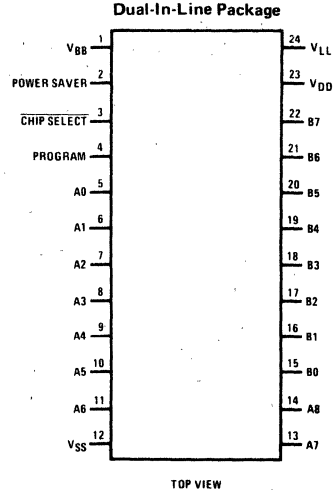
- Code Conversion
- Random Logic Synthesis
- Table Look-Up
- Character Generator
- Microprogramming
- Electronic Keyboards

Programming

The MM4204/MM5204 is normally shipped in the unprogrammed state. All 4096-bits are at logic "0" state. The table of electrical programming characteristics and Figure 2 give the conditions for programming of the device. In the

Block and Connection Diagrams





program mode the device effectively becomes a RAM with the 512 word locations selected by address inputs A_0-A_8. Data inputs are B_0-B_7 and write operation is controlled by pulsing the Program input. Since the EROM is initially shipped with all "0's," a V_{IHP} on any data input B_0-B_7 will leave the stored "0's" undisturbed, and a V_{ILP} on any data input B_0-B_7 will write a logic "1" into that location.

National offers programmer options with both the IMP16-P and the PACE IPC-16P Microprocessor Development Systems.

Microprocessor System	Programmer Part Number
IMP16-P	IMP-16P/805
IPC16-P	IPC-16P/805

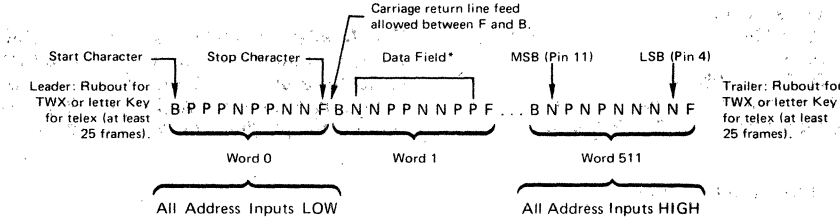
Contact the local sales office for further information. There are also several commercial programmers available such as the Data I/O Model V.

Most National Distributors have programming capabilities available. Those distributors should be contacted directly to determine which data entry formats are available.

In addition, data may be submitted to National Semiconductor for factory programming. One of the following formats should be observed:

Preferred Format

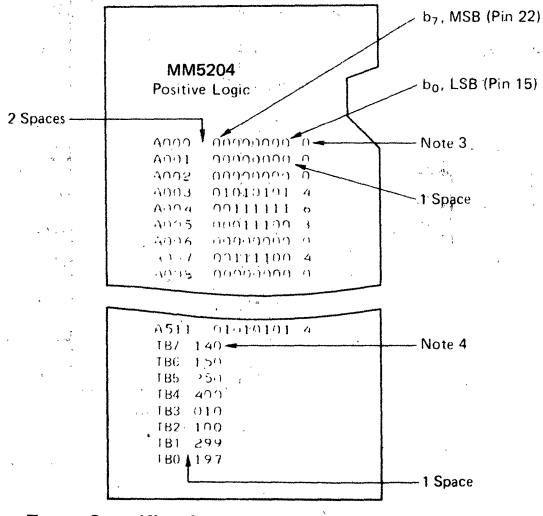
The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7-bit ASCII code from model 33 teletype or TWX. The paper tape should be as the following example:



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between the F stop character and the B start character. If an error is made in preparing a tape the entire word including the B and F start and stop characters must be rubbed out. Data for exactly 512 words must be entered beginning with word 0.

Alternate Format

(Punched tape (Note 1) or cards)



Note 1: The code is a 7-bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the latter A.

Note 3: The total number of "1" bits in the output word.

Note 4: The total number of "1" bits in each output column or bit position.

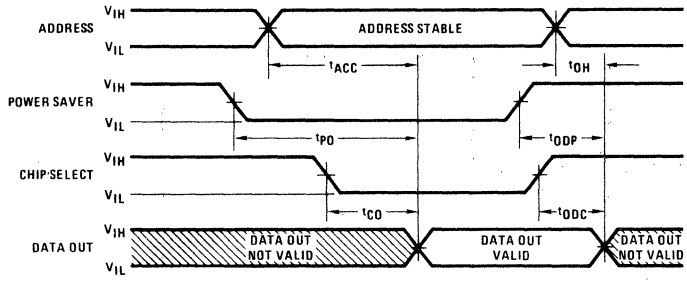
Erase Specification

The recommended dosage of ultraviolet light exposure is 6W sec/cm^2.

Erasing Procedure

The MM4204Q/MM5204Q may be erased by exposure to short-wave ultraviolet light - 253.7 nm. There exists no absolute rule for erasing time or distance from source. The erasing equipment output capability should be calibrated. Establish a worse case time required with the equipment. Then over-erase by a factor of 2, i.e., if the device appears erased after 8 minutes, continue exposure for an additional 16 minutes for a total of 24 minutes. Examples of UV sources include the Model UVS-54 and Model S-52 manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without shortwave filters. The MM4204 /MM5204 should be placed about one inch away from the lamp for about 20-30 minutes.

Switching Time Waveforms



Note. All times measured with respect to 1.5V level with t_r and $t_f \leq 20$ ns.

FIGURE 1. Read Operation

Programming Waveforms

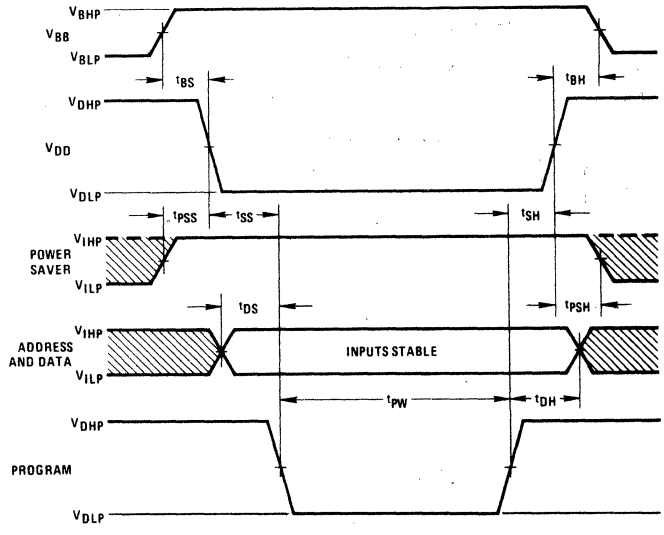
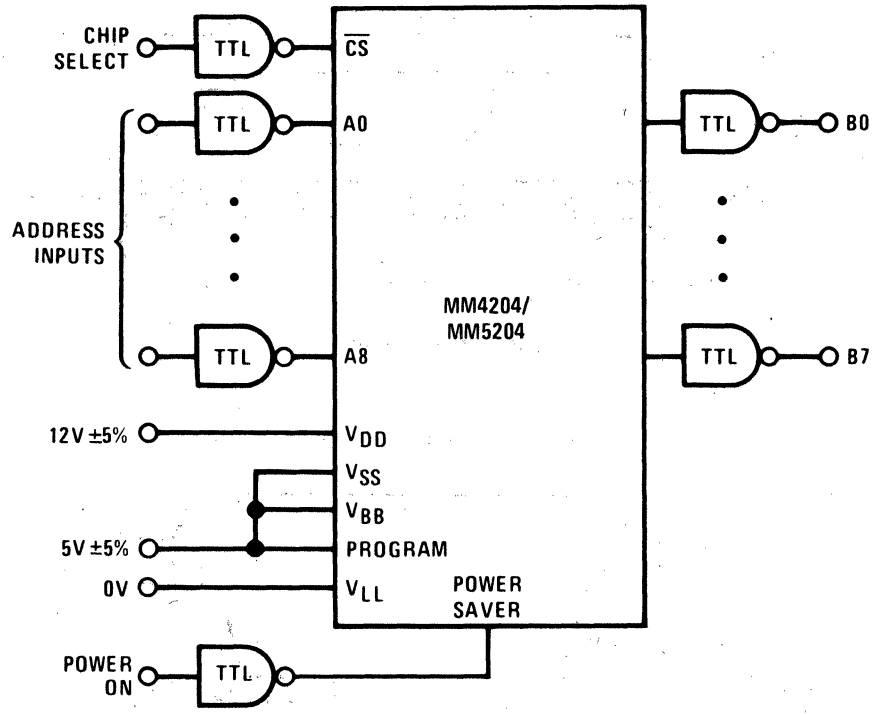


FIGURE 2. Programming Waveforms

Typical Application



5.6.10 INS8704 512 x 8 Erasable PROM

General Description

The 4096-bit (512 x 8) INS8704 is a high speed, UV erasable, and reprogrammable EPROM. It is ideally suited for applications requiring fast turn around and pattern experimentation.

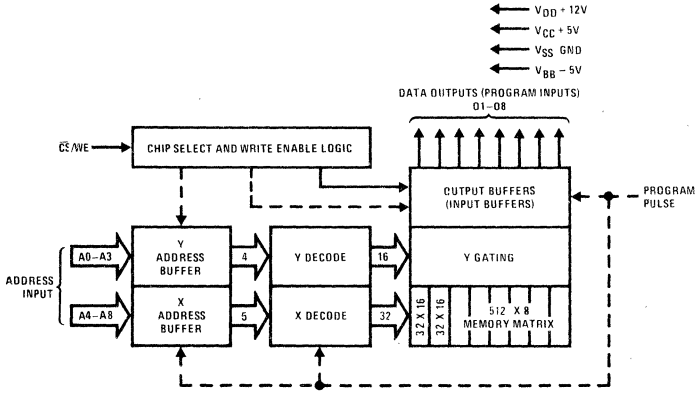
The INS8704 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultroviolet light to erase the bit pattern. A new pattern can be written into the device by following the programming procedure.

The INS8704 is fabricated with the reliable, high volume, time proven, N-channel silicon gate technology.

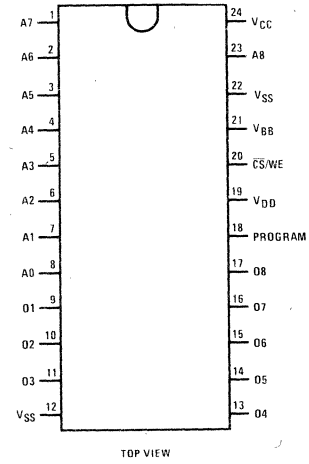
Features

- 512 x 8 Organization
- 800 mW Maximum Power
- Low Power During Programming
- Access Time - 450 ns max
- Standard Power Supplies: 12V, 5V, −5V
- Static - No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- TRI-STATE Output

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

PIN 22 MUST BE CONNECTED TO V_{SS}

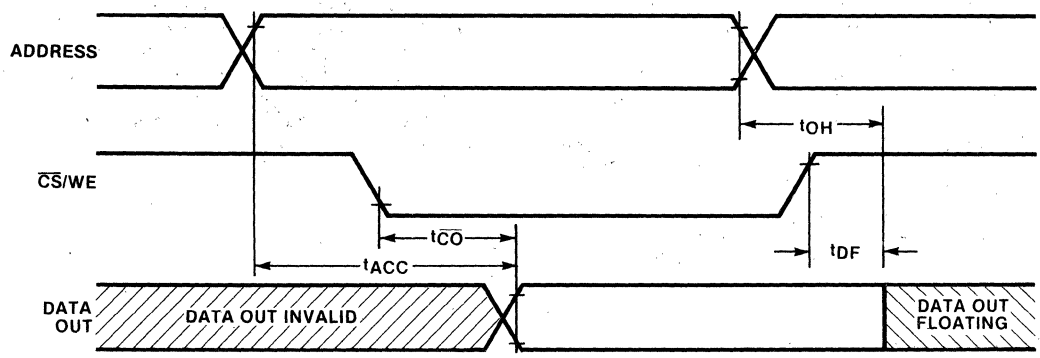
Pin Connection During Read or Program

MODE	PIN NUMBER						
	9–11, 13–17	12	18	19	20	21	24
Read	D_{OUT}	V_{SS}	V_{SS}	V_{DD}	V_{IL}	V_{BB}	V_{CC}
Program	D_{IN}	V_{SS}	Pulsed V_{IHP}	V_{DD}	V_{IHW}	V_{BB}	V_{CC}

Pin Description

A0–A8	Address inputs
O1–O8	Data outputs
$\overline{CS}$/WE	Chip select/write enable input

Switching Time Waveforms



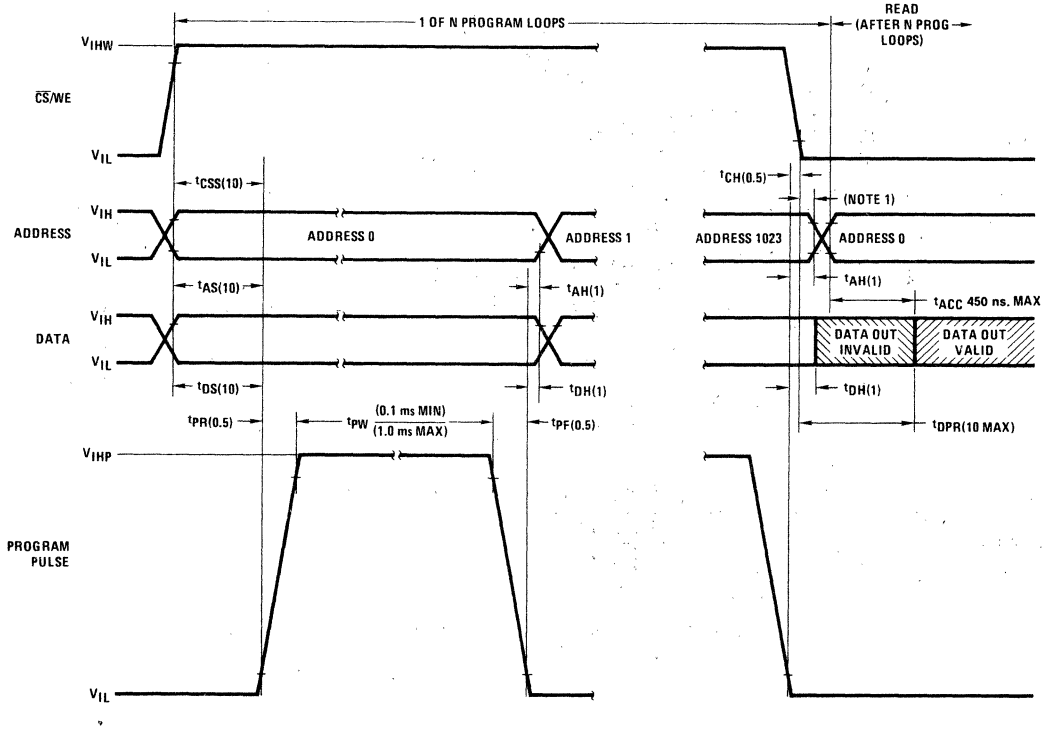
Programming Instructions

Initially, and after each erasure, all bits of the INS8704 are in the "1" state (output high). Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The circuit is set up for programming operation by raising the $\overline{CE}$/WE input (pin 20) to + 12V. The word address is selected in the same manner as in the read mode. Data to be programmed are presented, 8 bits in parallel, to the data output lines (01-08). Logic levels for address and data lines and the supply voltages are the same as for the read mode. After address and data set up, one program pulse per address is applied to the program input (pin 18). One pass through all addresses is defined as a program loop. The number of loops (N) required is a function of the program pulse width (t_{PW}) according to N x $t_{PW} \geq 100$ ms.

The width of the program pulse is from 0.1 to 1 ms. The number of loops (N) is from a minimum of 100 (t_{PW} = 1 ms) to greater than 1000 (t_{PW} = 0.1 ms). There must be N successive loops through all 512 addresses. *It is not permitted to apply N program pulses to an address and then change to the next address to be programmed.* Caution should be observed regarding the end of a program sequence. The $\overline{CS}$/WE falling edge transition must occur before the first address transition when changing from a program to a read cycle. The program pin should also be pulled down to V_{IPL} with an active instead of a passive device. This pin will source a small amount of current (I_{IPL}) when $\overline{CS}$/WE is at V_{IHW} (12V) and the program pulse is at V_{ILP}.

Programming Waveforms



Note 1: The $\overline{CS}$/WE transition must occur after the program pulse transition and before the address transition.

Note 2: Numbers in parentheses indicate minimum timing in microseconds unless otherwise specified.

5.6.11 INS8708A 1024 x 8 Erasable PROM

General Description

The 8192-bit (1024 x 8) INS8708A is a high speed, UV erasable, and reprogrammable EPROM. It is ideally suited for applications requiring fast turnaround and pattern experimentation.

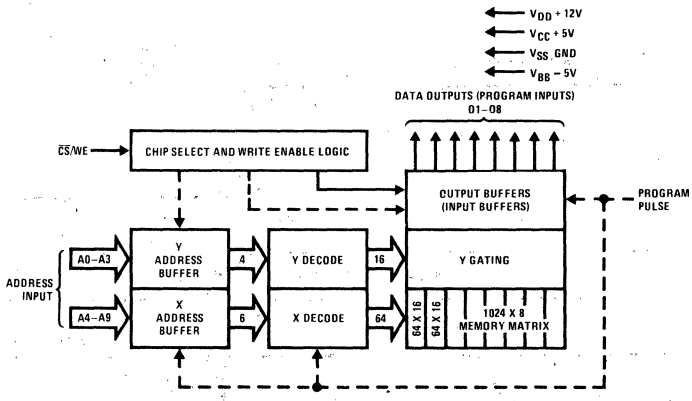
The INS8708A is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can be written into the device by following the programming procedure.

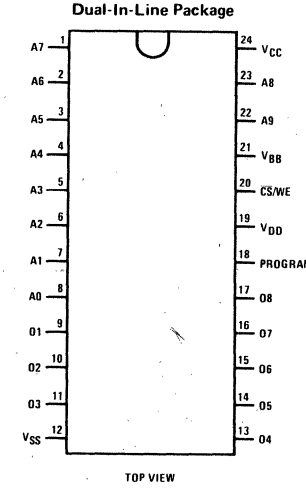
The INS8708A is fabricated with the reliable, high volume, time proven, N-channel silicon gate technology.

Features

- 1024 x 8 Organization
- 800 mW Maximum Power
- Low Power During Programming
- Access Time - 450 ns Max
- Standard Power Supplies: 12V, 5V, −5V
- Static - No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- TRI-STATE Output

Block and Connection Diagrams





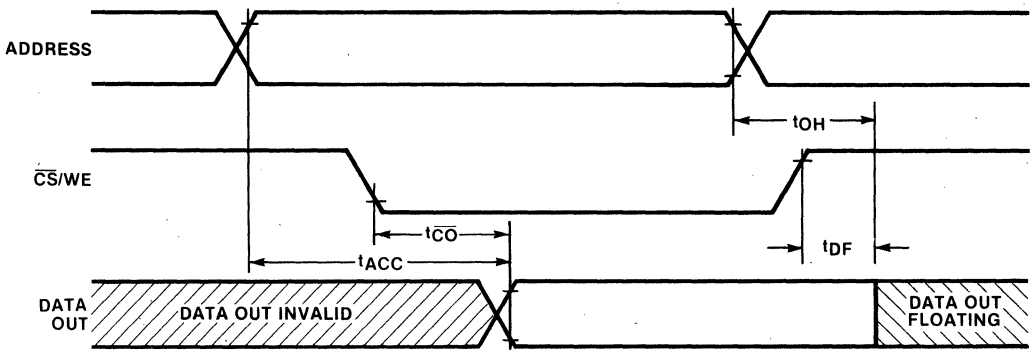
Pin Connection During Read or Program

MODE	PIN NUMBER						
	9–11, 13–17	12	18	19	20	21	24
Read	D_{OUT}	V_{SS}	V_{SS}	V_{DD}	V_{IL}	V_{BB}	V_{CC}
Program	D_{IN}	V_{SS}	Pulsed V_{IHP}	V_{DD}	V_{IHW}	V_{BB}	V_{CC}

Pin Description

A0–A9	Address inputs
O1–O8	Data outputs
$\overline{CS}$/WE	Chip select/write enable input

Switching Time Waveforms



5

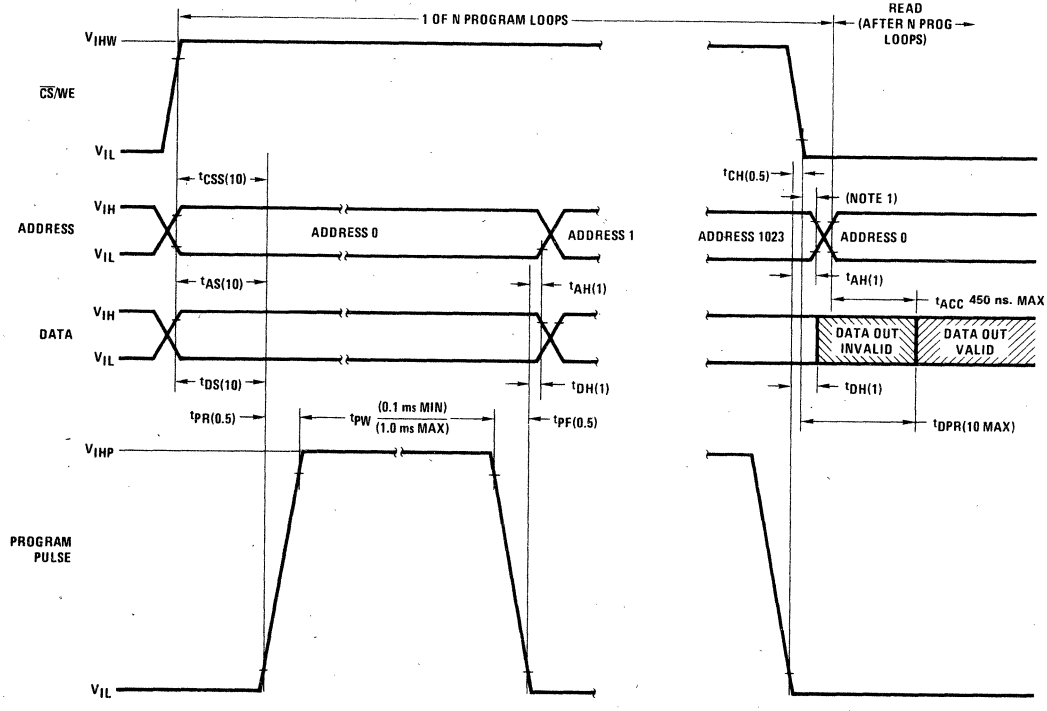
Programming Instructions

Initially, and after each erasure, all bits of the INS8708A are in the "1" state (output high). Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The circuit is set up for programming operation by raising the $\overline{CE}$/WE input (pin 20) to + 12V. The word address is selected in the same manner as in the read mode. Data to be programmed are presented, 8 bits in parallel, to the data output lines (01-08). Logic levels for address and data lines and the supply voltages are the same as for the read mode. After address and data set up, one program pulse per address is applied to the program input (pin 18). One pass through all addresses is defined as a program loop. The number of loops (N) required is a function of the program pulse width (t_{PW}) according to N x $t_{PW} \geq$ 100 ms.

The width of the program pulse is from 0.1 to 1 ms. The number of loops (N) is from a minimum of 100 (t_{PW} = 1 ms) to greater than 1000 (t_{PW} = 0.1 ms). There must be N successive loops through all 1024 addresses. *It is not permitted to apply N program pulses to an address and then change to the next address to be programmed.* Caution should be observed regarding the end of a program sequence. The $\overline{CS}$/WE falling edge transition must occur before the first address transition when changing from a program to a read cycle. The program pin should also be pulled down to V_{ILP} with an active instead of a passive device. This pin will source a small amount of current (I_{PL}) when $\overline{CS}$/WE is at V_{IHW} (12V) and the program pulse is at V_{ILP}.

Programming Waveforms



Note 1: The $\overline{CS}$/WE transition must occur after the program pulse transition and before the address transition.

Note 2: Numbers in parentheses indicate minimum timing in microseconds unless otherwise specified.

5.6.12 MM4242/MM5242 1024 x 8-BIT ROM

General Description

These static, 8192-bit ROMs are fabricated using N-Channel enhancement and depletion mode silicon gate technology. This provides complete DTL/TTL compatibility and single power supply operation.

Chip select inputs control the TRI-STATE® outputs and allow for memory expansion. The chip select code is programmed at the same time as the memory matrix and a code of 1:16 for the MM4242/MM5242 must be selected.

Applications

- Microprogramming
- Control Logic
- Random Logic Synthesis
- Table Lookup

Features

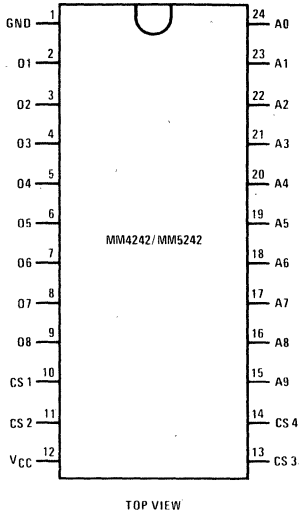
- Fully Decoded
- Single +5V Supply
- All Inputs and Outputs Directly DTL/TTL Compatible
- Static Operation
- TRI-STATE Outputs for Bus Interface
- Programmable Chip Selection
- Maximum Access Time 450 ns
- Pin Compatible with National's 4K and 16K ROMs

	Military	Commercial	Organization	Package
MM4242	X		1024 x 8	J
MM5242		X	1024 x 8	N, J

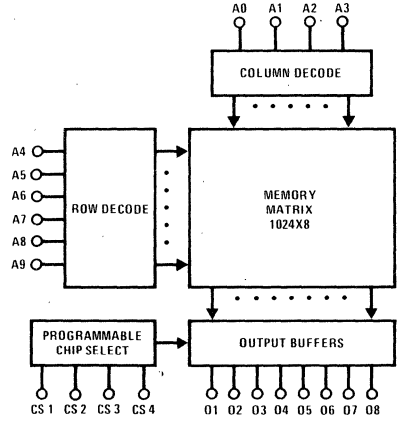
5

Connection and Block Diagrams

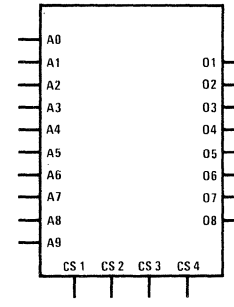
Dual-In-Line Package



TOP VIEW



Logic Symbol



Custom ROM Programming

Custom ROM programs are submitted to National in three formats: paper tape, punched cards, or truth table, with punched cards being the preferred. These programs are converted into machine language and outputted on a magnetic tape. This magnetic tape is used to make the programmable mask and the test tape. The wafers are tested at the wafer level. The wafer is then scribed and the good dice assembled. After assembly, the units are tested using the custom test tape to assure the correct output pattern for every address.

National has programs to convert NEGATIVE logic to POSITIVE or POSITIVE to NEGATIVE so ROMs can be entered in either logic, but the customer must specify which logic definition is used.

PROGRAMMING DEFINITIONS

Logic Definitions

NEGATIVE Logic: "0" = V_H = the more positive voltage. "1" = V_L = the more negative voltage.

POSITIVE Logic: "0" = V_L = the more negative voltage. "1" = V_H = the more positive voltage.

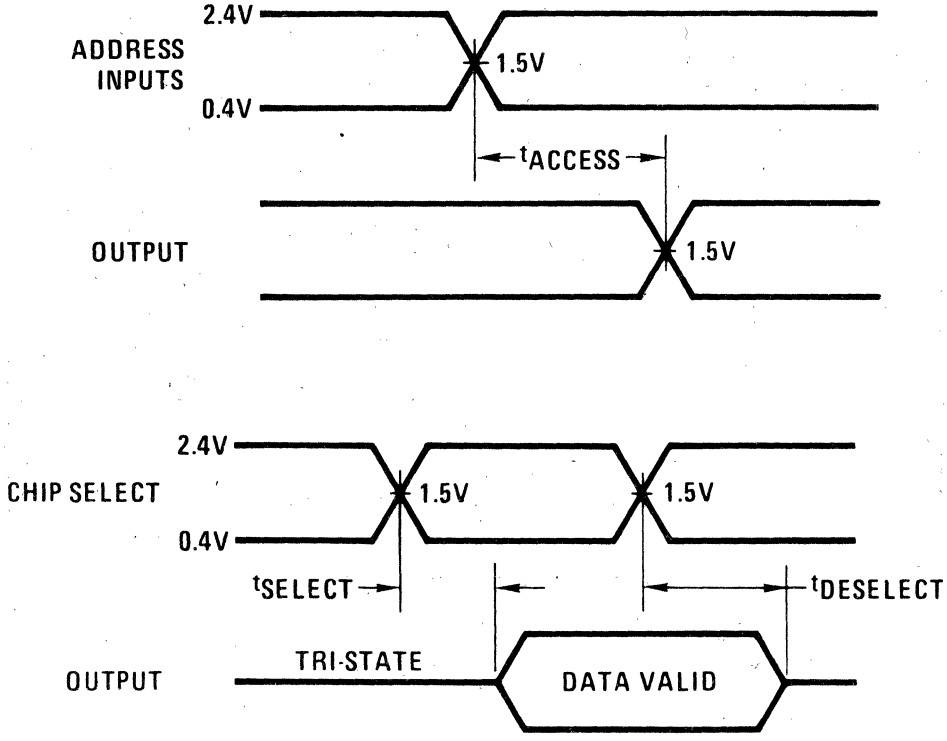
Input/Output Definitions

Address: AO is the least significant input address.

Outputs: 01 is the least significant output.

Custom ROM Programming

Switching Time Waveforms



5.6.13 INS8316A/E 16K (2048 x 8) ROM

General Description

The INS8316 is a static MOS 16,384-bit read-only memory organized in a 2048-word-by-8-bit format. It is fabricated using N-channel enhancement and depletion-mode silicon-gate technology which provides complete DTL/TTL compatibility and a single power-supply operation.

Three programmable chip selects controlling the TRI-STATE® outputs allow for memory expansion.

Programming of the memory array and chip-select active levels is accomplished by changing one mask during fabrication.

Features

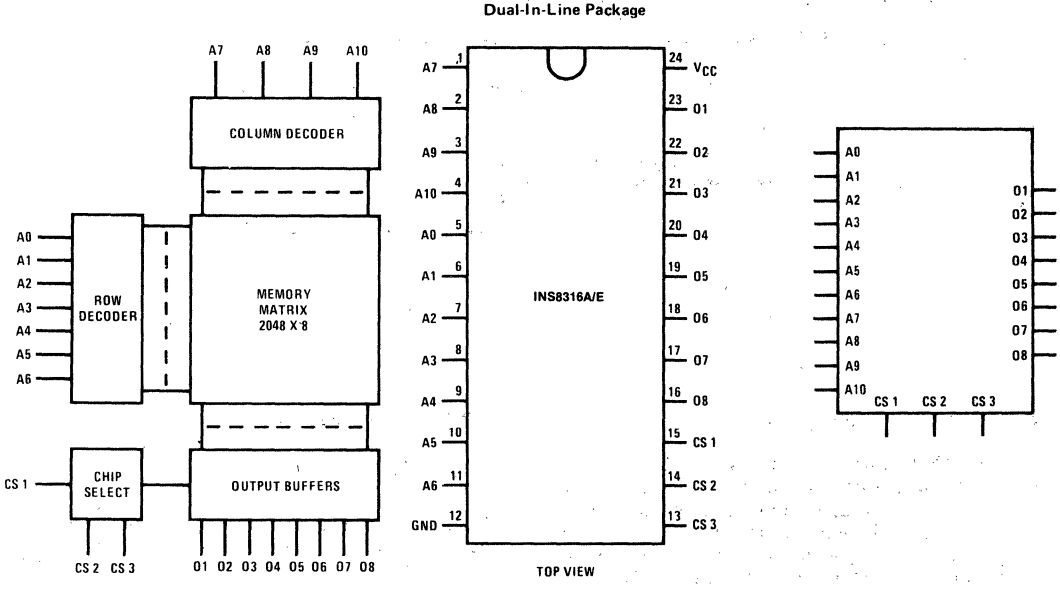
- Fully Decoded
- Single 5V Power Supply
- Inputs and Outputs TTL Compatible
- Static Operation
- TRI-STATE Outputs for Bus Interface
- Programmable Chip Selects
- 2048 Word by 8-bit Organization
- Maximum Access Time - 450 ns

Applications

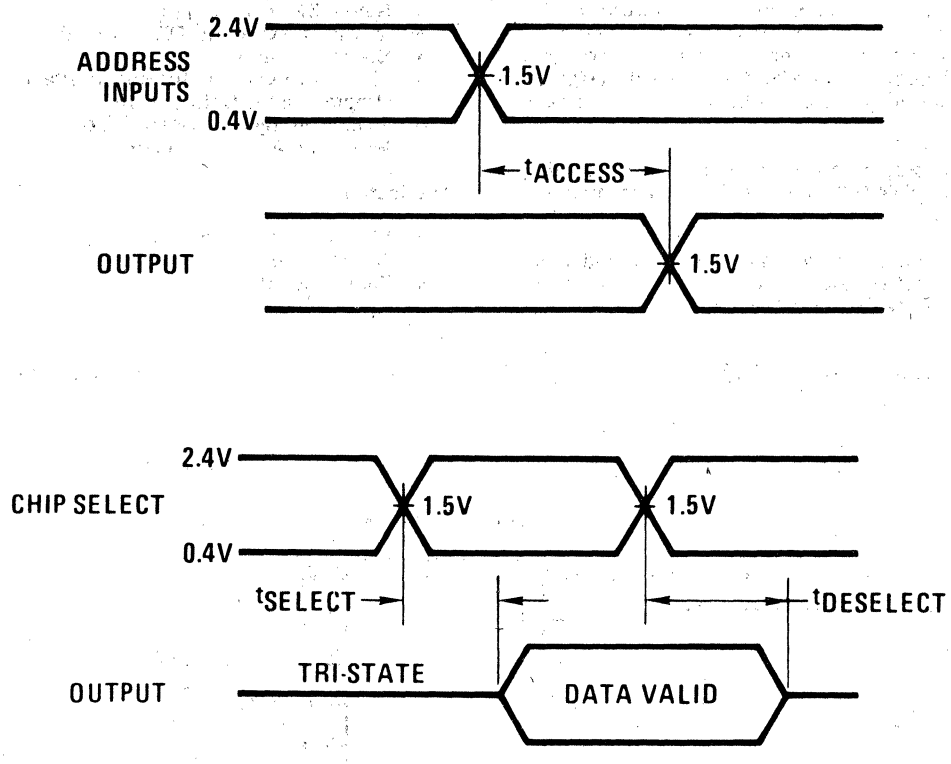
- Microprogramming
- Control Logic
- Table Look-Up

Block and Connection Diagrams

Logic Symbol



Switching Time Waveforms



Custom ROM Programming

Custom ROM programs are submitted to National in three formats: paper tape, punched cards, or truth table, with punched cards being the preferred. These programs are converted into machine language and outputted on a magnetic tape. This magnetic tape is used to make the programmable mask and the test tape. The wafers are tested at the wafer level. The wafer is then scribed and the good dice assembled. After assembly, the units are tested using the custom test tape to assure the correct output pattern for every address.

National has programs to convert NEGATIVE logic to POSITIVE or POSITIVE to NEGATIVE so ROMs can be entered in either logic, but the customer must specify which logic definition is used.

PROGRAMMING DEFINITIONS

Logic Definitions

NEGATIVE Logic: "0" = V_H = the more positive voltage. "1" = V_L = the more negative voltage.

POSITIVE Logic: "0" = V_L = the more negative voltage. "1" = V_H = the more positive voltage.

Input/Output Definitions

Address: A0 is the least significant input address.

Outputs: 01 is the least significant output.

Custom ROM Programming

5.6.14 INS8332E/MM52132 MAXI-ROM™ 32,768-Bit Read Only Memory

General Description

The MM52132 is a static MOS 32,768-bit read-only memory organized in a 4096-word-by-8-bit format. It is fabricated using N-channel enhancement and depletion-mode technology which provides complete DTL/TTL compatibility and single power-supply operation.

Two programmable chip selects controlling the TRI-STATE® outputs allow for memory expansion.

Programming of the memory array and chip-select active levels is accomplished by changing two masks during fabrication.

Features

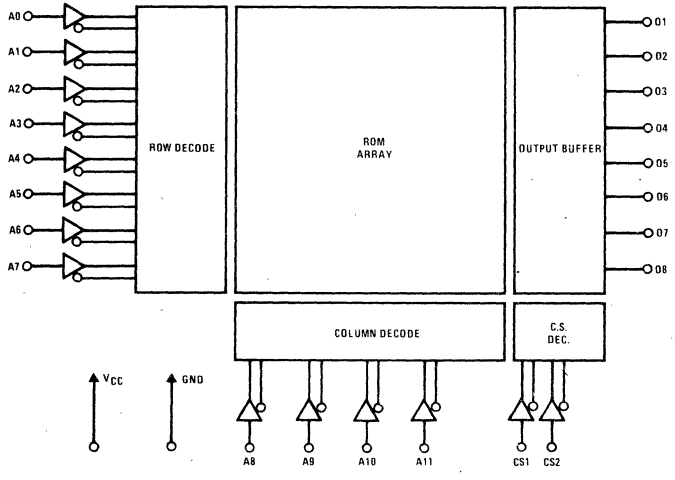
- Fully Decoded
- Single 5V Power Supply ±10% Tolerance
- Inputs and Outputs TTL Compatible
- Outputs Drive 2 TTL Loads and 100pF
- Static Operation
- TRI-STATE Outputs for Bus Interface
- Programmable Chip Selects
- 4096-Word-by-8-Bit Organization
- Maximum Access Time - 450 ns
- Industry Standard Pin Outs

Applications

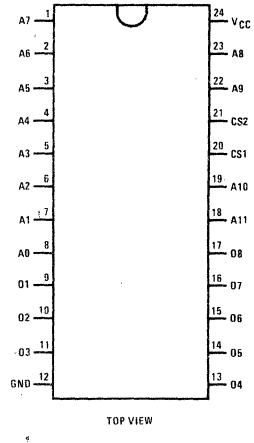
- Microprocessor Instruction Store
- Control Logic
- Table Look-Up

5

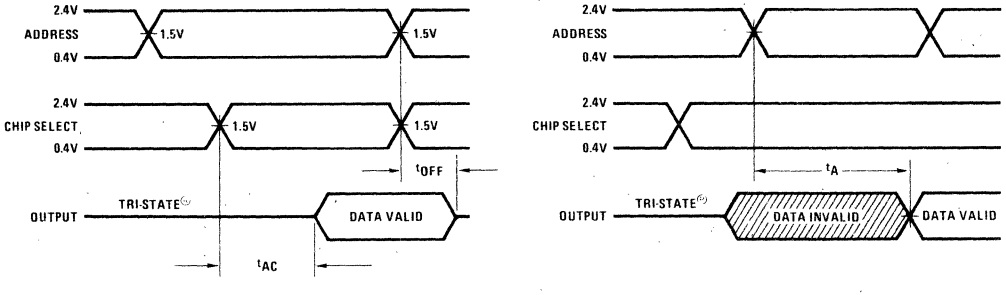
Block and Connection Diagrams



Dual-In-Line Package



Switching Time Waveforms



5.6.15 INS8364E/MM52164 MAXI-ROM ™ 65,536-Bit Read Only Memory

General Description

The INS8364E/MM52164 is a static MOS 65,536-bit read-only memory organized in an 8192-word by 8-bit format. It is fabricated using N-channel enhancement and depletion-mode technology which provides complete DTL/TTL compatibility and single power-supply operation.

One programmable chip select controlling the TRI-STATE® outputs allow for memory expansions.

Programming of the memory array and chip-select active levels is accomplished by changing two masks during fabrication.

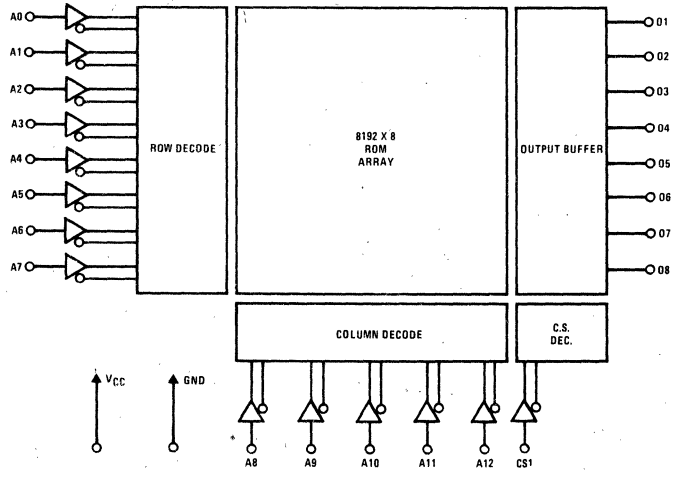
Features

- Fully Decoded
- Single 5V Power Supply ±10% Tolerance
- Inputs and Outputs TTL Compatible
- Outputs Drive 2 TTL Loads and 100pF
- Static Operation
- TRI-STATE Outputs for Bus Interface
- Programmable Chip Selects
- 8192-Word-by-8-Bit Organization
- Maximum Access Time - 450 ns
- Industry Standard Pin Outs

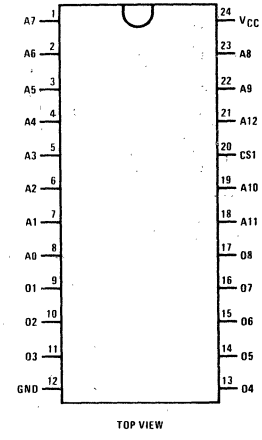
Applications

- Microprocessor Instruction Store
- Control Logic
- Table Look-Up

Block and Connection Diagrams

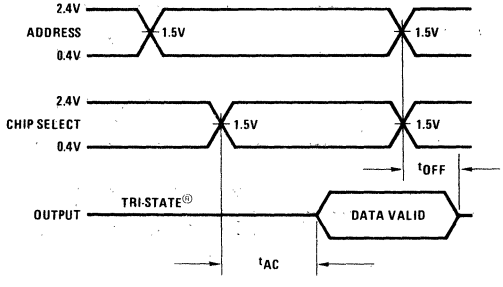


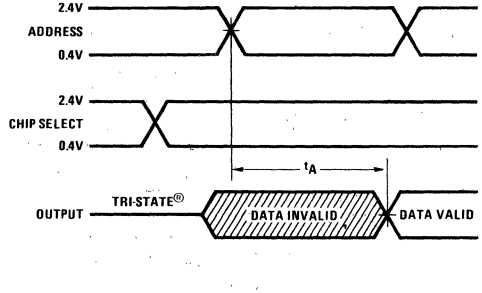
Dual-In-Line Package

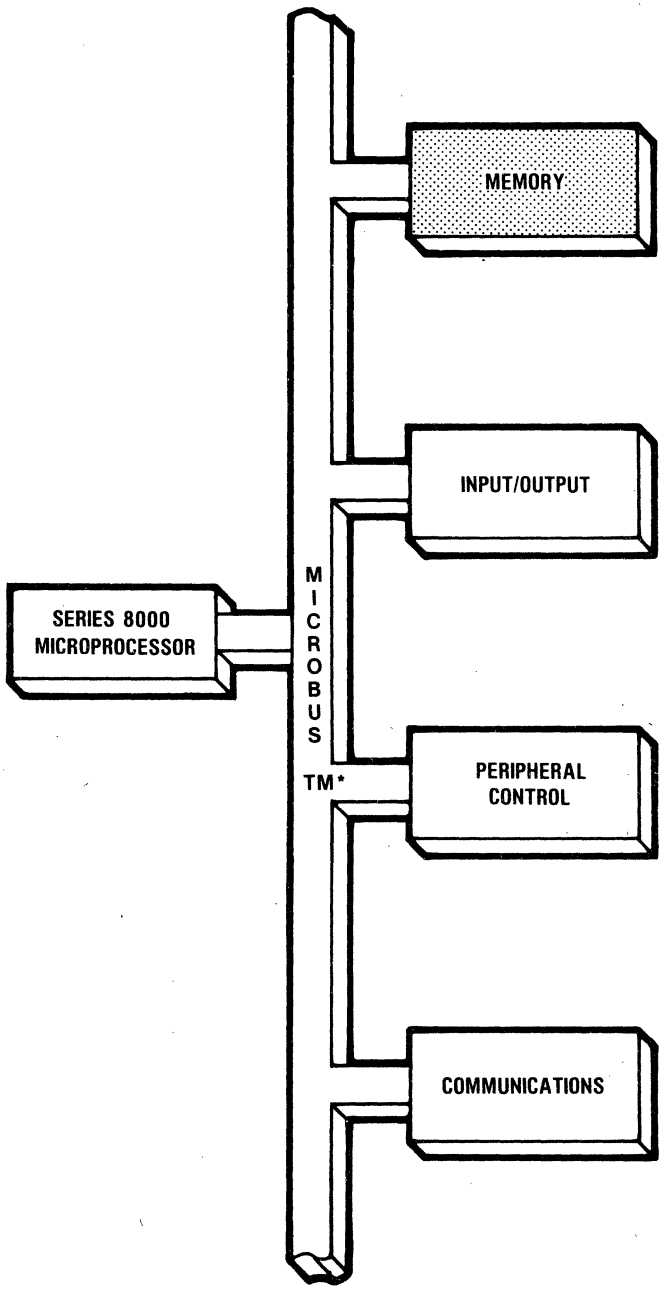


TOP VIEW

Switching Time Waveforms







Chapter 6
MAXI-ROMs

MEMORY

Part Number/Description

INS8298 E
8080A LLL Basic Interpreter
MM52132
MAXI-ROM (32K, 450 ns Access)
INS8364E/MM52164
MAXI-ROM (64K, 450 ns Access)

* Trademark, National Semiconductor Corporation

MAXI-ROMs

6.1 GENERAL DESCRIPTION

MAXI-ROMS are 32K, 64K and up static mask-programmable ROMS. This large size allows storage of complete programs, tables, etc.. Any user program or data may be mask programmed.

6.2 INTERFACING TO MEMORY

Basically, interfacing to memory is the same as any other ROM. Memory address location assignments should be coordinated with locations that the MAXI-ROM stored program requires.

6.3 UNPROGRAMMED MAXI-ROMs

Two unprogrammed MAXI-ROMs are currently available, as follows:

- MM52132 (4096 x 8 bits)
- INS8364E/MM52164 (8192 x 8 bits)

These devices can be mask-programmed with any user program or data.

6.4 INS8298E 8080A LLL BASIC INTERPRETER

The 8080A LLL BASIC interpreter operates with the 8080A microprocessor system to provide a high-level, easy-to-use language for performing both control and computational functions. Designed for use in data acquisition and control applications, the LLL BASIC interpreter enables the user to write and debug a program on-line.

The LLL BASIC interpreter (resident on the INS8298E ROM) is used to translate, debug, and execute user-written ASCII programs in read/write memory (RAM). Each statement is interpreted from its ASCII BASIC format and then executed line-by-line.

See the National Semiconductor LLL BASIC users manual for a description of the LLL BASIC language. While this manual describes the LLL BASIC language, it is not intended as a primer. Familiarity with high-level computer programming languages is assumed; familiarity with BASIC is desirable but not required. There are many excellent introductory textbooks on BASIC that should be consulted if a more tutorial approach is desired. See also the INS8298E 8080A LLL BASIC interpreter data sheet.

The BASIC interpreter accepts both program statements and control commands. Program statements describe (to the BASIC interpreter) operations to be performed on program data. A program statement preceded by a line number is inserted into the program for later execution at a spot determined by the line number. If no line number precedes the statement, it is executed immediately and then discarded. This latter mode, known as "immediate" or "direct," is especially valuble during program checkout. Control commands specify actions that alter the status of the user's program; for example, they direct the execution, saving, and retrieval of programs.

A Hexadecimal Debugging Routine (HDT) is also available on the INS8298E ROM. HDT allows the user to examine internal registers and memory locations and modify their contents. HDT is called from the BASIC interpreter to help debug user-developed software. Input and output data representation is in hexadecimal format. In addition to the usual debugging capabilities, HDT also has commands to perform the following functions:

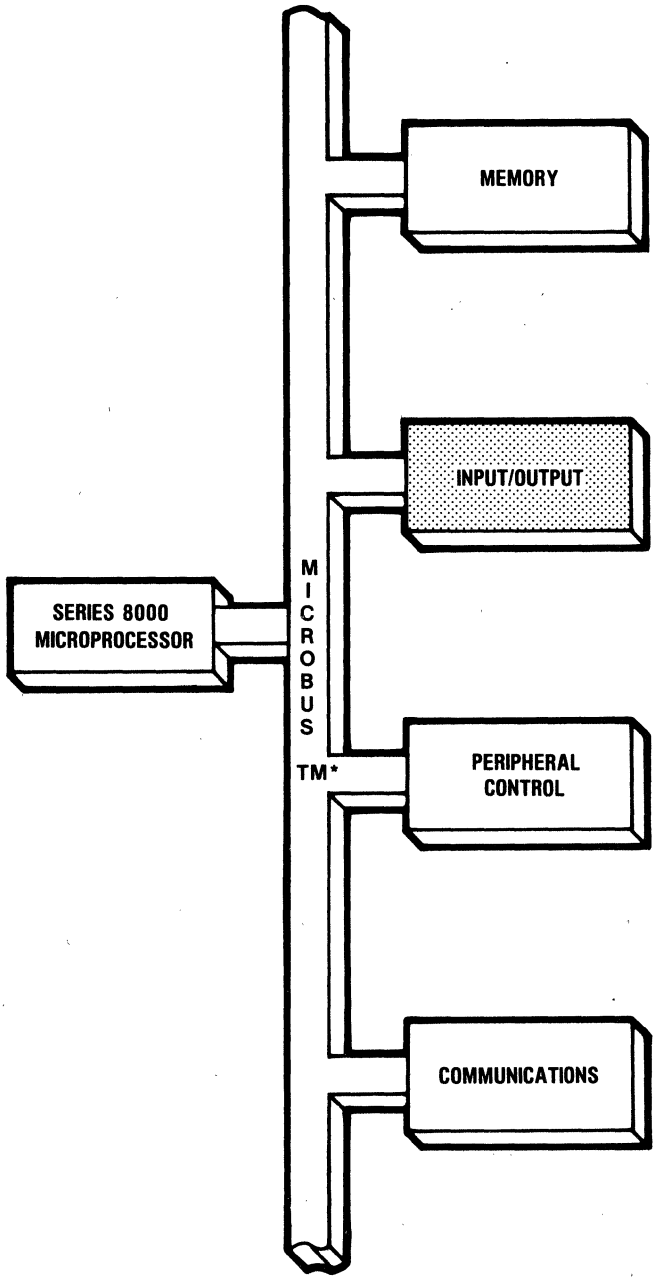
- Test a specified range of memory locations
- Load programs in hexadecimal, NSC, and LLL binary formats
- Save the contents of a specified range of memory locations

System Configuration

BASIC's internal I/O assumes a system configured in the manner of the BLC (or SBC) 80/10 or 80/20 Single-Board Computers, which use an INS8251 USART for console I/O. The data and status ports are at I/O addresses EC and ED (hex), respectively. It is also assumed that the user's system includes a monitor program (e.g., the BLC 80p Monitor) to initiate execution of BASIC and to initialize the USART.

The minimum hardware configuration required to support the LLL BASIC interpreter is as follows:

- 8080A Central Processing Unit (CPU)
- 110-Baud ASCII Terminal Interface
- INS8298E 8K-by-8 Read Only Memory (ROM)
- At least 512 bytes of Read-Write Memory (RAM) for user-written programs
- Model 33 ASR Teletype (TTY) or similar terminal
- Power Supplies (±5V, ±12V)



Chapter 7
Input/Output Components

Part Number/Description

INS8202
Tri-State 8-Bit Bus Driver

INS8203
Tri-State 8-Bit Bus Driver (Inverting)

INS8208B
8-Bit Bi-Directional Bus Driver

INS8216
4-Bit Bi-Directional Bus Driver

INS8226
4-Bit Bi-Directional Bus Driver (Inverting)

INS8212
8-Bit I/O Port

* Trademark, National Semiconductor Corporation

Input/Output Components

7.1 GENERAL DESCRIPTION

The general purpose of the Digital Input/Output components is to supplement the functions already present in other devices. Typical functions of these devices are I/O buffers, data/address latches, address decoders, and programmable I/O ports. (See also Chapter 8.)

Programmable input/output and peripheral functions enable the system designer to configure and adapt interface lines to his own requirements. In the Series 8000 family, the INS8212 8-Bit Input/Output Port, the INS8255 Programmable Peripheral Interface and the INS8251 Programmable Communication Interface (see chapter 9) can satisfy these system input/output requirements. The INS8212 is a multimode chip fabricated using National Semiconductor's Schottky bipolar technology. The device may be used to implement latches, gated buffers, or multiplexers. Thus, the chip can be used in a microcomputer system as either an address buffer, a priority interrupt arbitrator, or an input/output peripheral interface.

The INS8255 is a general-purpose programmable parallel input/output chip fabricated using the silicon gate MOS process. This device is designed to interface peripheral equipment to the 8080A system bus.

Due to the simplicity of the devices contained in this chapter, the majority of the devices will not be covered in any detail.

The digital I/O components illustrated in this section are but a small sample of those available from National Semiconductor. Detailed operational and parametric information on each of the devices is contained in Appendix D, Device Data Sheets.

7.2 INTERFACING INPUT/OUTPUT COMPONENTS

The input/output devices use the same MICROBUS for interfacing to the CPU group as the semiconductor memory components. A typical input/output interface is shown in figure 7-1. This interface enables the INS8080A Microprocessor to communicate with peripheral devices or structures such as keyboards, paper tape, floppy disks, printers, displays, data communication interfaces, sensors, relays and motor controls.

- Input/Output Addressing

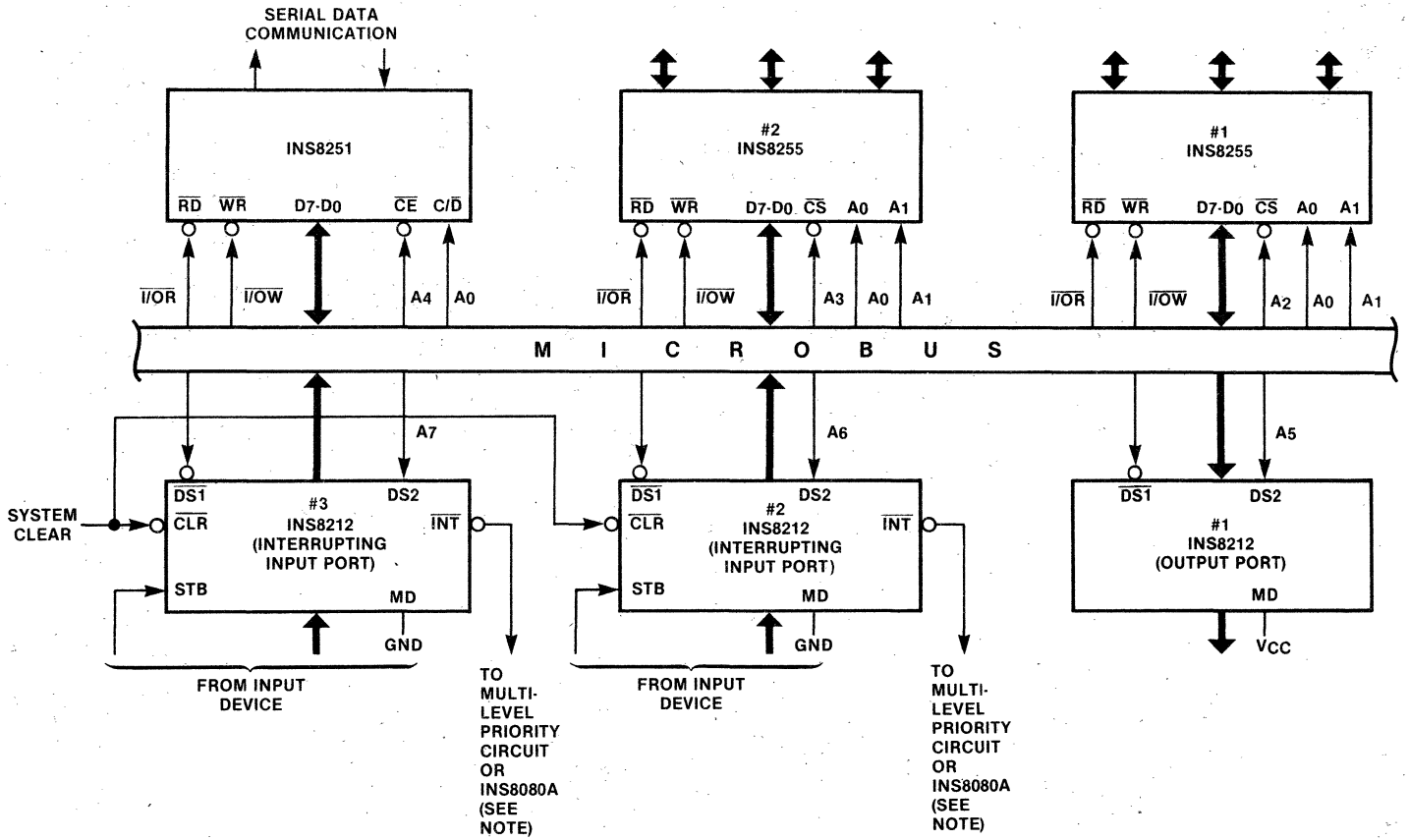
Depending on the system input/output environment, the input/output devices of the typical interface (figure 7-1) may be addressed using either the isolated input/output or memory mapped input/output technique and linear select. Thus, no decoders are required for generating chip select signals and each device has an exclusive enable bit. Figure 7-2, shows an example of how to address six National Semiconductor INS8255 Programmable Peripheral Interface devices using the isolated input/output addressing technique and linear select. In this example, the addressing format shown is the second byte of an IN or an OUT Instruction. Similarly, figure 7-3 shows an example of how to address 13 INS8255 devices using the memory mapped input/output addressing technique and linear select. In this example, the addressing format shown could be second and third bytes of any memory reference instruction that is used for the input/output devices (for example, MVI M, LDA, STA, SHLD, ADD M, ANA M, Et cetera). See chapter 11 "Programming for INS8080A instruction set.

- Interfacing 8-Bit Peripherals

As shown in the typical input/output interface of figure 7-1, two National Semiconductor INS8255 Programmable Peripheral Interface devices and three National Semiconductor INS8212 Input/Output Port devices are provided for interfacing 8-bit peripherals (keyboards, sensors, paper tape, displays, et cetera) to the system. Since each INS8255 has three ports, up to 24 bits of programmable input/output data and control signals are provided by each device. Note that the $\overline{I/O\ W}$ and $\overline{I/O\ R}$ signals from the Control Bus are used as write and read command signals for the transfer of data (D_7-D_0) to and from the INS8255 devices. Also, note that the $\overline{I/O\ W}$ signal is used in conjunction with the A_5 address bit to select the INS8212 device that functions as an output port; and that the $\overline{I/O\ R}$ signal is used in conjunction with either the A_6 or the A_7 address bit to select one of two INS8212 devices that function as interrupting input ports. The addressing formats for the INS8255 and INS8212 devices are shown in figure 7-4.

- Interfacing Serial Devices

As shown in the typical interface of figure 7-1, one National Semiconductor INS8251 Program-



NOTE: IF ONLY ONE INS8212 INTERRUPTING INPUT DEVICE IS USED, THE $\overline{INT}$ SIGNAL SHOULD BE CONNECTED TO THE INT PINOUT OF THE INS8080A VIA AN INVERTER. IN THIS WAY, A USER SELECTED SINGLE LEVEL INTERRUPT (RST 7) IS GATED ONTO THE INS8080A DATA BUS WITH A HIGH-LEVEL DBIN SIGNAL, WHEN THE INTERRUPT REQUEST IS ACKNOWLEDGED.

Figure 7-1 Typical Input/Output Interface

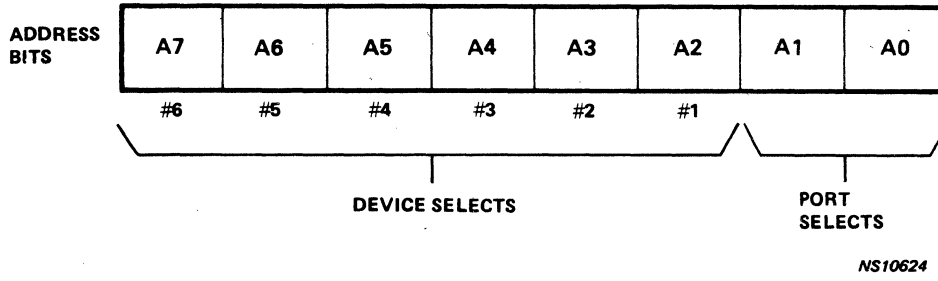


Figure 7-2. Example of Addressing INS8255 Devices Using Isolated Input/Output Technique and Linear Select

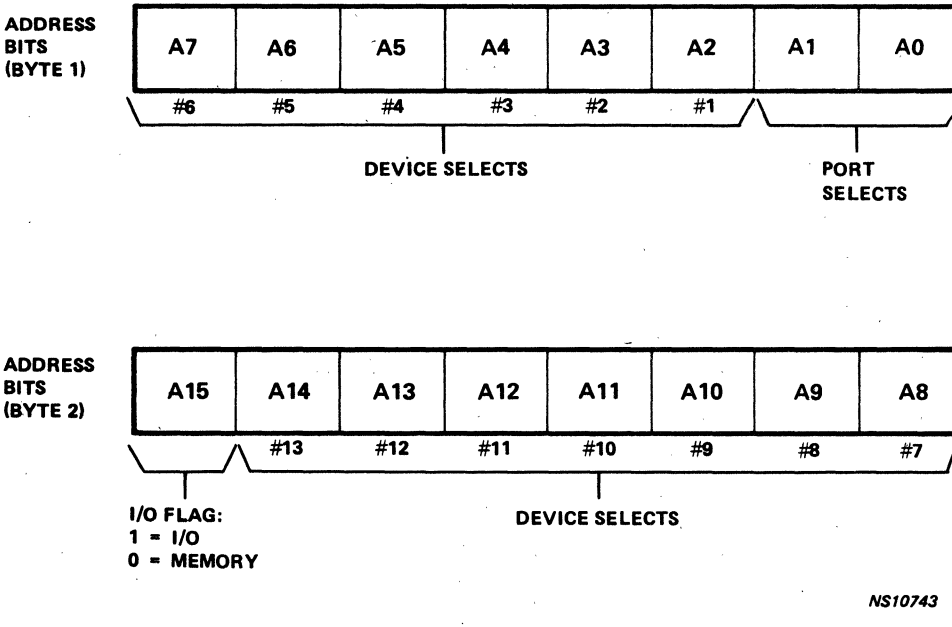


Figure 7-3. Example of Addressing INS8255 Devices Using Memory Mapped Input/Output Technique and Linear Select

mable Communication Interface device is provided for interfacing serial data devices (MODEMs, communications links, et cetera) to the system. Note that the $\overline{I/O\ W}$ and $\overline{I/O\ R}$ signals are also used as write and read command signals for the transfer of data to and from the INS8251 device. The addressing format for the INS8251 is shown in figure 7-5.

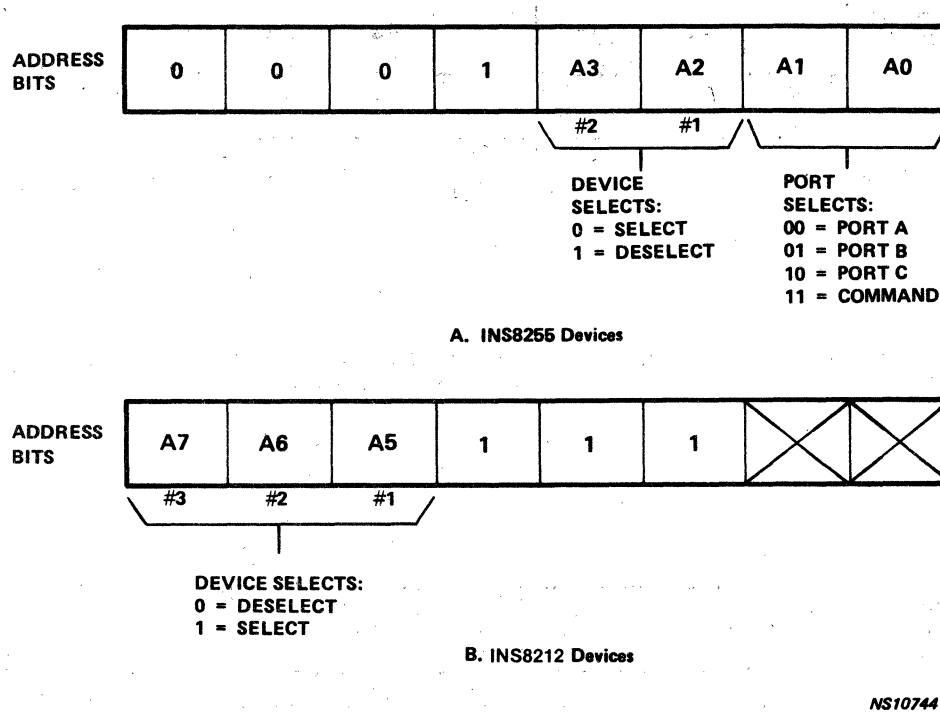


Figure 7-4. Addressing Format for INS8255 and INS8212 Devices

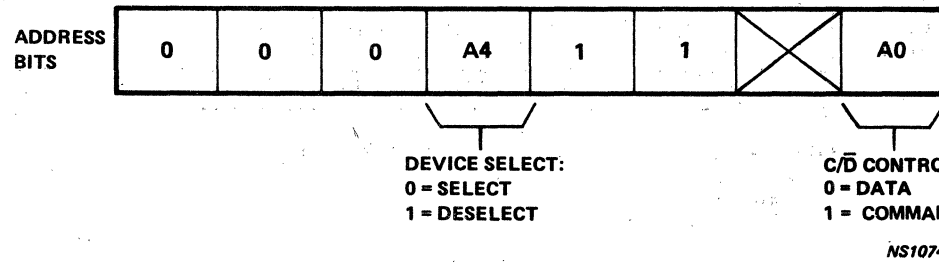


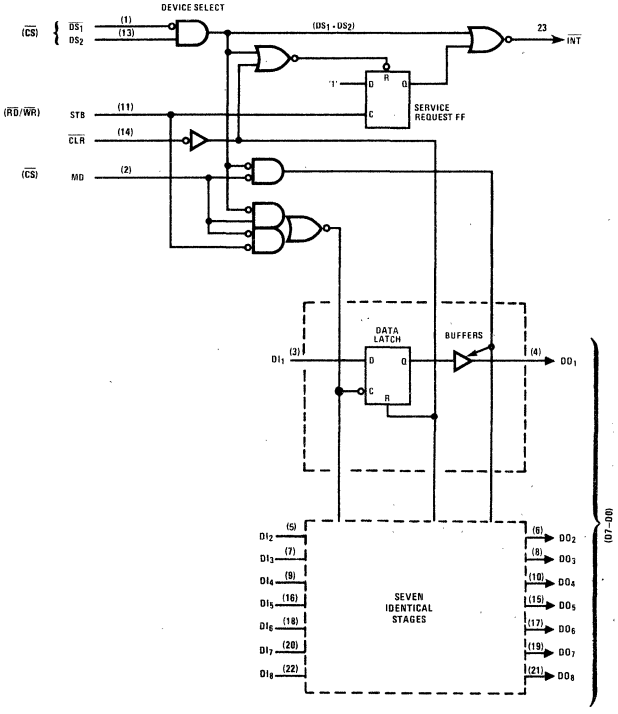
Figure 7-5. Addressing Format for INS8251 Device

7.3 INS8212 8-BIT INPUT/OUTPUT PORT

The INS8212 is an 8-bit input/output port that implements the major peripheral and input/output functions of the 8080A microprocessor system. The INS8212 includes an 8-bit latch with TRI-STATE output buffers, device selection and control logic, and a service request flip-flop for the generation and control of interrupts to the microprocessor.

Features

- 8-bit Data Latch/Buffer
- Service Request Flip/Flop
- TRI-STATE Outputs



Logic Table A

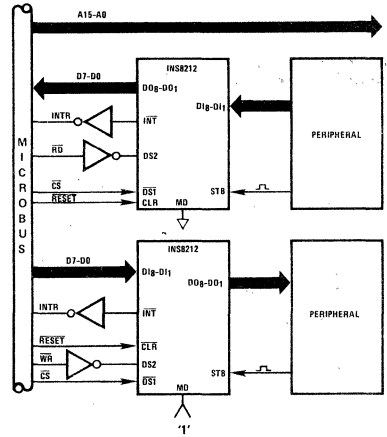
STB	MD	$(DS_1 \cdot DS_2)$	DATA OUT EQUALS
0	0	0	TRI-STATE
1	0	0	TRI-STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

$\overline{CLR}$ resets data latch to the output low state.

Logic Table B

$\overline{CLR}$	$(DS_1 \cdot DS_2)$	STB	Q*	$\overline{INT}$
0 RESET	0	0	0	1
1	0	0	0	1
1	0	0	0	0
1	1 RESET	0	0	0
1	0	0	0	1

*Internal Service Request flip-flop

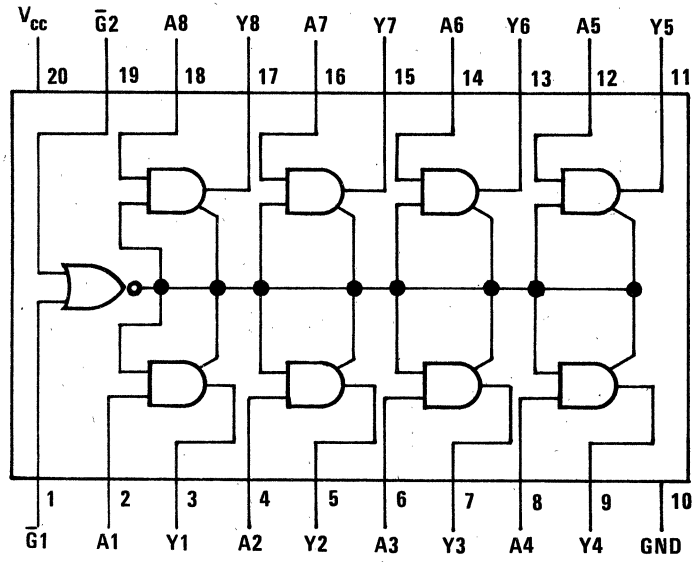


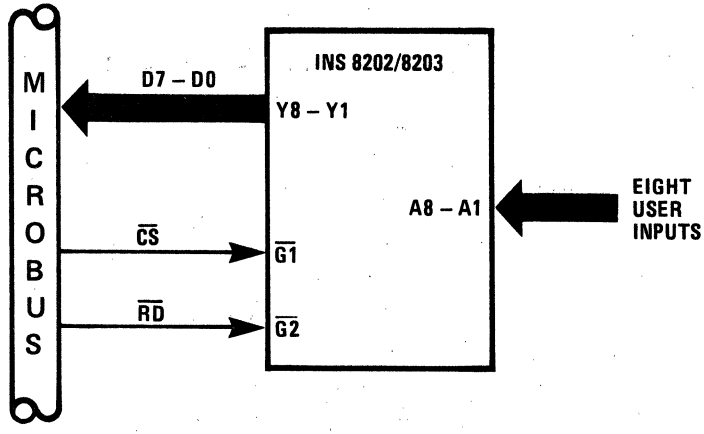
7.4 INS8202/8203 TRI-STATE OCTAL BUFFERS

These devices provide eight buffers in each package. A control line to each buffer gates the output into the TRI-STATE mode. The INS8202 contains non-inverting buffers while the INS8203 contains inverting buffers. The application shown utilizes the INS8202/8203 as a MICROBUS driver.

Features

- Low Power
- High Speed
- TRI-STATE Outputs





7.5 INS8208B 8-BIT BIDIRECTIONAL BUS DRIVER

General Description

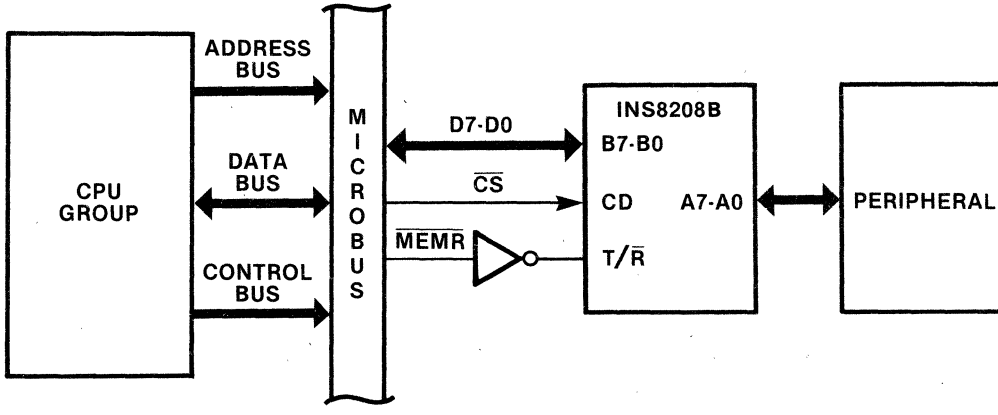
The INS8208B is an 8-bit TRI-STATE® low power Schottky transceiver. It provides bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with low power Schottky drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

One input, Transmit/$\overline{\text{Receive}}$, determines the direction of logic signals through the bidirectional transceiver: Transmit enables data from A ports to B ports: $\overline{\text{Receive}}$ enables data from B ports to A ports. The Chip Disable input disables both A and B ports by placing them in a TRI-STATE® condition.

The output high voltage (V_{OH}) is specified at 3.6V minimum to allow interfacing microprocessors, TTL, MOS, CMOS, RAM, or ROM.

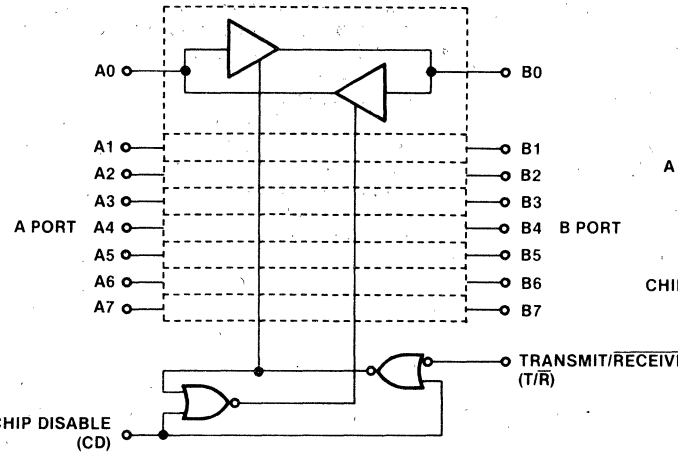
Features

- 8-Bit Bidirectional Data Flow Reduces System Package Count
- Bidirectional TRI-STATE® Inputs/Outputs Interface with Bus-Oriented Systems
- PNP Inputs Reduce Input Loading
- 3.6V Output High Voltage Interfaces with TTL, MOS, and CMOS
- 48mA/300pF Bus Drive Capability
- Pinouts Simplify System Interconnections
- Transmit/$\overline{\text{Receive}}$ and Chip Disable Simplify Control Logic
- Compact 20-Pin Dual-In-Line Package
- MICROBUS Compatible



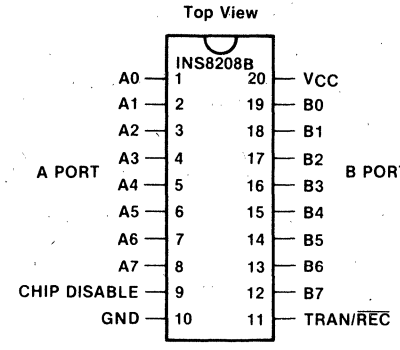
INS8208B MICROBUS Configuration

Logic and Connection Diagrams



NOTE: INS8208 B identical to DP8304

Top View

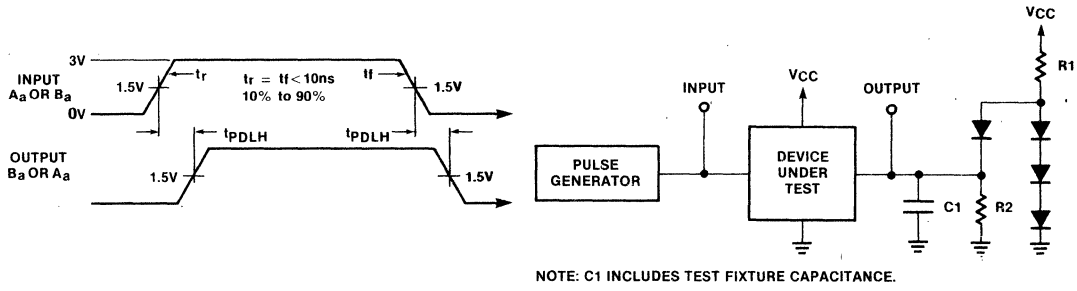


Logic Table

Inputs		Resulting Conditions	
Chip Disable	**Transmit/Receive**	**A Port**	**B Port**
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

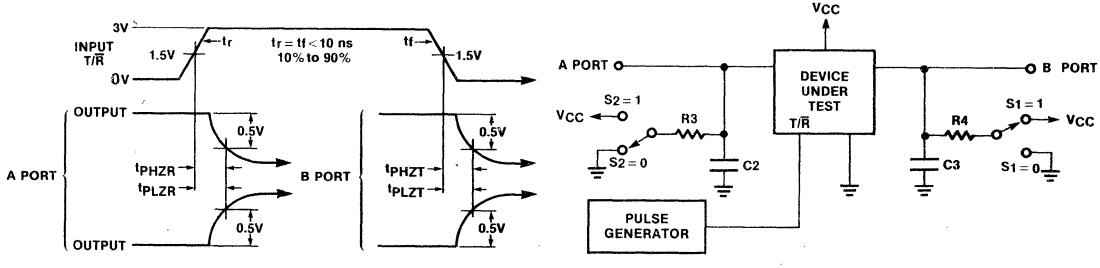
X = Don't Care

Switching Time Waveforms and AC Test Circuits



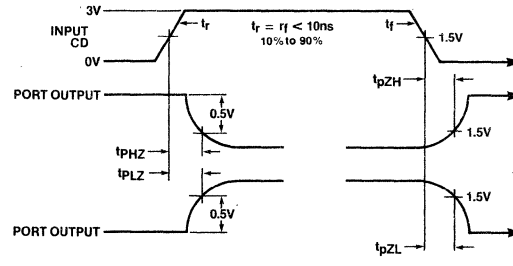
NOTE: C1 INCLUDES TEST FIXTURE CAPACITANCE.

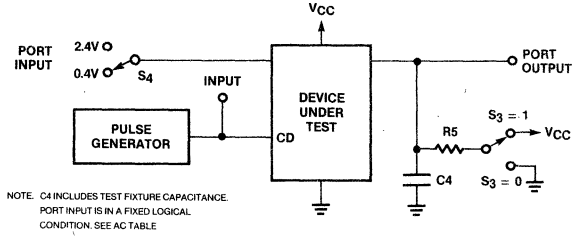
Propagation Delay from A Port to B Port or from B Port to A Port



NOTE: C2 AND C3 INCLUDE TEST FIXTURE CAPACITANCE

Propagation Delay from $T/\overline{R}$ to A Port or B Port





NOTE. C4 INCLUDES TEST FIXTURE CAPACITANCE. PORT INPUT IS IN A FIXED LOGICAL CONDITION. SEE AC TABLE

Propagation Delay to/from TRI-STATE® from CD to A Port or B Port

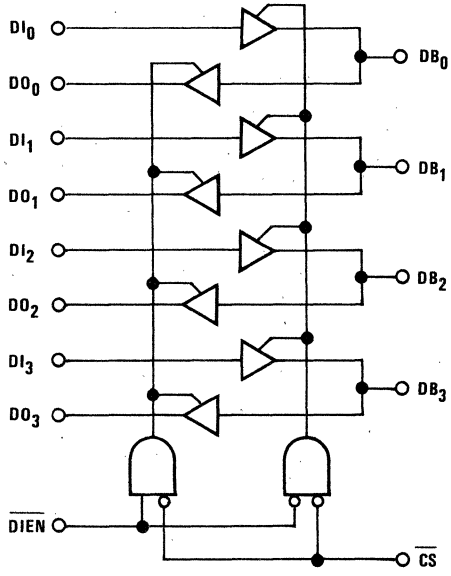
7

7.6 INS8216/8226 4-BIT BIDIRECTIONAL BUS DRIVER

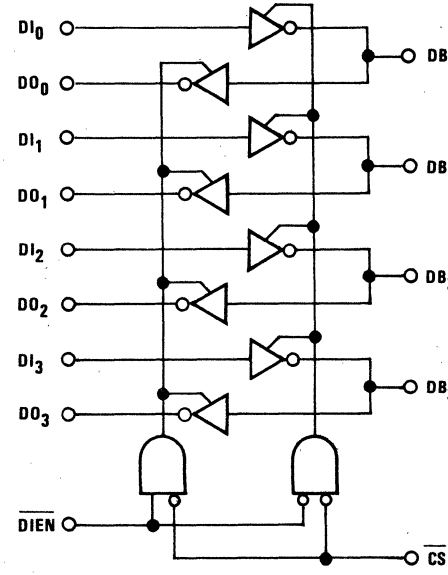
The INS8216/8226 are 4-bit bidirectional bus drivers for bus-oriented systems. Each line of the driver consists of two separate TRI-STATE buffers. On one side of the driver the output of one buffer and the input of the other are tied together to create a bidirectional TTL port for a system bus. The other side of the port has both a separate input and a separate output to provide for maximum system flexibility. The INS8216 contains non-inverting buffers and the INS8226 contains inverting buffers.

Features

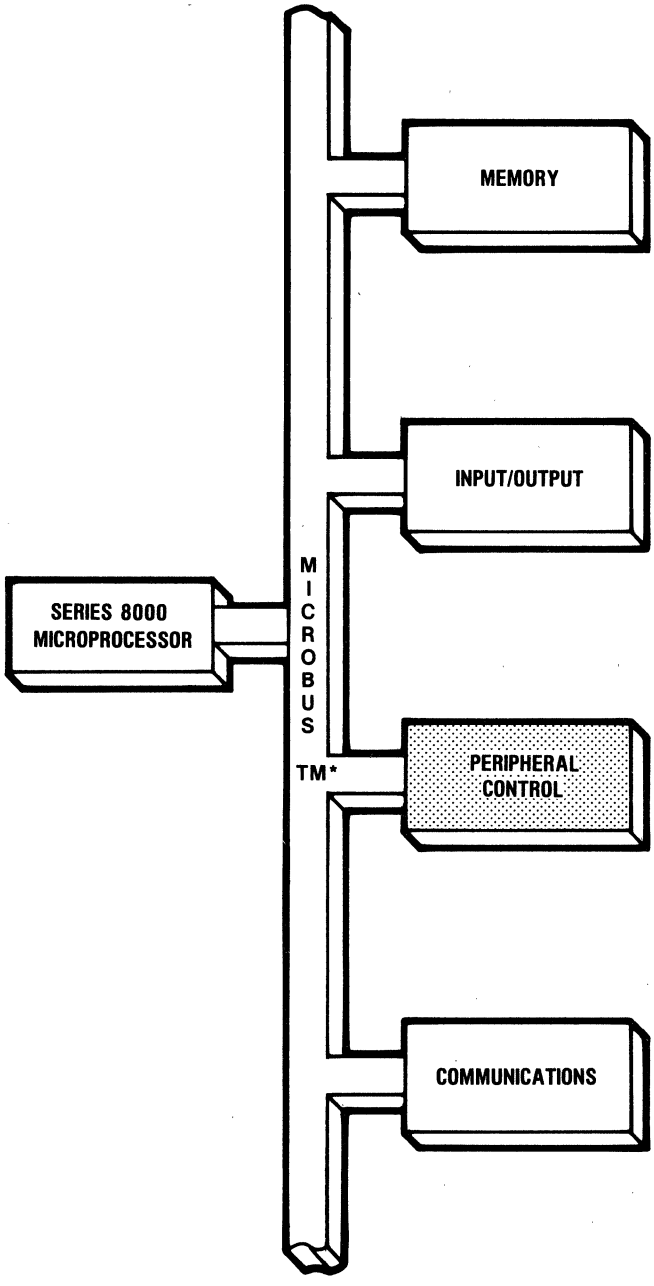
- Low Input Load Current
- High Bus Drive Capability
- TRI-STATE Outputs
- Inverting or Non-Inverting Outputs
- MOS compatible High-Voltage Outputs



INS8216



INS8226



Chapter 8
Peripheral Control Components

Part Number/Description

DP8350
Programmable CRT Controller
INS1771-1
Floppy Disk Formatter/Controller
INS8244
90-Key Keyboard Encoder
INS8245
16-Key Keyboard Encoder
INS8246
20-Key Keyboard Encoder
INS8247
4-Digit Display Controller
INS8248
6-Digit Display Controller
INS8253
3-16 bit Programmable Interval Timers
INS8285
Character Generator
INS8292
8-Bit A/D Converter with 16-Channel Analog MUX
INS8294
3¾-Digit DVM with Multiplexed BCD Output

* Trademark, National Semiconductor Corporation

Peripheral Control Components

8.1 GENERAL DESCRIPTION

The Series 8000 Microprocessor Family peripheral control components provide the interface between the microcomputer system and its commonly used peripherals (or the man-machine interface to the microcomputer). Being software programmable, these components are able to provide complex control functions that eliminate most of the discrete devices previously needed to implement the controlling functions.

The components contained in this chapter provide complex control functions for some commonly used peripherals. Thanks to Large Scale Integration, these devices allow both a reduced system chip count and reduced system design time, particularly because these devices are MICROBUS compatible. Due to the extreme flexibility of the INS8080A Instruction set, these peripheral control devices may be used as either memory mapped I/O or as peripherals (using the INS8080A I/O Control Group Instructions).

Detailed information on use of the Series 8000 Microprocessor Family Peripheral Control Components is contained in the following sections. Parametric information for the components is located in appendix D, Device Data Sheets.

8.2 INTERFACING THE PERIPHERAL CONTROL COMPONENTS

Figure 8-1, illustrates the general interfacing of peripheral control components. Most controlled devices will be interfaced directly with the associated peripheral control component.

Optional circuits might be used for interfacing to Special devices or to Enhance device capability.

8.3 KEYBOARD ENCODERS/DISPLAY CONTROLLERS

A variety of keyboard encoders are available from a 16-key CMOS device up to a 90-key MOS/LSI device. All have TRI-STATE*TM outputs.

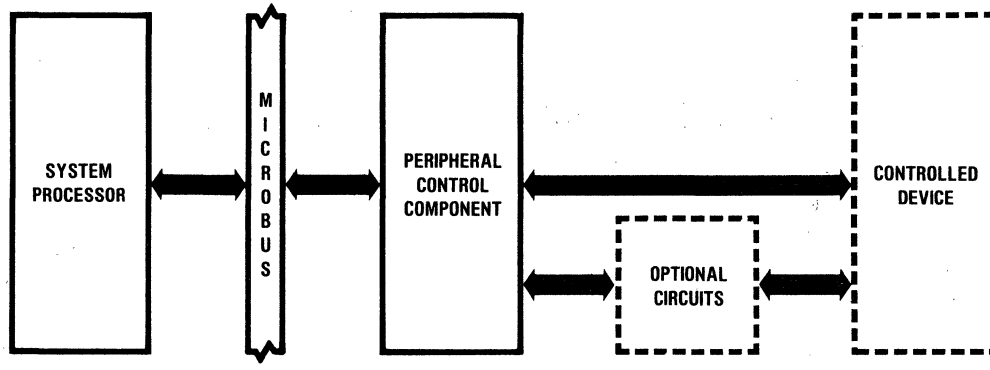


Figure 8-1. Interfacing the Peripheral Control Components

*Trademark, National Semiconductor Corporation

8.3.1 INS8244 90-Key Keyboard Encoder

The INS8244 is an MOS/LSI keyboard encoder capable of encoding 90 individual single-pole, single-throw switch closures into a usable 9-bit code.

Features

- TRI-STATE Data Outputs
- Function Inputs TTL Compatible
- Single TTL Clock
- N key/Two Key Rollover
- Key Bounce Masking

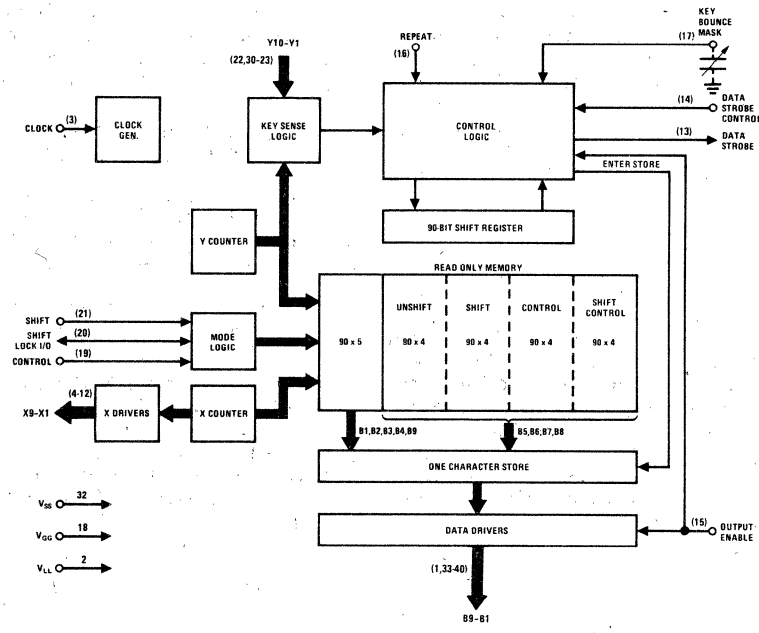


Figure 8-2. INS8244 Internal Block Diagram

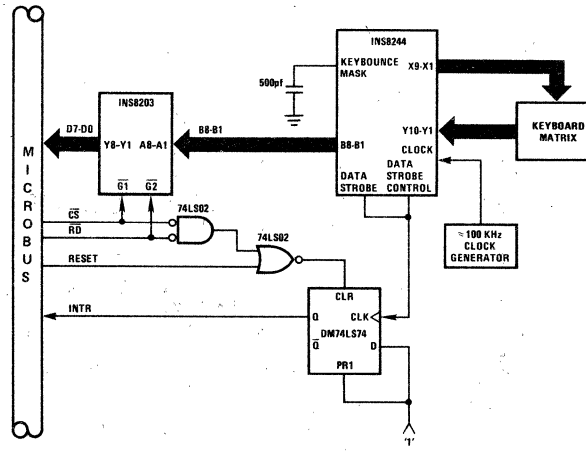


Figure 8-3. Typical Interrupt Driven Keyboard Interface

8.3.2 INS8245/8246 Keyboard Encoders

The INS8245/8246 are 16-key and 20-key encoders, respectively.These CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The encoders contain an on-chip debounce circuit and a data strobe output to ensure correct key entry. Two-key roll-over is also provided.

Features

- Accepts Up to 50KΩ Switch Resistance
- On or Off Chip Clock
- 2 Key Rollover
- TRI-STATE Outputs

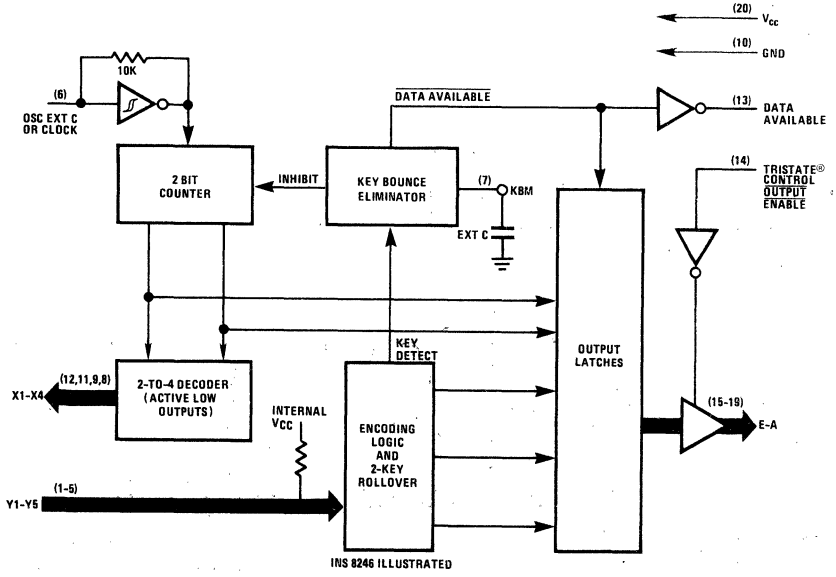


Figure 8-4. INS8246 Block Diagram

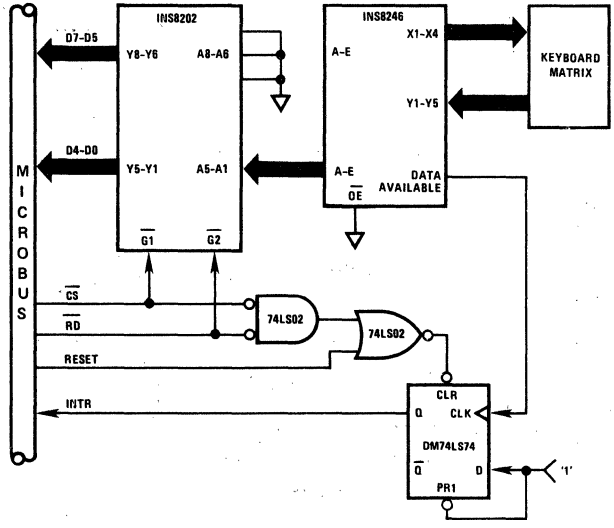


Figure 8-5. Typical MICROBUS Connection

8.3.3 INS8247/8248 Display Controller

The INS8247/8248 are display controllers that interface to a seven-segment display. The devices receive a digit address and the corresponding binary input data, convert the data and then output the corresponding seven-segment information to a display. Direct access to the internal registers is available via the digit lines through the use of the Digit I/O control signal. The INS8248 (not illustrated) contains internal BCD decoding and has a 6-digit output.

Features

- INS8248 - 6 Digits with 7 x 16 ROM Controlled by 4 Data Bits
- INS8247 - 4 Digits Controlled by 8 Data Bits
- Direct Segment Drive
- Random Access to Internal Registers

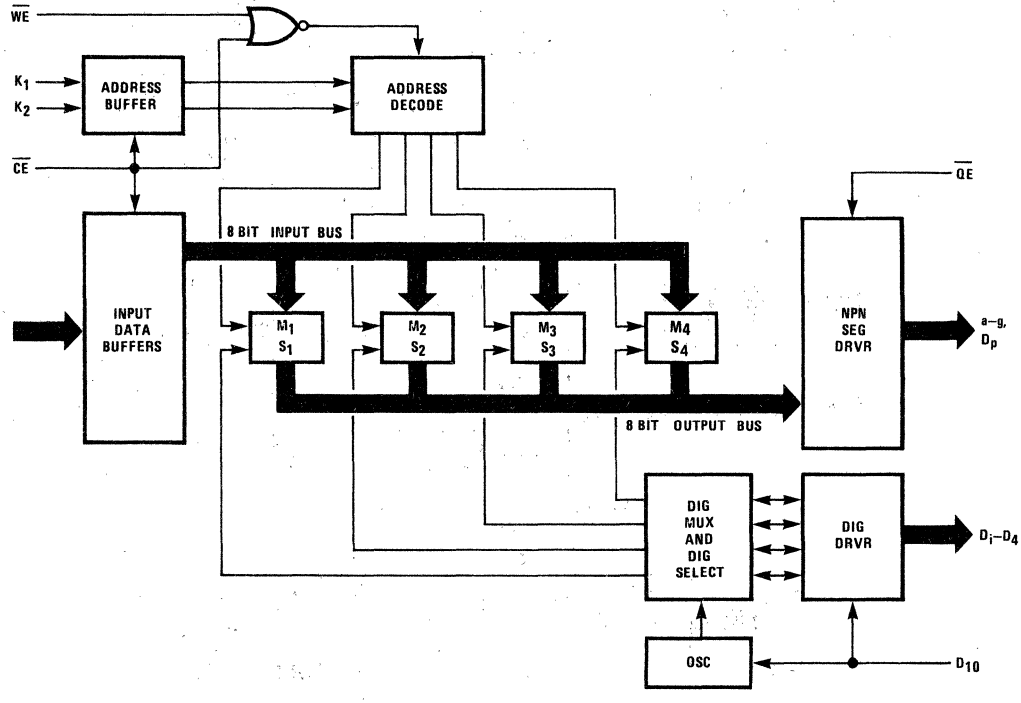


Figure 8-6. INS8247 Internal Block Diagram

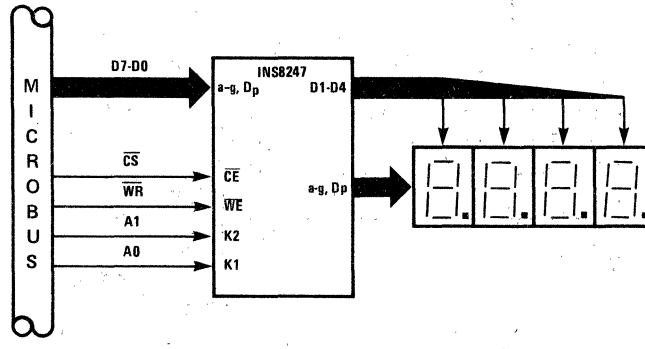


Figure 8-7. INS8247 MICROBUS Interface

8.4 INS8253 PROGRAMMABLE INTERVAL TIMER

The INS8253 is a software-controlled programmable counter/timer. The device can be set up by software to count or time-out three individual operations thereby allowing the CPU time to perform other functions until interrupted by a time-out or count from the INS8253.

Features

- Three Independent 16-Bit Counters
- Programmable Counter Modes
- Binary or BCD Count

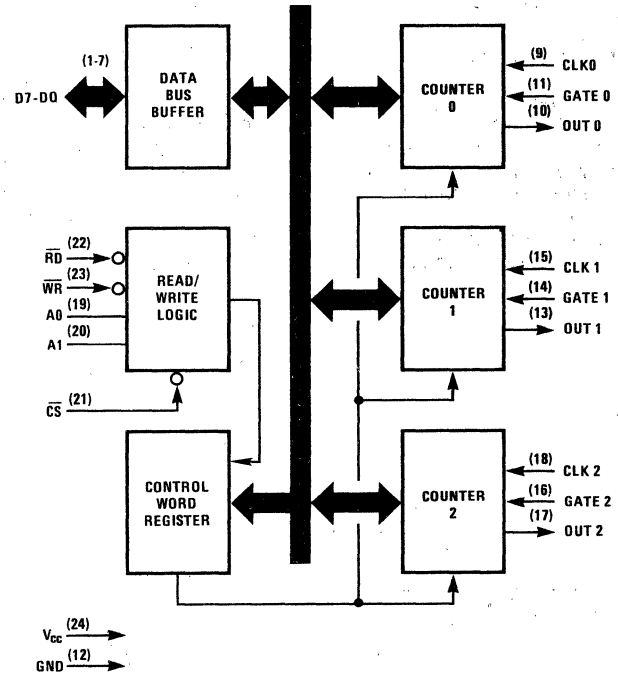


Figure 8-8. INS8253 Internal Block Diagram

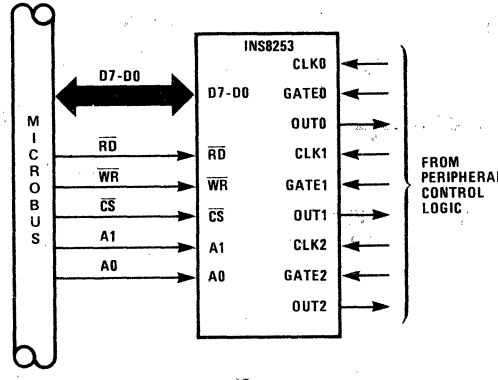


Figure 8-9. INS8253 MICROBUS Connection

8.5 INS1771-1 FLOPPY DISK FORMATTER/CONTROLLER

The INS1771-1 Floppy Disk Formatter/Controller will function with either the standard size floppy or the smaller mini-floppy.

Figure 8-10 shows an example of a diskette layout. Notice that the Index access hole is near the center of the diskette. This is a physical hole in the recording media sensed by a photocell to give a physical reference for determining the actual start of all recording tracks, which are concentric rings.

Track 00 is located near the outer edge of the recording surface while the highest numbered track is near the center (Track 76). When the diskette is initialized, track addresses are written for each track along with test data and after testing programs are run successfully, the diskette is ready for use. Clocking pulses and data are interleaved in the same track. See figure 8-11 which shows the read timing. Data must occur within the shaded portion of the timing diagram in order to be valid. The track format is shown in figure 8-12. After the physical sensing of the Index and a nominal delay, the Index Address Mark is written. This gives us the electronic start of that particular track. The ID record contains the sector adress and also the CRC (Cyclic Redundancy Check). This will be used by the error checking circuits to confirm valid data for ID record. This ID record is shown expanded in the left center of figure 8-12. A data field record is shown to the right. Byte one of the data field record is called the Data or Deleted Data Address Mark. This byte will allow recovery of deleted data prior to packing of the diskette, because the data is still there, although byte one is changed to indicate deleted data. The 128 bytes of user data is followed by CRC Bytes for error checking.

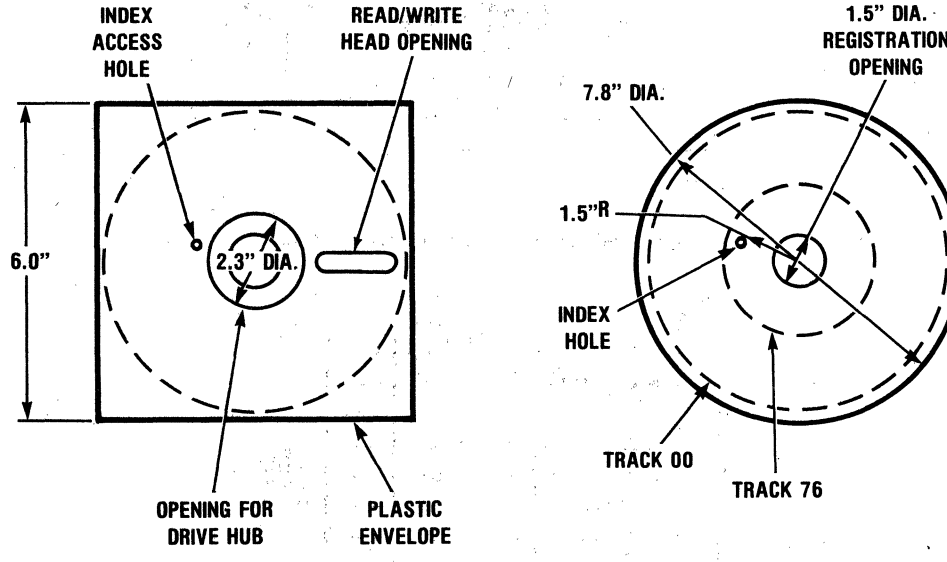
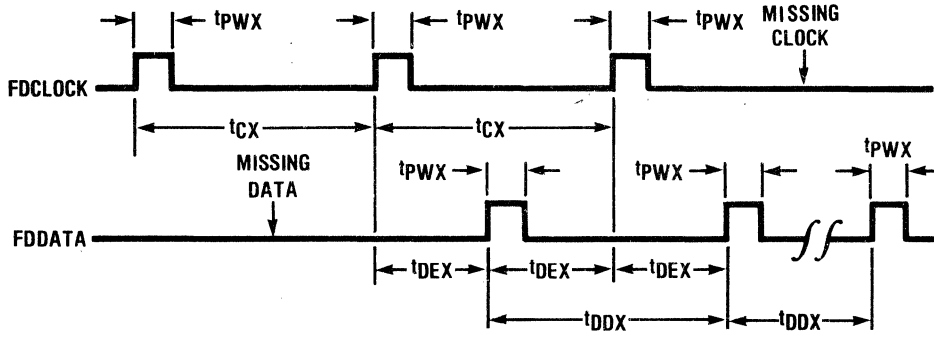
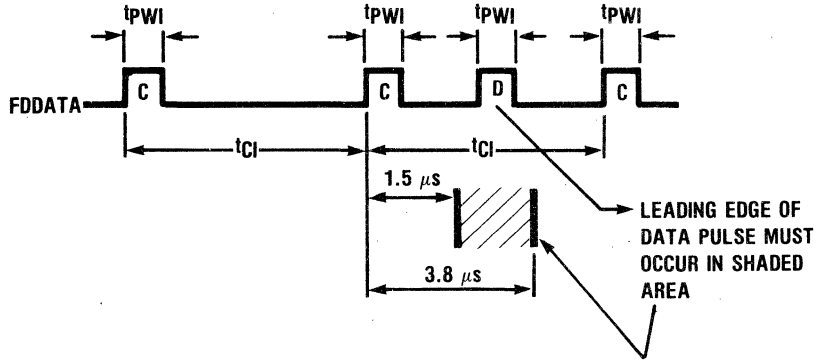


Figure 8-10. Diskette Layout (Example)



NOTES:
1. ABOVE TIMES ARE DOUBLED WHEN CLK = 1 MHz.
2. CONTACT NSC FOR EXTERNAL CLOCK/DATA SEPARATOR CIRCUITS.

Read Timing ($\overline{XTDS}$ = 0)



NOTES:
1. INTERNAL DATA SEPARATION MAY WORK FOR SOME APPLICATIONS. HOWEVER FOR APPLICATIONS REQUIRING HIGH DATA RECOVERY RELIABILITY, NSC RECOMMENDS THAT EXTERNAL DATA SEPARATION BE USED.
2. FDCLOCK MUST BE TIED HIGH.

Read Timing ($\overline{XTDS}$ = 1)

Figure 8-11. Read Timing

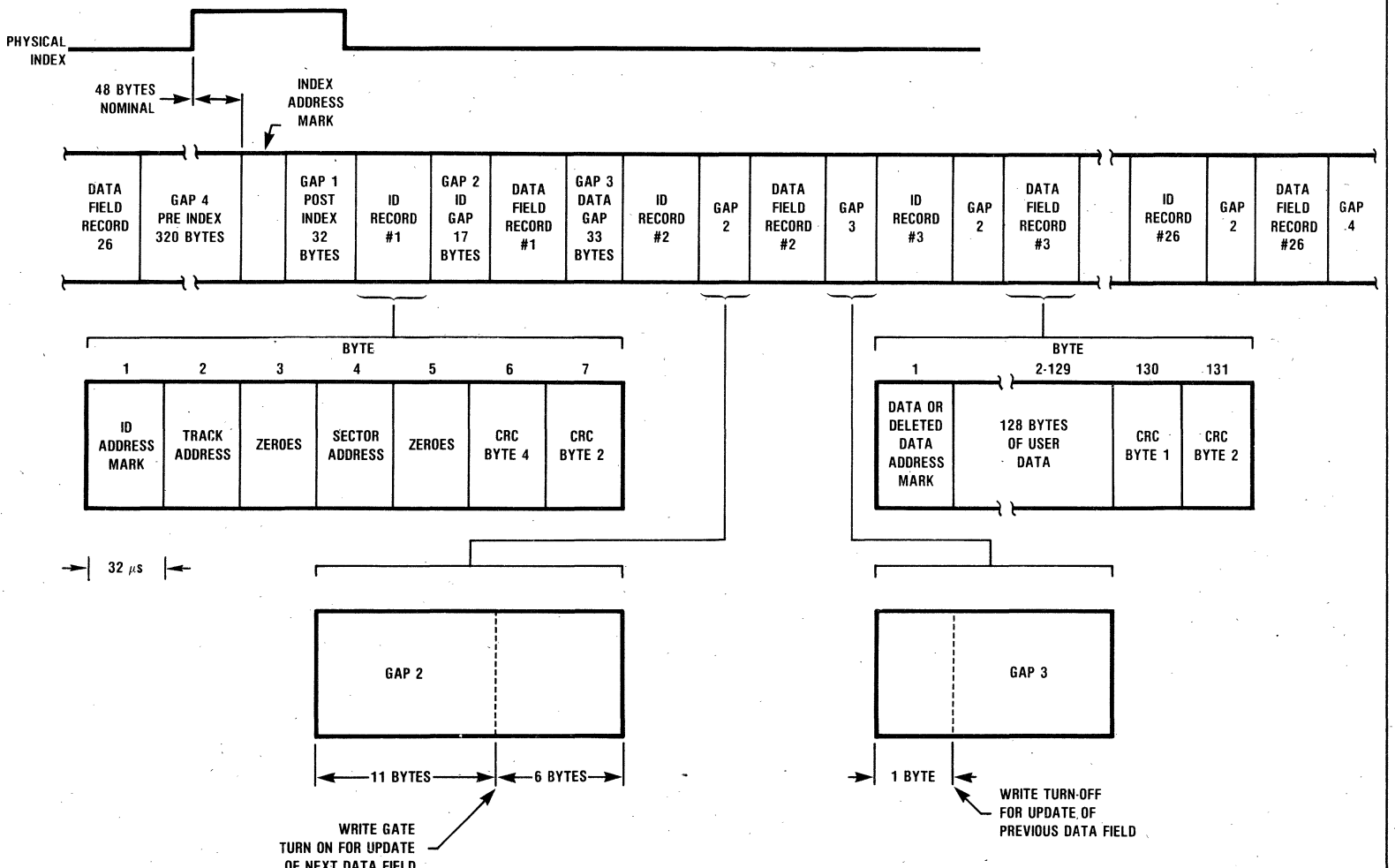


Figure 8-12. Track Format (Diskette)

The INS1771-1 provides for control of floppy disk drives including writing of the disk format by program control. This soft sector formatting may be either IBM3740 compatible or a user-selected, sector format. The INS1771-1 is programmed to carry out operations without continual control by the CPU, therefore freeing the CPU for other Operations. See figure 8-13 Interface to System Bus. The interleaved clock and data pulses are sent to a Data Separator, then the individual pulse streams are sent to the INS1771-1.

Figure 8-14 is a functional block diagram of the INS1771-1 device. The INS1771-1 includes error checking circuits and storage of status information such as sector and track location.

The chip is programmed by the system software, and program control information is transferred to the INS1771-1 over the system bus lines. This includes control words, status information, and all data transfers. These transfers for the INS1771-1 Floppy Disk Formatter/Controller are multiplexed on the system bus along with data for other bus-oriented devices. Interface to the system bus is shown in figure 8-13.

Selection of registers within the INS1771-1 is shown in table 8-10 Register select lines (A0, A1) are used in conjunction with either an active (low) $\overline{RE}$ or $\overline{WE}$ input to select an INS1771-1 register to read from or write into, as indicated in the table.

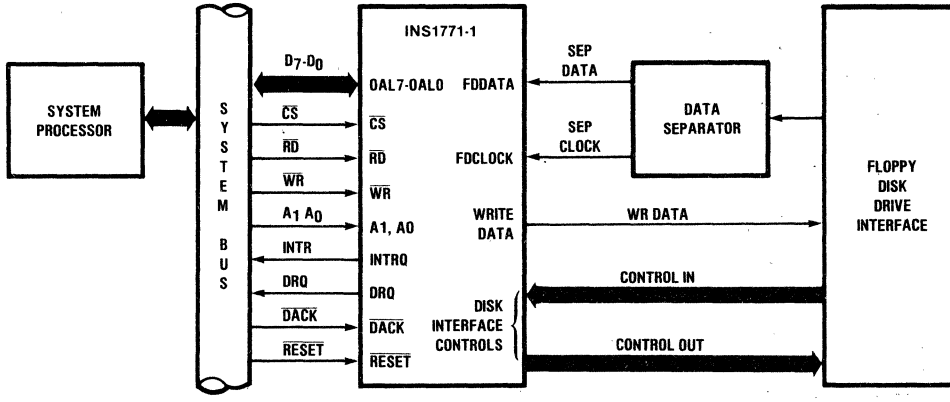


Figure 8-13. Interface to System Bus

Table 8-1. INS1771-1 Register Selection

A_1	A_0	$\overline{RE}$	$\overline{WE}$	Selected Register
0	0	0	1	Status Register
0	0	1	0	Command Register
0	1	0	1	Track Register
0	1	1	0	
1	0	0	1	Sector Register
1	0	1	0	
1	1	0	1	Data Register
1	1	1	0	

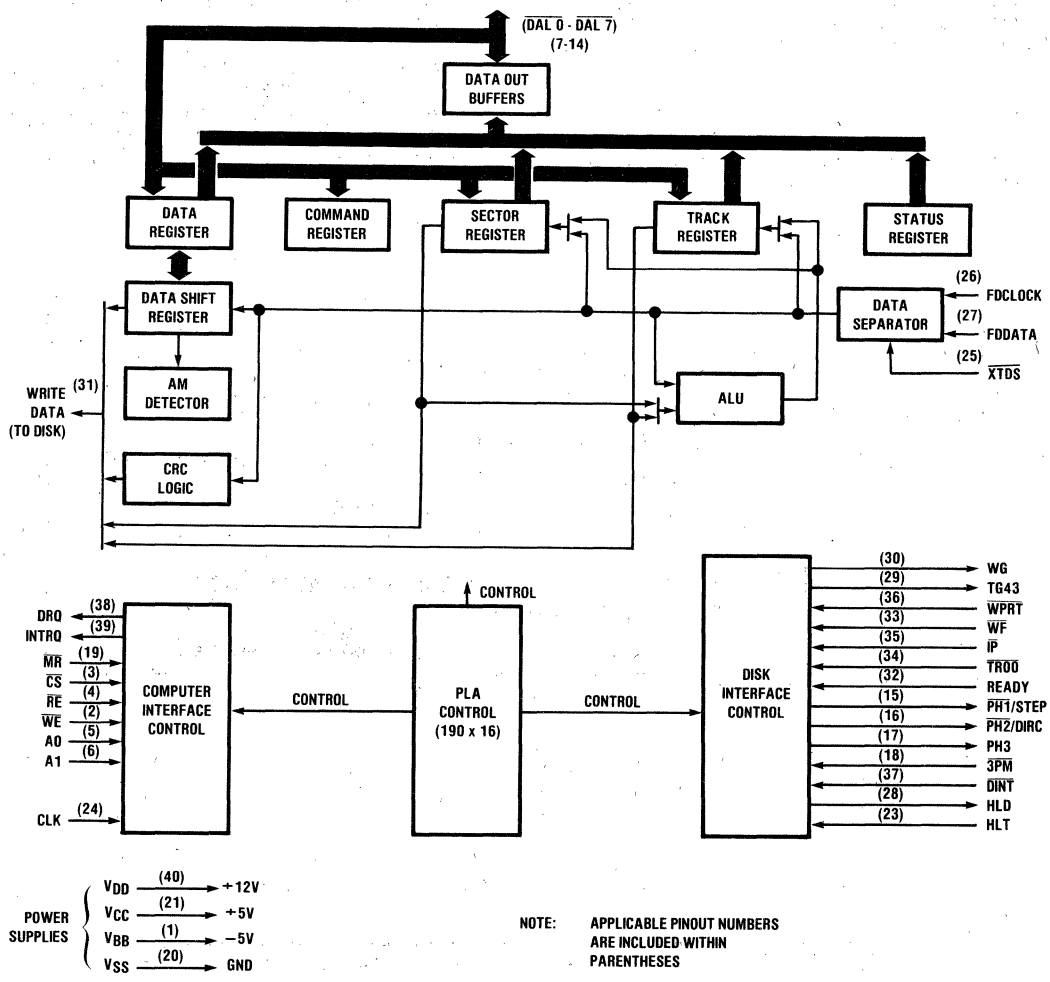


Figure 8-14. INS1771-1 Block Diagram

There are eleven commands grouped into four types are summarized in table 8-11. These command types are:

TYPE	GROUP
I	Head Positioning
II	Data Write/Read Commands
III	Track Commands (Format Disk)
IV	Force Interrupt

Table 8-2. Commands Summary

Type	Command	Bits							
		7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h		r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	$\bar{s}$
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

Type I commands are basically head positioning commands. Included are Restore, Seek, Step, Step In, and Step Out. Restore will cause positioning to track 00. Seek will position the head to a particular addressed track. Step, Step In, and Step Out are incremental step commands. Step In or Step Out cause movement to the adjoining track in the direction specified. Step will cause movement in the current direction to the next track.

Refer to figure 8-15 Seek Command, and also the Block Diagram in figure 8-14 for the following discussion. Recall that the data lines will transfer data, address and control information. During the Seek operation the track number which we desire is loaded into the Data Register. The current track is stored in the Track Register. When they are not equal, step commands will be issued. When they compare the Read/Write head has reached the desired position, and an interrupt will then be sent to the CPU via the system bus.

Type II Commands cause writing or Reading of data in one or more sectors. Error checking is performed and the command is terminated with an interrupt if a valid ID field is not found within two revolutions of the disk. The ID field must have a valid track number, sector number and CRC for proper operation, otherwise the Record Not Found status bit (bit 4) is set.

Type III commands are used to format the diskette. They are Read Address, Read Track, and Write Track. The Read Address command causes a read of the next ID field and transfers the data to the CPU.

Type IV Commands may be loaded into the command register at any time and will cause termination of any command under execution and an interrupt to be generated.

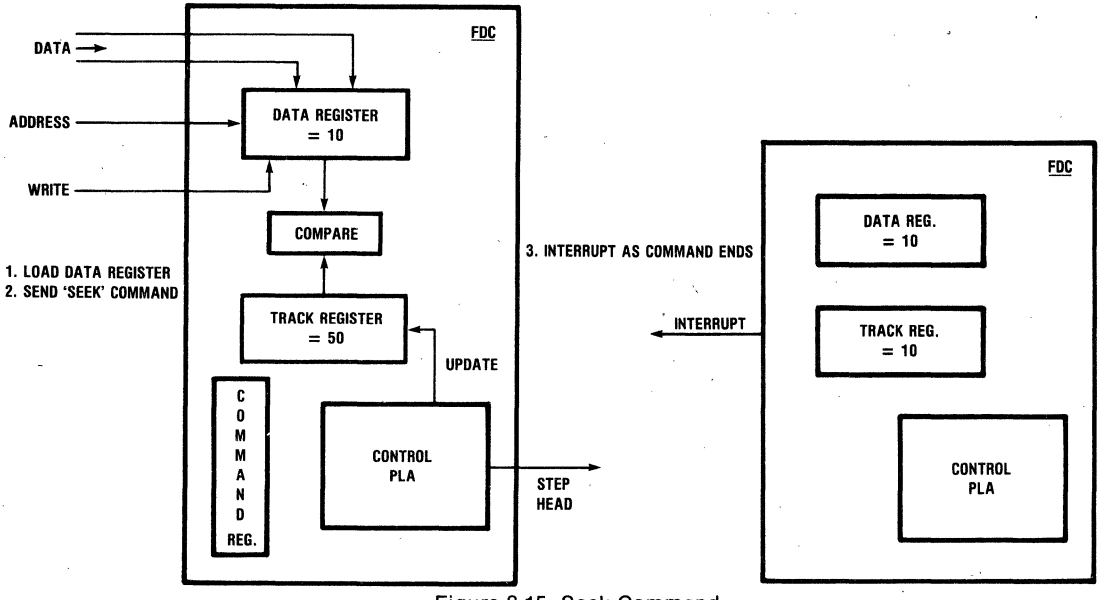


Figure 8-15. Seek Command

8.6 DP8350 PROGRAMMABLE CRT CONTROLLER

The DP8350 is a mask-programmable dedicated CRT display refresh controller. It is a single chip bipolar (I^2L technology) circuit in a 40 pin package. The DP8350 contains a crystal controlled dot rate clock, to ease system synchronization and a complete set of video synchronization output signals. Internal mask-programmable ROMs are used to provide a wide range of program control.

For systems where a dot rate clock is already provided, an external clock input may be used by the CRT controller. In either case, system synchronization is made possible with the use of the buffered Dot Rate Clock Output.

There are eleven character generation related outputs for use with system character ROMs and three on-chip registers that provide for external loading of the new row starting address, cursor address, and top-of-page address. The DP8350 can directly interface with up to 4K of memory via the three on-chip registers provided for external loading of the new row starting address, cursor address, and top of page address.

A complete set of video sync outputs is available including cursor enable, programmable vertical blanking, programmable horizontal blanking, programmable horizontal sync, and programmable vertical sync.

The DP8350 Programmable CRT Controller allows a wide range of program control:

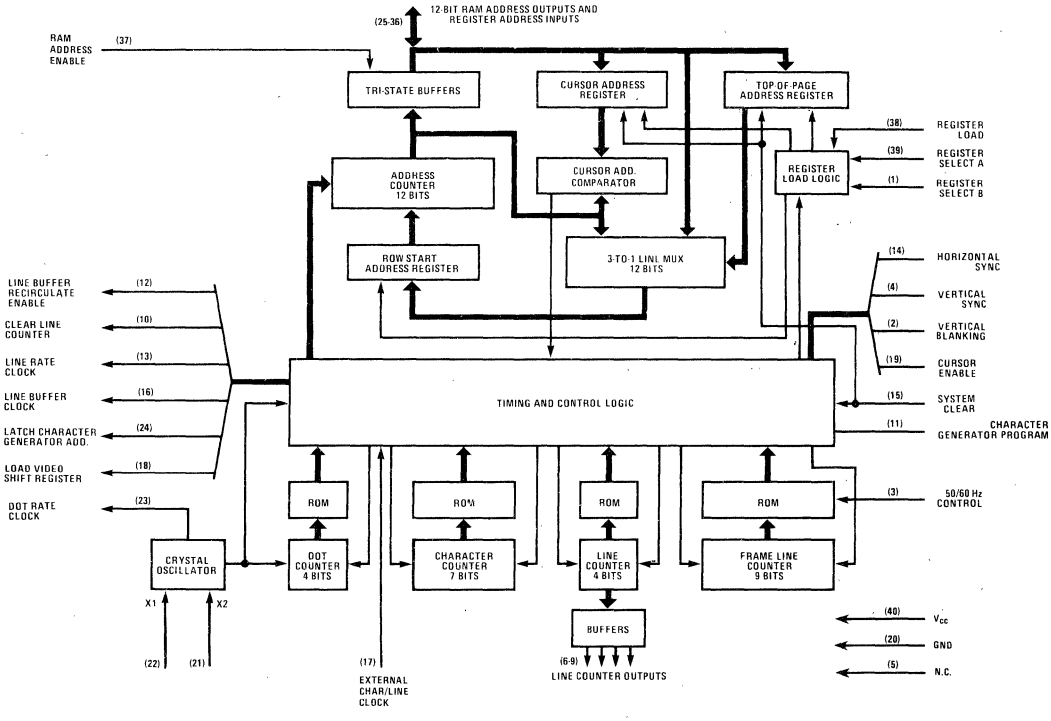
- Character Field (both number of dots/character and number of scan lines/character)
- Characters per Row
- Character Rows per Video Frame

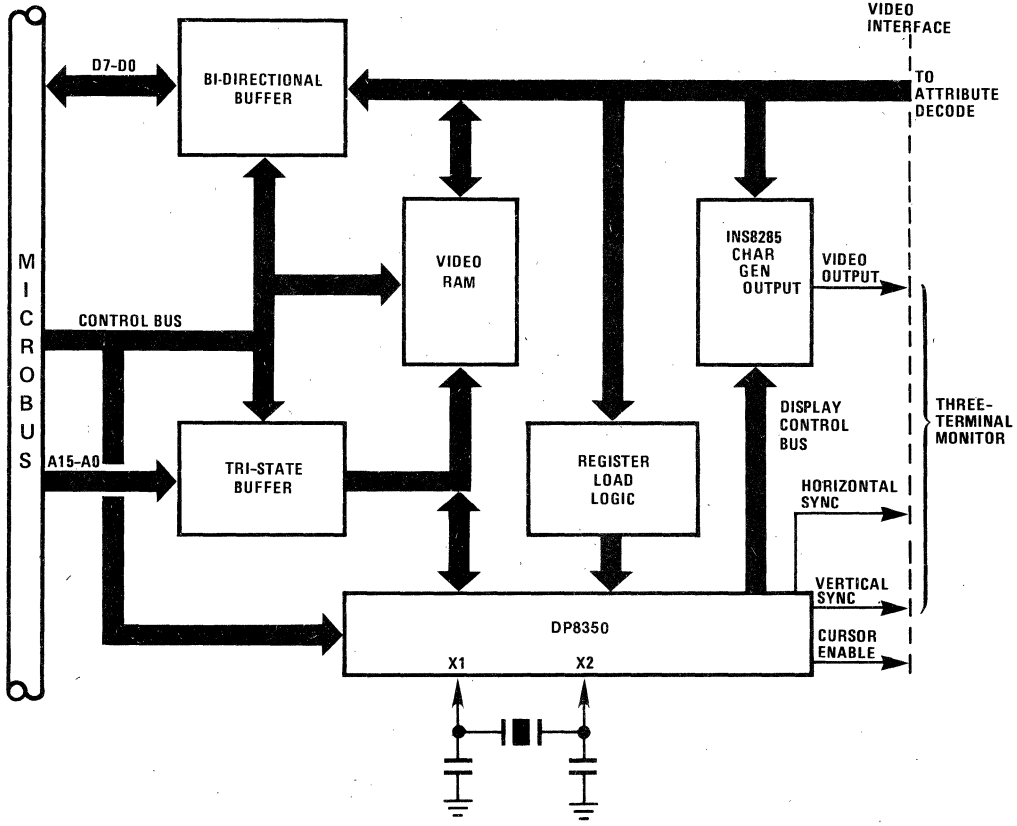
The CRT controller (CRTC) also provides program inputs, (including 50/60 Hz control), system clear, and characters/line rate clock.

The DP8350 operates on a single +5V power supply. Outputs and inputs are TTL compatible.

Features

- Internal Crystal Controlled Dot Rate Oscillator
- External Dot Rate Clock Input
- Buffered Dot Rate Clock Output
- Timing Pulses for Character Generation
- Character Memory Addressing
- Scrolling Capability
- Internal Cursor Address Register
- Internal Row Starting Address Register
- Programmable Character Field Size (up to16 x 16)
- Programmable Character/Row (5 to 110)
- Programmable Character Rows/Frame (1 to 64)
- Programmable Horizontal and Vertical Sync. Outputs
- Programmable Cursor Enable Output
- Programmable Vertical Blanking Output
- 50/60 Hz Refresh Rate
- Inputs and Outputs TTL Compatible
- Single +5V Power Supply


12-BIT RAM ADDRESS OUTPUTS AND REGISTER ADDRESS INPUTS
(25-36)
RAM ADDRESS ENABLE
(37)
TRI-STATE BUFFERS
CURSOR ADDRESS REGISTER
TOP OF PAGE ADDRESS REGISTER
ADDRESS COUNTER 12 BITS
CURSOR ADD. COMPARATOR
REGISTER LOAD LOGIC
(38) REGISTER LOAD
(39) REGISTER SELECT A
(1) REGISTER SELECT B
ROW START ADDRESS REGISTER
3-TO-1 LINE MUX 12 BITS
(14) HORIZONTAL SYNC
(4) VERTICAL SYNC
(2) VERTICAL BLANKING
(19) CURSOR ENABLE
(15) SYSTEM CLEAR
(11) CHARACTER GENERATOR PROGRAM
LINE BUFFER RECIRCULATE ENABLE
(12)
CLEAR LINE COUNTER
(10)
LINE RATE CLOCK
(13)
LINE BUFFER CLOCK
(16)
LATCH CHARACTER GENERATOR ADD.
(24)
LOAD VIDEO SHIFT REGISTER
(18)
DOT RATE CLOCK
(23)
TIMING AND CONTROL LOGIC
ROM
ROM
ROM
ROM
(3) 50/60 Hz CONTROL
CRYSTAL OSCILLATOR
DOT COUNTER 4 BITS
CHARACTER COUNTER 7 BITS
LINE COUNTER 4 BITS
FRAME LINE COUNTER 9 BITS
X1
X2
(22)
(21)
BUFFERS
(6-9) LINE COUNTER OUTPUTS
(17) EXTERNAL CHAR/LINE CLOCK
(40) Vcc
(20) GND
(5) N.C.


VIDEO INTERFACE
D7-D0
BI-DIRECTIONAL BUFFER
TO ATTRIBUTE DECODE
MICROBUS
VIDEO RAM
INS8285 CHAR GEN OUTPUT
VIDEO OUTPUT
CONTROL BUS
A15-A0
TRI-STATE BUFFER
REGISTER LOAD LOGIC
DISPLAY CONTROL BUS
THREE-TERMINAL MONITOR
HORIZONTAL SYNC
VERTICAL SYNC
CURSOR ENABLE
DP8350
X1
X2

8

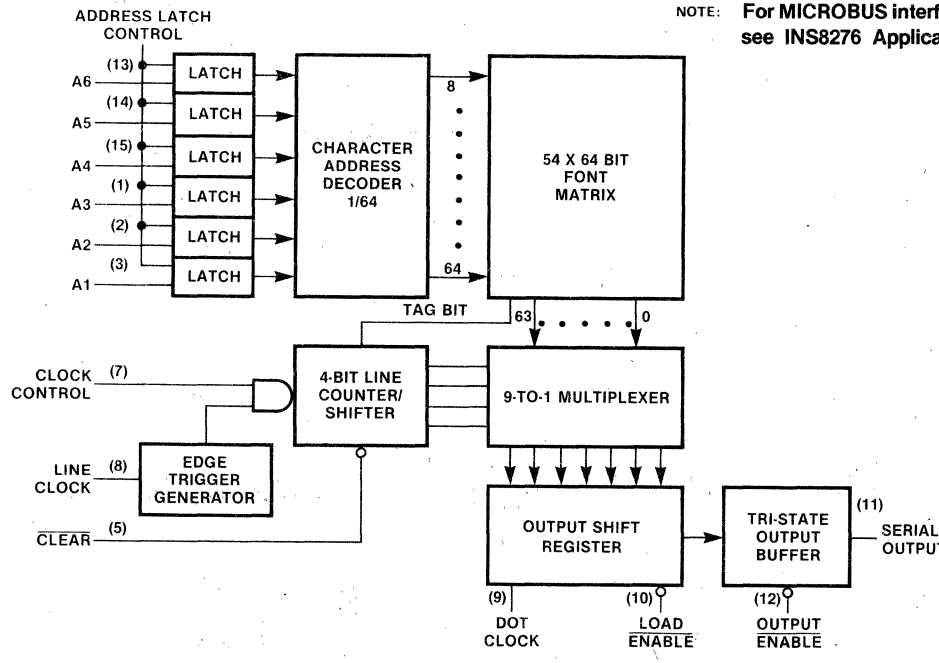
8.7 INS8285 CHARACTER GENERATOR

The INS8285 is a 64-character bipolar character generator with a serial output. The INS8285 performs the system functions of parallel-to-serial shifting, character address latching, character spacing, and character line spacing. The row scan character font is available in either 5 x 7 or 7 x 9 format with either shifted or unshifted character output available.

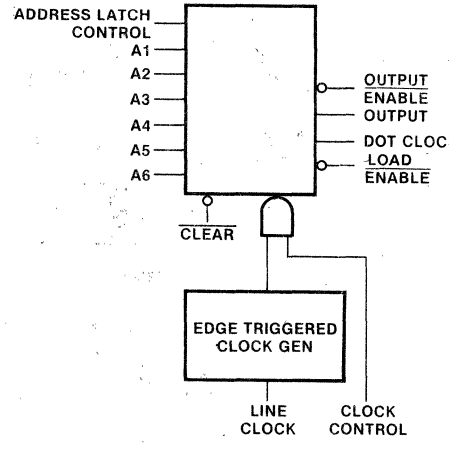
Features

- 64 Characters Per Row
- 5 x 7 or 7 x 9 Font
- Shifted Lower Case Characters
- Serial Output

NOTE: **For MICROBUS interface, see INS8276 Application**



LOGIC SYMBOL

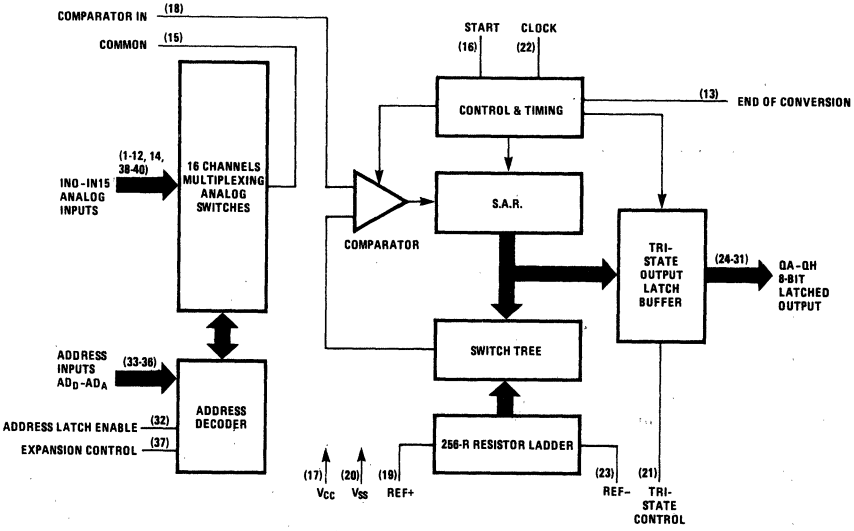


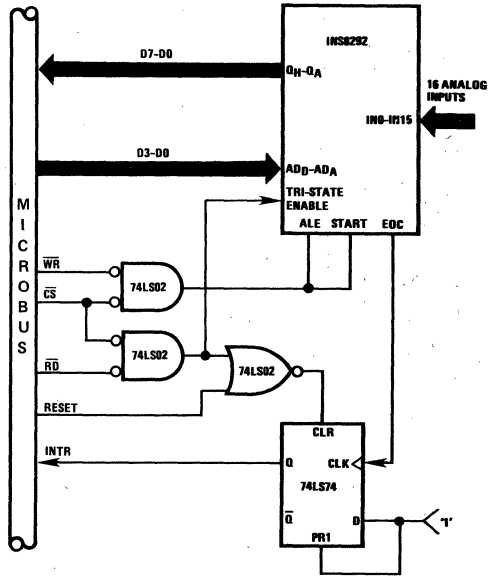
8.8 INS8292 CMOS 8-BIT A/D CONVERTER

The INS8292 is a monolithic A/D converter containing a 16-channel analog input multiplexer with an 8-bit latched TRI-STATE output. A reference voltage applied to the INS8292 provides a set voltage range within which the device will operate. Conversion is performed using a successive approximation technique. At the end of a conversion operation, the 8-bit binary equivalent to the unknown voltage is latched into the 8-bit latch.

Features

- Reference Voltage Ref $+V_{CC}$
- Reference Voltage Ref $-V_{SS}$
- TRI-STATE Output, TTL Compatible
- Monotonicity





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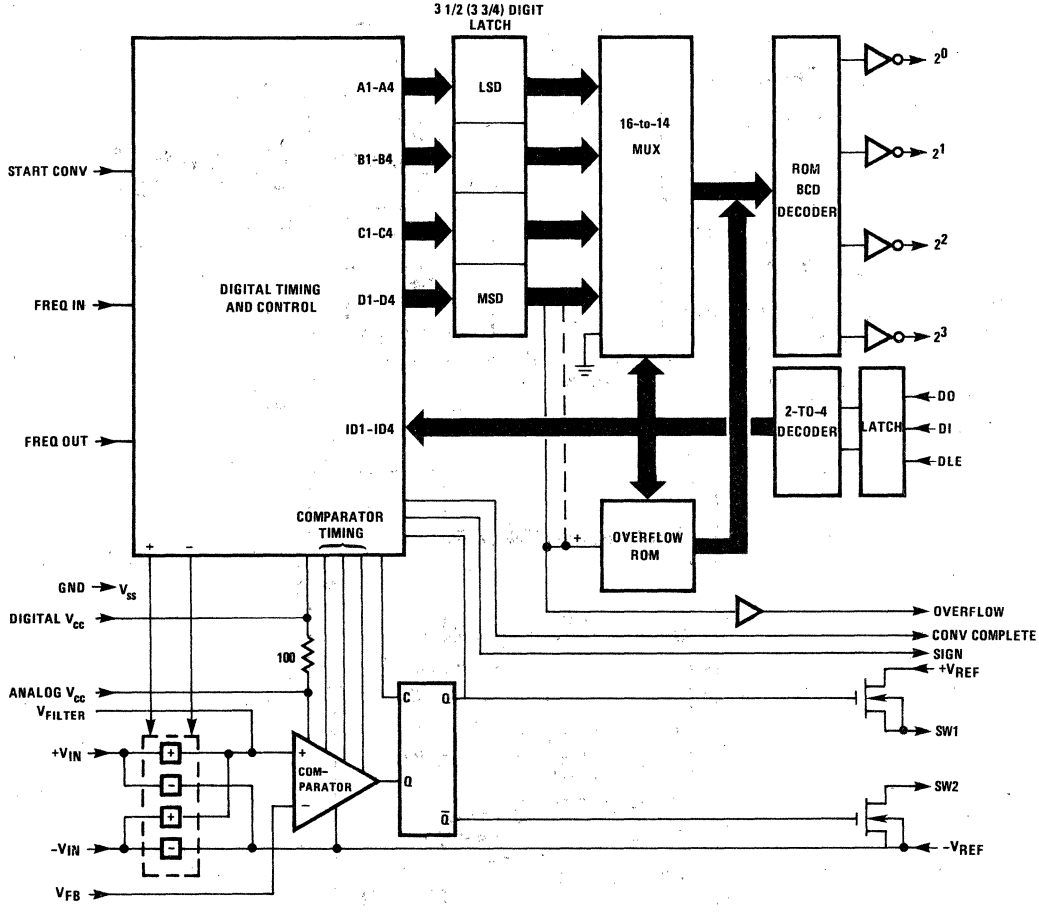
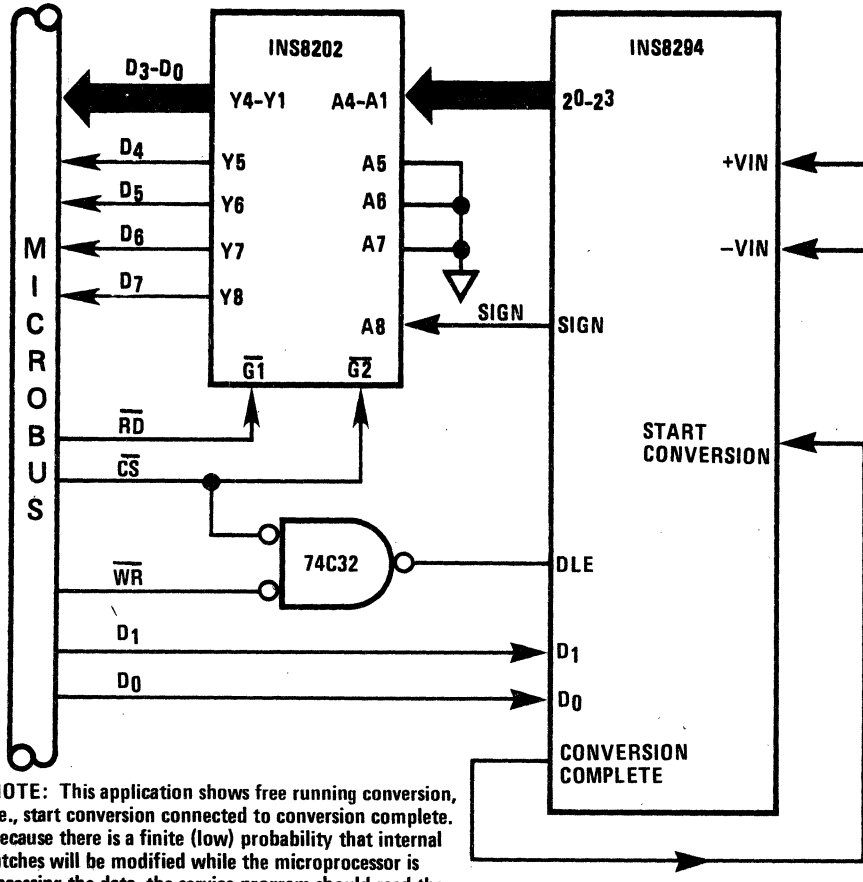
8.9 INS8294 3-¾ DIGIT DIGITAL VOLTMETER

The INS8294 is a CMOS Digital Voltmeter that uses a pulse-modulation A/D conversion technique and requires no external precision components for operation. The pulse-modulation technique allows the use of a reference voltage that is the same polarity as the input voltage. When operating with an isolated supply, both positive and negative voltages may be converted. The INS8294 has been designed to provide addressed BCD data which are selected on demand via digit select inputs. Start Conversion and Conversion Complete signals are also provided to ease microprocessor interfacing.

Features

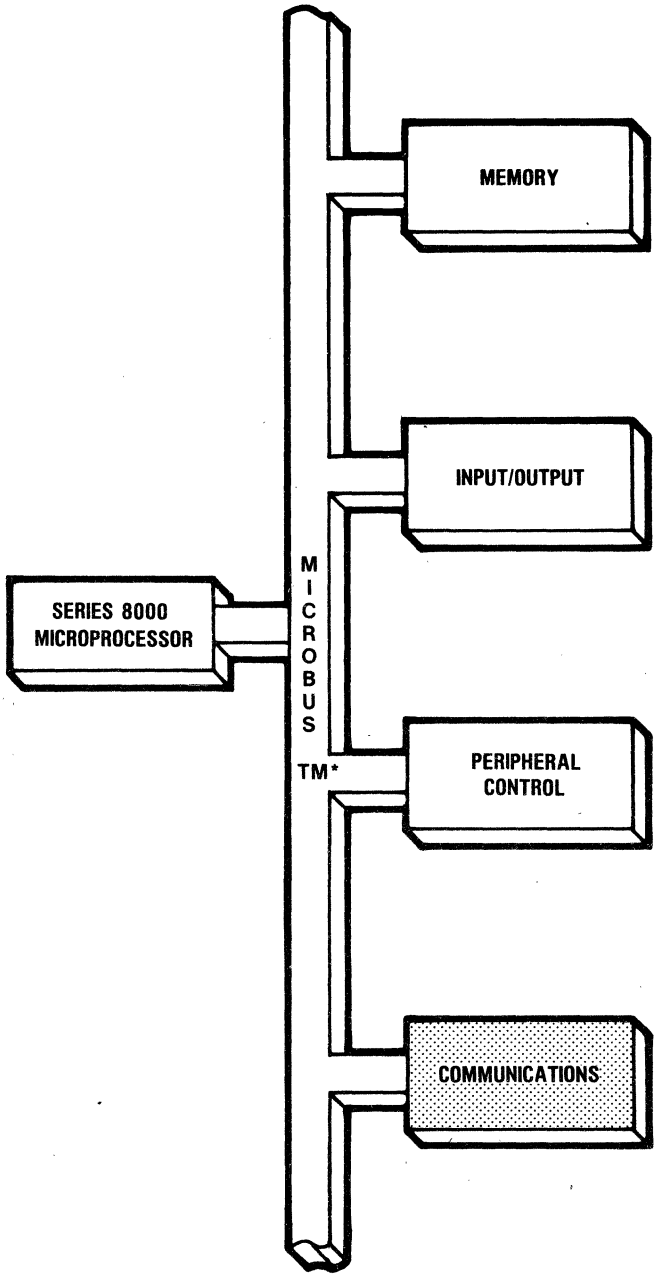
- Operates from Single 5V Supply
- Converts 0 to ±3999 Counts
- Addressable BCD Outputs
- No External Precison Components Necessary
- Easy Interface to Microprocessors





NOTE: This application shows free running conversion, i.e., start conversion connected to conversion complete. Because there is a finite (low) probability that internal latches will be modified while the microprocessor is accessing the data, the service program should read the data twice and compare the two samples to insure its validity.

8

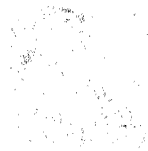


Chapter 9
Communications Components

Part Number/Description

INS8250
Asynchronous Communications Element (ACE)
INS8251
Programmable Communications Interface
INS1671
ASTRO Communications Interface

* Trademark, National Semiconductor Corporation



Communications Components

9.1 GENERAL DESCRIPTION

The Communications Components provide the serial link to either a data communications link or an RS-232 interface (or any other type interface) for a microcomputer. The programmable components in this chapter allow the user extreme flexibility when implementing serial data transfers.

The general operational concepts of the devices in this section are the same; parallel data transfers occur on the MICROBUS to/from the interface device and the interface device then converts and transmits the data to/from the peripheral device interface drivers over one or more serial I/O lines. In addition to performing the data transfer functions, the Communications Components also provide control signals to both the system and the peripheral interface to facilitate data transfers.

Detailed parametric information on each of the Communications Components is contained in appendix D, Device Data Sheets.

9.2 INTERFACING THE COMMUNICATIONS COMPONENTS

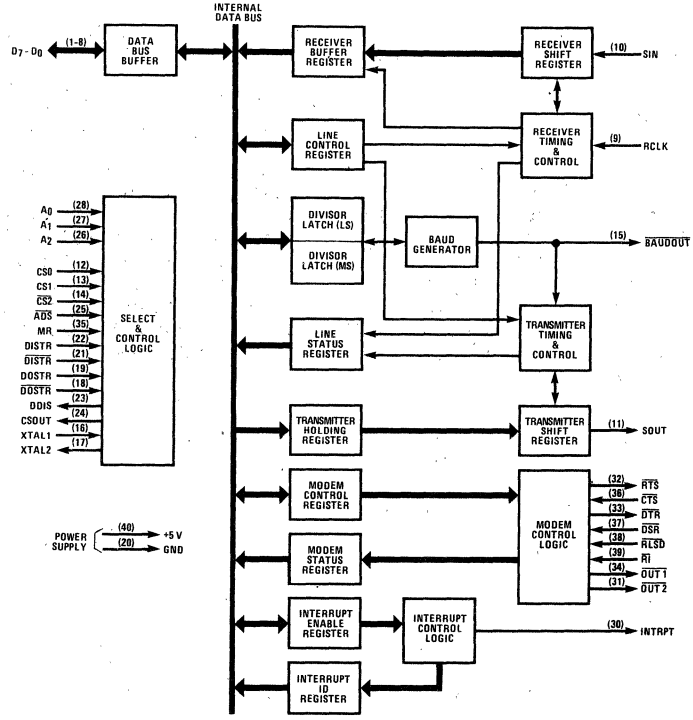
The communications components provide the serial interface to either a data communication link or an RS-232 interface. The devices contained in this section are all software-programmable which allow the user greater flexibility when implemeting serial data transfers. Due to the memory-mapped I/O capability of the INS8080A, these devices are compatible with the MICROBUS as far as data transfers are concerned. The remaining non-MICROBUS control signals on the communications components are for use with the peripheral devices.

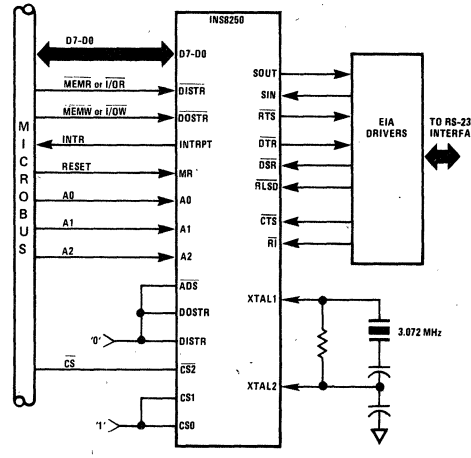
9.3 INS8250 ASYNCHRONOUS COMMUNICATIONS ELEMENT (ACE)

The INS8250 is a programmable Asynchronous Communications Element (ACE) that functions as a serial data input/output interface. The INS8250 performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. An important feature available with the INS8250 is the availability of the CPU to read the status of the INS8250 at any time.

Features

- Adds or Deletes Bits (Start, Stop, and Parity) to or from Serial Data Stream
- Full Double Buffering
- Independently Controlled Control Functions
- Programmable Baud-Rate Generator
- Complete Status Reporting Capabilities
- TRI-STATE Bus Drivers



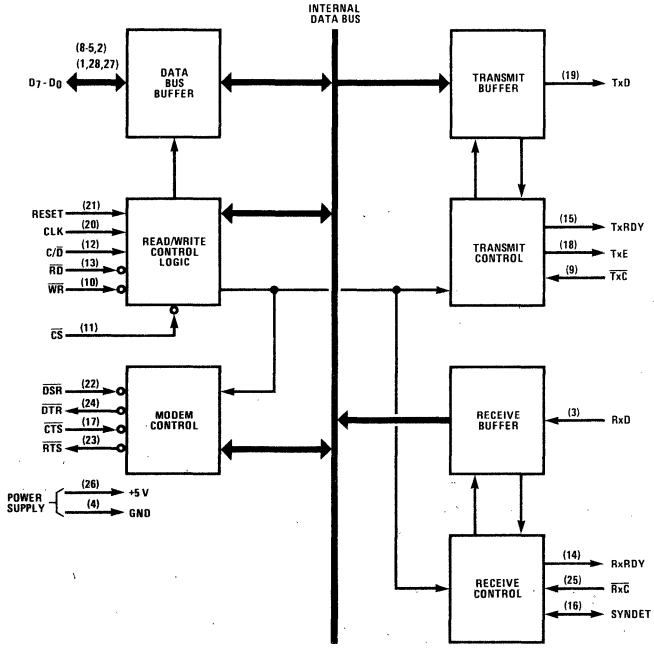


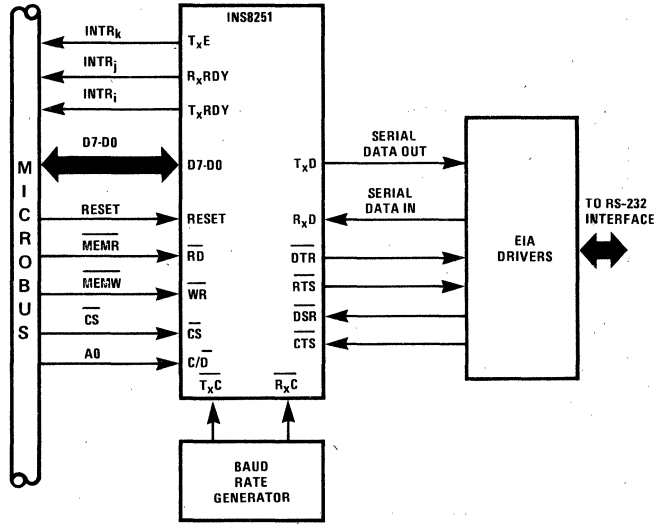
9.4 INS8251 PROGRAMMABLE COMMUNICATIONS INTERFACE

The INS8251 is a programmable Universal Synchronous/Asynchronous Receiver/Transmitter (USART) that provides a variety of synchronous and asynchronous serial data communication options. The INS8251 performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. This device is particularly suitable for implementing BISYNC protocol.

Features

- Synchronous and Asynchronous Full Duplex Operation
- Selectable Character Length
- Selectable Baud Rates
- Transmission Error Detection Capabilites
- Double Buffering of Data
- TTL Compatible





9.5 INS1671 ASYNCHRONOUS/SYNCHRONOUS TRANSMITTER/RECEIVER

General Description

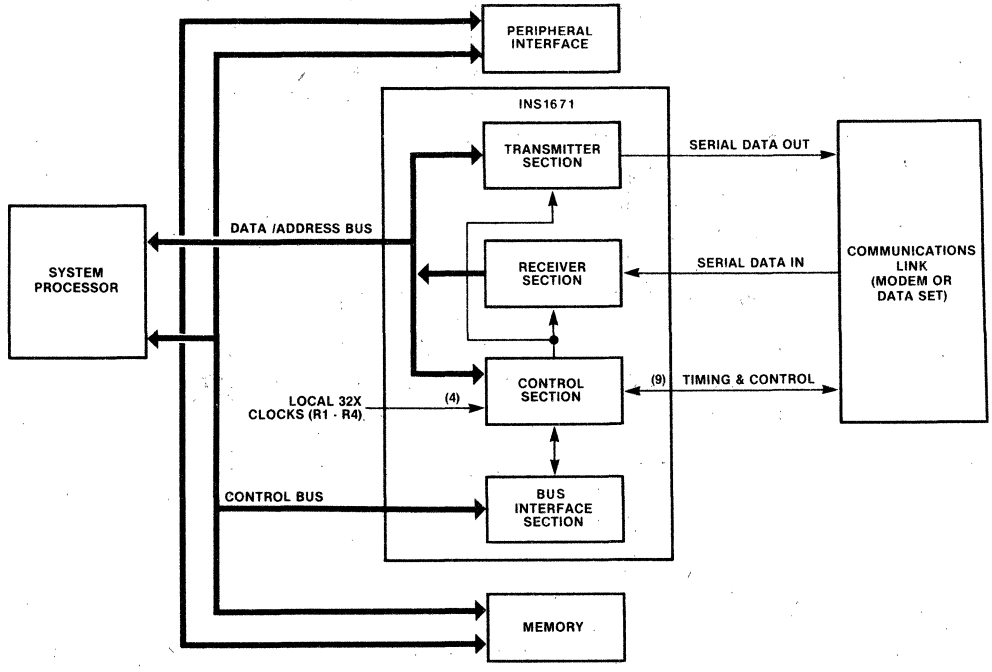
The INS1671 is a programmable Asynchronous/Synchronous Transmitter/Receiver (ASTRO) chip housed in a standard, 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate MOS technology, provides a serial data input/output interface in a bus-structured system. The chip is capable of full duplex operation with synchronous or asynchronous data communications systems.

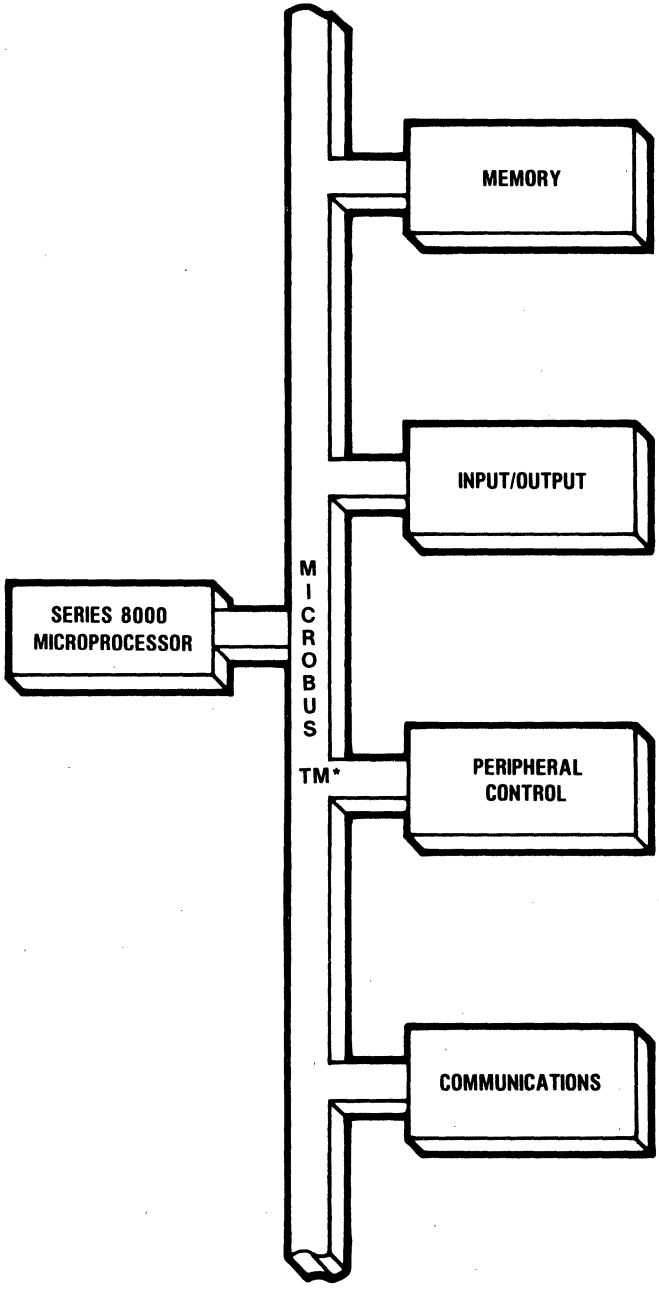
The INS1671 is designed to operate on a multiplexed, bidirectional bus with other bus-oriented devices. The functional configuration of the INS1671 is programmed by the system software via the bus and all parallel data transfers within the system are accomplished over the bus lines. In additon, the INS1671 contains a provision for hardwiring a unique 5-bit identification code to a chip, thereby allowing up to 32 INS1671 devices to be addressed via the multiplexed bus.

Features

- Synchronous and Asynchronous Full Duplex Operations
- Synchronous Mode Capabilities
  - Selectable 5-to-8-Bit Characters
  - Two Contiguous SYN Characters Provide Synchronization
  - Programmable SYN and DLE Characters Stripping
  - Programmable SYN and SYN-DLE Characters Insertion
- Asynchronous Mode Capabilities
  - Selectable 5-to-8-Bit Characters
  - Line Break Detection
  - 1-, 1½-, or 2-Stop Bit Detection
  - False Start Bit Detection
  - Automatic Serial Echo Mode
- DC to 1M Baud Rate
- 8 Selectable Clock Rates (4 Programmable)
- Transmission Error Detection Capabilities
  - Parity
  - Overrun
  - Framing
- Double Buffering of Data
- 8-Bit Bidirectional Bus for Data, Status, and Control Words
- All Inputs and Outputs TTL Compatible
- On-Line Diagnostic Mode
- Reduces System Component Count
- Direct Plug-In Replacement for Western Digital FD1671

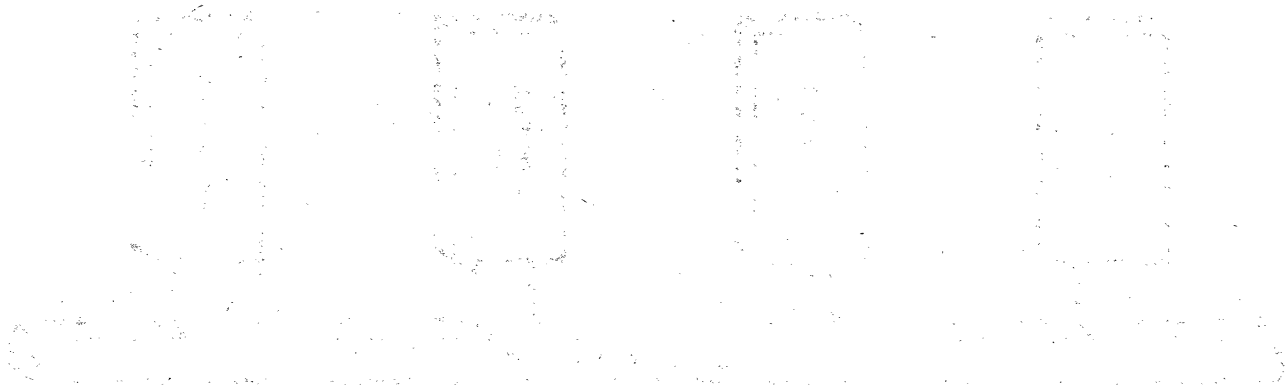
INS1671 General System Configuration





Chapter 10
Development Support

* Trademark, National Semiconductor Corporation



Development Support

10.1 GENERAL DESCRIPTION

National supports its microprocessor-based systems with a variety of software routines, hardware development systems, applications engineering services, and training services.

To ensure full support capability, all of the ancillary devices required are supplied by National and have been thoroughly tested in systems produced by National. The 8080A family is supported by industry-standard design kits, easy-to-use development systems, and a full complement of cross and resident assemblers. Various components and software also are available to support the 8080A family from experimentation to final production.

Design aids for the 8080A provide unique development and test capabilities, including comprehensive system control and debug, the examination/modification of all CPU registers and memory, and simulation of the user's PROM, RAM, or I/O. All of the capabilities and speed of execution of the 8080A microprocessor chip are available for the efficient implementation of the target system.

10.2 UNIVERSAL DEVELOPMENT SYSTEM (UDS1)

The Universal Development System (UDS1) is a disk-oriented operating system that can be used in the development of any NSC microprocessor-based system. UDS1 provieds all the capabilities of the Universal Development System, and further increases throughput and flexibility by providing the convenient mass storage capability of dual floppy disk drives. See figure 10-1, pictorial of UDS1 and figure 10-2, UDS1 block diagram.

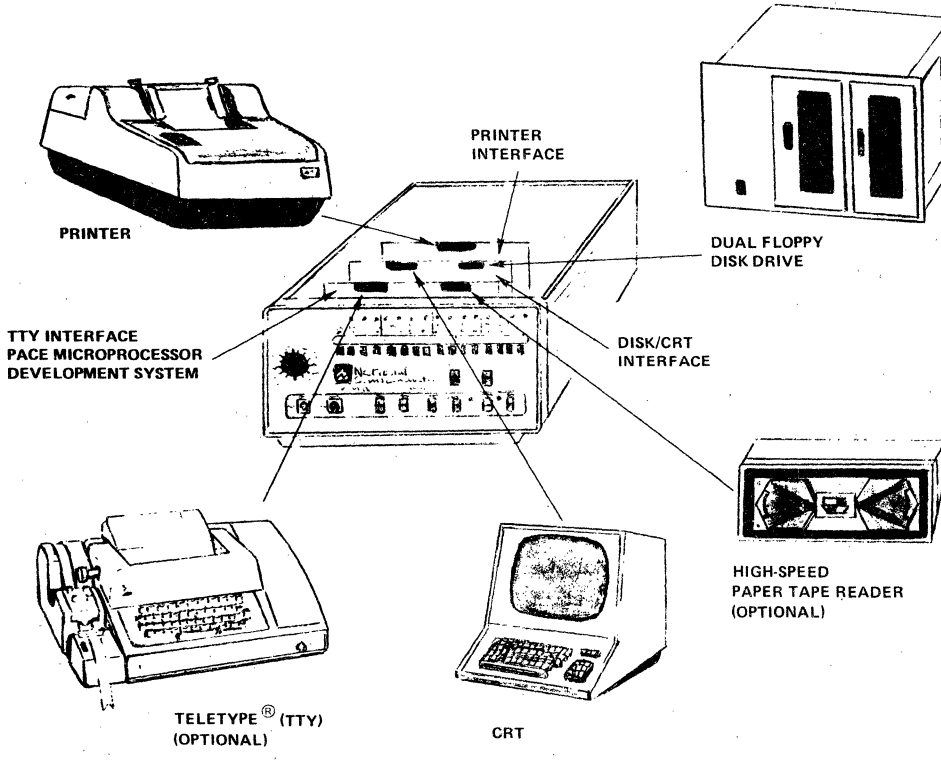


Figure 10-1. Universal Development System (UDS1)

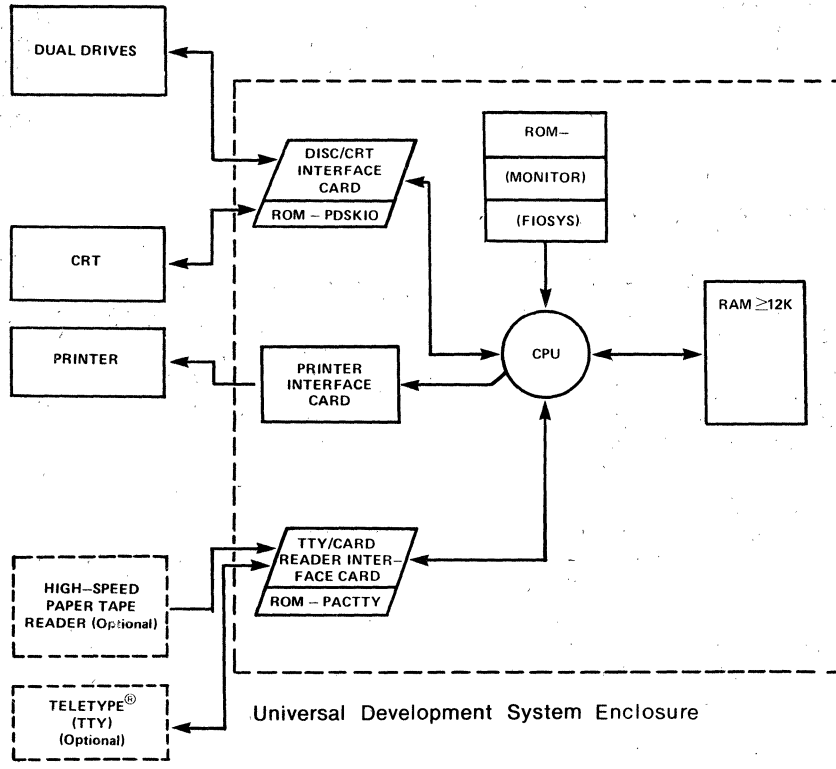


Figure 10-2. UDS1 Block Diagram

The Universal Development System and its associated peripherals provide a means whereby software for an application system can be readily developed, edited, and assembled. The inherent features of the Universal Development System make it a flexible tool suitable for use in developing a wide variety of microprocessor–oriented software applications. The combination of a CRT and the Universal Development System provides the minimum equipment necessary for immediate evaluation and development of software using UDS1.

The Programmers and Operators Controls facilitate software development/debugging and provide a convenient means of controlling UDS operation. Complete descriptions of the Programmers and Operators Controls are presented in the Universal Development System Users Manual.

The Universal Development System can be user-expanded to include the optional peripherals that are available to ease software development. In additon, to ease expansion, the basic Universal Development System is prewired to accept additonal memory and peripheral interface cards.

Getting Acquainted With UDS1

This paragraph summarizes the procedures required to "turn on" and initialize UDS1, to access and use the various system programs.

1. Turn on the power to the dual floppy disc drives, and insert the Master Diskette containing the system programs (refer to the UDS1 Users Manual).

2. Initialize UDS1 by setting the appropriate switches on the PACE Development System Control Panel (refer to the UDS1 Users Manual). The Monitor System will then ask you to identify the available peripheral devices by displaying the following:

   MONITOR
   PERIPH:

3. Type in the peripheral name designations. For Example; if all peripherals are available, type in *AL. The Monitor will then ask you to type in a command by displaying the colon prompt symbol (:).

4. Transfer control to the program you wish to access by typing in the Execute Disc File Command. For example, to transfer control to the Editor, type the following:

   @ EDITOR (CR)

   The Editor will then prompt for a command with a question mark (?). Editor commands are described in the Editor Users Manual.

5. To transfer control from the Editor to another Main Program, type in the command "@ filename." For example, to transfer to the assembler, type the following:

   ?@P8012ASM (CR)

   Or, to return to the Monitor, type:

   ?@(CR)

6. Upon completing your work at the Console, first remove your diskette(s) from the dual floppy disc drives, then turn off the power to the drives and the Control Panel. See Universal Development System Users Manual and Universal Development System Editor Users Manual. See also Preface for a list of related publications.

10.2.1 Hardware Support

The UDS hardware components consist of dual floppy disc drives mounted in a stand-alone enclosure, a Disk/CRT Interface Printed Circuit Card (containing disk input/output firmware), and the Universal Development System. UDS1 will also support several peripherals, such as, a Teletype (TTY), a Documation M300 Card Reader, a Centronics 702 High-Speed Printer, a Plessey 1000 CPS Paper Tape Reader, and a Hazeltine 1500 or equivalent CRT; refer to figure 10-2.

10.2.1.1 Dual Diskette Drives

The dual disc drive enclosure contains two floppy disc drives and the power supplies required by the drive electronics and mechanisms. Each drive can accept a diskette capable of storing over 2.5 million bits (aproximately 158,000 16-bit words). A single-element read/write head is used in each drive and straddle erase elements provide erased areas between data tracks to ensure diskette interchangeability between drives. Each diskette contains 77 tracks, addressable as 0 through X'4C, or 616 sectors, addressable as 0 through X'267.

10.2.1.2 Disk/CRT Interface Card

The Disk/Interface Card provides interfacing between the microprocessor, the dual disk drives, and a CRT terminal. The disk input/output firmware, contained in ROMs mounted on the Disk/CRT Interface Card, provides control of the disk mechanisms, data transfer, and a diskette formatting.

PDSKIO (PACE Disk I/O) is the firmware program responsible for the communication between the Universal Development System and the floppy disk. It resides on the Disk/CRT Interface Card and supports a two drive disk system. The UDS1 TTY firmware on the TTY/Card reader Interface Card handles data transfer between PACE and terminal at transmission rates of either 300 or 1200 baud to the EIA RS-232 Interface and 110 baud to the 20-milliampere current loop for the Teletype (TTY). For additional information, refer to the Universal Development System Users Manual.

10.2.1.3 Universal Development System

The Universal Development System is a flexible tool designed to facilitate the functions and operations involving UDS1. The system provides an economical and convenient means of expediting the development of both hardware and software with UDS1.

UDS1 requires an Universal Development System with 12K of memory and a heavy duty power supply for its minimum configuration. Development Systems with model serial numbers 6150 and above will accommodate the required hardware without any additional modifications.

10.2.1.4 Peripherals

Peripherals linked with the UDS1 Development System are as follows:

- Documation M300 Card Reader
- ASR-33 Teletype (TTY)
- Plessey 1000 CPS Paper Tape Reader
- Centronics 702 High-Speed Printer
- Hazeltine 1500 Video Display Terminal

The user has the option of using the various peripherals by connecting the hook-up (extended from the peripheral) to the designated peripheral interface card enclosed within the Universal Development System (refer to figure 10-3).

10.2.2 Software Support

The main software components of the Universal Development System are as follows:

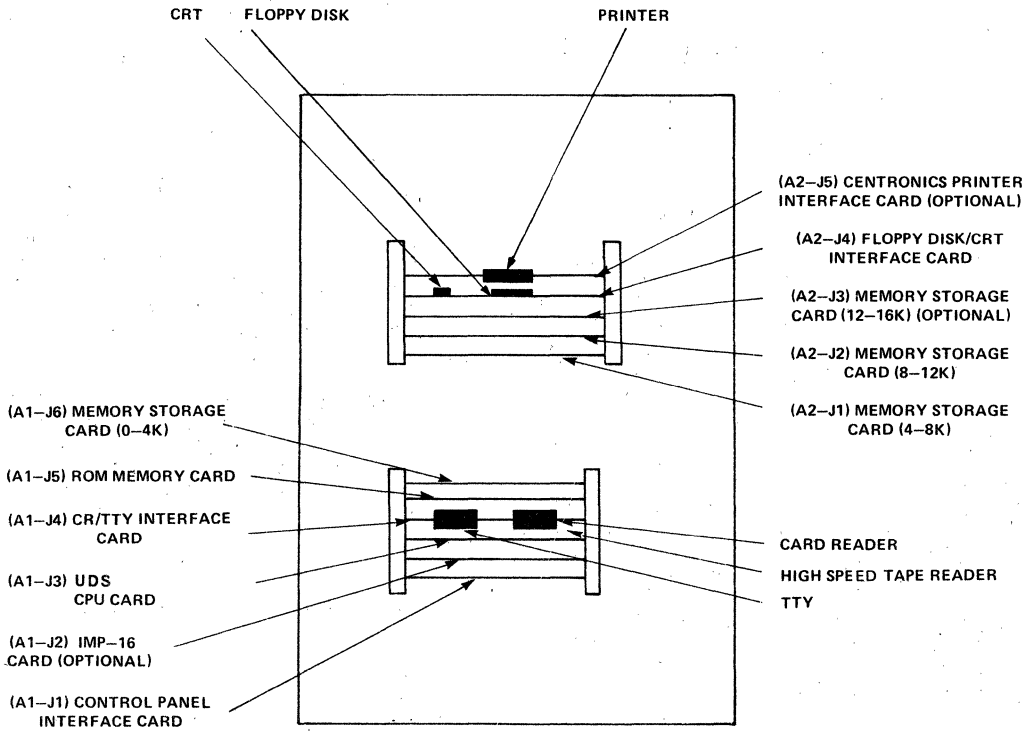


Figure 10-3. Top Internal View of Universal Development System

Stored in ROM

- Monitor System (MONITOR)
- File Input/Output Subsystem (FIOSYS)

Stored on Diskette

- File Manager (PACFM)
- Supporting System Software

10.2.2.1 Monitor System (MONITOR)

The Monitor System (MONITOR) resides on the Read-Only Memory (ROM) card. It provides control over system configuration and linkage to the Paper Tape Loader, Card Read Loader, Diskette, and the Debug Subsystem.

10.2.2.2 File Input/Output Subsystem (FIOSYS)

The File Input/Output Subsystem (FIOSYS) is a collection of software subroutines that reside on the Read-Only Memory (ROM) Card. These software subroutines provide the means of peripheral communication required by the remainder of the Universal Development System.

10.2.2.3 File Manager Program (PACFM)

The File Manager Program (PACFM) is a disk-resident manager of the directories on the disk. It gives the user control over file maintenance, space allocation and deallocation, and file protection. The files are identified by name, with the sector assignment handled automatically.

10.2.2.4 Supporting System Software

A disc-resident software package resides on a Master Diskette and includes a number of programs provided with the Universal Development System. These programs are described briefly below.

10.2.2.5 PACE 12K Resident Assembler (PAC12ASM)

The PACE 12K Resident Assembler (PAC12ASM) is a three-pass assembler, with macro capabilities, that loads and executes on a PACE Development System. The assembler accepts free-format PACE assembly language source statements as source input, assembles the statements, and outputs a program listing and/or a load module (LM) on paper tape or diskette. The load module can be loaded by the appropriate PACE loader, then executed, or it may be converted to a Main Program by LINKEDIT. The operating instructions for the assembler are contained in the PACE Macro Assemblers Operating Instructions. Information on the PACE assembly language, including instructions, directives, the assignment statement, macros, and the assembler input/output formats is contained in the PACE Assembly Language Programming Manual.

10.2.2.6 Cross Assemblers for 8060, 8070, and 8080 (See Section 10.3)

10.2.2.7 UDS1 Editor (EDITOR)

The UDS1 Editor program (EDITOR) allows a user to read, write, correct, display, and save source files. The Editor may be used to generate source files in a format suitable for input to the PACE assembler, other cross assemblers, or the PACE BASIC interpreter; or the Editor may be used to generate documentation such as lists, tables, directories, or manuals. Refer to the UDS Editor Users Manual for a complete description of the Editor program.

10.2.2.8 Linkage Editor (LINKEDIT)

The Linkage Editor (LINKEDIT) is a relocating and linking loader program that links one or more Load Modules (LMs) produced by the PACE Resident Assembler (PAC12ASM). LINKEDIT performs relocation and resolves external linkages, and writes a memory image to the disc in a format suitable for bootstrapping into memory for execution.

Each LM must be in the standard format (as described in the PACE Assembly Language Programming Manual). Each LM and the commands that control the loading process are then input to LINKEDIT. LMs can be input from cards, paper tape, or from the disc itself.

10.2.2.9 Diskette Diagnostic Program (PFDDIA)

The Diskette Diagnostic Program (PFDDIA) is a complete diagnostic program for checking out the diskettes and the disc drives. In addition, PFDDIA initializes the diskette, the diskette's File Directory, and system tables.

10.2.2.10 UDS1 Utility Programs

The UDS1 Utility Programs consist of the following:

- DPATCH (disc-patching utility)
- LIST (file-listing utility)
- IPCOPY (IMP to PACE copy)
- UPROM (Universal PROM Programming Software)
- XREF (Symbol-Listing Utility)

DPATCH is used during debugging to make corrections to Main Program files on diskettes. LIST is used to list any file on a diskette and provides numerous editing and formatting options. IPCOPY is used to convert an existing file on an IMP-16P diskette to an equivalent file on a PACE diskette. UPROM is used to convert a PACE, 8060, 8070, 8080, or IMP-16P LM to the proper format for generating a PROM or ROM. XREF is used to generate a cross- reference listing of the symbols contained in a symbolic file on disk.

10.3 INS8080A CROSS ASSEMBLER

The UDS1 Macro Assembler Programs are three-pass assemblers that are loaded and ex-

ecuted on a Universal Development System. The assemblers accept free-format assembly language source statements of a target microprocessor as source input, assemble the statements, and output a program listing and/or a load module (LM). The target microprocessor is the microprocessor that will execute the object (machine) code contained in the load module. For example, the UDS1 Macro Assembler accepts 8080 assembly language source statements and produces a load module. The load module may be loaded by an appropriate loader and executed by the target microprocessor. The load module may also be used to program PROMS.

Salient features of the PACE Assemblers are as follows:

- DOS Capabilities (12K Assemblers Only)
- Conditional Assemblies using the following Operators
  - IF Directive
  - ELSE Directive
  - ENDIF Directive
  - IFC Directive
- Macros with the following features
  - Parameter driven Macros
  - Local Symbols
  - Parameters called by number
  - Macro Time Looping
  - Nested Macro Calls
  - Nested Macro Definitions
  - Recursive Macro Calls
- Absolute Load Module Generation
- Relocatable Load Module Generation (PACE Assembler Only)
- Assembly Time Operators (+ − ★ / % & ! < = > ^ EQ NE)
- Parenthesized expressions (SC/MP and 8080 Assemblers Only)
- Diagnostic Messages that include Error Position in Source Line
- Wide Variety of Directives
- User Control over allocation of Literal Pool and Pointer Space (PACE Assembler Only)

For information on the assembly languages, see the appropriate Assembly Language Programming Manual. Input/Output device options are listed in table 10-1.

The UDS1 Editor provides the normal method used for generating and/or correcting source programs on paper tape or diskette.

8080A Microprocessor programs may be assembled by using the 8080A cross assembler program in the Universal Development System (UDS1).

Program Number	Program Name	Title and Description
430305394-000	P8012ASM	PACE 8080 Cross-Assembler 12K version. An 8080 Cross-Assembler for the Universal Development system requires 12K and uses NSC Assembler Directives.

Table 10-1. Assembler Peripheral Options

Function	Peripheral Options
Control Input	Teletype® or CRT/Keyboard
Source Input	Teletype Paper Tape Reader High Speed Paper Tape Reader Card Reader (12K and DOS only) Dual Diskette (12K and DOS only)
Program Listing Output	Teletype Printer High Speed Printer CRT Dual Diskette (12K and DOS only)
Load Module Output	Teletype Paper Tape Punch Dual Diskette (12K and DOS only)

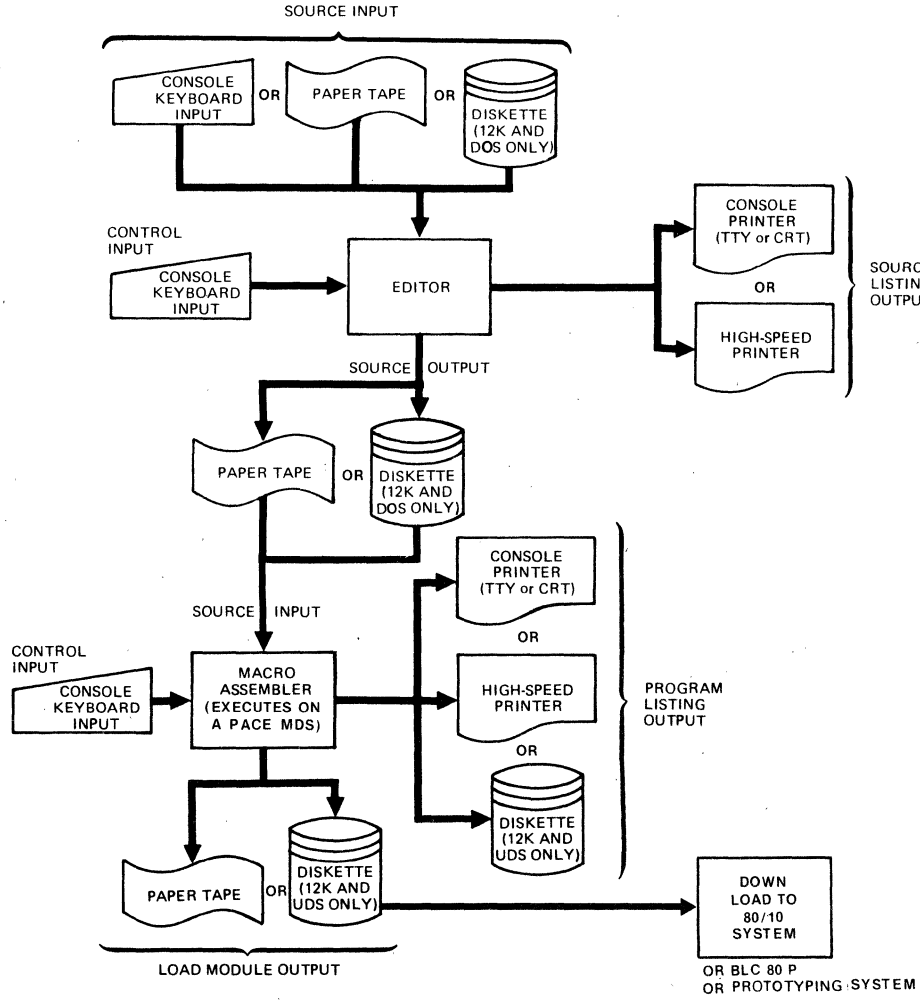


Figure 10-4. Operational Sequence of the UDS1 Editor and Assemblers

10.4 PROM PROGRAMMING

10.4.1 UDS1 PROM Programmer (Peripheral)

Because of the requirement that microprocessor based equipment be ready to operate when power is turned on, most manufacturers store their applications software in read-only memory (PROMs or ROMs) so that it is always ready for execution.

Even in an environment where application programs are read into memory from off-line storage for exection, it is advantageous to put often-used routines in ROM or PROM so that they are available without the overhead involved in loading them each time.

A critical factor in the development of microprocessor software is the capability of the user, once he has completed initial checkout, to program PROMs with the necessary routines and data for continued checkout and, perhaps, initial production. Then, after his product has been in the field for initial shakeout, he will need to make programming tapes from these same PROMs in order to commit his product to masked ROMs for the additional cost savings.

One of the major advantages of owning a "Universal Development System" is that program development may be done right in the lab without the need for outside services.

The Data I/O Model 7 and 9 PROM Programmers connnected to our Universal Development System (UDS1), provide these facilities. (See PROM Prograsmmer Software Manual and Data I/O Company for peipheral ordering information.) This gives the UDS1 user a complete, integrated, efficient capability for microprocessor software development. The Model 7 and 9 programmers are directly interfaced to UDS1 via a slave RS-232 serial I/O port.

The software package to support the programmer is PROM-independent. The Model 7 and 9 are "universal" PROM Programmers, which can program any of the widely used PROMs with only a change of a personality card or adapter. Generally personality cards and adapters are available as soon as the PROM itself is available.

The UDS1 PROM Programmer is interfaced to UDS through an RS-232 serial port. This port is located on a card which contains other RS-232 ports, such as a port for a serial link to one or more prototyping systems.

An additional advantage of the Model 7 and 9 programmers is the customer suppport provided by Data I/O. They provide publications such as PROM comparison charts, field bulletins which describe improved programming techniques, and technical bulletins which also discuss programming techniques and specific subjects related to programmers and specific PROMs. They also provide field service, usually through a direct field service department.

The Model 7 Programmer is a fairly basic programmer designed expressly for interfacing to a microprocessor through a serial interface of up to 9600 baud. Although the Model 9 is priced higher, it can be used stand alone as well as connected to a microprocessor system.

By insertion of the proper personality card and socket adapter, the PROM Programmer can be set up to program any of the most widely used PROMs:

National

2708, 2716, 1702A, 5204, 54/74S570, 54/74S387, 54/74S287, 54/74S470, 54/74S472, 54/74S572, etc.

Intel

1702A, 2704, 2708, 2716, 8748

Motorola

2-5003, 10149 ECL, 68708 (2708)

AMD

2708, 1702A

Electronic Arrays

2708

Fairchild

93438, 93448, 93452, 93453

As other PROMs are developed, additional personality cards and socket adapters allow use with the PROM Programmer.

The capabilities of the PROM Programmer and the UDS1 Software package are:

- Input of any standard NSC Load Module (LM) from paper tape or diskette.
- Input of UDS Main Program (MP) files from diskette.
- Input of binary (BI), binary complement (BC), or BPNF PROM programming tapes.
- Input or editing of hexadecimal or binary data from system console.
- PROM duplication, by performing READ of one PROM; then PROGRAM a duplicate PROM.
- Generation of BI, BC, or BPNF ROM programming tapes from input data or PROM data.
- Test of PROM for proper erased condition.
- PROM verification.
- Printout of PROM data, memory data, PROM checksum or write-buffer checksum on console or high-speed printer.
- Extensive legality checks of input data.
- Handling of portions of single programs as well as of multiple programs.
- Automatic setting of buffer to unprogrammed state.
- Interruption of long operations other than programming and, loading or punching of binary tapes.
- Programming of PROMs directly from UDS1 memory.

The Data I/O Model 7 and 9 programmers operate as a peripheral to National's UDS1 as shown in figure 10-5.

Detailed information on the Model 7 and 9 PROM Programmers and general information on PROM usage and PROM programming can be obtained from:

Data I/O
990 East Arques Avenue, Suite 106
Sunnyvale, California, 94086
(408)732-8246

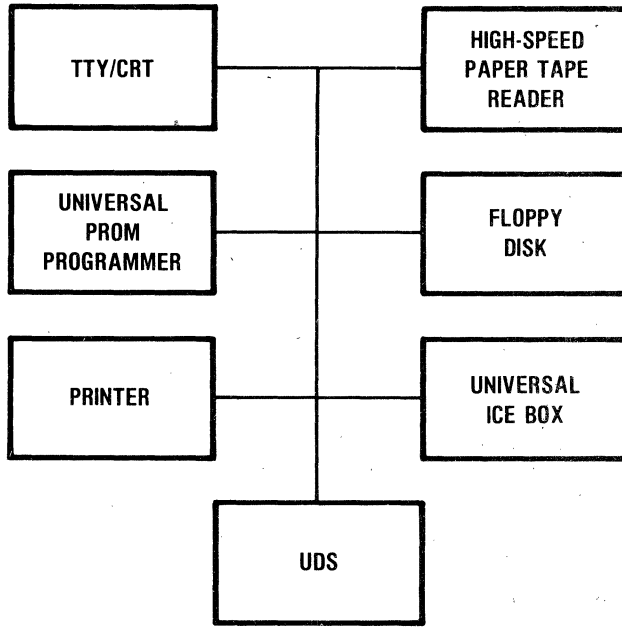


Figure 10-5 Universal Development System Configuration

10.4.2 UDS Serial Link Card

This optional card available at extra cost, plugs into a Universal Development System (UDS1). The card has an RS-232 Port which can be used to link the Data I/O Prom Programmer to the Universal Development System.
See section 10.4.1

10.5 SERIES/80 FAMILY INCLUDING UNIVERSAL PROTOTYPE BOARD (BLC905)

This section presents a brief description of the devices available.

Series/80 from National Semiconductor is an expanding new concept in OEM computer planning and design. A growing and varied family of microcomputer products based on the National BLC 80/10 Board Level Computer, Series/80 gives the user more options for flexible design by offering an increasing variety of memory, supporting periphrals, and design packaging alternatives.

The BLC 80/10 is a direct plug-for-plug replacement for the SBC 80/10.

Complete system design is facilitated by a variety of prototype packages, board chassis and power supplies.

10.5.1 Series/80 System Design Aids (BLC 80P Prototype Package)

Prototype Package includes:

- BLC 80 Board Level Computer
- BLC 604 System Card Cage
- BLC 905 Universal Prototype Board
- BLC 910 System Monitor

The BLC 905 Universal Prototype Board is available separately as are the other items listed. The BLC 905 allows the user to design and construct customized BLC-related circuits. The BLC 910 System Monitor is supplied with the kit in two preprogrammed MM2708 EPROMs. The Monitor enables the user to load, execute and debug BLC 80/10-related programs, and to examine and modify any RAM location or CPU register.

10.5.2 Board-Level Computers

The BLC 80/10, 80/11, 80/12, 80/14, and 80/204 are complete computers on a board. They use the National 8080A microprocessor and have on-board RAM memory and sockets for ROM/PROM memory. Expansion boards are available to increase system memory and I/O capabilities.

- Series/80 BLC 80/10

  The BLC 80/10 is a self-contained single board computer. It includes the central processor, system clock, RAM and ROM memories, I/O lines, serial communications interface, and the bus logic and drivers on a 6.75 inch by 12.00 inch printed circuit board. The BLC 80/10 is plug compatible with SBC 80/10.

- Series/80 BLC 80/11, 80/12, 80/14

  The BLC 80/11, 80/12, and 80/14 share all basic features and capabilities of the BLC 80/10 but add jumper-selectable I/O pins for RS-232 interface and have greater memory capacity.

- BLC 80/204

  The BLC 80/204 is a plug-for-plug replacement for the Intel SBC 80/204. It is completely bus-compatible with Series/80 boards, system peripherals, and expansion boards. The BLC 80/204 has parallel and serial interfaces, an interval timer for three software-controlled 16-bit counters (two of which may be cascaded to 32 bits), and eight vectored interrupts.

10.5.3 OEM Rack Mountable Computers (RMC 80-10, 80/14, 80/204)

National Semiconductor rack-mountable computers (RMC 80/10, 80/14, and 80/204) can be easily incorporated into OEM-designed systems. They are complete and self contained. The National RMC line combines a Series/80 Board Level Computer with front panel, on/off and reset switch, power supply, system monitor firmware, and capacity for up to three Series/80 expansion boards -- all in one 3-½ inch RETMA chassis.

10.5.4 Memory Boards

Expansion MOS RAM boards of 16K, 32K, 48K, and 64K bytes and expansion ROM, PROM, EPROM, cards in 16K or 32K capacities are available. All are plug-for-plug replacements for corresponding Intel SBC memory boards.

10.5.5 Input/Output and Memory Expansion Boards

Input and output port capacity can be expanded with boards that provide different configurations of I/O ports and expansion memory.

10.5.6 BLC 604 System Chassis and BLC 614 Expansion Board Cage

The BLC604 system Chassis and BLC614 Expansion Board Cage provide immediate and

economical solutions for housing, interconnection, and expansion of Series/80 systems. Stand-alone BLC 604 or 614 Board Cage holds up to four Series/80 systems. Stand-alone BLC 604 or 614 Board Cage holds up to four Series/80 boards in a molded chassis with interconnection backplane, bus signal terminating networks, and connectors.

10.5.7 RMC 660 System Chassis

The RMC 660 Systems Chassis suports the Board Level Computer and full complement of Series/80 expansion boards. The Chassis includes board cage for eight boards. The Chassis includes board cage for eight boards, seven-inch standard RETMA chassis, and BLC 665 heavy duty power supply. It also includes power-fail detect for orderly power-down sequence, and has current-limited outputs with overvoltage protection. Power on-off and reset switches on front panel are connected to system bus for external system control.

10.5.8 BLC 635 Power Supply

Ready-made, low cost power for BLC 80/10, 11, 12, 14, and 204 is provided by the BLC 635 power supply. It supports most configurations of BLC memory, and I/O expansion boards. DC power is provided on mating cables for direct connection to BLC 604 System Card Cage. The BLC 635 senses AC power failure and generates a TTL signal for orderly system power shutdown. It has current-limited outputs with over-voltage protection, and 100, 115, 200, 230, VAC input voltage; 50/60 Hz input frequency.

10.5.9 BLC 665 Heavy Duty Power Supply

The BLC 665 supplies approximately twice the rated current of the BLC 635. The BLC 665 will power a fully loaded BLC 80/10 and most combinations of seven additional expansion boards.

See National Semiconductor publications:

- Series/80 BLC 80P Prototyping Package Users Manual
- BLC 80/10 Hardware Reference Manual
- Series/80 Microcomputer System Brochure

10.6 PUBLICATIONS

Publications are available covering the various devices manufactured by National Semiconductor. The available literature is grouped in the following categories:

- Literature Index
- Handbooks
- Manuals
- Linear Applications, Vol I and II
- Databooks
- Guides
- Product Selection Guides
- Briefs
- Individual Application Notes
- Individual Data Sheets

See appendix C for more detailed reference material. For list of currently available literature, refer to the Literature Index.

10.7 TRAINING

National Semiconductor operates two microprocessor training centers: in Santa Clara, Calif., and in Boston, Mass. Each training center is fully equipped and professionally staffed to provide students with a good mix of hardware/software theory and hands-on laboratory experience. Courses offered are Microprocessor Fundamentals, 8060 SC/MP Applications, and complex peripherals. A brochure is available that describes the courses.

Microprocessor Fundamentals - 4-½ Days

A course intended for engineers, senior technicians, managers, and others who may have little or no experience with microprocessors or computers. The Fundamentals course provides a sound introduction to microprocessors and microcomputers and their potential applications. The course also provides a comparison of various types of microprocessors, and provides an insight on their appropriate applications. Extensive lab sessions allow the participant to become familiar with use of Development Systems and microprocessor programming.

OUTLINE

Monday - Getting Started

1. Microprocessor Concepts and Terminology
2. Review of Digital Logic, Boolean Algebra, and Number Systems
3. Microprocessor Architecture, Instructions, Addressing
4. Introduction to Programming - Flowcharting, Coding
5. Lab - Operating a Microcomputer Load and run a simple program

Tuesday - Learning the Tools

1. Assembly Language Instruction Set
2. Microprocessor Development Systems
3. Software Development Tools - Editors, Assemblers
4. Lab - Using the Development System

Wednesday - Getting Involved

1. Additional Addressing Modes
2. Programming Techniques
3. Software Development Tools - Loaders
4. Lab - Programming with the Development System

Thursday - Putting it all Together

1. Microprocessor System Design Considerations
2. Microprocessor Applications
3. The Floppy Disk Universal Development System
4. High Level Languages
5. Lab - Develop a Moderately Difficult Program

Friday (Morning only) - Wrapping it up

1. Review, Questions and Answer Session
2. Survey of Microprocessors and Appropriate Applications
3. Lab - Complete Programming Exercises

Complex Peripheral Chips for Microprocessors -3 Days

This course is intended for the engineer with microprocessor system design experience, who needs applications information on the many complex peripheral chips available for microprocessors. Although oriented towards the 8080A it is appropriate for those using any of the popular microprocessors (8085, Z80, etc.). The MICROBUS™ is explained in detail, followed by sessions on interfacing the various support chips to the MICROBUS™. This intensive course covers some 20 complex support chips, so to keep the class reasonably short, lab sessions have not been included. This course can save you weeks of time and stimulate new microprocessor ideas.

OUTLINE

Day 1 - The MICROBUS™, Parallel Ports and Other I/O Devices

1. Definition
2. Description - Data, Address, and Control Bus
3. Interface - Implementing the MICROBUS™
4. Octal Latch - INS82C06/MM74CS74
5. 8 Bit I/O Port - INS8212
6. Bit Programmable Peripheral Interface -INS8254
7. Programmable Peripheral Interface -INS8255
8. A/D Converter - INS8292
9. Programmable Interrupt Controller -INS8259

Day 2 - Communications: Concepts and New Devices

1. Serial Codes
2. 20ma Current Loop and RS232 Interfaces
3. Modems and Line Protocol (BISYNC, SDLC)
4. Programmable Communications Interface - INS8251/INS8261/INS2651
5. Multi-protocol Communications Controller - INS8274/INS2652
6. Asynchronous Control Element - INS8250
7. Programmable Interface Timer - INS8253
8. DMA Controller - INS8257

Day 3 - Floppy Disk Drive and CRT Terminal Design

1. Floppy Disk Drive Overview
2. Floppy Disk Controller/Formatter -INS1771-1
3. Keyboard Encoder - INS8244
4. Programmable CRT Controller - DP8350
5. Character Generator - INS8285/DP8678
6. Example System: CRT Terminal

10.8 NATIONAL'S MICROPROCESSOR USERS GROUP

National Semiconductor sponsors a microprocessor users group and a monthly newsletter, both called COMPUTE, as a service to users and potential users of National's microprocessors, and for anyone else who is interested in what is going on in the microprocessor industry. This provides a forum for members to exchange ideas, opinions, software, and products. National maintains the group's software library as a service to COMPUTE members. Products, services, and software offered for sale by COMPUTE members will often be published in the newsletter.

The newsletter is packed with articles on microprocessors and peripherals. In addition, there are:

- Product Announcements
- Application Notes
- Construction Projects
- Programming Hints
- Programming Aids
- Microprocessor Class Schedules
- Consultant Lists
- Announcements of Coming Events
- Literature Reviews
- Data Sheets
- Letters to the Editor
- Library Program Listings
- Contents
- Services
- Classified Ads

In summary, everything you need to know about microprocessors.

The software library contains utility programs, math routines, I/O routines, games, assemblers, compilers, translators, etc. Most of the library program listings are free; source paper tapes are available for a nominal charge.

National Semiconductor is not responsible for software in the software library, and will not provide applications support for that software. Descriptions published are those of the contributor, and National cannot guarantee their accuracy or the applicability of the software. Any product, service, or software offered for

sale in the newsletter is the responsibility of the person or company who offers it. Publication in COMPUTE does not constitute endorsement by National Semiconductor. Of course, any products or services offered for sale by National Semiconductor in the newsletter, will carry National's normal warranty and applications support.

You are invited to join COMPUTE, National's microprocessor users group. A lifetime membership to COMPUTE will cost you only $15.00 (DLR 15.00 for Australia) - a real bargain!

10.9 TECHNICAL SUPPORT PROGRAMS

National Semiconductor has the strongest on-the-scene technical support team - in the U.S and abroad - of any semiconductor manufacturer. Our large network of independent sales representatives and franchised distributors is backed by our Field Application Engineers (FAE's) and microprocessor applications engineers. The FAE's are available domestically and internationally to offer on-site technical assistance, and are equipped technically to help analyze your application, translate your needs into a viable hardware/software configuration, and then follow it through to system delivery. The microprocessor applications engineers are National's home-base technical-support specialists who support the FAE's in the field, and who help you use your microprocessor most effectively; they are always available to answer specific technical questions regarding the use of National's microprocessor and peripheral components.

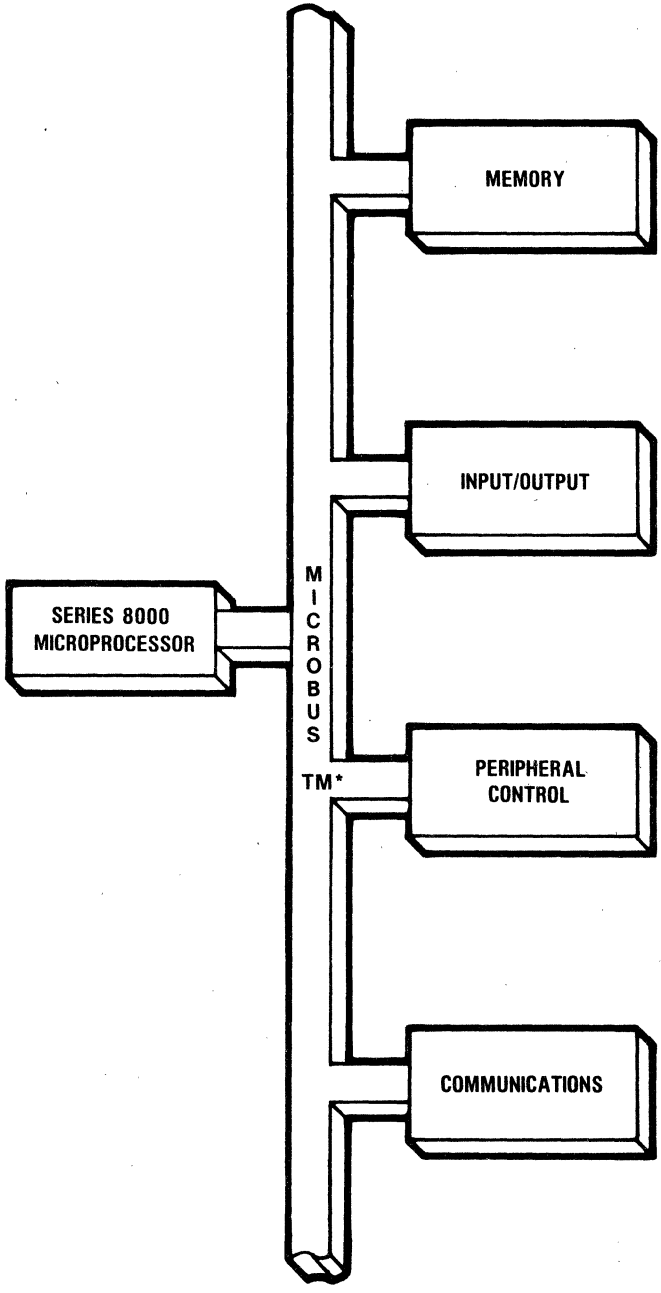
10.10 MICRO+ PROGRAM (QUALITY CONTROL AND TESTING PROCESS)

The MICRO + Program from National Semiconductor is a specially designed quality control and testing process that ensures our microprocessor parts meet extraordinary standards of quality and reliability. The MICRO+ Program serves users who cannot perform incoming inspection of microprocessors or who need significantly better quality and higher reliability levels than normally required.

Users who specify MICRO+ processed parts will find that the program offers the following benefits:

- Reduces the cost of reworking assembly boards
- Reduces field failures
- Simplifies system checkout
- Reduces equipment downtime
- Eliminates the need for, and thus the added cost of, independent testing laboratories
- Reduces the need for excess inventories due to yield loss incurred as a result of processing performed at independent testing laboratories
- Eliminates incoming electrical inspection

To provide a high quality level to all outgoing parts, an Acceptable Quality Level (AQL) is established. The AQL is the percentage of faulty devices that escape detection during inspection and testing at the manufacturer's facility; with the MICRO+ Program, the AQL is reduced to such an extent that the customer can eliminate incoming inspection and test.



Chapter 11
Programming

* Trademark, National Semiconductor Corporation

Programming

11.1 INS8080A INSTRUCTION SET

Five different types of instructions are included in the 8080 instruction set. These are:

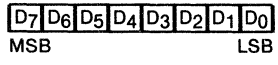
- Data Transfer Group — moves data between registers or between memory and registers.
- Arithmetic Group — Adds, subtracts, increments or decrements data in registers or in memory.
- Logical Group — AND, OR, EXCLUSIVE OR, compare, rotate, or complement data in registers or memory.
- Branch Group — Conditional and unconditional jump instructions, subroutine call instructions and return instructions.
- Stack, I/O and Machine Control Group — I/O, stack maintenance, and flag control.

11.1.1 Instruction and Data Formats

Memory for the 8080 is organized into 8-bit groups called bytes. Each byte has a unique 16-bit binary address corresponding to its sequential position in memory.

The 8080 can directly address up to 65,536 bytes of memory, which may consist of both read-only memory (ROM) elements and random-access memory (RAM) elements (read/write memory). Data in the 8080 is sorted in the form of 8-bit binary bytes:

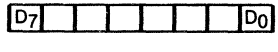
DATA WORD



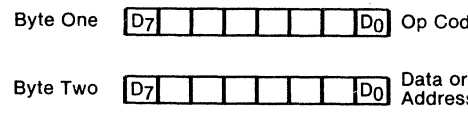
In the 8080, the Least Significant Bit (LSB), is called BIT 0, and the Most Significant Bit (MSB), is referred to as BIT 7 (of an 8-bit byte).

The 8080 instructions are one, two or three bytes in length. Multiple byte instructions must be stored in successive memory locations. The address of the first byte is always used as the address of the instruction. The exact instruction format will depend on the particular operation to be executed.

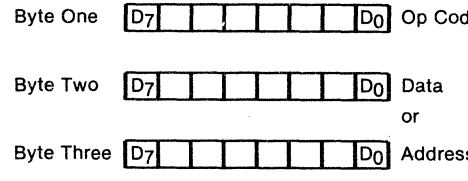
Single Byte Instructions



Two-Byte Instructions



Three-Byte Instructions



11.1.2 Addressing Modes

The 8080 machine code is stored sequentially in memory. Multi-byte data is stored in successive memory locations, starting with the least significant byte, and ending with the most significant byte. The 8080 has four different modes for addressing data stored in memory or in registers:

- Direct — Bytes 2 and 3 of the instruction contain the exact memory address of the data item. Byte 2 contains the low-order bits of the address. Byte 3 contains the high-order bits.
- Register — The instruction specifies the register or register-pair in which the data is located.
- Register Indirect — The instruction specifies a register-pair which contains the memory address where the data is located. The high-order bits of the address are in the first register of the pair, the low-order bits are in the second.
- Immediate — The instruction contains the data itself. This is either an 8-bit quantity or a 16-bit quantity (least significant byte first, most significant byte second).

Unless otherwise directed by an interrupt or branch instruction, the execution of instructions proceeds through consecutively increasing memory locations. A branch instruction can change the address of the next instruction to be executed in either of two ways. They are:

- Direct -The branch instruction contains the address of the next instruction to be executed. Except for the "RST" instruction, byte 2 contains the low-order address and byte 3 the high-order address.

- Register Indirect -The branch instruction indicates that the HL register pair contains the address of the next instruction to be executed. The high-order bits of the address are in the H register, the low-order bits in the L register.

The RST instruction is a special one-byte call instruction (usually used during interrupt sequences). RST includes a three-bit field; program control is transferred to the instruction whose address is eight times the contents of this three-bit field.

11.1.3 Condition Flags

There are five condition flags associated with the execution of the 8080 instructions. They are Zero, Sign, Parity, Carry, and Auxiliary Carry. Each is represented by a 1-bit register in the CPU. A flag is "reset" by forcing the bit to 0. Unless otherwise indicated, when an instruction affects a flag, it does so in the following manner:

Zero: If the result of an instruction has the value 0, this flag is set; otherwise it is reset.

Sign: If the most significant bit of the result of the operation has the value of 1, this flag is set; otherwise it is reset.

Parity: If the modulo 2 sum of the bits of the result of the operation is 0, (i.e., if the result has even parity), this flag is set; otherwise (i.e., if the result has odd parity) it is reset.

Carry: If the instruction resulted in a carry (from addition), or a borrow (from subtraction or a comparison) out of the high-order bit, this flag is set; otherwise it is reset.

Auxiliary Carry: If the instruction caused a carry out of bit 3 and into bit 4 of the resulting value, the auxiliary carry is set; otherwise it is reset. This flag is affected by single precision additions, subtractions, increments, decrements, comparisons, and logical operations, but is principally used with additions and increments preceding a DAA (Decimal Adjust Accumulator) instruction.

11.1.4 Presentation Format

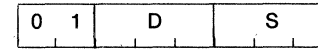
Figure 11-1 indicates the format used for describing each instruction. The symbols utilized are listed in table 11-1. (See page 11-3.)

11.1.5 Data Transfer Group

This group of instructions transfers data between registers or between registers and memory. Data may be transferred one byte at a time or two bytes at a time, depending on whether a single register or register pair is specified by the instruction. Condition flags are not affected by any instruction in this group.

MOVE REGISTER

MOV r1, r2



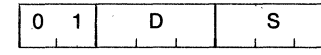
(r1) ← (r2)

The content of register r2 is moved to register r1.

Cycles: 1
States: 5
Addressing: register
Flags: none

MOVE FROM MEMORY

MOV r, M



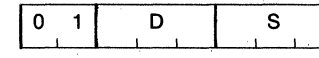
(r) ← ((H) (L))

The content of the memory location, whose address is in registers H and L, is moved to register r.

Cycles: 2
States: 7
Addressing: register indirect
Flags: none

MOVE TO MEMORY

MOV M, r



((H) (L)) ← (r)

SUBTRACT REGISTER — OPERATION

SUB r — MNEMONIC

1	0	0	1	0	S

OP CODE

(A) ← (A) − (r) — SYMBOLIC REPRESENTATION

The content of register r is subtracted from the content of the accumulator. The result is placed in the accumulator. — DESCRIPTION

Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC — FLAGS AFFECTED BY THE INSTRUCTION

Figure 11-1. Presentation Format

Table 11-1. Symbols and Notations

Symbol and Notation	Meaning
A	Register A (Accumulator)
B	Register B
C	Register C
D	Register D
E	Register E
H	Register H
L	Register L
M	Memory Byte (Address in HL register pair)
D,S	The bit pattern designating destination or source. (D = Destination, S = Source):

D or S	Designation	
000	B	Register
001	C	
010	D	
011	E	
100	H	
101	L	
110	M	Memory
111	A	Accumulator

Symbol and Notation	Meaning
byte 2	The second byte of the instruction.
byte 3	The third byte of the instruction.
port	8-bit address of an I.O device.
r,r1,r2	One of the registers A,B,C, D,E,H,L
PC	16-bit program counter register (PCH and PCL are used to refer to the high-order and low-order 8 bits, respectively.)
SP	16-bit stack pointer register (SPH and SPL are used to refer to the high-order and low-order 8 bits, respectively).
( )	The contents of the memory location or registers enclosed in the parentheses
←	"Is replaced by"

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Table 11-1 Symbols and Notations (Continued)

Symbol and Notation	Meaning
∧	Logical AND
⊻	Exclusive OR
∨	Inclusive OR
+	Addition
–	Twos complement subtraction
*	Multiplication
← →	"Exchange"
—	The ones complement (for example, $(\overline{A})$)
n	The restart number 0 through 7
N	The binary representation 000 through 111 for restart number 0 through 7, respectively
•	"Not affected"
0	"Reset"
1	"Set"
x	Unknown
↕	Flags affected according to Standard Rules, except as noted
RP	The bit pattern designating a register pair.
rp	The mnemonic designating a register pair.

rp	RP	Register Pair
B	ØØ	B-Pair (B and C)
D	Ø1	D-Pair (D and E)
H	1Ø	H-Pair (H and L)
SP	11	SP (Stack Pointer Register)
PSW	11	PSW (Processor Status Word) Consisting of Accumulator and Flag Register.

Note: Mnemonic PSW generates 11 for certain instructions, therefore SP is invalid for them.

Symbol and Notation	Meaning
data 16	16 bit data quantity.
C	Bit combination in branch instruction

C	Flag	Condition
ØØØ	(Z = Ø)	NZ-Not zero
ØØ1	(Z = 1)	Z-zero
Ø1Ø	(C-Y = Ø)	NC-No carry
Ø11	(C-Y = 1)	C-carry
1ØØ	(P5Q) P=0	PO-parity odd
1Ø1	(P = 1)	PE-parity even
11Ø	(S = Ø)	P-plus
111	(S = 1)	M-minus

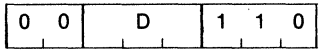
addr	16-bit address quantity
addr H	High-order address byte
addr L	Low-order address byte
data	8-bit data quantity
data H	High-order data byte
data L	Low-order data byte
rH	The high-order register of a designated register pair
rL	The low-order register of a designated pair
rm	Bit m of the register r (right to left, Ø through 7)

The content of register r is moved to the memory location whose address is in registers H and L.

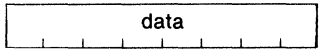
Cycles: 2
States: 7
Addressing: register indirect
Flags: none

MOVE IMMEDIATE

MVI r, data



Byte 1



Byte 2

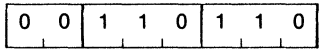
(r) ← data

The contents of byte 2 of the instruction is placed in register r.

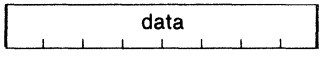
Cycles: 2
States: 7
Addressing: immediate
Flags: none

MOVE TO MEMORY IMMEDIATE

MVI M, DATA



Byte 1



Byte 2

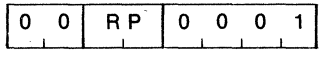
((H) (L)) ← data

The content of byte 2 of the instruction is moved to the memory location whose address is in registers H and L.

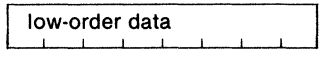
Cycles: 3
States: 10
Addressing: immediate/register indirect
Flags: none

LOAD REGISTER PAIR IMMEDIATE

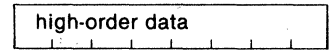
LXI rp, data 16



Byte 1



Byte 2



Byte 3

(r_H) ← $data_H$
(r_L) ← $data_L$

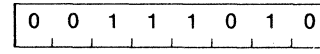
These instructions are used to load a specific register pair with a 16-bit operand. The operand immediately follows the instruction in the form of two 8-bit bytes.

Cycles: 3
States: 10
Addressing: immediate
Flags: none

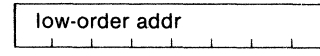
RP	(Register)
00	B-Pair (B and C)
01	D-Pair (D and E)
10	H-Pair (H and L)
11	SP (Stack Pointer)

LOAD ACCUMULATOR DIRECT

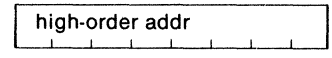
LDA addr



Byte 1



Byte 2



Byte 3

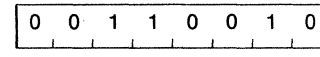
(A) ← ($addr_H$ $addr_L$)

This instruction will load the accumulator with a data byte from memory, specified by the two bytes which immediately follow the instruction.

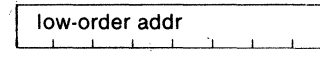
Cycles: 4
States: 13
Addressing: Direct
Flags: none

STORE ACCUMULATOR DIRECT

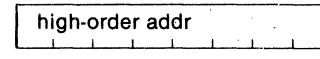
STA addr



Byte 1



Byte 2



Byte 3

($addr_H$ $addr_L$) ← (A)

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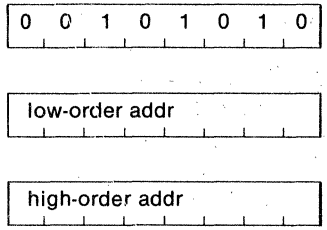
The contents of the accumulator will be stored in memory, at a location specified by the two bytes which immediately follow the instruction.

Cycles: 4
States: 13
Addressing: direct
Flags: none

LOAD H AND L REGISTERS DIRECT

LHLD addr



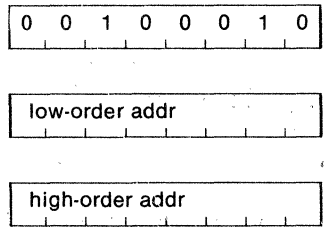
$(L) \leftarrow (addr_H\ addr_L)$
$(H) \leftarrow (addr_H\ addr_L + 1)$

This instruction enables the H and L Registers (H-pair) to be loaded with two consecutive bytes from memory. Register H is loaded by the second memory byte; L is loaded with the first memory byte, (which is specified by the two bytes that immediately follow the instruction).

Cycles: 5
States: 16
Addressing: direct
Flags: none

STORE H AND L DIRECT

SHLD addr



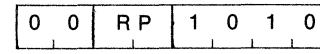
$(addr_H\ addr_L) \leftarrow (L)$
$(addr_H\ addr_L + 1) \leftarrow (H)$

The content of register L is moved to the memory location whose address is specified in byte 2 and byte 3. The content of register H is moved to the succeeding memory location.

Cycles: 5
States: 16
Addressing: direct
Flags: none

LOAD ACCUMULATOR INDIRECT

LDAX rp



$(A) \leftarrow ((rp))$

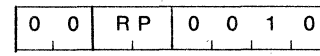
The content of the memory location, whose address is in the register pair rp, is moved to register A. Note: only register pairs B (registers B and C) or D (registers D and E) may be specified.

Cycles: 2
States: 7
Addressing: register indirect
Flags: none

RP
00 B-Pair
01 D-Pair

STORE ACCUMULATOR INDIRECT

STAX rp



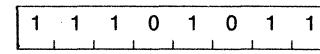
$((rp)) \leftarrow (A)$

The content of register A is moved to the memory location whose address is in the register pair rp. Note: only register pairs B (registers B and C) or D (registers D and E) may be specified.

Cycles: 2
States: 7
Addressing: register indirect
Flags: none

EXCHANGE H AND L WITH D AND E

XCHG



$(H) \leftrightarrow (D)$
$(L) \leftrightarrow (E)$

The contents of registers H and L are exchanged with the contents of registers D and E.

Cycles: 1
States: 4
Addressing: register
Flags: none

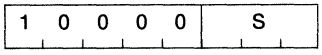
11.1.6 Arithmetic Group

This group of instructions performs arithmetic operations on data in registers and memory. Unless indicated otherwise, all instructions in this group affect the Zero, Sign, Parity, Carry, and Auxiliary Carry flags according to the standard rules. All Subtraction operations are performed using two's complement arithmetic. The carry flag is set to indicate that a borrow occurred and is cleared to indicate that no borrow occurred.

The following ADD Instructions (ADD, ADI, ADC, ACI) perform addition of a data byte or register with the accumulator, the result of the operation being placed in the accumulator.

ADD REGISTER

ADD r



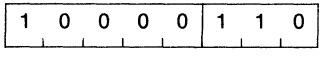
(A) ← (A) + (r)

The content of register r is added to the content of the accumulator. The result is placed in the accumulator.

Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

ADD MEMORY

ADD M



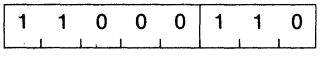
(A) ← (A) + ((H) (L))

The content of the memory location whose address is contained in the H and L registers is added to the content of the accumulator. The result is placed in the accumulator.

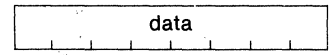
Cycles: 2
States: 7
Addressing: register indirect
Flags: Z,S,P,CY,AC

ADD IMMEDIATE

ADI data



Byte 1



Byte 2

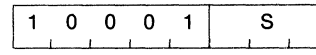
(A) ← (A) + data

The content of the second byte of the instruction is added to the content of the accumulator. The result is placed in the accumulator.

Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

ADD REGISTER WITH CARRY

ADC r



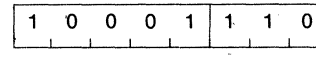
(A) ← (A) + (r) + (CY)

The content of register r and the content of the carry bit are added to the content of the accumulator. The result is placed in the accumulator.

Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

ADD MEMORY WITH CARRY

ADC M



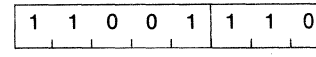
(A) ← (A) + ((H) (L)) + (CY)

The content of the memory location whose address is contained in the H and L registers and the content of the CY flag are added to the accumulator. The result is placed in the accumulator.

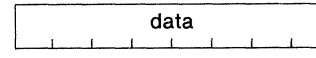
Cycles: 2
States: 7
Addressing: register indirect
Flags: Z,S,P,CY,AC

ADD IMMEDIATE WITH CARRY

ACI data



Byte 1



Byte 2

(A) ← (A) + data + (CY)

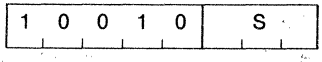
The content of the second byte of the instruction and the content of the CY flag are added to the contents of the accumulator. The result is placed in the accumulator.

Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

Subtract Instructions (SUB, SUI, SBB, SBI) subtract a data byte or register from the contents of the accumulator and place the result in the accumulator. All subtraction operations are performed using two's complement arithmetic and either set the carry flag (CY) to indicate a borrow or clear it to indicate no borrow.

SUBTRACT REGISTER

SUB r



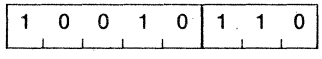
(A) ← (A) – (r)

The content of register r is subtracted from the content of the accumulator. The result is placed in the accumulator.

Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

SUBTRACT MEMORY

SUB M



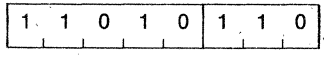
(A) ← (A) – ((H) (L))

The content of the memory location whose address is contained in the H and L registers is subtracted from the content of the accumulator. The result is placed in the accumulator.

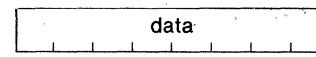
Cycles: 2
States: 7
Addressing: register indirect
Flags: Z,S,P,CY,AC

SUBTRACT IMMEDIATE

SUI data



Byte 1



Byte 2

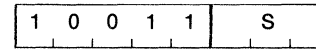
(A) ← (A) – data

The content of the second byte of the instruction is subtracted from the content of the accumulator. The result is placed in the accumulator.

Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

SUBTRACT REGISTER WITH BORROW

SBB r



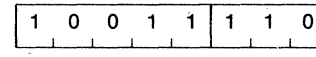
(A) ← (A) – (r) – (CY)

The content of register r and the content of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.

Cycles: 2
States: 7
Addressing: register indirect
Flags: Z,S,P,CY,AC

SUBTRACT MEMORY WITH BORROW

SBB M



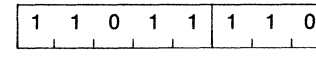
(A) ← (A) – ((H) (L)) – (CY)

The content of the memory location whose address is contained in the H and L registers and the content of the CY flags are both subtracted from the accumulator. The result is placed in the accumulator.

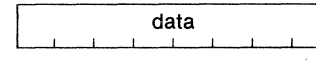
Cycles: 2
States: 7
Addressing: register indirect
Flags: Z,S,P,CY,AC,

SUBTRACT IMMEDIATE WITH BORROW

SBI data



Byte 1



Byte 2

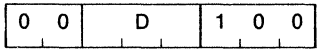
(A) ← (A) – data – (CY)

The contents of the second byte of the instruction and the contents of the CY flag are both subtracted from the accumulator. The result is placed in the accumulator.

Cycles: 2
States: 7
Addressing: register indirect
Flags: Z,S,P,CY,AC

INCREMENT REGISTER

INR r



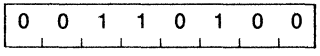
(r) ← (r) + 1

The content of register r is incremented by one. Note: All condition flags except CY are affected.

Cycles: 1
States: 5
Addressing: register
Flags: Z,S,P,AC

INCREMENT MEMORY

INR M



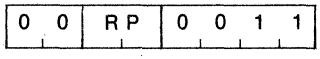
((H) (L)) ← ((H) (L)) + 1

The content of the memory location whose address is contained in the H and L registers is incremented by one. Note: All condition flags except CY are affected.

Cycles: 3
States: 10
Addressing: register indirect
Flags: Z,S,P,AC

INCREMENT REGISTER PAIR

INX rp



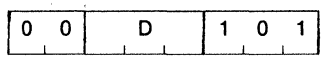
(r_H r_L) ← (r_H r_L) + 1

The content of the register pair rp is incremented by one. Note: No condition flags are affected.

Cycles: 1
States: 5
Addressing: register
Flags: none

DECREMENT REGISTER

DCR r



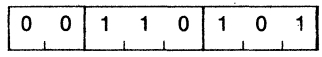
(r) ← (r) − 1

The content of register r is decremented by one. Note: All condition flags except CY are affected.

Cycles: 1
States: 5
Addressing: register
Flags: Z,S,P,AC

DECREMENT MEMORY

DCR M



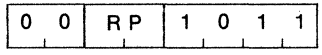
((H) (L)) ← ((H) (L)) − 1

The content of the memory location whose address is contained in the H and L registers is decremented by one. Note: All conditions flags except CY are affected.

Cycles: 3
States: 10
Addressing: register indirect
Flags: Z,S,P,AC

DECREMENT REGISTER PAIR

DCX rp



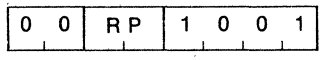
(r_H r_L) ← (r_H r_L) − 1

The content of the register pair rp is decremented by one. Note: No condition flags are affected.

Cycles: 1
States: 5
Addressing: register
Flags: none

ADD REGISTER PAIR TO H AND L

DAD rp



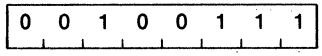
(H) (L) ← (H) (L) + (rh) (rl)

The contents of a specific register pair (rp) will be added to the H and L-Registers (H-Pair). The result is placed in the register pair H and L. Note: Only the CY flag is affected. It is set if there is a carry out of the double precision add; otherwise it is reset.

Cycles: 3
States: 10
Addressing: register
Flags: CY

DECIMAL ADJUST ACCUMULATOR

DAA



The eight-bit number in the accumulator is adjusted to form two four-bit BCD (Binary-Coded-Decimal) digits by the following process:

1. If the value of the least significant 4-bits of the accumulator is greater than 9 or if the AC flag is set, 6 is added to the accumulator.

2. If the value of the most significant 4-bits of the accumulator is now greater than 9, or if the CY flag is set, 6 is added to the most significant 4-bits of the accumulator.

Cycles: 3
States: 10
Flags: Z,S,P,CY,AC

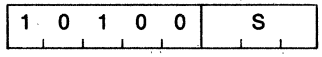
11.1.7 Logical Group

The logical Group of instructions performs logical (Boolean) operations on data in registers or memory and on condition flags. These instructions are: AND, OR, XOR, Compare, Rotate, and Complement. Unless otherwise indicated the Zero (Z), Sign (S), Parity (P), Auxiliary Carry (AC) and Carry (CY) flags will be affected according to the standard rules.

For AND Instructions (ANA, ANI): A register, data byte or memory byte may be AND'ed with the contentsof the accumulator with the results being placed into the accumulator.

AND REGISTER

ANA r



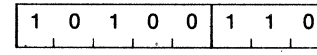
(A) ← (A) ∧ (r)

The content of the register r is logically AND'ed with the content of the accumulator. The result is placed in the accumulator. The CY flag is cleared.

Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

AND MEMORY

ANA M



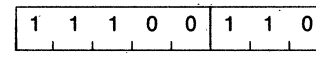
(A) ← (A) ∧ ((H) (L))

The contents of the memory location whose address is contained in the H and L registers is logically AND'ed with the content of the accumulator. The result is placed in the accumulator. The CY flag is cleared.

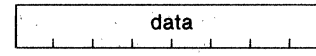
Cycles: 2
States: 7
Addressing: register indirect
Flags: Z,S,P,CY,AC

AND IMMEDIATE

ANI data



Byte 1



Byte 2

(A) ← (A) ∧ data

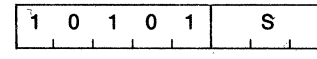
The content of the second byte of the instruction is logically AND'ed with the contents of the accumulator. The result is placed in the accumulator. The CY flag is cleared.

Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

For exclusive OR Instructions (XRA, XRI), a register, data byte or memory is exclusive — OR'd with the contents of the accumulator, with the result being placed in the accumulator.

EXCLUSIVE OR REGISTER

XRA r



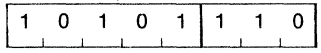
(A) ← (A) ∀ (r)

The content of register r is exclusive — OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

EXCLUSIVE OR MEMORY

XRA M

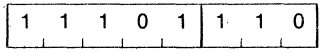


(A) ← (A) ⊻ ((H) (L))
The content of the memory location whose address is contained in the H and L registers is exclusive — OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

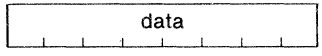
Cycles: 2
States: 7
Addressing: register indirect
Flags: Z,S,P,CY,AC

EXCLUSIVE OR IMMEDIATE

XRI data



Byte 1



Byte 2

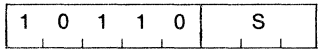
(A) ← (A) ⊻ data
The content of the second byte of the instruction is exclusive — OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

The OR Instructions (ORA, ORI) cause a register, data byte or memory location to be OR'd with the contents of the accumulator; the result being placed in the accumulator.

OR REGISTER

ORA r



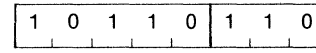
(A) ← (A) V (r)

The content of register r is inclusive — OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

OR MEMORY

ORA M

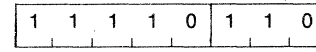


(A) ← (A) V ((H) (L))
The content of the memory location whose address is contained in the H and L registers is OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

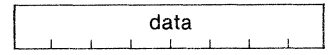
Cycles: 2
States: 7
Addressing: register indirect
Flags: Z,S,P,CY,AC

OR IMMEDIATE

ORI data



Byte 1



Byte 2

(A) ← (A) V data

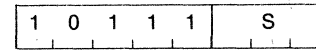
The content of the second byte of the instruction is inclusive — OR'd with the content of the accumulator. The result is placed in the accumulator. The CY and AC flags are cleared.

Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

The Compare instructions (CMP, CPI) allow a register, data byte or memory location to be compared with the accumulator. Results of the operation are reflected by the condition flags, and the contents of the accumulator will remain unchanged.

COMPARE REGISTER

CMP r



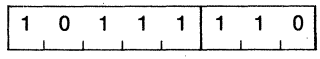
(A) – (r), (A) unchanged

The content of register r is subtracted from the accumulator. The accumulator remains unchanged. The condition flags are set as a result of the subtraction. The Z flag is set to 1 if (A) = (r). The CY flag is set to 1 if (A) < (r).

Cycles: 1
States: 4
Addressing: register
Flags: Z,S,P,CY,AC

COMPARE MEMORY

CMP M



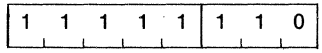
(A) – ((H) (L)), (A) unchanged

The content of the memory location whose address is contained in the H and L registers is subtracted from the accumulator. The accumulator remains unchanged. The condition flags are set as a result of the subtraction. The Z flag is set to 1 if (A) = ((H)(L)). The CY flag is set to 1 if (A) < ((H)(L)).

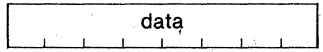
Cycles: 2
States: 7
Addressing: register indirect
Flags: Z,S,P,CY,AC

COMPARE IMMEDIATE

CPI data



Byte 1



Byte 2

(A) – data, (A) unchanged

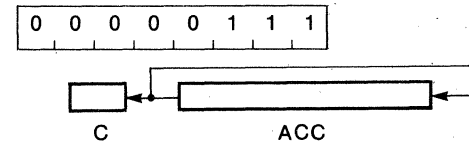
The content of the second byte of the instruction is subtracted from the accumulator. The condition flags are set by the result of the subtraction. The Z flag is set to 1 if (A) = (data). The CY flag is set to 1 if (A) < (data).

Cycles: 2
States: 7
Addressing: immediate
Flags: Z,S,P,CY,AC

Rotate Instructions (RLC, RRC, RAL, RAR) provide a method of recirculating the contents of the accumulator one position to the right or left. During Rotate Instructions, only the Carry flag (CY) is affected.

ROTATE LEFT

RLC

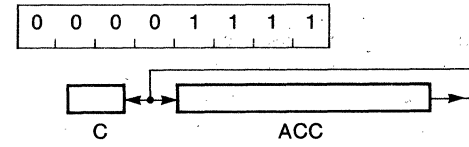


The content of the accumulator is rotated left one position. The low order bit and the CY flag are both set to the value shifted out of the high order bit position. Only the CY flag is affected.

Cycles: 1
States: 4
Flags: CY

ROTATE RIGHT

RRC

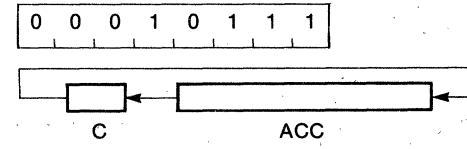


The content of the accumulator is rotated right one position. The high order bit and CY flag are both set to value shifted out of the low order bit position. Only the CY flag is affected.

Cycles: 1
States: 4
Flags: CY

ROTATE LEFT THROUGH CARRY

RAL

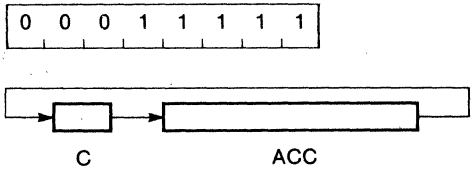


The content of the accumulator is rotated left one position through the CY flag. The low order bit is set equal to the CY flag and the CY flag is set to the value shifted out of the high order bit. Only the CY flag is affected.

Cycles: 1
States: 4
Flags: CY

ROTATE RIGHT THROUGH CARRY

RAR

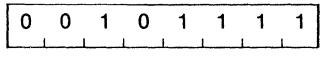


The content of the accumulator is rotated right one position through the CY flag. The high order bit is set equal to the CY flag and the CY flag is set to the value shifted out of the low order bit. Only the CY flag is affected.

Cycles: 1
States: 4
Flags: CY

COMPLEMENT ACCUMULATOR

CMA



$(A) \leftarrow (\overline{A})$

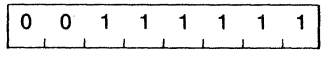
ONE's Complement of the accumulator is performed (zero bits become 1, one bits become 0).

Cycles: 1
States: 4
Flags: none

Complement Carry and Set Carry (CMC, STC) are provided for direct control of the Carry flag. These will allow the Carry flag to be set. No other flags will be affected by the operation.

COMPLEMENT CARRY

CMC



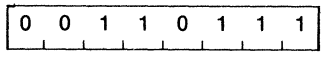
$(CY) \leftarrow (\overline{CY})$

The CY flag is complemented. No other flags are affected.

Cycles: 1
States: 4
Flags: CY

SET CARRY

STC



(CY) ← 1

The CY flag is set to 1. No other flags are affected.

Cycles: 1
States: 4
Flags: CY

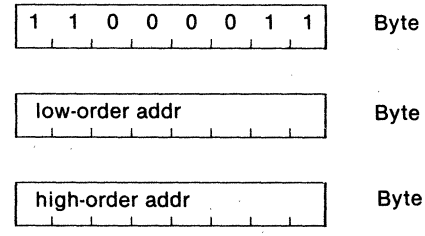
11.1.8 Branch Group

This group of instructions may alter normal sequential program execution. Condition flags are not affected by an instruction in this group. The two types of branch instructions are unconditional and conditional.

Unconditional transfers perform the specified operation on register PC (the program counter). Conditional transfers examine the status of one of the four processor flags to determine if the specified branch is to be executed.

JUMP (Unconditional)

JMP addr



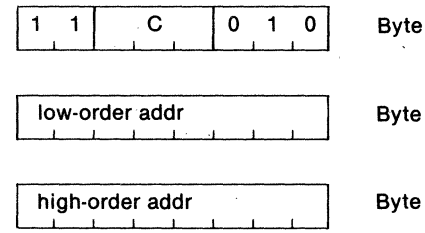
$(PC) \leftarrow addr_H\ addr_L$

Jump (unconditional) provides for loading of the Program Counter with the two bytes which immediately follow the instruction. Therefore, control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction.

Cycles: 3
States: 10
Addressing: immediate
Flags: none

CONDITIONAL JUMP

JZ,JNZ,JC,JNC,JPO,JPE,JP,JM addr



If the specified condition is true, control is tranferred to the instruction whose address is specified in byte 2 and byte 3 of the current instruction; otherwise, control continues sequentially. The conditions that may be specified are as follows:

Note: C denotes the bit combination in the Branch Instructions.

C	Flag	Condition
000	$(\overline{Z=0})$	NZ - Not Zero
001	(Z = 1)	Z - Zero
010	(CY = 0)	NC - No Carry
011	(CY = 1)	C - Carry
100	(P = 0)	PO - Parity Odd
101	(P = 1)	PE - Parity Even
110	(S = 0)	P - Plus
111	(S = 1)	M - Minus

Conditional jumps may occur for any condition flag except Auxiliary Carry (AC).

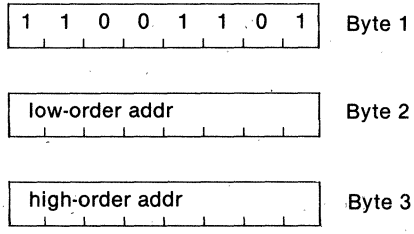
Cycles: 3
States: 10
Addressing: immediate
Flags: none

Call Instructions (CALL, CZ, CNZ, CC, CNC, CPO, CPE, CP, CM), like the Jump Instructions, provide for loading of the Program Counter with the two bytes which immediately follow the instruction. However, prior to loading the Program Counter, the current contents of the counter (which point to the next sequential memory location) are stored in Memory in an area specified by the Stack Pointer (SP), i.e. "pushed" onto the stack. Once the PC is stored on the stack, the PC is loaded with the two bytes immediately following the instruction and program control is transferred to the new location.

Call instructions may be unconditional, in which case the transfer of program control occurs immediately; or conditional, which checks for a specific condition flag before the call is executed.

CALL

Call addr



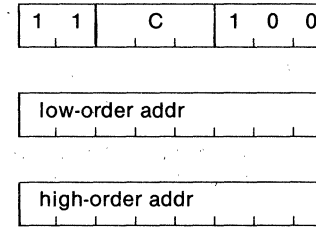
$((SP) - 1) \leftarrow (PC_H)$
$((SP) - 2) \leftarrow (PC_L)$
$(SP) \leftarrow (SP) - 2$
$(PC) \leftarrow addr_H\ addr_L$

The high-order eight bits of the next instruction address are moved to the memory location whose address is one less than the content of register SP. The low-order eight bits of the next instruction address are moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by 2. Control is transferred to the instruction whose address is specified in byte 3 and byte 2 of the current instruction.

Cycles: 5
States: 17
Addressing: immediate/register indirect
Flags: none

CONDITIONAL CALL

CZ,CNZ,CC,CNC,CPO,CPE,CP,CM addr



If (C), $((SP) - 1) \leftarrow (PC_H)$
$(SP) \leftarrow (SP) - 2$
$(PC) \leftarrow addr_H\ addr_L$

If the specified condition is true, the actions specified in the CALL instruction (see above) are performed; otherwise, control continues sequentially.

C denotes the bit combination in Byte 1 of the Instruction.

C	Flag	Condition
000	$(\overline{Z=0})$	NZ- Not zero
001	(Z = 1)	Z- Zero
010	(CY = 0)	NC- No Carry
011	(CY = 1)	C- Carry
100	(P = 0)	PO- Parity Odd
101	(P = 1)	PE- Parity Even
110	(S = 0)	P- Plus
111	(S = 1)	M- Minus

Note: / means depends on condition flags.

Cycles: 3/5
States: 11/17
Addressing: immediate/register indirect
Flags: none

Return Instructions (RET, RZ, RNZ, RC, RNC, RPO, RPE, RP, RM), provide a method of transferring program control back to a location from which an exit had occurred during a Call instruction. It is accomplished by "popping" the top two bytes from the stack into the Program Counter. Return instructions are unconditional or conditional.

RETURN

RET

1	1	0	0	1	0	0	1

$(PC_L) \leftarrow ((SP))$
$(PC_H) \leftarrow ((SP) + 1)$
$(SP) \leftarrow (SP) + 2$

The content of the memory location whose address is specified in register SP is moved to the low-order eight bits of register PC. The content of the memory location whose address is one more than the content of register SP is moved to the high-order eight bits of register PC. The content of register SP is incremented by 2.

Cycles: 3
States: 10
Addressing: register indirect
Flags: none

CONDITIONAL RETURN

RZ,RNZ,RC,RNC,RPO,RPE,RP,RM

1	1	C	0	0	0

If (C), $(PC_L) \leftarrow ((SP))$
$(PC_H) \leftarrow ((SP) + 1)$
$(SP) \leftarrow (SP) + 2$

If the specified condition is true, the actions specified in the RETURN Instruction are performed; otherwise control continues sequentially.

C denotes the bit combination in Byte 1 of the Instruction.

C	Flag	Condition
000	$(\overline{Z} = 0)$	NZ - Not Zero
001	$(Z = 1)$	Z - Zero
010	$(CY = 0)$	NC - No Carry
011	$(CY = 1)$	C - Carry
100	$(P = 0)$	PO - Parity Odd
101	$(P = 1)$	PE - Parity Even
110	$(S = 0)$	P - Plus
111	$(S = 1)$	M - Minus

Cycles: 1/3
States: 5/11
Addressing: register indirect
Flags: none

The Restart instructions (RST) are nearly identical to the Call instructions except:

1. The address to which program control is transferred is one of eight memory locations.

2. All Restart instructions are unconditional. Although these instructions can be supplied by software, they are normally forced into the microprocessor by the hardware during interrupt operations so that program control may be transferred to a selected location.

RESTART

RST n

1	1	N	1	1	1

$((SP) - 1) \leftarrow (PC_H)$
$((SP) - 2) \leftarrow (PC_L)$
$(SP) \leftarrow (SP) - 2$
$(PC) \leftarrow 8^* (N)$

The high-order bits of the next instruction address are moved to the memory location whose address is one less than the content of register SP. The low-order eight bits of the next instruction address are moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by two.

Control is transferred to an eight-byte Restart block starting with the location whose address is eight times the content of N. (See chart).

N	LOCATION
000	0000_{16}
001	0008_{16}
010	0010_{16}
011	0018_{16}
100	0020_{16}
101	0028_{16}
110	0030_{16}
111	0038_{16}

Program counter bit positions 3, 4, and 5 contain value of N. Other bit positions are forced to zero.

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

0	0	0	0	0	0	0	0	0	0	N	0	0	0

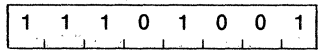
Program Counter

11

Cycles: 3
States: 11
Addressing: register indirect
Flags: none

LOAD PC FROM H AND L REGISTER

PCHL



$(PC_H) \leftarrow (H)$
$(PC_L) \leftarrow (L)$

The content of the H-Register is loaded into upper 8-bits of the PC and the L-Register is loaded into the lower 8-bits of the PC. Program control is transferred to the new address.

Cycles: 1
States: 5
Addressing: register
Flags: none

11.1.9 Stack, I/O, and Machine Control Group

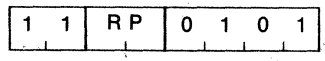
This group of instructions manipulates the stack, handles I/O data transfer and machine controls such as interrupt and internal control flags.

Stack instructions manipulate the stack, transferring data between the register pairs (within the microprocessor) and the stack. Data is transferred to the stack using PUSH instructions while data is removed from the stack by POP instructions.

The PUSH instructions (PUSH B, PUSH D, PUSH H, PUSH PSW) provide a method of storing the contents of various register pairs into memory. The area in which they are saved is the STACK, which is addressed by the Stack Pointer Register.

PUSH

Push rp



$((SP) - 1) \leftarrow (r_H)$
$((SP) - 2) \leftarrow (r_L)$
$(SP) \leftarrow (SP) - 2$

The content of the high-order register of register pair rp is moved to the memory location whose address is one less than the content of register SP. The content of the low-order register of register pair rp is moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by 2.

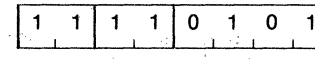
Note: Register pair rp = SP may *not* be specified.

RP
00 B-Pair (B and C-Registers)
01 D-Pair (D and E-Registers)
10 H-Pair (H and L-Registers)

Cycles: 3
States: 11
Addressing: register indirect
Flags: none

PUSH PROCESSOR STATUS WORD

PUSH PSW

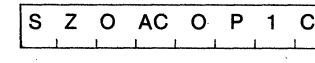


$((SP) - 1) \leftarrow (A)$
$((SP) - 2) \leftarrow (flags)$
$(SP) \leftarrow (SP) - 2$

The content of register A is moved to the memory location whose address is one less than register SP. The contents of the condition flags are assembled into a byte and the byte is moved to the memory location whose address is two less than the content of register SP. The content of register SP is decremented by two.

flags

MSB LSB

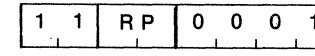


Cycles: 3
States: 11
Addressing: register indirect
Flags: none

The POP instructions (POP B, POP D, POP H) provide a method of loading register pairs with data contained on the stack.

POP REGISTER PAIR

pop rp



$(r_L) \leftarrow ((SP))$
$(r_H) \leftarrow ((SP) + 1)$
$(SP) \leftarrow ((SP) + 2)$

The content of the memory location, whose address is specified by the content of register SP, is moved to the low-order register of register pair rp. The content of the memory location, whose address is one more than the content of register SP, is moved to the high-order register of register pair rp. The content of register SP is incremented by 2.

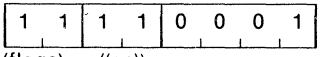
Note: Register pair rp = SP may *not* be specified.

RP
00 B-Pair (B and C-Registers)
01 D-Pair (D and E-Registers)
10 H-Pair (H and L-Registers)

Cycles: 3
States: 10
Addressing: register indirect
Flags: none

POP PROCESSOR STATUS WORD

POP PSW



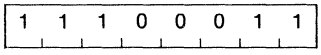
(flags) ← ((sp))
(A) ← ((SP) + 1)
(SP) ← (SP) + 2

The content of the memory location whose address is specified by the content of register SP is used to restore the condition flags. The content of the memory location whose address is one more than the content of register SP is moved to register A. The content of register SP is incremented by 2.

Cycles: 3
States: 10
Addressing: register indirect
Flags: Z,S,P,CY,AC

EXCHANGE TOP OF STACK WITH H & L

XTHL



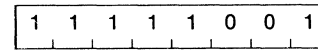
(L) ↔ (SP)
(H) ↔ (SP) + 1

The content of the L-Register is exchanged with the content of the memory location whose address is specified by the content of register SP. The content of the H-Register is exchanged with the content of the memory location whose address is one more than the content of register SP.

Cycles: 5
States: 18
Addressing: register indirect
Flags: none

MOVE H AND L TO SP

SPHL



(SP) ← (H) (L)

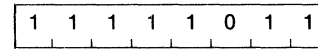
The contents of registers H and L (16-bits) are moved to register SP.

Cycles: 1
States: 5
Addressing: register
Flags: none

Interrupt Control instructions (EI, DI) are provided for the control of interrupts. An Enable Interrupt must be executed before the microprocessor will recognize any interrupt requests from the devices in the system. Once an interrupt is recognized by the microprocessor it will ignore all further requests until another EI is executed. If interrupts are enabled and the programmer wishes to ignore them a DI (disable interrupts) instructions may be used.

ENABLE INTERRUPTS

EI

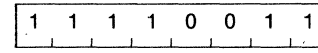


The interrupt system is enabled following the execution of the next instruction.

Cycles: 1
States: 4
Flags: none

DISABLE INTERRUPTS

DI



The interrupt system is disabled immediately following the execution of the DI instruction.

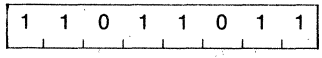
Cycles: 1
States: 4
Flags: none

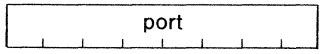
I/O Data Transfer Instructions (IN, OUT) provide a method of transferring a byte of data to or from an I/O port external to the microprocessor,

into or out of the accumulator. The port is selected by the second byte of the instruction.

INPUT

IN port





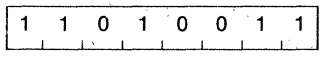
(A) ← (port data)

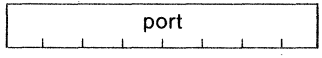
The data placed on the eight bit bidirectional data bus by the specified port is moved to the accumulator.

Cycles: 3
States: 10
Addressing: direct
Flags: none

OUTPUT

OUT port





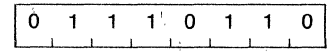
(port) ← (A)

The content of register A is placed on the eight bit bidirectional data bus for transmission to the specified port.

Cycles: 3
States: 10
Addressing: direct
Flags: none

HALT

HLT

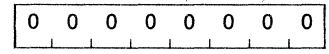


The processor is stopped. The registers and flags are unaffected.

Cycles: 1
States: 7
Flags: none

NO OPERATION

NOP



No operation is performed. The registers and flags are unaffected.

Cycles: 1 PC incremented by 1
States: 4
Flags: none

8080 INSTRUCTION SUMMARY

Table 11-2 is a complete summary of the 8080 Instruction Set.

Table 11-2 8080 Instruction Summary

Mnemonic	Description	Operation	Op Code D_7 D_6 D_5 D_4	Op Code D_3 D_2 D_1 D_0	No. of Bytes	No. of Machine (M) Cycles	No. of μcycles (T)	Condition Flags S	Z	AC	P	CY
DATA TRANSFER GROUP												
LDA	Load Accumulator Direct	(A) ← ((byte 3)(byte 2))	0 0 1 1	1 0 1 0	3	4	13					
LDAX B	Load Accumulator Indirect	(A) ← ((B))	0 0 0 0	1 0 1 0	1	2	7					
LDAX D	Load Accumulator Indirect	(A) ← ((D))	0 0 0 1	1 0 1 0	1	2	7					
LHLD	Load H and L Direct	(L) ← ((byte 3)(byte 2)) (H) ← ((byte 3)(byte 2) + 1)	0 0 1 0	1 0 1 0	3	5	16					
LXI B	Load Immediate, Registers B and C	(B) ← (byte 3) (C) ← (byte 2)	0 0 0 0	0 0 0 1	3	3	10					
LXI D	Load Immediate, Registers D and E	(D) ← (byte 3) (E) ← (byte 2)	0 0 0 1	0 0 0 1	3	3	10					
LXI H	Load Immediate, Registers H and L	(H) ← (byte 3) (L) ← (byte 2)	0 0 1 0	0 0 0 1	3	3	10					
LXI SP	Load Immediate, Stack Pointer	(SPH) ← (byte 3) (SPL) ← (byte 2)	0 0 1 1	0 0 0 1	3	3	10					
MOV M, r	Move to Memory	((H)(L)) ← (r)	0 1 1 1	0 *S S S*	1	2	7					
MOV r, M	Move from Memory	(r) ← ((H)(L))	0 1 *D D*	*D* 1 1 0	1	2	7					
MOV r1, r2	Move Registers	(r1) ← (r2)	0 1 *D D*	*D S S S*	1	1	5					
MVI M	Move to Memory Immediate	((H)(L)) ← (byte 2)	0 0 1 1	0 1 1 0	2	3	10					
MVI r	Move Immediate	(r) ← (byte 2)	0 0 *D D*	*D* 1 1 0	2	2	7					
SHLD	Store H and L Direct	((byte 3)(byte 2)) ← (L) ((byte 3)(byte 2) + 1) ← (H)	0 0 1 0	0 0 1 0	3	5	16					
STA	Store Accumulator Direct	((byte 3)(byte 2)) ← (A)	0 0 1 1	0 0 1 0	3	4	13					
STAX B	Store Accumulator Indirect	((B)) ← (A)	0 0 0 0	0 0 1 0	1	2	7					
STAX D	Store Accumulator Indirect	((D)) ← (A)	0 0 0 1	0 0 1 0	1	2	7					
XCHG	Exchange H and L with D and E	(H) ↔ (D) (L) ↔ (E)	1 1 1 0	1 0 1 1	1	1	4					
ARITHMETIC GROUP												
ACI	Add Immediate with Carry	(A) ← (A) + (byte 2) + (CY)	1 1 0 0	1 1 1 0	2	2	7	‡	‡	‡	‡	‡
ADC M	Add Memory with Carry	(A) ← (A) + ((H)(L)) + (CY)	1 0 0 0	1 1 1 0	1	2	7	‡	‡	‡	‡	‡
ADC r	Add Register with Carry	(A) ← (A) + (r) + (CY)	1 0 0 0	1 *S S S*	1	1	4	‡	‡	‡	‡	‡
ADD M	Add Memory	(A) ← (A) + ((H)(L))	1 0 0 0	0 1 1 0	1	2	7	‡	‡	‡	‡	‡
ADD r	Add Register	(A) ← (A) + (r)	1 0 0 0	0 *S S S*	1	1	4	‡	‡	‡	‡	‡
ADI	Add Immediate	(A) ← (A) + (byte 2)	1 1 0 0	0 1 1 0	2	2	7	‡	‡	‡	‡	‡
DAA	Decimal Adjust Accumulator	8-bit number in Accumulator is converted to two 4-bit BCD digits	0 0 1 0	0 1 1 1	1	1	4	‡	‡	‡	‡	‡
DAD B	Add B and C to H and L	(H)(L) ← (H)(L) + (B)(C)	0 0 0 0	1 0 0 1	1	3	10	·	·	·	·	‡
DAD D	Add D and E to H and L	(H)(L) ← (H)(L) + (D)(E)	0 0 0 1	1 0 0 1	1	3	10	·	·	·	·	‡
DAD H	Add H and L to H and L	(H)(L) ← (H)(L) + (H)(L)	0 0 1 0	1 0 0 1	1	3	10	·	·	·	·	‡
DAD SP	Add Stack Pointer to H and L	(H)(L) ← (H)(L) + (SP)	0 0 1 1	1 0 0 1	1	3	10	·	·	·	·	‡
DCR M	Decrement Memory	((H)(L)) ← ((H)(L)) − 1	0 0 1 1	0 1 0 1	1	3	10	‡	‡	‡	‡	·
DCR r	Decrement Register	(r) ← (r) − 1	0 0 *D D*	*D* 1 0 1	1	1	5	‡	‡	‡	‡	·
DCX B	Decrement Registers B and C	(B)(C) ← (B)(C) − 1	0 0 0 0	1 0 1 1	1	1	5	·	·	·	·	·
DCX D	Decrement Registers D and E	(D)(E) ← (D)(E) − 1	0 0 0 1	1 0 1 1	1	1	5	·	·	·	·	·
DCX H	Decrement Registers H and L	(H)(L) ← (H)(L) − 1	0 0 1 0	1 0 1 1	1	1	5	·	·	·	·	·
DCX SP	Decrement Stack Pointer	(SP) ← (SP) − 1	0 0 1 1	1 0 1 1	1	1	5	·	·	·	·	·
INR M	Increment Memory	((H)(L)) ← ((H)(L)) + 1	0 0 1 1	0 1 0 0	1	3	10	‡	‡	‡	‡	·
INR r	Increment Register	(r) ← (r) + 1	0 0 *D D*	*D* 1 0 0	1	1	5	‡	‡	‡	‡	·
INX B	Increment Registers B and C	(B)(C) ← (B)(C) + 1	0 0 0 0	0 0 1 1	1	1	5	·	·	·	·	·
INX D	Increment Registers D and E	(D)(E) ← (D)(E) + 1	0 0 0 1	0 0 1 1	1	1	5	·	·	·	·	·
INX H	Increment Registers H and L	(H)(L) ← (H)(L) + 1	0 0 1 0	0 0 1 1	1	1	5	·	·	·	·	·
INX SP	Increment Stack Pointer	(SP) ← (SP) + 1	0 0 1 1	0 0 1 1	1	1	5	·	·	·	·	·
SBB M	Subtract Memory with Borrow	(A) ← (A) − ((H)(L)) − (CY)	1 0 0 1	1 1 1 0	1	2	7	‡	‡	‡	‡	‡
SBB r	Subtract Register with Borrow	(A) ← (A) − (r) − (CY)	1 0 0 1	1 *S S S*	1	1	4	‡	‡	‡	‡	‡
SBI	Subtract Immediate with Borrow	(A) ← (A) − (byte 2) − (CY)	1 1 0 1	1 1 1 0	2	2	7	‡	‡	‡	‡	‡
SUB M	Subtract Memory	(A) ← (A) − ((H)(L))	1 0 0 1	0 1 1 0	1	2	7	‡	‡	‡	‡	‡
SUB r	Subtract Register	(A) ← (A) − (r)	1 0 0 1	0 *S S S*	1	1	4	‡	‡	‡	‡	‡
SUI	Subtract Immediate	(A) ← (A) − (byte 2)	1 1 0 1	0 1 1 0	2	2	7	‡	‡	‡	‡	‡
LOGICAL GROUP												
ANA M	AND Memory	(A) ← (A) ∧ ((H)(L))	1 0 1 0	0 1 1 0	1	2	7	‡	‡	·	‡	0
ANA r	AND Register	(A) ← (A) ∧ (r)	1 0 1 0	0 *S S S*	1	1	4	‡	‡	·	‡	0
ANI	AND Immediate	(A) ← (A) ∧ (byte 2)	1 1 1 0	0 1 1 0	2	2	7	‡	‡	·	‡	0
CMA	Complement Accumulator	(A) ← $(\overline{A})$	0 0 1 0	1 1 1 1	1	1	4	·	·	·	·	·
CMC	Complement Carry	(CY) ← $(\overline{CY})$	0 0 1 1	1 1 1 1	1	1	4	·	·	·	·	‡
CMP M	Compare Memory	(A) — ((H)(L))	1 0 1 1	1 1 1 0	1	2	7	‡	‡[a]	‡	‡	‡[a]
CMP r	Compare Register	(A) — (r)	1 0 1 1	1 *S S S*	1	1	4	‡	‡[b]	‡	‡	‡[b]
CPI	Compare Immediate	(A) — (byte 2)	1 1 1 1	1 1 1 0	2	2	7	‡	‡[c]	‡	‡	‡[c]
ORA M	OR Memory	(A) ← (A) ∨ ((H)(L))	1 0 1 1	0 1 1 0	1	2	7	‡	‡	0	‡	0
ORA r	OR Register	(A) ← (A) ∨ (r)	1 0 1 1	0 *S S S*	1	1	4	‡	‡	0	‡	0
ORI	OR Immediate	(A) ← (A) ∨ (byte 2)	1 1 1 1	0 1 1 0	2	2	7	‡	‡	0	‡	0
RAL	Rotate Left through Carry	$(A_{n+1}) \leftarrow (A_n)$, (CY) ← (A_7) (A_0) ← (CY)	0 0 0 1	0 1 1 1	1	1	4	·	·	·	·	‡
RAR	Rotate Right through Carry	$(A_n) \leftarrow (A_{n+1})$, (CY) ← (A_0) (A_7) ← (CY)	0 0 0 0	1 1 1 1	1	1	4	·	·	·	·	‡
RLC	Rotate Left	$(A_{n+1}) \leftarrow (A_n)$; $(A_0) \leftarrow (A_7)$ (CY) ← (A_7)	0 0 0 0	0 1 1 1	1	1	4	·	·	·	·	‡
RRC	Rotate Right	$(A_n) \leftarrow (A_{n-1})$, $(A_7) \leftarrow (A_0)$ (CY) ← (A_0)	0 0 0 0	1 1 1 1	1	1	4	·	·	·	·	‡
STC	Set Carry	(CY) ← 1	0 0 1 1	0 1 1 1	1	1	4	·	·	·	·	1
XRA M	Exclusive OR Memory	(A) ← (A) ∀ ((H)(L))	1 0 1 0	1 1 1 0	1	2	7	‡	‡	0	‡	0
XRA r	Exclusive OR Register	(A) ← (A) ∀ (r)	1 0 1 0	1 *S S S*	1	1	4	‡	‡	0	‡	0
XRI	Exclusive OR Immediate	(A) ← (A) ∀ (byte 2)	1 1 1 0	1 1 1 0	2	2	7	‡	‡	0	‡	0

(Flags Not Affected)

Notes: a. Z = 1 if (A) = (H)(L); CY = 1 if (A) < (H)(L)
b. Z = 1 if (A) = (r); CY = 1 if (A) < (r)
c. Z = 1 if (A) = (byte 2); CY = 1 if (A) < (byte 2)

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Table 11-2 8080 Instruction Summary (Continued)

Mnemonic	Description	Operation	Op Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	No. of Bytes	No. of Machine (M) Cycles	No. of μcycles (T)	Condition Flags S	Z	AC	P	CY
BRANCH GROUP																		
CALL	Call Unconditional	((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3)(byte 2)	1	1	0	0	1	1	0	1	3	5	17					
CC	Call on Carry	If CY = 1, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3)(byte 2)	1	1	0	1	1	1	0	0	3	3/5	11/17					
CM	Call on Minus	If S = 1, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3)(byte 2)	1	1	1	1	1	1	0	0	3	3/5	11/17					
CNC	Call on No Carry	If CY = 0, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3)(byte 2)	1	1	0	1	0	1	0	0	3	3/5	11/17					
CNZ	Call on Not Zero	If Z = 0, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3)(byte 2)	1	1	0	0	0	1	0	0	3	3/5	11/17	(Flags Not Affected)				
CP	Call on Positive	If S = 0, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3)(byte 2)	1	1	1	1	0	1	0	0	3	3/5	11/17					
CPE	Call on Parity Even	If P = 1, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3)(byte 2)	1	1	1	0	1	1	0	0	3	3/5	11/17					
CPO	Call on Parity Odd	If P = 0, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3)(byte 2)	1	1	1	0	0	1	0	0	3	3/5	11/17					
CZ	Call on Zero	If Z = 1, ((SP) - 1) ← (PCH) ((SP) - 2) ← (PCL) (SP) ← (SP) - 2 (PC) ← (byte 3)(byte 2)	1	1	0	0	1	1	0	0	3	3/5	11/17					
JC	Jump on Carry	If CY = 1, (PC) ← (byte 3)(byte 2)	1	1	0	1	1	0	1	0	3	3	10					
JM	Jump on Minus	If S = 1, (PC) ← (byte 3)(byte 2)	1	1	1	1	1	0	1	0	3	3	10					
JMP	Jump Unconditional	(PC) ← (byte 3)(byte 2)	1	1	0	0	0	0	1	1	3	3	10					
JNC	Jump on No Carry	If CY = 0, (PC) ← (byte 3)(byte 2)	1	1	0	1	0	0	1	0	3	3	10					
JNZ	Jump on Not Zero	If Z = 0, (PC) ← (byte 3)(byte 2)	1	1	0	0	0	0	1	0	3	3	10					
JP	Jump on Positive	If S = 0, (PC) ← (byte 3)(byte 2)	1	1	1	1	0	0	1	0	3	3	10					
JPE	Jump on Parity Even	If P = 1, (PC) ← (byte 3)(byte 2)	1	1	1	0	1	0	1	0	3	3	10					
JPO	Jump on Parity Odd	If P = 0, (PC) ← (byte 3)(byte 2)	1	1	1	0	0	0	1	0	3	3	10					
JZ	Jump on Zero	If Z = 1, (PC) ← (byte 3)(byte 2)	1	1	0	0	1	0	1	0	3	3	10					
PCHL	H and L to Program Counter	(PCH) ← (H) (PCL) ← (L)	1	1	1	0	1	0	0	1	1	1	5					
RC	Return on Carry	If CY = 1, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	1	1	0	0	0	1	1/3	5/11					
RET	Return	(PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	0	1	0	0	1	1	3	10					
RM	Return on Minus	If S = 1, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	1	1	0	0	0	1	1/3	5/11					
RNC	Return on No Carry	If CY = 0, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	1	0	0	0	0	1	1/3	5/11					
RNZ	Return on Not Zero	If Z = 0, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	0	0	0	0	0	1	1/3	5/11					
RP	Return on Positive	If S = 0, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	1	0	0	0	0	1	1/3	5/11					
RPE	Return on Parity Even	If P = 1, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	0	1	0	0	0	1	1/3	5/11					
RPO	Return on Parity Odd	If P = 0, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	0	0	0	0	0	1	1/3	5/11					

Appendices

Appendix A:
MICROBUS™*
Electrical Specifications

A.1 GENERAL DESCRIPTION

This section defines the electrical specifications for interface devices to be used in environments where:

a) Physical distance between devices is very short,
b) Electrical noise is low.

The electrical specifications for the driver and receiver circuits do not imply a particular technology.

Unless otherwise noted, all specifications apply for T_A = 0°C to 70°C and power supplies within ±5% of specified values.

A.2 LOGICAL AND ELECTRICAL STATE RELATIONSHIPS

The relationship between logical states and the electrical state levels present on signal lines is defined as follows:

LOGICAL STATE	FUNCTIONAL STATE	ELECTRICAL SIGNAL LEVEL
0	OFF	Corresponds to ≤ +0.8V called the low state
1	ON	Corresponds to ≥ +2.0V called the high state

This definition applies to signals whose mnemonic names do not have a line over them. Complemented signals, indicated by a line over the mnemonic, e.g, $\overline{RD}$, are defined as follows:

LOGICAL STATE	FUNCTIONAL STATE	ELECTRICAL SIGNAL LEVEL
0	OFF	Corresponds to ≥ +2.0V called the high state
1	ON	Corresponds to ≤ +0.8V called the low state

Current flow into a node is indicated with positive sign and current flow out of a node with a negative sign.

A.3 DRIVER REQUIREMENTS

A.3.1 Driver Types

Three types of drivers are defined. The first is the standard output which is either in the high or low state or is in transition. It has active drive capability to accept current in the low state and to provide current in the high state.

The second type of driver is the open collector or open drain. This driver will not provide or accept current in the high state.

The third type of driver is the TRI-STATE driver which can, in addition to the high, low, and transition states, be in the high impedance state.

A.3.2 Driver Specifications

The specifications for drivers shall be as follows:

Low State (V_{OL}): Output voltage $\leq +0.4V$ at $+1.6mA$ sink current
High State (V_{OH}): Output voltage (Standard and TRI-STATE) $\geq +2.4V$ at $-100\mu A$.

The above current specifications are regarded as the minimum acceptable values. New designs should provide for higher current specifications. The device designer who wishes to provide broader compatibility with various technologies will provide a high state output voltage $\geq +3.6V$. A lower current specification is acceptable at 3.6V when both 2.4V and 3.6V are specified.

The internal capacitive load of a driver shall not exceed 15pf at 25°C whether in the active or high impedance state.

The rise and fall times of driver outputs should be minimized; in no case should they exceed 100ns at the rated capacitive load.

A.4 RECEIVER REQUIREMENTS

A.4.1 Receiver Specifications, Standard

The specifications for receivers with nominal noise immunity shall be as follows:

Low State: Input Voltage - $+0.8V$
High State: Input Voltage - $+2.0V$

The device designer should minimize receiver current requirements recognizing that the MICROBUS minimum drive current is only 1.6mA in the low state and $-100\mu A$ in the high state.

The internal capacitive load of a receiver shall not exceed 10pf at 25°C.

A.4.2 Receiver Specifications, Special

To provide added noise immunity, the use of Schmitt-type receiver circuits is recommended. The specification for these receivers is as follows:

Hysteresis: $V_{tpos} - V_{tneg} \geq +0.4V$
Low State: Negative threshold voltage V_{tneg} $+0.6V$ (recommended $+0.8V$)
High State: Positive threshold voltage V_{tpos} $+2.0V$

The device designer should minimize receiver current requirements recognizing that the MICROBUS minimum drive current is only 1.6mA in the low state and $-100\mu A$ in the high state.

The internal capacitive load of a receiver shall not exceed 10 pf at 25°C.

A.5 BIDIRECTIONAL SIGNALS

Some interface signals such as the data bus (D_7-D_0), are combined TRI-STATE driver/receivers. For each function these devices must meet the same specifications as separate drivers and receivers. The internal capacitive load of a bi-directional signal shall not exceed 20 pf at 25°C.

A.6 READ CYCLE TIMING SPECIFICATION

Figure A-1 depicts the Read Cycle Waveforms with the pertinent timing parameters shown. Table A-1 specifies these parameters for Class 1 microprocessor systems. These values are for systems where the interface device is connected directly to the MICROBUS.

It is desirable that an interface device function in a buffered address bus and data bus environment in addition to MICROBUS. Adding bus drivers to the system address bus will reduce t_{AR} up to 30 nsec. If bus drivers are used on the D_7-D_0 lines between the device and the system data bus, the apparent t_{RD} to the system will be up to 30 nsec longer.

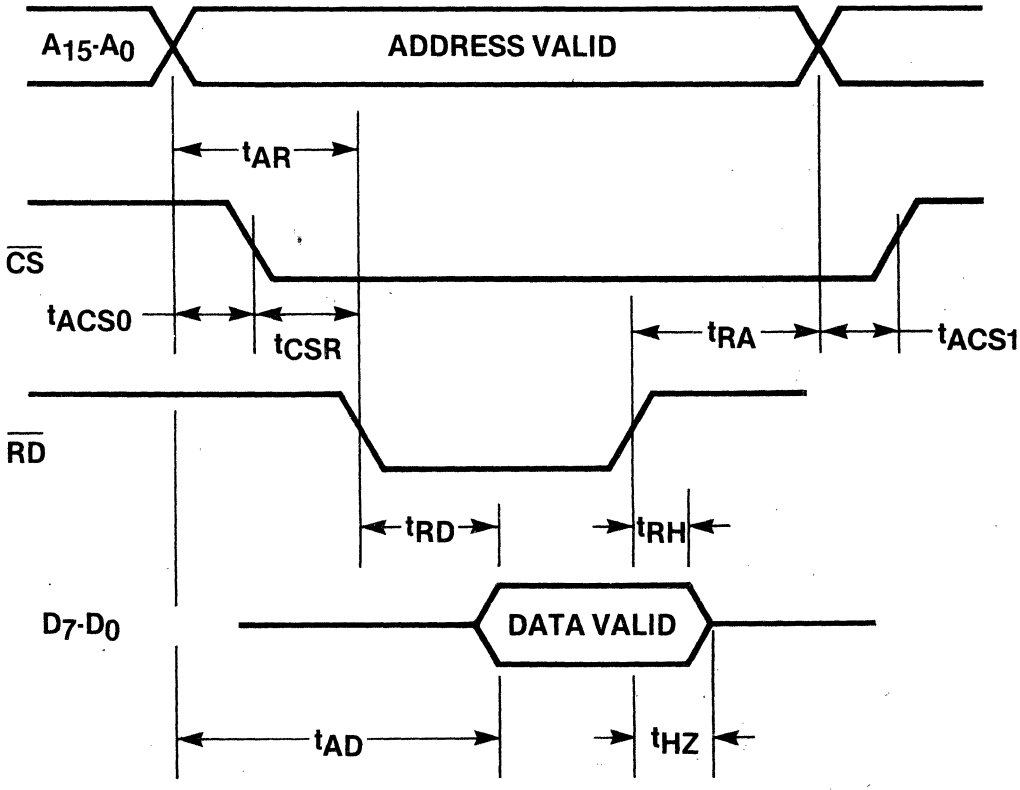


Figure A-1. Read Cycle Waveforms

A

Table A-1. Class 1 Read Cycle
Timing Specifications

Symbol	Parameter	Min	Typ	Max	Units	Comment
t_{ACS0}	Address. Bus Valid to Chip Select ON ($\overline{CS} = 0$)		40	(1)	ns	
t_{CSR}	Chip Select ON to Read Strobe.	(2)	70		ns	
t_{AR}	Address Bus Valid to Read Strobe.	110			ns	
t_{RD}	Read Cycle Access. Time from Read Strobe to Data Bus Valid.			375	ns	CL = 100pf
t_{RH}	Data hold time from trailing edge of Read Strobe.	0		250	ns	
t_{RA}	Address Bus hold time from trailing edge of Read Strobe.	50	500		ns	
t_{ACS1}	Address change to Chip Select OFF.		40		ns	
t_{AD}	Address bus valid to data valid.	560			ns	CL = 100pf
t_{HZ}	Time from trailing edge of Read Strobe until interface device bus drivers are in TRI-STATE mode.	0		250	ns	

NOTES:

1. The maximum value of this parameter is dependent upon implementation of the chip select circuit. This implementation is constrained by the relationship $t_{ACS0} + t_{CSR} = t_{AR}$. See appendix B.

2. $t_{CSR} = t_{AR} - t_{ACS0}$.

A.7 WRITE CYCLE TIMING SPECIFICATION

Figure A-2 depicts the Write Cycle Waveforms along with the pertinent timing parameters. Table A-2 specifies the limits of these parameters for Class 1 microprocessor systems.

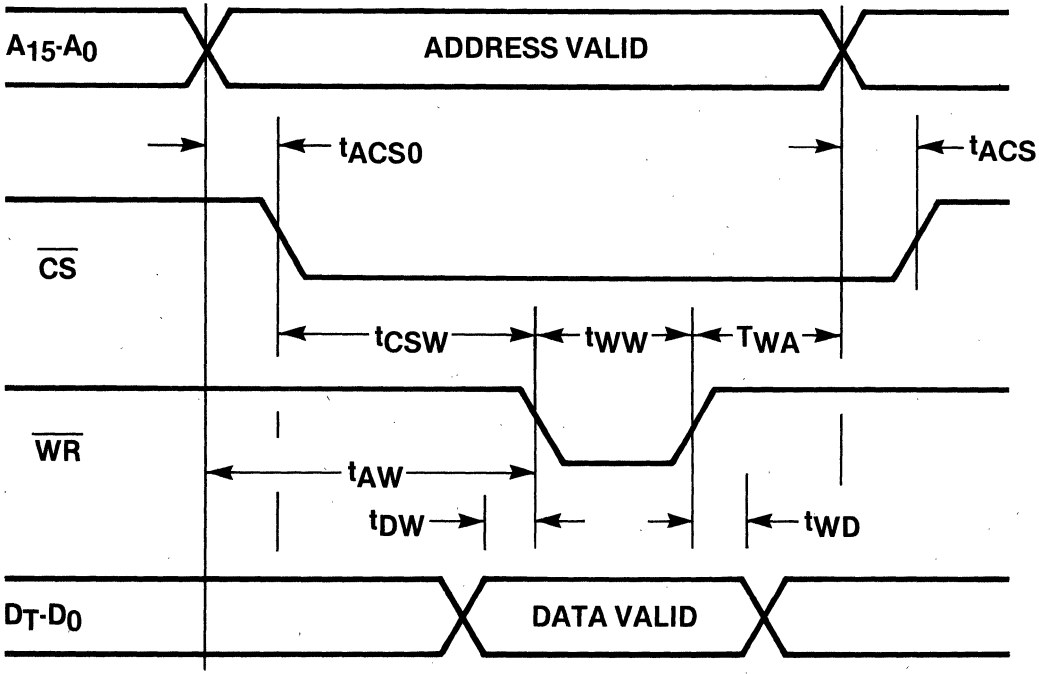


Figure A-2. Write Cycle Waveforms

A

Table A-2. Class 1 Write Cycle
Timing Specifications

Symbol	Parameter	Min	Typ	Max	Units	Comment
t_{ACS0}	Address Bus valid to Chip Select ON ($\overline{CS} = 0$)		40	(1)	ns	
t_{CSW}	Chip Select ON to Write Strobe	(2)	450		ns	
t_{AW}	Address Bus valid to Write Strobe	485			ns	
t_{WW}	Write Strobe Width.	430			ns	
t_{DW}	Data Bus valid before Write Strobe.	115			ns	
t_{WD}	Data Bus hold time following Write Strobe.	100			ns	
t_{WA}	Address Bus hold time following Write Strobe.	50			ns	
t_{ACS1}	Address change to Chip Select OFF ($\overline{CS} = 1$)		40	(1)	ns	

NOTES:

1. The maximum value of this parameter is dependent upon implementation of the chip select circuit. This implementation is constrained by the relationship $t_{ACS0} + t_{CSW} = t_{AW}$. See appendix B.
2. $t_{CSW} = t_{AW} - t_{ACS0}$

A.8 MICROBUS AND DEVICES

See figure 1-2 for devices that can be used on the MICROBUS.

Appendix B:
Series 8000 Microprocessor Family Design Example

A design example of a basic computer system is shown in figure B-1. The MICROBUS lines are shown by groups for purpose of illustration. A terminal is shown which uses the INS8298E LLL BASIC Interpreter, stored in a MAXI-ROM.

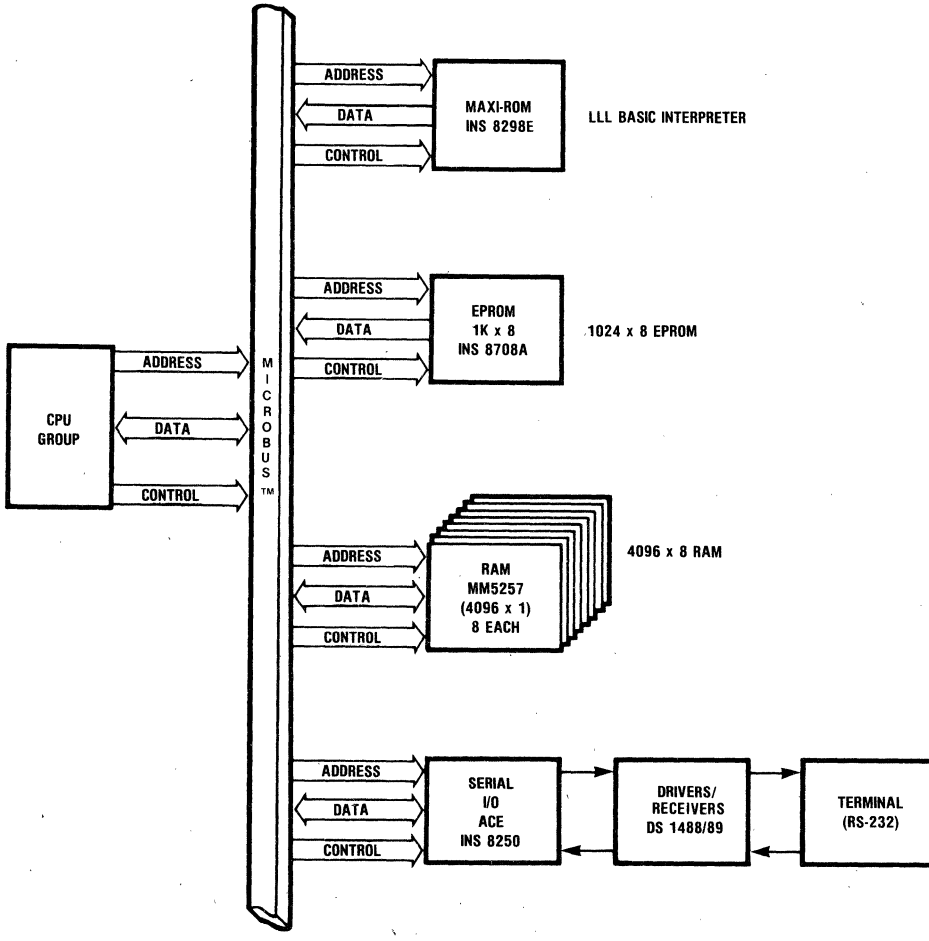


Figure B-1. Design Example (Basic Computer System)

Appendix C: **Additional Information Sources**

Categories of sources are:

- Publications
- National's Microprocessor Users Group (see section 10.8)
- Training Centers (see section 10.7)
- Technical Support Program (see section 10.9)

PUBLICATIONS

Publications are available covering the various devices manufactured by National Semiconductor. The currently available literature is grouped in the following categories:

- Literature Index
- Handbooks
- Manuals
- Linear Applications, Vol I and II
- Databooks
- Guides
- Product Selection Guides
- Briefs
- Individual Application Notes
- Individual Data Sheets

Current handbooks are:

- Audio Handbook
- Linear Applications Handbook Volume I and II
- SC/MP Microprocessor Applications Handbook
- Voltage Regulator Handbook
- Memory Applications Handbook
- Series 8000 Microprocessor Family Handbook

Current databooks are:

- Linear Databook
- TTL Databook
- Interface Databook
- Memory Databook
- Special Function Databook
- MOS/LSI Databook
- CMOS Databook
- FET Databook
- IDM2900 Family Microprocessor Databook
- Discrete Databook
- Power Transistor Databook

Current Product Selection Guides

- Analog Switches Cross Reference Guide
- Analog Switches Selection Guide
- Audio Amplifier Comparison Guide
- Bipolar RAM Cross Reference Guide
- Bipolar PROM Cross Reference Guide
- Bipolar PROM/ROM Selection Guide
- Calculator Kits Guide
- CMOS Status/Cross Reference Guide
- CMOS Watch Circuits Guide
- DIP Resistor Array Cross Reference Guide
- Display Driver Selection Guide
- FET Op Amp Cross Reference Guide
- Fixed Voltage Regulator Guide
- Hybrid Packaging Capability Guide
- Industrial and Commercial Hybrid Op Amp Selection Guide
- Industrial Op Amp Selection Guide
- Interface Status Guide
- JFET Selection Guide
- JFET Cross Reference Guide
- LED Display Selection Guide
- LED Lamp Cross Reference Guide
- LED Lamp Selection Guide
- Linear Cross Reference Guide
- Linear Product Status Guide
- Military Op Amp Selection Guide
- Military Hybrid Op Amp Selection Guide
- MOS Product Status Guide
- RAM Cross Reference Guide
- RAM Selection Guide
- ROM Status Guide
- Special Purpose Drivers Guide
- Special Purpose Linear Circuits Guide
- TO-92 Transistor Guide
- Transducer Selection Guide
- TTL Status Guide
- TTL Functional Product Guide
- Variable Voltage Regulator Guide
- Voltage Comparator Guide
- 54C/74C Users Guide

Current briefs are:

- Linear Briefs
- Digital Briefs
- MOS Briefs
- Microprocessor Briefs
- FET Briefs
- Opto Briefs
- Transducer Briefs

Some Current Application Notes

Number

AN-114 Microprocessors — An Introduction
AN-128 Microprocessor Mates with MOS/LSI Keyboard Encoder
AN-142 Using a Microprocessor Beyond Apparent Speed
AN-159 Data Acquisition System Interface to Computers
AN-163 SC/MP Mates with Cassette Recorder
AN-164 A Data Concentrator Using PACE
AN-189 A PROM Programmer for the SC/MP LCDS
AN-197 Multi-processing with SC/MP
AN-198 Simplify CRT Terminal Design with the DP8350
AN-199 A Low Component Count Video Data Terminal Using the DP8350 CRT Controller and the INS8080 CPU
AN-201 Motor RPM Control Made Easy

See appendix D for available data sheets of devices covered in this handbook.

For list of other available literature, refer to your local National Semiconductor Sales Representative.

Appendix D:
Data Sheets

The Series 8000 Microprocessor Family Data Sheets available at time of publication are listed below and included in this appendix in the order shown (for memory data sheets refer to National's Memory Databook):

D.1 CPU GROUP

INS8080A	8-Bit Microprocessor
INS8224	Clock Generator and Driver
INS8228/8238	System Controller and Bus Driver

D.2 DIGITAL I/O COMPONENTS

INS8202	TRI-STATE 8-Bit Bus Driver
INS8203	TRI-STATE 8-Bit Bus Driver (Inverting)
INS8208	8-Bit Bidirectional Bus Driver
INS8212	8-Bit I/O Port
INS8216	4-Bit Bidirectional Bus Driver
INS8226	4-Bit Bidirectional Bus Driver (Inverting)
INS8255	Programmable Peripheral Interface

D.3 PERIPHERAL CONTROL COMPONENTS

DP8350	Series Programmable CRT Controller
INS1771-1	Floppy Disk Formatter/ Controller
INS8253	Programmable Timer
INS8254	Programmable 16-Bit Addressable Peripheral Interface
INS8257	Programmable DMA Controller
INS8259	Programmable Interrupt Controller
INS8298E	LLL Basic Interpreter

D.4 COMMUNICATIONS COMPONENTS

INS1671	ASTRO Communications Interface
INS8250	Asynchronous Communications Element (ACE)
INS8251	Programmable Communications Interface

MARCH 1977
Pub. No. 420305226-001C

National Semiconductor

INS8080A 8-Bit N-Channel Microprocessor

general description

The INS8080A is an 8-bit microprocessor housed in a standard, 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate MOS technology, functions as the central processing unit (CPU) in National Semiconductor's N8080 microcomputer family.

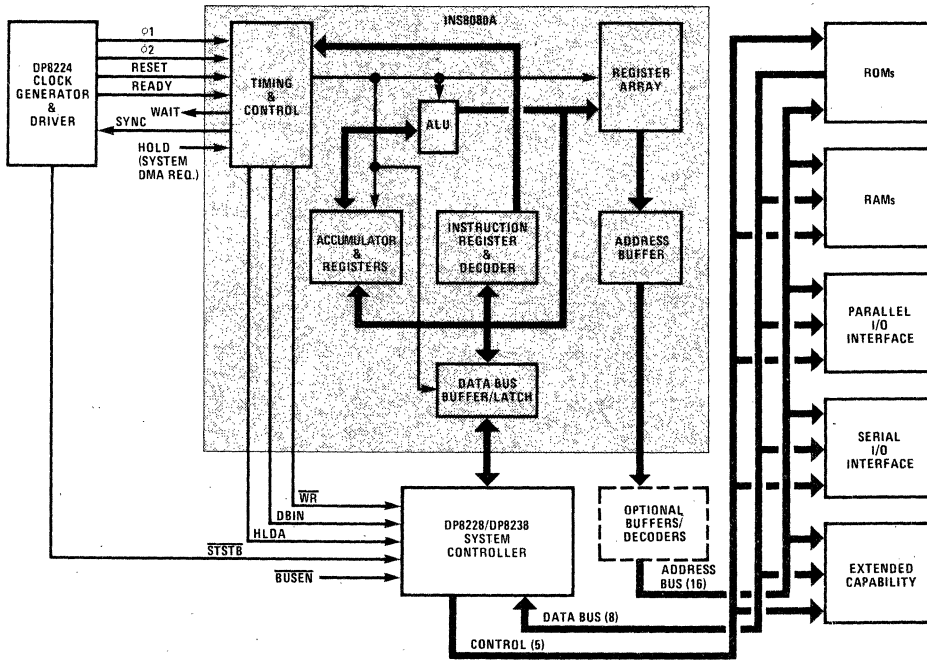
The INS8080A has a 16-bit address bus that is capable of addressing up to 65k bytes of memory and up to 256 input and 256 output devices. Data is routed to and from the INS8080A on a separate bidirectional 8-bit bus. This data bus is also TRI-STATE®, making direct memory addressing (DMA) and multiprocessing applications possible. The INS8080A directly provides signals to control the interface to memory and I/O ports. All buses, including control, are TTL compatible.

An asynchronous interrupt capability is included in the INS8080A to allow external signals to change the instruction sequence. The interrupting device may vector the program to a particular service routine location (or some other direct function) by specifying an interrupt instruction to be executed.

features

- 2μs Instruction Cycle
- Variable Length Instructions
- General Purpose Registers – Six plus an Accumulator
- Direct Addressing up to 65k Bytes
- Variable Length Stack Accessed by 16-bit Stack Pointer
- Addresses 256 Input and 256 Output Ports
- Provisions for Vectored Interrupts
- TRI-STATE® Bus for DMA and Multiprocessing Capability
- TRI-STATE TTL Drive Capabilities for Address and Data Buses
- Decimal Arithmetic Capability
- Multiple Addressing Modes
  - Direct
  - Register
  - Register Indirect
  - Immediate
- Direct Plug-in Replacement for Intel 8080A

N8080A microcomputer family block diagram



absolute maximum ratings

Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . -65°C to +150°C
All Input or Output Voltages
with Respect to V_{BB} . . . . . -0.3V to +20V
V_{CC}, V_{DD} and V_{SS} with Respect to V_{BB} . . -0.3V to +20V
Power Dissipation 1.5W

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

dc electrical characteristics

T_A = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, unless otherwise noted.

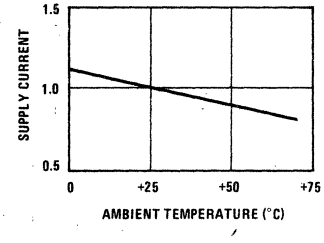
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	V_{SS}-1		V_{SS}+0.8	V	
V_{IHC}	Clock Input High Voltage	9.0		V_{DD}+1	V	
V_{IL}	Input Low Voltage	V_{SS}-1		V_{SS}+0.8	V	
V_{IH}	Input High Voltage	3.3		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs,
V_{OH}	Output High Voltage	3.7			V	I_{OH} = 150μA.
$I_{DD\ (AV)}$	Avg. Power Supply Current (V_{DD})		40	70	mA	Operation
$I_{CC\ (AV)}$	Avg. Power Supply Current (V_{CC})		60	80	mA	t_{CY} = 0.48μs
$I_{BB\ (AV)}$	Avg. Power Supply Current (V_{BB})		0.01	1	mA	
I_{IL}	Input Leakage			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{CL}	Clock Leakage			±10	μA	$V_{SS} \leq V_{CLOCK} \leq V_{DD}$
I_{DL}[2]	Data Bus Leakage in Input Mode			-100	μA	$V_{SS} \leq V_{IN} \leq V_{SS}$ + 0.8V
				-2.0	mA	V_{SS} + 0.8V $\leq V_{IN} \leq V_{CC}$
I_{FL}	Address and Data Bus Leakage			+10	μA	$V_{ADDR/DATA} = V_{CC}$
	During HOLD			-100	μA	$V_{ADDR/DATA} = V_{SS}$ + 0.45V

capacitance

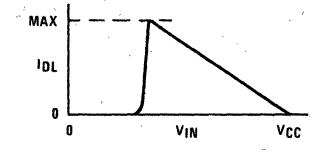
T_A = 25°C, V_{CC} = V_{DD} = V_{SS} = 0V, V_{BB} = -5V

Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pF	f_c = 1MHz
C_{IN}	Input Capacitance	6	10	pF	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pF	Returned to V_{SS}

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED[3]



DATA BUS CHARACTERISTIC DURING DBIN



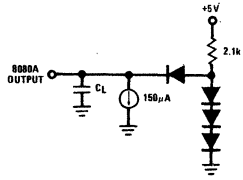
Notes:
1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pullup will be switched onto the Data Bus.
3. $\Delta I_{supply} / \Delta T_A$ = -0.45%/°C.

ac electrical characteristics

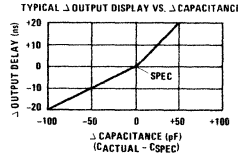
Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{CY} [3]	Clock Period	0.48	2.0	μs	
t_r, t_f	Clock Rise and Fall Time	0	50	ns	
$t_{\phi 1}$	ϕ_1 Pulse Width	60		ns	
$t_{\phi 2}$	ϕ_2 Pulse Width	220		ns	
t_{D1}	Delay ϕ_1 to ϕ_2	0		ns	
t_{D2}	Delay ϕ_2 to ϕ_1	70		ns	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	80		ns	
t_{DA} [2]	Address Output Delay from ϕ_2		200	ns	C_L = 100pF
t_{DD} [2]	Data Output Delay from ϕ_2		220	ns	C_L = 100pF
t_{DC} [2]	Signal Output Delay from ϕ_1 or ϕ_2 (SYNC, $\overline{WR}$, WAIT, HLDA)		120	ns	C_L = 50pF
t_{DF} [2]	DBIN Delay from ϕ_2	25	140	ns	C_L = 50pF
t_{DI} [1]	Delay for Input Bus to Enter Input Mode		t_{DF}	ns	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	30		ns	
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	150		ns	
t_{DH} [1]	Data Hold Time from ϕ_2 During DBIN	1		ns	
t_{IE} [2]	INTE Output Delay from ϕ_2		200	ns	C_L = 50pF
t_{RS}	READY Setup Time During ϕ_2	120		ns	
t_{HS}	HOLD Setup Time to ϕ_2	140		ns	
t_{IS}	INT Setup Time During ϕ_2 (During ϕ_1 in Halt Mode)	120		ns	
t_H	Hold Time from ϕ_2 (READY, INT, HOLD)	0		ns	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		120	ns	
t_{AW} [2]	Address Stable Prior to $\overline{WR}$	5		ns	C_L = 100pF : Address, Data C_L = 50pF: $\overline{WR}$, HLDA, DBIN
t_{DW} [2]	Output Data Stable Prior to $\overline{WR}$	6		ns	
t_{WD} [2]	Output Data Stable from $\overline{WR}$	7		ns	
t_{WA} [2]	Address Stable from $\overline{WR}$	7		ns	
t_{HF} [2]	HLDA to Float Delay	8		ns	
t_{WF} [2]	$\overline{WR}$ to Float Delay	9		ns	
t_{AH} [2]	Address Hold Time After DBIN During HLDA	-20		ns	

Notes:

1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50ns or t_{DF}, whichever is less.
2. Typical load circuit:



3. $t_{CY} = t_{D3} + t_{r\phi 2} + t_{\phi 2} + t_{D2} + t_{f\phi 2} + t_{r\phi 1} \geq 480$ns.

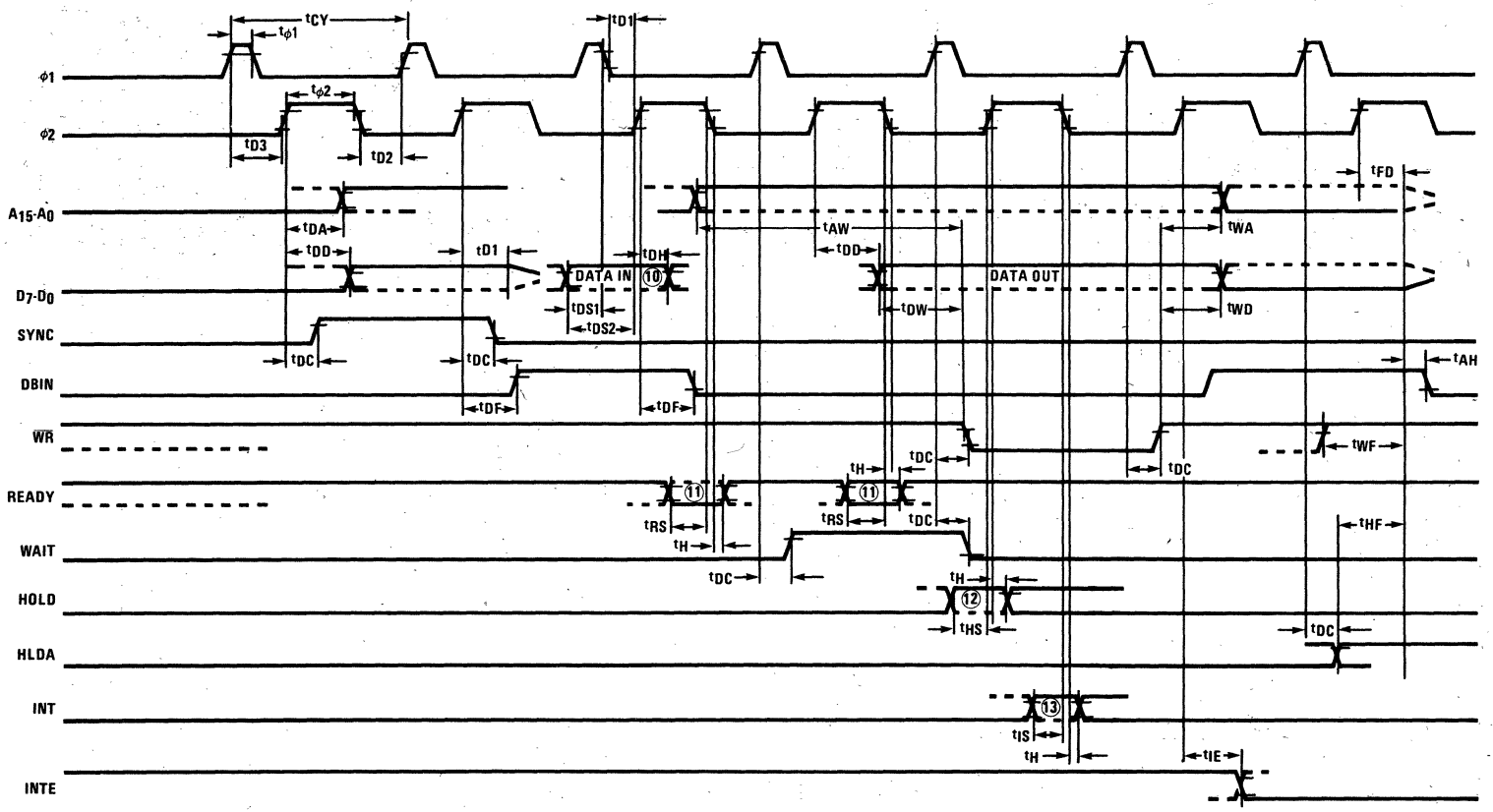


4. The following are relevant when interfacing the INS8080A to devices having V_{IH} = 3.3V:
   a) Maximum output rise time from 0.8V to 3.3V = 100ns @ C_L = SPEC.
   b) Output Delay when measured to 3.0V = SPEC + 60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC, add 0.6ns/pF if $C_L > C_{SPEC}$, subtract 0.3ns/pF (from modified delay) if $C_L < C_{SPEC}$.
5. $t_{AW} = 2t_{CY} - t_{D3} - t_{r\phi 2} - 140$ns.
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi 2} - 170$ns.
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi 2} + 10$ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi 2} - 50$ns.
9. $t_{WF} = t_{D3} + t_{r\phi 2} - 10$ns.
10. Data in must be stable for this period during DBIN · T_3. Both t_{DS1} and t_{DS2} must be satisfied.
11. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
12. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5, and T_{WH} when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

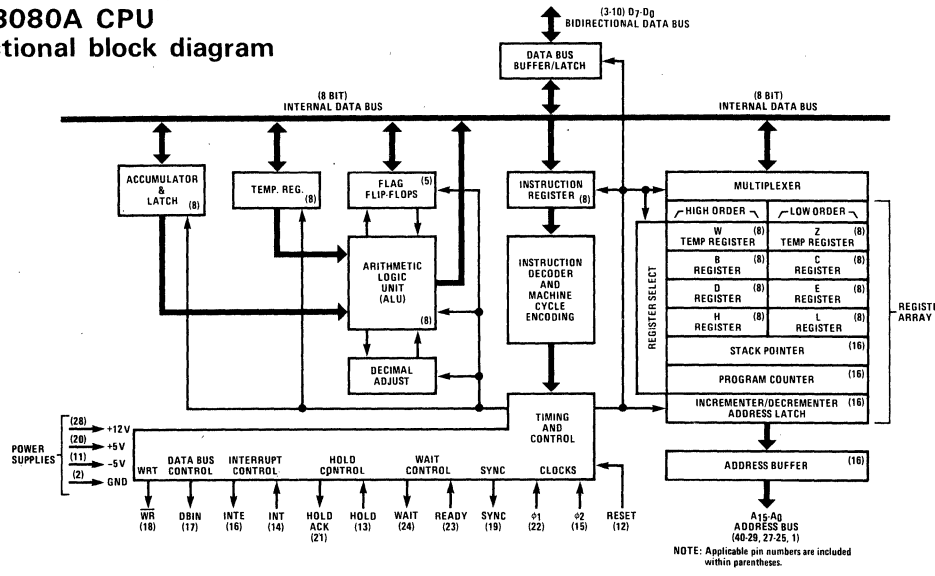
D.1

timing waveforms

Note: Timing measurements are made at the following reference voltages: CLOCK '1' = 8.0V, '0' = 1.0V; INPUTS '1' = 3.3V, '0' = 0.8V; OUTPUTS '1' = 2.0V, '0' = 0.8V.



INS8080A CPU functional block diagram



NOTE: Applicable pin numbers are included within parentheses.

INS8080A functional pin definition

The following describes the function of all of the INS8080A input/output pins. Some of these descriptions reference internal timing periods.

INPUT SIGNALS

Ready: When high (logic 1), indicates that valid memory or input data are available to the CPU on the INS8080A data bus. The READY signal is used to synchronize the CPU with slower memory or input/output devices. If the INS8080A does not receive a high READY input after sending out an address to memory or an input/output device, the INS8080A enters a WAIT mode for as long as the READY input remains low (logic 0). The CPU may also be single stepped by the use of the READY signal.

Hold: When high, requests that the CPU enter the HOLD mode. When the CPU is in the HOLD mode, the CPU address and data buses both will be in the high-impedance state. The HOLD mode allows an external device to gain control of the INS8080A address and data buses immediately following the completion of the current machine cycle by the CPU. The CPU acknowledges the HOLD mode via the HOLD ACKNOWLEDGE (HLDA) output line. The HOLD request is recognized under the following conditions:

- The CPU is in the HALT mode.
- The READY signal is active and the CPU is in the t_2 or t_W state.

Interrupt (INT) Request: When high, the CPU recognizes an interrupt request on this line after completing the current instruction or while in the HALT mode. An interrupt request is not honored if the CPU is in the HOLD mode (HLDA = logic 1) or the Interrupt Enable Flip-flop is reset (INTE = logic 0).

Reset: When activated (high) for a minimum of three clock periods, the content of the Program Counter is cleared and the Interrupt Enable and Hold Acknowledge Flip-flops are reset. Following a RESET, program execution starts at memory location 0. It should be noted that the status flags, accumulator, stack pointer, and registers are not cleared during the RESET sequence.

ϕ_1 and ϕ_2 Clocks: Two non-TTL compatible clock phases which provide nonoverlapping timing references for internal storage elements and logic circuits of the CPU.

+12 Volts: V_{DD} Supply.

+5 Volts: V_{CC} Supply.

–5 Volts: V_{BB} Supply.

Ground: V_{SS} (0 volt) reference.

OUTPUT SIGNALS

Synchronizing (SYNC) Signal: When activated (high), the beginning of a new machine cycle is indicated and the status word is outputted on the Data Bus.

Address (A_{15} – A_0) Bus: This bus comprises sixteen TRI-STATE output lines. The bus provides the address to memory (up to 65k bytes) or denotes the input/output device number for up to 256 input and 256 output peripherals.

Wait: When high, acknowledges that the CPU is in the WAIT mode.

Write ($\overline{WR}$): When low, the data on the data bus are stable for WRITE memory or output operation.

Hold Acknowledge (HLDA): Goes high in response to a logic 1 on the HOLD line and indicates that the data and address bus will go to the high-impedance state. The HLDA begins at one of the following times:

- The t_3 state of a READ memory input operation.
- The clock period following the t_3 state of a WRITE memory output operation.

In both cases, the HLDA signal starts after the rising edge of the ϕ_1 clock, and high impedance occurs after the rising edge of the ϕ_2 clock.

D.1

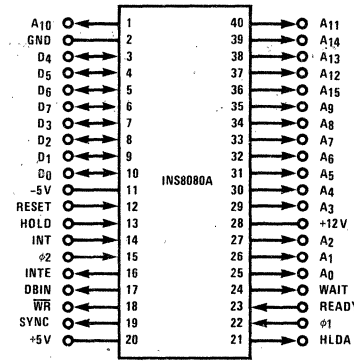
Interrupt Enable (INTE): Indicates the content of the internal Interrupt Enable Flip-flop. The Enable and Disable Interrupt (EI and DI) Instructions cause the Interrupt Enable Flip-flop to be set and reset, respectively. When the flip-flop is reset (INTE = logic 0), it inhibits interrupts from being accepted by the CPU. In addition, the Interrupt Enable Flip-flop is automatically reset (thereby disabling further interrupts) at the t_1 state of the instruction fetch cycle, when an interrupt is accepted; it is also reset by the RESET Signal.

Data Bus In (DBIN): When high, indicates to external circuits that the data bus is in the input mode. The DBIN Signal should be used to gate data from memory or an I/O device onto the Data Bus.

INPUT/OUTPUT SIGNALS

Data ($D_7 - D_0$) Bus: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communication between the CPU, memory, and input/output devices for instructions and data transfers. A status word (which describes the current machine cycle) is also outputted on the data bus during the first state of each machine cycle (SYNC = logic 1).

pin configuration



8080A status

Instructions for the 8080A require from one to five machine cycles for complete execution. The 8080A sends out 8 bits of status information on the data bus at the beginning of each machine cycle (during SYNC time). The following table defines the status information.

Status Information Definition

Symbols	Data Bus Bit	Definition
INTA*	D_0	Acknowledge signal for INTERRUPT request. Signal should be used to gate a restart instruction onto the data bus when DBIN is active.
$\overline{WO}$	D_1	Indicates that the operation in the current machine cycle will be a WRITE memory or OUTPUT function (WO = 0). Otherwise, a READ memory or INPUT operation will be executed.
STACK	D_2	Indicates that the address bus holds the pushdown stack address from the Stack Pointer.
HLTA	D_3	Acknowledge signal for HALT Instruction.
OUT	D_4	Indicates that the address bus contains the address of an output device and the data bus will contain the output data when WR is active.
M_1	D_5	Provides a signal to indicate that the CPU is in the fetch cycle for the first byte of an instuction.
INP*	D_6	Indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when DBIN is active.
MEMR*	D_7	Designates that the data bus will be used for memory read data.

*These three status bits can be used to control the flow of data onto the INS8080A data bus.

Status Word Chart

Machine Cycle	Type	Data Bus Bit							
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Instruction Fetch	1	1	0	1	0	0	0	1	0
Memory Read	2	1	0	0	0	0	0	1	0
Memory Write	3	0	0	0	0	0	0	0	0
Stack Read	4	1	0	0	0	0	1	1	0
Stack Write	5	0	0	0	0	0	1	0	0
Input Read	6	0	1	0	0	0	0	1	0
Output Write	7	0	0	0	1	0	0	0	0
Interrupt Acknowledge	8	0	0	1	0	0	0	1	1
Halt Acknowledge	9	1	0	0	0	1	0	1	0
Interrupt Acknowledge While Halt	10	0	0	1	0	1	0	1	1

instruction set

Mnemonic	Description	Operation	Op Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	No. of Bytes	No. of Machine (M) Cycles	No. of States (T)	Condition Flags S	Z	AC	P	CY
DATA TRANSFER GROUP																		
LDA	Load Accumulator Direct	(A) ← ((byte 3)(byte 2))	0	0	1	1	1	0	1	0	3	4	13					
LDAX B	Load Accumulator Indirect	(A) ← ((B)(C))	0	0	0	0	1	0	1	0	1	2	7					
LDAX D	Load Accumulator Indirect	(A) ← ((D)(E))	0	0	0	1	1	0	1	0	1	2	7					
LHLD	Load H and L Direct	(L) ← ((byte 3)(byte 2)) (H) ← ((byte 3)(byte 2) + 1)	0	0	1	0	1	0	1	0	3	5	16					
LXI B	Load Immediate, Registers B and C	(B) ← (byte 3) (C) ← (byte 2)	0	0	0	0	0	0	0	1	3	3	10					
LXI D	Load Immediate, Registers D and E	(D) ← (byte 3) (E) ← (byte 2)	0	0	0	1	0	0	0	1	3	3	10					
LXI H	Load Immediate, Registers H and L	(H) ← (byte 3) (L) ← (byte 2)	0	0	1	0	0	0	0	1	3	3	10					
LXI SP	Load Immediate, Stack Pointer	(SPH) ← (byte 3) (SPL) ← (byte 2)	0	0	1	1	0	0	0	1	3	3	10	(Flags Not Affected)				
MOV M, r	Move to Memory	((H)(L)) ← (r)	0	1	1	1	0	S	S	S	1	2	7					
MOV r, M	Move from Memory	(r) ← ((H)(L))	0	1	D	D	D	1	1	0	1	2	7					
MOV r1, r2	Move Registers	(r1) ← (r2)	0	1	D	D	D	S	S	S	1	1	5					
MVI M	Move to Memory Immediate	((H)(L)) ← (byte 2)	0	0	1	1	0	1	1	0	2	3	10					
MVI r	Move Immediate	(r) ← (byte 2)	0	0	D	D	D	1	1	0	2	2	7					
SHLD	Store H and L Direct	((byte 3)(byte 2)) ← (L) ((byte 3)(byte 2) + 1) ← (H)	0	0	1	0	0	0	1	0	3	5	16					
STA	Store Accumulator Direct	((byte 3)(byte 2)) ← (A)	0	0	1	1	0	0	1	0	3	4	13					
STAX B	Store Accumulator Indirect	((B)(C)) ← (A)	0	0	0	0	0	0	1	0	1	2	7					
STAX D	Store Accumulator Indirect	((D)(E)) ← (A)	0	0	0	1	0	0	1	0	1	2	7					
XCHG	Exchange H and L with D and E	(H) ↔ (D) (L) ↔ (E)	1	1	1	0	1	0	1	1	1	1	4					
ARITHMETIC GROUP																		
ACI	Add Immediate with Carry	(A) ← (A) + (byte 2) + (CY)	1	1	0	0	1	1	1	0	2	2	7	↕	↕	↕	↕	↕
ADC M	Add Memory with Carry	(A) ← (A) + ((H)(L)) + (CY)	1	0	0	0	1	1	1	0	1	2	7	↕	↕	↕	↕	↕
ADC r	Add Register with Carry	(A) ← (A) + (r) + (CY)	1	0	0	0	1	S	S	S	1	1	4	↕	↕	↕	↕	↕
ADD M	Add Memory	(A) ← (A) + ((H)(L))	1	0	0	0	0	1	1	0	1	2	7	↕	↕	↕	↕	↕
ADD r	Add Register	(A) ← (A) + (r)	1	0	0	0	0	S	S	S	1	1	4	↕	↕	↕	↕	↕
ADI	Add Immediate	(A) ← (A) + (byte 2)	1	1	0	0	0	1	1	0	1	2	7	↕	↕	↕	↕	↕
DAA	Decimal Adjust Accumulator	8-bit number in Accumulator is converted to two 4-bit BCD digits	0	0	1	0	0	1	1	1	1	1	4	↕	↕	↕	↕	↕
DAD B	Add B and C to H and L	(H)(L) ← (H)(L) + (B)(C)	0	0	0	0	1	0	0	1	1	3	10	·	·	·	·	↕
DAD D	Add D and E to H and L	(H)(L) ← (H)(L) + (D)(E)	0	0	0	1	1	0	0	1	1	3	10	·	·	·	·	↕
DAD H	Add H and L to H and L	(H)(L) ← (H)(L) + (H)(L)	0	0	1	0	1	0	0	1	1	3	10	·	·	·	·	↕
DAD SP	Add Stack Pointer to H and L	(H)(L) ← (H)(L) + (SP)	0	0	1	1	1	0	0	1	1	3	10	·	·	·	·	↕
DCR M	Decrement Memory	((H)(L)) ← ((H)(L)) − 1	0	0	1	1	0	1	0	1	1	3	10	↕	↕	↕	↕	·
DCR r	Decrement Register	(r) ← (r) − 1	0	0	D	D	D	1	0	1	1	1	5	↕	↕	↕	↕	·
DCX B	Decrement Registers B and C	(B)(C) ← (B)(C) − 1	0	0	0	0	1	0	1	1	1	1	5	·	·	·	·	·
DCX D	Decrement Registers D and E	(D)(E) ← (D)(E) − 1	0	0	0	1	1	0	1	1	1	1	5	·	·	·	·	·
DCX H	Decrement Registers H and L	(H)(L) ← (H)(L) − 1	0	0	1	0	1	0	1	1	1	1	5	·	·	·	·	·
DCX SP	Decrement Stack Pointer	(SP) ← (SP) − 1	0	0	1	1	1	0	1	1	1	1	5	·	·	·	·	·
INR M	Increment Memory	((H)(L)) ← ((H)(L)) + 1	0	0	1	1	0	1	0	0	1	3	10	↕	↕	↕	↕	·
INR r	Increment Register	(r) ← (r) + 1	0	0	D	D	D	1	0	0	1	1	5	↕	↕	↕	↕	·
INX B	Increment Registers B and C	(B)(C) ← (B)(C) + 1	0	0	0	0	0	0	1	1	1	1	5	·	·	·	·	·
INX D	Increment Registers D and E	(D)(E) ← (D)(E) + 1	0	0	0	1	0	0	1	1	1	1	5	·	·	·	·	·
INX H	Increment Registers H and L	(H)(L) ← (H)(L) + 1	0	0	1	0	0	0	1	1	1	1	5	·	·	·	·	·
INX SP	Increment Stack Pointer	(SP) ← (SP) + 1	0	0	1	1	0	0	1	1	1	1	5	·	·	·	·	·
SBB M	Subtract Memory with Borrow	(A) ← (A) − ((H)(L)) − (CY)	1	0	0	1	1	1	1	0	1	2	7	↕	↕	↕	↕	↕
SBB r	Subtract Register with Borrow	(A) ← (A) − (r) − (CY)	1	0	0	1	1	S	S	S	1	1	4	↕	↕	↕	↕	↕
SBI	Subtract Immediate with Borrow	(A) ← (A) − (byte 2) − (CY)	1	1	0	1	1	1	1	0	2	2	7	↕	↕	↕	↕	↕
SUB M	Subtract Memory	(A) ← (A) − ((H)(L))	1	0	0	1	0	1	1	0	1	2	7	↕	↕	↕	↕	↕
SUB r	Subtract Register	(A) ← (A) − (r)	1	0	0	1	0	S	S	S	1	1	4	↕	↕	↕	↕	↕
SUI	Subtract Immediate	(A) ← (A) − (byte 2)	1	1	0	1	0	1	1	0	2	2	7	↕	↕	↕	↕	↕
LOGICAL GROUP																		
ANA M	AND Memory	(A) ← (A) ∧ ((H)(L))	1	0	1	0	0	1	1	0	1	2	7	↕	↕	↕[d]	↕	0
ANA r	AND Register	(A) ← (A) ∧ (r)	1	0	1	0	0	S	S	S	1	1	4	↕	↕	↕[d]	↕	0
ANI	AND Immediate	(A) ← (A) ∧ (byte 2)	1	1	1	0	0	1	1	0	2	2	7	↕	↕	↕[d]	↕	0
CMA	Complement Accumulator	(A) ← $(\overline{A})$	0	0	1	0	1	1	1	1	1	1	4	·	·	·	·	·
CMC	Complement Carry	(CY) ← $(\overline{CY})$	0	0	1	1	1	1	1	1	1	1	4	·	·	·	·	↕
CMP M	Compare Memory	(A) — ((H)(L))	1	0	1	1	1	1	1	0	1	2	7	↕	↕[a]	↕	↕	↕[a]
CMP r	Compare Register	(A) — (r)	1	0	1	1	1	S	S	S	1	1	4	↕	↕[b]	↕	↕	↕[b]
CPI	Compare Immediate	(A) — (byte 2)	1	1	1	1	1	1	1	0	2	2	7	↕	↕[c]	↕	↕	↕[c]
ORA M	OR Memory	(A) ← (A) ∨ ((H)(L))	1	0	1	1	0	1	1	0	1	2	7	↕	↕	0	↕	0
ORA r	OR Register	(A) ← (A) ∨ (r)	1	0	1	1	0	S	S	S	1	1	4	↕	↕	0	↕	0
ORI	OR Immediate	(A) ← (A) ∨ (byte 2)	1	1	1	1	0	1	1	0	2	2	7	↕	↕	0	↕	0
RAL	Rotate Left through Carry	$(A_{n+1}) \leftarrow (A_n)$; (CY) ← (A_7) (A_0) ← (CY)	0	0	0	1	0	1	1	1	1	1	4	·	·	·	·	↕
RAR	Rotate Right through Carry	$(A_n) \leftarrow (A_{n+1})$; (CY) ← (A_0) (A_7) ← (CY)	0	0	0	1	1	1	1	1	1	1	4	·	·	·	·	↕
RLC	Rotate Left	$(A_{n+1}) \leftarrow (A_n)$; $(A_0) \leftarrow (A_7)$ (CY) ← (A_7)	0	0	0	0	0	1	1	1	1	1	4	·	·	·	·	↕
RRC	Rotate Right	$(A_n) \leftarrow (A_{n-1})$; $(A_7) \leftarrow (A_0)$ (CY) ← (A_0)	0	0	0	0	1	1	1	1	1	1	4	·	·	·	·	↕
STC	Set Carry	(CY) ← 1	0	0	1	1	0	1	1	1	1	1	4	·	·	·	·	1
XRA M	Exclusive OR Memory	(A) ← (A) ∀ ((H)(L))	1	0	1	0	1	1	1	0	1	2	7	↕	↕	0	↕	0
XRA r	Exclusive OR Register	(A) ← (A) ∀ (r)	1	0	1	0	1	S	S	S	1	1	4	↕	↕	0	↕	0
XRI	Exclusive OR Immediate	(A) ← (A) ∀ (byte 2)	1	1	1	0	1	1	1	0	2	2	7	↕	↕	0	↕	0

Notes:

a. Z = 1 if (A) = (H)(L); CY = 1 if (A) < (H)(L)

b. Z = 1 if (A) = (r); CY = 1 if (A) < (r)

c. Z = 1 if (A) = (byte 2); CY = 1 if (A) < (byte 2)

d. As if an arithmetic operation were performed.

D.1

instruction set (cont'd.)

Mnemonic	Description	Operation	Op Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	No. of Bytes	No. of Machine (M) Cycles	No. of States (T)	Condition Flags S	Z	AC	P	CY
BRANCH GROUP																		
CALL	Call Unconditional	((SP) – 1) ← (PCH) ((SP) – 2) ← (PCL) (SP) ← (SP) – 2 (PC) ← (byte 3) (byte 2)	1	1	0	0	1	1	0	1	3	5	17					
CC	Call on Carry	If CY = 1, ((SP) – 1) ← (PCH) ((SP) – 2) ← (PCL) (SP) ← (SP) – 2 (PC) ← (byte 3) (byte 2)	1	1	0	1	1	1	0	0	3	3/5	11/17					
CM	Call on Minus	If S = 1, ((SP) – 1) ← (PCH) ((SP) – 2) ← (PCL) (SP) ← (SP) – 2 (PC) ← (byte 3) (byte 2)	1	1	1	1	1	1	0	0	3	3/5	11/17					
CNC	Call on No Carry	If CY = 0, ((SP) – 1) ← (PCH) ((SP) – 2) ← (PCL) (SP) ← (SP) – 2 (PC) ← (byte 3) (byte 2)	1	1	0	1	0	1	0	0	3	3/5	11/17					
CNZ	Call on Not Zero	If Z = 0, ((SP) – 1) ← (PCH) ((SP) – 2) ← (PCL) (SP) ← (SP) – 2 (PC) ← (byte 3) (byte 2)	1	1	0	0	0	1	0	0	3	3/5	11/17	(Flags Not Affected)				
CP	Call on Positive	If S = 0, ((SP) – 1) ← (PCH) ((SP) – 2) ← (PCL) (SP) ← (SP) – 2 (PC) ← (byte 3) (byte 2)	1	1	1	1	0	1	0	0	3	3/5	11/17					
CPE	Call on Parity Even	If P = 1, ((SP) – 1) ← (PCH) ((SP) – 2) ← (PCL) (SP) ← (SP) – 2 (PC) ← (byte 3) (byte 2)	1	1	1	0	1	1	0	0	3	3/5	11/17					
CPO	Call on Parity Odd	If P = 0, ((SP) – 1) ← (PCH) ((SP) – 2) ← (PCL) (SP) ← (SP) – 2 (PC) ← (byte 3) (byte 2)	1	1	1	0	0	1	0	0	3	3/5	11/17					
CZ	Call on Zero	If Z = 1, ((SP) – 1) ← (PCH) ((SP) – 2) ← (PCL) (SP) ← (SP) – 2 (PC) ← (byte 3) (byte 2)	1	1	0	0	1	1	0	0	3	3/5	11/17					
JC	Jump on Carry	If CY = 1, (PC) ← (byte 3) (byte 2)	1	1	0	1	1	0	1	0	3	3	10					
JM	Jump on Minus	If S = 1, (PC) ← (byte 3) (byte 2)	1	1	1	1	1	0	1	0	3	3	10					
JMP	Jump Unconditional	(PC) ← (byte 3) (byte 2)	1	1	0	0	0	0	1	1	3	3	10					
JNC	Jump on No Carry	If CY = 0, (PC) ← (byte 3) (byte 2)	1	1	0	1	0	0	1	0	3	3	10					
JNZ	Jump on Not Zero	If Z = 0, (PC) ← (byte 3) (byte 2)	1	1	0	0	0	0	1	0	3	3	10					
JP	Jump on Positive	If S = 0, (PC) ← (byte 3) (byte 2)	1	1	1	1	0	0	1	0	3	3	10					
JPE	Jump on Parity Even	If P = 1, (PC) ← (byte 3) (byte 2)	1	1	1	0	1	0	1	0	3	3	10					
JPO	Jump on Parity Odd	If P = 0, (PC) ← (byte 3) (byte 2)	1	1	1	0	0	0	1	0	3	3	10					
JZ	Jump on Zero	If Z = 1, (PC) ← (byte 3) (byte 2)	1	1	0	0	1	0	1	0	3	3	10					
PCHL	H and L to Program Counter	(PCH) ← (H) (PCL) ← (L)	1	1	1	0	1	0	0	1	1	1	5					
RC	Return on Carry	If CY = 1, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	1	1	0	0	0	1	1/3	5/11					
RET	Return	(PCL) ← ((SP)); (PCH) ← ((SP) + 1); (SP) ← (SP) + 2;	1	1	0	0	1	0	0	1	1	3	10					
RM	Return on Minus	If S = 1, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	1	1	0	0	0	1	1/3	5/11					
RNC	Return on No Carry	If CY = 0, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	1	0	0	0	0	1	1/3	5/11					
RNZ	Return on Not Zero	If Z = 0, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	0	0	0	0	0	0	1	1/3	5/11					
RP	Return on Positive	If S = 0, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	1	0	0	0	0	1	1/3	5/11					
RPE	Return on Parity Even	If P = 1, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	0	1	0	0	0	1	1/3	5/11					
RPO	Return on Parity Odd	If P = 0, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1	1	1	0	0	0	0	0	1	1/3	5/11					

instruction set (cont'd.)

Mnemonic	Description	Operation	Op Code D_7 D_6 D_5 D_4	Op Code D_3 D_2 D_1 D_0	No. of Bytes	No. of Machine (M) Cycles	No. of States (T)	Condition Flags S	Z	AC	P	CY
BRANCH GROUP (continued)												
RST	Restart	((SP) − 1) ← (PCH) ((SP) − 2) ← (PCL) (SP) ← (SP) − 2 (PC) ← 8 * (NNN)	1 1 *N* *N*	*N* 1 1 1	1	3	11					
RZ	Return on Zero	If Z = 1, (PCL) ← ((SP)) (PCH) ← ((SP) + 1) (SP) ← (SP) + 2	1 1 0 0	1 0 0 0	1	1/3	5/11					
STACK, I/O, AND MACHINE CONTROL GROUP												
DI	Disable Interrupts	The Interrupt system is disabled following the execution of the DI instruction.	1 1 1 1	0 0 1 1	1	1	4	·	·	·	·	·
EI	Enable Interrupts	The interrupt system is enabled following the execution of next instruction.	1 1 1 1	1 0 1 1	1	1	4	·	·	·	·	·
HLT	Halt	Processor is stopped; registers and flags are unaffected.	0 1 1 1	0 1 1 0	1	1	7	·	·	·	·	·
IN	Input	(A) ← (data)	1 1 0 1	1 0 1 1	2	3	10	·	·	·	·	·
NOP	No Operation	No operation is performed; registers and flags are unaffected.	0 0 0 0	0 0 0 0	1	1	4	·	·	·	·	·
OUT	Output	(data) ← (A)	1 1 0 1	0 0 1 1	2	3	10	·	·	·	·	·
POP B	Pop Registers B and C off Stack	(C) ← ((SP)) (B) ← ((SP) + 1) (SP) ← (SP) + 2	1 1 0 0	0 0 0 1	1	3	10	·	·	·	·	·
POP D	Pop Registers D and E off Stack	(E) ← ((SP)) (D) ← ((SP) + 1) (SP) ← (SP) + 2	1 1 0 1	0 0 0 1	1	3	10	·	·	·	·	·
POP H	Pop Registers H and L off Stack	(L) ← ((SP)) (H) ← ((SP) + 1) (SP) ← (SP) + 2	1 1 1 0	0 0 0 1	1	3	10	·	·	·	·	·
POP PSW	Pop Accumulator and Flags off Stack	(CY) ← $((SP))_0$ (P) ← $((SP))_2$ (AC) ← $((SP))_4$ (Z) ← $((SP))_6$ (S) ← $((SP))_7$ (A) ← ((SP) + 1) (SP) ← (SP) + 2	1 1 1 1	0 0 0 1	1	3	10	↕	↕	↕	↕	↕
PUSH B	Push Registers B and C on Stack	((SP) − 1) ← (B) ((SP) − 2) ← (C) (SP) ← (SP) − 2	1 1 0 0	0 1 0 1	1	3	11	·	·	·	·	·
PUSH D	Push Registers D and E on Stack	((SP) − 1) ← (D) ((SP) − 2) ← (E) (SP) ← (SP) − 2	1 1 0 1	0 1 0 1	1	3	11	·	·	·	·	·
PUSH H	Push Registers H and L on Stack	((SP) − 1) ← (H) ((SP) − 2) ← (L) (SP) ← (SP) − 2	1 1 1 0	0 1 0 1	1	3	11	·	·	·	·	·
PUSH PSW	Push Accumulator and Flags on Stack	((SP) − 1) ← (A) $((SP) - 2)_0$ ← (CY) $((SP) - 2)_1$ ← 1 $((SP) - 2)_2$ ← (P) $((SP) - 2)_3$ ← 0 $((SP) - 2)_4$ ← (AC) $((SP) - 2)_5$ ← 0 $((SP) - 2)_6$ ← (Z) $((SP) - 2)_7$ ← (S) (SP) ← (SP) − 2	1 1 1 1	0 1 0 1	1	3	11	·	·	·	·	·
SPHL	Move H and L to Stack Pointer	(SP) ← (H) (L)	1 1 1 1	1 0 0 1	1	1	5	·	·	·	·	·
XTHL	Exchange Top of Stack with H and L	(L) ↔ ((SP)) (H) ↔ ((SP) + 1)	1 1 1 0	0 0 1 1	1	5	18	·	·	·	·	·

condition flags and standard rules

There are five condition flags associated with the execution of instructions on the INS8080A. They are Zero, Sign, Parity, Carry, and Auxiliary Carry, and each flag is represented by a 1-bit register in the CPU. A flag is "set" by forcing the bit to 1, "reset" by forcing the bit to 0. The bit positions of the flags are indicated in the PUSH and POP PSW instructions.

Unless indicated otherwise, when an instruction affects a flag, it affects it in the following manner:

ZERO (Z): If the result of an instruction has the value 0, this flag is set; otherwise, it is reset.

SIGN (S): If the most significant bit of the result of the operation has the value 1, this flag is set; otherwise, it is reset.

PARITY (P): If the modulo 2 sum of the bits of the result of the operation is 0 (that is, if the result has even parity), this flag is set; otherwise, it is reset (that is, if the result has odd parity).

CARRY (CY): If the instruction resulted in a carry (from addition) or a borrow (from subtraction or a comparison) out of the high-order bit, this flag is set; otherwise, it is reset.

AUXILIARY CARRY (AC): If the instruction caused a carry out of bit 3 and into bit 4 of the resulting value, the auxiliary carry is set; otherwise, it is reset. This flag is affected by single-precision additions, subtractions, increments, decrements, comparisons, and logical operations; however, AC is used principally with additions and increments preceding a DAA (Decimal Adjust Accumulator) Instruction.

D.1

symbols and abbreviations

The following symbols and abbreviations are used in the subsequent description of the INS8080A instructions:

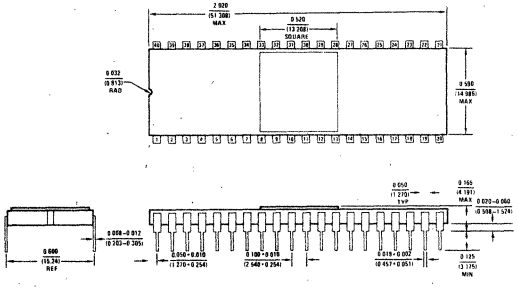
Symbols	Meaning
A	Register A (Accumulator)
B	Register B
C	Register C
D	Register D
H	Register H
L	Register L
DDD, SSS	The bit pattern designating one of the registers A, B, C, D, E, H, L (DDD = destination, SSS = source):

DDD or SSS	Register Name
111	A
000	B
001	C
010	D
011	E
100	H
101	L

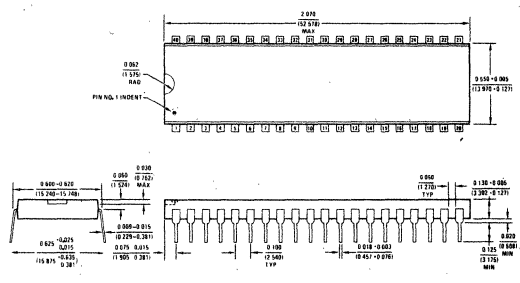
byte 2	The second byte of the instruction
byte 3	The third byte of the instruction
port	8-bit address of an I/O device
r, r1, r2	One of the registers A, B, C, D, E, H, L

Symbols	Meaning
PC	16-bit program counter register (PCH and PCL are used to refer to the high-order and low-order 8 bits respectively.)
SP	16-bit stack pointer register (SPH and SPL are used to refer to the high-order and low-order 8 bits respectively.)
( )	The contents of the memory location or registers enclosed in the parentheses
←	"Is replaced by"
∧	Logical AND
∀	Exclusive OR
∨	Inclusive OR
+	Addition
−	Twos complement subtraction
*	Multiplication
↔	"Exchange"
—	The ones complement (for example, $(\overline{A})$)
n	The restart number 0 through 7
NNN	The binary representation 000 through 111 for restart number 0 through 7 respectively
•	"Not affected"
0	"Reset"
1	"Set"
x	Unknown
↕	Flags affected according to Standard Rules, except as noted.

physical dimensions



40-Lead Ceramic Dual-in-Line Package (D)
Order Number INS8080AD



40-Lead Plastic Dual-in-Line Package (N)
Order Number INS8080N

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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National Semiconductor

APRIL 1978

INS8224 Clock Generator and Driver

General Description

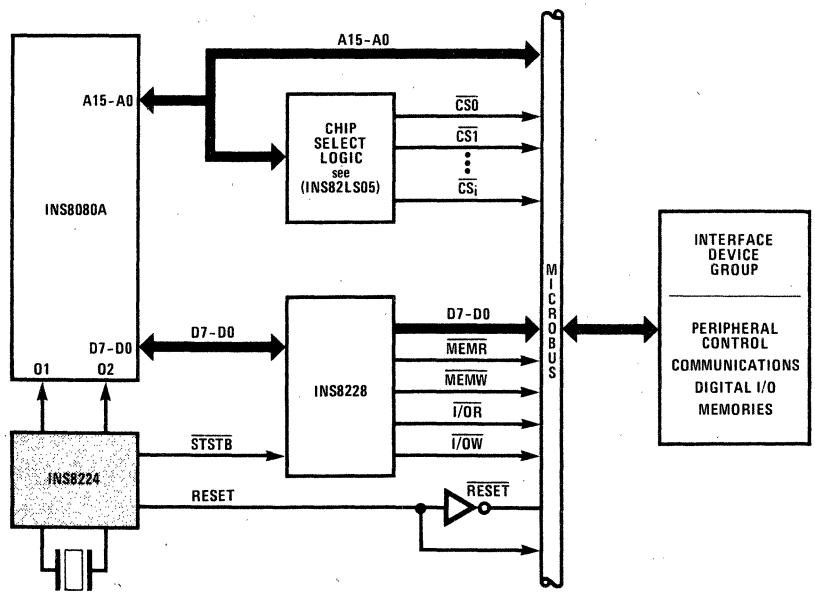
The INS8224 is a clock generator/driver contained in a standard, 16-pin dual-in-line package. The chip, which is fabricated using Schottky Bipolar technology, generates clocks and timing for National Semiconductor's INS8080 microcomputer family.

Included in the INS8224 is an oscillator circuit that is controlled by an external crystal, which is selected by the designer to meet a variety of system speed requirements. Also included in the chip are circuits that provide: a status strobe for the INS8228 or INS8238 system controllers, power-on reset for the INS8080A microprocessor, and synchronization of the READY input to the INS8080A.

Features

- Crystal-Controlled Oscillator for Stable System Operation
- Single Chip Clock Generator and Driver for INS8080A Microprocessor
- Provides Status Strobe for INS8228 or INS8238 System Controllers
- Provides Power-On Reset for INS8080A Microprocessor
- Synchronizes READY Input to INS8080A Microprocessor
- Provides Oscillator Output for Synchronization of External Circuits
- Reduces System Component Count

INS8080 Family CPU Group to MICROBUS™* Configuration



*Trademark, National Semiconductor Corp.

Absolute Maximum Ratings (NOTE 2)

Supply Voltage, V_{CC} . . . . . 7 V
V_{DD} . . . . . 15 V
Input Voltage . . . . . −1.0 V to +5.5 V
Storage Temperature Range. . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

Operating Conditions

	Min.	Max.	Units
Supply Voltage			
V_{CC}	4.75	5.25	V
V_{DD}	11.4	12.6	V
Temperature	0	70	°C

DC Electrical Characteristics

T_A = 0°C to +70°C; V_{CC} = +5.0 V ± 5%; V_{DD} = +12 V ± 5%.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Current Loading			−0.25	mA	V_F = 0.45 V
I_R	Input Leakage Current			10	μA	V_R = 5.25 V
V_C	Input Forward Clamp Voltage			−1.0	V	I_C = −5 mA
V_{IL}	Input "Low" Voltage			0.8	V	V_{CC} = 5.0 V
V_{IH}	Input "High" Voltage	2.6 2.0			V V	$\overline{RESIN}$ Input All Other Inputs
V_{IH} - V_{IL}	$\overline{RESIN}$ Input Hysteresis	0.25			V	V_{CC} = 5.0 V
V_{OL}	Output "Low" Voltage			0.45 0.45	V V	(ϕ_1, ϕ_2), Ready, Reset, $\overline{STSTB}$ I_{OL} = 2.5 mA All Other Outputs I_{OL} = 15 mA
V_{OH}	Output "High" Voltage ϕ_1, ϕ_2 READY, RESET All Other Outputs	 9.4 3.6 2.4			 V V V	 I_{OH} = −100 μA I_{OH} = −100 μA I_{OH} = −1 mA
I_{SC}[1]	Output Short Circuit Current (All Low Voltage Outputs Only)	−10		−60	mA	V_O = 0 V V_{CC} = 5.0 V
I_{CC}	Power Supply Current			115	mA	
I_{DD}	Power Supply Current			12	mA	

Notes:

1. Caution — ϕ_1 and ϕ_2 output drivers do not have short circuit protection.
2. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Crystal Requirements*

Tolerance. . . . . 0.005% at 0°C to +70°C
Resonance . . . . . Fundamental*
Load Capacitance . . . . . 20 pF to 30 pF
Equivalent Resistance. . . . . 75 Ω to 20 Ω
Power Dissipation (min). . . . . 4 mW

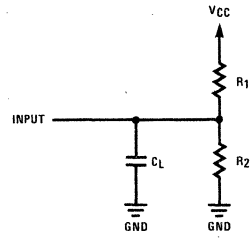
*It is good design practice to ground the case of the crystal
*With tank circuit use 3rd overtone mode.

AC Electrical Characteristics

$T_A = 0°C$ to $+70°C$; $V_{CC} = +5.0\ V \pm 5\%$; $V_{DD} = +12\ V \pm 5\%$.

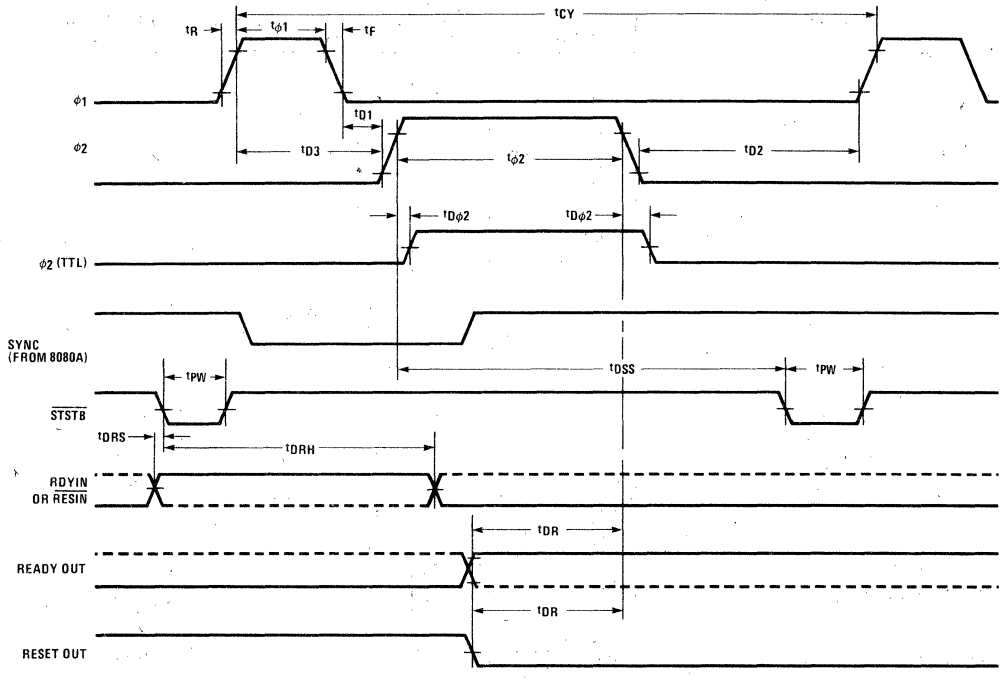
Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{\phi 1}$	ϕ_1 Pulse Width	$\frac{2t_{CY}}{9} - 20\ ns$			ns	$C_L = 20\ pF$ to $50\ pF$
$t_{\phi 2}$	ϕ_2 Pulse Width	$\frac{5t_{CY}}{9} - 35\ ns$				
t_{D1}	ϕ_1 to ϕ_2 Delay	0				
t_{D2}	ϕ_2 to ϕ_1 Delay	$\frac{2t_{CY}}{9} - 14\ ns$				
t_{D3}	ϕ_1 to ϕ_2 Delay	$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9} + 20\ ns$		
t_R	ϕ_1 and ϕ_2 Rise Time			20		
t_F	ϕ_1 and ϕ_2 Fall Time			20		
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	−5		+15	ns	ϕ_2 TTL, $C_L = 30\ pF$ $R_1 = 300\ \Omega$ $R_2 = 600\ \Omega$
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	$\frac{6t_{CY}}{9} - 30\ ns$		$\frac{6t_{CY}}{9}$		$\overline{STSTB}$, $C_L = 15\ pF$ $R_1 = 2\ k\Omega$ $R_2 = 4\ k\Omega$
t_{PW}	$\overline{STSTB}$ Pulse Width	$\frac{t_{CY}}{9} - 15\ ns$				
t_{DRS}	RDYIN Setup Time to Status Strobe	$50\ ns - \frac{4t_{CY}}{9}$				
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$	$\frac{4t_{CY}}{9}$				
t_{DR}	READY or RESET to ϕ_2 Delay	$\frac{4t_{CY}}{9} - 25\ ns$				Ready & Reset $C_L = 10\ pF$ $R_1 = 2\ k\Omega$ $R_2 = 4\ k\Omega$
t_{CLK}	CLK Period		$\frac{t_{CY}}{9}$			
f_{MAX}	Maximum Oscillating Frequency	27			MHz	
C_{IN}	Input Capacitance			8	pF	$V_{CC} = +5.0\ V$ $V_{DD} = +12\ V$ $V_{BIAS} = 2.5\ V$ $f = 1\ MHz$

Test Circuit



D.1

Waveforms



VOLTAGE MEASUREMENT POINTS: ϕ_1, ϕ_2 Logic "0" = 1.0 V, Logic "1" = 8.0 V. All other signals measured at 1.5 V.

AC Electrical Characteristics (For t_{CY} = 488.28 ns)

$T_A = 0°C$ to $+70°C$; V_{CC} = +5.0 V ± 5%; V_{DD} = +12 V ± 5%.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{\phi 1}$	ϕ_1 Pulse Width	89			ns	t_{CY} = 488.28 ns
$t_{\phi 2}$	ϕ_2 Pulse Width	236			ns	
t_{D1}	Delay ϕ_1 to ϕ_2	0			ns	
t_{D2}	Delay ϕ_2 to ϕ_1	95			ns	ϕ_1 & ϕ_2 Loaded to C_L = 20 to 50 pF
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	109		129	ns	
t_r	Output Rise Time			20	ns	
t_f	Output Fall Time			20	ns	
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	296		326	ns	
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	
t_{PW}	Status Strobe Pulse Width	40			ns	
t_{DRS}	RDYIN Setup Time to $\overline{STSTB}$	-167			ns	Ready & Reset Loaded to 2 mA/10 pF
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$	217			ns	All measurements referenced to 1.5 V unless specified otherwise.
t_{DR}	READY or RESET to ϕ_2 Delay	192			ns	
f_{MAX}	Oscillator Frequency			18.432	MHz	

INS8224 Functional Pin Definitions

The following describes the function of all of the INS8224 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Crystal Connections (XTAL 1 and XTAL 2): Two inputs that connect an external crystal to the oscillator circuit of the INS8224. Normally, a fundamental mode crystal is used to determine the basic operating frequency of the oscillator. However, overtone mode crystals may also be used. The crystal frequency is nine times the desired microprocessor speed (that is, crystal frequency equals $1/t_{CY} \times 9$). When the crystal frequency is above 10 MHz, a selected capacitor (3 to 10 picofarads) may have to be connected in series with the crystal to produce the exact desired frequency. Figure A.

Tank: Allows the use of overtone mode crystals with the oscillator circuit. When an overtone mode crystal is used, the tank input connects to a parallel LC network that is ac coupled to ground. The formula for determining the resonant frequency of this LC network is as follows:

$$F = \frac{1}{2\pi\sqrt{LC.}}$$

Synchronizing (SYNC) Signal: When high, indicates the beginning of a new machine cycle. The INS8080A microprocessor outputs a status word (which describes the current machine cycle) onto its data bus during the first state (SYNC interval) of each machine cycle.

Reset In ($\overline{\text{RESIN}}$): Provides an automatic system reset and start-up upon application of power as follows. The $\overline{\text{RESIN}}$ input, which is obtained from the junction of an external RC network that is connected between V_{CC} and ground, is routed to an internal Schmitt Trigger circuit. This circuit converts the slow transition of the power supply rise into a sharp, clean edge when its input reaches a predetermined value. When this occurs, an internal D-type flip-flop is synchronously reset, thereby providing the RESET output signal discussed below.

For manual system reset, a momentary contact switch that provides a low (ground) when closed is also connected to the $\overline{\text{RESIN}}$ input.

Ready In (RDYIN): An asynchronous READY signal that is re-clocked by a D-type flip-flop of the INS8224 to provide the synchronous READY output discussed below.

+5 Volts: V_{CC} supply.

+12 Volts: V_{DD} supply.

Ground: 0 volt reference.

OUTPUT SIGNALS

Oscillator (OSC): A buffered oscillator signal that can be used for external timing purposes.

ϕ_1 and ϕ_2 Clocks: Two non-TTL compatible clock phases that provide nonoverlapping timing references for internal storage elements and logic circuits of the INS8080A microprocessor. The two clock phases are produced by an internal clock generator that consists of a divide-by-nine counter and the associated decode gating logic. Figure B.

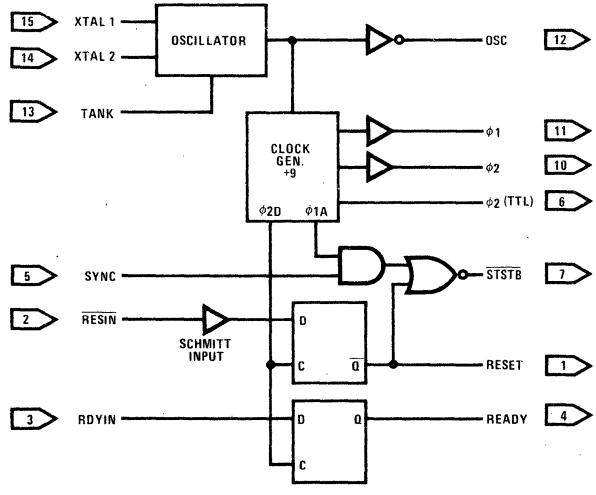
ϕ_2 (TTL) Clock: A TTL ϕ_2 clock phase that can be used for external timing purposes.

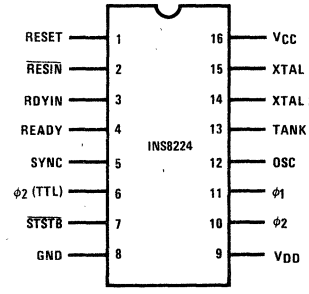
Status Strobe ($\overline{\text{STSTB}}$): Activated (low) at the start of each new machine cycle. The $\overline{\text{STSTB}}$ signal is generated by gating a high-level SYNC input with the ϕ_{1A} timing signal from the internal clock generator of the INS8224. The $\overline{\text{STSTB}}$ signal is used to clock status information into the status latch of the INS8228 system controller and bus driver.

Reset: When the RESET signal is activated, the content of the program counter of the INS8080A is cleared. After RESET, the program will start at location 0 in memory.

Ready: The READY signal indicates to the INS8080A that valid memory or input data is available. This signal is used to synchronize the INS8080A with slower memory or input/output devices.

Logic Diagram and Pin Configuration





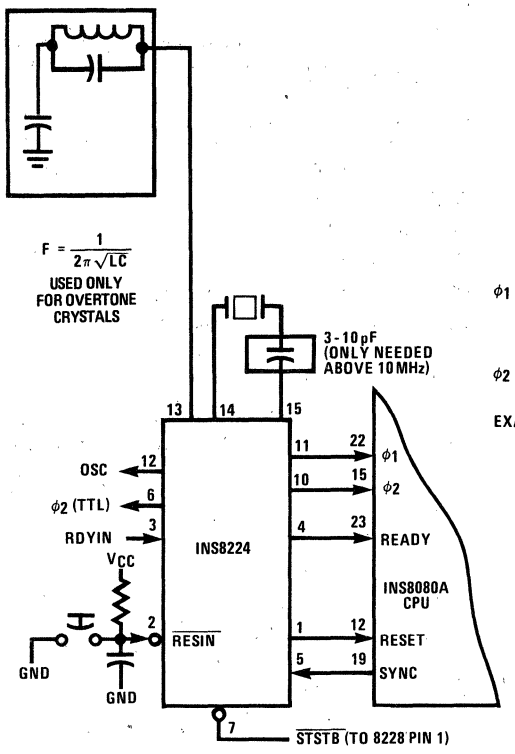


Figure A. INS8224 Connection Diagram

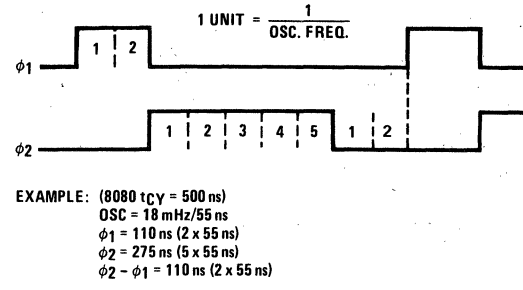
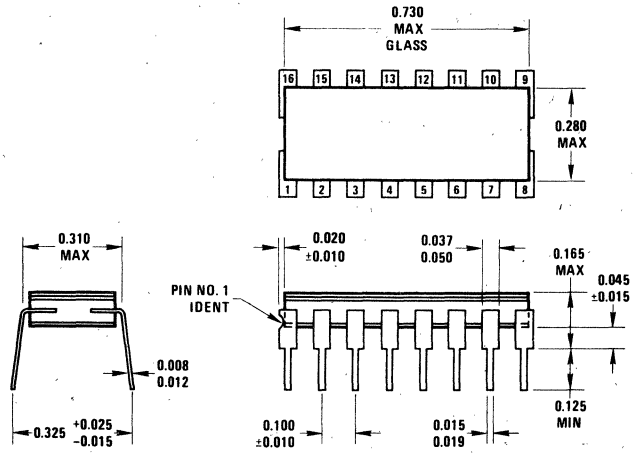


Figure B. INS8224 Clock Generator Waveforms

Physical Dimensions



16-Pin D Package
Order Number INS8224D

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National Semiconductor

APRIL 1978

INS8228/INS8238 System Controller and Bus Driver

General Description

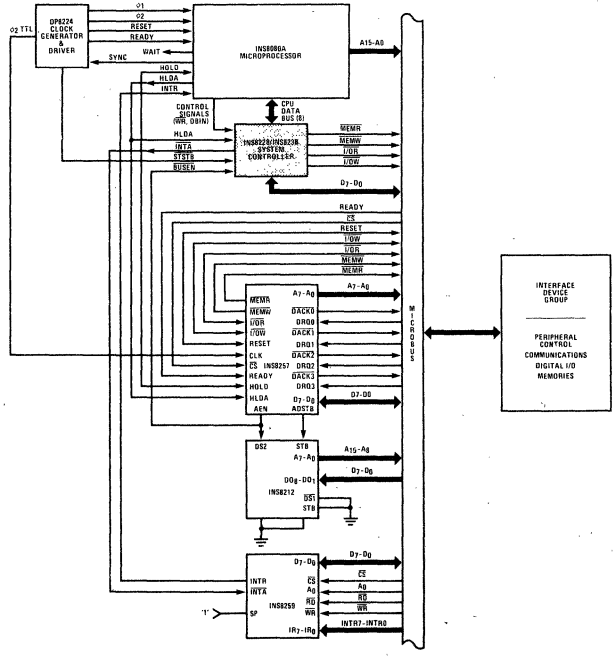
The INS8228/INS8238 is a system controller/bus driver contained in a standard, 28-pin dual-in-line package. The chip, which is fabricated using Schottky Bipolar technology, generates all the read and write control signals required to directly interface the memory and input/output components of National Semiconductor's INS8080A microcomputer family. The chip also provides drive and isolation for the bidirectional data bus of the INS8080A microprocessor. Data bus isolation enables the use of slower memory and input/output components in a system, and provides for enhanced system noise immunity.

A user-selected single-level interrupt vector (RST 7) is provided by the chip for use in the interrupt structure of small systems that need only one basic vector. No additional components (such as an interrupt instruction port) are required to use the single interrupt vector in these systems. The INS8228/INS8238 also generates an Interrupt Acknowledge ($\overline{INTA}$) control signal for each byte of a multibyte CALL instruction when an interrupt is acknowledged by the INS8080A. This feature permits the use of a multilevel priority interrupt structure in large, interrupt-driven systems.

Features

- MICROBUS™* Compatible
- Single Chip System Controller and Bus Driver for INS8080A Microcomputer Systems
- Allows Use of Multibyte CALL Instructions for Interrupt Acknowledge
- Provides User-Selected Single-Level Interrupt Vector (RST 7)
- Provides Isolation for Data Bus
- Supports a Wide Variety of System Bus Structures
- Reduces System Component Count
- INS8238 Provides Advanced Input/Output Write and Memory Write Control Signals for Large System Timing Control

INS8080 Family CPU Group to MICROBUS Configuration



*Trademark, National Semiconductor Corp.

Absolute Maximum Ratings

Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . -65°C to +150°C
Supply Voltage, V_{CC} . . . . . -0.5 V to +7 V
Input Voltage . . . . . -1.5 V to +7 V
Output Current . . . . . 100 mA

DC Electrical Characteristics

T_A = 0°C to +70°C; V_{CC} = 5 V ± 5%.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.[1]	Max.		
V_C	Input Clamp Voltage, All Inputs		0.75	-1.0	V	V_{CC} = 4.75 V; I_C = -5 mA
I_F	Input Load Current					
	$\overline{STSTB}$			500	μA	V_{CC} = 5.25 V
	D_2 & D_6			750	μA	V_F = 0.45 V
	D_0, D_1, D_4, D_5, & D_7			250	μA	
	All Other Inputs			250	μA	
I_R	Input Leakage Current					
	$\overline{STSTB}$			100	μA	V_{CC} = 5.25 V
	DB_0 - DB_7			20	μA	V_R = 5.25 V
	All Other Inputs			100	μA	
V_{TH}	Input Threshold Voltage, All Inputs	0.8		2.0	V	V_{CC} = 5 V
I_{CC}	Power Supply Current		140	190	mA	V_{CC} = 5.25 V
V_{OL}	Output Low Voltage					
	D_0 - D_7			0.45	V	V_{CC} = 4.75 V; I_{OL} = 2 mA
	All Other Outputs			0.45	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage					
	D_0 - D_7	3.6	3.8		V	V_{CC} = 4.75 V; I_{OH} = -10 μA
	All Other Outputs	2.4			V	I_{OH} = -1 mA
I_{OS}	Short Circuit Current, All Outputs	15		90	mA	V_{CC} = 5 V
$I_{O\,(off)}$	Off State Output Current					
	All Control Outputs			100	μA	V_{CC} = 5.25 V; V_O = 5.25 V
				-100	μA	V_O = 0.45 V
I_{INT}	INTA Current			5	mA	(See Test Conditions—Pg. 3)

Notes:
1. Typical values are for T_A = 25°C and nominal supply voltages.

Capacitance

This parameter is periodically sampled and not 100% tested.

Symbol	Parameter	Limits			Units
		Min.	Typ.[1]	Max.	
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

V_{BIAS} = 2.5 V, V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz.

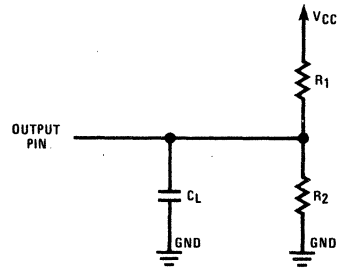
AC Electrical Characteristics

$T_A = 0°C$ to $+70°C$; $V_{CC} = 5\ V \pm 5\%$.

Symbol	Parameter	Limits		Units	Condition
		Min.	Max.		
t_{PW}	Width of Status Strobe	22		ns	
t_{SS}	Setup Time, Status Inputs D_0 - D_7	8		ns	
t_{SH}	Hold Time, Status Inputs D_0 - D_7	5		ns	
t_{DC}	Delay from $\overline{STSTB}$ to any Control Signal	20	60	ns	$C_L = 100$ pF
t_{RR}	Delay from DBIN to Control Outputs		30	ns	$C_L = 100$ pF
t_{RE}	Delay from DBIN to Enable/Disable 8080 Bus		45	ns	$C_L = 25$ pF
t_{RD}	Delay from System Bus to 8080 Bus during Read		30	ns	$C_L = 25$ pF
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	5	45	ns	$C_L = 100$ pF
t_{WE}	Delay to Enable System Bus DB_0 - DB_7 after $\overline{STSTB}$		30	ns	$C_L = 100$ pF
t_{WD}	Delay from 8080 Bus D_0 - D_7 to System Bus DB_0 - DB_7 during Write	5	40	ns	$C_L = 100$ pF
t_E	Delay from System Bus Enable to System Bus DB_0 - DB_7		30	ns	$C_L = 100$ pF
t_{HD}	HLDA to Read Status Outputs		25	ns	$C_L = 100$ pF
t_{DS}	Setup Time, System Bus Inputs to HLDA	10		ns	
t_{DH}	Hold Time, System Bus Inputs to HLDA	20		ns	

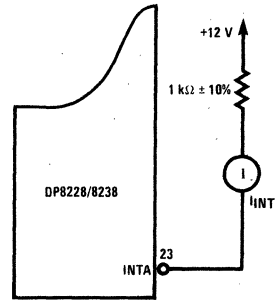
Test Conditions

Test Load[2]



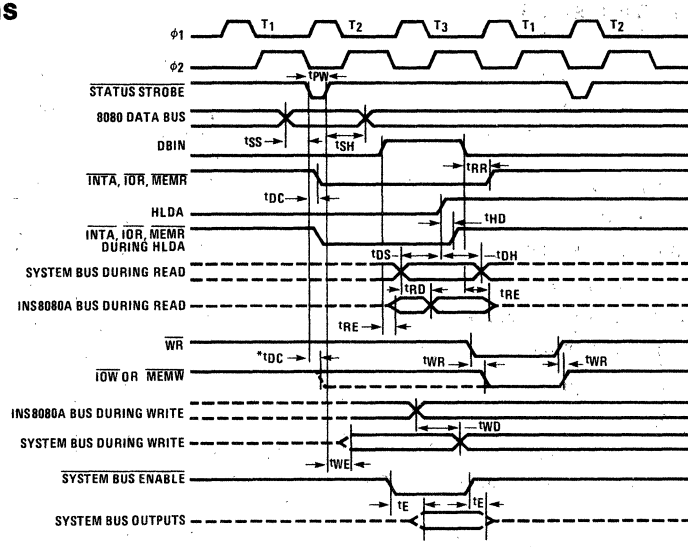
2. For D_0 - D_7: $R_1 = 4\ k\Omega$, $R_2 = \infty$, $C_L = 25$ pF. For all other outputs: $R_1 = 500\ \Omega$, $R_2 = 1\ k\Omega$, $C_L = 100$ pF.

INTA Test Circuit (for RST 7)



D.1

Waveforms



VOLTAGE MEASUREMENT POINTS: D_0 - D_7 (when outputs) Logic "0" = 0.8 V, Logic "1" = 3.0 V. All other signals measured at 1.5 V.

*Advanced $\overline{I/OW}$ $\overline{MEMW}$ for 8238 only.

INS8228/INS8238 Functional Pin Definitions

The following describes the function of all of the INS8228/INS8238 pinouts. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Status Strobe ($\overline{STSTB}$): Activated (low) at the start of each new machine cycle. The $\overline{STSTB}$ input is used to store a status word (refer to chart) from the INS8080A microprocessor into the internal status latch of the INS8228/INS8238. The INS8080A outputs this status word onto its data bus during the first state (SYNC interval) of each machine cycle.

Data Bus In (DBIN): When high, indicates that the INS8080A data bus is in the input mode. The DBIN signal is used to gate data from memory or an input/output device onto the data bus.

Write ($\overline{WR}$): When low, indicates that the data on the INS8080A data bus are stable for WRITE memory or output operation.

Hold Acknowledge (HLDA): When high, indicates that the INS8080A data and address buses will go to their high impedance state. When in the data bus read mode, DBIN input in the high state, a high HLDA input will latch the data bus information into the driver circuits and gate off the applicable control signal $\overline{I/OR}$, $\overline{MEMR}$, or $\overline{INTA}$ (return to the output high state).

Bus Enable ($\overline{BUSEN}$): Asynchronous DMA input to the internal gating array of the INS8228/INS8238. When low, normal operation of the internal bidirectional bus driver and gating array occurs. When high, the bus driver and gating array are driven to their high impedance state.

V_{CC} Supply: +5 volts.

Ground: 0 volt reference.

OUTPUT SIGNALS

Memory Read ($\overline{MEMR}$): When low, signals data to be loaded in from memory. The $\overline{MEMR}$ signal is generated by strobing in status word 1, 2, or 4. (Refer to status word chart.)

Memory Write ($\overline{MEMW}$): When low, signals data to be stored in memory. The $\overline{MEMW}$ signal is generated for the INS8238 by strobing in status word 3 or 5. (Refer to status word chart.) For the INS8228, the $\overline{MEMW}$ signal is generated by gating a low-level $\overline{WR}$ input with the strobed in status word 3 or 5.

Input/Output Read ($\overline{I/OR}$): When low, signals data to be loaded in from an addressed input/output device. The $\overline{I/OR}$ signal is generated by strobing in status word 6.

Input/Output Write ($\overline{I/OW}$): When low, signals data to be transferred to an addressed input/output device. The $\overline{I/OW}$ signal for the INS8238 is generated by strobing in status word 7. For the INS8228 the $\overline{I/OW}$ signal is generated by gating in a low-level $\overline{WR}$ input with the strobed in status word 7.

Interrupt Acknowledge ($\overline{INTA}$): When low, indicates that an interrupt has been acknowledged by the INS8080A microprocessor. The $\overline{INTA}$ signal is generated by strobing in status word 8 or 10.

Single Level Interrupt (RST 7): When the $\overline{INTA}$ output is tied to 12V through a 1 kΩ resistor, strobing in status word 8 or 10 will cause the CPU data bus outputs, when active, to go to the high state.

INPUT/OUTPUT SIGNALS

CPU Data (D_7-D_0) Bus: This bus comprises eight TRI-STATE input/output lines that connect to the INS8080A microprocessor. The bus provides bidirec-

INS8228/INS8238 Functional Pin Definitions (cont'd)

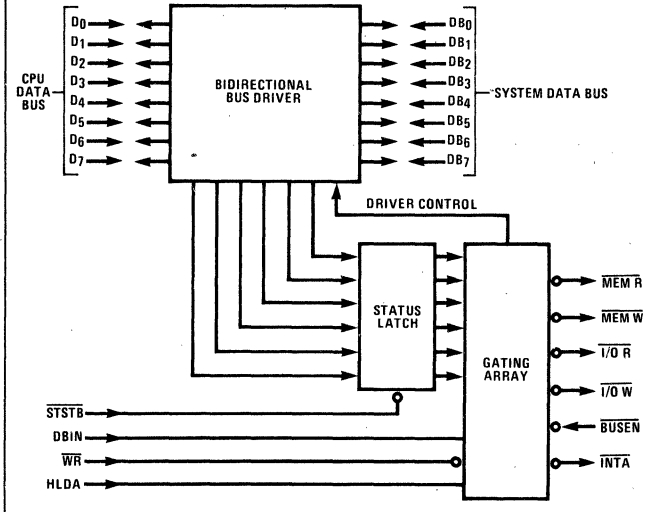
tional communication between the CPU, memory, and input/output devices for instructions and data transfers. A status word (which describes the current machine cycle) is also outputted on this data bus during the first microcycle of each machine cycle (SYNC = logic 1).

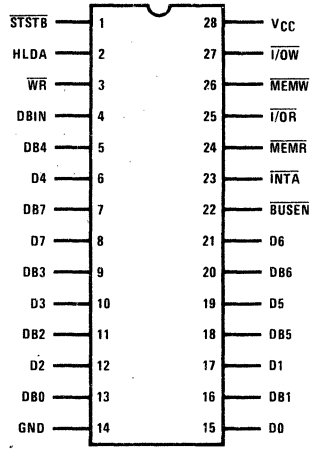
System Data (DB_7-DB_0) Bus: This bus comprises eight TRI-STATE input/output lines that connect to the memory and input/output components of the system. The internal bidirectional bus driver isolates the DB_7-DB_0 Data Bus from the D_7-D_0 Data Bus.

Status Word Chart

Machine Cycle	Status Word	Data Bus Bit								Control Signal
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Instruction Fetch	1	1	0	1	0	0	0	1	0	$\overline{MEMR}$
Memory Read	2	1	0	0	0	0	0	1	0	$\overline{MEMR}$
Memory Write	3	0	0	0	0	0	0	0	0	$\overline{MEMW}$
Stack Read	4	1	0	0	0	0	1	1	0	$\overline{MEMR}$
Stack Write	5	0	0	0	0	0	1	0	0	$\overline{MEMW}$
Input Read	6	0	1	0	0	0	0	1	0	$\overline{I/OR}$
Output Write	7	0	0	0	1	0	0	0	0	$\overline{I/OW}$
Interrupt Acknowledge	8	0	0	1	0	0	0	1	1	$\overline{INTA}$
Halt Acknowledge	9	1	0	0	0	1	0	1	0	(none)
Interrupt Acknowledge While Halt	10	0	0	1	0	1	0	1	1	$\overline{INTA}$

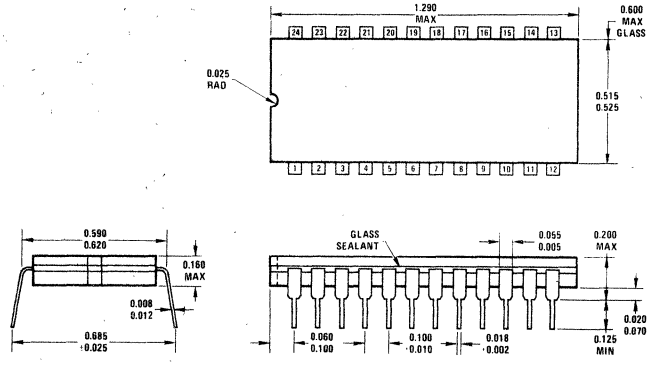
INS8228/INS8238 Block Diagram and Pin Configuration



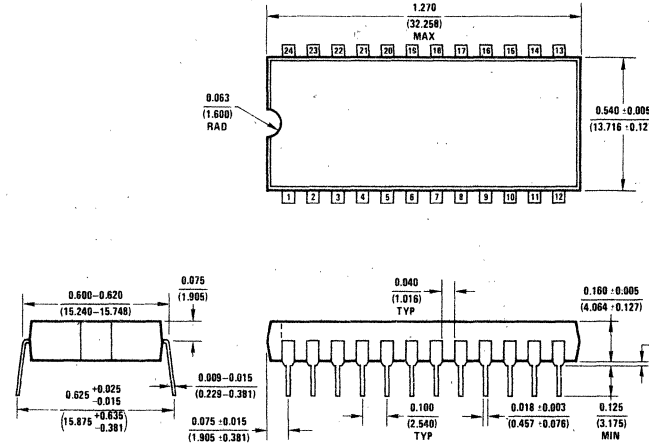


NOTE: INS8228/INS8238 Identical to DP8228/DP8238

Physical Dimensions



Ceramic Dual-in-Line Package (J)
Order Number INS8228J/INS8238J



24-Lead Molded DIP (N)
Order Number INS8228N/INS8238N

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National Semiconductor

JULY 1978

INS8202/8203 TRI-STATE® Octal Buffers

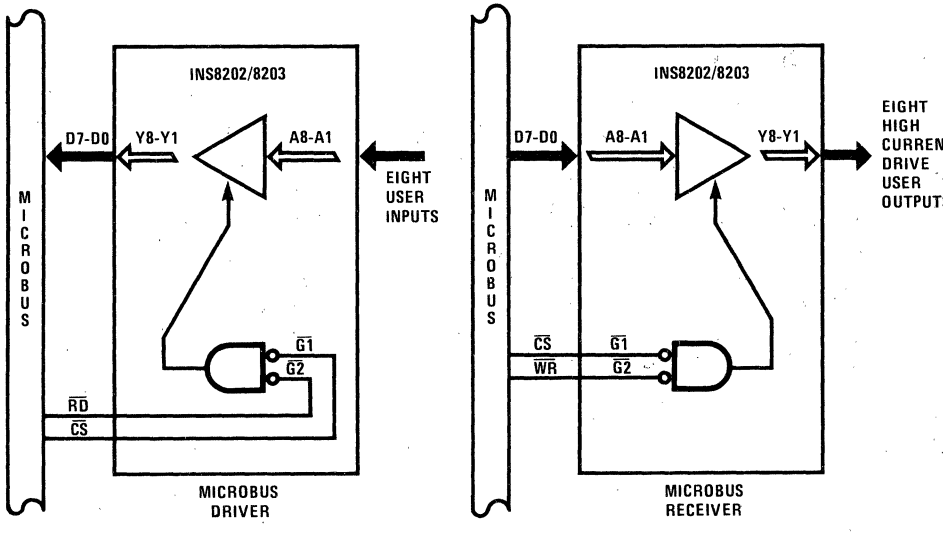
General Description

These devices provide eight two-input buffers in each package. All employ the newest low power Schottky TTL technology. One of the two inputs to each buffer is used as a control line to gate the output into the high-impedance state, while the other input passes the data through the buffer. The INS8202 presents true data at the outputs, while the INS8203 is inverting. All eight TRI-STATE enable lines are common, with access through a 2-input NOR gate. The outputs are placed in the TRI-STATE condition by applying a high logic level to the enable pins. These devices represent octal, low power Schottky versions of the very popular DM8095 and 96 TRI-STATE hex buffers.

Features

- Identical to DM81LS95 and DM81LS96
- Octal versions of popular DM80LS95, 80LS96
- Typical power dissipation
  INS8202 — 80mW
  INS8203 — 65mW
- Typical propagation delay
  INS8202 — 13ns
  INS8203 — 10ns
- Low power Schottky TRI-STATE technology
- MICROBUS™* compatible

INS8202/8203 MICROBUS Configuration



*Trademark, National Semiconductor Corp.

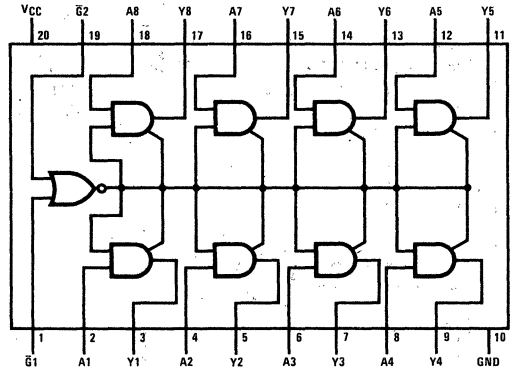
Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

	Parameter		Conditions			INS8202/8203 Min	Typ	Max	Units
V_{IH}	High Level Input Voltage					2			V
V_{IL}	Low Level Input Voltage							0.8	V
V_I	Input Clamp Voltage		V_{CC} = min, I_I = −18mA					−1.5	V
I_{OH}	High Level Output Current							−2.6	mA
V_{OH}	High Level Output Voltage		V_{CC} = min, V_{IH} = 2V, V_{IL} = 0.8V	I_{OH} = max		2.7			V
				I_{OH} = −5mA		2.4			
I_{OL}	Low Level Output Current							16	mA
V_{OL}	Low Level Output Voltage		V_{CC} = min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = max					0.5	V
$I_{O(OFF)}$	Off-State (High-Impedance State) Output Current		V_{CC} = max, V_{IH} = 2V, V_{IL} = 0.8V	V_O = 0.4V				−20	μA
				V_O = 2.4V				20	
I_I	Input Current at Maximum Input Voltage		V_{CC} = max, V_I = 7V					0.1	mA
I_{IH}	High Level Input Current		V_{CC} = max, V_I = 2.7V					20	μA
I_{IL}	Low Level Input Current	A Input	V_{CC} = max	Both G Inputs at 2V	V_I = 0.5V			−20	μA
		G Input		Both G Inputs at 0.4V	V_I = 0.4V			−0.36	mA
					V_I = 0.4V			−0.36	
I_{OS}	Short Circuit Output Current		V_{CC} = max (Note 2)			−30	−60	−130	mA
I_{CC}	Supply Current		V_{CC} = max	INS8202			16	26	mA
				INS8203			13	21	

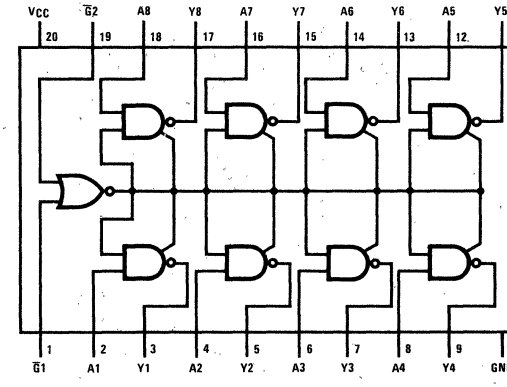
Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

Connection Diagrams



INS8202



INS8203

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Parameter		Conditions	INS8202			INS8203			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15pF, R_L = 2kΩ		11	16		6	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			15	22		13	17	ns
t_{ZH}	Output Enable Time to High Level			16	25		17	27	ns
t_{ZL}	Output Enable Time to Low Level			13	20		16	25	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5pF, R_L = 2kΩ		13	20		13	20	ns
t_{LZ}	Output Disable Time from Low Level			19	27		18	27	ns

Truth Tables

Inputs			Output
$\overline{G1}$	$\overline{G2}$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

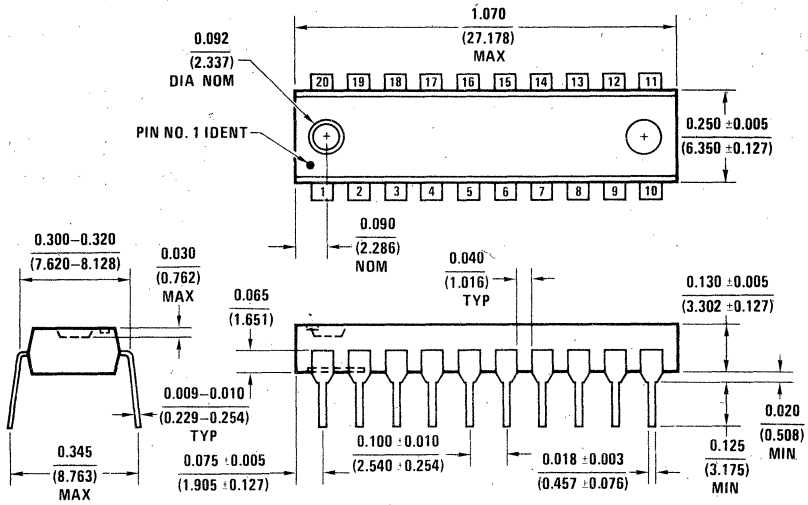
20-Lead Dual-In-Line Package
Order Number INS8202(N)

Inputs			Output
$\overline{G1}$	$\overline{G2}$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

20-Lead Dual-In-Line Package
Order Number INS8203(N)

D.2

Physical Dimensions inches (millimeters)



20-Lead Dual-In-Line Package
Order Number INS8203(N)
NS Package Number N20A

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National Semiconductor

APRIL 1978

INS8208 8-Bit Bidirectional Transceiver

General Description

The INS8208 is an 8-bit TRI-STATE® low power Schottky transceiver. It provides bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with low power Schottky drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

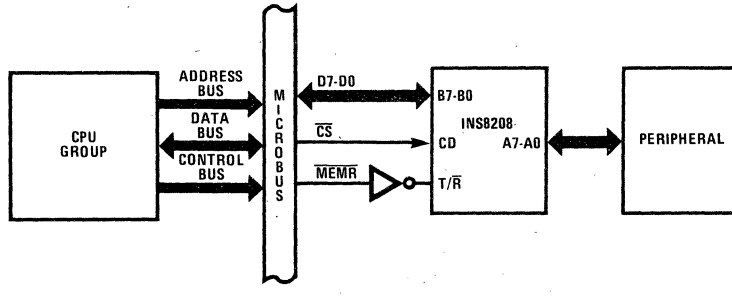
One input, Transmit/Receive, determines the direction of logic signals through the bidirectional transceiver: Transmit enables data from A ports to B ports; Receive enables data from B ports to A ports. The Chip Disable input disables both A and B ports by placing them in a TRI-STATE® condition.

The output high voltage (V_{OH}) is specified at 3.6 V minimum to allow interfacing microprocessors, TTL, MOS, CMOS, RAM, or ROM.

Features

- 8-Bit Bidirectional Data Flow Reduces System Package Count
- Bidirectional TRI-STATE® Inputs/Outputs Interface with Bus-Oriented Systems
- PNP inputs Reduce Input Loading
- 3.6V Output High Voltage Interfaces with TTL, MOS, and CMOS
- 48mA/300pF Bus Drive Capability
- Pinouts Simplify System Interconnections
- Transmit/Receive and Chip Disable Simplify Control Logic
- Compact 20-Pin Dual-In-Line Package
- Low I_{CC} Power (8mA per bidirectional bit)
- MICROBUS™ * Compatible

INS8208 MICROBUS™ Configuration



* Trademark, National Semiconductor Corporation

Absolute Maximum Ratings (Note 1)

Supply Voltage	7 V
Input Voltage	5.5 V
Output Voltage	5.5 V
Storate Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	600 mW

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature (T_A)	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Parameter		Conditions	Limits			Units
Symbol	Description		Min	Typ	Max	
A Port (A0 - A7)						
V_{IH}	Logical "1" Input Voltage	CD = 0.8 V, T/$\overline{R}$ = 2.0 V	2.0			V
V_{IL}	Logical "0" Input Voltage	CD = 0.8 V, T/$\overline{R}$ = 2.0 V			0.8	V
V_{OH}	Logical "1" Output Voltage	CD = 0.8 V, T/$\overline{R}$ = 0.8 V I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.8		V
V_{OL}	Logical "0" Output Voltage	CD = 0.8 V, T/$\overline{R}$ = 0.8 V, I_{OL} = 5 mA		0.3	0.45	V
I_{OS}	Output Short Circuit Current	CD = 0.8 V, T/$\overline{R}$ = 0.8 V, V_O = 0 V, V_{CC} = 5.25 V, Note 4	−10	−22	−75	mA
I_{IH}	Logical "1" Input Current	CD = 0.8 V, T/$\overline{R}$ = 2.0 V, V_{IH} = 2.7 V		1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0 V, V_{CC} = 5.25 V, V_{IH} = 5.25 V			1	mA
I_{IL}	Logical "0" Input Current	CD = 0.8 V, T/$\overline{R}$ = 2.0 V, V_{IL} = 0.4 V		−70	−250	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0 V, I_{IN} = −12 mA		−0.2	−1.5	V
I_{OD}	Output/Input TRI-STATE® Current	CD = 2.0 V, V_{IN} = 0.4 V			−200	μA
		CD = 2.0 V, V_{IN} = 4.0 V			80	μA
B Port (B0 - B7)						
V_{IH}	Logical "1" Input Voltage	CD = 0.8 V, T/$\overline{R}$ = 0.8 V	2.0			V
V_{IL}	Logical "0" Input Voltage	CD = 0.8 V, T/$\overline{R}$ = 0.8 V			0.8	V
V_{OH}	Logical "1" Output Voltage	CD = 0.8 V, T/$\overline{R}$ = 2.0 V, I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.8		V
		CD = 0.8 V, T/$\overline{R}$ = 2.0 V, I_{OH} = −5 mA	2.7	3.6		V
		CD = 0.8 V, T/$\overline{R}$ = 2.0 V, I_{OH} = −10 mA	2.4	3.3		V
V_{OL}	Logical "0" Output Voltage	CD = 0.8 V, T/$\overline{R}$ = 2.0 V, I_{OL} = 20 mA		0.3	0.4	V
		CD = 0.8 V, T/$\overline{R}$ = 2.0 V, I_{OL} = 48 mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	CD = 0.8 V, T/$\overline{R}$ = 2.0 V, V_O = 0 V, V_{CC} = 5.25 V, Note 4		−35	−150	mA
I_{IH}	Logical "1" Input Current	CD = 0.8 V, T/$\overline{R}$ = 0.8 V, V_{IH} = 2.7 V		1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0 V, V_{CC} = 5.25 V, V_{IH} = 5.25 V			1	mA
I_{IL}	Logical "0" Input Current	CD = 0.8 V, T/$\overline{R}$ = 0.8 V, V_{IL} = 0.4 V		−12	−250	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0 V, I_{IN} = −12 mA		−0.3	−1.5	V
I_{OD}	Output/Input TRI-STATE® Current	CD = 2.0 V, V_{IN} = 0.4 V			−200	μA
		CD = 2.0 V, V_{IN} = 4.0 V			+200	μA

DC Electrical Characteristics continued (Notes 2 and 3)

Parameter		Conditions		Limits			Units
Symbol	Description			Min	Typ	Max	
Control Inputs CD, T/$\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7 V			0.5	20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.25 V, V_{IH} = 5.25 V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4 V	T/$\overline{R}$		0.23	0.4	mA
			CD		0.45	0.8	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA			−0.8	−1.5	V
Power Supply Current							
I_{CC}	Power Supply Current	CD = 2.0 V, V_{CC} = 5.25 V, V_{IN} = 0.4 V			65	100	mA

AC Electrical Characteristics V_{CC} = 5 V, T_A = 25°C

Parameter		Conditions	Min	Typ	Max	Units
A Port Data/Mode Specifications						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4 V, T/$\overline{R}$ = 0.4 V (figure A) R1 = 1k, R2 = 5k, C1 = 30 pF		24	40	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4 V, T/$\overline{R}$ = 0.4 V (figure A) R1 = 1k, R2 = 5k, C1 = 30 pF		11	20	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE® from CD to A Port	B0 to B7 = 0.4 V, T/$\overline{R}$ = 0.4 V (figure C) S_3 = 1, R5 = 1k, C4 = 15 pF		12	18	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE® from CD to A Port	B0 to B7 = 2.4 V, T/$\overline{R}$ = 0.4 V (figure C) S_3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE® to a Logical "0" from CD to A Port	B0 to B7 = 0.4 V, T/$\overline{R}$ = 0.4 V (figure C) S_3 = 1, R5 = 1k, C4 = 30 pF		32	50	ns
t_{PZHA}	Propagation Delay from TRI-STATE® to a Logical "1" from CD to A Port	B0 to B7 = 2.4 V, T/$\overline{R}$ = 0.4 V (figure C) S_3 = 0, R5 = 5k, C4 = 30 pF		16	25	ns
B Port Data/Mode Specifications						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4 V, T/$\overline{R}$ = 2.4 V (figure A) R1 = 100 Ω, R2 = 1k, C1 = 300 pF		17	27	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4 V, T/$\overline{R}$ = 2.4 V (figure A) R1 = 100 Ω, R2 = 1k, C1 = 300 pF		15	23	ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE® from CD to B Port	A0 to A7 = 0.4 V, T/$\overline{R}$ = 2.4 V (figure C) S_3 = 1, R5 = 1k, C4 = 15 pF		25	40	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE® from CD to B Port	A0 to A7 = 2.4 V, T/$\overline{R}$ = 2.4 V (figure C) S_3 = 0, R5 = 1k, C4 = 15 pF		16	25	ns
t_{PZLB}	Propagation Delay from TRI-STATE® to a Logical "0" from CD to B Port	A0 to A7 = 0.4 V, T/$\overline{R}$ = 2.4 V (figure C) S_3 = 1, R5 = 100 Ω, C4 = 300 pF		33	50	ns
t_{PZHB}	Propagation Delay from TRI-STATE® to a Logical "1" from CD to B Port	A0 to A7 = 2.4 V, T/$\overline{R}$ = 2.4 V (figure C) S_3 = 0, R5 = 1k, C4 = 300 pF		16	25	ns

AC Electrical Characteristics continued $V_{CC} = 5\,V$, $T_A = 25°C$

Parameter		Conditions	Min	Typ	Max	Units
Transmit/Receive Mode Specifications						
t_{PHZR}	Propagation Delay from a Logical "1" to TRI-STATE® from T/$\overline{R}$ to A Port	CD = 0.4 V (figure B) S_1 = 1, R4 = 100 Ω, C3 = 300 pF S_2 = 0, R3 = 1k, C2 = 15 pF		14	22	ns
t_{PLZR}	Propagation Delay from a Logical "0" to TRI-STATE® from T/$\overline{R}$ to A Port	CD = 0.4 V (figure B) S_1 = 0, R4 = 1k, C3 = 300 pF S_2 = 1, R3 = 1k, C2 = 15 pF		20	30	ns
t_{PHZT}	Propagation Delay from a Logical "1" to TRI-STATE® from T/$\overline{R}$ to B Port	CD = 0.4 V (figure B) S_1 = 0, R4 = 1k, C3 = 15 pF S_2 = 1, R3 = 5k, C2 = 30 pF		22	33	ns
t_{PLZT}	Propagation Delay from a Logical "0" to TRI-STATE® from T/$\overline{R}$ to B Port	CD = 0.4 V (figure B) S_1 = 1, R4 = 1k, C3 = 15 pF S_2 = 0, R3 = 1k, C2 = 30 pF		34	50	ns
t_{PRL}	Propagation Delay from Transmit Mode to a Logical "0," T/$\overline{R}$ to A Port	$t_{PRL} = t_{PHZT} + t_{PDHLA}$		46	70	ns
t_{PRH}	Propagation Delay from Transmit Mode to a Logical "1," T/$\overline{R}$ to A Port	$t_{PRH} = t_{PLZT} + t_{PDLHA}$		45	70	ns
t_{PTL}	Propagation Delay from Receive Mode to a Logical "0," T/$\overline{R}$ to B Port	$t_{PTL} = t_{PHZR} + t_{PDHLB}$		31	50	ns
t_{PTH}	Propagation Delay from Receive Mode to a Logical "1," T/$\overline{R}$ to B Port	$t_{PTH} = t_{PLZR} + t_{PDLHB}$		35	50	ns

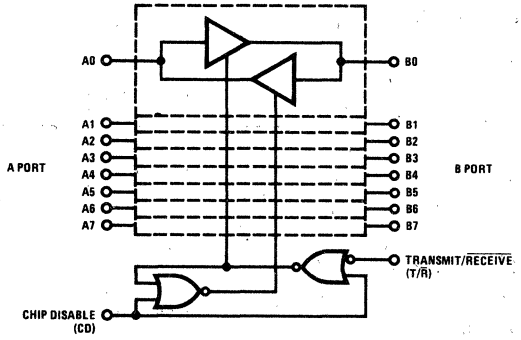
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75 V to 5.25 V power supply range. All typical values given are for $V_{CC} = 5\,V$ and $T_A = 25°C$.

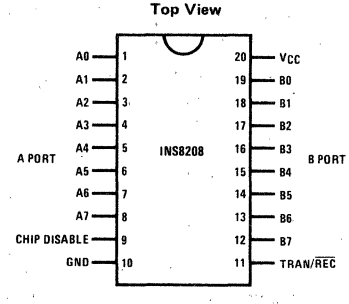
Note 3: All Currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Logic and Connection Diagrams



Top View



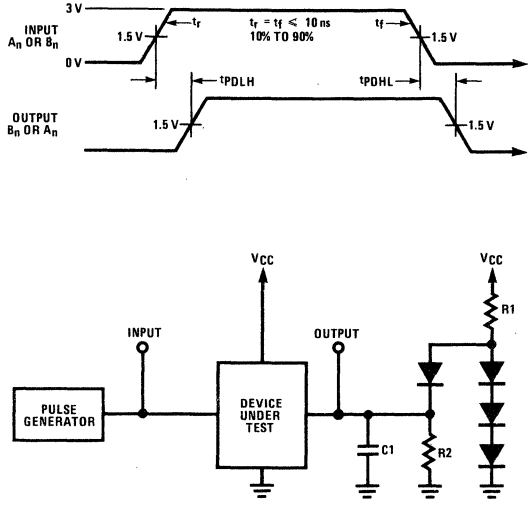
Logic Table

Inputs		Resulting Conditions	
Chip Disable	Transmit/Receive	A Port	B Port
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't Care

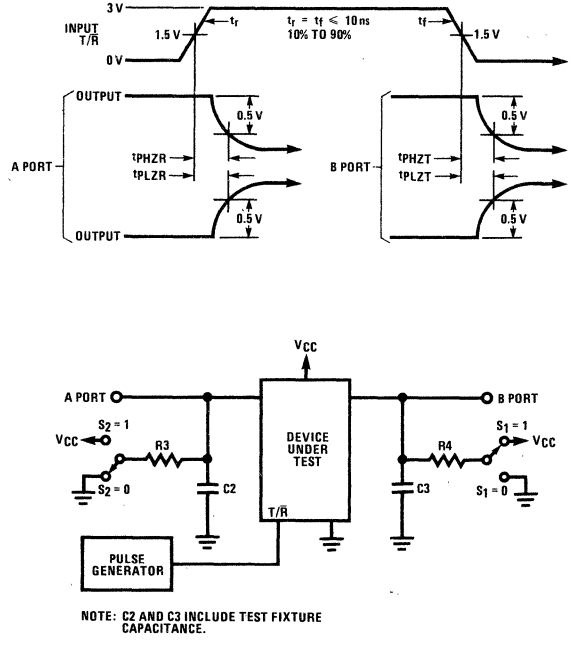
Note: INS8208 is identical to the DP8304

Switching Time Waveforms and AC Test Circuits



NOTE: C1 INCLUDES TEST FIXTURE CAPACITANCE.

FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port



NOTE: C2 AND C3 INCLUDE TEST FIXTURE CAPACITANCE.

FIGURE B. Propagation Delay from T/$\overline{R}$ to A Port or B Port

D.2

National Semiconductor

APRIL 1978

INS8212 8-Bit Input/Output Port

General Description

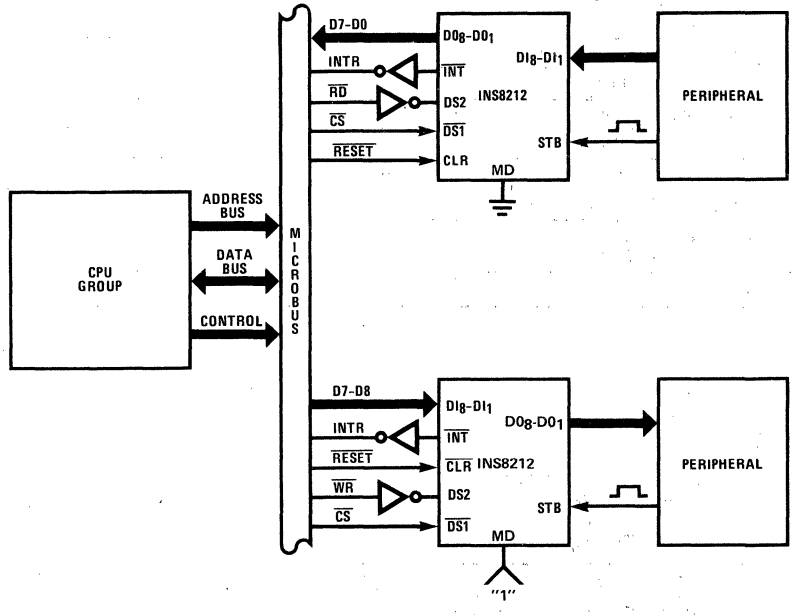
The INS8212 is an 8-bit input/output port contained in a standard 24-pin dual-in-line package. The device, which is fabricated using Schottky Bipolar technology, is part of National Semiconductor's INS8080A microprocessor family. The INS8212 can be used to implement latches, gated buffers, or multiplexers. Thus, all of the major peripheral and input/output functions of a microcomputer system can be implemented with this device.

The INS8212 includes an 8-bit latch with TRI-STATE® output buffers, and device selection and control logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

Features

- 8-Bit Data Latch and Buffer
- Service Request Flip-Flop for Generation and Control of Interrupts
- 0.25 mA Input Load Current
- TRI-STATE TTL Output Drive Capability
- Outputs Sink 15 mA
- Asynchronous Latch Clear
- 3.65V Output for Direct Interface to INS8080A
- Reduces System Package Count by Replacing Buffers, Latches, and Multiplexers in Microcomputer Systems
- MICROBUS™* Compatible

INS8212 MICROBUS Configuration



*Trademark, National Semiconductor Corp.

Absolute Maximum Ratings

Temperature Under Bias Plastic . . . . . −65°C to +75°C
Storage Temperature . . . . . −65°C to +160°C
All Output or Supply Voltages. . . . . −0.5V to +7V
All Input Voltages. . . . . −1.0V to 5.5V
Output Currents 125mA

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

DC Electrical Characteristics

$T_A = 0°C$ to $+75°C$, $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Load Current STB, DS_2, $\overline{CLR}$, DI_1-DI_8 Inputs			−0.25	mA	$V_F = 0.45V$
I_F	Input Load Current MD Input			−0.75	mA	$V_F = 0.45V$
I_F	Input Load Current $\overline{DS_1}$ Input			−1.0	mA	$V_F = 0.45V$
I_R	Input Leakage Current STB, DS_2, $\overline{CLR}$, DI_1-DI_8 Inputs			10	μA	$V_R = 5.25V$
I_R	Input Leakage Current MD Input			30	μA	$V_R = 5.25V$
I_R	Input Leakage Current $\overline{DS_1}$ Input			40	μA	$V_R = 5.25V$
V_C	Input Forward Voltage Clamp			−1	V	$I_C = -5mA$
V_{IL}	Input "Low" Voltage			0.85	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			0.45	V	$I_{OL} = 15mA$
V_{OH}	Output "High" Voltage	3.65	4.0		V	$I_{OH} = -1mA$
I_{SC}	Short Circuit Output Current	−15		−75	mA	$V_O = 0V$
$\|I_O\|$	Output Leakage Current High Impedance State			20	μA	$V_O = 0.45V/5.25V$
I_{CC}	Power Supply Current		90	130	mA	

Capacitance*

$F = 1MHz$, $V_{BIAS} = 2.5V$, $V_{CC} = +5V$, $T_A = 25°C$

Symbol	Test	Limits	
		Typ.	Max.
C_{IN}	DS_1, MD Input Capacitance	9pF	12pF
C_{IN}	DS_2, $\overline{CLR}$, STB, DI_1-DI_8 Input Capacitance	5pF	9pF
C_{OUT}	DO_1-DO_8 Output Capacitance	8pF	12pF

*This parameter is sampled and not 100% tested.

AC Electrical Characteristics

$T_A = 0°C$ to $+75°C$, $V_{CC} = +5V \pm 5\%$

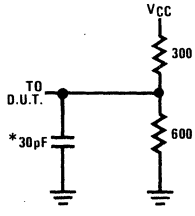
Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
t_{PW}	Pulse Width	30			ns	
t_{PD}	Data to Output Delay			30	ns	
t_{WE}	Write Enable to Output Delay			40	ns	
t_{SET}	Data Setup Time	15			ns	
t_H	Data Hold Time	20			ns	
t_R	Reset to Output Delay			40	ns	
t_S	Set to Output Delay			30	ns	
t_E	Output Enable/Disable Time			45	ns	
t_C	Clear to Output Delay			55	ns	

Switching Characteristics

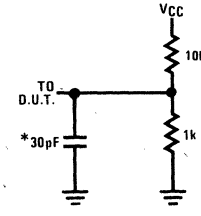
Conditions of Test:

1. Input Pulse Amplitude = 2.5V.
2. Input Rise and Fall Times = 5ns.
3. Between 1V and 2V Measurements made at 1.5V with 15mA & 30pF Test Load.

Test Load
15mA & 30pF



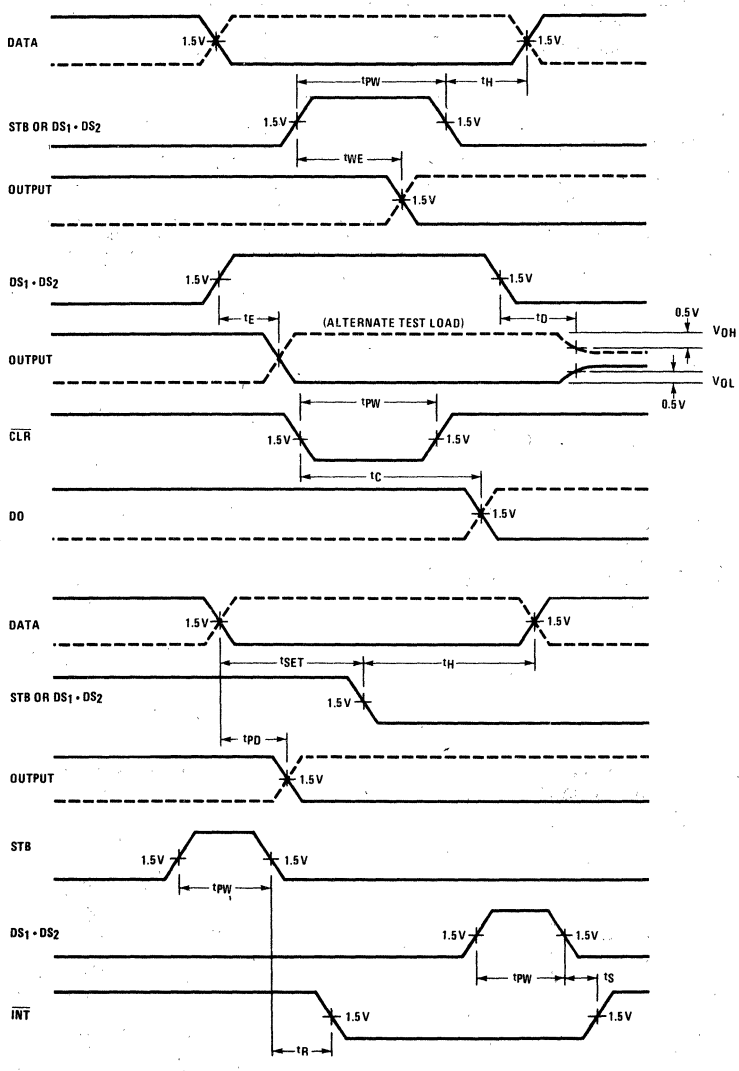
Alternate Test Load



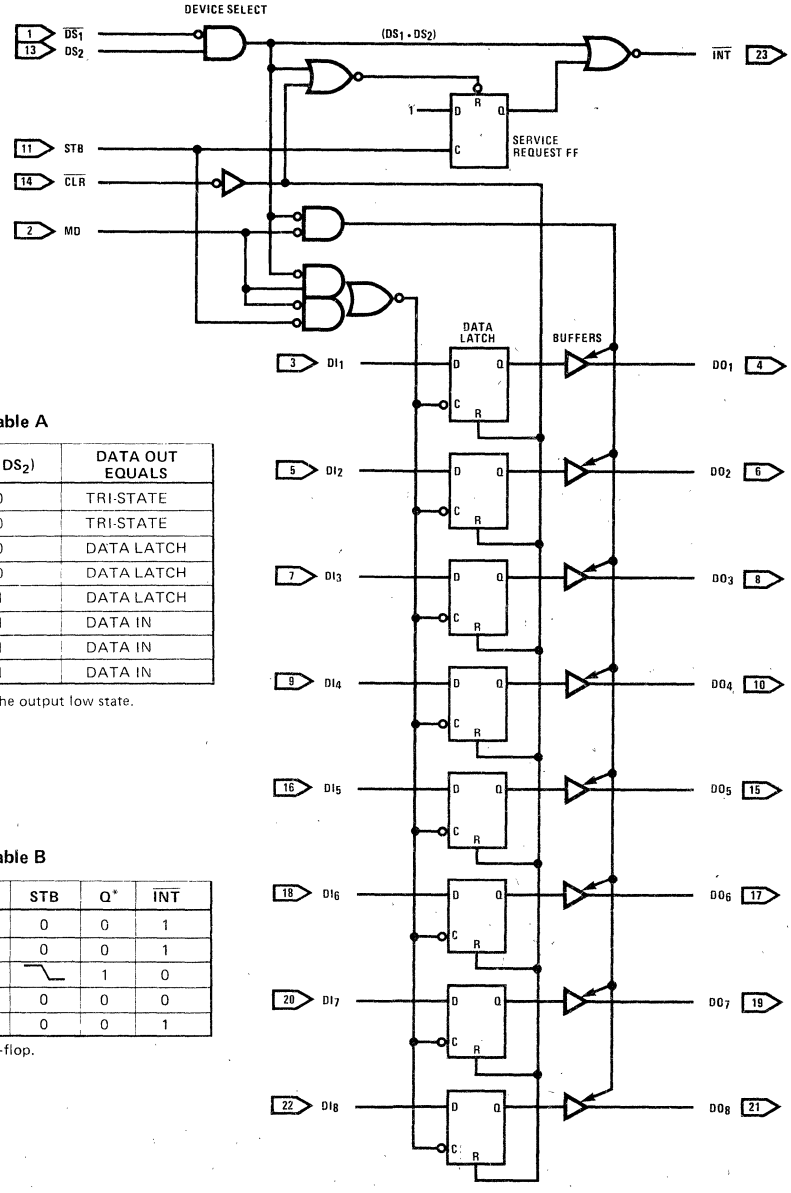
*including jig & probe capacitance

D.2

Timing Diagram



INS8212 Logic Diagram



Logic Table A

STB	MD	$(DS_1 \cdot DS_2)$	DATA OUT EQUALS
0	0	0	TRI-STATE
1	0	0	TRI-STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

$\overline{CLR}$ ⌥ resets data latch to the output low state.

Logic Table B

$\overline{CLR}$	$(DS_1 \cdot DS_2)$	STB	Q*	$\overline{INT}$
0 RESET	0	0	0	1
1	0	0	0	1
1	0	⌥	1	0
1	1 RESET	0	0	0
1	0	0	0	1

*Internal Service Request flip-flop.

INS8212 Functional Pin Definitions

The following describes the function of all the INS8212 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Device Select (DS_1, DS_2): When DS_1 is low and DS_2 is high, the device is selected. The output buffers are enabled and the service request flip-flop is asynchronously reset (cleared) when the device is selected.

Mode (MD): When high (output mode), the output buffers are enabled and the source of the data latch clock input is the device selection logic $(DS_1 \cdot DS_2)$. When low (input mode), the state of the output buffers is determined by the device selection logic $(DS_1 \cdot DS_2)$ and the source of the data latch clock input is the strobe (STB) input.

D.2

INS8212 Functional Pin Definitions continued

Strobe (STB): Used as data latch clock input when the mode (MD) input is low (input mode). Also used to synchronously set the service request flip-flop, which is negative edge triggered.

Data In (DI_1-DI_8): Eight-bit data input to the data latch, which consists of eight D-type flip-flops. While the data latch clock input is high, the Q output of each flip-flop follows the data input. When the clock input returns low, the data latch stores the data input. The clock input high overrides the clear (CLR) input data latch reset.

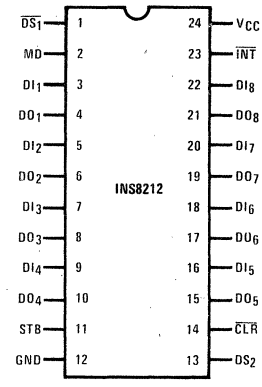
Clear (CLR): When low, asynchronously resets (clears) the data latch and the service request flip-flop. The service request flip-flop is in the non-interrupting state when reset.

OUTPUT SIGNALS

Interrupt (INT): Goes low (interrupting state) when either the service request flip-flop is synchronously set by the strobe (STB) input or the device is selected.

Data Out (DO_1-DO_8): Eight-bit data output of data buffers, which are TRI-STATE, non-inverting stages. These buffers have a common control line that either enables the buffers to transmit the data from the data latch outputs or disables the buffers by placing them in the high-impedance state.

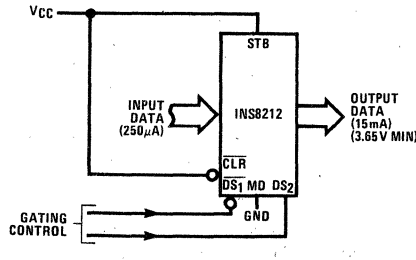
Pin Configuration



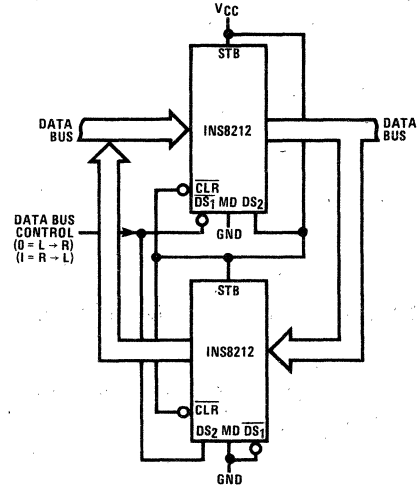
NOTE: INS8212 Identical to DP8212

Applications in Microcomputer Systems

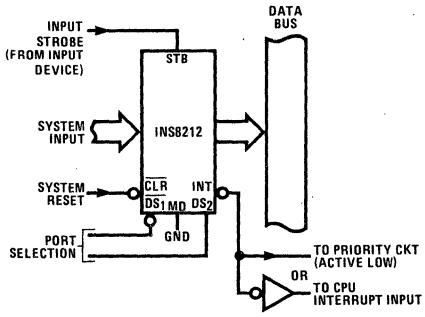
Gated Buffer
(TRI-STATE)



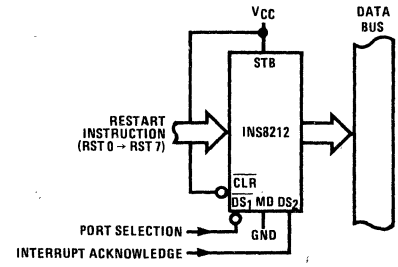
Bidirectional Bus Driver



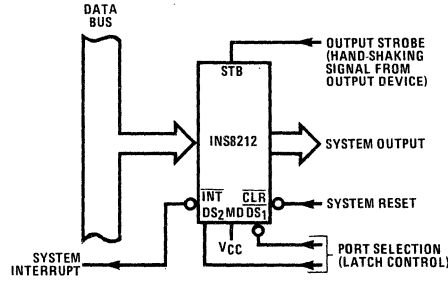
Interrupting Input Port



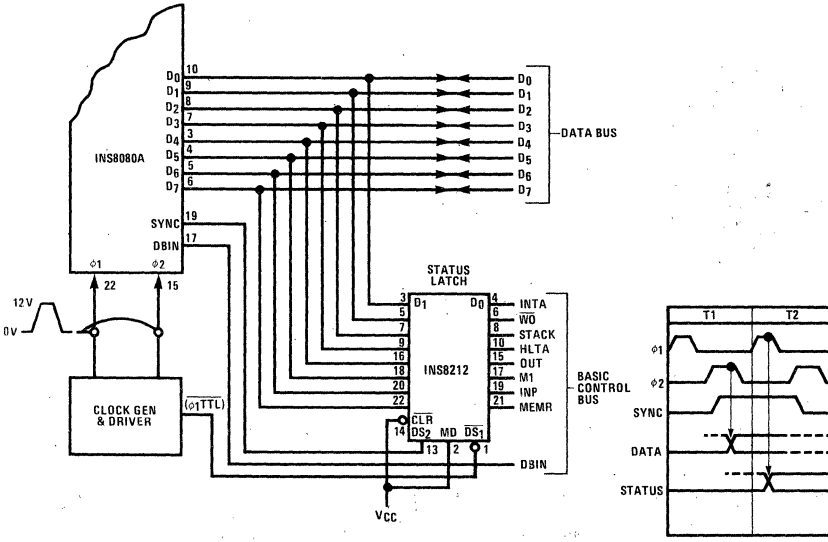
Interrupt Instruction Port



Output Port (with Hand-Shaking)

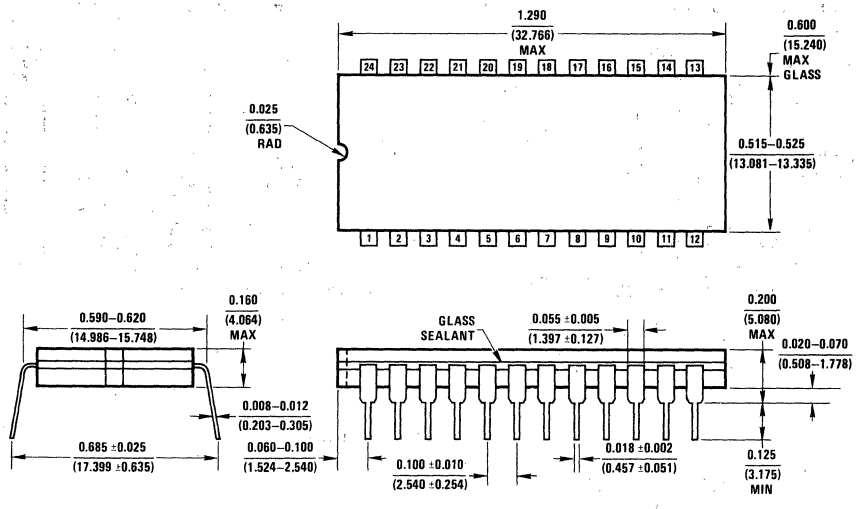


INS8080A Status Latch

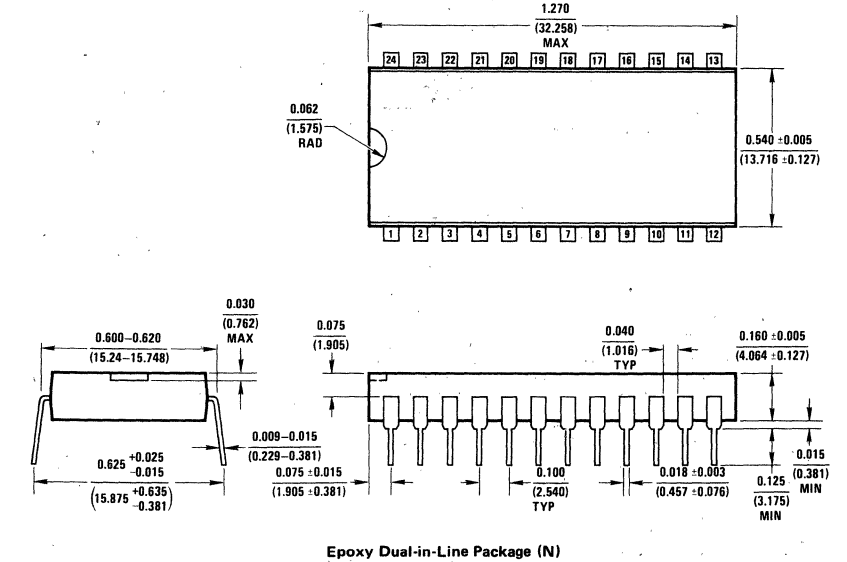


D.2

Physical Dimensions



Ceramic Dual-in-Line Package (J)
Order Number INS8212J



Epoxy Dual-in-Line Package (N)
Order Number INS8212N

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National Semiconductor

AUGUST 1978

INS8216/8226 4-Bit Bidirectional Bus Transceivers

General Description

The INS8216 and INS8226 are four-bit bidirectional bus drivers for use in bus oriented applications. The non-inverting INS8216 and inverting INS8226 drivers are provided for flexibility in system design.

Each buffered line of the four-bit driver consists of two separate buffers that are TRI-STATE® to achieve direct bus interface and bidirectional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB); this side is used to interface to the system side components such as memories, I/O, etc., because its interface is TTL compatible and it has high drive (50mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bidirectional bus. The DO outputs on this side of the driver have a special high voltage output drive capability so that direct interface to the 8080 type CPUs is achieved with an adequate amount of noise immunity.

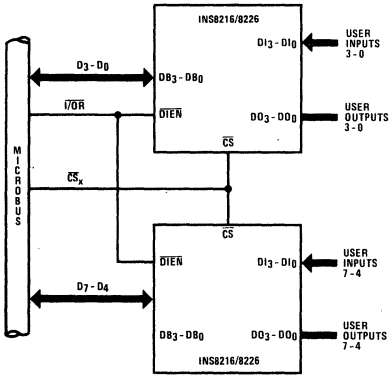
The $\overline{CS}$ input is a device enable. When it is "high" the output drivers are all forced to their high-impedance state. When it is a "low" the device is enabled and the direction of the data flow is determined by the $\overline{DIEN}$ input.

The $\overline{DIEN}$ input controls the direction of data flow, which is accomplished by forcing one of the pair of buffers into its high-impedance state and allowing the other to transmit its data. A simple two-gate circuit is used for this function.

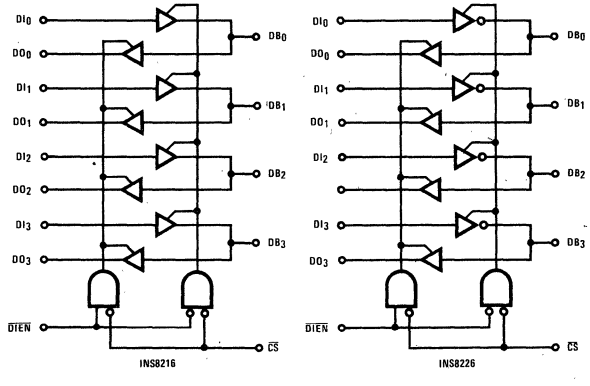
Features

- Data bus buffer driver for 8080 type CPUs
- Low input load current — 0.25mA maximum
- High output drive capability for driving system data bus — 50mA at 0.5V
- Power up-down protection
- The INS8216 has non-inverting outputs.
- The INS8226 has inverting outputs.
- Output high voltage compatible with direct interface to MOS
- TRI-STATE outputs
- Advanced Schottky processing
- Available in military and commercial temperature ranges
- MICROBUS™* compatible

INS8216/8226 MICROBUS Configuration



Logic Diagrams



*Trademark, National Semiconductor Corp.

Absolute Maximum Ratings (Note 1)

	Min	Max	Units
All Output and Supply Voltages	−0.5	+7.0	V
All Input Voltages	−1.0	+5.5	V
Output Currents		125	mA
Lead Temperature (soldering, 10 seconds)		+300	°C
Storage Temperature	−65	+150	°C
Power Dissipation*			
Cavity Package		1160	mW
Molded Package		1000	mW

*Derate Cavity Package at 80°C/W above 70°C; derate Molded Package at 90°C/W above 70°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
INS8216, INS8226	4.75	5.25	V
Temperature, T_A			
INS8216, INS8226	0	+70	°C

DC Electrical Characteristics V_{CC} = 5V ± 5% (Notes 2, 3, and 4)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
DRIVERS						
V_{IL}	Input Low Voltage				0.95	V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	V_F = 0.45V		−0.03	−0.25	mA
I_R	Input Leakage Current	V_R = 5.25V			10	μA
V_C	Input Clamp Voltage	I_C = −5mA			−1.2	V
V_{OL1}	Output Low Voltage	I_{OL} = 25mA		0.3	0.45	V
V_{OL2}	Output Low Voltage	INS8216 — I_{OL} = 55mA INS8226 — I_{OL} = 50mA		0.5	0.6	V
V_{OH}	Output High Voltage	I_{OH} = −10mA	2.4	3.0		V
I_{SC}	Output Short Circuit Current	V_{CC} = 5.0V	−30	−75	−120	mA
$\|I_O\|$	Output Leakage Current TRI-STATE	V_O = 0.45V/5.5V			100	μA
RECEIVERS						
V_{IL}	Input Low Voltage				0.95	V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	V_F = 0.45V		−0.08	−0.25	mA
V_C	Input Clamp Voltage	I_C = −5mA			−1.2	V
V_{OL}	Output Low Voltage	I_{OL} = 15mA		0.3	0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −1mA	3.65	4.0		V
I_{SC}	Output Short Circuit Current	$V_O \approx 0V$	−15	−35	−65	mA
$\|I_O\|$	Output Leakage Current TRI-STATE	V_O = 0.45V/5.5V			20	μA
CONTROL INPUTS ($\overline{CS}$, $\overline{DIEN}$)						
V_{IL}	Input Low Voltage				0.95	V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	V_F = 0.45V		−0.15	−0.5	mA
I_R	Input Leakage Current	V_R = 5.25V			20	μA
I_{CC}	Power Supply Current					
	INS8216			95	130	mA
	INS8226			85	120	mA

AC Electrical Characteristics (Notes 2, 3, and 4)

Symbol	Parameter	Conditions	Limits Min	Limits Typ	Limits Max	Units
INS8216/8226 — V_{CC} = 5.0V ± 5%						
t_{PD1}	Input to Output Delay, DO Outputs	C_L = 30pF, R_1 = 300Ω, R_2 = 600Ω		15	25	ns
t_{PD2}	Input to Output Delay, DB Outputs	C_L = 300pF, R_2 = 90Ω, R_2 = 180Ω				
	INS8216			20	30	ns
	INS8226			16	25	ns
t_E	Output Enable Time	DO Outputs: C_L = 30pF, R_1 = 300Ω/10kΩ, R_2 = 600Ω/1kΩ DB Outputs: C_L = 300pF, R_1 = 90Ω/10kΩ, R_2 = 180Ω/1kΩ				
	INS8216			45	65	ns
	INS8226			35	54	ns
t_D	Output Disable Time	C_L = 5pF, R_1 = 300Ω/10kΩ, R_2 = 600Ω/1kΩ DB Outputs: C_L = 5pF, R_1 = 90Ω/10kΩ, R_2 = 180Ω/1kΩ		20	35	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range for the INS8216 and INS8226. All typical values are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Capacitance T_A = 25°C

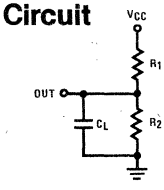
Symbol	Parameter	Limit Min	Limit Typ	Limit Max	Units
C_{IN}	Input Capacitance		4	6	pF
C_{OUT}	Output Capacitance				
	DO Outputs		6	10	pF
	DB Outputs		13	18	pF

Note: This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1MHz, V_{BIAS} = 2.5V, V_{CC} = 5.0V, and T_A = 25°C.

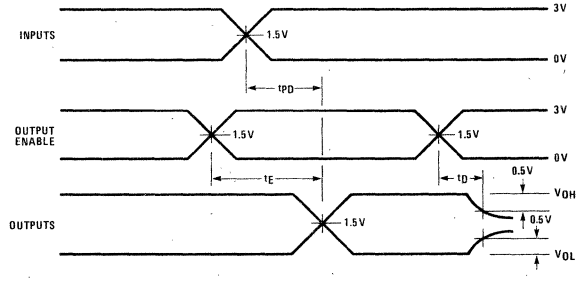
Test Conditions

Input pulse amplitude of 2.5V.
Input rise and fall times of 5.0ns between 1.0V and 2.0V.
Output loading is 5.0mA and 10pF.
Speed measurements are made at 1.5V levels.

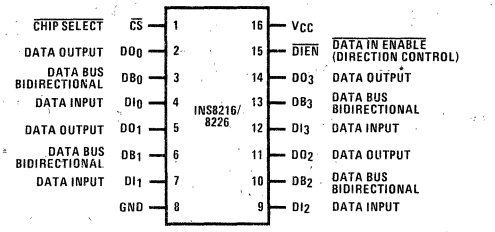
Test Load Circuit



Switching Time Waveforms



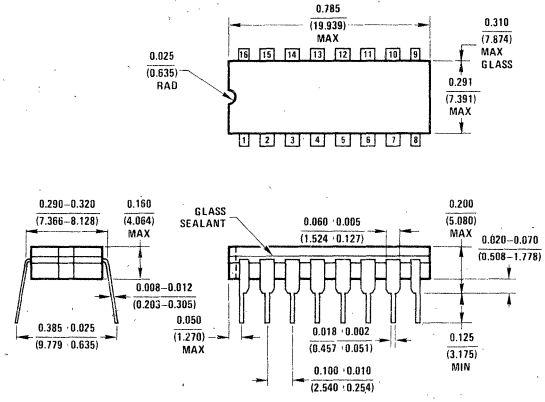
Pin Configuration



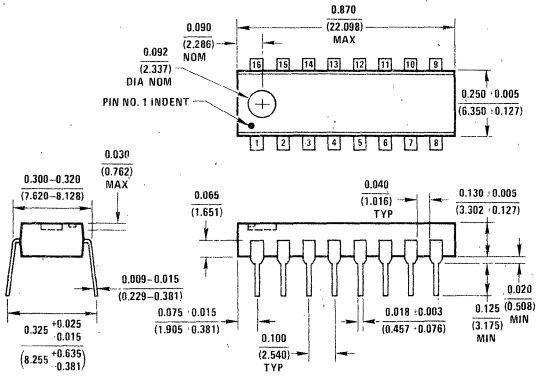
NOTE: THE INS8216/8226 ARE IDENTICAL TO THE DP8216/6226.

Physical Dimensions

inches (millimeters)



16-Lead Cavity DIP (J)
Order Numbers INS8216J, INS8226J
NS Package Number J16A



16-Lead Molded DIP (N)
Order Numbers INS8216N, INS8226N
NS Package Number N16A

Note: The INS8216/8226 are identical to the DP8216/8226.

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National Semiconductor

APRIL 1978

INS8255 Programmable Peripheral Interface

General Description

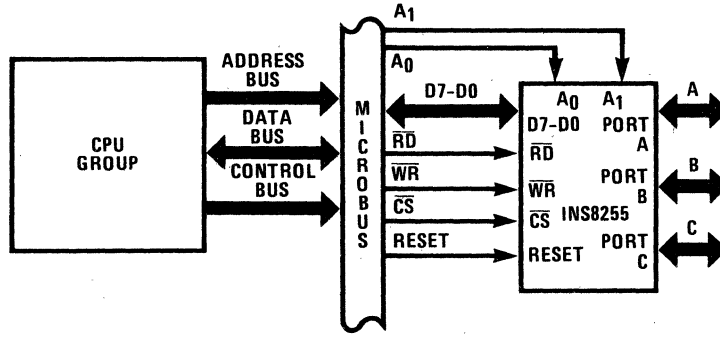
The INS8255 is a programmable peripheral interface contained in a standard, 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, functions as a general-purpose parallel input/output interface in National Semiconductor's N8080 microcomputer family. The functional configuration of the INS8255 is programmed by the system software so that normally no external logic is required to interface peripheral devices.

The INS8255 has three basic modes of operation that can be selected by the system software. In the first mode (Mode 0), the INS8255 provides simple input and output operations for three 8-bit ports. Data is simply written to or read from a specified port (Port A, B or C) without the use of "handshaking" signals. In the second mode (Mode 1), the INS8255 enables the transfer of input/output data to or from a specified 8-bit port (Port A or B) in conjunction with strobes or "handshaking" signals. Ports A and B use the lines of Port C in this mode to generate or accept the "handshaking" signals with the peripheral device. In the third mode (Mode 2), the INS8255 enables communications with a peripheral device or structure via one bidirectional 8-bit bus port (Port A). "Handshaking" signals are provided over the lines of Port C in this mode to maintain proper bus flow discipline.

Features

- Outputs Source 1 mA at 1.5 Volts
- 24 Programmable Input/Output Pins
- Direct Bit Set/Reset Capability
- TTL Compatible
- Reduces System Component Count
- MICROBUS™* Compatible

INS8255 MICROBUS Configuration



Typical Diagram of MODE 0 operation. The 8 bit ports A, B, C are defined by the user's program to be either an input or an output from/to the peripherals.

*Trademark, National Semiconductor Corp.

DC Electrical Characteristics

$T_A = 0°C$ to $+70°C$; $V_{CC} = +5\,V \pm 5\%$; $V_{SS} = 0\,V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 1.6\,mA$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -50\,\mu A$ ($-100\,\mu A$ for D.B. Port)
I_{OH}[1]	Darlington Drive Current		2.0		mA	$V_{OH} = 1.5\,V$, $R_{EXT} = 390\,\Omega$
I_{CC}	Power Supply Current		40		mA	

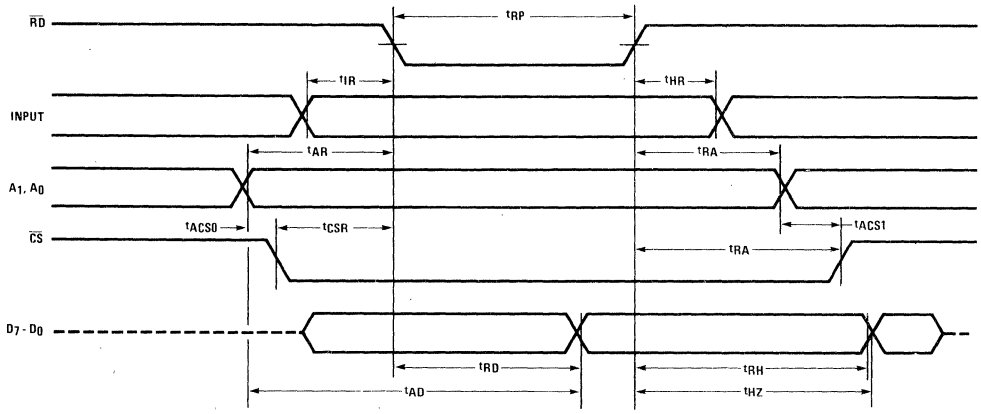
NOTE:
1. Available on 8 pins only of ports B and C. Selected randomly.

AC Electrical Characteristics

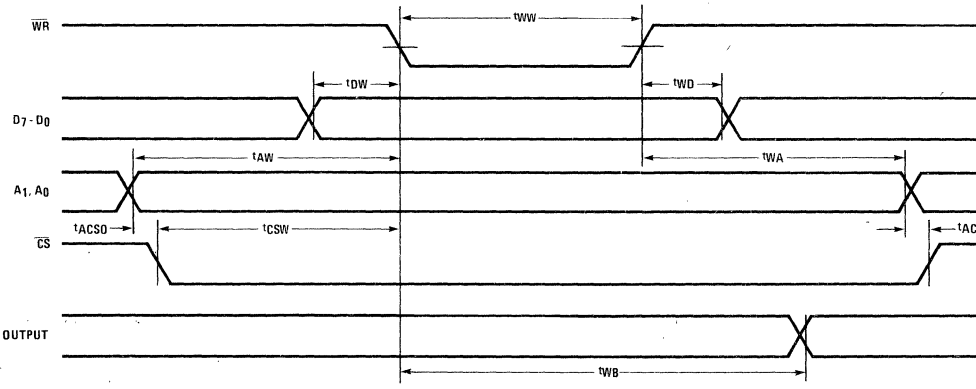
$T_A = 0°C$ to $+70°C$; $V_{CC} = +5\,V \pm 5\%$, $V_{SS} = 0\,V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{WW}	Pulse Width of $\overline{WR}$	400			ns	
t_{DW}	Time D.B. Stable before $\overline{WR}$	50			ns	
t_{WD}	Time D.B. Stable after $\overline{WR}$	35			ns	
t_{AW}	Time Address Stable before $\overline{WR}$	20			ns	
t_{WA}	Time Address Stable after $\overline{WR}$	20			ns	
t_{CSW}	Chip Select on to $\overline{WR}$		450		ns	
t_{WB}	Delay from $\overline{WR}$ to Output			500	ns	
t_{RP}	Pulse Width of $\overline{RD}$	405			ns	
t_{IR}	$\overline{RD}$ Set-Up Time	0			ns	
t_{HR}	Input Hold Time	100			ns	
t_{RD}	Delay from $\overline{RD} = 0$ to System Bus			295	ns	
t_{RH}	Delay from $\overline{RD} = 1$ to System Bus			150	ns	
t_{HZ}	$\overline{RD} = 0$ to TRI-STATE of Bus Drivers	10		150	ns	
t_{AR}	Time Address Stable before $\overline{RD}$	50			ns	
t_{CSR}	Time $\overline{CS}$ Stable before $\overline{RD}$		70		ns	
t_{AK}	Width of $\overline{ACK}$ Pulse	500			ns	
t_{ST}	Width of $\overline{STB}$ Pulse	500			ns	
t_{PS}	Set-Up Time for Peripheral	60			ns	
t_{PH}	Hold Time for Peripheral	180			ns	
t_{RA}	Hold Time, Address Bus Trailing Edge to $\overline{RD}$	0			ns	
t_{RC}	Hold Time for $\overline{CS}$ after $\overline{RD} = 1$	5			ns	
t_{AD}	Address Bus Valid to Data Valid			400	ns	
t_{KD}	Time from $\overline{ACK} = 1$ to Output Floating	20		480	ns	
t_{WO}	Time from $\overline{WR} = 1$ to $\overline{OBF} = 0$			650	ns	
t_{AO}	Time from $\overline{ACK} = 0$ to $\overline{OBF} = 1$			450	ns	
t_{SI}	Time from $\overline{STB} = 0$ to IBF			450	ns	
t_{RI}	Time from $\overline{RD} = 1$ to IBF = 0			360	ns	
t_{ACS0}	Address Bus Valid to $\overline{CS}$		40		ns	
t_{ACS1}	Address Change to $\overline{CS}$ OFF		40		ns	

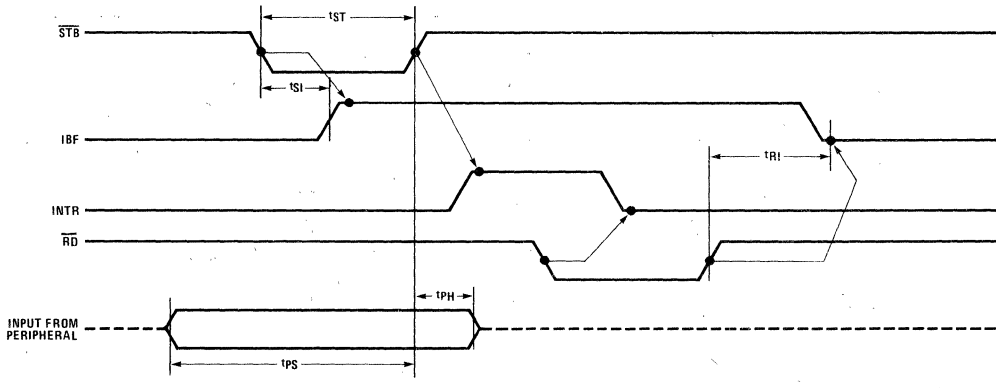
Timing Waveforms



Mode 0 (Basic Input)



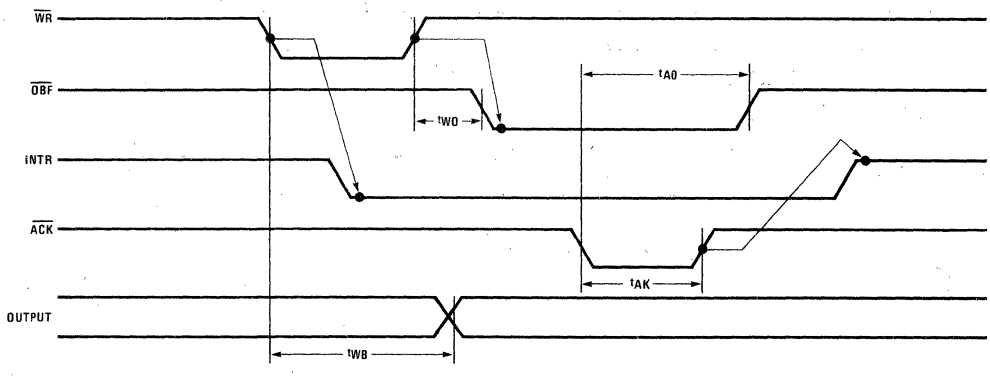
Mode 0 (Basic Output)



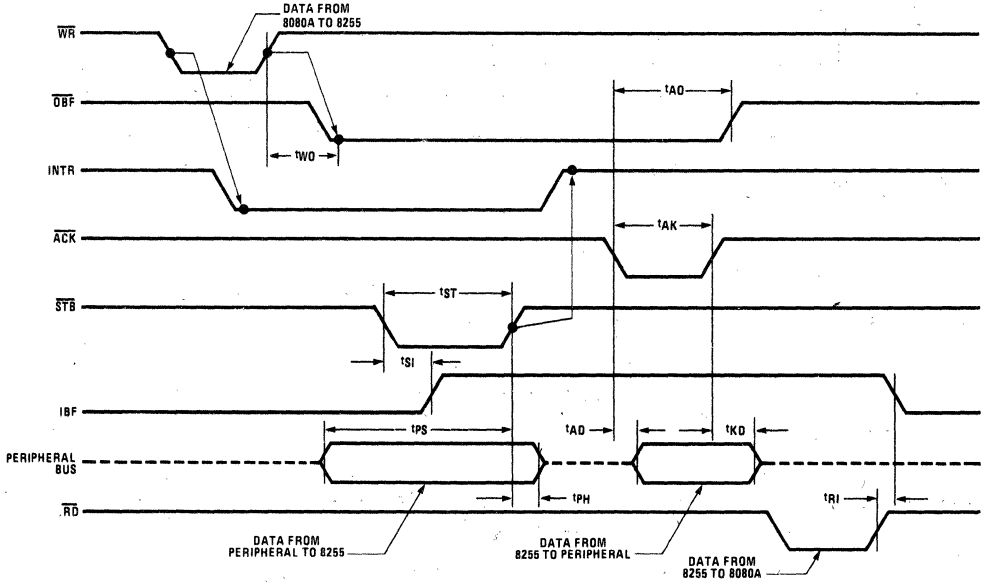
Mode 1 (Strobed Input)

D.2

Timing Waveforms (cont'd.)

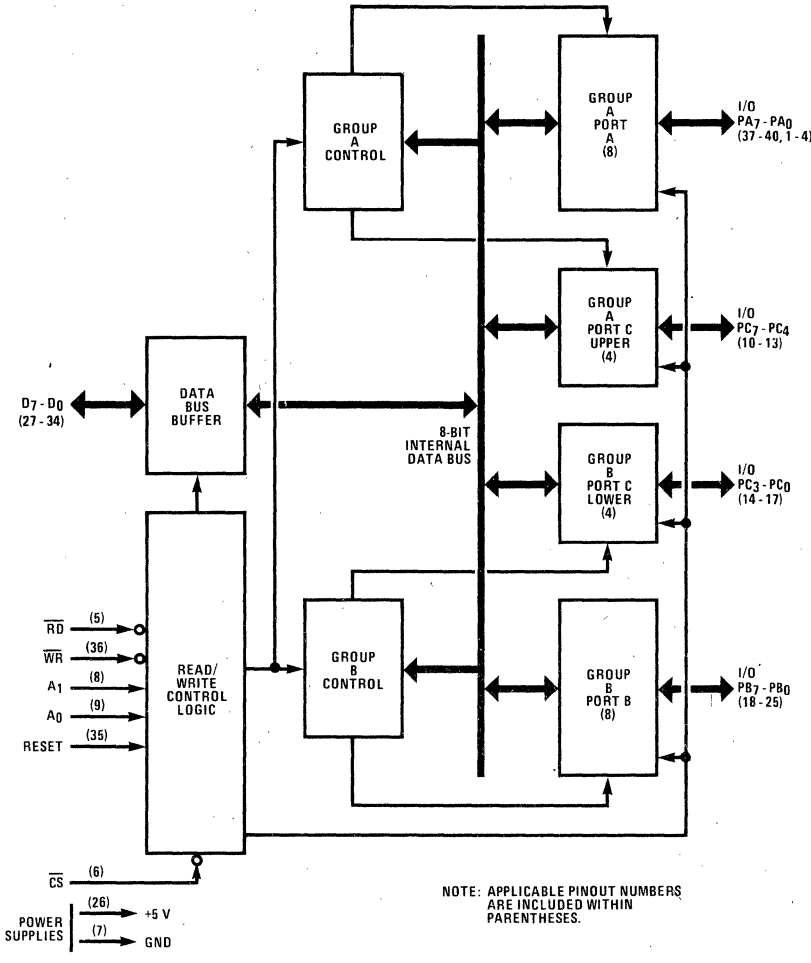


Mode 1 (Strobed Output)



Mode 2 (Bidirectional)

INS8255 Block Diagram



INS8255 Functional Pin Definitions

The following describes the function of all the INS8255 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Chip Select ($\overline{CS}$), Pin 6: When low, the chip is selected. This enables communication between the INS8255 and the INS8080A microprocessor.

Read ($\overline{RD}$), Pin 5: When low, allows the INS8080A to read data or status information from the INS8255.

Write ($\overline{WR}$), Pin 36: When low, allows the INS8080A to write data or control words into the INS8255.

Port Select (A_0, A_1), Pins 9 and 8: These two inputs, which are normally connected to the least significant bits of the A_{15}-A_0 Address Bus, control the selection of one of three 8-bit ports (A, B and C) or the internal control word register as indicated below.

A_1	A_0	Selected
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Control Word Register

Reset, Pin 35: When high, clears all the internal registers of the chip and sets Ports A, B and C to the input high impedance mode.

+5 Volts, Pin 26: V_{CC} supply.

Ground, Pin 7: 0 Volt reference.

D.2

INPUT/OUTPUT SIGNALS

Data (D_7-D_0) Bus, Pins 27-34: This bus comprises eight TRI-STATE input/output lines. The bus provides bi-directional communication between the INS8255 and the INS8080A. Data is routed to or from the internal data bus buffer upon execution of an OUT or IN Instruction, respectively, by the INS8080A. In addition, control words and status information are transferred through the data bus buffer.

Port A (PA_7-PA_0), Pins 37-40, 1-4: This 8-bit input/output port forms one 8-bit data output latch/buffer and/or one 8-bit data input latch.

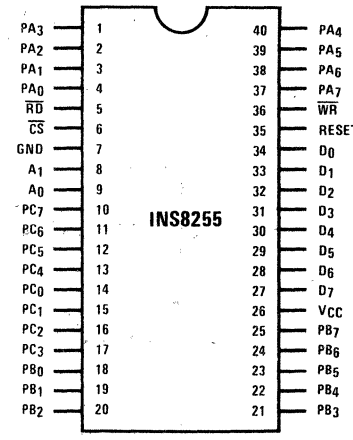
NOTE

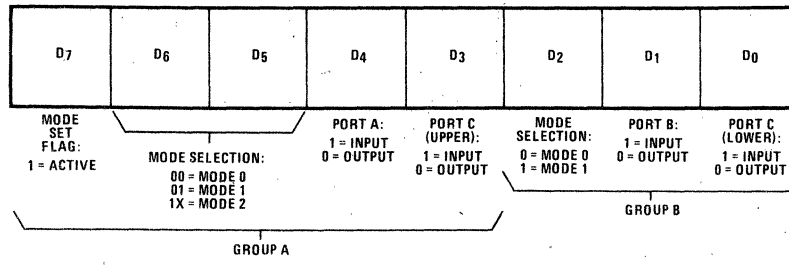
The system software uses a Mode Definition Control Word (see figure) as the second byte of OUT Instruction(s) to program the functional configuration of Ports A through C. Whenever the mode is changed, all output registers (and status flip-flops) are reset.

Port B (PB_7-PB_0), Pins 18-25: This 8-bit input/output port forms one 8-bit data output latch/buffer or one 8-bit data input buffer.

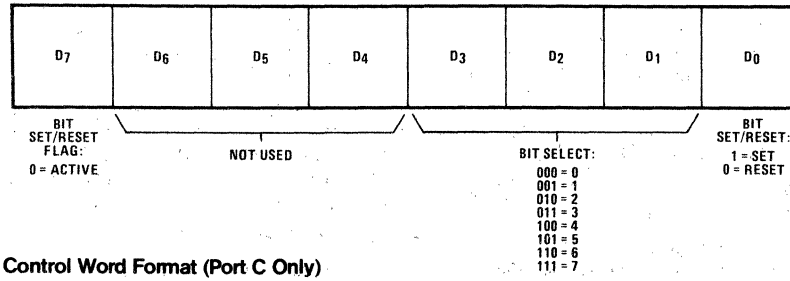
Port C (PC_7-PC_0), Pins 10-17: This 8-bit input/output port forms one 8-bit data output latch/buffer or one 8-bit data input buffer. The port can be split into two 4-bit ports under the mode control. Each of these 4-bit ports contains a 4-bit latch that may be used for the control and status signals, in conjunction with Ports A and B. The system software includes a Bit Set/Reset Control Word (see figure) for setting or resetting any of the eight bits of Port C. When Port C is being used as a status/control for Port A or B, the Port C bits can be set or reset by using the Bit Set/Reset Control Word as the second byte of OUT Instruction(s).

Pin Configuration





Mode Definition Control Word Format



Bit Set/Reset Control Word Format (Port C Only)

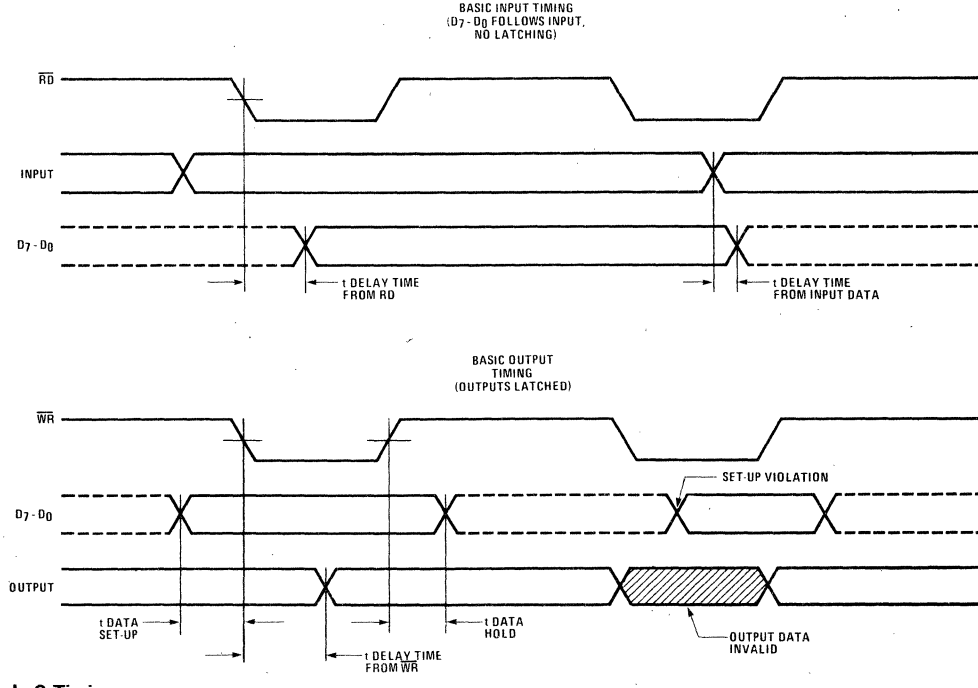
Operating Modes

Mode 0 (Basic Input/Output)

In this mode, simple input and output operations for each of the three ports are provided. No "handshaking" is required; data is simply written to or read from a specified port.

Mode 0 Port Definition Chart

No.	Control Word Bits								Group A		Group B	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Port A	Port C (Upper)	Port B	Port C (Lower)
0	1	0	0	0	0	0	0	0	OUTPUT	OUTPUT	OUTPUT	OUTPUT
1	1	0	0	0	0	0	0	1	OUTPUT	OUTPUT	OUTPUT	INPUT
2	1	0	0	0	0	0	1	0	OUTPUT	OUTPUT	INPUT	OUTPUT
3	1	0	0	0	0	0	1	1	OUTPUT	OUTPUT	INPUT	INPUT
4	1	0	0	0	1	0	0	0	OUTPUT	INPUT	OUTPUT	OUTPUT
5	1	0	0	0	1	0	0	1	OUTPUT	INPUT	OUTPUT	INPUT
6	1	0	0	0	1	0	1	0	OUTPUT	INPUT	INPUT	OUTPUT
7	1	0	0	0	1	0	1	1	OUTPUT	INPUT	INPUT	INPUT
8	1	0	0	1	0	0	0	0	INPUT	OUTPUT	OUTPUT	OUTPUT
9	1	0	0	1	0	0	0	1	INPUT	OUTPUT	OUTPUT	INPUT
10	1	0	0	1	0	0	1	0	INPUT	OUTPUT	INPUT	OUTPUT
11	1	0	0	1	0	0	1	1	INPUT	OUTPUT	INPUT	INPUT
12	1	0	0	1	1	0	0	0	INPUT	INPUT	OUTPUT	OUTPUT
13	1	0	0	1	1	0	0	1	INPUT	INPUT	OUTPUT	INPUT
14	1	0	0	1	1	0	1	0	INPUT	INPUT	INPUT	OUTPUT
15	1	0	0	1	1	0	1	1	INPUT	INPUT	INPUT	INPUT



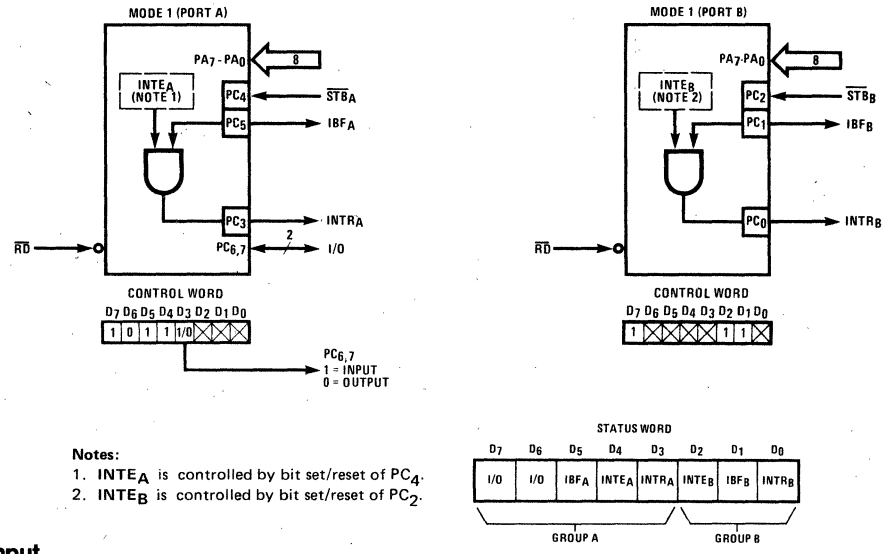
Mode 0 Timing

D.2

Operating Modes (cont'd.)

Mode 1 (Strobed Input/Output)

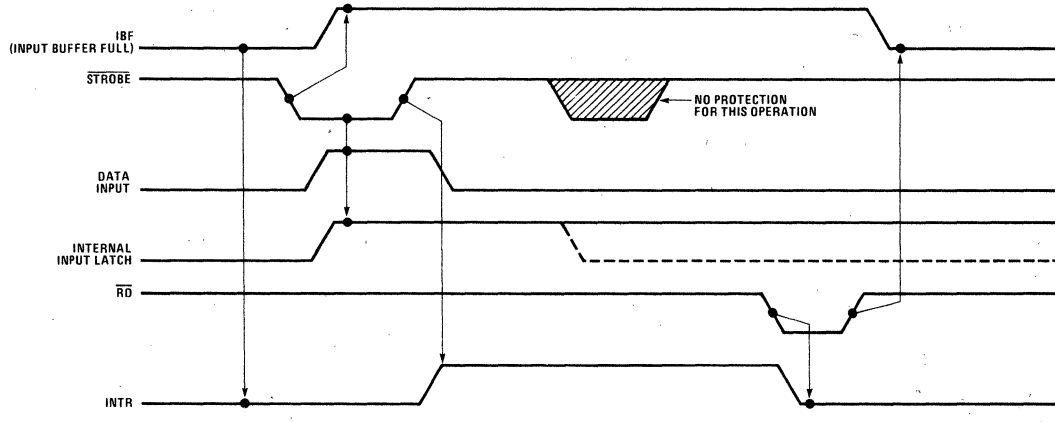
In this mode, a means for transferring input/output data to or from a specified port in conjunction with strobes or "handshaking" signals is provided. Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals in Mode 1. The programmer can read the contents of Port C to test or verify the status of each peripheral device. Since no special instruction is provided in the INS8080A microcomputer system to read the Port C status information, a normal read operation must be executed to perform this function.



Notes:

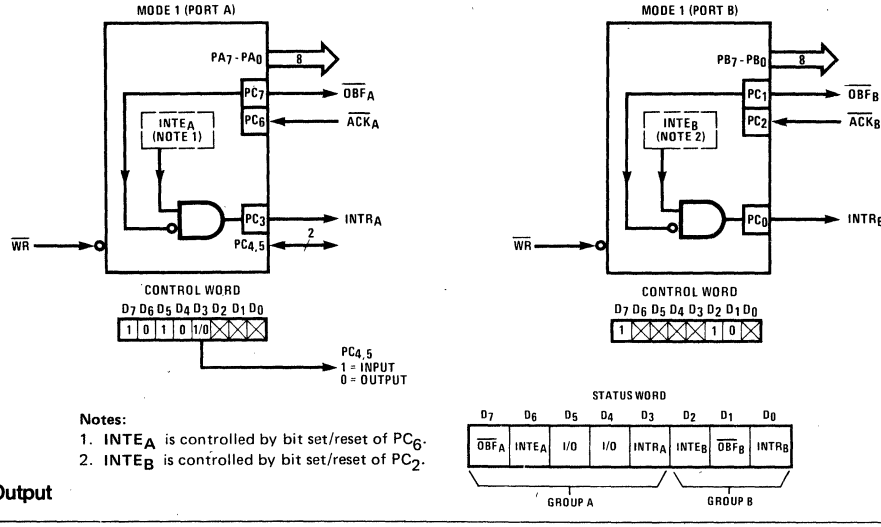
1. $INTE_A$ is controlled by bit set/reset of PC_4.
2. $INTE_B$ is controlled by bit set/reset of PC_2.

Mode 1 Input



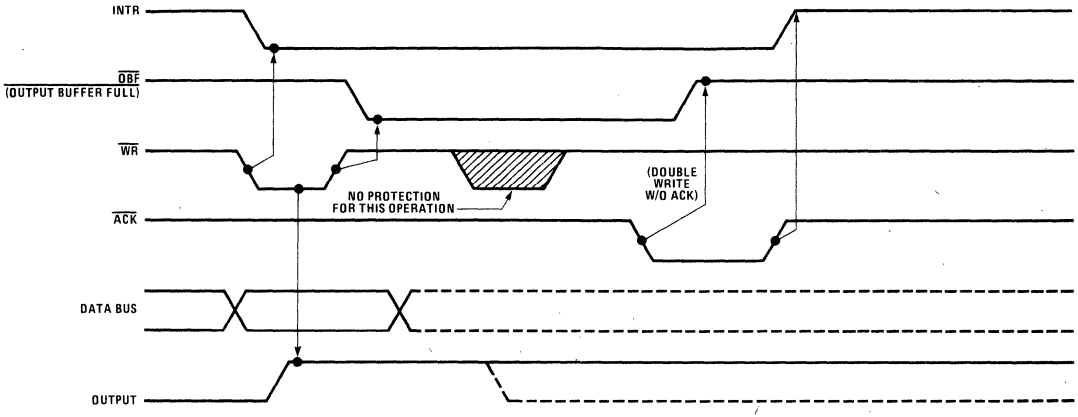
Mode 1 Input Timing

Operating Modes (cont'd.)

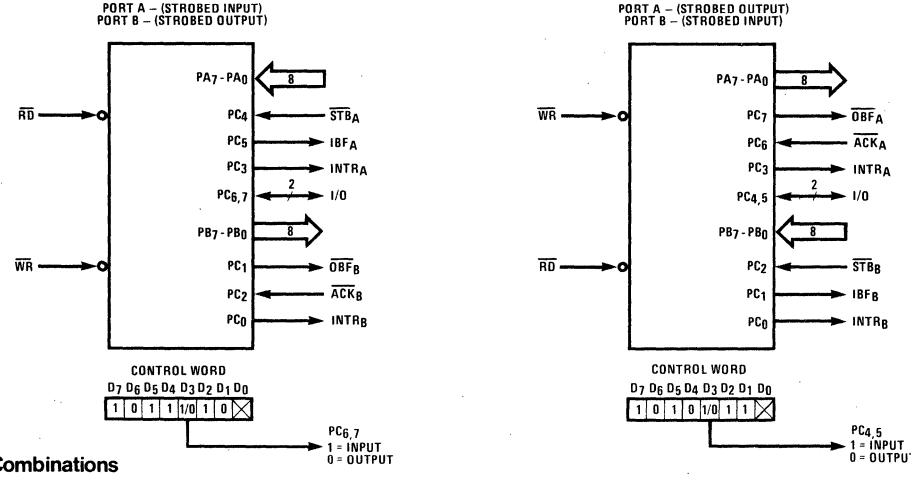


Notes:
1. $INTE_A$ is controlled by bit set/reset of PC_6.
2. $INTE_B$ is controlled by bit set/reset of PC_2.

Mode 1 Output



Mode 1 Output Timing



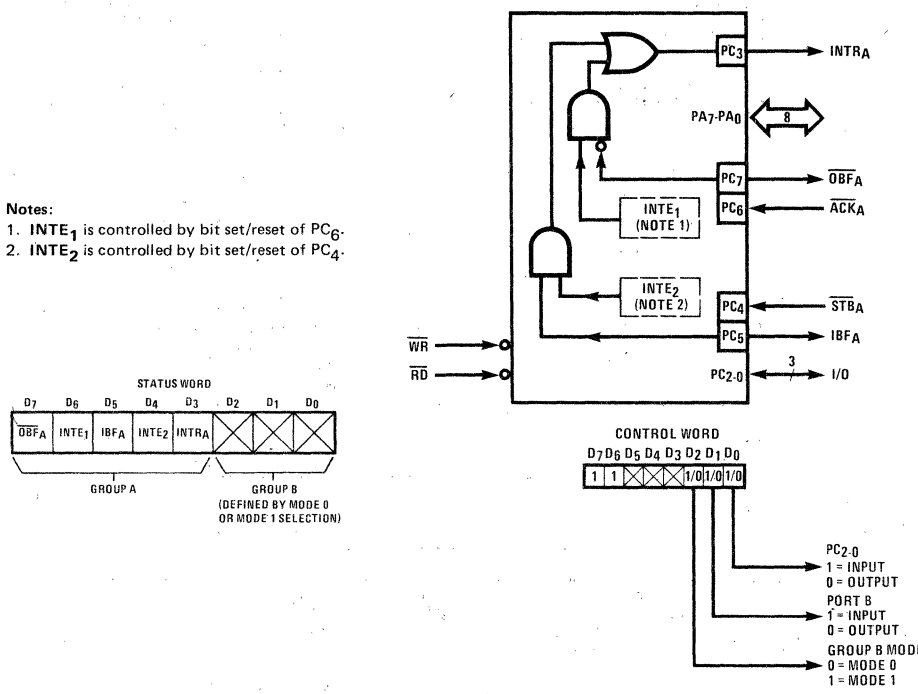
Mode 1 Combinations

D.2

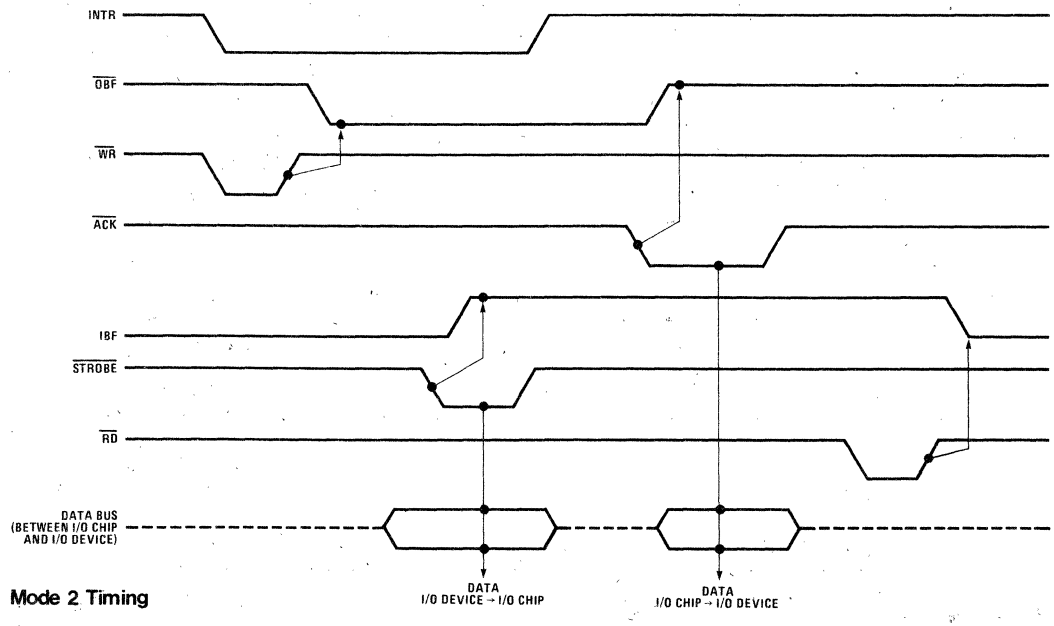
Operating Modes (cont'd.)

Mode 2 (Strobed Bidirectional Bus Input/Output)

This mode enables communication with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus input/output). "Handshaking" signals are provided to maintain proper bus flow discipline in a manner similar to Mode 1. In addition, interrupt generation and enable/disable functions are available in Mode 2.



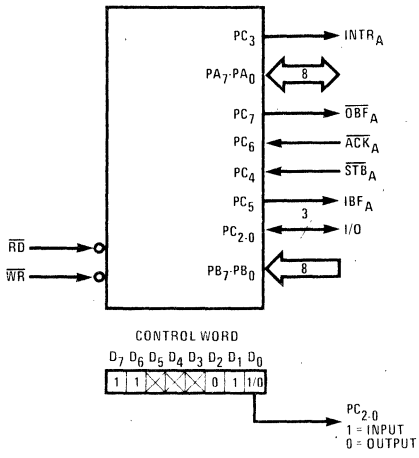
Mode 2



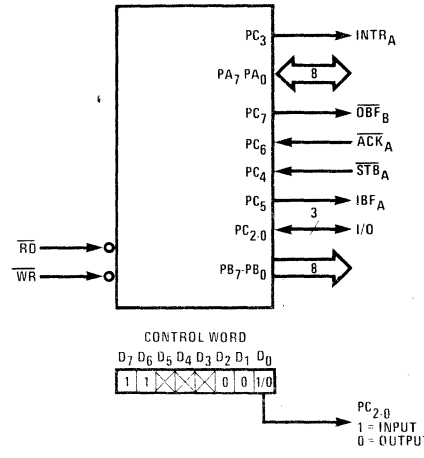
Mode 2 Timing

Operating Modes (cont'd.)

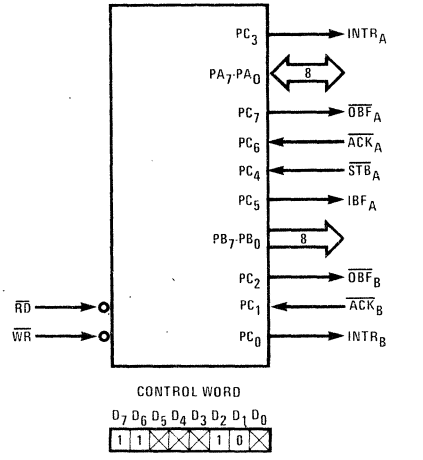
MODE 2 AND MODE 0 (INPUT)



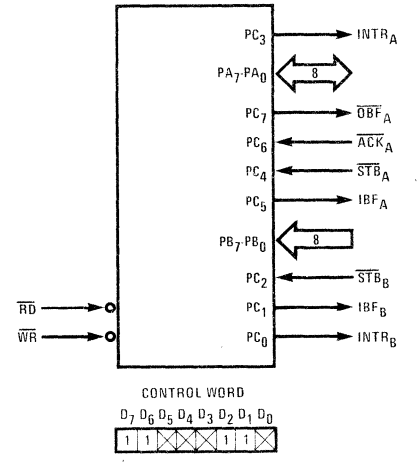
MODE 2 AND MODE 0 (OUTPUT)



MODE 2 AND MODE 1 (OUTPUT)



MODE 2 AND MODE 1 (INPUT)



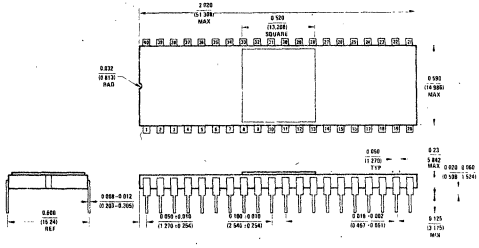
D.2

Mode 2 Combinations

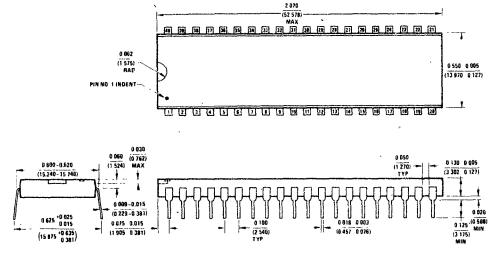
Mode Definition Summary Table

Port Bits	Mode 0		Mode 1		Mode 2
	IN	OUT	IN	OUT	Group A Only
PA_0	IN	OUT	IN	OUT	Bidirectional
PA_1	IN	OUT	IN	OUT	↕
PA_2	IN	OUT	IN	OUT	
PA_3	IN	OUT	IN	OUT	
PA_4	IN	OUT	IN	OUT	
PA_5	IN	OUT	IN	OUT	
PA_6	IN	OUT	IN	OUT	
PA_7	IN	OUT	IN	OUT	Bidirectional
PB_0	IN	OUT	IN	OUT	
PB_1	IN	OUT	IN	OUT	
PB_2	IN	OUT	IN	OUT	
PB_3	IN	OUT	IN	OUT	(Mode 0 or Mode 1 only)
PB_4	IN	OUT	IN	OUT	
PB_5	IN	OUT	IN	OUT	
PB_6	IN	OUT	IN	OUT	
PB_7	IN	OUT	IN	OUT	
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$
PC_5	IN	OUT	IBF_A	I/O	IBF_A
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

Physical Dimensions



Ceramic Dual-In-Line Package (D)
Order Number INS8255D



Plastic Dual-In-Line Package (N)
Order Number INS8255N

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, California 95051
Tel: (408) 737-5000
TWX: (910) 339-9240

National Semiconductor GmbH
8000 München 21
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Telex: 05-22772

NS International Inc., Japan
Miyake Building
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Tokyo, Japan
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TWX: 232-2015 NSCJ-J

NS Electronics (Hong Kong) Ltd.
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Cheung Kong Electronic Bldg.
4 Hing Yip Street
Kwun Tong
Kowloon, Hong Kong
Tel. 3-411241-8
Telex: 73866 NSEHK HX
Cable: NATSEMI

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Avda Brigadeiro Faria Lima 844
11 Andar Conjunto 1104
Jardim Paulistano
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NS Electronics Pty. Ltd.
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National Semiconductor

AUGUST 1978

DP8350 Series Programmable CRT Controllers

General Description

The DP8350 Series of CRT Controllers are single-chip bipolar (I^2L technology) circuits in a 40-pin package. They are designed to be dedicated CRT display refresh circuits.

The CRT Controller (CRTC) provides an internal dot rate crystal controlled oscillator for ease of system design. For systems where a dot rate clock is already provided, an external clock input may be used by the CRTC. In either case system synchronization is made possible with the use of the buffered Dot Rate Clock Output.

The DP8350 Series has 11 character generation related timing outputs. These outputs are compatible for systems with or without line buffers, using character ROMS, or DM8678-type latch/ROM/shift register circuits.

12 bits (4k) of bidirectional TRI-STATE® character memory addresses are provided by the CRTC for direct interface to character memory.

Three on-chip registers provide for external loading of the row starting address, cursor address, and top-of-page address.

A complete set of video outputs is available including cursor enable, programmable vertical blanking, programmable horizontal sync, and programmable vertical sync.

The DP8350 Series CRTC provides for a wide range of programmability using internal mask programmable ROMs:

- Character Field (both number of dots/character and number of scan lines/character)
- Characters per Row
- Character Rows per Video Frame

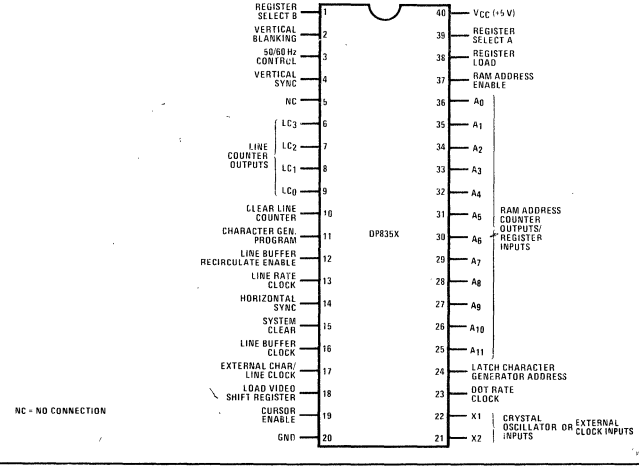
The CRTC also provides system sync and program inputs including 50/60 Hz control, system clear, external character/line rate clock, and character generator program.

The DP8350 Series operates on a single +5 V power supply. Outputs and inputs are TTL compatible.

Features

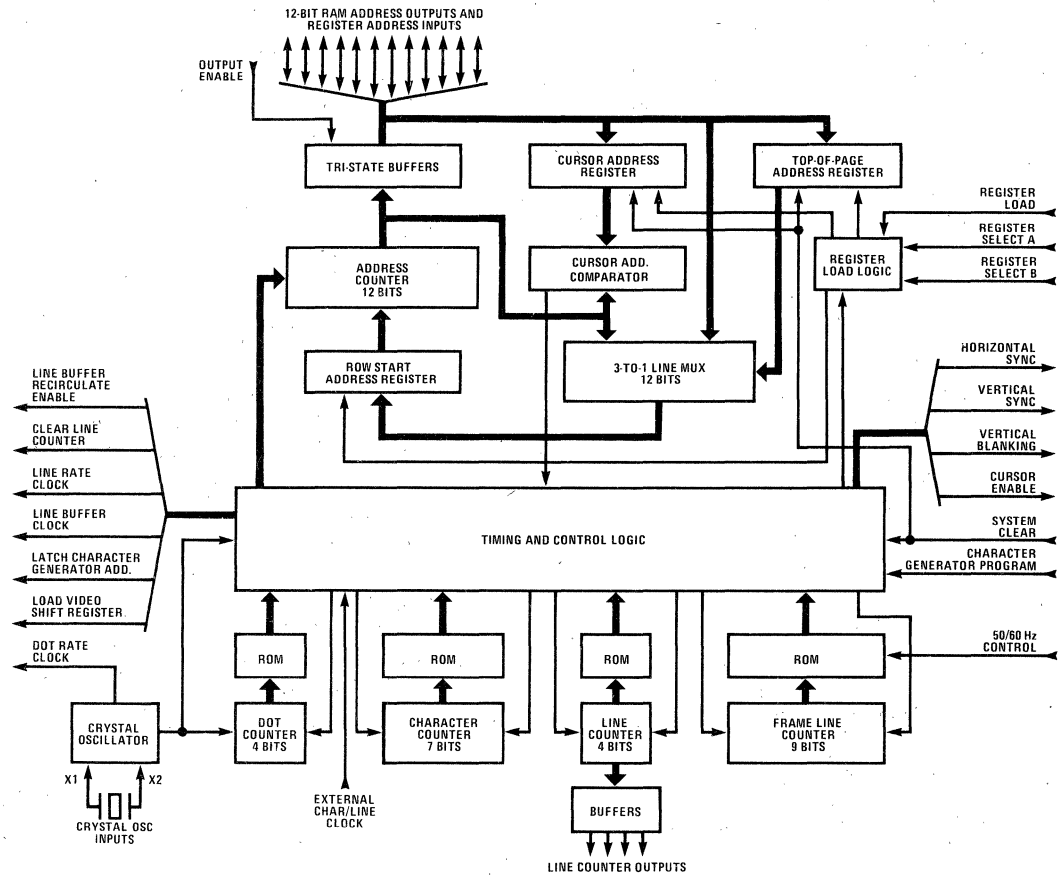
- Internal crystal controlled dot rate oscillator
- External dot rate clock input
- Buffered dot rate clock output
- Timing pulses for character generation
- Character memory address outputs (12 bits)
- Internal cursor address register
- Internal row starting address register
- Top-of-page address register (for scrolling)
- Programmable horizontal and vertical sync outputs
- Programmable cursor enable output
- Programmable vertical blanking output
- 50/60 Hz refresh rate
- Programmable characters/row (5 to 110)
- Programmable character field size (up to 16 dots x 16 scan line field size)
- Programmable character rows/frame (1 to 64)
- Single +5 V power supply
- Inputs and outputs TTL compatible
- Ease of system design/application

DP8350 Series Connnnection Diagram



D.3

DP8350 Block Diagram



CHARACTER GENERATION/TIMING OUTPUTS

The CRTC provides 11 interface timing outputs for line buffers, character generator ROM, DM8678-type latch/ROM/shift register combination character generators, and system status timing. All outputs are TTL compatible and directly interface to popular system circuits, including:

- DM8678 Series Character Generators
- MM52157, MM52179 Character ROMs
- DM74166 Dot Shift Register
- MK1007P, 33571/2, 2532 80-Bit Shift Registers (Line Buffers)

Dot Rate Clock: This output is buffered for use in system synchronization and interface to dot shift register. Positive edge clock at crystal oscillator frequency.

Load Video Shift Register: Buffered output at character rate frequency. Used for direct interface to dot shift register. This output is active only during video time and therefore performs both the horizontal and vertical blanking functions. Low level active.

Latch Character Generator Address: Buffered output at character rate frequency. Active at all times. Positive edge clock.

Line Buffer Clock: This output directly interfaces to line buffers. Output operates at character rate. Negative edge clock. Not active during horizontal blanking. The number of clocks per scan line is equivalent to the number of video characters per row.

Line Rate Clock: Line rate frequency output for use with DM8678-type character generator.

Line Counter Outputs (LC_0 to LC_3): Buffered outputs at line rate frequency for use with character ROMs without internal line counter. These outputs are also useful for system decode of present line position in character row. Outputs clock in sync with Line Rate Clock at start of horizontal blanking. Outputs are always active.

Clear Line Counter: Row rate clock — occurs in sync with Line Rate Clock during horizontal blanking between last line of any row and first line of a new row. This output is always active and is a negative edge clock — direct interface to the DM8678.

Line Buffer Recirculate Enable: This output interfaces to a line buffer and becomes inactive (logic "0" state) during the last line or the first line of a character row, depending on the state of the character generator program input. A low level on this output indicates (in line buffer applications) the time during which the line buffer is loaded with the next row of character codes.

Table 1. Character Generator Program Truth Table

Character Generator Program Input	Recirculate Enable Output Low Level and New Row Address at Address Outputs
"0"	Last line of character row
"1"	First line of character row

The pulse appears at the start of horizontal blanking prior to when the memory address bus must be transferred to the CRTC, then returns to the high state at the next horizontal blanking interval.

MEMORY ADDRESS OUTPUTS/INPUTS AND REGISTERS

CRT Character Address Outputs (TRI-STATE) — A_0 to A_{11}: 12 bits of bidirectional CRT character address counter outputs are provided by the CRTC. These outputs directly interface to the system RAM memory address bus.

Within a scan line the counter is pre-set to the address contained within the Row Start Register (RSR) three character times before the start of video time. The counter is then advanced sequentially at character rate to the max video character address plus 1 for the present scan line. This address is then held during the horizontal blanking interval up to three character times before video start for the next scan line. At this point the counter is again pre-set to the contents of the RSR and the above sequence is repeated. This sequence provides scan line address repetition for every scan line of a character location within a row. Row-to-row start address modifications are accomplished by updating the contents of the RSR.

During vertical blanking the address counter operation is modified by stopping the pre-set load of the contents of the RSR into the address counter, thereby allowing the address outputs to free run during vertical blanking. This allows minimum access time to the CRTC when the CRTC address counter outputs are being used for dynamic RAM refresh.

RAM Address Enable Input: At all times the status of the address counter outputs is controlled externally by the Enable Input. Logic "0" = TRI-STATE, Logic "1" = Active.

Internal Top-of-Page, Row Start, and Cursor Registers: Control pins are provided for loading the top-of-page, row start, and cursor address into three 12-bit CRTC registers from the bidirectional memory address pins.

The Top-of-Page Register (TOPR) holds the address of the first character of the first video row. This register allows display scroll with the CRTC without the use of external memory address adders. If the TOPR is not loaded after a system clear its contents will be zero and the address outputs will be sequential from zero at the top-of-page.

The Cursor Register (CR) holds the present address of the cursor and is cleared to zero after a system clear. Once the TOPR and CR registers have been loaded they need not be accessed again until modification of their contents is required. These registers may be loaded at any time, but to cause minimum display distortion it is recommended that they be loaded only during blanking intervals.

The Row Start Register (RSR) is the working register for the CRTC address counter. It determines the first video character address on a scan line to scan line basis.

Modification of this register after the start of video in a scan line will modify the address counter outputs at the start of video on the next scan line. (See address output description.) If the RSR is never externally loaded, the CRTC address outputs will be sequential on a row-to-row basis from the TOPR contents at the start of the video page. With external loading, row-to-row non-sequential operation of the CRTC address outputs is possible, thus row-to-row edit capability. When used in this mode the RSR should be loaded after the start of video time of the last scan line of the previous row. A load to the RSR during vertical blanking will also load the TOPR.

Table 2. Register Load Truth Table

Register Select A	Register Select B	Register Load Input	Register Access
0	0	0	No Select
0	1	0	Top-of-Page
1	0	0	Row Start*
1	1	0	Cursor
X	X	1	No Select

*During vertical blanking a load to this register will also load the top-of-page register.

VIDEO RELATED OUTPUTS

Horizontal Sync: This output provides the necessary line (scan) rate sync to either three-terminal or composite sync monitors. The pulse is programmable in position and width at character time increments. This output may also be programmed to have RS-170 compatible serration pulses during the vertical sync interval. The active logic state of this output is also programmable.

Vertical Sync: This output provides the necessary frame rate sync consistent with either three-terminal or composite type monitors. The pulse is programmable in position and width at line (scan) time increments. The active logic state of this output is also programmable.

Cursor Enable: When a match with the CRTC cursor address register and address counter occurs a pulse will appear at this output at that video character time (character field width) for every line in that row. This output may also be programmed to appear on only one line of a character row. With the character generator program pin in a logic "0" position the cursor enable output will not be valid on the last line of a character row for that row. Like the Load Video Shift Register Output, this output is not active during horizontal or vertical blanking. High level active output.

CRT SYSTEM CONTROL FUNCTIONS

50/60 Hz Control Input: This input controls the CRT system refresh rate. The CRTC may also be programmed for refresh rates other than 50 and 60 Hz.

50/60 Hz Control	Refresh Rate
1	60 Hz (f_1)
0	50 Hz (f_0)

Vertical Blanking Output: This output becomes active (logic "1") at the start of vertical blanking and may be programmed to stop at the end of any line of the character row before the start of the first video row. This output is useful for flag applications to other elements in the CRT system. Its active level is also programmable.

System Clear Input: This input when low sets and holds the CRTC at the start of vertical blanking for system sync and test. It also clears to zero the cursor and top-of-page registers. The input has hysteresis and may be connected to a resistor to V_{CC} and a capacitor to ground to provide power-up system clear.

Character Generator Program Input: This input modifies both the position of the recirculate enable output low level and the time at which the address outputs change to a new row address. It is intended to provide optimum use of the CRTC with character generator/ROMs programmed with or without active video on the first or last line of a character row. (See Recirculate Enable for truth table.)

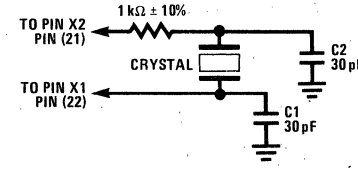
External Character/Line Rate Clock: This input is intended to aid testing of the CRTC and is not meant to be used as an active input in a CRT system. When this input is left open it is guaranteed not to interfere with normal operation.

Crystal Inputs X1 and X2: The oscillator is controlled by an external, parallel resonant crystal connected between the X1 and X2 pins. Normally, a fundamental mode crystal is used to determine the operating frequency of the oscillator; however, overtone mode crystals may be used.

Crystal Specifications (parallel resonant):

Type . . . . . AT-Cut Crystal
Tolerance . . . . . 0.005% at 25°C
Stability . . . . . 0.01% from 0°C to +70°C
Resonance . . . . . Fundamental (parallel)
Maximum Series Resistance . . . . . Dependent on frequency (for 10.92 MHz, 50 Ω)
Load Capacitance . . . . . 20 pF

Connection Diagram



If the DP8350 series is clocked at dot rate by a system clock, pin 22 (X1 input) should be clocked directly using a Schottky series circuit. Pin 21 (X2 input) may be left open.

Timing Waveforms

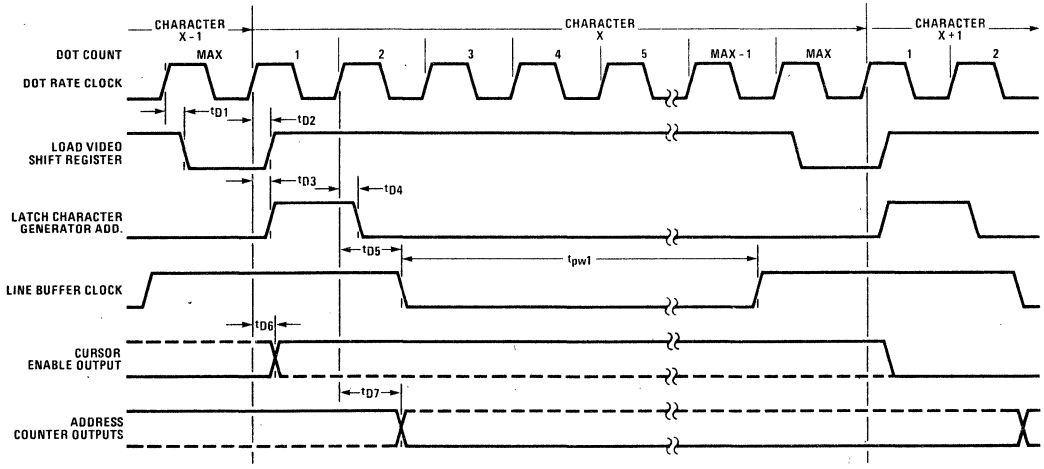
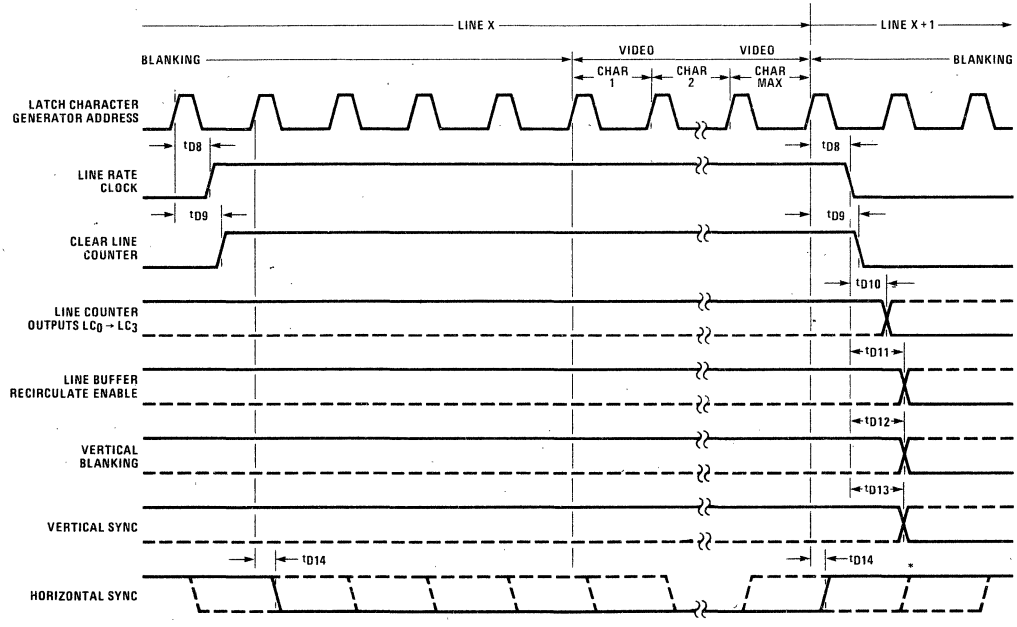


Figure 1. Dot/Character Rate Timing

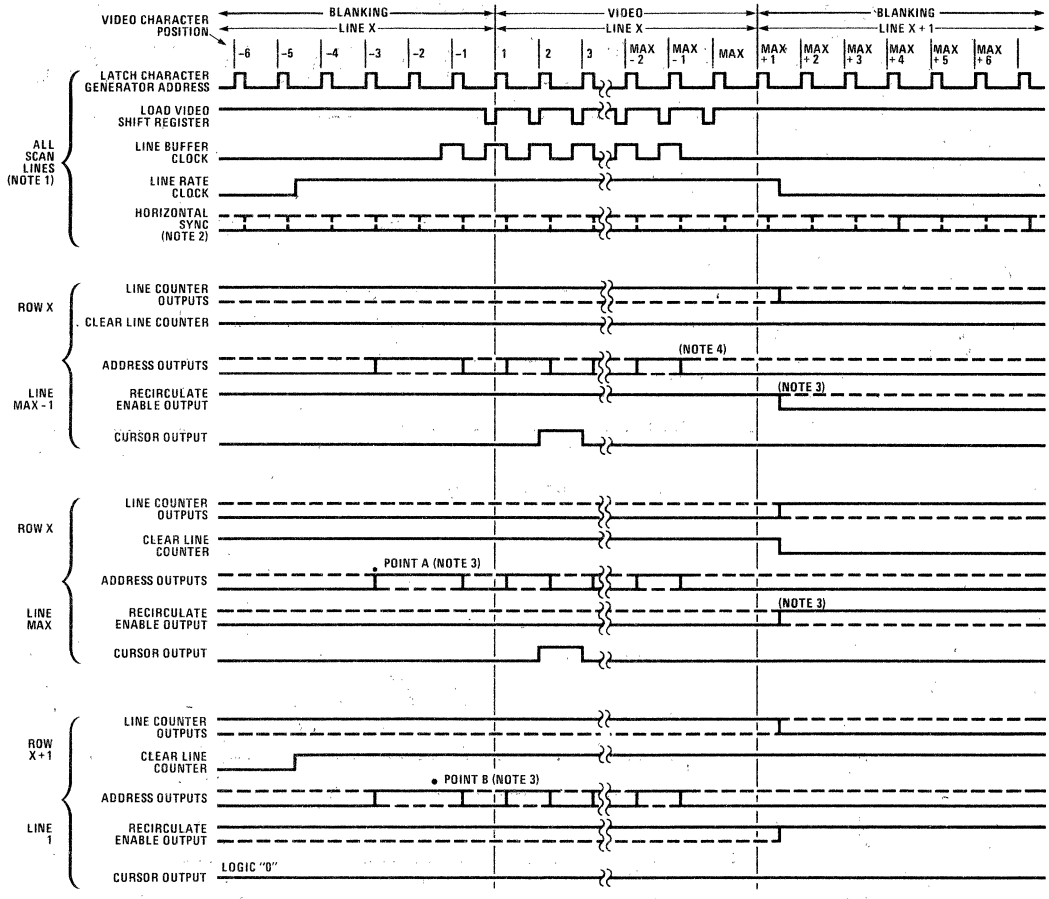


*THE POSITION OF THE START AND STOP POINTS OF THE HORIZONTAL SYNC PULSE ARE PROGRAMMABLE BY CHARACTER TIME – WITHIN ONE CHARACTER TIME THE POINTS WILL HAVE THE t_{D14} TIME RELATIONSHIP.

Figure 2. Character/Line Rate Timing

D.3

Timing Waveforms (cont'd.)



Note 1: The load video shift register output is not active during vertical or horizontal blanking (remains in the logic "1" state during these intervals.

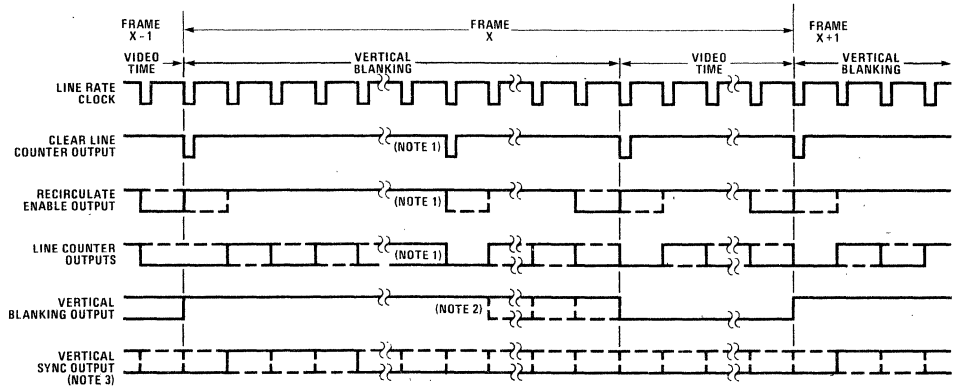
Note 2: The horizontal sync output start and stop point positions are user-programmable at character width intervals.

Note 3: The position of the recirculate enable output logic "0" level is dependent on the state of the character generator program input (CGPI). With CGPI = "0," recirculate enable occurs on the max line of a character row (solid line) and the address counter outputs roll over to the new row address at point A. With CGPI = "1," recirculate enable occurs on the first line of a character row (dashed line) and the address counter outputs roll over to the new row address at point B.

Note 4: The address counter outputs clock to the address of the last character of a video row plus 1. This address is then held during the horizontal blanking interval until video minus three character times. At this point the outputs are modified to the contents of the Row Start Register (RSR). With no external loading of the RSR the contents will be either the character address of the first character in the present row or the character address of the first character of the next video row (depending on the state of the Character Generator Program input) which will be sequential from the last character address of the last row. If the RSR was loaded, then the address outputs will be modified to the contents of the register.

Figure 3. Character/Line Rate Functional Diagram

Timing Waveforms (cont'd.)

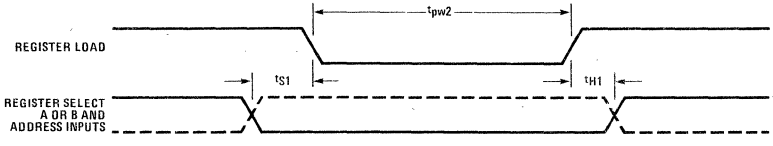


Note 1: One full row before start of video the line counter is set to zero state – this provides line counter synchronization in cases where the number of lines in vertical blanking are not even multiples of the number of lines per row.

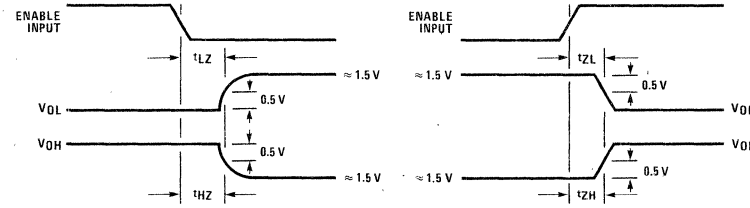
Note 2: The stop point of vertical blanking is programmable at line intervals within the last character row before start of video.

Note 3: The Vertical Sync Output start and stop points are programmable at line rate increments.

Figure 4. Line/Frame Rate Functional Diagram

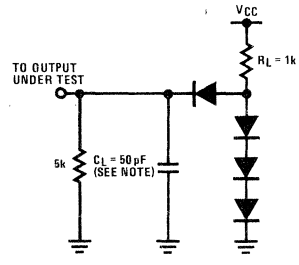


REGISTER LOAD WAVEFORMS

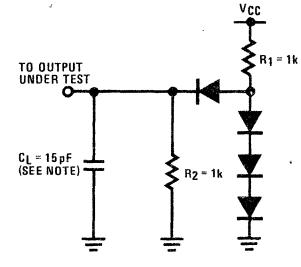


ADDRESS OUTPUTS ENABLE/DISABLE WAVEFORMS

Test Load Circuits



LOAD CIRCUIT 1



LOAD CIRCUIT 2

NOTE: C_L INCLUDES PROBE AND JIG CAPACITANCE
ALL DIODES ARE 1N914 OR EQUIVALENT.

D.3

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0 V
Input Voltage	−1 V to +5.5 V
Output Voltage	5.5 V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	+70	°C

Electrical Characteristics V_{CC} = 5 V ± 5%, T_A = 0°C to +70°C (Notes 2 and 3)

Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage					
	(System Clear)		2.6			V
	(All Other Inputs Except X1, X2)		2.0			V
V_{IL}	Logic "0" Input Voltage					
	(System Clear)				0.8	V
	(All Other Inputs Except X1, X2)				0.8	V
V_{IH}-V_{IL}	System Clear Input Hysteresis			0.4		V
V_{clamp}	Input Clamp Voltage (All Inputs Except X1, X2, & Char/Line Rate Clock)	I_{IN} = −12 mA		−0.8		V
I_{IH}	Logic "1" Input Current					
	(Address Outputs)	Enable Input = 0 V, V_{CC} = 5.25 V, V_R = 5.25 V		10		μA
	(All Other Inputs Except X1, X2)	V_{CC} = 5.25 V, V_R = 5.25 V		2		μA
I_{IL}	Input Current					
	(Address Outputs)	Enable Input = 0 V, V_{CC} = 5.25 V, V_{IN} = 0.5 V		−20		μA
	(All Other Inputs Except X1, X2)	V_{CC} = 5.25 V, V_{IN} = 0.5 V		−20		μA
V_{OH}	Logic "1" Output Voltage	I_{OH} = −100 μA	3.2	4.1		V
		I_{OH} = −1 mA	2.5	3.3		V
V_{OL}	Logic "0" Output Voltage	I_{OL} = 5 mA		0.35	0.5	V
I_{OS}	Output Short Circuit Current	V_{CC} = 5 V, V_{OUT} = 0 V, (Note 4)		−40		mA
I_{CC}	Power Supply Current	V_{CC} = 5.25 V		170		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75 V to 5.25 V power supply range. All typical values are for T_A = 25°C and V_{CC} = 5.0 V.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5.0 V, T_A = 25°C (Notes 1 and 2)

	Parameter	Conditions	Min	Typ	Max	Unit
t_{D1}	Dot Clock to Load Video Shift Register Negative Edge	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		5		ns
t_{D2}	Dot Clock to Load Video Shift Register Positive Edge	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		11		ns
t_{D3}	Dot Clock to Latch Character Generator Positive Edge	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		11		ns
t_{D4}	Dot Clock to Latch Character Generator Negative Edge	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		4		ns
t_{D5}	Dot Clock to Line Buffer Clock Negative Edge	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		20		ns
t_{PW1}	Line Buffer Clock Pulse Width	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		N(DT)*		ns
t_{D6}	Dot Clock to Cursor Enable Output Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		25		ns
t_{D7}	Dot Clock to Valid Address Output	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		20		ns
t_{D8}	Latch Character Generator to Line Rate Clock Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		300+2DT		ns
t_{D9}	Latch Character Generator to Clear Line Counter Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		400+2DT		ns
t_{D10}	Line Rate Clock to Line Counter Output Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		180		ns
t_{D11}	Line Rate Clock to Line Buffer Recirculate Enable Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		200		ns
t_{D12}	Line Rate Clock to Vertical Blanking Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		200		ns
t_{D13}	Line Rate Clock to Vertical Sync Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		200		ns
t_{D14}	Latch Character Generator to Horizontal Sync Transition	C_L = 50 pF, R_L = 1 kΩ, Load Circuit 1		100		ns
t_{SI}	Register Select/Memory Address Setup Time Prior to Register Load Negative Edge			100		ns
t_{HI}	Register Select Memory Hold Time After Register Load Positive Edge			0		ns
t_{PW2}	Register Load Pulse Width			150		ns
f_{MAXdot}	Maximum Dot Rate Frequency			25		MHz
$f_{MAXchar}$	Maximum Character Rate Frequency			2.5		MHz
t_{LZ}, t_{HZ}	Delay from Enable Input to High Impedance State from Logic "0" and Logic "1"	C_L = 15 pF, Load Circuit 2		25		ns
t_{ZL}, t_{ZH}	Delay from Enable Input to Logic "0" and Logic "1" from High Impedance State	C_L = 15 pF, Load Circuit 2		25		ns

Note 1: Unless otherwise specified, all AC measurements are referenced to the 1.5 V level of the input to 1.5 V of the output.

Note 2: When external clock inputs are used, the input characteristics are Z_{OUT} = 50 Ω and $t_R \leq 10$ ns, $t_F \leq 10$ ns.

*"DT" is defined as the duration (in ns) of one full cycle of the Dot Rate Clock (Item 20 of the ROM Program Table). "N" denotes the number of DTs per definition in Item 24 of the ROM Program Table.

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DP8350 Series Option Program Table (Notes 1, 2, and 3)

Item No.	Parameter		Value	
1	Character (Font Size)	Dots per Character		
2		Scan Lines per Character		
3	Character Field (Block Size)	Dots per Character		
4		Scan Lines per Character		
5	Number of Video Characters per Row			
6	Number of Video Character Rows per Frame			
7	Number of Video Scan Lines (Item 4 x Item 6)			
8	Frame Refresh Rate (Hz) (two frequencies allowed)		f1 =	f0 =
9	Delay after/before Vertical Blank start to start of Vertical Sync (+/– Number of Scan Lines)			
10	Vertical Sync Width (Number of Scan Lines)			
11	Delay after Vertical Blank start to start of Video (Number of Scan Lines)			
12	Total Scan Lines per Frame (Item 7 + Item 11 = Item 13 ÷ Item 8)			
13	Horizontal Scan Frequency (Line Rate) (kHz) Item 8 x Item 12)			
14	Number of Character Times per Scan Line			
15	Character Clock Rate (MHz) Item 13 x Item 14)			
16	Character Time (ns) (1 ÷ Item 15)			
17	Delay after/before Horizontal Blank start to Horizontal Sync Start (+/– Character Times)			
18	Horizontal Sync Width (Character Times)			
19	Dot Frequency (MHz) (Item 3 x Item 15)			
20	Dot Time (ns) (1 ÷ Item 19)			
21	Vertical Blanking Stop before start of Video (Number of Scan Lines) (Range = Item 4 – 1 line to 0 lines)			
22	Cursor Enable on all Scan Lines of a Row? (Yes or No) If not, which Line?			
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)			
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)			
25	Serration Pulse Width, if used (Character Times)			
26	Horizontal Sync Pulse Active state logic level (1 or 0)			
27	Vertical Sync Pulse Active state logic level (1 or 0)			
28	Vertical Blanking Pulse Active state logic level (1 or 0)			

Note 1: If the Cursor Enable, Item 22, is active on only one line of a character row, then Item 21 must be either "1" or "0" unless it is the same as the line selected for Cursor Enable.

Note 2: Item 24 x Item 20 should be > 250 ns.

Note 3: Item 11 must be greater than Item 4 + 1.

DP8350 Series Option Program Table

DP8350 Option: 80 Characters x 24 Rows, 5 x 7 Character Font, 7 x 10 Character Field

Item No.	Parameter		Value	
1	Character (Font Size)	Dots per Character	5	
2		Scan Lines per Character	7	
3	Character Field (Block Size)	Dots per Character	7	
4		Scan Lines per Character	10	
5	Number of Video Characters per Row		80	
6	Number of Video Character Rows per Frame		24	
7	Number of Video Scan Lines (Item 4 x Item 6)		240	
8	Frame Refresh Rate (Hz) (two frequencies allowed)		f1 = 60 Hz	f0 = 50 Hz
9	Delay after/before Vertical Blank start to start of Vertical Sync (+/– Number of Scan Lines)		4	30
10	Vertical Sync Width (Number of Scan Lines)		10	10
11	Delay after Vertical Blank start to start of Video (Number of Scan Lines)		20	72
12	Total Scan Lines per Frame (Item 7 + Item 11 = Item 13 ÷ Item 8)		260	312
13	Horizontal Scan Frequency (Line Rate) (kHz) Item 8 x Item 12)		15.6 kHz	
14	Number of Character Times per Scan Line		100	
15	Character Clock Rate (MHz) Item 13 x Item 14)		1.56 MHz	
16	Character Time (ns) (1 ÷ Item 15)		641 ns	
17	Delay after/before Horizontal Blank start to Horizontal Sync Start (+/– Character Times)		0	
18	Horizontal Sync Width (Character Times)		43	
19	Dot Frequency (MHz) (Item 3 x Item 15)		10.920 MHz	
20	Dot Time (ns) (1 ÷ Item 19)		91.6 ns	
21	Vertical Blanking Stop before start of Video (Number of Scan Lines) (Range = Item 4 – 1 line to 0 lines)		1	
22	Cursor Enable on all Scan Lines of a Row? (Yes or No) If not, which Line?		Yes	
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)		No	
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)		4	
25	Serration Pulse Width, if used (Character Times)		–	
26	Horizontal Sync Pulse Active state logic level (1 or 0)		1	
27	Vertical Sync Pulse Active state logic level (1 or 0)		0	
28	Vertical Blanking Pulse Active state logic level (1 or 0)		1	

FULL/HALF ROW CONTROL (PIN 5)

Device pin 5 converts the DP8350 programmed display from 80 characters by 24 rows to 80 characters by 12 rows.

Full/Half Row (Pin 5) Logic State	Display Size
1	80 by 24
0	80 by 12

With pin 5 in logic "0" state, the 12 character rows are equally spaced vertically on the CRT. Each row is spaced by one full row of blanked video.

Also in this mode the address counter outputs address the same memory space for two rows — the video row and the blanked row. Thus one half of the CRT memory space is addressed with pin 5 in logic "0" state as compared to pin 5 in logic "1" state.

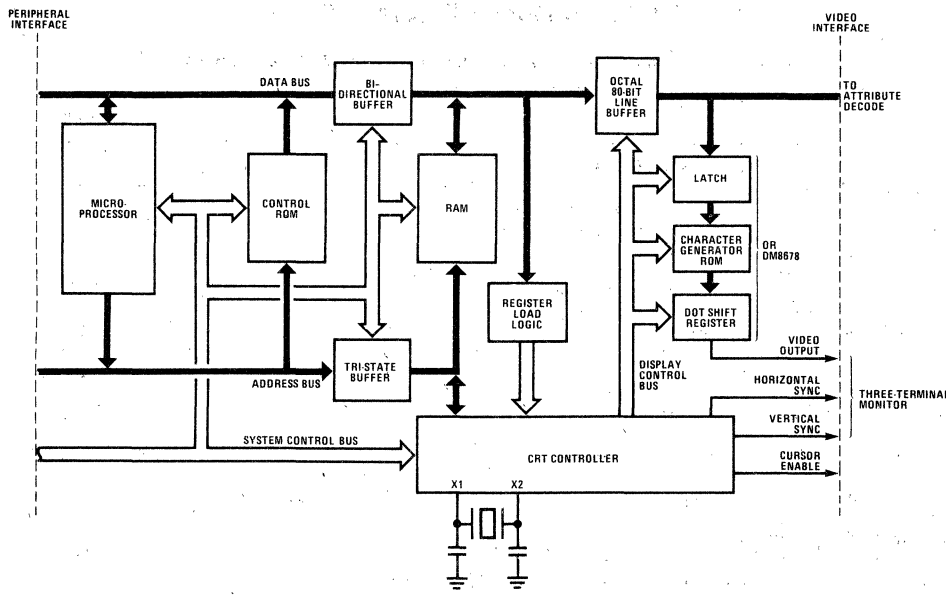


Figure 6. System Diagram Using a Line Buffer

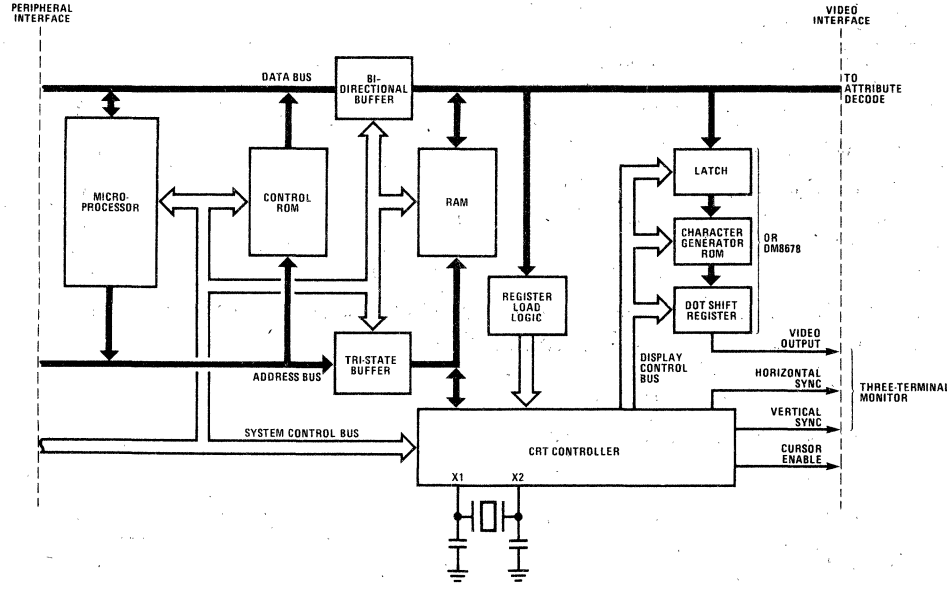


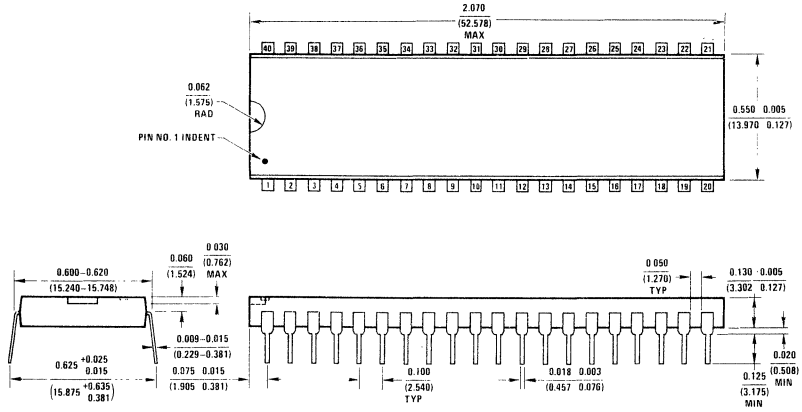
Figure 7. System Diagram with no Line Buffer

Note 1: If the Cursor Enable, Item 22, is active on only one line of a character row, then Item 21 must be either "1" or "0" unless it is the same as the line selected for Cursor Enable.

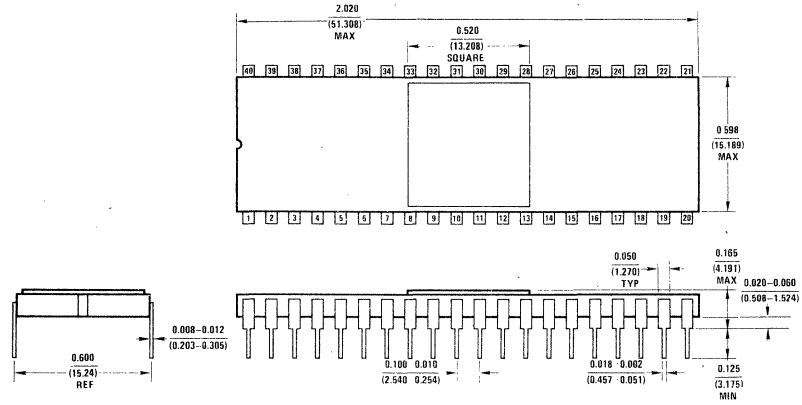
Note 2: Item 24 x Item 20 should be > 250 ns.

Note 3: Item 11 must be greater than Item 4 + 1.

Physical Dimensions



40-Lead Molded DIP (N)
NS Package Number N40A



40-Lead Cavity DIP (D)
NS Package Number D40C

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INS1771-1 Floppy Disk Formatter/Controller

General Description

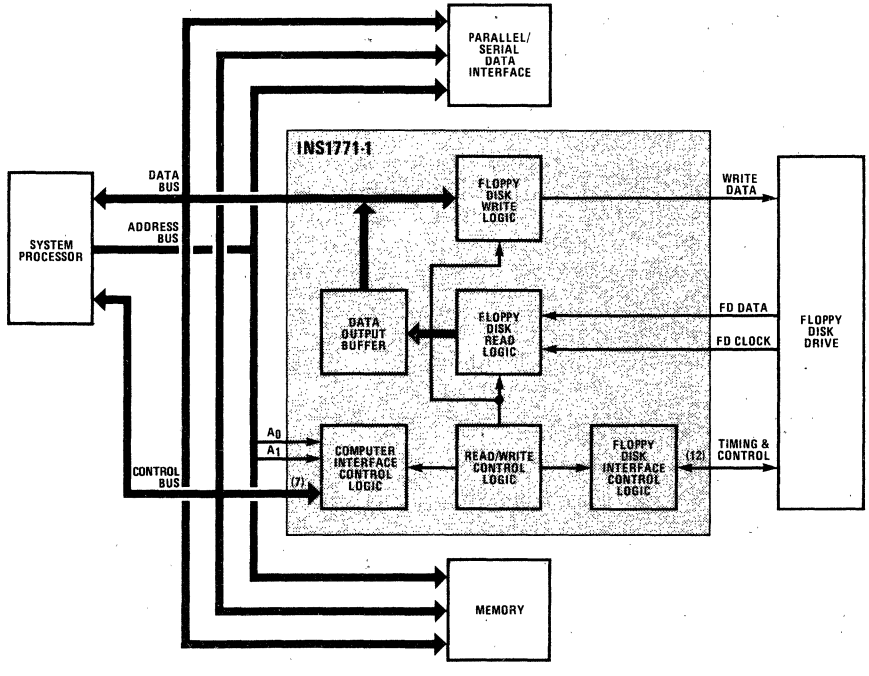
The INS1771-1 is a programmable floppy disk formatter/controller chip contained in a standard 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, interfaces a floppy disk drive directly to a computer interface bus. The INS1771-1 provides soft sector formatting, which may be either IBM 3740 compatible or a user-selected sector format.

The INS1771-1 is designed to operate on a multiplexed, TRI-STATE® 8-bit bidirectional bus with other bus-oriented devices. The chip is programmed by the system software via the bus and all data, status information, and control words are transferred over the bus lines.

Features

- Soft Sector Format Compatibility
- Automatic Track Seek with Verification
- Provisions for Miniature Floppy Disk Interface
- Read Mode Capabilities
  - Single/Multiple Record Read with Automatic Sector Search or Entire Track Read
  - Selectable 128-Byte or Variable Record Length
- Write Mode Capabilities
  - Single/Multiple Record Write with Automatic Sector Search
  - Entire Track Write for Diskette Initialization
- Programmable Controls
  - Selectable Track-to-Track Stepping Time
  - Selectable Head Settling and Head Engage Times
  - Selectable Three Phase or Step and Direction and Head Positioning Motor Controls
- Double Buffering of Data
- TTL Compatible
- DMA or Programmed Data Transfers
- Reduces System Component Count
- On-Chip CRC Generation and Checking
- Direct Plug-in Replacement for Western Digital FD1771-1

INS1771-1 General System Configuration



Absolute Maximum Ratings

V_{DD} with Respect to V_B . . . . . +20 V to −0.3 V
Max Voltage to Any Input with Respect to V_{BB} . . . +20 V to −0.3 V
Operating Temperature. . . . . 0°C to +70°C
Storage Temperature . . . . . −55°C to +125°C

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = +12.0 V ± 0.6 V, V_{BB} = −5.0 V ± 0.25 V, V_{SS} = 0 V, V_{CC} = +5 V ± 0.25 V, I_{DD} = 10 mA nominal, I_{CC} = 30 mA nominal, I_{BB} = 0.4 nA nominal.

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	μA	$V_{OUT} = V_{DD}$
V_{IH}	Input High Voltage	2.6			V	
V_{IL}	Input Low Voltage (All Inputs)			0.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = −100 μA
V_{OL}*	Output Low Voltage			0.45	V	I_O = 1.6 mA

Note: $V_{OL} \leq 0.4$ V when interfacing with low-power Schottky parts ($I_O < 1$ mA).

*V_{OL} = 0.5 V on WG.

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = +12 V ± 0.6 V, V_{BB} = −5 V ± 0.25 V, V_{SS} = 0 V, V_{CC} = +5 V ± 0.25 V.

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions
Read Operations						
t_{ET}	Setup ADDR & $\overline{CS}$ to $\overline{RE}$	100			ns	
t_{HLD}	Hold ADDR & $\overline{CS}$ from $\overline{RE}$	10			ns	
t_{RE}	$\overline{RE}$ Pulse Width	500			ns	C_L = 25 pF
t_{DRR}	DRQ Reset from $\overline{RE}$			500	ns	
t_{IRR}	INTRQ Reset from $\overline{RE}$			3000	ns	
t_{DACC}	Data Access from $\overline{RE}$			450	ns	C_L = 25 pF
t_{DOH}	Data Hold from $\overline{RE}$	50		150	ns	C_L = 25 pF
Write Operations						
t_{SET}	Setup ADDR & $\overline{CS}$ to $\overline{WE}$	100			ns	
t_{HLD}	Hold ADDR & $\overline{CS}$ from $\overline{WE}$	10			ns	
t_{WE}	$\overline{WE}$ Pulse Width	350			ns	
t_{DRR}	DRQ Reset from $\overline{WE}$			500	ns	
t_{IRR}	INTRQ Reset from $\overline{WE}$			3000	ns	(see note)
t_{DS}	Data Setup to $\overline{WE}$	250			ns	
t_{DH}	Data Hold from $\overline{WE}$	150			ns	

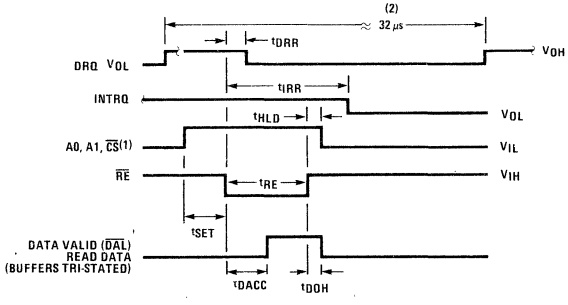
AC Electrical Characteristics (cont.)

T_A = 0°C to +70°C, V_{DD} = +12 V ± 0.6 V, V_{BB} = −5 V ± 0.25 V, V_{SS} = 0 V, V_{CC} = +5 V ± 0.25 V.

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions
External Data Separation ($\overline{XTDS}$ = 0)						
t_{PWX}	Pulse Width Rd Data & Rd Clock	150		350	ns	
t_{CX}	Clock Cycle Ext	2500			ns	
t_{DEX}	Data to Clock	500			ns	
t_{DDX}	Data to Data Cycle	2500			ns	
Internal Data Separation ($\overline{XTDS}$ = 1)						
t_{PWI}	Pulse Width Data & Clock	150		1000	ns	
t_{CI}	Clock Cycle Internal	3500		5000	ns	
Write Data Timing						
t_{WGD}	Write Gate to Data		1200		ns	300 ns ± CLK tolerance
t_{PWW}	Pulse Width Write Data	500		600	ns	
t_{CDW}	Clock to Data		2000		ns	±0.5% ± CLK tolerance
t_{CW}	Clock Cycle Write		4000		ns	±0.5% ± CLK tolerance
t_{WGH}	Write Gate Hold to Data	0		100	ns	
Miscellaneous Timing						
t_{CD1}	Clock Duty	175			ns	2 MHz ± 1% (see note)
t_{CD2}	Clock Duty	210			ns	
t_{STP}	Step Pulse Output	3800		4200	ns	
t_{DIR}	Dir Setup to Step	24			µs	
t_{MR}	Master Reset Pulse Width	10			µs	These times doubled when CLK = 1 MHz
t_{IP}	Index Pulse Width	10			µs	
t_{WF}	Write Fault Pulse Width	10			µs	

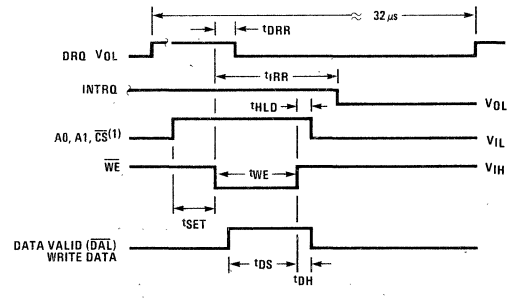
Note: Timings are given for 2 MHz Clock. For those timings noted, values will double when chip is operated at 1 MHz.

Timing Waveforms



NOTES:
1. $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED.
2. FOR READ TRACK COMMAND, THIS TIME MAY BE 12 TO 32 µs WHEN $\overline{S}$ = 0. (THIS TIME DOUBLES WHEN CLK = 1 MHz.)

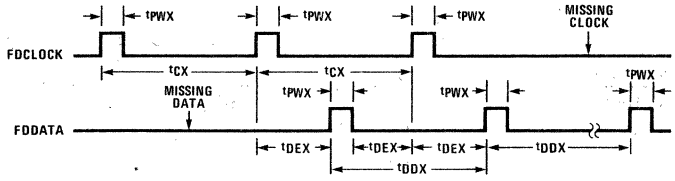
Read Enable Timing



NOTES:
1. $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED.
2. WHEN WRITING DATA INTO SECTOR, TRACK, OR DATA REGISTER, USER CANNOT READ THIS REGISTER UNTIL AT LEAST 8 µs AFTER THE RISING EDGE OF $\overline{WE}$. WHEN WRITING INTO THE COMMAND REGISTER, STATUS IS NOT VALID UNTIL SOME 12 µs LATER. THESE TIMES ARE DOUBLED WHEN CLK = 1 MHz.

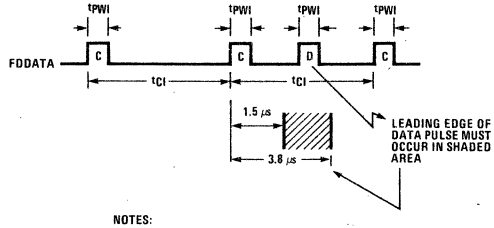
Write Enable Timing

Timing Waveforms (cont.)



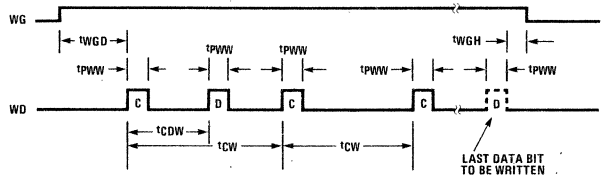
NOTES:
1. ABOVE TIMES ARE DOUBLED WHEN CLK = 1 MHz.
2. CONTACT NSC FOR EXTERNAL CLOCK/DATA SEPARATOR CIRCUITS.

Read Timing ($\overline{XTDS}$ = 0)

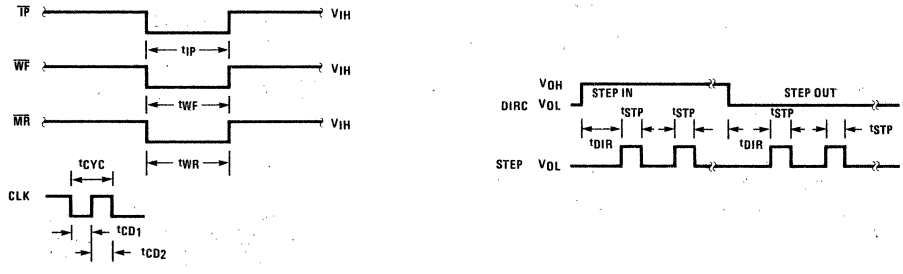


NOTES:
1. INTERNAL DATA SEPARATION MAY WORK FOR SOME APPLICATIONS. HOWEVER, FOR APPLICATIONS REQUIRING HIGH DATA RECOVERY RELIABILITY, NSC RECOMMENDS THAT EXTERNAL DATA SEPARATION BE USED.
2. FDCLOCK MUST BE TIED HIGH.

Read Timing ($\overline{XTDS}$ = 1)

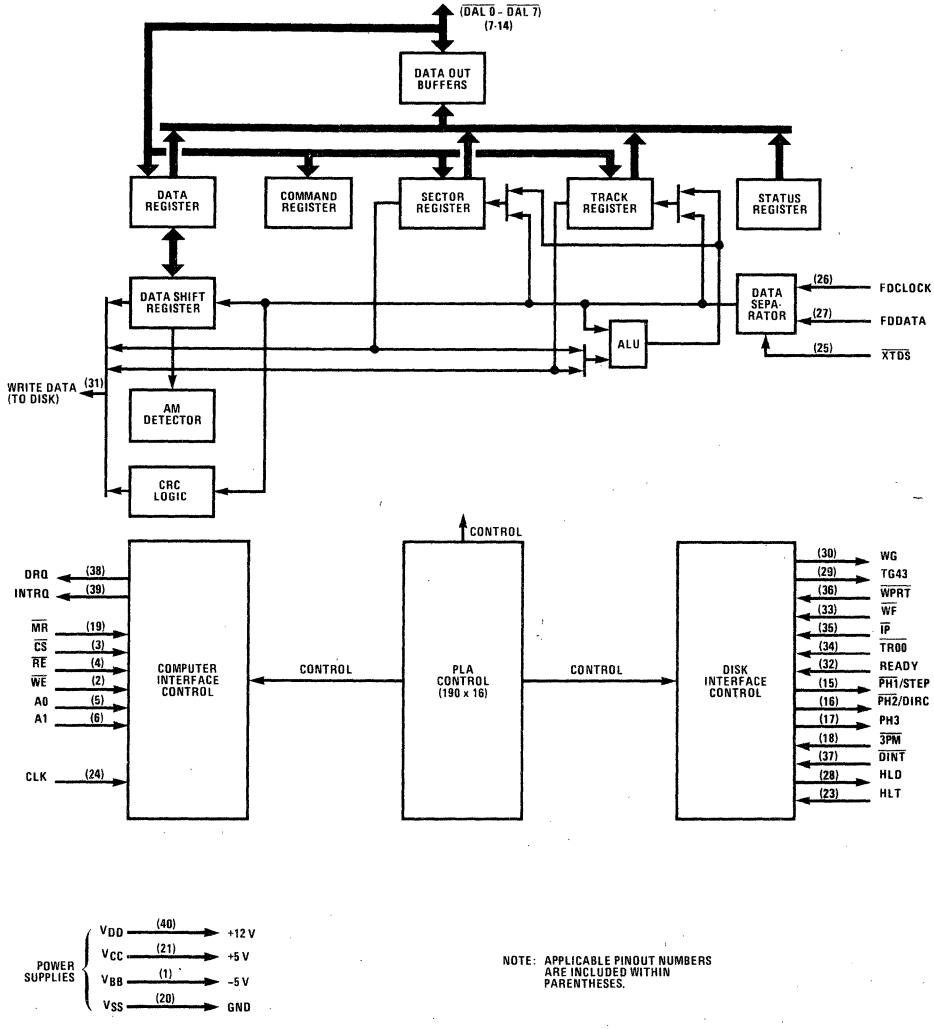


Write Data Timing



Miscellaneous Timing

INS1771-1 Block Diagram



INS1771-1 Functional Pin Definitions

The following describes the function of all INS1771-1 input/output pins. Some of these descriptions reference internal circuits.

NOTE

In the following descriptions, a low represents a logic 0 (0 Volt nominal) and a high represents a logic 1 (+5 Volts nominal).

INPUT SIGNALS

Chip Select ($\overline{CS}$): When low, the chip is selected. This enables communication between the INS1771-1 and the CPU.

Read Enable ($\overline{RE}$): When low coincident with an active (low) $\overline{CS}$ input, allows the CPU to read data or status information from a selected register of the chip.

D.3

Functional Pin Definitions (cont.)

Write Enable ($\overline{WE}$): When low coincident with an active (low) $\overline{CS}$ input, allows the CPU to write data or control words into a selected register of the chip.

Register Select (A_0, A_1) Lines: These two inputs are used in conjunction with either an active (low) $\overline{RE}$ or $\overline{WE}$ input to select an INS1771-1 register to read from or write into as indicated below.

A_1	A_0	$\overline{RE}$	$\overline{WE}$	Selected Register
0	0	0	1	Status Register
0	0	1	0	Command Register
0	1	0	1	Track Register
0	1	1	0	
1	0	0	1	Sector Register
1	0	1	0	
1	1	0	1	Data Register
1	1	1	0	

Master Reset ($\overline{MR}$): When low, clears the Command Register, resets bit 7 (Not Ready) of the Status Register low, and makes the $\overline{PH1}$/STEP output active low. When the $\overline{MR}$ returns high, a Restore command is executed (regardless of the state of the Ready input from the floppy disk drive).

Clock (CLK): This input pin requires a 2-megahertz (±1%) squarewave clock as a reference for all internal timing.

NOTE

For a miniature floppy disk, a 1-MHz (±1%) squarewave clock is required.

External Data Separator ($\overline{XTDS}$): When low, the composite read disk serial data (data bits and clock) from the floppy disk drive is separated externally by the user. When high or open, the composite read disk data is separated by the internal data separator of the chip.

Floppy Disk Data (FDDATA): This input pin provides either of the following serial data: both clock and data bits (composite read disk data) when the $\overline{XTDS}$ input is high; or externally separated data bits when the $\overline{XTDS}$ input is low.

Floppy Disk Clock (FDCLK): This input pin provides the externally separated clock when the $\overline{XTDS}$ input is low. The FDCLK input should be connected to +5 Volts (logic 1) when the $\overline{XTDS}$ input is high.

Write Protect ($\overline{WPRT}$): When low, immediately terminates a Write command and sets bit 6 (Record Type/Write Protect) of the Status Register high. In addition, an interrupt is generated when the $\overline{WPRT}$ input is low. The $\overline{WPRT}$ input is sampled whenever a Write command is received from the CPU.

Write Fault ($\overline{WF}$): When low coincident with an active (high) Write Gate (WG) output, causes the current Write command to be terminated and sets bit 5 (Record Type/Write Fault) of the Status Register high. The $\overline{WF}$ input should be made inactive (high) coincident with an inactive (low) WG output. If not used, tie high.

Index Pulse ($\overline{IP}$): Goes low for 10 microseconds (minimum) whenever an index mark is encountered (once per revolution) on the diskette.

Track 00 ($\overline{TR00}$): Goes low whenever the Read/Write head is positioned over track 00 of the diskette.

Ready: When high before the execution of a Read or Write command, indicates that the floppy disk drive is ready for a Read or Write operation. When low, the Read or Write operation is not performed and an interrupt is generated. However, a Seek operation is always performed. The complement of the Ready input appears as bit 7 (Not Ready) of the Status Register.

Three-Phase Motor Select ($\overline{3PM}$): When low, the three-phase motor control interface is selected for the floppy disk drive by the INS1771-1. When high or open, the step-direction motor control interface is selected by the INS1771-1.

Disk Initialization ($\overline{DINT}$): When low coincident with a Write Track command from the CPU, causes the Write Track operation to be terminated and bit 6 (Record Type/Write Protect) of the Status Register to be set high.

Test: This input pin is normally tied to +5 Volts. However, it may be used to disable the programmed stepping rate delays for testing the INS1771-1 or for disk drives that do not require the long delay times to change tracks. These delays are disabled by tying the Test input to ground.

Head Load Timing (HLT): When high, the Read/Write head is assumed to be engaged against the recording medium (diskette). The HLT input is sampled after each 10 millisecond internal delay after HLD is asserted.

V_{BB}: -5 Volt supply.

V_{CC}: +5 Volt supply.

V_{DD}: +12 Volt supply.

V_{SS}: Ground (0 Volt) reference.

OUTPUT SIGNALS

Data Request (DRQ): Open-drain output to the CPU that goes high when the INS1771-1 is ready to transfer a byte of data during a Read or Write operation. The DRQ output is reset low upon the completion of a byte Read or Write operation.

Interrupt Request (INTRQ): Open-drain output to the CPU that goes high at the completion or termination of any operation. The INTRQ output is reset low when a new command is loaded into the Command Register, or Status Register Read.

Write Data (WD): Composite write disk data (both clock and data bits of 500 nanoseconds in duration) output to the floppy disk drive. The WD output can drive two TTL loads.

Write Gate (WG): Active (high) whenever data is to be written on the diskette. As a precaution to erroneous writing, the first data byte must be loaded into the Data Register (in response to a DRQ output from the INS1771-1) before the WG output can be activated.

Functional Pin Definitions (cont.)

Track Greater Than 43 (TG43): When high during a Read or Write operation, informs the floppy disk drive that the Read/Write head is positioned between tracks 44 and 76.

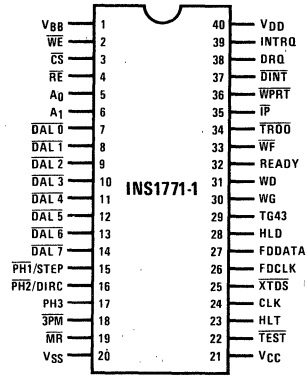
Three-Phase Motors/Step-Direction Motors Control Lines ($\overline{PH1}$/STEP, $\overline{PH2}$/DIRC, PH3): These three control lines provide either of the following outputs: successive three-phase pulses (active high PH3 signal and active low $\overline{PH1}$ and $\overline{PH2}$ signals) over the lines for three-phase stepping motors; or a level over the $\overline{PH2}$/DIRC line (high level for stepping in and low level for stepping out) and 4 microsecond high-level pulses over the $\overline{PH1}$/STEP line to determine the direction and stepping rate for step-direction motors. For direction control of three-phase motors, the stepping sequence is 1-2-3-1 when stepping in and 1-3-2 when stepping out. The particular motor interface selected is determined by the hardwiring of the $\overline{3PM}$ input. The $\overline{PH1}$/STEP output is made active low after a master reset.

Head Load (HLD): High-level output that controls the loading of the Read/Write head against the recording medium (diskette). A Read or Write operation does not occur until a high-level HLT input is sampled by the INS1771-1. The HLD becomes active at the beginning of a Read, Write (E flag is set high) or Verify operation, or a Seek or Step Operation with the H flag set high; it remains active until the third index pulse following the last operation that used the head.

INPUT/OUTPUT SIGNALS

Data Access Lines (DAL) Bus: This TRI-STATE bus comprises eight inverted input/output lines ($\overline{DAL0}$ - $\overline{DAL7}$). The bus provides bidirectional communications between the CPU and the INS1771-1. Data, control words and status information are transferred via the DAL Bus.

Pin Configuration



INS1771-1 Commands

The INS1771-1 accepts and executes the eleven commands listed and summarized in table 1. Flags associated with these commands are summarized in table 2. With the exception of the Force Interrupt command, a command word should be loaded into the internal Command Register only when bit 0 (Busy) of the Status Register is inactive (low). Whenever a command is being executed, the Busy status bit is set high. When a command is completed or an error condition exists, an interrupt is generated and the Busy status bit is reset low. The Status Register indicates whether a completed command encountered an error or was fault free.

As indicated in table 1, the eleven commands accepted and executed by the INS1771-1 are divided into four types. The following paragraphs describe the eleven commands under these four divisions.

TYPE I COMMANDS

Type I Commands are basically head positioning commands and include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate (r_1r_0) field (bits 0 and 1) that determines the stepping motor rate as defined in the table below:

r_1	r_0	CLK = 2 MHz TEST = 1	CLK = 1 MHz TEST = 1	CLK = 2 MHz TEST = 0	CLK = 1 MHz TEST = 0
0	0	6 ms	12 ms	≈ 400 μs	≈ 800 μs
0	1	6 ms	12 ms		
1	0	10 ms	20 ms		
1	1	20 ms	40 ms		

The Type I Commands contain a head load (h) flag (bit 3) that determines whether or not the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command (HLD output made active high). If h = 0, the HLD output is made inactive low. Once the head is loaded (HLD is active), the head will remain engaged until the INS1771-1 receives a command that specifically disengages the head. If the INS1771-1 does not receive any commands after two revolutions of the disk, the head will be disengaged (HLD made inactive). The Head Load Timing (HLT) input is only sampled after a 10 millisecond delay, when actual reading or writing on the diskette is to occur. Note that a verification, described below, requires reading off the diskette.

The Type I Commands also contain a verification (V) flag (bit 2) that determines whether or not verification is to take place on the last track. If V = 0, no verification is performed. If V = 1, a verification is performed.

During verification, the head is loaded (HLD is active) and after an internal 10 millisecond delay, the HLT input is sampled. When the HLT input is active (high),

Table 1. Commands Summary

Type	Command	Bits							
		7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	$\bar{s}$
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

Table 2. Command Flags Summary

h = Head Load flag (bit 3 of Type I)

h = 1, Load head at beginning
h = 0, Do not load head at beginning

V = Verify flag (bit 2 of Type I)

V = 1, Verify on last track
V = 0, No verify

r_1r_0 = Stepping Motor Rate (bits 1 - 0 of Type I)

r_1r_0 = 00, 6 ms between steps
r_1r_0 = 01, 6 ms between steps
r_1r_0 = 10, 10 ms between steps
r_1r_0 = 11, 20 ms between steps

u = Update flag (bit 4 of Type I)

u = 1, Update Track Register
u = 0, No update

m = Multiple Record flag (bit 4 of Type II)

m = 0, Single Record
m = 1, Multiple Records

b = Block Length flag (bit 3 of Type II)

b = 1, IBM format (128 to 1024 bytes)
b = 0, Non-IBM format (16 to 4096 bytes)

E = Enable HLD & 10 ms delay (bit 2 of Type II)

E = 1, Enable HLD, HLT & 10 ms delay
E = 0, Head is assumed engaged & no 10 ms delay

a_1a_0 = Data Address Mark (bits 1 - 0 of Type II)

a_1a_0 = 00, FB (Data Mark)
a_1a_0 = 01, FA (Data Mark)
a_1a_0 = 10, F9 (Data Mark)
a_1a_0 = 11, F8 (Data Mark)

$\bar{s}$ = Synchronize flag (bit 0 of Type III)

$\bar{s}$ = 0, Synchronize to AM
$\bar{s}$ = 1, Do not synchronize to AM

I_n = Interrupt Condition flags (bits 3 - 0 of Type IV)

I_0 = 1, Not Ready to Ready Transition
I_1 = 1, Ready to Not Ready Transition
I_2 = 1, Index Pulse
I_3 = Immediately

INS1771-1 Commands (cont.)

the first encountered ID field is read off the diskette. The track address of the ID field is then compared to the Track Register. If there is a match and a valid ID CRC, the verification is complete, an interrupt is generated, and the Busy status bit is reset. If there is not a match and a valid ID CRC, an interrupt is generated, the Seek Error status bit (bit 4) is set high, and the Busy status bit is reset low. If there is not a valid CRC, the CRC Error status bit (bit 3) is set high, and the next encountered ID field is read off the diskette for verification. If an ID field with a valid CRC cannot be found after four revolutions of the diskette, the INS1771-1 terminates the operation and sends an interrupt (INTRQ) signal to the CPU.

The Step, Step-In and Step-Out commands contain an update (u) flag (bit 4). When u = 1, the Track Register is updated by one for each step. When u = 0, the Track Register is not updated.

Restore (Seek Track 0): Upon receipt of this command, the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low (indicating the Read/Write head is positioned over track 0), the Track Register is loaded with zeros and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses at a rate specified by the r_1r_0 field (bits 0 and 1) are issued until the $\overline{TR00}$ input is active low. At this time, the Track Register is loaded with zeros and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the INS1771-1 gives up and interrupts with the Seek Error status bit set. Note that the Restore command is executed when the $\overline{MR}$ input goes from an active (low) to an inactive (high) state. A verification operation takes place if the V flag (bit 2) is set. The setting of the h flag (bit 3) allows the head to be loaded at the start of the command.

Seek: This command assumes that the Track Register contains the track number of the current position of the Read/Write head and that the Data Register contains the desired track number. The INS1771-1 will update the Track Register and issue stepping pulses in the appropriate direction until the contents of the Track Register are equal to the contents of the Data Register. A verification operation takes place if the V flag (bit 2) is set. The setting of the h flag (bit 3) allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step: Upon receipt of this command, the INS1771-1 issues one stepping pulse to the floppy disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field (bits 0 and 1), a verification takes place if the V flag (bit 2) is set. If the u flag (bit 4) is set, the Track Register is updated. The setting of the h flag (bit 3) allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

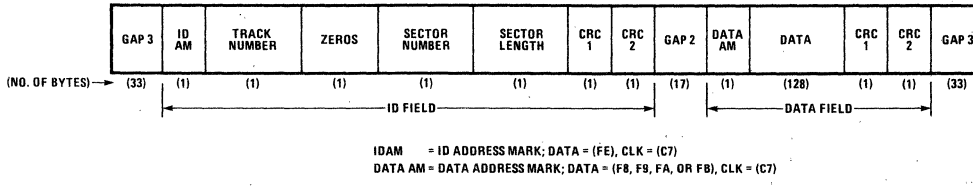
Step-In: Upon receipt of this command, the INS1771-1 issues one stepping pulse in the direction towards track 76. If the u flag (bit 4) is set, the Track Register is decremented by one. After a delay determined by the r_1r_0 field (bits 0 and 1), a verification takes place if the V flag (bit 2) is set. The setting of the h flag (bit 3) allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step-Out: Upon receipt of this command, the INS1771-1 issues one stepping pulse in the direction towards track 0. If the u flag (bit 4) is set, the Track Register is decremented by one. After a delay determined by the r_1r_0 field (bits 0 and 1), a verification takes place if the V flag (bit 2) is on. The setting of the h flag (bit 3) allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands include the Read sector(s) and Write sector(s) commands. Prior to loading the Type II Commands into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II Commands, the Busy status bit is set. If the E flag (bit 2) = 1 (this is the normal case), HLD is made active and HLT is sampled after an internal 10 millisecond delay. If the E flag = 0, the head is assumed engaged and there is no internal 10 millisecond delay.

When an ID field (see figure 1) is located on the diskette, the INS1771-1 compares the Track Number of the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is made. If there is a match, the sector number of the ID field is then compared with the Sector Register. If there is not a match, the next encountered ID field is read and a comparison is made. If there is a match, the CRC field is read. (The polynomial for the CRC is $G(x) = x^{16} + x^{12} + x^5 + 1$. The CRC includes all the information starting with the address mark and up to the CRC characters.) If there is a CRC error, the CRC Error status bit is set and the next ID field is read off the diskette and comparisons are made. If the CRC is correct, the data field is located and will be either written or read, depending upon command. The INS1771-1 must find an ID field with a valid track number, sector number, and CRC within four revolutions of the diskette; otherwise, the Record Not Found status bit (bit 4) is set and the command is terminated with an interrupt.



IDAM = ID ADDRESS MARK; DATA = (FE), CLK = (C7)
DATA AM = DATA ADDRESS MARK; DATA = (F8, F9, FA, OR FB), CLK = (C7)

Figure 1. IBM 3740 ID Field and Data Field Formats

Each of the Type II Commands contains a b flag (bit 3), which in conjunction with the sector length field contents of the ID, determines the length (number of characters) of the data field. For IBM 3740 compatibility, the b flag (bit 3) should equal 1. The numbers of bytes in the data field (sector) is then 128×2^n where n = 0, 1, 2, or 3.

For b = 1:

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

When the b flag (bit 3) equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field as shown below:

For b = 0:

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
01	16
02	32
03	48
04	64
•	•
•	•
•	•
FF	4080
00	4096

Each of the Type II Commands also contains an m flag (bit 4) that determines whether multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the Sector Register internally updated so that an address verification can occur on the next record. The INS1771-1 continues to read or write multiple records and update the Sector Register until the Sector Register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register. When either of these occurs, the command is terminated and an interrupt is generated.

Read Command: Upon receipt of this command, the Read/Write head is loaded and the Busy status bit is set. Then, when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is inputted to the computer. The Data Address Mark of the data field must be found within 28 bytes of the correct ID field. If not, the Record Not Found status bit is set and the operation is terminated. When the first character or byte of the data field has been shifted through the Data Shift Register, it is transferred to the Data Register and a Data Request (DRQ) output is generated. When the next byte is loaded into the Data Shift Register, it is transferred to the Data Register and another DRQ output is generated, provided that the CPU has previously read the Data Register. If one or more characters are lost, the Lost Data status bit is set. This sequence continues until the data field has been inputted to the computer. If there is a CRC error in the data field, the CRC Error status bit is set, and the command is terminated (even if it is a multiple record command). At the end of the operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (bits 5 and 6) as shown below:

Status Bit 5	Status Bit 6	Data AM (hex)
0	0	FB
0	1	FA
1	0	F9
1	1	F8

Write Command: Upon receipt of this command, the Read/Write head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ output is generated. The INS1771-1 counts off 11 bytes from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the Data Register has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of all Zero levels are then written on the diskette. At this time, the Data Address Mark is then written on the diskette, as determined by the a_1a_0 field (bits 0 and 1) of the command as shown below:

a_1	a_0	Data Mark (hex)	Clock Mark (hex)
0	0	FB	C7
0	1	FA	C7
1	0	F9	C7
1	1	F8	C7

The INS1771-1 then writes the data field by generating DRQ outputs to the computer. If the DRQ is not serviced in time, the Lost Data status bit is set and a byte of zeros is written on the diskette. The command is not terminated. After the last data byte has been written on the diskette, the two-byte CRC is computed internally and written on the diskette followed by one byte of all One levels. WG is then made inactive.

TYPE III COMMANDS

Read Address: Upon receipt of this command, the head is loaded and the Busy status bit is set. The next encountered ID field is then read in off the diskette, and the six data bytes of the ID field are assembled and transferred to the Data Register, and a DRQ output is generated for each byte. (The six bytes of the ID field are shown in figure 1.)

Although the CRC characters are inputted to the computer, the INS1771-1 checks for validity and the CRC Error status bit is set if there is a CRC error. The Sector Address of the ID field is written into the Sector Register. At the end of the operation, an interrupt is generated and the Busy status bit is reset.

INS1771-1 Commands (cont.)

Read Track: Upon receipt of this command, the head is loaded and the Busy status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled, it is transferred to the Data Register and the Data Request (DRQ) output is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If the $\bar{s}$ flag (bit 0) of the command is a low, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

The INS1771-1 handles single density frequency modulated (FM) data. Each data cell is defined by clock pulses. A pulse recorded between clock pulses indicates the presence of a logic 1 bit; the absence of this pulse is interpreted as a logic 0 bit. The Address Marks for Index, ID, and Data are identified by a particular pattern not repeated in the remainder of the ID field or Data field. This is accomplished by reading patterns that are recorded with missing clock bits (logic 0) as shown below:

For initialization:

Write 2 CRC Characters	Data	1 1 1 1 0 1 1 1 = F7
	Clock	1 1 1 1 1 1 1 1 = FF
Index Address Mark	Data	1 1 1 1 1 1 0 0 = FC
	Clock	1 1 0 1 0 1 1 1 = D7
ID Address Mark	Data	1 1 1 1 1 1 1 0 = FE
	Clock	1 1 0 0 0 1 1 1 = C7
Data Address Mark	Data	1 1 1 1 1 0 1 1 = F9 - FB
	Clock	1 1 0 0 0 1 1 1 = C7
Deleted Data Address Mark	Data	1 1 1 1 1 0 0 0 = F8
	Clock	1 1 0 0 0 1 1 1 = C7
Spare	Data	1 1 1 1 1 1 0 1 = FD
	Clock	(user designated)

These patterns are used as synchronization codes by the INS1771-1 when reading data and are recorded by the formatting command (Write Track) when the INS1771-1 is presented with data F7 through FE.

Write Track: Upon receipt of this command, the head is loaded and the Busy status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request output is activated immediately upon receiving the command and writing does not start until after the first byte has been loaded into the Data Register. If the Data Register has not been loaded by the second index pulse, the operation is terminated. This sets the Not Busy and Lost Data status bits, and activates the interrupt. If a byte is not present in the Data Register when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the diskette by detecting certain data byte patterns in the outgoing data stream as shown above. The CRC generator is initialized to all Ones when any data byte from F8 to FE is about to be transferred from the Data Register to the Data Shift Register.

The Write Track command does not execute if the $\overline{\text{DINT}}$ input is grounded. Instead, the Write Protect status bit is set and the interrupt is activated. One F7 pattern in the Data Register generates 2 CRC characters.

TYPE IV COMMANDS

Force Interrupt: This command can be loaded into the Command Register at any time. If there is a current command under execution (Busy status bit is set), the command is terminated and an interrupt is generated when the condition specified in the I_0 through I_3 field (bits 0 through 3) is detected. More than one condition may be specified. The interrupt conditions are indicated below:

I_0 = Not Ready-to-Ready Transition
I_1 = Ready-to-Ready Transition
I_2 = Every Index Pulse
I_3 = Interrupt Occurs Immediately

NOTE

If I_0 through I_3 = 0, no interrupt is generated; however, the current command is terminated and the Busy status bit is reset.

INS1771-1 Status Register

An 8-bit register is provided in the INS1771-1 to hold device status information. This Status information varies according to the type of command executed as shown in table 3. The contents of the Status Register, which can be read into the DAL Bus by a Read operation, are described below.

Bit 0: When high (set), indicates that a command is under execution. When low (reset), indicates that no command is under execution.

Bit 1: For Type I Commands, this bit is the complement of the Index Pulse ($\overline{\text{IP}}$) input. When set, it indicates that an index mark has been detected on the diskette.

For Types II and III Commands, this bit is a copy of the Data Request (DRQ) output. When set, it indicates that the Data Register is full during a Read operation or that the Data Register is empty during a Write operation. Bit 1 is reset to zero when updated.

Bit 2: For Type I Commands, this bit is the complement of the Track 00 ($\overline{\text{TR00}}$) input. When set, it indicates that the Read/Write head is positioned over track 0.

For Types II and III Commands, this bit is set to indicate that the computer did not respond to the DRQ output from the INS1771-1 in one byte time. Bit 2 is reset to zero when updated.

Bit 3: For Type I Commands, this bit is set when one or more CRC errors were encountered on an unsuccessful Track Verification operation. Bit 3 is reset to zero when updated.

For Type II and III Commands, bit 3 is set when an error is found in one or more ID fields, while bit 4 is set. Bit 3 is reset low when updated.

Bit 4: For Type I Commands, this bit is set to indicate that the desired track was not verified. Bit 4 is reset low when updated.

For Type II and III Commands, bit 4 is set to indicate that the desired track and sector were not found. Bit 4 is reset low when updated.

Bit 5: For Type I Commands, this bit is set to indicate that the Read/Write head is loaded and engaged. Bit 5

INS1771-1 Commands (cont.)

is the logical AND of the Head Load (HLD) output and the Head Load Timing (HLT) input.

For Type II and III Commands, bit 5 indicates the following: the LSB of the record-type code from the data field address mark during execution of a Read Command; and a write fault during execution of a Write or Write Track Command. Bit 5 is reset low when updated.

Bit 6: For Type I Commands, this bit is the complement of the Write Protect ($\overline{WRPT}$) input. When set, it indicates that the write protect is activated.

For Type II and III Commands, bit 6 indicates the following: the MSB of the record-type code from the data field address mark during execution of a Read Command; and a write fault during execution of a Write or Write Track command. Bit 6 is reset low when updated.

Bit 7: When set, indicates that the floppy disk drive is not ready. When reset, indicates that the drive is ready. Bit 7 is the complement of the Ready input and is logically ORed with the Master Reset ($\overline{MR}$) input. The Types II and III Commands are not executed unless the floppy disk drive is ready.

Table 3. Status Register Summary

Bit	Commands					
	All Type I Commands	Read Address	Read	Read Track	Write	Write Track
S7	Not Ready	Not Ready	Not Ready	Not Ready	Not Ready	Not Ready
S6	Write Protect	0	Record Type	0	Write Protect	Write Protect
S5	Head Engaged	0	Record Type	0	Write Fault	Write Fault
S4	Seek Error	ID Not Found	Record Not Found	0	Record Not Found	0
S3	CRC Error	CRC Error	CRC Error	0	CRC Error	0
S2	Track 0	Lost Data	Lost Data	Lost Data	Lost Data	Lost Data
S1	Index	DRQ	DRQ	DRQ	DRQ	DRQ
S0	Busy	Busy	Busy	Busy	Busy	Busy

Programming Examples

Some examples of the software control of the INS1771-1 are shown in flowchart form. The first example (figure 2) shows the writing of information onto a particular track and sector. The second example (figure 3) shows accessing of information from successive sectors. The third example (figure 4) shows how information may be sought by using Track 00 as a table of contents.

INS1771-1 Operation

The following describes the operation of the INS1771-1. Use the block diagram on page 5, as necessary, to follow these descriptions.

INS1771-1 PROCESSOR INTERFACE

All commands, status and data are transferred over the TRI-STATE bidirectional DAL (Data Access Lines) Bus. The 8 lines of the DAL Bus ($\overline{DAL0}$ - $\overline{DAL7}$) present an open circuit to the comman processor peripheral bus until activated by the low-level $\overline{CS}$ (Chip Select) signal. An active $\overline{CS}$ combined with a low-level $\overline{RE}$ (Read Enable) sets the DAL Bus into the transmitter mode, while the $\overline{CS}$ combined with a low-level $\overline{WE}$ (Write Enable) sets the DAL Bus in the receiver mode.

When transfer of data with the INS1771-1 is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The least significant address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation, are interpreted as selecting the following registers:

A1	A0	Read ($\overline{RE}$)	Write ($\overline{WE}$)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the INS1771-1 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations, the Data Request (DRQ) output is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more

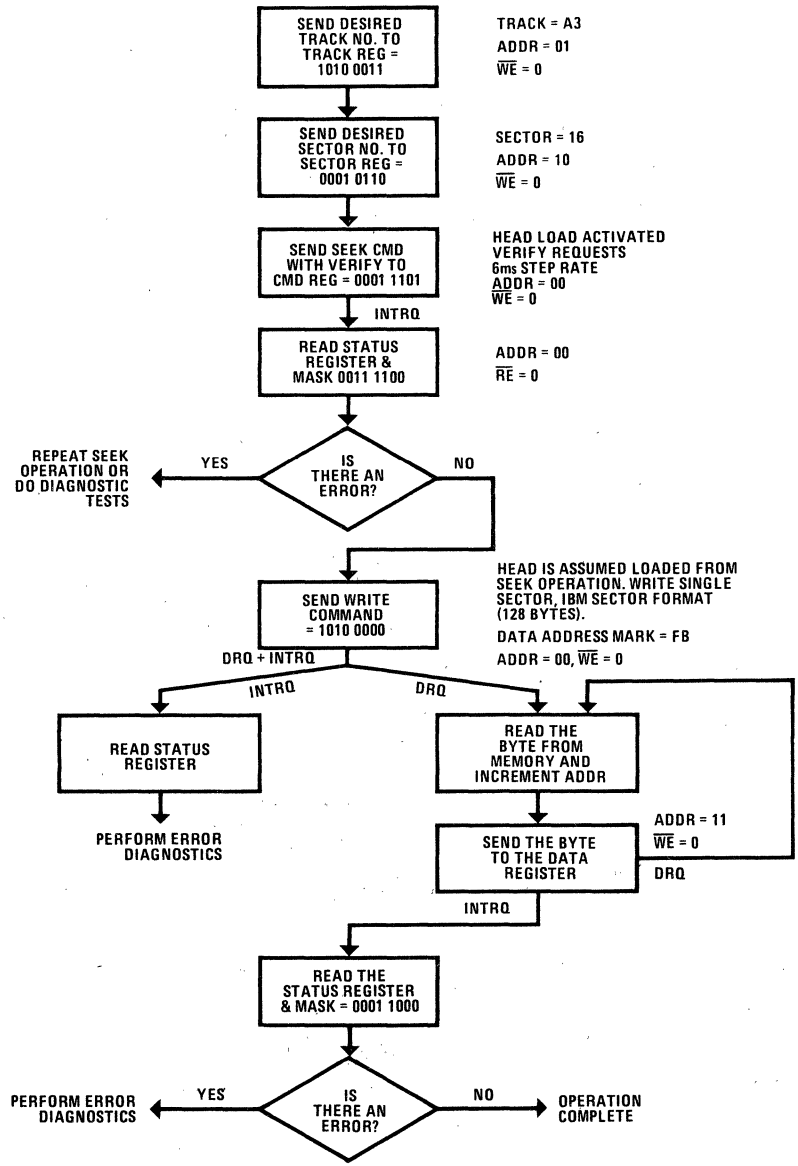


Figure 2. Writing Data

D.3

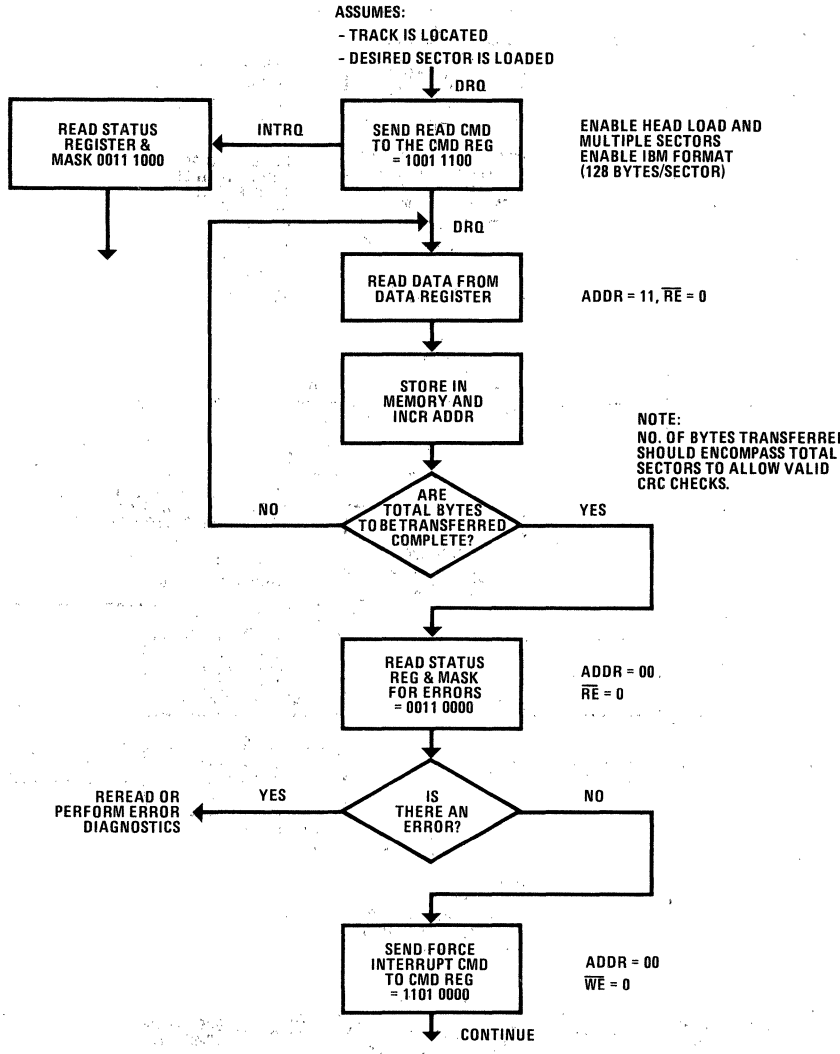


Figure 3. Reading Successive Sectors of Data

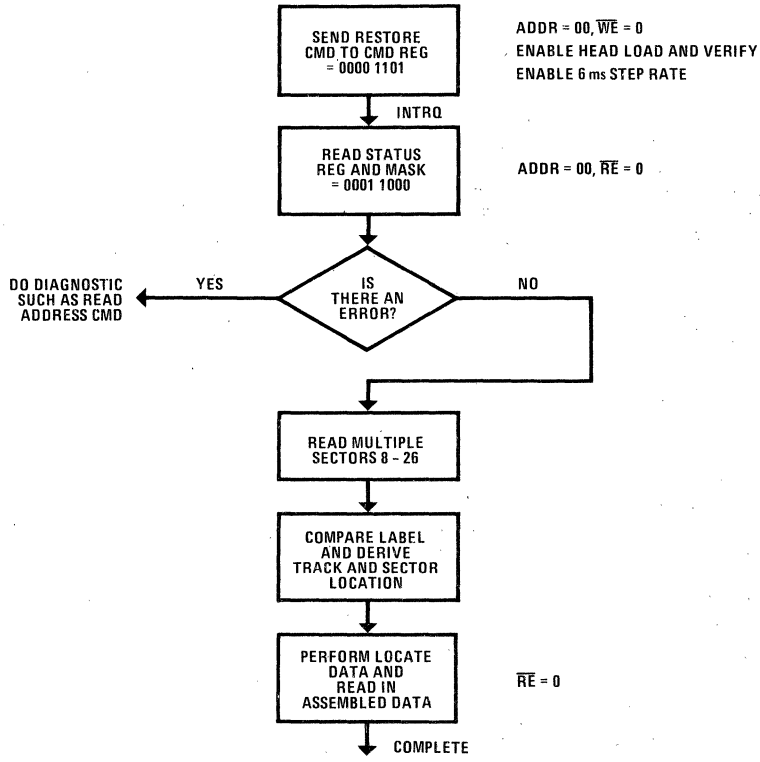


Figure 4. Using Track 00 as Table of Contents

characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations, the Data Request output is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the floppy disk drive, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

The Lost Data bit and certain other bits in the Status Register will activate the Interrupt Request (INTRQ) output. The interrupt line is also activated with normal completion or abnormal termination of all controller operations. The INTRQ signal remains active until reset by reading the Status Register to the processor or by the loading of the Command Register. In addition, the INTRQ output is generated if a Force Interrupt command condition is met.

INS1771-1 FLOPPY DISK DRIVE INTERFACE

The INS1771-1 floppy disk drive interface consists of head positioning controls, write gate controls, and data transfers. A 2.0 MHz ± 1% square wave clock is required at the CLK input for internal control timing. (A 1.0 MHz clock is required for a miniature floppy disk.)

Head Positioning

Four commands cause positioning of the Read/Write head (see INS1771-1 Commands section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step, an additional 10 milliseconds of head settling time takes place. The four programmable stepping rates (r_1r_0) are tabulated under the Type I Commands description.

The r_1r_0 rates can be applied to a three-phase motor or a step-direction motor through the device interface. When the $\overline{3PM}$ input is connected to ground the device operates with a three-phase motor control interface, with one active signal per phase on the three output signals ($\overline{PH1}$, $\overline{PH2}$ and PH3). The stepping sequence is 1-2-3-1 when stepping in and 1-3-2-1 when stepping out. Phase 1 is active low after Master Reset.

The Step-Direction Motor Control interface is activated by leaving input $\overline{3PM}$ open or connecting it to +5 Volts. The phase 1 pin ($\overline{PH1}$) becomes a step pulse of 4 microseconds width. The phase 2 pin ($\overline{PH2}$) becomes a direction control, with a high voltage on this pin indicating a Step In, and a low voltage indicating a Step Out. The Direction output is valid a minimum of 24 microseconds prior to the activation of the step pulse.

When a Seek, Step or Restore command is executed, an optional verification of Read/Write head position can be performed by setting bit 2 in the command word to a logic 1. The verification operation begins at the end of the 10 millisecond settling time after the head is loaded against the medium. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete. If track comparison is not made but the CRC checks, an interrupt is generated, the Seek Error status bit (bit 4) is set, and the Busy status bit is preset. If there is no track comparison nor a valid CRC, a step is made in the same direction as specified and the verify operation is repeated. The additional stepping can be repeated twice to account for two defective tracks. If no verification is received at this point, the Seek Error (bit 4) is set in the Status Register.

The Head Load (HDL) output controls the movement of the Read/Write head against the diskette for data recording or retrieval. It is activated at the beginning of a Read, Write (E flag on) or Verify operation, or a Seek or Step operation with the head load bit (h) a logic high; it remains activated until the third index pulse following the last operation which uses the Read/Write head. Reading or Writing does not occur until a minimum of 10 milliseconds after the HDL signal is made active. If executing the Type II Commands with the E flag off, there is no 10 millisecond delay and the head is assumed to be engaged. The delay is determined by sampling of the Head Load Timing (HLT) input every 10 milliseconds. A low logic state input, generated from the Head Load output transition and delayed externally, identifies engagement of the head against the diskette. In the Seek and Step commands, the head is loaded at the start of the command execution when the h bit is a logic 1. In a verify command, the head is loaded before stepping to the destination track on the diskette whenever the h bit is a logic 0.

Disk Read Operation

The 2.0 MHz external clock provided to the device is internally divided by 4 to form the 500 kHz clock rate for data transfer. When reading data from a diskette, this divider is synchronized to transitions of the Read Data (FDDATA) input. When a transition does not occur on the 500 kHz clock active state, the clock divider circuit injects a clock to maintain a continuous 500 kHz data clock. The 500 kHz data clock is further divided by 2 internally to separate the clock and information bits. The divider is phased to the information by the detection of the address mark.

In the internal data read and separation mode, the Read Data input toggles from one state to the opposite state for each logic 1 bit of clock or information. This signal can be derived from the amplified, differentiated, and sliced Read Head signal, or by the output of a flip-flop toggling on the Read Data pulses. This input is sampled by the 2 MHz clock to detect transitions.

The chip can also operate on externally separated data, as supplied by methods such as phase-lock loop, one-shots, or variable frequency oscillators. This is accomplished by grounding the External Data Separator ($\overline{XTDS}$) input. When the Read Data input makes a high-to-low transition, the information input to the FDDATA line is clocked into the Data Shift Register. The assembled 8-bit data from the Data Shift Register are then transferred to the Data Register.

The normal sector length for Read or Write operations with the IBM 3740 format is 128 bytes. This format or binary multiplex of 128 bytes will be adopted by setting a logic 1 in bit 3 of the Read Track and Write Track commands. Additionally, a variable sector length feature is provided which allows an indicator recorded in the ID Field to control the length of the sector. Variable sector lengths can be read or written in Read or Write commands respectively by setting a logic 0 in bit 0 of the command word. The sector length indicator specifies the number of 16-byte groups, or 16 x N, where N is equal to 1 to 256 groups. An indicator of all zeros is interpreted as 256 sixteen-byte groups.

Disk Write Operation

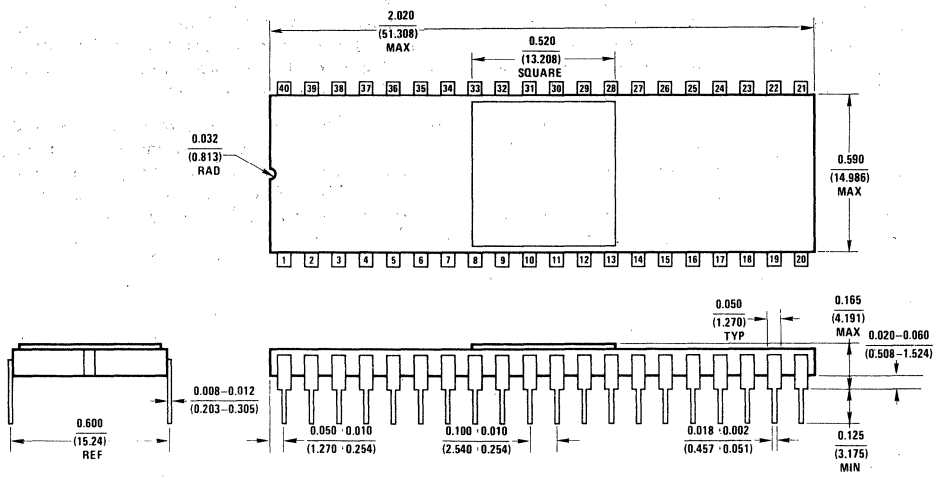
After data is loaded from the processor into the Data Register, and is transferred to the Data Shift Register, data will be shifted serially through the Write Data (WD) output. Interlaced with each bit of data is a positive clock pulse of 0.5 microsecond duration. This signal may be used to externally toggle a flip-flop to control the direction of write current flow.

When writing is to take place on the diskette, the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing, the first data byte must be loaded into the Data Register in response to a Data Request from the INS1771-1 before the Write Gate signal can be activated.

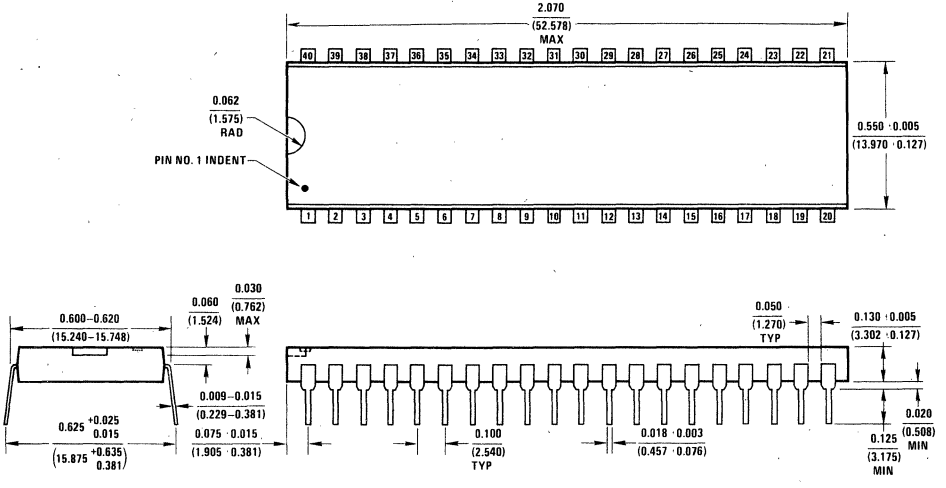
Writing is inhibited when the Write Protect ($\overline{WPRT}$) input is a logic 0, in which case any Write command is immediately terminated, an interrupt is generated, and the Write Protect status bit is set. The Write Fault ($\overline{WF}$) input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate (WG) is activated. On detection of this fault, the INS1771-1 terminates the current command and sets the Write Fault bit (bit 5) of the Status Register. The Write Fault ($\overline{WF}$) input should be made inactive when the Write Gate (WG) output becomes inactive.

Whenever a Read or Write command is received, the INS1771-1 samples the Ready input. If this input is logic 0, the command is not executed and an interrupt is generated. The Seek or Step commands are performed regardless of the state of the Ready input.

Physical Dimensions



Ceramic Dual-In-Line Package (D)
Order Number INS1771D-1
NS Package Number J40A



Plastic Dual-In-Line Package (N)
Order Number INS1771N-1
NS Package Number N40A

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National Semiconductor

Preliminary

JULY 1978

INS8253 Programmable Interval Timer

General Description

The INS8253 is a programmable timer/counter device contained in a standard, 24-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, provides counting or time-out services in a microcomputer system. The various operating modes and other functional characteristics of the INS8253 are programmed by the system software.

The INS8253 provides three independent 16-bit down counters, each of which is capable of count rates in the range DC to 2MHz. Through software initialization, each counter can be made to operate in any one of six modes. The modulus and counting system used are also specified by system software. The operating characteristics of any individual counter can be modified by the software at any time to meet changing system requirements.

The modulus of any given counter can be changed at the program's discretion by loading a new value into the counter. A counter load operation may be limited to the counter's least significant byte or to its most significant byte, or it may revise both halves of the counter.

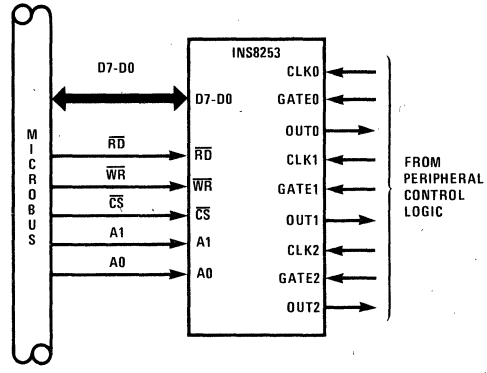
Count sequences may be in either binary or BCD. This choice is also individually specified for each counter by the software.

The contents of each counter may be read either directly or through an auxiliary register. A direct reading of the counter can be made whenever the counter is inhibited from counting. A count value can also be read without interfering with the counting process. This is done by transferring the counter's current value to an auxiliary register and then reading that register. This counter-to-register transfer can be executed without affecting the normal count sequence.

Features

- 3 Individually Programmable 16-Bit Counters
- 6 Operating Modes
- DC to 2MHz Count Rates
- Individual Count Rate and Modulus for Each Counter
- Selectable Counting System (Binary or BCD) for Each Counter
- TRI-STATE® TTL Drive Capability for Bidirectional Data Bus
- Single +5 Volt Power Supply
- 24-Pin Dual-in-Line Package
- MICROBUS™* Compatible

INS8253 MICROBUS Configuration



*A trademark of National Semiconductor Corporation.

Absolute Maximum Ratings

Ambient Temperature Under Bias ..... 0°C to +70°C
Maximum Voltage to Any Input
with Respect to GND ..... −0.5V to +7V
Storage Temperature ..... −65°C to +150°C
Power Dissipation ..... 1 Watt

Note: Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics

(T_A = 0°C to +70°C; V_{CC} = 5V ± 5%)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.2	V_{CC} + 0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	Note 1
V_{OH}	Output High Voltage	2.4		V	Note 2
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0V
I_{CC}	V_{CC} Supply Current		140	mA	

Note 1: INS8253, I_{OL} = 1.6mA.
Note 2: INS8253, I_{OH} = −150μA.

Capacitance

T_A = 25°C; V_{CC} = GND = 0V.

Symbol	Parameter	Min	Max	Unit	Test Conditions
C_{IN}	Input Capacitance		10	pF	f_C = 1MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to V_{SS}

AC Electrical Characteristics

T_A = 0°C to +70°C; V_{CC} = 5.0V ± 5%; GND = 0V

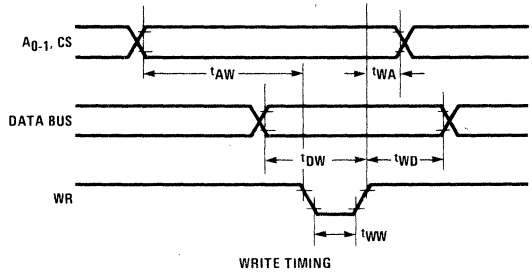
Bus Parameters:

Symbol	Parameter	Min	Max	Unit
READ CYCLE				
t_{AR}	Address Stable Before $\overline{READ}$	50		ns
t_{RA}	Address Hold Time for $\overline{READ}$	5		ns
t_{RR}	$\overline{READ}$ Pulse Width	400		ns
t_{RD}	Data Delay from $\overline{READ}$ (Note 2)		300	ns
t_{DF}	$\overline{READ}$ to Data Floating	25	125	ns
WRITE CYCLE				
t_{AW}	Address Stable Before $\overline{WRITE}$	50		ns
t_{WA}	Address Hold Time for $\overline{WRITE}$	30		ns
t_{WW}	$\overline{WRITE}$ Pulse Width	400		ns
t_{DW}	Data Setup Time for $\overline{WRITE}$	300		ns
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		ns
t_{RV}	Recovery Time Between $\overline{WRITE}$s	1		ns

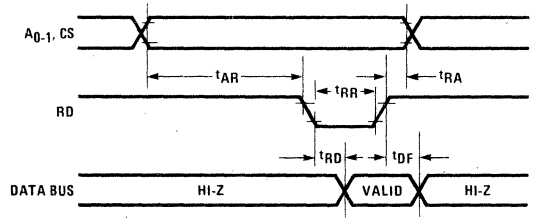
Note 1: AC timings measured at V_{OH} = 2.2V, V_{OL} = 0.8V.

Note 2: Test conditions: INS8253, C_L = 100pF.

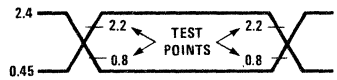
Input Waveforms for AC Tests



WRITE TIMING



READ TIMING

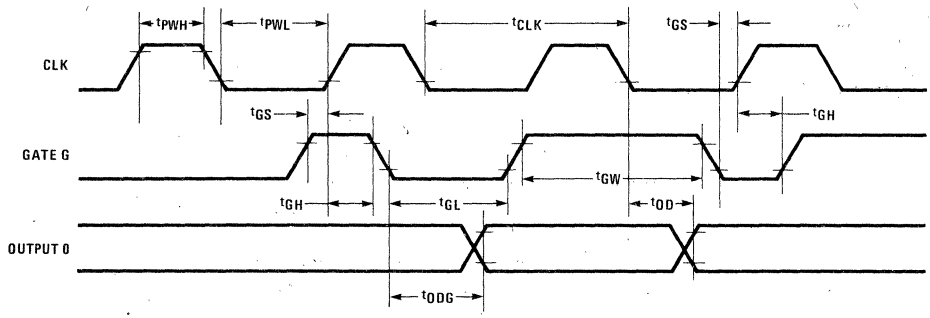


D.3

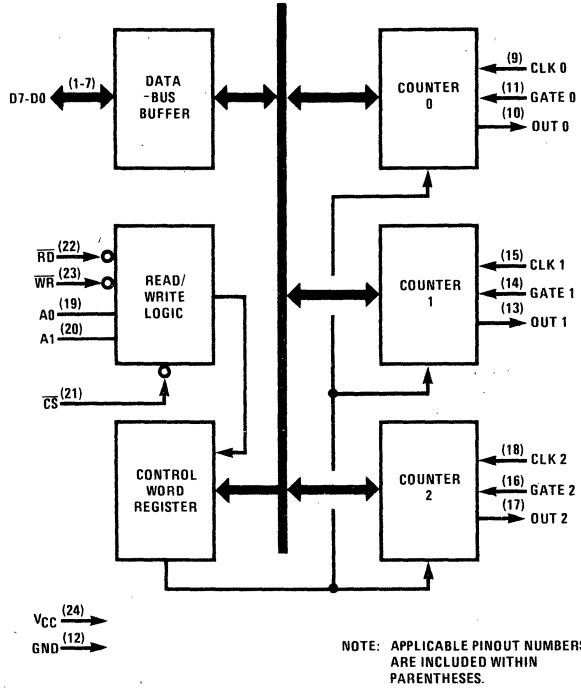
Clock and Gate Timing

Symbol	Parameter	Min	Max	Unit
t_{CLK}	Clock Period	380	DC	ns
t_{PWH}	High Pulse Width	230		ns
t_{PWL}	Low Pulse Width	150		ns
t_{GW}	Gate Width High	150		ns
t_{GL}	Gate Width Low	100		ns
t_{GS}	Gate Setup Time to CLK ↑	100		ns
t_{GH}	Gate Hold Time After CLK ↑	50		ns
t_{OD}	Output Delay From CLK ↓ (Note 1)		400	ns
t_{ODG}	Output Delay From Gate ↓ (Note 1)		300	ns

Note 1: Test conditions: INS8253, C_L = 100pF.



INS8253 Functional Block Diagram



NOTE: APPLICABLE PINOUT NUMBERS ARE INCLUDED WITHIN PARENTHESES.

INS8253 Functional Pin Description

The following describes the functions of all INS8253 input/output pins. Some of these descriptions refer to internal circuits.

NOTE

In the following descriptions, a low represents a logic 0 (0 Volt, nominal) and a high represents a logic 1 (+2.4 Volts, nominal).

INPUT SIGNALS

Chip Select ($\overline{CS}$): When low, the chip is selected. This enables communication between the INS8253 and the microprocessor.

Read ($\overline{RD}$): When low, allows the microprocessor to read contents of counter specified by A0, A1.

Write ($\overline{WR}$): When low, writes control word into control word register or loads new count value into selected counter. Destination of data (control word register or counter 0, 1 or 2) is specified by A0, A1.

A0, A1: These inputs are used to select one of the counters for reading or writing or to select the control word register for writing. A0, A1 may be controlled via address bus lines.

Clock (CLK0-CLK2): Each counter has a separate clock input that drives the counter.

Gate (Gate 0-Gate 2): Each counter is individually controlled by a separate Gate input (1 = enable, 0 = inhibit). In some modes, the positive edge of Gate is used to initiate the counting process. Specific use of Gate depends on the counter's operating mode. Details are provided in the section entitled INS8253 Programming.

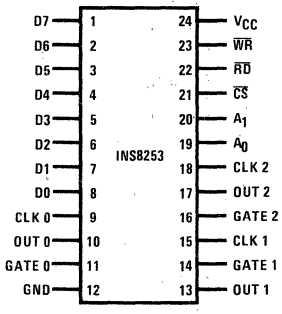
OUTPUT SIGNALS

Output (Out 0-Out 2): Each counter has a single output that indicates whether or not the counter has reached its terminal count. Specific operation of this output depends on the counter's mode. Details are provided in the section entitled INS8253 Programming.

INPUT/OUTPUT SIGNALS

Data (D7-D0) Bus: This bus, which comprises eight TRI-STATE input/output lines, provides for bidirectional communication between the INS8253 and the microprocessor. Control words and count value bytes are transferred over these lines.

INS8253 Pin Configuration



INS8253 Programming

This section provides basic information for programming the INS8253 and describes the methods for reading counter status. Table 1 summarizes the control signals needed to write command words and new count values into the INS8253 and to read the contents of individual counters.

Table 1. Bus Control for INS8253 I/O Operations

Output Operations	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	A1	A0
LOAD COUNTER 0	0	0	1	0	0
LOAD COUNTER 1	0	0	1	0	1
LOAD COUNTER 2	0	0	1	1	0
WRITE CONTROL WORD	0	0	1	1	1
Input Operations					
READ COUNTER 0	0	1	0	0	0
READ COUNTER 1	0	1	0	0	1
READ COUNTER 2	0	1	0	1	0

WRITING CONTROL WORDS

Each counter's mode and counting system (binary or BCD) are specified by an eight-bit control word. See figure 1. An I/O write operation with A0, A1 = 11 will load the control word into the control word register. The control word contains four fields:

- D7, D6 (SC1, SC0) — This field specifies which counter will be affected by the other control fields.
- D5, D4 (RL1, RL0) — A bit pattern of 00 in this field causes the contents of the selected counter to be latched in an auxiliary register. The count value can then be read without inhibiting the counter. The other three bit patterns specify which byte(s) of the selected counter will be affected by any subsequent read/write operations addressed to that counter.
- D3, D2, D1 (M2, M1, M0) — This field specifies the mode of operation for the selected counter.
- D0 (BCD) — This one-bit field specifies the counting system to be used by the selected counter.

Any time after a counter is initialized by a control word, its initial count value can be loaded. This is done by means of a write operation addressed to that counter. Details are given in the section entitled Loading Initial Count Value.

Programming of the three counters can be executed in any sequence, with only two requirements.

1. A counter must be issued a control word before it is given an initial count value.
2. Read and write operations addressed to a counter must conform to the byte-selection rules specified by the RL1, RL0 field in the control word. For example, if the counter's RL1, RL0 bits = 10, subsequent counter load operations addressed to that counter must be intended for the most significant byte only.

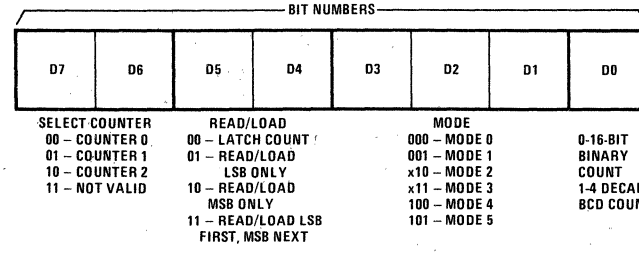


Figure 1. Control Word Format

COUNTER MODE DESCRIPTIONS

Figure 2 provides timing information for the six INS8253 operating modes.

- Mode 0, Timed Interrupt — In this mode, OUT goes low when the mode is set. The counter begins counting CLK cycles when the count is loaded. OUT remains low until the terminal count is reached, at which point it goes high and remains high until either the mode or count is reloaded. The gate input will inhibit the count when low.

  If the counter is loaded with a new value during a count cycle, counting will stop when the first byte is loaded and will begin decrementing from the new value after the second byte is loaded.

- Mode 1, Retriggerable One Shot — In this mode, OUT goes low on the first CLK after a rising transition on Gate. OUT goes high again on the terminal count.

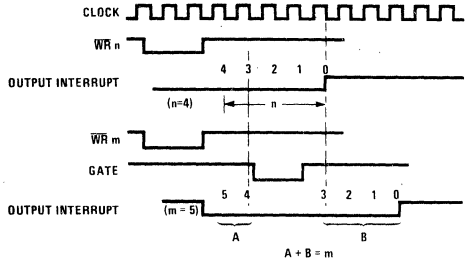
  Gate can be used to retrigger the counter. Each positive transition of Gate causes the counter to begin decrementing from the initial count value.

  If a new initial count value is loaded during a count cycle, the new value will not take effect until the next rising transition of Gate.

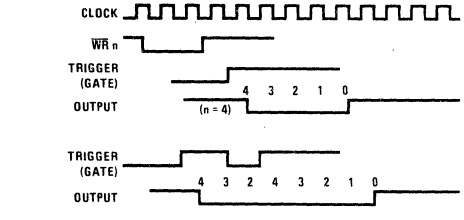
- Mode 2, Rate Generator — In this mode, OUT goes low for one CLK cycle at the end of each count sequence. The leading edge of each pulse occurs at the start of the terminal CLK cycle. The counter will repeat count sequences as long as Gate remains high. Any positive transition of Gate will start a new count sequence at the initial count value. This allows the counter to be synchronized by Gate.

  If a new initial count value is loaded during a count sequence, the current sequence will run to completion and the following sequence will then start at the new initial count value.

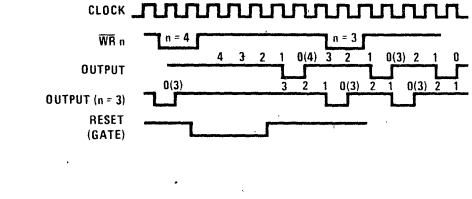
MODE 0



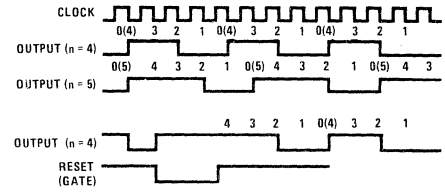
MODE 1



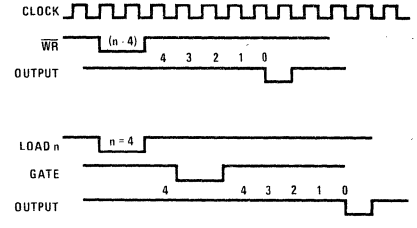
MODE 2



MODE 3



MODE 4



MODE 5

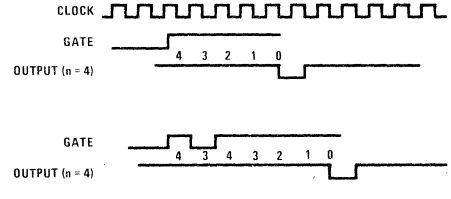


Figure 2. Mode Timing Waveforms

- Mode 3, Square Wave Generator — In this mode, the counter generates a square wave signal at the OUT pin so long as Gate remains high. The period of the square wave is equal to one count cycle. If the initial count value is even, OUT will be high for the first half of each count sequence and low during each second half. For an odd count, OUT is high for (N + 1)/2 counts and low for (N – 1)/2 counts.

  If a new initial count value is loaded during a count sequence, the current sequence will run to completion and the following sequence will then start at the new initial count value.

  Any positive transition of Gate will start a new count sequence at the initial count value. This allows the counter to be synchronized by Gate.

- Mode 4, Software Triggered Strobe — In this mode, OUT is normally high and goes low for one CLK cycle after the terminal count is reached. Counting is enabled when Gate is high. Counting is initiated by loading the modulus.

  If a new initial count value is loaded during a count sequence, the current sequence will run to completion and the following sequence will then start at the new initial count value.

  A low on the Gate input inhibits the count.

- Mode 5, Hardware Triggered Strobe — In this mode, any positive transition of Gate will initiate a new count sequence. OUT then goes low for one CLK cycle when the terminal count is reached.

LOADING INITIAL COUNT VALUE

Each counter's modulus is determined by presetting the counter to the desired value. This is done by means of one or two I/O write operations with A1, A0 selecting the counter to be preset. The write operation loads the contents of the data bus (D7-D0) into the upper or lower half of the selected counter, as determined by the control word's RL1, RL0 field. Figure 3 summarizes the various counter loading conditions.

After a counter's initial count value is loaded, it is ready for operation in the specified mode. It begins counting CLK cycles when its Gate input goes high. Each CLK decrements the enabled counter by one until the full count cycle has been completed.

The initial count value of any counter can be changed by loading a new value into the counter's:

- LSB only (RL1, RL0 = 01),
- MSB only (RL1, RL0 = 10), or
- LSB first, and then MSB (RL1, RL0 = 11).

Read/Load Conditions RL1	RL0	Effect of Subsequent Write Operation
0	1	$\overline{WR}$ loads D7-D0 into LSB of counter selected by A1, A0.*
1	0	$\overline{WR}$ loads D7-D0 into MSB of counter selected by A1, A0.
1	1	First $\overline{WR}$ loads D7-D0 into LSB of counter selected by A1, A0. Next $\overline{WR}$ loads D7-D0 into counter's MSB.

*A1	A0	
0	0	Selects Counter 0
0	1	Selects Counter 1
1	0	Selects Counter 2

Figure 3. Initial Count Loading Summary

READING COUNT VALUES

The current status of a count sequence can be examined at any time by the program. This can be done either by reading the counter contents directly or by latching the counter contents into an auxiliary register and then reading that register.

A counter can be read directly with the following bus conditions:

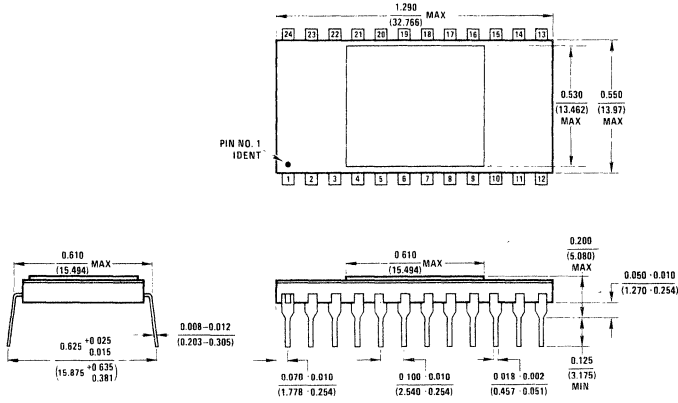
	$\overline{RD}$	A1	A0
To Read Counter 0	0	0	0
To Read Counter 1	0	0	1
To Read Counter 2	0	1	0

The count should remain stable during direct reading of a counter. Stability is assured by holding the Gate input low or inhibiting the CLK input (by means of external logic) for the duration of the read operation. Counter status can also be sampled without inhibiting the count sequence. This is done by issuing a control word to the counter with RL1, RL0 = 00, followed by an I/O read of that counter's location. The RL1, RL0 bits cause the contents of the addressed counter to be latched into the auxiliary register. The subsequent read operations access the auxiliary register.

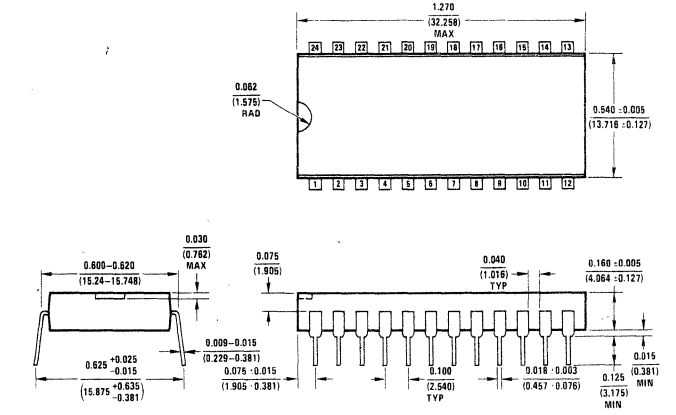
When reading either a counter or the auxiliary register, the read operation must follow the format programmed for that counter by RL0 and RL1. Note that issuing a latch command of RL1, RL0 = 00 does not alter the previously programmed RL0 and RL1.

Physical Dimensions

inches (millimeters)



24-Lead Hermetic DIP (D)
NS Package Number D24A



24-Lead Molded DIP (N)
NS Package Number N24A

D.3

National Semiconductor

JULY 1978

INS8254 N-Channel Bit Programmable Peripheral Interface

General Description

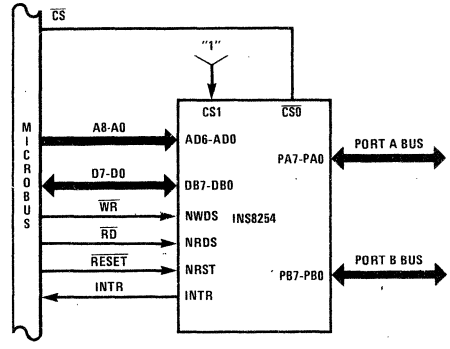
The INS8254 is an LSI device which provides two 8-bit ports of peripheral interfacing capability for microcomputer systems. The I/O chip contains two peripheral ports of eight bits each. Each of the I/O pins in the two ports may be defined as an input or an output to provide maximum flexibility. Each port may be read from or written to in a parallel (8-bit byte) mode. To improve efficiency and simplify programming in control-based applications, a single bit of I/O in either port may be set, cleared or read with a single microprocessor instruction. In addition to basic I/O, one of the ports, port A, may be programmed to operate in several types of strobed mode with handshake. Strobed mode together with optional interrupt operation permit both high speed parallel data transfers and interface to a wide variety of peripherals with no external logic.

The INS8254 is an n-channel silicon gate device packaged in a 40-pin dual-in-line package. It operates with a single 5-volt power supply and is fully TTL compatible.

Features

- Single +5-volt power supply
- Low power dissipation
- Fully static operation
- Completely TTL compatible
- Two 8-bit programmable I/O ports
- I/O port A has TRI-STATE® capability
- Handshake controls for strobed mode of operation
- Single bit I/O operations with single instruction
- Reduces system package count
- Direct interface with SC/MP-II
- MICROBUS ™* compatible

INS8254 MICROBUS Configuration



*Trademark, National Semiconductor Corp.

Absolute Maximum Ratings*

Voltage at Any Pin	−0.5 V to +7.0 V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

*Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under Electrical Characteristics.

DC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5 V ± 5% unless otherwise specified.)

Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage		2.0		V_{CC}+0.5	V
V_{IL}	Logical "0" Input Voltage		−0.5		0.8	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −100 μA	2.4			V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 2.0 mA			0.4	V
I_{LI}	Input Load Current	V_{IN} = 0 V to 5.25 V			±10	μA
I_{LO}	Output Leakage Current	High Impedance State			±10	μA
I_{CCI}	Power Supply Current	All Outputs Open, T_A = 25°C, NRST ≤ 0.8 V		45	60	mA

AC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5 V ± 5% unless otherwise specified — see Note 1.)

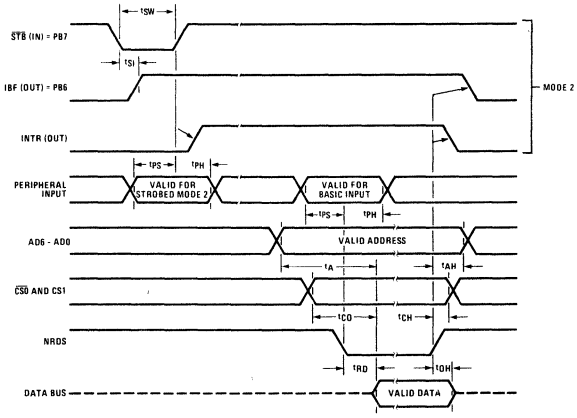
Parameter		Conditions	Min	Typ	Max	Units
READ CYCLE						
t_{SW}	$\overline{STB}$ Pulse Width (Mode 2 only)		300			ns
t_{SI}	$\overline{STB}$ ↓ to IBF ↑ Delay (Mode 2 only)				250	ns
t_{PS}	Peripheral Setup		50			ns
t_{PH}	Peripheral Hold		120			ns
t_{AH}	Address Hold		50			ns
t_{CH}	CS Hold		50			ns
t_{RD}	NRDS ↓ to Data Valid				350	ns
t_A	Access				560	ns
t_{CO}	Chip Select to Output				520	ns
t_{OH}	Data Valid After NRDS ↑		0	125		ns
	Output Load Capacitance				75	pF
WRITE CYCLE						
t_{AS}	Address Setup		50			ns
t_{AH}	Address Hold		0			ns
t_{CS}	CS Setup		50			ns
t_{CH}	CS Hold		0			ns
t_{DS}	Data Setup		50			ns
t_{DH}	Data Hold		50			ns

AC Electrical Characteristics (cont'd.)

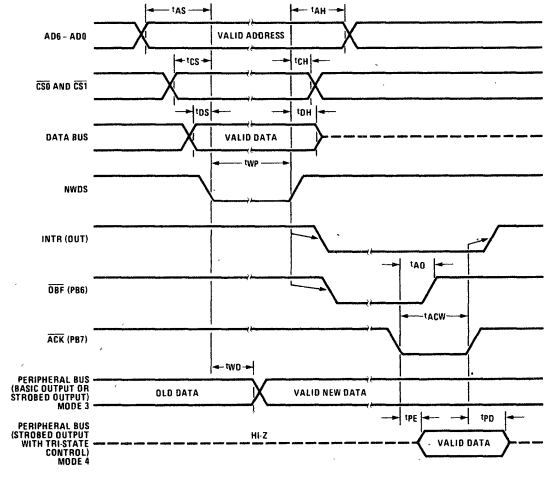
Parameter		Conditions	Min	Typ	Max	Units
t_{WP}	NWDS Pulse Width		300			ns
t_{AO}	$\overline{ACK}$ ↓ to OBF ↑ (Modes 3 & 4 only)				250	ns
t_{ACW}	$\overline{ACK}$ Pulse Width (Modes 3 & 4 only)		300			ns
t_{WD}	Port Data Valid After NWDS ↓				300	ns
t_{PE}	$\overline{ACK}$ ↓ to Valid Output (Mode 4 only)				300	ns
t_{PD}	$\overline{ACK}$ ↑ to Hi-Z (Mode 4 only)		0	125		ns
	Output Load Capacitance				75	pF
$t_{W\overline{RST}}$	Master Reset Pulse		300			ns

Note 1: All times measured from a valid logic "0" level = 0.8 V or a valid logic "1" level = 2.0 V.

Timing Diagrams



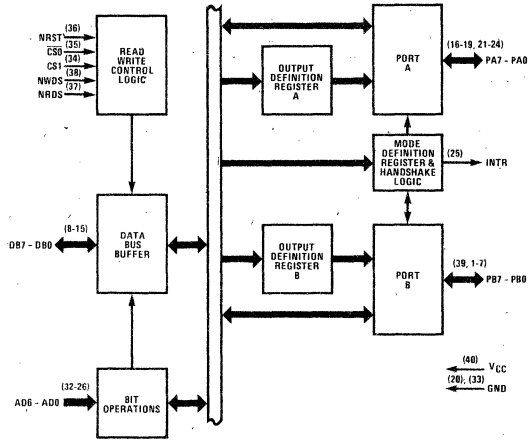
Read Cycle



Write Cycle

D.3

INS8254 Block Diagram



Basic Functional Description

The 16-bit input/output provides interface capability between a microcomputer and its peripherals by means of the two 8-bit I/O ports. The ability to program the configuration and operating modes of the I/O ports allows interfacing a microcomputer to a wide variety of peripherals with minimum external logic. Major functional blocks of the chip are shown in figure 1; an operational summary of the chip is provided in figure 2. A description of the chip pinouts and a summary of the internal chip registers is given below.

(DB7 - DB0) Data Bus Buffers

The data bus buffer is a TRI-STATE, bidirectional, 8-bit buffer that is used to interface the INS8254 to a microcomputer data bus. Data, control, and status information is transmitted to and received from the INS8254 via the data bus buffers. Execution of a STORE instruction by the microprocessor may be used to transmit data and control information from the CPU to the INS8254. Execution of a LOAD instruction may be used to transmit data and status information from the INS8254 to the CPU.

(PA7 - PA0, PB7 - PB0) Peripheral Ports A and B

The INS8254 contains two eight-bit I/O ports: port A and port B. Each port consists of an eight-bit output data latch with buffer and an eight-bit input data latch. Full flexibility is provided with the ability to define any bit of the two ports either as an input or as an output. Bit set, clear and read of all I/O pins are also provided. Moreover, port A may be operated in strobed input or strobed output modes.

($\overline{CS0}$ and CS1) Chip Select Inputs

The combination of a low on $\overline{CS0}$ and a high on CS1 input pins enables communication between the INS8254 and the microprocessor.

(NRDS) Read Strobe

NRDS is an active-low read strobe. A low on this pin enables data or status information to be read from the INS8254.

(NWDS) Write Strobe

NWDS is an active-low write strobe. A low on this pin enables data or control information to be written into the INS8254.

(AD6 - AD0) Address Inputs

The address input bus determines where in the INS8254 communication will take place. The address determines which I/O or control register will be enabled for communication with the CPU. These pins are normally connected to the seven low address lines of the microprocessor.

(MDR) Mode Definition Register

The Mode Definition Register is an internal control register that determines the operating mode of port A. This register is *write only*. If a read operation is performed with the address set to that of the MDR, the data bus will remain in the high impedance state.

(NRST) Master Reset

NRST is the master reset input for the INS8254 chip. A low on this pin clears all registers in the I/O portion of the chip (MDR, ODRA, ODRB, and the port output data latches) and places the data bus in the high impedance state independent of any other control strobes. After a master reset, the I/O ports will both be in the basic I/O mode and configured as inputs.

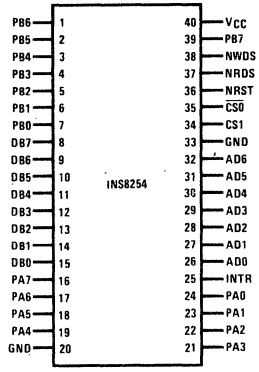
(INTR) Interrupt Request

The interrupt request (INTR) output is an active high signal used to interrupt the microprocessor when a strobed mode data transaction has occured. This signal is active only when port A is in the strobed mode. INTR will be set to a low when a master reset is applied (NRST set low).

Output Definition Registers — ODRA and ODRB

Associated with each port is an output definition register (ODR). Each ODR is an eight-bit latch that defines which of the I/O pins in the respective port are to be used as outputs. ODRA controls the direction of port A and ODRB controls the direction of port B. Both ODRs are *write only* registers. If a read operation is performed with the address set to that of an ODR, the data bus will remain in the high impedance state.

Pin Configuration



Pin Names

DB7 - DB0	DATA BUS
AD6 - AD0	ADDRESS INPUT
NRST	RESET INPUT
$\overline{CS0}$, CS1	CHIP SELECTS
NWDS	WRITE STROBE
NRDS	READ STROBE
PA7 - PA0	PORT A
PB7 - PB0	PORT B
INTR	INTERRUPT REQUEST
V_{CC}	+5 VOLTS
GND	0 VOLTS

Figure 1. Pin Identification

Operation	NRST	NRDS	NWDS	$\overline{CS0}$	CS1	A6	A5	A4	A3	A2	A1	A0
BIT OPERATIONS												
Set Bit Port A	1	1	0	0	1	0	0	1	0	B2	B1	B0
Clear Bit Port A	1	1	0	0	1	0	0	0	0	B2	B1	B0
Read Bit Port A	1	0	1	0	1	0	0	X	0	B2	B1	B0
Set Bit Port B	1	1	0	0	1	0	0	1	1	B2	B1	B0
Clear Bit Port B	1	1	0	0	1	0	0	0	1	B2	B1	B0
Read Bit Port B	1	0	1	0	1	0	0	X	1	B2	B1	B0
PORT OPERATIONS												
Port A → Data Bus	1	0	1	0	1	0	1	0	0	0	0	0
Data Bus → Port A	1	1	0	0	1	0	1	0	0	0	0	0
Port B → Data Bus	1	0	1	0	1	0	1	0	0	0	0	1
Data Bus → Port B	1	1	0	0	1	0	1	0	0	0	0	1
CONTROL OPERATIONS												
Data Bus → Output Definition A	1	1	0	0	1	0	1	0	0	0	1	0
Data Bus → Output Definition B	1	1	0	0	1	0	1	0	0	0	1	1
Data Bus → Mode Definition Register	1	1	0	0	1	0	1	0	0	1	0	0
DISABLE FUNCTION												
Master Reset	0	X	X	X	X	X	X	X	X	X	X	X
Data Bus → Hi-Z	1	1	1	0	1	X	X	X	X	X	X	X
Data Bus → Hi-Z	1	X	X	1	X	X	X	X	X	X	X	X
Data Bus → Hi-Z	1	X	X	X	0	X	X	X	X	X	X	X

Figure 2. Truth Table

D.3

Detailed Operation

Mode Definition Register

The mode definition register defines the operating mode for port A. Port B is always in the basic I/O mode. There are four operating modes for port A:

Mode 1 – basic I/O

Mode2 – strobed input

Mode 3 – strobed output

Mode 4 – strobed output with TRI-STATE control

In mode 1, basic I/O, there is no handshaking and data is simply written to or read from the specified port. Port B is always in this mode. When NRST goes low, both port A and port B are set to the basic I/O mode with all bits set to input. Mode 2, strobed input, provides a means for transferring data from the peripheral into port A in response to handshake or strobe signals. Mode 3, strobed output, provides a means for transferring data from port A to the peripheral in response to strobes or handshake signals. Mode 4, strobed output with TRI-STATE control is similar to mode 3 except that port A is in the high impedance state until the handshake signal goes active. Figure 3 summarizes what data should be written into the MDR to place port A in the desired mode. When port A is operated in any one of the three strobed modes, two pins of port B are used for handshake control functions; accordingly, only six of the eight port B pins are available for data input/output bits.

Output Definition Registers

Although addressed separately from the ports, the output definition registers are an integral part of the I/O ports as shown in figure 4. This figure shows the input data latch and output data latch/buffer of a bit in a port and the bit of the ODR associated with it. Thus there is one bit of an ODR associated with each peripheral I/O pin in port A and port B. If a low or "0" is written into the ODR, the output data buffer associated with it will be disabled, and the I/O bit is in the input mode. If a high or "1" is written into the ODR, the I/O bit is in the output mode. When strobed mode operation (modes 2 through 4) is defined for port A via the MDR, it is also necessary to set up proper input/output definition in ODRA for port A.

Basic I/O – Mode 1

In the basic I/O mode of operation data is simply written to or read from a port without handshake signals; the interrupt request (INTR) is always low when port A is operated in this mode. Port B is always in the basic I/O mode, whereas the MDR bit 5 (M in figure 3) must be set to zero to define port A in the basic I/O mode. Since the MDR, ODRA and ODRB are all cleared by a master reset, both port A and port B will be in the basic input mode after a master reset (NRST set low).

Figure 5 shows a timing diagram for basic output. When the microprocessor performs a write operation to a port, the data on the data bus is latched in the output latch on the leading edge of the write strobe. The data will remain valid until another write to the port with new data occurs. If the new data written is the same as the old data, then no change will occur so long as the proper data and strobe timing is maintained.

Figure 6 shows a timing diagram for basic input. When the microprocessor reads the port, the peripheral data is *latched* in the input latch on the leading edge of the read strobe. The data bus buffers are enabled so the contents of the latch are gated on to the system data bus. The data remains latched until the end of the read cycle (i.e., until the trailing edge of the read strobe). Latching the input data in this manner allows the chip to synchronize asynchronous peripheral signals with slow rise and fall times to the microprocessor.

A port can have some input pins and some output pins, since there is an ODR latch for each bit in the port. A write to a pin defined as an input will load a new value into the output data latch, but since the output data buffer is disabled, it will have no effect on the I/O pin. A data read from I/O pins defined as outputs will read the data from the output data latch. The data will be read properly only if the I/O lines are permitted to be greater than V_{IH} for a logic 1 output and less than V_{IL} for a logic 0 output. If the I/O pins are loaded in such a way that valid levels are not reached, the data read will not always agree with the data stored in the output data latch.

Bit Set, Clear, and Read

In addition to reading and writing each port as an eight-bit parallel byte, it is also possible to set, clear or read any individual bit in either port. Bit set or clear is performed by doing a write operation with the chip selected and the proper address. Since the address determines which bit is operated on and whether it is set or cleared, the eight data bus lines are all don't-care for a bit set or clear. This permits the microprocessor to do a bit set or clear with a single instruction without initially setting up the accumulator. The three low order bits of the address determine which bit of the port is set or cleared (e.g., AD2 = 0, AD1 = 1 and AD0 = 0 would indicate bit 2). Address bit 3 (AD3) determines if port A or port B is acted upon. Address bit 4 (AD4) determines if the operation is a bit set or clear.

When a bit read is performed, the selected bit is placed on data bus bit 7 (DB7) and all other bits of the data bus are set to zero. The bit is selected by reading from the chip with the same addresses described for bit set and clear. All bit operations are summarized in figure 7.

Besides simplifying programming in control applications, bit operations are used to control interrupt enable when port A is in the strobed mode. The timing for bit operations is the same as that for basic input/output except that, for bit set and bit clear operations, the data bus is a "don't care." A bit set to a pin whose previous value was a "1" or a bit clear to a pin whose previous value was a "0" will not cause that pin to leave its previous value, even momentarily.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Bit Location
TS	OUT	M	–	–	–	–	–	MDR Bit Name
X	X	0	X	X	X	X	X	Basic I/O
X	0	1	X	X	X	X	X	Strobed Input
0	1	1	X	X	X	X	X	Strobed Output
1	1	1	X	X	X	X	X	Strobed Output with TRI-STATE Control

Figure 3. Mode Definition of Port A with MDR

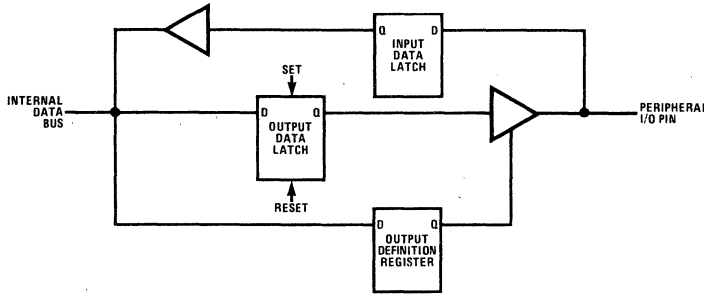


Figure 4. Internal Logic of One Bit of an I/O Port with ODR

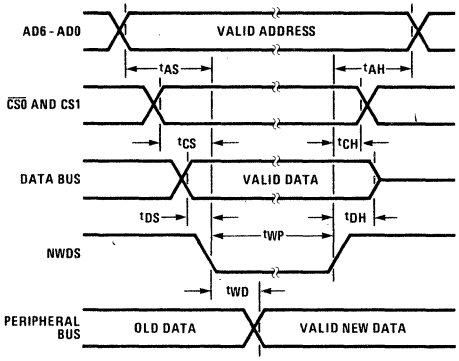


Figure 5. Basic Output Timing

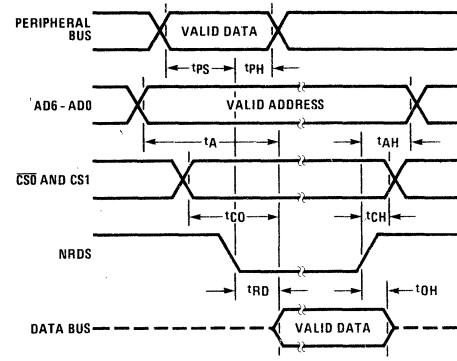


Figure 6. Basic Input Timing

	NRDS	NWDS	A4	A3	A2	A1	A0
BIT SET & CLEAR							
Bit Set, Port A	1	0	1	0	B2	B1	B0
Bit Clear, Port A	1	0	0	0	B2	B1	B0
Bit Set, Port B	1	0	1	1	B2	B1	B0
Bit Clear, Port B	1	0	0	1	B2	B1	B0
BIT READ Selected Bit → DB7 0 → DB6 - DB0							
Bit Read, Port A	0	1	X	0	B2	B1	B0
Bit Read, Port B	0	1	X	1	B2	B1	B0

Bit Operations Enabled When $\overline{CS0}$ = 0, CS1 = 1, A6 = 0, & A5 = 0.

B2, B1, & B0 select which bit is selected (B0 is least significant bit).

Figure 7. Bit Operations

D.3

Strobed Input (Port A) – Mode 2

This mode allows data to be read from a peripheral in a two-step transaction. First, the peripheral strobes data into the INS8254 input latch and notifies the microprocessor that data is ready to be read. Second, the processor reads the contents of the INS8254 input latch and resets the handshake control signals for the next transaction to take place. Transferring data in two steps frees the microprocessor to undertake other tasks in between data transfers from the port A peripheral. Figure 8 shows the signal timing and figure 9 shows a logic diagram for the handshake signals. The handshake control signals are as follows:

$\overline{\text{STB}}$ ($\overline{\text{Strobe}}$)

The $\overline{\text{STB}}$ signal is an active-low strobe generated by a peripheral to signify that data is valid at the peripheral bus on the trailing edge of this strobe. This signal is fed into pin PB7 of the INS8254. $\overline{\text{STB}}$ latches peripheral bus data into the INS8254 input data latch on its trailing edge. This does *not* require the INS8254 to be selected. Should STB pulse low more than once before the arrival of NRDS, the data stored in the INS8254 input data latch will be the *last* stored data.

IBF (Input Buffer Full)

The IBF signal is an output from the INS8254 driven by pin PB6; IBF is set by the leading edge of $\overline{\text{STB}}$ and is reset by the trailing edge of NRDS when the microprocessor is performing a byte-read from port A. IBF high tells the peripheral that data is latched in the port A input data latch. IBF goes low on the trailing edge of the microprocessor NRDS strobe to notify the peripheral that data has been read in the microprocessor and that the next transaction can now take place. The microprocessor can override IBF by doing a bit set or bit clear to PB6.

IE (Interrupt Enable)

IE is the output data latch of PB7, whose output is ANDed with the interrupt request latch to produce the INTR signal. IE is zero after a master reset (NRST) but may be written into from the microprocessor by doing a bit set/clear to PB7.

INTR (Interrupt Request)

When enabled by IE, INTR is an output that is set on the trailing edge of $\overline{\text{STB}}$, requesting the microprocessor to read the data in the port A input data latch. When the microprocessor responds to read port A, the trailing edge of NRDS resets INTR. Should IE *not* be set, INTR will remain low.

In a multiple-interrupt application, the microprocessor can poll the INS8254 for the existence of an interrupt request by doing a bit read of PB7. Being able to read the INTR status on the microprocessor system bus is useful in multi-interrupt schemes to find the originator of an interrupt.

Parallel write operations to port B while port A is in any one of its strobed modes will leave bits PB6 and PB7 unaffected. Thus, port B now has 6 data I/O bits associated with it and the handshake bits PB6 and PB7 respond only to valid changes in handshake status or to bit set/bit clear operations.

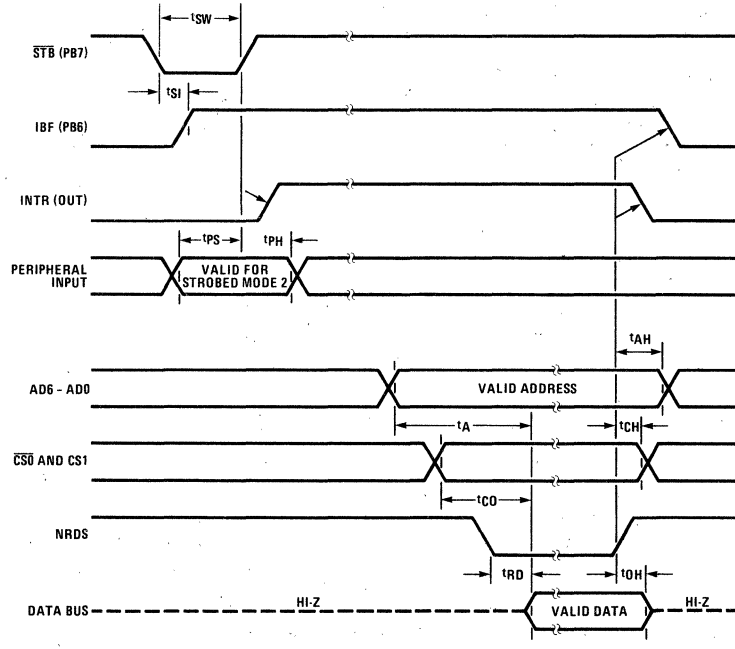
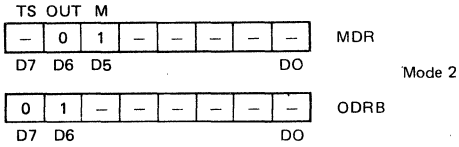


Figure 8. Strobed Input, Mode 2 Timing

Initializing Strobed Input — Mode 2

Prior to operation, an initialization procedure must be undertaken. The MDR must have a "1" written into bit 5 and a "0" written into bit 6. The ODRA must have "0s" written into it to identify the pins in port A which will function in mode 2. The ODRB must have a "0" written into PB7 in order to make it an input which will receive $\overline{STB}$ from the peripheral. Also, PB6 must be defined as an output so that it can drive the IBF signal. The remaining six lower bits of ODRB are configured as needed for the basic input/output transactions occuring in port B.



ODRA = "0s" at mode 2 pins.

Writing to the MDR to define mode 2 operation will automatically initialize both IBF and INTR in such a manner that they will be expecting the peripheral to begin the first I/O transaction with a $\overline{STB}$ strobe, i.e., both INTR and IBF will initialize low when the above write to the MDR takes place.

Handshake Status

Handshake status control signals IBF and INTR will be reset by a microprocessor LOAD instruction only if it is addressed to port A as a byte read. A parallel write or bit write or bit read to port A will *not* affect handshake status. A byte read or write to port B will not affect handshake status either, since PB6 and PB7 are masked from byte writes to port B when port A is in any of its strobed modes. It is possible, however, to override IBF or IE by an appropriate bit write to PB6 or PB7, respectively.

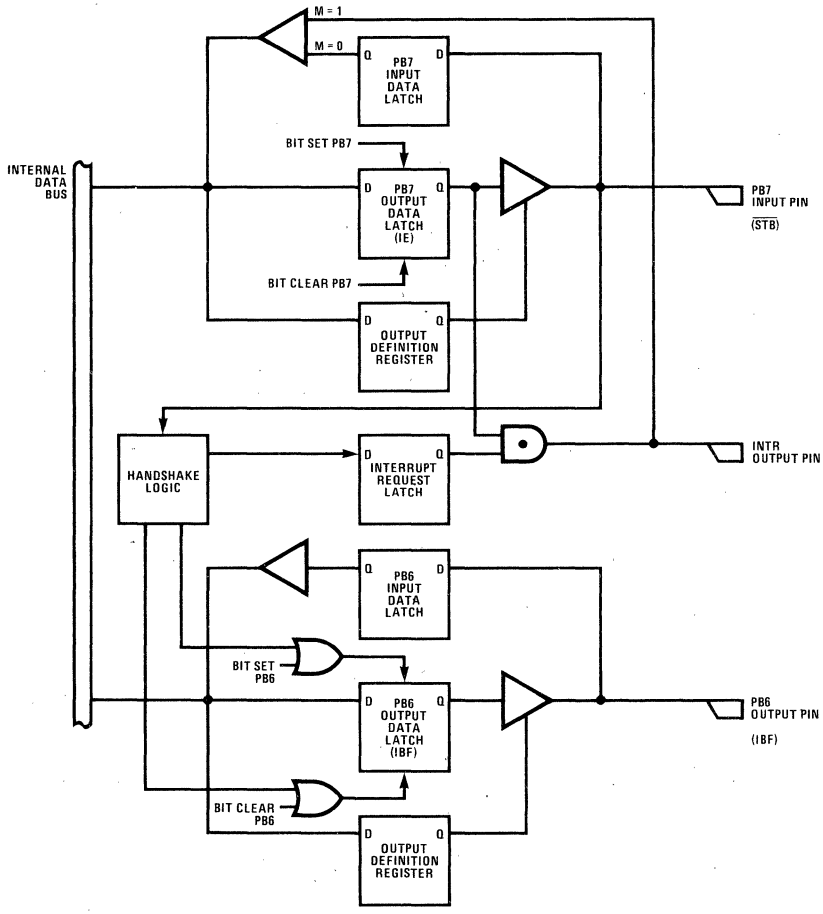


Figure 9. Strobed Input, Mode 2 Handshake Logic

D.3

Strobed Output (Port A) — Mode 3

This mode allows outputting data from the CPU to an asynchronous peripheral. The CPU writes into the output latch of the INS8254; in turn this creates a handshake signal which notifies the peripheral that its bus has new data on it. The peripheral reads the port A bus and returns the handshake signals to their previous state, awaiting the next CPU write. The peripheral bus is always being driven by the port A buffers in this mode. Pertinent timing relationships are shown in figure 10 and a logic diagram showing the handshake signals is shown in figure 11.

The handshake signals associated with mode 3 are the following:

$\overline{ACK}$ ($\overline{Acknowledge}$)

$\overline{ACK}$ is an active-low strobe generated by peripheral to read the data present on its bus. $\overline{ACK}$ drives the INS8254 PB7 input and it sets the $\overline{OBF}$ signal on its leading edge and sets the INTR on its trailing edge; for this to happen, the INS8254 need not be selected.

$\overline{OBF}$ ($\overline{Output\ Buffer\ Full}$)

$\overline{OBF}$ is an active-low signal generated by the INS8254 PB6 output. $\overline{OBF}$ goes low in response to the trailing edge of NWDS for a parallel write to port A and returns high on the leading edge of $\overline{ACK}$. $\overline{OBF}$ being low signals to the peripheral that valid data is now ready to be read on the peripheral bus.

IE (Interrupt Enable)

This is the same as for mode 2.

INTR (Interrupt Request)

When enabled by IE, INTR is set on the trailing edge of $\overline{ACK}$ and reset on the trailing edge of NWDS when a byte write to port A occurs.

The value of INTR can be read from the CPU data bus side by means of a bit read to PB7. This is useful in locating the originator of an interrupt in a multi-interrupt scheme.

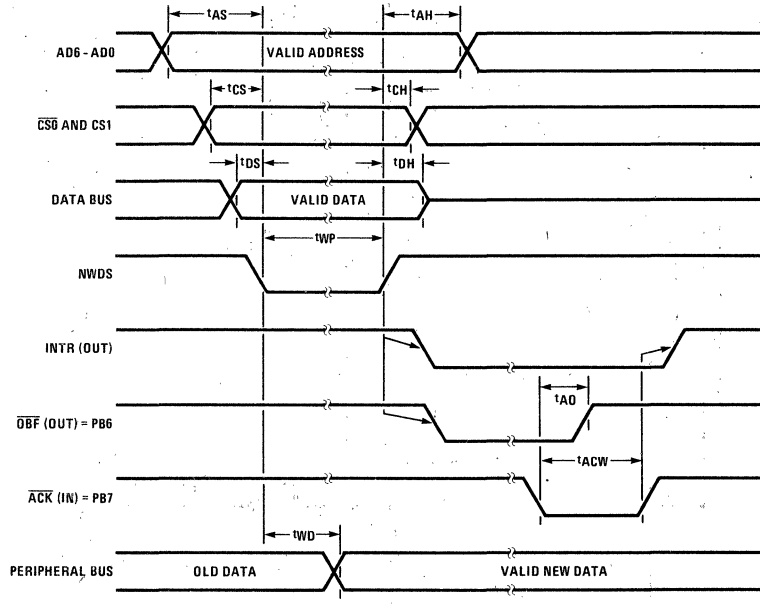
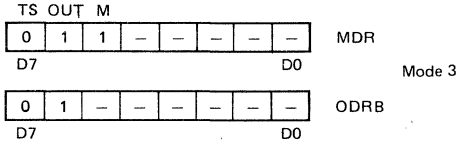


Figure 10. Strobed Output, Mode 3 Timing

Initializing Strobed Output — Mode 3

To initialize for mode 3 operation, the MDR must have "1s" written into bits 5 and 6. A "0" must also be written into bit 7.

The ODRA must have "1s" written into it to identify the bits of port A which will function in mode 3. The ODRB must have a "0" in PB7 in order to make it an input which will receive $\overline{ACK}$ from the peripheral. Also, PB6 must be defined as an output so that it can drive the $\overline{OBF}$ signal. The remaining 6 lower order bits of port B are configured as needed for the basic I/O transactions occurring in port B.



ODRA = "1s" at mode 3 pins.

Writing to the MDR to define mode 3 operation will automatically initialize both $\overline{OBF}$ and INTR such that the INS8254 will be expecting the first strobed operation to take place. Both INTR and $\overline{OBF}$ are initialized high for mode 3, provided IE is set to a "1." If IE is set to "0," INTR will not initialize high.

Handshake Status — Mode 3

Handshake status control signals $\overline{OBF}$ and INTR will be reset low by a CPU STORE instruction only if it is addressed to port A as a *parallel write*. A parallel read or any bit operation to port A will *not* affect handshake status. A word read or write to port B will not affect handshake status either, since PB6 and PB7 are masked from word writes to port B when port A is in any of its strobed modes. It is possible, however, to override $\overline{OBF}$ or IE by an appropriate bit write to PB6 or PB7, respectively.

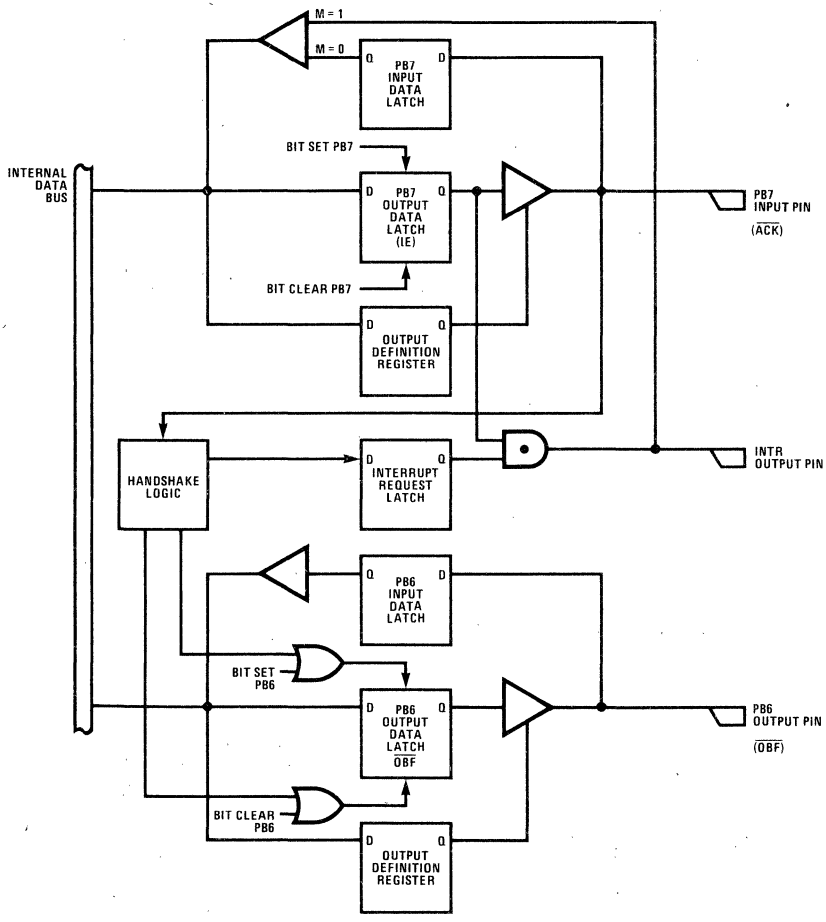


Figure 11. Strobed Output, Mode 3 Handshake Logic

D.3

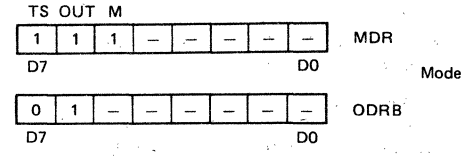
Strobed Output with TRI-STATE Control — Mode 4

This mode is similar to mode 3 in that it uses the same handshake signals and transfers data in the same direction. A timing diagram for mode 4 is shown in figure 12. Handshake logic is shown in figure 11. The main difference from mode 3 is the fact that the peripheral bus is in the TRI-STATE condition at all times except when $\overline{ACK}$ is low, enabling the INS8254 to drive the peripheral bus to its valid state.

The CPU writes into the output latch of the INS8254; this resets INTR and $\overline{OBF}$ but the peripheral bus remains in TRI-STATE until the peripheral responds with a low-going $\overline{ACK}$ strobe. The $\overline{ACK}$ strobe enables the INS8254 port output buffers to drive the peripheral bus active during this strobe time. The leading edge of $\overline{ACK}$ sets the $\overline{OBF}$ and the trailing edge of $\overline{ACK}$ sets INTR. The trailing edge of NWDS for a byte write to port A resets both $\overline{OBF}$ and INTR the same as in mode 3.

Initializing Strobed Output — Mode 4

To initialize for mode 4 operation, the MDR must have "1s" written into bits 5, 6, and 7. The ODRA must have "1s" written into it to identify the bits of port A which will function in mode 4. The ODRB must have a "0" in bit 7 and a "1" in bit 6.



ODRA = "1s" at mode 4 pins.

Writing to the MDR to define mode 4 operation will automatically initialize both $\overline{OBF}$ and INTR high such that the INS8254 will be expecting the first strobed operation to take place, provided IE is set to a "1." If not, INTR will not be initialized high.

Handshake Status — Mode 4

Handshake status control signals $\overline{OBF}$ and $\overline{INTR}$ will be reset low by a CPU STORE instruction only if it is addressed to port A as a parallel write. A parallel read or any bit operation to port A will *not* affect handshake status. A word read or write to port B will not affect handshake status either, since PB6 and PB7 are masked from word writes to port B when port A is in any of its strobed modes. It is possible, however, to override $\overline{OBF}$ or IE by an appropriate bit write to PB6 or PB7, respectively.

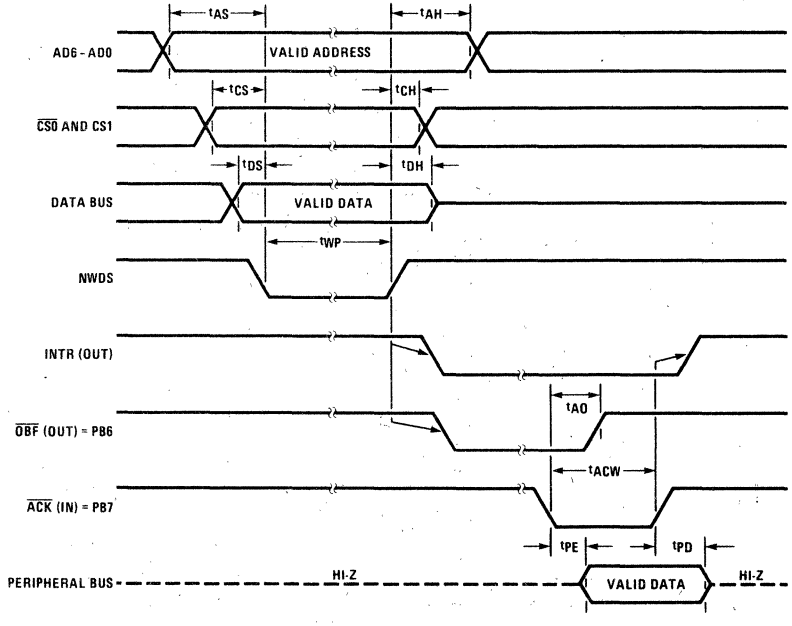


Figure 12. Strobed Output with TRI-STATE Mode 4 Timing

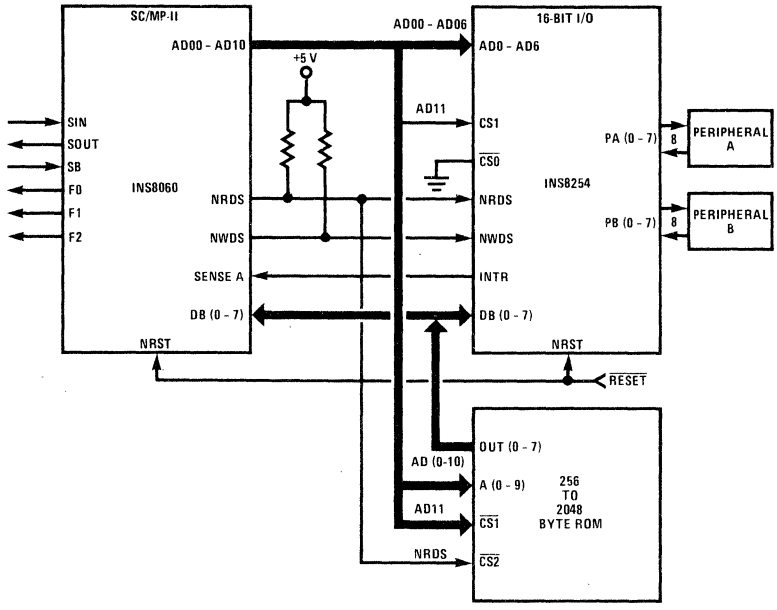


Figure 13. Typical Application – Three-Chip SC/MP Family System with 22 Bits of I/O and Up to 2048 Bytes of ROM.

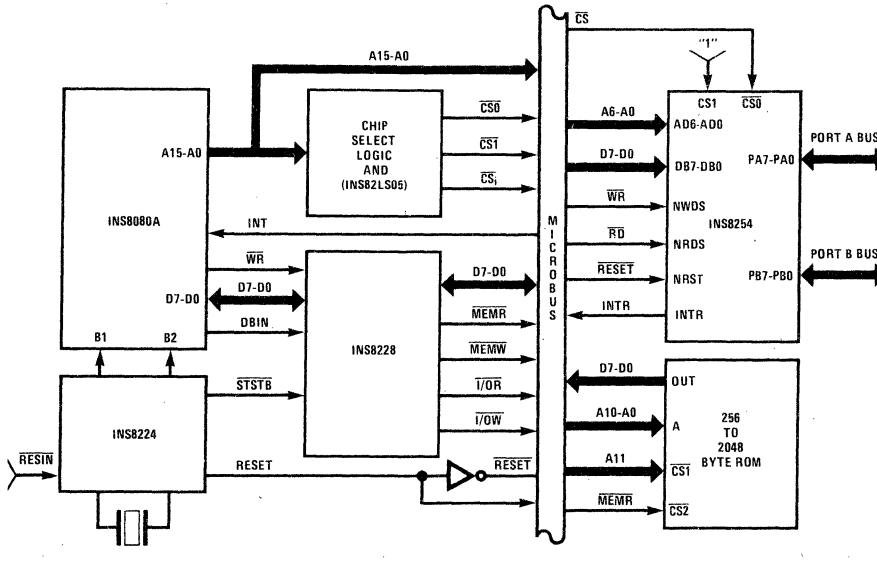
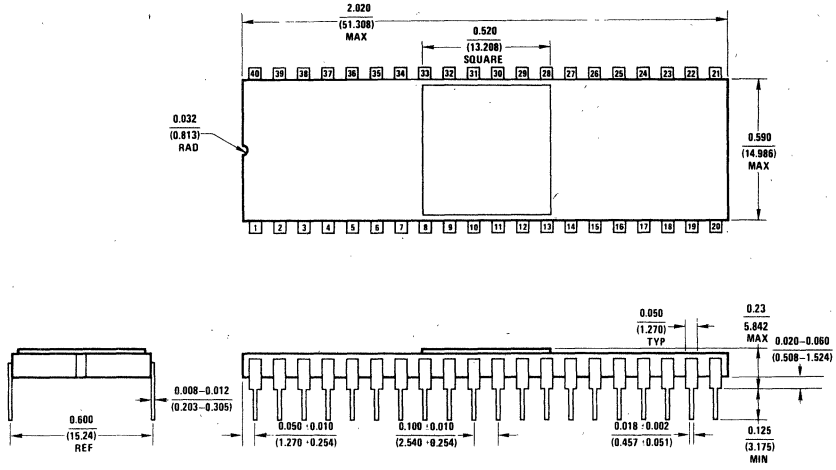


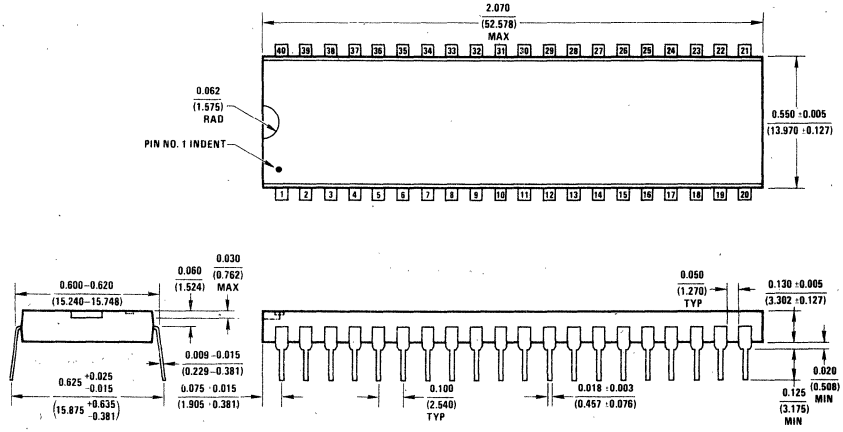
Figure 14. Typical Application – INS8080 System with 16 Bits of I/O and up to 2048 Bytes of ROM.

D.3

Physical Dimensions Inches/Millimeters.



40-Lead Ceramic Dual-in-Line Package (D)



40-Lead Plastic Dual-in-Line Package (N)

Ordering Information

The INS8254 may be ordered through the local National Semiconductor sales representative or by contacting our world or international headquarters listed below.

For "N" Package: INS8254N
For "D" Package: INS8254D

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, California 95051
Tel.: (408) 737-5000
TWX: (910) 339-9240

National Semiconductor GmbH
8000 München 21
Eisenheimerstrasse 61/2
West Germany
Tel.: 089/9 15027
Telex: 05-22772

NS International Inc., Japan
Miyake Building
1-9 Yotsuya, Shinjuku-ku 160
Tokyo, Japan
Tel.: (03) 355-3711
TWX: 232-2015 NSCJ-J

National Semiconductor (Hong Kong) Ltd.
8th Floor,
Cheung Kong Electronic Bldg.
4 Hing Yip Street
Kwun Tong
Kowloon, Hong Kong
Tel.: 3-411241-8
Telex: 73866 NSEHK HX
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Jardim Paulistano
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Telex:
1121008 CABINE SAO PAULO

NS Electronics Pty. Ltd.
Cnr. Stud Rd. & Mtn. Highway
Bayswater, Victoria 3153
Australia
Tel.: 03-729-6333
Telex: 32096

National Semiconductor

Preliminary

JULY 1978

INS8257 Programmable DMA Controller

General Description

The INS8257 is a Direct Memory Access (DMA) controller contained in a standard 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, performs direct control of high speed data transfers to and from memory over four separate channels. Data can be transferred in single bytes or in blocks containing up to 16,384 bytes.

The INS8257 accepts requests for memory access from peripheral devices attached to its four DMA channels and acquires control of the system bus whenever the DMA request is honored. Competing requests are resolved according to a programmable priority scheme (fixed or rotating).

Program control of the INS8257 is exercised via a mode set register and four pairs of channel control registers (one pair per channel). A status register is also included, which provides terminal count status for each channel. The status register also contains a register programming flag, which is a valuable aid in maintaining byte synchronization when programming channel control registers.

The mode set register contains four individual channel enable bits plus option select bits for the following options: rotating priority, extended write, TC stop and auto load.

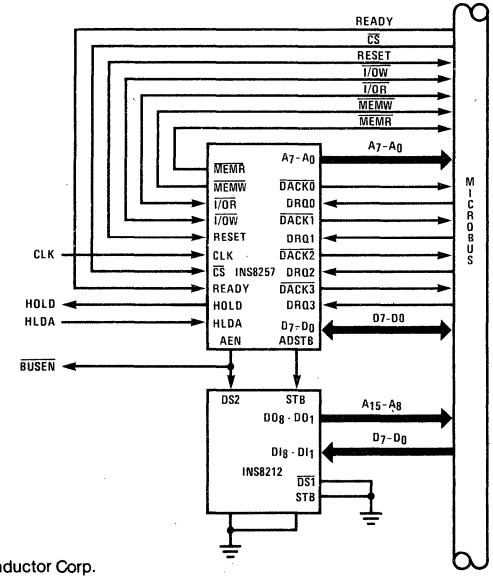
The channel control registers consist of four 16-bit DMA address registers and four 16-bit terminal count (TC) registers. These registers provide the means for controlling DMA transfers on their respective channels.

The auto load feature permits the repetition of block transfers or the chaining of data blocks with a minimum of register initialization required.

Features

- Four-Channel DMA Controller
- Priority DMA Request Logic
- Channel Inhibit Logic
- Terminal Count and Modulo 128 Outputs
- Auto Load Mode
- Single TTL Clock
- Single +5V Supply
- Expandable
- MICROBUS™* Compatible

INS8080 Family CPU Group MICROBUS Configuration



*Trademark, National Semiconductor Corp.

Absolute Maximum Ratings

Maximum Voltage to Any Input with Respect to GND ..... −0.5V to +7V
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Power Dissipation ..... 1 Watt

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, GND = 0V

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	**Input Low Voltage**	−0.5	0.8	Volts	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	Volts	
V_{OL}	Output Low Voltage		0.45	Volts	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4	V_{CC}	Volts	I_{OH} = −150μA for AB, DB and AEN I_{OH} = −80μA for others
V_{HH}	HRQ Output High Voltage	3.3	V_{CC}	Volts	I_{OH} = −80μA
I_{CC}	V_{CC} Current Drain		120	mA	
I_{IL}	Input Leakage		10	μA	V_{IN} = V_{CC}
I_{OFL}	Output Leakage During Float		10	μA	V_{OUT} (Note 1)

Note 1: $V_{CC} > V_{OUT} >$ GND + 0.45V.

Capacitance T_A = 25°C, V_{CC} = *GND* = 0V

Symbol	Parameter	Min	Max	Units	Test Conditions
C_{IN}	**Input Capacitance**		**10**	**pF**	f_C = 1MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to GND

AC Electrical Characteristics T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, GND = 0V (Note 1)

Bus Parameters
READ CYCLE

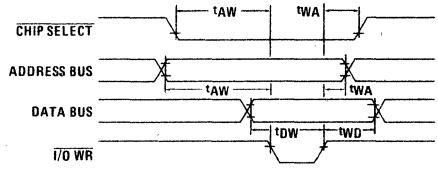
Symbol	Parameter	Min	Max	Units	Test Conditions
t_{AR}	**Adr or CS↓** Setup to RD↓	0		ns	
t_{RA}	Adr or CS↑ Hold from RD↑	0		ns	
T_{RD}	Data Access from RD↓	0	300	ns	(Note 2)
t_{DF}	DB → Float Delay from RD↑	20	150	ns	
t_{RR}	RD Width	250		ns	
WRITE CYCLE					
t_{AW}	Adr Setup to WR↓	20		ns	
t_{WA}	Adr Hold from WR↑	0		ns	
t_{DW}	Data Setup to WR↑	200		ns	
t_{WD}	Data Hold from WR↑	0		ns	
t_{WW}	WR Width	200		ns	
OTHER TIMING					
t_{RSTW}	Reset Pulse Width	300		ns	
t_{RSTD}	Power Supply↑ (V_{CC}) Setup to Reset↓	500		ns	
t_R	Signal Rise Time		20	ns	
t_F	Signal Fall Time		20	ns	
t_{RSTS}	Reset to First IOWR	2		t_{CY}	

Note 1: All timing measurements are made at the following reference voltages unless otherwise specified: Input "1" at 2.0V, "0" at 0.8V; Output "1" at 2.0V, "0" at 0.8V.

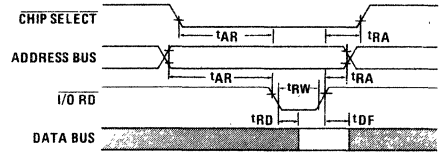
Note 2: C_L = 100pF.

Timing Waveforms (Peripheral Mode)

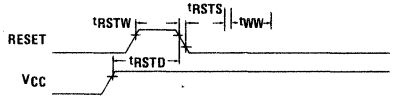
Write Timing



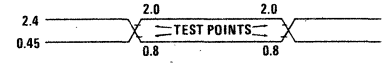
Read Timing



Reset



Input Waveforms for AC Tests



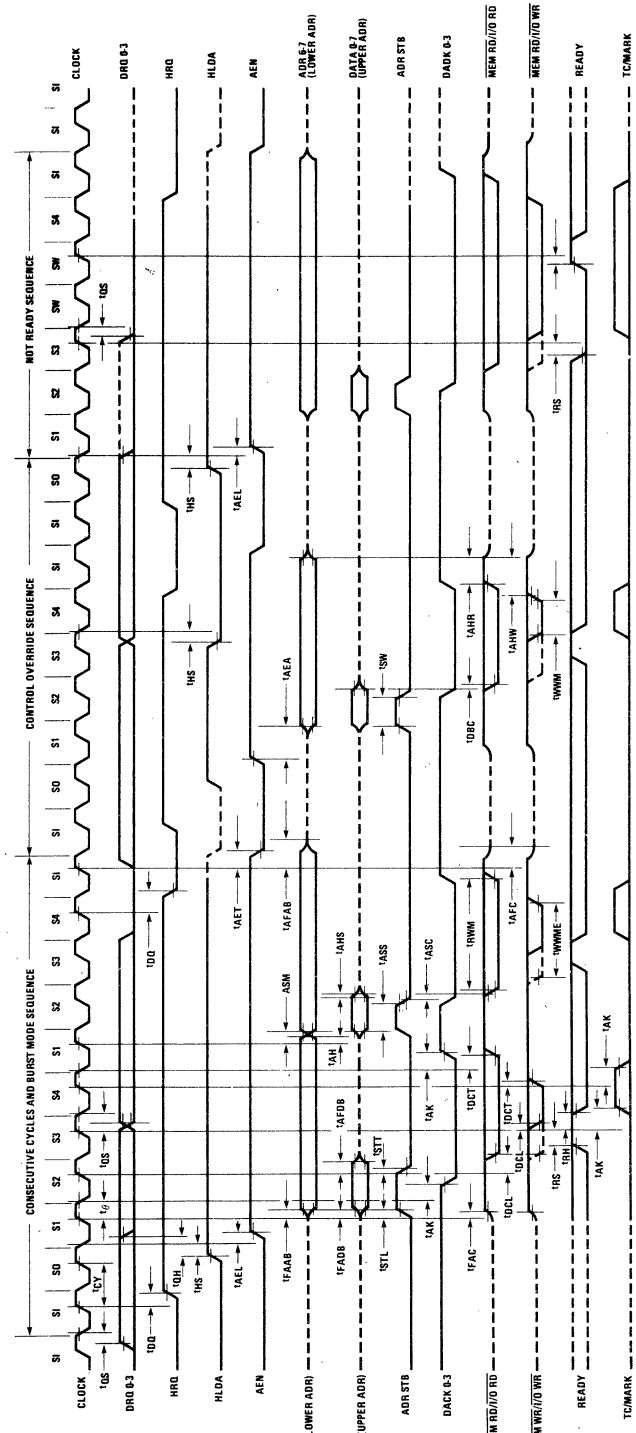
D.3

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$, GND = 0V

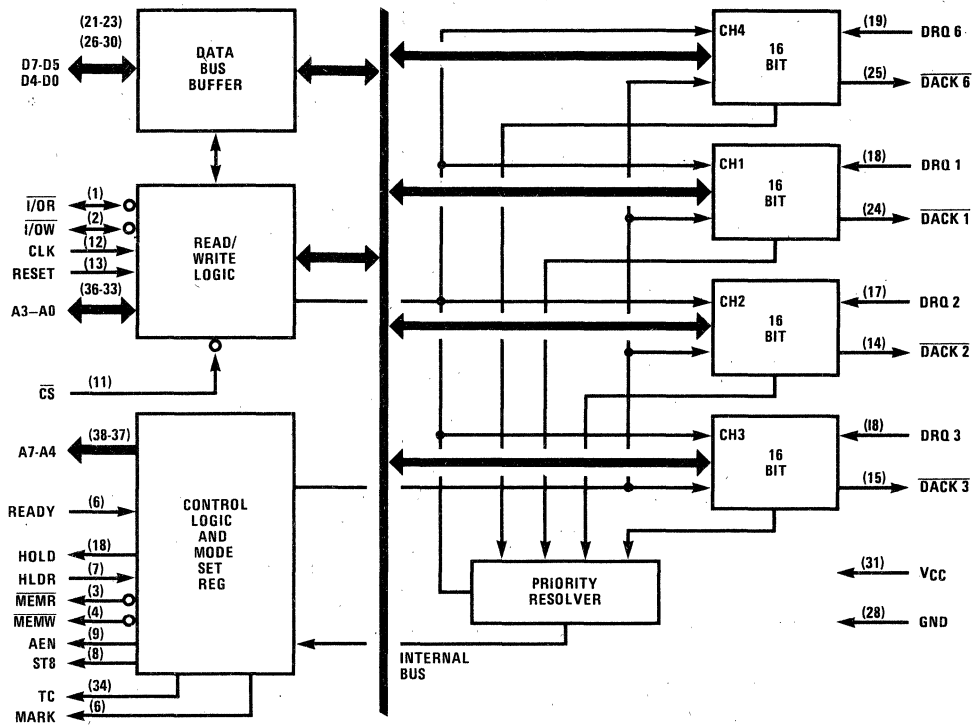
DMA (Master) Mode

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{CY}	**Cycle Time (Period)**	**0.320**	**4**	μs	
t_θ	Clock Active (High)	120	$0.8t_{CY}$	ns	
t_{QS}	DRQ↑ Setup to θ↓(SI,S4)	120		ns	
t_{QH}	DRQ↓ Hold from HLDA↑	0			Tracking Specification
t_{DQ}	HRQ↑ or ↓Delay from θ↑(SI,S4) at 2.0V)		160	ns	Load = 1 TTL
t_{DQ1}	HRQ↑ or ↓Delay from θ↑(SI,S4) (measured at 3.3V)		160	ns	Load = 1 TTL + (R_L = 3.3k), V_{OH} = 3.3V
t_{HS}	HLDA↑ or ↓Setup to θ↓(SI,S4)	100		ns	
t_{AEL}	AEN↑ Delay from θ↓(S1)		300	ns	Load = 1 TTL
t_{AET}	AEN↓ Delay from θ↑(SI)		200	ns	Load = 1 TTL
t_{AEA}	Adr(AB) (Active) Delay from AEN↑(S1)	20		ns	Tracking Specification
t_{FAAB}	Adr(AB) (Active) Delay from θ↑(S1)		250	ns	Load = 1 TTL + 50pF
t_{AFAB}	Adr(AB) (Float) Delay from θ↑(SI)		150	ns	Load = 1 TTL + 50pF
t_{ASM}	Adr(AB) (Stable) Delay from θ↑(S1)		250	ns	Load = 1 TTL + 50pF
t_{AH}	Adr(AB) (Stable) Hold from θ↑(S1)	$t_{ASM} - 50$		ns	Load = 1 TTL + 50pF
t_{AHR}	Adr(AB) (Valid) Hold from Rd↑(S1,SI)	60		ns	Tracking Specification
t_{AHW}	Adr(AB) (Valid) Hold from Wr↑(S1,SI)	300		ns	Tracking Specification
t_{FADB}	Adr(DB) (Active) Delay from θ↑(S1)		300	ns	Load = 1 TTL + 50pF
t_{AFDB}	Adr(DB) (Float) Delay from θ↑(S2)	$t_{SST} + 20$	250	ns	Load = 1 TTL + 50pF
t_{ASS}	Adr(DB) Setup to AdrStb↓(S1-S2)	100		ns	Tracking Specification
t_{AHS}	Adr(DB) (Valid) Hold from AdrStb↓(S2)	50		ns	Tracking Specification
t_{STL}	AdrStb↑ Delay from θ↑(S1)		200	ns	Load = 1 TTL
t_{STT}	AdrStb↓ Delay from θ↑(S2)		140	ns	Load = 1 TTL
t_{SW}	AdrStb Width (S1-S2)	$t_{CY} - 100$		ns	Tracking Specification
t_{ASC}	Rd↓ or Wr(Ext)↓ Delay from AdrStb↓(S2)	70		ns	Tracking Specification
t_{DBC}	Rd↓ or Wr(Ext)↓ Delay from Adr(DB) (Float)(S2)	20		ns	Tracking Specification
t_{AK}	DACK↑ or ↓Delay from θ↓(S2,S1) and TC/Mark↑ Delay from θ↑(S3) and TC/Mark↓ Delay from θ↑(S4)		250	ns	Load = 1 TTL, $\Delta t_{AK} < 50ns$
t_{DCL}	Rd↓ or Wr(Ext)↓ Delay from θ↑(S2) and Wr↓ Delay from θ↑(S3)		200	ns	Load = 1 TTL + 50pF, $\Delta t_{DCL} < 50ns$
t_{DCT}	Rd↑ Delay from θ↓(S1,SI) and Wr↑ Delay from θ↑(S4)		200	ns	Load = 1 TTL + 50pF, $\Delta t_{DCT} < 50ns$
t_{FAC}	Rd or Wr (Active) from θ↑(S1)		300	ns	Load = 1 TTL + 50pF
t_{AFC}	Rd or Wr (Float) from θ↑(SI)		150	ns	Load = 1 TTL + 50pF
t_{RWM}	Rd Width (S2-S1 or SI)	$2t_{CY} + t_\theta - 50$		ns	Tracking Specification
t_{WWM}	Wr Width (S3-S4)	$t_{CY} - 50$		ns	Tracking Specification
t_{WWME}	Wr(Ext) Width (S2-S4)	$2t_{CY} - 50$		ns	Tracking Specification
t_{RS}	READY Setup Time to θ↑(S3,Sw)	30		ns	
t_{RH}	READY Hold Time from θ↑(S3,Sw)	20		ns	

Timing Waveforms (DMA Mode)



INS8257 Functional Block Diagram



NOTE: APPLICABLE PINOUT NUMBERS ARE INCLUDED WITHIN PARENTHESES.

INS8257 Functional Pin Description

The following describes the functions of all INS8257 input/output pins. Some of these descriptions refer to internal circuits.

INPUT SIGNALS

Data Request (DRQ0-DRQ3): Each channel interface has a separate DRQ input, which is used by the peripheral to request DMA cycles. To make a request for DMA service, a peripheral raises its DRQ line and holds it high so long as DMA cycles are needed. The peripheral drops its DRQ n when the DMA acknowledge ($\overline{DACK}$ n) is received for the last DMA cycle in the data block. See Output Signals for a description of the $\overline{DACK}$ signal.

Clock (CLK): This clock is supplied by the $\phi 2$ (TTL) output of the INS8224 Clock Generator and Driver (pin 6) or its equivalent.

Reset: When raised to the high logic level, this input clears all INS8257 registers and control lines, excepting the channel address registers. It would normally be supplied by the INS8224 Clock Generator and Driver (pin 1) or its equivalent.

Chip Select ($\overline{CS}$): When this input is low, the chip is selected. This enables the INS8257 read/write interface logic.

Ready: This input inserts wait states into the INS8257's memory read and write cycles if required by the addressed memory.

Hold Acknowledge (HLDA): When high, this input from the CPU notifies the INS8257 that it has control of the system bus.

OUTPUT SIGNALS

DMA Acknowledge ($\overline{DACK3}$-$\overline{DACK0}$): Each channel interface has a separate DMA acknowledge output. When a channel's DMA request (DRQ) is honored by the priority logic, that channel's $\overline{DACK}$ output is brought low to notify the peripheral that it has been selected for a DMA cycle.

Address Lines (A7-A4): These four TRI-STATE® address outputs carry bits 7 through 4 of the memory address produced by the INS8257 during the addressing phase of DMA cycles.

Hold Request (HRQ): The INS8257 raises this output in order to request control of the system bus.

Memory Read ($\overline{MEMR}$): The INS8257 brings this TRI-STATE output low in order to read data from memory during DMA read operations.

Memory Write ($\overline{MEMW}$): The INS8257 brings this TRI-STATE output low in order to write data into memory during DMA write operations.

Address Strobe (ADSTB): The INS8257 uses this output to strobe address bits A15-A8 from the INS8257's bidirectional data lines (D7-D0) into the memory's address buffer (e.g., INS8212).

Address Enable (AEN): The INS8257 may use this output to disable the system data bus and the system control bus. It does this by applying AEN to the Bus Enable input of the CPU's System Controller chip (e.g., INS8228). It may also be used to isolate non-DMA devices from the system address bus during DMA operations. This is done by applying AEN to the enable input of each address bus driver chip to be disabled.

Terminal Count (TC): The INS8257 uses this output to notify the selected peripheral that the current DMA cycle is the last cycle in the data block. If the mode set register's TC Stop bit (bit 6) is set, the selected channel is automatically disabled at the end of that DMA cycle. The INS8257 control logic issues TC when the terminal count register decrements to 0 (excluding bits 14 and 15).

Modulo 128 Mark (MARK): The INS8257 uses this output to notify the selected peripheral that 128 DMA cycles have occurred since the previous MARK output. MARK always occurs at 128 (and all multiples of 128) cycles from the end of the data block.

INPUT/OUTPUT SIGNALS

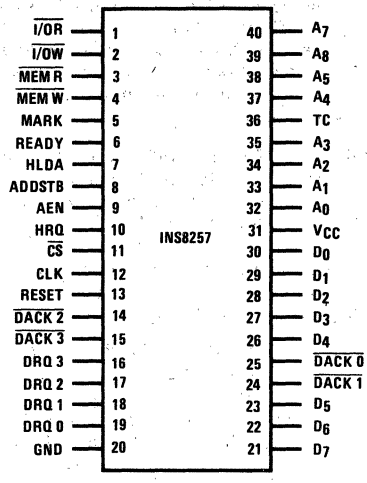
Data (D0-D7) Bus: This bus, which comprises eight TRI-STATE input/output lines, provides for bidirectional communication between the INS8257 and the CPU. When the CPU is initializing the INS8257, this bus may carry data for the DMA address register, terminal count register or mode set register. Read data is carried by these lines when the CPU reads a DMA address register, a terminal count register or the status register. During the address phase of a DMA cycle, these lines carry the eight high-order bits of the memory address. During the data transfer phase of a DMA cycle, this bus carries the data byte being written into or read from memory.

I/O Read ($\overline{I/OR}$): This is a low-true, bidirectional TRI-STATE line. It is used by the CPU to read INS8257 registers (DMA address register, terminal count register or status register) and by the INS8257 to input data from a selected peripheral during DMA write operations.

I/O Write ($\overline{I/OW}$): This is a low-true, bidirectional TRI-STATE line. It is used by the CPU to write into INS8257 registers (DMA address register, terminal count register or mode set register) and by the INS8257 to output data to a selected peripheral during DMA read operations.

Address Lines (A3-A0): These lines, which carry the four least significant system address bits, are bidirectional. They function as input lines when the CPU uses them to select one of the INS8257 registers. They function as output lines during DMA cycles when they carry the four least significant bits of the memory address.

Pin Configuration



INS8257 Programming Information

This section provides basic information for programming the INS8257 and describes the status information available to the programmer. Table 1 summarizes the bus controls needed to output control information to the INS8257 and to read INS8257 status.

Table 1. INS8257 System Bus Controls

Function	A_3	A_2	A_1	A_0	(Note 1) $\overline{I/OW}$	(Note 1) $\overline{I/OR}$	CS
Load Ch0 DMA Address Register	0	0	0	0	0	1	0
Load Ch1	0	0	1	0	0	1	0
Load Ch2	0	1	0	0	0	1	0
Load Ch3	0	1	1	0	0	1	0
Read Ch0 DMA Address Register	0	0	0	0	1	0	0
Read Ch1	0	0	1	0	1	0	0
Read Ch2	0	1	0	0	1	0	0
Read Ch3	0	1	1	0	1	0	0
Load Ch0 TC Register	0	0	0	1	0	1	0
Load Ch1	0	0	1	1	0	1	0
Load Ch2	0	1	0	1	0	1	0
Load Ch3	0	1	1	1	0	1	0
Read Ch0 TC Register	0	0	0	1	1	0	0
Read Ch1	0	0	1	1	1	0	0
Read Ch2	0	1	0	1	1	0	0
Read Ch3	0	1	1	1	1	0	0
Load Mode Set Register	1	0	0	0	0	1	0
Read Status Register	1	0	0	0	1	0	0

Note 1: First $\overline{I/OW}$ or $\overline{I/OR}$ loads or reads low-order byte, second $\overline{I/OW}$ or $\overline{I/OR}$ loads or reads high-order byte.

PROGRAMMING

There are three types of registers that must be initialized:

1. Four DMA address registers (one per channel)
2. Four terminal count registers (one per channel)
3. One mode set register.

The DMA address registers and TC registers can be programmed in any order. However, the mode set register should not be programmed until after the DMA address and TC registers are initialized. This precaution is intended to prevent invalid access of memory in the event a spurious DMA request (DRQ n) is generated.

NOTE

For any transfer on the system data bus involving position-weighted bits, D7 = most significant bit and D0 = least significant bit.

Because each channel register is two bytes wide, two I/O read or write operations are required to read or load an entire register. When one of these registers is selected by the CPU, INS8257 logic automatically accesses the register's lower half for the first I/O operation and the upper half for the second I/O operation.

Part of this logic is a first/last flip-flop (F/L) that toggles with each I/O operation directed to a channel register. This flip-flop controls which half of the register is affected. It is essential that the state of this flip-flop not be lost through any of the following conditions:

- Loading the mode set register when only the lower half of a channel register has been accessed,
- Clocking $\overline{CS}$ while either $\overline{I/OR}$ or $\overline{I/OW}$ is active,
- Allowing the microprocessor to be interrupted when only the lower half of a channel register has been accessed,
- Not completing both halves of a channel register read or load sequence.

LOADING DMA ADDRESS REGISTERS

Each channel is assigned a separate 16-bit DMA address register. This register is loaded with the starting memory address for the next DMA operation to be conducted on the corresponding channel.

Loading of a single DMA address register requires two I/O write operations, with the chip selected by CS and the register selected by system address lines A3-A0.

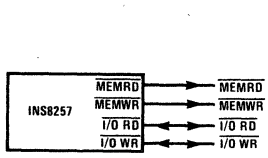
The DMA address information is presented to the INS8257 via the system data bus in the following manner:

	DMA Addr Register		
First $\overline{I/OW}$	LS Byte	←	D7-D0
Second $\overline{I/OW}$	MS Byte	←	D7-D0

LOADING TC REGISTERS

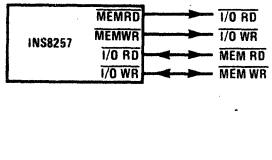
Each channel is assigned a separate TC register. This register's 14 least significant bits are loaded with a value equal to one less than the number of DMA cycles in the channel's next block transfer. For example, if the next DMA operation for channel 0 will require 32 (hex 20) DMA cycles, the value 31 (hex 1F) should be loaded into channel 0's TC register.

Bits 14 and 15 of each TC register are loaded with mode control bits for the corresponding channel. There are three possible operating modes to be specified by these bits. How they are implemented depends on whether the INS8257 is part of a standard (isolated) I/O bus structure or whether a memory-mapped I/O configuration is used. Figure 1 identifies the mode control functions of TC register bits 14 and 15 for both I/O schemes.



Isolated I/O

Function	Bit 15	Bit 14
DMA Verify	0	0
DMA Write	0	1
DMA Read	1	0
Illegal	1	1



Memory Mapped I/O

Function	Bit 15	Bit 14
DMA Verify	0	0
DMA Write	1	0
DMA Read	0	1
Illegal	1	1

Figure 1. TC Register Mode Control Bits

The DMA verify mode allows pseudo DMA cycles to be performed in which no data is transferred. In this mode, the INS8257 responds to DMA requests in the same manner as in other modes, except that $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$, $\overline{\text{I/OR}}$ and $\overline{\text{I/OW}}$ are inhibited. This mode allows a peripheral to cycle through a block of data for internal control or housekeeping purposes without affecting memory.

In a DMA read cycle, the INS8257 issues $\overline{\text{MEMR}}$ in order to read the contents of the addressed memory location and I/O to write that same data byte into the selected peripheral.

In a DMA write cycle, the INS8257 issues $\overline{\text{I/OR}}$ in order to read the data byte presented by the selected peripheral and $\overline{\text{MEMW}}$ to write that same data byte into the addressed memory location.

Loading of a single TC register requires two I/O write operations, with the chip selected by $\overline{\text{CS}}$ and the register selected by system address lines A3-A0.

The terminal count information is presented to the INS8257 via the system data bus in the following manner:

	TC Register		
First $\overline{\text{I/OW}}$	LS Byte	←	D7-D0
Second $\overline{\text{I/OW}}$	MS Byte	←	D7-D0

LOADING MODE SET REGISTER

The contents of the mode set register are used to individually enable/disable the four DMA channels and to selectively implement four optional functions in the INS8257. Mode set register bit functions are identified in figure 2 and are described in the following paragraphs.

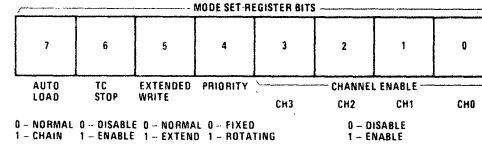


Figure 2. Mode Set Register Bit Functions

Loading the mode set register requires a single I/O write operation, with the chip selected by $\overline{\text{CS}}$ and the register selected by A3-A0.

DMA Channel Enables (Bits 3-0)

These four bits can be individually set or reset by the program in order to enable or disable their respective channels. If the TC stop bit (mode set register bit 6) is set, the channel enable bit of the currently selected channel is automatically reset after Terminal Count (TC) goes true. This assures the disabling of a channel after it completes its DMA operations. If the TC stop bit is not set, the program should reset any channel enable bit whose DMA address and TC registers are not currently valid.

Rotating Priority Option (Bit 4)

When this bit = 0 (e.g., following power on reset), the priority control logic resolves competing DMA requests according to a fixed priority scheme. In this fixed priority mode, channel 0 always has highest priority and channel 3 always has lowest priority.

When mode set register bit 4 is set, the rotating priority mode is selected. In this mode, the completion of a DMA cycle will cause the channel just serviced to be assigned lowest priority. All other channels then move up one priority level. Channel 0 will always have highest priority after a reset or mode set operation.

Extended Write (Bit 5)

The extended write option is useful when the INS8257 is accessing a high-speed memory or I/O device whose Ready response is activated by the leading edge of $\overline{\text{MEMW}}$ or $\overline{\text{I/OW}}$. Ordinarily, the late arrival of Ready would cause the INS8257 to insert a

wait state into the DMA cycle, even though the device is capable of completing the transfer without that wait state. This unnecessary wait state can be avoided by use of the extended write option.

When the extended write bit (bit 5) is set, the INS8257 generates $\overline{\text{MEMW}}$ or $\overline{\text{I/OW}}$ earlier in the DMA cycle. This permits the memory or I/O device to issue its Ready response earlier in the cycle, thereby avoiding unnecessary wait states in the INS8257.

TC Stop Bic (Bit 6)

Setting this bit assures that a channel will be disabled as soon as it performs the last DMA cycle in a programmed DMA transfer. When Terminal Count (TC) goes true at the end of a transfer sequence, the channel enable bit of the currently selected channel is automatically reset. This channel remains disabled until its channel enable bit is set again by the program.

Auto Mode (Bit 7)

This mode provides the means for automatically repeating block transfers or for chaining of multiple block transfers, without requiring direct control by the program between blocks. In this mode, the channel 2 and channel 3 registers operate in tandem. The contents of the channel 2 registers are used to control the first DMA operation.

The channel 3 registers temporarily store the parameters required for the next block to be transferred. Upon completion of the first DMA block transfer, the contents of the channel 3 registers are automatically copied into the channel 2 registers and the next block is transferred under channel 2 register control.

NOTE

The TC stop bit does not affect the channel 2 enable bit when in auto load mode.

When the auto load bit is set, writing new parameters into the channel 2 registers automatically loads those same parameters into the channel 3 registers. In this way, all parameters required for a repeat block transfer are loaded in a single channel programming sequence.

If different parameters are required for the second block transfer (for chaining block transfers), channel 3 can be programmed after channel 2.

The channel 3 register contents are copied into the channel 2 registers during an update cycle, which occurs right after the TC output goes true. Each time an update cycle begins, an update flag is set. This flag is available to the program via bit 4 of the status register. Following re-initialization of channel 2, the first DMA cycle of the new data block begins. The update flag is reset when this first DMA cycle is completed.

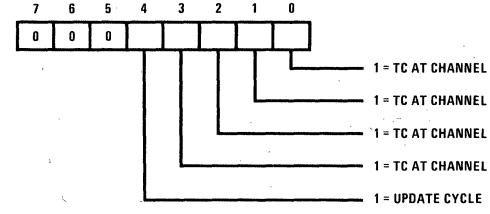
To continue a block chaining sequence, the auto load bit is left in the set state and the channel 3 registers are programmed for the next data block. Before loading new parameters into the channel 3 registers, the update flag should be tested to be certain the channel 2 update operation has been completed.

NOTE

DMA transfers can be performed on channel 3 when the auto load bit is set. However, any parameters loaded into channel 3 registers will be copied into channel 2 registers during the next update cycle.

Reading Status Register

Five status bits are available to the system at one register address.

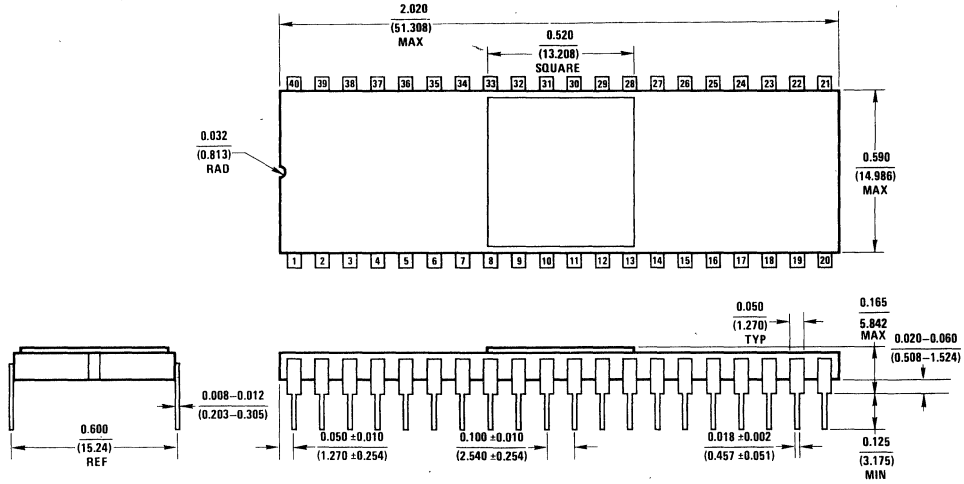


A channel's TC status bit is set when that channel is selected and the TC output is activated. Reading the status register resets all TC bits.

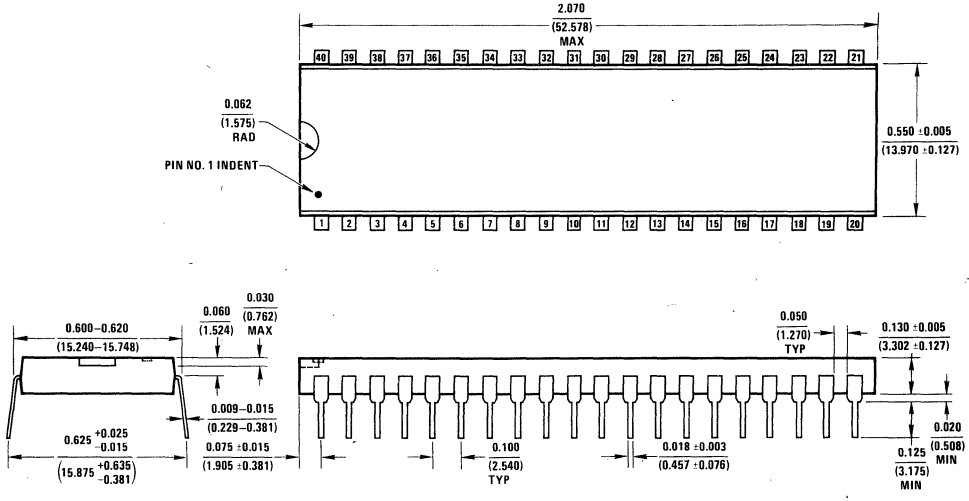
The update flag (bit 4) is set at the start of an update cycle and resets at the end of the update cycle. The update flag is also cleared by resetting the auto load bit and by resetting the INS8257. It is not cleared when the status register is read.

Reading the status register requires a single I/O read operation, with the chip selected by CS and the register selected by system address lines A3-A0.

Physical Dimensions inches (millimeters)



40-Lead Ceramic Dual-In-Line Package (D)
Order Number INS8257D
NS Package Number D40C



40-Lead Plastic Dual-In-Line Package (N)
Order Number INS8257N
NS Package Number N40A

D.3

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National Semiconductor

Preliminary
JULY 1978

INS8259 Programmable Interrupt Controller

General Description

The INS8259 is a Programmable Interrupt Controller chip contained in a standard 28-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, functions as a versatile interrupt management device in a microcomputer system.

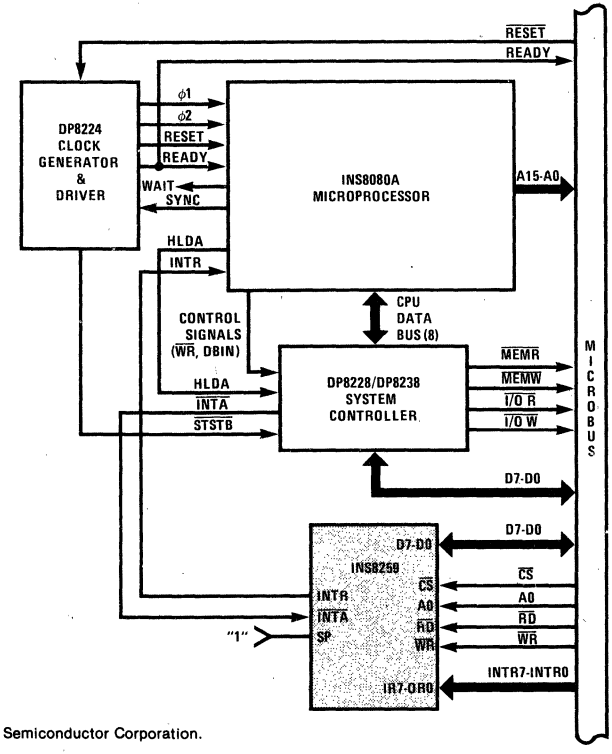
Each INS8259 resolves interrupt requests from up to eight different sources. These devices can be cascaded to provide interrupt management of up to 64 levels with no other circuitry required.

The INS8259 minimizes software and real time overhead when handling multi-level priority interrupts. Its four operating modes allow the device to satisfy diverse system requirements.

Features

- Performs Priority Control of up to Eight Interrupt Levels
- Can be Expanded to Handle up to 64 Levels Through Cascading
- Four Programmable Operating Modes
- Programmable Interrupt Vectors, Allowing Service Routines to be Located Anywhere in Memory
- Interrupt Request Inputs Can be Individually Masked
- TRI-STATE® TTL Drive Capability for Bidirectional Data and Control Buses
- Single +5 Volt Power Supply
- 28-Pin Dual-in-Line Package
- MICROBUS™* Compatible

INS8080 Family CPU Group to MICROBUS Configuration



*A trademark of National Semiconductor Corporation.

Absolute Maximum Ratings

Ambient Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 1 Watt

Note: Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics

T_A = 0°C to +70°C; V_{CC} = +5V ± 5%, GND = 0V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.5V	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400μA
V_{OH-INT}	Interrupt Output High Voltage	2.4 3.5			V V	I_{OH} = −400μA I_{OH} = −50μA
$I_{IL(IR0-7)}$	Input Leakage Current for IR_{0-7}			−300 10.	μA μA	V_{IN} = 0V V_{IN} = V_{CC}
I_{IL}	Input Leakage Current for Other Inputs			10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage			±10	μA	V_{OUT} = 0.45V to V_{CC}
I_{CC}	V_{CC} Supply Current			100	mA	

Capacitance

T_A = +25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
C_{IN}	Input Capacitance			20	pF	f_C = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins to ground

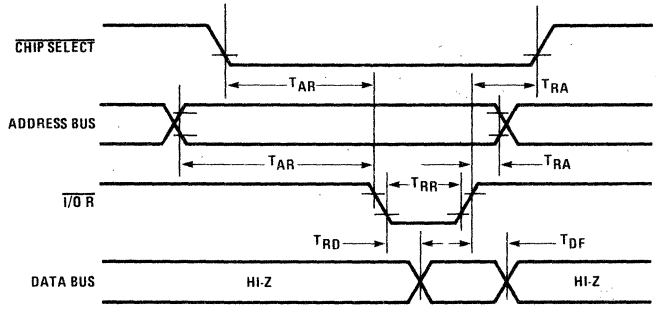
AC Electrical Characteristics

T_A = 0°C to +70°C; V_{CC} = +5.0V ± 5%, GND = 0V

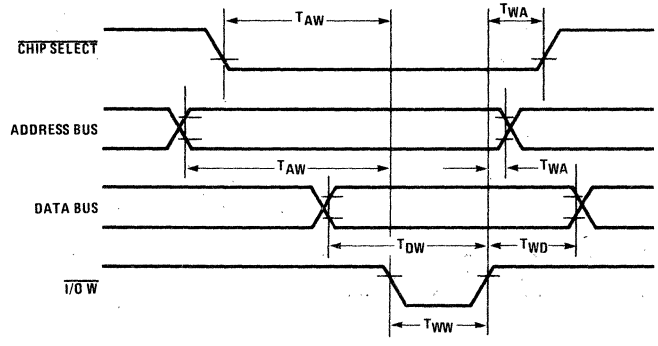
Symbol	Parameter	Min	Max	Unit	Test Conditions
BUS PARAMETERS					
READ					
t_{AR}	$\overline{CS}/A_0$ Stable before $\overline{RD}$ or $\overline{INTA}$	50		ns	
t_{RA}	$\overline{CS}/A_0$ Stable after $\overline{RD}$ or $\overline{INTA}$	5		ns	
t_{RR}	$\overline{RD}$ Pulse Width	420		ns	
t_{RD}	Data Valid from $\overline{RD}/\overline{INTA}$		300	ns	C_L = 100pF
t_{DF}	Data Float after $\overline{RD}/\overline{INTA}$		200		C_L = 100pF
t_{DF}		20		ns	C_L = 20pF
WRITE					
t_{AW}	A_0 Stable before $\overline{WR}$	50		ns	
t_{WA}	A_0 Stable after $\overline{WR}$	20		ns	
t_{WW}	$\overline{WR}$ Pulse Width	400		ns	
t_{DW}	Data Valid to $\overline{WR}$ (T.E.)	300		ns	
t_{WD}	Data Valid after $\overline{WR}$	40		ns	
OTHER TIMINGS					
t_{IW}	Width of Interrupt Request Pulse	100		ns	
t_{INT}	INT ↑ after IR ↑	400		ns	
t_{IC}	Cascade Line Stable after $\overline{INTA}$ ↑	400		ns	

Timing Waveforms

Read Timing



Write Timing



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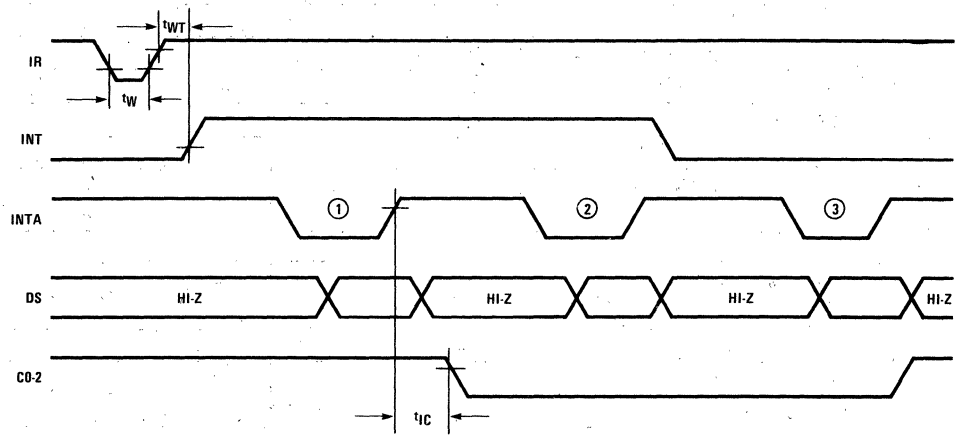
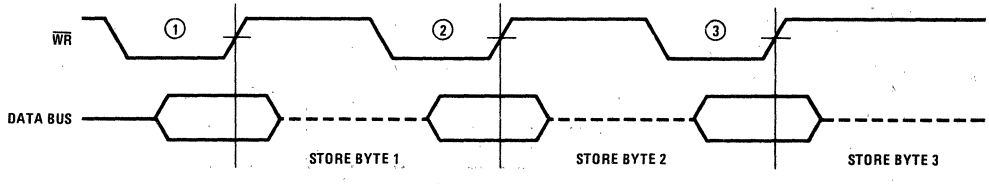
Timing Waveforms (cont'd.)

Other Timing

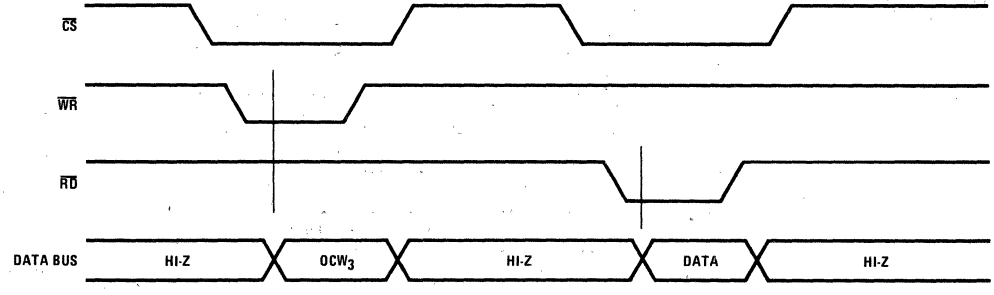


NOTE: INTERRUPT REQUEST MUST REMAIN "HIGH" (AT LEAST) UNTIL LEADING EDGE OF FIRST $\overline{INTA}$.

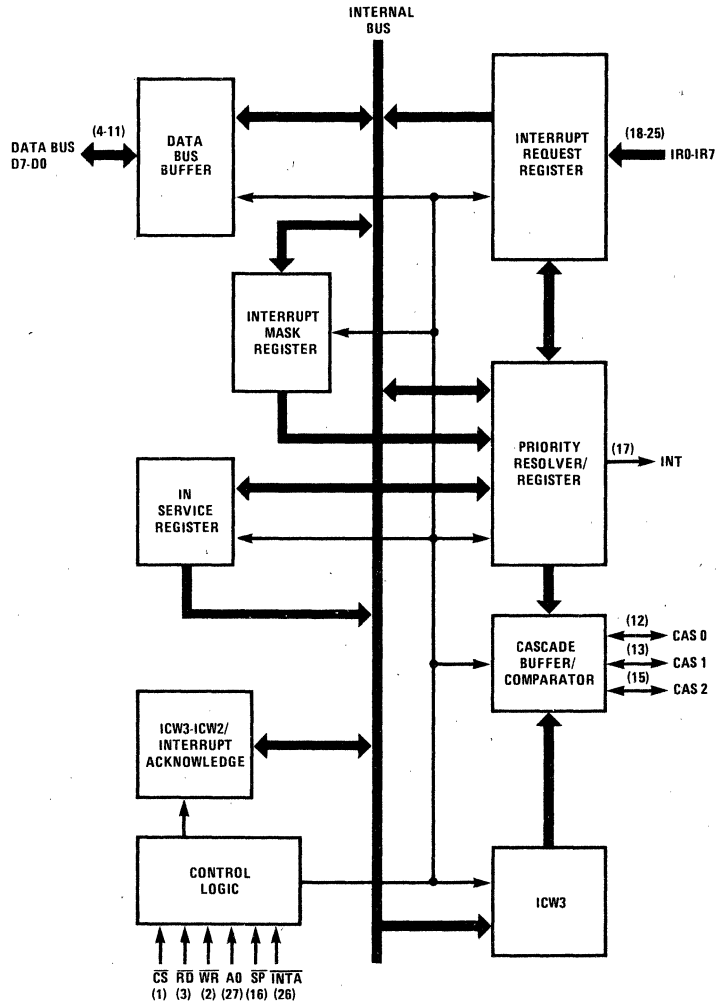
Initialization Sequence



Read Status/Poll Mode



INS8259 Block Diagram



INS8259 Functional Pin Description

The following describes the functions of all INS8259 input/output pins. Some of these descriptions refer to internal circuits.

INPUT SIGNALS

Chip Select ($\overline{CS}$): When low, the device is selected, enabling communication between the INS8259 and the microprocessor.

Read ($\overline{RD}$): When low, allows the microprocessor to read contents of Interrupt Request Register (IRR), In Service Register (ISR) or Interrupt Mask Register (IMR) or the BCD value of the current interrupt level.

Write ($\overline{WR}$): When low, allows the microprocessor to write control words (ICWs and OCWs) to the INS8259.

A0: This input is used in conjunction with the $\overline{WR}$ signal to write command words into specific command registers and with the $\overline{RD}$ signal to read specific status registers. A0 can be controlled via one of the microprocessor address lines.

Interrupt Acknowledge ($\overline{INTA}$): This input is generally provided by the CPU group's System Controller element (e.g., INS8228). Each INT is acknowledged by a sequence of three $\overline{INTA}$ pulses, which causes the INS8259 to output a three-byte CALL instruction onto the Data Bus.

Interrupt Request (IR7-IR0): These eight inputs are used by external circuits to request servicing by the CPU. A low-to-high transition on one of these lines represents a new interrupt request from the circuit controlling that line. Each positive transition on the IR lines causes the INS8259 to issue a separate interrupt to the microprocessor. The IR line must remain high through the first $\overline{INTA}$ pulse or the INT line will go low. Concurrent interrupt requests are resolved according to their relative positions in the priority scheme. Typically, an active (high) IR input is reset by the interrupt service routine associated with that line.

Slave Program ($\overline{SP}$): This control input is used in systems having cascaded INS8259s, where one INS8259 operates as the master and all others operate as slaves. A high level at the $\overline{SP}$ input appoints that INS8259 as master, while a low level assigns the role of slave.

OUTPUT SIGNALS

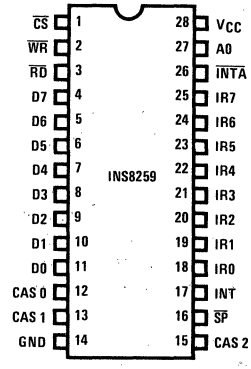
Interrupt (INT): This output is applied to the microprocessor's interrupt input (e.g., pin 14 of INS8080A).

INPUT/OUTPUT SIGNALS

Data (D7-D0) Bus: This bus, which comprises eight TRI-STATE input/output lines, provides bidirectional communication between the INS8259 and the CPU. Command words, status words and CALL instructions are transferred over these lines.

Cascade (CAS2-CAS0): These three lines are used in systems having cascaded INS8259s. The master INS8259 outputs the three-bit ID of a slave device on CAS2-CAS0 in order to select that slave for interrupt servicing.

Pin Configuration



INS8259 Programming Information

Two types of command words are used to program the INS8259. These are:

- Initialization Command Words (ICWs) — A sequence of two or three ICWs is required to prepare the INS8259 for operation. Two words are used if a single INS8259 is being initialized. A three-word sequence is used if a master/slave configuration is being initialized. See figure 1 for an illustration of this sequence. Each ICW is timed by a separate WR pulse.
- Operation Command Words (OCWs) — These command words are used to specify various operating characteristics of the INS8259 and to read the status of certain registers.

Figure 1 summarizes the bus controls needed to output command words to the INS8259 and to read INS8259 status.

A0	D4	D3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Operation
READ						
0			0	1	0	(Note 1) IRR, ISR or Interrupt Level to Data Bus
1			0	1	0	IMR to Data Bus
WRITE						
0	1	X	1	0	0	Data Bus to ICW1
0	0	0	1	0	0	Data Bus to OCW2
0	0	1	1	0	0	Data Bus to OCW3
1	X	X	1	0	0	(Note 2) Data Bus to OCW1, ICW2, ICW3
DISABLE						
X	X	X	1	1	0	Data Bus to Hi-Z
X	X	X	X	X	1	Data Bus to Hi-Z

Notes:

1. Selection of IRR, ISR or Interrupting Level controlled by OCW3 written prior to the Read operation.
2. Proper sequence set by on-chip sequencer.

Figure 1. Basic Control for INS8259 I/O Operations

INITIALIZATION COMMAND WORDS (ICWs)

Figure 2 summarizes the command format for ICW1, ICW2 and ICW3. There are two variations of the ICW3 format, one for the master device and one for the slaves.

Figure 3 describes the INS8259 initialization sequence.

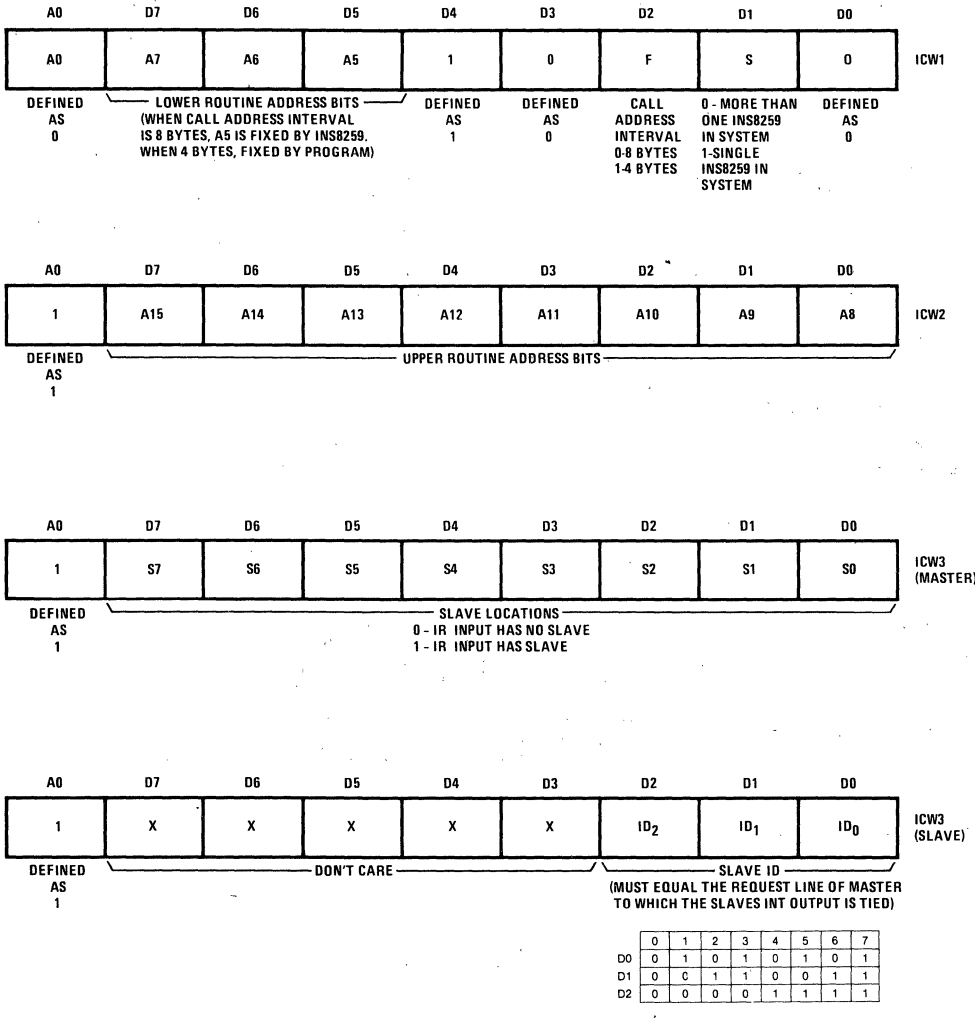


Figure 2. Initialization Command Word Format

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When an ICW1 is received, the following functions are performed in the INS8259.

- The edge sense circuit is reset, which prepares it to detect a positive transition at an IR input.
- The Interrupt Mask Register (IMR) is cleared.
- The IR7 input is assigned lowest priority (i.e., priority level 7).
- The special mask mode and status read flip-flops are reset. ICW1 also contains three types of programming information.
  - — Single INS8259 or Master with Slave(s) configuration, as set by D1 of ICW1.
  - — Four- or eight-byte CALL address interval, as set by D2 of ICW1.
  - — If the four-byte CALL interval is used, bits A5-A7 of the CALL address are specified by D5-D7 of ICW1 and bits A0-A4 are provided by the INS8259. If the eight-byte interval is used, bits A6 and A7 are specified by bits D6 and D7 of ICW1, while bits A0-A5 are provided by the INS8259. Refer to table 1.

The contents of ICW2 specify bits A8-A15 of the CALL address.

ICW3 is used only if a master/slave configuration is being initialized. The ICW3 issued to the master INS8259 identifies which IR inputs have slaves attached. Each bit position corresponds to a separate IR input (D0 = IR0 and D7 = IR7). For each IR input that has a slave attached, the corresponding ICW3 bit is set to 1. Those IR positions without a slave are identified by 0s in the corresponding ICW3 bit positions. The ICW3 is also used to assign three-bit identifiers to the slave INS8259s. A separate ICW3 is sent to each slave with a unique ID contained in bits D0-D2. The ID must correspond to which master IR line the slave's INT is connected to. Later, when a slave's interrupt request is selected for servicing, the master INS8259 automatically issues byte 1 of the CALL sequence and sets the ID assigned to that slave on the CAS2-CAS0 lines. This enables the specified slave to release bytes 2 and 3 of the CALL sequence.

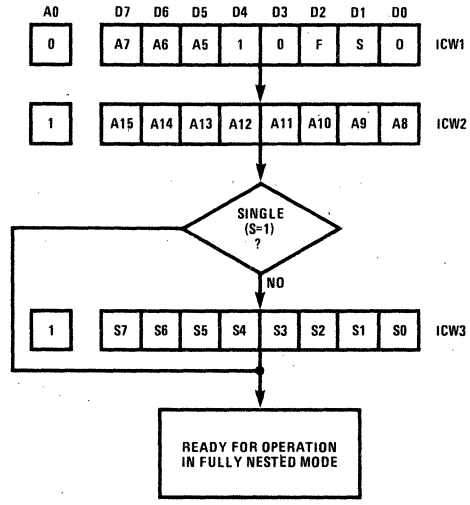


Figure 3. Initialization Sequence

Table 1.

	Interval = 4								Interval = 8							
	Lower Memory Routine Address															
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
IR7	A7	A6	A5	1	1	1	0	0	A7	A6	1	1	1	0	0	0
IR6	A7	A6	A5	1	1	0	0	0	A7	A6	1	1	0	0	0	0
IR5	A7	A6	A5	1	0	1	0	0	A7	A6	1	0	1	0	0	0
IR4	A7	A6	A5	1	0	0	0	0	A7	A6	1	0	0	0	0	0
IR3	A7	A6	A5	0	1	1	0	0	A7	A6	0	1	1	0	0	0
IR2	A7	A6	A5	0	1	0	0	0	A7	A6	0	1	0	0	0	0
IR1	A7	A6	A5	0	0	1	0	0	A7	A6	0	0	1	0	0	0
IR0	A7	A6	A5	0	0	0	0	0	A7	A6	0	0	0	0	0	0

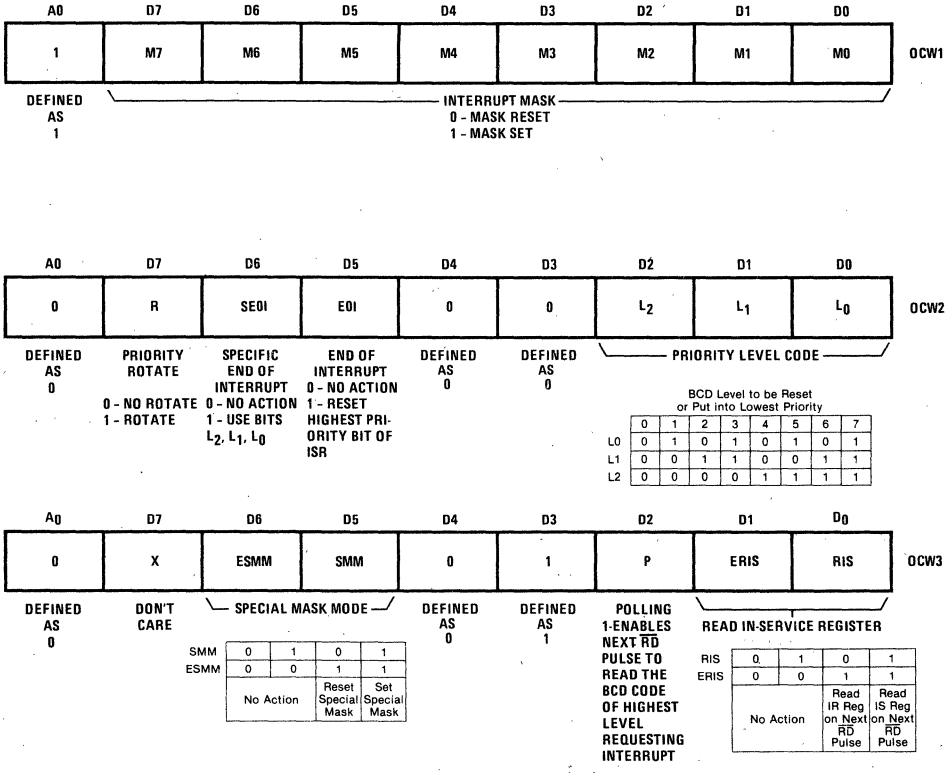


Figure 4. Operation Command Word Format

D.3

OPERATION COMMAND WORDS (OCWs)

Figure 4 summarizes the bit functions for OCW1, OCW2 and OCW3. These command words can be issued to the INS8259 at any time after initialization to alter the device's operating mode or to read specified registers.

FULLY NESTED MODE

Immediately following the ICW sequence, the INS8259 is ready to operate in the fully nested mode, with the highest priority assigned to IR0 and the lowest priority to IR7. In this mode, processing of lower priority interrupts is nested within higher priority interrupts. That is, a new interrupt will be sent to the microprocessor whenever an interrupt request is received, if no higher priority interrupt is in service. If any lower priority interrupt is in service at this time, execution of its routine is suspended until all higher level interrupts are serviced. When the microprocessor acknowledges the new interrupt, its CALL address is released. No interrupt will be issued for an interrupt request so long as a higher level interrupt is in service.

As part of the completion of an interrupt service routine, the microprocessor must issue an End of Interrupt (EOI) command, which resets the highest level ISR bit. After an ISR bit resets, the ISR or IRR bit then having the highest priority is serviced. The EOI is issued by means of an OCW2, in which bit D5 = 1. To maintain the operating characteristics of the fully nested mode, bit D7 must equal 0.

ROTATING PRIORITY MODE

In the rotating priority mode, an interrupt level is automatically assigned lowest priority immediately after it is serviced. Highest priority then passes to the next lower interrupt level. For example, when servicing of interrupt level 3 is completed (ISR bit 3 is reset), interrupt level 3 is assigned lowest priority and interrupt level 4 assumes highest priority.

To operate in rotating priority mode, the EOI issued at the end of *each* service routine must have bit 7 and bit 5 set to 1.

The lowest priority can be program-assigned by means of an OCW2. The OCW2 used to make a specific priority assignment would need to be in the range (hex) C0-C7. For example, if the OCW2 value is C3, interrupt level 3 is assigned lowest priority and level 4 is given highest priority.

INTERRUPT MASKING AND SPECIAL MASKING

OCW1 can be used to mask off individual interrupt levels. This command is specified by A0 = 1. Each data bit in OCW1 controls a separate bit in the Interrupt Mask Register (IMR). When an IMR bit is set, the corresponding bit position is masked at the IRR and, when in special mask mode, at the ISR.

If an ISR bit is already set at the time it is masked, the lower priority interrupts will remain inhibited by the masked interrupt level. These lower priority levels can be enabled by an EOI command that resets that ISR bit or by issuing a special mask command.

The special mask command is issued by means of an OCW3, in which bit D5 = 1 and D6 = 1. This sets the special mask mode flip-flop, which enables all unmasked interrupt levels. These remain enabled until the special mask mode flip-flop is reset by an OCW3 with bit D5 = 0 and bit D6 = 1.

POLLED MODE

The polled mode is used when the program assumes full control of device servicing and does not allow processor interrupts.

In this mode, the microprocessor disables its interrupt input and, when it wishes to service a device attached to the INS8259, it issues an OCW3 with bit D2 = 1. This is followed by an $\overline{RD}$ pulse with A0 = 0. If any IRR bits are set when the $\overline{RD}$ pulse is received, the INS8259 sets the ISR bit corresponding to the highest priority level requesting service. It also identifies that priority level on the data bus in the following manner:

D7	D6	D5	D4	D3	D2	D1	D0
I	–	–	–	–	W2	W1	W0

W0-2 — BCD code of the highest priority level requesting service.

I — Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels — so that the $\overline{INTA}$ sequence is not needed (and this saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

END OF INTERRUPT (EOI) AND SPECIFIC END OF INTERRUPT (SEOI)

The EOI command is used in the fully nested mode to reset the appropriate ISR bit when that interrupt level's service routine is concluding. The non-specific EOI command always resets the highest level ISR bit that is currently set. For this reason, it is reliable only in a fixed priority scheme, such as the fully nested mode. When priority assignments are changed from the standard order (i.e., IR7 = lowest), the specific EOI command must be used. This command contains the BCD value of the interrupt level that is to be reset.

Both specific and non-specific EOI are issued by means of an OCW2. For the non-specific EOI version, bit D5 of the command is set to 1 and bit D6 is 0. For the specific EOI version, bit D5 of the command is set to 1 and bit D6 is set to 1. In the specific EOI command, the BCD value of the ISR bit to be reset is contained in command bits D0-D2.

READING INS8259 REGISTERS

Four types of status can be read from the INS8259: the contents of IRR, the contents of ISR, the contents of IMR and the BCD value of the interrupt level requesting service.

The microprocessor reads the contents of IRR by issuing an OCW3, in which bit D0 = 0 and bit D1 = 1. This is followed by a $\overline{RD}$ pulse, during which the INS8259 places the IRR status on the data bus with the IRR low order bit (0) present on D0 and the IRR high order bit (7) present on D7. The contents of ISR are read in the same manner, except that OCW3 bit D0 is set to 1 as well as bit D1. The contents of IMR can be read by setting A0 = 1 and issuing a $\overline{RD}$ pulse.

The BCD value of the interrupt level requesting service is placed on the data bus in response to a poll command. This technique was described earlier under Polled Mode.

CASCADE OPERATION

A typical cascading system is shown in figure 5.

Once a slave line is activated and later acknowledged, the INS8080 CALL code is released by the master during the first $\overline{INTA}$ pulse. The CAS lines will contain the slave address code from the trailing edge of this pulse until the trailing edge of the third $\overline{INTA}$ pulse. This allows the corresponding slave to release the two-byte service routine address during the second and third $\overline{INTA}$ pulses.

Because the CAS lines default to 000, no slave should be connected to IR0 on the master unless master request inputs IR1 through IR7 are connected to slaves.

Each INS8259 in the system must follow its own initialization sequence and can be programmed to operate in any mode. Two EOI commands must be issued: one for the master and one for the slave.

The EOI allows the respective request input to generate a new interrupt. To allow a slave to have nested interrupts, the master should be sent an EOI as soon as possible in the service routine.

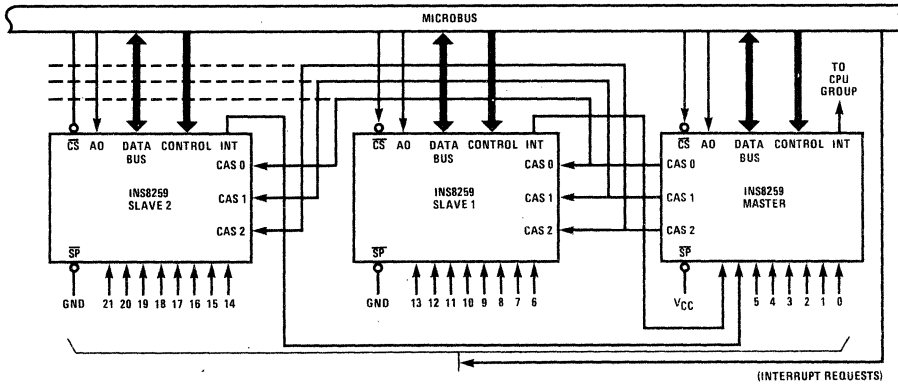


Figure 5. Cascade Operation

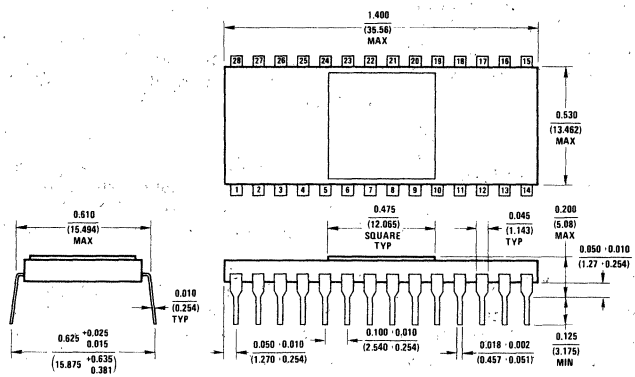
	Instruction	A0	D7	D6	D5	D4	D3	D2	D1	D0	Operation Description
1	ICW1 A	0	A7	A6	A5	1	0	1	1	0	Byte 1 initialization, format = 4, single.
2	ICW1 B	0	A7	A6	A5	1	0	1	0	0	Byte 1 initialization, format = 4, not single.
3	ICW1 C	0	A7	A6	A5	1	0	0	1	0	Byte 1 initialization, format = 8, single.
4	ICW1 D	0	A7	A6	A5	1	0	0	0	0	Byte 1 initialization, format = 8, not single.
5	ICW2	1	A15	A14	A13	A12	A11	A10	A9	A8	Byte 2 initialization (Address no. 2).
6	ICW3 M	1	S7	S6	S5	S4	S3	S2	S1	S0	Byte 3 initialization — master.
7	ICW3 S	1	0	0	0	0	0	S2	S1	S0	Byte 3 initialization — slave.
8	OCW1	1	M7	M6	M5	M4	M3	M2	M1	M0	Load mask reg, read mask reg.
9	OCW2 E	0	0	0	1	0	0	0	0	0	Non-specific EOI.
10	OCW2 SE	0	0	1	1	0	0	L2	L1	L0	Specific EOI, L2, L1, L0 code of ISFF to be reset.
11	OCW2 RE	0	1	0	1	0	0	0	0	0	Rotate at EOI (Auto Mode).
12	OCW2 RSE	0	1	1	1	0	0	L2	L1	L0	Rotate at EOI (Specific Mode), L2, L1, L0, code of line to be reset and selected as bottom priority.
13	OCW2 RS	0	1	1	0	0	0	L2	L1	L0	L2, L1, L0 code of bottom priority line.
14	OCW3 P	0	—	0	0	0	1	1	0	0	Poll mode.
15	OCW3 RIS	0	—	0	0	0	1	0	1	1	Read IS register.
16	OCW3 RR	0	—	0	0	0	1	0	1	0	Read requests register.
17	OCW3 SM	0	—	1	1	0	1	0	0	0	Set special mask mode.
18	OCW3 RSM	0	—	1	0	0	1	0	0	0	Reset special mask mode.

Notes:
1. In the master mode $\overline{SP}$ pin = 1; in slave mode $\overline{SP}$ = 0.
2. (—) = don't care.

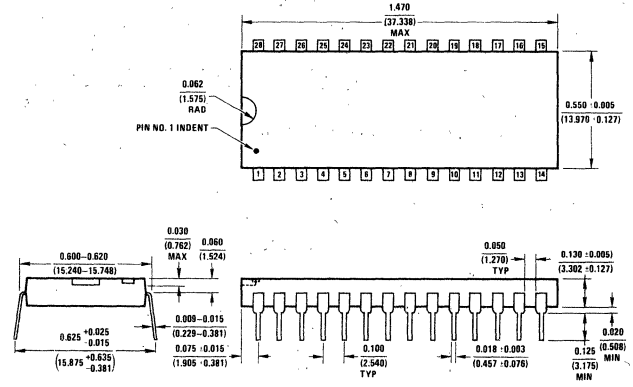
Figure 6. INS8259 Instruction Set

Physical Dimensions

inches (millimeters)



28-Lead Ceramic Dual-In-Line Package (D)
Order Number INS8259D
NS Package Number D28A



28-Lead Plastic Dual-In-Line Package (N)
Order Number INS8259N
NS Package Number N28A

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National Semiconductor

MARCH 1978

INS8298/INS8298E 8080A LLL BASIC Interpreter

General Description

The INS8298/INS8298E is a 65k MAXI-ROM™*, organized into 8192 8-bit words, that is preprogrammed with the 8080A Lawrence Livermore Laboratory (LLL) BASIC Interpreter. Unprogrammed versions of the INS8298 and INS8298E are the MM5235 (28 pin, 800 ns access) and INS8364E/MM52164 (24 pin, 450 ns access), respectively. Both the INS8298 and INS8298E provide complete TTL compatibility and single 5V power supply. Three chip selects controlling TRI-STATE™ outputs allow for memory expansion.

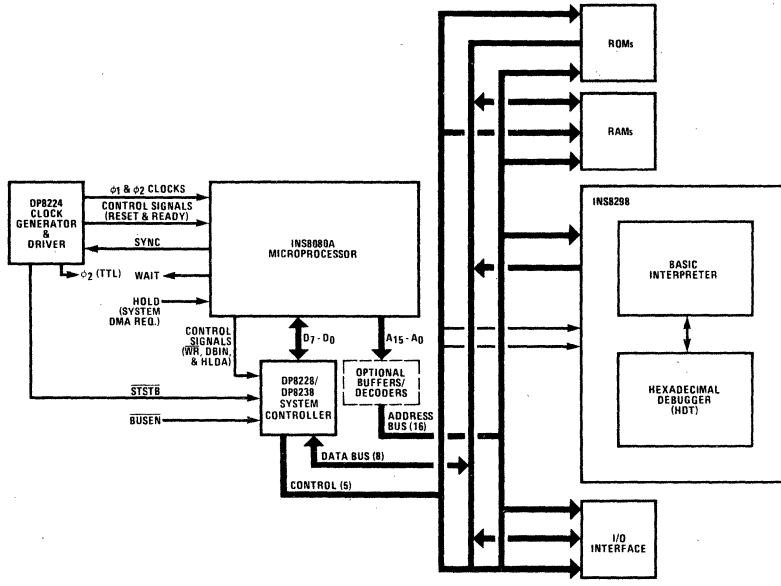
The 8080A LLL BASIC Interpreter operates with the INS8080A microprocessor system to provide a high-level, easy-to-use language for performing both control and computation functions in the INS8080A. Designed for use in data acquisition and control applications, the LLL BASIC Interpreter enables the user to write and debug a program on-line. The interpreter executes source code statements directly, thus avoiding the need to translate into machine language. This approach has the advantage of easier source code manipulation (because the source is always available), and instant revision of the program when errors are detected.

Features

- Reduces software effort in microcomputer applications
- Provides easy source code manipulation and instant program revision
- Allows immediate-mode execution of program statements to assist program checkout
- Includes floating-point arithmetic package to provide full computational capability
- Readily adaptable to user-supplied I/O routines
- Allows calls to high-speed, machine-language subroutines
- Allows use of indestructible hexadecimal debugging package
- Available as INS8298 (28 pin, 800 ns access) and INS8298E (24 pin, 450 ns access)
- MICROBUS™* compatible

*A trademark of National Semiconductor Corporation.

General System Configuration



D.3

The LLL BASIC Interpreter is used to translate, debug, and execute user-written ASCII programs in read/write memory (RAM). Each statement is interpreted from its ASCII BASIC format, and then executed line-by-line. An LLL BASIC Compiler, written in FORTRAN, will soon be available in the public domain.* (See figure 1.)

The BASIC Interpreter accepts both program statements and control commands. Program statements describe (to the BASIC Interpreter) operations to be performed on program data. A program statement preceded by a line number is inserted into the program for later execution at a spot determined by the line number. If no line number precedes the statement, it is executed immediately and then discarded. This latter mode, known as "immediate" or "direct," is especially valuable during program checkout. Control commands specify actions that alter the status of the user's program; for example, they direct the execution, saving, and retrieval of programs. Program statements are summarized in table 1; control commands are summarized in table 2.

The BASIC Interpreter is located in ROM from 1000_{16} through $2FFF_{16}$. BASIC assumes that its RAM starts at location $3D00_{16}$. The memory map is shown in table 3. All I/O routines used by the INS8298 are located in the upper 256 bytes of the address space so that a simple address decoding circuit can allow the substitution of a special user-supplied I/O package, if necessary. As an alternative scheme for allowing the user to tailor I/O to his own needs, entry points to the interpreter are provided that allow the page zero initialization program to channel all BASIC I/O through its own routines.

A hexadecimal debugging routine (HDT) is also available on the INS8298 ROM. HDT allows the user to examine internal registers and memory locations and modify their contents. HDT is called from the BASIC Interpreter to help debug user-developed software. Input and output data representation is in hexadecimal format. In addition to the usual debugging capabilities, HDT also has commands to perform the following functions:

- Test a specified range of memory locations
- Load programs in hexadecimal, NSC, and LLL binary formats
- Save the contents of a specified range of memory locations

In addition to the features summarized previously, LLL BASIC has many capabilities found in other standard BASIC systems (see tables 1 and 2). However, LLL BASIC does not include built-in operations as intrinsic functions, e.g., trigonometric or string-manipulation functions. Also, LLL BASIC does not permit arbitrary arithmetic expressions beyond those of the form:

variable op variable

where the first variable in the expression may be preceded by a minus (–); op may be a plus (+), minus (–), asterisk (*) for multiplication, or slash (/) for division; and either variable can be an identifier, function, or number.

*For additional information, contact:

Argonne Code Center
Argonne National Laboratory
9700 South Cass Avenue
Argonne, Illinois 60439

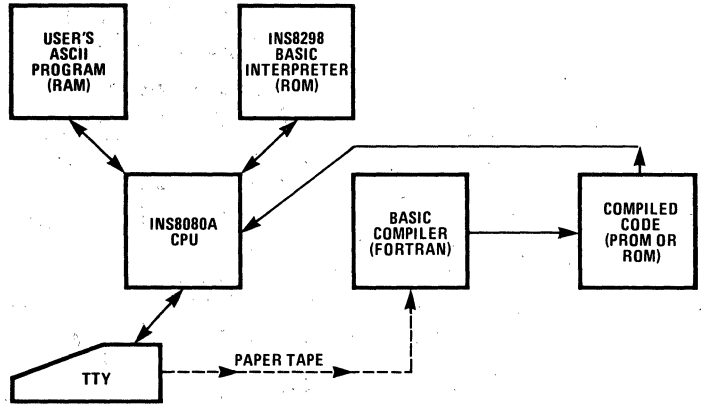


Figure 1. Operation of the LLL BASIC Interpreter and Compiler with the INS8080A

Table 1. BASIC Statements

Statement	Function
CALL	Calls user-written assembly-language routines.
DIM	Declares a one-dimensional array. (Indexing is from zero.)
END	Terminates a program and returns control to BASIC.
FOR	Causes program to iterate through a loop a designated number of times.
GET expression	Reads input data from a specified port.
GOSUB nn	Transfers control to a subroutine beginning at line nn.
GOTO nn	Transfers control to line nn.
IF expression THEN nn	Transfers to line nn if the condition of the expression is met.
INPUT list	Allows the user to supply numeric data to a program directly from the terminal.
LET identifier = expression	Assigns the value of an expression to the identifier on the left side of the equal sign.
NEXT	Signals the end of a loop.
PRINT	Allows numeric data and character strings to be printed on the terminal.
PUT expression	Writes output data to a specified port.
REM	Allows comments to be inserted in the program listing.
RETURN	Returns control to the line after the last GOSUB.
STOP	Suspends program execution and returns.

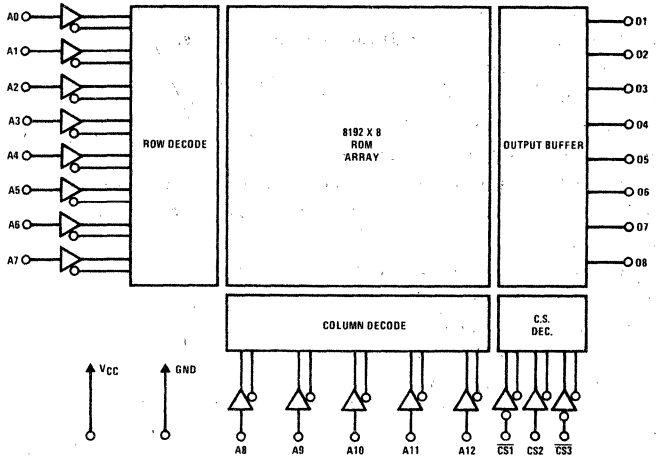
Table 2. BASIC Commands

Command	Function
CONTROL/H (backspace)	Deletes the previous character typed during input.
CONTROL/S	Interrupts program during execution and returns to immediate mode.
DEBUG	Transfers control to the Hexadecimal Debugger program (HDT).
LIST	Prints out all or part of a program at the terminal.
PACK	Frees memory locations in RAM to allow the user more working space.
PLIST	Punches paper-tape copy of a program.
PTAPE	Reads in paper-tape copy of program using high-speed reader.
RUN	Begins execution of the program currently in memory.
SCR	Erases the program in memory

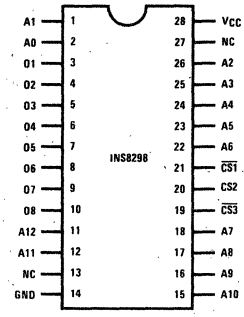
Table 3. Memory Map for BASIC Interpreter

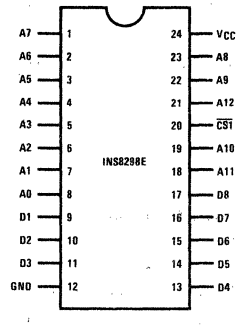
ROM Address (hex)	Function
1000 - 1008	BASIC entry points for initialization.
1009 - 27FF	BASIC Interpreter.
2800 - 2EFF	Hexadecimal Debugger (HDT) and loaders.
2F00 - 2FFF	System I/O routines for INS8251 USART (ports EC and ED).
RAM Address (hex)	**Function**
3D00 - 3DFF	BASIC RAM scratch area (buffers, variables, etc.).
3E00 upward	BASIC user program space.
Top of RAM downward	BASIC stack area.
Chip Selects	
$\overline{CS1}$	Active low (0).
CS2	Active high (1).
$\overline{CS3}$	Active low (0).

Block and Connection Diagrams



NOTE: CS2 AND $\overline{CS3}$ NOT AVAILABLE IN INS8298E.





Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.5V to +6.5V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1 W
Lead Temperature (Soldering, 10 seconds)	+300°C

Chip Selects

CS No.	Pin No.	Active Level
INS8298		
1	21	0
2	20	1
3	19	0
INS8298E		
1	20	0

DC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = +5V ± 5%, unless otherwise specified.) See AC test circuit and switching time waveforms.

Parameter (Note 3)		Conditions	Min.	Typ. (Note 4)	Max.	Units
I_{LI}	Input Current	V_{IN} = 0V to V_{CC}			10	μA
V_{IH}	Logical "1" Input Voltage		2.2		V_{CC}+1.0	V
V_{IL}	Logical "0" Input Voltage		−0.5		0.6	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −200 μA	2.4			V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 3.2 mA			0.4	V
I_{LOH}	Output Leakage Current	V_{OUT} = 4 V, Chip Deselected			10	μA
I_{LOL}	Output Leakage Current	V_{OUT} = 0.45 V, Chip Deselected			−20	μA
I_{CC1}	Power Supply Current	All Inputs = 5.25 V, Data Output Open		100	130	mA

Capacitance

Parameter (Note 3)		Conditions	Min.	Typ. (Note 4)	Max.	Units
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			15.0	pF

AC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = +5V ± 5%, unless otherwise specified.) See AC test circuit and switching time waveforms.

Parameter (Note 3)		Conditions	Limits						Units
			INS8298			INS8298E			
			Min.	Typ. (Note 4)	Max.	Min.	Typ. (Note 4)	Max.	
t_A	Address Access Time	See AC Load Circuit. All times except t_{OFF} measured to 1.5V level with t_r and t_f of input < 20 ns (figures 2 & 3), t_{OFF} TRI-STATE output level measured to less than ±20 μA output current.		450	800			450	ns
t_{AC}	Chip Select Access Time			150	250			150	ns
t_{OFF}	Output Turn OFF Delay			150	250			150	ns
t_C	Cycle Time		800	450					ns
t_{AS}	Address Set-Up Time Referenced to Chip Select		550						ns

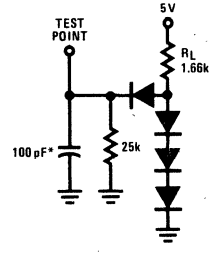
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used: logical "1" = most positive voltage level, logical "0" = most negative voltage level.

Note 4: Typical values are for T_A = 25°C and nominal supply voltage.

AC Test Circuit and Switching Time Waveforms



*INCLUDES JIG CAPACITANCE.

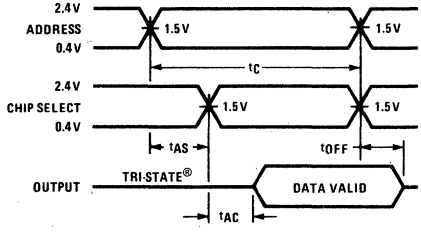


Figure 2. Address Precedes Chip Select

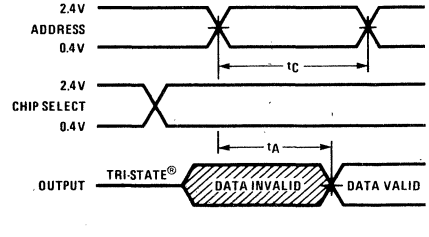


Figure 3. Address Follows Chip Select

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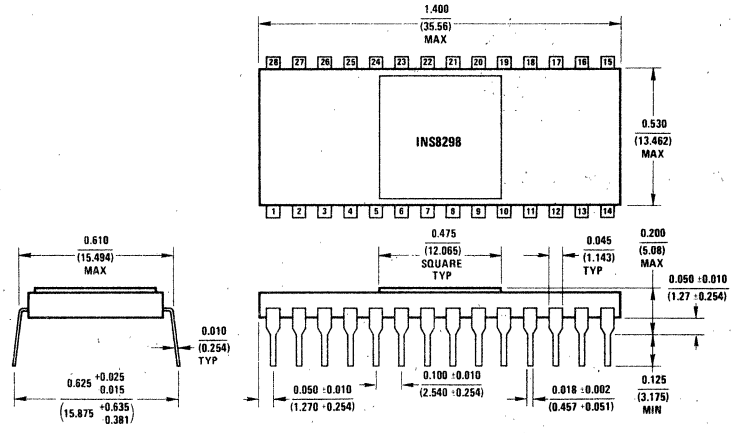
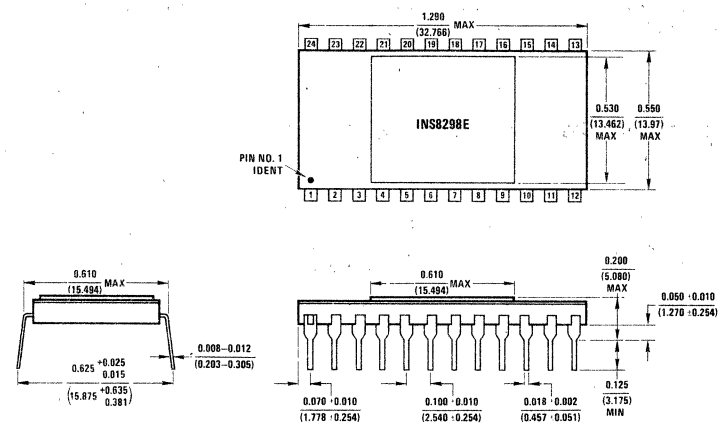
Physical Dimensions inches (millimeters)



28-Lead Cavity Dual-In-Line Package (D)
Order Number INS8298D
NS Package Number D28A



24-Lead Cavity Dual-In-Line Package (D)
Order Number INS8298ED
NS Package Number D24A

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National Semiconductor

MARCH 1977
Pub. No. 426305451-001A

INS1671 Asynchronous/Synchronous Transmitter/Receiver

General Description

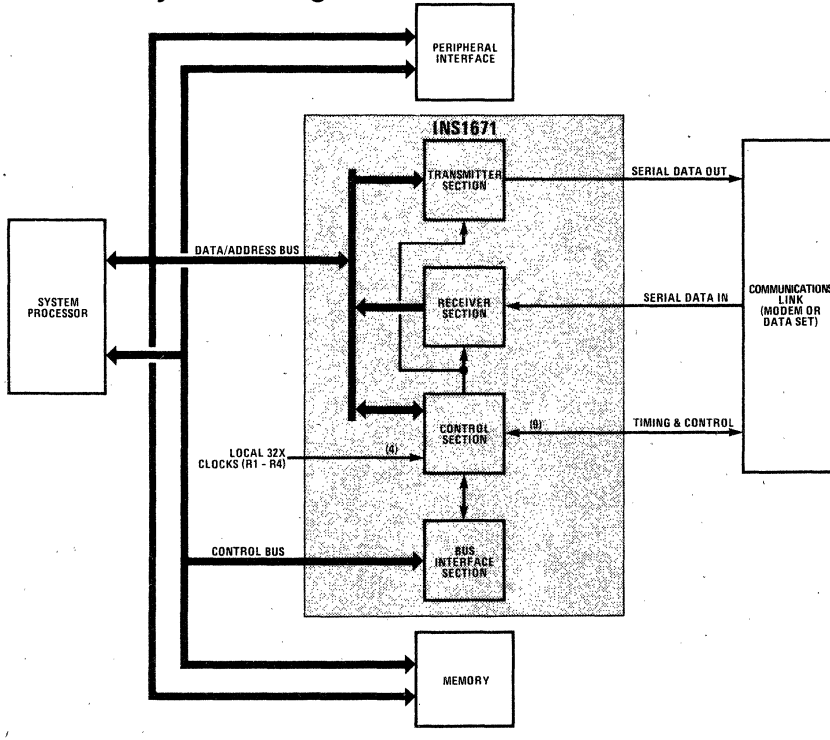
The INS1671 is a programmable Asynchronous/Synchronous Transmitter/Receiver (ASTRO) chip housed in a standard, 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate MOS technology, provides a serial data input/output interface in a bus-structured system. The chip is capable of full duplex operation with synchronous or asynchronous data communications systems.

The INS1671 is designed to operate on a multiplexed, bidirectional bus with other bus-oriented devices. The functional configuration of the INS1671 is programmed by the system software via the bus and all parallel data transfers within the system are accomplished over the bus lines. In addition, the INS1671 contains a provision for hardwiring a unique 5-bit identification code to a chip, thereby allowing up to 32 INS1671 devices to be addressed via the multiplexed bus.

Features

- Synchronous and Asynchronous Full Duplex Operations
- Synchronous Mode Capabilities
  - Selectable 5- to 8-Bit Characters
  - Two Contiguous SYN Characters Provide Synchronization
  - Programmable SYN and DLE Characters Stripping
  - Programmable SYN and SYN-DLE Characters Insertion
- Asynchronous Mode Capabilities
  - Selectable 5- to 8-Bit Characters
  - Line Break Detection
  - 1-, 1½-, or 2-Stop Bit Detection
  - False Start Bit Detection
  - Automatic Serial Echo Mode
- DC to 1M Baud Rate
- 8 Selectable Clock Rates (4 Programmable)
- Transmission Error Detection Capabilities
  - Parity
  - Overrun
  - Framing
- Double Buffering of Data
- 8-Bit Bidirectional Bus for Data, Status, and Control Words
- All Inputs and Outputs TTL Compatible
- On-Line Diagnostic Mode
- Reduces System Component Count
- Direct Plug-In Replacement for Western Digital FD1671

INS1671 General System Configuration



Absolute Maximum Ratings

V_{DD} with Respect to V_{BB} (Ground) . . . . . +20 V to −0.3 V
Maximum Voltage to Any Input with Respect to V_{BB} . . . +20 V to −0.3 V
Operating Temperature. . . . . 0°C to +70°C
Storage Temperature . . . . . −55°C to +125°C
Power Dissipation . . . . . 1000 mW

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = +12.0 V ± 0.6 V, V_{BB} = −5.0 V ± 0.25 V, V_{SS} = 0 V, V_{CC} = +5 V ± 0.25 V

Symbol	Parameter	Unit	Min	Typ	Max	Conditions
I_{LI}	Input Leakage	μA			10	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage	μA			10	$V_{OUT} = V_{DD}$
I_{BB}	V_{BB} Supply Current	mA			1	V_{BB} = −5 V
I_{CCAVE}	V_{CC} Supply Current	mA			80	
I_{DDAVE}	V_{DD} Supply Current	mA			10	
V_{IH}	Input High Voltage	V	2.4			
V_{IL}	Input Low Voltage (All Inputs)	V			0.8	
V_{OH}	Output High Voltage	V	2.8			I_O = −100 μA
V_{OL}	Output Low Voltage	V			0.4	I_O = 1.6 mA

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = +12.0 V ± 0.6 V, V_{BB} = −5.0 V ± 0.25 V, V_{CC} = +5.0 V ± 0.25 V, V_{SS} = 0 V, C_{LMAX} = 20 pF

Symbol	Parameter	Unit	Min	Typ	Max	Conditions
t_{AS}	Address Setup Time	ns	0			
t_{AH}	Address Hold Time	ns	150			
t_{ARL}	Address to $\overline{RPLY}$ Delay	ns			400	
t_{CS}	$\overline{CS}$ Width	ns	250			
t_{CSRLF}	$\overline{CS}$ to Reply Off Delay	ns	0		250	R_L = 2.7 kΩ
READ CYCLE						
t_{ARE}	Address to $\overline{RE}$ Spacing	ns	250			
t_{RECSH}	$\overline{RE}$ and $\overline{CS}$ Overlap	ns	20			
t_{RECS}	$\overline{RE}$ to $\overline{CS}$ Spacing	ns	250			
t_{RED}	$\overline{RE}$ to Data Out Delay	ns			180	C_L = 20 pF
t_{RE}	$\overline{RE}$ Width	ns	200		1000	
WRITE CYCLE						
t_{AWE}	Address to $\overline{WE}$ Spacing	ns	250			
t_{WECSH}	$\overline{WE}$ and $\overline{CS}$ Overlap	ns	20			
t_{WE}	$\overline{WE}$ Width	ns	200		1000	
t_{DS}	Data Setup Time	ns	150			
t_{DH}	Data Hold Time	ns	100			
t_{WECS}	$\overline{WE}$ to $\overline{CS}$ Spacing	ns	250			

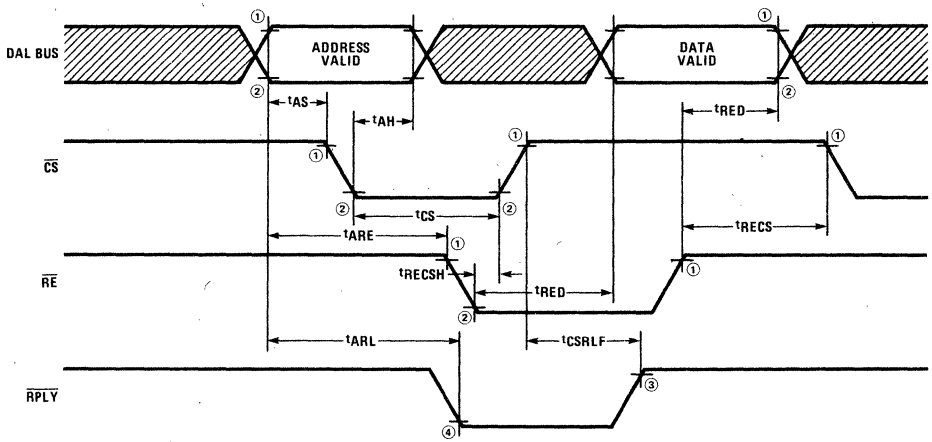
Interrupt

Symbol	Parameter	Unit	Min	Typ	Max	Conditions
t_{CSI}	$\overline{CS}$ to $\overline{IACKI}$ Delay	ns	0			
t_{CSRE}	$\overline{CS}$ to $\overline{RE}$ Delay	ns	250			
t_{CSREH}	$\overline{CS}$ and $\overline{RE}$ Overlap	ns	20			
t_{RECS}	$\overline{RE}$ to $\overline{CS}$ Spacing	ns	250			
t_{PI}	$\overline{IACKI}$ Pulse Width	ns	200			
t_{IAD}	$\overline{IACKI}$ to Valid ID Code Delay	ns			250	(Note 1)
t_{RED}	$\overline{RE}$ Off to $\overline{DAL}$ Open Delay	ns			180	
t_{IARL}	$\overline{IACKI}$ to $\overline{RPLY}$ Delay	ns			250	
t_{CSRLF}	$\overline{CS}$ to $\overline{RPLY}$ Off Delay	ns	0		250	$R_L = 2.7\,k\Omega$
t_{IAIH}	$\overline{IACKI}$ On to $\overline{INTR}$ Off Delay	ns			300	
t_{II}	$\overline{IACKI}$ to $\overline{IACKO}$ Delay	ns			200	
t_{REI}	$\overline{RE}$ Off to $\overline{IACKO}$ Off Delay	ns			250	

Note 1: If $\overline{RE}$ goes low after $\overline{IACKI}$ goes low, the delay will be from the falling edge of $\overline{RE}$.

Timing Waveforms

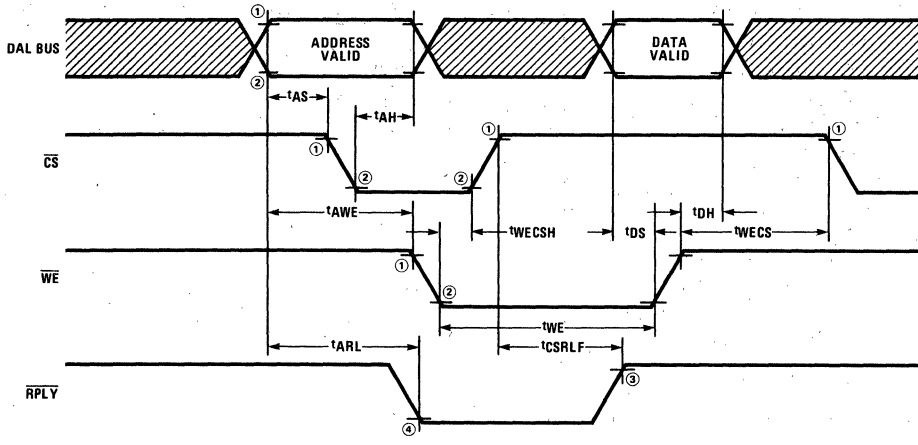
① = V_{IH} (MIN) = 2.4 V
② = V_{IL} (MAX) = 0.8 V
③ = V_{OH} (MIN) = 2.8 V
④ = V_{OL} (MAX) = 0.4 V



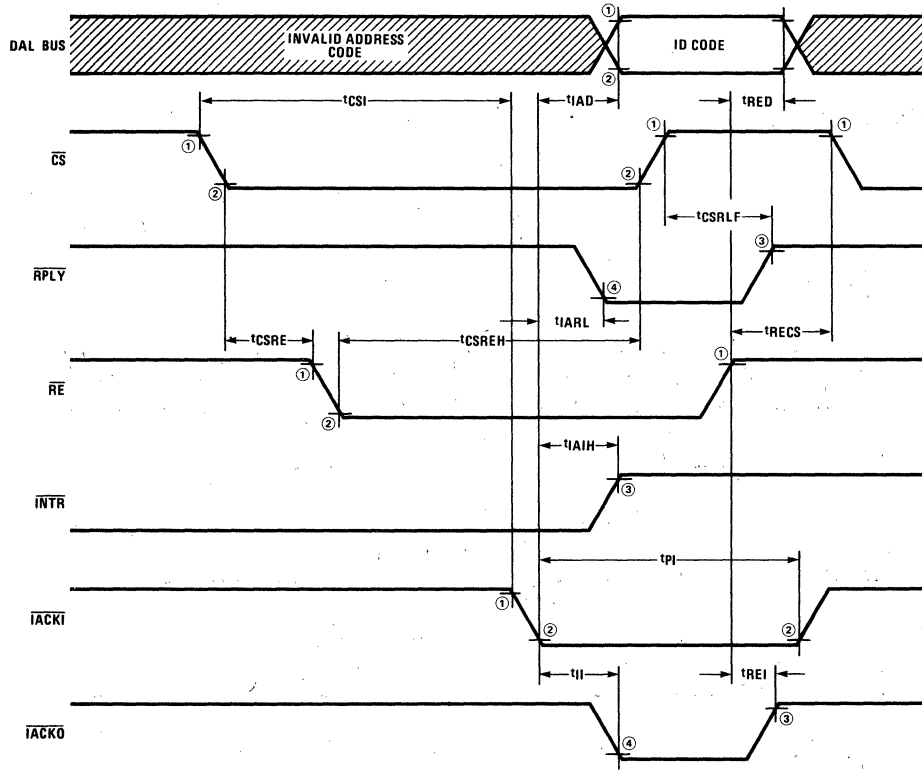
READ TIMING (Note 1)

D.4

Timing Waveforms (cont.)



WRITE TIMING (Notes 1 & 2)

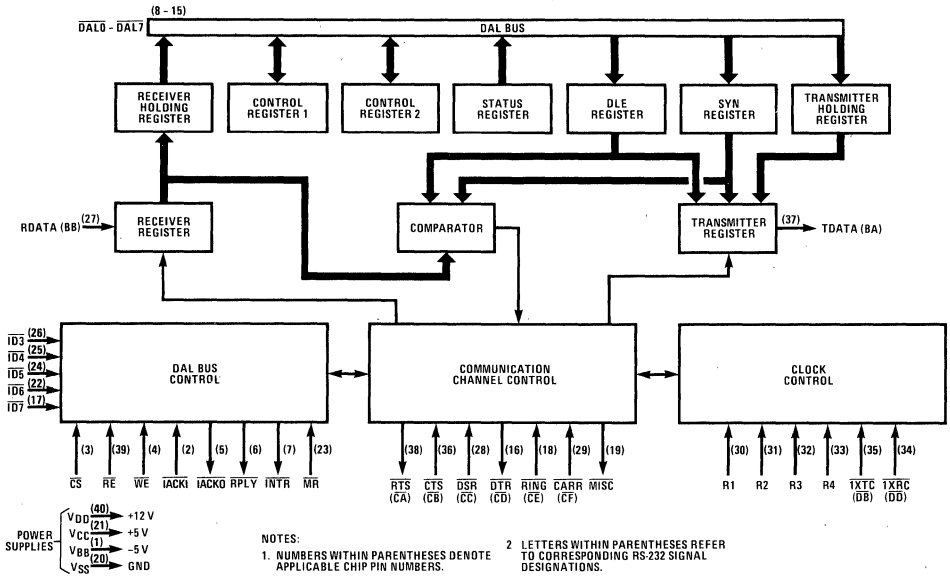


INTERRUPT TIMING (Note 3)

NOTES:

1. ID DECODE is the major factor in t_{ARE}, t_{AWE}, and t_{ARL} timing.
2. If changing Control Register 1 while processing data, the $\overline{WE}$ pulse width must be contained within the Data Valid envelope to insure correct data processing.
3. DALO must be a logic high coincident with an active $\overline{CS}$ to form an invalid address during Daisy Chain Interrupt Response.

INS1671 Functional Block Diagram



INS1671 Functional Pin Definitions

The following describes the function of all INS1671 input/output pins. Some of these descriptions reference internal circuits.

NOTE

In the following descriptions, a low represents a logic 0 and a high represents a logic 1 (refer to dc characteristics).

INPUT SIGNALS

Chip Select ($\overline{CS}$): When low, the chip is selected by a valid address on the DAL Bus. This enables communication between the INS1671 and the CPU (or controller).

Select Code ($\overline{ID7}$ - $\overline{ID3}$): Five input pins that are used for hardwiring a unique 5-bit identification code to the chip. The unique code is used to select the chip when addressing up to 32 INS1671 devices and to identify the chip when responding to interrupts.

Read Enable ($\overline{RE}$): When low coincident with an active $\overline{CS}$ input, allows the CPU (or controller) to read either of the following: data, control words, and status information from associated registers of the chip; or interrupt identification information. A Read operation is initiated by the controller when it places an 8-bit address on the Data Access Lines (DAL) Bus coincident with a low-level $\overline{CS}$ input. When bits 3 through 7 of the 8-bit address input match the unique 5-bit identification code of the chip, the device is selected. Bits 0 through 2 of the 8-bit address input are then used to select INS1671 registers to read from as indicated below.

A_2	A_2	A_0	Selected Register
0	0	0	Control Register 1
0	1	0	Control Register 2
1	0	0	Status Register
1	1	0	Receiver Holding Register

When the $\overline{RE}$ input is made active (low) by the controller, the INS1671 gates the contents of the addressed register onto the DAL Bus. When the $\overline{RE}$ and $\overline{CS}$ inputs are both returned to a high level, the Read operation is terminated and the chip is deselected.

Write Enable ($\overline{WE}$): When low coincident with an active $\overline{CS}$ input, allows the CPU (or controller) to write data or control words into associated registers of the chip. A Write operation is initiated by the controller as described above for a Read operation. However, bits 0 through 2 of the 8-bit address input are used to select INS1671 registers to be written into as indicated below.

A_2	A_1	A_0	Selected Register
0	0	0	Control Register 1
0	1	0	Control Register 2
1	0	0	SYN Register
1	0	0	DLE Register
1	1	0	Transmitter Holding Register

When the $\overline{WE}$ input is made active (low) by the controller, the INS1671 gates the data from the DAL Bus into the addressed register. As indicated in the above table, the same address (100) is used to write data into both the SYN and DLE registers. The INS1671 is set up so that data is written into the SYN Register and then into the DLE Register by a succeeding $\overline{WE}$ input with address 100. Any intervening Write or Read operation with a different register address causes the next address 100 input to select the SYN Register. When the $\overline{WE}$ and $\overline{CS}$ inputs are both returned to a high level, the Write operation is terminated and the chip is deselected.

Master Reset ($\overline{MR}$): When low, clears the Control Register, Status Register, and other controls of the chip.

D.4

Interrupt Acknowledge In (IACKI): Forced low by the CPU (or controller) when it is polling to determine which device is requesting an interrupt. When the device requesting the interrupt receives a low-level IACKI input coincident with a low-level RE input, the chip places its unique 5-bit identification code (ID7 - ID3) on the DAL7 through DAL3 lines, respectively, and a high (Receiver interrupt) or low (Transmitter interrupt) on the DAL2 line of the DAL Bus. Also, at this time, the requesting device provides a low-level Reply (RPLY) output and all other INS1671 devices receiving a low-level IACKI input force their Interrupt Acknowledge Output (IACKO) signal to a low level. When the RE input returns to a high level, the interrupt identification information is removed from the DAL Bus.

Clock Rates (R1 - R4): Four input pins that accept four different local 32X baud rate clocks for the Transmitter and Receiver sections of the chip. The clock input at the R4 pin may be divided down into a 32X clock from either a 32X, 64X, 128X, or 256X clock input. The 32X clock is only used in the Asynchronous mode. Internal Control Register 2 selects the use of the local clocks.

Received Data (RDATA): Serial data input from the communications link (MODEM or data set).

Clear to Send (CTS): When low, enables the Transmitter section of the chip to transmit serial data to a MODEM or data set.

Data Set Ready (DSR): If low (On) or high (Off) when the internal Data Terminal Ready signal (bit 0 of Control Register 1) is high (On), generates an interrupt. The Data Set Ready input appears as bit 6 in the internal Status Register.

Ring Indicator (RING): If low (On) when the internal Data Terminal Ready signal (bit 0 of Control Register 1) is low (Off), generates an interrupt.

Carrier Detector (CARR): If low (On) or high (Off) when the internal Data Terminal Ready signal (bit 0 of Control Register 1) is high (On), generates an interrupt. The Carrier Detector input appears as bit 5 in the internal Status Register.

Transmitter Timing (1XTC): This input is the 1X baud rate clock for the Transmitter section of the chip. The 1X clock is primarily used in the Synchronous mode. Internal Control Register 2 selects the use of the 1X clock. Transmitter data is clocked out of the INS1671 on the falling edge of this clock input.

Receiver Timing (1XRC): This input is the 1X baud rate clock for the Receiver section of the chip. The 1X clock is primarily used in the Synchronous mode. Internal Control Register 2 selects the use of the 1X clock. Receiver data is clocked into the INS1671 on the rising edge of this clock input.

V_{BB}: -5-volt supply.

V_{CC}: +5-volt supply.

V_{DD}: +12-volt supply.

V_{SS}: Ground (0-volt) reference.

OUTPUT SIGNALS

Interrupt (INTR): Open-drain output that goes low when any one of the communication interrupt conditions indicated below occurs.

1. Data Received (Receiver Holding Register Full)
2. Transmitter Holding Register Empty
3. Carrier Detector On (CARR input low)
4. Carrier Detector Off (CARR input high)
5. Data Set Ready On (DSR input low)
6. Data Set Ready Off (DSR input high)
7. Ring Indicator On (RING input low)

Interrupt Acknowledge Out (IACKO): Goes low in response to a low-level IACKI input, when the chip is not the interrupting device. (The IACKO output is mutually exclusive with the RPLY output.)

Reply (RPLY): Open-drain output that goes low when the chip is selected by a valid address on the DAL Bus or when the chip identifies itself as the interrupting device during interrupt polling.

Transmitted Data (TDATA): Composite serial data output to a MODEM or data set. This output is held in the Marking state (logic 1) when the Transmitter section of the chip is disabled.

Data Terminal Ready (DTR): Set low when the CPU (or controller) is ready to communicate with a MODEM or data set. This output is generated by bit 0 of Control Register 1.

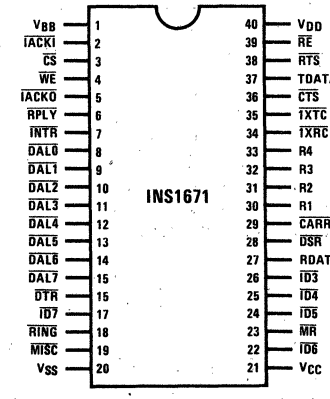
Request to Send (RTS): Set low when the CPU (or controller) is ready to transmit data to a MODEM or data set. This output is enabled by bit 1 of Control Register 1.

Miscellaneous (MISC): User-designated, programmable low-level output. This output is controlled by bit 4 of Control Register 1.

INPUT/OUTPUT SIGNALS

Data Access Lines (DAL) Bus: This bus comprises eight input/output lines (DAL0 - DAL7). The bus provides bidirectional communications between the CPU (or controller) and the INS1671. Data, control words, status information and address information are transferred via the DAL Bus.

Pin Configuration



INS1671 Programming

The system software determines the operative conditions (mode selection, clock selection, interface signal control, data format, *et cetera*) of the INS1671 via internal Control Registers 1 and 2. Each of these 8-bit registers can be loaded from the DAL Bus by a Write Operation or read into the DAL Bus by a Read Operation. The contents of Control Register 1 can be changed at any time, while the contents of Control Register 2 (usually loaded first) should be changed only when the Receiver and Transmitter sections of the chip are both in the idle mode. The contents of the two control registers are shown in figures 1 and 2 and are described below.

CONTROL REGISTER 1 (CR1) CONTENTS

Bit 0: Controls the generation of the Data Terminal Ready ($\overline{DTR}$) output. When high (logic 1), enables the Carrier Detector and Data Set Ready interrupts. When low (logic 0), enables only the Ring Indicator On interrupt.

Bit 1: Controls the enabling of the Request to Send ($\overline{RTS}$) output. When high in coincidence with a low-level Clear to Send ($\overline{CTS}$) input, enables the Transmitter section of the chip and allows the generation of Transmitter Holding Register Empty (THRE) interrupts. When low, disables the Transmitter section and disables the Request to Send ($\overline{RTS}$) output. Before the Transmitter section is disabled, any character in the Transmitter Register is completely transferred to the MODEM or data set.

Bit 2: When high, enables the INS1671 to perform the following: (1) transfer a new character into the Receiver Holding Register; (2) update Receiver status bits 1 through 4; and (3) generate Data Received interrupts. When low, disables the Receiver section and clears Receiver status bits 1 through 4.

Bit 3: When high while in the Asynchronous mode, enables a parity check on each received character and the generation of a parity bit for each transmitted character. When high while in the Synchronous mode, enables a parity check on each received character.

Bit 4: When high while the Receiver section is enabled (bit 2 of Control Register 1 is high) and in the Asynchronous mode, causes the INS1671 to enter the Echo mode. In this mode, the Transmitted Data (TDATA) output is obtained directly from the clocked regenerated data (assembled received characters) instead of the transmission characters from the Transmitter Register. Echoing does not start until a character has been received and the Transmitter section is idle. The Transmitter section does not have to be enabled in the Echo mode.

NOTE

Only the first character of a break condition of all zeros (null character) is echoed when a Line Break condition is detected. For all subsequent null characters with low-level Stop bits, a steady Marking (high) condition is transmitted until normal character reception is resumed.

When high while the Receiver section is enabled and in the Synchronous mode, causes stripping of received characters that match the contents of the DLE Register. In addition, parity checking is disabled at this time.

When high while the Receiver section is disabled and in the Synchronous mode, causes the generation of a low-level Miscellaneous ($\overline{MISC}$) output from the chip. (This output may be used as a New Sync signal on a Model 201 Data Set.) With a 32X clock selected, a high-level bit 4 causes the Receiver bit timing to be synchronized on Mark-Space (high-low) transitions.

Bit 5: When high while the Transmitter section is enabled and in the Asynchronous mode, causes a single Stop bit to be transmitted.

When low while the Transmitter section is enabled and in the Asynchronous mode, causes 2 Stop bits to be transmitted for character lengths of 6, 7, or 8 bits and 1½ Stop bits for a character length of 5 bits.

When high while the Transmitter section is disabled and in the Asynchronous mode, causes the generation of a low-level Miscellaneous ($\overline{MISC}$) output from the chip. (This output may be used for a Make Busy signal on a Model 103 Data Set, a Secondary Transmit signal on a Model 202 Data Set, and a Dialing Signal on a CBS Data Coupler.)

When high in coincidence with a high-level bit 6 while in the Synchronous mode, causes the contents of the DLE Register to be transmitted before the loading of the next character in the Transmitter Holding Register, as part of the Transmit Transparent mode.

When high in coincidence with a low-level bit 6 of Control Register 1 while in the Synchronous mode, enables transmit parity. If bit 6 is high or bit 5 is low, no parity is generated.

Bit 6: When high while the Transmitter section is enabled and in the Asynchronous mode, holds the Transmitted Data (TDATA) output of the chip in a Spacing (low) condition, starting at the end of any current transmitted character. In this case, normal transmitter timing continues so that the Transmission Break condition is timed out after the loading of new characters in the Transmitter Holding Register.

When high while in the Synchronous mode, conditions the Transmitter section to the Transmit Transparent mode, which implies that the idle Transmitter time will be filled by DLE-SYN character transmission and that a DLE can be forced ahead of any character in the Transmitter Holding Register by setting bit 5 of Control Register 1 high, prior to loading the THR.

Bit 7: When low, the INS1671 is configured to provide an internal data and control loop (On-line Diagnostic mode), and the Ring Indicator On interrupt is disabled. When high, the chip is in the normal full duplex configuration and the Ring Indicator On interrupt is enabled.

In the On-line Diagnostic mode, the following occur (via internal logic):

1. The TDATA output (pin 37) is connected to the RDATA input (pin 27). The TDATA output is held in the Marking (high) condition and the RDATA input from the MODEM or data set is disregarded.
2. The Transmitter clock is also used as the Receiver clock, when the 1X clock is selected by bits 0 - 2 of Control Register 1.
3. Bit 0 (Data Terminal Ready) of Control Register 1 is connected to the $\overline{DSR}$ input (pin 28). The $\overline{DTR}$ output (pin 16) is held in the Off (high) condition and the $\overline{DSR}$ input from the MODEM or data set is disregarded.
4. Bit 1 (Request to Send) of Control Register 1 is connected to both the $\overline{CTS}$ input (pin 36)

and the $\overline{CARR}$ input (pin 29). The $\overline{RTS}$ output (pin 38) is held in the Off (high) condition and the $\overline{CTS}$ and $\overline{CARR}$ inputs from the MODEM or data set are disregarded.

5. The $\overline{MISC}$ output (pin 19) is held in the Off (high) condition.

CONTROL REGISTER 2 (CR2) CONTENTS

Bits 0-2: Select clocks for Receiver and Transmitter secitions of the chip as indicated below.

B_2	B_1	B_0	Clock Selected
0	0	0	1XTC and 1XRC inputs for Transmitter and Receiver sections, respectively
0	0	1	R1 (32X) input
0	1	0	R2 (32X) input
0	1	1	R3 (32X) input
1	0	0	R4 (32X) input
1	0	1	R4 (64X) input ÷2
1	1	0	R4 (128X) input ÷4
1	1	1	R4 (256X) input ÷8

Bit 3: When low while in the Asynchronous mode, selects the R1 (32X) clock input for the Receiver section of the chip. When high, selects the same 32X clock rate for the Receiver section as selected for the Transmitter section.

NOTE

Bit 3 must be high (logic 1) for the 1X clock selection by bits 0-2 of Control Register 2.

When high while in the Synchronous mode, causes stripping of all DLE and SYN characters in the Transmit Transparent mode (selected by bit 6 of Control Register 1) or of all SYN characters in the Transmit Non-Transparent mode. In addition, no Data Received interrupt is generated and the SYN Detect status bit is set high with the reception of the next assembled character.

Bit 4: When high while parity is enabled (bit 3 and/or bit 5 of Control Register 1 are high), selects Odd parity. When low while parity is enabled, selects Even parity.

Bit 5: When high, selects the Synchronous mode for the INS1671. When low, selects the Asynchronous mode for the chip.

Bits 6 and 7: Select the character length as indicated below.

B_7	B_6	Character Length
0	0	8 bits
0	1	7 bits
1	0	6 bits
1	1	5 bits

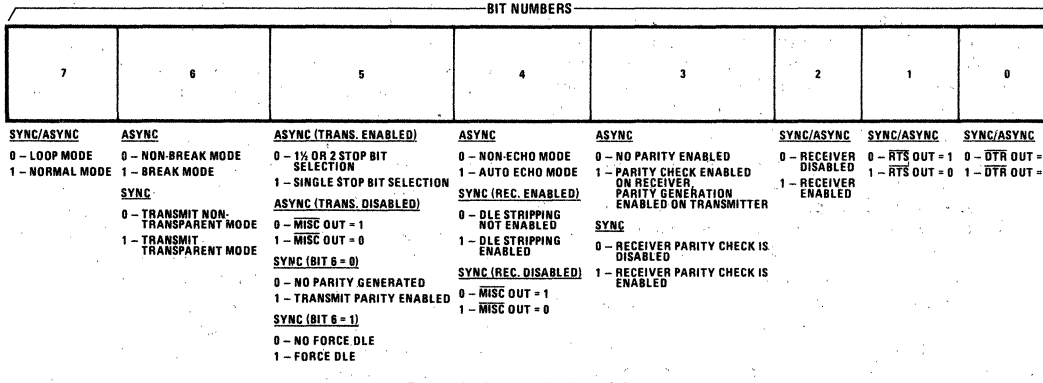


Figure 1. Control Register 1 Contents

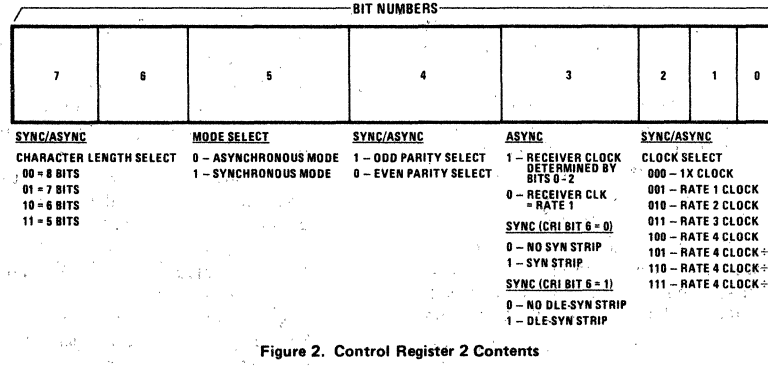


Figure 2. Control Register 2 Contents

INS1671 Status Register

The Status Register of the INS1671 holds information that defines data conditions of the Receiver and Transmitter sections of the chip, and the status of the MODEM or data set. This 8-bit register can be read onto the DAL Bus by a Read operation. The contents of the Status Register are shown in figure 3 and are described below.

Bit 0: When high, indicates that no character is contained in the Transmitter Holding Register while the Transmitter section is enabled. Bit 0 is set high when the contents of the Transmitter Holding Register are transferred to the Transmitter Register. Bit 0 is reset low when the Transmitter Holding Register is loaded from the DAL Bus or when the Transmitter section is disabled by forcing the $\overline{CTS}$ input to a high level.

Bit 1: When high, indicates that the Receiver Holding Register has been loaded from the Receiver Register while the Receiver section is enabled. Bit 1 is reset low when the Receiver Holding Register is read onto the DAL Bus or when the Receiver Section is disabled by forcing bit 2 of Control Register 1 to a low level.

Bit 2: When high, indicates an overrun error that occurs if the previous character in the Receiver Holding Register has not been read onto the DAL Bus and Data Received status bit 0 has not been reset low, at the time a new character is to be transferred to the Receiver Holding Register. Bit 2 is reset low when no overrun error is detected or when the Receiver section is disabled.

Bit 3: When high while DLE stripping is enabled (bit 4 of Control Register 1 is high) and the Receiver section is enabled, indicates that the character previous to the presently assembled character matched the contents of the DLE Register. Bit 3 is reset low when a no match condition exists between the previous character and the contents of the DLE Register.

When high while DLE stripping is disabled, parity checking is enabled (bit 3 of Control Register 1 is high) and the Receiver section is enabled, indicates that the last received character has a parity error. Bit 3 is reset low when a correct parity condition exists.

NOTE

Bit 3 is reset low during DLE stripping or parity error checking when the Receiver section is disabled.

Bit 4: When high while in the Asynchronous mode, indicates that the Received Data (RDATA) input contains a low-level Stop bit after the last bit of the character (framing error), while the Receiver section is enabled. Bit 4 is reset low when the proper high-level Stop bit is detected.

When high while in the Synchronous mode, indicates that the contents of the Receiver Register matched the contents of the SYN Register, while the Receiver section is enabled. Bit 4 remains high for the duration of a full character assembly.

NOTE

Bit 4 is reset low in both modes when the Receiver section is disabled.

Bit 5: Complement of the active low-level Carrier Detector ($\overline{CARR}$) input.

Bit 6: Complement of the active low-level Data Set Ready ($\overline{DSR}$) input. Bit 6 may be used for a Secondary Receive signal on type 202 data sets.

Bit 7: When high, indicates that there is a change in the state of the Data Set Ready ($\overline{DSR}$) or Carrier Detector ($\overline{CARR}$) input to the INS1671, while the internal Data Terminal Ready signal (bit 0 of Control Register 1) is high (On); or that the Ring Indicator ($\overline{RING}$) input is low (On) while the internal Data Terminal Ready signal (bit 0 of Control Register 1) is low (Off). Bit 7 is reset low when the contents of the Status Register are read onto the DAL Bus.

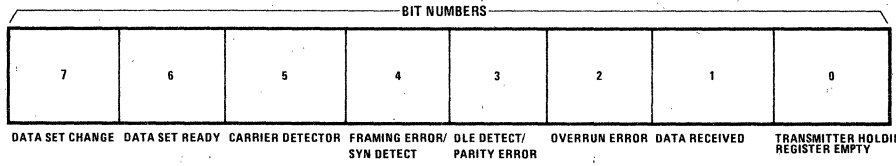


Figure 3. Status Register Contents

D.4

INS1671 Operation

The following describes the operation of the INS1671 chip. Use the functional block diagram on page 5 as necessary to follow these descriptions.

ASYNCHRONOUS MODE

Framing of asynchronous characters is provided by a low-level (logic 0) Start bit at the beginning of a character and a high-level (logic 1) Stop bit at the end of a character. Reception of a character is initiated on recognition of the first Start bit after a preceding Stop bit by a positive transition of the receiver clock. The Start and Stop bits are stripped off while assembling the serial input into a parallel character.

The character assembly is completed by the reception of the Stop bit after reception of the last character bit. If this bit is high, the character is determined to have correct framing and the INS1671 is prepared to receive the next character. If the Stop bit is low, the Framing Error flag (bit 4 of Status Register) is set and the Receiver section assumes this bit to be the Start bit of the next character. Character assembly continues from this point if the input is still low, when sampled at the theoretical center of the assumed Start bit. As long as the Receiver input is a Spacing (low) condition, all zero characters are assembled and error flags and Data Received interrupts are generated so that Line Break conditions can be detected. After a character of all zeroes is assembled along with a zero in the Stop bit location, the first received Marking (high) condition is determined as a Stop bit and this resets the Receiver section to a Ready state for assembly of the next character.

In the Asynchronous mode, the character transmission occurs when information contained in the Transmitter Holding Register is transferred to the Transmitter Register. Transmission is initiated by the insertion of a Start bit, followed by the serial output of the character least significant bit first with parity (if enabled) following the most significant bit; then the insertion of a 1-, 1½-, or 2-bit length Stop condition. If the Transmitter Holding Register is full, the next character transmission starts after the transmission of the Stop bit of the present character in the Transmitter Register. Otherwise, the Marking condition is continuously transmitted until the Transmitter Holding Register is loaded.

In order to allow re-transmission of data received at a slightly faster character rate, means are provided for shortening the Stop bit length to allow transmission of characters to occur at the same rate as the reception of characters. The Stop bit is shortened by 1/16 of a bit period for 1-Stop bit selection and 3/16 of a bit period for 1½- or 2-Stop bit selection, if the next character is ready in the Transmitter Holding Register.

SYNCHRONOUS MODE

Framing of characters is carried out by a special Synchronization (SYN) Character Code transmitted at the beginning of a block of characters. When the Receiver section is enabled, it searches for two continuous characters matching the bit pattern contained in the SYN Register. During the time the Receiver section is searching, data is not transferred to the Receiver Holding Register, status bits are not updated, and the Receiver interrupt is not activated. After the detection of the first SYN character, the Receiver section assembles subsequent bits into characters whose length is determined by the contents of Control Register 2. If, after the first SYN character detection, a second SYN character is present, the Receiver section enters the synchronized state until the Receiver Enable Bit (bit 2 of Control Register 1) is turned Off. If a second successive SYN character is not detected, the Receiver reverts to the Search mode.

In the Synchronous mode, a continuous stream of characters is transmitted once the Transmitter section is enabled. If the Transmitter Holding Register is not loaded at the time the Transmitter Register has completed transmission of a character, this idle time will be filled by a transmission of the character contained in the SYN register in the Transmit Non-Transparent mode, or the characters contained in the DLE and SYN registers respectively while in the Transmit Transparent mode of operation.

DETAILED OPERATION

Receiver Section: The data input to the Receiver section is clocked into the Receiver Register by a 1X Receiver clock from a MODEM or data set, or by a local 32X bit rate clock selected from one of four externally supplied clock inputs. When using the 1X clock, the Received Data (RDATA) input is sampled on the positive transition of the clock in both the Asynchronous and Synchronous modes. When using a 32X clock in the Asynchronous mode, the Receiver sampling clock is phased to the Mark-To-Space transition of the Start bit of the data input and defines, through clock counts, the center of each received data bit within +0%, -3% at the positive transition 16 clock periods later.

In the Synchronous mode, the Receiver sampling clock is phased to all Mark-To-Space transitions of the data inputs when using a 32X clock. Each transition of the data causes an incremental correction of the sampling clock by 1/32 of a bit period. The sampling clock can be immediately phased to every Mark-To-Space data transition by setting bit 4 of Control Register 1 high, while the Receiver section is disabled.

When the complete character has been shifted into the Receiver Register, it is then transferred to the Receiver Holding Register; the unused, higher number bits are filled with zeroes. At this time, the Receiver status bits (Framing Error/SYN Detect, Parity Error/DLE Detect, Overrun Error, and Data Received) are updated in the Status Register and the Data Received interrupt is activated. Parity Error is set, if encountered while the Receiver parity check is enabled in Control Register 1. The Overrun Error flag (bit 2 of Status Register) is set if the Data Received status bit (bit 1) is not cleared through a Read operation by an external device, when a new character is ready to be transferred to the Receiver Holding Register. This error flag indicates that a character has been lost, as new data is lost and the old data and its status flags are saved.

The characters assembled in the Receiver Register that match the contents of the SYN or DLE Register are not

loaded into the Receiver Holding Register, and the Data Received interrupt is not generated, if bit 3 (SYN Strip) of Control Register 2 or bit 4 (DLE Strip) of Control Register 1 are set respectively; the SYN-DET and DLE-DET status bits are set with the next non-SYN or non-DLE character. When both the SYN Strip and DLE Strip bits are set (Transmit Transparent mode), the DLE-SYN combination is stripped. The SYN comparison occurs only with the character received after the DLE character. If two successive DLE characters are received, only the first DLE character is stripped. No parity check is made while in this mode.

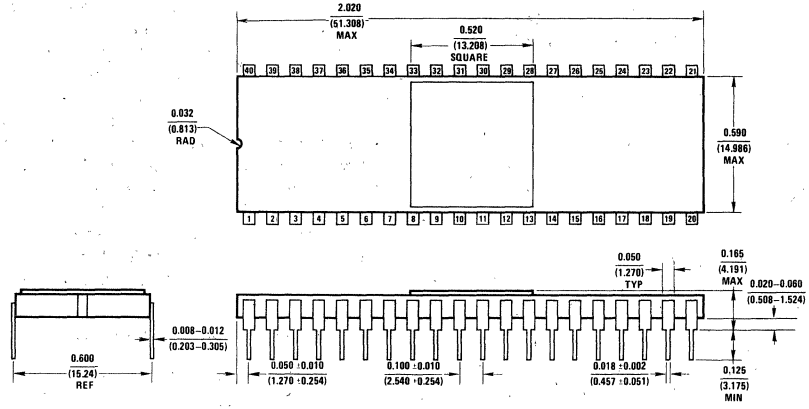
Transmitter Section: Information is transferred to the Transmitter Holding Register by a Write operation. Information can be loaded into this register at any time, even when the Transmitter section is not enabled. Transmission of data is initiated only when the Request to Send ($\overline{RTS}$) bit (bit 1 of Control Register 1) is set high and the Clear to Send ($\overline{CTS}$) input is low. Information is normally transferred from the Transmitter Holding Register to the Transmitter Register when the latter has completed transmission of a character. However, information in the DLE Register may be transferred prior to the information contained in the Transmitter Holding Register if the Force DLE signal condition is enabled (bits 5 and 6 of Control Register 1 set high). The Force DLE control bit (bit 5 of Control Register 1) must be set prior to loading of a new character in the Transmitter Holding Register to ensure forcing the DLE character prior to transmission of the data character. The Transmitter Register output is applied to a flip-flop which delays the output by one clock period. When using the 1X clock generated by the MODEM or data set, the output data changes state on the negative clock transition and the delay is one bit period. When using a local 32X clock, the Transmitter section selects one of the four selected rate inputs and divides the clock down to the baud rate. This clock is phased to the Transmitter Holding Register Empty flag (bit 0 of Status Register) such that transmission of characters occurs within two clock times of the loading of the Transmitter Holding Register, when the Transmitter Register is empty.

When the Transmitter section is enabled, a Transmitter interrupt is generated each time the Transmitter Holding Register is empty. If the Transmitter Holding Register is empty when the Transmitter Register is ready for a new character, the Transmitter section enters an idle state. During this idle time, a high will be presented to the Transmitted Data (TDATA) output in the Anynchronous mode or the contents of the SYN Register will be presented in the Synchronous Transmit Non-Transparent mode. In the Synchronous Transmit Transparent mode (enabled by a high-level bit 6 of Control Register 1), the idle state will be filled by a DLE-SYN character transmission in that order. When entering the Transmit Transparent mode, the DLE-SYN fill will not occur until the first forced DLE.

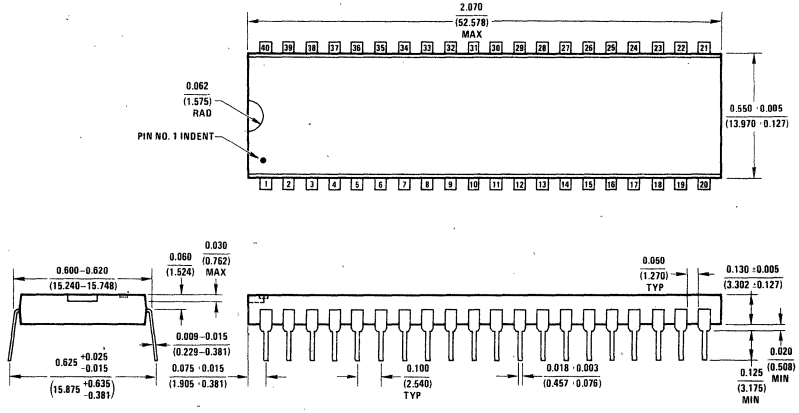
If the Transmitter section is disabled by a reset of the Request to Send control bit, any partially transmitted character is completed before the Transmitter section of the INS1671 is disabled. As soon as the Clear to Send ($\overline{CTS}$) input goes high, the Transmitted Data output will go high.

When the Transmit parity is enabled, the selected Odd or Even parity bit is inserted into the last bit of the character in place of the last bit of the Transmitter Register. This limits transfer of character information to a maximum of seven bits plus parity or eight bits without parity. Parity cannot be enabled in the Synchronous Transmit Transparent mode.

Physical Dimensions



Ceramic Dual-In-Line Package (D)
Order Number INS1671D



Plastic Dual-In-Line Package (N)
Order Number INS1671N

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National Semiconductor

Preliminary
JULY 1978

INS8250 Asynchronous Communications Element

General Description

The INS8250 is a programmable Asynchronous Communications Element (ACE) chip contained in a standard 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, functions as a serial data input/output interface in a microcomputer system. The functional configuration of the INS8250 is programmed by the system software via a TRI-STATE® 8-bit bidirectional data bus.

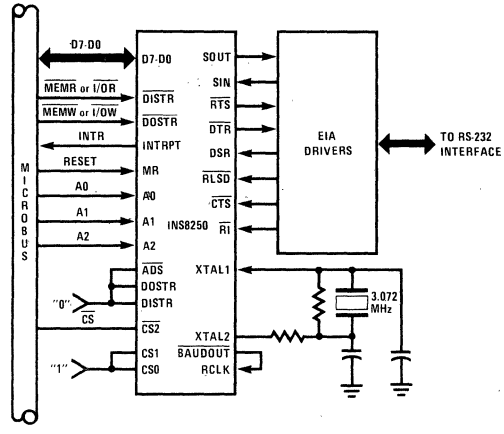
The INS8250 performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the INS8250 at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the INS8250, as well as any error conditions (parity, overrun, framing, or break interrupt).

In addition to providing control of asynchronous data communications, the INS8250 includes a programmable Baud Generator that is capable of dividing the timing reference clock input by divisors of 1 to $(2^{16} - 1)$, and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the INS8250 is a complete MODEM-control capability, and a processor-interrupt system that may be software tailored to the user's requirements to minimize the computing time required to handle the communications link.

Features

- Designed to be Easily Interfaced to Most Popular Microprocessors.
- Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or from Serial Data Stream
- Full Double Buffering Eliminates Need for Precise Synchronization
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Programmable Baud Rate Generator Allows Division of Any Input Clock by 1 to $(2^{16} - 1)$ and Generates the Internal 16x Clock
- Independent Receiver Clock Input
- MODEM Control Functions (CTS, RTS, DSR, DTR, RI, and Carrier Detect)
- Fully Programmable Serial-Interface Characteristics
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even, Odd, or No-Parity Bit Generation and Detection
  - 1-, 1½-, or 2-Stop Bit Generation
  - Baud Rate Generation (DC to 56k Baud)
- False Start Bit Detection
- Complete Status Reporting Capabilities
- TRI-STATE TTL Drive Capabilities for Bidirectional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities
  - Loopback Controls for Communications Link Fault Isolation
  - Break, Parity, Overrun, Framing Error Simulation
- Full Prioritized Interrupt System Controls
- Single +5-Volt Power Supply
- MICROBUS™* Compatible

INS8250 MICROBUS Configuration



*Trademark, National Semiconductor Corp.

Absolute Maximum Ratings

Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
All Input or Output Voltages with Respect to V_{SS} . . . . −0.5 V to +7.0 V
Power Dissipation . . . . . 400 mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics

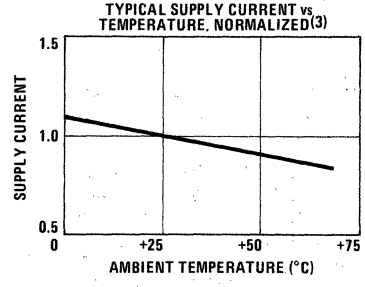
T_A = 0°C to +70°C, V_{CC} = +5 V ± 5%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{ILX}	Clock Input Low Voltage	−0.5		0.8	V	
V_{IHX}	Clock Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1.6 mA on all outputs,
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −100 µA
I_{CC} (AV)	Avg Power Supply Current (V_{CC})		65	80	mA	
I_{IL}	Input Leakage			±10	µA	
I_{CL}	Clock Leakage			±10	µA	

Capacitance

T_A = 25°C, V_{CC} = V_{SS} = 0 V

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
C_{XIN}	Clock Input Capacitance		15	20	pF	
C_{XOUT}	Clock Output Capacitance		20	30	pF	f_c = 1 MHz
C_{IN}	Input Capacitance		6	10	pF	Unmeasured pins returned to V_{SS}
C_{OUT}	Output Capacitance		10	20	pF	



AC Electrical Characteristics

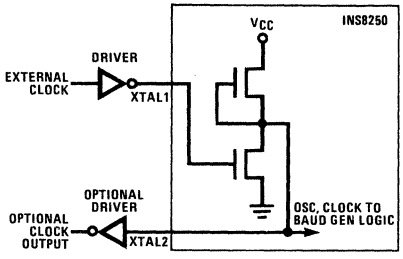
$T_A = 0°C$ to $\pm 70°C$, $V_{CC} = +5\ V \pm 5\%$

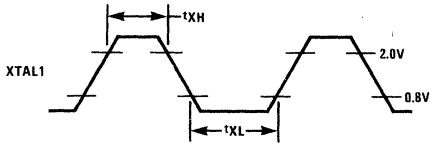
Symbol	Parameter	Min	Max	Units	Test Conditions
t_{AW}	Address Strobe Width	90	—	ns	
t_{AS}	Address Setup Time	110	—	ns	
t_{AH}	Address Hold Time	0	—	ns	
t_{CS}	Chip Select Setup Time	110	—	ns	
t_{CH}	Chip Select Hold Time	0	—	ns	
t_{CSS}	Chip Select Output Delay from Strobe	0	90	ns	–@ 100 pF loading
t_{DID}	$\overline{DISTR}$/DISTR Strobe Delay	0	—	ns	
t_{DIW}	$\overline{DISTR}$/DISTR Strobe Width	175	—	ns	
t_{RC}	Read Cycle Delay	1735	—	ns	
RC	Read Cycle = $t_{AW} + t_{DID} + t_{DIW} + t_{RC}$	2000	—	ns	
t_{DD}	$\overline{DISTR}$/DISTR to Driver Disable Delay	—	150	ns	–@ 100 pF loading
t_{DDD}	Delay from $\overline{DISTR}$/DISTR to Data	—	250	ns	–@ 100 pF loading
t_{HZ}	$\overline{DISTR}$/DISTR to Floating Data Delay	100	—	ns	–@ 100 pF loading
t_{DOD}	$\overline{DOSTR}$/DOSTR Strobe Delay	50	—	ns	
t_{DOW}	$\overline{DOSTR}$/DOSTR Strobe Width	175	—	ns	
t_{WC}	Write Cycle Delay	1785	—	ns	
WC	Write Cycle – $t_{AW} + t_{DOD} + t_{DOW} + t_{WC}$	2100	—	ns	
t_{DS}	Data Setup Time	175	—	ns	
t_{DH}	Data Hold Time	60	—	ns	
t_{CSC}*	Chip Select Output Delay from Select	—	200	ns	–@ 100 pF loading
t_{RA}*	Address Hold Time from $\overline{DISTR}$/DISTR	50	—	ns	
t_{RCS}*	Chip Select Hold Time from $\overline{DISTR}$/DISTR	50	—	ns	
t_{AR}*	$\overline{DISTR}$/DISTR Delay from Address	110	—	ns	
t_{CSR}*	$\overline{DISTR}$/DISTR Delay from Chip Select	110	—	ns	
t_{WA}*	Address Hold Time from $\overline{DOSTR}$/DOSTR	50	—	ns	
t_{WCS}*	Chip Select Hold Time from $\overline{DOSTR}$/DOSTR	50	—	ns	
t_{AW}*	$\overline{DOSTR}$/DOSTR Delay from Address	160	—	ns	
t_{CSW}*	$\overline{DOSTR}$/DOSTR Delay from Select	160	—	ns	
t_{MRW}	Master Reset Pulse Width	25	—	μs	

*Applicable only when $\overline{ADS}$ input is tied permanently low.

AC Electrical Characteristics (cont'd.)

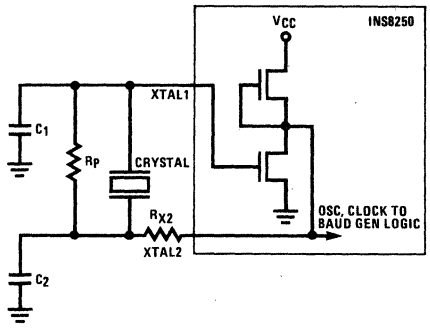
Symbol	Parameter	Min	Max	Units	Test Conditions
BAUD GENERATOR					
N	Baud Rate Divisor	1	$2^{16}-1$		
t_{BLD}	Baud Output Negative Edge Delay		250 typ	ns	100 pF Load
t_{BHD}	Baud Output Positive Edge Delay		250 typ	ns	100 pF Load
t_{LW}	Baud Output Down Time	425 typ		ns	100 pF Load
t_{HW}	Baud Output Up Time	330 typ		ns	100 pF Load
RECEIVER					
t_{SCD}	Delay from RCLK to Sample Time		2 typ	μs	
t_{SINT}	Delay from Stop to Set Interrupt		2 typ	μs	100 pF Load
t_{RINT}	Delay from $\overline{\text{DISTR}}$/DISTR (RD RBR/RDLSR) to Reset Interrupt		1 typ	μs	100 pF Load
TRANSMITTER					
t_{HR}	Delay from $\overline{\text{DOSTR}}$/DOSTR (WR THR) to Reset Interrupt		1 typ	μs	100 pF Load
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		16 typ	$\overline{\text{BAUDOUT}}$ Cycles	
t_{SI}	Delay from Initial Write to Interrupt		24 typ	$\overline{\text{BAUDOUT}}$ Cycles	
t_{SS}	Delay from Stop to Next Start		1 typ	μs	
t_{STI}	Delay from Stop to Interrupt (THRE)		8 typ	$\overline{\text{BAUDOUT}}$ Cycles	
t_{IR}	Delay from $\overline{\text{DISTR}}$/DISTR (RD IIR) to Reset Interrupt (THRE)		1 typ	μs	100 pF Load
MODEM CONTROL					
t_{MDO}	Delay from DOSTR/$\overline{\text{DOSTR}}$ (WR MCR) to Output		1 typ	μs	100 pF Load
t_{SIM}	Delay to Set Interrupt from MODEM Input		1 typ	μs	100 pF Load
t_{RIM}	Delay to Reset Interrupt from $\overline{\text{DISTR}}$/DISTR (RD MSR)		1 typ	μs	100 pF Load





Timing	Min	Units
t_{XH}	140	ns
t_{XL}	140	ns

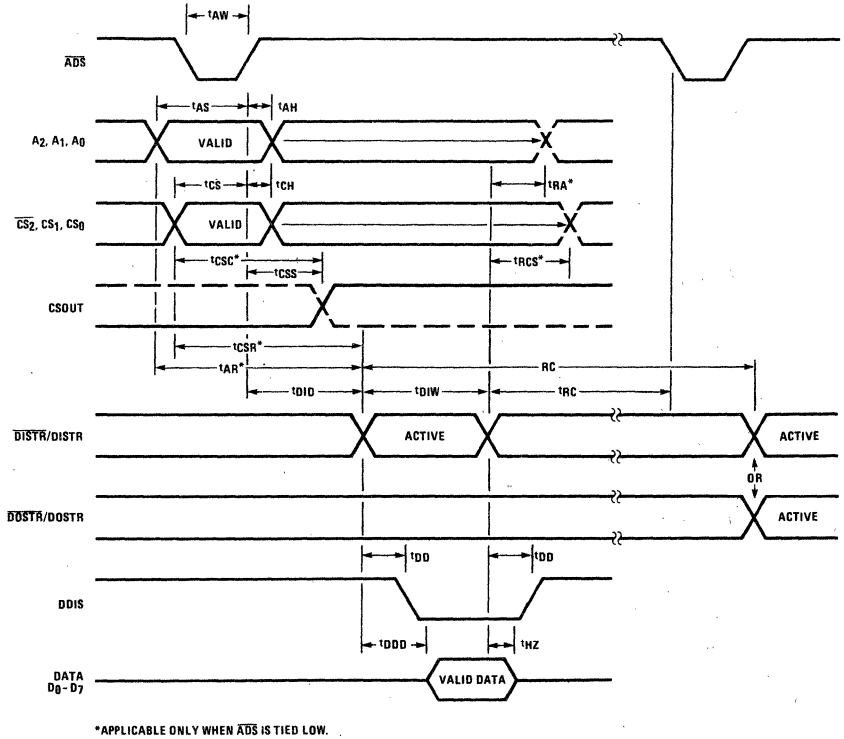
A. External Clock Input (3.1 MHz Max.)



CRYSTAL	RP	RX2	C1	C2
3.1 MHz	1 MΩ	1.5K	10 - 30 pF	40 - 60 pF

B. Typical Crystal Oscillator Network

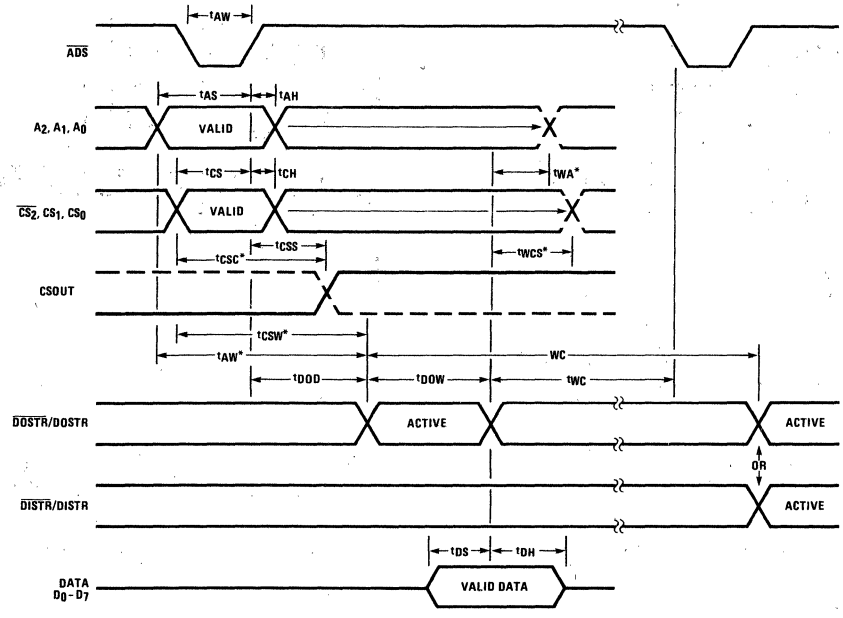
Timing Waveforms



*APPLICABLE ONLY WHEN ADS IS TIED LOW.

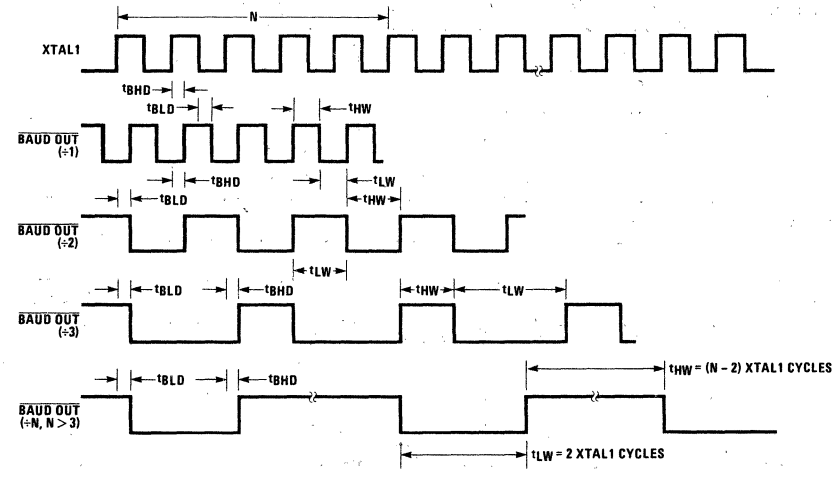
Read Cycle

Timing Waveforms (cont'd.)



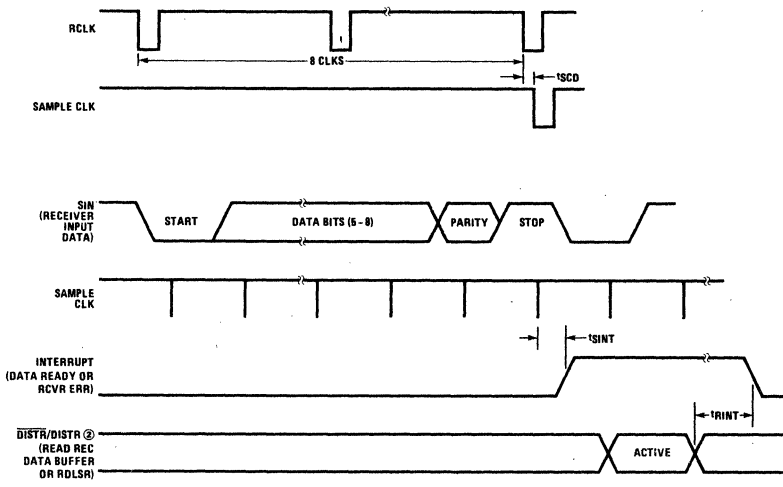
*APPLICABLE ONLY WHEN ADS IS TIED LOW.

Write Cycle

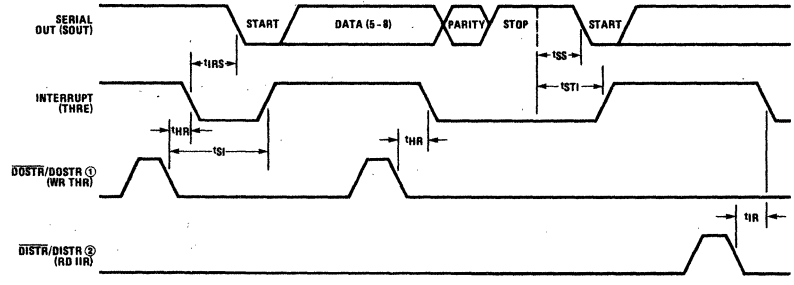


BAUDOUT Timing

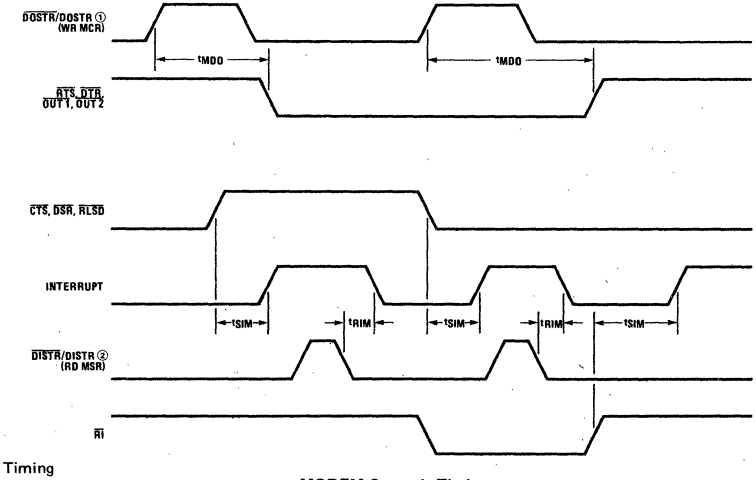
Timing Waveforms (cont'd.)



Receiver Timing



Transmitter Timing

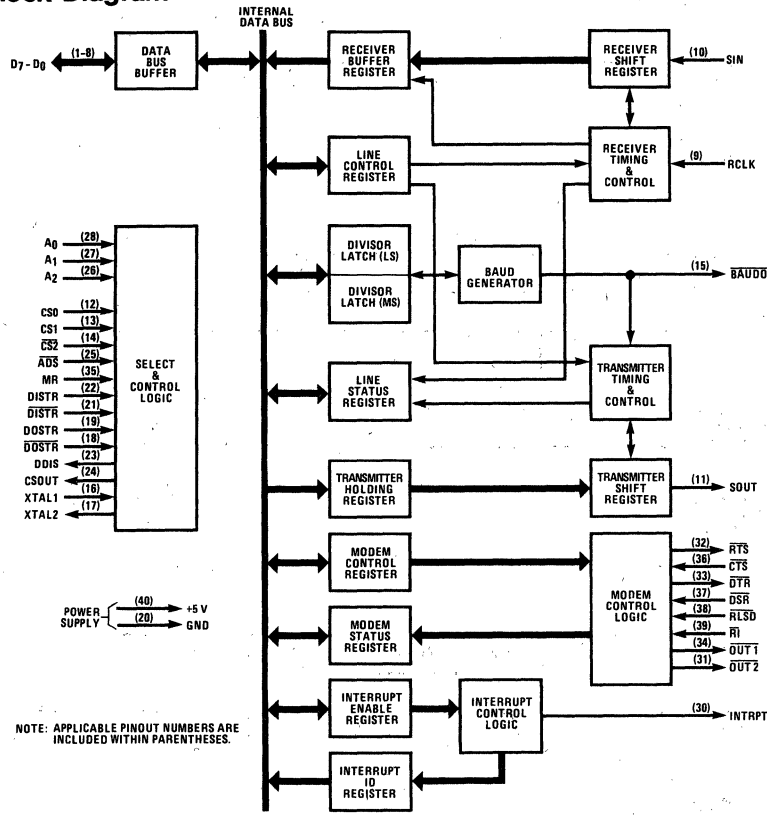


MODEM Controls Timing

NOTES:
① See Write Cycle Timing
② See Read Cycle Timing

D.4

INS8250 Block Diagram



INS8250 Functional Pin Description

The following describes the function of all INS8250 input/output pins. Some of these descriptions reference internal circuits.

NOTE

In the following descriptions, a low represents a logic 0 (0 volt nominal) and a high represents a logic 1 (+2.4 volts nominal).

INPUT SIGNALS

Chip Select (CS0, CS1, $\overline{CS2}$), Pins 12 - 14: When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) Address Strobe ($\overline{ADS}$) input. This enables communication between the INS8250 and the CPU.

Data Input Strobe (DISTR, $\overline{DISTR}$), Pins 22 and 21: When DISTR is high or $\overline{DISTR}$ is low while the chip is selected, allows the CPU to read status information or data from a selected register of the INS8250.

NOTE

Only an active DISTR or $\overline{DISTR}$ input is required to transfer data from the INS8250 during a read operation. Therefore, tie either the DISTR input permanently low or the $\overline{DISTR}$ input permanently high, if not used.

Data Output Strobe (DOSTR, $\overline{DOSTR}$), Pins 19 and 18: When DOSTR is high or $\overline{DOSTR}$ is low while the chip is selected, allows the CPU to write data or control words into a selected register of the INS8250.

NOTE

Only an active DOSTR or $\overline{DOSTR}$ input is required to transfer data to the INS8250 during a write operation. Therefore, tie either the DOSTR input permanently low or the $\overline{DOSTR}$ input permanently high, if not used.

Address Strobe ($\overline{ADS}$), Pin 25: When low, provides latching for the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{CS2}$) signals.

NOTE

An active $\overline{ADS}$ input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{ADS}$ input permanently low.

Register Select (A0, A1, A2), Pins 26 - 28: These three inputs are used during a read or write operation to select an INS8250 register to read from or write into as indicated in the table below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain INS8250 registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	None
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Master Reset (MR), Pin 35: When high, clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the INS8250. Also, the state of various output signals (SOUT, INTRPT, $\overline{OUT\,1}$, $\overline{OUT\,2}$, $\overline{RTS}$, $\overline{DTR}$) are affected by an active MR input. (Refer to table 1.)

Receiver Clock (RCLK), Pin 9: This input is the 16x baud rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

Clear to Send ($\overline{CTS}$), Pin 36: The $\overline{CTS}$ signal is a MODEM control function input whose condition can be tested by the CPU by reading bit 4 (CTS) of the MODEM Status Register. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Data Set Ready ($\overline{DSR}$), Pin 37: When low, indicates that the MODEM or data set is ready to establish the communications link and transfer data with the INS8250. The $\overline{DSR}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MODEM Status Register. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Received Line Signal Detect ($\overline{RLSD}$), Pin 38: When low, indicates that the data carrier has been detected by the MODEM or data set. The $\overline{RLSD}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 7 (RLSD) of the MODEM Status Register. Bit 3 (DRLSD) of the MODEM Status Register indicates whether the $\overline{RLSD}$ input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the RLSD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Ring Indicator ($\overline{RI}$), Pin 39: When low, indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 6 (RI) of the MODEM Status Register. Bit 2 (TERI) of the MODEM Status Register indicates whether the $\overline{RI}$ input has changed from a low to a high state since the previous reading of the MODEM Status Register.

NOTE

Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Interrupt is enabled.

V_{CC}, Pin 40: +5-volt supply.

V_{SS}, Pin 20: Ground (0-volt) reference.

OUTPUT SIGNALS

Data Terminal Ready ($\overline{DTR}$), Pin 33: When low, informs the MODEM or data set that the INS8250 is ready to communicate. The DTR output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. The $\overline{DTR}$ signal is set high upon a Master Reset operation.

Request to Send ($\overline{RTS}$), Pin 32: When low, informs the MODEM or data set that the INS8250 is ready to transmit data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. The $\overline{RTS}$ signal is set high upon a Master Reset operation.

Output 1 ($\overline{OUT\,1}$), Pin 34: User-designated output that can be set to an active low by programming bit 2 ($\overline{OUT\,1}$) of the MODEM Control Register to a high level. The $\overline{OUT\,1}$ signal is set high upon a Master Reset operation.

Output 2 ($\overline{OUT\,2}$), Pin 31: User-designated output that can be set to an active low by programming bit 3 ($\overline{OUT\,2}$) of the MODEM Control Register to a high level. The $\overline{OUT\,2}$ signal is set high upon a Master Reset operation.

Chip Select Out (CSOUT), Pin 24: When high, indicates that the chip has been selected by active CS0, CS1, and $\overline{CS2}$ inputs. No data transfer can be initiated until the CSOUT signal is a logic 1.

Driver Disable (DDIS), Pin 23: Goes low whenever the CPU is reading data from the INS8250. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and INS8250 on the D_7-D_0 Data Bus) at all times, except when the CPU is reading data.

Baud Out ($\overline{BAUDOUT}$), Pin 15: 16x clock signal for the transmitter section of the INS8250. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input of the chip.

Interrupt (INTRPT), Pin 30: Goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available; Transmitter Holding Register Empty; and MODEM Status. The INTRPT signal is reset low upon the appropriate interrupt service or a Master Reset operation.

Serial Output (SOUT), Pin 11: Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation.

INPUT/OUTPUT SIGNALS

Data ($D_7 - D_0$) Bus, Pins 1 - 8: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the INS8250 and the CPU. Data, control words, and status information are transferred via the $D_7 - D_0$ Data Bus.

External Clock Input/Output (XTAL 1, XTAL 2), Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the INS8250.

Pin Configuration

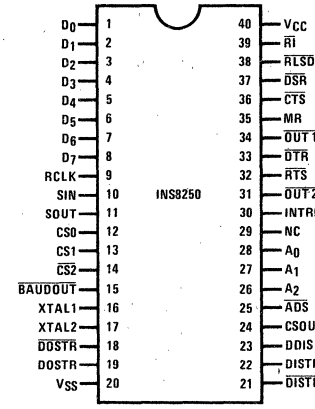


Table 1. ACE Reset Functions

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low (0 - 3 forced and 4 - 7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3 - 7 are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 & 6 are High
MODEM Status Register	Master Reset	Bits 0 - 3 Low Bits 4 - 7 — Input Signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{\text{OUT 2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{OUT 1}}$	Master Reset	High

INS8250 Accessible Registers

The system programmer may access or control any of the INS8250 registers summarized in table 2 via the CPU. These registers are used to control INS8250 operations and to transmit and receive data.

INS8250 LINE CONTROL REGISTER

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated in table 2 and are described below.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1½ Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Table 2. Summary of INS8250 Accessible Registers

	Register Address									
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	3	4	5	6	0 DLAB = 1	1 DLAB = 1
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Shift Register Empty (TSRE)	Ring Indicator (RI)	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Received Line Signal Detect (RLSD)	Bit 7	Bit 15

* Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver as a logic 0 if bit 4 is a logic 1 or as a logic 1 if bit 4 is a logic 0.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there regardless of other transmitter activity. The set break is disabled by setting bit 6 to a logic 0. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

INS8250 PROGRAMMABLE BAUD RATE GENERATOR

The INS8250 contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3.1 MHz) and dividing it by any divisor from 1 to $(2^{16}-1)$. The output frequency of the Baud Generator is 16x the Baud rate [divisor # = (frequency input) ÷ (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Rate Generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38400 and below the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

NOTE

The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 3 and below, the maximum frequency is equal to the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1 MHz. In no case should the data rate be greater than 56k Baud.

LINE STATUS REGISTER

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 may be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Table 3. Baud Rates Using 1.8432 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired & Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

NOTE: 1.8432 MHz is the standard 8080 frequency divided by 10.

Table 4. Baud Rates Using 3.072 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired & Actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits).

NOTE

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the INS8250 is ready to accept a new character for transmission. In addition, this bit causes the INS8250 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register. Bit 6 is a read-only bit.

Bit 7: This bit is permanently set to logic 0.

INTERRUPT IDENTIFICATION REGISTER

The INS8250 has an on-chip interrupt capability that allows for complete flexibility in interfacing to all the popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the INS8250 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt are stored in the Interrupt Identification Register (refer to table 5). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in table 5.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Table 5. Interrupt Control Functions

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

INTERRUPT ENABLE REGISTER

This 8-bit register enables the four types of interrupts of the INS8250 to separately active the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

MODEM CONTROL REGISTER

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in table 2 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

NOTE

The $\overline{DTR}$ output of the INS8250 may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a loopback feature for diagnostic testing of the INS8250. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the INS8250.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The INS8250 interrupt system can be tested by writing into the lower six bits of the Line Status Register and the lower four bits of the MODEM Status Register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal INS8250 operation. To return to normal operation, the registers must be reprogrammed for normal operation and then bit 4 of the MODEM Control Register must be reset to logic 0.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM STATUS REGISTER

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the $\overline{RLSD}$ input to the chip has changed state.

NOTE

Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Received Line Signal Detect ($\overline{RLSD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 of the MCR.

Typical Applications

Figures 1 and 2 show how to use the INS8250 chip in an INS8080A system and in a microcomputer system with a high-capacity data bus.

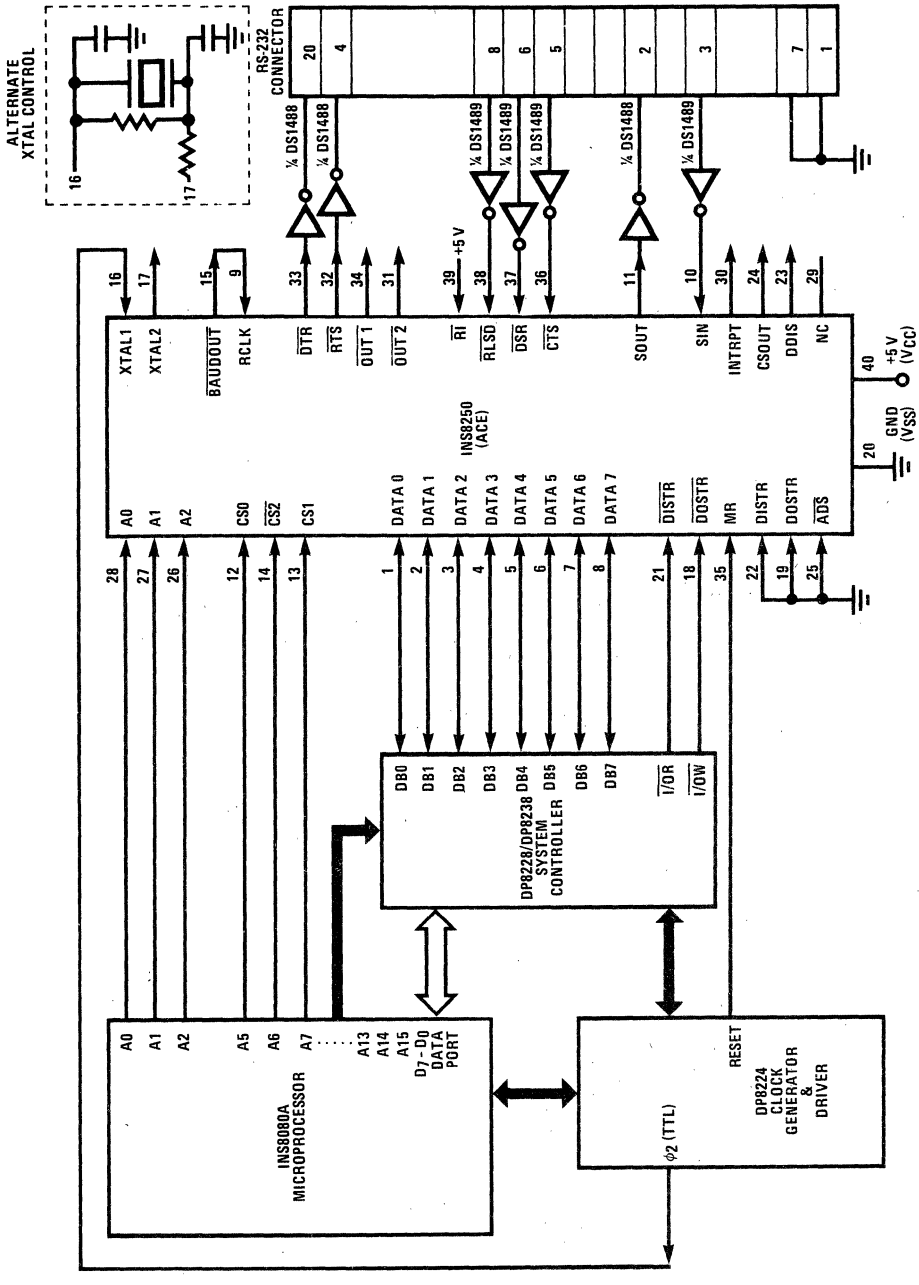


Figure 1. Typical INS8080A/INS8250 RS-232 Terminal Interface

D.4

Typical Applications (cont'd)

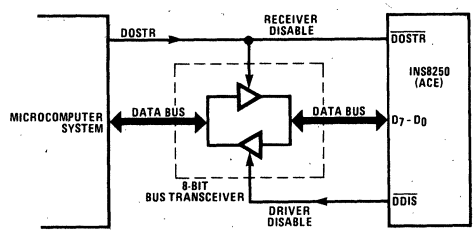
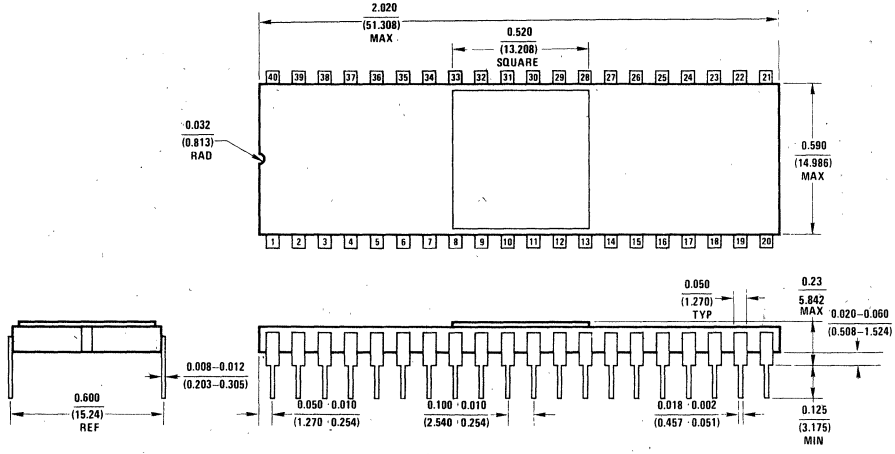


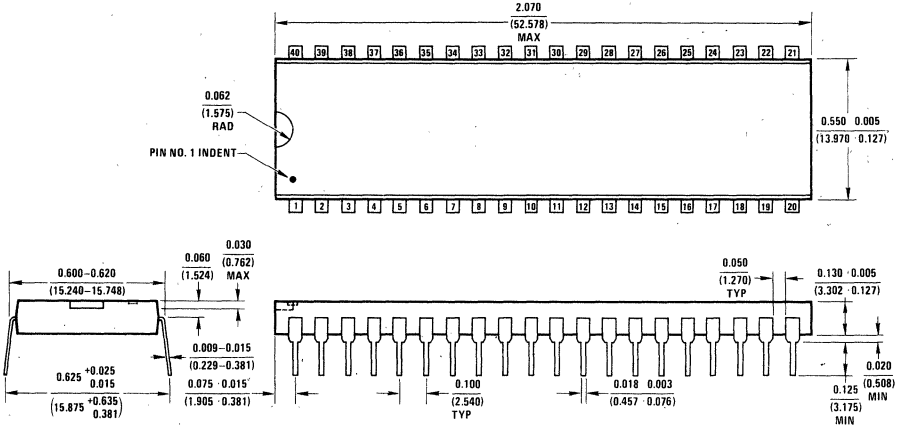
Figure 2. Typical Interface for a High-Capacity Data Bus

Physical Dimensions

inches (millimeters)



Ceramic Dual-In-Line Package (D)
Order Number INS8250D
NS Package Number D40C



Plastic Dual-In-Line Package (N)
Order Number INS8250N
NS Package Number D40A

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INS8251 Programmable Communication Interface

General Description

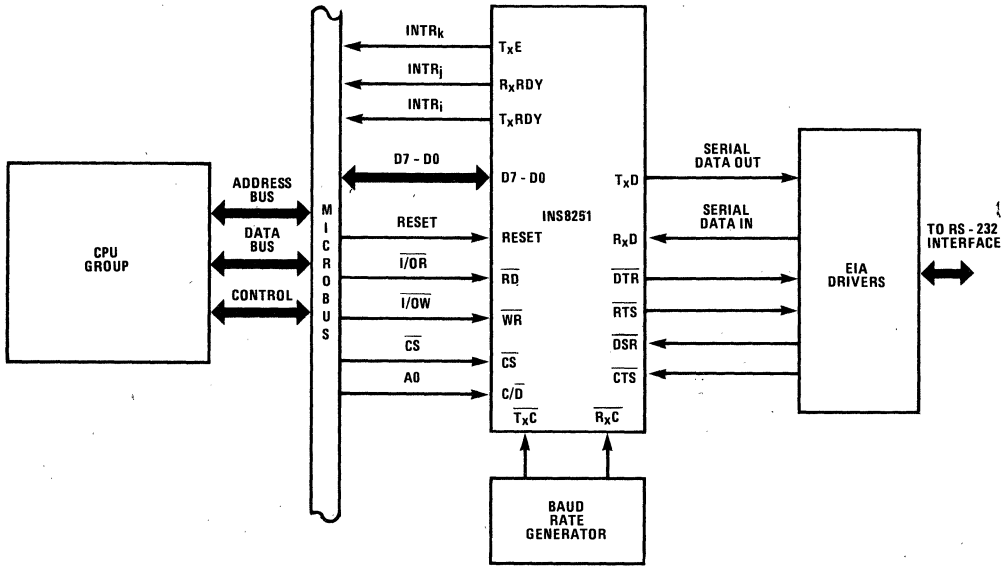
The INS8251 is a programmable Universal Synchronous/Asynchronous Receiver/Transmitter (USART) chip contained in a standard 28-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, functions as a serial data input/output interface in National Semiconductor's N8080 microcomputer family. The functional configuration of the INS8251 is programmed by the system software for maximum flexibility, thereby allowing the system to receive and transmit virtually any serial data communication signal presently in use (including IBM Bisync).

The INS8251 can be programmed to receive and transmit either synchronous or asynchronous serial data. The INS8251 performs serial-to-parallel conversion on data characters received from an input/output device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the INS8251 at any time during the functional operation. Status information reported includes the type and the condition of the transfer operations being performed by the INS8251, as well as any transmission error conditions (parity, overrun, or framing).

Features

- Synchronous and Asynchronous Full Duplex Operations
- Synchronous Mode Capabilities
  - Selectable 5- to 8-Bit Characters
  - Internal or External Character Synchronization
  - Automatic Sync Insertion
- Asynchronous Mode Capabilities
  - Selectable 5- to 8-Bit Characters
  - 3 Selectable Clock Rates (1x, 16x or 64x the Baud Rate)
  - Line Break Detection and Generation
  - 1-, 1½-, or 2-Stop Bit Detection and Generation
  - False Start Bit Detection
- Baud Rates
  - DC to 56k Baud (Synchronous Mode)
  - DC to 9.6k Baud (Asynchronous Mode)
- Transmission Error Detection Capabilities
  - Parity
  - Overrun
  - Framing
- Double Buffering of Data
- TTL Compatible
- Single TTL Clock
- Reduces System Component Count
- MICROBUS™* Compatible

INS8251 MICROBUS Configuration



*Trademark, National Semiconductor Corp.

Absolute Maximum Ratings

Ambient Temperature Under Bias. . . . . 0°C to +70°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin with Respect to Ground . . . . . -0.5 V to +7 V
Power Dissipation . . . . . 1 Watt

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

DC Electrical Characteristics

T_A = 0°C to +70°C; V_{CC} = 5.0 V ± 5%; GND = 0 V

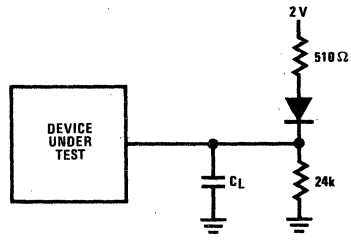
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -100 μA
I_{DL}	Data Bus Leakage			-50 10	μA μA	V_{OUT} = 0.45 V V_{OUT} = V_{CC}
I_{IL}	Input Leakage			10	μA	V_{IN} = V_{CC}
I_{CC}	Power Supply Current		45	80	mA	

Capacitance

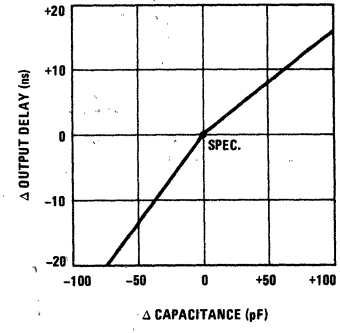
T_A = 25°C; V_{CC} = GND = 0 V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	f_C = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND.

Test Load Circuit



Typical Δ Output Delay vs. Δ Capacitance (pF)



AC Electrical Characteristics

$T_A = 0°C$ to $+70°C$; $V_{CC} = 5.0\ V \pm 5\%$; GND = 0 V

Symbol	Parameter	Min	Max	Unit	Test Conditions
BUS PARAMETERS (Note 1)					
Read Cycle					
t_{AR}	Address Stable Before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	50		ns	
t_{RA}	Address Hold Time for $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	5		ns	
t_{RR}	$\overline{READ}$ Pulse Width	430		ns	
t_{RD}	Data Delay from $\overline{READ}$		350	ns	$C_L = 100\ pF$
t_{DF}	$\overline{READ}$ to Data Floating		200	ns	$C_L = 100\ pF$
		25		ns	$C_L = 15\ pF$
t_{RV}	Recovery Time Between WRITES (Note 2)	6		t_{CY}	
Write Cycle					
t_{AW}	Address Stable Before $\overline{WRITE}$	20		ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$	20		ns	
t_{WW}	$\overline{WRITE}$ Pulse Width	400		ns	
t_{DW}	Data Set-Up Time for $\overline{WRITE}$	200		ns	
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		ns	
OTHER TIMINGS					
t_{CY}	Clock Period (Note 3)	0.420	1.35	μs	
$t_{\phi W}$	Clock Pulse Width	220	0.7 t_{CY}	ns	
t_R, t_F	Clock Rise and Fall Time	0	50	ns	
t_{DTx}	TxD Delay from Falling Edge of $\overline{TxC}$		1	μs	$C_L = 100\ pF$
t_{SRx}	Rx Data Set-Up Time to Sampling Pulse	2		μs	$C_L = 100\ pF$
t_{HRx}	Rx Data Hold Time to Sampling Pulse	2		μs	$C_L = 100\ pF$
f_{Tx}	Transmitter Input Clock Frequency				
	1x Baud Rate	DC	56	kHz	
	16x and 64x Baud Rate	DC	520	kHz	
t_{TPW}	Transmitter Input Clock Pulse Width				
	1x Baud Rate	12		t_{CY}	
	16x and 64x Baud Rate	1		t_{CY}	
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1x Baud Rate	15		t_{CY}	
	16x and 64x Baud Rate	3		t_{CY}	
f_{Rx}	Receiver Input Clock Frequency				
	1x Baud Rate	DC	56	kHz	
	16x and 64x Baud Rate	DC	520	kHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1x Baud Rate	12		t_{CY}	
	16x and 64x Baud Rate	1		t_{CY}	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1x Baud Rate	15		t_{CY}	
	16x and 64x Baud Rate	3		t_{CY}	
t_{Tx}	TxRDY Delay from Center of Data Bit		16	t_{CY}	$C_L = 50\ pF$
t_{Rx}	RxRDY Delay from Center of Data Bit		20	t_{CY}	
t_{IS}	Internal SYNDET Delay from Center of Data Bit		25	t_{CY}	
t_{ES}	Internal SYNDET Set-Up Time Before Falling Edge of $\overline{RxC}$		16	t_{CY}	
t_{TxE}	TxEMPTY Delay from Center of Data Bit		16	t_{CY}	$C_L = 50\ pF$
t_{WC}	Control Delay from Rising Edge of $\overline{WRITE}$ (TxE, $\overline{DTR}$, $\overline{RTS}$)		16	t_{CY}	
t_{CR}	Control to $\overline{READ}$ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)		16	t_{CY}	

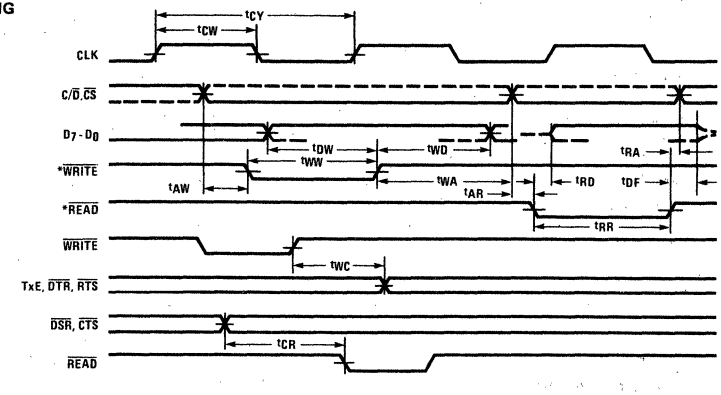
NOTES:

1. AC timings measured at $V_{OH} = 2.0\ V$, $V_{OL} = 0.8\ V$, and with test load circuit of page 2.
2. This recovery time is for initialization only, when MODE, SYNC1, SYNC2, COMMAND and first DATA BYTES are written into the USART. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.
3. The $\overline{TxC}$ and $\overline{RxC}$ frequencies have the following limitations with respect to CLK:
   for 1x Baud Rate, f_{Tx} or $f_{Rx} \leq 1/30\ t_{CY}$)
   for 16x and 64x Baud Rate, f_{Tx} or $f_{RX} \leq 1/4.5\ t_{CY}$)
4. Reset Pulse Width = $6\ t_{CY}$ minimum.

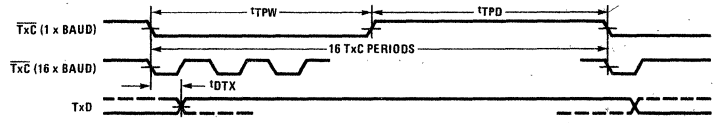
Timing Waveforms

READ AND WRITE TIMING

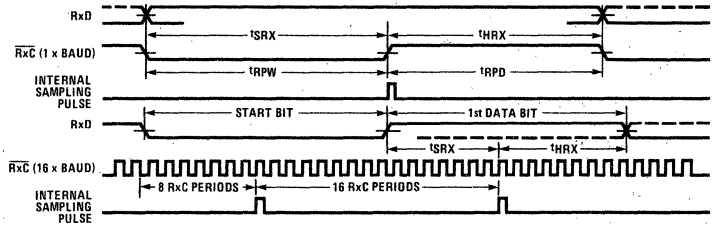
*WRITE AND READ PULSES HAVE NO TIMING LIMITATION WITH RESPECT TO CLK.



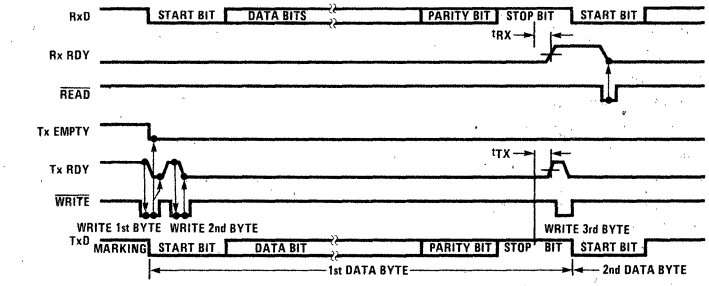
TRANSMITTER CLOCK AND DATA



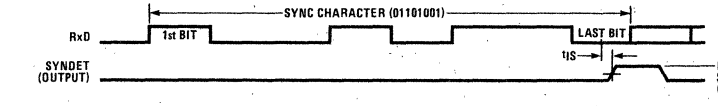
RECEIVER CLOCK AND DATA



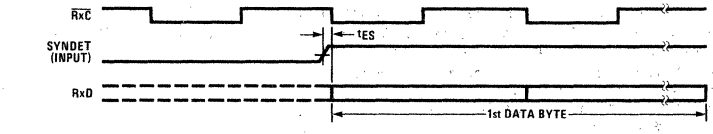
Tx RDY AND Rx RDY TIMING (ASYNC MODE)



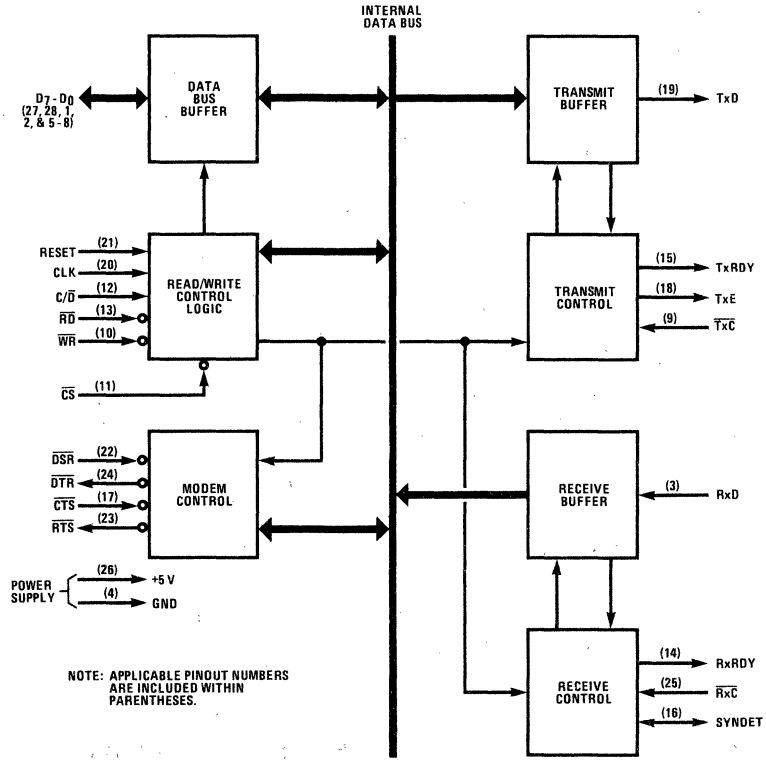
INTERNAL SYNC DETECT



EXTERNAL SYNC DETECT



INS8251 Block Diagram



INS8251 Functional Pin Definitions

The following describes the function of all the INS8251 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Chip Select ($\overline{CS}$): When low (logic 0), the chip is selected. This enables communication between the INS8251 and the INS8080A microprocessor.

Read ($\overline{RD}$): When low, allows the INS8080A to read data or status information from the INS8251.

Write ($\overline{WR}$): When low, allows the INS8080A to write data or control words into the INS8251.

Control/Data (C/$\overline{D}$): Used in conjunction with an active $\overline{RD}$ or $\overline{WR}$ input (logic 0) to determine overall device operation as indicated below.

$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	Operation
0	0	0	1	Data character read from INS8251
0	0	1	0	Data character written into INS8251
0	1	0	1	Status information read from INS8251
0	1	1	0	Control word written into INS8251
1	x	x	x	Device not selected

Reset: When high (logic 1), places the INS8251 in the idle mode. The device remains in this mode until a new set of control words is written into the INS8251 to program its functional definition. Minimum Reset pulse width is 6 t_{CY}.

Clock (CLK): TTL clock that is used to generate internal timing signals for the INS8251. The minimum frequency of the CLK input is 30 times the receiver/transmitter clock frequency for the synchronous mode, and 4.5 times the receiver/transmitter clock frequency for the asynchronous mode. The CLK input is normally connected to the ϕ_2 (TTL) output of the INS8224 Clock Generator and Driver device.

Transmitter Clock ($\overline{TxC}$): This clock input controls the rate at which a data character is to be transmitted. The frequency of the $\overline{TxC}$ input is equal to the Baud Rate for the synchronous mode, and is a multiple (1x, 16x or 64x) of the Baud Rate for the asynchronous mode. A portion of the Mode Instruction Word (see figure) selects the value of the Baud Rate Factor when in the asynchronous mode. Transmitter Data are clocked out of the INS8251 on the falling edge of the $\overline{TxC}$ input.

Data Set Ready ($\overline{DSR}$): General-purpose input whose condition can be tested by the INS8080A using a status read operation. However, a low-level $\overline{DSR}$ input is normally used to test data set ready conditions.

Clear to Send ($\overline{CTS}$): If low when the TxEN bit (D_0) of the Command Instruction Control Word (see figure) is set high, enables the INS8251 to transmit serial data.

Receiver Data (RxD): Serial data input from a MODEM or an input/output device.

Receiver Clock ($\overline{RxC}$): This clock input controls the rate at which a data character is to be received. The frequency and selection of the $\overline{RxC}$ input is as described above for the $\overline{TxC}$ input. Receiver data are clocked into the INS8251 on the rising edge of the $\overline{RxC}$ input.

V_{CC}: +5-volt supply.

Ground: 0-volt reference.

OUTPUT SIGNALS

Data Terminal Ready ($\overline{DTR}$): General-purpose output which can be set to an active low by programming the $\overline{DTR}$ bit (D_1) of the Command Instruction Control Word. However, a low-level DTR output is normally used for data terminal ready or rate select control.

Request to Send ($\overline{RTS}$): General-purpose output which can be set to an active low by programming the $\overline{RTS}$ bit (D_5) of the Command Instruction Control Word. However, the RTS output is normally used for request to send control in the transmit mode.

Transmitter Data (TxD): Composite serial data output to a MODEM or input/output device. The TxD output is held in the marking state (logic 1) upon a Reset operation.

Transmitter Ready (TxRDY): When high, alerts the INS8080A that the transmitter is ready to accept a data character. The TxRDY output, which is automatically reset whenever a character is written into the INS8251, can be used as an interrupt to the system. For polled operation, the condition of the TxRDY signal can be tested by the INS8080A using a status read operation.

Transmitter Empty (TxE): Goes high to indicate the end of a transmit mode. The TxE output is automatically reset whenever a character is written into the INS8251. In the synchronous mode, a high-level TxE output indicates that a character has not been loaded, the transmitter buffer is empty, and the sync character(s) of a data block are soon to be transmitted automatically as fillers.

Receiver Ready (RxRDY): When high, alerts the INS8080A that the receiver contains a data character that is ready to be input to the CPU. The RxRDY output, which is automatically reset whenever a character is read from the INS8251, can be used as an interrupt to the system. For polled operation, the condition of the RxRDY signal can be tested by the INS8080A using a status read operation.

INPUT/OUTPUT SIGNALS

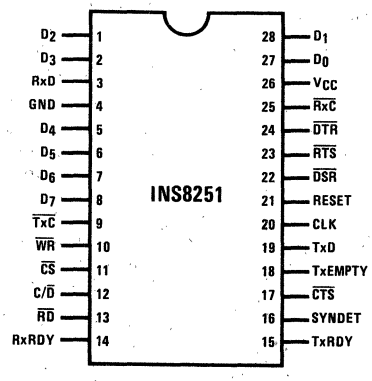
Data (D_7 - D_0) Bus: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the INS8251 and the INS8080A. Data are routed to or from the internal data bus buffer upon execution of an INS8080A OUT or IN instruction, respectively. In addition, control words, command words and status information are transferred through the data bus buffer.

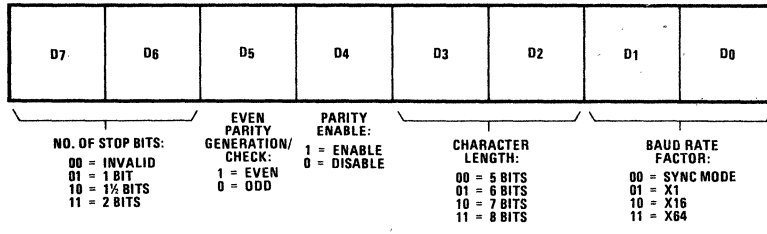
Sync Detect (SYNDET): This pin may be used in the synchronous mode only. System software can program SYNDET as either an input or an output. When used as an output (internal sync detect mode), a high-level SYNDET indicates that the INS8251 has detected sync character(s) in the received serial data. The SYNDET output is automatically reset upon a status read operation by the INS8080A. When used as an input (external sync detect mode), a high-level SYNDET causes the INS8251 to start assembling data characters on the falling edge of the next RxC input.

INS8251 Programming

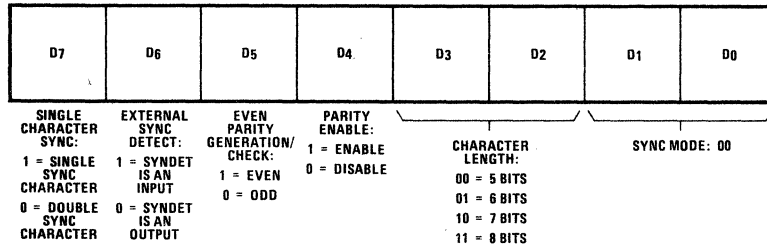
The system software uses a Mode Instruction Control Word and a Command Instruction Control Word (see figures) to establish the complete functional definition of the INS8251. These control words must immediately follow an internal or external reset operation. Once the Mode Instruction Control Word has been written into the INS8251 by the CPU, sync characters (when applicable) or Command Instruction Control Words may be inserted as shown in the typical data block transfer diagram.

Pin Configuration



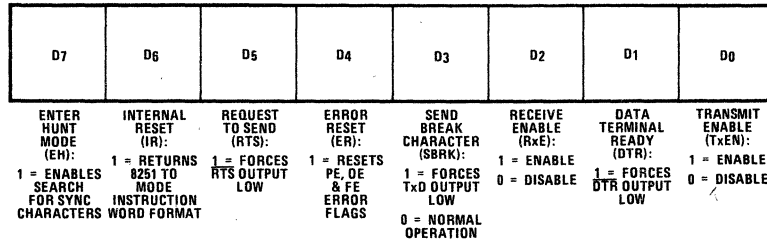


ASYNCHRONOUS MODE

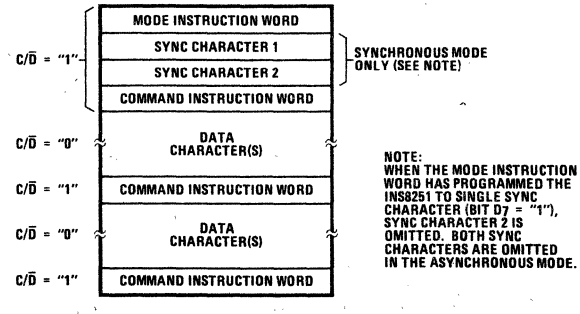


SYNCHRONOUS MODE

mode instruction control word format



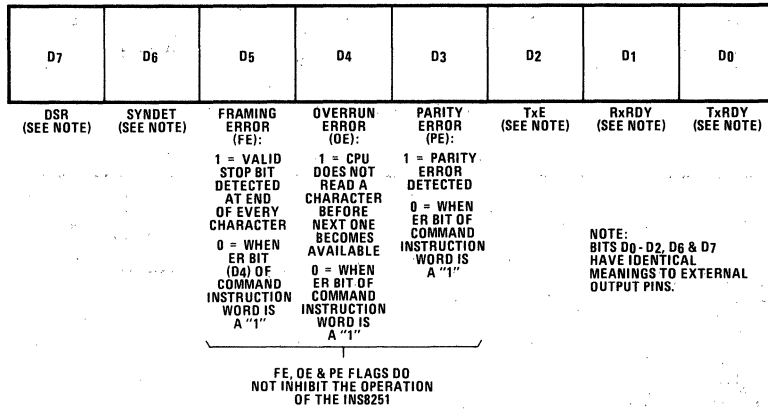
command instruction control word format



typical data block transfer

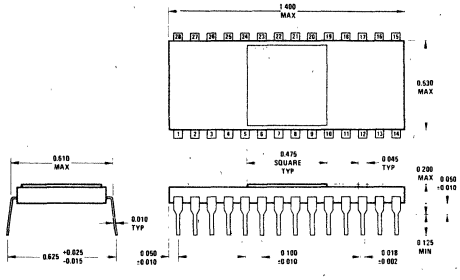
INS8251 Status

The INS8251 has provisions for allowing the programmer to read the status of the device at any time during the functional operation. When the C/$\overline{D}$ input is a high-level, a normal read operation is executed to read this status information. The figure below shows the bits in the Status Read Word format. Since some of the status word bits have identical meaning to external output pins, the INS8251 can be used in a completely polled environment or in an interrupt driven environment.



status read word format

Physical Dimensions



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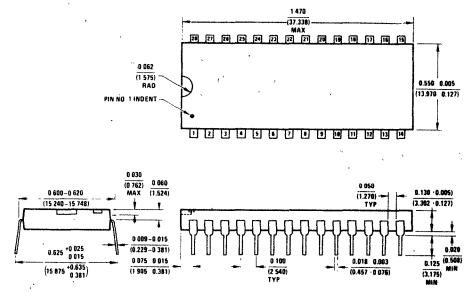

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