MEMORY
DATABOOK

NATIONAL
SEMICONDUCTOR

MEMORY
DATABOOK

National Semiconductor Corporation 2900 Semiconductor Drive Santa Clara, California 95051 Tel: (408) 737-5000 TWX: (910) 339-9240

President's Message

Dear Customer:

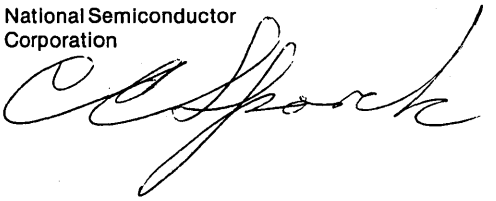
The exciting future of memory applications is limited only by our collective abilities to make use of the continuing stream of rapid technological advances. Annual consumption of semiconductor memory components has already surpassed a billion dollars per year and will soon cross the two billion dollar level. Years ago National established the reputation as a high volume supplier of high quality, cost-effective components for the complete range of discretes, linears, optoelectronics, transducers, A/D and D/A, hybrids, large scale integrated memory, microprocessor and logic arrays. We are pleased to continue our expansion of this broad product line to include the memories you will require in the future.

National is leading the way to higher density memories and we are the innovators of "the system environment approach to memory component testing".*

Our world-wide network of factory representatives, local stocking distributors, and field applications engineers is at your service to help meet your needs — just give any of them a call.

We appreciate your interest in National's products and services, and look forward to supplying your present and future requirements.

National Semiconductor
Corporation



Charles E. Sporck
President

* Refer to the following page.

MST™ Program
The System Environment Approach to Memory Component Testing

The Memory System Test (MST) program is designed to provide our customers with mainframe memory components that *have already been through the test/temperature processing that the user normally implements at the board level.*

This program assures memory components of significantly better quality and higher reliability than that achieved by the usual approach to memory component testing. *MST processed components have experienced board level environmental testing over the temperature range of 25°C to 70°C.*The parts are tested 4 separate times with 4 different test set-ups and 3 kinds of testers (this includes the final QA electrical testing) which also contributes to the increased quality.

Specifying MST processing offers you the following:

- Provides parts that have already operated in a system environment within system margins at maximum operating temperature
- Simplifies system checkout and shortens card burn-in/test
- Eliminates inventory throughput time at incoming test or at independent test laboratories
- Eliminates inventory cost and throughput time at board test and reduces inventory cost and throughput time at system test
- Eliminates the need for additional burn-in and testing at independent test laboratories
- Reduces board rework
- Reduces field failures and equipment downtime
- Provides soft error detection during component processing
- Increases reliability

The result is you get higher quality at lower cost.

Present Capability

The MST process can be specified for all of the mainframe dynamic RAMs manufactured by National. Tooling exists for the memory components listed here at the time of this printing.

Part No.	Organization
MM5298	8k × 1
MM5290	16k × 1
NMC5295	16k × 1 (5V only part)
NMC4164	64k × 1 (5V only part)

How to specify MST

Contact your local NSC Representative or Sales Office for a full briefing on your options.

Table of Contents

Section 1—NMOS RAMs

Section 2—CMOS RAMs

Table of Contents (Continued)

Section 2—CMOS RAMs (Continued)

Section 3—Bipolar RAMs

Section 4—Magnetic Bubble Memories

Section 5—MOS EPROMs

Table of Contents (Continued)

Section 6—Bipolar PROMs

Section 7—MOS ROMs

Section 8—Character Generators

Table of Contents (Continued)

Section 9—Memory Support Circuits

Section 10—Physical Dimensions

Alpha-Numerical Index

Alpha-Numerical Index (Continued)

Alpha-Numerical Index (Continued)

Alpha-Numerical Index (Continued)

Alpha-Numerical Index (Continued)

Definition of Terms

The following selection guides as well as the data sheets in this manual include products that represent the state-of-the-art design and processing of semiconductor memories. These devices had not been released to production at the time this book was printed. No orders can be placed for these devices without prior approval by National Semiconductor via your local National representative or distributor. These products are in various stages of design and/or pre-production. Samples *may* be available as you read this. Contact your local representative or distributor for up-to-date status on product availability.

The individual data sheets show the product status at the time of printing. These classification labels are defined as follows:

Status	Product Stage	Specifications
PREVIEW	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
ADVANCE INFORMATION	Sampling or Pre-Production	This data sheet contains advance information and specifications are subject to change without notice.
PRELIMINARY	First Production	This data sheet contains preliminary data and supplementary data will be published at a later date. NSC reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Proposed Standard Terminology

This databook includes a new set of symbols. This new format is a proposed industry standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent.

DC Electrical Parameter Abbreviations

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

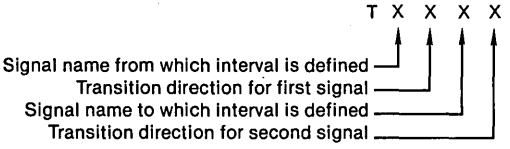
V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL—Input Low Voltage
IOZ—Output Leakage Current

AC Electrical Parameter Abbreviations

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four or more descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two or more descriptors for each signal point specify the signal name and signal transitions. The format using four descriptors is:



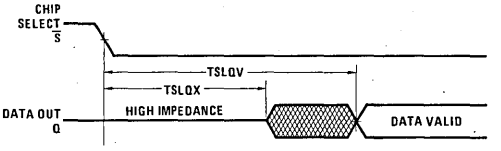
Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

Example:



Chip Select access time, TSLQV, the time from Chip Select low to Data Out valid, and the time from Chip Select low to Data Out active, TSLQX, are shown.

Timing Limits

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view; e.g., the address set-up time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view, e.g., the access time is shown as a maximum since the device never provides data later than that time.

Waveforms

Waveform Symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	N/A	HIGH IMPEDANCE

MOS RAM Selection Guide

Size	Organization	Part No.	Operation	Max Supply Current (mA)	Standby Current (mA)	Max Access Time (ns)	Supply Voltage (V)	Pkg	Temp* Range	Status**
65,536	65,536 × 1	NMC4164-2	Dynamic	45	4	120	+5	16	C	Preview
		NMC4164-3	Dynamic	45	4	150	+5	16	C	Preview
	8,192 × 8	NMC4864	Pseudo-Static	40	6	150	+5	28	C	Preview
32,768	4,096 × 8	NMC6132-3	Pseudo-Static	40	25	200	+5	28	C	Preview
		NMC6132-4	Pseudo-Static	40	25	250	+5	28	C	Preview
		NMC6132-5	Pseudo-Static	40	25	300	+5	28	C	Preview
16,384	16,384 × 1	NMC5295-2	Dynamic	35	4	80	+5	16	C	Advance Info
		NMC5295-3	Dynamic	35	4	100	+5	16	C	Advance Info
		NMC5295-4	Dynamic	35	4	120	+5	16	C	Advance Info
		MM5290-1	Dynamic	40	1.5	120	±5, +12	16	C	Production
		MM5290-2	Dynamic	40	1.5	150	±5, +12	16	C	Production
		MM5290-3	Dynamic	40	1.5	200	±5, +12	16	C	Production
		MM5290-4	Dynamic	40	1.5	250	±5, +12	16	C	Production
8,192	8,192 × 1	MM5298A-2	Dynamic	40	1.5	150	±5, +12	16	C	Production
		MM5298A-3	Dynamic	40	1.5	200	±5, +12	16	C	Production
		MM5298A-4	Dynamic	40	1.5	250	±5, +12	16	C	Production
		MM5298B-2	Dynamic	40	1.5	150	±5, +12	16	C	Production
		MM5298B-3	Dynamic	40	1.5	200	±5, +12	16	C	Production
		MM5298B-4	Dynamic	40	1.5	250	±5, +12	16	C	Production
4,096	4,096 × 1	MM2147	Static	160	20	70	+5	18	C	Production
		MM2147-3	Static	180	30	55	+5	18	C	Production
		MM2147L	Static	140	10	70	+5	18	C	Production
		MM2147L-1	Static	140	10	90	+5	18	C	Production
		NMC2141	Static	120	15	120	+5	18	C	Preview
		NMC5257A	Static	120	120	120	+5	18	C	Preview
		MM5257	Static	90	90	450	+5	18	C	Production
		MM5257L	Static	65	65	450	+5	18	C	Production
		MM5257-2	Static	90	90	200	+5	18	C	Production
		MM5257-2L	Static	65	65	200	+5	18	C	Production
4,096	4,096 × 1	MM5257-3	Static	90	90	300	+5	18	C	Production
		MM5257-3L	Static	65	65	300	+5	18	C	Production
		MM4280	Dynamic	60	≈0	270	±5, +12	22	I	Production
		MM5280	Dynamic	60	≈0	200	±5, +12	22	C	Production
		MM5280-5	Dynamic	60	≈0	270	±5, +12	22	C	Production
	1,024 × 4	NMC2148	Static	160	20	70	+5	18	C	Preview
		NMC2148-3	Static	180	30	55	+5	18	C	Preview
		NMC2148L	Static	140	10	70	+5	18	C	Preview
		NMC2142A	Static	50	50	120	+5	20	C	Preview
		NMC2142AP	Static	15	15	120	+5	20	C	Preview
		NMC2114A	Static	50	50	120	+5	20	C	Preview
		NMC2114AP	Static	50	15	120	+5	18	C	Preview
		MM2114	Static	100	100	450	+5	18	C	Production
		MM2114L	Static	70	70	450	+5	18	C	Production
		MM2114-2	Static	100	100	200	+5	18	C	Production
		MM2114-2L	Static	70	70	200	+5	18	C	Production
		MM2114-3	Static	100	100	300	+5	18	C	Production
		MM2114-3L	Static	70	70	300	+5	18	C	Production
1,024	1,024 × 1	MM2102A	Static	50	50	350	+5	16	C	Production
		MM2102A-L	Static	33	33	350	+5	16	C	Production
		MM2102A-2	Static	50	50	250	+5	16	C	Production
		MM2102A-2L	Static	33	33	250	+5	16	C	Production
		MM2102A-4	Static	50	50	450	+5	16	C	Production
		MM2102A-4L	Static	33	33	450	+5	16	C	Production
		MM2102A-6	Static	50	50	650	+5	16	C	Production
		MM2102A-6L	Static	33	33	650	+5	16	C	Production

*C = 0°C to 70°C
I = −40°C to +85°C

**See Definition of Terms

CMOS RAM Selection Guide

Size	Organization	Part No.	Max Supply Current (mA)	Standby Current (nA)	Max Access Time (ns)	Supply Voltage (V)	Pkg	Temp* Range	Status**
4,096	4,096 × 1	NMC6504-9	7	50	320	+5	18	I	Preliminary
		NMC6504-5	7	500	370	+5	18	C	Preliminary
	1,024 × 4	NMC6514-2	7	50	320	+5	18	M	Preliminary
		NMC6514-9	7	50	320	+5	18	I	Preliminary
		NMC6514-5	7	500	370	+5	18	C	Preliminary
1,024	1,024 × 1	NMC6508B-2	4	10	180	+5	16	M	Production
		NMC6508-2	4	10	250	+5	16	M	Production
		NMC6508B-9	4	10	180	+5	16	I	Production
		NMC6508-9	4	10	250	+5	16	I	Production
		NMC6508-5	4	100	310	+5	16	C	Production
		MM54C929	4	20	265	+5	16	M	Production
		MM74C929	4	10	240	+5	16	I	Production
		MM74C929-3	4	100	315	+5	16	I	Production
		NMC6518B-2	4	10	180	+5	18	M	Production
		NMC6518-2	4	10	250	+5	18	M	Production
		NMC6518B-9	4	10	180	+5	18	I	Production
		NMC6518-9	4	10	250	+5	18	I	Production
		NMC6518-5	4	100	310	+5	18	C	Production
		MM54C930	4	20	265	+5	18	M	Production
		MM74C930	4	10	240	+5	18	I	Production
		MM74C930-3	4	100	315	+5	18	I	Production
	256 × 4	NMC6551B-2	4	10	220	+5	22	M	Production
		NMC6551-2	4	10	300	+5	22	M	Production
		NMC6551B-9	4	10	220	+5	22	I	Production
1,024	256 × 4	NMC6551-9	4	10	300	+5	22	I	Production
		NMC6551-5	4	10	360	+5	22	C	Production
		MM54C921	4	20	275	+5	22	M	Production
		MM74C921	4	10	250	+5	22	I	Production
		MM74C921-3	4	100	325	+5	22	I	Production
		NMC6552B-2	4	10	220	+5	18	M	Production
		NMC6552-2	4	10	300	+5	18	M	Production
		NMC6552B-9	4	10	220	+5	18	I	Production
		NMC6552-9	4	10	300	+5	18	I	Production
		NMC6552-5	4	100	360	+5	18	C	Production
		MM54C920	4	20	275	+5	22	M	Production
		MM74C920	4	10	250	+5	22	I	Production
		MM74C920-3	4	100	325	+5	22	I	Production

*C = 0°C to +70°C
I = −40°C to +85°C
M = −55°C to +125°C

**See Definition of Terms

MOS EPROM Selection Guide

Size	Organization	Part No.	Max Supply Current (mA)	Standby Current (mA)	Max Access Time (ns)	Supply Voltage (V)	Pkg	Temp* Range	Status**
65,536	8,192 × 8	NMC2564	180	30	450	+5	28	C	Preview
32,768	4,096 × 8	NMC2732	150	30	450	+5	24	C	Preliminary
		NMC2532	150	30	450	+5	24	C	Advance Info
16,384	2,048 × 8	NMC27C16	10/MHz	0.05	450	+5	24	C	Preview
		MM2716M	115	30	450	+5	24	M	Production
		MM2716E	100	25	450	+5	24	I	Production
		MM2716	100	25	450	+5	24	C	Production
		MM2716-1	100	25	350	+5	24	C	Production
		MM2716-2	100	25	390	+5	24	C	Production
8,192	1,024 × 8	MM2758A	100	25	450	+5	24	C	Production
		MM2758A-1	100	25	350	+5	24	C	Production
		MM2758B	100	25	450	+5	24	C	Production
		MM2758B-1	100	25	350	+5	24	C	Production
		MM2708M	65	65	450	±5, +12	24	M	Production
		MM2708	65	65	450	±5, +12	24	C	Production
		MM2708-1	65	65	350	±5, +12	24	C	Production
4,096	512 × 8	MM4204	52	12	1250	±5, −12	24	M	Production
		MM5204	42	10	1000	+5, −12	24	C	Production
		MM5204-1	42	10	700	±5, −12	24	C	Production
2,048	512 × 4	MM4203	55	55	1000	±5, −12	24	M	Production
		MM5203	55	55	1000	±5, −12	24	C	Production
	256 × 8	MM4203	55	55	1000	±5, −12	24	M	Production
		MM5203	55	55	1000	±5, −12	24	C	Production
		MM1702A	60	60	1000	±5, −9	24	C	Production

*C = 0°C to +70°C
I = −40°C to +85°C
M = −55°C to +125°C

**See Definition of Terms

Bipolar PROM Selection Guide

Size	Organization		Package	Part Number	Maximum Supply Current (mA)	Maximum Access Time (ns)	Temp* Range	Status**
16,384	2k × 8	OC	24	DM77S190	185	100	M	Preliminary
		OC	24	DM87S190	175	80	C	Preliminary
		TS	24	DM77S191	185	100	M	Preliminary
		TS	24	DM87S191	175	80	C	Preliminary
8,192	2k × 4	OC	18	DM77S184	140	75	M	Production
		OC	18	DM87S184	140	60	C	Production
		TS	18	DM77S185	140	75	M	Production
		TS	18	DM87S185	140	60	C	Production
	1k × 8	OC	24	DM77S180	160	90	M	Preliminary
		OC	24	DM87S180	160	70	C	Preliminary
		TS	24	DM77S181	160	90	M	Preliminary
		TS	24	DM87S181	160	70	C	Preliminary
4,096	1k × 4	OC	18	DM54S572	140	75	M	Production
		OC	18	DM74S572	140	60	C	Production
		TS	18	DM54S573	140	75	M	Production
		TS	18	DM74S573	140	60	C	Production
	512 × 8	OC	20	DM54S473	155	75	M	Production
		OC	20	DM74S473	155	60	C	Production
		TS	20	DM54S472	155	75	M	Production
		TS	20	DM74S472	155	60	C	Production
		OC	24	DM54S475	170	75	M	Production
		OC	24	DM74S475	170	65	C	Production
		TS	24	DM54S474	170	75	M	Production
		TS	24	DM74S474	170	65	C	Production
2,048	512 × 4	OC	16	DM54S570	130	65	M	Production
		OC	16	DM74S570	130	55	C	Production
		TS	16	DM54S571	130	65	M	Production
		TS	16	DM74S571	130	55	C	Production
1,024	256 × 4	OC	16	DM54S387	130	60	M	Production
		OC	16	DM74S387	130	50	C	Production
		TS	16	DM54S287	130	60	M	Production
		TS	16	DM74S287	130	50	C	Production
256	32 × 8	OC	16	DM54S188	110	45	M	Production
		OC	16	DM74S188	110	35	C	Production
		TS	16	DM54S288	110	45	M	Production
		TS	16	DM74S288	110	35	C	Production
		OC	16	DM77S188	140	20	M	Preview
		OC	16	DM87S188	140	15	C	Preview
		TS	16	DM77S288	140	20	M	Preview
		TS	16	DM87S288	140	15	C	Preview

*C = 0°C to +70°C
M = −55°C to +125°C

**See Definition of Terms

MOS ROM Selection Guide

Size	Organization	Part No.	Max Supply Current (mA)	Max Access Time (ns)	Supply Voltage (V)	Pkg	Temp* Range	Status**
65,536	8,192 × 8	MM52164	130	450	+5	24	C	Production
		MM52264	50	300	+5	24	C	Preview
32,768	4,096 × 8	MM52132	130	450	+5	24	C	Production
16,384	2,048 × 8	MM52116	100	450	+5	24	C	Production
4,096	1,024 × 4	MM4232	37	1000	+5, −12	24	M	Production
		MM5232	37	1000	+5, −12	24	C	Production
	512 × 8	MM4214	37	1000	+5, −12	24	M	Production
		MM5214	37	1000	+5, −12	24	C	Production
		MM4232	37	1000	+5, −12	24	M	Production
		MM5232	37	1000	+5, −12	24	M	Production
2,048	512 × 4	MM4213	35	850	+5, −12	24	M	Production
		MM5213	35	850	+5, −12	24	C	Production
		MM4230	40	725	±12	24	M	Production
		MM5230	40	725	±12	24	C	Production
		MM4231	30	950	+5, −12	24	M	Production
		MM5231	30	950	+5, −12	24	C	Production
	256 × 8	MM4213	35	850	+5, −12	24	M	Production
		MM5213	35	850	+5, −12	24	C	Production
		MM4230	40	725	±12	24	M	Production
		MM5230	40	725	±12	24	C	Production
		MM4231	30	950	+5, −12	24	M	Production
		MM5231	30	950	+5, −12	24	C	Production
1,024	256 × 4	MM4220	25	650	±12	24	M	Production
		MM5220	25	650	±12	24	C	Production
		MM4221	12	950	+5, −12	24	M	Production
		MM5221	12	950	+5, −12	24	C	Production
	128 × 8	MM4220	25	650	±12	24	M	Production
		MM5220	25	650	±12	24	C	Production
		MM4221	12	950	+5, −12	24	M	Production
		MM5221	12	950	+5, −12	24	C	Production

*C = 0°C to +70°C
M = −55°C to +125°C

**See Definition of Terms

MOS RAM Cross Reference Guide

Size	Org	Pkg	Operation	National	AMD	FSC	Fujitsu	Hitachi	Intel	Mostek	Motorola	NEC	Synertec	TI	Zilog
65,536	65,536 × 1	16	Dynamic	NMC4164					2164	MK4164	MCM4164			TMS4164	
16,384	16,384 × 1	16	Dynamic	NMC5295					2118	MK4516					
		16	Dynamic	MM5290		F16K	MB8116	HM4716	2117	MK4116	MCM4116	μPD416		TMS4116	Z6116
8,192	8,192 × 1	16	Dynamic	MM5298					2109	MK4108					
4,096	4,096 × 1	18	Static	NMC2147	9147		MBM2147	HM4847	2147		MCM2147	μPD2147	SY2147		
		18	Static	NMC2141					2141						
		18	Static	MM5257	4044						MCM6641			TMS4044	
		22	Dynamic	MM5280	9060		MB8107	HM4711	2107		MCM6605	μPD411		TMS4060	
	1,024 × 4	18	Static	NMC2148					2148						
		20	Static	NMC2142A					2142						
		20	Static	NMC2142AP											
		18	Static	NMC2114A					2114A						
		18	Static	NMC2114AP											
		18	Static	MM2114	9114	2114	MD8114	HM2114	2114		MCM2114		SY2114	TMS4045	
1,024	1,024 × 1	16	Static	MM2102A	9102	2102			2102A			μPD2102			

CMOS RAM Cross Reference Guide

Size	Organization	Pkg	National (Present)	National (Previous)	AMI	Harris	Hitachi	Intersil	Intel	NEC	RCA	Synertec	TI	Toshiba
4,096	4,096 × 1	18	NMC6504			6504		IM6504						54104
	1,024 × 4	18	NMC6514			6514		IM6514			5114			5047
2,048	2,048 × 1	18	NMC6503			6503								
	512 × 4	18	NMC6513			6513								
1,024	1,024 × 1	16	NMC6508	74C929	56508	6508		IM6508		6508	5001	5102	6508	5508
		18	NMC6518	74C930		6518		IM6518						
	256 × 4	16				6562						5112		
		18	NMC6552	74C921										
		18				6561		IM6561				5111		
		22	NMC6551	74C920		6551		IM6551						
		22			55101	6501	35101		5101	5101	5040	5101	5101	5501

MOS EPROM Cross Reference Guide

Size	Org	Pkg.	National	AMD	Fairchild	Fujitsu	Hitachi	Intel	Mostek	Motorola	NEC	Synertec	TI
65,536	8,192 × 8	28	NMC2564										2564
32,768	4,096 × 8	24	NMC2532										2532
		24	NMC2732					2732					
16,384	2,048 × 8	24	MM2716	2716	2716	MBM2716	HN42716	2716	MK2716	MCM2716	μPD2716	SY2716	TMS2516
8,192	1,024 × 8	24	MM2758					2758					
		24	MM2708	2708	2708	MBM8518	HN462708	2708		MCM2708			TMS2708
4,096	512 × 8	24	MM5204										
2,048	512 × 4	24	MM5203										
	256 × 8	24	MM5203										
			MM1702A					1702A					

Bipolar PROM Cross-Reference Guide

Size	Org		Pkg	National	AMD	Fairchild	Harris	Intel	Intersil	MMI	Signetics	TI	Fujitsu
16,384	2k × 8	OC	24	DM87S190			HM-76160-5				N82S190		
		TS	24	DM87S191			HM-76161-5	3636			N82S191		MB7138
8,192	2k × 4	OC	18	DM87S184			HM-7684-5				N82S184		
		TS	18	DM87S185			HM-7685-5				N82S185		MB7128
	1k × 8	OC	24	DM87S180		93450	HM-7680-5	3608		6380-1	N82S180	SN74S479	
		TS	24	DM87S181		93451	HM-7681-5	3628		6381-1	N82S181	SN74S478	MB7032
4,096	1k × 4	OC	18	DM74S572	AM27S32	93452	HM-7642-5	3605	IM5606C	6352-1	N82S136	SN74S477	
		TS	18	DM74S573	AM27S33	93453	HM-7643-5	3625	IM5626C	6353-1	N82S137	SN74S476	MB7122
	512 × 8	OC	20	DM74S473	AM27S28					6348-1	N82S146	SN74S473	
		TS	20	DM74S472	AM27S29					6349-1	N82S147	SN74S472	
		OC	24	DM74S475	AM27S30	93438	HM-7640-5	3604A	IM5605C	6340-1	N82S140	SN74S475	
		TS	24	DM74S474	AM27S31	93448	HM-7641-5	3624A	IM5625C	6341-1	N82S141	SN74S474	
2,048	512 × 4	OC	16	DM74S570	AM27S12	93436	HM-7620-5	3602	IM5604C	6305-1	N82S130		MB7058
		TS	16	DM74S571	AM27S13	93446	HM-7621-5	3622	IM5624C	6306-1	N82S131		MB7053
1,024	256 × 4	OC	16	DM74S387	AM27S20	93417	HM-7610-5	3601	IM5603AC	6300-1	N82S126	SN74S387	MB7057
		TS	16	DM74S287	AM27S21	93427	HM-7611-5	3621	IM5623C	6301-1	N82S129	SN74S287	MB7052
256	32 × 8	OC	16	DM74S188	AM27S18		HM-7602-5		IM5600C	6330-1	N82S23	SN74S188	MB7056
		TS	16	DM74S288	AM27S19		HM-7603-5		IM5610C	6331-1	N82S123	SN74S288	MB7051
		OC	16	DM87S188									
		TS	16	DM87S288									

Section 1

NMOS RAMs

1

NMOS static and dynamic read/write memory devices constitute the majority of semiconductor memory worldwide consumption. National plays a leadership role in this area as a major supplier of products included in this section. In addition to the devices included here, National is developing more advanced higher density, high speed RAMs for future equipment designs. Contact your local National representative for further assistance.

Static RAMs

National Semiconductor

NMOS RAMs

MM2102A, MM2102AL Family 1024-Bit (1024 x 1) Static RAMs

General Description

The MM2102A family of high speed 1024 x 1-bit static random access read/write memories is manufactured using N-channel depletion-mode silicon gate technology. Static storage cells eliminate the need for clocks or refresh circuitry and the resultant cost associated with them.

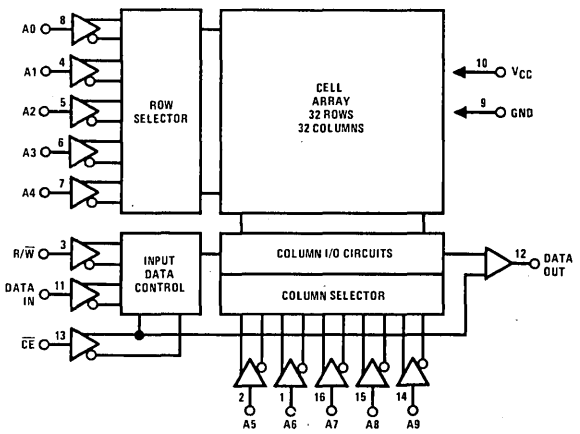
Low threshold silicon gate N-channel technology allows complete DTL/TTL compatibility of all inputs and outputs as well as a single 5V supply. The separate chip enable input ($\overline{CE}$) controlling the TRI-STATE® output allows easy memory expansion by OR-tying individual devices to a data bus. Data in and data out have the same polarity.

In addition to the MM2102A, a low power version, the MM2102AL, is also available. This selection offers a maximum operating current of 33 mA and a guaranteed standby mode down to a power supply voltage of 1.5V.

Features

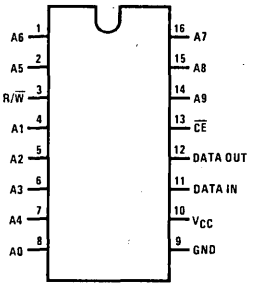
- Single 5V supply
- All inputs and outputs directly DTL/TTL compatible
- Static operation—no clocks or refresh
- TRI-STATE output for bus interface
- All inputs protected against static charge
- Access time down to 250 ns

Block Diagram



Connection Diagram

Dual-In-Line Package



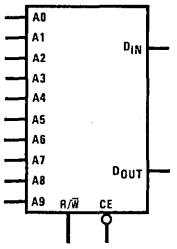
TOP VIEW

Order Number:	Order Number:
MM2102AJ-2L	MM2102AN-2L
MM2102AJ-2	MM2102AN-2
MM2102AJ-L	MM2102AN-L
MM2102AJ	MM2102AN
MM2102AJ-4L	MM2102AN-4L
MM2102AJ-4	MM2102AN-4
MM2102AJ-6L	MM2102AN-6L
MM2102AJ-6	MM2102AN-6
See NS Package J16A	See NS Package N16A

Truth Table

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	Hi-Z	Not selected
L	L	L	L	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{OUT}	Read

Logic Symbol



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.5V to +7V
Storage Temperature	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C
Input Low Voltage	−0.5	0.8	V
Input High Voltage	2.0	V_{CC}	V

DC Electrical Characteristics

T_A = 0°C to +70°C, V_{CC} = ±5%, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MM2102A, MM2102A-2, MM2102A-4, MM2102A-6		MM2102A-L, MM2102A-2L, MM2102A-4L, MM2102A-6L		UNITS
			MIN	MAX	MIN	MAX	
I_{LI}	Input Load Current	V_{IN} = 0 to 5.25V		10		10	μA
I_{LOH}	Output Leakage Current	$\overline{CE}$ = 2V, V_{OUT} = 2.4V		5		5	μA
I_{LOL}	Output Leakage Current	$\overline{CE}$ = 2V, V_{OUT} = 0.4V		−10		−10	μA
I_{CC}	Power Supply Current	All Inputs = 5.25V, Data Output Open, T_A = 25°C		45		31	mA
I_{CC}	Power Supply Current	All Inputs = 5.25V, Data Output Open, T_A = 0°C		50		33	mA
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −200 μA	2.4		2.4		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the device may be permanently damaged. They do not mean the device may be operated at these values.

AC Electrical Characteristics

(With standard load) T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified.

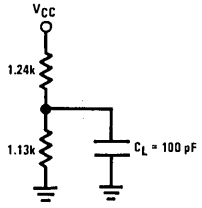
SYMBOL	PARAMETER	MM2102A-2, MM2102A-2L		MM2102A, MM2102A-L		MM2102A-4, MM2102A-4L		MM2102A-6, MM2102A-6L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE *(Figure 1)*										
t_{RC}	Read Cycle	250		350		450		650		ns
t_A	Access Time		250		350		450		650	ns
t_{CO}	Chip Enable to Output Time		100		150		200		200	ns
t_{OH1}	Previous Read Data Valid with Respect to Address	40		40		40		50		ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0		0		0		ns
WRITE CYCLE *(Figure 2)*										
t_{WC}	Write Cycle	250		350		450		650		ns
t_{AW}	Address to Write Set-Up	20		20		20		20		ns
t_{WP}	Write Pulse Width	100		150		200		200		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{DW}	Date Set-Up Time	85		125		175		175		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{CW}	Chip Enable To Write Set-Up	100		150		200		200		ns

AC Electrical Characteristics $T_A = 25°C$, f = 1 MHz

SYMBOL	PARAMETER	LIMIT (pF)	
		TYP	MAX
CAPACITANCE [2]			
C_{IN}	Input Capacitance (All Inputs V_{IN} = 0V)	3	5
C_{OUT}	Output Capacitance, V_O = 0V	4	6

Note 2: This parameter is guaranteed by periodic testing

AC Test Circuit



Switching Time Waveforms

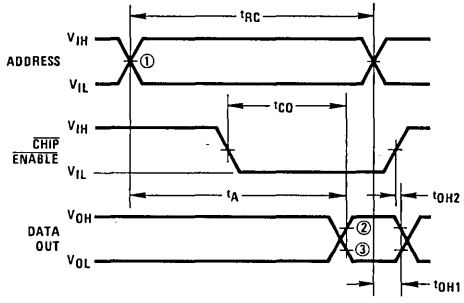


FIGURE 1. Read Cycle

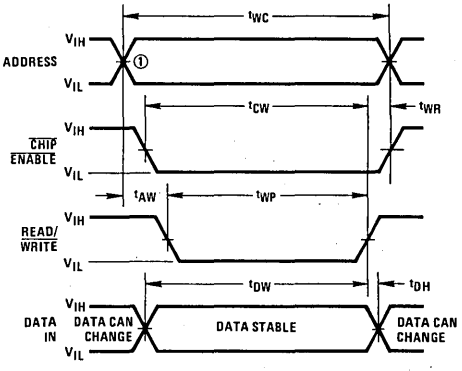


FIGURE 2. Write Cycle

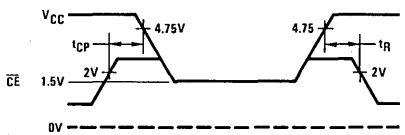
Note ①: Input reference level for timing is 1.5V.
Note ②: V_{OH} = 2V is reference level for output high.
Note ③: V_{OL} = 0.8V is reference level for output low.
Note ④: Input rise and fall times are 10 ns.

Standby Characteristics $T_A = 0°C$ to $+70°C$

SYMBOL	PARAMETER	CONDITIONS	MM2102A, MM2102A-2, MM2102A-4, MM2102-6			MM2102A-L, MM2102A-2L, MM2102A-4L, MM2102A-6L			UNITS
			MIN	TYP(3)	MAX	MIN	TYP(3)	MAX	
V_{PD}	V_{CC} in Standby		1.5			1.5			V
V_{CES}	$\overline{CE}$ Bias in Standby	$2 \leq V_{PD} \leq V_{CCMAX}$	2.0			2.0			V
V_{CES}	$\overline{CE}$ Bias in Stand-by	$1.5 \leq V_{PD} \leq 2$	V_{PD}			V_{PD}			V
I_{PD1}	Standby Current	All Inputs = V_{PD} = 1.5V			28			23	mA
I_{PD2}	Standby Current	All Inputs = V_{PD} = 2V			38			28	mA
t_{CP}	Chip Deselect to Standby Time		0			0			ns
t_R	Recovery Time (Note 4)		t_{RC}			t_{RC}			ns

Note 3: Typical values at $T_A = 25°C$.
Note 4: $t_R = t_{RC}$ = read cycle time.

Standby Waveforms



National Semiconductor

MM2114, MM2114L Family 4096-Bit (1024 x 4) Static RAMs

General Description

The MM2114 family of 1024-word by 4-bit static random access memories is fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

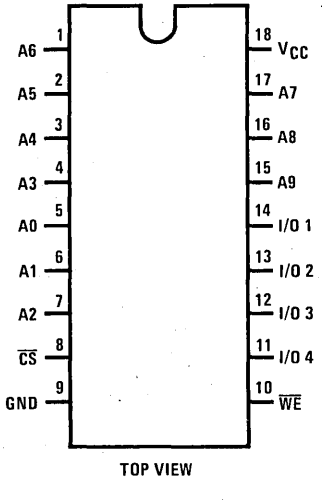
The separate chip select input ($\overline{CS}$) allows easy memory expansion by OR-tying individual devices to a data bus.

Features

- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Low power—225 mW typical
- High speed—down to 200 ns access time
- TRI-STATE® output for bus interface
- Common Data In and Data Out pins
- Single 5V supply
- Standard 18-pin dual-in-line package

Connection Diagram

Dual-In-Line Package

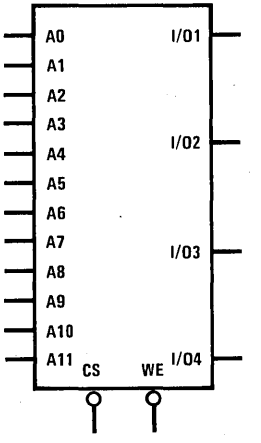


TOP VIEW

Order Number MM2114J-25L, MM2114J-25, MM2114J-2L, MM2114J-2, MM2114J, MM2114J-L, MM2114J-3L or MM2114J-3
See NS Package J18A

Order Number MM2114N-2L, MM2114N-2, MM2114N, MM2114N-L, MM2114N-3L or MM2114N-3
See NS Package N18A

Logic Symbol



Truth Table

$\overline{CS}$	$\overline{WE}$	I/O	MODE
H	X	Hi-Z	Not Selected
L	L	H	Write 1
L	L	L	Write 0
L	H	D_{OUT}	Read

Functional Description

Two pins control the operation of the MM2114. Chip Select ($\overline{CS}$) enables write and read operations and controls TRI-STATING of the data-output buffer. Write Enable ($\overline{WE}$) chooses between READ and WRITE modes and also controls output TRI-STATING. The truth table details the states produced by combinations of the $\overline{CS}$ and $\overline{WE}$ controls.

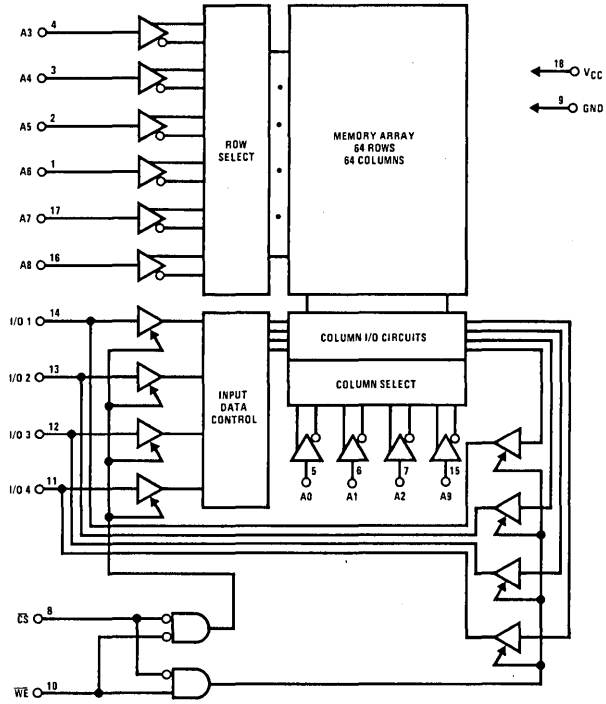
READ-cycle timing is shown in the section on Switching Time Waveforms. $\overline{WE}$ is kept high. Independent of $\overline{CS}$, any change in address code causes new data to be fetched and brought to the output buffer. $\overline{CS}$ must be low, however, for the output buffer to be enabled and transfer the data to the output pin.

Address access time, t_A, is the time required for an address change to produce new data at the output pin, assuming $\overline{CS}$ has enabled the output buffer prior to data arrival. Chip Select-to-output delay, t_{CO}, is the time required for $\overline{CS}$ to enable the output buffer and transfer previously fetched data to the output pin. Operation with $\overline{CS}$ continuously held low is permissible.

WRITE-cycle timing is shown in the section on Switching Time Waveforms. Writing occurs only during the time both $\overline{CS}$ and $\overline{WE}$ are low. Minimum write pulse width, t_{WP}, refers to this simultaneous low region. Data set-up and hold times are measured with respect to whichever control first rises. Successive write operations may be performed with $\overline{CS}$ continuously held low. $\overline{WE}$ then is used to terminate WRITE between address changes. Alternatively, $\overline{WE}$ may be held low for successive WRITES and $\overline{CS}$ used for WRITE interruption between address change.

In any event, either $\overline{WE}$ or $\overline{CS}$ (or both) must be high during address transitions to prevent erroneous WRITE.

Block Diagram



Absolute Maximum Ratings

Voltage at Any Pin	−0.5V to +7V
Storage Temperature	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C

DC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MM2114 MM2114-2 MM2114-25 MM2114-3		MM2114-L MM2114-2L MM2114-25L MM2114-3L		UNITS
			MIN	MAX	MIN	MAX	
V_{IH}	Logical "1" Input Voltage		2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Logical "0" Input Voltage		−0.5	0.8	−0.5	0.8	V
V_{OH}	Logical "1" Output Voltage	$I_{OH} = -1.0$ mA	2.4		2.4		V
V_{OL}	Logical "0" Output Voltage	$I_{OL} = 2.1$ mA		0.4		0.4	V
I_{LI}	Input Load Current	$V_{IN} = 0$ to 5.25V	−10	10	−10	10	μA
I_{LO}	Output Leakage Current	$V_O = 4V$ to 0.4V, $\overline{CS} = V_{IH}$	−10	10	−10	10	μA
I_{CC1}	Power Supply Current	All Inputs = 5.25V, $T_A = 25°C$		95		65	mA
I_{CC2}	Power Supply Current	All Inputs = 5.25V, $T_A = 0°C$		100		70	mA

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, (Note 2)

SYMBOL	PARAMETER	MM2114-2 MM2114-2L		MM2114-25 MM2114-25L		MM2114-3 MM2114-3L		MM2114 MM2114-L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE										
t_{RC}	Read Cycle Time ($\overline{WE} = V_{IH}$)	200		250		300		450		ns
t_A	Access Time		200		250		300		450	ns
t_{CO}	Chip Select to Output Valid		70		90		100		120	ns
t_{CX}	Chip Select to Output Active	20		20		20		20		ns
t_{COT}	Chip Select to Output TRI-STATE	0	40	0	60	0	80	0	100	ns
t_{OHA}	Output Hold from Address Change	10		10		10		10		ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	200		250		300		450		ns
t_{WP}	Write Pulse Width	100		125		150		200		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{DS}	Data Set-Up Time	100		125		150		200		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{WOT}	Write Enable to Output TRI-STATE	0	40	0	60	0	80	0	100	ns
t_{WO}	Write Enable to Output Valid		80		90		100		120	ns

Capacitance $T_A = 25°C$, f = 1 MHz, (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MM2114 MM2114-2 MM2114-25 MM2114-3		MM2114-L MM2114-2L MM2114-25L MM2114-3L		UNITS
			MIN	MAX	MIN	MAX	
C_{IN}	Input Capacitance	All Inputs $V_{IN} = 0V$		5		5	pF
C_{OUT}	Output Capacitance	$V_O = 0V$		10		10	pF

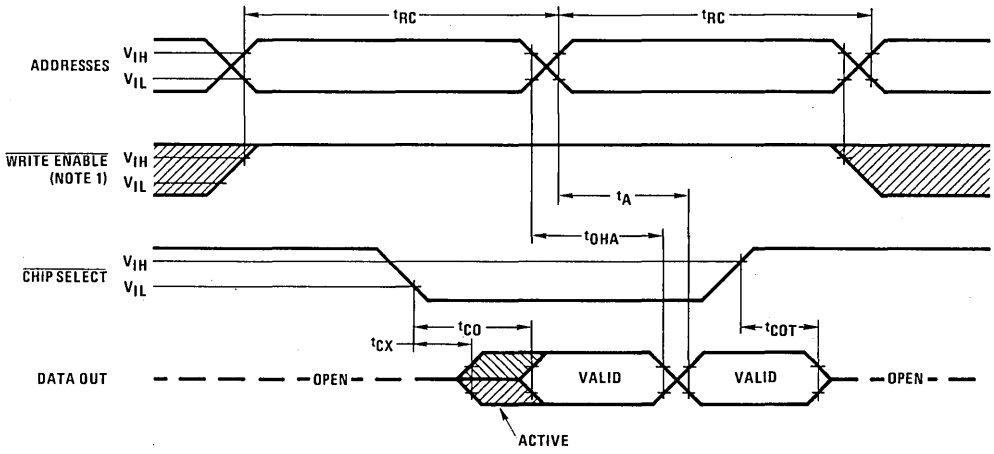
Note 1: Typical values at $T_A = 25°C$.

Note 2: All input transitions ≤ 10 ns. Timing referenced to $V_{IL(MAX)}$ or $V_{IH(MIN)}$ for inputs, 0.8V and 2V for output. For test purposes, input levels should swing between 0V and 3V. Output load = 1 TTL gate and $C_L = 100$ pF.

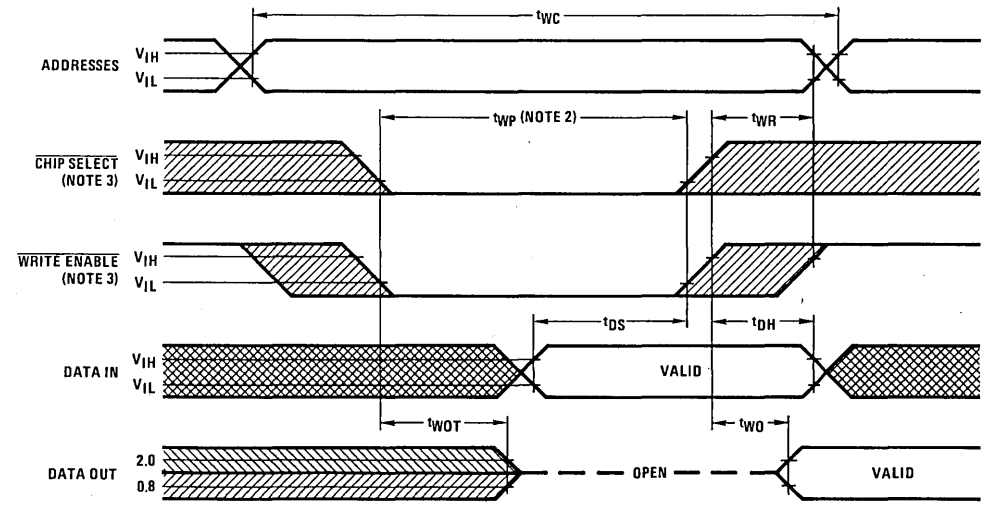
Note 3: This parameter is guaranteed by periodic testing.

Switching Time Waveforms

Read Cycle



Write Cycle



Note 1: $\overline{WE}$ is high during a read cycle ($\overline{WE} \geq V_{IH(MIN)}$).

Note 2: t_{WP} defines the period when both $\overline{CS}$ and $\overline{WE}$ are low. t_{AW} is referenced to the later of $\overline{CS}$ or $\overline{WE}$ going low while t_{DS}, t_{DH} and t_{WR} are referenced to the earlier of $\overline{CS}$ or $\overline{WE}$ going high. t_{WOT} and t_{WO} are referenced to $\overline{WE}$ with $\overline{CS}$ low.

Note 3: Either $\overline{WE}$ or $\overline{CS}$ (or both) must be high during address transitions to prevent erroneous write.

National Semiconductor

NMOS RAMs

MM2147/MM2147L Family 4096 x 1 Static RAMs

General Description

The MM2147 is a 4096-word by 1-bit static random access memory fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data.

The separate chip select input automatically switches the part to its low power standby mode.

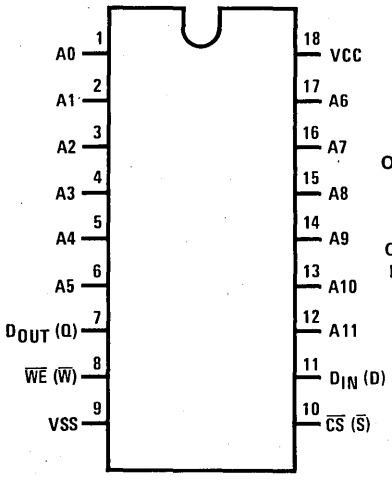
The output is held in a high impedance state during write to simplify common I/O applications.

Features

- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Automatic power down
- High speed— down to 55 ns access time
- TRI-STATE® output for bus interface
- Separate Data In and Data Out pins
- Single +5V supply
- Standard 18-pin dual-in-line package

Connection Diagram*

Dual-In-Line Package

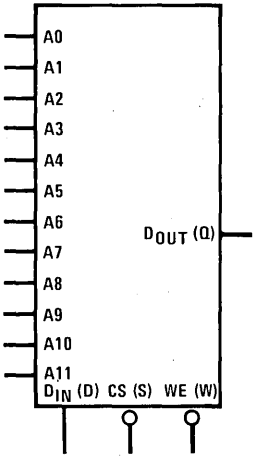


TOP VIEW

Order Number MM2147N-3, MM2147N, MM2147N-L or MM2147N-1L
See NS Package N18A

Order Number MM2147J-3, MM2147J, MM2147J-L or MM2147J-1L
See NS Package J18A

Logic Symbol*



Pin Names*

A0–A11	Address Inputs
$\overline{WE}$ ($\overline{W}$)	Write Enable
$\overline{CS}$ ($\overline{S}$)	Chip Select
D_{IN} (D)	Data In
D_{OUT} (Q)	Data Out
VCC	Power (+5V)
VSS	Ground

Truth Table*

$\overline{CS}$ ($\overline{S}$)	$\overline{WE}$ ($\overline{W}$)	D_{IN} (D)	D_{OUT} (Q)	MODE	POWER
H	X	X	Hi-Z	Not Selected	Standby
L	L	H	Hi-Z	Write 1	Active
L	L	L	Hi-Z	Write 0	Active
L	H	X	D_{OUT}	Read	Active

* The symbols in parentheses are proposed industry standard.

Functional Description

Two pins control the operation of the MM2147. Chip select enables write and read operations, deselects the device putting it in the low power standby mode, and controls TRI-STATING of the data-output buffer. Write enable chooses between READ and WRITE modes and also controls output TRI-STATING. The truth table details the states produced by combinations of the controls.

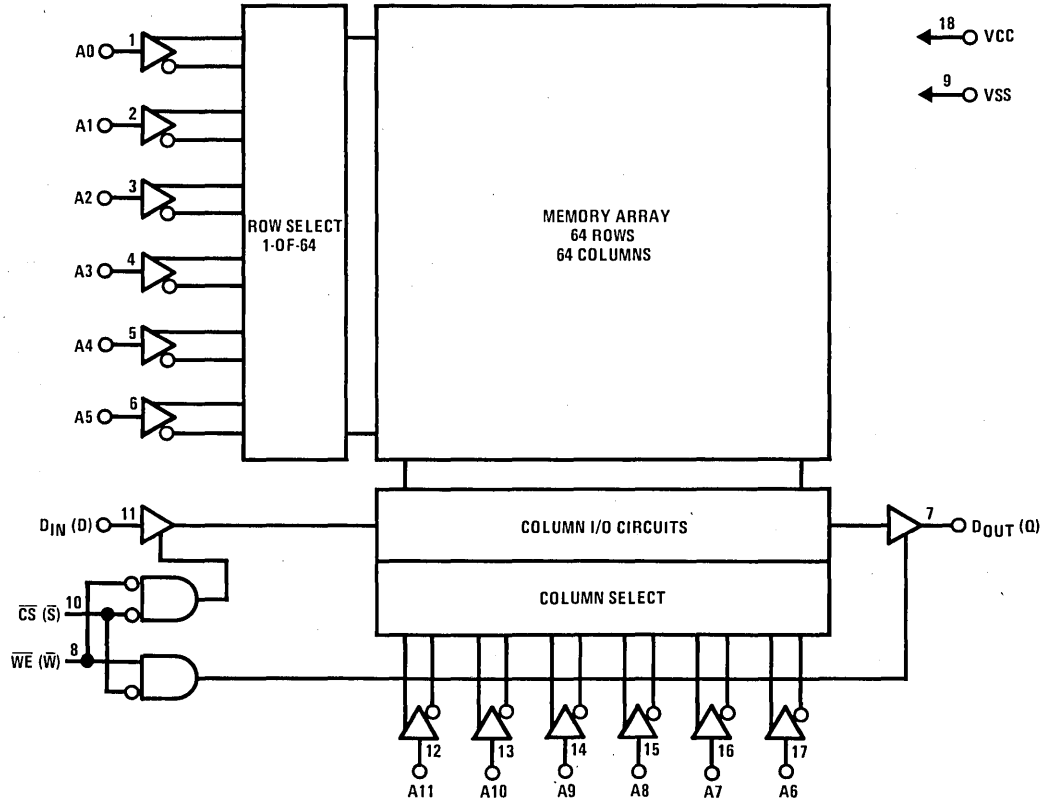
READ-cycle timing is shown in the section on Switching Time Waveforms. Write enable is kept high. Independent of chip select any change in address code causes new data to be fetched and brought to the output buffer. Chip select must be low, however, for the output buffer to be enabled and transfer the data to the output pin.

Address access time is the time required for an address change to produce new data at the output pin, assuming chip select has enabled the output buffer prior to data arrival. Chip select access time is the time required for chip select to enable the output buffer and transfer previously fetched data to the output pin. Operation with chip select continuously held low is permissible.

WRITE-cycle timing is shown in the section on Switching Time Waveforms. Writing occurs only during the time both chip select and write enable are low. Minimum write pulse width refers to this simultaneous low region. Data set-up and hold times are measured with respect to whichever control first rises. Successive write operations may be performed with chip select continuously held low. Write enable then is used to terminate WRITE between address changes. Alternatively, write enable may be held low for successive WRITES and chip select used for write interruption between address change. In any event, either write enable or chip select (or both) must be high during address transitions to prevent erroneous WRITE.

Standby operation allows data to be maintained with approximately 85% less current. The device automatically switches to the low power standby mode whenever it is deselected.

Block Diagram *



* The symbols in parentheses are proposed industry standard.

Absolute Maximum Ratings

Voltage on any Pin Relative to VSS	−1.5V to +7V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1.2W
DC Output Current	20 mA
Bias Temperature Range	−10°C to +85°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (VCC)	4.5	5.5	V
Ambient Temperature (TA)	0	+70	°C

DC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ±10% (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MM2147-3		MM2147		MM2147L MM2147L-1		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
VIH	Logical "1" Input Voltage		2.0	6.0	2.0	6.0	2.0	6.0	V
VIL	Logical "0" Input Voltage		−1.0	0.8	−1.0	0.8	−1.0	0.8	V
VOH	Logical "1" Output Voltage	IOH = −4.0 mA	2.4		2.4		2.4		V
VOL	Logical "0" Output Voltage	IOL = 8.0 mA		0.4		0.4		0.4	V
ILI	Input Load Current	VIN = 0 to 5.25V, VCC = Max		10		10		10	μA
|ILO|	Output Leakage Current	VO = 4.5V to Gnd, $\overline{CS}$ = VIH, VCC = Max		50		50		50	μA
ICC1	Power Supply Current	VCC = Max, $\overline{CS}$ = VIL, Outputs Open, TA = 25°C		170		150		135	mA
ICC2	Power Supply Current	VCC = Max, $\overline{CS}$ = VIL, Outputs Open, TA = 0°C		180		160		140	mA
ISB	Standby Current	VCC = Min to Max, $\overline{CS}$ = VIH		30		20		10	mA
IPO	Peak Power ON Current (Note 2)	VCC = Gnd to VCC Min, $\overline{CS}$ = Lower of VCC or VIH (MIN)		70		50		30	mA

Capacitance TA = 25°C, f = 1 MHz (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
CIN	Input Capacitance	All Inputs VIN = 0V		5	pF
COUT	Output Capacitance	VO = 0V		6	pF

AC Test Conditions (Note 4)

Input Pulse Levels	Gnd to 3.5V
Input Rise and Fall Times	≤ 10 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See *Figure 1*

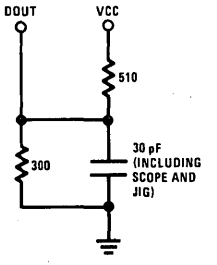


FIGURE 1. Output Load

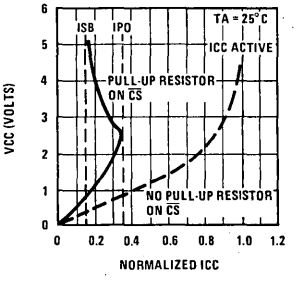


FIGURE 2. Power On Current

Note 1: Guaranteed with transverse air flow greater than 400 linear feet per minute.

Note 2: A pull-up resistor to VCC on the chip select input is required to keep the device deselected or power on current approaches ICC active (see *Figure 2*).

Note 3: This parameter is guaranteed by periodic testing.

Note 4: This device requires a 500 ns time delay after VCC reaches the specified minimum limit to ensure proper operation after power on. This allows the internally generated substrate bias to reach its functional level.

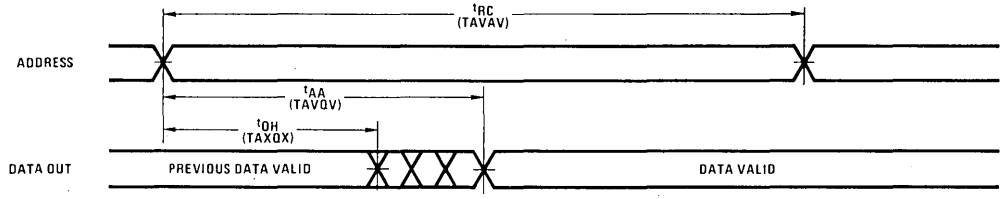
Read Cycle AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$

SYMBOL		PARAMETER	MM2147-3		MM2147, MM2147L		MM2147L-1		UNITS
ALTERNATE	STANDARD		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	TAVAV	Read Cycle Time	55		70		90		ns
t_{AA}	TAVQV	Address Access Time		55		70		90	ns
t_{ASC1}	TSLQV1	Chip Select Access Time (Note 5)		55		70		90	ns
t_{ASC2}	TSLQV2	Chip Select Access Time (Note 6)		65		80		105	ns
t_{OH}	TAXQX	Output Hold from Address Change	5		5		5		ns
t_{LZ}	TSLQX	Chip Selection to Output Active	10		10		10		ns
t_{HZ}	TSHQZ	Chip Deselection to Output TRI STATE	0	40	0	40	0	50	ns
t_{PU}	TSLICCH	Chip Selection to Power Up	0		0		0		ns
t_{PD}	TSLICCL	Chip Deselection to Power Down		30		30		35	ns

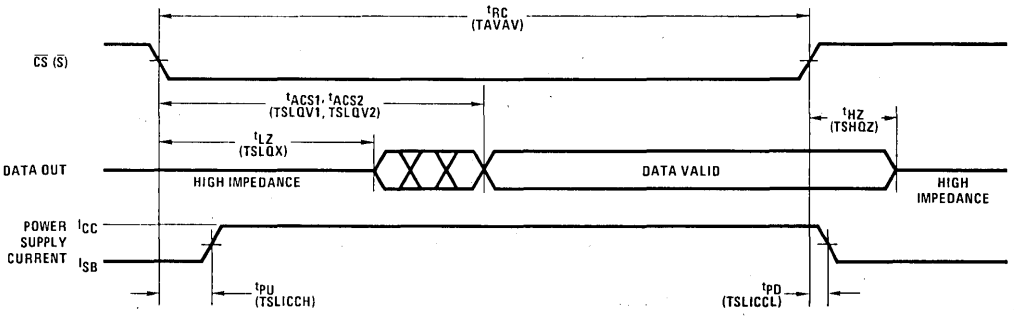
Note 5: Chip deselected for greater than 55 ns prior to selection.
Note 6: Chip deselected for a finite time that is less than 55 ns prior to selection.

Read Cycle Waveforms*

Read Cycle No. 1 (Continuously Selected)



Read Cycle No. 2 (Chip Select Switched)



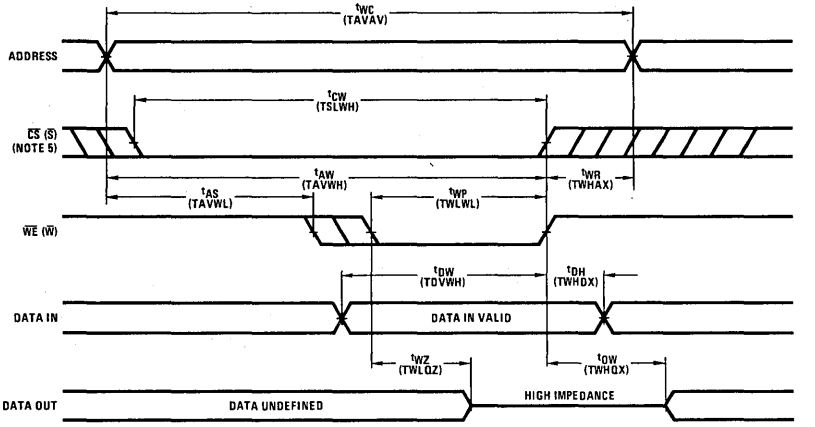
* The symbols in parentheses are proposed industry standard.

Write Cycle AC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ±10%

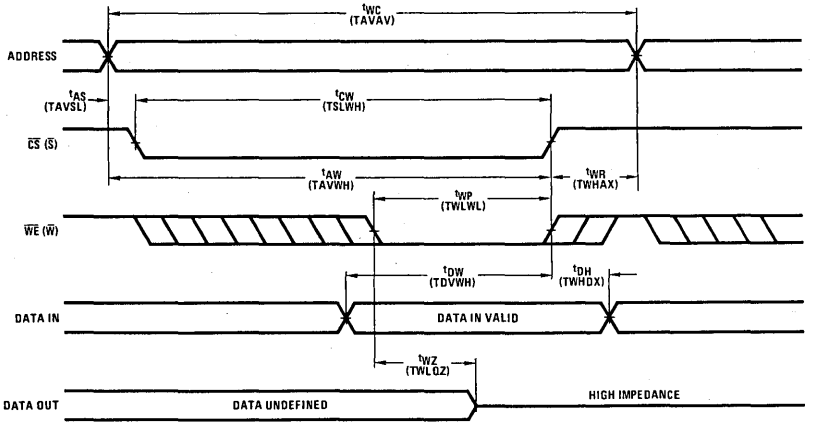
SYMBOL		PARAMETER	MM2147-3		MM2147, MM2147L		MM2147L-1		UNITS
ALTERNATE	STANDARD		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	TAVAV	Write Cycle Time	55		70		90		ns
t_{CW}	TSLWH	Chip Selection to End of Write	45		55		60		ns
t_{AW}	TAVWH	Address Valid to End of Write	45		55		60		ns
t_{AS}	TAVWL TAVSL	Address Setup Time	0		0		0		ns
t_{WP}	TWLWL	Write Pulse Width	35		40		60		ns
t_{WR}	TWHAX	Write Recovery Time	10		15		20		ns
t_{DW}	TDVWH	Data Valid to End of Write	25		30		35		ns
t_{DH}	TWHDX	Data Hold Time	10		10		10		ns
t_{WZ}	TWLQZ	Write Enabled to Output in Hi-Z	0	30	0	35	0	40	ns
t_{DW}	TWHQX	Output Active from End of Write	0		0		0		ns

Write Cycle Waveforms* (Note 7)

Write Cycle No. 1 ($\overline{WE}$ Controlled)



Write Cycle No. 2 ($\overline{CS}$ Controlled)



Note 7: A write occurs during the coincidental low of $\overline{CS}$ and $\overline{WE}$. The output remains TRI-STATE® if $\overline{CS}$ and $\overline{WE}$ go high simultaneously. $\overline{WE}$ or $\overline{CS}$ or both must be high during address transitions.

* The symbols in parentheses are proposed industry standard.

National Semiconductor

MM5257, MM5257L Family
4096-Bit (4096 x 1) Static RAMs

General Description

The MM5257 family of 4096-word by 1-bit static random access memories is fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data.

The separate chip enable input ($\overline{CE}$) controlling the TRI-STATE® output allows easy memory expansion by OR-tying individual devices to a data bus.

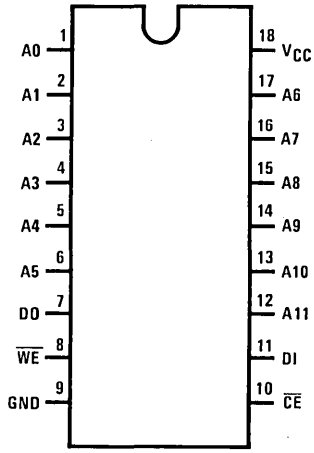
The output is held in a high impedance state during write to simplify common I/O applications.

Features

- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Low power—225 mW typical
- High speed—down to 200 ns access time
- TRI-STATE output for bus interface
- Separate Data In and Data Out pins
- Single +5V supply
- Standard 18-pin dual-in-line package

Connection Diagram

Dual-In-Line Package

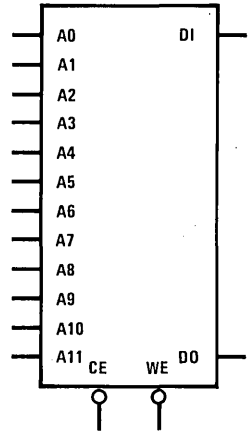


TOP VIEW

Order Number MM5257J, J-2, J-25, J-3, J-L, J-2L, J-25L or J-3L
See NS Package J18A

Order Number MM5257N, N-2, N-25, N-3, N-L, N-2L, N-25L, or N-3L
See NS Package N18A

Logic Symbol



Truth Table

$\overline{CE}$	$\overline{WE}$	DI	D_{OUT}	MODE
H	X	X	Hi-Z	Not Selected
L	L	H	Hi-Z	Write 1
L	L	L	Hi-Z	Write 0
L	H	X	D_{OUT}	Read

Functional Description

Two pins control the operation of the MM5257. Chip Enable ($\overline{CE}$) enables write and read operations and controls TRI-STATING of the data-output buffer. Write Enable ($\overline{WE}$) chooses between READ and WRITE modes and also controls output TRI-STATING. The truth table details the states produced by combinations of the $\overline{CE}$ and $\overline{WE}$ controls.

READ-cycle timing is shown in the section on Switching Time Waveforms. $\overline{WE}$ is kept high. Independent of $\overline{CE}$, any change in address code causes new data to be fetched and brought to the output buffer. $\overline{CE}$ must be low, however, for the output buffer to be enabled and transfer the data to the output pin.

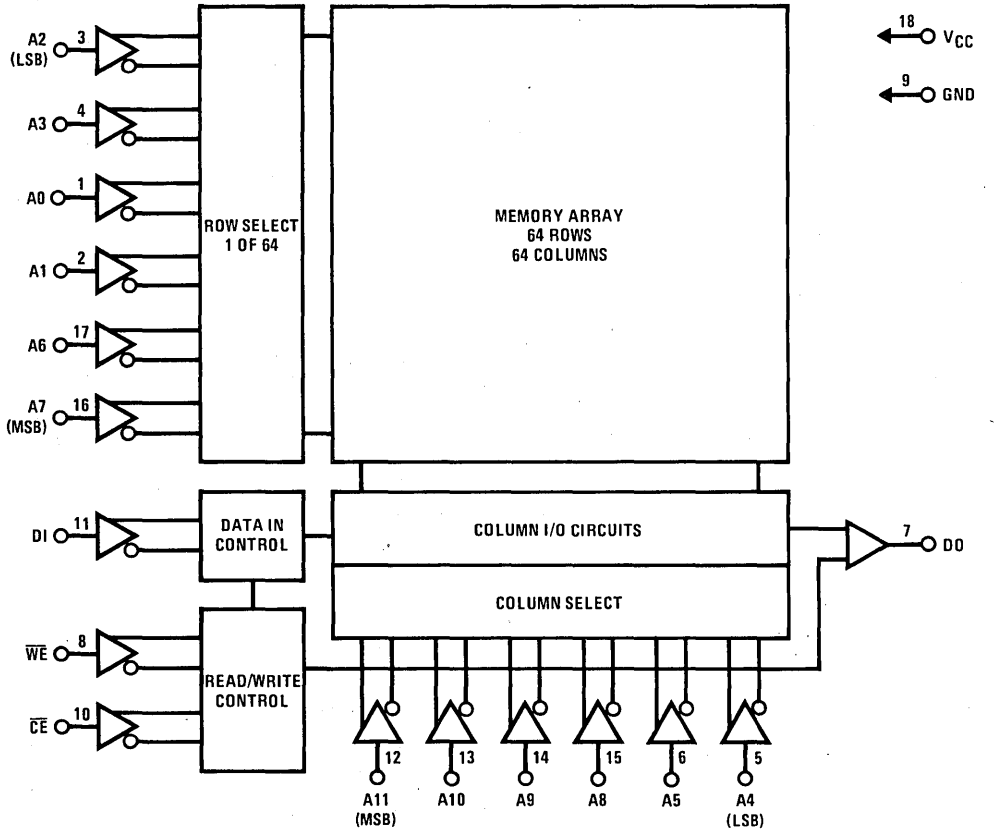
Address access time, t_A, is the time required for an address change to produce new data at the output pin, assuming $\overline{CE}$ has enabled the output buffer prior to data arrival. Chip Enable-to-output delay, t_{CO}, is the time required for $\overline{CE}$ to enable the output buffer and transfer previously fetched data to the output pin. Operation with $\overline{CE}$ continuously held low is permissible.

WRITE-cycle timing is shown in the section on Switching Time Waveforms. Writing occurs only during the time both $\overline{CE}$ and $\overline{WE}$ are low. Minimum write-pulse width, t_{WP}, refers to this simultaneous low region. Data set-up and hold times are measured with respect to whichever control first rises. Successive write operations may be performed with $\overline{CE}$ continuously held low. $\overline{WE}$ then is used to terminate WRITE between address changes. Alternatively, $\overline{WE}$ may be held low for successive WRITES and $\overline{CE}$ used for WRITE interruption between address change.

In any event, either $\overline{WE}$ or $\overline{CE}$ (or both) must be high during address transitions to prevent erroneous WRITE.

Stand-by operation allows data to be maintained with approximately 50% less operating current. The 2 requirements to guarantee data retention are: a) the power supply voltage must meet the condition $V_{CC} \geq 1.5V$, and b) $\overline{CE}$ must be controlled; to disable the chip prior to reducing V_{CC}, to keep it disabled during the time V_{CC} is reduced, and to maintain the disabled state long enough after V_{CC} is increased to normal for the chip to recover. These requirements are shown by the stand-by waveforms and characteristics.

Block Diagram



Absolute Maximum Ratings

Voltage on Any Pin Relative to V_{SS}	−0.3V to +7V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Short-Circuit Output Current	50 mA
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C

DC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MM5257 MM5257-2 MM5257-25 MM5257-3		MM5257-L MM5257-2L MM5257-25L MM5257-3L		UNITS
			MIN	MAX	MIN	MAX	
V_{IH}	Logical "1" Input Voltage		2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Logical "0" Input Voltage		−0.5	0.8	−0.5	0.8	V
V_{OH}	Logical "1" Output Voltage	$I_{OH} = -200\ \mu A$	2.4		2.4		V
V_{OL}	Logical "0" Output Voltage	$I_{OL} = 2.1$ mA		0.4		0.4	V
I_{LI}	Input Load Current	$V_{IN} = 0$ to 5.25V	−10	10	−10	10	μA
I_{LO}	Output Leakage Current	$V_O = 4V$ to 0.4V, $\overline{CE} = V_{IH}$	−10	10	−10	10	μA
I_{CC}	Power Supply Current	All Inputs = 5.25V, $T_A = 25°C$		80		55	mA
I_{CC}	Power Supply Current	All Inputs = 5.25V, $T_A = 0°C$		90		65	mA

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, (Note 2)

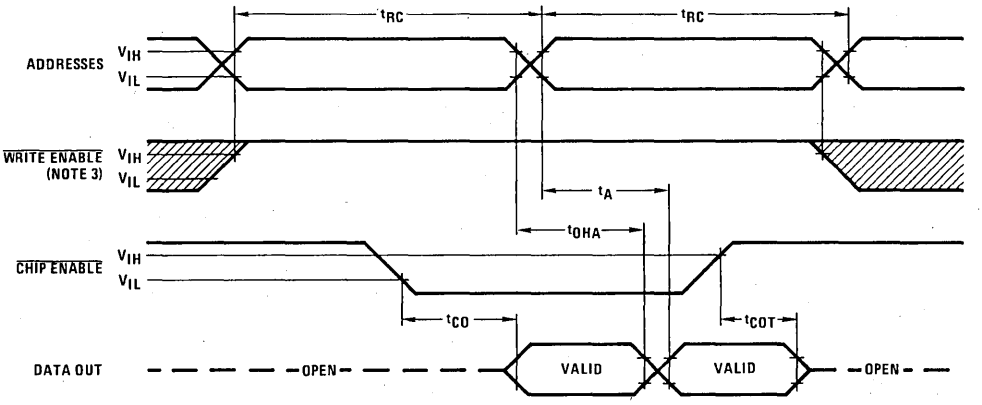
SYMBOL	PARAMETER	MM5257-2 MM5257-2L		MM5257-25 MM5257-25L		MM5257-3 MM5257-3L		MM5257 MM5257-L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE										
t_{RC}	Read Cycle Time ($\overline{WE} = V_{IH}$)	200		250		300		450		ns
t_A	Access Time		200		250		300		450	ns
t_{CO}	Chip Enable to Output Valid		80		100		150		200	ns
t_{COT}	Chip Enable to Output TRI-STATE	0	60	0	70	0	80	0	100	ns
t_{OHA}	Output Hold from Address Change	30		30		30		30		ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	200		250		300		450		ns
t_{WP}	Write Pulse Width	100		100		150		200		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{DS}	Data Set-Up Time	85		85		120		175		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{WOT}	Write Enable to Output TRI-STATE	0	80	0	80	0	100	0	120	ns
t_{WO}	Write Enable to Output Valid		80		80		100		120	ns

Note 1: Typical values at $T_A = 25°C$.

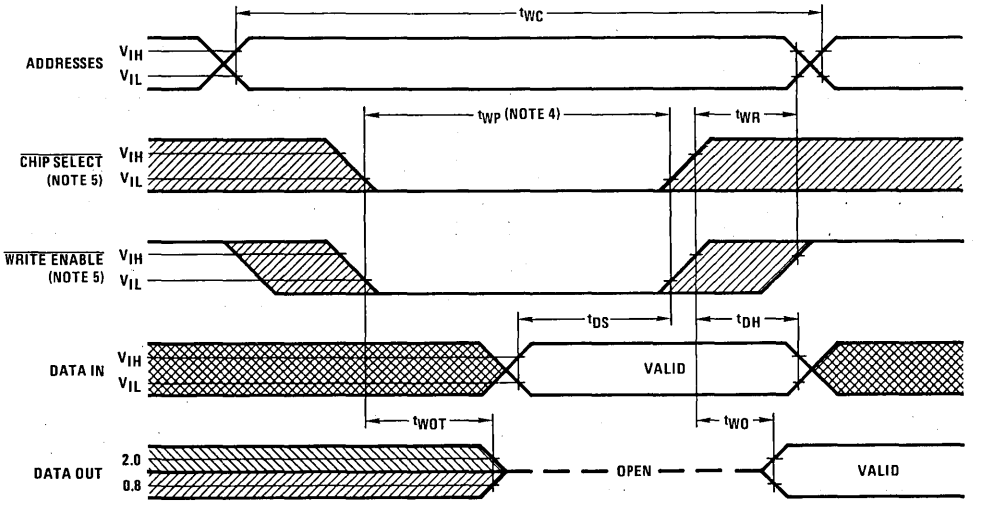
Note 2: All input transitions ≤ 10 ns. Timing referenced to $V_{IL(MAX)}$ or $V_{IH(MIN)}$ for inputs, 0.8V and 2V for output. For test purposes, input levels should swing between 0V and 3V. Output load = 1 TTL gate and $C_L = 50$ pF.

Switching Time Waveforms

Read Cycle



Write Cycle



Note 3: $\overline{WE}$ is high during a read cycle ($\overline{WE} \geq V_{IH(MIN)}$).

Note 4: t_{WP} defines the period when both $\overline{CE}$ and $\overline{WE}$ are low. t_{AW} is referenced to the later of $\overline{CE}$ or $\overline{WE}$ going low while t_{DS}, t_{DH} and t_{WR} are referenced to the earlier of $\overline{CE}$ or $\overline{WE}$ going high. t_{WOT} and t_{WO} are referenced to $\overline{WE}$ with $\overline{CE}$ low.

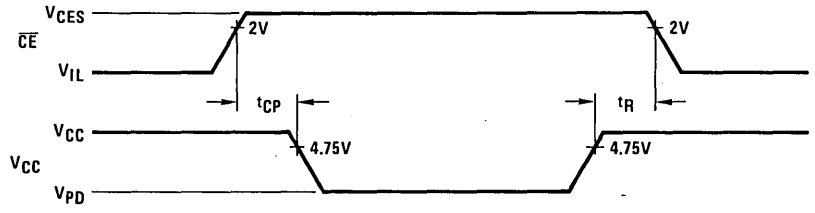
Note 5: Either $\overline{WE}$ or $\overline{CE}$ (or both) must be high during address transitions to prevent erroneous write.

Standby Characteristics $T_A = 0°C$ to $+70°C$

SYMBOL	PARAMETER	CONDITIONS	MM5257 MM5257-2 MM5257-25 MM5257-3		MM5257-L MM5257-2L MM5257-25L MM5257-3L		UNITS
			MIN	MAX	MIN	MAX	
V_{PD}	V_{CC} in Stand-by		1.5		1.5		V
V_{CES}	$\overline{CE}$ Bias in Stand-by	$2 \leq V_{PD} \leq V_{CC(MAX)}$	2.0		2.0		V
V_{CES}	$\overline{CE}$ Bias in Stand-by	$1.5 \leq V_{PD} \leq 2$	V_{PD}		V_{PD}		V
I_{PD1}	Stand-by Current	All Inputs = V_{PD} = 1.5V		70		45	mA
I_{PD2}	Stand-by Current	All Inputs = V_{PD} = 2V		75		50	mA
t_{CP}	Chip Deselect to Stand-by Time		0		0		ns
t_R	Recovery Time		t_{RC}		t_{RC}		ns
CAPACITANCE $T_A = 25°C$, f = 1 MHz, (Note 6)							
C_{IN}	Input Capacitance	All Inputs V_{IN} = 0V		5		5	pF
C_{OUT}	Output Capacitance	V_O = 0V		10		10	pF

Note 6: This parameter is guaranteed by periodic testing.

Standby Waveforms



National Semiconductor

NMOS RAMs
PREVIEW

NMC2114A, NMC2114AP 4096-Bit (1024 x 4) Static RAMs

General Description

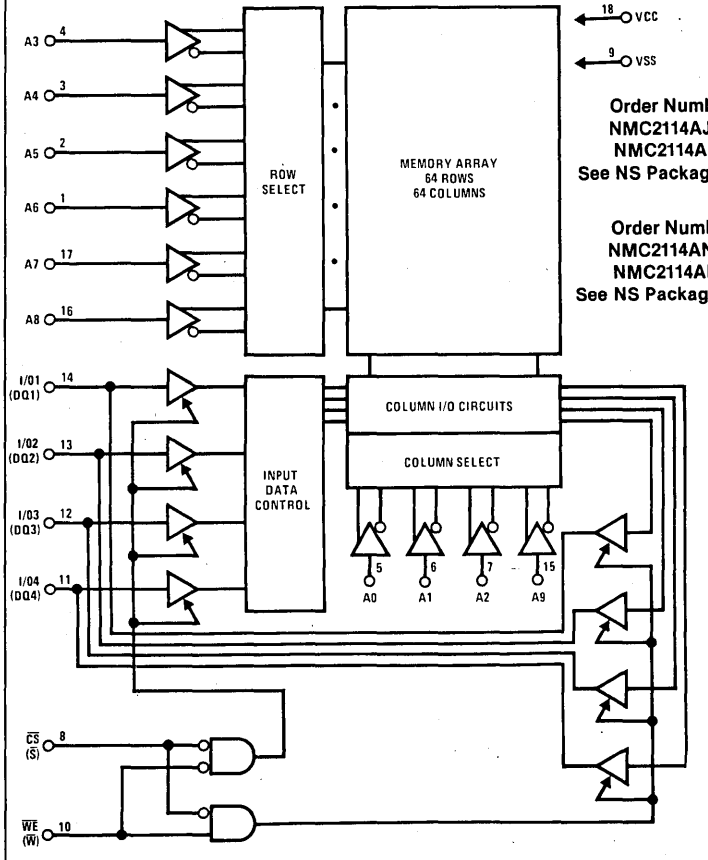
These 1024-word by 4-bit static random access memories are fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The separate chip select input allows easy memory expansion by OR-tying individual devices to a data bus and automatically powers down the NMC2114AP.

Features

- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Low power—225 mW typical
- High speed—120 ns max access time
- TRI-STATE® output for bus interface
- Common Data In and Data Out pins
- Single 5V supply
- Power down option—NMC2114AP

Block Diagram*

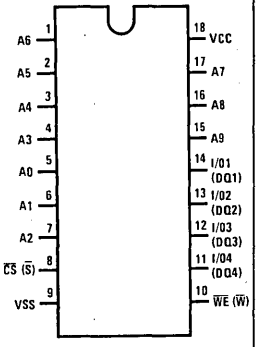


Order Number NMC2114AJ or NMC2114APJ
See NS Package J18A

Order Number NMC2114AN or NMC2114APN
See NS Package N18A

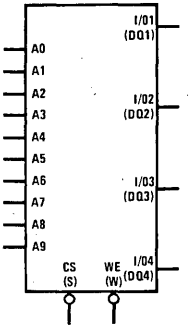
Connection Diagram*

Dual-In-Line Package



TOP VIEW

Logic Symbol*



Pin Names*

A0-A9	Address Inputs
$\overline{WE}$ ($\overline{W}$)	Write Enable
$\overline{CS}$ ($\overline{S}$)	Chip Select
I/01-I/04 (DQ1-DQ4)	Data Input/Output

* The symbols in parentheses are proposed industry standard.

Absolute Maximum Ratings

Voltage at Any Pin with Respect to VSS	−1.5V to +7V
Storage Temperature	−65°C to +150°C
Temperature with Bias	−10°C to +85°C
DC Output Current	20 mA
Power Dissipation	1.2W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (VCC)	4.5	5.5	V
Ambient Temperature (TA)	0	+70	°C

DC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ±10%

Symbol	Parameter	Conditions	NMC2114A		NMC2114AP		Units
			Min	Max	Min	Max	
ILI	Input Load Current (All Input Pins)	VIN = 0V to 5.5V		10		10	μA
|ILO|	I/O Leakage Current	$\overline{CS}$ = 2.4V, VI/O = 0.4V to VCC		10		10	μA
ICC1	Power Supply Current	VIN = 5.5V, II/O = 0 mA, TA = 25°C		45		45	mA
ICC2	Power Supply Current	VIN = 5.5V, II/O = 0 mA, TA = 0°C		50		50	mA
VIL	Input Low Voltage		−1.0	0.8	−1.0	0.8	V
VIH	Input High Voltage		2.0	6.0	2.0	6.0	V
IOL	Output Low Current	VOL = 0.4V	8.0		8.0		mA
IOH	Output High Current	VOH = 2.4V	−4.0		−4.0		mA
IOS	Output Short Circuit Current	VI/O = VSS to VCC (Note 1)	−120	120	−120	120	mA
ISB	Standby Current	VCC = Min to Max, $\overline{CS}$ = VIH		ICC		15	mA
IPO	Peak Power-On Current	VCC = VSS to VCC Min $\overline{CS}$ = Lower of VCC or VIH Min		ICC		15	mA

Capacitance TA = 25°C, f = 1.0 MHz (Note 2)

Symbol	Parameter	Conditions	NMC2114A		NMC2114AP		Units
			Min	Max	Min	Max	
CI/O	Input/Output Capacitance	VI/O = 0V		10		10	pF
CIN	Input Capacitance	VIN = 0V		5		5	pF

AC Test Conditions (Note 3)

Input Pulse Levels	0.8V to 2.4V
Input Rise and Fall Times	≤10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and CL = 100 pF

Note 1: Maximum duration of 60 seconds.

Note 2: This parameter is guaranteed by periodic testing.

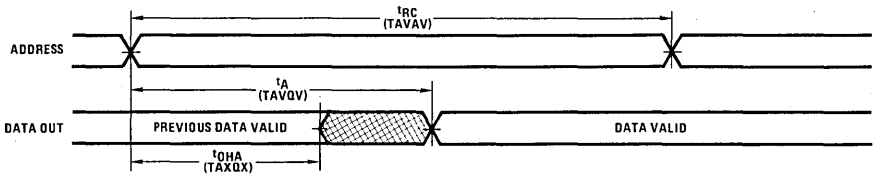
Note 3: These circuits require 500 μs time delay after VCC reaches the specified minimum limit to ensure proper operation after power on. This allows the internally generated substrate bias to reach its functional level.

Read Cycle AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$

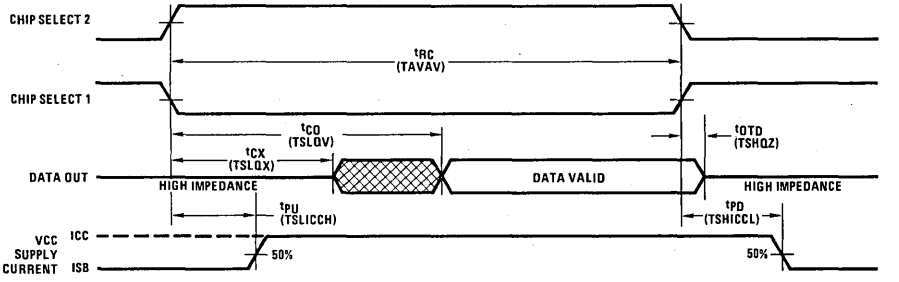
Symbol		Parameter	NMC2114A		NMC2114AP		Units
Alternate	Standard		Min	Max	Min	Max	
t_{RC}	TAVAV	Read Cycle Time	120		120		ns
t_A	TAVQV	Address Access Time		120		120	ns
t_{CO}	TSLQV	Chip Select Access Time (Notes 4 and 5)		70		120	ns
t_{CX}	TSLQX	Chip Select to Output Active	20		20		ns
t_{OTD}	TSHQZ	Chip Select to Output TRI-STATE®		60		60	ns
t_{OHA}	TAXQX	Output Hold from Address Change	10		10		ns
t_{PU}	TSLICCH	Chip Select to Power Up			0		ns
t_{PD}	TSHICCL	Chip Select to Power Down				60	ns

Read Cycle Waveforms*

Read Cycle 1 (Continuous Selection $\overline{CS}$ = VIL, $\overline{WE}$ = VIH)



Read Cycle 2 (Chip Select Switched, $\overline{WE}$ = VIH) (Note 5)



Note 4: This parameter is increased by 10 ns for the NMC2114AP if the device is deselected for less than 55 ns.

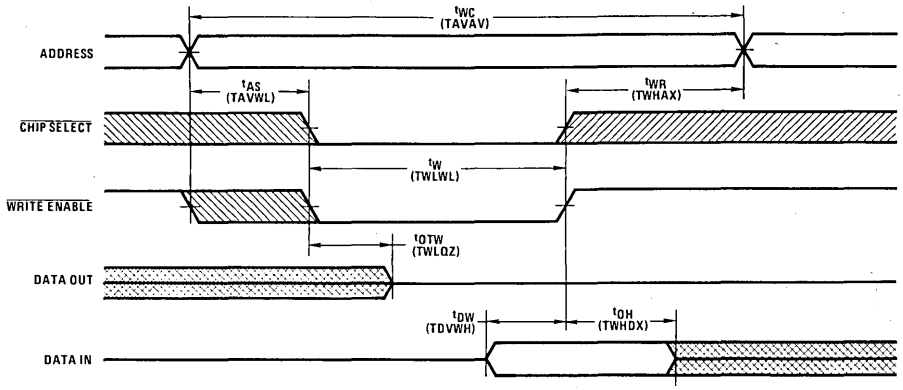
Note 5: Addresses must be valid coincident with or prior to the chip select transition from high to low for the NMC2114AP. Addresses must be valid 50 ns or more prior to the chip select transition from high to low for the NMC2114A.

* Symbols in parentheses are proposed industry standard.

Write Cycle AC Electrical Characteristics (Note 6) TA = 0°C to +70°C, VCC = 5V ±10%

Symbol		Parameter	NMC2114A		NMC2114AP		Units
Alternate	Standard		Min	Max	Min	Max	
t_{WC}	TAVAV	Write Cycle Time	120		120		ns
t_{AS}	TAVSL TAVWL	Address Set-Up Time	0		0		ns
t_W	TWLWL	Write Time	60		60		ns
t_{WR}	TWHAX	Write Recovery Time	10		10		ns
t_{DW}	TDVWH	Data Set-Up Time	50		50		ns
t_{DH}	TWHDX	Data Hold Time	10		10		ns
t_{OTW}	TWLQZ	Write Enable to Output TRI-STATE		60		60	ns

Write Cycle Waveforms* (Note 7)



Note 6: A write occurs during the coincidence low of $\overline{CS}$ and $\overline{WE}$.

Note 7: The outputs remain in TRI-STATE if the $\overline{CS}$ low transition and the $\overline{WE}$ low transition occur simultaneously. $\overline{WE}$ or $\overline{CS}$ or both must be high during the address transitions.

* Symbols in parentheses are proposed industry standard.

National Semiconductor

NMOS RAMs
PREVIEW

NMC2141, NMC5257A 4096-Bit (4096 x 1) Static RAMs

General Description

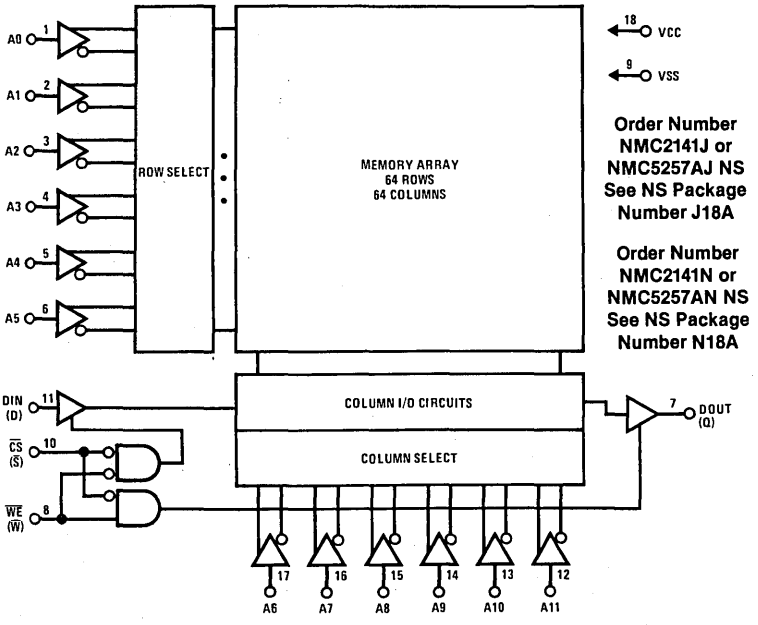
These 4096-word by 1-bit static random access memories are fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data. Separate input/output pins are provided.

The separate chip select input allows easy memory expansion by OR-tying individual devices to a data bus and automatically powers down the NMC2141.

Features

- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Low power—225 mW typical
- High speed—120 ns max access time
- TRI-STATE® output for bus interface
- Common Data In and Data Out pins
- Single 5V supply
- Power down option—NMC2141

Block Diagram*



Order Number NMC2141J or NMC5257AJ NS See NS Package Number J18A

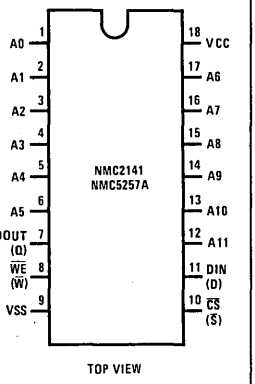
Order Number NMC2141N or NMC5257AN NS See NS Package Number N18A

Pin Names*

A0-A11	All Inputs
$\overline{WE}$ (W)	Write Enable
$\overline{CS}$ (S)	Chip Select
DIN (D)	Data Input
DOUT (Q)	Data Output

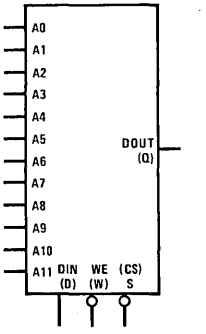
Connection Diagram*

Dual-In-Line Package



TOP VIEW

Logic Symbol*



* The symbols in parentheses are proposed industry standard.

Absolute Maximum Ratings

Voltage at Any Pin with Respect to VSS	−1.5V to +7V
Storage Temperature	−65°C to +150°C
Temperature with Bias	−10°C to +85°C
DC Output Current	20 mA
Power Dissipation	1.2W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (VCC)	4.5	5.5	V
Ambient Temperature (TA)	0	+70	°C

DC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ± 10%

Symbol	Parameter	Conditions	NMC5257A		NMC2141		Units
			Min	Max	Min	Max	
ILI	Input Load Current (All Input Pins)	VIN = 0V to 5.5V		10		10	μA
|ILO|	Output Leakage Current	$\overline{CS}$ = 2.4V, VOUT = 0.4V to VCC		10		10	μA
ICC1	Power Supply Current	VIN = 5.5V, TA = 25°C Output Open		45		45	mA
ICC2	Power Supply Current	VIN = 5.5V, TA = 0°C Output Open		50		50	mA
VIL	Input Low Voltage		−1.0	0.8	−1.0	0.8	V
VIH	Input High Voltage		2.0	6.0	2.0	6.0	V
IOL	Output Low Current	VOL = 0.4V	8.0		8.0		mA
IOH	Output High Current	VOH = 2.4V	−4.0		−4.0		mA
IOS	Output Short Circuit Current	VOUT = VSS to VCC (Note 1)	−120	120	−120	120	mA
ISB	Standby Current	VCC = Min to Max, $\overline{CS}$ = VIH		ICC		15	mA
IPO	Peak Power-On Current	VCC = VSS to VCC Min $\overline{CS}$ = Lower of VCC or VIH Min		ICC		15	mA

Capacitance TA = 25°C, f = 1.0 MHz (Note 2)

Symbol	Parameter	Conditions	NMC5257A		NMC2141		Units
			Min	Max	Min	Max	
COUT	Output Capacitance	VOUT = 0V		6		5	pF
CIN	Input Capacitance	VIN = 0V		5		5	pF

AC Test Conditions (Note 3)

Input Pulse Levels	
NMC2141	GND to 3.5V
NMC5257A	0.8V to 2.4V
Input Rise and Fall Times	≤ 10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and CL = 100 pF

Note 1: Maximum duration of 60 seconds.

Note 2: This parameter is guaranteed by periodic testing.

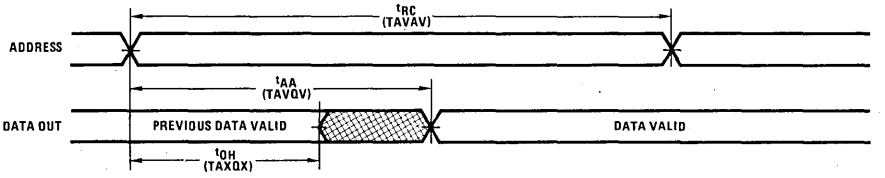
Note 3: These circuits require 500 μs time delay after VCC reaches the specified minimum limit to ensure proper operation after power on. This allows the internally generated substrate bias to reach its functional level.

Read Cycle AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$

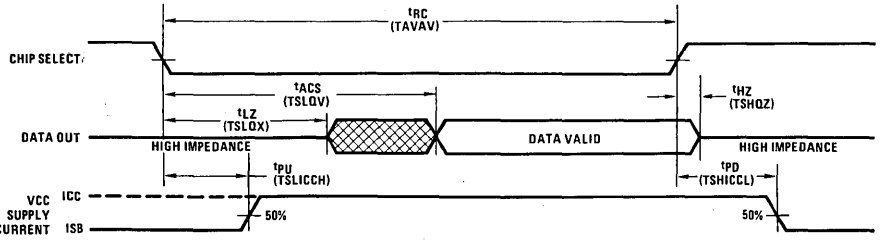
Symbol		Parameter	NMC5257A		NMC2141		Units
Alternate	Standard		Min	Max	Min	Max	
t_{RC}	TAVAV	Read Cycle Time	120		120		ns
t_{AA}	TAVQV	Address Access Time		120		120	ns
t_{ACS}	TSLQV	Chip Select Access Time (Notes 4 and 5)		70		120	ns
t_{LZ}	TSLQX	Chip Select to Output Active	20		20		ns
t_{HZ}	TSHQZ	Chip Select to Output TRI-STATE		60		60	ns
t_{OH}	TAXQX	Output Hold from Address Change	10		10		ns
t_{PU}	TSLICCH	Chip Select to Power Up			0		ns
t_{PD}	TSHICCL	Chip Select to Power Down				60	ns

Read Cycle Waveforms*

Read Cycle 1 (Continuous Selection $\overline{CS}$ = VIL, $\overline{WE}$ = VIH)



Read Cycle 2 (Chip Select Switched, $\overline{WE}$ = VIH) (Note 5)



Note 4: This parameter is increased by 10 ns for the NMC2141 if the device is deselected for less than 55 ns.

Note 5: Addresses must be valid coincident with or prior to the chip select transition from high to low for the NMC2141. Addresses must be valid 50 ns or more prior to the chip select transition from high to low for the NMC5257A.

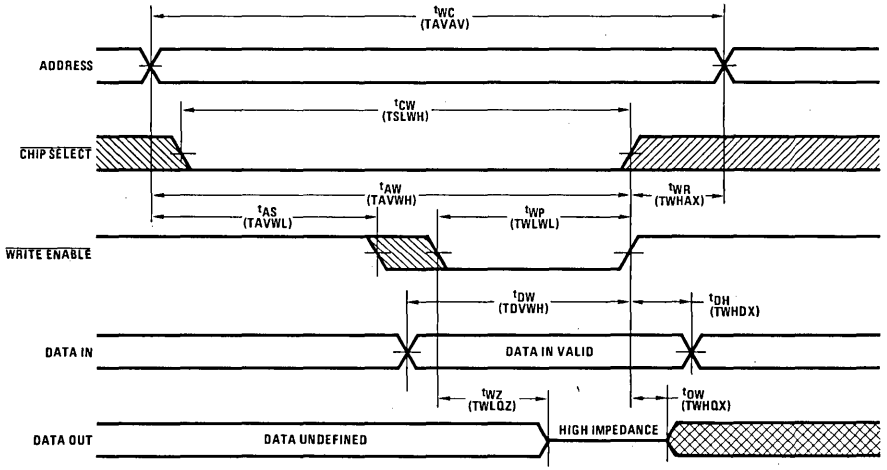
* Symbols in parentheses are proposed industry standard.

Write Cycle AC Electrical Characteristics (Note 6) TA = 0°C to +70°C, VCC = 5V ± 10%

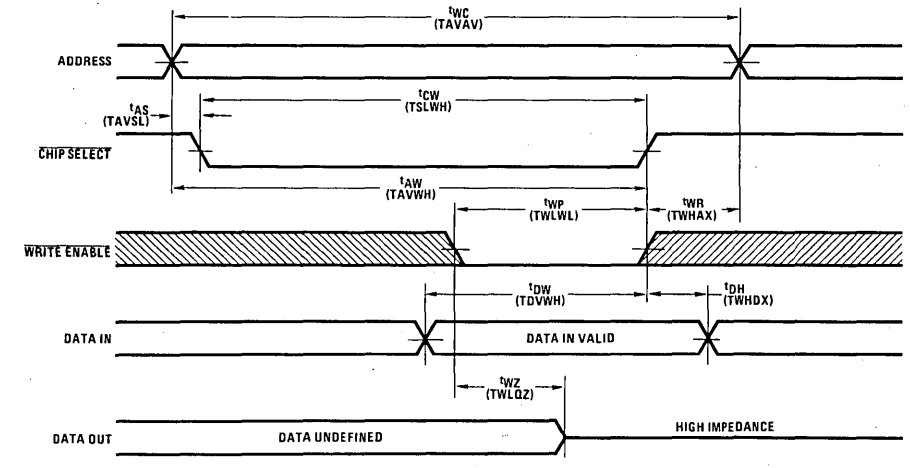
Symbol		Parameter	NMC5257A		NMC2141		Units
Alternate	Standard		Min	Max	Min	Max	
t_{RC}	TAVAV	Write Cycle Time	120		120		ns
t_{AS}	TAVSL TAVWL	Address Set-Up Time	0		0		ns
t_{WP}	TWLWL	Write Pulse Width	60		60		ns
t_{WR}	TWHAX	Write Recovery Time	10		10		ns
t_{DW}	TDVWH	Data Set-Up Time	50		50		ns
t_{DH}	TWHDX	Data Hold Time	10		10		ns
t_{WZ}	TWLQZ	Write Enable to Output TRI-STATE		60		60	ns
t_{OW}	TWHQX	Write Enable to Output Active		5		5	ns
t_{CW}	TSLWH	Chip Select to End of Write		110		110	ns
t_{AW}	TAVWH	Address Valid to End of Write		110		110	ns

Write Cycle Waveforms* (Note 7)

Write Cycle 1 (Write Enable Limited)



Write Cycle 2 (Chip Select Limited)



Note 6: A write occurs during the coincidence low of $\overline{CS}$ and $\overline{WE}$.

Note 7: The output remains TRI-STATE if the $\overline{CS}$ and $\overline{WE}$ go high simultaneously. $\overline{WE}$ or $\overline{CS}$ or both must be high during the address transitions.

* Symbols in parentheses are proposed industry standard.

National Semiconductor

NMOS RAMs
PREVIEW

NMC2142A, NMC2142AP 4096-Bit (1024 × 4) Static RAMs

General Description

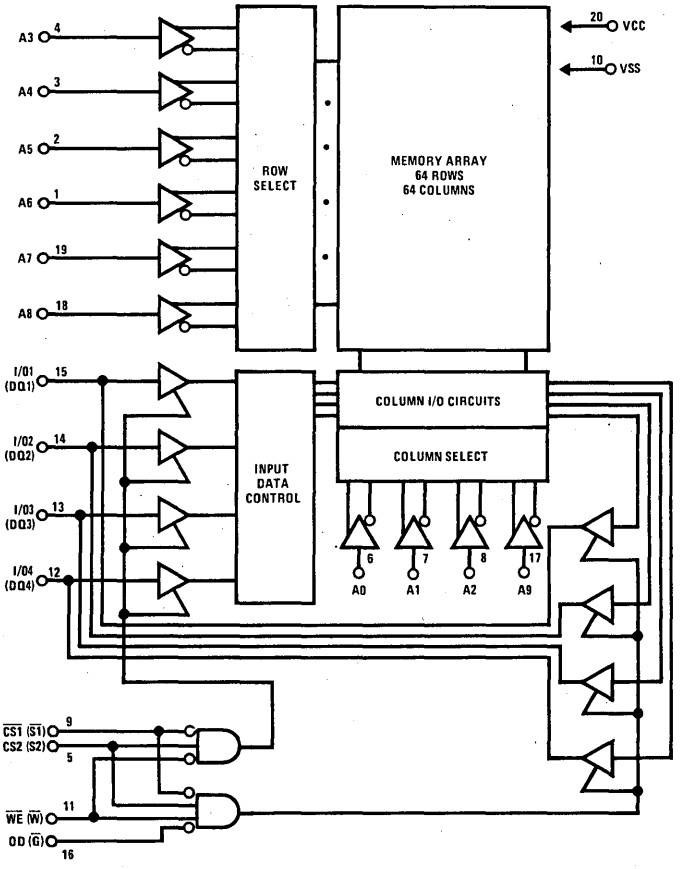
These 1024-word by 4-bit static random access memories are fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The separate chip select inputs allow easy memory expansion by OR-tying individual devices to a data bus and automatically powers down the NMC2142AP.

Features

- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Low power—225 mW typical
- High speed—120 ns max access time
- TRI-STATE® output for bus interface
- Common Data In and Data Out pins
- Single 5V supply
- Power down option—NMC2142AP

Block Diagram*



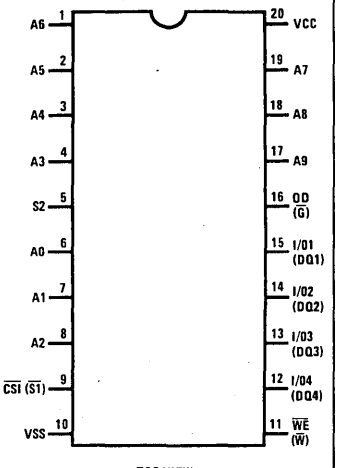
Pin Names*

A0-A9	Address Inputs
$\overline{WE}$ ($\overline{W}$)	Write Enable
$\overline{CS1}$, CS2 ($\overline{S1}$, S2)	Chip Select
I/01-I/04 (DQ1-DQ4)	Data Input/Output
OD ($\overline{G}$)	Output Disable

* The symbols in parentheses are proposed industry standard.

Connection Diagram*

Dual-In-Line Package

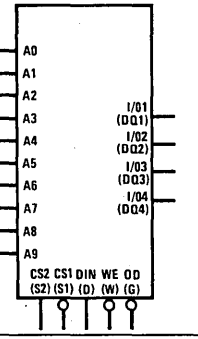


TOP VIEW

Order Number
NMC2142AJ or NMC2142APJ
See NS Package J20B

Order Number
NMC2142AN or NMC2142APN
See NS Package N20A

Logic Symbol*



Absolute Maximum Ratings

Voltage at Any Pin with Respect to VSS	−1.5V to +7V
Storage Temperature	−65°C to +150°C
Temperature with Bias	−10°C to +85°C
DC Output Current	20 mA
Power Dissipation	1.2W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (VCC)	4.5	5.5	V
Ambient Temperature (TA)	0	+70	°C

DC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ±10%

Symbol	Parameter	Conditions	NMC2142A		NMC2142AP		Units
			Min	Max	Min	Max	
ILI	Input Load Current (All Input Pins)	VIN = 0V to 5.5V		10		10	μA
|ILO|	I/O Leakage Current	$\overline{CS}$ = 2.4V, VI/O = 0.4V to VCC		10		10	μA
ICC1	Power Supply Current	VIN = 5.5V, II/O = 0 mA, TA = 25°C		45		45	mA
ICC2	Power Supply Current	VIN = 5.5V, II/O = 0 mA, TA = 0°C		50		50	mA
VIL	Input Low Voltage		−1.0	0.8	−1.0	0.8	V
VIH	Input High Voltage		2.0	6.0	2.0	6.0	V
IOL	Output Low Current	VOL = 0.4V	8.0		8.0		mA
IOH	Output High Current	VOH = 2.4V	−4.0		−4.0		mA
IOS	Output Short Circuit Current	VI/O = VSS to VCC (Note 1)	−120	120	−120	120	mA
ISB	Standby Current	VCC = Min to Max, $\overline{CS}$ = VIH		ICC		15	mA
IPO	Peak Power-On Current	VCC = VSS to VCC Min $\overline{CS}$ = Lower of VCC or VIH Min		ICC		15	mA

Capacitance TA = 25°C, f = 1.0 MHz (Note 2)

Symbol	Parameter	Conditions	NMC2142A		NMC2142AP		Units
			Min	Max	Min	Max	
CI/O	Input/Output Capacitance	VI/O = 0V		5		5	pF
CIN	Input Capacitance	VIN = 0V		5		5	pF

AC Test Conditions (Note 3)

Input Pulse Levels	0.8V to 2.4V
Input Rise and Fall Times	≤10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and CL = 100 pF

Note 1: Maximum duration of 60 seconds.

Note 2: This parameter is guaranteed by periodic testing.

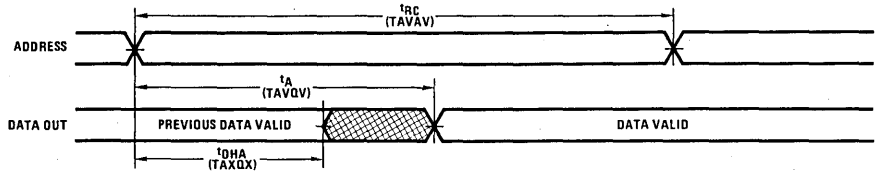
Note 3: These circuits require 500 μs time delay after VCC reaches the specified minimum limit to ensure proper operation after power on. This allows the internally generated substrate bias to reach its functional level.

Read Cycle AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$

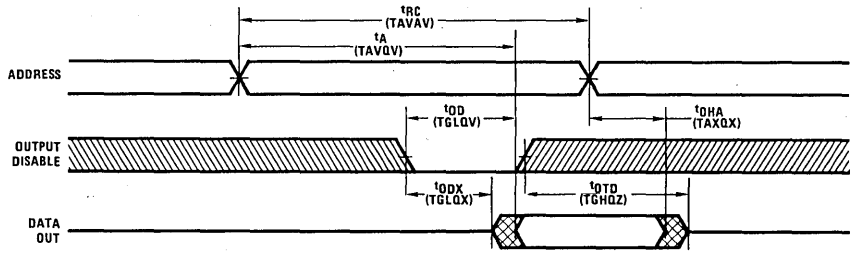
Symbol		Parameter	NMC2142A		NMC2142AP		Units
Alternate	Standard		Min	Max	Min	Max	
t_{RC}	TAVAV	Read Cycle Time	120		120		ns
t_A	TAVQV	Address Access Time		120		120	ns
t_{CO}	TSXQV	Chip Select Access Time (Notes 4 and 5)		70		120	ns
t_{CX}	TSLQX	Chip Select to Output Active	20		20		ns
t_{OTD}	TGHQZ TSHQZ	Output TRI-STATE from Disable		60		60	ns
t_{OHA}	TAXQX	Output Hold from Address Change	10		10		ns
t_{OD}	TGLQV	Output Disable to Output Valid		60		60	ns
t_{ODX}	TGLQX	Output Disable to Output Active	20		20		ns
t_{PU}	TSLICCH	Chip Select to Power Up			0		ns
t_{PD}	TSHICCL	Chip Select to Power Down				60	ns

Read Cycle Waveforms*

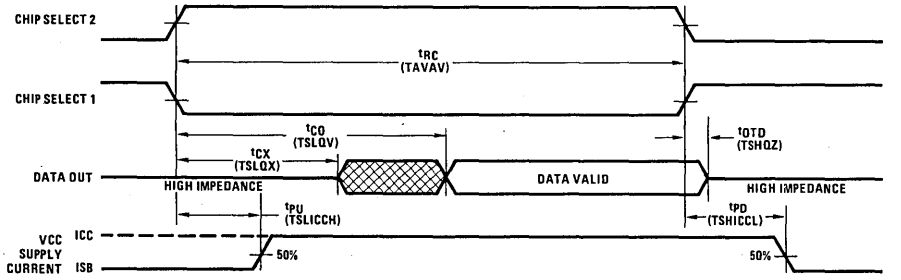
Read Cycle 1 (Continuous Selection $\overline{CS1}$ = VIL, CS2 = VIH, OD = VIL, $\overline{WE}$ = VIH)



Read Cycle 2 (Continuous Selection with Output Disable Switched, $\overline{CS1}$ = VIL, CS2 = VIH, $\overline{WE}$ = VIH)



Read Cycle 3 (Chip Select(s) Switched, OD = VIL, $\overline{WE}$ = VIH) (Note 5)



Note 4: This parameter is increased by 10 ns for the NMC2142AP if the device is deselected for less than 55 ns.

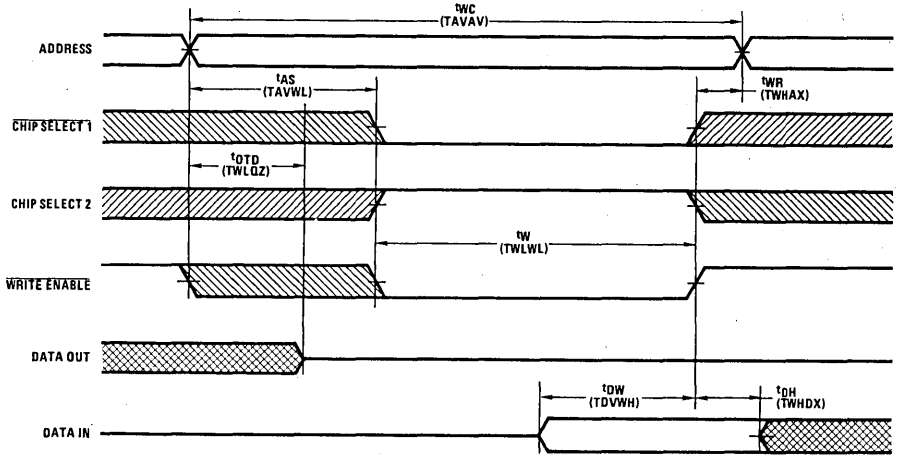
Note 5: Addresses must be valid coincident with or prior to the chip select transition from high to low for the NMC2142AP. Address must be valid 50 ns or more prior to the chip select transition from high to low for the NMC2142A.

* Symbols in parentheses are proposed industry standard.

Write Cycle AC Electrical Characteristics (Note 6) TA = 0°C to +70°C, VCC = 5V ±10%

Symbol		Parameter	NMC2142A		NMC2142AP		Units
Alternate	Standard		Min	Max	Min	Max	
t_{WC}	TAVAV	Write Cycle Time	120		120		ns
t_{AS}	TAVSX TAVWL	Address Set-Up Time	0		0		ns
t_{W}	TWLWL	Write Time	60		60		ns
t_{WR}	TWHAX	Write Recovery Time	10		10		ns
t_{DW}	TDVWH	Data Set-Up Time	50		50		ns
t_{DH}	TWHDX	Data Hold Time	10		10		ns
t_{OTD}	TSXQZ TWLQZ	Write Enable to Output TRI-STATE		60		60	ns

Write Cycle Waveforms* (OD = VIH) (Note 7)



Note 6: A write occurs during the coincidence low of $\overline{CS}$ and $\overline{WE}$.

Note 7: The outputs remain in TRI-STATE if the chip is deselected with a chip select transition simultaneously with the $\overline{WE}$ low transition. $\overline{WE}$ or $\overline{CS}$ or both must be high during the address transitions.

* Symbols in parentheses are proposed industry standard.

National Semiconductor

NMOS RAMs
PREVIEW

NMC2148/NMC2148L 1024 x 4 Static RAM

General Description

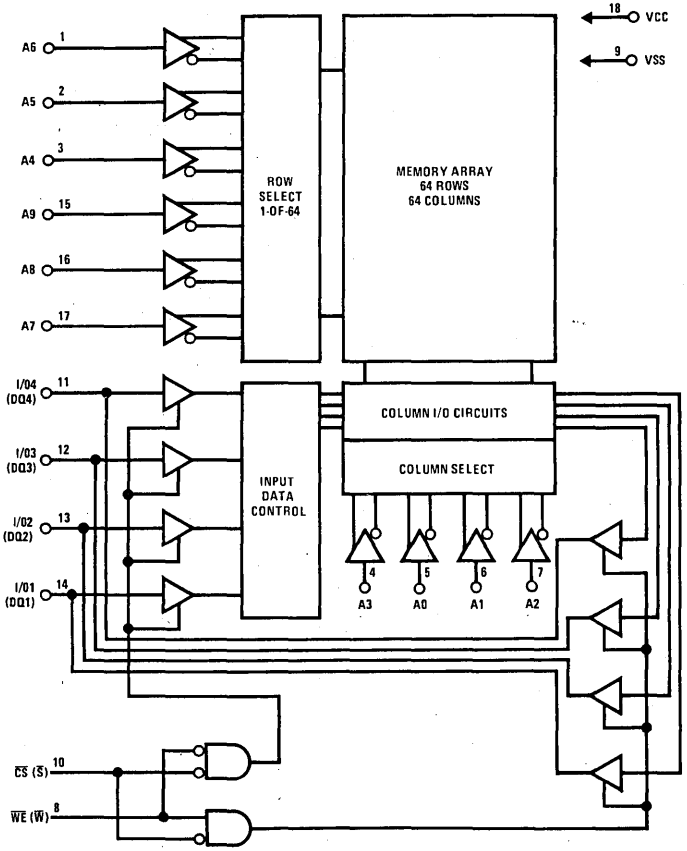
The NMC2148 is a 1024-word by 4-bit static random access memory fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data.

The separate chip select input automatically switches the part to its low power standby mode when it goes high. Common input/output pins are provided.

Features

- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Automatic power down
- High speed—down to 55 ns access time
- TRI-STATE® output for bus interface
- Common Data I/O pins
- Single +5V supply
- Standard 18-pin dual-in-line package

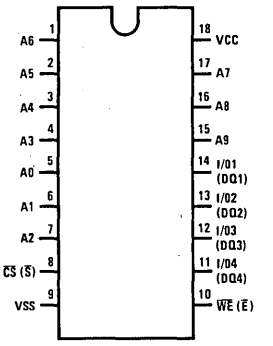
Block Diagram*



* The symbols in parentheses are proposed industry standard.

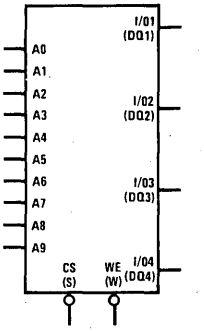
Connection Diagram*

Dual-In-Line Package



TOP VIEW

Logic Symbol*



Pin Names*

A0-A9	Address Inputs
$\overline{WE}$ ($\overline{W}$)	Write Enable
$\overline{CS}$ ($\overline{S}$)	Chip Select
I/01-I/04 (DQ1-DQ4)	Data Input/Output
VCC	Power (+5V)
VSS	Ground

Pseudo-Static RAMs

National Semiconductor

NMOS RAMs
PREVIEW

NMC4864 64k Pseudo-Static Byte-Wide RAM

General Description

The NMC4864 is a single 5V power supply pseudo-static NMOS RAM organized as 8192 words by 8 bits. The circuit uses single-transistor dynamic storage cells with internal refresh control to make the part appear static to the user. The byte-wide (8-bit input/output) organization makes this RAM ideal for microprocessor applications. The part is manufactured using National's new TRI-POLY™ scaled process.

The NMC4864 has separate address and data I/O pins for use with either separate or multiplexed address/data buses. Two modes of operation are possible with the cycle initiated by the Read ($\overline{R}$)/Write ($\overline{W}$) signals or the Address ($\overline{E}$) signal.

The NMC4864 has a bidirectional refresh status and control pin $\overline{F}$ ($\overline{RFSH}$). Use of this pin selects either of two cycle-initiated refresh modes or the self-timed standby mode.

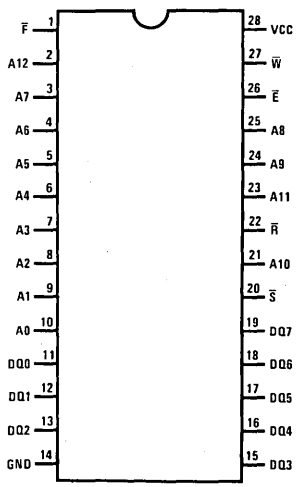
The NMC4864 is packaged in a standard 28-pin DIP with the JEDEC proposed standard pinout. This pinout is EPROM/ROM compatible with minimal modification.

Features

- 8192 words × 8-bit organization
- High performance
  Access time — 150 ns
  Cycle time — 250 ns
- Low power: 200 mW active, 50 mW standby
- Single 5V 10% supply with on-chip substrate bias generator
- 256 refresh cycles/4 ms automatically provided
- Automatic self refresh with fast and slow cycle modes
- Standby/single step auto-refresh allows infinite maximum cycle time
- Standard 28-pin DIP with JEDEC proposed pinout
- Pinout ROM/EPROM compatible

Connection Diagram

Dual-In-Line Package



TOP VIEW

Pin Names

A0-A12	Address inputs
$\overline{E}$	Address latch enable
$\overline{R}$	Read strobe
$\overline{W}$	Write strobe
$\overline{S}$	Chip select
DQ0-DQ7	Data input/output (TRI-STATE®)
$\overline{F}$ ($\overline{RFSH}$)	Refresh (bidirectional)
VCC	Power supply
VSS	Ground

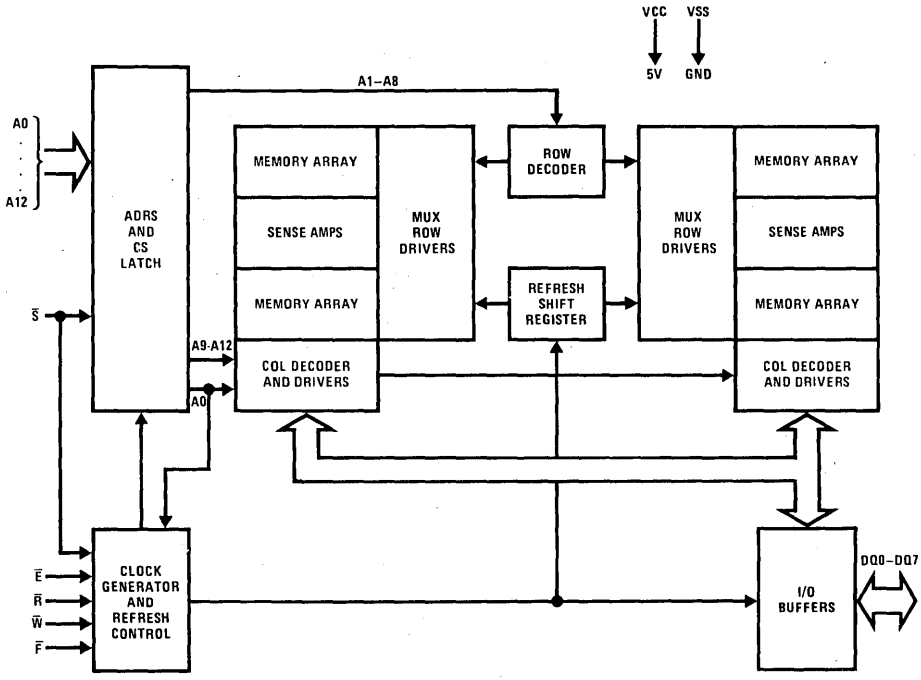
Absolute Maximum Ratings

Operating Temperature Range	0°C to + 70°C
Storage Temperature	− 65°C to + 150°C
All Pins with Respect to VSS	− 3.0V to + 7.0V
Power Dissipation	1.25W

DC Electrical Characteristics TA = 0°C to + 70°C, VCC = 5V ± 10%, VSS = 0V

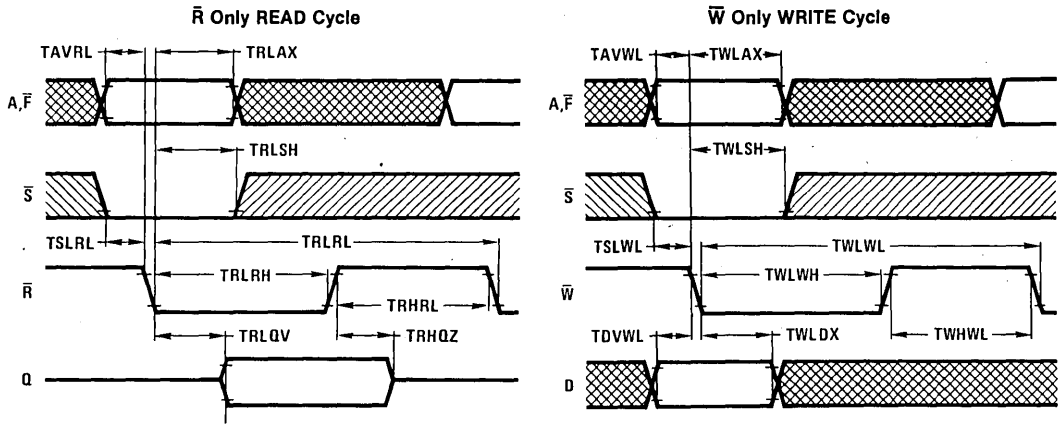
JEDEC Symbol	Parameter	Conditions	Min	Max	Units
VIH	Input Voltage HIGH		2.0	7.0	V
VIL	Input Voltage LOW		− 1.0	0.8	V
II	Input Leakage Current		− 10	10	μA
IOZ	Output Leakage Current		− 10	10	μA
VOH	Output Voltage HIGH	IOH = − 1 mA	2.4		V
VOL	Output Voltage LOW	IOL = 4 mA		0.4	V
ICC1	Power Supply Current (Operating)			40	mA
ICC2	Power Supply Current (Standby)			10	mA
IF	Refresh Output LOW Current	VF = 0.4V		6.0	mA
CI	Input Capacitance (A)			5	pF
CC	Input Capacitance ($\bar{E}$, $\bar{R}$, $\bar{W}$)			10	pF
CO	Output Capacitance (DQ, $\bar{F}$)			10	pF

Block Diagram



$\overline{R}$ Only READ Cycle and $\overline{W}$ Only WRITE Cycle $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$

Waveforms



AC Characteristics $\overline{R}$ Only READ Cycle

JEDEC Symbol	Parameter	Min	Max	Units
TRLRL	Cycle Time			
	Short Cycle Mode ($\overline{F}$ = HIGH)	250		ns
	Double Cycle Mode ($\overline{F}$ = LOW)	500		ns
	Standby/Single Step Mode		∞	ns
TRLRH	Read LOW Pulse Width	0.150	100	μs
TRHRL	Read HIGH Pulse Width	80		ns
TAVRL	Address/Refresh Set-Up Time	0		ns
TRLAX	Address/Refresh Hold Time	20		ns
TSLRL	Select Set-Up Time	0		ns
TRLSH	Select Hold Time	20		ns
TRLQV	Read Access Time		150	ns
TRHQZ	Output Deselect Time		35	ns

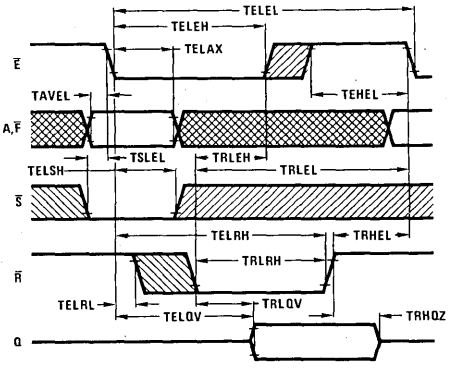
AC Characteristics $\overline{W}$ Only WRITE Cycle

JEDEC Symbol	Parameter	Min	Max	Units
TWLWL	Cycle Time			
	Short Cycle Mode ($\overline{F}$ = HIGH)	250		ns
	Double Cycle Mode ($\overline{F}$ = LOW)	500		ns
	Standby/Single Mode		∞	ns
TWLWH	Write LOW Pulse Width	0.150	100	μs
TWHWL	Write HIGH Pulse Width	80		ns
TAVWL	Address/Refresh Set-Up Time	0		ns
TWLAX	Address/Refresh Hold Time	20		ns
TSLWL	Select Set-Up Time	0		ns
TWLSH	Select Hold Time	20		ns
TDVWL	Data Set-Up Time	0		ns
TWLDX	Data Hold Time	20		ns

$\overline{E}$ Only READ or WRITE Cycle $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$

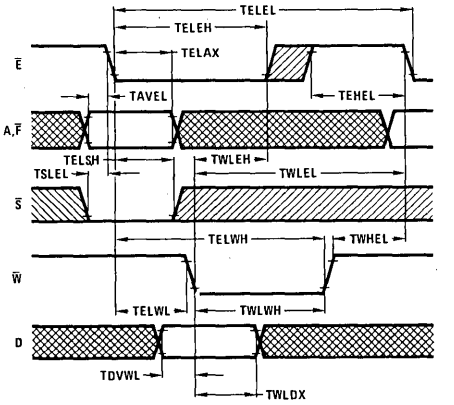
Waveforms

$\overline{E}$ READ Cycle



Note: TRHQZ is determined by the earliest rising edge of either $\overline{E}$ or $\overline{R}$.

$\overline{E}$ WRITE Cycle



Note: WRITE cycle is terminated by the earliest rising edge of either $\overline{E}$ or $\overline{W}$.

AC Characteristics

JEDEC Symbol	Parameter	Min	Max	Units
READ OR WRITE				
TELEL	Cycle Time			
	Short Cycle Mode ($\overline{F}$ = HIGH)	250		ns
	Double Cycle Mode ($\overline{F}$ = LOW)	500		ns
	Standby/Single Step Mode		∞	ns
TELEH	Enable LOW Pulse Width	50		ns
TEHEL	Enable HIGH Pulse Width	80		ns
TAVEL	Address/Refresh Set-Up Time	0		ns
TELAX	Address/Refresh Hold Time	20		ns
TSLEL	Chip Select Set-Up Time	0		ns
TELSH	Chip Select Hold Time	20		ns
READ				
TELRL	Enable LOW to Read LOW Delay Time	0	100	μs
TRLRH	Read LOW Pulse Width	50		ns
TELRH	Enable LOW to Read HIGH Delay Time	0.150	100	μs
TRHEL	Read HIGH to Enable LOW Delay Time	80		ns
TRLEH	Read LOW to Enable HIGH Delay Time	20		ns
TRLEL	Read LOW to Enable LOW Delay Time			
	Short Cycle Mode ($\overline{F}$ = HIGH)	130		ns
	Double Cycle Mode ($\overline{F}$ = LOW)	400		ns
TELQV	Enable Access Time		150	ns
TRLQV	Read Access Time		35	ns
TRHQZ	Output Deselect Time		35	ns
WRITE				
TELWL	Enable LOW to Write LOW Delay Time	0	100	μs
TWLWH	Write LOW Pulse Width	50		ns
TELWH	Enable LOW to Write HIGH Delay Time	0.150	100	μs
TWHEL	Write HIGH to Enable LOW Delay Time	80		ns
TWLEH	Write LOW to Enable HIGH Delay Time	20		ns
TWLEL	Write LOW to Enable LOW Delay Time			
	Short Cycle Mode ($\overline{F}$ = HIGH)	130		ns
	Double Cycle Mode ($\overline{F}$ = LOW)	400		ns
TDVWL	Data Set-Up Time	0		ns
TWLDX	Data Hold Time	20		ns

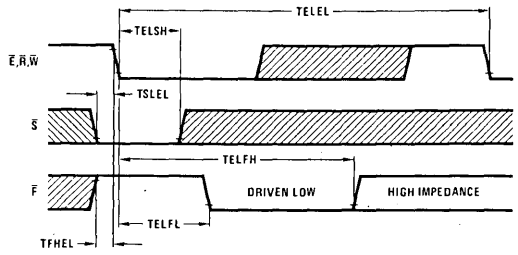
Refresh Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$

AC Characteristics

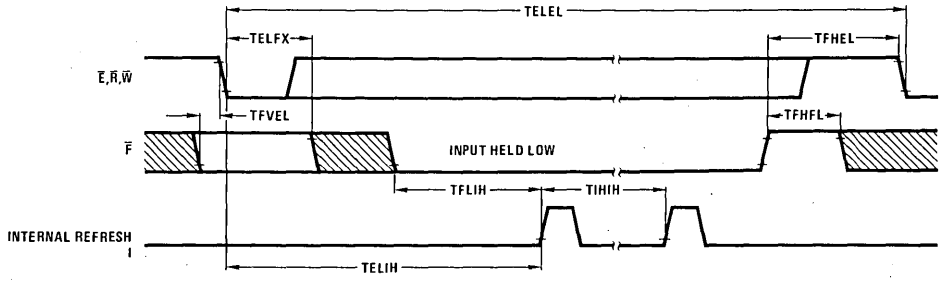
JEDEC Symbol	Parameter	Min	Max	Units
INTERNALLY INITIATED DOUBLE CYCLE (SHORT CYCLE MODE)				
TELEL	Cycle Time	500		ns
TSLEL	Chip Select Set-Up Time	0		ns
TELSH	Chip Select Hold Time	20		ns
TFHEL	Refresh Set-Up Time	0		ns
TELFL	Enable to Refresh LOW Delay Time		50	ns
TELFH	Enable to Refresh Disable Time		500	ns
STANDBY/SINGLE STEP AUTO REFRESH MODE				
TELEL	Cycle Time		∞	ns
TFVEL	Refresh Set-Up Time	0		ns
TELFX	Refresh Hold Time	20		ns
TFHFL	Refresh HIGH Pulse Width	100		ns
TFHEL	Refresh Recovery Time	300		ns
TELIH	Enable to Internal Refresh Delay Time	10		μs
TFLIH	Refresh to Internal Refresh Delay Time	10		μs
TIHIH	Internal Refresh Cycle Time	10	15	μs
TREF	Refresh Time		4	ms

Waveforms

Internally Initiated Double Cycle (Short Cycle Refresh Mode Only)



Standby/Single Step Auto Refresh Mode



Functional Description

The memory is organized as two separate 4k x 8 halves selected by address A0. This architecture provides the means for a highly efficient self refresh scheme. During a read or write to the even half, the odd half is refreshed and vice versa. This is one of three self refresh modes which are fully described later.

The address, chip select, and $\overline{F}$ ($\overline{RFSH}$) inputs are clocked into on-chip latches by one of three control clocks: $\overline{E}$, $\overline{R}$ or $\overline{W}$. The address latch clock, $\overline{E}$, latches address, chip select and $\overline{F}$ on its falling edge. To simplify use in nonmultiplexed systems $\overline{E}$ may be tied permanently HIGH and read or write timing controlled with the falling edge of either the $\overline{R}$ or $\overline{W}$ clocks.

Read Cycles

Read cycles are controlled by the $\overline{S}$, $\overline{R}$, and $\overline{E}$ inputs. For a read cycle $\overline{S}$ must be LOW as specified with respect to $\overline{R}$ or $\overline{E}$ transitions, otherwise $\overline{R}$ and $\overline{E}$ are ignored except to initiate refresh. Two types of read cycles are provided: a $\overline{R}$ only cycle and an $\overline{E}$ cycle.

The $\overline{R}$ only cycle *(Figure 1)* provides simple timing for nonmultiplexed address and data bus systems. With $\overline{E}$ left HIGH, the falling edge of $\overline{R}$ latches the address and $\overline{S}$ inputs; and initiates the cycle. The outputs remain TRI-STATE until after the access time when the data becomes valid. After $\overline{R}$ returns HIGH the data pins return to TRI-STATE.

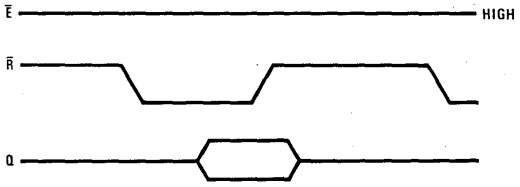


FIGURE 1. $\overline{R}$ Only Read Cycle

The $\overline{E}$ read cycle *(Figure 2)* provides direct compatible timing for multiplexed address and data bus systems. The data bus may be tied directly to the address bus when $\overline{E}$ cycles are used due to time multiplexing of the address and data. Care must be taken with the timing to insure that data outputs are TRI-STATE during address or data input times. The falling edge of $\overline{E}$ latches the address and $\overline{S}$ inputs and initiates the cycle. $\overline{R}$ must go LOW to enable the output buffers. While $\overline{R}$ is LOW $\overline{E}$ may either remain LOW or return HIGH without affecting the output. As long as $\overline{E}$ remains LOW the $\overline{R}$ input acts only as an output enable and may repeatedly be toggled to select and deselect the same output data. The read cycle is terminated by the latter of the rising edges of $\overline{R}$ or $\overline{E}$.

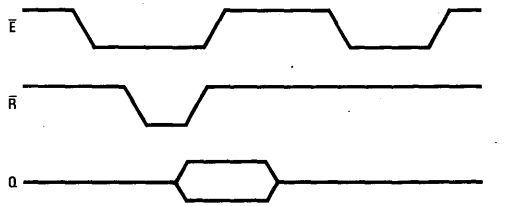


FIGURE 2. $\overline{E}$ Read Cycle

Write Cycles

Write cycles are controlled by the $\overline{S}$, $\overline{W}$ and $\overline{E}$ inputs. For a write cycle $\overline{S}$ must be LOW as specified with respect to $\overline{W}$ and $\overline{E}$ transitions, otherwise $\overline{W}$ and $\overline{E}$ are ignored except to initiate refresh. Two types of write cycles are provided; a $\overline{W}$ only cycle and an $\overline{E}$ cycle.

The $\overline{W}$ only write cycle provides simple timing for nonmultiplexed address and data bus systems. With $\overline{E}$ left HIGH, the falling edge of $\overline{W}$ latches the data in, address and $\overline{S}$ inputs; and initiates the cycle. The rising edge terminates the cycle.

The $\overline{E}$ write cycle provides direct compatible timing for multiplexed address and data bus systems. Care must be taken with the timing to insure that data outputs are TRI-STATE during address or data input times. The falling edge of $\overline{E}$ latches the address and $\overline{S}$ inputs and initiates the cycle. $\overline{W}$ going LOW latches and writes the data in. While $\overline{W}$ is LOW, $\overline{E}$ may either return HIGH or remain LOW. The latter of the $\overline{W}$ or $\overline{E}$ rising edges terminates the cycle.

Self Refresh Operation

The NMC4864 must be refreshed with 256 refresh cycles every 4 ms. One of three refresh modes may be chosen to meet this requirement which provide transparent refresh in most circumstances. During active operation two refresh approaches are available which depend on the user's cycle time requirements. These are the double cycle mode and the short cycle mode. The third refresh mode is for standby and single step operation where long periods occur between clocking, including up to infinite cycle time.

Double Cycle Refresh Mode

For cycle times greater than TELEL (min, double cycle model), the double cycle self refresh mode may be selected by a LOW input on $\overline{F}$ ($\overline{RFSH}$) at the start of the cycle. This input is latched by $\overline{E}$, $\overline{R}$, or $\overline{W}$ but may be tied permanently LOW if the cycle time is less than 10 μs.

In this mode every read/write cycle is automatically followed by a refresh operation to both array halves. This refresh is totally transparent to the user since both timing and refresh address are internally created. The data (D/Q) pins are not affected by this refresh operation and remain under control of the $\overline{R}$ and $\overline{W}$ pins. When $\overline{E}$, $\overline{R}$ and $\overline{W}$ are clocked with the part deselected ($\overline{S}$ = HIGH), only the refresh operation is done.

This double cycle self refresh mode is the best for microprocessor applications where the cycle time normally exceeds 500 ns. No data interruption is required for refresh with this refresh mode. The only requirement for this mode is that 256 memory cycles (selected or deselected) be done for each 4 ms time period.

Short Cycle Refresh Mode

This self refresh mode allows highest speed operation with cycle times down to TELEL(min, short cycle mode). This mode is selected by pulling the $\overline{F}$ ($\overline{RFSH}$) pin HIGH through a pull up resistor (1 kΩ, typ) which allows wire-OR connections of the $\overline{F}$ outputs from several NMC4864 devices.

Functional Description (Continued)

For the short cycle self refresh mode the required 256 refresh cycles per 4 ms to both array halves will automatically be provided as long as the average cycle time, TELEL, over any 4 ms is less than 820 ns according to the following equation.

$$\text{TELEL(average)} = \frac{\text{TREF}}{(19 \times 256)}$$

where TREF = 4 ms

This mode utilizes the split array architecture to perform refresh on the non-addressed half and read/write on the addressed half simultaneously as determined by the least significant address input, A0. The details concerning the operation of this refresh mode follow.

Each $\overline{E}$, $\overline{R}$ or $\overline{W}$ cycle when deselected ($\overline{S}$ = HIGH) refreshes both array halves and increments the internal refresh address.

Each $\overline{E}$, $\overline{R}$ or $\overline{W}$ cycle when selected ($\overline{S}$ = LOW) refreshes the array half not addressed by A0 and performs the read/write operation to the other half. The refresh address is incremented after each time both array halves are selected.

In this mode normal memory activity will perform the required 256 refresh cycles to each half for each 4 ms period. In the unlikely event that a long string of all odd or even addresses occurs, a built in cycle counter is provided to guarantee adequate refresh. Should 18 continuous cycles be selected ($\overline{S}$ = LOW) with address A0 either always LOW or always HIGH then on the 19th cycle the $\overline{F}$ output will be pulled LOW to request a double length cycle *(Figure 3)*. Refresh will be done automatically to both halves just as in the double cycle mode. The $\overline{F}$ pin returns to open (allowing it to go HIGH) when the refresh is completed.

The $\overline{F}$ pin in this mode may be tied to the READY or WAIT input *(Figure 4)* on most microprocessors. This is a convenient method by which the memory cycle time may be lengthened to allow for the double length cycle only when required.

Standby/Single Step Auto Refresh Mode

This mode completes the pseudo-static nature of the NMC4864 allowing it to be used for most static RAM applications. In particular, this mode is ideal for applications requiring very long periods with no clocks being cycled such as in single step operation or during microprocessor power down.

The standby mode *(Figure 5)* is entered if $\overline{F}$ (RFSH) is held LOW for 100 μs uninterrupted by active cycles. Each active cycle restarts the timer when $\overline{F}$ is LOW. This standby/single step mode is entered 100 microseconds after the latter of the falling edge of $\overline{F}$ or the start of the last $\overline{E}$, $\overline{R}$ or $\overline{W}$ cycle.

During standby mode all other read/write timing specifications apply except for the maximum active pulse widths for $\overline{E}$, $\overline{R}$ and $\overline{W}$ which may be HIGH or LOW during standby, but must not be cycled. While $\overline{R}$ remains LOW from the cycle entering standby the outputs remain valid without time limit. If the cycle entering standby was deselected ($\overline{S}$ = HIGH) or if $\overline{R}$ is HIGH the outputs remain TRI-STATE. The internal auto refresh cycle occurs every 15 μs during standby. This minimizes standby power while refreshing the memory every 3.84 ms.

Exit from standby/single step mode is best done by returning $\overline{F}$ HIGH before the next active cycle by the time TFHEL. $\overline{F}$ need only remain HIGH for time TFHFL which allows for short or double cycle mode selection on the first active cycle after standby mode termination. This method of standby exit provides a safe exit from the asynchronous internal refresh operations during standby, with zero error probability.

Power Up Characteristics

The NMC4864 has an internal substrate bias generator that requires up to 500 ns to reach its functional level. In addition, the device requires up to 128 cycles to initialize the internal clock chain.

Therefore, it is necessary for the system designer to provide a delay of at least 500 ns after VCC reaches 4.5V followed by a minimum of 128 dummy cycles. These 128 dummy cycles must also be provided following a violation of refresh timing. Any 128 read or write cycles satisfies this requirement regardless of whether or not the chip is selected.

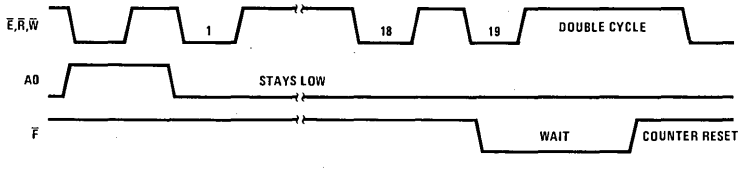


FIGURE 3. Short Cycle Auto Refresh Timing

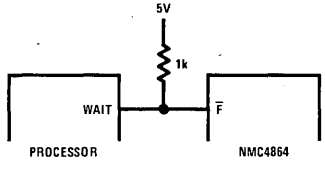


FIGURE 4. Circuit for Short Cycle

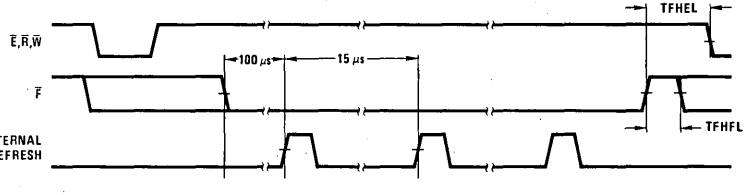


FIGURE 5. Standby/Single Step Auto Refresh Mode

National Semiconductor

NMOS RAMs
PREVIEW

NMC6132 32k Pseudo-Static NMOS RAM

General Description

The NMC6132 is a single 5V power supply pseudo-static NMOS RAM organized as 4096 words by 8 bits. The circuit uses single-transistor dynamic storage cells with internal refresh control to make the part appear static to the user. The byte-wide (8-bit input/output) organization makes this RAM ideal for microprocessor applications.

The NMC6132 has separate address and data I/O pins for use with either separate or multiplexed address/data buses.

The NMC6132 has a bidirectional refresh status and control pin $\overline{F}$ ($\overline{RFSH}$). Use of this pin selects either of two cycle initiated refresh modes.

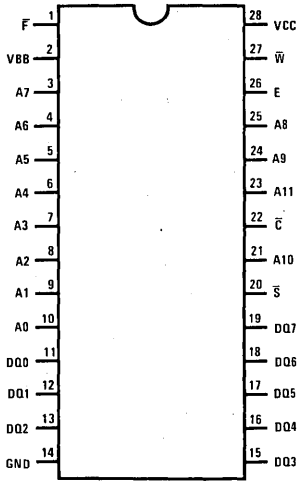
The NMC6132 is packaged in a standard 28-pin DIP with the JEDEC proposed standard pinout. This pinout is EPROM/ROM compatible with minimal modification.

Features

- 4096 words x 8 bit organization
- High performance
  - Access time—200 ns
  - Cycle time—350 ns
- Low power: 200 mW active, 125 mW standby
- 128 refresh cycles/2 ms automatically provided
- Single 5V 10% power supply with on-chip substrate bias generator
- Automatic self refresh with fast and slow cycle modes
- Standard 28-pin DIP with JEDEC proposed pinout
- Pinout ROM/EPROM compatible

Connection Diagram

Dual-In-Line Package



TOP VIEW

Pin Names

A0-A12	Address Inputs
E	Address Latch Enable
$\overline{C}$	Data Strobe
$\overline{W}$	Write
$\overline{S}$	Chip Select
DQ0-DQ7	Data Input/Output (TRI-STATE®)
$\overline{F}$ ($\overline{RFSH}$)	Refresh (Bidirectional)
VCC	Power Supply
VSS	Ground
VBB	Substrate Bias Output

Dynamic RAMs

National Semiconductor

NMOS RAMs

MM4280 4096-Bit (4096 x 1) Extended Temperature Range Dynamic RAM

General Description

National's MM4280 is a 4096 word by 1 bit dynamic RAM. It incorporates the latest memory design features and can be used in a wide variety of applications, from those which require very high speed to ones where low cost and large bit capacity are the prime criteria.

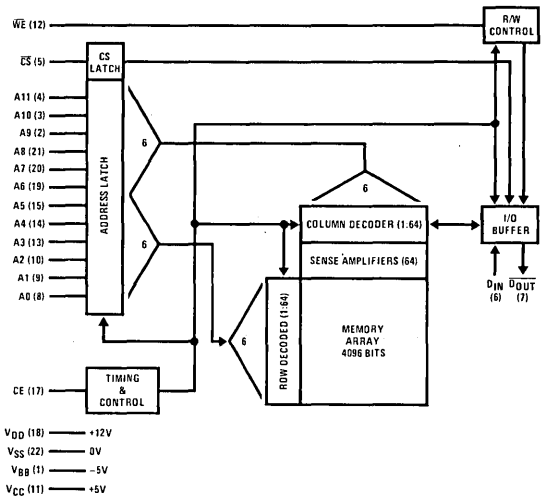
The MM4280 must be refreshed every 1 ms. This can be accomplished by performing a read cycle at each of the 64 row addresses (A0–A5). The chip select input can be either high or low for refresh. Addresses (A6–A11) must have a stable address during the refresh cycle. Any address is satisfactory as long as the address set-up and hold times are met. The chip select input can be either high or low for refresh.

The MM4280 has been designed with minimum production costs as a prime criterion. It is fabricated using N-channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits. The MM4280 uses a single transistor cell to minimize the device area. The single device cell, along with unique design features in the on-chip peripheral circuits, yields a high performance memory device.

Features

- Extended temperature range: −55°C to +85°C
- Organization: 4096 x 1
- Access time 270 ns maximum
- Cycle time 470 ns minimum
- Easy system interface
  - One high voltage input—chip enable
  - TTL compatible—all other inputs and outputs
- Address registers on-chip
- TRI-STATE® output
- Simple read-modify-write operation
- Industry standard pin configuration

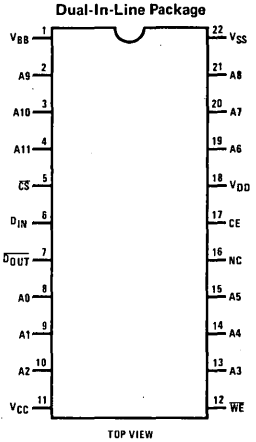
Block Diagram



Memory Inverts From Data In to Data Out

Connection Diagram

Dual-In-Line Package

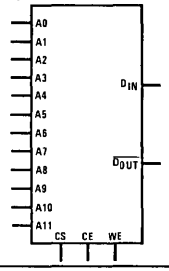


TOP VIEW

Order Number MM4280D
See NS Package D22B

Order Number MM4280J
See NS Package J22A

Logic Symbol



Pin Names

A0–A11	Address Inputs *	V_{BB}	Power (−5V)
CE	Chip Enable	V_{CC}	Power (+5V)
$\overline{CS}$	Chip Select	V_{DD}	Power (+12V)
D_{IN}	Data Input	V_{SS}	Ground
$\overline{D_{OUT}}$	Data Output	$\overline{WE}$	Write Enable
NC	Not Connected		

* Refresh Address A0–A5

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Voltage on any Pin Relative to V_{BB} ($V_{SS} - V_{BB} \geq 4.5V$)	−0.3V to +20V
Power Dissipation	1.25W

Operating Conditions

	MIN	MAX	UNITS
Operating Temperature Range	−55	+85	°C
V_{DD} Voltage	11.4	12.6	V
V_{CC} Voltage	4.75	5.25	V
V_{BB} Voltage	−5.5	−4.5	V

DC Electrical Characteristics

$T_A = -55°C$ to $+85°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, V_{BB} (Note 2) $= -5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Input Load Current	$V_{IN} = 0V$ to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	$V_{IN} = 0V$ to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC} or $\overline{CS} = V_{IH}$, $V_O = 0V$ to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to 0.6V, (Note 4)		110	300	μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, $T_A = 25°C$		20	50	mA
I_{DDAV1}	Average V_{DD} Current	Cycle Time = 470 ns, t_{CE} = 300 ns		35	70	mA
I_{CC1}	V_{CC} Supply Current During CE "OFF"	CE = V_{ILC} or $\overline{CS} = V_{IH}$ (Note 5)		0.01	10	μA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	$t_T = 20$ ns	−1.0		0.6	V
V_{IH}	Input High Voltage		2.2		$V_{CC}+1$	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		$V_{DD}-1$		$V_{DD}+1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2$ mA	0		0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -2$ mA	2.4		V_{CC}	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages referenced to V_{SS} and V_{BB} must be applied before and removed after other supply voltages.

Note 3: Typical values are for $T_A = 25°C$ and nominal power supply voltages.

Note 4: The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.

Note 5: During CE "ON" V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

AC Electrical Characteristics $T_A = -55°C$ to $+85°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 10\%$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				1	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		100			ns
t_{CC}	CE "OFF" Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
READ CYCLE						
t_{CY}	Cycle Time		470			ns
t_{CE}	CE "ON" Time		300		3000	ns
t_{CO}	CE Output Delay	$C_{LOAD} = 50$ pF, Load = 1 TTL Gate, Ref = 2V,			250	ns
t_{ACC}	Address to Output Access	$t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$			270	ns
t_{WL}	CE to $\overline{WE}$		0			ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns

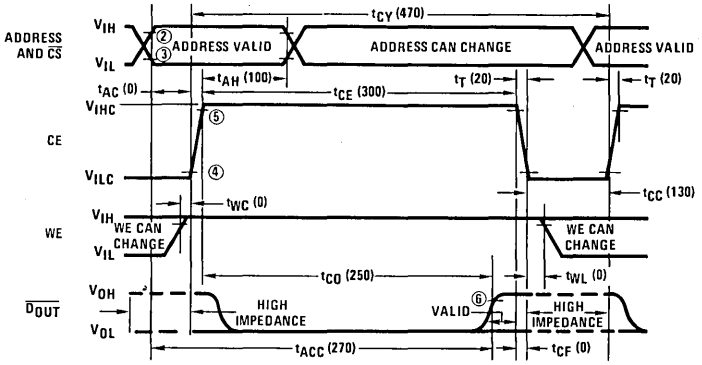
AC Electrical Characteristics (Continued)

$T_A = -55°C$ to $+85°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = 5V \pm 10\%$

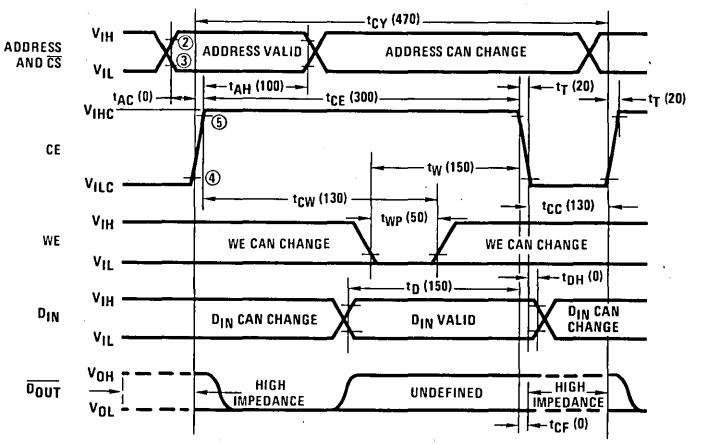
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE						
t_{CY}	Cycle Time		470			ns
t_{CE}	CE "ON" Time		300		3000	ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{CW}	CE to $\overline{WE}$	$t_T = 20$ ns	130			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	$\overline{WE}$ Pulse Width		50			ns

Switching Time Waveforms

Read and Refresh Cycle ①



Write Cycle



Note 1: For refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
Note 2: V_{IL} max is the reference level for measuring timing of the address, $\overline{CS}$ and D_{IN}.
Note 3: V_{IH} min is the reference level for measuring timing of the addresses, $\overline{CS}$ and D_{IN}.
Note 4: $V_{SS} + 2V$ is the reference level for measuring timing of CE.
Note 5: $V_{DD} - 2V$ is the reference level for measuring timing of CE.
Note 6: $V_{SS} + 2V$ is the reference level for measuring the timing of D_{OUT} for a high output.

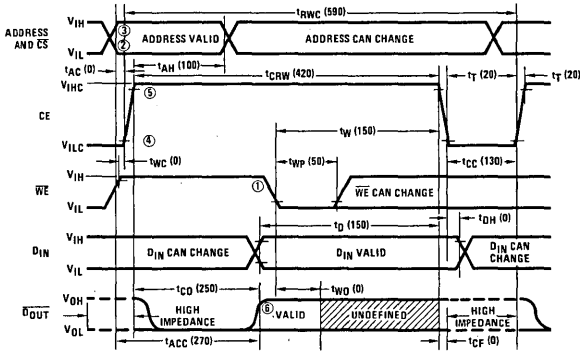
AC Electrical Characteristics (Continued) $T_A = -55°C$ to $+85°C$, $V_{DD} = 12V \pm 5V \pm 5\%$, $V_{BB} = -5V \pm 10\%$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read/Modify/Write (RMW) Cycle Time		590			ns
t_{CRW}	CE Width During RMW		420		3000	ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{WP}	$\overline{WE}$ Pulse Width	t_T = 20 ns, C_{LOAD} = 50 pF, Load = 1 TTL Gate, Ref = 2V, $t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$	50			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				250	ns
t_{WO}	$\overline{WE}$ to $\overline{D_{OUT}}$ Invalid		0			ns
t_{ACC}	Access Time				270	ns
CAPACITANCE (Note 1) $T_A = 25°C$						
C_{AD}	Address Capacitance, CS	$V_{IN} = V_{SS}$		2	6	pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15	25	pF
C_{OUT}	Data Output Capacitance	$V_{OUT} = 0V$		5	10	pF
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	$V_{IN} = V_{SS}$		4	6	pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

Switching Time Waveforms (Continued)

Read Modify Write Cycle



Note 1: $\overline{WE}$ must be high until end of t_{CO}.

Note 2: V_{IL} max is the reference level for measuring timing of the address, $\overline{CS}$, D_{IN} and $\overline{WE}$.

Note 3: V_{IH} min is the reference level for measuring timing of the address, $\overline{CS}$, D_{IN} and $\overline{WE}$.

Note 4: $V_{SS} + 2V$ is the reference level for measuring timing of CE.

Note 5: $V_{DD} - 2V$ is the reference level for measuring timing of CE.

Note 6: $V_{SS} + 2V$ is the reference level for measuring the timing of $\overline{D_{OUT}}$ for a high output.

National Semiconductor

NMOS RAMs

MM5280 4096-Bit (4096 x 1) Dynamic RAM

General Description

National's MM5280 is a 4096 word by 1 bit dynamic RAM. It incorporates the latest memory design features and can be used in a wide variety of applications, from those which require very high speed to ones where low cost and large bit capacity are the prime criteria.

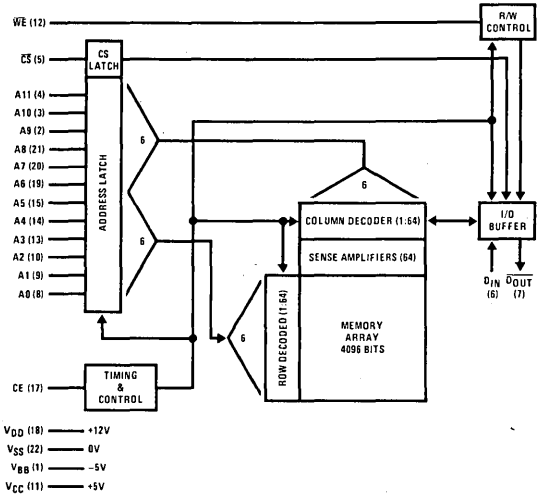
The MM5280 must be refreshed every 2 ms. This can be accomplished by performing a read cycle at each of the 64 row addresses (A0–A5). The chip select input can be either high or low for refresh.

The MM5280 has been designed with minimum production costs as a prime criterion. It is fabricated using N-channel silicon gate MOS technology, which is an ideal choice for high density integrated circuits. The MM5280 uses a single transistor cell to minimize the device area. The single device cell, along with unique design features in the on-chip peripheral circuits, yields a high performance memory device.

Features

- Organization: 4096 x 1
- Access time 200 ns maximum
- Cycle time 400 ns minimum
- Easy system interface
  - One high voltage input–chip enable
  - TTL compatible–all other inputs and output
- Address registers on-chip
- TRI-STATE® output
- Simple read-modify-write operation
- Industry standard pin configuration

Block Diagram



Memory Inverts From Data In to Data Out

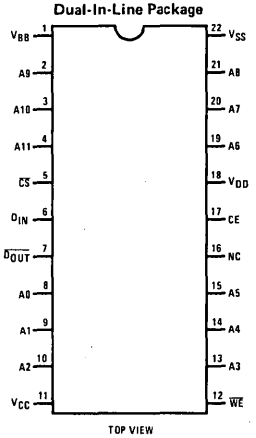
Pin Names

A0–A11	Address Inputs *	V_{BB}	Power (−5V)
CE	Chip Enable	V_{CC}	Power (+5V)
$\overline{CS}$	Chip Select	V_{DD}	Power (+12V)
D_{IN}	Data Input	V_{SS}	Ground
$\overline{D_{OUT}}$	Data Output	$\overline{WE}$	Write Enable
NC	Not Connected		

* Refresh Address A0–A5

Connection Diagram

Dual-In-Line Package

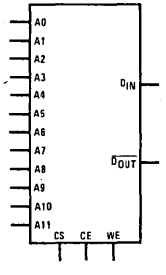


TOP VIEW

Order Number MM5280N See NS Package N22A

Order Number MM5280J See NS Package J22A

Logic Symbol



Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V
Supply Voltages V_{DD}, V_{CC} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.25W

Operating Conditions

	MIN	MAX	UNITS
Operating Temperature Range	0	+70	°C
V_{DD} Voltage	10.8	13.2	V
V_{CC} Voltage	4.5	5.5	V
V_{BB} Voltage	−5.5	−4.5	V

DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} (Note 2) = −5V ±10%, V_{SS} = 0V, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +6V, Note 4		110	300	μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, T_A = 25°C		20	40	mA
$I_{DD\ AV1}$	Average V_{DD} Current	T_A = 25°C Cycle Time = 400 ns, t_{CE} = 230 ns		35	60	mA
$I_{DD\ AV2}$	Average V_{DD} Current	T_A = 25°C Cycle Time = 1000 ns, t_{CE} = 230 ns		15	30	mA
I_{CC1}	V_{CC} Supply Current During CE "OFF"	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, (Note 5)		0.01	10	μA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns *(Figure 4)*	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V_{CC}	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for T_A = 25°C and nominal power supply voltages.

Note 4: The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.

Note 5: During CE "ON" V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

AC Electrical Characteristics T_A = 0°C to +70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ±10%, V_{BB} = −5V ±10%

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		50			ns
t_{CC}	CE "OFF" Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
READ CYCLE						
t_{CY}	Cycle Time		400			ns
t_{CE}	CE "ON" Time		230		3000	ns
t_{CO}	CE Output Delay	C_{LOAD} = 50 pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$			180	ns
t_{ACC}	Address to Output Access				200	ns
t_{WL}	CE to $\overline{WE}$		0			ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns

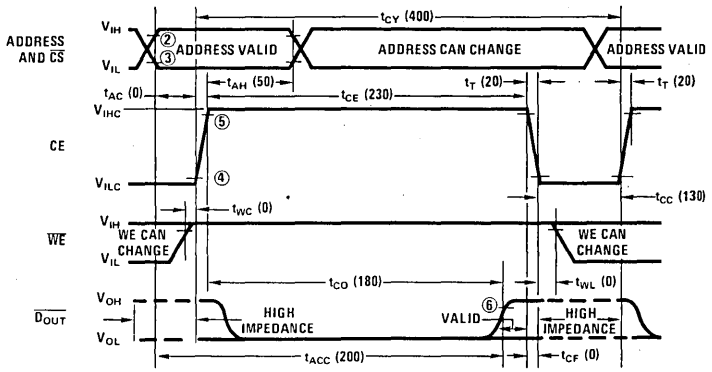
AC Electrical Characteristics (Continued)

$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5\% \pm 10\%$

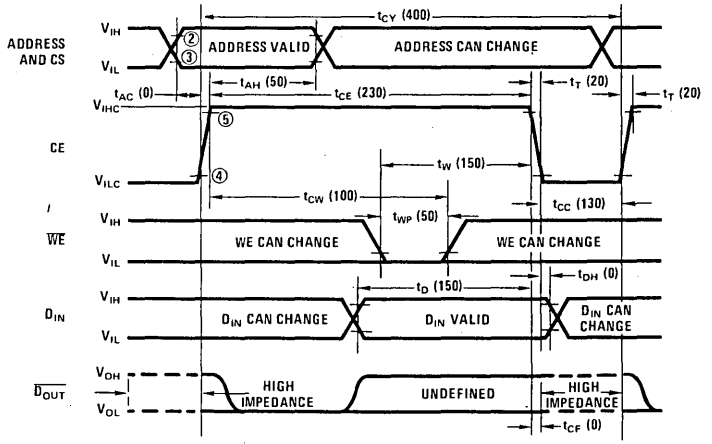
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WRITE CYCLE						
t_{CY}	Cycle Time		400			ns
t_{CE}	CE "ON" Time		230		3000	ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{CW}	CE to $\overline{WE}$	t_T = 20 ns	100			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	$\overline{WE}$ Pulse Width		50			ns

Switching Time Waveforms

Read and Refresh Cycle①



Write Cycle



Note 1: For refresh cycle, row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
Note 2: V_{IL} max is the reference level for measuring timing of the address, $\overline{CS}$ and D_{IN}.
Note 3: V_{IH} min is the reference level for measuring timing of the addresses, $\overline{CS}$ and D_{IN}.
Note 4: V_{SS} + 2.0V is the reference level for measuring timing of CE.
Note 5: V_{DD} − 2V is the reference level for measuring timing of CE.
Note 6: V_{SS} + 2.0V is the reference level for measuring the timing of D_{OUT} for a high output.

AC Electrical Characteristics (Continued)

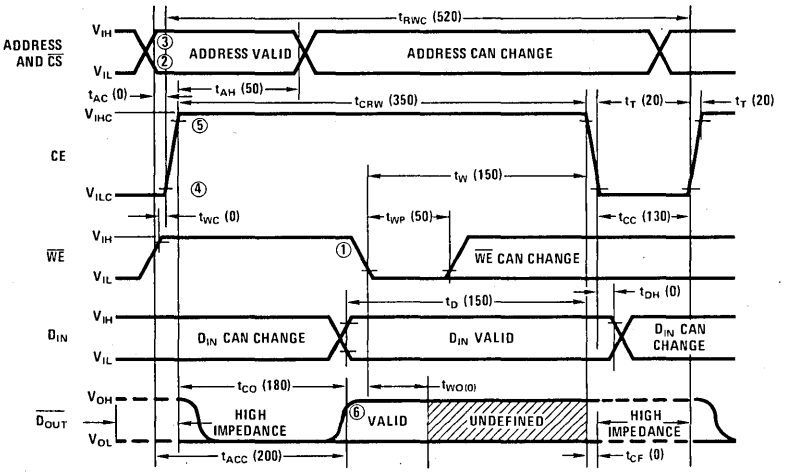
$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{BB} = -5\% \pm 10\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time		520			ns
t_{CRW}	CE Width During RMW		350		3000	ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{WP}	$\overline{WE}$ Pulse Width	$t_T = 20$ ns, $C_{LOAD} = 50$ pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO} + 1\ t_T$	50			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				180	ns
t_{WO}	$\overline{WE}$ to $\overline{D_{OUT}}$ Invalid		0			
t_{ACC}	Access Time				200	ns
CAPACITANCE (Note 1)		$T_A = 25°C$				
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15		pF
C_{OUT}	Data Output Capacitance	$V_{OUT} = 0V$		5		pF
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	$V_{IN} = V_{SS}$		4		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

Switching Time Waveforms (Continued)

Read Modify Write Cycle



Note 1: $\overline{WE}$ must be high until end of t_{CO}.
Note 2: V_{IL} max is the reference level for measuring timing of the address, $\overline{CS}$, D_{IN} and $\overline{WE}$.
Note 3: V_{IH} min is the reference level for measuring timing of the address, $\overline{CS}$, D_{IN} and $\overline{WE}$.
Note 4: $V_{SS} + 2.0V$ is the reference level for measuring timing of CE.
Note 5: $V_{DD} - 2V$ is the reference level for measuring timing of CE.
Note 6: $V_{SS} + 2.0V$ is the reference level for measuring the timing of $\overline{D_{OUT}}$ for a high output.

National Semiconductor

NMOS RAMs

MM5280-5 4096-Bit (4096 x 1) Dynamic RAM

General Description

The MM5280-5 is a slower speed version of National's MM5280. Please refer to the MM5280 specification for pin configuration, block diagram and switching time waveforms.

Features

- Access time—270 ns
- Cycle time—470 ns

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to the Most Negative Supply Voltage, V_{BB}	−0.3V to +25V
Supply Voltages V_{DD}, V_{CC} and V_{SS} with Respect to V_{BB}	−0.3V to +20V
Power Dissipation	1.25W

Operating Conditions

	MIN	MAX	UNITS
Operating Temperature Range	0	+70	°C
V_{DD} Voltage	11.4	12.6	V
V_{CC} Voltage	4.75	5.25	V
V_{BB} Voltage	−5.25	−4.75	V

Order Number MM5280J-5
See NS Package J22A

Order Number MM5280N-5
See NS Package N22A

DC Electrical Characteristics

$T_A = 0°C$ to $+70°C$ $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, V_{BB} (Note 2) $= -5V \pm 5\%$, $V_{SS} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 0V to V_{IH} max, (All Inputs Except CE)		0.01	10	μA
I_{LC}	Input Load Current	V_{IN} = 0V to V_{IHC} max		0.01	10	μA
$\|I_{LO}\|$	Output Leakage Current Up For High Impedance State	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, V_O = 0V to 5.25V		0.01	10	μA
I_{DD1}	V_{DD} Supply Current During CE "OFF"	CE = −1V to +6V, Note 4		110	300	μA
I_{DD2}	V_{DD} Supply Current During CE "ON"	CE = V_{IHC}, $T_A = 25°C$		20	40	mA
$I_{DD\ AV1}$	Average V_{DD} Current	$T_A = 25°C$ Cycle Time = 400 ns, t_{CE} = 230 ns		35	60	mA
$I_{DD\ AV2}$	Average V_{DD} Current	$T_A = 25°C$ Cycle Time = 1000 ns, t_{CE} = 230 ns		15	30	mA
I_{CC1}	V_{CC} Supply Current During CE "OFF"	CE = V_{ILC} or $\overline{CS}$ = V_{IH}, (Note 5)		0.01	10	μA
I_{BB}	V_{BB} Supply Current Average			5	100	μA
V_{IL}	Input Low Voltage	t_T = 20 ns	−1.0		0.6	V
V_{IH}	Input High Voltage		2.4		V_{CC}+1	V
V_{ILC}	CE Input Low Voltage		−1.0		1.0	V
V_{IHC}	CE Input High Voltage		V_{DD}−1		V_{DD}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	0.0		0.45	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V_{CC}	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Typical values are for $T_A = 25°C$ and nominal power supply voltages.

Note 4: The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.

Note 5: During CE "ON" V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.

AC Electrical Characteristics

$T_A = 0°C$ to $+70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ, WRITE, READ/MODIFY/WRITE, AND REFRESH CYCLE						
t_{REF}	Time Between Refresh				2	ms
t_{AC}	Address to CE Set-Up Time	t_{AC} is Measured From End of Address Transition	0			ns
t_{AH}	Address Hold Time		50			ns
t_{CC}	CE "OFF" Time		130			ns
t_T	CE Transition Time		10		40	ns
t_{CF}	CE "OFF" to Output High Impedance State		0			ns
READ CYCLE						
t_{CY}	Cycle Time		470			ns
t_{CE}	CE "ON" Time		300		3000	ns
t_{CO}	CE Output Delay	C_{LOAD} = 50 pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO} + 1\,t_T$			250	ns
t_{ACC}	Address to Output Access				270	ns
t_{WL}	CE to $\overline{WE}$		0			ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns
WRITE CYCLE						
t_{CY}	Cycle Time		470			ns
t_{CE}	CE "ON" Time		300		3000	ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{CW}	CE to $\overline{WE}$	t_T = 20 ns	130			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{WP}	$\overline{WE}$ Pulse Width		50			ns
READ/MODIFY/WRITE CYCLE						
t_{RWC}	Read Modify Write (RMW) Cycle Time		590			ns
t_{CRW}	CE Width During RMW		420		3000	ns
t_{WC}	$\overline{WE}$ to CE "ON"		0			ns
t_W	$\overline{WE}$ to CE "OFF"		150			ns
t_{WP}	$\overline{WE}$ Pulse Width	t_T = 20 ns, C_{LOAD} = 50 pF, Load = 1 TTL Gate, Ref = 2.0V, $t_{ACC} = t_{AC} + t_{CO} + 1\,t_T$	50			ns
t_D	D_{IN} to CE Set-Up		150			ns
t_{DH}	D_{IN} Hold Time		0			ns
t_{CO}	CE to Output Delay				250	ns
t_{WO}	$\overline{WE}$ to $\overline{D_{OUT}}$ Invalid		0			
t_{ACC}	Access Time				270	ns
CAPACITANCE (Note 1)		$T_A = 25°C$				
C_{AD}	Address Capacitance, $\overline{CS}$	$V_{IN} = V_{SS}$		2		pF
C_{CE}	CE Capacitance	$V_{IN} = V_{SS}$		15		pF
C_{OUT}	Data Output Capacitance	$V_{OUT} = 0V$		5		pF
C_{IN}	D_{IN} and $\overline{WE}$ Capacitance	$V_{IN} = V_{SS}$		4		pF

Note 1: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$ with the current equal to a constant 20 mA.

National Semiconductor

NMOS RAMs

MM5290*16,384-Bit (16,384 x 1) Dynamic RAM

General Description

The MM5290 is a 16,384 x 1 bit dynamic RAM. It features a multiplexed address input with separate row and column strobes. This added flexibility allows the MM5290 to be used in page mode operation.

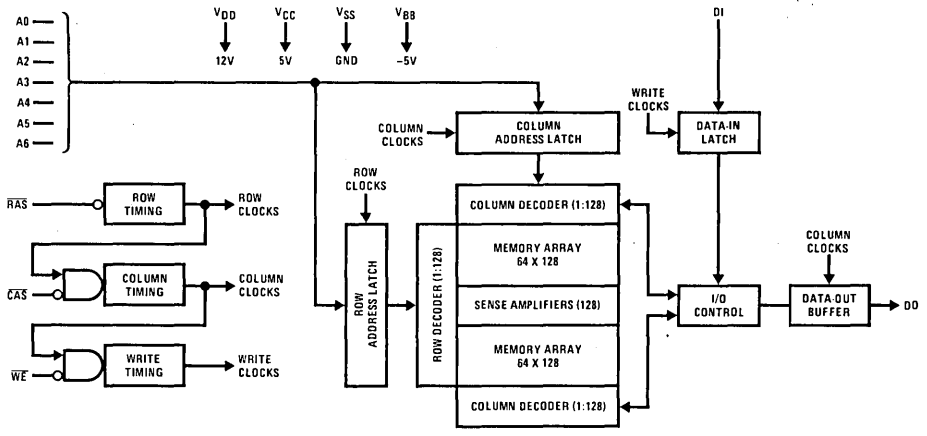
The MM5290 must be refreshed every 2 ms. This can be accomplished by performing any cycle which brings the Row Address Strobe active including a $\overline{RAS}$-only cycle at each of the 128 row addresses.

N-channel double-poly silicon gate technology, developed by National, is used in the manufacture of the MM5290. This process combines high density and performance with reliability. Greater system densities are achievable by the use of a 16-pin dual-in-line package for the MM5290.

Features

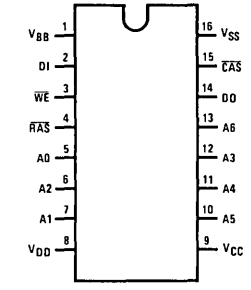
- Access times: 150 ns, 200 ns, 250 ns
- Low power: 528 mW max
- TTL compatible: all inputs and output
- Gated $\overline{CAS}$–noncritical timing
- Read, Write, Read-Modify-Write and $\overline{RAS}$-only Refresh cycles
- Page mode operation
- Industry standard 16-pin configuration

Block Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

*See the MST™ Program page 3.

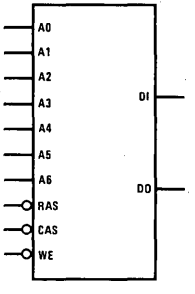
Pin Names

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0–A6	Address Inputs
DI	Data Input
DO	Data Output
V_{DD}	Power (12V)
V_{CC}	Power (5V)
V_{SS}	Ground
V_{BB}	Power (−5V)

Order Number MM5290J-2, MM5290J-3, or MM5290J-4
See NS Package J16A

Order Number MM5290N-2, MM5290N-3, or MM5290N-4
See NS Package N16A

Logic Diagram



Absolute Maximum Ratings (Note 1)

Storage Temperature −65°C to +150°C
Power Dissipation 1W
Voltage on Any Pin Relative to V_{BB} −0.3V to +20V
($V_{SS} - V_{BB} \geq 4.5V$)
Lead Temperature (Soldering, 10 seconds) 300°C

Recommended DC Operating Conditions

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
T_A	Ambient Temperature	0	70	°C	
V_{DD}	Supply Voltages	10.8	13.2	V	2, 3
V_{CC}		4.5	5.5	V	2, 3
V_{SS}		0	0	V	2, 3
V_{BB}		−4.5	−5.5	V	2, 3
V_{IHC}	Input High Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	2.7	7.0	V	2
V_{IH}	Input High Voltage, A0–A6, DI	2.4	7.0	V	2
V_{IL}	Input Low Voltage, All Inputs	−1.0	0.8	V	2

DC Electrical Characteristics Over the range of Recommended DC Operating Conditions unless otherwise noted

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DD1}	**Operating Current**		35	mA	4
I_{CC1}	Average Power Supply Operating Current				5
I_{BB1}	($\overline{RAS}$, $\overline{CAS}$ Cycling; t_{RC} = t_{RC} MIN)		200	μA	
I_{DD2}	**Standby Current**		1.5	mA	
I_{CC2}	Power Supply Standby Current ($\overline{RAS}$ = V_{IHC},	−10	10	μA	
I_{BB2}	DO = High Impedance)		100	μA	
I_{DD3}	**Refresh Current**		25	mA	4
I_{CC3}	Average Power Supply Current, Refresh Mode	−10	10	μA	
I_{BB3}	($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = t_{RC} MIN)		200	μA	
I_{DD4}	**Page Mode Current**		27	mA	4
I_{CC4}	Average Power Supply Current, Page Mode				5
I_{BB4}	($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling; t_{PC} = 225 ns)		200	μA	
$I_{I(L)}$	**Input Leakage** Input Leakage Current, Any Input (V_{BB} = −5V, 0V ≤ V_{IN} ≤ 7V, All Other Pins not Under Test = 0V)	−10	10	μA	
$I_{O(L)}$	**Output Leakage** Output Leakage Current (DO is Disabled, 0V ≤ V_{OUT} ≤ 5.5V)	−10	10	μA	
	Output Levels				
V_{OH}	Output High Voltage (I_{OUT} = −5 mA)	2.4		V	
V_{OL}	Output Low Voltage (I_{OUT} = 4.2 mA)		0.4	V	
CAPACITANCE					
C_I	Input Capacitance A0–A6, DI		5	pF	6
C_C	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$		10	pF	6
C_O	Output Capacitance, DO		7	pF	6

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Recommended DC Operating Conditions" provides conditions for actual device operation.

Note 2: All voltages referenced to V_{SS}. When applying voltages to the device, V_{DD}, V_{CC} or V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Several cycles are required after power-up before proper device operation is achieved. Any 8 RAS cycles are adequate for this purpose.

Note 4: I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate.

Note 5: I_{CC} depends on output load.

Note 6: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$. Capacitance is guaranteed by periodic testing.

AC Electrical Characteristics

Over the range of Recommended DC Operating Conditions unless otherwise noted

SYMBOL	PARAMETER	MM5290-2		MM5290-3		MM5290-4		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	375		375		410		ns	7, 8
t_{RWC}	Read-Write Cycle Time	375		375		515		ns	7, 8
t_{PC}	Page Mode Cycle Time	170		225		275		ns	
t_{RAC}	Access Time from $\overline{RAS}$		150		200		250	ns	9, 11
t_{CAC}	Access Time from $\overline{CAS}$		100		135		165	ns	10, 11
t_{OFF}	Output Buffer Turn-Off Delay	0	40	0	50	0	60	ns	12
t_T	Transition Time (Rise and Fall)	3	35	3	50	3	50	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	100		120		150		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10,000	200	10,000	250	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	100		135		165		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	150		200		250		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	100	10,000	135	10,000	165	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	65	35	85	ns	9
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	−20		−20		−20		ns	
t_{ASR}	Row Address Set-Up Time	0		0		0		ns	
t_{RAH}	Row Address Hold Time	20		25		35		ns	
t_{ASC}	Column Address Set-Up Time	−10		−10		−10		ns	
t_{CAH}	Column Address Hold Time	45		55		75		ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{RCS}	Read Command Set-Up Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{WCH}	Write Command Hold Time	45		55		75		ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{WP}	Write Command Pulse Width	45		55		75		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	60		80		100		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	60		80		100		ns	
t_{DS}	Data-In Set-Up Time	0		0		0		ns	13, 14
t_{DH}	Data-In Hold Time	45		55		75		ns	13, 14
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (for Page Mode Cycle Only)	60		80		100		ns	
t_{REF}	Refresh Period		2		2		2	ms	
t_{WCS}	$\overline{WE}$ to $\overline{CAS}$ Set-Up Time	−20		−20		−20		ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	70		95		125		ns	15
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	120		160		200		ns	15

Note 7: The specifications for $t_{RC(MIN)}$ and $t_{RWC(MIN)}$ are used only to indicate cycle time at which proper operation over the full temperature range is guaranteed.

Note 8: Transition times are measured between V_{IHC} or V_{IH} and V_{IL}. Timing measurements are made between $V_{IHC(MIN)}$ or $V_{IH(MIN)}$ and $V_{IL(MAX)}$, and assume $t_T = 5$ ns.

Note 9: Assumes row-limited access, i.e., $t_{RCD} \leq t_{RCD(MAX)}$. If this condition is not satisfied, then note 10 applies.

Note 10: Assumes column-limited access, i.e., $t_{RCD} > t_{RCD(MAX)}$.

Note 11: Equivalent load is 2 standard TTL inputs plus 100 pF.

Note 12: $\overline{CAS}$ going high disables the Data Output. t_{OFF} is the delay to the high impedance state.

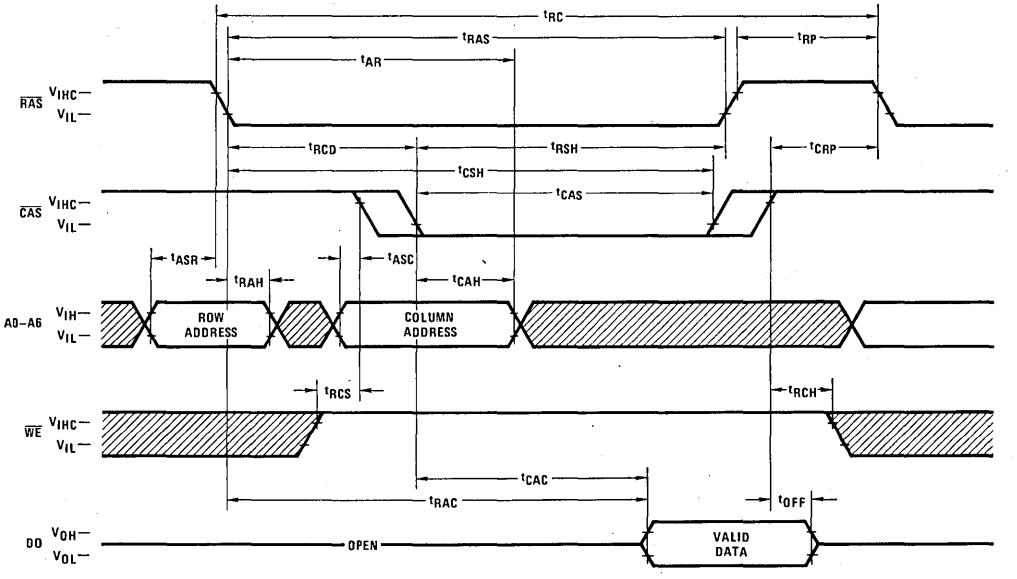
Note 13: These parameters are referenced to the negative edge of $\overline{CAS}$ in an early-write cycle and to the negative edge of $\overline{WE}$ in a Read-Modify-Write cycle. (See Note 12).

Note 14: If $t_{WCS} \geq t_{WCS(MIN)}$, the Data Output is guaranteed to remain in the high impedance state for the duration of the cycle. This is the "early-write" cycle.

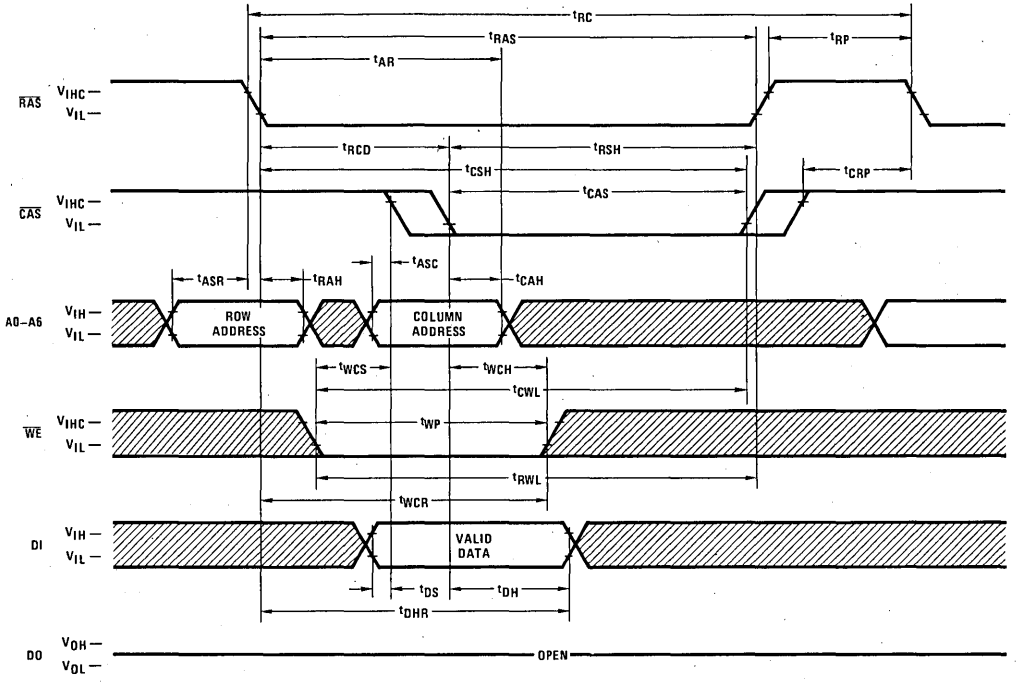
Note 15: If $t_{CWD} \geq t_{CWD(MIN)}$ and $t_{RWD} \geq t_{RWD(MIN)}$, the Data Output will contain the original data in the selected cell. This is the Read-Modify-Write cycle. If either of these conditions is not satisfied, the output will be indeterminate unless the early-write condition of Note 12 is met.

Switching Time Waveforms

Read Cycle

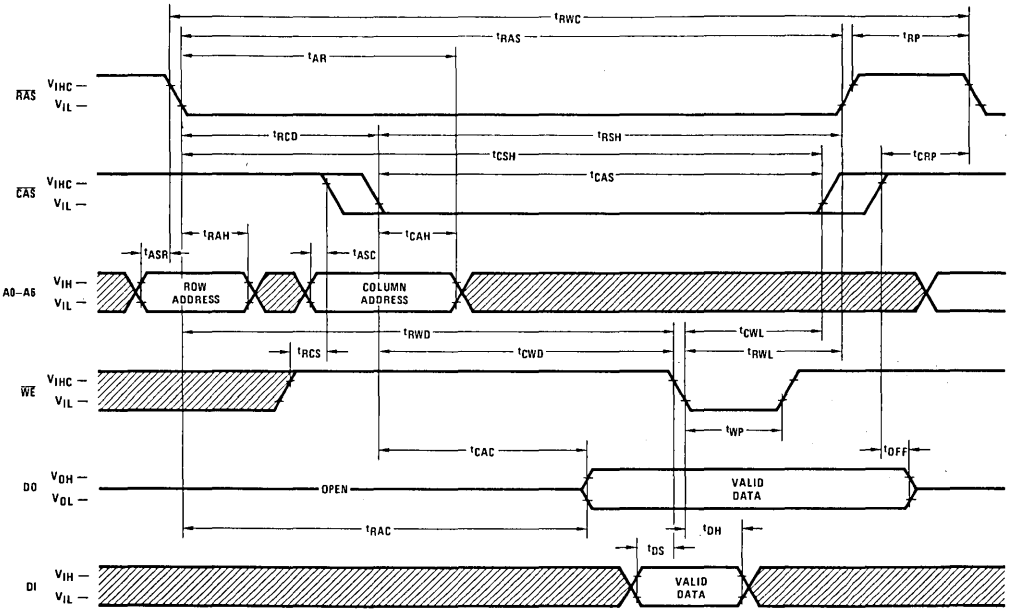


Write Cycle (Early Write)

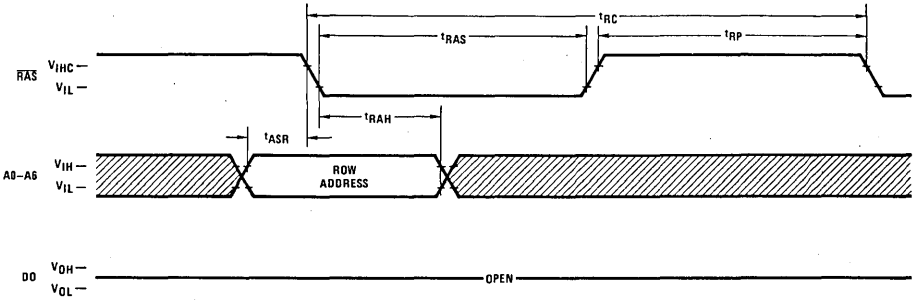


Switching Time Waveforms (Continued)

Read-Write Cycle, Read-Modify-Write Cycle



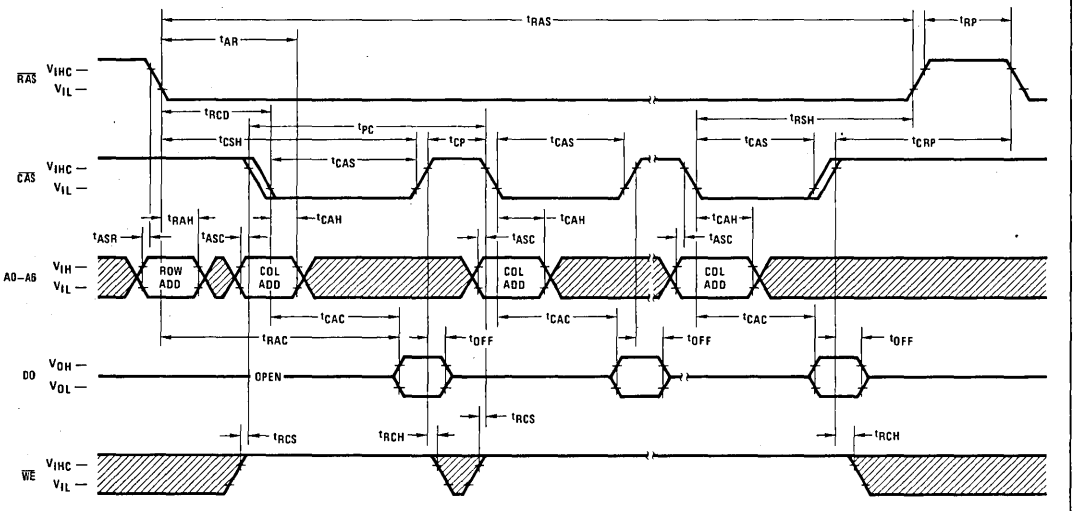
RAS-Only Refresh Cycle



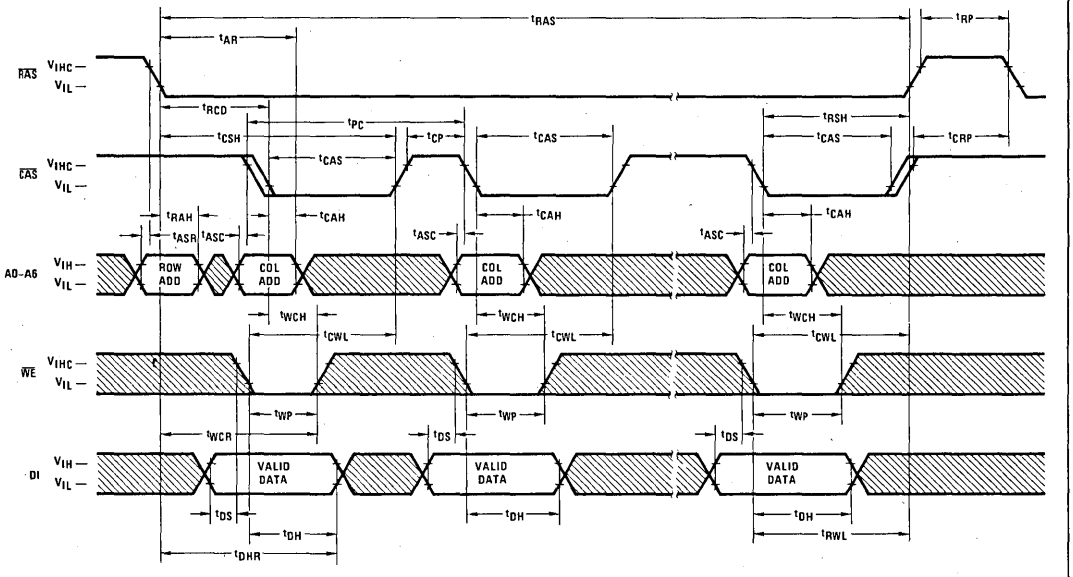
Note. $\overline{CAS}$ = V_{IHC}, $\overline{WE}$ = don't care

Switching Time Waveforms (Continued)

Page Mode Read Cycle



Page Mode Write Cycle



Note. Standard part not tested for page mode

National Semiconductor

NMOS RAMs

MM5298** 8192-Bit (8192 x 1) Dynamic RAM

General Description

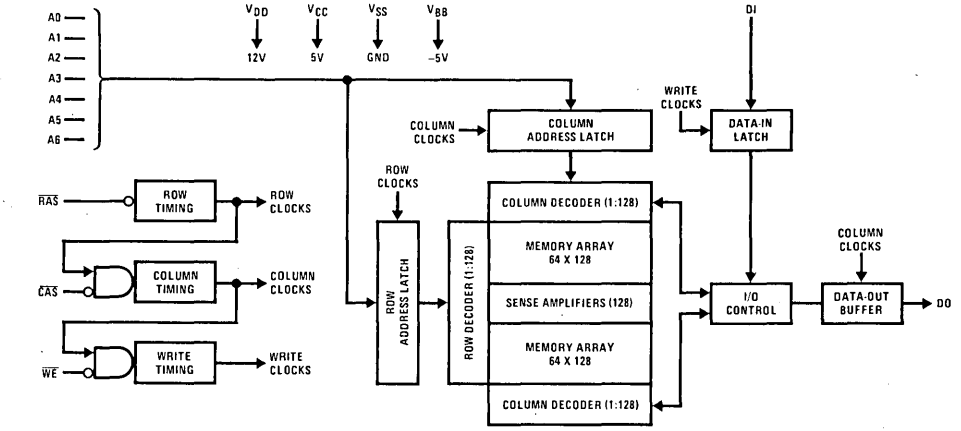
The MM5298 is an 8192 x 1-bit dynamic RAM. It features a multiplexed address input with separate row and column strobes. This added flexibility allows the MM5298 to be used in page mode operation. The MM5298 employs the same masks and highly reliable production-proven 2-layer polysilicon NMOS technology as the MM5290.

As shown in the block diagram, the MM5298 is available as either the upper or lower half of the MM5290. Address A5 selects the operating half. For MM5298A, A5 should be low (V_{IL}) during row address hold time (t_{RAH}). For MM5298B, A5 should be high (V_{IH}) during t_{RAH}. The MM5298 requires only 64 cycles of Refresh every 2 ms. This can be accomplished by performing any cycle which brings the RAS active including an $\overline{RAS}$-only cycle at each of the 64 row addresses used.

Features

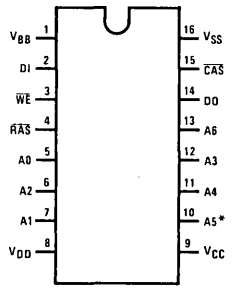
- 100% DC and AC compatible with MM5290
- Only 64 Refresh cycles every 2 ms
- Access Times: 150 ns, 200 ns, 250 ns
- Low power: 528 mW max
- TTL compatible: all inputs and output
- Gated $\overline{CAS}$–noncritical timing
- Read, Write, Read-Modify-Write and $\overline{RAS}$-only Refresh cycles
- Page mode operation
- Industry standard 16-pin configuration

Block Diagram



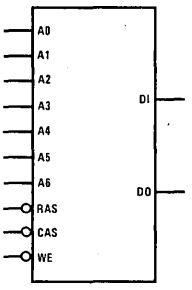
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Diagram



Pin Names

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0–A6	Address Inputs
DI	Data Input
DO	Data Output
V_{DD}	Power (12V)
V_{CC}	Power (5V)
V_{SS}	Ground
V_{BB}	Power (−5V)

Order Number MM5298AJ-2, MM5298BJ-2, MM5298AJ-3, MM5298BJ-3, MM5298AJ-4 or MM5298BJ-4
See NS Package J16A

Order Number MM5298AN-2, MM5298BN-2, MM5298AN-3, MM5298BN-3, MM5298AN-4 or MM5298BN-4
See NS Package N16A

*For MM5298A A5 must be at V_{IL} during t_{RAH}.
For MM5298B A5 must be at V_{IH} during t_{RAH}.

**See the MST™ Program page 3.

Absolute Maximum Ratings (Note 1)

Storage Temperature −65°C to +150°C
Power Dissipation 1W
Voltage on Any Pin Relative to V_{BB} −0.3V to +20V
($V_{SS} - V_{BB} \geq 4.5V$)
Lead Temperature (Soldering, 10 seconds) 300°C

Recommended DC Operating Conditions

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
T_A	Ambient Temperature	0	70	°C	
V_{DD}	Supply Voltages	10.8	13.2	V	2, 3
V_{CC}		4.5	5.5	V	2, 3
V_{SS}		0	0	V	2, 3
V_{BB}		−4.5	−5.5	V	2, 3
V_{IHC}	Input High Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	2.7	7.0	V	2
V_{IH}	Input High Voltage, A0–A6, DI	2.4	7.0	V	2
V_{IL}	Input Low Voltage, All Inputs	−1.0	0.8	V	2

DC Electrical Characteristics Over the range of Recommended DC Operating Conditions unless otherwise noted

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DD1}	**Operating Current**		40	mA	4
I_{CC1}	Average Power Supply Operating Current				5
I_{BB1}	($\overline{RAS}$, $\overline{CAS}$ Cycling; t_{RC} = t_{RC} MIN)		200	μA	
I_{DD2}	**Standby Current**		1.5	mA	
I_{CC2}	Power Supply Standby Current ($\overline{RAS}$ = V_{IHC},	−10	10	μA	
I_{BB2}	DO = High Impedance)		100	μA	
I_{DD3}	**Refresh Current**		30	mA	4
I_{CC3}	Average Power Supply Current, Refresh Mode	−10	10	μA	
I_{BB3}	($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = t_{RC} MIN)		200	μA	
I_{DD4}	**Page Mode Current**		32	mA	4
I_{CC4}	Average Power Supply Current, Page Mode				5
I_{BB4}	($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling; t_{PC} = 225 ns)		200	μA	
$I_{I(L)}$	**Input Leakage**	−10	10	μA	
	Input Leakage Current, Any Input				
	(V_{BB} = −5V, 0V ≤ V_{IN} ≤ 7V, All Other				
	Pins not Under Test = 0V)				
$I_{O(L)}$	**Output Leakage**	−10	10	μA	
	Output Leakage Current (DO is Disabled,				
	0V ≤ V_{OUT} ≤ 5.5V)				
	Output Levels				
V_{OH}	Output High Voltage (I_{OUT} = −5 mA)	2.4		V	
V_{OL}	Output Low Voltage (I_{OUT} = 4.2 mA)		0.4	V	
CAPACITANCE					
C_I	Input Capacitance A0–A6, DI		5	pF	6
C_C	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$		10	pF	6
C_O	Output Capacitance, DO		7	pF	6

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Recommended DC Operating Conditions" provides conditions for actual device operation.

Note 2: All voltages referenced to V_{SS}. When applying voltages to the device, V_{DD}, V_{CC} or V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Several cycles are required after power-up before proper device operation is achieved. Any 8 RAS cycles are adequate for this purpose.

Note 4: I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate.

Note 5: I_{CC} depends on output load.

Note 6: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$. Capacitance is guaranteed by periodic testing.

AC Electrical Characteristics

Over the range of Recommended DC Operating Conditions unless otherwise noted

SYMBOL	PARAMETER	MM5298-2A, MM5298-2B		MM5298-3A, MM5298-3B		MM5298-4A, MM5298-4B		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	375		375		410		ns	7, 8
t_{RWC}	Read-Write Cycle Time	375		375		515		ns	7, 8
t_{PC}	Page Mode Cycle Time	170		225		275		ns	
t_{RAC}	Access Time from $\overline{RAS}$		150		200		250	ns	9, 11
t_{CAC}	Access Time from $\overline{CAS}$		100		135		165	ns	10, 11
t_{OFF}	Output Buffer Turn-Off Delay	0	40	0	50	0	60	ns	12
t_T	Transition Time (Rise and Fall)	3	35	3	50	3	50	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	100		120		150		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10,000	200	10,000	250	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	100		135		165		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	100	10,000	135	10,000	165	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	65	35	85	ns	9
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	−20		−20		−20		ns	
t_{ASR}	Row Address Set-Up Time	0		0		0		ns	
t_{RAH}	Row Address Hold Time	20		25		35		ns	
t_{ASC}	Column Address Set-Up Time	−10		−10		−10		ns	
t_{CAH}	Column Address Hold Time	45		55		75		ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{RCS}	Read Command Set-Up Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{WCH}	Write Command Hold Time	45		55		75		ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{WP}	Write Command Pulse Width	45		55		75		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	60		80		100		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	60		80		100		ns	
t_{DS}	Data-In Set-Up Time	0		0		0		ns	13, 14
t_{DH}	Data-In Hold Time	45		55		75		ns	13, 14
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (for Page Mode Cycle Only)	60		80		100		ns	
t_{REF}	Refresh Period		2		2		2	ms	
t_{WCS}	$\overline{WE}$ to $\overline{CAS}$ Set-Up Time	−40		−40		−40		ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	70		95		125		ns	15
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	120		160		200		ns	15

Note 7: The specifications for $t_{RC(MIN)}$ and $t_{RWC(MIN)}$ are used only to indicate cycle time at which proper operation over the full temperature range is guaranteed.

Note 8: Transition times are measured between V_{IHC} or V_{IH} and V_{IL}. Timing measurements are made between $V_{IHC(MIN)}$ or $V_{IH(MIN)}$ and $V_{IL(MAX)}$, and assume $t_T = 5$ ns.

Note 9: Assumes row-limited access, i.e., $t_{RCD} \leq t_{RCD(MAX)}$. If this condition is not satisfied, then note 10 applies.

Note 10: Assumes column-limited access, i.e., $t_{RCD} > t_{RCD(MAX)}$.

Note 11: Equivalent load is 2 standard TTL inputs plus 100 pF.

Note 12: $\overline{CAS}$ going high disables the Data Output. t_{OFF} is the delay to the high impedance state.

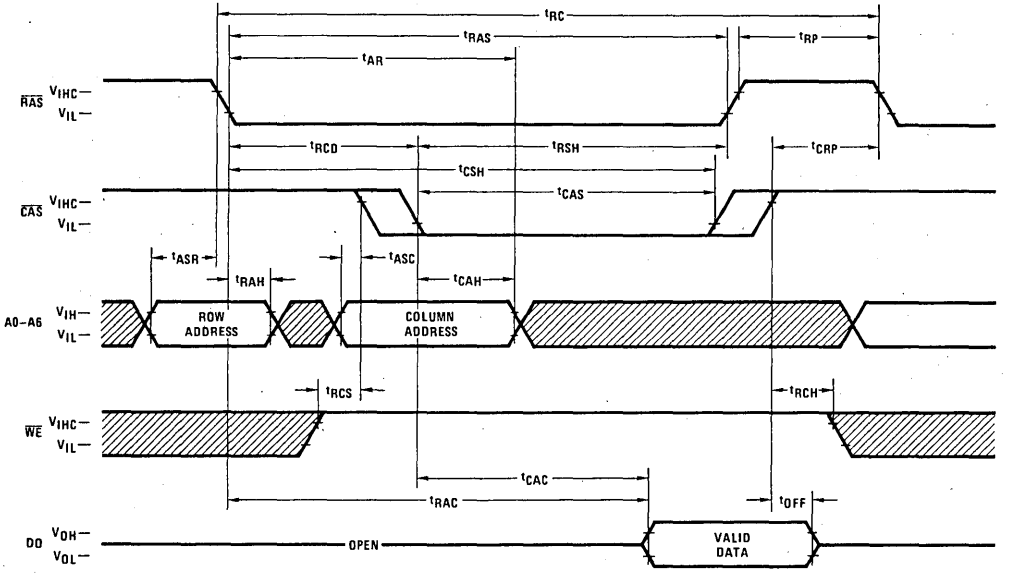
Note 13: These parameters are referenced to the negative edge of $\overline{CAS}$ in an early-write cycle and to the negative edge of $\overline{WE}$ in a Read-Modify-Write cycle. (See Note 14 below).

Note 14: If $t_{WCS} \geq t_{WCS(MIN)}$, the Data Output is guaranteed to remain in the high impedance state for the duration of the cycle. This is the "early-write" cycle.

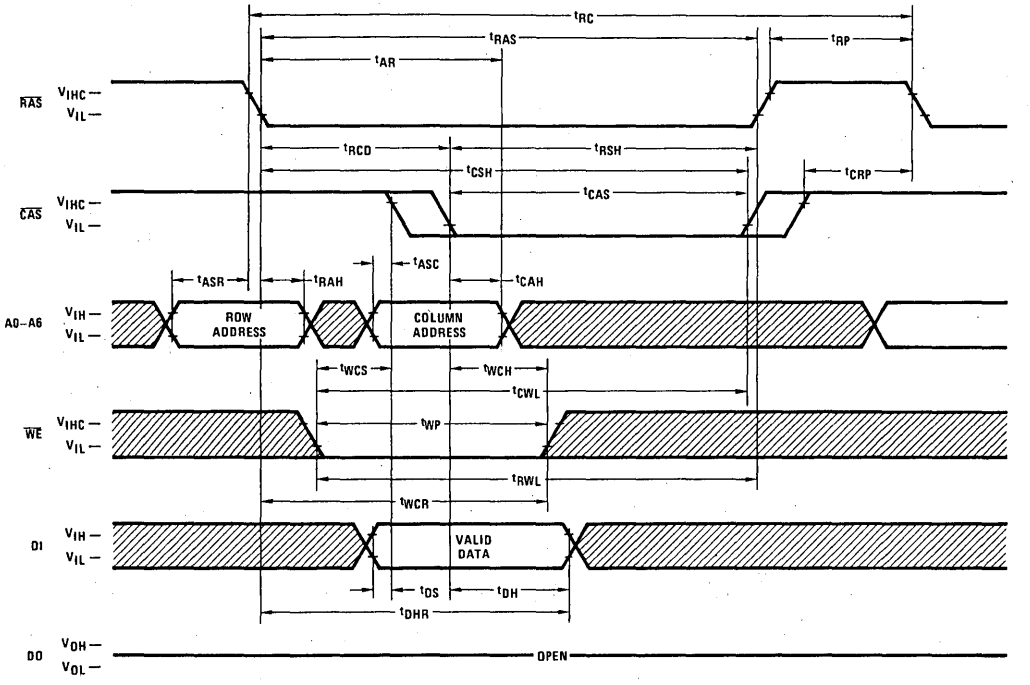
Note 15: If $t_{CWD} \geq t_{CWD(MIN)}$ and $t_{RWD} \geq t_{RWD(MIN)}$, the Data Output will contain the original data in the selected cell. This is the Read-Modify-Write cycle. If either of these conditions is not satisfied, the output will be indeterminate unless the early-write condition of Note 12 is met.

Switching Time Waveforms

Read Cycle

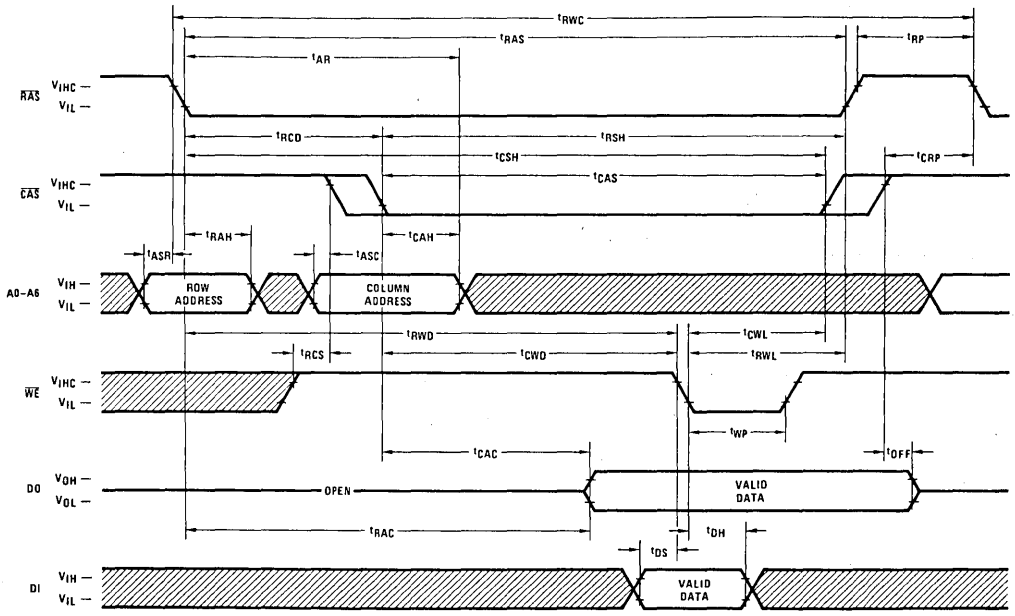


Write Cycle (Early Write)

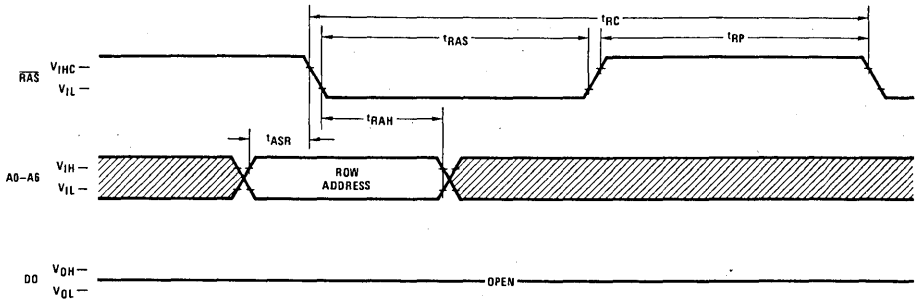


Switching Time Waveforms (Continued)

Read-Write Cycle, Read-Modify-Write Cycle



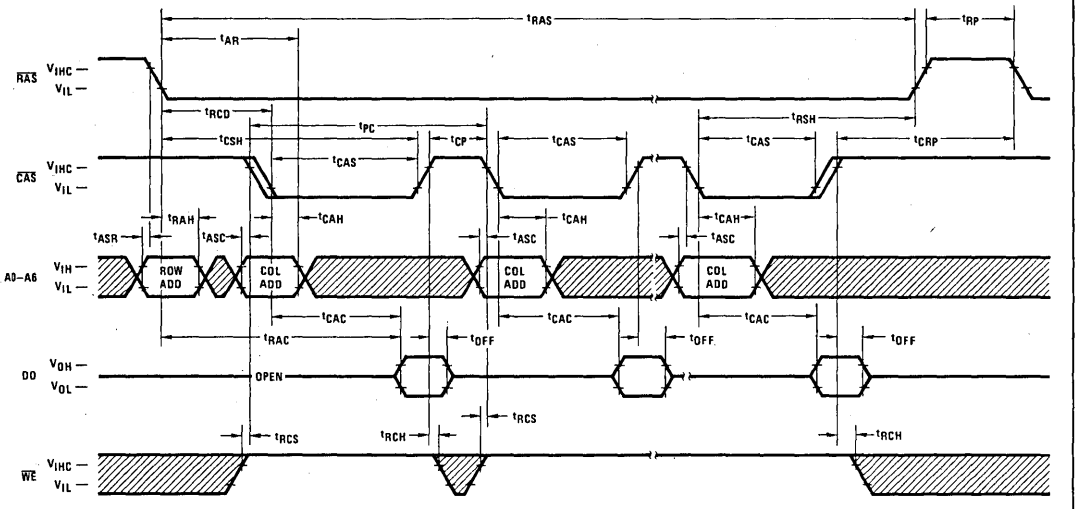
RAS-Only Refresh Cycle



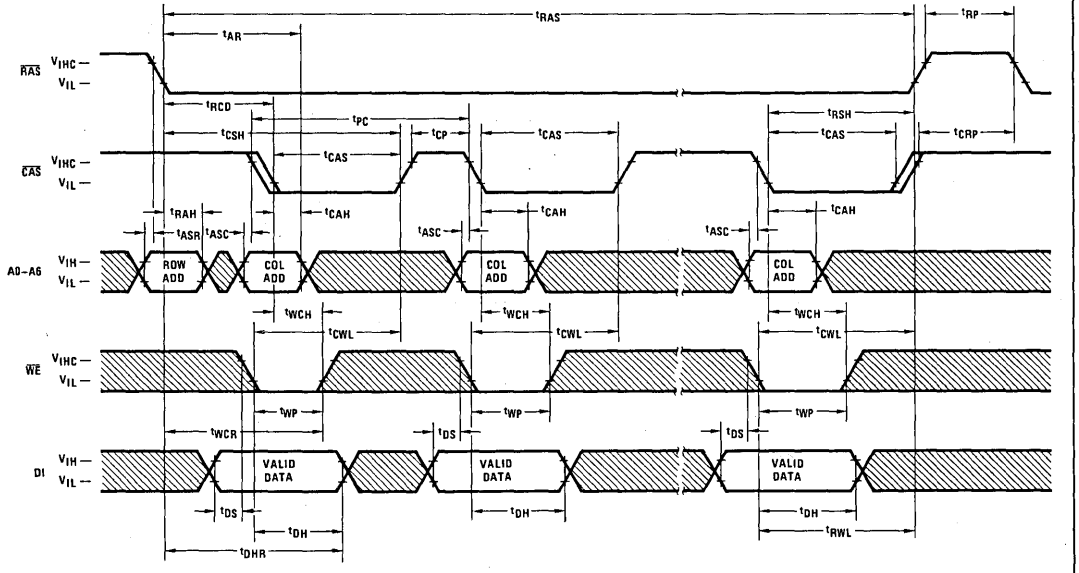
Note. $\overline{CAS}$ = V_{IHC}, $\overline{WE}$ = don't care

Switching Time Waveforms (Continued)

Page Mode Read Cycle



Page Mode Write Cycle



Note. Standard part not tested for page mode

National Semiconductor

NMOS RAMs
PREVIEW

NMC4164† 65,536-Bit (65,536 x 1) Dynamic RAM

General Description

The NMC4164 is a 65,536 x 1 bit dynamic RAM. It features a multiplexed address input with separate row and column strobes.

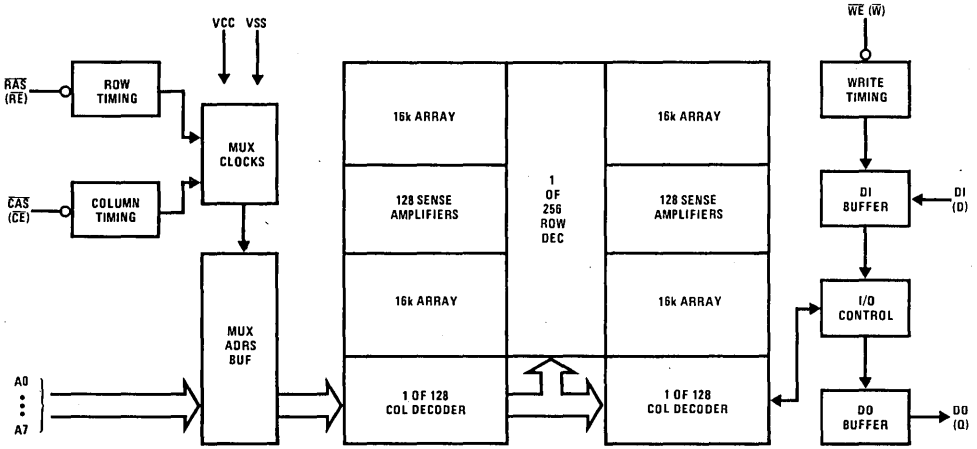
The NMC4164 must be refreshed every 4 ms. This can be accomplished by performing any cycle which brings the Row Address Strobe active including an $\overline{RAS}$ ($\overline{RE}$)-only cycle at each of the 256 row addresses.

N-channel triple-polysilicon gate technology, developed by National, is used in the manufacture of the NMC4164. This process combines high density and performance with reliability.

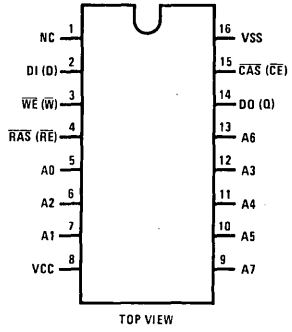
Features

- Single 5V ± 10% supply
- 256 cycle 4 ms refresh
- Access times:
  - NMC4164-1 — 120 ns
  - NMC4164-2 — 150 ns
- Low power — 250 mW
- TTL compatible: all inputs and output
- Gated $\overline{CE}$ — noncritical timing
- Read, write, read-modify-write and $\overline{RAS}$ ($\overline{RE}$)-only refresh cycles
- Buried refresh option
- Page mode operation
- Industry standard 16-pin configuration
- TRI-STATE® output
- On-chip substrate bias generator

Block and Connection Diagrams**



Dual-In-Line Package



Order Number NMC4164J-X*
See NS Package J16A

Order Number NMC4164N-X*
See NS Package N16A

Pin Names

$\overline{RAS}$ ($\overline{RE}$)	Row Address Strobe
$\overline{CAS}$ ($\overline{CE}$)	Column Address Strobe
$\overline{WE}$ ($\overline{W}$)	Write Enable
A0-A7	Address Inputs
DI (D)	Data Input
DO (Q)	Data Output
VCC	Power (5V)
VSS	Ground

†See the MST™ Program page 3.

** Symbols in parentheses are proposed industry standard.

* X = Speed selection

Absolute Maximum Ratings (Note 1)

Operating Temperature Range	0°C to +70°C	Voltage on Any Pin Relative to VSS	−1.0 to +7V
Storage Temperature	−65°C to +150°C	Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	1W		

Recommended DC Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
TA	Ambient Temperature	0	70	°C	
VCC	Supply Voltages	4.5	5.5	V	2, 3
VSS		0	0	V	2, 3
VIH	Input High Voltage, All Inputs	2.4	7.0	V	2
VIL	Input Low Voltage, All Inputs	−1.0	0.8	V	2

DC Electrical Characteristics

Over the range of Recommended DC Operating Conditions unless otherwise noted

Symbol	Parameter	Min	Max	Units	Notes
ICC1	**Operating Current** Average Power Supply Operating Current ($\overline{RE}$, $\overline{CE}$ Cycling; TRELREL = TRELREL Min)		45	mA	4
ICC2	**Standby Current** Power Supply Standby Current ($\overline{RE}$ = VIH, Q = High Impedance)		4	mA	
ICC3	**Refresh Current** Average Power Supply Current, Refresh Mode $\overline{CE}$ Cycling, $\overline{CE}$ = VIH; TRELREL = TRELREL Min)		35	mA	4
ICC4	**Page Mode Current** Average Power Supply Current, Page Mode ($\overline{RE}$ = VIL, $\overline{CE}$ Cycling; TCELCEL = 100 ns)		37	mA	4
II	**Input Leakage** Input Leakage Current, Any Input (0V ≤ VIN ≤ 7V, All Other Pins not Under Test = 0V)	−10	10	μA	
IOZ	**Output Leakage** Output Leakage Current (Q is Disabled, 0V ≤ VOUT ≤ 5.5V)	−10	10	μA	
	Output Levels				
VOH	Output High Voltage (IOUT = −5 mA)	2.4		V	
VOL	Output Low Voltage (IOUT = 4.2 mA)		0.4	V	

Capacitance

Symbol	Parameter	Max	Units	Notes
CI	Input Capacitance A0-A6, D	5	pF	5
CC	Input Capacitance $\overline{RE}$, $\overline{CE}$, $\overline{W}$	10	pF	5
CQ	Output Capacitance, Q	7	pF	5

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Recommended DC Operating Conditions" provides conditions for actual device operation.

Note 2: All voltages referenced to VSS. When applying voltages to the device, VCC should never be 1.0V more negative than VSS.

Note 3: Several cycles are required after power-up before proper device operation is achieved. Any 8 $\overline{RE}$ cycles are adequate for this purpose.

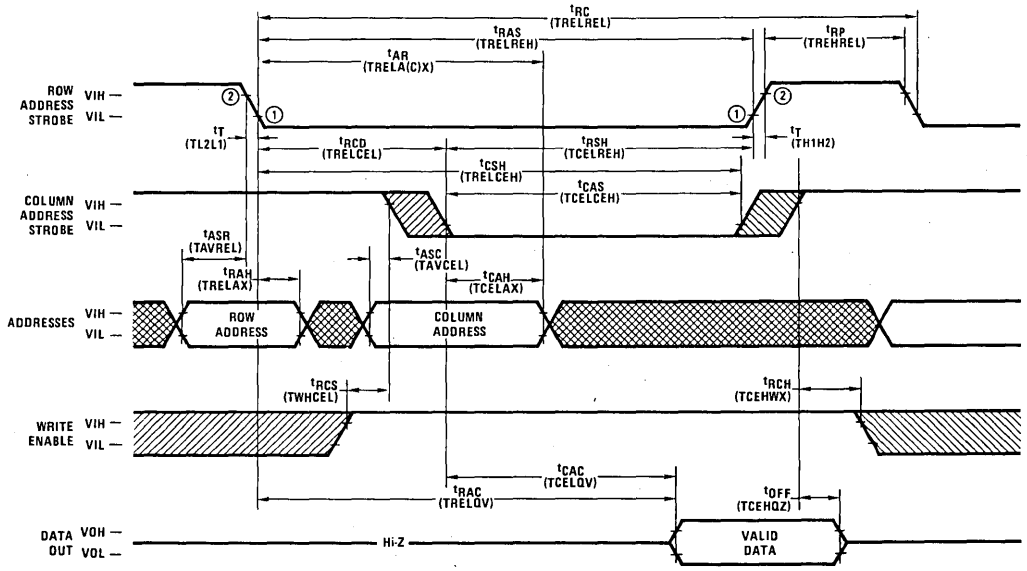
Note 4: ICC1, ICC3 and ICC4 depend on cycle rate.

Note 5: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation C = IΔt/ΔV. Capacitance is guaranteed by periodic testing.

Read Cycle AC Electrical Characteristics (Notes 1, 2, 3 and 4)

Symbol		Parameter	NMC4164-1		NMC4164-2		Units	Notes
Alternate	Standard		Min	Max	Min	Max		
t_{RC}	TRELREL	Random Read Cycle Time	270		305		ns	
t_{RAS}	TRELREH	$\overline{RAS}$ Pulse Width	140	10,000	165	10,000	ns	
t_{RP}	TREHREL	$\overline{RAS}$ Precharge Time	120		130		ns	
t_T	TH1H2	Rise Time	3	50	3	50	ns	
t_T	TL2L1	Fall Time	3	50	3	50	ns	
t_{RCD}	TRELCEL	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	30	60	ns	5
t_{RSH}	TCELREH	$\overline{RAS}$ Hold Time	85		100		ns	
t_{CSH}	TRELCEH	$\overline{CAS}$ Hold Time	135		150		ns	
t_{CAS}	TCELCEH	$\overline{CAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{CP}	TCEHCEL	$\overline{CAS}$ Precharge Time	70		80		ns	6
t_{ASR}	TAVREL	Row Address Set-Up Time	0		0		ns	
t_{RAH}	TRELAX	Row Address Hold Time	20		25		ns	
t_{ASC}	TAVCEL	Column Address Set-Up Time	0		0		ns	
t_{CAH}	TCELAX	Column Address Hold Time	25		30		ns	
t_{AR}	TRELA(C)X	Column Address Hold Time Referenced to $\overline{RAS}$	80		90		ns	7
t_{RCS}	TWHCEL	Read Command Set-Up Time	0		0		ns	
t_{RCH}	TCEHWX	Read Command Hold Time	0		0		ns	8
t_{RAC}	TRELQV	Access Time from $\overline{RAS}$		120		150	ns	9, 10
t_{CAC}	TCELQV	Access Time from $\overline{CAS}$		65		90	ns	10, 11
t_{OFF}	TCEHQZ	Output Buffer Turn-Off Delay	0	50	0	55	ns	12

Read Cycle Waveforms*

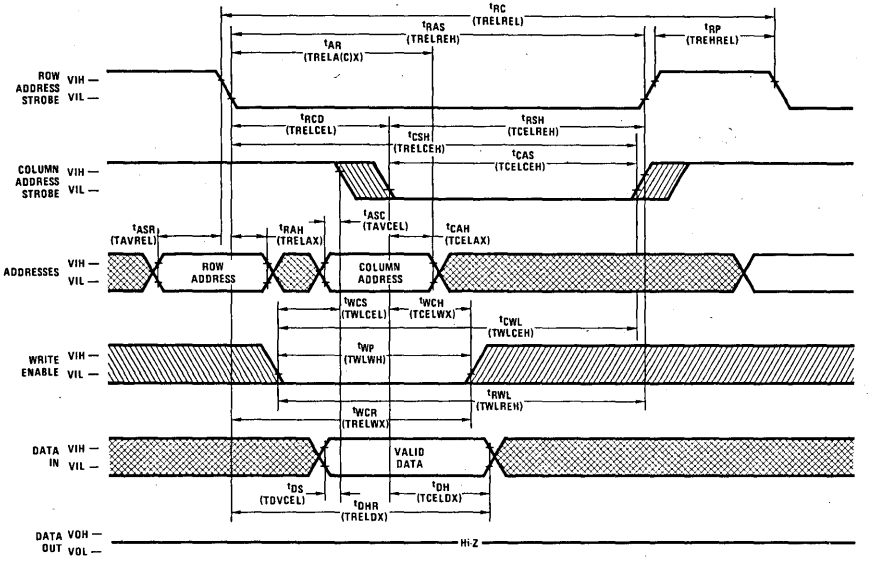


*Symbols in parentheses are proposed industry standard.

Write Cycle AC Electrical Characteristics

Symbol		Parameter	NMC4164-1		NMC4164-2		Units	Notes
Alternate	Standard		Min	Max	Min	Max		
t_{WC}	TRELREL	Random Write Cycle Time	270		305		ns	
t_{RAS}	TRELREH	$\overline{RAS}$ Pulse Width	140	10,000	165	10,000	ns	
t_{RP}	TREHREL	$\overline{RAS}$ Precharge Time	120		130		ns	
t_T	TH1H2	Rise Time	3	50	3	50	ns	
t_T	TL2L1	Fall Time	3	50	3	50	ns	
t_{RCD}	TRELCEL	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	30	60	ns	
t_{RSH}	TCELREH	$\overline{RAS}$ Hold Time	85		100		ns	
t_{CSH}	TRELCEH	$\overline{CAS}$ Hold Time	135		150		ns	
t_{CAS}	TCELCEH	$\overline{CAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{CP}	TCEHCEL	$\overline{CAS}$ Precharge Time	70		80		ns	6
t_{ASR}	TAVREL	Row Address Set-Up Time	0		0		ns	
t_{RAH}	TRELAX	Row Address Hold Time	20		25		ns	
t_{ASC}	TAVCEL	Column Address Set-Up Time	0		0		ns	
t_{CAH}	TCELAX	Column Address Hold Time	25		30		ns	
t_{AR}	TRELA(C)X	Column Address Hold Time Referenced to $\overline{RAS}$	80		90		ns	
t_{WCS}	TWLCEL	$\overline{WE}$ to $\overline{CAS}$ Set-Up Time	0		0		ns	13
t_{WCH}	TCELWX	Write Command Hold Time	35		45		ns	
t_{WP}	TWLWH	Write Command Pulse Width	40		45		ns	
t_{CWL}	TWLCEH	Write Command to $\overline{CAS}$ Lead Time	85		95		ns	
t_{RWL}	TWLREH	Write Command to $\overline{RAS}$ Lead Time	90		100		ns	
t_{WCR}	TRELWX	Write Command Hold Time Referenced to $\overline{RAS}$	90		100		ns	
t_{DS}	TDVCEL	Data In Set-Up Time	0		0		ns	
t_{DH}	TCELDX	Data In Hold Time	35		40		ns	
t_{DHR}	TRELDX	Data In Hold Time Referenced to $\overline{RAS}$	90		100		ns	

Write Cycle (Early-Write) Waveforms* (Note 13)

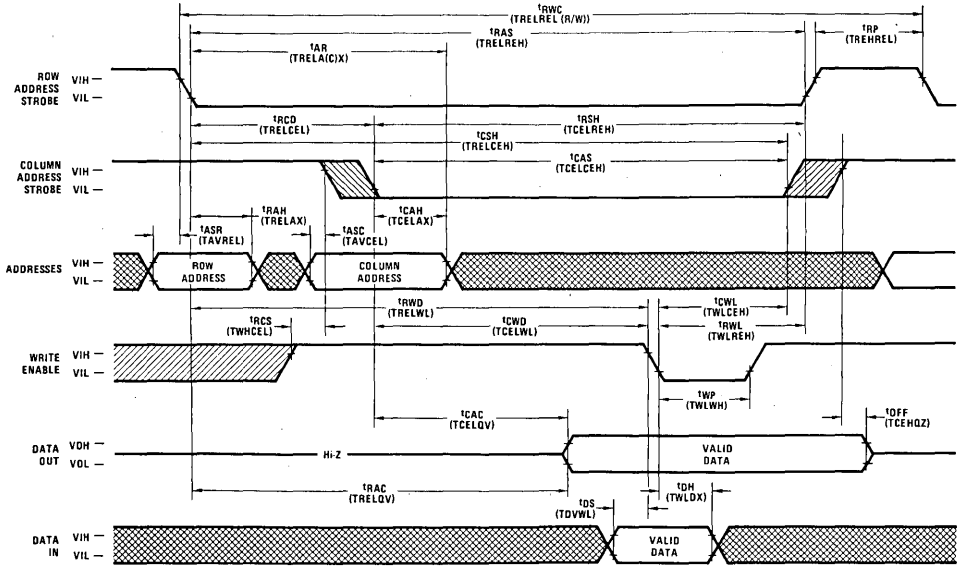


*Symbols in parentheses are proposed industry standard.

Read-Write and Read-Modify-Write Cycle AC Electrical Characteristics

Symbol		Parameter	NMC4164-1		NMC4164-2		Units	Notes
Alternate	Standard		Min	Max	Min	Max		
t_{RWC}	TRELREL (R/W)	Read-Write Cycle Time	345		385		ns	14
t_{RAS}	TRELREH	$\overline{RAS}$ Pulse Width	215	10,000	245	10,000	ns	14
t_{RP}	TREHREL	$\overline{RAS}$ Precharge Time	120		130		ns	
t_T	TH1H2	Rise Time	3	50	3	50	ns	
t_T	TL2L1	Fall Time	3	50	3	50	ns	
t_{RCD}	TRELCEL	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	30	60	ns	5
t_{RSH}	TCELREH	$\overline{RAS}$ Hold Time	85		100		ns	
t_{CSH}	TRELCEH	$\overline{CAS}$ Hold Time	135		150		ns	
t_{CAS}	TCELCEH	$\overline{CAS}$ Pulse Width	160	10,000	185	10,000	ns	14
t_{CP}	TCEHCEL	$\overline{CAS}$ Precharge Time	70		80		ns	6
t_{ASR}	TAVREL	Row Address Set-Up Time	0		0		ns	
t_{RAH}	TRELAX	Row Address Hold Time	20		25		ns	
t_{ASC}	TAVCEL	Column Address Set-Up Time	0		0		ns	
t_{CAH}	TCELAX	Column Address Hold Time	25		30		ns	
t_{AR}	TRELA(C)X	Column Address Hold Time Referenced to $\overline{RAS}$	80		90		ns	7
t_{RCS}	TWHCEL	Read Command Set-Up Time	0		0		ns	
t_{WP}	TWLWH	Write Command Pulse Width	40		45		ns	
t_{CWL}	TWLCEH	Write Command to $\overline{CAS}$ Lead Time	85		95		ns	
t_{RWL}	TWLREH	Write Command to $\overline{RAS}$ Lead Time	90		100		ns	
t_{RWD}	TRELWL	$\overline{RAS}$ to $\overline{WE}$ Delay	120		150		ns	
t_{CWD}	TCELWL	$\overline{CAS}$ to $\overline{WE}$ Delay	65		90		ns	13
t_{DS}	TDVWL	Data In Set-up Time	0		0		ns	
t_{DH}	TWLDX	Data In Hold Time	35		40		ns	
t_{RAC}	TRELQV	Access Time from $\overline{RAS}$		120		150	ns	9, 10
t_{CAC}	TCELQV	Access Time from $\overline{CAS}$		65		90	ns	10, 11
t_{OFF}	TCEHQZ	Output Buffer Turn-Off Delay	0	50	0	55	ns	12

Read-Write and Read-Modify-Write Waveforms*

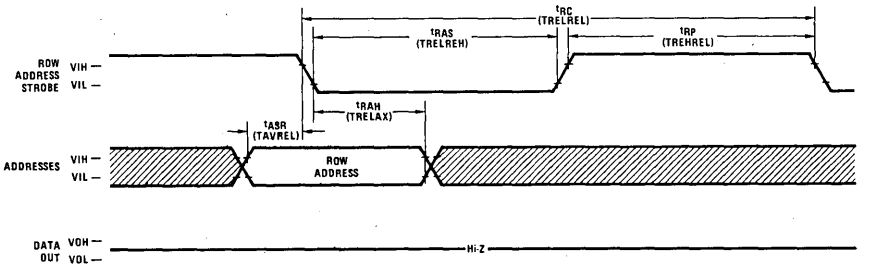


*Symbols in parentheses are proposed industry standard.

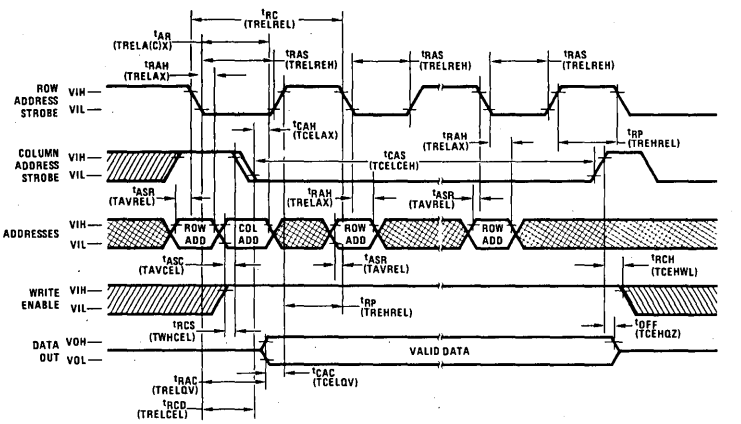
$\overline{RAS}$-Only Refresh and Buried Refresh AC Electrical Characteristics

Symbol		Parameter	NMC4164-1		NMC4164-2		Units	Notes
Alternate	Standard		Min	Max	Min	Max		
t_{RC}	TRELREL	Random Read or Write Cycle Time	270		305		ns	
t_{RAS}	TRELREH	$\overline{RAS}$ Pulse Width	140	10,000	165	10,000	ns	
t_{RP}	TREHREL	$\overline{RAS}$ Precharge Time	120		130		ns	
t_T	TH1H2	Rise Time	3	50	3	50	ns	
t_T	TL2L1	Fall Time	3	50	3	50	ns	
t_{RCD}	TRELCEL	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	30	60	ns	5
t_{RSH}	TCELREH	$\overline{RAS}$ Hold Time	85		100		ns	
t_{CSH}	TRELCEH	$\overline{CAS}$ Hold Time	135		150		ns	
t_{CAS}	TCELCEH	$\overline{CAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{CP}	TCEHCEL	$\overline{CAS}$ Precharge Time	70		80		ns	6
t_{ASR}	TAVREL	Row Address Set-Up Time	0		0		ns	
t_{RAH}	TRELAX	Row Address Hold Time	20		25		ns	
t_{ASC}	TAVCEL	Column Address Set-Up Time	0		0		ns	
t_{CAH}	TCELAX	Column Address Hold Time	25		30		ns	
t_{AR}	TRELA(C)X	Column Address Hold Time Referenced to $\overline{RAS}$	80		90		ns	7
t_{RCS}	TWHCEL	Read Command Set-Up Time	0		0		ns	
t_{RCH}	TCEHWX	Read Command Hold Time	0		0		ns	8
t_{RAC}	TRELQV	Access Time from $\overline{RAS}$		120		150	ns	9, 10
t_{CAC}	TCELQV	Access Time from $\overline{CAS}$		65		90	ns	10, 11
t_{OFF}	TCEHQZ	Output Buffer Turn-Off Delay	0	50	0	55	ns	12

$\overline{RAS}$-Only Refresh Waveforms* ($\overline{CAS}$ = VIH, $\overline{WE}$ = don't care)



Buried Refresh Waveforms*

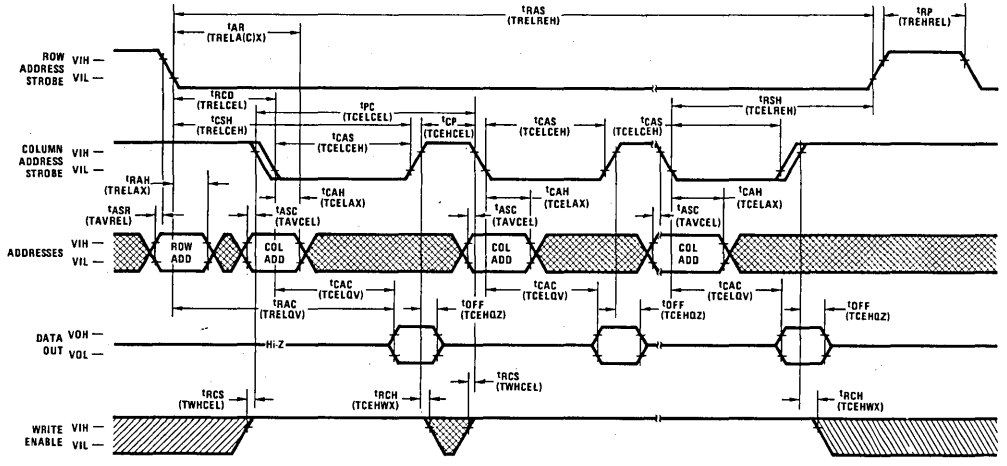


*Symbols in parentheses are proposed industry standard.

Page Mode Read Cycle AC Electrical Characteristics†

Symbol		Parameter	NMC4164-1		NMC4164-2		Units	Notes
Alternate	Standard		Min	Max	Min	Max		
t_{PC}	TRELREL	Page Mode Cycle Time	235		270		ns	14
t_{RAS}	TRELREH	$\overline{RAS}$ Pulse Width	445	10,000	510	10,000	ns	14
t_{RP}	TREHREL	$\overline{RAS}$ Precharge Time	120		130		ns	
t_T	TH1H2	Rise Time	3	50	3	50	ns	
t_T	TL2L1	Fall Time	3	50	3	50	ns	
t_{RCD}	TRELCEL	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	30	60	ns	5
t_{RSH}	TCELREH	$\overline{RAS}$ Hold Time	85		100		ns	
t_{CSH}	TRELCEH	$\overline{CAS}$ Hold Time	135		150		ns	13
t_{CAS}	TCELCEH	$\overline{CAS}$ Pulse Width	155	10,000	180	10,000	ns	14
t_{CP}	TCEHCEL	$\overline{CAS}$ Precharge Time, Page Mode	70		80		ns	6
t_{ASR}	TAVREL	Row Address Set-Up Time	0		0		ns	
t_{RAH}	TRELAX	Row Address Hold Time	20		25		ns	
t_{ASC}	TAVCEL	Column Address Set-Up Time	0		0		ns	
t_{CAH}	TCELAX	Column Address Hold Time	25		30		ns	
t_{AR}	TRELA(C)X	Column Address Hold Time Referenced to $\overline{RAS}$	80		90		ns	7
t_{RCS}	TWHCEL	Read Command Set-Up Time	0		0		ns	
t_{WP}	TWLWH	Write Command Pulse Width	40		45		ns	
t_{CWL}	TWLCEH	Write Command to $\overline{CAS}$ Lead Time	85		95		ns	
t_{RWL}	TWLREH	Write Command to $\overline{RAS}$ Lead Time	90		100		ns	
t_{RWD}	TRELWL	$\overline{RAS}$ to $\overline{WE}$ Delay	120		150		ns	13
t_{CWP}	TCELWL	$\overline{CAS}$ to $\overline{WE}$ Delay	65		90		ns	
t_{DS}	TDVWL	Data In Set-Up Time	0		0		ns	
t_{DH}	TWLDX	Data In Hold Time	35		40		ns	
t_{RAC}	TRELQV	Access Time from $\overline{RAS}$		120		150	ns	9, 10
t_{CAC}	TCELQV	Access Time from $\overline{CAS}$		65		90	ns	10, 11
t_{OFF}	TCEHQZ	Output Buffer Turn-Off Delay	0	50	0	55	ns	12

Page Mode Read Cycle Waveforms*

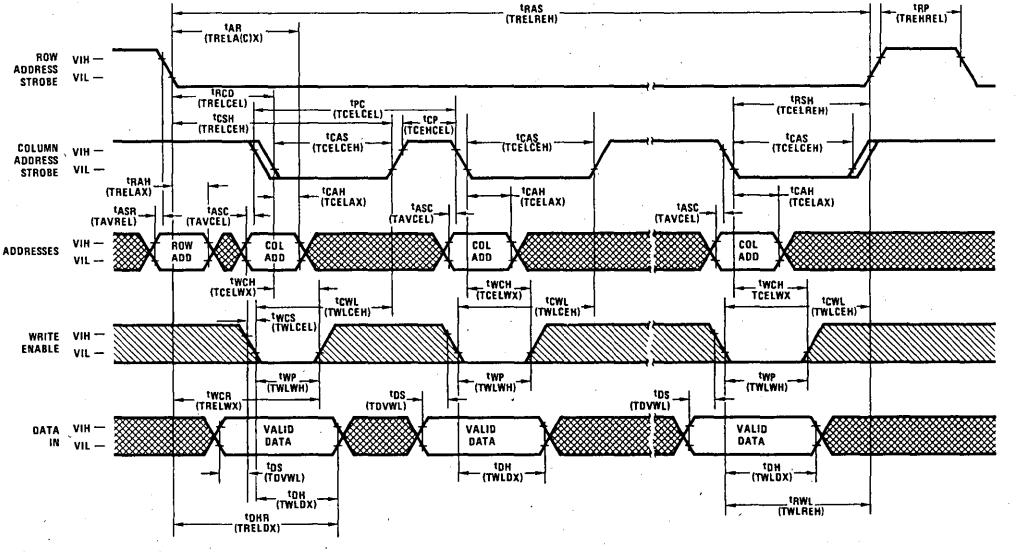


† Standard part not tested for page mode.
* Symbols in parentheses are proposed Industry standard.

Page Mode Write Cycle AC Electrical Characteristics †

Symbol		Parameter	NMC4164-1		NMC4164-2		Units	Notes
Alternate	Standard		Min	Max	Min	Max		
t_{PC}	TRELREL	Page Mode Cycle Time	160		190		ns	
t_{RAS}	TRELREH	$\overline{RAS}$ Pulse Width	300	10,000	350	10,000	ns	
t_{RP}	TREHREL	$\overline{RAS}$ Precharge Time	120		130		ns	
t_T	TH1H2	Rise Time	3	50	3	50	ns	
t_T	TL2L1	Fall Time	3	50	3	50	ns	
t_{RCD}	TRELCEL	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	30	60	ns	
t_{RSH}	TCELREH	$\overline{RAS}$ Hold Time	85		100		ns	
t_{CSH}	TRELCEH	$\overline{CAS}$ Hold Time	135		150		ns	
t_{CAS}	TCELCEH	$\overline{CAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{CP}	TCEHCEL	$\overline{CAS}$ Precharge Time	70		80		ns	6
t_{ASR}	TAVREL	Row Address Set-Up Time	0		0		ns	
t_{RAH}	TRELAX	Row Address Hold Time	20		25		ns	
t_{ASC}	TAVCEL	Column Address Set-Up Time	0		0		ns	
t_{CAH}	TCELAX	Column Address Hold Time	25		30		ns	
t_{AR}	TRELA(C)X	Column Address Hold Time Referenced to $\overline{RAS}$	80		90		ns	
t_{WCS}	TWLCEL	Write Command to $\overline{CAS}$ Set-Up Time	0		0		ns	13
t_{WCH}	TCELWX	Write Command Hold Time	35		45		ns	
t_{WP}	TWLWH	Write Command Pulse Width	40		45		ns	
t_{CWL}	TWLCEH	Write Command to $\overline{CAS}$ Lead Time	85		95		ns	
t_{RWL}	TWLREH	Write Command to $\overline{RAS}$ Lead Time	90		100		ns	
t_{WCR}	TRELWX	Write Command Hold Time Referenced to $\overline{RAS}$	90		100		ns	
t_{DS}	TDVWL	Data In Set-Up Time	0		0		ns	
t_{DH}	TWLDX	Data In Hold Time	35		40		ns	
t_{DHR}	TRELDX	Data In Hold Time Referenced to $\overline{RAS}$	90		100		ns	

Page Mode Write Cycle Waveforms*



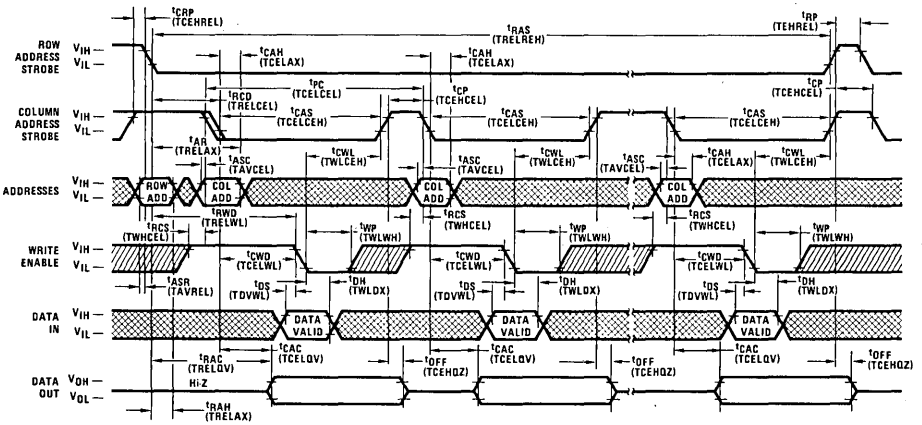
† Standard part not tested for page mode.

* Symbols in parentheses are proposed Industry standard.

Page Mode Read-Modify-Write Cycle AC Electrical Characteristics†

Symbol		Parameter	NMC4164-1		NMC4164-2		Units	Notes
Alternate	Standard		Min	Max	Min	Max		
t_{PC}	TRELREL	Page Mode Cycle Time	235		270		ns	14
t_{RAS}	TRELREH	$\overline{RAS}$ Pulse Width	445	10,000	510	10,000	ns	14
t_{RP}	TREHREL	$\overline{RAS}$ Precharge Time	120		130		ns	
t_T	TH1H2	Rise Time	3	50	3	50	ns	
t_T	TL2L1	Fall Time	3	50	3	50	ns	
t_{RCD}	TRELCEL	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	30	60	ns	5
t_{RSH}	TCELREH	$\overline{RAS}$ Hold Time	85		100		ns	
t_{CSH}	TRELCEH	$\overline{CAS}$ Hold Time	135		150		ns	13
t_{CAS}	TCELCEH	$\overline{CAS}$ Pulse Width	155	10,000	180	10,000	ns	14
t_{CP}	TCEHCEL	$\overline{CAS}$ Precharge Time, Page Mode	70		80		ns	6
t_{ASR}	TAVREL	Row Address Set-Up Time	0		0		ns	
t_{RAH}	TRELAX	Row Address Hold Time	20		25		ns	
t_{ASC}	TAVCEL	Column Address Set-Up Time	0		0		ns	
t_{CAH}	TCELAX	Column Address Hold Time	25		30		ns	
t_{AR}	TRELA(C)X	Column Address Hold Time Referenced to $\overline{RAS}$	80		90		ns	7
t_{RCS}	TWHCEL	Read Command Set-Up Time	0		0		ns	
t_{WP}	TWLWH	Write Command Pulse Width	40		45		ns	
t_{CWL}	TWLCEH	Write Command to $\overline{CAS}$ Lead Time	85		95		ns	
t_{RWL}	TWLREH	Write Command to $\overline{RAS}$ Lead Time	90		100		ns	
t_{RWD}	TRELWL	$\overline{RAS}$ to $\overline{WE}$ Delay	120		150		ns	13
t_{CWP}	TCELWL	$\overline{CAS}$ to $\overline{WE}$ Delay	65		90		ns	
t_{DS}	TDVWL	Data In Set-Up Time	0		0		ns	
t_{DH}	TWLDX	Data In Hold Time	35		40		ns	
t_{RAC}	TRELQV	Access Time from $\overline{RAS}$		120		150	ns	9, 10
t_{CAC}	TCELQV	Access Time from $\overline{CAS}$		65		90	ns	10, 11
t_{OFF}	TCEHQZ	Output Buffer Turn-Off Delay	0	50	0	55	ns	12

Page Mode Read-Modify-Write Waveforms*



† Standard part not tested for page mode.
* Symbols in parentheses are proposed industry standard.

AC Notes

Note 1: All voltages referenced to VSS.

Note 2: Any 8 cycles that perform refresh must be applied following either power on or periods of no Row Address Strobe activity exceeding 2 ms.

Note 3: Transition times are assumed to be 5 ns.

Note 4: Timing reference points are VIH(min) and VIL(max).

Note 5: If TRELCEL(min) ≤ TRELCEL ≤ TRELCEL(max) the access time is TRELQV (row timing limited). If the TRELCEL exceeds TRELCEL(max) the access time is TRELCEL plus TCELQV (column timing limited).

Note 6: TCEHCEL is necessary for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by a $\overline{CAS}$ only cycle or Page Mode cycles.

Note 7: (C) indicates that column addresses are referenced.

Note 8: TCEHWX is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.

Note 9: Load = 2 TTL loads and 100 pF.

Note 10: Assumes TRELCEL ≤ TRELCEL(max) (row limited timing).

Note 11: Assumes TRELCEL > (max) (column limited timing).

Note 12: TCEHQZ is measured to IOUT ≤ IO(L).

Note 13: The placement of the negative going edge of $\overline{W}$ with respect to the negative edge of $\overline{CAS}$ determines the type of Write cycle. If TWLCEL is greater than 0 ns (negative edge of $\overline{W}$ before negative edge of $\overline{CAS}$) the memory is in an Early-Write cycle and Data Out is TRI-STATE. If TCELWL is greater than TCELWL(min) (negative edge of $\overline{W}$ coincident with or after Data Out valid) the memory is in a Read-Write or Read-Modify-Write cycle and Data Out is the original contents of the selected cell. If $\overline{W}$ goes LOW between these two times the cycle is a Write cycle and Data Out is indeterminate.

Note 14: (R/W) indicates a Read-Write or Read-Modify-Write cycle parameter.

National Semiconductor

MOS RAMs
ADVANCE INFORMATION

NMC5295† 16,384-Bit (16,384 × 1) Dynamic RAM

General Description

The NMC5295 is a 16,384 × 1 bit dynamic RAM. It features a multiplexed address input with separate row and column strobes. This added flexibility allows the NMC5295 to be used in page mode operation.

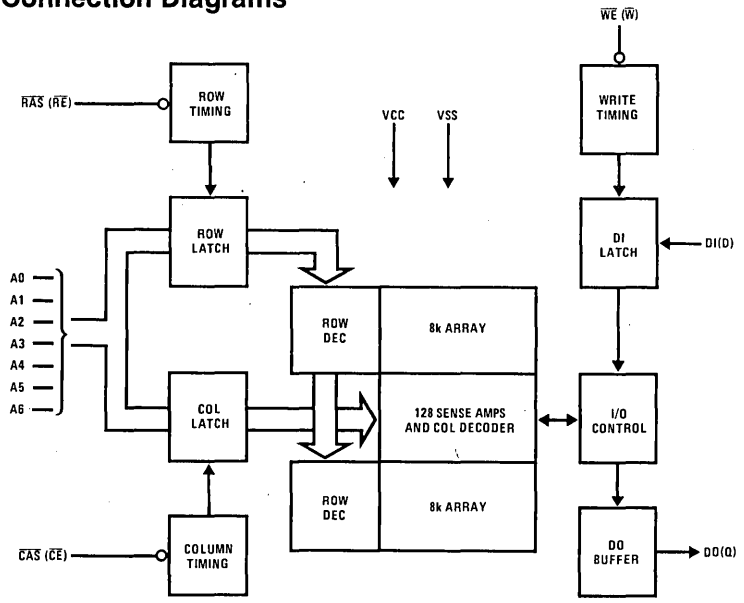
The NMC5295 must be refreshed every 2 ms. This can be accomplished by performing any cycle which brings the Row Address Strobe active including $\overline{RAS}$ ($\overline{RE}$)-only cycle at each of the 128 row addresses.

N-channel triple-polysilicon gate technology, developed by National, is used in the manufacture of the NMC5295. This process combines high density and performance with reliability. Greater system densities are achievable by the use of a 16-pin dual-in-line package for the NMC5295.

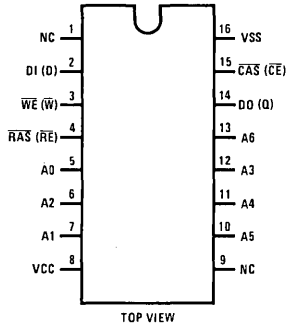
Features

- Single 5V ± 10% supply
- 128 cycle, 2 ms refresh
- Access times: 80 ns, 100 ns, 120 ns
- Low power: 200 mW max
- TTL compatible: all inputs and output
- Gated $\overline{CAS}$ ($\overline{CE}$)—non-critical timing
- Read, write, read-modify-write and $\overline{RAS}$ ($\overline{RE}$)-only refresh cycles
- Buried refresh option
- Page mode operation
- Industry standard 16-pin configuration
- TRI-STATE® output
- On-chip substrate bias generator

Block and Connection Diagrams**



Dual-In-Line Package



Order Number NMC5295J-X*
See NS Package J16A

Order Number NMC5295N-X*
See NS Package N16A

Pin Names

$\overline{RAS}$ ($\overline{RE}$)	Row Address Strobe
$\overline{CAS}$ ($\overline{CE}$)	Column Address Strobe
$\overline{WE}$ ($\overline{W}$)	Write Enable
A0-A6	Address Inputs
DI (D)	Data Input
DO (Q)	Data Output
VCC	Power (5V)
VSS	Ground

†See the MST™ Program, page 3.

** Symbols in parentheses are proposed industry standard.

* X = Speed selection

Absolute Maximum Ratings (Note 1)

Operating Temperature Range	0°C to +70°C	Voltage on Any Pin Relative to VSS	−1.0 to +7V
Storage Temperature	−65°C to +150°C	Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	1W		

Recommended DC Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
TA	Ambient Temperature	0	70	°C	
VCC	Supply Voltages	4.5	5.5	V	2, 3
VSS		0	0	V	2, 3
VIH	Input High Voltage, All Inputs	2.4	7.0	V	2
VIL	Input Low Voltage, All Inputs	−1.0	0.8	V	2

DC Electrical Characteristics

Over the range of Recommended DC Operating Conditions unless otherwise noted.

Symbol	Parameter	Min	Max	Units	Notes
ICC1	**Operating Current** Average Power Supply Operating Current ($\overline{RE}$, $\overline{CE}$ Cycling; TRELREL = TRELREL Min)		35	mA	4
ICC2	**Standby Current** Power Supply Standby Current ($\overline{RE}$ = VIH, Q = High Impedance)		4	mA	
ICC3	**Refresh Current** Average Power Supply Current, Refresh Mode ($\overline{RE}$ Cycling, $\overline{CE}$ = VIH; TRELREL = TRELREL Min)		27	mA	4
ICC4	**Page Mode Current** Average Power Supply Current, Page Mode ($\overline{RE}$ = VIL, $\overline{CE}$ Cycling; TCELCEL = 100 ns)		27	mA	4
II	**Input Leakage** Input Leakage Current, Any Input (0V ≤ VIN ≤ 7V, All Other Pins not Under Test = 0V)	−10	10	μA	
IOZ	**Output Leakage** Output Leakage Current (Q is Disabled, 0V ≤ VOUT ≤ 5.5V)	−10	10	μA	
	Output Levels				
VOH	Output High Voltage (IOUT = −5 mA)	2.4		V	
VOL	Output Low Voltage (IOUT = 4.2 mA)		0.4	V	

Capacitance

Symbol	Parameter	Max	Units	Notes
CI	Input Capacitance A0-A6, D	5	pF	5
CC	Input Capacitance $\overline{RE}$, $\overline{CE}$, $\overline{W}$	10	pF	5
CQ	Output Capacitance, Q	7	pF	5

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Recommended DC Operating Conditions" provides conditions for actual device operation.

Note 2: All voltages referenced to VSS. When applying voltage to the device, VCC should never be 1.0V more negative than VSS.

Note 3: Several cycles are required after power-up before proper device operation is achieved. Any 8 $\overline{RE}$ cycles are adequate for this purpose.

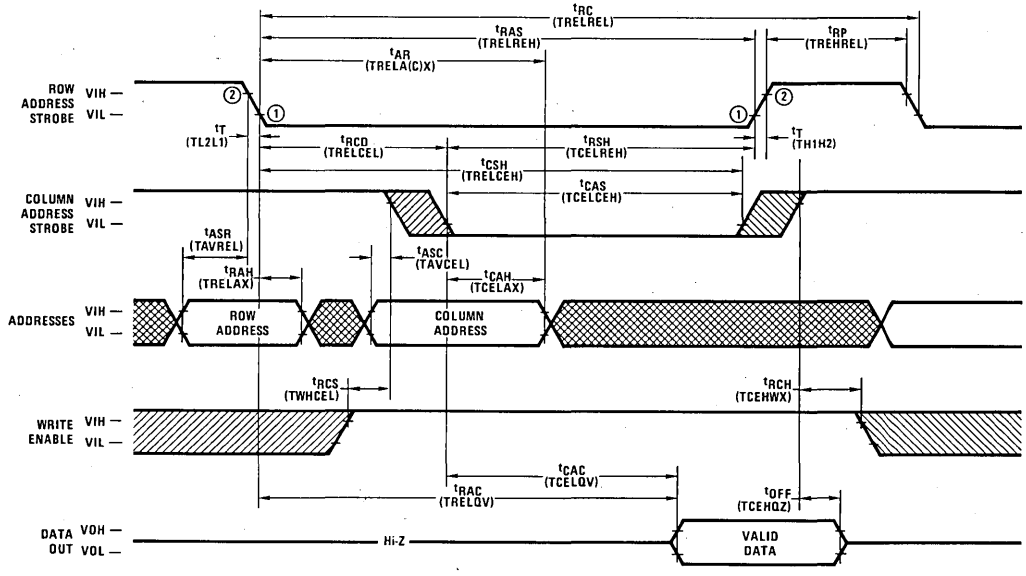
Note 4: ICC1, ICC3 and ICC4 depend on cycle rate.

Note 5: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$. Capacitance is guaranteed by periodic testing.

Read Cycle AC Electrical Characteristics (Notes 1, 2, 3 and 4)

Symbol		Parameter	NMC5295-2		NMC5295-3		NMC5295-4		Units	Notes
Alternate	Standard		Min	Max	Min	Max	Min	Max		
t_{RC}	TRELREL	Random Read Cycle Time	200		235		270		ns	
t_{RAS}	TRELREH	$\overline{RAS}$ Pulse Width	95	10,000	115	10,000	140	10,000	ns	
t_{RP}	TREHREL	$\overline{RAS}$ Precharge Time	95		110		120		ns	
t_T	TH1H2	Rise Time	3	50	3	50	3	50	ns	
t_T	TL2L1	Fall Time	3	50	3	50	3	50	ns	
t_{RCD}	TRELCEL	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	15	40	20	50	25	55	ns	5
t_{RSH}	TCELREH	$\overline{RAS}$ Hold Time	55		65		85		ns	
t_{CSH}	TRELCEH	$\overline{CAS}$ Hold Time	90		110		135		ns	
t_{CAS}	TCELCEH	$\overline{CAS}$ Pulse Width	50	10,000	60	10,000	80	10,000	ns	
t_{CP}	TCEHCEL	$\overline{CAS}$ Precharge Time	50		60		70		ns	6
t_{ASR}	TAVREL	Row Address Set-Up Time	0		0		0		ns	
t_{RAH}	TRELAX	Row Address Hold Time	10		15		20		ns	
t_{ASC}	TAVCEL	Column Address Set-Up Time	0		0		0		ns	
t_{CAH}	TCELAX	Column Address Hold Time	15		20		25		ns	
t_{AR}	TRELA(C)X	Column Address Hold Time Referenced to $\overline{RAS}$	55		70		80		ns	7
t_{RCS}	TWHCEL	Read Command Set-Up Time	0		0		0		ns	
t_{RCH}	TCEHWX	Read Command Hold Time	0		0		0		ns	8
t_{RAC}	TRELQV	Access Time from $\overline{RAS}$		80		100		120	ns	9, 10
t_{CAC}	TCELQV	Access Time from $\overline{CAS}$		40		50		65	ns	10, 11
t_{OFF}	TCEHQZ	Output Buffer Turn-Off Delay	0	40	0	45	0	50	ns	12

Read Cycle Waveforms*

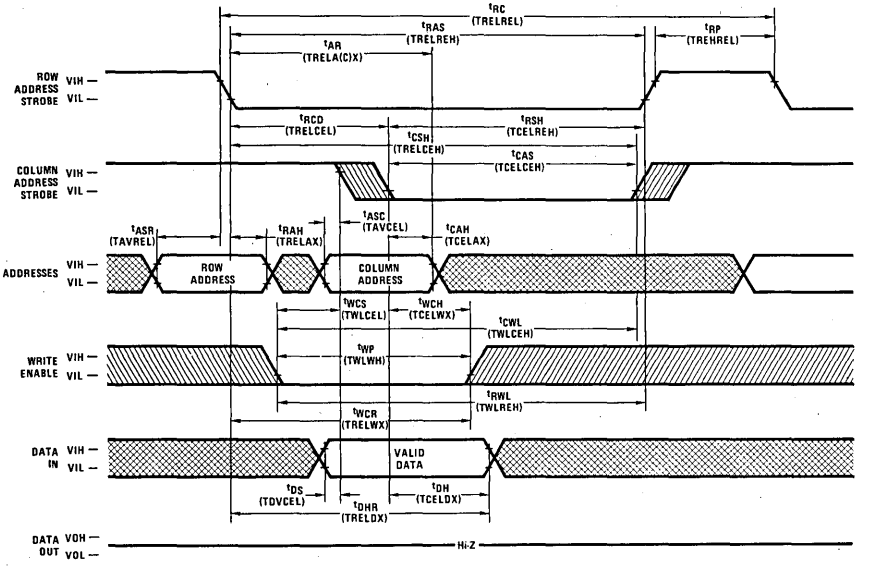


* Symbols in parentheses are proposed industry standard.

Write Cycle AC Electrical Characteristics (Notes 1, 2, 3 and 4)

Symbol		Parameter	NMC5295-2		NMC5295-3		NMC5295-4		Units	Notes
Alternate	Standard		Min	Max	Min	Max	Min	Max		
t_{WC}	TRELREL	Random Write Cycle Time	200		235		270		ns	
t_{RAS}	TRELREH	$\overline{RAS}$ Pulse Width	95	10,000	115	10,000	140	10,000	ns	
t_{RP}	TREHREL	$\overline{RAS}$ Precharge Time	95		110		120		ns	
t_T	TH1H2	Rise Time	3	50	3	50	3	50	ns	
t_T	TL2L1	Fall Time	3	50	3	50	3	50	ns	
t_{RCD}	TRELCEL	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	15	40	20	50	25	55	ns	
t_{RSH}	TCELREH	$\overline{RAS}$ Hold Time	55		65		85		ns	
t_{CSH}	TRELCEH	$\overline{CAS}$ Hold Time	90		110		135		ns	
t_{CAS}	TCELCEH	$\overline{CAS}$ Pulse Width	50	10,000	60	10,000	80	10,000	ns	
t_{CP}	TCEHCEL	$\overline{CAS}$ Precharge Time	50		60		70		ns	6
t_{ASR}	TAVREL	Row Address Set-Up Time	0		0		0		ns	
t_{RAH}	TRELAX	Row Address Hold Time	10		15		20		ns	
t_{ASC}	TAVCEL	Column Address Set-Up Time	0		0		0		ns	
t_{CAH}	TCELAX	Column Address Hold Time	15		20		25		ns	
t_{AR}	TRELA(C)X	Column Address Hold Time Referenced to $\overline{RAS}$	55		70		80		ns	
t_{WCS}	TWLCEL	$\overline{WE}$ to $\overline{CAS}$ Set-Up Time	0		0		0		ns	13
t_{WCH}	TCELWX	Write Command Hold Time	30		30		35		ns	
t_{WP}	TWLWH	Write Command Pulse Width	35		35		40		ns	
t_{CWL}	TWLCEH	Write Command to $\overline{CAS}$ Lead Time	55		65		85		ns	
t_{RWL}	TWLREH	Write Command to $\overline{RAS}$ Lead Time	60		70		90		ns	
t_{WCR}	TRELWX	Write Command Hold Time Referenced to $\overline{RAS}$	70		80		90		ns	
t_{DS}	TDVCEL	Data In Set-Up Time	0		0		0		ns	
t_{DH}	TCELDX	Data In Hold Time	30		30		30		ns	
t_{DHR}	TRELDX	Data In Hold Time Referenced to $\overline{RAS}$	70		80		90		ns	

Write Cycle (Early-Write) Waveforms* (Note 13)



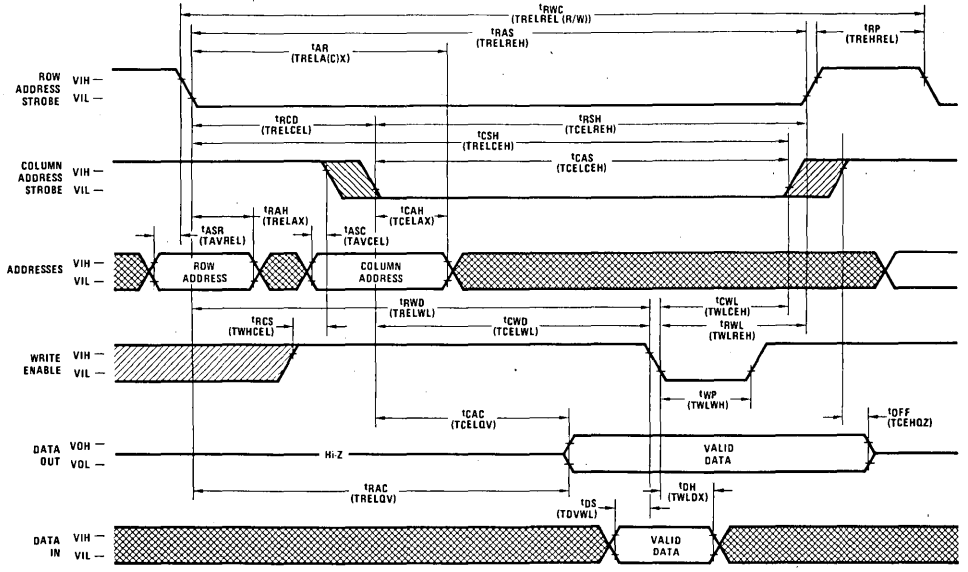
*Symbols in parentheses are proposed industry standard.

Read-Write and Read-Modify-Write Cycle AC Electrical Characteristics

(Notes 1, 2, 3 and 4)

Symbol		Parameter	NMC5295-2		NMC5295-3		NMC5295-4		Units	Notes
Alternate	Standard		Min	Max	Min	Max	Min	Max		
t_{RWC}	TRELREL (R/W)	Read-Write Cycle Time	250		295		345		ns	14
t_{RRW}	TRELREH (R/W)	$\overline{RAS}$ Pulse Width	145	10,000	175	10,000	215	10,000	ns	14
t_{RP}	TREHREL	$\overline{RAS}$ Precharge Time	95		110		120		ns	
t_T	TH1H2	Rise Time	3	50	3	50	3	50	ns	
t_T	TL2L1	Fall Time	3	50	3	50	3	50	ns	
t_{RCD}	TRELCEL	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	15	40	20	50	25	55	ns	5
t_{RSH}	TCELREH	$\overline{RAS}$ Hold Time	55		65		85		ns	
t_{CSH}	TRELCEH	$\overline{CAS}$ Hold Time	90		110		135		ns	
t_{CRW}	TCELCEH (R/W)	$\overline{CAS}$ Pulse Width	105	10,000	125	10,000	160	10,000	ns	14
t_{CP}	TCEHCEL	$\overline{CAS}$ Precharge Time	50		60		70		ns	6
t_{ASR}	TAVREL	Row Address Set-Up Time	0		0		0		ns	
t_{RAH}	TRELAX	Row Address Hold Time	10		15		20		ns	
t_{ASC}	TAVCEL	Column Address Set-Up Time	0		0		0		ns	
t_{CAH}	TCELAX	Column Address Hold Time	15		20		25		ns	
t_{AR}	TRELA(C)X	Column Address Hold Time Referenced to $\overline{RAS}$	55		70		80		ns	7
t_{RCS}	TWHCEL	Read Command Set-Up Time	0		0		0		ns	
t_{WP}	TWLWH	Write Command Pulse Width	35		35		40		ns	
t_{CWL}	TWLCEH	Write Command to $\overline{CAS}$ Lead Time	55		65		85		ns	
t_{RWL}	TWLREH	Write Command to $\overline{RAS}$ Lead Time	60		70		90		ns	
t_{RWD}	TRELWL	$\overline{RAS}$ to $\overline{WE}$ Delay	80		100		120		ns	
t_{CWD}	TCELWL	$\overline{CAS}$ to $\overline{WE}$ Delay	40		50		65		ns	13
t_{DS}	TDVWL	Data In Set-Up Time	0		0		0		ns	
t_{DH}	TWLDX	Data In Hold Time	30		30		35		ns	
t_{RAC}	TRELQV	Access Time from $\overline{RAS}$		80		100		120	ns	9, 10
t_{CAC}	TCELQV	Access Time from $\overline{CAS}$		40		50		65	ns	10, 11
t_{OFF}	TCEHQZ	Output Buffer Turn-Off Delay	0	40	0	45	0	50	ns	12

Read-Write and Read-Modify-Write Waveforms*

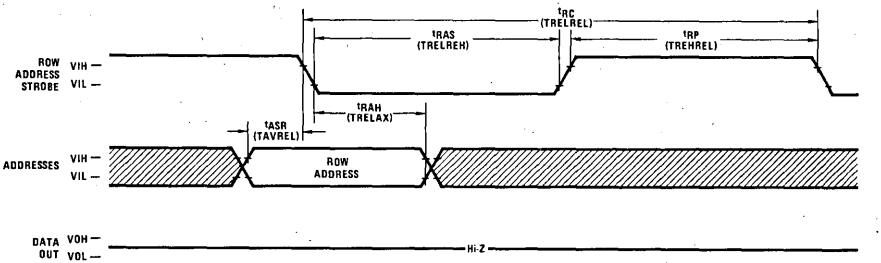


* Symbols in parentheses are proposed industry standard.

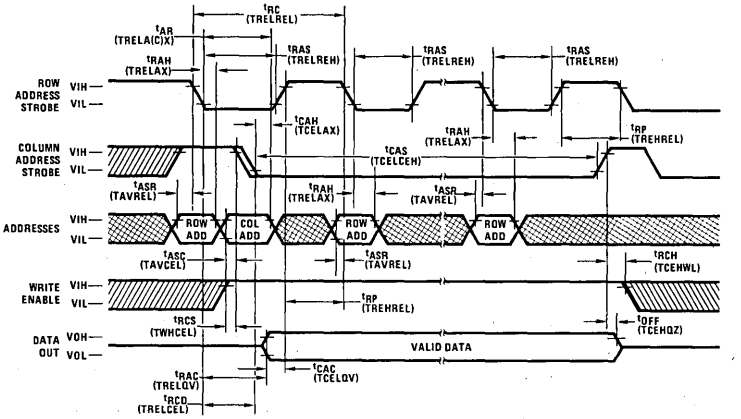
$\overline{RAS}$-Only Refresh and Buried Refresh AC Electrical Characteristics

Symbol		Parameter	NMC5295-2		NMC5295-3		NMC5295-4		Units	Notes
Alternate	Standard		Min	Max	Min	Max	Min	Max		
t_{RC}	TRELREL	Random Read or Write Cycle Time	200		235		270		ns	
t_{RAS}	TRELREH	$\overline{RAS}$ Pulse Width	95	10,000	115	10,000	140	10,000	ns	
t_{RP}	TREHREL	$\overline{RAS}$ Precharge Time	95		110		120		ns	
t_T	TH1H2	Rise Time	3	50	3	50	3	50	ns	
t_T	TL2L1	Fall Time	3	50	3	50	3	50	ns	
t_{RCD}	TRELCEL	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	15	40	20	50	25	55	ns	5
t_{RSH}	TCELREH	$\overline{RAS}$ Hold Time	55		65		85		ns	
t_{CSH}	TRELCEH	$\overline{CAS}$ Hold Time	90		110		135		ns	
t_{CAS}	TCELCEH	$\overline{CAS}$ Pulse Width	50		60		80		ns	15
t_{CP}	TCEHCEL	$\overline{CAS}$ Precharge Time	50		60		70		ns	6
t_{ASR}	TAVREL	Row Address Set-Up Time	0		0		0		ns	
t_{RAH}	TRELAX	Row Address Hold Time	10		15		20		ns	
t_{ASC}	TAVCEL	Column Address Set-Up Time	0		0		0		ns	
t_{CAH}	TCELAX	Column Address Hold Time	15		20		25		ns	
t_{AR}	TRELA(C)X	Column Address Hold Time Referenced to $\overline{RAS}$	55		70		80		ns	7
t_{RCS}	TWHCEL	Read Command Set-Up Time	0		0		0		ns	
t_{RCH}	TCEHWX	Read Command Hold Time	0		0		0		ns	8
t_{RAC}	TRELQV	Access Time from $\overline{RAS}$		80		100		120	ns	9, 10
t_{CAC}	TCELQV	Access Time from $\overline{CAS}$		40		50		65	ns	10, 11
t_{OFF}	TCEHQZ	Output Buffer Turn-Off Delay	0	40	0	45	0	50	ns	12

$\overline{RAS}$-Only Refresh Waveforms* ($\overline{CAS}$ = VIH, $\overline{WE}$ = don't care)



Buried Refresh Waveforms*

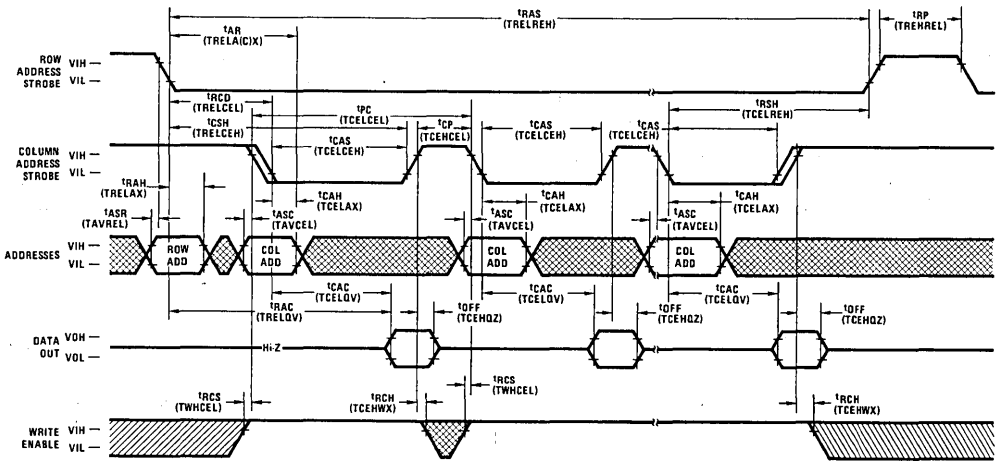


* Symbols in parentheses are proposed industry standard.

Page Mode Read Cycle AC Electrical Characteristics† (Notes 1, 2, 3 and 4)

Symbol		Parameter	NMC5295-2		NMC5295-3		NMC5295-4		Units	Notes
Alternate	Standard		Min	Max	Min	Max	Min	Max		
t_{PC}	TRELREL	Page Mode Cycle Time	110		130		160		ns	
t_{RAS}	TRELREH	$\overline{RAS}$ Pulse Width	205	10,000	245	10,000	300	10,000	ns	
t_{RP}	TREHREL	$\overline{RAS}$ Precharge Time	95		110		120		ns	
t_T	TH1H2	Rise Time	3	50	3	50	3	50	ns	
t_T	TL2L1	Fall Time	3	50	3	50	3	50	ns	
t_{RCD}	TRELCEL	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	15	40	20	50	25	55	ns	5
t_{RSH}	TCELREH	$\overline{RAS}$ Hold Time	55		65		85		ns	
t_{CSH}	TRELCEH	$\overline{CAS}$ Hold Time	90		110		135		ns	
t_{CAS}	TCELCEH	$\overline{CAS}$ Pulse Width	50	10,000	60	10,000	80	10,000	ns	
t_{CP}	TCEHCEL	$\overline{CAS}$ Precharge Time	50		60		70		ns	6
t_{ASR}	TAVREL	Row Address Set-Up Time	0		0		0		ns	
t_{RAH}	TRELAX	Row Address Hold Time	10		15		20		ns	
t_{ASC}	TAVCEL	Column Address Set-Up Time	0		0		0		ns	
t_{CAH}	TCELAX	Column Address Hold Time	15		20		25		ns	
t_{AR}	TRELA(C)X	Column Address Hold Time Referenced to $\overline{RAS}$	55		70		80		ns	7
t_{RCS}	TWHCEL	Read Command Set-Up Time	0		0		0		ns	
t_{RCH}	TCEHWX	Read Command Hold Time	0		0		0		ns	8
t_{RAC}	TRELQV	Access Time from $\overline{RAS}$		80		100		120	ns	9, 10
t_{CAC}	TCELQV	Access Time from $\overline{CAS}$		40		50		65	ns	10, 11
t_{OFF}	TCEHQZ	Output Buffer Turn-Off Delay	0	40	0	45	0	50	ns	12

Page Mode Read Cycle Waveforms*



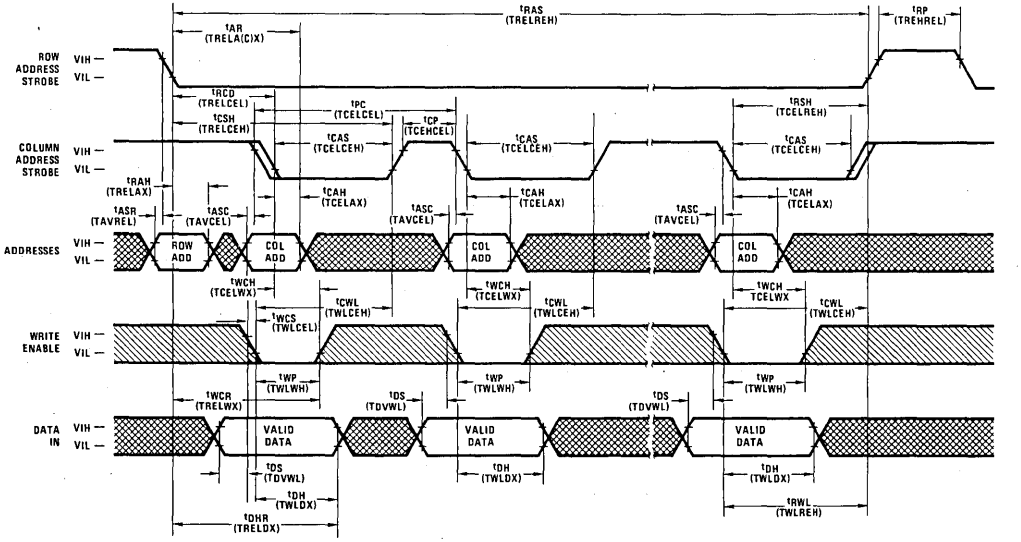
† Standard part not tested for page mode.

* Symbols in parentheses are proposed industry standard.

Page Mode Write Cycle AC Electrical Characteristics†

Symbol		Parameter	NMC5295-2		NMC5295-3		NMC5295-4		Units	Notes
Alternate	Standard		Min	Max	Min	Max	Min	Max		
t_{PC}	TRELREL	Page Mode Cycle Time	110		130		160		ns	
t_{RAS}	TRELREH	$\overline{RAS}$ Pulse Width	205	10,000	245	10,000	300	10,000	ns	
t_{RP}	TREHREL	$\overline{RAS}$ Precharge Time	95		110		120		ns	
t_T	TH1H2	Rise Time	3	50	3	50	3	50	ns	
t_T	TL2L1	Fall Time	3	50	3	50	3	50	ns	
t_{RCD}	TRELCEL	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	15	40	20	50	25	55	ns	
t_{RSH}	TCELREH	$\overline{RAS}$ Hold Time	55		65		85		ns	
t_{CSH}	TRELCEH	$\overline{CAS}$ Hold Time	90		110		135		ns	
t_{CAS}	TCELCEH	$\overline{CAS}$ Pulse Width	50	10,000	60	10,000	80	10,000	ns	
t_{CP}	TCEHCEL	$\overline{CAS}$ Precharge Time	50		60		70		ns	6
t_{ASR}	TAVREL	Row Address Set-Up Time	0		0		0		ns	
t_{RAH}	TRELAX	Row Address Hold Time	10		15		20		ns	
t_{ASC}	TAVCEL	Column Address Set-Up Time	0		0		0		ns	
t_{CAH}	TCELAX	Column Address Hold Time	15		20		25		ns	
t_{AR}	TRELA(C)X	Column Address Hold Time Referenced to $\overline{RAS}$	55		70		80		ns	
t_{WCS}	TWLCEL	$\overline{WE}$ to $\overline{CAS}$ Set-Up Time	0		0		0		ns	13
t_{WCH}	TCELWX	Write Command Hold Time	30		30		35		ns	
t_{WP}	TWLWH	Write Command Pulse Width	35		35		40		ns	
t_{CWL}	TWLCEH	Write Command to $\overline{CAS}$ Lead Time	55		65		85		ns	
t_{RWL}	TWLREH	Write Command to $\overline{RAS}$ Lead Time	60		70		90		ns	
t_{WCR}	TRELWX	Write Command Hold Time Referenced to $\overline{RAS}$	70		80		90		ns	
t_{DS}	TDVCEL	Data In Set-Up Time	0		0		0		ns	
t_{DH}	TWLDX	Data In Hold Time	30		30		35		ns	
t_{DHR}	TRELDX	Data In Hold Time Referenced to $\overline{RAS}$	70		80		90		ns	

Page Mode Write Cycle Waveforms*



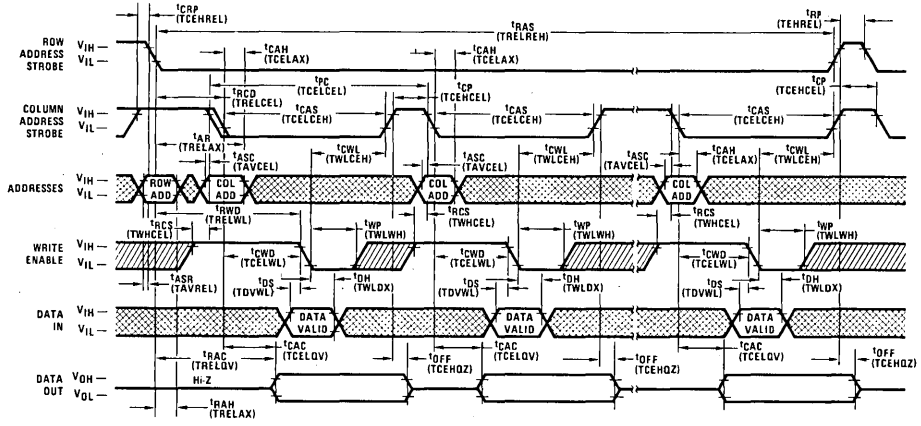
†Standard part not tested for page mode.

*Symbols in parentheses are proposed industry standard.

Page Mode Read-Modify-Write Cycle AC Electrical Characteristics†

Symbol		Parameter	NMC5295-2		NMC5295-3		NMC5295-4		Units	Notes
Alternate	Standard		Min	Max	Min	Max	Min	Max		
t_{PC}	TRELREL (R/W)	Read-Write Cycle Time	160		190		235		ns	14
t_{RAS}	TRELREH (R/W)	$\overline{RAS}$ Pulse Width	300	10,000	360	10,000	445	10,000	ns	14
t_{RP}	TREHREL	$\overline{RAS}$ Precharge Time	95		110		120		ns	
t_T	TH1H2	Rise Time	3	50	3	50	3	50	ns	
t_T	TL2L1	Fall Time	3	50	3	50	3	50	ns	
t_{RCD}	TRELCEL	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	15	40	20	50	25	55	ns	5
t_{RSH}	TCELREH	$\overline{RAS}$ Hold Time	55		65		85		ns	
t_{CSH}	TRELCEH	$\overline{CAS}$ Hold Time	90		110		135		ns	13
t_{CAS}	TCELCEH (R/W)	$\overline{CAS}$ Pulse Width	100	10,000	120	10,000	155	10,000	ns	14
t_{CP}	TCEHCEL	$\overline{CAS}$ Precharge Time	50		60		70		ns	6
t_{ASR}	TAVREL	Row Address Set-Up Time	0		0		0		ns	
t_{RAH}	TRELAX	Row Address Hold Time	10		15		20		ns	
t_{ASC}	TAVCEL	Column Address Set-Up Time	0		0		0		ns	
t_{CAH}	TCELAX	Column Address Hold Time	15		20		25		ns	
t_{AR}	TRELA(C)X	Column Address Hold Time Referenced to $\overline{RAS}$	55		70		80		ns	7
t_{RCS}	TWHCEL	Read Command Set-Up Time	0		0		0		ns	
t_{WP}	TWLWH	Write Command Pulse Width	35		35		40		ns	
t_{CWL}	TWLCEH	Write Command to $\overline{CAS}$ Lead Time	55		65		85		ns	
t_{RWL}	TWLREH	Write Command to $\overline{RAS}$ Lead Time	60		70		90		ns	
t_{RWD}	TRELWL	$\overline{RAS}$ to $\overline{WE}$ Delay	80		100		120		ns	13
t_{CWD}	TCELWL	$\overline{CAS}$ to $\overline{WE}$ Delay	40		50		65		ns	
t_{DS}	TDVWL	Data-In Set-Up Time	0		0		0		ns	
t_{DH}	TWLDX	Data-In Hold Time	30		30		35		ns	
t_{RAC}	TRELQV	Access Time from $\overline{RAS}$		80		100		120	ns	9, 10
t_{CAC}	TCELQV	Access Time from $\overline{CAS}$		40		50		65	ns	10, 11
t_{OFF}	TCEHQZ	Output Buffer Turn-Off Delay	0	40	0	45	0	50	ns	12

Page Mode Read-Modify-Write Waveforms*



† Standard part not tested for page mode.
* Symbols in parentheses are proposed industry standard.

AC Notes

Note 1: All voltages referenced to VSS.

Note 2: Any 8 cycles that perform refresh must be applied following either power on or periods of no Row Address Strobe activity exceeding 2 ms.

Note 3: Transition times are assumed to be 5 ns.

Note 4: Timing reference points are VIH(min) and VIL(max).

Note 5: If TRELCEL(min) ≤ TRELCEL ≤ TRELCEL(max) the access time is TRELQV (row timing limited). If the TRELCEL exceeds TRELCEL(max) the access time is TRELCEL plus TCELQV (column timing limited).

Note 6: TCEHCEL is necessary for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by a $\overline{CAS}$ only cycle or Page Mode cycles.

Note 7: (C) indicates that column addresses are referenced.

Note 8: TCEHWX is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.

Note 9: Load = 2 TTL loads and 100 pF.

Note 10: Assumes TRELCEL ≤ TRELCEL(max) (row limited timing).

Note 11: Assumes TRELCEL > (max) (column limited timing).

Note 12: TCEHQZ is measured to IOUT ≤ IO(L).

Note 13: The placement of the negative going edge of $\overline{W}$ with respect to the negative edge of $\overline{CAS}$ determines the type of Write cycle. If TWLCEL is greater than 0 ns (negative edge of $\overline{W}$ before negative edge of $\overline{CAS}$) the memory is in an Early-Write cycle and Data Out is TRI-STATE. If TCELWL is greater than TCELWL(min) (negative edge of $\overline{W}$ coincident with or after Data Out valid) the memory is in a Read-Write or Read-Modify-Write cycle and Data Out is the original contents of the selected cell. If $\overline{W}$ goes LOW between these two times the cycle is a Write cycle and Data Out is indeterminate.

Note 14: (R/W) indicates a Read-Write or Read-Modify-Write cycle parameter.

Note 15: Max limit does not apply for $\overline{RAS}$-Only Refresh. During Buried Refresh $\overline{CAS}$ can be low and valid output maintained for any desired period of time.

Section 2

CMOS RAMs

2

CMOS RAMs provide the lowest power of any of the semiconductor read/write memory technologies. National's CMOS memory line may be mixed with our CMOS logic, TTL logic, bipolar microprocessor, MOS microprocessor, custom LSI, and our other semiconductor products to optimize system power/speed/cost tradeoffs. Refer to National's related databooks and catalogs for further details: an order form is included in this book.

National Semiconductor

CMOS RAMs

MM54C89/MM74C89 64-Bit (16 × 4) TRI-STATE® RAM

General Description

The MM54C89/MM74C89 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a write enable line and a memory enable line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register, latches the address information on the positive to negative transition of the memory enable input. The four TRI-STATE® data output lines working in conjunction with the memory enable input provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note: The timing is different than the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

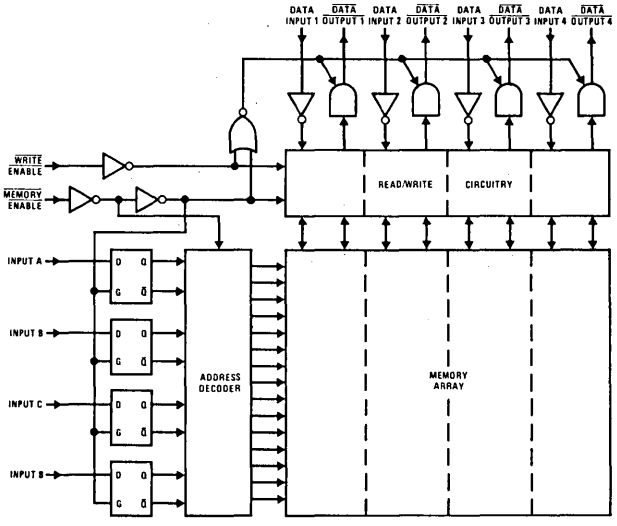
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the four outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

When the device is writing or disabled the output assumes a TRI-STATE (Hi-z) condition.

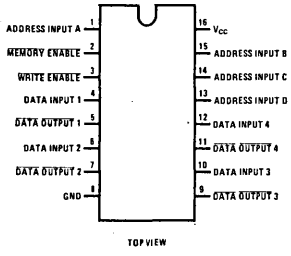
Features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- Low power TTL compatibility — fan out of 2 driving 74L
- Input address register
- Low power consumption — 100 nW/package typ @ V_{CC} = 5V
- Fast access time — 130 ns typ at V_{CC} = 10V
- TRI-STATE output

Logic and Connection Diagrams



Dual-In-Line Package



Order Number MM54C89J or MM74C89J
See NS Package J16A

Order Number MM74C89N
See NS Package N16A

Absolute Maximum Ratings

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

Ambient Temperature Range	
MM54C89	−55°C to +125°C
MM74C89	−40°C to +85°C
Supply Voltage Range	
MM54C89	3V to 15V
MM74C89	3V to 15V

DC Electrical Characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Output Current in High Impedance State	V_{CC} = 15V, V_O = 15V		0.005	1.0	μA
	V_{CC} = 15V, V_O = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
	74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = +360μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = +360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

AC Electrical Characteristics (T_A = 25°C, C_L = 50 pF, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from $\overline{\text{Memory Enable}}$ (t_{pd})	V_{CC} = 5.0V		270	500	ns
	V_{CC} = 10V		100	220	ns
Access Time from Address Input (t_{acc})	V_{CC} = 5.0V		350	650	ns
	V_{CC} = 10V		130	280	ns
Address Input Setup Time (t_{SA})	V_{CC} = 5.0V	150			ns
	V_{CC} = 10V	60			ns
Address Input Hold Time (t_{HA})	V_{CC} = 5.0V	60			ns
	V_{CC} = 10V	40			ns
$\overline{\text{Memory Enable}}$ Pulse Width (t_{ME})	V_{CC} = 5.0V	400	250		ns
	V_{CC} = 10V	150	90		ns
$\overline{\text{Memory Enable}}$ Pulse Width ($t_{\overline{ME}}$)	V_{CC} = 5.0V	400	200		ns
	V_{CC} = 10V	150	70		ns

AC Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Setup Time for a Read (t_{SR})	V_{CC} = 5.0V V_{CC} = 10V	0 0			ns ns
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Setup Time for a Write (t_{WS})	V_{CC} = 5.0V V_{CC} = 10V			t_{ME} t_{ME}	ns ns
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Pulse Width ($t_{W\overline{E}}$)	V_{CC} = 5.0V, t_{WS} = 0 V_{CC} = 10V, t_{WS} = 0	300 100	160 60		ns ns
Data Input Hold Time (t_{HD})	V_{CC} = 5.0V V_{CC} = 10V	50 25			ns ns
Data Input Setup (t_{SD})	V_{CC} = 5.0V V_{CC} = 10V	50 25			ns ns
Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from $\overline{\text{Memory}}$ $\overline{\text{Enable}}$ (t_{1H}, t_{OH})	V_{CC} = 5.0V, C_L = 5.0 pF, R_L = 10k V_{CC} = 10V, C_L = 5.0 pF, R_L = 10k		180 85	300 120	ns ns
Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from $\overline{\text{Write}}$ $\overline{\text{Enable}}$ (t_{1H}, t_{OH})	V_{CC} = 5.0V, C_L = 5.0 pF, R_L = 10k V_{CC} = 10V, C_L = 5.0 pF, R_L = 10k		180 85	300 120	ns ns
Input Capacity (C_{IN})	Any Input (Note 2)		5.0		pF
Output Capacity (C_{OUT})	Any Output (Note 2)		6.5		pF
Power Dissipation Capacity (C_{pd})	(Note 3)		230		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

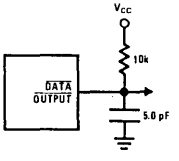
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Truth Table

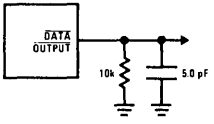
ME	WE	OPERATION	CONDITION OF OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	TRI-STATE
H	H	Inhibit, Storage	TRI-STATE

AC Test Circuits

t_{0H}

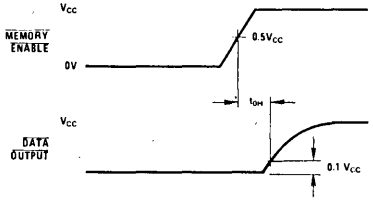


t_{1H}

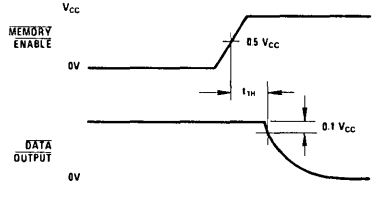


Switching Time Waveforms

t_{0H}

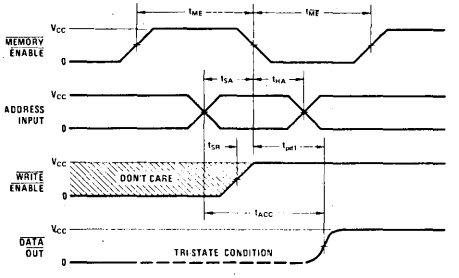


t_{1H}

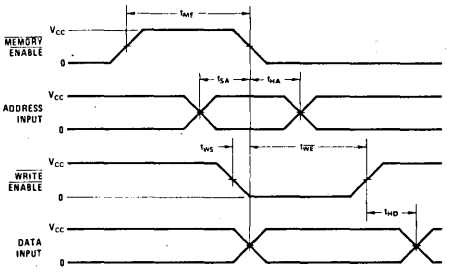


Switching Time Waveforms (Continued)

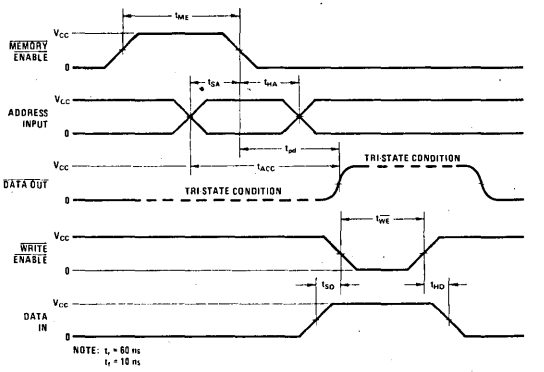
Read Cycle



Write Cycle



Read Modify Write Cycle



National Semiconductor

CMOS RAMs

MM54C200/MM74C200
256-Bit (256 x 1) TRI-STATE® RAM

General Description

The MM54C200/MM74C200 is a 256-bit random access read/write memory. Inputs consist of eight address lines, a data input line, a write enable line, and three chip enables. The eight binary address inputs are decoded internally to select each of the 256 locations. An internal address register, latches and address information on the positive to negative edge of $\overline{CE}_3$. The TRI-STATE data output line working in conjunction with $\overline{CE}_1$ or $\overline{CE}_2$ inputs provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of $\overline{CE}_3$. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition).

Note: The timing is different than the DM74200 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

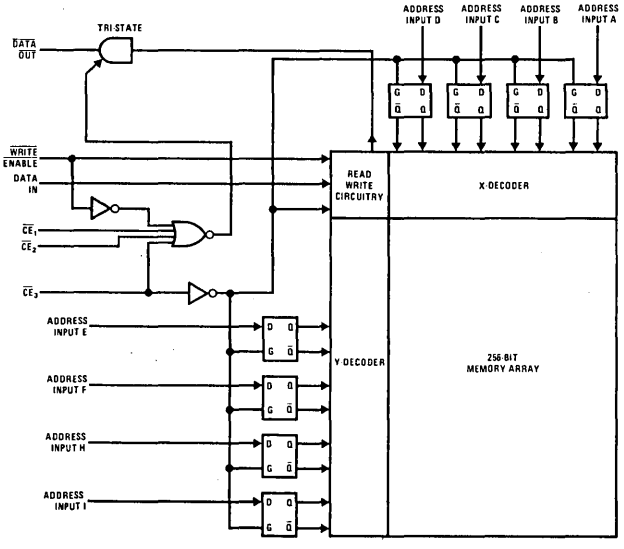
Read Operation: The data is read out by selecting the proper address and bringing $\overline{CE}_3$ low and write enable high. Holding $\overline{CE}_1$ or $\overline{CE}_2$ or $\overline{CE}_3$ at a high level forces the output into TRI-STATE. When used in bus organized systems, $\overline{CE}_1$, or $\overline{CE}_2$, a TRI-STATE control, provides for fast access times by not totally disabling the chip.

Write Operation: Data is written into the memory with $\overline{CE}_3$ low and write enable low. The state of $\overline{CE}_1$ or $\overline{CE}_2$ has no effect on the write cycle. The output assumes TRI-STATE with write enable low.

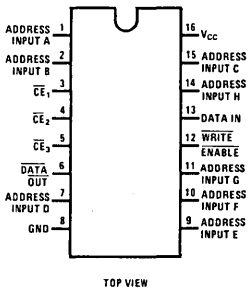
Features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- TTL compatibility — fan out of 1 driving standard TTL
- Low power — 500 nW typ
- Internal address register

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM54C200J or MM74C200J
See NS Package J16A

Order Number MM74C200N
See NS Package N16A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

Ambient Temperature Range	
MM54C200	−55°C to +125°C
MM74C200	−40°C to +85°C
Supply Voltage Range	
MM54C200	3V to 15V
MM74C200	3V to 15V

DC Electrical Characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9.0			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA			0.5 1.0	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.10	600	μA
CMOS/TTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −1.6 mA 74C, V_{CC} = 4.75V, I_O = −1.6 mA	2.4 2.4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 1.6 mA 74C, V_{CC} = 4.75V, I_O = 1.6 mA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	−4.0 −1.8	−6.0		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−16.0 −1.50	−25		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	5.0	8.0		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	20.0	30		mA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Access Time From Address (t_{ACC})	V_{CC} = 5.0V V_{CC} = 10V		450 200	900 400	ns ns
Propagation Delay From $\overline{CE}_3$ (t_{pd})	V_{CC} = 5.0V V_{CC} = 10V		360 120	700 300	ns ns
Propagation Delay From $\overline{CE}_1$ or $\overline{CE}_2$ ($t_{p\overline{CE}1}$)	V_{CC} = 5.0V V_{CC} = 10V		250 85	500 200	ns ns
Address Setup Time (t_{SA})	V_{CC} = 5.0V V_{CC} = 10V	200 100	80 30		ns ns
Address Hold Time (t_{HA})	V_{CC} = 5.0V V_{CC} = 10V	50 25	15 5		ns ns

AC Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Pulse Width ($t_{\overline{WE}}$)	V_{CC} = 5.0V	300	160		ns
	V_{CC} = 10V	150	70		ns
$\overline{CE}_3$ Pulse Widths (t_{CE})	V_{CC} = 5.0V	400	200		ns
	V_{CC} = 10V	160	80		ns
Input Capacity (C_{IN})	Any Input (Note 2)		5.0		pF
Output Capacity in TRI-STATE (C_{OUT})	(Note 2)		9.0		pF
Power Dissipation Capacity (C_{pd})	(Note 3)		400		pF

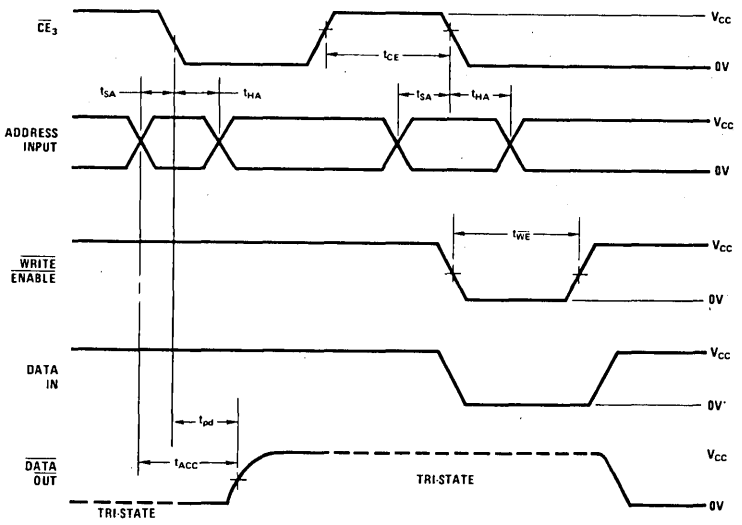
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

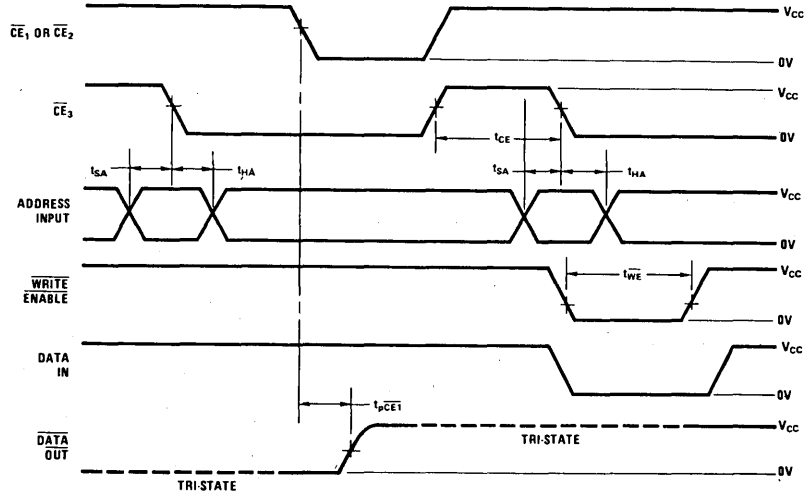
Note 3: C_{pd} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Switching Time Waveforms

Read and Write Cycles Using $\overline{CE}_3$ ($\overline{CE}_1$ = $\overline{CE}_2$ = logic 0)



Read and Write Cycles Using $\overline{CE}_3$ and $\overline{CE}_1$ (or $\overline{CE}_2$)



Note: Used for fast access time in bused systems.

National Semiconductor

CMOS RAMs

MM54C910/MM74C910 256-Bit (64 x 4) TRI-STATE® RAM

General Description

The MM54C910/MM74C910 is a 64 word by 4 bit random access memory. Inputs consist of six address lines, four data input lines, a write enable, and a memory enable line. The six address lines are internally decoded to select one of 64 word locations. An internal address register, latches the address information on the positive to negative transition of memory enable. The TRI-STATE outputs allow for easy memory expansion.

Address Operation: Address inputs must be stable (t_{SA}) prior to the positive to negative transition of memory enable, and (t_{HA}) after the positive to negative transition of memory enable. The address register holds the information and stable address inputs are not needed at any other time.

Write Operation: Data is written into memory at the selected address if write enable goes low while memory enable is low. Write enable must be held low for t_{WE} and data must remain stable t_{HD} after write enable returns high.

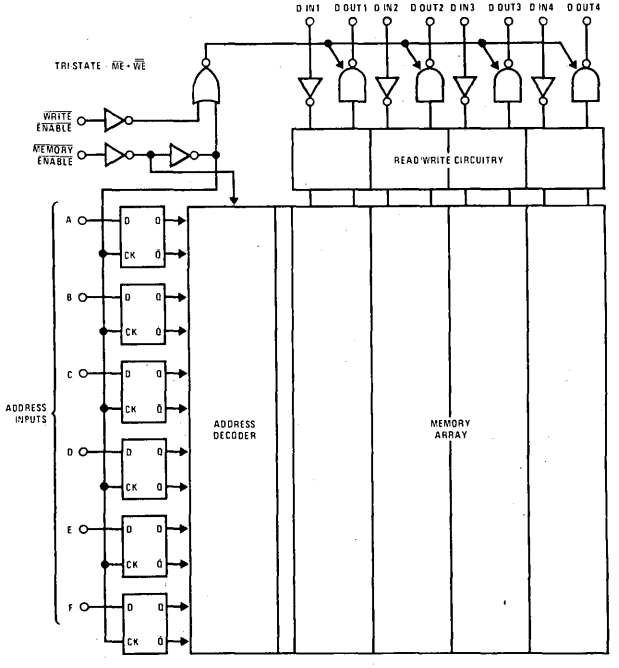
Read Operation: Data is nondestructively read from a memory location by an address operation with write enable held high.

Outputs are in the TRI-STATE (Hi-Z) condition when the device is writing or disabled.

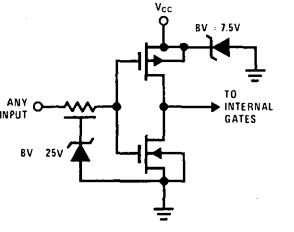
Features

- Supply voltage range — 3V to 5.5V
- High noise immunity — 0.45 V_{CC} typ
- TTL compatible fan out — 1 TTL load
- Input address register
- Low power consumption — 250 nW/package typ (chip enabled or disabled)
- Fast access time — 250 ns typ at 5V
- TRI-STATE outputs
- High voltage inputs

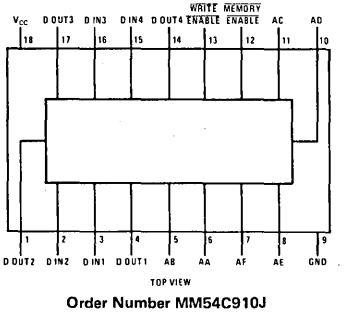
Logic and Connection Diagrams



Input Protection



Dual-In-Line Package



Order Number MM54C910J or MM74C910J
See NS Package J18A

Order Number MM74C910N
See NS Package N18A

Absolute Maximum Ratings (Note 1)

Voltage At Any Output Pin	−0.3V to V_{CC} +0.3V
Voltage At Any Input Pin	−0.3V to +15V
Package Dissipation	500 mW
Absolute Maximum V_{CC}	6.0V
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
MM54C910	4.5	5.5	V
MM74C910	4.75	5.25	V
Temperature (T_A)			
MM54C910	−55	+125	°C
MM74C910	−40	+85	°C
Operating V_{CC} Range			3.0V to 5.5V
Standby V_{CC} Range			1.5V to 5.5V

DC Electrical Characteristics MM54C910/MM74C910

(Min/max limits apply across the temperature and power supply range indicated).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	Full Range	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	Full Range			0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 15V		0.005	2	μA
		V_{IN} = 5V		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0V	−1	−0.005		μA
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −150μA	V_{CC}−0.5			V
		I_O = −400μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 1.6 mA			0.4	V
	Output Current in High	V_O = 5V		0.005	1	μA
	Impedence State	V_O = 0V	−1	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 5V		0.05	300	μA

AC Electrical Characteristics MM54C910/MM74C910

T_A = 25°C, V_{CC} = 5V, C_L = 50 pF

PARAMETER		MIN	TYP	MAX	UNITS
t_{ACC}	Access Time from Address		250	500	ns
t_{PD}	Propagation Delay from $\overline{ME}$		180	360	ns
t_{SA}	Address Input Set-Up Time	140	70		ns
t_{HA}	Address Input Hold Time	20	10		ns
t_{ME}	$\overline{\text{Memory Enable}}$ Pulse Width	200	100		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	400	200		ns
t_{SD}	Data Input Set-Up Time	0			ns
t_{HD}	Data Input Hold Time	30	15		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	140	70		ns
t_{1H}, t_{OH}	Delay to TRI-STATE (Note 4)		100	200	ns
CAPACITANCE					
C_{IN}	Input Capacity				
	Any Input (Note 2)		5		pF
C_{OUT}	Output Capacity				
	Any Output (Note 2)		9		pF
C_{PD}	Power Dissipation Capacity (Note 3)		350		pF

AC Electrical Characteristics (Continued)

C_L = 50 pF

PARAMETER		MM54C910 T_A = −55°C to +125°C V_{CC} = 4.5V to 5.5V		MM74C910 T_A = −40°C to +85°C V_{CC} = 4.75V to 5.25V		UNITS
		MIN	MAX	MIN	MAX	
t_{ACC}	Access Time from Address		860		700	ns
t_{PD1}, t_{PD0}	Propagation Delay from $\overline{ME}$		660		540	ns
t_{SA}	Address Input Set-Up Time	200		160		ns
t_{HA}	Address Input Hold Time	20		20		ns
t_{ME}	$\overline{\text{Memory Enable}}$ Pulse Width	280		260		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	750		600		ns
t_{SD}	Data Input Set-Up Time	0		0		ns
t_{HD}	Data Input Hold Time	50		50		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	200		180		ns
t_{1H}, t_{0H}	Delay to TRI-STATE (Note 4)		200		200	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

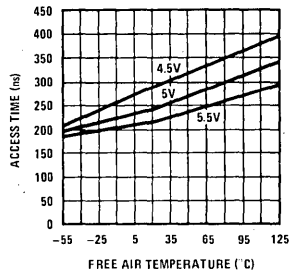
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{pd} determines the no load ac power consumption for any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Note 4: See ac test circuit for t_{1H}, t_{0H}.

Typical Performance Characteristics

Typical Access Time vs Ambient Temperature

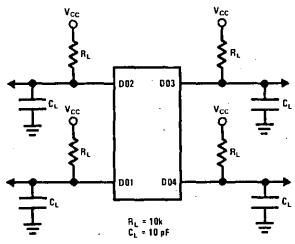


Truth Table

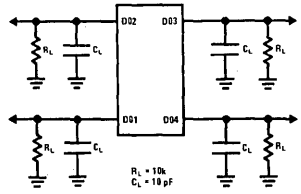
$\overline{ME}$	$\overline{WE}$	OPERATION	OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Data
H	L	Inhibit, Store	TRI-STATE
H	H	Inhibit, Store	TRI-STATE

AC Test Circuits

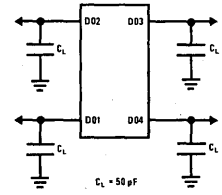
t_{0H}



t_{1H}

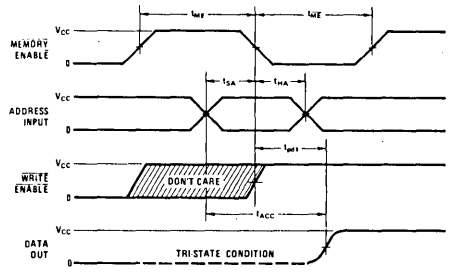


All Other AC Tests

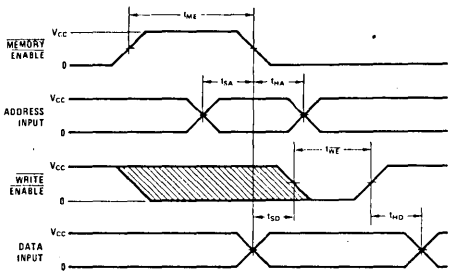


Switching Time Waveforms

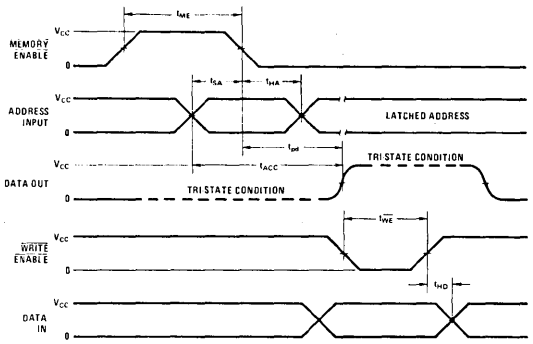
Read Cycle
(See Note 1)



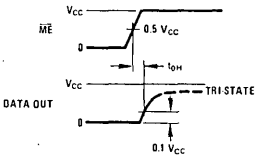
Write Cycle
(See Note 1)



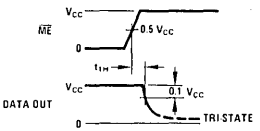
Read Modify Write Cycle
(See Note 1)



t_{0H}



t_{1H}



Note 1: $\overline{\text{MEMORY ENABLE}}$ must be brought high for t_{ME} nanoseconds between every address change.
Note 2: $t_r = t_f = 20$ ns for all inputs.

National Semiconductor

CMOS RAMs

MM54C920/MM74C920, MM54C921/MM74C921 1024-Bit (256 x 4) Static RAMs

General Description

The MM54C920/MM74C920 256 x 4 random access read/write memory is manufactured using silicon gate CMOS technology. Data output is the same polarity as data input. Internal latches store address inputs, $\overline{CES}$ and data output. This RAM is specifically designed to operate from standard 54/74 TTL power supplies. All inputs and outputs are TTL compatible.

The MM54C921/MM74C921 is identical to the MM54C920/MM74C920, except data inputs are internally connected to data outputs; the number of package leads thereby is reduced to 18.

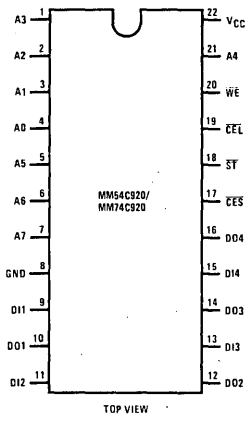
Complete address decoding as well as 2-chip select functions, $\overline{CEL}$ and $\overline{CES}$, and TRI-STATE® outputs allow easy expansion with a minimum of external components. Versatility plus high speed and low power make these RAMs ideal elements for use in microprocessor, minicomputer as well as main frame memory applications.

Features

- 256 x 4-bit organization
- Access time
  - 250 ns max MM74C920, MM74C921
  - 275 ns max MM54C920, MM54C921
  - 300 ns max MM74C921-3
- TRI-STATE outputs
- Low power
- On-chip registers
- Single 5V supply
- Data retained with V_{CC} as low as 2V

Connection Diagrams

Dual-In-Line Package

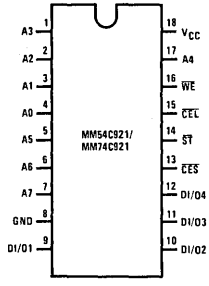


TOP VIEW

Order Number MM54C920J, MM74C920J or MM74C920J-3
See NS Package J22A

Order Number MM74C920N or MM74C920N-3
See NS Package N22A

Dual-In-Line Package

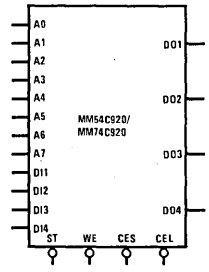


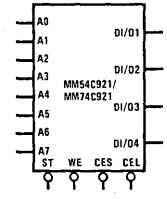
TOP VIEW

Order Number MM54C921J, MM74C921J or MM74C921J-3
See NS Package J18A

Order Number MM74C921N or MM74C921N-3
See NS Package N18A

Logic Symbols





Functional Description

The functional description will reference the logic diagram of the MM54C920/MM74C920 shown in *Figure 1.* Input addresses and $\overline{CES}$ are clocked into the input latches by the falling edge of $\overline{STROBE}$. Input set-up and hold times must be observed on these signals (see timing diagrams): The true and complement address information is fed to the row and column decoders which access the selected 4-bit memory word.

The addressed word (4 bits) is fed to 4 sense amplifiers through the column decoders. The information from the sense amplifiers is latched into the output register when $\overline{STROBE}$ rises. The register drives the TRI-STATE output buffers.

Chip select inputs, $\overline{CEL}$ and $\overline{CES}$, have identical functions except that $\overline{CES}$ (Chip Enable Stored) is clocked into a latch on the falling edge of $\overline{STROBE}$; $\overline{CEL}$ (Chip Enable Level) is not.

Note that set-up and hold times must be observed on $\overline{CES}$. Because $\overline{CEL}$ is not clocked by $\overline{STROBE}$, it may fall after $\overline{STROBE}$ has fallen without affecting access time provided that the t_{OE} requirement is met.

The outputs are in a high impedance state when the chip is not selected ($\overline{CES}$ or $\overline{CEL}$ high) or when writing ($\overline{WE}$ low). Note that the information stored in the output latches will be changed whenever $\overline{STROBE}$ falls, regardless of the logic states of $\overline{WE}$, $\overline{CEL}$ or $\overline{CES}$.

The switching time waveforms in *Figures 2, 3 and 4* define the read, write, and output enable/disable parameters respectively.

Reduced-Voltage Operation

These memories will retain data with reduced V_{CC} and hence are useful for battery-backup data storage. Certain precautions must be observed as V_{CC} is reduced: (1) input voltages must remain between the V_{CC} and ground of the RAM or supply latch-up can occur, (2) WRITE mode must be avoided, (3) during power-up of V_{CC}, $\overline{ST}$ logic state must be maintained (either GND or V_{CC}) while address control lines stabilize.

Logic Diagram *

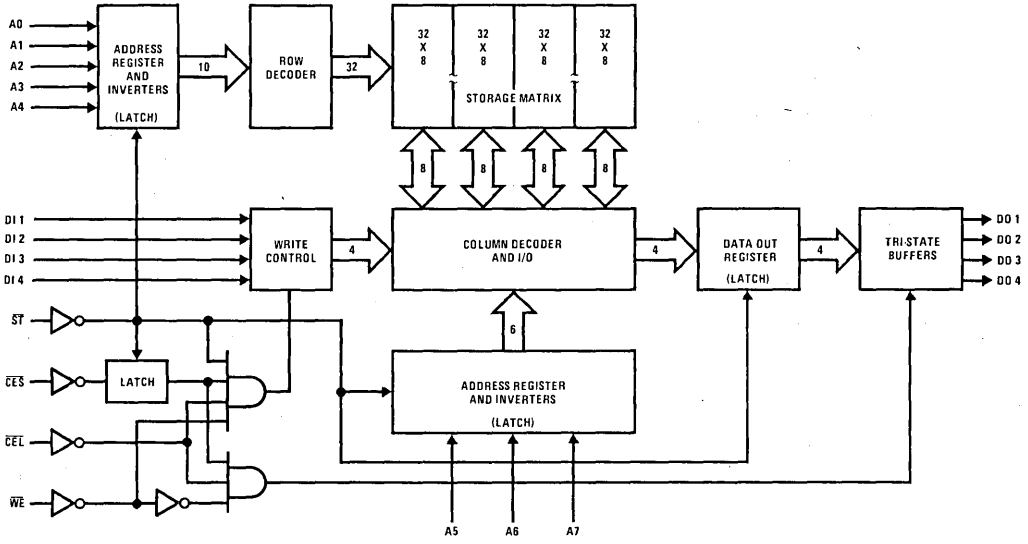


FIGURE 1. MM54C920/MM74C920

* The logic diagram for the MM54C921/MM74C921 is identical to this except that data inputs (DI1–DI4) are connected to data outputs (DO1–DO4).

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
MM54C920, MM54C921	4.5	5.5	V
MM74C920, MM74C921	4.5	5.5	V
MM74C920-3, MM74C921-3	4.75	5.25	V
Ambient Temperature (T_A)			
MM54C920, MM54C921	−55	+125	°C
MM74C920, MM74C921	−40	+85	°C
MM74C920-3, MM74C921-3	0	+70	°C

DC Electrical Characteristics (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MM54C920 MM54C921		MM74C920 MM74C921		MM74C920–3 MM74C921–3		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	Logical "1" Input Voltage		V_{CC}−2.0	V_{CC}	V_{CC}−2.0	V_{CC}	V_{CC}−1.5	V_{CC}	V
V_{IL}	Logical "0" Input Voltage		0	0.8	0	0.8	0	0.8	V
V_{OH1}	Logical "1" Output Voltage	I_{OH} = −1 mA	2.4		2.4		2.4		V
V_{OH2}	Logical "1" Output Voltage	I_{OUT} = 0	V_{CC}−0.1		V_{CC}−0.1		V_{CC}−0.1		V
V_{OL1}	Logical "0" Output Voltage	I_{OL} = 2 mA		0.4		0.4		0.4	V
V_{OL2}	Logical "0" Output Voltage	I_{OUT} = 0		0.01		0.01		0.01	V
I_{IL}	Input Leakage	$0V \leq V_{IN} \leq V_{CC}$	−1.0	1.0	−1.0	1.0	−1.0	1.0	μA
I_O	Output Leakage	$0V \leq V_O \leq V_{CC}$, $\overline{CEL} = V_{CC}$	−1.0	1.0	−1.0	1.0	−1.0	1.0	μA
I_{CC}	Supply Leakage Current	$V_{IN} = V_{CC}$, $\overline{ST}$ = 0V, V_O = 0V		20		10		100	μA
V_{DR}	V_{CC} for Data Retention	(Note 3)	2.0		2.0		2.0		V
I_{DR}	I_{CC} for Data Retention	$\overline{CEL} = V_{CC}$ = 2V, Typical at 25°C		0.01(typ)		0.01(typ)		0.01(typ)	μA

Capacitance (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		4	7	pF
C_O	Output Capacitance	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		6	9	pF
$C_{I/O}$	Data Input/Output Capacitance	MM54C921/MM74C921 Only		8	12	pF

Note 1: "Absolute Maximum Ratings" are those values above which the device may be permanently damaged. They do not mean the device may be operated at these values.

Note 2: These limits apply over the entire operating range specified in the "Operating Conditions" unless otherwise stated.

Note 3: $\overline{CEL} = V_{CC} - 2V$ or = 2V, whichever is greater.

Note 4: Capacitance is guaranteed by periodic testing.

Truth Table

$\overline{ST}$	$\overline{CES}$*	$\overline{CEL}$	$\overline{WE}$	DI*	FUNCTION
X	X	1	X	X	Output in Hi-Z state
0	1	X	X	X	Output in Hi-Z state
X	X	X	0	X	Output in Hi-Z state
0	0	0	0	0	Write "0", output in Hi-Z state
0	0	0	0	1	Write "1", output in Hi-Z state
0	0	0	1	X	Read data, output enabled

*Set-up and hold times must be met
X = don't care

AC Electrical Characteristics (Note 5)

SYMBOL	PARAMETER	MM54C920 MM54C921		MM74C920 MM74C921		MM74C920–3 MM74C921–3		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_C	Cycle Time	290		255		330		ns
t_{ACC}	Access Time From Address		275		250		325	ns
t_{ACS}	Access Time From Strobe		250		225		300	ns
t_{AS}	Address Set-Up Time	25		25		25		ns
t_{AH}	Address Hold Time	25		25		25		ns
t_{OE}	Output Enable Time		150		130		130	ns
t_{OD}	Output Disable Time		150		130		130	ns
$t_{\overline{ST}}$	$\overline{ST}$ Pulse Width (Negative)	150		130		165		ns
t_{ST}	ST Pulse Width (Positive)	140		125		165		ns
t_{WP}	Write Pulse Width (Negative)	150		130		165		ns
t_{DS}	Data Set-Up Time	100		90		90		ns
t_{DH}	Data Hold Time	60		60		60		ns

Note 5: These limits apply over the operating range specified in the "Operating Conditions" with $t_{RISE} = t_{FALL} = 5$ ns, load = 1 TTL gate + 50 pF.

Switching Time Waveforms

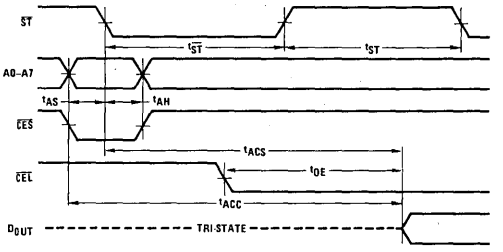
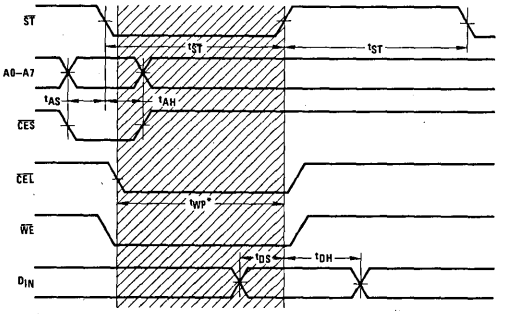
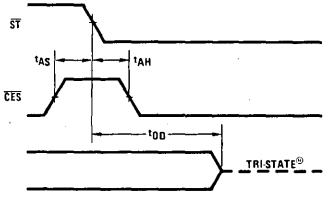


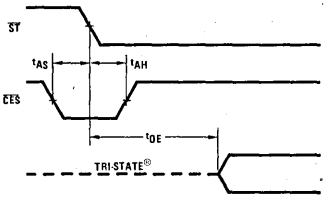
FIGURE 2. Read Cycle ($\overline{WE}$ = V_{IH})



*t_{WP} (the Write Pulse Width) is the time $\overline{ST}$, $\overline{CEL}$ and $\overline{WE}$ are coincidentally low

FIGURE 3. Write Cycle





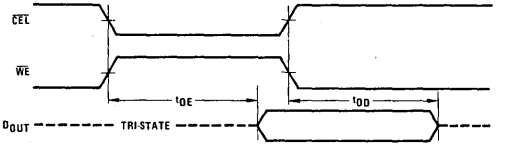
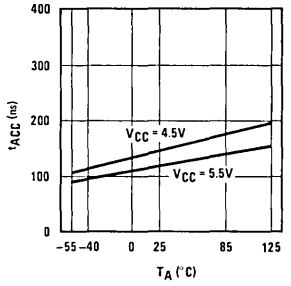


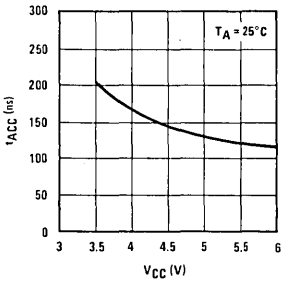
FIGURE 4. Output Enable/Disable

Typical Performance Characteristics

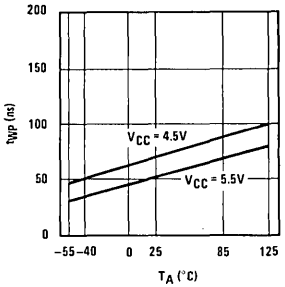
Access Time vs Ambient Temperature



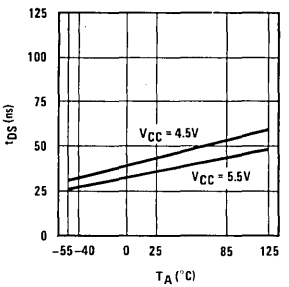
Access Time vs Power Supply Voltage



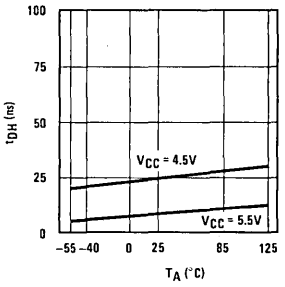
Minimum Write Pulse Width vs Ambient Temperature



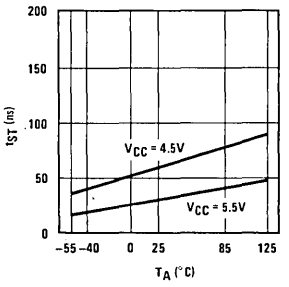
Data-In Setup Time vs Ambient Temperature



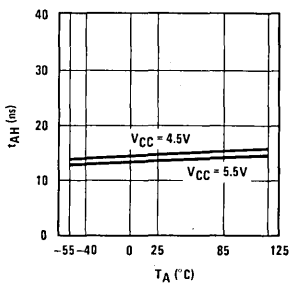
Data In Hold Time vs Ambient Temperature



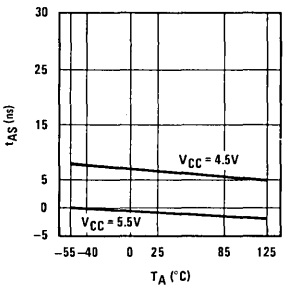
Minimum ST Pulse Width (Positive) vs Ambient Temperature



Address Hold Time vs Ambient Temperature

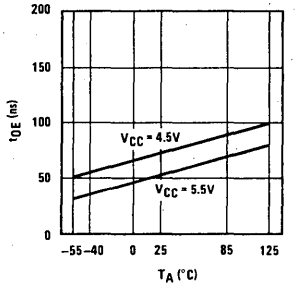


Address Setup Time vs Ambient Temperature

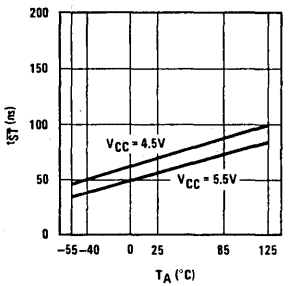


Typical Performance Characteristics (Continued)

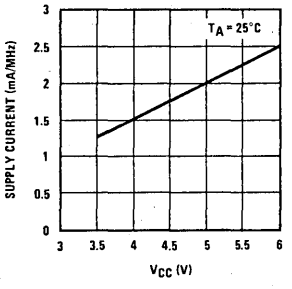
Output Enable Time vs Ambient Temperature



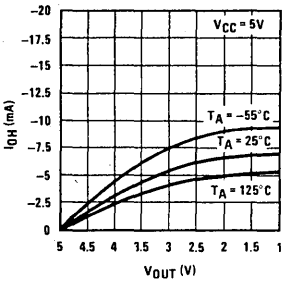
Minimum $\overline{ST}$ Pulse Width (Negative) vs Ambient Temperature



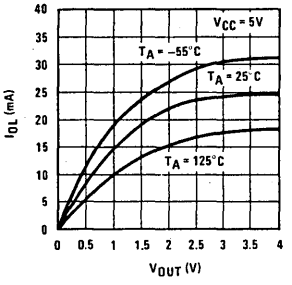
Dynamic Current vs Power Supply Voltage ($V_{IH} = V_{CC}$, $V_{IL} = 0V$)



Output Source Current vs Output Voltage



Output Sink Current vs Output Voltage



National Semiconductor

CMOS RAMs

MM54C929/MM74C929, MM54C930/MM74C930 1024-Bit (1024 x 1) Static RAMs

General Description

The MM54C929/MM74C929 and the MM54C930/MM74C930 1024 x 1 random access read/write memories are manufactured using silicon-gate CMOS technology. These RAMs are specifically designed to operate from standard 54/74 TTL power supplies; all inputs and outputs are TTL compatible. Data output is the same polarity as data input. Internal latches store the address inputs and data output. Chip select input $\overline{CS1}$ serves as a chip strobe, controlling address and data latching. The Data-In and Data-Out terminals can be tied together for common I/O applications. Complete address decoding, 3-chip select functions (MM54C930/MM74C930) and TRI-STATE® output allow easy memory expansion and organization. The MM54C929/MM74C929 differs from the MM54C930/MM74C930 only in that $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$ are internally connected together, providing a single chip-select input $\overline{CS}$.

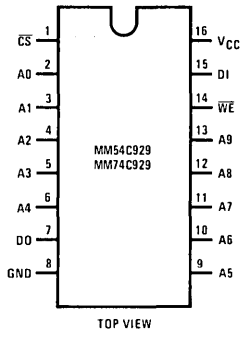
Versatility, high speed, and low power make these RAMs ideal elements for use in many microprocessor, minicomputer and main-frame-memory applications.

Features

- Fast access—250 ns max
- TRI-STATE outputs
- Low power—10 μA max standby
- On-chip registers
- Single 5V supply
- Inputs and output TTL compatible
- Data retained with V_{CC} as low as 2V
- Can be operated common I/O

Connection Diagrams

Dual-In-Line Package

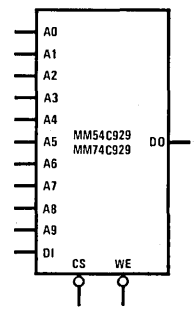


TOP VIEW

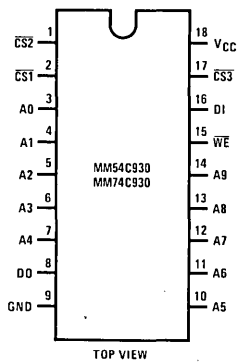
Order Number MM54C929J, MM74C929J or MM74C929J-3
See NS Package J16A

Order Number MM74C929N or MM74C929N-3
See NS Package N16A

Logic Symbols



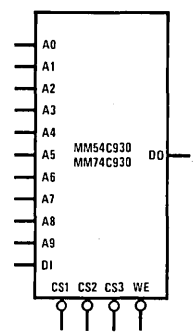
Dual-In-Line Package



TOP VIEW

Order Number MM54C930J, MM74C930J or MM74C930J-3
See NS Package J18A

Order Number MM74C930N or MM74C930N-3
See NS Package N18A



2

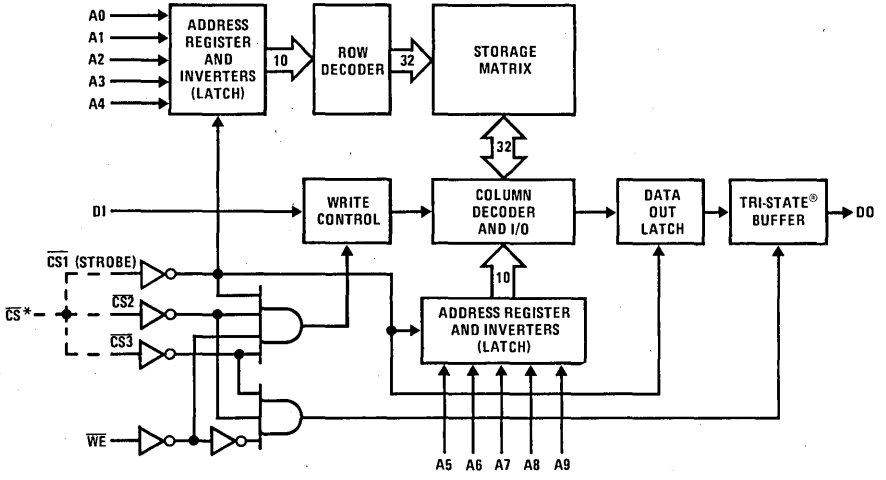
Functional Description

Address inputs are clocked into the input latches by the falling edge of chip strobe $\overline{CS1}$; set-up and hold times must be observed on these input signals (see timing diagram). The true and complement address information is fed to the row and column decoders which select one of the 1024-bit locations. The addressed bit is fed, via a sense amplifier, to the output register and TRI-STATE buffer. The information is latched into the output register on the rising edge of chip strobe $\overline{CS1}$. The output is in a high impedance state when the chip is not selected ($\overline{CS2}$ or $\overline{CS3}$ high) or when writing ($\overline{WE}$ low). Output buffer control is independent of chip strobe $\overline{CS1}$.

Reduced-Voltage Operation

These memories will retain data with reduced V_{CC} and hence are useful for battery-backup data storage. Certain precautions must be observed as V_{CC} is reduced: (1) input voltages must remain between the V_{CC} and ground of the RAM or supply latch-up can occur, (2) WRITE mode must be avoided, (3) during power-up of V_{CC}, strobe ($\overline{CS}$ for the MM74C929 and $\overline{CS1}$ for the MM74C930) logic state must be maintained (either GND or V_{CC}) while address control lines stabilize.

Logic Diagram *



*The MM74C930 has 3 chip selects $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$. The MM74C929 has these internally connected together providing a single chip select input $\overline{CS}$.

FIGURE 1

Absolute Maximum Ratings

Supply Voltage, V_{CC}	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering 10 seconds)	300°C

Operating Conditions

Operating Temperature Range	
MM54C929, MM54C930	−55°C to +125°C
MM74C929, MM74C930	−40°C to +85°C
MM74C929-3, MM74C930-3	0°C to +70°C

DC Electrical Characteristics V_{CC} = 5V ±10%, T_A = Operating Range, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MM54C929, MM54C930		MM74C929, MM74C930		MM74C929-3, MM74C930-3 (NOTE 1)		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	Logical "1" Input Voltage		V_{CC}−2.0	V_{CC}	V_{CC}−2.0	V_{CC}	V_{CC}−2.0	V_{CC}	V
V_{IL}	Logical "0" Input Voltage		0	0.8	0	0.8	0	0.8	V
V_{OH1}	Logical "1" Output Voltage	I_{OH} = 1 mA	2.4		2.4		2.4		V
V_{OH2}	Logical "1" Output Voltage	I_{OUT} = 0	V_{CC}−0.1		V_{CC}−0.1		V_{CC}−0.1		V
V_{OL1}	Logical "0" Output Voltage	I_{OL} = 2.0 mA		0.4		0.4		0.4	V
V_{OL2}	Logical "0" Output Voltage	I_{OUT} = 0		0.01		0.01		0.01	V
I_{IL}	Input Leakage	$0V \leq V_{IN} \leq V_{CC}$	−1.0	1.0	−1.0	1.0	−1.0	1.0	μA
I_O	Output Leakage	$0V \leq V_O \leq V_{CC}$, (Note 2)	−1.0	1.0	−1.0	1.0	−1.0	1.0	μA
I_{CC}	Supply Leakage Current	$V_{IN} = V_{CC}$, V_O = 0V		20		10		100	μA
V_{DR}	V_{CC} for Data Retention	(Note 3)	2.0		2.0		2.0		V
I_{DR}	I_{CC} for Data Retention	V_{CC} = 2V, T_A = 25°C, (Note 2)		0.01 (typ)		0.01 (typ)		0.1 (typ)	μA

Note 1: V_{CC} = 5V ±5%.
Note 2: $\overline{CS2}$ = $\overline{CS3}$ = V_{CC} or $\overline{CS}$ = V_{CC}.
Note 3: $\overline{CS2}$ or $\overline{CS3}$ or $\overline{CS}$ = V_{CC} − 2V or = 2V, whichever is greater.

AC Electrical Characteristics V_{CC} = 5V ±10%, T_A = Operating Range, unless otherwise noted

TTL Interface (V_{IH} = V_{CC} − 2V, V_{IL} = 0.8V, Input t_{RISE} = t_{FALL} = 5 ns, Load = 1 TTL Gate + 50 pF)

SYMBOL	PARAMETER	MM54C929, MM54C930		MM74C929, MM74C930		MM74C929-3, MM74C930-3 (NOTE 1)		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_C	Cycle Time	290		255		330		ns
t_{ACC}	Access Time From Address		265		240		315	ns
t_{ACS},t_{ACS1}	Access Time From $\overline{CS}$, $\overline{CS1}$		250		225		300	ns
t_{AS}	Address Set-Up Time	15		15		15		ns
t_{AH}	Address Hold Time	50		50		50		ns
t_{OE}	Output Enable Time		150		130		130	ns
t_{OD}	Output Disable Time		150		130		130	ns
$t_{\overline{CS}}$,$t_{\overline{CS1}}$ (Note 4)	$\overline{CS}$, $\overline{CS1}$ Pulse Width (Negative)	150		130		165		ns
t_{CS},t_{CS1}	$\overline{CS}$, $\overline{CS1}$ Pulse Width (Positive)	140		125		165		ns
t_{WP}	Write Pulse Width (Negative)	150		130		165		ns
t_{DS}	Data Set-Up Time, (Note 5)	150		140		140		ns
t_{DH}	Data Hold Time, (Note 5)	0		0		0		ns

Note 4: Greater than minimum $\overline{CS}$ pulse width must be used when reading data from the MM54C929/MM74C929 to ensure that output TRI-STATING does not occur before data becomes valid. Writing has no such limitation.

Note 5: t_{DS} and t_{DH} are referenced to the low-to-high transition of $\overline{CS1}$ or $\overline{CS2}$ or $\overline{CS3}$ or $\overline{WE}$,whichever switches first, for the MM54C930/MM74C930 and are referenced to the $\overline{CS}$ or $\overline{WE}$ low-to-high transition, whichever switches first, for the MM54C929/MM74C929.

Capacitance (Note 6)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0, f = 1 MHz, T_A = 25°C	4	7	pF
C_O	Output Capacitance	V_{IN} = 0, f = 1 MHz, T_A = 25°C	6	9	pF
$C_{\overline{CS}}$	Chip Select Capacitance	MM54C929/MM74C929, MM74C929-3	8	12	pF

Note 6: Capacitance maximum is guaranteed by periodic testing.

Truth Tables

MM54C929/MM74C929

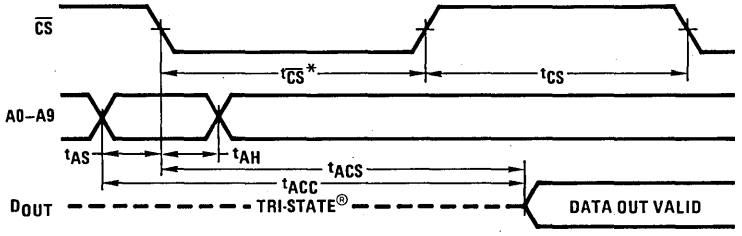
$\overline{CS}$	$\overline{WE}$	DI	FUNCTION
1	X	X	Output in Hi-Z State
X	0	X	Output in Hi-Z State
0	0	0	Write "0," Output in Hi-Z State
0	0	1	Write "1," Output in Hi-Z State
0	1	X	Read Data, Output Enabled

X = Don't care

MM54C930/MM74C930

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{WE}$	DI	FUNCTION
X	1	X	X	X	Output in Hi-Z State
X	X	1	X	X	Output in Hi-Z State
X	X	X	0	X	Output in Hi-Z State
0	0	0	0	0	Write "0," Output in Hi-Z State
0	0	0	0	1	Write "1," Output in Hi-Z State
0	0	0	1	X	Read Data, Output Enabled

Switching Time Waveforms



*Greater than minimum $\overline{CS}$ pulse width must be used when reading data from the MM54C929/MM74C929 to ensure that output TRI-STATING does not occur before data becomes valid. Writing has no such limitation, *(Figure 4a)*.

FIGURE 2a. MM54C929/MM74C929 Read Cycle

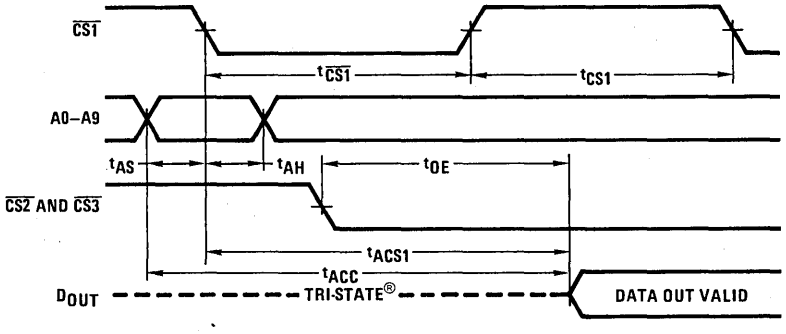
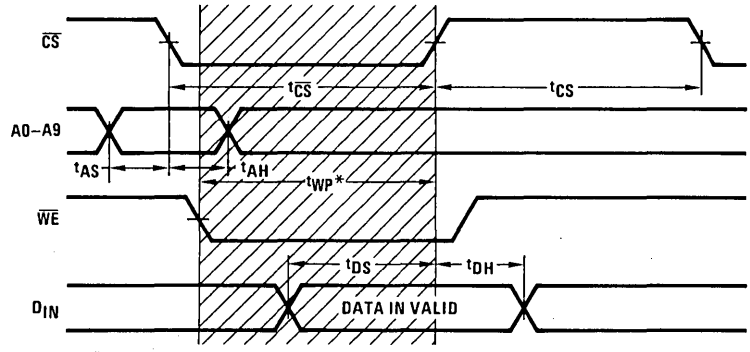


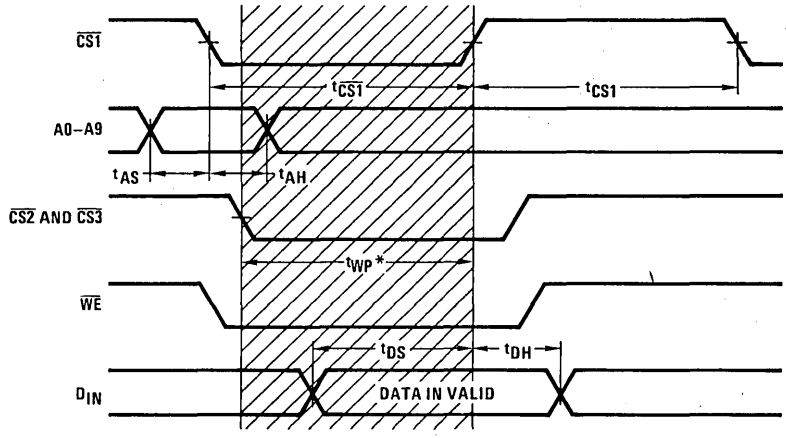
FIGURE 2b. MM54C930/MM74C930 Read Cycle

Switching Time Waveforms (Continued)



*t_{WP} (the Write Pulse width) is the time $\overline{CS}$ and $\overline{WE}$ are coincidentally low

FIGURE 3a. MM54C929/MM74C929 Write Cycle



*t_{WP} (the Write Pulse width) is the time $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$ and $\overline{WE}$ are coincidentally low

FIGURE 3b. MM54C930/MM74C930 Write Cycle

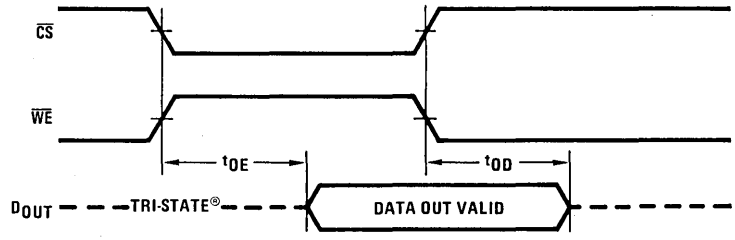


FIGURE 4a. MM54C929/MM74C929

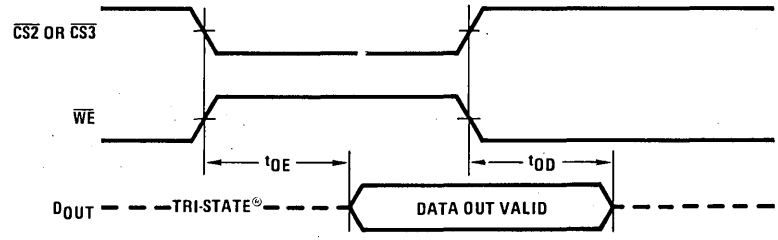
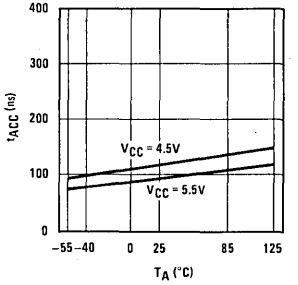


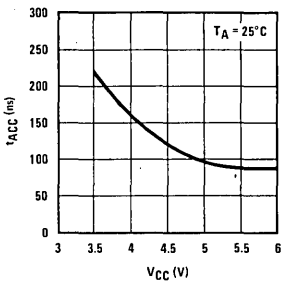
FIGURE 4b. MM54C930/MM74C930

Typical Performance Characteristics

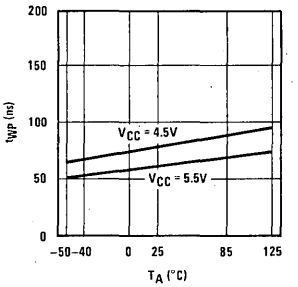
Access Time vs Ambient Temperature



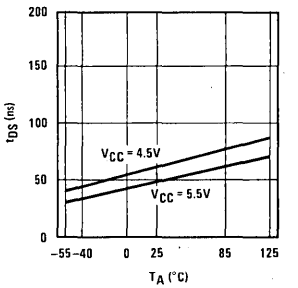
Access Time vs Power Supply Voltage



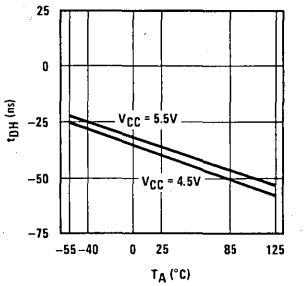
Minimum Write Pulse Width vs Ambient Temperature



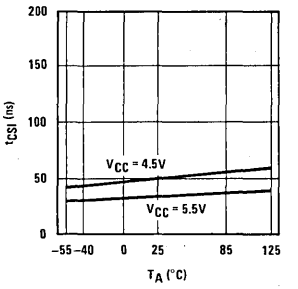
Data-In Set-Up Time vs Ambient Temperature



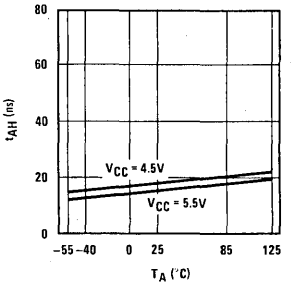
Data-In Hold Time vs Ambient Temperature



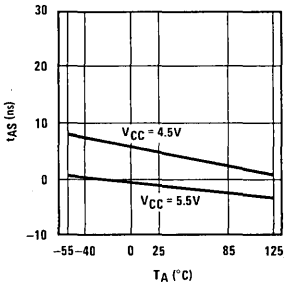
Minimum $\overline{CSI}$ Pulse Width (Positive) vs Ambient Temperature



Address Hold Time vs Ambient Temperature

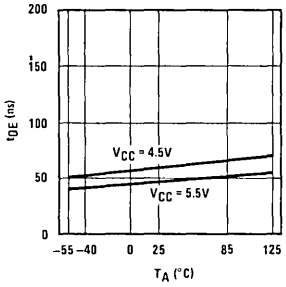


Address Set-Up Time vs Ambient Temperature

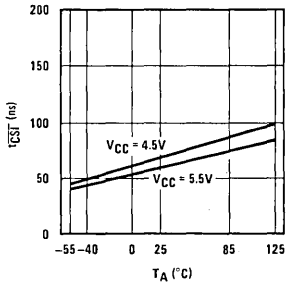


Typical Performance Characteristics (Continued)

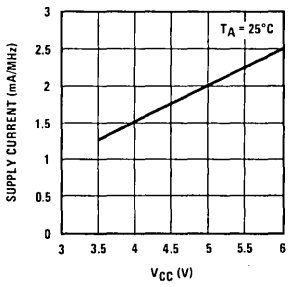
Output Enable Time vs Ambient Temperature



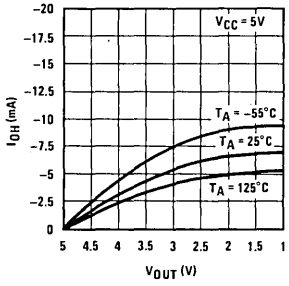
Minimum $\overline{CS1}$ Pulse Width (Negative) vs Ambient Temperature



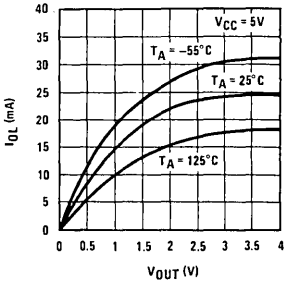
Dynamic Current vs Power Supply Voltage ($V_{IH} = V_{CC}$, V_{IL} = 0V)



Output Source Current vs Output Voltage



Output Sink Current vs Output Voltage



National Semiconductor

CMOS RAMs

MM54C989/MM74C989 64-Bit (16 x 4) TRI-STATE® RAM

General Description

The MM54C989/MM74C989 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of 4 address lines, 4 data input lines, a write enable line and a memory enable line. The 4 binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register latches the address information on the positive to negative transition of the memory enable input. The 4 TRI-STATE data output lines working in conjunction with the memory enable input provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note. The timing is different than the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

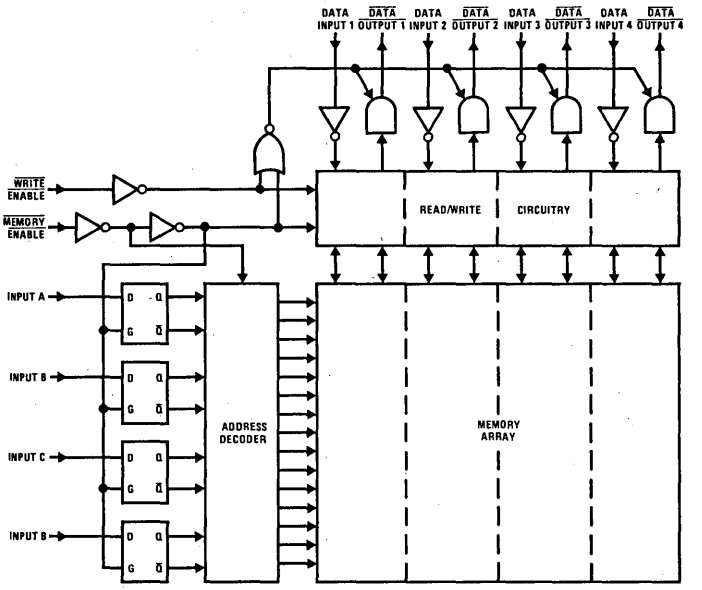
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the 4 outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

When the device is writing or disabled the output assumes a TRI-STATE (Hi-Z) condition.

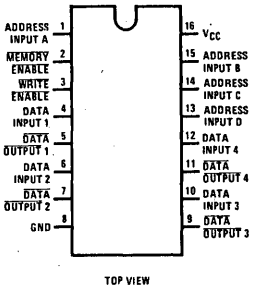
Features

- Wide supply voltage range — 3.0V to 5.5V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- Low power TTL compatibility — fan out of 2 driving 74L
- Input address register
- Low power consumption — 250 nW/package typ @ V_{CC} = 5V
- Fast access time — 140 ns typ at V_{CC} = 5V
- TRI-STATE output

Logic and Connection Diagrams



Dual-in-Line Package



TOP VIEW

Order Number MM54C989J or MM74C989J
See NS Package J16A

Order Number MM74C989N
See NS Package N16A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Package Dissipation	500 mW
Absolute Maximum V_{CC}	7.0V
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
MM54C989	4.7	5.5	V
MM74C989	4.75	5.25	V
Temperature (T_A)			
MM54C989	−55	+125	°C
MM74C989	−40	+85	°C
Operating V_{CC} Range			3.0V to 5.5V
Standby V_{CC} Range			1.5V to 5.5V

DC Electrical Characteristics MM54C989/MM74C989

(Min/max limits apply across the temperature and power supply range indicated).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 5V		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0	−1	−0.005		μA
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −360 μA	2.4			V
		I_O = −150 μA	V_{CC}−0.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 360 μA			0.4	V
	Output Current in High Impedance State	V_O = 5V		0.005	1	μA
		V_O = 0	−1	−0.005		μA
I_{CC}	Supply Current (Active)	$\overline{ME}$ = 0, V_{CC} = 5V		0.05	150	μA
	Supply Current (Stand-By)	$\overline{ME}$ = 5V			3	μA

AC Electrical Characteristics MM54C989/MM74C989

T_A = 25°C, V_{CC} = 5V, C_L = 50 pF

PARAMETER		MIN	TYP	MAX	UNITS
t_{ACC}	Access Time From Address		140	500	ns
t_{PD}	Propagation Delay From $\overline{ME}$		110	360	ns
t_{SA}	Address Input Set-Up Time	140	30		ns
t_{HA}	Address Input Hold Time	20	15		ns
t_{ME}	Memory Enable Pulse Width	200	80		ns
$t_{\overline{ME}}$	Memory Enable Pulse Width	400	100		ns
t_{SD}	Data Input Set-Up Time	0			ns
t_{HD}	Data Input Hold Time	30	20		ns
$t_{\overline{WE}}$	Write Enable Pulse Width	140	70		ns
t_{1H}, t_{0H}	Delay to TRI-STATE, C_L = 5 pF, R_L = 10k, (Note 4)		100	200	ns
CAPACITANCE					
C_{IN}	Input Capacity, Any Input, (Note 2)		5		pF
C_{OUT}	Output Capacity, Any Output, (Note 2)		8		pF
C_{PD}	Power Dissipation Capacity, (Note 3)		350		pF

AC Electrical Characteristics (Continued)

MM54C989: $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$. $C_L = 50$ pF
MM74C989: $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.75V$ to $5.25V$. $C_L = 50$ pF

PARAMETER		MM54C989		MM74C989		UNITS
		MIN	MAX	MIN	MAX	
t_{ACC}	Access Time From Address		500		620	ns
t_{PD1}, t_{PD0}	Propagation Delay From $\overline{ME}$		350		430	ns
t_{SA}	Address Input Set-Up Time	150		140		ns
t_{HA}	Address Input Hold Time	50		60		ns
t_{ME}	$\overline{\text{Memory Enable}}$ Pulse Width	250		310		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	520		400		ns
t_{SD}	Data Input Set-Up Time	0		0		ns
t_{HD}	Data Input Hold Time	60		50		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	220		180		ns
t_{1H}, t_{0H}	Delay to TRI-STATE, (Note 4)		200		200	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

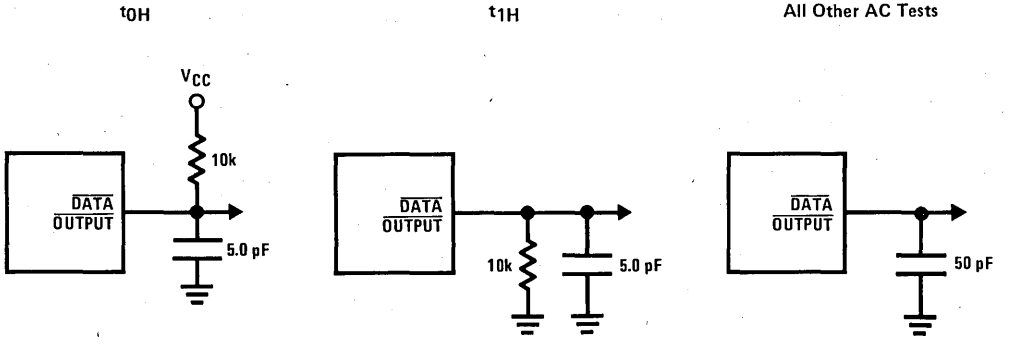
Note 3: C_{PD} determines the no load AC power consumption for any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Note 4: See AC test circuit for t_{1H}, t_{0H}.

Truth Table

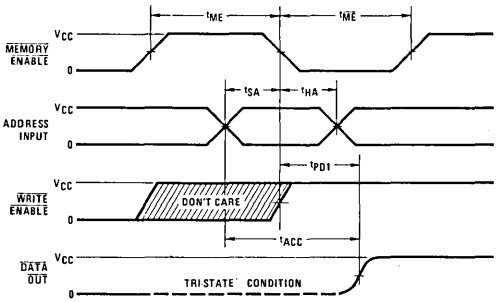
$\overline{ME}$	$\overline{WE}$	OPERATION	CONDITION OF OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	TRI-STATE
H	H	Inhibit, Storage	TRI-STATE

AC Test Circuits

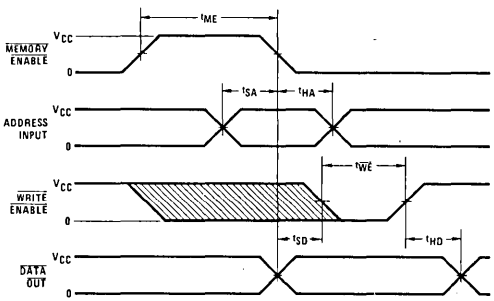


Switching Time Waveforms

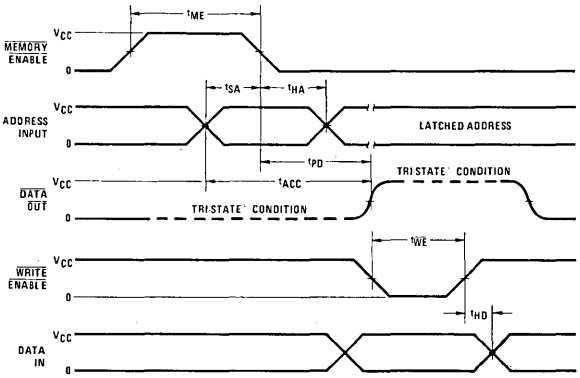
Read Cycle (Note 1)



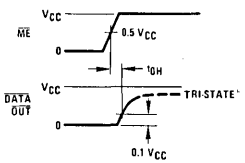
Write Cycle (Note 1)



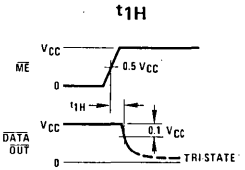
Read-Modify-Write Cycle (Note 1)



t_{0H}



t_{1H}



Note 1: $\overline{\text{MEMORY ENABLE}}$ must be brought high for t_{ME} ns between every address change.

Note 2: $t_r = t_f = 20$ ns for all inputs.

National Semiconductor

CMOS RAMs
PRELIMINARY

NMC6504 4096-Bit (4096 x 1) Static RAM

General Description

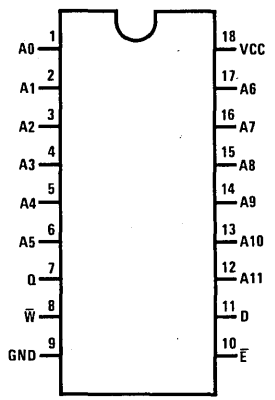
The NMC6504 is a static CMOS random access read/write memory organized as 4096 words of 1 bit each. This device is fabricated with National Semiconductor's silicon-gate CMOS technology and is fully compatible to the TTL environment. Synchronous operation is provided by on-chip address, data, and write latches. The ENABLE input serves as the device strobe controlling the latching functions. The TRI-STATE® output, in conjunction with the ENABLE input, allows easy memory expansion.

Features

- Industry standard pinout
- Low data retention voltage — 2V
- Low speed/power product
- TTL compatible — all inputs and outputs
- TRI-STATE® outputs for bus operation
- High output drive
- High noise immunity
- Military temperature range available
- On-chip address registers (latches)
- Common I/O — high density packaging
- Output data latches
- Input data latches
- Select latch for microprocessor interface

Connection Diagram

Dual-In-Line Package

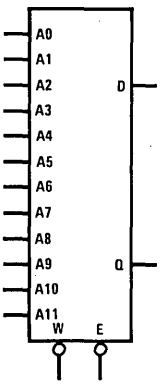


TOP VIEW

Order Number NMC6504J-2, NMC6504J-9 or NMC6504J-5
See NS Package J18A

Order Number NMC6504N-5
See NS Package N18A

Logic Symbol



Pin Names

A0–A11	Address Inputs
Ē	Chip Enable
W̄	Write Enable
D	Data Input
Q	Data Output

Functional Description

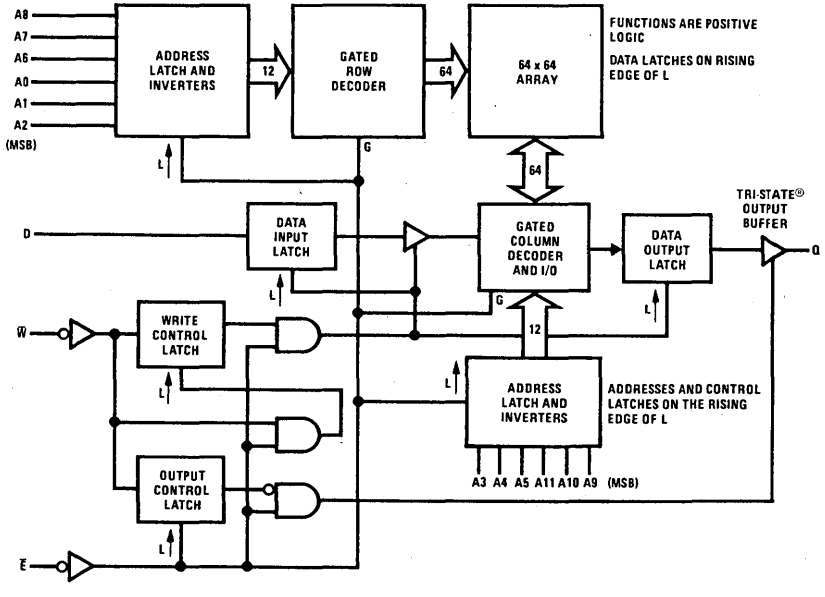
An NMC6504 memory cycle is initiated by the falling edge of the ENABLE ($\overline{E}$) input which latches the address information into the on-chip registers. On-chip latches allow selection of a read, early write, or read-modify-write cycle as a function of the ENABLE and WRITE ($\overline{W}$) input levels and timing. Data output is enabled by the falling edge of the ENABLE input and disabled by the rising edge except when performing an early write cycle. The input and output data latches are transparent except during the write pulse (not the WRITE input).

When performing a read cycle a minimum ENABLE LOW time is required to assure valid data at the output. This minimum LOW time is defined as the enable access time. A minimum ENABLE HIGH time is required to return the columns to the HIGH state and to precharge the sense amplifiers in preparation of the next cycle.

An early write cycle is performed by preceding the ENABLE with the HIGH to LOW transition of the WRITE input. The WRITE input level is latched, and set-up and hold times must be met. The data output is not enabled during an early write cycle. The input data set-up and hold times are referenced to the leading edge of the write pulse, which is initiated by the falling edge of the ENABLE input and terminated by the rising edge of the ENABLE.

A read-modify-write cycle is performed as a read cycle, for the enable access time, followed by the write pulse which is initiated by the falling edge of the WRITE input and terminated by the rising edge of either the ENABLE or WRITE input, whichever occurs first. The input data set-up and hold times are referenced to the falling edge of the WRITE input. Data is latched when the WRITE input goes LOW, allowing the modified data to be written into the memory while continuing to read the original data.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	7V
Voltage at Any Pin	−0.3V to VCC +0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Range

	Min	Max
Supply Voltage		
NMC6504-9	4.5V	5.5V
NMC6504-2	4.5V	5.5V
NMC6504-5	4.75V	5.25V
Temperature		
NMC6504-9	−40°C	85°C
NMC6504-2	−55°C	125°C
NMC6504-5	0°C	75°C

DC Electrical Characteristics over the operating range, unless otherwise noted

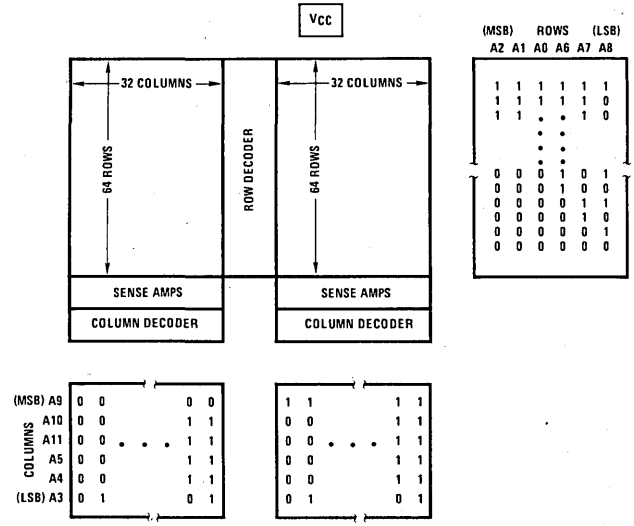
Symbol	Parameter	Conditions	NMC6504-9, NMC6504-2		NMC6504-5		Units
			Min	Max	Min	Max	
VCCDR	Data Retention Supply Voltage	VI = VCC, GND	2.0		2.0		V
ICCSB	Standby Supply Current			50		500	μA
ICCOP*	Operating Supply Current	f = 1 MHz, IO = 0, VI = VCC or GND		10		10	mA
ICCDR	Data Retention Supply Current	VCC = 3.0V, IO = 0, VI = VCC or GND		25		500	μA
II	Input Leakage Current	VI = VCC, GND	−1.0	+1.0	−10	+10	μA
VIL	Input Low Voltage		−0.3	0.8	−0.3	0.8	V
VIH	Input High Voltage		VCC − 2.0	VCC + 0.3	VCC − 2	VCC + 0.3	V
IOZ	Output Leakage Current	VI = VCC, GND	−1.0	+1.0	−10	+10	μA
VOL	Output Low Voltage	IOL = 2.0 mA		0.4		0.45	V
VOH	Output High Voltage	IOH = −1.0 mA	2.4		2.4		V
CI	Input Capacitance	f = 1 MHz		8		8	pF
CO	Output Capacitance	f = 1 MHz		10		10	pF

*ICCOP is proportional to operating frequency.

AC Test Conditions

Input Rise and Fall Times: ≤20 ns
All Timing Reference Levels: 1/2 VCC
Output Load: 1 TTL Load, 50 pF

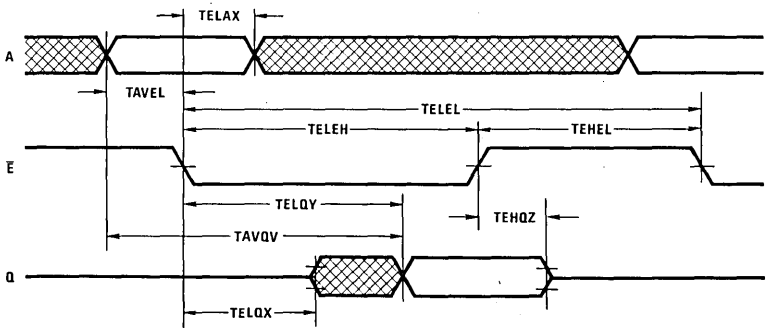
NMC6504 Bit Map and Address Decoding



Read Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6504-9, NMC6504-2		NMC6504-5		Units
		Min	Max	Min	Max	
TAVEL	Address Set-up Time	20		20		ns
TELAX	Address Hold Time	50		50		ns
TELQV	Enable Access Time		300		350	ns
TAVQV	Address Access Time		320		370	ns
TELEH	Enable ($\bar{E}$) Minimum Low Time	300		350		ns
TELEL	Read or Write Cycle Time	420		500		ns
TEHEL	Enable ($\bar{E}$) Minimum High Time	120		150		ns
TELQX	Output Enable from Enable ($\bar{E}$)		100		100	ns
TEHQZ	Output Disable from Enable ($\bar{E}$)		100		100	ns

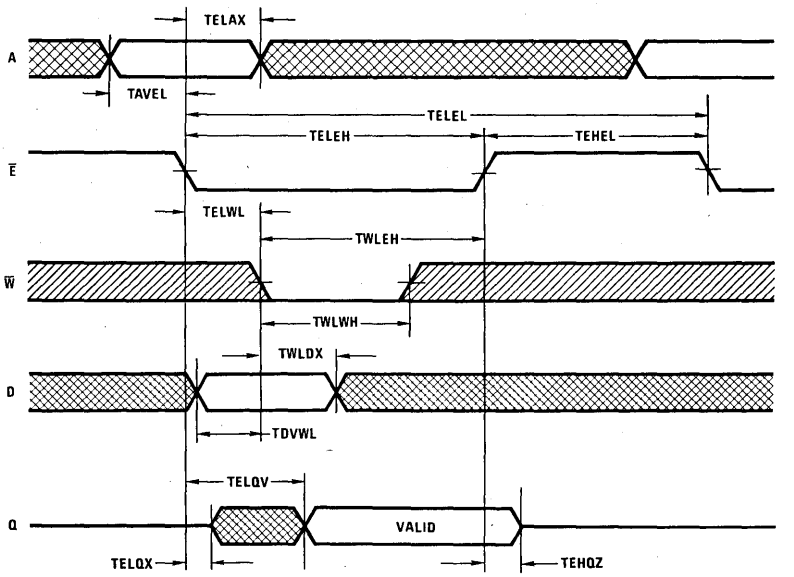
Read Cycle Waveforms



Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6504-9, NMC6504-2		NMC6504-5		Units
		Min	Max	Min	Max	
TAVEL	Address Set-up Time	20		20		ns
TELAX	Address Hold Time	50		50		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	80		100		ns
TELEL	Read or Write Cycle Time	420		500		ns
TELEH	Enable ($\overline{E}$) Minimum Low Time	300		350		ns
TDVWL	Data Set-up Time	0		30		ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	120		150		ns
TWLDX	Data Hold Time	80		100		ns
TELWH	Write Pulse Width ($\overline{E}$ and $\overline{W}$ Low)	80		100		ns
TELWL	Early Write Output Hi-Z Time	0		0		ns
TWLEH	Write Pulse Width ($\overline{W}$ and $\overline{E}$ Low)	200		250		ns
TELQX	Output Enable from $\overline{E}$		100		100	ns
TELQV	Enable Access Time		300		350	ns
TEHQZ	Output Disable from $\overline{E}$		100		100	ns

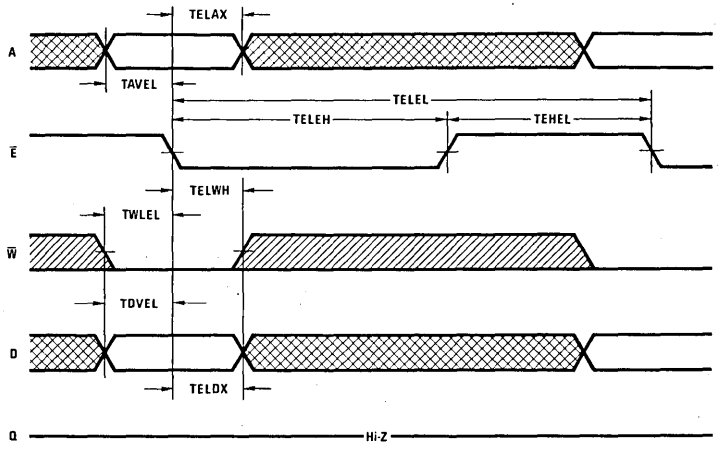
Write Cycle Waveforms



Early Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6504-9, NMC6504-2		NMC6504-5		Units
		Min	Max	Min	Max	
TAVEL	Address Set-up Time	20		20		ns
TELAX	Address Hold Time	50		50		ns
TELWH	Write Pulse Width ($\bar{E}$ and $\bar{W}$ Low)	80		100		ns
TDVEL	Early Write Data Set-up Time	0		30		ns
TELEH	Enable ($\bar{E}$) Minimum Low Time	300		350		ns
TWLEL	Early Write Set-up Time	0		0		ns
TEHEL	Enable ($\bar{E}$) Minimum High Time	120		150		ns
TELDX	Early Write Data Hold Time	80		100		ns
TELEL	Read or Write Cycle Time	420		500		ns

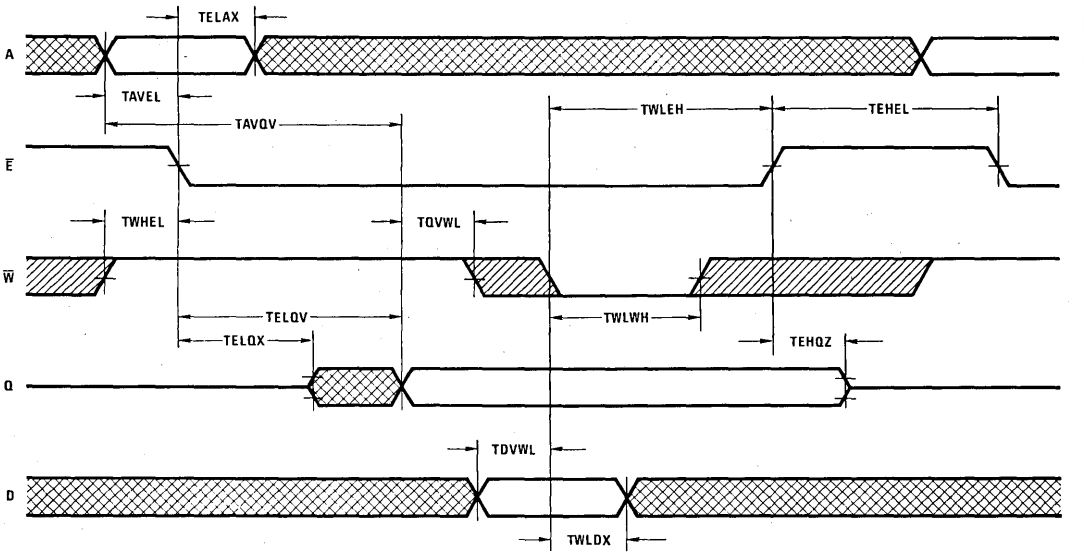
Early Write Cycle Waveforms



Read-Modify-Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6504-9, NMC6504-2		NMC6504-5		Units
		Min	Max	Min	Max	
TAVEL	Address Set-up Time	20		20		ns
TELAX	Address Hold Time	50		50		ns
TELQV	Enable Access Time		300		350	ns
TAVQV	Address Access Time		320		370	ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	120		150		ns
TWHEL	$\overline{W}$ Read Mode Set-up Time	0		0		ns
TWLEH	Write Pulse Width ($\overline{W}$ and $\overline{E}$ Low)	200		250		ns
TQVWL	Data Valid to Write Time	0		0		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	80		100		ns
TWLDX	Data Hold Time	80		100		ns
TELQX	Output Enable from Enable ($\overline{E}$)		100		100	ns
TEHQZ	Output Disable from Enable ($\overline{E}$)		100		100	ns
TDVWL	Data Set-up Time	0		30		ns

Read-Modify-Write Cycle Waveforms



National Semiconductor

CMOS RAMs

NMC6508 1024-Bit (1024 x 1) Static RAM

General Description

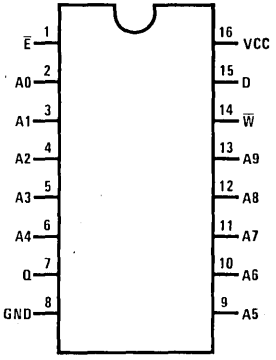
The NMC6508 is a static CMOS random access read/write memory organized as 1024 words of 1 bit each. This device is fabricated with National Semiconductor's silicon-gate CMOS technology and is fully compatible to the TTL environment. Synchronous operation is provided by the on-chip latches for the address inputs. The NMC6508 may be used in common I/O applications by externally connecting the data input and output terminals. The TRI-STATE® output, in conjunction with the ENABLE input, allows for easy memory expansion.

Features

- Industry standard pinout
- Low data retention voltage — 2V
- Low speed/power product
- TTL compatible — all inputs and outputs
- TRI-STATE® outputs for bus operation
- High output drive
- High noise immunity
- Military temperature range available
- On-chip address registers (latches)
- 16 pin — high density packaging
- Output data latches

Connection Diagram

Dual-In-Line Package

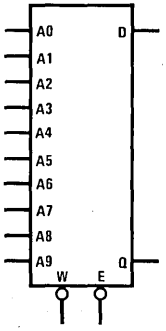


TOP VIEW

Order Number NMC6508J-2, NMC6508J-9 or NMC6508J-5
See NS Package J18A

Order Number NMC6508N-5
See NS Package N18A

Logic Symbol



Pin Names

A0-A9	Address Inputs
Ē	Chip Enable
W̄	Write Enable
D	Data Input
Q	Data Output

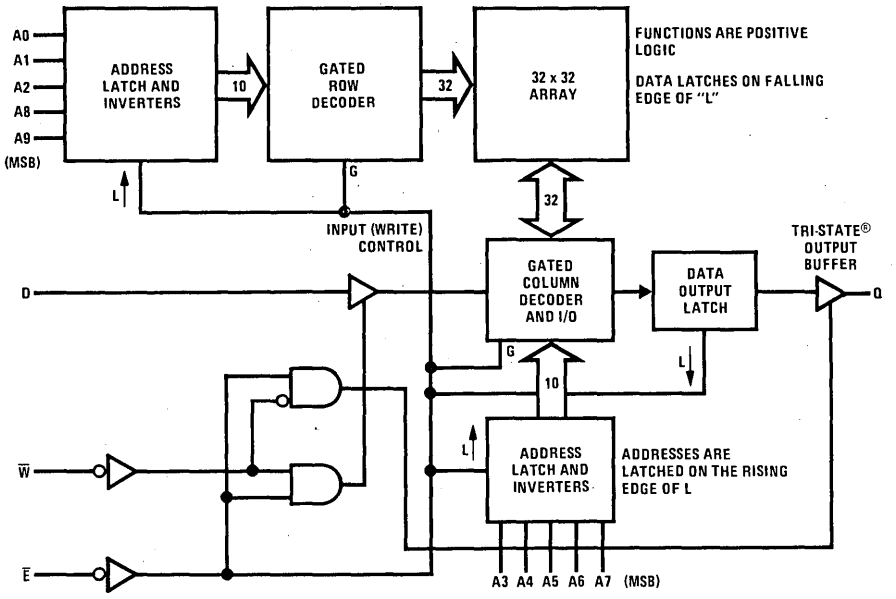
Functional Description

An NMC6508 memory cycle is initiated by the falling edge of the ENABLE ($\overline{E}$) input, which latches the address information into the on-chip registers. The output buffer is enabled when the WRITE ($\overline{W}$) input is HIGH and the ENABLE input is LOW.

When performing a read cycle a minimum ENABLE LOW time is required to assure valid data at the output. This minimum LOW time is defined as the device enable access time. A minimum ENABLE HIGH time is required to return the columns to the HIGH state and to precharge the sense amplifiers in preparation of the next memory cycle.

When performing a write cycle, the minimum ENABLE LOW time is required to enter new data. The write pulse is created by the coincident LOW of the ENABLE and WRITE inputs. The data set-up and hold times are referenced to the rising edge of either the ENABLE or WRITE input, whichever occurs first.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	7V
Voltage at Any Pin	−0.3V to VCC +0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Range

	Min	Max
Supply Voltage		
NMC6508B-9	4.5V	5.5V
NMC6508B-2	4.5V	5.5V
NMC6508-9	4.5V	5.5V
NMC6508-2	4.5V	5.5V
NMC6508-5	4.75V	5.25V
Temperature		
NMC6508B-9	−40°C	85°C
NMC6508B-2	−55°C	125°C
NMC6508-9	−40°C	85°C
NMC6508-2	−55°C	125°C
NMC6508-5	0°C	75°C

DC Electrical Characteristics over the operating range, unless otherwise noted

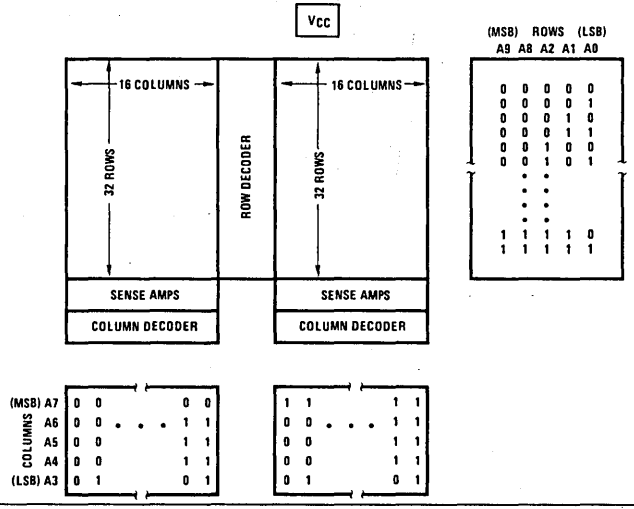
Symbol	Parameter	Conditions	NMC6508B-9, NMC6508B-2 NMC6508-9, NMC6508-2		NMC6508-5		Units
			Min	Max	Min	Max	
VCCDR	Data Retention Supply Voltage	VI = VCC, GND	2.0		2.0		V
ICCSB	Standby Supply Current			10		100	μA
ICCOP*	Operating Supply Current	f = 1 MHz, IO = 0, VI = VCC or GND		4		4	mA
ICCDR	Data Retention Supply Current	VCC = 3.0V, IO = 0, VI = VCC or GND		10		100	μA
II	Input Leakage Current	VI = VCC, GND	−1.0	+1.0	−1.0	+1.0	μA
VIL	Input Low Voltage		−0.3	0.8	−0.3	0.8	V
VIH	Input High Voltage		VCC − 2.0	VCC + 0.3	VCC − 2	VCC + 0.3	V
IOZ	Output Leakage Current	VI = VCC, GND	−1.0	+1.0	−1.0	+1.0	μA
VOL	Output Low Voltage	IOL = 3.2 mA		0.4		0.4	V
VOH	Output High Voltage	IOH = −0.4 mA	2.4		2.4		V
CI	Input Capacitance	f = 1 MHz		6		6	pF
CO	Output Capacitance	f = 1 MHz		10		10	pF

* ICCOP is proportional to operating frequency.

AC Test Conditions

Input Rise and Fall Times: ≤20 ns
All Timing Reference Levels: 1/2 VCC
Output Load: 1 TTL Load, 50 pF

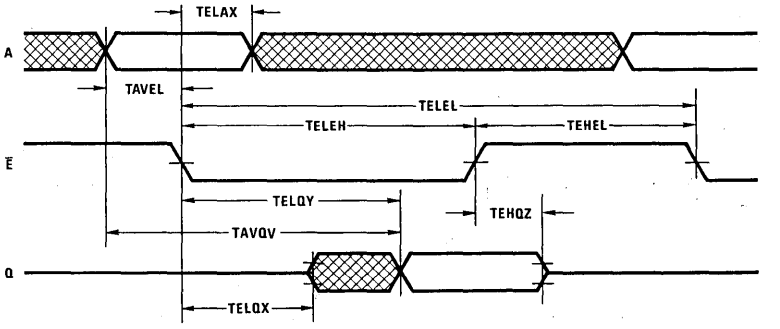
NMC6508 Bit Map and Address Decoding



Read Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6508B-9 NMC6508B-2		NMC6508-9 NMC6508-2		NMC6508-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TELQV	Enable Access Time		180		250		300	ns
TAVQV	Address Access Time		180		250		310	ns
TELEH	Enable ($\bar{E}$) Minimum Low Time	180		250		300		ns
TELQX	Output Enable from Enable ($\bar{E}$)		120		160		200	ns
TEHQZ	Output Disable from Enable ($\bar{E}$)		120		160		200	ns
TEHEL	Enable ($\bar{E}$) Minimum High Time	100		100		150		ns
TELEL	Read or Write Cycle Time	280		350		450		ns

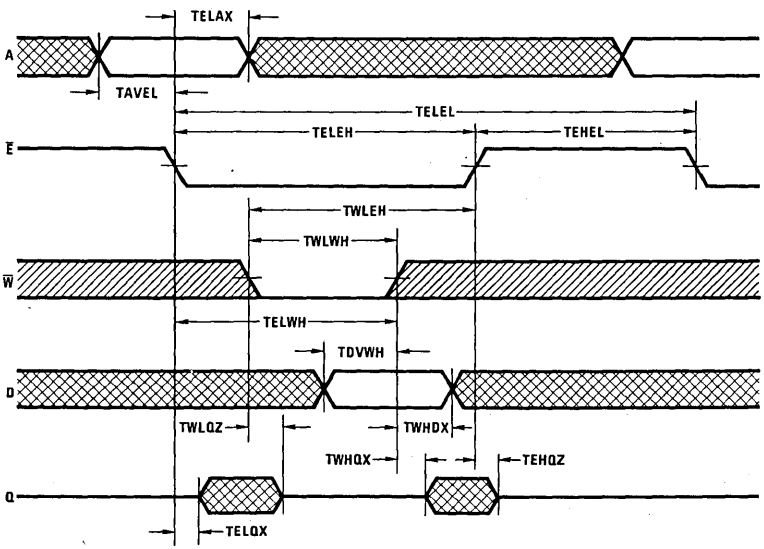
Read Cycle Waveforms



Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6508B-9 NMC6508B-2		NMC6508-9 NMC6508-2		NMC6508-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	100		100		150		ns
TDVWH	Data Set-up Time	80		110		130		ns
TELWH	Write Pulse Width ($\overline{E}$ and $\overline{W}$ Low)	100		130		160		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	100		130		160		ns
TELEL	Read or Write Cycle Time	280		350		450		ns
TWHDM	Data Hold Time	0		0		0		ns
TWLEH	Write Pulse Width ($\overline{E}$ and $\overline{W}$ Low)	100		130		160		ns
TELEH	Enable ($\overline{E}$) Minimum Low Time	180		250		300		ns
TELQX	Output Enable from $\overline{E}$		120		160		200	ns
TWLQZ	Output Disable from $\overline{W}$		120		160		200	ns
TWHQX	Output Enable from $\overline{W}$		120		160		200	ns
TEHQZ	Output Disable from $\overline{E}$		120		160		200	ns

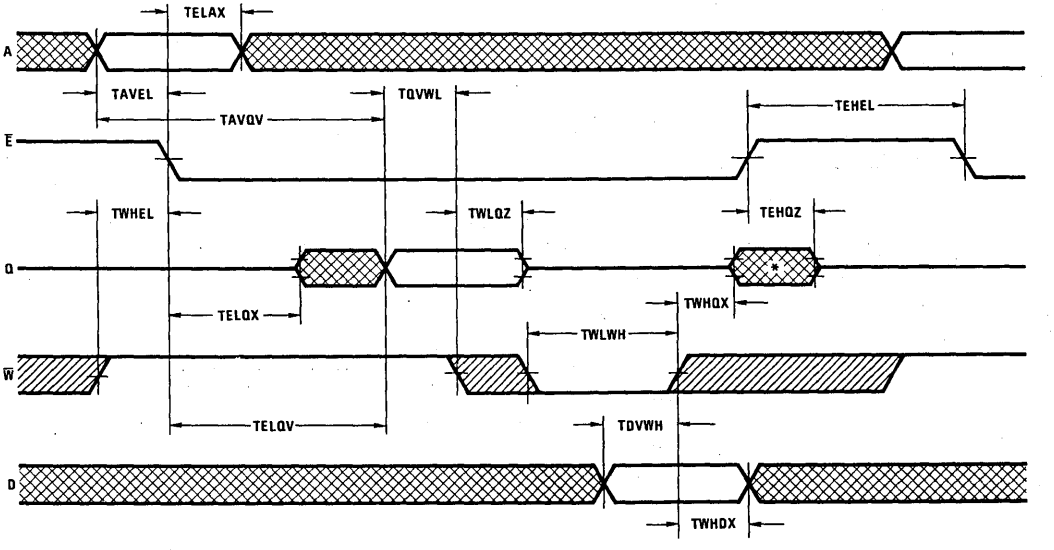
Write Cycle Waveforms



Read-Modify-Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6508B-9 NMC6508B-2		NMC6508-9 NMC6508-2		NMC6508-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TELQV	Enable Access Time		180		250		300	ns
TAVQV	Address Access Time		180		250		310	ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	100		100		150		ns
TWHDM	Data Hold Time	0		0		0		ns
TQVWL	Data Valid to Write Time	0		0		0		ns
TWHEL	$\overline{W}$ Read Mode Set-up Time	0		0		0		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	100		130		160		ns
TELQX	Output Enable from Enable ($\overline{E}$)		120		160		200	ns
TEHQZ	Output Disable from Enable ($\overline{E}$)		120		160		200	ns
TWLQZ	Output Disable from Write ($\overline{W}$)		120		160		200	ns
TDVWH	Data Set-up Time	80		110		130		ns
TWHQX	Output Enable from Write ($\overline{W}$)		120		160		200	ns

Read-Modify-Write Cycle Waveforms



* Output enable can be avoided by preceding the rising edge of $\overline{W}$ with the rising edge of $\overline{E}$ by time; TEHQZ

National Semiconductor

CMOS RAMs
PRELIMINARY

NMC6514 4096-Bit (1024 x 4) Static RAM

General Description

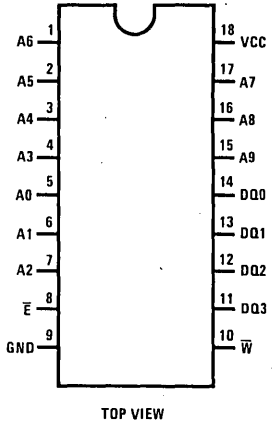
The NMC6514 is a static CMOS random access read/write memory organized as 1024 words of 4 bits each. This device is fabricated with National Semiconductor's silicon-gate CMOS technology and is fully compatible with the TTL environment. Synchronous operation is provided by on-chip address latches. The ENABLE input serves as the device strobe controlling the address latching function. The data I/O terminals, when not output data enabled, represent a high impedance for easy memory expansion.

Features

- Industry standard pinout
- Low data retention voltage — 2V
- Low speed/power product
- TTL compatible — all inputs and outputs
- TRI-STATE® outputs for bus operation
- High output drive
- High noise immunity
- Military temperature range available
- On-chip address registers (latches)
- Common I/O — high density packaging

Connection Diagram

Dual-In-Line Package



TOP VIEW

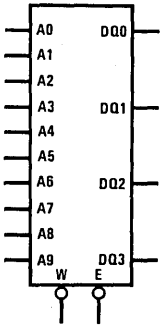
Order Number NMC6514J-2, NMC6514J-9 or NMC6514J-5
See NS Package J18A

Order Number NMC6514N-5
See NS Package N18A

Pin Names

A0-A9	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
DQ0-DQ3	Data In/Out

Logic Symbol



Functional Description

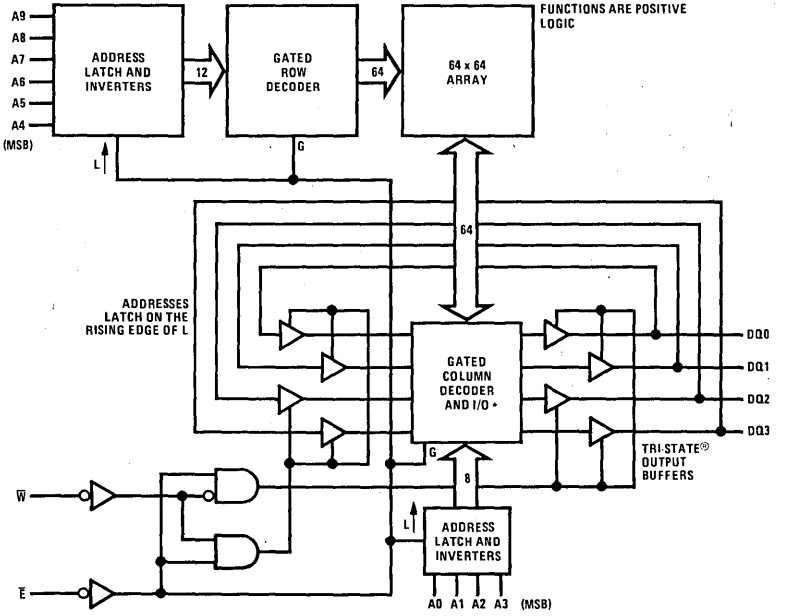
An NMC6514 memory cycle is initiated by the falling edge of the ENABLE ($\overline{E}$) input, which latches the address information into the on-chip registers. Read, write, the read-modify-write cycles are selected as a function of the ENABLE and WRITE ($\overline{W}$) input levels and timing. Data output is enabled by the falling edge of the ENABLE input and disabled by the rising edge when the WRITE input is HIGH. The output is disabled when writing.

When performing a read cycle a minimum ENABLE LOW time is required to assure valid data at the output. This minimum LOW time is defined as the device enable access time. A minimum ENABLE HIGH time is required to return the columns to the HIGH state and to precharge the sense amplifiers in preparation of the next cycle.

When performing a write cycle a minimum ENABLE LOW time is required to enter the new data. The write pulse is created by the coincident LOW of the ENABLE and WRITE inputs. The data set-up and hold time are referenced to the rising edge of either the ENABLE or WRITE inputs whichever occurs first.

A read-modify-write cycle is performed as a read cycle, for the enable access time, followed by the write pulse caused by the LOW time of the WRITE input. The output data is disabled by the falling edge of the WRITE input, and input data, meeting the set-up and hold requirements must be provided.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	7V
Voltage at Any Pin	−0.3V to VCC +0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Range

	Min	Max
Supply Voltage		
NMC6514-9	4.5V	5.5V
NMC6514-2	4.5V	5.5V
NMC6514-5	4.75V	5.25V
Temperature		
NMC6514-9	−40°C	85°C
NMC6514-2	−55°C	125°C
NMC6514-5	0°C	75°C

DC Electrical Characteristics over the operating range, unless otherwise noted

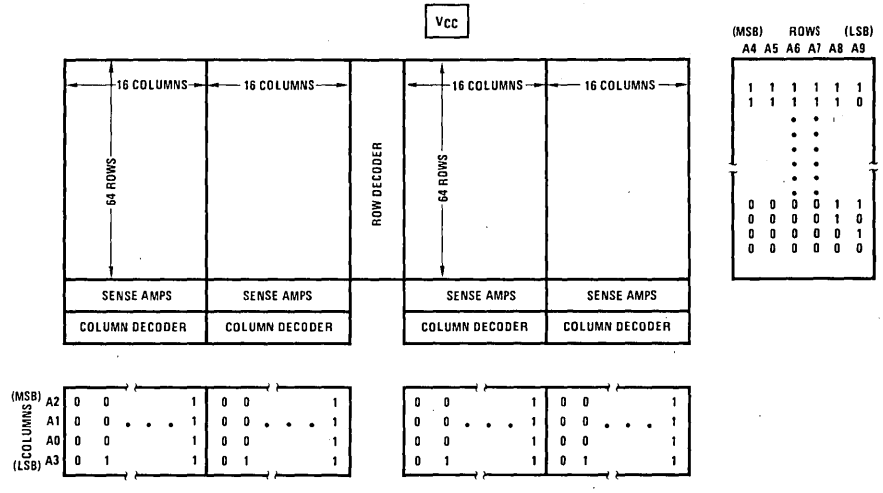
Symbol	Parameter	Conditions	NMC6514-9, NMC6514-2		NMC6514-5		Units
			Min	Max	Min	Max	
VCCDR	Data Retention Supply Voltage	VI = VCC, GND	2.0		2.0		V
ICCSB	Standby Supply Current			50		500	μA
ICCOP*	Operating Supply Current	f = 1 MHz, IO = 0, VI = VCC or GND		10		10	mA
ICCDR	Data Retention Supply Current	VCC = 3.0V, IO = 0, VI = VCC or GND		25		500	μA
II	Input Leakage Current	VI = VCC, GND	−1.0	+1.0	−10	+10	μA
VIL	Input Low Voltage		−0.3	0.8	−0.3	0.8	V
VIH	Input High Voltage		VCC−2.0	VCC+0.3	VCC−2	VCC+0.3	V
IOZ	Output Leakage Current	VI = VCC, GND	−1.0	+1.0	−10	+10	μA
VOL	Output Low Voltage	IOL = 2.0 mA		0.4		0.4	V
VOH	Output High Voltage	IOH = −1.0 mA	2.4		2.4		V
CI	Input Capacitance	f = 1 MHz		8		8	pF
CO	Output Capacitance	f = 1 MHz		10		10	pF

* ICCOP is proportional to operating frequency.

AC Test Conditions

Input Rise and Fall Times: ≤20 ns
All Timing Reference Levels: 1/2 VCC
Output Load: 1 TTL Load, 50 pF

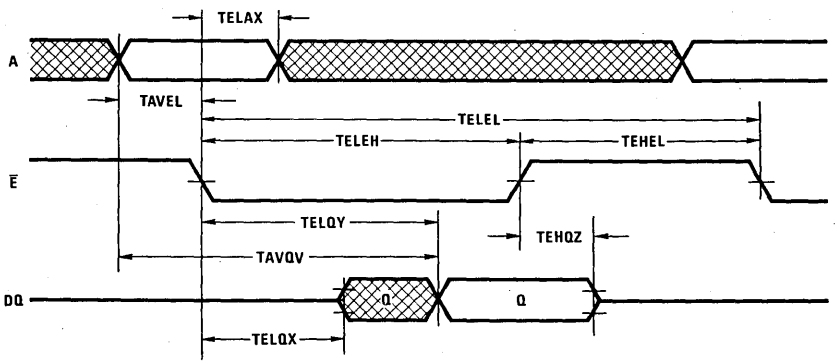
NMC6514 Bit Map and Address Decoding



Read Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6514-9, NMC6514-2		NMC6514-5		Units
		Min	Max	Min	Max	
TAVEL	Address Set-up Time	20		20		ns
TELAX	Address Hold Time	50		50		ns
TELQV	Enable Access Time		300		350	ns
TAVQV	Address Access Time		320		370	ns
TELEH	Enable ($\bar{E}$) Minimum Low Time	300		350		ns
TEHEL	Enable ($\bar{E}$) Minimum High Time	120		150		ns
TELQX	Output Enable from Enable ($\bar{E}$)		100		100	ns
TEHQZ	Output Disable from ($\bar{E}$)		100		100	ns
TELEL	Read or Write Cycle Time	420		500		ns

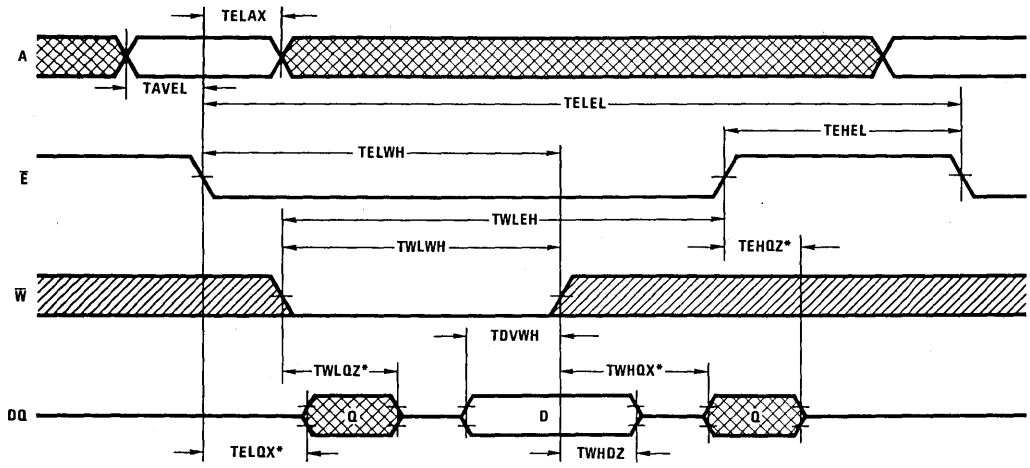
Read Cycle Waveforms



Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6514-9, NMC6514-2		NMC6514-5		Units
		Min	Max	Min	Max	
TAVEL	Address Set-up Time	20		20		ns
TELAX	Address Hold Time	50		50		ns
TWLEH	Write Pulse Width ($\bar{E}$ and $\bar{W}$ Low)	300		350		ns
TEHEL	Enable ($\bar{E}$) Minimum High Time	120		150		ns
TWLWH	Write Pulse Width ($\bar{W}$ Low)	300		350		ns
TELEL	Read or Write Cycle Time	420		500		ns
TWHQX	Output Enable from Write ($\bar{W}$)		100		100	ns
TELQX	Output Enable from Enable ($\bar{E}$)		100		100	ns
TEHQZ	Output Disable from Enable ($\bar{E}$)		100		100	ns
TWLQZ	Output Disable from Write ($\bar{W}$)		100		100	ns
TDVWH	Data Set-up Time	200		250		ns
TWHDZ	Data Hold Time	0		0		ns
TELWH	Write Pulse Width ($\bar{E}$ and $\bar{W}$ Low)	300		350		ns

Write Cycle Waveforms

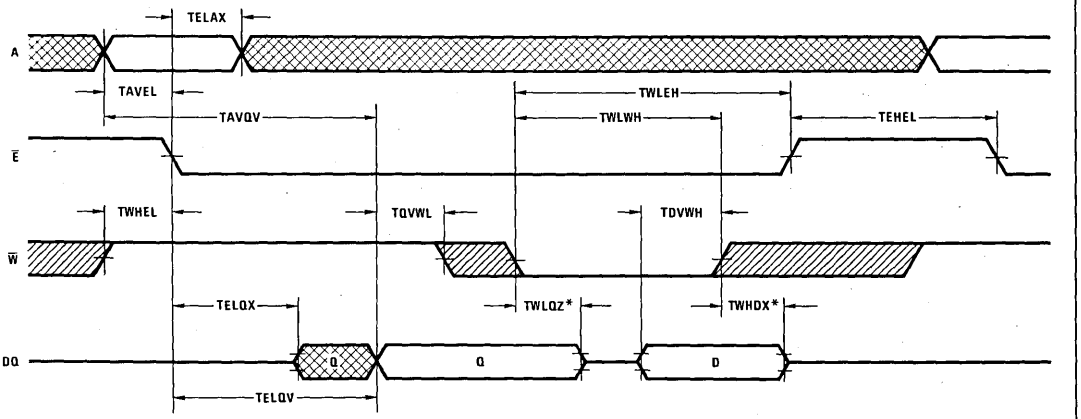


* Avoid bus contention

Read-Modify-Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6514-9, NMC6514-2		NMC6514-5		Units
		Min	Max	Min	Max	
TAVEL	Address Set-up Time	20		20		ns
TELAX	Address Hold Time	50		50		ns
TELQV	Enable Access Time		300		350	ns
TAVQV	Address Access Time		320		370	ns
TWLQZ	Output Disable from Write ($\overline{W}$)		100		100	ns
TDVWH	Data Set-up Time	200		250		ns
TWHDX	Data Hold Time	0		0		ns
TWLEH	Write Pulse Width ($\overline{W}$ and $\overline{E}$ Low)	300		350		ns
TQVWL	Data Valid to Write Time	0		0		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	300		350		ns
TELQX	Output Enable from Enable ($\overline{E}$)		100		100	ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	120		150		ns
TWHEL	$\overline{W}$ Read Mode Set-up Time	0		0		ns

Read-Modify-Write Cycle Waveforms



* Avoid bus contention

NMC6518 1024-Bit (1024 x 1) Static RAM

General Description

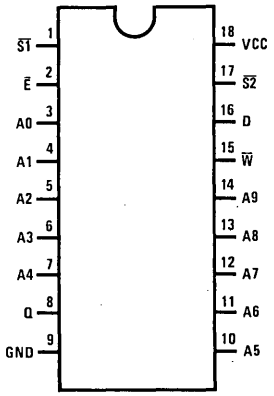
The NMC6518 is a static CMOS random access read/write memory organized as 1024 words of 1 bit each. This device is fabricated with National Semiconductor's silicon-gate CMOS technology and is fully compatible with the TTL environment. Synchronous operation is provided by the on-chip latches for the address inputs and data output. The ENABLE input serves as the device strobe controlling the latching functions. The TRI-STATE® output, in conjunction with the ENABLE input, allow easy memory expansion.

Features

- Industry standard pinout
- Low data retention voltage — 2V
- Low speed/power product
- TTL compatible — all inputs and outputs
- TRI-STATE® outputs for bus operation
- High output drive
- High noise immunity
- Military temperature range available
- On-chip address registers (latches)
- 18 pin — high density packaging
- Output data latches

Connection Diagram

Dual-In-Line Package

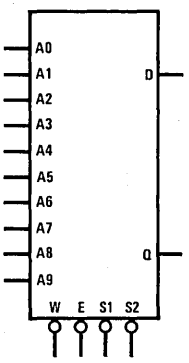


TOP VIEW

Order Number NMC6518J-2, NMC6518J-9 or NMC6518J-5
See NS Package J16A

Order Number NMC6518N-5
See NS Package N16A

Logic Symbol



Pin Names

A0-A9	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output
$\overline{S1}$, $\overline{S2}$	Chip Selects

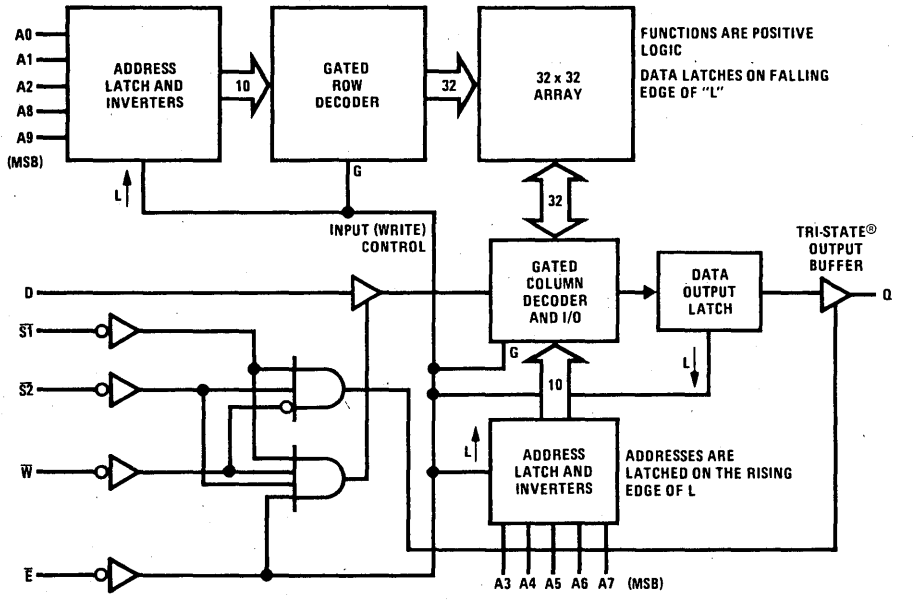
Functional Description

An NMC6518 memory cycle is initiated by the falling edge of the ENABLE input, which latches the address information into the on-chip registers. Data output is enabled when the WRITE ($\overline{W}$) input is high and the ENABLE, SELECT 1 ($\overline{S1}$) and SELECT 2 ($\overline{S2}$) inputs are LOW.

When performing a read cycle a minimum ENABLE LOW time is required to assure valid data at the output. This minimum ENABLE LOW time is defined as the device enable access time. A minimum ENABLE HIGH time is required to return the columns to the HIGH state and to precharge the sense amplifiers in preparation of the next cycle.

When performing a write cycle, the minimum ENABLE LOW time is required to enter new data. The write pulse is created by the coincident LOW of the WRITE, ENABLE and both SELECT inputs. The input data set-up and hold times are referenced to the rising edge of the WRITE, ENABLE, SELECT 1 or SELECT 2 inputs, whichever occurs first.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	7V
Voltage at Any Pin	−0.3V to VCC +0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Range

	Min	Max
Supply Voltage		
NMC6518B-9	4.5V	5.5V
NMC6518B-2	4.5V	5.5V
NMC6518-9	4.5V	5.5V
NMC6518-2	4.5V	5.5V
NMC6518-5	4.75V	5.25V
Temperature		
NMC6518B-9	−40°C	85°C
NMC6518B-2	−55°C	125°C
NMC6518-9	−40°C	85°C
NMC6518-2	−55°C	125°C
NMC6518-5	0°C	75°C

DC Electrical Characteristics over the operating range, unless otherwise noted

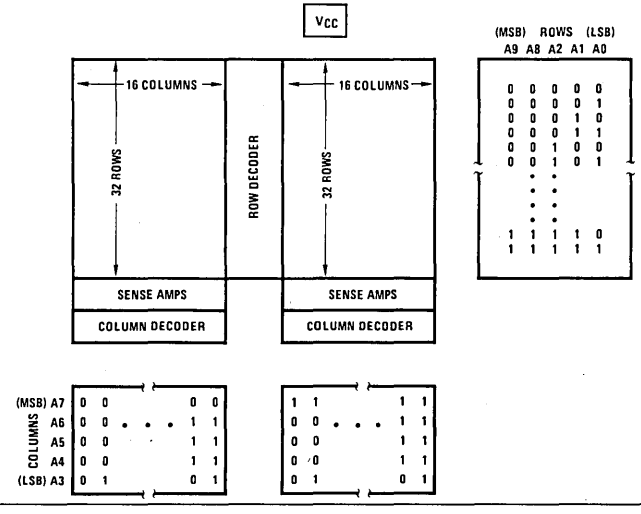
Symbol	Parameter	Conditions	NMC6518B-9, NMC6518B-2 NMC6518-9, NMC6518-2		NMC6518-5		Units
			Min	Max	Min	Max	
VCCDR	Data Retention Supply Voltage	VI = VCC, GND	2.0		2.0		V
ICCSB	Standby Supply Current			10		100	μA
ICCOP*	Operating Supply Current	f = 1 MHz, IO = 0, VI = VCC or GND		4		4	mA
ICCDR	Data Retention Supply Current	VCC = 3.0V, IO = 0, VI = VCC or GND		10		100	μA
II	Input Leakage Current	VI = VCC, GND	−1.0	+1.0	−1.0	+1.0	μA
VIL	Input Low Voltage		−0.3	0.8	−0.3	0.8	V
VIH	Input High Voltage		VCC −2.0	VCC +0.3	VCC −2	VCC +0.3	V
IOZ	Output Leakage Current	VI = VCC, GND	−1.0	+1.0	−1.0	+1.0	μA
VOL	Output Low Voltage	IOL = 3.2 mA		0.4		0.4	V
VOH	Output High Voltage	IOH = −0.4 mA	2.4		2.4		V
CI	Input Capacitance	f = 1 MHz		6		6	pF
CO	Output Capacitance	f = 1 MHz		10		10	pF

* ICCOP is proportional to operating frequency.

AC Test Conditions

Input Rise and Fall Times: ≤20 ns
All Timing Reference Levels: 1/2 VCC
Output Load: 1 TTL Load, 50 pF

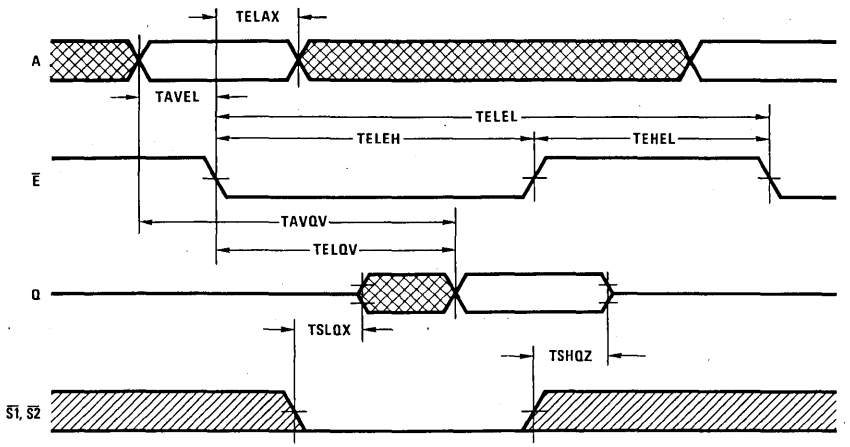
NMC6518 Bit Map and Address Decoding



Read Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6518B-9 NMC6518B-2		NMC6518-9 NMC6518-2		NMC6518-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		50		ns
TELQV	Enable Access Time		180		250		300	ns
TAVQV	Address Access Time		180		250		310	ns
TELEH	Enable ($\overline{E}$) Minimum Low Time	180		250		300		ns
TELEL	Read or Write Cycle Time	280		350		450		ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	100		100		150		ns
TSHQX	Chip Select Output Disable Time		120		160		200	ns
TSLQX	Chip Select Output Enable Time		120		160		200	ns

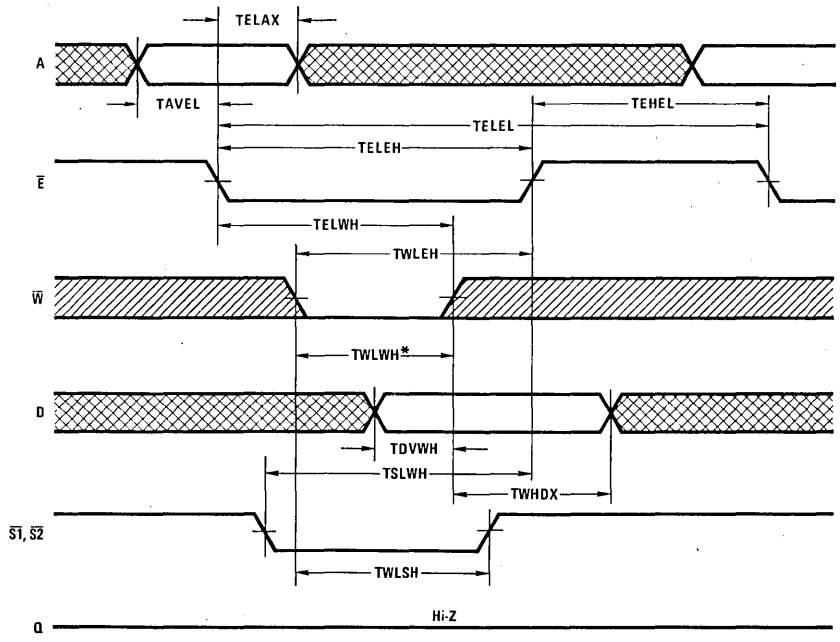
Read Cycle Waveforms



Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6518B-9 NMC6518B-2		NMC6518-9 NMC6518-2		NMC6518-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		50		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	100		130		160		ns
TELEL	Read or Write Cycle Time	280		350		450		ns
TWLSH	Chip Select Write Pulse Set-up Time	100		130		160		ns
TWLEH	Chip Enable Write Pulse Set-up Time	100		130		160		ns
TSLWH	Chip Select Write Pulse Hold Time	100		130		160		ns
TWHDX	Data Hold Time	0		0		0		ns
TDVWH	Data Set-up Time	80		110		130		ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	100		100		150		ns
TELEH	Enable ($\overline{E}$) Minimum Low Time	180		250		300		ns
TELWH	Write Pulse Width ($\overline{E}$ and $\overline{W}$ Low)	100		130		160		ns

Write Cycle Waveforms

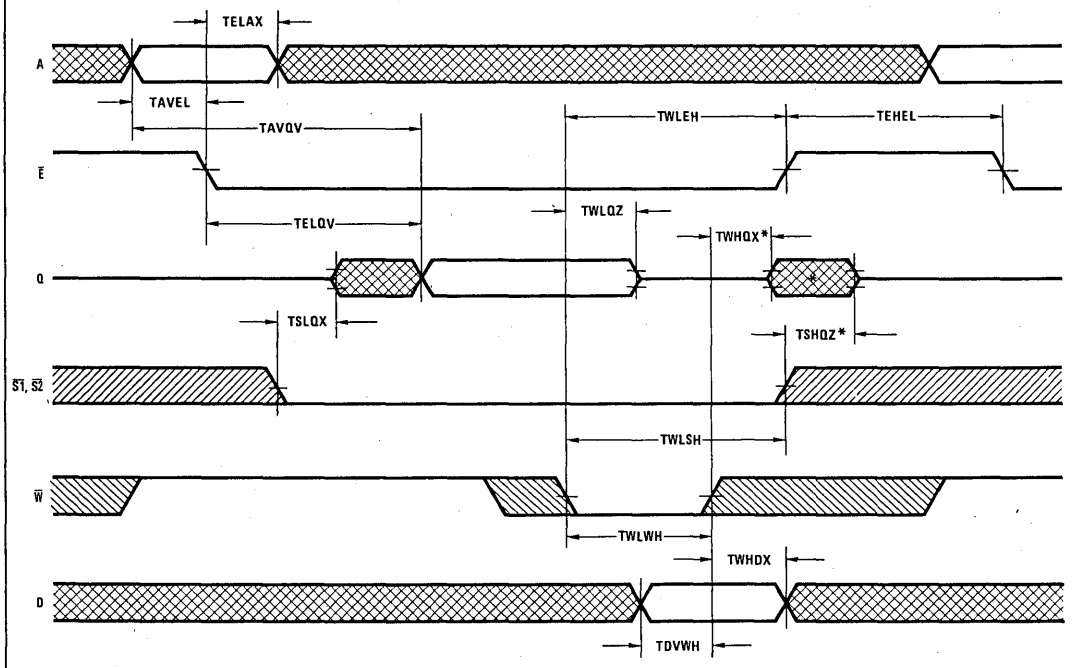


* TWLWH, the write pulse, is coincidence low of $\overline{E}$, $\overline{W}$, $\overline{S1}$, and $\overline{S2}$ inputs

Read-Modify-Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6518B-9 NMC6518B-2		NMC6518-9 NMC6518-2		NMC6518-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		50		ns
TELQV	Enable Access Time		180		250		300	ns
TAVQV	Address Access Time		180		250		310	ns
TSHQX	Chip Select Output Disable Time		120		160		200	ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	100		130		160		ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	100		100		150		ns
TWLSH	Chip Select Write Pulse Set-up Time	100		130		160		ns
TWLEH	Chip Enable Write Pulse Set-up Time	100		130		160		ns
TSLQX	Chip Select Output Enable Time		120		160		200	ns
TWHDX	Data Hold Time	0		0		0		ns
TDVWH	Data Set-up Time	80		110		130		ns
TWHQX	Output Enable from Write ($\overline{W}$)		120		160		200	ns
TWLQZ	Output Disable from Write ($\overline{W}$)		120		160		200	ns

Read-Modify-Write Cycle Waveforms



* Precede $\overline{W}$ rising edge with $\overline{E}$ rising edge to avoid unwanted output enabling

National Semiconductor

NMC6551 1024-Bit (256 x 4) Static RAM

General Description

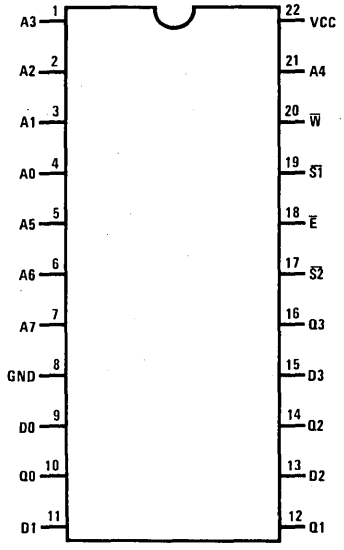
The NMC6551 is a static CMOS random access read/write memory organized as 256 words of 4 bits each. This device is fabricated with National Semiconductor's silicon-gate CMOS technology and is fully compatible with the TTL environment. Synchronous operation is provided by on-chip address input and data output latches. The ENABLE input serves as the device strobe controlling the latching functions. The I/O terminals when not data output enabled, represent high impedance ports for easy memory expansion.

Features

- Industry standard pinout
- Low data retention voltage — 2V
- Low speed/power product
- TTL compatible — all inputs and outputs
- TRI-STATE® outputs for bus operation
- High output drive
- High noise immunity
- Military temperature range available
- On-chip address registers (latches)
- 22 pin — high density packaging
- Output data latches
- Select latch for microprocessor interface

Connection Diagram

Dual-In-Line Package



TOP VIEW

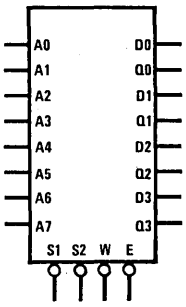
Order Number NMC6551J-2, NMC6551J-9 or NMC6551J-5
See NS Package J22A

Order Number NMC6551N-5
See NS Package N22A

Pin Names

A0-A7	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output
$\overline{S1}$, $\overline{S2}$	Chip Selects

Logic Symbol



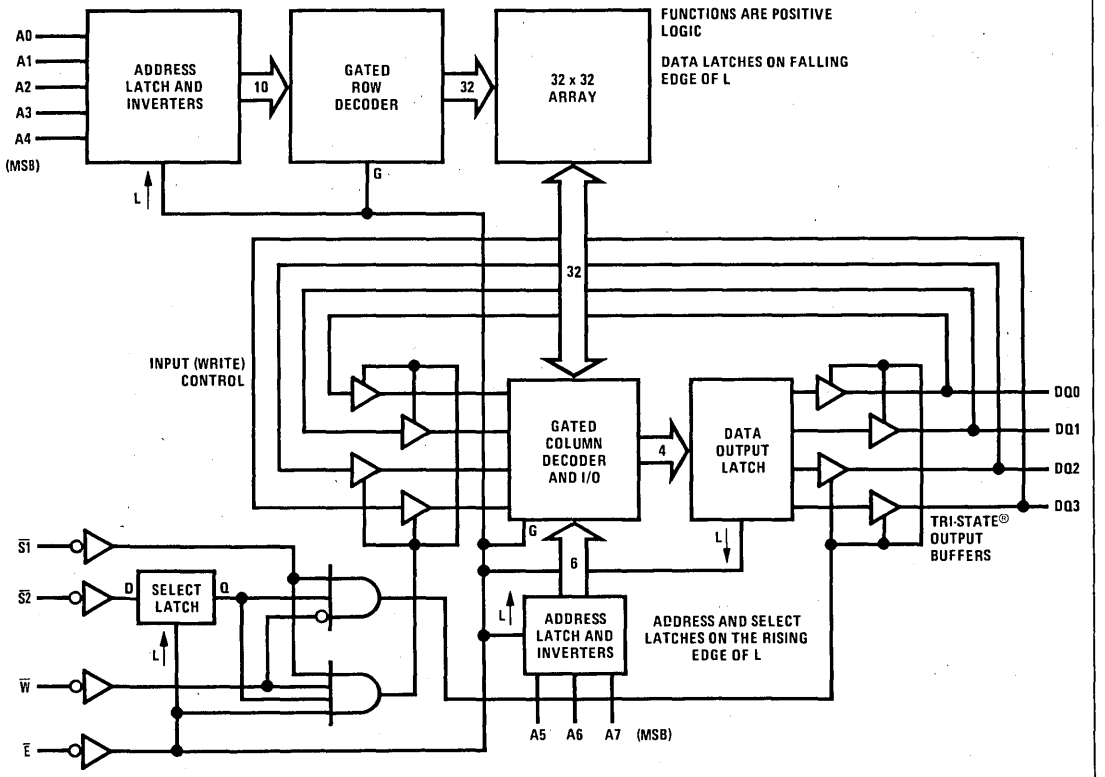
Functional Description

An NMC6551 memory cycle is initiated by the falling edge of the ENABLE ($\overline{E}$) input, which latches the ADDRESS and SELECT 2 ($\overline{S2}$) information into the on-chip registers. Set-up and hold times must be met. Data output is enabled when the WRITE ($\overline{W}$) input is HIGH and the ENABLE and SELECT 1 inputs are LOW.

When performing a read cycle a minimum ENABLE LOW time is required to assure valid data at the outputs. This minimum LOW time is defined as the device enable access time. A minimum ENABLE HIGH time is required to return the columns to the HIGH state and to precharge the sense amplifiers in preparation of the next memory cycle.

When performing a write cycle, the minimum ENABLE LOW time is required to enter new data. The write pulse timing is created by the coincident LOW of the WRITE, ENABLE and SELECT 1 inputs. The data set-up and hold times are referenced to the rising edge of the WRITE, ENABLE, or SELECT 1 input, whichever occurs first.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	7V
Voltage at Any Pin	−0.3V to VCC +0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Range

	Min	Max
Supply Voltage		
NMC6551B-9	4.5V	5.5V
NMC6551B-2	4.5V	5.5V
NMC6551-9	4.5V	5.5V
NMC6551-2	4.5V	5.5V
NMC6551-5	4.75V	5.25V
Temperature		
NMC6551B-9	−40°C	85°C
NMC6551B-2	−55°C	125°C
NMC6551-9	−40°C	85°C
NMC6551-2	−55°C	125°C
NMC6551-5	0°C	75°C

DC Electrical Characteristics over the operating range, unless otherwise noted

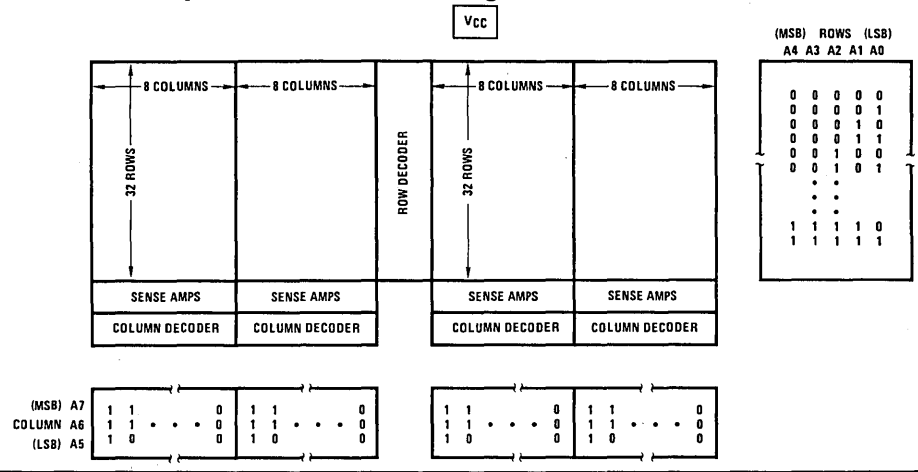
Symbol	Parameter	Conditions	NMC6551B-9, NMC6551B-2 NMC6551-9, NMC6551-2		NMC6551-5		Units
			Min	Max	Min	Max	
VCCDR	Data Retention Supply Voltage	VI = VCC, GND	2.0		2.0		V
ICCSB	Standby Supply Current			10 1(+25°C)		100	μA
ICCOP*	Operating Supply Current	f = 1 MHz, IO = 0, VI = VCC or GND		4		4	mA
ICCDR	Data Retention Supply Current	VCC = 3.0V, IO = 0, VI = VCC or GND		10		100	μA
II	Input Leakage Current	VI = VCC, GND	−1.0	+1.0	−1.0	+1.0	μA
VIL	Input Low Voltage		−0.3	0.8	−0.3	0.8	V
VIH	Input High Voltage		VCC −2.0	VCC +0.3	VCC −2	VCC +0.3	V
IOZ	Output Leakage Current	VI = VCC, GND	−1.0	+1.0	−1.0	+1.0	μA
VOL	Output Low Voltage	IOL = 3.2 mA		0.4		0.4	V
VOH	Output High Voltage	IOH = −0.4 mA	2.4		2.4		V
CI	Input Capacitance	f = 1 MHz		6		6	pF
CO	Output Capacitance	f = 1 MHz		10		10	pF

* ICCOP is proportional to operating frequency.

AC Test Conditions

Input Rise and Fall Times: ≤20 ns
All Timing Reference Levels: 1/2 VCC
Output Load: 1 TTL Load, 50 pF

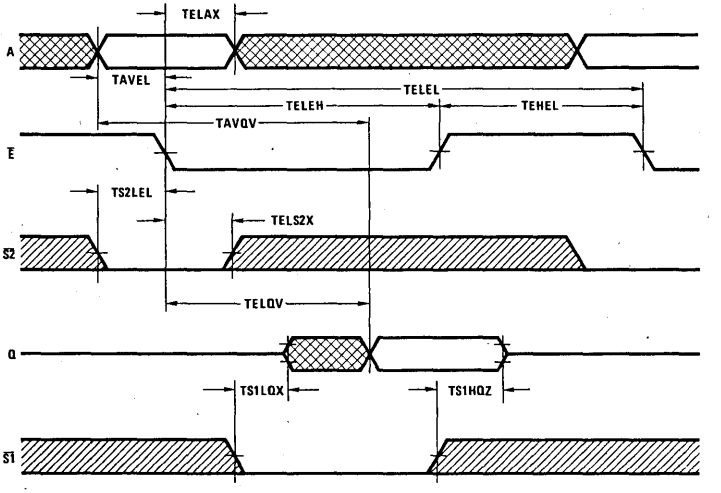
NMC6551 Bit Map and Address Decoding



Read Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6551B-9 NMC6551B-2		NMC6551-9 NMC6551-2		NMC6551-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TELQV	Enable Access Time		220		300		350	ns
TAVQV	Address Access Time		220		300		360	ns
TELEH	Enable ($\overline{E}$) Minimum Low Time	220		300		350		ns
TELS2X	Chip Select 2 Hold Time	40		50		70		ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	100		100		150		ns
TELEL	Read or Write Cycle Time	320		400		500		ns
TS1LQX	Chip Select 1 Output Enable Time		130		150		180	ns
TS1HQZ	Chip Select 1 Output Disable Time		130		150		180	ns
TS2LEL	Chip Select 2 Set-up Time	0		0		10		ns

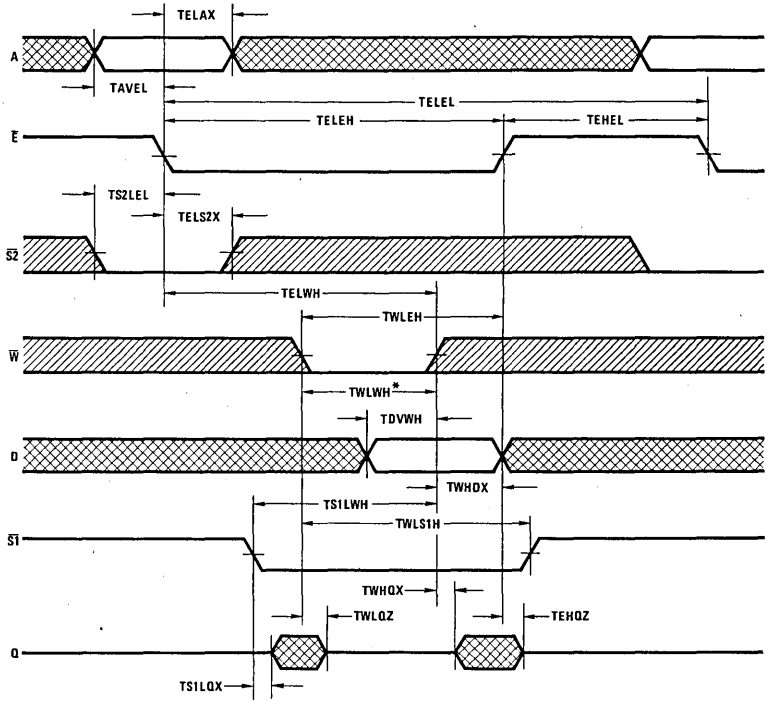
Read Cycle Waveforms



Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6551B-9 NMC6551B-2		NMC6551-9 NMC6551-2		NMC6551-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	120		180		210		ns
TELEL	Read or Write Cycle Time	320		400		500		ns
TELEH	Enable ($\bar{E}$) Minimum Low Time	220		300		350		ns
TS2LEL	Chip Select 2 Set-up Time	0		0		10		ns
TWHDX	Data Hold Time	0		0		0		ns
TELS2X	Chip Select 2 Hold Time	40		50		70		ns
TDVWH	Data Set-up Time	100		150		170		ns
TELWH	Write Pulse Width ($\bar{E}$ and $\overline{W}$ Low)	120		180		210		ns
TEHEL	Enable ($\bar{E}$) Minimum High Time	100		100		150		ns
TWLEH	Write Pulse Width ($\bar{E}$ and $\overline{W}$ Low)	120		180		210		ns
TS1LWH	Chip Select 1 Write Pulse Hold Time	120		180		210		ns
TWLS1H	Chip Select 1 Write Pulse Set-up Time	120		180		210		ns
TS1LQX	Output Enable from $\overline{S1}$		130		150		180	ns
TWLQZ	Output Disable from $\overline{W}$		130		150		180	ns
TWHQX	Output Enable from $\overline{W}$		130		150		180	ns
TEHQZ	Output Disable from $\bar{E}$		130		150		180	ns

Write Cycle Waveforms

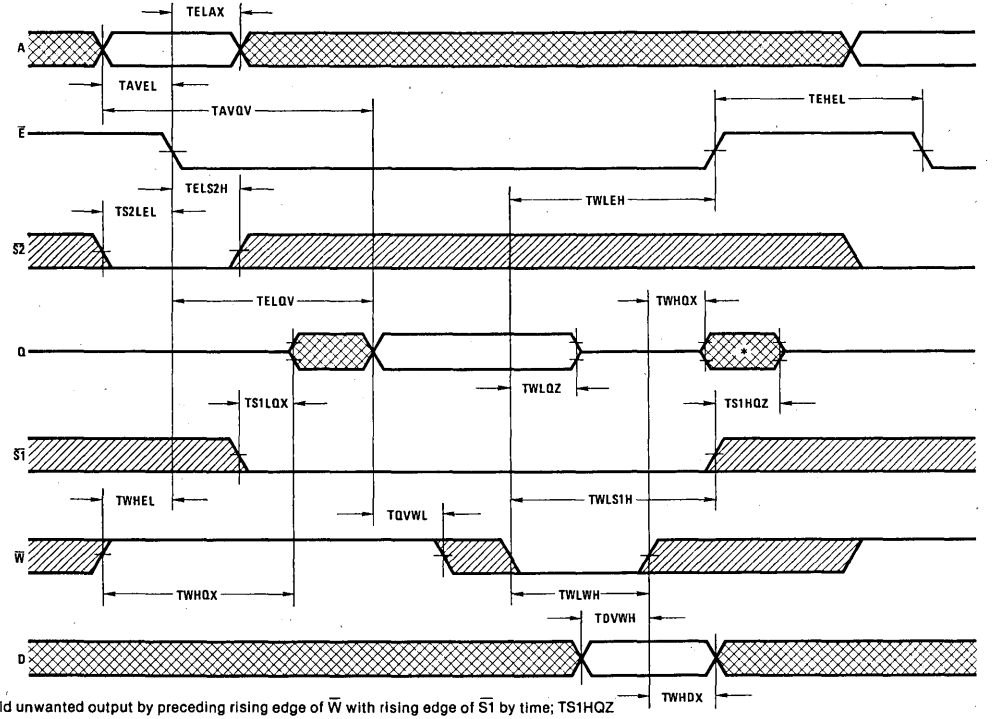


* TWLWH, the write pulse, is the coincidence low of $\bar{E}$, $\overline{W}$, and $\overline{S1}$ inputs

Read-Modify-Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6551B-9 NMC6551B-2		NMC6551-9 NMC6551-2		NMC6551-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TELQV	Enable Access Time		220		300		350	ns
TAVQV	Address Access Time		220		300		360	ns
TWLEH	Write Pulse Width ($\overline{W}$ and $\overline{E}$ Low)	120		180		210		ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	100		100		150		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	120		180		210		ns
TELEL	Read or Write Cycle Time	320		400		500		ns
TS1LQX	Chip Select 1 Output Enable Time		130		150		180	ns
TS1HQZ	Chip Select 1 Output Disable Time		130		150		180	ns
TS2LEL	Chip Select 2 Set-up Time	0		0		10		ns
TWHDX	Data Hold Time	0		0		0		ns
TELS2H	Chip Select 2 Hold Time	40		50		70		ns
TWLS1H	Chip Select 1 Write Pulse Set-up Time	120		180		210		ns
TWLQZ	Output Disable from Write ($\overline{W}$)		130		150		180	ns
TDVWH	Data Set-up Time	100		150		170		ns
TQVWL	Data Valid to Write Time	0		0		0		ns
TWHEL	$\overline{W}$ Read Mode Set-up Time	0		0		0		ns
TWHQX	Output Enable from Write ($\overline{W}$)		130		150		180	ns

Read-Modify-Write Cycle Waveforms



* Avoid unwanted output by preceding rising edge of $\overline{W}$ with rising edge of $\overline{S1}$ by time; TS1HQZ

National Semiconductor

CMOS RAMs

NMC6552 1024-Bit (256 x 4) Static RAM

General Description

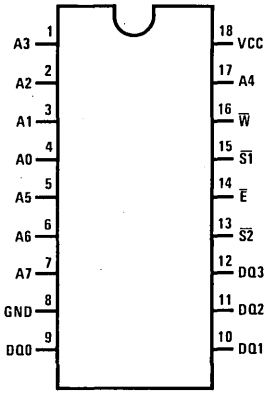
The NMC6552 is a static CMOS random access read/write memory organized as 256 words of 4 bits each. This device is fabricated with National Semiconductor's silicon-gate CMOS technology and is fully compatible with the TTL environment. Synchronous operation is provided by the on-chip address input and data output registers. The ENABLE input serves as the device strobe controlling the latching functions. The data I/O terminals, when not output data enabled, represent a high impedance for easy memory expansion.

Features

- Low data retention voltage — 2V
- Low speed/power product
- TTL compatible — all inputs and outputs
- TRI-STATE® outputs for bus operation
- High output drive
- High noise immunity
- Military temperature range available
- On-chip address registers (latches)
- Common I/O — high density packaging
- Output data latches
- Select latch for microprocessor interface

Connection Diagram

Dual-In-Line Package

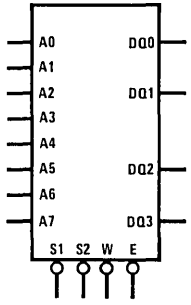


TOP VIEW

Order Number NMC6552J-2, NMC6552J-9 or NMC6552J-5
See NS Package J18A

Order Number NMC6552N-5
See NS Package N18A

Logic Symbol



Pin Names

A0-A7	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
DQ0-DQ3	Data In/Out
$\overline{S1}$, $\overline{S2}$	Chip Selects

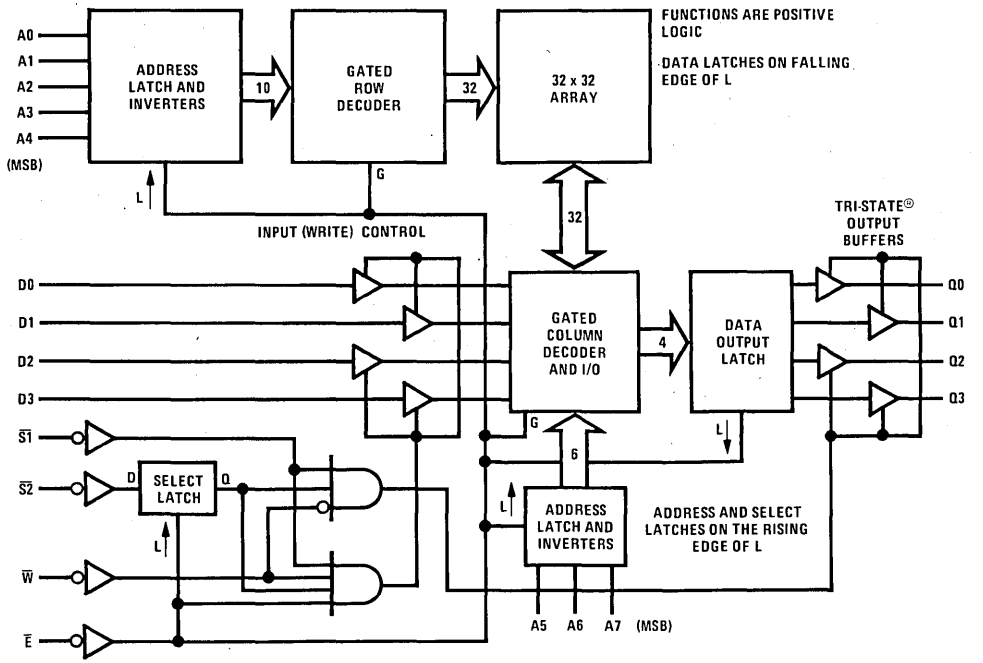
Functional Description

An NMC6552 memory cycle is initiated by the falling edge of the ENABLE ($\overline{E}$) input, which latches the ADDRESS and SELECT 2 ($\overline{S2}$) information into the on-chip registers. The output data latches are transparent when the ENABLE input is LOW, allowing the state of the memory to be presented to the output buffers. The output buffers are enabled when the WRITE ($\overline{W}$) input is HIGH, and the SELECT 1 ($\overline{S1}$) input is LOW.

When performing a read cycle, a minimum ENABLE LOW time is required to assure valid data at the device outputs. This minimum LOW time is defined as the enable access time. A minimum ENABLE HIGH time is required to return the columns to the HIGH state and to precharge the sense amplifiers in preparation of the next cycle. The data is latched with the rising edge of the ENABLE input, allowing maintenance of output data until the SELECT 1 input goes HIGH.

When performing a write cycle, a minimum ENABLE LOW time is required for new data entry. The write pulse timing is defined by the coincident LOW of the WRITE, ENABLE and SELECT 1 inputs. The input data set-up and hold times are referenced to the rising edge of the WRITE, ENABLE, or SELECT 1 inputs, whichever occurs first.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	7V
Voltage at Any Pin	−0.3V to VCC +0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Range

	Min	Max
Supply Voltage		
NMC6552B-9	4.5V	5.5V
NMC6552B-2	4.5V	5.5V
NMC6552-9	4.5V	5.5V
NMC6552-2	4.5V	5.5V
NMC6552-5	4.75V	5.25V
Temperature		
NMC6552B-9	−40°C	85°C
NMC6552B-2	−55°C	125°C
NMC6552-9	−40°C	85°C
NMC6552-2	−55°C	125°C
NMC6552-5	0°C	75°C

DC Electrical Characteristics over the operating range, unless otherwise noted

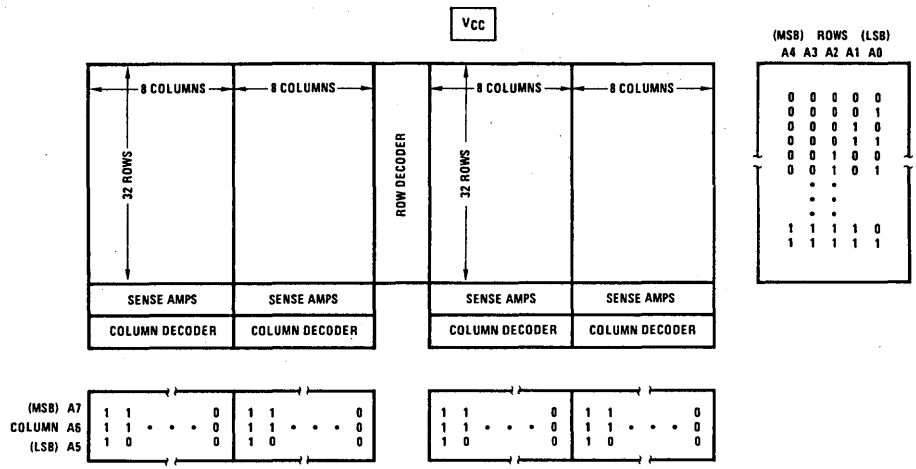
Symbol	Parameter	Conditions	NMC6552B-9, NMC6552B-2 NMC6552-9, NMC6552-2		NMC6552-5		Units
			Min	Max	Min	Max	
VCCDR	Data Retention Supply Voltage	VI = VCC, GND	2.0		2.0		V
ICCSB	Standby Supply Current			10 1(+25°C)		100	μA
ICCOP*	Operating Supply Current	f = 1 MHz, IO = 0, VI = VCC or GND		4		4	mA
ICCDR	Data Retention Supply Current	VCC = 3.0V, IO = 0, VI = VCC or GND		10		100	μA
II	Input Leakage Current	VI = VCC, GND	−1.0	+1.0	−1.0	+1.0	μA
VIL	Input Low Voltage		−0.3	0.8	−0.3	0.8	V
VIH	Input High Voltage		VCC−2.0	VCC+0.3	VCC−2	VCC+0.3	V
IOZ	Output Leakage Current	VI = VCC, GND	−1.0	+1.0	−1.0	+1.0	μA
VOL	Output Low Voltage	IOL = 3.2 mA		0.4		0.4	V
VOH	Output High Voltage	IOH = −0.4 mA	2.4		2.4		V
CI	Input Capacitance	f = 1 MHz		6		6	pF
CO	Output Capacitance	f = 1 MHz		10		10	pF

* ICCOP is proportional to operating frequency.

AC Test Conditions

Input Rise and Fall Times: ≤20 ns
All Timing Reference Levels: 1/2 VCC
Output Load: 1 TTL Load, 50 pF

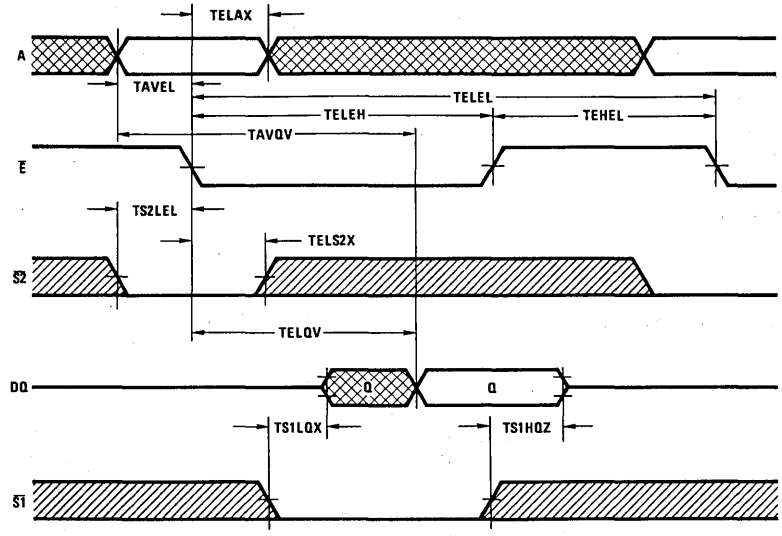
NMC6552 Bit Map and Address Decoding



Read Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6552B-9 NMC6552B-2		NMC6552-9 NMC6552-2		NMC6552-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TELQV	Enable Access Time		220		300		350	ns
TAVQV	Address Access Time		220		300		360	ns
TELEH	Enable ($\overline{E}$) Minimum Low Time	220		300		350		ns
TELS2X	Chip Select 2 Hold Time	40		50		70		ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	100		100		150		ns
TELEL	Read or Write Cycle Time	320		400		500		ns
TS1LQX	Chip Select 1 Output Enable Time		130		150		180	ns
TS1HQZ	Chip Select 1 Output Disable Time		130		150		180	ns
TS2LEL	Chip Select 2 Set-up Time	0		0		10		ns

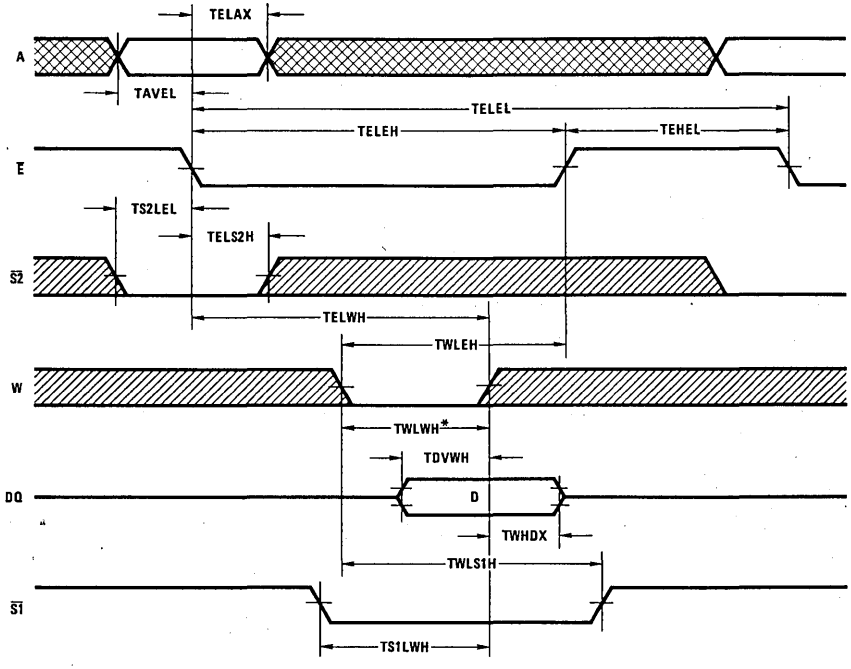
Read Cycle Waveforms



Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6552B-9 NMC6552B-2		NMC6552-9 NMC6552-2		NMC6552-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TS2LEL	Chip Select 2 Set-up Time	0		0		10		ns
TWHDX	Data Hold Time	0		0		0		ns
TELEH	Enable ($\bar{E}$) Minimum Low Time	220		300		350		ns
TWLWH	Write Pulse Width ($\bar{W}$ Low)	120		180		210		ns
TELEL	Read or Write Cycle Time	320		400		500		ns
TEHEL	Enable ($\bar{E}$) Minimum High Time	100		100		150		ns
TDVWH	Data Set-up Time	100		150		170		ns
TELWH	Write Pulse Width ($\bar{E}$ and $\bar{W}$ Low)	120		180		210		ns
TWLEH	Write Pulse Width ($\bar{W}$ and $\bar{E}$ Low)	120		180		210		ns
TELS2H	Chip Select 2 Hold Time	40		50		70		ns
TWLS1H	Chip Select 1 Write Pulse Set-up Time	120		180		210		ns
TS1LWL	Chip Select 1 Write Pulse Hold Time	120		180		210		ns

Write Cycle Waveforms

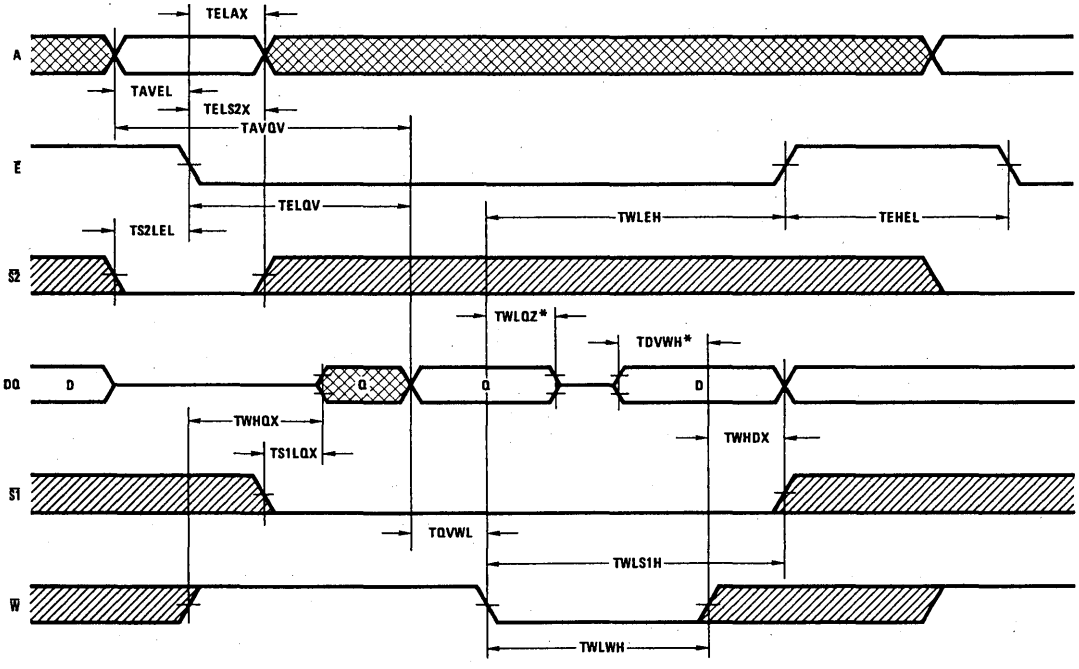


* TWLWH, the write pulse, is the coincidence low of $\bar{E}$, $\bar{W}$, and $\bar{S1}$ inputs

Read-Modify-Write Cycle AC Electrical Characteristics over the operating range

Symbol	Parameter	NMC6552B-9 NMC6552B-2		NMC6552-9 NMC6552-2		NMC6552-5		Units
		Min	Max	Min	Max	Min	Max	
TAVEL	Address Set-up Time	0		0		10		ns
TELAX	Address Hold Time	40		50		70		ns
TELQV	Enable Access Time		220		300		350	ns
TAVQV	Address Access Time		220		300		360	ns
TS2LEL	Chip Select 2 Set-up Time	0		0		10		ns
TWHDX	Data Hold Time	0		0		0		ns
TELS2X	Chip Select 2 Hold Time	40		50		70		ns
TWLS1H	Chip Select 1 Write Pulse Set-up Time	120		180		210		ns
TS1LQX	Chip Select 1 Output Enable Time		130		150		180	ns
TDVWH	Data Set-up Time	100		150		170		ns
TWLEH	Write Pulse Width ($\overline{W}$ and $\overline{E}$ Low)	120		180		210		ns
TQVWL	Data Valid to Write Time	0		0		0		ns
TWLWH	Write Pulse Width ($\overline{W}$ Low)	120		180		210		ns
TEHEL	Enable ($\overline{E}$) Minimum High Time	100		100		150		ns
TQVWL	Data Valid to Write Time	0		0		0		ns
TWHQX	Output Enable from Write ($\overline{W}$)		130		150		180	ns
TWLQZ	Output Disable from Write ($\overline{W}$)		130		150		180	ns

Read-Modify-Write Cycle Waveforms



* Avoid bus contention

Section 3

Bipolar RAMs

3

Bipolar RAMs offer the best sclution to problems requiring high speed read-write memory. National's product line includes the devices in this section to complement our bipolar microprocessor and logic lines.

TTL

National Semiconductor

Bipolar RAMs

DM7589/DM8589 64-Bit (16 x 4) RAM

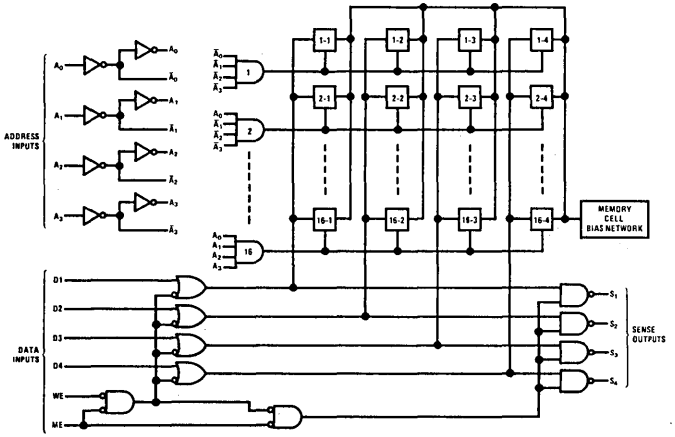
General Description

The DM7589/DM8589 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the logical "1" state.

Features

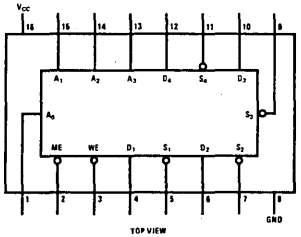
- Series 54/74 compatible
- Organized as 16 4-bit words
- Typical access from chip enable 23 ns
- Typical access 35 ns
- Typical power dissipation 400 mW
- Open collector outputs to permit "wire OR" capability

Block Diagram



Connection Diagram

Dual-In-Line Package



Order Number DM7589J or DM8589J
See NS Package J16A

Order Number DM8589N
See NS Package N16A

Truth Table

MEMORY ENABLE	WRITE ENABLE	OPERATION	OUTPUTS
0	0	Write	Logical "1" State
0	1	Read	Complement of Data Stored in Memory
1	X	Hold	Logical "1" State

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Operating Conditions

Operating Temperature Range	
DM7589	−55°C to +125°C
DM8589	0°C to +70°C

Electrical Characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7589 / DM8589	V_{CC} = 4.5V / V_{CC} = 4.75V		2.0			V
Logical "0" Input Voltage	DM7589 / DM8589	V_{CC} = 4.5V / V_{CC} = 4.75V				0.8	V
Logical "1" Output Current	DM7589 / DM8589	V_{CC} = 5.5V / V_{CC} = 5.25V	V_O = 5.25V			100 / 20	μA / μA
Logical "0" Output Voltage	DM7589 / DM8589	V_{CC} = 4.5V / V_{CC} = 4.75V	I_O = 12 mA			0.4	V
Logical "1" Input Current	DM7589 / DM8589	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 2.4V			40	μA
	DM7589 / DM8589	V_{CC} = 5.5V / V_{CC} = 5.25V	V_{IN} = 5.5V			1	mA
Logical "0" Input Current	DM7589 / DM8589	V_{CC} = 5.5V / V_{CC} = 5.25V				−1.6	mA
Supply Current	DM7589 / DM8589	V_{CC} = 5.5V / V_{CC} = 5.25V	All Inputs at GND		80	120	mA
Input Clamp Voltage	DM7589 / DM8589	V_{CC} = 4.5V / V_{CC} = 4.75V	I_{IN} = −12 mA			−1.5	V

Switching Characteristics (Over recommended operating ranges of V_{CC} and T_A)

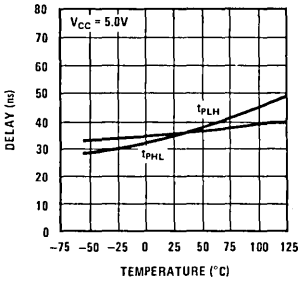
PARAMETER			CONDITIONS	DM7589 MIN	DM7589 TYP	DM7589 MAX	DM8589 MIN	DM8589 TYP	DM8589 MAX	UNITS
t_{PLH}	Access Time From Address		R_{L1} = 300Ω, R_{L2} = 600Ω, C_L = 30 pF		34	80		34	60	ns
t_{PHL}					35	80		35	60	ns
t_{PLH}	Disable Time From Memory Enable				23	55		23	40	ns
t_{PHL}	Enable Time From Memory Enable				23	55		23	40	ns
t_{SETUP}	Setup Time	Address to Write Enable		0	−14		0	−14		ns
		Data to Write Enable		0	−15		0	−15		ns
		Memory Enable To Write Enable		0	−10		0	−10		ns
t_{HOLD}	Hold Time	Address From Write Enable		5	−7		5	−7		ns
		Data From Write Enable		0	−14		0	−14		ns
		Memory Enable From Write Enable		0	−10		0	−10		ns
t_{WP}	Write Pulse Width			50	20		40	20		ns
t_{SR}	Sense Recovery Time				31	65		31	55	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

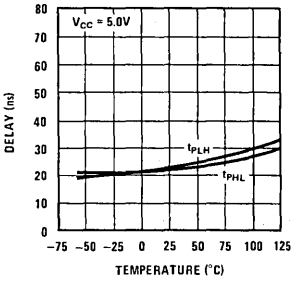
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7589 and across the 0°C to 70°C range for the DM8589. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Typical Performance Characteristics

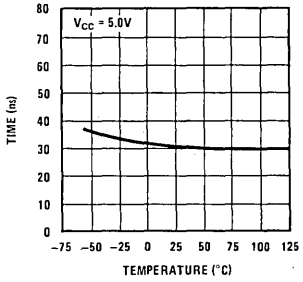
Delay from Address to Output



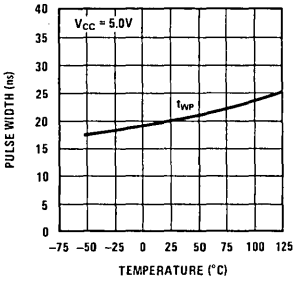
Delay from Memory Enable to Output



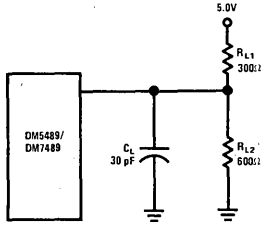
Sense Recovery Time



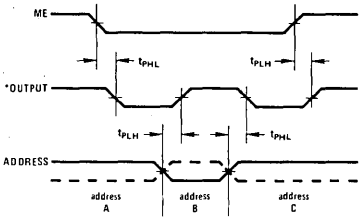
Minimum Write Pulse Width



AC Test Circuit and Switching Time Waveforms

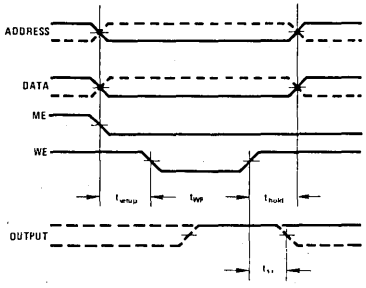


Read Cycle



*Output shown for stored data in address A = 1, in address B = 0.

Write Cycle



National Semiconductor

DM7599/DM8599 64-Bit (16 × 4) TRI-STATE® RAM

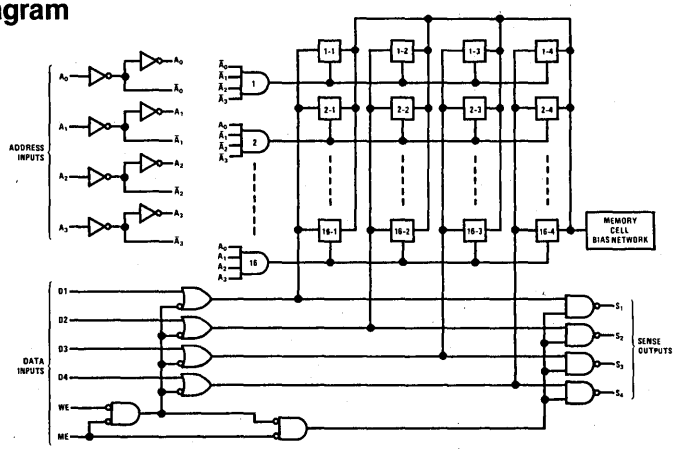
General Description

The DM7599/DM8599 is a fully decoded 64-bit RAM organized as 16 4-bit words. The memory is addressed by applying a binary number to the four Address inputs. After addressing, information may be either written into or read from the memory. To write, both the Memory Enable and the Write Enable inputs must be in the logical "0" state. Information applied to the four Write inputs will then be written into the addressed location. To read information from the memory the Memory Enable input must be in the logical "0" state and the Write Enable input in the logical "1" state. Information will be read as the complement of what was written into the memory. When the Memory Enable input is in the logical "1" state, the outputs will go to the high-impedance state. This allows up to 128 memories to be connected to a common bus-line without the use of pull-up resistors. All memories except one are gated into the high-impedance while the one selected memory exhibits the normally totem-pole low impedance output characteristics of TTL.

Features

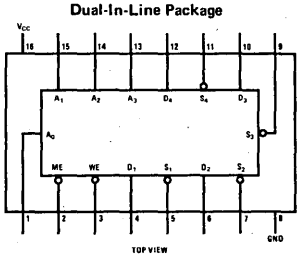
- Series 54/74 compatible
- Same pin-out as SN5489/SN7489
- Organized as 16 4-bit words
- Expandable to 2048 4-bit words without additional resistors (DM8599 only)
- Typical access from chip enable 20 ns
- Typical access time 28 ns
- Typical power dissipation 400 mW

Block Diagram



Connection Diagram

Dual-In-Line Package



Order Number DM7599J or DM8599J
See NS Package J16A
Order Number DM8599N
See NS Package N16A

Truth Table

MEMORY ENABLE	WRITE ENABLE	OPERATION	OUTPUTS
0	0	Write	Hi-Z State
0	1	Read	Complement of Data Stored in Memory
1	X	Hold	Hi-Z State

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Time that two bus-connected devices may be in opposite low impedance states simultaneously	Indefinite
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Operating Conditions

Operating Temperature Range	
DM7599	−55°C to +125°C
DM8599	0°C to +70°C

Electrical Characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7599	V_{CC} = 4.5V		2.0			V
	DM8599	V_{CC} = 4.75V					
Logical "0" Input Voltage	DM7599	V_{CC} = 4.5V				0.8	V
	DM8599	V_{CC} = 4.75V					
Logical "1" Output Voltage	DM7599	V_{CC} = 4.5V	I_O = −2 mA	2.4			V
	DM8599	V_{CC} = 4.75V	I_O = −5.2 mA	2.4			V
Logical "0" Output Voltage	DM7599	V_{CC} = 4.5V	I_O = 12 mA			0.4	V
	DM8599	V_{CC} = 4.75V					
Third State Output Current	DM7599	V_{CC} = 5.5V	V_O = 0.4V			±40	μA
	DM8599	V_{CC} = 5.25V	V_O = 2.4V			±40	
Logical "1" Input Current	DM7599	V_{CC} = 5.5V	V_{IN} = 2.4V			40	μA
	DM8599	V_{CC} = 5.25V					
	DM7599	V_{CC} = 5.5V	V_{IN} = 5.5V			1	mA
	DM8599	V_{CC} = 5.25V					
Logical "0" Input Current	DM7599	V_{CC} = 5.5V	V_{IN} = 0.4V			−1.6	mA
	DM8599	V_{CC} = 5.25V					
Output Short Circuit Current (Note 3)	DM7599	V_{CC} = 5.5V		−30		−70	mA
	DM8599	V_{CC} = 5.25V					
Supply Current	DM7599	V_{CC} = 5.5V	All Inputs at GND		80	120	mA
	DM8599	V_{CC} = 5.25V					
Input Clamp Voltage	DM7599	V_{CC} = 4.5V	I_{IN} = −12 mA			−1.5	V
	DM8599	V_{CC} = 4.75V					

Switching Characteristics (Over recommended operating ranges of V_{CC} and T_A)

PARAMETER			CONDITIONS	DM7599 MIN	DM7599 TYP	DM7599 MAX	DM8599 MIN	DM8599 TYP	DM8599 MAX	UNITS
t_{PLH}	Access Time From Address		R_{L1} = 400Ω, R_{L2} = 1.0 kΩ, C_L = 50 pF		27	70		27	50	ns
t_{PHL}					28	70		28	50	ns
t_{ZH}	Enable Time From Memory Enable				16	45		16	30	ns
t_{ZL}					20	40		20	35	ns
t_{ZH}	Sense Recovery Time From Write Enable				20	40		20	35	ns
t_{ZL}					35	65		35	55	ns
t_{HZ}	Disable Time From Memory Enable		R_{L1} = 400Ω, R_{L2} = 1.0k, C_L = 5.0 pF		10	30		10	25	ns
t_{LZ}					14	35		14	30	ns
t_{SETUP}	Setup Time	Address to Write Enable		0	−14		0	−14		ns
		Data to Write Enable		0	−15		0	−15		ns
		Memory Enable to Write Enable		0	−10		0	−10		ns
t_{HOLD}	Hold Time	Address From Write Enable		5	−7		5	−7		ns
		Data From Write Enable		0	−14		0	−14		ns
		Memory Enable From Write Enable		0	−10		0	−10		ns
t_{WP}	Write Pulse Width			50	20		40	20		ns

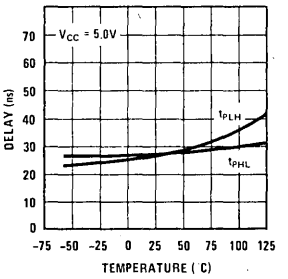
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7599 and across the 0°C to 70°C range for the DM8599. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

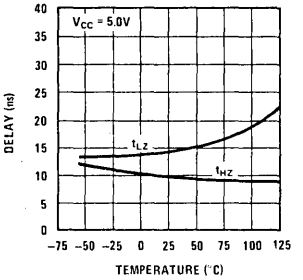
Note 3: Only one output at a time should be shorted.

Typical Performance Characteristics

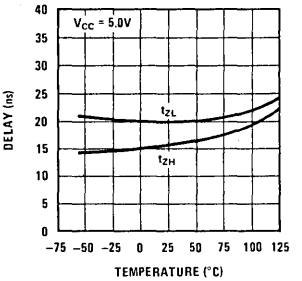
Delay from Address to Output



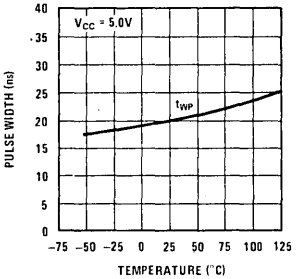
Delay From Memory Enable To High Impedance State



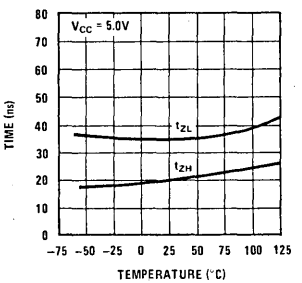
Delay from Memory Enable to Low Impedance State



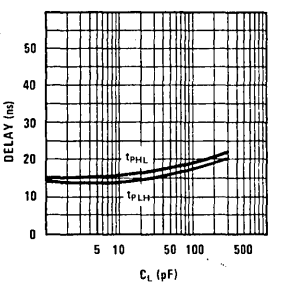
Minimum Write Pulse Width



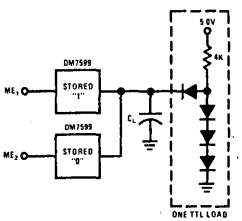
Sense Recovery Time



Delay from Enable to Output vs Load Capacitance



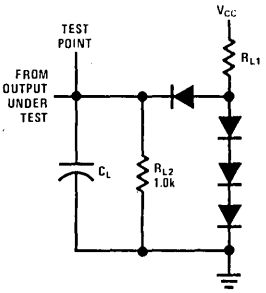
Test Circuit



Test Circuit for Delay vs Load Capacitance

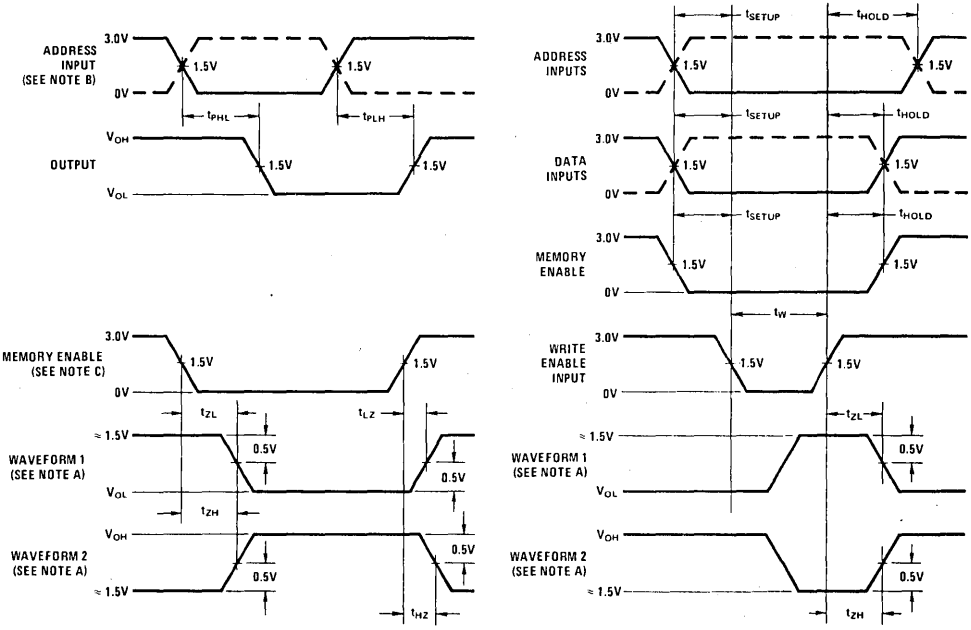
Note: In a typical application the output of the TRI-STATE memories might be wired together and one would be switching to the low impedance state at the same time the circuit previously selected would be switching back into the high impedance state. The measurements of delay versus load capacitance were made under conditions which simulate actual operating conditions in an application. (See test circuit.)

AC Test Circuit



C_L includes probe and jig capacitance.
All diodes are 1N3064.

Switching Time Waveforms



Note A: Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.

Note B: When measuring delay times from address inputs, the memory enable input is low and the write enable input is high.

Note C: When measuring delay times from memory enable input, the address inputs are steady-state and the write enable input is high.

Note D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1.0 MHz, and $Z_{OUT} \approx 50\Omega$.

Schottky

National Semiconductor

Bipolar RAMs

DM85S68 16 x 4 Edge Triggered Registers

General Description

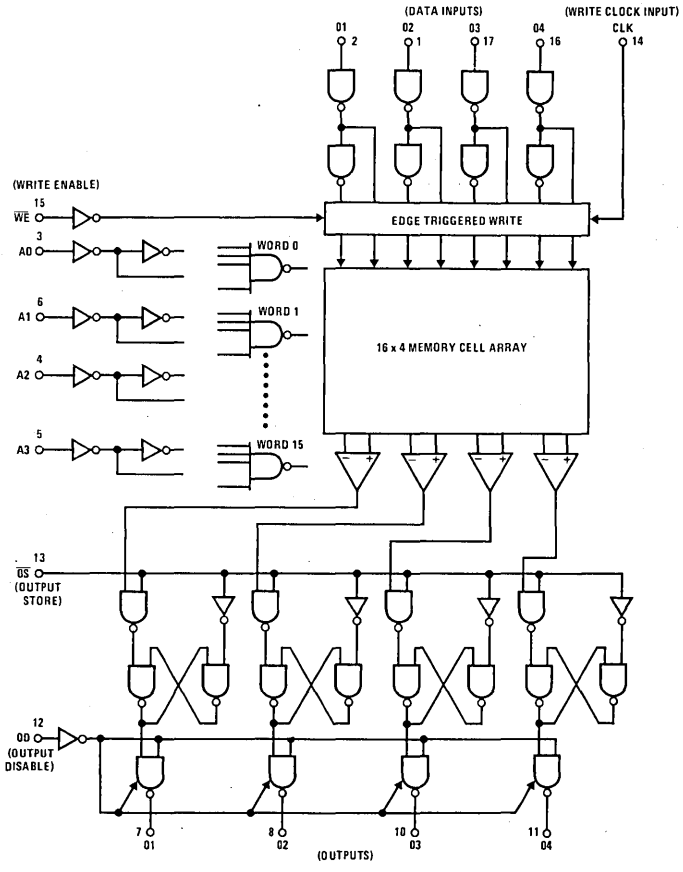
These Schottky memories are addressable "D" register files. Any of its 16 four-bit words may be asynchronously read or may be written into on the next clock transition. An input terminal is provided to enable or disable the synchronous writing of the input data into the location specified by the address terminals. An output disable terminal operates only as a TRI-STATE® output control terminal. The addressable register data may be latched at the outputs and retained as long as the output store terminal is held in a low state. This memory storage condition is independent of the state of the output disable terminal.

All input terminals are high impedance at all times, and all outputs have low impedance active drive logic states and the high impedance TRI-STATE condition.

Features

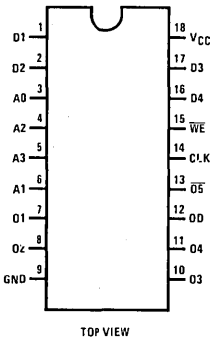
- On-chip output register
- PNP inputs reduce input loading
- Edge triggered write
- High speed—30 ns typ
- All parameters guaranteed over temperature
- TRI-STATE output
- Schottky-clamped for high speed
- Optimized for register stack applications
- Typical power dissipation—350 mW

Logic and Block Diagram



Connection Diagram

Dual-In-Line Package



Order Number DM85S68N
See NS Package N18A

Absolute Maximum Ratings

Supply Voltage	−0.5V to +7V
Input Voltage	−1.2V to +5.5V
Output Voltage	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

DC Electrical Characteristics (Note 2)

Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = −5.2 mA	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA			0.45	V
I_{IH}	High Level Input Current	V_{CC} = Max, Clock Input V_{IH} = 2.4V All Others			50 25	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_{IH} = 5.5V			1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, Clock Input V_{IL} = 0.5V All Others			−500 −250	μA μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max, V_{OL} = 0V (Note 3)	−20		−55	mA
I_{CC}	Supply Current	V_{CC} = Max		70	100	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA			−1.2	V
I_{OZ}	TRI-STATE Output Current	V_{CC} = Max V_O = 2.4V V_O = 0.5V			40 −40	μA

AC Electrical Characteristics (With standard load) 5V ± 5%, 0°C to +70°C

Parameter			Conditions	Min	Typ	Max	Units
t_{ZH}	Output Enable to High Level				20	35	ns
t_{ZL}	Output Enable to Low Level				14	24	ns
t_{HZ}	Output Disable Time from High Level				10	15	ns
t_{LZ}	Output Disable Time from Low Level				12	18	ns
t_{AA}	Access Time	Address to Output			30	40	ns
t_{OSA}		Output Store to Output			20	30	
t_{CA}		Clock to Output			25	40	
t_{ASC}	Set-Up Time	Address to Clock		15	5		ns
t_{DSC}		Data to Clock		5	5		
t_{ASOS}		Address to Output Store		30	0		
t_{WESC}		Write Enable Set-Up Time		5	15		
t_{OSSC}		Store Before Write (t_{10})		10	0		
t_{AHC}	Hold Time	Address from Clock		10	5		ns
t_{DHC}		Data from Clock		15	5		
t_{AHOS}		Address from Output Store		5	0		
t_{WEHC}		Write Enable Hold Time		15	5		

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 3: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor

IDM29705/IDM29705A 16-Word by 4-Bit Two-Port RAM/Register File

General Description

The IDM29705 and IDM29705A are 16-word by 4-bit RAM/Register File chips housed in a standard 28-pin dual-in-line package. The IDM29705 and the IDM29705A feature TRI-STATE® outputs. These RAMs, which are fabricated using SCL® (Schottky ECL Technology) feature two separate output ports that enable any two 4-bit words to be read form these outputs simultaneously. Each output port contains a four-bit latch. A common Latch Enable (LE) input is used to control all eight latches. The device, which has two Write Enable (WE) inputs, is designed so that either Write Enable ($WE_{1 \text{ or } 2}$) and Latch Enable (LE) inputs can be wired together to make the operation of the RAM appear edge-triggered.

The device, which has fully decoded A-address and B-address fields, can address any of the 16 memory words for the A-output port and, simultaneously, select any of the 16 words for presentation at the B-output port. Incoming data is written into the four-bit RAM word selected by the B-address. The D inputs are used to load the new data into the device.

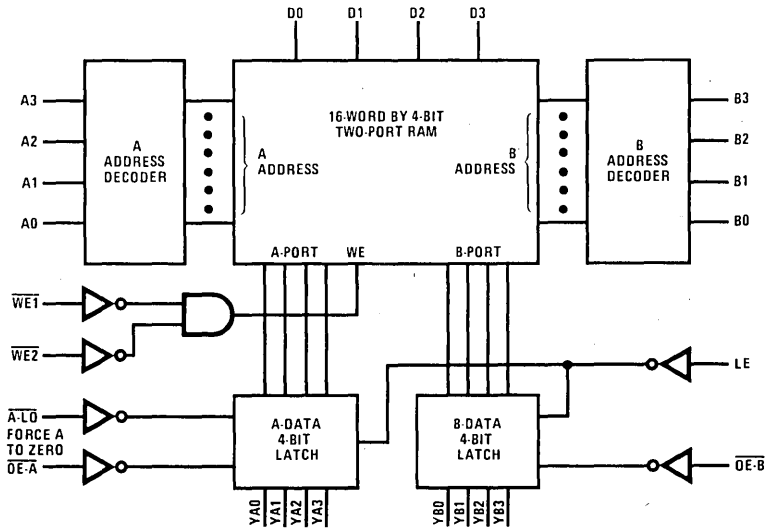
Several of these devices can be cascaded to increase the total number of memory words in the system. When $\overline{OE}$-A is high, the A-output port is in the high-impedance mode. $\overline{OE}$-B, when high, forces the B-output port to the high-impedance state.

The writing of new data into the RAM is controlled by the Write Enable inputs. With both Write Enable inputs low, data is written into the word selected by the B-address field. The memory outputs follow the data inputs during writing if the Latch Enable (LE) is high. With either Write Enable high, no data is written into the RAM.

Features and Benefits

- 16-Word by 4-Bit, 2-Port RAM/Register Files
- Two Output Ports, Each with Separate Output Control
- 4-Bit Latches on Each Output Port
- Non-Inverted Data Output with Respect to Data Input
- Output Enable and Write Enable Inputs Provide Ease in Cascading
- SCL Technology (Schottky ECL) Provides ECL Speeds While Keeping Low Power Schottky Input/Output Voltage and Power Consumption Compatibility
- 100% Reliability Testing in Compliance with MIL-STD-883

IDM29705/29705A Block Diagram



Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +6.3V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5V to +5.5V
DC Output Current, into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Operating Range

P/N	Ambient Temperature	V_{CC}
IDM29705JC	0°C to +70°C	4.75V to 5.25V
IDM29705JM, JM/883	−55°C to +125°C	4.50V to 5.50V
IDM29705AJC, NC	0°C to +70°C	4.75V to 5.25V
IDM29705AJM, JM/883	−55°C to +125°C	4.50V to 5.50V

Standard Screening (conforms to MIL-STD-883 for Class C parts)

Step	MIL-STD-883 Method	Conditions	Level	
			DC, PC	DM, FM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C: 24-hour 150°C	100%	100%
Temperature Cycle	1010	C: −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B: 10,000 G	100%	100%
Fine Leak	1014	A: 5×10^{-8} atm-cc/cm^3	100%	100%
Gross Leak	1014	C2: Fluorocarbon	100%	100%
Electrical Test Subgroups 1 and 7 and 9	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening Here for Class B Parts				
Group A Sample Tests				
Subgroup 1	5005	See below for definitions of subgroups	LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 5
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 5

Additional Screening for Class B Parts

Step	MIL-STD-883 Method	Conditions	Level
			DMB, FMB
Burn-In	1015	D: 125°C, 160 hours min	100%
Electrical Test	5004		
Subgroup 1			100%
Subgroup 2			100%
Subgroup 3			100%
Subgroup 7			100%
Subgroup 9			100%
Return to Group A Tests in Standard Screening			

Group A Subgroups

(as defined in MIL-STD-883, method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum rated temperature
3	DC	Minimum rated temperature
7	Function	25°C
8	Function	Maximum and minimum rated temperature
9	Switching	25°C
10	Switching	Maximum rated temperature
11	Switching	Minimum rated temperature

Electrical Characteristics (over operating temperature range, unless otherwise noted)

Parameter		Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage (IDM29705 only)	V_{CC} = min, V_{IN} = V_{IH} or V_{IL}	Mil, I_{OH} = −2.0mA	2.4			Volts
			Com'l, I_{OH} = −4.0mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
			I_{OL} = 12mA			0.5	
			Com'l, I_{OL} = 16mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = min, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = max, V_{IN} = 0.4V	A_i, B_i			−0.25	mA
			Others			−0.36	
I_{IH}	Input HIGH Current	V_{CC} = max, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = max, V_{IN} = 5.5V				0.1	mA
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = max, V_{IN} = V_{IH} or V_{IL}	V_o = 2.7V			20	μA
			V_o = 0.4V			−20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = max		−30		−85	mA
I_{CC}	Power Supply Current	V_{CC} = max			110	175	mA
		AJC	V_{CC} = 5.25V, T = 70°C			155	mA
		AJM	V_{CC} = 5.5V, T = 125°C			145	mA

Note 1: For conditions shown as min or max, use the appropriate value specified under Electrical Characteristics for the applicable device type.

Note 2: Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

Note 3: Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics (Input Levels = 0V and 3.0V, Transitions measured at 1.5V)

Combinational Delays (in nanoseconds) (R_L = 430Ω, C_L = 50pF)

Parameters	From	To	Conditions	Comm'l Max (Note 5)		Mil Max (Note 6)	
				705	705A	705	705A
Access Time	A Address Stable	YA Stable	LE = HIGH	50	25	55	30
	B Address Stable	YB Stable		50	25	55	30
	Both WE LOW	YA = D	LE = HIGH, A = B	45	35	48	40
		YB = D	LE = HIGH	45	35	48	40
Turn-On Time	OE-A or OE-B LOW			25	20	25	20
Turn-Off Time	OE-A or OE-B HIGH	YA or YB Off	C_L = 5pF	20	20	20	20
Reset Time	A-LO LOW	YA LOW		30	20	30	25
Enable Time	LE HIGH	YA and YB Stable		25	20	25	25
	Data In	YA or YB = D	LE = HIGH, WE both LOW, A = B	45	35	45	40

Switching Characteristics (continued)

Minimum Setup and Hold Times (in nanoseconds)

Parameters	From	To	Conditions	Typ (Note 4)	Comm'l Max (Note 5) 705	Comm'l Max (Note 5) 705A	Mil Max (Note 6) 705	Mil Max (Note 6) 705A
Data Setup Time	D Stable	Either WE HIGH		7	20	12	25	15
Data Hold Time	Either WE HIGH	D Changing		0	0	0	0	0
Address Setup Time	B Stable	Both WE LOW		0	5	0	5	3
Address Hold Time	Either WE HIGH	B Changing		0	0	0	0	0
Latch Close Before Write Begins	LE LOW	WE_1 LOW	WE_2 LOW	0	0	0	0	0
	LE LOW	WE_2 LOW	WE_1 LOW	0	0	0	0	0
Address Setup Before Latch Closes	A or B Stable	LE LOW		8	30	15	40	20

Minimum Pulse Widths (in nanoseconds)

Parameters	From	To	Conditions	Typ (Note 4)	Comm'l Max (Note 5) 705	Comm'l Max (Note 5) 705A	Mil Max (Note 6) 705	Mil Max (Note 6) 705A
Write Pulse Width	WE_1	HIGH-LOW-HIGH	WE_2 LOW	8	25	20	25	20
	WE_2	HIGH-LOW-HIGH	WE_1 LOW	8	20	20	20	20
A Latch Reset Pulse	A-LO	HIGH-LOW-HIGH		5	20	15	20	15
Latch Data Capture	LE	LOW-HIGH-LOW	Address Stable	5	20	15	20	15

Note 4: $T_A = 25°C$, $V_{CC} = 5.0V$.
Note 5: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$.
Note 6: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$.

Function Tables

Write Control

$\overline{WE_1}$	$\overline{WE_2}$	Function	RAM Outputs at Latch Inputs A-Port	RAM Outputs at Latch Inputs B-Port
L	L	Write D into B	A data ($A \neq B$)	D input data
X	H	No write	A data	B data
H	X	No write	A data	B data

YA Read

Inputs $\overline{OE\text{-}A}$	Inputs A-LO	Inputs LE	YA Output	Function
H	X	X	Z	High Impedance
L	L	X	L	Force YA LOW
L	H	H	A-Port RAM data	Latches transparent
L	H	L	NC	Latches retain data

Function Tables (continued)

YB Read

Inputs			
$\overline{OE}$-B	LE	YB Output	Function
H	X	Z	High impedance
L	H	B-Port RAM data	Latches transparent
L	L	NC	Latches retain data

H = HIGH Z = High impedance
L = LOW NC = No change
X = Don't care

Pinout Descriptions of the IDM29705/29705A

D_3-D_0: Through these inputs new data can be written in the location specified by the B-address inputs.

A_3-A_0: The 4-bit address presented at the A inputs selects one of the 16 memory words for presentation at the A-data latch outputs.

B_3-B_0: The 4-bit address presented at the B inputs selects one of the 16 memory words for presentation at the B-data latch outputs. This address also selects the location into which data is written.

YA_3-YA_0: The four A-data latch outputs.

YB_3-YB_0: The four B-data latch outputs.

$\overline{WE}_1$, $\overline{WE}_2$: Write enable inputs. When both are low, enables data to be written into the RAM location selected by the B-address field. When either Write Enable input is high, no data can be written into memory.

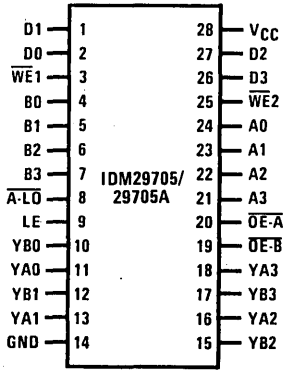
$\overline{OE}$-A: A-port output enable. When low, data in the A-data latch is present at the YA_i outputs. When high, the YA_i outputs are in the high-impedance mode.

$\overline{OE}$-B: B-port output enable. When low, data in the B-data latch is presented at the YB_i outputs. When high, the YB_i outputs are in the high-impedance mode.

LE: Latch enable. The LE input acts as control for both the RAM-A and RAM-B output ports. When high the latches are transparent and data from the RAM, as selected by the A and B address inputs, is presented at the outputs. When low, the latches retain the last data read from the RAM regardless of the current A and B address inputs.

$\overline{A\text{-}LO}$: Force A to zero. This input operates to force the A-port latch outputs low independent of the LE input or A address inputs. The A-output bus can be forced low using this control input. With $\overline{A\text{-}LO}$ high, the A latches operate in their normal manner. Once forced low, the A latches remain low independent of the $\overline{A\text{-}LO}$ input if the Latch Enable (LE) is low.

IDM29705/29705A Connections Diagram



Order Number IDM29705JC, IDM29705JM, IDM29705JM/883, IDM29705AJC, IDM29705AJM, or IDM29705JM/883
See NS Package J28A

Order Number IDM29705NC
See NS Package N28A

ECL

National Semiconductor

DM10414, DM10414A 256 x 1 ECL Random Access Memory

General Description

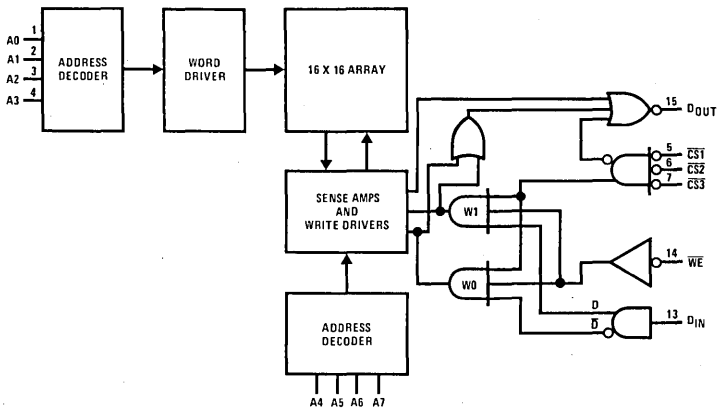
The DM10414, DM10414A is a 256-word by 1-bit ECL random access memory. The fully static memory is designed with active low chip selects and separate I/O pins. The 8 address bits (A0 through A7) are fully decoded on the chip. Applications such as scratch pad, cache, and buffer memories are ideal for this high speed RAM.

An unterminated emitter-follower output is provided to allow the outputs to be wire-ORed. Separate Data In and non-inverted Data Out pins are provided. These RAMs are compatible with compensated and uncompensated 10k ECL families.

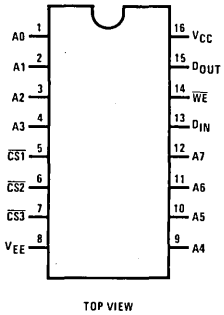
Features

- Fully compatible with standard and voltage compensated 10k series ECL
- Temperature range 0°C to +75°C
- Unterminated emitter-follower output for wire-ORing
- Power dissipation decreases with increasing temperature
- Typical address access
  - DM10414 10 ns
  - DM10414A 7 ns
- Typical chip select access
  - DM10414 4 ns
  - DM10414A 3 ns

Block and Connection Diagrams



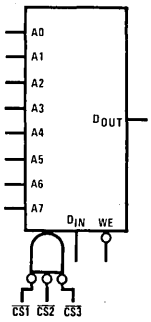
Dual-In-Line Package



TOP VIEW

Order Number DM10414J
or DM10414AJ
See NS Package J16A

Logic Symbol



Pin Names

A0–A7	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$	Chip Select Inputs
$\overline{WE}$	Write Enable

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	MODE
H	X	X	L	Not Selected
L	L	H	L	Write 1
L	L	L	L	Write 0
L	H	X	D_{OUT}	Read

L = low (−1.7V nominal)
H = high (−0.9V nominal)
X = don't care

Absolute Maximum Ratings

Temperature Under Bias (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
V_{EE} Relative to V_{CC}	−7.0V to +0.5V
Any Input Relative to V_{CC}	V_{EE} to +0.5V
Output Current (Output High)	−30 mA to +0.1 mA
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{EE})	−5.72	−4.68	V
Ambient Temperature (T_A)	0	+75	°C

DC Electrical Characteristics

V_{EE} = −5.2V ±10%, Output Load = 50Ω and 30 pF to −2.0V, T_A = 0°C to +75°C (Notes 1–4)

SYMBOL	PARAMETER	CONDITIONS	T_A	B LIMIT	A LIMIT	UNITS
V_{OH}	Output Voltage High	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	−1000	−840	mV
			+25°C	−960	−810	
			+75°C	−900	−720	
V_{OL}	Output Voltage Low	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	−1870	−1665	mV
			+25°C	−1850	−1650	
			+75°C	−1830	−1625	
V_{OHC}	Output Voltage High	$V_{IN} = V_{IHB}$ or V_{ILA} Performed on one input at a time	0°C	−1020		mV
			+25°C	−980		
			+75°C	−920		
V_{OLC}	Output Voltage Low	$V_{IN} = V_{IHB}$ or V_{ILA} Performed on one input at a time	0°C		−1645	mV
			+25°C		−1630	
			+75°C		−1605	
V_{IH}	Input Voltage High	Guaranteed Input Voltage High for All Inputs	0°C	−1145	−840	mV
			+25°C	−1105	−810	
			+75°C	−1045	−720	
V_{IL}	Input Voltage Low	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	−1490	mV
			+25°C	−1850	−1475	
			+75°C	−1830	−1450	
I_{IH}	Input Current High	$V_{IN} = V_{IHA}$ Performed on one input at a time	0°C to +75°C		220	μA
I_{IL}	Input Current Low, $\overline{CS}$	$V_{IN} = V_{ILB}$ Performed on one input at a time	+25°C	0.5	170	μA
	All Others		+25°C	−50		
I_{EE}	Power Supply Current (Pin 8) (Note 5)	All Inputs and Outputs Open	0°C	−150		mA

Note 1: Conditions for testing not shown in the tables are chosen to guarantee operation under "worst case" conditions.

Note 2: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 3: Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical resistance values of the package are: θ_{JA}, (Junction to Ambient) = 90°C/W (still air); θ_{JA} (Junction to Ambient) = 50°C/W (at 400 F.P.M. air flow); θ_{JA} (Junction to Case) = 25°C/W.

Note 4: "A" indicates the most positive value, "B" indicates the most negative value.

Note 5: Typical values at V_{EE} = −5.2V: T_A = 0°C, I_{EE} = −105 mA; T_A = 75°C, I_{EE} = −90 mA.

Functional Description

Addressing the DM10414, DM10414A is achieved by means of the 8 address lines A0–A7. Each of the 2^8 one-zero combinations of the address lines corresponds to a bit location in the memory. The active low Chip Selects together with the unterminated emitter-follower output allows for wire-ORing. A 50Ω resistor to −2V (or an equivalent network) is required to provide a low at the output when the device is off. This termination is required for both single device or wire-ORed operation.

The device is selected with $\overline{CS}$ low and deselected with $\overline{CS}$ high. The operating mode is controlled by the active low Write Enable ($\overline{WE}$). $\overline{WE}$ low causes the data at the Data Input (D_{IN}) to be stored at the selected address. $\overline{WE}$ low also causes the output to be disabled (low due to the 50Ω pull-down resistor). $\overline{WE}$ high causes the data stored at the selected address to be present at the Data Out (D_{OUT}) pin.

AC Electrical Characteristics

V_{EE} = −5.2V ±10%, Output Load = 50Ω, 30 pF to −2.0V, T_A = 0°C to 75°C

SYMBOL	PARAMETER	CONDITIONS	DM10414A			DM10414			UNITS
			MIN	TYP (NOTE 6)	MAX	MIN	TYP (NOTE 6)	MAX	
READ MODE									
t_{ACS}	Chip Select Access Time	Measured Between 50% Points (Note 7)		3	5		4	7	ns
t_{RCS}	Chip Select Recovery Time			3	5		4	7	ns
t_{AA}	Address Access Time			7	10		10	15	ns
WRITE MODE									
t_W	Write Pulse Width (to Guarantee Writing)	Measured Between 50% Points	6	3.5		8	5		ns
t_{WSD}	Data Set-Up Time Prior to Write		2	0		2	0		ns
t_{WHD}	Data Hold Time After Write		2	0		2	0		ns
t_{WSA}	Address Set-Up Time Prior to Write		3	0		4	0		ns
t_{WHA}	Address Hold Time After Write		2	0		3	1		ns
t_{WSCS}	Chip Select Set-Up Time Prior to Write		2	0		2	0		ns
t_{WHCS}	Chip Select Hold Time After Write		2	0		2	0		ns
t_{WS}	Write Disable Time		5	3		7	4		ns
t_{WR}	Write Recovery Time		5	3		7	4		ns
RISE TIME AND FALL TIME									
t_r	Output Rise Time	Measured Between 50% Points		3			4		ns
t_f	Output Fall Time			3			4		ns

Capacitance

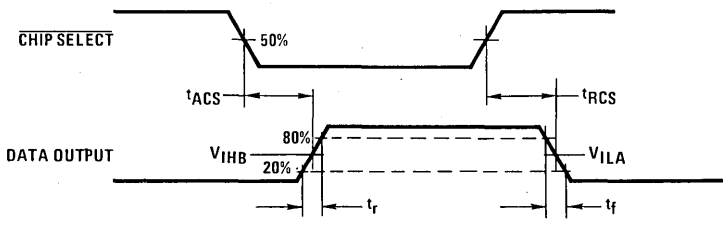
SYMBOL	PARAMETER	CONDITIONS	DM10414A			DM10414			UNITS
			MIN	TYP (NOTE 6)	MAX	MIN	TYP (NOTE 6)	MAX	
C_{IN}	Input Pin Capacitance	Measure With a Pulse Technique		4	5		4	5	pF
C_{OUT}	Output Pin Capacitance			7	8		7	8	pF

Note 6: Typical values are at V_{EE} = −5.2V, T_A = 25°C and maximum loading.

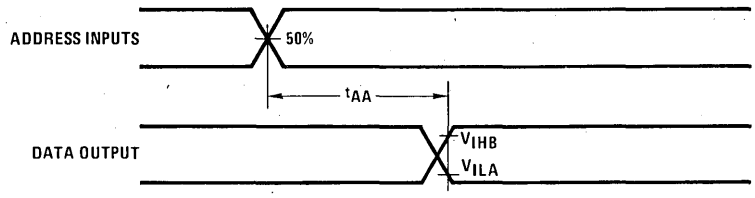
Note 7: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Switching Time Waveforms

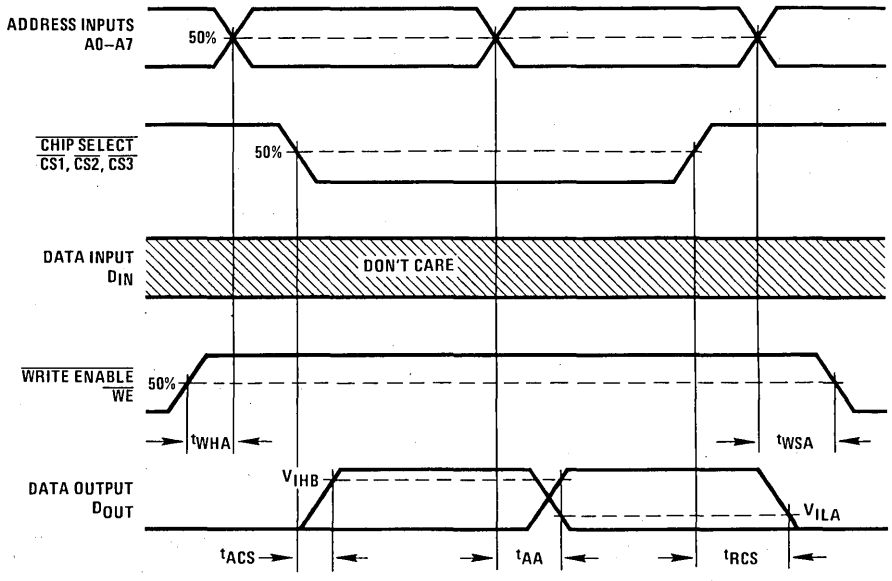
Chip Select Access Time



Address Access Time

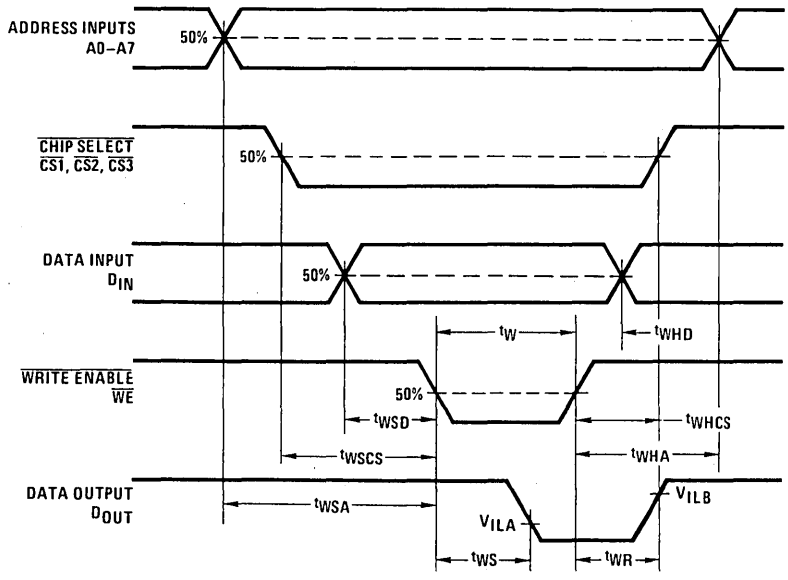


Read Mode



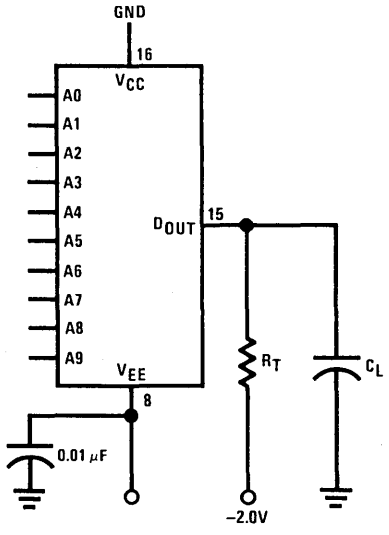
Switching Time Waveforms (Continued)

Write Mode

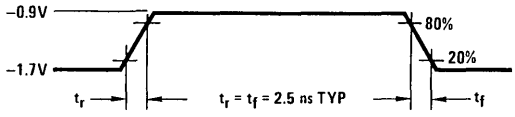


Test Conditions

Loading Conditions



Input Levels



All timing measurements referenced to 50% of input levels
C_L = 10 pF including jig and stray capacitance
R_T = 50Ω

National Semiconductor

DM10415, DM10415A 1024 x 1 ECL Random Access Memory

General Description

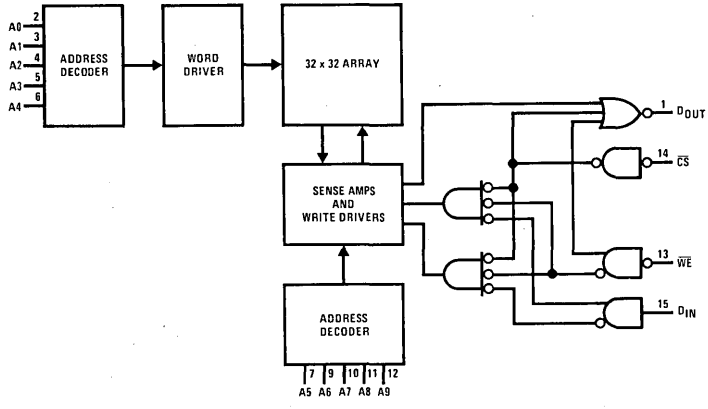
The DM10415, DM10415A is a 1024-word by 1-bit ECL random access memory. This fully static memory is designed with an active low chip select and separate I/O pins. The 10 address bits (A0 through A9) are fully decoded on the chip. Applications such as scratch pad, cache, and buffer memories are ideal for this high speed RAM.

An unterminated emitter-follower output is provided to allow the outputs to be wire-ORed. Separate Data In and non-inverted Data Out pins are provided. These RAMs are compatible with compensated and uncompensated 10k ECL families.

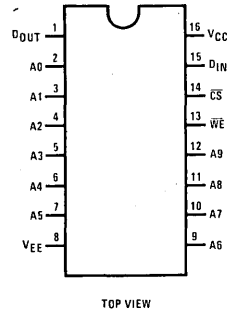
Features

- Fully compatible with standard and voltage compensated 10k series ECL
- Temperature range 0°C to +75°C
- Unterminated emitter-follower output for wire-ORing
- Power dissipation decreases with increasing temperature
- Typical address access
  - DM10415 25 ns
  - DM10415A 12 ns
- Typical chip select access
  - DM10415 7 ns
  - DM10415A 4 ns

Block and Connection Diagrams



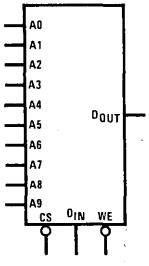
Dual-In-Line Package



TOP VIEW

Order Number DM10415J or DM10415AJ
See NS Package J16A

Logic Symbol



Pin Names

A0–A9	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	MODE
H	X	X	L	Not Selected
L	L	H	L	Write 1
L	L	L	L	Write 0
L	H	X	D_{OUT}	Read

L = low (−1.7V nominal)
H = high (−0.9V nominal)
X = don't care

Absolute Maximum Ratings

Temperature Under Bias (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
V_{EE} Relative to V_{CC}	−7.0V to +0.5V
Any Input Relative to V_{CC}	V_{EE} to +0.5V
Output Current (Output High)	−30 mA to +0.1 mA
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{EE})	−5.46	−4.94	V
Ambient Temperature (T_A)	0	+75	°C

DC Electrical Characteristics

V_{EE} = −5.2V, Output Load = 50Ω and 30 pF to −2.0V, T_A = 0°C to +75°C (Notes 1 − 4)

SYMBOL	PARAMETER	CONDITIONS	T_A	B LIMIT	A LIMIT	UNITS
V_{OH}	Output Voltage High	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C +25°C +75°C	−1000 −960 −900	−840 −810 −720	mV
V_{OL}	Output Voltage Low	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C +25°C +75°C	−1870 −1850 −1830	−1665 −1650 −1625	mV
V_{OHC}	Output Voltage High	$V_{IN} = V_{IHB}$ or V_{ILA}	0°C +25°C +75°C	−1020 −980 −920		mV
V_{OLC}	Output Voltage Low	$V_{IN} = V_{IHB}$ or V_{ILA}	0°C +25°C +75°C		−1645 −1630 −1605	mV
V_{IH}	Input Voltage High	Guaranteed Input Voltage High for All Inputs	0°C +25°C +75°C	−1145 −1105 −1045	−840 −810 −720	mV
V_{IL}	Input Voltage Low	Guaranteed Input Voltage Low for All Inputs	0°C +25°C +75°C	−1870 −1850 −1830	−1490 −1475 −1450	mV
I_{IH}	Input Current High	$V_{IN} = V_{IHA}$	0°C to +75°C		220	μA
I_{IL}	Input Current Low, $\overline{CS}$ All Others	$V_{IN} = V_{ILB}$	+25°C +25°C	0.5 −50	170	μA
I_{EE}	Power Supply Current (Pin 8) (Note 5)	All Inputs and Outputs Open	0°C	−150		mA

Note 1: Conditions for testing not shown in the tables are chosen to guarantee operation under "worst case" conditions.

Note 2: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 3: Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical resistance values of the package are: θ_{JA} (Junction to Ambient) = 90°C/W (still air); θ_{JA} (Junction to Ambient) = 50°C/W (at 400 F.P.M. air flow); θ_{JA} (Junction to Case) = 25°C/W.

Note 4: "A" indicates the most positive value, "B" indicates the most negative value.

Note 5: Typical values at V_{EE} = −5.2V: T_A = 0°C, I_{EE} = −105 mA; T_A = 75°C, I_{EE} = −90 mA.

Functional Description

Addressing the DM10415/DM10415A is achieved by means of the 10 address lines A0–A9. Each of the 2^{10} one-zero combinations of the address lines corresponds to a bit location in the memory. The active low Chip Select ($\overline{CS}$) together with the unterminated emitter-follower output allows for memory array expansion to 2048 words without additional decoding. This emitter-follower output allows for wire-ORing. A 50Ω resistor to −2V (or an equivalent network) is required to provide a low at the output when the device is off. This termination is required for both single device or wire-ORed operation.

The device is selected with $\overline{CS}$ low and deselected with $\overline{CS}$ high. The operating mode is controlled by the active low Write Enable ($\overline{WE}$). $\overline{WE}$ low causes the data at the Data Input (D_{IN}) to be stored at the selected address. $\overline{WE}$ low also causes the output to be disabled (low due to the 50Ω pull-down resistor). $\overline{WE}$ high causes the data stored at the selected address to be present at the Data Out (D_{OUT}) pin.

AC Electrical Characteristics

V_{EE} = −5.2V ±5%, Output Load = 50Ω, 30 pF to −2.0V, T_A = 0°C to +75°C

SYMBOL	PARAMETER	CONDITIONS	DM10415A			DM10415			UNITS
			MIN	TYP (NOTE 6)	MAX	MIN	TYP (NOTE 6)	MAX	
READ MODE									
t_{ACS}	Chip Select Access Time	Measured at 50% of Input to Valid Output (Note 7)		4			7	10	ns
t_{RCS}	Chip Select Recovery Time			4			7	10	ns
t_{AA}	Address Access Time			12	20		25	35	ns
WRITE MODE									
t_W	Write Pulse Width (to Guarantee Writing)								
	DM10415A	t_{WSA} = 8 ns	12	10		25	20		ns
	DM10415	t_{WSA} = 20 ns							
t_{WSD}	Data Set-Up Time Prior to Write			0		5	0		ns
t_{WHD}	Data Hold Time After Write			0		5	0		ns
t_{WSA}	Address Set-Up Time Prior to Write								
	DM10415A	t_W = 12 ns		5		8	5		ns
	DM10415	t_W = 25 ns							
t_{WHA}	Address Hold Time After Write			0		4	1		ns
t_{WSCS}	Chip Select Set-Up Time Prior to Write			0		5	0		ns
t_{WHCS}	Chip Select Hold Time After Write			0		5	0		ns
t_{WS}	Write Disable Time			4			7	10	ns
t_{WR}	Write Recovery Time			4			7	10	ns
RISE TIME AND FALL TIME									
t_r	Output Rise Time	Measured Between 20% and 80% Points		5			5		ns
t_f	Output Fall Time			5			5		ns

Capacitance

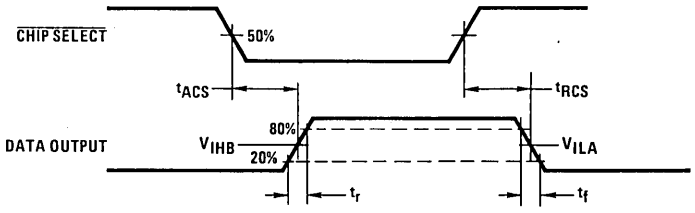
SYMBOL	PARAMETER	CONDITIONS	DM10415A			DM10415			UNITS
			MIN	TYP (NOTE 6)	MAX	MIN	TYP (NOTE 6)	MAX	
C_{IN}	Input Pin Capacitance	Measure With a Pulse Technique		4	5		4	5	pF
C_{OUT}	Output Pin Capacitance			7	8		7	8	pF

Note 6: Typical values are at V_{EE} = −5.2V, T_A = 25°C and maxumum loading.

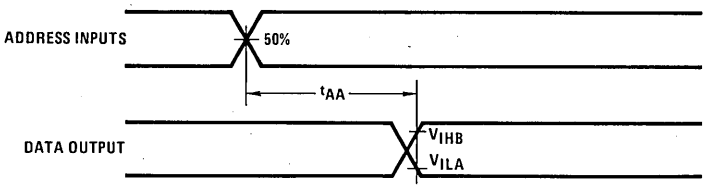
Note 7: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Switching Time Waveforms

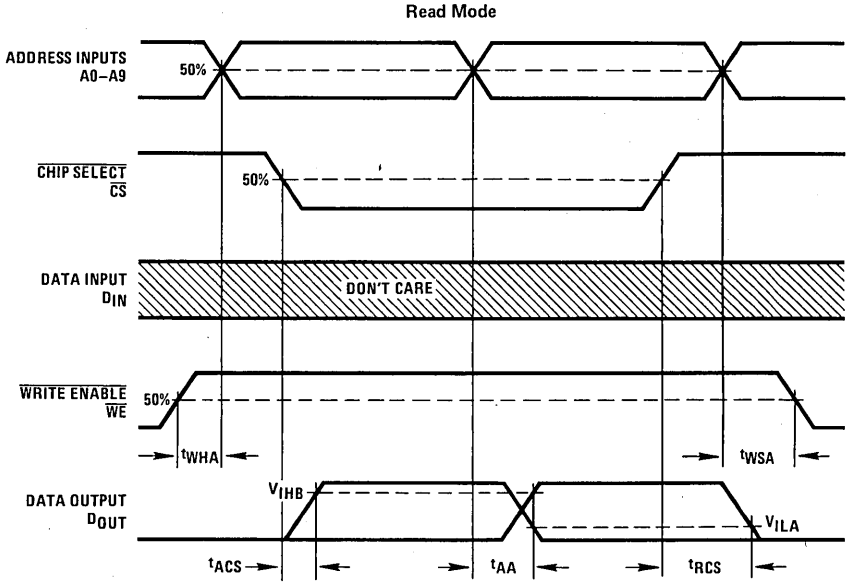
Chip Select Access Time



Address Access Time

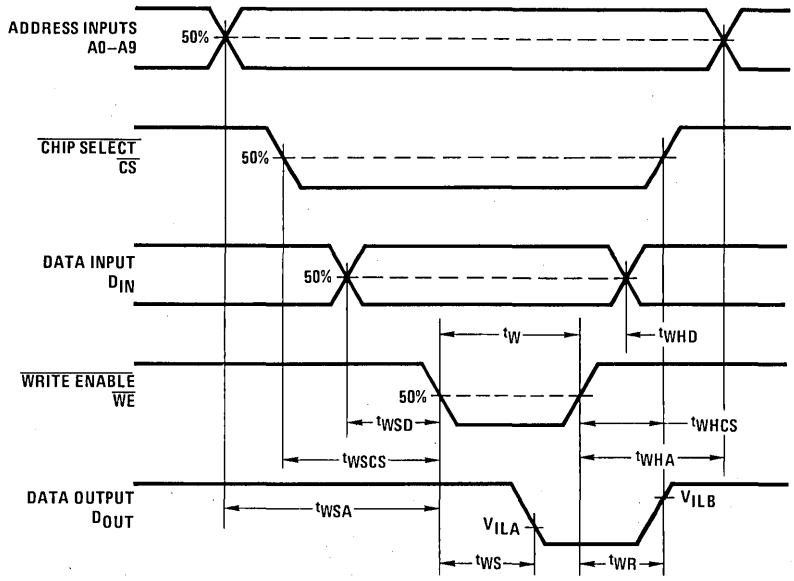


Read Mode



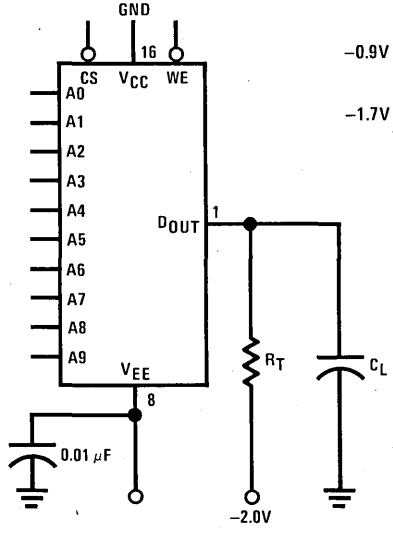
Switching Time Waveforms (Continued)

Write Mode

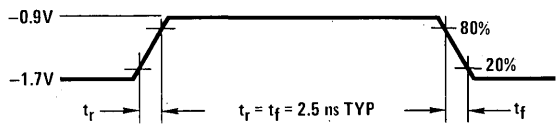


Test Conditions

Loading Conditions



Input Levels



All timing measurements referenced to 50% of input levels
C_L = 30 pF including jig and stray capacitance
R_T = 50Ω

National Semiconductor

Bipolar RAMs
PREVIEW

DM10422 1024-Bit (256 x 4) ECL RAM

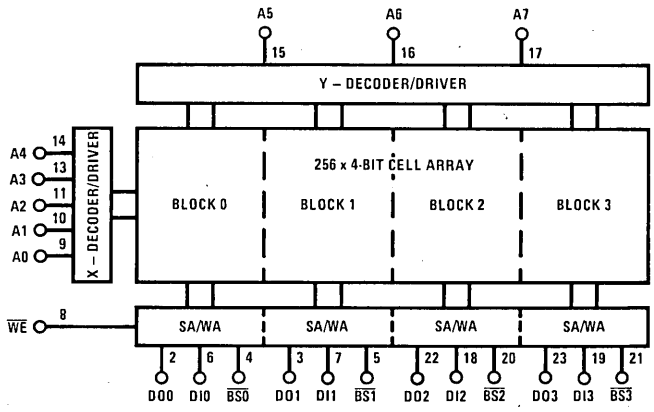
General Description

The DM10422 is normally a 256-word by 4-bit random access memory. However the memory has four Block Select (BS0-BS3) inputs which allow "WIRE OR" of any of the four blocks for a maximum 1024-word by 1-bit memory. The high speed access time allows its use in scratch pad, buffer, and control storage applications. The device is voltage compensated and is compatible with all 10K logic. Separate Data In and Data Out pins allow the set up of data for a write cycle while performing a read.

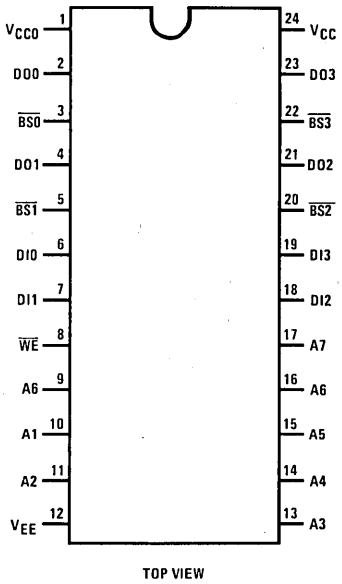
Features

- 4 separate Block Select inputs for from 256 x 4 to 1024 x 1 configuration
- Typical address access time—12 ns
- Block Select access time—4 ns
- 10k logic compatible

Block and Connection Diagrams

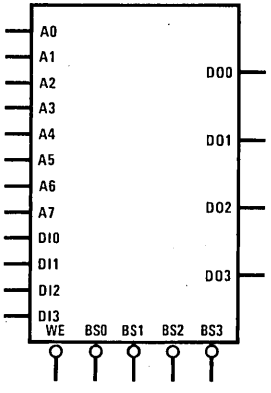


Dual-In-Line Package



TOP VIEW

Logic Symbol



Pin Names

$\overline{BS0}$-$\overline{BS3}$	Block Selects
A0-A7	Address Inputs
$\overline{WE}$	Write Enable
DI0-DI3	Data Inputs
DO0-DO3	Data Outputs

Truth Table (Positive Logic)

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	DI		
H	X	X	L	Disable
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	DO	Read

National Semiconductor

Bipolar RAMs
PREVIEW

DM10470 4096-Bit (4096 x 1) ECL RAM

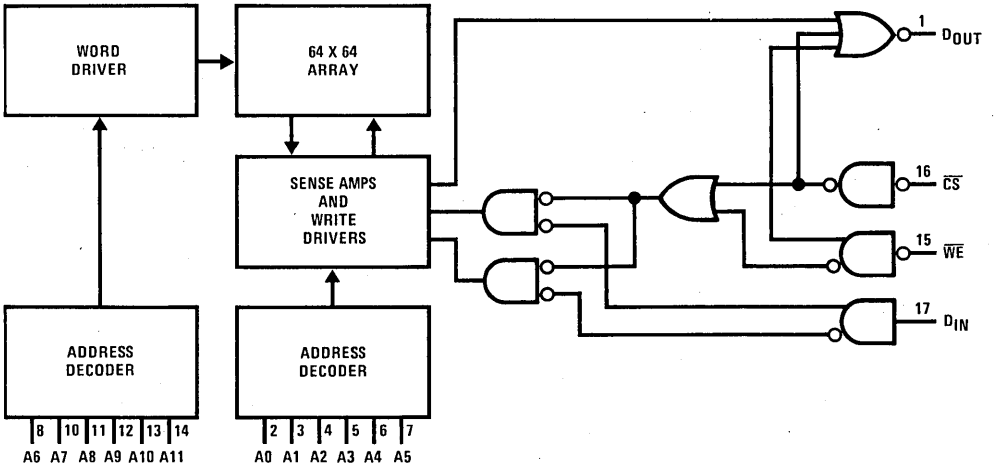
General Description

The DM100470 is a 4096-bit random access memory organized 4096-words by 1-bit. It is designed for high speed scratch pad and buffer storage applications. It is voltage and temperature compensated and compatible with all 100k logic. It has separate Data In and Data Out pins. The active low Chip Select $\overline{CS}$ and open emitter outputs allow easy expansion.

Features

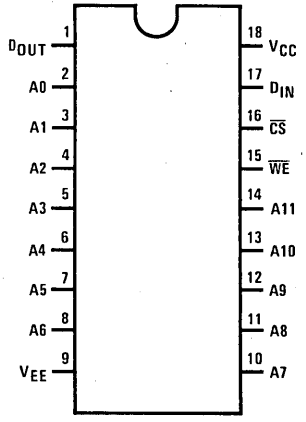
- Typical address access time—18 ns
- Typical Chip Select access time—10 ns
- 100K logic compatible
- Open emitter outputs
- Power dissipation—0.25 mW/bit

Logic Diagram



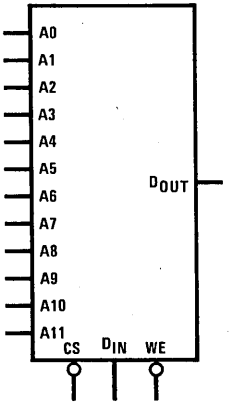
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Symbol



Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	Open Emitter	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

Pin Names

$\overline{CS}$	Chip Select Inputs
A0-A11	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

National Semiconductor

Bipolar RAMs
PREVIEW

DM100414 256-Bit (256 x 1) ECL RAM

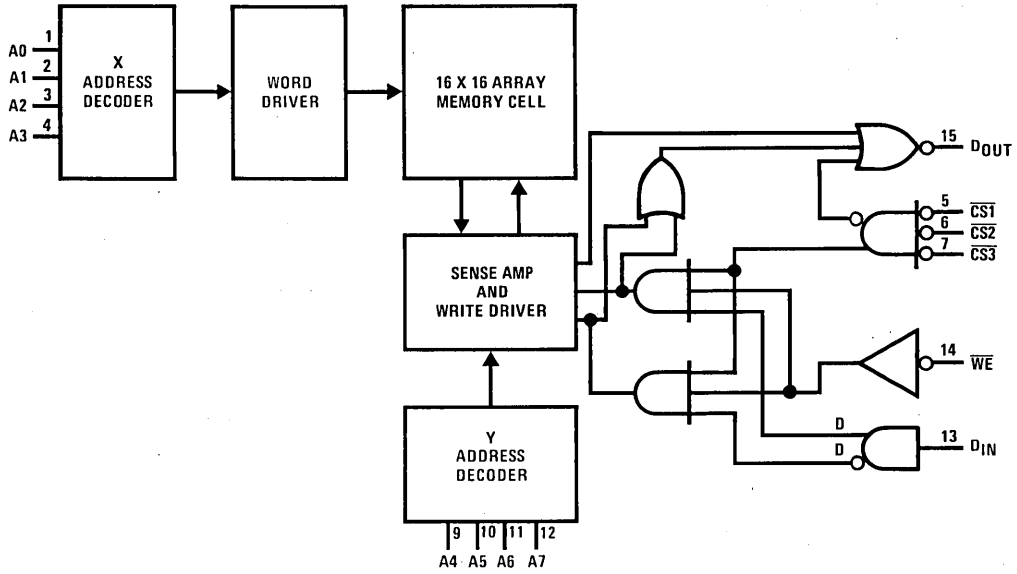
General Description

The DM100414 is a 256-bit random access memory, organized 256-words by 1-bit. It is designed for high speed scratch pads, control and buffer storage applications. The device has three chip selects (CS1-CS3) and separate Data In and Data Out pins. The open emitter output allows "OR" tying for easy expansion. It is both voltage and temperature compensated to be compatible with all 100k logic.

Features

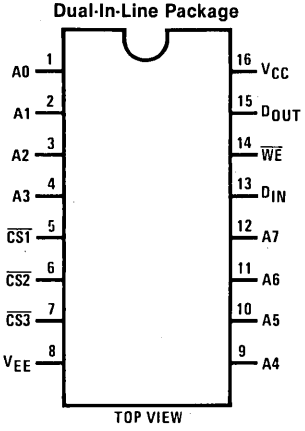
- Typical address access time—7 ns
- Typical chip select time—4 ns
- 50 kΩ pull-down resistors
- Open emitter outputs

Logic Diagram

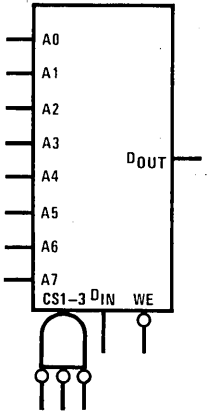


Connection Diagram

Dual-In-Line Package



Logic Symbol



Truth Table

Input					Output	Mode
$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{WE}$	D_{IN}		
X	X	H*	X	X	L	Not Selected
L	L	L	L	L	L	Write "0"
L	L	L	L	H	L	Write "1"
L	L	L	H	X	D_{OUT}	Read

*One or more Chip Selects HIGH

Pin Names

$\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$	Chip Select Inputs
A0-A7	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input

National Semiconductor

Bipolar RAMs
PREVIEW

DM100415 1024 x 1 ECL RAM

General Description

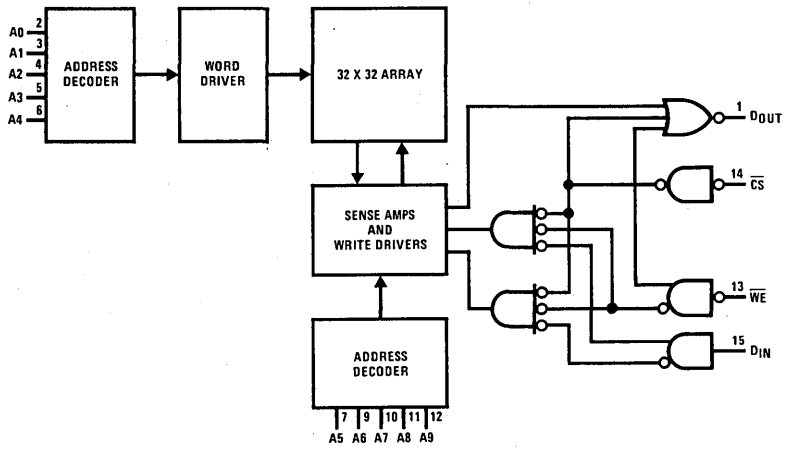
The DM100415 is a 1024-word by 1-bit ECL random access memory. This fully static memory is designed with an active low chip select and separate I/O pins. The 10 address bits (A0 through A9) are fully decoded on the chip. Applications such as scratch pad, cache, and buffer memories are ideal for this high speed RAM.

An unterminated emitter-follower output is provided to allow the outputs to be wire-ORed. Separate Data In and non-inverted Data Out pins are provided. These RAMs are compatible with all 100k logic.

Features

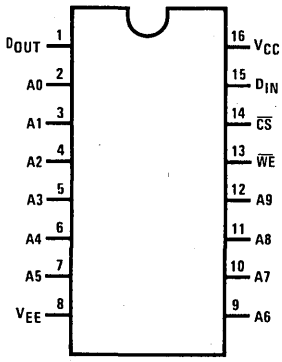
- Fully compatible with standard 100k logic
- Temperature range—0°C to +85°C
- Unterminated emitter-follower output—full wire-ORing
- Power dissipation decreases with increasing temperature
- Typical address access—12 ns
- Typical chip select access—5 ns

Block Diagram



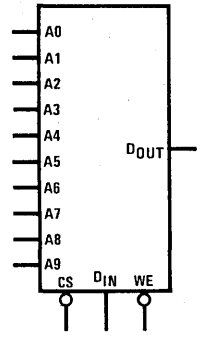
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Symbol



Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Mode
H	X	X	L	Not Selected
L	L	H	L	Write "1"
L	L	L	L	Write "0"
L	H	X	D_{OUT}	Read

L = low (−1.7V nominal)
H = high (−0.9V nominal)
X = don't care

Pin Description

A0-A9	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable

National Semiconductor

Bipolar RAMs
PREVIEW

DM100422 1024-Bit (256 x 4) ECL RAM

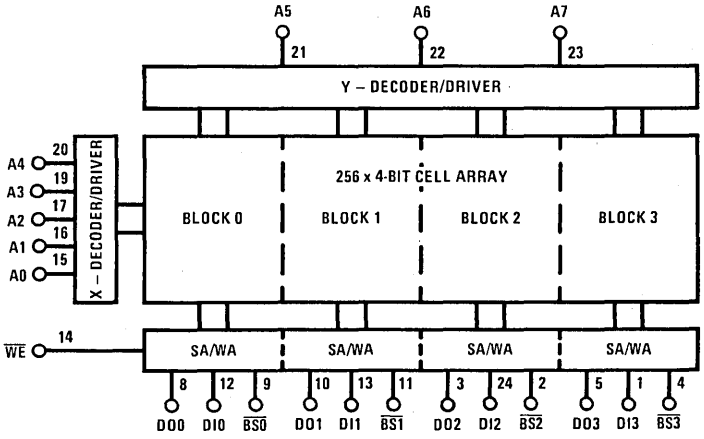
General Description

The DM100422 is normally a 256-word by 4-bit random access memory. However the memory has four Block Select (BS0-BS3) inputs which allow "wire-OR" of any of the four blocks for a maximum 1024-word by 1-bit memory. The high speed access time allows its use in scratch pad, buffer, and control storage application. The device is both voltage and temperature compensated and is compatible with all 100k logic. Separate Data In and Data Out pins allow the set up of data for a write cycle while performing a read.

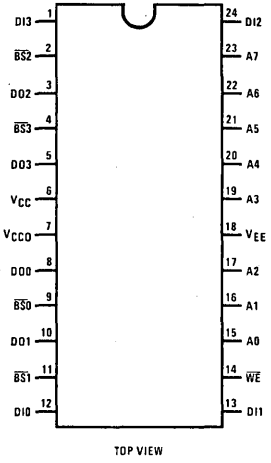
Features

- 4 separate Block Select inputs for 256 x 4 to 1024 x 1 configuration
- Typical address access time—10 ns
- Block Select access time—3 ns
- 100k logic compatible

Logic and Connection Diagrams

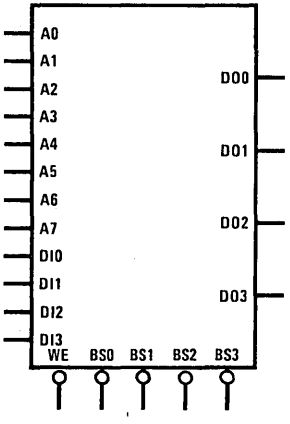


Dual-In-Line Package



TOP VIEW

Logic Symbol



Truth Table (Positive Logic)

$\overline{BS}$	Input $\overline{WE}$	DI	Output	Mode
H	X	X	L	Disable
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	DO	Read

Pin Names

$\overline{BS0}$-$\overline{BS3}$	Block Select
A0-A7	Address Inputs
$\overline{WE}$	Write Enable
DI0-DI3	Data Inputs
DO0-DO3	Data Outputs

National Semiconductor

Bipolar RAMs
PREVIEW

DM100470 4096-Bit (4096 x 1) ECL RAM

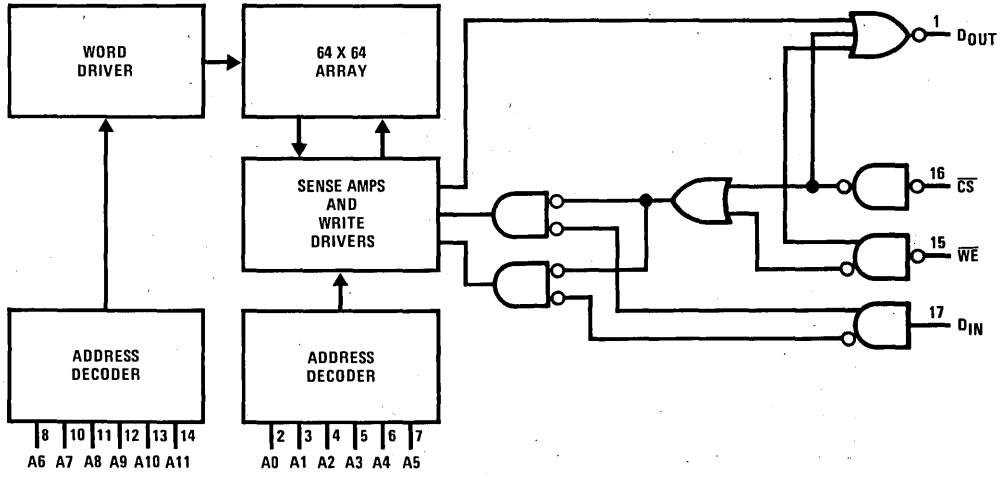
General Description

The DM10470 is a 4096-bit random access memory organized 4096-words by 1-bit. It is designed for high speed scratch pads and buffer storage applications. It is voltage compensated for high noise immunity and compatible with all 10k series logic. It has separate Data In and Data Out pins. The active low Chip Select $\overline{CS}$ and open emitter outputs allow easy expansion.

Features

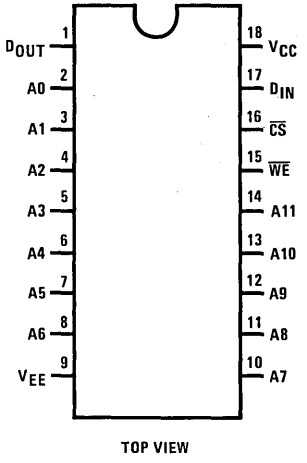
- Typical address access time—30 ns
- Typical Chip Select access time—10 ns
- 10k logic compatible
- Open emitter outputs
- Power dissipation—0.25 mW/bit

Block Diagram



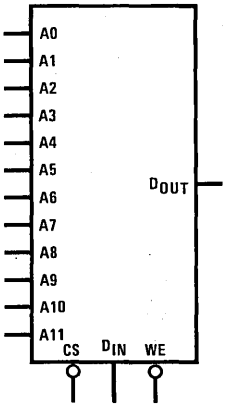
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Symbol



Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	Open Emitter	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

Pin Names

$\overline{CS}$	Chip Select Inputs
A0-A11	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

Section 4
Magnetic Bubble Memories

4

Magnetic domain memories, provide the highest density of the extant memory technologies. The inherent simplicity in processing and lack of "charged" elements promise high reliability not found in traditional memory technologies. The high density also affords low cost. The non-volatility of bubble memories make them especially suited for portable applications and remote terminals. The solid state nature offers higher reliability and lower maintenance costs than moving medium technologies. Support circuits permitting easy design into any host system are also shown in the section.

National Semiconductor

Magnetic Bubble Memories
PREVIEW

DS3615 Bubble Memory Function Driver

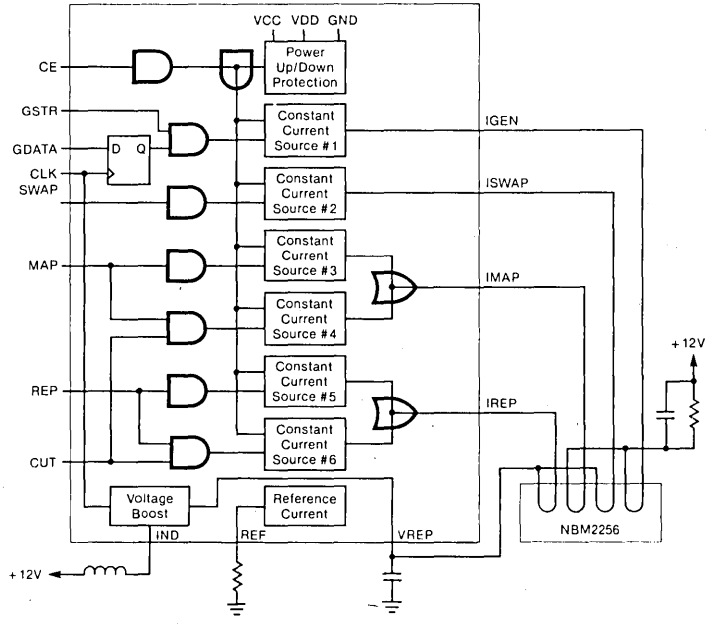
General Description

The DS3615 is a function driver that converts digital TTL level pulses generated by a timing circuit into the current pulses required by National's NBM2256 256K-bit magnetic bubble memory. The DS3615 consists of input logic gates that are TTL compatible, a D flip-flop, a voltage boost circuit, and six current generators. The current generators deliver constant currents for driving the swap gate, generator element, map gate, and replicator gate of the magnetic bubble memory. Operation is from 0°C to 70°C.

Features

- TTL compatible inputs
- Operates from two standard supplies: +5V, +12V
- PNP inputs minimize loading
- Built-in voltage boost circuitry—does not require an extra voltage supply
- Power up/down glitch-free protection for both supplies

DS3615 Functional Block Diagram



National Semiconductor

DS3616 Bubble Memory Coil Driver

General Description

A, B, C, and HLD-EN are TTL compatible low current inputs to insure easy interfacing to MOS controller circuits. Internal logic controls the output sinking and sourcing transistors to drive the X and Y bubble memory coils in a diode bridged push-pull configuration.

Sourcing transistors are driven into saturation by the on-chip voltage booster for maximum current drive to the coil.

An internal power up/down control circuit prevents glitches and noise on the outputs during system initialization.

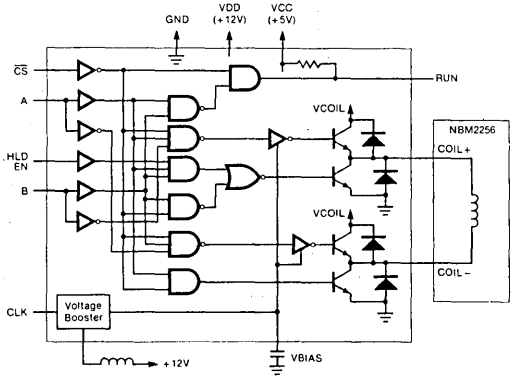
$\overline{CS}$ enables the output drive transistors. The RUN output is used to disable function drivers during power up/down.

The DS3616 is characterized to operate from 0°C to 70°C.

Features

- Two high-current push-pull outputs
- TTL compatible low current inputs
- Two power supplies: +5V and +12V
- Internal clamp diodes
- Power up/down control circuit
- Optional internal voltage booster
- RUN output for function driver control

DS3616 Functional Block Diagram



DS3617 Bubble Memory Sense Amplifier

General Description

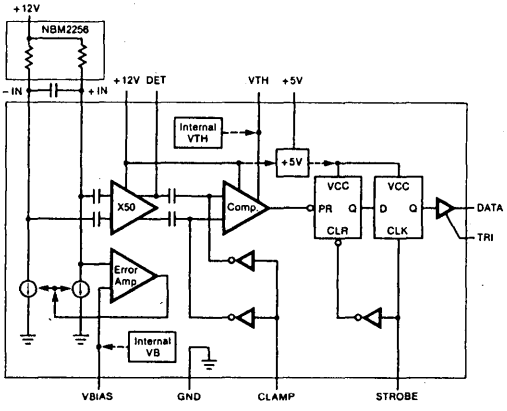
The DS3617 is a bubble memory sense amplifier that converts low level signals from the magneto-resistive detector of a bubble memory into TTL compatible output levels. Internal functions consist of an input bias circuit, an internally AC coupled amplifier, a high-speed precision comparator, two flip-flops and a TRI-STATE® output stage.

TTL compatible control inputs allow either average-to-peak or clamp and strobe (peak-to-peak) sensing of the input signal. The threshold voltage and the input bias voltage are externally adjustable, allowing compatibility with different types of bubble memories. Operation is specified from 0°C to 70°C.

Features

- +5V and +12V supply operation
- On-chip adjustable detector bias circuit
- Choice of average-to-peak or clamp and strobe sensing
- Guaranteed tight threshold limits over the specified temperature and supply voltage range
- Threshold externally adjustable over 0mV to 10mV range
- High threshold voltage sensitivity
- TRI-STATE® output
- Compatible with a wide range of bubble memories
- Standard 16-pin DIP

DS3617 Functional Block Diagram



National Semiconductor

Magnetic Bubble Memories
PREVIEW

INS82851 Bubble Memory Controller

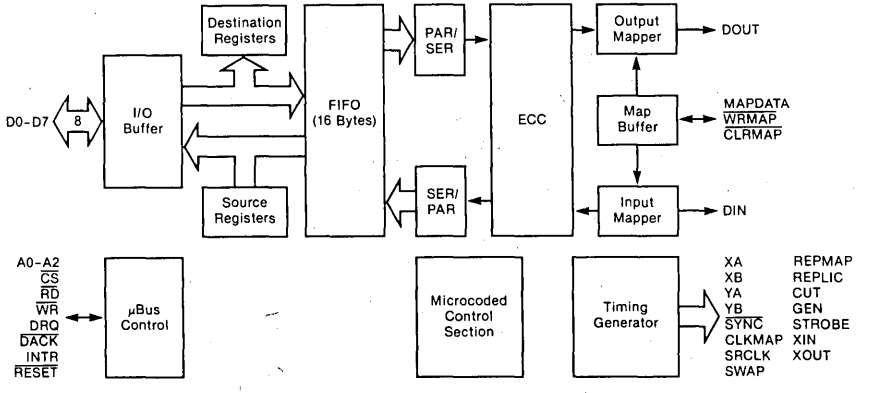
General Description

The INS82851 is an NMOS controller specifically programmed for use with National Semiconductor's NBM2256 256K-bit magnetic bubble memory. The controller provides all the system control needed for a single NBM2256 module, and with the addition of a few TTL parts can control 2, 4 or 8 modules. Among the functions provided are power up/down sequencing, error map bootstrap, address initialization, address conversion and cycle counting for data read/write, redundant bit insertion/deletion, error detection and correction, FIFO buffering, timing generator for interface circuits, and data transfer signals for DMA, interrupt or software polling. Operation is from 0°C to 70°C.

Features

- Controls 1, 2, 4 or 8 NBM2256 modules
- MICROBUS™ interface for microprocessor applications
- DMA, interrupt or polled transfer signals
- Provides complete timing generation for interface circuits
- Redundancy insertion/deletion
- FIFO buffering
- Error detection/correction
- 40-pin DIP, +5V supply

INS82851 Controller



INS82851

National Semiconductor

Magnetic Bubble Memories
PREVIEW

NBM2256 Bubble Memory

General Description

National Semiconductor's NBM2256 is a low cost, non-volatile, highly reliable solid state memory that uses magnetic bubble technology. The NBM2256 has the form of a dual-in-line package complete with the required in-plane rotating field coils and permanent magnet bias structure.

The package has a magnetic shield around it to protect the data from externally induced magnetic fields. The magnetic materials are so chosen that data integrity is guaranteed over a wide temperature range.

The NBM2256 memory module has a nominal* capacity of 256k bits organized as 256 storage loops each having 1024 storage locations. The storage loops have an input track with a swap gate on one side and an output track with a replicate gate on the other. The input track is serviced by a generator and the output track leads into a sensing area where bubbles are stretched to produce a signal large enough to be discriminated reliably using standard electronic circuitry.

In addition to storage area there is one more storage loop which can be used for the purpose of storing defective loop information and/or the address reference locations.

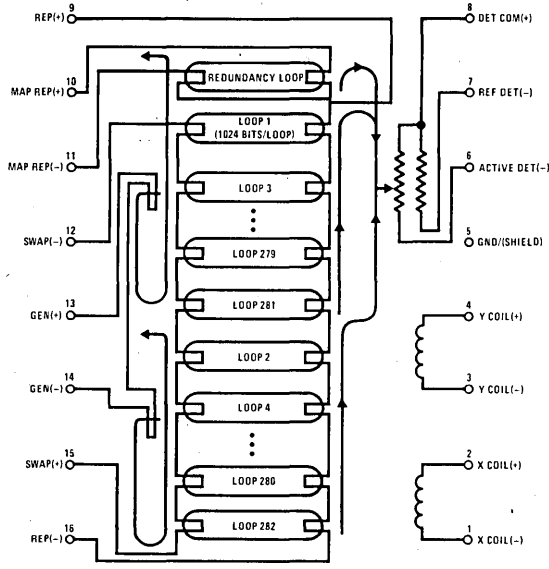
The NBM2256 Bubble Memory can operate asynchronously up to its maximum operating frequency, can be started and stopped at will and does not lose data when power is disconnected.

*A usable number; physically there are more loops to impart defect tolerancy.

Features

- ☐ Solid State
- ☐ Non-Volatile
- ☐ High Density
- ☐ Low Power
- ☐ Redundant Storage Loops
- ☐ Page-Oriented Access
- ☐ Sequential Read/Write
- ☐ Start/Stop Capability
- ☐ Modular Capacity
- ☐ On-Chip Error Map

Chip Organization



4

General Specifications

Capacity	256K bits
Bubble Size	$\leq 3\mu m$
Chip Size	$\leq$ 100K mil^2
Shift Rate	$\geq$ 100kHz
Average Access Time	< 7m sec.
Power Dissipation	< 1 Watt
Magnetic Shielding	> 20 Oe
Operating Temperature	0°C to 70°C (case)

Applications

- ☐ Microcomputer Mass Storage
- ☐ Word Processing Terminals
- ☐ Stored Program Controllers
- ☐ Measurement and Test Equipment
- ☐ Electronic Disc Applications
- ☐ Point-of-Sale Terminals
- ☐ Operating System Storage
- ☐ Fast Auxiliary Storage

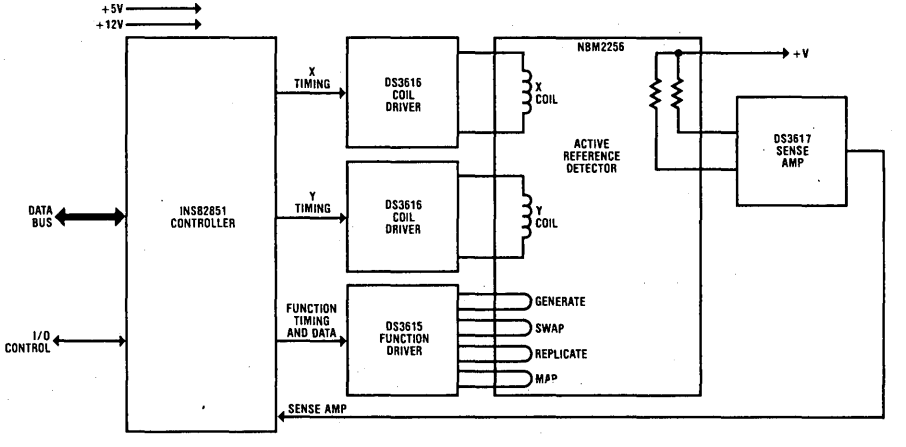
Functions

A "write" operation requires current pulsing the generators sequentially according to the data pattern desired and then pulsing the swap gate when the data block propagates and aligns with the transfer-in ports of the storage loops. A "read" operation consists of pulsing the replicate gate at the proper time when the required data block is at the transfer-out/replicate port. Since data is replicated, a true non-destructive read operation is performed which does not require storing back the data block as in the case of major/minor loop organization. The replicated data block then is sequentially propagated through the detectors to be sensed electronically. A data modifying operation is similar to the "write" operation since "true swap" gates used exchange the new data block with the old one in one step. The old data block is discarded by propagating through the guard rails. The swap gates also eliminate the necessity of sustaining power for a duration longer than the swap operation in the event of power failure.

What are magnetic bubbles

Magnetic bubbles are tiny cylindrical magnetic domains which are formed in a thin magnetic layer when a stabilizing magnetic field of optimum

National's Magnetic Bubble Module and Required Interface — A Functional Block Diagram



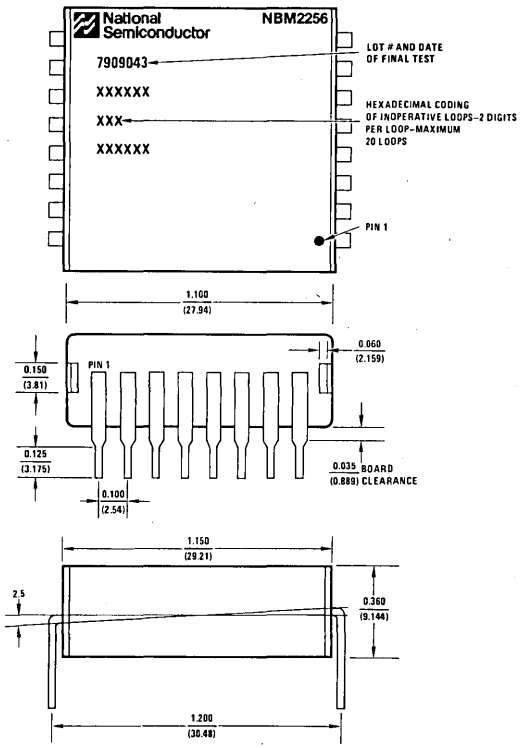
magnitude is applied orthogonally to the magnetic layer. This magnetic layer is grown by liquid phase epitaxy techniques over a non-magnetic substrate.

The cylindrical magnetic domains can be moved over in a controlled manner with the aid of an in-plane rotating field by the creation of attracting manetic poles in a soft magnetic layer such as Permalloy. These domains can be created and destroyed at will by using magnetic fields generated by current-carrying conductors. The absence or presence of a domain can be used to denote binary information ("0", "1") used in digital computers. The detection of the cyclindrical domains is performed by their interaction with a magneto-resistive element whose change in resistance is converted into a voltage by forcing a constant current through the element.

Applications

Magnetic bubble memories are presently used in portable terminals, as message recorders in telephone systems and as floppy disc replacements where the environment is hazardous to rotating memories. In addition, they are being considered for microprocessor mass storage applications, in word processing machines, in point-of-sale terminals where the small number of terminals can not justify a rotating memory, in data communication links, in programmable calculators, in diagnostic data logging for large computers, and in military and airborne applications where reliability is of prime importance. They are also being considered as cache between main memory and large capacity disc files to improve performance of the total system.

Physical Dimensions inches (millimeters)



Section 5

MOS EPROMs

5

Customer-reprogrammable read-only memory has made a remarkable impact upon the art of logic design. National's EPROMs make practical new applications of microprocessors. National is a volume production source of the products included here, and is developing larger EPROMs for tomorrow's applications.

National Semiconductor

MM1702A 2048-Bit (256 x 8) UV Erasable PROM

General Description

The MM1702A is a 256 word by 8-bit electrically programmable ROM ideally suited for uses where fast turn-around and pattern experimentation are important. The MM1702A undergoes complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.

The MM1702AQ is packaged in a 24-pin dual-in-line package with a transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device. The MM1702AD is packaged in a 24-pin dual-in-line package with a metal lid and is not erasable.

The circuitry of the MM1702A is entirely static; no clocks are required.

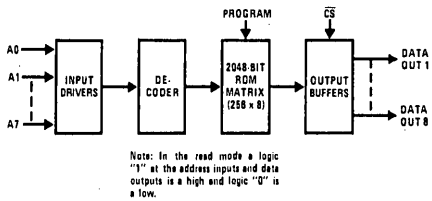
A pin-for-pin metal mask programmed ROM, the MM1302 is ideal for large volume production runs of systems initially using the MM1702A.

The MM1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

Features

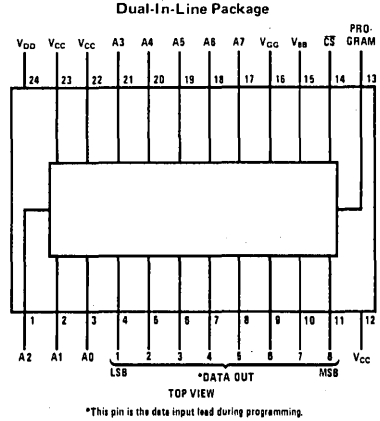
- Fast programming—30 seconds for all 2048 bits
- All 2048 bits guaranteed programmable—100% factory tested
- Fully decoded, 256 x 8 organization
- Static MOS—no clocks required
- Inputs and outputs DTL and TTL compatible
- TRI-STATE® output—OR-tie capability
- Simple memory expansion—chip select input lead
- Direct replacement for the Intel 1702A

Block and Connection Diagrams



Note: In the read mode a logic "1" at the address inputs and data outputs is a high and logic "0" is a low.

Dual-In-Line Package



*This pin is the data input lead during programming.

Order Number MM1702AQ
See NS Package J24CQ

Pin Names

A0–A7	Address Inputs
$\overline{CS}$	Chip Select Input
$D_{OUT\,1} - D_{OUT\,8}$	Data Outputs

Pin Connections*

MODE/PIN	12 (V_{CC})	13 (PROGRAM)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG} (V_{IL4P})	GND	GND

*The external lead connections to the MM1702A differ, depending on whether the device is being programmed or used in read mode. (See following table.) In the programming mode, the data inputs are pins 4–11 respectively.

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +125°C
Power Dissipation	2W
Read Operation	
Input Voltages and Supply Voltages with Respect to V_{CC}	+0.5V to −20V
Program Operation	
Input Voltages and Supply Voltages with Respect to V_{CC}	−48V
Lead Temperature (Soldering, 10 seconds)	300°C

Read Operation DC Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5%, unless otherwise noted. Typical values are at nominal voltages and T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Address and Chip Select Input Load Current	V_{IN} = 0.0V			1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC} −2			1	μA
I_{DDO}	Power Supply Current	V_{GG} = V_{CC}, $\overline{CS}$ = V_{CC} −2 I_{OL} = 0.0 mA, T_A = 25°C, (Note 2)		5	10	mA
I_{DD1}	Power Supply Current	$\overline{CS}$ = V_{CC} −2, I_{OL} = 0.0 mA, T_A = 25°C		35	50	mA
I_{DD2}	Power Supply Current	$\overline{CS}$ = 0.0, I_{OL} = 0.0 mA, T_A = 25°C		32	46	mA
I_{DD3}	Power Supply Current	$\overline{CS}$ = V_{CC} −2, I_{OL} = 0.0 mA, T_A = 0°C		38.5	60	mA
I_{CF1}	Output Clamp Current	V_{OUT} = −1.0V, T_A = 0°C		8	14	mA
I_{CF2}	Output Clamp Current	V_{OUT} = −1.0, T_A = 25°C			13	mA
I_{GG}	Gate Supply Current				1	μA
V_{IL1}	Input Low Voltage for TTL Interface		−1.0		V_{CC}−4.1	V
V_{IL2}	Input Low Voltage for MOS Interface		V_{DD}		V_{CC}−6	V
V_{IH}	Address and Chip Select Input High Voltage		V_{CC}−2		V_{CC}+0.3	V
I_{0L}	Output Sink Current	V_{OUT} = 0.45V	1.6	4		mA
I_{0H}	Output Source Current	V_{OUT} = 0.0V	−2.0			mA
V_{0L}	Output Low Voltage	I_{OL} = 1.6 mA		−0.7	0.45	V
V_{0H}	Output High Voltage	I_{OH} = −100μA	3.5	4.5		V

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Note 2: Power-Down Option: V_{GG} may be clocked to reduce power dissipation. The average I_{DD} will vary between I_{DDO} and I_{DD1} depending on the V_{GG} duty cycle (see typical characteristics). For this option, please specify MM1702AL.

Read Operation AC Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$, $V_{GG} = -9V \pm 5\%$, unless otherwise noted.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Freq.	Repetition Rate			1	MHz
t_{0H}	Previous Read Data Valid			100	ns
t_{ACC}	Address to Output Delay		0.7	1	μs
t_{DVGG}	Clocked V_{GG} Set-Up (Note 1)	1			μs
t_{CS}	Chip Select Delay			100	ns
t_{CO}	Output Delay From $\overline{CS}$			900	ns
t_{0D}	Output Deselect			300	ns
t_{0HC}	Data Out Hold in Clocked V_{GG} Mode (Note 1)			5	μs

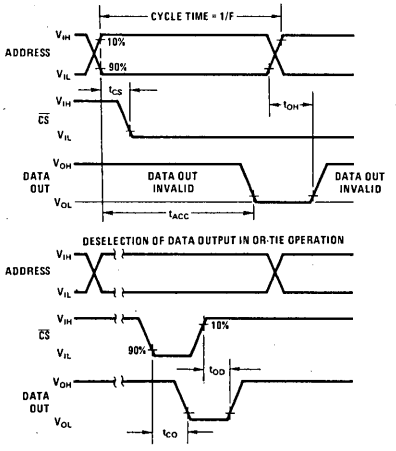
Capacitance Characteristics $T_A = 25°C$ (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance	All Unused	$V_{IN} = V_{CC}$		8	15	pF
C_{OUT}	Output Capacitance	Pins Are	$\overline{CS} = V_{CC}$		10	15	pF
C_{VGG}	V_{GG} Capacitance (Note 1)	At ac Ground	$V_{OUT} = V_{CC}$ $V_{GG} = V_{CC}$			30	pF

Note 3: This parameter is periodically sampled and is not 100% tested.

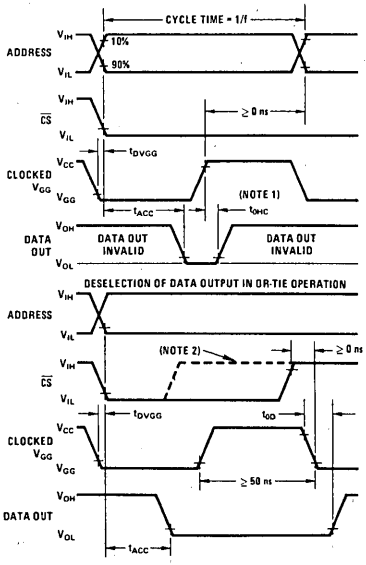
Read Operation Switching Time Waveforms

(a) Constant V_{GG} Operation



Conditions of Test:
Input pulse amplitudes: 0–4V, t_r, $t_f \leq 50$ ns. Output load is 1 TTL gate; measurements made at output of TTL gate ($t_{PD} \leq 15$ ns), $C_L = 15$ pF.

(b) Power-Down Option (Note 1)



Note 1: The output will remain valid for t_{0HC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

Note 2: If $\overline{CS}$ makes a transition from V_{IL} to V_{IN} while clocked V_{GG} is at V_{GG}, then deselection of output occurs at t_{0D} as shown in static operation with constant V_{GG}.

Programming Operation DC Characteristics

$T_A = 25°C$, $V_{CC} = 0V$, $V_{BB} = 12V \pm 10\%$, $\overline{CS} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI1P}	Address and Data Input Load Current	$V_{IN} = -48V$			10	mA
I_{LI2P}	Program and V_{GG} Load Current	$V_{IN} = -48V$			10	mA
I_{BB}	V_{BB} Supply Load Current	(Note 5)		10	100	mA
I_{DDP}	Peak I_{DD} Supply Load Current	$V_{DD} = V_{PROG} = -48V$ $V_{GG} = -35V$ (Note 4)		200	300	mA
V_{IHP}	Input High Voltage				0.3	V
V_{IL1P}	Pulsed Data Input Low Voltage		−46		−48	V
V_{IL2P}	Address Input Low Voltage		−40		−48	V
V_{IL3P}	Pulsed Input Low V_{DD} and Program Voltage		−46		−48	V
V_{IL4P}	Pulsed Input Low V_{GG} Voltage		−35		−40	V

Note 4: I_{DDP} flows only during V_{DD}, V_{GG} on time. I_{DDP} should not be allowed to exceed 300 mA for greater than 100μs. Average power supply current I_{DDP} is typically 40 mA at 20% duty cycle.

Note 5: The V_{BB} supply must be limited to 100 mA max current to prevent damage to the device.

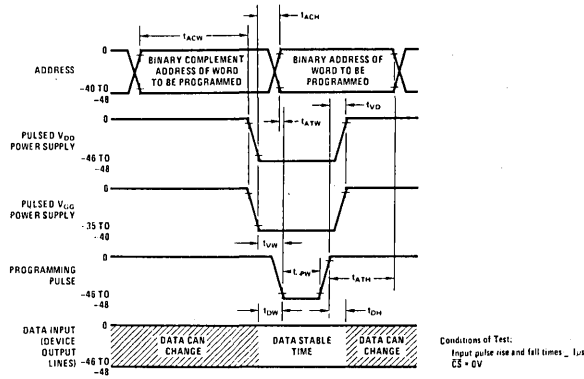
Programming Operation AC Characteristics

$T_A = 25°C$, $V_{CC} = 0V$, $V_{BB} = 12V \pm 10\%$, $\overline{CS} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Duty Cycle (V_{DD}, V_{GG})				20	%
$t_{\phi PW}$	Program Pulse Width	$V_{GG} = -35V$, $V_{DD} = V_{PROG} = -48V$			3	ms
t_{DW}	Data Set-Up Time		25			μs
t_{DH}	Data Hold Time		10			μs
t_{VW}	V_{DD}, V_{GG} Set-Up		100			μs
t_{VD}	V_{DD}, V_{GG} Hold		10		100	μs
t_{ACW}	Address Complement Set-Up	(Note 6)	25			μs
t_{ACH}	Address Complement Hold	(Note 6)	25			μs
t_{ATW}	Address True Set-Up		10			μs
t_{ATH}	Address True Hold		10			μs

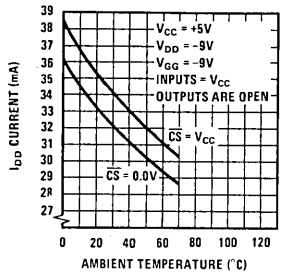
Note 6: All 8 address bits must be in the complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses (0–255) must be programmed as shown in the timing diagram until data reads true, then over-programmed 4 times that amount. (Symbolized by x + 4x.)

Programming Operation Switching Time Waveforms

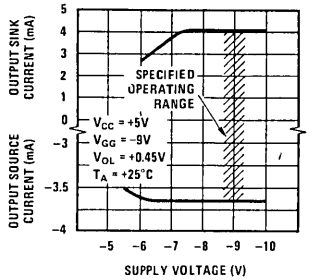


Typical Performance Characteristics

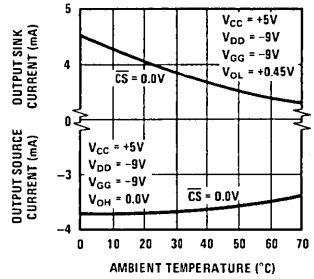
I_{DD} Current vs Temperature



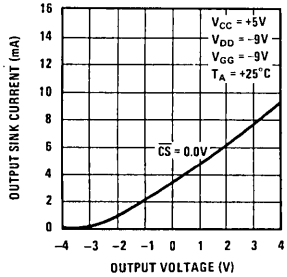
Output Current vs V_{DD} Supply Voltage



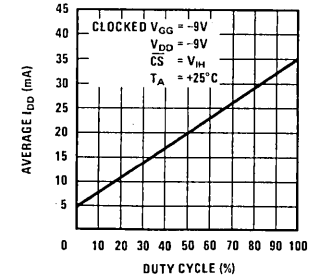
Program Waveforms



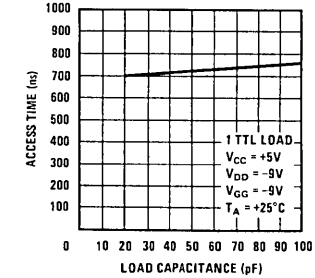
Output Sink Current vs Output Voltage



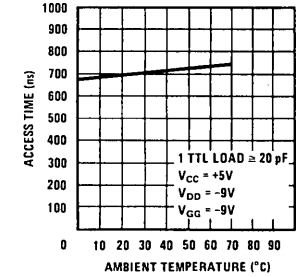
Average Current vs Duty Cycle for Clocked V_{GG} (Note 1)



Access Time vs Load Capacitance



Access Time vs Temperature



5

Operation of the MM1702A in Program Mode

Initially, all 2048 bits of the ROM are in the "0" state (output low). Information is introduced by selectively programming "1's" (output high) in the proper bit locations.

Word address selection is done by the same decoding circuitry used in the READ mode (see table for logic levels). All 8 address bits must be in the binary complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses must be held in their binary complement state for a minimum of 25μs after V_{DD} and V_{GG} have moved to their negative levels. The addresses must then make the transition to their true state a minimum of 10μs before the program pulse is applied. The addresses should be programmed in the sequence 0–255 for a minimum of 32 times. The eight output terminals are used as data inputs to determine the information pattern in the eight bits of each word. A low data input level (–48V) will program a "1" and a high data input level (ground) will leave a "0" (see table on page 4-4). All eight bits of one word are programmed simultaneously be setting the desired bit information patterns on the data input terminals.

During the programming, V_{GG}, V_{DD} and the Program Pulse are pulsed signals.

MM1702A Erasing Procedure

The MM1702A may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose (i.e., UV intensity x exposure time) is 6W sec/cm^2. Examples of ultraviolet sources which can erase the MM1702A in 10 to 20 minutes are the Model UVS-54 and Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters, and the MM1702A to be erased should be placed about one inch away from the lamp tubes. There exists no absolute rule for erase time. Establish a worst case time required with the equipment. Then over-erase by a factor of 2, i.e., if the device appears erased after 8 minutes, continue exposure for an additional 16 minutes for a total of 24 minutes. (May be expressed as x + 2x.)

National Semiconductor

MM2708, MM2708-1 8192-Bit (1024 x 8) UV Erasable PROMs

General Description

The MM2708, MM2708-1 are high speed 8192 UV erasable and electrically reprogrammable EPROMs ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

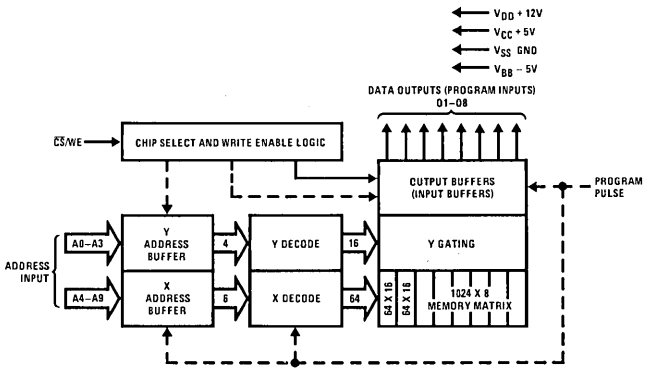
The MM2708, MM2708-1 are packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the devices by following the programming procedure.

These EPROMs are fabricated with the reliable, high volume, time proven, N-channel silicon gate technology.

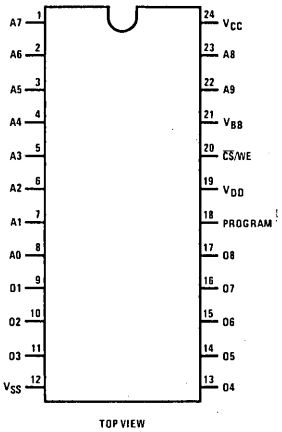
Features

- 1024 x 8 organization
- 800 mW max
- Low power during programming
- Access time – MM2708, 450 ns; MM2708-1, 350 ns
- Standard power supplies: 12V, 5V, –5V
- Static–no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- TRI-STATE® output

Block and Connection Diagrams



Dual-In-Line Package



Order Number MM2708Q or MM2708Q-1
See NS Package J24CQ

Pin Connection During Read or Program

MODE	PIN NUMBER						
	9–11, 13–17	12	18	19	20	21	24
Read	D_{OUT}	V_{SS}	V_{SS}	V_{DD}	V_{IL}	V_{BB}	V_{CC}
Program	D_{IN}	V_{SS}	Pulsed V_{IHP}	V_{DD}	V_{IHW}	V_{BB}	V_{CC}

Pin Description

A0–A9	Address inputs
O1–O8	Data outputs
$\overline{CS}$/WE	Chip select/write enable input

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−25°C to +85°C
Storage Temperature	−65°C to +125°C
V_{DD} with Respect to V_{BB}	20V to −0.3V
V_{CC} and V_{SS} with Respect to V_{BB}	15V to −0.3V
All Input or Output Voltages with Respect to V_{BB} During Read	15V to −0.3V
$\overline{CS}$/WE Input with Respect to V_{BB} During Programming	20V to −0.3V
Program Input with Respect to V_{BB}	35V to −0.3V
Power Dissipation	1.5 W
Lead Temperature (Soldering, 10 seconds)	300°C

Read Operation

DC Operating Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5%, V_{DD} = 12V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V, unless otherwise noted, (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Address and Chip Select Input Sink Current	V_{IN} = 5.25V or V_{IN} = V_{IL}		1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.25V, $\overline{CS}$/WE = 5V		1	10	μA
I_{DD}	V_{DD} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		44	65	mA
I_{CC}	V_{CC} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		7	10	mA
I_{BB}	V_{BB} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		34	45	mA
V_{IL}	Input Low Voltage		V_{SS}		0.65	V
V_{IH}	Input High Voltage		3.0		V_{CC}+1	V
V_{OH1}	Output High Voltage	I_{OH} = −100 μA	3.7			V
V_{OH2}	Output High Voltage	I_{OH} = −1 mA	2.4			V
V_{OL}	Output Low Votlage	I_{OL} = 1.6 mA			0.45	V
P_D	Power Dissipation				800	mW

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5%, V_{DD} = 12V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V, unless otherwise noted

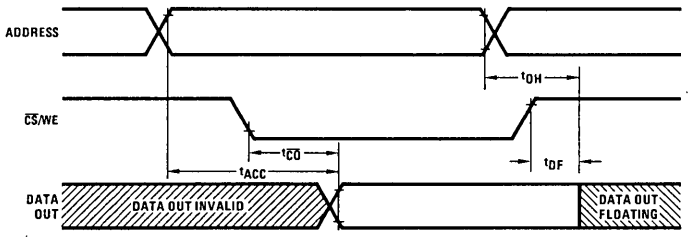
SYMBOL	PARAMETER	CONDITIONS	MM2708		MM2708-1		UNITS
			MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay	Output Load: 1 TTL Gate and C_L = 100 pF, Input Rise and Fall Times ≤ 20 ns: Timing Measurement Reference Levels: 0.8V and 2.8V for Inputs; 0.8V and 2.4V for Outputs, Input Pulse Levels: 0.65V to 3V		450		350	ns
t_{CO}	Chip Select to Output Delay			120		120	ns
t_{DF}	Chip Deselect to Output Delay		0	120		120	ns
t_{OH}	Address to Output Hold		0		0		ns
CAPACITANCE (Note 2)							
C_{IN}	Input Capacitance	V_{IN} = 0V, T_A = 25°C, f = 1 MHz		6		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, T_A = 25°C, f = 1 MHz		12		12	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing. T_A = 25°C, f = 1 MHz

Note 3: Typical conditions are for operation at: T_A = 25°C, V_{CC} = 5V, V_{DD} = 12V, V_{BB} = −5V, and V_{SS} = 0V.

Switching Time Waveforms



Programming Instructions

Initially, and after each erasure, all bits of the MM2708, MM2708-1 are in the "1" state (output high). Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The circuit is set up for programming operation by raising the $\overline{CE}$/WE input (pin 20) to +12V. The word address is selected in the same manner as in the read mode. Data to be programmed are presented, 8 bits in parallel, to the data output lines (O1–O8). Logic levels for address and data lines and the supply voltages are the same as for the read mode. After address and data set up, one program pulse per address is applied to the program input (pin 18). One pass through all addresses is defined as a program loop. The number of loops (N) required is a function of the program pulse width (t_{PW}) according to $N \times t_{PW} \geq 100$ ms.

The width of the program pulse is from 0.1 to 1 ms. The number of loops (N) is from a minimum of 100 (t_{PW} = 1 ms) to greater than 1000 (t_{PW} = 0.1 ms). There must be N successive loops through all 1024 addresses. *It is not permitted to apply N program pulses to an address and then change to the next address to be programmed.* Caution should be observed regarding the end of a program sequence. The $\overline{CS}$/WE falling edge transition must occur before the first address transition when changing from a program to a read cycle. The program pin should also be pulled down to V_{ILP} with an active instead of a passive device. This pin will source a small amount of current (I_{IPL}) when $\overline{CS}$/WE is at V_{IHW} (12V) and the program pulse is at V_{ILP}.

Programming Characteristics

T_A = 25°C, V_{CC} = 5V ±5%, V_{DD} = 12V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V, unless otherwise noted

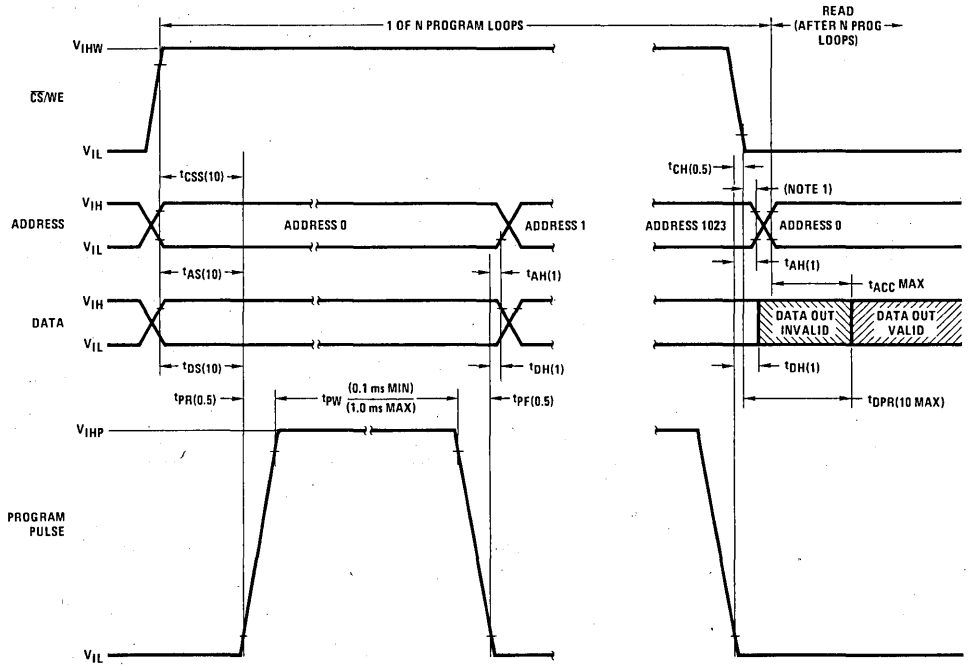
DC Programming Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Address and $\overline{CS}$/WE Input Sink Current	V_{IN} = 5.25V			10	μA
I_{IPL}	Program Pulse Source Current				3	mA
I_{IPH}	Program Pulse Sink Current				20	mA
I_{DD}	V_{DD} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		44	65	mA
I_{CC}	V_{CC} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		7	10	mA
I_{BB}	V_{BB} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		34	45	mA
V_{IL}	Input Low Level (Except Program)		V_{SS}		0.65	V
V_{IH}	Input High Level, All Addresses and Data		3.0		V_{CC}+1	V
V_{IHW}	$\overline{CS}$/WE Input High Level	Referenced to V_{SS}	11.4		12.6	V
V_{IHP}	Program Pulse High Level	Referenced to V_{SS}	25		27	V
V_{ILP}	Program Pulse Low Level	$V_{IHP} - V_{ILP}$ = 25V Min	V_{SS}		1	V

AC Programming Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{AS}	Address Set-Up Time		10			μs
t_{CSS}	$\overline{CS}$/WE Set-Up Time		10			μs
t_{DS}	Data Set-Up Time		10			μs
t_{AH}	Address Hold Time		1			μs
t_{CH}	$\overline{CS}$/WE Hold Time		0.5			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Chip Deselect to Output Float Delay		0		120	μs
t_{DPR}	Program to Read Delay				10	μs
t_{PW}	Program Pulse Width		0.1		1.0	ms
t_{PR}	Program Pulse Rise Time		0.5		2.0	μs
t_{PF}	Program Pulse Fall Time		0.5		2.0	μs

Programming Waveforms



Note 1: The $\overline{CS}$/WE transition must occur after the program pulse transition and before the address transition.
Note 2: Numbers in parentheses indicate minimum timing in microseconds unless otherwise specified.

Functional Description

ERASING

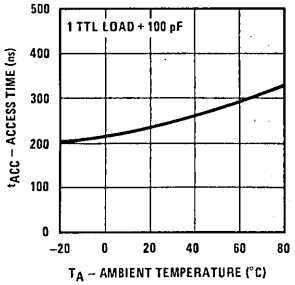
The MM2708 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the MM2708 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time. Direct sunlight can also cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc.) should be placed over the package window if this product is to be operated under these lighting conditions.

An ultraviolet source of 2537 Å yielding a total integrated dosage of 15 watt-seconds/cm^2 is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a 12,000 $\mu W/cm^2$ power rating is used. The MM2708 to be erased should be placed 1 inch away from the lamp and no filters should be used.

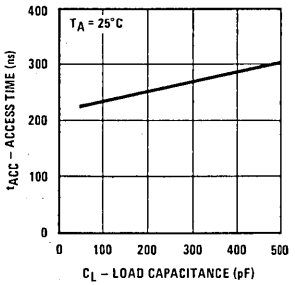
An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance is changed, or the lamp is aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components and system designs have been erroneously suspected when incomplete erasure was the basic problem.

Typical AC Performance Characteristics

Access Time vs Temperature



Access Time vs Load Capacitance



National Semiconductor

MOS EPROMs

MM2716 16,384-Bit (2048 x 8) UV Erasable PROM

General Description

The MM2716 is a high speed 16k UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

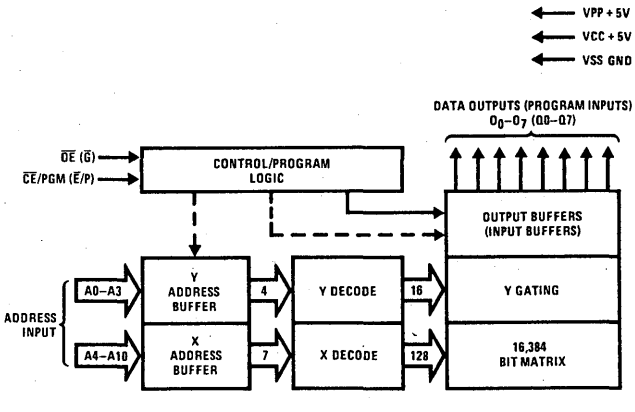
The MM2716 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, N-channel silicon gate technology.

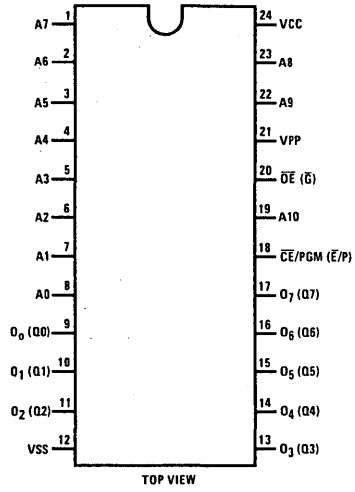
Features

- 2048 x 8 organization
- 525 mW max active power, 132 mW max standby power
- Low power during programming
- Access time—MM2716, 450 ns; MM2716-1, 350 ns; MM2716-2, 390 ns
- Single 5V power supply
- Static—no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- TRI-STATE® output

Block and Connection Diagrams *



Dual-In-Line Package



Order Number MM2716Q, MM2716Q-1 or MM2716Q-2
See NS Package J24CQ

Pin Connection During Read or Program

MODE	PIN NAME/NUMBER				
	CE/PGM (E/P) 18	OE (G) 20	VPP 21	VCC 24	OUTPUTS 9–11, 13–17
Read	VIL	VIL	5	5	DOUT
Program	Pulsed VIL to VIH	VIH	25	5	DIN

*Symbols in parentheses are proposed industry standard

Pin Names

A0–A10	Address Inputs
O0–O7 (Q0–Q7)	Data Outputs
CE/PGM (E/P)	Chip Enable/Program
OE (G)	Output Enable
VPP	Read 5V, Program 25V
VCC	Power (5V)
VSS	Ground

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−25°C to +85°C	All Input or Output Voltages with Respect to VSS (except VPP)	6V to −0.3V
Storage Temperature	−65°C to +125°C	Power Dissipation	1.5 W
VPP Supply Voltage with Respect to VSS	26.5V to −0.3V	Lead Temperature (Soldering, 10 seconds)	300°C

READ OPERATION (Note 2)

DC Operating Characteristics

T_A = 0°C to +70°C, VCC = 5V ±5%, (VCC = 5V ±10% for MM2716-1), VPP = VCC ±0.6V (Note 3), VSS = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ILI	Input Current	VIN = 5.25V or VIN = VIL			10	μA
ILO	Output Leakage Current	VOUT = 5.25V, $\overline{CE}$/PGM = 5V			10	μA
IPP1	VPP Supply Current	VPP = 5.85V			5	mA
ICC1	VCC Supply Current (Standby)	$\overline{CE}$/PGM = VIH, $\overline{OE}$ = VIL		10	25	mA
ICC2	VCC Supply Current (Active)	$\overline{CE}$/PGM = $\overline{OE}$ = VIL		57	100	mA
VIL	Input Low Voltage		0.1		0.8	V
VIH	Input High Voltage		2.0		V_{CC} + 1	V
VOH	Output High Voltage	IOH = 400 μA	2.4			V
VOL	Output Low Voltage	IOL = 2.1 mA			0.45	V

AC Characteristics (Note 4)

T_A = 0°C to +70°C, VCC = 5V ±5%, (VCC = 5V ±10% for MM2716-1), VPP = VCC ±0.6V (Note 3), VSS = 0V, unless otherwise noted.

SYMBOL		PARAMETER	CONDITIONS	MM2716		MM2716-1		MM2716-2		UNITS
ALTERNATE	STANDARD			MIN	MAX	MIN	MAX	MIN	MAX	
t_{ACC}	TAVQV	Address to Output Delay	$\overline{CE}$/PGM = $\overline{OE}$ = VIL		450		350		390	ns
t_{CE}	TELQV	$\overline{CE}$ to Output Delay	$\overline{OE}$ = VIL		450		350		390	ns
t_{OE}	TGLQV	Output Enable to Output Delay	$\overline{CE}$/PGM = VIL		120		120		120	ns
t_{DF}	TGHQZ	Output Enable High to Output Hi-Z	$\overline{CE}$/PGM = VIL	0	100	0	100	0	100	ns
t_{OH}	TAXQX	Address to Output Hold	$\overline{CE}$/PGM = $\overline{OE}$ = VIL	0		0		0		ns
t_{OD}	TEHQZ	$\overline{CE}$ to Output Hi-Z	$\overline{OE}$ = VIL	0	100	0	100	0	100	ns

Capacitance (Note 5)

T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP	MAX	UNITS
CI	Input Capacitance	VIN = 0V	4	6	pF
CO	Output Capacitance	VOUT = 0V	8	12	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Typical conditions are for operation at: T_A = 25°C, VCC = 5V, VPP = VCC, and VSS = 0V.

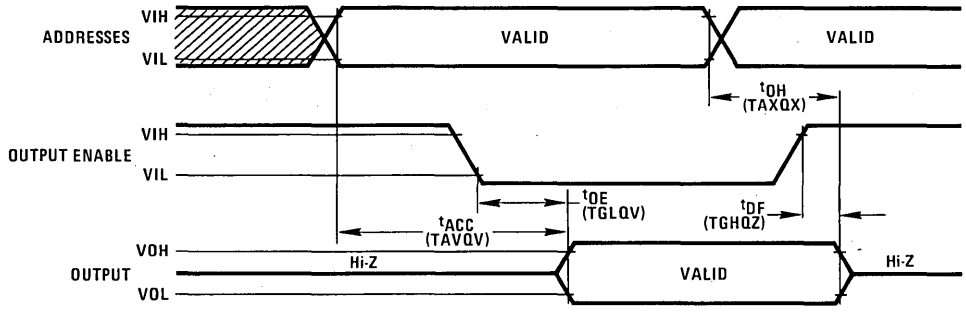
Note 3: VPP may be connected to VCC except during program. The ±0.6V tolerance allows a circuit to switch VPP between the read voltage and the program voltage.

Note 4: Output load: 1 TTL gate and CL = 100 pF. Input rise and fall times ≤ 20 ns.

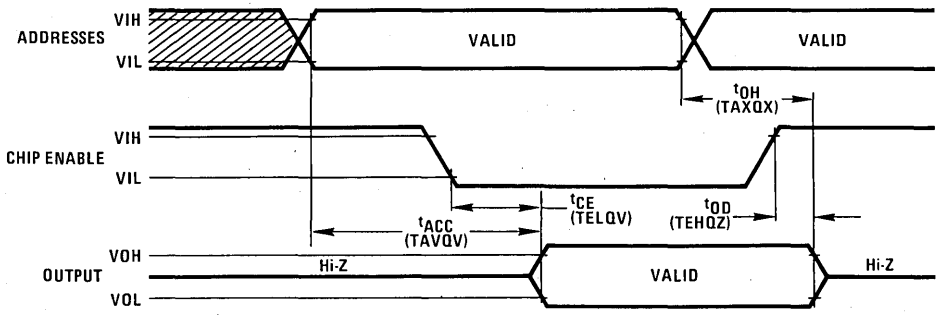
Note 5: Capacitance is guaranteed by periodic testing.

Switching Time Waveforms *

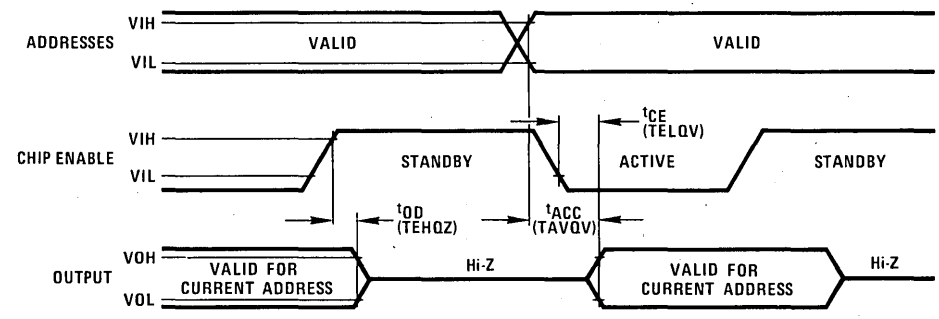
Read Cycle ($\overline{CE}$/PGM = VIL)



Read Cycle ($\overline{OE}$ = VIL)



Standby Power Down Mode ($\overline{OE}$ = VIL)



*Symbols in parentheses are proposed industry standard

PROGRAM OPERATION

DC Electrical Characteristics and Operating Conditions (Notes 1 and 2)

(T_A = 25°C ±5°C) (VCC = 5V ±5%, VPP = 25V ±1V)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
ILI	Input Leakage Current (Note 3)			10	μA
VIL	Input Low Level	−0.1		0.8	V
VIH	Input High Level	2.0		VCC + 1	V
ICC	VCC Power Supply Current			100	mA
IPP1	VPP Supply Current (Note 4)			5	mA
IPP2	VPP Supply Current During Programming Pulse (Note 5)			30	mA

AC Characteristics and Operating Conditions (Notes 1, 2, and 6)

(T_A = 25°C ±5°C) (VCC = 5V ±5%, VPP = 25V ±1V)

SYMBOL		PARAMETER	MIN	TYP	MAX	UNITS
ALTERNATE	STANDARD					
t_{AS}	TAVPH	Address Setup Time	2			μs
t_{OS}	TGHPH	$\overline{OE}$ Setup Time	2			μs
t_{DS}	TDVPH	Data Setup Time	2			μs
t_{AH}	TPLAX	Address Hold Time	2			μs
t_{OH}	TPLGX	$\overline{OE}$ Hold Time	2			μs
t_{DH}	TPLDX	Data Hold Time	2			μs
t_{DF}	TGHQZ	Chip Disable to Output Float Delay (Note 4)	0		100	ns
t_{CE}	TGLQV	Chip Enable to Output Delay (Note 4)			120	ns
t_{PW}	TPHPL	Program Pulse Width	45	50	55	ms
t_{PR}	TPH1PH2	Program Pulse Rise Time	5			ns
t_{PF}	TPL2PL1	Program Pulse Fall Time	5			ns

Note 1: VCC must be applied at the same time or before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be inserted into a board with power applied.

Note 2: Care must be taken to prevent overshoot of the VPP supply when switching to +25V.

Note 3: 0.45V ≤ VIN ≤ 5.25V.

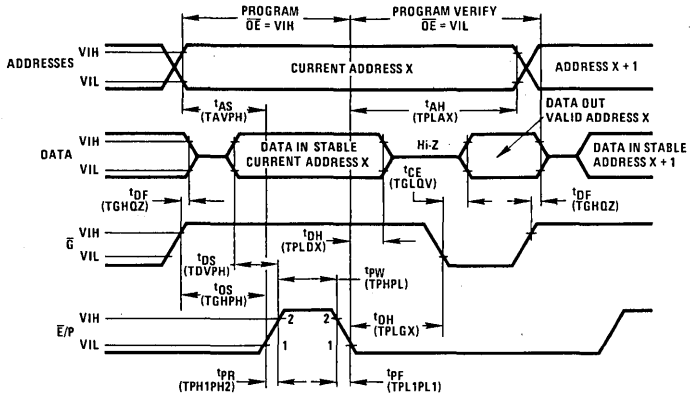
Note 4: $\overline{CE}$/PGM = VIL, VPP = VCC + 0.6V.

Note 5: VPP = 26V.

Note 6: Transition times ≤ 20 ns unless noted otherwise.

Timing Diagram *

Program Mode



Functional Description

DEVICE OPERATION

The MM2716 has 3 modes of operation in the normal system environment. These are shown in Table I.

Read Mode

The MM2716 read operation requires that $\overline{OE}$ = VIL, $\overline{CE}$/PGM = VIL and that addresses A0–A10 have been stabilized. Valid data will appear on the output pins after t_{ACC}, t_{OE} or t_{CE} times (see Switching Time Waveforms) depending on which is limiting.

Deselect Mode

The MM2716 is deselected by making $\overline{OE}$ = VIH. This mode is independent of $\overline{CE}$/PGM and the condition of the addresses. The outputs are Hi-Z when $\overline{OE}$ = VIH. This allows OR-tying 2 or more MM2716's for memory expansion.

Standby Mode (Power Down)

The MM2716 may be powered down to the standby mode by making $\overline{CE}$/PGM = VIH. This is independent of $\overline{OE}$ and automatically puts the outputs in their Hi-Z state. The power is reduced to 25% (132 mW max) of the normal operating power. VCC and VPP must be maintained at 5V. Access time at power up remains either t_{ACC} or t_{CE} (see Switching Time Waveforms).

PROGRAMMING

The MM2716 is shipped from National completely erased. All bits will be at a "1" level (output high) in this initial state and after any full erasure. Table II shows the 3 programming modes.

TABLE I. OPERATING MODES (VCC = VPP = 5V)

MODE	PIN NAME/NUMBER		
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	OUTPUTS 9–11, 13–17
Read	VIL	VIL	DOUT
Deselect	Don't Care	VIH	Hi-Z
Standby	VIH	Don't Care	Hi-Z

TABLE II. PROGRAMMING MODES (VCC = 5V)

MODE	PIN NAME/NUMBER			
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	VPP 21	OUTPUTS Q 9–11, 13–17
Program	Pulsed VIL to VIH	VIH	25	DIN
Program Verify	VIL	VIL	25(5)	DOUT
Program Inhibit	VIL	VIH	25	Hi-Z

*Symbols in parentheses are proposed industry standard

Functional Description (Continued)

Program Mode

The MM2716 is programmed by introducing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, a sequence of addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the chip enable pin. All input voltage levels, including the program pulse on chip enable are TTL compatible. The programming sequence is:

With VPP = 25V, VCC = 5V, $\overline{OE}$ = VIH and $\overline{CE}$/PGM = VIL, an address is selected and the desired data word is applied to the output pins. (VIL = "0" and VIL = "1" for both address and data.) After the address and data signals are stable the program pin is pulsed from VIL to VIH with a pulse width between 45 ms and 55 ms.

Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (VIH or higher) *must not* be maintained longer than $t_{PW(MAX)}$ on the program pin during programming. MM2716's may be programmed in parallel with the same data in this mode.

Program Verify Mode

The programming of the MM2716 may be verified either 1 word at a time during the programming (as shown in the timing diagram) or by reading all of the words out at the end of the programming sequence. This can be done with VPP = 25V (or 5V) in either case.

Program Inhibit Mode

The program inhibit mode allows programming several MM2716's simultaneously with different data for each one by controlling which ones receive the program pulse. All similar inputs of the MM2716 may be paralleled. Pulsing the program pin (from VIL to VIH) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{OE}$ = VIH will put its outputs in the Hi-Z state.

ERASING

The MM2716 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the MM2716 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time. Direct sunlight can also cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc.) should be placed over the package window if this product is to be operated under these lighting conditions.

An ultraviolet source of 2537 Å yielding a total integrated dosage of 15 watt-seconds/cm^2 is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a 12,000 $\mu W/cm^2$ power rating is used. The MM2716 to be erased should be placed 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance is changed, or the lamp is aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

National Semiconductor

MOS EPROMs
PRELIMINARY

MM2716E 16,384-Bit (2048 x 8) UV Erasable PROM Extended Temperature Range

General Description

The MM2716E is a high speed 16k UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

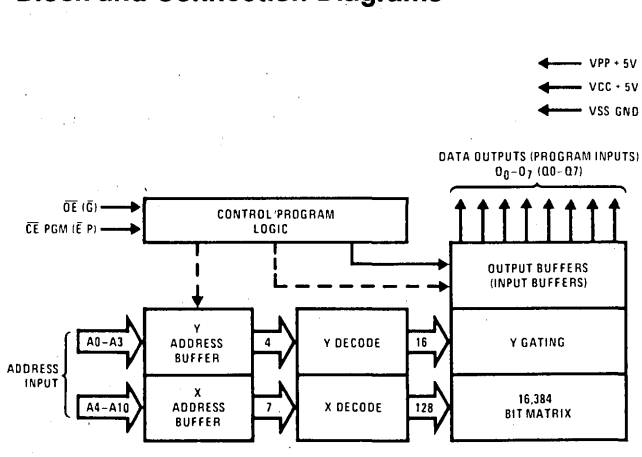
The MM2716E is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, N-channel silicon gate technology.

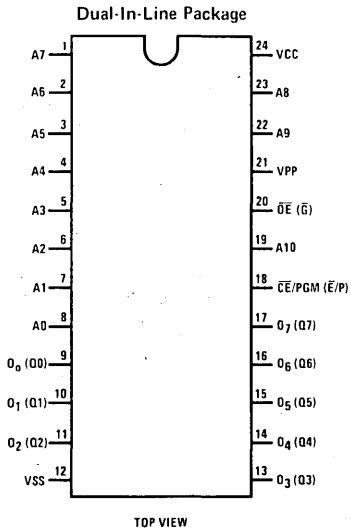
Features

- −40°C to +85°C
- 2048 x 8 organization
- 550 mW max active power, 137.5 mW max standby power
- Low power during programming
- Access time – 450 ns
- Single 5V ±10% power supply
- Static—no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- TRI-STATE® output

Block and Connection Diagrams*



Dual-In-Line Package



TOP VIEW

Order Number MM2716QE
See NS Package J24CQ

Pin Connection During Read or Program

MODE	PIN NAME/NUMBER				
	CE/PGM (E/P) 18	OE (G) 20	VPP 21	VCC 24	OUTPUTS 9–11, 13–17
Read	VIL	VIL	5	5	DOUT
Program	Pulsed VIL to VIH	VIH	25	5	DIN

Pin Names

A0–A10	Address Inputs
O0–O7 (Q0–Q7)	Data Outputs
CE/PGM (E/P)	Chip Enable/Program
OE (G)	Output Enable
VPP	Read 5V, Program 25V
VCC	Power (5V)
VSS	Ground

*Symbols in parentheses are proposed industry standard

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−50°C to +100°C	All Input or Output Voltages with Respect to VSS (except VPP)	6V to −0.3V
Storage Temperature	−65°C to +125°C	Power Dissipation	1.5 W
VPP Supply Voltage with Respect to VSS	26.5V to −0.3V	Lead Temperature (Soldering, 10 seconds)	300°C

READ OPERATION (Note 2)

DC Operating Characteristics

T_A = −40°C to +85°C, VCC = 5V ±10%, VPP = VCC ±0.6V (Note 3), VSS = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ILI	Input Current	VIN = 5.5V or VIN = VIL			10	μA
ILO	Output Leakage Current	VOUT = 5.5V, $\overline{CE}$/PGM = 5V			10	μA
IPP1	VPP Supply Current	VPP = 6.1V			5	mA
ICC1	VCC Supply Current (Standby)	$\overline{CE}$/PGM = VIH, $\overline{OE}$ = VIL		10	25	mA
ICC2	VCC Supply Current (Active)	$\overline{CE}$/PGM = $\overline{OE}$ = VIL		57	100	mA
VIL	Input Low Voltage		−0.1		0.8	V
VIH	Input High Voltage		2.0		V_{CC} + 1	V
VOH	Output High Voltage	IOH = −400 μA	2.4			V
VOL	Output Low Voltage	IOL = 2.1 mA			0.45	V

AC Characteristics (Note 4)

T_A = −40°C to +85°C, VCC = 5V ±10%, VPP = VCC ±0.6V (Note 3), VSS = 0V, unless otherwise noted.

SYMBOL		PARAMETER	CONDITIONS	MIN	MAX	UNITS
ALTERNATE	STANDARD					
t_{ACC}	TAVQV	Address to Output Delay	$\overline{CE}$/PGM = $\overline{OE}$ = VIL		450	ns
t_{CE}	TELQV	$\overline{E}$ to Output Delay	$\overline{OE}$ = VIL		450	ns
t_{OE}	TGLQV	Output Enable to Output Delay	$\overline{CE}$/PGM = VIL		120	ns
t_{DF}	TGHQZ	Output Enable High to Output Hi-Z	$\overline{CE}$/PGM = VIL	0	100	ns
t_{OH}	TAXQX	Address to Output Hold	$\overline{CE}$/PGM = $\overline{OE}$ = VIL	0		ns
t_{OD}	TEHQZ	$\overline{E}$ to Output Hi-Z	$\overline{OE}$ = VIL	0	100	ns

Capacitance (Note 5)

T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP	MAX	UNITS
CI	Input Capacitance	VIN = 0V	4	6	pF
CO	Output Capacitance	VOUT = 0V	8	12	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Typical conditions are for operation at: T_A = 25°C, VCC = 5V, VPP = VCC, and VSS = 0V.

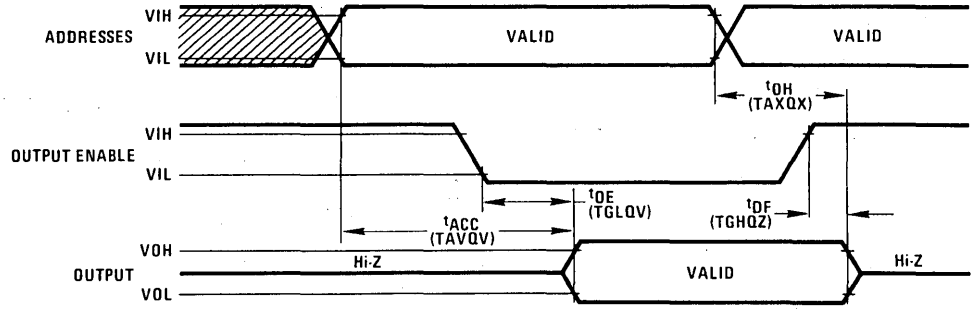
Note 3: VPP may be connected to VCC except during program. The ±0.6V tolerance allows a circuit to switch VPP between the read voltage and the program voltage.

Note 4: Output load: 1 TTL gate and CL = 100 pF. Input rise and fall times ≤ 20 ns.

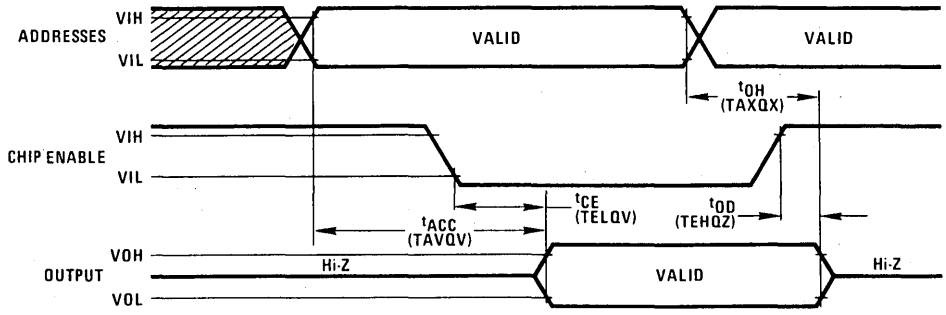
Note 5: Capacitance is guaranteed by periodic testing.

Switching Time Waveforms*

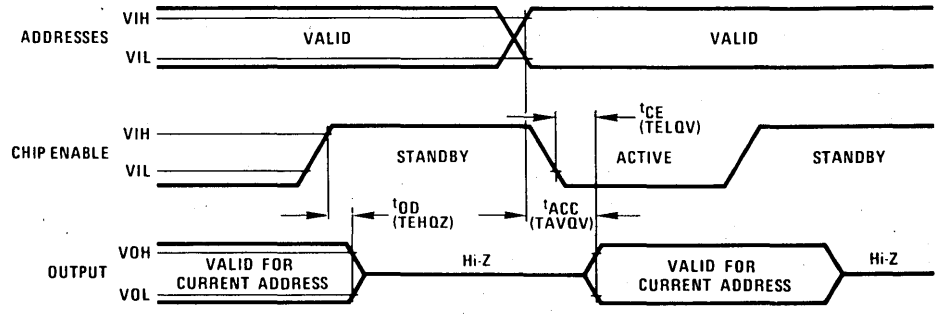
Read Cycle ($\overline{CE}$/PGM = VIL)



Read Cycle ($\overline{OE}$ = VIL)



Standby Power Down Mode ($\overline{OE}$ = VIL)



*Symbols in parentheses are proposed industry standard

PROGRAM OPERATION

DC Electrical Characteristics and Operating Conditions (Notes 1 and 2)

(T_A = 25°C ±5°C) (VCC = 5V ±5%, VPP = 25V ±1V)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
ILI	Input Leakage Current (Note 3)			10	μA
VIL	Input Low Level	−0.1		0.8	V
VIH	Input High Level	2.0		VCC + 1	V
ICC	VCC Power Supply Current			100	mA
IPP1	VPP Supply Current (Note 4)			5	mA
IPP2	VPP Supply Current During Programming Pulse (Note 5)			30	mA

AC Characteristics and Operating Conditions (Notes 1, 2, and 6)

(T_A = 25°C ±5°C) (VCC = 5V ±5%, VPP = 25V ±1V)

SYMBOL		PARAMETER	MIN	TYP	MAX	UNITS
ALTERNATE	STANDARD					
t_{AS}	TAVPH	Address Setup Time	2			μs
t_{OS}	TGHPH	$\overline{OE}$ Setup Time	2			μs
t_{DS}	TDVPH	Data Setup Time	2			μs
t_{AH}	TPLAX	Address Hold Time	2			μs
t_{OH}	TPLGX	$\overline{OE}$ Hold Time	2			μs
t_{DH}	TPLDX	Data Hold Time	2			μs
t_{DF}	TGHQZ	Chip Disable to Output Float Delay (Note 4)	0		100	ns
t_{CE}	TGLQV	Chip Enable to Output Delay (Note 4)			120	ns
t_{PW}	TPHPL	Program Pulse Width	45	50	55	ms
t_{PR}	TPH1PH2	Program Pulse Rise Time	5			ns
t_{PF}	TPL2PL1	Program Pulse Fall Time	5			ns

Note 1: VCC must be applied at the same time or before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be inserted into a board with power applied.

Note 2: Care must be taken to prevent overshoot of the VPP supply when switching to +25V.

Note 3: 0.45V ≤ VIN ≤ 5.25V.

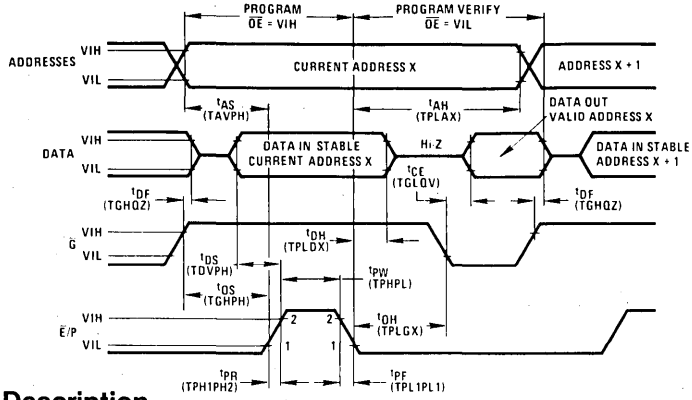
Note 4: $\overline{CE}$/PGM = VIL, VPP = VCC + 0.6V.

Note 5: VPP = 26V.

Note 6: Transition times ≤ 20 ns unless noted otherwise.

Timing Diagram*

Program Mode



Note: VPP = 25V

Functional Description

DEVICE OPERATION

The MM2716E has 3 modes of operation in the normal system environment. These are shown in Table I.

Read Mode

The MM2716E read operation requires that $\overline{OE}$ = VIL, $\overline{CE}$/PGM = VIL and that addresses A0–A10 have been stabilized. Valid data will appear on the output pins after t_{ACC}, t_{OE}, t_{CE} times (see Switching Time Waveforms) depending on which is limiting.

Deselect Mode

The MM2716E is deselected by making $\overline{OE}$ = VIH. This mode is independent of $\overline{CE}$/PGM and the condition of the addresses. The outputs are Hi-Z when $\overline{OE}$ = VIH. This allows OR-tying 2 or more MM2716Es for memory expansion.

Standby Mode (Power Down)

The MM2716E may be powered down to the standby mode by making $\overline{CE}$/PGM = VIH. This is independent of $\overline{OE}$ and automatically puts the outputs in their Hi-Z state. The power is reduced to 25% (150 mW max) of the normal operating power. VCC and VPP must be maintained at 5V. Access time at power up remains either t_{ACC} or t_{CE} (see Switching Time Waveforms).

PROGRAMMING

The MM2716E is shipped from National completely erased. All bits will be at a "1" level (output high) in this initial state and after any full erasure. Table II shows the 3 programming modes.

TABLE I. OPERATING MODES (VCC = VPP = 5V)

MODE	PIN NAME/NUMBER		
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	OUTPUTS 9–11, 13–17
Read	VIL	VIL	DOUT
Deselect	Don't Care	VIH	Hi-Z
Standby	VIH	Don't Care	Hi-Z

TABLE II. PROGRAMMING MODES (VCC = 5V)

MODE	PIN NAME/NUMBER			
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	VPP 21	OUTPUTS Q 9–11, 13–17
Program	Pulsed VIL to VIH	VIH	25	DIN
Program Verify	VIL	VIL	25(5)	DOUT
Program Inhibit	VIL	VIH	25	Hi-Z

*Symbols in parentheses are proposed industry standard

Functional Description (Continued)

Program Mode

The MM2716E is programmed by introducing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, a sequence of addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the chip enable pin. All input voltage levels, including the program pulse on chip-enable are TTL compatible. The programming sequence is:

With VPP = 25V, VCC = 5V, $\overline{OE}$ = VIH and $\overline{CE}$/PGM = VIL, an address is selected and the desired data word is applied to the output pins. (VIL = "0" and VIH = "1" for both address and data.) After the address and data signals are stable the program pin is pulsed from VIL to VIH with a pulse width between 45 ms and 55 ms.

Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (VIH or higher) *must not* be maintained longer than $t_{PW(MAX)}$ on the program pin during programming. MM2716Es may be programmed in parallel with the same data in this mode.

Program Verify Mode

The programming of the MM2716E may be verified either 1 word at a time during the programming (as shown in the timing diagram) or by reading all of the words out at the end of the programming sequence. This can be done with VPP = 25V (or 5V) in either case.

Program Inhibit Mode

The program inhibit mode allows programming several MM2716Es simultaneously with different data for each one by controlling which ones receive the program pulse. All similar inputs of the MM2716E may be paralleled. Pulsing the program pin (from VIL to VIH) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{OE}$ = VIH will put its outputs in the Hi-Z state.

ERASING

The MM2716E is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the MM2716E be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time. Direct sunlight (any intense light) can cause temporary functional failure due to generation of photo current. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc.) should be placed over the package window if this product is to be operated under these lighting conditions.

An ultraviolet source of 2537 Å yielding a total integrated dosage of 15 watt-seconds/cm^2 is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a 12,000 μW/cm^2 power rating is used. The MM2716E to be erased should be placed 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance is changed, or the lamp is aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

National Semiconductor

MOS EPROMs

MM2716M 16,384-Bit (2048 x 8) UV Erasable PROM Military Temperature Range

General Description

The MM2716M is a high speed 16k UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

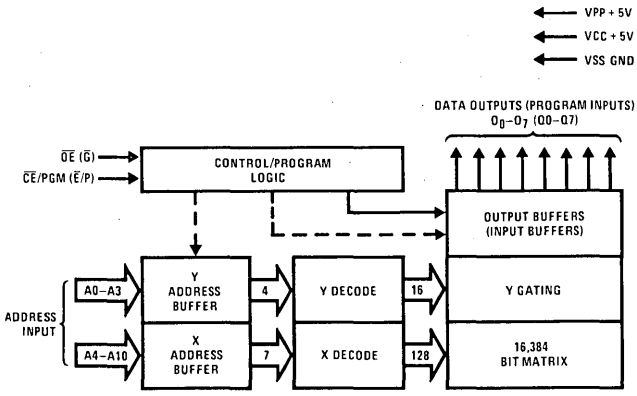
The MM2716M is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, N-channel silicon gate technology.

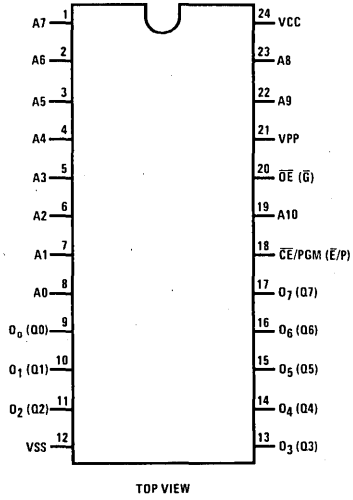
Features

- −55°C to +125°C
- 2048 x 8 organization
- 632 mW max active power, 150 mW max standby power
- Low power during programming
- Access time — 450 ns
- Single 5V ±10% power supply
- Static—no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- TRI-STATE® output

Block and Connection Diagrams *



Dual-In-Line Package



TOP VIEW

Order Number MM2716QM
See NS Package J24CQ

Pin Connection During Read or Program

MODE	PIN NAME/NUMBER				
	CE/PGM (E/P) 18	OE (G) 20	VPP 21	VCC 24	OUTPUTS 9–11, 13–17
Read	VIL	VIL	5	5	DOUT
Program	Pulsed VIL to VIH	VIH	25	5	DIN

Pin Names

A0–A10	Address Inputs
O0–O7 (Q0–Q7)	Data Outputs
CE/PGM (E/P)	Chip Enable/Program
OE (G)	Output Enable
VPP	Read 5V, Program 25V
VCC	Power (5V)
VSS	Ground

*Symbols in parentheses are proposed industry standard

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−65°C to +125°C	All Input or Output Voltages with Respect to VSS (except VPP)	6V to −0.3V
Storage Temperature	−65°C to +125°C	Power Dissipation	1.5 W
VPP Supply Voltage with Respect to VSS	26.5V to −0.3V	Lead Temperature (Soldering, 10 seconds)	300°C

READ OPERATION (Note 2)

DC Operating Characteristics

$T_A = -55^\circ C$ to $+125^\circ C$, VCC = 5V ±10%, VPP = VCC ±0.6V (Note 3), VSS = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ILI	Input Current	VIN = 5.5V or VIN = VIL			10	μA
ILO	Output Leakage Current	VOUT = 5.5V, $\overline{CE}$/PGM = 5V			10	μA
IPP1	VPP Supply Current	VPP = 6.1V			5	mA
ICC1	VCC Supply Current (Standby)	$\overline{CE}$/PGM = VIH, $\overline{OE}$ = VIL		10	30	mA
ICC2	VCC Supply Current (Active)	$\overline{CE}$/PGM = $\overline{OE}$ = VIL		57	115	mA
VIL	Input Low Voltage		−0.1		0.8	V
VIH	Input High Voltage		2.0		V_{CC} + 1	V
VOH	Output High Voltage	IOH = −400 μA	2.4			V
VOL	Output Low Voltage	IOL = 2.1 mA			0.45	V

AC Characteristics (Note 4)

$T_A = -55^\circ C$ to $+125^\circ C$, VCC = 5V ±10%, VPP = VCC ±0.6V (Note 3), VSS = 0V, unless otherwise noted.

SYMBOL		PARAMETER	CONDITIONS	MIN	MAX	UNITS
ALTERNATE	STANDARD					
t_{ACC}	TAVQV	Address to Output Delay	$\overline{CE}$/PGM = $\overline{OE}$ = VIL		450	ns
t_{CE}	TELQV	$\overline{E}$ to Output Delay	$\overline{OE}$ = VIL		450	ns
t_{OE}	TGLQV	Output Enable to Output Delay	$\overline{CE}$/PGM = VIL		150	ns
t_{DF}	TGHQZ	Output Enable High to Output Hi-Z	$\overline{CE}$/PGM = VIL	0	130	ns
t_{OH}	TAXQX	Address to Output Hold	$\overline{CE}$/PGM = $\overline{OE}$ = VIL	0		ns
t_{OD}	TEHQZ	$\overline{E}$ to Output Hi-Z	$\overline{OE}$ = VIL	0	130	ns

Capacitance (Note 5)

$T_A = 25^\circ C$, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP	MAX	UNITS
CI	Input Capacitance	VIN = 0V	4	6	pF
CO	Output Capacitance	VOUT = 0V	8	12	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Typical conditions are for operation at: $T_A = 25^\circ C$, VCC = 5V, VPP = VCC, and VSS = 0V.

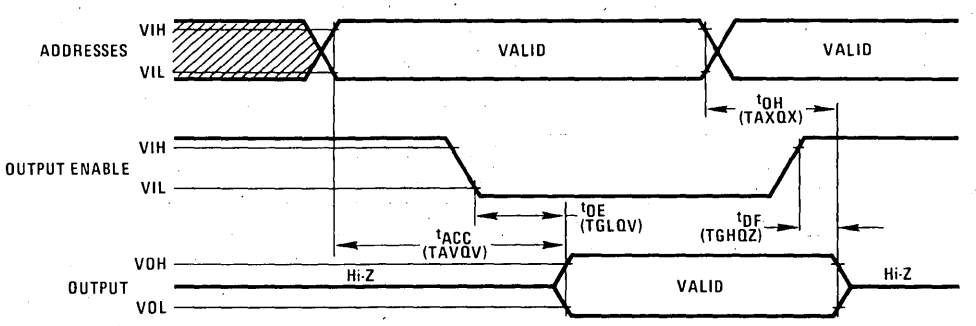
Note 3: VPP may be connected to VCC except during program. The ±0.6V tolerance allows a circuit to switch VPP between the read voltage and the program voltage.

Note 4: Output load: 1 TTL gate and CL = 100 pF. Input rise and fall times ≤ 20 ns.

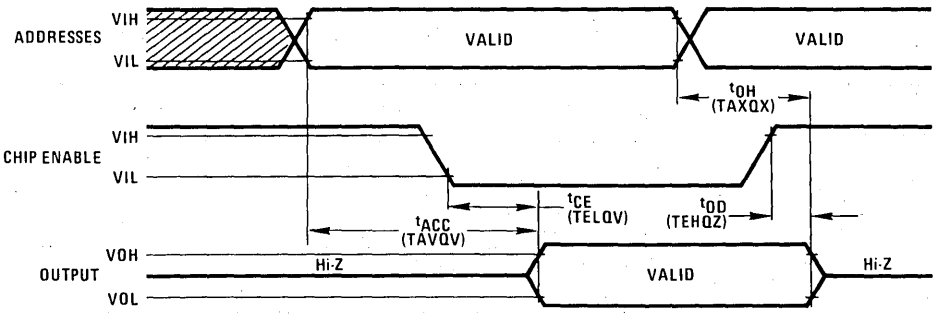
Note 5: Capacitance is guaranteed by periodic testing.

Switching Time Waveforms*

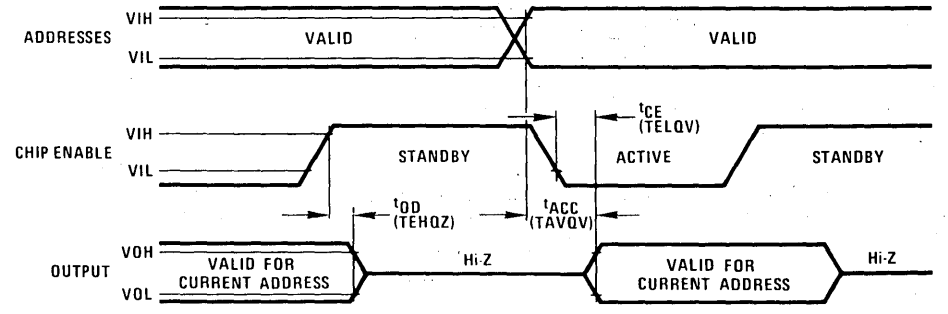
Read Cycle ($\overline{CE}$/PGM = VIL)



Read Cycle ($\overline{OE}$ = VIL)



Standby Power Down Mode ($\overline{OE}$ = VIL)



*Symbols in parentheses are proposed industry standard

PROGRAM OPERATION

DC Electrical Characteristics and Operating Conditions (Notes 1 and 2)

(T_A = 25°C ±5°C) (VCC = 5V ±5%, VPP = 25V ±1V)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
ILI	Input Leakage Current (Note 3)			10	μA
VIL	Input Low Level	−0.1		0.8	V
VIH	Input High Level	2.0		VCC + 1	V
ICC	VCC Power Supply Current			100	mA
IPP1	VPP Supply Current (Note 4)			5	mA
IPP2	VPP Supply Current During Programming Pulse (Note 5)			30	mA

AC Characteristics and Operating Conditions (Notes 1, 2, and 6)

(T_A = 25°C ±5°C) (VCC = 5V ±5%, VPP = 25V ±1V)

SYMBOL		PARAMETER	MIN	TYP	MAX	UNITS
ALTERNATE	STANDARD					
t_{AS}	TAVPH	Address Setup Time	2			μs
t_{OS}	TGHPH	$\overline{OE}$ Setup Time	2			μs
t_{DS}	TDVPH	Data Setup Time	2			μs
t_{AH}	TPLAX	Address Hold Time	2			μs
t_{OH}	TPLGX	$\overline{OE}$ Hold Time	2			μs
t_{DH}	TPLDX	Data Hold Time	2			μs
t_{DF}	TGHQZ	Chip Disable to Output Float Delay (Note 4)	0		130	ns
t_{CE}	TGLQV	Chip Enable to Output Delay (Note 4)			150	ns
t_{PW}	TPHPL	Program Pulse Width	45	50	55	ms
t_{PR}	TPH1PH2	Program Pulse Rise Time	5			ns
t_{PF}	TPL2PL1	Program Pulse Fall Time	5			ns

Note 1: VCC must be applied at the same time or before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be inserted into a board with power applied.

Note 2: Care must be taken to prevent overshoot of the VPP supply when switching to +25V.

Note 3: 0.45V ≤ VIN ≤ 5.25V.

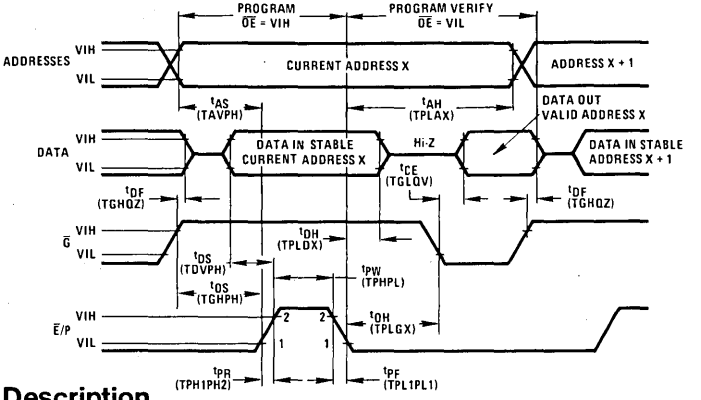
Note 4: $\overline{CE}$/PGM = VIL, VPP = VCC + 0.6V.

Note 5: VPP = 26V.

Note 6: Transition times ≤ 20 ns unless noted otherwise.

Timing Diagram*

Program Mode



Note: VPP = 25V

Functional Description

DEVICE OPERATION

The MM2716M has 3 modes of operation in the normal system environment. These are shown in Table I.

Read Mode

The MM2716M read operation requires that $\overline{OE}$ = VIL, $\overline{CE}$/PGM = VIL and that addresses A0–A10 have been stabilized. Valid data will appear on the output pins after t_{ACC}, t_{OE}, t_{CE} times (see Switching Time Waveforms) depending on which is limiting.

Deselect Mode

The MM2716M is deselected by making $\overline{OE}$ = VIH. This mode is independent of $\overline{CE}$/PGM and the condition of the addresses. The outputs are Hi-Z when $\overline{OE}$ = VIH. This allows OR-tying 2 or more MM2716M's for memory expansion.

Standby Mode (Power Down)

The MM2716M may be powered down to the standby mode by making $\overline{CE}$/PGM = VIH. This is independent of $\overline{OE}$ and automatically puts the outputs in their Hi-Z state. The power is reduced to 25% (150 mW max) of the normal operating power. VCC and VPP must be maintained at 5V. Access time at power up remains either t_{ACC} or t_{CE} (see Switching Time Waveforms).

PROGRAMMING

The MM2716M is shipped from National completely erased. All bits will be at a "1" level (output high) in this initial state and after any full erasure. Table II shows the 3 programming modes.

TABLE I. OPERATING MODES (VCC = VPP = 5V)

MODE	PIN NAME/NUMBER		
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	OUTPUTS 9–11, 13–17
Read	VIL	VIL	DOUT
Deselect	Don't Care	VIH	Hi-Z
Standby	VIH	Don't Care	Hi-Z

TABLE II. PROGRAMMING MODES (VCC = 5V)

MODE	PIN NAME/NUMBER			
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	VPP 21	OUTPUTS O 9–11, 13–17
Program	Pulsed VIL to VIH	VIH	25	DIN
Program Verify	VIL	VIL	25(5)	DOUT
Program Inhibit	VIL	VIH	25	Hi-Z

*Symbols in parentheses are proposed industry standard

Functional Description (Continued)

Program Mode

The MM2716M is programmed by introducing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, a sequence of addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the chip enable pin. All input voltage levels, including the program pulse on chip-enable are TTL compatible. The programming sequence is:

With VPP = 25V, VCC = 5V, $\overline{OE}$ = VIH and $\overline{CE}$/PGM = VIL, an address is selected and the desired data word is applied to the output pins. (VIL = "0" and VIH = "1" for both address and data.) After the address and data signals are stable the program pin is pulsed from VIL to VIH with a pulse width between 45 ms and 55 ms.

Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (VIH or higher) *must not* be maintained longer than $t_{PW(MAX)}$ on the program pin during programming. MM2716M's may be programmed in parallel with the same data in this mode.

Program Verify Mode

The programming of the MM2716M may be verified either 1 word at a time during the programming (as shown in the timing diagram) or by reading all of the words out at the end of the programming sequence. This can be done with VPP = 25V (or 5V) in either case.

Program Inhibit Mode

The program inhibit mode allows programming several MM2716M's simultaneously with different data for each one by controlling which ones receive the program pulse. All similar inputs of the MM2716M may be paralleled. Pulsing the program pin (from VIL to VIH) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{OE}$ = VIH will put its outputs in the Hi-Z state.

ERASING

The MM2716M is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the MM2716M be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time. Direct sunlight can also cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc.) should be placed over the package window if this product is to be operated under these lighting conditions.

An ultraviolet source of 2537 Å yielding a total integrated dosage of 15 watt-seconds/cm^2 is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a 12,000 $\mu W/cm^2$ power rating is used. The MM2716M to be erased should be placed 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance is changed, or the lamp is aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

National Semiconductor

MOS EPROMs

MM2758 8192-Bit (1024 x 8) UV Erasable PROM

General Description

The MM2758 is a high speed 8k UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

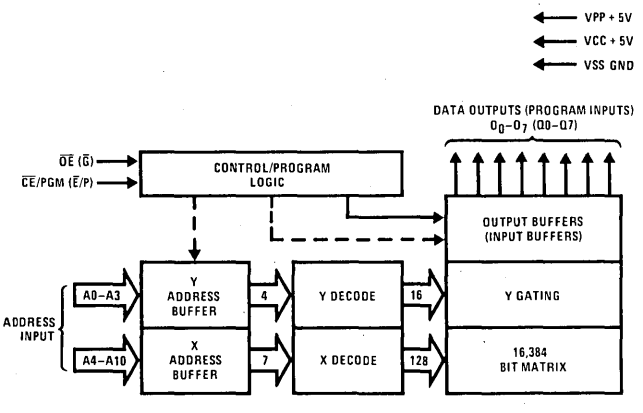
The MM2758 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, N-channel silicon gate technology.

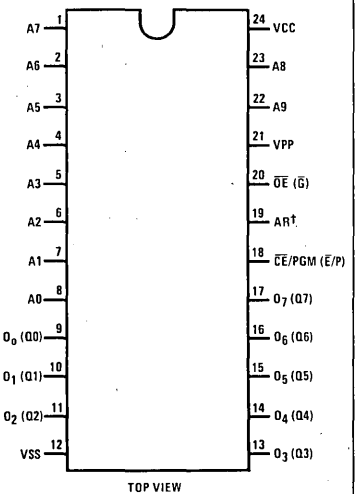
Features

- 1024 x 8 organization
- 525 mW max active power, 132 mW max standby power
- Low power during programming
- Access time—450 ns
- Single 5V power supply
- Static—no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- TRI-STATE® output

Block and Connection Diagrams *



Dual-In-Line Package



TOP VIEW

Order Number MM2758AQ or MM2758BQ
See NS Package J24CQ

Pin Connection During Read or Program

MODE	PIN NAME/NUMBER				
	CE/PGM (E/P) 18	OE (G) 20	VPP 21	VCC 24	OUTPUTS 9–11, 13–17
Read	VIL	VIL	5	5	DOUT
Program	Pulsed VIL to VIH	VIH	25	5	DIN

Pin Names

A0–A10	Address Inputs
O0–O7 (Q0–Q7)	Data Outputs
CE/PGM (E/P)	Chip Enable/Program
OE (G)	Output Enable
VPP	Read 5V, Program 25V
VCC	Power (5V)
VSS	Ground

*Symbols in parentheses are proposed industry standard
†For MM2758A AR = VIL for all operating modes
For MM2758B AR = VIH for all operating modes

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−25°C to +85°C	All Input or Output Voltages with Respect to VSS (except VPP)	6V to −0.3V
Storage Temperature	−65°C to +125°C	Power Dissipation	1.5 W
VPP Supply Voltage with Respect to VSS	26.5V to −0.3V	Lead Temperature (Soldering, 10 seconds)	300°C

READ OPERATION (Note 2)

DC Operating Characteristics

T_A = 0°C to +70°C, VCC = 5V ±5%,
VPP = VCC ±0.6V (Note 3), VSS = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ILI	Input Current	VIN = 5.25V or VIN = VIL			10	μA
ILO	Output Leakage Current	VOUT = 5.25V, $\overline{CE}$/PGM = 5V			10	μA
IPP1	VPP Supply Current	VPP = 5.85V			5	mA
ICC1	VCC Supply Current (Standby)	$\overline{CE}$/PGM = VIH, $\overline{OE}$ = VIL		10	25	mA
ICC2	VCC Supply Current (Active)	$\overline{CE}$/PGM = $\overline{OE}$ = VIL		57	100	mA
VIL	Input Low Voltage		0.1		0.8	V
VIH	Input High Voltage		2.0		V_{CC} + 1	V
VOH	Output High Voltage	IOH = 400 μA	2.4			V
VOL	Output Low Voltage	IOL = 2.1 mA			0.45	V

AC Characteristics (Note 4)

T_A = 0°C to +70°C, VCC = 5V ±5%,
VPP = VCC ±0.6V (Note 3), VSS = 0V, unless otherwise noted.

SYMBOL		PARAMETER	CONDITIONS	MM2758		UNITS
ALTERNATE	STANDARD			MIN	MAX	
t_{ACC}	TAVQV	Address to Output Delay	$\overline{CE}$/PGM = $\overline{OE}$ = VIL		450	ns
t_{CE}	TELQV	$\overline{CE}$ to Output Delay	$\overline{OE}$ = VIL		450	ns
t_{OE}	TGLQV	Output Enable to Output Delay	$\overline{CE}$/PGM = VIL		120	ns
t_{DF}	TGHQZ	Output Enable High to Output Hi-Z	$\overline{CE}$/PGM = VIL	0	100	ns
t_{OH}	TAXQX	Address to Output Hold	$\overline{CE}$/PGM = $\overline{OE}$ = VIL	0		ns
t_{OD}	TEHQZ	$\overline{CE}$ to Output Hi-Z	$\overline{OE}$ = VIL	0	100	ns

Capacitance (Note 5)

T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	TYP	MAX	UNITS
CI	Input Capacitance	VIN = 0V	4	6	pF
CO	Output Capacitance	VOUT = 0V	8	12	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Typical conditions are for operation at: T_A = 25°C, VCC = 5V, VPP = VCC, and VSS = 0V.

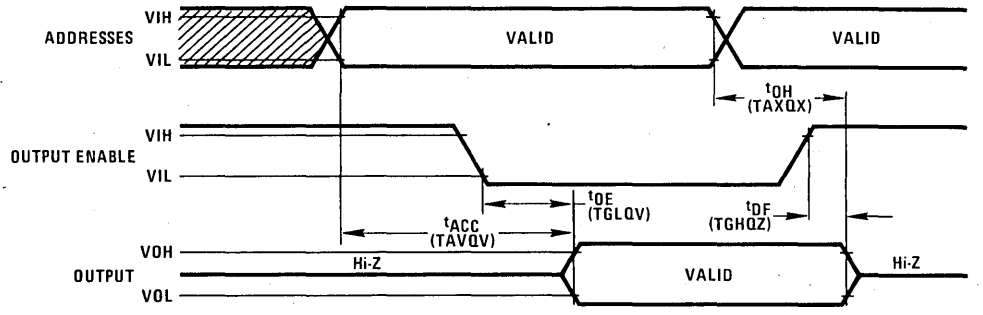
Note 3: VPP may be connected to VCC except during program. The ±0.6V tolerance allows a circuit to switch VPP between the read voltage and the program voltage.

Note 4: Output load: 1 TTL gate and CL = 100 pF. Input rise and fall times ≤ 20 ns.

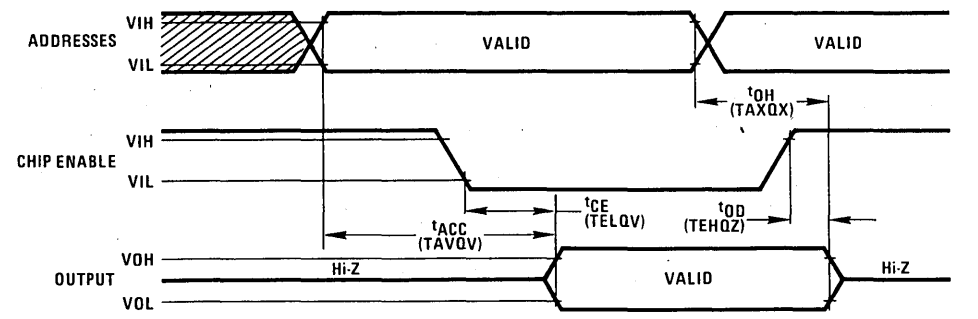
Note 5: Capacitance is guaranteed by periodic testing.

Switching Time Waveforms *

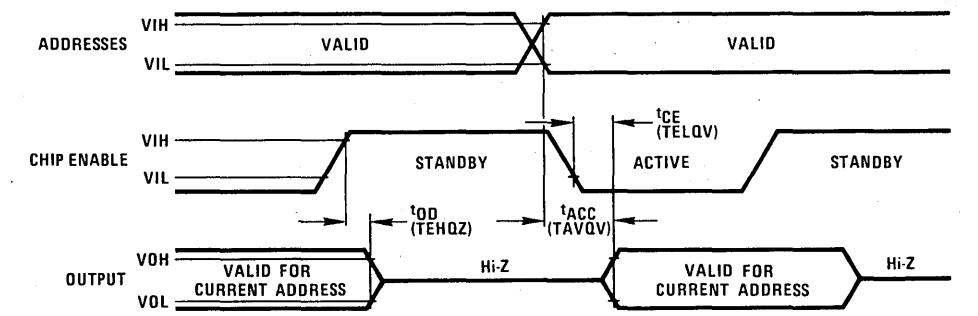
Read Cycle ($\overline{CE}$/PGM = VIL)



Read Cycle ($\overline{OE}$ = VIL)



Standby Power Down Mode ($\overline{OE}$ = VIL)



*Symbols in parentheses are proposed industry standard

PROGRAM OPERATION

DC Electrical Characteristics and Operating Conditions (Notes 1 and 2)

(T_A = 25°C ±5°C) (VCC = 5V ±5%, VPP = 25V ±1V)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
ILI	Input Leakage Current (Note 3)			10	μA
VIL	Input Low Level	−0.1		0.8	V
VIH	Input High Level	2.0		VCC + 1	V
ICC	VCC Power Supply Current			100	mA
IPP1	VPP Supply Current (Note 4)			5	mA
IPP2	VPP Supply Current During Programming Pulse (Note 5)			30	mA

AC Characteristics and Operating Conditions (Notes 1, 2, and 6)

(T_A = 25°C ±5°C) (VCC = 5V ±5%, VPP = 25V ±1V)

SYMBOL		PARAMETER	MIN	TYP	MAX	UNITS
ALTERNATE	STANDARD					
t_{AS}	TAVPH	Address Setup Time	2			μs
t_{OS}	TGHPH	$\overline{OE}$ Setup Time	2			μs
t_{DS}	TDVPH	Data Setup Time	2			μs
t_{AH}	TPLAX	Address Hold Time	2			μs
t_{OH}	TPLGX	$\overline{OE}$ Hold Time	2			μs
t_{DH}	TPLDX	Data Hold Time	2			μs
t_{DF}	TGHQZ	Chip Disable to Output Float Delay (Note 4)	0		100	ns
t_{CE}	TGLQV	Chip Enable to Output Delay (Note 4)			120	ns
t_{PW}	TPHPL	Program Pulse Width	45	50	55	ms
t_{PR}	TPH1PH2	Program Pulse Rise Time	5			ns
t_{PF}	TPL2PL1	Program Pulse Fall Time	5			ns

Note 1: VCC must be applied at the same time or before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be inserted into a board with power applied.

Note 2: Care must be taken to prevent overshoot of the VPP supply when switching to +25V.

Note 3: $0.45V \leq VIN \leq 5.25V$.

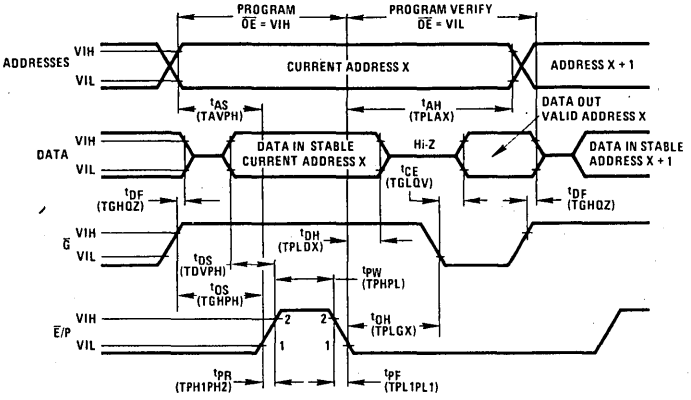
Note 4: $\overline{CE}/PGM$ = VIL, VPP = VCC + 0.6V.

Note 5: VPP = 26V.

Note 6: Transition times ≤ 20 ns unless noted otherwise.

Timing Diagram *

Program Mode



Functional Description

DEVICE OPERATION

The MM2758 has 3 modes of operation in the normal system environment. These are shown in Table I.

Read Mode

The MM2758 read operation requires that $\overline{OE}$ = VIL, $\overline{CE}$/PGM = VIL and that addresses A0–A10 have been stabilized. Valid data will appear on the output pins after t_{ACC}, t_{OE} or t_{CE} times (see Switching Time Waveforms) depending on which is limiting.

Deselect Mode

The MM2758 is deselected by making $\overline{OE}$ = VIH. This mode is independent of $\overline{CE}$/PGM and the condition of the addresses. The outputs are Hi-Z when $\overline{OE}$ = VIH. This allows OR-tying 2 or more MM2716's for memory expansion.

Standby Mode (Power Down)

The MM2758 may be powered down to the standby mode by making $\overline{CE}$/PGM = VIH. This is independent of $\overline{OE}$ and automatically puts the outputs in their Hi-Z state. The power is reduced to 25% (132 mW max) of the normal operating power. VCC and VPP must be maintained at 5V. Access time at power up remains either t_{ACC} or t_{CE} (see Switching Time Waveforms).

PROGRAMMING

The MM2758 is shipped from National completely erased. All bits will be at a "1" level (output high) in this initial state and after any full erasure. Table II shows the 3 programming modes.

TABLE I. OPERATING MODES (VCC = VPP = 5V)

MODE	PIN NAME/NUMBER		
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	OUTPUTS 9–11, 13–17
Read	VIL	VIL	DOUT
Deselect	Don't Care	VIH	Hi-Z
Standby	VIH	Don't Care	Hi-Z

TABLE II. PROGRAMMING MODES (VCC = 5V)

MODE	PIN NAME/NUMBER			
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	VPP 21	OUTPUTS Q 9–11, 13–17
Program	Pulsed VIL to VIH	VIH	25	DIN
Program Verify	VIL	VIL	25(5)	DOUT
Program Inhibit	VIL	VIH	25	Hi-Z

*Symbols in parentheses are proposed industry standard

Functional Description (Continued)

Program Mode

The MM2758 is programmed by introducing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, a sequence of addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the chip enable pin. All input voltage levels, including the program pulse on chip enable are TTL compatible. The programming sequence is:

With VPP = 25V, VCC = 5V, $\overline{OE}$ = VIH and $\overline{CE}$/PGM = VIL, an address is selected and the desired data word is applied to the output pins. (VIL = "0" and VIL = "1" for both address and data.) After the address and data signals are stable the program pin is pulsed from VIL to VIH with a pulse width between 45 ms and 55 ms.

Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (VIH or higher) *must not* be maintained longer than $t_{PW(MAX)}$ on the program pin during programming. MM2758's may be programmed in parallel with the same data in this mode.

Program Verify Mode

The programming of the MM2758 may be verified either 1 word at a time during the programming (as shown in the timing diagram) or by reading all of the words out at the end of the programming sequence. This can be done with VPP = 25V (or 5V) in either case.

Program Inhibit Mode

The program inhibit mode allows programming several MM2758s simultaneously with different data for each one by controlling which ones receive the program pulse. All similar inputs of the MM2758 may be paralleled. Pulsing the program pin (from VIL to VIH) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{OE}$ = VIH will put its outputs in the Hi-Z state.

ERASING

The MM2758 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the MM2758 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time. Direct sunlight can also cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc.) should be placed over the package window if this product is used under these lighting conditions.

An ultraviolet source of 2537 Å yielding a total integrated dosage of 15 watt-seconds/cm^2 is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a 12,000 μW/cm^2 power rating is used. The MM2758 to be erased should be placed 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance is changed, or the lamp is aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

National Semiconductor

MOS EPROMs

MM4203/MM5203 2048-Bit (256 x 8 or 512 x 4) UV Erasable PROM

General Description

The MM4203/MM5203 is a 2048-bit static read-only memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as a 256-8-bit words or 512-4-bit words. Programming of the memory contents is accomplished by storing a charge in a cell location by programming that location with a 50 volt pulse. Separate output supply lead is provided to reduce internal power dissipation in the output stage (V_{LL}).

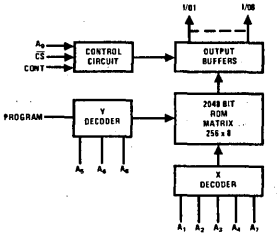
Features

- Field programmable
- Bipolar compatibility — +5V, −12V operation
- High speed operation — 1μs max access time
- Pin compatible with MM5213, MM5231 mask programmable ROMs
- Static operation — no clocks required
- Common data busing (TRI-STATE® output)
- "Q" quartz lid version erasable with short wave ultra-violet light (i.e. 253.7 n.m.)
- Chip select output control
- 256 x 8 or 512 x 4 organization

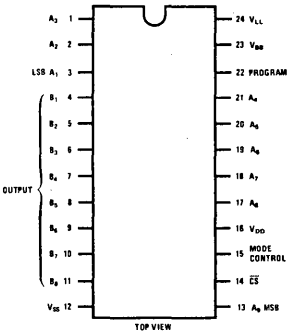
Applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Micro-programming

Block and Connection Diagrams



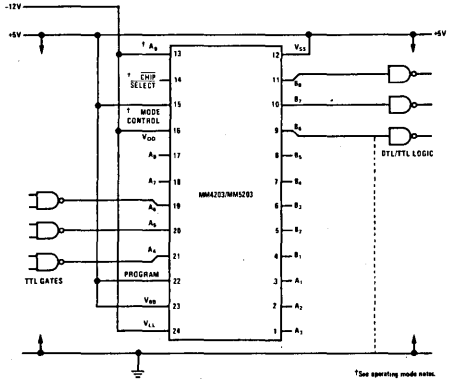
Dual-In-Line Package



Order Number MM4203Q or MM5203Q
See NS Package J24CQ

Typical Applications

256 x 8 PROM Showing TTL Interface



Operating Modes

256 x 8 ROM connection (shown)
Mode Control — HIGH (V_{SS})
A_9 — LOW

512 x 4 ROM connections
Mode Control — LOW (GND or V_{DD})
A_9 — Logic HIGH enables the odd (B_1, B_3..B_7) outputs
— Logic LOW enables the even (B_2, B_4 . B_8) outputs

The outputs are enabled when a logic LOW is applied to the Chip Select line.

Programming is accomplished in 256 x 8 mode only.

Absolute Maximum Ratings

All Input or Output Voltages with Respect to V_{BB} Except During Programming +.3V to −20V
Power Dissipation 1W
Storage Temperature Range −65°C to 125°C
Lead Temperature (Soldering, 10 sec) 300°C

Operating Conditions

Operating Temperature Range MM4203 −55°C to 85°C
MM5203 0°C to 70°C

Electrical Characteristics

T_A within operating temperature range, V_{SS} = +5V ±5%, $V_{DD} = V_{LL}$ = −12V, ±5%, V_{BB} = PROGRAM = V_{SS} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Input Current	V_{IN} = 0V			1	μA
I_{LO}	Output Leakage	V_{OUT} = 0V $\overline{CS}$ = V_{SS} − 2.0			1	μA
I_{SS}	Power Supply Current	T_A = 25°C $\overline{CS}$ = V_{SS} − 2.0		35	55	mA
V_{IL}	Input LOW Voltage		V_{SS} − 10		V_{SS} − 4.0	V
V_{IH}	Input HIGH Voltage		V_{SS} − 2.0		V_{SS} + .3	V
V_{OL}	Output LOW Voltage	1.6 mA sink −12.6V < V_{LL} < −3V			.40	V
I_{CF}	Output Clamp Current	V_{LL} = −3.0V V_{OUT} = −1.0V (Note 8) T_A = 0°C		3.5	6.0	mA
		V_{LL} = −12.6V V_{OUT} = −1.0V (Note 8) T_A = 0°C		8.0	15.0	mA
V_{OH}	Output HIGH Voltage	0.8 mA source	2.4			V
T_{OH}	Data Hold Time	(Min Access Time) Figures 1 & 2			100	ns
T_{ACC}	Access Time	T_A = 25°C Figures 1 & 2 (Note 6)		.700	1	μs
T_{CO}	Chip Select Time	Figures 1 & 3			500	ns
T_{OD}	Chip Deselect Time	Figures 1 & 3			500	ns
t_{CS}	Allowable Chip Select Delay	Figures 1 & 2 Allowable delay in selecting chip after change of address without affecting access time.			100	ns
C_{IN}	Input Capacitance	V_{IN} = V_{SS} } f = 1.0 MHz (Note 2)		8	15	pF
C_{OUT}	Output Capacitance	V_{OUT} = V_{SS} } $\overline{CS}$ = V_{SS} − 2.0		8	15	pF

Programming Characteristics (see Figure 4)

T_A = 25°C, V_{SS} = 0V, V_{BB} = +12V ±10%, $\overline{CS}$ = 0V unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LD}	Address and Data Input Load Current	V_{IN} = −50V		0	10	mA
I_{LP}	Program Load Current	V_{IN} = −50V		0	10	mA
I_{LB}	V_{BB} Supply Load Current			0	10	mA
I_{LDD}	Peak I_{DD} Supply Load Current (Note 3)	$V_{DD} = V_{program}$ = −50V		650		mA
V_{IHP}	Input High Voltage		−2		+.3	V
V_{ILP}	Address and Data Input Low Voltage		−50		−40	V
	Pulsed Input Low Voltage:					
	V_{DD}, and Program, V_{DLP}		−50		−48	V
	V_{LL}	(Note 5)	−50		0	V
	V_{DD} Pulse Duty Cycle				2	%
t_{PW}	Program Pulse Width (Note 4)	$V_{DD} = V_{program}$ = −50V			20	ms
t_{DW}	Data and Address Set Up Time			1		μs
t_{DH}	Data and Address Hold Time,			0		μs
t_{SS}	Pulsed V_{DD} Supply Overlap,			1	100	μs
t_{SH}	Pulsed V_{DD} Supply Overlap,			−.1	3	ms
	V_{DD}, Program, Address, and Input Rise and Fall Times				1	μs

Note 1: During programming, data is always applied in the 256 x 8 mode, regardless of the logic state of Ag and MODE CONTROL.
Note 2: Capacitances are not tested on a production basis but are periodically sampled.
Note 3: I_{DDP} flows only during program period t_{PWP}. Average power supply current I_{LDD} is typically 15 mA at 2% duty cycle.
Note 4: Maximum duty cycle of t_{PW} should not be greater than 2% of cycle time so that power dissipation is minimized. The program cycle should be repeated until the data reads true, then over-program three times that number of cycles (symbolized as X+3X programming.
Note 5: V_{LL} is not needed during programming but may be tied to V_{DD} for convenience.
Note 6: T_{ACC} = 1000 ns + 25(N−1) where N is the number of chips wired-OR together.
Note 7: Measured under continuous operation.
Note 8: I_{CF} flows out the V_{LL} pin, it does not flow out the V_{DD} pin.

Access Time Diagrams

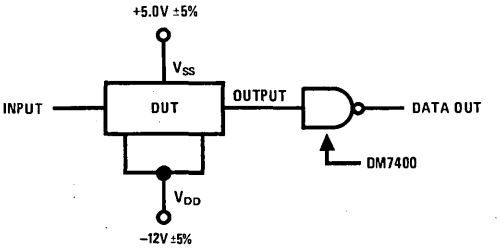


Figure 1

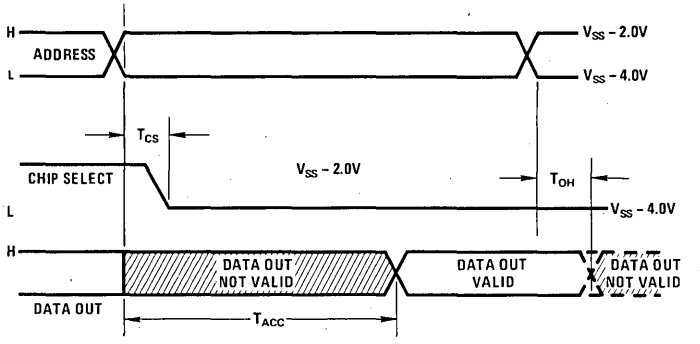


Figure 2

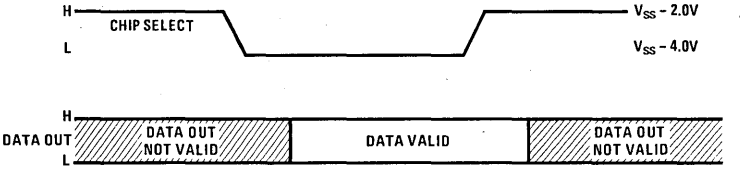


Figure 3

Program Waveforms

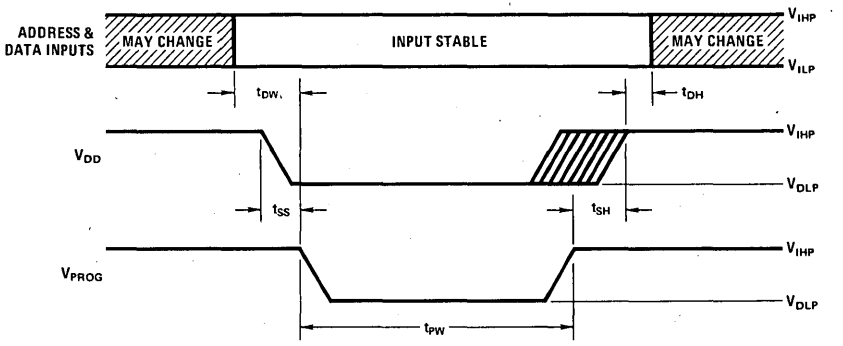


Figure 4

Operation of the MM4203/MM5203 in Program Mode

Initially, all 2048 bits of the MM4203/MM5203 are in the HIGH state. Information is introduced by selectively programming LOWS in the proper bit locations. (Note 1)

Word address selection is done by the same decoding circuitry used in the Read mode. The eight output terminals are used as data inputs to determine the information pattern in the eight bits of each word. A LOW data input level (−50V) will leave a HIGH and a HIGH data input level will allow programming of a LOW. All eight bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals. The duty cycle of the V_{DD} pulse (amplitude and width as specified on page 4) should be limited to 2%. The address should be applied for at least 1 μs before application of the Program pulse. In programming mode, data inputs 1–8 are pins 4–11 respectively regardless of the logic state of A_9 and mode control. Chip select should be disabled (HIGH).

Positive logic is used during the read mode for addresses and data out. Address 0 corresponds to all address inputs at V_{IL} and address 255_{10} corresponds to all address inputs at V_{IH}. A "1" or a P at a data output corresponds to V_{OH}. A "0" or an N at a data output corresponds to V_{OL}. Positive logic is also used during the programming mode for addresses. Address 0 corresponds to all address inputs at V_{ILP} and address 255_{10} corresponds to all address inputs at V_{IHP}.

Negative logic is used during the programming mode for data in. A "1" or a P at a data input corresponds to V_{ILP}. A "0" or an N at a data input corresponds to V_{IHP}.

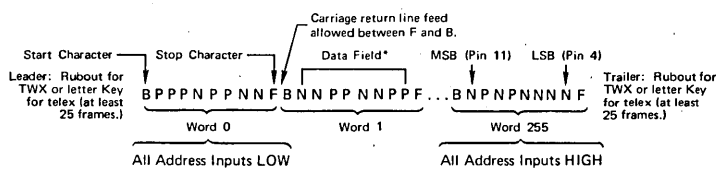
MODE	DATA AND ADDRESS LINES		V_{SS}	V_{BB}	V_{DD}	PROGRAM	$\overline{CS}$	V_{LL}
	HIGH	LOW						
Read	V_{SS} − 2.0	V_{SS} − 4.0	+5	V_{SS}	−12	V_{SS}	V_{SS} − 4V	−3V to −12V
Program	V_{SS} −2.0	V_{SS} − 40	GND	+12	−48 (Pulse)	−48 (Pulse)	GND	GND to −50V

Erasing Procedure

The MM4203Q/MM5203Q may be erased by exposure to short-wave ultraviolet light—253.7 nm. There exists no absolute rule for erasing time or distance from source. The erasing equipment output capability should be calibrated. Establish a worst-case time required with the equipment. Then over-erase by a factor of 2, i.e., if the device appears erased after 8 minutes, continue exposure for an additional 16 minutes for a total of 24 minutes. Examples of UV sources include the Model UVS-54 and Model S-2 manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters. The MM4203/MM5203 should be placed about one inch away from the lamp for about 20–30 minutes.

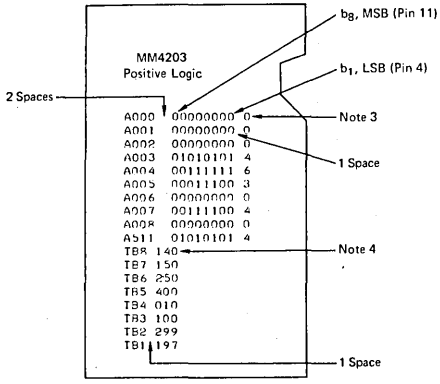
Preferred Tape Format

The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7 bit ASCII code from model 33 teletype or TWX. The paper tape should be as the following example:



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start character. If an error is made in preparing a tape the entire word including the B and F start and stop characters must be rubbed out. Data for exactly 256 words must be entered, beginning with word 0.

Alternate Format [Punched Tape (Note 1) or Cards]



Note 1: The code is a 7-bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

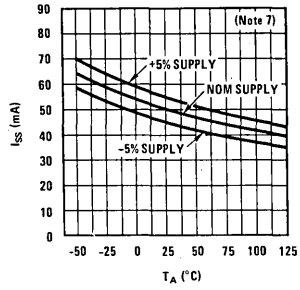
Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1" bits in the output word.

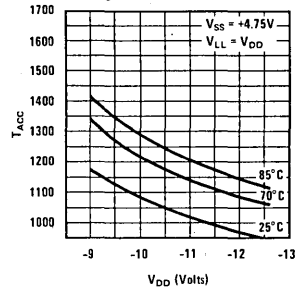
Note 4: The total number of "1" bits in each output column or bit position.

Typical Performance Characteristics

Maximum Supply Current I_{SS} as a Function of Temperature



Maximum Access Time (T_{ACC}) as a Function of V_{DD} Supply Voltage



National Semiconductor

MOS EPROMs

MM4204/MM5204 4096-Bit (512 x 8) UV Erasable PROM

General Description

The MM4204/MM5204 is a 4096-bit static read only memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as 512 words by 8 bits per word. Programming of the memory is accomplished by storing a charge in a cell location by applying a −50V pulse. A logic input, Power Saver, is provided which gives a 5:1 decrease in power when the memory is not being accessed.

Features

- Field programmable
- Fast program time: ten seconds typical for 4096 bits
- Fast access time

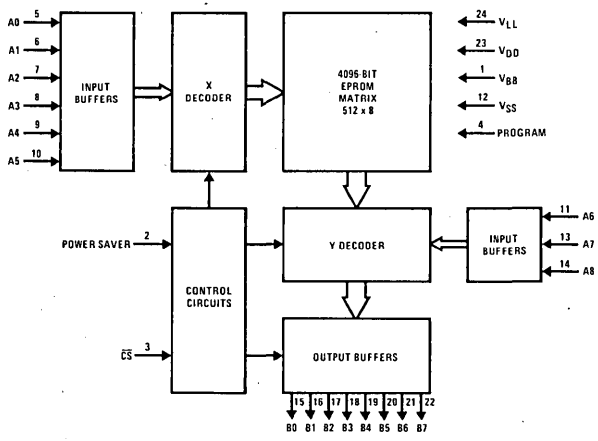
MM4204	1.25 μs
MM5204	1 μs

- DTL/TTL compatibility
- Standard power supplies 5V, −12V
- Static operation—no clock required
- Easy memory expansion—TRI-STATE® output Chip Select input ($\overline{CS}$)
- "Q" quartz lid version erasable with short wave ultraviolet light (i.e., 253.7 nm)
- Low power dissipation
- "Power Saver" control for low power applications
- Compatible with SC/MP II N-channel microprocessor

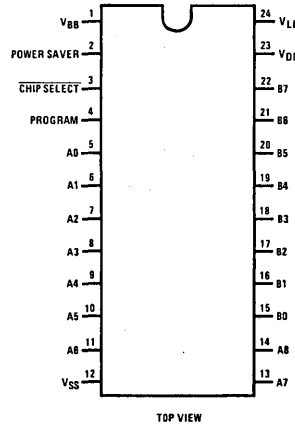
Applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming
- Electronic keyboards

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM4204D or MM5204D
See NS Package D24C

Order Number MM4204Q or MM5204Q
See NS Package J24CQ

5

Absolute Maximum Ratings (Note 1)

All Input or Output Voltages with Respect to V_{BB} Except During Programming	+0.3V to −20V
Power Dissipation	750 mW
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

Operating Temperature Range	
MM5204	0°C to +70°C
MM4204	−55°C to +85°C

DC Electrical Characteristics

T_A within operating temperature range, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, MM4204: V_{SS} = 5V ±10%, V_{DD} = −12V ±10%, MM5204: V_{SS} = 5V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
V_{IL}	Input Low Voltage		V_{SS}−14		V_{SS}−4.2	V
V_{IH}	Input High Voltage		V_{SS}−1.5		V_{SS}+0.3	V
I_{LI}	Input Current	V_{IN} = 0V			1.0	μA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	V_{LL}		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −0.8 mA	2.4		V_{SS}	V
I_{LO}	Output Leakage Current	V_{OUT} = 0V, $\overline{CS}$ = V_{IH}			1.0	μA
I_{DD}	Power Supply Current	MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}		28	40.0	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			50.0	mA
		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}		6.0	8.0	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			10.0	mA
		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			42	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IL}			52	mA
I_{SS}		MM5204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			10	mA
		MM4204 T_A = 0°C, $\overline{CS}$ = V_{IH}, Power Saver = V_{IH}			12	mA

AC Electrical Characteristics

T_A within operating temperature range, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, MM4204: V_{SS} = 5V ±10%, V_{DD} = −12V ±10%, MM5204: V_{SS} = 5V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
t_{ACC}	Access Time					
	MM5204	T_A = 70°C, *(Figure 1)*, (Note 4)		0.75	1.0	μs
	MM4204	T_A = 85°C, *(Figure 1)*, (Note 4)			1.25	μs
t_{PO}	Power Saver Set-Up Time					
	MM5204	*(Figure 1)*			1.8	μs
	MM4204	*(Figure 1)*			2.0	μs
t_{CO}	Chip Select Delay					
	MM5204	*(Figure 1)*			500	ns
	MM4204	*(Figure 1)*			600	ns
t_{OH}	Data Hold Time	*(Figure 1)*	30	50		ns
t_{ODC}	Chip Select Deselect Time					
	MM5204	*(Figure 1)*	30	300	500	ns
	MM4204	*(Figure 1)*	30	300	600	ns
t_{ODP}	Power Saver Deselect Time					
	MM5204	*(Figure 1)*	30	300	500	ns
	MM4204	*(Figure 1)*	30	300	600	ns
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = V_{SS}, f = 1.0 MHz, (Note 2)		5.0	8.0	pF
C_{OUT}	Output Capacitance (All Outputs)	V_{OUT} = V_{SS}, $\overline{CS}$ = V_{IH}, f = 1.0 MHz, (Note 2)		8.0	15	pF

Programmer Electrical Characteristics

$T_A = 25°C$, $V_{SS} = \overline{CS}$ = Power Saver = 0V, V_{LL} = 0V to −14V, unless otherwise specified, *(Figure 2)*, (Note 5).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (Note 7)	MAX	UNITS
I_{LD}	Data Input Load Current	V_{IN} = −18V			−10	mA
I_{ALD}	Address Input Load Current	V_{IN} = −50V			−10	mA
I_{LP}	Program Load Current	V_{IN} = −50V			−10	mA
I_{LBB}	V_{BB} Load Current				50	mA
I_{LDD}	V_{DD} Load Current	V_{DD} = PROGRAM = −50V			−200	mA
V_{IHP}	Address Data and Power Saver Input High Voltage		−2.0		0.3	V
V_{ILP}	Address Input Low Voltage		−50		−11	V
	Data Input Low Voltage		−18		−11	V
V_{DHP}	V_{DD} and Program High Voltage		−2.0		0.5	V
V_{DLP}	V_{DD} and Program Low Voltage		−50		−48	V
V_{BLP}	V_{BB} Low Voltage		0		0.4	V
V_{BHP}	V_{BB} High Voltage		11.4		12.6	V
V_{DD}	Pulse Duty Cycle				25	%
t_{PW}	Program Pulse Width		0.5		5.0	ms
t_{DS}	Data and Address Set-Up Time		40			μs
t_{DH}	Data and Address Hold Time		0			μs
t_{SS}	Pulsed V_{DD} Set-Up Time		40		100	μs
t_{SH}	Pulsed V_{DD} Hold Time		1.0			μs
t_{BS}	Pulsed V_{BB} Set-Up Time		1.0			μs
t_{BH}	Pulsed V_{BB} Hold Time		1.0			μs
t_{PSS}	Power Saver Set-Up Time		1.0			μs
t_{PSH}	Power Saver Hold Time		1.0			μs
t_R, t_F	V_{DD}, Program, Address and Data Rise and Fall Time				1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: Positive true logic notation is used except on data inputs during programming
Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

Note 4: t_{ACC} = 700 ns + 25 (N-1) where N is the number of devices wire−OR'd together.

Note 5: The program cycle should be repeated until the data reads true, then over-programmed 5 times that number of cycles. (Symbolized as X + 5X programming).

Note 6: The EPROM is initially programmed with all "0's." A V_{IHP} on any data input B0−B7 will leave the stored "0's" undisturbed, and a V_{ILP} on any data input B0−B7 will write a logic "1" into that location.

Note 7: Typical values are for nominal voltages and $T_A = 25°C$, unless otherwise specified.

Erase Specification

The recommended dosage of ultraviolet light exposure is 6W sec/cm².

Programming

The MM4204/MM5204 is normally shipped in the unprogrammed state. All 4096-bits are at logic "0" state. The table of electrical programming characteristics and *Figure 2* give the conditions for programming of the device. In the program mode the device effectively becomes a RAM with the 512 word locations selected by address inputs A0−A8. Data inputs are B0−B7 and write operation is controlled by pulsing the Program input. Since the EROM is initially shipped with all "0's," a V_{IHP} on any data input B0−B7 will leave the stored "0's" undisturbed and a V_{ILP} on any data input B0−B7 will write a logic "1" into that location.

Programming (Continued)

National offers programmer options with both the IMP16-P and the PACE IPC-16P Microprocessor Development Systems.

Microprocessor System	Programmer Part Number
IMP16-P	IMP16-P/805
IPC-16P	IPC-16P/805

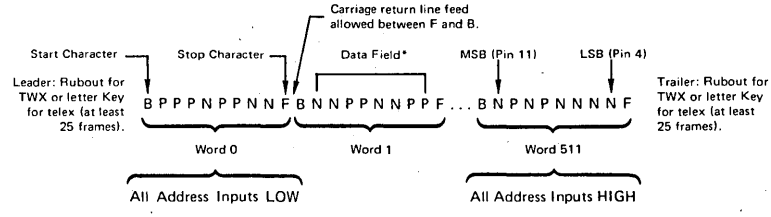
Contact the local sales office for further information. There are also several commercial programmers available such as the Data I/O Model V.

Most National distributors have programming capabilities available. Those distributors should be contacted directly to determine which data entry formats are available.

In addition, data may be submitted to National Semiconductor for factory programming. One of the following formats should be observed:

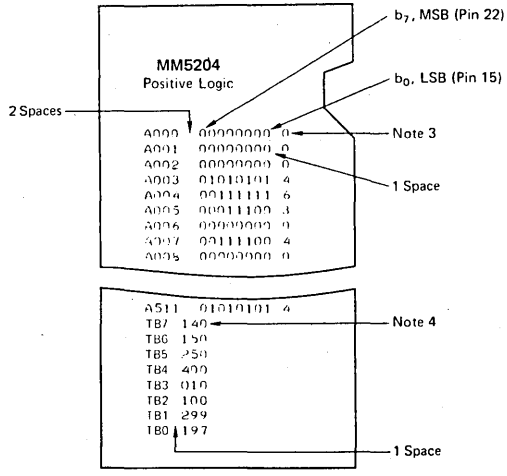
Preferred Format

The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7-bit ASCII code from model 33 teletype or TWX. The paper tape should be as the following example:



*Data Field: Must have only P's or N's typed between B and F. No nulls or rubouts. Must have exactly eight P and N characters between B and F. Any characters except B and F may be typed between the F stop character and the B start character. If an error is made in preparing a tape the entire word including the B and F start and stop characters must be rubbed out. Data for exactly 512 words must be entered beginning with word 0.

Alternate Format [Punched Tape (Note 1) or Cards]



Note 1: The code is a 7-bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the latter A.

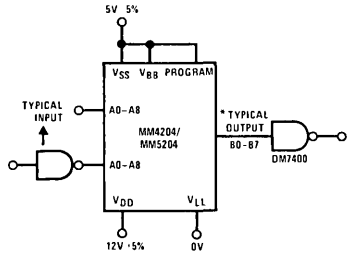
Note 3: The total number of "1" bits in the output word.

Note 4: The total number of "1" bits in each output column or bit position.

Erasing Procedure

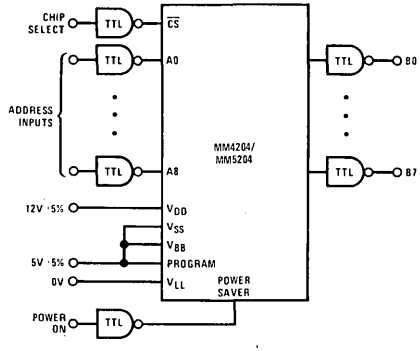
The MM4204Q/MM5204Q may be erased by exposure to short-wave ultraviolet light—253.7 nm. There exists no absolute rule for erasing time or distance from source. The erasing equipment output capability should be calibrated. Establish a worse case time required with the equipment. Then over-erase by a factor of 2, i.e., if the device appears erased after 8 minutes, continue exposure for an additional 16 minutes for a total of 24 minutes. Examples of UV sources include the Model UVS-54 and Model S-52 manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters. The MM4204/MM5204 should be placed about one inch away from the lamp for about 20—30 minutes.

AC Test Circuit

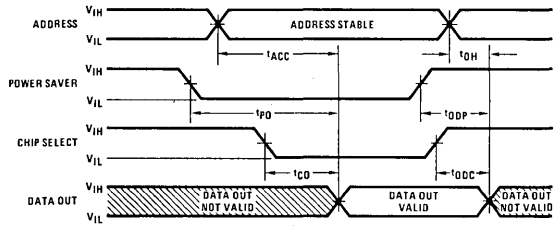


*t_{ACC}, t_{OH}, t_{CD}, and t_{OD} measured at output of MM4204/MM5204.

Typical Application



Switching Time Waveforms



Note. All times measured with respect to 1.5V level with t_r and $t_f \leq 20$ ns

FIGURE 1. Read Operation

Programming Waveforms

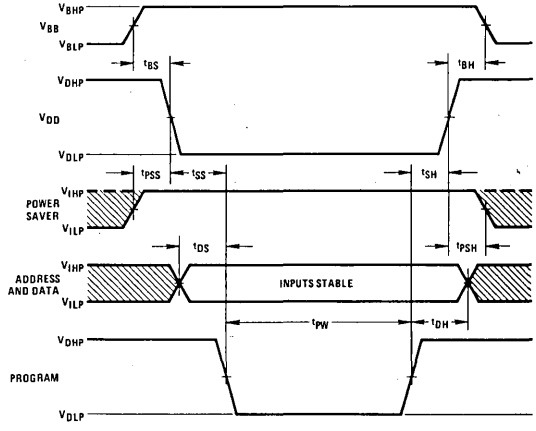


FIGURE 2. Programming Waveforms

5

National Semiconductor

MOS EPROMs

MM5204-1 4096-Bit (512 x 8) UV Erasable PROM

General Description

The MM5204-1 is a 4096-bit static Read Only Memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as 512 words by 8 bits per word. Programming of the memory is accomplished by storing a charge in a cell location by applying a −50V pulse. A logic input, "Power Saver", is provided which gives a 5:1 decrease in power when the memory is not being accessed.

- Static operation—no clock required
- Easy memory expansion—TRI-STATE® output Chip Select input ($\overline{CS}$)
- "Q" quartz lid version erasable with short wave ultraviolet light (i.e., 253.7 nm)
- Low power dissipation
- "Power Saver" control for low power applications
- Compatible with SC/MP II N-channel microprocessor

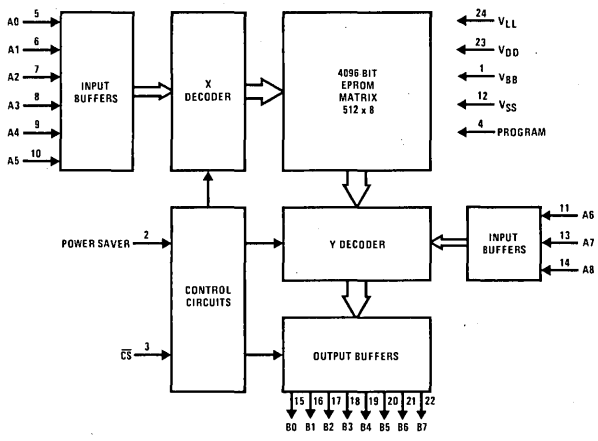
Features

- Field programmable
- Fast program time: ten seconds typical for 4096 bits
- Fast access time
  - MM5204-1 700 ns
- DTL/TTL compatibility
- Standard power supplies 5V, −12V

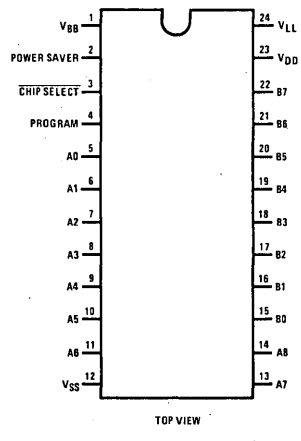
Applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming
- Electronic keyboards

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5204Q-1
See NS Package J24CQ

Absolute Maximum Ratings (Note 1)

All Input or Output Voltages with Respect to V_{BB} Except During Programming	+0.3V to −20V
Power Dissipation	750 mW
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

T_A = 0°C, to +70°C, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, V_{SS} = 5V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
V_{IL}	Input Low Voltage		V_{SS}−14		V_{SS}−4.2	V
V_{IH}	Input High Voltage		V_{SS}−1.5		V_{SS}+0.3	V
I_{LI}	Input Current	V_{IN} = 0V			1.0	μA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	V_{LL}		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −0.8 mA	2.4		V_{SS}	V
I_{LO}	Output Leakage Current	V_{OUT} = 0V, $\overline{CS}$ = V_{IH}			1.0	μA
I_{DD}	Power Supply Current	T_A = 0°C, $\overline{CS}$ = V_{IH},				
		Power Saver = V_{IL}		28	40.0	mA
		Power Saver = V_{IH}		6.0	8.0	mA
I_{SS}	V_{SS} Current	T_A = 0°C, $\overline{CS}$ = V_{IH}				
		Power Saver = V_{IL}			42	mA
		Power Saver = V_{IH}			10	mA

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{LL} = 0V, V_{BB} = PROGRAM = V_{SS}, V_{SS} = 5V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

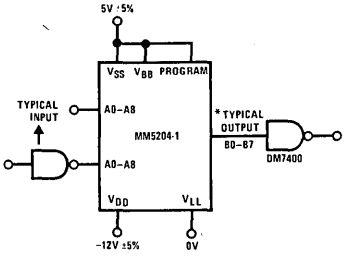
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
t_{ACC}	Access Time	T_A = 70°C, *(Figure 1)*			700	ns
t_{PO}	Power Saver Set-Up Time	*(Figure 1)*			1.4	μs
t_{CO}	Chip Select Delay	*(Figure 1)*			250	ns
t_{OH}	Data Hold Time	*(Figure 1)*	30	50		ns
t_{ODC}	Chip Select Deselect Time	*(Figure 1)*	30	200	500	ns
t_{ODP}	Power Saver Deselect Time	*(Figure 1)*	30	200	500	ns
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = V_{SS}, f = 1.0 MHz, (Note 3)		5.0	8.0	pF
C_{OUT}	Output Capacitance (All Outputs)	V_{OUT} = V_{SS}, $\overline{CS}$ = V_{IH}, f = 1.0 MHz, (Note 3)		8.0	15	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Typical values are for nominal voltages and T_A = 25°C, unless otherwise specified.

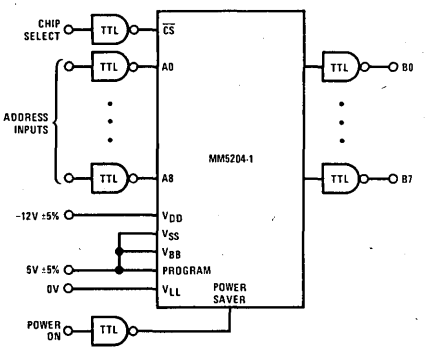
Note 3: Capacitance is guaranteed by periodic testing.

AC Test Circuit

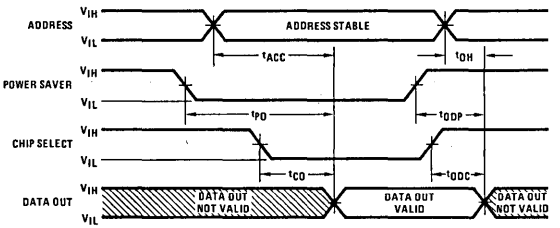


*t_{ACC}, t_{OH}, t_{CD} and t_{OD} measured at output of MM5204-1

Typical Application



Switching Time Waveforms



Note. All times measured with respect to 1.5V level with t_r and $t_f \leq 20$ ns

FIGURE 1. Read Operation

Programming Information

Refer to the MM4204/MM5204 data sheet for programming information.

National Semiconductor

MOS EPROMs
ADVANCE INFORMATION

NMC2532 32k-Bit (4k x 8) UV Erasable PROM

General Description

The NMC2532 is a 32,768-bit EPROM operating from a single 5V power supply. This device is an ultraviolet erasable, electrically programmable, read only memory fabricated using National's high speed, low power, silicon gate technology.

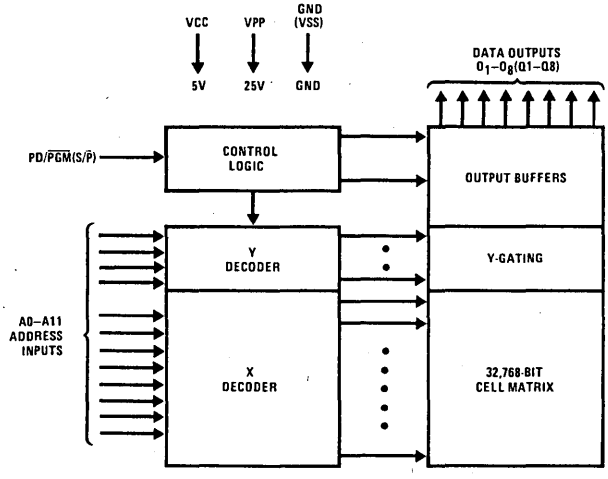
This device is deselected when pin 20 is high and automatically placed in the standby mode. This mode provides an 85% reduction in power with no increase in access time.

Bits may be programmed at random, in sequence or singly. Typical erasure time is 20 minutes using a 12 mW/cm^2 ultraviolet lamp.

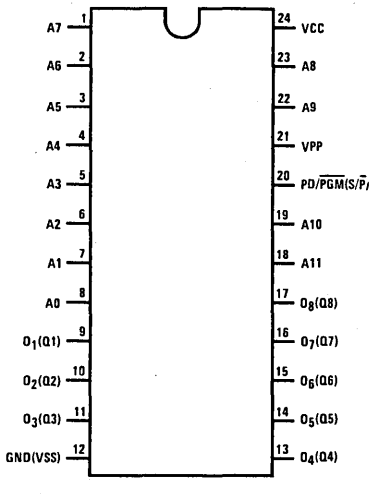
Features

- Single 5V power supply
- 450 ns max access time
- Low power:
  Active — 160 mA max
  Standby — 25 mA max
- Fully static
- TRI-STATE® output
- All I/O pins TTL compatible
- Pin compatible with existing EPROMs and ROMs
- Single location programming

Block and Connection Diagrams*



Dual-In-Line Package



TOP VIEW

Order Number NMC2532Q
See NS Package J24CQ

Modes*

Mode	Pin Name/Number			
	PD/PGM (S/P) 20	VPP 21	VCC 24	Outputs 9-11, 13-17
Read	VIL	5V	5V	DOUT
Standby	VIH	5V	5V	Hi-Z
Program	Pulsed VIH to VIL	25V	5V	DIN
Program Verify	VIL	5V	5V	DOUT
Program Inhibit	VIH	25V	5V	Hi-Z

Pin Names*

PD/PGM (S/P)	Power Down (Chip Select)
A0-A11	Address Inputs
O1-O8(Q1-Q8)	Data Outputs
VPP	Program Power (25V)
VCC	Power (5V)
GND (VSS)	Ground

* Symbols in parentheses are proposed industry standard.

Absolute Maximum Ratings (Note 1)

Temperature under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input and Output Voltages with Respect to VSS During Read	+6V to −0.3V
VPP Supply Voltage with Respect to VSS During Programming	+26.5V to −0.3V
Power Dissipation	1.5W
Lead Temperature (Soldering, 10 seconds)	300°C

READ OPERATION

DC Operating Characteristics (Note 2)

TA = 0°C to 70°C, VCC = 5V ± 5%, VSS = 0V, VPP = VCC ± 0.6V (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ILI	Input Load Current	VIN = 5.25V			10	μA
ILO	Output Leakage Current	VOUT = 5.25V			10	μA
ICC1	VCC Current Standby	PD/$\overline{PGM}$ (S/$\overline{P}$) = VIH		15	25	mA
ICC2	VCC Current Active	PD/$\overline{PGM}$ (S/$\overline{P}$) = VIL		85	160	mA
VIL	Input Low Voltage		−0.1		0.65	V
VIH	Input High Voltage		2.2		VCC+1	V
VOL	Output Low Voltage	IOL = 2.1 mA			0.45	V
VOH	Output High Voltage	IOH = −400 μA	2.4			V
IPP1/IPP2	VPP Standby/Active Current				300	μA

AC Characteristics

TA = 0°C to 70°C, VCC = 5V ± 5%, VSS = 0V, VPP = VCC ± 0.6V (Note 3)

Symbol		Parameter	Conditions	Min	Max	Units
Alternate	Standard					
t_{ACC}	TAVQV	Address to Output Valid	PG/$\overline{PGM}$ = VIL		450	ns
t_{APR}	TSLQV	Select to Output Valid			450	ns
t_{PXZ}	TSHQZ	Select to Output Hi-Z		0	100	ns
t_{PVX}	TAXQX	Address to Output Hold	PD/$\overline{PGM}$ = VIL	0		ns

Capacitance (Note 4) TA = 25°C, f = 1 MHz

Symbol	Parameter	Conditions	Typ	Max	Units
CIN	Input Capacitance	VIN = 0V	4	6	pF
COUT	Output Capacitance	VOUT = 0V	8	12	pF

AC Test Conditions

Output Load: 1 TTL gate and CL = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Recommended DC Operating Conditions" provides conditions for actual device operation.

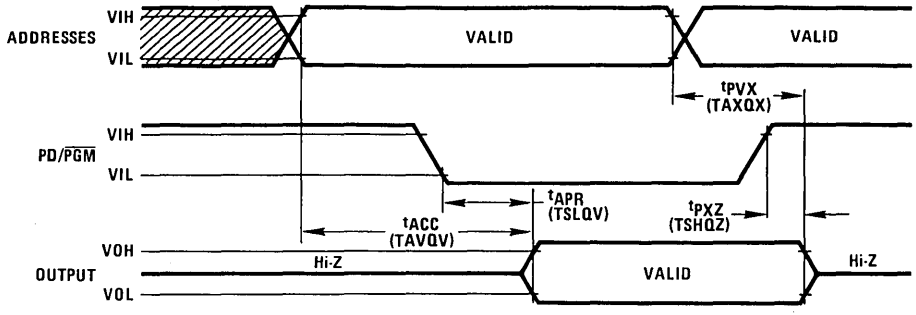
Note 2: Typical values are for TA = 25°C and nominal supply voltages.

Note 3: VPP can be tied directly to VCC (except during programming).

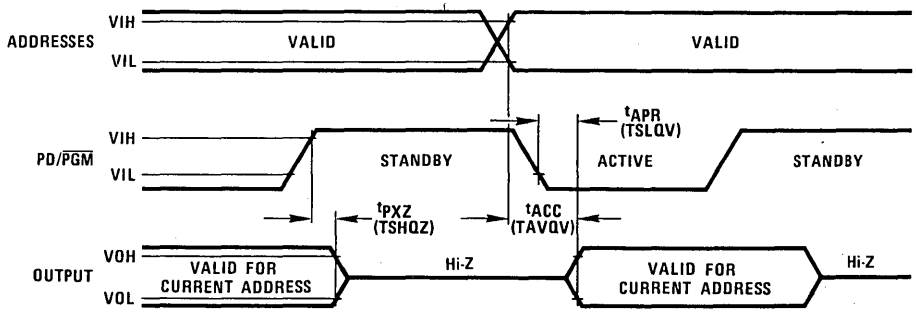
Note 4: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation C = IΔt/ΔV. Capacitance is guaranteed by periodic testing.

Switching Time Waveforms*

Read Cycle



Standby Power Down Mode



* Symbols in parentheses are proposed industry standard.

PROGRAM OPERATION

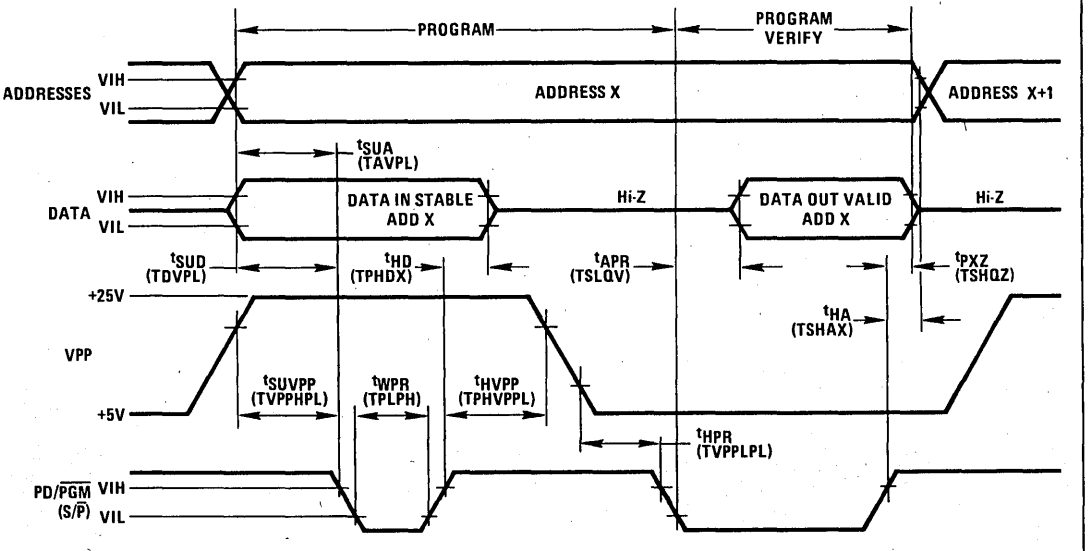
DC Characteristics $T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ILI	Input Current All Inputs	VIN = VIL or VIH			10	μA
VOL	Output Low Voltage During Verify	IOL = 2.1 mA			0.45	V
VOH	Output High Voltage During Verify	IOH = −400 μA	2.4			V
ICC	VCC Supply Current			85	160	mA
VIL	Input Low Level All Inputs		−0.1		0.65	V
VIH	Input High Level All Inputs Except VPP		2.2		VCC + 1	V
IPP	VPP Supply Current	PD/$\overline{PGM}$ (S/$\overline{P}$) = VIL			30	mA

AC Characteristics $T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$

Symbol		Parameter	Min	Typ	Max	Units
Alternate	Standard					
t_{SUA}	TAVPL	Address Set-Up Time	2			μs
t_{SUD}	TDVPL	Data Set-Up Time	2			μs
t_{SUVPP}	TVPPHPL	VPP Set-Up Time	0			ns
t_{WPR}	TPLPH	Program Pulse Width	45	50	55	ms
t_{HD}	TPHDX	Data Hold Time	2			μs
t_{HVPP}	TPHVPPL	VPP Hold Time	0			ns
t_{HPR}	TVPPLPL	VPP Recovery Time	0			ns
t_{APR}	TSLQV	Select to Output Valid			450	ns
t_{HA}	TSHAX	Address Hold Time	0			ns
t_{PXZ}	TSHQZ	Select to Output Hi-Z	0		100	ns

Programming Waveforms* (Note 5) $T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$



Note 5: The Input timing reference level is 0.65V for VIL and 2.2V for VIH.
* Symbols in parentheses are proposed industry standard.

Functional Description

DEVICE OPERATION

The NMC2532 has two modes of operation in the normal system environment. These are shown in Table I.

TABLE I. OPERATING MODES (VCC = 5V)*

Mode \ Pins	PD/$\overline{PGM}$ (S/$\overline{P}$) 20	ICC Max 24	Outputs 9-11, 13-17
Read	VIL	160 mA	DOUT
Standby	VIH	25 mA	Hi-Z

Read Mode

The NMC2532 read operation requires that PD/$\overline{PGM}$ = VIL and that addresses A0-A11 have been stabilized. Valid data will apear on the output pins after t_{ACC} or t_{APR} times (see Switching Time Waveforms) depending on which is limiting.

Standby Mode

The NMC2532 is placed in the standby mode (deselected and powered down) by making PD/$\overline{PGM}$ = VIH. This automatically controls the outputs to their Hi-Z state. The power dissipation is reduced to 15% of the normal operating power. VCC must be kept at 5V. Access time at power up (chip selection) remains either t_{ACC} or t_{APR} (see Switching Time Waveforms).

PROGRAMMING

The NMC2532 is shipped from National completely erased. All bits will be at a "1" level (outputs high) in this initial state after any full erasure. Table II shows the three programming modes.

TABLE II. PROGRAMMING MODES (VCC = 5V)*

Mode \ Pins	PD/$\overline{PGM}$ (S/$\overline{P}$) 20	VPP 18	Outputs 9-11, 13-17
Program	VIL	25V	DIN
Program Verify	VIL	5V	DOUT
Program Inhibit	VIH	25V	Hi-Z

Program Mode

The NMC2532 is programmed by placing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, a sequence of addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the PD/$\overline{PGM}$ (S/$\overline{P}$) pin. All input voltage levels, including the program pulse on the PD/$\overline{PGM}$ pin are TTL compatible. The programming sequence is:

With the VPP pin at 25V and VCC = 5V, an address is selected and the desired data word is applied to the output pins (VIL = "0" and VIH = "1" for both address and data). After the address and data signals are stable the PD/$\overline{PGM}$ pin is pulsed from VIH to VIL with a pulse width between 45 ms and 55 ms.

Multiple pulses are not needed but will not cause device damage. No pins should be left open. A low level, VIL or lower *must not* be maintained steady state (DC signal) on the PD/$\overline{PGM}$ pin during programming. Several NMC2532s may be programmed in parallel (the same data in each one) in this mode.

Program Verify

The programming of the NMC2532 may be verified, either one word at a time during the programming (as shown in the timing diagram) or by reading all of the words out at the end of the programming sequence.

Program Inhibit

The program inhibit mode allows programming several NMC2532s in parallel with different data for each one by controlling which ones receive the program pulse. All similar inputs may be paralleled. Pulsing the PD/$\overline{PGM}$ pin from VIH to VIL on a selected unit or units will cause programming, while inhibiting the PD/$\overline{PGM}$ pulse will inhibit programming and keep the outputs of the inhibited devices in the Hi-Z state.

ERASURE PROCEDURE

The NMC2732 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gates to their initial state through induced photo current. It is recommended that this device be kept out of direct sunlight. The UV content of sunlight may cause the a partial erasure of some bits in a relatively short period of time. Direct sunlight (any intense light) can cause temporary functional failure due to generation of photo current. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label etc.) should be placed over the package window if this product is to be operated under these lighting conditions.

An ultraviolet source of 2537Å yielding a total integrated dosage of 15 Watt-seconds/cm^2 is required. This will erase a unit in approximately 15 to 20 minutes when a UV lamp of a 12 mW/cm^2 power rating is used. The NMC2532 to be erased should be placed one inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

* Symbols in parentheses are proposed industry standard.

National Semiconductor

MOS EPROMs
PREVIEW

NMC2564 64k-Bit (8k × 8) UV Erasable PROM

General Description

The NMC2564 is a 65,536-bit EPROM operating from a single 5V power supply. This device is an ultraviolet erasable, electrically programmable, read only memory fabricated using National's high speed, low power, silicon gate technology.

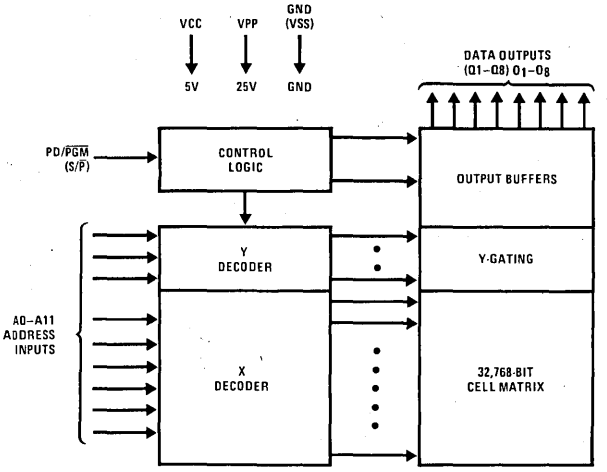
This device is deselected when pin 20 is high and automatically placed in the standby mode. This mode provides an 85% reduction in power with no increase in access time.

Bits may be programmed at random, in sequence or singly. Typical erasure time is 20 minutes using a 12 mW/cm^2 ultraviolet lamp.

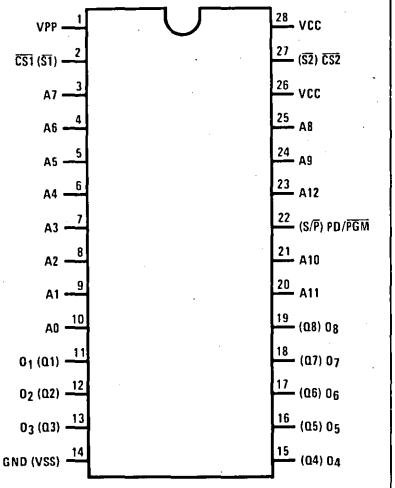
Features

- Single 5V power supply
- 450 ns max access time
- Low power:
  Active — 200 mA max
  Standby — 30 mA max
- Fully static
- TRI-STATE® output
- All I/O pins TTL compatible
- Pin compatible with the 2516 and 2532 EPROMs
- Separate chip selects for multiple bus systems
- Single location programming

Block and Connection Diagrams*



Dual-In-Line Package



TOP VIEW

Modes

Mode	Pin Name/Number					
	VCC 26, 28	VPP 1	PD/PGM (S/P) 22	CS1 (S1) 2	CS2 (S2) 27	Outputs (Q1-Q8) 11-13, 15-19
Read	5	5	VIL	VIL	VIL	DOUT
Deselect	5	5	VIL	VIH	X	Hi-Z
Deselect	5	5	VIL	X	VIH	Hi-Z
Standby	5	5	VIH	X	X	Hi-Z
Program Inhibit	5	25	VIH	X	X	DIN
Program Inhibit	5	25	X	VIH	X	DIN
Program Inhibit	5	25	X	X	VIH	DIN
Program	5	25	Pulsed VIH to VIL	VIL	VIL	DIN

X = don't care

* Symbols in parentheses are industry standard

Pin Names

PD/PGM (S/P)	Power Down (Chip Select)
A0-A12	Address Inputs
O_1-O_8 (Q1-Q8)	Data Outputs
VPP	Program Power (+25V)
VCC	Power (+5V)
GND (VSS)	Ground

National Semiconductor

MOS EPROMs
PREVIEW

NMC27C16 16,384-Bit (2048 x 8) UV Erasable CMOS PROM

General Description

The NMC27C16 is a high speed 16k UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

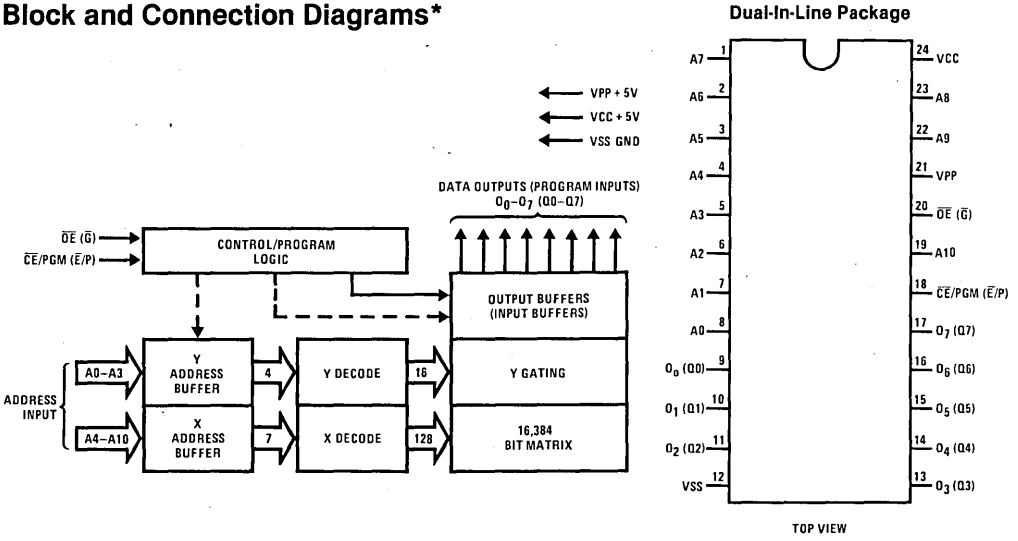
The NMC27C16 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This ERPOM is fabricated with the reliable, high volume, time proven, CMOS silicon gate technology.

Features

- 2048 x 8 organization
- Low power during programming
- Access time—450 ns
- Single 5V power supply
- Static—no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- TRI-STATE® output

Block and Connection Diagrams*



Dual-In-Line Package

TOP VIEW

Pin Connection During Read or Program

Mode	Pin Name/Number				
	CE/PGM (E/P) 18	OE (G) 20	VPP 21	VCC 24	Outputs 9-11, 13-17
Read	VIL	VIL	5	5	DOUT
Program	Pulsed VIL to VIH	VIH	25	5	DIN

Pin Names

A0-A10	Addres Inputs
O_0-O_7(Q0-Q7)	Data Outputs
CE/PGM (E/P)	Chip Enable/Program
OE (G)	Output Enable
VPP	Read 5V, Program 25V
VCC	Power 5V
VSS	Ground

* Symbols in parentheses are proposed industry standard.

5

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−25°C to +85°C
Storage Temperature	−65°C to +125°C
VPP Supply Voltage with Respect to VSS	26.5V to −0.3V
All Input or Output Voltages with Respect to VSS (except VPP)	VCC + 0.3V to −0.3V
Power Dissipation	1.5W
Lead Temperature (Soldering, 10 seconds)	300°C

READ OPERATION

DC Operating Characteristics TA = 0°C to +70°C, VCC = 5V ± 5%, (VCC = 5V ± 10% for NMC27C16-1), VPP = VCC ± 0.6V (Note 3), VSS = 0V, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ILI	Input Current	VIN = 5.25V or VIN = VIL			10	μA
ILO	Output Leakage Current	VOUT = 5.25V, $\overline{CE}$/PGM = 5V			10	μA
IPP1	VPP Supply Current	VPP = 5.85V			5	mA
ICC1	VCC Supply Current (Standby)	$\overline{CE}$/PGM = VIH, $\overline{OE}$ = VIL		10	25	mA
ICC2	VCC Supply Current (Active)	$\overline{CE}$/PGM = $\overline{OE}$ = VIL		57	100	mA
VIL	Input Low Voltage		−0.1		0.8	V
VIH	Input High Voltage		2.0		VCC + 1	V
VOH	Output High Voltage	IOH = −400 μA	2.4			V
VOL	Output Low Voltage	IOL = 2.1 mA			0.45	V

AC Characteristics (Note 2) TA = 0°C to +70°C, VCC = 5V ± 5%, (VCC = 5V ± 10% for NMC27C16-1), VPP = VCC ± 0.6V (Note 3), VSS = 0V, unless otherwise noted.

Symbol		Parameter	Conditions	NMC27C16		NMC27C16-1		NMC27C16-2		Units
Alternate	Standard			Min	Max	Min	Max	Min	Max	
t_{ACC}	TAVQV	Address to Output Delay	$\overline{CE}$/PGM = $\overline{OE}$ = VIL		450		350		390	ns
t_{CE}	TELQV	$\overline{CE}$ to Output Delay	$\overline{OE}$ = VIL		450		350		390	ns
t_{OE}	TGLQV	Output Enable to Output Delay	$\overline{CE}$/PGM = VIL		120		120		120	ns
t_{DF}	TGHQZ	Output Enable High to Output Hi-Z	$\overline{CE}$/PGM = VIL	0	100	0	100	0	100	ns
t_{OH}	TAXQX	Address to Output Hold	$\overline{CE}$/PGM = $\overline{OE}$ = VIL	0		0		0		ns
t_{OD}	TEHQZ	$\overline{CE}$ to Output Hi-Z	$\overline{OE}$ = VIL	0	100	0	100	0	100	ns

Capacitance TA = 25°C, f = 1 MHz

Symbol	Parameter	Conditions	Typ	Max	Units
CI	Input Capacitance	VIN = 0V	4	6	pF
CO	Output Capacitance	VOUT = 0V	8	12	pF

AC Test Conditions

Output Load: 1 TTL gate and CL = 100 pF
Input Rise and Fall Times: ≤20 ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

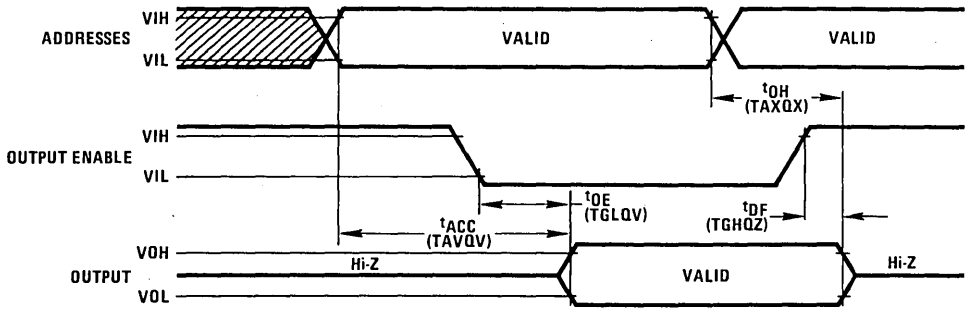
Note 2: Typical conditions are for operation at: TA = 25°C, VCC = 5V, VPP = VCC, and VSS = 0V.

Note 3: VPP may be connected to VCC except during program. The ± 0.6V tolerance allows a circuit to switch VPP between the read voltage and the program voltage.

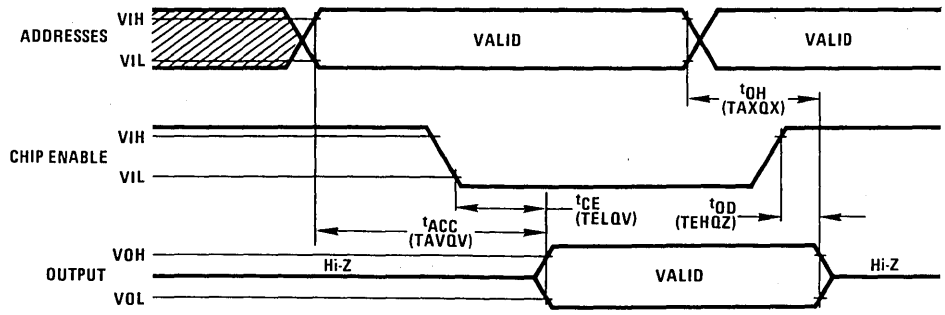
Note 4: Capacitance is guaranteed by periodic testing. TA = 25°C, f = 1 MHz.

Switching Time Waveforms *

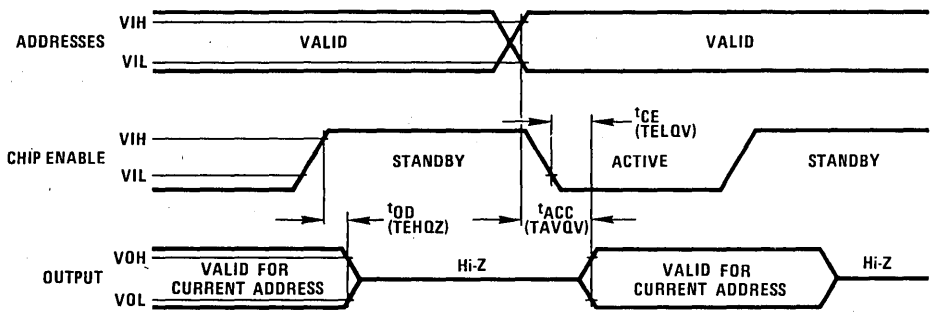
Read Cycle ($\overline{CE}$/PGM = VIL)



Read Cycle ($\overline{OE}$ = VIL)



Standby Power Down Mode ($\overline{OE}$ = VIL)



* Symbols in parentheses are proposed industry standard.

PROGRAM OPERATION

DC Electrical Characteristics and Operating Conditions (Notes 1 and 2)

(TA = 25°C ± 5°C) (VCC = 5V ± 5%, VPP = 25V ± 1V)

Symbol	Parameter	Min	Typ	Max	Units
ILI	Input Leakage Current (Note 3)			10	μA
VIL	Input Low Level	−0.1		0.8	V
VIH	Input High Level	2.0		VCC + 1	V
ICC	VCC Power Supply Current			100	mA
IPP1	VPP Supply Current (Note 4)			5	mA
IPP2	VPP Supply Current During Programming Pulse (Note 5)			30	mA

AC Characteristics and Operating Conditions (Notes 1, 2, and 6)

(TA = 25°C ± 5°C) (VCC = 5V ± 5%, VPP = 25V ± 1V)

Symbol		Parameter	Min	Typ	Max	Units
Alternate	Standard					
t_{AS}	TAVPH	Address Set-up Time	2			μs
t_{OS}	TGHPH	$\overline{OE}$ Set-up Time	2			μs
t_{DS}	TDVPH	Data Set-up Time	2			μs
t_{AH}	TPLAX	Address Hold Time	2			μs
t_{OH}	TPLGX	$\overline{OE}$ Hold Time	2			μs
t_{DH}	TPLDX	Data Hold Time	2			μs
t_{DF}	TGHQZ	Chip Disable to Output Float Delay (Note 4)	0		130	ns
t_{CE}	TGLQV	Chip Enable to Output Delay (Note 4)			150	ns
t_{PW}	TPHPL	Program Pulse Width	45	50	55	ms
t_{PR}	TPH1PH2	Program Pulse Rise Time	5			ns
t_{PF}	TPL2PL1	Program Pulse Fall Time	5			ns

Note 1: VCC must be applied at the same time or before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be inserted into a board with power applied.

Note 2: Care must be taken to prevent overshoot of the VPP supply when switching to +25V.

Note 3: 0.45V ≤ VIN ≤ 5.25V

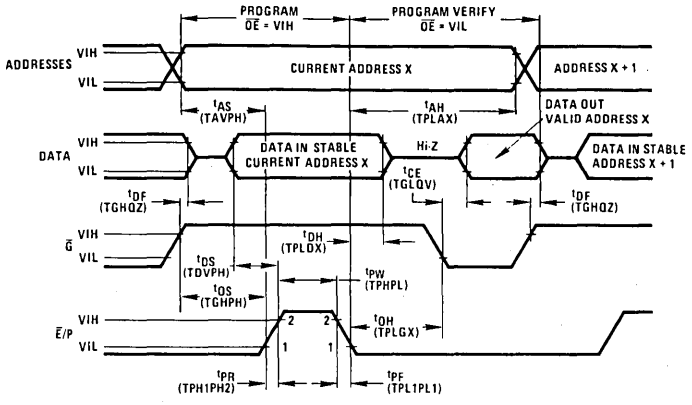
Note 4: $\overline{CE}$/PGM = VIL, VPP = VCC

Note 5: VPP = 26V

Note 6: Transition times ≤ 20 ns unless noted otherwise.

Timing Diagram *

Program Mode



Functional Description

DEVICE OPERATION

The NMC27C16 has 3 modes of operation in the normal system environment. These are shown in Table I.

Read Mode

The NMC27C16 read operation requires that $\overline{OE}$ = VIL, $\overline{CE}$/PGM = VIL and that addresses A0–A10 have been stabilized. Valid data will appear on the output pins after t_{ACC}, t_{OE} or t_{CE} times (see Switching Time Waveforms) depending on which is limiting.

Deselect Mode

The NMC27C16 is deselected by making $\overline{OE}$ = VIH. This mode is independent of $\overline{CE}$/PGM and the condition of the addresses. The outputs are Hi-Z when $\overline{OE}$ = VIH. This allows OR-tying 2 or more NMC27C16's for memory expansion.

Standby Mode (Power Down)

The NMC27C16 may be powered down to the standby mode by making $\overline{CE}$/PGM = VIH. This is independent of $\overline{OE}$ and automatically puts the outputs in their Hi-Z state. The power is reduced to 25% (132 mW max) of the normal operating power. VCC and VPP must be maintained at 5V. Access time at power up remains either t_{ACC} or t_{CE} (see Switching Time Waveforms).

PROGRAMMING

The NMC27C16 is shipped from National completely erased. All bits will be at a "1" level (output high) in this initial state and after any full erasure. Table II shows the 3 programming modes.

TABLE I. OPERATING MODES (VCC = VPP = 5V)

Mode	Pin Name/Number		
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	Outputs 9–11, 13–17
Read	VIL	VIL	DOUT
Deselect	Don't Care	VIH	Hi-Z
Standby	VIH	Don't Care	Hi-Z

TABLE II. PROGRAMMING MODES (VCC = 5V)

Mode	Pin Name/Number			
	$\overline{CE}$/PGM ($\overline{E}$/P) 18	$\overline{OE}$ ($\overline{G}$) 20	VPP 21	Outputs Q 9–11, 13–17
Program	Pulsed VIL to VIH	VIH	25	DIN
Program Verify	VIL	VIL	25(5)	DOUT
Program Inhibit	VIL	VIH	25	Hi-Z

* Symbols in parentheses are proposed industry standard

Functional Description (Continued)

Program Mode

The NMC27C16 is programmed by introducing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, a sequence of addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the chip enable pin. All input voltage levels, including the program pulse on chip enable are TTL compatible. The programming sequence is:

With VPP = 25V, VCC = 5V, $\overline{OE}$ = VIH and $\overline{CE}$/PGM = VIL, an address is selected and the desired data word is applied to the output pins. (VIL = "0" and VIL = "1" for both address and data.) After the address and data signals are stable the program pin is pulsed from VIL to VIH with a pulse width between 45 ms and 55 ms.

Multiple pulses are not needed but will not cause device damage. No pins should be left opmn. A high level (VIH or higher) *must not* be maintained longer than $t_{PW(MAX)}$ on the program pin during programming. NMC27C16s may be programmed in parallel with the same data in this mode.

Program Verify Mode

The programming of the NMC27C16 may be verified either 1 word at a time during the programming (as shown in the timing diagram) or by reading all of the words out at the end of the programming sequence. This can be done with VPP = 25V (or 5V) in either case.

Program Inhibit Mode

The program inhibit mode allows programming several NMC27C16s simultaneously with different data for each one by controlling which ones receive the program pulse. All similar inputs of the NMC27C16 may be paralleled. Pulsing the program pin (from VIL to VIH) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{OE}$ = VIH will put its outputs in the Hi-Z state.

ERASING

The NMC27C16 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the NMC27C16 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time. Direct sunlight can also cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc.) should be placed over the package window if this product is to be operated under these lighting conditions.

An ultraviolet source of 2537Å yielding a total integrated dosage of 15 watt-seconds/cm^2 is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a 12,000 $\mu W/cm^2$ power rating is used. The NMC27C16 to be erased should be placed 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1 inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance is changed, or the lamp is aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

National Semiconductor

MOS EPROMs
PRELIMINARY

NMC2724 16k-Bit (2k x 8) UV Erasable PROM

General Description

The NMC2724 is a 16,384-bit EPROM operating from a single 5V power supply. This device is an ultraviolet erasable, electrically programmable, read only memory fabricated using National's high speed, low power, silicon gate technology.

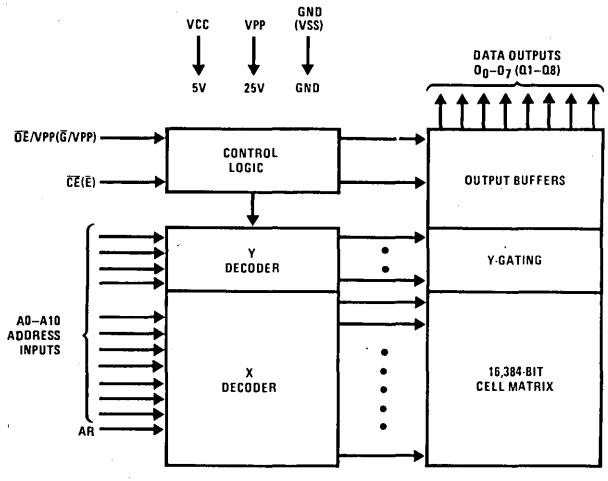
This device is deselected when pin 18 is high and automatically placed in the standby mode. This mode provides an 80% reduction in power with no increase in access time. The NMC2724 has an output enable control to eliminate bus contention in microprocessor systems.

Bits may be programmed at random, in sequence or singly. Typical erasure time is 20 minutes using a 12 mW/cm^2 ultraviolet lamp.

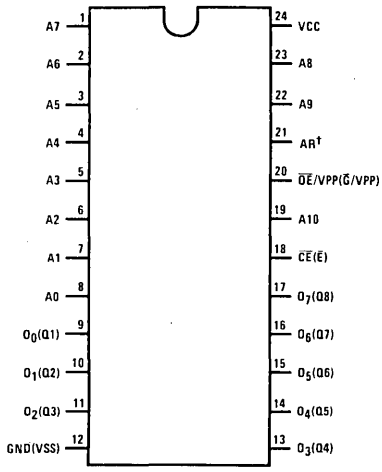
Features

- Single 5V power supply
- 450 ns max access time
- Low power:
  Active—150 mA max
  Standby—30 mA max
- Fully static
- TRI-STATE® output
- All I/O pins TTL compatible
- Pin compatible with existing EPROMs and ROMs
- Output enable control

Block and Connection Diagrams*



Dual-In-Line Package



TOP VIEW

Modes*

Mode	Pin Name/Number			
	$\overline{CE}$ ($\overline{E}$) 18	$\overline{OE}$/VPP ($\overline{G}$/VPP) 20	VCC 24	Outputs 9-11, 13-17
Read	VIL	VIL	5V	DOUT
Standby	VIH	Don't Care	5V	Hi-Z
Program	VIL	25V	5V	DIN
Program Verify	VIL	VIL	5V	DOUT
Program Inhibit	VIH	25V	5V	Hi-Z

Order Number NMC2724Q-A or NMC2724Q-B
See NS Package J24CQ

Pin Names*

$\overline{CE}$ ($\overline{E}$)	Chip Enable
$\overline{OE}$ ($\overline{G}$)	Output Enable
A0-A10	Address Inputs
O_0-O_7 (Q1-Q8)	Data Outputs
VPP	Program Power 25V
VCC	Power 5V
GND (VSS)	Ground
AR	Select Reference Input Level

* Symbols in parentheses are proposed industry standard.

†NMC2724A, AR ≤ VIL for all operating modes.
NMC2724B, AR ≥ VIH for all operating modes.

Absolute Maximum Ratings (Note 1)

Temperature under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input and Output Voltages with Respect to VSS During Read	+6V to −0.3V
VPP Supply Voltage with Respect to VSS During Programming	+26.5V to −0.3V
Power Dissipation	1.5W
Lead Temperature (Soldering, 10 seconds)	300°C

READ OPERATION

DC Operating Characteristics (Note 2) TA = 0°C to 70°C, VCC = 5V ± 5%, VSS = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ILI1	Input Load Current	VIN = 5.25V			10	μA
ILI2	$\overline{OE}$/VPP Input Load Current	VIN = 5.25V			300	μA
ICC1	VCC Current Standby	$\overline{CE}$ = VIH, $\overline{OE}$ = VIL		15	30	mA
ICC2	VCC Current Active	$\overline{OE}$ = $\overline{CE}$ = VIL		85	150	mA
VIL	Input Low Voltage		−0.1		0.8	V
VIH	Input High Voltage		2.0		VCC+1	V
VOL	Output Low Voltage	IOL = 2.1 mA			0.45	V
VOH	Output High Voltage	IOH = −400 μA	2.4			V

AC Characteristics TA = 0°C to 70°C, VCC = 5V ± 5%, VSS = 0V

Symbol		Parameter	Conditions	Min	Typ	Max	Units
Alternate	Standard						
t_{ACC}	TAVQV	Address to Output Valid	$\overline{CE}$ = $\overline{OE}$ = VIL			450	ns
t_{CE}	TELQV	$\overline{CE}$ to Output Delay	$\overline{OE}$ = VIL			450	ns
t_{OE}	TGLQV	Output Enable to Output Delay	$\overline{CE}$ = VIL			120	ns
t_{DF}	TGHQZ	Output Enable High to Output Hi-Z	$\overline{CE}$ = VIL	0		100	ns
t_{OH}	TAXQX	Address to Output Hold	$\overline{CE}$ = $\overline{OE}$ = VIL	0			ns
t_{PF}	TEHQZ	$\overline{CE}$ ($\overline{E}$) to Output Hi-Z	$\overline{OE}$ = VIL	0		100	ns

Capacitance (Note 3) TA = 25°C, f = 1 MHz

Symbol	Parameter	Conditions	Typ	Max	Units
CIN1	Input Capacitance Except $\overline{OE}$/VPP ($\overline{G}$/VPP)	VIN = 0V	4	6	pF
CIN2	$\overline{OE}$/VPP ($\overline{G}$/VPP) Input Capacitance	VIN = 0V		20	pF
COUT	Output Capacitance	VOUT = 0V		12	pF

AC Test Conditions

Output Load: 1 TTL gate and CL = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

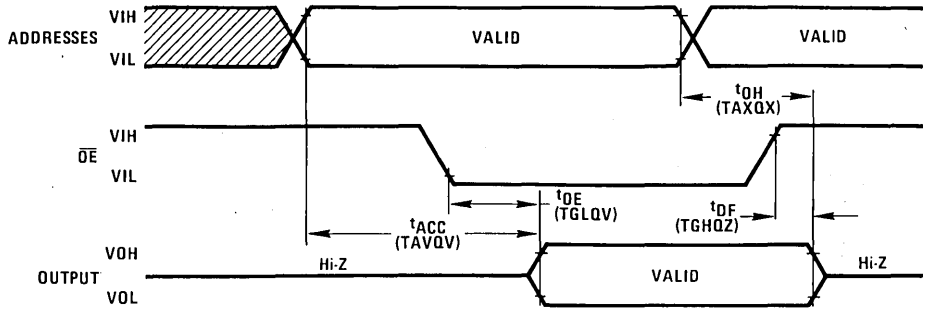
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Recommended DC Operating Conditions" provides conditions for actual device operation.

Note 2: Typical values are for TA = 25°C and nominal supply voltages.

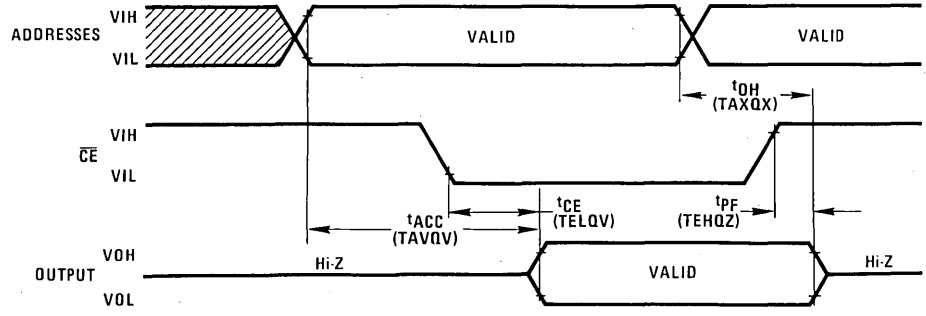
Note 3: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation C = IΔt/ΔV. Capacitance is guaranteed by periodic testing.

Switching Time Waveforms*

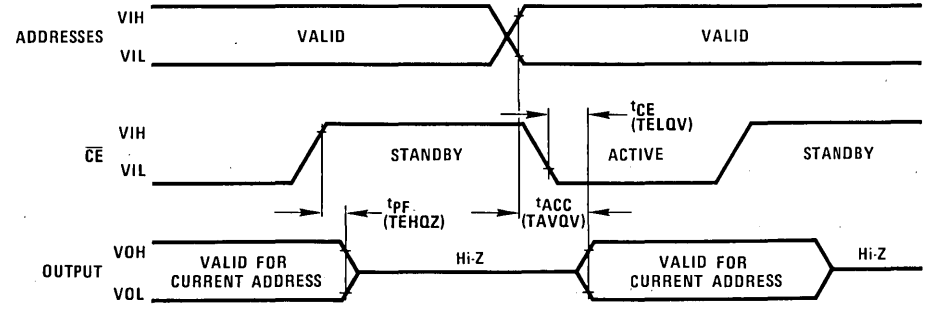
Read Cycle ($\overline{CE}$ = VIL)



Read Cycle ($\overline{OE}$ ($\overline{G}$) = VIL)



Standby Power Down Mode ($\overline{OE}$ = VIL)



* Symbols in parentheses are proposed industry standard.

PROGRAM OPERATION

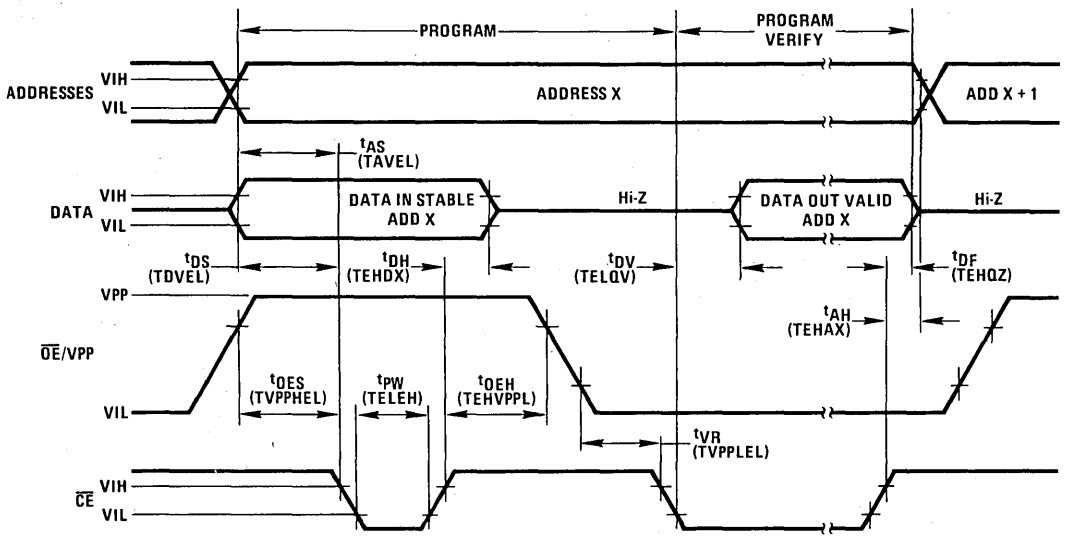
DC Characteristics $T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ILI	Input Current All Inputs	VIN = VIL or VIH			10	μA
VOL	Output Low Voltage During Verify	IOL = 2.1 mA			0.45	V
VOH	Output High Voltage During Verify	IOH = −400 μA	2.4			V
ICC	VCC Supply Current			85	150	mA
VIL	Input Low Level All Inputs		−0.1		0.8	V
VIH	Input High Level All Inputs Except $\overline{OE}$/VPP		2.0		VCC + 1	V
IPP	VPP Supply Current	$\overline{CE}$ = VIL, $\overline{OE}$ = VPP			30	mA

AC Characteristics $T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$

Symbol		Parameter	Conditions	Min	Typ	Max	Units
Alternate	Standard						
t_{AS}	TAVEL	Address Set-Up Time		2			μs
t_{OES}	TVPPHEL	Program Voltage Set-Up Time		2			μs
t_{DS}	TDVEL	Data Set-Up Time		2			μs
t_{AH}	TEHAX	Address Hold Time		0			μs
t_{OEH}	TEHVPPL	$\overline{OE}$ Hold Time		2			μs
t_{DH}	TEHDX	Data Hold Time		2			μs
t_{DF}	TEHQZ	Chip Enable to Output Hi-Z		0		120	ns
t_{DV}	TELQV	Data Valid from $\overline{CE}$	$\overline{OE}$ = VIL			1	μs
t_{PW}	TELEH	$\overline{CE}$ Pulse Width During Programming		45	50	55	ms
t_{VR}	TVPPLEL	VPP Recovery Time		2			μs

Programming Waveforms* (Note 4) $T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$



Note 4: The input timing reference level is 1V for VIL and 2V for VIH.

*Symbols in parentheses are proposed industry standard.

Functional Description

DEVICE OPERATION

The NMC2724 has two modes of operation in the normal system environment. These are shown in Table I.

TABLE I. OPERATING MODES (VCC = 5V)*

Mode \ Pins	$\overline{CE}$ ($\overline{E}$) 18	$\overline{OE}$/VPP ($\overline{G}$/VPP) 20	ICC Max 24	Outputs 9-11, 13-17
Read	VIL	VIL	150 mA	DOUT
Standby	VIH	Don't Care	30 mA	Hi-Z

Read Mode

The NMC2724 read operation requires that $\overline{CE}$ = VIL, and $\overline{OE}$/VPP = VIL and that addresses A0-A10 have been stabilized. Valid data will apear on the output pins after t_{ACC}, t_{OE}, or t_{CE} times (see Switching Time Waveforms) depending on which is limiting.

Standby Mode

The NMC2724 is placed in the standby mode (deselected and powered down) by making $\overline{CE}$ = VIH. This is independent of the Output Enable control and automatically controls the outputs to their Hi-Z state. The power dissipation is reduced to 20% of the normal operating power. VCC must be kept at 5V. Access time at power up (chip selection) remains either t_{ACC} or t_{CE} (see Switching Time Waveforms).

PROGRAMMING

The NMC2724 is shipped from National completely erased. All bits will be at a "1" level (outputs high) in this initial state after any full erasure. Table II shows the three programming modes.

TABLE II. PROGRAMMING MODES (VCC = 5V)*

Mode \ Pins	$\overline{CE}$ ($\overline{E}$) 18	$\overline{OE}$/VPP ($\overline{G}$/VPP) 20	Outputs 9-11, 13-17
Program	VIL	25V	DIN
Program Verify	VIL	VIL	DOUT
Program Inhibit	VIH	25V	Hi-Z

Program Mode

The NMC2724 is programmed by placing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, a sequence of addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the $\overline{CE}$ pin. All input voltage levels, including the program pulse on the $\overline{CE}$ pin are TTL compatible. The programming sequence is:

With the $\overline{OE}$/VPP pin at 25V and VCC = 5V, an address is selected and the desired data word is applied to the output pins (VIL = "0" and VIH = "1" for both address and data). After the address and data signals are stable the $\overline{CE}$ pin is pulsed from VIH to VIL with a pulse width between 45 ms and 55 ms.

Multiple pulses are not needed but will not cause device damage. No pins should be left open. A low level, VIL or lower *must not* be maintained steady state (DC signal) on the $\overline{CE}$ pin during programming. Several NMC2724s may be programmed in parallel (the same data in each one) in this mode.

Program Verify

The programming of the NMC2724 may be verified, either one word at a time during the programming (as shown in the timing diagram) or by reading all of the words out at the end of the programming sequence.

Program Inhibit

The program inhibit mode allows programming several NMC2724s in parallel with different data for each one by controlling which ones receive the program pulse. All similar inputs may be paralleled. Pulsing the $\overline{CE}$ pin from VIH to VIL on a selected unit or units will cause programming, while inhibiting the $\overline{CE}$ pulse will inhibit programming and keep the outputs of the inhibited devices in the Hi-Z state.

ERASURE PROCEDURE

The NMC2724 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gates to their initial state through induced photo current. It is recommended that this device be kept out of direct sunlight. The UV content of sunlight may cause the a partial erasure of some bits in a relatively short period of time. Direct sunlight (any intense light) can cause temporary functional failure due to generation of photo currents. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc.) should be placed over the package window if this product is to be operated under these lighting conditions.

An ultraviolet source of 2537Å yielding a total integrated dosage of 15 Watt-seconds/cm^2 is required. This will erase a unit in approximately 15 to 20 minutes when a UV lamp of a 12 mW/cm^2 power rating is used. The NMC2724 to be erased should be placed one inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

* Symbols in parentheses are proposed industry standard.

National Semiconductor

MOS EPROMs
PRELIMINARY

NMC2732 32k-Bit (4k x 8) UV Erasable PROM

General Description

The NMC2732 is a 32,768-bit EPROM operating from a single 5V power supply. This device is an ultraviolet erasable, electrically programmable, read only memory fabricated using National's high speed, low power, silicon gate technology.

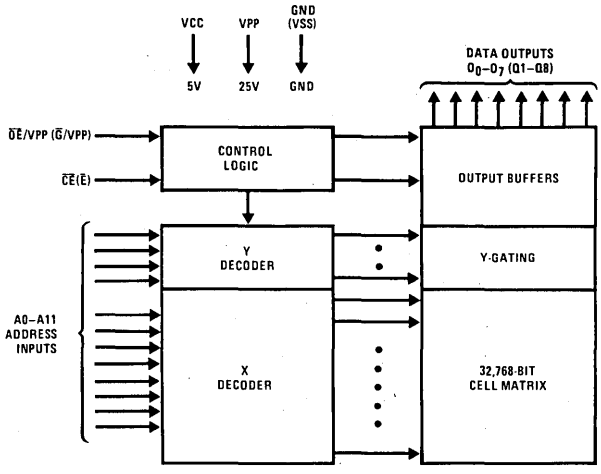
This device is deselected when pin 18 is high and automatically placed in the standby mode. This mode provides an 80% reduction in power with no increase in access time. The NMC2732 has an output enable control to eliminate bus contention in microprocessor systems.

Bits may be programmed at random, in sequence or singly. Typical erasure time is 20 minutes using a 12 mW/cm^2 ultraviolet lamp.

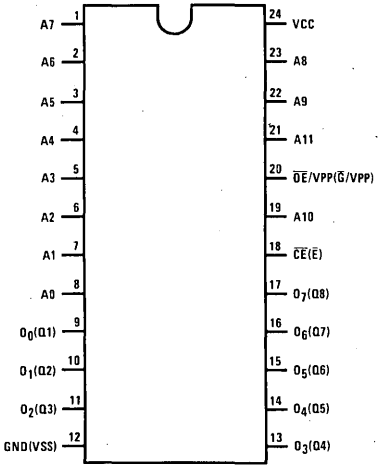
Features

- Single 5V power supply
- 450 ns max access time
- Low power:
  Active—150 mA max
  Standby—30 mA max
- Fully static
- TRI-STATE® output
- All I/O pins TTL compatible
- Pin compatible with existing EPROMs and ROMs
- Output enable control

Block and Connection Diagrams*



Dual-In-Line Package



TOP VIEW

Order Number NMC2732Q
See NS Package J24CQ

Modes*

Mode	Pin Name/Number			
	CE (E) 18	OE/VPP (G/VPP) 20	VCC 24	Outputs 9-11, 13-17
Read	VIL	VIL	5V	DOUT
Standby	VIH	Don't Care	5V	Hi-Z
Program	VIL	25V	5V	DIN
Program Verify	VIL	VIL	5V	DOUT
Program Inhibit	VIH	25V	5V	Hi-Z

Pin Names*

CE (E)	Chip Enable
OE (G)	Output Enable
A0–A11	Address Inputs
O0–O7 (Q1–Q8)	Data Outputs
VPP	Program Power 25V
VCC	Power 5V
GND (VSS)	Ground

* Symbols in parentheses are proposed industry standard.

Absolute Maximum Ratings (Note 1)

Temperature under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input and Output Voltages with Respect to VSS During Read	+6V to −0.3V
VPP Supply Voltage with Respect to VSS During Programming	+26.5V to −0.3V
Power Dissipation	1.5W
Lead Temperature (Soldering, 10 seconds)	300°C

READ OPERATION

DC Operating Characteristics (Note 2) TA = 0°C to 70°C, VCC = 5V ± 5%, VSS = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ILI1	Input Load Current	VIN = 5.25V			10	μA
ILI2	$\overline{OE}$/VPP Input Load Current	VIN = 5.25V			300	μA
ICC1	VCC Current Standby	$\overline{CE}$ = VIH, $\overline{OE}$ = VIL		15	30	mA
ICC2	VCC Current Active	$\overline{OE}$ = $\overline{CE}$ = VIL		85	150	mA
VIL	Input Low Voltage		−0.1		0.8	V
VIH	Input High Voltage		2.0		VCC+1	V
VOL	Output Low Voltage	IOL = 2.1 mA			0.45	V
VOH	Output High Voltage	IOH = −400 μA	2.4			V

AC Characteristics TA = 0°C to 70°C, VCC = 5V ± 5%, VSS = 0V

Symbol		Parameter	Conditions	Min	Typ	Max	Units
Alternate	Standard						
t_{ACC}	TAVQV	Address to Output Valid	$\overline{CE}$ = $\overline{OE}$ = VIL			450	ns
t_{CE}	TELQV	$\overline{CE}$ to Output Delay	$\overline{OE}$ = VIL			450	ns
t_{OE}	TGLQV	Output Enable to Output Delay	$\overline{CE}$ = VIL			120	ns
t_{DF}	TGHQZ	Output Enable High to Output Hi-Z	$\overline{CE}$ = VIL	0		100	ns
t_{OH}	TAXQX	Address to Output Hold	$\overline{CE}$ = $\overline{OE}$ = VIL	0			ns
t_{PF}	TEHQZ	$\overline{CE}$ ($\overline{E}$) to Output Hi-Z	$\overline{OE}$ = VIL	0		100	ns

Capacitance (Note 3) TA = 25°C, f = 1 MHz

Symbol	Parameter	Conditions	Typ	Max	Units
CIN1	Input Capacitance Except $\overline{OE}$/VPP ($\overline{G}$/VPP)	VIN = 0V	4	6	pF
CIN2	$\overline{OE}$/VPP ($\overline{G}$/VPP) Input Capacitance	VIN = 0V		20	pF
COUT	Output Capacitance	VOUT = 0V		12	pF

AC Test Conditions

Output Load: 1 TTL gate and CL = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

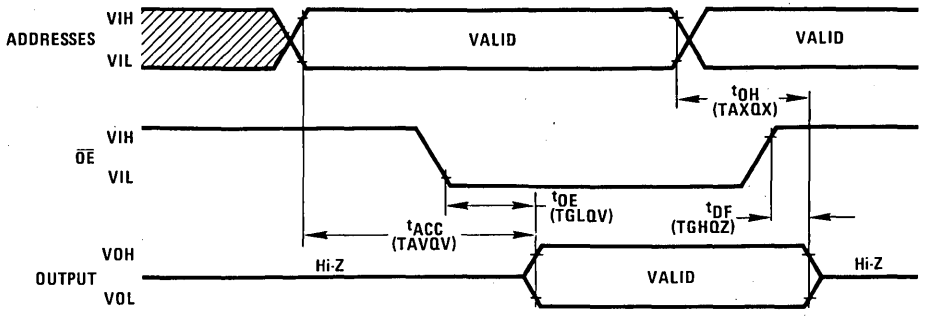
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Recommended DC Operating Conditions" provides conditions for actual device operation.

Note 2: Typical values are for TA = 25°C and nominal supply voltages.

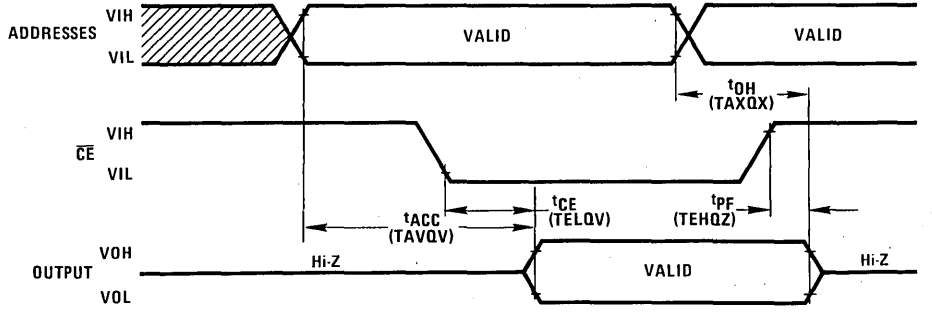
Note 3: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation C = IΔt/ΔV. Capacitance is guaranteed by periodic testing.

Switching Time Waveforms*

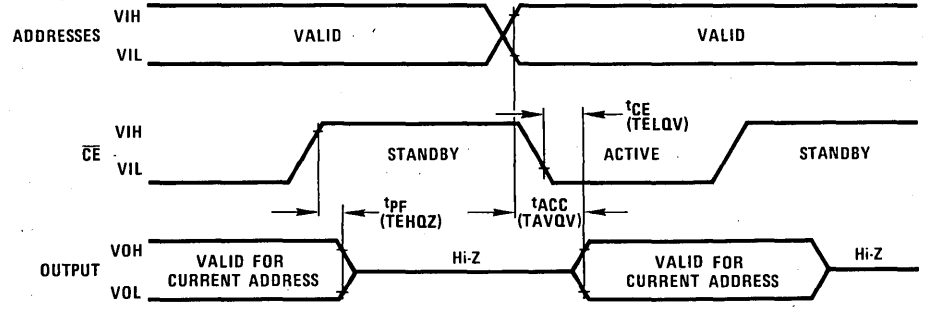
Read Cycle ($\overline{CE}$ = VIL)



Read Cycle ($\overline{OE}$ ($\overline{G}$) = VIL)



Standby Power Down Mode ($\overline{OE}$ = VIL)



* Symbols in parentheses are proposed industry standard.

PROGRAM OPERATION

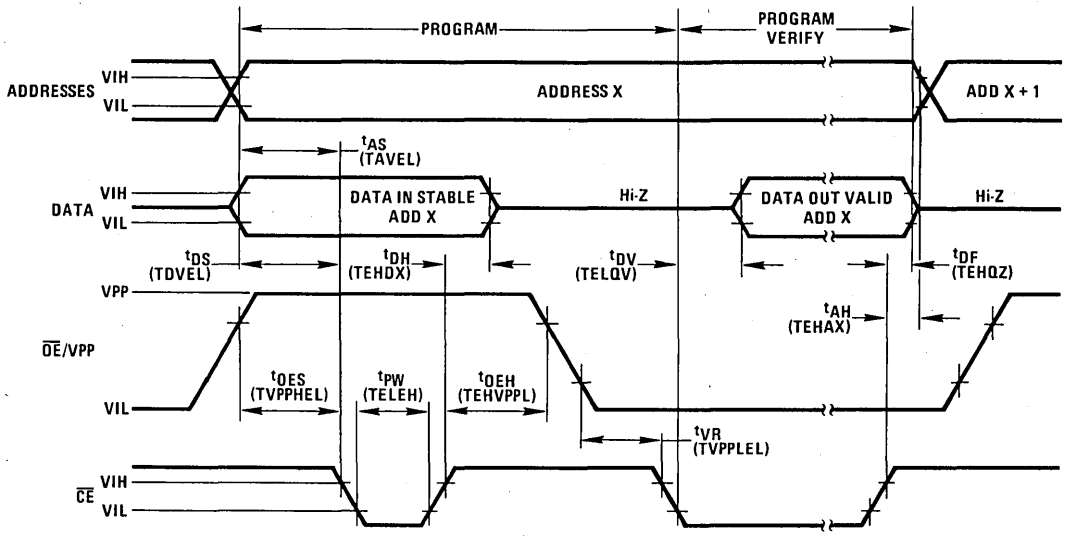
DC Characteristics TA = 25°C ± 5°C, VCC = 5V ± 5%, VPP = 25V ± 1V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ILI	Input Current All Inputs	VIN = VIL or VIH			10	μA
VOL	Output Low Voltage During Verify	IOL = 2.1 mA			0.45	V
VOH	Output High Voltage During Verify	IOH = −400 μA	2.4			V
ICC	VCC Supply Current			85	150	mA
VIL	Input Low Level All Inputs		−0.1		0.8	V
VIH	Input High Level All Inputs Except $\overline{OE}$/VPP		2.0		VCC + 1	V
IPP	VPP Supply Current	$\overline{CE}$ = VIL, $\overline{OE}$ = VPP			30	mA

AC Characteristics TA = 25°C ± 5°C, VCC = 5V ± 5%

Symbol		Parameter	Conditions	Min	Typ	Max	Units
Alternate	Standard						
t_{AS}	TAVEL	Address Set-Up Time		2			μs
t_{OES}	TVPPHEL	Program Voltage Set-Up Time		2			μs
t_{DS}	TDVEL	Data Set-Up Time		2			μs
t_{AH}	TEHAX	Address Hold Time		0			μs
t_{OEH}	TEHVPPL	$\overline{OE}$ Hold Time		2			μs
t_{DH}	TEHDX	Data Hold Time		2			μs
t_{DF}	TEHQZ	Chip Enable to Output Hi-Z		0		120	ns
t_{DV}	TELQV	Data Valid from $\overline{CE}$	$\overline{OE}$ = VIL			1	μs
t_{PW}	TELEH	$\overline{CE}$ Pulse Width During Programming		45	50	55	ms
t_{VR}	TVPPLEL	VPP Recovery Time		2			μs

Programming Waveforms* (Note 4) TA = 25°C ± 5°C, VCC = 5V ± 5%, VPP = 25V ± 1V



Note 4: The input timing reference level is 1V for VIL and 2V for VIH.

* Symbols in parentheses are proposed industry standard.

Functional Description

DEVICE OPERATION

The NMC2732 has two modes of operation in the normal system environment. These are shown in Table I.

TABLE I. OPERATING MODES (VCC = 5V)*

Mode \ Pins	$\overline{CE}$ ($\overline{E}$) 18	$\overline{OE}$/VPP ($\overline{G}$/VPP) 20	ICC Max 24	Outputs 9-11, 13-17
Read	VIL	VIL	150 mA	DOUT
Standby	VIH	Don't Care	30 mA	Hi-Z

Read Mode

The NMC2732 read operation requires that $\overline{CE}$ = VIL, and $\overline{OE}$/VPP = VIL and that addresses A0-A11 have been stabilized. Valid data will apear on the output pins after t_{ACC}, t_{OE}, or t_{CE} times (see Switching Time Waveforms) depending on which is limiting.

Standby Mode

The NMC2732 is placed in the standby mode (deselected and powered down) by making $\overline{CE}$ = VIH. This is independent of the Output Enable control and automatically controls the outputs to their Hi-Z state. The power dissipation is reduced to 20% of the normal operating power. VCC must be kept at 5V. Access time at power up (chip selection) remains either t_{ACC} or t_{CE} (see Switching Time Waveforms).

PROGRAMMING

The NMC2732 is shipped from National completely erased. All bits will be at a "1" level (outputs high) in this initial state after any full erasure. Table II shows the three programming modes.

TABLE II. PROGRAMMING MODES (VCC = 5V)*

Mode \ Pins	$\overline{CE}$ ($\overline{E}$) 18	$\overline{OE}$/VPP ($\overline{G}$/VPP) 20	Outputs 9-11, 13-17
Program	VIL	25V	DIN
Program Verify	VIL	VIL	DOUT
Program Inhibit	VIH	25V	Hi-Z

Program Mode

The NMC2732 is programmed by placing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, a sequence of addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the $\overline{CE}$ pin. All input voltage levels, including the program pulse on the $\overline{CE}$ pin are TTL compatible. The programming sequence is:

With the $\overline{OE}$/VPP pin at 25V and VCC = 5V, an address is selected and the desired data word is applied to the output pins (VIL = "0" and VIH = "1" for both address and data). After the address and data signals are stable the $\overline{CE}$ pin is pulsed from VIH to VIL with a pulse width between 45 ms and 55 ms.

Multiple pulses are not needed but will not cause device damage. No pins should be left open. A low level, VIL or lower *must not* be maintained steady state (DC signal) on the $\overline{CE}$ pin during programming. Several NMC2732s may be programmed in parallel (the same data in each one) in this mode.

Program Verify

The programming of the NMC2732 may be verified, either one word at a time during the programming (as shown in the timing diagram) or by reading all of the words out at the end of the programming sequence.

Program Inhibit

The program inhibit mode allows programming several NMC2732s in parallel with different data for each one by controlling which ones receive the program pulse. All similar inputs may be paralleled. Pulsing the $\overline{CE}$ pin from VIH to VIL on a selected unit or units will cause programming, while inhibiting the $\overline{CE}$ pulse will inhibit programming and keep the outputs of the inhibited devices in the Hi-Z state.

ERASURE PROCEDURE

The NMC2532 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gates to their initial state through induced photo current. It is recommended that this device be kept out of direct sunlight. The UV content of sunlight may cause the a partial erasure of some bits in a relatively short period of time. Direct sunlight (any intense light) can cause temporary functional failure due to generation of photo currents. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc.) should be placed over the package window if this product is to be operated under these lighting conditions.

An ultraviolet source of 2537Å yielding a total integrated dosage of 15 Watt-seconds/cm^2 is required. This will erase a unit in approximately 15 to 20 minutes when a UV lamp of a 12 mW/cm^2 power rating is used. The NMC2732 to be erased should be placed one inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

* Symbols in parentheses are proposed industry standard.

Section 6

Bipolar PROMs

6

High speed microcontrol storage is made practical at very low cost through the use of National's bipolar PROMs. This generic family utilizes the latest in Schottky circuitry and Titanium-Tungsten fuse link technology. National offers these and other memory and logic products for state-of-the-art solutions to data processing and control logic design problems. Refer to National's Memory Applications Handbook for suggestions on how to use these devices effectively.

Schottky PROMs

National Semiconductor

DM54S188/DM74S188 256-Bit (32 x 8) Open-Collector PROM
DM54S288/DM74S288 256-Bit (32 x 8) TRI-STATE® PROM

General Description

These Schottky PROM memories are organized in the popular 32 words by 8 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions and are available as ROM's as well as PROM's.

PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

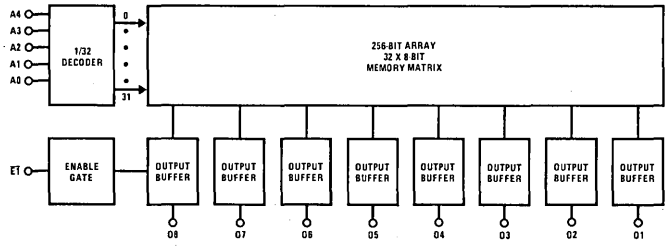
See the last page of this section for detailed programming information.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—35 ns max
  - Enable access—25 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming

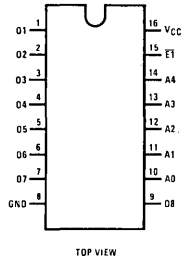
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S188		X	X		N, J
DM74S288		X		X	N, J
DM54S188	X		X		J
DM54S288	X			X	J

Block Diagram



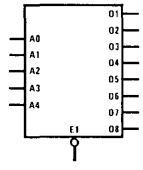
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Symbol



Order Number DM54S188J, DM54S288J, DM74S188J or DM74S288J
See NS Package J16A

Order Number DM74S188N or DM74S288N
See NS Package N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	-0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S188, DM54S288	4.5	5.5	V
DM74S188, DM74S288	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S188, DM54S288	−55	+125	°C
DM74S188, DM74S288	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

DC Electrical Characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S188, 54S288			DM74S188, 74S288			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		70	110		70	110	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S188, 54S288 5V ±10%; −55°C to +125°C			DM74S188, 74S288 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			22	45		22	35	ns
t_{EA}	Enable Access Time			15	30		15	20	ns
t_{ER}	Enable Recovery Time			15	35		15	25	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to either A0 (pin 10) or A4 (pin 14).

National Semiconductor

DM54S287/DM74S287 1024-Bit (256 x 4) TRI-STATE® PROM
DM54S387/DM74S387 1024-Bit (256 x 4) Open-Collector PROM

General Description

These Schottky memories are organized in the popular 256 words by 4 bits configuration. Two memory enable inputs are provided to control the output states. When both enable inputs are in the low state, the outputs present the contents of the selected word.

If either or both of the enable inputs is raised to a high state, it causes all four outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

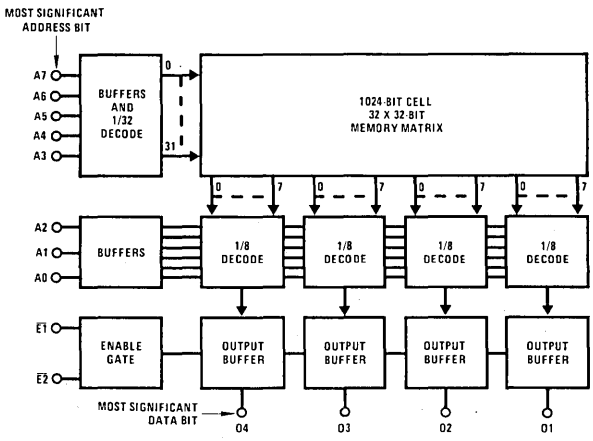
See the last page of this section for detailed programming information.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—50 ns max
  - Enable access—25 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- ROM mates are DM74S187 and DM85S97

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S387		X	X		N, J
DM74S287		X		X	N, J
DM54S387	X		X		J
DM54S287	X			X	J

Block Diagram

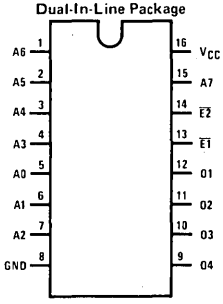


Order Number DM54S287J, DM54S387J, DM74S287J or DM74S387J
See NS Package J16A

Order Number DM74S287N or DM74S387N
See NS Package N16A

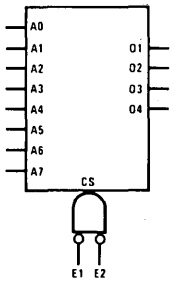
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Symbol



6

Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S387, DM54S287	4.5	5.5	V
DM74S387, DM74S287	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S387, DM54S287	−55	+125	°C
DM74S387, DM74S287	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

DC Electrical Characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S387/54S287			DM74S387/74S287			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_F	Input Load Current, All Inputs	V_{CC} = Max, V_F = 0.45V		−80	−250		−80	−250	μA
I_R	Input Leakage Current, All Inputs	V_{CC} = Max, V_R = 2.7V			25			25	μA
I_{RB}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{RB} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		80	130		80	130	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S387/54S287 5V ±10%; −55°C to +125°C			DM74S387/74S287 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time	*(Figure 1)*	10	35	60	10	35	50	ns
t_{EA}	Enable Access Time	*(Figure 2)*	5	15	30	5	15	25	ns
t_{ER}	Enable Recovery Time	*(Figure 2)*	5	15	30	5	15	25	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

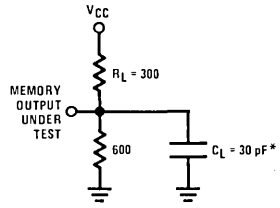
Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH} or I_{CEX} on an unprogrammed part, apply 10.5V to both A7 and A2 (pin 15 and pin 7).

Standard Test Load



*C_L includes probe and jig capacitance.

- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50Ω, $t_r \leq 2.5$ ns and $t_f \leq 2.5$ ns (between 1.0V and 2.0V).
- t_{AA} is measured with both enable inputs at a steady low level.
- t_{EA} and t_{ER} are measured from the 1.5V on inputs and outputs with all address inputs at a steady level and with the unused enable input at a steady low level.

Switching Time Waveforms

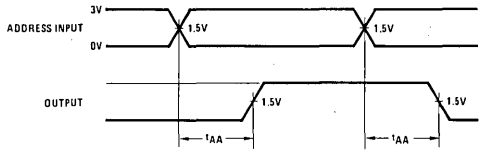


FIGURE 1. Address Access Time

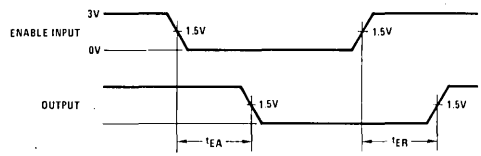
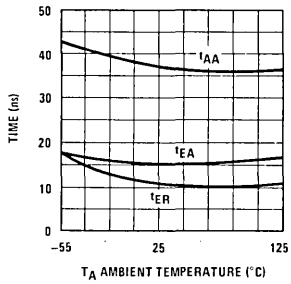


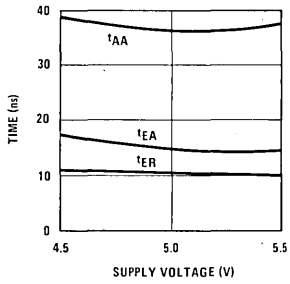
FIGURE 2. Enable Access Time and Recovery Time

Typical Performance Characteristics

Typical Switching Characteristics as a Function of Temperature (V_{CC} = 5V, Standard Load)

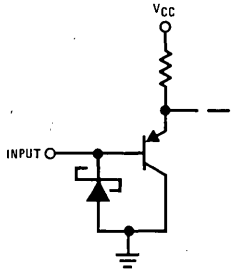


Typical Switching Characteristics as a Function of V_{CC} (T_A = 25°C, Standard Load)

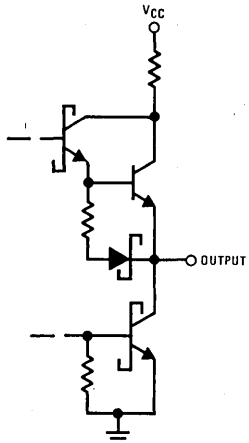


Equivalent Circuits

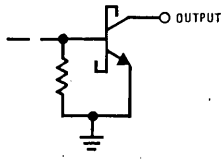
Equivalent of Each Input



Typical TRI-STATE Output



Typical Open-Collector Output



National Semiconductor

DM54S473/DM74S473 4096-Bit (512 x 8) Open-Collector PROM
DM54S472/DM74S472 4096-Bit (512 x 8) TRI-STATE® PROM

General Description

These Schottky PROM memories are organized in the popular 512 words by 8 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions.

PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

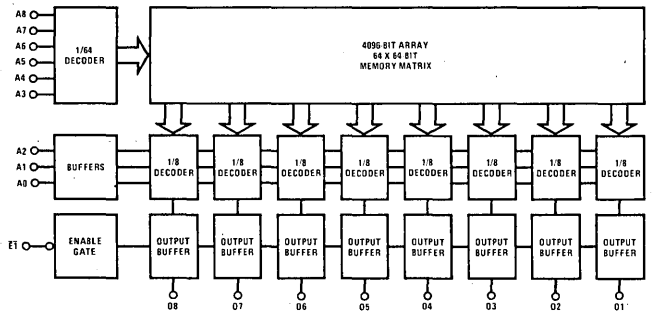
See the last page of this section for detailed programming information.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—60 ns max
  Enable access—30 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- High density 20-pin package

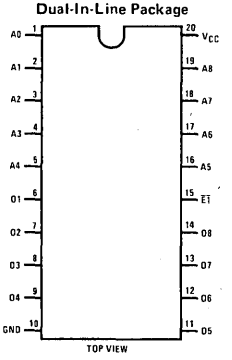
	Military	Commercial	Open-Collector	TRI-STATE	Package
		X	X		N, J
DM74S472		X		X	N, J
DM54S473	X		X		J
DM54S472	X			X	J

Block Diagram

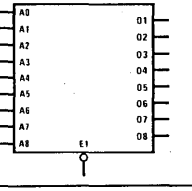


Connection Diagram

Dual-In-Line Package



Logic Symbol



Order Number DM54S472J, DM54S473J, DM74S472J or DM74S473J
See NS Package J20B

Order Number DM74S472N or DM74S473N
See NS Package N20A

Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S473, DM54S472	4.5	5.5	V
DM74S473, DM74S472	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S473, DM54S472	−55	+125	°C
DM74S473, DM74S472	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

DC Electrical Characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S473, 54S472			DM74S473, 74S472			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		120	155		120	155	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S473, 54S472 5V ±10%; −55°C to +125°C			DM74S473, 74S472 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time				75			60	ns
t_{EA}	Enable Access Time				35			30	ns
t_{ER}	Enable Recovery Time				35			30	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V.

National Semiconductor

DM54S474/DM74S474 4096-Bit (512 x 8) TRI-STATE® PROM
DM54S475/DM74S475 4096-Bit (512 x 8) Open-Collector PROM

General Description

These Schottky memories are organized in the popular 512 words by 8 bits configuration. Four memory enable inputs are provided to control the output states. When E1 and E2 are low and E3 and E4 are high, the output presents the contents of the selected word.

If E1 or E2 are high, or E3 or E4 are low, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

See the last page of this section for detailed programming information.

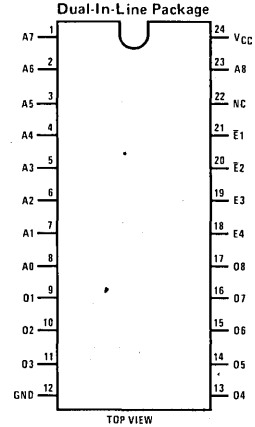
Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—65 ns
  - Enable access—35 ns
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- ROM mates are DM87S95 and DM87S96

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S475		X	X		N, J
DM74S474		X		X	N, J
DM54S475	X		X		J
DM54S474	X			X	J

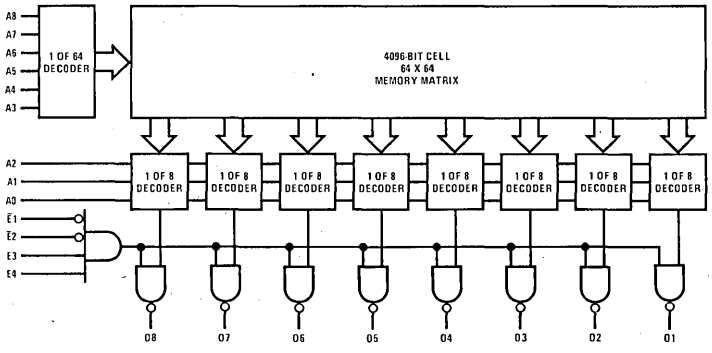
Connection Diagram

Dual-In-Line Package

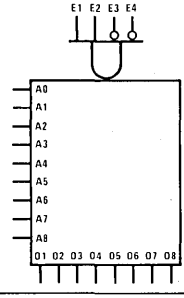


TOP VIEW

Block Diagram



Logic Symbol



Order Number DM54S474J, DM54S475J, DM74S474J or DM74S475J
See NS Package J24A

Order Number DM74S474N or DM74S475N
See NS Package N24B

Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S474, DM54S475	4.5	5.5	V
DM74S474, DM74S475	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S474, DM54S475	−55	+125	°C
DM74S474, DM74S475	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

DC Electrical Characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S474, DM54S475			DM74S474, DM74S475			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		115	170		115	170	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S474, DM54S475 5V ±10%; −55°C to +125°C			DM74S474, DM74S475 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time	*(Figure 1)*		40	75		40	65	ns
t_{EA}	Enable Access Time	*(Figure 2)*		20	40		20	35	ns
t_{ER}	Enable Recovery Time	*(Figure 2)*		20	40		20	35	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

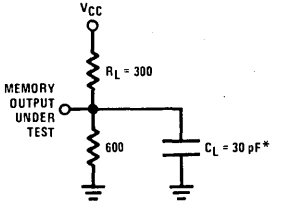
Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to both A7 and A2 (pin 1 and pin 6).

Standard Test Load



*C_L includes probe and jig capacitance.

- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50Ω, $t_r \leq 2.5$ ns and $t_f \leq 2.5$ ns (between 1.0V and 2.0V).
- t_{AA} is measured with both enable inputs at a steady low level.
- t_{EA} and t_{ER} are measured from the 1.5V on inputs and outputs with all address inputs at a steady level and with the unused enable input at a steady low level.

Switching Time Waveforms

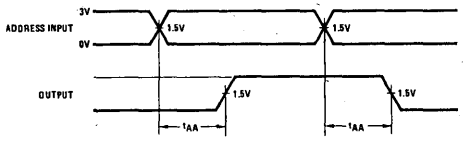


FIGURE 1. Address Access Time

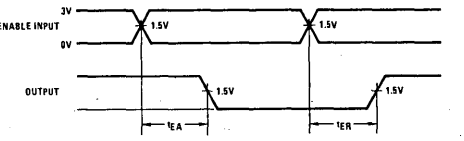
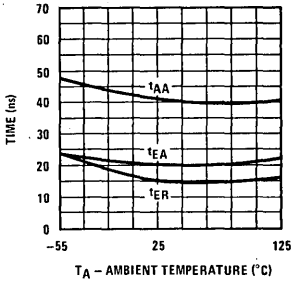


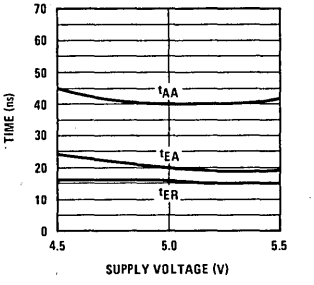
FIGURE 2. Enable Access Time and Recovery Time

Typical Performance Characteristics

Typical Switching Characteristics as a Function of Temperature (V_{CC} = 5V, Standard Load)

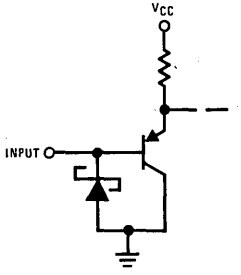


Typical Switching Characteristics as a Function of V_{CC} (T_A = 25°C, Standard Load)

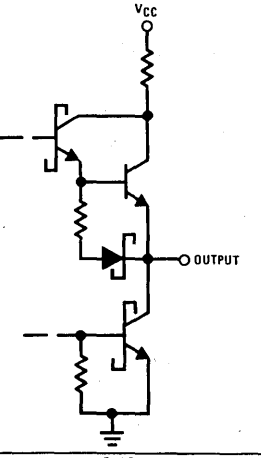


Equivalent Circuits

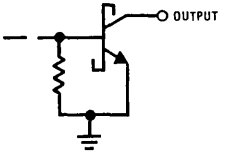
Equivalent of Each Input



Typical TRI-STATE Output



Typical Open-Collector Output



National Semiconductor

DM54S570/DM74S570 2048-Bit (512 x 4) Open-Collector PROM

DM54S571/DM74S571 2048-Bit (512 x 4) TRI-STATE® PROM

General Description

These Schottky memories are organized in the popular 512 words by 4 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 4 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE versions and are available as ROM's as well as PROM's.

PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

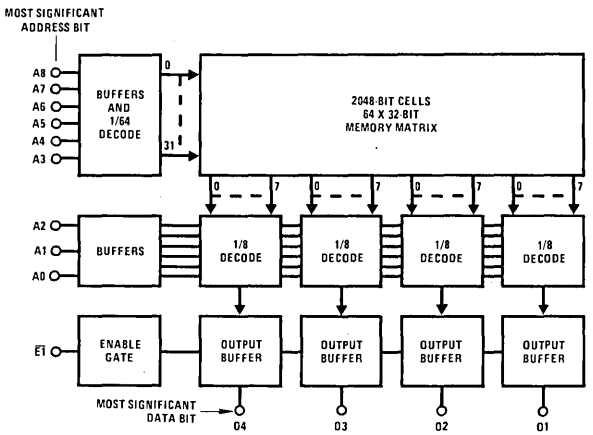
See the last page of this section for detailed programming information.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—55 ns max
  Enable access—30 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- ROM mates are DM74S270 and DM74S370

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S570		X	X		N, J
DM74S571		X		X	N, J
DM54S570	X		X		J
DM54S571	X			X	J

Block Diagram

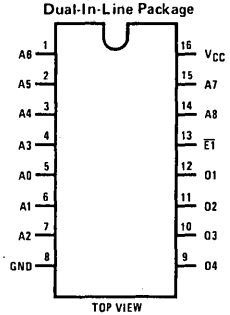


Order Number DM54S570J, DM54S571J, DM74S570J or DM74S571J
See NS Package J16A

Order Number DM74S570N or DM74S571N
See NS Package N16A

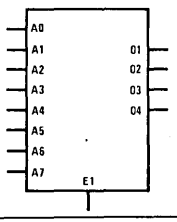
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Symbol



Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S570, DM54S571	4.5	5.5	V
DM74S570, DM74S571	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S570, DM54S571	−55	+125	°C
DM74S570, DM74S571	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

DC Electrical Characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S570, 54S571			DM74S570, 74S571			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		90	130		90	130	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S570, 54S571 5V ±10%; −55°C to +125°C			DM74S570, 74S571 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time	*(Figure 1)*		40	65		40	55	ns
t_{EA}	Enable Access Time	*(Figure 2)*		20	35		20	30	ns
t_{ER}	Enable Recovery Time	*(Figure 2)*		20	35		20	30	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

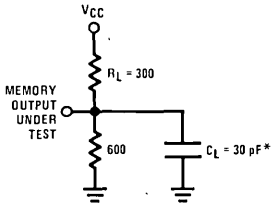
Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to both A8 and A2 (pin 14 and pin 7).

Standard Test Load



*C_L includes probe and jig capacitance.

- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50Ω, $t_r \leq 2.5$ ns and $t_f \leq 2.5$ ns (between 1.0V and 2.0V).
- t_{AA} is measured with both enable inputs at a steady low level.
- t_{EA} and t_{ER} are measured from the 1.5V on inputs and outputs with all address inputs at a steady level and with the unused enable input at a steady low level.

Switching Time Waveforms

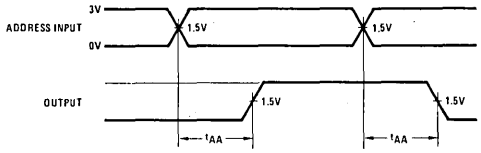


FIGURE 1. Address Access Time

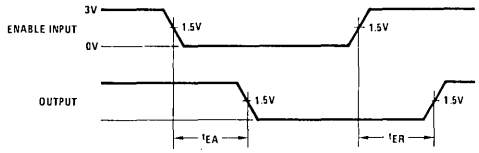
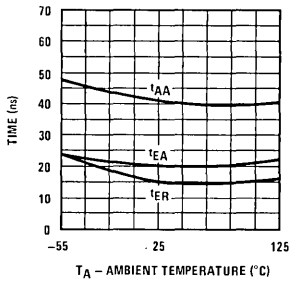


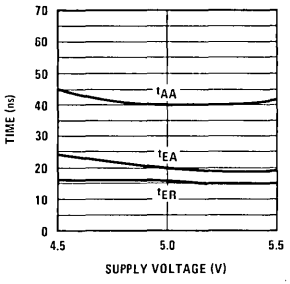
FIGURE 2. Enable Access Time and Recovery Time

Typical Performance Characteristics

Typical Switching Characteristics as a Function of Temperature (V_{CC} = 5V, Standard Load)

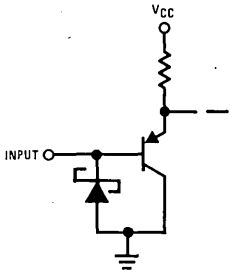


Typical Switching Characteristics as a Function of V_{CC} (T_A = 25°C, Standard Load)

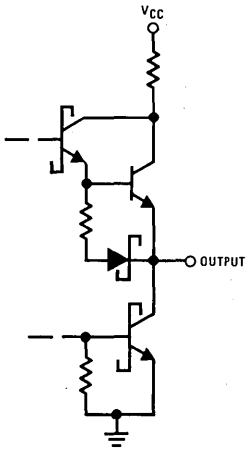


Equivalent Circuits

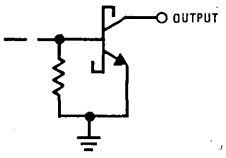
Equivalent of Each Input



Typical TRI-STATE Output



Typical Open-Collector Output



National Semiconductor

Bipolar PROMs

DM54S572/DM74S572 4096-Bit (1024 x 4) Open-Collector PROM
DM54S573/DM74S573 4096-Bit (1024 x 4) TRI-STATE® PROM

General Description

These Schottky PROM memories are organized in the popular 1024 words by 4 bits configuration. Two memory enable inputs are provided to control the output states. When the enable inputs are in the low state, the outputs present the contents of the selected word.

If either or both of the enable inputs is raised to a high level, it causes all 4 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

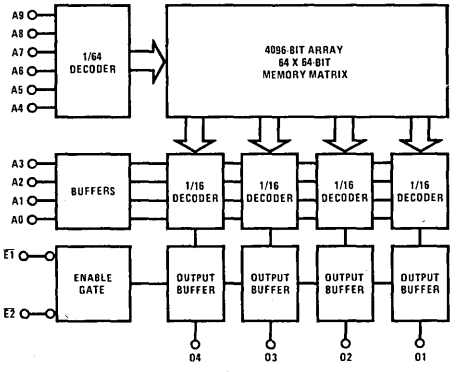
See the last page of this section for detailed programming information.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—60 ns max
  Enable access—35 ns max
- PNP inputs reduce input loading
- All dc and ac parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Board level programming
- High density 18-pin package

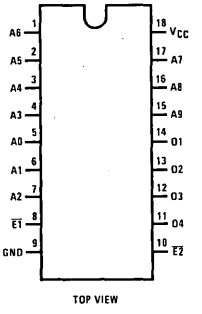
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S572		X	X		N,J
DM74S573		X		X	N,J
DM54S572	X		X		J
DM54S573	X			X	J

Block Diagram



Connection Diagram

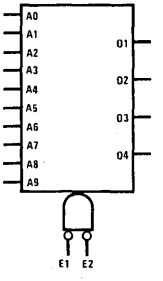
Dual-In-Line Package



TOP VIEW

Order Number DM54S572J, DM54S573J, DM74S572J or DM74S573J
See NS Package J18A

Logic Symbol



Order Number DM74S572N or DM74S573N
See NS Package N18A

Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	-0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM54S572, DM54S573	4.5	5.5	V
DM74S572, DM74S573	4.75	5.25	V
Ambient Temperature (T_A)			
DM54S572, DM54S573	−55	+125	°C
DM74S572, DM74S573	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

DC Electrical Characteristics (Note 3)

PARAMETER		CONDITIONS	DM54S572, 54S573			DM74S572, 74S573			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only) (Note 5)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		125	140		125	140	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current (Note 5)	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High, (Note 5)	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With standard load)

PARAMETER		CONDITIONS	DM54S572, 54S573 5V ±10%; −55°C to +125°C			DM74S572, 74S573 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			40	75		40	60	ns
t_{EA}	Enable Access Time			25	45		25	35	ns
t_{ER}	Enable Recovery Time			25	45		25	35	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Note 5: To measure V_{OH}, I_{CEX} or I_{SC} on an unprogrammed part, apply 10.5V to both A5 and A2 (pin 2 and pin 7).

National Semiconductor

Bipolar PROMs

DM77S180/DM87S180, DM77S181/DM87S181
1024 x 8-Bit TTL PROM

General Description

These Schottky memories are organized in the popular 1024 words by 8 bits configuration. Four memory enable inputs are provided to control the output states. When $\overline{E1}$ and $\overline{E2}$ are low and E3 and E4 are high, the output presents the contents of the selected word.

If $\overline{E1}$ or $\overline{E2}$ are high, or E3 or E4 are low, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

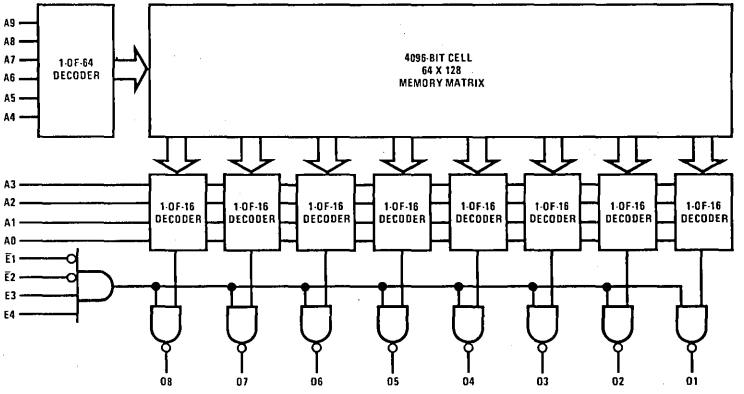
See the last page of this section for detailed programming information.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—40 ns typ
  - Enable access—15 ns typ
- PNP inputs reduce input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

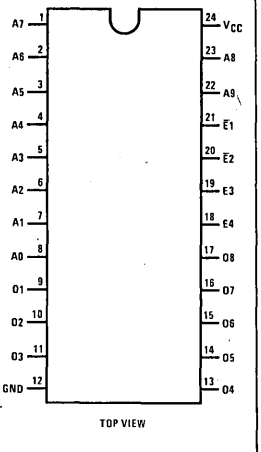
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM87S180		X	X		N, J
DM87S181		X		X	N, J
DM77S180	X		X		J
DM77S181	X			X	J

Block Diagram



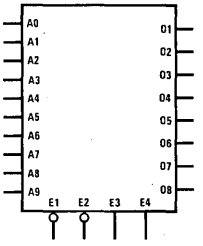
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Symbol



Pin Names

$\overline{E1}$ to E4	Enable Inputs
A0 to A9	Address Inputs
O1 to O8	Data Outputs

Order Number DM77S180J, DM77S181J, DM87S180J or DM87S181J
See NS Package J24A

Order Number DM87S180N or DM87S181N
See NS Package N24B

Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM77S180, DM77S181	4.5	5.5	V
DM87S180, DM87S181	4.75	5.25	V
Ambient Temperature (T_A)			
DM77S180, DM77S181	−55	+125	°C
DM87S180, DM87S181	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Parameter		Conditions	DM77S180, DM77S181			DM87S180, DM87S181			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−10	−100		−10	−100	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			50			50	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		115	170		115	170	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With standard load)

Parameter		Conditions	DM77S180, DM77S181 5V ± 10%; −55°C to +125°C			DM87S180, DM87S181 5V ± 5%, 0°C to +70°C			Units
			Min	Typ	Max	Min	Typ	Max	
t_{AA}	Address Access Time			40	75		40	60	ns
t_{EA}	Enable Access Time			15	35		15	30	ns
t_{ER}	Enable Recovery Time			15	35		15	30	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unles stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor

DM77S184/DM87S184 8192-Bit (2048 x 4) Open-Collector PROM
DM77S185/DM87S185 8192-Bit (2048 x 4) TRI-STATE® PROM

General Description

These Schottky PROM memories are organized in the popular 2048 words by 4 bits configuration. One memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 4 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

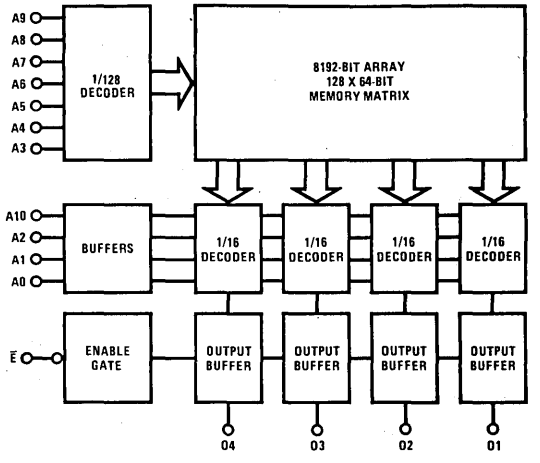
PROM's are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. See the last page of this section for detailed programming information.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—40 ns max
  - Enable access—15 ns max
- PNP inputs reduce input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM87S184		X	X		N, J
DM87S185		X		X	N, J
DM77S184	X		X		J
DM77S185	X			X	J

Block Diagram

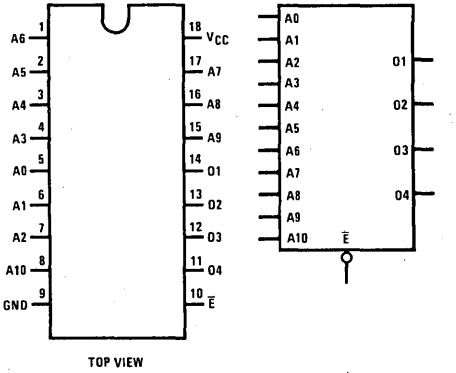


Pin Names

$\overline{E}$	Enable Input
A0-A10	Address Inputs
O1-O4	Data Outputs

Connection Diagram Logic Symbol

Dual-In-Line Package



TOP VIEW

Order Number DM77S184J, DM77S185J, DM87S184J or DM87S185J
See NS Package J18A

Order Number DM87S184N or DM87S185N
See NS Package N18A

Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM77S184, DM77S185	4.5	5.5	V
DM87S184, DM87S185	4.75	5.25	V
Ambient Temperature (T_A)			
DM77S184, DM77S185	−55	+125	°C
DM87S184, DM87S185	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

DC Electrical Characteristics (Note 3)

PARAMETER		CONDITIONS	DM77S184, DM77S185			DM87S184, DM87S185			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−10	−100		−10	−100	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			50			50	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		100	140		100	170	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With standard load)

PARAMETER		CONDITIONS	DM77S184, DM77S185 5V ±10%; −55°C to +125°C			DM87S184, DM87S185 5V ±5%; 0°C to +70°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time			40	75		40	55	ns
t_{EA}	Enable Access Time			15	35		15	30	ns
t_{ER}	Enable Recovery Time			15	35		15	30	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor

DM77S188/DM87S188, DM77S288/DM87S288
32 x 8-Bit TTL PROM

General Description

These Schottky PROM memories are organized in the popular 32 words by 8 bits configuration. A memory enable input is provided to control the output states. When the enable input is in the low state, the outputs present the contents of the selected word.

If the enable input is raised to a high level, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

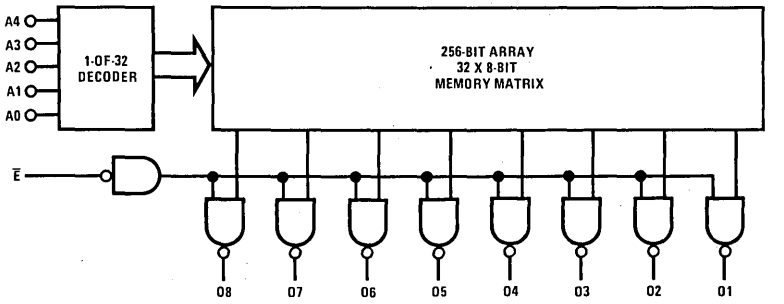
See the last page of this section for detailed programming information.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  Address access—12 ns typ
  Enable access—8 ns typ
- PNP inputs reduce input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

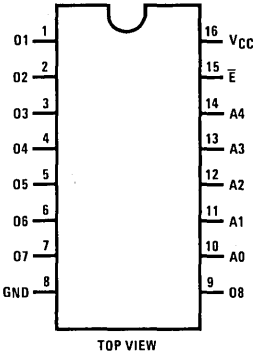
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM87S188		X	X		N, J
DM87S288		X		X	N, J
DM77S188	X		X		J
DM77S288	X			X	J

Block Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

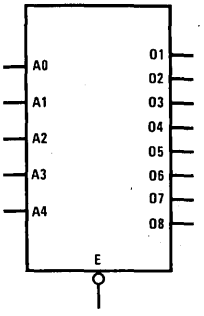
Order Number DM77S188J, DM77S288J, DM87S188J or DM87S288J
See NS Package J16A

Order Number DM87S188N or DM87S288N
See NS Package N16A

Pin Names

Ē	Enable Input
A0 to A4	Address Inputs
O1 to O8	Data Outputs

Logic Symbol



Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM77S188, DM77S288	4.5	5.5	V
DM87S188, DM87S288	4.75	5.25	V
Ambient Temperature (T_A)			
DM77S188, DM77S288	−55	+125	°C
DM87S188, DM87S288	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Parameter		Conditions	DM77S188, DM77S288			DM87S188, DM87S288			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V			−100			−100	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			50			50	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 12 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		120			120		mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With standard load)

Parameter		Conditions	DM77S188, DM77S288 5V ± 10%; −55°C to +125°C			DM87S188, DM87S288 5V ± 5%, 0°C to +70°C			Units
			Min	Typ	Max	Min	Typ	Max	
t_{AA}	Address Access Time			12	20		12	15	ns
t_{EA}	Enable Access Time			8	12		8	10	ns
t_{ER}	Enable Recovery Time			8	12		8	10	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unles stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor

DM77S190/DM87S190, DM77S191/DM87S191
2048 x 8-Bit TTL PROM

General Description

These Schottky memories are organized in the popular 2048 words by 8 bits configuration. Three memory enable inputs are provided to control the output states. When $\overline{E}1$ is low and E2 and E3 are high, the output presents the contents of the selected word.

If $\overline{E}1$ is high, or E2 or E3 are low, it causes all 8 outputs to go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

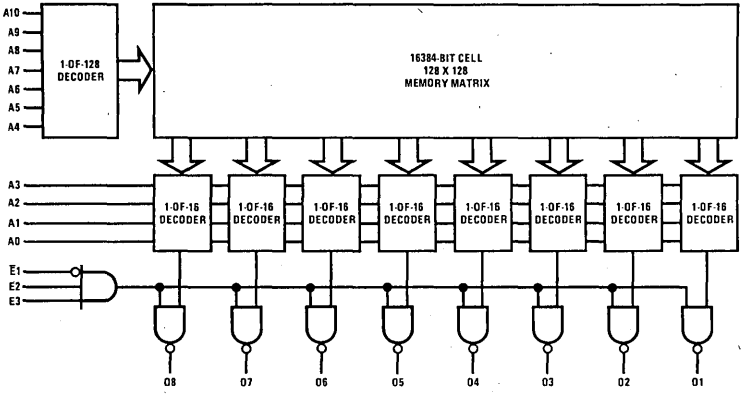
See the last page of this section for detailed programming information.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—40 ns typ
  - Enable access—20 ns typ
- PNP inputs reduce input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

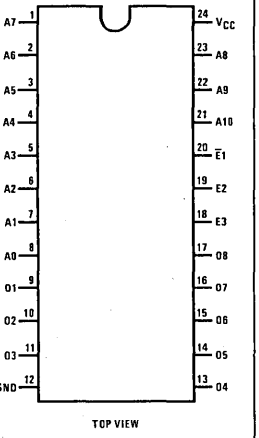
	Military	Commercial	Open-Collector	TRI-STATE	Package
DM87S190		X	X		N, J
DM87S191		X		X	N, J
DM77S190	X		X		J
DM77S191	X			X	J

Block Diagram



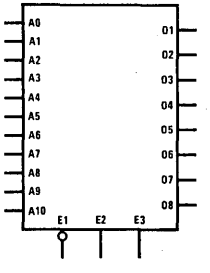
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Symbol



Pin Names

$\overline{E}1$ to E3	Enable Inputs
A0 to A10	Address Inputs
O1 to O8	Data Outputs

Order Number DM77S190J, DM77S191J, DM87S190J or DM87S191J
See NS Package J24A

Order Number DM87S190N or DM87S191N
See NS Package N24A

Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	−0.5V to +7V
Input Voltage (Note 2)	−1.2V to +5.5V
Output Voltage (Note 2)	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM77S190, DM77S191	4.5	5.5	V
DM87S190, DM87S191	4.75	5.25	V
Ambient Temperature (T_A)			
DM77S190, DM77S191	−55	+125	°C
DM87S190, DM87S191	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

DC Electrical Characteristics (Note 3)

Parameter		Conditions	DM77S190, DM77S191			DM87S190, DM87S191			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−10	−150		−10	−100	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			50			50	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 12 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		120	175		120	175	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 4)	−20		−70	−20		−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High	I_{OH} = −2 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With standard load)

Parameter		Conditions	DM77S190, DM77S191 5V ± 10%; −55°C to +125°C			DM87S190, DM87S191 5V ± 5%, 0°C to +70°C			Units
			Min	Typ	Max	Min	Typ	Max	
t_{AA}	Address Access Time			40	85		40	70	ns
t_{EA}	Enable Access Time			20	35		20	30	ns
t_{ER}	Enable Recovery Time			20	35		20	30	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

Note 3: These limits apply over the entire operating range unles stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 4: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

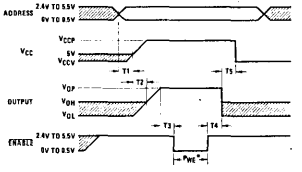
Schottky PROM Programming Procedure

These parts are shipped from the factory with all fuses intact. As a result, the outputs will be low (logical "0") for all addresses. In order to generate a high level on the outputs, the part must be programmed. Information on available programming equipment may be obtained from National. However, if it is desired to build your own programmer, the following conditions must be observed.

1. Programming should be attempted only at temperatures between 15°C and 30°C.
2. Addresses and chip enable pins must be driven from normal TTL logic levels during both programming and verification.
3. Programming will occur at a selected address when V_{CC} is held at 10.5V, the appropriate output is held at 10.5V and the chip is subsequently enabled. To achieve these conditions in the appropriate sequence, the following procedure must be followed:
   a) Select the desired word by applying a high or low level to the appropriate address inputs. Disable the chip by applying a high level to one or both enable inputs.
   b) Increase V_{CC} to 10.5V ±0.5V with the rate of increase being between 1.0 and 10.0V/μs. Since V_{CC} supplies the current to program the fuse as well as the I_{CC} of the device at programming voltage, it must be capable of supplying 750 mA at 11.0V.
   c) Select the output where a high level is desired by raising that output voltage to 10.5V ±0.5V. Limit the rate of increase to a value between 1.0 and 10.0V/μs. This voltage change may occur simultaneously with the increase in V_{CC} but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or tied to a high impedance source of at least 20 kΩ. (Remember that the outputs of the device are still disabled at this time because the chip enables are high.)
   d) Enable the device by taking both chip enables to a low level. This is done with a pulse of 10μs. The 10μs duration refers to the time that the circuit is enabled. Normal input levels are used and rise and fall times are not critical.
   e) Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 4.0V ±0.2V. Verification at a V_{CC} level of 4.0V will guarantee proper output states over the V_{CC} and temperature range of the programmed part. The chip must be enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits. Steps b, c and d must be repeated 10 times or until verification that the bit has programmed.
   f) Following verification, apply five additional programming pulses to the bit being programmed. The programming procedure is now complete for the selected bit.
   g) Repeat steps a through f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at programming voltage must be limited to a maximum of 25%. This is necessary to minimize chip junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

Note: Since only an enabled chip is programmed, it is possible to program these parts at the board level if all programming parameters are complied with.

Programming Waveforms

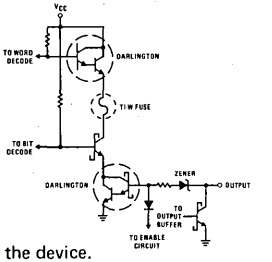


T1 = 100 ns min
T2 = 5μs min (T2 may be ≥ 0 if V_{CCP} rises at the same rate or faster than V_{OP})
T3 = 100 ns min
T4 = 100 ns min
T5 = 100 ns min

*P_{WE} is repeated for 5 additional pulses after verification of V_{OH} indicates a bit has programmed

Equivalent Circuit

Programming Equivalent Circuit for One Memory Output (Applies to All NSC Generic Schottky PROMs)



Programming Parameters

Do not test or you may program the device.

PARAMETERS		CONDITIONS	MIN	RECOMMENDED VALUE	MAX	UNITS
V_{CCP}	Required V_{CC} for Programming		10.0	10.5	11.0	V
I_{CCP}	I_{CC} During Programming	V_{CC} = 11V	600		750	mA
V_{OP}	Required Output Voltage for Programming		10.0	10.5	11.0	V
I_{OP}	Output Current while Programming	V_{OUT} = 11V			20	mA
t_{RR}	Rate of Voltage Change of V_{CC} or Output		1.0		10.0	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCV}	Required V_{CC} for Verification		3.8	4.0	4.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

ECL
PROMs

National Semiconductor

Bipolar PROMs
PREVIEW

DM10416 256 x 4-Bit ECL PROM

General Description

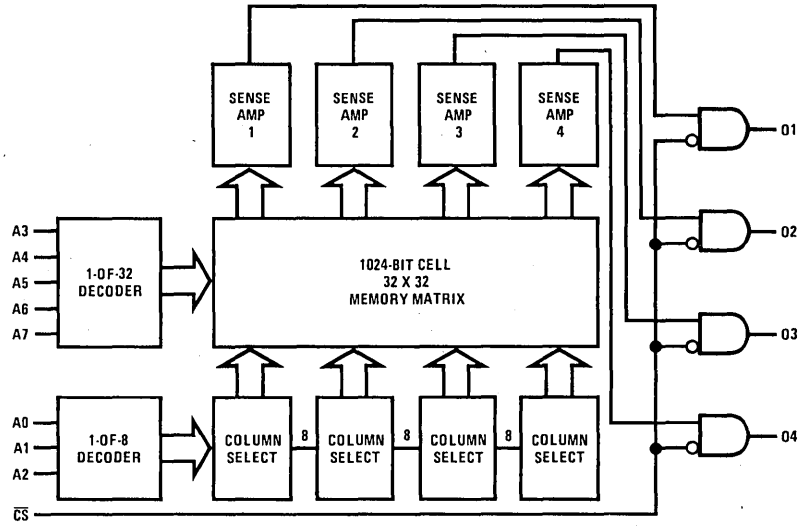
The DM10416 is a fully decoded high speed 1024-bit field Programmable Read Only Memory, organized 256 words by four bits. The DM10416 is voltage compensated and compatible with 10k ECL families. The device is enabled when $\overline{CS}$ is LOW. Programmed bits will furnish HIGH levels at corresponding outputs. When the device is disabled ($\overline{CS}$ is HIGH) all outputs are LOW.

See the last page of this section for detailed programming information.

Features

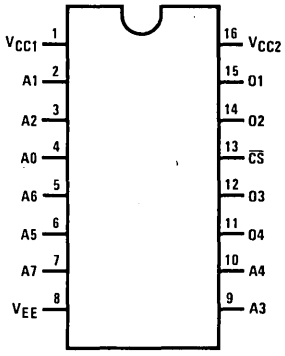
- Fast cycle time—12 ns typ
- Organization—256 words x 4 bits
- 10k and uncompensated 10k ECL logic
- Chip select input provides easy expansion
- Open emitter outputs for memory expansion
- Standard 16-pin dual-in-line package
- Full address decoding on chip

Block Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

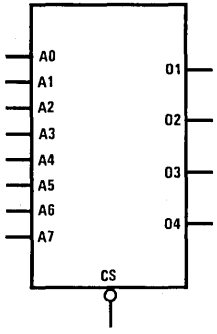
Pin Names

$\overline{CS}$	Chip Select Input
A0 to A7	Address Inputs
O1 to O4	Data Outputs

Note:
V_{CC1} (Pin 1) is connected to the Programmer (+6.0V) during programming only.

V_{CC1} = GND (Read only) = Pin 1
V_{CC2} = GND = Pin 16
V_{EE} = Pin 8

Logic Symbol



National Semiconductor

Bipolar PROMs
PREVIEW

DM100416 256 x 4-Bit ECL PROM

General Description

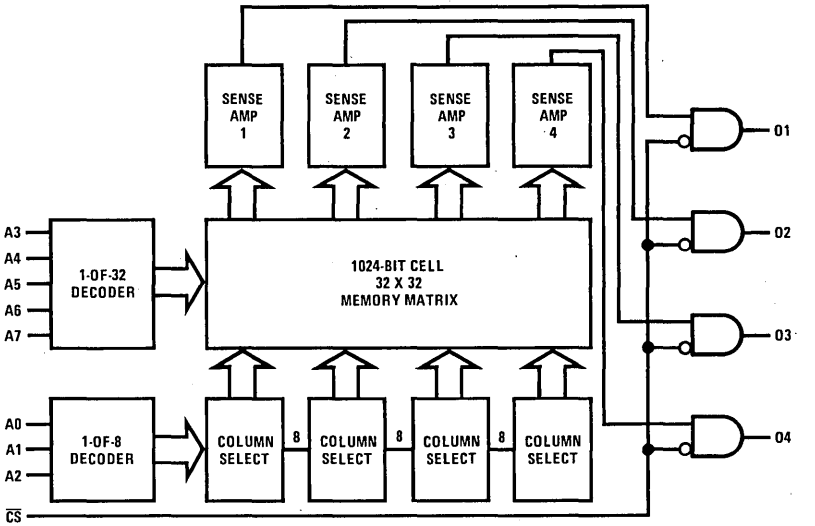
The DM100416 is a fully decoded high speed 1024-bit field Programmable Read Only Memory, organized 256 words by 4 bits. The DM100416 is voltage and temperature compensated and compatible with the 100k family. The device is enabled when $\overline{CS}$ is LOW. Programmed bits will furnish HIGH levels at corresponding outputs. When the device is disabled ($\overline{CS}$ is HIGH) all outputs are LOW.

See the last page of this section for detailed programming information.

Features

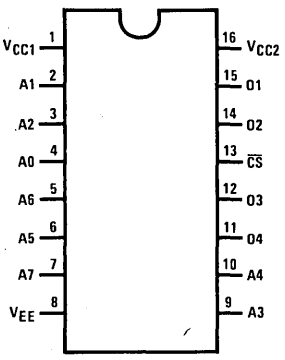
- Fast cycle time—12 ns typ
- Organization—256 words x 4 bits
- 100k logic
- Chip select input provides easy memory expansion
- Open emitter outputs for memory expansion
- Standard 16-pin dual-in-line package
- Full address decoding on chip

Block Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

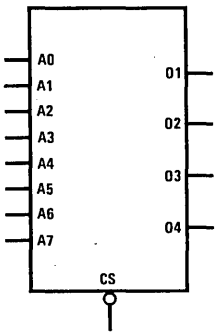
Pin Names

$\overline{CS}$	Chip Select Input
A0 to A7	Address Inputs
O1 to O4	Data Outputs

Note:
V_{CC1} (Pin 1) is connected to the Programmer (+6.0V) during programming only.

V_{CC1} = GND (Read only) = Pin 1
V_{CC2} = GND = Pin 16
V_{EE} = Pin 8

Logic Symbol



Section 7

MOS ROMs

7

Program storage for microprocessors has become the fastest growing area of ROM application. As the performance of microprocessors and the sophistication of users increase, so will the requirements for large amounts of program storage. Also influencing larger ROM sizes is the trend toward higher level languages for microcomputers. The MAXI-ROM is a perfect vehicle for "Silicon Software" — which is National's name for putting high level languages such as INS8080A BASIC, PACE BASIC, and NIBL (National Industrial Basic Language) for the INS8060 (SC/MP) into mask-encoded ROM at a reasonable cost. Refer to National's Memory Applications Handbook for data on using the pin-compatible series of MAXI-ROMs.

National Semiconductor

MOS ROMs

MM5213 2048-Bit (256 x 8 or 512 x 4) ROM

General Description

The MM5213 is a 2048-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as a 256-8 bit words or 512-4 bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

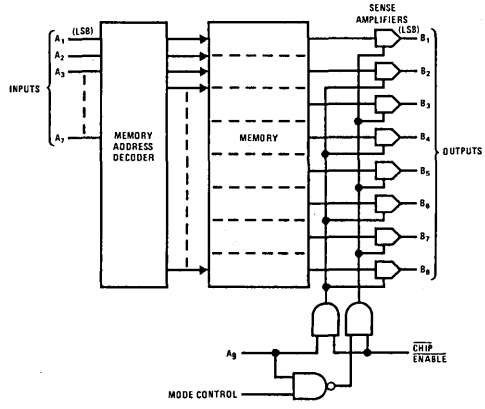
Features

- Bipolar compatibility — +5V, −12V operation
- High speed operation — 600 ns typ
- Pin compatible with MM5203 PROM
- Static operation — No clocks required
- Common data busing — Output wire AND capability
- Chip enable output control
- TRI-STATE output

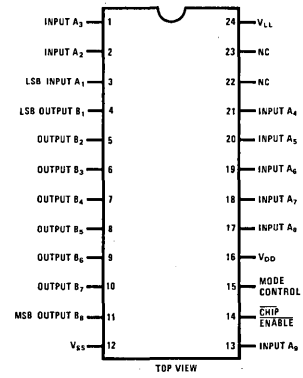
Applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming

Block and Connection Diagrams



Dual-In-Line Package



Order Number MM5213J
See NS Package J24A

Order Number MM5213N
See NS Package N24B

Note: For programming information see Memory Applications Handbook, page 4-6.

Absolute Maximum Ratings

V_{LL} Supply Voltage	V_{SS} – 20V
V_{DD} Supply Voltage	V_{SS} – 20V
Input Voltage	$(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + 0.3)\ V$
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Operating Conditions

Operating Temperature	0°C to +70°C

Electrical Characteristics POSITIVE LOGIC (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Current Capability					
Logical "1"	V_{OUT} = 2.4V	200			μA
Logical "0"	V_{OUT} = 0.4V	−1.6			mA
Input Voltage Levels					
Logical "0"				V_{SS} – 4.0	V
Logical "1"		V_{SS} – 2.0			V
Power Supply Current	T_A = 25°C				
I_{SS} (Note 2)	V_{SS} = +5V $V_{LL} = V_{DD}$ = −12V		20	40	mA
Input Leakage	V_{IN} = −12V			1	μA
Input Capacitance (Note 5)	f = 1.0 MHz, V_{IN} = 0V		5		pF
Address Time					
T_{ACCESS}	T_A = 25°C, V_{SS} = +5.0V $V_{GG} = V_{DD}$ = −12.0V		600	850	ns
Output AND Connections (Note 4)				10	

Note 1: These specifications apply for V_{SS} = +5.0V ±5%, V_{LL} = −12V, T_A = −25°C to +70°C unless otherwise specified.

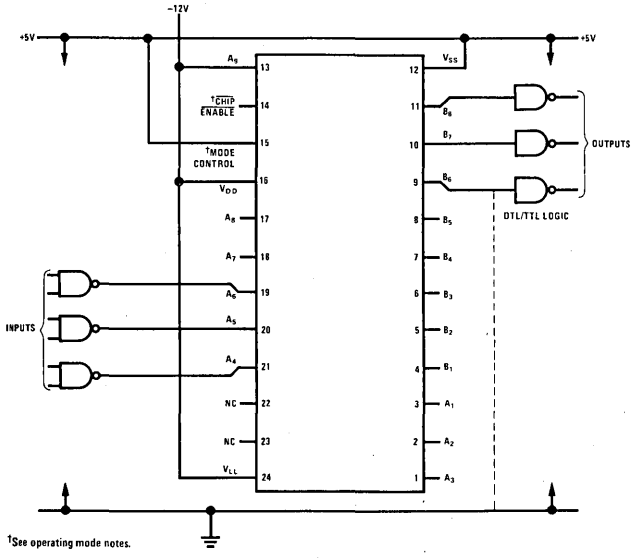
Note 2: Outputs open.

Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate.

Note 4: The address time in the TTL load configuration follows the equation: T_{ACCESS} = The specified limit + (N – 1) (25) ns. Where N = Number of AND connections.

Note 5: Capacitances are measured on a lot sample basis only.

Typical Applications (Continued)



†See operating mode notes.

Operating Modes

256x8 ROM connection (shown)
Mode Control – Logic "1"
A_9 – Logic "0"

512x4 ROM connection
Mode Control – Logic "0"
A_9 – Logic "1" Enables the odd (B_1, B_3 . . . B_9) outputs
– Logic "0" Enables the even (B_2, B_4 . . . B_8) outputs.

The outputs are "Enabled" when a logic "0" is applied to the Chip Enable line.

Mode Control should be "hard wired" to V_{LL} (Logical "0") or V_{SS} (Logical "1").

National Semiconductor

MOS ROMs

MM5214 4096-Bit (512 x 8) ROM

General Description

The MM5214 4096-bit static read only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology to achieve bipolar compatibility. TRI-STATE® outputs provide wire ORed capability without loading common data lines or reducing system access times. The ROM is organized in a 512 word x 8-bit memory organization.

Customer programs may be submitted for production in a paper tape or punched card format.

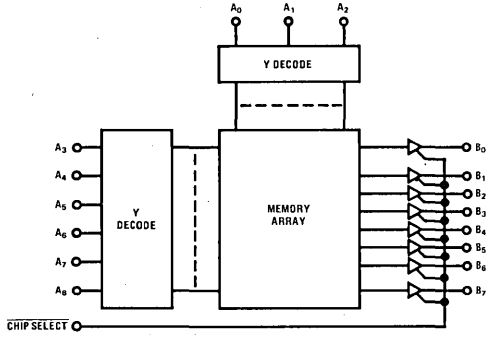
Features

- Pin compatible with MM5204 PROM
- Bipolar compatibility — No external components required
- Standard supplies — +5.0V, −12V
- Bus ORable output — TRI-STATE outputs
- Static operation — No clocks required

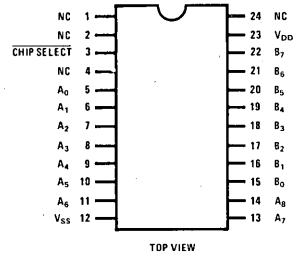
Applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

Logic and Connection Diagrams



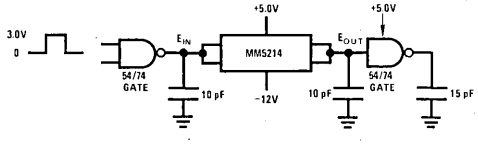
Dual-In-Line Package

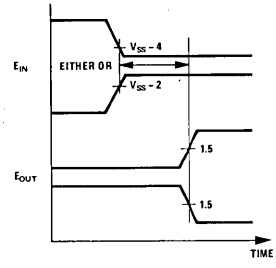


Order Number MM5214J
See NS Package J24A

Order Number MM5214N
See NS Package N24B

Timing Diagram/Address Time





Note: For programming information see Memory Applications Handbook, page 4-6.

Absolute Maximum Ratings

V_{DD} Supply Voltage $V_{SS} - 20V$
Input Voltage $(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + 0.03)\ V$
Storage Temperature Range $-65°C$ to $+150°C$
Lead Temperature (Soldering, 10 seconds) $300°C$

Operating Conditions

Operating Temperature Range $-25°C$ to $+70°C$

Electrical Characteristics POSITIVE LOGIC

T_A within operating temperature range, $V_{SS} = +5.0V \pm 5\%$, $V_{DD} = -12V \pm 5\%$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
Logical Low Level (V_{IL})	I_L = 1.6 mA Sink			0.4	V
Logical High Level (V_{IH})	I_L = 100μA Source	2.4			V
Input Voltage Levels					
Logical Low Level (V_L)				$V_{SS}-4.0$	V
Logical High Level (V_H)		$V_{SS}-2.0$			V
Power Supply Current (I_{SS}) (Note 4)	V_{SS} = 5.0V, V_{DD} = −12V, T_A = 25°C		23	37	mA
Input Leakage	$V_{IN} = V_{SS} - 10V$			1.0	μA
Input Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		5.0	10	pF
Output Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		4.0	10	pF
Address Time (T_{ACCESS}) (Note 2)	V_{DD} = −12V, V_{SS} = 5.0V, T_A = 25°C	150		1000	ns
Output AND Connections (Note 3)				20	

Note 1: Capacitances are measured periodically only.

Note 2: Address is measured from the change of data on any input or chip enable line to the output of a TTL gate. (See Timing Diagram.)

Note 3: The address time follows the following equation: T_{ACCESS} = The specified limit + (N−1) x 25 ns where N = Number of AND connections.

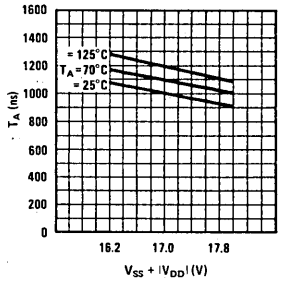
Note 4: Outputs open.

Note 5: Positive true logic notation is used. Logic "1" = most positive voltage level. Logic "0" = most negative voltage level.

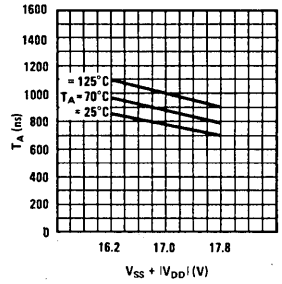
Note 6: Chip is enabled when Chip Select is low.

Typical Performance Characteristics

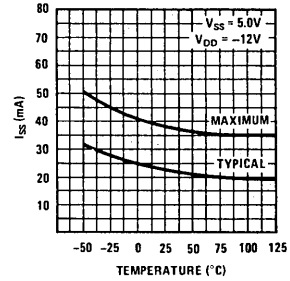
Guaranteed Access Time vs Supply Voltage



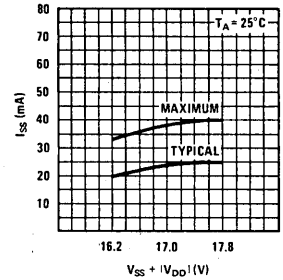
Typical Access Time vs Supply Voltage



Power Supply Current vs Temperature



Power Supply Current vs Voltage



National Semiconductor

MOS ROMs

MM5220 1024-Bit (128 × 8 or 256 × 4) ROM

General Description

The MM5220 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as 128-8-bit words or 256-4-bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication. Customer programs may be supplied in a tape, card, or pattern selection format.

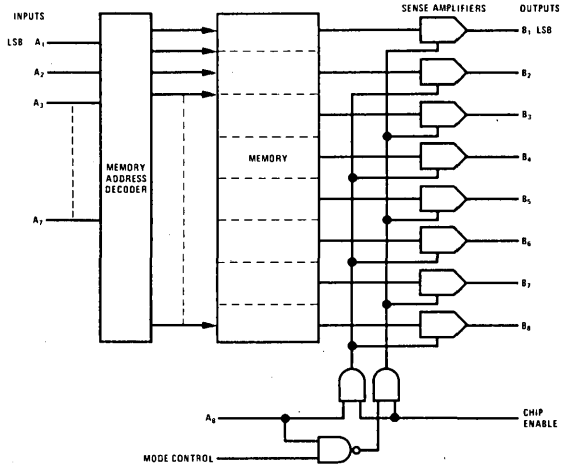
Features

- Bipolar compatibility
- High speed operation — 500 ns typ
- Static operation — no clocks required
- Common data busing — output wire AND capability
- Chip enable output control.

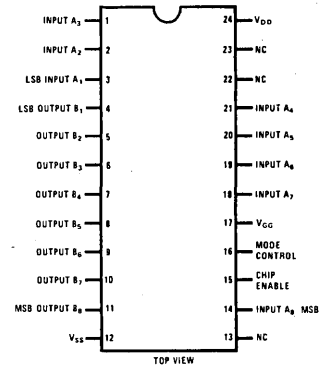
Applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming

Block and Connection Diagrams



Dual-In-Line Package



Order Number MM5220J
See NS Package J24A

Order Number MM5220N
See NS Package N24B

Note: For programming information see Memory Applications Handbook, page 4-6.

Absolute Maximum Ratings

V_{GG} Supply Voltage	$V_{SS}-30V$
V_{DD} Supply Voltage	$V_{SS}-15V$
Input Voltage	$(V_{SS}-20)V < V_{IN} < (V_{SS}+0.3)V$
Storage Temperature	$-65°C$ to $+150°C$
Lead Temperature (Soldering, 10 sec)	$300°C$

Operating Conditions

Operating Temperature	$0°C$ to $+70°C$

Electrical Characteristics

T_A within operating temperature range, V_{SS} = +12V ±5% and V_{GG} = −12V ±5%, unless otherwise specified.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	1 MΩ to GND Load (Note 1)			V_{SS} −9.0	V
Logical "0"		V_{SS} −1.0			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate Input	+2.4			V
Input Voltage Levels					
Logical "1"				V_{SS} −8.0	V
Logical "0"		V_{SS} −2.0			V
Power Supply Current	$T_A = 25°C$				
V_{SS}			19	25	mA
V_{GG} (Note 1)				1	μA
Input Leakage	$V_{IN} = V_{SS}$ −12V			1	μA
Input Capacitance	f = 1.0 MHz V_{IN} = 0V		5		pF
Access Time (Notes 2, 3)	$T_A = 25°C$				
T_{ACCESS}	(See Timing Diagram) V_{SS} = +12V V_{GG} = −12V	150	500	650	ns
Output AND Connection	MOS Load			3	
	TTL Load			8	

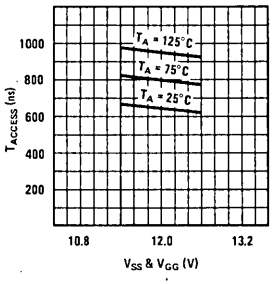
Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. See Timing Diagram.

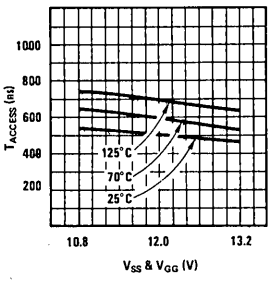
Note 3: The access time in the TTL load configuration follows the equation: T_{ACCESS} = the specified time + (N − 1) (50) ns where N = number of AND connections.

Performance Characteristics

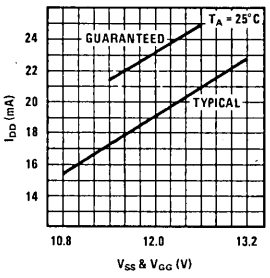
Guaranteed Access Time vs Supply Voltages



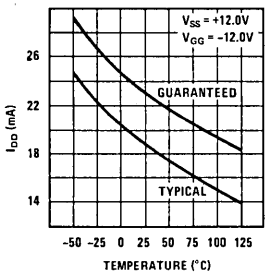
Typical Access Time vs Supply Voltages



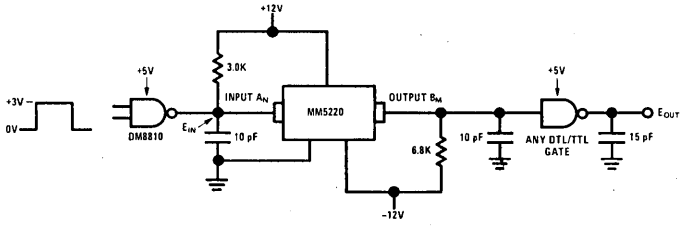
Power Supply Current vs Voltage

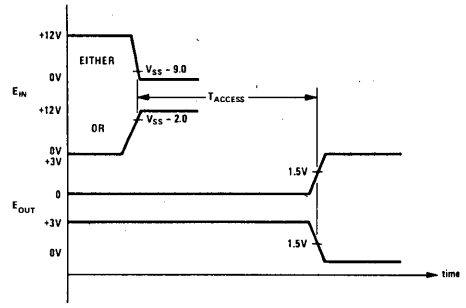


Power Supply Current vs Temperature



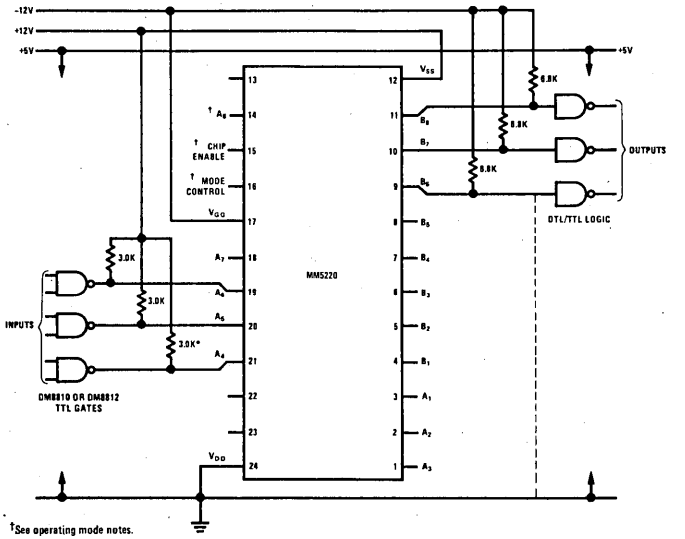
Timing Diagram/Address Time





Typical Application

128-8 Bit ROM Showing TTL Interface



†See operating mode notes.

*R values can vary from 740 to 30 kΩ depending on speed requirements.

Operating Modes

128x8 ROM connection
Mode Control – Logic "0"
A_8 – Logic "1"

256x4 ROM connection
Mode Control – Logic "1"
A_8 – Logic "0" Enables the odd ($B_1 \ldots B_7$) outputs
– Logic "1" Enables the even ($B_2 \ldots B_8$) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

The outputs are connected to V_{DD} through an internal MOS resistor when "Disabled."

The logic levels are in negative voltage logic notation.

National Semiconductor

MM5221 1024-Bit (128 × 8 or 256 × 4) ROM

General Description

The MM5221 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as 128-8-bit words or 256-4-bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

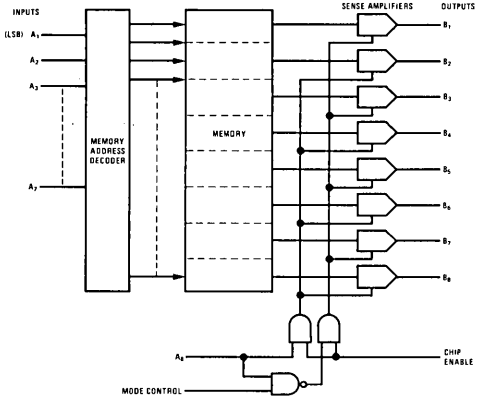
Features

- Bipolar compatibility — +5V, −12V operation
- High speed operation — <700 ns typ
- Static operation — no clocks required
- Common data busing — output wire AND capability
- Chip enable output control

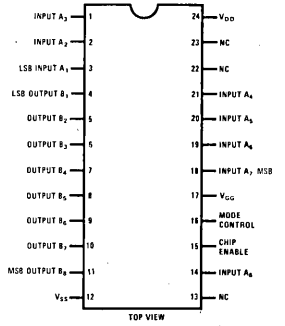
Applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming.

Block and Connection Diagrams



Dual-In-Line Package



Order Number MM5221J
See NS Package J24A

Order Number MM5221N
See NS Package N24B

Note: For programming information see Memory Applications Handbook, page 4-6.

Absolute Maximum Ratings

V_{GG} Supply Voltage	V_{SS} – 20V
V_{DD} Supply Voltage	V_{SS} – 20V
Input Voltage	$(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Operating Conditions

Operating Temperature	0°C to +70°C

Electrical Characteristics

T_A within operating temperature range, V_{SS} = +5V ±5%, V_{GG} = V_{DD} = −12V ±5%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to TTL					
Logical "1"	6.8 kΩ ±5% to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	+2.4			V
Output Current Capability					
Logical "0"	V_{OUT} = 2.4V	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} – 4.2	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current	T_A = 25°C				
I_{DD}	V_{SS} = +5V		6.5	12.0	mA
I_{GG} (Note 1)	V_{GG} = V_{DD} = −12V			1	μA
Input Leakage	V_{IN} = V_{SS} – 12V			1	μA
Input Capacitance	f = 1.0 MHz, V_{IN} = 0V		5		pF
V_{GG} Capacitance (Note 4)	f = 1.0 MHz, V_{IN} = 0V		15	25	pF
Address Time (Note 2)	See Timing Diagram				
T_{ACCESS}	T_A = 25°C, V_{SS} = 5V V_{GG} = V_{DD} = −12V		700	950	ns
Output AND Connections (Note 3)	6.8 kΩ ±5% to V_{GG} Plus One Standard Series 54/74 Gate			8	

Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

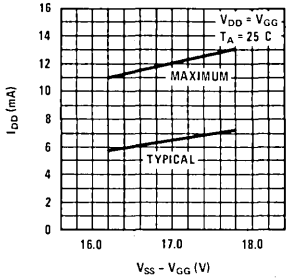
Note 2: Address time is measured from the change of data on any input except mode control or Chip Enable line to the output of a TTL gate. (See Timing Diagram). See curves for guaranteed limit over temperature.

Note 3: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N – 1) (50) ns
Where N = Number of AND connections.

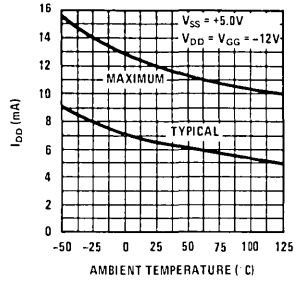
Note 4: Capacitance guaranteed by design.

Performance Characteristics

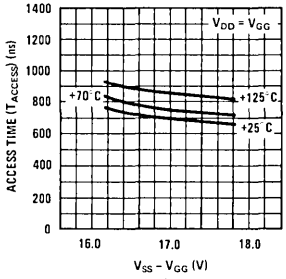
Power Supply Current vs
Power Supply Voltages



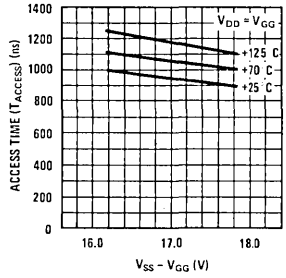
Power Supply Current vs
Ambient Temperature



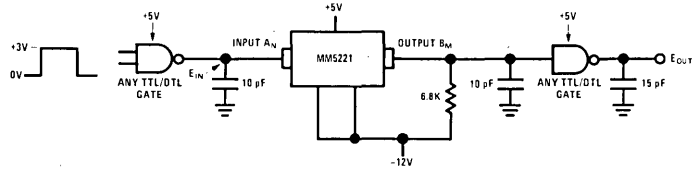
Typical Access Time vs
Power Supply Voltages

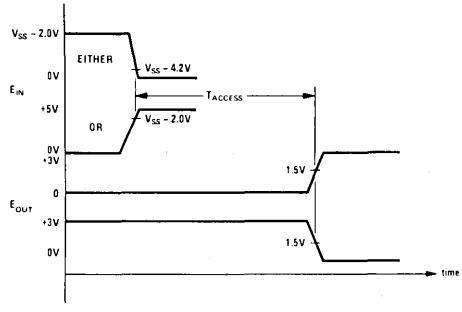


Guaranteed Access Time vs
Power Supply Voltages



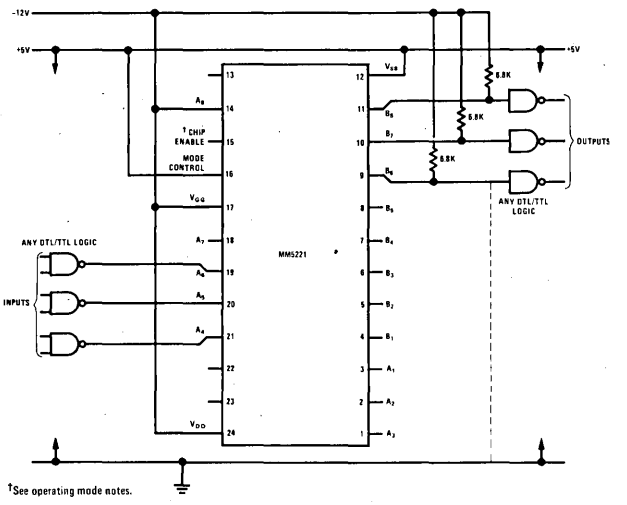
Timing Diagram/Address Time





Typical Application

128-8 Bit ROM Showing TTL Interface



Operating Modes

128x8 ROM connection
Control – Logic "0"
A_8 – Logic "1"

256x4 ROM connection
Control – Logic "1"
A_8 – Enables the odd ($B_1 \ldots B_7$) or even ($B_2 \ldots B_8$) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

The outputs are connected to ground through an internal MOS resistor when "Disabled."

Logic levels are negative true MOS logic.

Mode control should be "hard wired" to either V_{DD} (logical "1") or V_{SS} (logical "0").

The logic levels are in negative voltage logic notation.

National Semiconductor

MOS ROMs

MM5230 2048-Bit (256 × 8 or 512 × 4) ROM

General Description

The MM5230 is a 2048-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as 256-8 bit words or 512-4 bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication. Customer programs may be supplied in a tape, card, or pattern selection format.

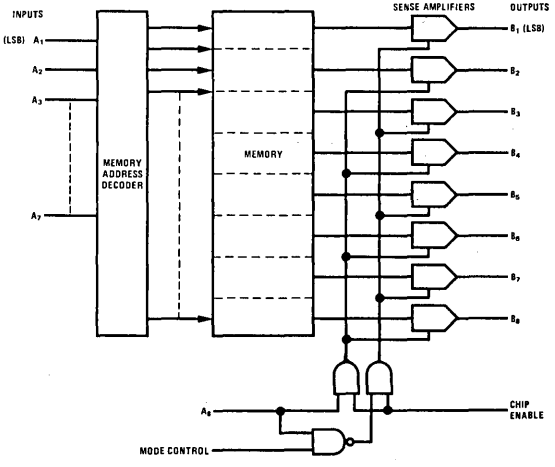
Features

- Bipolar compatibility
- High speed operation — 500 ns typ
- Static operation — no clocks required
- Common data busing — output wire AND capability
- Chip enable output control.

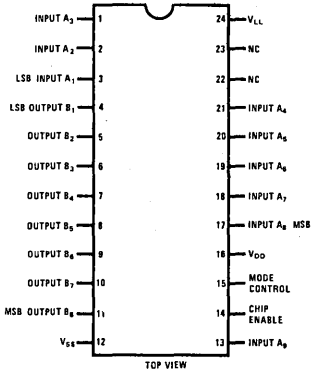
Applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Microprogramming.

Block and Connection Diagrams



Dual-In-Line Package



Order Number MM5230J
See NS Package J24A

Order Number MM5230N
See NS Package N24B

Note: For programming information see Memory Applications Handbook, page 4-6.

Absolute Maximum Ratings

V_{GG} Supply Voltage	$V_{SS}-30V$
V_{DD} Supply Voltage	$V_{SS}-15V$
Input Voltage	$(V_{SS}-20)V < V_{IN} < (V_{SS}+0.3)V$
Storage Temperature	$-65°C$ to $+150°C$
Lead Temperature (Soldering, 10 sec)	$300°C$

Operating Conditions

Operating Temperature	$0°C$ to $+70°C$

Electrical Characteristics

T_A within operating temperature range, $V_{SS} = +12V \pm 5\%$ and $V_{GG} = -12V \pm 5\%$, unless otherwise specified.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	1 MΩ to GND Load (Note 1)			$V_{SS}-9.0$	V
Logical "0"		$V_{SS}-1.0$			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate Input	+2.4			V
Input Voltage Levels					
Logical "1"				$V_{SS}-8.0$	V
Logical "0"		$V_{SS}-2.0$			V
Power Supply Current	$T_A = 25°C$				
V_{SS}			24	40	mA
V_{GG} (Note 1)				1	μA
Input Leakage	$V_{IN} = V_{SS}-12V$			1	μA
Input Capacitance	f = 1.0 MHz $V_{IN} = 0V$		5		pF
Access Time (Notes 2, 3)	$T_A = 25°C$				
T_{ACCESS}	(See Timing Diagram) $V_{SS} = +12V$ $V_{GG} = -12V$	150	500	725	ns
Output AND Connection	MOS Load			3	
	TTL Load			8	

Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

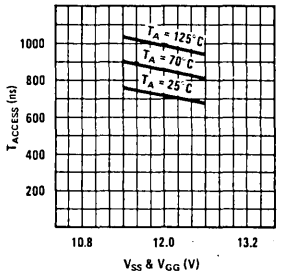
Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. See Timing Diagram.

Note 3: The access time in the TTL load configuration follows the equation: T_{ACCESS} = the specified time + (N − 1) (50) ns where N = number of AND connections.

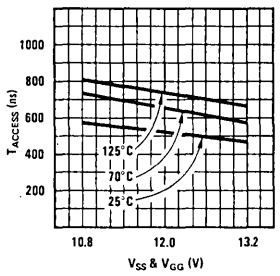
Note 4: The above logic levels are indicated in negative logic notation.

Performance Characteristics

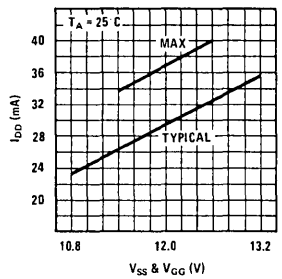
Guaranteed Access Time vs Supply Voltages



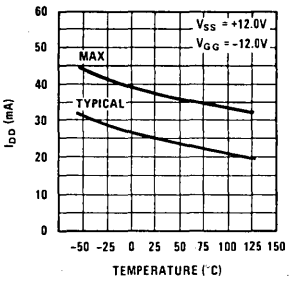
Typical Access Time vs Supply Voltages



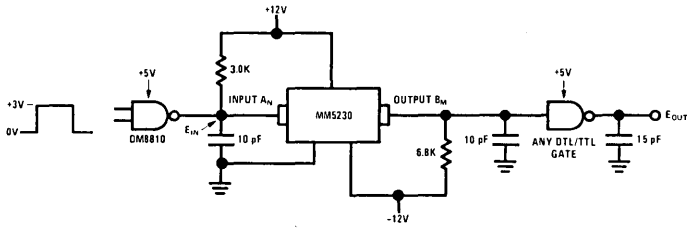
Power Supply Current vs Voltages

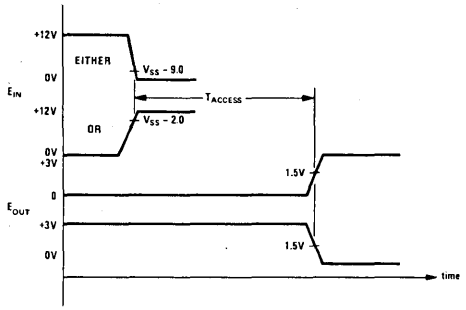


Power Supply Current vs Temperature



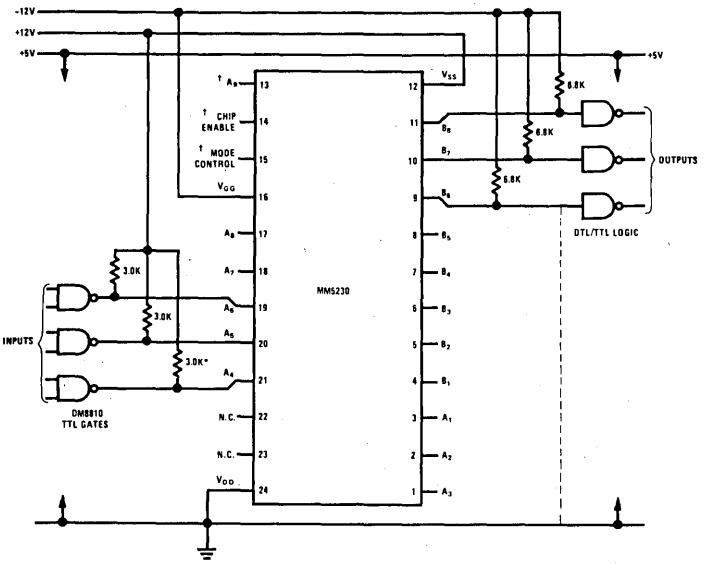
Timing Diagram/Address Time





Typical Application

256 x 8 Bit ROM Showing TTL Interface



†See operating mode notes.
*R values can vary from 740Ω to 30 kΩ.

Operating Modes

128x8 ROM connection
Mode Control – Logic "0"
A_9 – Logic "1"

256x4 ROM connection
Mode Control – Logic "1"
A_9 – Logic "0" Enables the odd ($B_1 \ldots B_7$) outputs
– Logic "1" Enables the even ($B_2 \ldots B_8$) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

The outputs are connected to V_{DD} through an internal MOS resistor when "Disabled."

The logic levels are in negative voltage logic notation.

National Semiconductor

MM5231 2048-Bit (256 × 8 or 512 × 4) ROM

General Description

The MM5231 is a 2048-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as a 256-8 bit words or 512-4 bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

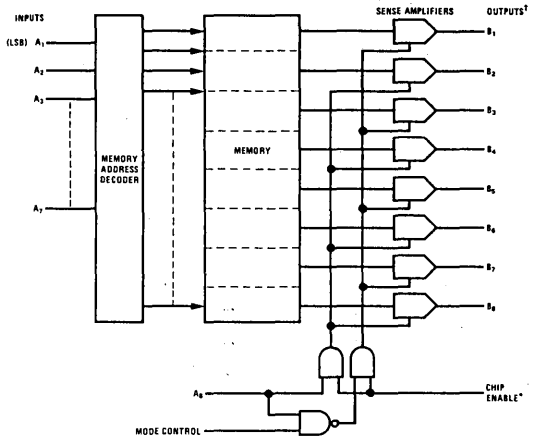
Features

- Bipolar compatibility — +5V, −12V operation
- High speed operation — 640 ns typ.
- Static operation — No clocks required
- Common data busing — Output wire AND capability
- Chip enable output control

Applications

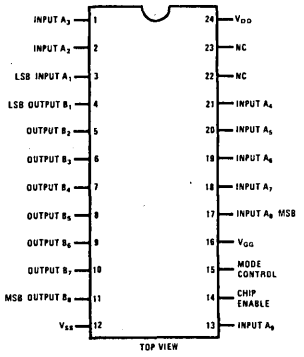
- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Microprogramming

Block and Connection Diagrams



† The outputs are open when Disabled.
* The output is enabled by applying a Logic "1" to the Chip Enable line.

Dual-In-Line Package



Order Number MM5231J
See NS Package J24A

Order Number MM5231N
See NS Package N24B

Note: For programming information see Memory Applications Handbook, page 4-6.

Absolute Maximum Ratings

V_{GG} Supply Voltage V_{SS} − 20V
V_{DD} Supply Voltage V_{SS} − 20V
Input Voltage $(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature −65°C to +150°C
Lead Temperature (Soldering, 10 sec) 300°C

Operating Conditions

Operating Temperature 0°C to +70°C

Electrical Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to TTL					
Logical "1"	6.8 kΩ ±5% to V_{DD} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	2.4			V
Output Current Capability					
Logical "0"	V_{OUT} = 2.4V	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} − 4.2	V
Logical "0"		V_{SS} − 2.0			V
Power Supply Current	T_A = 25°C				
I_{DD}	V_{SS} = +5V		15	30	mA
I_{GG} (Note 1)	$V_{GG} = V_{DD}$ = −12V			1	μA
Input Leakage	V_{IN} = −12V			1	μA
Input Capacitance	f = 1.0 MHz, V_{IN} = 0V		5		pF
V_{GG} Capacitance	f = 1.0 MHz, V_{IN} = 0V		15		pF
Address Time (Note 2)	See Timing Diagram				
T_{ACCESS}	T_A = 25°C V_{SS} = +5.0V $V_{GG} = V_{DD}$ = −12.0V		640	950	ns
Output AND Connections (Note 3)	6.8 kΩ ±5% to V_{DD} Plus One Standard Series 54/74 Gate			8	

Note 1: These specifications apply for V_{SS} = +5V ±5%, $V_{GG} = V_{DD}$ = −12V ±5%, T_A = −25°C to +70°C unless otherwise specified.

Note 2: The V_{GG} supply may be clocked to reduce device power without affecting access time.

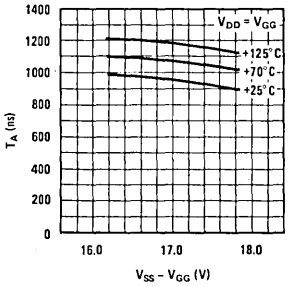
Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.) See curves for guaranteed limit over temperature.

Note 4: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N − 1) (50) ns.
Where N = Number of AND connections.

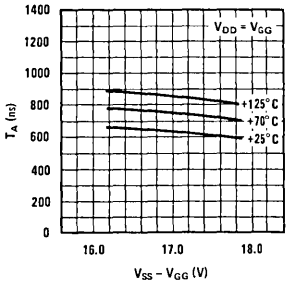
Note 5: Capacitances are measured on a lot sample basis only.

Performance Characteristics

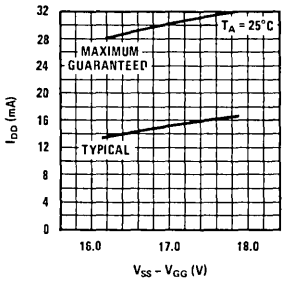
Guaranteed Access Time (T_A) vs Power Supply Voltage



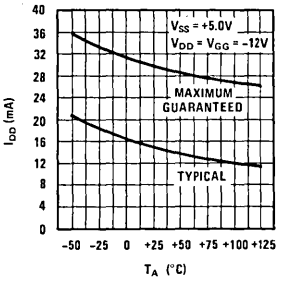
Typical Access Time (T_A) vs Power Supply Voltage



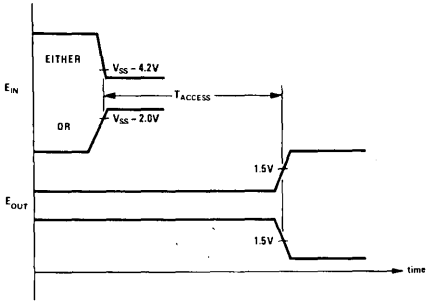
Power Supply Current vs Power Supply Voltage

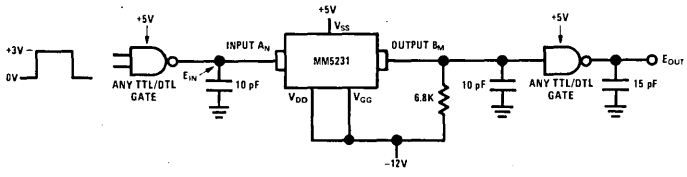


Power Supply Current vs Ambient Temperature



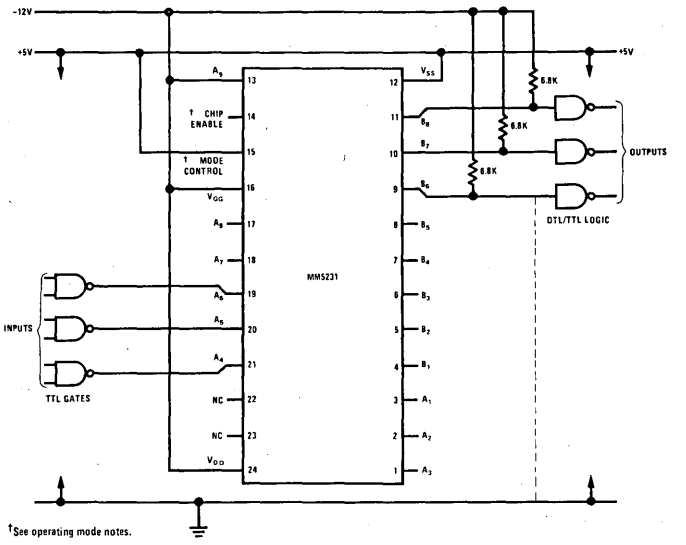
Timing Diagram/Address Time





Typical Application

256 x 8 Bit ROM Showing TTL Interface



Operating Modes

256 x 8 ROM connection (shown)
Mode Control – Logic "0"
A_9 – Logic "1"

512 x 4 ROM connection
Mode Control – Logic "1"
A_9 – Logic "0" Enables the odd (B_1, B_3 . . . B_9) outputs
– Logic "1" Enables the even (B_2, B_4 . . . B_8) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

Logic levels are negative true MOS logic.

Mode Control should be "hard wired" to V_{DD} (Logical "1") or V_{SS} (Logical "0").

The logic levels are in negative voltage logic notation.

National Semiconductor

MM5232 4096-Bit (512 x 8 or 1024 x 4) ROM

General Description

The MM5232 4096-bit static read only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology to achieve bipolar compatibility. TRI-STATE® outputs provide wire ORed capability without loading common data lines or reducing system access times. The ROM is organized in a 512 word x 8-bit or 1024 word x 4-bit memory organization that is controlled by the mode control input. Programmable Chip Enables (CE_1 and CE_2) provide logic control of up to 16K bits without external logic. A separate output supply lead is provided to reduce internal power dissipation in the output stages.

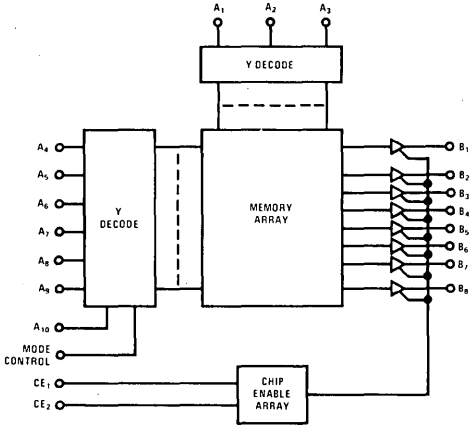
Features

■ Bipolar compatibility	No external components required
■ Standard supplies	+5V, −12V
■ Bus ORable output	TRI-STATE outputs
■ Static operation	No clocks required
■ Multiple ROM control	Two-programmable Chip Enable lines

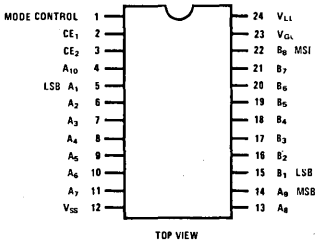
Applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

Block and Connection Diagrams



Dual-In-Line Package



Order Number MM5232J
See NS Package J24A

Order Number MM5232N
See NS Package N24B

Note: For programming information see Memory Applications Handbook, page 4-6.

Absolute Maximum Ratings

V_{GG} Supply Voltage	V_{SS} – 20V
V_{LL} Supply Voltage	V_{SS} – 20V
Input Voltage	$(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + .03)V$
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Operating Conditions

Operating Temperature Range	0°C to +70°C

Electrical Characteristics (Positive Logic)

T_A within operating temperature range, V_{SS} = +5.0V ±5%, $V_{GG} = V_{LL}$ = −12V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
Logical "0", V_{OL}	I_L = 1.6 mA Sink			.4	V
Logical "1", V_{OH}	I_L = 100 μA Source	2.4			V
Input Voltage Levels					
Logical "0", V_{IL}		V_{GG}		V_{SS} – 4.0	V
Logical "1", V_{IH}		V_{SS} – 2.0		V_{SS} + 0.3	V
Power Supply Current					
I_{SS} (Note 4)	V_{SS} = 5, V_{GG} = −12, V_{LL} = −12, T_A = 25°C		23	37	mA
Input Leakage	$V_{IN} = V_{SS}$ – 10V			1	μA
Input Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		5	15	pF
Output Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		4	10	pF
Address Time (Note 2)	T_A = 25°C, V_{SS} = 5	150		1000	ns
T_{ACCESS}	$V_{GG} = V_{LL}$ = −12V				
Output AND Connections (Note 3)				20	

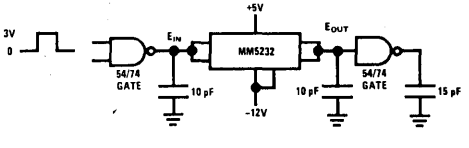
Note 1: Capacitances are measured periodically only.

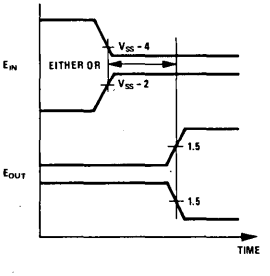
Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.)

Note 3: The address time follows the following equation: T_{ACCESS} = the specified limit + (N – 1) x 25 ns where N = Number of AND connections.

Note 4: Outputs open.

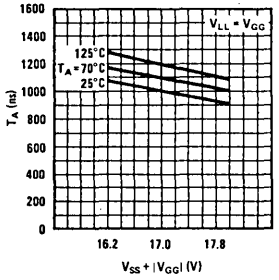
Timing Diagram/Address Time



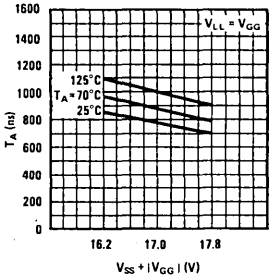


Performance Characteristics

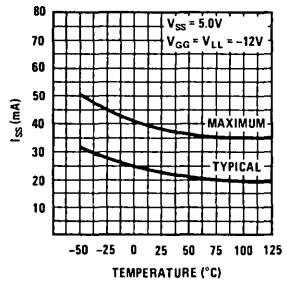
Guaranteed Access Time vs Supply Voltage



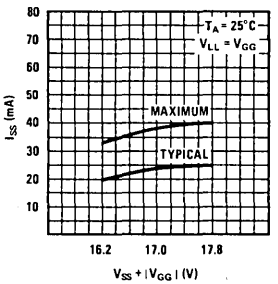
Typical Access Time vs Supply Voltage



Power Supply Current vs Temperature



Power Supply Current vs Voltage



Typical Applications

TTL/MOS Interface

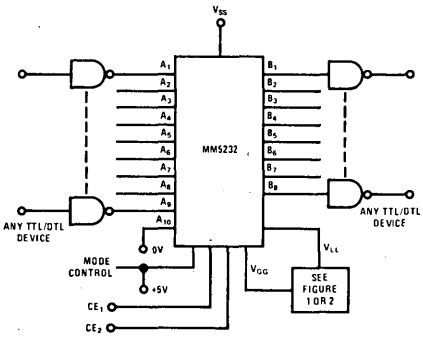
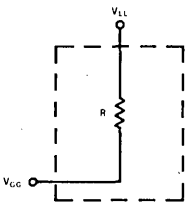
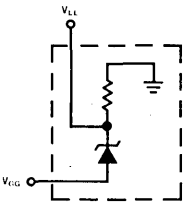


FIGURE 1. Power Saver for Small Memory Arrays



ASSUME $|V_{LL}|_{MIN} = |-3V|$
$V_{GG} - V_{LL}$ MIN = R (1.6 mA) (N) where N = 7 for 5 x 7 font.
N = 8 for 6 x 8 font.

FIGURE 2. Power Saver for Large Memory Arrays



Operating Modes

512 x 8 ROM connection
Mode Control = V_{IH}
$A_{10} = V_{IL}$

1024 x 4 ROM connection
Mode Control = V_{IL}
$A_{10} = V_{IL}$ enables the odd ($B_1 \ldots B_7$) outputs
V_{IH} enables the even ($B_2 \ldots B_8$) outputs

Note: Both chip enables may be programmed to provide any of four combinations. Example if $CE_1 = 1$ and $CE_2 = 1$ outputs (Positive Logic) would be enabled only when device pins 2 and 3 are Logic "1". The outputs will be in the third state when disabled.

National Semiconductor

MOS ROMs

MM5240 2560-Bit Static Character Generator

General Description

The MM5240 2560-bit static read only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology to achieve bipolar compatibility. TRI-STATE® outputs provide wire ORed capability without loading common data lines or reducing system access times. The ROM is organized in a 64 x 8 word by 5-bit memory organization.

The MM5240 may be used as a 512 x 5-bit read only memory for applications other than character generation.

Features

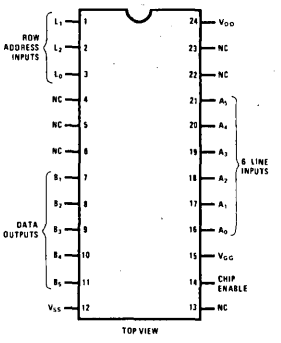
- Bipolar compatibility
- High speed operation—500 ns max
- ±12 volt power supplies
- Static operation—no clocks required
- Multiple ROM logic application—chip enable output control
- Standard fonts available—off-the-shelf delivery

Applications

- Character generation
- Random logic synthesis
- Micro-programming
- Table look-up

Connection Diagram

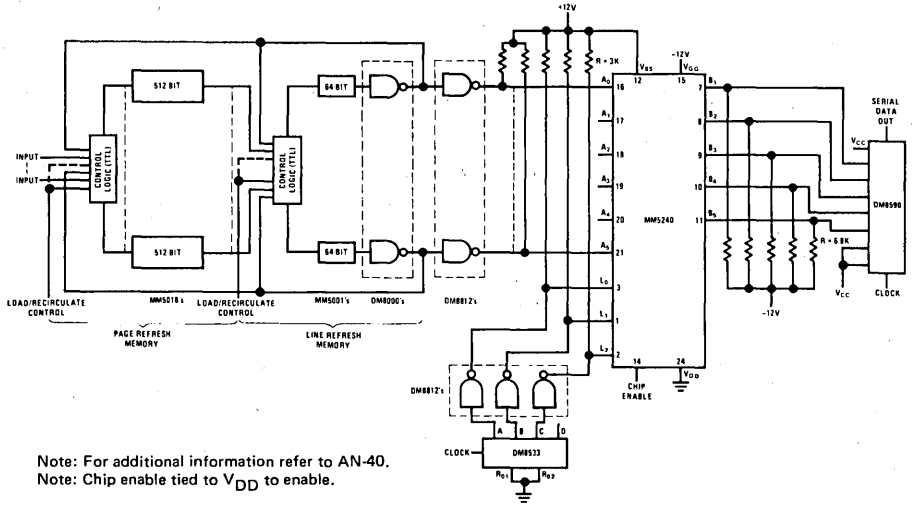
Dual-In-Line Package



Order Number MM5240J
See NS Package J24A

Order Number MM5240N
See NS Package N24B

Typical Application



Note: For additional information refer to AN-40.
Note: Chip enable tied to V_{DD} to enable.

Absolute Maximum Ratings

V_{GG} Supply Voltage V_{SS} - 30V
V_{DD} Supply Voltage V_{SS} - 15V
Input Voltage $(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature -65°C to +150°C
Lead Temperature (Soldering, 10 sec) 300°C

Operating Conditions

Operating Temperature 0°C to +70°C

Electrical Characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	IMΩ to GND			V_{SS} - 9.0	V
Logical "0"		V_{SS} - 1.0			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	+2.5			V
Output Current Capability					
Logical "0"	$V_{OUT} = V_{SS} - 6.0V$	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} - 8.0	V
Logical "0"		V_{SS} - 2.0			V
Power Supply Current	$T_A = 25°C$				
I_{DD}	MOS Load		25	55	mA
I_{GG} (Note 2)				1	μA
Input Leakage	$V_{IN} = V_{SS} - 12V$			1	μA
Input Capacitance (Note 5)	f = 1.0 MHz, V_{IN} = 0V		5	8	pF
V_{GG} Capacitance (Note 5)	f = 1.0 MHz, V_{IN} = 0V		25	40	pF
Address Time (Note 3)	See Timing Diagram				
T_{ACCESS}	$T_A = 25°C$	150	425	500	ns
Output AND Connection	MOS Load			4	
(Note 4)	TTL Load			10	

Note 1: These specifications apply for V_{SS} = +12V ±5%, V_{GG} = −12V ±5%, T_A = 0°C to +70°C unless otherwise specified.

Note 2: The V_{GG} supply may be clocked to reduce device power without affecting access time.

Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram). See curves for guaranteed limit over temperature.

Note 4: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N − 1) (50) ns

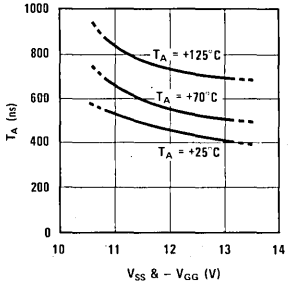
Where N = Number of AND connections.

The number of AND ties in the MOS load configuration can be increased at the expense of MOS "0" level.

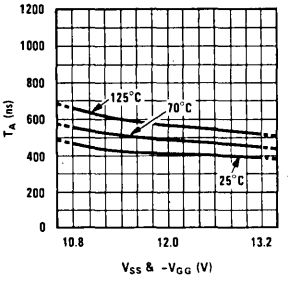
Note 5: Guaranteed by design.

Performance Characteristics

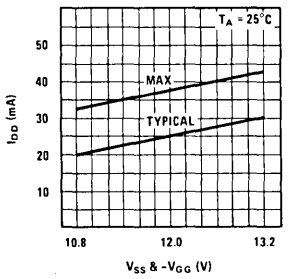
Guaranteed Access Time (T_A) vs Supply Voltage



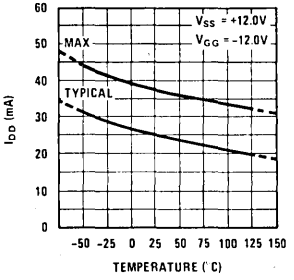
Typical Access Time (T_A) vs Supply Voltage



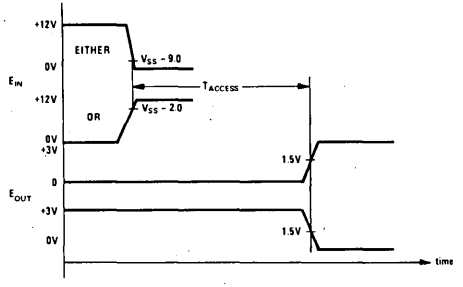
Power Supply Current vs Voltage

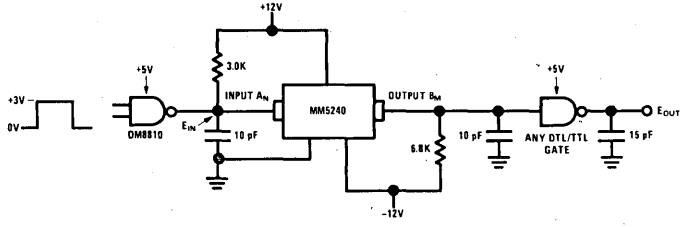


V_{DD} Power Supply Current vs Temperature



Timing Diagram/Address Time





National Semiconductor

MOS ROMs

MM5241 3072-Bit (64 × 6 × 8) ROM

General Description

The MM5241 3072-bit static read only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology to achieve bipolar compatibility. TRI-STATE® outputs provide wire ORed capability without loading common data lines or reducing system access times. The ROM is organized in a 64 x 6 word by 8-bit memory organization. Programmable Chip Enables (CE_1 and CE_2) provide logic control of multiple packages without external logic. A separate output supply lead is provided to reduce internal power dissipation in the output stages.

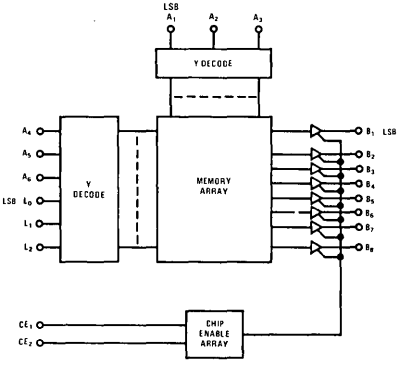
Features

■ Bipolar compatibility	No external components required
■ Standard supplies	+5V, −12V
■ Bus ORable output	TRI-STATE outputs
■ Static operation	No clocks required
■ Multiple ROM control	Two programmable Chip Enable lines

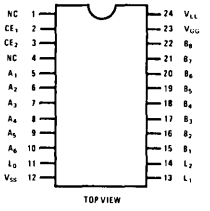
Applications

- Character generator
- Random logic synthesis
- Microprogramming
- Table look-up

Block and Connection Diagrams



Dual-In-Line Package



Order Number MM5241J
See NS Package J24A

Order Number MM5241N
See NS Package N24B

Typical Applications

TTL/MOS Interface

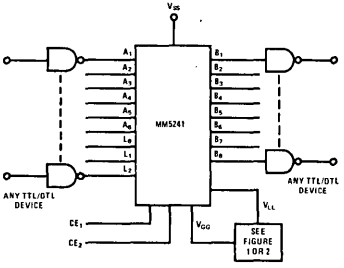


FIGURE 1. Power Saver for Small Memory Arrays

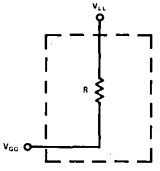
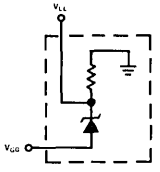


FIGURE 2. Power Saver for Large Memory Arrays



ASSUME $|V_{LL}|_{MIN} = |-3V|$
$V_{GG} - V_{LL}$ MIN = R (1.6 mA) (N) where N = 7 for 5 x 7 font.
N = 8 for 6 x 8 font.

Note: Both chip enables may be programmed to provide any of four combinations. Example: If $CE_1 = 1$ and $CE_2 = 1$ outputs (Negative Logic) would be enabled only when device pins 2 and 3 are negative (Logic "1"). The outputs will be in the third state when disabled. L_0, L_1 and L_2 (device pins 11, 13 and 14) are in positive logic (1 = most positive voltage levels = $V_S - 2V$; 0 = most negative voltage level = $V_{SS} - 4V$).

Note: For programming information see Memory Applications Handbook, page 4-6.

Absolute Maximum Ratings

V_{GG} Supply Voltage	V_{SS} – 20V
V_{LL} Supply Voltage	V_{SS} – 20V
Input Voltage	$(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + .03)V$
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Operating Conditions

Operating Temperature Range	−25°C to +70°C

Electrical Characteristics (Negative Logic) (Note 5)

T_A within operating temperature range, V_{SS} = +5.0V ±5%, $V_{GG} = V_{LL}$ = −12V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
Logical "1"	I_L = 1.6 mA sink			.4	V
Logical "0"	I_L = 100 μA source	2.4			V
Input Voltage Levels					
Logical "1"				V_{SS} – 4.0	V
Logical "0"		V_{SS} – 2.0			V
Power Supply Current					
I_{SS} (Note 4)	V_{SS} = 5, V_{GG} = −12, V_{LL} = −12, T_A = 25°C		23	50	mA
Input Leakage	$V_{IN} = V_{SS}$ – 10V			1	μA
Input Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		5	15	pF
Output Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		4	10	pF
Address Time (Note 2) T_{ACCESS}	T_A = 25°C, V_{SS} = 5 $V_{GG} = V_{LL}$ = −12V	150	700	900	ns
Output AND Connections (Note 3)				20	

Note 1: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.) See curves for guaranteed limit over temperature.

Note 2: Capacitances are measured periodically only.

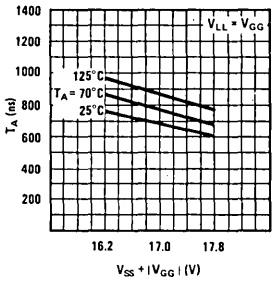
Note 3: The address time follows the following equation: T_{ACCESS} = the specified limit + (N – 1) x 25 ns where N = Number of AND connections.

Note 4: Outputs open.

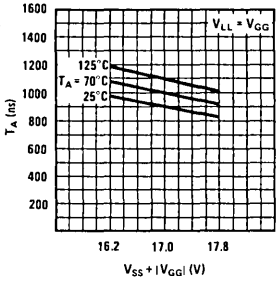
Note 5: All addresses and outputs are in negative true logic with the exception of L_0, L_1, and L_2 which are in positive logic.

Performance Characteristics

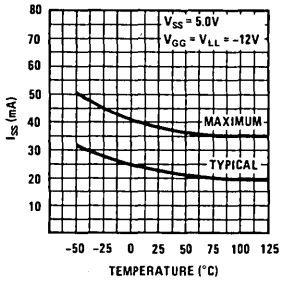
Typical Access Time vs Supply Voltage



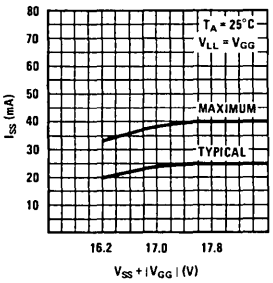
Guaranteed Access Time vs Supply Voltage



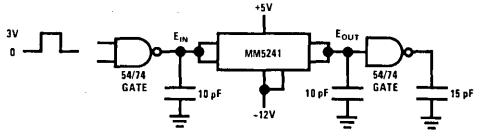
Power Supply Current vs Temperature

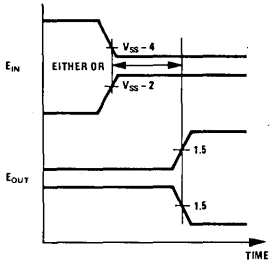


Power Supply Current vs Voltage



Timing Diagram/Address Time





National Semiconductor

MM52116 (2316E) 16,384-Bit Read Only Memory

General Description

The MM52116 is a static MOS 16,384-bit read-only memory organized in an 2048-word-by-8-bit format. It is fabricated using N-channel enhancement and depletion-mode technology which provides complete DTL/TTL compatibility and single power-supply operation.

Three programmable chip selects controlling the TRI-STATE® outputs allow for memory expansion.

Programming of the memory array and chip-select active levels is accomplished by changing two masks during fabrication.

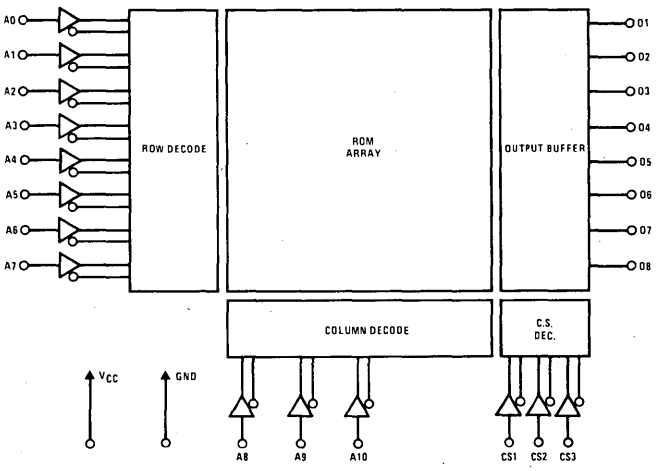
Features

- Fully decoded
- Single 5V power supply ±10% tolerance
- Inputs and outputs TTL compatible
- Outputs drive 2 TTL loads and 100 pF
- Static operation
- TRI-STATE outputs for bus interface
- Programmable chip selects
- 2048-word-by-8-bit organization
- Maximum access time — 450 ns
- Industry standard pin outs (2316E)
- Compatible to standard EPROMs

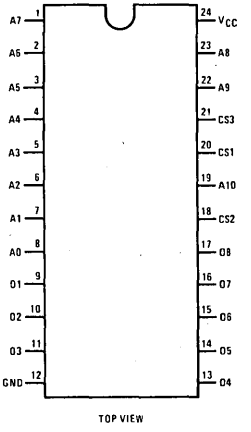
Applications

- Microprocessor instruction store
- Control logic
- Table look-up

Block and Connection Diagrams



Dual-In-Line Package



Order Number MM52116D
See NS Package D24C

Order Number MM52116N
See NS Package N24B

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.5V to +7.0V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

Operating Temperature Range	0°C to 70°C

DC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ±10%, unless otherwise specified).

PARAMETER (Note 2)		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
I_{LI}	Input Current	V_{IN} = 0 to V_{CC}			10	μA
V_{IH}	Logical "1" Input Voltage	0°C	2.0		V_{CC}+1.0	V
V_{IH}	Logical "1" Input Voltage	−40°C	2.2		V_{CC}+1.0	V
V_{IL}	Logical "0" Input Voltage		−0.5		0.8	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 3.2 mA			0.4	V
I_{LOH}	Output Leakage Current	V_{OUT} = 4V, Chip Deselected			10	μA
I_{LOL}	Output Leakage Current	V_{OUT} = 0.45V, Chip Deselected			−10	μA
I_{CC1}	Power Supply Current	All Inputs = 5.25V, Data Output Open		70	100	mA

Capacitance

PARAMETER (Note 3)		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			15.0	pF

AC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ±10%, unless otherwise specified). See AC test circuit and switching time waveforms.

PARAMETER		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
t_{AC}	Chip Select Access Time	See AC Test Circuit; t_{AC} and t_A Measured to Valid Output Levels with t_r and t_f of Input <20 ns, t_{OFF} Measured to <±20 μA Output Current			120	ns
t_{OFF}	Output Turn OFF Delay				100	ns
t_A	Address Access Time				450	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Positive true logic notation is used: logical "1" = most positive voltage level, logical "0" = most negative voltage level.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: Typical values are for T_A = 25°C and nominal supply voltage.

Switching Time Waveforms and AC Test Circuit

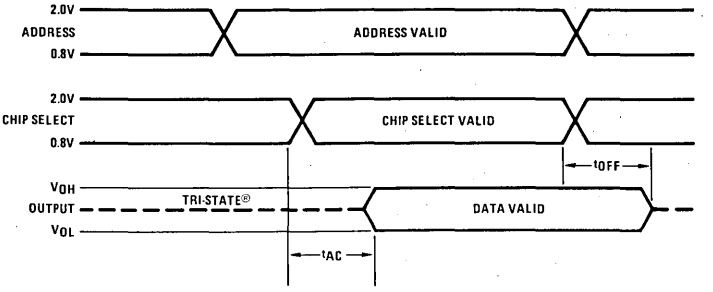


FIGURE 1. Address Precedes Chip Select

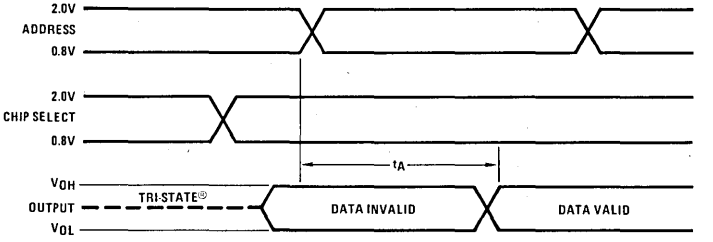
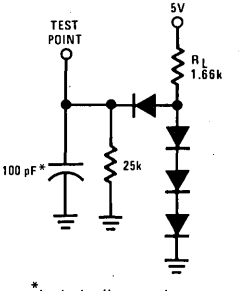


FIGURE 2. Address Follows Chip Select



*Includes jig capacitance

ROM Programming Information

ROM programs for the MM52116 can be supplied to National in a number of means:

A. 2708 PROM sets

B. 2516 PROM (or equivalent)

C. 2716 PROM (or equivalent)

D. Intellec HEX punched paper tape

E. Binary punched paper tape

Since the MM52116 has programmable chip selects, it is imperative that chip select information be provided along with the ROM program. The information should be supplied as shown:

CS1 is to be programmed logical_____(Hi or Lo)

CS2 is to be programmed logical_____(Hi or Lo)

CS3 is to be programmed logical_____(Hi or Lo)

Given any of the above means of program data is received by National, verification of ROM programs is handled internally via a sophisticated computerized system. The original input device (PROM, tape, etc.) is read, the data is reprocessed to formats required by various production machines, and the final reconstructed data is then compared back to the original input device.

The verification package returned to the customer for approval will consist of a listing of the program and a PROM or tape which matches the data National will use to create the programmed MM52116. In a normal situation, the verification package returned to the customer for approval, because of the system described, may consist of the original PROM or tape submitted by the customer. This program data, now in National's production format, is stored in archives for future customer re-orders.

National Semiconductor

MM52132 32,768-Bit (4096 × 8) MAXI-ROM™

General Description

The MM52132 is a static MOS 32,768-bit read-only memory organized in a 4096-word-by-8-bit format. It is fabricated using N-channel enhancement and depletion-mode technology which provides complete DTL/TTL compatibility and single power-supply operation.

Two programmable chip selects controlling the TRI-STATE® outputs allow for memory expansion.

Programming of the memory array and chip-select active levels is accomplished by changing two masks during fabrication.

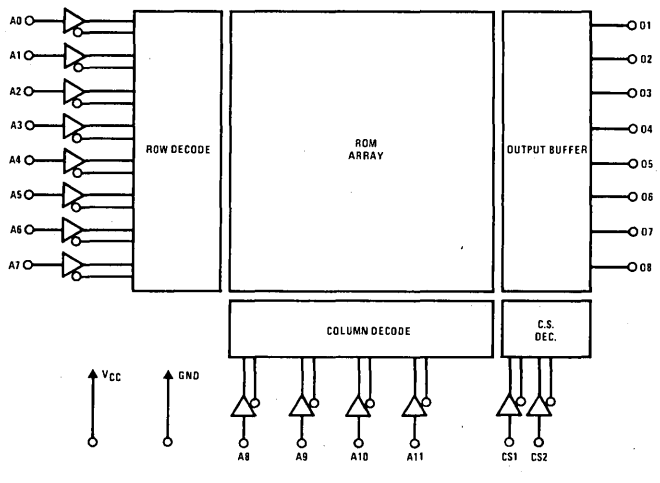
Features

- Fully decoded
- Single 5V power supply ±10% tolerance
- Inputs and outputs TTL compatible
- Outputs drive 2 TTL loads and 100 pF
- Static operation
- TRI-STATE outputs for bus interface
- Programmable chip selects
- 4096-word-by-8-bit organization
- Maximum access time — 450 ns
- Industry standard pin outs

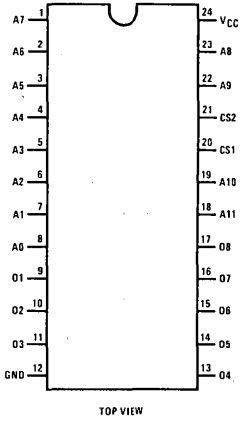
Applications

- Microprocessor instruction store
- Control logic
- Table look-up

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM52132D
See NS Package D24C
Order Number MM52132N
See NS Package N24B

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.5V to +6.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

Operating Temperature Range	0°C to +70°C

DC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ±10%, unless otherwise specified).

PARAMETER (Note 2)		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
I_{LI}	Input Current	V_{IN} = 0 to V_{CC}			10	μA
V_{IH}	Logical "1" Input Voltage		2		V_{CC}+1.0	V
V_{IL}	Logical "0" Input Voltage		−0.5		0.8	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −200 μA	2.4			V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 3.2 mA			0.4	V
I_{LOH}	Output Leakage Current	V_{OUT} = 4V, Chip Deselected			10	μA
I_{LOL}	Output Leakage Current	V_{OUT} = 0.45V, Chip Deselected			−20	μA
I_{CC1}	Power Supply Current	All Inputs = 5.25V, Data Output Open		100	130	mA

Capacitance

PARAMETER (Note 3)		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			15.0	pF

AC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ±10%, unless otherwise specified). See AC test circuit and switching time waveforms.

PARAMETER		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
t_{AC}	Chip Select Access Time	See AC Test Circuit. All Times (Except t_{OFF})			120	ns
t_{OFF}	Output Turn OFF Delay	Measured to 1.5V Level with t_r and t_f of			100	ns
t_A	Address Access Time	Input < 20 ns, *(Figures 1 and 2)*, t_{OFF} TRI-STATE Output Level Measured to Less than ±20 μA Output Current			450	ns

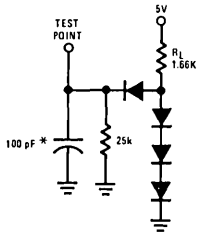
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Positive true logic notation is used: logical "1" = most positive voltage level, logical "0" = most negative voltage level.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: Typical values are for T_A = 25°C and nominal supply voltage.

AC Test Circuit and Switching Time Waveforms



*Includes jig capacitance

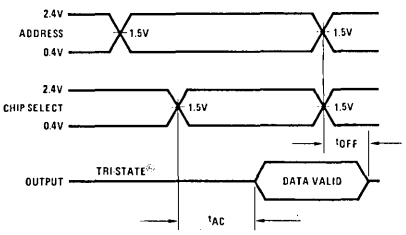


FIGURE 1. Address Precedes Chip Select

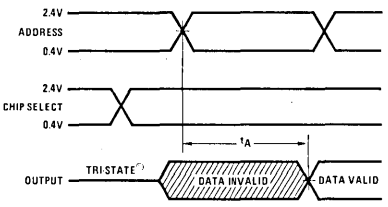


FIGURE 2. Address Follows Chip Select

Custom ROM Programming

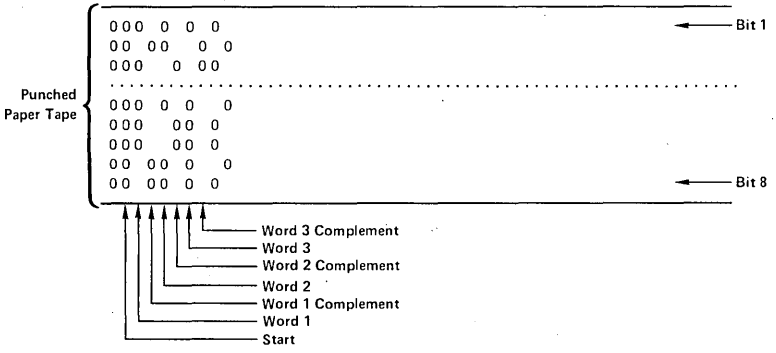
INFORMATION NEEDED

So that National can better serve its customers, the following information *must* be submitted with each ROM order.

National Semiconductor Corporation 2900 Semiconductor Dr., Santa Clara, CA. 95051 Phone (408) 737-5000 TWX 910-339-9240			NATIONAL PART NUMBER ROM LETTER CODE (NATIONAL USE ONLY)
NAME			DATE
ADDRESS			CUSTOMER PRINT OR ID NO.
CITY		STATE ZIP	PURCHASE ORDER NO.
TELEPHONE	NAME OF PERSON NATIONAL CAN CONTACT (PRINT)	AUTHORIZED SIGNATURE	DATE
CHIP SELECT INFORMATION		LOGIC ☐ POS ☐ NEG	
CS1	CS2	CS3	

Tape Entry Format

A. Binary Complement Format



POSITIVE Logic: A punch is a "1" or most positive voltage. Omission of a punch is a "0" or the more negative voltage.

Pre-Programmed PROM

B. Hex Format (Intel Standard Hex)

- 2708
- 2716
- Or combinations of the above to make 16k, 32k or 64k bits.

National Semiconductor

MM52164 65,536-Bit (8192 x 8) MAXI-ROM™

General Description

The MM52164 is a static MOS 65,536-bit read-only memory organized in an 8192-word by 8-bit format. It is fabricated using N-channel enhancement and depletion-mode technology which provides complete DTL/TTL compatibility and single power-supply operation.

One programmable chip select controlling the TRI-STATE® outputs allow for memory expansions.

Programming of the memory array and chip-select active levels is accomplished by changing two masks during fabrication.

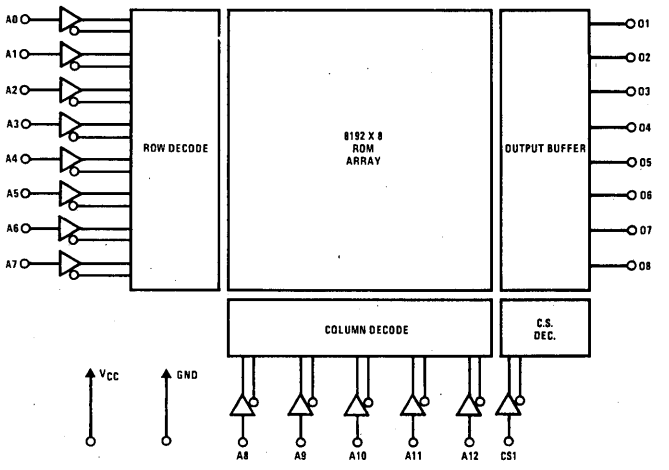
Features

- Fully decoded
- Single 5V power supply ±10% tolerance
- Inputs and outputs TTL compatible
- Outputs drive 2 TTL loads and 100 pF
- Static operation
- TRI-STATE outputs for bus interface
- Programmable chip select
- 8192-word-by-8-bit organization
- Maximum access time — 450 ns
- Industry standard pin outs

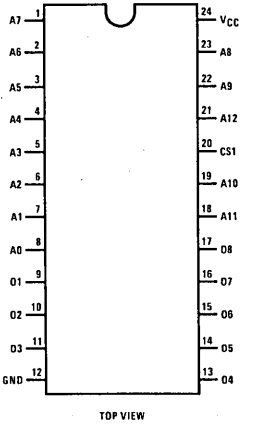
Applications

- Microprocessor instruction store
- Control logic
- Table look-up

Block and Connection Diagrams



Dual-In-Line Package



Order Number MM52164D
See NS Package D24C

Order Number MM52164N
See NS Package N24B

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.5V to +6.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

Operating Temperature Range	0°C to +70°C

DC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ±10%, unless otherwise specified).

PARAMETER (Note 2)		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
I_{LI}	Input Current	V_{IN} = 0 to V_{CC}			10	μA
V_{IH}	Logical "1" Input Voltage		2.2		V_{CC}+1.0	V
V_{IL}	Logical "0" Input Voltage		−0.5		0.6	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −200 μA	2.4			V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 3.2 mA			0.4	V
I_{LOH}	Output Leakage Current	V_{OUT} = 4V, Chip Deselected			10	μA
I_{LOL}	Output Leakage Current	V_{OUT} = 0.45V, Chip Deselected			−20	μA
I_{CC1}	Power Supply Current	All Inputs = 5.25V, Data Output Open		100	130	mA

Capacitance

PARAMETER (Note 3)		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			15.0	pF

AC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ±10%, unless otherwise specified). See AC test circuit and switching time waveforms.

PARAMETER		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
t_{AC}	Chip Select Access Time	See AC Test Circuit. All Times (Except t_{OFF})			120	ns
t_{OFF}	Output Turn OFF Delay	Measured to 1.5V Level with t_r and t_f of			100	ns
t_A	Address Access Time	Input < 20 ns, *(Figures 1 and 2)*, t_{OFF} TRI-STATE Output Level Measured to Less than ±20 μA Output Current			450	ns

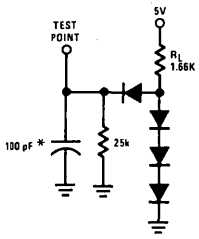
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Positive true logic notation is used: logical "1" = most positive voltage level, logical "0" = most negative voltage level.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: Typical values are for T_A = 25°C and nominal supply voltage.

AC Test Circuit and Switching Time Waveforms



*Includes jig capacitance

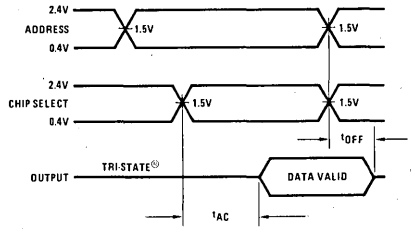


FIGURE 1. Address Precedes Chip Select

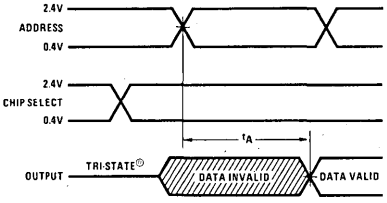


FIGURE 2. Address Follows Chip Select

Custom ROM Programming

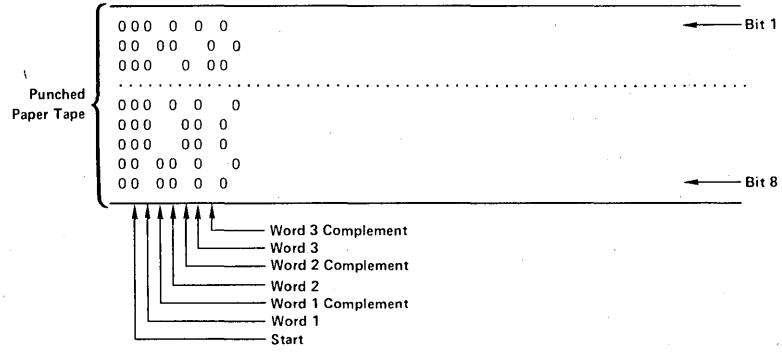
INFORMATION NEEDED

So that National can better serve its customers, the following information *must* be submitted with each ROM order.

National Semiconductor Corporation 2900 Semiconductor Dr., Santa Clara, CA. 95051 Phone (408) 737-5000 TWX 910-339-9240			NATIONAL PART NUMBER ROM LETTER CODE (NATIONAL USE ONLY)
NAME			DATE
ADDRESS			CUSTOMER PRINT OR ID NO.
CITY		STATE ZIP	PURCHASE ORDER NO.
TELEPHONE	NAME OF PERSON NATIONAL CAN CONTACT (PRINT)	AUTHORIZED SIGNATURE	DATE
CHIP SELECT INFORMATION		LOGIC ☐ POS ☐ NEG	
CS1	CS2	CS3	

Tape Entry Format

A. Binary Complement Format



POSITIVE Logic: A punch is a "1" or most positive voltage. Omission of a punch is a "0" or the more negative voltage.

Pre-Programmed PROM

B. Hex Format (Intel Standard Hex)

- 2708
- 2716
- Or combinations of the above to make 16k, 32k or 64k bits.

National Semiconductor

MOS ROMs
PREVIEW

MM52264 MAXI-ROM™ 65,536-Bit Clocked Read Only Memory

General Description

The MM52264 is a clocked MOS 65,536-bit read-only memory organized in an 8192-word-by-8-bit format. It is fabricated using N-channel enhancement and depletion-mode technology which provides complete DTL/TTL compatibility and single power-supply operation. Programming of the memory array is accomplished by changing two masks during fabrication.

The MM52264 was designed for those ROM applications requiring fast access time and low power dissipation. Dynamic circuitry has been used extensively to reduce access time. The utilization of a clock input allows the device to be put into a low power standby mode during inactive periods. The device is put into the standby mode by maintaining the clock input $\overline{CE}$ at an input "1" voltage. $\overline{CE}$ must be maintained at a "1" voltage for the minimum specified time (tp) to allow for adequate precharging of the internal dynamic circuitry.

After the address data has been applied to the device, a read operation is initiated by bringing $\overline{CE}$ to an input "0" voltage. The falling-edge of $\overline{CE}$ triggers the generation of a series of internal clock signals which latch address data in address buffers, decode addresses into row and column lines, and enable output sense amplifiers and buffers. Since the address is latched in address buffers, the input address data can be changed during a read operation after the address hold time (t_{AH}) specification is met.

Power dissipation increases during a read operation; however once the output data is latched in the TRI-STATE® output buffers, most of the dynamic circuitry is automatically switched off to conserve power.

The output data remains valid as long as $\overline{CE}$ is maintained at a "0" voltage level. Switching $\overline{CE}$ to a "1" voltage level will return the device to the standby mode and all data outputs to a high impedance OFF state.

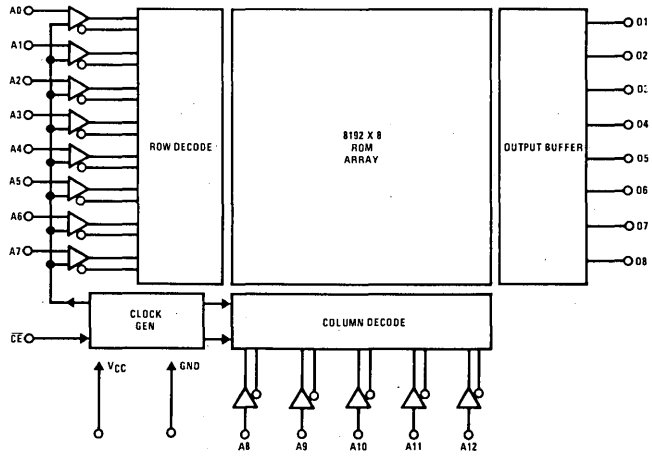
Features

- Fully decoded
- Single 5V power supply ±10% tolerance
- Inputs and outputs TTL compatible
- Outputs drive 2 TTL loads and 100 pF
- Clocked operation
- TRI-STATE outputs for bus interface
- 8192-word-by-8-bit organization
- Maximum access time — 300 ns
- Industry standard pin outs

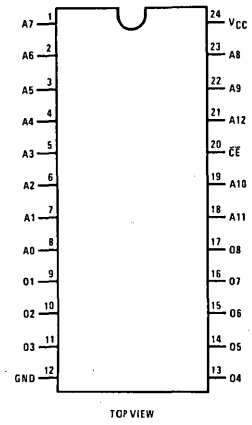
Applications

- Microprocessor instruction store
- Control logic
- Table look-up

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

7

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.5V to +6.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

Operating Temperature Range	0°C to +70°C

DC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ±10%, unless otherwise specified).

PARAMETER (Note 3)		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
I_{LI}	Input Current	V_{IN} = 0 to V_{CC}			10	μA
V_{IH}	Logical "1" Input Voltage		2.0		V_{CC}+1.0	V
V_{IL}	Logical "0" Input Voltage		−0.5		0.8	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −200 μA	2.4			V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 3.2 mA			0.4	V
I_{LOH}	Output Leakage Current	V_{OUT} = 4V, Chip Deselected			10	μA
I_{LOL}	Output Leakage Current	V_{OUT} = 0.45V, Chip Deselected			−10	μA
I_{CC1}	Power Supply Standby Current	All Inputs = 5.25V, Data Output Open		10	15	mA
I_{CC2}	Power Supply Active Current			30	50	mA

Capacitance

PARAMETER (Note 3)		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			15.0	pF

AC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ±10%, unless otherwise specified). See AC test circuit and switching time waveforms.

PARAMETER		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
t_C	$\overline{CE}$ Cycle Time	See AC Test Circuit and *Figure 1*. All Times (Except t_{OFF})	450			ns
t_P	$\overline{CE}$ Precharge Time		150			ns
t_{CE}	$\overline{CE}$ Pulse Width		300			ns
t_{AH}	Address Hold Time from $\overline{CE}$		50			ns
t_{AS}	Address to $\overline{CE}$ Setup Time		0			ns
t_{AC}	$\overline{CE}$ to Output Access Time				300	ns
t_{OFF}	Output Turn OFF Delay	Measured to 1.5V TRI-STATE Level with t_r and t_f of Input < 20 ns			150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Positive true logic notation is used: logical "1" = most positive voltage level, logical "0" = most negative voltage level.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: Typical values are for T_A = 25°C and nominal supply voltage.

Section 8

Character Generators

8

The Character Generators included in this section represent very cost effective solutions to problems arising in the design and implementation of CRT display subsystems. National's innovations in these devices in conjuction with the DP8350 series of CRT Controllers have assisted in the growth of this very important marketplace. Contact your local National representative for costs and other assistance.

Bipolar
Character Generators

National Semiconductor

DM8678 Bipolar Character Generator

General Description

The DM8678 is a 64-character bipolar character generator with serial output designed primarily for the CRT display marketplace, and packaged in a standard 16-pin DIP. The DM8678 incorporates several CRT system level functions, as well as a 7 x 9 or 5 x 7 row scan character font. The DM8678 performs the system functions of parallel to serial shifting, character address latching, character spacing and character line spacing. These system functions have required extra packages in the past.

Shifted characters can be generated by the on-chip subtractor.

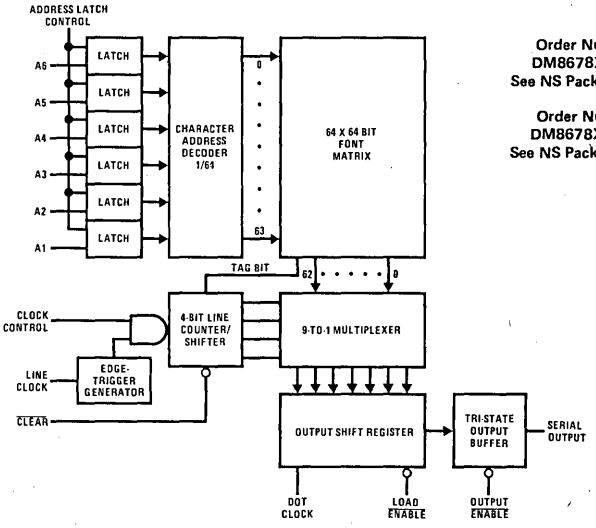
The $\overline{\text{clear}}$ input and the load $\overline{\text{enable}}$ input are active low. Load $\overline{\text{enable}}$ is synchronous with the dot clock. Both the line clock and the dot clock are positive edge-triggered. When the address latch control signal is high, the character addresses "fall through" the latch. And when the address latch control signal goes low, the character addresses are latched.

Features

- 64-character—row scan
- 5 x 7 or 7 x 9 font
- Shifted lower case descending characters
- Serial output
- 16-pin package
- 16 MHz min clock rate
- On-chip input latches
- On-chip shift register
- On-chip dot blanking
- On-chip row blanking
- TRI-STATE® output

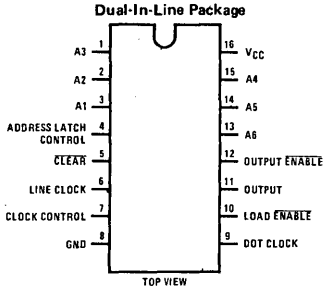
	ROW SCAN	7 x 9	5 x 7	FONT	PACKAGE
DM8678BWF	X	X		Upper Case Block Letters	N, J
DM8678CAE	X	X		Shifted Lower Case Block	N, J
DM8678CAB	X		X	Upper Case Block Letters	N, J
DM8678CAH	X		X	Shifted Lower Case Block	N, J
DM8678CAD	X	X		Kata Kana	N, J
DM8678BTK	X	X		Upper Case Script Letters	N, J
DM8678CAS	X	X		IBM 3741 Selectric	N, J

Block Diagram



Connection Diagram

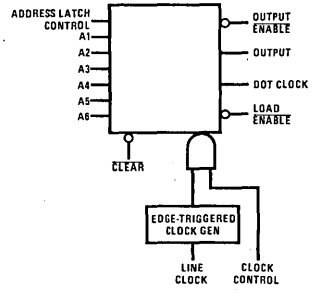
Dual-In-Line Package



Order Number DM8678XXX/J
See NS Package J16A

Order Number DM8678XXX/N
See NS Package N16A

Logic Symbol



Absolute Maximum Ratings

Supply Voltage	−0.5V to +7V
Input Voltage	−1.5V to +5.5V
Output Voltage	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

DC Electrical Characteristics (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−0.8	−1.6	mA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.4V			40	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45	V
V_{IL}	Low Level Input Voltage	V_{CC} = Min			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = Min	2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA		−0.8	−1.5	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		115	145	mA
	TRI-STATE PARAMETERS					
I_{SC}	Output Short-Circuit Current	V_O = 0V, V_{CC} = Max	−15		−50	mA
I_{HZ}	Output Leakage	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±40	μA
V_{OH}	Output Voltage High	I_{OH} = −2 mA	2.4	3.2		V

AC Electrical Characteristics (With standard load) (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Access Time					
T_{DO}	Dot Clock to Output			35	55	ns
T_{EA}	Output Enable			20	45	ns
T_{ER}	Output Disable			20	45	ns
	Set-Up Time					
T_{S1}	Load to Dot Clock		40	25		ns
T_{S2}	Address to Load		350	200		ns
T_{S3}	Clear to Load	See Switching Time Waveforms	350			ns
T_{S4}	Control to Line Clock		40			ns
T_{S5}	Line Clock to Load		950			ns
T_{S6}	Address to Address Latch		40			ns
	Hold Time					
T_{H1}	Load from Dot Clock		0			ns
T_{H2}	Address from Load		0			ns
T_{H3}	Control from Line Clock		100			ns
T_{H4}	Address from Address Latch		40			ns

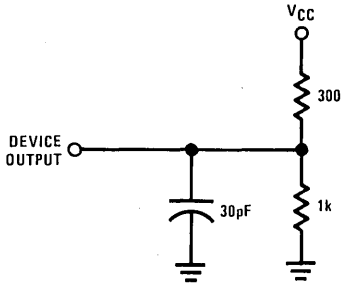
AC Electrical Characteristics (Continued) (With standard load) (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
	Minimum Pulse Width					
T_{W1}	Line Clock		40			ns
T_{W2}	Clear		40			ns
T_{W3}	Dot Clock	See Switching Time Waveforms	30			ns
T_{W4}	Load		40			ns
T_{W5}	Address Latch		40			ns
f_{MAX}	Maximum Clock Frequency		16	20		MHz

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

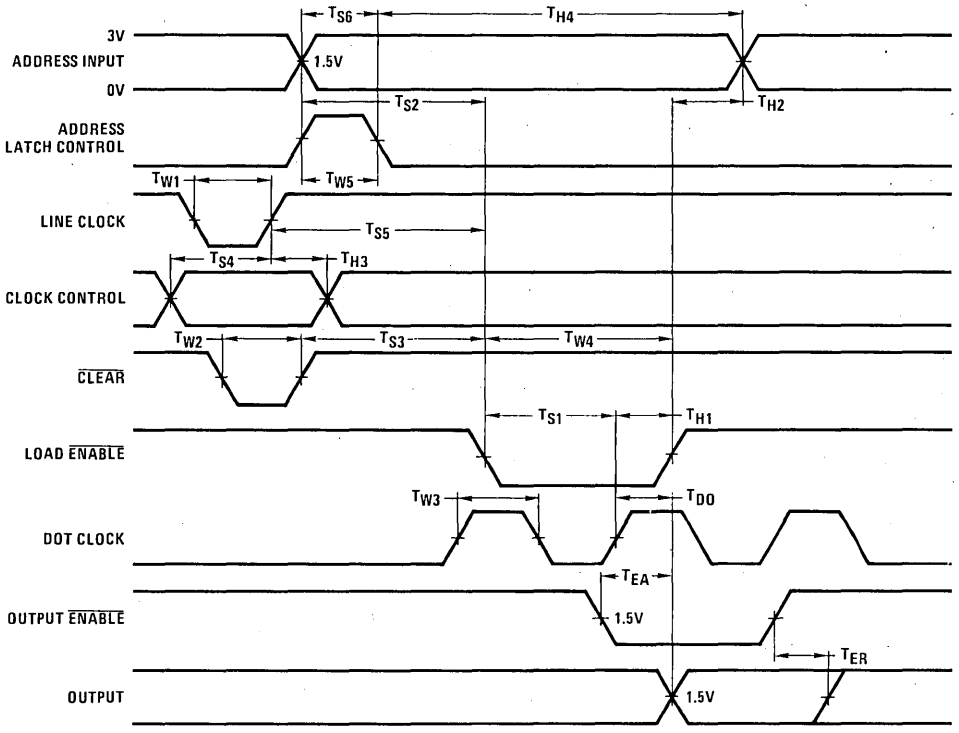
Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Standard Test Load



- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50 Ω, $t_r < 5$ ns and $t_f < 5$ ns (between 1.0V and 2.0V).
- T_{DO} is measured with output enable at a steady low level.

Switching Time Waveforms



Truth Tables

a) Address Latch

ADDRESS LATCH CONTROL	FUNCTION PERFORMED
0	Latched
1	Fall Through

b) Output

$\overline{\text{OUTPUT ENABLE}}$	STATE OF THE OUTPUT
1	Output Hi-Z
0	Data Out

c) 4-Bit Line Counter

CLOCK CONTROL	LINE CLOCK	$\overline{\text{CLEAR}}$	LINE COUNTER
H	⌐	H	Increment line counter
X	X	L	Asynchronous clear resets counter
L	X	H	Clock inhibited
H	¬	H	No change on high-to-low clock edge

X = Don't care

Definitions

A1–A6: Character address. A 6-bit code which selects 1 of the 64 characters in the font.

$\overline{\text{Clear}}$: Active low clear for mod 16 row counter, (can be used to truncate mod 16 counter).

Line Clock: Clock that advances the line counter. Advances counter on the low-to-high transition.

Clock Control: Enables line clock when high and disables line clock when low.

Load $\overline{\text{Enable}}$: Active low load command which routes data from the character ROM to the "D" inputs of the 7-bit shift register.

Dot Clock: A low-to-high transition of the dot clock loads the shift register if load $\overline{\text{enable}}$ is low or shifts data if load $\overline{\text{enable}}$ is high.

Output $\overline{\text{Enable}}$: An active low output enable. When high the output is in the Hi-Z state.

Output: A TTL TRI-STATE output buffer.

Functional Description

To select a character, a 6-bit binary word must be present at the address inputs A1–A6 when the address latch control is high. This address can be latched by bringing the address latch control signal low after a 40 ns set-up time. When the $\overline{\text{clear}}$ input receives a low pulse, the counter is reset to zero. The shift register can be loaded (T_{S2} ns) after the character is addressed. Data, representing one horizontal line of the addressed character, is available at the output when the load $\overline{\text{enable}}$ input is brought low. As shown in *Figure 1*, valid data arrives serially at the output. Dot clock pulses beyond that required to shift out one line of the character will add lows to the end of character. This provides a horizontal spacing between characters.

Figure 2 shows how the counter sequences through the rows of addressed lines with the application of clock pulses at the line clock input. Any additional line clocks beyond that required to display the character will put a vertical space between characters. This spacing can be truncated by bringing the $\overline{\text{clear}}$ input low. Detailed system application infomation is contained in application note AN-167 available from National.

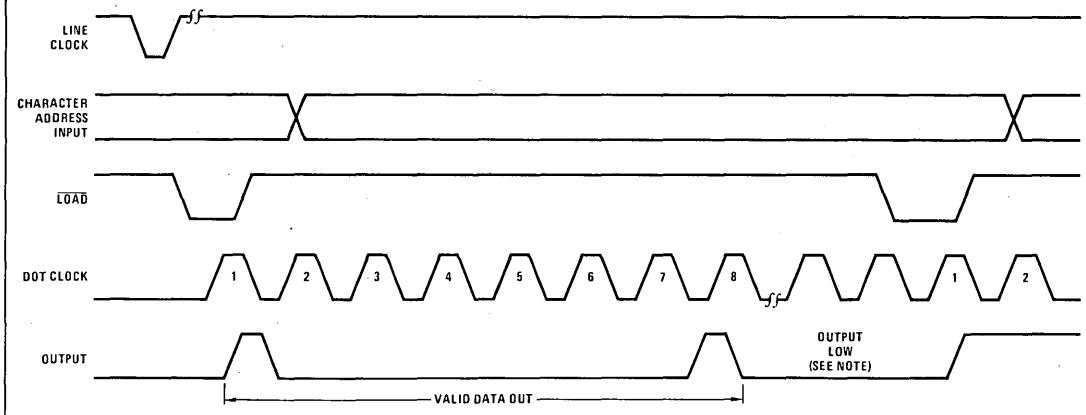
A two character display example is shown in *Figure 3* and a typical system timing waveform is shown in *Figure 4.*

A chip select input is provided for expansion of the character font. The various standard fonts are shown in *Figures 5, 6, 7, 8, 9 and 10.*

Functional Description (Continued)

Character Cycle – ROM data corresponding to one line of characters is loaded into the shift register T_{S2} after the ROM is addressed. When load $\overline{\text{enable}}$ goes low, ROM data is allowed to be present at the D input of the shift register via the MUX. The first bit of the ROM data is transferred to the output at the next low-to-high transition of the dot clock. After load $\overline{\text{enable}}$ goes back high, the second to seventh clock pulses shift out the rest of the selected row of the addressed character. Additional clock pulses will shift out low data used for spacing.

Line Cycle – The line counter is a mod 16 counter. A low-to-high transition of the line clock advances the line counter to the next count. If, for any reason, the counts need to be truncated, a low signal at the $\overline{\text{clear}}$ input resets the counter to zero. The clock control may be used as a line clock disable. A high signal at the line clock control terminal enables the counter and a low signal disables the line clock.



Note. Output goes and stays low following the leading edge of the eighth Dot-Clock pulse until Load $\overline{\text{enable}}$ is enabled again and new parallel data is loaded into the shift register.

FIGURE 1. Character Cycle

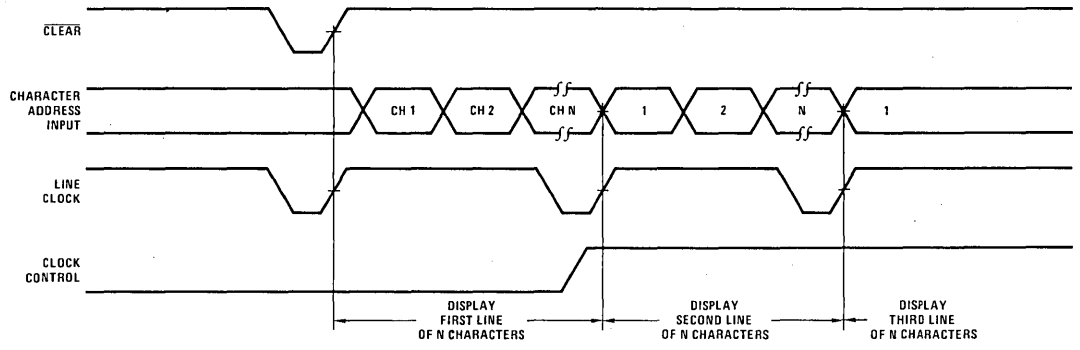


FIGURE 2. Line Cycle

Functional Description (Continued)

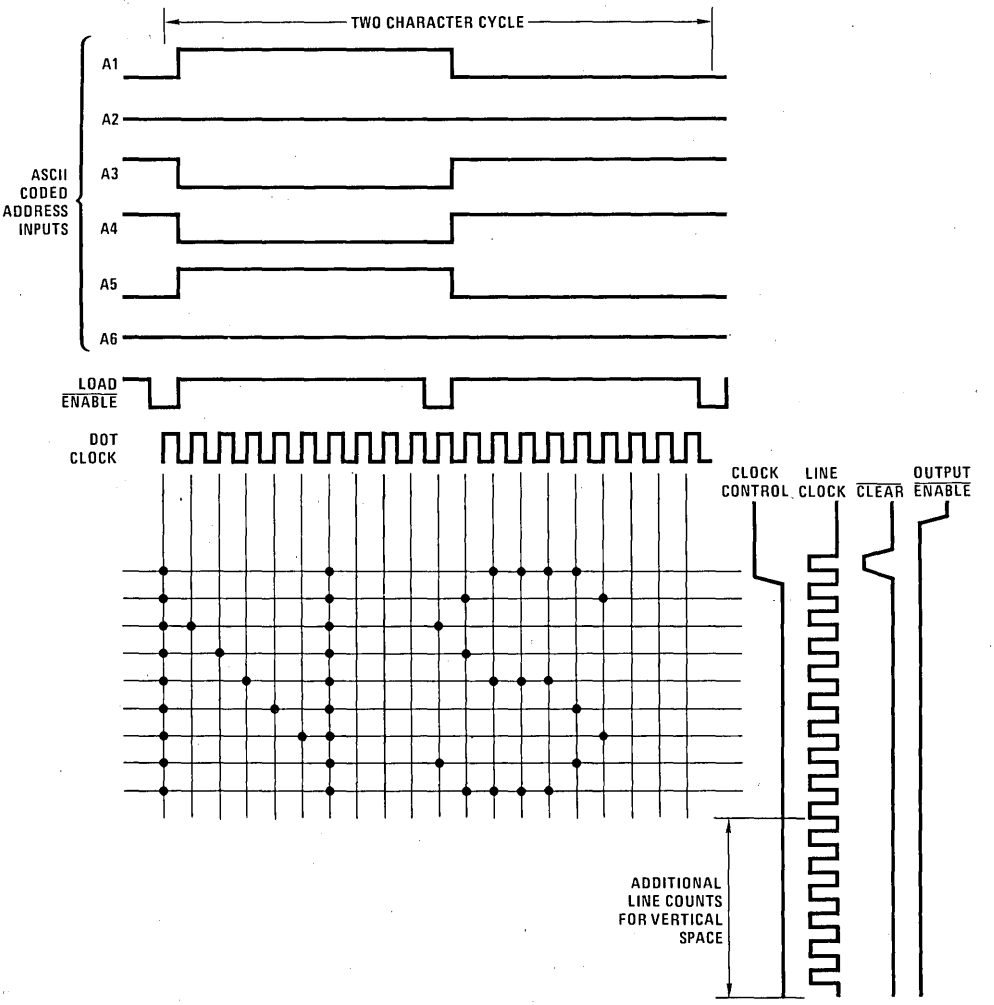
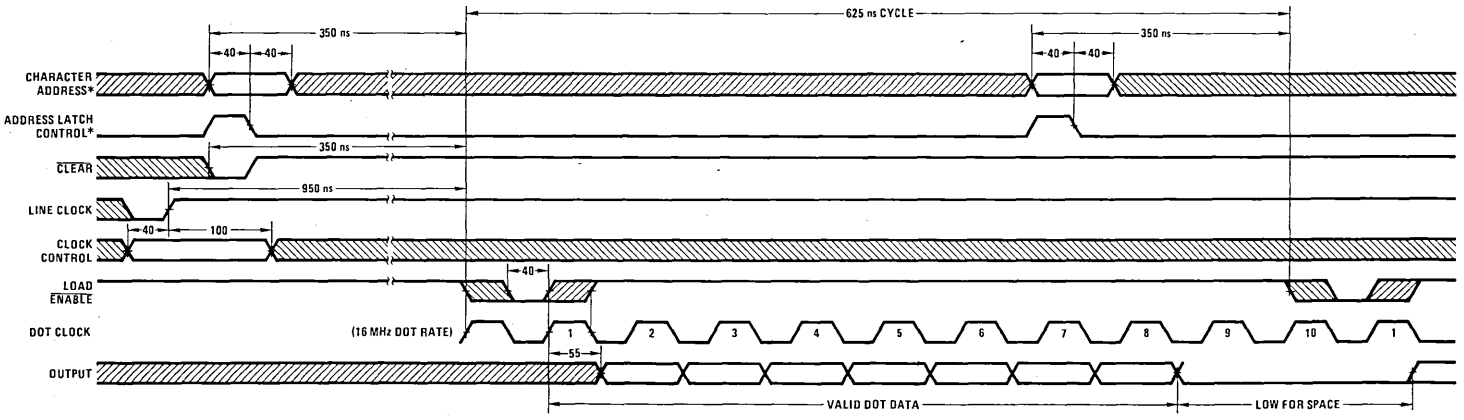


FIGURE 3. Example of Two Character Display Timing



*Shown here for operation with dynamic memory. For static memory operation the address latch control would be tied high and the character addresses would be stable between each address change occurring 350 ns before the high-to-low transition of Load enable.

FIGURE 4. Typical System Timing Waveform

Functional Description (Continued)

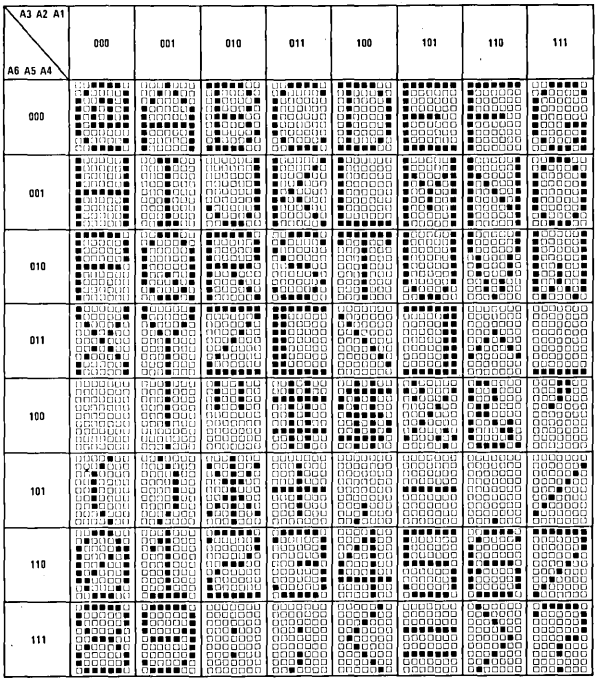
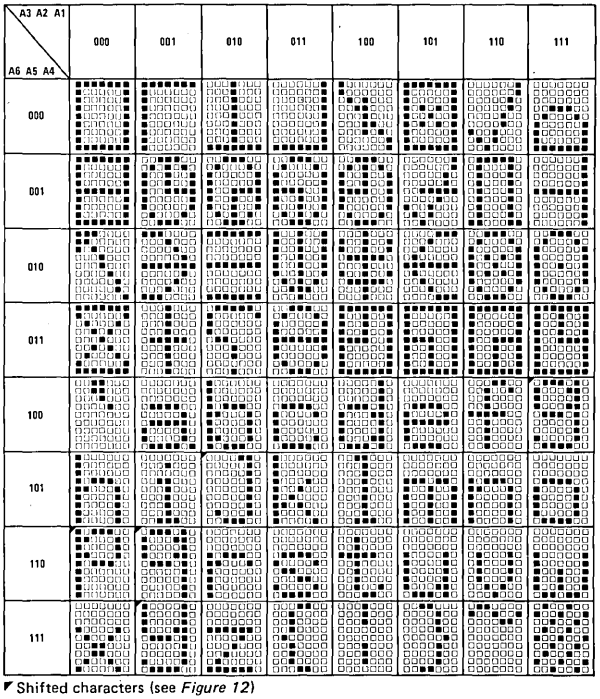


FIGURE 5. DM8678BWF



◤ Shifted characters (see *Figure 12*)

FIGURE 6. DM8678CAE

Note. A "filled in" dot represents a high memory output.

Functional Description (Continued)

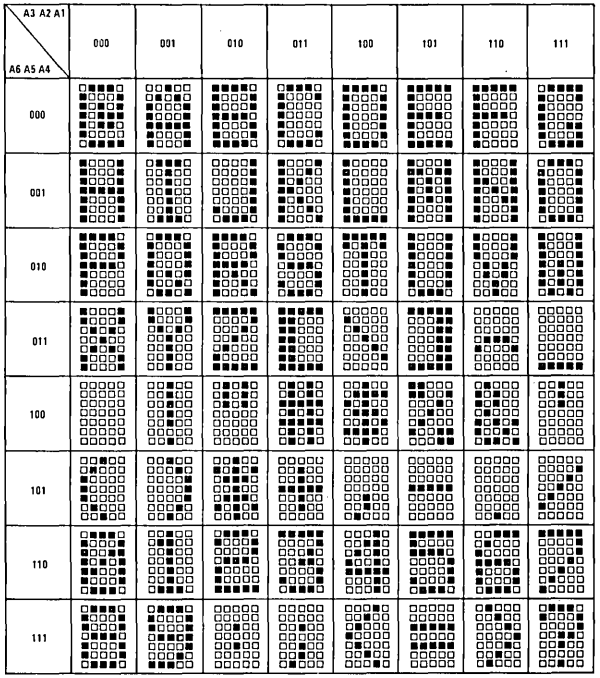
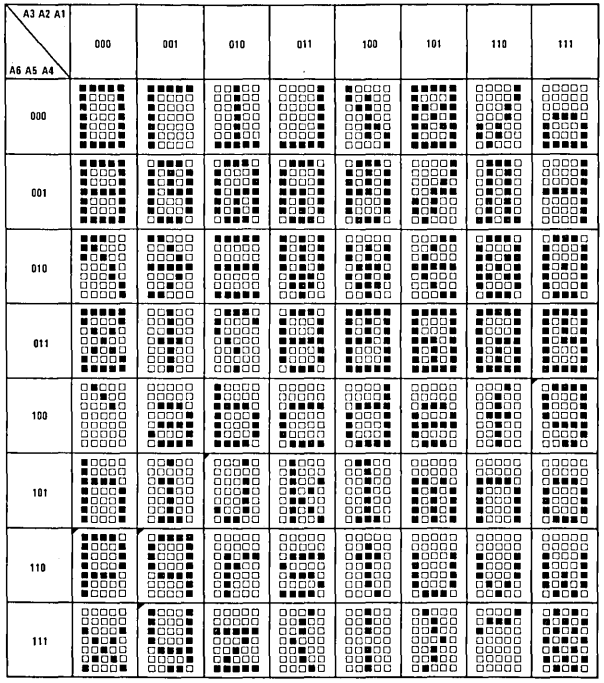


FIGURE 7. DM8767CAB



◤ Shifted characters (see *Figure 13*)

FIGURE 8. DM8678CAH

Functional Description (Continued)

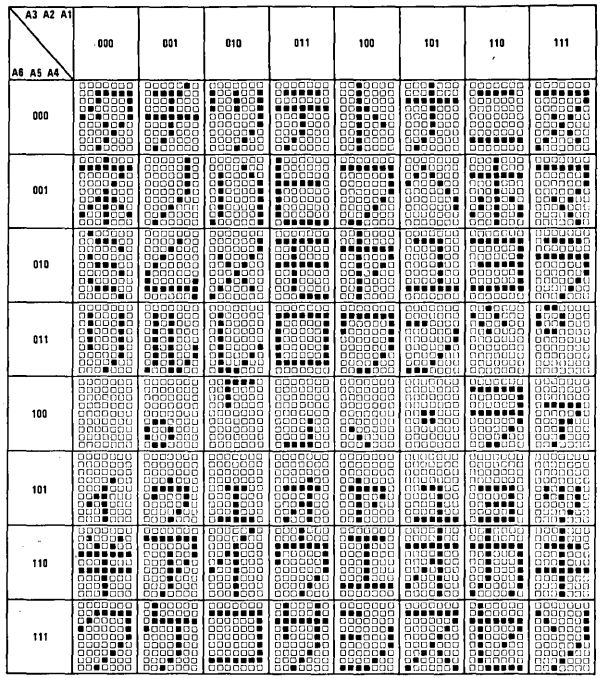


FIGURE 9. DM8678CAD

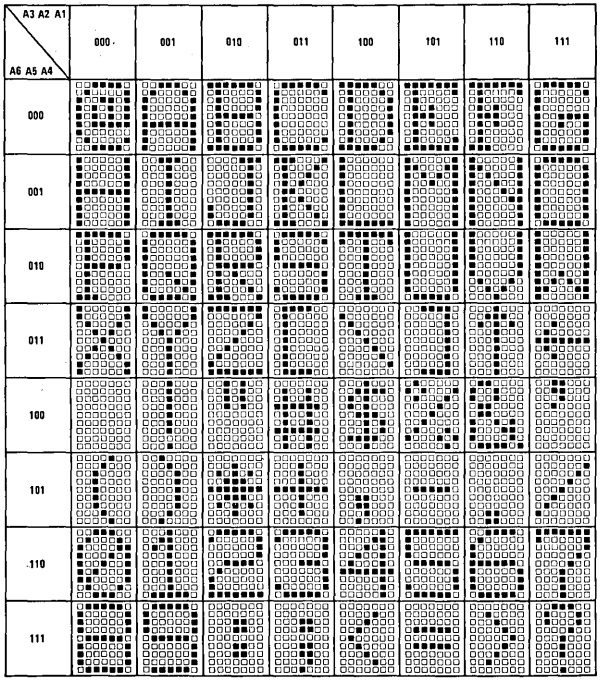


FIGURE 10. DM8678BTK

Functional Description (Continued)

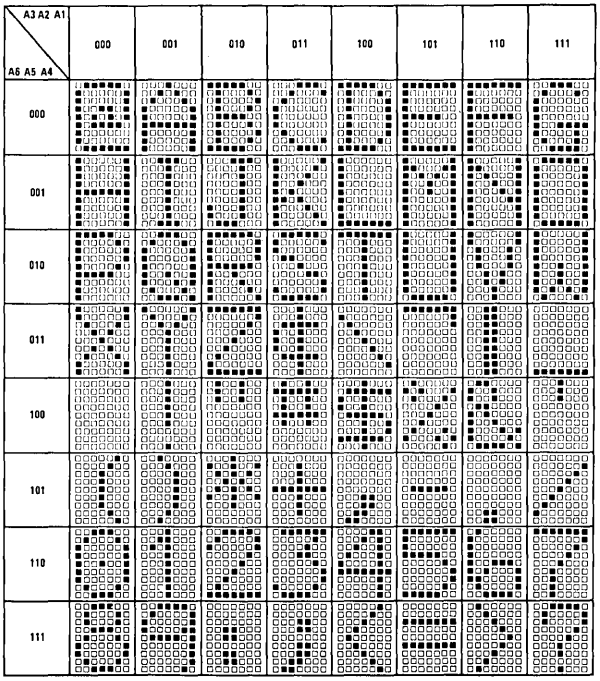
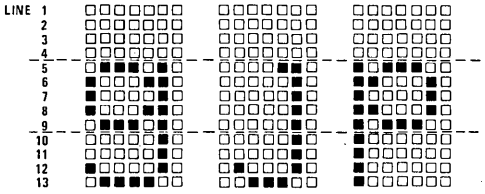


FIGURE 11. DM8678CAS



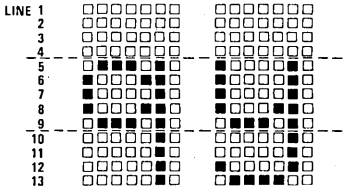
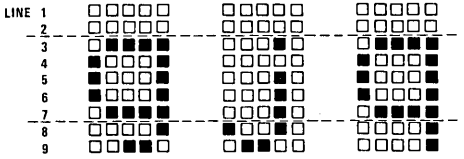


FIGURE 12. Shifted Characters for CAE



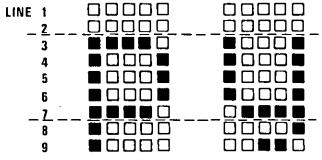


FIGURE 13. Shifted Characters for CAH

8

Ordering Information (For special character font for device DM8678).

CUSTOMER CARD INPUT FORMAT

Column 1–3
2-digit character address, from 0–63 preceded by a letter "C".

Column 4
Blank

Column 5–6
1-digit line address, from 0–8, preceded by a letter "L".

Column 7
Blank

Column 8–14
Row data which represents one horizontal row of dots at the specified line address and character address, with first dot at Column 8 and seventh dot at Column 14. Character for TTL high level is 1, for low level is 0.

Column 15
Blank

Column 16
Tag bit–0 for normal character and 1 for shifted character only.

Column 17
Blank

Column 18
Row SUM–Total number of "1's" presents in row data and tag bit expressed in decimal.

"TB" CARD FORMAT (total of eight cards)

Immediately following the data cards, there should be "TB" cards to indicate the column sum.

Column 1–2
The character "TB".

Column 3
1-digit corresponding to Dot number. Use number 8 for tag bit.

Column 4
Blank

Column 5–7
Column SUM–Total number of "1's" in column expressed in decimal.

Truth Table Input Format

CHARACTER ADDRESS	LINE ADDRESS	DOT DATA D1, D2, D3, D4, D5, D6, D7	TAG BIT	SUM
0	0			
0	1			
0	2			
0	3			
0	4			
0	5			
0	6			
0	7			
0	8			
1	0			
1	1			
1	2			
1	3			
1	4			
1	5			
1	6			
1	7			
1	8			
2	0			
2	1			
2	2			
2	3			
2	4			
2	5			
2	6			
2	7			
2	8			
.	.			
.	.			
.	.			
.	.			
TB				

National Semiconductor

DM76S64/DM86S64 Bipolar Character Generator

General Description

The DM76S64/DM86S64 is a 64-character bipolar character generator with serial output designed primarily for the CRT display marketplace, and packaged in a standard 16-pin DIP. The DM76S64/DM86S64 incorporates several CRT system level functions, as well as a 7 x 9 or 5 x 7 row scan character font. The DM76S64/DM86S64 performs the system functions of parallel to serial shifting, character address latching, character spacing and character line spacing. These system functions have required extra packages in the past.

Shifted characters can be generated by the on-chip subtractor.

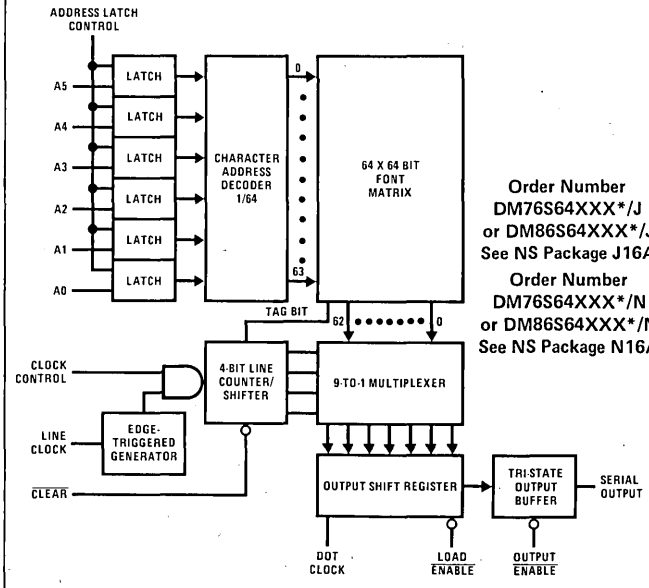
The $\overline{\text{clear}}$ input and the load $\overline{\text{enable}}$ input are active low. Load $\overline{\text{enable}}$ is synchronous with the dot clock. Both the line clock and the dot clock are positive edge-triggered. When the address latch control signal is high, the character addresses "fall through" the latch. And when the address latch control signal goes low, the character addresses are latched.

Features

- 64-character—row scan
- 5 x 7 or 7 x 9 font
- Custom fonts available with shift options
- Serial output
- 16-pin package
- 35 MHz typ clock rate
- On-chip input latches
- On-chip shift register
- On-chip dot blanking
- On-chip row blanking
- TRI-STATE® output

	7 x 9	5 x 7	FONT	PACKAGE
DM76S64BWF/DM86S64BWF	X		Upper Case Block Letters	N, J
DM76S64CAE/DM86S64CAE	X		Shifted Lower Case Block	N, J
DM76S64CAB/DM86S64CAB		X	Upper Case Block Letters	N, J
DM76S64CAH/DM86S64CAH		X	Shifted Lower Case Block	N, J
DM76S64ACS/DM86S64ACS	X		ASCII Character Set	N, J
DM76S64ANC/DM86S64ANC	X		ASCII Numerals and Control	N, J

Block Diagram

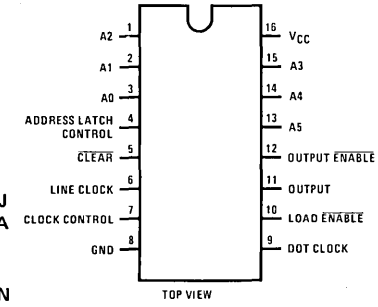


Order Number DM76S64XXX*/J or DM86S64XXX*/J
See NS Package J16A

Order Number DM76S64XXX*/N or DM86S64XXX*/N
See NS Package N16A

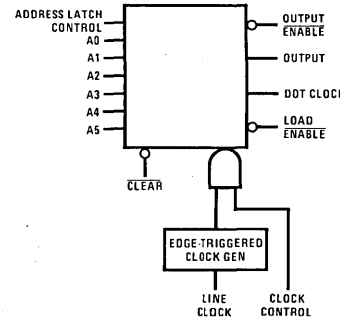
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Symbol



* alpha pattern designators

Absolute Maximum Ratings (Note 1)

Supply Voltage	−0.5V to +7V
Input Voltage	−1.5V to +5.5V
Output Voltage	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM76S64	4.5	5.5	V
DM86S64	4.75	5.25	V
Ambient Temperature (T_A)			
DM76S64	−55	+125	°C
DM86S64	0	+70	°C
Logical "0" Voltage	0	0.8	V
Logical "1" Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 2)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V			−800	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.4V			40	μA
I_I	Input Leakage Current	V_{CC} = Max, V_{IN} = 5.5V			1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45	V
V_{IL}	Low Level Input Voltage	V_{CC} = Min			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = Min	2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA		−0.8	−1.5	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, Output Open		80	140	mA
TRI-STATE PARAMETERS						
I_{SC}	Output Short-Circuit Current	V_O = 0V, V_{CC} = Max	−15		−70	mA
I_{HZ}	Output Leakage	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±40	μA
V_{OH}	Output Voltage High	I_{OH} = −2 mA	2.4	3.2		V

AC Electrical Characteristics (Note 2)

	PARAMETER	CONDITIONS	DM76S64			DM86S64			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Access Time								
T_{DO}	Dot Clock to Output			25	50		25	40	ns
T_{EA}	Output Enable			10	35		10	30	ns
T_{ER}	Output Disable			13	35		13	30	ns
	Set-Up Time								
T_{S1}	Load to Dot Clock		25	7		20	7		ns
T_{S2}	Address to Load	See	335	54		280	54		ns
T_{S3}	Clear to Load	Switching	335	14		280	14		ns
T_{S4}	Control to Line Clock	Time	50	−10		40	−10		ns
T_{S5}	Line Clock to Load	Waveforms	1140	156		950	156		ns
T_{S6}	Address to Address Latch		50	6		40	6		ns
	Hold Time								
T_{H1}	Load from Dot Clock		5	−6		0	−6		ns
T_{H2}	Address from Load		0	−14		0	−14		ns
T_{H3}	Control from Line Clock		120	23		100	23		ns
T_{H4}	Address from Address Latch		50	3		40	3		ns

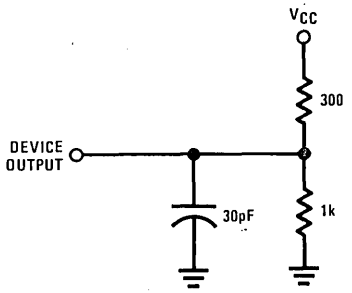
AC Electrical Characteristics (Continued) (Note 2)

PARAMETER		CONDITIONS	DM76S64			DM86S64			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Pulse Width								
T_{W1}	Line Clock		50	12		40	12		ns
T_{W2}	Clear		50	6		40	6		ns
T_{W3}	Dot Clock		25	12		20	12		ns
T_{W4}	Load		40	8		30	8		ns
T_{W5}	Address Latch		50	22		40	22		ns
f_{MAX}	Clock Frequency		18	35		22	35		MHz

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

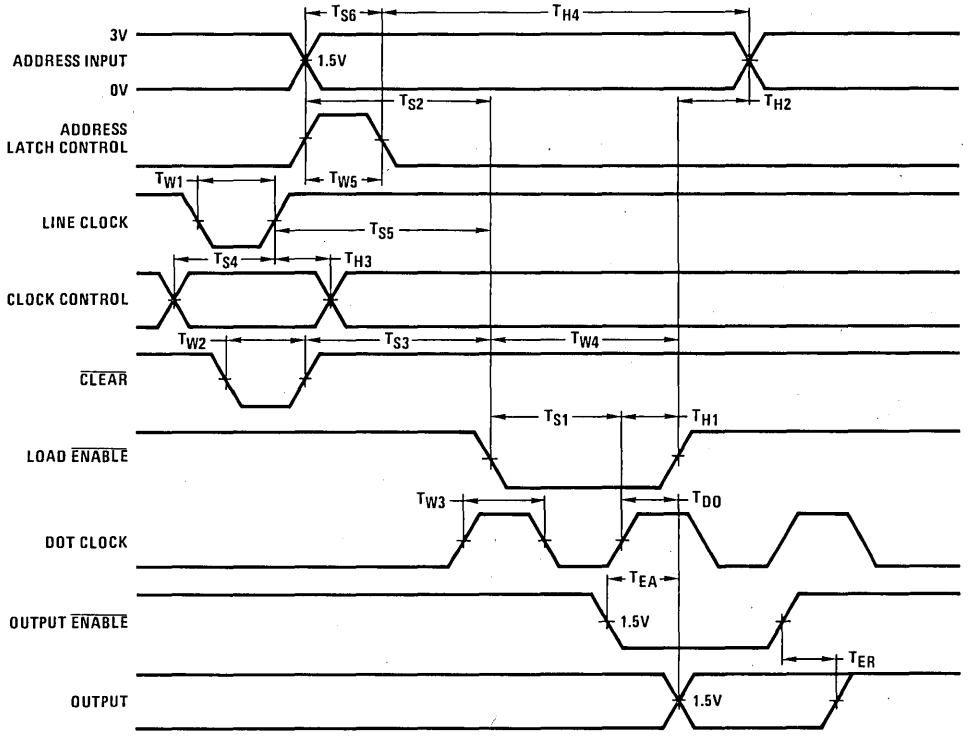
Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Standard Test Load



- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50 Ω, $t_r < 5$ ns and $t_f < 5$ ns (between 1.0V and 2.0V).
- T_{DO} is measured with output enable at a steady low level.

Switching Time Waveforms



Truth Tables

A) ADDRESS LATCH

ADDRESS LATCH CONTROL	FUNCTION PERFORMED
0	Latched
1	Fall Through

B) OUTPUT

OUTPUT $\overline{\text{ENABLE}}$	STATE OF THE OUTPUT
1	Output Hi-Z
0	Data Out

C) 4-BIT LINE COUNTER

CLOCK CONTROL	LINE CLOCK	$\overline{\text{CLEAR}}$	LINE COUNTER
H	⌐	H	Increment line counter
X	X	L	Asynchronous clear resets counter
L	X	H	Clock inhibited
H	⌐	H	No change on high-to-low clock edge

X = Don't care

Definitions

A0–A5: Character address. A 6-bit code which selects 1 of the 64 characters in the font.

$\overline{\text{Clear}}$: Active low clear for mod 16 row counter, (can be used to truncate mod 16 counter).

Line Clock: Clock that advances the line counter. Advances counter on the low-to-high transition.

Clock Control: Enables line clock when high and disables line clock when low.

Load $\overline{\text{Enable}}$: Active low load command which routes data from the character ROM to the "D" inputs of the 7-bit shift register.

Dot Clock: A low-to-high transition of the dot clock loads the shift register if load $\overline{\text{enable}}$ is low or shifts data if load $\overline{\text{enable}}$ is high.

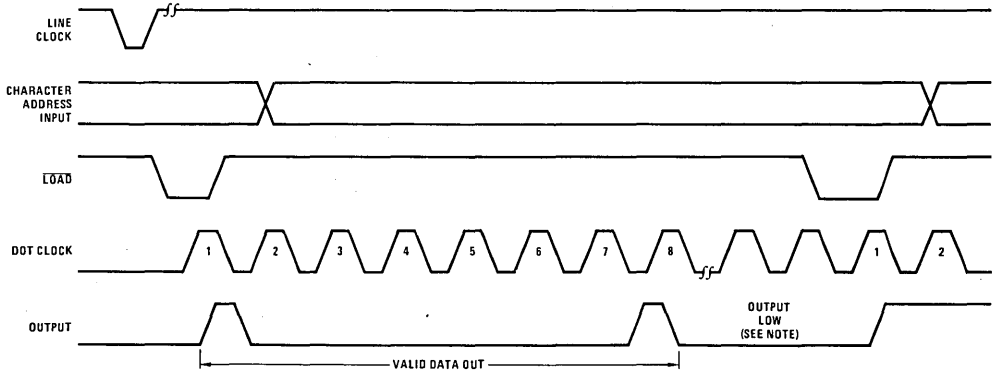
Output $\overline{\text{Enable}}$: An active low output enable. When high the output is in the Hi-Z state.

Output: A TTL TRI-STATE output buffer.

Functional Description

To select a character, a 6-bit binary word must be present at the address inputs A0–A5 when the address latch control is high. This address can be latched by bringing the address latch control signal low after a 40 ns set-up time. When the clear input receives a low pulse, the counter is reset to zero. The shift register can be loaded (T_{S2} ns) after the character is addressed. Data, representing 1 horizontal line of the addressed character, is available at the output when the load enable input is brought low. As shown in *Figure 1*, valid data arrives serially at the output. Dot clock pulses beyond that required to shift out 1 line of the character will add lows to the end of character. This provides a horizontal spacing between characters.

Figure 2 shows how the counter sequences through the rows of addressed lines with the application of clock pulses at the line clock input. Any additional line clocks beyond that required to display the character will put a vertical space between characters. This spacing can be truncated by bringing the $\overline{\text{clear}}$ input low. Detailed system application infomation is contained in application note AN-167 available from National.



Note. Output goes and stays low following the leading edge of the eighth Dot-Clock pulse until Load $\overline{\text{enable}}$ is enabled again and new parallel data is loaded into the shift register.

FIGURE 1. Character Cycle.

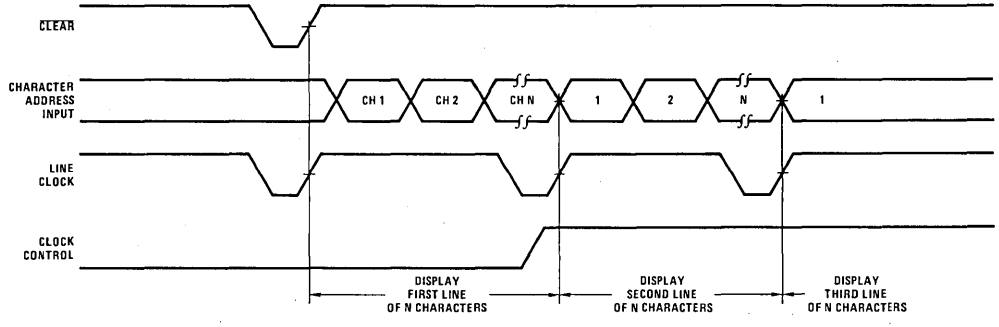


FIGURE 2. Line Cycle

Functional Description (Continued)

A two character display example is shown in *Figure 3* and a typical system timing waveform is shown in *Figure 4.*

A chip select input is provided for expansion of the character font. The various standard fonts are shown in *Figures 5, 6, 7, 8, 9 and 10.* Descending characters in the 5 x 7 fonts are shifted by virtue of their placement in the matrix. Descending characters in the 7 x 9 fonts are shifted (by the on-chip line shifter/counter) the number of lines indicated by the number in the upper left hand corner of the character drawings in the figures.

Character Cycle – ROM data corresponding to 1 line of characters is loaded into the shift register T_{S2} after the ROM is addressed. When load $\overline{\text{enable}}$ goes low, ROM data is allowed to be present at the D input of the shift register via the MUX. The first bit of the ROM data is transferred to the output at the next low-to-high transition of the dot clock. After load $\overline{\text{enable}}$ goes back high, the second to seventh clock pulses shift out the rest of the selected row of the addressed character. Additional clock pulses will shift out low data used for spacing.

Line Cycle – The line counter is a mod 16 counter. A low-to-high transition of the line clock advances the line counter to the next count. If, for any reason, the counts need to be truncated, a low signal at the $\overline{\text{clear}}$ input resets the counter to zero. The clock control may be used as a line clock disable. A high signal at the line clock control terminal enables the counter and a low signal disables the line clock.

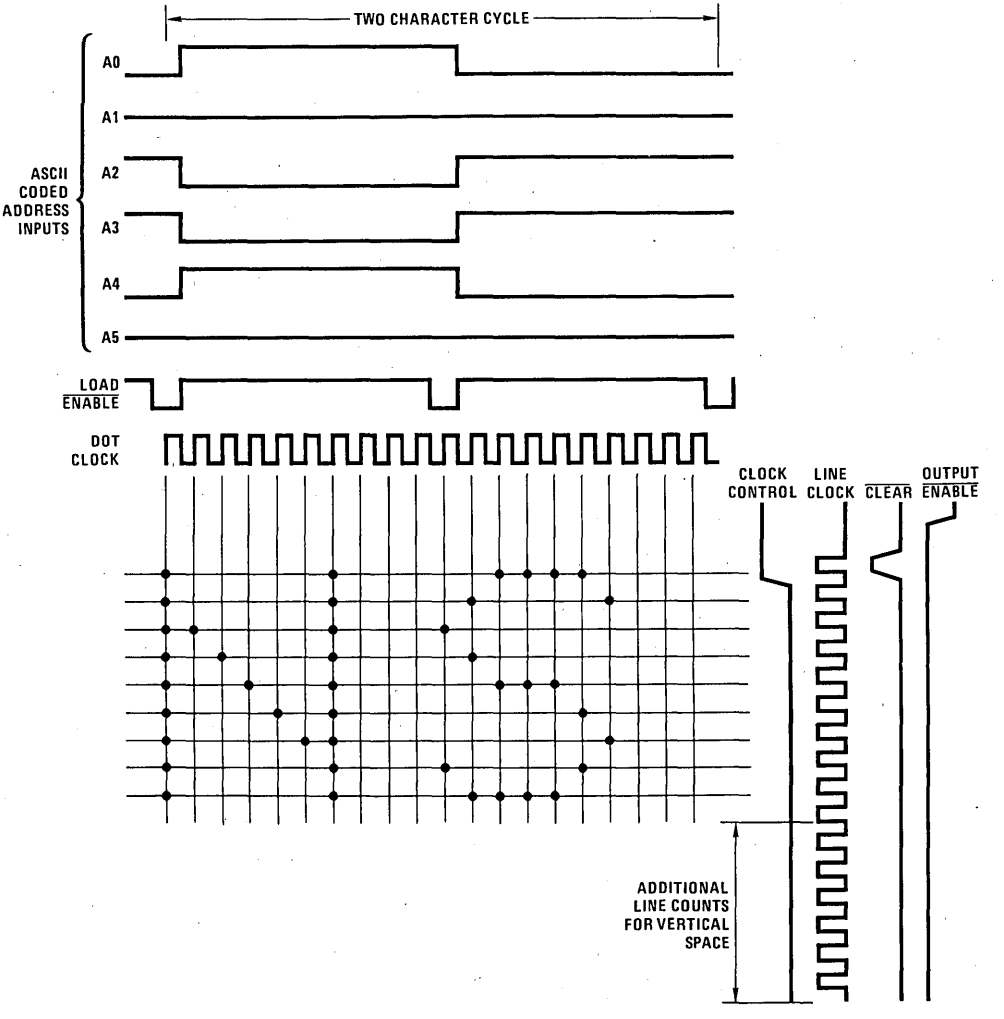
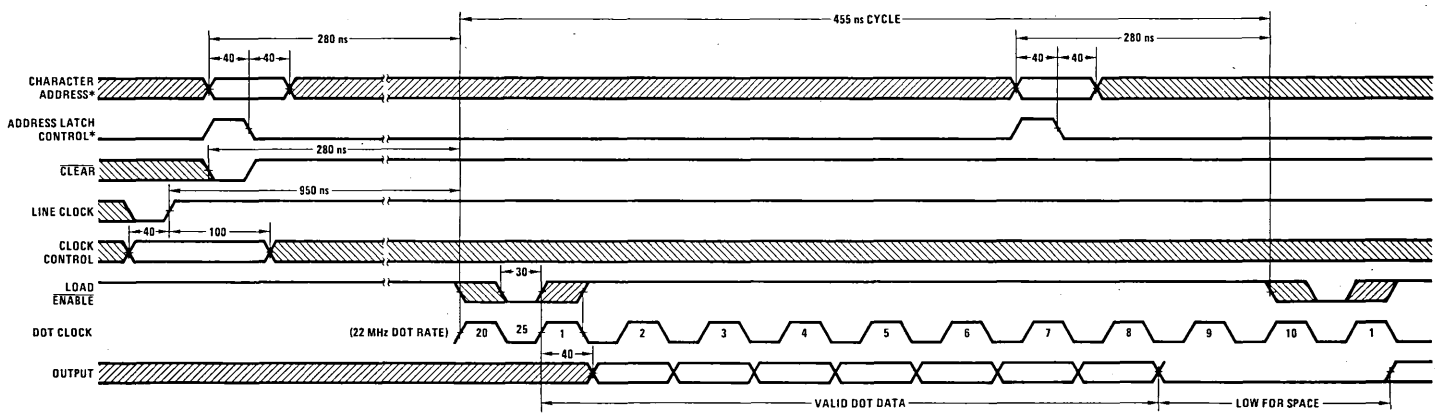


FIGURE 3. Example of Two Characters Display Timing



*Shown here for operation with dynamic memory. For static memory operation the address latch control would be tied high and the character addresses would be stable between each address change occurring 280 ns before the high-to-low transition of Load enable.

FIGURE 4. Typical System Timing Waveform

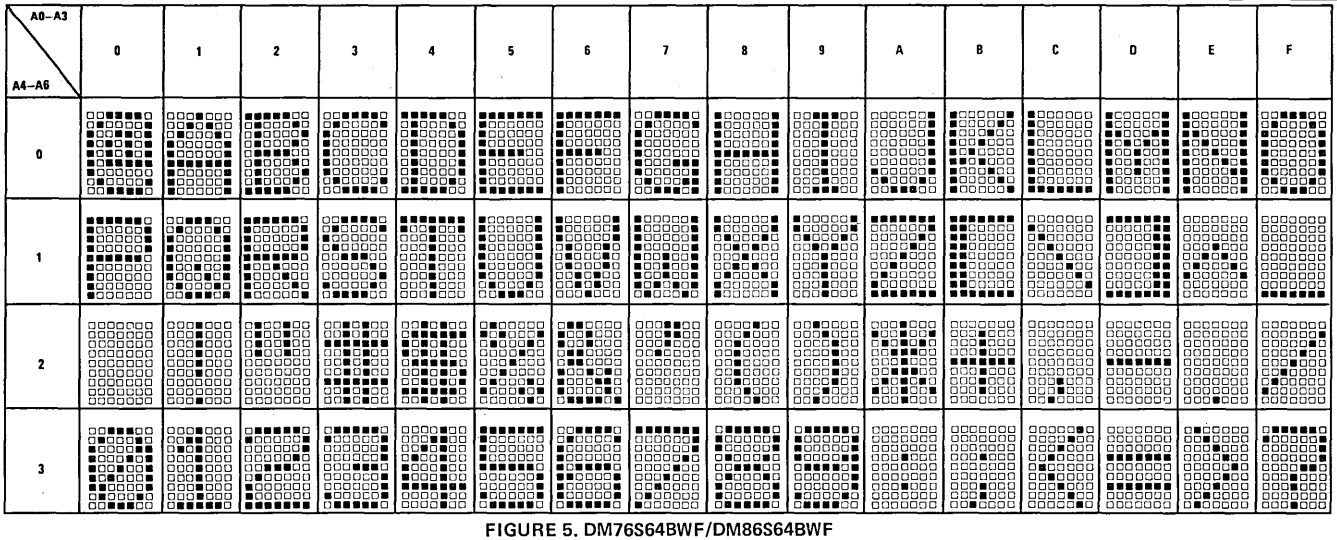


FIGURE 5. DM76S64BWF/DM86S64BWF

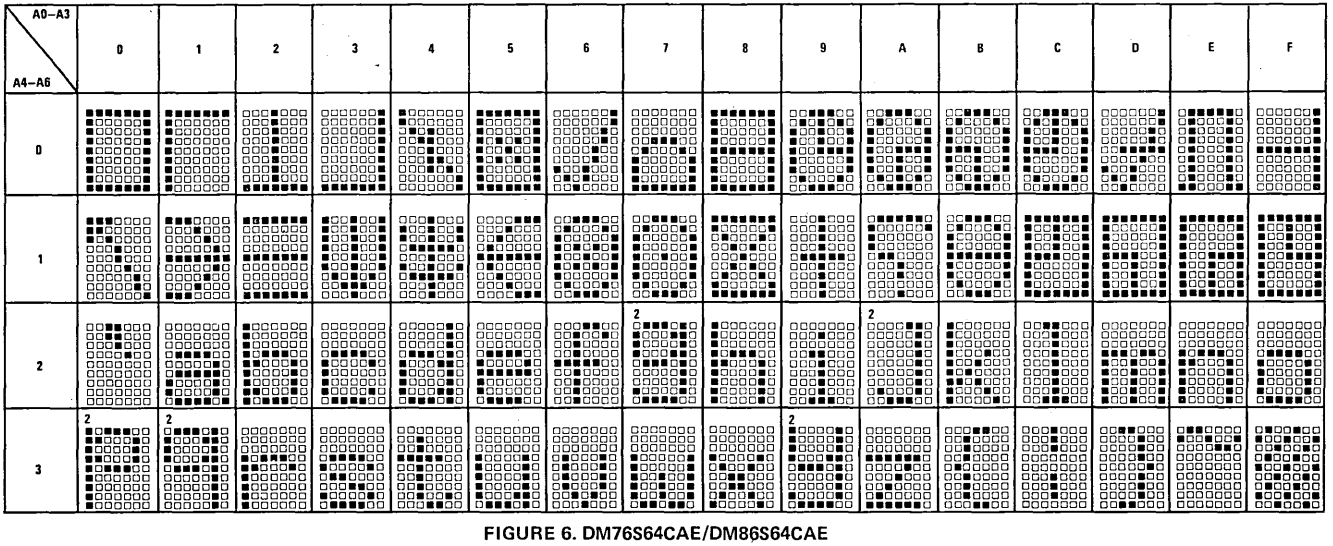


FIGURE 6. DM76S64CAE/DM86S64CAE

Functional Description (Continued)

FIGURE 7. DM76S64CAB/DM86S64CAB

FIGURE 8. DM76S64CAH/DM86S64CAH

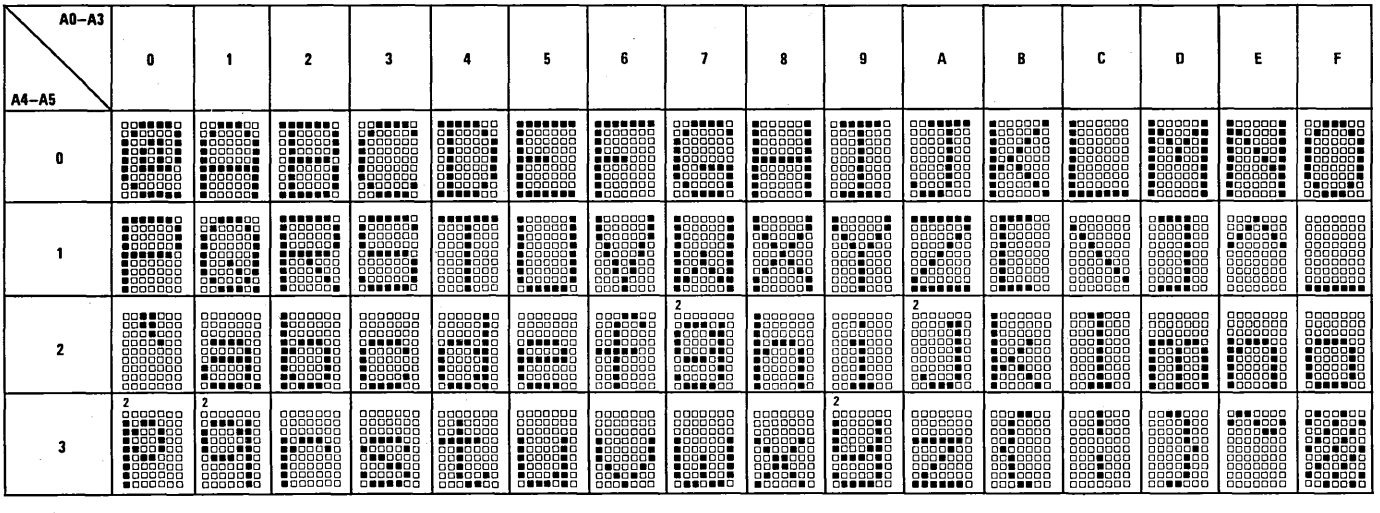


FIGURE 9. DM76S64ACS/DM86S64ACS

Functional Description (Continued)

FIGURE 10. DM76S64ANC/DM86S64ANC

National Semiconductor

Character Generators
ADVANCE INFORMATION

DM76S128/DM86S128 Bipolar Character Generator

General Description

The DM76S128/DM86S128 is a 128-character bipolar character generator with serial output designed primarily for the CRT display marketplace, and packaged in a standard 16-pin DIP. The DM76S128/DM86S128 incorporates several CRT system level functions, as well as a 7 x 9 or 5 x 7 row scan character font. The DM76S128/DM86S128 performs the system functions of parallel to serial shifting, character address latching, character spacing and character line spacing. These system functions have required extra packages in the past.

Shifted characters can be generated by the on-chip adder/subtracter.

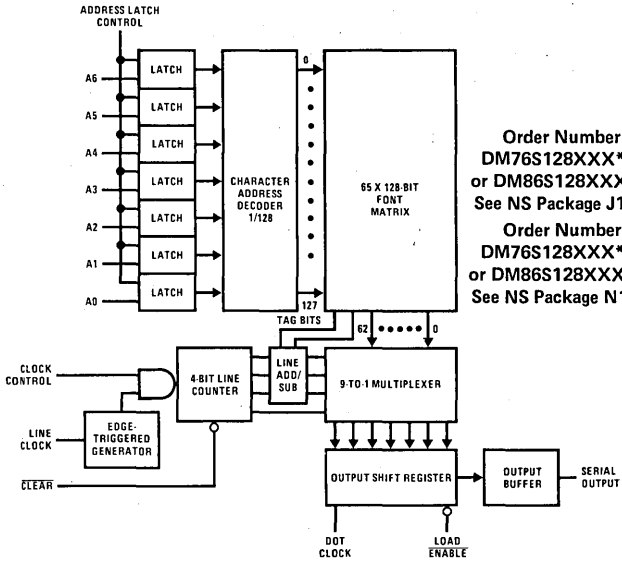
The $\overline{\text{clear}}$ input and the load $\overline{\text{enable}}$ input are active low. Load $\overline{\text{enable}}$ is synchronous with the dot clock. Both the line clock and the dot clock are positive edge-triggered. When the address latch control signal is high, the character addresses "fall through" the latch. And when the address latch control signal goes low, the character addresses are latched.

Features

- 128 character—row scan
- 5 x 7 or 7 x 9 font
- Custom fonts available with shift options
- Serial output
- 16-pin package
- 35 MHz typical clock rate
- On-chip input latches
- On-chip shift register
- On-chip dot blanking
- On-chip row blanking
- Low power—400 mW typical

	7 x 9	5 x 7	FONT	PACKAGE
DM76S128CNC/DM86S128CNC	X		Upper and Shifted Lower Case Block	N, J
DM76S128CND/DM86S128CND		X	Upper and Lower Case Block	N, J
DM76S128CQH/DM86S128CQH	X		ASCII CHARACTER SET	N, J
DM76S128CQJ/DM86S128CQJ		X	ASCII CHARACTER SET	N, J

Block Diagram



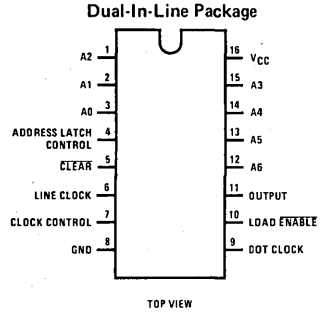
*alpha pattern designators

Order Number
DM76S128XXX*/J
or DM86S128XXX*/J
See NS Package J16A

Order Number
DM76S128XXX*/N
or DM86S128XXX*/N
See NS Package N16A

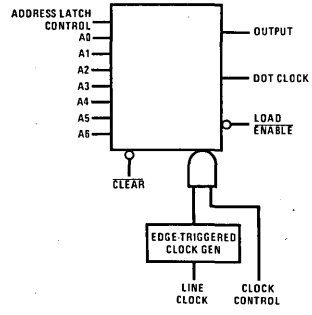
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Symbol



Absolute Maximum Ratings (Note 1)

Supply Voltage	−0.5V to +7V
Input Voltage	−1.5V to +5.5V
Output Voltage	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM76S128	4.5	5.5	V
DM86S128	4.75	5.25	V
Ambient Temperature (T_A)			
DM76S128	−55	+125	°C
DM86S128	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

DC Electrical Characteristics (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V			−800	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.4V			40	μA
I_I	Input Leakage Current	V_{CC} = Max, V_{IN} = 5.5V			1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45	V
V_{OH}	Output Voltage High	I_{OH} = −2 mA	2.4	3.2		V
V_{IL}	Low Level Input Voltage	V_{CC} = Min			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = Min	2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA		−0.8	−1.5	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, Output Open		100	140	mA
I_{SC}	Output Short-Circuit Current	V_O = 0V, V_{CC} = Max	−15		−70	mA

AC Electrical Characteristics

DM76S128: T_A = −55°C to +125°C, V_{CC} = 4.5V to 5.5V. C_L = 50 pF.
DM86S128: T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V. C_L = 50 pF.

PARAMETER		DM76S128			DM86S128			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
	Access Time							
T_{DO}	Dot Clock to Output		25	50		25	40	ns
	Set Up Time							
T_{S1}	Load to Dot Clock	25	7		20	7		ns
T_{S2}	Address to Load	335	54		280	54		ns
T_{S3}	Clear to Load	335	14		280	14		ns
T_{S4}	Control to Line Clock	50	−10		40	−10		ns
T_{S5}	Line Clock to Load	1140	156		950	156		ns
T_{S6}	Address to Address Latch	50	6		40	6		ns
	Hold Time							
T_{H1}	Load from Dot Clock	5	−6		0	−6		ns
T_{H2}	Address from Load	0	−14		0	−14		ns
T_{H3}	Control from Line Clock	120	23		100	23		ns
T_{H4}	Address from Address Latch	50	3		40	3		ns
	Pulse Width							

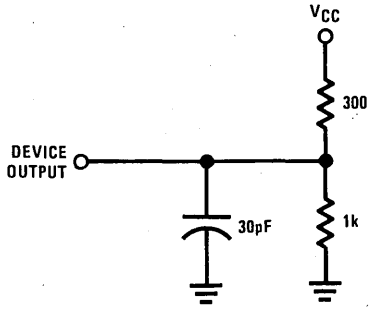
AC Electrical Characteristics (Continued) (With standard load) (Note 2)

PARAMETER		DM76S128			DM86S128			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
T_{W1}	Line Clock	50	12		40	12		ns
T_{W2}	Clear	50	6		40	6		ns
T_{W3}	Dot Clock	25	12		20	12		ns
T_{W4}	Load	40	8		30	8		ns
T_{W5}	Address Latch	50	22		40	22		ns
f_{MAX}	Clock Frequency	18	35		22	35		MHz

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Standard Test Load



- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50 Ω, $t_r < 5$ ns and $t_f < 5$ ns (between 1.0V and 2.0V).

Truth Tables

A) ADDRESS LATCH

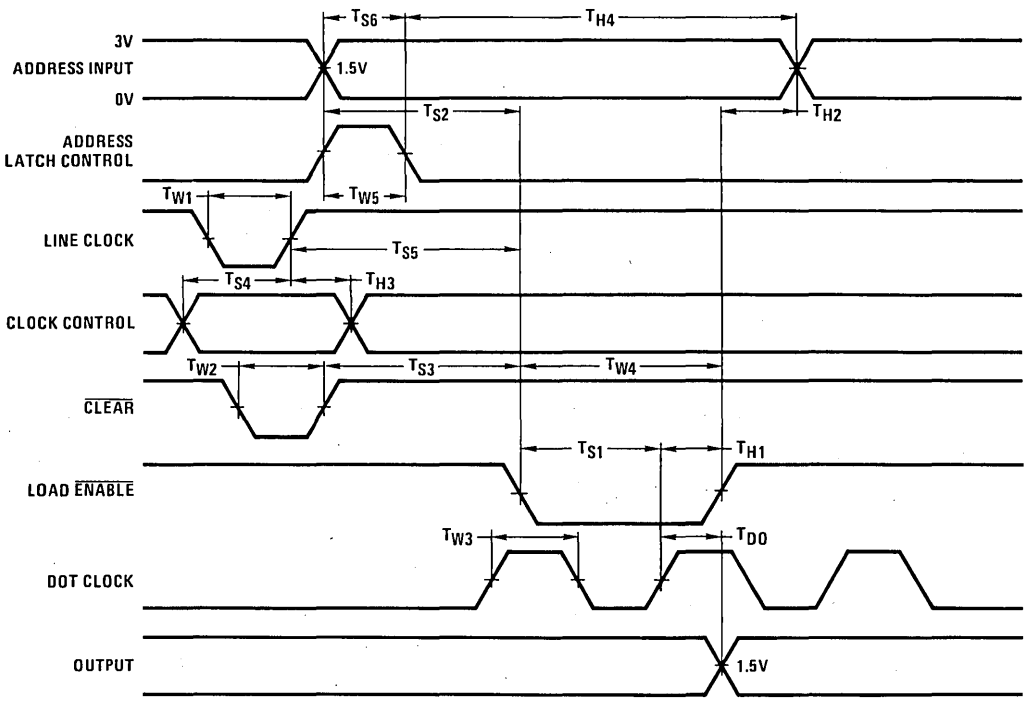
ADDRESS LATCH CONTROL	FUNCTION PERFORMED
0	Latched
1	Fall Through

B) 4-BIT LINE COUNTER

CLOCK CONTROL	LINE CLOCK	$\overline{\text{CLEAR}}$	LINE COUNTER
H	⌐	H	Increment line counter
X	X	L	Asynchronous clear resets counter
L	X	H	Clock inhibited
H	⌐	H	No change on high-to-low clock edge

X = Don't care

Switching Time Waveforms



Definitions

A0–A6: Character address. A 7-bit code which selects 1 of the 128 characters in the font.

Clear: Active low clear for mod 16 row counter, (can be used to truncate mod 16 counter).

Line Clock: Clock that advances the line counter. Advances counter on the low-to-high transition.

Clock Control: Enables line clock when high and disables line clock when low.

Load Enable: Active low load command which routes data from the character ROM to the "D" inputs of the 7-bit shift register.

Dot Clock: A low-to-high transition of the dot clock loads the shift register if load enable is low or shifts data if load enable is high.

Output: A TTL BI-STATE output buffer.

Functional Description

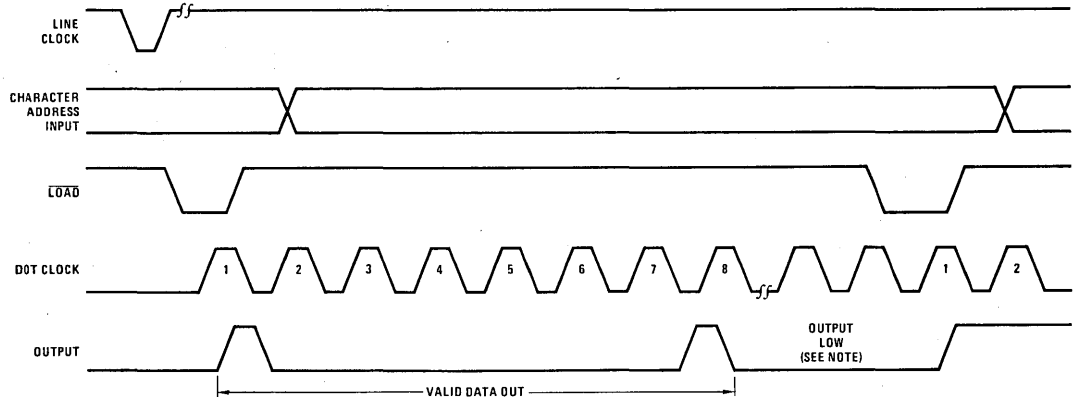
To select a character, a 7-bit binary word must be present at the address inputs A0–A6 when the address latch control is high. This address can be latched by bringing the address latch control signal low after a 40 ns set-up time. When the $\overline{\text{clear}}$ input receives a low pulse, the counter is reset to zero. The shift register can be loaded (T_{S2} ns) after the character is addressed. Data, representing one horizontal line of the addressed character, is available at the output when the load $\overline{\text{enable}}$ input is brought low. As shown in *Figure 1*, valid data arrives serially at the output. Dot clock pulses beyond that required to shift out one line of the character will add lows to the end of character. This provides a horizontal spacing between characters.

Figure 2 shows how the counter sequences through the rows of addressed lines with the application of clock pulses at the line clock input. Any additional line clocks beyond that required to display the character will put a vertical space between characters. This spacing can be truncated by bringing the $\overline{\text{clear}}$ input low.

A two character display example is shown in *Figure 3* and a typical system timing waveform is shown in *Figure 4*. The standard fonts are shown in *Figures 5, 6, 7 and 8*. Descending characters in the 5 x 7 fonts are shifted by virtue of their placement in the matrix. Descending characters in the 7 x 9 fonts are shifted (by th on-chip line shifter/counter) the number of lines indicated by the number in the upper left hand corner of the character drawings in the figures.

Character Cycle – ROM data corresponding to one line of characters is loaded into the shift register T_{S2} after the ROM is addressed. When load $\overline{\text{enable}}$ goes low, ROM data is allowed to be present at the D input of the shift register via the MUX. The first bit of the ROM data is transferred to the output at the next low-to-high transition of the dot clock. After load $\overline{\text{enable}}$ goes back high, the second to seventh clock pulses shift out the rest of the selected row of the addressed character. Additional clock pulses will shift out low data used for spacing.

Line Cycle – The line counter is a mod 16 counter. A low-to-high transition of the line clock advances the line counter to the next count. If, for any reason, the counts need to be truncated, a low signal at the $\overline{\text{clear}}$ input resets the counter to zero. The clock control may be used as a line clock disable. A high signal at the line clock control terminal enables the counter and a low signal disables the line clock.



Note. Output goes and stays low following the leading edge of the eighth Dot-Clock pulse until Load $\overline{\text{enable}}$ is enabled again and new parallel data is loaded into the shift register.

FIGURE 1. Character Cycle

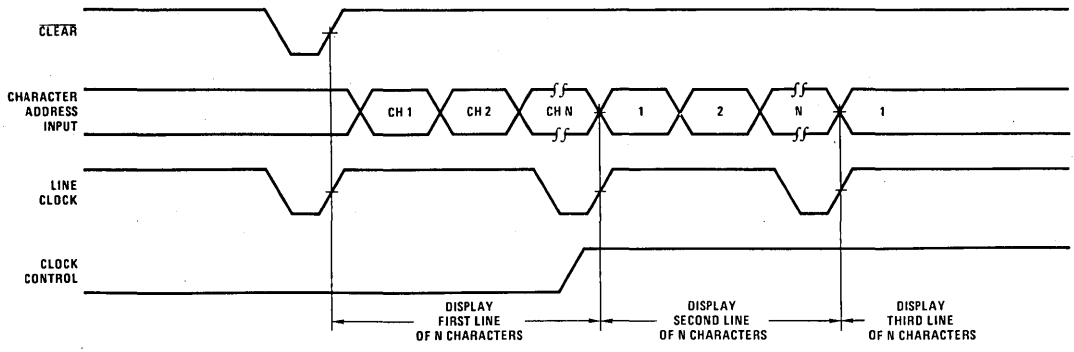


FIGURE 2. Line Cycle

Functional Description (Continued)

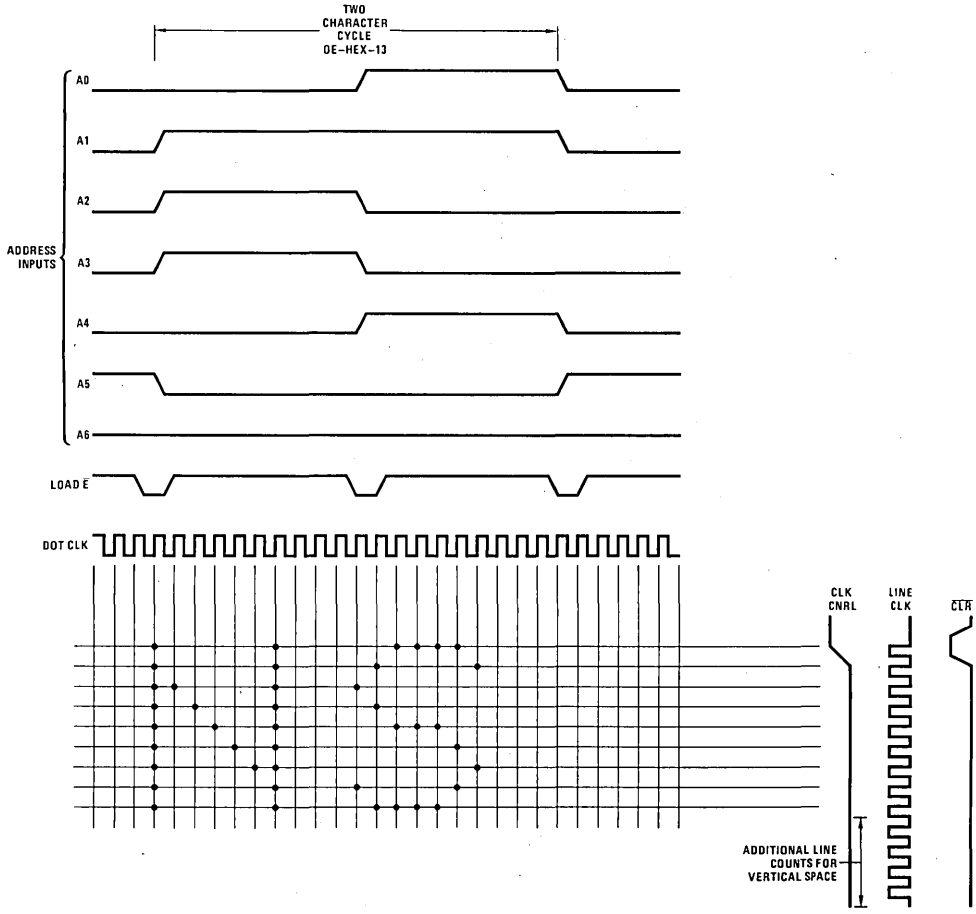
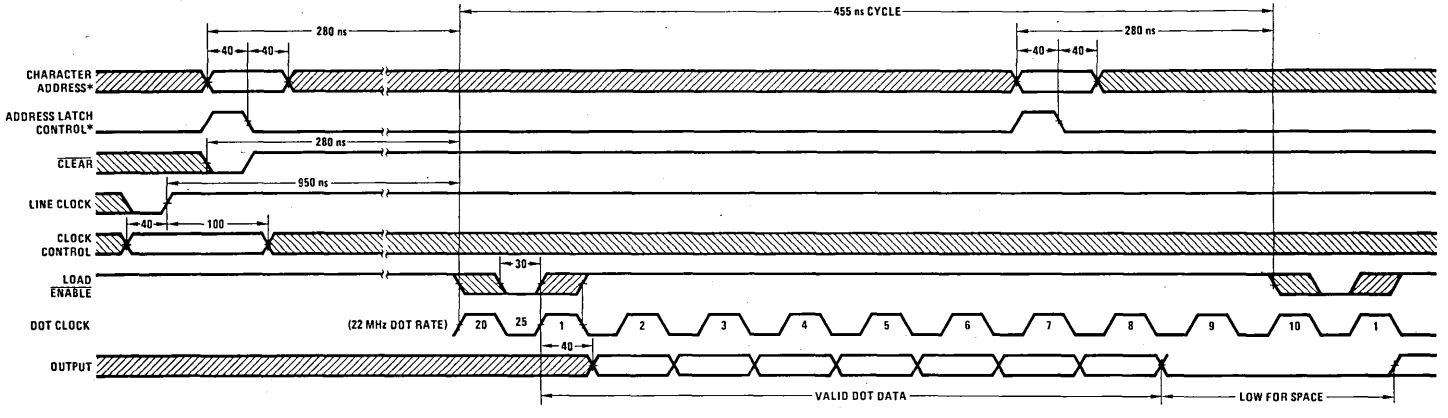


FIGURE 3. Example, Two Character Display Timing — DM86S128CNC



*Shown here for operation with dynamic memory. For static memory operation the address latch control would be tied high and the character addresses would be stable between each address change occurring 280 ns before the high-to-low transition of Load $\overline{\text{enable}}$.

FIGURE 4. Typical System Timing Waveform

Functional Description (Continued)

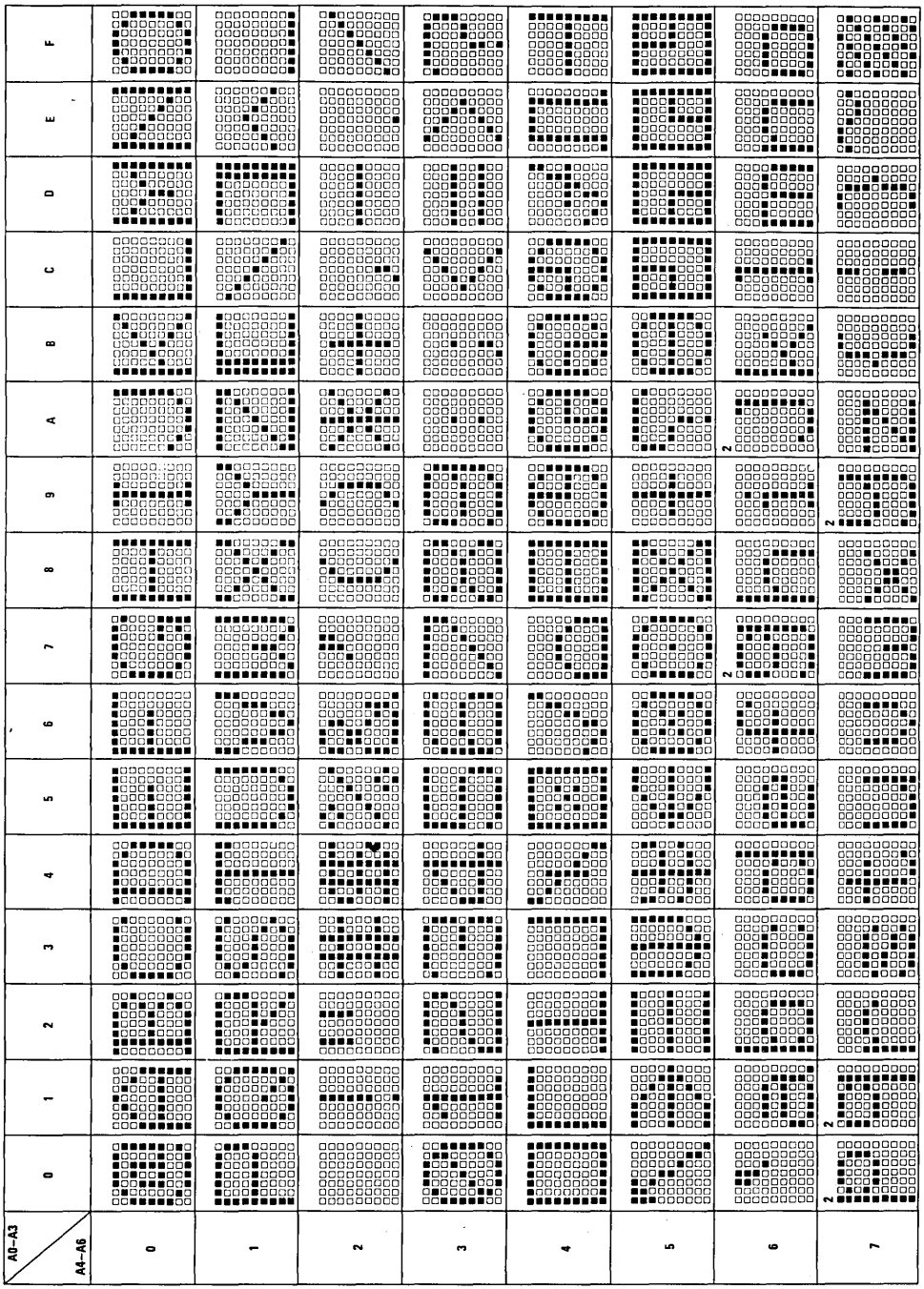


FIGURE 5. DM86S128CNC

Functional Description (Continued)

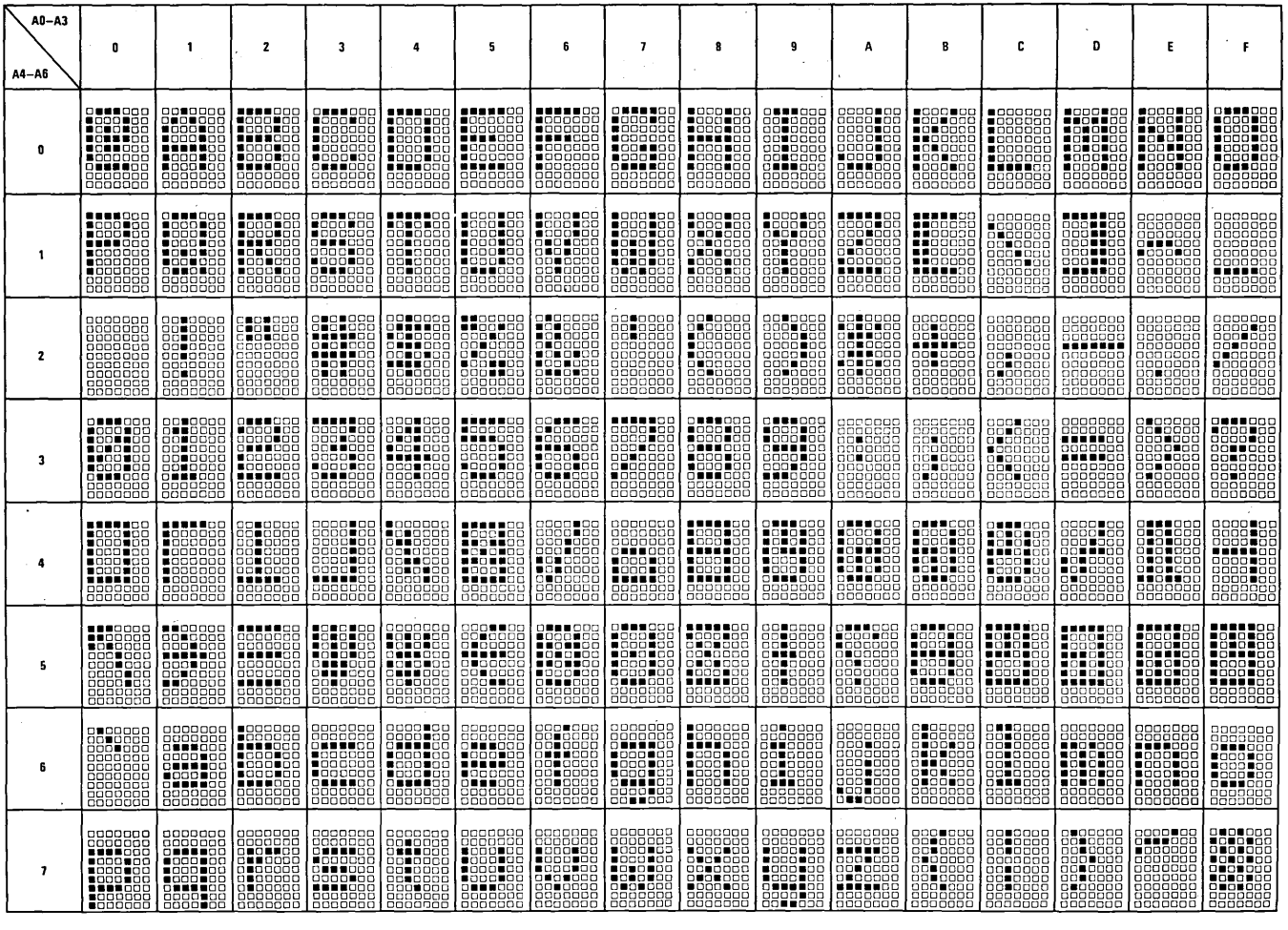


FIGURE 6. DM86S128CND

Functional Description (Continued)

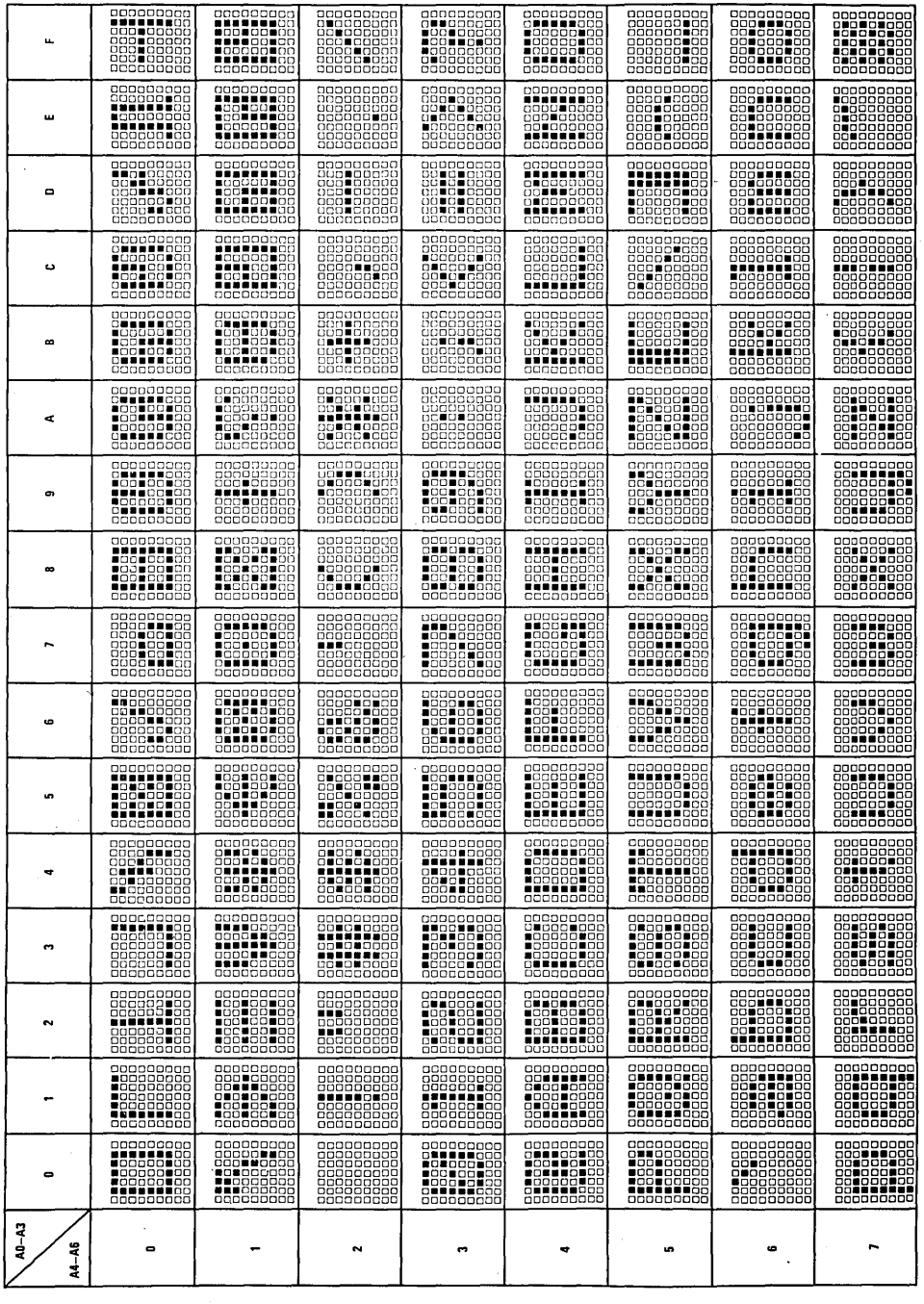


FIGURE 7. DM86S128CQJ

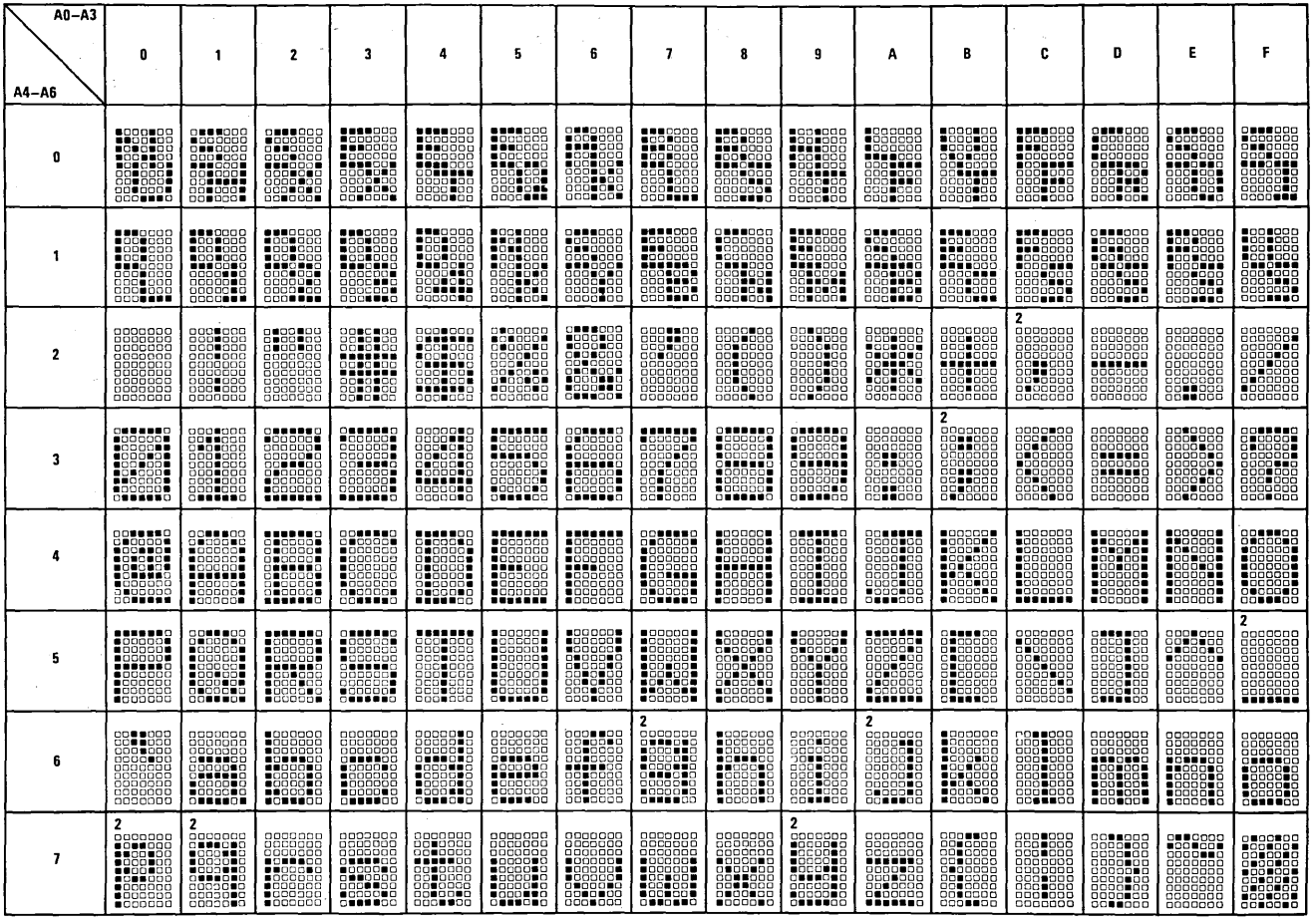


FIGURE 8. DM86S128CQH

MOS
Character Generators

MM5240AA, MM5240AE, MM5241ABL American and European Character Fonts

Three popular 64-character subsets for displays and printers are now available from National as single-chip, standard character generators. These parts, listed in Table 1, are sold off-the-shelf without a ROM masking charge.

The ROMs are static, bipolar-compatible types, operating without clocks on standard power supplies. Row and column access times are typically 450 and 700 ns respectively. An MM5240 2560-bit ROM is used for the 5 x 7 horizontal-scan fonts and an MM5241 3072-bit ROM for the 7 x 5 vertical-scan font. The MM5240 and MM5241 operate over the temperature range of $-25^{\circ}C$ to $+70^{\circ}C$.

Input-output configurations and character formats for the ROMs are shown in Figures 1 and 2. Application Note *AN-40 The Systems Approach to Character Generators* gives examples of line and column address-control logic, and CRT and printer operating techniques. Refer to the MM5240 and MM5241 in section 7 for specifications and ordering information.

TYPE NUMBER	CODE	64-CHARACTER SUBSET	FIGURE		
Horizontal Scan (5 x 7)				CE	
MM5240AA	ASCII	Upper-case alphanumeric	3	1	
MM5240AE	ASCII	Lower-case alpha and symbols	4	1	
Vertical Scan (7 x 5)				CE 1	CE 2
MM5241ABL	ASCII	Upper-case alphanumeric	8	1	1

TABLE 1. Single Chip, Standard Horizontal-Scan and Vertical-Scan Character Generators

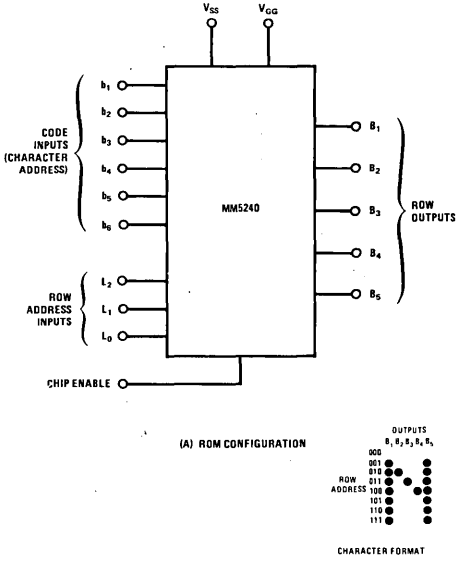


FIGURE 1. Horizontal-Scan Character Generator ROM

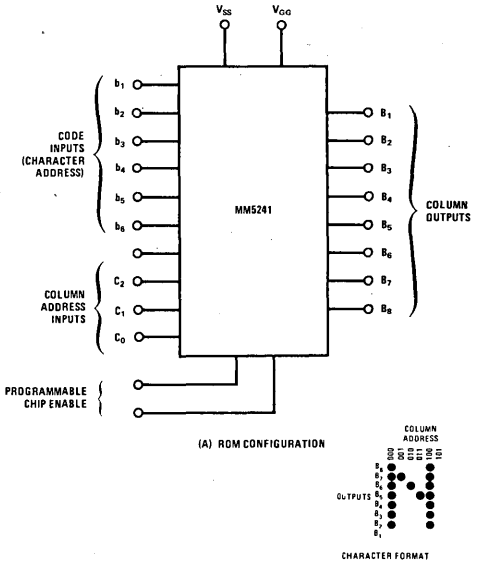


FIGURE 2. Vertical-Scan Character Generator ROM

Note that each ROM has a chip-enable input to permit multi-ROM operation with common control logic. For instance, two horizontal-scan ASCII character generators may be operated in tandem to obtain upper and lower-case characters. In this case, chip-enable would be controlled with bit b_6 of the normal 7-bit ASCII code, and its complement, $\overline{b_6}$.

HORIZONTAL SCAN FONTS

The subsets of 64 5 x 7 characters in the horizontal-scan fonts are the ones most commonly used in low-cost TV and CRT raster-scan displays and dot-matrix line printers.

The MM5240AA contains the ASCII-6 preferred graphic subset, formed from ASCII-7 by ignoring bit b_6. The remaining six bits form two octal address characters. One is formed by the three more significant bits, b_7, b_5 and b_4, and the second by b_3, b_2 and b_1.

Also, characters 36 and 37 in ASCII (x3.4 1968)* are respectively a carat (or circumflex), and an underscore. These are awkward in a video display, so they are replaced by the more useful arrows. (The arrows are related to characters in an older teletypewriter set.) This font is shown in Figure 3. The MM5240 data sheet should be referred to for operating characteristics of all the horizontal-scan character generators.

The MM5240AE generates unique symbols describing the ASCII-7 control codes, as well as lower-case letters (Figure 4). The designer may not wish to display or dot-print the symbols. Since the symbols are generated only when the most significant address bit is logic "0", this bit line may be used to disable the chip, and blank the screen when control signals are transmitted. If not, the system designer can use the symbols as he likes.

*American National Standards Institute (ANSI)

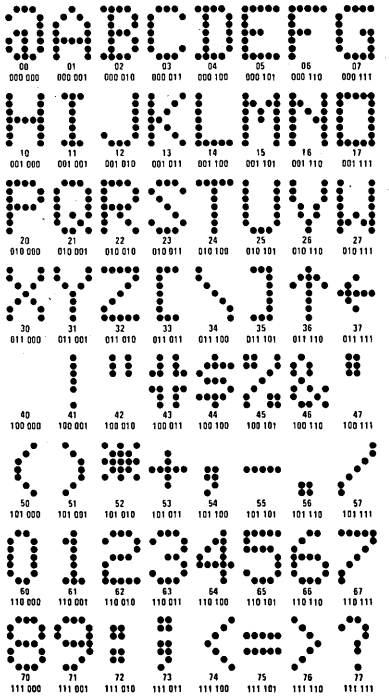


FIGURE 3. MM5240AA Horizontal-Scan ASCII-7 Graphic Subset

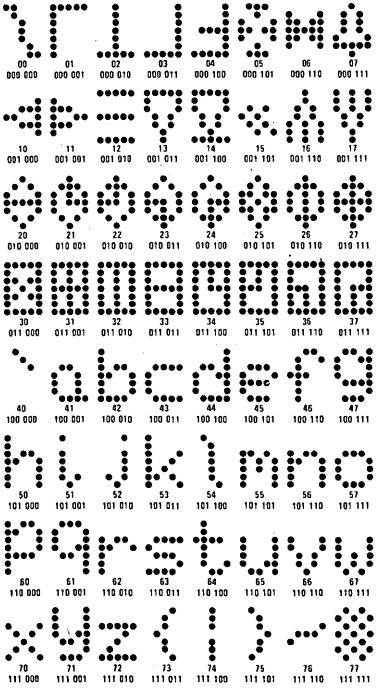


FIGURE 4. MM5240AE Horizontal-Scan ASCII-7 Lower-Case Graphic and Control Symbol Subset

VERTICAL SCAN FONTS

The standard vertical-scan subset in Figure 8 is generated with 6-bit codes derived from code recommendations R646 of the International Organization for Standardization.

The ASCII subset in Figure 5, is practically identical to the horizontal-scan subset. The underscore (character 37) is dropped below the line so that it may be used as a cursor.

Vertical-scan character generators are generally used in dot-matrix tape printers, ink-dot spray printers and high-definition sawtooth or pedestal-scan CRT displays. They may also be used to control raster-scan TV tubes or CRTs if the tube is turned on its side so that the raster scan is made vertically to provide a page-like format.

With standard programming, the bits in the column outputs are sequenced for a sawtooth scan with dot columns running in the same direction, as illustrated in Figure 6a. For a pedestal scan, Figure 6b, alternate columns can be reversed by putting an 8-bit shift left/right TTL shift register (DM74198) on the output as illustrated in Figure 7.

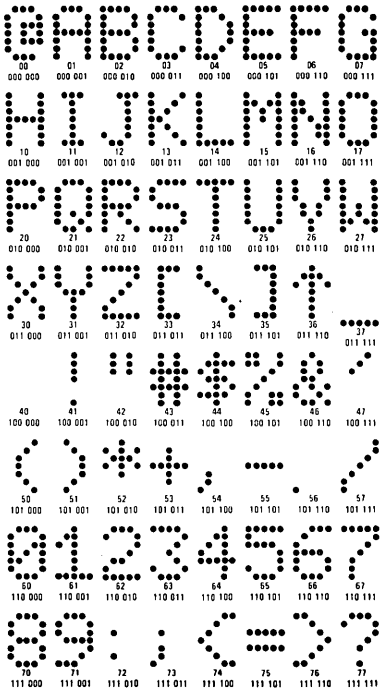


FIGURE 5. MM5241ABL Vertical-Scan ASCII-7 Graphic Subset

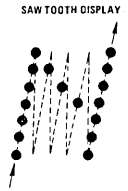


FIGURE 6a. Sawtooth Vertical Scan

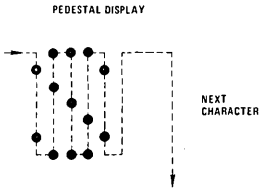


FIGURE 6b. Pedestal Vertical Scan

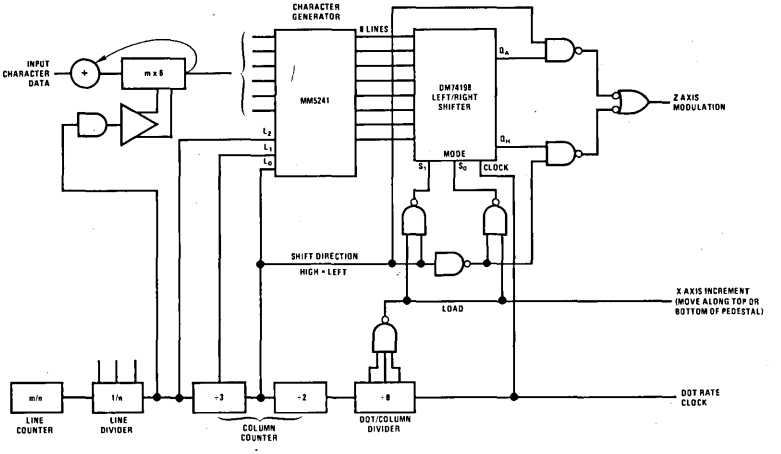


FIGURE 7. Conversion of Sawtooth Output to Pedestal Scan

CUSTOM FONTS

The two ROMs can also be custom-programmed to provide special characters, or fonts larger than 5 x 7. The MM5240 actually stores 64 5 x 8 characters or character segments and the MM5241 stores 64 8 x 6 characters or segments. They are not limited to 5 x 7 and 7 x 5.

For example, the extra height may be used in an otherwise 5 x 7 font to drop the tails of commas, semicolons and lower-case letters below the bottom line of the capital letters. Fonts as large as 16 x 12 are entirely practical without additional control logic, using the chip-enable feature of four MM5241s. Large-font organizations are discussed in AN-40.

National Semiconductor

MM52116FDW, MM52116FDX Character Generators

General Description

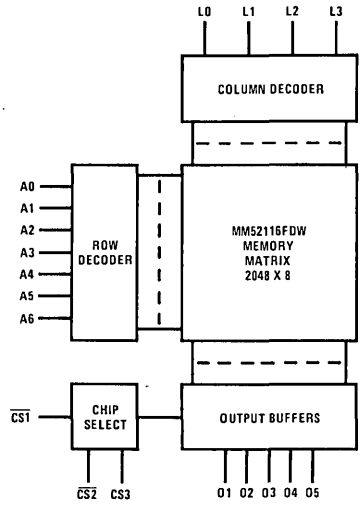
The MM52116FDW, MM52116FDX are 128-character, N-channel, silicon-gate character generators designed primarily for CRT display applications. The MM52116FDW/MM52116FDX provide 5x7 and 7x9 row scan character fonts, respectively. They provide complete DTL/TTL compatibility with single 5V power supply operation.

Features

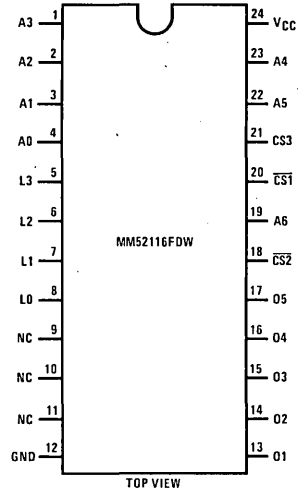
- 128-character row scan
- 5x7 or 7x9 font
- Maximum access time – 450 ns
- TRI-STATE® outputs for bus interface
- Programmable chip selects
- Single 5V power supply
- Inputs and outputs TTL compatible
- MM2316E and MM2716 pin compatible

Block and Connection Diagrams

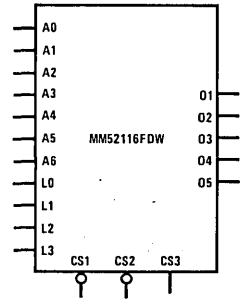
Chip Select Enable Pattern $\overline{CS1}$ = 0, $\overline{CS2}$ = 0, CS3 = 1



Dual-In-Line Package



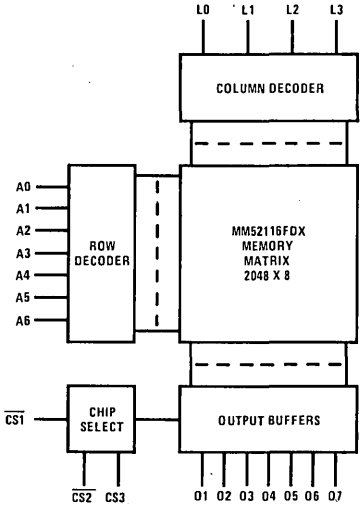
Logic Symbols



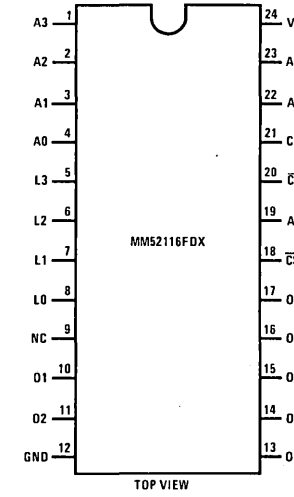
Order Number MM52116FDW-D
or MM52116FDX-D
See NS Package D24C

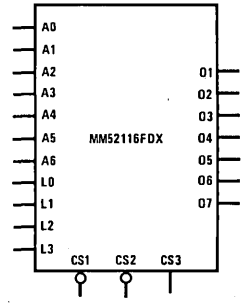
Order Number MM52116FDW-N
or MM52116FDX-N
See NS Package N24A

Chip Select Enable Pattern $\overline{CS1}$ = 1, $\overline{CS2}$ = 0, CS3 = 1



Dual-In-Line Package





8

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.5V to +6.5V
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ±10%, unless otherwise specified).

PARAMETER (Note 2)		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
I_{LI}	Input Current	V_{IN} = 0 to V_{CC}			10	μA
V_{IH}	Logical "1" Input Voltage		2.0		V_{CC}+1.0	V
V_{IL}	Logical "0" Input Voltage		−0.5		0.8	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 3.2 mA			0.4	V
I_{LOH}	Output Leakage Current	V_{OUT} = 4V, Chip Deselected			10	μA
I_{LOL}	Output Leakage Current	V_{OUT} = 0.45V, Chip Deselected			−10	μA
I_{CC1}	Power Supply Current	All Inputs = 5.25V, Data Output Open		70	100	mA

Capacitance

PARAMETER (Note 3)		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
C_{IN}	Input Capacitance (All Inputs)	V_{IN} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, T_A = 25°C, f = 1 MHz, (Note 2)			15.0	pF

AC Electrical Characteristics

(T_A within operating temperature range, V_{CC} = 5V ±10%, unless otherwise specified). See AC test circuit and switching time waveforms.

PARAMETER		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
t_{AC}	Chip Select Access Time	See AC Test Circuit; t_{AC} and t_A Measured to Valid Output Levels with t_r and t_f of Input <20 ns; t_{OFF} Measured to <±20 μA Output Current			120	ns
t_{OFF}	Output Turn OFF Delay				100	ns
t_A	Address Access Time				450	ns

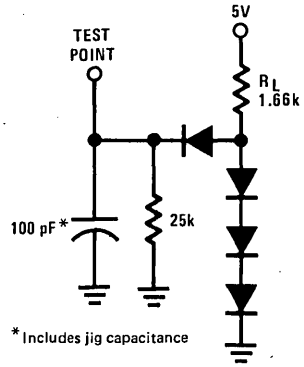
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Positive true logic notation is used: logical "1" = most positive voltage level, logical "0" = most negative voltage level.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: Typical values are for T_A = 25°C and nominal supply voltage.

AC Test Circuit and Switching Time Waveforms



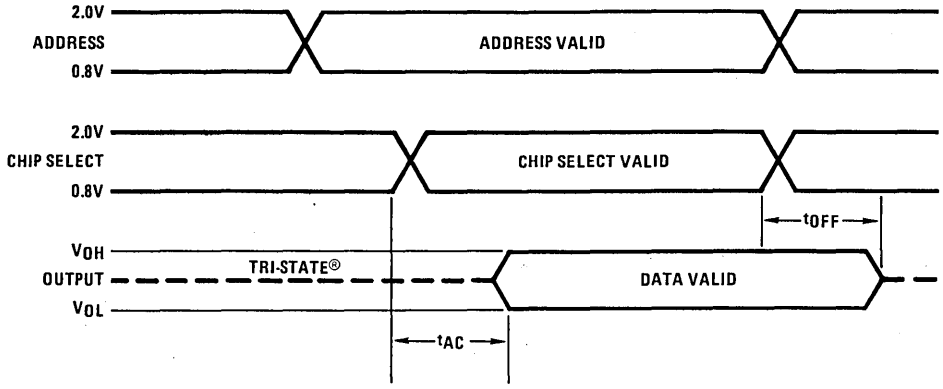


FIGURE 1. Address Precedes Chip Select

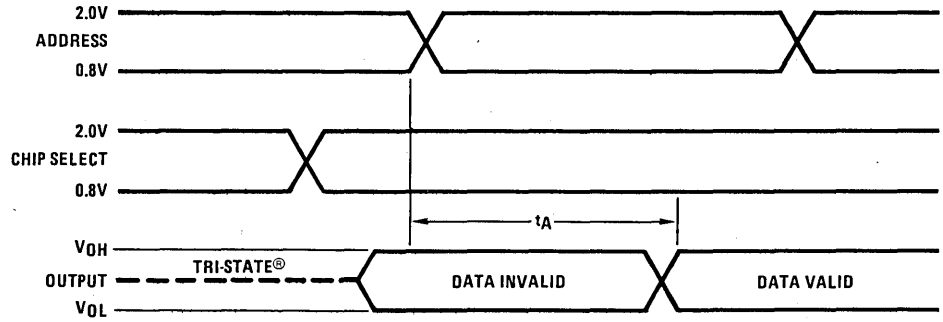


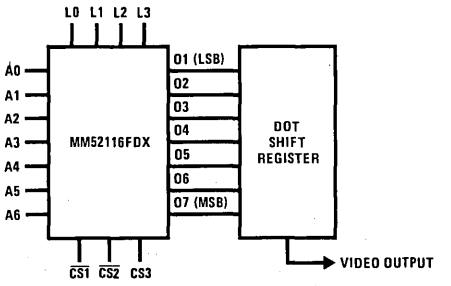
FIGURE 2. Address Follows Chip Select

Functional Description

The chip is selected by applying the proper logic levels to the 3-chip select pins. A 7-bit binary word must be present at the character address inputs, A0–A6 to select a character. The dot matrix of selected characters is generated by cycling the line count address inputs L0–L3 through the line counts necessary to generate the characters. A dot is generated when an output is a "1" (at V_{OH}).

Figure 3 shows an example of the conditions required at the address and line count pins to generate the dot matrix of the character A. *Figures 5 and 6* show the character fonts of the MM52116FDW and MM52116FDX.

Functional Description (Continued)



CHIP SELECT			CHARACTER ADDRESS							LINE COUNT				DOT MATRIX							
$\overline{CS1}$	$\overline{CS2}$	CS3	A6		A4	A3			A0	L3	L2	L1	L0	O7							O1
1	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	0
										0	0	0	1	0	1	0	0	0	1	0
										0	0	1	0	1	0	0	0	0	0	1
										0	0	1	1	1	0	0	0	0	0	1
										0	1	0	0	1	0	0	0	0	0	1
										0	1	0	1	1	1	1	1	1	1	1
										0	1	1	0	1	0	0	0	0	0	1
										0	1	1	1	1	0	0	0	0	0	1
										1	0	0	0	1	0	0	0	0	0	1

Note. A "1" = V_{IH} for address, line count and chip select inputs and a "1" = V_{OH} for outputs.

FIGURE 3. Example of Generating the Character A

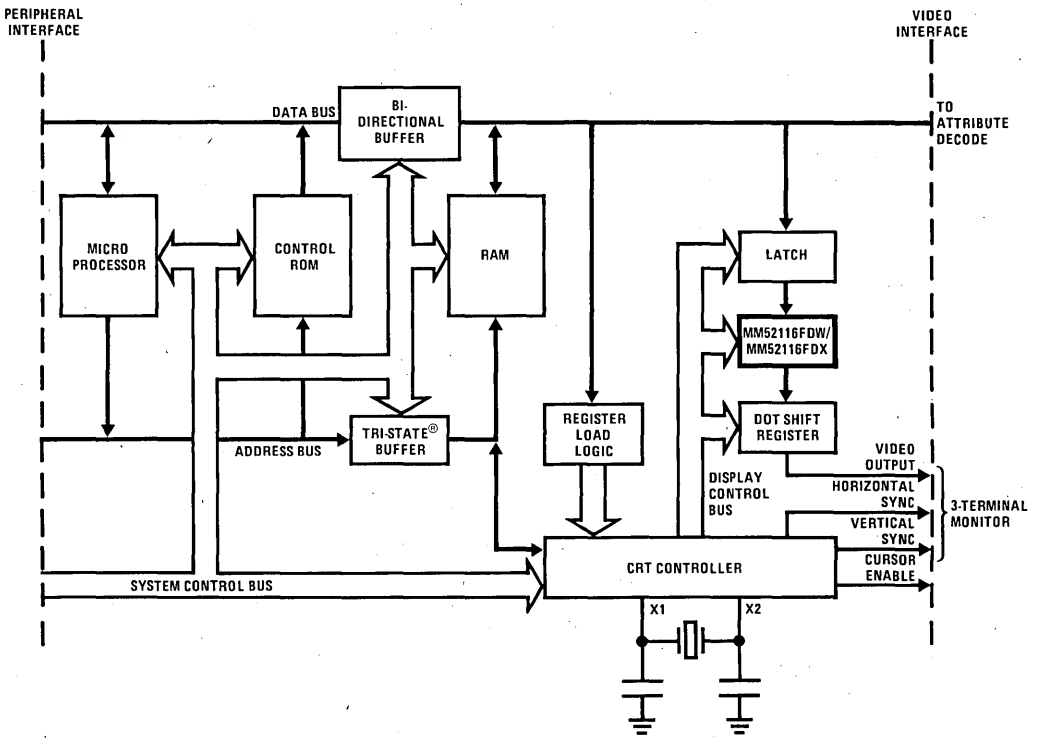


FIGURE 4. Typical MM52116FDW and MM52116FDX Application

Functional Description (Continued)

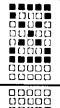
A6	A5 A4 A3 \ A2 A1 A0	000	001	010	011	100	101	110	111
0	000								
0	001								
0	010								
0	011								
0	100								
0	101								
0	110								
0	111								
1	000								
1	001								
1	010								
1	011								
1	100								
1	101								
1	110								
1	111								

FIGURE 5. MM52116FDW

Functional Description (Continued)

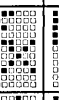
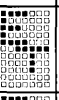
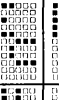
A6	A5 A4 A3 \ A2 A1 A0	000	001	010	011	100	101	110	111
0	000								
0	001								
0	010								
0	011								
0	100								
0	101								
0	110								
0	111								
1	000								
1	001								
1	010								
1	011								
1	100								
1	101								
1	110								
1	111								

FIGURE 6. MM52116FDX

Functional Description (Continued)

MM52116FDX ASCII CHARACTER SET IN HEXADECIMAL REPRESENTATION

Character	7-Bit Hexadecimal Number	Character	7-Bit Hexadecimal Number	Character	7-Bit Hexadecimal Number	Character	7-Bit Hexadecimal Number
NUL	00	SP	20	@	40	\	60
SOH	01	!	21	A	41	a	61
STX	02	"	22	B	42	b	62
ETX	03	#	23	C	43	c	63
EOT	04	$	24	D	44	d	64
ENQ	05	%	25	E	45	e	65
ACK	06	&	26	F	46	f	66
BEL	07	'	27	G	47	g	67
BS	08	(	28	H	48	h	68
HT	09	)	29	I	49	i	69
LF	0A	*	2A	J	4A	j	6A
VT	0B	+	2B	K	4B	k	6B
FF	0C	,	2C	L	4C	l	6C
CR	0D	-	2D	M	4D	m	6D
SO	0E	.	2E	N	4E	n	6E
SI	0F	/	2F	O	4F	o	6F
DLE	10	0	30	P	50	p	70
DC1	11	1	31	Q	51	q	71
DC2	12	2	32	R	52	r	72
DC3	13	3	33	S	53	s	73
DC4	14	4	34	T	54	t	74
NAK	15	5	35	U	55	u	75
SYN	16	6	36	V	56	v	76
ETB	17	7	37	W	57	w	77
CAN	18	8	38	X	58	x	78
EM	19	9	39	Y	59	y	79
SUB	1A	:	3A	Z	5A	z	7A
ESC	1B	;	3B	[	5B		7B
FS	1C	<	3C	\	5C		7C
GS	1D	=	3D	]	5D	ALT	7D
RS	1E	>	3E	↑	5E	ESC	7E
US	1F	?	3F	←	5F	DEL,RUBOUT	7F

Section 9

Memory Support Circuits

9

National offers a complete line of memory drivers, buffers, sense amps, voltage comparators, and other interface circuits. This section provides data on several frequently used interface devices. Refer to National's Interface Integrated Circuits Databook for additional data on our complete line of interface devices.

National offers a selection of memory support circuits to facilitate the interface of memory components in systems architecture. The memory support circuits were developed specifically to accommodate the addressing, clocking, data I/O, and control signals associated with memory systems application as shown in figure 1. Additional circuits are available to interface with data bus structured computers and microprocessors. For additional information contact National's Interface Product Marketing Manager.

FEATURES OF THE TTL LEVEL MOS DRIVERS

Figure 2 compares the switching response of the DS3628 with a 74S TTL gate. Two features can be observed from the switching waveforms: 1) the DS3628 is as fast as the 74S TTL driving TTL loads, and 2) the output high level (V_{OH}) of the DS3628 is higher than that of the 74S TTL.

In a memory system composed of MOS RAMs the load is capacitive and not resistive. Figure 3 compares the switching response of the DS3628 with a 74S TTL gate driving capacitive loads of 50 pF, 150 pF, and 300 pF. The switching waveforms show that the fall time of the DS3628 is as fast as or faster than those of the 74S TTL, but most obvious is the rise time of the DS3628 – much faster than that of the 74S TTL. In addition, the 74S has an objectionable glitch in its rise time. The output high (V_{OH}) level of the DS3628 is higher driving capacitance due to a bootstrap effect in the circuit.

The switching response of the circuits interfacing with a memory array is important since any delay subtracts from the overall memory access time. The switching response driving a capacitive load is more important; as an example, the address drivers might be expected to drive 420 pF in a memory containing 64 MOS RAMs with 5 pF input capacitance each plus 100 pF of board capacitance. The same is typical of clock signals, select signals, and read/write signals.

The input logic levels of MOS RAMs are generally higher than TTL gate levels (typically 400 mV higher). Therefore, the higher output high level (V_{OH}) of the DS3628 is preferable for noise immunity and switching overdrive.

The features of the DS3628 are typical of the other TTL level memory support circuits shown in the Selection Guide.

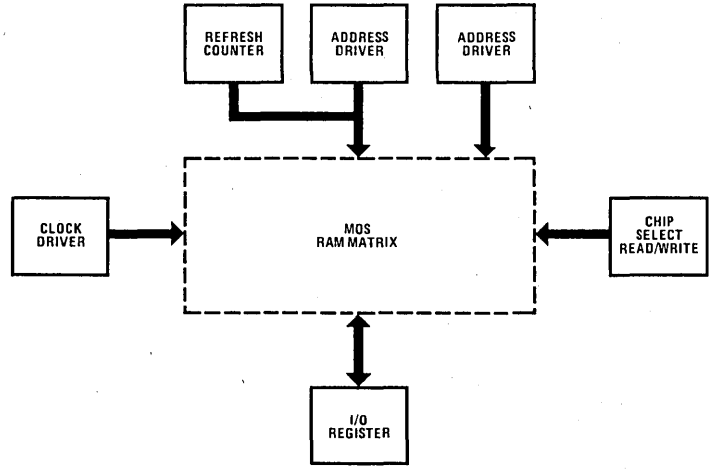


Figure 1. Memory System Block Diagram

DAMPING RINGING OF CLOCK SIGNALS

Ringing of clock signals in a system where the logic fan-out is less than 10 is not generally a big problem, but with higher fan-out the increased capacitive load associated with even a small amount of wiring inductance is a problem. When the capacitance is small the switching currents are small, but as the load increases the increased current through the inductance makes the effect of the inductance increase.

To reduce the associated ringing on the clock signals a resistor may be placed in series with the output of the clock driver to critically dampen the signal response. Many of the memory support circuits are available with this resistor in the output, such as the DS3649 which has a 15Ω dampening resistor, or the DS3679 which is functionally the same without a dampening resistor.

FALL-THROUGH LATCH

In many memory applications a holding register is required either for address or data I/O. Most commercially available registers have an objectionable propagation delay since the circuit's response is the sum of many gate delays. The address and data I/O paths are critical to the memory system access time and a faster register is preferred. The memory support circuits provide a selection of faster latches. These circuits are the DS3645/75 and the DS3647/77/147/177 series. These registers are faster since the latch function is in parallel instead of series with the signal path.

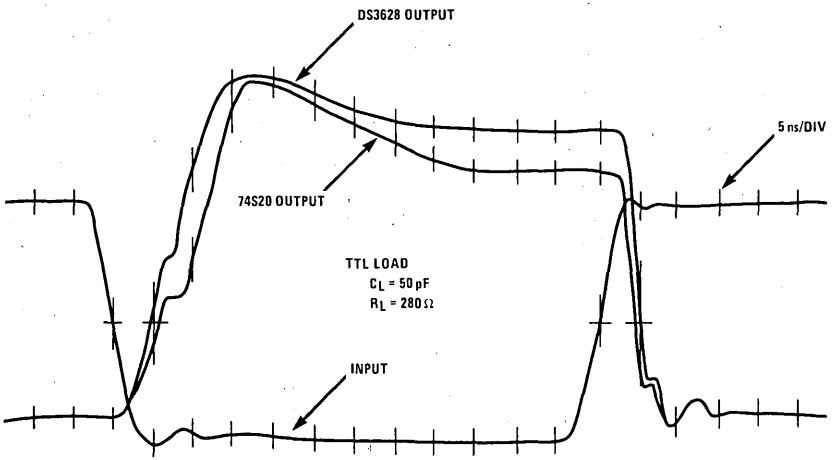


Figure 2. Switching Response with TTL Load

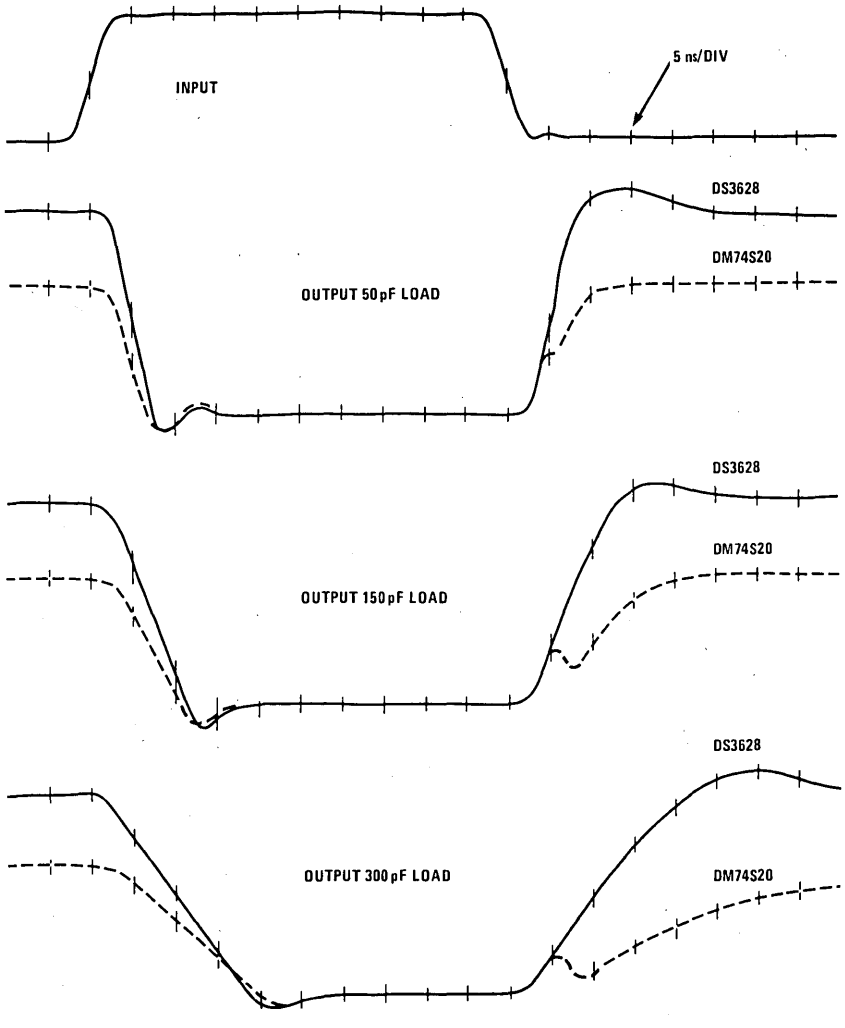


Figure 3. Switching Response with Capacitive Load

SELECTION GUIDE FOR N-CHANNEL MOS MEMORY INTERFACE CIRCUITS

(Refer to 1980 Interface Databook for complete specifications)

Device Number and Name	5V Clock Drivers	12V Clock Drivers	4k RAM Address Drivers	16k RAM Address Drivers	Data I/O	Timing and Control Drivers
CD4520B Dual Synchronous Up Counters				•		
DM8556 TRI-STATE® Programmable Decade/ Binary Counters				•		
DM74LS373, DM74LS374 Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops					•	
DM74S240, DM74S241 Octal TRI-STATE Buffer/Line Driver/ Line Receiver					•	
DP7303/DP8303, DP7304B/DP8304B, DP7307/DP8307, DP7308/DP8308 8-Bit Bidirectional Transceiver Families					•	
DP8212 8-Bit Input/Output Port					•	
DP8216, DP8226 4-Bit Bidirectional Transceiver					•	
DP8350 Programmable CRT Controller Series						•
DS3628 Octal TRI-STATE MOS Driver	•			•		
DS3631, DS3632, DS3633, DS3634 CMOS Dual Peripheral Drivers						•
DS3643, DS3673 Quad Decoded MOS Clock Driver		•				
DS3644, DS3674 Quad MOS Clock Driver		•				
DS3645, DS3675 Hex TRI-STATE MOS Driver Latch			•			
DS3647, DS3677, DS36147, DS36177 Quad TRI-STATE MOS Memory I/O Register					•	
DS3648, DS3678 TRI-STATE MOS Multiplexer/Driver	•		•	•		•
DS3649, DS3679 HEX TRI-STATE MOS Driver	•		•			•
DS36149, DS36179 HEX MOS Driver	•		•			•
DS75322, DS3622 Dual TTL-to-MOS Driver		•				
DS8T26, DS8T28 Quad TRI-STATE Bus Driver					•	
MM74C240, MM74C244 Octal Buffers and Line Drivers with TRI-STATE Outputs					•	
MM74C373, MM74C374 TRI-STATE Octal D-Type Latch and Flip-Flop					•	

National Semiconductor

CD4518BM/CD4518BC, CD4520BM/CD4520BC Dual Synchronous Up Counters

General Description

The CD4518BM/CD4518BC dual BCD counter and the CD4520BM/CD4520BC dual binary counter are implemented with complementary MOS (CMOS) circuits constructed with N and P-channel enhancement mode transistors.

Each counter consists of two identical, independent, synchronous, 4-stage counters. The counter stages are toggle flip-flops which increment on either the positive-edge of CLOCK or negative-edge of ENABLE, simplifying cascading of multiple stages. Each counter can be asynchronously cleared by a high level on the RESET line. All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 6 MHz counting rate (typ) at V_{DD} = 10V

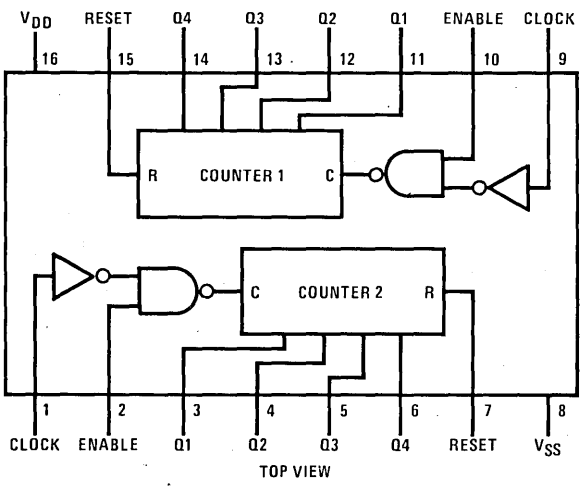
Truth Table

CLOCK	ENABLE	RESET	ACTION
↗	1	0	Increment counter
0	↘	0	Increment counter
↘	X	0	No change
X	↗	0	No change
↗	0	0	No change
1	↘	0	No change
X	X	1	Q1 thru Q4 = 0

X = Don't Care

Connection Diagram

Dual-In-Line and Flat Package



TOP VIEW

National Semiconductor

DM7555/DM8555, DM7556/DM8556 TRI-STATE® Programmable Decade/Binary Counters

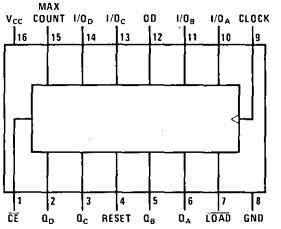
General Description

These circuits are synchronous, edge-sensitive, fully-programmable 4-bit counters. The counters feature both conventional totem-pole and TRI-STATE outputs; such that when the outputs are in the high-impedance mode, they can be used to enter data from the bus lines. In addition, the clear input operates completely independent of all other inputs. During the programming operation, data is loaded into the flip-flops on the positive-going edge of the clock pulse. To facilitate cascading of these counters, the MAX COUNT output can be tied directly into the count enable input.

Features

- DM7555/8555—Decade counter
- DM7556/8556—Binary counter
- Typical clock frequency 35 MHz
- TRI-STATE outputs
- Fully independent clear
- Synchronous loading
- Cascading circuitry provided internally

Connection Diagram



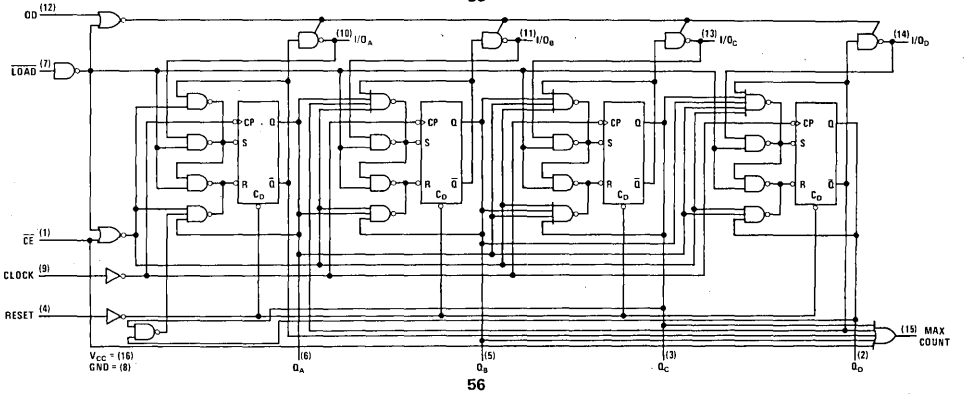
Truth Table

J	K	M	CLEAR	Q_{n+1}
0	0	1	0	Q_n
1	0	1	0	1
0	1	1	0	0
1	1	1	0	$\overline{Q}_n$
X	X	0	0	D
X	X	X	1	0*

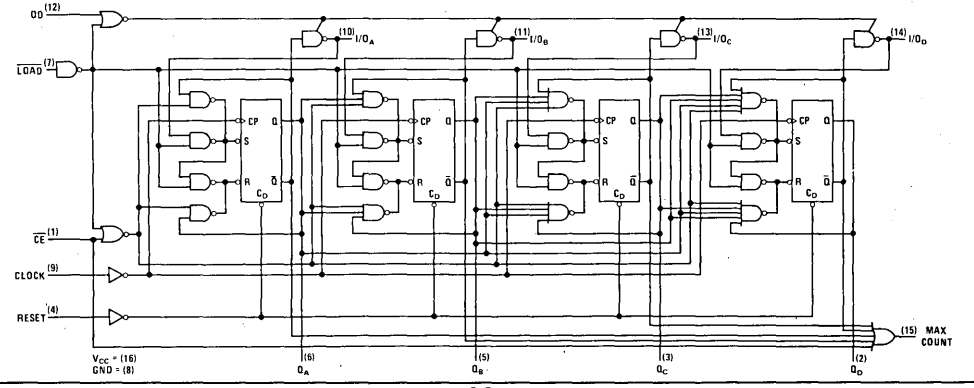
*Asynchronous Transition
Note: See Timing Diagrams

Logic Diagrams

55



56



National Semiconductor

DM54LS373/DM74LS373, DM54LS374/DM74LS374 Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole TRI-STATE® outputs designed specifically for driving highly-capacitive or relatively low impedance loads. The high impedance TRI-STATE and increased high logic level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The 8 latches of the DM54LS373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

The 8 flip-flops of the DM54LS374/DM74LS374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the 8 outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high impedance state the outputs neither load nor drive the bus lines significantly.

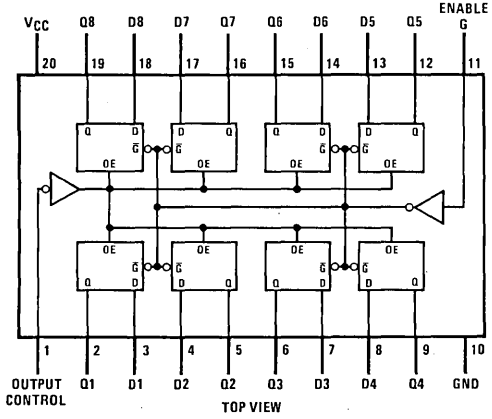
The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are OFF.

Features

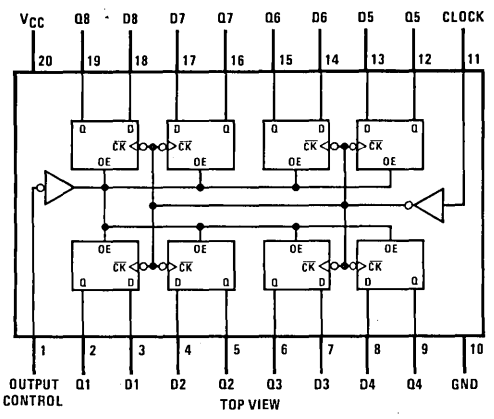
- Choice of 8 latches or 8 D-type flip-flops in a single package
- TRI-STATE bus driving outputs
- Full parallel access for loading
- Buffered control inputs
- PNP inputs reduce DC loading on data lines

Connection Diagrams and Truth Tables

DM54LS373/DM74LS373
Dual-In-Line Package



DM54LS374/DM74LS374
Dual-In-Line Package



ENABLE G	D	OUTPUT
H	H	H
H	L	L
L	X	Q0

CLOCK	D	OUTPUT
↑	H	H
↑	L	L
L	X	Q0

When output control is high, the output is disabled to high impedance state; however, sequential operation of these devices are not affected.

National Semiconductor

DM54S240/DM74S240, DM54S241/DM74S241, DM54S940/DM74S940, DM54S941/DM74S941 Octal TRI-STATE® Buffers/Line Drivers/Line Receivers

General Description

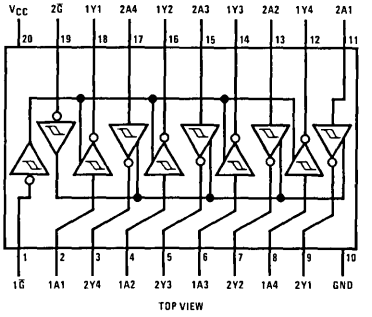
These buffers/line drivers are designed specifically to improve both the performance and PC board density of TRI-STATE® buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs to restore Schottky TTL levels completely, and can be used to drive terminated lines down to 133Ω.

Features

- High performance Schottky TTL line drivers and/or receivers in a high density 20-pin package
- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at inputs improves noise margins

Connection Diagrams

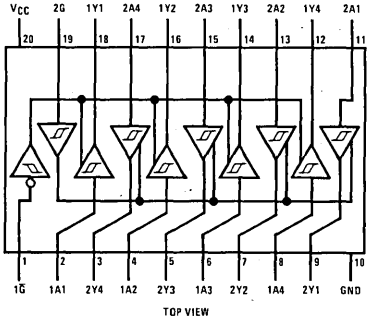
DM54S240/DM74S240



TOP VIEW

$1Y = 1\overline{A}$ when $1\overline{G}$ is low
$2Y = 2\overline{A}$ when $2\overline{G}$ is low
When $1\overline{G}$ is high, 1Y outputs are at a high impedance
When $2\overline{G}$ is high, 2Y outputs are at a high impedance

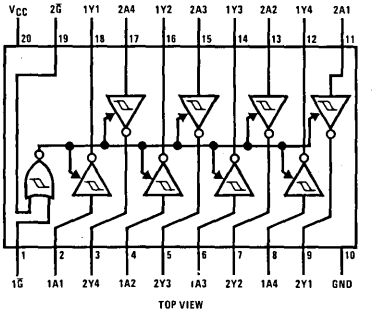
DM54S241/DM74S241



TOP VIEW

1Y = 1A when $1\overline{G}$ is low
2Y = 2A when 2G is high
When $1\overline{G}$ is high, 1Y outputs are at a high impedance
When $2\overline{G}$ is low 2Y outputs are at a high impedance

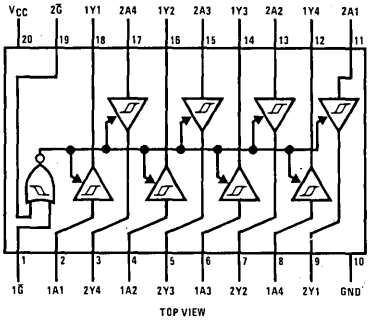
DM54S940/DM74S940



TOP VIEW

$1Y = 1\overline{A}$ when $1\overline{G}$ and $2\overline{G}$ are low
$2Y = 2\overline{A}$ when $1\overline{G}$ and $2\overline{G}$ are low
When either $1\overline{G}$ or $2\overline{G}$ is high, all outputs are a high impedance

DM54S941/DM74S941



TOP VIEW

1Y = 1A when $1\overline{G}$ and $2\overline{G}$ are low
2Y = 2A when $1\overline{G}$ and $2\overline{G}$ are low
When either $1\overline{G}$ or $2\overline{G}$ is high, all outputs are at a high impedance

National Semiconductor

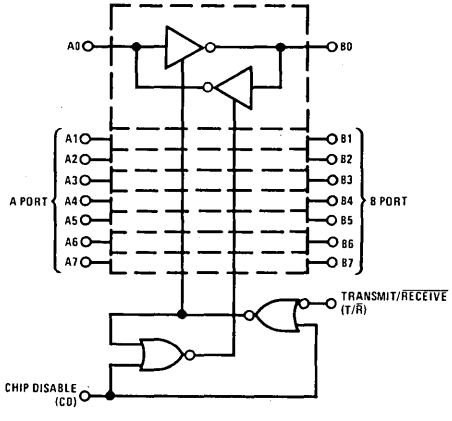
Memory Support Circuits

DP7303/DP8303 8-Bit TRI-STATE® Bidirectional Transceiver (Inverting)

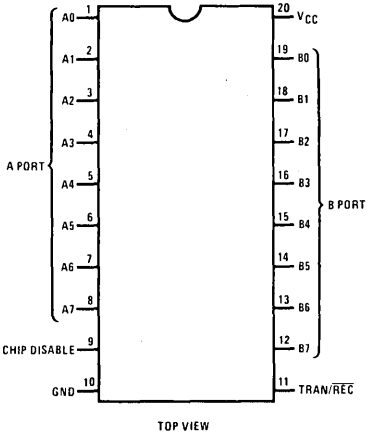
Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Transmit/$\overline{\text{Receive}}$ and chip disable simplify control logic
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Logic Table

INPUTS		RESULTING CONDITIONS	
Chip Disable	Transmit/$\overline{\text{Receive}}$	A Port	B Port
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't care

National Semiconductor

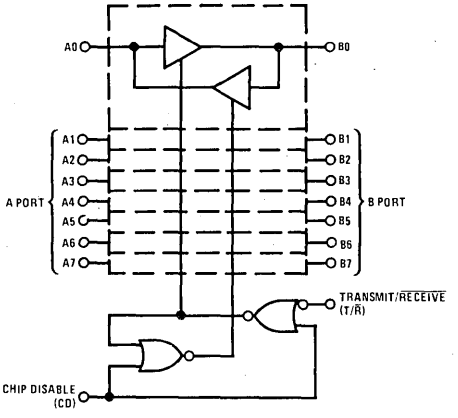
Memory Support Circuits

DP7304B/DP8304B 8-Bit TRI-STATE® Bidirectional Transceiver (Non-Inverting)

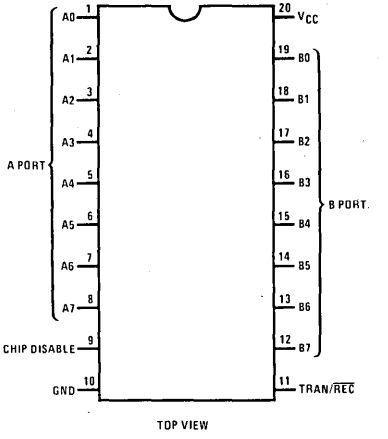
Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Transmit/$\overline{\text{Receive}}$ and chip disable simplify control logic
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Logic Table

INPUTS		RESULTING CONDITIONS	
Chip Disable	Transmit/$\overline{\text{Receive}}$	A Port	B Port
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't care

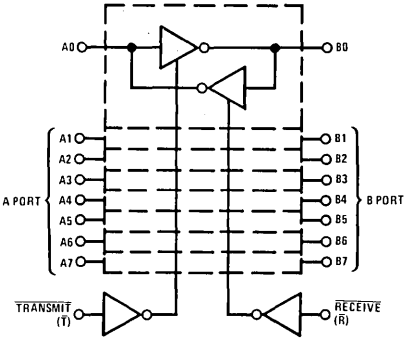
National Semiconductor

DP7307/DP8307 8-Bit TRI-STATE® Bidirectional Transceiver (Inverting)

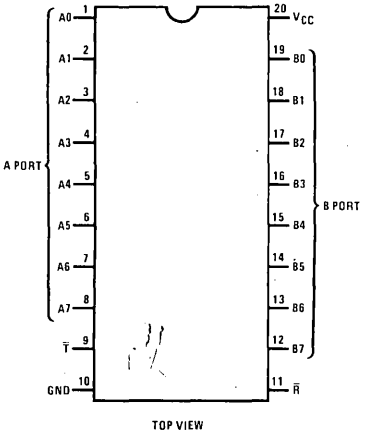
Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Independent $\overline{T}$ and $\overline{R}$ controls for versatility
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Logic Table

CONTROL INPUTS		RESULTING CONDITIONS	
$\overline{\text{Transmit}}$	$\overline{\text{Receive}}$	A Port	B Port
1	0	OUT	IN
0	1	IN	OUT
1	1	TRI-STATE	TRI-STATE
0	0	Both Active*	

*This is not an intended logic condition and may cause oscillations.

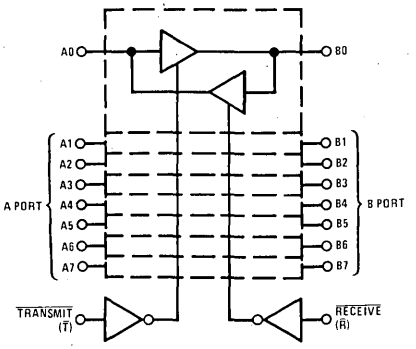
National Semiconductor

DP7308/DP8308 8-Bit TRI-STATE® Bidirectional Transceiver (Non-Inverting)

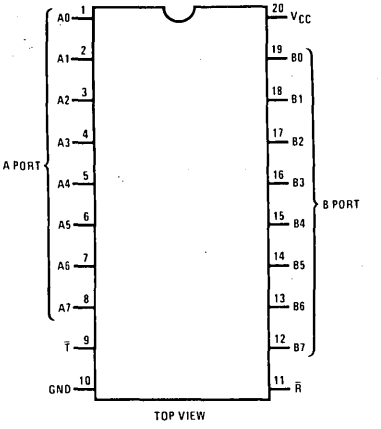
Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Independent $\overline{T}$ and $\overline{R}$ controls for versatility
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



Dual-In-Line Package



Logic Table

CONTROL INPUTS		RESULTING CONDITIONS	
$\overline{\text{Transmit}}$	$\overline{\text{Receive}}$	A Port	B Port
1	0	OUT	IN
0	1	IN	OUT
1	1	TRI-STATE	TRI-STATE
0	0	Both Active*	

*This is not an intended logic condition and may cause oscillations.

National Semiconductor

DP8212, DP8212M 8-Bit Input/Output Port

General Description

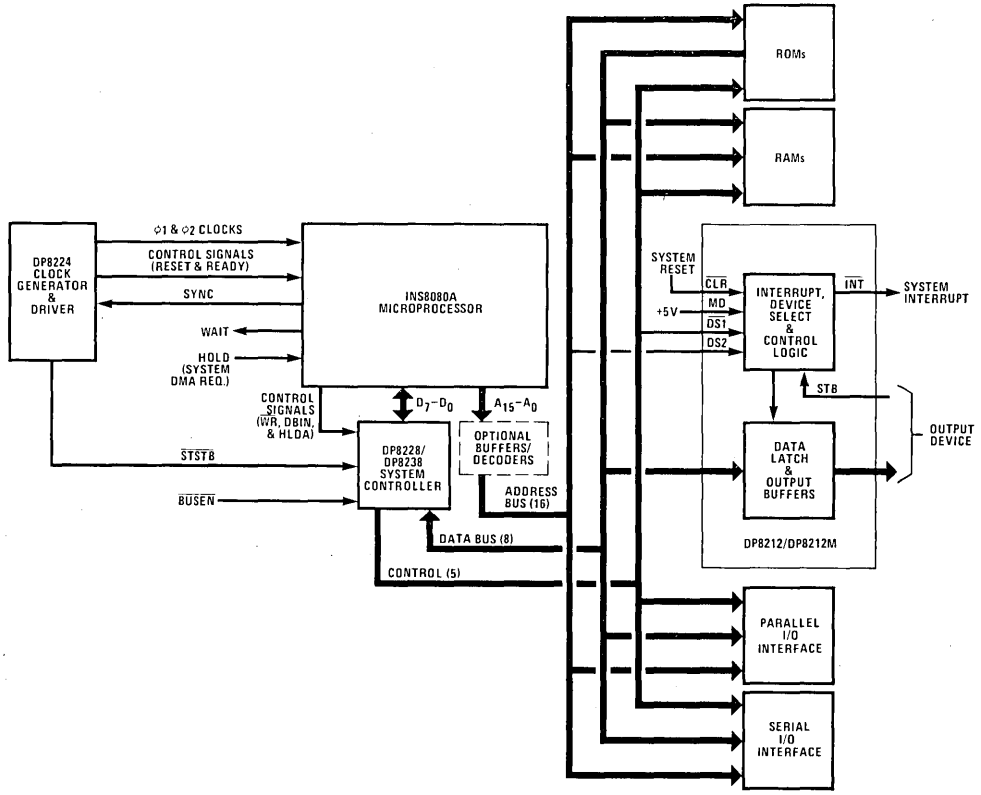
The DP8212/DP8212M is an 8-bit input/output port contained in a standard 24-pin dual-in-line package. The device, which is fabricated using Schottky Bipolar technology, is part of National Semiconductor's N8080 microcomputer family. The DP8212/DP8212M can be used to implement latches, gated buffers, or multiplexers. Thus, all of the major peripheral and input/output functions of a microcomputer system can be implemented with this device.

The DP8212/DP8212M includes an 8-bit latch with TRI-STATE® output buffers, and device selection and control logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

Features

- 8-Bit Data Latch and Buffer
- Service Request Flip-flop for Generation and Control of Interrupts
- 0.25mA Input Load Current
- TRI-STATE TTL Output Drive Capability
- Outputs Sink 15mA
- Asynchronous Latch Clear
- 3.65V Output for Direct Interface to INS8080A
- Reduces System Package Count by Replacing Buffers, Latches, and Multiplexers in Microcomputer Systems

N8080A Microcomputer Family Block Diagram



National Semiconductor

DP8216, DP8216M,DP8226, DP8226M 4-Bit Bidirectional Bus Transceivers

General Description

The DP8216/DP8216M and DP8226/DP8226M are 4-bit bidirectional bus drivers for use in bus oriented applications. The non-inverting DP8216/DP8216M and inverting DP8226/DP8226M drivers are provided for flexibility in system design.

Each buffered line of the four-bit driver consists of two separate buffers that are TRI-STATE® to achieve direct bus interface and bidirectional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB); this side is used to interface to the system side components such as memories, I/O, etc., because its interface is TTL compatible and it has high drive (50 mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bidirectional bus. The DO outputs on this side of the driver have a special high voltage output drive capability so that direct interface to the 8080 type CPUs is achieved with an adequate amount of noise immunity.

The $\overline{CS}$ input is a device enable. When it is "high" the output drivers are all forced to their high-impedance state. When it is a "low" the device is enabled and the direction of the data flow is determined by the DIEN input.

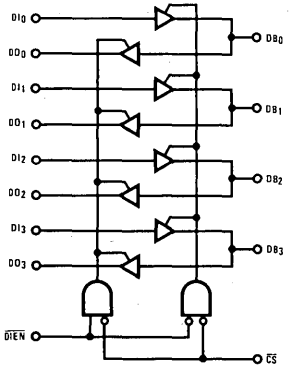
The DIEN input controls the direction of data flow, which is accomplished by forcing one of the pair of buffers into its high-impedance state and allowing the other to transmit its data. A simple two-gate circuit is used for this function.

Features

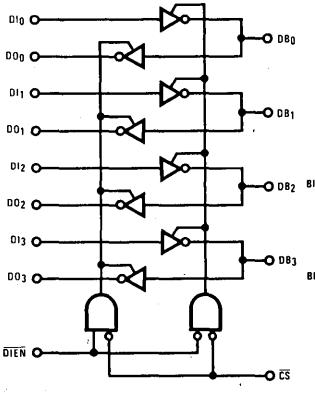
- Data bus buffer driver for 8080 type CPUs
- Low input load current – 0.25 mA maximum
- High output drive capability for driving system data bus – 50 mA at 0.5 V
- Power up-down protection
- DP8216/DP8216M have non-inverting outputs
- DP8226/DP8226M have inverting outputs
- Output high voltage compatible with direct interface to MOS
- TRI-STATE outputs
- Advanced Schottky processing
- Available in military and commercial temperature ranges

Logic and Connection Diagrams

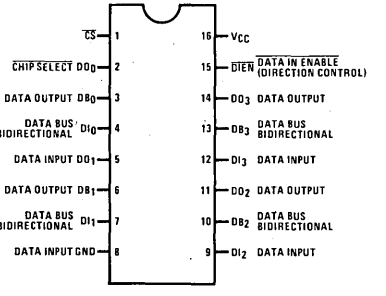
DP8216/DP8216M



DP8226/PD8226M



Dual-In-Line Package



National Semiconductor

DP8350 Series Programmable CRT Controllers

General Description

The DP8350 Series of CRT Controllers are single-chip bipolar (I^2L technology) circuits in a 40-pin package. They are designed to be dedicated CRT display refresh circuits.

The CRT Controller (CRTC) provides an internal dot rate crystal controlled oscillator for ease of system design. For systems where a dot rate clock is already provided, an external clock input may be used by the CRTC. In either case system synchronization is made possible with the use of the buffered Dot Rate Clock Output.

The DP8350 Series has 11 character generation related timing outputs. These outputs are compatible for systems with or without line buffers, using character ROMS, or DM8678-type latch/ROM/shift register circuits.

12 bits (4k) of bidirectional TRI-STATE® character memory addresses are provided by the CRTC for direct interface to character memory.

Three on-chip registers provide for external loading of the row starting address, cursor address, and top-of-page address.

A complete set of video outputs is available including cursor enable, programmable vertical blanking, programmable horizontal sync, and programmable vertical sync.

The DP8350 Series CRTC provides for a wide range of programmability using internal mask programmable ROMs:

- Character Field (both number of dots/character and number of scan lines/character)
- Characters per Row
- Character Rows per Video Frame

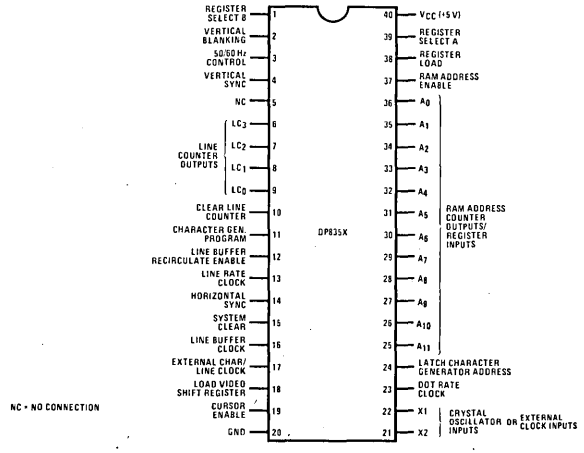
The CRTC also provides system sync and program inputs including 50/60 Hz control, system clear, external character/line rate clock, and character generator program.

The DP8350 Series operates on a single +5 V power supply. Outputs and inputs are TTL compatible.

Features

- Internal crystal controlled dot rate oscillator
- External dot rate clock input
- Buffered dot rate clock output
- Timing pulses for character generation
- Character memory address outputs (12 bits)
- Internal cursor address register
- Internal row starting address register
- Top-of-page address register (for scrolling)
- Programmable horizontal and vertical sync outputs
- Programmable cursor enable output
- Programmable vertical blanking output
- 50/60 Hz refresh rate
- Programmable characters/row (5 to 110)
- Programmable character field size (up to 16 dots x 16 scan line field size)
- Programmable character rows/frame (1 to 64)
- Single +5 V power supply
- Inputs and outputs TTL compatible
- Ease of system design/application

DP8350 Series Connection Diagram



National Semiconductor

DS1628/DS3628 Octal TRI-STATE® MOS Driver

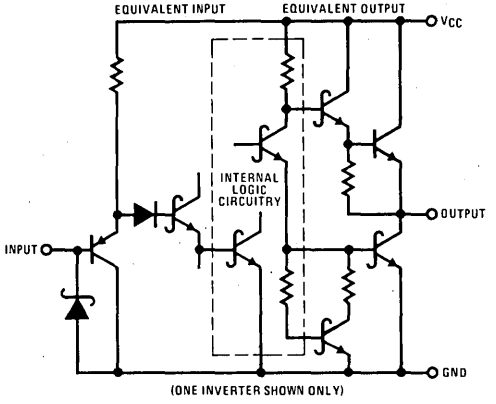
General Description

The DS1628/DS3628 are octal Schottky memory drivers with TRI-STATE® outputs designed to drive high capacitive loads associated with MOS memory systems. The drivers' output (V_{OH}) is specified at 3.4 V to provide additional noise immunity required by MOS inputs. A PNP input structure is employed to minimize input currents. The circuit employs Schottky-clamped transistors for high speed. A NOR gate of two inputs, DIS1 and DIS2, controls the TRI-STATE mode.

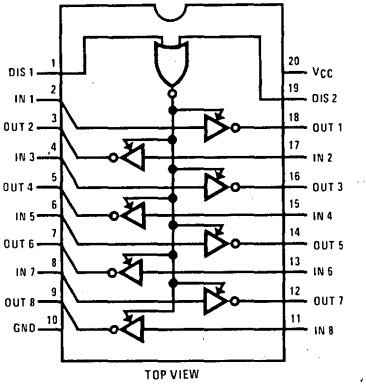
Features

- High speed capabilities
  - typ 5 ns driving 50 pF & 8 ns driving 500 pF
- TRI-STATE outputs
- High V_{OH} (3.4 V min)
- High density
  - eight drivers and two disable controls for TRI-STATE in a 20-pin package
- PNP inputs reduce DC loading on bus lines
- Glitch-free power up/down

Schematic and Connection Diagrams



Dual-In-Line Package

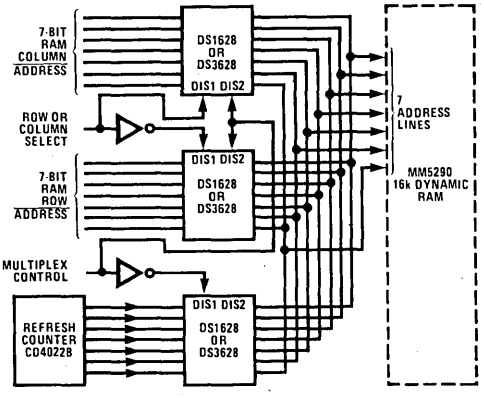


Truth Table

Disable Input		Input	Output
DIS 1	DIS 2		
H	H	X	Z
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

H = high level
L = low level
X = don't care
Z = high impedance (off)

Typical Application



National Semiconductor

Memory Support Circuits

DS1631/DS3631, DS1632/DS3632, DS1633/DS3633, DS1634/DS3634 CMOS Dual Peripheral Drivers

General Description

The DS1631 series of dual peripheral drivers was designed to be a universal set of interface components for CMOS circuits.

Each circuit has CMOS compatible inputs with thresholds that track as a function of V_{CC} (approximately 1/2 V_{CC}). The inputs are PNPs providing the high impedance necessary for interfacing with CMOS.

Outputs have high voltage capability, minimum breakdown voltage is 56V at 250μA.

The outputs are Darlington connected transistors. This allows high current operation (300 mA max) at low internal V_{CC} current levels since base drive for the output transistor is obtained from the load in proportion to the required loading conditions. This is essential in order to minimize loading on the CMOS logic supply.

Typical V_{CC} = 5V power is 28 mW with both outputs ON. V_{CC} operating range is 4.5V to 15V.

The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance OFF state with the same breakdown levels as when V_{CC} was applied.

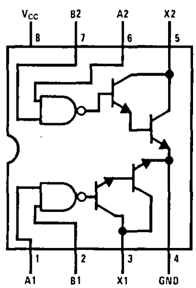
Pin-outs are the same as the respective logic functions found in the following popular series of circuits: DS75451, DS75461, DS3611. This feature allows direct conversion of present systems to the MM74C CMOS family and DS1631 series circuits with great power savings.

The DS1631 series is also TTL/DTL compatible at V_{CC} = 5V.

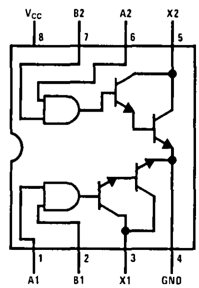
Features

- CMOS compatible inputs
- TTL/DTL compatible inputs
- High impedance inputs — PNP's
- High output voltage breakdown — 56V min
- High output current capability — 300 mA max
- Same pin-outs and logic functions as DS75451, DS75461 and DS3611 series circuits
- Low V_{CC} power dissipation (28 mW both outputs "ON" at 5V)

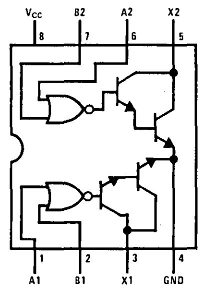
Connection Diagrams (Dual-In-Line and Metal Can Packages)



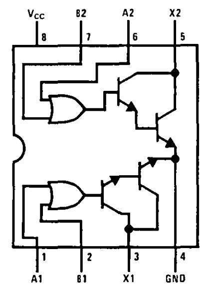
TOP VIEW



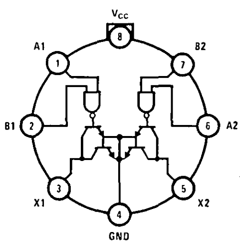
TOP VIEW



TOP VIEW

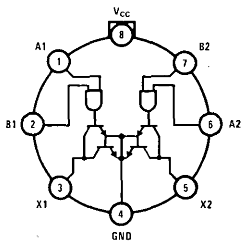


TOP VIEW



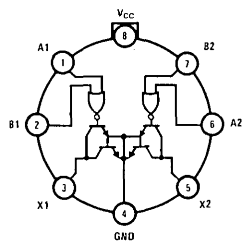
TOP VIEW

(Pin 4 is electrically connected to the case.)



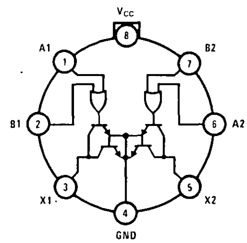
TOP VIEW

(Pin 4 is electrically connected to the case.)



TOP VIEW

(Pin 4 is electrically connected to the case.)



TOP VIEW

(Pin 4 is electrically connected to the case.)

National Semiconductor

DS1644/DS3644, DS1674/DS3674 Quad TTL-MOS Clock Drivers

General Description

The DS1644/DS3644 and DS1674/DS3674 are quad bipolar-to-MOS clock drivers with TTL/DTL compatible inputs. They are designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

The device features two common enable inputs, a refresh input, and a clock control input for simplified system designs. The circuit was designed for driving highly capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transistors are used on all inputs thereby minimizing input loading.

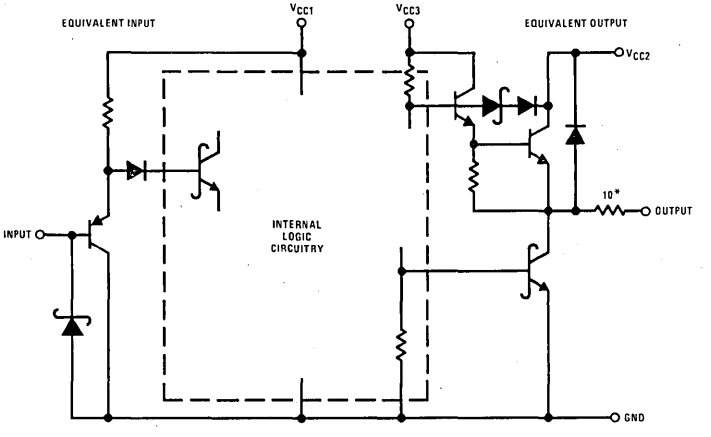
The circuit may be connected to provide a 12V clock output amplitude as required by 4k RAMs or a 5V clock output amplitude as required by 16k RAMs.

The DS1644/DS3644 contains a 10Ω resistor in series with each output to dampen the transients caused by the fast-switching output, while the DS1674/DS3674 has a direct, low impedance output for use with or without an external damping resistor.

Features

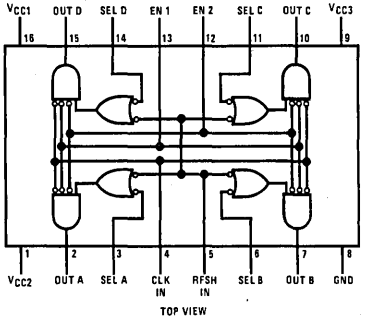
- TTL/DTL compatible inputs
- 12V clock or 5V clock driver
- Operates from standard bipolar and MOS supplies
- PNP inputs minimize loading
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Pin and function compatible with MC3460 and 3235
- Built-in damping resistors (DS1644/DS3644)

Schematic and Connection Diagrams



* DS1644/DS3644 only

Dual-In-Line Package



TOP VIEW

DS1645/DS3645, DS1675/DS3675 Hex TRI-STATE® TTL-MOS Latches/Drivers

General Description

The DS1645/DS3645 and DS1675/DS3675 are hex MOS latches/drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are used to reduce input currents, allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE® outputs which allow bus operation.

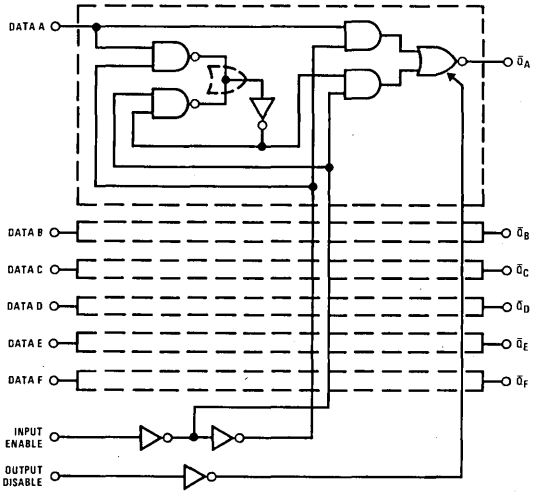
The DS1645/DS3645 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast switching output circuit. The DS1675/DS3675 has a direct, low impedance output for use with or without an external resistor.

The circuit employs a fall-through-latch which captures the data in parallel with the output, thereby eliminating the delay normally encountered in other latch circuits. The DS1645/DS3645 and DS1675/DS3675 may be used for input address lines or input/output data lines of a MOS memory system.

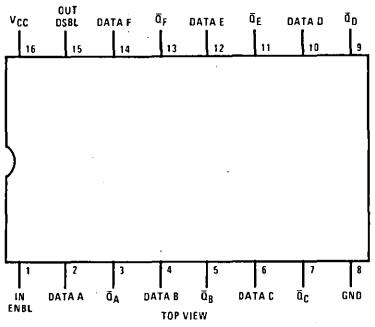
Features

- TTL/DTL compatible inputs
- PNP inputs minimize loading
- Capacitance-driving outputs
- TRI-STATE outputs
- Built-in damping resistor (DS1645/DS3645)

Logic and Connection Diagrams



Dual-In-Line Package



Truth Table

INPUT ENABLE	OUTPUT DISABLE	DATA	OUTPUT	OPERATION
1	0	1	0	Data Feed-Through
1	0	0	1	Data Feed-Through
0	0	X	Q	Latched to Data Present when Enable Went Low
X	1	X	Hi-Z	High Impedance Output

X = Don't care
Hi-Z = TRI-STATE mode

National Semiconductor

DS1647/DS3647, DS1677/DS3677, DS16147/DS36147, DS16177/DS36177 Quad TRI-STATE® MOS Memory I/O Registers

General Description

The DS1647/DS3647 series are 4-bit I/O buffer registers intended for use in MOS memory systems. The circuits employ a fall-through latch for data storage. This method of latching captures the data in parallel with the output, thus eliminating the delays encountered in other designs. The circuits use Schottky-clamped transistor logic for minimum propagation delay and employ PNP input transistors so that input currents are low, allowing large fan-out to these circuits needed in a memory system.

Two pins per bit are provided, and data transfer is bi-directional so that the register can handle both input and output data. The direction of data flow is controlled through the input enables. The latch control, when taken low, will cause the register to hold the data present at that time and display it at the outputs. Data can be latched into the register independent of the output disables or EXPANSION input. Either or both of the outputs may be taken to the high-impedance state with the output disables. The EXPANSION pin disables both outputs to facilitate multiplexing with other I/O registers on the same data lines.

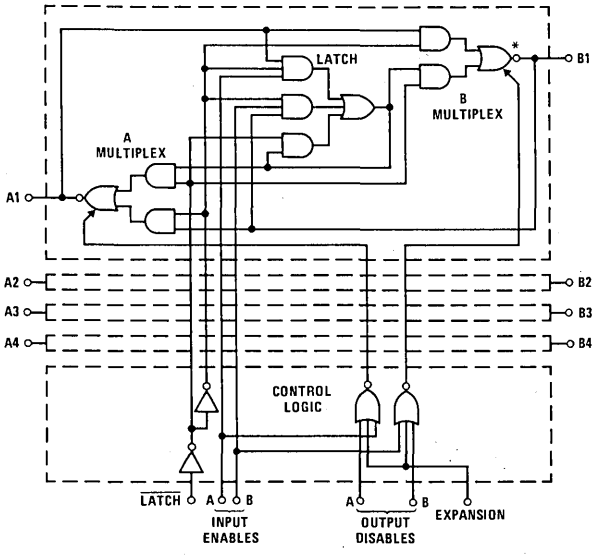
The "B" port outputs in the DS16147/DS36147 and DS16177/DS36177 are open collectors, and in the DS1647/DS3647 and DS1677/DS3677 they are TRI-STATE. The "B" port outputs are also designed for use in bus organized data transmission systems and can sink 80 mA and source −5.2 mA. The "A" port outputs in all four types are TRI-STATE.

Data going from port "A" to port "B" is inverted in the DS1647/DS3647 and DS16147/DS36147 and is not inverted in the DS1677/DS3677 and DS16177/DS36177. Data going from port "B" to port "A" is inverted in all four types.

Features

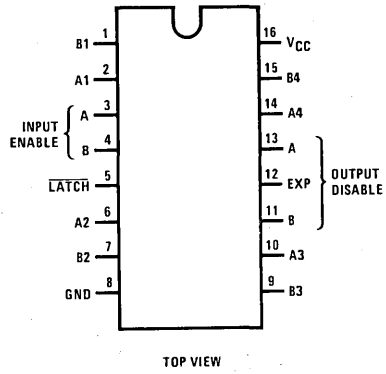
- PNP inputs minimize loading
- Fall-through latch design
- Propagation delay of only 15 ns
- TRI-STATE outputs
- EXPANSION control
- Bi-directional data flow
- TTL/DTL compatible
- Transmission line driver output

Logic and Connection Diagrams



*Inverting DS1647/DS3647 and DS16147/DS36147 only

Dual-In-Line Package



TOP VIEW

National Semiconductor

DS1648/DS3648, DS1678/DS3678 TRI-STATE® MOS Multiplexers/Drivers

General Description

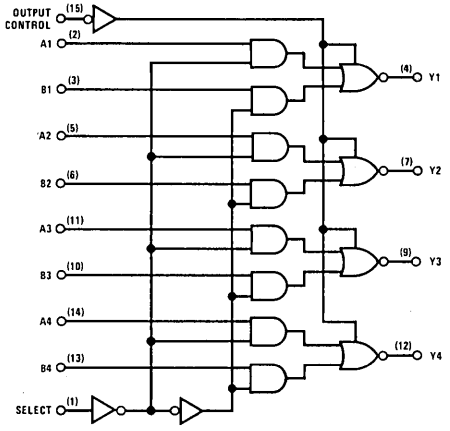
The DS1648/DS3648 and DS1678/DS3678 are quad 2-input multiplexers with TRI-STATE outputs designed to drive the large capacitive loads (up to 500 pF) associated with MOS memory systems. A PNP input structure is employed to minimize input currents so that driver loading in large memory systems is reduced. The circuit employs Schottky-clamped transistors for high speed and TRI-STATE outputs for bus operation.

The DS1648/DS3648 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1678/DS3678 has a direct, low impedance output for use with or without an external resistor.

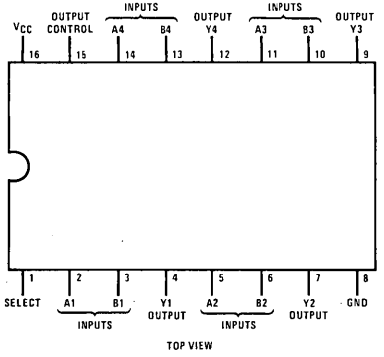
Features

- TRI-STATE outputs interface directly with system bus
- Schottky-clamped for better ac performance
- PNP inputs to minimize input loading
- DTL and TTL compatible
- High-speed capacitive load drivers
- Built-in damping resistor (DS1648/DS3648 only)

Logic and Connection Diagrams

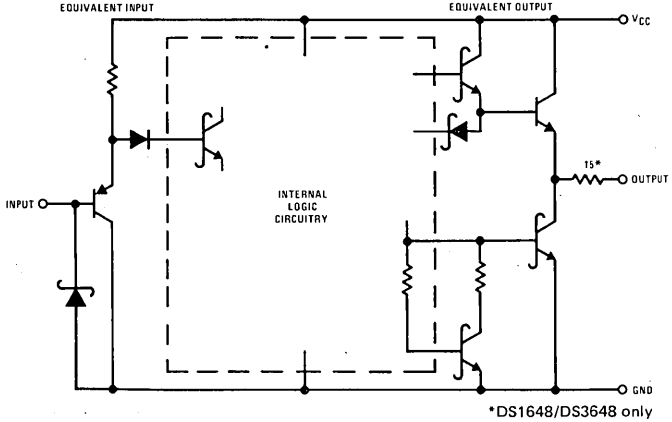


Dual-In-Line Package



TOP VIEW

Schematic Diagram



*DS1648/DS3648 only

National Semiconductor

DS1649/DS3649, DS1679/DS3679
Hex TRI-STATE® TTL-MOS Drivers

General Description

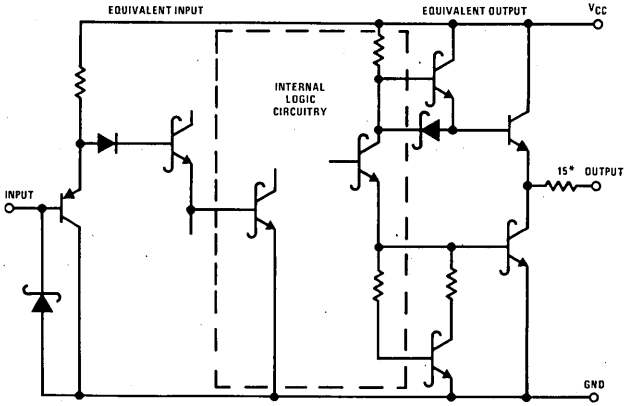
The DS1649/DS3649 and DS1679/DS3679 are Hex TRI-STATE MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE outputs for bus operation.

The DS1649/DS3649 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1679/DS3679 has a direct low impedance output for use with or without an external resistor.

Features

- High speed capabilities
  - Typ 9 ns driving 50 pF
  - Typ 30 ns driving 500 pF
- TRI-STATE outputs for data bussing
- Built-in 15 Ω damping resistor (DS1649/DS3649)
- Same pin-out as DM8096 and DM74366

Schematic Diagram



*DS1649/DS3649 only

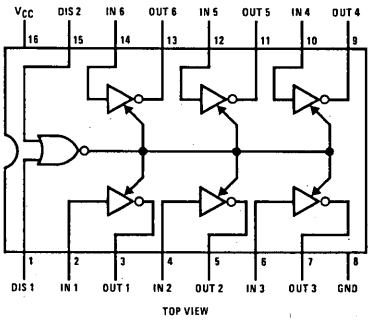
Truth Table

DISABLE INPUT		INPUT	OUTPUT
DIS 1	DIS 2		
0	0	0	1
0	0	1	0
0	1	X	Hi-Z
1	0	X	Hi-Z
1	1	X	Hi-Z

X = Don't care
Hi-Z = TRI-STATE mode

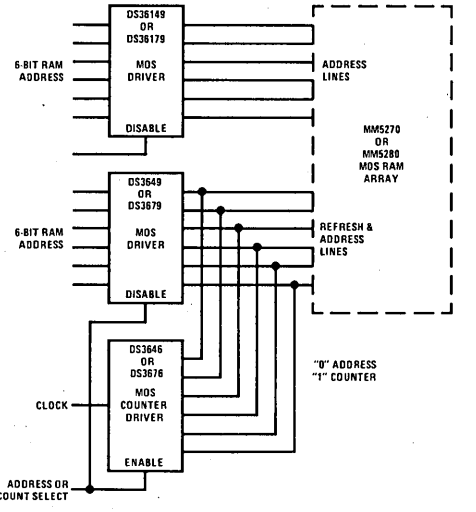
Connection Diagram

Dual-In-Line Package



TOP VIEW

Typical Application



National Semiconductor

DS3643, DS3673 Decoded Quad MOS Clock Drivers

General Description

The DS3643 and DS3673 are quad bipolar-to-MOS decoder/clock drivers with TTL/DTL compatible inputs. They are designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

The device features full decoding of input address lines from two inputs to one of four outputs. Also featured is the capability of expanding to three inputs to one of eight outputs with the use of the Expansion and $\overline{\text{Expansion}}$ inputs. Also included are clock and refresh inputs.

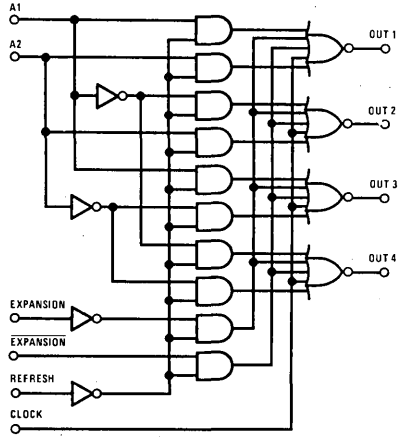
The circuit was designed for driving large capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transistors are used on all inputs, thereby minimizing input loading.

The DS3643 has a 10 Ω damping resistor in series with each output to dampen transients caused by the fast switching output. while the DS3673 has a direct, low impedance output, for use with or without an external resistor.

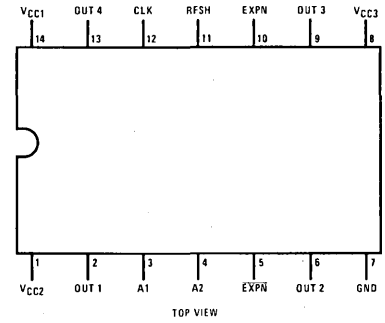
Features

- TTL/DTL compatible inputs
- Operates from standard bipolar and MOS supplies
- PNP inputs minimize input loading
- Full logic decoding for either two inputs to one of four outputs or three inputs to one of eight outputs
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Built-in damping resistors (DS3643)

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Truth Table

INPUTS						OUTPUTS			
CLOCK	REFRESH	EXPANSION	$\overline{\text{EXPANSION}}$	A_2	A_1	OUT 1	OUT 2	OUT 3	OUT 4
1	X	X	X	X	X	0	0	0	0
0	1	X	X	X	X	1	1	1	1
0	0	1	0	0	0	1	0	0	0
0	0	1	0	0	1	0	1	0	0
0	0	1	0	1	0	0	0	1	0
0	0	1	0	1	1	0	0	0	1
0	0	1	1	X	X	0	0	0	0
0	0	0	1	X	X	0	0	0	0
0	0	0	0	X	X	0	0	0	0

X = don't care state

National Semiconductor

DS16149/DS36149, DS16179/DS36179 Hex MOS Drivers

General Description

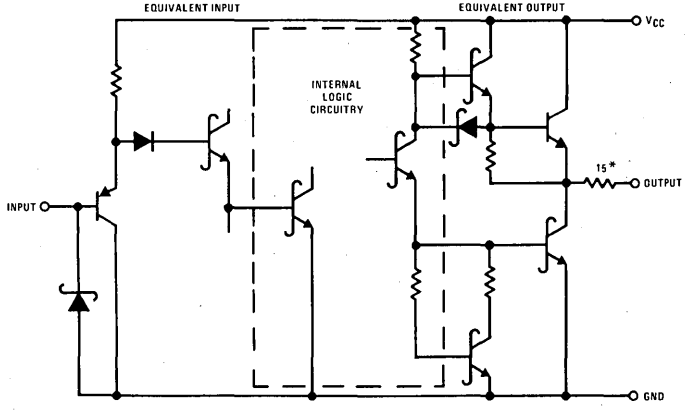
The DS16149/DS36149 and DS16179/DS36179 are Hex MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and a disable control that places the outputs in the logic "1" state (see truth table). This is especially useful in MOS RAM applications where a set of address lines has to be in the logic "1" state during refresh.

The DS1649/DS3649 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1679/DS3679 has a direct low impedance output for use with or without an external resistor.

Features

- High speed capabilities
  - Typ 9 ns driving 50 pF
  - Typ 29 ns driving 500 pF
- TRI-STATE outputs for data bussing
- Built-in 15 Ω damping resistor (DS16149/DS36149)
- Same pin-out as DM8096 and DM74366

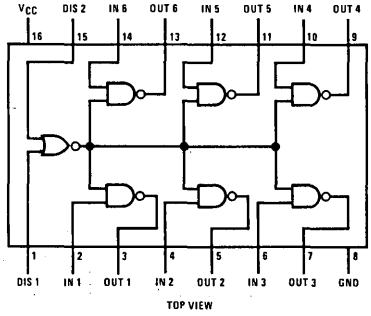
Schematic Diagram



*DS16149/DS36149 only.

Connection Diagram

Dual-In-Line Package



TOP VIEW

Truth Table

DISABLE INPUT		INPUT	OUTPUT
DIS 1	DIS 2		
0	0	0	1
0	0	1	0
0	1	X	1
1	0	X	1
1	1	X	1

X = Don't care

National Semiconductor

DS75322 Dual TTL-MOS Driver
DS3622 Dual Fail-Safe TTL-MOS Driver

General Description

The DS75322 is a dual TTL-MOS high speed driver. The input structure of the device is TTL and DTL compatible. A common strobe input is provided for gating the outputs to the low state. The outputs provide high current and high voltage levels ideal for driving MOS circuits. The DS75322 specifically meets the requirements for driving N-channel RAMs where low power dissipation is desirable when the driver is in the low state.

The DS3622 provides output fail-safe protection. Powering down V_{CC1} activates the fail-safe circuit, forcing the outputs to the low state. The fail-safe feature eliminates output glitches that may occur in systems that power down V_{CC1}. Functionally, the DS3622 and the DS75322 are identical.

The DS75322, DS3622 require 2 external PNP transistors per package.

The DS75322, DS3622 are characterized for operation from 0°C to +70°C.

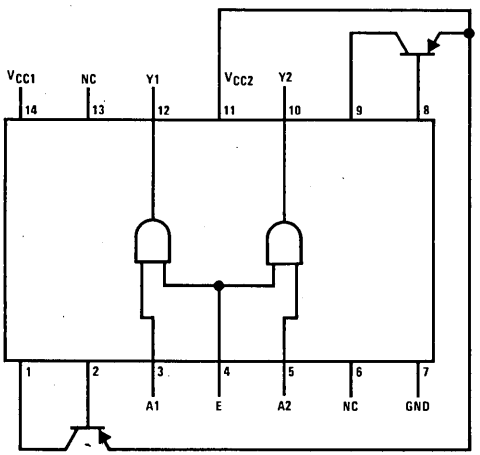
The DS75322 and the DS3622 are ideal for driving the UPD411D, MM5280 and the MM5270 4k RAMs.

Features

- Dual positive-logic and TTL-MOS driver
- TTL and DTL compatible inputs
- High voltage/current outputs
- Operates from standard bipolar and MOS supplies
- High speed switching
- Input and output clamping diodes
- Separate driver address inputs with common strobe
- V_{OH} and V_{OL} compatible with 4k RAMs and other popular MOS RAMs
- No current (leakage only) when outputs are in low state (DS75322)
- Outputs forced to low state with loss of V_{CC1} (DS3622)

Connection Diagram

Dual-In-Line Package



TOP VIEW

Positive Logic Y = AE
Recommended PNP Transistors
2N5910, 2N5771

National Semiconductor

DS8T26A, DS8T26AM, DS8T28, DS8T28M
4-Bit Bidirectional Bus Transceivers

General Description

The DS8T26A, DS8T28 consists of 4 pairs of TRI-STATE® logic elements configured as quad bus drivers/receivers along with separate buffered receiver enable and driver enable lines. This single IC quad transceiver design distinguishes the DS8T26A, DS8T28 from conventional multi-IC implementations. In addition, the DS8T26A, DS8T28's ultra high speed while driving heavy bus capacitance (300 pF) makes these devices particularly suitable for memory systems and bidirectional data buses.

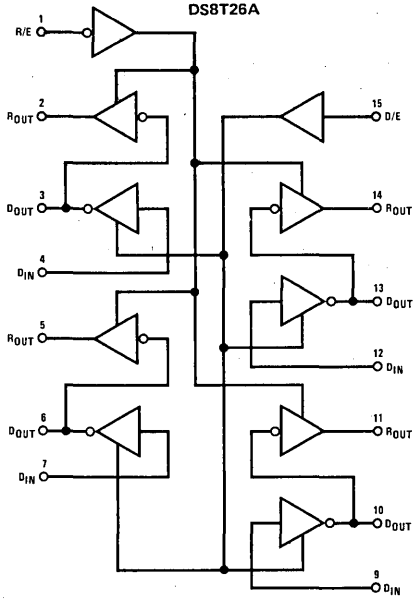
Both the driver and receiver gates have TRI-STATE outputs and low current PNP inputs. PNP inputs reduce input loading to 200 μA maximum.

Features

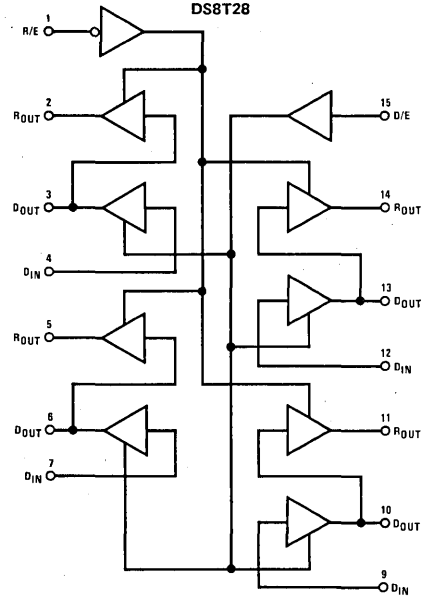
- Inverting outputs in the DS8T26A
- Non-inverting outputs in the DS8T28
- TRI-STATE outputs
- Low current PNP inputs
- Fast switching times (20 ns)
- Advanced Schottky processing
- Driver glitch free power up/down
- Non-overlapping TRI-STATE

Logic and Connection Diagrams

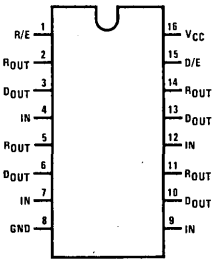
DS8T26A



DS8T28



Dual-In-Line Package



TOP VIEW

National Semiconductor

MM54C240/MM74C240 Inverting Outputs
MM54C244/MM74C244 Non-Inverting Outputs
Octal Buffers and Line Drivers with TRI-STATE® Outputs

General Description

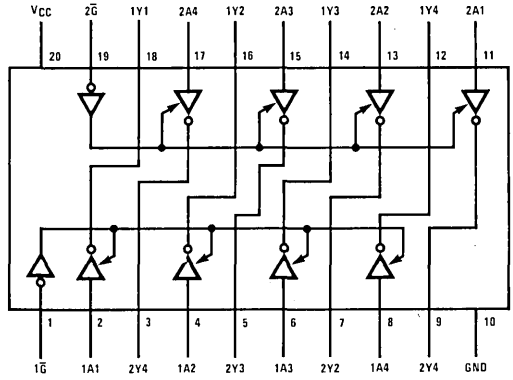
These octal buffers and line drivers are monolithic complementary MOS (CMOS) integrated circuits with TRI-STATE® outputs. These outputs have been specially designed to drive highly capacitive loads such as bus-oriented systems. These devices have a fan-out of 6 low power Schottky loads. A high logic level on the output disable control input G makes the outputs go into the high impedance state.

Features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{CC} typ
- Low power consumption
- High capacitive load
- TRI-STATE® outputs
- Input protection
- TTL compatibility
- 20-pin dual-in-line package

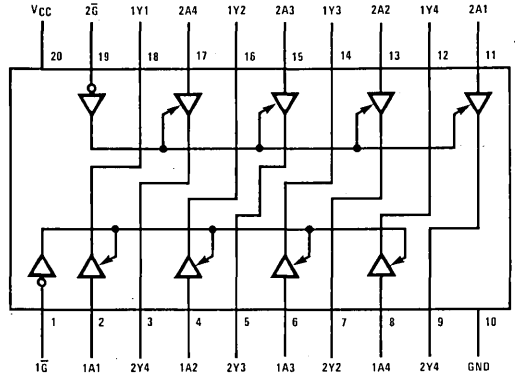
Connection Diagrams

(TOP VIEW)



MM74C240

(TOP VIEW)



MM74C244

National Semiconductor

MM54C373/MM74C373 TRI-STATE® Octal D-Type Latch
MM54C374/MM74C374 TRI-STATE® Octal D-Type Flip-Flop

General Description

The MM54C373/MM74C373, MM54C374/MM74C374 are integrated, complementary MOS (CMOS), 8-bit storage elements with TRI-STATE® outputs. These outputs have been specially designed to drive highly capacitive loads, such as one might find when driving a bus, and to have a fan-out of 1 when driving standard TTL. When a high logic level is applied to the OUTPUT DISABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54C373/MM74C373 is an 8-bit latch. When $\overline{\text{LATCH ENABLE}}$ is high the Q outputs will follow the D inputs. When $\overline{\text{LATCH ENABLE}}$ goes low, data at the D inputs, which meets the set-up and hold time requirements, will be retained at the outputs until $\overline{\text{LATCH ENABLE}}$ returns high again.

The MM54C374/MM74C374 is an 8-bit, D-type, positive-edge triggered flip-flop. Data at the D inputs, meeting the set-up and hold time requirements, is transferred to the Q outputs on positive-going transitions of the CLOCK input.

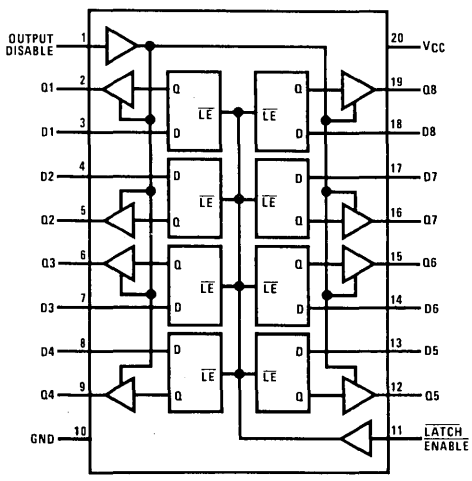
Both the MM54C373/MM74C373 and the MM54C374/MM74C374 are being assembled in 20-pin dual-in-line packages with 0.300" pin centers.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{CC} typ
- Low power consumption
- TTL compatibility — fan-out of 1 driving standard TTL
- Bus driving capability
- TRI-STATE outputs
- Eight storage elements in one package
- Single CLOCK/$\overline{\text{LATCH}}$ $\overline{\text{ENABLE}}$ and OUTPUT DISABLE control inputs
- 20-pin dual-in-line package with 0.300" centers takes half the board space of a 24-pin package

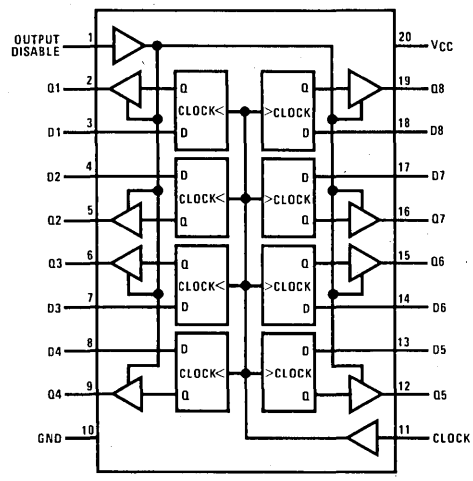
Connection Diagrams

MM54C373/MM74C373
Dual-In-Line Package



TOP VIEW

MM54C374/MM74C374
Dual-In-Line Package



TOP VIEW

Section 10

Physical Dimensions

10

National Semiconductor

Physical Dimensions

PACKAGES

Dual-In-Line Packages

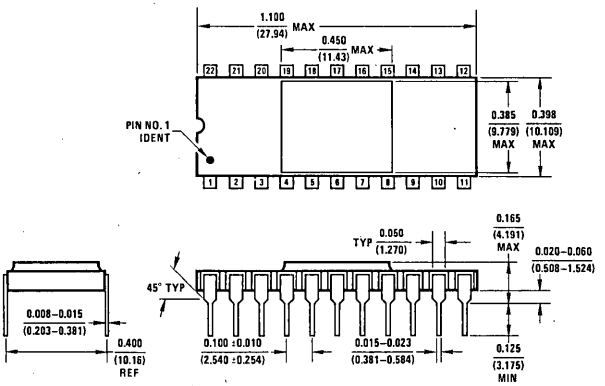
(N) Devices ordered with "N" suffix are supplied in molded dual-in-line package. Molding material is EPOXY B2, a highly reliable compound suitable for military as well as commercial temperature range applications. Lead material is Alloy 42 with a hot solder dipped surface to allow for ease of solderability.

(J) Devices ordered with the "J" suffix are supplied in a ceramic dual-in-line package. The body and lid of the package are made of ceramic. Hermeticity is accomplished through a high temperature sealing glass. Lead material is tin-plated kovar.

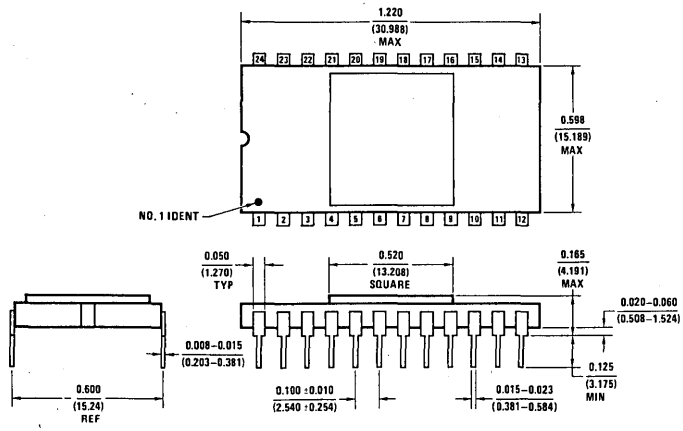
(D) Devices ordered with the "D" suffix are supplied in glass/metal dual-in-line package. The top and bottom of the package are gold-plated kovar. The side walls are glass, through which the leads extend forming a hermetic seal. The kovar leads may be either gold or tin-plated.

(Q) Devices ordered with the "Q" suffix are supplied in a glass/metal dual-in-line package with a round quartz window.

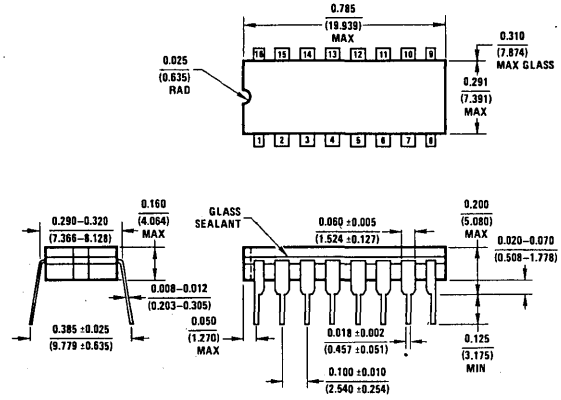
Note: All dimensions expressed as $\frac{\text{inches}}{\text{(millimeters)}}$



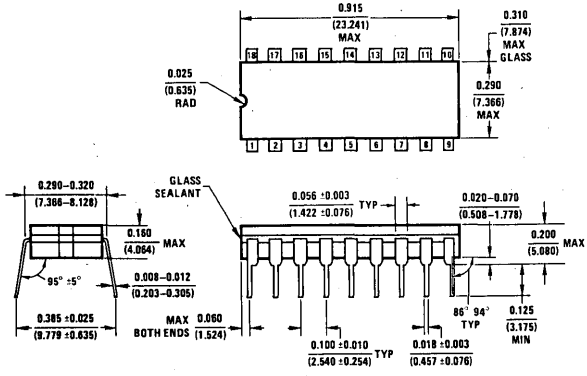
NS Package D22B
22-Lead Cavity DIP (D)



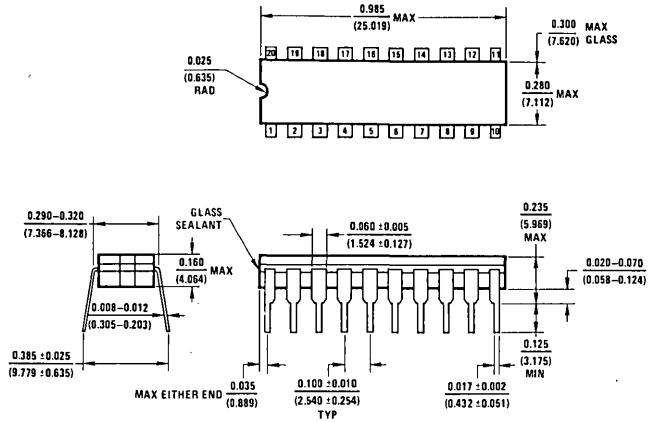
NS Package D24C
24-Lead Hermetic DIP (D)



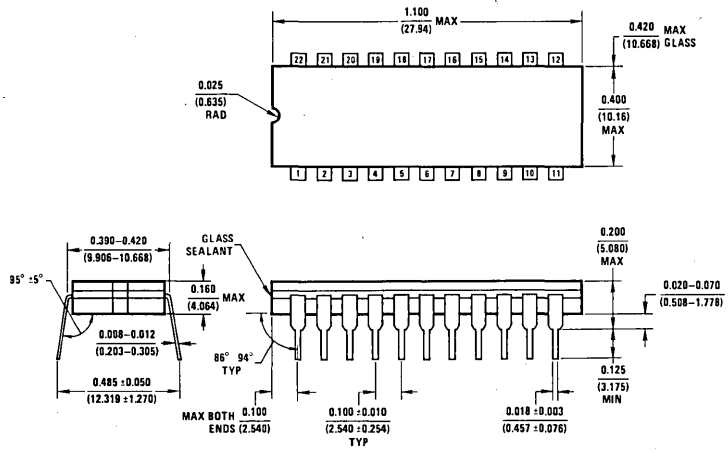
NS Package J16A
16-Lead Cavity DIP (J)



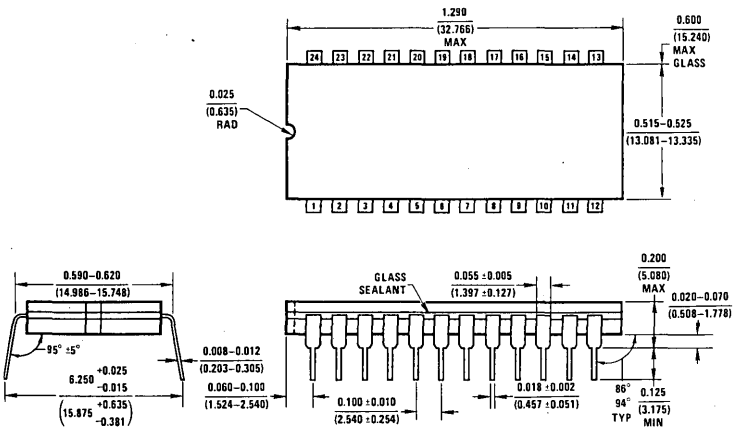
NS Package J18A
18-Lead Cavity DIP (J)



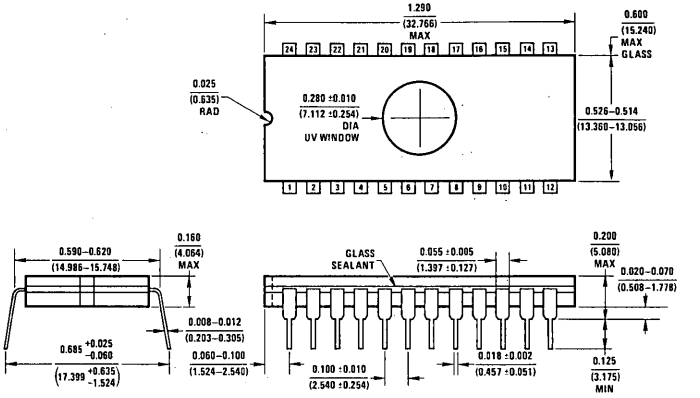
NS Package J20B
20-Lead Cavity DIP (J)



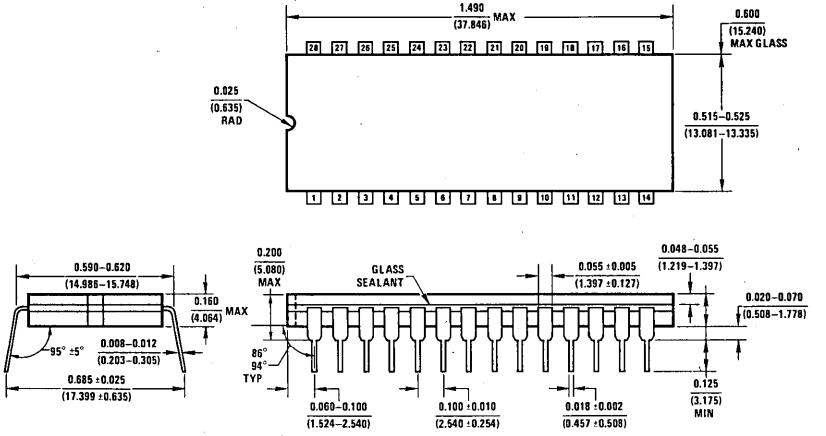
NS Package J22A
22-Lead Cavity DIP (J)



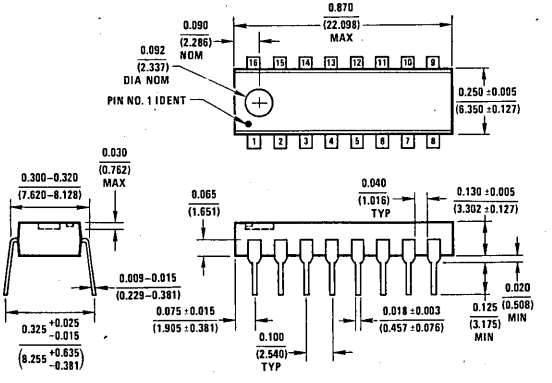
NS Package J24A
24-Lead Cavity DIP (J)



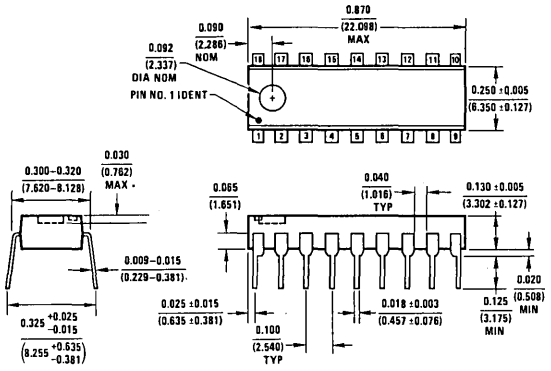
NS Package J24CQ
24-Lead UV Window Cavity DIP (J)



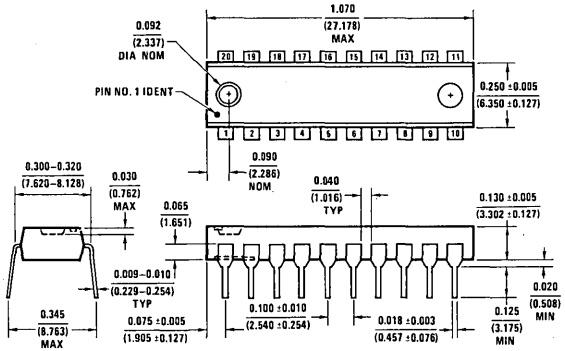
NS Package J28A
28-Lead Hermetic DIP (J)



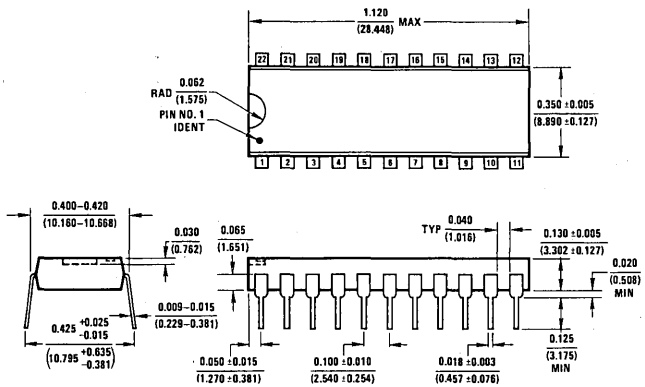
NS Package N16A
16-Lead Molded DIP (N)



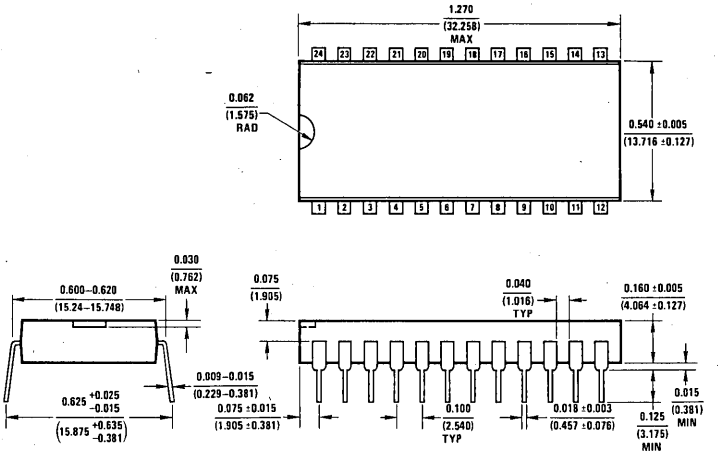
NS Package N18A
18-Lead Molded DIP (N)



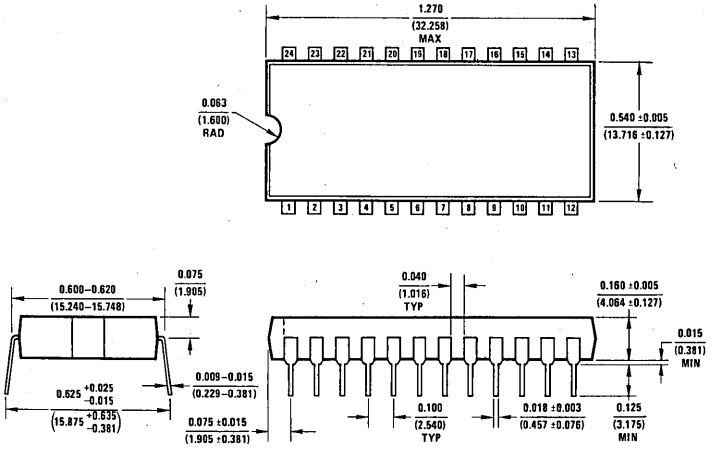
NS Package N20A
20-Lead Molded DIP (N)



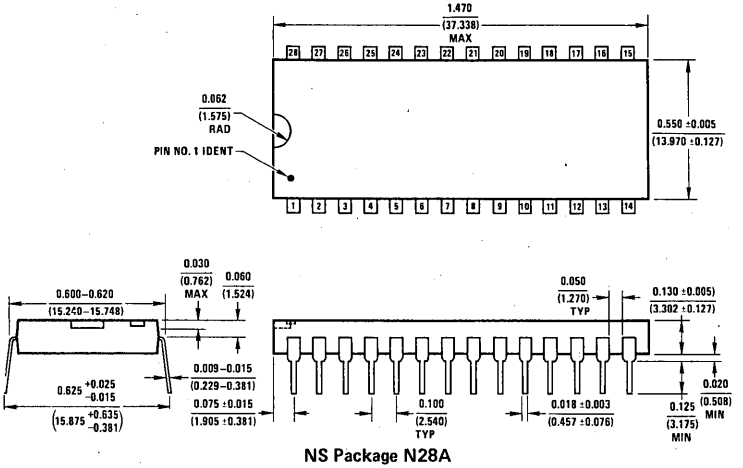
NS Package N22A
22-Lead Molded DIP (N)



NS Package N24A
24-Lead Molded DIP (N)



NS Package N24B
24-Lead Molded DIP (N)



NS Package N28A
28-Lead Molded DIP (N)

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, California 95051
Tel: (408) 737-5000
TWX: (910) 339-9240

National Semiconductor
District Sales Office
345 Wilson Avenue, Suite 404
Downsview, Ontario M3H 5W1
Canada
Tel: (416) 635-7260

Electronica NSC de Mexico SA
Helgel No. 153-204
Mexico 5 D.F. Mexico
Tel: (905) 531-1689, 531-0659

NS Electronics Do Brasil
Avada Brigadeiro Faira Lima 844
11 Andar Conjunto 1140
Jardim Paulistano
Sao Paulo, Brasil
Telex: 1121008 CABINE SAO PAULO

National Semiconductor GmbH
Eisenheimerstrasse 61/II
8000 Munchen 21
West Germany
Tel: (089/9) 576091
Telex: 522772

National Semiconductor (UK) Ltd.
301 Harpur Centre
Horne Lane
Bedford MK40 1TR
United Kingdom
Tel: 0234-47147
Telex: 826 209

National Semiconductor Benelux
Ave. Charles Quint 545
1080 Brussels
Belgium
Tel: (02) 4661807
Telex: 61007

National Semiconductor (UK) Ltd.
1, Bianco Lunos Alle
DK-1868 Copenhagen V
Denmark
Tel: (01) 213211
Telex: 15179

National Semiconductor
Expansion 10000
28, Rue de la Redoute
92260 Fontenay-aux-Roses
France
Tel: (01) 660-8140
Telex: 250956

National Semiconductor S.p.A.
Via Solferino 19
20121 Milano
Italy
Tel: (02) 345-2046/7/8/9
Telex 332835

National Semiconductor AB
Box 2016
12702 Skarholmen
Sweden
Tel: (08) 970190
Telex: 10731

National Semiconductor
Calle Nunez Morgado 9
Esc. Dcha. 1-A
Madrid 16
Spain
Tel: (01) 733-2954/733-2958
Telex: 46133

National Semiconductor Switzerland
Alte Winterthurerstrasse 53
Postfach 567
CH-8304 Wallisellen-Zurich
Tel: (01) 830-2727
Telex: 59000

NS Japan K. K.
POB4152 Shinjuku Center Building
1-25-1 Nishishinjuku, Shinjuku-ku
Tokyo 160, Japan
Tel: (03) 349-0811
TWX: 232-2015 NSCJ-J

National Semiconductor (Hong Kong) Ltd.
1st Floor
Cheung Kong Electronic Bldg.
4 Hing Yip Street
Kwun Tong
Kowloon, Hong Kong
Tel: 3-899235
Telex: 43866 NSEHK HX
Cable: NATSEMI HX

NS Electronics Pty. Ltd.
Cnr. Stud Rd. & Mtn. Highway
Bayswater, Victoria 3153
Australia
Tel: 03-729-6333
Telex: 32096

National Semiconductor (Pty.) Ltd.
9th Floor
Pub Building, Devonshire Wing
Somerset Road
Singapore 0923
Tel: 7379338/7379339
Telex: NAT SEMI RS 21402

National Semiconductor (Taiwan) Ltd.
P.O.Box 68-332 Taipei
3rd Flr. Apollo Bldg.No. 281-7
Chung Shiao E. Rd., Sec. 4
Taipei
Tel: 7310393-4, 7310465-6
Telex: 22837 NSTW
Cable: NSTW TAIPEI

National Semiconductor (Hong Kong) Lt.
Korea Liaison Office
6th Floor, Kunwon Bldg.
1-2 Mookjung-Dong
Choong-Ku, Seoul
C.P.O.Box 7941 Seoul
Tel: 267-9473
Telex: K24942

IM-CP20RRD50M30/Printed in U.S.A.