Series 32000

DB32016 Development Board User's Manual

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Series 32000™

DB32016 Development Board
User's Manual

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REVISION RECORD

REVISION	RELEASE DATE	SUMMARY OF CHANGES
A	03/84	First Release. DB16000A Development Board User's Manual Publication No. 420310111-001

PREFACE

This manual provides detailed information on using the DB16000A Development Board. It includes descriptions of the board hardware as well as providing set-up and operating procedures.

Reference Documents. The following documents support the DB16000 Development Board and NS16000 Family:

NS16000 Programmer's Reference Manual	(Pub. No. 420306565-001)
NS16000 Cross-Assembler Reference Manual	(Pub. No. 420306619-002)
NS16000 Pascal Language and Compiler Reference Manual	(Pub. No. 420306618-002)
NS16000 NSX16 Cross-Support Utilities Reference Manual	(Pub. No. 420306617-002)
NS16000 Development Board Monitor Reference Manual	(Pub. No. 420308221-002)
NS16000 NSX16 Operations Manual	(Pub. No. 424009011-002)
NS16000 Run-Time Support Library Reference Manual	(Pub. No. 420308038-002)
NS16000 Symbolic Debugger Reference Manual	(Pub. No. 420306676-002)
NS16000 Floating-Point Support Library Reference Manual	(Pub. No. 420308220-002)
NS16000 ISE/16: NS16032 and NS08032 In-System Emulators User's Manual	(Pub. No. 420306675-002)
NS16000 BLMX-16: Board Level Multi-Tasking Executive System Reference Manual	(Pub. No. 420308147-001)
NS16000 TDS: Tiny Development System	(Pub. No. 420306440-001)
NS16000 DB32000 Development Board User's Manual	(Pub. No. 420010144-001)
NS16000 GENIX Cross-Support Software Programmers Manual	
Volume 1	(Pub. No. 424010106-001)
Volume 2	(Pub. No. 424010106-002)
NS16000 GENIX Programmer's Manual	
Volume 1	(Pub. No. 424308225-001)
Volume 2	(Pub. No. 424308225-002)
NS16000 SYS16 System Manual	(Pub. No. 420308225-001)

The information contained in this manual is for reference only and is subject to change without notice.

To enhance product positioning, National Semiconductor has recently changed the NS16000 Family names to Series 32000 Family names. The DB16000A development board has been renumbered the DB32016 development board to coincide with these changes. Replace "NS16000 Family" and "DB16000A" with "Series 32000 Family" and "DB32016", respectively, wherever applicable. A revised manual, completely renamed, will be available at a later date.

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Chapter 1

INTRODUCTION AND OVERVIEW

1.1 MANUAL SCOPE AND ORGANIZATION

The DB16000A development board is a complete microcomputer system. It is designed to assist the user in evaluating NS16000 microprocessors, slave processors, and support chips in a variety of application environments. This manual details the extent of the DB16000A's flexibility, and the manner in which hardware options may be implemented.

In most cases, this manual should be used in conjunction with an appropriate software user's manual to gain a complete understanding of the DB16000A as a system. The DB16000A is factory-configured with TDS (Tiny Development System) software in on-board PROM; therefore, the TDS user's manual should be consulted for operating information once the hardware is properly configured.

The remaining sections of Chapter 1 contain a brief overview of the DB16000A's hardware capability, as well as physical, environmental, and electrical interconnect specifications.

Chapter 2, "Operating Configurations", describes the DB16000A's intended use as an evaluation/development tool. Variations in user mode configuration, 16K family mix, and MULTIBUS usage are explained.

Chapter 3, "Hardware Organization", explains the functional organization of DB16000A hardware. This chapter is intended for use in conjunction with schematics supplied with the DB16000A; however, the text alone is sufficient to gain a general understanding of the hardware implementation.

Chapter 4, "Program Interface", contains information necessary to operate DB16000A hardware under program control. The means of program access and manipulation of hardware is explained.

Chapter 5, "Hardware Options", describes how the DB16000A hardware functions may be altered.

1.2 PRODUCT DESCRIPTION

The following is a brief overview of DB16000A.

1.2.1 Features

- 10 MHz operation (DB16000A-110) or 6 MHz operation (DB16000A-006)
- CPU socket accepts either an NS16032 or NS08032 microprocessor (NS16032 supplied in factory configuration)
- Socket for NS16081 floating-point unit--extremely high speed floating-point arithmetic (NS16081 is installed in DB16000A-110)
- Socket for NS16082 memory management unit--demand-paged virtual memory management (NS16082 is installed in DB16000A-110)
- Socket for NS16202 interrupt controller unit--provides up to 16 levels of maskable, vectored interrupts (NS16202 is installed in DB16000A-110)
- NS16201 timing control unit--provides CPU and TTL-level clocks
- 128K bytes of on-board, dual-port dynamic RAM
- Dual-port RAM external address jumper selectable
- Four sockets for up to 96K bytes of 24/28-pin ROM or EPROM
- TDS16A (Tiny Development System) software in PROM
- One BLX expansion module connector for additional I/O capability
- 24 programmable, parallel I/O lines
- Two programmable synchronous/asynchronous RS232 compatible serial data ports
- Three programmable 16-bit timer/event counters
- MULTIBUS interface with multimaster capability
- MULTIBUS BCLK and CCLK meet MULTIBUS specifications regardless of CPU speed
- 24-bit addressing allowing access of up to 16M bytes of combined system memory and I/O

1.2.2 Functions

The DB16000A may be operated in either of two configurations:

- Stand-alone
- Host-assisted

In stand-alone mode, the factory-configured TDS on-board software can be used to edit, assemble, and debug small programs. The intent is to allow the user to explore the NS16000 instruction set.

In host-assisted mode, the DB16000A is used in conjunction with a larger host computer. The host, together with development software, is used to develop programs for execution on the DB16000A. In this case, the DB16000A functions as a native NS16000 execution/debug environment for the host-developed program. An appropriate monitor program replaces TDS, allowing the program to be downloaded and controlled by the host.

The DB16000A's flexibility is further enhanced by its MULTIBUS interface. In all user modes, additional MULTIBUS compatible boards can be used to expand the DB16000A's I/O capability.

Further, the DB16000A permits the user to selectively evaluate combinations of NS16000 family members from the following set:

- NS16032 32-bit CPU; 16-bit data bus
- NS08032 32-bit CPU; 8-bit data bus
- NS16082 MMU; memory management slave processor
- NS16081 FPU; floating-point slave processor
- NS16202 ICU; interrupt controller
- NS16201 TCU; timing control unit

Note that the NS16082 can not be used in conjunction with the NS08032.

1.2.3 Physical Description

The DB16000A (Figure 1-1) is a rectangular printed circuit assembly measuring 6.75 inches by 12 inches. The board is specifically designed for use in MULTIBUS compatible card cages. If a card cage is not used, the board may be placed on a nonconductive surface for operation.

Three physical features of the DB16000A are:

- Six connectors
- Three switches
- Four LED indicators

Connectors. Six connectors on the DB16000A provide interfaces to peripherals and the MULTIBUS interface. Three connectors (J1, J2, and J3) are found on the front edge of the assembly, two connectors (P1 and P2) are found on the rear edge of the assembly, and one connector J4 is positioned near the front edge of the assembly.

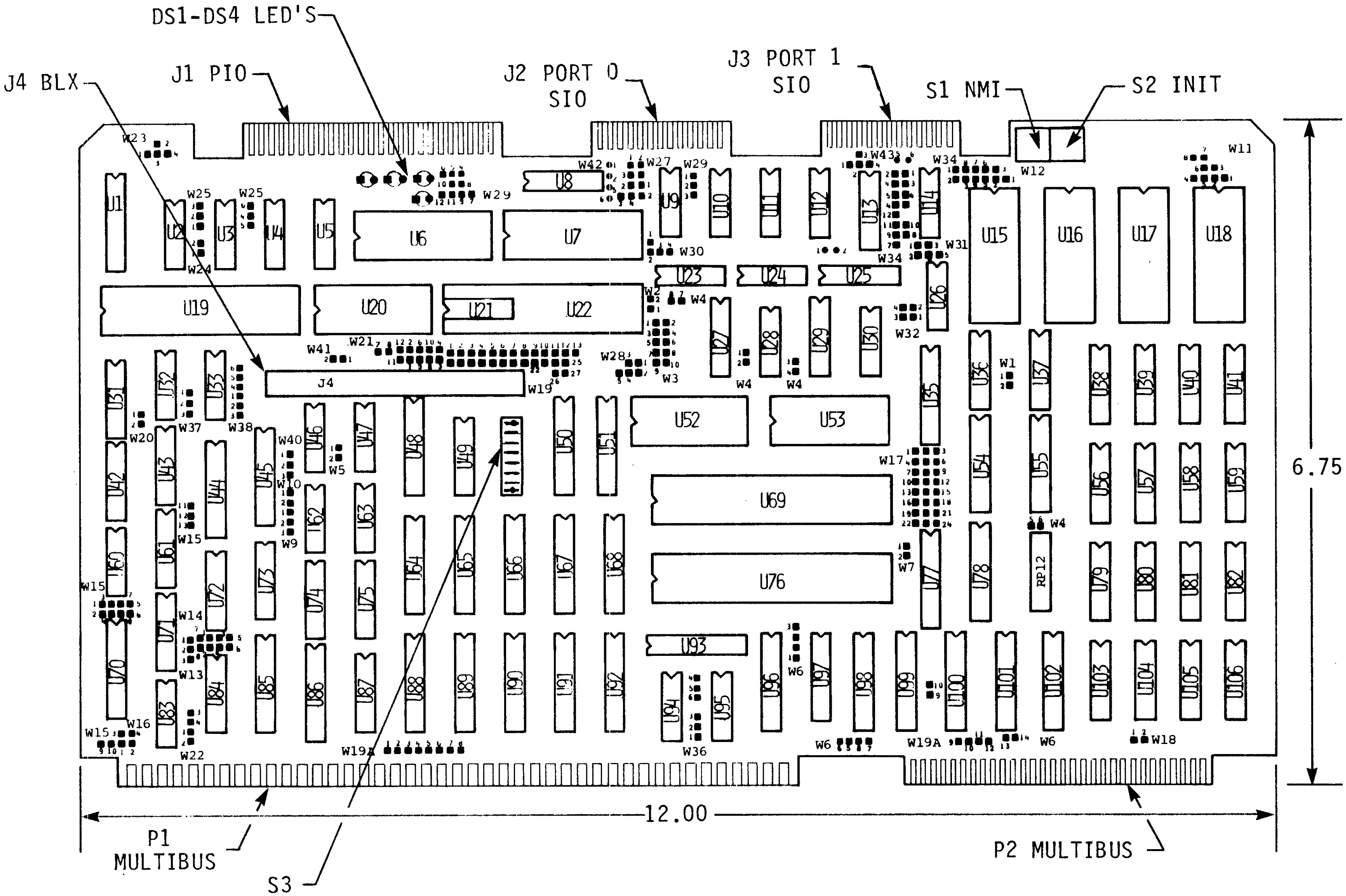

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Figure 1-1 DB16000A Topography

Connector J1 is a 50-pin pc tongue connector with 25 0.1-inch spaced contacts on each side of the board. The connector is dedicated for parallel I/O use. Note that all contacts (odd numbered) on the component side of the board are connected to ground. Therefore, a mating flat-cable assembly will have alternate conductors grounded, reducing noise coupling among adjacent signals.

Some vendors of mating connectors to J1 are:

- 3M #3415-0001
- AMP #88083-1

Connectors J2 and J3 are 26-pin pc tongue connectors with 13 0.1-inch spaced contacts on each side of the board. These connectors are dedicated for serial I/O (RS232C) use. The DB16000A is designed to permit the use of "flat cable" assemblies for J2 and J3 connection.

Some vendors of mating connectors to J2 and J3 are:

- 3M #3462-0001 CRIMP
- AMP #88106-1

Connector P1 is an 86-pin pc tongue connector with 43 0.156-inch spaced contacts on each side of the board. P1 is the principle means of connection to the MULTIBUS interface. In addition, all power for the DB16000A is provided through this connector.

Some vendors of mating connectors to P1 are:

- Viking #2KH43/9AMK12 (for soldered connections)
- Elfab #BW1562D43PBB (for wire wrap connections)

Connector P2 is a 60-pin pc tongue connector with 30 0.1-inch spaced contacts on each side of the board. P2 is the auxilliary bus connector, providing access to the upper MULTIBUS address bits and various DB16000A control signals.

Some vendors of mating connectors to P2 are:

- Elfab #BS1020A30PBB (for soldered connections)
- Viking #3KH30/9JNK (for wire wrap connections)

Connector J4 consists of a BLX (Board Level Expansion) connector. J4 permits installation of 8- or 16-bit expansion boards; e.g. National Semiconductor Corporation's BLX-351. The connector consists of a 36-pin field for 8-bit expansion modules, plus an additional 8-pin field for 16-bit capability. Refer to National Semiconductor Corporation's Board Level Computer products databook for further information on expansion boards.

<u>Switches</u>. Two pushbutton switches (S1 and S2), and one 8-position DIP switch (S3) are provided on the DB16000A.

S1, labeled NMI, introduces a nonmaskable interrupt to the DB16000A's CPU when pressed. S2, labeled INIT, resets the board when pressed. Both switches are located on the front edge of the board assembly.

S3 consists of eight SPST switches in a dual in-line package. S3 is utilized by firmware to indicate options invoked by the user; e.g. serial port baud rate. The switch is located near the center of the board.

Indicators. Four LED indicators (DS1 through DS4) are mounted near the front edge of the board assembly.

DS1 through DS3 are controlled by the content of a program addressed register. These are provided for use by the TDS power on confidence test program to indicate test status. They may also be used to indicate any other information the user desires.

DS4 is driven directly by a one-shot timer whose period is approximately 15 milliseconds. DS4 will light up whenever there is no memory or I/O access completed by the CPU within this period. This is useful for indicating a MULTIBUS timeout or malfunctioning CPU.

1.3 SPECIFICATIONS

1.3.1 Environment

The DB16000A is designed for operation in an office or laboratory environment. Avoid confining the DB16000A in a closed space, unless sufficient air flow is provided to ensure all components are operated within their specified temperature range.

- Temperature: Operating 0°C to 55°C
  Nonoperating -40°C to 75°C

- Humidity: 5% to 95% relative, noncondensing

- Altitude: Operating 15,000 ft.
  Nonoperating 25,000 ft.

1.3.2 Power Requirements

The DB16000A requires three regulated DC voltages for operation:

- +12 volt DC, ±10%, 50 mA maximum
- -12 volt DC, ±10%, 50 mA maximum
- +5 volt DC, ±5%, 7.5 A maximum

1.3.3 Interfaces

There are five interfaces provided in the DB16000A:

- Parallel I/O (J1)
- Serial I/O Port 0 (J2)
- Serial I/O Port 1 (J3)
- MULTIBUS I/O (P1 and P2)
- BLX (J4)

The following sections detail connector pinout and signal definitions for each of the interfaces.

Parallel I/O. A 24-line parallel interface provides a means of controlling I/O devices. The function of each line is defined under program control. Jumper options, as well as socketed interface transceivers, are provided for the purpose of altering the factory configuration.

The 24 interface lines are organized as three, 8-bit ports: Port A, Port B, and Port C.

Table 1-1 lists J1 pin numbers, bit assignment, interface element, signal direction, and termination for the factory configuration.

Serial I/O. The DB16000A serial interfaces are designed to provide a wide variety of synchronous and asynchronous, RS232C compatible communications. Jumper options are provided for the purpose of altering the configuration of each interface.

As configured by the factory, Port 0 (J2) is intended to connect to an RS232C compatible terminal, and is configured as DCE (Data Communication Equipment). Port 1 (J3) is configured as DTE (Data Terminal Equipment), and is intended for connection to a modem or host computer. Both interfaces are set for 9600 baud asynchronous communication.

Table 1-2 lists pinout, signal definition and direction for the factory configuration.

MULTIBUS I/O. The DB16000A incorporates a MULTIBUS interface, allowing the user to configure larger systems. Most often, the DB16000A would be used in conjunction with MULTIBUS compatible expansion RAM, disk controller, or serial controller boards. However there is no restriction, beyond MULTIBUS compliance.

TABLE 1-1 J1 PIO PIN/SIGNAL

PIN	SIGNAL	PIN	SIGNAL	INTERFACE	DIRECTION	TERMINATION
1	GND	2	Port B, bit 7	7437	OUT	NONE
3	GND	4	Port B, bit 6	7437	OUT	NONE
5	GND	6	Port B, bit 5	7437	OUT	NONE
7	GND	8	Port B, bit 4	7437	OUT	NONE
9	GND	10	Port B, bit 3	7437	OUT	NONE
11	GND	12	Port B, bit 2	7437	OUT	NONE
13	GND	14	Port B, bit 1	7437	OUT	NONE
15	GND	16	Port B, bit 0	7437	OUT	NONE
17	GND	18	Port C, bit 3	7437	OUT	NONE
19	GND	20	Port C, bit 2	7437	OUT	NONE
21	GND	22	Port C, bit 1	7437	OUT	NONE
23	GND	24	Port C, bit 0	7437	OUT	NONE
25	GND	26	Port C, bit 4	7437	OUT	NONE
27	GND	28	Port C, bit 5	7437	OUT	NONE
29	GND	30	Port C, bit 6	7437	OUT	NONE
31	GND	32	Port C, bit 7	7437	OUT	NONE
33	GND	34	Port A, bit 7	8303	IN/OUT	4.7K PU
35	GND	36	Port A, bit 6	8303	IN/OUT	4.7K PU
37	GND	38	Port A, bit 5	8303	IN/OUT	4.7K PU
39	GND	40	Port A, bit 4	8303	IN/OUT	4.7K PU
41	GND	42	Port A, bit 3	8303	IN/OUT	4.7K PU
43	GND	44	Port A, bit 2	8303	IN/OUT	4.7K PU
45	GND	46	Port A, bit 1	8303	IN/OUT	4.7K PU
47	GND	48	Port A, bit 0	8303	IN/OUT	4.7K PU
49	GND	50	No Connect			

TABLE 1-2 J2 AND J3 PIN/SIGNAL

RS232 PIN	J2/J3 PIN	SIGNAL NAME	FUNCTION	J2 (DCE) IN/OUT	J3 (DTE) IN/OUT
1	2	GND	Logic Ground	--	--
2	4	TXD	Transmit Data receive data	IN	OUT
3	6	RXD	Receive Data transmit data	OUT	IN
4	8	RTS	Request to Send	IN	OUT
5	10	CTS	Clear to Send	OUT	IN
data set ready 6	12	DSR	Data Set Ready	OUT	IN
7	14	GND	Logic Ground	--	--
carrier detect 8	16	--	--	--	--
9	18	--	--	--	--
10	20	--	--	--	--
11	22	+12	+12 VDC TTY Interface Power	NC	NC
12	24	--	--	--	--
13	26	SCTS	Secondary Clear to Send	NC	NC
14	1	--	--	--	--
15	3	TSET	Transmit Sig. Timing (DCE Source)	NC	NC
16	5	SRXD	Secondary Receive Data	NC	NC
17	7	RSET	Receive Sig. Timing (DCE Source)	NC	NC
18	9	--	--	--	--
19	11	--	--	--	--
20	13	DTR	Data Terminal Ready	IN	OUT
21	15	--	--	--	--
22	17	--	--	--	--
23	19	-12	-12 VDC TTY Interface Power	NC	NC
24	21	TSET	Transmit Sig. Timing (DTE Source)	NC	NC
25	23	+5	+5 VDC TTY Interface Power	NC	NC

The DB16000A's MULTIBUS compliance levels (refer to Intel MULTIBUS Specification, 9800683-04) are:

- Master--D16 M24 I16 V0 El; indicationg 8/16-bit data path, 24-bit memory address path, 8 or 16-bit I/O address path, and level or edge triggered non-bus vectored interrupts (if the NS16202 is installed)

- Slave--D16 M24; indicating 8/16-bit data path and 24-bit memory address path.

The user must be mindful of MULTIBUS compliance levels when constructing a MULTIBUS system. Compliance levels among boards in the system need not be the same. However, system bus transactions between any two boards must be in accordance with the lowest level of compliance. For example, a master with 8/16-bit data path may transact with a slave possessing an 8-bit data path. In this case, transactions are limited to 8-bit data.

Table 1-3 lists P1 pin numbers and signal names. Likewise, Table 1-4 lists P2 pin numbers and signal names. Table 1-5 defines P1 signals and Table 1-6 defines P2 signals.

NOTE: Most signals in P2 pertain to the DB16000A's CPU cluster. These signals are provided as reference only; the user is not advised to incorporate these signals in external circuitry.

BLX. The board level expansion connector is provided as an additional means of extending the DB16000A's I/O capability; e.g. additional serial or parallel interfaces may be added.

Table 1-7 lists the connector pinout and signal names for J4. Table 1-8 lists signal definitions.

1.4 RELATED DOCUMENTATION

The documents listed in the Preface of this manual may be helpful while using the DB16000A.

In addition, the user should have on hand any pertinent documentation for peripheral devices (e.g. printer or terminal and other MULTIBUS boards to be interfaced with DB16000A.

This manual makes no attempt to instruct the user in proper design of NS16000-based hardware or software.

TABLE 1-3 P1 PIN/SIGNAL

FUNCTION	(COMPONENT SIDE)			(SOLDER SIDE)		
	PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
POWER SUPPLIES	1	GND	Signal GND	2	GND	Signal GND
	3	+5V	+5 VDC	4	+5V	+5 VDC
	5	+5V	+5 VDC	6	+5V	+5 VDC
	7	+12V	+12 VDC	8	+12V	+12 VDC
	9			10		
	11	GND	Signal GND	12	GND	Signal GND
BUS CONTROLS	13	BCLK/ NC	Bus Clock	14	INIT/ NC	Initialize
	15	BPRN/ GND	Bus Priority In	16	BPRO/ N.C	Bus Priority Out
	17	BUSY/ NC	Bus Busy	18	BREQ/ N.C	Bus Request
	19	MRDC/ RD NC	Memory Read Command	20	MWTC/ WR NC	Memory Write Command — RD × WR × AL
	21	IORC/	I/O Read Command	22	IOWC/	I/O Write Command
	23	XACK/	Transfer Acknowledge	24	INH1/	Inhibit 1 Disable RAM
BUS CONTROLS AND ADDRESS	25	LOCK/ NC	Bus Lock	26	NC	
	27	BHEN/ (HBE)	Byte High Enable	28	AD~~10~~ 16/	Address Bus
	29	CBRQ/ +5	Common Bus Request	30	AD~~11~~ 17/	
	31	CCLK/	Constant Clk	32	AD12/ NC	
	33	NC		34	AD13/ NC	
T.D. output INTERRUPTS	35	INT6/	Parallel Interrupt Requests	36	INT7/	Parallel Interrupt Requests
	37	INT4/		38	INT5/	
ADC	39	INT2/		40	INT3/	
	41	INT0/ KYB		42	INT1/	

CLK for 8253 Timers (ext) connected to pin 7 W21.

9/3/87 This was changed to pin 11 W21 (123 KHz)

TABLE 1-3 (Cont.)

FUNCTION	(COMPONENT SIDE)			(SOLDER SIDE)		
	PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
ADDRESS	43	ADR~~E~~/14	Address Bus	44	ADR~~F~~/15	Address Bus
	45	ADR~~C~~/12		46	ADR~~D~~/13	
	47	ADR~~A~~/10		48	ADR~~B~~/11	
	49	ADR8/		50	ADR9/	
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
DATA	59	DAT~~E~~/14	Data Bus	60	DAT~~F~~/15	Data Bus
	61	DAT~~C~~/12		62	DAT~~D~~/13	
	63	DAT~~A~~/10		64	DAT~~B~~/11	
	65	DAT8/		66	DAT9/	
	67	DAT6/		68	DAT7/	
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
POWER SUPPLIES	75	GND	Signal GND	76	GND	Signal GND
	77			78		
	79	-12V	-12 VDC	80	-12V	-12 VDC
	81	+5V	+5 VDC	82	+5V	+5 VDC
	83	+5V	+5 VDC	84	+5V	+5 VDC
	85	GND	Signal GND	86	GND	Signal GND

TABLE 1-4 P2 PIN/SIGNAL

PIN	(COMPONENT SIDE)		(SOLDER SIDE)		
	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
1	GND	Ground	2	GND	Ground
3	ECLK	External Clock	4		
5			6		
7	MMUI/	MMU Interrupt Out	8		
9	IRQA	Interrupt Input	10	IRQB	Interrupt Input
11	IRQC	Interrupt Input	12	IRQD	Interrupt Input
13	IRQE	Interrupt Input	14	IRQF	Interrupt Input
15	PFS/	Prog Flow Status	16	ILO/	Interlocked Out
17	ENMI/	External NMI	18	UNS	User/Not Supr.
19	RD/	Read Strobe	20	WR/	Write Strobe
21	DBE/	Data Buffer Enable	22	DDIN/	Data Direction
23			24		
25	EWAIT4/	Wait 4 Request	26	EWAIT8/	Wait 8 Request
27	EWAIT1/	Wait 1 Request	28	EWAIT2/	Wait 2 Request
29	BTMO	Bus Time Out	30	ECWAIT/	Ext. Cont. Wait
31	EPER/	Peripheral Input	32	PAV/	Address Strobe
33	ERST/	External Reset	34	EHOLD/	Hold Request
35	HOLDA/	Hold Acknowledge	36		
37	ST2	Status Bit 2	38	ST3	Status Bit 3
39	ST0	Status Bit 0	40	ST1	Status Bit 1
41			42		
43			44		
45			46		
47			48		
49			50		
51			52		
53	A24	Physical Address	54		
55	ADR16/	Address Bus	56	ADR17/	Address Bus
57	ADR14/	Address Bus	58	ADR15/	Address Bus
59			60		

Notes: 1. All odd-numbered pins (1.3.5, etc.) are on component side of the board. Pin 1 is the left-most pin when viewed from the component side of the board with the extractors at the top.

2. Cable connector numbering convention may not agree with connector numbering convention.

TABLE 1-5 P1 SIGNAL DEFINITION

SIGNAL	FUNCTIONAL DESCRIPTION
ADR0/-ADRF/, ADR10/-ADR13/	Address. These 20 lines transmit the memory location or I/O port to be accessed. AD13/ is the most significant address bit. Note that additonal address lines are available on P2.
BCLK/	Bus Clock. Used to synchronize the bus contention logic on all bus masters. When generated by the DB16000A board, BCLK/ has a period of 108.5 nanoseconds (9.21 MHz) with a 50 percent duty cycle.
BHEN/	Byte High Enable. Used to select the upper byte (bits 8 through F) of a 16-bit word. The signal is functional only in systems that incorporate 16-bit memory and I/O devices.
BPRN/	Bus Priority In. Indicates to a particular bus master that no higher priority master is requesting use of the bus. BPRN/ is synchronized with BCLK/.
BPRO/	Bus Priority Out. In serial (daisy chain) priority resolution schemes, BPRO/ must be connected to the BPRN/ input of the bus master with the next lower bus priority.
BREQ/	Bus Request. In parallel priority resolution schemes, BREQ/ indicates that a particular bus master requires control of the bus for one or more data transfers. BREQ/ is synchronized with BCLK/.
BUSY/	Bus Busy. Indicates that the bus is in use and prevents all other bus masters from gaining control of the bus. BUSY/ is synchronized with BCLK/.
CBRQ/	Common Bus Request. Indicates that a bus master wishes control of the bus but does not presently have control. As soon as control of the bus is obtained, the requesting bus controller releases the CBRQ/ signal.
CCLK/	Constant Clock. Provides a clock signal of constant frequency for use by other system modules. When generated by the DB16000A board, CCLK/ has a period of 108.5 nanoseconds (9.21 MHz) with a 50 percent duty cycle.

TABLE 1-5 (Cont.)

SIGNAL	FUNCTIONAL DESCRIPTION
DAT0/-DATF/	Data. These 16 bidirectional data lines transmit and receive data to and from the addressed memory location or I/O port. DATF/ is the most-significant bit.
INH1/	Inhibit RAM. For system application, allows DB16000A board dual-port RAM addresses to be overlaid by another RAM in the system.
INIT/	Initialize. Resets the entire system to a known internal state.
IORC/	I/O Read. Indicates that the address of an I/O port is on the system bus interface address lines and that the output of that port is to be read (placed) onto the system bus interface data lines.
IOWC/	I/O Write. Indicates that the address of an I/O port is on the system bus interface data lines are to be accepted on the addressed port.
LOCK/	LOCK. When a system bus master accesses the on-board dual port RAM and activates the LOCK/ signal, the on-board CPU is locked out of the dual port RAM until the LOCK/ signal is removed by the system master. LOCK/ can be enabled onto the system bus interface to perform the same function on another dual ported RAM board.
MRDC/	Memory Read Command. Indicates that the address of a memory location is on the system bus interface address lines and that the contents of that location are to be read (placed) on the system bus interface data lines.
MWTC/	Memory Write Command. Indicates that the address of a memory location is on the system bus interface address lines and that the contents of the system bus interface data lines are to be written into that location.

TABLE 1-5 (Cont.)

SIGNAL	FUNCTIONAL DESCRIPTION
XACK/	Transfer Acknowledge. Indicates to the bus master that the read or write operation is completed by the generating device and that valid data is available on the system bus interface.
INT0/-INT7/	Interrupt Requests. Interrupts are requested by activating one of the eight interrupt request lines. INT0/ has the highest priority and INT7/ has the lowest priority.

TABLE 1-6 P2 SIGNAL DEFINITION

SIGNAL	FUNCTIONAL DESCRIPTION
ECLK	External Clock. External clock input to the NS16201 TCU when the on-board oscillator is not used.
MMUI/	MMU Interrupt Output. Active low interrupt output from the MMU that indicates a break condition has occurred.
IRQA-IRQF	Interrupt Requests. Additional interrupt request inputs to the NS16202. Jumper enabled.
PFS/	Program Flow Status. Active low signal from the CPU that indicates the beginning of an instruction execution.
ILO/	Interlock Output. Active low signal from the CPU that indicates an interlocked set bit or clear bit instruction for multiprocessor semaphore primitives has been executed.
ENMI/	External NMI. External input to generate a nonmaskable interrupt. Pulled high (disabled) by a pull-up resistor when left floating.
UNS	User Not Supervisor Mode. Output from CPU. High indicates User mode, low indicates Supervisor mode.
RD/	Read Strobe. Active low read strobe from TCU.
WR/	Write Strobe. Active low write strobe from TCU.
DBE/	Data Buffer Enable. Active low output from the TCU that is used to enable bidirectional data buffers.
DDIN/	Data Direction In. Active low output from the CPU that indicates the direction of data flow during a data transfer.
EWAIT1,2,4,8/	External Wait N Inputs. These inputs allow from 0 to 15 wait states to be specified. They are binarily weighted (as their names imply), thus if EWAIT4/ and EWAIT1/ are active (low), then five wait states will be inserted.

TABLE 1-6 (Cont.)

SIGNAL	FUNCTIONAL DESCRIPTION
BTMO	Bus Time Out. Indicates more than 15 milliseconds wait to memory or I/O acknowledgement (XACK/).
ECWAIT/	External Continuous Wait. This active low TCU input causes a cycle hold or continuous wait when asserted.
EPER/	External Peripheral Cycle. Active low input to TCU to cause a peripheral bus cycle.
PAV/	Physical Address Strobe. Active low output used to indicate address is valid. If an MMU is installed, this signal will come from the MMU. If no MMU is present, the signal is ADS/ from the CPU.
ERST/	External Reset. Active low input to cause a system reset.
EHOLD/	External Hold. Active low input to the CPU and MMU to cause a processor hold.
HOLDA/	Hold Acknowledge. Active low output to acknowledge a hold cycle.
ST0-ST3	Status Output Bits. Status outputs from the CPU that indicate the type of bus cycle.
A24	Physical Address 24. Most significant physical address bit, valid only when MMU installed.
ADR14/-ADR17/	Address. The upper address I/O signals provide the highest four address bits in a 24-bit addressing system. The signals are used to access up to 16 megabytes of memory space, when required.

TABLE 1-7 J4 BLX PIN/SIGNAL

PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
1	+12V	+12 Volts	2	-12V	-12 Volts
3	GND	Ground	4	+5V	+5 Volts
5	RESET	Module Reset	6	MCLK	Module Clock
7	MA3	Address Bit 3	8		Reserved
9	MA2	Address Bit 2	10		Reserved
11	MA1	Address Bit 1	12	MINTR1	Module Interrupt 1
13	IOWRT/	I/O Write Command	14	MINTR0	Module Interrupt 0
15	IORD/	I/O Read Command	16	MWAIT/	Wait-State Request
17	GND	Ground	18	+5V	+5 volts
19	MD7	Module Data Bit 7	20	MCS1/	Module Chip Select
21	MD6	Module Data Bit 6	22	MCS0/	Module Chip Select
23	MD5	Module Data Bit 5	24		Reserved
25	MD4	Module Data Bit 4	26		Reserved
27	MD3	Module Data Bit 3	28	OPT1	Option Line 1
29	MD2	Module Data Bit 2	30	OPT0	Option Line 0
31	MD1	Module Data Bit 1	32		Reserved
33	MD0	Module Data Bit 0	34		Reserved
35	GND	Ground	36	+5V	+5 volts
37	MDE	Module Data Bit E	38	MDF	Module Data Bit F
39	MDC	Module Data Bit C	40	MDD	Module Data Bit D
41	MDA	Module Data Bit A	42	MDB	Module Data Bit B
43	MD8	Module Data Bit 8	44	MD9	Module Data Bit 9

NOTE: With an NS16032 16-bit data bus CPU installed, either 8-bit or 16-bit BLX boards can be installed. If an NS06032 8-bit data bus CPU is installed, only 8-bit and not 16-bit BLX boards can be used.

Note A23 must be set to enable data buffers

TABLE 1-8 BLX SIGNAL DEFINITION

SIGNAL	FUNCTIONAL DESCRIPTION
IORD/	BLX READ Command. Commands the BLX board to perform the READ operation.
IOWRT/	BLX WRITE Command. Commands the BLX board to perform the WRITE operation.
RESET	BLX RESET Signal. Initializes the BLX board to a known internal state.
MCS0/	BLX Chip Select. Selects even I/O addresses from C00060 to C0006EH for either 8-bit or 16-bit devices of the J4 BLX connector.
MCS1/	Chip Select. Selects even I/O addresses from C00070 to C0007EH (for 8-bit devices only) on the J4 BLX connector, selects odd I/O addresses from C00061 to C0006FH (for a 16-bit device) on the J4 BLX connector.
MA1, MA2, MA3	Least Three Bits of the I/O Address. Used on conjunction with the chip select and command lines.
MINTR0, MINTR1	Two interrupt request lines from the BLX boards to the DB16000A board interrupt matrix.
MWAIT/	BLX Wait-State Request to the CPU. Causes DB16000A board to execute wait states until the BLX board is ready to respond.
MCLK	9.21-MHz timing reference from the DB16000A board for the BLX board.
OPT0, OPT1	Optional Use Lines. May be used for additional interrupt request lines.
MD0-MDF	16 bidirectional data lines.

Chapter 2

OPERATING CONFIGURATIONS

2.1 INTRODUCTION

The DB16000A offers the user a wide variety of operating configurations. There are three, relatively independent areas of flexibility:

- Stand-alone or host-assisted development. Variations are termed "user modes" and are discussed in Section 2.3

- NS16000 Family mix. Permissible combinations of family members are discussed in Section 2.4

- MULTIBUS systems. Information helpful to a system designer is contained in Section 2.5

Unpacking, inspection, and initial checkout procedures are detailed in Section 2.2.

2.2 UNPACKING, INSPECTION, AND INITIAL CHECKOUT

The DB16000A is shipped from the factory with the following materials:

- DB16000A Development Board User's Manual
- TDS (Tiny Development System) User's Manual
- Schematics
- Two RS232 cable sets
- Warranty information

The DB16000A is shipped in an anti-static bag. The user is advised to store the board in this bag to reduce the likelihood of damage to components from static discharge.

The user should examine the DB16000A for evidence of damage during shipment. Socketed components should be firmly seated. Jumper option pins should not touch adjacent pins or components. Any indication of damage must be noted by both the recipient and the carrier. All damage claims should be promptly filed with the carrier's representative.

The DB16000A is shipped with automatic, power-on confidence test software, residing with the TDS software in PROM. This permits straightforward initial checkout. The user is advised to perform this checkout, prior to altering the DB16000A's factory configuration.

The DB16000A is factory configured for stand-alone operation. The following is a checkout procedure for the DB16000A. This procedure assumes no configuration changes have been made.

Checkout Procedure:

1. Referring to Section 1.3.2 the user should first select power supplies of suitable current capacity and regulation. Power is applied to the DB16000A via the P1 connector. The user may choose to insert the DB16000A into a MULTIBUS compatible backplane or wire a compatible connector (see Section 1.2.3) for power delivery. If the latter option is chosen, consult Table 1-3 for pin number information.

WARNING

Incorrect voltage polarity will damage the DB16000A

2. Once power supply connections are made and verified, the DB16000A can be powered on. An automatic power-on reset circuit will initialize the circuity, and the board will attempt to execute the confidence test routines. All four LED indicators (DS1 through DS4) should be extinguished after 15 seconds, indicating the test found no errors.

3. If any LED remains lighted, verify the power supply voltages are within regulation. If necessary, readjust the voltage levels and/or current limits. Cycle the supplies off, then on, and observe the LEDs.

4. If LED failure indications persist, consult Appendix A for analysis information.

2.3 USER MODES

The DB16000A can operate stand-alone, with no assistance from a host computer system. Optionally, the board can be operated in conjunction with a host, taking advantage of more powerful software development tools and I/O capabilities.

Figure 2-1 represents the most common variations in user modes.

2.3.1 Stand-Alone Mode (Factory Configuration)

The stand-alone user mode (see Figure 2-1) is the most simplistic, requiring the least additional equipment. In this case, only an RS232C compatible terminal and power supplies for the DB16000A are required to achieve effective operation.

1. STAND-ALONE MODE

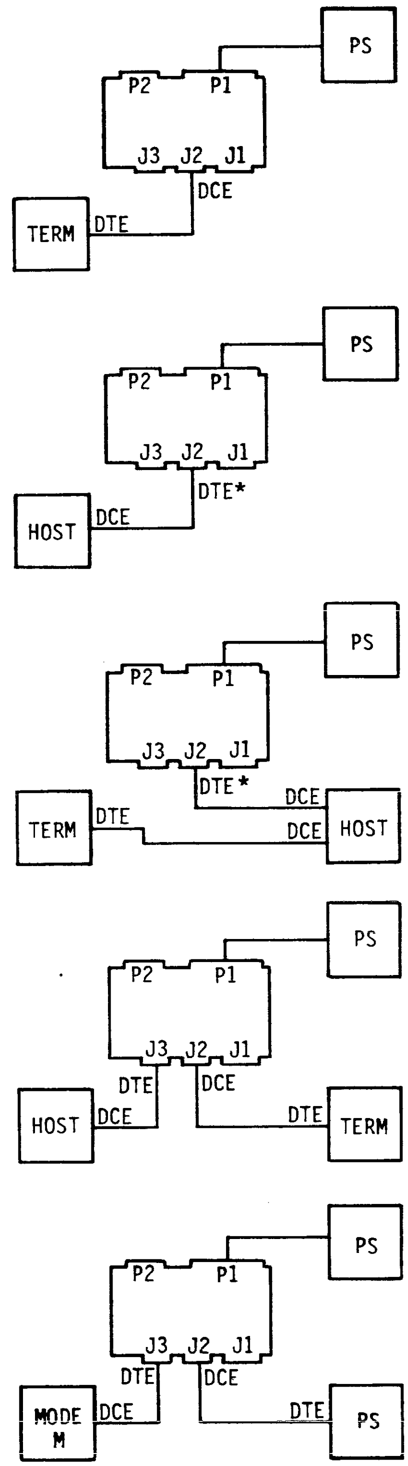
2. HOST-ASSISTED MODES

a) STAND-ASIDE, SINGLE-USER HOST (eg.SPX II)

b) STAND-ASIDE MULTIUSER HOST

c) TRANSPARENT, LOCAL HOST

d) TRANSPARENT, REMOTE HOST



*REQUIRES RECONFIGURATION

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Figure 2-1 DB16000A User Modes

TDS16A (Tiny Development System) software is supplied in on-board PROM to support this user mode. TDS is used to edit, assemble, and execute small assembly language programs. In addition, TDS can control the DB16000A's on-board I/O to provide cassette and printer interfaces; making the DB16000A a light duty development vehicle. For a full description of TDS capabilities, consult the TDS User's Manual.

Stand-Alone Requirements and Setup. The following items are required for stand-alone operation:

- DB16000A with TDS16A PROM based software installed
- RS232 cable set (supplied)
- RS232 compatible terminal and documentation

It is assumed the user has already performed power supply connection and board checkout procedures, as described in Section 2.2.

1. Terminal Connection (see Figures 2-2 and 2-3). The DB16000A's J2 connector is configured as DCE. This should allow simple connection to any RS232C compatible terminal. Using either of the two RS232 cable sets supplied with the DB16000A, perform the following:

   - Each cable set consists of two cables; one with a 26-pin card edge connector and a 25-pin RS232 female connector. Identify this cable and connect it to J2 (as shown in Figure 2-2).

   - Connect the remaining end of the cable to the terminal's RS232 connector. If the terminal connector is not male, it will be necessary to install the cable set's remaining male-to-male RS232 cable (as shown in Figure 2-3).

2. Terminal Configuration Once the terminal is properly cabled to the DB16000A, communication can be verified. Variations of baud rate settings and RS232C handshake signal usage by the terminal may require some reconfiguration of the DB16000A.

   First, try it without reconfiguration. Assuming power-on confidence tests passed, the TDS16A software will transmit its banner to the terminal screen each time the DB16000A is powered on or manually reset.

   If no characters appear on the screen, it may be necessary to loop back the RTS/CTS and DSR/DTR RS232 handshake signals at the J2 connector. The DB16000A is factory-configured to expect these signals to be utilized by the terminal. If the terminal does not support these signals, consult Section 5.2.3 or J2 (Port 0) optioning instructions.

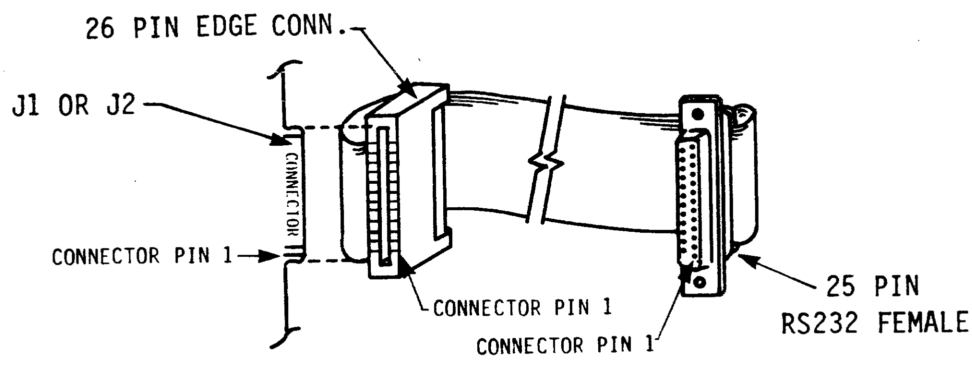

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Figure 2-2 Serial Cable For Edge Connector

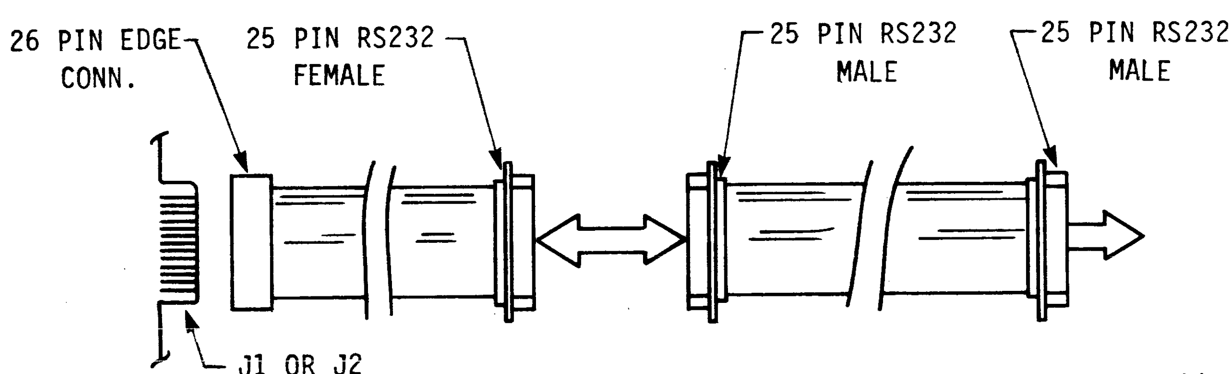

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Figure 2-3 Edge Connector Using Male-to-Male Cable

If garbled characters appear on the screen, it may be necessary to alter the DB16000A's baud rate. The DB16000A is factory-configured to support 9600 baud rate communication at Port 0. If the terminal cannot support this baud rate, consult Section 5.2.3 for instructions to alter the Port 0 baud rate.

Once the TDS16A banner properly appears on the terminal screen, equipment setup is completed for stand-alone mode. The user should now procede to the Initialization section in the TDS16 User's Manual for information on program initialization.

2.3.2 Host-Assisted Modes

Referring to Figure 2-1, the DB16000A can be connected to another computer system or host. In this case, the user first develops NS16000 software on the host system, then uses RS232 communication to download the software to the DB16000A. The DB16000A functions as a means of executing and debugging the software in a native environment.

Several development software packages are available for use in generating NS16000 user programs. Among them are:

- NSX16 for SPXII and VAX/VMS environments
- GENIX Cross-Support for machines executing the GENIX™ operating system

Host-assisted modes require the TDS16A PROMs to be replaced by a PROM-based monitor program compatible to the host development software. Monitor software is provided with both NSX16 and GENIX cross-support. The monitor provides:

- A terminal handler, to control RS232 communications
- Run-time environment, to permit execution of downloaded programs
- Debugger execute module, to facilitate operation with the host's symbolic debugger software

The basic host-assisted modes are stand-aside and transparent. The terms stand-aside and transparent may be visualized by observing the communication configuration in each mode (see Figure 2-1).

In transparent mode, the user's communication with the host is conducted through the DB16000A; the DB16000A is transparent to the user. An advantage is that a single RS232 port on the host computer will support both the user's terminal, and the DB16000A.

In stand-aside mode, the user communicates directly with the host while the DB16000A "stands aside". This mode is useful when the DB16000A is connected to single-user hosts, notably STARPLEX II™. Optionally, stand-aside operation is possible with multi-user hosts, where two RS232 ports are available.

Stand-Aside Requirements and Setup. It is assumed the user has already performed power supply connection and initial checkout procedures as described in Section 2.2.

The following items are required for stand-aside operation:

- DB16000A
- RS232 cable set (supplied)
- Monitor software in PROMs
- RS232 port on host computer

Monitor software must be compatible with the host development software package.

Determine the port baud rate, whether the host port is DTE or DCE, and whether or not RTS/CTS and DSR/DTR signals are used before connecting the DB16000A. Test host port operation beforehand, as well.

1. Monitor PROM Installation. Be certain power is off when performing this sequence.

    - Remove and set aside the TDS16A PROM set. TDS16A resides in two 27128 PROMs, located in U15 and U18.

    - Insert the monitor PROMs in U15 and U18 following instructions provided with the monitor PROMs.

    NOTE: Be sure that the monitor installation procedure supplied is appropriate for DB16000A. If the procedure was written for the earlier DB16000 board, refer to Section 5.2.2 for configuration instructions.

    If no instructions are supplied with the monitor PROM's, the user must ascertain the following:

    - Lower Bank (U15 and U18)
      PROM capacity and type (2716, 2732, etc.)
      PROM access time, maximum

    - Upper Bank (U16 and U17), if any
      PROM capacity and type
      PROM access time, maximum
      Upper bank starting address

    Then refer to Section 5.2.2 to configure the DB16000A to support the PROMs.

2. Port Connection (see Figure 2-1). Monitor software designed by National Semiconductor anticipates that the host is connected to Port 0 (J2), for stand-aside mode. Connection is straightforward, using either of the two cable sets supplied with DB16000A. Connections are made in the following manner:

   - Locate the cable with the 26-pin card edge connector. Connect the cable as shown in Figure 2-2.

   - Connect the remaining end of the cable to the host port. If the host port connector is not male, it will be necessary to install the cable set's remaining male-to-male cable, as shown in Figure 2-3.

3. Port Configuration. Consult the host documentation. Is the host port DTE or DCE? Most host system RS232 ports are configured as DCE (Data Communication Equipment). The DB16000A factory configuration for Port 0 (J2) is also DCE. Therefore, Port 0 should be reconfigured as DTE to be compatible with the host's port; one port must be DTE, the other DCE, to avoid use of odd cable arrangements. The procedure to convert Port 0 to DTE is explained in Section 5.2.3.

   Determine whether the host port uses RTS/CTS and DSR/DTR RS232 handshake signals. The DB16000A is factory-configured to expect these signals. If the host does not support them, it will be necessary to reconfigure Port 0. Consult Section 5.2.3 for instructions to "loop back" RTS/CTS and DSR/DTR.

   Next, determine the host port's baud rate. The DB16000A is factory-configured for 9600 baud communication rate. If the host cannot support this speed, it will be necessary to reconfigure Port 0 baud rate. Refer to Section 5.2.3 for instructions.

   Finally, test the total configuration. Load and invoke the host's software development package. Activate the program which communicates with the DB16000A, usually the symbolic debugger. Power on the DB16000A. At this point, refer to the debugger's command set, and attempt communication. If no communication is possible, double check the DTE vs. DCE arrangements, as well as the handshake signal usage. If communication is garbled, check the baud rate.

<u>Transparent Requirements and Setup</u>. It is assumed the user has already performed power supply connection and initial checkout procedures as described in Section 2.2.

The following items are required for transparent operation:

- DB16000A
- Two RS232 cable sets (supplied)

- Monitor software in PROMs
- RS232 port on host computer
- RS232 compatible terminal and documentation

NOTE: The user is reminded that monitor software must be compatible with the host development software package.

Ascertain the exact configuration of the host's RS232 port. Determine whether the port is DTE or DCE, whether or not RTS/CTS and DSR/DTR signals are used, and the baud rate. This information will be helpful in achieving proper communication between the host and DB16000A. Further, it is advised to test the host port before attempting connection to the DB16000A.

1. Monitor PROM Installation. Be certain power is not applied to DB16000A while performing this sequence.

   - Remove and set aside the TDS16A PROM set. TDS16A resides in two 27128 PROMs, located in U15 and U18.

   - Following instructions provided with the monitor PROMs, insert the PROMs in U15 and U18.

   NOTE: Be sure that the monitor installation procedure supplied is appropriate for DB16000A. If the procedure was written for the earlier DB16000 board, refer to Section 5.2.2 for configuration instructions.

   If no instructions are supplied with the monitor PROMs, the user must ascertain the following:

   - Lower Bank (U15 and U18)
     PROM capacity and type (2716, 2732, etc.)
     PROM access time, maximum

   - Upper Bank (U16 and U17), if any
     PROM capacity and type
     PROM access time, maximum
     Upper bank starting address

   Refer to Section 5.2.2 to configure the DB16000A to support these PROMs.

2. Port Connections (see Figure 2-1). Monitor software designed by National Semiconductor assumes Port 0 (J2) will be connected to the user's terminal and Port 1 (J3) will be connected to the host or a modem for transparent mode. Connection is simple using the two cable sets supplied with DB16000A.

Connect the terminal to J2, using either of the two cable sets as follows:

- Locate the cable with the 26-pin card edge connector. Connect the cable as shown in Figure 2-2.

- Connect the remaining end of the cable to the terminal's RS232 connector. If the terminal connector is not male, it will be necessary to install the cable set's remaining male-to-male cable, as shown in Figure 2-3.

Now connect the host or modem to J3 using the remaining cable set. The procedure is the same as for J2 connections.

3. Terminal Configuration, Port 0 (J2). Port 0 (J2) is factory-configured as DCE allowing direct connection to terminals. Once the terminal is properly cabled to J2, communication can be verified. Variations in baud rate settings and RS232 handshake signal usage may require some reconfiguration of the DB16000A. This is productive, since terminal, DB16000A, and monitor operation can be verified before configuring Port 1.

   First, try it without reconfiguration. Apply power to the DB16000A. The monitor's banner should appear on the terminal screen each time the DB16000A is powered on or manually reset.

   If no characters appear on the screen, it may be necessary to loop back the RTS/CTS and DSR/DTR handshake signals. The DB16000A is factory configured to expect these signals. If these signals are not used by the terminal, consult Section 5.2.3 for J2 (Port 0) optioning instructions.

   If garbled characters appear on the screen, it may be necessary to reconfigure the Port 0 baud rate. The factory configuration is 9600 baud. Before reconfiguring the port, consider that Port 0 baud rate must never be less than Port 1's baud rate during transparent operation. If Port 0's baud rate is less, there is risk of overrun when the host transmits to the terminal. If possible, reconfigure the terminal to operate at 9600 baud. If the terminal cannot support 9600 baud, use its next highest baud rate, then configure the DB16000A Port 0 to match. Instructions to alter Port 0 baud rate are found in Section 5.2.3.

4. Host Port Configuration, Port 1 (J3). Port 1 (J3) is factory-configured as DTE (Data Terminal Equipment). Consult the host RS232 port documentation. If the host port is DCE (most are) then the DB16000A Port 1 configuration is compatible. If the host port is DTE, Port 1 must be reconfigured as DCE. Consult Section 5.2.3 for instructions to convert Port 1 to DCE.

Determine whether the host port uses RTS/CTS and DSR/DTR RS232 handshake signals. The DB16000A is factory-configured to use these signals. If the host does not support them, it will be necessary to reconfigure Port 1. Consult Section 5.2.3 for instructions to "loop back" RTS/CTS and DSR/DTR.

Next, determine the host port baud rate. If the host port is not 9600 baud, or if Port 0 is no longer set to 9600 baud, reconfiguration will be necessary. Recall that in transparent mode Port 0 must be greater than or equal to Port 1 baud. Consult Section 5.2.3 for baud rate option instructions.

Finally, test the entire setup: load and invoke the host's software development package. Activate the DB16000A and user terminal. Invoke the monitor's transparent mode. Log onto the host system.

2.4 NS16000 FAMILY CONFIGURATIONS

The DB16000A will permit operation of the following NS16000 components:

- NS16032 32-bit CPU; 16-bit data bus
- NS08032 32-bit CPU; 8-bit data bus
- NS16082 MMU; memory management slave processor
- NS16081 FPU; floating-point slave processor
- NS16202 ICU; interrupt controller
- NS16201 TCU; timing control unit

The user may evaluate each of these components in a native environment.

A minimum configuration requires the NS16201 TCU and either the NS16032 or the NS08032 CPU. The difference in data bus width between the two CPU's is easily accommodated by DB16000A's configuration jumpers. The remaining NS16000 family members may be operated in almost any mix. The single exception is the NS08032 CPU which will not function with the NS16082 MMU.

The DB16000A hardware design permits operation of the NS16000 components at speeds up to 10 MHz CTTL frequency. A plug-in crystal-controlled TTL output oscillator provides the 2X CTTL base frequency to the NS16201 TCU. This permits the user to substitute other operating frequencies, if desired; however, the frequency can be no greater than that permitted by the slowest NS16000 component installed.

Section 5.2.1 contains all information necessary to install NS16000 components in the board.

Note that when the NS16202 ICU is installed, its clock output pin is available for use as the baud rate clock to the DB16000A's serial ports. TDS16A and MON16 PROM base software use this function to implement programmable baud rate.

2.5 MULTIBUS SYSTEM CONFIGURATIONS

The user may contemplate evaluation of NS16000 components in system designs much larger or more complex than those implemented in DB16000A. For this reason, the DB16000A incorporates a MULTIBUS interface, permitting the user to configure systems incorporating other MULTIBUS compatible boards. Such boards are:

- Expansion RAM
- Expansion ROM
- Disk Controllers
- LAN Controllers
- Process Control and Instrumentation Interfaces

A wide variety of these products is available from National Semiconductor Corporation's Microcomputer System (MCS) division. Refer to the MULTIBUS Board Level Computer Products databook or a National Semiconductor sales representative for more information on boards, cardcages, backplanes, and power supplies. Wherever possible, the DB16000A permits maximum flexibility in the system configuration. Multiple DB16000A's may be installed in the system to permit multiprocessor evaluations.

2.5.1 Required Equipment

The following equipment is required for any configuration of DB16000A and MULTIBUS compatible boards.

- MULTIBUS compatible cardcage or enclosure. Possible sources include National Semiconductor's BLC-604 and BLC-614 cardcages. The BLC-604 is a 4-slot cardcage. It can be expanded in increments of four slots by attaching BLC-614's.

- DC Power Supplies. Possible sources include National Semiconductor's BLC-635 and BLC-665 power supplies. Either supply will power the DB16000A and permit operation of additional boards. The user must select power supplies of sufficient current capacity to operate the boards installed. Below is a summary of BLC-635 and BLC-665 capacities:

VDC	BLC-635	BLC-665
+5	14.0 A	30.0 A
-5	0.9 A	1.75 A
+12	2.0 A	4.5 A
-12	0.8 A	1.75 A

Power supply and cardcage requirements may be met by purchasing National Semiconductor's RMC-655 or RMC-660 System Chassis. The RMC-655 contains a BLC-635 power supply and a BLC-604 4-slot cardcage. The RMC-660 contains a BLC-665 power supply and an 8-slot cardcage assembly.

2.5.2 MULTIBUS System Parameters

When configuring a MULTIBUS system with a DB16000A, no less than eight system parameters must be configured:

- Bus arbitration
- Interrupt usage
- Off-board addressing
- Bus data path
- Dual port RAM usage
- Bus lock and system semaphores
- Clock sources
- Initialization

The magnitude of permissible system configurations is quite large. Therefore, this manual attempts only to acquaint the user with the nature of the variables, and options incorporated in the DB16000A design. Pertinent jumper options are mentioned in this section. Specific option definitions are contained in Section 5.2.5.

Bus Arbitration. The DB16000A design permits operation in single- or multimaster systems. In single-master systems, the DB16000A will be the only board capable of bus acquisition (i.e. there are no cases where another board must acquire it). In multimaster systems, the DB16000A must contend for the bus among other potential bus masters.

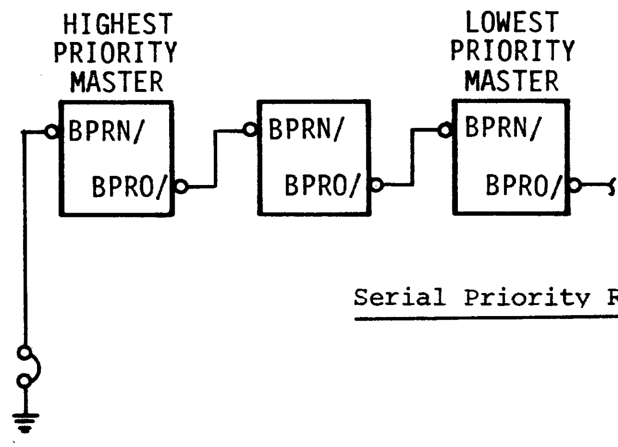
Bus contention among masters is resolved by hardware arbitration. Two arbitration schemes are permitted, serial and parallel resolution. The user must choose one.

In serial resolution schemes, a request for bus access is propagated from one board's arbiter circuitry to the next. Priority is implicit in the board's position within the cardcage/backplane. A lower priority board may acquire the board only if a higher priority master is not requesting the bus.

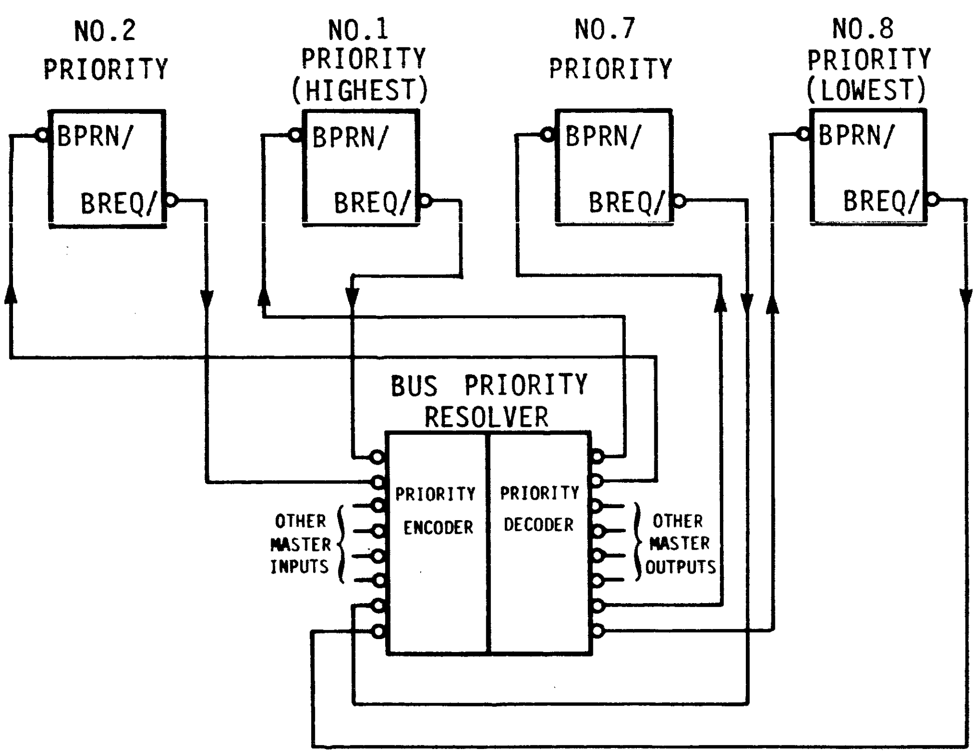
In parallel resolution schemes, a central arbitration circuit must be added to the system. In this case, each master's request is presented, in parallel, to the central arbiter. Priority resolution is a property of the central arbiter's design.

Figure 2-4 illustrates the two schemes.

Serial resolution is the simplest of the two schemes and is the default condition for single-master systems. In Figure 2-4 note that the highest priority master must have its BPRN/ signal grounded at the backplane connector, indicating no higher priority requests. This is done by grounding P1, pin 15.



Serial Priority Resolution



Parallel Priority Resolution

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Figure 2-4 MULTIBUS Priority Resolution Schemes

Implicit in serial resolution is the possibility that the lowest priority master can be starved for bus access. The CBRQ/ signal may be used to reduce this possibility.

CBRQ/ is an open-collector signal that can be driven by any master. It is used to notify the active master that a lower priority board must have the bus. The active master responds by terminating its bus access as soon as possible. Not all MULTIBUS boards implement the CBRQ/ usage. Clearly the scheme requires all masters in the system to implement CBRQ/ if any one master uses it. Jumper W9 on the DB16000A enables its use of CBRQ/.

In the factory configuration, CBRQ/ is disabled. If enabled, the DB16000A acquires and retains the bus until another master asserts CBRQ/. If disabled, the DB16000A must contend for the bus in each word or byte transfer. For single master systems, the user is advised to enable CBRQ/, thus saving the contention time for each transaction on the bus. If enabled, be certain CBRQ/ is pulled up on the backplane.

If parallel priority resolution is to be implemented, the user must disable the DB16000A's BPRO/ signal. This is done via jumper W10. The DB16000A is factory-configured with BPRO/ enabled.

Interrupt Usage. If MULTIBUS interrupts are to be recognized by the DB16000A, the NS16202 ICU must be installed. Refer the Section 5.2.1 for installation instructions.

In the factory configuration, no connection is made between the NS16202 ICU and the MULTIBUS interrupt signals (INT0/ throught INT7/). These must be wire-wrapped as required by the user. Refer to Section 5.2.1 for instructions.

Off-board Addressing. The NS16000 architecture assumes all accesses to be memory mapped. This poses no real problem since its address space is quite large (32M bytes if the MMU is used or 16M bytes if not).

In the factory configuration, with 128K bytes of on-board RAM, the DB16000A treats addresses ranging from 028000H to 7FFFFFH as off-board RAM. Addresses from 800000H to 9FFFFFH are considered off-board I/O ports. In both cases, a 24-bit address is presented to the MULTIBUS slave. The lower 20 bits are presented on the P1 connector and the upper 4 bits on the P2 connector.

MULTIBUS compatible slaves may respond to 16-, 20-, or 24-bit addresses. Consequently, the actual system address capacity is limited by the board utilizing the fewest address bits. In any case, DB16000A software references remain the same. For example, if the smallest board address capacity is an I/O board with 16 address bits, the DB16000A will still present a full 24-bit address. The upper 8 bits are simply ignored by the 16-bit board. However, an adjacent 20-bit board would require its upper four bits of address decoding to be "don't care", for compatibility.

Bus Data Path. Since the DB16000A permits operation with either NS08032 or NS16032 CPU's, special consideration must be given the system data path width while selecting other MULTIBUS boards. The DB16000A will have no difficulty accessing boards whose data paths are symmetrical to its CPU (i.e. NS08032 vs. 8-bit slaves and NS16032 vs. 16-bit slaves).

With the NS16032 installed, transactions with 8-bit slaves are limited. Obviously, full 16-bit word transfers are not possible. Therefore, programs to be executed by the NS16032 cannot be read from an 8-bit slave. Operand accesses may be made, provided they are in byte quantities.

Dual-Port RAM Usage. The DB16000A's on-board RAM can be accessed by another bus master. When this occurs, the DB16000A is considered the bus slave. Its MULTIBUS slave compatibility code is "D16", indicating the RAM can be accessed by 8- or 16-bit masters, with no data path restrictions.

In the factory configuration, dual-port operation is disabled and all on-board RAM is private to the DB16000A CPU. Dual-port operation is enabled by W13. Consult Section 5.2.5 for instructions.

Once dual port is enabled, its MULTIBUS address must be configured. This is the address other masters use to access the DB16000A RAM.

To configure the dual port's MULTIBUS address, first determine the addressing range of the other bus masters. Choosing the smallest range capability, configure the DB16000A to match. The dual-port address decode logic can function with 16-, 20-, and 24-bit MULTIBUS addresses. Configuration is best approached by starting with 24 bits and working down.

If the full 24 address bits cannot be used, disable the megabyte address decoder. This is accomplished with jumper W13, and shrinks the MULTIBUS addressing to one megabyte (000000H to 0FFFFFH). If all 24 address bits can be used, select the megabyte address range, via jumper W14. Selection is made in one megabyte increments. The factory configuration places the RAM in the highest megabyte (F00000H to FFFFFFH).

Next select the starting address of DB16000A RAM, within the selected megabyte range. This is accomplished via jumper W15 in increments of 32K bytes. If the MULTIBUS address field is 20 bits, any of the 32 starting positions may be selected. If the MULTIBUS address field is limited to 16 bits, the selected starting address must be within the lower 64K bytes of the range.

Finally, select the degree of privacy. This means the user can select the portion of DB16000A's RAM which can be accessed by other masters; the remaining portion is private to the DB16000A CPU. This is accomplished via jumper W16 in increments of one quarter of RAM (i.e., if one-quarter of the RAM is designated accessible, the upper three-quarters are private, if one-half the RAM is accessible, the upper half is private, etc.).

Bus Lock and System Semaphores. The DB16000A implements the MULTIBUS lock signal. When activated, no master may access the bus, or its own dual port RAM, except the master asserting lock. This function is used to implement system semaphores.

The DB16000A may assert lock by any of three means:

- Under program control, by accessing the DB16000A mode register
- By executing an interlocked NS16000 instruction
- By permitting MMU update cycles to cause lock

The latter choice, MMU update, is enabled via jumper W4. If enabled, lock is asserted each time the MMU accesses its page tables.

Clock Sources. MULTIBUS clock signals BCLK and CCLK, may be supplied by only one master on the MULTIBUS interface. The clocks are supplied by the selected master, at all times.

The DB16000A is factory-configured to supply BCLK and CCLK. This function can be disabled via jumper W22.

Initialization. The DB16000A generates and accepts the MULTIBUS INIT signal. On power-on, the DB16000A drives the INIT signal for a period greater than 38 milliseconds, but less than 200 milliseconds.

If INIT is driven at any other time by another means, the NS16000 CPU requires the period to be greater than or equal to 64 CTTL cycles (greater than or equal to 10.7 microseconds at 6 MHz CTTL and greater than or equal to 6.4 microseconds at 10-MHz CTTL).

Chapter 3

HARDWARE ORGANIZATION

3.1 INTRODUCTION

The DB16000A is divided into three main modules:

- CPU Module
- Memory Module
- I/O Module

These are described in Sections 3.3 through 3.5.

3.2 DOCUMENTATION CONVENTION

The circuit descriptions in this chapter are based on the logic diagrams supplied with the board. The circuit names are those used on the detailed block diagram (Sheet 1 of 10). The signal name mnemonics are used to both identify particular functions and to trace circuit lines from sheet to sheet. Signal mnemonics are defined as they are used in the text.

Both active low and active high signals are used in the DB16000A circuit. Active low signals are suffixed by a slash (/), or overscored (‾). For example, the signals, RAS/ and $\overline{\text{CAS}}$, are active low. Signals not specifically identified as active low are active high. MUXSEL and RMA0 are active high signals.

NOTE: Low and high are TTL levels, i.e., low is > = -0.5 volts, but < = +0.8 volts and high is > +2.0 volts, but < +5.5 volts.

3.3 CPU MODULE

The CPU module consists of:

- CPU
- Clock and Time Base Generator
- Memory Management Unit (MMU)
- Floating-Point Unit (FPU)

These are described in Sections 3.3.1 through 3.3.4.

3.3.1 CPU

The CPU on the DB16000A can be either the NS16032 (16-bit data bus) or the NS08032 (8-bit data bus). When the NS16032 is installed, transfers between the CPU and the on-board dual-port RAM, the MULTIBUS interface, or the BLX connector can be either 8-bit or 16-bit data transfers. When the NS08032 is installed, all data transfers are 8-bit data transfers and are always made on the eight least significant data lines.

3.3.2 Clock and Time Base Generator

Clock and control signals to the NS16000 components in the CPU module (CPU, MMU, and FPU) are generated by the NS16201 Timing Control Unit (TCU). The TCU provides two nonoverlapping clock signals for the NS16000 CPU and a synchronous TTL clock signal for support chips. In addition, the TCU generates synchronized reset and ready signals for the CPU. The state of the reset and ready signals depends on inputs to the TCU from peripherals.

The TCU provides for easy generation of different numbers of wait states during CPU bus cycles. There are four WAIT inputs to the TCU. Each provides for a different number of wait states to be inserted in a CPU bus cycle. Up to 15 wait states can be inserted in this manner, allowing the CPU to interface with different speed memories and peripherals with a minimum of additional circuitry.

The TCU also provides data flow control signals used by memory devices and peripherals. These signals ensure proper timing of data transferring to and out of the CPU.

Detailed information on the TCU can be found in the NS16201 Timing Control Unit data sheet.

The timebase for baud generation, programmable interval timers, and the MULTIBUS clocks (BCLK and CCLK) is provided by an 18.432-MHz oscillator.

3.3.3 Memory Management Unit (MMU)

The MMU is an optional slave processor that supports a virtual memory system, with all the capabilities of an operation system memory management environment. The MMU is capable of dynamic address translation, virtual memory management, and memory protection. The MMU also provides for software debugging in a virtual machine environment and for hardware debugging in an in-system emulation environment.

The MMU is driven directly by the CPU bus. The CPU generates virtual addresses (as given by the software) and the MMU converts these to the physical addresses as required by the hardware. If the virtual address points to a data block not currently in system main memory, the MMU notifies the CPU, which will move the required data into main memory and restart the program at the interrupted instruction.

Detailed information on the MMU can be found in the NS16082 Memory Management Unit (MMU) data sheet.

3.3.4 Floating-Point Unit (FPU)

The FPU is an optional slave processor that provides very high speed floating-point operations for both single- and double-precision operands. When installed, the FPU receives opcodes and operands from the CPU, and returns results and status to the CPU, when operations are complete. Use of the FPU frees the CPU for other tasks while long computations are being performed.

Detailed information on the FPU can be found in the NS10081 Floating-Point Unit data sheet.

3.4 MEMORY MODULE

The memory module consists of:

- Dual-port RAM
- Dual-port RAM controller
- ROM/EPROM sockets

These are described in Sections 3.4.1 through 3.4.3

3.4.1 Dual-port RAM

The DB16000A is supplied with 128K-byte dual-port RAM. The RAM array consists of sixteen 64K-bit dynamic RAM devices.

The 128K-byte dual-port dynamic RAM address is fixed for access from the local CPU, beginning at 008000 (hex). The address of the RAM when accessed as a slave from the MULTIBUS interface can be set by jumpers.

For slave accesses, the address can be set to any 32K-byte boundary in the 16M-byte MULTIBUS address space. Jumpers can be set to permit all 3/4, 1/2, 1/4, or none of the dual-port RAM to be private to the local CPU. The slave address space can not cross a megabyte boundary.

3.4.2 Dual-Port RAM Controller

The dual-port RAM controller arbitrates requests for access to the RAM from the local CPU, an external MULTIBUS bus master, and the refresh counter. The refresh counter has the highest priority. An external request has the next highest priority and the local CPU has the lowest priority.

3.4.3 ROM/PROM Sockets

Two pairs of 24/28-pin ROM/PROM sockets on the DB16000A provide up to 96K bytes of on-board ROM/PROM. One pair (lower bank) always has a base address of 0. The other pair (upper bank) can start immediately following the end of the lower bank address range (contiguous mode) or be jumper-selected to start at address D00000 (hex) (high address mode). The following ROM/PROM devices can be used:

- 16K-bit device (2716)
- 32K-bit device (2732)
- 64K-bit device (2764)
- 128K-bit device (27128)
- 256K-bit device (27256); for future expansion

The upper and lower banks need not be the same size, though both devices in one bank must be the same size.

The total ROM/PROM that can be contiguous in the lower address range is 32K bytes. This can be any combination of PROM sizes for the lower and upper bank as long as the total of the two pairs (four devices) does not exceed 32K bytes. For the two banks to be contiguous, the upper bank must not be larger than the lower bank.

If only the lower bank is at the lower address range, the lower bank can consist of 2716, 2732, 2764, or 27128 devices. If both the lower and upper bank are at the lower address, a 2764 device is the largest device that can be used. Finally, if the upper bank is set to reside at D00000 (hex), the upper bank can consist of any device from 2716 to 27256.

3.5 I/O MODULE

The I/O module consists of:

- RS232C Serial Communication Ports
- Parallel Port
- Switches and Indicators
- ICU
- MULTIBUS Interface Arbiter

These are described in Sections 3.5.1 through 3.5.5.

3.5.1 RS232C Serial Communication Ports

Two RS232C ports (J2 and J3) provide synchronous or asynchronous serial communication. Each of these ports is implemented with an 8251A programmable communications interface.

3.5.2 Parallel Port

The parallel port provides 24 parallel I/O lines. The DB16000A provides sockets for buffering or terminating the signal lines. The parallel port is implemented with an 8255A programmable peripheral interface.

The 24 parallel I/O lines are grouped as three 8-bit ports. One of the ports can have a bidirectional inverting or non-inverting buffer. The two other ports can either have terminating networks or unidirectional buffers.

3.5.3 Switches and Indicators

Two pushbutton switches are provided. One switch resets the board to an initial state. The other switch causes a nonmaskable interrupt.

An 8-position DIP switch on the DB16000A is used to indicate board configuration; e.g. the presence of the FPU and MMU.

Three LED indicators are provided for diagnostic information and general user application. One LED is a diagnostic run indicator that, when lit, indicates the diagnostic monitor program is executing. Another LED is a diagnostic fail indicator that, when lit, indicates the diagnostic monitor did not pass all tests. The third LED is not dedicated to a specific purpose and is provided for user application.

3.5.4 ICU

The NS16202 Interrupt Control Unit (ICU) provides interrupt capability and a programmable counter for the serial port baud generation, when installed and enabled. ICU is configured to operate in the 8-bit mode. IR10 and IR11 can be connected to TXRDY and RXRDY from the serial interface Port 0, J2 connector. All lines are jumper selectable to various on-board and off-board (MULTIBUS) sources.

3.5.5 MULTIBUS Interface

A MULTIBUS interface arbiter, along with bus interface logic, provides full multimaster interface to the MULTIBUS interface. Twenty-four address lines and sixteen data lines permit 16-bit transfers in the full 16M-byte address space of MULTIBUS systems. A constant clock (CCLK) and bus clock (BCLK) can be generated at a frequency of 9.216 MHz, independent of the CPU frequency.

Chapter 4

PROGRAM INTERFACE

4.1 INTRODUCTION

This chapter contains informantion necessary to manipulate the DB16000A under program control. Only information related to the hardware implementation is supplied (i.e., register address assignments).

Information in this chapter should be considered supplemental to that found in pertinent device specifications and programming guides. The user is encouraged to have specifications on hand for the following devices before writing software for DB16000A execution:

- NS16032 CPU
- NS08032 CPU
- NS16082 MMU
- NS16081 FPU
- NS16202 ICU

If the user intends to develop software to use on-board I/O devices, the following additional specification and operation data is required:

- Type 8253-5 Programmable Interval Timer
- Type 8255A-5 Programmable Peripheral Interface
- Type 8251A Programmable Communication Interface

4.2 ADDRESSABLE ELEMENTS

The DB16000A incorporates a 16-megabyte address space. Table 4-1 depicts the partitioning of the space.

The DB16000A's data path is configurable via hardware for 8-bit data (NS08032 installed) or 16-bit data (NS16032 installed). Both on-board ROM and RAM are fully byte-addressable. Serial I/O, Parallel I/O, Programmable Timers, and ICU are even-byte addressable (A0=0) only. BLX and MULTIBUS off-board I/O addressing are functions of user configurations.

4.2.1 On-Board I/O

Addresses between C00000H and CFFFFFH are reserved for DB16000A on-board I/O elements. The following is a description of register address assignment and function for each element. All elements are even-byte addressed, and use the lower eight data bits. (D0 through D7).

TABLE 4-1 DB16000A ADDRESS SPACE

ADDRESS RANGE (HEX)	DESCRIPTION
000000-007FFF	On-board ROM/EPROM expansion
008000-027FFF	Dual-port RAM
028000-7FFFFF	Off-board RAM
800000-9FFFFF	Off-board I/O ports
C00000-CFFFFF	On-board I/O ports
C00000-C00004	Serial port J2 Port 0
C00030-C0003E	Configuration Switch/Register
C00040-C0004F	Serial port J3 Port 1
C00050-C0005F	Programmable timers
C00060-C0006E (even)	BLX J4 MCS0/
C00070-C0007E (even)	BLX J4 MCS1/
C00061-C0006F (odd)	BLX J4 MCS1/
D00000-D0FFFF	On-board ROM/EPROM expansion
E00000-FFFFFF	ICU ports

Configuration Switch and Register (C00030 - C0003E).

CONFIGURATION SWITCH (S3)

The content of an 8-position DIP switch can be read from location C00030. Each of the eight individual switches corresponds to a data bit. When closed, a switch is read as 0. When open, a switch is read as 1.

The configuration switch is provided as a means of indicating user-selectable options to the on-board software.

CONFIGURATION REGISTER

An 8-bit register is provided for program control of:

- System override function (refer to Section 5.2.5)
- LED indicators DS1 through DS3 (refer to Section 1.2.3)
- Serial port diagnostic loopback

The register is write-only. Each bit is byte addressed with D0 determining whether the bit is set or cleared. All bits are cleared by power-on or manual reset. Table 4-2 lists the program control functions of the configuration register and the address location of those functions.

Serial I/O Ports 0 and 1. Type 8251A USARTS are provided for serial communication. The device internal registers can be addressed as follows:

Port 0

C00000	data read/write
C00002	command

Port 1

C00040	data read/write
C00042	command

Both serial port baud rates can be placed under program control via the 8253-5 PIT. This, however, also requires reconfiguration of hardware jumper options. Refer to Section 5.2.3 for details. If the NS16202 ICU is installed, serial port operation can be interrupt driven. Note that both ports may be placed in a special, diagnostic mode via the configuration register. In diagnostic mode, TxD/RxD and RTS/CTS loop-back is provided via hardware.

Parallel I/O (PIO). A type 8255A-5 PPI device is provided for peripheral interfacing. The device internal registers can be addressed as shown in Table 4-3. Hardware options for PIO interface are described in Section 5.2.4. Note that Port C can be configured to pass peripheral interrupts to the NS16202 ICU.

TABLE 4-2 CONFIGURATION REGISTER CONTROL FUNCTIONS

LOCATION	FUNCTION
C00030	Override; asserts MULTIBUS LOCK/ signal if D0 = 1
C00032	DS3 LED; illuminated if D0 = 0
C00034	DS2 LED; illuminated if D0 = 0
C00036	DS1 LED: illuminated if D0 = 0
C00038	Serial port diagnostic mode; connects RTS to CTS, TXD to RXD, and imposes gang clock for both ports, if D0 = 1
C00003A-C0003E	Reserved

TABLE 4-3 PPI INTERNAL REGISTER ADDRESSES

LOCATION	READ	WRITE
C00020	Port A	Port A
C00022	Port B	Port B
C00024	Port C	Port C
C00026	Illegal	Control Word
C00028-2E	Reserved	

Programmable Interval Timers (PIT). A type 8253-5 PIT device is provided for on-board time base generation. It provides the basis of software controlled serial baud rates, as well as an additional periodic interrupt input to the NS16202 ICU. Three, independent 16-bit counter/timers are provided. The intended timer output usage is as follows:

- Timer 0-interrupt input to ICU (refer to Figure 5-2)
- Timer 1-baud clock for Port 1 or interrupt input to ICU
- Timer 2-baud clock for Port 0 (refer to Section 5.2.3)

Use of any timer output requires jumper optioning.

The device internal registers may be accessed as shown in Table 4-4.

4.2.2 ICU

The DB16000A implements the NS16202 ICU in 8-bit mode. If installed, this device can accept up to 16 hardware-generated interrupt inputs. Refer to Figure 5-2 for interrupt input choices.

Installation of the ICU is described in Section 5.2.1.

TABLE 4-4 PIT INTERNAL REGISTER ADDRESSES

LOCATION	READ	WRITE
C00050	Counter 0	Counter 0
C00052	Counter 1	Counter 1
C00054	Counter 2	Counter 2
C00056	NOP	Mode Word
C00058-5E	Reserved	

8 bit bus mode

TABLE 4-5 ICU REGISTER ADDRESSING

REG. NUMBER AND ADDRESS IN HEX	REG. NAME	REG. FUNCTION
FFFE00 R0(00) F	HVCT	HARDWARE VECTOR
FFFF02 R1(02) F	SVCT	SOFTWARE VECTOR CMB FFFEϕ2 =1ϕ
R3(06) R2(04) 0	xxxx|x000 ELTG	EDGE/LEVEL TRIGGERING
R5(0A) R4(08) 3	xxxx|x011 TPL	TRIGGERING POLARITY
R7(0E) FF R6(0C) FE	IPND	INTERRUPTS PENDING CMB FFFEϕC =4ϕ CMB FFFEϕE =4ϕ
R9(12) ϕ R8(10) ϕ	ISRV	INTERRUPTS IN-SERVICE
R11(16) FF R10(14) F8	1111|1111|1111|1000 IMSK	INTERRUPT MASK CMB FFFE14 = FE
R13(1A) ϕ R12(18) ϕ	CSRC	CASCADED SOURCE
R15(1E) ϕ R14(1C) 2	FPRT	FIRST PRIORITY
R16(20) 2	MCTL	MODE CONTROL
R17(22) ϕ	OCASN	OUTPUT CLOCK ASSIGNMENT
R18(24) FF	CIPTR	COUNTER INTERRUPT POINTER
counters are assigned to interrupt position 15		
R19(26) FF	PDAT	PORT DATA
R20(28) FF	IPS	INTERRUPT/PORT SELECT
R21(2A) FF	PDIR	PORT DIRECTION
R22(2C) 54	CCTL	COUNTER CONTROL
R23(2E) C	CICTL	COUNTER INTERRUPT CONTROL
R25(32) R24(30) 5F	LCSV	L-COUNTER STARTING VALUE
R27(36) R26(34) FF	HCSV	H-COUNTER STARTING VALUE
R29(3A) R28(38) FF	LCCV	L-COUNTER CURRENT VALUE
R31(3E) R30(3C) FF	HCCV	H-COUNTER CURRENT VALUE

Register Address = $FFFEXX_H$; XX denoted in parenthesis beside register number

Chapter 5

HARDWARE OPTIONS

5.1 INTRODUCTION

The DB16000A's purpose is to incorporate a great deal of flexibility in a relatively small form factor. Like any complex tool, one must be careful applying it.

This chapter contains instructions needed to invoke the options implemented in DB16000A hardware. The user is encouraged to read the entire chapter, to gain a sense of the total flexibility, and how certain options interrelate.

Finally, the user is encouraged to plan each alteration, and execute methodically. This will consume much less time than debugging a mistake created in haste.

<u>WARNING</u>

> Do not alter DB16000A hardware configuration while power is applied. Serious circuit damage may result. Such damage is not covered by the warranty.

5.2 OPTION PROCEDURES

Optional functions include:

- NS16000 Family Mix
- PROM Capacity
- Serial I/O
- Parallel I/O
- MULTIBUS I/O
- BLX I/O

The following sections prescribe the method of invoking each option. Note that some cases entail programming requirements, as well as the prescribed hardware configuration.

5.2.1 NS16000 Family

The user may selectively configure the DB16000A to operate:

- With an NS16032 or NS08032 CPU
- With or without an NS16082 MMU
- With or without an NS16081 FPU
- With or without an NS16202 ICU

Further, the user may elect to operate the NS16000A family at frequencies other than factory-configured. Figure 5-1 depicts the location of option items.

NS08032 CPU Installation (U64, U69, U86, U88, W5, W17, W37).

1. Remove the NS16032 from its socket, U69, and set aside.

2. Insert the NS08032 into U69 making sure the orientation of pin 1 is correct.

3. Remove W5 jumper 1 to 2 and set aside.

4. Remove W17 jumpers 1 to 2, 4 to 5, 7 to 8, 10 to 11, 13 to 14, 16 to 17, 19 to 20, and 22 to 23.

5. Install W17 jumpers 2 to 3, 5 to 6, 8 to 9, 11 to 12, 14 to 15, 17 to 18, 20 to 21, and 23 to 24.

6. Remove W37 jumper 1 to 2.

7. Install W37 jumper 2 to 3.

8. Remove the socketed IC from U86 (8304) and set aside.

9. Remove the socketed IC from U88 (8303) and insert in socket U64. Make sure the orientation of pin 1 is correct.

NOTE: With NS08032 installed, data transactions occur in byte units only. DB16000A on-board I/O addressing is still restricted to even bytes, except for certain BLX configurations.

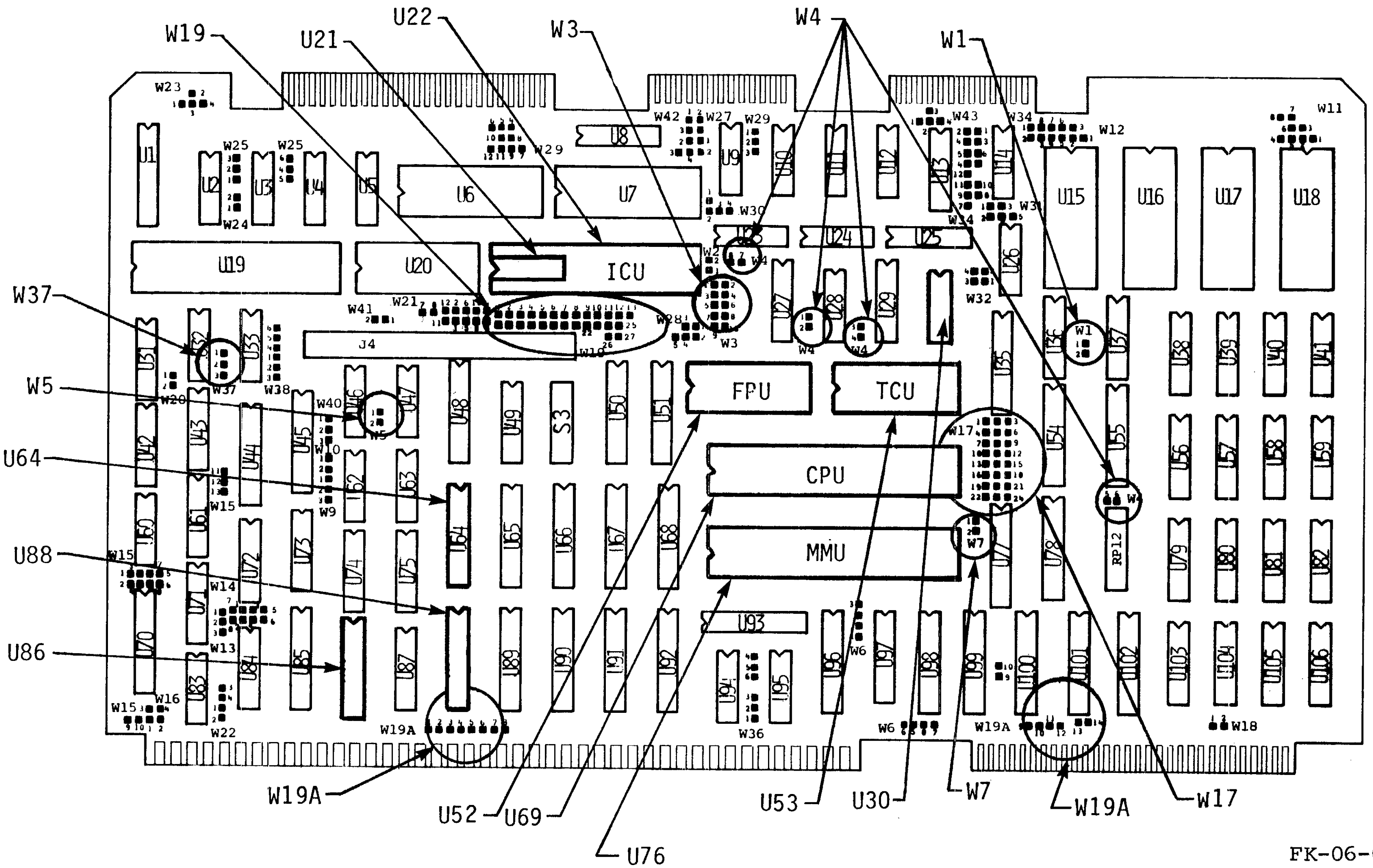

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Figure 5-1 NS16000 Option Items

NS16082 MMU Installation (U76, W4, W7).

1. Insert the NS16032 into socket location U76 making sure the orientation of pin 1 is correct.

2. Remove W4 jumpers 1 to 2, 3 to 4, and 5 to 6 and set aside.

3. If the DB16000A is used in a MULTIBUS multimaster system, install W4 jumper 7 to 8.

4. If MMU debug functions (breakpoint and trace) are to be invoked with interrupt capability, install W7 jumper 1 to 2.

Programming Note: MMU operation is entirely under program control. Refer to NS16082 data sheet.

NS16081 FPU Installation (U52).

1. Insert the NS16081 into socket location U52 making sure the orientation of pin 1 is correct.

Programming Note: FPU operation is entirely under program control. Refer to NS16081 data sheet.

NS16202 ICU Installation (U21, U22, W19, W19A).

1. Remove the socketed IC from location U22 (LS92) and set aside.

2. Insert the NS16202 into socket location U21 making sure the orientation of pin 1 is correct.

3. Referring to Figure 5-2, configure the desired hardware interrupt inputs via the W19 jumper field. Most options require wire wrap.

NOTE: With U22 (LS92) removed, serial port gang clock line is no longer driven by hardware. The ICU can drive the line, if programmed to do so. Refer to Section 5.2.3 for alternatives.

Programming Note: ICU operation is entirely under program control. Refer to NS16202 data sheet.

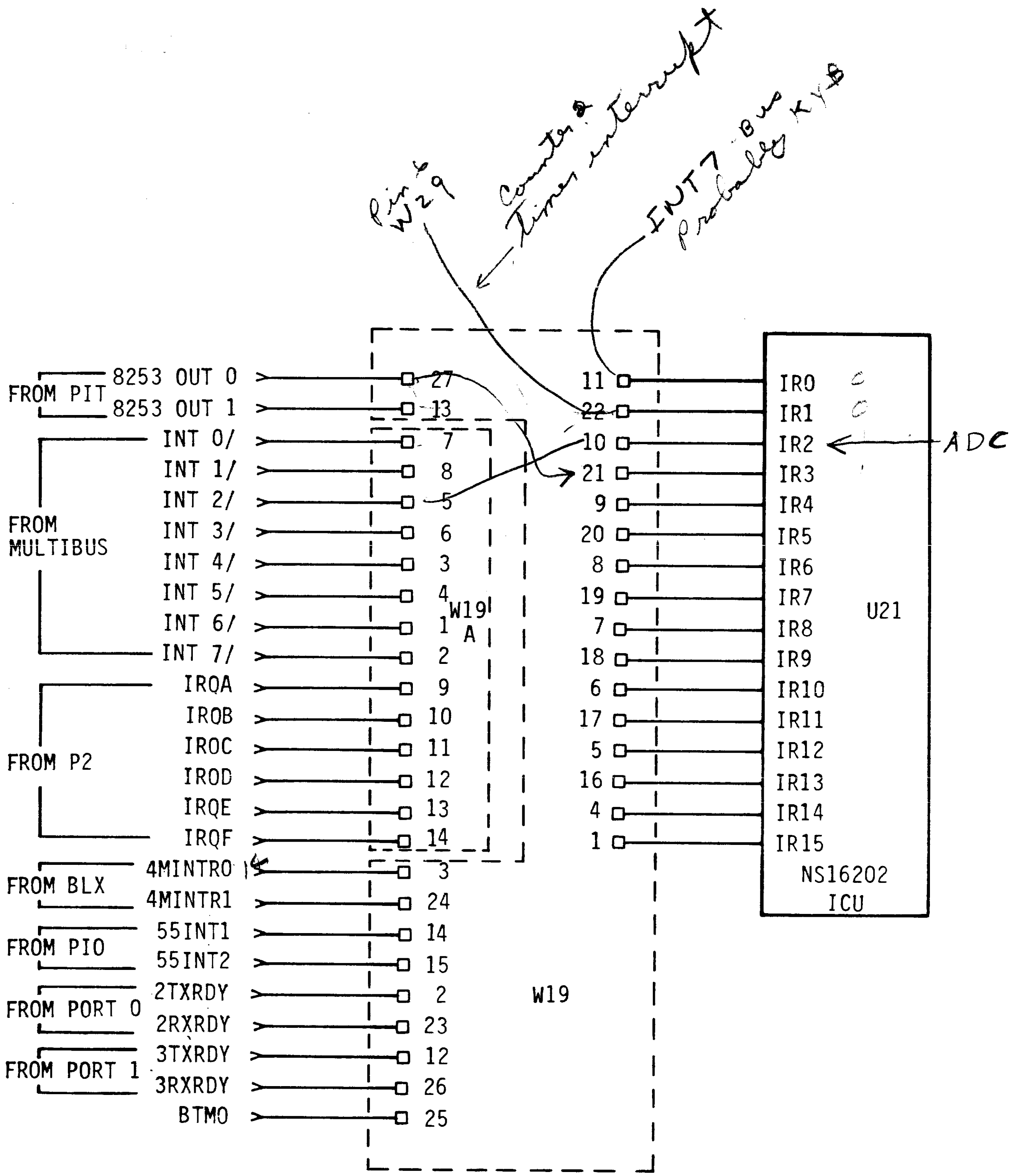

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Figure 5-2 ICU Interrupt Matrix

CTTL Frequency Alteration (U30, W1, W3).

Alternative 1:

1. Remove socketed oscillator at location U30 and set aside.

2. Install TTL output frequency source in U30.

Alternative 2:

1. Remove W1 jumper 1 to 2 and set aside.

2. Using clip leads, attach TTL output frequency source to W1 jumper post 2.

Alternative 3:

1. Remove W1 jumper 1 to 2 and set aside.

2. Attach TTL output frequency source to P2 connector pin 3.

NOTE: The CTTL operating frequency is one-half that supplied to the DB16000A. The minimum CTTL frequency is 200 KHz. The maximum CTTL frequency must equal the operating frequency of the slowest NS16000 component installed.

Increasing the CTTL frequency above factory configuration will also require alteration of on-board I/O wait state selection.

- For frequencies above 6.0 MHz operation, install W3 jumper 5 to 6, and remove W3 jumper 1 to 2.

- For 200-KHz to 6.0-MHz operation, install W3 jumper 1 to 2 and remove W3 jumper 5 to 6.

The TTL output frequency source must always be ground-referenced to DB16000A.

5.2.2 PROM Installation

Four sockets, U15 through U18 are provided for PROM-based software. Each socket consists of 28 pins permitting insertion of 24- or 28-pin PROMs. The following PROMs are permitted on the DB16000A:

- 2716
- 2732
- 2764
- 27128
- 27256

The PROM array is organized as two banks, each consisting of two sockets. One socket within a bank contains even addressed (A0=0) data bytes. The other bank contains odd addressed (A0=1) data bytes.

The two banks are designated, lower and upper. The lower bank always begins at address 000000H. The upper bank starting address is flexible.

Socket designations are:

- U18-lower bank, even byte
- U17-upper bank, even byte
- U16-upper bank, odd byte
- U15-lower bank, odd byte

Each bank must contain PROMs of identical capacity. However, bank capacities need not be the same (i.e., 2732 PROM's in one bank and 2764 PROM's in the other).

Wait state compensation for PROM access times is flexible. Wait state selection must correspond to the slowest PROMs installed.

In factory configuration, 27128 PROMs, containing TDS16A software are installed in U15 and U18. U16 and U17 are vacant, but are configured for 27128 PROMs. Wait state compensation is configured for less than or equal to 450 nsec access time.

Either or both banks can be reconfigured by the following procedure:

1. Select and configure the desired bank capacities and upper bank start address. Refer to Section 5.2.2.

2. Configure sockets to accept the desired PROM type and insert the PROM. Refer to Section 5.2.2.

3. Select and configure the wait state compensation required for the slowest PROMs. Refer to Section 5.2.2.

Figure 5-3 depicts the location of option items.

Bank Capacity and Upper Bank Start Address Selection (W6). The DB16000A recognizes two CPU address ranges as belonging to on-board PROM:

- 000000H to 007FFFH (32K bytes)
- D00000H to D0FFFFH (64K bytes)

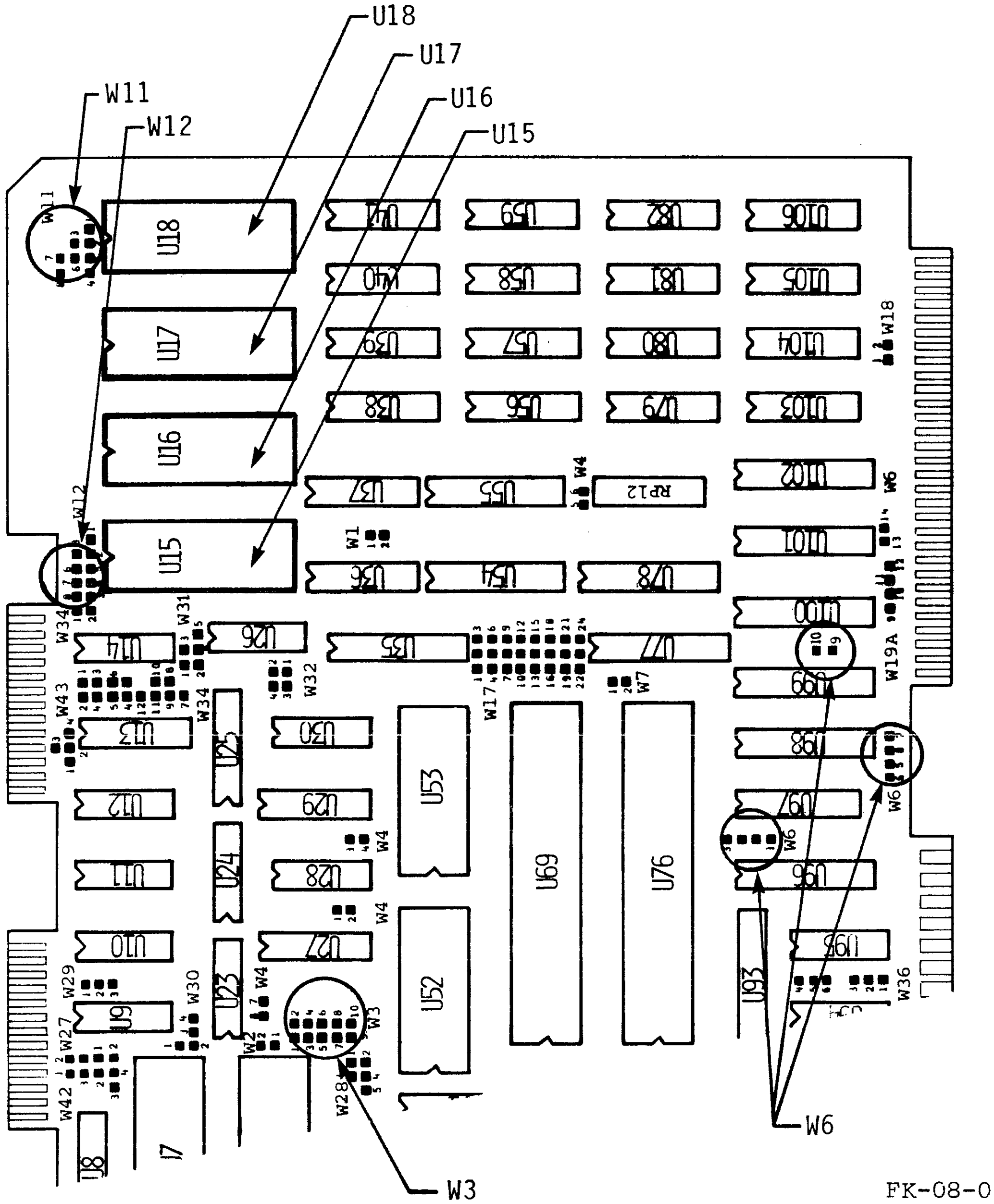

Figure 5-3 PROM Option Items

The total available PROM address space is 96K bytes. The user may elect to employ both PROM banks in the lower address range, provided their combined capacity does not exceed 32K bytes. Alternatively, the banks may be split, with the lower bank residing in the low address range (starting at 000000H) and the upper bank residing in high PROM address space (starting at D00000H). In any case, the low bank must be populated.

All permissible PROM types contain 8-bit data. For reference, individual bank capacity versus installed PROM type is listed in Table 5-1. 27256 PROMs cannot be installed in the lower bank, since the lower address range is restricted to 32K bytes and a bank of 27256 PROMs would be 64K bytes.

Table 5-2 lists permissible PROM mixes for both banks, the W6 jumper settings, and the resulting addresses and net capacities.

Programming Note: When both PROM banks reside in the low address range, it is advised to place the larger PROMs in the lower bank. If this is not done, the active addresses will be noncontiguous.

<u>Socket Configuration (U15, U16, U17, U18, W11, W12)</u>. All four DB16000A PROM sockets will accommodate 24- or 28-pin devices. Caution must be exercised when configuring the sockets. A mistake may damage the PROM, the DB16000A, or both.

Two jumper fields are provided for socket configuration, one for each bank. W11 jumpers configure the lower bank (U15 and U18) while W12 jumpers configure the upper bank (U16 and U17).

To configure each bank's sockets:

1. Determine whether the replacement PROMs are the same type as those being replaced (e.g. 2716)

2. Remove the existing PROMs from the bank and set aside.

3. Insert the replacement PROMs observing the proper odd/even byte designation of the sockets.

   NOTE: 24-pin devices must be placed so that their direction is aligned with the socket's and the device is located in the bottom of the socket pin field. Refer to Figure 5-4.

4. If the replacement PROM is a type different from the previous configuration, remove all jumpers from the corresponding field; W11 for the lower bank and W12 for the upper bank.

5. Install jumpers appropriate to the replacement PROM type as recommended in Table 5-3.

TABLE 5-1 BANK CAPACITY FOR INSTALLED PROM TYPES

TYPE	BANK CAPACITY
2716 (2K x 8)	4K bytes
2732 (4K x 8)	8K bytes
2764 (8K x 8)	16K bytes
27128 (16K x 8)	32K bytes
27256 (32K x 8)	64K bytes

TABLE 5-2 PROM BANK CAPACITY AND ADDRESS SELECTIONS

LOWER BANK (U15 AND U18)					UPPER BANK (U16 AND U17)							
W6 JUMPER		PROM		BANK	W6 JUMPER			PROM		BANK	NET	
9-10	7-8	TYPE	ADDRESS RANGE	CAPACITY	5-6	3-4	1-2	TYPE	ADDRESS RANGE	CAPACITY	CAPACITY	
x	x	2716	000000-000FFF	4K		NA		NONE	NA	0	4K	
					x	x	x	2716	001000-001FFF	4K	8K	
					x	x	-	2732	002000-003FFF	8K	12K*	
x	-	2732	000000-001FFF	8K		NA		NONE	NA	0	8K	
					x	x	x	2716	002000-002FFF	4K	12K	LOWER
					x	x	-	2732	002000-003FFF	8K	16K	32K
					x	-	x	2764	004000-007FFF	16K	24K*	ADDRESS
-	x	2764	000000-003FFF	16K		NA		NONE	NA	0	16K	
					x	x	x	2716	004000-004FFF	4K	20K	
					x	x	-	2732	004000-005FFF	8K	24K	
					x	-	x	2764	004000-007FFF	16K	32K	
-	-	27128	000000-007FFF	32K		NA		NONE	NA	0	32K	
					x	-	-	2716	D00000-D00FFF	4K	Lower + 4K	UPPER
					-	x	x	2732	D00000-D01FFF	8K	Lower + 8K	64K
					-	x	-	2764	D00000-D03FFF	16K	Lower + 16K	ADDRESS
					-	-	x	27128	D00000-D07FFF	32K	Lower + 32K	RANGE
					-	-	-	27256	D00000-D0FFFF	64K	Lower + 64K	

x Install Jumper
- Remove Jumper
* Noncontiguous Addressing

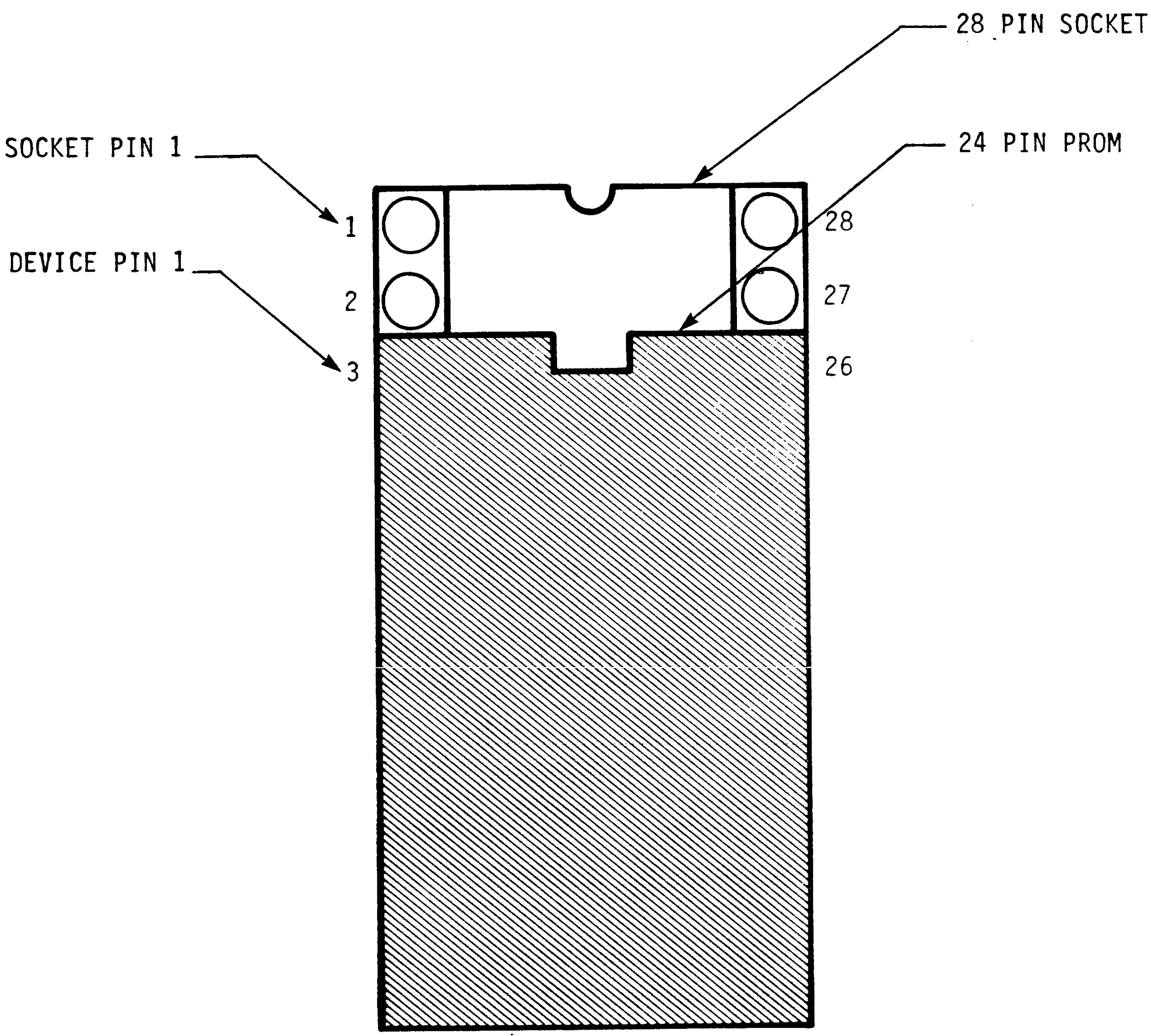

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Figure 5-4 24-Pin PROM Installation

TABLE 5-3 PROM BANK CONFIGURATION JUMPERS VS. PROM TYPE

PROM TYPE	LOWER BANK (U16 AND U18) W11 JUMPERS	UPPER BANK (U16 AND U17) W12 JUMPERS
2716	2-3, 5-6	2-3, 5-6
2732	1-2, 5-6	1-2, 5-6
2764	1-2, 6-7	1-2, 6-7
27128	1-2, 4-5, 6-7	1-2, 4-5, 6-7
27256	NA	1-2, 4-5, 7-8

Wait State Compensation (W3). PROM wait state compensation must be configured for the slowest devices installed. Further, the wait state selection will be influenced by the DB16000A's CTTL frequency.

If the user intends to operate the DB16000A at CTTL frequencies other than factory configuration, it is advised to configure the PROM wait states for the highest anticipated operating frequency. This ensures proper compensation at lower frequencies.

NOTE: On-board I/O wait compensation is also effected by CTTL variation. Refer the Section 5.2.1.

Table 5-4 contains wait state requirements and W3 jumper settings for various PROM maximum access times versus CTTL frequency. Factory configuration is for 450 nsec access time.

To set up the required compensation:

1. Determine the maximum access time of devices installed in either bank.

2. If the slowest device exceeds 450 nsec access, reconfiguration is necessary. If not, reconfiguration is optional.

3. Remove any jumpers installed in W3 jumper 3 to 4, 7 to 8, or 9 to 10.

4. Referring to Table 5-4, install the required W3 jumpers.

5.2.3 Serial I/O

The following sections describe procedures to alter each serial port:

- Clock source and baud rate
- DTE/DCE configuration
- Handshake signal usage

While both ports are capable of synchronous or asynchronous data communication, the option procedures deal with asynchronous operation only. The procedures further assume each port's transmit baud rate to equal its receive baud rate.

Figure 5-5 shows the location of option items.

Clock Sources and Baud Rate Configuration (W29, W34). Each port may receive baud clocks from three sources:

- External source-synchronous modes, only
- Gang clock-a clock signal available to both ports
- PIT-a programmed clock signal from the PIT; one for each port

TABLE 5-4 PROM WAIT STATE COMPENSATION

PROM T_{ACC}, MAX.	6 MHZ CTTL	W3 JUMPERS	10 MHZ CTTL	W3 JUMPERS
250 nsec or less	0	None	1	3-4
300 nsec or less	0	None	2	7-8
350 nsec or less	0	None	2	7-8
400 nsec or less	1	3-4	3	3-4, 7-8
450 nsec or less	1	3-4	3	3-4, 7-8
500 nsec or less	1	3-4	4	9-10
550 nsec or less	2	7-8	4	9-10
600 nsec or less	2	7-8	5	3-4, 9-10
650 nsec or less	2	7-8	5	3-4, 9-10
700 nsec or less	2	7-8	6	7-8, 9-10
750 nsec or less	3	3-4, 7-8	6	7-8, 9-10
800 nsec or less	3	3-4, 7-8	7	3-4, 7-8, 9-10
850 nsec or less	3	3-4, 7-8	7	3-4, 7-8, 9-10
900 nsec or less	4	9-10	NA	
950 nsec or less	4	9-10	NA	

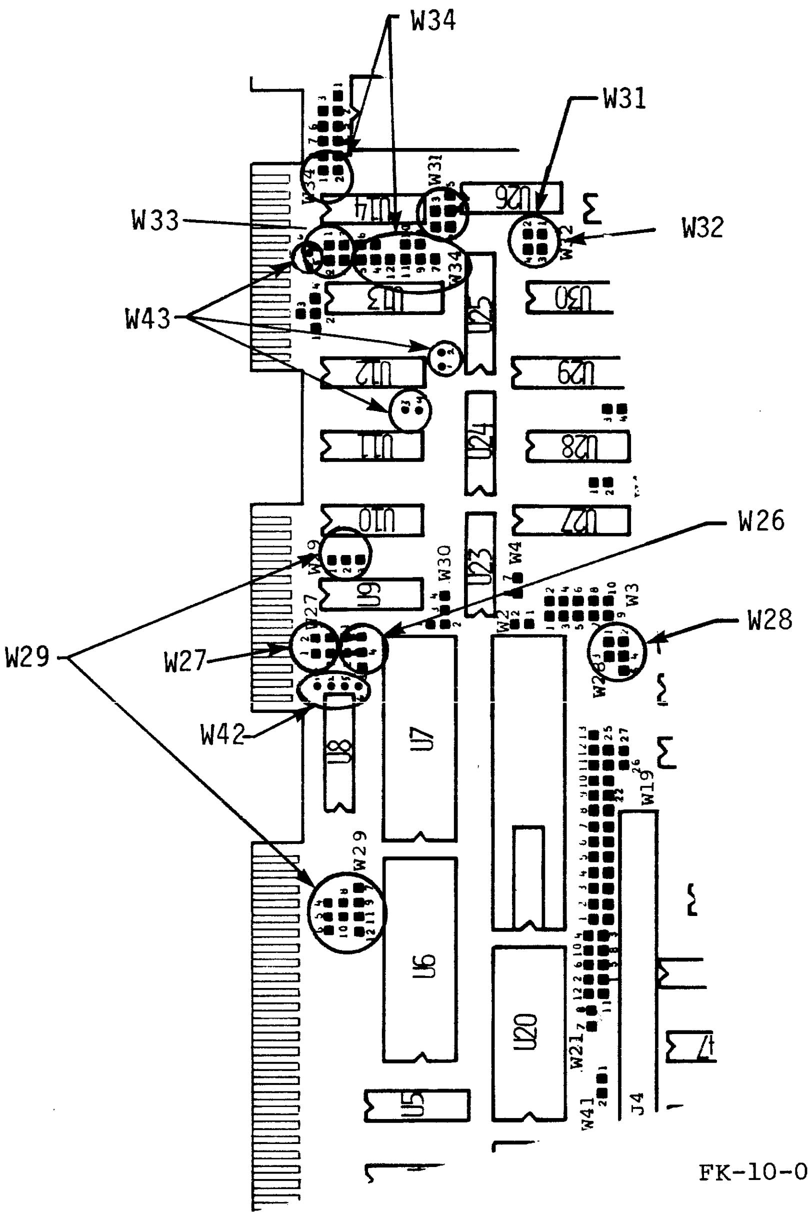


Figure 5-5 Serial I/O Option Items

The gang clock line originates from the DB16000A's ICU (NS16202) cluster. If the ICU is installed, the clock rate is programmable and driven by the ICU's clock pin (pin 29). If the ICU is not installed, the gang line may be driven by a 74LS92 inserted in socket U22. In this case, the gang clock frequency is fixed at 153.6 kHz.

Two of the PIT's counter outputs are available for jumper connection as baud clock inputs to the serial ports. The easiest configuration for the PIT counters is to connect PIT counter 1 output to Port 1 and connect PIT counter 2 output to Port 0. The connection can be reversed (e.g. counter 1 to Port 0), but requires wire-wrap to make the connection.

In factory-configuration, both ports are configured to use the gang clock line. To operate the ports at unequal baud rates, one or both of the ports must be optioned to use a PIT counter as its baud clock source.

NOTE: If diagnostic mode is entered, the hardware will automatically gate the gang clock line to each serial port clock input regardless of jumper selections.

CONNECTING PORT 0 CLOCK INPUT TO PIT COUNTER 2

1. Remove W29 jumper 4 to 5
2. Install W29 jumper 5 to 6

CONNECTING PORT 0 CLOCK INPUT TO PIT COUNTER 1

1. Remove W29 jumper 4 to 5
2. Wire wrap W29 Post 5 to W34 Post 6

CONNECTING PORT 1 CLOCK INPUT TO PIT COUNTER 1

1. Remove W34 jumper 4 to 5
2. Install W34 jumper 5 to 6

CONNECTING PORT 1 CLOCK INPUT TO PIT COUNTER 2

1. Remove W34 jumper 4 to 5
2. Wire wrap W34 Post 5 to W29 Post 6

Programming Note: Both TDS16A and MON16 on-board software will automatically configure the NS16202 ICU to drive the gang clock line. The clock frequency will be 16 times the baud rate indicated by the DB16000A's configuration switch settings (e.g., 153.6 KHz for 9600 baud).

If Port 1 is operated at some frequency other than the Port 0 baud rate, perform the following:

1. Connect Port 1 to either PIT counter 1 or PIT counter 2
2. Power up and initialize the DB16000A
3. Perform one of the following software patches:

   a) If PIT counter 1 was selected,

```
CMB C00056=76     ;sets PIT mode to load counter 1
CMB C00052=b1     ;loads LSB of count divisor into counter 1
CMB C00052=b2     ;loads MSB of count divisor into counter 1
```

   b) If PIT counter 2 was selected,

```
CMB C00056=B6     ;sets PIT mode to load counter 2
CMB C00054=b1     ;loads LSB of count divisor into counter 2
CMB C00054=b2     ;loads MSB of count divisor into counter 2
```

The count divisor is the hexadecimal value of 76800 ÷ baud rate.

DTE and DCE Configuration (W26, W27, W28, W31, W32, W33). In factory configuration, Port 0 is configured as DCE (Data Communication Equipment), and Port 1 is configured as DTE (Data Terminal Equipment). Figures 5-6 and 5-7 show Port 0 configured as DCE and Port 1 configured as DTE respectively.

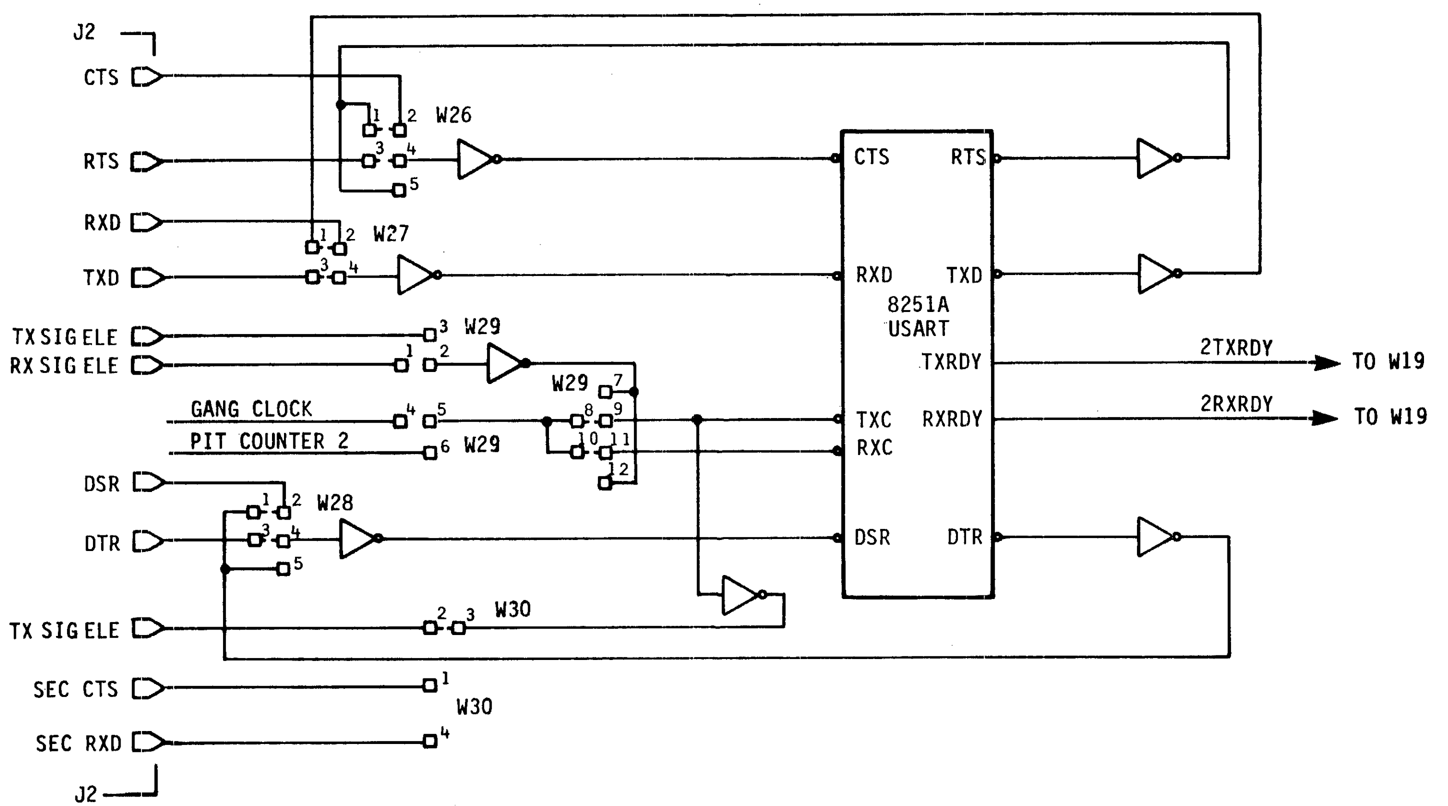
CONFIGURING PORT 0 TO BE DTE

1. Remove W26 jumpers 1 to 2 and 3 to 4
2. Install W26 jumpers 1 to 3 and 2 to 4
3. Remove W27 jumpers 1 to 2 and 3 to 4
4. Install W27 jumpers 1 to 3 and 2 to 4
5. Remove W28 jumpers 1 to 2 and 3 to 4
6. Install W28 jumpers 1 to 3 and 2 to 4

CONFIGURING PORT 1 TO BE DCE

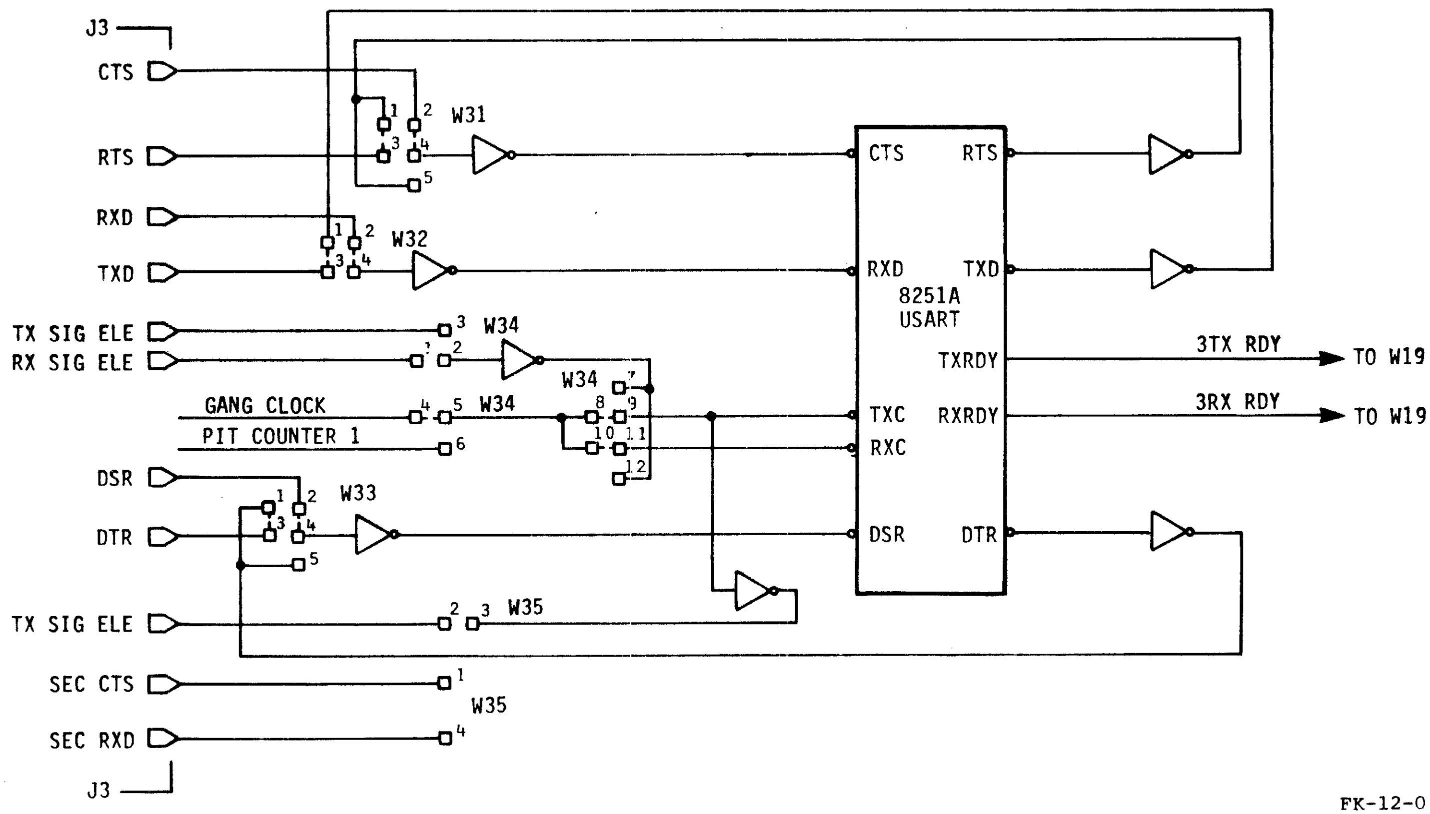
1. Remove W31 jumpers 1 to 3 and 2 to 4
2. Install W31 jumpers 1 to 2 and 3 to 4
3. Remove W32 jumpers 1 to 3 and 2 to 4
4. Install W32 jumpers 1 to 2 and 3 to 4
5. Remove W33 jumpers 1 to 3 and 2 to 4
6. Install W33 jumpers 1 to 2 and 3 to 4

Handshake Signal Loop-back (W26, W28, W31, W33). In factory-configuration, Port 0 and 1 expect RTS/CTS and DSR/DTR handshake signals to be used. If the corresponding terminal or host RS232 interface does not support these signals, they must be looped back.



Note: ◻-◻ Indicates factory configuration for DCE

Figure 5-6 Factory Configuration, DCE Port 0



Note: ▫-▫ Indicates factory configuration for DTE

Figure 5-7 Factory Configuration, DTE Port 1

PORT 0 HANDSHAKE LOOP-BACK

1. Remove all W26 jumpers and set aside
2. Install W26 jumper 4 to 5, this loops RTS to CTS
3. Remove all W28 jumpers and set aside
4. Install W28 jumper 4 to 5, this loops DSR to DTR

PORT 1 HANDSHAKE LOOP-BACK

1. Remove all W31 jumpers and set aside
2. Install W31 jumper 4 to 5, this loops RTS to CTS
3. Remove all W33 jumpers and set aside
4. Install W33 jumper 4 to 5, this loops DSR to DTR

5.2.4 Parallel I/O (PIO)

The 8255A programmable perpheral interface provides 24 interface signals for use in expanding the DB16000A's I/O capabilites. The 24 lines are organized as three 8-bit ports; Port A, Port B, and Port C. The function of each port is under program control.

Hardware option items include:

- Port A direction control
- Port B and C driver or terminator choices
- Use of Port C bits as interrupt inputs

Figure 5-8 depicts the location of hardware option items. Figure 5-9 is a block diagram of the parallel interface.

Port A Driver/Receiver Direction (W23). An 8303 transceiver installed in U1 completes the signal path between Port A and J1. In factory-configuration, U1's direction is controlled by the content of Port C, bit 6 (PC6). If PC6=0, U1 will operate as an output driver. If PC6=1, U1 will function as a receiver.

Optionally, U1 can be configured to operate as a driver or receiver.

U1 AS A DRIVER

1. Remove W23 jumper 3 to 4
2. Install W23 jumper 2 to 3

U1 AS A RECEIVER

1. Remove W23 jumper 3 to 4
2. Install W23 jumper 1 to 3

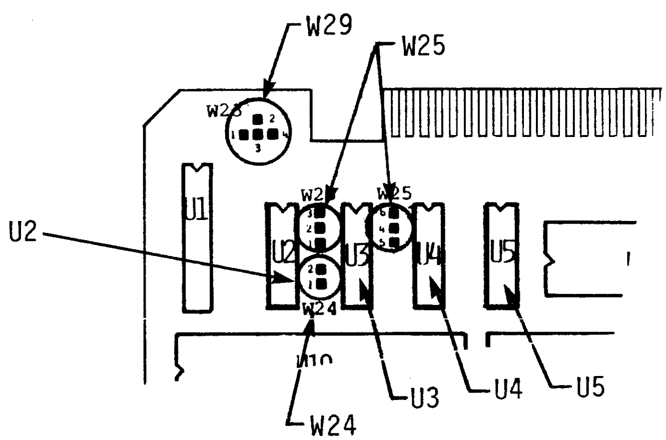


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Figure 5-8 PIO Option Items

Port B and Port C Driver/Terminators (U2, U3, U4, U5). Driver/Terminator sockets complete the signal path between J1 and Ports B and C. Ports B and C are each connected to two 14-pin sockets. Each socket will accept either a driver or resistor terminator. If a resistor terminator is installed, signals at the interface connector J1 are restricted to TTL levels for the port in question. If drivers are installed, the user may choose among a variety of totem-pole or open collector devices.

Port B is considered to be a single 8-bit port. Therefore, sockets connected to it (U4 and U5) must both contain either drivers or terminators.

Port C can be configured as two 4-bit ports. PC0 through PC3 are connected to U3. PC4 through PC7 are connected to U2. Each socket may have either a driver or terminator installed.

COMPATIBLE DRIVERS

The following is a list of compatible drivers:

7400	inverting output, 16 mA sink
7403	inverting open collector output, 16 mA sink
7408	noninverting output, 16 mA sink
7409	noninverting open collector output, 16 mA sink
7426	inverting open collector output, 16 mA sink
7432	noninverting output, 16 mA sink
7437	inverting output, 48 mA sink
7438	inverting open collector output, 48 mA sink

In factory-configuration, 7437's are installed in U2 through U5.

COMPATIBLE TERMINATORS

BLC 901-220 ohm/330 ohm dividers
BLC 902-1k ohm pullups

NOTE: When a terminator is installed in U2, it is possible for the external peripheral device connected to J1 to control Port A's transceiver direction. Refer to Figure 5-9.

Port C Interupt Inputs (U2, U3, W25). The 8255A permits use of Port C bits as external interrupt requests to the DB16000A. The bits in question are PC0 and PC3. To utilize these bits as interrupt inputs, the user must relinquish their use as signals connected to U3. Further, a terminator must be installed in U2 and U3.

PC0 as INTERRUPT INPUT

1. Remove W25 jumper 2 to 3
2. Install W25 jumper 1 to 2

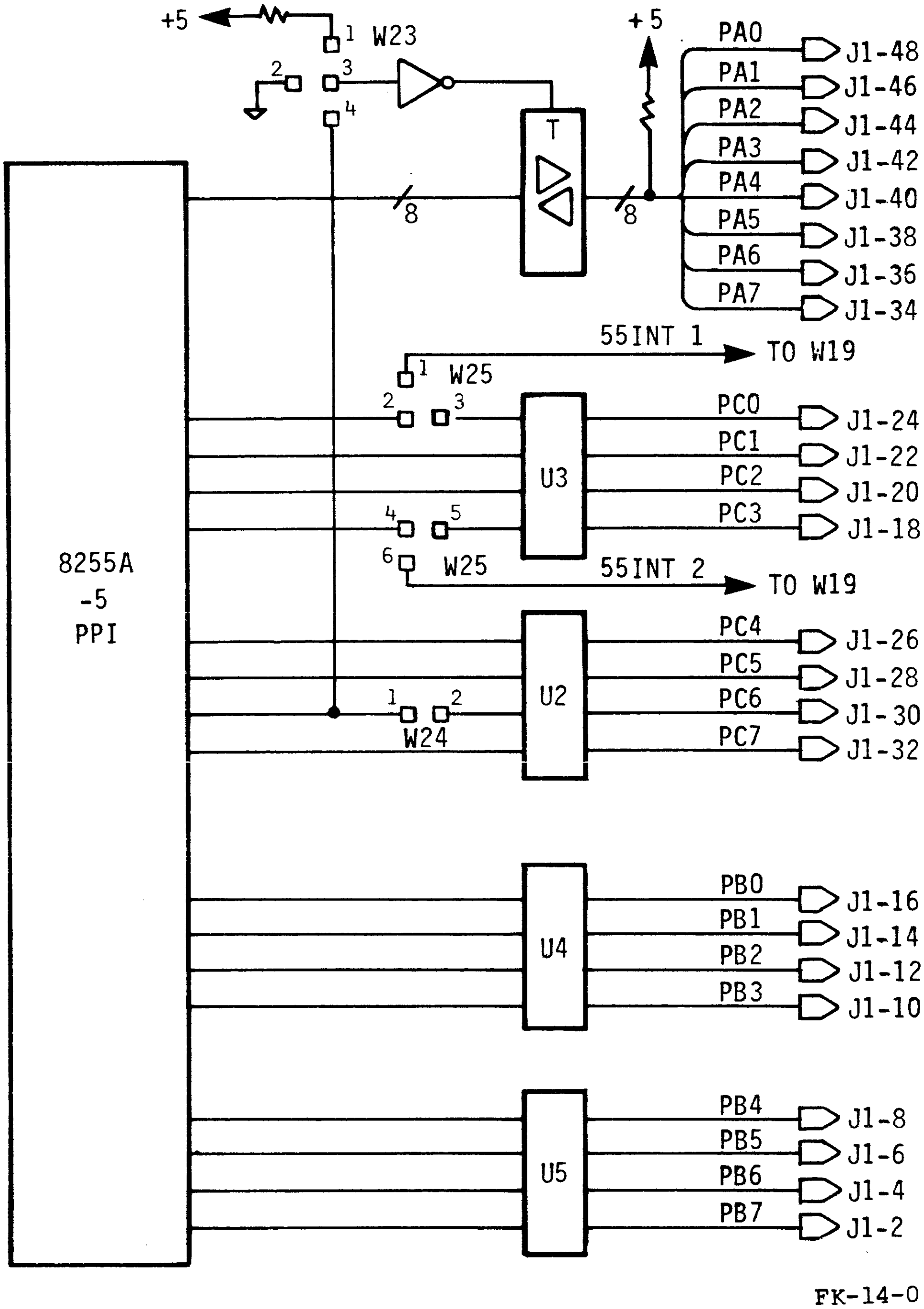


Figure 5-9 PIO Block Diagram

PC3 as INTERRUPT INPUT

1. Remove W25 jumper 4 to 5
2. Install W25 jumper 5 to 6

PC0 and PC3 are now available as potential NS16202 ICU input in the W19 jumper field. Refer to Section 5.2.1.

5.2.5 MULTIBUS I/O

The DB16000A is factory-configured to operate by itself with no I/O devices accessible via its MULTIBUS interface. In this case, the DB16000A's RAM is assumed private to its CPU and no off-board accesses are required.

If the MULTIBUS I/O capability is to be used, the following options must be configured:

- Arbitration
- Interrupts
- Dual-Port RAM
- Bus Clocks

The exact choice of options is dependent on the system configuration in which the DB16000A is to function.

Figure 5-10 depicts the location of option items.

Arbitration Options (W9, W10, W40). The user must configure the DB16000A's bus arbitration logic for the following:

- Serial or parallel priority resolution
- Whether or not system override will be invoked
- Whether or not common bus request (CBRQ/) will be used

SERIAL VERSUS PARALLEL PRIORITY RESOLUTION (W10)

The DB16000A is factory-configured for serial resolution. If parallel resolution is implemented, the board must be reconfigured to disconnect to BPRO/ signal from the DB16000A bus arbiter; the central arbiter will want to drive this signal.

For parallel resolution, remove W10 jumper 1 to 2 and set aside.

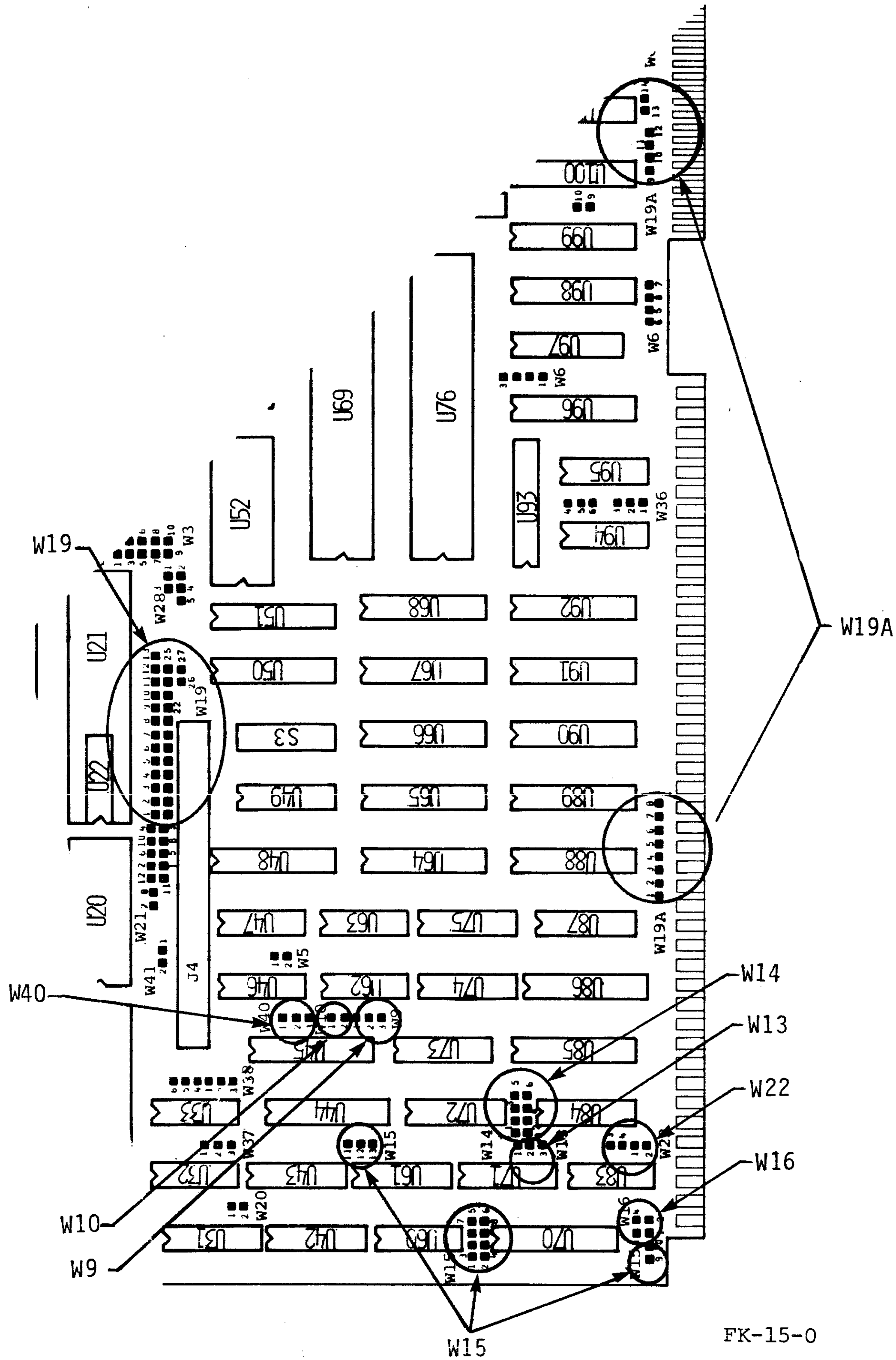


Figure 5-10 MULTIBUS I/O Option Items

SYSTEM OVERRIDE (LOCK/) (W40)

The DB16000A is factory-configured to assume no other bus master can access system semaphores kept in RAM (i.e. there is no other bus master, or no master will attempt access to the information).

If the system is to be configured for use of common semaphore areas, all masters must assert the bus override condition (LOCK/) before accessing the semaphore. LOCK/ can only be asserted when the master has acquired the bus. This means the master must wait until the bus is granted, even if the locked access is to its on-board dual-port RAM. Furthermore, when LOCK/ is asserted, no master can access its own dual-port RAM (i.e., LOCK/ can freeze the system).

The DB16000A will attempt to override the system whenever:

- Software override is asserted via the configuration register
- An interlocked instruction is executed
- The NS16082 is installed and it asserts the FLT signal to access page tables (refer to Section 5.2.1)

In factory configuration, the DB16000A always assumes immediate success in overriding the system. On-board RAM accesses proceed without waiting for bus arbitration.

If common semaphores are to be implemented, enable the use of the MULTIBUS LOCK/ signal:

1. Remove W40 jumper 2 to 3
2. Install W40 jumper 1 to 2

COMMON BUS REQUEST (CBRQ/) (W9)

The DB16000A is factory configured to arbitrate for the bus, for each off-board access. Once the access is completed, it will relinquish the bus.

If there is no other bus master, or if all bus masters support use of CBRQ/, the DB16000A's bus transactions can be optimized. This is done by enabling the CBRQ/ signal to the DB16000A bus arbiter. As long as the CBRQ/ signal is not asserted by another bus master, the DB16000A will retain the bus saving arbitration time.

To enable CBRQ/:

1. Remove W9 jumper 1 to 2
2. Install W9 jumper 2 to 3

INTERRUPT OPTIONS (W19, W19A)

When the NS16202 ICU is installed, the DB16000A can be configured to accept non-bus vectored MULTIBUS interrupts from other MULTIBUS boards.

A wire-wrap jumper field, W19A Posts 1 through 7, is connected to MULTIBUS interrupt signals INT0/ through INT7/. These signals may be connected to ICU interrupt input posts as required. Note that INT0/ is the highest priority MULTIBUS interrupt and IR0 is the highest priority ICU interrupt input.

Refer to Figure 5-2 for pertinent W19 and W19A post assignments.

NOTE: ICU acceptance and processing of interrupts is entirely under program control.

Dual-Port RAM (W13, W14, W15, W16). The user may configure the DB16000A's RAM controller and slave address decoder to:

- Enable dual-port access
- Select the megabyte address range
- Select the starting address within the selected megabyte
- Enforce privacy for a fraction of on-board RAM

ENABLING DUAL PORT ACCESS (W13)

In the factory-configuration, the DB16000A's slave address decoder is disabled making all on-board RAM private to the CPU.

To enable the slave address decoder, remove W13 jumper 1 to 2 and set aside.

MEGABYTE ADDRESS RANGE ENABLE (W13)

If the system supports use of MULTIBUS address bits ADR14/ through ADR17/, enable the megabyte range decoder.

To enable the megabyte decoder, install W13 jumper 2 to 3. If the decoder is not enabled, the system address of on-board RAM is restricted to 000000H-0FFFFFH.

MEGABYTE ADDRESS SELECTION (W14)

In factory-configuration, the megabyte decoder is configured to respond to system address F00000H-FFFFFFH, if enabled. It can be configured to respond to any other megabyte address range, via W14 jumper selection. This option can be set only if the megabyte decoder is enabled.

Table 5-5 depicts the appropriate combinations of W14 jumper for each of the 16 possibilities.

TABLE 5-5 MEGABYTE RANGE SELECTION

W14 JUMPERS				MEGABYTE ADDRESS RANGE
1 to 2	3 to 4	5 to 6	7 to 8	
-	-	-	-	000000-0FFFFF
x	-	-	-	100000-1FFFFF
-	x	-	-	200000-2FFFFF
x	x	-	-	300000-3FFFFF
-	-	x	-	400000-4FFFFF
x	-	x	-	500000-5FFFFF
-	x	x	-	600000-6FFFFF
x	x	x	-	700000-7FFFFF
-	-	-	x	800000-8FFFFF
x	-	-	x	900000-9FFFFF
-	x	-	x	A00000-AFFFFF
x	x	-	x	B00000-BFFFFF
-	-	x	x	C00000-CFFFFF
x	-	x	x	D00000-DFFFFF
-	x	x	x	E00000-EFFFFF
x	x	x	x	F00000-FFFFFF

x indicates jumper

STARTING ADDRESS SELECTION (W15)

The system address within the selected megabyte of on-board RAM is mappable in 32K-byte increments anywhere within the active megabyte range.

In factory-configuration, the starting system address begins at 000000H. This can be adjusted upward in 32K byte increments via appropriate selection of W15 jumpers.

Table 5-6 depicts combinations of W15 jumpers for all possible starting addresses.

Note that selection of starting addresses XE8000, XF0000, and XF8000, progressively force the 128K on-board RAM out of MULTIBUS address range. Dual-port RAM address cannot cross a megabyte boundary.

PRIVACY SELECTION (W16)

In factory-configuration, all on-board RAM is accessible from the MULTIBUS interface if the dual port is enabled. The user may choose to make only a fraction of the RAM available to MULTIBUS access, reserving the rest as private to the CPU.

Table 5-7 depicts combinations of W16 jumpers to permit MULTIBUS access in increments of one-quarter RAM capacity.

Bus Clocks (W22). Bus clock signals, BCLK/ and CCLK/, must originate from one bus master only.

In factory-configuraton, the DB16000A will supply the bus clocks.

If it is desired to allow another bus master to drive the bus clocks, remove W22 jumpers 1 to 2 and 3 to 4 and set them aside.

5.2.6 BLX I/O (J4, W38, W41)

The DB16000A permits installation of one BLX I/O expansion module via connector J4. BLX modules with 8-bit data paths may be installed regardless of the DB16000A CPU configuration. Figure 5-11 depicts the location of option items.

If a 16-bit BLX module is installed, the NS08032 CPU cannot interface to it properly because the NS08032 has an 8-bit data path.

8-BIT BLX INSTALLATION (J4)

The BLX module plugs directly into the female J4 connector on the DB16000A. The module is then secured at an additional point with additional nylon hardware to ensure the mechanical security of the assembly.

TABLE 5-6 DUAL-PORT START ADDRESS SELECTION

W15 JUMPERS							STARTING BOUNDARY
1 to 2	3 to 4	5 to 6	7 to 8	9 to 10	11 to 12	12 to 13	
x	x	x	x	x	-	x	00000
-	x	x	x	x	x	-	08000
x	-	x	x	x	-	x	10000
-	-	x	x	x	x	-	18000
x	x	-	x	x	-	x	20000
-	x	-	x	x	x	-	28000
x	-	-	x	x	-	x	30000
-	-	-	x	x	x	-	38000
x	x	x	-	x	-	x	40000
-	x	x	-	x	x	-	48000
x	-	x	-	x	-	x	50000
-	-	x	-	x	x	-	58000
x	x	-	-	x	-	x	60000
-	x	-	-	x	x	-	68000
x	-	-	-	x	-	x	70000
-	-	-	-	x	x	-	78000
x	x	x	x	-	-	x	80000
-	x	x	x	-	x	-	88000
x	-	x	x	-	-	x	90000
-	-	x	x	-	x	-	98000
x	x	-	x	-	-	x	A0000
-	x	-	x	-	x	-	A8000
x	-	-	x	-	-	x	B0000
-	-	-	x	-	x	-	B8000
x	x	x	-	-	-	x	C0000
-	x	x	-	-	x	-	C8000
x	-	x	-	-	-	x	D0000
-	-	x	-	-	x	-	D8000
x	x	-	-	-	-	x	E0000
-	x	-	-	-	x	-	E8000
x	-	-	-	-	-	x	F0000
-	-	-	-	-	x	-	F8000

x indicates jumper

TABLE 5-7 DUAL-PORT PRIVACY SELECTION

W16 JUMPERS		ACCESSIBLE FRACTION	
1 to 2	3 to 4		
x	x	first 1/4	32K
-	x	first 1/2	64K
x	-	first 3/4	96K
-	-	all	128K

x indicates jumper

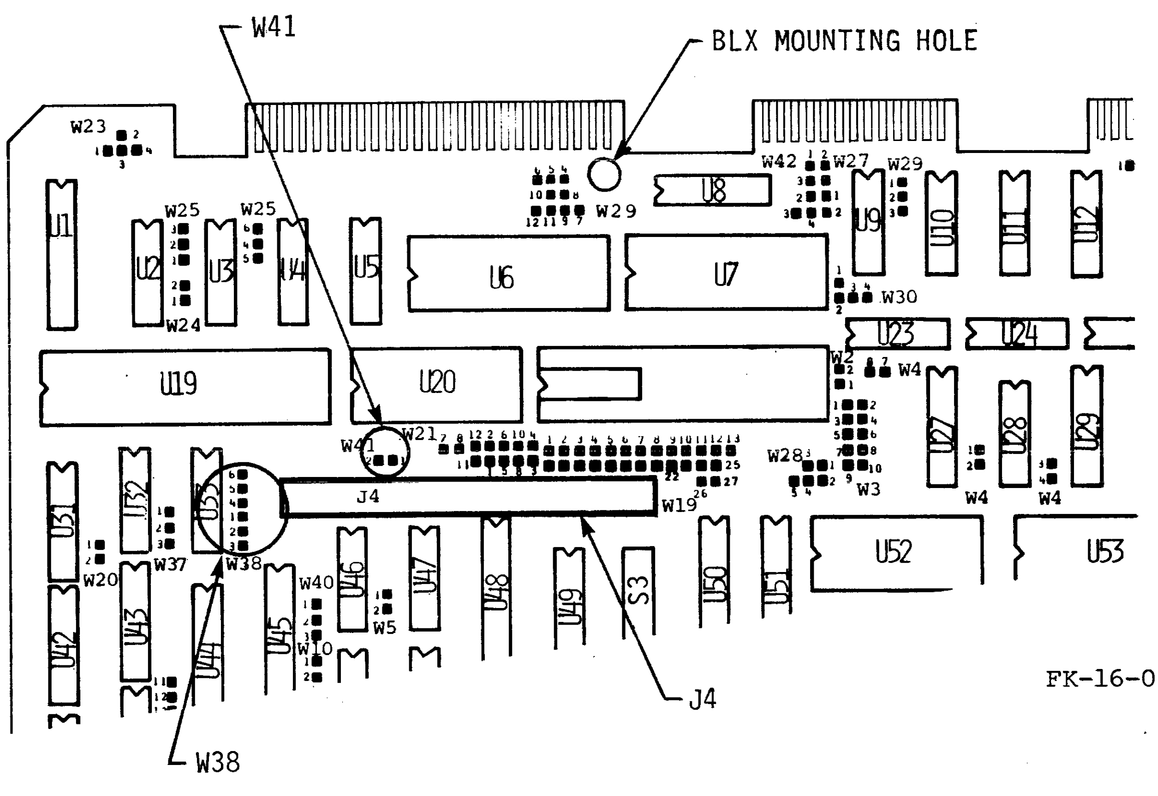


Figure 5-11 BLX Option Items

16-BIT BLX INSTALLATION (W38)

Install the BLX as described. The DB16000A is factory-configured for 8-bit BLX modules; therefore, some jumper reconfiguration is necessary:

1. Remove W38 jumpers 1 to 2 and 4 to 5
2. Install W38 jumpers 2 to 3 and 5 to 6

BLX OPT 0 AND OPT 1 SIGNAL CONNECTION (W41)

When a BLX module is installed, certain of the module's signals are designated as optional to basic operation. These signals are presented to the DB16000A via J4. The user may connect these signals via wire-wrap jumpers to implement additional functions (e.g. ICU interrupt inputs).

Signal assignment:

OPT 0	W41 Post 2
OPT 1	W41 Post 1

5.3 OPTION SUMMARY

The following sections contain tabular information describing all DB16000A jumper and socket options. The information is provided for quick reference and should be used in conjunction with informantion provided in Chapter 2 and Chapter 5 (Sections 5.1 and 5.2).

5.3.1 Jumper Option Tabulation

Jumper options are listed in Table 5-8. Figure 5-12 shows the location of each jumper on the board.

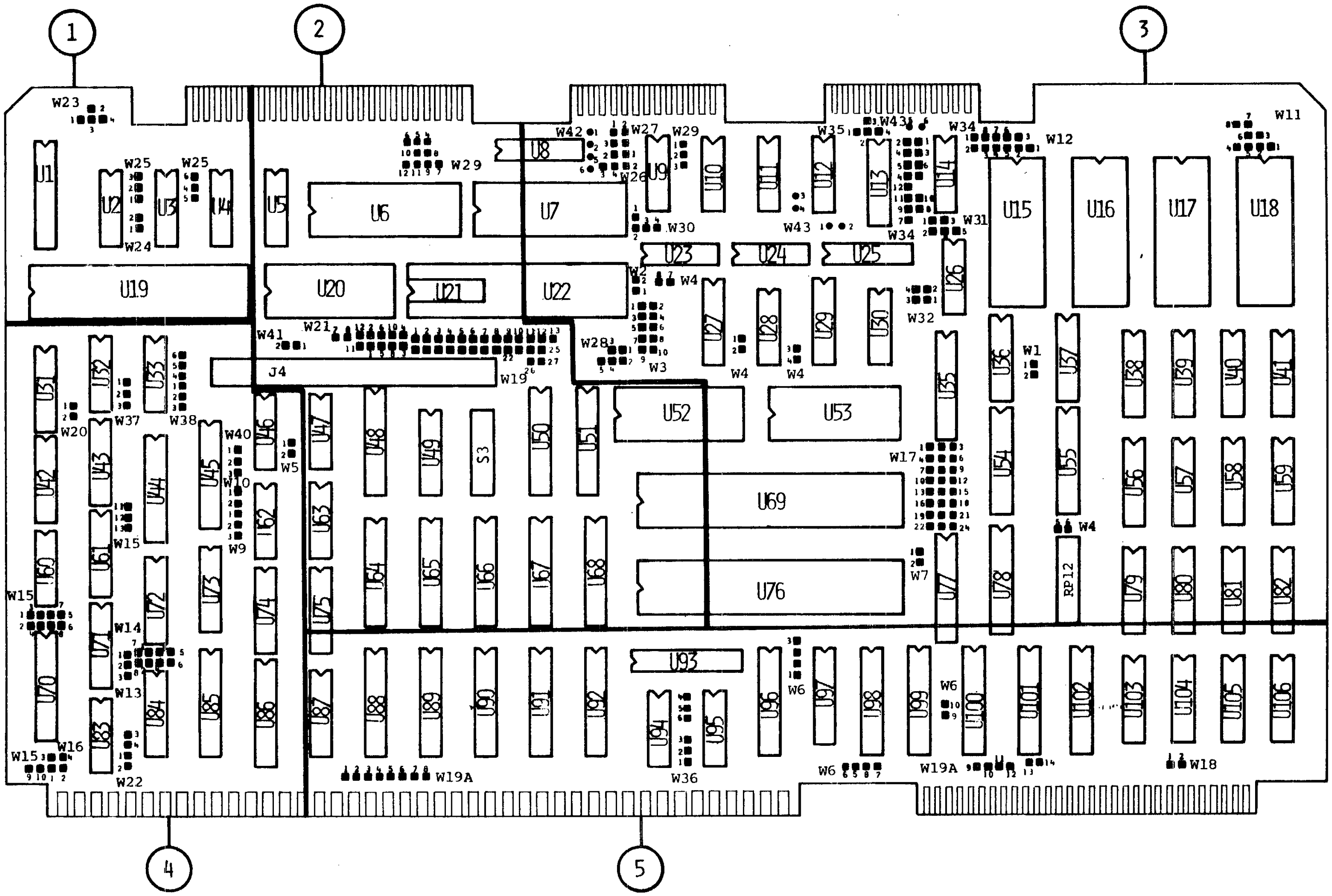
5.3.2 Socketed Option Tabulation

Socketed options appear in Table 5-9.

5.3.3 Standard Shipping Configurations

The DB16000A is available in two versions at the time of this writing. Both versions are configured from the same basic board assembly. The difference between the two versions are confined to operating speed and NS16000 family mix.

Model DB16000A-006 is configured for operation at 6 MHz, with NS16032 and NS16201 installed. Model DB16000A-110 is configured for operation at 10 MHz, with NS16032, NS16201, NS16081, NS16082, and NS16202 installed. Table 5-10 lists factory-configured jumper and socket options for both models of DB16000A.



FK-17-0

Figure 5-12 Jumper Locations

JUMPER NUMBER	FIELD AREA	FUNCTION	DESCRIPTION
W1	3	CPU Time	When connected, 1-2 connects the on-board TTL oscillator, U30, to NS16201 TCU input.
W2	3	Wait 1	Connects CWAIT/ to CWAIT1 input so all CWAIT states end with a WAITN (n=1), reference 16201-10, Rev. B user information sheet. Jumper 1-2 enables additonal wait state. Remove Jumper 1-2 to disable additional wait state.
W3	3	On-Board I/O Wait States	Selects wait states for on-board I/O, and EPROM as follows: # Wait States — I/O — EPROM 0 — None — None 1 — 1-2 — 3-4 2 — 5-6 — 7-8 3 — 1-2 & 5-6 — 3-4 & 7-8 4 — n/a — 9-10 5 — n/a — 9-10 & 3-4 6 — n/a — 9-10 & 7-8 7 — n/a — 9-10, 3-4, & 7-8
W4	3	MMU	Configures for presence or absence of MMU and FLT/ connection to LOCK/. With no MMU installed, 1-2, 3-4 and 5-6 must be installed and 7-8 determines if FLT/ drives bus over-ride and LOCK/. With 7-8 installed, FLT/ drives bus override and LOCK/; with 7-8 removed it does not.
W5	4	CPU	Selects state of HBE/. Install jumper 1-2 for 16032 CPU, remove jumper for 08032. (See also jumpers W17 and W37 for 16032/0832 configuration.)

TABLE 5-8 (Cont.)

JUMPER NUMBER	FIELD AREA	FUNCTION	DESCRIPTION
W6	5	PROM Banks	Selects PROM size and locations according to the following table (X indicates jumper installed): (See also W11 & W12.)

LOWER BANK (U15 & U18) JUMPER 9-10	7-8	SIZE	RANGE	UPPER BANK (U16 & U17) JUMPER 5-6	3-4	1-2	SIZE	RANGE
X	X	2716	0-0FFF					
X		2732	0-1FFF					
	X	2764	0-3FFF					
		27128	0-7FFF					
X	X	2716	0-0FFF	X	X	X	2716	001000-001FFF
X	X	2716	0-0FFF	X	X		2732	002000-003FFF
X	X	2716	0-0FFF	X		X	2764	004000-007FFF
X		2732	0-1FFF	X	X	X	2716	002000-002FFF
X		2732	0-1FFF	X	X		2732	002000-003FFF
X		2732	0-1FFF	X		X	2764	004000-007FFF
	X	2764	0-3FFF	X	X	X	2716	004000-004FFF
	X	2764	0-3FFF	X	X		2732	004000-005FFF
	X	2764	0-3FFF	X		X	2764	004000-007FFF
		27128	0-7FFF					
		27128	0-7FFF					
		27128	0-7FFF					
				X			2716	D00000-D00FFF
					X	X	2732	D00000-D01FFF
					X		2764	D00000-D03FFF
						X	27128	D00000-D07FFF
							27256	D00000-D0FFFF

JUMPER NUMBER	FIELD AREA	FUNCTION	DESCRIPTION
W7	3	MMU	Enables/disables MMU interrupt input to processor NMI input. 1-2 installed enables, removed disables.
W9	4	CBRQ/ MULTIBUS	P1 CBRQ selection. When enabled (jumper 2-3), MULTIBUS arbitration logic will retain the MULTIBUS bus between bus operations as long as no other master is requesting bus access. When disabled (jumper 1-2), bus will be released after each bus transfer. CBRQ/ should never be used with (older) boards that do not implement CBRQ/.

TABLE 5-8 (Cont.)

JUMPER NUMBER	FIELD AREA	FUNCTION	DESCRIPTION
W10	4	BPRO/ MULTIBUS	Connects driver to BPRO/. Install jumper 1-2 for serial bus priority, remove jumper 1-2 for parallel bus priority.
W11, W12	3	PROM Type	Select size of EPROM. W11 and W12 have identical functions for the lower (U15 & U18) and upper (U17 & U18) EPROM banks, respectively. Size is according to the following table: (See also W6.) EPROM Type — W11 or W12 Jumpers Installed 2716 — 2-3, 5-6 2732 — 1-2, 5-6 2764 — 1-2, 6-7 27128 — 1-2, 4-5, 6-7 27256 — 1-2, 4-5, 7-8
W13	4	Dual Port Megabyte Enable	Dual port and megabyte address. Access to the on-board dual port RAM from the MULTIBUS is disabled (all on-board memory is private to the local CPU) when jumper 1-2 is installed. Dual port RAM will be enabled if no W13 jumper is installed or if jumper 2-3 is installed. With 2-3 installed, the slave memory responds to all 24 MULTIBUS address lines, including the megabyte address on P2 (ADR14/-ADR17/). With 2-3 removed, the megabyte address lines will be ignored when selecting slave access to the dual port RAM. This permits operation in systems that do not bus P2 but limits total MULTIBUS address space to 1 megabyte.

TABLE 5-8 (Cont.)

JUMPER NUMBER	FIELD AREA	FUNCTION	DESCRIPTION
W14	4	Dual Port Megabyte Range	Dual port megabyte select. (Relevant only if W13 2-3 is installed.) The megabyte address range of the dual port memory (of which the dual port address is a subset) is selected according to the following table (X indicates jumper installed):

1-2	3-4	5-6	7-8	Megabyte Address Range
				000000-0FFFFF
X				100000-1FFFFF
	X			200000-2FFFFF
X	X			300000-3FFFFF
		X		400000-4FFFFF
X		X		500000-5FFFFF
	X	X		600000-6FFFFF
X	X	X		700000-7FFFFF
			X	800000-8FFFFF
X			X	900000-9FFFFF
	X		X	A00000-AFFFFF
X	X		X	B00000-BFFFFF
		X	X	C00000-CFFFFF
X		X	X	D00000-DFFFFF
	X	X	X	E00000-EFFFFF
X	X	X	X	F00000-FFFFFF

TABLE 5-8 (Cont.)

JUMPER NUMBER	FIELD AREA	FUNCTION	DESCRIPTION
W15	4	Dual Port Start	W15 sets the starting 32K boundary of the dual port RAM within the megabyte selected by W14. Starting address is according to the following table (X indicates jumper installed):

1-2	3-4	5-6	7-8	9-10	11-12	12-13	STARTING BOUNDARY
X	X	X	X	X		X	00000
	X	X	X	X	X		08000
X		X	X	X		X	10000
		X	X	X	X		18000
X	X		X	X		X	20000
	X		X	X	X		28000
X			X	X		X	30000
			X	X	X		38000
X	X	X		X		X	40000
	X	X		X	X		48000
X		X		X		X	50000
		X		X	X		58000
X	X			X		X	60000
	X			X	X		68000
X				X		X	70000
				X	X		78000
X	X	X	X			X	80000
	X	X	X		X		88000
X		X	X			X	90000
		X	X		X		98000
X	X		X			X	A0000
	X		X		X		A8000
X			X			X	B0000
			X		X		B8000
X	X	X				X	C0000
	X	X			X		C8000
X		X				X	D0000
		X			X		D8000
X	X					X	E0000
	X				X		E8000
X						X	F0000
					X		F8000

TABLE 5-8 (Cont.)

JUMPER NUMBER	FIELD AREA	FUNCTION	DESCRIPTION
W16	4	Dual-Port Privacy	Sets amount of the dual port RAM that can be accessed from the MULTIBUS interface according to the following table (note that the fraction 0 (none) can be accomplished with W13). 1-2 / 3-4 / ACCESSIBLE FRACTION / 64K DEVICES X / X / first 1/4 / 32K bytes — / X / first 1/2 / 64K bytes X / — / first 3/4 / 96K bytes — / — / all / 128K bytes
W17	3	CPU	Configures ROM for 8 or 16 bit CPU. (See also W5 and W37.) Jumper as follows: CPU / JUMPERS 08032 / 2-3,5-6,8-9,11-12,14-15,17-18,20-21,23-24 16032 / 1-2,4-5,7-8,10-11,13-14,16-17,19-20,22-23
W18	5	Reserved	Used to connect address drive to pin 1 of dynamic RAMs. Used only for 256K RAM devices.
W19	2	ICU	Interrupt matrix. Refer to Figure 5-2.
W20	4	I/O Time Base	When installed, 1-2 connects on-board TTL oscillator, U32, to produce I/O time base.
W21	2	PIT	Normally, jumpers are installed in 1-2, 3-4, 5-6, 7-8, 9-10 and 11-12. Special applications of the programmable interval timer (U20) can be accomplished by changing these.
W22	4	MULTIBUS Clocks	1-2 connects CCLK/ driver to MULTIBUS. 3-4 connects BCLK/ driver to Multibus. In a system with multiple bus masters, only one can have these jumpers installed.
W23	1	PIO Port A	Selects source of direction control on Port A bidirectional buffer: JUMPER / DIRECTION 1-3 / Port A is input 2-3 / Port A is output 3-4 / Port A direction controlled by PC6
W24	1	PIO Port A	Removal of jumper 1-2 disconnects PC6 from the interface connection. Refer to Figure 5-9.

TABLE 5-8 (Cont.)

JUMPER NUMBER	FIELD AREA	FUNCTION	
W25	1	PIO Interrupt	Selects source of PPI interrupt source for the interrupt matrix. Refer to Figure 5-9.
W26	3	SIO Port 0	Request to Send and Clear to Send configuration for DTE, DCE or loop back as follows for serial J2: DTE 1-3,2-4 DCE 1-2,3-4 loop back 4-5
W27	3	SIO Port 0	Transmitted data and Received data configuration for DTE or DCE for serial port J2 as follows: DTE 1-3,2-4 DCE 1-2,3-4
W28	3	SIO Port 0	Data Terminal Ready and Data Set Ready configuration for DTE, DCE or loop back for serial port J2 as follows: DTE 1-3,2-4v DCE 1-2,3-4 loop back 4-5
W29	3	SIO	Selects baud clock for serial port J2. Refer to Figure 5-6.
W30	3	SIO	Selects transmitter clock output for serial port J2. Refer to Figure 5-6.
W31	3	SIO Port 1	Request to Send and Clear to Send configuration for DTE, DCE or loop back as follows for serial port J3: DTE 1-3,2-4 DCE 1-2,3-4 loop back 4-5
W32	3	SIO Port 1	Transmitted data and Received data configuration for DTE or DCE for serial port J3 as follows: DTE 1-3,2-4 DCE 1-2,3-4
W33	3	SIO	Data Terminal Ready and Data Set Ready configuration DTE, DCE or loop back for serial port J3 as follows: DTE 1-3,2-4 DCE 1-2,3-4 loop back 4-5

TABLE 5-8 (Cont.)

JUMPER NUMBER	FIELD AREA	FUNCTION	DESCRIPTION
W34	3	SIO Port 1	Selects baud clock for serial port J3. Refer to Figure 5-7.
W35	3	SIO Port 1	Selects transmitter clock output for serial port J3. Refer to Figure 5-7
W36	5	Reserved	Selects delay line signals for dynamic RAM timing.
W37	4	CPU	Selects odd enable signal for PROM enables, jumper 1-2 for 16032 installed, 2-3 for 08032 installed. (See also W5 and W17.)
W38	4	BLX	Selects 8 or 16 bit BLX expansion module according to the following table: CPU / MODULE SIZE / JUMPERS 16032 / 8 bit / 1-2,4-5 08032 / 8 bit / 1-2,4-5 16032 / 16 bit / 2-3,5-6 08032 / 16 bit / NOT PERMITTED
W40	4	MULTIBUS LOCK/	Installed from 1-2 for normal operation. Can be connected from 2-3 to insure bus arbiter will not block local access for operation in non-Multibus system.
W41	2	BLX OPT0 and OPT1	Option jumpers for BLX expansion interface.
W42	3	Port 0 TTY Power	Power for TTY interface. 1-2 connects J2 pin 23 to +5 VDC 3-4 connects J2 pin 19 to -12 VDC 5-6 connects J2 pin 22 to +12 VDC
W42	3	Port 1 TTY Power	Power for TTY interface. 1-2 connects J3 pin 22 to +12 VDC 3-4 connects J3 pin 23 to +5 VDC 5-6 connects J3 pin 19 to -12 VDC

TABLE 5-9 SOCKETED OPTIONS

JUMPER NUMBER	FUNCTION	DESCRIPTION
U2-U5	Driver/ Terminator	PIO Ports B and C. 7437 normally installed.
U21	NS16202 ICU	Interrupt Control Unit. May be installed only if U22 is vacant.
U22	74LS92	Gang Clock Hardware Counter. May be installed only if U21 is vacant.
U30	TTL Oscillator	CPU Time Base. TTL compatible output oscillator.
U52	NS16081 FPU	Floating-Point Unit.
U64	DS8303	Installed with NS08032 CPU. Vacant with NS16032 CPU.
U69	CPU	NS16032 or NS08032.
U76	NS16082 MMU	Memory Management Unit.
U86	DS8304	Installed with NS16032 CPU. Vacant with NS08032 CPU.
U88	DS8303	Installed with NS16032 CPU. Vacant with NS08032 CPU.

TABLE 5-10 FACTORY-CONFIGURED JUMPER AND SOCKET OPTIONS MODEL

JUMPER OR SOCKET	FUNCTION	MODEL -006	MODEL -110
W1	CPU Time Base	1-2	1-2
W2	Add 1 Wait 1	1-2	1-2
W3	Wait States	1-2,3-4	5-6,3-4,7-8
W4	MMU	1-2,3-4,5-6	7-8
W5	CPU HBE	1-2	1-2
W6	PROM Add	1-2	1-2
W7	MMU	None	1-2
W9	CBRQ/	~~1-2~~ 2-3	1-2
W10	BPRO/	1-2	1-2
W11	PROM Type Lower Bank	1-2,4-5,6-7	1-2,4-5,6-7
W12	PROM Type Upper Bank	1-2,4-5,6-7	1-2,4-5,6-7
W13	Dual Port Enable	1-2	1-2
W14	Dual Port Range	1-2,3-4,5-6,7-8	1-2,3-4,5-6,7-8
W15	Dual Port Start Add	1-2,3-4,5-6,7-8, 9-10,12-13	1-2,3-4,5-6,7-8, 9-10,12-13
W16	Dual Port Privacy	None	None
W17	CPU	1-2,4-5,7-8,10-11, 13-14,16-17,19-20, 22-23	1-2,4-5,7-8,10-11, 13-14,16-17,19-20, 22-23

TABLE 5-10 (Cont.)

JUMPER OR SOCKET	FUNCTION	MODEL	
		-006	-110
W18	256K RAM	None	None
W19 & W19A	ICU	None	None
W20	I/O Time Base	1-2	1-2
W21	PIT	1-2,3-4,5-6,7-8 9-10,11-12	1-2,3-4,5-6,7-8 9-10,11-12
W22	Bus Clocks	1-2,3-4	1-2,3-4
W23	PIO	3-4	3-4
W24	PIO	1-2	1-2
W25	PIO	2-3,4-5	2-3,4-5
W26	Port 0	1-2,3-4	1-2,3-4
W27	Port 0	1-2,3-4	1-2,3-4
W28	Port 0	1-2,3-4	1-2,3-4
W29	Port 0	4-5,8-9,10-11	4-5,8-9,10-11
W30	Port 0	None	None
W31	Port 1	1-3,2-4	1-3,2-4
W32	Port 1	1-3,2-4	1-3,2-4
W33	Port 1	1-3,2-4	1-3,2-4
W34	Port 1	4-5,8-9,10-11	4-5,8-9,10-11
W35	Port 1	None	None
W36	Delay Line	None	None

TABLE 5-10 (Cont.)

JUMPER OR SOCKET	FUNCTION	MODEL	
		-006	-110
W37	CPU	1-2	1-2
W38	BLX	1-2,4-5	1-2,4-5
W40	LOCK/	2-3	2-3
W41		None	None
W42		None	None
W43		None	None
U2-U5		7437	7437
U21		Vacant	NS16202
U22		74LS92	Vacant
U30		12.0 MHz Oscillator	20.0 MHz Oscillator
U52		Vacant	NS16081
U64		Vacant	Vacant
U69		NS16032	NS16032
U76		Vacant	NS16082
U86		DS8304	DS8304
U88		DS8303	DS8303

Appendix A

DB16000A CONFIDENCE TEST

A.1 GENERAL DESCRIPTION

The DB16000A Confidence Test (DCT16) is a ROM- or PROM-based program that tests the hardware of a DB16000A board level computer. In addition to providing confidence in the hardware when the test passes, diagnostic information about the source of a failure is provided in the event of a test failure. Progress of the confidence test can be monitored with two LED indicator lamps on the DB16000A board and through the two serial ports. One of the lamps (DS1) is on throughout the test to indicate a test in progress. The other lamp (DS2) turns on only to indicate a test failure. A sign-on message is sent to both of the serial interface ports. Any individual test failures are reported to both serial ports.

DCT16 is designed to work immediately after a power-on hardware reset by making no assumptions about the state of any of the hardware other than normal reset conditions. As much as possible, the hardware is left in the same condition as a hardware reset when the tests are all complete.

Configuration of the board and baud settings for the serial ports are taken from the on-board DIP switch (see Section A.2). No off-board access are performed which means that the MULTIBUS interface and the dual port arbiter are not tested by DCT16.

A.2 INTERFACE CHARACTERISTICS

A.2.1 DIP Switch Settings

Table A-1 contains the DIP switch interpretations.

A.2.2 LED Indicators

Software control of the two LED indicators provides visual indication of the progress and results of DCT16. Hardware features add to this visual indication of test progress.

When a hardware reset is asserted on the board, all four LEDs light as a lamp test feature. If the processor begins executing a program, the bus time out LED indicator (DS4) extinguishes. Therefore, if DS4 does not extinguish after reset, the processor is not fetching and executing instructions.

TABLE A-1 DIP SWITCH SETTINGS (S3)

S4	S3	S2	S1	BAUD RATE
on	on	on	on	19200
on	on	on	off	9600
on	on	off	on	7200
on	on	off	off	4800
on	off	on	on	3600
on	off	on	off	2400
on	off	off	on	2000
on	off	off	off	1800
off	on	on	on	1200
off	on	on	off	600
off	on	off	on	300
off	on	off	off	150
off	off	on	on	134
off	off	on	off	110
off	off	off	on	75
off	off	off	off	50

S5: On only when FPU installed on-board.
S6: On only when MMU installed on-board.
S7: Off enables testing of 8255A PPI connected to J1. On inhibits testing of 8255A PPI connected to J1.

Assuming the processor does fetch and execute instructions, the first step in DCT16 is to extinguish all three software controlled LED indicators, DS1, DS2, DS3. The next step is to turn on the Confidence Test Run LED, DS1. The Confidence Test Fail LED, DS2, then lights only upon failure of any one of the DCT16 tests. After completion of DCT16 execution, the Confidence Test Run LED extinguishes. If the Fail LED is lit, it will remain so.

A.2.3 Serial Ports

DCT16 test failures are output on both of the serial ports (redundancy in case one fails) to provide mnemonic description of the failed test. Baud for each serial device is set according to the baud DIP switches described in A.2.1. This baud setting is valid only when the board is in diagnostic mode and, therefore, should not be used by an application program that executes after DCT16.

A.2.4 RAM Usage

DCT16 requires no RAM for operation. This permits operation of DCT16 as a diagnostic tool even when the DB16000A on-board RAM is not functional. It further provides diagnostic information about partially operational RAM.

All RAM testing is done nondestructively. Execution of DCT16 will, therefore, not disturb user programs in RAM. Every location is tested for the capability of storing true and complement data but is restored upon test completion to its original value.

A.3 TEST SEQUENCE

This section describes the tests executed, the sequence in which the tests are executed, and the fail codes associated with each test. The following sections describe a basic test which will always output an error message if failure occurs or a "tick" if the test passes. A tick is a single plus sign (+). Unless an unexpected exception occurs, such as NMI or other traps, all enabled tests are performed independent of pass/fail of other tests. Disabled tests, such as the FPU test which must be disabled via dip switch when no FPU is installed, will still provide a tick for consistent tracing of failure location should the program cease execution or otherwise get lost in some test before displaying a fail message.

Each test description that follows includes the error message the test might generate. For quick location of a fail message, each is underlined in this text.

If an unexpected exception occurs during execution of DCT16, the following message is displayed:

XXXX EEE exception occurred, ***DCT16 ABORTED***

where:

XXXX is the fail code associated with the test that was in progress when the exception occurred.

EEE is the exception that occurred, encoded as follows:

NVI	Nonvectored interrupt
NMI	Nonmaskable interrupt
ABT	Memory Management Unit abort
FPU	Floating-Point Unit exception
ILL	Illegal instruction trap
SVC	Supervisor Call trap
DVZ	Divide by zero trap
FLG	Flag trap
BPT	Breakpoint trap
TRC	Trace trap
UND	Undefined instruction trap

A.3.1 CPU Test

<u>00XX CPU FAILURE</u>

A CPU confidence test is performed by writing and reading most program accessible registers in the CPU.

A.3.2 Configuration and Exception Setup

<u>0100</u>

Setup of exception environment and configuration. Error code only meaningful for exception error.

A.3.3 J2 Transmitter Test

<u>03XX J2 Transmitter failed</u>

This failure indicates transmitter ready (TxRDY) from serial port J2 is not present during the sign-on message output to J2.

A.3.4 J2 Receiver Test

<u>03XX J2 Receiver failed</u>

This failure indicates receiver ready (RxRDY) from serial port J2 is not present during the sign-on message output to J2.

A.3.5 J2 Loopback Test

<u>03XX J2 Local loop back failed</u>

This failure indicates the data read from J2 serial port does not match data transmitted during the sign-on message output to J2.

A.3.6 J3 Transmitter Test

<u>03XX J3 Transmitter failed</u>

This failure indicates transmitter ready (TxRDY) from serial port J3 is not present during the sign-on message output to J3.

A.3.7 J3 Receiver Test

<u>03XX J3 Receiver failed</u>

This failure indicates receiver ready (RxRDY) from serial port J3 is not present during the sign-on message output to J3.

A.3.8 J3 Loopback Test

<u>03XX J3 Local loop back failed</u>

This failure indicates the data read from J3 serial port does not match data transmitted during the sign-on message output to J3.

A.3.9 RAM Data Test

<u>0400 RAM Data Test Failure: bbbbbbbbbbbbbbbb</u>

Nondestructive data test of RAM. The b field is a 16-bit binary field corresponding the 16-bit data bus, least significant bit on the right. A 0 indicates a pass condition and a 1 indicates a fail condition. All fails (ones) often indicate an address failure. Refer to RAM address test.

A.3.10 RAM Address Test

<u>0500 RAM Address Test Failure: bbbbbbbbbbbbbbbbbbbbbbbb</u>

Nondestructive RAM address test. The b field is a binary 24-bit field corresponding to the address bus. A 0 indicates a pass condition and a 1 indicates a fail condition.

A.3.11 RAM Refresh Test

<u>06XX RAM Refresh Test</u>

RAM refresh and part of the dual-port arbiter is tested as follows:

1. A data pattern is written to eight words of memory. Addresses are selected according to the actual RAM row address connections.

2. The CPU executes a tight ROM resident loop that decrements a counter in RAM so that minimal addresses in the RAM are read or written, but RAM reads and writes are frequent. Time for this tight loop is approximately one second with CPU running at 10 MHz.

3. Data pattern is read checked for validity.

A.3.12 MMU Register Test

<u>070X register failure: HHHHHHHH</u>

If present (as indicated by DIP switch), the MMU is verified by first writing and reading all program-accessible registers. The H field is a 32-bit hex field that is an exclusive OR of the expected data with actual register data. failed registers can be determined by fail codes as follows:

0701 & 0702	PTB0
0703 & 0704	PTB1
0705 & 0706	BPR0
0707 & 0708	BPR1
0709 & 070A	BCNT

A.3.13 MMU Trace Test

<u>071X MMU Trace test failure</u>

Test of trace capability and PF0, PF1 and SC registers.

A.3.14 Floating-Point Unit Test

080X FPU test failed

All registers of the FPU are loaded with floating-point data and arithmetic performed to check functionality.

A.3.15 Programmable Interval Timer Test

09XX PIT failure

The 8253 programmable interval timer is verified by programming each of the counters and reading each to observe count progress Particular timer failure can be determined by the fail code:

090X	Counter 0
091X	Counter 1
092X	Counter 2

After checking the counters, they are set to specific values that yield the following frequencies when jumpers are set according to factory-default shipping configuration:

Counter 0:	100 Hertz
Counter 1:	1 Kilohertz
Counter 2:	1 Kilohertz

A.3.16 Programmable Peripheral Interface Test

0AXX PPI test failure

The 8355A PPI is tested only if the proper DIP switch is set to enable testing. This ensures that testing does not interfere with external application hardware that might be tied to the parallel port. Testing the 8255A requires the ports to be configured as outputs and data read from them. After this test, the ports are returned to the input mode.

A.3.17 Interrupt Control Unit Timer Test

0B0X ICU Timer failure

If present (determined by attempting to write and read H-counter starting value, low register) the ICU timer is tested by programming a specific value and verifying the count progress.

A.3.18 Interrupt Control Unit Interrupt Test

0B1X ICU Interrupt failure

The ICU is programmed to provide an interrupt to the CPU via a software interrupt. The CPU must vector to the correct interrupt location.

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