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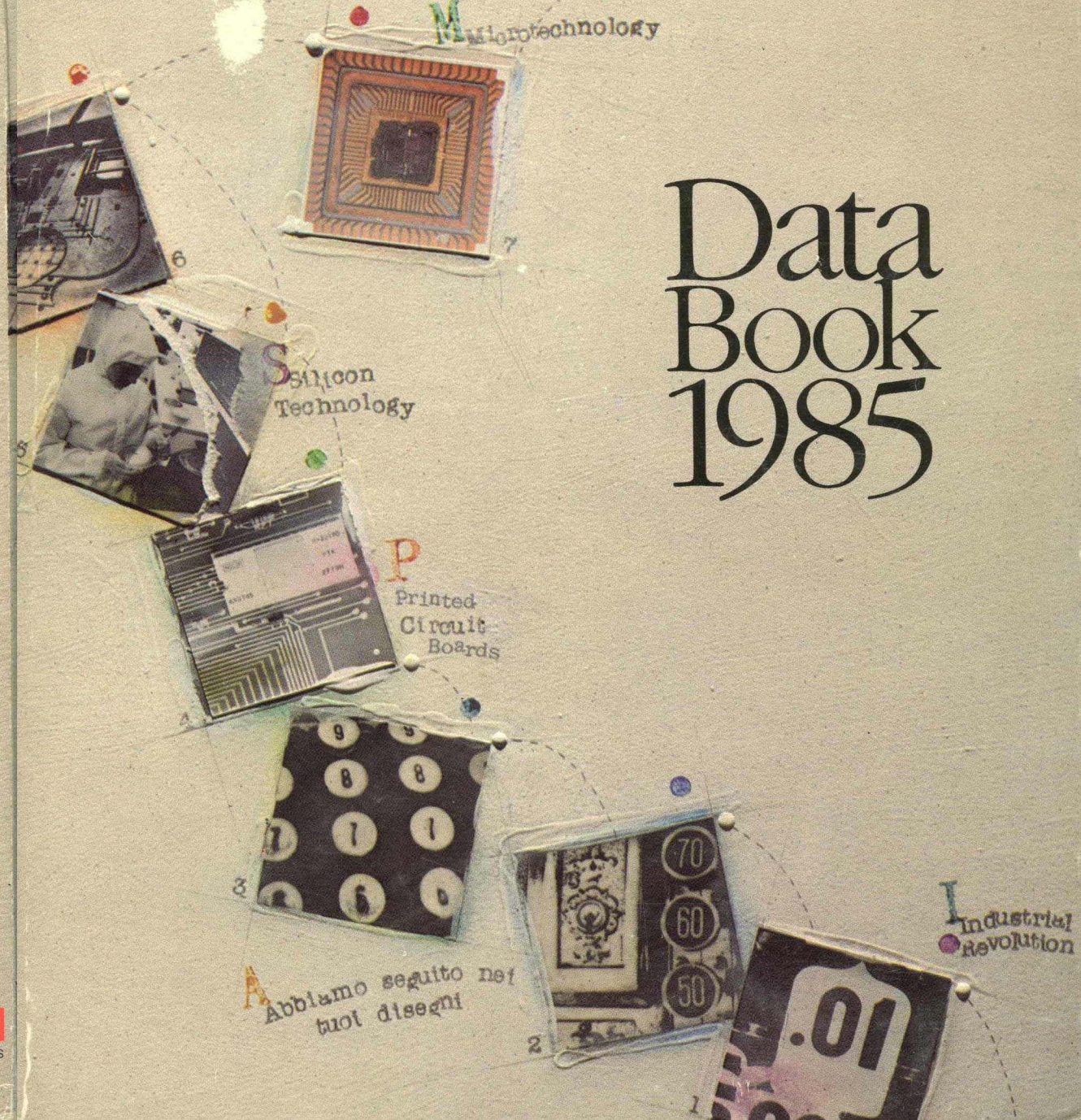
Data Book 1985



Data Book 1985

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NCR Microelectronics Data Book - 1985

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Woburn, MA 01801
Phone: (617) 933-0778

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Santa Clara, CA 95050
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(513) 866-7471 in Ohio or International
Telex: 241669 NCR NVMEM MSBG

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2001 Danfield Court
Fort Collins, CO 80525-2998
Phone: (303) 226-9500 or (303) 223-5100
Telex: 45-4505 NCR MICRO FTCN

MICROPROCESSORS/PERIPHERALS

NCR Microelectronics Division
1635 Aeroplaza Drive
Colorado Springs, CO 80916
Phone: (303) 596-5612 (800) 525-2252
Telex: 452-457 NCR MICRO CSP

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INTRODUCTION

MEMORIES

NCR SEMICUSTOM DESIGN

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MICROCOMPUTERS/MICROPROCESSORS

SPECIAL FUNCTION CHIPS

NCR Microelectronics

NCR, a multi-billion-dollar manufacturer of computer systems, terminal products, and semiconductors, established its first microelectronics laboratory in 1963 to stay abreast of the emerging semiconductor technology. The laboratory was expanded in 1966 to provide limited quantities of prototype microcircuits designed for use in a number of new products. By 1968 the first MOS circuits were produced, and by 1970 a complete family of circuits had been designed, produced in prototype quantities, and incorporated into new NCR products. Based upon knowledge gained in this research and confidence in the ultimate advantages of MOS, the decision was made to expand the internal production capability. In 1971, the Miamisburg, Ohio plant was completed.

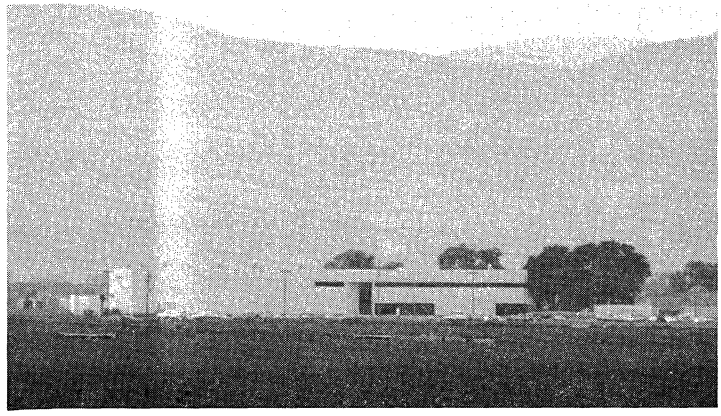
To meet internal demand, NCR expanded its microelectronics operation in 1975 with the addition of a second production facility in Colorado Springs, Colorado, and in 1979 added a third facility in Ft. Collins, Colorado. The Colorado Springs facility was replaced in 1982 by a new plant occupying 100,000 square feet. This new plant is one of the most modern, best-equipped facilities of its kind anywhere.

NCR Microelectronics manufactures state-of-the-art NMOS, CMOS, and non-volatile SNOS components which provide a competitive advantage to its computer systems and terminal product lines.

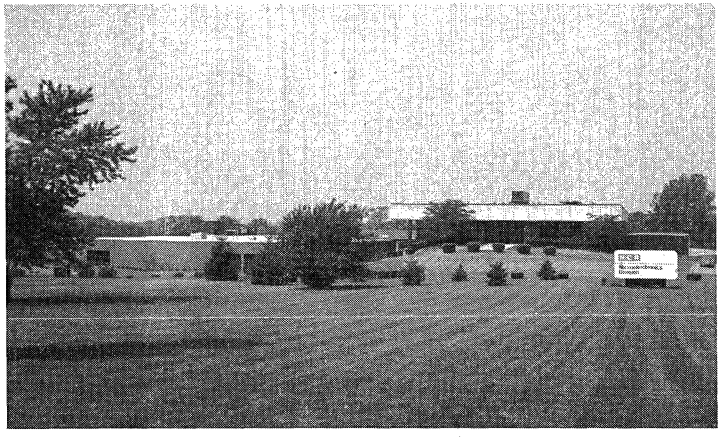
In mid-1981 NCR announced its entry into the merchant semiconductor market. The strength and discipline gained in 10 years of internal supply is now being made available to our customers. This experience, together with a family of innovative products and services, establishes NCR as a leading supplier of semiconductor devices and services.

Colorado Springs, Colorado

Fort Collins, Colorado



Miamisburg, Ohio



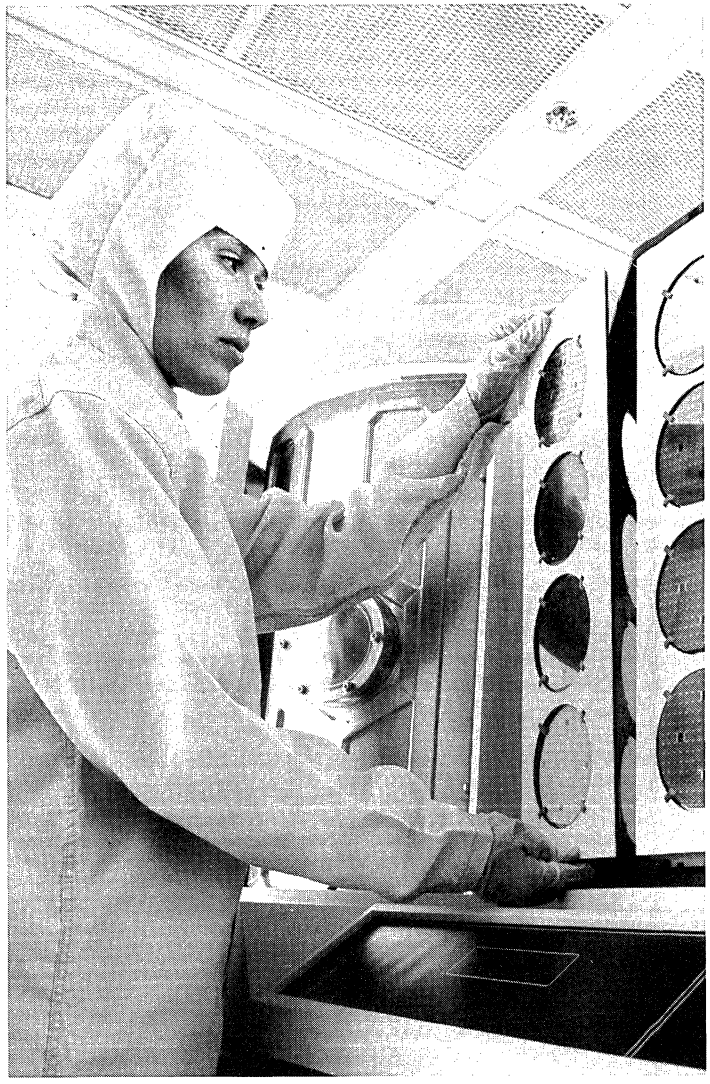
NCR's Commitment to Quality

As a pioneer in microelectronic technology, NCR has been manufacturing components for its own product line since 1971. This experience has provided opportunities to learn about user application problems, the importance of component quality and reliability, and their effects on total system reliability. The net result of such experience is a dedication to manufacturing superior components based on a firm commitment to quality and reliability.

NCR Quality Assurance completes a rigorous evaluation of each product to ensure conformance of the product to its specification. Once a component is approved for production, stringent process and assembly controls along with detailed inspections are used to build in reliability. Comprehensive electrical testing is performed to guarantee the performance of each component; finished products are inspected before shipment to assure the conformance to specification of each lot of devices, and sampling plans are constantly revised and updated to improve quality.

Essential to any reliability program is feedback from the system user—communication that is vital for reliability growth. NCR strives to "close the loop" by communicating with users to evaluate problems and respond with corrective action. The closed-loop concept results in better understanding of user needs while improving reliability.

The NCR commitment to quality and reliability is an integral part of corporate philosophy originating from and emphasized by the highest levels of NCR management. This management direction, combined with NCR's manufacturing and user application experience, provides a solid framework for continued improvement in quality and reliability.



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Tustin, CA 92680
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Technology Marketing Corporation
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Fort Wayne, IN 46804
(219) 432-5553

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REP Associates Corp.
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(319) 373-0152

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Technology Marketing Corporation
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(502) 499-7808

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Marktron, Inc.
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England
Maidenhead (0628) 75851

Read Only Memories

NCR offers a full line of Read Only Memories (ROM) with a variety of pin-outs and access times. The NCR NMOS and CMOS processes and experience in the ROM market allow NCR to provide fast turnaround of prototype and production quantities plus provide the customer service and support required of a major supplier of ROMs in today's market. Look to NCR for your ROM requirements to insure that your products reach the market place in time for maximum market penetration.

PRODUCT SELECTION GUIDE

FUNCTION	PART NUMBER	ORGANIZATION	PAGE
16K ROM	NCR 2316	2K x 8	09
32K ROM	NCR 2332	4K x 8	13
	NCR 2333	4K x 8	17
64K ROM	NCR 2364	8K x 8	21
	NCR 23C64	8K x 8	25
	NCR 2364A	Two 4K x 8 banks	29
	NCR 2365	8K x 8	33
	NCR 23C65	8K x 8	37
128K ROM	NCR 23128	16K x 8	41
	NCR 23128A	Four 4K x 8 banks	45
256K ROM	NCR 23256	32K x 8	49
	NCR 23C256	32K x 8	53
	NCR 23257	32K x 8	57

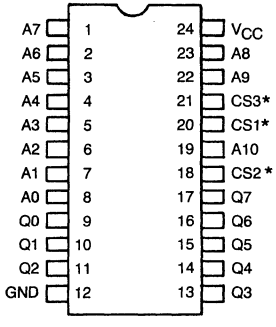
Note: Commercial operating temperature (0°C-70°C) is standard for all NCR ROM's. Industrial operating temperature (–40°C-85°C) is also available.

2316
16K (2K X 8) ROM

- **Fully Static Operation**
- **Programmable Chip Selects**
- **Maximum Access Time**
  2316-30 ..... 300ns
  2316-45 ..... 450ns
- **0°C –70°C Operating Range.**
- **3-State Outputs**
- **Fully TTL Compatible**
- **Single ±10% 5 Volt Supply**
- **Pin Compatible with 2716 and 2516 EPROM's and 2316 Type ROM's.**

The NCR2316 is a mask programmable read-only-memory with a 2K word by 8-bit organization. Designed for ease of use, this device requires only a 5 volt supply, is TTL compatible, and because of its totally static (asynchronous) operation requires no clock. The active level of the three-chip select inputs are programmable and are defined by the user. These ROMs are available in a 24 pin package and are pin compatible with industry standard EPROMs and ROMs.

PIN CONFIGURATION

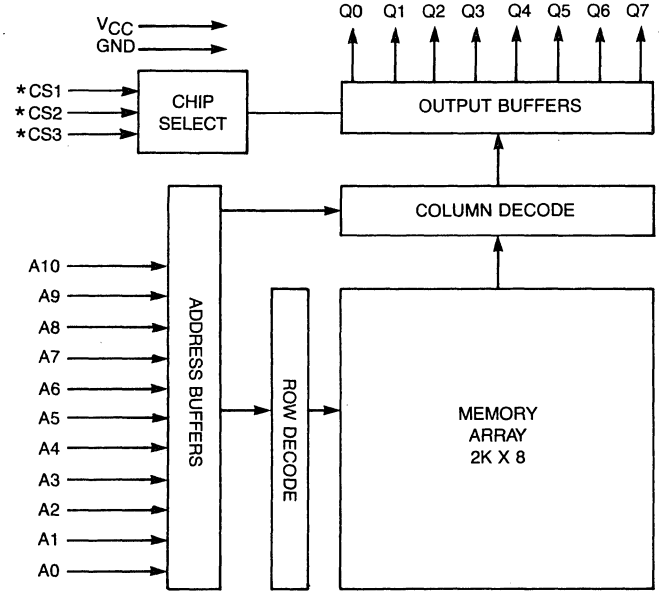


*Active Level (Hi, Low and Don't Care) of chip selects are defined by user.

PIN NAMES

A0 - A10	Address Inputs
Q0 - Q7	Data Outputs
CS1 - CS3	Programmable Chip Selects
V_{CC}	5V ± 10% Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



*MASK PROGRAMMABLE

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NCR

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to ground −.5 to +7V
Storage temperature..... −65°C to 150°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operating conditions stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Supply voltage*	4.5	5.0	5.5	Volts
V_{IH}	Input high level voltage	2.0		V_{CC}	Volts
V_{IL}	Input low level voltage	−0.5		0.8	Volts
T_A	Operating ambient temperature	0		70	°C

* V_{CC} must be applied at least 100μs before proper device operation is achieved.

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IN}	Input leakage current	V_{IN} = 0V to V_{CC} max			10	μA
I_O	Output leakage current	V_O = 0.2 to V_{CC} max, Chip Deselected			±10	μA
V_{OH}	Output high voltage	I_{OH}=−160μA	2.4			Volts
V_{OL}	Output low voltage	I_{OL}=1.6mA			0.4	Volts
I_{CC}	Supply current	Outputs Open			80	mA

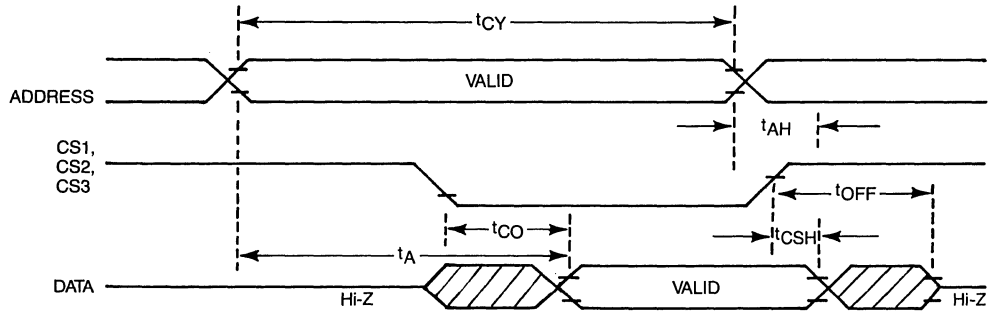
CAPACITANCE, T_A = 25°C, f=1 MHZ

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
C_{IN}	Input capacitance	All pins except pin under			7	pF
C_O	Output capacitance	test are tied to ground			12.5	pF

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

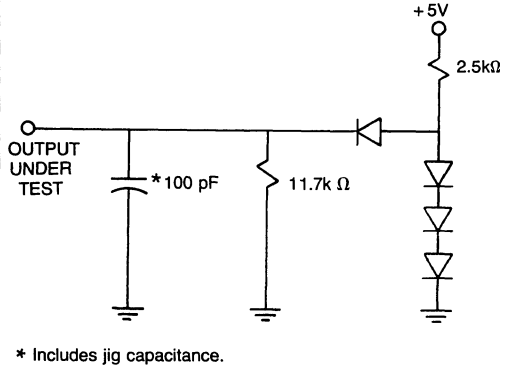
Symbol	Parameter	2316-30			2316-45			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{CY}	Cycle time	300			450			ns
t_A	Address access time			300			450	ns
t_{CO}	Chip select access time			150			200	ns
t_{OFF}	Chip select to data off (Hi Z)			150			200	ns
t_{CSH}	Chip select to data hold	0			0			ns
t_{AH}	Address to data hold	0			0			ns

AC WAVEFORMS



The chip select lines are assumed to be active low.

AC TEST LOAD CIRCUIT



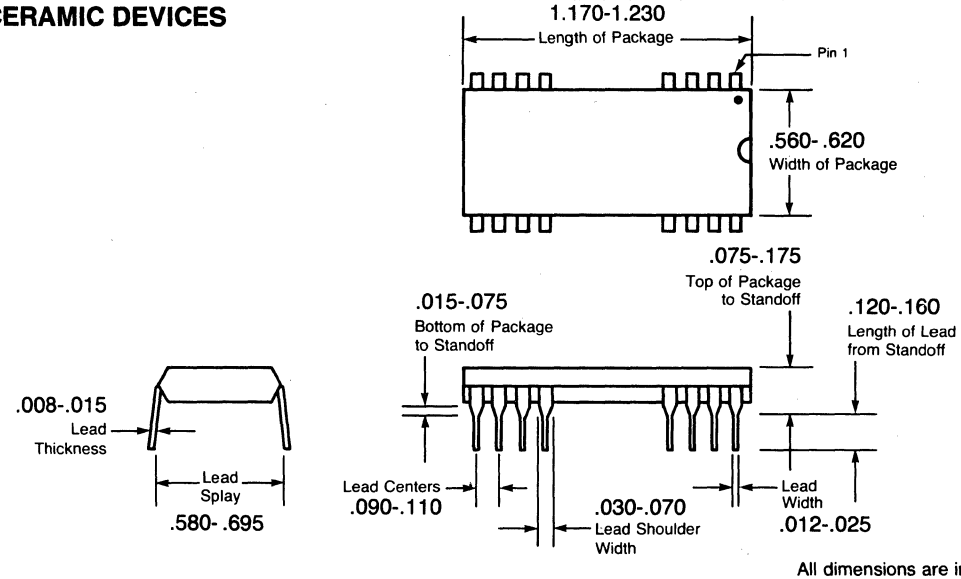
* Includes jig capacitance.
All diodes 1N3064 or equivalent.

A.C. CONDITION OF TESTS

Input Pulse Levels . . . . . .0.8 Volts to 2.0 Volts
Inputs Rise & Fall Times . . . . . .10 ns
Output Timing Levels . . . . . .0.8 Volts to 2.0 Volts

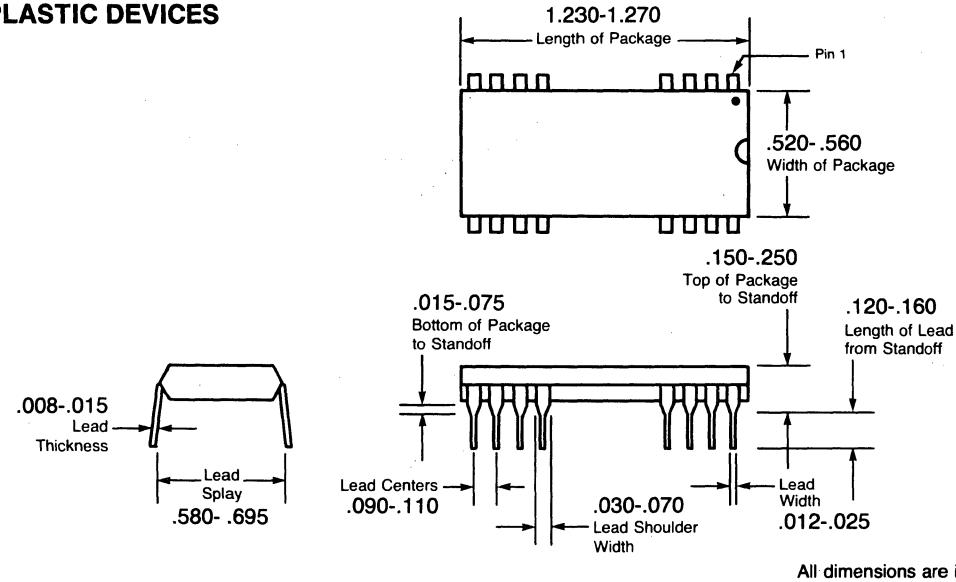
MECHANICAL DATA 24 PIN

CERAMIC DEVICES



All dimensions are inches.

PLASTIC DEVICES



All dimensions are inches.

NCR

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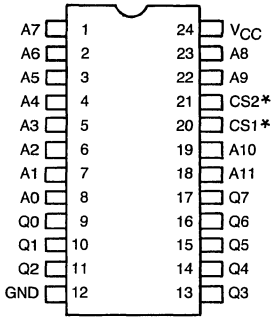
Phone: 1-800-543-5618 outside Ohio
513/866-7217 Ohio or International

2332
32K (4K X 8) ROM

- **Fully Static Operation**
- **Programmable Chip Selects**
- **Maximum Access Time**
  2332-30 ..... 300ns
  2332-45 ..... 450ns
- **0°C –70°C Operating Range.**
- **3-State Outputs**
- **Fully TTL Compatible**
- **Single ±10% 5 Volt Supply**
- **Pin Compatible with 2532 EPROM's and 2332 Type ROM's.**

The NCR2332 is a mask programmable read-only-memory with a 4K word by 8-bit organization. Designed for ease of use, this device requires only a 5 volt supply, is TTL compatible, and because of its totally static (asynchronous) operation requires no clock. The active level of the two chip select inputs are programmable and are defined by the user. These ROMs are available in a 24 pin package and are pin compatible with 2532 EPROMs and 2332 Type ROMs.

PIN CONFIGURATION

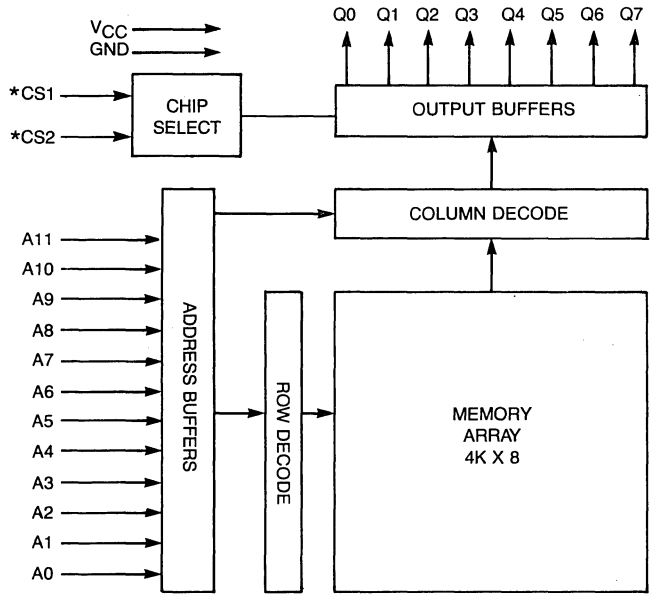


* Active Level (Hi, Low and Don't Care) of chip selects are defined by user.

PIN NAMES

A0 - A11	Address Inputs
Q0 - Q7	Data Outputs
CS1 - CS2	Programmable Chip Selects
V_{CC}	5V ± 10% Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



*MASK PROGRAMMABLE

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ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to ground −.5 to +7V
Storage temperature..... −65°C to 150°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operating conditions stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Supply voltage*	4.5	5.0	5.5	Volts
V_{IH}	Input high level voltage	2.0		V_{CC}	Volts
V_{IL}	Input low level voltage	−0.5		0.8	Volts
T_A	Operating ambient temperature	0		70	°C

* V_{CC} must be applied at least 100μs before proper device operation is achieved.

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IN}	Input leakage current	V_{IN}=OV to V_{CC} max			10	μA
I_O	Output leakage current	V_O = 0.2 to V_{CC} max, Chip Deselected			±10	μA
V_{OH}	Output high voltage	I_{OH}=−160μA	2.4			Volts
V_{OL}	Output low voltage	I_{OL}=1.6mA			0.4	Volts
I_{CC}	Supply current	Outputs Open			80	mA

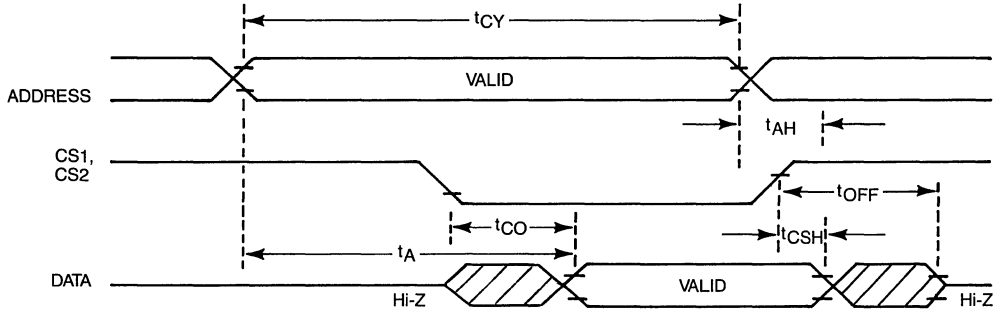
CAPACITANCE, T_A = 25°C, f=1 MHZ

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
C_{IN}	Input capacitance	All pins except pin under			7	pF
C_o	Output capacitance	test are tied to ground			12.5	pF

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

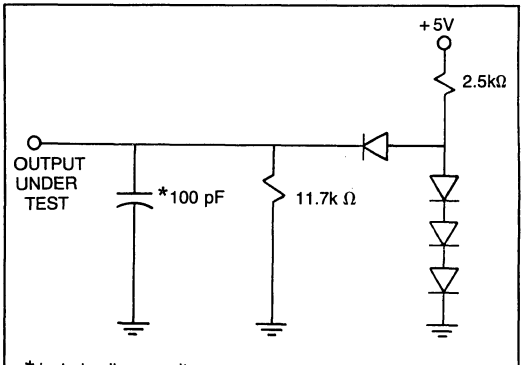
Symbol	Parameter	2332-30			2332-45			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{CY}	Cycle time	300			450			ns
t_A	Address access time			300			450	ns
t_{CO}	Chip select access time			150			200	ns
t_{OFF}	Chip select to data off (Hi Z)			150			200	ns
t_{CSH}	Chip select to data hold	0			0			ns
t_{AH}	Address to data hold	0			0			ns

AC WAVEFORMS



The chip select lines are assumed to be active low.

AC TEST LOAD CIRCUIT



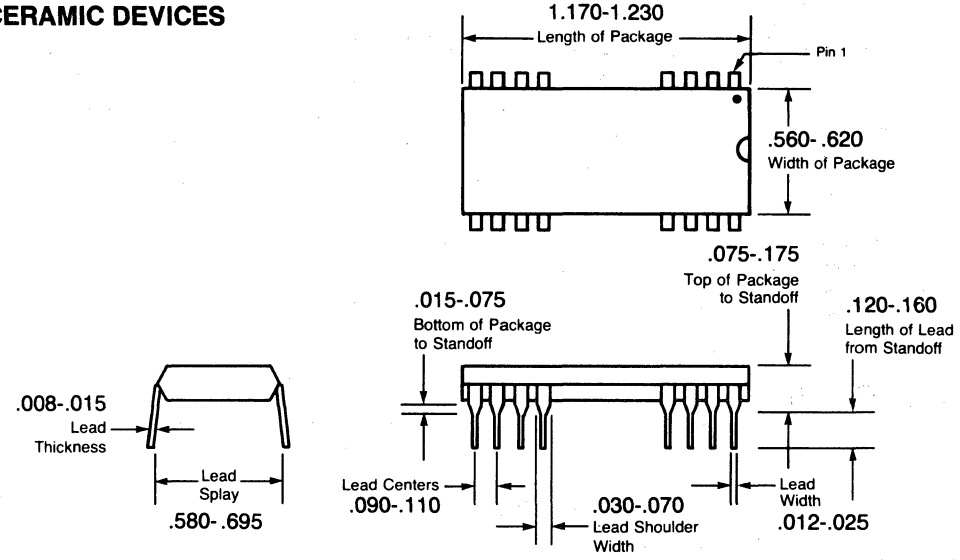
* Includes jig capacitance.
All diodes 1N3064 or equivalent.

A.C. CONDITION OF TESTS

Input Pulse Levels . . . . . .0.8 Volts to 2.0 Volts
Inputs Rise & Fall Times . . . . . .10 ns
Output Timing Levels . . . . . .0.8 Volts to 2.0 Volts

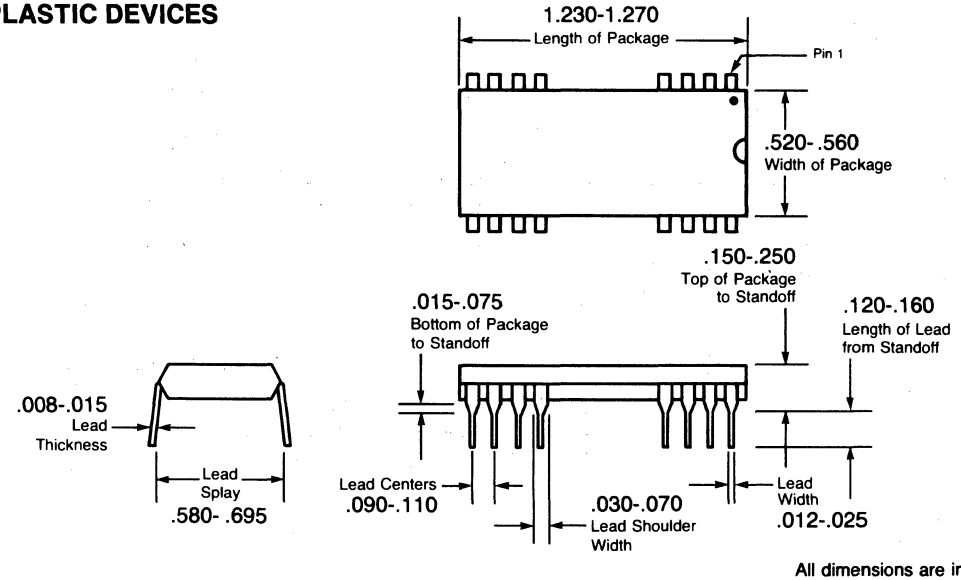
MECHANICAL DATA 24 PIN

CERAMIC DEVICES



All dimensions are inches.

PLASTIC DEVICES



All dimensions are inches.

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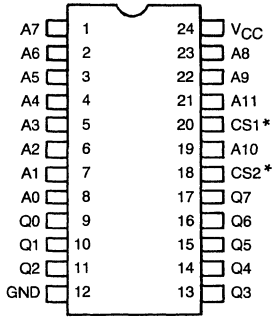
2333
32K (4K X 8) ROM

- **Fully Static Operation**
- **Programmable Chip Selects**
- **Maximum Access Time**
  2333-30 ..... 300ns
  2333-45 ..... 450ns
- **0°C –70°C Operating Range.**
- **3-State Outputs**
- **Fully TTL Compatible**
- **Single ±10% 5 Volt Supply**
- **Pin Compatible with 2732 EPROM's**

The NCR2333 is a mask programmable read-only-memory with a 4K word by 8-bit organization. Designed for ease of use, this device requires only a 5 volt supply, is TTL compatible, and because of its totally static (asynchronous) operation requires no clock. The active level of the two chip select inputs are programmable and are defined by the user. These ROMs are available in a 24 pin package and are pin compatible with 2732 EPROMs.

PIN CONFIGURATION

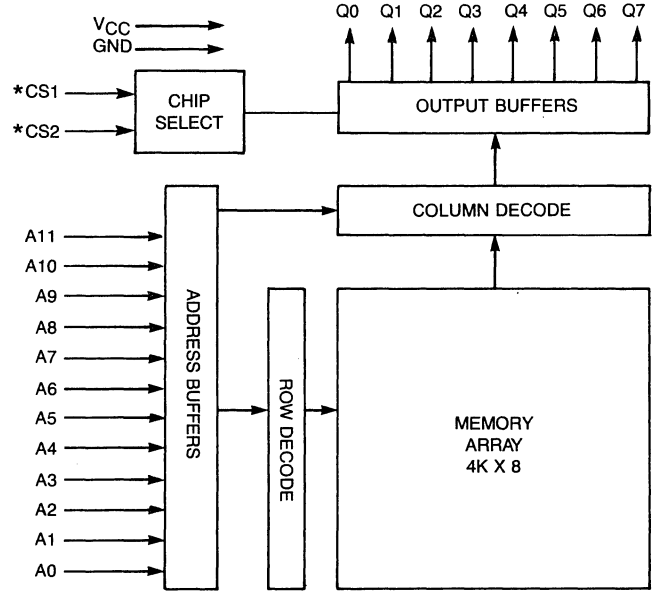


* Active Level (Hi, Low and Don't Care) of chip selects are defined by user.

PIN NAMES

A0 - A11	Address Inputs
Q0 - Q7	Data Outputs
CS1 - CS2	Programmable Chip Selects
V_{CC}	5V ± 10% Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



* MASK PROGRAMMABLE

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NCR

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to ground −.5 to +7V
Storage temperature..... −65°C to 150°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operating conditions stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Supply voltage *	4.5	5.0	5.5	Volts
V_{IH}	Input high level voltage	2.0		V_{CC}	Volts
V_{IL}	Input low level voltage	−0.5		0.8	Volts
T_A	Operating ambient temperature	0		70	°C

*V_{CC} must be applied at least 100μs before proper device operation is achieved.

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IN}	Input leakage current	V_{IN}=OV to V_{CC} max			10	μA
I_O	Output leakage current	V_O = 0.2 to V_{CC} max, Chip Deselected			±10	μA
V_{OH}	Output high voltage	I_{OH}= −160μA	2.4			Volts
V_{OL}	Output low voltage	I_{OL}=1.6mA			0.4	Volts
I_{cc}	Supply current	Outputs Open			80	mA

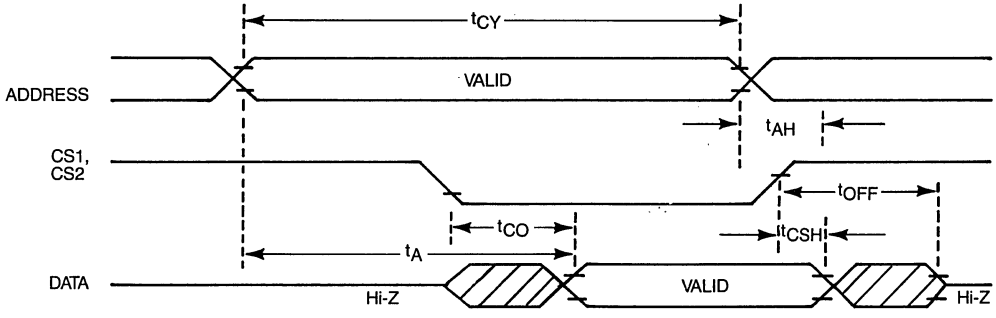
CAPACITANCE, T_A = 25°C, f=1 MHZ

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
C_{IN}	Input capacitance	All pins except pin under			7	pF
C_O	Output capacitance	test are tied to ground			12.5	pF

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

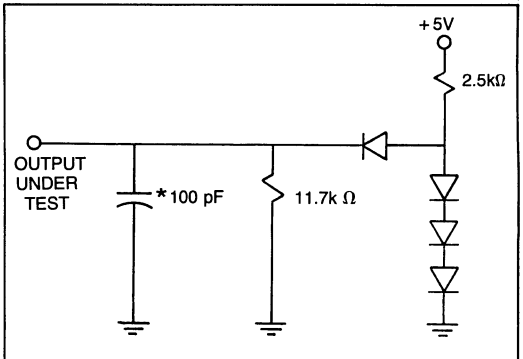
Symbol	Parameter	2333-30			2333-45			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{CY}	Cycle time	300			450			ns
t_A	Address access time			300			450	ns
t_{CO}	Chip select access time			150			200	ns
t_{OFF}	Chip select to data off (Hi Z)			150			200	ns
t_{CSH}	Chip select to data hold	0			0			ns
t_{AH}	Address to data hold	0			0			ns

AC WAVEFORMS



The chip select lines are assumed to be active low.

AC TEST LOAD CIRCUIT



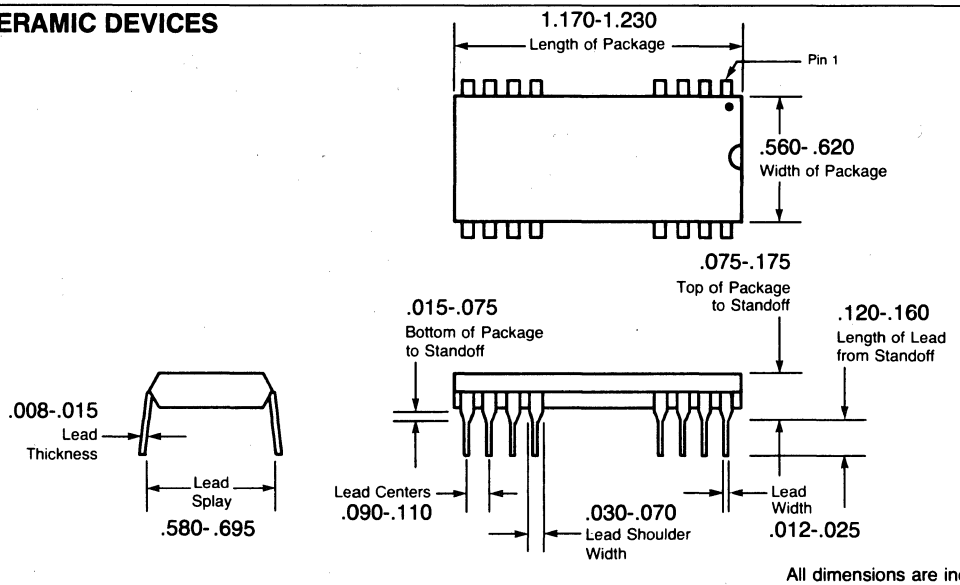
* Includes jig capacitance.
All diodes 1N3064 or equivalent.

A.C. CONDITION OF TESTS

Input Pulse Levels . . . . . .0.8 Volts to 2.0 Volts
Inputs Rise & Fall Times . . . . . .10 ns
Output Timing Levels . . . . . .0.8 Volts to 2.0 Volts

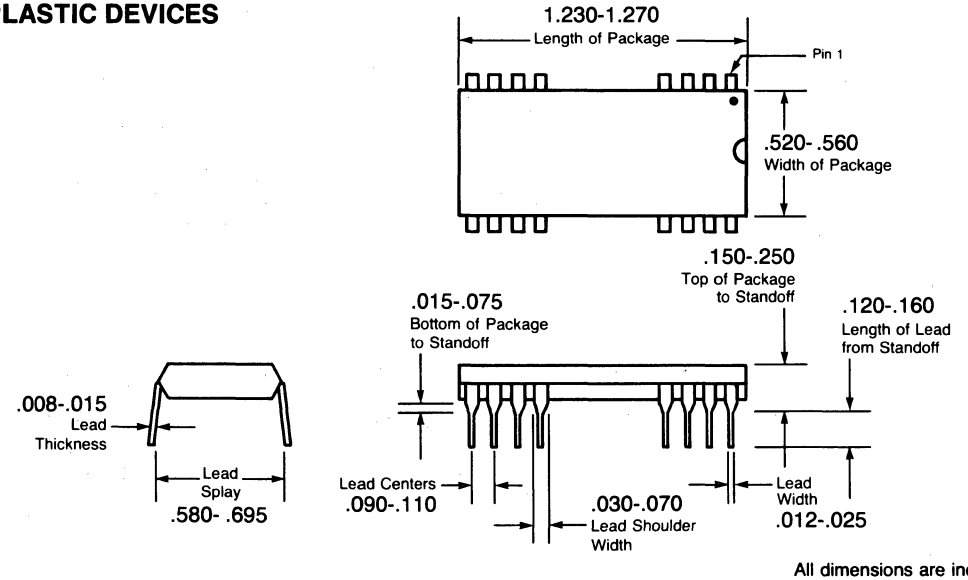
MECHANICAL DATA 24 PIN

CERAMIC DEVICES



All dimensions are inches.

PLASTIC DEVICES



All dimensions are inches.

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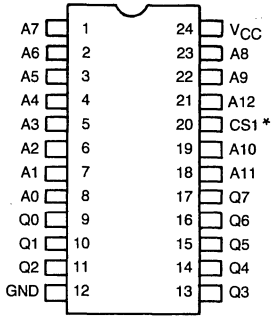
2364
64K (8K X 8) ROM

- **Fully Static Operation**
- **Programmable Chip Selects**
- **Maximum Access Time**
  - **2364-25 .....250ns**
  - **2364-30 .....300ns**
  - **2364-45 .....450ns**
- **0°C –70°C Operating Range.**
- **3-State Outputs**
- **Fully TTL Compatible**
- **Single ±10% 5 Volt Supply**
- **Pin Compatible with 2564 EPROM's**

The NCR2364 is a mask programmable read-only-memory with an 8K word by 8-bit organization. Designed for ease of use, this device requires only a 5 volt supply, is TTL compatible, and because of its totally static (asynchronous) operation requires no clock. The active level of the chip select input is programmable and is defined by the user. These ROMs are available in a 24 pin package and are pin compatible with 2564 EPROMs.

PIN CONFIGURATION

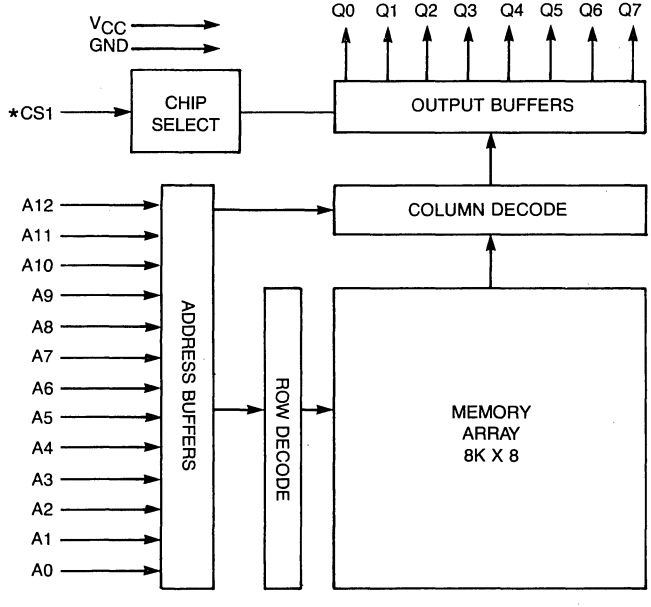


* Active Level (Hi, Low and Don't Care) of chip select is defined by user.

PIN NAMES

A0 - A12	Address Inputs
Q0 - Q7	Data Outputs
CS1	Programmable Chip Select
V_{CC}	5V ± 10% Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



*MASK PROGRAMMABLE

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ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to ground ..... −0.5 to +7V
Storage temperature..... −65°C to 150°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operating conditions stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Supply voltage *	4.5	5.0	5.5	Volts
V_{IH}	Input high level voltage	2.0		V_{CC}	Volts
V_{IL}	Input low level voltage	−0.5		0.8	Volts
T_A	Operating ambient temperature	0		70	°C

* V_{CC} must be applied at least 100μs before proper device operation is achieved.

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IN}	Input leakage current	V_{IN}= 0V to V_{CC} max			10	μA
I_O	Output leakage current	V_O = 0.2 to V_{CC} max, Chip Deselected			±10	μA
V_{OH}	Output high voltage	I_{OH}=−160μA	2.4			Volts
V_{OL}	Output low voltage	I_{OL}=1.6mA			0.4	Volts
I_{CC}	Supply current	Outputs Open			85	mA

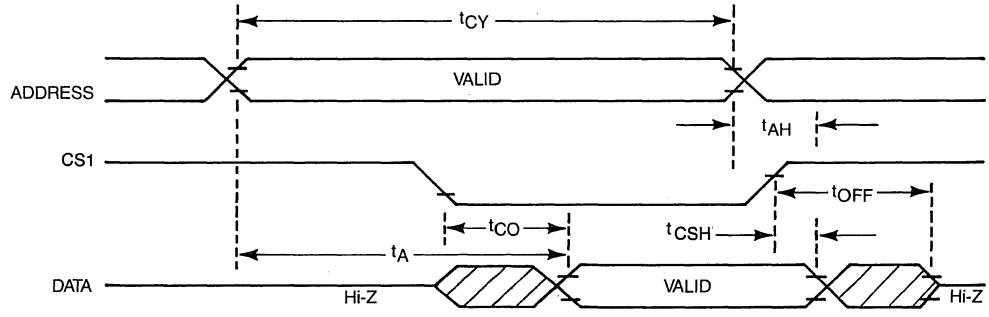
CAPACITANCE, T_A = 25°C, f=1 MHZ

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
C_{IN}	Input capacitance	All pins except pin under			7	pF
C_O	Output capacitance	test are tied to ground			12.5	pF

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

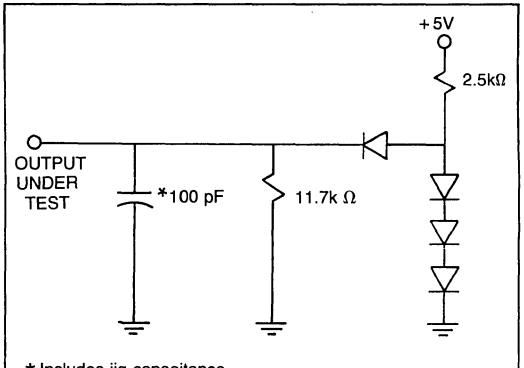
Symbol	Parameter	2364-25			2364-30			2364-45			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{CY}	Cycle time	250			300			450			ns
t_A	Address access time			250			300			450	ns
t_{CO}	Chip select access time			120			150			200	ns
t_{OFF}	Chip select to data off (Hi Z)			120			150			200	ns
t_{CSH}	Chip select to data hold	0			0			0			ns
t_{AH}	Address to data hold	0			0			0			ns

AC WAVEFORMS



The chip select line is assumed to be active low.

AC TEST LOAD CIRCUIT



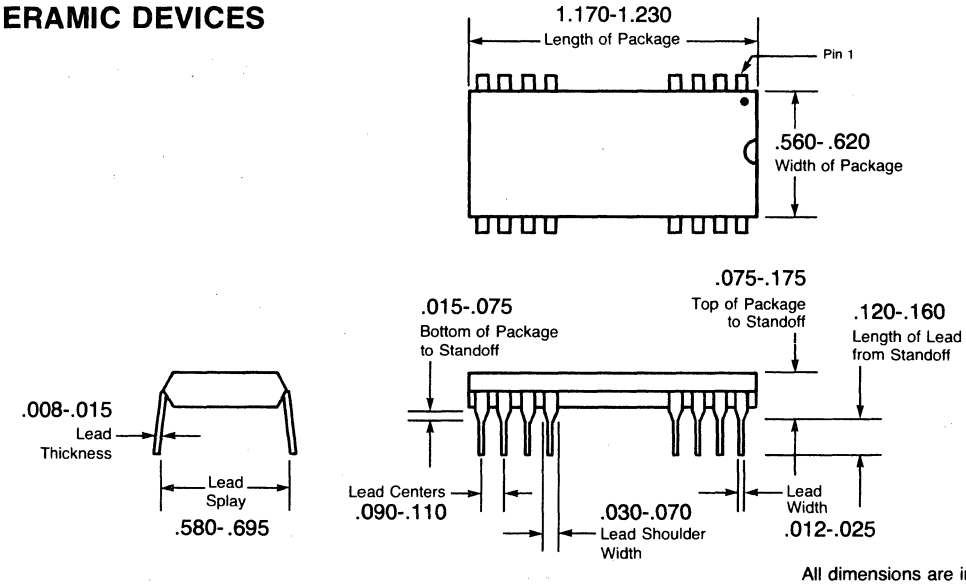
* Includes jig capacitance.
All diodes 1N3064 or equivalent.

A.C. CONDITION OF TESTS

Input Pulse Levels. . . . . .0.8 Volts to 2.0 Volts
Inputs Rise & Fall Times . . . . . .10 ns
Output Timing Levels . . . . . .0.8 Volts to 2.0 Volts

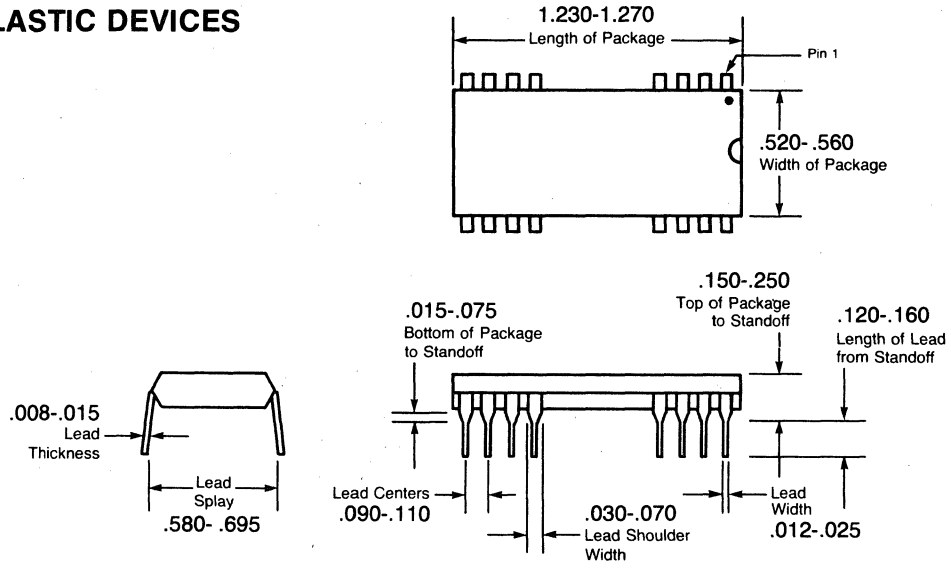
MECHANICAL DATA 24 Pin

CERAMIC DEVICES



All dimensions are inches.

PLASTIC DEVICES



All dimensions are inches.

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23C64
64K BIT CMOS MASK ROM

GENERAL DESCRIPTION

The NCR23C64 is an 8,192 words x 8 bits asynchronous, static, mask programmable ROM on a monolithic CMOS chip, and is characterized by fast access time and very low power dissipation. The static nature of the memory requires no external clock. Both the inputs and outputs are TTL compatible, and the three-state output allows easy system design and easy expansion of memory capacity. These features make the NCR23C64 usable in a wide-range of applications, especially when low power dissipation is required in microprocessor systems.

FEATURES

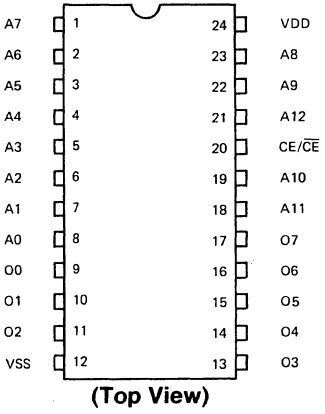
- Access time . . . . . 250 ns max.
- Low power supply current
  - Standby. . . . . 10 μA max.
  - Operation . . . . . 25 mA max.
- Standby power not affected by address transitions
- Completely static
- Single power supply. . . . . +5.0V± 10%
- All inputs and outputs are TTL compatible
- Three-state output for direct bus compatibility
- Pin compatible with EPROMs
- All inputs protected against static charge of 1000 V Nominal
- CE/$\overline{CE}$ active level is mask programmable
- Compatible with 2 MHz NCR65C02 Microprocessor

PIN FUNCTION

A0–A12	Address input
CE/$\overline{CE}$	Chip enable
O0–O7	Data output
VDD	Power supply (+5.0V)
VSS	Power supply (GND)

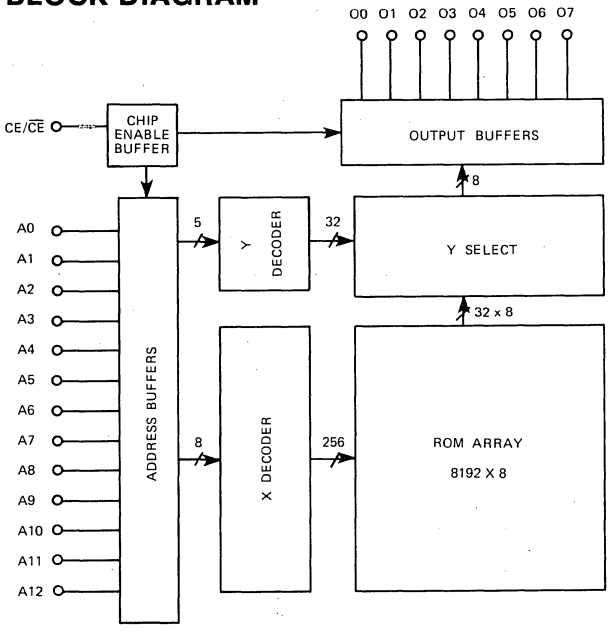
*Specifications are subject to change without notice.

PIN CONFIGURATION



(Top View)

BLOCK DIAGRAM



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NCR

ABSOLUTE MAXIMUM RATINGS* (V_{DD} = 5.0V ± 10%, V_{SS} = 0.0V, T_A = 0° to + 70°C)

RATING	SYMBOL	VALUE	UNIT
VOLTAGE ON ANY TERMINAL RELATIVE TO V_{SS}	V_{IN}	− 1.0 to + 7.0	V
OPERATING TEMPERATURE (AMBIENT)	T_A	0 to 70	°C
STORAGE TEMPERATURE (CERAMIC)	T_{STG}	− 65 to + 150	°C
STORAGE TEMPERATURE (PLASTIC)	T_{STG}	− 55 to + 125	°C
POWER DISSIPATION	—	1	W

*NOTE: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYM	MIN	TYP	MAX	UNITS
POWER SUPPLY VOLTAGE	V_{DD}	4.5	5.0	5.5	V
INPUT LOW VOLTAGE	V_{IL}	−0.5	—	0.8	V
INPUT HIGH VOLTAGE	V_{IH}	2.0	—	V_{DD}	V

DC CHARACTERISTICS (V_{DD} = 5V ± 10%, T_A = 0° to + 70°C)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES***
V_{DD} POWER SUPPLY CURRENT (ACTIVE)	I_{DD}	—	—	25	mA	1
V_{DD} POWER SUPPLY CURRENT (STANDBY)	I_{SB}	—	—	10	μA	2
INPUT LEAKAGE CURRENT	$I_{I(L)}$	− 10	—	10	μA	3
OUTPUT LEAKAGE CURRENT	$I_{O(L)}$	− 10	—	10	μA	4
OUTPUT LOW VOLTAGE @ I_{OUT} = 1.6 mA	V_{OL}	—	—	0.4	V	
OUTPUT HIGH VOLTAGE @ I_{OUT} = − 100 μA	V_{OH}	2.4	—	—	V	

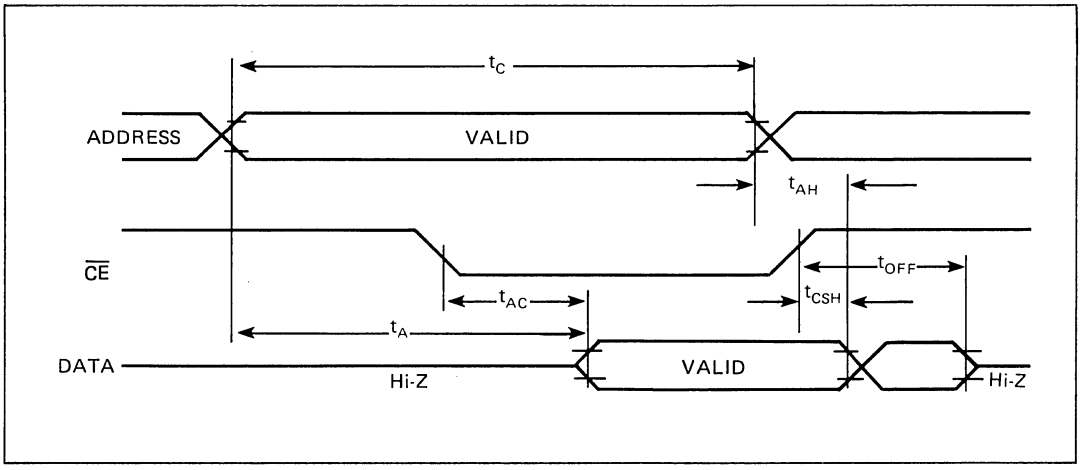
CAPACITANCE (T_A = 0° to + 70°C)

PARAMETER	SYM	TYP	MAX	UNITS	NOTES***
INPUT CAPACITANCE	C_I	5	8	pF	5,6
OUTPUT CAPACITANCE	C_O	7	15	pF	5,6

***NOTES:

1. Current is proportional to cycle rate. I_{DD} is measured at the specified minimum cycle time. Data Outputs open. (V_{IL}=V_{SS} , V_{IH}=V_{DD}.)
2. $\overline{CE} \geq V_{DD} - 0.3V$ or $CE \leq V_{SS} + 0.3V$.
3. V_{IN} = 0.0 V to 5.5 V (V_{DD} = 5.0 V).
4. Device deselected. (V_{OUT} = 0.0 V to 5.5 V).
5. Capitance measured with Boonton Meter or effective capacitance calculated from the equation: $\frac{\Delta Q}{\Delta V}$ with ΔV = 3.0V
6. This parameter is periodically sampled and not 100% tested.
7. Measured with 1 TTL load and 100 pF, transition times ≤ 20 ns. Timing measurement reference levels: inputs 0.8 V and 2.0 V; outputs 0.8 V and 2.0 V.
8. $\overline{CE}$ shown, similar timing is achieved for CE.

TIMING DIAGRAM

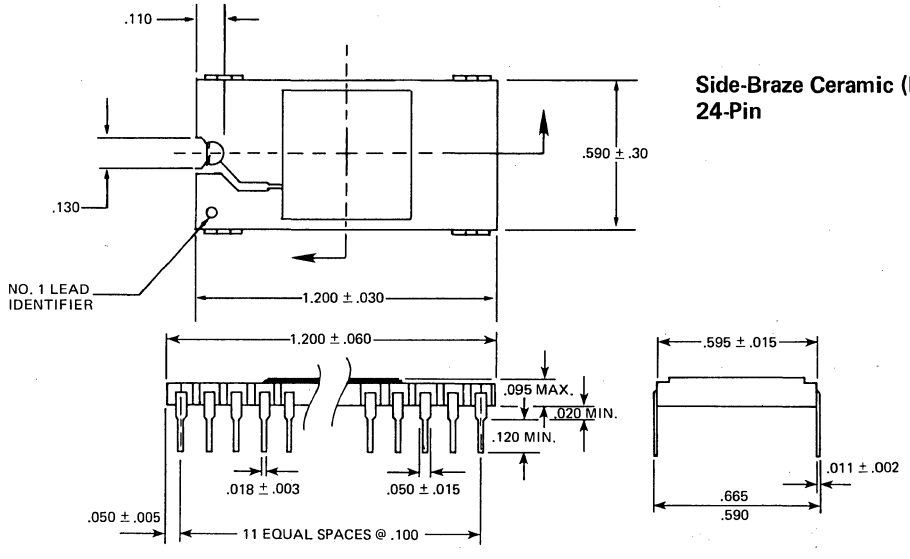


AC CHARACTERISTICS (See Notes 7 and 8, page 2)

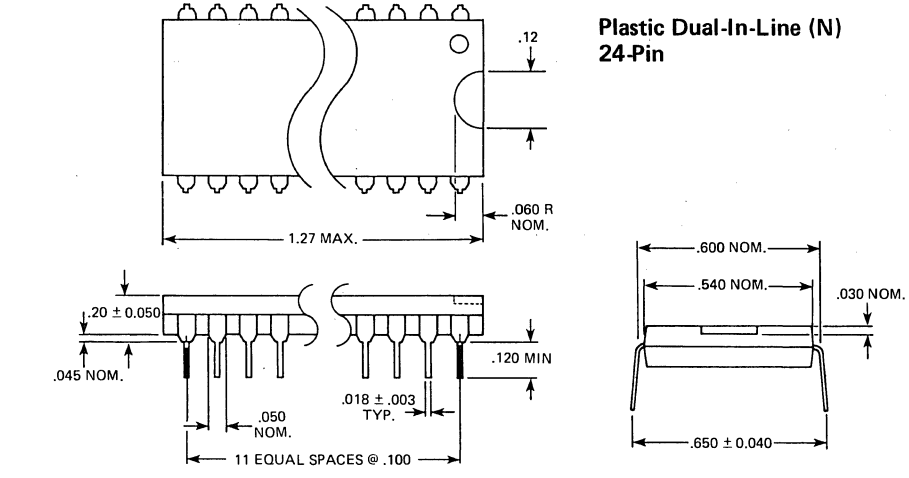
(V_{DD} = 5.0V ± 10%, T_A = 0° to + 70°C)

PARAMETER	SYM	MIN	MAX	UNITS
CYCLE TIME	t_C	250	–	ns
ADDRESS ACCESS TIME	t_A	–	250	ns
CE/$\overline{CE}$ ACCESS TIME	t_{AC}	–	250	ns
OUTPUT TURN OFF DELAY	t_{OFF}	–	50	ns
DATA HOLD FROM CHIP SELECT	t_{CSH}	10	50	ns
DATA HOLD FROM ADDRESS	t_{AH}	10	–	ns

PACKAGE DESCRIPTIONS (All dimensions shown in inches)



Side-Braze Ceramic (P)
24-Pin



Plastic Dual-In-Line (N)
24-Pin

NOTE: Overall length includes .005 flash on either end of package.

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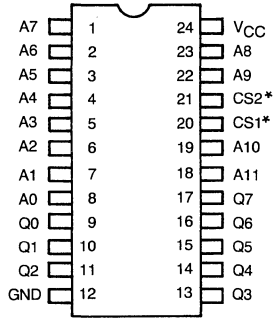
2364A
64K BANK SELECTABLE ROM †

- 64K Mask Programmable ROM
- Organized as two-4Kx8 Banks
- Fully Static 5 Volt Operation
- Maximum Access Time . . . 450 ns
- JEDEC Standard Pin-Out
- Fully TTL Compatible
- Pin Compatible with 2332 Type ROMs
- Programmable Chip Selects

The 2364A is a mask programmable 64K Bank Selectable ROM. A key feature of this device enables the user to access 8K bytes of ROM with only 4K bytes of system address available. This is accomplished by the inclusion of an on-board data latch. This latch essentially is the 13th address bit and is used internally to select one of the 4Kx8 ROM banks. Bank selection is accomplished by accessing address locations FF8 or FF9. Accessing FF8 will select the lower 4K bytes (Bank 0) of the 2364A, and accessing FF9 will select the upper 4K bytes (Bank 1). Except for the bank selection operation, the 2364A functions as a standard 32K ROM, but with twice the memory. This ROM requires only 5 Volts, is fully TTL compatible and is pin compatible with 2332 type ROMs and 2532 type EPROM's. Like the NCR 2332, the two chip select inputs of the 2364A are programmable and are defined by the user.

PIN CONFIGURATION

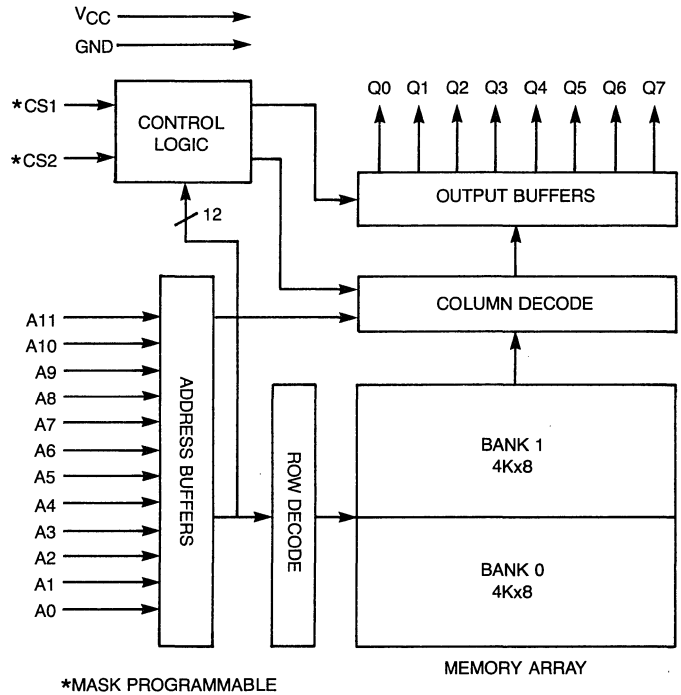


* Active Level (Hi, Low and Don't Care) of chip selects are defined by user.

PIN NAMES

A0-A11	Address Inputs
Q0-Q7	Data Outputs
CS1-CS2	Programmable Chip Selects
V_{CC}	5V ± 10% Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



*MASK PROGRAMMABLE

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† Licensed Under U.S. Patent #4368515

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to ground −.5 to +7V
Storage temperature..... −65°C to 150°C

Stress above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operating conditions stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Supply voltage*	4.5	5.0	5.5	Volts
V_{IH}	Input high level voltage	2.0		V_{CC}	Volts
V_{IL}	Input low level voltage	−0.5		0.8	Volts
T_A	Operating ambient temperature	0		70	°C

*V_{CC} must be applied at least 100 μs before proper device operation is achieved.

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

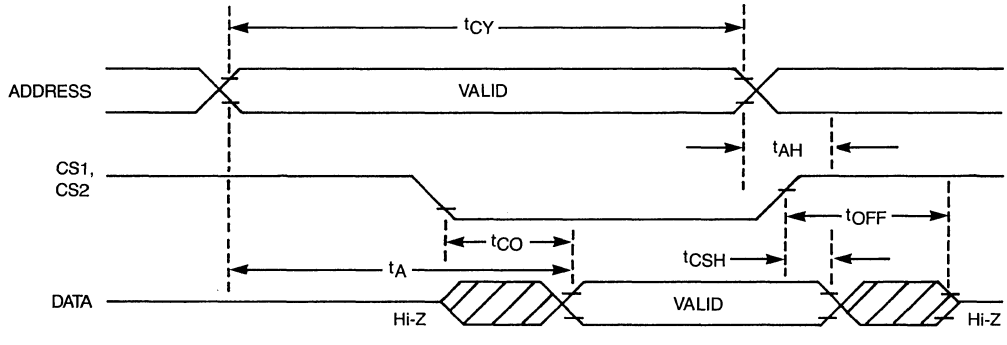
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IN}	Input leakage current	V_{IN}=0V to V_{CC} max.			10	μA
I_O	Output leakage current	V_O = 0.2V to V_{CC} max, Chip Deselected			±10	μA
V_{OH}	Output high voltage	I_{OH}=−160μA	2.4			Volts
V_{OL}	Output low voltage	I_{OL}=1.6mA			0.4	Volts
I_{CC}	Supply current	Outputs Open			85	mA

CAPACITANCE, T_A = 25°C, f=1 MHZ

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
C_{IN}	Input capacitance	All pins except pin			7.0	pF
C_O	Output capacitance	under test are tied to ground			12.5	pF

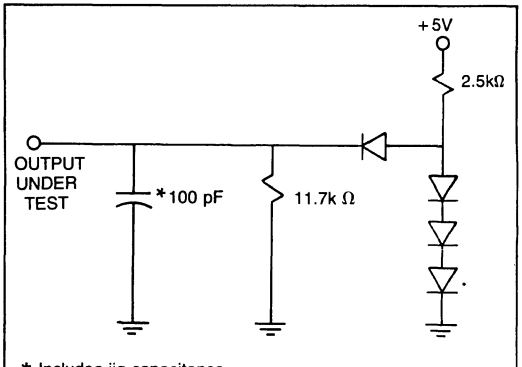
AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{CY}	Cycle Time	450			ns
t_A	Address Access Time			450	ns
t_{CO}	Chip Select Access Time			200	ns
t_{OFF}	Chip Select to Data Off (Hi Z)			200	ns
t_{CSH}	Chip Select to Data Hold	0			ns
t_{AH}	Address to Data Hold	0			ns



NOTE 1 The chip select lines are assumed to be active low.
NOTE 2 Data will be invalid during bank select operation (accessing FF8 or FF9).

AC TEST LOAD CIRCUIT



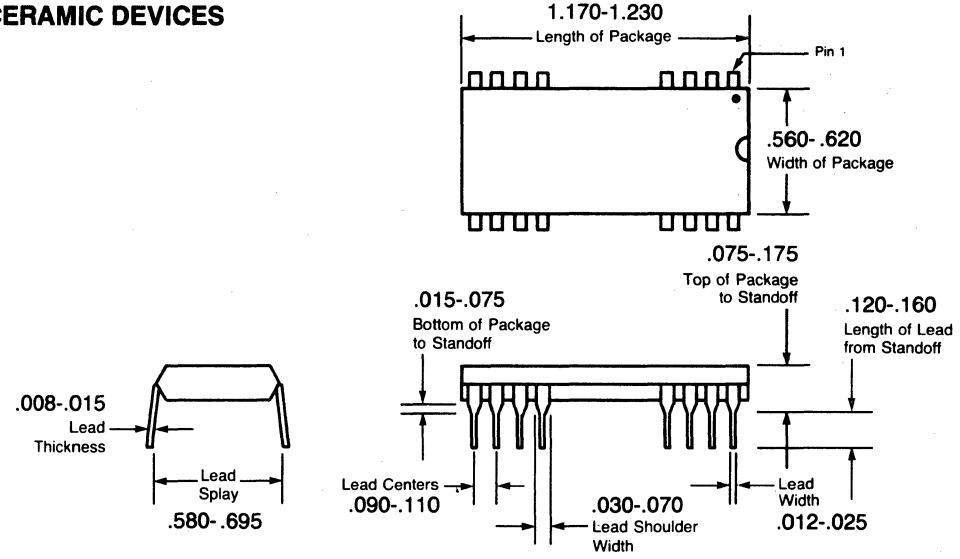
* Includes jig capacitance.
All diodes 1N3064 or equivalent.

A.C. CONDITION OF TESTS

Input Pulse Levels . . . . . .0.8 Volts to 2.0 Volts
Inputs Rise & Fall Times . . . . . .10 ns
Output Timing Levels . . . . . .0.8 Volts to 2.0 Volts

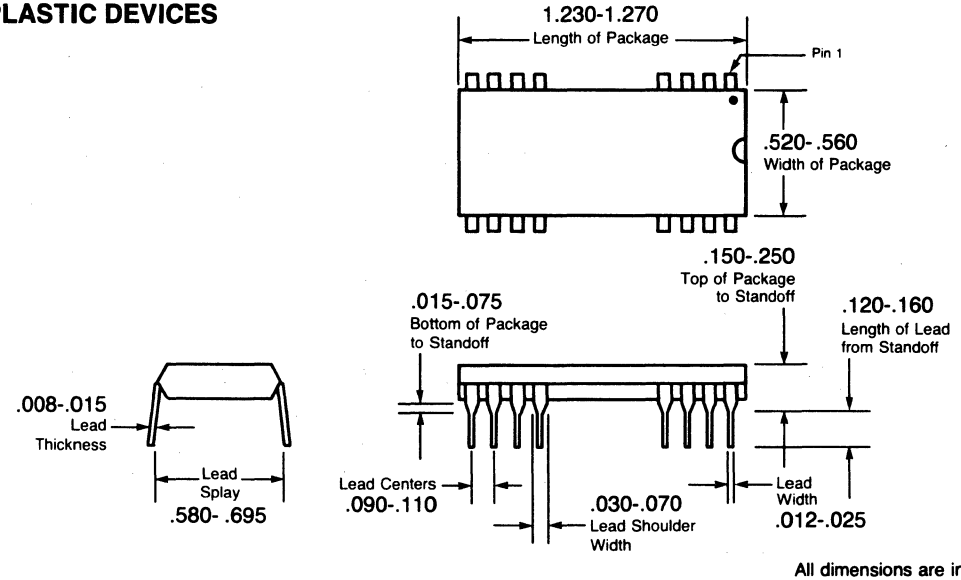
MECHANICAL DATA 24 PIN

CERAMIC DEVICES



All dimensions are inches.

PLASTIC DEVICES



All dimensions are inches.

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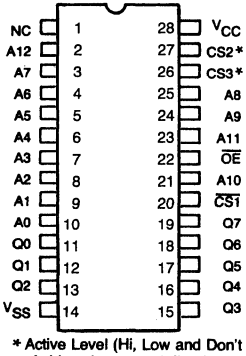
513/866-7217 Ohio or International

2365
64K(8K X 8) ROM

- **Fully Static Operation**
- **Programmable Chip Selects**
- **Maximum Access Time**
  - **2365-25 ..... 250ns**
  - **2365-30 ..... 300ns**
  - **2365-45 ..... 450ns**
- **3-State Outputs**
- **Fully TTL Compatible**
- **Single ±10% 5 Volt Supply**
- **Pin Compatible with 2764 EPROM's**
- **0°to 70°C Operating Range**

The NCR2365 is a mask programmable read-only-memory with an 8K word by 8-bit organization. Designed for ease of use, this device requires only a 5 volt supply, is TTL compatible, and because of its totally static (asynchronous) operation requires no clock. The active levels of two chip select inputs are programmable and are defined by the user. These ROMs are available in a 28 pin package and are pin compatible with 2764 EPROMs.

PIN CONFIGURATION

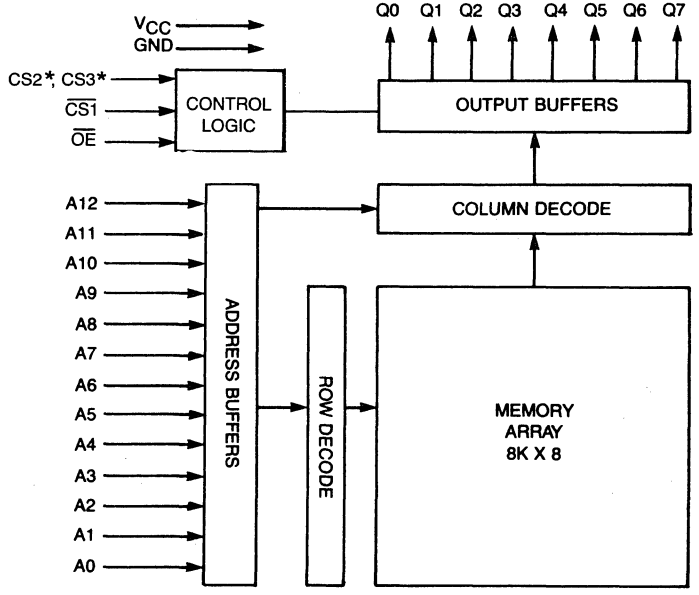


* Active Level (Hi, Low and Don't Care) of chip selects are defined by user.

PIN NAMES

A0 - A12	Address Inputs
Q0 - Q7	Data Outputs
$\overline{CS1}$, CS2, CS3	Chip Selects
V_{CC}	5V ± 10% Supply Voltage
$\overline{OE}$	Output Enable

FUNCTIONAL BLOCK DIAGRAM



*MASK PROGRAMMABLE

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ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to ground −.5 to +7V
Storage temperature..... −65°C to 150°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operating conditions stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Supply voltage*	4.5	5.0	5.5	Volts
V_{IH}	Input high level voltage	2.0		V_{CC}	Volts
V_{IL}	Input low level voltage	−0.5		0.8	Volts
T_A	Operating ambient temperature	0		70	°C

* V_{CC} must be applied at least 100μs before proper device operation is achieved.

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IN}	Input leakage current	V_{IN} = 0V to V_{CC} max			10	μA
I_O	Output leakage current	V_O = 0.2 to V_{CC} max, Chip Deselected			±10	μA
V_{OH}	Output high voltage current	I_{OH} = -160μA	2.4			Volts
V_{OL}	Output low voltage	I_{OL}=1.6mA			0.4	Volts
I_{CC}	Supply current	Outputs Open			85	mA

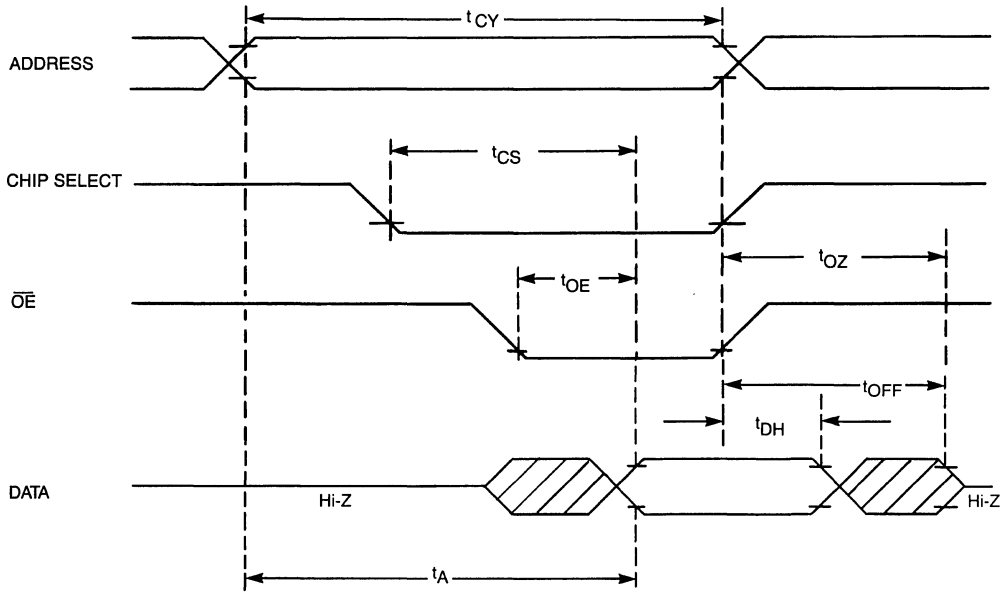
CAPACITANCE, T_A = 25°C, f = 1 MHZ

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
C_{IN}	Input capacitance	All pins except pin under			7	pF
C_o	Output capacitance	test are tied to ground			12.5	pF

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

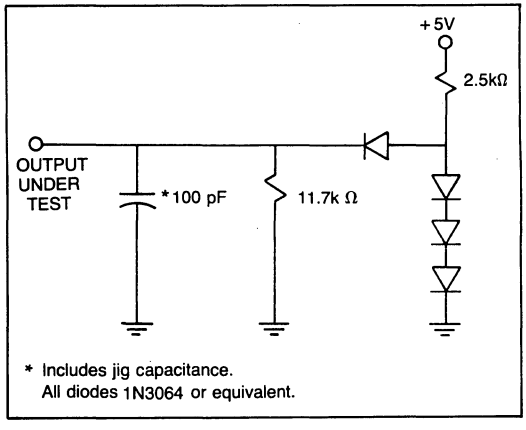
		2365-25			2365-30			2365-45			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{CY}	Cycle time	250			300			450			ns
t_A	Address access time			250			300			450	ns
t_{CS}	Chip select access time			120			150			200	ns
t_{OE}	Output enable to data valid			120			150			200	ns
t_{DH}	Data hold time	0			0			0			ns
t_{OFF}	Chip select or output enable to data Hi-Z			120			150			200	ns

AC WAVEFORMS



Programmable Chip Selects are assumed to be active low.

AC TEST LOAD CIRCUIT



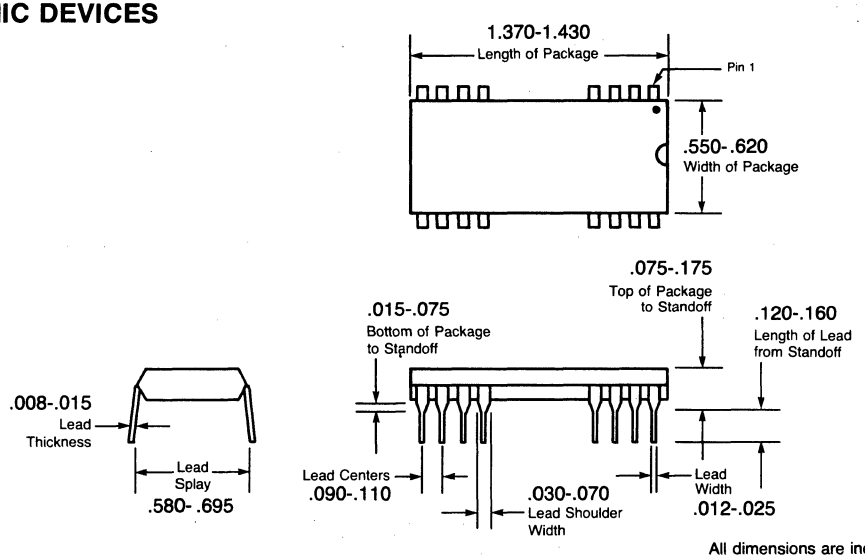
* Includes jig capacitance.
All diodes 1N3064 or equivalent.

A.C. CONDITION OF TESTS

Input Pulse Levels . . . . . .0.8 Volts to 2.0 Volts
Inputs Rise & Fall Times . . . . . .10 ns
Output Timing Levels . . . . . .0.8 Volts to 2.0 Volts

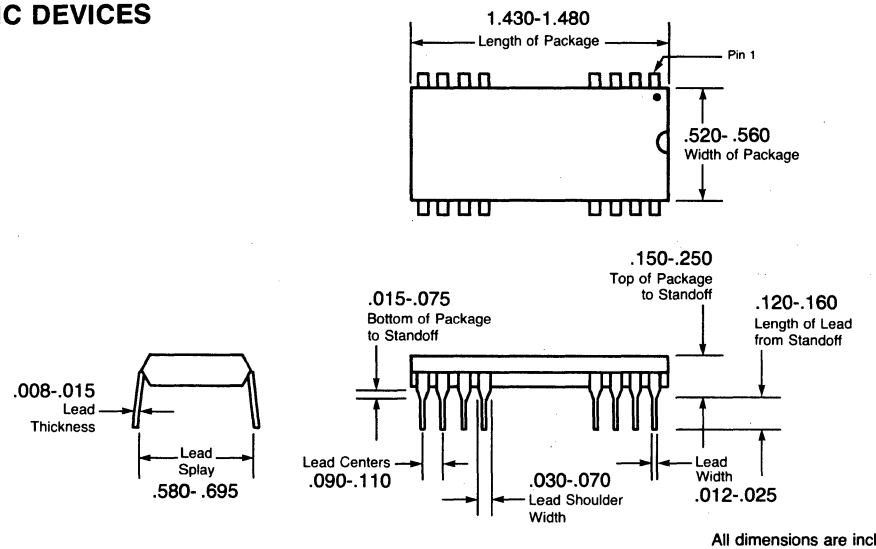
MECHANICAL DATA 28 Pin

CERAMIC DEVICES



All dimensions are inches.

PLASTIC DEVICES



All dimensions are inches.

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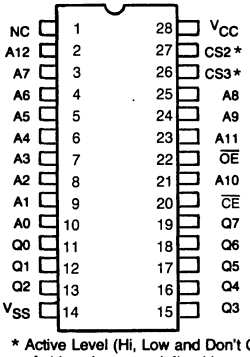
NCR 23C65
64K BIT CMOS MASK ROM

PRELIMINARY

- Access time . . . . . 250 ns max.
- Low power supply current
  - Standby. . . . . 10 μA max.
  - Operation . . . . . 25 mA max.
- Standby power not affected by address transitions
- Completely static
- Single power supply. . . . . +5.0V± 10%
- All inputs and outputs are TTL compatible
- Three-state output for direct bus compatibility
- Pin compatible with EPROMs
- All inputs protected against static charge of 1000 V Nominal
- CS2 & CS3 active level is mask programmable
- Compatible with 2 MHz NCR65C02 Microprocessor

The NCR23C65 is an 8,192 words × 8 bits asynchyronous, static, mask programmable ROM on a monolithic CMOS chip, and is characterized by fast access time and very low power dissipation. The static nature of the memory requires no external clock. Both the inputs and outputs are TTL compatible, and the three-state output allows easy system design and easy expansion of memory capacity. These features make the NCR23C65 usable in a wide-range of applications, especially when lower power dissipation is required in microprocessor systems.

PIN CONFIGURATION

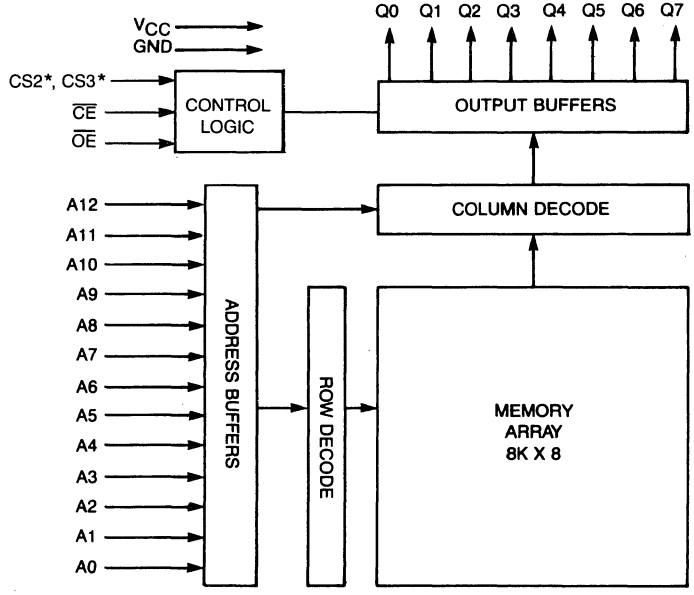


* Active Level (Hi, Low and Don't Care) of chip selects are defined by user.

PIN NAMES

A0 - A12	Address Inputs
Q0 - Q7	Data Outputs
CS3, CS2	Chip Selects
$\overline{CE}$	Chip Enable
V_{CC}	5V ± 10% Supply Voltage
$\overline{OE}$	Output Enable

FUNCTIONAL BLOCK DIAGRAM



*MASK PROGRAMMABLE

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This is advance information and NCR reserves the right to change the specifications without notice.

ABSOLUTE MAXIMUM RATINGS* (V_{CC} = 5.0V ± 10%, V_{SS} = 0.0V, T_A = 0° to + 70°C)

RATING	SYMBOL	VALUE	UNIT
VOLTAGE ON ANY TERMINAL RELATIVE TO V_{SS}	V_{IN}	− 1.0 to + 7.0	V
OPERATING TEMPERATURE (AMBIENT)	T_A	0 to 70	°C
STORAGE TEMPERATURE (CERAMIC)	T_{STG}	− 65 to + 150	°C
STORAGE TEMPERATURE (PLASTIC)	T_{STG}	− 55 to + 125	°C
POWER DISSIPATION	−	1	W

*NOTE: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYM	MIN	TYP	MAX	UNITS
POWER SUPPLY VOLTAGE	V_{CC}	4.5	5.0	5.5	V
INPUT LOW VOLTAGE	V_{IL}	−0.5	−	0.8	V
INPUT HIGH VOLTAGE	V_{IH}	2.0	−	V_{CC}	V

DC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0° to + 70°C)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES***
V_{CC} POWER SUPPLY CURRENT (ACTIVE)	I_{CC}	−	−	25	mA	1
V_{CC} POWER SUPPLY CURRENT (STANDBY)	I_{SB}	−	−	10	μA	2
INPUT LEAKAGE CURRENT	$I_{I(L)}$	− 10	−	10	μA	3
OUTPUT LEAKAGE CURRENT	$I_{O(L)}$	− 10	−	10	μA	4
OUTPUT LOW VOLTAGE @ I_{OUT} = 1.6 mA	V_{OL}	−	−	0.4	V	
OUTPUT HIGH VOLTAGE @ I_{OUT} = − 100 μA	V_{OH}	2.4	−	−	V	

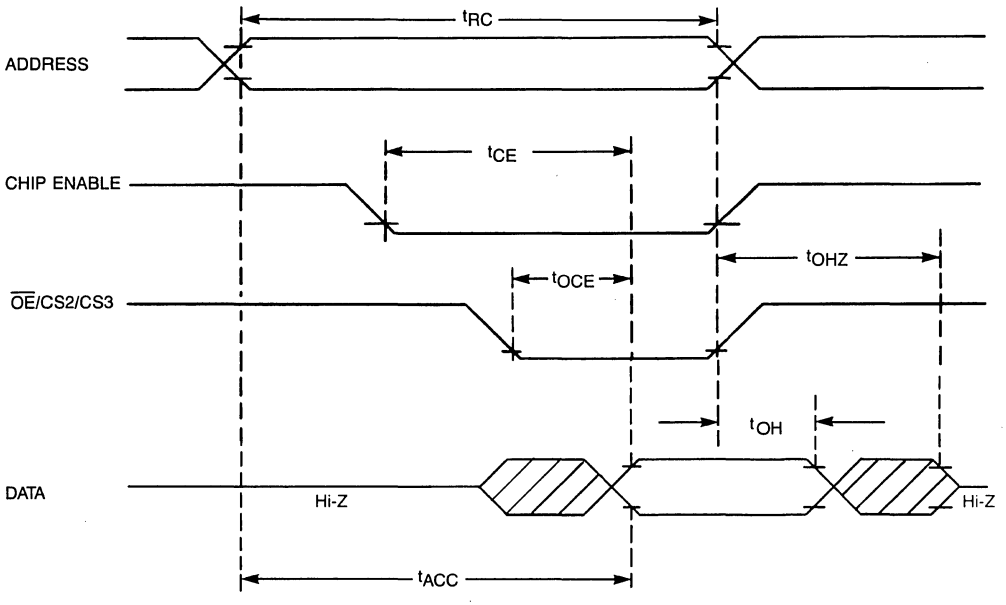
CAPACITANCE (T_A = 0° to + 70°C)

PARAMETER	SYM	TYP	MAX	UNITS	NOTES***
INPUT CAPACITANCE	C_I	5	8	pF	5,6
OUTPUT CAPACITANCE	C_O	7	15	pF	5,6

***NOTES:

1. Current is proportional to cycle rate. I_{CC} is measured at the specified minimum cycle time. Data Outputs open. (V_{IL}=V_{SS} , V_{IH}=V_{CC}.)
2. $\overline{CE} \geq V_{CC} - 0.3V$ or $CE \leq V_{SS} + 0.3V$.
3. V_{IN} = 0.0 V to 5.5 V (V_{CC} = 5.0 V).
4. Device deselected. (V_{OUT} = 0.0 V to 5.5 V).
5. Capitance measured with Boonton Meter or effective capacitance calculated from the equation: $\frac{\Delta Q}{\Delta V}$ with ΔV = 3.0V
6. This parameter is periodically sampled and not 100% tested.
7. Measured with 1 TTL load and 100 pF, transition times ≤20 ns. Timing measurement reference levels: inputs 0.8 V and 2.0 V; outputs 0.8 V and 2.0 V.
8. $\overline{CE}$ shown, similar timing is achieved for CE.

AC WAVEFORMS



Programmable Chip Selects are assumed to be active low.

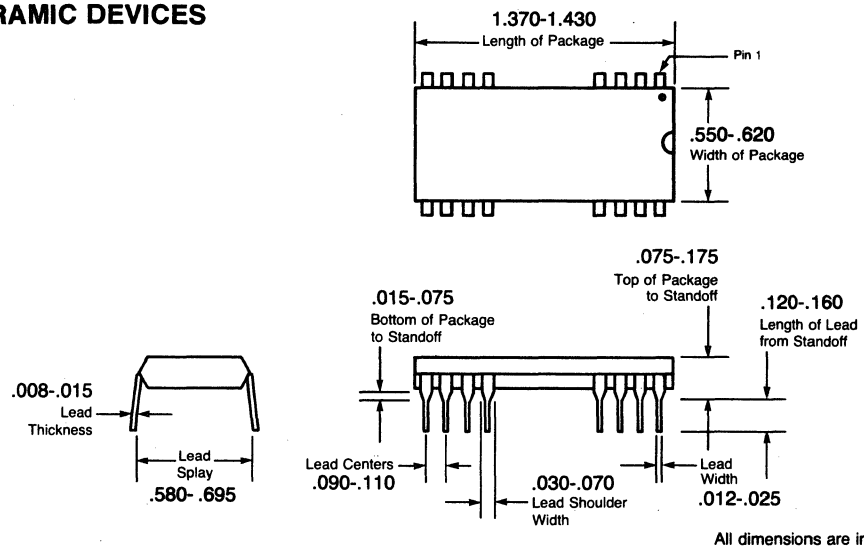
AC CHARACTERISTICS (See Notes 7 and 8, page 2)

(V_{CC} = 5.0V ± 10%, T_A = 0° to + 70°C)

Parameter	Sym	Min	Max	Units
Cycle Time	t_{RC}	250	—	ns
Address Access Time	t_{ACC}	—	250	ns
CE Access Time	t_{CE}	—	250	ns
$\overline{OE}$/CS Access Time	t_{OCE}	—	150	ns
Control to Output High Impedance	t_{OHZ}	—	50	ns
Data Hold From CE, $\overline{OE}$, or Address	t_{OH}	10	—	ns

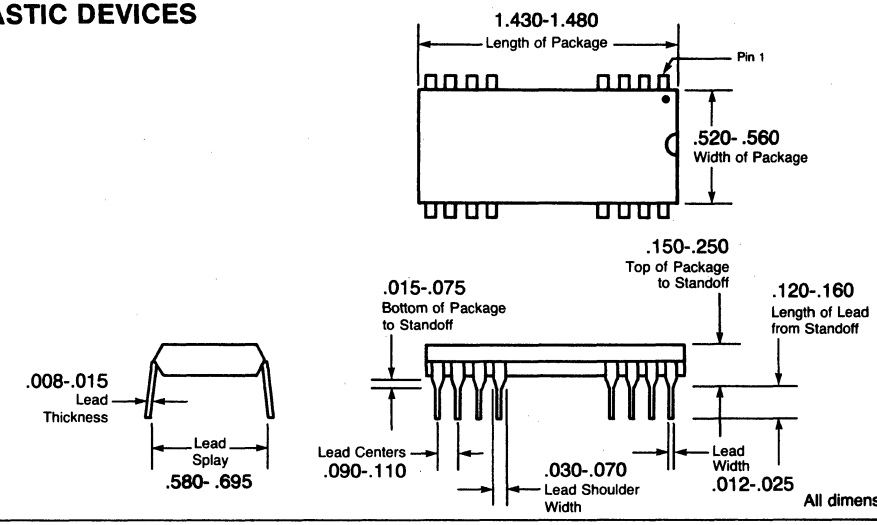
MECHANICAL DATA 28 Pin

CERAMIC DEVICES



All dimensions are inches.

PLASTIC DEVICES



All dimensions are inches.

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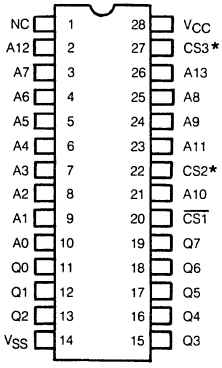
23128
128K (16K X 8) ROM

- **23128 . . . Non-Power Down**
- **23128S . . . Automatic Power Down**
- **Fully Static Operation**
- **Silicon Gate NMOS Technology**
- **Maximum Access Times**
  - **23128/23128S-25 . . . 250ns**
  - **23128/23128S-30 . . . 300ns**
  - **23128/23128S-45 . . . 450ns**
- **Fully TTL Compatible**
- **5 Volt Only Operation**
- **Byte-Wide Industry Standard JEDEC Pin-Out**
- **0°C to 70°C Operating Range**

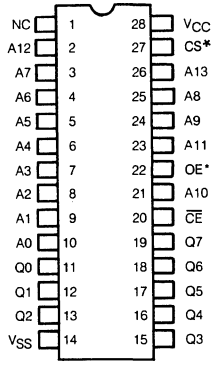
The NCR 23128 is a mask programmable read-only-memory with a 16K word by 8 bit organization. Designed for ease of use, this device requires only a 5 volt supply, is TTL compatible, and because of its totally static (asynchronous) operation, requires no clock. This memory device is available in two versions. The NCR 23128 is a non-power down version where the active level of chip selects CS2 and CS3 is programmable and is defined by the user to facilitate system memory expansion. The NCR 23128S offers an automatic power down feature (standby) controlled by the chip enable $\overline{CE}$ input. When $\overline{CE}$ goes high, the device automatically powers down and remains in a low power standby mode as long as $\overline{CE}$ remains high. Also, on the 23128S, the active level of chip select CS and output enable OE is programmable, thus eliminating bus contention in multiplexed bus microprocessor systems. The NCR 23128 is packaged in a 28 pin DIP with an industry standard byte-wide JEDEC pin-out.

PIN CONFIGURATION

NCR 23128



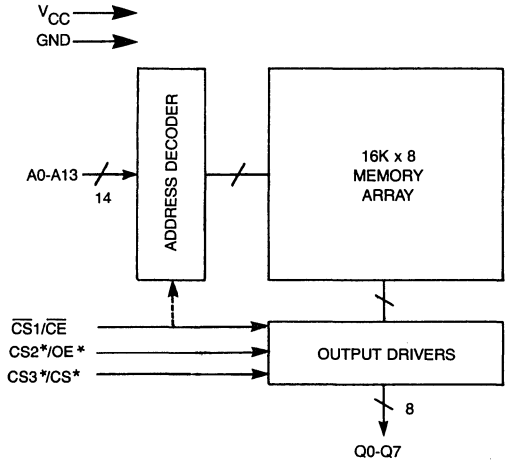
NCR 23128S



* Programmable Active High or Low

NOTE:
23128 Only: Chip Selects $\overline{CS1}$, CS2 and CS3 are normally AND'd, ie, ($\overline{CS1}$•CS2•CS3). At the option of the user, $\overline{CS1}$ and CS2 may be internally OR'd and then AND'd with CS3 ie, [($\overline{CS1}$ + CS2)•CS3]

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0 - A_{13}	Address Inputs	$\overline{CE}$	Chip Enable
Q_0 - Q_7	Data Outputs	OE	Output Enable
$\overline{CS1}$, CS2, CS3, CS	Chip Selects	V_{CC}	5 Volt ± 10% Power Supply
NC	No Connection		

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ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to ground ..... −0.5 to +7V
Storage temperature..... −65°C to 150°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operating conditions stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply voltage*	4.5	5.0	5.5	Volts
V_{IH}	Input high level voltage	2.0		V_{CC}	Volts
V_{IL}	Input low level voltage	-0.5		0.8	Volts
T_A	Operating ambient temperature	0		70	°C

*V_{CC} must be applied at least 100 μs before proper device operation is achieved.

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{IN}	Input leakage current	V_{IN} = 0V to V_{CC} max			10	μA
I_O	Output leakage current	V_O = 0.2 to V_{CC} max, Chip Deselected			±10	μA
V_{OH}	Output high voltage	I_{OH} = -200μA	2.4			Volts
V_{OL}	Output low voltage	I_{OL} = 3.2mA			0.4	Volts
I_{CC}	Supply current — Active	Outputs Open			75	mA
I_{SB}*	Supply current — Standby	Chip Deselected			10	mA

* Applies to 23128S Power Down Version only.

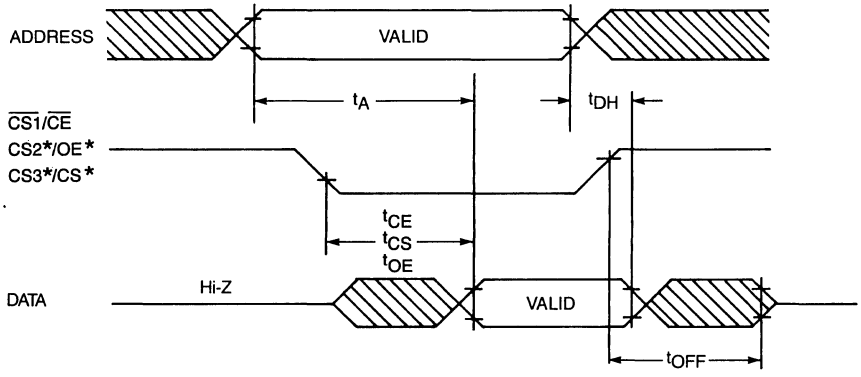
CAPACITANCE, T_A = 25°C, f = 1 MHZ

Symbol	Parameter	Condition	Min	Typ	Max	Units
C_{IN}	Input capacitance	All pins except pin under test are tied to ground			7.0	pF
C_O	Output capacitance				12.5	pF

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	23128-25 23128S-25			23128-30 23128S-30			23128-45 23128S-45			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_A	Address Access Time			250			300			450	ns
t_{CE}	Chip Enable Access Time			250			300			450	ns
t_{CS}	Chip Select Access Time			120			150			200	ns
t_{OE}	Output Enable Access Time			120			150			200	ns
t_{DH}	Data Hold Time	0			0			0			ns
t_{OFF}	CS Active to Data High Impedance			120			150			200	ns

AC WAVEFORMS

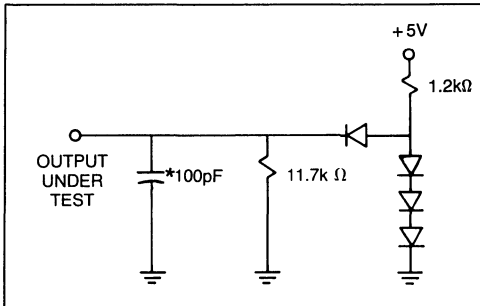


*Programmable Chip Selects CS, CS2 and CS3 and Output Enable OE are assumed to be active low for this example.

A. C. CONDITIONS OF TESTS

Input Pulse Levels.....0.8 Volts to 2.0 Volts
Input Rise and Fall Times.....10 ns
Output Timing Levels .....0.8 Volts to 2.0 Volts

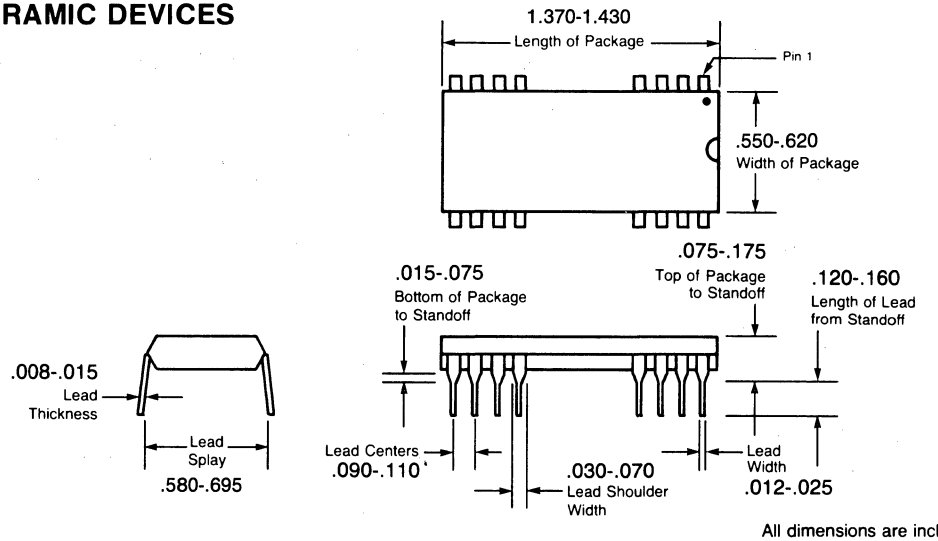
AC TEST LOAD CIRCUIT



* Includes jig capacitance.
All diodes 1N3064 or equivalent.

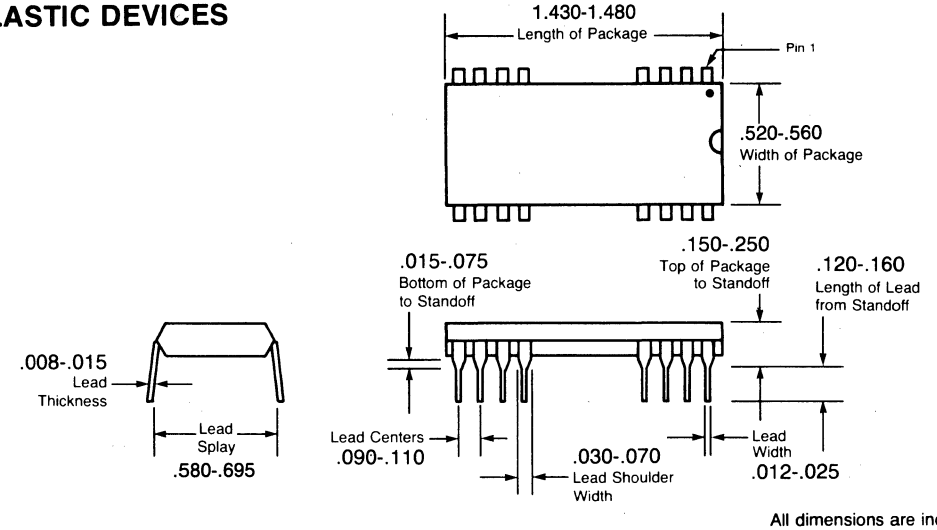
MECHANICAL DATA 28 PIN

CERAMIC DEVICES



All dimensions are inches.

PLASTIC DEVICES



All dimensions are inches.

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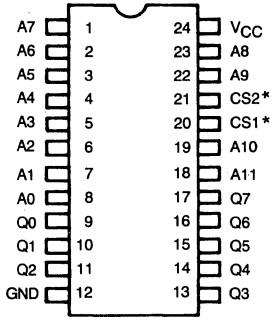
23128A
128K BANK SELECTABLE ROM†

- 128K Mask Programmable ROM
- Organized as 4-4K x 8 Banks
- Fully Static 5 Volt Operation
- Maximum Access Time ..... 450 ns
- JEDEC Standard Pin-Out
- Fully TTL Compatible
- Pin Compatible with 2332 Type ROMs
- Programmable Chip Selects

The 23128A is a mask programmable 128K Bank Selectable ROM. A key feature of this device enables the user to access 16K bytes of ROM with only 4K bytes of system address available. This is accomplished by the inclusion of on-board data latches. These latches serve as the 13th and 14th address bits, and are used internally to select one of the 4K x 8 ROM banks. Bank selection is accomplished by accessing address locations FF6, FF7, FF8 and FF9. An access of FF6 selects the lowest 4K bytes (Bank 0), FF7 selects the lower middle 4K bytes (Bank 1), FF8 selects the upper middle 4K bytes (Bank 2), and FF9 selects the highest 4K bytes (Bank 3). Except for the bank selection operation, the 23128A functions as a standard 32K ROM, but with four times the memory. This ROM requires only 5 volts, is fully TTL compatible, and is pin-compatible with 2332 type ROMs and 2532 type EPROMs. Like the NCR 2332 and 2364A, the two chip select inputs of the 23128A are programmable and are defined by the user.

PIN CONFIGURATION

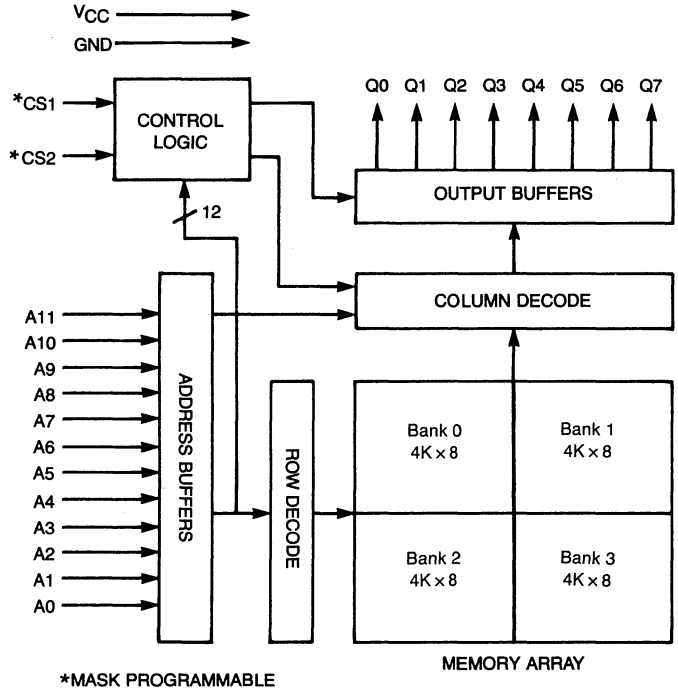


* Active Level (Hi, Low and Don't Care) of chip selects are defined by user.

PIN NAMES

A0-A11	Address Inputs
Q0-Q7	Data Outputs
CS1-CS2	Programmable Chip Selects
V_{CC}	5V ± 10% Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



*MASK PROGRAMMABLE

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† Licensed Under U.S. Patent #4368515

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to ground −.5 to +7V
Storage temperature..... −65°C to 150°C

Stress above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operating conditions stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Supply voltage*	4.5	5.0	5.5	Volts
V_{IH}	Input high level voltage	2.0		V_{CC}	Volts
V_{IL}	Input low level voltage	−0.5		0.8	Volts
T_A	Operating ambient temperature	0		70	°C

* V_{CC} must be applied at least 100 μs before proper device operation is achieved.

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IN}	Input leakage current	V_{IN}=0V to V_{CC} max.			10	μA
I_O	Output leakage current	V_O = 0.2 to V_{CC} max, Chip Deselected			±10	μA
V_{OH}	Output high voltage	I_{OH}=−160μA	2.4			Volts
V_{OL}	Output low voltage	I_{OL}=1.6mA			0.4	Volts
I_{CC}	Supply current	Outputs Open			110	mA

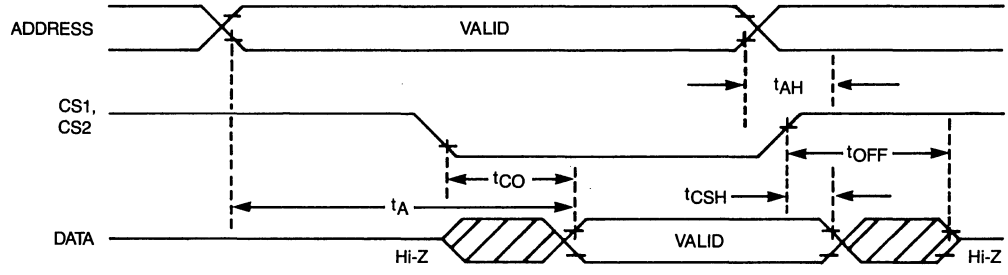
CAPACITANCE, T_A = 25°C, f=1 MHZ

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
C_{IN}	Input capacitance	All pins except pin			7.0	pF
C_O	Output capacitance	under test are tied to ground			12.5	pF

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

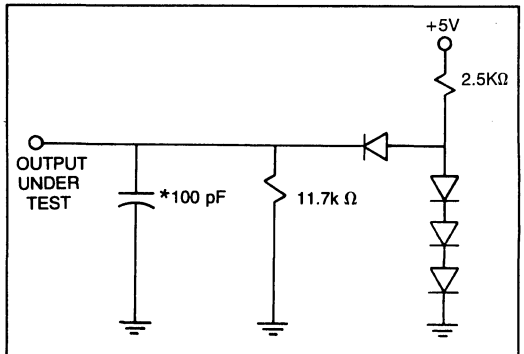
Symbol	Parameter	Min.	Typ.	Max.	Units
t_A	Address Access Time			450	ns
t_{CO}	Chip Select Access Time			200	ns
t_{OFF}	Chip Select to Data Off (Hi Z)			200	ns
t_{CSH}	Chip Select to Data Hold	0			ns
t_{AH}	Address to Data Hold	0			ns

AC WAVE FORMS



NOTE 1 The chip select lines are assumed to be active low.
NOTE 2 Data will be invalid during bank select operation (accessing FF6, FF7, FF8 or FF9)

AC TEST LOAD CIRCUIT



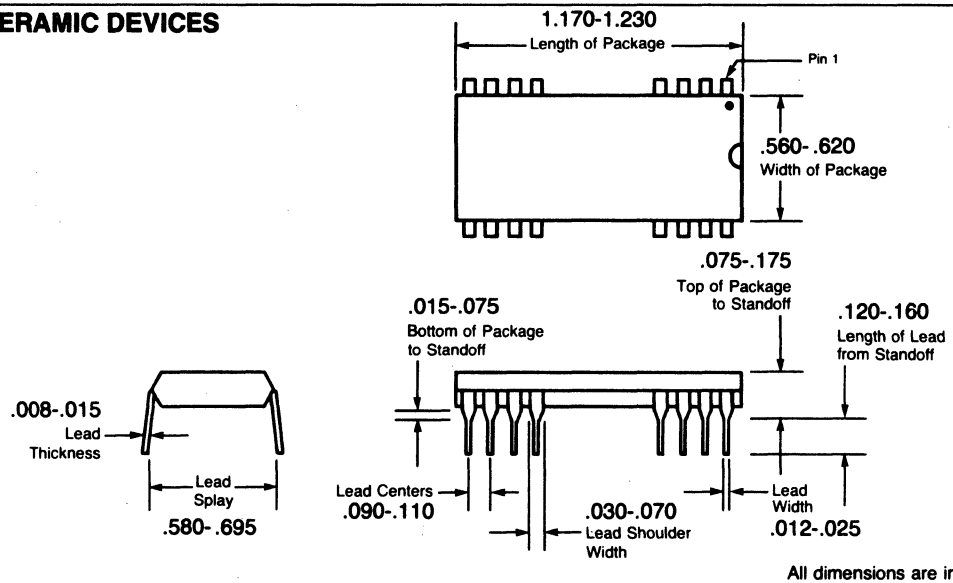
* Includes jig capacitance.
All diodes 1N3064 or equivalent.

A.C. CONDITION OF TESTS

Input Pulse Levels . . . . . .0.8 Volts to 2.0 Volts
Inputs Rise & Fall Times . . . . . .10 ns
Output Timing Levels . . . . . .0.8 Volts to 2.0 Volts

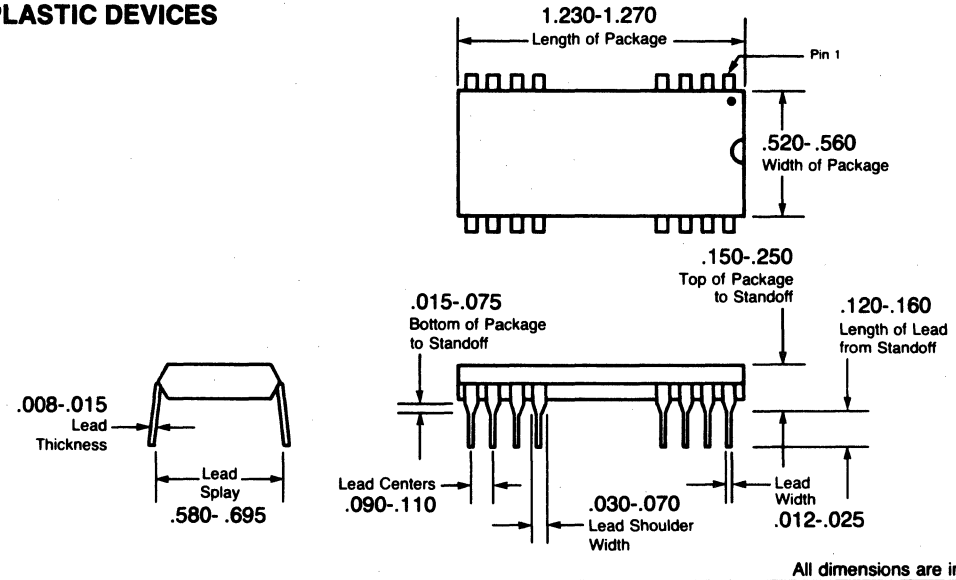
MECHANICAL DATA 24 PIN

CERAMIC DEVICES



All dimensions are inches.

PLASTIC DEVICES



All dimensions are inches.

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513/866-7217 Ohio or International

23256
256K (32K X 8) ROM

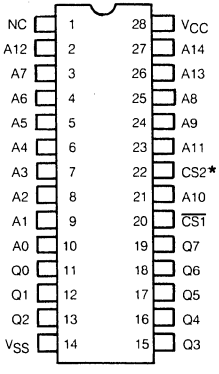
- **23256 . . . Non-Power Down**
- **23256 S . . . Automatic Power Down**
- **Fully Static Operation**
- **Silicon Gate NMOS Technology**
- **Maximum Access Times**
  - **23256/23256S-20 . . 200ns**
  - **23256/23256S-25 . . 250ns**
  - **23256/23256S-30 . . 300ns**
  - **23256/23256S-45 . . 450ns**
- **Fully TTL Compatible**
- **5 Volt Only Operation**
- **Byte-Wide Industry Standard JEDEC Pin-Out**
- **0° to 70° Operating Range**

The NCR 23256 is a mask programmable read-only-memory with a 32K word by 8 bit organization. Designed for ease of use, this device requires only a 5 volt supply, is TTL compatible, and because of its totally static (asynchronous) operation, requires no clock. This memory device is available in two versions. The NCR 23256 is a non-power down version where the active level of chip select CS2 is programmable and is defined by the user to facilitate system memory expansion. The NCR 23256S offers an automatic power down feature (standby) controlled by the chip enable $\overline{CE}$ input. When $\overline{CE}$ goes high, the device automatically powers down and remains in a low power standby mode as long as $\overline{CE}$ remains high. Also, on the 23256S, the active level of output enable OE is programmable, thus eliminating bus contention in multiplexed bus microprocessor systems. The NCR 23256 is packaged in a 28 pin DIP with an industry standard byte-wide JEDEC pin-out.

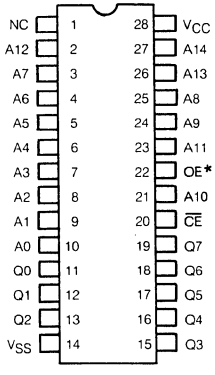
This 256K ROM is also available with an alternate pin-out where pin 1 = A14 and pin 27 = NC. The alternate pin-out part is identified as the NCR 23257 and is described in a separate data sheet.

PIN CONFIGURATION

NCR 23256



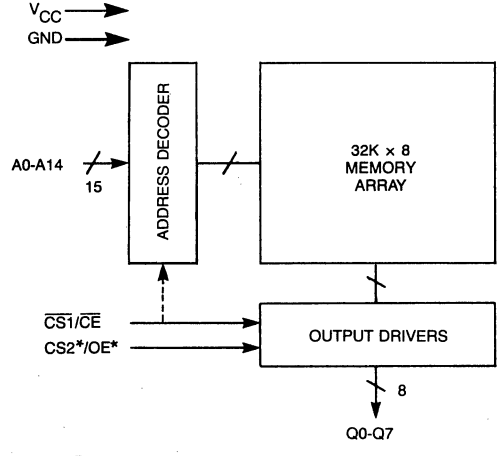
NCR 23256S



* Programmable Active High or Low

NOTE:
23256 Only: Chip Selects $\overline{CS1}$ and CS2 are normally AND'd, but may be internally OR'd at the option of the user.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0 - A_{14}	Address Inputs	OE	Output Enable
Q_0 - Q_7	Data Outputs	$\overline{CE}$	Chip Enable
$\overline{CS1}$, CS2	Chip Selects	V_{CC}	5 Volt ± 10% Power Supply
NC	No Connection		

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NCR

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to ground ..... −0.5 to +7V
Storage temperature ..... −65°C to 150°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operating conditions stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply voltage*	4.5	5.0	5.5	Volts
V_{IH}	Input high level voltage	2.0		V_{CC}	Volts
V_{IL}	Input low level voltage	−0.5		0.8	Volts
T_A	Operating ambient temperature	0		70	°C

*V_{CC} must be applied at least 100 μs before proper device operation is achieved.

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{IN}	Input leakage current	V_{IN} = 0V to V_{CC} max,			10	μA
I_O	Output leakage current	V_O = 0.2 to V_{CC} max, Chip Deselected			±10	μA
V_{OH}	Output high voltage	I_{OH} = −200 μA	2.4			Volts
V_{OL}	Output low voltage	I_{OL} = 3.2mA			0.4	Volts
I_{CC}	Supply current — Active	Outputs Open			95	mA
I_{SB}*	Supply current — Standby	Chip Deselected			10	mA

*Applies to 23256S Power Down Version Only

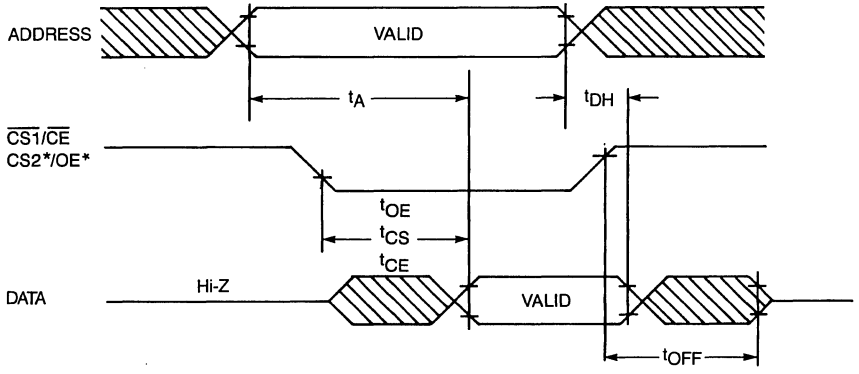
CAPACITANCE, T_A = 25°C, f = 1 MHZ

Symbol	Parameter	Condition	Min	Typ	Max	Units
C_{IN}	Input capacitance	All pins except pin under test are tied to ground			7.0	pF
C_O	Output capacitance				12.5	pF

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	23256-20 23256S-20		23256-25 23256S-25		23256-30 23256S-30		23256-45 23256S-45		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_A	Address Access Time		200		250		300		450	ns
t_{CE}	Chip Enable Access Time		200		250		300		450	ns
t_{CS}	Chip Select Access Time		100		120		150		200	ns
t_{OE}	Output Enable Access Time		100		120		150		200	ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{OFF}	CS Active to Data High Impedance		100		120		150		200	ns

AC WAVEFORMS

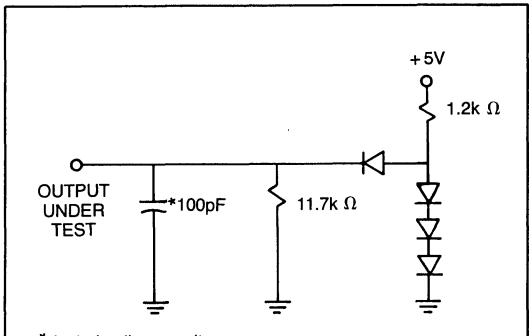


* Programmable Chip Select CS2 and Output Enable OE are assumed to be active low for this example.

AC CONDITION OF TESTS

Input Pulse Levels . . . . . .0.8 Volts to 2.0 Volts
Input Rise and Fall Times . . . . . .10 ns
Output Timing Levels . . . . . .0.8 Volts to 2.0 Volts

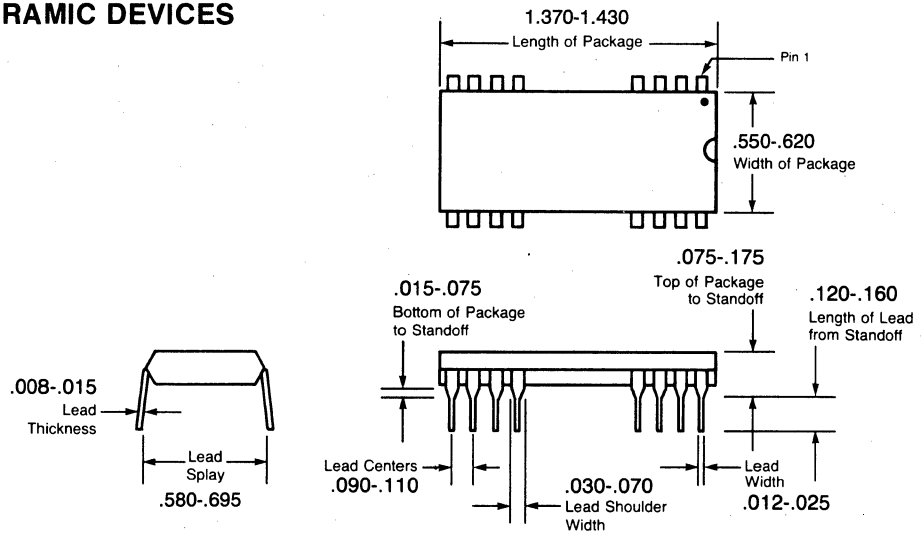
AC TEST LOAD CIRCUIT



* Includes jig capacitance.
All diodes 1N3064 or equivalent.

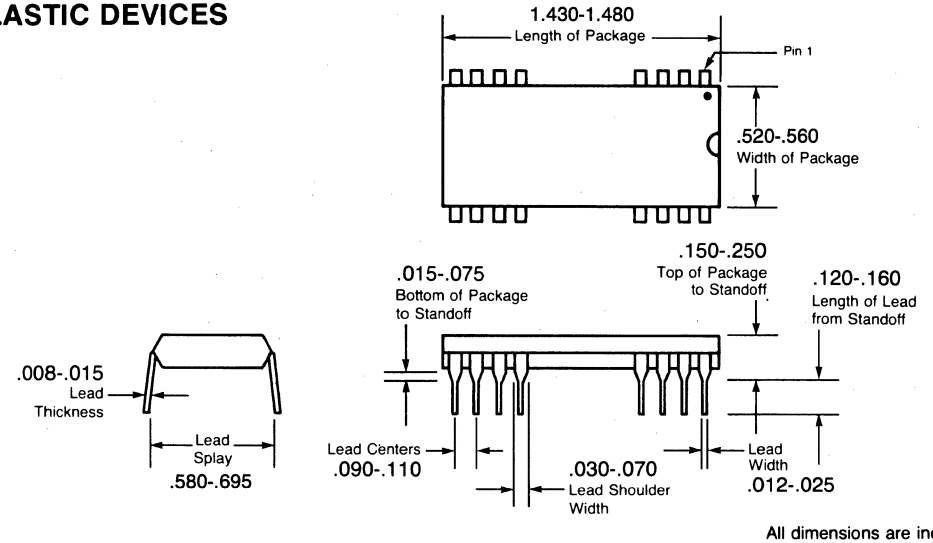
MECHANICAL DATA 28 PIN

CERAMIC DEVICES



All dimensions are inches.

PLASTIC DEVICES



All dimensions are inches.

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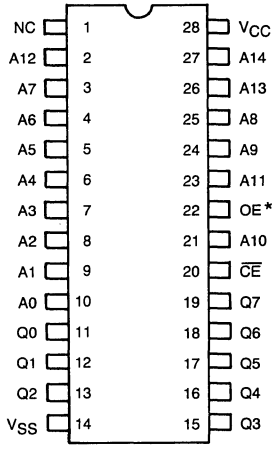
23C256
256K (32K × 8) CMOS ROM

PRELIMINARY

- **Fully Static Operation**
- **Silicon Gate CMOS Technology**
- **Maximum Access Time ..... 250 ns**
- **Fully TTL Compatible**
- **5 Volt Only Operation**
- **Byte-Wide Industry Standard JEDEC Pin-Out**

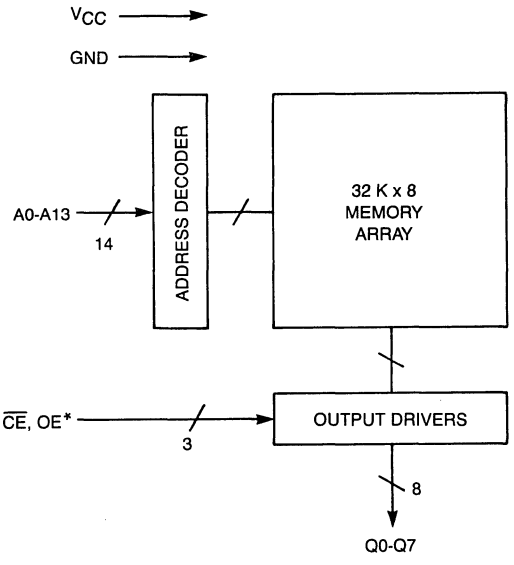
The NCR 23C256 is a mask programmable read-only-memory with a 32K word by 8 bit organization. Designed for ease of use, this device requires only a 5 volt power supply, is TTL compatible, and because of its totally static (asynchronous) operation, requires no clock. This CMOS ROM offers very low power dissipation in the operational mode and has an automatic power down feature that significantly reduces power consumption in the standby mode. The active level of output enable OE is programmable, thus eliminating bus contention in multiplexed bus microprocessor systems. The NCR 23C256 is packaged in a 28 pin DIP with an industry standard byte-wide JEDEC pin-out.

PIN CONFIGURATION



*Programmable Chip Select

FUNCTIONAL BLOCK DIAGRAM



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This is advance information and NCR reserves the right to change the specifications without notice.

NCR

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to ground ..... -0.5 to +7V
Storage temperature ..... -65°C to 150°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operating conditions stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply voltage*	4.5	5.0	5.5	Volts
V_{IH}	Input high level voltage	2.0		V_{CC}	Volts
V_{IL}	Input low level voltage	-0.3		0.8	Volts
T_A	Operating ambient temperature	0		70	°C

*V_{CC} must be applied at least 100 μs before proper device operation is achieved.

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_N	Input leakage current	V_{IN} = 0V to V_{CC} max			10	μA
I_O	Output leakage current	V_O = 0.2 to V_{CC} max Chip Deselected			±10	μA
V_{OH}	Output high voltage	I_{OH} = -200μA	2.4			Volts
V_{OL}	Output low voltage	I_{OL} = 3.2mA			0.4	Volts
I_{CC}	Supply current—active	Outputs Open			40	mA
I_{SB}	Supply current—standby	Chip Deselected			100	μA

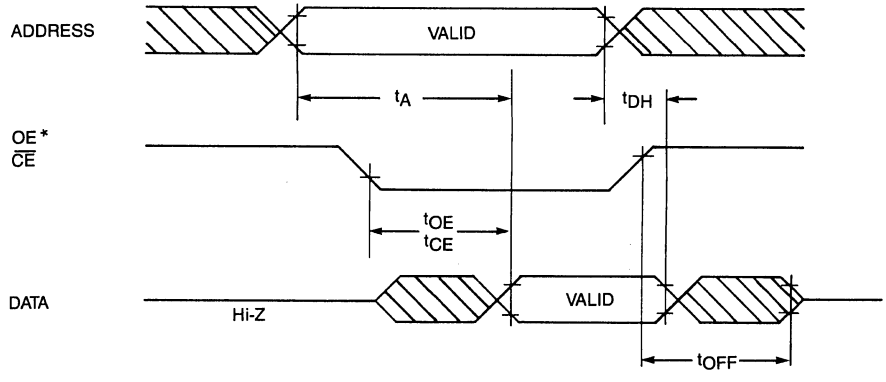
CAPACITANCE, T_A = 25°C, f = 1 MHZ

Symbol	Parameter	Condition	Min	Typ	Max	Units
C_{IN}	Input capacitance	All pins except pin under test			10.0	pF
C_O	Output capacitance	are tied to ground			12.5	pF

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

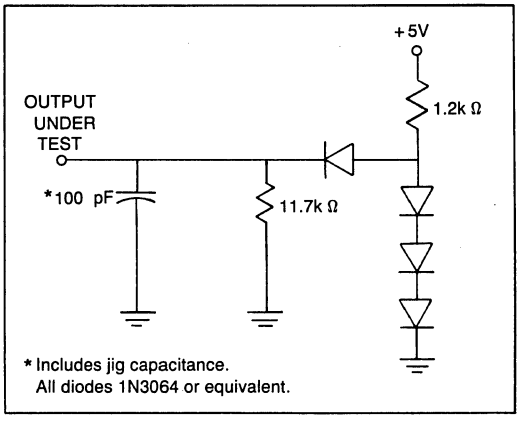
Symbol	Parameter	Min	Typ	Max	Units
t_A	Address Access Time			250	ns
t_{CE}	Chip Enable Access Time			250	ns
t_{OE}	Output Enable Access Time			120	ns
t_{DH}	Data Hold Time	0			
t_{OFF}	CS Active to Data High Impedance			120	ns

AC WAVEFORMS



***NOTE:** Programmable Output Enable OE is assumed to be active low for this example.

AC TEST LOAD CIRCUIT



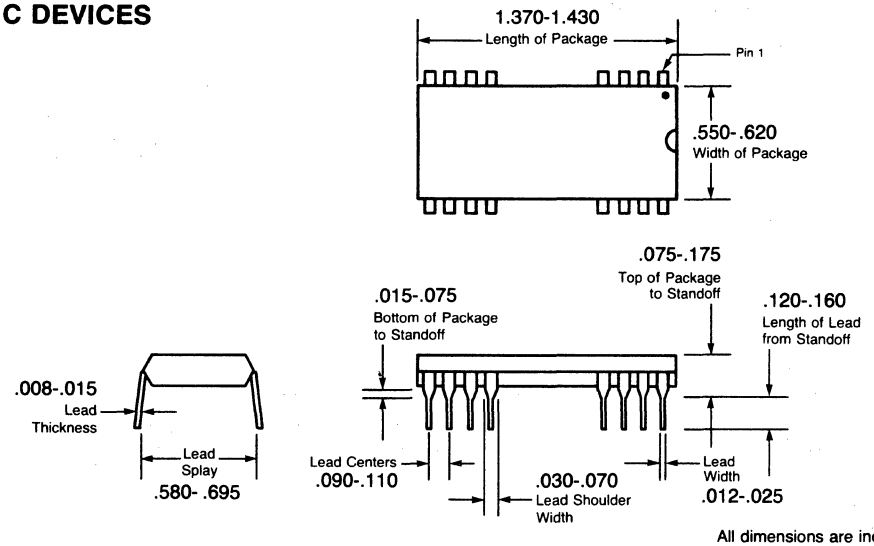
* Includes jig capacitance.
All diodes 1N3064 or equivalent.

AC CONDITIONS OF TEST

Input Pulse Levels ..... 0.8 volts to 2.0 volts
Input Rise & Fall Times ..... 10 ns
Output Timing Levels ..... 0.8 volts to 2.0 volts

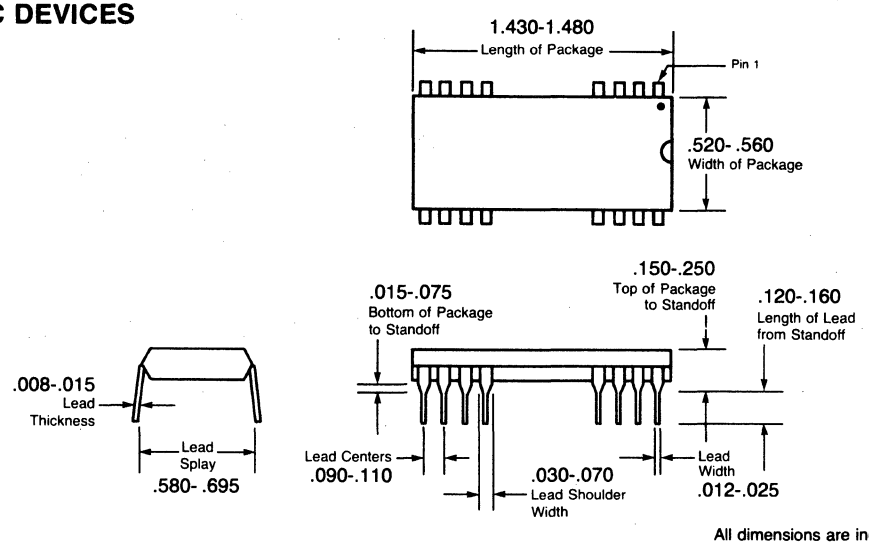
MECHANICAL DATA 28 Pin

CERAMIC DEVICES



All dimensions are inches.

PLASTIC DEVICES



All dimensions are inches.

NCR Microelectronics Division
8181 Byers Road
Miamisburg, Ohio 45342
Telex: 241669 NCR NVMEM MSBG
Phone: 1-800-543-5618 outside Ohio
513/866-7217 Ohio or International

23257
256K (32K X 8) ROM

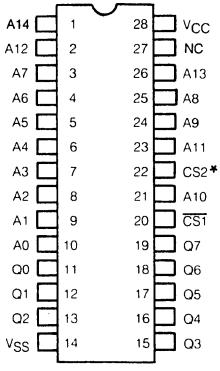
- **23257 . . . Non-Power Down**
- **23257 S . . . Automatic Power Down**
- **Fully Static Operation**
- **Silicon Gate NMOS Technology**
- **Maximum Access Times**
  - **23257/23257S-20 . . 200ns**
  - **23257/23257S-25 . . 250ns**
  - **23257/23257S-30 . . 300ns**
  - **23257/23257S-45 . . 450ns**
- **Fully TTL Compatible**
- **5 Volt Only Operation**
- **Byte-Wide Industry Standard JEDEC Pin-Out**
- **0° to 70° Operating Range**

The NCR 23257 is a mask programmable read-only-memory with a 32K word by 8 bit organization. Designed for ease of use, this device requires only a 5 volt supply, is TTL compatible, and because of its totally static (asynchronous) operation, requires no clock. This memory device is available in two versions. The NCR 23257 is a non-power down version where the active level of chip select CS2 is programmable and is defined by the user to facilitate system memory expansion. The NCR 23257S offers an automatic power down feature (standby) controlled by the chip enable $\overline{CE}$ input. When $\overline{CE}$ goes high, the device automatically powers down and remains in a low power standby mode as long as $\overline{CE}$ remains high. Also, on the 23257S, the active level of output enable OE is programmable, thus eliminating bus contention in multiplexed bus microprocessor systems. The NCR 23257 is packaged in a 28 pin DIP with byte-wide alternate pin-out.

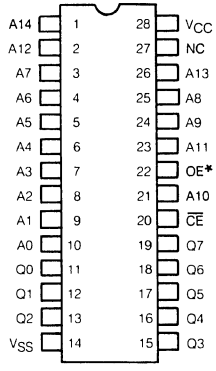
This 256K ROM is also available with a byte wide industry standard JEDEC pin-out where pin 1 = NC and pin 27 = A14. The JEDEC pin-out part is identified as the NCR 23256 and is described in a separate data sheet.

PIN CONFIGURATION

NCR 23257



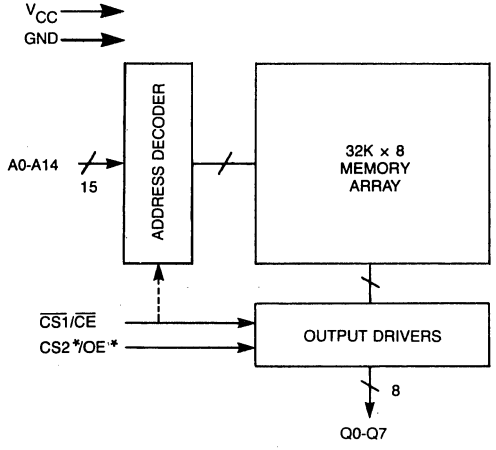
NCR 23257S



*Programmable Active High or Low

NOTE:
23257 Only: Chip Selects $\overline{CS1}$ and CS2 are normally AND'd, but may be internally OR'd at the option of the user.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0 - A_{14}	Address Inputs	OE	Output Enable
Q_0 - Q_7	Data Outputs	$\overline{CE}$	Chip Enable
$\overline{CS1}$, CS2	Chip Selects	V_{CC}	5 Volt ± 10% Power Supply
NC	No Connection		

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NCR

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to ground ..... −0.5 to +7V
Storage temperature ..... −65°C to 150°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operating conditions stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply voltage*	4.5	5.0	5.5	Volts
V_{IH}	Input high level voltage	2.0		V_{CC}	Volts
V_{IL}	Input low level voltage	−0.5		0.8	Volts
T_A	Operating ambient temperature	0		70	°C

* V_{CC} must be applied at least 100 μs before proper device operation is achieved.

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{IN}	Input leakage current	V_{IN} = 0V to V_{CC} max,			10	μA
I_O	Output leakage current	V_O = 0.2 to V_{CC} max, Chip Deselected			±10	μA
V_{OH}	Output high voltage	I_{OH} = −200 μA	2.4			Volts
V_{OL}	Output low voltage	I_{OL} = 3.2mA			0.4	Volts
I_{CC}	Supply current — Active	Outputs Open			95	mA
I_{SB}*	Supply current — Standby	Chip Deselected			10	mA

* Applies to 23257S Power Down Version Only

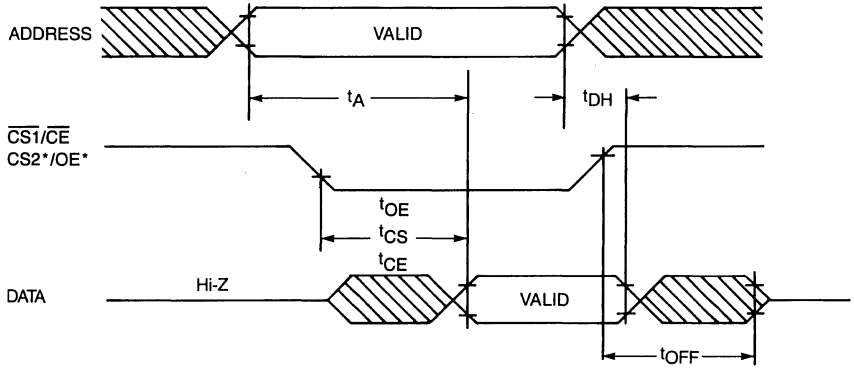
CAPACITANCE, T_A = 25°C, f = 1 MHZ

Symbol	Parameter	Condition	Min	Typ	Max	Units
C_{IN}	Input capacitance	All pins except pin under test are tied to ground			7.0	pF
C_O	Output capacitance				12.5	pF

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	23257-20 23257S-20		23257-25 23257S-25		23257-30 23257S-30		23257-45 23257S-45		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_A	Address Access Time		200		250		300		450	ns
t_{CE}	Chip Enable Access Time		200		250		300		450	ns
t_{CS}	Chip Select Access Time		100		120		150		200	ns
t_{OE}	Output Enable Access Time		100		120		150		200	ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{OFF}	CS Active to Data High Impedance		100		120		150		200	ns

AC WAVEFORMS

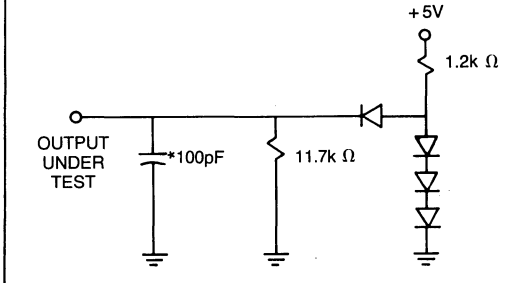


* Programmable Chip Select CS2 and Output Enable OE are assumed to be active low for this example.

AC CONDITION OF TESTS

Input Pulse Levels . . . . . .0.8 Volts to 2.0 Volts
Input Rise and Fall Times . . . . . .10 ns
Output Timing Levels . . . . . .0.8 Volts to 2.0 Volts

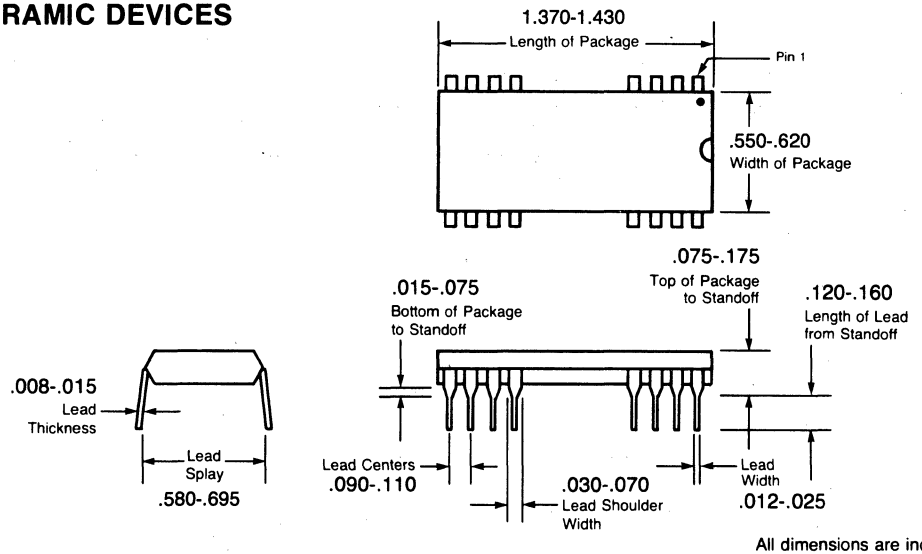
AC TEST LOAD CIRCUIT



* Includes jig capacitance.
All diodes 1N3064 or equivalent.

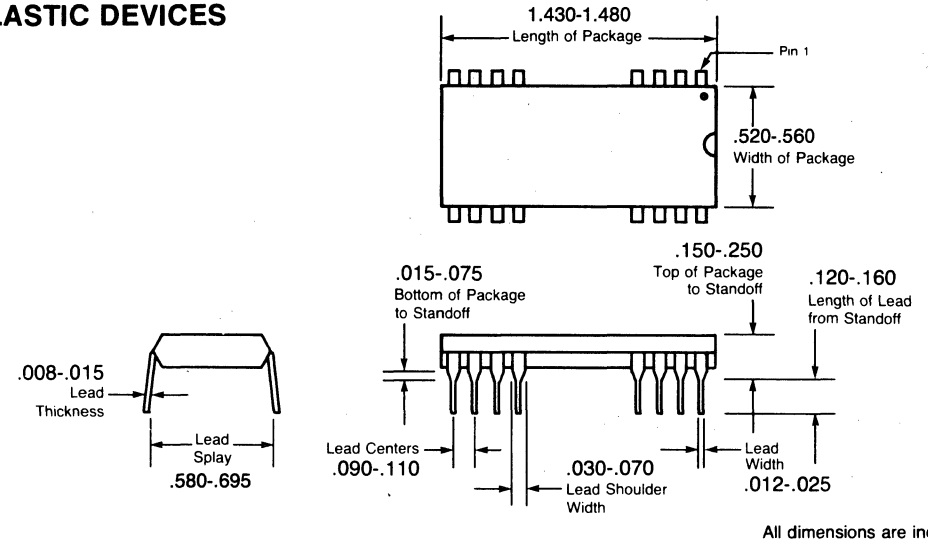
MECHANICAL DATA 28 PIN

CERAMIC DEVICES



All dimensions are inches.

PLASTIC DEVICES



All dimensions are inches.

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513/866-7217 Ohio or International

Chip-On-Board

The NCR Chip-On-Board package is a low cost, versatile packaging system eliminating the need for a dual in-line package in game cartridges and many other applications. With the Chip-On Board (COB) concept, the integrated circuit is bonded directly to a specially designed printed circuit board (PCB). Wire bonding is accomplished by direct connection to the PCB conductors using standard integrated circuit assembly equipment. For protection, the chip and wires are encapsulated with a thoroughly cured electronic grade epoxy coating. Optionally, protection can be provided by a Ryton cap.

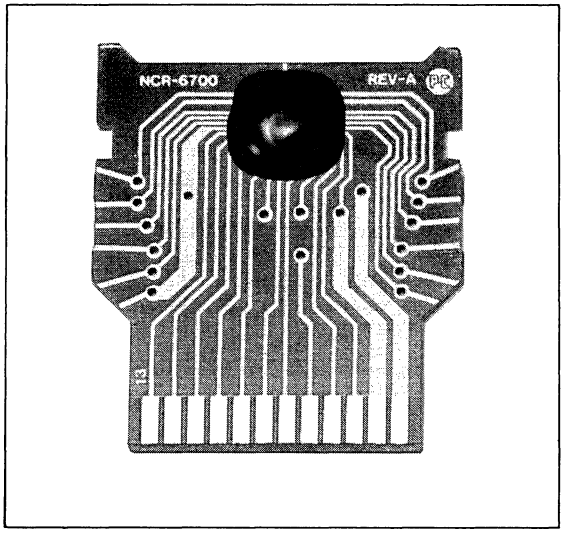
PRODUCT SELECTION GUIDE

BOARD TYPE	NCR ROM PART NO.	ADDRESS ACCESS TIME (ns)	CHIP SELECT ACCESS TIME (ns)	PAGE NUMBER
ATARI® 2600 VCS™ Registered Trademark of Atari, Inc.	2332-45 2364A-45* 23128A-45*	450 450 450	200 200 200	63
ATARI® 5200™ Registered Trademark of Atari, Inc.	2332-30 2364-30 23128-30	300 300 300	150 150 150	65
COLECOVISION® ADAM™ Registered Trademark of Coleco Industries, Inc.	2332-45 2364-45 23128-45	450 450 450	200 200 200	67
COMMODORE 64™ Registered Trademark of Commodore Electronics, Inc.	2332-30 2364-30 23128-30	300 300 300	150 150 150	69
IBM PC JR.™ Registered Trademark of International Business Machines Corp.	2332-25 2364-25 23128-25 23256-25	250 250 250 250	120 120 120 120	71

*Licensed under U.S. Patent #4368515

Chip-On-Board
ATARI® 2600 VCS™

- Cost Effective
- CEM-3 Printed Circuit Board
- Gold Edge Connector Plating
- Encapsulation With Conformal Epoxy Coating Or Optional Protective Cap
- Multiple ROM Densities Available



The NCR Chip-On-Board package is a low cost, versatile packaging system which eliminates the need for a dual in-line package in many integrated circuit applications. With the Chip-On-Board (COB) concept, the integrated circuit is bonded directly to a specially designed printed circuit board (PCB). Wire bonding is accomplished by direct connection to the PCB conductors using standard integrated circuit assembly equipment. For protection, the chip and wires are encapsulated with a thoroughly cured electronic grade epoxy coating. Optionally, protection can be provided by a Ryton cap.

NCR uses standard commercial grade printed circuit board material (CEM-3) for the chip-on-board package. Wafers are manufactured at any one of the three NCR microelectronics facilities, with chip to board assembly coordinated by the Miamisburg, Ohio plant. Final quality assurance testing of the finished COB is controlled by the Miamisburg facility.

ROM PRODUCTS FOR ATARI® 2600 VCS™

NCR P/N	Address Access Time (ns)	Chip Select Access (ns)
2332-45	450	200
2364A-45*	450	200
23128A-45*	450	200

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* Licensed under U.S. Patent Number 4368515

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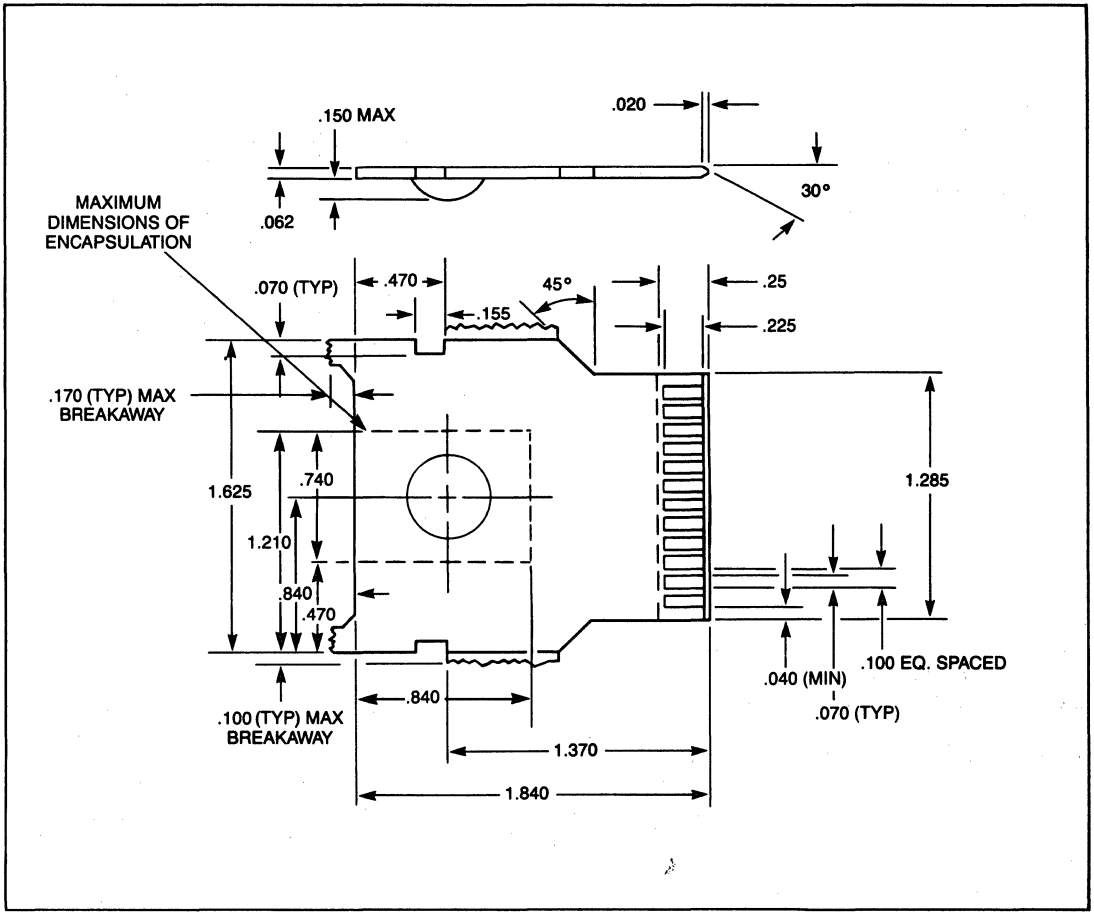

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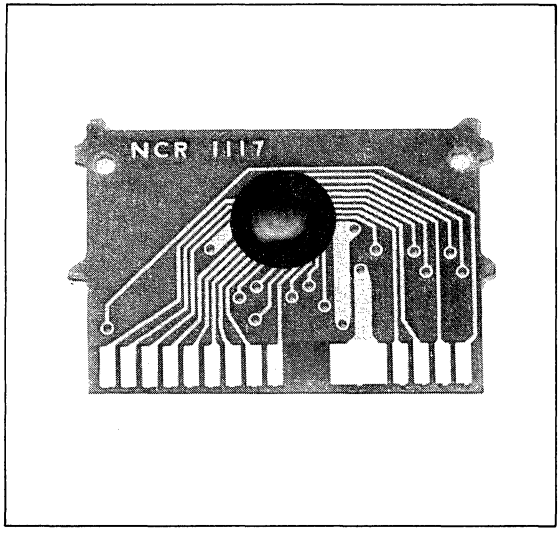
Chip-On-Board
ATARI® 5200™

- **Cost Effective**
- **CEM-3 Printed Circuit Board**
- **Gold Edge Connector Plating**
- **Encapsulation With Conformal Epoxy Coating Or Optional Protective Cap**
- **Multiple ROM Densities Available**



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ROM PRODUCTS FOR ATARI® 5200™

NCR P/N	Address Access Time (ns)	Chip Select Access (ns)
2332-30	300	150
2364-30	300	150
23128-30	300	150

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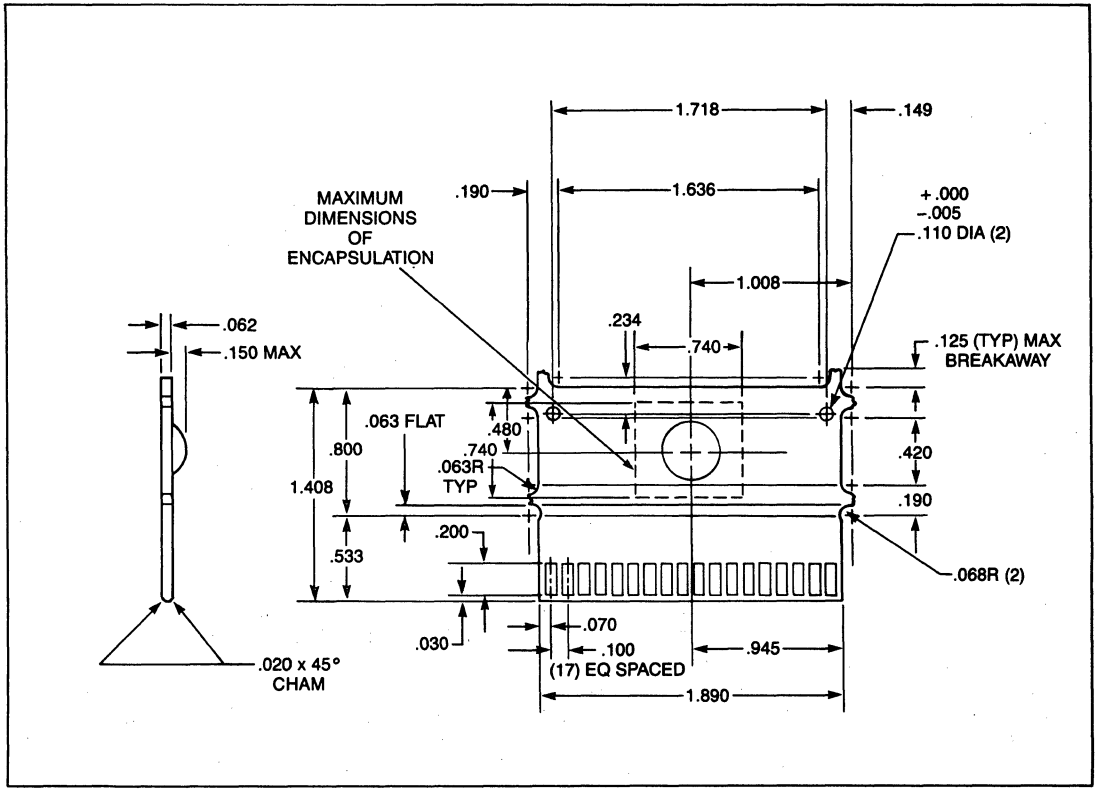

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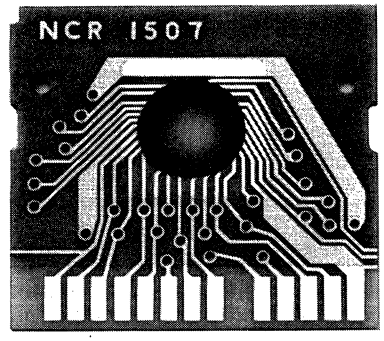
1-513-866-7217 Ohio or International

Chip-On-Board
ColecoVision® (ADAM™)

- **Cost Effective**
- **CEM-3 Printed Circuit Board**
- **Gold Edge Connector Plating**
- **Encapsulation With Conformal Epoxy Coating Or Optional Protective Cap**
- **Multiple ROM Densities Available**



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NCR uses standard commercial grade printed circuit board material (CEM-3) for the chip-on-board package. Wafers are manufactured at any one of the three NCR microelectronics facilities, with chip to board assembly coordinated by the Miamisburg, Ohio plant. Final quality assurance testing of the finished COB is controlled by the Miamisburg facility.

ROM PRODUCTS FOR COLECOVISION® (ADAM™)

NCR P/N	Address Access Time (ns)	Chip Select Access (ns)
2332-45	450	200
2364-45	450	200
23128-45	450	200

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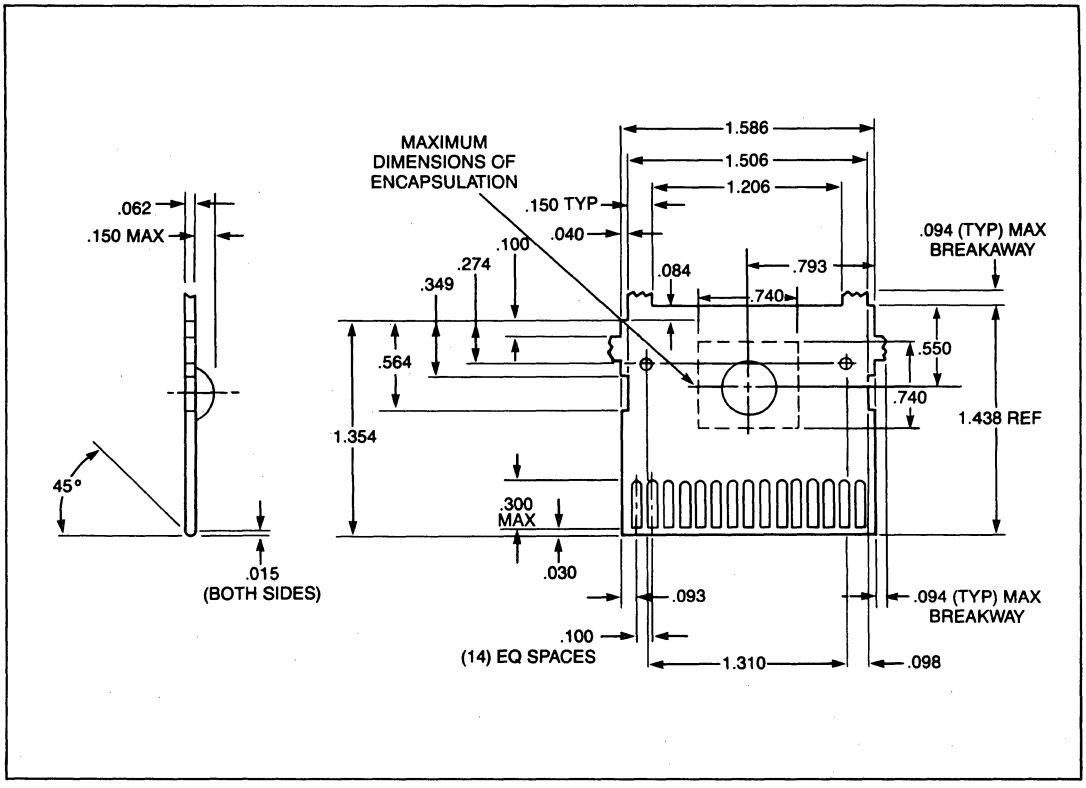
ColecoVision® (Adam™) is a Registered Trademark of Coleco Industries, Inc.



NCR

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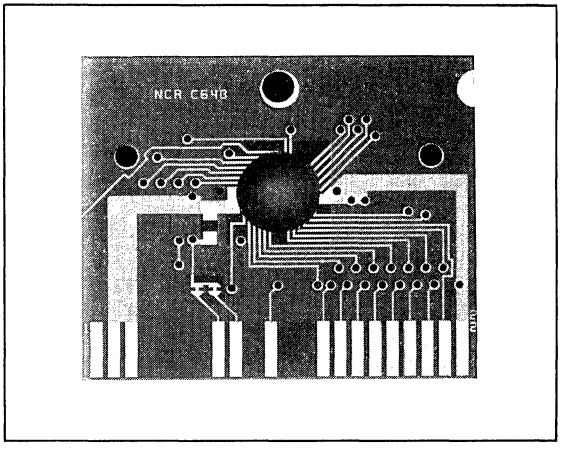
Phone: 1-800-543-5618 outside Ohio
1-513-866-7217 Ohio or International

Chip-On-Board
COMMODORE 64™

- **Cost Effective**
- **CEM-3 Printed Circuit Board**
- **Gold Edge Connector Plating**
- **Encapsulation With Conformal Epoxy Coating Or Optional Protective Cap**
- **Multiple ROM Densities Available**



The NCR Chip-On-Board package is a low cost, versatile packaging system which eliminates the need for a dual in-line package in many integrated circuit applications. With the Chip-On-Board (COB) concept, the integrated circuit is bonded directly to a specially designed printed circuit board (PCB). Wire bonding is accomplished by direct connection to the PCB conductors using standard integrated circuit assembly equipment. For protection, the chip and wires are encapsulated with a thoroughly cured electronic grade epoxy coating. Optionally, protection can be provided by a Ryton cap.

The standard chip-on-board package is normally supplied with $\overline{\text{GAME}}$ and $\overline{\text{EXROM}}$ pins tied to logic "0" (0 volts). However, these pins can be individually programmed to either logic "1" or "0" by simple circuit changes on the PCB.

NCR uses standard commercial grade printed circuit board material (CEM-3) for the chip-on-board package. Wafers are manufactured at any one of the three NCR microelectronics facilities, with chip to board assembly coordinated by the Miamisburg, Ohio plant. Final quality assurance testing of the finished COB is controlled by the Miamisburg facility.

ROM PRODUCTS FOR COMMODORE 64™

NCR P/N	Address Access Time (ns)	Chip Select Access (ns)
2332-30	300	150
2364-30	300	150
23128-30	300	150

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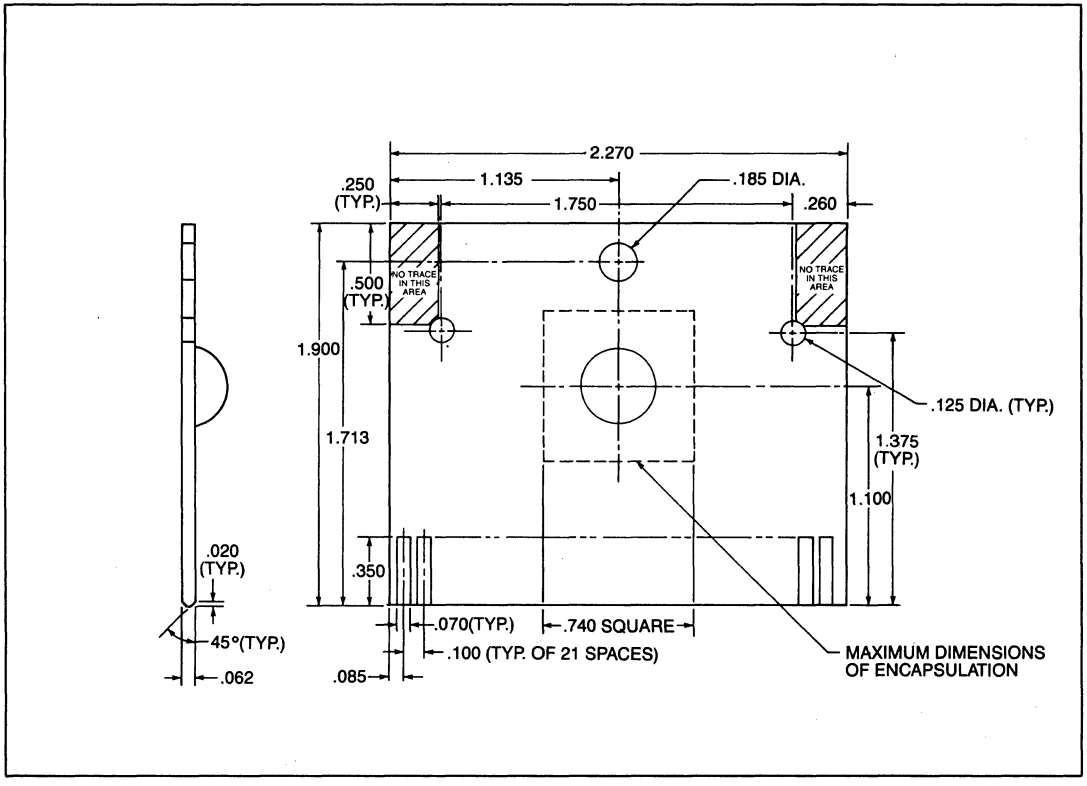

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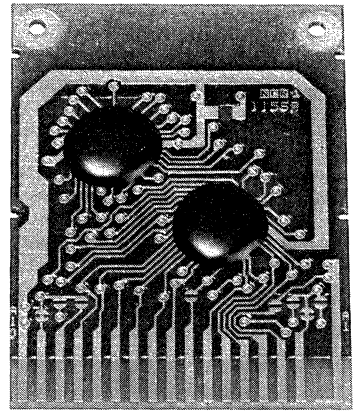
Chip-On-Board
IBM PC JR™

- **Cost Effective**
- **CEM-3 Printed Circuit Board**
- **Gold Edge Connector Plating**
- **Encapsulation With Conformal Epoxy Coating Or Optional Protective Cap**
- **Multiple ROM Densities Available**



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ROM PRODUCTS FOR IBM PC JR™

NCR P/N	Address Access Time (ns)	Chip Select Access (ns)
2332-25	250	120
2364-25	250	120
23128-25	250	120
23256-25	250	120

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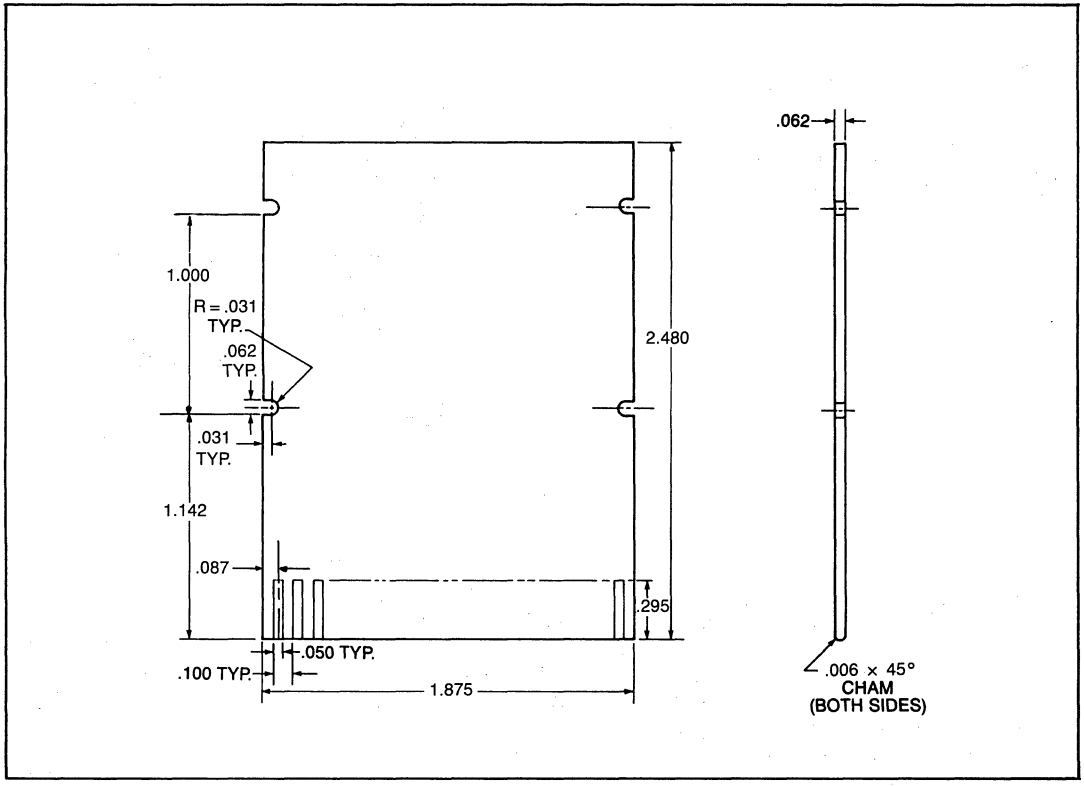

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Non-Volatile RAM

Non-volatile RAM (NVRAM) circuits combine high performance static RAM with electrically erasable PROM on a single integrated circuit. The primary advantage NVRAMs offer the system designer is its ease of interfacing with a microprocessor without affecting system performance. This is possible because an NVRAM looks and performs like a static RAM during normal operation. During a system power failure the entire contents of the static RAM are stored in the EEPROM array and are available for recall when system power returns to normal levels. NCR NVRAMs are offered in commercial, industrial, and military temperature ranges.

PRODUCT SELECTION GUIDE

FUNCTION	PART NUMBER	ORGANIZATION	PAGE NUMBER
256 Bit NVRAM	NCR 52210	64 x 4	75
512 Bit NVRAM	NCR 52211	128 x 4	83
1K NVRAM	NCR 52212	256 x 4	91
1K NVRAM	NCR 52001	128 x 8	99
2K NVRAM	NCR 52002	256 x 8	107
4K NVRAM	NCR 52004	512 x 8	115

CROSS REFERENCE LISTING

NCR PART NUMBER	EQUIVALENT	
NCR 52210	XICOR	X2210
NCR 52211	XICOR	X2211
NCR 52212	XICOR	X2212
NCR 52001	XICOR	X2001
NCR 52002	XICOR	X2002
NCR 52004-28	XICOR	X2004
	INTEL	2004

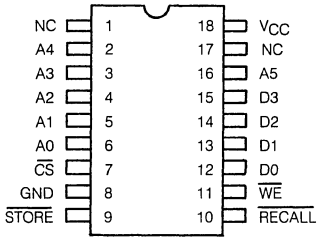
52210
256 BIT (64 x 4) NVRAM

- **256 BIT Static RAM backed by 256 BIT Electrically Erasable PROM**
- **Fully 5V Only Operation**
- **Directly TTL Compatible**
- **In Circuit E²PROM Changes**
- **SRAM Cycle Time less than 300 ns**
- **Power-Failure Protection**
- **Unlimited Recall Cycles**
- **Memory Margining Capability**
- **Operating Ranges**

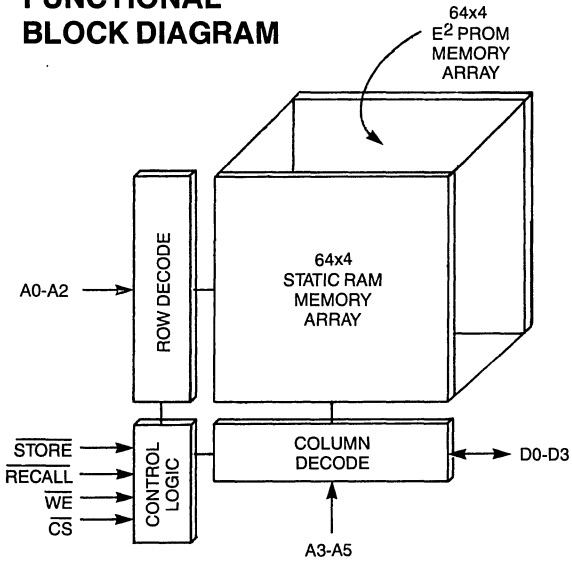
52210	0° C to +70 ° C
52210I	−40° C to +85 ° C
52210HR	−55° C to +125° C

The NCR 52210 non-volatile RAM combines 256 (64x4) bits of conventional static RAM (SRAM) with an identical size array of Electrically Erasable PROM (E²PROM). Non-volatile data can be stored in the E²PROM while independent data is accessed simultaneously in the SRAM. Data can be transferred back and forth between the SRAM and E²PROM by simple Store and Recall operations. A Store signal transfers data from the SRAM to the non-volatile E²PROM where it is safely stored even when power is removed. The data stored in the non-volatile E²PROM can be recalled an unlimited number of times. The 52210 requires only a single 5 volt power supply for all modes of operation. The device is completely TTL compatible with fully static timing and three-state outputs. The NCR 52210 is available in an 18 pin package in commercial, industrial, and high reliability versions.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A0-A5	Address Inputs
D0-D3	Data I/O
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{STORE}$	Store Operation
$\overline{RECALL}$	Array Recall Operation
V_{CC}	5V ± 10% Supply Voltage

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DEVICE OPERATION

SRAM READ/WRITE

The NCR 52210 can be read like a conventional static RAM. With $\overline{CS}$ low and $\overline{WE}$ high, valid data will be presented to the output pins. With $\overline{CS}$ low and $\overline{WE}$ low, the SRAM can be written to like a conventional static RAM.

STORE*

Transferring data from the SRAM to the non-volatile E^2PROM is controlled by the Store operation. When $\overline{STORE}$ is brought low, the entire contents of the SRAM array are copied into the non-volatile E^2PROM array. The data in the SRAM array is unaffected by a Store operation. The $\overline{RECALL}$ line is inhibited by a Store operation, and $\overline{CS}$ can either be high or low.

The I/O terminals are in the high impedance state during a Store operation. The contents of the E^2PROM remain valid with or without power being supplied. The data retention time of the E^2PROM can be measured by memory margining.

During power up or power down, precaution must be taken to prevent an unintentional Store cycle. Holding $\overline{STORE}$ high or $\overline{RECALL}$ low will inhibit the initiation of a Store cycle.

RECALL*

The data stored in the non-volatile E^2PROM array is transferred back into SRAM by the Recall operation. When $\overline{RECALL}$ is brought low, the entire contents of the E^2PROM are copied back into the SRAM array (overwriting any data already existing in the SRAM). The data in the E^2PROM is unaffected by a Recall operation. The I/O terminals are in a high impedance state during a Recall operation. The $\overline{STORE}$ line is inhibited by a Recall operation and $\overline{CS}$ can either be high or low. To ensure a Recall cycle is initiated on power up, a $\overline{RECALL}$ signal should be applied until VCC reaches specification limits.

MEMORY MARGINING

The NCR 52210 supports margining of the memory transistors. Memory margining allows device retention time to be projected for the purpose of device evaluation. An application note describing the memory margining algorithm is available.

MODE SELECTION

MODE	INPUTS			
	$\overline{CS}$	$\overline{WE}$	$\overline{STORE}$	$\overline{RECALL}$
READ	L	H	H	H
WRITE	L	L	H	H
STORE	X	X	L	H
RECALL	X	X	H	L

* To ensure a valid Store or Recall cycle, do not apply $\overline{STORE}$ and $\overline{RECALL}$ at the same time.

ABSOLUTE MAXIMUM RATINGS

All inputs or outputs relative to ground . . . . . −0.5 to +7V

Storage temperature without data retention . . . . . −65°C to +150°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operational limits stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	52210			52210I			52210HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage	4.5		5.5	4.5		5.5	4.5		5.5	V
V_{IH}	Input high level voltage	2.0		V_{CC}	2.0		V_{CC}	2.0		V_{CC}	V
V_{IL}	Input low level voltage	−0.3		0.8	−0.3		0.8	−0.3		0.8	V
T_A	Ambient Temperature	0		70	−40		85	−55		125	°C

All voltages are with respect to ground

STATIC ELECTRICAL CHARACTERISTICS, OVER RECOMMENDED OPERATION CONDITIONS (UNLESS OTHERWISE NOTED)

Symbol	Parameter	Condition	52210			52210I			52210HR**			Unit
			Min	Typ*	Max	Min	Typ*	Max	Min	Typ*	Max	
I_{IN}	Input leakage current	V_{IN} = 0V to +5.5V		0.1	10		0.1	10		0.1	10	μA
I_O	I/O leakage current	V_O = 0.4V to 5.5V Chip Deselected		0.1	10		0.1	10		0.1	10	μA
I_{CC}	Supply Current	Outputs Open		30	50		30	50		30	60	mA
V_{OH}	Output high voltage	I_{OH} = −400μA	2.4			2.4			2.4			V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA			0.4			0.4			0.4	V
T_S	Non-Volatile storage time		1.0									yr

*Typical values are at 25°C and nominal supply voltages.

CAPACITANCE T_A = 25°C, f = 1.0MHz, V_{CC} = 5V

Symbol	Parameter	Condition	52210			52210I			52210HR**			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
C	Capacitance of Input & Data I/O pins	All pins at VSS (ground)			10			10			10	pF

*,**The 52210 HR data is preliminary and is subject to change.

NCR

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

READ CYCLE

Symbol	Parameter	52210			52210I			52210HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RC}	Read Cycle Time	300			300			450			ns
t_{ACC}	Address Access Time			300			300			450	ns
t_{A}	Chip Select To Data Active	0			0			0			ns
t_{CS}	Chip Select Access Time			100			120			120	ns
t_{OH}	Output Hold Time	10			10			10			ns
t_{OZ}	Chip Select Output High Impedance Time			90			90			90	ns

WRITE CYCLE

Symbol	Parameter	52210			52210I			52210HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{WC}	Write Cycle Time	300			300			450			ns
t_{CW}	Chip Select to End of Write	150			150			300			ns
t_{WP}	Write Pulse Width	150			150			300			ns
t_{WR}	Write Release Time	25			25			25			ns
t_{DTW}	Output High Impedence From Write Enable			100			100			100	ns
t_{DW}	Data to Write Time Overlap	150			150			200			ns
t_{OW}	Output Active from End of Write	10			10			10			ns
t_{DH}	Data Hold From Write Time	20			20			20			ns
t_{AS}	Address Setup	50			50			50			ns

STORE CYCLE

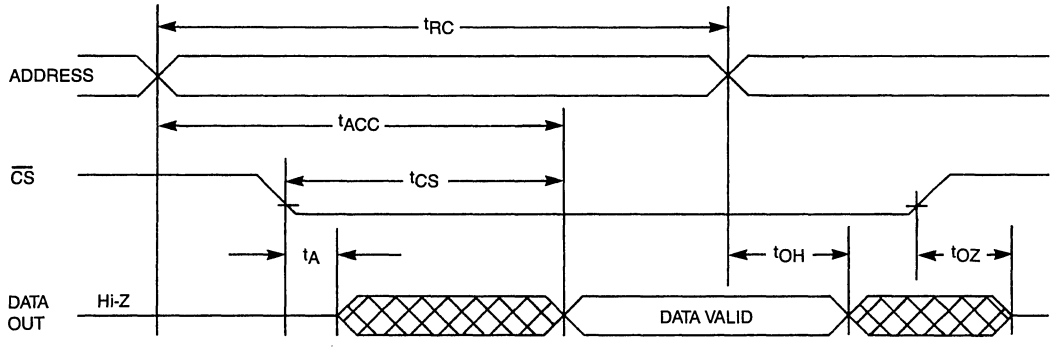
Symbol	Parameter	52210			52210I			52210HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{STC}	Store Cycle Time			10			10			10	ms
t_{STP}	Store Pulse Width	100			100			100			ns
t_{STZ}	Store to Output Hi-Z			100			100			100	ns
N_{SC}	Number of Store Cycles	10^4			10^4			10^4			

RECALL CYCLE

Symbol	Parameter	52210			52210I			52210HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RCC}	Array Recall Cycle Time		30	70			260			360	μs
t_{RCP}	Recall Pulse Width	200			200			450			ns
t_{RCZ}	Recall to Output Hi-Z			100			100			100	ns

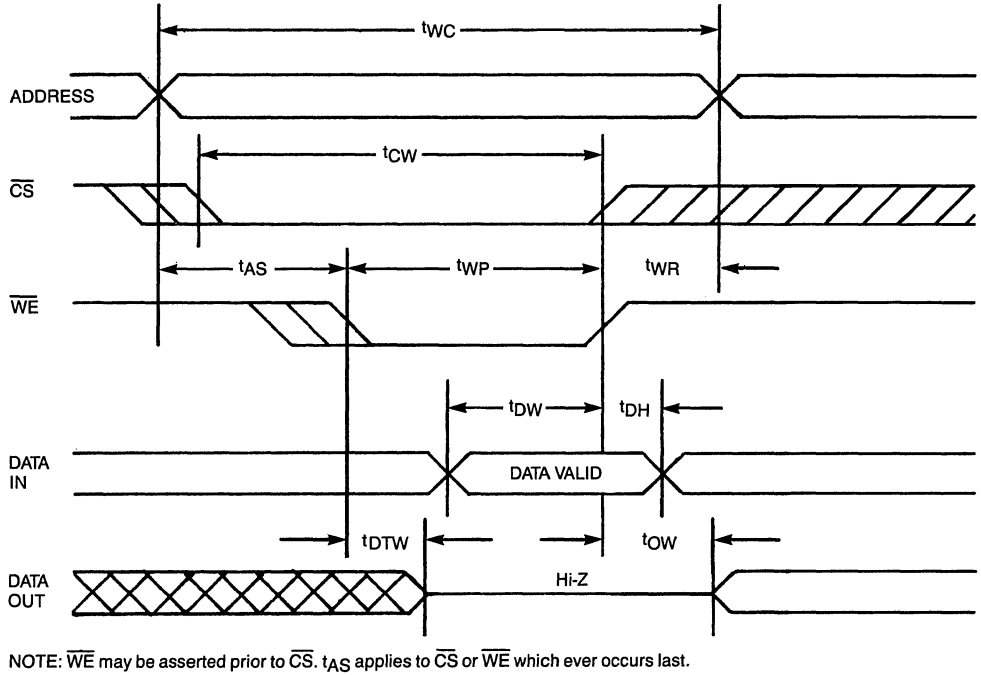
**The 52210 HR data is preliminary and is subject to change.

READ CYCLE



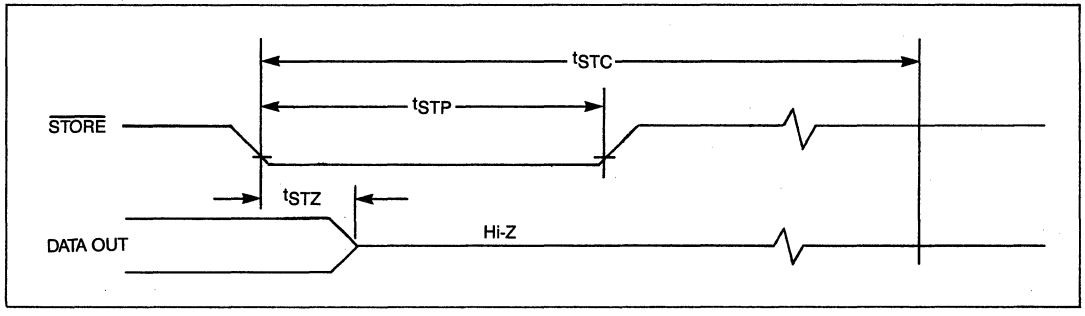
NOTE: During a read operation $\overline{WE}$ should be held at V_{IH}

WRITE CYCLE

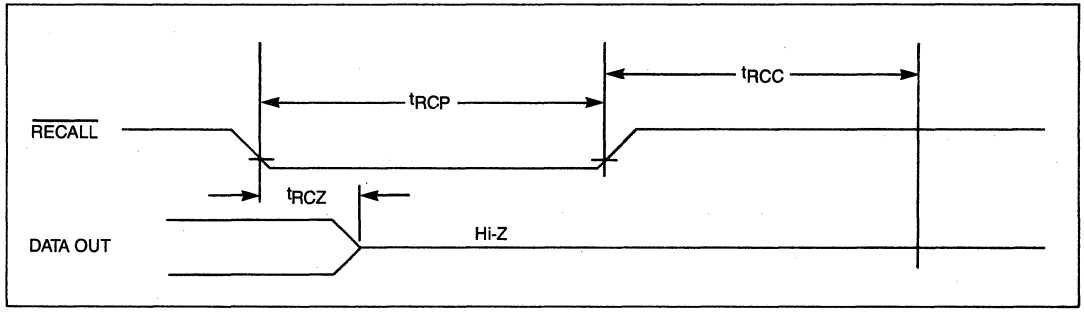


NOTE: $\overline{WE}$ may be asserted prior to $\overline{CS}$. t_{AS} applies to $\overline{CS}$ or $\overline{WE}$ which ever occurs last.

STORE CYCLE



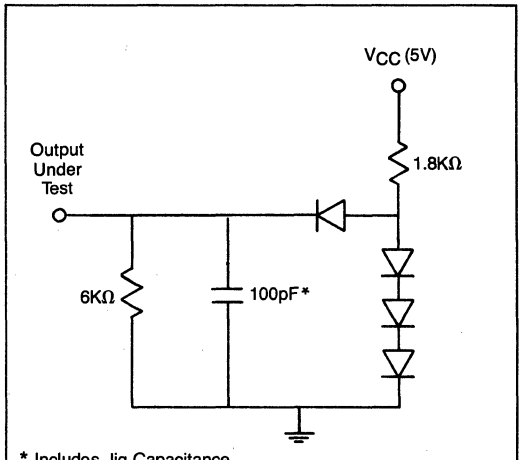
RECALL CYCLE



A. C. CONDITION OF TESTS

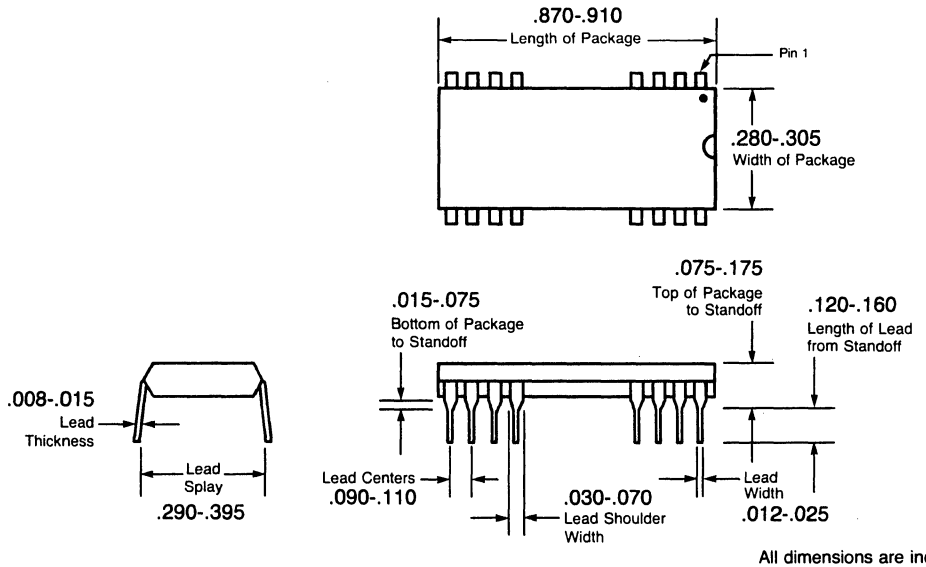
Input Pulse Levels . . . . . 0.8 Volts to 2.0 Volts
Inputs Rise & Fall Times. . . . . 10 ns
Output Timing Levels . . . . . 0.8 Volts to 2.0 Volts

TEST LOAD CIRCUIT



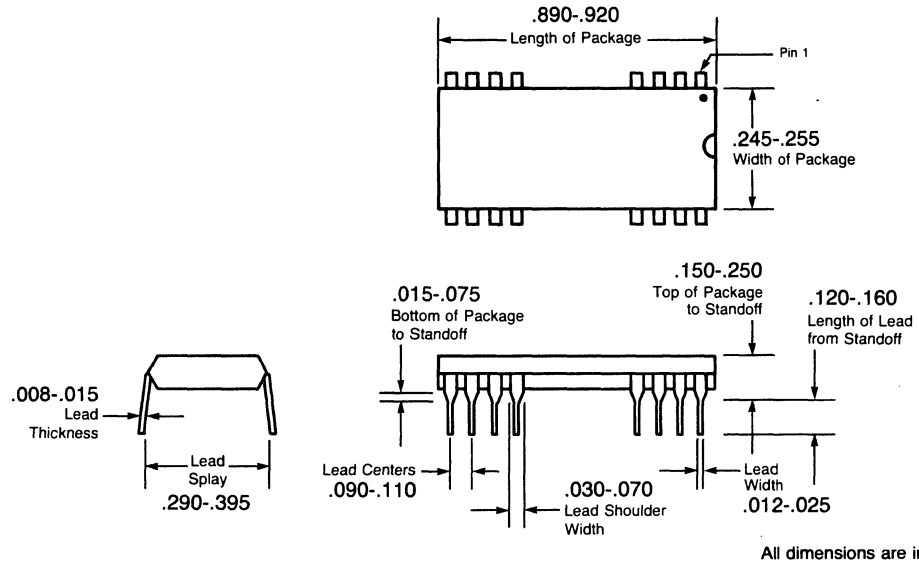
MECHANICAL DATA 18 PIN

CERAMIC DEVICES



All dimensions are inches.

PLASTIC DEVICES



All dimensions are inches.

NCR

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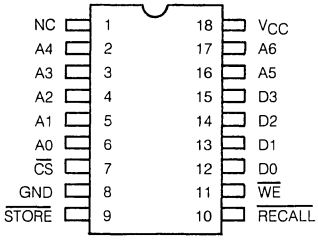
52211
512 BIT (128 x 4) NVRAM

- **512 BIT Static RAM backed by 512 BIT Electrically Erasable PROM**
- **Fully 5V Only Operation**
- **Directly TTL Compatible**
- **In Circuit E²PROM Changes**
- **SRAM Cycle Time less than 300 ns**
- **Power-Failure Protection**
- **Unlimited Recall Cycles**
- **Memory Margining Capability**
- **Operating Ranges**

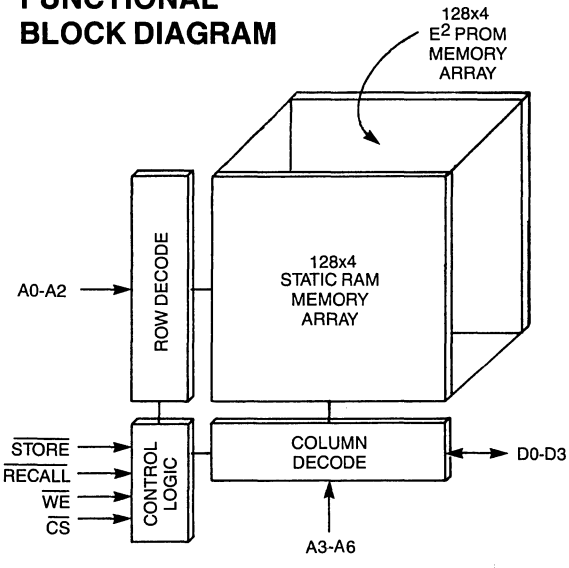
52211	0° C to +70° C
52211 I	−40° C to +85° C
52211 HR	−55° C to +125° C

The NCR 52211 non-volatile RAM combines 512 (128x4) bits of conventional static RAM (SRAM) with an identical size array of Electrically Erasable PROM (E²PROM). Non-volatile data can be stored in the E²PROM while independent data is accessed simultaneously in the SRAM. Data can be transferred back and forth between the SRAM and E²PROM by simple Store and Recall operations. A Store signal transfers data from the SRAM to the non-volatile E²PROM where it is safely stored even when power is removed. The data stored in the non-volatile E²PROM can be recalled an unlimited number of times. The 52211 requires only a single 5 volt power supply for all modes of operation. The device is completely TTL compatible with fully static timing and three-state outputs. The NCR 52211 is available in an 18 pin package in commercial, industrial, and high reliability versions.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A0-A6	Address Inputs
D0-D3	Data I/O
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{STORE}$	Store Operation
$\overline{RECALL}$	Array Recall Operation
V_{CC}	5V ± 10% Supply Voltage

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DEVICE OPERATION

SRAM READ/WRITE

The NCR 52211 can be read like a conventional static RAM. With $\overline{CS}$ low and $\overline{WE}$ high, valid data will be presented to the output pins. With $\overline{CS}$ low and $\overline{WE}$ low, the SRAM can be written to like a conventional static RAM.

STORE*

Transferring data from the SRAM to the non-volatile E^2PROM is controlled by the Store operation. When $\overline{STORE}$ is brought low, the entire contents of the SRAM array are copied into the non-volatile E^2PROM array. The data in the SRAM array is unaffected by a Store operation. The $\overline{RECALL}$ line is inhibited by a Store operation, and $\overline{CS}$ can either be high or low.

The I/O terminals are in the high impedance state during a Store operation. The contents of the E^2PROM remain valid with or without power being supplied. The data retention time of the E^2PROM can be measured by memory margining.

During power up or power down, precaution must be taken to prevent an unintentional Store cycle. Holding $\overline{STORE}$ high or $\overline{RECALL}$ low will inhibit the initiation of a Store cycle.

RECALL*

The data stored in the non-volatile E^2PROM array is transferred back into SRAM by the Recall operation. When $\overline{RECALL}$ is brought low, the entire contents of the E^2PROM are copied back into the SRAM array (overwriting any data already existing in the SRAM). The data in the E^2PROM is unaffected by a Recall operation. The I/O terminals are in a high impedance state during a Recall operation. The $\overline{STORE}$ line is inhibited by a Recall operation and $\overline{CS}$ can either be high or low. To ensure a Recall cycle is initiated on power up, a $\overline{RECALL}$ signal should be applied until VCC reaches specification limits.

MEMORY MARGINING

The NCR 52211 supports margining of the memory transistors. Memory margining allows device retention time to be projected for the purpose of device evaluation. An application note describing the memory margining algorithm is available.

MODE SELECTION

MODE	INPUTS			
	$\overline{CS}$	$\overline{WE}$	$\overline{STORE}$	$\overline{RECALL}$
READ	L	H	H	H
WRITE	L	L	H	H
STORE	X	X	L	H
RECALL	X	X	H	L

* To ensure a valid Store or Recall cycle, do not apply $\overline{STORE}$ and $\overline{RECALL}$ at the same time.

ABSOLUTE MAXIMUM RATINGS

All inputs or outputs relative to ground . . . . . −0.5 to +7V

Storage temperature without data retention . . . . . −65°C to +150°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operational limits stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	52211			52211I			52211HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage	4.5		5.5	4.5		5.5	4.5		5.5	V
V_{IH}	Input high level voltage	2.0		V_{CC}	2.0		V_{CC}	2.0		V_{CC}	V
V_{IL}	Input low level voltage	−0.3		0.8	−0.3		0.8	−0.3		0.8	V
T_A	Ambient Temperature	0		70	−40		85	−55		125	°C

All voltages are with respect to ground

STATIC ELECTRICAL CHARACTERISTICS, OVER RECOMMENDED OPERATION CONDITIONS (UNLESS OTHERWISE NOTED)

Symbol	Parameter	Condition	52211			52211I			52211HR**			Unit
			Min	Typ*	Max	Min	Typ*	Max	Min	Typ*	Max	
I_{IN}	Input leakage current	V_{IN} = 0V to +5.5V		0.1	10		0.1	10		0.1	10	μA
I_O	I/O leakage current	V_O = 0.4V to 5.5V Chip Deselected		0.1	10		0.1	10		0.1	10	μA
I_{CC}	Supply Current	Outputs Open		30	50		30	50		30	60	mA
V_{OH}	Output high voltage	I_{OH} = −400μA	2.4			2.4			2.4			V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA			0.4			0.4			0.4	V
T_S	Non-Volatile storage time		1.0									yr

*Typical values are at 25°C and nominal supply voltages.

CAPACITANCE T_A = 25°C, f = 1.0MHz, V_{CC} = 5V

Symbol	Parameter	Condition	52211			52211I			52211HR**			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
C	Capacitance of Input & Data I/O pins	All pins at VSS (ground)			10			10			10	pF

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

READ CYCLE

Symbol	Parameter	52211			52211I			52211HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RC}	Read Cycle Time	300			300			450			ns
t_{ACC}	Address Access Time			300			300			450	ns
t_{A}	Chip Select To Data Active	0			0			0			ns
t_{CS}	Chip Select Access Time			100			120			120	ns
t_{OH}	Output Hold Time	10			10			10			ns
t_{OZ}	Chip Select Output High Impedance Time			100			90			90	ns

WRITE CYCLE

Symbol	Parameter	52211			52211I			52211HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{WC}	Write Cycle Time	300			300			450			ns
t_{CW}	Chip Select to End of Write	150			150			300			ns
t_{WP}	Write Pulse Width	150			150			300			ns
t_{WR}	Write Release Time	25			25			25			ns
t_{DTW}	Output High Impedence From Write Enable			100			100			100	ns
t_{DW}	Data to Write Time Overlap	150			150			200			ns
t_{OW}	Output Active from End of Write	10			10			10			ns
t_{DH}	Data Hold From Write Time	20			20			20			ns
t_{AS}	Address Setup	50			50			50			ns

STORE CYCLE

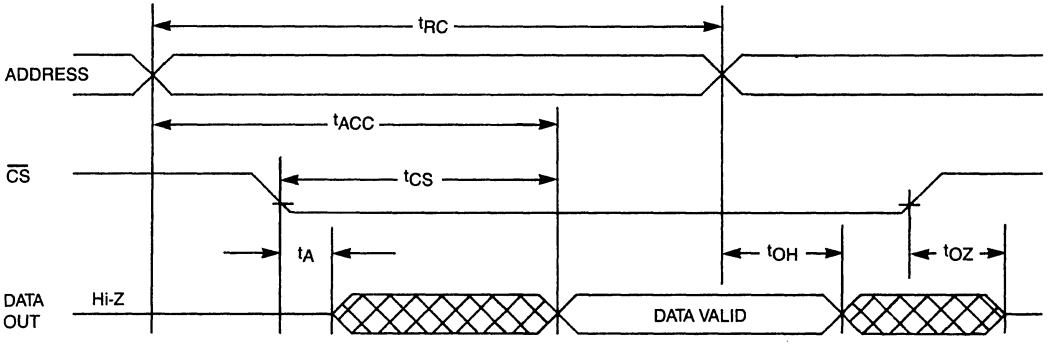
Symbol	Parameter	52211			52211I			52211HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{STC}	Store Cycle Time			10			10			10	ms
t_{STP}	Store Pulse Width	100			100			100			ns
t_{STZ}	Store to Output Hi-Z			100			100			100	ns
N_{SC}	Number of Store Cycles	10^4			10^4			10^4			

RECALL CYCLE

Symbol	Parameter	52211			52211I			52211HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RCC}	Array Recall Cycle Time		30	70			260			360	μs
t_{RCP}	Recall Pulse Width	200			200			450			ns
t_{RCZ}	Recall to Output Hi-Z			100			100			100	ns

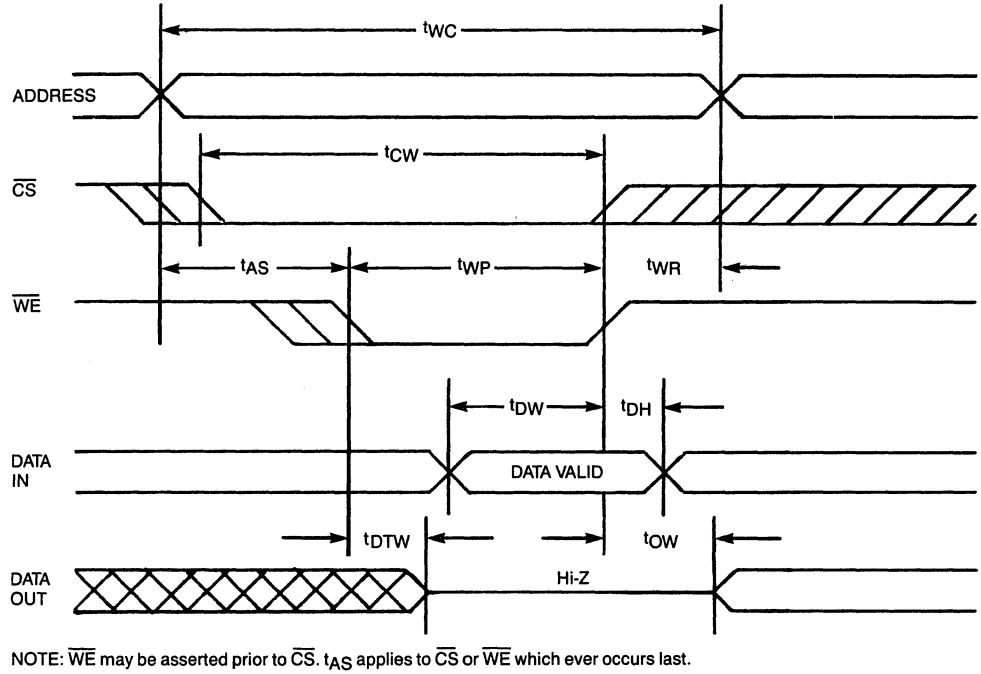
**The 52211 HR data is preliminary and is subject to change.

READ CYCLE



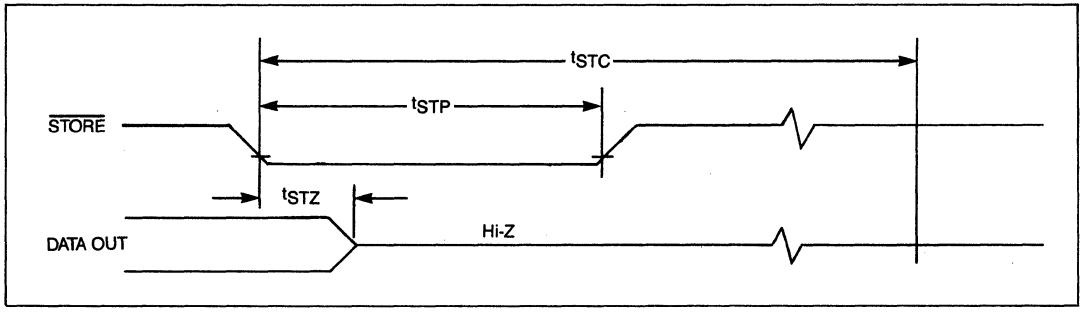
NOTE: During a read operation $\overline{WE}$ should be held at V_{IH}

WRITE CYCLE

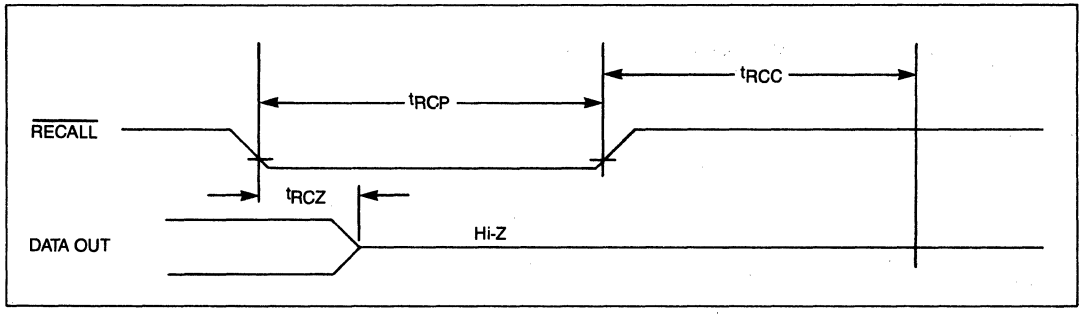


NOTE: $\overline{WE}$ may be asserted prior to $\overline{CS}$. t_{AS} applies to $\overline{CS}$ or $\overline{WE}$ which ever occurs last.

STORE CYCLE



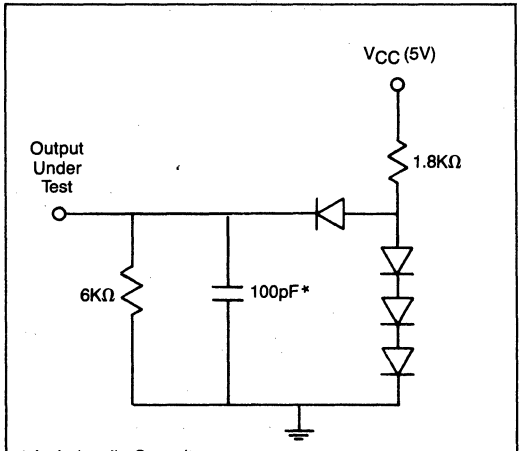
RECALL CYCLE



A. C. CONDITION OF TESTS

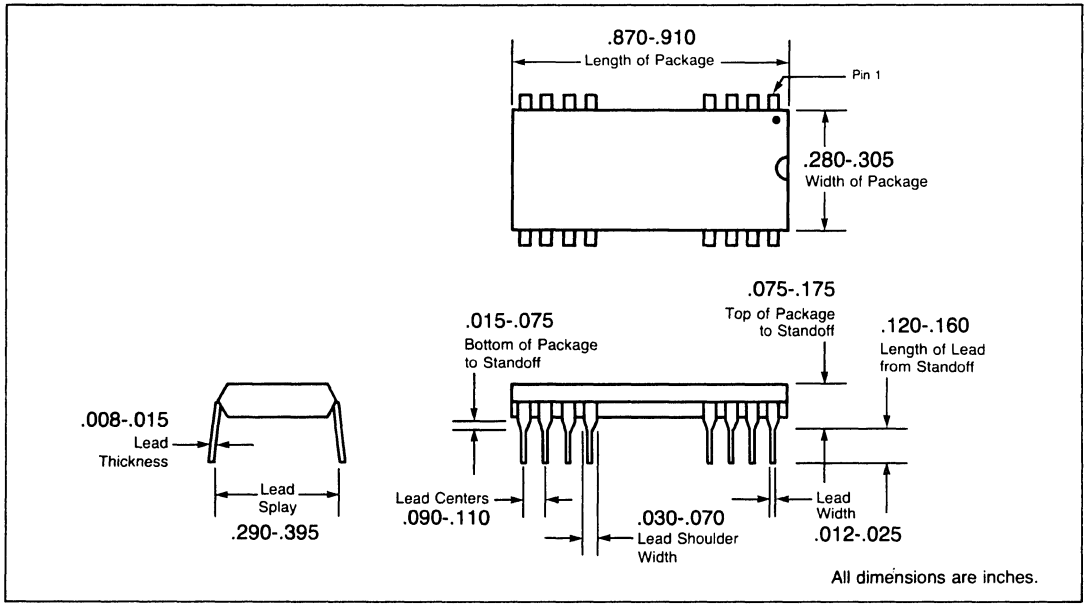
Input Pulse Levels . . . . . 0.8 Volts to 2.0 Volts
Inputs Rise & Fall Times. . . . . 10 ns
Output Timing Levels . . . . . 0.8 Volts to 2.0 Volts

TEST LOAD CIRCUIT

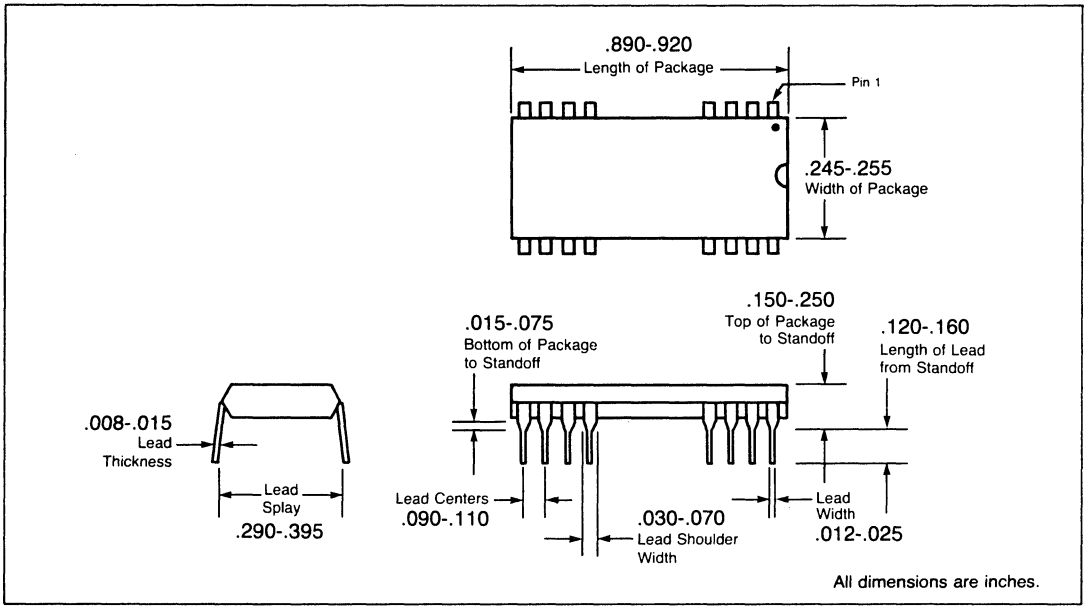


MECHANICAL DATA 18 PIN

CERAMIC DEVICES



PLASTIC DEVICES



NCR

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513/866-7217 Ohio or International

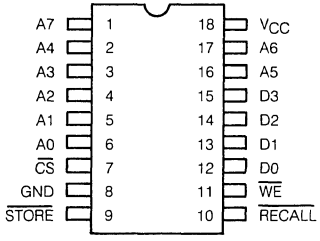
52212
1K BIT (256 x 4) NVRAM

- **1K Bit Static RAM backed by 1K Bit Electrically Erasable PROM**
- **Fully 5V Only Operation**
- **Directly TTL Compatible**
- **In Circuit E^2PROM Changes**
- **SRAM Cycle Time less than 300 ns**
- **Power-Failure Protection**
- **Unlimited Recall Cycles**
- **Memory Margining Capability**
- **Operating Ranges**

52212	0°C to +70°C
52212 I	–40°C to +85°C
52212 HR	–55°C to +125°C

The NCR 52212 non-volatile RAM combines 1K(256x4) bits of conventional static RAM (SRAM) with an identical size array of Electrically Erasable PROM (E^2PROM). Non-volatile data can be stored in the E^2 PROM while independent data is accessed simultaneously in the SRAM. Data can be transferred back and forth between the SRAM and E^2PROM by simple Store and Recall operations. A Store signal transfers data from the SRAM to the non-volatile E^2PROM where it is safely stored even when power is removed. The data stored in the non-volatile E^2PROM can be recalled an unlimited number of times. The 52212 requires only a single 5 volt power supply for all modes of operation. The device is completely TTL compatible with fully static timing and three-state outputs. The NCR 52212 is available in an 18 pin package in commercial, industrial, and high reliability versions.

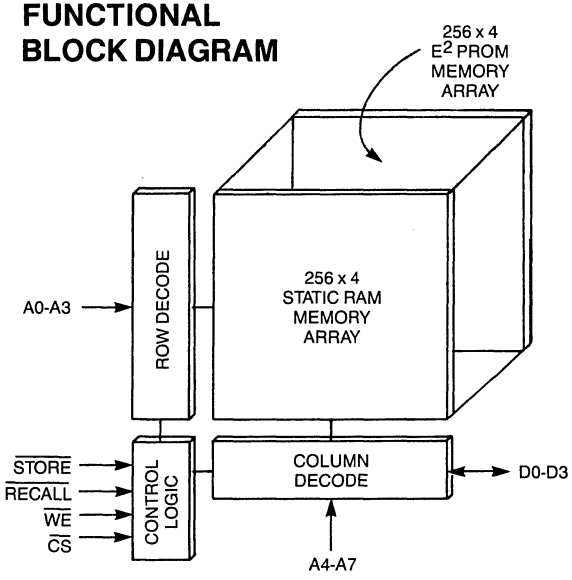
PIN CONFIGURATION



PIN NAMES

A0-A7	Address Inputs
D0-D3	Data I/O
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{STORE}$	Store Operation
$\overline{RECALL}$	Array Recall Operation
V_{CC}	5V ± 10% Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



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DEVICE OPERATION

SRAM READ/WRITE

The NCR 52212 can be read like a conventional static RAM. With $\overline{CS}$ low and $\overline{WE}$ high, valid data will be presented to the output pins. With $\overline{CS}$ low and $\overline{WE}$ low, the SRAM can be written to like a conventional static RAM.

STORE*

Transferring data from the SRAM to the non-volatile E^2PROM is controlled by the Store operation. When $\overline{STORE}$ is brought low, the entire contents of the SRAM array are copied into the non-volatile E^2PROM array. The data in the SRAM array is unaffected by a Store operation. The $\overline{RECALL}$ line is inhibited by a Store operation, and $\overline{CS}$ can either be high or low.

The I/O terminals are in the high impedance state during a Store operation. The contents of the E^2PROM remain valid with or without power being supplied. The data retention time of the E^2PROM can be measured by memory margining.

During power up or power down, precaution must be taken to prevent an unintentional Store cycle. Holding $\overline{STORE}$ high or $\overline{RECALL}$ low will inhibit the initiation of a Store cycle.

RECALL*

The data stored in the non-volatile E^2PROM array is transferred back into SRAM by the Recall operation. When $\overline{RECALL}$ is brought low, the entire contents of the E^2PROM are copied back into the SRAM array (overwriting any data already existing in the SRAM). The data in the E^2PROM is unaffected by a Recall operation. The I/O terminals are in a high impedance state during a Recall operation. The $\overline{STORE}$ line is inhibited by a Recall operation and $\overline{CS}$ can either be high or low. To ensure a Recall cycle is initiated on power up, a $\overline{RECALL}$ signal should be applied until VCC reaches specification limits.

MEMORY MARGINING

The NCR 52212 supports margining of the memory transistors. Memory margining allows device retention time to be projected for the purpose of device evaluation. An application note describing the memory margining algorithm is available.

MODE SELECTION

MODE	INPUTS			
	$\overline{CS}$	$\overline{WE}$	$\overline{STORE}$	$\overline{RECALL}$
READ	L	H	H	H
WRITE	L	L	H	H
STORE	X	X	L	H
RECALL	X	X	H	L

* To ensure a valid Store or Recall cycle, do not apply $\overline{STORE}$ and $\overline{RECALL}$ at the same time.

ABSOLUTE MAXIMUM RATINGS

All inputs or outputs relative to ground . . . . . – 0.5 to + 7V

Storage temperature without data retention . . . . . – 65°C to + 150°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operational limits stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	52212			52212I			52212HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage	4.5		5.5	4.5		5.5	4.5		5.5	V
V_{IH}	Input high level voltage	2.0		V_{CC}	2.0		V_{CC}	2.0		V_{CC}	V
V_{IL}	Input low level voltage	– 0.3		0.8	– 0.3		0.8	– 0.3		0.8	V
T_A	Ambient Temperature	0		70	– 40		85	– 55		125	°C

All voltages are with respect to ground

STATIC ELECTRICAL CHARACTERISTICS, OVER RECOMMENDED OPERATION CONDITIONS (UNLESS OTHERWISE NOTED)

Symbol	Parameter	Condition	52212			52212I			52212HR**			Unit
			Min	Typ*	Max	Min	Typ*	Max	Min	Typ*	Max	
I_{IN}	Input leakage current	V_{IN} = 0V to + 5.5V		0.1	10		0.1	10		0.1	10	μA
I_O	I/O leakage current	V_O = 0.4V to 5.5V Chip Deselected		0.1	10		0.1	10		0.1	10	μA
I_{CC}	Supply Current	Outputs Open		30	50		30	50		30	60	mA
V_{OH}	Output high voltage	I_{OH} = – 400μA	2.4			2.4			2.4			V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA			0.4			0.4			0.4	V
T_S	Non-Volatile storage time		1.0									yr

* Typical values are at 25°C and nominal supply voltages.

CAPACITANCE T_A = 25°C, f = 1.0MHz, V_{CC} = 5V

Symbol	Parameter	Condition	52212			52212I			52212HR**			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
C	Capacitance of Input & Data I/O pins	All pins at VSS (ground)			10			10			10	pF

**The 52212 HR data is preliminary and is subject to change.

NCR

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

READ CYCLE

Symbol	Parameter	52212			52212I			52212HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RC}	Read Cycle Time	300			300			450			ns
t_{ACC}	Address Access Time			300			300			450	ns
t_{A}	Chip Select To Data Active	0			0			0			ns
t_{CS}	Chip Select Access Time			100			120			120	ns
t_{OH}	Output Hold Time	10			10			10			ns
t_{OZ}	Chip Select Output High Impedance Time			90			90			90	ns

WRITE CYCLE

Symbol	Parameter	52212			52212I			52212HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{WC}	Write Cycle Time	300			300			450			ns
t_{CW}	Chip Select to End of Write	150			150			300			ns
t_{WP}	Write Pulse Width	150			150			300			ns
t_{WR}	Write Release Time	25			25			25			ns
t_{DTW}	Output High Impedence From Write Enable			100			100			100	ns
t_{DW}	Data to Write Time Overlap	150			150			200			ns
t_{OW}	Output Active from End of Write	10			10			10			ns
t_{DH}	Data Hold From Write Time	20			20			20			ns
t_{AS}	Address Setup	50			50			50			ns

STORE CYCLE

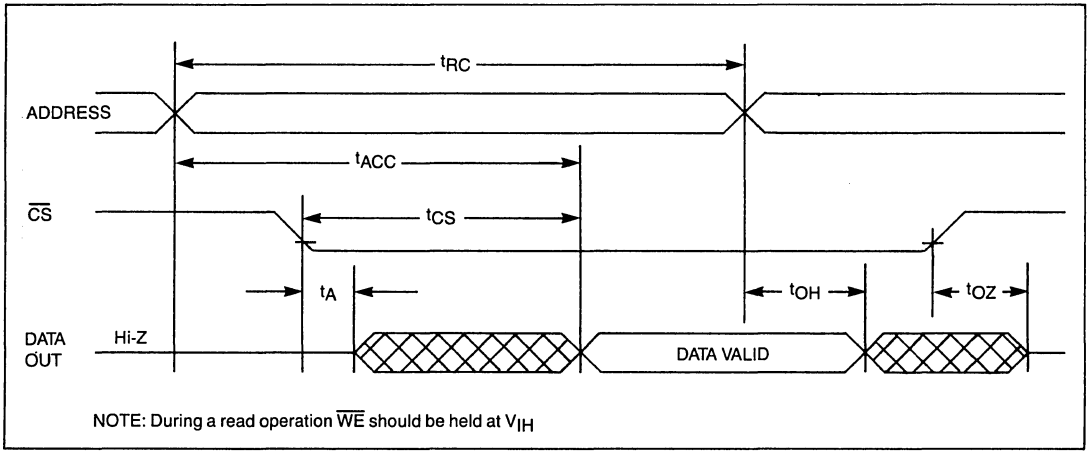
Symbol	Parameter	52212			52212I			52212HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{STC}	Store Cycle Time			10			10			10	ms
t_{STP}	Store Pulse Width	100			100			100			ns
t_{STZ}	Store to Output Hi-Z			100			100			100	ns
N_{SC}	Number of Store Cycles	10^4			10^4			10^4			

RECALL CYCLE

Symbol	Parameter	52212			52212I			52212HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RCC}	Array Recall Cycle Time		30	70			260			360	μs
t_{RCP}	Recall Pulse Width	200			200			450			ns
t_{RCZ}	Recall to Output Hi-Z			100			100			100	ns

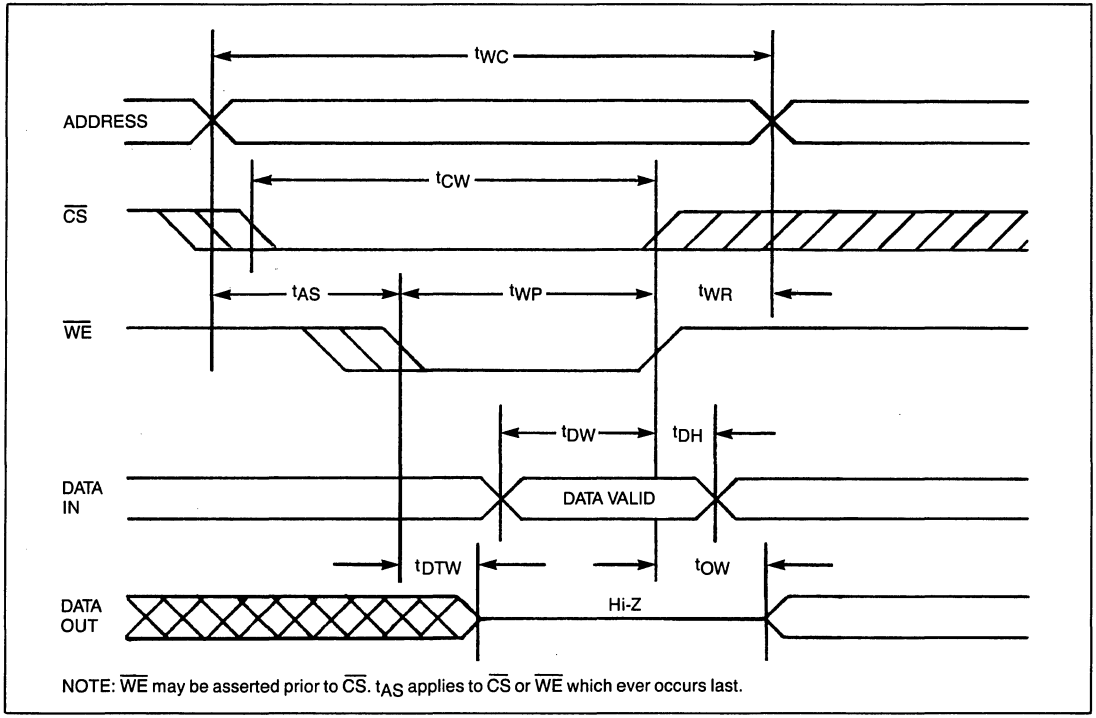
**The 52212 HR data is preliminary and is subject to change.

READ CYCLE



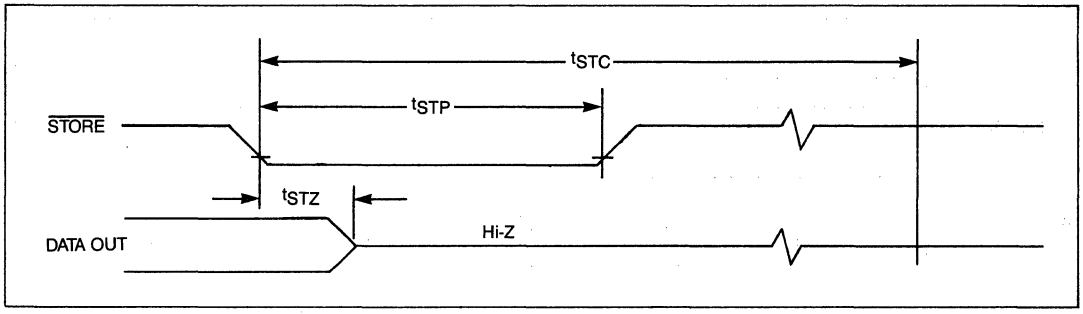
NOTE: During a read operation $\overline{WE}$ should be held at V_{IH}

WRITE CYCLE

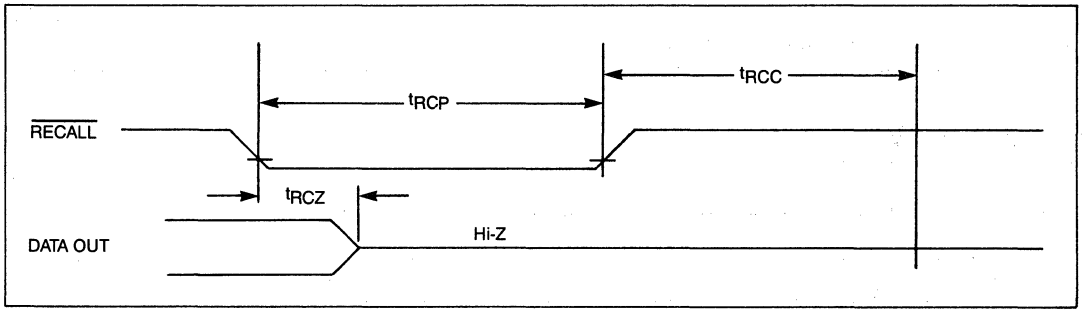


NOTE: $\overline{WE}$ may be asserted prior to $\overline{CS}$. t_{AS} applies to $\overline{CS}$ or $\overline{WE}$ which ever occurs last.

STORE CYCLE



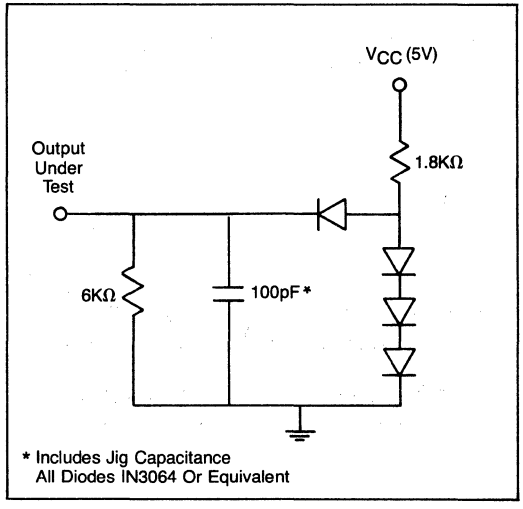
RECALL CYCLE



A. C. CONDITION OF TESTS

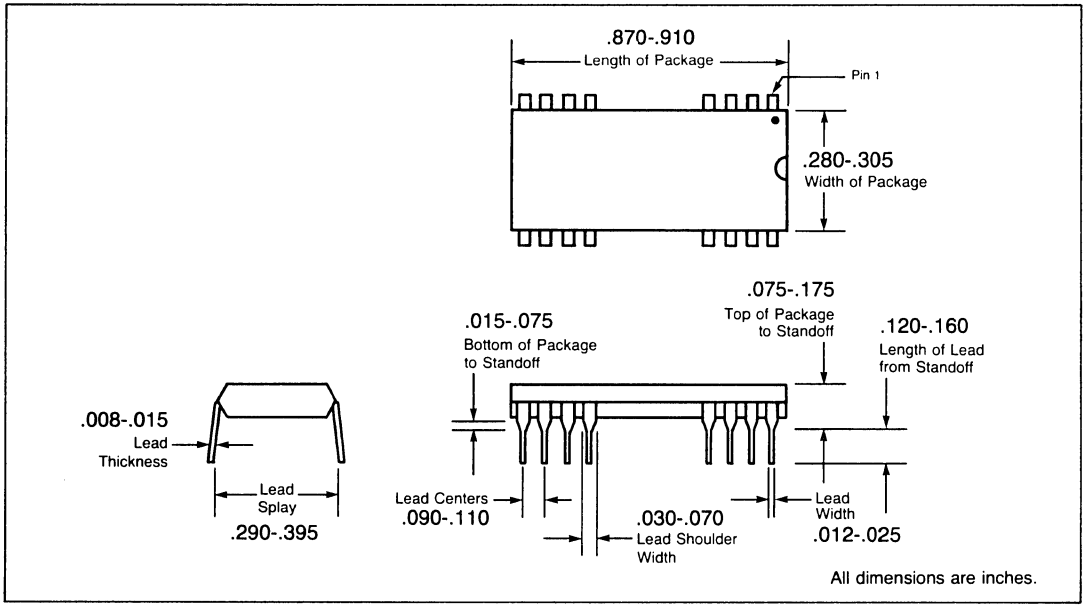
Input Pulse Levels . . . . . 0.8 Volts to 2.0 Volts
Inputs Rise & Fall Times. . . . . 10 ns
Output Timing Levels . . . . . 0.8 Volts to 2.0 Volts

TEST LOAD CIRCUIT

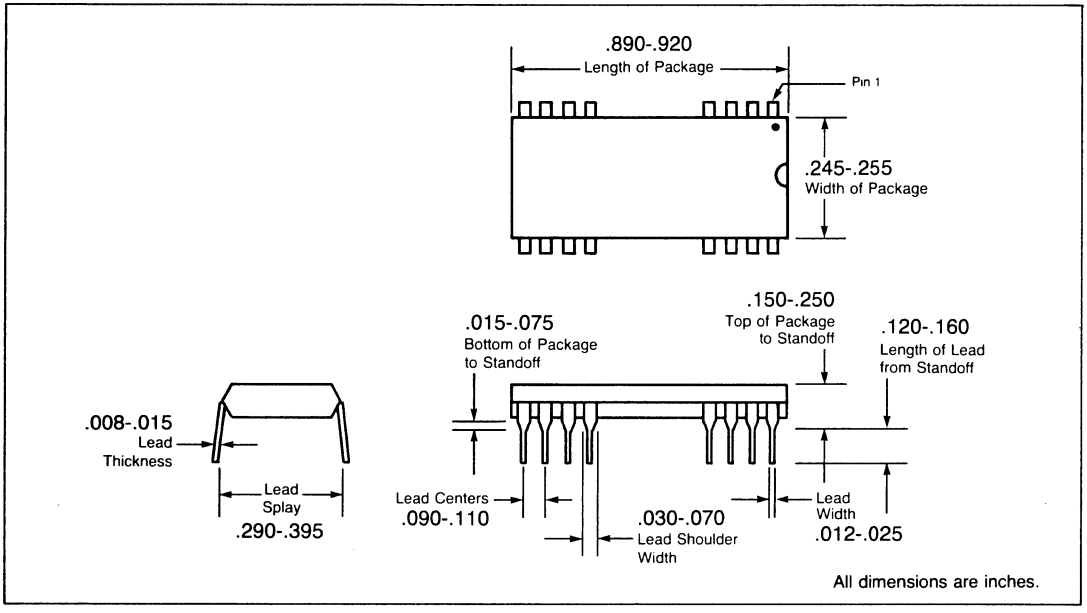


MECHANICAL DATA 18 PIN

CERAMIC DEVICES



PLASTIC DEVICES



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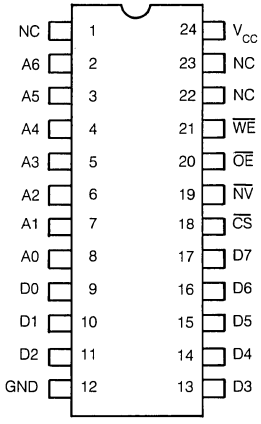
52001
1K BIT (128 x 8)NVRAM

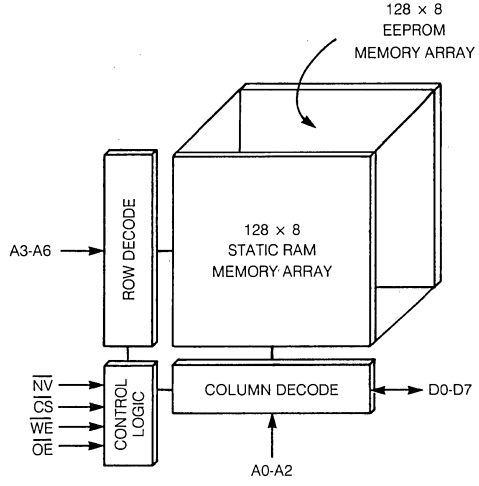
- **1K Bit Static RAM backed by 1K Bit Electrically Erasable PROM**
- **Fully 5V Only Operation**
- **Directly TTL Compatible**
- **In Circuit EEPROM Changes**
- **SRAM Cycle Time less than 300 ns**
- **Power-Failure Protection**
- **Unlimited Recall Cycles**
- **Memory Margining Capability**
- **Operating ranges**
  52001 ..... 0°C to +70°C
  52001I ..... -40°C to +85°C
  52001HR ..... -55°C to +125°C

The NCR 52001 non-volatile RAM combines 1K (128 x 8) bits of conventional static RAM (SRAM) with an identical size array of Electrically Erasable PROM (EEPROM). Non-volatile data can be stored in the EEPROM while independent data is accessed simultaneously in the SRAM. Data can be transferred back and forth between the SRAM and the EEPROM by simple Store and Recall operations. A non-volatile Store signal transfers data from the SRAM to the non-volatile EEPROM where it is safely stored even when power is removed. When power is restored, the data in the EEPROM is automatically recalled into the SRAM. Data stored in the non-volatile EEPROM can be recalled an unlimited number of times. The NCR 52001 requires only a single 5 volt power supply for all modes of operation, and is completely TTL compatible with fully static timing and three state outputs. The NCR 52001 is available in a 24 pin package in commercial, industrial and high reliability versions.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A0-A6	Address Inputs	$\overline{WE}$	Write Enable
D0-D7	Data I/0	$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select	NC	No Connection
$\overline{NV}$	Non-Volatile Enable	V_{CC}	+5 Volts ±10%

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DEVICE OPERATION

SRAM READ/WRITE

The NCR 52001 can be read like a conventional static RAM. With $\overline{CS}$ and $\overline{OE}$ low and $\overline{WE}$ high, valid data will be presented to output pins. With $\overline{CS}$ and $\overline{WE}$ low, and $\overline{OE}$ high, the SRAM can be written to like a conventional static RAM.

STORE

Transferring data from the SRAM to the non-volatile EEPROM is controlled by the Store operation. The $\overline{NV}$ input signal controls the non-volatile operations (i.e., Store and Recall), except for automatic data recall upon power up. When $\overline{NV}$ and $\overline{WE}$ are brought low, the entire contents of the SRAM array are copied into the non-volatile EEPROM array. The data in the SRAM is unaffected by a Store operation. The Recall cycle is inhibited by a Store operation, and $\overline{CS}$ can either be high or low.

The I/0 terminals are in the high impedance state during a Store operation. The contents of the EEPROM remain valid with or without power being supplied. The data retention time of the EEPROM can be measured by memory margining.

During power up or power down, precaution must be taken to prevent an unintentional Store cycle. Holding $\overline{NV}$ high will inhibit the initiation of a Store cycle. Additionally, a Store operation should not be initiated until the supply voltage (V_{CC}) is at specification limits.

RECALL

The data stored in the non-volatile EEPROM array is transferred back into the SRAM by the Recall operation. When $\overline{NV}$ and $\overline{OE}$ are brought low, the entire contents of the EEPROM are copied back into the SRAM (overwriting any data already existing in the SRAM). An Array Recall cycle can take place when $\overline{CS}$ is either high or low. An array Recall operation will automatically be performed upon power up. The data in the EEPROM is unaffected by a Recall operation.

The Data I/0 terminals are in a high impedance state during a non-volatile operation (i.e., Store or Recall). When a non-volatile cycle is initiated, all other operations are inhibited until the first operation is complete.

MEMORY MARGINING

The NCR 52001 supports margining of the memory transistors. Memory margining allows device retention time to be projected for the purpose of device evaluation. An application note describing the memory margining algorithm is available.

MODE SELECTION

	INPUTS			
MODE	$\overline{CS}$	$\overline{NV}$	$\overline{WE}$	$\overline{OE}$
READ	L	H	H	L
WRITE	L	H	L	H
STORE	X	L	L	H
RECALL	X	L	H	L

ABSOLUTE MAXIMUM RATINGS

All inputs or outputs relative to Vss . . . . . – 0.5 to + 7V
Storage temperature without
data retention . . . . . –65°C to + 150°C

Stress above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operational limits stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

		52001			52001I			52001HR**			
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	Input high level voltage	2.0		V_{CC}	2.0		V_{CC}	2.0		V_{CC}	V
V_{IL}	Input low level voltage	-0.3		0.8	-0.3		0.8	-0.3		0.8	V
T_A	Ambient Temperature	0		70	-40		85	-55		125	°C

All voltages are with respect to GND.

STATIC ELECTRICAL CHARACTERISTICS, OVER RECOMMENDED OPERATION CONDITIONS (UNLESS OTHERWISE NOTED)

			52001			52001I			52001HR**			
Symbol	Parameter	Condition	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{IN}	Input leakage current	V_{IN} = 0V TO 5.5V		0.1	10		0.1	10		0.1	10	µA
I_O	I_O leakage current	V_O = 0.4V TO 5.5V Chip Deselected		0.1	10		0.1	10		0.1	10	µA
I_{CC}	Supply Current	Outputs Open		35	70		45	80			80	
V_{OH}	Output High Voltage	I_{OH} = -400µA	2.4			2.4			2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			0.4			0.4			0.4	V
T_S	Non-Volatile storage time		1.0									yr

*Typical values are at 25°C and typical supply voltages.

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

			52001			52001I			52001HR**			
Symbol	Parameter	Condition	Min	Typ	Max	Min	Typ*	Max	Min	Typ	Max	Unit
C	Capacitance of Input & Data I/O pins	All pins at VSS (ground)			10			10			10	pF

**The 52001HR Data is preliminary and is subject to change.

NCR

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

READ CYCLE

		52001			52001I			52001HR**			
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
t_{RC}	Read Cycle Time	300			300			450			ns
t_{ACC}	Address Access Time			300			300			450	ns
t_{A}	Chip Select or Output Enable to Data Active	0			0			0			ns
t_{OE}	Output Enable Time			100			120			120	ns
t_{CS}	Chip Select Access Time			100			120			120	ns
t_{OH}	Output Hold Time	10			10			10			ns
t_{OZ}	Chip Select Or Output Enable To Output High Impedance Time			90			90			90	ns

WRITE CYCLE

		52001			52001I			52001HR**			
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
t_{WC}	Write Cycle Time	300			300			450			ns
t_{W}	Write Pulse Width	150			150			300			ns
t_{WR}	Write Release Time	25			25			25			ns
t_{DW}	Data to Write Time Overlap	150			150			200			ns
t_{DH}	Data Hold From Write Time	20			20			20			ns
t_{AS}	Address Setup Time	50			50			50			ns

STORE CYCLE

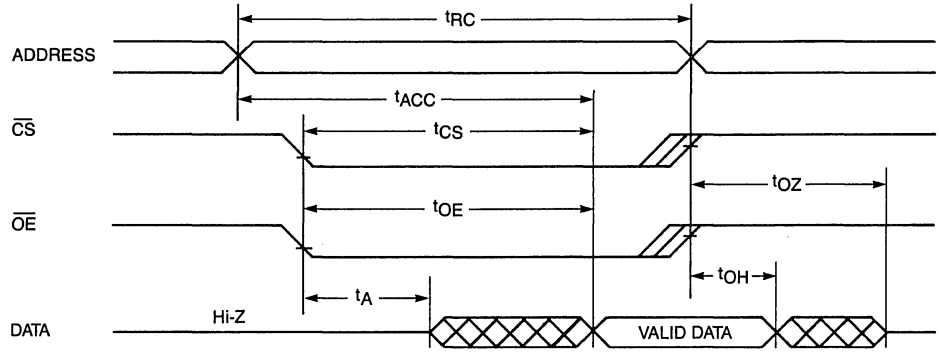
		52001			52001I			52001HR**			
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
t_{STC}	Store Cycle Time			10			10			10	ms
t_{NW}	NV to Write Overlap	100			100			100			ns
t_{NS}	NV Setup Time	0			0			0			ns
t_{STZ}	Store to Output Hi-Z			100			100			100	ns
t_{SC}	Number of Store Cycles	10^4			10^4			10^4			cycle

RECALL CYCLE

		52001			52001I			52001HR**			
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
t_{RCC}	Array Recall Cycle Time			70			260			360	μs
t_{NO}	NV to Output Overlap	200			450			450			ns
t_{NS}	NV Setup time	0			0			0			ns
t_{RCZ}	Recall to Output Hi-Z			100			100			100	ns

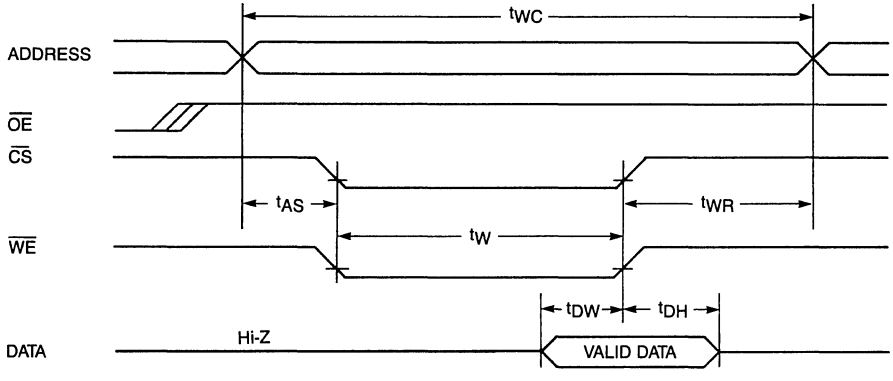
**The 52001HR Data is preliminary and is subject to change.

READ CYCLE



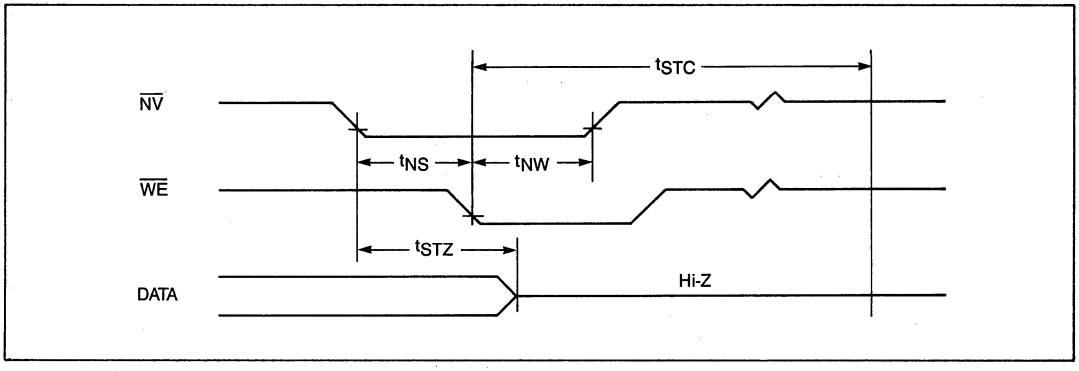
NOTE: During a read operation $\overline{WE}$ should be held at V_{IH}.

WRITE CYCLE

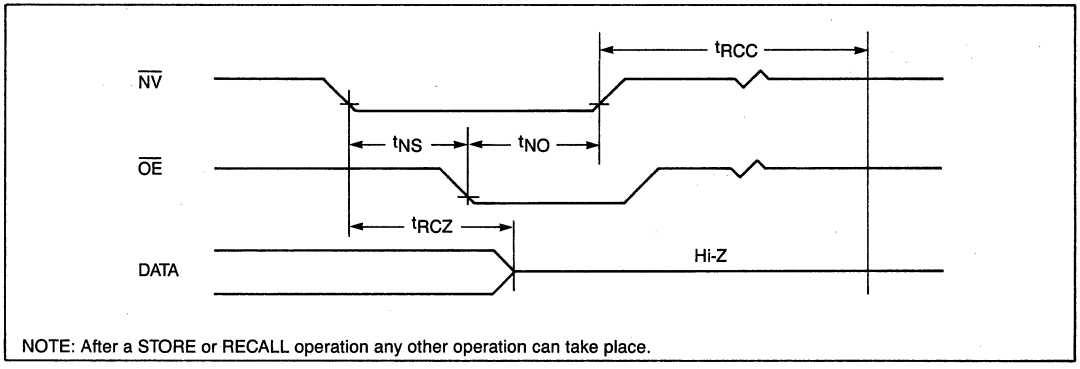


NOTE: $\overline{WE}$ may be asserted prior to $\overline{CS}$. t_{AS} applies to $\overline{CS}$ or $\overline{WE}$ whichever occurs last.

STORE CYCLE



RECALL CYCLE

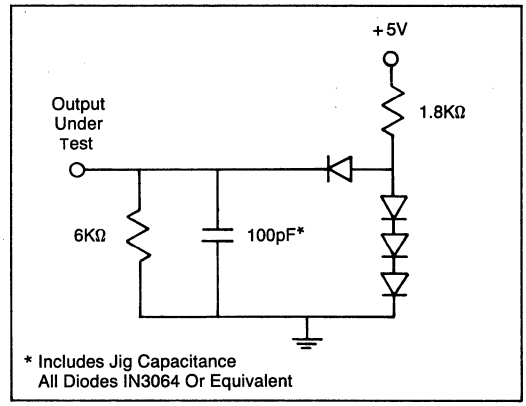


NOTE: After a STORE or RECALL operation any other operation can take place.

A. C. CONDITIONS OF TESTS

Input Pulse Levels . . . . . 0.8 Volts to 2.0 Volts
Input Rise & Fall Times . . . . . 10 nsec
Output Timing Levels . . . . . 0.8 Volts to 2.0 Volts

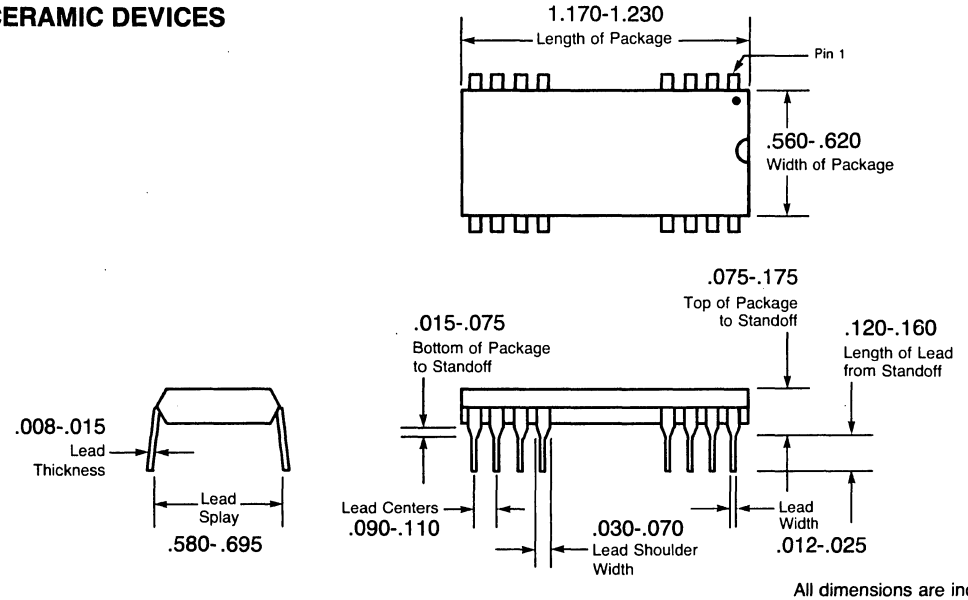
TEST LOAD CIRCUIT



* Includes Jig Capacitance
All Diodes IN3064 Or Equivalent

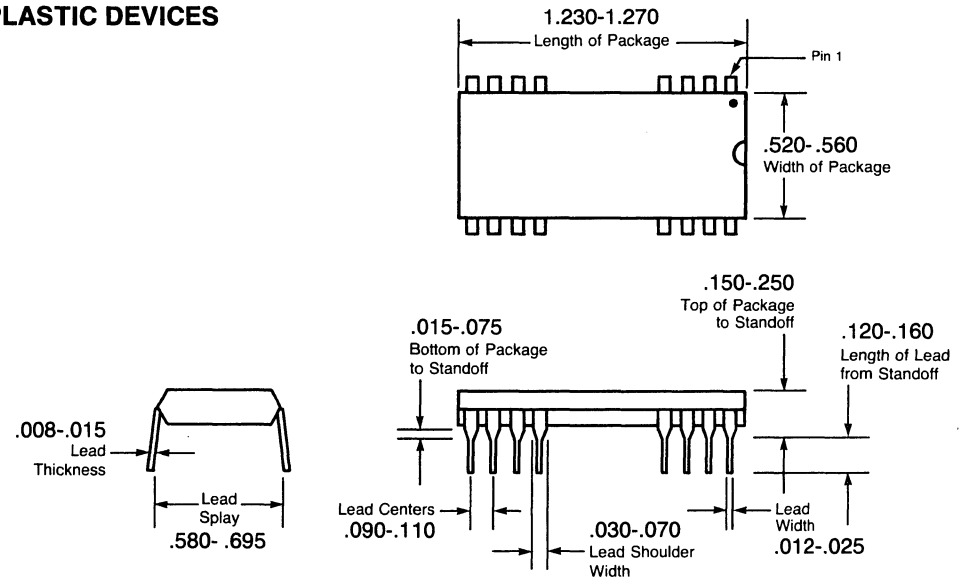
MECHANICAL DATA 24 PIN

CERAMIC DEVICES



All dimensions are inches.

PLASTIC DEVICES



All dimensions are inches.

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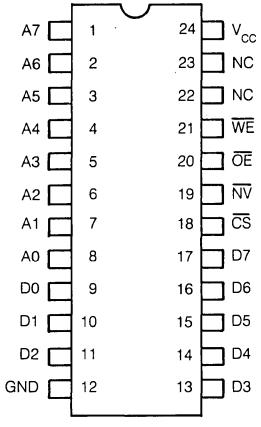
513/866-7217 Ohio or International

52002
2K BIT (256 x 8)NVRAM

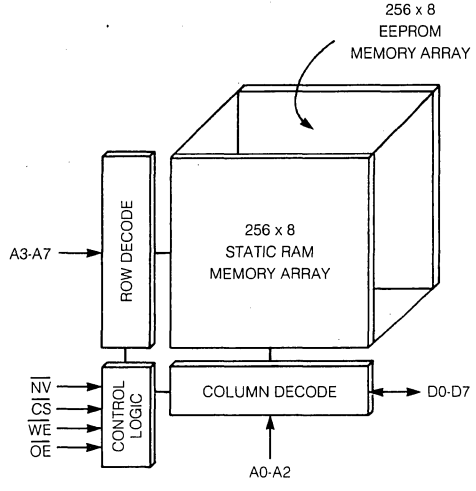
- **2K Bit Static RAM backed by 2K Bit Electrically Erasable PROM**
- **Fully 5V Only Operation**
- **Directly TTL Compatible**
- **In Circuit EEPROM Changes**
- **SRAM Cycle Time less than 300 ns**
- **Power-Failure Protection**
- **Unlimited Recall Cycles**
- **Memory Margining Capability**
- **Operating ranges**
  52002 ..... 0°C to +70°C
  52002I ..... -40°C to +85°C
  52002HR ..... -55°C to +125°C

The NCR 52002 non-volatile RAM combines 2K (256 x 8) bits of conventional static RAM (SRAM) with an identical size array of Electrically Erasable PROM (EEPROM). Non-volatile data can be stored in the EEPROM while independent data is accessed simultaneously in the SRAM. Data can be transferred back and forth between the SRAM and the EEPROM by simple Store and Recall operations. A non-volatile Store signal transfers data from the SRAM to the non-volatile EEPROM where it is safely stored even when power is removed. When power is restored, the data in the EEPROM is automatically recalled into the SRAM. Data stored in the non-volatile EEPROM can be recalled an unlimited number of times. The NCR 52002 requires only a single 5 volt power supply for all modes of operation, and is completely TTL compatible with fully static timing and three state outputs. The NCR 52002 is available in a 24 pin package in commercial, industrial and high reliability versions.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A0-A7	Address Inputs	$\overline{WE}$	Write Enable
D0-D7	Data I/0	$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select	NC	No Connection
$\overline{NV}$	Non-Volatile Enable	V_{CC}	+5 Volts ±10%

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DEVICE OPERATION

SRAM READ/WRITE

The NCR 52002 can be read like a conventional static RAM. With $\overline{CS}$ and $\overline{OE}$ low and $\overline{WE}$ high, valid data will be presented to output pins. With $\overline{CS}$ and $\overline{WE}$ low, and $\overline{OE}$ high, the SRAM can be written to like a conventional static RAM.

STORE

Transferring data from the SRAM to the non-volatile EEPROM is controlled by the Store operation. The $\overline{NV}$ input signal controls the non-volatile operations (i.e., Store and Recall), except for automatic data recall upon power up. When $\overline{NV}$ and $\overline{WE}$ are brought low, the entire contents of the SRAM array are copied into the non-volatile EEPROM array. The data in the SRAM is unaffected by a Store operation. The Recall cycle is inhibited by a Store operation, and $\overline{CS}$ can either be high or low.

The I/0 terminals are in the high impedance state during a Store operation. The contents of the EEPROM remain valid with or without power being supplied. The data retention time of the EEPROM can be measured by memory margining.

During power up or power down, precaution must be taken to prevent an unintentional Store cycle. Holding $\overline{NV}$ high will inhibit the initiation of a Store cycle. Additionally, a Store operation should not be initiated until the supply voltage (V_{CC}) is at specification limits.

RECALL

The data stored in the non-volatile EEPROM array is transferred back into the SRAM by the Recall operation. When $\overline{NV}$ and $\overline{OE}$ are brought low, the entire contents of the EEPROM are copied back into the SRAM (overwriting any data already existing in the SRAM). An Array Recall cycle can take place when $\overline{CS}$ is either high or low. An array Recall operation will automatically be performed upon power up. The data in the EEPROM is unaffected by a Recall operation.

The Data I/0 terminals are in a high impedance state during a non-volatile operation (i.e., Store or Recall). When a non-volatile cycle is initiated, all other operations are inhibited until the first operation is complete.

MEMORY MARGINING

The NCR 52002 supports margining of the memory transistors. Memory margining allows device retention time to be projected for the purpose of device evaluation. An application note describing the memory margining algorithm is available.

MODE SELECTION

	INPUTS			
MODE	$\overline{CS}$	$\overline{NV}$	$\overline{WE}$	$\overline{OE}$
READ	L	H	H	L
WRITE	L	H	L	H
STORE	X	L	L	H
RECALL	X	L	H	L

ABSOLUTE MAXIMUM RATINGS

All inputs or outputs relative to Vss . . . . . −0.5 to +7V
Storage temperature without
data retention . . . . . .−65°C to + 150°C

Stress above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operational limits stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

		52002			52002I			52002HR**			
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	Input high level voltage	2.0		V_{CC}	2.0		V_{CC}	2.0		V_{CC}	V
V_{IL}	Input low level voltage	−0.3		0.8	−0.3		0.8	−0.3		0.8	V
T_A	Ambient Temperature	0		70	−40		85	−55		125	°C

All voltages are with respect to GND.

STATIC ELECTRICAL CHARACTERISTICS, OVER RECOMMENDED OPERATION CONDITIONS (UNLESS OTHERWISE NOTED)

			52002			52002I			52002HR**			
Symbol	Parameter	Condition	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{IN}	Input leakage current	V_{IN} = 0V TO 5.5V		0.1	10		0.1	10		0.1	10	µA
I_O	I_O leakage current	V_O = 0.4V TO 5.5V Chip Deselected		0.1	10		0.1	10		0.1	10	µA
I_{CC}	Supply Current	Outputs Open		35	70		45	80		45	80	mA
V_{OH}	Output High Voltage	I_{OH} = −400µA	2.4			2.4			2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			0.4			0.4			0.4	V
T_S	Non-Volatile storage time		1.0									yr

*Typical values are at 25°C and typical supply voltages.

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

			52002			52002I			52002HR**			
Symbol	Parameter	Condition	Min	Typ	Max	Min	Typ*	Max	Min	Typ	Max	Unit
C	Capacitance of Input & Data I/O pins	All pins at VSS (ground)			10			10			10	pF

**The 52002HR Data is preliminary and is subject to change.

NCR

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

READ CYCLE

Symbol	Parameter	52002			52002I			52002HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RC}	Read Cycle Time	300			300			450			ns
t_{ACC}	Address Access Time			300			300			450	ns
t_{A}	Chip Select or Output Enable to Data Active	0			0			0			ns
t_{OE}	Output Enable Time			100			120			120	ns
t_{CS}	Chip Select Access Time			100			120			120	ns
t_{OH}	Output Hold Time	10			10			10			ns
t_{OZ}	Chip Select Or Output Enable To Output High Impedance Time			90			90			90	ns

WRITE CYCLE

Symbol	Parameter	52002			52002I			52002HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{WC}	Write Cycle Time	300			300			450			ns
t_{W}	Write Pulse Width	150			150			300			ns
t_{WR}	Write Release Time	25			25			25			ns
t_{DW}	Data to Write Time Overlap	150			150			200			ns
t_{DH}	Data Hold From Write Time	20			20			20			ns
t_{AS}	Address Setup Time	50			50			50			ns

STORE CYCLE

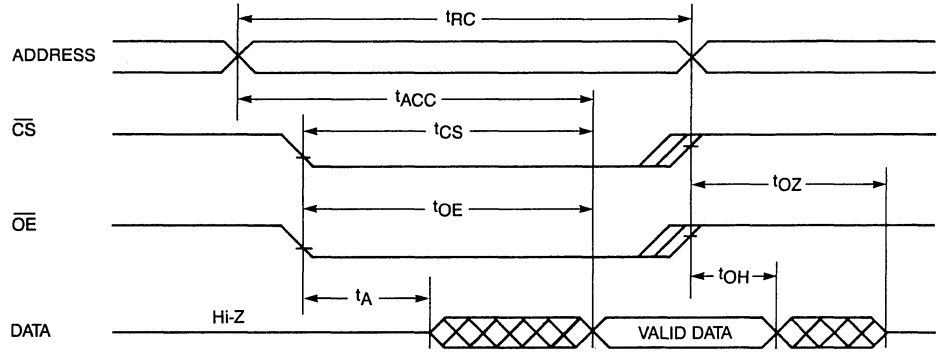
Symbol	Parameter	52002			52002I			52002HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{STC}	Store Cycle Time			10			10			10	ms
t_{NW}	NV to Write Overlap	100			100			100			ns
t_{NS}	NV Setup Time	0			0			0			ns
t_{STZ}	Store to Output Hi-Z			100			100			100	ns
t_{SC}	Number of Store Cycles	10^4			10^4			10^4			cycle

RECALL CYCLE

Symbol	Parameter	52002			52002I			52002HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RCC}	Array Recall Cycle Time			70			260			360	μs
t_{NO}	NV to Output Overlap	200			450			450			ns
t_{NS}	NV Setup time	0			0			0			ns
t_{RCZ}	Recall to Output Hi-Z			100			100			100	ns

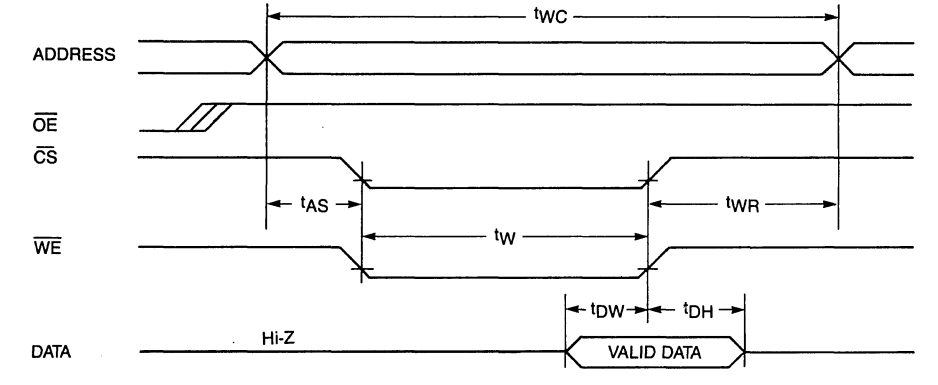
**The 52002HR Data is preliminary and is subject to change.

READ CYCLE



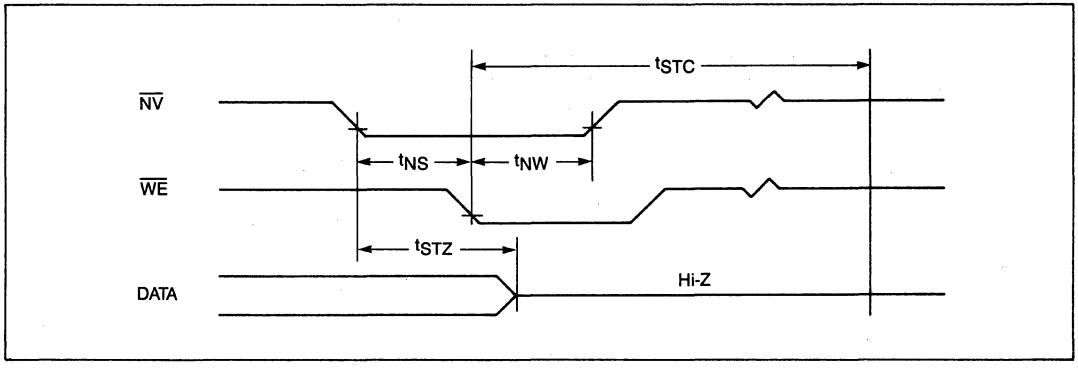
NOTE: During a read operation $\overline{WE}$ should be held at V_{IH}.

WRITE CYCLE

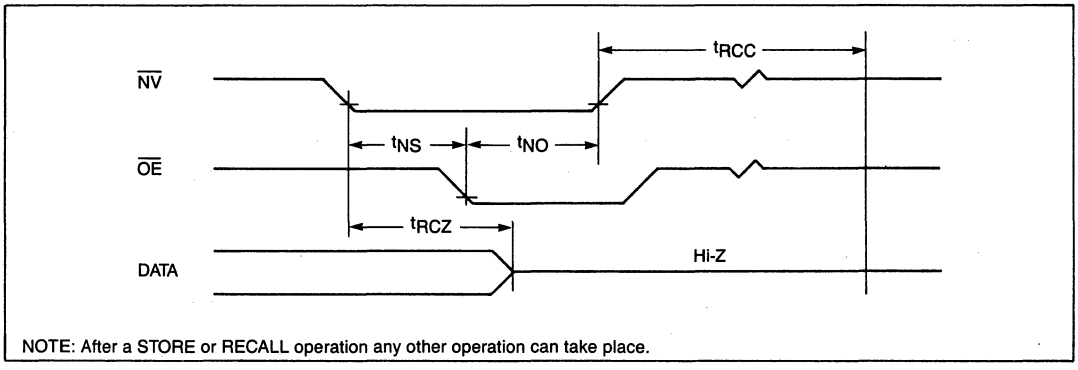


NOTE: $\overline{WE}$ may be asserted prior to $\overline{CS}$. t_{AS} applies to $\overline{CS}$ or $\overline{WE}$ whichever occurs last.

STORE CYCLE



RECALL CYCLE

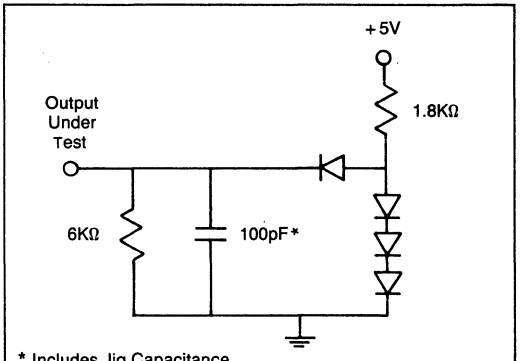


NOTE: After a STORE or RECALL operation any other operation can take place.

A. C. CONDITIONS OF TESTS

Input Pulse Levels . . . . . 0.8 Volts to 2.0 Volts
Input Rise & Fall Times . . . . . 10 nsec
Output Timing Levels . . . . . 0.8 Volts to 2.0 Volts

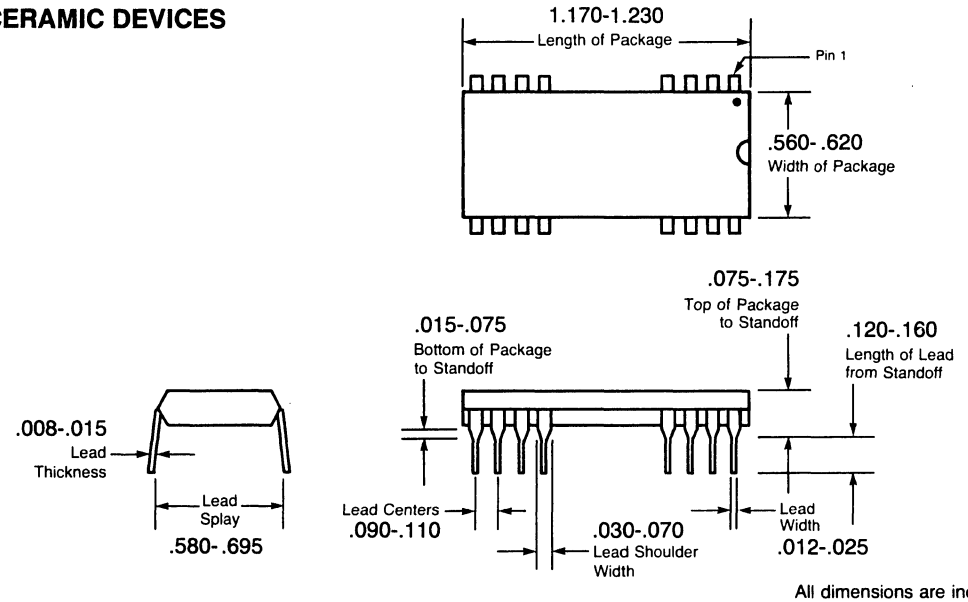
TEST LOAD CIRCUIT



* Includes Jig Capacitance
All Diodes IN3064 Or Equivalent

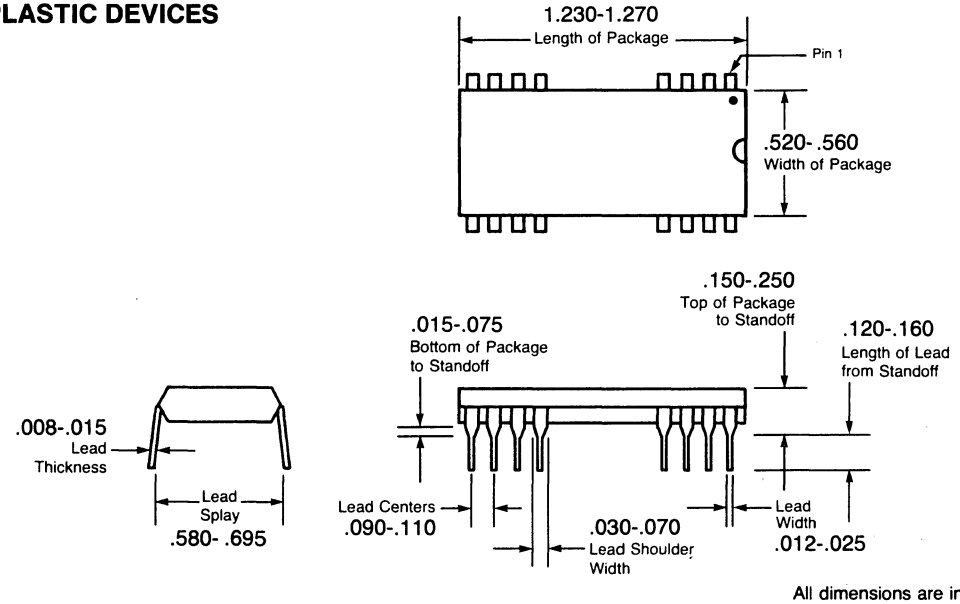
MECHANICAL DATA 24 PIN

CERAMIC DEVICES



All dimensions are inches.

PLASTIC DEVICES



All dimensions are inches.

NCR

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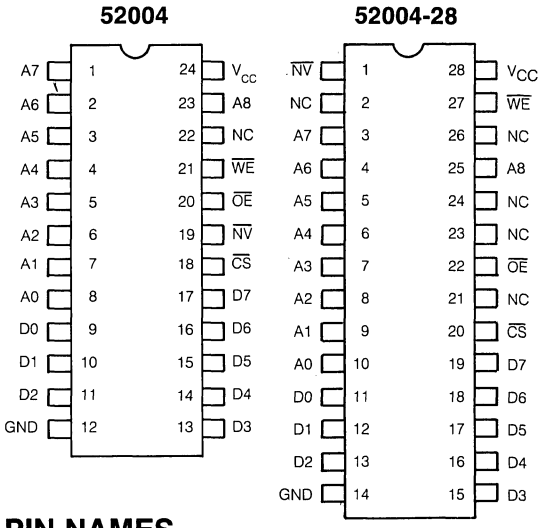
52004
4K BIT (512 x 8)NVRAM

PRELIMINARY

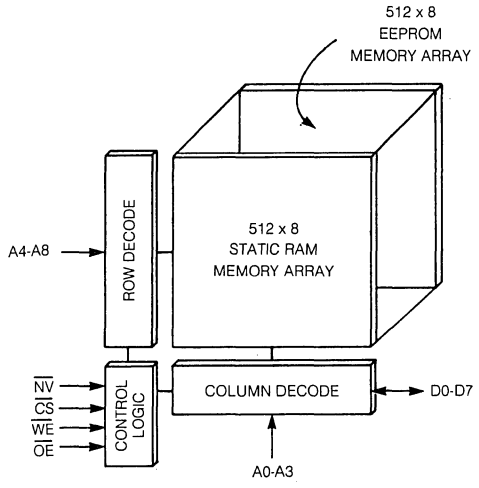
- **4K Bit Static RAM backed by 4K Bit Electrically Erasable PROM**
- **Fully 5V Only Operation**
- **Directly TTL Compatible**
- **In Circuit EEPROM Changes**
- **SRAM Cycle Time less than 300 ns**
- **Power-Failure Protection**
- **Unlimited Recall Cycles**
- **Memory Margining Capability**
- **Operating ranges**
  52004 ..... 0°C to +70°C
  52004I ..... -40°C to +85°C
  52004HR ..... -55°C to +125°C

The NCR 52004 non-volatile RAM combines 4K (512 x 8) bits of conventional static RAM (SRAM) with an identical size array of Electrically Erasable PROM (EEPROM). Non-volatile data can be stored in the EEPROM while independent data is accessed simultaneously in the SRAM. Data can be transferred back and forth between the SRAM and the EEPROM by simple Store and Recall operations. A non-volatile Store signal transfers data from the SRAM to the non-volatile EEPROM where it is safely stored even when power is removed. When power is restored, the data in the EEPROM is automatically recalled into the SRAM. Data stored in the non-volatile EEPROM can be recalled an unlimited number of times. The NCR 52004 requires only a single 5 volt power supply for all modes of operation, and is completely TTL compatible with fully static timing and three state outputs. The NCR 52004 is available in a 24 pin package and an optional 28 pin package, in commercial, industrial and high reliability versions.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A0-A8	Address Inputs	$\overline{WE}$	Write Enable
D0-D7	Data I/0	$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select	NC	No Connection
$\overline{NV}$	Non-Volatile Enable	V_{CC}	+5 Volts ±10%

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This is advance information and NCR reserves the right to change the specifications without notice.

DEVICE OPERATION

SRAM READ/WRITE

The NCR 52004 can be read like a conventional static RAM. With $\overline{CS}$ and $\overline{OE}$ low and $\overline{WE}$ high, valid data will be presented to output pins. With $\overline{CS}$ and $\overline{WE}$ low, and $\overline{OE}$ high, the SRAM can be written to like a conventional static RAM.

STORE

Transferring data from the SRAM to the non-volatile EEPROM is controlled by the Store operation. The $\overline{NV}$ input signal controls the non-volatile operations (i.e., Store and Recall), except for automatic data recall upon power up. When $\overline{NV}$ and $\overline{WE}$ are brought low, the entire contents of the SRAM array are copied into the non-volatile EEPROM array. The data in the SRAM is unaffected by a Store operation. The Recall cycle is inhibited by a Store operation, and $\overline{CS}$ can either be high or low.

The I/0 terminals are in the high impedance state during a Store operation. The contents of the EEPROM remain valid with or without power being supplied. The data retention time of the EEPROM can be measured by memory margining.

During power up or power down, precaution must be taken to prevent an unintentional Store cycle. Holding $\overline{NV}$ high will inhibit the initiation of a Store cycle. Additionally, a Store operation should not be initiated until the supply voltage (V_{CC}) is at specification limits.

RECALL

The data stored in the non-volatile EEPROM array is transferred back into the SRAM by the Recall operation. When $\overline{NV}$ and $\overline{OE}$ are brought low, the entire contents of the EEPROM are copied back into the SRAM (overwriting any data already existing in the SRAM). An Array Recall cycle can take place when $\overline{CS}$ is either high or low. An array Recall operation will automatically be performed upon power up. The data in the EEPROM is unaffected by a Recall operation.

The Data I/0 terminals are in a high impedance state during a non-volatile operation (i.e., Store or Recall). When a non-volatile cycle is initiated, all other operations are inhibited until the first operation is complete.

MEMORY MARGINING

The NCR 52004 supports margining of the memory transistors. Memory margining allows device retention time to be projected for the purpose of device evaluation. An application note describing the memory margining algorithm is available.

MODE SELECTION

	INPUTS			
MODE	$\overline{CS}$	$\overline{NV}$	$\overline{WE}$	$\overline{OE}$
READ	L	H	H	L
WRITE	L	H	L	H
STORE	X	L	L	H
RECALL	X	L	H	L

ABSOLUTE MAXIMUM RATINGS

All inputs or outputs relative to Vss . . . . . – 0.5 to + 7V
Storage temperature without
data retention . . . . . –65°C to + 150°C

Stress above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operational limits stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

		52004			52004I			52004HR**			
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	Input high level voltage	2.0		V_{CC}	2.0		V_{CC}	2.0		V_{CC}	V
V_{IL}	Input low level voltage	–0.3		0.8	–0.3		0.8	–0.3		0.8	V
T_A	Ambient Temperature	0		70	–40		85	–55		125	°C

All voltages are with respect to GND.

STATIC ELECTRICAL CHARACTERISTICS, OVER RECOMMENDED OPERATION CONDITIONS (UNLESS OTHERWISE NOTED)

			52004			52004I			52004HR**			
Symbol	Parameter	Condition	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{IN}	Input leakage current	V_{IN} = 0V TO 5.5V		0.1	10		0.1	10		0.1	10	µA
I_O	I_O leakage current	V_O = 0.4V TO 5.5V Chip Deselected		0.1	10		0.1	10		0.1	10	µA
I_{CC}	Supply Current	Outputs Open		35	70		45	80		45	80	mA
V_{OH}	Output High Voltage	I_{OH} = –400µA	2.4			2.4			2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			0.4			0.4			0.4	V
T_S	Non-Volatile storage time		TBD									yr

*Typical values are at 25°C and typical supply voltages.

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

			52004			52004I			52004HR**			
Symbol	Parameter	Condition	Min	Typ	Max	Min	Typ*	Max	Min	Typ	Max	Unit
C	Capacitance of Input & Data I/O pins	All pins at VSS (ground)			10			10			10	pF

* *The 52004HR Data is preliminary and is subject to change.

NCR

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

READ CYCLE

		52004			52004I			52004HR**			
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
t_{RC}	Read Cycle Time	300			300			450			ns
t_{ACC}	Address Access Time			300			300			450	ns
t_{A}	Chip Select or Output Enable to Data Active	0			0			0			ns
t_{OE}	Output Enable Time			100			120			120	ns
t_{CS}	Chip Select Access Time			100			120			120	ns
t_{OH}	Output Hold Time	10			10			10			ns
t_{OZ}	Chip Select Or Output Enable To Output High Impedance Time			90			90			90	ns

WRITE CYCLE

		52004			52004I			52004HR**			
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
t_{WC}	Write Cycle Time	300			300			450			ns
t_{W}	Write Pulse Width	150			150			300			ns
t_{WR}	Write Release Time	25			25			25			ns
t_{DW}	Data to Write Time Overlap	150			150			200			ns
t_{DH}	Data Hold From Write Time	20			20			20			ns
t_{AS}	Address Setup Time	50			50			50			ns

STORE CYCLE

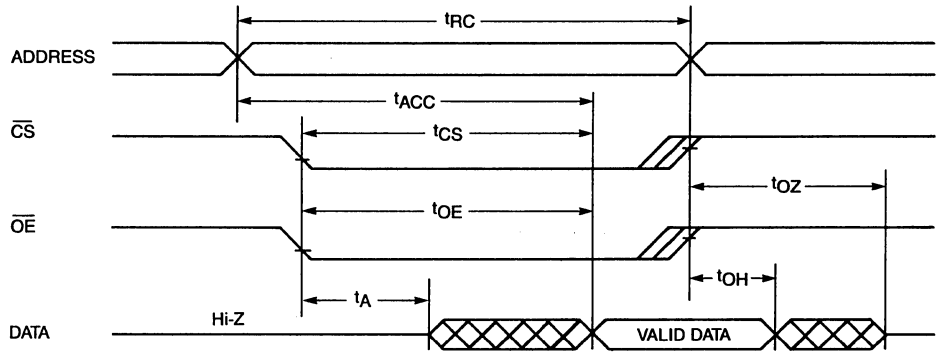
		52004			52004I			52004HR**			
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
t_{STC}	Store Cycle Time			10			10			10	ms
t_{NW}	NV to Write Overlap	100			100			100			ns
t_{NS}	NV Setup Time	0			0			0			ns
t_{STZ}	Store to Output Hi-Z			100			100			100	ns
t_{SC}	Number of Store Cycles	10^4			10^4			10^4			cycle

RECALL CYCLE

		52004			52004I			52004HR**			
Symbol	Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
t_{RCC}	Array Recall Cycle Time			20							μs
t_{NO}	NV to Output Overlap	200			450			450			ns
t_{NS}	NV Setup time	0			0			0			ns
t_{RCZ}	Recall to Output Hi-Z			100			100			100	ns

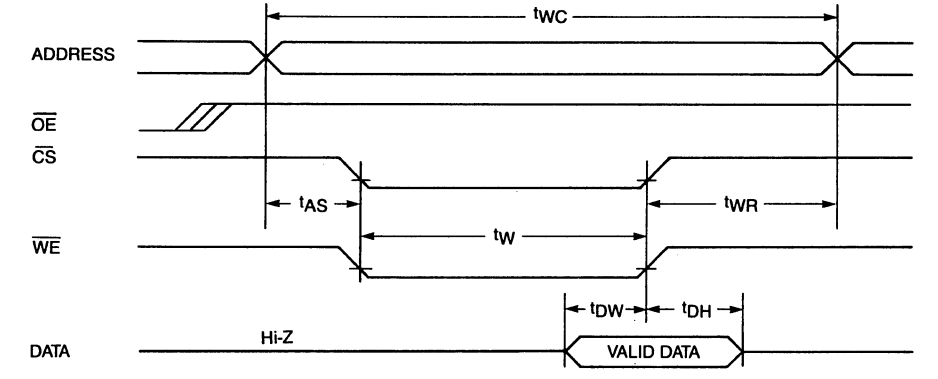
**The 52004HR Data is preliminary and is subject to change.

READ CYCLE



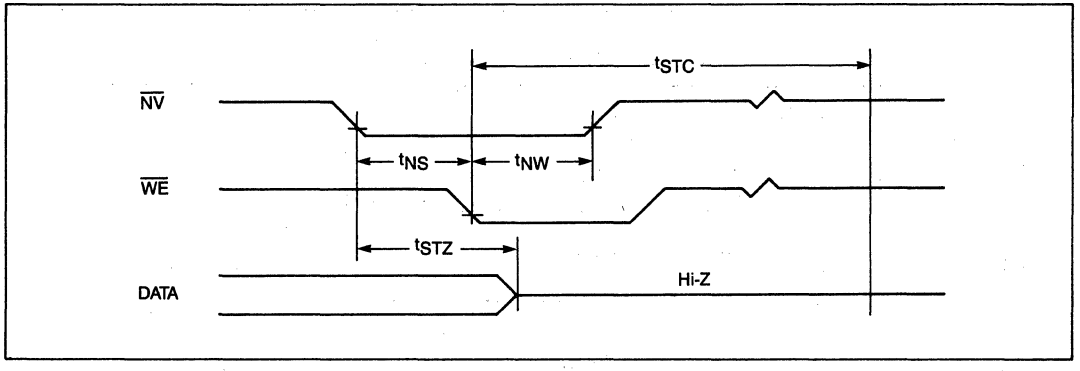
NOTE: During a read operation $\overline{WE}$ should be held at V_{IH}.

WRITE CYCLE

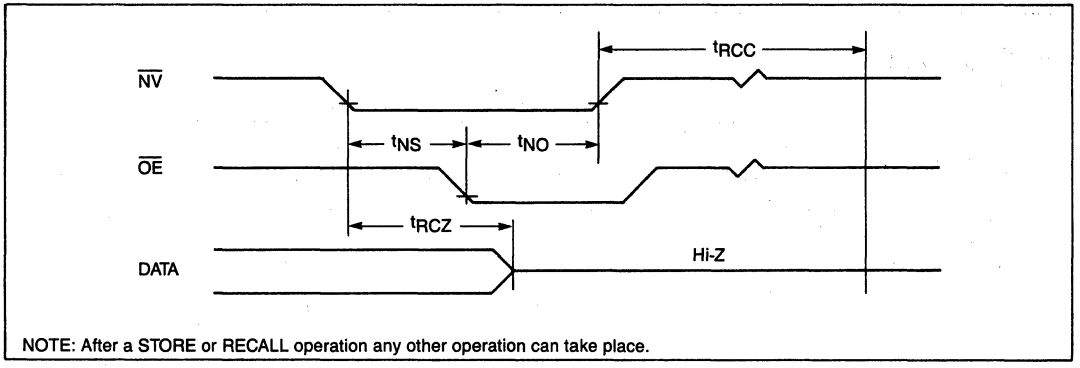


NOTE: $\overline{WE}$ may be asserted prior to $\overline{CS}$. t_{AS} applies to $\overline{CS}$ or $\overline{WE}$ whichever occurs last.

STORE CYCLE



RECALL CYCLE

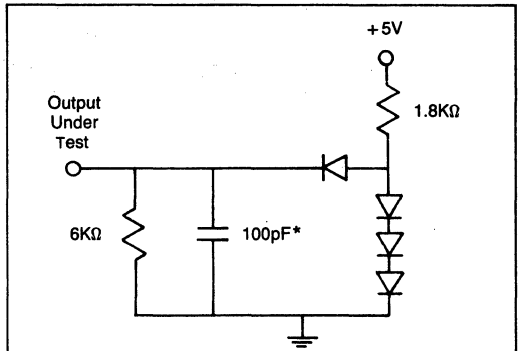


NOTE: After a STORE or RECALL operation any other operation can take place.

A. C. CONDITIONS OF TESTS

Input Pulse Levels . . . . . 0.8 Volts to 2.0 Volts
Input Rise & Fall Times . . . . . 10 nsec
Output Timing Levels . . . . . 0.8 Volts to 2.0 Volts

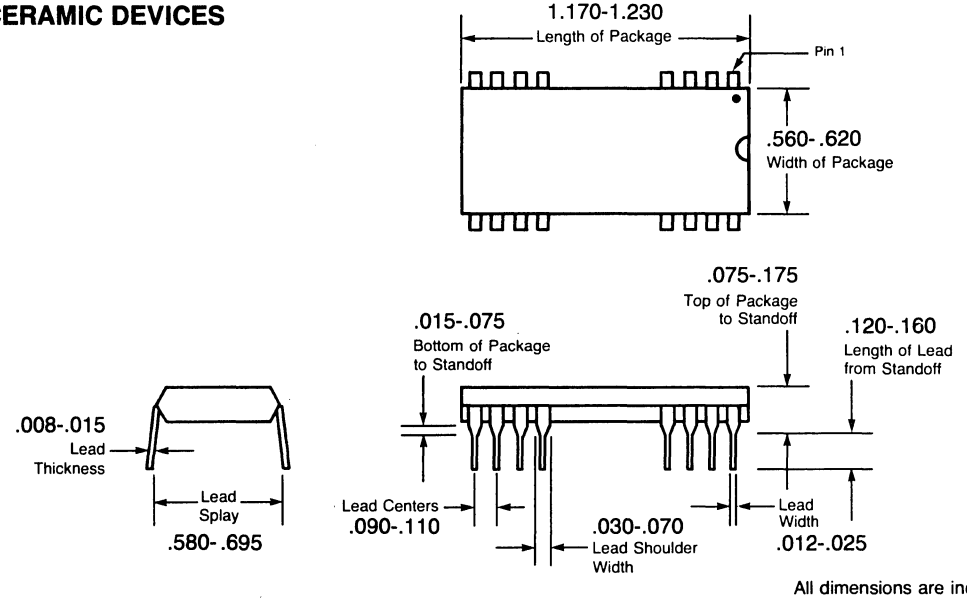
TEST LOAD CIRCUIT



* Includes Jig Capacitance
All Diodes IN3064 Or Equivalent

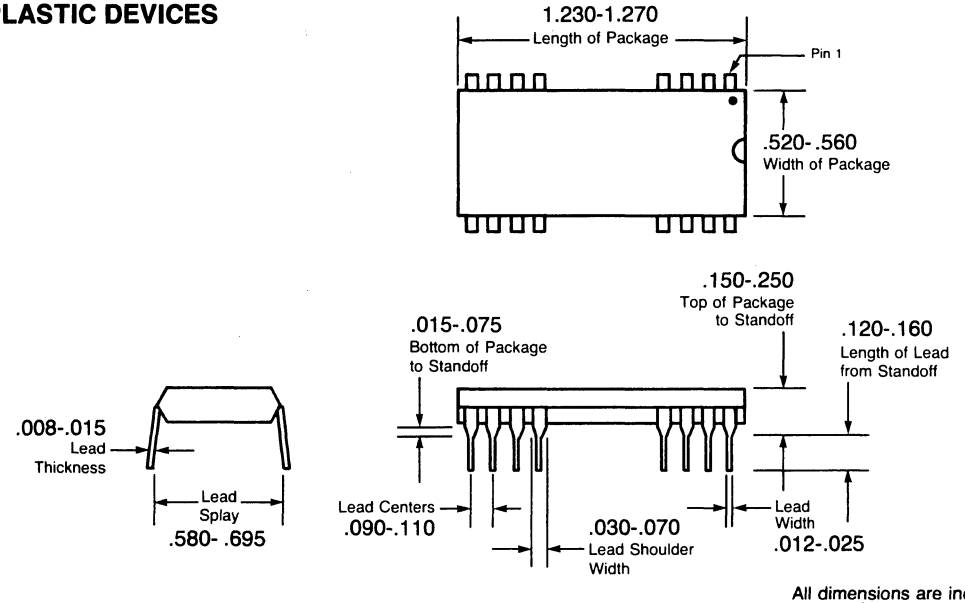
MECHANICAL DATA 24 PIN

CERAMIC DEVICES



All dimensions are inches.

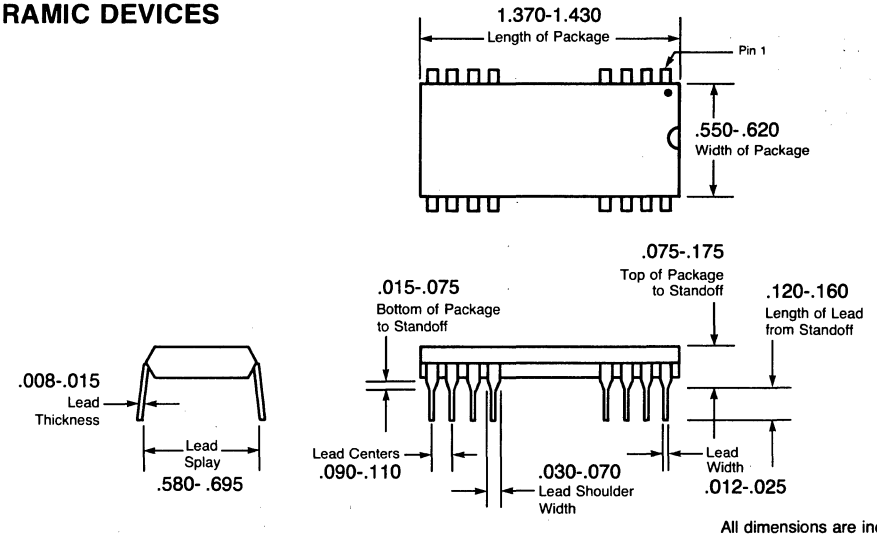
PLASTIC DEVICES



All dimensions are inches.

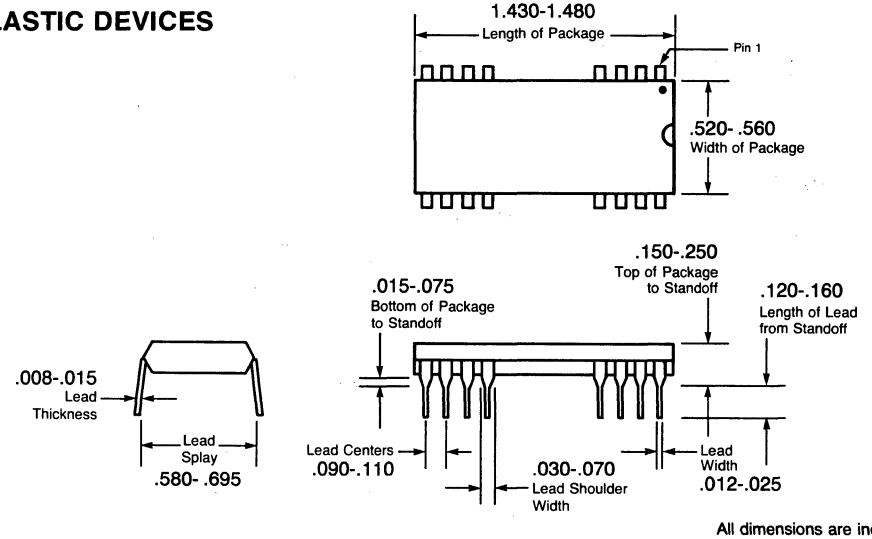
MECHANICAL DATA 28 Pin

CERAMIC DEVICES



All dimensions are inches.

PLASTIC DEVICES



All dimensions are inches.

NCR Microelectronics Division
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513/866-7217 Ohio or International

Electrically Erasable PROM

The NCR family of EEPROMs includes small organization serial devices for applications requiring a limited amount of storage capability. The NCR family also includes high density by eight devices for applications requiring maximum data storage. All members of the NCR EEPROM family are 5 volt only devices with all high erase/write voltages being generated on chip. This combination of high density and 5 volt only operation places NCR in the leadership position in EEPROMs. NCR EEPROMs are offered in commercial, industrial, and military temperature ranges.

PRODUCT SELECTION GUIDE

FUNCTION	PART NUMBER	ORGANIZATION	PAGE NUMBER
256 BIT EEPROM	NCR 52801	16 x 16	127
256 BIT EEPROM	NCR 59306	16 x 16	135
1K EEPROM	NCR 59308	64 x 16	143
32K EEPROM	NCR 52832	4K x 8	149
64K EEPROM	NCR 52864	8K x 8	157

CROSS REFERENCE LISTING

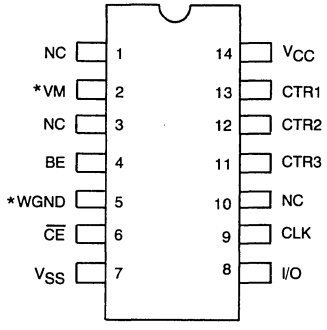
NCR PART NUMBER	EQUIVALENT	
NCR 52801	MOTOROLA	MCM 2801
NCR 59306	NATIONAL	NMC 9306
	GI	ER 59256
NCR 59308	NATIONAL	NMC 9346

52801
256-BIT (16 X 16) EEPROM

- **Electrically Erasable PROM**
- **Advanced SNOS N-Channel Technology**
- **5 Volt Only Operation**
- **In-System Reprogrammability**
- **Memory Margining Capability**
- **Fully TTL Compatible**
- **Serial I/O**
- **Unlimited Read Accesses**
- **125 kHz Maximum Clock Rate**

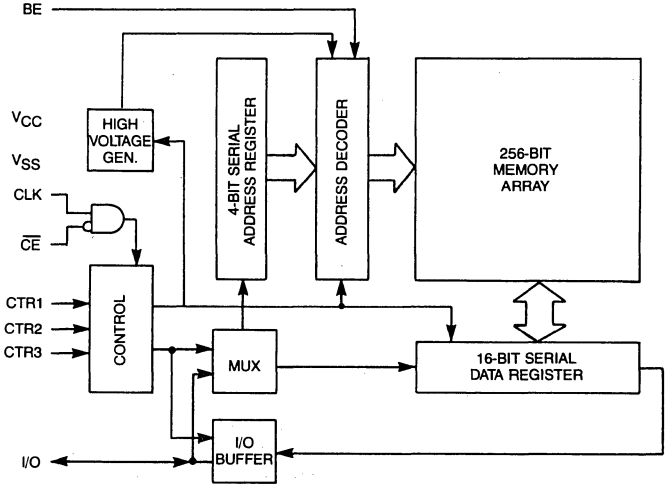
The NCR 52801 is a 256 bit Electrically Erasable PROM utilizing the Silicon-Nitride-Oxide-Silicon (SNOS) process developed by NCR. Designed for ease of use, the 52801 requires only a 5 volt source for all modes of operation. All voltages required for programming are generated internally by an on-chip bias generator, thus eliminating the need for external high voltage supplies. The timing of the 52801 is controlled totally by external TTL logic level signals. Address and data flow are in serial format through a common TTL compatible I/O port at a maximum clock rate of 125 kHz. Reprogramming the 52801 is basically a two step process, first erasing either a word or the entire block, and then writing a new word. The 52801 is available in a 14 pin package, in both commercial and industrial versions.

PIN CONFIGURATION



*Tie to V_{SS} for normal operation.

FUNCTIONAL BLOCK DIAGRAM



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DEVICE OPERATION

Data is stored in SNOS memory transistors by applying positive writing pulses that selectively tunnel charge into the nitride at the gate of the transistor. When the writing voltage is removed, the charge trapped in the nitride results in a positive shift in the threshold of the selected SNOS transistor. A negative bias across SNOS transistors reverses this process resulting in a negative shift in threshold for data erasure.

The memory stores sixteen words of sixteen bits each. All functions except the block erase are selected by a 3-bit parallel control code. The clock line is used to strobe these codes and to serially shift data and addresses.

READ CYCLE

Read-out is done in three steps. First, the 4-bit serial address is shifted in on the I/O Pin and into the address register while the Serial Address In code is applied to the three control pins. Next, the Read instruction is strobed in using one clock pulse. This will read the word from the location in the address register and place it into the data register. Finally, while applying the Serial Data Out code, data is shifted out with 16 clock pulses.

WRITE CYCLE

To write new data in, first the address must be changed if the location is different than that in the address register. Then, while applying the Serial Data In code, data is shifted into the data register with 16 clock cycles (unless data to be written is already in the register). Next, the Word Erase code is applied and, after erase time t_E min., the Write code is applied and held for at least t_W min.

When a Read mode immediately follows a Word Erase or Write mode (for the same memory location), one of two options must be used in order to ensure a valid Read operation:

Option 1: Maintain a Read mode (CTR3 = 0, CTR2 = 1, CTR1 = 1) for at least two clock cycles before implementing the Serial Data Out mode (1,1,0).

Option 2: Place the device in a Standby mode (0,0,0 or 1,1,1) for at least one clock cycle before implementing the Read mode (0,1,1).

BLOCK ERASE

The entire memory is erased when BE is held high for t_E min. To ensure a proper Block Erase, the clock should he held low for the entire erase cycle, and the mode of operation prior to the Block Erase should be either Standby (0,0,0 or 1,1,1), Read (0,1,1), Serial Data In (1,0,1) or Serial Address In (0,0,1). A t_{WAIT} time (defined as the negative edge of BE to the positive edge of the clock) of 8 μs must be observed if a Read mode is to immediately follow a Block Erase.

STANDBY

Both Standby codes produce the same results. The memory is placed in an inactive state, the I/O is in a high-impedance state and the clock will have no effect on the device.

PIN DESCRIPTION

CLK - The clock signal is active high, and used for shifting addresses and data into their respective registers and latching control signals.

I/O - The I/O pin is used for inputting data and addresses, and outputting data.

$\overline{CE}$ - Chip enable is active low, and when high will block the clock signal and put the I/O pin into a high-impedance state. It should be noted that when $\overline{CE}$ is high, the device is not automatically placed into a standby mode.

BE - Block erase is active high and used to clear the entire memory. To accomplish block erase, the BE Pin must be held high for t_E. This pin can be tied to V_{SS} during normal operation.

MEMORY MARGINING

The NCR 52801 supports margining of the memory transistors. Memory margining allows device retention time to be projected for the purpose of device evaluation. An application note describing the memory margining algorithm is available.

COMMENTS

- The device should not be in the programming mode (i.e. Erase or Write) during power-up or power-down.
- Erased state results in logical zero at I/O during data output.
- In order to protect data during power-up or power-down, one of the following conditions must exist:
  - — CS held high — Control Lines held low
  - — CLK held low — Control Lines held high

MODE SELECTION

Mode	CTR3	CTR2	CTR1
Standby	1	1	1
Word Erase	1	0	0
Write	0	1	0
Serial Data Out	1	1	0
Serial Address In	0	0	1
Serial Data In	1	0	1
Read	0	1	1
Standby	0	0	0

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin
Relative to V_{SS} . . . . . +8 to −0.5V
Storage Temperature (Without
Data Retention) . . . . . −65 to +150°C

Stress above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operational limits stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

		52801			52801I			Units
Symbol	Parameter	Min	Typ.	Max.	Min.	Typ.	Max.	
V_{CC}	Supply Voltage.(See NOTE 1)	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.0		V_{CC} + 1	2.0		V_{CC} + 1	V
V_{IL}	Input Low Voltage	−0.1		0.8	−0.1		0.8	V
T_A	Ambient Temperature	0		70	−40		85	°C

NOTE 1. V_{CC} must be applied at least 100μs before proper operation is achieved.

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

			52801			52801I			Units
Symbol	Parameter	Condition	Min	Typ.	Max.	Min.	Typ.	Max.	
I_{IN}	Input Current	V_{in} = 0 TO V_{CC}			10			10	μA
I_{CC}	V_{CC} Supply Current	V_{CC} = 5.5V			15			20	mA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA			0.4			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −0.1 mA	2.4			2.4			V
T_S	Non-Volatile Data Storage Time	Following Min. Erase and Write Timings, $N_{EW} \leq 10^4$ Cycles	10			10			Yr.

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

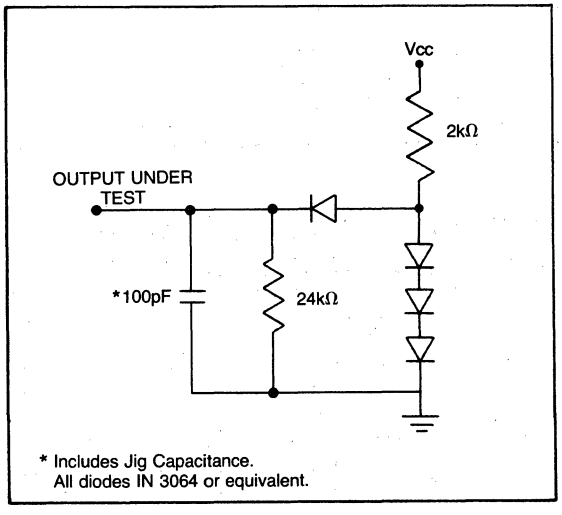
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_E	Erase Time	100			ms
t_W	Write Time	10		50	ms
t_{CHCL}	Clock High Level Hold Time	4		10	μs
t_{CLCH}	Clock Low Level Hold Time	4			μs
t_R	Clock Rise Time	5		1000	ns
t_F	Clock Fall Time	5		1000	ns
t_{SLCH}	Chip Select Setup	1			μs
t_{CLSH}	Chip Select Hold	1			μs
t_{CHQV}	Data Out Delay			1	μs
t_{AVCL}	Address In Setup	1			μs
t_{DVCL}	Data In Setup	1			μs
t_{CLDX}	Data In Hold	200			ns
t_{CTRVCH}	Control Setup	1			μs
t_{CTRX}	Control Hold	50			ns
t_{CHQZ}	Data Off Time From Clock			3	μs
t_{SLQX}	Chip Select Low to Output Active			2	μs
t_{SHQZ}	Chip Select High to Output Inactive			2	μs
$N_{E/W}$	Number of Erase/Write Cycles (See NOTE 2)			10^4	cycles

NOTE 2. The specified maximum of 10^4 cycles will ensure a T_S min. of 10 years, increasing $N_{E/W}$ beyond 10^4 cycles will degrade T_S logarithmically.

A.C. TEST CONDITIONS

Input Timing Levels: 0.8 Volts and 2.0 Volts
Output Timing Levels: 0.8 Volts and 2.0 Volts
Input Rise and Fall Times (except Clock): 20 ns
Input Pulse Levels: 0.45 Volts and 2.4 Volts

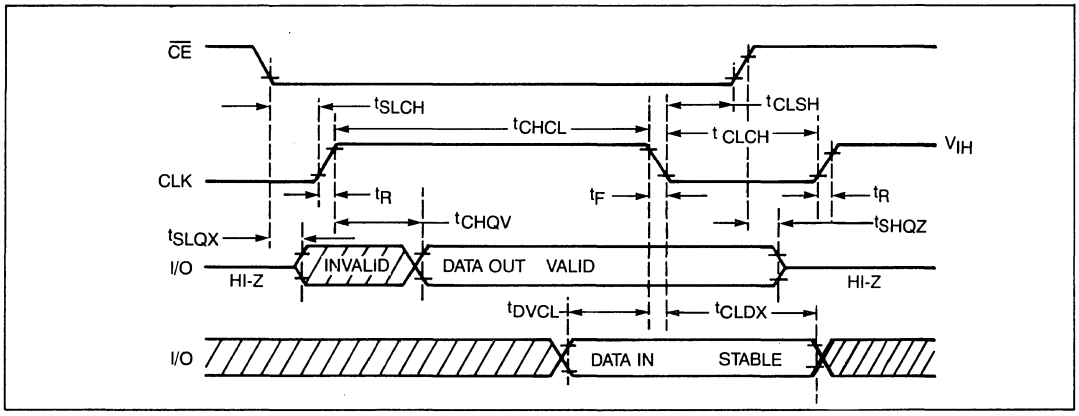
TEST LOAD CIRCUIT



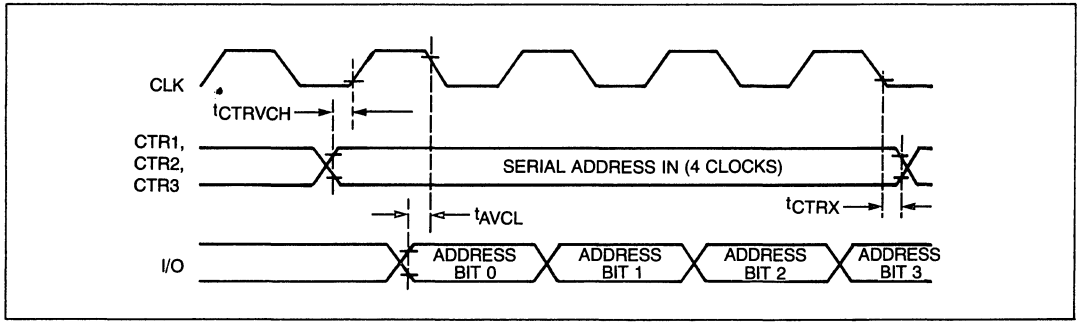
* Includes Jig Capacitance.
All diodes IN 3064 or equivalent.

WAVE FORMS

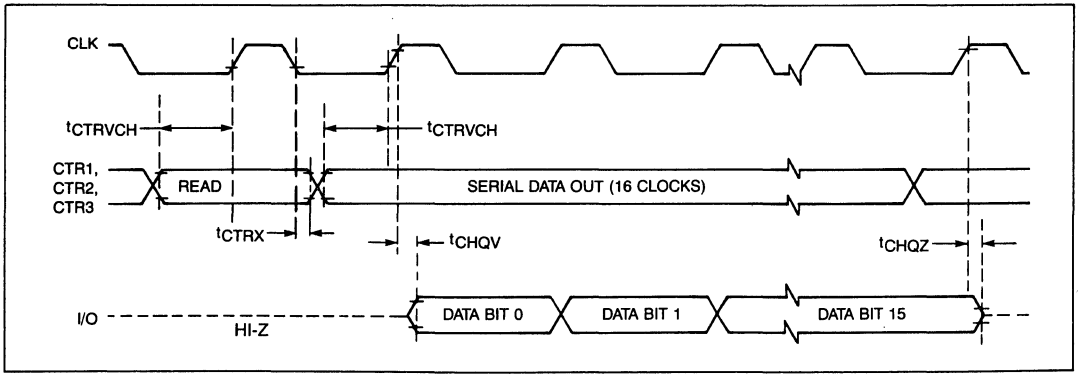
CLOCK CYCLE DETAIL



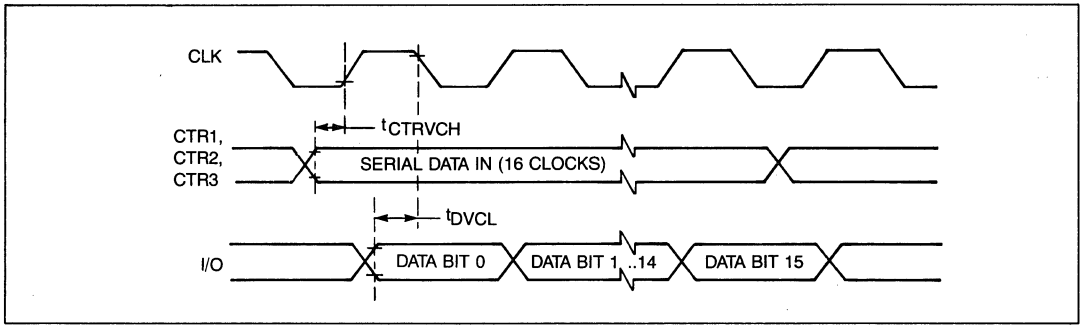
SERIAL ADDRESS IN



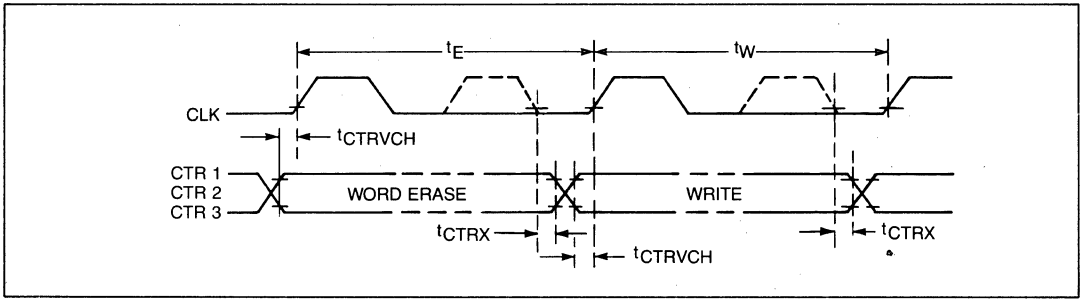
READ AND SERIAL DATA OUT



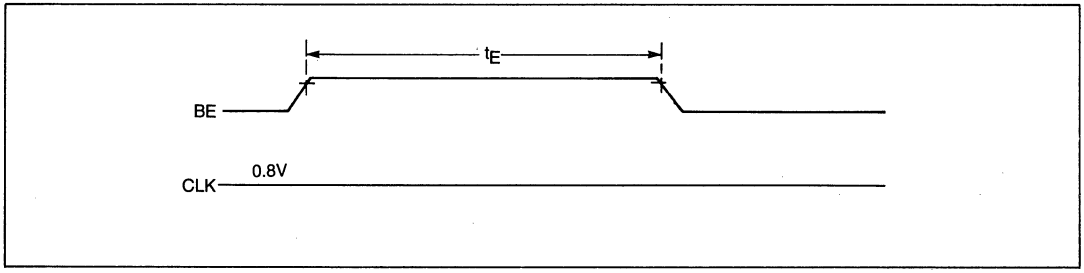
SERIAL DATA IN



ERASE WRITE SEQUENCE

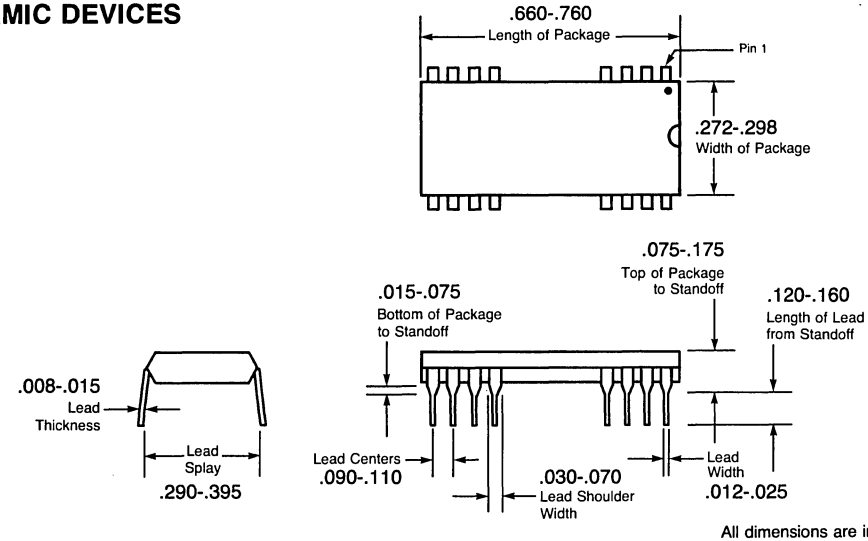


BLOCK ERASE



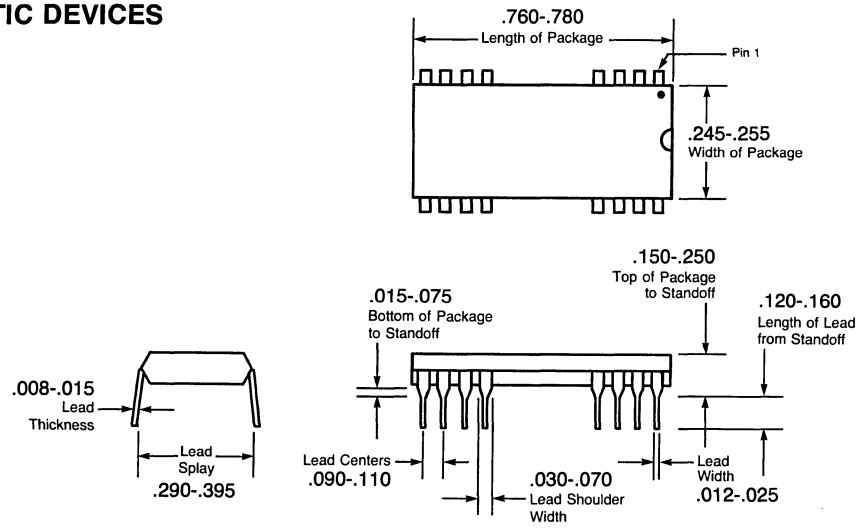
MECHANICAL DATA 14 Pin

CERAMIC DEVICES



All dimensions are inches.

PLASTIC DEVICES



All dimensions are inches.

NCR

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513/866-7217 Ohio or International

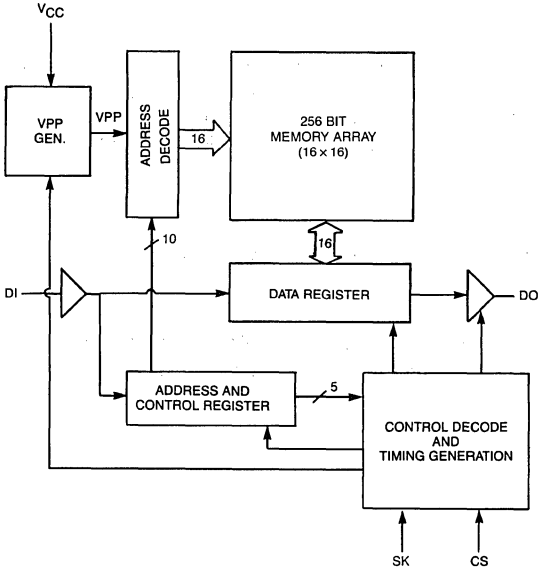
59306
256 Bit (16 x 16) EEPROM

PRELIMINARY

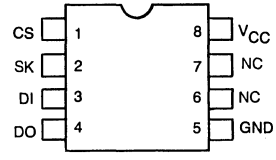
- Electrically Erasable PROM
- Non-Volatile Erase and Write
- Self Timed Erase and Write
- In-System Reprogrammability
- 5 Volt Only Operation (± 10%)
- Serial I/O and Control
- Advanced SNOS N-Channel Technology
- Compatible with COP 400 processors
- Fully TTL Compatible
- Low Power Standby Mode

The NCR 59306 is a 256 bit (16 × 16) serial access Electrically Erasable PROM (EEPROM) fabricated in the Silicon-Nitride-Oxide-Silicon (SNOS) process developed by NCR. The 59306 requires only a 5 volt source for all modes of operation. An on-chip voltage generator produces all voltages required for programming. The Erase and Write operations are self-timed and after the command is initiated, the system controller is free to perform other functions. Additionally the ready/busy status of the erase/write operations may be polled on the serial data out pin (DO). Control, address, and data are input in a serial format through the serial data input pin. The read data is output in serial format through the serial data output pin. The NCR 59306 is available in an 8 pin dual-in-line package.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

CS	CHIP SELECT
SK	SERIAL DATA CLOCK
DI	SERIAL DATA INPUT
DO	SERIAL DATA OUTPUT
GND	GROUND
V_{CC}	POWER SUPPLY
NC	NO CONNECTION

This is advance information and NCR reserves the right to change the specifications without notice.

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FUNCTIONAL DESCRIPTION

The NCR 59306 is organized as 16 words of 16 bits each. Control, address, and data are input serially through the serial data input pin (DI) and are latched on the rising edge of the clock (SK). Read data is output serially through serial data output pin (DO) propagating from the rising edge of the clock. The NCR 59306 supports four instructions—READ, WRITE, ERASE, and ERAL. Each instruction consists of nine (9) bits—a start bit, followed by four(4) operation code bits, followed by four (4) address bits. The nine bits are clocked serially into the instruction shift register (ISR). When the start bit reaches the end of the ISR, further shifting of data into the ISR is inhibited. The write and erase instructions are initiated by the falling edge of the chip select. The NCR 59306 automatically times out the erase and write instructions during which any shifting of the ISR and Data Shift Register (DSR) is inhibited. The status of the time-out may be polled on the serial data out pin (DO). The ISR is cleared on the completion of an erase or write time-out or on the falling edge of CS after a read cycle. Both the ISR and DSR are cleared on power up. DO is only in the high impedance state when the chip is deselected. In all cycles, except when reading data, DO is driven high when the device is ready to accept another command or low when executing an E/W time-out. DO outputs read data after a read cycle is decoded. Prior to executing any of the four commands. the CS must cycle to the low state before the new instruction and address are loaded.

READ

When the start bit reaches the end of the ISR and a Read command is decoded, a read pulse is generated which loads 16 data bits from the selected row of the memory into the DSR in parallel. During this read pulse the output is driven low generating a Dummy Read Bit (DRB). On the following clock cycle, read data is serially shifted out propagating from the rising edge of the clock. The ISR is cleared after a read when the chip select is low thus preparing the chip to accept another command.

ERASE

A word must be erased (set to all ones) before data can be written into the memory. When an Erase command is clocked into the ISR, the erase is not initiated until the chip select goes low. From the falling edge of the chip select the 59306 times out the Erase command freeing all control of the device. However, status of the device may be polled through the DO pin. During the erase time out, shifting of data into the device is inhibited. For an Erase, only the selected word is erased and all other words are left undisturbed.

ERAL

ERAL operates in the same manner as an Erase except all words are erased (set to all ones).

WRITE

After a Write command is shifted into the ISR, 16 data bits must be shifted into the DSR. The Write command is initiated on the falling edge of the chip select and is automatically timed out on chip. The status of the write may be polled on the DO pin by selecting the chip.

INSTRUCTION SET

INSTRUCTION	SB	OP CODE	ADDRESS	DATA IN	DRB	DATA OUT
ERAL	1	0010	XXXX*	NA	NA	1
ERASE	1	1100	A3-A0	NA	NA	1
WRITE	1	0100	A3-A0	D15-D0	NA	1
READ	1	1000	A3-A0	NA	0	D15-D0

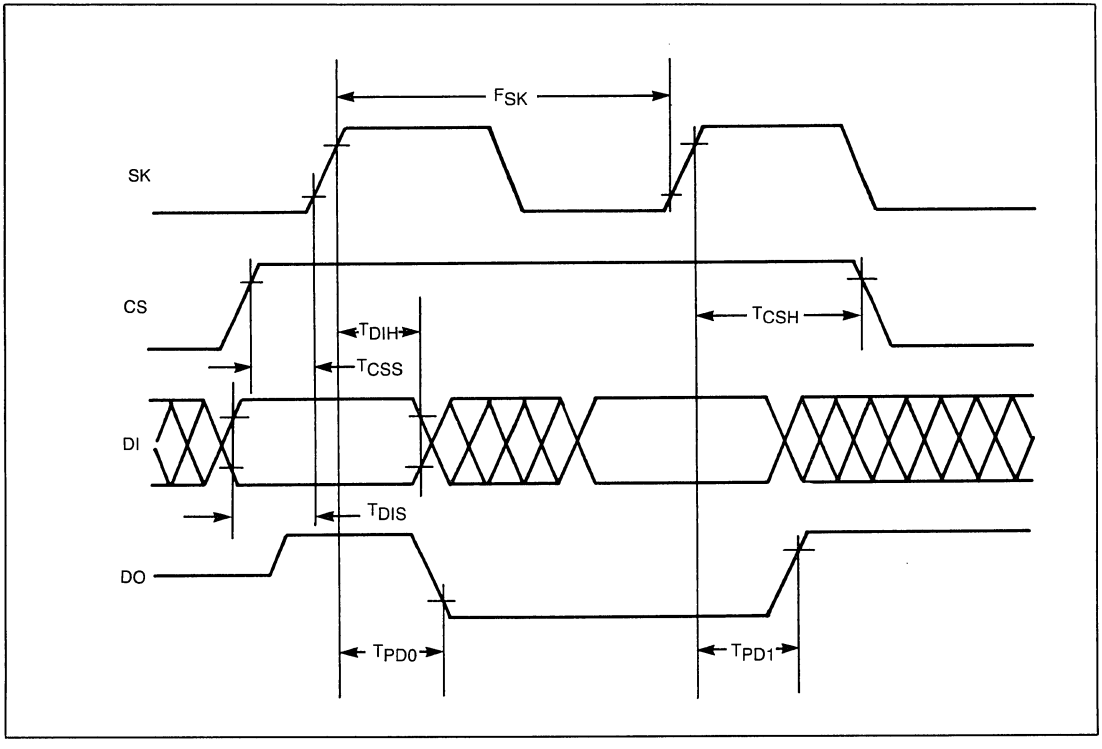
*X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Voltage Relative to Ground . . . . . +6V to −0.3V
Storage Temperature
(without data retention). . . . . −65°C to 150°C
Lead Temperature (Soldering, 10 sec.). . . . . .300°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operating conditions stipulated elsewhere in this specification is not implied.

TIMING DETAIL



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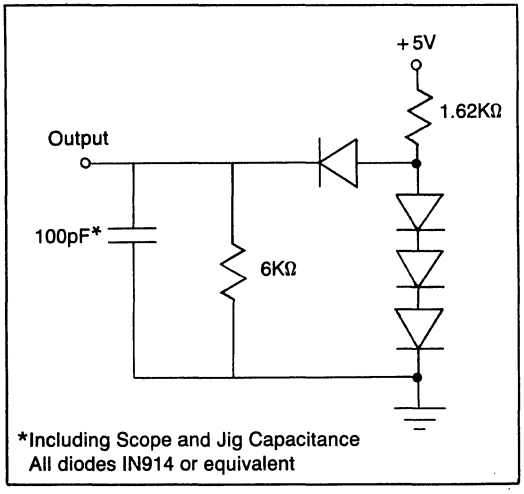
ELECTRICAL CHARACTERSTICS
(0°C to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage		4.5	5.0	5.5	V
I_{CC1}	Operating Current	CS = 1 V_{CC} = 5.5V			10	mA
I_{CC2}	Standby Current	CS = 0 V_{CC} = 5.5V			5	mA
I_{CC3}	E/W Operating Current	V_{CC} = 5.5V			12	mA
V_{IL}	Input Low Level		-0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -0.4mA	2.4			V
I_{IN}	Input Leakage Current	V_{IN} = 5.5V			10	μA
I_{OUT}	Output Leakage Current	CS = 0 V_{OUT} = 5.5V			10	μA
F_{SK}	SK Frequency		0.0		250	kHz
D_{SK}	SK Duty Cycle		25		75	%
T_{CSS}	Select Set-up Time		0.2			μs
T_{CSH}	Select Hold Time		1.0			μs
T_{DIS}	Data Set-up Time		0.4			μs
T_{DIH}	Data Hold Time		0.4			μs
T_{PD0}	Output Low Delay from Clock	CL = 100 pF V_{OL} = 0.8V, V_{OH} = 2.0V			2.0	μs
T_{PD1}	Output High Delay from Clock	CL = 100 pF V_{OL} = 0.8V, V_{OH} = 2.0V			2.0	μs
$T_{E/W}$	Erase/Write Time				20	ms

CAPACITANCE
(f = 1.0MHz, T_A = 25°C, V_{CC} = 5.0V, V_{IN} = 0V)

			59306			59306I			
Symbol	Parameter	Condition	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V			10			10	pF
C_O	Output Capacitance	$\overline{OE}$ = $\overline{CE}$ = V_{IH}			12			12	pF

TEST LOAD CIRCUIT



*Including Scope and Jig Capacitance
All diodes IN914 or equivalent

A.C. CONDITION OF TESTS

Input Pulse Levels . . . . . .0.8 Volts to 2.0 Volts
Inputs Rise & Fall Times . . . . . .10 ns
Output Timing Levels . . . . . .0.4 Volts to 2.4 Volts

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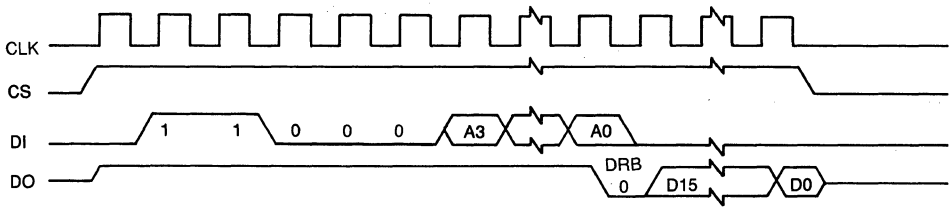
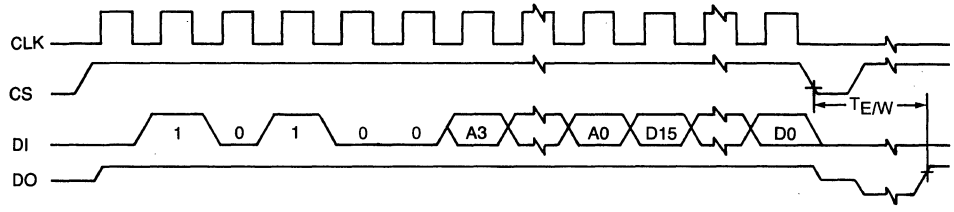
TIMING DIAGRAMS

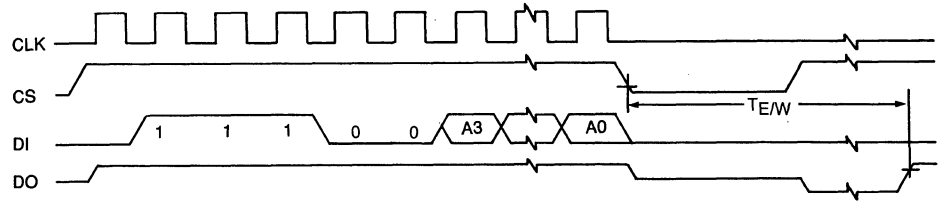
READ



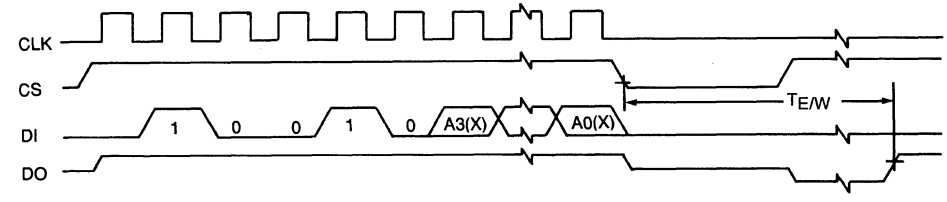
WRITE



ERASE

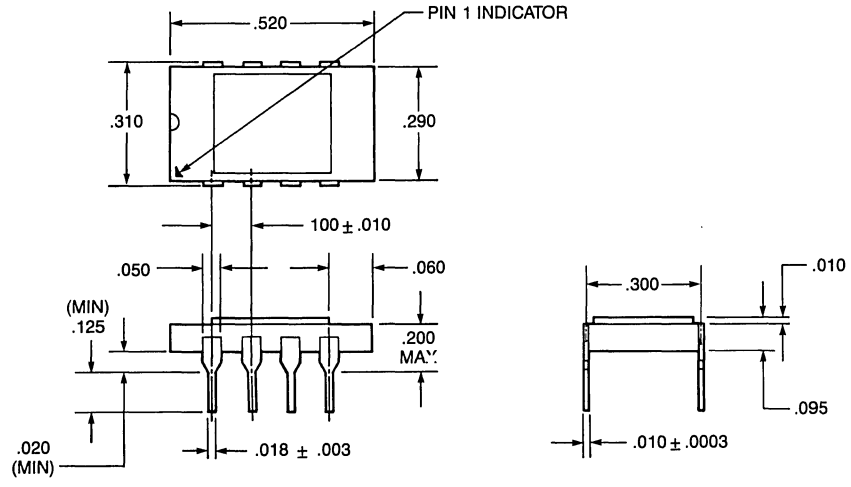


ERAL

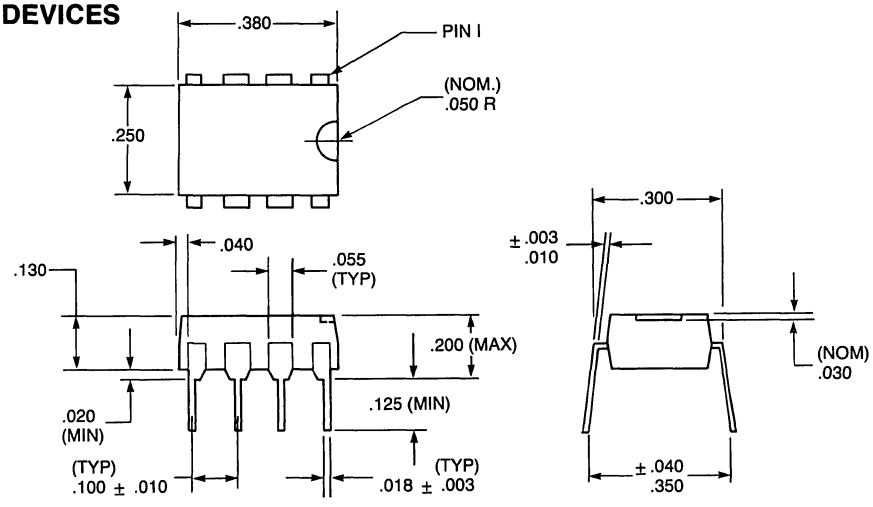


MECHANICAL DATA 8 PIN

CERAMIC DEVICES



PLASTIC DEVICES



Notes: Unless otherwise specified, tolerance = .005.
All dimensions are inches.

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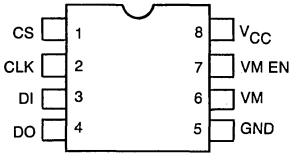
513/866-7217 Ohio or International

59308
1024 Bit (64x16) EEPROM

- Electrically Erasable PROM
- Advanced SNOS N-Channel Technology
- 5 Volt Only Operation
- In-System Reprogrammability
- Ready/Busy Indication thru DO
- Fully TTL Compatible
- Serial I/O and Control
- Self Timed Erase and Write
- 500 kHz Clock Rate
- Low Power Standby Mode

The NCR 59308 is a 1024 bit (64x16) serial access Electrically Erasable PROM (EEPROM) fabricated in the Silicon-Nitride-Oxide Silicon (SNOS) process developed by NCR. The 59308 requires only a 5 volt source for all modes of operation. An on-chip voltage generator produces all voltages required for programming. The Erase and Write operations are self-timed and after the command is initiated, the system controller is free to perform other functions. Additionally, the ready/busy status of the erase/write operations may be polled on the serial data out pin (DO). Control, address, and data are input in a serial format through the serial data input pin. The read data is output in a serial format through the serial data output pin. The NCR 59308 is available in an 8 pin dual-in-line package in commercial and industrial versions.

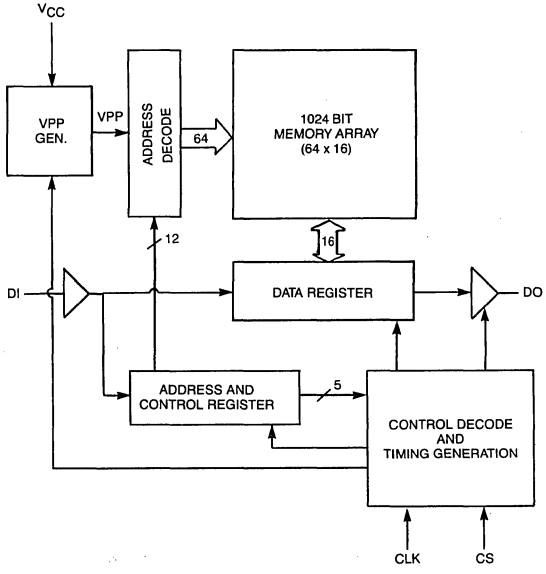
PIN CONFIGURATION



PIN NAMES

CS	CHIP SELECT
CLK	SERIAL DATA CLOCK
DI	SERIAL DATA INPUT
DO	SERIAL DATA OUTPUT
GND	GROUND
VM	MARGINING VOLTAGE
VM EN	MARGINING ENABLE
V_{CC}	POWER SUPPLY

FUNCTIONAL BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

The NCR 59308 is organized as 64 words of 16 bits each. Control, address, and data are input serially through the serial data input pin (DI) on the rising edge of the clock (CLK). Read data is output serially through serial data outut pin (DO) on the rising edge of the clock. The NCR 59308 supports four instructions — Read, Write, Word Erase, and Chip Erase. Each instruction consists of nine (9) bits — a start bit, followed by two (2) operation code bits, followed by six (6) address bits. The nine bits are clocked serially into the instruction shift register (ISR). When the start bit reaches the end of the ISR, further shifting of data into the ISR is inhibited. The Write and Erase instructions are initiated by the falling edge of the chip select. The NCR 59308 automatically times out the Erase and Write instructions during which any shifting of the ISR and Data Shift Register (DSR) is inhibited. The status of the time out may be polled on the serial data out pin (DO). When the chip select is brought high, a low state on the DO pin indicates that the chip is busy performing the erase or write, a high state indicates the chip is not busy and is ready to receive another instruction.The output is in a high impedance state only when the chip is deselected.Prior to executing any of the four commands,the CS must cycle to the low state before the new instruction and address are loaded.

READ

When the start bit reaches the end of the ISR and a Read command is decoded, a read pulse is generated which loads 16 data bits from the selected row of the memory into the DSR in parallel. During this read pulse the output is driven low generating a Dummy Read Bit(DRB).On the following clock cycle, read data is serially shifted out propagating from the rising edge of the clock.The ISR is cleared after a read when the chip select is low thus preparing the chip to accept another command.

WRITE

After a Write command is shifted into the ISR, 16 data bits must be shifted into the DSR. The Write command is initiated on the falling edge of the chip select and is automatically timed out on chip. The status of the write may be polled on the DO pin by selecting the chip — a low indicates the device is busy, a high indicates the device is ready to accept another command.

WORD ERASE

A word must be erased (set to all ones) before data can be written into the memory. When a Word Erase command is clocked into the ISR, the erase is not initiated until the chip select goes low. From the falling edge of the chip select the 59308 times out the Erase command freeing all control of the device. During the erase time out, shifting of data into the device is inhibited. However, status of the device may be polled through the DO pin. When the chip select is high, a low signal on the DO pin indicates the device is "busy", a high signal indicates the device is "not busy" and is ready to receive another command. For a Word Erase, only the selected word is erased and all other words are left undisturbed.

CHIP ERASE

A Chip Erase operates in the same manner as a Word Erase except all words are erased (set to all ones).

MEMORY MARGINING

The NCR 59308 supports margining of the memory transistors. Memory margining allows device retention time to be projected for the purpose of device evaluation. An application note describing the memory margining procedure is available.

INSTRUCTION SET

INSTRUCTION	SB	OP CODE	ADDRESS	DATA IN	DRB	DATA OUT
Chip Erase	1	00	10XXXX*	NA	NA	1
Word Erase	1	11	A5-A0	NA	NA	1
Write	1	01	A5-A0	D15-D0	NA	1
Read	1	10	A5-A0	NA	0	D15-D0

*X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Voltage Relative to Ground . . . . . +6V to –0.3V
Storage Temperature
(without data retention). . . . . –65°C to 150°
Lead Temperature (Soldering, 10 sec.) . . . . . 300°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operating conditions stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS
(Over full operating voltage and temperature range unless specified otherwise.)

		59308			59308I			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IL}	Input Low Level	–0.1		0.8	–0.1		0.8	V
V_{IH}	Input High Level	2.0		$V_{CC}+1$	2.0		$V_{CC}+1$	V
T_A	Ambient Temperature	0		70	–40		85	°C

NCR

OPERATING DC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (Unless otherwise noted)

Symbol	Parameter	Condition	59308			59308I			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IN}	Input Leakage Current	$0 \le V_{IN} < V_{CC}$			10			10	μA
I_{OUT}	Output Leakage Current	CS = 0 $0 \le V_{OUT} \le V_{CC}$			10			10	μA
$I_{CC}1$	Operating Current	CS = 1 V_{CC} = 5.5V			12			15	mA
$I_{CC}2$	Standby Current	CS = 0 V_{CC} = 5.5V			5			5	mA
$I_{CC}3$	E/W Operating Current	V_{CC} = 5.5V			15			20	mA
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			0.4			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −0.4mA	2.4			2.4			V

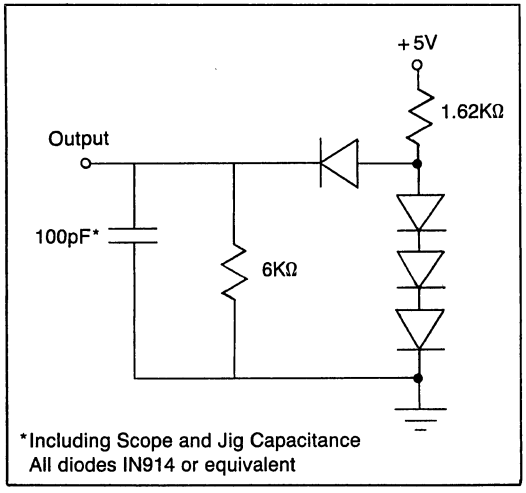
CAPACITANCE
($f = 1.0MHz$, $T_A = 25°C$, $V_{CC} = 5.0V$, $V_{IN} = 0V$)

Symbol	Parameter	Condition	59308			59308I			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
C_{IN}	Input Capacitance	All Pins At			10			10	pF
C_O	Output Capacitance	V_{SS} (Ground)			12			12	pF

AC CHARACTERISTICS
(Over recommended operating conditions)

Symbol	Parameter	59308			59308I			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{CHCL}	Clock High Time	1.0			1.0			μ sec.
t_{CLCH}	Clock Low Time	1.0			1.0			μ sec.
t_{SHCH}	Select Set-up Time	0.2			0.2			μ sec.
t_{CHSL}	Select Hold Time	1.0			1.0			μ sec.
t_{SLSH}	Select Low Time	0.5			0.5			μ sec.
t_{DVCH}	Data Set-Up Time	0.4			0.4			μ sec.
t_{CHDX}	Data Hold Time	0.4			0.4			μ sec.
t_{SHQV}	Output Delay from Select			1.0			1.0	μ sec.
t_{CHQV}	Output Delay from Clock			1.0			1.0	μ sec.
t_{SLQZ}	Output Inactive from Select			1.0			1.0	μ sec.
t_R	Clock Rise Time			0.5			0.5	μ sec.
t_F	Clock Fall Time			0.5			0.5	μ sec.
t_E	Erase Time			20			20	ms
t_W	Write Time			20			20	ms
t_S	Non-Volatile Data Storage	10			10			years
N_{EW}	Number of Erase/Write Cycles	10^4			10^4			cycles

TEST LOAD CIRCUIT

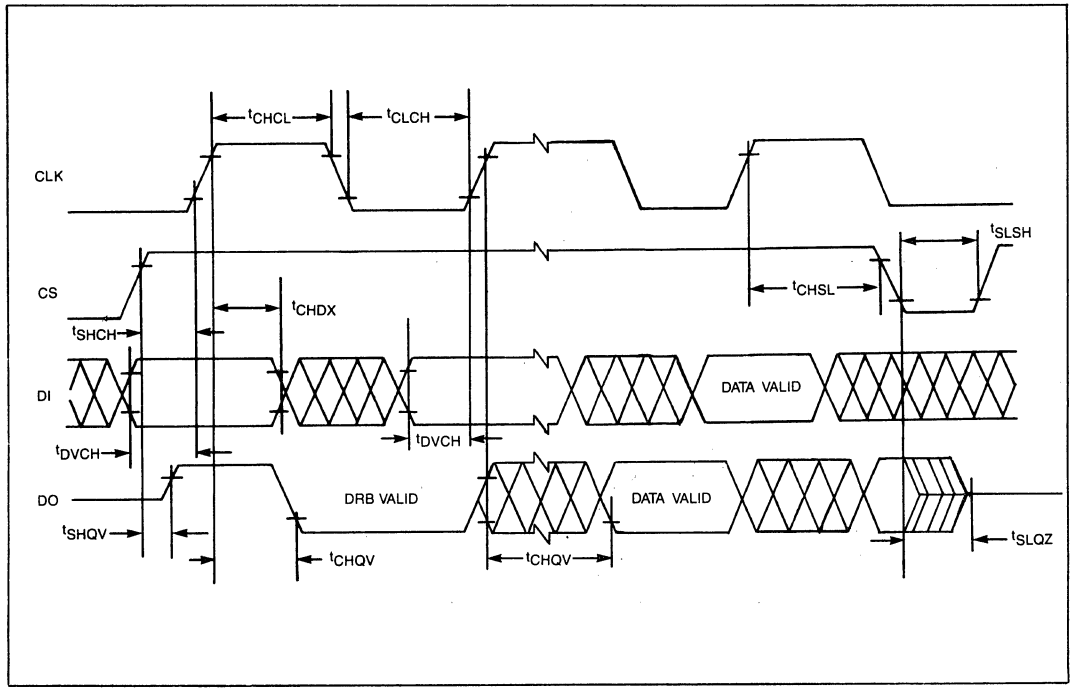


*Including Scope and Jig Capacitance
All diodes IN914 or equivalent

A.C. CONDITION OF TESTS

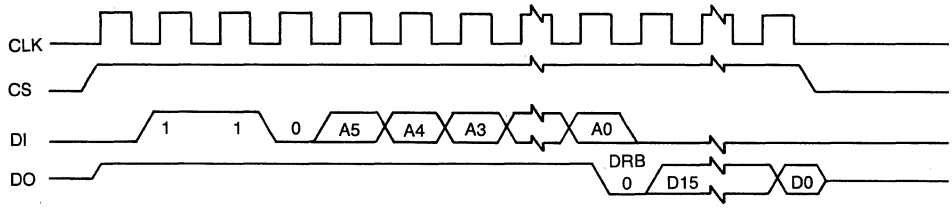
Input Pulse Levels . . . . . .0.8 Volts to 2.0 Volts
Inputs Rise & Fall Times . . . . . .10 ns
Output Timing Levels . . . . . .0.4 Volts to 2.4 Volts

TIMING DETAIL

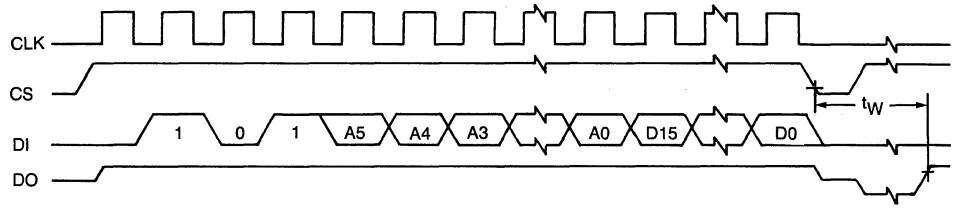


TIMING DIAGRAMS

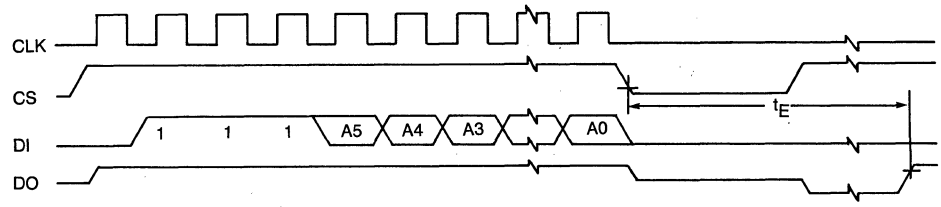
READ



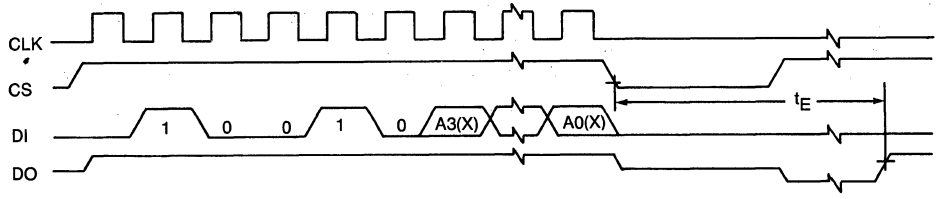
WRITE



WORD ERASE

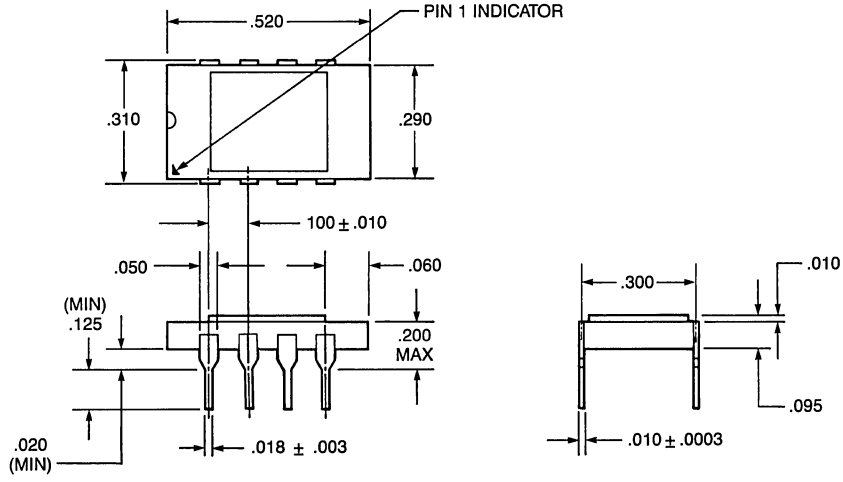


CHIP ERASE

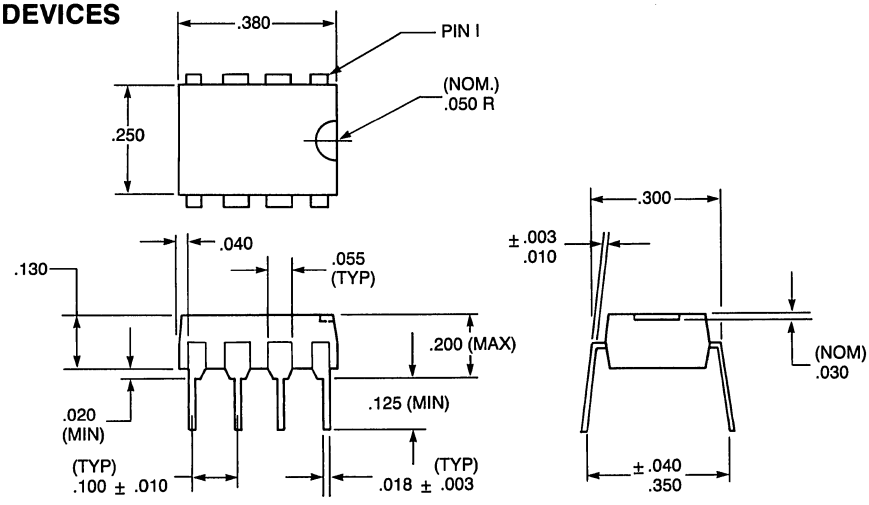


MECHANICAL DATA 8 PIN

CERAMIC DEVICES



PLASTIC DEVICES



Note: Unless otherwise specified tolerance is ± .005
All dimensions are inches.

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513/866-7217 Ohio or International

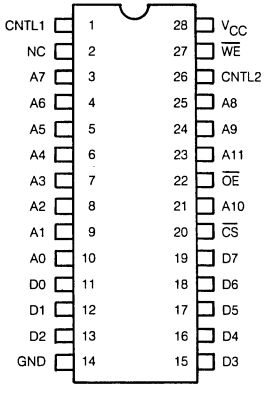
52832
32K (4Kx8) EEPROM

- **Electrically Erasable PROM**
- **Advanced SNOS N-Channel Technology**
- **300 ns Access Times**
- **Low Power Dissipation**
- **Memory Margining**
- **5 Volt Only Operation**
- **In-System Reprogrammability**
- **3-State Outputs**
- **Latched Address & Data Bus**
- **28 Pin DIP With Industry Standard Byte-Wide Pinout**
- **Optional 32 Pin LCC Available**
- **Page Alterable**

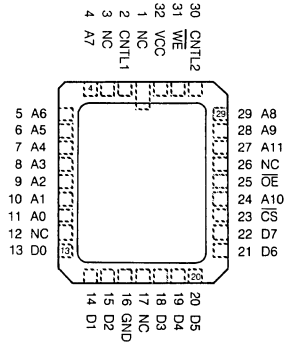
The NCR 52832 is a 32K bit (4Kx8) Electrically Erasable PROM utilizing the Silicon-Nitride-Oxide-Silicon (SNOS) process developed by NCR. Designed for ease-of-use, the 52832 requires only a 5 volt source for all modes of operation. All voltages required for programming are generated internally by an on-chip voltage generator, thus eliminating the need for any external high voltage supplies. The 52832 also provides on-board latching of addresses and data lines during non-volatile operations. The 52832 allows memory margining in order to predict the data retention time. All control line inputs, as well as the address inputs and data I/O's, are TTL compatible. This feature, combined with access times of 300 ns and a byte-wide industry standard pinout makes the 52832 highly compatible with existing microprocessors. Erasing the 52832 is accomplished in either a chip or page fashion. Writing the device can be performed either word by word or, in applications requiring fast system reprogramming, by a contiguous page of 16 words. The NCR 52832 is available in a 28 pin DIP in commercial, industrial and high reliability versions. Optionally, the NCR 52832 can be packaged in a 32 pin leadless chip carrier (LCC).

PIN CONFIGURATION

28 PIN DIP

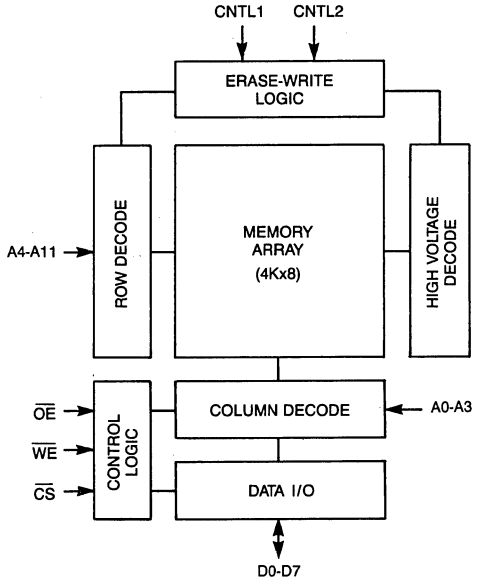


32 PIN LCC



(Top View)

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A0-A11	Address Inputs	$\overline{WE}$	Write Enable
D0-D7	Data I/O	$\overline{OE}$	Output Enable
CNTL 1 & CNTL 2	Control Lines	NC	No Connection
$\overline{CS}$	Chip Select	V_{CC}	+5 Volt ± 10% Supply Voltage

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DEVICE OPERATION

READ MODE

The 52832 is read like a conventional static RAM. Valid data is available on the output pins when a valid address is provided and $\overline{CS}$ and $\overline{OE}$ are brought low. If the address lines change while $\overline{CS}$ and $\overline{OE}$ are maintained low, valid data will be available after a delay of t_{ACC}.

CHIP ERASE MODE

Chip erase is accomplished by holding CNTL1 high and CNTL2 low followed by bringing $\overline{CS}$ and $\overline{OE}$ low. During chip erase all data and address lines are "don't care". An erased state corresponds to a logical "0".

PAGE ERASE MODE

Page (16 bytes) erase is accomplished in a manner similar to chip erase except that $\overline{OE}$ is held high and $\overline{WE}$ is brought low, and a page address (A_4-A_{11}) must be provided. As in chip erase, the data lines are "don't care" and the erased state corresponds to a logical "0".

LOAD DATA MODE

During the load data mode, data is loaded into 16, 8 bit internal latches. In this mode, data is loaded much the same way as it is for a SRAM. Both CNTL lines are held low while "clocking" $\overline{CS}$ and $\overline{WE}$. Addresses and data must be valid while $\overline{CS}$ and $\overline{WE}$ are low. The load data mode must be followed by a write mode to prevent losing the data that has been loaded in. Data may be loaded and then written 1 to 16 bytes at a time.

WRITE MODE

Data can be written into non-volatile cells by holding CNTL2 high and maintaining CNTL1 low while $\overline{CS}$ and $\overline{WE}$ are brought low. Data and address lines are "don't care" during a write cycle. A written state corresponds to a logical "1".

MEMORY MARGINING

The NCR 52832 supports margining of the memory transistors. Memory margining allows device retention time to be projected for the purpose of device evaluation. An application note describing the memory margining algorithm is available.

MODE SELECTION

MODE	$\overline{OE}$	$\overline{WE}$	CNTL1	CNTL2	$\overline{CS}$
Standby	X	X	H	H	H
Read	L	H	H	H	L
Chip Erase	L	H	H	L	L
Page Erase	H	L	H	L	L
Load Data	H	L	L	L	L
Write	H	L	L	H	L

ABSOLUTE MAXIMUM RATINGS

Voltage On Any Pin With
Respect to GND ..... -0.5 to +7V
Voltage on CNTL1 and CNTL2
(During Memory Margining Only)..... -6V to +22V
Storage Temperature ..... -65°C to 150°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operational limits stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	52832			52832I			52832HR			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	Input High-Level Voltage	2		$V_{CC}+1$	2		$V_{CC}+1$	2		$V_{CC}+1$	V
V_{IL}	Input Low-Level Voltage	-0.3		0.8	-0.3		0.8	-0.3		0.8	V
T_A	Ambient Temperature	0		70	-40		85	-55		125	°C

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (Unless Otherwise Noted)

Symbol	Parameter	Conditions	52832			52832I			52832HR			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{IN}	Input Leakage Current	V_{IN} = 0V to 5.5V			10			10			10	μA
I_O	I/O Leakage Current	CS = V_{IH} V_O = 0V to 5.5V			10			10			10	μA
I_{CC}	Supply Current	Outputs Open, CS = V_{IL} CS = V_{IH}			60 30			60 30			60 30	mA mA
V_{OH}	Output High-Level Voltage	I_{OH} = —400μA	2.4			2.4			2.4			V
V_{OL}	Output Low-Level Voltage	I_{OL} = 2.1mA			0.4			0.4			0.4	V
T_S	Non-Volatile Data Storage	Following Minimum Erase/Write Cond.	10			10			10			Yr

NCR

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

READ CYCLE

Symbol	Parameter	52832			52832I			52832HR			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{ACC}	Address Access Time			300			450			450	ns
t_{CS}	Chip Select Access Time			300			450			450	ns
t_{OE}	Output Enable Access Time			150			150			150	ns
t_{OZ}	Output Enable Or Chip Select to Output High Impedance			90			115			115	ns
t_{SC}	Control Setup Time										
	• After Erase or Write	50			50			50			µs
	• After Load or Read	500			500			500			ns
t_{CH}	Control Hold Time	0			0			0			ns

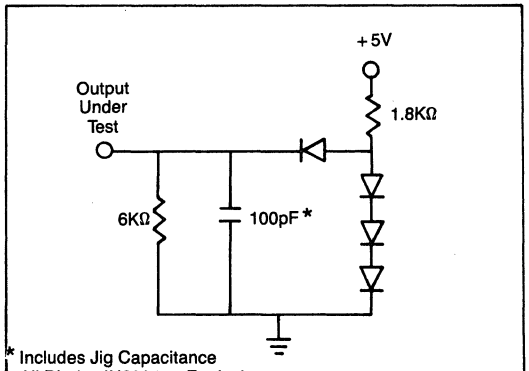
ERASE/LOAD/WRITE CYCLE

Symbol	Parameter	52832			52832I			52832HR			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_E	Erase Time	100		200	100		200	100		200	ms
t_W	Write Time	10		20	10		20	10		20	ms
t_{SC}	Control Setup Time										
	• After Erase or Write	50			50			50			µs
	• After Load or Read	500			500			500			ns
t_{CSS}	Chip Select Setup Time	0			0			0			ns
t_{CSH}	Chip Select Hold Time	0			0			0			ns
t_{AS}	Address or Data Setup Time	0			0			0			ns
t_{AH}	Address or Data Hold Time	0			0			0			ns
t_{OEL}	Output Enable Pulse Width	200			200			200			ns
t_{WEL}	Write Enable Pulse Width	200			200			200			ns
t_{WEH}	Write Enable Recovery Time	100			100			100			ns
t_{DW}	Data to Write Time Overlap	200			200			200			ns
t_{DH}	Data Hold Time	0			0			0			ns
$N_{E/W}$	Number of Erase/Write Cycles	10^4			10^4			10^4			Cycles

A. C. CONDITIONS OF TESTS

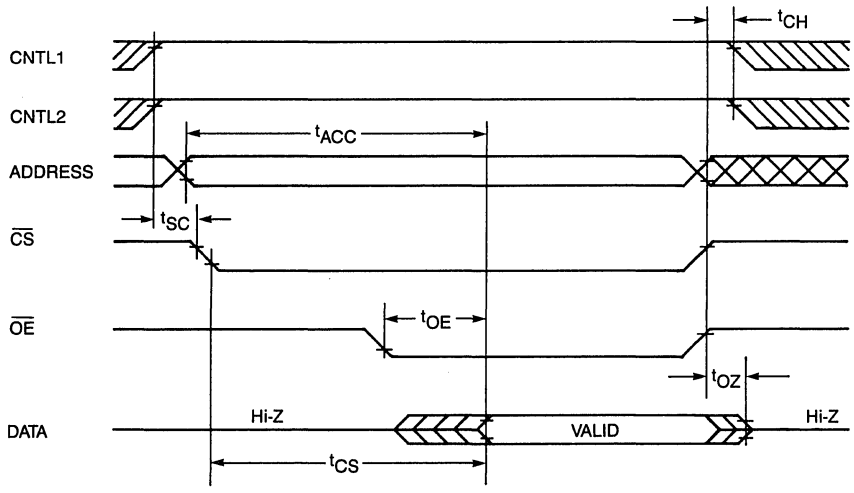
Input Pulse Levels. . . . . .0.8 Volts to 2.0 Volts
Input Rise & Fall Times . . . . . .10 ns
Input & Output Timing Levels . .0.8 Volts to 2.0 Volts

TEST LOAD CIRCUIT

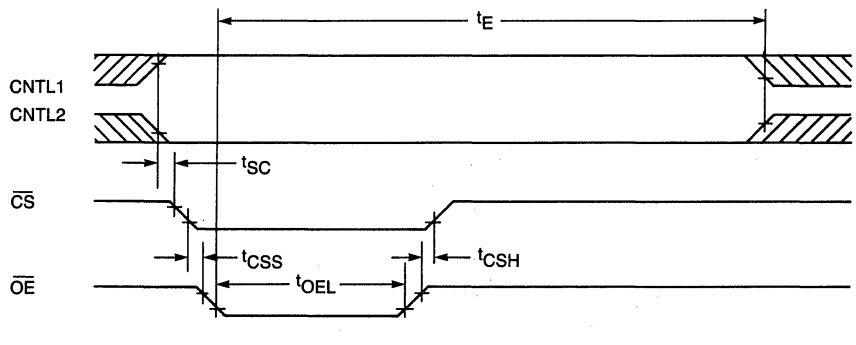


* Includes Jig Capacitance
All Diodes IN3064 or Equivalent

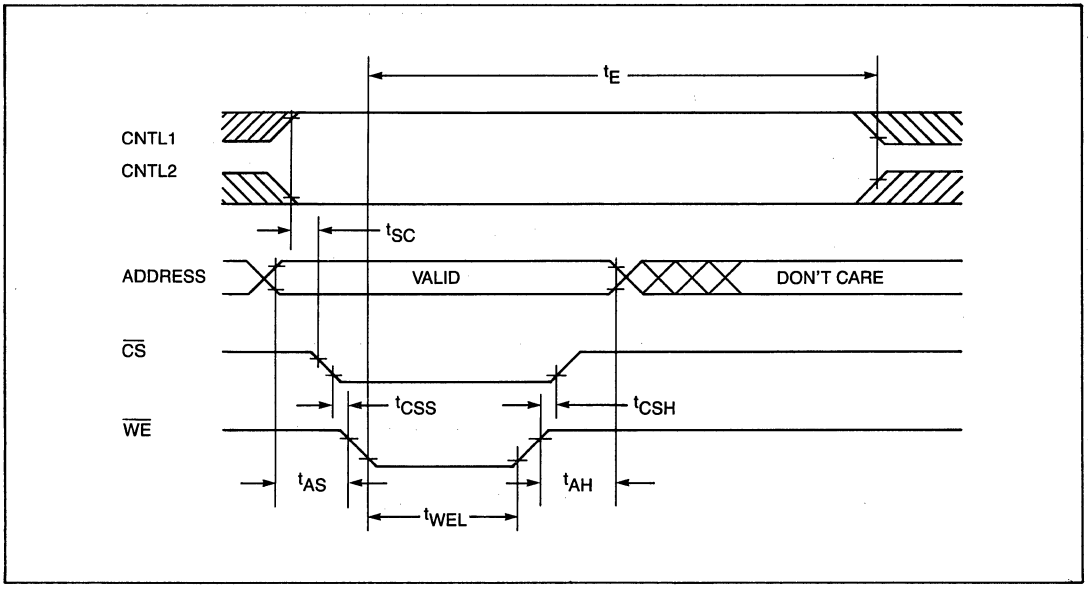
READ MODE



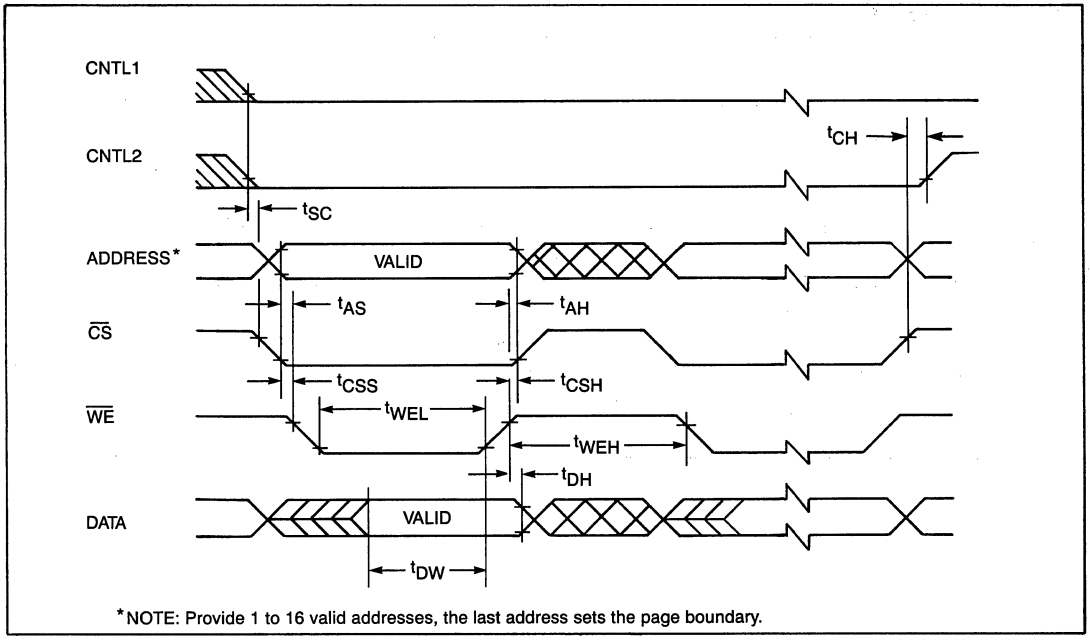
CHIP ERASE MODE



PAGE ERASE MODE

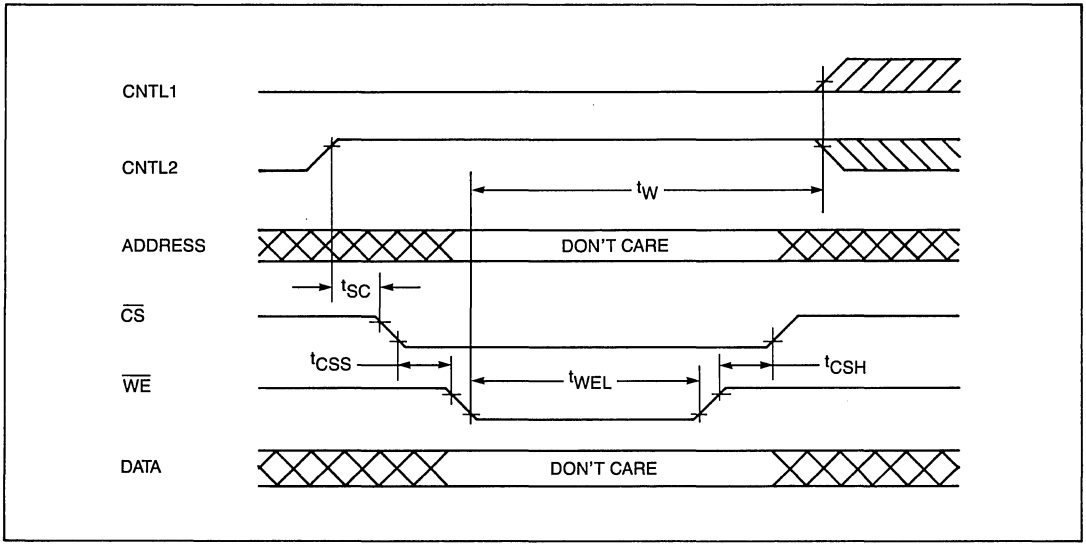


LOAD DATA MODE

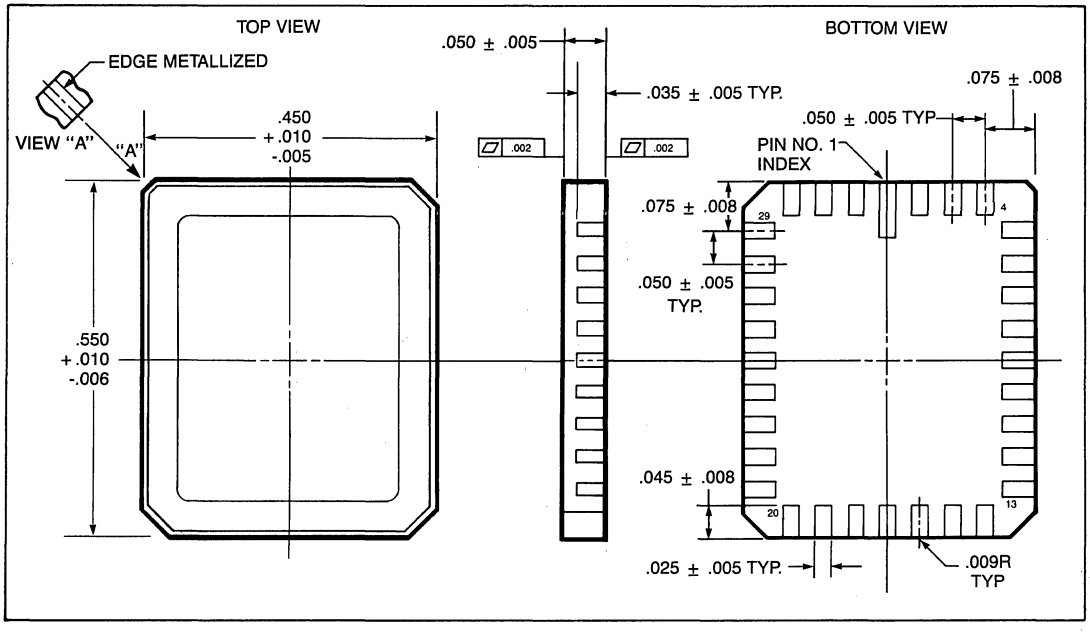


*NOTE: Provide 1 to 16 valid addresses, the last address sets the page boundary.

WRITE MODE

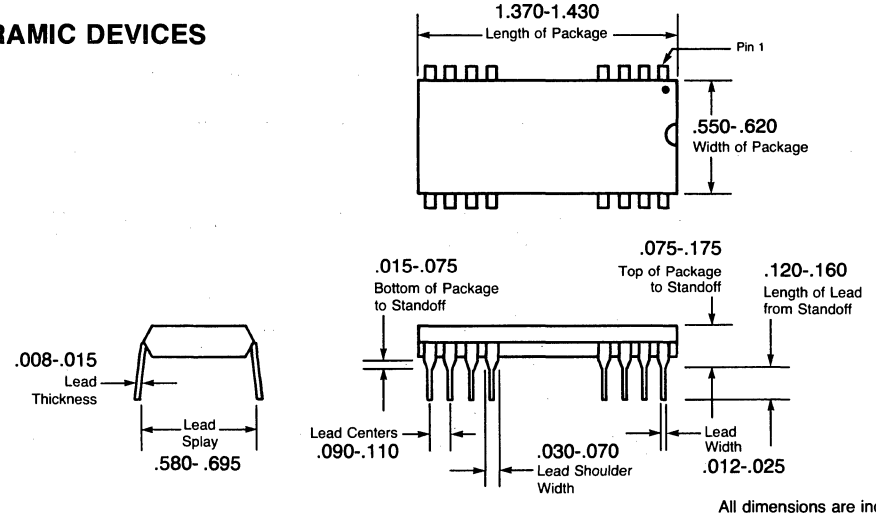


32 PIN LEADLESS CHIP CARRIER



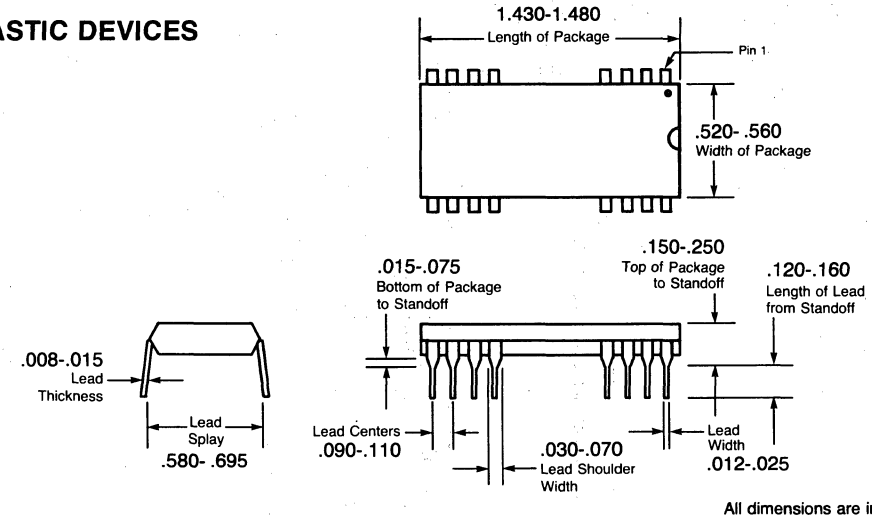
MECHANICAL DATA 28 PIN

CERAMIC DEVICES



All dimensions are inches.

PLASTIC DEVICES



All dimensions are inches.

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52864
64K (8Kx8) EEPROM

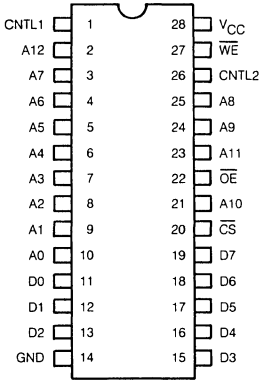
PRELIMINARY

- Electrically Erasable PROM
- Advanced SNOS N-Channel Technology
- 300 ns Access Times
- Low Power Dissipation
- Memory Margining
- 5 Volt Only Operation
- In-System Reprogrammability
- 3-State Outputs
- Latched Address & Data Bus
- 28 Pin DIP With Industry Standard Byte-Wide Pinout
- Optional 32 Pin LCC Available
- Page Alterable

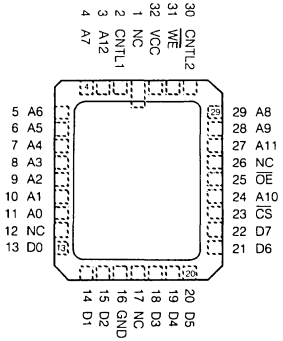
The NCR 52864 is a 64K bit (8Kx8) Electrically Erasable PROM utilizing the Silicon-Nitride-Oxide-Silicon (SNOS) process developed by NCR. Designed for ease-of-use, the 52864 requires only a 5 volt source for all modes of operation. All voltages required for programming are generated internally by an on-chip voltage generator, thus eliminating the need for any external high voltage supplies. The 52864 also provides on-board latching of addresses and data lines during non-volatile operations. The 52864 allows memory margining in order to predict the data retention time. All control line inputs, as well as the address inputs and data I/O's, are TTL compatible. This feature, combined with access times of 300 ns and a byte-wide industry standard pinout makes the 52864 highly compatible with existing microprocessors. Erasing the 52864 is accomplished in either a chip or page fashion. Writing the device can be performed either word by word or, in applications requiring fast system reprogramming, by a contiguous page of 16 words. The NCR 52864 is available in a 28 pin DIP in commercial, industrial and high reliability versions. Optionally, the NCR 52864 can be packaged in a 32 pin leadless chip carrier (LCC).

PIN CONFIGURATION

28 PIN DIP

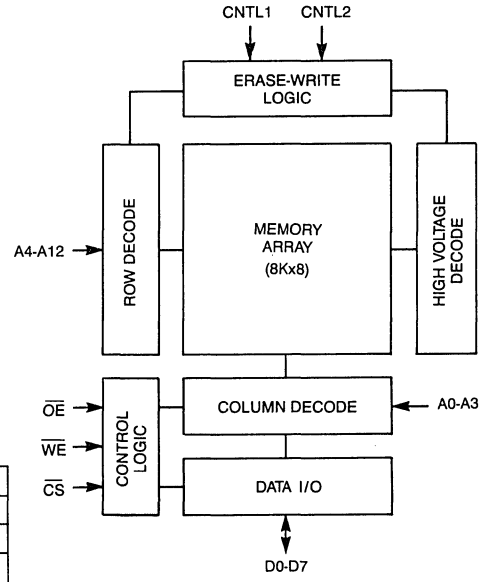


32 PIN LCC



(Top View)

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A0-A12	Address Inputs	WE	Write Enable
D0-D7	Data I/O	OE	Output Enable
CNTL 1 & CNTL 2	Control Lines	NC	No Connection
		V_{CC}	+5 Volt ± 10% Supply Voltage
CS	Chip Select		

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This is advance information and NCR reserves the right to change the specifications without notice.

DEVICE OPERATION

READ MODE

The 52864 is read like a conventional static RAM. Valid data is available on the output pins when a valid address is provided and $\overline{CS}$ and $\overline{OE}$ are brought low. If the address lines change while $\overline{CS}$ and $\overline{OE}$ are maintained low, valid data will be available after a delay of t_{ACC}.

CHIP ERASE MODE

Chip erase is accomplished by holding CNTL1 high and CNTL2 low followed by bringing $\overline{CS}$ and $\overline{OE}$ low. During chip erase all data and address lines are "don't care". An erased state corresponds to a logical "0".

PAGE ERASE MODE

Page (16 bytes) erase is accomplished in a manner similar to chip erase except that $\overline{OE}$ is held high and $\overline{WE}$ is brought low, and a page address (A_4-A_{12}) must be provided.As in chip erase, the data lines are "don't care" and the erased state corresponds to a logical "'0".

LOAD DATA MODE

During the load data mode, data is loaded into 16, 8 bit internal latches. In this mode, data is loaded much the same way as it is for a SRAM. Both CNTL lines are held low while "clocking" $\overline{CS}$ and $\overline{WE}$. Addresses and data must be valid while $\overline{CS}$ and $\overline{WE}$ are low. The load data mode must be followed by a write mode to prevent losing the data that has been loaded in. Data may be loaded and then written 1 to 16 bytes at a time.

WRITE MODE

Data can be written into non-volatile cells by holding CNTL2 high and maintaining CNTL1 low while $\overline{CS}$ and $\overline{WE}$ are brought low. Data and address lines are "don't care" during a write cycle. A written state corresponds to a logical "1".

MEMORY MARGINING

The NCR 52864 supports margining of the memory transistors. Memory margining allows device retention time to be projected for the purpose of device evaluation. An application note describing the memory margining algorithm is available.

MODE SELECTION

MODE	$\overline{OE}$	$\overline{WE}$	CNTL1	CNTL2	$\overline{CS}$
Standby	X	X	H	H	H
Read	L	H	H	H	L
Chip Erase	L	H	H	L	L
Page Erase	H	L	H	L	L
Load Data	H	L	L	L	L
Write	H	L	L	H	L

ABSOLUTE MAXIMUM RATINGS

Voltage On Any Pin With
Respect to GND ..... -0.5 to +7V
Voltage on CNTL1 and CNTL2
(During Memory Margining Only)..... -6V to +22V
Storage Temperature ..... -65°C to 150°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operational limits stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

		52864			52864I			52864HR			
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	Input High-Level Voltage	2		$V_{CC}+1$	2		$V_{CC}+1$	2		$V_{CC}+1$	V
V_{IL}	Input Low-Level Voltage	-0.3		0.8	-0.3		0.8	-0.3		0.8	V
T_A	Ambient Temperature	0		70	-40		85	-55		125	°C

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (Unless Otherwise Noted)

			52864			52864I			52864HR			
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{IN}	Input Leakage Current	V_{IN} = 0V to 5.5V			10			10			10	μA
I_O	I/O Leakage Current	CS = V_{IH} V_O = 0V to 5.5V			10			10			10	μA
I_{CC}	Supply Current	Outputs Open, CS = V_{IL} CS = V_{IH}			60 30			60 30			60 30	mA mA
V_{OH}	Output High-Level Voltage	I_{OH} = —400μA	2.4			2.4			2.4			V
V_{OL}	Output Low-Level Voltage	I_{OL} = 2.1mA			0.4			0.4			0.4	V
T_S	Non-Volatile Data Storage	Following Minimum Erase/Write Cond.	10			10			10			Yr

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AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

READ CYCLE

Symbol	Parameter	52864			52864I			52864HR			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{ACC}	Address Access Time			300			450			450	ns
t_{CS}	Chip Select Access Time			300			450			450	ns
t_{OE}	Output Enable Access Time			150			150			150	ns
t_{OZ}	Output Enable Or Chip Select to Output High Impedance			90			115			115	ns
t_{SC}	Control Setup Time										
	• After Erase or Write	50			50			50			µs
	• After Load or Read	500			500			500			ns
t_{CH}	Control Hold Time	0			0			0			ns

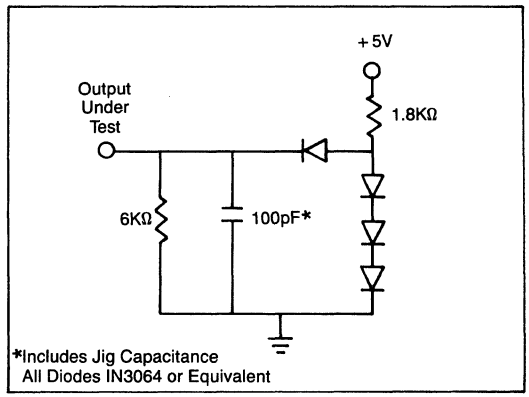
ERASE/LOAD/WRITE CYCLE

Symbol	Parameter	52864			52864I			52864HR			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_E	Erase Time	100		200	100		200	100		200	ms
t_W	Write Time	10		20	10		20	10		20	ms
t_{SC}	Control Setup Time										
	• After Erase or Write	50			50			50			µs
	• After Load or Read	500			500			500			ns
t_{CSS}	Chip Select Setup Time	0			0			0			ns
t_{CSH}	Chip Select Hold Time	0			0			0			ns
t_{AS}	Address or Data Setup Time	0			0			0			ns
t_{AH}	Address or Data Hold Time	0			0			0			ns
t_{OEL}	Output Enable Pulse Width	200			200			200			ns
t_{WEL}	Write Enable Pulse Width	200			200			200			ns
t_{WEH}	Write Enable Recovery Time	100			100			100			ns
t_{DW}	Data to Write Time Overlap	200			200			200			ns
t_{DH}	Data Hold Time	0			0			0			ns
$N_{E/W}$	Number of Erase/Write Cycles	10^4			10^4			10^4			Cycles

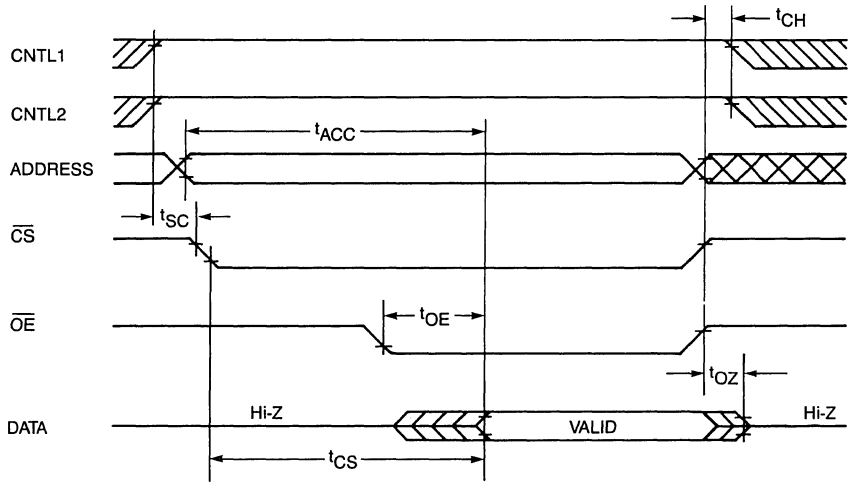
A. C. CONDITIONS OF TESTS

Input Pulse Levels. . . . . .0.8 Volts to 2.0 Volts
Input Rise & Fall Times . . . . . .10 ns
Input & Output Timing Levels . .0.8 Volts to 2.0 Volts

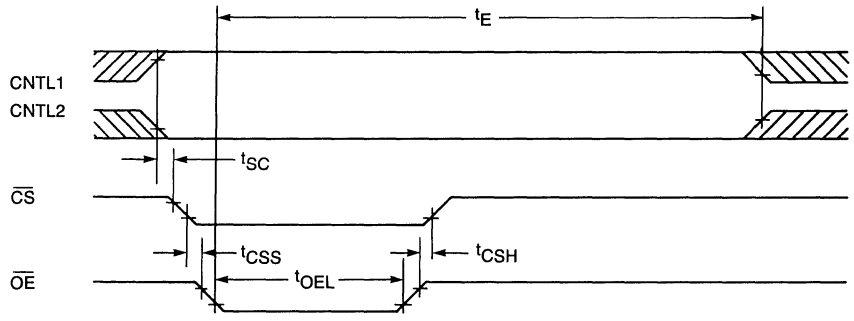
TEST LOAD CIRCUIT



READ MODE



CHIP ERASE MODE



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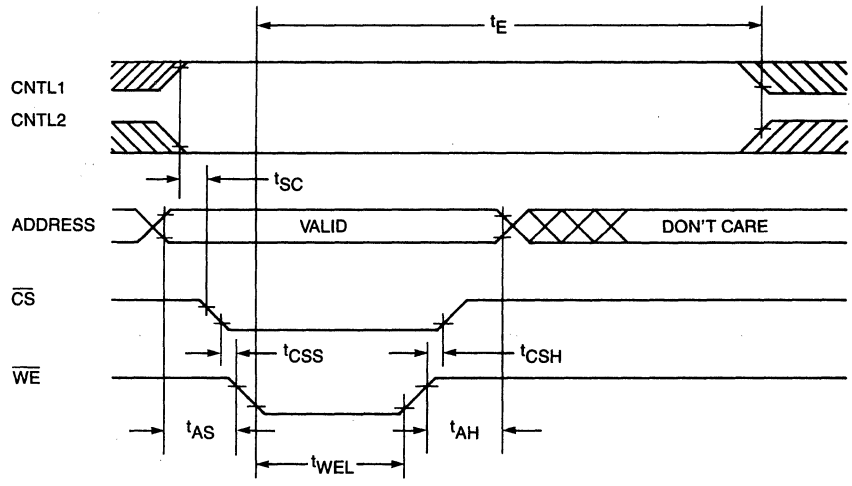
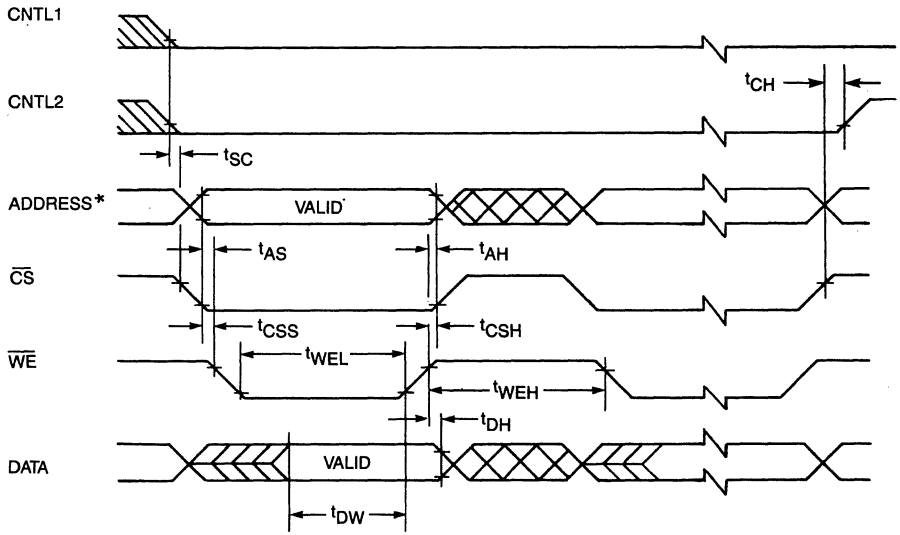
PAGE ERASE MODE

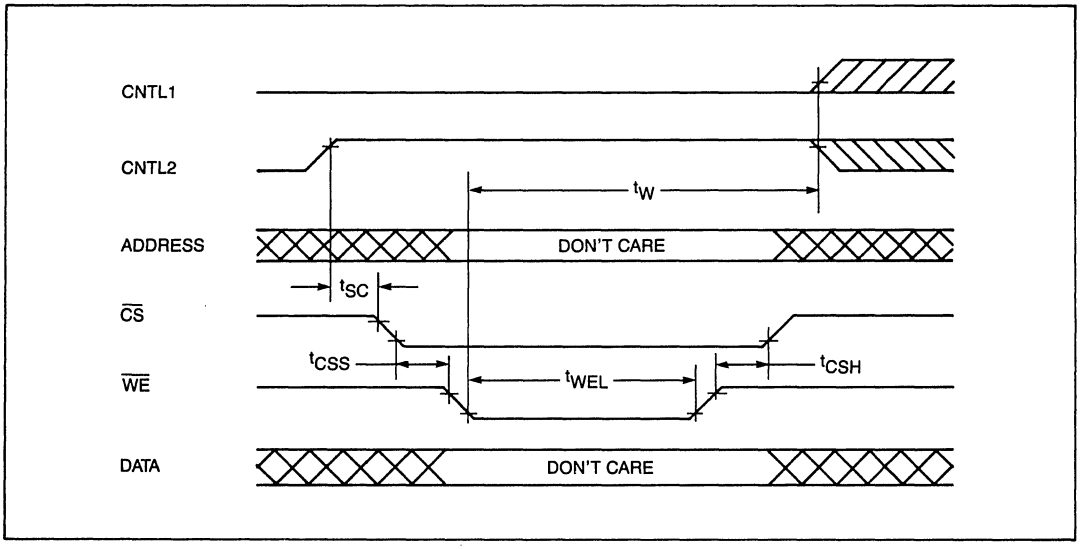


LOAD DATA MODE

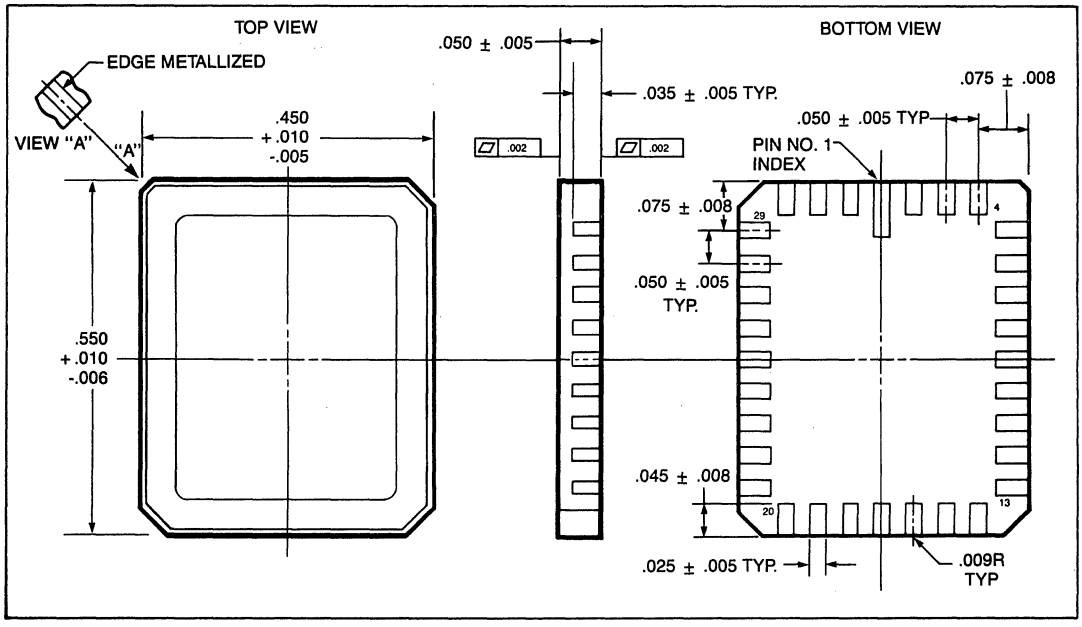


* NOTE: Provide 1 to 16 valid addresses, the last address sets the page boundary.

WRITE MODE

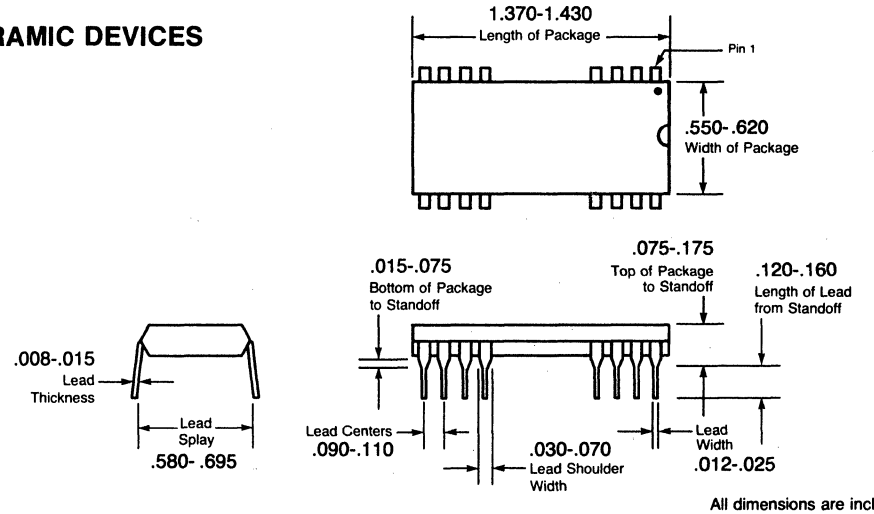


32 PIN LEADLESS CHIP CARRIER



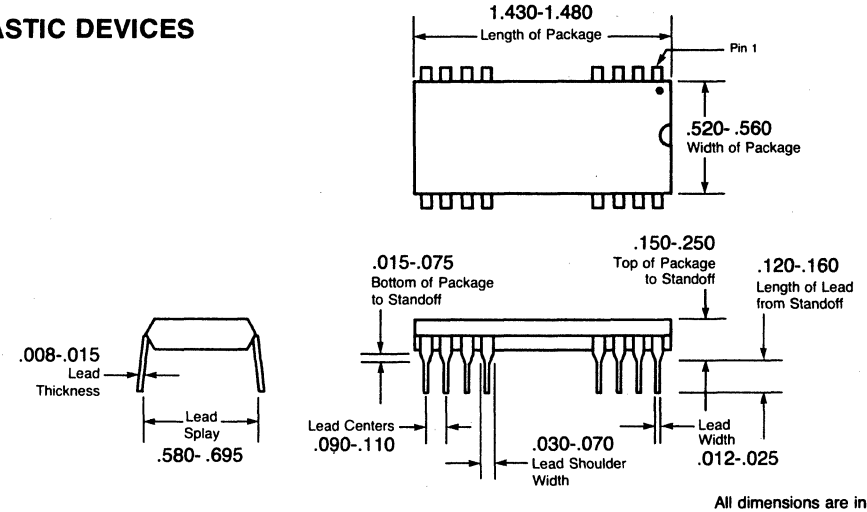
MECHANICAL DATA 28 PIN

CERAMIC DEVICES



All dimensions are inches.

PLASTIC DEVICES



All dimensions are inches.

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Application Notes

SNOS Non-Volatile Memory Reliability

APPLICATION NOTE

NCR Microelectronics

NCR established its first microelectronics laboratory in 1963 to stay abreast of the emerging semiconductor technology. In 1971, the first microelectronics facility was established in Miamisburg, Ohio to manufacture P-channel MOS integrated circuits. In 1973, NCR produced the world's first 4K bit Electrically-Alterable Read Only Memory (EAROM), a non-volatile component using P-channel, Metal-Nitride-Oxide-Semiconductor (MNOS) technology. Further development efforts resulted in several 1K to 16K bit EAROM, Word-Alterable Read Only Memory (WAROM), and Non-Volatile Random Access Memory (NVRAM) components. These components provided a competitive advantage to our computer systems and terminal product lines.

To meet internal demand, the microelectronics operation was expanded with the addition of a second facility in Colorado Springs, Colorado in 1975 and a third facility in Fort Collins, Colorado in 1979.

Recognizing the need for high-performance non-volatile memory arrays, NCR developed the Silicon Nitride Oxide Silicon (SNOS) process which utilizes the N-channel, silicon gate, double level polysilicon technology. The development of this process led to the introduction of the NCR 4485 4K NVRAM in early 1981.

Backed with the strength and discipline gained in over 10 years of internal supply, NCR entered the merchant semiconductor market in mid-1981, and has established itself as a leading supplier of semiconductor devices, especially non-volatile products.

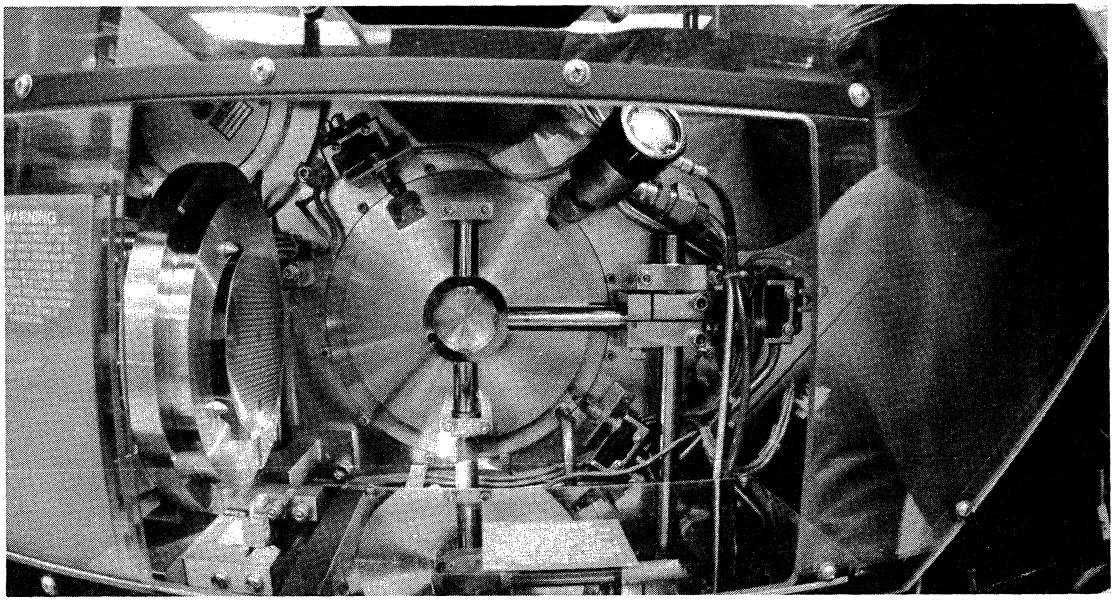
NCR now offers a family of 5-Volt only, SNOS processed Electrically Erasable Programmable Read Only Memory (EEPROM) and NVRAM components. Our future strategy is to maintain and strengthen our leadership position in non-volatile memories by providing new and innovative products of the highest quality to the market place while providing superior customer services.

NCR Quality and Reliability Assurance Program

The NCR commitment to quality, reliability, and customer support is an integral part of corporate philosophy and policy, originating from, and emphasized by, the highest levels of NCR management.

The NCR Corporate Quality policy states the following:

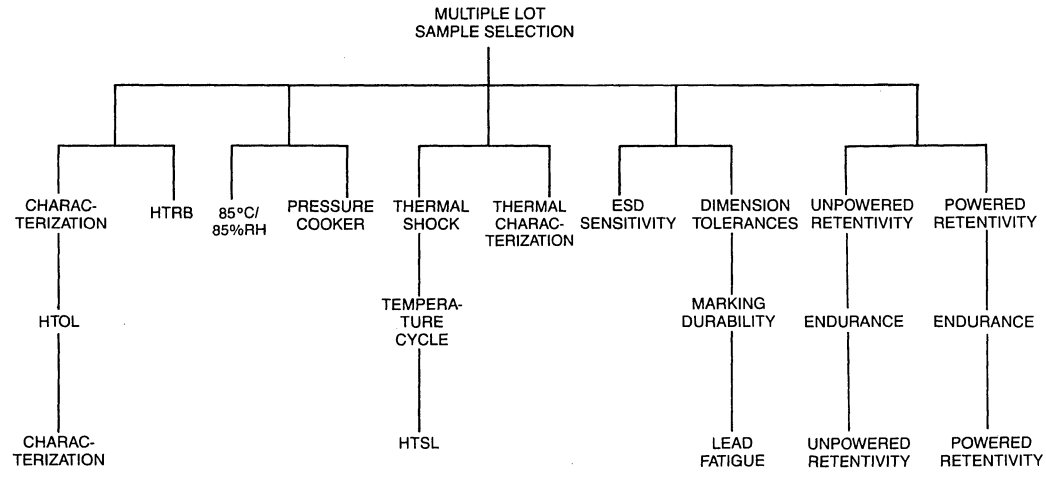
> The NCR Corporation is dedicated to providing products and services which are of superior quality and reliability.
>
> Implicit in the NCR Quality Policy is the identification and establishment of realistic and appropriate product specifications consistent with the intended use of the product, and a commitment to meet them.
>
> In order to enhance its quality leadership position NCR fosters the habit of continuous quality improvement.
>
> Consistent and diligent implementation of these doctrines ensures that our products and services offer value which is superior to that of our competition.



The NCR commitment is embodied in a comprehensive quality program which emphasizes superior product quality and reliability and excellent customer support.

The NCR Quality and Reliability program includes:

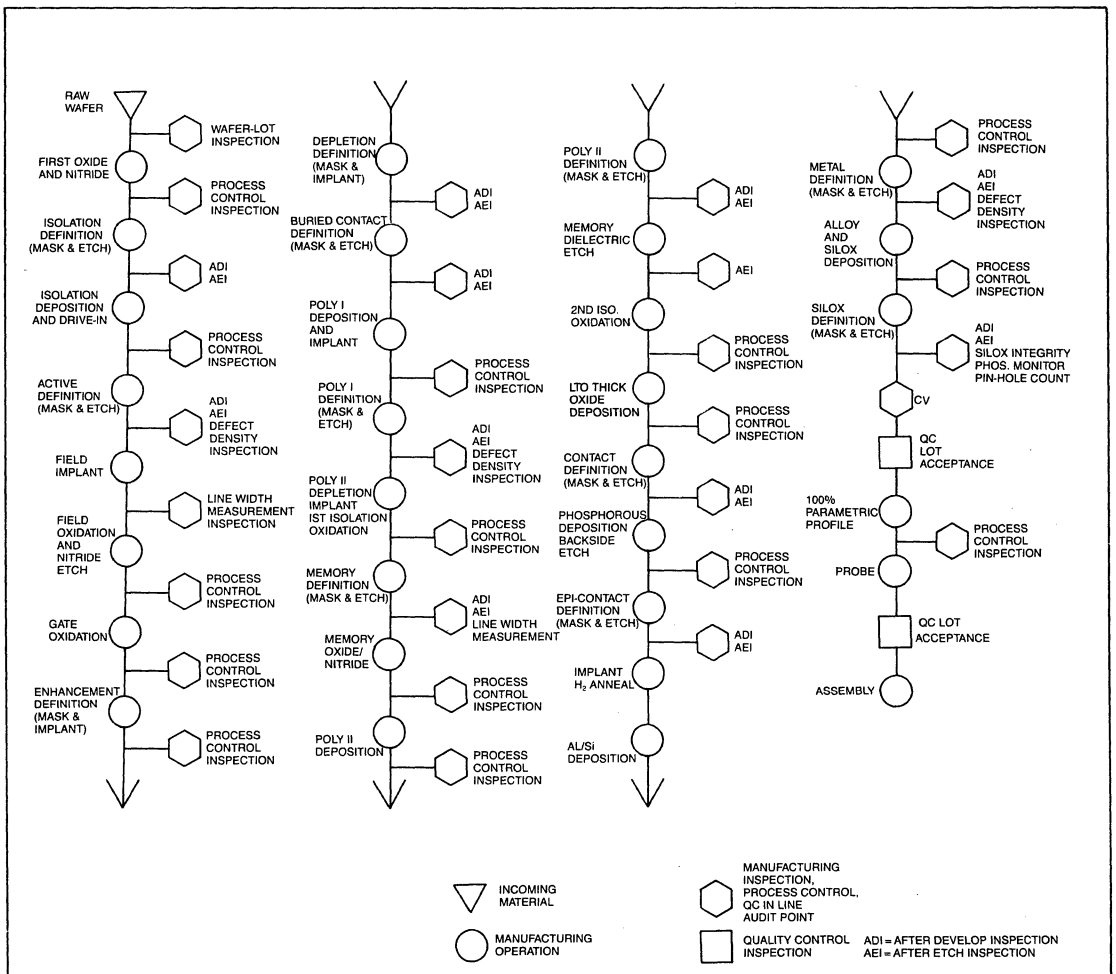
- **A Quality Program Structured According to MIL-Q-9858A**
  The NCR Quality program is a very comprehensive and extensively documented program that is structured to meet the intent of military quality requirements standard MIL-Q-9858A. This program assures quality throughout the production phases; for example, design, development, processing, assembly, inspection, test, maintenance, packaging, shipping, and storage. It provides for the prevention and ready detection of discrepancies and for timely and positive corrective action.
- **A Comprehensive Design Acceptance Evaluation**
  Prior to the release of a new component, NCR Quality Assurance completes a comprehensive design acceptance evaluation to ensure conformance of the component to its specification, and to the quality and reliability goals.



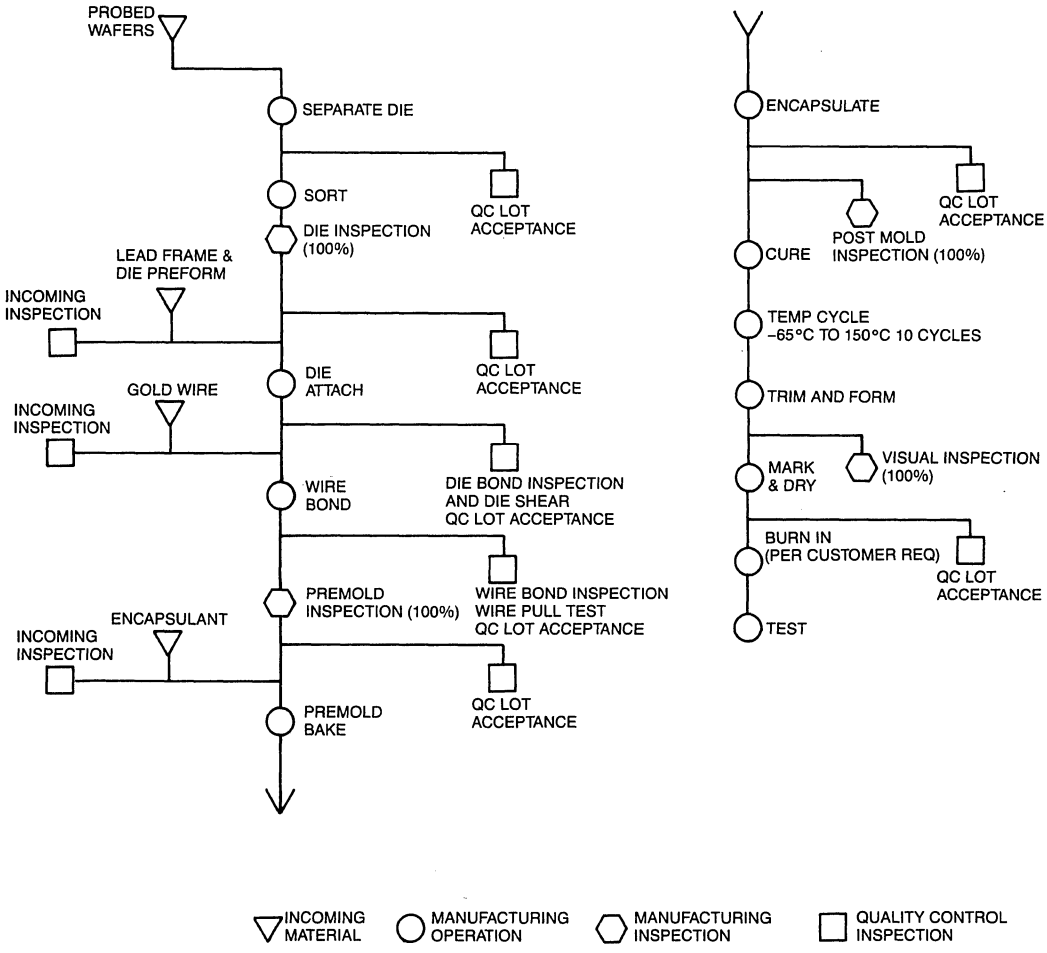
DESIGN ACCEPTANCE EVALUATION PLAN

- **Stringent Process/Assembly Controls**
  Process and assembly controls are used extensively to build-in quality and reliability of the finished products. These stringent controls are evident in the SNOS wafer processing and package assembly flows. To name a few examples of these controls:

  Line width measurement and defect inspection are performed before and after etching (ADI and AEI) for critical mask definition steps to ensure that the device geometry is within the design and process requirements. Phosphorous concentration measurement and pin-hole count are performed to ensure the silox integrity for enhanced moisture performance of plastic packaged devices.

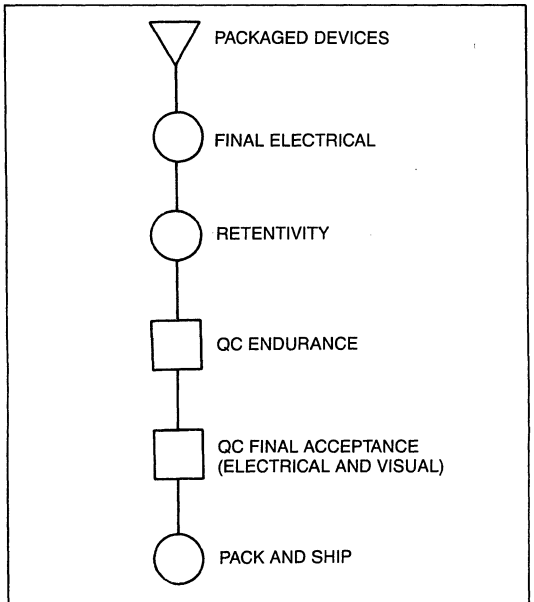


SNOS WAFER PROCESSING FLOW CHART



PLASTIC PACKAGING ASSEMBLY FLOWCHART

- **Statistical In-Process Quality Control**
  Statistical quality control methods are employed to monitor the manufacturing process through the use of $\overline{X}$ and R (average and range) control charts.
- **On-going Quality Audits**
  On-going quality audits are performed throughout the manufacturing plant, at our suppliers' plants, and at assembly, burn-in, and testing sites.
- **Thorough Electrical Testing**
  To ensure that the finished products meet our customers' requirements, thorough electrical testing is performed. In processing, capacitance-voltage measurements are made to test for ionic contamination. 100% parametric profile measurements are made to ensure all process parameters such as the non-volatile characteristics, thresholds, and transconductance are within the process acceptance limits. Testing of packaged devices is accomplished in accordance with the standard test flow as illustrated. 100% Final electrical testing is performed at room temperature and at high and/or low temperatures as required by the specification. 100% retentivity testing utilizing the direct memory margining technique and sample endurance testing are performed to guarantee the non-volatile performance.



SNOS TEST FLOW

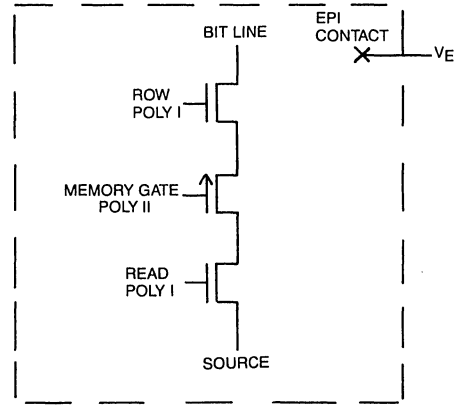
- **Aggressive Quality Control Sampling Plans, Zero Defects Ultimate Quality Goal**
  Quality Control acceptance sampling is performed on each lot to assure conformance of the final product to our customers' requirements. Very stringent sampling plans are employed at final acceptance. The ultimate quality goal and challenge is to ship defect free products to our customers.
- **Quality Circles and Training Programs**
  Quality Circles and training programs are essential to the NCR Quality program. In addition to improving the technical skills of all NCR people, these programs stimulate the awareness of "quality" and encourage the attitude that "all errors and defects are preventable."
- **On-going Reliability Monitoring Program**
  The objectives of an on-going Reliability Monitoring program are:
  —To evaluate the reliability of as-shipped products
  —To build a statistically large reliability data base for reliability prediction
  —To detect changes in product performance so that timely and positive corrective action can be taken.

  On-going Reliability Monitoring is initiated for each product family after the completion of the design acceptance process. Each week, samples are pulled from production lines for reliability evaluation. The evaluation includes operating life, package integrity, and non-volatile performance testing. When failures are generated, in-depth failure analysis is performed to identify the failure mechanisms. Results are fed back to Engineering and Manufacturing for positive correction action.
- **Dedicated Customer Support**
  Closed Loop Communication and Corrective Action
  With over 10 years of experience in internal supply, NCR Microelectronics understands customers' needs and is dedicated to providing customers with high quality products and services. To achieve this, NCR Microelectronics works closely with customers to ensure that the applications are consistent with the intended use

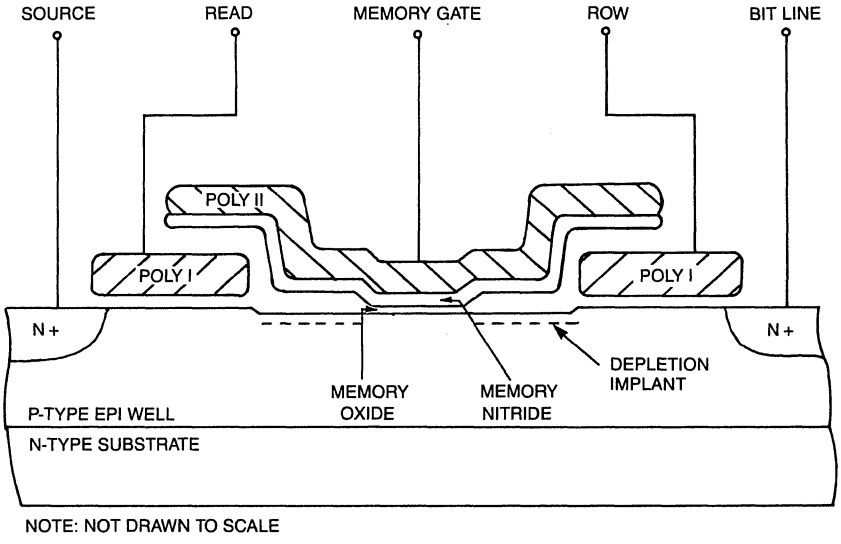
of the products. When encountering application or test correlation difficulties, NCR performs analysis, and recommends system modifications, or implements screening procedures or other corrective action to ensure "Fitness For Use." NCR firmly believes that such closed-loop communication and corrective action result in a better understanding of user needs and improved quality and reliability.

Electrically Erasable Programmable Read Only Memory (EEPROM)

A SNOS EEPROM cell consists of two Poly I enhancement transistors in series with a Poly II - Si_3N_4 - SiO_2 nonvolatile memory transistor. The illustration depicts both the schematic and cross-sectional view of a SNOS EEPROM cell.



SCHEMATIC OF A SNOS EEPROM CELL



NOTE: NOT DRAWN TO SCALE

CROSS-SECTION OF A SNOS EEPROM CELL

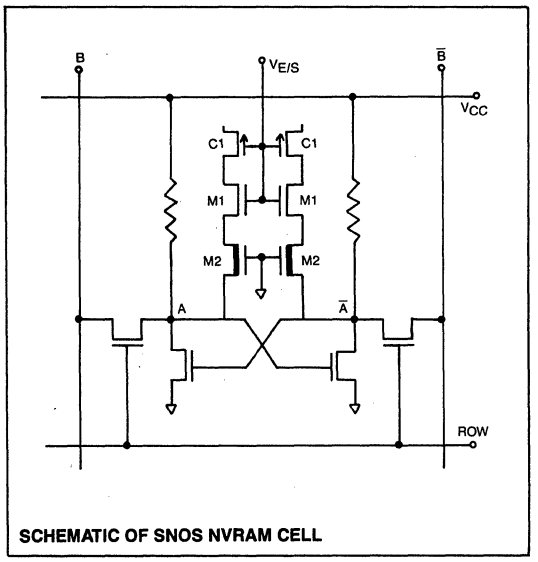
Memory operations in EEPROMs are Erase, Write "one", Write "zero", and Read. In the Erase and Write operations, data is transferred from the data registers to the non-volatile memory. In the Read operation, data is transferred from the non-volatile memory back to the data registers.

- **Erase**
  During an Erase operation, the MEMORY GATE is held at ground while the epi well is charged to +20 Volts. This produces a 20 volt differential across the gate dielectric of the memory transistor, causing a net positive charge to be stored in the memory nitride, thereby making the memory a depletion transistor (with a negative threshold).
- **Write "One"**
  To write a "one" into memory, the BIT LINE is forced to ground by the data register. The MEMORY GATE is pulsed from ground to +20 Volts, while the epi is regulated at –2.5 Volts. With the ROW line selected (at +5 Volts), the surface potential of the memory transistor is held to zero by the BIT LINE. The resulting 20 Volt differential between the memory gate and the silicon surface below it will be dropped across the memory gate dielectric. This differential causes negative charges to replace the positive charges that were stored in the memory nitride, thereby making the memory an enhancement transistor (with a positive threshold).
- **Write "Zero"**
  To write a "zero" into memory, the BIT LINE is held high by the data register. With both the BIT LINE and the ROW LINE being at +5 Volts, the ROW transistor turns off as the memory gate is pushed above +5 Volts. The surface potential of the memory is now free to follow the memory gate voltage, resulting in the formation of a depletion region in the silicon below the memory gate. Since the capacitance of the depletion region is much smaller than that of the memory dielectric, the majority of the potential (a total of 22.5 Volts between the memory gate and the epi) is dropped across the depletion region instead of the memory dielectric. As a result, the memory remains in the erased state. This process in which memory transistors remain erased during a Write operation is called "channel shielding."
- **Read Data**
  During a Read operation, the MEMORY GATE is held at ground. If the row is selected and the memory transistor is erased (depletion mode), the memory cell will conduct and pull the BIT LINE low. If the memory cell is written (enhancement mode), no current will conduct and the BIT LINE will be pulled high.

Non-Volatile Random Access Memory (NVRAM)

The schematic and cross-section of a SNOS NVRAM cell show that it consists of a six-element static RAM cell and two three-element non-volatile memory devices. The RAM cell consists of four poly I enhancement transistors and two polysilicon load resistors. Each of the two nonvolatile devices consists of a non-volatile Poly II capacitor C1, a Poly II depletion transistor M1, and a Poly I depletion transistor M2. C1 and M1 share a common Poly II gate.

Memory operations in NVRAMs are Store and Recall. In the Store operation, data is transferred from the static RAM cells to the non-volatile memory. In the Recall operation, data is transferred from the non-volatile memory back to the static RAM cells.



SCHEMATIC OF SNOS NVRAM CELL

Store

During a Store operation, the following sequence of events occurs.

- Erase

  First, a self-timed Erase of the non-volatile capacitors is performed. VE/S node is pulsed to –22 Volts and the substrate bias is regulated at –2.5 Volts. A net potential of 19.5 Volts appears across the memory dielectric of C1 capacitors, causing a net positive charge to be stored in the memory nitride, thereby shifting the threshold of the two C1 capacitor to about –6 Volts.

- Write

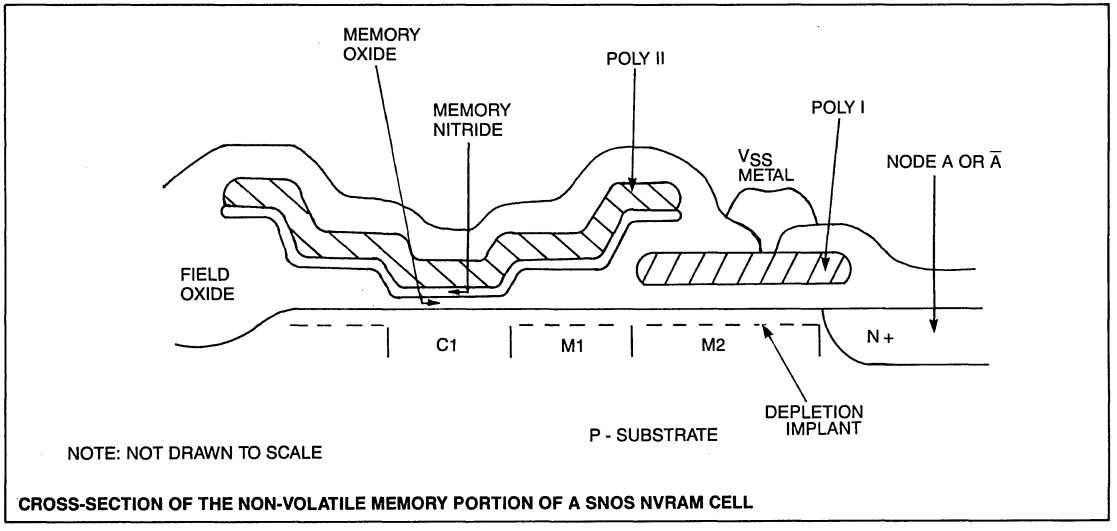
  Next, VE/S node is pulsed to +22 volts for a self-timed Write operation. Suppose the RAM flip-flop was previously set such that node A is high and node $\overline{A}$ is low (at 0 volt). With node A set high, the M2 transistor on the side of node A will be off. The surface potential of C1 on the A side is then free to follow VE/S very closely. As a result, this C1 capacitor becomes channel shielded, and its threshold remains unaltered. The C1 capacitor on the node $\overline{A}$ side, however, will have all of the VE/S potential dropped across its memory dielectric, since its surface potential is held to zero by node $\overline{A}$ through the conducting M2 transistor on the $\overline{A}$ side. Consequently, the threshold of the C1 capacitor on the $\overline{A}$ side is shifted from the –6 Volts erased level to a +6 Volts written level.

  Suppose a "one" input corresponds to an erased C1 on the A side and a written C1 on the $\overline{A}$ side, then a "zero" input corresponds to the opposite configuration of a written C1 on the A side and an erased C1 on the $\overline{A}$ side.

Recall

During a Recall operation, VE/S is held at 0 Volt. C1 on the $\overline{A}$ side (with +6 Volts threshold) is turned off, while C1 on the A side (with –6 Volts threshold) is turned on. The capacitive load provided by the nonvolatile memory element on the $\overline{A}$ side of the cell is therefore lighter than the capacitive load on the A side. When both nodes A and $\overline{A}$ are simultaneously grounded and then released, node $\overline{A}$ will charge faster than node A. When node $\overline{A}$ charges to the threshold of the grounding transistor of node A, node A is pulled to ground, and node $\overline{A}$ continues to charge to V_{CC}. This process, grounding both sides of the cell and then releasing them, is how data is recalled from the nonvolatile memory elements and placed back into the RAM cell.

Note that the data in the cell after the Recall is opposite to the data which was in the cell during the Store. Data correction circuitry in the periphery compensates for this inversion, therefore, the internal data inversion is transparent.



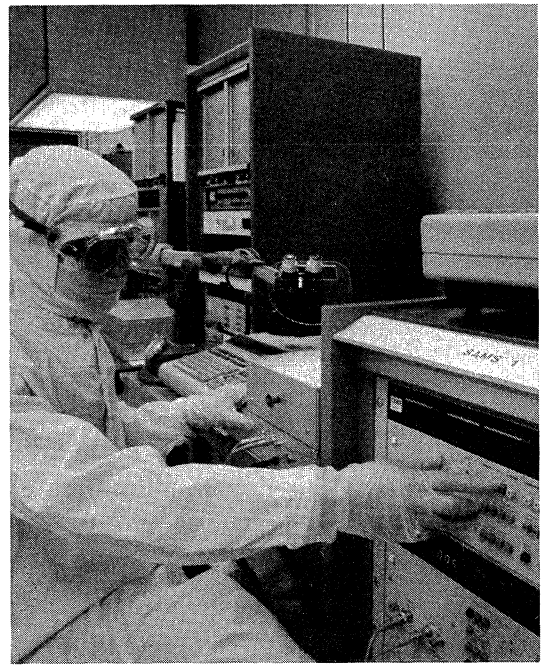
CROSS-SECTION OF THE NON-VOLATILE MEMORY PORTION OF A SNOS NVRAM CELL

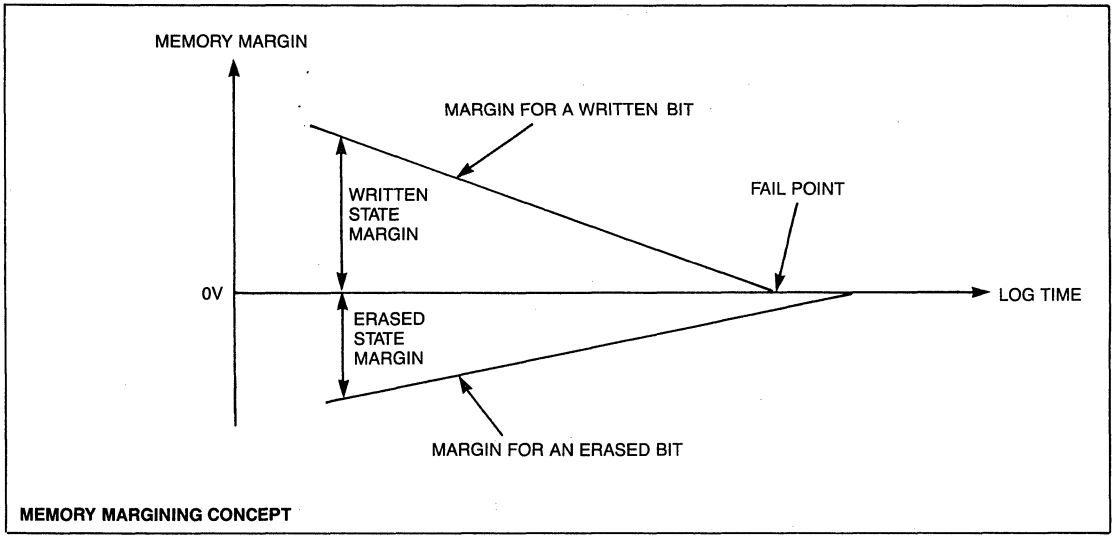
Margining Capability
A Means For 100% Testing Of Retentivity

The NCR SNOS non-volatile components differ from other non-volatile products in the industry in that they have a direct memory margining capability. This capability allows prediction of data retentivity and provides the means for 100% testing of SNOS components in manufacturing to guarantee the required retentivity.

Margining is the process of measuring the non-volatile memory thresholds to predict retentivity. In the margining mode, the memory gate is directly accessible through an external pin. This allows the memory gate voltage to be varied (positively for written state and negatively for erased state) to determine the memory margin.

The charge stored in the nitride has been found to decay logarithmically with time. Therefore, margins measured at various times (after 24 hours) can be used to project retentivity. The fail point occurs when either the written state margin or the erased state margin becomes zero. (An application note describing the memory margining technique in detail is available.)





MEMORY MARGINING CONCEPT

SNOS Reliability

The reliability of the NCR SNOS non-volatile components is effectively evaluated through the use of the following tests: High Temperature Operating Life (HTOL), Retentivity, Endurance, Temperature Humidity Bias (85°C/85%RH), Pressure Cooker, Temperature Cycle, and Thermal Shock. Retentivity and endurance tests are unique to non-volatile components and must be done to ensure reliability. All others are standard tests for most types of integrated circuits and are designed to place components under severe conditions that accelerate die related and package related types of failures.

Current data from both Qualification and Reliability Monitor evaluation are presented in the following paragraphs. Reliability data gathered during on-going Reliability Monitoring is reported quarterly and is available upon request.

High Temperature Operating Life (HTOL)

HTOL is a dynamic stress at 125°C. A maximum V_{CC} voltage of +5.5 Volts is applied to the components under stress. This test is performed to accelerate failures resulting from thermally activated defects. Failure mechanisms include die related defects which can occur during wafer processing and both die and package related defects which can occur during assembly.

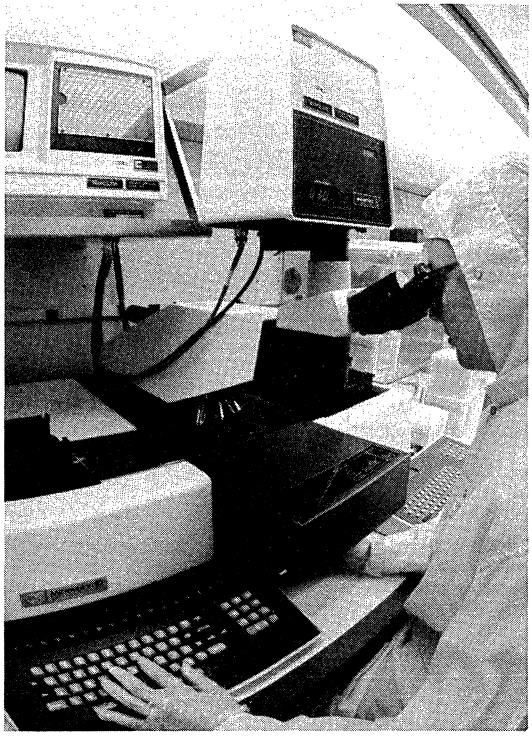
HTOL Test Results

Part Type	125°C Device Test Hrs	70°C Equivalent Hrs.	70°C Fail Rate (FITs) 60% Confidence Level
NCR 52212	6.48E5	6.87E7	105
NCR 52210	7.07E4	7.49E6	120
NCR 52801	7.65E5	8.11E7	155
Combined	1.48E6	1.57E8	120

Since temperature is the primary stress mechanism for this test, the Arrhenius Equation which relates reaction rate to temperature is used to model the acceleration between temperatures of interest. For this analysis, 1.0eV is used for the activation energy value. Based upon these assumptions and Chi-squared statistics, the 70°C combined failure rate at a 60% confidence level demonstrated for SNOS processed devices is 120 Fits. (1 Fit is equivalent to 1 failure per 10^9 device hours.)

Of the few failures observed during life testing, the predominant failure mode was nitride breakdown due to random nitride defects. Analysis showed that these life test failures were of the same type as the endurance (erase/write cycling) failures. Their failing symptoms indicated that they resulted from the erase/write stress which occurred during functional verification (at periodic intervals during life testing) rather than the life test stress itself. When these failures were detected, processing and screening enhancements were employed. The effectiveness of these enhancements has been supported by recent life test data which shows a significant reduction of these kinds of defects.

(A discussion of nitride failures is included in the section under Endurance.)



Retentivity

The retentivity of a device is the length of time data can be retained in its memory before reprogramming is required.

The direct memory margining capability of all NCR SNOS non-volatile components allows accurate prediction of retentivity. It provides the means for 100% testing of NCR SNOS non-volatile components to guarantee their retentivity performance.

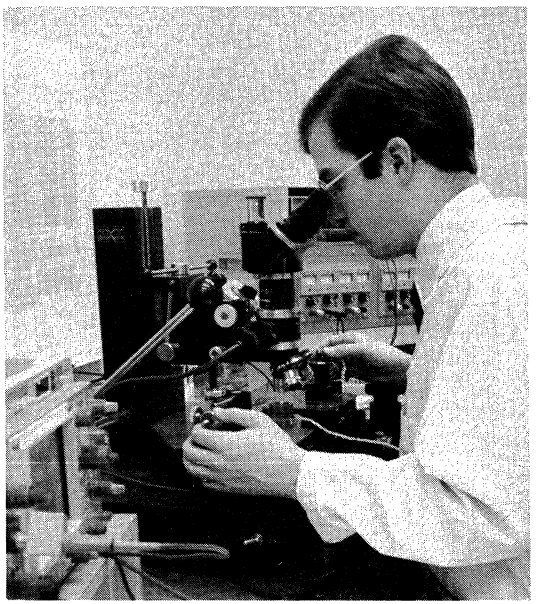
Test conditions used in the retentivity evaluation are at or exceed worst case specification conditions: maximum endurance stress of the entire memory, and maximum temperature biased or unbiased storage. The non-volatile memory is margined at regular intervals for projection of data retention time.

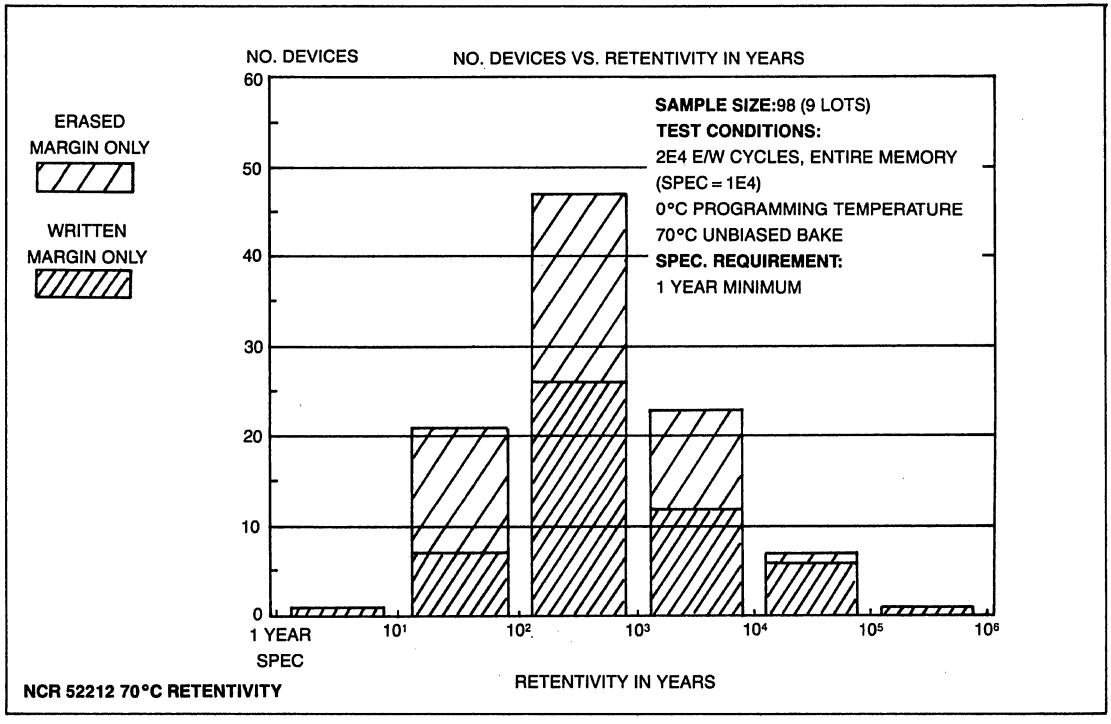
Data summarized below, and expressed in histograms in the following pages, shows the retentivity performance of the samples randomly pulled for the on-going Reliability Monitor. This data is typical of NVRAMs and EEPROMs. As shown by the data, all components tested exceed the retentivity requirement of their specification.

The specified maximum 10^4 erase/write cycles will conservatively ensure a minimum data retentivity of 1 year for NVRAMs and 10 years for EEPROMs. If the number of erase/write cycles exceeds 10^4, some degradation in retentivity can be expected.

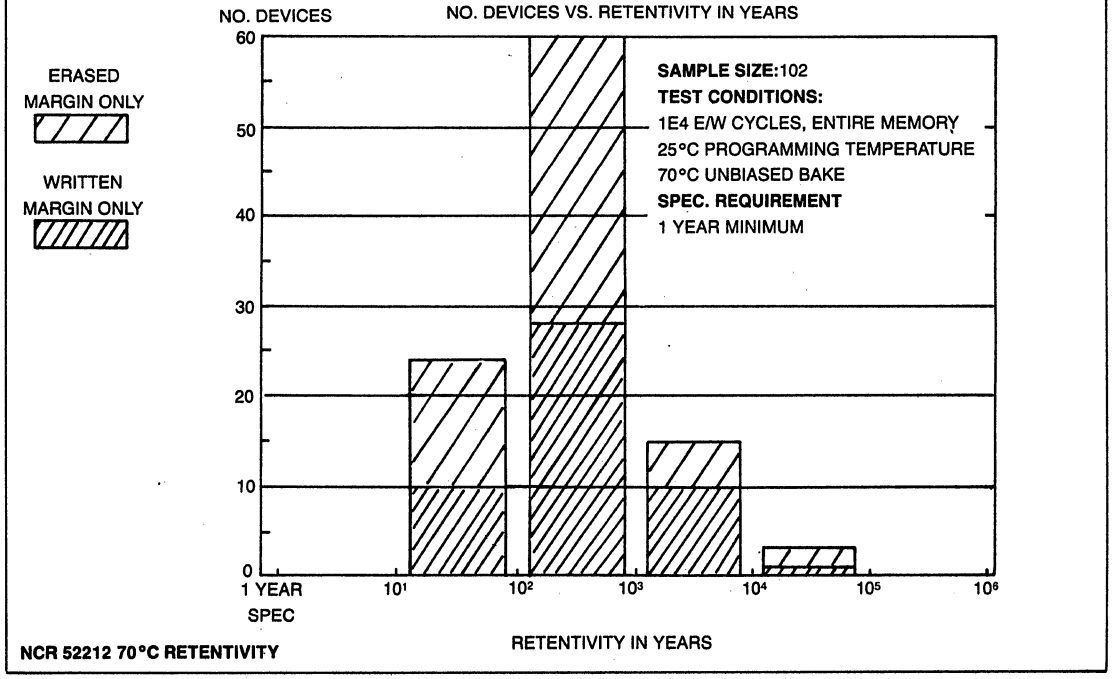
Retentivity Test Results:

	Number Tested	Test Condition	Retentivity: Worst Case	Median	Spec. Requirements
Typical NVRAM	98	70°C unbiased bake 2E4 E/W	7 yrs.	500 yrs.	
	102	70°C unbiased bake 1E4 E/W	15 yrs.	500 yrs.	1 yr. at 70°C 1E4 E/W
	44	Biased at 70°C 1E4 E/W	22 yrs.	500 yrs.	
Typical EEPROM	20	125°C unbiased bake 1E4 E/W	500 yrs.	1500 yrs.	10 yrs. at 70°C for commercial product. 10 yrs. at 105°C for automotive. 1E4 E/W for all.



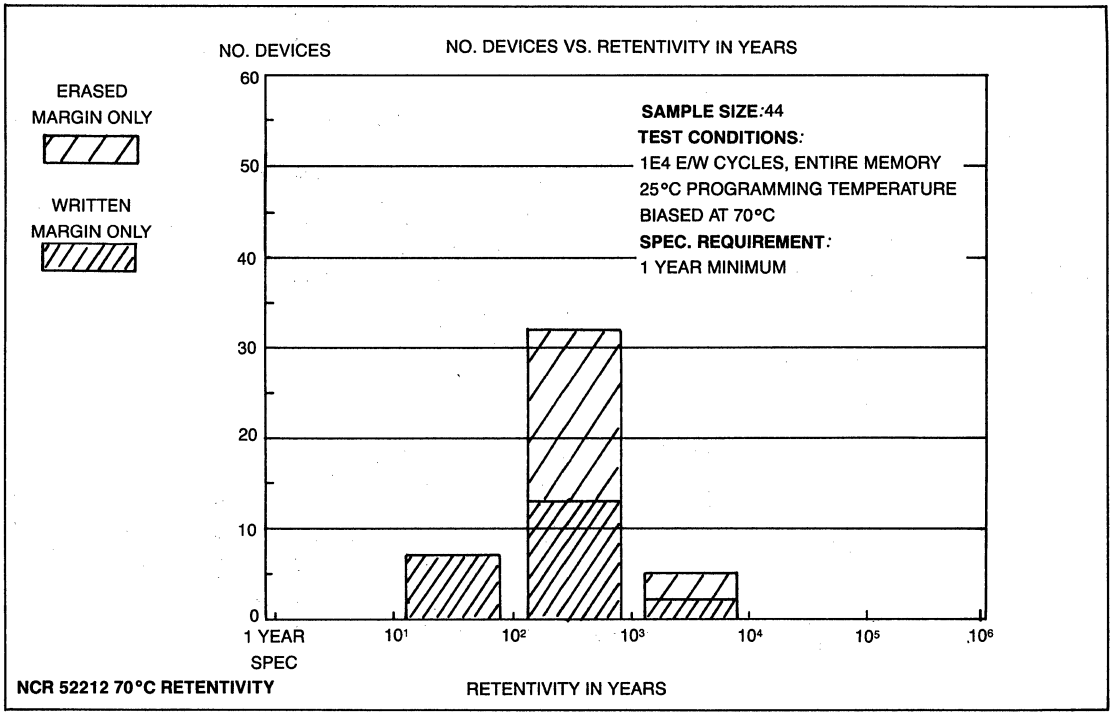


NCR 52212 70°C RETENTIVITY

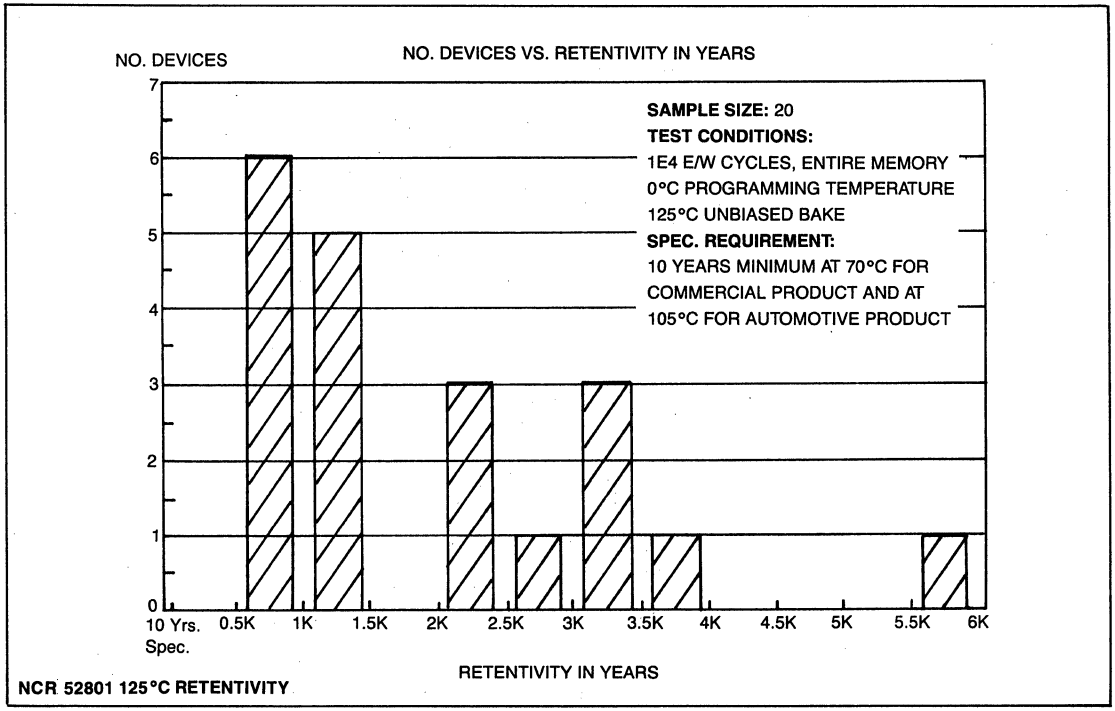


NCR 52212 70°C RETENTIVITY

SNOS Non-Volatile Memory Reliability



NCR 52212 70°C RETENTIVITY



NCR 52801 125°C RETENTIVITY

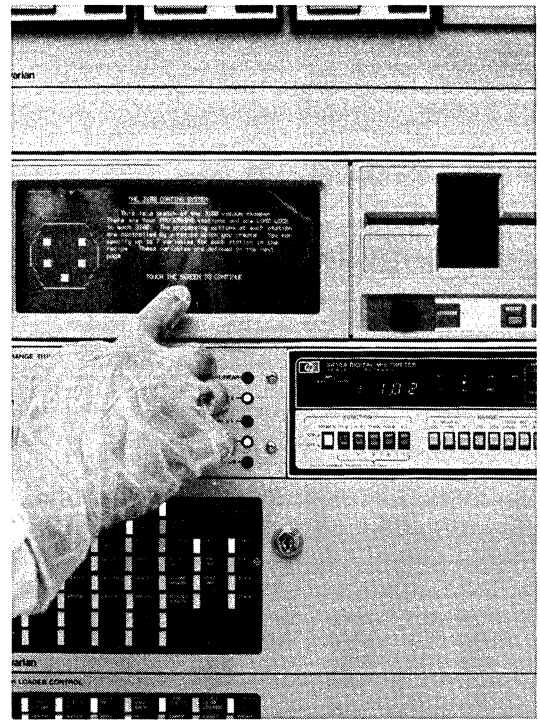
Endurance

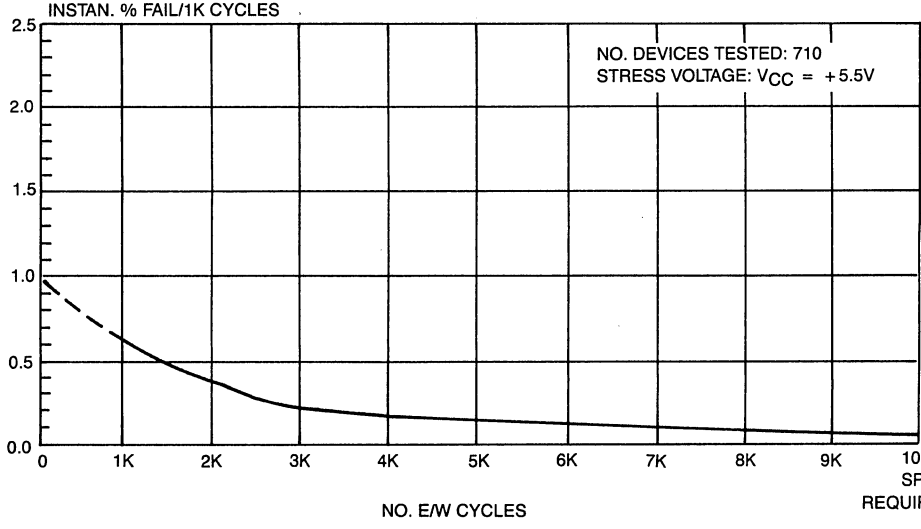
Endurance (erase/write cycling) capability is the measurement of the maximum number of erase/write cycles or programming operations that may be performed before component failure occurs.

In the evaluation, the entire memory is erase/write cycled with V_{CC} at its maximum voltage of +5.5 volts.

In the accompanying illustration, the typical endurance performance of SNOS non-volatile components is presented with the instantaneous % fail/1000 cycles plotted against the total number of erase/write cycles. Data shows that the instantaneous failure rate decreases at increased numbers of erase/write cycles over the specified range of 10^4. As mentioned previously, the major cause of failure has been found to be nitride breakdown due to random defects. Failures caused by nitride breakdown are catastrophic as exhibited by the inability to change data.

Endurance failure is the most common failure mode for all non-volatile components in the industry. However, with processing and screening enhancements in place, the endurance failure rate of NCR SNOS non-volatile components has been reduced to the low levels shown in the endurance performance plot below. As we continue to refine our processing techniques, it is anticipated that the failure rate can be reduced to even lower levels.





NCR 52212 ERASE/WRITE CYCLING PERFORMANCE

Temperature Humidity Bias

This test evaulates the moisture performance of plastic components by accelerating the moisture induced corrosion of metallization. Test samples are biased at +5.0 Volts in the static HTRB configuration in a 85°C/85°% relative humidity chamber.

The test results summarized below show that the controls employed in manufacturing for glassivation integrity (phosphorous concentration and pin-hole monitors) and plastic packaging are very effective.

85°C/85%RH Test Results:

Part Type	Package Type	Number Tested	Results: No. Failed 24 Hrs	120 Hrs	336 Hrs	1000 Hrs
NCR 52212/10	18 Pin Plastic	239	0	0	0	0
NCR 52801	14 Pin Plastic	136	0	0	0	0
Combined		375	0	0	0	0

Pressure Cooker

This test evaluates the moisture performance of plastic components by using a combination of temperature, humidity, and pressure to accelerate moisture ingress along the lead-frame-molding-compound-interface path. Test samples are stored without bias at 121°C and 1 atmospheric (gauge) pressure.

As in the case of Temperature Humidity Bias, the Pressure Cooker test results indicate good moisture performance of the NCR plastic components.

Pressure Cooker Test Results:

Part Type	Package Type	Results: No. Failed/No. Tested 24 Hrs	48 Hrs	96 Hrs	144 Hrs	192 Hrs
NCR 52801	14 Pin Plastic	0/104	0/104	0/104	0/104	0/104
		0/29	0/29	0/29	0/29	—
		0/48	0/48	1/48	—	—
		0/110	—	—	—	—
NCR 52212	18 Pin Plastic	0/45	0/45	0/45	1/45	
Combined		0/336	0/226	1/226	1/178	0/104

Temperature Cycle

This test is performed to accelerate the effects of thermal expansion mismatch among the different components within a specific packaging system. Test samples are temperature cycled from −65°C to +150°C, air to air, using MIL STD 883C, Method 1010.5, Condition C.

Temperature Cycle Test Results:

Part Type	Results: No. Failed/No. Tested		
	10 Cycles	100 Cycles	1000 Cycles
NCR 52212	0/312	0/77	—
NCR 52210	0/81	—	—
NCR 52801	0/184	0/107	0/77

Thermal Shock

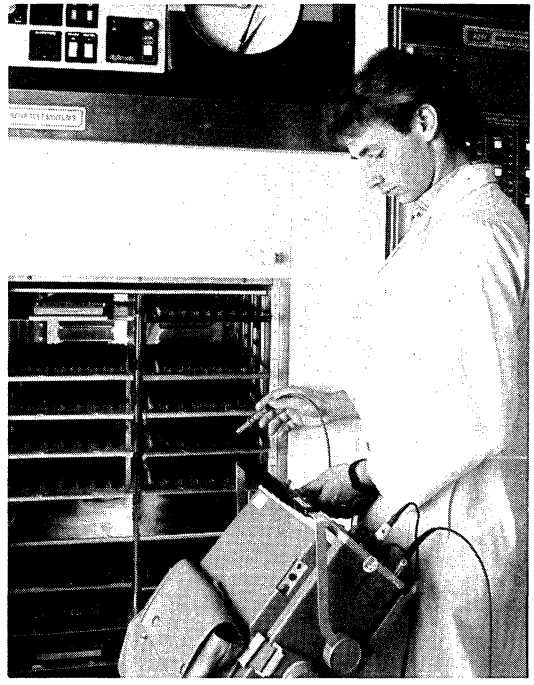
The objective of Thermal Shock is the same as that for Temperature Cycle. The differences between the two tests are that the temperature change is more sudden and that the thermal conductivity of the media used is higher in Thermal Shock. Test samples are transferred from one liquid medium at −65°C to another liquid medium at +150°C, using MIL-STD-883C, Method 1011.4, Condition C.

Thermal Shock Test Results:

Part Type	Results: No. Failed/No. Tested	
	20 Cycles	100 Cycles
NCR 52212	0/234	—
NCR 52210	0/81	—
NCR 52801	0/77	0/77

Summary

NCR Microelectronics manufactures high quality and reliable non-volatile components. Stringent process/assembly controls and thorough testing are employed to assure quality and to build-in reliability. Attention to detail is emphasized throughout the manufacturing process, from the inspection of incoming materials to the thorough testing of final products. Most important of all, NCR works closely with users to ensure fitness for use through closed-loop corrective action. Total commitment to quality, reliability, and customer support is the philosophy of all NCR people.



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Microprocessor Interface to the NCR Bytewide EEPROMs

APPLICATION NOTE

INTRODUCTION

The NCR 52832 and 52864 five volt only, Electrically Erasable PROMS (EEPROMS) are used in applications where occasional in-system programmability and long term data retention without power (non-volatility) are required. Some of these applications include storage of programmable character fonts in intelligent terminals, storage of data or firmware in remote systems that require periodic updating, user programmable video games, and RAM backup.

SEMICONDUCTOR TECHNOLOGY

NCR's Silicon-Nitride-Oxide-Silicon (SNOS) process allows for an infinite number of reads while achieving access times of less than 300ns. Also, the 528NN family boasts 10 year data retention and 10^4 erase/write cycles. Finally, the N channel process supports 5V only operation and is directly compatible with NMOS and TTL signal levels.

The SNOS memory cell stores data by trapping charge in the oxide-nitride gate dielectric. On-chip charge pumps generate the high voltage write and erase signals that rapidly inject and remove the charge necessary for long term data storage.

DEVICE DESCRIPTION

Mechanical

The 528NN family is compatible with the 28 pin JEDEC standard for bytewide memory products. Therefore, a 28 pin socket could easily be configured to accept the 52832, 52864 or any of the many other ROMs and RAMs conforming to the industry standard. Along with the commercial version, the 52832 and 52864 are available in industrial and military versions with no degradation in data retention.

Operation

The five functional modes of the 528NN family are described below. Table 1 summarizes the role of each control signal for each mode.

Read Mode

The 52832 is read like a conventional static RAM. Valid data is available on the output pins when a valid address is provided and $\overline{CS}$ and $\overline{OE}$ are brought low. If the address lines change while $\overline{CS}$ and $\overline{OE}$ are maintained low, valid data will be available after a delay of t_{ACC}.

Chip Erase Mode

Chip erase is accomplished by holding CNTL1 high and CNTL2 low followed by bringing $\overline{CS}$ and $\overline{OE}$ low. During chip erase all data and address lines are "don't care". An erased state corresponds to a logical "0".

Page Erase Mode

Page (16 bytes) erase is accomplished in a manner similar to chip erase except that $\overline{OE}$ is held high and $\overline{WE}$ is brought low, and a page address (A_4-A_{12}) must be provided. As in chip erase, the data lines are "don't care" and the erased state corresponds to a logical "0".

Load Data Mode

During the load data mode, data is loaded into 16, 8-bit internal latches. In this mode, data is loaded much the same way as it is for a SRAM. Both CNTL lines are held low while "clocking" $\overline{CS}$ and $\overline{WE}$. Addresses and data must be valid while $\overline{CS}$ and $\overline{WE}$ are low. The load data mode must be followed by a write mode to prevent losing the data that has been loaded in. Data may be loaded and then written 1 to 16 bytes at a time. The A_4-A_{12} address bits of the last byte loaded is the address the EEPROM latches as the page address. It is not necessary that the data bytes within a page be loaded in order of their addresses (e.g., A_0-A_3 are valid for each byte).

Write Mode

Data can be written into non-volatile cells by holding CNTL2 high and maintaining CNTL1 low while $\overline{CS}$ and $\overline{WE}$ are brought low. Data and address lines are "don't care" during a write cycle.

Table 1

Mode	$\overline{OE}$	$\overline{WE}$	CNTL1	CNTL2	$\overline{CS}$
STANDBY	X*	X	H	H	H
READ	L	H	H	H	L
CHIP ERASE	L	H	H	L	L
PAGE ERASE	H	L	H	L	L
LOAD DATA	H	L	L	L	L
WRITE	H	L	L	H	L

*X = don't care
L = V_{IL}
H = V_{IH}

APPLICATION

Figures 1 and 2 illustrate typical microprocessor interfaces to the 528NN family. The straightforward interface to the 8085 seen in Figure 1 is generally applicable to the Z80, NSC800, 8088, and 8086 family of microprocessors. Similarly, figure 2 shows a standard interface to the 6502 which is also useful in interfacing the 528NN family to the 6500, 6802, and 6809 processors.

In many systems, it is essential that the critical inputs to non-volatile memories be held inactive during power supply ramp-up and ramp-down to avoid inadvertent writes and erases to the memory cells. Figures 1, 2 and 3 incorporate effective and inexpensive circuits assuring that the CNTL lines of the 528NN family are held high during power supply transition. In figures 1 and 2, the 74HCT374 octal flip-flop has the useful qualities of having TTL compatible inputs along with outputs that will remain tri-stated down to $V_{CC} = 2V$. Since most non-volatile memories cannot erase or write data at $V_{CC} < 2.5V$, the active low inputs critical to the data storage functions are pulled high when the power supply is between approximately 4.4V and 2.5V. The circuit controlling the $\overline{OE}$ input to the 74HCT374 assures that its outputs are tri-stated when $2.0V < V_{CC} < 4.4V$ by turning the transistor off during this time and allowing $\overline{OE}$ to follow V_{CC}. In this situation, the CNTL inputs of EEPROM will be logic high via the 1K pull-up resistors. Of course, when $V_{CC} > 4.4V$ the zener diode conducts and forward biases the transistor which pulls $\overline{OE}$ low and in turn enables the outputs of the 74HCT374 to follow its inputs.

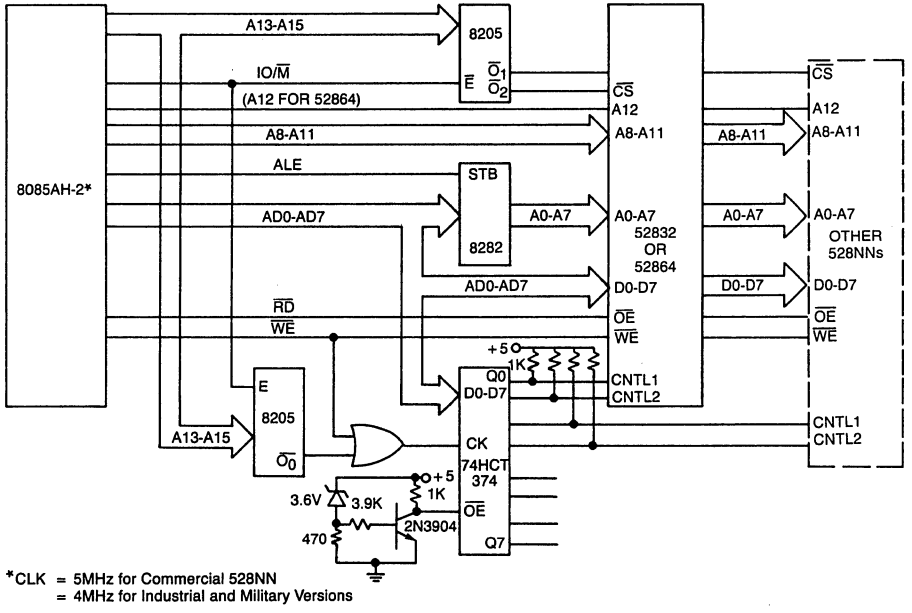

Figure 1. 8085 Interface to the 528NN

If only one 528NN is used in a system, an even less expensive circuit can be utilized in avoiding inadvertent memory writes and erases as illustrated in figure 3. At $V_{CC} = 5V$, the power sense circuitry is isolated from the CNTL inputs of the 528NN by D_1 and D_2. In this mode, the 10KΩ resistors are essentially in series with the high impedance MOS inputs and add a maximum of 100ns to the CNTL line set-up time. When the power supply is in transition between 4.4 and 2.5 volts, the transitor is turned off and the 470Ω pull-up resistor guarantees that a valid logic high is on the inputs of the 528NN regardless of the states of the MODE inputs from the microprocessor.

Basically, the usual mode of operation in both designs is the Read Mode. In this mode, control lines CNTL1 and CNTL2 are latched in the high state by the 74HCT374 and memory reads are conducted according to the standard timing constraints of the 8085 and the 6502 respectively. To perform a Read on the 528NN, simply select the part by decoding the appropriate address bits and pulling $\overline{CS}$ low, and read any address location by pulling $\overline{OE}$ low with the $\overline{RD}$ line. To avoid possible bus contention with faster memories in the 6502 system, R/$\overline{W}$ should be gated with the ϕ_2 clock (E on the 6802 family) to generate a $\overline{RD}$ signal, as seen in figure 2. With access times of 300ns, the 528NN family can be operated without wait states at up to 5MHz by the 8085AH and up to 1.8 MHz by the 6502-C. It is suggested that the CNTL lines be held high between Read cycles to avoid inadvertently beginning an Erase or Write cycle during address transitions, and to avoid having to wait the required 500ns CNTL line set-up time before beginning the next read cycle.

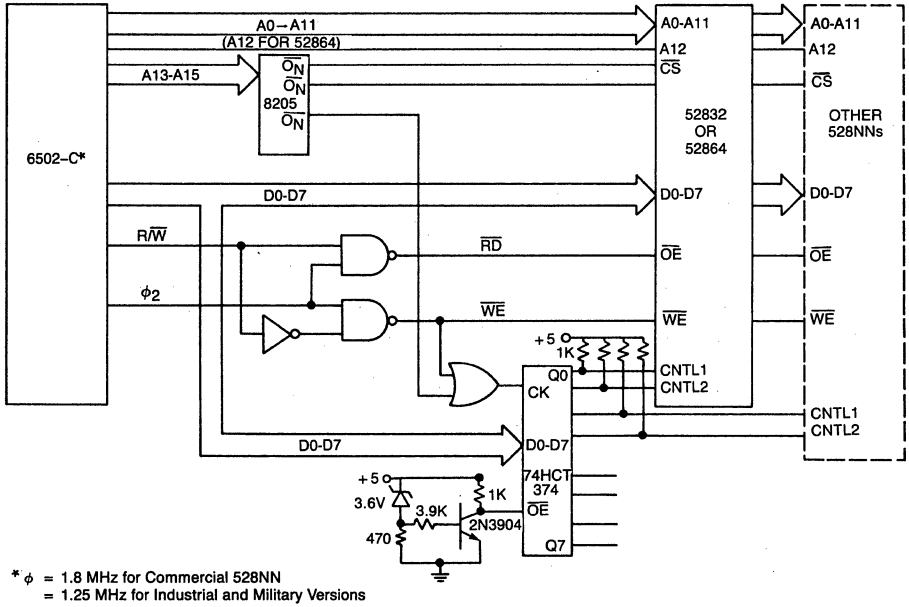

Figure 2. 6502 Interface to the 528NN

In addition to the standard Read function, data storage is accomplished by the following steps: first, erasing a page (16 bytes) or the whole chip by performing a Page Erase or Chip Erase function; second, loading a new page of data into the internal latches by performing a Load Data function; third, writing the new page of data into EEPROM by performing a Write function; and fourth, repeating steps two and three for each page erased.

Outlined below are a few system timing requirements involved in erasing and programming the 528NN family:

1. After a Chip or Page Erase has begun, the CNTL lines must remain stable in the Chip or Page Erase mode for at least 100 ms but not more than 200 ms. This allows adequate time for cycle completion.
2. After an Erase or a Write, it is necessary to wait at least 50μs after the CNTL lines change before beginning the next cycle. This permits time for the high voltages to bleed off.
3. After a 1 to 16 byte Load Data cycle is executed, the CNTL lines must go directly into the Write Mode to avoid clearing the data buffers.
4. If or when the control lines change states after a Load Data or Read cycle, it is essential to wait at least 500ns before initiating the next cycle, even if it is a Read cycle.
5. A Write function dictates that the control lines remain in the write mode for at least 10ms but no more than 20ms after its initiation.

Shorter erase times and write times are useful for storing data in applications where limited erase/write time is available such as in power fail situations. Longer erase and write times will result in longer data retention.

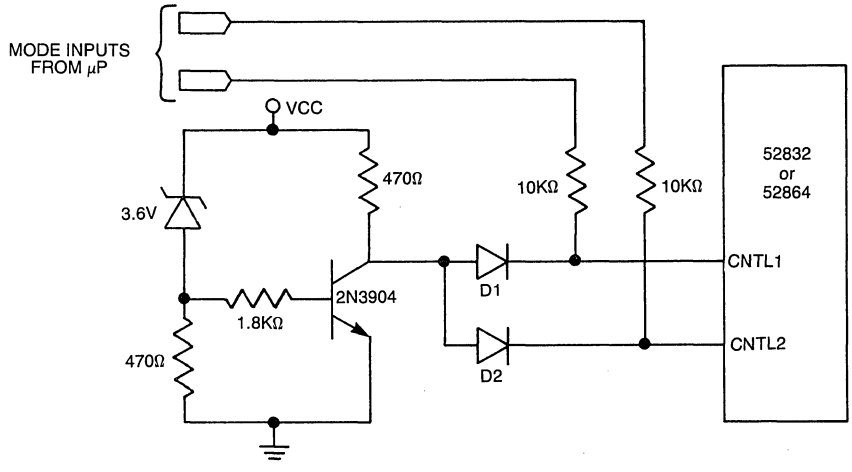

Figure 3. Low Cost power Up/Power Down Protection for One EEPROM

The flow chart in Figure 4 illustrates how system firmware can be structured according to the timing requirements for programming the 528NN family.

Finally, Figure 5 illustrates an 8080/8085/Z80/NSC800 program that erases a 4K block of 52832 EEPROM and then transfers data from a block of RAM into the block of EEPROM. This routine assumes the following:

1. An 8085 is running at 5MHz
2. Addresses 0 - IFFF are ROM
3. Addresses C000 - CFFF are RAM
4. Addresses 2000 - 2FFF are a 52832 EEPROM

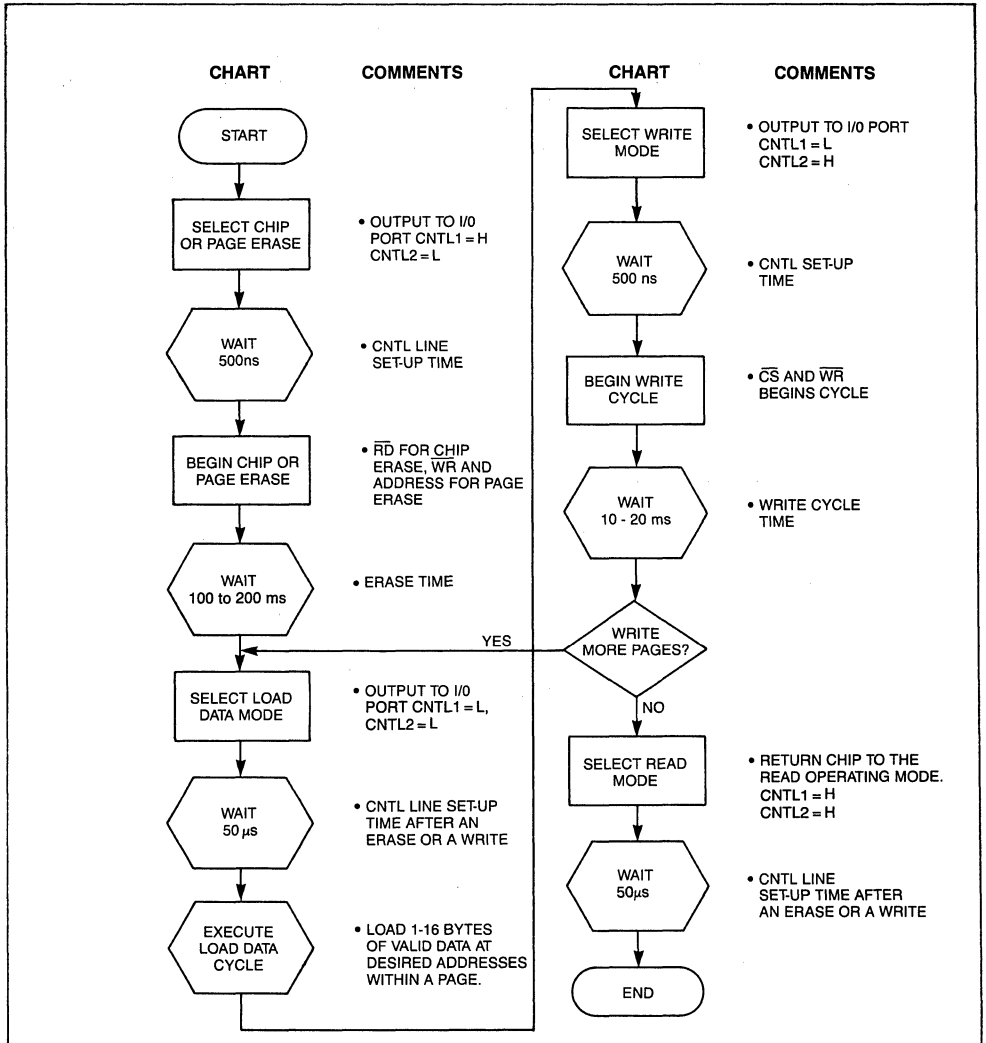

Figure 4. Flow Chart—Programming the 528NN Family

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LOC  OBJ        SEQ         SOURCE STATEMENT

1000              1         ORG 1000H
1000 2100C0       2 BLXFER: LXI H,0C000H     ;LOAD RAM STARTING ADDRESS
1003 110020       3         LXI D,2000H      ;LOAD EEPROM STARTING ADDRESS
1006 3EFD         4         MVI A,0FDH       ;SELECTS CHIP ERASE MODE
1008 D300         5         OUT 00H
100A 00           6         NOP              ;WAIT 500NS FOR CNTL LINE SETUP
100B 3A0020       7         LDA 2000H        ;DUMMY READ TO START CHIP ERASE
100E CD4C10       8         CALL ERATIM      ;WAIT 100MS FOR ERASE COMPLETION
1011 0E00         9         MVI C,00H        ;PAGE COUNT=256 PAGES
1013 3EFC        10 LDPG:   MVI A,0FCH       ;SELECT LOAD DATA MODE
1015 D300        11         OUT 00H
1017 CD3B10      12         CALL SUTIM       ;WAIT 50µS CNTL LINE SETUP
                 13                          ;AFTER AN ERASE OR WRITE
101A 0610        14         MVI B,10H        ;BYTE COUNT FOR 1 PAGE OF DATA
101C 7E          15 LDBYTE: MOV A,M          ;READ DATA FROM RAM LOCATION
                 16                          ;SPECIFIED BY H-L
101D 12          17         STAX D           ;WRITE DATA TO EEPROM LOCATION
                 18                          ;SPECIFIED BY D-E
101E 23          19         INX H            ;INCREMENT RAM ADDRESS FOR NEXT
                 20                          ;TRANSFER
101F 13          21         INX D            ;INCREMENT EEPROM ADDR FOR
                 22                          ;NEXT TRANSFER
1020 05          23         DCR B            ;DECREMENT BYTE COUNT
1021 C21C10      24         JNZ LDBYTE       ;IF COMPLETE PAGE IS NOT YET
                 25                          ;LOADED, GET NEXT BYTE
1024 3EFE        26 WRTPG:  MVI A,0FEH       ;COMPLETE PAGE IS LOADED,
                 27                          ;SELECT WRITE MODE
1026 D300        28         OUT 00H
1028 00          29         NOP              ;500NS CNTL LINE SETUP
                 30                          ;AFTER A LOAD CYCLE
1029 320020      31         STA 2000H        ;DUMMY WRITE TO START WRITE CYCLE
102C CD4210      32         CALL WRTIM       ;WAIT 10MS FOR WRITE COMPLETION
102F 0D          33         DCR C            ;DECREMENT PAGE COUNT
1030 C21310      34         JNZ LDPG         ;LOAD NEXT PAGE UNTIL ALL
                 35                          ;PAGES LOADED AND WRITTEN
1033 3EFF        36 RDMD:   MVI A,0FFH       ;SELECT READ MODE AFTER CHIP
                 37                          ;(ALL PAGES) IS WRITTEN
1035 D300        38         OUT 00H
1037 CD3B10      39         CALL SUTIM       ;50µS CNTL LINE SETUP TIME
                 40                          ;AFTER A WRITE CYCLE
103A C9          41         RET              ;RETURN FROM EEPROM PROGRAM
                 42                          ;ROUTINE
                 43 ;
                 44 ;
                 45 ;THE FOLLOWING ROUTINES ARE THE SOFTWARE TIMERS FOR
                 46                  ;A 5MHZ 8085
                 47 ;
                 48 ;
103B 3E16        49 SUTIM:  MVI A,22D        ;=>51.8µS TIMER FOR CNTL
                 50                          ;LINE SETUP TIME AFTER AN ERASE
                 51                          ;OR A WRITE
103D 3D          52 TIMRA:  DCR A
103E C23D10      53         JNZ TIMRA
1041 C9          54         RET
1042 06BA        55 WRTIM:  MVI B,186D       ;186*54µS=>10MS WRITE CYCLE TIMER
1044 CD3B10      56 TIMRB:  CALL SUTIM       ;=>52µS DELAY
1047 05          57         DCR B
1048 C24410      58         JNZ TIMRB
104B C9          59         RET
104C 0E0A        60 ERATIM: MVI C,10D        ;10*10MS=>100MS ERASE CYCLE TIMER
104E CD4210      61 TIMRC:  CALL WRTIM
1051 0D          62         DCR C
1052 C24E10      63         JNZ TIMRC
1055 C9          64         RET
1000             65         END 1000H



ASSEMBLY COMPLETE,   NO ERRORS
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Figure 5. 52832 Programming Routine

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Non-Volatile Applications - Memory Margining Nibble Wide NVRAMs - 52210, 52211, 52212

APPLICATION NOTE

Introduction

Among the many features offered by NCR in their nibble wide family of NVRAM's is memory margining. The memory margining feature allows the user to determine the length of time that an NVRAM will retain information stored in the EEPROM portion of the memory (An NVRAM is a combination of an SRAM and an EEPROM). The length of time that the EEPROM retains information (without being rewritten) is known as retention time.

This application note presents all the necessary information needed to margin and predict retention times for NCR'S family of nibble wide NVRAM'S.

Predicting Retention Time

Retention time for an NVRAM is determined by plotting the voltage measured during memory margining (V_M) versus the time (T) when the device was margined. As shown in the example retention plot, at least two points (two each for both 1's and 0's) must be plotted to predict retention time. Since the relationship between V_M and T is generally logarithmic, the data should be plotted on semi-log paper. Plot V_M on the y-axis and T on the x-axis (this is the log axis). The following steps outline the procedure used to collect the data needed to predict both 1's and 0's retention times.

1. Write a known pattern into the static RAM (SRAM). A checkerboard (CB) pattern is generally preferred because it allows the user to margin both 1's and 0's with the same pattern. A description of how a checkerboard pattern is generated for each of the nibble wide NVRAM's has been included in this application note.

NOTE: Although the same pattern may be used, 1's and 0's must be margined separately. That is, all steps required to generate both data points for the 1's margin must be completed and the CB pattern must be stored again in the EEPROM before margining of the 0's can begin. The reason for this is that the margining of one state disturbs the margin of the other state.

2. Store the checkerboard pattern (CB) into the EEPROM.
3. Recall the CB pattern to the SRAM.
4. Read the CB pattern from the SRAM. (Steps 3 and 4 need to be done to ensure that the CB pattern has been stored correctly.)
5. Bake the device under test (DUT) for 96 hours at 70°C. (The device should be baked at the upper temperature limit of the device's specification. This is the worst case temperature for retention characteristics. For a commercial device 70°C is chosen.) The bake should be an unbiased bake with the device placed in antistatic foam or other conductive material.
6. Margin 1's. (The Memory Margining section outlines the technique employed to margin both 1's and 0's.) Record V_M, the voltage determined during margining, and the exact number of hours (to the nearest hour) since the pattern was stored in the EEPROM. The data collected at this point should be recorded as $V_{M1(one's)}$ and $T_{1(one's)}$.

7. Bake the device for an additional 408 hours at 70°C. (The total bake is 504 hours with data collection at 96 and at 504 hours.)
8. Margin 1's. Record $V_{M2(one's)}$ and $T_{2(one's)}$.
9. Plot $T_{1(one's)}$, $T_{2(one's)}$, $V_{M1(one's)}$, $V_{M2(one's)}$ to determine the 1's retention characteristics of the DUT. This is illustrated in the example retention plot.
10. Repeat steps 1 thru 5. (1's margining was completed in step 9. Steps 10 thru 14 address 0's margining.)
11. Margin 0's. Record $V_{M1(zero's)}$ and $T_{1(zero's)}$.
12. Bake the DUT for an additional 408 hours at 70°C. (Same as step 7).
13. Margin 0's. Record $V_{M2(zero's)}$ and $T_{2(zero's)}$.
14. Plot $T_{1(zero's)}$, $T_{2(zero's)}$, $V_{M1(zero's)}$, and $V_{M2(zero's)}$.

NOTE: The following conditions are recommended for writing, storing, reading, and recalling the DUT.

V_{CC} = 5.0V $V_{IL} \leq$ 0.8V
$V_{IH} \geq$ 2.0V T_A = Room Temperature

In addition to plotting the data to determine retention time, the following equation can be used to predict V_M at 1 year. That is, the equation will predict the remaining 1's or 0's margin after one year of storage.

$$V_{M(1\ yr)} = \left[\left(\frac{V_{M2}-V_{M1}}{\log_{10} T_2 - \log_{10} T_1}\right)(3.94 - \log_{10} T_1)\right] + V_{M1}$$

NOTE: The times (T) must be in hours.

The device will recall correctly at one year if the following inequalities are met.

$$V_{M(one's)} \text{ @ 1 yr.} > OV$$

$$V_{M(zero's)} \text{ @ 1 yr} < OV$$

STORE and WE

During memory margining a voltage must be applied to each of the memory capacitors in the DUT. To achieve this, STORE (pin 9) and WE (pin 11) are utilized. STORE takes on the additional function of Margin Enable (ME) and WE takes on the additional function of Margining Voltage (MV). Timings and voltage limits for these pins may be found in the AC Characteristics section. In the interest of clarity, these pins will be denoted as STORE (ME) and WE (MV) in this application note.

Memory Margining

Information is retained in the EEPROM portion of the NVRAM by storing a charge in each of the memory capacitors. This storage of charge is reflected in a change of the threshold voltage (V_{TH}) of the memory capacitor. The rate at which V_{TH} decays is directly related to the retention time of an NVRAM. Unfortunately, V_{TH} cannot be measured directly. However, the voltage V_M, that is applied to the WE (MV) pin is used to determine the magnitude of V_{TH}. It is in this manner that V_{TH} is evaluated. The following steps outline the technique that is used to evaluate V_{TH} (using V_M) correctly.

NOTE: The following is the margining technique that is referred to in steps 6, 8, 11, and 13 in the Predicting Retention Time section. (This entire section must be performed in order to execute each of the steps listed above.)

1. Write an inverted checkerboard pattern (ICB) into the SRAM. (An ICB pattern is written into the SRAM at this point to ensure that each memory location will be forced to change state when the CB pattern is recalled from the EEPROM.)
2. Set up the STORE (ME) and WE (MV) pins for margining. See AC Characteristics for correct timings.
3. Apply the correct V_M to the WE (MV) pin. The next section, Performing a Binary Search, explains the method that must be used to generate the correct V_M. (Once the initial limits have been chosen for V_M, this step may be directly replaced by the second step in the Performing a Binary Search section.)
4. Recall the CB pattern to the SRAM. (This is the CB pattern that was stored in the EEPROM in step one of the Predicting Retention Time section.)
5. Set up the STORE(ME) and WE(MV) pins so the SRAM can be read.

6. Read the SRAM. If the SRAM verifies correctly, this iteration is considered a "pass"; if the SRAM does not verify correctly, this iteration is considered a "fail". A new V_M is generated based on whether the SRAM verified correctly or not, as shown in step 3 of the next section. (Once the binary search technique is understood this step may be replaced by the third step in the Performing a Binary Search section.)

NOTE: A device whose pattern does not verify correctly ("fails") does not mean that the device is no longer functioning correctly. When a device recalls incorrectly it means that the value of V_M has exceeded the value of V_{TH}, which is part of the margining technique.

7. Repeat steps 1 thru 6 eight additional times. (A total of nine iterations are needed to ensure the resolution of V_M.)
8. After the ninth iteration is complete, add the last pass limit and fail limit (as determined in step 6) together and divide by two. This is the V_M that should be recorded for plotting.

Performing a Binary Search

The binary search method must be used during memory margining to generate the margining voltage (V_M) for both 1's and 0's. This method is used because it is the most efficient way to accurately generate the margining voltage with the fewest number of iterations. (Applying V_M to the memory degrades the margin slightly, therefore as few iterations as possible are desired.)

The 1's margin search window is 0 to 6 volts; the 0's margin search window is 0 to -6 volts. In each case, nine margining iterations are used to determine the correct V_M within the appropriate window. A description of the binary search technique for determining the 1's margin voltage $V_{M(one's)}$ follows. (Determining $V_{M(zero's)}$ is the same except that the initial window is 0 to –6 volts.)

1. Begin with a "fail limit" of 6 volts and a "pass limit" of 0 volts. (The window between the pass and fail limits is the search window.)
2. Add the pass and fail limits together and divide by two. (The first V_M will be 3 volts). This is the manner in which the margin voltage is determined for each iteration.
3. If the device passes (that is, if the pattern recalls correctly as determined by steps 4, 5, and 6 of the preceding section) at the V_M determined in step 2 of this section, set the new pass limit equal to that V_M and keep the previous fail limit. If the device fails (does not recall correctly) at the V_M determined in step 2, set the new fail limit equal to that V_M and keep the previous pass limit.
4. Repeat step 2 to determine the new V_M.

To determine the 0's margin voltage, repeat the above procedure except begin with a fail limit of -6 volts and a pass limit of 0 volts.

The resolution of the margin voltage determined by the binary search method can be determined by the following equation.

$$V_M\,(\text{RESOLUTION}) = \pm \frac{L_F - L_P}{2^{i+1}}$$

where
L_F = fail limit
L_P = pass limit
i = number of iterations

For a 6 volt window and a total of 9 iterations, the resolution of the resultant V_M will be approximately ± 6 mV.

Pitfalls

— The resolution of V_M, the voltage that is applied to the $\overline{WE}$(MV) pin, is very important. To ensure accurate results the resolution of the V_M power supply should be no worse than ± 0.010mV.

— Nine binary search iterations must be performed to ensure the resolution of the V_M that is plotted. With nine iterations and a V_M power supply resolution of ± 0.010mV the overall resolution of V_M will be within ± 0.016mV.

— V_{ME}, the voltage applied to the $\overline{STORE}$(ME) pin during margining should be 24 ± 0.5V.

— 1's and 0's must be margined separately. That is, all steps required to generate both 1's margin data points must be completed and the CB pattern must be stored again in the EEPROM before margining of the 0's can begin.

— Write, store, read, and recall operations must meet the specification for the particular device being margined.

— Margining must be performed in accordance with the timings and voltages presented in the AC Characteristics section of this application note.

— The retention bake temperature should be chosen to match the upper temperature limit of the specification of the device being evaluated.

— The DUT should be margined within several (up to 4) hours after being removed from the retention bake.

— For the purpose of predicting retention times, the DUT should not be margined prior to 24 hours after a pattern has been stored in the EEPROM. The relationship between V_{TH} and T during the first 24 hours is generally log-log. Retention time predictions with one of the data points collected prior to 24 hours will be incorrect.

— For the purpose of this application note, a "1" may be considered to be a "written" state and a "0" to be an "erased" state. A discussion of the relationship between written and erased states and logical 1's and 0's may be found in the SNOS NONVOLATILE MEMORY RELIABILITY REPORT.

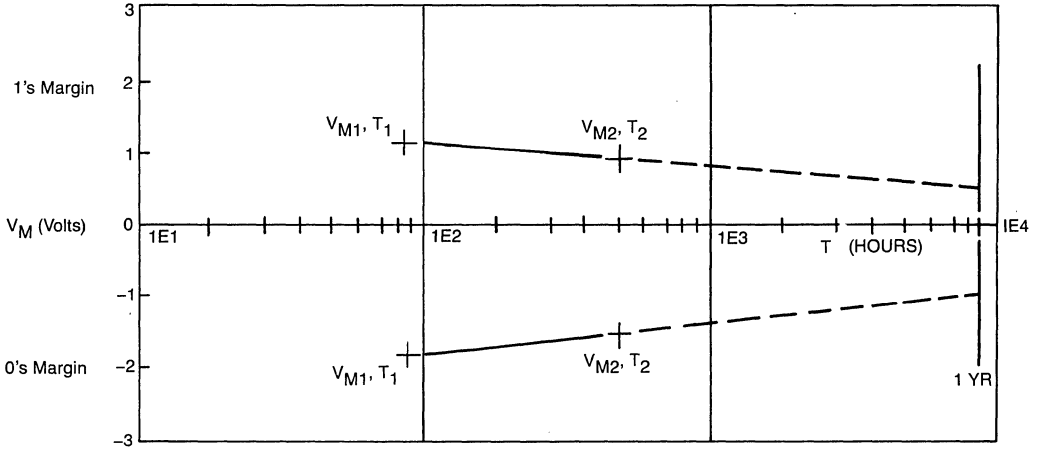
Predicting Retention - An Example

The following example is based on data collected from a sample of NCR 52212's. It is representative of the retention characteristics generated by any one of the products in NCR's family of nibble wide NVRAM's.

The 1's were margined at 94 and 506 hours, and the 0's were margined at 101 and 499 hours with the following results.

	T_1	T_2
1's Margin	1.140 V	0.980 V
0's Margin	–1.820 V	–1.580 V

The following plot was generated from the data. It shows approximately 0.7V of 1's margin and -1V of 0's margin at one year.



EXAMPLE RETENTION PLOT

In addition to plotting the data, the 1's and 0's margin (at 1 year) have been calculated below.

$$V_{M\ (one's)\ @\ 1\ yr.} = \left[\left(\frac{0.980 - 1.140}{\log_{10} 506 - \log_{10} 94}\right)(3.94 - \log_{10} 94)\right] + 1.140$$

$$= \left(\frac{-0.160}{0.731}\right)(1.967) + 1.140$$

$$= -0.431 + 1.140$$

$$= 0.709 \text{ Volts (1's margin)}$$

$$V_{M\ (zero's)\ @\ 1\ yr.} = \left[\left(\frac{-1.580-(-1.820)}{\log_{10} 499 - \log_{10} 101}\right)(3.94 - \log_{10} 101)\right] + (-1.820)$$

$$= \left(\frac{0.240}{0.694}\right)(1.936) + (-1.820)$$

$$= 0.669 + (-1.820)$$

$$= -1.150 \text{ Volts (0's margin)}$$

In both of the above examples, the inequalities $V_{M(one's)}$ @ 1 yr > 0V and $V_{M(zero's)}$ @ 1yr < 0V were met. This predicts that the DUT will recall both 1's and 0's correctly after one year of storage.

Writing a Checkerboard Pattern

NCR 52210

The memory array of NCR's 52210 64 x 4 bit nibble wide NVRAM consists of four data banks (one each for D0 thru D3). Each bank contains an 8 column by 8 row matrix (see memory map). Inputs A0-A2 are the row addresses and A3-A5 are the column addresses. Address 0 references the bit position in the upper lefthand corner of each data bank. Since the row addresses are less significant than the column addresses, address 1 is the bit position in row 1, column 0 (directly below address 0).

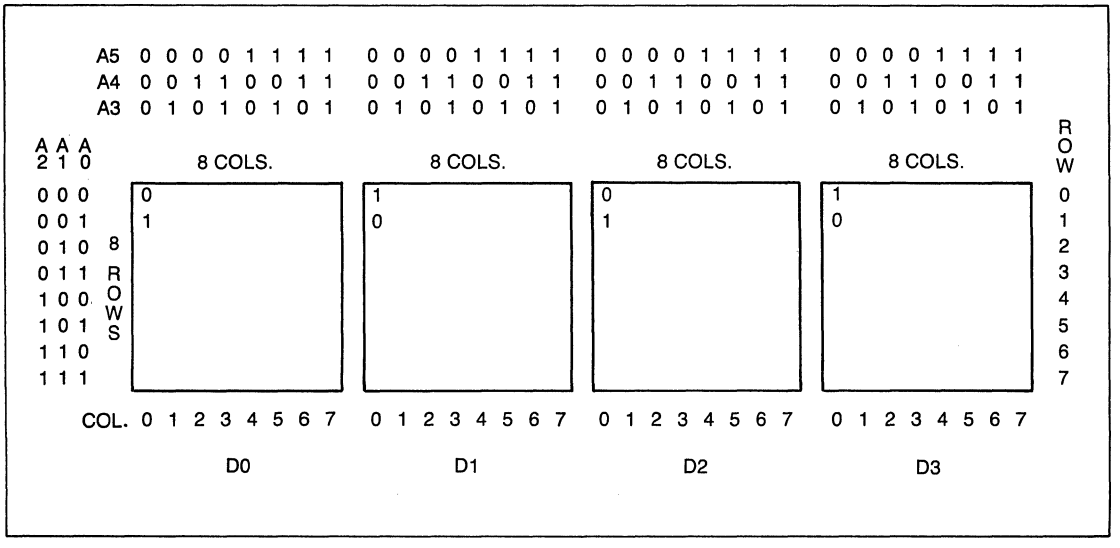
A checkerboard pattern resides in the SRAM array when adjacent memory cells contain complementary data. The procedure used to generate such a pattern is described below:

1. Begin at address 0 by writing the data 1010 (D0 is the least significant bit).
2. Increment the address and complement the data. (Address 1 data would be 0101.)

NOTE: Address 0 (data 1010) is shown in the upper left-hand corner of each data bank. Address 1 (data 0101)is shown just below address 0.

3. Write the complemented data.
4. Repeat steps 2 and 3 six additional times (until the last row is written).
5. Begin the next column by incrementing the address without complementing the data. Write the uncomplemented data.
6. Repeat steps 2, 3, and 4 until the column is completed.
7. Repeat steps 5 and 6 six additional times to complete the array.

An inverted checkerboard pattern may be generated by following the above procedure except that all the data must be complemented. (Address 0 for an inverted checkerboard would be 0101.)



NCR 52211

The memory array of NCR's 52211 128 x 4 bit nibble wide NVRAM consists of four data banks (one each for D0 thru D3). Each bank contains a 16 column by 8 row matrix (see memory map). Inputs A0-A2 are the row addresses and A3-A6 are the column addresses. Address 0 references the bit position in the upper left-hand corner of each data bank. Since the row addresses are less significant than the column addresses, address 1 is the bit position in row 1, column 0 (directly below address 0).

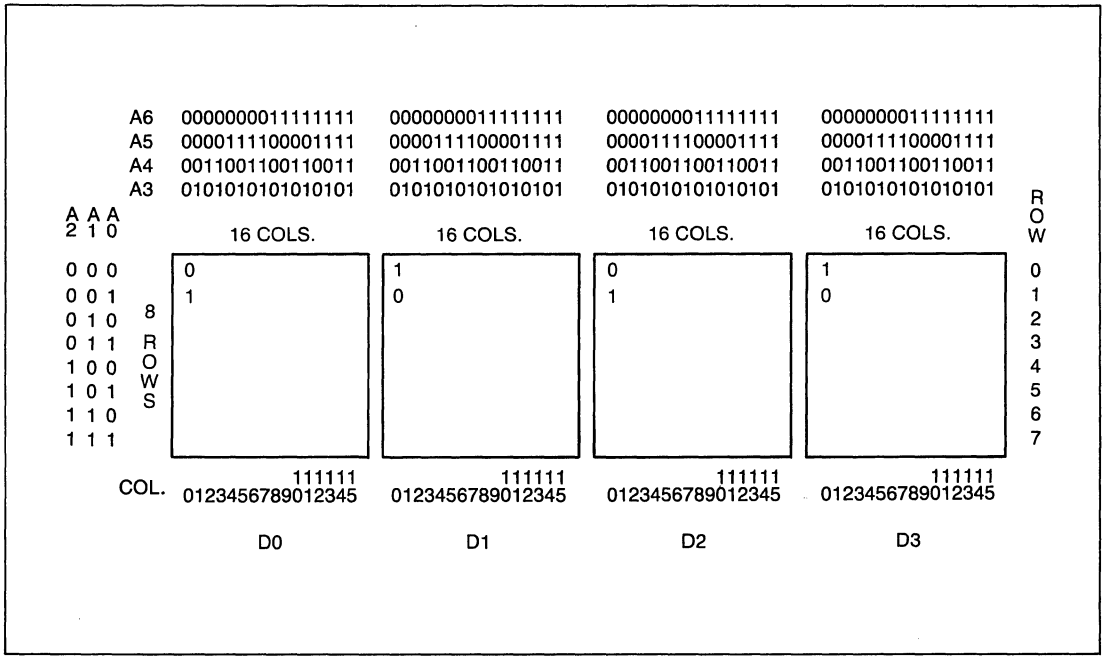
A checkerboard pattern resides in the SRAM array when adjacent memory cells contain complementary data. The procedure used to generate such a pattern is described below:

1. Begin at address 0 by writing the data 1010 (D0 is the least significant bit).
2. Increment the address and complement the data. (Address 1 data would be 0101.)

NOTE: Address 0 (data 1010) is shown in the upper left-hand corner of each data bank. Address 1 (data 0101) is shown just below address 0.

3. Write the complemented data.
4. Repeat steps 2 and 3 six additional times (until the last row is written).
5. Begin the next column by incrementing the address without complementing the data. Write the uncomplemented data.
7. Repeat steps 5 and 6 fourteen additional times to complete the array.

An inverted checkerboard pattern may be generated by following the above procedure except that all the data must be complemented. (Address 0 for an inverted checkerboard would be 0101.)



NCR 52212

The memory array of NCR's 52212 256 x 4 bit nibble wide NVRAM consists of four data banks (one each for D0 thru D3). Each bank contains a 16 column by 16 row matrix (see memory map). Inputs A0-A3 are the row addresses and A4-A7 are the column addresses. Address 0 references the bit position in the upper left-hand corner of each data bank. Since the row addresses are less significant that the column addresses, address 1 is the bit position in row 1, column 0 (directly below address 0).

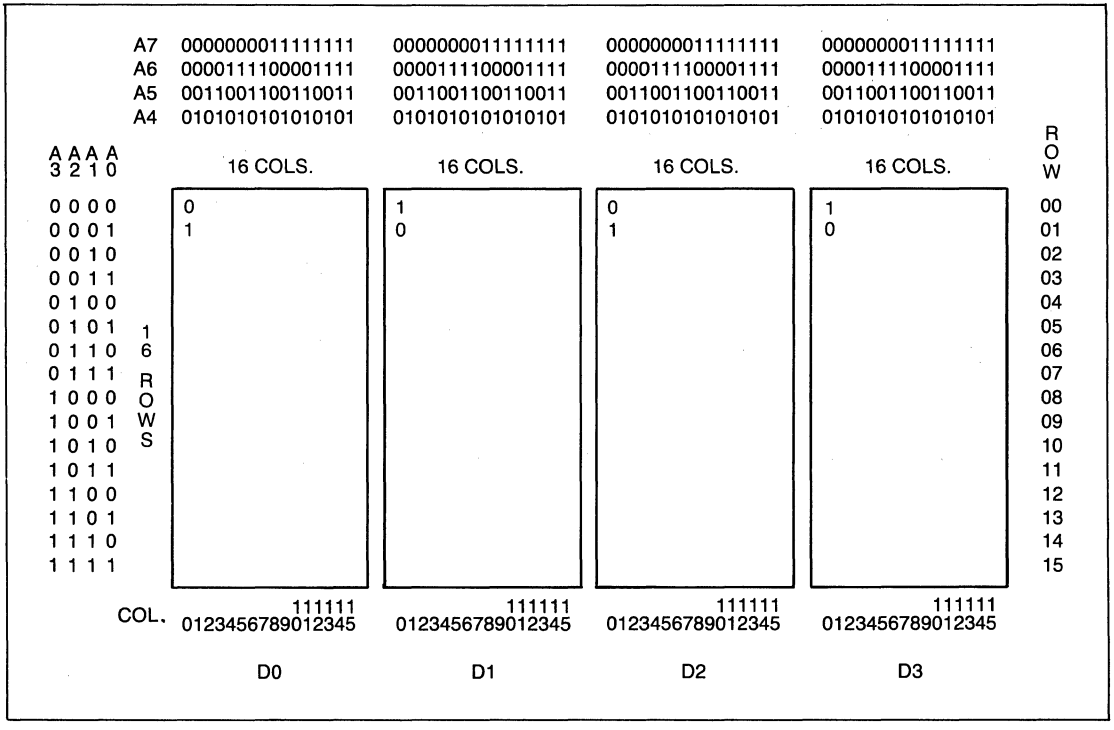
A checkerboard pattern resides in the SRAM array when adjacent memory cells contain complementary data. The procedure used to generate such a pattern is described below:

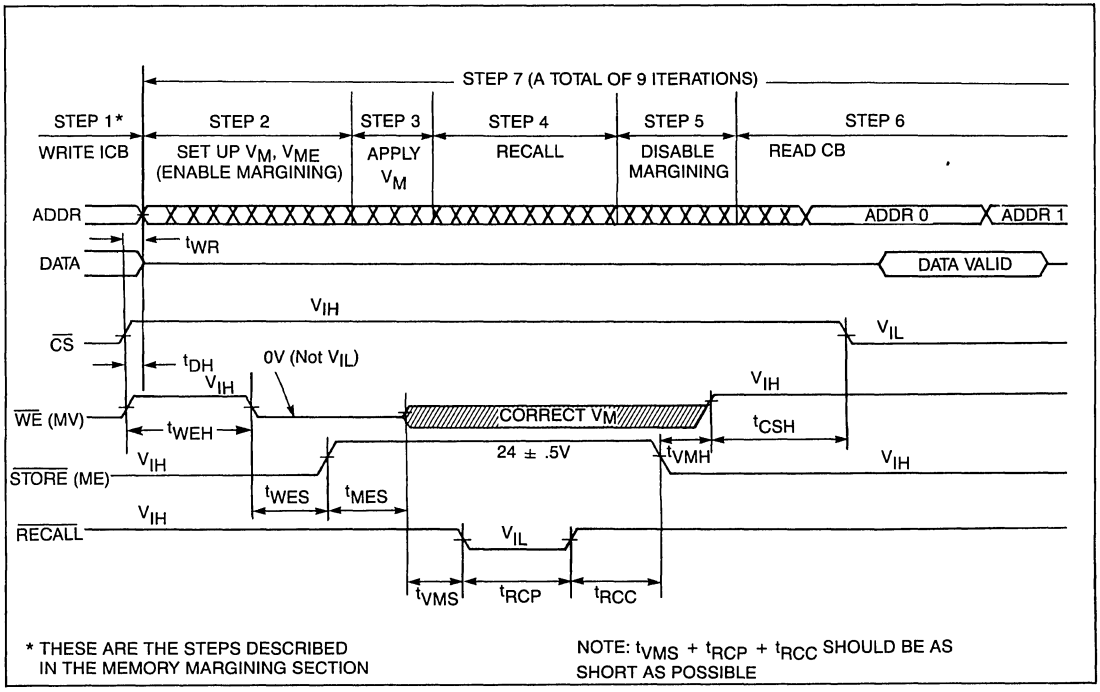
1. Begin at address 0 by writing the data 1010 (D0 is the least significant bit).
2. Increment the address and complement the data. (Address 1 data would be 0101).

NOTE: Address 0 (data 1010) is shown in the upper left-hand corner of each data bank. Address 1 (data 0101) is shown just below address 0.

3. Write the complemented data.
4. Repeat steps 2 and 3 fourteen additional times (until the last row is written).
5. Begin the next column by incrementing the address without complementing the data. Write the complemented data.
6. Repeat steps 2, 3, and 4 until the column is completed.
7. Repeat steps 5 and 6 fourteen additional times to complete the array.

An inverted checkerboard pattern may be generated by following the above procedure except that all the data must be complemented. (Address 0 for an inverted checkerboard would be 0101.)





* THESE ARE THE STEPS DESCRIBED IN THE MEMORY MARGINING SECTION

NOTE: $t_{VMS} + t_{RCP} + t_{RCC}$ SHOULD BE AS SHORT AS POSSIBLE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_M	MARGIN VOLTAGE	V_{CC} = + 5.0V	-6.0	*	6.0	V
V_{ME}	MARGIN ENABLE	V_{CC} = + 5.0V	23.5		24.5	V
t_{DH}	DATA HOLD FROM WRITE TIME		SEE APPROPRIATE SPECIFICATION			
t_{WEH}	WRITE ENABLE HOLD FROM CHIP SELECT		100			ns
t_{WES}	WRITE ENABLE SET-UP TO MARGIN ENABLE		0			ns
t_{MES}	MARGIN ENABLE SET-UP TO MARGIN VOLTAGE		50			μs
t_{VMS}	MARGIN ENABLE SET-UP TO ARRAY RECALL		250			μs
t_{RCP}	RECALL PULSE WIDTH		SEE APPROPRIATE SPECIFICATION			
t_{RCC}	ARRAY RECALL CYCLE TIME		SEE APPROPRIATE SPECIFICATION			
t_{VMH}	MARGIN VOLTAGE HOLD FROM RECALL CYCLE		0			ns
t_{CSH}	CHIP SELECT HOLD FROM END OF MARGIN VOLTAGE		100			ns
t_{WR}	WRITE RELEASE TIME		SEE APPROPRIATE SPECIFICATION			

AC CHARACTERISTICS

*See Binary Search section for correct V_M.

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Non-Volatile Applications - Memory Margining Byte Wide NVRAMs - 52001, 52002, 52004

APPLICATION NOTE

Introduction

Among the many features offered by NCR in their byte wide family of NVRAMs is memory margining. The memory margining feature allows the user to determine the length of time an NVRAM will retain information stored in the EEPROM portion of the memory (An NVRAM is a combination of an SRAM and an EEPROM). The length of time that the EEPROM retains information (without being rewritten) is known as retention time.

This application note presents all the necessary information needed to margin and predict retention times for NCR'S family of byte wide NVRAM'S.

Predicting Retention Time

Retention time for an NVRAM is determined by plotting the voltage measured during memory margining (V_M) versus the time (T) when the device was margined. As shown in the example retention plot, at least two points (two each for both 1's and 0's) must be plotted to predict retention time. Since the relationship between V_M and T is generally logarithmic, the data should be plotted on semi-log paper. Plot V_M on the y-axis and T on the x-axis (this is the log axis). The following steps outline the procedure used to collect the data needed to predict both 1's and 0's retention time.

1. Write a known pattern into the static RAM (SRAM). A checkerboard (CB) pattern is generally preferred because it allows the user to margin both 1's and 0's with the same pattern. A description of how a checkerboard pattern is generated for each of the nibble wide NVRAM's has been included in this application note.

NOTE: Although the same pattern may be used, 1's and 0's must be margined separately. That is, all steps required to generate both data points for the 1's margin must be completed and the CB pattern must be stored again in the EEPROM before margining of the 0's can begin. The reason for this is that the margining of one state disturbs the margin of the other state.

2. Store the checkerboard pattern (CB) into the EEPROM.
3. Recall the CB pattern to the SRAM.
4. Read the CB pattern from the SRAM. (Steps 3 and 4 need to be done to ensure that the CB pattern has been stored correctly.)
5. Bake the device under test (DUT) for 96 hours at 70°C. (The device should be baked at the upper temperature limit of the device's specification. This is the worst case temperature for retention characteristics. For a commercial device 70°C is chosen.) The bake should be an unbiased bake with the device placed in antistatic foam or other conductive material.
6. Margin 1's. (The Memory Margining section outlines the technique employed to margin both 1's and 0's.) Record V_M, the voltage determined during margining, and the exact number of hours (to the nearest hour) since the pattern was stored in the EEPROM. The data collected at this point should be recorded as $V_{M1(one's)}$ and $T_{1(one's)}$.

7. Bake the device for an additional 408 hours at 70°C. (The total bake is 504 hours with data collection at 96 and at 504 hours.)
8. Margin 1's. Record $V_{M2(one's)}$ and $T_{2(one's)}$.
9. Plot $T_{1(one's)}$, $T_{2(one's)}$, $V_{M1(one's)}$, $V_{M2(one's)}$ to determine the 1's retention characteristics of the DUT. This is illustrated in the example retention plot.
10. Repeat steps 1 thru 5. (1's margining was completed in step 9. Steps 10 thru 14 address 0's margining.)
11. Margin 0's. Record $V_{M1(zero's)}$ and $T_{1(zero's)}$.
12. Bake the DUT for an additional 408 hours at 70°C. (Same as step 7).
13. Margin 0's. Record $V_{M2(zero's)}$ and $T_{2(zero's)}$.
14. Plot $T_{1(zero's)}$, $T_{2(zero's)}$, $V_{M1(zero's)}$, and $V_{M2(zero's)}$.

NOTE: The following conditions are recommended for writing, storing, reading, and recalling the DUT.

V_{CC} = 5.0V $V_{IL} \leq$ 0.8V
$V_{IH} \geq$ 2.0V T_A = Room Temperature

In addition to plotting the data to determine retention time, the following equation can be used to predict V_M at 1 year. That is, the equation will predict the remaining 1's or 0's margin after one year of storage.

$$V_{M(1\ yr)} = \left[\left(\frac{V_{M2}-V_{M1}}{\log_{10} T_2 - \log_{10} T_1}\right)(3.94 - \log_{10} T_1)\right] + V_{M1}$$

NOTE: The times (T) must be in hours.

The device will recall correctly at one year if the following inequalities are met.

$$V_{M\ (one's)} @ 1\ yr. > OV$$

$$V_{M\ (zero's)} @ 1\ yr < OV$$

$\overline{NV}$ and $\overline{WE}$

During memory margining a voltage must be applied to each of the memory capacitors in the DUT. To achieve this, $\overline{NV}$ (pin 19) and $\overline{WE}$ (pin 21) are utilized. $\overline{NV}$ takes on the additional function of Margin Enable (ME) and $\overline{WE}$ takes on the additional function of Margining Voltage (MV). Timings and voltage limits for these pins may be found in the AC Characteristics section. In the interest of clarity, these pins will be denoted as $\overline{NV}$(ME) and $\overline{WE}$(MV) in this application note.

NOTE: For the 52004-28, $\overline{NV}$ is pin 1 and $\overline{WE}$ is pin 27.

Memory Margining

Information is retained in the EEPROM section of the NVRAM by storing a charge in each of the memory capacitors. This storage of charge is reflected in a change of the threshold voltage (V_{TH}) of the memory capacitor. The rate at which V_{TH} decays is directly related to the retention time of an NVRAM. Unfortunately, V_{TH} cannot be measured directly. However, the voltage V_M, that is applied to the $\overline{WE}$ (MV) pin is used to determine the magnitude of V_{TH}. It is in this manner that V_{TH} is evaluated. The following steps outline the technique that is used to evaluate V_{TH} (using V_M) correctly.

NOTE: The following is the margining technique that is referred to in steps 6, 8, 11, and 13 in the Predicting Retention Time section. (This entire section must be performed in order to execute each of the steps listed above.)

1. Write an inverted checkerboard pattern (ICB) into the SRAM. (An ICB pattern is written into the SRAM at this point to ensure that each memory location will be forced to change state when the CB pattern is recalled from the EEPROM.)
2. Set up the $\overline{NV}$ (ME) and $\overline{WE}$ (MV) pins for margining. See AC Characteristics for correct timings.
3. Apply the correct V_M to the $\overline{WE}$ (MV) pin. The next section, Performing a Binary Search, explains the method that must be used to generate the correct V_M. (Once the initial limits have been chosen for V_M, this step may be directly replaced by the second step in the Performing a Binary Search section.)
4. Recall the CB pattern to the SRAM. (This is the CB pattern that was stored in the EEPROM in step one of the Predicting Retention Time section.)

5. Set up the $\overline{NV}$ (ME) and $\overline{WE}$ (MV) pins so the SRAM can be read.
6. Read the SRAM. If the SRAM verifies correctly, this iteration is considered a "pass"; if the SRAM does not verify correctly, this iteration is considered a "fail". A new V_M is generated based on whether the SRAM verified correctly or not, as shown in step 3 of the next section. (Once the binary search technique is understood this step may be replaced by the third step found in the Performing a Binary Search section.)

NOTE: A device whose pattern does not verify correctly ("fails") does not mean that the device is no longer functioning correctly. When a device recalls incorrectly it means that the value of V_M has exceeded the value of V_{TH}, which is part of the margining technique.

7. Repeat steps 1 thru 6 eight additional times. (A total of nine iterations are needed to ensure the resolution of V_M.)
8. After the ninth iteration is complete, add the last pass limit and fail limit (as determined in step 6) together and divide by two. This is the V_M that should be recorded for plotting.

Performing a Binary Search

The binary search method must be used during memory margining to generate the margining voltage (V_M) for both 1's and 0's. This method is used because it is the most efficient way to accurately generate the margining voltage with the fewest number of iterations. (Applying V_M to the memory degrades the margin slightly, therefore as few iterations as possible are desired.)

The 1's margin search window is 0 to 6 volts; the 0's margin search window is 0 to -6 volts. In each case, nine margining iterations are used to determine the correct V_M within the appropriate window. A description of the binary search technique for determining the 1's margin voltage $V_{M(one's)}$ follows. (Determining $V_{M(zero's)}$ is the same except that the initial window is 0 to –6 volts.)

1. Begin with a "fail limit" of 6 volts and a "pass limit" of 0 volts. (The window between the pass and fail limits is the search window.)
2. Add the pass and fail limits together and divide by two. (The first V_M will be 3 volts). This is the manner in which the margin voltage is determined for each iteration.
3. If the device passes (that is, if the pattern recalls correctly as determined by steps 4, 5, and 6 of the preceding section) at the V_M determined in step 2 (of this section), set the new pass limit equal to that VM and keep the previous fail limit. If the device fails (does not recall correctly) at the V_M determined in step 2, set the new fail limit equal to that V_M and keep the previous pass limit.
4. Repeat step 2 to determine the new V_M.

To determine the 0's margin voltage, repeat the above procedure except begin with a fail limit of -6 volts and a pass limit of 0 volts.

The resolution of the margin voltage determined by the binary search method can be determined by the following equation.

$$\frac{L_F - L_P}{2^{i+1}}$$

where
L_F = fail limit
L_P = pass limit
i = number of iterations

For a 6 volt window and a total of 9 iterations, the resolution of the resultant V_M will be approximately ±6 mV.

Pitfalls

— The resolution of V_M, the voltage that is applied to the $\overline{WE}$(MV) pin, is very important. To ensure accurate results the resolution of the V_M power supply should be no worse than ±0.010mV.

— Nine binary search iterations must be performed to ensure the resolution of the V_M that is plotted. With nine iterations and a V_M power supply resolution of ±0.010mV the overall resolution of V_M will be within ±0.016mV.

— V_{ME}, the voltage applied to the $\overline{NV}$ (ME) pin during margining should be 24 ±0.5V.

— 1's and 0's must be margined separately. That is, all steps required to generate both 1's margin data points must be completed and the CB pattern must be stored again in the EEPROM before margining of the 0's can begin.

— Write, store, read, and recall operations must meet the specification for the particular device being margined.

— Margining must be performed in accordance with the timings and voltages presented in the AC Characteristics section of this application note.

— The retention bake temperature should be chosen to match the upper temperature limit of the specification of the device being evaluated.

— The DUT should be margined within several (up to 4) hours after being removed from the retention bake.

— For the purpose of predicting retention times, the DUT should not be margined prior to 24 hours after a pattern has been stored in the EEPROM. The relationship between V_{TH} and T during the first 24 hours is generally log-log. Retention time predictions with one of the data points collected prior to 24 hours will be incorrect.

— For the purpose of this application note, a "1" may be considered to be a "written" state and a "0" to be an "erased" state. A discussion of the relationship between written and erased states and logical 1's and 0's may be found in the SNOS NONVOLATILE MEMORY RELIABILITY REPORT.

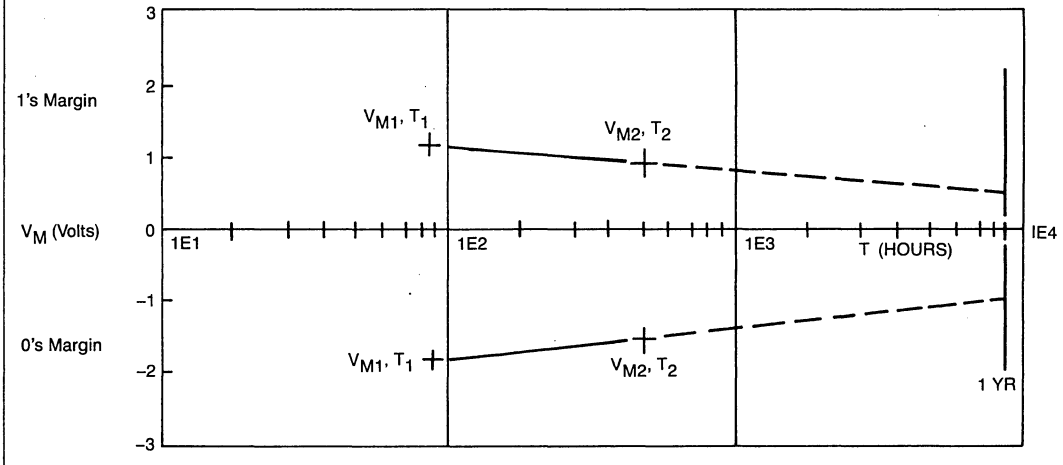
Predicting Retention - An Example

The following example is based on data collected from a sample of NCR 52001's. It is representative of the retention characteristics generated by any one of the products in NCR's family of byte wide NVRAM's.

The 1's were margined at 97 and 498 hours, and the 0's were margined at 102 and 510 hours with the following results.

	T_1	T_2
1's Margin	1.125 V	0.960 V
0's Margin	−1.805 V	−1.560 V

The following plot was generated from the data. It shows approximately 0.7V of 1's margin and -1V of 0's margin at one year.



EXAMPLE RETENTION PLOT

In addition to plotting the data, the 1's and 0's margin (at 1 year) have been calculated below.

$$V_{M\ (one's)\ @\ 1\ yr.} = \left[\left(\frac{0.960 - 1.125}{\log_{10} 498 - \log_{10} 97}\right)(3.94 - \log_{10} 97)\right] + 1.125$$

$$= \left(\frac{-0.165}{0.710}\right)(1.953) + 1.125$$

$$= -0.454 + 1.125$$

$$= 0.671 \text{ Volts (1's margin)}$$

$$V_{M\ (zero's)\ @\ 1\ yr.} = \left[\left(\frac{-1.560 - (-1.805)}{\log_{10} 510 - \log_{10} 102}\right)(3.94 - \log_{10} 102)\right] + (-1.805)$$

$$= \left(\frac{0.245}{0.699}\right)(1.931) + (-1.805)$$

$$= 0.677 + (-1.805)$$

$$= -1.128 \text{ Volts (0's margin)}$$

In both of the above examples, the inequalities $V_{M(one's)}$ @1 yr > 0V and $V_{M(zero's)}$ @ 1yr < 0V were met. This predicts that the DUT will recall both 1's and 0's correctly after one year of storage.

Writing a Checkerboard Pattern

NCR 52001

The memory array of NCR's 52001 128 x 8 bit byte wide NVRAM consists of eight data banks (one each for D0 thru D7). Each bank contains an 8 column by 16 row matrix (see memory map). Inputs A0-A2 are the column addresses and A3-A6 are the row addresses. Address 0 references the bit position in the upper lefthand corner of each data bank. Since the column addresses are less significant than the row addresses, address 1 is the bit position in row 0, column 1 (to the right of address 0).

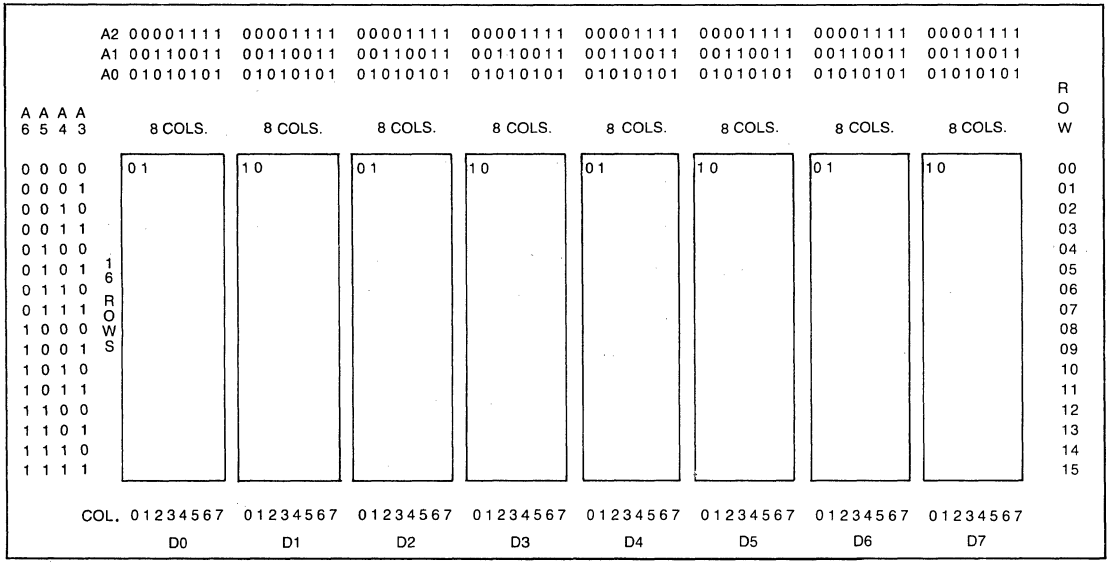
A checkerboard pattern resides in the SRAM array when adjacent memory cells contain complementary data. The procedure used to generate such a pattern is described below:

1. Begin at address 0 by writing the data 10101010 (D0 is the least significant bit).
2. Increment the address and complement the data. (Address 1 would be 01010101.)

NOTE: Address 0 (data 10101010) is shown in the upper left-hand corner of each data bank. Address 1 (data 01010101) is shown just to the right of address 0.

3. Write the complemented data.
4. Repeat steps 2 and 3 six additional times (until the last column is written).
5. Begin the next row by incrementing the address without complementing the data. Write the uncomplemented data.
6. Repeat steps 2, 3, and 4 until the row is completed.
7. Repeat steps 5 and 6 fourteen additional times to complete the array.

An inverted checkerboard pattern may be generated by following the above procedure except that all the data must be complemented. (Address 0 for an inverted checkerboard would be 01010101.)



NCR 52002

The memory array of NCR's 52002 256 x 8 bit byte wide NVRAM consists of eight data banks (one each for D0 - D7). Each bank contains an 8 column by 32 row matrix (see memory map). Inputs A0-A2 are the column addresses and A3-A7 are the row addresses. Address 0 references the bit position in the upper left-hand corner of each data bank. Since the column addresses are less significant than the row addresses, address 1 is the bit position in row 0, column 1 (to the right of address 0).

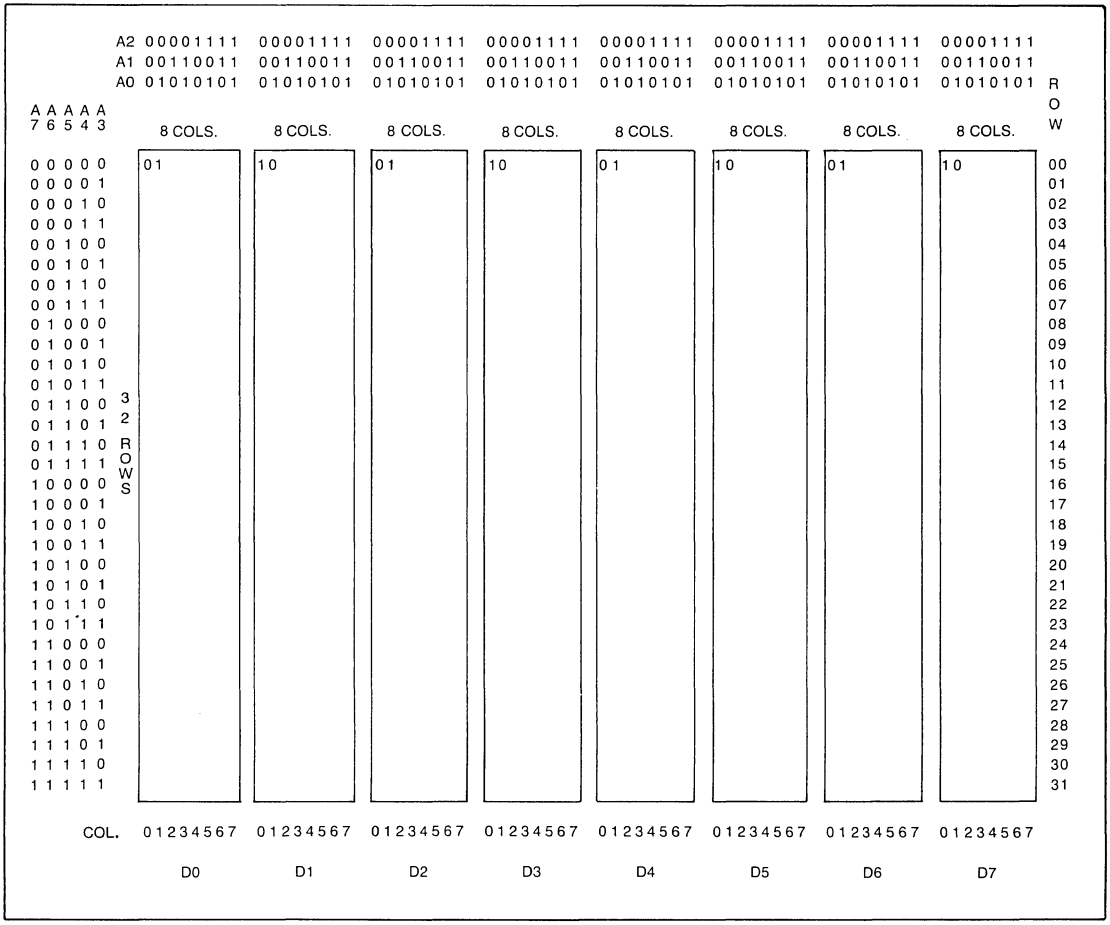
A checkerboard pattern resides in the SRAM array when adjacent memory cells contain complementary data. The procedure used to generate such a pattern is described below:

1. Begin at address 0 by writing the data 10101010 (D0 is the least significant bit).
2. Increment the address and complement the data. (Address 1 would be 01010101.)

NOTE: Address 0 (data 10101010) is shown in the upper left-hand corner of each data bank. Address 1 (data 01010101) is shown just to the right of address 0.

3. Write the complemented data.
4. Repeat steps 2 and 3 six additional times (until the last column is written).
5. Begin the next row by incrementing the address without complementing the data. Write the uncomplemented data.
6. Repeat steps 2, 3, and 4 until the row is completed.
7. Repeat steps 5 and 6 thirty additional times to complete the array.

An inverted checkerboard pattern may be generated by following the above procedure except that all the data must be complemented. (Address 0 for an inverted checkerboard would be 01010101.)



NCR 52004

The memory array of NCR's 52004 512 x 8 bit byte wide NVRAM consists of eight data banks (one each for D0 - D7). Each bank contains a 16 column by 32 row matrix (see memory map). Inputs A0-A3 are the column addresses and A4-A8 are the row addresses. Address 0 references the bit position in the upper left-hand corner of each data bank. Since the column addresses are less significant that the row addresses, address 1 is the bit position in row 0, column 1 (to the right of address 0).

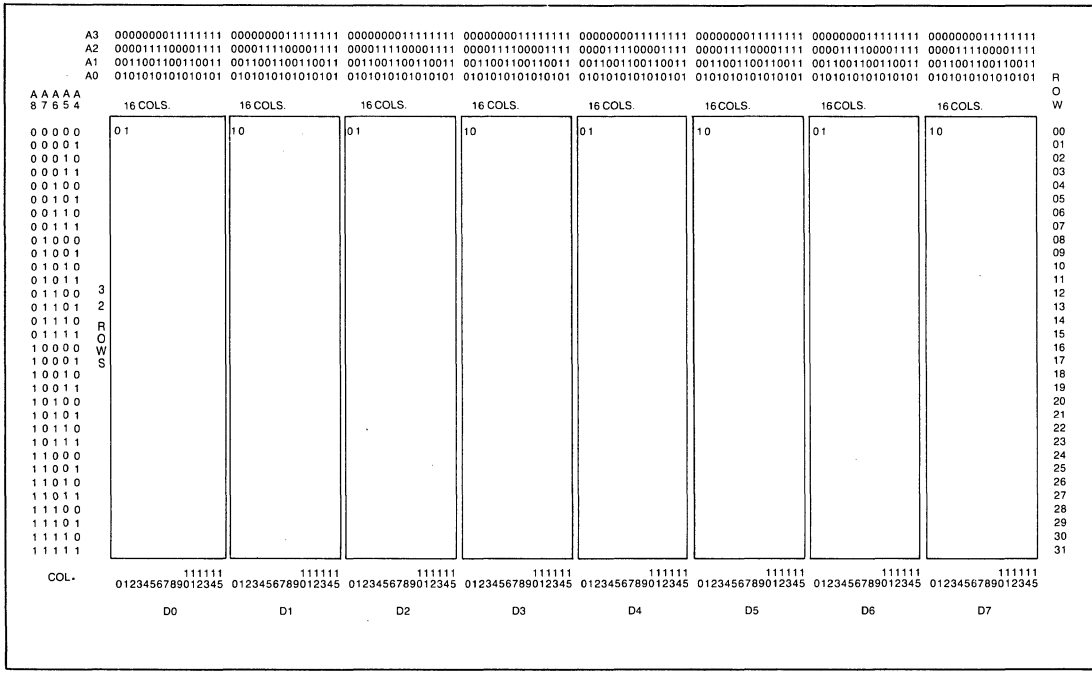
A checkerboard pattern resides in the SRAM array when adjacent memory cells contain complementary data. The procedure used to generate such a pattern is described below:

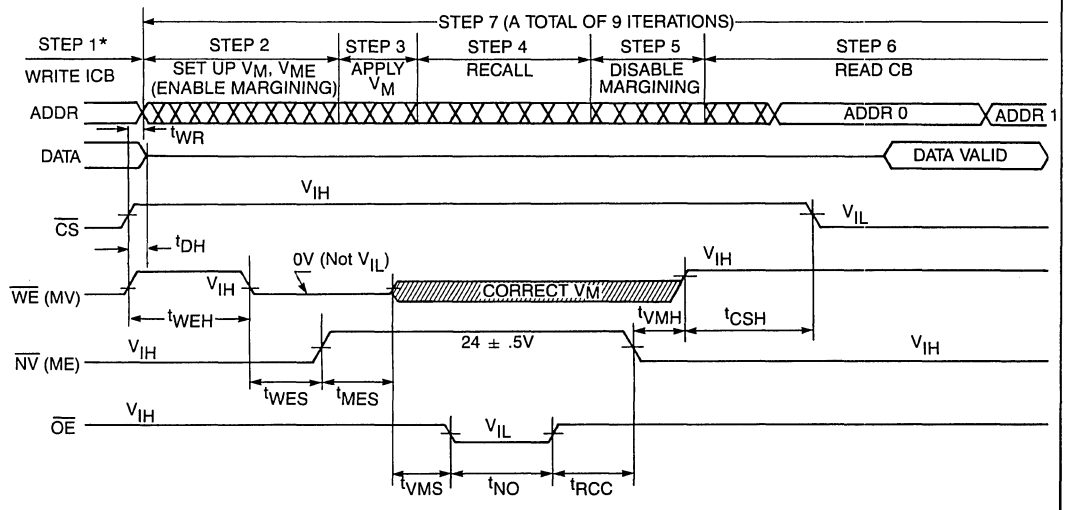
1. Begin at address 0 by writing the data 10101010 (D0 is the least significant bit).
2. Increment the address and complement the data. (Address 1 would be 01010101).

NOTE: Address 0 (data 10101010) is shown in the upper left-hand corner of each data bank. Address 1 (data 01010101) is shown just to the right of address 0.

3. Write the complemented data.
4. Repeat steps 2 and 3 fourteen additional times (until the last column is written).
5. Begin the next row by incrementing the address without complementing the data. Write the uncomplemented data.
6. Repeat steps 2, 3, and 4 until the column is completed.
7. Repeat steps 5 and 6 thirty additional times to complete the array.

An inverted checkerboard pattern may be generated by following the above procedure except that all the data must be complemented. (Address 0 for an inverted checkerboard would be 01010101.)





NOTE: $t_{VMS} + t_{NO} + t_{RCC}$ SHOULD BE AS SHORT AS POSSIBLE

* THESE ARE THE STEPS DESCRIBED IN THE MEMORY MARGINING SECTION

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_M	MARGIN VOLTAGE	V_{CC} = +5.0V	–6.0	*	6.0	V
V_{ME}	MARGIN ENABLE	V_{CC} = +5.0V	23.5	24.0	24.5	V
t_{DH}	DATA HOLD FROM WRITE TIME		SEE APPROPRIATE SPECIFICATION			
t_{WEH}	WRITE ENABLE HOLD FROM CHIP SELECT		100			ns
t_{WES}	WRITE ENABLE SET-UP TO MARGIN ENABLE		0			ns
t_{MES}	MARGIN ENABLE SET-UP TO MARGIN VOLTAGE		50			µs
t_{VMS}	MARGIN VOLTAGE SET-UP TO ARRAY RECALL		250			µs
t_{NO}	NV TO OUTPUT OVERLAP		SEE APPROPRIATE SPECIFICATION			
t_{RCC}	ARRAY RECALL CYCLE TIME		SEE APPROPRIATE SPECIFICATION			
t_{VMH}	MARGIN VOLTAGE HOLD FROM RECALL CYCLE		0			ns
t_{CSH}	CHIP SELECT HOLD FROM END OF MARGIN VOLTAGE		100			ns
t_{WR}	WRITE RELEASE TIME		SEE APPROPRIATE SPECIFICATION			

AC CHARACTERISTICS

*See Binary Search section for correct V_M.

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Non-Volatile Applications - Memory Margining Serial I/O EEPROMs 52801

APPLICATION NOTE

Introduction

Among the many features offered by NCR in their family of serial I/O Electrically Erasable PROM'S (EEPROM) is memory margining. Memory margining allows the user to determine the length of time that an EEPROM will retain the information written into it. The length of time that the EEPROM retains information (without being rewritten) is known as retention time.

This application note presents all the necessary information needed to margin and predict retention times for NCR'S family of serial I/O EEPROM's.

Predicting Retention Time

Retention time for an EEPROM is determined by plotting the voltage measured during memory margining (V_M) versus the time (T) when the device was margined. As shown in the example retention plot, at least two points (two each for both 1's and 0's margin) must be plotted to predict retention time. Since the relationship between V_M and T is generally logarithmic, the data should be plotted on semi-log paper. Plot V_M on the y-axis and T on the x-axis (this is the log axis). The following steps outline the procedure used to collect the data needed to predict both 1's and 0's retention times.

1. Block erase the EEPROM.
2. Write a known pattern into the EEPROM. A checkerboard (CB) pattern is generally preferred because it allows the user to margin both 1's and 0's with the same pattern. A description of how a checkerboard pattern is generated for the NCR 52801 has been included in this application note.

NOTE: Although the same pattern may be used, 1's and 0's must be margined separately. That is, all steps required to generate both data points for the 1's margin must be completed and the CB pattern must be rewritten to the EEPROM before margining of the 0's can begin. The reason for this is that the margining of one state disturbs the margin of the other state.

3. Read the CB pattern from the EEPROM. (This step needs to be done to ensure that the CB pattern has been written correctly.)
4. Bake the device under test (DUT) for 96 hours at 70°C. (The DUT should be baked at the upper temperature limit of the device's specification. This is the worst case temperature for margining. For a commercial device 70°C is chosen.) The bake should be an unbiased bake with the device placed in antistatic foam or other conductive material.
5. Margin 1's. (The Memory Margining section outlines the technique employed to margin both 1's and 0's.) Record V_M, the voltage determined during margining, and the exact number of hours (to the nearest hour) since the pattern was written to the EEPROM. The data collected at this point should be recorded as $V_{M1(one's)}$ and $T_{1(one's)}$.

6. Bake the DUT for an additional 408 hours at 70°C. (The total bake is 504 hours with data collection at 96 and at 504 hours.)
7. Margin 1's. Record $V_{M2(one's)}$ and $T_{2(one's)}$.
8. Plot $T_{1(one's)}$, $T_{2(one's)}$, $V_{M1(one's)}$, $V_{M2(one's)}$ to determine the 1's retention characteristics of the DUT. This is illustrated in the example retention plot.
9. Repeat steps 1 thru 4. (1's margining was completed in step 8. Steps 9 thru 13 address 0's margining.)
10. Margin 0's. Record $V_{M1(zero's)}$ and $T_{1(zero's)}$.
11. Bake the DUT for an additional 408 hours at 70°C. (Same as step 7).
12. Margin 0's. Record $V_{M2(zero's)}$ and $T_{2(zero's)}$.
13. Plot $T_{1(zero's)}$, $T_{2(zero's)}$, $V_{M1(zero's)}$, and $V_{M2(zero's)}$ to determine the 0's retention characteristics of the DUT.

NOTE:
The following conditions are recommended for reading, writing, and erasing the EEPROM.

V_{CC} = 5.0V $V_{IL} \leq$ 0.8V
$V_{IH} \geq$ 2.0V T_A = Room Temperature

In addition to plotting the data to determine retention time, the following equation can be used to predict V_M at 10 years. That is, the equation will predict the remaining 1's or 0's margin after ten years of storage.

$$V_{M\,(10\ yrs)} = \left[\left(\frac{V_{M2}-V_{M1}}{\log_{10} T_2 - \log_{10} T_1}\right)(4.94 - \log_{10} T_1)\right] + V_{M1}$$

NOTE: The times (T) must be in hours.

The device will read correctly at ten years if the following inequalities are met.

$$V_{M\,(one's)} @ 10\ yrs. > OV$$

$$V_{M\,(zero's)} @ 10\ yrs. < OV$$

WGND and VM

During memory margining a voltage must be applied to each of the memory transistors in the DUT. To achieve this, WGND (pin 5) and VM (pin 2) are utilized. When WGND is active, it allows the margin voltage (V_M) to be applied to the memory transistors. When margining 1's, the active state for WGND is a positive voltage and when margining 0's, the active state is a negative voltage. The margin voltage V_M is applied to the V_M pin. Timings and voltage limits for these pins may be found in the AC Characteristics section.

Memory Margining

Information is retained in the EEPROM by storing a charge in each of the memory transistors. This storage of charge is reflected as a change in the threshold voltage (V_{TH}) of the memory transistor. The rate at which V_{TH} decays is directly related to the retention time of an EEPROM. Unfortunately, V_{TH} cannot be measured directly. However, the voltage V_M, that is applied to the VM pin is used to determine the magnitude of V_{TH}. It is in this manner that V_{TH} is evaluated. The following steps outline the technique that is used to evaluate V_{TH} (using V_M) correctly.

NOTE: The following is the margining technique that is referred to in steps 5, 7, 10 and 12 in the Predicting Retention Time section. (This entire section must be performed in order to execute each of the steps listed above.)

1. Set up the WGND and VM pins for margining. See AC Characteristics for correct timings. (The WGND voltage is V_{ME}.)
2. Apply the correct V_M to the VM pin. The next section, Performing a Binary Search, explains the method that must be used to generate the correct V_M. (Once the initial limits have been chosen for V_M, this step may be directly replaced by the second step in the Performing a Binary Search section.)
3. Read the CB pattern from the EEPROM. (This is the pattern that was written into the EEPROM in step 2 of the Predicting Retention Time section.) If the pattern reads correctly, this iteration is considered a "pass"; if the pattern does not read correctly, this iteration is considered a "fail". A new V_M is generated based on whether the pattern read correctly or not, as shown in step 3 of the next section. (Once the binary search technique is understood, this step may be replaced by the third step in the Performing a Binary Search section.)

NOTE: A pattern that does not verify correctly ("fails") does not mean that the DUT is no longer functioning correctly. When a pattern reads incorrectly it means that the value of V_M has exceeded the value of V_{TH}, which is part of the margining technique.

4. Repeat steps 2 and 3 eight additional times. (A total of nine iterations are needed to ensure the resolution of V_M.)
5. After the ninth iteration is complete, add the last pass limit and fail limit (as determined in step 3) together and divide by two. This is the V_M that should be recorded for plotting.

Performing a Binary Search

The binary search method must be used during memory margining to generate the margining voltage (V_M) for both 1's and 0's. This method is used because it is the most efficient way to accurately generate the margining voltage with the fewest number of iterations. (Applying V_M to the memory degrades the margin slightly, therefore as few iterations as possible are desired.)

The 1's margin search window is 0 to +5 volts; the 0's margin search window is 0 to -5 volts. In each case, nine margining iterations are used to determine the correct V_M within the appropriate window. A description of the binary search technique for determining the 1's margin voltage follows. (The technique for 0's is the same except that the initial window is 0 to –5 volts.)

1. Begin with a "fail limit" of +5 volts and a "pass limit" of 0 volts. (The window between the pass and fail limits is the search window.)
2. Add the pass and fail limits together and divide by two. (The first V_M will be +2.5 volts). This is the manner in which the margining voltage is determined for each iteration.
3. If the device passes (that is, if the pattern reads correctly as determined in step 3 of the preceding section) at the V_M determined in step 2 of this section, set the new pass limit equal to that V_M and keep the previous fail limit. If the device fails (does not read correctly) at the V_M determined in step 2, set the new fail limit equal to that V_M and keep the previous pass limit.
4. Repeat step 2 to determine the new V_M.

To determine the 0's margin voltage, repeat the above procedure except begin with a fail limit of -5 volts and a pass limit of 0 volts.

The resolution of the margin voltage determined by the binary search method can be determined by the following equation.

$$\frac{L_F - L_P}{2^{i+1}}$$

where
L_F = fail limit
L_P = pass limit
i = number of iterations

For a 5 volt window and a total of 9 iterations, the resolution of the resultant V_M will be approximately ±5 mV.

Pitfalls

— The resolution of V_M, the voltage that is applied to the VM pin, is very important. To ensure accurate results the resolution of the V_M power supply should be no worse than ±0.010V.

— Nine binary search iterations must be performed to ensure the resolution of the V_M that is plotted. With nine iterations and a V_M power supply resolution of ±0.010V the overall resolution of V_M will be within ±0.015V.

— V_{ME}, the margin enable voltage applied to the WGND pin during margining, should be +9.0 ±0.5V for 1's margining and –7.0 ±0.5V for 0's margining.

— 1's and 0's must be margined separately. That is, all steps required to generate both 1's margin data points must be completed and the CB pattern must be rewritten into the EEPROM before margining of the 0's can begin.

— Write, read, and erase operations must meet the specification for the particular device being margined.

— Margining must be performed in accordance with the timings and voltages presented in the AC Characteristics section of this application note.

— The retention bake temperature should be chosen to match the upper temperature limit of the specification of the device being evaluated.

— The DUT should be margined within several (up to 4) hours after being removed from the retention bake.

— For the purpose of predicting retention times, an EEPROM should not be margined prior to 24 hours after a pattern has been written into it. The relationship between V_{TH} and T during the first 24 hours is generally log-log. Retention time predictions with one of the data points collected prior to 24 hours will be incorrect.

— For the purpose of this application note, a "1" may be considered to be a "written" state and a "0" to be an "erased" state. A discussion of the relationship between written and erased states and logical 1's and 0's may be found in the SNOS NON-VOLATILE MEMORY RELIABILITY REPORT.

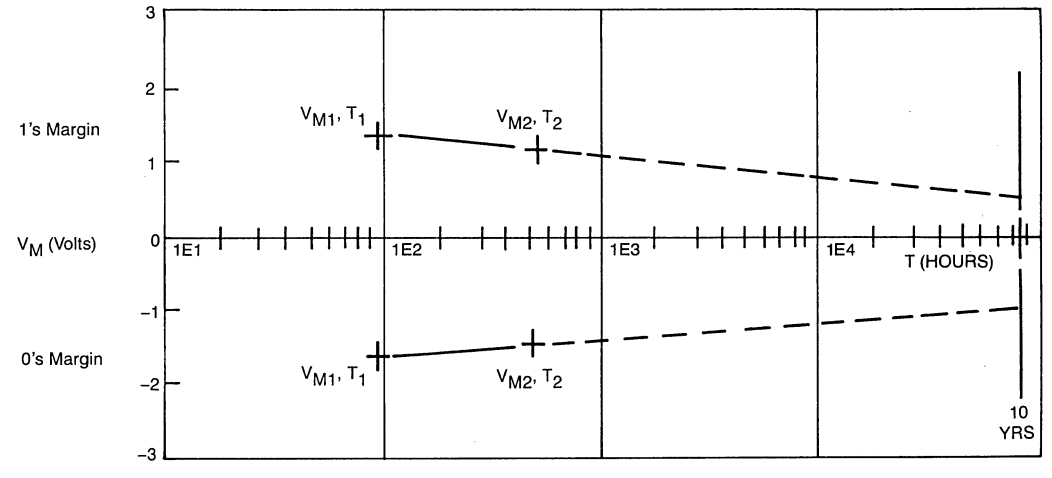
Predicting Retention - An Example

The following example is based on data collected from a sample of NCR 52801's. It is representative of the retention characteristics generated by any one of the products in NCR's family of serial I/O EEPROM's.

The 1's were margined at 94 and 503 hours, and the 0's were margined at 93 and 502 hours with the following results.

	T_1	T_2
1's Margin	1.320 V	1.120 V
0's Margin	−1.660 V	−1.510 V

The following plot was generated from the data. It shows approximately 0.5V of 1's margin and -1V of 0's margin at ten years.



EXAMPLE RETENTION PLOT

In addition to plotting the data, the 1's and 0's margin (at 10 years) have been calculated below.

$$V_{M\ (one's)\ @\ 10\ yrs.} = \left[\left(\frac{1.120 - 1.320}{\log_{10} 503 - \log_{10} 94}\right)(4.94 - \log_{10} 94)\right] + 1.320$$

$$= \left(\frac{-0.200}{0.728}\right)(2.967) + 1.320$$

$$= -0.815 + 1.320$$

$$= 0.505 \text{ Volts (1's margin)}$$

$$V_{M\ (zero's)\ @\ 10\ yrs.} = \left[\left(\frac{-1.510 - (-1.660)}{\log_{10} 502 - \log_{10} 93}\right)(4.94 - \log_{10} 93)\right] + (-1.660)$$

$$= \left(\frac{0.150}{0.732}\right)(2.971) + (-1.660)$$

$$= 0.609 + (-1.660)$$

$$= -1.051 \text{ Volts (0's margin)}$$

In both of the above examples, the inequalities $V_{M(one's)@10\ yrs} > 0V$ and $V_{M(zero's)@\ 10\ yrs} < 0V$ were met. This predicts that the DUT will recall both 1's and 0's correctly after ten years of storage.

Writing a Checkerboard Pattern

52801

The memory array of NCR's 52801 256-bit EEPROM is configured in 16 words, with each word containing 16 bits (D0 thru D15).

A checkerboard pattern exists in the EEPROM when adjacent memory cells contain complementary data. The procedure used to generate such a pattern is described below:

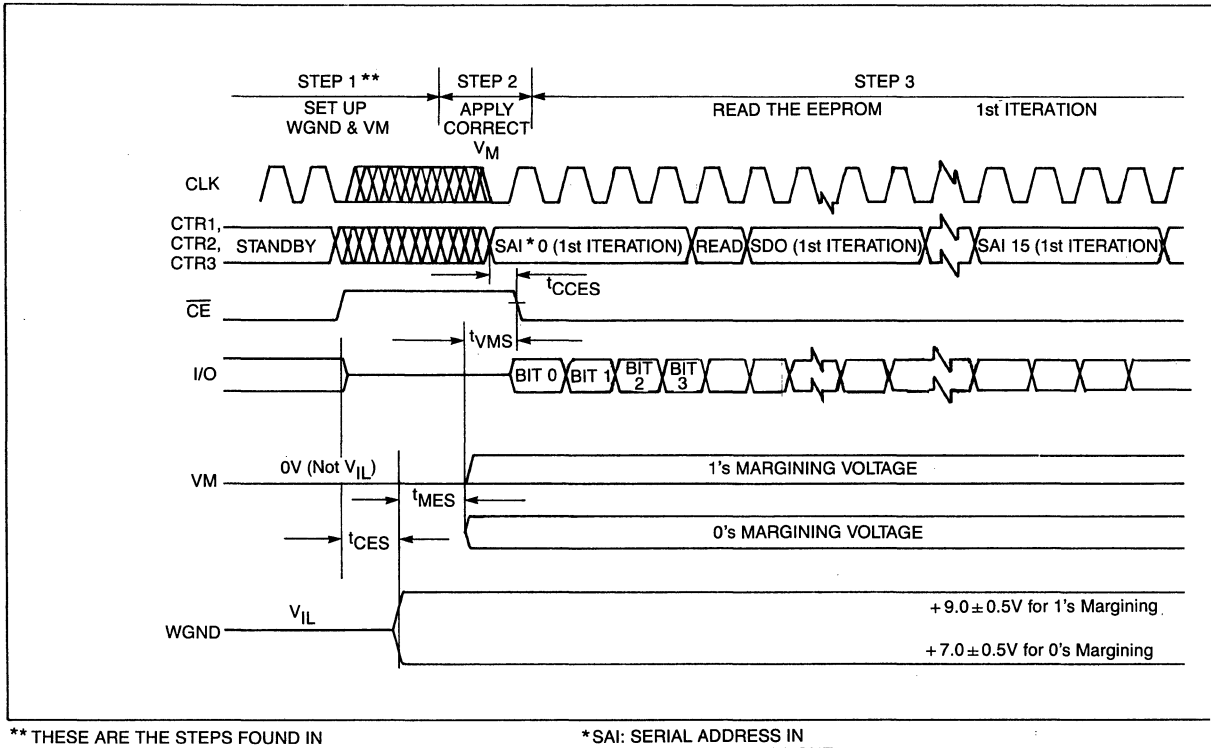
1. Begin at address 0 by writing the data 1111111100000000.
2. Increment the address and complement the data. (Address 1 would be 0000000011111111.)
3. Repeat step 2 fourteen additional times (a total of 16 addresses should be written).

An inverted checkerboard pattern may be generated by following the same procedure except that all the data must be complemented. (The data for address 0 would be 0000000011111111.)

The bit map for a checkerboard pattern is illustrated below.

	BIT															
ADDRESS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
A1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
A2	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
A3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
A4	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
A5	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
A6	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
A7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
A8	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
A9	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
A10	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
A11	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
A12	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
A13	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
A14	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
A15	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Although the above pattern is not a checkerboard when it is external to the 52801, the internal pattern, due to the decoding circuitry, will be a checkerboard.

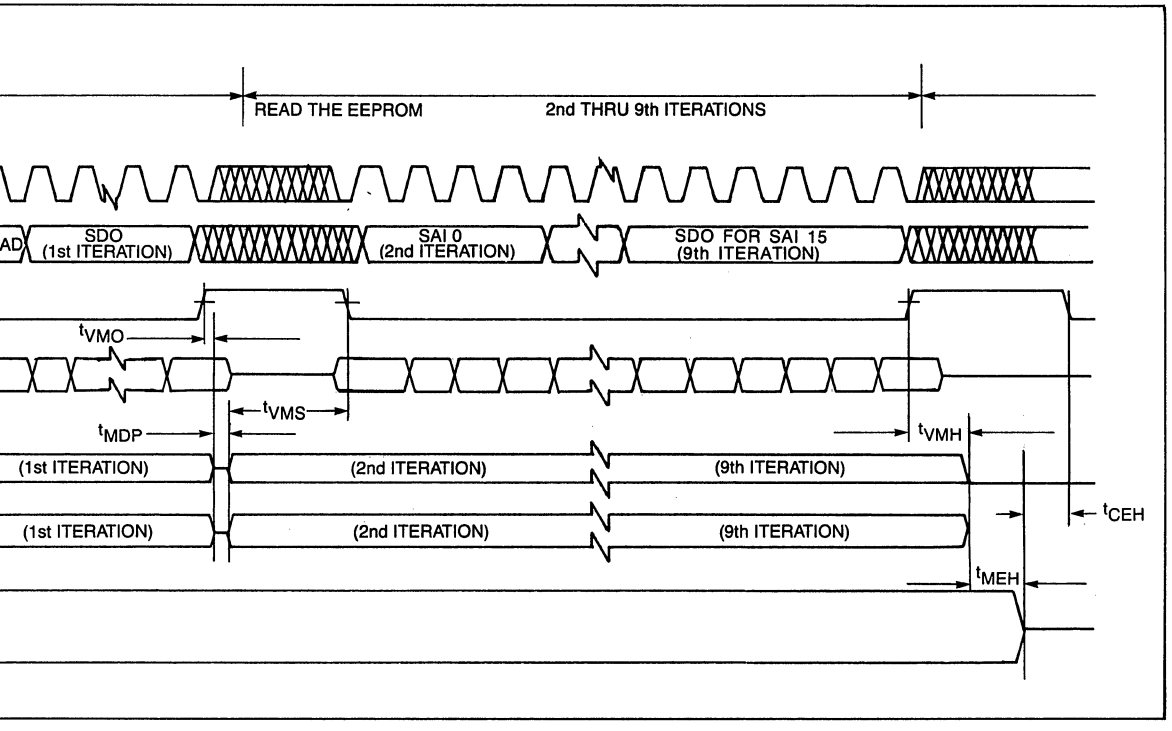


** THESE ARE THE STEPS FOUND IN THE MEMORY MARGINING SECTION

* SAI: SERIAL ADDRESS IN
SDO: SERIAL ADDRESS OUT

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VM	MARGINING VOLTAGE	VCC = 5.0V	−5.0	SEE BINARY SEARCH SECTION	+5.0	V
WGND (1's)	MARGINING ENABLE 1's	VCC = 5.0V	8.5	9.0	9.5	V
WGND (0's)	MARGINING ENABLE 0's	VCC = 5.0V	−7.5	−7.0	−6.5	V
t_{CES}	$\overline{CE}$ HIGH TO MARGINING ENABLE	—	0	—	—	nS
t_{MES}	MARGINING ENABLE SET UP TO MARGINING VOLTAGE	VCC = 5.0V	50	—	—	μS
t_{VMS}	MARGINING VOLTAGE SETUP TO $\overline{CE}$ LOW	—	100	—	—	μS
t_{CCES}	CTR 1, 2, 3 TO $\overline{CE}$ LOW	—	1	—	—	μS
t_{VMO}	VM HOLD AFTER $\overline{CE}$ HIGH	—	0	—	—	nS
t_{MDP}	NEW VM AFTER OLD VM	—	0	—	—	nS
t_{VMH}	$\overline{CE}$ HIGH TO VM OFF	—	0	—	—	nS
t_{MEH}	VM OFF TO WGND OFF	—	0	—	—	nS
t_{CEH}	MARGINING ENABLE OFF TO $\overline{CE}$ LOW	—	100	—	—	μS

NCR 52801 AC CHARACTERISTICS



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Non-Volatile Applications - Memory Margining Serial I/O EEPROMs 59308

APPLICATION NOTE

Introduction

Among the many features offered by NCR in their family of serial I/O Electrically Erasable PROM'S (EEPROM) is memory margining. Memory margining allows the user to determine the length of time that an EEPROM will retain the information written into it. The length of time that the EEPROM retains information (without being rewritten) is known as retention time.

This application note presents all the necessary information needed to margin and predict retention times for NCR'S family of serial I/O EEPROM's.

Predicting Retention Time

Retention time for an EEPROM is determined by plotting the voltage measured during memory margining (V_M) versus the time (T) when the device was margined. As shown in the example retention plot, at least two points (two each for both 1's and 0's margin) must be plotted to predict retention time. Since the relationship between V_M and T is generally logarithmic, the data should be plotted on semi-log paper. Plot V_M on the y-axis and T on the x-axis (this is the log axis). The following steps outline the procedure used to collect the data needed to predict both 1's and 0's retention times.

1. Block erase the EEPROM.
2. Write a known pattern into the EEPROM. A checkerboard (CB) pattern is generally preferred because it allows the user to margin both 1's and 0's with the same pattern. A description of how a checkerboard pattern is generated for the NCR 59308 has been included as a reference.

NOTE: Although the same pattern may be used, 1's and 0's must be margined separately. That is, all steps required to generate both data points for the 1's margin must be completed and the CB pattern must be rewritten to the EEPROM before margining of the 0's can begin. The reason for this is that the margining of one state disturbs the margin of the other state.

3. Read the CB pattern from the EEPROM. (This step needs to be done to ensure that the CB pattern has been written correctly.)
4. Bake the device under test (DUT) for 96 hours at 70°C. (The DUT should be baked at the upper temperature limit of the device's specification. This is the worst case temperature for margining. For a commercial device 70°C is chosen.) The bake should be an unbiased bake with the device placed in antistatic foam or other conductive material.
5. Margin 1's. (The Memory Margining section outlines the technique employed to margin both 1's and 0's.) Record V_M, the voltage determined during margining, and the exact number of hours (to the nearest hour) since the pattern was written to the EEPROM. The data collected at this point should be recorded as $V_{M1(one's)}$ and $T_{1(one's)}$.
6. Bake the DUT for an additional 408 hours at 70°C. (The total bake is 504 hours with data collection at 96 and at 504 hours.)

7. Margin 1's. Record $V_{M2(one's)}$ and $T_{2(one's)}$.
8. Plot $T_{1(one's)}$, $T_{2(one's)}$, $V_{M1(one's)}$, $V_{M2(one's)}$ to determine the 1's retention characteristics of the DUT. This is illustrated in the example retention plot.
9. Repeat steps 1 thru 4. (1's margining was completed in step 8. Steps 9 thru 13 address 0's margining.)
10. Margin 0's. Record $V_{M1(zero's)}$ and $T_{1(zero's)}$.
11. Bake the DUT for an additional 408 hours at 70°C. (Same as step 7).
12. Margin 0's. Record $V_{M2(zero's)}$ and $T_{2(zero's)}$.
13. Plot $T_{1(zero's)}$, $T_{2(zero's)}$, $V_{M1(zero's)}$, and $V_{M2(zero's)}$ to determine the 0's retention characteristics of the DUT.

NOTE: The following conditions are recommended for reading, writing, and erasing the EEPROM.

V_{CC} = 5.0V $V_{IL} \leq 0.8V$
$V_{IH} \geq 2.0V$ T_A = Room Temperature

In addition to plotting the data to determine retention time, the following equation can be used to predict V_M at 10 years. That is, the equation will predict the remaining 1's or 0's margin after ten years of storage.

$$V_M\,(10\ yrs) = \left[\left(\frac{V_{M2}-V_{M1}}{\log_{10} T_2 - \log_{10} T_1}\right)(4.94 - \log_{10} T_1)\right] + V_{M1}$$

NOTE: The times (T) must be in hours.

The device will read correctly at ten years if the following inequalities are met.

$$V_{M\,(one's)} @ 10\ yrs. > OV$$
$$V_{M\,(zero's)} @ 10\ yrs. < OV$$

VM EN and VM

During memory margining a voltage must be applied to each of the memory transistors in the DUT. To achieve this, VM EN (pin 7) and VM (pin 6) are utilized. When VM EN is active, it allows the margining voltage (V_M) to be applied to the memory transistors. When margining 1's, the active state for VM EN is a positive voltage, and when margining 0's, the active state is a negative voltage. Timings and voltage limits for these pins may be found in the AC Characteristics section.

Memory Margining

Information is retained in the EEPROM by storing a charge in each of the memory transistors. This storage of charge is reflected as a change in the threshold voltage (V_{TH}) of the memory transistor. The rate at which V_{TH} decays is directly related to the retention time of an EEPROM. Unfortunately, V_{TH} cannot be measured directly. However, the voltage V_M, that is applied to the VM pin is used to determine the magnitude of V_{TH}. It is in this manner that V_{TH} is evaluated. The following steps outline the technique that is used to evaluate V_{TH} (using V_M) correctly.

NOTE: The following is the margining technique that is referred to in steps 5, 7, 10 and 12 in the Predicting Retention Time section. (This entire section must be performed in order to execute each of the steps listed above.)

1. Set up the VM EN and VM pins for margining. See AC Characteristics for correct timings. (The VM EN voltage is V_{ME}.)
2. Apply the correct V_M to the VM pin. The next section, Performing a Binary Search, explains the method that must be used to generate the correct V_M. (Once the initial limits have been chosen for V_M, this step may be directly replaced by the second step in the Performing a Binary Search section.)
3. Read the CB pattern from the EEPROM. (This is the pattern that was written into the EEPROM in step 2 of the Predicting Retention Time section.) If the pattern reads correctly, this iteration is considered a "pass"; if the pattern does not read correctly, this iteration is considered a "fail". A new V_M is generated based on whether the pattern read correctly or not, as shown in step 3 of the next section. (Once the binary search technique is understood, this step may be replaced by the third step in the Performing a Binary Search section.)

NOTE: A pattern that does not verify correctly ("fails") does not mean that the DUT is no longer functioning correctly. When a pattern reads incorrectly it means that the value of V_M has exceeded the value of V_{TH}, which is part of the margining technique.

4. Repeat steps 2 and 3 eight additional times. (A total of nine iterations are needed to ensure the resolution of V_M.)
5. After the ninth iteration is complete, add the last pass limit and fail limit (as determined in step 3) together and divide by two. This is the V_M that should be recorded for plotting.

Performing a Binary Search

The binary search method must be used during memory margining to generate the margining voltage (V_M) for both 1's and 0's. This method is used because it is the most efficient way to accurately generate the margining voltage with the fewest number of iterations. (Applying V_M to the memory degrades the margin slightly, therefore as few iterations as possible are desired.)

The 1's margin search window is 0 to +5 volts; the 0's margin search window is 0 to -5 volts. In each case, nine margining iterations are used to determine the correct V_M within the appropriate window. A description of the binary search technique for determining the 1's margin voltage follows. (The technique for 0's is the same except that the initial window is 0 to −5 volts.)

1. Begin with a "fail limit" of +5 volts and a "pass limit" of 0 volts. (The window between the pass and fail limits is the search window.)
2. Add the pass and fail limits together and divide by two. (The first V_M will be +2.5 volts). This is the manner in which the margining voltage is determined for each iteration.
3. If the device passes (that is, if the pattern reads correctly as determined in step 3 of the preceding section) at the V_M determined in step 2 of this section, set the new pass limit equal to that V_M and keep the previous fail limit. If the device fails (does not read correctly) at the V_M determined in step 2, set the new fail limit equal to that V_M and keep the previous pass limit.
4. Repeat step 2 to determine the new V_M.

To determine the 0's margin voltage, repeat the above procedure except begin with a fail limit of -5 volts and a pass limit of 0 volts.

The resolution of the margin voltage determined by the binary search method can be determined by the following equation.

$$\frac{L_F - L_P}{2^{i+1}}$$

where
L_F = fail limit
L_P = pass limit
i = number of iterations

For a 5 volt window and a total of 9 iterations, the resolution of the resultant V_M will be approximately ±5 mV.

Pitfalls

— The resolution of V_M, the voltage that is applied to the VM pin, is very important. To ensure accurate results the resolution of the V_M power supply should be no worse than ±0.010V.

— Nine binary search iterations must be performed to ensure the resolution of the V_M that is plotted. With nine iterations and a V_M power supply resolution of ±0.010V the overall resolution of V_M will be within ±0.015V.

— V_{ME}, the margin enable voltage applied to the VM EN pin during margining, should be +9.0 ±0.5V for 1's margining and −7.0 ±0.5V for 0's margining.

— 1's and 0's must be margined separately. That is, all steps required to generate both 1's margin data points must be completed and the CB pattern must be rewritten into the EEPROM before margining of the 0's can begin.

— Write, read, and erase operations must meet the specification for the particular device being margined.

— Margining must be performed in accordance with the timings and voltages presented in the AC Characteristics section of this application note.

— The retention bake temperature should be chosen to match the upper temperature limit of the specification of the device being evaluated.

— The DUT should be margined within several (up to 4) hours after being removed from the retention bake.

— For the purpose of predicting retention times, an EEPROM should not be margined prior to 24 hours after a pattern has been written into it. The relationship between V_{TH} and T during the first 24 hours is generally log-log. Retention time predictions with one of the data points collected prior to 24 hours will be incorrect.

— For the purpose of this application note, a "1" may be considered to be a "written" state and a "0" to be an "erased" state. A discussion of the relationship between written and erased states and logical 1's and 0's may be found in the SNOS NONVOLATILE MEMORY RELIABILITY REPORT.

Predicting Retention - An Example

The following example is based on data collected from a sample of NCR 59308's. It is representative of the retention characteristics generated by any one of the products in NCR's family of serial I/O EEPROM's.

The 1's were margined at 90 and 500 hours, and the 0's were margined at 98 and 499 hours with the following results.

	T_1	T_2
1's Margin	1.330 V	1.130 V
0's Margin	−1.670 V	−1.510 V

The following plot was generated from the data. It shows approximately 0.5V of 1's margin and -1V of 0's margin at ten years.

In addition to plotting the data, the 1's and 0's margin (at 10 years) have been calculated below.

$$V_{M\ (one's)\ @\ 10\ yrs.} = \left[\left(\frac{1.130 - 1.330}{\log_{10} 500 - \log_{10} 90}\right)(4.94 - \log_{10} 90)\right] + 1.330$$

$$= \left(\frac{-0.200}{0.745}\right)(2.986) + 1.330$$

$$= -0.802 + 1.330$$

$$= 0.528 \text{ Volts (1's margin)}$$

$$V_{M\ (zero's)\ @\ 10\ yrs.} = \left[\left(\frac{-1.510 - (-1.670)}{\log_{10} 499 - \log_{10} 98}\right)(4.94 - \log_{10} 98)\right] + (-1.670)$$

$$= \left(\frac{0.160}{0.707}\right)(2.949) + (-1.670)$$

$$= 0.667 + (-1.670)$$

$$= -1.003 \text{ Volts (0's margin)}$$

In both of the above examples, the inequalities $V_{M(one's)}$ @ 10 yrs > 0V and $V_{M(zero's)}$ @ 10 yrs < 0V were met. This predicts that the DUT will recall both 1's and 0's correctly after ten years of storage.

Writing a Checkerboard Pattern

59308

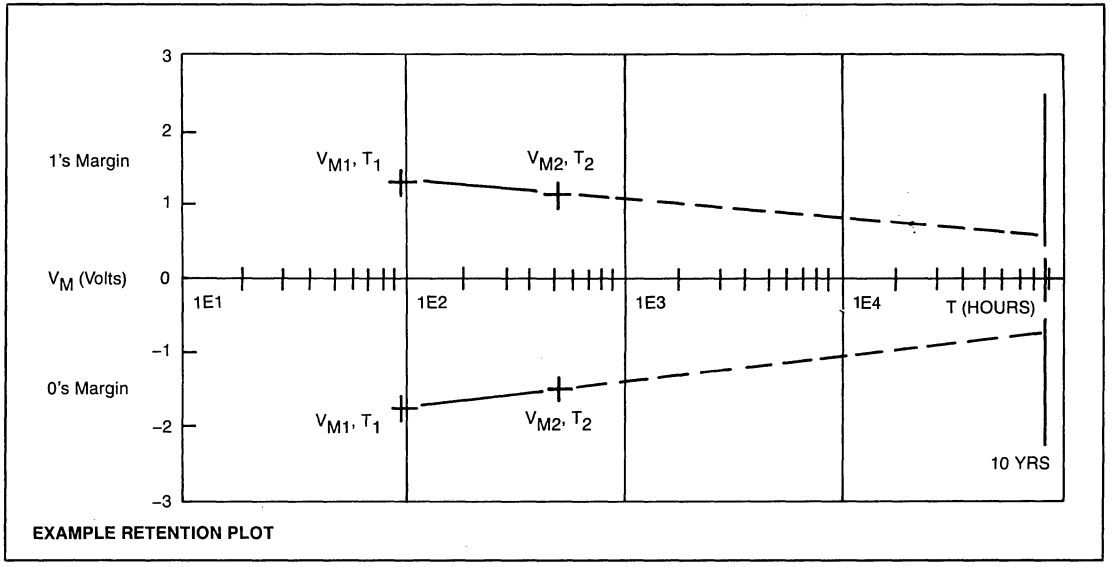
The memory array of NCR's 59308 1024-bit Serial I/O EEPROM is configured in 64 words, with each word containing 16 bits (D0 thru D15).

A checkerboard pattern exists in the EEPROM when adjacent memory cells contain complementary data. The procedure used to generate such a pattern is described below:

1. Begin at address 0 by writing the data 1010101010101010.
2. Increment the address and complement the data. (Address 1 would be 0101010101010101.)
3. Repeat step 2 sixty-two additional times (a total of 64 addresses should be written).

An inverted checkerboard pattern may be generated by following the same procedure except that all the data must be complemented. (The data for address 0 would be 0101010101010101.)

The bit map for a checkerboard pattern is illustrated on the following page.



EXAMPLE RETENTION PLOT

ADDRESSES					BIT (A5 = 0)														BIT (A5 = 1)													
A4	A3	A2	A1	A0	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
0	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	0	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
0	0	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	1	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
0	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
0	1	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	1	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
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1	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
1	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
1	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
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1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
1	0	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1	1	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
1	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
1	1	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
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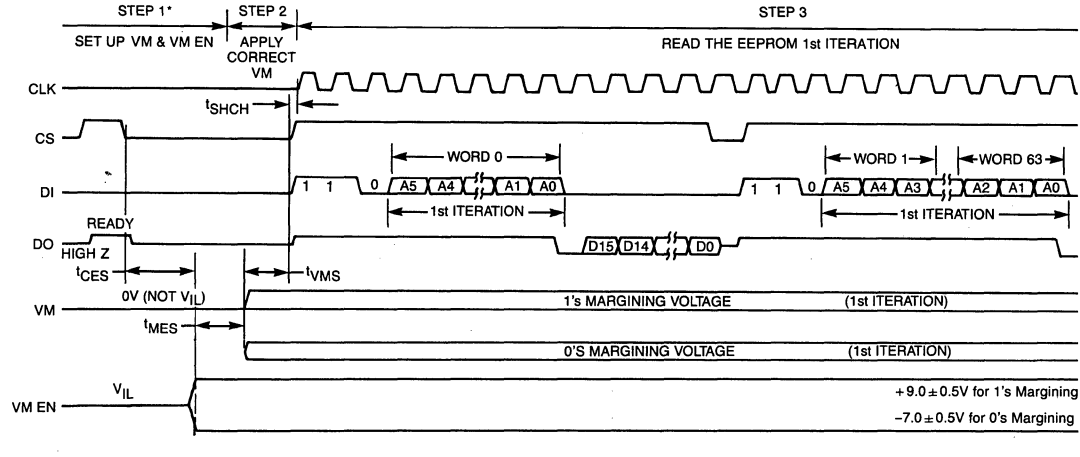
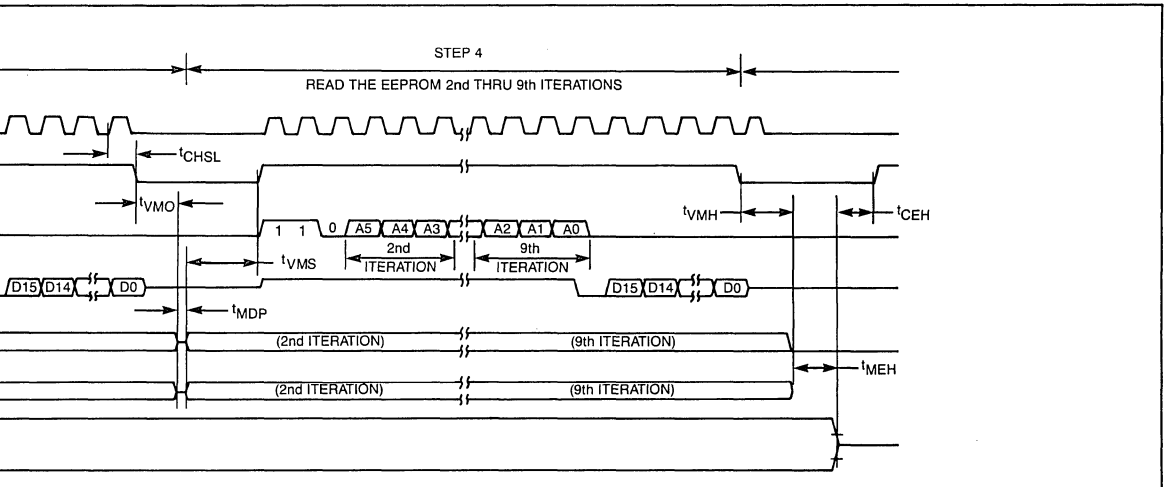
1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
1	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1



NCR 59308 AC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VM	MARGINING VOLTAGE	VCC = 5.0V	-5.0	SEE BINARY SEARCH SECTION	+5.0	V
VM EN (1's)	MARGINING ENABLE 1's	VCC = 5.0V	8.5	9.0	9.5	V
VM EN (0's)	MARGINING ENABLE 0's	VCC = 5.0V	-7.5	-7.0	-6.5	V
t_{CES}	CS LOW TO MARGINING ENABLE	—	0	—	—	nS
t_{MES}	MARGINING ENABLE SET UP TO MARGINING VOLTAGE	—	50	—	—	μS
t_{VMS}	MARGINING VOLTAGE SETUP TO CS HIGH	—	100	—	—	μS
t_{SHCH}	SELECT SET-UP TIME	—	200	—	—	ns
t_{CHSL}	SELECT HOLD TIME	—	1	—	—	μS
t_{VMO}	VM HOLD AFTER CS,OFF	—	0	—	—	nS
t_{MDP}	NEW VM AFTER OLD VM	—	0	—	—	nS
t_{VMH}	CS LOW TO VM OFF	—	0	—	—	nS
t_{MEH}	VM OFF TO VM EN OFF	—	0	—	—	nS
t_{CEH}	MARGINING ENABLE OFF TO CS HIGH	—	100	—	—	μS

*THESE ARE THE STEPS FOUND IN THE MEMORY MARGINING SECTION



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Non-Volatile Applications - Memory Margining Byte Wide EEPROMs 52832, 52864

APPLICATION NOTE

Introduction

Among the many features offered by NCR in their family of byte wide Electrically Erasable PROM'S (EEPROM) is memory margining. Memory margining allows the user to determine the length of time that an EEPROM will retain the information written into it. The length of time that the EEPROM retains information (without being rewritten) is known as retention time.

This application note presents all the necessary information needed to margin and predict retention times for NCR'S family of byte wide EEPROM's.

Predicting Retention Time

Retention time for an EEPROM is determined by plotting the voltage measured during memory margining (V_M) versus the time (T) when the device was margined. As shown in the example retention plot, at least two points (two each for both 1's and 0's margin) must be plotted to predict retention time. Since the relationship between V_M and T is generally logarithmic, the data should be plotted on semi-log paper. Plot V_M on the y-axis and T on the x-axis (this is the log axis). The following steps outline the procedure used to collect the data needed to predict both 1's and 0's retention times.

1. Block erase the EEPROM.
2. Write a known pattern into the EEPROM utilizing the Load and Write modes. A checkerboard (CB) pattern is generally preferred because it allows the user to margin both 1's and 0's with the same pattern. A description of how a checkerboard pattern is generated for the NCR 52832 and 52864 has been included in this application note.

NOTE: Although the same pattern may be used, 1's and 0's must be margined separately. That is, all steps required to generate both data points for the 1's margin must be completed and the CB pattern must be rewritten to the EEPROM before margining of the 0's can begin. The reason for this is that the margining of one state disturbs the margin of the other state.

3. Read the CB pattern from the EEPROM. (This step needs to be done to ensure that the CB pattern has been written correctly.)
4. Bake the device under test (DUT) for 96 hours at 70°C. (The DUT should be baked at the upper temperature limit of the device's specification. This is the worst case temperature for margining. For a commercial device 70°C is chosen.) The bake should be an unbiased bake with the device placed in antistatic foam or other conductive material.
5. Margin 1's. (The Memory Margining section outlines the technique employed to margin both 1's and 0's.) Record V_M, the voltage determined during margining, and the exact number of hours (to the nearest hour) since the pattern was written to the EEPROM. The data collected at this point should be recorded as $V_{M1(one's)}$ and $T_{1(one's)}$.

6. Bake the DUT for an additional 408 hours at 70°C. (The total bake is 504 hours with data collection at 96 and at 504 hours.)
7. Margin 1's. Record $V_{M2(one's)}$ and $T_{2(one's)}$.
8. Plot $T_{1(one's)}$, $T_{2(one's)}$, $V_{M1(one's)}$, $V_{M2(one's)}$ to determine the 1's retention characteristics of the DUT. This is illustrated in the example retention plot.
9. Repeat steps 1 thru 4. (1's margining was completed in step 8. Steps 9 thru 13 address 0's margining.)
10. Margin 0's. Record $V_{M1(zero's)}$ and $T_{1(zero's)}$.
11. Bake the DUT for an additional 408 hours at 70°C. (Same as step 7).
12. Margin 0's. Record $V_{M2(zero's)}$ and $T_{2(zero's)}$.
13. Plot $T_{1(zero's)}$, $T_{2(zero's)}$, $V_{M1(zero's)}$, and $V_{M2(zero's)}$ to determine the 0's retention characteristics of the DUT.

NOTE: The following conditions are recommended for reading, writing, loading and erasing the EEPROM.

V_{CC} = 5.0V $V_{IL} \leq$ 0.8V
$V_{IH} \geq$ 2.0V T_A = Room Temperature

In addition to plotting the data to determine retention time, the following equation can be used to predict V_M at 10 years. That is, the equation will predict the remaining 1's or 0's margin after ten years of storage.

$$V_M\,(10\ yrs) = \left[\left(\frac{V_{M2}-V_{M1}}{\log_{10} T_2 - \log_{10} T_1}\right)(4.94 - \log_{10} T_1)\right] + V_{M1}$$

NOTE: The times (T) must be in hours.

The device will read correctly at ten years if the following inequalities are met.

$$V_{M\,(one's)} @\ 10\ yrs. > OV$$
$$V_{M\,(zero's)} @\ 10\ yrs. < OV$$

CNTL1 and CNTL2

During memory margining a voltage must be applied to each of the memory transistors in the DUT. To achieve this, CNTL1 (pin 1) and CNTL2 (pin 26) are utilized. CNTL1 takes on the additional function of Margin Enable (ME) and CNTL2 takes on the additional function of Margin Voltage (MV). Timings and voltage limits for these pins may be found in the AC Characteristics section. In the interest of clarity, these pins will be denoted as CNTL1 (ME) and CNTL2 (MV) in this application note.

Memory Margining

Information is retained in the EEPROM by storing a charge in each of the memory transistors. This storage of charge is reflected as a change in the threshold voltage (V_{TH}) of the memory transistor. The rate at which V_{TH} decays is directly related to the retention time of an EEPROM. Unfortunately, V_{TH} cannot be measured directly. However, the voltage V_M, that is applied to the CNTL2 (MV) pin is used to determine the magnitude of V_{TH}. It is in this manner that V_{TH} is evaluated. The following steps outline the technique that is used to evaluate V_{TH} (using V_M) correctly.

NOTE: The following is the margining technique that is referred to in steps 5, 7, 10 and 12 in the Predicting Retention Time section. (This entire section must be performed in order to execute each of the steps listed above.)

1. Set up the CNTL1 (ME) & CNTL2 (MV) pins for margining. See AC Characteristics for correct timings. (The CNTL1 voltage is V_{ME}.)
2. Apply the correct V_M to the CNTL2 pin. The next section, Performing a Binary Search, explains the method that must be used to generate the correct V_M. (Once the initial limits have been chosen for V_M, this step may be directly replaced by the second step in the Performing a Binary Search section.)
3. Read the CB pattern from the EEPROM. (This is the pattern that was written into the EEPROM in step 2 of the Predicting Retention Time section.) If the pattern reads correctly, this iteration is considered a "pass"; if the pattern does not read correctly, this iteration is considered a "fail". A new V_M is generated based on whether the pattern read correctly or not, as shown in step 3 of the next section. (Once the binary search technique is understood, this step may be replaced by the third step in the Performing a Binary Search section.)

NOTE: A pattern that does not verify correctly ("fails") does not mean that the DUT is no longer functioning correctly. When a pattern reads incorrectly it means that the value of V_M has exceeded the value of V_{TH}, which is part of the margining technique.

4. Repeat steps 2 and 3 eight additional times. (A total of nine iterations are needed to ensure the resolution of V_M.)
5. After the ninth iteration is complete, add the last pass limit and last fail limit (as determined in step 3) together and divide by two. This is the V_M that should be recorded for plotting.

Performing a Binary Search

The binary search method must be used during memory margining to generate the margining voltage (V_M) for both 1's and 0's. This method is used because it is the most efficient way to accurately generate the margining voltage with the fewest number of iterations. (Applying V_M to the memory degrades the margin slightly, therefore as few iterations as possible are desired.)

The 1's margin search window is 0 to +5 volts; the 0's margin search window is 0 to -5 volts. In each case, nine margining iterations are used to determine the correct V_M within the appropriate window. A description of the binary search technique for determining the 1's margin voltage follows. (The technique for 0's is the same except that the initial window is 0 to –5 volts.)

1. Begin with a "fail limit" of +5 volts and a "pass limit" of 0 volts. (The window between the pass and fail limits is the search window.)
2. Add the pass and fail limits together and divide by two. (The first V_M will be +2.5 volts). This is the manner in which the margining voltage is determined for each iteration.
3. If the device passes (that is, if the pattern reads correctly as determined in step 3 of the preceding section) at the V_M determined in step 2 of this section, set the new pass limit equal to that V_M and keep the previous fail limit. If the device fails (does not read correctly) at the V_M determined in step 2, set the new fail limit equal to that V_M and keep the previous pass limit.
4. Repeat step 2 to determine the new V_M.

To determine the 0's margin voltage, repeat the above procedure except begin with a fail limit of -5 volts and a pass limit of 0 volts.

The resolution of the margin voltage determined by the binary search method can be determined by the following equation.

$$\frac{L_F - L_P}{2^{i+1}}$$

where
L_F = fail limit
L_P = pass limit
i = number of iterations

For a 5 volt window and a total of 9 iterations, the resolution of the resultant V_M will be approximately ±5 mV.

Pitfalls

— The resolution of V_M, the voltage that is applied to the CNTL2 pin, is very important. To ensure accurate results the resolution of the V_M power supply should be no worse than ±0.010V.

— Nine binary search iterations must be performed to ensure the resolution of the V_M that is plotted. With nine iterations and a V_M power supply resolution of ±0.010V the overall resolution of V_M will be within ±0.015V.

— V_{ME}, the margin enable voltage applied to the CNTL1 pin during margining, should be +22.0 ±0.5V for 1's margining and –6.0 ±0.5V for 0's margining.

— 1's and 0's must be margined separately. That is, all steps required to generate both 1's margin data points must be completed and the CB pattern must be rewritten into the EEPROM before margining of the 0's can begin.

— Write, read, load, and erase operations must meet the specification for the particular device being margined.

— Margining must be performed in accordance with the timings and voltages presented in the AC Characteristics section of this application note.

— The retention bake temperature should be chosen to match the upper temperature limit of the specific device being evaluated.

— The DUT should be margined within several (up to 4) hours after being removed from the retention bake.

— For the purpose of predicting retention times, an EEPROM should not be margined prior to 24 hours after a pattern has been written into it. The relationship between V_{TH} and T during the first 24 hours is generally log-log. Retention time predictions with one of the data points collected prior to 24 hours will be incorrect.

— For the purpose of this application note, a "1" may be considered to be a "written" state and a "0" to be an "erased" state. A discussion of the relationship between written and erased states and logical 1's and 0's may be found in the SNOS NONVOLATILE MEMORY RELIABILITY REPORT.

Predicting Retention - An Example

The following example is based on data collected from a sample of NCR 52832's. It is representative of the retention characteristics generated by any one of the products in NCR's family of byte wide EEPROM's.

The 1's were margined at 97 and 505 hours, and the 0's were margined at 93 and 501 hours with the following results.

	T_1	T_2
1's Margin	1.360 V	1.200 V
0's Margin	−1.250 V	−1.090 V

The following plot was generated from the data. It shows approximately 0.7V of 1's margin and -0.6V of 0's margin at ten years.

In addition to plotting the data, the 1's and 0's margin (at 10 years) have been calculated below.

$$V_{M\ (one's)\ @\ 10\ yrs.} = \left[\left(\frac{1.200 - 1.360}{\log_{10} 505 - \log_{10} 97}\right)(4.94 - \log_{10} 97)\right] + 1.360$$

$$= \left(\frac{-0.160}{0.716}\right)(2.953) + 1.360$$

$$= -0.660 + 1.360$$

$$= 0.700 \text{ Volts (1's margin)}$$

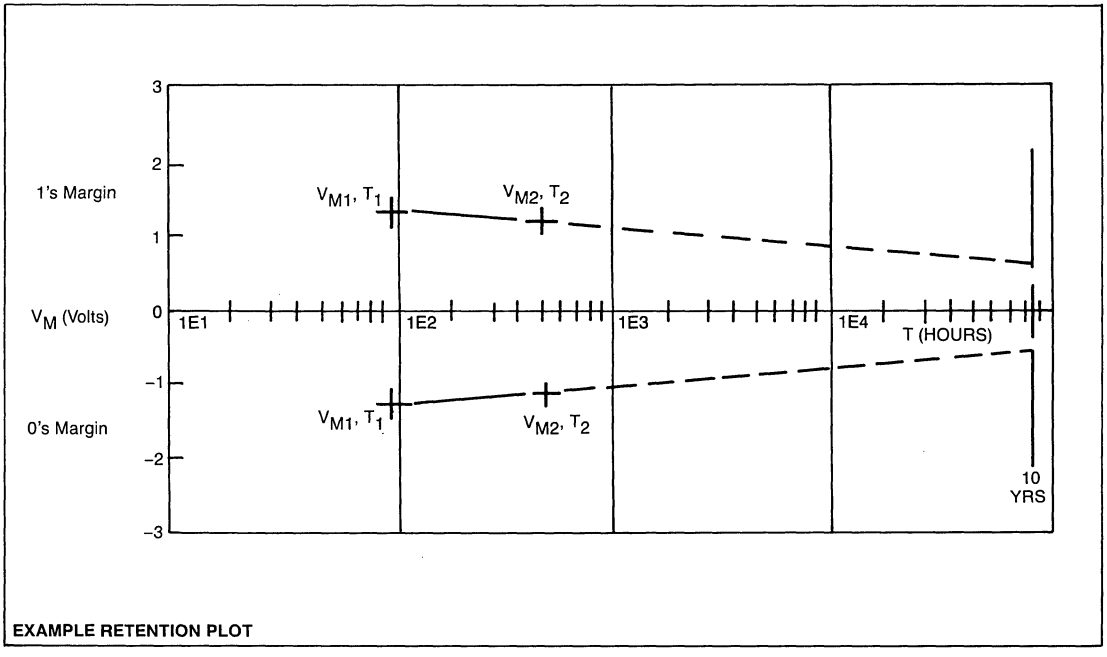
$$V_{M\ (zero's)\ @\ 10\ yrs.} = \left[\left(\frac{-1.090 - (-1.250)}{\log_{10} 501 - \log_{10} 93}\right)(4.94 - \log_{10} 93)\right] + (-1.250)$$

$$= \left(\frac{0.160}{0.731}\right)(2.971) + (-1.250)$$

$$= 0.650 + (-1.250)$$

$$= -0.600 \text{ Volts (0's margin)}$$

In both of the above examples, the inequalities $V_{M(one's)}$ @10 yrs > 0V and $V_{M(zero's)}$ @ 10 yrs < 0V were met. This predicts that the DUT will recall both 1's and 0's correctly after ten years of storage.



EXAMPLE RETENTION PLOT

Writing a Checkerboard Pattern

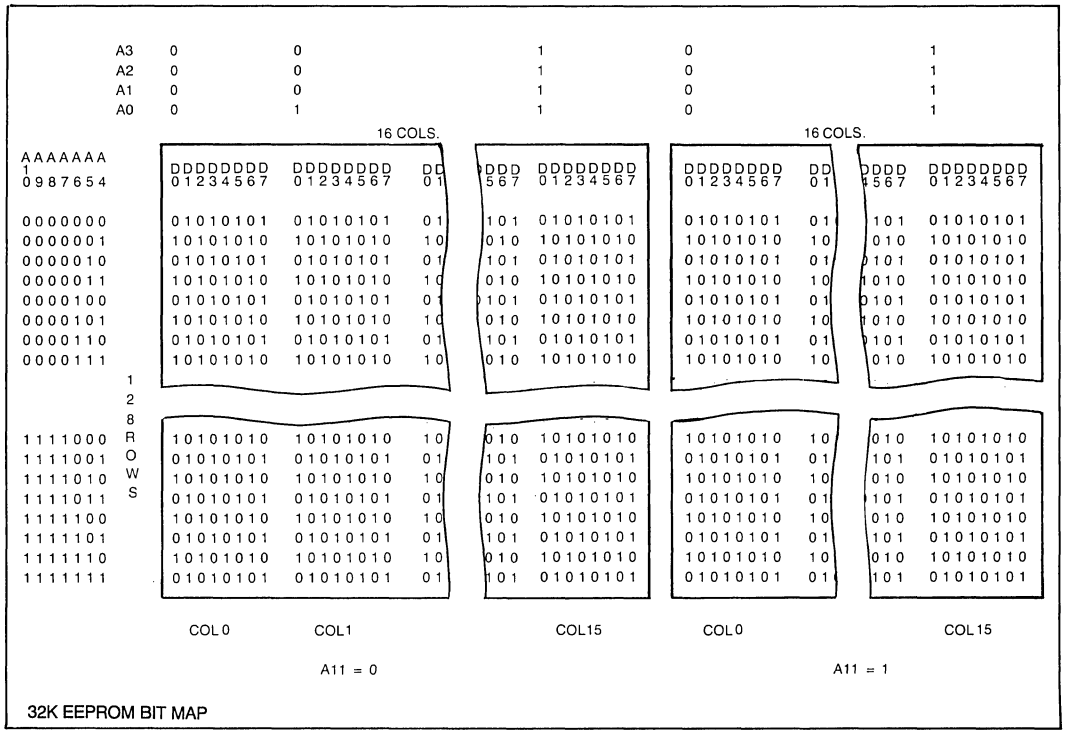
52832

The memory array of NCR's 52832 4K × 8 bit EEPROM consists of two data banks. Each bank contains a 16 column by 128 row matrix with each column consisting of 8 data bits (see memory map). Inputs A4-A 10 are the row addresses and A0-A3 are the column addresses. Address 0 references the bit position in the upper left-hand corner of each bank. The left bank is selected by A11 = 0, and the right bank by A11 = 1. Since the column addresses are less significant than the row addresses, address 1 is the bit position in row 0 column 1 (directly to the right of address 0).

A checkerboard pattern resides in the array when adjacent memory cells contain complementary data. The procedure used to generate such a pattern is described below:

1. Begin at address 0 by loading the data 01010101 (bit D0-D7 with A11 = 0).
2. Increment the address and load the same data. (In row 1 the data is 01010101).
3. Repeat step 2 fourteen additional times until all sixteen columns are loaded.
4. Write the data.
5. Begin the next row by complementing the data and incrementing the address (data for the second row is 10101010).
6. Repeat steps 2, 3, 4, and 5 to complete the left bank (a total of 128 times).
7. Set A11 = 1 and repeat steps 1, 2, 3, 4, 5 and 6 to complete the matrix.

An inverted checkerboard pattern may be generated by following the same procedure except that all the data must be complemented. (The data for address 0 would be 10101010.)



32K EEPROM BIT MAP

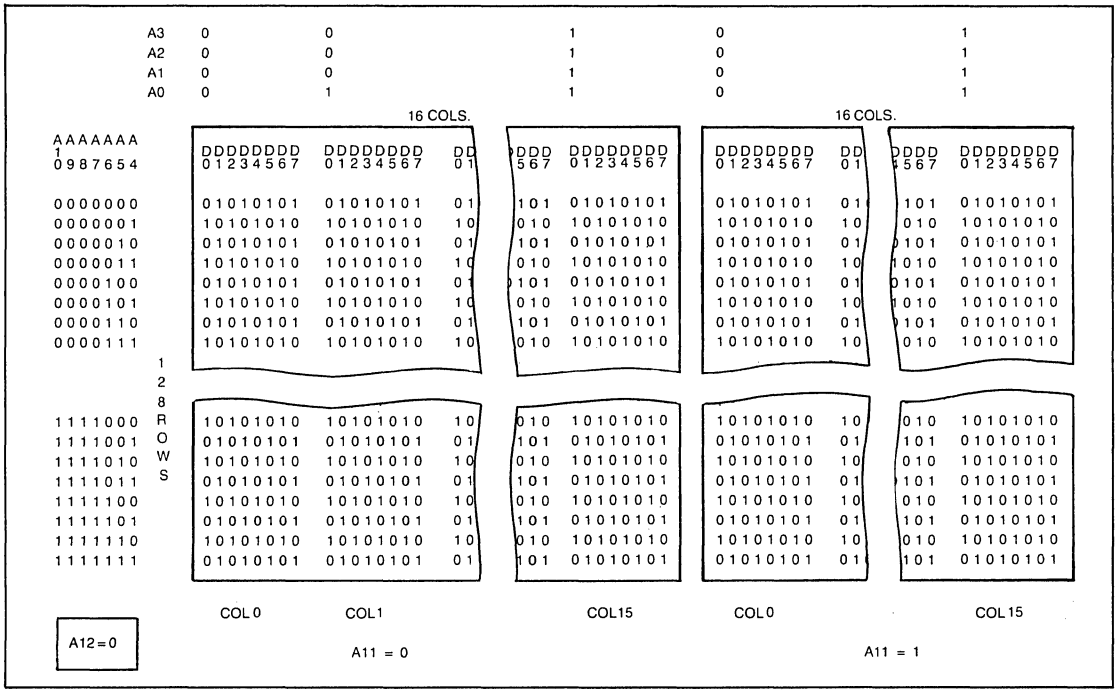
52864

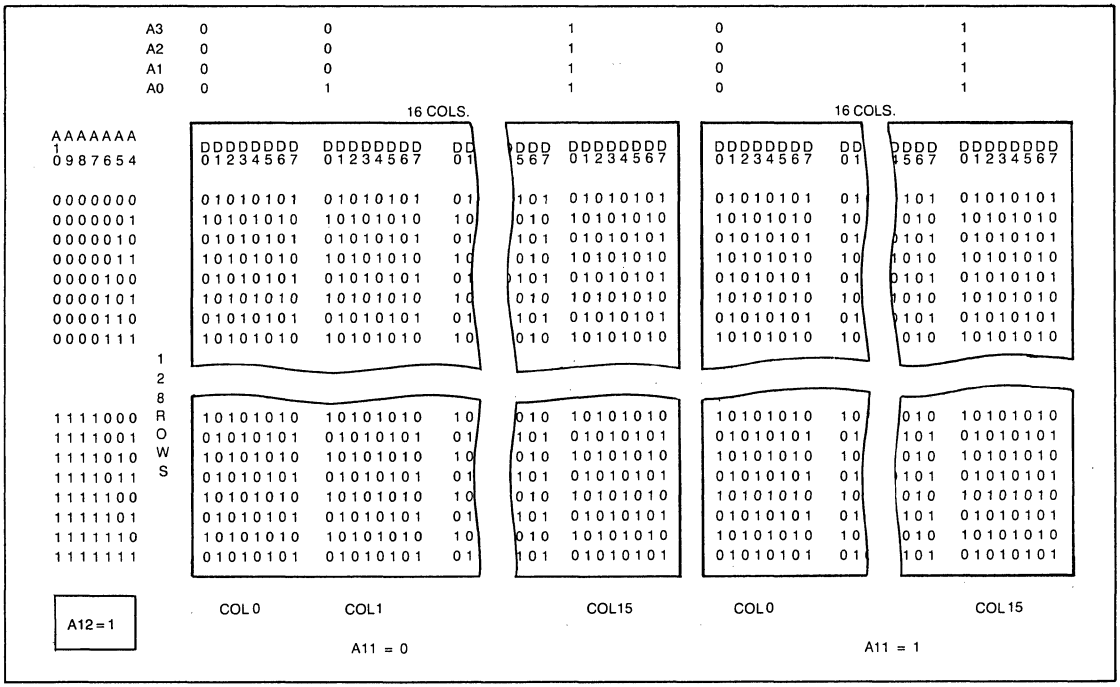
The memory array of NCR's 52864 8K x 8 bit EEPROM consists of four data banks. Each bank contains a 16 column by 128 row matrix with each column consisting of 8 data bits (see memory map). Inputs A4-A10 are the row addresses and A0-A3 are the column addresses. Address 0 references the bit position in the upper left-hand corner of each bank. The left bank is selected by A11 = 0, and the right bank by A11 = 1. The upper two banks are selected by A12 = 0, and the lower banks by A12 = 1. Since the column addresses are less significant than the row addresses, address 1 is the bit position in row 0 column 1 (directly to the right of address 0).

A checkerboard pattern resides in the array when adjacent memory cells contain complementary data. The procedure used to generate such a pattern is described below:

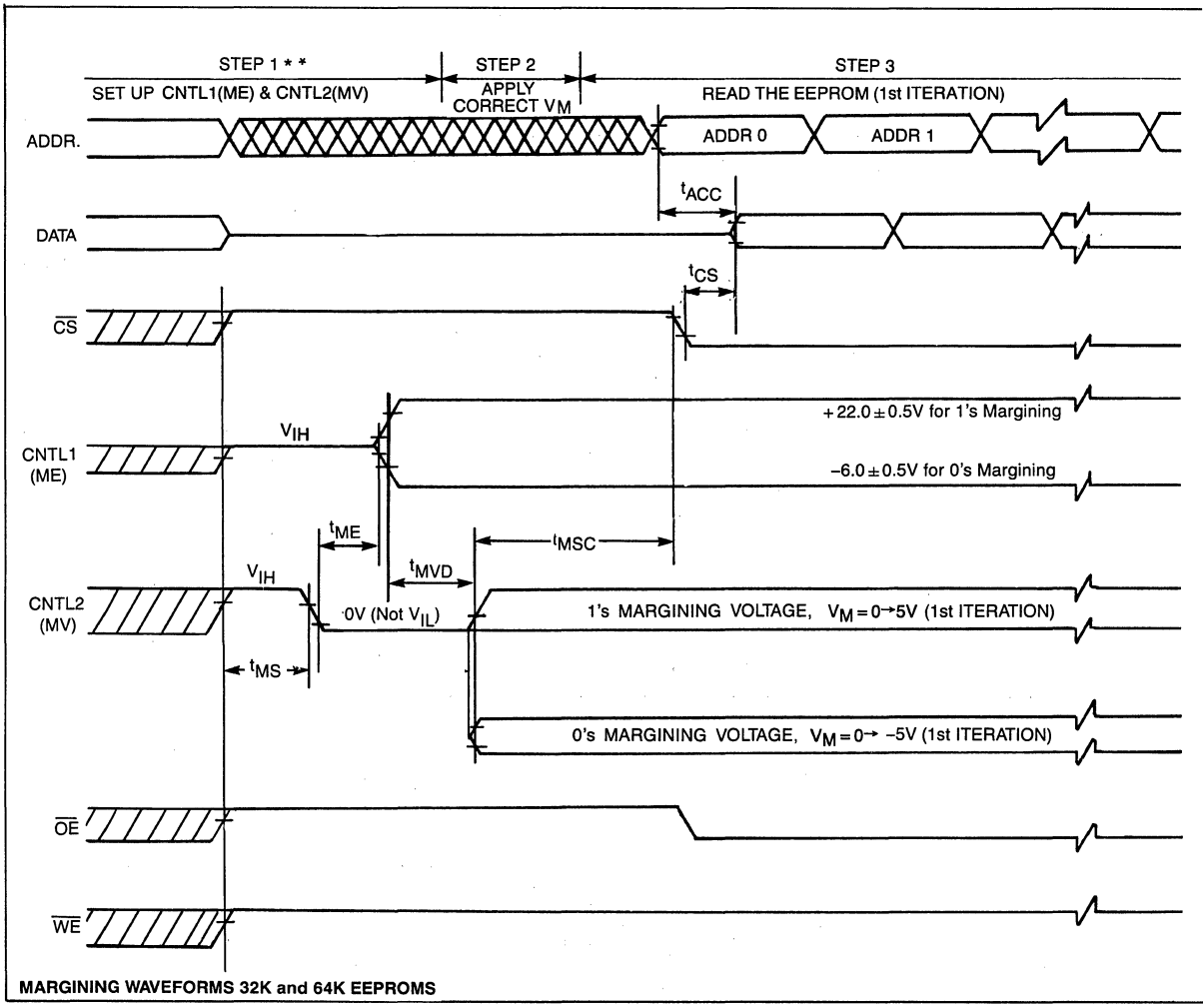
1. Begin at address 0 by loading the data 01010101 (bit D0-D7 with A11 = 0 and A12 = 0).
2. Increment the address and load the same data. (In row 1 the data is 01010101).
3. Repeat step 2 fourteen additional times until all sixteen columns are loaded.
4. Write the data.
5. Begin the next row by complementing the data and incrementing the address (data for the second row is 10101010).
6. Repeat steps 2, 3, 4 and 5 to complete the left upper bank (a total of 128 times).
7. Set A11 = 1, A12 = 0, and repeat steps 1, 2, 3, 4, 5 and 6 to complete the upper matrix.
8. Set A11 = 0, A12 = 1, and repeat steps 1, 2, 3, 4, 5 and 6 to complete the left half of the lower matrix.
9. Set A11 = 1, A12 = 1, and repeat steps 1, 2, 3, 4, 5 and 6 to complete the array.

An inverted checkerboard pattern may be generated by following the same procedure except that all the data must be complemented. (The data for address 0 would be 10101010.)





64K EEPROM BIT MAP

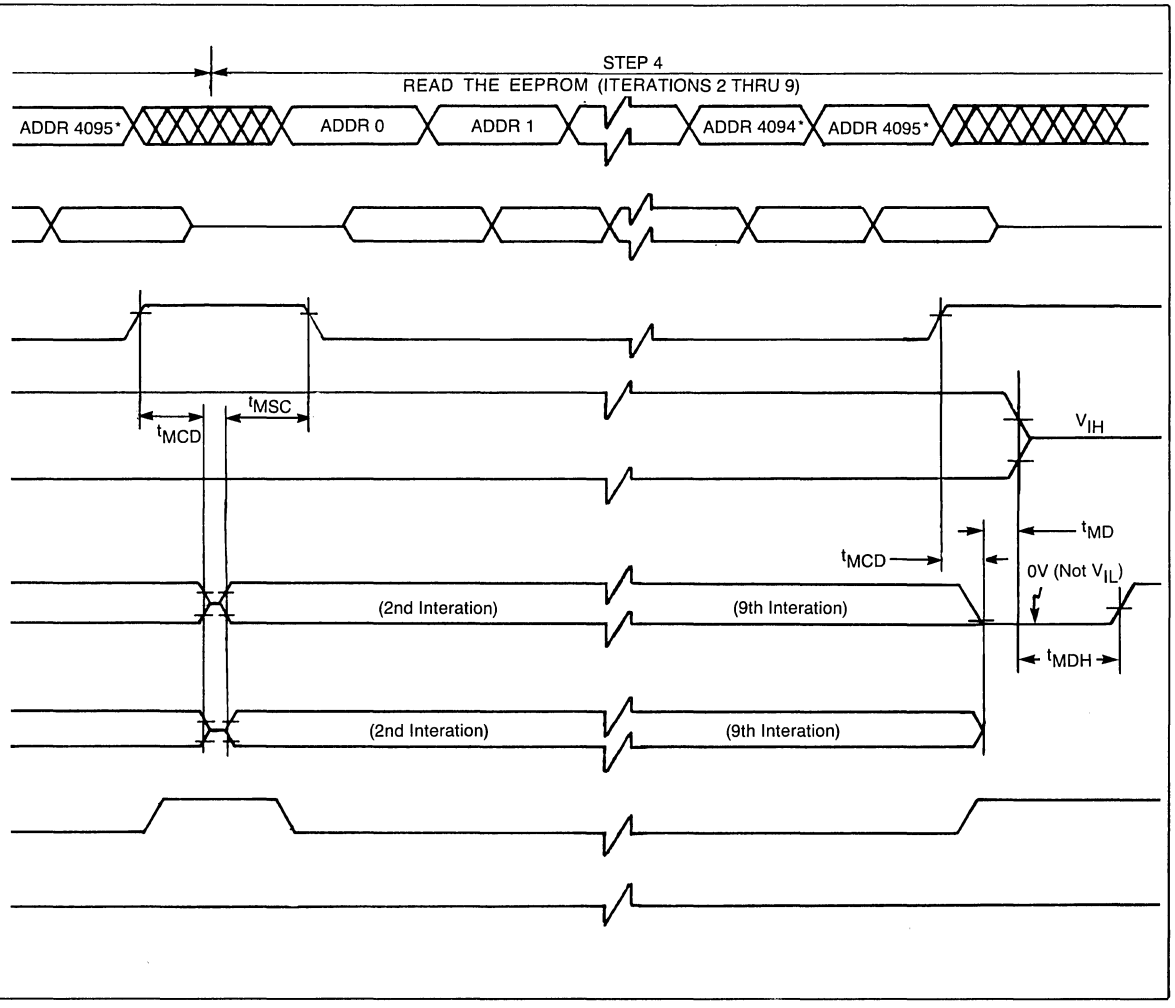


MARGINING WAVEFORMS 32K and 64K EEPROMS

* THIS IS THE LAST ADDRESS FOR THE 32K EEPROM ,THE LAST ADDRESS FOR THE 64K EEPROM IS 8191.
* * THESE ARE THE STEPS FOUND IN THE MEMORY MARGINING SECTION

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CNTL2 (MV)	MARGINING VOLTAGE	VCC = 5.0V	-5.0	SEE BINARY SEARCH SECTION	+5.0	V
CNTL1 (ME) 1's	MARGINING ENABLE 1's	VCC = 5.0 V	21.5	22.0	22.5	V
CNTL1 (ME) 0's	MARGINING ENABLE 0's	VCC = 5.0V	-6.5	-6.0	-5.5	V
t_{MS}	MARGINING SET-UP	—	50	—	—	μS
t_{ME}	MARGINING ENABLE	—	20	—	—	μS
t_{MVD}	MARGINING VOLTAGE DELAY	—	20	—	—	μS

TIMINGS



SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{MSC}	MARGINING VOLTAGE SET-UP BEFORE $\overline{CS}$	—	50	—	—	μS
t_{ACC}	ADDRESS ACCESS TIME	—	SEE APPROPRIATE SPECIFICATION			nS
t_{CS}	CHIP SELECT ACCESS TIME	—	SEE APPROPRIATE SPECIFICATION			nS
t_{MCD}	MARGINING VOLTAGE TO $\overline{CS}$ DELAY	—	0	—	—	nS
t_{MD}	MARGINING DISABLE	—	50	—	—	μS
t_{MDH}	MARGINING DISABLE TO CNTL2 (MV) HIGH	—	20	—	—	μS

NCR Microelectronics Division
8181 Byers Road
Miamisburg, Ohio 45342
Telex: 241669 NCR NVMEM MSBG
Phone: 1-800-543-5618 outside Ohio
1-513-866-7217 Ohio or International

NCR Semicustom Design

NCR SEMICUSTOM DESIGN

- **Performance—propagation delays less than LSTTL and HCMOS technologies.**
- **Advanced process technology—low power CMOS.**
- **Directly TTL and HCMOS Compatible—no interface or pullups required.**
- **Sophisticated CAD System—minimizes risk while easing and speeding design providing a first pass working part.**
- **Optional ROM, Static RAM, PLA and DSP—Customer definable in size and organization, with the option of analog and a core microprocessor on the same chip.**
- **Silicon Efficient—no fixed-routing channels or cell locations. NCR Semicustom Design allows close packing of high-level functions for minimum die size and lowest overall cost of any semicustom solution.**
- **Many 7400/5400 equivalent functions.**
- **Versatile in-house assembly capability for plastic and ceramic dual-in-line and chip carrier package types.**

NCR Semicustom Design offers you the same high performance, design flexibility and breadth of functions as a fully-customized integrated circuit, while simultaneously minimizing development time and cost. Key elements of the NCR system include computer-aided design (CAD) tools, advanced process technologies, total technical support and a wide selection of cell functions in a 3-micron CMOS standard cell library.

You can take the lead in design and development with NCR technical expertise and foundry facilities to aid you in finding and implementing the optimal solution to your needs. Every phase of the design and development process is followed up with the NCR state-of-the-art support system, permitting more freedom and security to explore alternatives at minimal cost.

Specifications subject to change without notice.

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COST

Compared to discrete logic, the use of an NCR cell library device to integrate system logic greatly reduces system power requirements, board space, component cost, manufacturing cost, weight, and overhead costs such as rework, inventory and purchasing. Reliability and performance will also be improved. All these factors directly impact unit pricing, particularly in volume production, making a cell library device a mandatory design choice.

DESIGN AND APPLICATIONS ASSISTANCE

You have the option of using one of the Semicustom Design Centers where fully-supported Daisy and Mentor Graphics workstations are available for your use, or you may prefer to purchase a workstation and design your device in your facility. In either case, NCR will provide full engineering support.

Options include:

- completing design verification in your facility.
- designing the device at the NCR facility or an NCR Design Center.
- permitting NCR or an NCR Design Center to perform design verification and provide a device which meets your logic specifications.

CAD TOOLS

Semicustom design and development are done with the most sophisticated tools available. NCR is committed to being the industry leader in technology, applications support and service. To meet this commitment, NCR has acquired and developed the best CAD tools that the industry can offer.

When using cell library technology, you have a choice of the Apollo-based Mentor Graphics workstation or the Daisy workstation, both of which have the extensive NCR CMOS cell library and user-friendly software. When using gate array technology, the Mentor Graphics workstation is supported. NCR design and applications engineers are available full-time to assist you in every phase of design and development, including hands-on training on a workstation. NCR is actively involved in the movement of CAD tools to engineering workstations, the development of new tools and the evaluation of those being developed and offered by other companies. We continue to have new NCR CAD programs in development.

NCR has developed proprietary software programs including timing analysis and test program generation to insure design accuracy and first pass success. For timing analysis, NCR has developed the VITA™ (VLSI Timing and Interconnect Analysis) package of programs. Release 3 of NODE DELAY and PATH DELAY features user prompts and keeps track of signal names for ease of use. PLUG DELAY provides feedback to logic simulators for realtime simulations. These programs can be run both before layout, using estimated interconnect capacitances, and after layout, using extracted capacitance values.

Layout, using NCR's CPR, a modification of an industry standard auto-place-and-route (APR) program, has become a streamlined activity producing excellent results. Designers have the option of having NCR perform the layout from a provided netlist and specifications, or by obtaining an industry standard APR for in-house use. NCR is also cooperating with industry efforts to develop APR capability on the Mentor Graphics and Daisy workstations.

For analog simulations, NCR will provide SPICE models for the cells, and full characterization data sheets.

The CAD Software Tools include the following:

- Schematic entry
- Netlist extraction
- Logic simulation—Tegas™ V and workstation based simulation, to guarantee functionality and eliminate design errors.
- Timing Analysis—VITA™ (VLSI Interconnect and Timing Analysis) uses both estimated interconnect capacitance and extracted interconnect capacitance to eliminate timing problems.
- Automatic place and route—CPR3, CAL-MP™—optimizes placement of cells and automatically routes the entire circuit, taking into account any specified critical paths for standard cells.
- Layout verification includes—Electrical Rule Checks (ERC), and Design Rule Checks (DRC), comparison of layout to the logical circuit description to verify place and route accuracy and search for "transistor-level" errors to ensure operation. Mentor CADISYS is the program used for checking ERC's and DRC's for gate arrays.
- Fault grading—Verifies test pattern quality.
- Test pattern generation—Automatically creates test vectors from logic simulation patterns.

Tegas™ is a registered trademark of General Electric—CALMA Co.

VITA™ is a registered trademark of NCR Corporation.

CAL–MP™ is a registered trademark of SILVAR-LISCO.

Daisy™ is a registered trademark of Daisy Systems, Inc.

Mentor Graphics™ is a registered trademark of Mentor Graphics Corporation.

NCR SEMICUSTOM PROCESS TECHNOLOGY

The NCR 3-micron drawn channel length CMOS process provides excellent performance. This process uses p-well silicon gate technology, positive photoresist, and projection alignment on 4-inch wafers.

NCR's CMOS is immume to most latch-up situations with latch-up protection of 90 mA at 12V. Worst case ESD (electro-static discharge) is rated at 2.5kV.

NCR's 3-micron CMOS technology has proven to be a very reliable high volume process which provides circuit densities and performances which are extremely competitive in today's market.

Manufacturing

Whether your semicustom design is performed by NCR, a design house, or yourself, NCR offers complete foundry services to meet your production requirements. Both 3-micron CMOS and NMOS foundry services are available.

Packaging

NCR's fast-turn assembly facility permits short development cycles and rapid ramp-up for initial production. In-house packaging includes plastic and ceramic DIPs and chip carriers. Off-shore packaging capabilities offer low cost volume on all packaging alternatives.

GATE ARRAY TECHNOLOGY

Gate arrays are a viable option if you have a low volume design or one requiring fewer functions and therefore fewer gates. Design and development cycles are customarily shorter and less costly for gate arrays. The trade-off is in design flexibility and production costs, since a cell library device is smaller and less costly in larger production quantities.

NCR design engineers will assist you in making the most cost-effective decision to meet your needs, whether is is a cell library device or a gate array.

CMOS II DIGITAL CELL LIBRARY

SSI Functions:

- Buffers/inverters
  - high drive
  - low drive
  - tri-state
  - schmitt trigger
- NAND/NOR
  - available with 2, 3, 4 inputs
- AND/OR
  - available with 8 inputs
- Combinational logic
  - AND-OR INVERTS and OR-AND INVERT
- Other
  - EXOR

Flip-Flops/Latches:

- Cross coupled latches
  - both NOR and NAND
- Level sensitive transparent latches
  - with Reset
  - without Reset
  - with clock driver
- Edge triggered D Flip-flops
  - with Reset
  - with Set and Reset
  - without Set and Reset
  - with clock driver, Set and Reset
- Edge triggered JK flip-flops
  - with Set and Reset
  - with Set, Reset and clock driver
- External 2-phase clock driver

MSI Functions:

- Two-to-one cascadeable multiplexer
- Single-bit cascadeable loaded shift register with serial or parallel in, and serial out, with or without clock driver
- Single-bit cascadeable, loadable, up-down counter with Reset and Enable, carry in and carry out

Input Pads and Buffers

For pad-limited designs and non-pad-limited designs:

- Standard
- Schmitt trigger

Output Pads and Buffers

For pad-limited designs and non-pad-limited designs:

- Standard drive = ± 3mA with TTL switchpoints
- High drive = ± 10mA with TTL switchpoints
- Open drain with or without pullup
- Tri-state
- TTL switchpoints at 1.4V or 1.9V

I/O Pads and Buffers

For pad-limited designs and non-pad-limited designs

- Standard drive
- High drive
- Open drain
- Tri-state

The variety of cells offered allows for optimization of silicon area. A smaller die size means better performance and lower costs.

CMOS II ANALOG CELL LIBRARY

- Op Amp
- Comparators
- Analog Switch
- Bandgap Voltage References
- Expandable Oscillators
- 8-bit D/A, 4-bit D/A, 6-bit D/A
- 8-bit A/D
- Sound Generator D/A
- Negative Supply generation, –5V
- Bias generators
- Logic Level Shifter
- Power-On-Reset

NCR QUALITY ASSURANCE

The NCR Microelectronics goal in all design projects is to meet or exceed the customer's quality and reliability requirements by building quality in. Each of NCR's processes and products has been extensively characterized and qualified. Design Assurance Engineers have worked closely with Standard Cell Designers and Computer-Aided-Design Software Engineers to help assure first pass design success for all customers using Standard Cells. Each cell has been fully characterized and subjected to the same rigorous reliability testing used to qualify the process itself. In addition to the initial qualification, the Quality Assurance Department samples parts from each product and performs ongoing reliability testing to maintain a high level of confidence in fabrication and assembly operations. Each part receives full functional testing and visual inspection prior to shipment.

As a result of exceedingly high standards and a desire to be a leader, NCR Microelectronics has one of the lowest part reject records in the industry.

NCR SEMICUSTOM DESIGN CENTER LOCATIONS

Custom Silicon, Inc.
600 Suffolk Street
Lowell, MA 01854
(617) 454-4600
Contact: David Guinther

Integrated Circuit Systems, Inc.
1012 W. Ninth Avenue
King of Prussia, PA 19406
(215) 265-8690
Contact: Ed Arnold

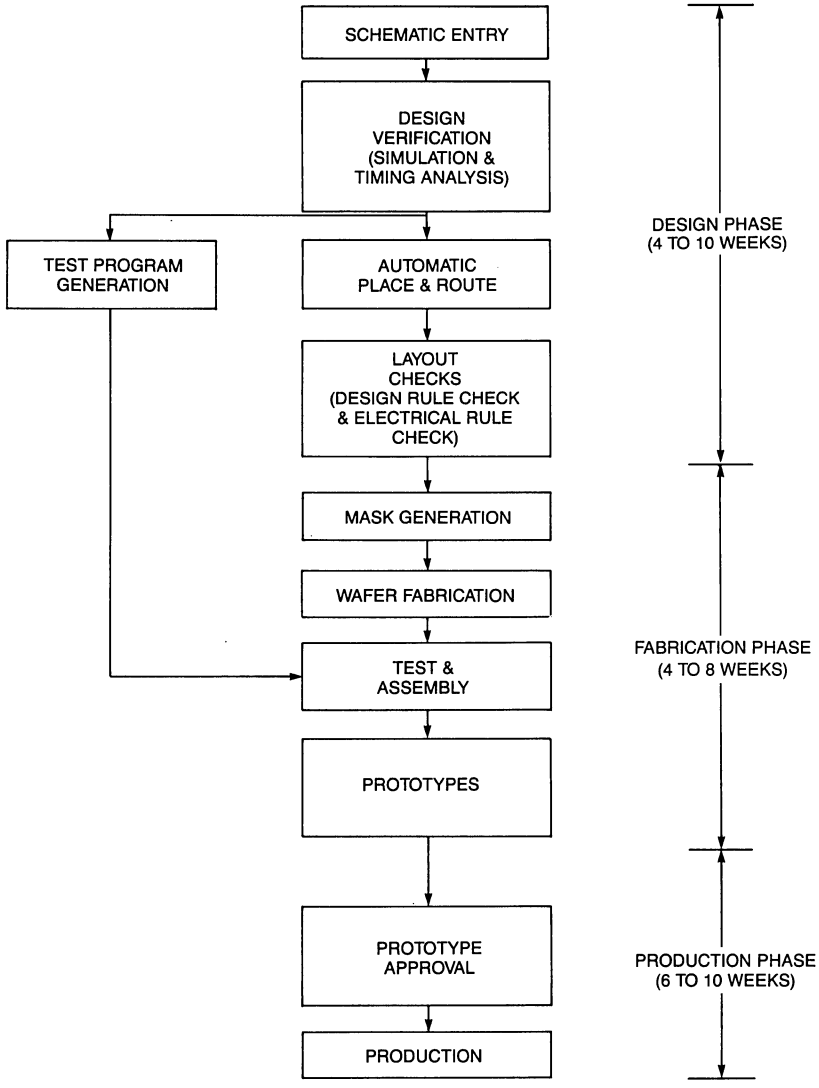
DNA, Inc.
9207 McAfee
Houston, TX 77031
(713) 778-9270
Contact: Steve Davis

Ontario Centre for Microelectronics
1150 Morrison Drive
Suite 400
Ottawa, Canada K2H9B8
Contact: Dr. Karl Siemens

Array Technology
992 S. Saratoga–Sunnyvale Road
San Jose, CA 95129
(408) 252-9900
Contact: Bill O'Neill

Manhattan-Skyline, Limited
Manhattan House
Bridge Road
Maidenhead
Berkshire SL6 8DB
ENGLAND
Maidenhead (0628) 75851
Contact: Stu Kitchener

Aptek Micro Systems, Inc.
700 N.W. 12th Avenue
Deerfield Beach, FL 33441
(305) 421-8450
Contact: Triygve (Trig) Ivesdal



NCR SEMICUSTOM DESIGN SYSTEM

NCR Microelectronics
2001 Danfield Ct.
Fort Collins, Colorado 80525
Telex: 45-4505 NCRMICRO FTCN
Phone: 303/226-9500, 303/223-5100

NCR CMOS II
DIGITAL STANDARD CELL LIBRARY

CROSS REFERENCE LISTING (Alphabetic by Cell)

Specifications subject to change without notice.

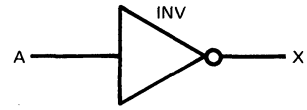
NCR

INVERTER

INV

CELL GEOMETRY

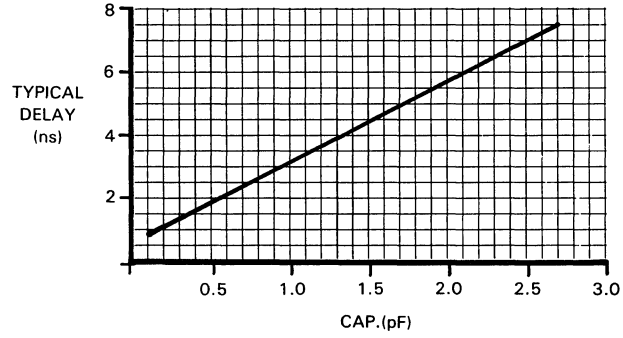
LOGIC SYMBOL



INPUT CAP. 0.11pF

INPUT: A
OUTPUT: X

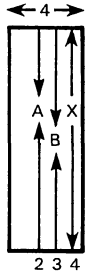
PROPAGATION CHART



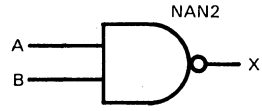
2-INPUT NAND GATE

NAN2

CELL GEOMETRY



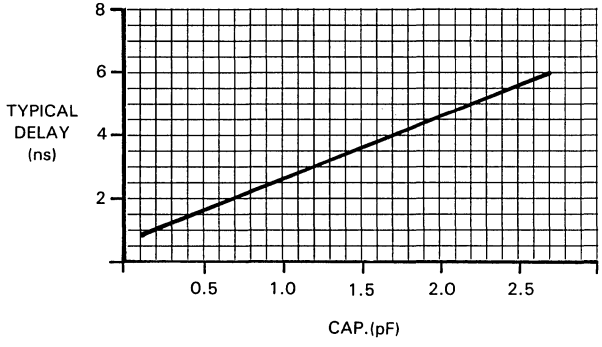
LOGIC SYMBOL



INPUT CAP. 0.14pF

INPUTS: A, B
OUTPUT: X

PROPAGATION CHART

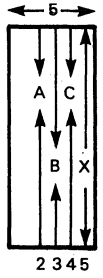


NCR

3-INPUT NAND GATE

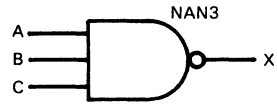
NAN3

CELL GEOMETRY



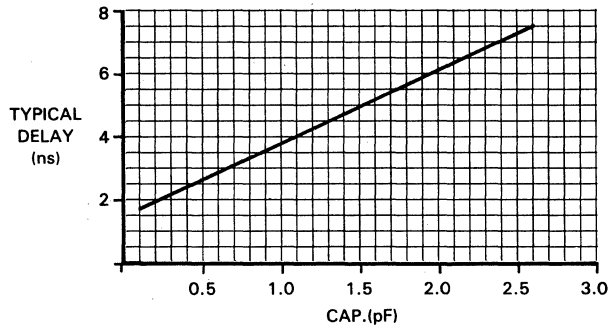
INPUT CAP. 0.16pF

LOGIC SYMBOL



INPUTS: A, B, C
OUTPUT: X

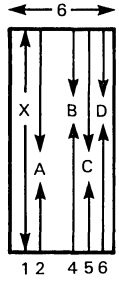
PROPAGATION CHART



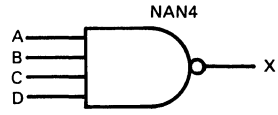
4-INPUT NAND GATE

NAN4

CELL GEOMETRY



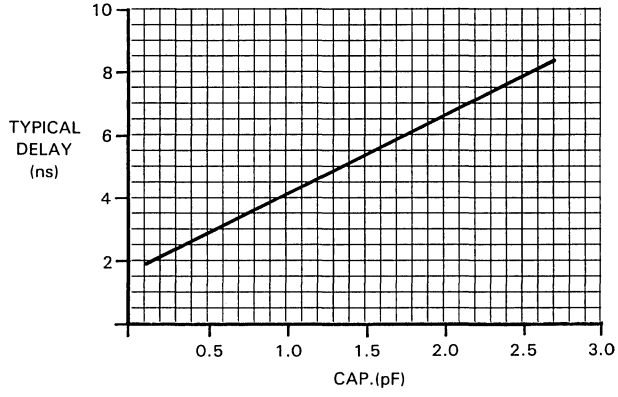
LOGIC SYMBOL



INPUT CAP. 0.15pF

INPUTS: A, B, C, D
OUTPUT: X

PROPAGATION CHART

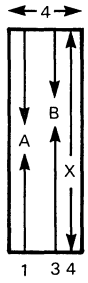


NCR

2-INPUT NOR GATE

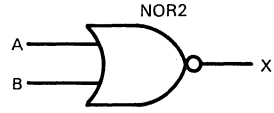
NOR2

CELL GEOMETRY



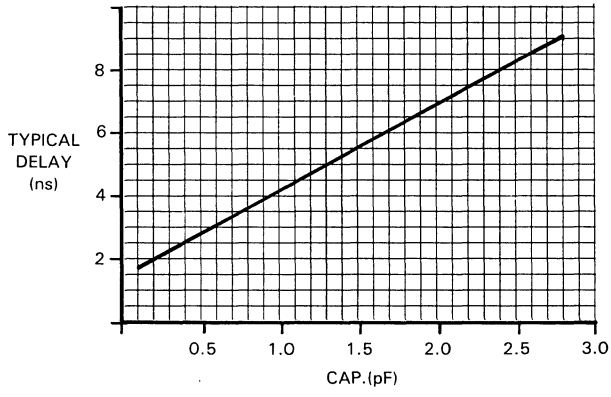
INPUT CAP. 0.15pF

LOGIC SYMBOL



INPUTS: A, B
OUTPUT: X

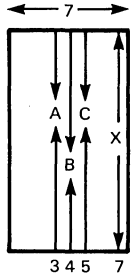
PROPAGATION CHART



3-INPUT NOR GATE

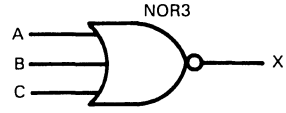
NOR3

CELL GEOMETRY



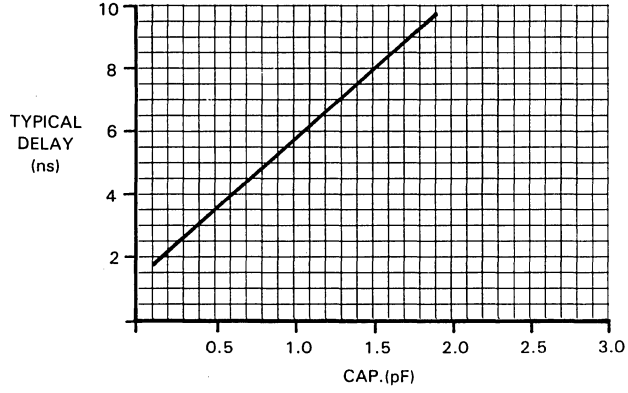
INPUT CAP. 0.23pF

LOGIC SYMBOL



INPUTS: A, B, C
OUTPUT: X

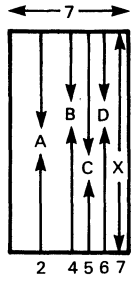
PROPAGATION CHART



4-INPUT NOR GATE

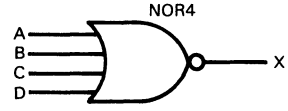
NOR4

CELL GEOMETRY



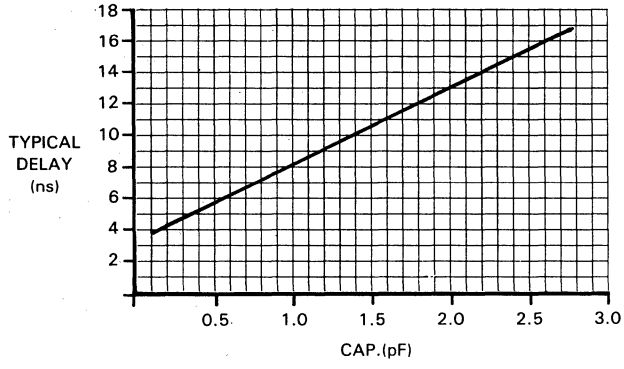
INPUT CAP. 0.18pF

LOGIC SYMBOL



INPUTS: A, B, C, D
OUTPUT: X

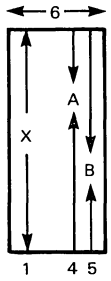
PROPAGATION CHART



EXCLUSIVE OR GATE

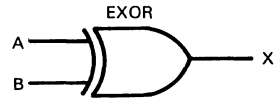
EXOR

CELL GEOMETRY



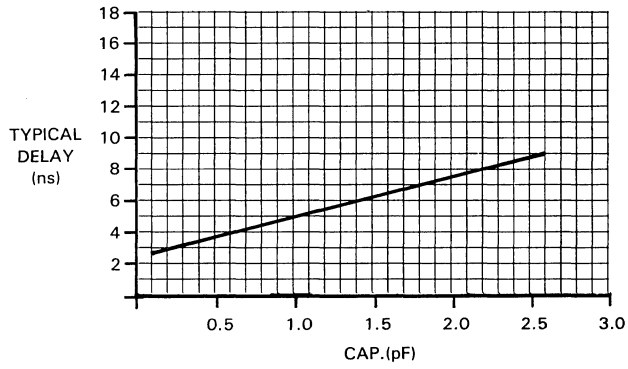
INPUT CAP. 0.12pF

LOGIC SYMBOL



INPUTS: A, B
OUTPUT: X

PROPAGATION CHART

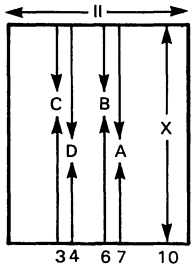


NCR

2-1-1 AND-OR-INVERT

AOI211

CELL GEOMETRY

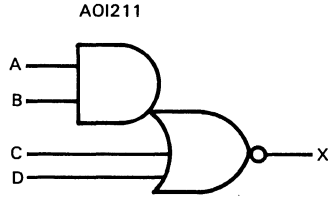


INPUT CAP. 0.30pF

INPUTS: A, B, C, D
OUTPUT: X

Minimum pulse width: 12ns

LOGIC SYMBOL

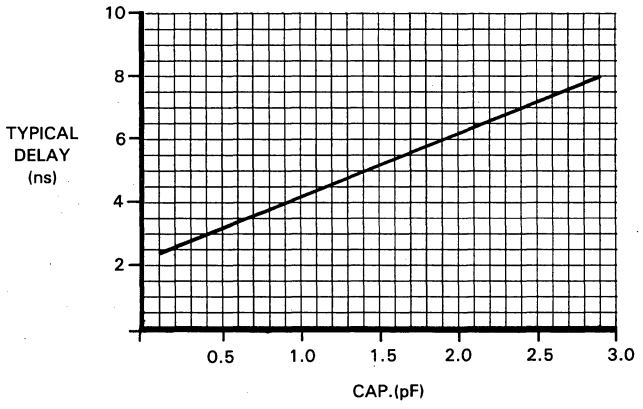


TRUTH TABLE

A	B	C	D	X
1	1	X	X	0
X	X	1	X	0
X	X	X	1	0
X	0	0	0	1
0	X	0	0	1

$X = \overline{AB + C + D}$

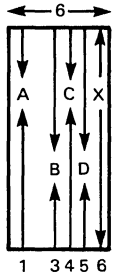
PROPAGATION CHART



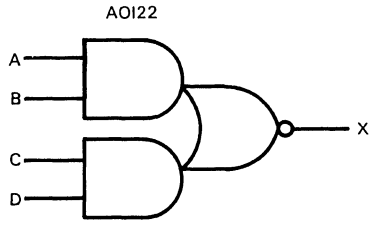
2-2 AND-OR-INVERT

AOI22

CELL GEOMETRY



LOGIC SYMBOL



TRUTH TABLE

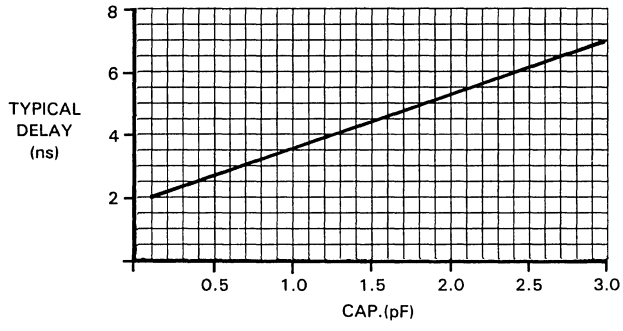
A	B	C	D	X
1	1	X	X	0
X	X	1	1	0
X	0	X	0	1
X	0	0	X	1
0	X	X	0	1
0	X	0	X	1

$X = \overline{AB + CD}$

INPUT CAP. 0.23pF

INPUTS: A, B, C, D
OUTPUT: X

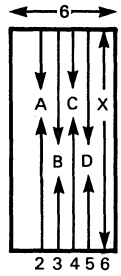
PROPAGATION CHART



3-1 AND-OR-INVERT

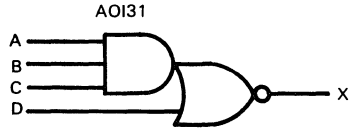
AOI31

CELL GEOMETRY



INPUT CAP. 0.25pF

LOGIC SYMBOL



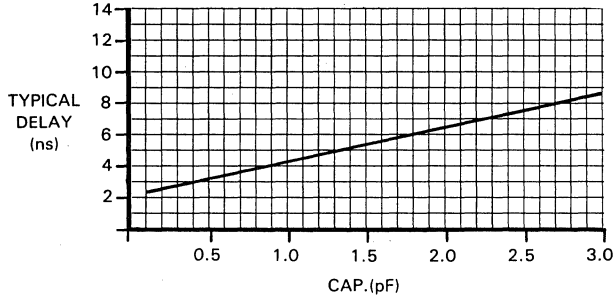
TRUTH TABLE

A	B	C	D	X
X	X	X	1	0
1	1	1	X	0
0	X	X	0	1
X	0	X	0	1
X	X	0	0	1

$X = \overline{ABC + D}$

INPUTS: A, B, C, D
OUTPUT: X

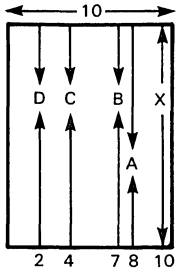
PROPAGATION CHART



3-1 OR-AND-INVERT

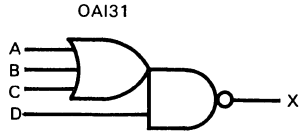
OAI31

CELL GEOMETRY



INPUT CAP. 0.29pF

LOGIC SYMBOL



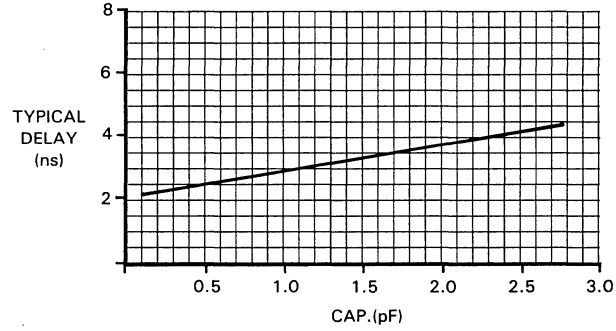
TRUTH TABLE

A	B	C	D	X
X	X	X	0	1
0	0	0	X	1
1	X	X	1	0
X	1	X	1	0
X	X	1	1	0

$X = \overline{(A + B + C) \cdot D}$

INPUTS: A, B, C, D
OUTPUT: X

PROPAGATION CHART

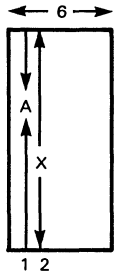


NCR

HIGH DRIVE BUFFER

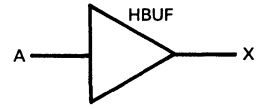
HBUF

CELL GEOMETRY



INPUT CAP. 0.18pF

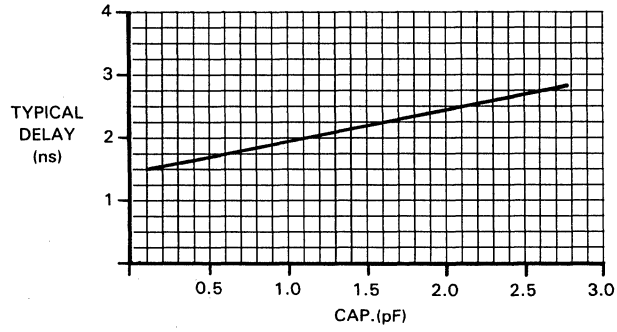
LOGIC SYMBOL



This is a high drive non-inverting buffer. The HBUF can be used to generate inverted output signals when it drives an inverting output pad.

INPUT: A
OUTPUT: X

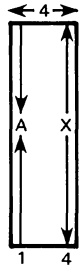
PROPAGATION CHART



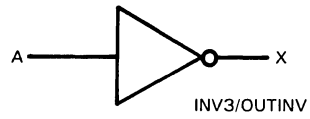
HIGH DRIVE INVERTER/OUTPUT BUFFER

INV3 AND OUTINV

CELL GEOMETRY



LOGIC SYMBOL

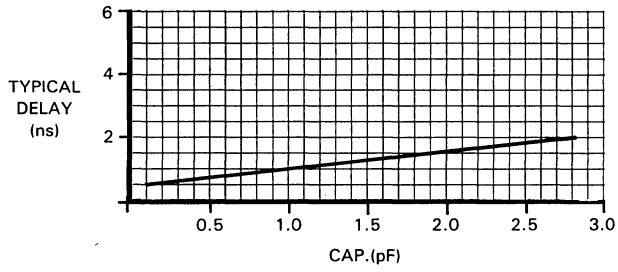


INPUT CAP. 0.31pF

Both INV3 and OUTINV are high drive inverters. OUTINV is used as a buffer for output pads.

INPUT: A
OUTPUT: X

PROPAGATION CHART

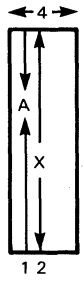


NCR

MEDIUM DRIVE BUFFER

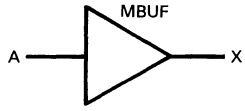
MBUF

CELL GEOMETRY



INPUT CAP. 0.11pF

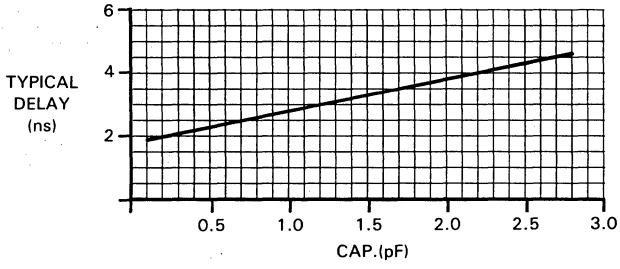
LOGIC SYMBOL



RMBUF is a medium drive non-inverting buffer.

INPUT: A
OUTPUT: X

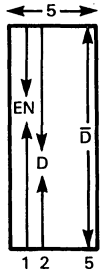
PROPAGATION CHART



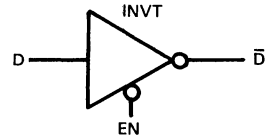
INVERTING TRI-STATE DRIVER

INVT

CELL GEOMETRY



LOGIC SYMBOL

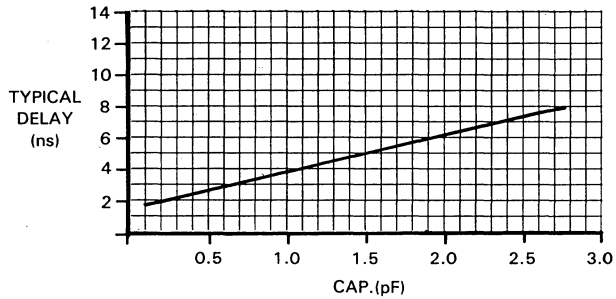


INPUT CAP. 0.20pF
OUTPUT CAP. 0.25pF

This driver inverts the signal when EN is low. When EN is high, the output is hi-Z.

INPUTS: D, EN
OUTPUT: $\bar{D}$

PROPAGATION CHART

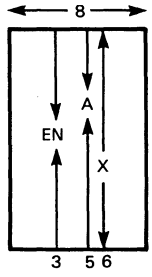


NCR

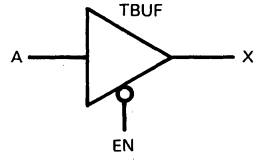
NON-INVERTING TRI-STATE BUFFER

TBUF

CELL GEOMETRY



LOGIC SYMBOL

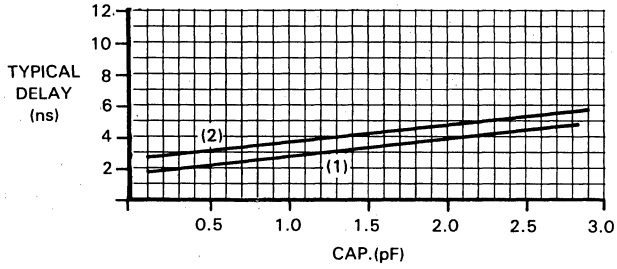


INPUT CAP.	A, EN	0.19pF
OUTPUT CAP.	X	0.37pF

EN is active low. When EN is high, the output is hi-Z.

INPUTS: A, EN
OUTPUT: X

PROPAGATION CHART

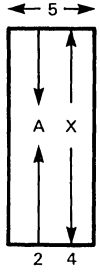


(1) A → X
(2) EN → X

SCHMITT TRIGGERS

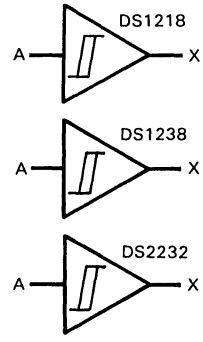
DS1218, DS1238, DS2232

CELL GEOMETRY



INPUT CAP. 0.12pF

LOGIC SYMBOL

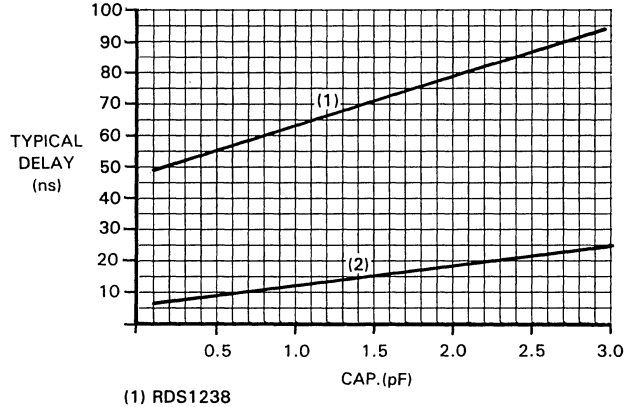


The Schmitt trigger can be used in place of INBUF.

RDS1218	RDS1238	RDS2232
$V_{TH\ HIGH}$ = 1.8V	$V_{TH\ HIGH}$ = 3.8V	$V_{TH\ HIGH}$ = 3.2V
$V_{TH\ LOW}$ = 1.2V	$V_{TH\ LOW}$ = 1.2V	$V_{TH\ LOW}$ = 2.2V

INPUT: A
OUTPUT: X

PROPAGATION CHART



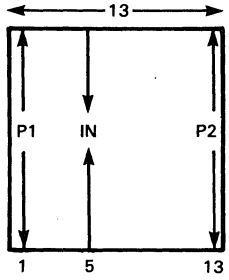
(1) RDS1238
(2) RDS1218, RDS2232

NCR

TWO-PHASE CLOCK

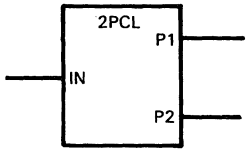
2PCL

CELL GEOMETRY



INPUT CAP. 0.18pF

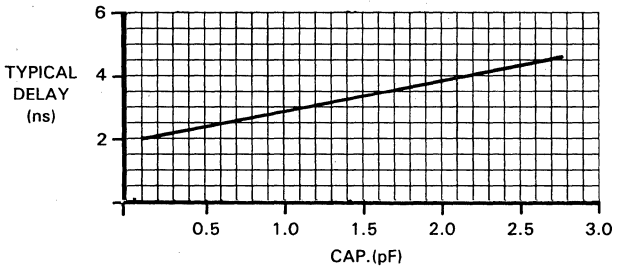
LOGIC SYMBOL



2PCL is for use with clocked cells. A positive edge triggered cell is created by connecting P1 to $\overline{CK}$ and P2 to CK. A negative edge triggered cell is created by connecting P1 to CK and P2 to $\overline{CK}$.

INPUT: IN
OUTPUTS: P1, P2

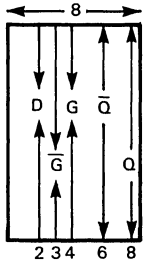
PROPAGATION CHART



TRANSPARENT LATCH

LAT

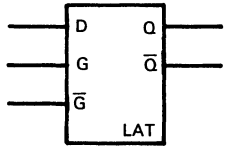
CELL GEOMETRY



INPUT CAP.

D	0.38pF
G & $\overline{G}$	0.10pF

LOGIC SYMBOL



TRUTH TABLE

D	G	Q	$\overline{Q}$
0	1	0	1
1	1	1	0
X	0	Q_o	$\overline{Q}_o$

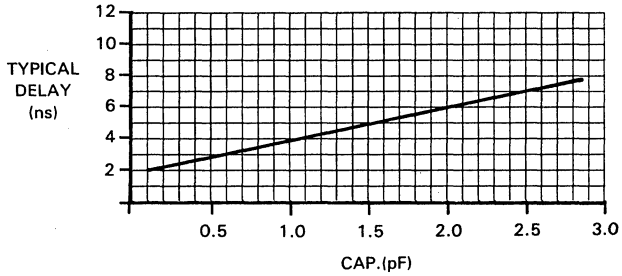
Q_o = the level of Q before these input conditions were established.

This level sensitive latch holds data when G is low, and is transparent when G is high. G and $\overline{G}$ are complimentary signals. This cell is buffered internally.

INPUTS: D, G, $\overline{G}$
OUTPUTS: Q, $\overline{Q}$

DATA SETUP TIME: 10ns
DATA HOLD TIME: 5ns

PROPAGATION CHART

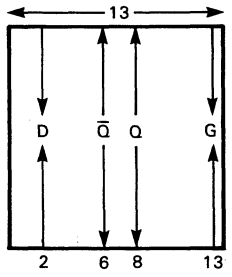


NCR

TRANSPARENT LATCH WITH CLOCK DRIVER

T2LAT

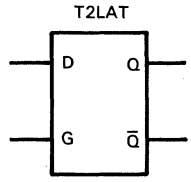
CELL GEOMETRY



INPUT CAP.

D	0.38pF
G	0.15pF

LOGIC SYMBOL



TRUTH TABLE

D	G	Q
0	1	0
1	1	1
X	0	Q_o

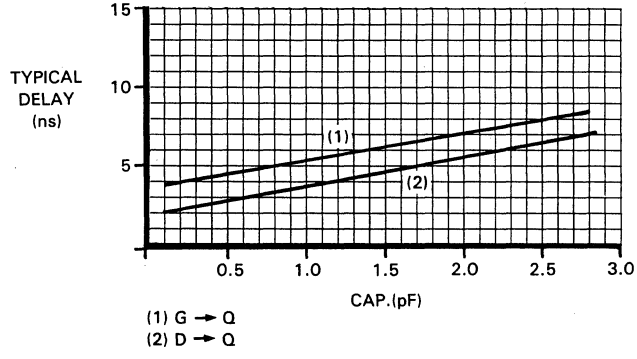
Q_o = the level of Q before these input conditions were established.

This level sensitive latch holds data when G is low, and is transparent when G is high. This cell is not buffered internally.

INPUTS: D, G
OUTPUTS: Q, $\overline{Q}$

SETUP TIME: 10ns
HOLD TIME: 5ns

PROPAGATION CHART

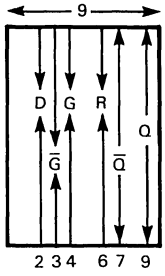


(1) G → Q
(2) D → Q

TRANSPARENT LATCH WITH RESET

LATR

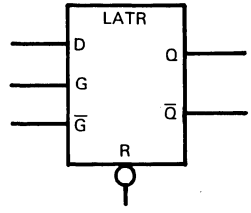
CELL GEOMETRY



INPUT CAP.

D	0.45pF
G & $\overline{G}$	0.10pF
R	0.16pF

LOGIC DIAGRAM



TRUTH TABLE

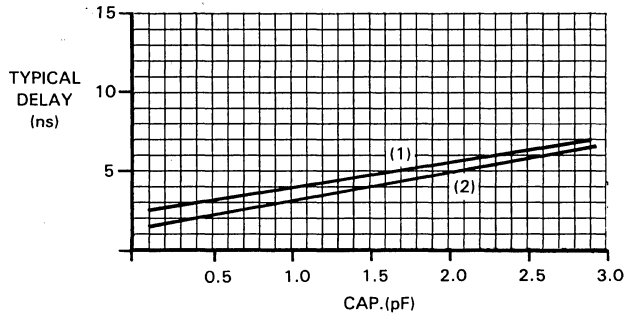
R	D	G	Q
0	X	X	0
1	0	1	0
1	1	1	1
1	X	0	Q_o

Q_o = the level of Q before these input conditions were established.

This latch holds data when G is low, and is transparent when G is high. R is asynchronous and active low. G and $\overline{G}$ are complimentary signals. This cell is buffered internally.

INPUTS: R, D, G, $\overline{G}$
OUTPUTS: Q, $\overline{Q}$
DATA SETUP TIME: 10ns
DATA HOLD TIME: 5ns

PROPAGATION CHART

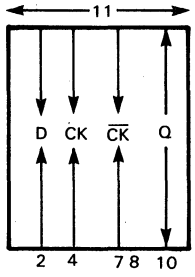


(1) G → Q
(2) R → Q

D FLIP-FLOP

DFF

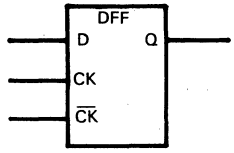
CELL GEOMETRY



INPUT CAP.

D	0.22pF
CK & $\overline{CK}$	0.12pF

LOGIC SYMBOL



TRUTH TABLE

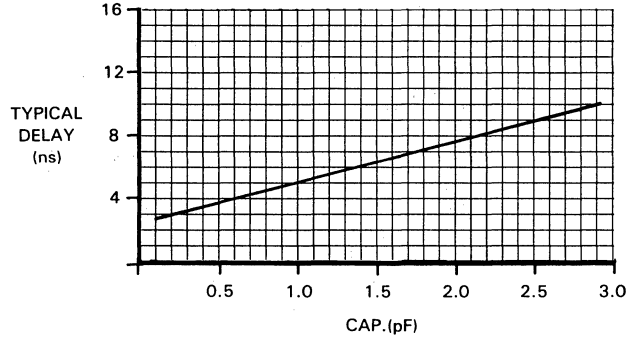
D	CK	Q
0	↓	0
1	↓	1

DFF is a fully static D-type edge triggered flip-flop. Complimentary clock signals (CK and $\overline{CK}$) are required. It is negative edge triggered with respect to CK. This cell is not buffered internally.

INPUTS: D, CK, $\overline{CK}$
OUTPUTS: Q

DATA SETUP TIME: 10ns
DATA HOLD TIME: 5ns

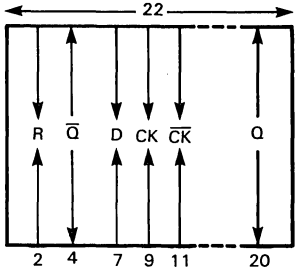
PROPAGATION CHART



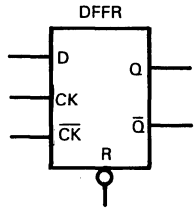
D FLIP-FLOP WITH RESET

DFFR

CELL GEOMETRY



LOGIC SYMBOL



TRUTH TABLE

D	CK	R	Q	Q̄
0	↓	1	0	1
1	↓	1	1	0
X	X	0	0	1

INPUT CAP.

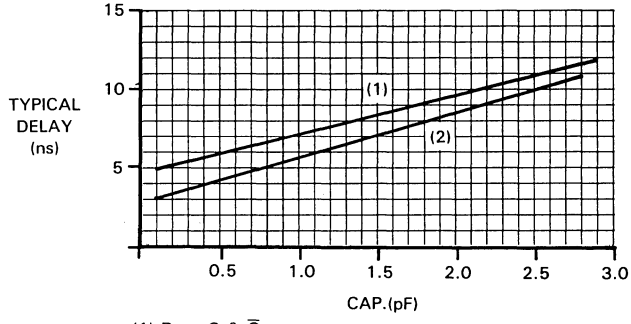
D	0.22pF
R	0.16pF
CK & $\overline{CK}$	0.19pF

DFFR is a fully static D-type edge-triggered flip-flop. R is asynchronous and low active. Complimentary clock signals (CK and $\overline{CK}$) are required. It is negative edge triggered with respect to CK.

INPUTS: R, D, CK, $\overline{CK}$
OUTPUTS: Q, $\overline{Q}$

DATA SETUP TIME: 10ns
DATA HOLD TIME: 5ns

PROPAGATION CHART



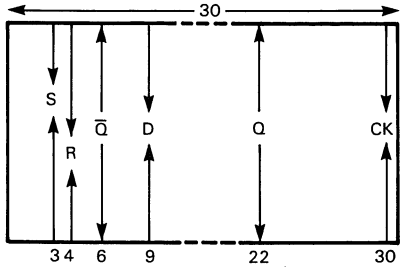
(1) R to Q & $\overline{Q}$
(2) CK to Q & $\overline{Q}$

NCR

D FLIP FLOP WITH SET & RESET

LS74

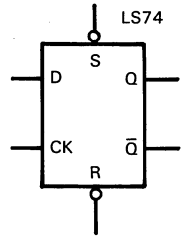
CELL GEOMETRY



INPUT CAP.

D	0.22pF
R & S	0.19pF
CK	0.15pF

LOGIC SYMBOL



TRUTH TABLE

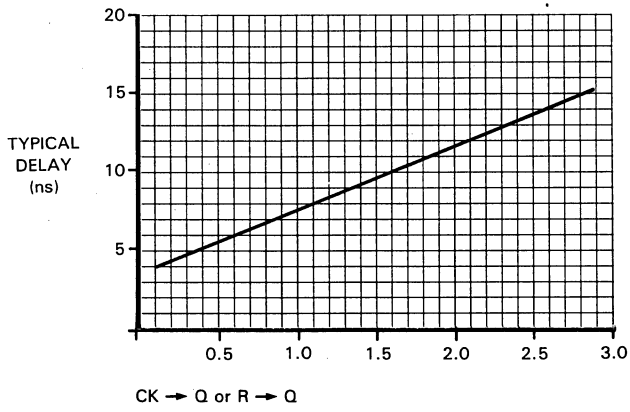
S	R	CK	D	Q	Q̄
1	1	↑	0	0	1
1	1	↑	1	1	0
0	0	X	X	0	0
0	1	X	X	1	0
1	0	X	X	0	1

LS74 is a fully static D-type positive edge triggered Flip Flop. S and R are asynchronous and are active low. This cell is functionally compatible with a TTL 74LS74.

INPUTS: D, CK, S, R
OUTPUTS: Q, $\overline{Q}$

DATA SETUP TIME: 10ns
DATA HOLD TIME: 5ns

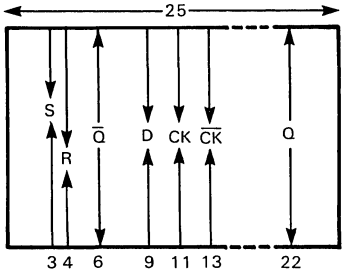
PROPAGATION CHART



D FLIP FLOP WITH SET & RESET

DFFRS

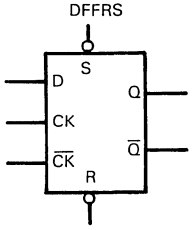
CELL GEOMETRY



INPUT CAP.

D	0.22pF
R & S	0.19pF
CK & $\overline{CK}$	0.16pF

LOGIC SYMBOL



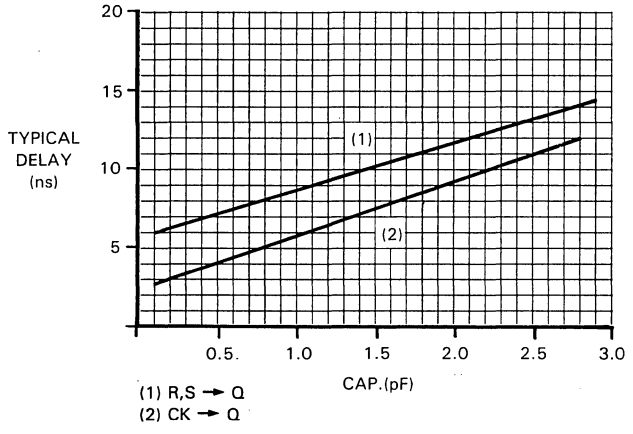
TRUTH TABLE

S	R	CK	D	Q	$\overline{Q}$
1	1	↓	0	0	1
1	1	↓	1	1	0
1	0	X	X	0	1
0	1	X	X	1	0
0	0	X	X	0	0

DFFRS is a fully static D-type edge triggered flip-flop. S and R are asynchronous and are active low. Complimentary clock signals (CK & $\overline{CK}$) are required. It is negative edge triggered with respect to CK.

INPUTS: R, S, D, CK, $\overline{CK}$
OUTPUTS: Q, $\overline{Q}$
DATA SETUP TIME: 10 ns
DATA HOLD TIME: 5 ns

PROPAGATION CHART

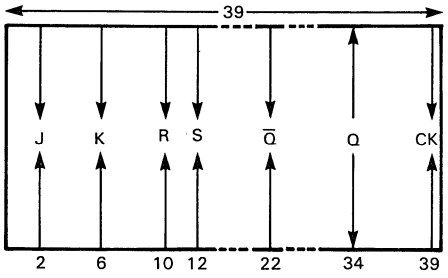


NCR

J-K FLIP-FLOP

LS76

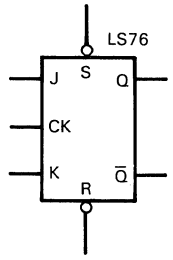
CELL GEOMETRY



INPUT CAP.

J & K	0.13pF
R & S	0.23pF
CK	0.15pF

LOGIC SYMBOL



TRUTH TABLE

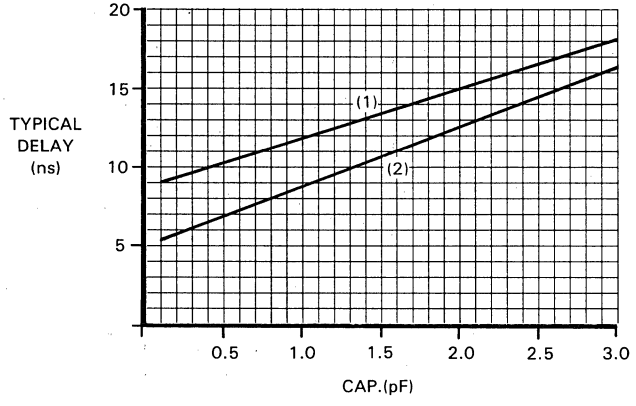
CK	S	R	J	K	Q	$\overline{Q}$
↓	1	1	1	1	TOGGLE	TOGGLE
↓	1	1	1	0	1	0
↓	1	1	0	1	0	1
↓	1	1	0	0	Q_o	$\overline{Q}_o$
X	0	1	X	X	1	0
X	1	0	X	X	0	1
X	0	0	X	X	0	0

JKFF is a fully static JK-type negative edge triggered flip-flop. S and R are asynchronous and are active low. This cell is functionally compatible with a TTL 74LS76.

INPUTS: J, K, R, S, CK
OUTPUTS: Q, $\overline{Q}$

MIN. CLOCK WIDTH: 11ns
MIN. R & S WIDTH: 15ns
J SETUP TIME: 13ns
K SETUP TIME: 10ns
HOLD TIME: 5 ns

PROPAGATION CHART

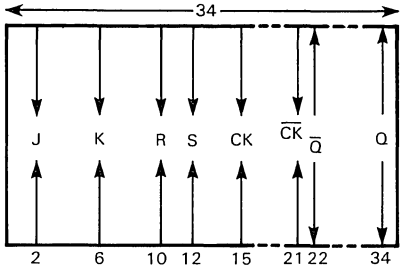


(1) R & S → Q & $\overline{Q}$
(2) CK → Q

J-K FLIP-FLOP

JKFF

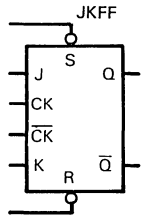
CELL GEOMETRY



INPUT CAP.

J & K	0.13pF
R & S	0.23pF
CK & $\overline{CK}$	0.24pF

LOGIC SYMBOL



TRUTH TABLE

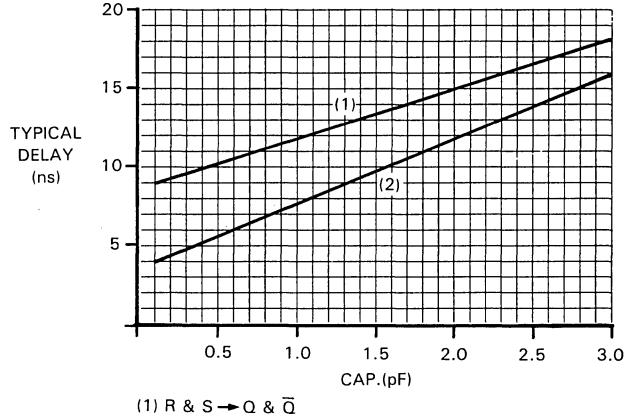
CK	S	R	J	K	Q	$\overline{Q}$
↓	1	1	1	1	TOGGLE	TOGGLE
↓	1	1	1	0	1	0
↓	1	1	0	1	0	1
↓	1	1	0	0	Q_o	$\overline{Q}_o$
X	0	1	X	X	1	0
X	1	0	X	X	0	1
X	0	0	X	X	0	0

JKFF is a fully static JK-type edge triggered flip-flop. S and R are asynchronous and are active low. Complimentary clock signals (CK and $\overline{CK}$) are required. It is negative edge triggered with respect to CK.

INPUTS: J, K, R, S, CK, $\overline{CK}$
OUTPUTS: Q, $\overline{Q}$

MIN. CLOCK WIDTH: 11 ns
MIN. R & S WIDTH: 15 ns
J & K SETUP TIME: 18 ns
HOLD TIME: 5 ns

PROPAGATION CHART



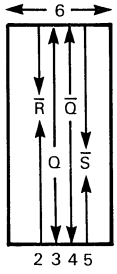
(1) R & S → Q & $\overline{Q}$
(2) CK → Q & $\overline{Q}$

NCR

CROSS-COUPLED NAND LATCH

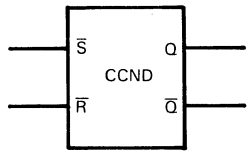
CCND

CELL GEOMETRY



INPUT CAP. 0.12pF

LOGIC SYMBOL



TRUTH TABLE

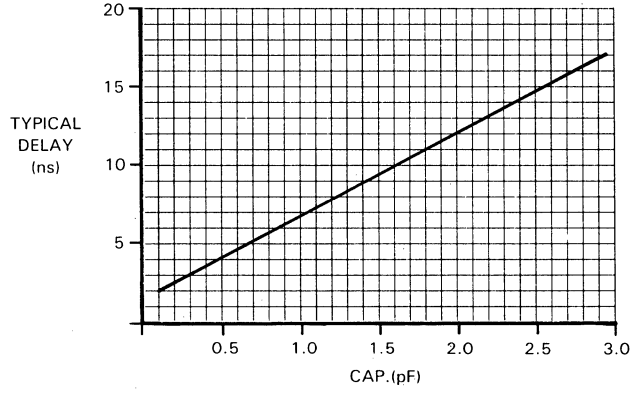
S̄	R̄	Q	Q̄
0	0	1	1
1	0	0	1
0	1	1	0
1	1	Q_o	$\bar{Q}_o$

CCND is very susceptible to negative going glitches on $\bar{S}$ or $\bar{R}$. This cell is not buffered internally.

INPUTS: $\bar{S}$, $\bar{R}$
OUTPUTS: Q, $\bar{Q}$

Minimum pulse width: 10 ns

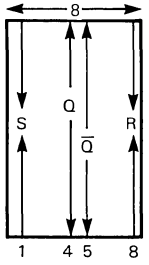
PROPAGATION CHART



CROSS-COUPLED NOR LATCH

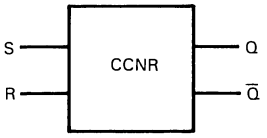
CCNR

CELL GEOMETRY



INPUT CAP. 0.15pF

LOGIC SYMBOL



TRUTH TABLE

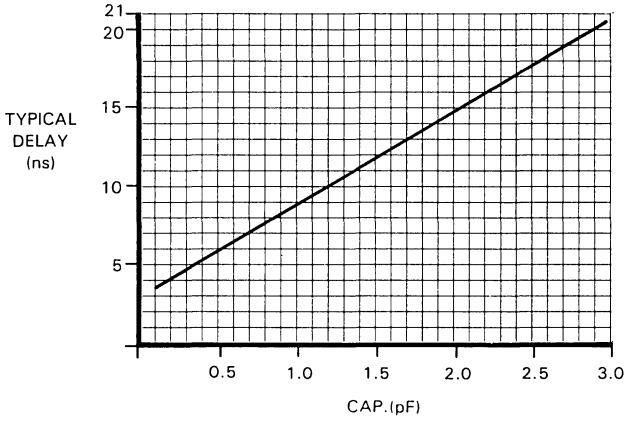
S	R	Q	$\overline{Q}$
0	0	Q_o	$\overline{Q}_o$
0	1	0	1
1	0	1	0
1	1	0	0

CCNR is very susceptible to positive going glitches on S or R. This cell is not buffered internally.

INPUTS: S, R
OUTPUTS: Q, $\overline{Q}$

Minimum pulse width: 10ns

PROPAGATION CHART

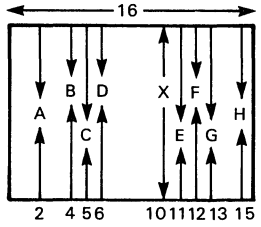


NCR

8-INPUT OR GATE

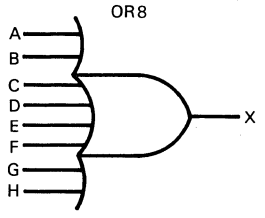
OR8

CELL GEOMETRY



INPUT CAP. 0.18pF

LOGIC SYMBOL

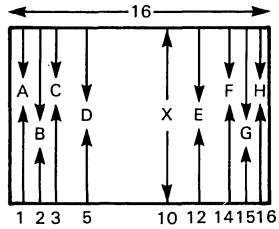


INPUT: A, B, C, D, E, F, G, H
OUTPUT: X

8-INPUT AND GATE

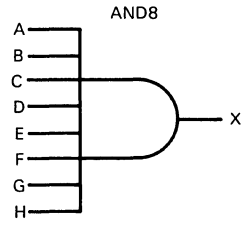
AND8

CELL GEOMETRY



INPUT CAP. 0.28pF

LOGIC SYMBOL



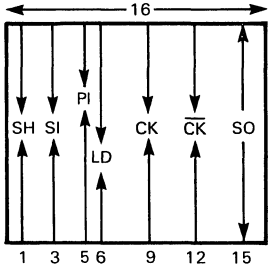
INPUTS: A, B, C, D, E, F, G, H
OUTPUT: X

NCR

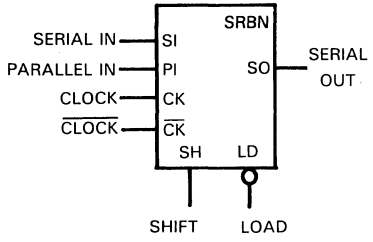
SHIFT REGISTER

SRBN

CELL GEOMETRY



LOGIC SYMBOL



TRUTH TABLE

SH	SI	LD	PI	CK	SO
1	0	1	X	↓	0
1	1	1	X	↓	1
0	X	0	0	↓	0
0	X	0	1	↓	1
1*	X	0*	X	↓	*
0*	X	1*	X	↓	*

* = ILLEGAL INPUT COMBINATION

INPUT CAP.

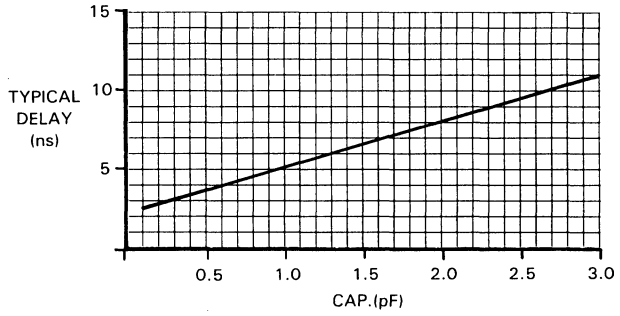
SH & $\overline{LD}$	0.08pF
CK & $\overline{CK}$	0.13pF
PI & SI	0.57pF

SRBN is a 1-bit edge triggered shift register. It is negative edge triggered with respect to CK. Serial input is clocked in when SH is high. Parallel input is clocked in when LD is low. SH and LD can be tied together during normal operation. This cell is not buffered internally.

INPUTS: SI, SH, PI, LD, CK, $\overline{CK}$
OUTPUT: SO

SETUP TIME: SH, SI, PI, LD 10ns
HOLD TIME: 5ns

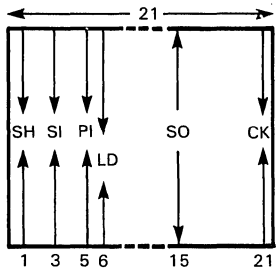
PROPAGATION CHART



SHIFT REGISTER

T2SR1N and T2SR1P

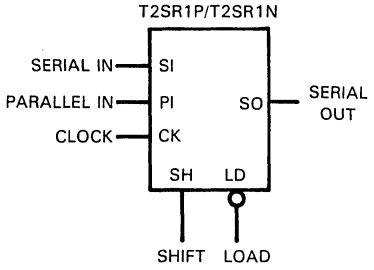
CELL GEOMETRY



INPUT CAP.

SH, LD	0.08pF
CL	0.15pF
PI, SI	0.57pF

LOGIC SYMBOL



TRUTH TABLE

SH	SI	LD	PI	CK	SO
1	0	1	X	↓	0
1	1	1	X	↓	1
0	X	0	0	↓	0
0	X	0	1	↓	1
0	X	1	X	X	SO_0
1	X	0	X	X	*

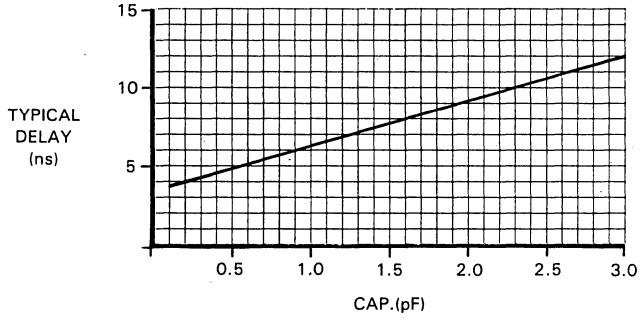
* = ILLEGAL INPUT COMBINATION

T2SR1N and T2SR1P are single-bit edge triggered shift registers. Serial input is clocked in when SH is high. Parallel input is clocked in when LD is low. SH and LD can be tied together during normal operation. T2SR1N is negative edge triggered and T2SR1P is positive edge triggered. This cell is not buffered internally.

INPUTS: SI, SH, PI, LD, CK
OUTPUT: SO

SETUP TIME: SH, SI, PI, LD 10ns
HOLD TIME: 5ns

PROPAGATION CHART

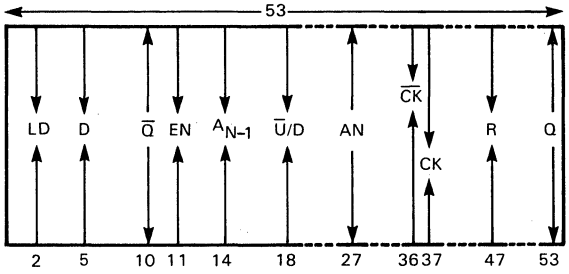


NCR

UP/DOWN COUNTER

UDC

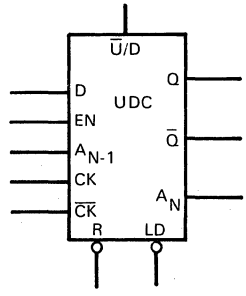
CELL GEOMETRY



INPUT CAP.

$\overline{U}/D$, CK, $\overline{CK}$	0.32pF
LD, EN	0.13pF
A_{N-1}, R	0.22pF
D	0.64pF

LOGIC SYMBOL



TRUTH TABLE

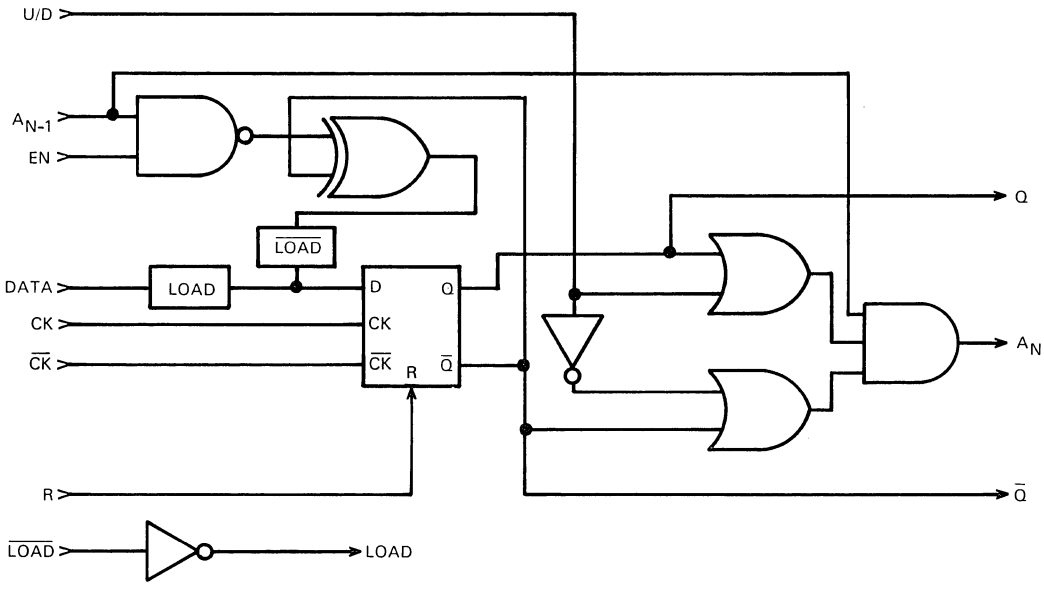
R	D	LD	EN	A_{N-1}	$\overline{U}/D$	CK	Q	AN
0	X	X	X	0	X	X	0	0
0	X	X	X	X	0	X	0	0
0	X	X	X	1	1	X	0	1
X	X	X	X	0	X	X		0
1	D	0	X	0	X	↓	D	0
1	D	0	X	1	0	↓	D	D
1	D	0	X	1	1	↓	D	$\overline{D}$
1	X	1	0	X	X	↓	Q_0	
1	X	1	1	0	X	↓	Q_0	
1	X	1	1	1	0	↓	Toggle	$\overline{Q}_0$
1	X	1	1	1	1	↓	Toggle	Q_0

UDC is a 1-bit, cascadeable Up-Down Counter. The EN input enables counting when high. Loading and counting functions operate on the negative edge of CK. Reset is asynchronous and complimentary clocks (CK and $\overline{CK}$) are required. A_N is the ripple carry output and A_{N-1} is a carry from the previous cell.

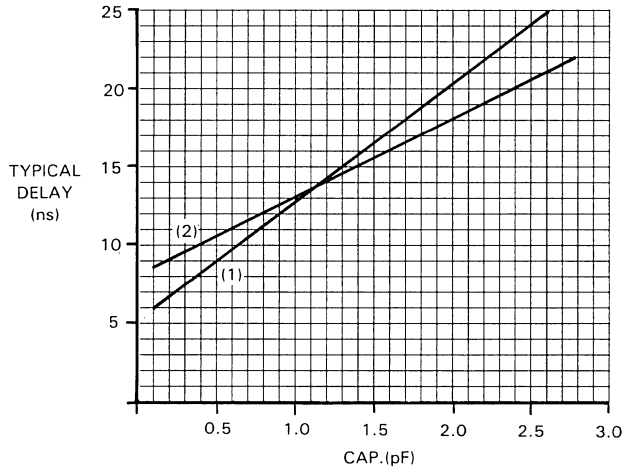
INPUTS: R, D, LD, EN, AN-1, $\overline{U}/D$, CK, $\overline{CK}$
OUTPUTS: AN, Q, $\overline{Q}$

DATA SETUP TIME: 10ns
DATA HOLD TIME: 5ns

FUNCTIONAL BLOCK DIAGRAM



PROPAGATION CHART

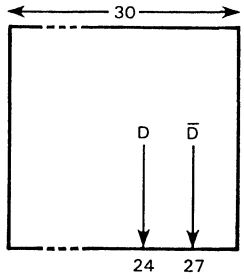


(1)CK TO Q & $\overline{Q}$
(2) R TO Q & $\overline{Q}$

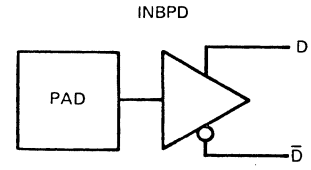
INPUT PAD WITH BUFFER

INBPD

CELL GEOMETRY



LOGIC SYMBOL

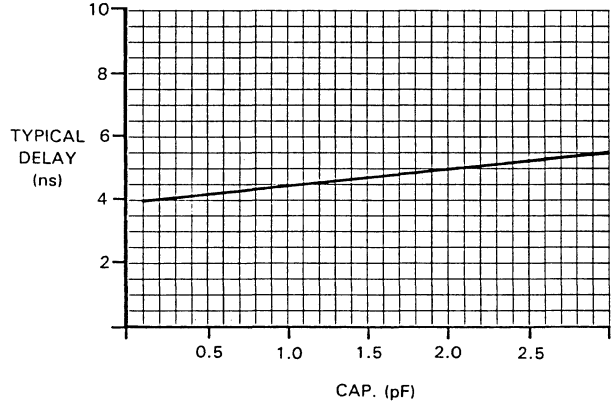


INPUT CAP. 3.5pF

For use in designs that are **not** pad-limited. D and $\overline{D}$ are **not** designed for minimum skew when both are loaded.

INPUT: PAD
OUTPUTS: D, $\overline{D}$

PROPAGATION CHART*

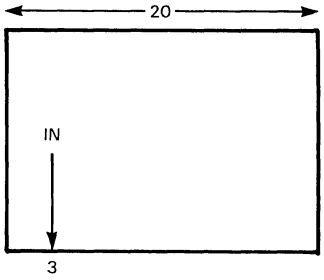


*From Switch Point (1.4v) to Output (2.5v).

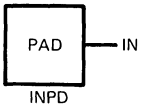
INPUT PAD

INPD

CELL GEOMETRY



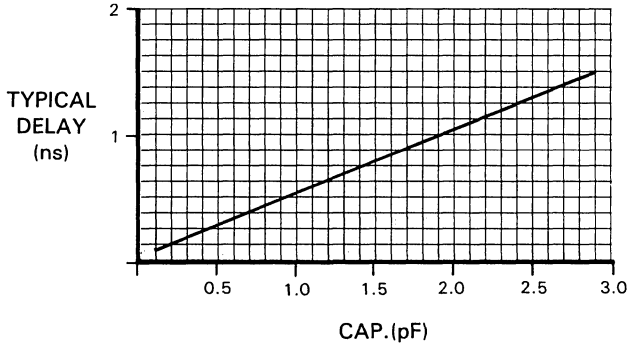
LOGIC SYMBOL



INPUT CAP. 2.5pF

For use with INBUF, DS1238, DS1218 or DS2232.

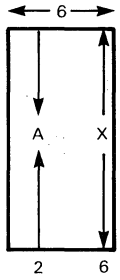
INPUT: PAD
OUTPUT: IN



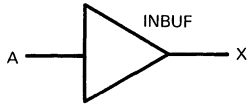
INPUT BUFFER

INBUF

CELL GEOMETRY



LOGIC SYMBOL



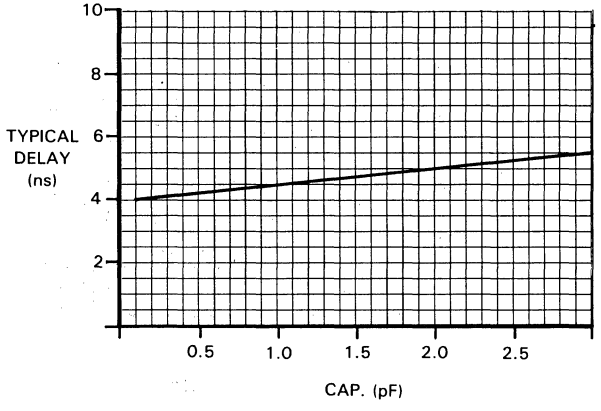
INPUT CAP. 0.38pF

INBUF is used with INPD.

INPUT: A
OUTPUT: X

	LIMITS
V_{IL} = 0.8V max I_{IL} = + 10μA	V_{IL} = V_{SS} −0.3V min
V_{IH} = 2.0V min I_{IH} = ±10μA	V_{IH} = V_{CC} +0.3V max

PROPAGATION CHART*

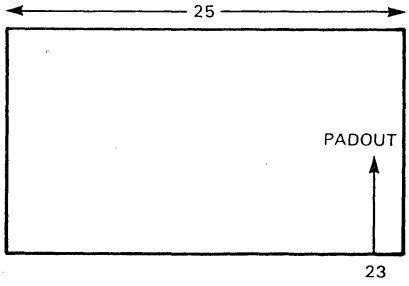


*This Delay includes INPD delay.

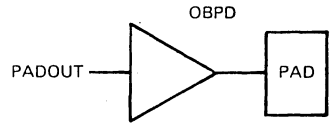
OUTPUT PAD WITH BUFFER

OBPD

CELL GEOMETRY



LOGIC SYMBOL

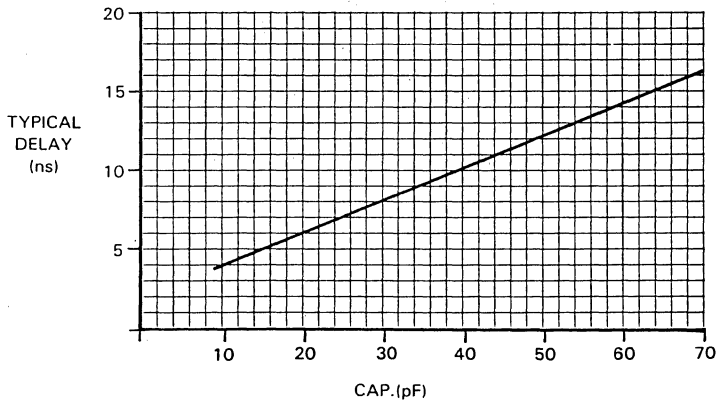


INPUT CAP. 0.36pF

For use in designs that are **NOT** pad-limited.

INPUT: PADOUT
OUTPUT: PAD

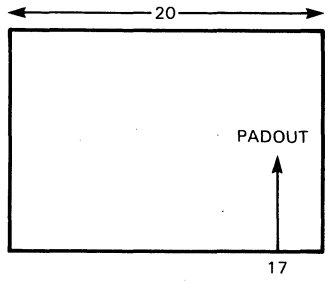
PROPAGATION CHART



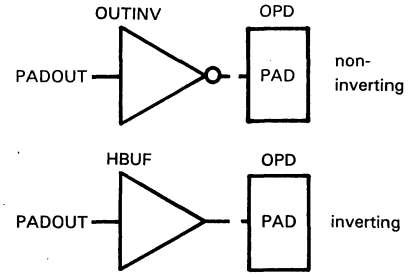
OUTPUT PAD

OPD

CELL GEOMETRY



LOGIC SYMBOL



INPUT CAP. 1.91 pF

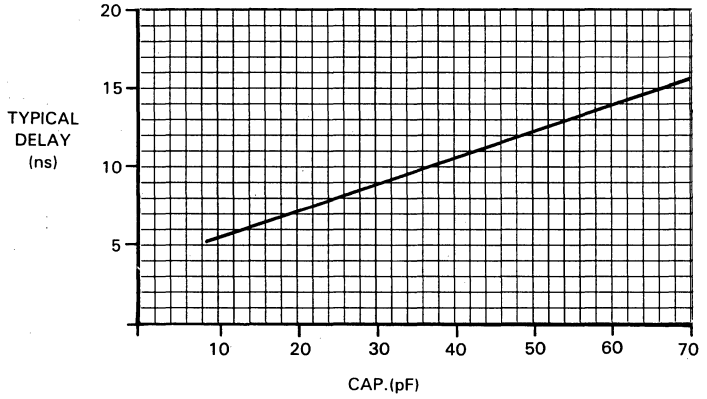
This is an inverting pad and requires either HBUF, OUTINV or TBUF for PADOUT input.

INPUT: PADOUT
OUTPUT: PAD

V_{OL} = 0.4V max
V_{OH} = 4.0V min

I_{OL} = 4.0 mA
I_{OH} = 2.0 mA

PROPAGATION CHART *

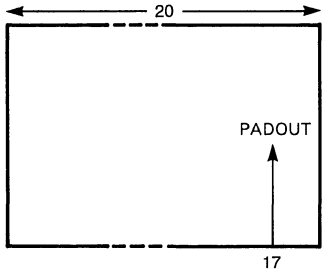


*This delay includes OUTINV Delay.

HIGH DRIVE OUTPUT PAD

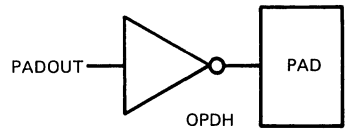
OPDH

CELL GEOMETRY



INPUT CAP. 3.6pF

LOGIC SYMBOL



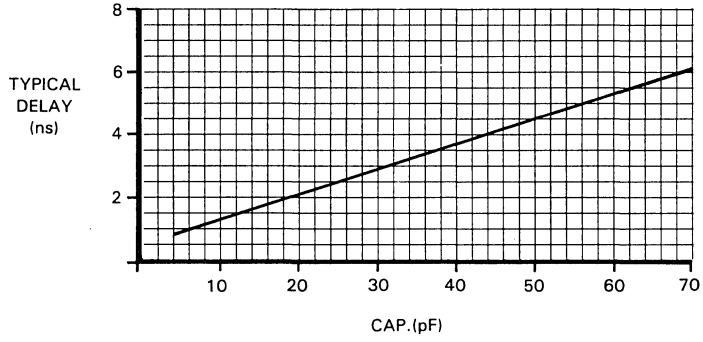
This is an inverting pad and requires either HBUF or OUTINV for PADOUT input.

INPUT: PADOUT
OUTPUT: PAD

V_{OL} = 0.4V max
V_{OH} = 4.0V min

I_{OL} = 8.0 mA
I_{OH} = 2.0 mA

PROPAGATION CHART

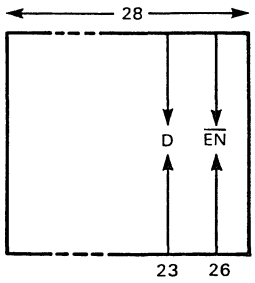


NCR

TRI-STATE OUTPUT PAD WITH BUFFER

TOBPD

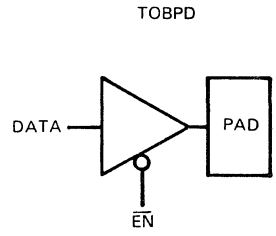
CELL GEOMETRY



INPUT CAP.

D	0.28pF
$\overline{EN}$	0.45pF

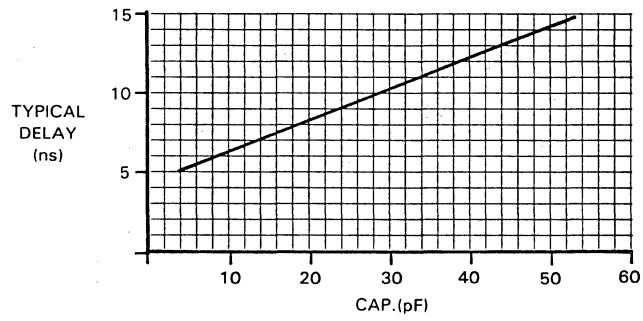
LOGIC SYMBOL



$\overline{EN}$ is active low. When $\overline{EN}$ is high, the output is hi-Z. Non-inverting output.

INPUTS: $\overline{EN}$, D
OUTPUT: PAD

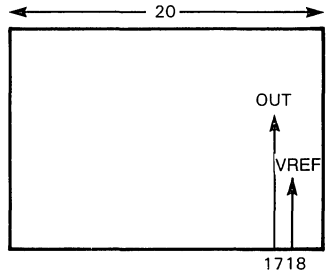
PROPAGATION CHART



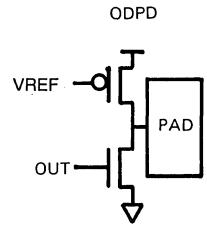
OPEN-DRAIN OUTPUT PAD

ODPD

CELL GEOMETRY



LOGIC SYMBOL



INPUT CAP. 1.2pF

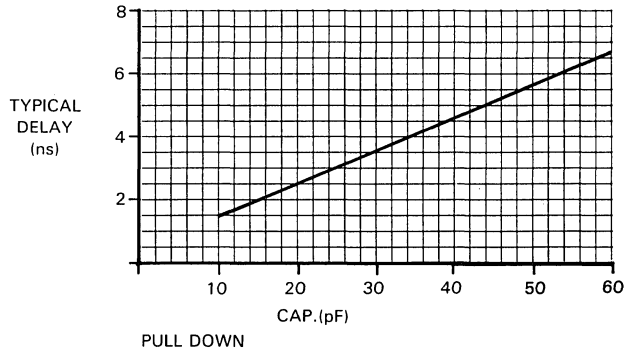
This is an inverting pad and requires either HBUF or OUTINV for OUT input. Also, if VCM is connected to VREF, then the internal pullup resistor is enabled. If VREF is connected to V_{DD} then the internal pullup is disabled.

INPUTS: V, OUT
OUTPUT: PAD

V_{OL} = 0.4V max
V_{OH} = 4.0V min

I_{OL} = 4.0 mA
I_{OH} = 400μA

PROPAGATION CHART



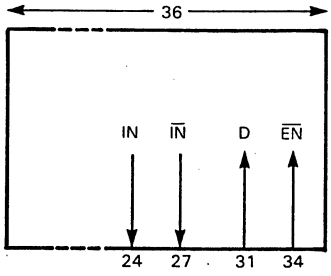
PULL DOWN

NCR

I/O PAD WITH BUFFER

IOBPD

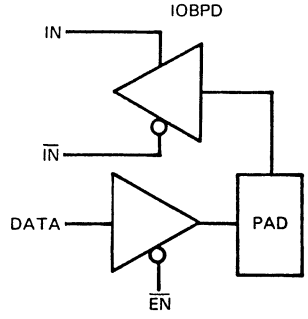
CELL GEOMETRY



INPUT CAP.

D	0.22pF
$\overline{EN}$	0.45pF
PAD	2.4pF

LOGIC SYMBOL

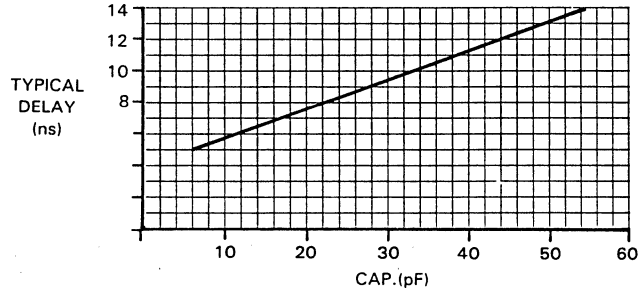


$\overline{EN}$ is low active. If $\overline{EN}$ is high, the output is hi-Z. For use in designs that are **NOT** pad-limited. IN and $\overline{IN}$ are **NOT** designed for minimum skew. D is non-inverting at pad output.

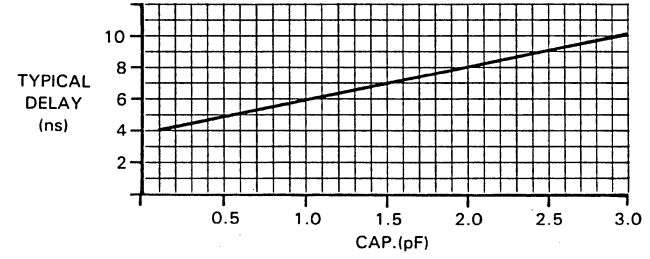
INPUTS: $\overline{EN}$, D, PAD
OUTPUTS: IN, $\overline{IN}$, PAD

PROPAGATION CHARTS

D, $\overline{EN}$ → OUTPUT



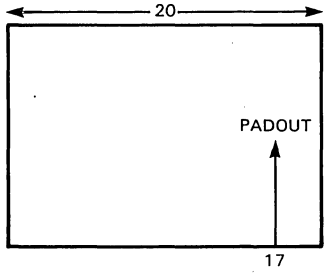
PAD → IN & $\overline{IN}$



OPEN-DRAIN OUTPUT PAD WITH NO PULL-UP

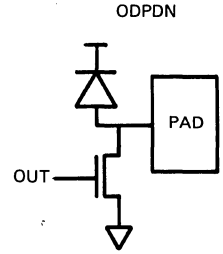
ODPDN

CELL GEOMETRY



INPUT CAP. 1.02pF

LOGIC SYMBOL

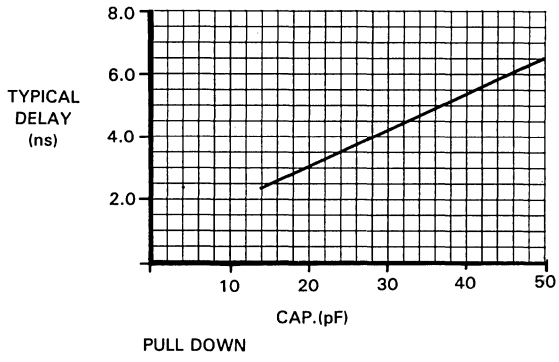


This is an inverting pad and requires either HBUF or OUTINV to drive PADOUT.

INPUT: PADOUT
OUTPUT: PAD

V_{OL} = 0.4V I_{OL} = 4.0 mA
$I_{Leakage}$ = ±10μA.

PROPAGATION CHART

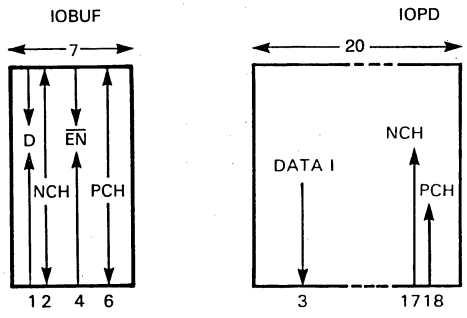


PULL DOWN

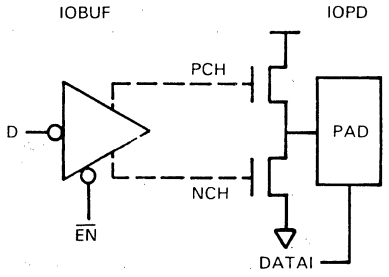
I/O PAD AND BUFFER

IOPD AND IOBUF

CELL GEOMETRY



LOGIC SYMBOL



INPUT CAP.

$\overline{EN}$, D	0.22pF
PAD	2.52pF

IOPD and IOBUF must be used together. This combination is non-inverting. DATA I must drive INBUF.

V_{OL} = 0.4V max
V_{OH} = 4.0V min

I_{OL} = 4.0 mA
I_{OH} = 2.0 mA

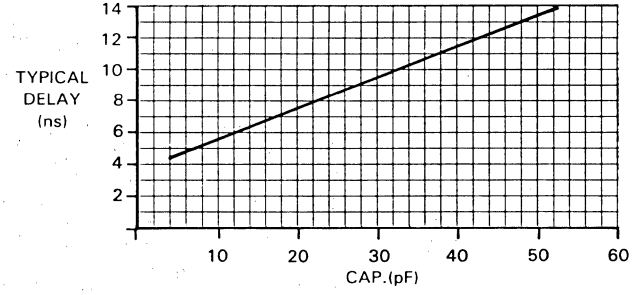
I_{IL} = ±10μA
I_{IH} = ±10μA

IOPD

INPUTS: NCH, PCH, PAD
OUTPUTS: DATAI, PAD

D, $\overline{EN}$ → OUTPUT

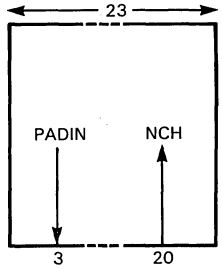
PROPAGATION CHARTS



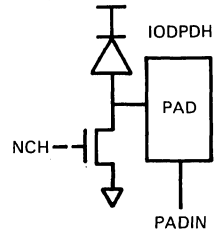
HIGH DRIVE OPEN-DRAIN I/O PAD

IODPDH

CELL GEOMETRY



LOGIC SYMBOL



INPUT CAP.

NCH	2.00pF
PAD	1.81pF

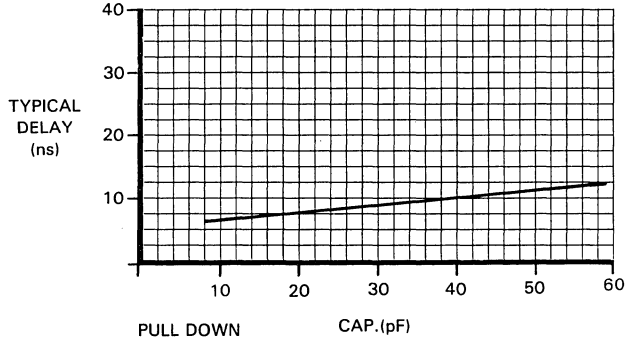
IODPDH and OUTINV must be used together. This combination is used for pad-limited designs and is non-inverting. It must be pulled high externally.

INPUTS: NCH, PAD
OUTPUTS: PADIN, PAD

V_{OL} = 0.4V I_{OL} = 8.0 mA
$I_{leakage}$ = ±10μA

PROPAGATION CHART

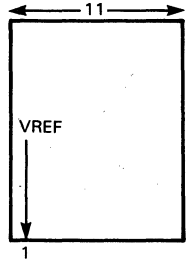
NCH → PAD



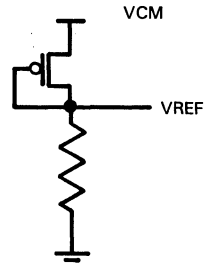
VOLTAGE REFERENCE

VCM

CELL GEOMETRY



LOGIC SYMBOL



VCM supplies 2.6V for ODPD.

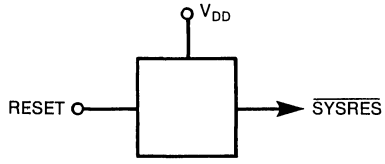
OUTPUT: VREF

V_{DD}	4.5V	5.0V	5.5V
VREF	2.22V	2.59V	2.96V

POWER ON RESET

POR

LOGIC SYMBOL



TRUTH TABLE

V_{DD}	RESET	$\overline{SYSRES}$
↑	0	⌐
X	1	0
1	↓	⌐

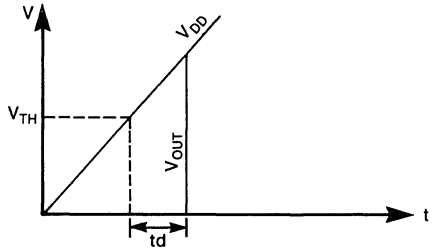
FEATURES

- Guaranteed logic operation while reset is valid
- No external components required
- Retriggerable reset under digital control
- Built in schmitt trigger prevents multiple reset pulses

POR is a digital cell which generates a pulse during power up for the purpose of resetting logic elements to known states. Upon application of the positive supply voltage to the device, POR generates a negative pulse which remains valid approximately 1μs after the positive supply has exceeded the sum of an n channel and a p channel FET threshold. This insures that all digital circuits are operational during the period when the output pulse is low. An additional input is supplied to the cell which allows the output to be retriggered under external control.

Electrical Specification

	Min	Nom	Max	Condition
Supply Current			1μA	$V_{DD}=5v$
Reset Trigger Voltage (V_{TH})[1]	$V_{TP}+V_{TN}+0.1v$	$V_{TP}+V_{TN}+0.3v$		
Minimum Output pulse Duration (td)[1]	200ns	1μs		
Output Pulse Rise Time		20ns		C1 = 0.5pF
Input Loading		0.2pF		



[1] POR Output wrt V_{DD} and time

NCR

32KHz OSCILLATOR

OSCPAD

FEATURES:

- Suitable for battery operation
- Voltage regulated for low drift over supply voltage
- Low power dissipation

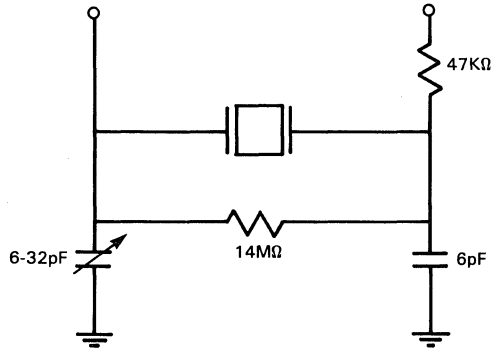
OSCPAD is a precision crystal oscillator cell suitable for use with crystals having a resonant frequency less than 75KHz. The cell contains a built-in voltage regulator to allow operation over a wide range of supply voltages with minimal frequency drift. Frequency tuning and start-up components must be supplied off-chip.

Electrical Specification

	Min	Nom	Max	Conditions
Frequency range		32KHz	75KHz	
Frequency stability over supply voltage		+3ppm/v	+5ppm/v	T = 25°C
Frequency stability over temperature*		+3, −12ppm +3, −78ppm	+5, −20ppm +5, −120ppm	T = 10°-40°C T = 0°-70°C
Operating voltage	2.5V		5.5V	f_o = 32KHz
Supply current		8μA	12μA	V_{DD} = 3.5V, T = 25°C f_o = 32768Hz
On chip drive			2pF	

*Measured using a crystal having frequency drift < −0.04ppm/°C²

RECOMMENDED CIRCUIT CONFIGURATION



GENERAL PURPOSE OSCILLATOR

OSCP

FEATURES

- 1 to 20 MHz operation
- On-chip tuning capacitors (5pF/pad)
- On-chip start up resistor (1MΩ)
- 40% to 60% output duty cycle
- Buffered on-chip output

OSCP is a general purpose crystal oscillator cell designed for use with 1MHz to 20MHz parallel resonant crystals. Tuning capacitors and a start up resistor are supplied internally to the cell, allowing oscillator operation without the requirement of additional off-chip components. The buffered on-chip output is suitable for driving 5pF loads at 20 MHz.

Electrical Specification

	Min	Nom	Max	Condition
Supply Voltage	4.5V		5.5V	$f_o = 20MHz$
Supply Current		500μA/MHz		$V_{DD} = 5V$
Tuning Capacitance		5pF/pad		
Start Up Resistance	250KΩ	1MΩ		
Operating Frequency	1MHz		20MHz	$V_{DD} = 4.5$ to 5.5V
Frequency Error		0.1%	0.3%	$T = 25°C$, $V_{DD} = 5V$
Output Duty Cycle	40%	50%	60%	
Load Output			5pF	$f_o = 20MHz$, $V_{DD} = 5V$

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Fort Collins, Colorado 80525
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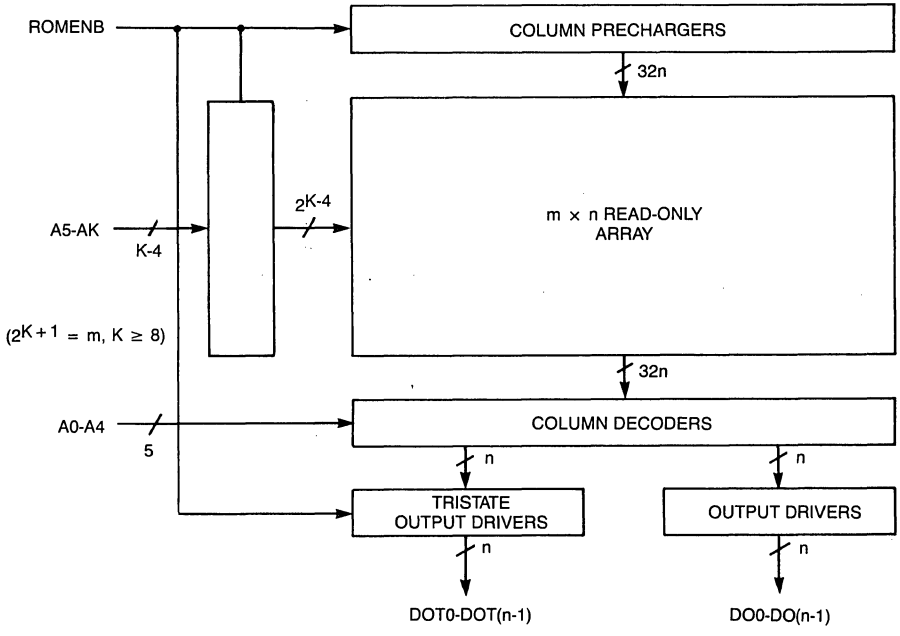
ROM SUPERCELL

- **Modular ROM allows flexible organization**
- **Clocked operation suited to Microcomputer Applications**
- **Access Time: Less than 200 ns**
- **Active Power Dissipation: 6 mW/MHz**
- **Standby Power Dissipation: 100μW**

The modular ROM supercell uses clocked operation to reduce complexity and operating power. The enable input (ROMENB) must be taken high between each access. The memory array is organized as "m" words, where each word has "n" bits. "m" can be any multiple of 512, while "n" can be any integer. Both tri-stateable and always-driving outputs are provided.

FUNCTIONAL BLOCK DIAGRAM
(m × n Array)



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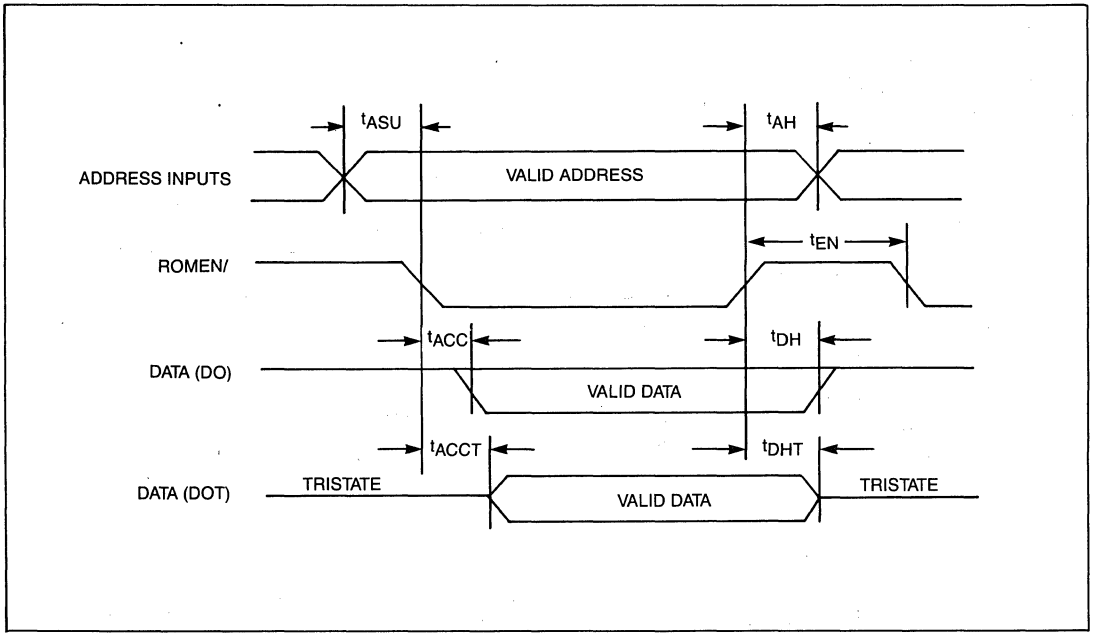
DYNAMIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{ASU}	Address Set-Up Time Before ROMENB	40	—	ns
t_{AH}	Address Hold Time After ROMENB	—	0	ns
t_{EN}	ROMENB High Pulse Width	150	—	ns
t_{ACC}	ROMENB to DO Outputs Valid	—	200	—
t_{DH}	DO Outputs Hold Time	40	120	ns
t_{ACCT}	ROMENB to DOT Outputs Valid	—	200	—
t_{DHT}	DO Outputs Hold Time	10	50	ns

DYNAMIC WAVEFORMS



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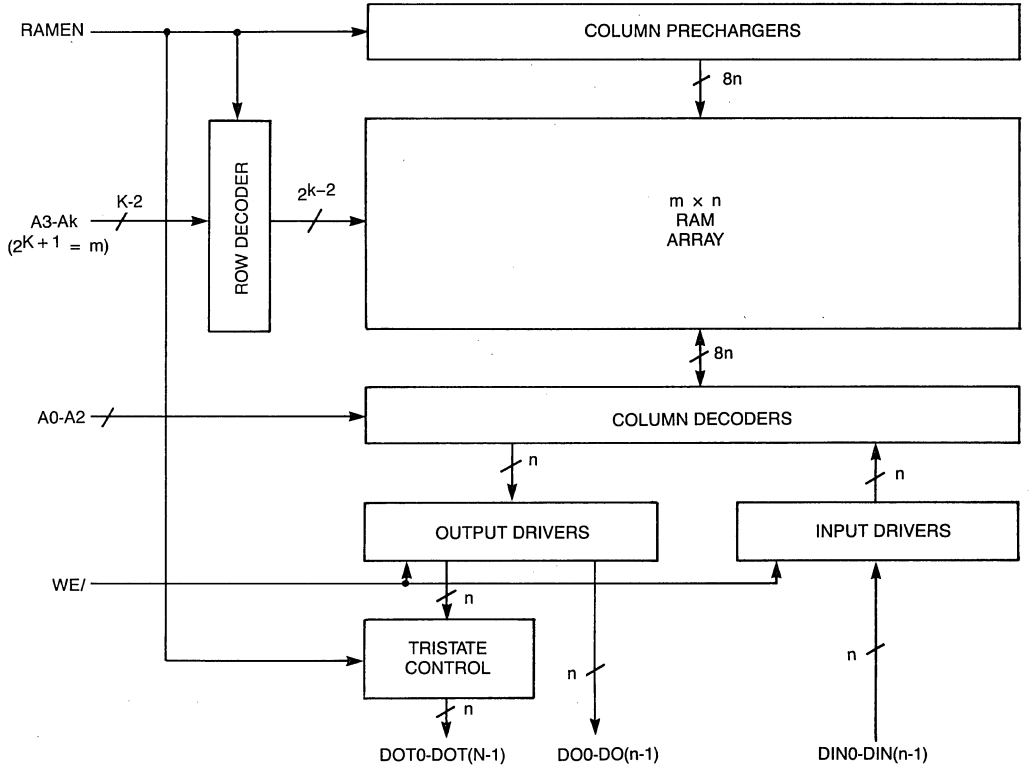
RAM SUPERCELL

- **Modular RAM allows flexible organization**
- **Clocked operation suited to Microcomputer Applications**
- **Access Time: Less than 200 ns**
- **Active Power Dissipation: 6 mW/MHz**
- **Standby Power Dissipation: 100μW**

The modular RAM supercell uses clocked operation to reduce complexity and operating power. The enable input (RAMEN) must be taken low between each read access. The memory array is organized as "m" words, where each word has "n" bits. "m" can be any multiple of 16, while "n" can be any integer. Both tri-stateable and always-driving outputs are provided. By externally tying a tri-stateable output (DOTn) to a data input (DINn), a bi-directional I/O line is possible. The DO outputs will output data being written in a write cycle.

FUNCTIONAL BLOCK DIAGRAM
(m × n Array)



NCR SEMICUSTOM DESIGN

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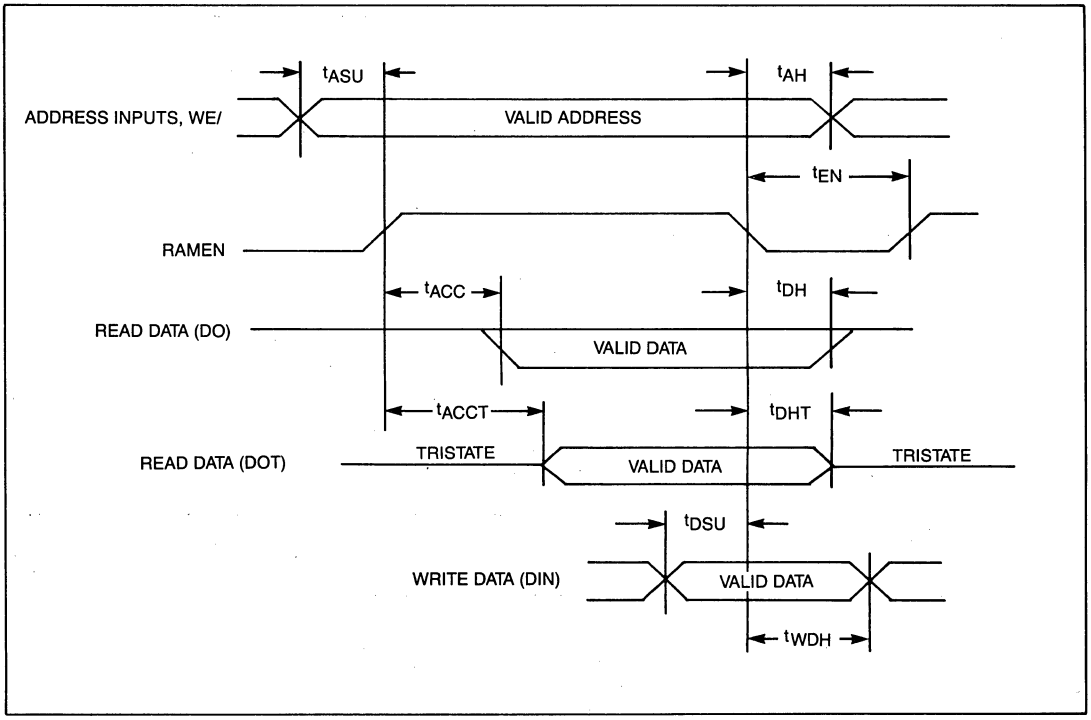
DYNAMIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{ASU}	Address Set-Up Time Before RAMEN (Read)	40	—	ns
t_{AH}	Address Hold Time After RAMEN	—	—	ns
t_{EN}	RAMEN Low Pulse Width	150	—	ns
t_{ACC}	RAMEN to DO Outputs Valid (Read)		200	
t_{DH}	DO Outputs Hold Time (Read, Write)	40	120	ns
t_{ACCT}	RAMEN to DOT Outputs Valid (Read)		200	
t_{DHT}	DOT Outputs Hold Time	10	50	ns
t_{DSU}	Write Data Set-Up Time Before RAMEN		50	
t_{WDH}	Write Data Hold Time After RAMEN	10	—	ns

DYNAMIC WAVEFORMS



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TIMER I SUPERCELL

- **16-Bit Counter**
- **One-Shot or Continuous Operation**
- **Timing Compatible with 65CX02 Supercell**
- **Single Pulse and Toggle Outputs Available**

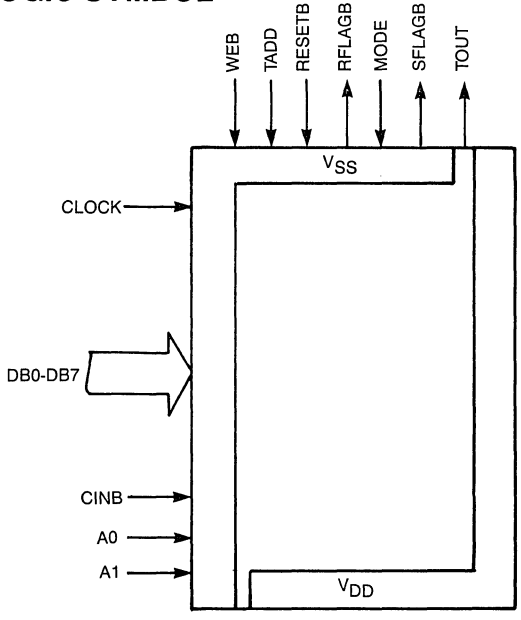
The Timer 1 supercell consists of two 8-bit latches and a 16-bit counter. The latches store data which is to be loaded into the counter. Once the counter is loaded it decrements at the input clock rate. Once the counter reaches 0, it generates a negative pulse on SFLAGB for setting an interrupt flag. The counter is automatically reloaded from the latches and continues to decrement. Further interrupts may or may not be generated depending on whether the timer is set for one-shot or continuous mode operation.

In one-shot mode operation, an interrupt is generated after the counter decrements the first time. Subsequent interrupts are blocked until the high counter is written.

In continuous mode, the counter is reloaded and an interrupt is generated each time the counter decrements to 0.

Another timer output is provided that is initially low and toggles each time the counter decrements to 0 in the continuous mode.

LOGIC SYMBOL



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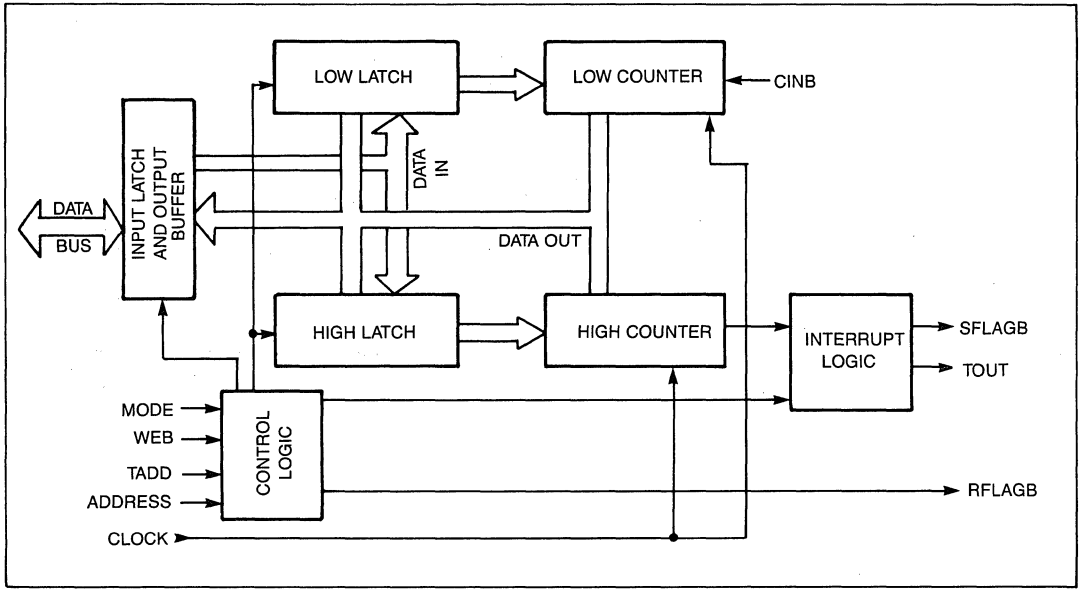
BLOCK DIAGRAM



PORT FUNCTIONS:

Port	Function
A0, A1	Address Inputs
CLOCK	Clock Input
DB0-DB7	Bidirectional Databus
WEB	Write Enable Input
TADD	Timer Address Enable Input
RESETB	Reset Input
SFLAGB	Set Interrupt Flag Output
RFLAGB	Reset Interrupt Flag Output
MODE	One Shot/Continuous Mode Select Input
TOUT	Timer Output
CINB	Count Enable Input

INPUT PORT CAPACITANCES	
A1, A2	0.12 pF
CLOCK	0.20 pF
DB0-DB7	0.46 pF
WEB	0.47 pF
TADD	0.58 pF
RESETB	0.29 pF
MODE	0.11 pF
CINB	0.30 pF

SIGNAL DESCRIPTION

A0, A1: Together with the Write Enable signal, the two address bits control the selection of the high -and low-byte latches and counters for reading and writing operations. See Table 1 for address decoding.

WEB: This selects either a read operation (WEB = 1) or a write operation (WEB = 0).

TABLE 1

TIMER 1 LOW-ORDER LATCHES	TIMER 1 HIGH-ORDER LATCHES
WRITE — 8-bits loaded into T1 low-order latches. READ — 8-bits from T1 low-order latches transferred to MPU. **TIMER 1 LOW-ORDER COUNTER** WRITE — 8-bits loaded into T1 low-order latches. Latch contents are transferred into low-order counter at the time the high-order counter is loaded. READ — 8-bits from T1 low-order counter transferred to MPU. RFLAGB goes low.	WRITE — 8-bits loaded into T1 high-order latches. RFLAGB goes low. READ — 8-bits from T1 high-order latches transferred to MPU. **TIMER 1 HIGH-ORDER COUNTER** WRITE — 8-bits loaded into T1 high-order latches. Also, at this time both high-and low-order latches transferred into T1 counter, and initiates countdown. RFLAGB goes low. READ — 8-bits from T1 high-order counter transferred to MPU.

WEB	A1	A0	DESCRIPTION
1	0	0	Read Low Counter
1	0	1	Read High Counter
1	1	0	Read Low Latch
1	1	1	Read High Latch
0	X	0	Write To Low Latch
0	0	1	Write To High Latch and Load Both Latches To Counters
0	1	1	Write To High Latch

SIGNAL DESCRIPTION

TADD: This functions as a "cell select". When TADD is low, the timer super-cell is deselected. The outputs are tristated and the two 8-bit latches cannot be written. TADD is high for normal operation.

RESETB: This input resets all the flip-flops in the timer. The counters are not reset. In particular, it blocks any interrupts the timer may generate, providing no attempt is made to load the counters. SFLAGB is set high and TOUT is set low. Writing to the counters enables the interrupt outputs, SFLAGB, and TOUT.

TOUT: Resetting the timer sets TOUT high. Whenever the counter reaches 0, the latches automatically load the counter and the state of TOUT is inverted if the timer is operating in the continuous mode. If the timer is operating in the one-shot mode, TOUT inverts only after the first interrupt is generated. If the high byte counter is written, TOUT is reset low.

MODE: This input selects one-shot or continuous mode for the timer and interrupts outputs. In the continuous mode, an interrupt is generated from SFLAGB each time the counter reaches 0 and the timer output TOUT changes state.

In the one-shot mode, TOUT and SLFAGB change state only the first time the counter reaches 0. No further interruptions are generated until the high byte counter is written. MODE is low for one-shot operation.

RLFAGB: This output generates a low signal one-half clock cycle long for resetting an interrupt flag bit. This signal is generated whenever the low byte counter is read *or* the high byte latch is written *or* the high byte counter is written.

CLOCK: Clock cycles begin on the falling edge.

DB0-DB7: These ports comprise an 8-bit bidirectional databus. The buffers driving this bus are tristated except when reading latch or counter contents.

CINB: This is the counter enable input. The LSB toggles on clock low whenever CINB is low.

SFLAGB: Resetting the timer sets this output high, and blocks any further state changes until the high byte counter is written. When the counter subsequently reaches 0, this output goes low for one clock cycle.

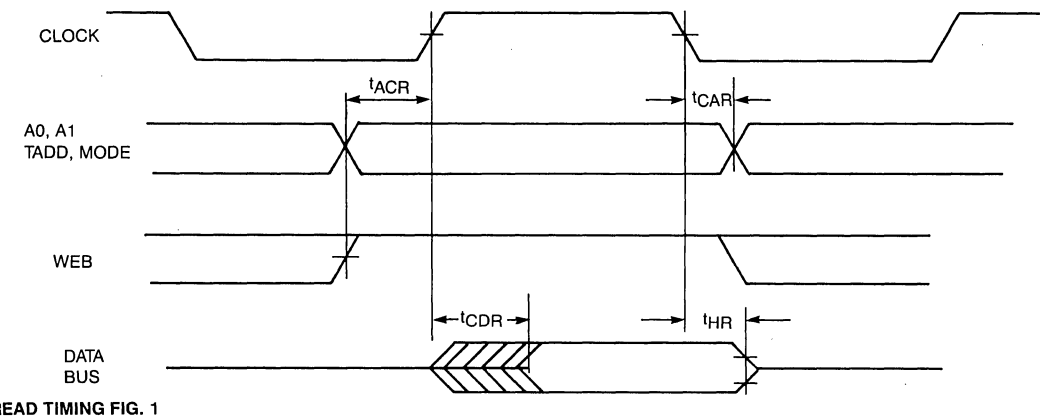
AC CHARACTERISTICS

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
READ TIMER SELECT, ADDRESS, WEB SETUP	t_{ACR}	45	—	ns
READ TIMER SELECT, ADDRESS, WEB HOLD	t_{CAR}	0	—	ns
READ DATA DELAY*	t_{CDR}	—	30	ns
READ DATA HOLD	t_{HR}	10	—	ns
WRITE TIMER SELECT, ADDRESS, WEB SETUP	t_{ACW}	45	—	ns
WRITE TIMER SELECT, ADDRESS, WEB HOLD	t_{CAW}	0	—	ns
WRITE DATA SETUP*	t_{DCW}	45	—	ns
WRITE DATA HOLD	t_{HW}	10	—	ns
TIMER OUTPUT DELAY**	t_{OD}	—	35	ns
COUNTER INPUT SETUP	t_{CIS}	80	—	ns
COUNTER INPUT HOLD	t_{CIH}	5	—	ns
RESET INTERRUPT FLAG DELAY		—	25	ns
(WRITE DELAY)	t_{RWD}	—	25	ns
(READ DELAY)	t_{RRD}	—	25	ns

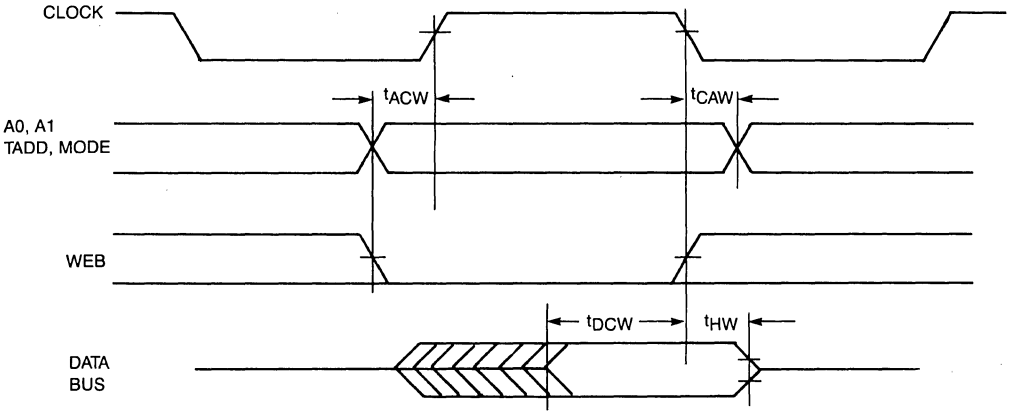
*5pF assumed for databus capacitance.

**2pF assumed for load capacitance at port.

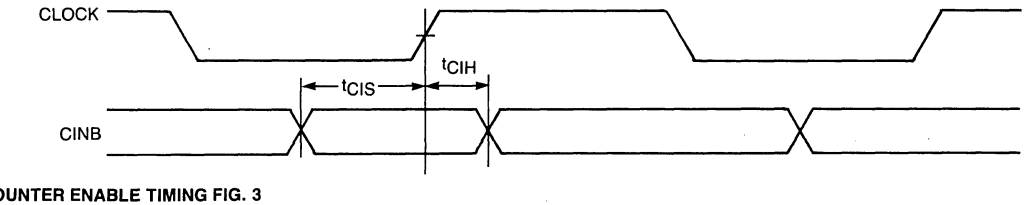
TIMING DIAGRAMS



READ TIMING FIG. 1

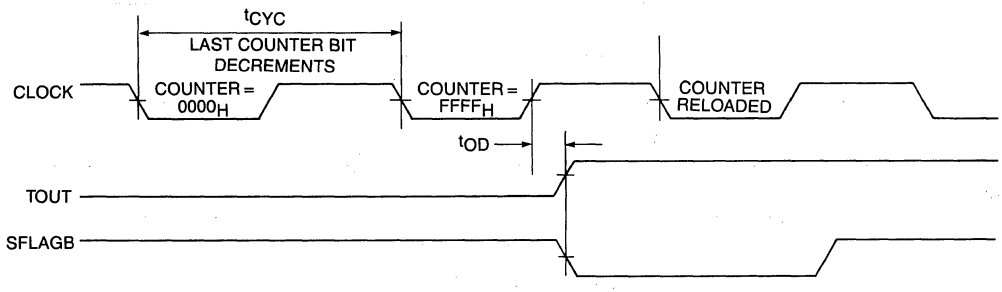


WRITE TIMING FIG. 2

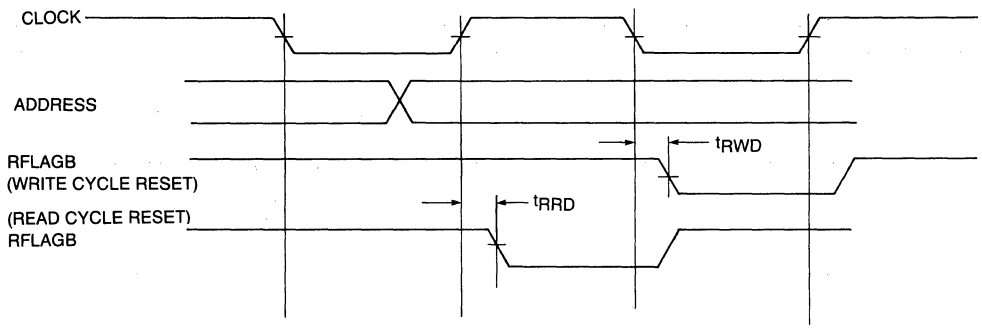


COUNTER ENABLE TIMING FIG. 3

TIMING DIAGRAMS



INTERRUPT OUTPUT TIMING FIG. 4



RESET FLAG OUTPUT TIMING FIG. 5

NCR Microelectronics
2001 Danfield Ct.
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Phone: 303/226-9500, 303/223-5100

65CX02
CMOS II
STANDARD CELL LIBRARY
65CX02 SUPERCELL

- Enhanced software performance including 59 additional OP codes encompassing fourteen new instructions and two additional addressing modes.
- 70 microprocessor instructions.
- 15 addressing modes.
- 210 operational codes.
- Up to 3MHz operation.
- Operates at frequencies as low as 200 Hz for even lower power consumption (pseudostatic: stop during F2M high).
- Compatible with NMOS 6500 series microprocessors.
- 64 K-byte addressable memory.
- Interrupt capability.
- Lower power consumption. 4mA @ 1MHz.
- 8-bit bidirectional data bus.
- Bus Compatible with M6800.
- Non-maskable interrupt.
- 8-bit parallel processing.
- Decimal and binary arithmetic.
- Pipeline architecture.
- Programmable stack pointer.
- Variable length stack.

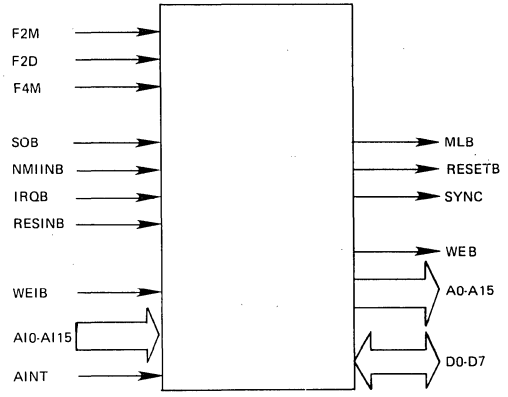
NCR SEMICUSTOM DESIGN

The 65CX02 supercell is an 8-bit microprocessor which is software compatible with the NMOS 6502. Enhancements include fourteen additional instructions (four more than the NCR65C02 microprocessor), expanded operational codes and two new addressing modes. Bit manipulation instructions have been added to facilitate software control of memory-mapped I/O and control registers.

PORT FUNCTIONS

PORT	FUNCTION
A0-A15	Address Bus Outputs
AI0-AI15	Address Bus from External Source (for DMA)
AINT	Internal Address Selector
D0-D7	Bidirectional Data Bus
F2D	Phase 2 Clock for Interrupts
F2M	Phase 2 Clock
F4M	Phase 4 Clock
IRQB	Interrupt Request (Maskable)
MLB	Memory Lock
NMIINB	Non-Maskable Interrupt
RESETB	Reset Output
RESINB	Reset Input
SOB	Set Overflow
SYNC	Synchronize
WEB	Write Enable Output
WEIB	Write Enable from External Source (for DMA)

LOGIC SYMBOL



* Specifications are subject to change without notice.

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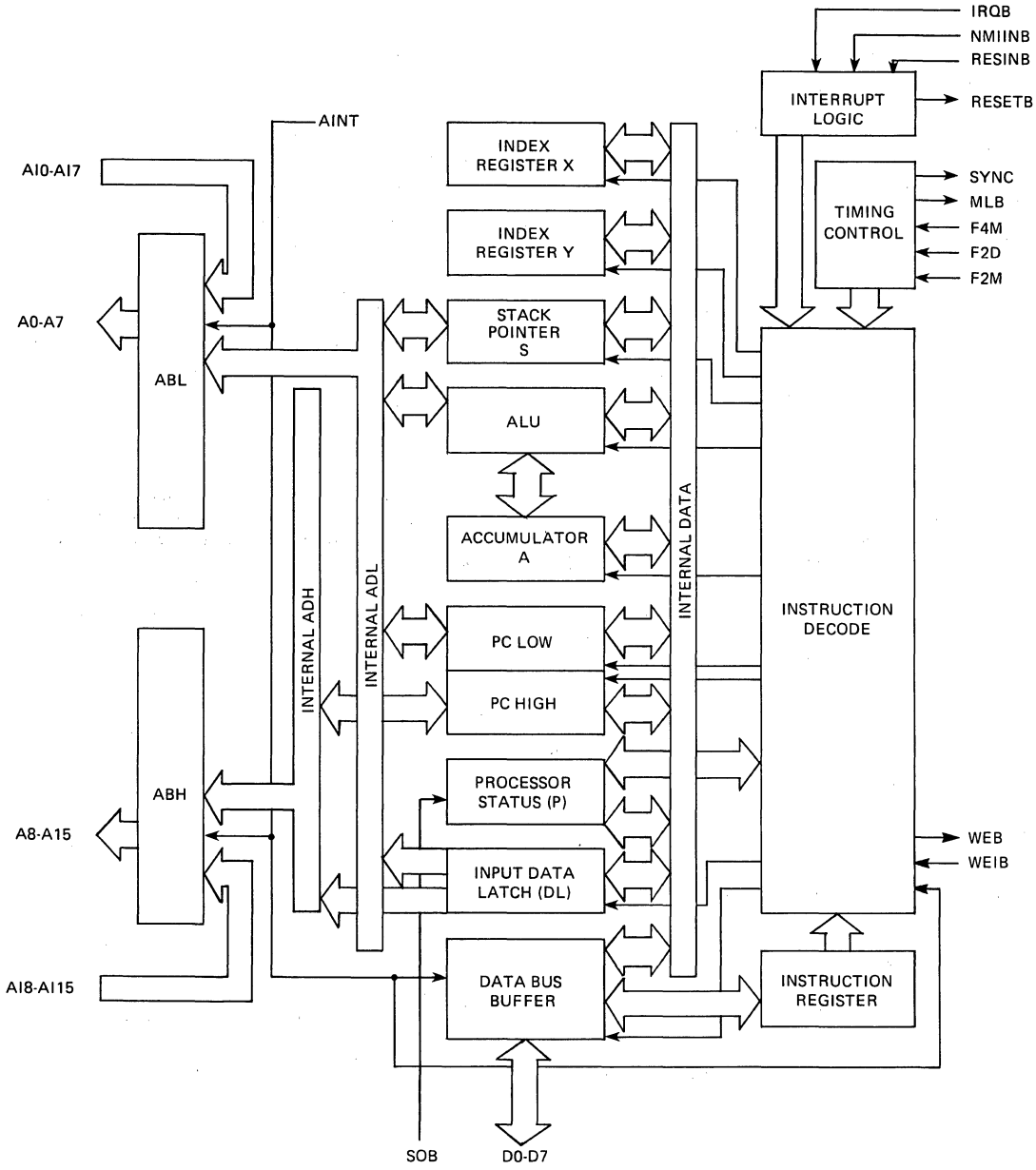
■ NCR65CX02 SUPERCELL BLOCK DIAGRAM



■ MICROPROCESSOR OPERATIONAL ENHANCEMENTS

Function	NMOS 6502 Microprocessor	NCR65CX02 Supercell
Indexed addressing across page boundary.	Extra read of invalid address.	Extra read of last instruction byte.
Execution of invalid op codes.	Some terminate only by reset. Results are undefined.	All are NOPs (reserved for future use). Op Code / Bytes / Cycles X2 / 2 / 2 X3, XB / 1 / 1 44 / 2 / 3 54,D4,F4 / 2 / 4 5C / 3 / 8 DC, FC / 3 / 4
Jump indirect, operand=XXFF.	Page address does not increment.	Page address increments and adds one additional cycle.
Read/modify/write instructions at effective addresses.	One read and two write cycles.	Two read and one write cycle.
Decimal flag.	Indeterminate after reset.	Initialized to binary mode (D = O) after reset and interrupts.
Flags after decimal operation.	Invalid N, V and Z flags.	Valid flag adds one additional cycle.
Interrupt after fetch of BRK instruction.	Interrupt vector is loaded, BRK vector is ignored.	BRK is executed, then interrupt is executed.

■ NEW INSTRUCTION MNEMONICS

HEX	MNEMONIC	DESCRIPTION
0F-7F	BBRn	Branch on bit "n" reset [Zero page]
8F-FF	BBSn	Branch on bit "n" set [Zero page]
80	BRA	Branch relative always [Relative]
3A	DEA	Decrement accumulator [Accum]
1A	INA	Increment accumulator [Accum]
DA	PHX	Push X on stack [Implied]
5A	PHY	Push Y on stack [Implied]
FA	PLX	Pull X from stack [Implied]
7A	PLY	Pull Y from stack [Implied]
07-77	RMBn	Reset memory bit "n" [Zero page]
87-F7	SMBn	Set memory bit "n" [Zero page]
9C	STZ	Store zero [Absolute]
9E	STZ	Store zero [ABS, X]
64	STZ	Store zero [Zero page]
74	STZ	Store zero [ZPG, X]
1C	TRB	Test and reset memory bits with accumulator [Absolute]
14	TRB	Test and reset memory bits with accumulator [Zero page]
0C	TSB	Test and set memory bits with accumulator [Absolute]
04	TSB	Test and set memory bits with accumulator [Zero page]

■ INPUT PORT CAPACITANCES

Port	Input Capacitance (pF)	Port	Input Capacitance (pF)
AI0	.48	AI13	.47
AI1	.46	AI14	.42
AI2	.43	AI15	.40
AI3	.41	AINT	3.10
AI4	.38	D0-D7	1.06
AI5	.36	F2D	.46
AI6	.34	F2M	3.24
AI7	.33	F4M	1.74
AI8	.63	IRQB	.11
AI9	.61	NMIINB	.15
AI10	.57	RESINB	.15
AI11	.54	SOB	.11
AI12	.50	WEIB	.18

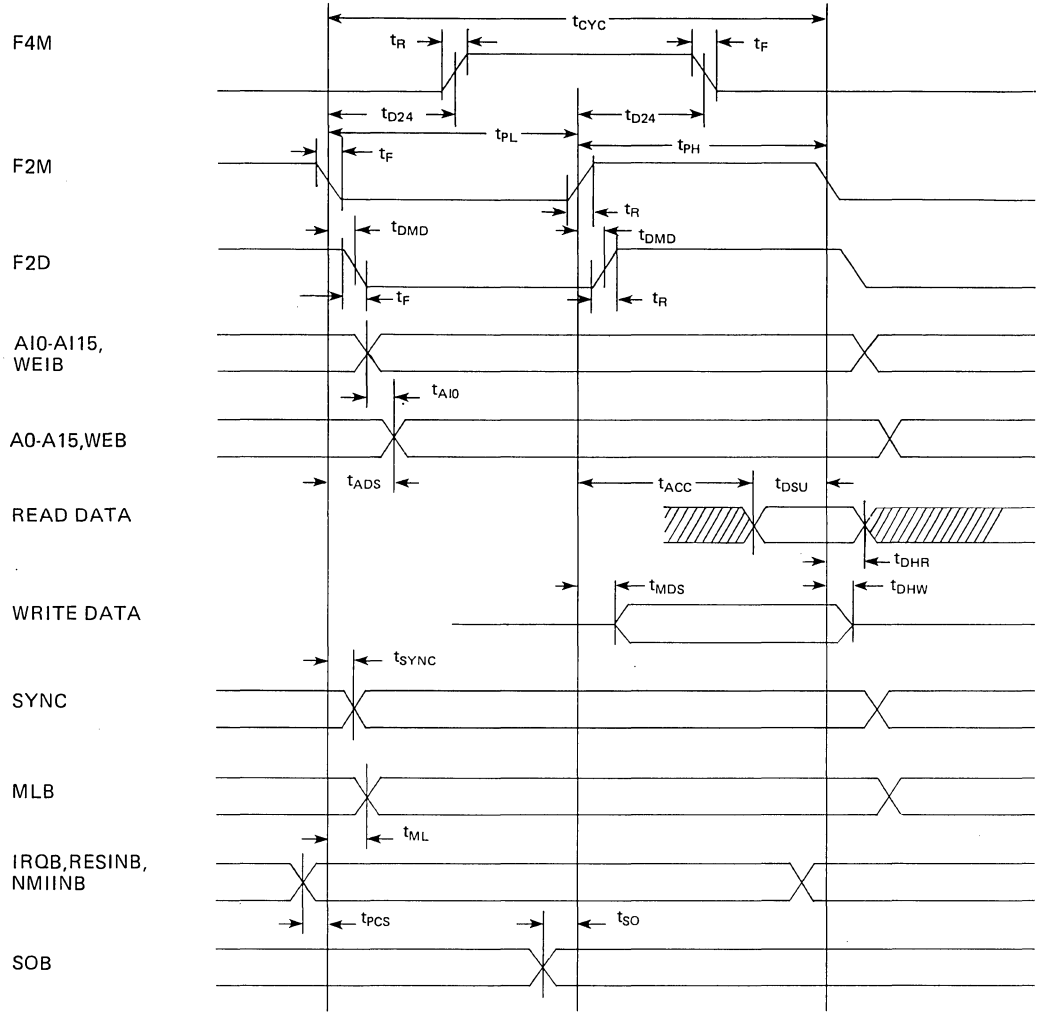
■ AC CHARACTERISTICS

V_{DD} = 5V ± 10%, T_A = 0°C to 70°C, Load = 5pF

Parameter	Symbol	Min.	Max.	Units
Cycle Time*	t_{CYC}	0.333	5000	uS
Clock Pulse Width Low	t_{PL}	160		nS
Clock Pulse Width High	t_{PH}	160		nS
Fall Time, Rise Time	t_F, t_R		20	nS
Phase 2 to Phase 4 Delay	t_{D24}	$\frac{1}{2}t_{pl} - 10$	$\frac{1}{2}t_{pl} + 10$	nS
F2M to F2D Delay	t_{DMD}	− 20	20	nS
Address Input to Output (AINT low)	t_{AIO}	20	40	nS
Address Setup Time (AINT high)	t_{ADS}	10	60	nS
Read Access Time	t_{ACC}	130		nS
Read Data Setup Time	t_{DSU}	30		nS
Read Data Hold Time	t_{DHR}	10		nS
Write Data Delay Time	t_{MDS}		30	nS
Write Data Hold Time	t_{DHW}	10		nS
SYNC Delay Time	t_{SYNC}		50	nS
Memory Lock Delay Time	t_{ML}		50	nS
Processor Control Setup Time**	t_{PCS}	40		nS
SO Setup Time	t_{SO}	50		nS

*The processor can be stopped with F2M and F4M held low.
**This parameter must only be met to guarantee that the signal will be recognized at the current clock cycle.

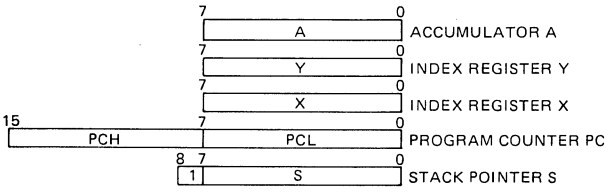
■ TIMING DIAGRAM

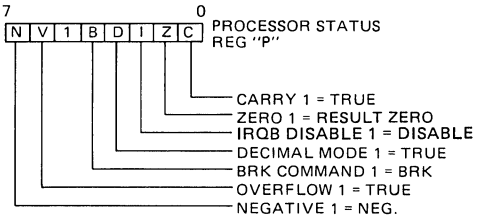


■ ADDITIONAL INSTRUCTION ADDRESSING MODES

HEX	MNEMONIC	DESCRIPTION
72	ADC	Add memory to accumulator with carry [(ZPG)]
32	AND	"AND" memory with accumulator[(ZPG)]
3C	BIT	Test memory bits with accumulator [ABS, X]
34	BIT	Test memory bits with accumulator [ZPG, X]
D2	CMP	Compare memory and accumulator [(ZPG)]
52	EOR	"Exclusive Or" memory with accumulator [(ZPG)]
7C	JMP	Jump (New addressing mode) [ABS(IND, X)]
B2	LDA	Load accumulator with memory [(ZPG)]
12	ORA	"OR" memory with accumulator [(ZPG)]
F2	SBC	Subtract memory from accumulator with borrow [(ZPG)]
92	STA	Store accumulator in memory [(ZPG)]

■ MICROPROCESSOR PROGRAMMING MODEL





■ FUNCTIONAL DESCRIPTION

Timing Control
The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase two clock pulse for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

Program Counter
The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order 8-bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

Instruction Register and Decode
Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register, then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

Arithmetic and Logic Unit (ALU)
All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

Accumulator
The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations, and in addition, the accumulator usually contains one of the two data words used in these operations.

Index Registers
There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address.

When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible (see addressing modes).

Stack Pointer
The stack pointer is an 8-bit register used to control the addressing of the variable-length stack on page one. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts (NMIINB and IRQB). The stack allows simple implementation of nested sub-routines and multiple level interrupts. The stack pointer should be initialized before any interrupts or stack operations occur.

Processor Status Register
The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU. The 6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags (see microprocessor programming model).

■ ADDRESSING MODES

Fifteen addressing modes are available to the user of the NCR65CX02 microprocessor. The addressing modes are described in the following paragraphs:

Implied Addressing [Implied]
In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

Accumulator Addressing [Accum]
This form of addressing is represented with a one byte instruction and implies an operation on the accumulator.

Immediate Addressing [Immediate]
With immediate addressing, the operand is contained in the second byte of the instruction; no further memory addressing is required.

Absolute Addressing [Absolute]
For absolute addressing, the second byte of the instruction specifies the eight low-order bits of the effective address, while the third byte specifies the eight high-order bits. Therefore, this addressing mode allows access to the total 64K bytes of addressable memory.

Zero Page Addressing [Zero Page]
Zero page addressing allows shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. The careful use of zero page addressing can result in significant increase in code efficiency.

Absolute Indexed Addressing [ABS, X or ABS, Y]
Absolute indexed addressing is used in conjunction with X or Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields, resulting in reduced coding and execution time.

Zero Page Indexed Addressing [ZPG, X or ZPG, Y]
Zero page absolute addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high-order eight bits of memory, and crossing of page boundaries does not occur.

Relative Addressing [Relative]
Relative addressing is used only with branch instructions; it establishes a destination for the conditional branch. The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the program counter when the counter is set at the next instruction. The range of the offset is −128 to +127 bytes from the next instruction.

Zero Page Indexed Indirect Addressing [(IND, X)]
With zero page indexed indirect addressing (usually referred to as indirect X) the second byte of the instruction is added to the contents of the X index register; the carry is discarded. The result of this addition points to a memory location on page zero whose contents is the low-order eight bits of the effective address. The next memory location in page zero contains the high-order eight bits of the effective address. Both memory locations specifying the high- and low-order bytes of the effective address must be in page zero.

***Absolute Indexed Indirect Addressing [ABS(IND, X)]**
(Jump Instruction Only)
With absolute indexed indirect addressing the contents of the second and third instruction bytes are added to the X register. The result of this addition, points to a memory location containing the lower-order eight bits of the effective address. The next memory location contains the higher-order eight bits of the effective address.

Indirect Indexed Addressing [(IND), Y]
This form of addressing is usually referred to as Indirect, Y. The second byte of the instruction points to a memory location in page zero. The contents of this memory location are added to the contents of the Y index register, the result being the low-order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high-order eight bits of the effective address.

***Zero Page Indirect Addressing [(ZPG)]**
In the zero page indirect addressing mode, the second byte of the instruction points to a memory location on page zero containing the low-order byte of the effective address. The next location on page zero contains the high-order byte of the effective address.

Absolute Indirect Addressing [(ABS)]
(Jump Instruction Only)
The second byte of the instruction contains the low-order eight bits of a memory location. The high-order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low-order byte of the effective address. The next memory location contains the high-order byte of the effective address which is loaded into the 16 bit program counter.

NOTE: * = New Address Modes

■ SIGNAL DESCRIPTION

Address Bus Outputs (A0-A15)
A0-A15 form a 16-bit address bus for memory and I/O exchanges on the data bus. These outputs will reflect the state of the CPU's internal address if AINT is input high, otherwise the external address (AI0-AI15) is output. The address bus outputs are buffered sufficiently to drive large on-chip busses.

External Address Bus Inputs (AI0-AI15)
An external controller can take over control of the address bus by pulling AINT low asynchronously. Immediately, the address bus outputs (A0-A15) and WEB will reflect the inputs at AI0-AI15 and WEIB.

Address Bus Selector (AINT)
Selects whether the CPU's internal address and write enable, or the external address bus and WEIB will appear at the A0-A15 outputs and WEB. This input is immediate: the outputs will update t_{AIO} after AINT changes.

Data Bus (D0-D7)
The data lines (D0-D7) constitute an 8-bit bidirectional data bus used for data exchanges to and from the CPU supercell and other elements of a microcomputer system (on-chip or off-chip). The outputs are buffered sufficiently to drive large on-chip busses.

Interrupt Clock (F2D)
In normal operation, F2D is exactly in phase with the main CPU clock, F2M. F2D is used to latch in the signals RESINB, NMIINB, and IRQB. Separating F2D and F2M allows a low power "sleep mode," where the main CPU can be shut down by stopping F2M and F4M low. A reset or interrupt can then "wake up" the CPU if F2D is still running. The power dissipation necessary to keep F2D running is considerably less than for F2M.

Phase 2 Clock (F2M)
This is the main time base for the CPU. Each cycle begins on a falling edge of F2M. Data bus transfers occur when F2M is high (see Timing Diagram). When the CPU is put in sleep mode or when DMA operations are invoked by pulling AINT low, F2M must stop after a falling edge, so that all data on the data bus will have been latched into its proper destination. If in DMA mode, the data bus will then be available to the external bus master.

Phase 4 Clock (F4M)
F4M is used for additional internal timing in the CPU, and should lead F2M by a quarter cycle (see timing Diagram). In sleep mode or DMA modes, F4M should be stopped low.

Interrupt Request (IRQB)
This input requests that an interrupt sequence begin within the microprocessor. The IRQB is sampled during F2 operation; if the interrupt flag in the processor status register is zero, the current instruction is completed and the interrupt sequence begins during the next cycle. The program counter and processor status register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further IRQBs may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, transferring program control to the memory vector located at these addresses.

Memory Lock (MLB)
In a multiprocessor system, the MLB output indicates the need to defer the rearbitration of the next bus cycle to ensure the integrity of read-modify-write instructions. MLB goes low during ASL, BBRn, BBSn, DEC, INC, LSR, RMBn, ROL, ROR, SMBn, TRB, TSB memory referencing instructions. This signal is low for the modify and write cycles.

Non-Maskable Interrupt (NMIINB)
A negative-going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. The NMIINB is sampled during F2; the current instruction is completed and the interrupt sequence begins during the next cycle. The program counter is loaded with the interrupt vector from locations FFFA (low byte) and FFFB (high byte), thereby transferring program control to the non-maskable interrupt routine.

Note: Since this interrupt is non-maskable, another NMIIB can occur before the first is finished. Care should be taken when using NMIINB to avoid this.

Reset (RESETB)
This output is a buffered version of the CPU's internal reset signal, for use by other circuits on chip that need to be initialized.

Reset Input (RESINB)
This input is used to reset the microprocessor. Reset must be held low for at least two clock cycles after V_{DD} reaches operating voltage from a power down. A positive transition on this pin will then cause an initialization sequence to begin. Likewise, after the system has been operating, a low on this line of at least two cycles will cease microprocessing activity, followed by initialization after the positive edge on RESINB.

When a positive edge is detected, there is an initialization sequence lasting six clock cycles. Then the interrupt mask flag is set, the decimal mode is cleared, and the program counter is loaded with the restart vector from locations FFFC (low byte) and FFFD (high byte). This is the start location for program control. This input should be high in normal operation. A latched version of RESINB will appear at the RESETB output after one falling F2 edge.

Set Overflow (SOB)
A negative transition on this line sets the overflow bit in the status code register. The signal is sampled halfway through each cycle (see Timing Diagram).

Synchronize (SYNC)
This output line is provided to identify those cycles during which the microprocessor is doing an OP CODE fetch. The SYNC line goes high at the beginning of an OP CODE fetch and stays high for the remainder of that cycle. If OP CODEs of X3 or XB (X = don't care) are

■ SIGNAL DESCRIPTION (CONTINUED)

fetched, another OP CODE will be fetched in the next cycle, and SYNC will remain high for the two fetch cycles.

Write Enable (WEB)
This signal is normally in the high state, indicating that the CPU is reading data from memory. If AINT is high, the CPU's internal write signal will appear on the WEB output. When AINT is low, the WEIB input is gated to the WEB output. A low on WEB indicates that whatever device has control of the busses has data to be written to the addressed memory location.

External Write Enable Input (WEIB)
This input is used in conjunction with the AI0-AI15 inputs when AINT is pulled low, to indicate whether the addressed memory location is to be read from or written to.

■ INSTRUCTION SET — ALPHABETICAL SEQUENCE

ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift One Bit Left
*BBRn	Branch on Bit "n" Reset
*BBSn	Branch on Bit "n" Set
BCC	Branch on Carry Clear
BCS	Branch on Carry Set
BEQ	Branch on Result Zero
BIT	Test Memory Bits with Accumulator
BMI	Branch on Result Minus
BNE	Branch on Result not Zero
BPL	Branch on Result Plus
*BRA	Branch Always
BRK	Force Break
BVC	Branch on Overflow Clear
BVS	Branch on Overflow Set
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
*DEA	Decrement Accumulator
DEC	Decrement by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive-or" Memory with Accumulator
*INA	Increment Accumulator
INC	Increment by One
INX	Increment Index X by One
INY	Increment Index Y by One
JMP	Jump to New Location
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right
NOP	No Operation
ORA	"OR" Memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Processor Status on Stack
* PHX	Push Index X on Stack
*PHY	Push Index Y on Stack
PLA	Pull Accumulator from Stack
PLP	Pull Processor Status from Stack
* PLX	Pull Index X from Stack
*PLY	Pull Index Y from Stack
*RMBn	Reset Memory Bit "n"
ROL	Rotate One Bit Left
ROR	Rotate One Bit Right
RTI	Return from Interrupt
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Bit
*SMBn	Set Memory Bit "n"
STA	Store Accumulator in Memory
STX	Store Index X in Memory
STY	Store Index Y in Memory
*STZ	Store Zero in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
* TRB	Test and Reset Memory Bits with Accumulator
*TSB	Test and Set Memory Bits with Accumulator
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Pointer
TYA	Transfer Index Y to Accumulator

Note: * = New Instruction

NCR

■ OPERATIONAL CODES, EXECUTION TIME, AND MEMORY REQUIREMENTS

		IMME-DIATE			ABSO-LUTE			ZERO PAGE			ACCUM			IM-PLIED			(IND), X			(IND), Y			ZPG, X			ZPG, Y			ABS, X			ABS, Y			RELA-TIVE			(ABS)			ABS (IND, X)			(ZPG)			PROCESSOR STATUS CODES	
																																													7 6 5 4 3 2 1 0	
MNE	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N V . B D I Z C	MNE
ADC	A + M + C → A (1,3)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2				7D	4	3	79	4	3													72	5	2	N V . . . . Z C	ADC
AND	A ∧ M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2				3D	4	3	39	4	3													32	5	2	N . . . . . Z .	AND
ASL	C→[7 0]→0 (1)				OE	6	3	06	5	2	0A	2	1										16	6	2				1E	6	3																N . . . . . Z C	ASL
BBRn	Branch if M_n = 0 (2)							0F-7F	5	3																																						. . . . .	BBRn
BBSn	Branch if M_n = 1 (2)							8F-FF	5	3																																							. . . . .	BBSn
BCC	Branch if C=0 (2)																																															. . . . .	BCC
BCS	Branch if C=1 (2)																																															. . . . .	BCS
BEQ	Branch if Z=1 (2)																																															. . . . .	BEQ
BIT	A ∧ M (4,5)	89	2	2	2C	4	3	24	3	2													34	4	2				3C	4	3																	M_7→M_6→ . . . Z .	BIT
BMI	Branch if N=1 (2)																																															. . . . .	BMI
BNE	Branch if Z=0 (2)																																															. . . . .	BNE
BPL	Branch if N=0 (2)																																															. . . . .	BPL
BRA	Branch Always (2)																																															. . . . .	BRA
BRK	Break													00	7	1																																. . 1 . 1 . .	BRK
BVC	Branch if V=0 (2)																																															. . . . .	BVC
BVS	Branch if V=1 (2)																																															. . . . .	BVS
CLC	0 → C													18	2	1																																 0	CLC
CLD	0 → D													D8	2	1																																. . . . 0 . .	CLD
CLI	0 → I													58	2	1																																. . . . . 0 .	CLI
CLV	0 → V													B8	2	1																																. 0	CLV
CMP	A - M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2				DD	4	3	D9	4	3													D2	5	2	N . . . . . Z C	CMP
CPX	X - M	E0	2	2	EC	4	3	E4	3	2																																							N . . . . . Z C	CPX
CPY	Y - M	C0	2	2	CC	4	3	C4	3	2																																							N . . . . . Z C	CPY
DEA	A - 1 → A										3A	2	1																																		N . . . . . Z .	DEA
DEC	M - 1 → M (1)				CE	6	3	C6	5	2													D6	6	2				DE	6	3																N . . . . . Z .	DEC
DEX	X - 1 → X													CA	2	1																																N . . . . . Z .	DEX
DEY	Y - 1 → Y													88	2	1																																N . . . . . Z .	DEY
EOR	A ⊻ M → A	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2				5D	4	3	59	4	3													52	5	2	N . . . . . Z .	EOR
INA	A + 1 → A										1A	2	1																																		N . . . . . Z .	INA
INC	M + 1 → M (1)				EE	6	3	E6	5	2													F6	6	2				FE	6	3																N . . . . . Z .	INC
INX	X + 1 → X													E8	2	1																																N . . . . . Z .	INX
INY	Y + 1 → Y													C8	2	1																																N . . . . . Z .	INY
JMP	Jump to new loc				4C	3	3																																		6C	6	3	7C	6	3				. . . . .	JMP
JSR	Jump Subroutine				20	6	3																																											JSR
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2				BD	4	3	B9	4	3													B2	5	2	N . . . . . Z .	LDA
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																B6	4	2				BE	4	3														N . . . . . Z .	LDX
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2				BC	4	3																N . . . . . Z .	LDY
LSR	0→[7 0]→[C] (1)				4E	6	3	46	5	2	4A	2	1										56	6	2				5E	6	3																0 . . . . . Z C	LSR
NOP	PC + 1 → PC													EA	2	1																																. . . . .	NOP
ORA	A V M → A (1)	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2				1D	4	3	19	4	3													12	5	2	N . . . . . Z .	ORA
PHA	A → M_S S - 1 → S													48	3	1																																. . . . .	PHA
PHP	P → M_S S - 1 → S													08	3	1																																. . . . .	PHP
PHX	X → M_S S - 1 → S													DA	3	1																																. . . . .	PHX
PHY	Y → M_S S - 1 → S													5A	3	1																																. . . . .	PHY
PLA	S + 1 → S M_S → A													68	4	1																																N . . . . . Z .	PLA
PLP	S + 1 → S M_S → P													28	4	1																																N V . 1 D I Z C	PLP
PLX	S + 1 → S M_S → X													FA	4	1																																N . . . . . Z .	PLX
PLY	S + 1 → S M_S → Y													7A	4	1																																N . . . . . Z .	PLY
RMBn	0 → M_n							07-77	5	2																																						. . . . .	RMBn
ROL	[7 0]→[C] (1)				2E	6	3	26	5	2	2A	2	1										36	6	2				3E	6	3																N . . . . . Z C	ROL
ROR	[C]→[7 0] (1)				6E	6	3	66	5	2	6A	2	1										76	6	2				7E	6	3																N . . . . . Z C	ROR
RTI	Return from Inter.													40	6	1																																N V . 1 D I Z C	RTI
RTS	Return from Subr.													60	6	1																																. . . . .	RTS
SBC	A - M - $\overline{C}$ → A (1,3)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2				FD	4	3	F9	4	3													F2	5	2	N V . . . . Z C	SBC
SEC	1 → C													38	2	1																																 1	SEC
SED	1 → D													F8	2	1																																. . . . 1 . .	SED
SEI	1 → I													78	2	1																																. . . . . 1 .	SEI
SMBn	1 → M_n							87-F7	5	2																																							. . . . .	SMBn
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2				9D	5	3	99	5	3													92	5	2	. . . . .	STA
STX	X → M				8E	4	3	86	3	2																96	4	2																						STX
STY	Y → M				8C	4	3	84	3	2													94	4	2																										STY
STZ	00 → M				9C	4	3	64	3	2													74	4	2				9E	5	3																		STZ
TAX	A → X													AA	2	1																																N . . . . . Z .	TAX
TAY	A → Y													A8	2	1																																N . . . . . Z .	TAY
TRB	$\overline{A}$ ∧ M → M (4)				1C	6	3	14	5	2																																								Z .	TRB
TSB	A V M → M (4)				0C	6	3	04	5	2																																									. . . . . Z .	TSB
TSX	S → X													BA	2	1																																N . . . . . Z .	TSX
TXA	X → A													8A	2	1																																N . . . . . Z .	TXA
TXS	X → S													9A	2	1																																		. . . . .	TXS
TYA	Y → A													98	2	1																																N . . . . . Z .	TYA

Notes:

1. Add 1 to "n" if page boundary is crossed.
2. Add 1 to "n" if branch occurs to same page.
   Add 2 to "n" if branch occurs to different page.
3. Add 1 to "n" if decimal mode.
4. V bit equals memory bit 6 prior to execution.
   N bit equals memory bit 7 prior to execution.

*5. The immediate addressing mode of the BIT instruction leaves bits 6 & 7 (V & N) in the Processor Status Code Register unchanged.

X Index X
Y Index Y
A Accumulator
M Memory per effective address
M_S Memory per stack pointer

\+ Add
− Subtract
∧ And
V Or
⊻ Exclusive or

n No. Cycles
No. Bytes
M_6 Memory bit 6
M_7 Memory bit 7
M_n Memory bit n

■ MICROPROCESSOR OP CODE TABLE

S D	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	BRK	ORA ind, X			TSB* zpg	ORA zpg	ASL zpg	RMB0* zpg	PHP	ORA imm	ASL A		TSB * abs	ORA abs	ASL abs	BBR0* zpg	0
1	BPL rel	ORA ind, Y	ORA*† (zpg)		TRB* zpg	ORA zpg, X	ASL zpg, X	RMB1* zpg	CLC	ORA abs, Y	INA* A		TRB* abs	ORA abs, X	ASL abs, X	BBR1* zpg	1
2	JSR abs	AND ind, X			BIT zpg	AND zpg	ROL zpg	RMB2* zpg	PLP	AND imm	ROL A		BIT abs	AND abs	ROL abs	BBR2* zpg	2
3	BMI rel	AND ind, Y	AND*† (zpg)		BIT* zpg, X	AND zpg, X	ROL zpg, X	RMB3* zpg	SEC	AND abs, Y	DEA* A		BIT*† abs, X	AND abs, X	ROL abs, X	BBR3* zpg	3
4	RTI	EOR ind, X				EOR zpg	LSR zpg	RMB4* zpg	PHA	EOR imm	LSR A		JMP abs	EOR abs	LSR abs	BBR4* zpg	4
5	BVC rel	EOR ind, Y	EOR*† (zpg)			EOR zpg, X	LSR zpg, X	RMB5* zpg	CLI	EOR abs, Y	PHY*			EOR abs, X	LSR abs, X	BBR5* zpg	5
6	RTS	ADC ind, X			STZ* zpg	ADC zpg	ROR zpg	RMB6* zpg	PLA	ADC imm	ROR A		JMP (abs)	ADC abs	ROR abs	BBR6* zpg	6
7	BVS rel	ADC ind, Y	ADC*† (zpg)		STZ* zpg, X	ADC zpg, X	ROR zpg, X	RMB7* zpg	SEI	ADC abs, Y	PLY*		JMP*† abs (ind, X)	ADC abs, X	ROR abs, X	BBR7* zpg	7
8	BRA* rel	STA ind, X			STY zpg	STA zpg	STX zpg	SMB0* zpg	DEY	BIT* imm	TXA		STY abs	STA abs	STX abs	BBS0* zpg	8
9	BCC rel	STA ind, Y	STA*† (zpg)		STY zpg, X	STA zpg, X	STX zpg, Y	SMB1* zpg	TYA	STA abs, Y	TXS		STZ* abs	STA abs, X	STZ* abs, X	BBS1* zpg	9
A	LDY imm	LDA ind, X	LDX imm		LDY zpg	LDA zpg	LDX zpg	SMB2* zpg	TAY	LDA imm	TAX		LDY abs	LDA abs	LDX abs	BBS2* zpg	A
B	BCS rel	LDA ind, Y	LDA*† (zpg)		LDY zpg, X	LDA zpg, X	LDX zpg, Y	SMB3* zpg	CLV	LDA abs, Y	TSX		LDY abs, X	LDA abs, X	LDX abs, Y	BBS3* zpg	B
C	CPY imm	CMP ind, X			CPY zpg	CMP zpg	DEC zpg	SMB4* zpg	INY	CMP imm	DEX		CPY abs	CMP abs	DEC abs	BBS4* zpg	C
D	BNE rel	CMP ind, Y	CMP*† (zpg)			CMP zpg, X	DEC zpg, X	SMB5* zpg	CLD	CMP abs, Y	PHX*			CMP abs, X	DEC abs, X	BBS5* zpg	D
E	CPX imm	SBC ind, X			CPX zpg	SBC zpg	INC zpg	SMB6* zpg	INX	SBC imm	NOP		CPX abs	SBC abs	INC abs	BBS6* zpg	E
F	BEQ rel	SBC ind, Y	SBC*† (zpg)			SBC zpg, X	INC zpg, X	SMB7* zpg	SED	SBC abs, Y	PLX*			SBC abs, X	INC abs, X	BBS7* zpg	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

Note: * = New OP Codes
Note: † = New Address Modes

NCR

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8-BIT GENERAL PURPOSE ANALOG TO DIGITAL CONVERTER

- **Single or dual supply operation**
- **2V to 5V full scale range**
- **8-Bit Linearity**
- **Low Power Consumption**
- **30 μs Conversion Cycle**
- **CMOS Compatible**

NCR's 8-bit A to D supercell is a successive approximation converter utilizing CMOS technology in a switched capacitor charge redistribution architecture. The A to D performs an 8-bit unipolar conversion (8-bit magnitude) at rates ranging from 20μs to 100μs, under control of a 100 KHz to 500 KHz master clock. The full scale analog range of the converter is 2.0V to 5.0V.

ELECTRICAL SPECIFICATION ROOM TEMPERATURE

	Min	Typ	Max	Comments
V_{DD} Supply Current (mA)		1.1	1.25	F_{CONV} = 50KHZ V_{DD} = 5V
V_{SS} Supply Current (mA)		0.17	0.2	V_{SS} = -5V VREF' = 2.5V
		0.34	0.4	V_{SS} = -5V VREF' = 5.0V
Offset Voltage (mV)	-22	-10	+2	V_{SS} = 0
	-10	+2	+14	V_{SS} = -2V VREF' = 2.5V
	-5	+7	+19	V_{SS} = -5V VREF' = 2.5V
	-35	-8	+19	V_{SS} = -5V VREF' = 5.0V
Gain Error (%FS)		0.3	1.0	V_{SS} = 0 VREF' = 2.5V
		0.1	0.4	V_{SS} = -2V VREF' = 2.5V
		0.1	0.4	V_{SS} = -5V VREF' = 2.5V
		0.05	0.2	V_{SS} = -5V VREF' = 5.0V
Integral Non-Linearity (LSB)		1.0	2.0	V_{SS} = 0 VREF' = 2.5V
		0.6	0.8	V_{SS} = -2V VREF' = 2.5V
		0.6	0.8	V_{SS} = -5V VREF' = 2.5V
		0.6	0.8	V_{SS} = -5V VREF' = 5.0V
Differential Non-Linearity (LSB)		0.4	0.7	VREF' = 2.5V
		0.3	0.6	VREF' = 5.0V
A.C. Supply Rejection (dB) Positive Supply @ 10KHZ		30		
A.C. Supply Rejection (dB) Negative supply @ 10KHZ		26		V_{SS} = 0
		29		V_{SS} = -5V
Minimum Conversion Time (μs)		20	30	V_{SS} = -5V
Maximum Conversion Time (μs)			100	
Input capacitance (pf)				
VREF Input		50	60	
VIN Input		50	60	
BIAS IN Input		2	4	

I/O CONNECTION LIST

Name	Type	Function
MCLK	Digital Input	Master Clock Controling Successive Approximation Cycle
RST	Digital Input	Reset SAR after power up. Reset EOC Low.
SAMPLE	Digital Input	Initiate Conversion Cycle
EOC	Digital Output	Indicates Completion of Conversion Cycle
D7	Digital Output	BIT 8 (MSB)
D6	Digital Output	BIT 7
D5	Digital Output	BIT 6
D4	Digital Output	BIT 5
D3	Digital Output	BIT 4
D2	Digital Output	BIT 3
D1	Digital Output	BIT 2
D0	Digital Output	BIT 1 (LSB)
VIN	Analog Input	Input Signal Voltage
VREF	Analog Input	Reference Voltage
BIAS VREF	Analog Input	Voltage For Connection To Negative Follower Input For Supply Independent Biasing
BIAS IN	Analog Input	Voltage From Follower Output For Supply Independent Biasing
V_{DD}	Supply Input	Positive Supply
AN GND	Supply Input	Analog Ground
DIG GND	Supply Input	Digital Ground
V_{SS}	Supply Input	Negative Supply (Analog Only)

NCR SEMICUSTOM DESIGN

Specifications subject to change without notice.

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Digital Considerations

Before the successive approximation register (SAR) can begin cycling, the logic must be reset to an initial state after power is applied. A reset input (RST) is included in the SAR circuit for this purpose. Reset will occur when RST is brought high and the master clock input (MCLK) is low. The minimum duration of a true RST•MCLK to insure reset is 20 ns. The RST input may be supplied from off-chip or internally by using a standard cell, POR, from the NCR library.

The complete conversion cycle requires a minimum of 10 master clock cycles to perform the functions of capacitor array reset, signal sampling and 8-bits of successive approximation. Two modes of signal sampling are available; external control or free-running operation. External sampling control is enabled one full MCLK cycle after the previous conversion has been completed. As shown in Figure 1, a high sample input (SAMPLE) following a high to low MCLK transition after a high to low end of conversion ($\overline{EOC}$) transition will initiate signal sampling and a subsequent conversion cycle. The minimum duration for a valid SAMPLE input is 10 ns. The analog sample is acquired with the next positive MCLK edge following a high SAMPLE input. A low to high $\overline{EOC}$ transition indicates the signal has been sampled and a conversion initiated. Free-running operation may be selected by connecting SAMPLE to the positive supply. As shown in Figure 2, free-running operation results in a sample acquisition once every 10 MCLK cycles. Signal sampling again occurs on a positive MCLK edge.

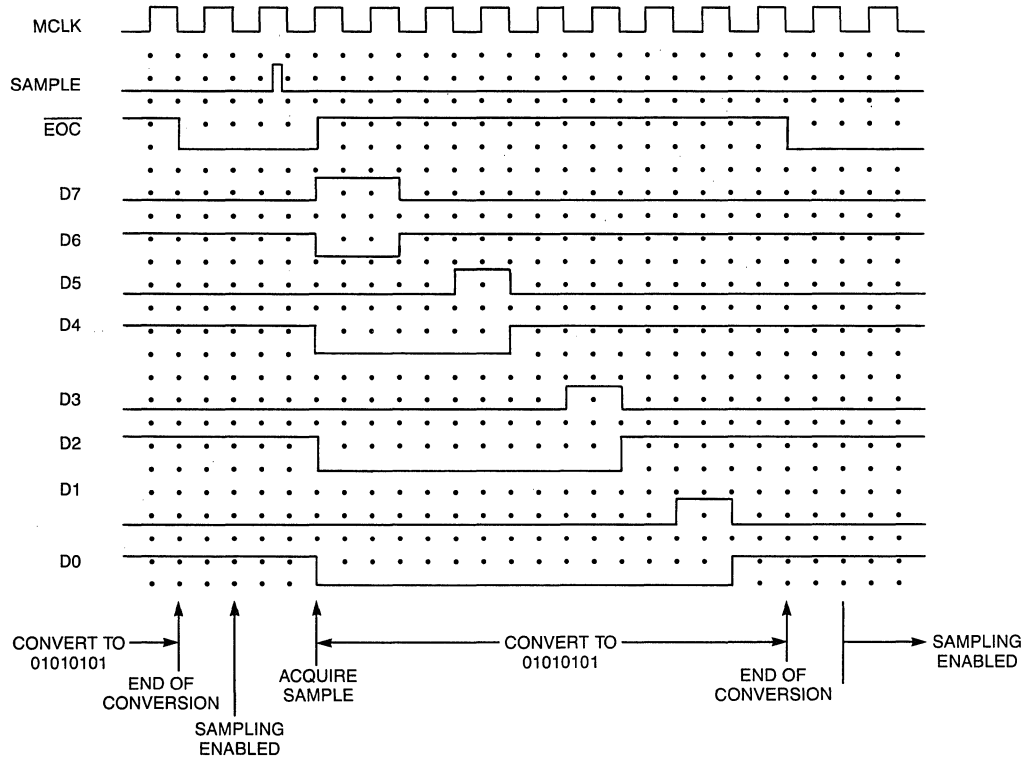

Figure 1. A TO D CONVERSION CYCLE WITH EXTERNAL SAMPLING CONTROL

Data becomes valid at the SAR outputs (D0-D7) during the conversion, starting with the MSB (D7) and ending with the LSB (D0). The high to low transition of $\overline{EOC}$ indicates the conversion is complete. Data will remain latched in the SAR until the next sample is acquired as indicated by a low to high transition of $\overline{EOC}$. If subsequent latching of the SAR outputs is required, the falling edge of $\overline{EOC}$ may be used for latch control synchronization. It is important to note that the skew between the $\overline{EOC}$ falling edge and the final transition of D0 to the steady state LSB value is dependent on the loading of these two outputs. For subsequent latching of the output data, it is recommended that a delayed version of $\overline{EOC}$; i.e., $\overline{EOC}$ latched with a positive MCLK edge, be used as a latching control signal.

Data is output in positive true binary format. All digital outputs (D0-D7 and $\overline{EOC}$) are unbuffered, however buffers may be selected from the NCR library of standard cells if required. When bringing output signals off-chip, keep in mind that the majority of NCR library output pad cells are inverting. Therefore, the data format will be changed to negative true binary unless an additional inversion is added to the output signal path.

All logic inputs are CMOS compatible. If TTL compatibility is required, TTL to CMOS input pad cells from the NCR standard cell library must be used for logic inputs.

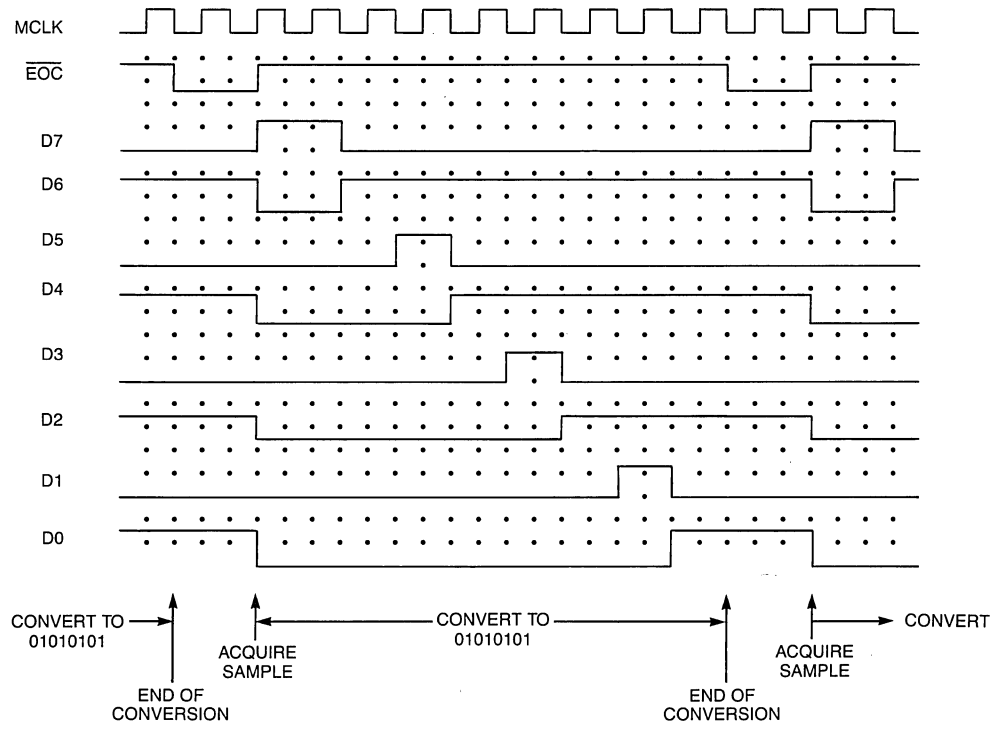

Figure 2. A TO D CONVERSION CYCLE WITH FREE-RUNNING OPERATION

Analog Considerations

Power Supplies

Two separate ground connections; one for analog circuitry and one for digital circuitry, are required for A to D operation. These may be connected together at the supercell boundary, at the ground bonding pad, or off-chip. Noise considerations dictate that analog and digital grounds be connected at only a single point. If the connection is made on-chip, the analog grounding path should not share any high current digital grounding connections. An off-chip connection should be made as close to the package as possible, or alternatively at the common grounding point between separate analog and digital system supplies, if applicable.

The positive supply for the A to D is common between analog and digital circuitry within the supercell, and has a nominal value of 5.0± 0.5V. If other additional logic is contained on chip, the connection between A to D and chip supplies should not include any high current digital paths. Alternatively, connection can be made at the positive supply bonding pad.

The A to D also requires a supply V_{SS}) that is negative with respect to ground in certain cases. For operation, the difference between V_{DD} and V_{SS} must be greater than or equal to twice the full scale signal swing as set by the voltage reference. In other words, applications having full scale swings greater than 2.5V require a separate V_{SS} supply. V_{SS}, if required, may range anywhere from the minumum set by the full scale swing to –5.0V. A negative supply generator from the NCR cell library (available October '84) may be used to generate V_{SS}. If V_{SS} is not required, the V_{SS} supercell connection must be tied on-chip to analog ground.

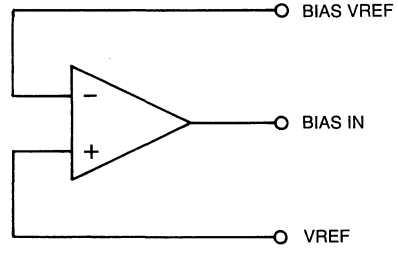

Figure 3. FOLLOWER CONNECTION FOR SUPPLY INDEPENDENT BIAS CIRCUIT

Biasing

Biasing for the A to D comparator is supplied through a supply voltage independent bias circuit which derives a constant current from the reference voltage. A non-precision Op Amp must be connected to the A to D supercell as shown in Figure 3 for bias network operation. This Op Amp may be placed on-chip using OPAMPL, OPAMPM or PPAMP (available August '84) from the NCR library. Alternatively, an off-chip Op Amp, such as the 741, may be used. The nominal value of the Op Amp output voltage will be approximately V_{DD}-VREF'-1.8V, where VREF' is the full scale swing of the converter, and V_{DD} is nominally 5V. The main requirement for the Op Amp is to insure adequate output voltage swing given the power supplies available.

Reference Voltage

Internally, the A to D supercell is a positive supply reference system. Referencing to the positive supply is desirable from the standpoint of supply rejection to the positive rail, which is common for analog and digital portions of the circuit. The positive supply reference system is diagramed in Figure 4. In this diagram, VREF' is the full scale swing of the signal and VREF is the absolute reference voltage with respect to ground; i.e., VREF' = V_{DD}–VREF. VREF is the voltage used for comparison with the signal level. The signal voltage may range between VREF and V_{DD}. The magnitude of VREF with respect to ground tracks V_{DD} variations, as does the signal voltage with respect to the ground.

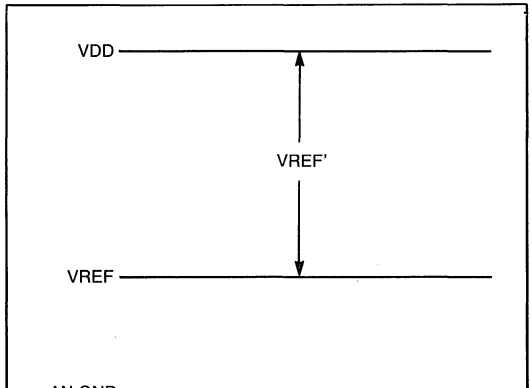

Figure 4. POSITIVE SUPPLY REFERENCING

The reference voltage may be supplied from off-chip using a standard reference and an Op Amp to subtract the reference voltage from V_{DD}. Alternatively, an on-chip amp such as OPAMPM or PPAMP from the NCR library may be used to subtract the reference voltage from V_{DD}. Another option is using the externally trimmed on-chip reference, VRFVDD (available in October '84) from the NCR library, which produces a voltage referenced to V_{DD}.

Any ground referenced signal requires level translation to fit the positive supply referenced scheme. This is accomplished by summing VREF to the signal; either off-chip or on-chip using PPAMP from the NCR cell library. Figures 5 and 6 show possible summing configurations, with accommodations made for gain and offset tweeking. A floating reference signal may be interfaced directly to the A to D by using VREF as the signal common.

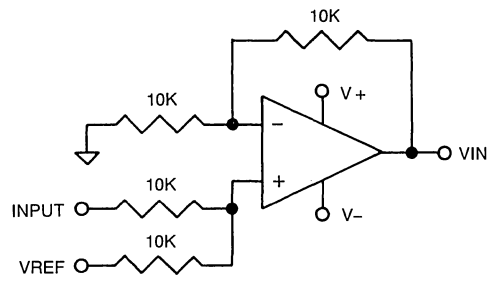

Figure 5. CONFIGURATION FOR SUMMING SIGNAL VOLTAGE TO VREF

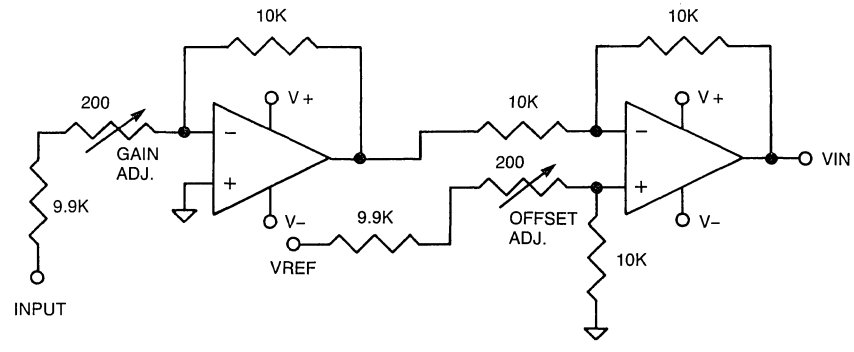

Figure 6. CONFIGURATION FOR SUMMING SIGNAL VOLTAGE TO VREF WITH ADJUSTABLE GAIN AND OFFSET

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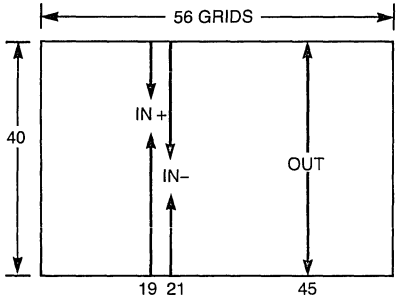
GENERAL PURPOSE OP AMP

- **Low Leakage CMOS Inputs**
- **3 Bias Current Options Available**
- **Class A Output Stage**
- **Internally Compensated**
- **Low Input Offset Voltage**
- **Low Input Referred Noise**
- **Internal or Pad Row Placement**

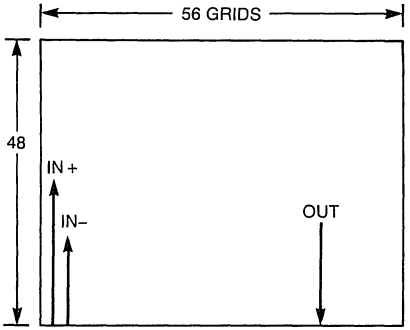
The NCR cell library General Purpose Op Amp is a two-stage differential input, single-ended output, high-gain amplifier. Compensation for unity gain operation is provided internally utilizing a poly/thin oxide/diffusion capacitor. A class A output stage provides drive capability for capacitive loads of up to 20pF and resistive loads of greater than 10K. CMOS inputs reduce leakage currents to less than 100pA in applications where connection to a bonding pad is not required.

Six versions of the Op Amp are available, all of which use the same Op Amp core circuit. Three different current bias options are offered to allow the optimization of power consumption, output drive, open loop gain and bandwidth for any specific application. (Low, medium, and high bias options are referenced with an "L," "M," or "H" in the cell name.) Two cell geometry options are also offered with each bias option. The standard cell geometry allows the circuit to be placed internally on the chip in a row of analog cells. The pad cell geometry option allows the circuit to be placed in a row of bonding pads. This is useful for non-pad limited chips where normally unused area is available in the periphery. (The pad cell geometry option is referenced by a "P" at end of the cell name.)

CELL GEOMETRY

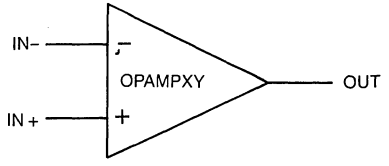


STANDARD



PAD

LOGIC SYMBOL



X = L, M, H (LOW, MEDIUM, HIGH BIAS)
Y = P FOR PAD GEOMETRY

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ELECTRICAL SPECIFICATIONS
MEDIUM BIAS OPTION

(All Measurements Made at Room Temperature)

	Min	Typ	Max	Conditions
Supply Current (mA)		0.45	0.55	$V_{DD} - V_{SS}$ = 5V, R_L = 100K
		0.65	0.75	$V_{DD} - V_{SS}$ = 10V, R_L = 100K
Open Loop Gain (V/mV) *(Note 6)*	35	40		$V_{DD} - V_{SS}$ = 5V, R_L = 500K
	4.1	4.7		R_L = 20K
	25	30		$V_{DD} - V_{SS}$ = 10V, R_L = 500K
	3.8	4.3		R_L = 20K
Input Offset Voltage (mV)		1.5	5.00	
Input Common Mode Range (V)		V_{SS} +1.4 to V_{DD} – 1.4		$V_{DD} - V_{SS}$ = 5V, CMRR > 94dB
	V_{SS} +1.2 to V_{DD} –1.2	V_{SS} +0.9 to V_{DD} –0.9		$V_{DD} - V_{SS}$ = 5V, CMRR > 80dB
		V_{SS} +2.8 to V_{DD} –2.8		V_{DD}–V_{SS} = 10V, CMRR > 70dB
	V_{SS} +1.2 to V_{DD} –1.2	V_{SS} +1.0 to V_{DD} –1.0		V_{DD}–V_{SS} = 10V, CMRR > 60dB
Common Mode Rejection Ratio (dB)		100		$V_{DD} - V_{SS}$ = 5V, V_{SS} + 1.8 < V_{CM} < V_{DD} –1.8
		72		$V_{DD} - V_{SS}$ = 10V, V_{SS} +3.5 < V_{CM} < V_{DD} –3.5
High Level Output Voltage (V) *(Note 6)*	V_{DD}–0.5			$V_{DD} - V_{SS}$ = 5V, Av > 10 V/mV, R_L = 500K
	V_{DD} –0.5			Av > 1 V/mV, R_L = 20K
	V_{DD} –1.3			$V_{DD} - V_{SS}$ = 10V, Av > 10 V/mV, R_L = 500K
	V_{DD} –1.5			Av > 1 V/mV, R_L = 20K
Low Level Output Voltage (V) *(Note 6)*			V_{SS} +0.75	$V_{DD} - V_{SS}$ = 5V, Av > 10 V/mV, R_L = 500K
			V_{SS} +0.75	Av > 1 V/mV, R_L = 20K
			V_{SS} +1.00	$V_{DD} - V_{SS}$ = 10V, Av > 10 V/mV, R_L = 500K
			V_{SS} +3.00	Av > 1 V/mV, R_L = 20K

ELECTRICAL SPECIFICATIONS
MEDIUM BIAS OPTION

(All Measurements Made at Room Temperature)

	Min	Typ	Max	Conditions
Unity Gain Bandwith MHz *(Note 1)*	1.2 1.4	1.6 1.8		V_{DD}-V_{SS} = 5V, R_L = 10K, C_L = 15pF V_{DD}-V_{SS} = 10V, R_L = 10K, C_L = 15pF
1% Settling Time (μs) *(Note 2)*		3.0 3.0	4.5 4.5	V_{DD}-V_{SS} = 5V, R_L = 10K, C_L = 15pF V_{DD}-V_{SS} = 10V, R_L = 10K, C_L = 15pF
Overshoot % *(Note 2)*		29 34	34 38	V_{DD} - V_{SS} = 5V R_L = 10K, C_L = 15pF V_{DD} - V_{SS} = 10V, R_L = 10K, C_L = 15pF
Positive Slew Rate (V/μs) *(Note 3)*	2.0 2.5	3.5 4.0		V_{DD}-V_{SS} = 5V, R_L = 100K, C_L = 15pF V_{DD}-V_{SS} = 10V, R_L = 100K, C_L = 15pF
Negative Slew Rate (V/μs) *(Note 3)*	1.5 2.0	3.0 3.5		V_{DD}-V_{SS} = 5V, R_L = 100K, C_L = 15pF V_{DD}-V_{SS} = 10V, R_L = 100K, C_L = 15pF
DC Power Supply Rejection Ratio, Positive Supply (dB)	60 62	66 72		V_{DD} - V_{SS} = 5V, R_L = 100K V_{DD} - V_{SS} = 10V, R_L = 100K
DC Power Supply Rejection Ratio, Negative Supply (dB)				V_{DD} - V_{SS} = 5V, R_L = 100K V_{DD} - V_{SS} = 10V, R_L = 100K
AC Power Supply Rejection Ratio, Positive Supply (dB) *(Note 4)*	60 25	66 28		f = 1 KHz, R_L = 100K f = 100 KHz, R_L = 100K
AC Power Supply Rejection Ratio, Negative Supply (dB) *(Note 4)*				f = 1 KHz, R_L = 100K f = 100 KHz, R_L = 100K
Input Refered Noise ($nV_{RMS}/\sqrt{Hz}$) *(Note 5)*		80 40 40		V_{DD} - V_{SS} = 5V, f = 100 Hz f = 1 KHz f = 100 KHz

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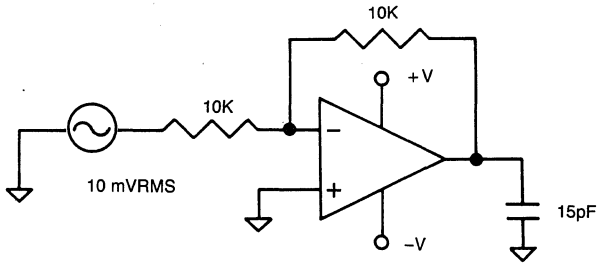
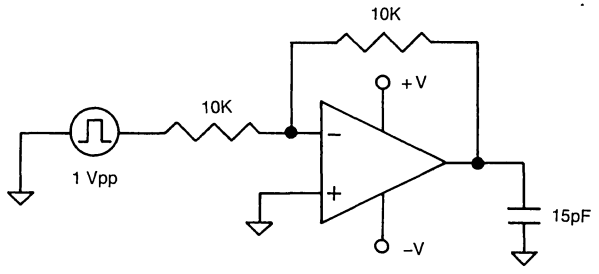
ELECTRICAL SPECIFICATIONS
MEDIUM BIAS OPTION

(All Measurements Made at Room Temperature)

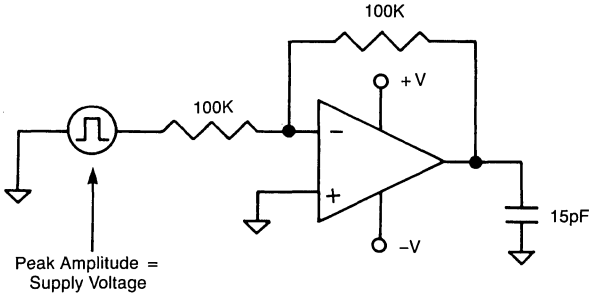
	Min	Typ	Max	Conditions
1/f Noise Corner (Hz) *(Note 5)*		400		$V_{DD}-V_{SS}=5V$
Input Referred Broadband Noise (μV_{RMS}) *(Note 5)*		50		$V_{DD}-V_{SS}=5V$, f = 10Hz to 1.4 MHz
Input Current (μA) (Bonded Inputs)		0.2	1.0	Due to protection diodes $V_{DD}-V_{SS}=5V$
Input Current Offset (μA) (Bonded Inputs)		0.05		$V_{IN}+ = V_{IN}-$
Input Capacitance (pF)		5		
Input Capacitance (pF) (Bonded Inputs)		6		



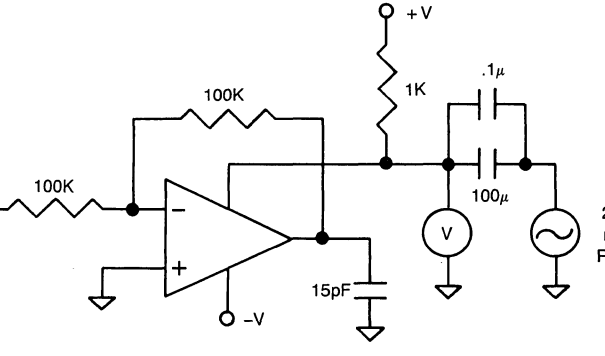
NOTE 1. Closed Loop Frequency Response Measurement Configuration



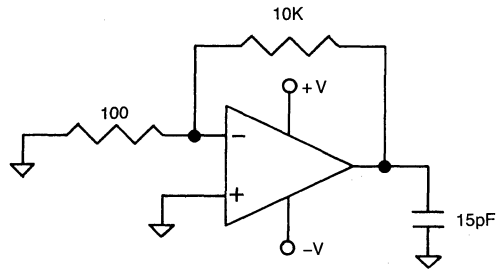
NOTE 2. Settling Time Measurement Configuration



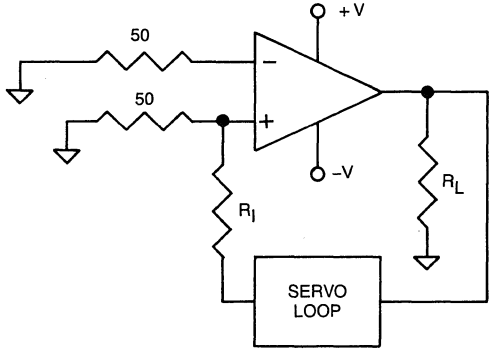
NOTE 3. Slew Rate Measurement Configuration



NOTE 4. AC Power Supply Rejection Configuration



NOTE 5. Noise Measurement Configuration



NOTE 6. Open Loop Measurement Configuration

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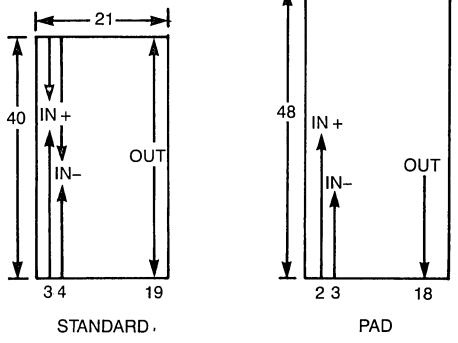
HIGH-SPEED LOW-POWER COMPARATOR
COMP05 COMP5P

- **Fast Response Time**
- **Low Power**
- **High Gain**
- **Low Leakage CMOS Inputs**
- **Rail to Rail Output Swing**
- **Internal or Pad Row Placement**

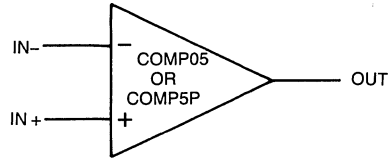
COMP05 is a two-stage differential input, single-ended output voltage comparator. The second stage uses positive feedback to provide fast response time while minimizing quiescent bias current. Rail-to-rail output swing is obtained by a circuit configuration resembling a CMOS logic gate. The comparator output is therefore compatible with all CMOS logic gates and buffers in the NCR standard cell library. CMOS inputs reduce leakage currents to less than 100pA in applications where connection to a bonding pad is not required.

Two cell geometry options are available for the comparator. The standard geometry (COMP05) allows the circuit to be placed next to other analog cells in an internal cell row. The pad cell geometry (COMP5P) allows the circuit to be placed in a bonding pad row. This is useful for non-pad-limited designs, where unused area is available in the chip periphery.

CELL GEOMETRY



LOGIC SYMBOL



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(Room Temperature)

	Min	Typ	Max	Conditions
Supply Current (μA)		90	120	V_{DD} = 5V
				2 Vpp 10KHz Input
Supply Voltage (V)	4.5	5.0	5.5	
Open Loop Gain (V/mV)	1000			
Input Common Mode Range (V)		1.8 to 3.4		V_{DD} = 5V
Low Level Output Voltage (V)			V_{SS} +0.1	R_L > 1M Ohm
High Level Output Voltage (V)	V_{DD} -0.1			R_L > 1M Ohm
Low to High Response Time (ns)				C_L = 1 pF
		130	200	10mV Overdrive
		60	80	100mV Overdrive
		40	60	1V Overdrive
High to Low Response Time (ns)				C_L = 1 pF
		350	520	10mV Overdrive
		90	120	100mV Overdrive
		40	60	1V Overdrive

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GENERAL PURPOSE COMPARATOR

- **Low Leakage CMOS Inputs**
- **Bias Current Options Available**
- **Low Offset Voltage**
- **Internal or Pad Row Placement**

The General Purpose Comparator is a two-stage voltage comparator with cascoded class A output. Bias options, as supplied by the Bias Generator Cell, allow the user to trade off response time and power dissipation.

HIGH BIAS
(ROOM TEMPERATURE)

	Min	Typ	Max	Conditions
Supply Current (mA)		1.4	1.7	$V_{DD} - V_{SS}$ = 5V 2 Vpp, 10 KHz Input
		2.2	3.0	$V_{DD} - V_{SS}$ = 10V 2 Vpp, 10 KHz Input
Input Offset Voltage (mV)		2.5	8.0	
Open Loop Gain (V/mV)	20			$V_{DD} - V_{SS}$ = 5V
Input Common Mode Range (V)				
Low Level Output Voltage (V)		0.3		V_{DD} = 5V, V_{SS} = 0V RL = 500K
High Level Output Voltage (V)		4.4		V_{DD} = 5V, V_{SS} = 0V RL = 500K
Low to High Response Time (μs)				$V_{DD} - V_{SS}$ = 5V C_L = 1 pF
		2.00	3.50	10 mV overdrive
		0.55	0.75	100 mV overdrive
		0.18	0.23	1V overdrive
				$V_{DD} - V_{SS}$ = 10V C_L = 1 pF
		3.60	5.50	10 mV overdrive
		0.70	0.90	100 mV overdrive
		0.20	0.30	1V overdrive
High to Low Response Time (μs)				$V_{DD} - V_{SS}$ = 5V C_L = 1 pF
		1.70	2.50	10 mV overdrive
		0.65	0.75	100 mV overdrive
		0.15	0.20	1V overdrive
				$V_{DD} - V_{SS}$ = 10V C_L = 1 pF
		1.60	2.50	10 mV overdrive
		0.40	0.55	100 mV overdrive
		0.15	0.20	1V overdrive

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MEDIUM BIAS
(ROOM TEMPERATURE)

	Min	Typ	Max	Conditions
Supply Current (mA)		0.60	0.75	$V_{DD} - V_{SS}$ = 5V 2 Vpp, 10 KHz Input
		0.90	1.10	$V_{DD} - V_{SS}$ = 10V 2 Vpp, 10 KHz Input
Input Offset Voltage (mV)		1.50	5.0	
Open Loop Gain (V/mV)	50			$V_{DD} - V_{SS}$ = 5V R_L > 100K
Input Common Mode Range (V)				
Low Level Output Voltage (V)			0.50	V_{DD} = 5V, V_{SS} = 0V R_L = 500K
High Level Output Voltage (V)			4.50	V_{DD} = 5V, V_{SS} = 0V R_L = 500K
Low to High Response Time (μs)				$V_{DD} - V_{SS}$ = 5V C_L = 1 pF
		4.50	7.0	10 mV overdrive
		1.0	1.25	100 mV overdrive
		0.35	0.45	1V overdrive
				$V_{DD} - V_{SS}$ = 10V C_L = 1 pF
		8.0	11.5	10 mV overdrive
		2.0	2.50	100 mV overdrive
		0.50	0.75	1V overdrive
High to Low Response Time (μs)				$V_{DD} - V_{SS}$ = 5V C_L = 1 pF
		2.50	4.50	10 mV overdrive
		0.90	1.10	100 mV overdrive
		0.25	0.35	1V overdrive
				$V_{DD} - V_{SS}$ = 10V C_L = 1 pF
		2.50	4.50	10 mV overdrive
		1.60	2.0	100 mV overdrive
		0.30	0.50	1V overdrive

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ANALOG SWITCH
ANSW

- **Rail-to-Rail Analog Signal Range**
- **Low Leakage**
- **CMOS Compatible**
- **Parallel Hookup for Lower Resistance**
- **Digital Cell Geometry**

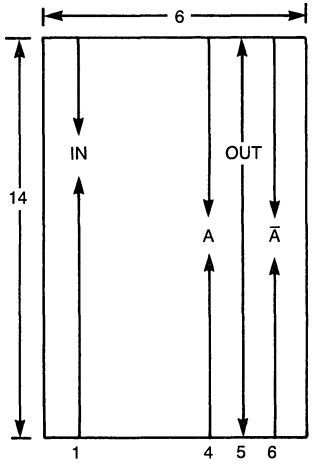
ANSW is a CMOS switch designed for multiplexer and sample and hold applications. The control gates for the n-channel and p-channel switching devices, A and $\overline{A}$ respectively, are the digital inputs to the cell. Usually, A and $\overline{A}$ will be complementary control signals. The switch is turned on by bringing A high and $\overline{A}$ low. Logic levels should equal the positive and negative supply voltages, with the difference between logic "high" and "low" ranging from 3V to 10V. Rail-to-rail analog signals can be switched using complementary control signals.

In specific applications with low analog signal levels, complementary switching control may not be necessary. For analog signals that range only within 2V of either rail, one of the control inputs may be tied to a supply voltage with only a small increase in "on" resistance. For example, in a circuit running off 5V and ground, tying $\overline{A}$ low will still allow switching of 3-5V signals, or tying A high will allow 0-2V switching.

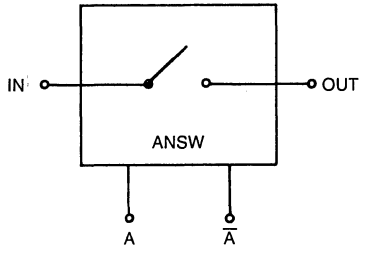
Interface from 0-5V CMOS logic to –5 to 5V switching control levels can be accomplished using a standard cell from the NCR library, LLS. Standard cells are also available for interfacing off-chip TTL to 0-5V CMOS.

In applications where lower "on" resistance than that of a single switch is required, switch cells may be connected in parallel. When a parallel combination of cells is used, the effective resistance of the switch is lowered, but charge injection and leakage will increase. "Off" isolation will also degrade, but this parameter is load dependent and the amount of signal feedthrough in the "off" state will vary with the specific application.

CELL GEOMETRY



LOGIC SYMBOL



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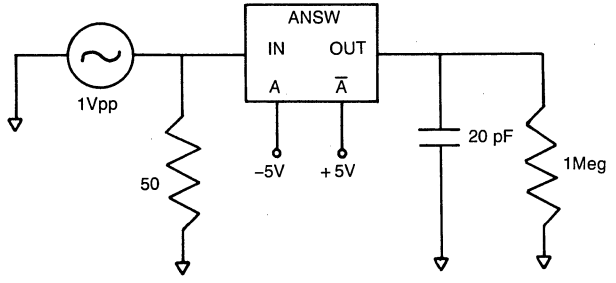
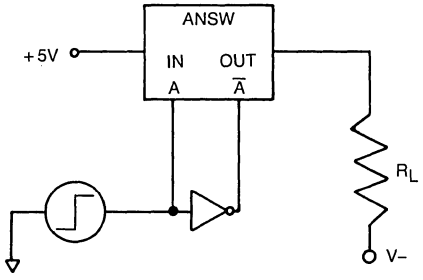
ELECTRICAL SPECIFICATION
ROOM TEMPERATURE

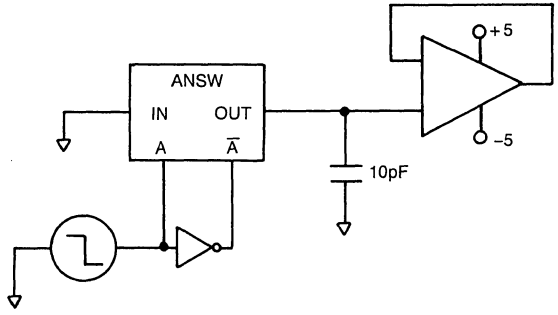
	Min	Typ	Max	Comments
"On" Resistance (k-ohm)		2.5	2.8	5V Control
		1.8	2.3	10V Control
A. C. Isolation (dB) (Note 1)	60	66		f = 1 KHz
	46	50		f = 20 KHz
Turn on Time (ns) (Note 2)				5V Control
		70	100	R_{ON} = 5K, R_L = 5K
		160	200	R_{ON} = 3K, R_L = 5K
				10V Control
		50	80	R_{ON} = 5K, R_L = 5K
		120	200	R_{ON} = 2K, R_L = 5K
Charge Injection (fC) (Note 3)		200	400	5V Control
		270	600	10V Control
Junction Leakage (pA)		0.2		



Note 1. A.C. Isolation Measurement Configuration



NOTE 2. Turn On Time Measurement Configuration



NOTE 3. Charge Injection Measurement Configuration

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CURRENT BIAS GENERATORS

- **Operation with 5V to 10V supply current**
- **3 current options available**

The current Bias Generator cell is a supply-independent current source, useful for circuit biasing and constant current pull-up application.

BIAS GENERATORS
(ROOM TEMPERATURE)

	Min	Typ	Max	Conditions
Supply Current (μA)				
LOW BIAS				$V_{DD} - V_{SS}$ = 5V Output connected to V_{SS}
MEDIUM BIAS		300	340	
HIGH BIAS		670	760	
LOW BIAS				$V_{DD} - V_{SS}$ = 10V Output connected to V_{SS}
MEDIUM BIAS		430	490	
HIGH BIAS		900	1040	
Output Current (μA)				$V_{DD} - V_{SS}$ = 5V Output connected to V_{SS}
LOW BIAS				
MEDIUM BIAS	115	132	150	
HIGH BIAS	425	500	575	
LOW BIAS				$V_{DD} - V_{SS}$ = 10V Output connected to V_{SS}
MEDIUM BIAS	130	153	175	
HIGH BIAS	550	637	725	
Output Supply Sensitivity (%/V)				Output connected to V_{SS}
LOW BIAS				
MEDIUM BIAS		3.3	5.0	
HIGH BIAS		5.8	7.0	
Output Supply Sensitivity (%/V) to Output Voltage				$V_{DD} - V_{SS}$ = 5V
LOW BIAS				$V_{OUT} < V_{DD}$ -1.5V
MEDIUM BIAS		1.7		$V_{OUT} < V_{DD}$ -1.5V
HIGH BIAS		5.2		$V_{OUT} < V_{DD}$ -1.5V

NCR SEMICUSTOM DESIGN

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GATE ARRAY LIBRARY

The NCR DHS (Digital High Speed) family of gate arrays includes arrays from 150 up to 1800 gates. They are manufactured using a 3μ silicon-gate CMOS process, and were designed for a linear shrink of the core to 2.25μ. They currently utilize a single metallization layer with programmable contacts.

Each of the basic cells in the core of the gate array consists of three pairs of N-channel and P-channel transistors with a single polysilicon underpass. These cells are butted directly together without the poly routing area typically found in CMOS gate arrays. A tremendous space saving results from the ability to actual-route the interconnect over the active areas, and the speed is greatly improved through the ability to place contacts directly on the diffusions. Most of the connections on a DHS gate array can be made directly from the output diffusion to the gate of the next macro.

Clock speeds of up to 30 MHz are achievable with the DHS family of gate arrays, making them suitable for more demanding microprocessor systems and peripheral applications.

Array	Total Cells	Equiv. Gates	I/O Buffers	Total Pads
DHS-150	100	150	28	34
DHS-300	200	300	38	44
DHS-450	300	450	48	56
DHS-675	450	675	58	66
DHS-900	600	900	68	76
DHS-1200	800	1200	78	86
DHS-1500	1000	1500	90	98
DHS-1800	1200	1800	100	108

Specifications subject to change without notice.

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Total Cells	Unused Gates	Description
2	2	And-or-invert
2	0	And-or-invert
2	0	And-or-invert
2	0	And-or-invert
3	1	And-or-invert
1	0	And-or-invert
2	2	And-or-invert
2	2	And-or-invert
2	1	And-or-invert
2	0	And-or-invert
2	2	And-or-invert
4	0	D Flip-Flop
4	0	D Flip-Flop with active-high reset
4	0	D Flip-Flop with active-low reset
4	0	D Flip-Flop with active-high set
4	0	D Flip-Flop with active-low set
5	0	D Flip-Flop with active-high reset and set
5	0	D Flip-Flop with active-low reset and set
5	2	DF with active-low reset/active-high set

Total Cells	Unused Gates	Description
2	0	D Latch
2	0	D Latch with active-high reset
2	0	D Latch with active-low reset
2	0	D Latch with active-high set
2	0	D Latch with active-low set
3	1	D Latch with active-high reset and set
3	1	D Latch with active-low reset and set
1	2	Single inverter
1	1	Dual inverter
1	0	Triple inverter
—	—	Standard input protection
1	1	2-Input nand gate
1	0	3-Input nand gate
2	2	4-Input nand gate
2	1	5-Input nand gate
1	1	2-Input nor gate
1	0	3-Input nor gate
2	2	Or-and-invert
2	0	Or-and-invert
1	0	Or-and-invert

MACROS

Total Cells	Unused Gates	Description
2	2	Or-and-invert
2	2	Or-and-invert
2	1	Or-and-invert
2	0	Or-and-invert
—	—	Standard output driver
—	—	Double output driver
1	0	Partial Schmitt Trigger
1	0	Transmission switch
1	0	Tristate driver
1	0	TTL compatible input cell
1	0	Small, high speed exclusive-nor cell
1	0	Small, high speed exclusive-or cell

SUPERMACROS

7400 Series Equivalent	Description
74109	JK Flip-Flop
74109	JK Flip-Flop with active-low reset and set

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NCR/32 Processor Family

NCR/32 Processor Family

Features

- 32-bit system architecture
- 13.3 Megahertz frequency
- Effective emulation of mid-range mainframes
- Externally microprogrammable
- Real and virtual memory operation
- Large direct memory addressing
- Interface provided to slower peripherals
- On-chip error check and correction

Functional Description

The NCR/32 VLSI Processor family combines the latest advances in semiconductor technology with experience gained in three generations of computer mainframe design to provide a comprehensive microprogrammable 32-bit system architecture. Because the chipset is externally microprogrammable it can be used to capture existing software bases.

The NCR/32 VLSI Processor family consists of the Central Processor Chip (CPC), the Address Translation Chip (ATC), and the System Interface Controller (SIC). Additional members of the family include the Extended Arithmetic Chip (EAC), the System Interface Transmitter (SIT) and Receiver (SIR) chips, and the Bus Assist Chip (BAC).

The CPC performs the basic microprocessing function using four 32-bit internal data paths, complemented by two independent external data paths: the 32-bit Processor Memory (PM) Bus and the 16-bit Instruction Storage Unit (ISU) Bus. An integral part of the CPC is the Arithmetic Logic Unit (ALU) which is used for performing decimal and binary arithmetic functions and logical operations. There are two sets of registers in the CPC. The Register Storage Unit consists of 16, 32-bit registers used for storage and manipulation of data; the additional 22 registers of the Internal Register Unit are used as jump address registers and operand pointer registers. A three-stage pipeline insures that one microinstruction is being fetched, another read, and a third executed in the same time frame.

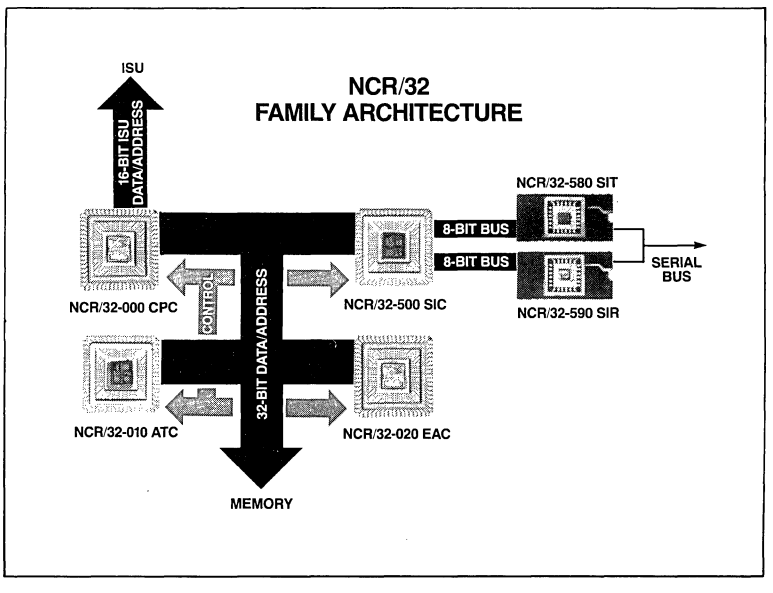
The system clock is a two-phase, non-overlapping clock operating at 13.3MHz. This yields a 150 nanosecond clock cycle with 90% of the microinstructions executing in one cycle.

The ATC provides memory management functions using either virtual or real memory addressing. To support virtual memory operations in the NCR/32 chipset, an extra PM bus cycle precedes the standard memory access. Two 32-bit registers, the TOD Register/Counter and the Interval Timer Monitor Register, are used for time interval monitoring. An NCR-patented "scrubbing" technique checks, and corrects if necessary, a 64K word block of memory every 1.048 seconds. The ATC has three virtual address page sizes: 1K, 2K, and 4K bytes.

The EAC is a performance booster used during arithmetic operations. Fixed point, decimal, and hexadecimal floating point formats are all handled by the EAC. (Hexadecimal floating point format is compatible with the IBM/370.) Results are in either single (one word) or double (two words) precision. Conversion operations between formats are also handled.

The SIC performs communication management between the NCR/32 chipset and the I/O devices. Used with the SIT and SIR (which perform data format conversions) the SIC sends and receives messages at up to 24 megabits per second per channel. The SIC/SIT/SIR communications subsystem operates in either Data Link Control mode or Local Area Network mode. In the Data Link Control mode, the SIC has access to eight transmission channels through a polling scheme. This mode is designed to control multiple peripheral devices on a system. The Local Area Network mode is designed for high-speed transmissions in a network environment, using two different channels of access.

A full range of design support tools is planned to aid in developing NCR/32-based systems. In addition, experienced NCR applications engineers can assist in determining the suitability of the NCR/32 family for solving applications problems. These engineers can provide extensive training on the NCR/32 systems architecture, individual chips, and the use of design support tools.



NCR/32-000
CENTRAL PROCESSOR CHIP (CPC)

- True 32-bit internal/external architecture
- Externally microprogrammable
- Two independent external data paths
  - 32-bit Processor-Memory Bus (PM Bus)
  - 16-bit Instruction Storage Unit Bus (Microinstruction ISU Bus)
- Sixteen 32-bit true general purpose registers (RSU)
- 32-bit ALU
  - Nibble (digit), byte, halfword, word, and field (string) data types
  - Decimal, binary, and boolean operations
- 3-stage microinstruction pipeline
- 179 microinstructions and variants with register to register format
- 95% of instructions execute in one clock cycle
- 8 addressable 16-bit microinstruction jump registers
- Addressing Range
  - 4 Gigabytes of direct virtual memory
  - 16 Megabytes of direct real memory
  - 128 Kilobytes of direct microinstruction memory
- 3 main memory scratch pad pointers
- Special logic for opcode cracking in virtual machine applications
- NMOS silicon gate technology

The NCR/32-000 CPC mainframe-type architecture and high operating speed have been possible only with the use of an efficient chip design and state-of-the-art technology.

The ALU has been located in the center of the chip in order to efficiently interface to three internal 32-bit busses. The Control ROM (CROM) containing the internal CPC microcode has been partitioned to place the Control ROM output lines as close as possible to their associated control logic. All other functional areas of the chip have been similarly placed to minimize chip area and bus lengths, thereby reducing die cost and increasing device performance.

The CPC incorporates high-density silicon gate NMOS and Silicide technologies to further decrease die area and significantly increase performance.

The NCR 32-000 Central Processor Chip (CPC) combines the latest advances in semiconductor technology with experience gained during three generations of computer mainframe design to provide a comprehensive, microprogrammable, true 32-bit microprocessor. With external microprogram capability, an extremely flexible microinstruction set, and a powerful set of internal registers, the NCR/32-000 offers flexibility and high performance advantages not available with other microprocessors.

Along with an existing set of VLSI family support devices, the NCR/32-000 CPC offers effective emulation of register, stack and descriptor-based system architectures, as well as execution of high-level languages directly from microcode. The NCR/32-000 is well suited for applications requiring direct addressing of a large memory space, high numeric precision, and very-high-speed execution such as bit-mapped graphics and relational data bases.

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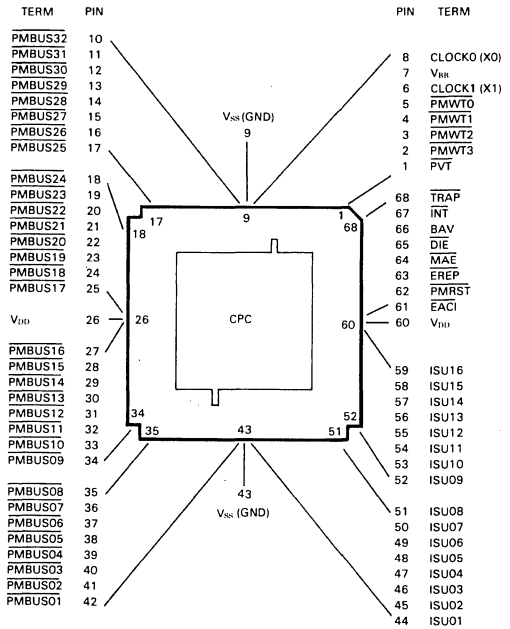
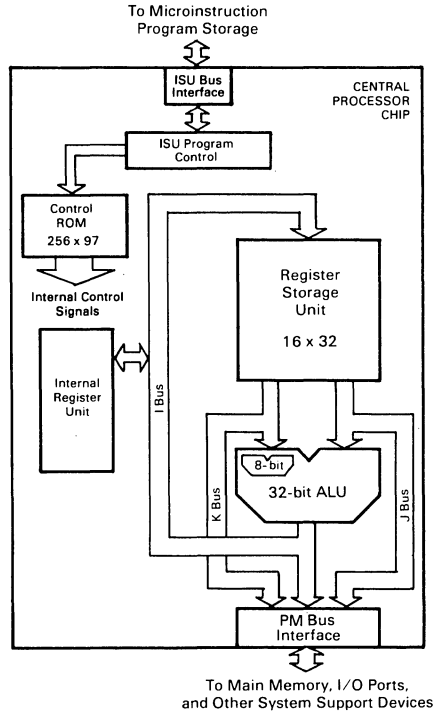
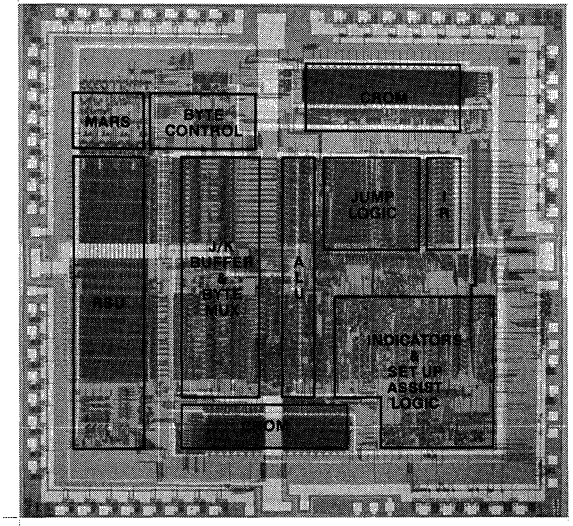
PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



NCR/32-000 CHIP DESIGN



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to 7.0	V
Input Voltage	V_{IN}	-1.0 to 7.0	V
Input Voltage Clock	V_{INC}	-1.0 to 7.0	V
Substrate Bias Voltage	V_{BB}	-7.0 to 0.5	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature	T_{STG}	-55 to 155	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance (Ceramic Flat-Pack)	Θ_{JA}	15	°C/W

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0Vdc ± 5%, V_{SS} = OV, V_{BB} = -2.5Vdc ± 10%, T_A = 0°C to 70°C)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	VDD	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Input High Voltage Clock	V_{IHC}	$.9V_{DD}$	6.0	V
Input Low Voltage Clock	V_{ILC}	-1.0	0.4	V
Output High Voltage @ 400 μA (ISU Bus)	V_{OH}	2.4		V
Output Low Voltage @ 8 mA	V_{OL}		0.5	V
Leakage Current (V_{SS} to V_{DD}) Non-Clock Pins Three-State (Offstate) Current (V_{SS} to V_{DD}) ISU16-01	I_{TS}	-10	10	μA
Supply Current	I_{DD}		400	mA
Substrate Bias Current	I_{BB}		1.0	mA
Power Dissipation @ 6.67 MHz	P_D		3.0	W
Capacitance (non-clock pins)	C		20	pF
Leakage Current (V_{SS} to V_{DD}) clock pins	I_{LC}	-100	100	μA
Capacitance, Clock 0	C0		200	pF
Capacitance, Clock 1	C1		200	pF

CPC TIMING PARAMETERS

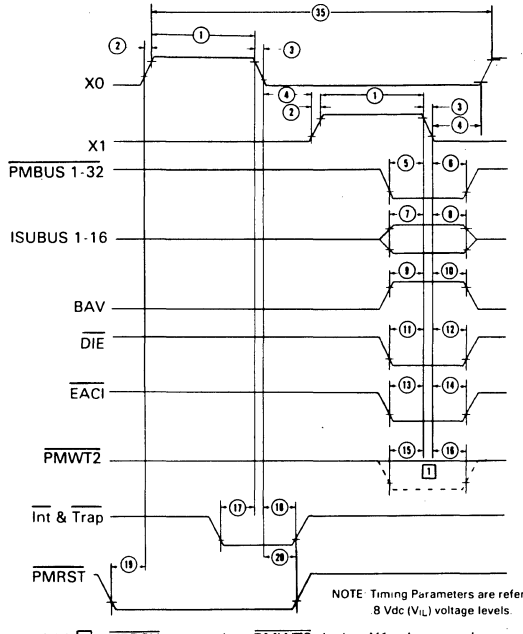
NUMBER	Parameter	Symbol	150 ηSec Min	150 ηSec Max	Unit
1	Clock Width High	t_{CH}	40	500	ηS
2	Clock Rise Time	t_{CR}		10	ηS
3	Clock Fall Time	t_{CF}		10	ηS
4	Clock Separation	t_{CS}	15	100	ηS
5	PM Bus Input Data Setup Time	t_{IDS}	20		ηS
6	PM Bus Input Data Hold Time	t_{IDH}	0		ηS
7	ISU Bus Data Setup Time	t_{DS}	15		ηS
8	ISU Bus Data Hold Time	t_{DH}	5		ηS
9	Bus Available Setup Time	t_{BAVS}	15		ηS
10	Bus Available Hold Time	t_{BAVH}	5		ηS
11	Data Input Enable Setup Time	t_{DIES}	15		ηS
12	Data Input Enable Hold Time	t_{DIEH}	5		ηS
13	EAC Setup Time	t_{EACS}	25		ηS
14	$\overline{EAC}$ Hold Time	t_{EACH}	10		ηS
15	$\overline{VPBSY}$ Setup Time	t_{BSYS}	15		ηS
16	$\overline{VPBSY}$ Hold Time	t_{BSYH}	5		ηS
17	Interrupt/Trap Setup Time	t_{INTS}	15		ηS
18	Interrupt/Trap Hold Time	t_{INTH}	5		ηS
19	PM Bus Reset Setup Time	t_{RSTS}	25		ηS
20	PM Bus Reset Hold Time	t_{RSTH}	10		ηS
21	PM Bus Address Delay	t_{PMAD}		25	ηS
22	PM Bus Address Hold Time	t_{PMAH}	5	20	ηS
23	PM Bus Output Data Delay	t_{ODD}		25	ηS
24	PM Bus Output Data Hold Time	t_{ODH}	5	20	ηS
25	ISU Bus Address Delay	t_{AD}		15	ηS
26	ISU Bus Address Hold Time	t_{AH}	5	20	ηS
27	Byte Write Tags Delay	t_{WTD}		15	ηS
28	Byte Write Tags Hold Time	t_{WTH}	5	20	ηS
29	Processor Virtual Transfer Delay	t_{PVTD}		15	ηS
30	Processor Virtual Transfer Hold Time	t_{PVTH}	5	20	ηS
31	Mem Address Enable, Ext Register Enable/Permit Delay	t_{MAED}		15	ηS
32	Mem Address Enable, Ext Register Enable/Permit Hold Time	t_{MAEH}	5	20	ηS
33	$\overline{BKPTWE}$, $\overline{BKPTE}$, $\overline{BCT}$ Delay Time	t_{BCTD}		15	ηS
34	$\overline{BKPTWE}$, $\overline{BKPTE}$, $\overline{BCT}$ Hold Time	t_{BCTH}	5	20	ηS
35	Clock Period	t_{CYC}	150		ηS

(V_{DD} = 5.0 Vdc + 5%, V_{SS} = 0 Vdc, V_{BB} = -2.5 Vdc ± 10%, T_A = 0°C to 70°C)
NOTE: THE TEST LOAD IS A 680Ω PULL UP RESISTOR AND 50pF CAPACITANCE

This is advance information and NCR reserves the right to change the specifications without notice.

NCR

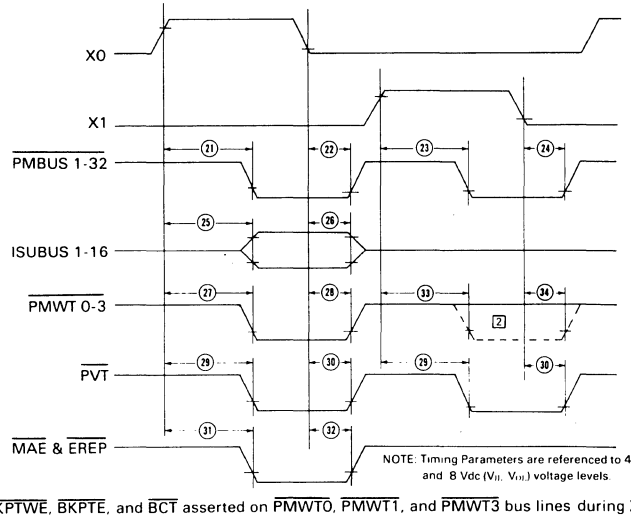
CPC INPUT TIMING DIAGRAM



NOTE: Timing Parameters are referenced to 4.5 Vdc (V_{IH}) and .8 Vdc (V_{IL}) voltage levels.

NOTE [1]: VPBSY asserted on PMWT2 during X1 when used.

CPC OUTPUT TIMING DIAGRAM



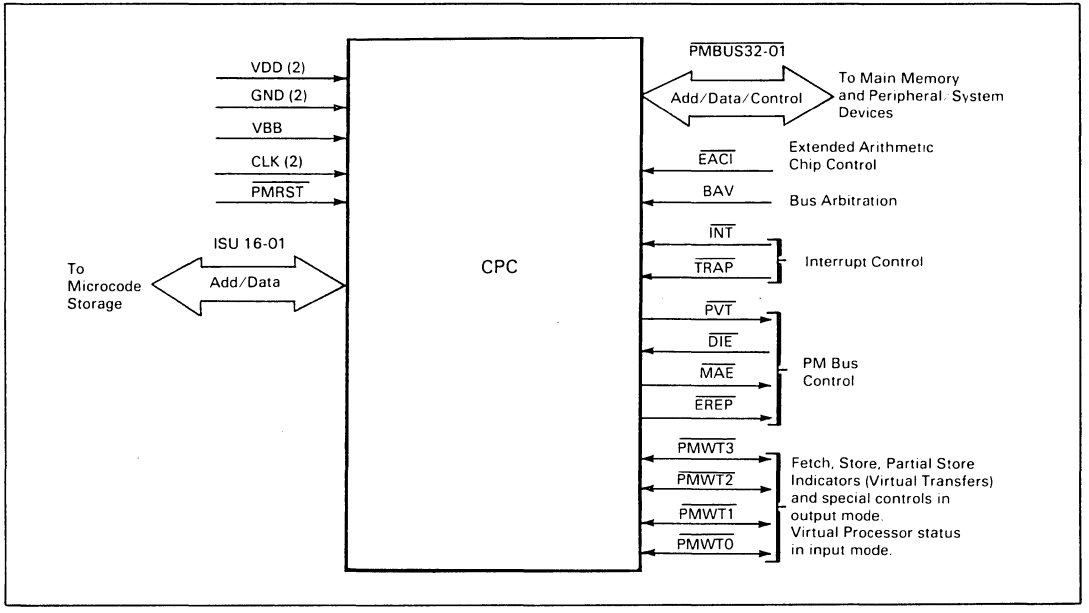
NOTE: Timing Parameters are referenced to 4.5 Vdc (V_{IH}, V_{IH}) and .8 Vdc (V_{IL}, V_{IL}) voltage levels.

NOTE [2]: BKPTWE, BKPTE, and BCT asserted on PMWT0, PMWT1, and PMWT3 bus lines during X1 when used.

SIGNAL DESCRIPTION

The CPC input and output signals can be organized into groups as shown below. A description of each CPC signal or signal group and a summary of the signals are contained in the following tables.

INPUT AND OUTPUT SIGNALS



SIGNAL DESCRIPTION

Pin	Signal	Description
1	$\overline{PVT}$	Processor Virtual Transfer — This active low signal is asserted by the processor during the initial X0 clock phase of all virtual memory operations. This signal is also asserted by the processor during the X1 clock phase of all processor-generated memory operations; that is, for all processor generated PM bus operations with the exception of ERU transfers.
2-5	$\overline{PMWT3}$- $\overline{PMWT0}$	Processor to Memory Write Tags 0-3 — These active low signals are asserted during the X0 interval that $\overline{PVT}$ is asserted by the processor. They indicate which bytes are to be written into memory during a virtual transfer. $\overline{PMWT3}$ corresponds to memory byte 3, etc. All Write Tags inactive implies a Fetch operation. During the X1 clock phase, these signals have other definitions as follows: $\overline{BCT}$ (Between Commands Testing) — This processor output is asserted on the $\overline{PMWT3}$ pin during every X1 clock phase. It is enabled by the BCT bit of Control Array #1 in the processor. If the BCT bit is set to a 1, then $\overline{PMWT3}$ will be low during each X1. $\overline{VPBSY}$ (Virtual Processor Busy) — The input $\overline{VPBSY}$ is monitored on the $\overline{PMWT2}$ pin during the X1 clock phase when the JRPX and JRMX instructions are in the interpret stage of the CPC pipeline. $\overline{BKPTE}$ (Breakpoint Enable) — During the X1 clock phase, this signal is asserted on $\overline{PMWT1}$. It is intended to be used to represent the data bit (breakpoint set/reset) to be loaded into an optional off-chip breakpoint RAM if the signal $\overline{BKPTWE}$ enables modification of the addressed breakpoint. This signal is enabled by the DJOR and RTI instructions. $\overline{BKPTWE}$ (Breakpoint Write Enable) — This signal is asserted during the X1 clock phase on the $\overline{PMWT0}$ pin. It is intended to be used as the write enable control for an optional off-chip breakpoint RAM. When this signal is active, it permits the breakpoint RAM to be modified as directed by the $\overline{BKPTE}$ signal. This signal is enabled with the DJOR and RTI instructions.
6 8	X1 X0	CLOCK1 (X1) phase input. CLOCK0 (X0) phase input. The processor uses two externally-supplied, 2-phase, non-overlapping clocks to control all internal operations. These free-running clocks are X0, the first phase clock, and X1, the second phase clock.
7	VBB	Negative voltage supply
9, 43	VSS	Ground.
10-25 27-42	$\overline{PMBUS32}$- $\overline{PMBUS01}$	Processor Memory Bus — This active low, open drain, time-shared bus is the connecting data/address path between the processor and the other NCR/32-000 family chips and main memory. ERU addresses are transferred from the processor over the PM bus during X0. Memory addresses are transferred from the processor during X0. ERU and memory data is transferred to/from the processor during X1.
44-59	ISU01- ISU16	Instruction Storage Unit Bus — This is an active high, tri-state bus which links the processor to its ISU memory. During the X0 phase of each clock cycle, the processor outputs an address onto this bus. At the end of the X1 clock phase of the same clock cycle, the processor latches the contents of this bus into its Instruction Register. This is the microcode instruction or literal stored at the addressed ISU location.
26, 60	VDD	Positive voltage supply
61	$\overline{EACI}$	Extended Arithmetic Chip Information — This is a status input to the CPC from the EAC. Assertion of this signal clears the EAC Busy bit in the Indicator Array to indicate that the EAC has completed an operation.
62	$\overline{PMRST}$	PM Bus Reset — This asynchronous active low reset signal is asserted by the system external reset logic. $\overline{PMRST}$ is used within the CPC to initialize the processor control logic.
63	$\overline{EREP}$	External Register Enable/Permit — This active low processor output is asserted by the processor during X0 to initiate an ERU transfer.

NOTE: Signals with bars are active-low-true signals.

SIGNAL DESCRIPTION (Cont.)

Pin	Signal	Description
64	$\overline{\text{MAE}}$	Memory Address Enable — This active low signal is asserted by the processor during the initial X0 clock interval of real memory address transfers initiated by the processor via the PM bus.
65	$\overline{\text{DIE}}$	Data Input Enable — This active low signal is monitored by the processor at the end of all X1 times following the initiation of a memory fetch sequence to synchronize the processor pipeline to the availability of memory data on the PM bus. If $\overline{\text{DIE}}$ is asserted during X1 and meets the required setup and hold times, the processor unlocks the pipeline and latches the data that is asserted on the PM bus the following X1 clock.
66	BAV	Bus Available — This is an input to the processor and its assertion indicates that the PM bus will be free for the processor to use during the next clock cycle. For processor instructions which do not require the PM bus, this signal is ignored. For instructions which require the use or availability of the PM bus, the processor will halt until it is informed by BAV that it may use the bus in the next cycle.
67	$\overline{\text{INT}}$	Interrupt — The processor monitors the $\overline{\text{INT}}$ signal at the end of all X0 intervals to determine whether an interrupt is being sourced to the processor.
68	$\overline{\text{TRAP}}$	Trap — The processor monitors the $\overline{\text{TRAP}}$ signal at the end of all X0 intervals to determine whether a trap is being sourced to the processor.

NOTE: Signals with bars are active-low-true signals.

SIGNAL SUMMARY

Signal Name	Pin #	Symbol	Input/Output	Active State	Drive
Processor Virtual Transfer	1	$\overline{\text{PVT}}$	Output	Low	Open Drain
Processor-Memory Write Tag	2,3,4,5	$\overline{\text{PMWT3-0}}$	Input/Output	Low	Open Drain
Clock 1	6	X1	Input	High	Input
Power Input (Negative Voltage)	7	VBB	Input	—	—
Clock 0	8	X0	Input	High	Input
Ground	9,43	VSS	Input	—	—
Processor-Memory Bus	10-25, 27-42	$\overline{\text{PMBUS32-01}}$	Input/Output	Low	Open Drain
Instruction Storage Unit Bus	44-59	ISU01-16	Input/Output	High	3-State
Power Input (Positive Voltage)	26, 60	VDD	Input	—	—
Extended Arithmetic Chip Information	61	$\overline{\text{EACI}}$	Input	Low	Input
Processor-Memory Reset	62	$\overline{\text{PMRST}}$	Input	Low	Input
External Register Enable/Permit	63	$\overline{\text{EREP}}$	Output	Low	Open Drain
Memory Address Enable	64	$\overline{\text{MAE}}$	Output	Low	Open Drain
Data Input Enable	65	$\overline{\text{DIE}}$	Input	Low	Input
Bus Available	66	BAV	Input	High	Input
Interrupt	67	$\overline{\text{INT}}$	Input	Low	Input
Trap	68	$\overline{\text{TRAP}}$	Input	Low	Input

MEMORY

The NCR/32-000 CPC accesses two separate memory arrays. One is the Instruction Storage Unit (ISU) and the other is Main Memory.

ISU MEMORY

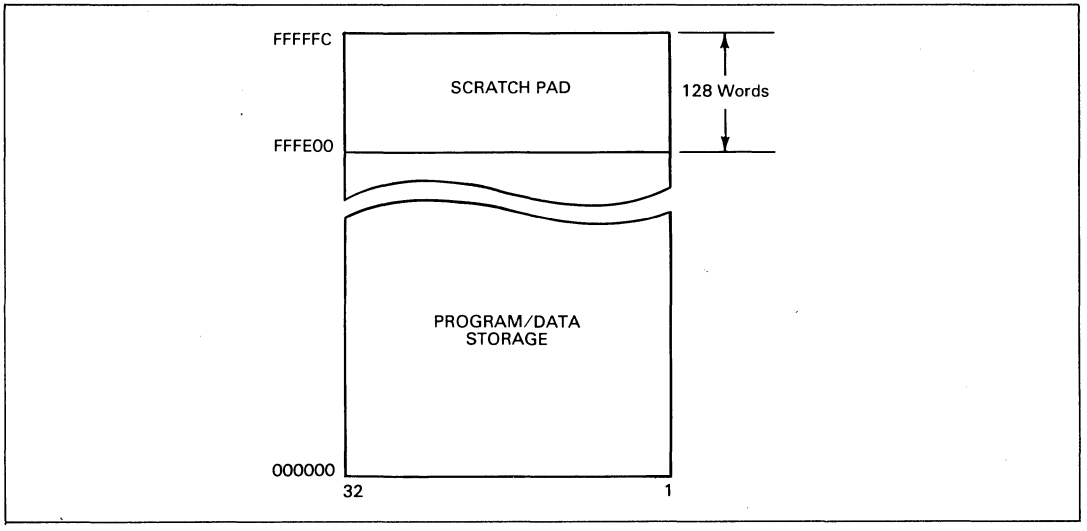
The CPC accesses ISU memory through a 16-bit multiplexed ISU bus. The ISU memory contains the external CPC microinstruction programs.

MAIN MEMORY

The CPC accesses main memory through a 32-bit multiplexed PM bus. During read operations (Fetch-Receive instruction sequence), an entire 32-bit word is read from memory and written into a designated RSU location. During store operations, an entire word or part of a word (individual bits) is written into a Main Memory location or into an external register.

The upper 128 words of Main Memory is designated Scratch Pad memory. Special instructions allow the NCR/32-000 CPC fast access to this area of Main Memory, significantly increasing CPC throughput. Scratch Pad access is real rather than virtual and is identified on the PM bus by an asserted $\overline{\text{PMBUS32}}$.

MAIN MEMORY ORGANIZATION



PM BUS

The CPC transfers data to/from main memory and offboard external registers (ERUs) via the PM Bus. The PM Bus consists of 32 active-low, multiplexed address/data lines and associated control lines.

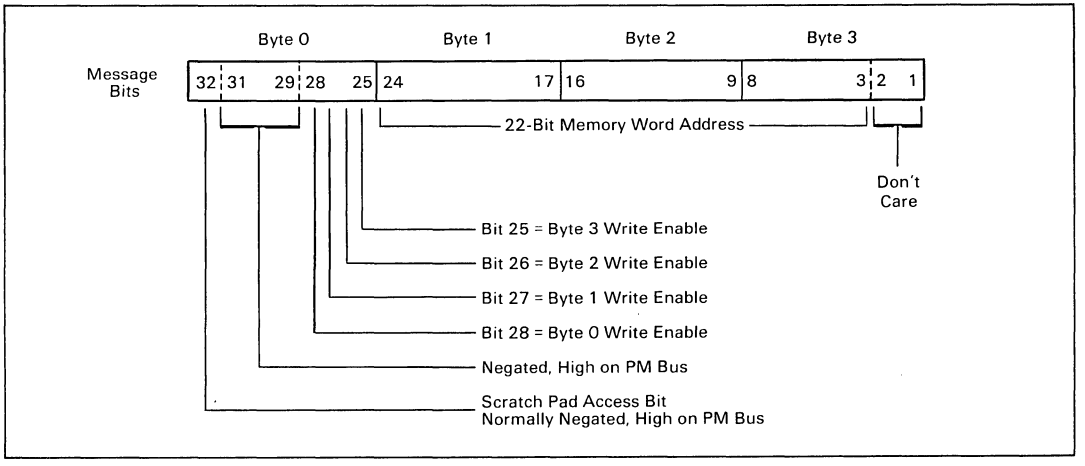
The CPC transfers data over the PM Bus using three types of memory/register accesses: Real, Virtual, and ERU. Real accesses are direct accesses in which no address translation takes place. Virtual accesses are indirect accesses requiring an extra bus cycle during which a memory management device, such as the NCR/32-010 Address Translation Chip (ATC), translates the CPC virtual address into a new real address. ERU accesses are a form of Real access used by the CPC to access external registers. The CPC initiates a memory/register access by asserting a message containing an address and either (1) byte write and scratch pad access information, (2) memory access protection check codes, or (3) a direction of data transfer bit, during X0. Both message format and PM Bus definition differ for each type of message.

REAL MEMORY DATA TRANSFERS

There are three types of CPC Real Memory Data transfers: Real Fetch, Real Full Store, and Real Partial Store. The CPC reads an entire data word during a Real Fetch operation; writes an entire word into memory during a Full Store operation; and writes one, two, or three bytes into a memory word location during a Real Partial Store operation.

The real address is presented to the memory interface without translation. The Byte Write Enables identify to the system the type of real memory message initiated (Fetch, Full Store, or Partial Store), where an asserted Byte Write Enable (low on bus) indicates a write to the appropriate byte in the addressed word, and no asserted Byte Write Enable indicates a fetch. Bit 32 is asserted only when special CPC scratch pad access commands are executed.

REAL MESSAGE FORMAT



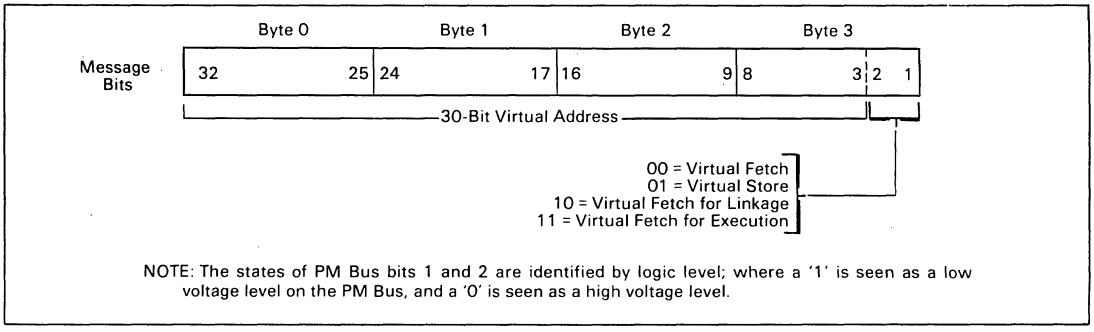
VIRTUAL MEMORY DATA TRANSFERS

Virtual Memory Data transfers are essentially Real Memory Data transfers (as seen by the memory interface) preceded by an extra bus cycle during which a virtual address from the CPC is translated into a real address by the ATC. There are, therefore, three types of Virtual Memory Data transfers, analogous to the Real Memory Data transfers: Virtual Fetch, Virtual Full Store, and Virtual Partial Store.

The Virtual Message format is shown below. The message consists of a 30-bit virtual address, and a 2-bit field containing a memory access Protection Check Code which identifies for the ATC the type of memory operation being executed.

Byte read/write information is asserted by the CPC on the $\overline{\text{PMWT0-3}}$ bus lines during the first X0 clock of Virtual Message transfers. During virtual transfers, these lines serve the same function as the Byte Write Enable bits contained in real messages.

VIRTUAL MEMORY MESSAGE FORMAT



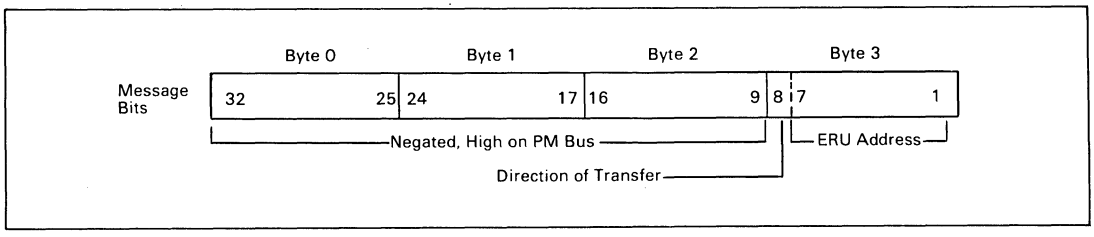
NOTE: The states of PM Bus bits 1 and 2 are identified by logic level; where a '1' is seen as a low voltage level on the PM Bus, and a '0' is seen as a high voltage level.

EXTERNAL REGISTER DATA TRANSFERS

The CPC can address and transfer data to/from as many as 96 external registers using the TIE (Transfer In External) and TOE (Transfer Out External) instructions. Some of these registers are internal to the ATC, and some are pseudo registers used to access scratch pad memory. Register addresses not accessing ATC registers or scratch pad access pseudo registers are either not used or are reserved for future NCR/32 Family devices. The system designer is free to implement these "unused" addresses in custom designs.

The ERU message format is illustrated below. ERU message bits 9-32 are not used, bit 8 determines the direction of data transfer (read or write), and bits 1-7 are the ERU address.

EXTERNAL REGISTER MESSAGE FORMAT



THREE-STAGE PIPELINE

The NCR/32-000 executes microinstructions utilizing a three-stage pipeline consisting of a fetch stage, an interpret stage, and an execute stage.

In the fetch stage a microinstruction in the ISU memory is addressed by the CPC Control Register (CR), a program counter, then read from ISU memory and written into the CPC Instruction Register (IR). The CR and IR are not directly accessible by the user.

In the interpret stage the microinstruction currently in the Instruction Register is decoded to set up the controls used during the instruction execution and to read out the operands from the Register Storage Unit (RSU) which will be used during the instruction execution.

In the execute stage the operands are processed according to the instruction. Information is routed internally throughout the CPC and externally over the PM Bus. Results are written back into an RSU as required.

ARITHMETIC LOGIC UNIT (ALU)

The NCR/32-000 ALU performs binary operations on words and bytes, decimal arithmetic operations on bytes, logical functions on words, bytes, and nibbles, and shift operations on words.

Binary arithmetic operations include Add, Subtract, and Compare. Decimal operations include Add and Subtract. Logical operations include AND, OR, Exclusive OR, and Invert. Shift operations include single-bit Shift Right and Shift Left.

INTERNAL REGISTERS

The NCR/32-000 has two sets of registers available to the user: the Register Storage Unit (RSU) and the Internal Register Unit (IRU). The Register Storage Unit consists of sixteen 32-bit registers that are used for data and address storage and manipulation. The Internal Register Unit consists of twenty-two special registers used for status information, jump addresses, field byte count information (Tally Register), and special set-up for virtual machine emulation.

NCR

REGISTER STORAGE UNIT (RSU)

The RSU consists of sixteen 32-bit registers. Most non-literal instruction operands are read from the RSU during the pipeline Interpret phase of instruction processing. Results of an operation are written back into the RSU during the Execution phase.

RSU CHARACTERISTICS

RSU#	Transfers W	HW	B[1]	D	MARS Function	Memory Access WF	WS	BS	Protection Checks R	W	L	E	Field Usage
0	X	X	X	X	MARS0 Addr.	X	X	X	X	X	X		
1	X	X	X	X	MARS0 Data	X	X	X	X	X	X		
2	X	X	X	X	MARS1 Addr.	X	X	X	X	X	X		
3	X	X	X	X	MARS1 Data	X	X	X	X	X	X		
4	X	X			MARS2 Addr.	X	X	X	X	X	X		
5	X	X			MARS2 Data	X	X	X	X	X	X		
6	X	X			MARS3 Addr.	X	X	X	X	X	X		
7	X	X			MARS3 Data	X	X	X	X	X	X		
8	X	X			MARS4 Addr.	X	X	X	X	X	X		Operand
9	X	X	X		MARS4 Data	X	X	X	X	X	X		Fetch
10	X	X			MARS5 Addr.	X	X	X	X	X	X		Operand
11	X	X	X		MARS5 Data	X	X	X	X	X	X		Fetch
12	X	X			MARS6 Addr.	X	X	X	X	X	X		Operand
13	X	X	X		MARS6 Data	X	X	X	X	X	X		Store
14	X	X			MARS7 Addr.	X	X	X				X	V Cont. Reg.
15	X	X	X		MARS7 Data	X	X	X				X	V Inst. Reg.

B = Byte
D = Digit (Nibble)
HW = Halfword
W = Word
WF = Word Fetch
WS = Word Store
BS = Byte Store
R = Read
W = Write
L = Linkage
E = Execute

NOTES:
1. Byte transfers to/from RSU 9, 11, 13, and 15 are during field instructions only.
2. 32-bit words can be fetched from main memory and placed into any of the RSU locations as specified by the J-field and K-field of the microinstruction. Full or partial word stores can be used to place data into main memory from any RSU location.
3. During virtual transfers, the two least-significant bits of the PM bus ($\overline{\text{PMBUS02}}$ and $\overline{01}$) are used for the memory access Protection Check Code.

INTERNAL REGISTER UNIT (IRU)

The IRU consists of twenty-two internal CPC registers which are accessed by the Transfer Out Internal (TOI) and Transfer In Internal (TII) instructions at address locations 00-1F (hexadecimal).

INTERNAL REGISTER (IRU) ADDRESS ASSIGNMENTS

7-Bit Address Decimal	7-Bit Address Hexa-decimal	Function	Transfer Instruction
00-07	00-07	Jump Registers	
08	08	Restore FIFO	
09	09	State Register	
10	0A	① Setup Register #3	
11	0B	Setup Register #4	
12	0C	Tally Register	
13-15	0D-0F	Not used	
16	10	Indicator Array	
17	11	Virtual Indicator Array	TII
18	12	Setup Register #5	and
19	13	Setup Register #1	TOI
20	14	Setup Register #2	
21-23	15-17	Not used	
24	18	② Operand Pointers #1 & #2	
25	19	Not used	
26	1A	Stack Pointer	
27	1B	Control Array #1	
28	1C	MARS6 Write Tags	
29-31	1D-1F	Not used	

NOTES: ① 16-bit right-justified registers. A TII (Transfer In Internal) instruction does not affect the left half of the destination RSU.
② 16-bit left-justified registers. A TII from one of these registers does not affect the right half of the destination RSU.

EXTERNAL REGISTERS

The CPC can access up to 96 external registers called ERUs.

ERUs 32-38 are pseudo registers which are used to access the scratch pad area of main memory. ERUs 40-55 are registers internal to the ATC. ERUs 56-63 are reserved for future NCR/32 Family peripheral devices. ERUs 64-127 are reserved for user I/O applications. ERU 39 is not used.

Scratch pad accesses using pseudo registers 32-38 are real memory transfers. All other ERU accesses are fast, single-cycle data transfers identified on the PM Bus by the assertion of $\overline{\text{EREP}}$.

EXTERNAL REGISTER (ERU) ADDRESS ASSIGNMENTS

7-Bit Address Decimal	7-Bit Address Hexa-decimal	Function		Transfer Instruction
32	20	Operand Data 1	Indirect Scratch Pad Reference	
33	21	Operand Data 1 Inc.		
34	22	Operand Data 1 Dec.		
35	23	Operand Data 2		
36	24	Operand Data 2 Inc.		
37	25	Operand Data 2 Dec.		
38	26	Stack Data		
39	27	Not used		TIE
40	28	Control Array #2	ATC Registers	and
41	29	Interrupt/Trap Array		TOE
42	2A	Interrupt Mask		
43	2B	Interval Monitor		
44	2C	Time of Day		
45	2D	Address Monitor		
46	2E	BIN Register		
47-55	2F-37	Associative Memory Functions		
56-63	38-3F	Reserved for Future Use		
64-127	40-7F	User I/O		TIP & TOP

SCRATCH PAD ACCESS

Various sections of scratch pad can be accessed using the Operand Pointers, the Stack Pointer, and the FL and SL instructions.

The Operand Pointers and Stack Pointer scratch pad accesses are through ERU pseudo registers 32-38.

Scratch pad accesses via these pseudo registers are real memory transfers on the PM Bus. As such, the transfers are formatted as Real Memory data transfers and not ERU transfers. $\overline{\text{EREP}}$ is not asserted (low) as with transfers to/from other ERU locations.

A TIE from scratch pad triggers a real memory read operation. Because of this, the RCV instruction must be used to receive the data.

INTERRUPTS AND TRAPS

The normal program flow of instructions within the processor may be exited when program traps or program interrupts occur. Traps are normally considered conditions that, upon detection, must be serviced immediately. Interrupts are normally considered conditions that, upon detection, may be serviced immediately, may be serviced at a later time, or may be masked out altogether.

INTERRUPT/TRAP RECOGNITION

The trap line ($\overline{\text{TRAP}}$) and the interrupt line ($\overline{\text{INT}}$) are external inputs to the processor. When $\overline{\text{TRAP}}$ is asserted (low) and the Trap Indicator bit (bit 11) in Control Array #1 (CA1) is clear (a trap is not currently being processed), the microinstruction Control Register is written with the trap address 0000. An immediate jump to the trap routine occurs. The Trap Indicator bit is set, but the Normal Interrupt Enable bit (CA1, bit 10) is not affected. The instruction in the Execute stage of the pipeline is executed, but the instructions in the Fetch and Interpret stages of the pipeline are not executed. The pipeline is advanced one cycle and halted.

When the interrupt line is asserted (low) and the Trap Indicator bit in Control Array #1 is clear and the Normal Interupt Enable bit is set (an interrupt is not currently being processed), the microinstruction Control Register is written with the interrupt address 0002 if the instruction being interpreted is not non-interruptible. An immediate jump to the interrupt routine occurs, and the Normal Interrupt Enable bit is cleared. If both an interrupt and trap occur simultaneously, the trap is serviced first.

INTERRUPT/TRAP SERVICING

Servicing of traps and interrupts is a function of both CPC logic and firmware.

CPC logic forces the program jump to the trap or interrupt address, clears Normal Interrupt Enable or sets the Trap Indicator, and disables the clocking of the Restore FIFO.

Firmware must transfer in external interrupt status and test each condition to determine which caused the interrupt or trap in systems allowing multiple traps and interrupts. Firmware must also determine the priorities of the interrupt and trap conditions in the event that multiple interrupts have occurred.

SAVING THE MACHINE STATE

At times it may become necessary to save the state of the processor when a trap or interrupt occurs that prevents a timely completion of a software routine, typically in a time-share application. State saving requires that internal and external registers pertinent to a recovery of the current task be saved in the scratch pad or some other reserved section of main memory. The restore FIFO must be read (three successive Transfers In from IRU08) and saved, thereby saving the ISU addresses of the three instructions in the pipeline at the time the interrupt or trap was taken. Control Array #1 and other essential status states must also be read and saved.

RESTORING FROM INTERRUPTS/TRAPS

The Restore from Traps and Interrupts (RTI) instruction is used to control the restore sequence. RTI injects an instruction address saved in the restore FIFO into the internal microinstruction Control Register. By executing three consecutive RTI instructions, the pipeline is restored to the pre-interrupt/trap state.

If an interrupt or trap is pending at the time the third RTI is executed, the Restore FIFO is not restarted. The Trap Indicator is cleared by the RTI, but then immediately set if a trap is pending; Normal Interrupt Enable is set by the RTI, but then immediately cleared if an interrupt is pending.

SETUP ASSIST

The NCR/32-000 features special logic associated with Setup Registers 1-5 designed to support virtual machine applications. This logic allows execution of special setup instructions and map indicator instructions used in the emulation of the IBM 370 and NCR-VRX/NVM virtual machines. While specifically designed for these virtual machines, the CPC setup features (setup registers and instructions) may be used in the emulation of other machines.

These setup features assist in cracking virtual op codes, loading virtual pointers into the Operand Pointers or the Stack Pointer, isolating literal fields in virtual instructions, and creating jump vectors for entering additional firmware setup routines and command execution routines.

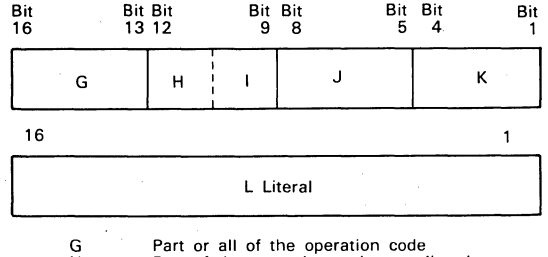
The map indicator instructions map various indicators in the processor Indicator Array into the corresponding bits of the Virtual Indicators Array according to the virtual machine being emulated.

INSTRUCTION SET

The instruction set executed by the CPC utilizes and provides the following important features:

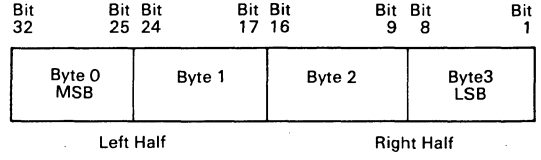
- Sixteen 32-bit General Purpose Registers in the Register Storage Unit (RSU)
- 32-bit (fullword) and 16-bit (halfword) instructions
- Digit, byte, halfword, and fullword instructions
- Digit, byte, and word arithmetic functions
- Field instructions employing MARS (Memory Assist Register Sets) units
- Eight instruction-addressable subroutine jump registers
- Special setup instructions to assist in the emulation of existing NCR mainframe and IBM/370 instruction sets
- 4 gigabyte external virtual address capability, 16 megabyte physical (real) memory addressing

INSTRUCTION AND OPERAND FORMATS



G — Part or all of the operation code
H — Part of the operation code or a literal
I — Part of the operation code or a literal or part of the address field for ERU and scratch pad memory.
J — RSU/MARS, Jump Register addressing or a literal
K — RSU/MARS addressing or a literal
L — Jump literal address or an RSU load literal

Primitive Instruction Format



Operand Format

NCR Microelectronics Division
1635 Aeroplaza Drive
Colorado Springs, Colorado 80916
Telex: 452-457
Phone: 303/596-5612
800/525-2252

NCR/32-010
ADDRESS TRANSLATION CHIP (ATC)

- **NCR/32-000 compatibility**
- **Memory management with dual four-level memory access protection**
- **Three types of memory operations**
  - **— Virtual**
  - **— Real**
  - **— Refresh (main memory)**
- **Error check and correction, and syndrome bit generation**
- **Time-of-day counter, and time interval monitoring**
- **Virtual address monitoring for breakpoint and trace functions**
- **1K, 2K, and 4K byte page options**

The NCR/32-010 ATC incorporates state-of the art VLSI technology coupled with an efficient chip design to provide a powerful set of features in a high-speed chip not possible until now.

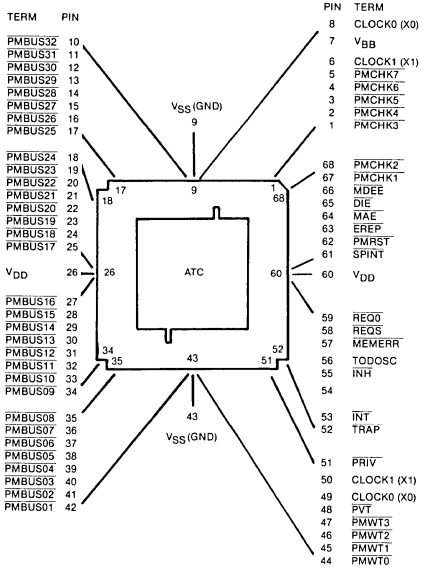
The ATC incorporates high-density silicon gate NMOS and Silicide technologies for reduced die size and high-speed operation. Functional areas of the chip have been located to minimize internal chip bus lengths and interface logic.

These technologies and design efforts have resulted in the powerful performance necessary for a 32 bit NCR/32 Family device.

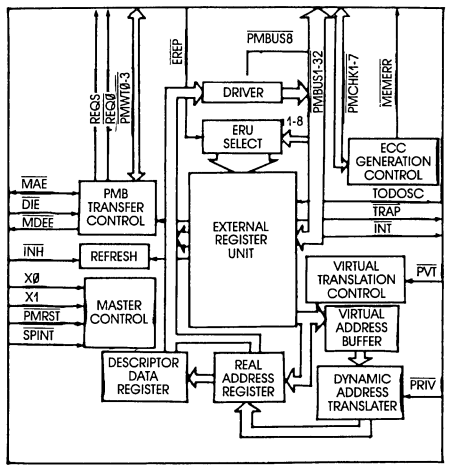
The NCR/32-010 Address Translation Chip (ATC) is an NMOS, 32-bit memory management unit that features system memory management, data error detection and correction, memory refresh, and supervisor/user isolation with four-level access protection. In addition, the ATC provides virtual address translation for memory fetches, full stores, and partial stores, allowing direct processor access to a 4-Gigabyte address space.

The ATC can be interfaced to the NCR/32-000 Central Processor Chip to form a general-purpose controller and virtual machine emulator. Other NCR/32 Family devices are available which, when interfaced to the ATC and CPC, form a powerful yet flexible processor system that is well-suited for a wide variety of applications considered beyond the capability of microprocessor systems until now.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



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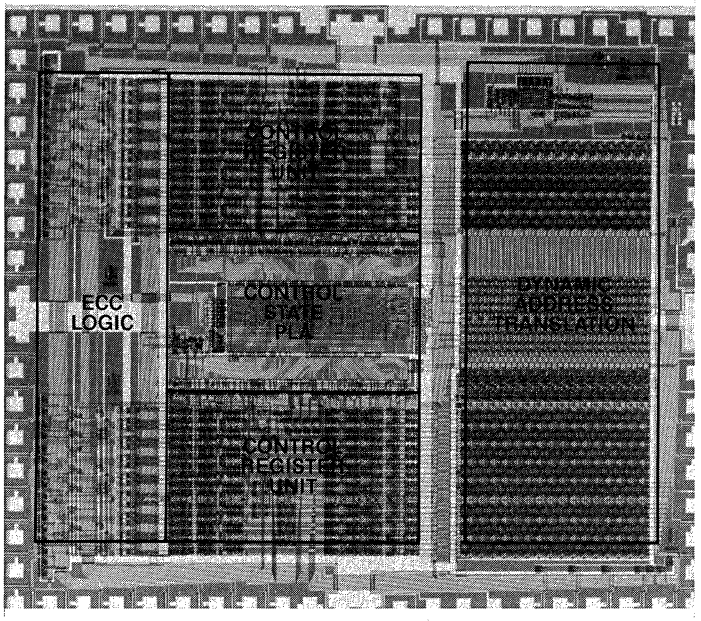
NCR/32-010 CHIP DESIGN



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to 7.0	V
Input Voltage	V_{IN}	-1.0 to 7.0	V
Input Voltage Clock	V_{INC}	-1.0 to 7.0	V
Substrate Bias Voltage	V_{BB}	-7.0 to 0.5	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature	T_{STG}	-55 to 155	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance (Ceramic Flat-Pack)	Θ_{JA}	15	°C/W

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0 Vdc ± 5%, V_{SS} = OV, V_{BB} = −2.5Vdc ± 10%, T_A = 0°C to 70°C)

Characteristic	Symbol	Min.	Max.	Unit
Input High Voltage	V_{IH}	2.3	5.25	V
Input Low Voltage	V_{IL}	−0.1	0.8	V
Input High Voltage Clock	V_{IHC}	4.2	5.25	V
Input Low Voltage Clock	V_{ILC}	−0.1	0.4	V
Output High Voltage @ 200 μA (SP REQ)	V_{OH}	2.4		V
Output Low Voltage @ 8 mA*	V_{OL}		0.5	V
Leakage Current (V_{SS} to V_{DD}), Non-Clock Pins	I_L	−100	100	μA
Leakage Current (V_{SS} to V_{DD}), Clock Pins	I_{LC}	−500	100	μA
Supply Current	I_{DD}		550	mA
Substrate Bias Current	I_{BB}		1.0	mA
Power Dissipation @ 6.67 MHz	P_D		3.0	W
Capacitance, Non-Clock Pins	C		20	pF
Capacitance, Clock Pins	Cc		100	pF

*@ 2mA FOR SPECIAL REQUEST

This is advance information and NCR reserves the right to change the specifications without notice.

ATC INPUT TIMING PARAMETERS

NUMBER	Parameter	Symbol	150nS(1) Min	150nS(1) Max	180nS(2) Min	180nS(2) Max	Unit
1.	Clock Width High	t_{CH}	50		60		nS
2.	Clock Rise Time	t_{CR}		10		10	nS
3.	Clock Fall Time	t_{CF}		10		10	nS
4.	Clock Separation	t_{CS}	15	100	10	100	nS
5.	PM Bus Input Message Setup Time	t_{PMIMS}	18		18		nS
6.	PM Bus Input Message Hold Time	t_{PMIMH}	3		3		nS
7.	PM Bus X1 Input Data Setup Time	t_{XIDS}	18		25		nS
8.	PM Bus X1 Input Data Hold Time	t_{XIDH}	3		3		nS
9.	PM Bus X0 Input Data Setup Time	t_{XODS}	25		32		nS
10.	PM Bus X0 Input Data Hold Time	t_{XODH}	3		3		nS
11.	Byte Write Tags Setup Time	t_{WTS}	22		25		nS
12.	Byte Write Tags Hold Time	t_{WTH}	3		3		nS
13.	PM Bus Check Input Setup Time	t_{CHKIS}	25		25		nS
14.	PM Bus Check Input Hold Time	t_{CHKIN}	3		3		nS
15.	Processor Virtual Transfer X0 Setup Time	t_{PVTSO}	22		22		nS
16.	Processor Virtual Transfer X0 Hold Time	t_{PVTHO}	3		3		nS
17.	Processor Virtual Transfer X1 Setup Time	t_{PVTSI}	15		15		nS
18.	Processor Virtual Transfer X1 Hold Time	t_{PVTHI}	0		0		nS
19.	Special Interrupt Setup Time	t_{SINTS}	20		20		nS
20.	Special Interrupt Hold Time	t_{SINTH}	3		3		nS
21.	Inhibit Setup Time	t_{INHS}	15		15		nS
22.	Inhibit Hold Time	t_{INHH}	3		3		nS
23.	Privilege X0 Setup Time	t_{PRVSO}	15		15		nS
24.	Privilege X0 Hold Time	t_{PRVHO}	3		3		nS
25.	Privilege X1 Setup Time	t_{PRVSI}	15		15		nS
26.	Privilege X1 Hold Time	t_{PRVHI}	3		3		nS
27.	External Register Enable/Permit Setup Time	t_{ERS}	18		18		nS
28.	External Register Enable/Permit Hold Time	t_{ERH}	3		3		nS
29.	Memory Address Enable Setup Time	t_{MAES}	22		24		nS
30.	Memory Address Enable Hold Time	t_{MAEH}	3		3		nS
31.	Data Input Enable Setup Time	t_{DIES}	20		20		nS
32.	Data Input Enable Hold Time	t_{DIEH}	3		3		nS
33.	Tme of Day Oscillator Setup Time	t_{TODS}	20		20		nS
34.	Time of Day Oscillator Hold Time	t_{TODH}	3		3		nS
35.	Clock Period	t_{CTL}	150		180		nS

(1) NCR/32-010*5 (2) NCR/32-010*8

(V_{DD} = 5.0 Vdc ±5%, V_{SS} = 0V, V_{BB} = −2.5 Vdc ± 10%, T_A = 0°C to 70°C)
Test load is a 680 Ω pull-up resistor and 50 pF capacitance

ATC OUTPUT TIMING PARAMETERS

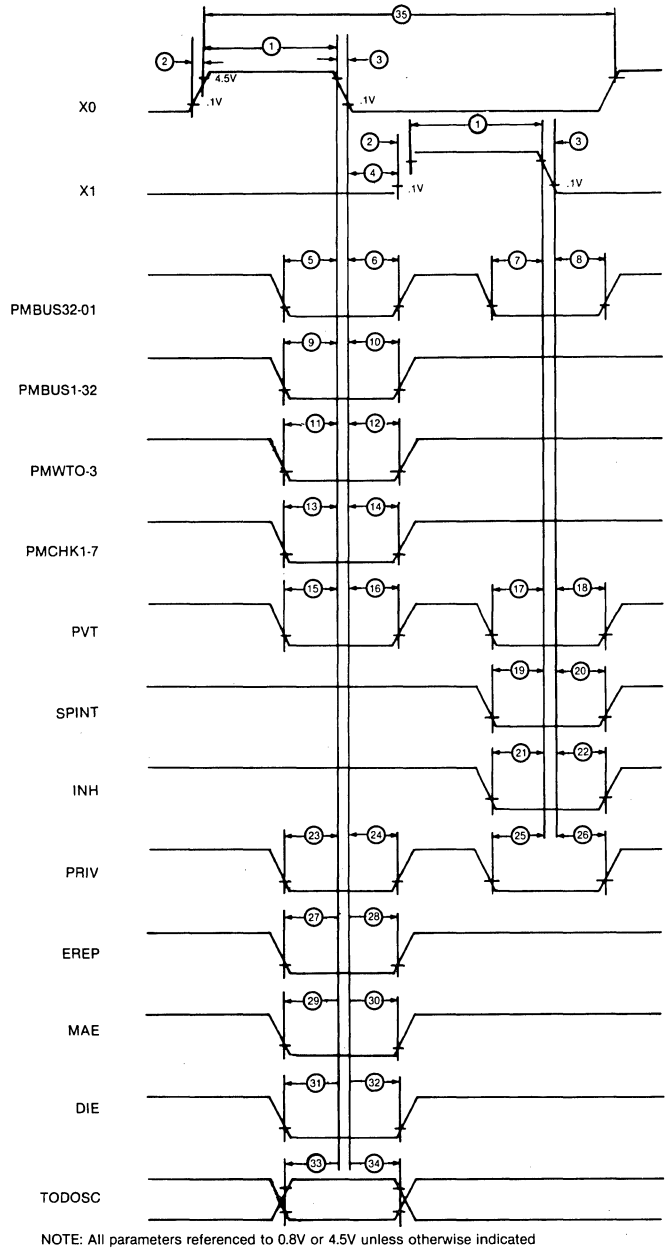
NUMBER	Parameter	Symbol	150nS(1) Min	150nS(1) Max	180nS(2) Min	180nS(2) Max	Unit
36.	PMS Bus X0 Output Delay Time	t_{PMXOD}		25		25	nS
37.	PM Bux X0 Output Hold Time	t_{PMXOH}	5	15	5	15	nS
38.	PM Bus X1 Output Delay Time	t_{PMXID}		25		25	nS
39.	PM Bus X1 Output Hold Time	t_{PMXIH}	5	15	5	15	nS
40.	Memory Data Delay Time	t_{MOD}		38		43	nS
41.	Memory Data Hold Time	t_{MOH}	5	15	5	15	nS
42.	Memory Address Enable Delay Time	t_{MAED}		15		15	nS
43.	Memory Address Enable Hold Time	t_{MAEH}	5	20	5	20	nS
44.	External Register Enable/Permit Delay Time	t_{ERPD}		20		20	nS
45.	External Register Enable/Permit Hold Time	t_{ERPH}	5	20	5	20	nS
46.	Memory Data Enable/Error Delay Time	t_{MDED}		30		30	nS
47.	Memory Data Enable/Error Hold Time	t_{MDEH}	5	20	5	20	nS
48.	Memory Error Delay Time	t_{MED}		30		30	nS
49.	Memory Error Hold Time	t_{MEH}	5	20	5	20	nS
50.	Interrupt Delay Time	t_{INTD}		30		30	nS
51.	Interrupt Hold Time	t_{INTH}	5	20	5	20	nS
52.	Trap Delay Time	t_{TRPD}		30		30	nS
53.	Trap Hold Time	t_{TRPH}	5	20	5	20	nS
54.	PM Bus Request 0 Delay Time	t_{RQOD}		25		25	nS
55.	PM Bus Request 0 Hold Time	t_{RQOH}	5	20	5	20	nS
56.	PM Bus Special Request Delay Time (ATC Command)	t_{ARQD}		49		54	nS
57.	PM Bus Special Request Hold Time (ATC Command)	t_{ARQH}	5	20	5	20	nS
58.	PM Bus Special Delay Time (Mem Error)	t_{MRQD}		56		61	nS
59.	PM Bus Special Request Hold Time (Mem Error)	t_{MRQH}	5	20	5	20	nS
60.	PM Bus Check Bit Delay Time	t_{CHKD}		49		49	nS
61.	PM Bus Check Bit Hold Time	t_{CHKH}	5	38	5	38	nS

(1) NCR/32-010*5 (2) NCR/32-010*8

(V_{DD} = 5.0 Vdc ±5%, V_{SS} = 0V, V_{BB} = −2.5 Vdc ± 10%, T_A = 0°C to 70°C)
Test load is a 680 Ω pull-up resistor and 50 pF capacitance

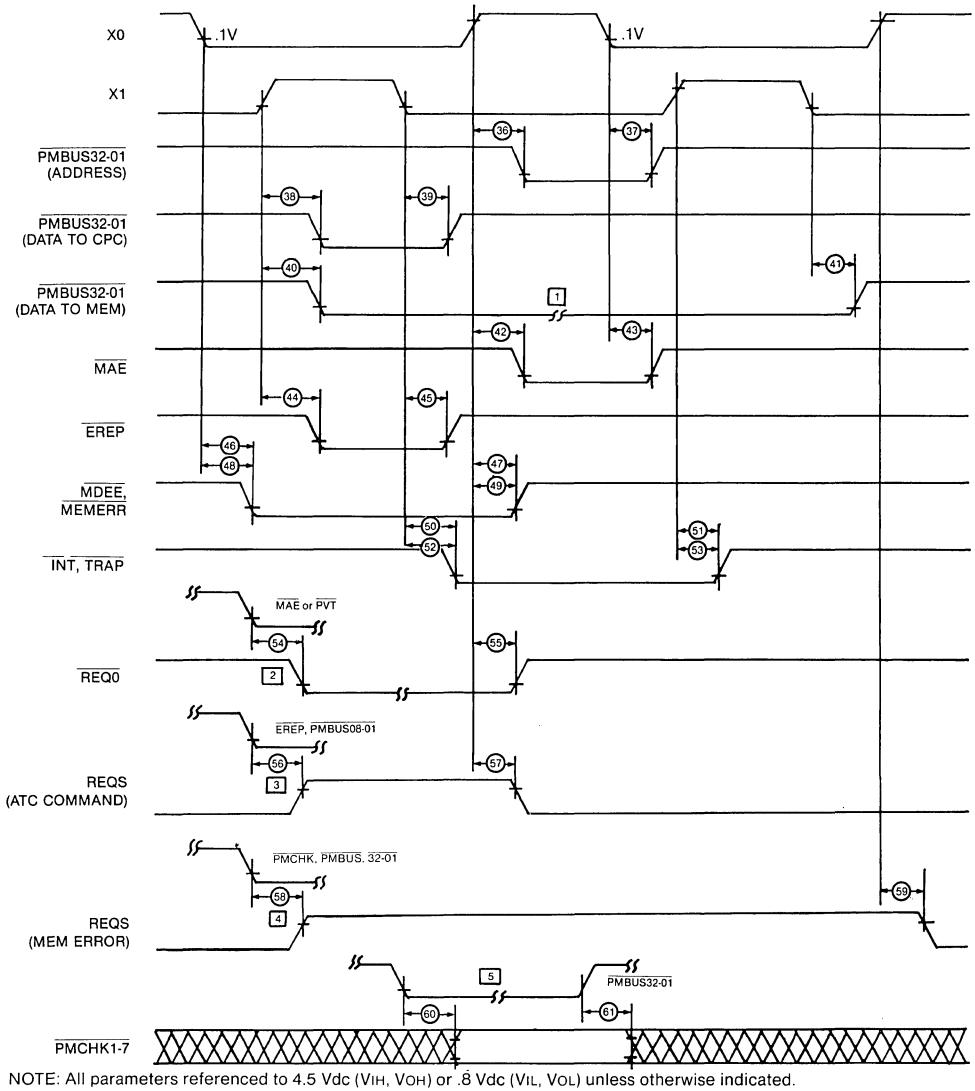
This is advance information and NCR reserves the right to change the specifications without notice.

ATC INPUT TIMING DIAGRAM



NOTE: All parameters referenced to 0.8V or 4.5V unless otherwise indicated

ATC OUTPUT TIMING-DIAGRAM



NOTE: All parameters referenced to 4.5 Vdc (V_{IH}, V_{OH}) or .8 Vdc (V_{IL}, V_{OL}) unless otherwise indicated.

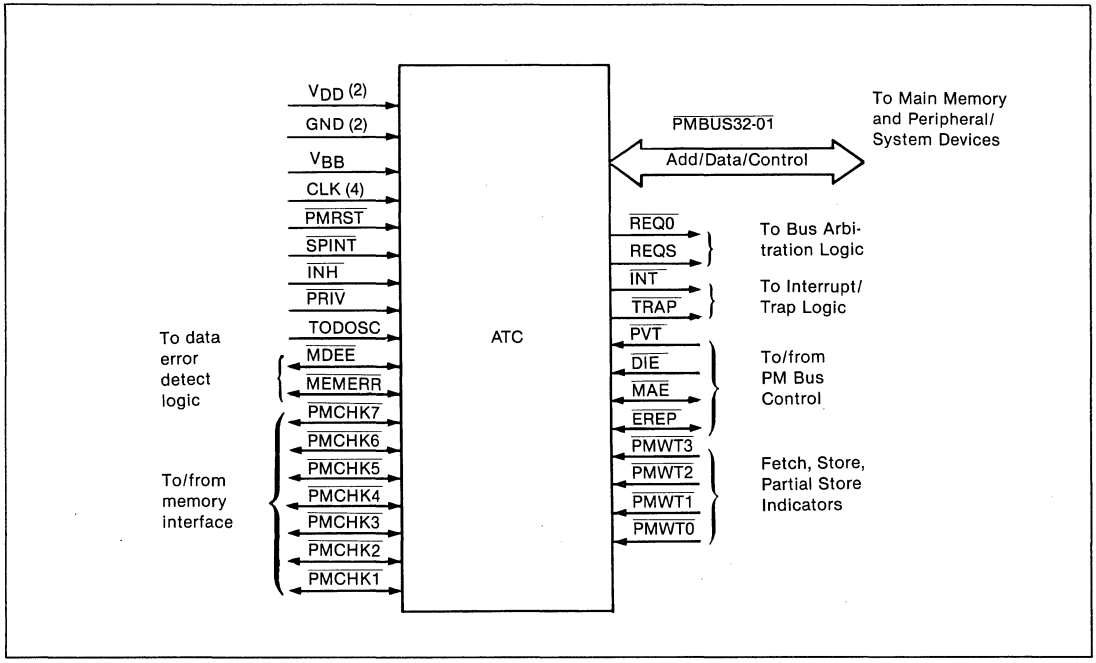
NOTES:
1. A write to memory may require several bus cycles, pending assertion of $\overline{DIE}$.
2. $\overline{REQ0}$ is asserted in response to $\overline{MAE}$ or $\overline{PVT}$ assertion during X0 when required by an ATC operation. $\overline{REQ0}$ may be asserted several cycles by the ATC depending on the operation.
3. REQS is asserted during CPC execution of several commands in response to $\overline{EREP}$ and $\overline{PMBUS08\text{-}01}$ assertion during X0. Assertion of REQS is referenced to last signal, $\overline{EREP}$ or $\overline{PMBUS08\text{-}01}$, which is asserted.
4. REQS is asserted in response to $\overline{PMCHK1\text{-}7}$ and $\overline{PMBUS32\text{-}01}$ data assertion during X0 when an uncorrectable memory error is detected by the ATC. Assertion of REQS is referenced to last signal, $\overline{PMCHK1\text{-}7}$ or $\overline{PMBUS32\text{-}01}$, which is asserted.
5. While the ECC function is enabled, the ATC generates syndrome bits at all times. The ECC treats all assertion on the PM Bus as data requiring syndrome bit generation.

NCR

SIGNAL DESCRIPTION

The ATC input and output signals can be organized into groups as shown below. A description of each ATC signal or signal group and a summary of the signals are contained in the following tables.

INPUT AND OUTPUT SIGNALS



PIN #	Symbol	Description
10-25 27-42	PMBUS32-01	Processor Memory Bus — These multiplexed bus lines are used to transfer information between devices. In general, address information is transferred to a destination device during X0, and data is transferred to/from a destination device during X1. However, all address and data transfers between the ATC and memory occur during X0.
8, 49	X0	Phase 0 input clock
6, 50	X1	Phase 1 input clock
62	PMRST	PM Bus Reset — This input, when asserted, holds the ATC in a reset state.
61	SPINT	Special Interrupt — This input is sampled by the ATC during X1. The ATC responds to an asserted SPINT by setting bit 12 (Special Interrupt) of the I/T Array and asserting INT if the interrupt is not masked in the Interrupt Mask Register. SPINT is normally tied to the system low-voltage/power-fail detection circuit.

Continued on next page.

PIN #	Symbol	Description
63	$\overline{\text{EREP}}$	External Register Enable/Permit — When this input is asserted during X0, the ATC decodes the External Register Unit number from the address lines to determine if one of the ATC External Register Units (registers) is being addressed.
64	$\overline{\text{MAE}}$	Memory Address Enable — This input, when asserted, indicates that a device has initiated a real memory operation. If the operation is a fetch, the ATC reads and checks the data for errors during the X0 that $\overline{\text{DIE}}$ is asserted following the assertion of $\overline{\text{MAE}}$, and asserts the checked data on the PM Bus the following X1 for reading by the requesting device. The ATC is forced to execute multiple fetches/corrections by the assertion of $\overline{\text{MAE}}$ and $\overline{\text{DIE}}$ during X0 clocks, and remains in the fetch/correct state until $\overline{\text{MAE}}$ is no longer asserted with $\overline{\text{DIE}}$ during X0. The ATC asserts $\overline{\text{MAE}}$ when it asserts a real address on the PM Bus after address translation in response to a virtual memory message; that is, the ATC asserts $\overline{\text{MAE}}$ and a real address on the PM Bus during X0 if $\overline{\text{PVT}}$ was asserted the previous X0, indicating a virtual memory operation.
48	$\overline{\text{PVT}}$	Processor Virtual Transfer — The ATC initiates a virtual memory operation when this input signal is asserted low during X0. If Control Array bit 9 (Virtual Equals Real) is clear, the ATC translates the message virtual address. If Control Array bit 9 is set, the ATC asserts the untranslated message address on the PM Bus the following X0.
44-47	$\overline{\text{PMWT0-3}}$	Processor Memory Write Tags 0-3 — The ATC monitors these inputs during virtual memory operations to determine which bytes in the addressed word are to be written. These signals are equivalent to the Byte Write Enable signals in real memory messages. If all of the write tags are negated, a fetch is indicated. If one or more are asserted, a corresponding byte(s) is written. $\overline{\text{PMWT0}}$ corresponds to byte 0, $\overline{\text{PMWT3}}$ corresponds to byte 3, etc.
67, 68 1-5	$\overline{\text{PMCHK7-1}}$	PM Check 7-1 — These bidirectional lines are used for syndrome bit (ECC) transfer between the ATC and memory. These signals are asserted by the ATC during store operations, and by the memory during fetch operations.
65	$\overline{\text{DIE}}$	Data Input Enable — This signal is asserted by the system Memory Interface during X0 and X1 to indicate that memory data is to be asserted on the PM Bus as part of a fetch, partial store, or refresh operation: or that the Memory Interface is ready to accept data.
66	$\overline{\text{MDEE}}$	Memory Data/Enable Error — The ATC asserts this signal during the X1 clock that it detects an uncorrectable (multiple bit) memory error during a fetch or partial store operation.
57	$\overline{\text{MEMERR}}$	Memory Error — The ATC asserts this signal during X1 in response to a correctable (single bit) or non-correctable (multiple bit) error detected during a partial store, fetch, or refresh operation.
59	$\overline{\text{REQ0}}$	Request 0 — The ATC asserts $\overline{\text{REQ0}}$ to gain access to the PM Bus the following PM Bus cycle. $\overline{\text{REQ0}}$ is the highest priority system request. When the ATC asserts $\overline{\text{REQ0}}$, it takes control of the PM Bus the following cycle without further handshaking. The system bus arbitration logic must force other devices off the PM Bus at this time. The ATC may continue asserting $\overline{\text{REQ0}}$ for several consecutive cycles to complete an operation.

Continued on next page.

PIN #	Symbol	Description
58	REQS	Special Request — The ATC asserts this line high to give the CPC immediate access to the PM Bus. While REQS remains asserted, the system bus arbitration logic must ignore all other bus requests, and de-select all other devices. Uncorrectable memory errors require immediate CPC intervention before other data transfers occur. When the ATC detects an uncorrectable data error, it asserts REQS until the CPC has serviced the error condition, indicated by CPC clearing of the trap bit in the ATC I/T Array. Three ATC associative commands force the ATC to assert REQS: the Purge Selective (PS) command, the Purge Selective With Mask (PSM) command, and the Translate Virtual Address (TVA) command. The ATC asserts REQS for one cycle in response to these commands. ATC memory refresh operation is inhibited while REQS is asserted.
53	$\overline{INT}$	Interrupt — The ATC asserts $\overline{INT}$ when any bit in the I/T Array other than a trap bit is set. The ATC negates $\overline{INT}$ when the bit forcing the interrupt is cleared, if no other interrupts are pending. $\overline{INT}$ assertion is inhibited during X1.
52	$\overline{TRAP}$	Trap — The ATC asserts $\overline{TRAP}$ when any trap bit in the I/T Array is set. The ATC negates $\overline{TRAP}$ when the bit forcing the trap is cleared, if no other traps are pending. Traps cannot be masked. $\overline{TRAP}$ assertion is inhibited during X1.
56	TODOSC	Time of Day Oscillator — This input is driven by a free-running 250 KHz external oscillator, and is used to drive the TOD (Time Of Day) Counter/Register in the ATC. The frequency of this input affects the memory refresh rate.
55	$\overline{INH}$	Inhibit — This input, when asserted low, inhibits ATC refresh operation to allow system expansion.
51	$\overline{PRIV}$	Privilege Mode — $\overline{PRIV}$ is an input used to set/reset the Privilege Flag, bit 1, in the Control Array. $\overline{PRIV}$ must first be asserted during X0. If $\overline{PRIV}$ is asserted the following X1, the Privilege Flag is set; if $\overline{PRIV}$ is negated the following X1, the Privilege Flag is cleared.
7	V_{BB}	Negative voltage supply
9, 43	V_{SS}	Ground
26, 60	V_{DD}	Positive Voltage Supply
54	NC	No Connection (not used)

Barred terms are active low.

SIGNAL SUMMARY

Signal Name	Pin #	Symbol	Input/Output	Active State	Drive
Processor-Memory Bus	10-25 27-42	$\overline{\text{PMBUS32-01}}$	Input/Output	Low	Open Drain
Clock 0	8, 49	X0	Input	High	Input
Clock 1	6, 50	X1	Input	High	Input
PM Bus Reset	62	$\overline{\text{PMRST}}$	Input	Low	Input
Special Interrupt	61	$\overline{\text{SPINT}}$	Input	Low	Input
External Reg. Enable/Permit	63	$\overline{\text{EREP}}$	Input/Output	Low	Open Drain
Memory Address Enable	64	$\overline{\text{MAE}}$	Input/Output	Low	Open Drain
Processor Virtual Transfer	48	$\overline{\text{PVT}}$	Input	Low	Input
Processor Write Tags	44-47	$\overline{\text{PMWTO-3}}$	Input	Low	Input
Processor Memory Check Bits	5-1 68, 67	$\overline{\text{PMCHK7-1}}$	Input/Output	Low	Open Drain
Data Input Enable	65	$\overline{\text{DIE}}$	Input	Low	Input
Memory Data Enable/Error	66	$\overline{\text{MDEE}}$	Input/Output	Low	Open Drain
Memory Error	57	$\overline{\text{MEMERR}}$	Output	Low	Open Drain
PM Bus Request "0"	59	$\overline{\text{REQ0}}$	Output	Low	Open Drain
Special Request	58	REQS	Output	High	Push-Pull
Interrupt	53	$\overline{\text{INT}}$	Output	Low	Open Drain
Trap	52	$\overline{\text{TRAP}}$	Output	Low	Open Drain
Time-of-Day Osc.	56	TODOSC	Input	High	Input
Inhibit	55	$\overline{\text{INH}}$	Input	Low	Input
Privilege Mode	51	$\overline{\text{PRIV}}$	Input	Low	Input
Power Supply (Pos)	26, 60	V_{DD}	Input	—	—
Power Supply (Neg)	7	V_{BB}	Input	—	—
Ground	9, 43	V_{SS}	Input	—	—

PM BUS AND PM CHECK BUS

The PM Bus is a 32 bit, open drain, multiplexed (address and data) bus which interfaces the ATC to other bus masters and to memory in a system. The ATC receives three types of messages via the PM Bus: control messages called External Register Unit (ERU) messages, real messages which the ATC "passes" unaltered, and virtual messages which the ATC, when so programmed, translates into real messages. Messages are address and control information asserted by a bus master during the X0 clock interval. Operations initiated by these messages are called External Register Data Transfers, Real Memory Data Transfers, and Virtual Memory Data Transfers.

The PM Check Bus ($\overline{\text{PMCHK1-7}}$) is an open drain bus tied to the system memory or memory interface that is used by the ATC to assert and read seven syndrome bits associated with each work in memory. These syndrome bits are generated by the ATC Error Correction Code (ECC) logic and stored with each word in memory to maintain memory data integrity. The ATC "intercepts" all data to be stored into memory by a bus master, steals a system cycle during which it generates syndrome bits for the data, then stores the data word and the associated syndrome bits into memory when the memory is ready for the data — indicated by the assertion of $\overline{\text{DIE}}$. When a bus master fetches data from memory, the ATC "intercepts" the data and its associated syndrome bits, generates new syndrome bits of the data word, and compares the new syndrome bits with the syndrome bits that were stored with the data word. Using this comparison the ATC detects and corrects single bit errors, and detects all double bit errors.

The ATC is designed to interface directly with the NCR/32-000 Central Processor Chip. Although the ATC can be designed into systems utilizing other processors, system timing in systems utilizing the ATC must be identical to CPC-ATC system timing.

REAL MEMORY DATA TRANSFERS

There are three types of CPC Real Memory Data Transfers: Real Fetch, Real Full Store, and Real Partial Store. The CPC reads an entire data word during a Real Fetch operation; writes an entire word into memory during a Full Store operation; and writes one, two, or three bytes into a memory word location during a Real Partial Store operation.

The real address is presented to the memory interface by the ATC without translation. The Byte Write Enables identify to the ATC the type of real memory message initiated (Fetch, Full Store, or Partial Store), where an asserted Byte Write Enable (low on bus) indicates a write to the appropriate byte in the addressed word, and no asserted Byte Write Enable indicates a fetch. Bit 32 is asserted only when CPC scratch pad accesses are executed.

VIRTUAL MEMORY DATA TRANSFERS

Virtual memory data transfers are essentially real memory data transfers (as seen by the memory interface) preceeded by an extra bus cycle during which a virtual address from the CPC is translated into a real address by the ATC. There are, therefore, three types of virtual memory data transfers, analogous to the real memory data transfers: Virtual Fetch, Virtual Full Store, and Virtual Partial Store.

Byte read/write information is asserted by the CPC on the $\overline{\text{PMWT0-3}}$ bus lines during the first X0 clock of Virtual Message transfers. During virtual transfers, these lines serve the same function as the Byte Write Enable bits contained in real messages.

The ATC can operate on either 24 bit or 32 bit virtual addresses, determined by the state of bit 5 in the Control Array (CA5). The ATC determines that a virtual operation is being initiated when the $\overline{\text{PVT}}$ (Processor Virtual Transfer) line is asserted during X0, at which time a virtual address is asserted by the CPC onto the PM Bus. The ATC strobes the address into its Virtual Address Register Buffer and starts the translation process. If the translation is not successful, the ATC asserts DAT (Dynamic Address Translation) No Match Interrupt. If the translation is successful and protection check is enabled by a clear bit 6 in the Control array, the ATC protection bits associated with the virtual address are checked according to the operation indicated by the states of bits 2 and 1 of the virtual message as follows:

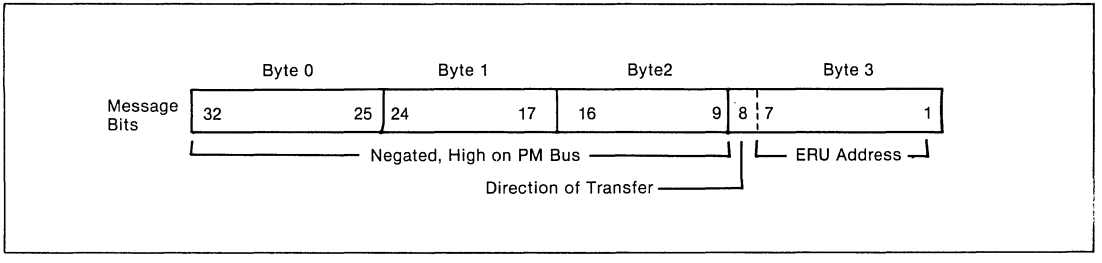
BIT# 2 1
- 0 0 Virtual Fetch
- 0 1 Virtual Store
- 1 0 Virtual Fetch for Linkage
- 1 1 Virtual Fetch for Execution

If there is an access violation, the ATC asserts a DAT Access Violation interrupt. Otherwise the ATC latches the translated real address into the Real Address register and continues with the operation.

EXTERNAL REGISTER DATA TRANSFERS

The CPC can address and transfer data to/from the ATC internal registers using External Register Unit (ERU) messages addressed to the ATC. The ERU message format is shown below. ERU message bits 9-32 are not used, bit 8 determines the direction of data transfer (read or write), and bits 1-7 are the ERU address.

EXTERNAL REGISTER UNIT MESSAGE FORMAT



MEMORY REFRESH

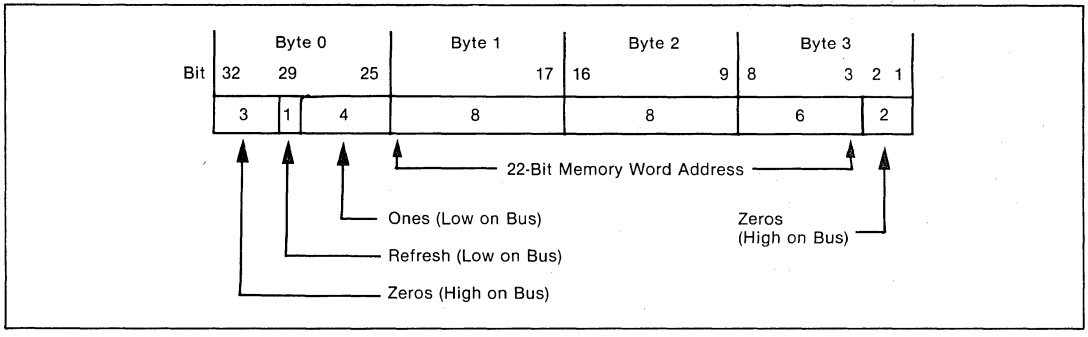
The ATC can be programmed to periodically refresh system main memory (memory accessed via the PM Bus) automatically. An internal 32-bit counter, the Time Of Day (TOD) Register/Counter, is used by the ATC to determine the memory refresh interval and period, and to store the incrementing refresh address.

The TOD counter is externally clocked via the TODOSC pin. If a 250 KHz (4us) clock is used to drive the TOD, the ATC will refresh a row of memory approximately every 16 microseconds. Thus the entire memory (256 rows) is refreshed approximately every 1.048 seconds.

The memory refresh message format is shown below. Refresh operations are essentially real memory operations identified by the assertion of $\overline{\text{PMBUS29}}$ on the PM Bus during message transfer. The refresh address, bits 3-24 of the message, is the value of the TOD bits 3-24 at the time of the refresh. The memory interface must identify the operation as a memory refresh by the assertion of $\overline{\text{PMBUS29}}$, must use the lower 8 bits of the refresh address $\overline{\text{PMBUS3-10}}$ as the RAS term, and the upper 14 bits ($\overline{\text{PMBUS11-24}}$) as the CAS term. $\overline{\text{PMBUS25-28}}$, the Byte Write Enable signals, are asserted during the message transfer.

During each refresh operation the ATC reads one addressed memory and its associated syndrome bits and checks the word for errors. The ATC then writes the work and its syndrome bits back into memory unaltered if it detected no error, writes the corrected word and new syndrome bits back into memory if it detected a single bit error, and aborts the operation if it detected an uncorrectable error. In this way each word in memory is "scrubbed" of errors periodically.

REFRESH MESSAGE FORMAT



ERROR CHECK CORRECTION AND SYNDROME BIT GENERATION (ECC)

Associated with each word in memory are seven syndrome bits used by the ATC to verify the integrity of the data word. The syndrome bits are generated by the ATC Error Check and Correction logic (ECC) during each memory store operation, are asserted on the $\overline{\text{PMCHK1-7}}$ bus lines, and are stored into memory along with the data word. During subsequent ATC memory fetch operations, the seven syndrome bits associated with the fetched data are read and used by the ATC to detect and correct single-bit errors in the fetched data or its associated syndrome bits, and to detect some multiple-bit errors.

The ECC circuit consists of random logic which operates on the PM Bus at all times. ECC operation is disabled by setting bit 7 in the ATC Control Array (CA7 = 1); ECC syndrome bit generation is inhibited by use of the ATC Syndrome Register, accessed only during ATC diagnostic operations.

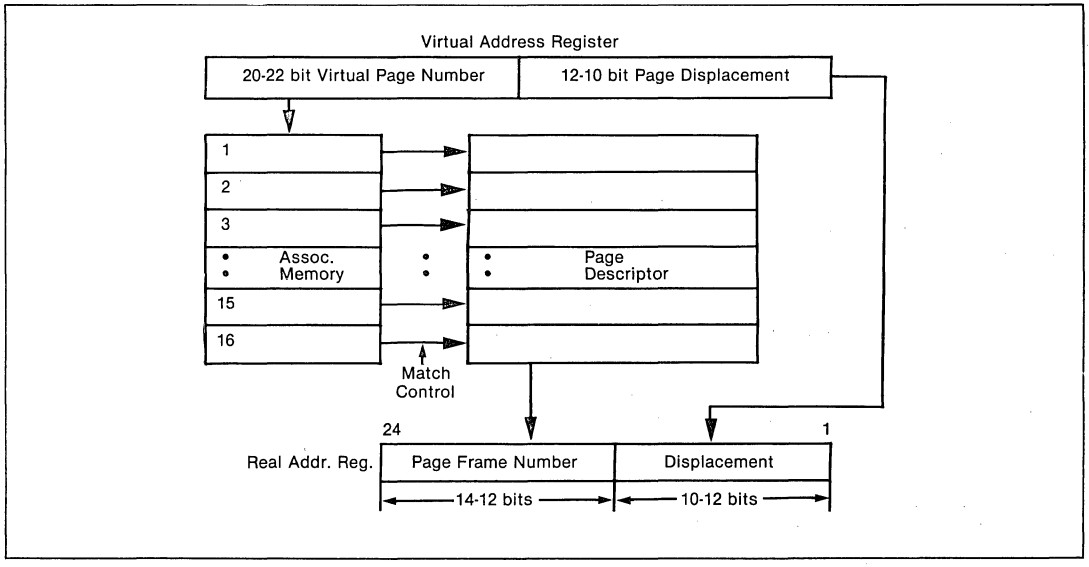
DYNAMIC ADDRESS TRANSLATION UNIT

The Dynamic Address Translation Unit (DAT) consists of 16 sets of registers which are used to translate virtual addresses into real addresses and to control DAT operation. Each entry consists of two parts: the Associative Memory (AM) entry, and the corresponding Page Descriptor entry.

The AM entries are a set of 22-bit Virtual Page Numbers (VPNs) which constitute a virtual address lookup table. The Page Descriptors are 25-bit registers consisting of eight Protection Check bits, a 14-bit Page Frame Number (PFN), two AM entry control bits (Changed Page and Register Referenced bits), an Invalid Register bit, and two sets of 4-bit memory access protection mask bits. The Associative Memory array and the Page Descriptor array are accessed with several ATC commands.

Two types of address messages can be asserted for the ATC by the system processor (CPC): real and virtual. When a real message is asserted, the ATC performs no address translation on the address; that is, the ATC accesses memory using the address contained in the real message. When a virtual message is asserted, the ATC uses the entries in the DAT unit to translate the virtual message into a real address which is then used to access memory.

DAT MODEL

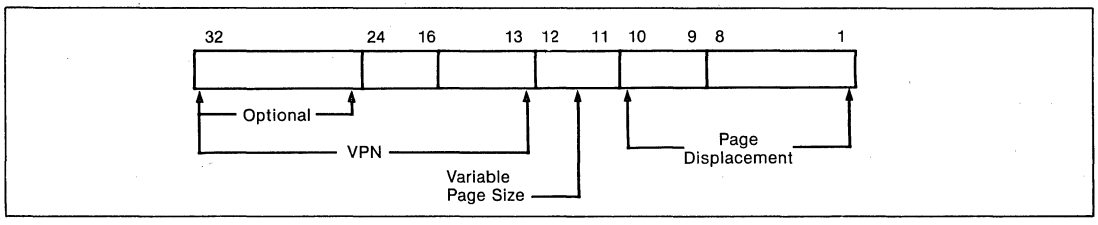


VIRTUAL ADDRESS TRANSLATION

All virtual messages asserted by the CPC are composed of a Virtual Page Number (VPN) and a Page Displacement with the following format.

When a virtual message is asserted by the processor, the ATC latches the message into its Virtual Address Register and compares the VPN content of the message with the VPN content of the Associative Memory array. If there is no match, the ATC asserts a DAT No Match interrupt (see Interrupt/Trap Array). If there is a match, the ATC concatenates the Page Frame Number in the Page Descriptor associated with the matching AM entry with the Page Displacement in the Virtual Address Register, stores the resulting real address into the ATC Real Address Register, and asserts the real address onto the PM Bus.

VIRTUAL MESSAGE FORMAT



MEMORY ACCESS PROTECTION

Each Page Descriptor entry in the DAT contains two sets of memory access protection mask bits. One set is used for operation in the privileged state, the other set is used for operation in the non-privileged state. Each set consists of a PCR, a PCW, a PCE, and a PCL bit which control the types of accesses into the associated virtual page that are permitted: fetch (read), store (write), fetch for execute, and fetch for linkage. Which set of access protection bits is used is determined by the state of the Privilege Flag, bit 1, in the Control Array. If CA1 is set, the privileged set is used; if CA1 is cleared, the non-privileged set is used.

The least significant two bits of a virtual message are memory access code bits which identify the type of memory access being executed. During each virtual memory operation, these bits are decoded and compared with the appropriate protection check bits associated with the virtual page being accessed. An attempt to access memory for an operation violating the selected protection results in an access violation. If an access violation occurs, the memory operation is aborted and the DAT Access Violation interrupt bit is set in the Interrupt/Trap Array.

MEMORY ACCESS PROTECTION

Protection Mask Bit	Bit State	Function Prevented/Permitted in related page in Memory
PCR (read)	0	Prevents a Read
	1	Permits a Read
PCW (write)	0	Prevents a Write
	1	Permits a Write
PCE (execute)	0	Prevents an Execute
	1	Permits an Execute
PCL (linkage)	0	Prevents Linkage
	1	Permits Linkage

DAT CONTROL BITS

The DAT Page Descriptors include three bits which provide protection against use of invalid DAT entries for the firmware, flag the processor whenever a virtual page is initially written into, and allow easy control of DAT entry changes. These bits, the Invalid Register (IR) bit, the Changed Page (CP) bit, and the Register Referenced (RR) bit, are controlled by several ATC commands.

ATC REGISTERS

The ATC has several registers external to the DAT which can be classified into two groups: special purpose registers, and virtual operation registers.

Most registers can be accessed by the system processor. The NCR/32-000 CPC, when used as the system processor, accesses the ATC using External Register Unit (ERU) transfer operations. The ATC is mapped in the CPC External Register Unit map. When accessing an ATC register, the CPC indicates to the ATC that the operation is an ERU access by asserting the $\overline{\text{EREP}}$ signal on the system bus, addresses the ATC register using bits 1-7 of the ERU message, and identifies the operation as a read or a write using bit 8 of the message.

ATC REGISTER ERU ASSIGNMENTS

ERU Address Dec.	ERU Address Hex.	Transfer Out Operation (Bit 8 = 1)	Transfer In Operation (Bit 8 = 0)
40	28	Control Array #2	Control Array #2
41	29	I/T Array	I/T Array
42	2A	Interrupt Mask Reg	Interrupt Mask Reg
43	2B	Intvl. Timer/Monitor Reg	Intvl. Timer/Monitor Reg
44	2C	Time-Of-Day Reg/Counter	Time-Of-Day Reg/Counter
45	2D	Address Monitor Reg	Address Monitor Reg
46	2E	Bus Interrupt Reg	Bus Interrupt Reg
47	2F	Write Page Size (WPS)	Read Page Size (RPS)
48	30	Invldt Assoc Mem (IAM)	Enabl & Set Pg Frm (ESPF)
49	31	Write Syndrome Bits	Read Syndrome Bits
50	32	Write Vitural Page (WVP)	Read Page Frame (RPF)
51	33	Write & Set Pg Frm (WSPF)	Clear Assoc Mem (CAM)
52	34	Purge Selective (PS)	Reserved for future use
53	35	Write Purge Mask (WPM)	Read Purge Mask (RPM)
54	36	Purge Set W Mask (PSM)	Read Virtual Address (RVA)
55	37	Trans Virt Addr (TVA)	Read Real Address (RRA)

TRAP AND INTERRUPT OPERATION AND SERVICING

Interrupts are asserted in response to conditions that may be serviced immediately, may be serviced after a time delay, or may be masked and not recognized at all according to system requirements. Traps are asserted in response to conditions that are considered to require immediate firmware servicing in all applications and cannot therefore be ignored.

OPERATION

Each time an interrupt bit sets in the Interrupt/Trap Array, the ATC asserts the INT output signal to interrupt the processor. Each time a trap bit sets in the Interrupt/Trap Array, the ATC asserts the Trap output signal to trap the processor. The setting of these bits forces $\overline{\text{INT/TRAP}}$ assertion.

SERVICING

Most interrupts and all traps can be cleared by writing the appropriate bit clear in the Interrupt/Trap Array. Normally the processor reads the Interrupt/Trap Array with a TIE operation in response to the assertion of $\overline{\text{INT}}$ or $\overline{\text{TRAP}}$, then clears the set interrupt/trap bit with a TOE operation to the Interrupt/Trap Array. The Interrupt/Trap Array is first read to identify the set bit forcing the interrupt/trap, then the set bit is cleared by the processor and written to the Interrupt/Trap Array with all other bits in the state in which they were read. If more than one bit is set, the interrupt/trap with the highest priority is serviced first.

NCR

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NCR/32-020
EXTENDED ARITHMETIC CHIP (EAC)

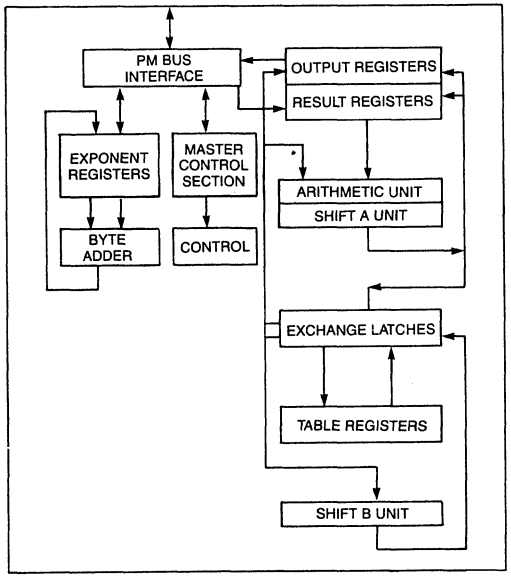
- **NCR/32-000 compatibility**
- **Variety of operations**
  - **— Hexadecimal Floating Point**
  - **— Binary Coded Decimal Floating Point**
  - **— Fixed Point Binary Multiplication and Division**
  - **— Conversion**
  - **— Shift**
- **8 Externally accessible registers**
- **50 Function Codes specifying the various operations**
- **Up to 3 word (96 bit) operand width**

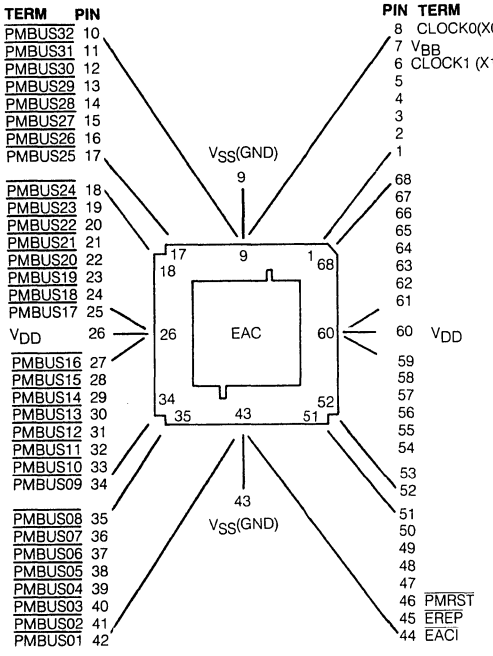
The NCR/32-020 is built on a very high density NMOS VLSI logic chip with about 45,000 transitors. As part of the NCR/32 family, the EAC will enhance system performance by assisting the CPC chip with various arithmetic operations.

The EAC is made up of eight major functional blocks. These are the master control sections, output registers, result registers, arithmetic unit, shift units, digit transfers, exponent section, control and miscellaneous logic.

The NCR/32-020 Extended Arithmetic Chip is an NMOS, 32-bit math coprocessor which performs hexadecimal floating point, binary coded decimal floating point, fixed point binary multiplication and division, conversion, and shift operations. It features six 32-bit wide operand registers, which facilitate triple precision math. The chip is commanded with a set of 50 different function codes.

The EAC can be interfaced to the NCR/32-000 Central Processor Chip over the PM-Bus to enhance the performance of a CPC application. The CPC and EAC, in conjunction with other NCR/32 family devices, comprise a powerful VLSI based processor system well suited for a wide variety of applications.





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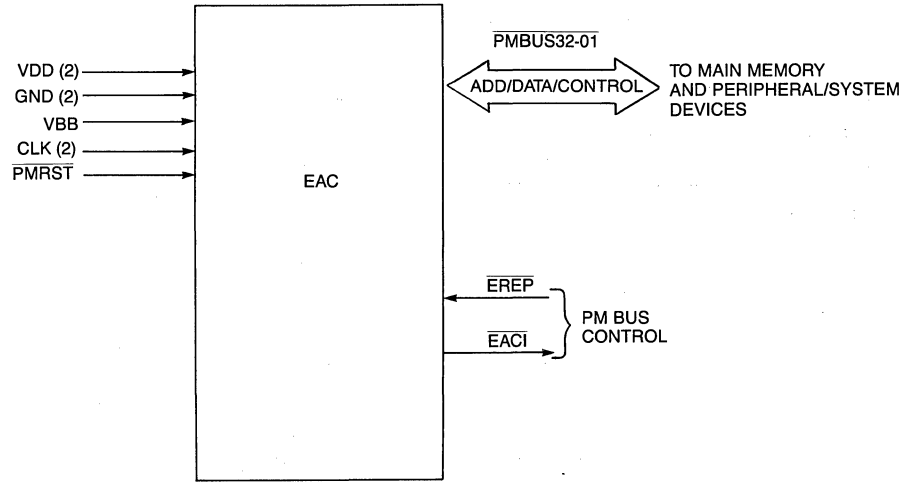
SIGNAL DESCRIPTION

The EAC input and output signals can be organized into groups as shown below. A description of each EAC signal or signal group and a summary of the signals is contained in the following tables.

PIN #	SYMBOL	DESCRIPTION
10-25 27-42	$\overline{\text{PMBUS32-01}}$	Processor Memory Bus — These multiplexed bus lines are used to transfer information between devices. In general, address information is transferred to a destination device during X0, and data is transferred to/from a destination devlce during X1.
8	X0	Phase 0 clock input
6	X1	Phase 1 clock input
44	$\overline{\text{EACI}}$	Extended Arithmetic Chip Information — After the EAC receives a function command, this line is set high to indicate that the EAC is busy. When the function is complete the EAC sets this line low to indicate to the CPC that this information or status is available.
45	$\overline{\text{EREP}}$	External Register Enable/Permit — This line, when pulsed low by the selected subsystem, indicates that the information on the PM Bus during X0 is the destination tag (direction of transfer and external register unit number) for a data transfer. The EAC monitors $\overline{\text{EREP}}$ to detect possible ERU transfers using its registers.
46	$\overline{\text{PMRST}}$	PM Bus Reset — This input, when asserted, holds the EAC in a reset state.
26,60	V_{DD}	Positive voltage supply.
9,43	V_{SS}	Ground
7	V_{BB}	Negative voltage supply
1-5	—	No connection (not used).
47-59	—	
61-68	—	

INPUT AND OUTPUT SIGNALS



DESCRIPTION AND OPERATION

When extended arithmetic operations are required, the CPC chip will execute a group of Transfer Out External (TOE) instructions to the EAC. The information transferred includes the function code and the operands to be executed. The EAC will then perform the requested function using the operands supplied. When the operation is complete, the EAC issues the EACI signal (active low) to inform the CPC that the data result is ready. Then, by executing a group of Transfer In External (TIE) instructions, the CPC recovers the contents of the EAC Status register and also the data results. All transfers between the CPC and EAC are done via the 32-bit Processor-Memory (P-M) bus.

EAC FUNCTION CODES

The CPC microinstruction EAF (Extended Arithmetic Function) causes the EAC function code to be sent to the EAC with a register to register transfer. The eight bit literal part of the EAF instruction forms the actual function code that is sent to the EAC. The 50 function codes are listed here, along with the mnemonics and descriptions.

MNEM.	CODE	FUNCTION	BIT FLOW
BMSS	11	Binary Multiply Signed Single Precision	32 x 32—>32
BMSD	15	Binary Multiply Signed Double Precision Result	32 x 32—>64
BDSS	19	Binary Divide and Modulo Signed Single Precision	32/32—>32 32MOD32—>32
BDSD	1E	Binary Divide and Modulo Signed Double by Single	64/32—>64 64MOD32—>32
FPAS	21	Floating Point Add Single Precision	32 + 32—>32
FPSS	25	Floating Point Subtract Single Precision	32–32—>32
FPASU	29	Floating Point Add Single Precision Unnormalized	32 + 32—>32
FPSSU	2D	Floating Point Subtract Single Precision Unnormalized	32–32—>32
FPAD	22	Floating Point Add Double Precision	64 + 64—>64
FPSD	26	Floating Point Subtract Double Precision	64–64—>64
FPADU	2A	Floating Point Add Double Precision Unnormalized	64 + 64—>64
FPSDU	2E	Floating Point Subtract Double Precision Unnormalized	64–64—>64
FPMS	41	Floating Point Multiply Single Precision	32 x 32—>32
FPDS	31	Floating Point Divide Single Precision	32/32—>32
FPIS	35	Floating Point Integer Divide Single Precision	32/32—>32
FPMD	42	Floating Point Multiply Double Precision	64 x 64—>64
FPDD	32	Floating Point Divide Double Precision	64/64—>64
FPID	36	Floating Point Integer Divide Double Precision	64/64—>64
FPSH	3D	Floating Point Half Single Precision	32 x (1/2)—>32
FPDH	3E	Floating Point Half Double Precision	64 x (1/2)—>64
FPMOS	39	Floating Point Modulo Single Precision	32MOD32—>32
FPMOD	3A	Floating Point Modulo Double Precision	64MOD64—>64
FPMSE	45	Floating Point Multiply	32 x 32—>64

Continued on next page.

MNEM.	CODE	FUNCTION	BIT FLOW
DFA	E3	Decimal Floating Point Add	21 + 21—>21*
DFS	E7	Decimal Floating Point Subract	21-21—>21*
DFM	FF	Decimal Floating Point Multiply	21 x 21—>21*
DFD	F3	Decimal Floating Point Divide	21/21—>21*
DFID	F7	Decimal Floating Point Integer Divide	21/21—>21*
DFMOD	FB	Decimal Floating Point Modulo	21MOD21—>21*
DFN	EB	Decimal Floating Point Normalization Operation	21—>21*
DFAE	EF	Decimal Floating Point Align to Exponent	21—>21*
CVBSDF	4A	Signed Binary(32) to Floating Point (64)	32—>64
CVDFBS	4D	Floating Point (64) to Signed Binary (32)	64—>32
CVBS10	D1	Signed Binary (32) to Decimal Floating Point	32—>21*
CV10BS	D5	Decimal Floating Point to Signed Binary (32)	21—>32
CVDF10	DA	Floating Point (64) to Decimal Floating Point	64—>21 22 x 21 —>21*
CV10DF	5E	Decimal Floating Point to Floating Point (64)	21—>64 64 x 64—>64
CVBD10	D2	Signed Binary (64) to Decimal Floating Point	64—>21*
CV10BD	D6	Decimal Floating Point to Signed Binary (64)	21—>64
CVSF10	D9	Floating Point (32) to Decimal Floating Point	32—>21 22 x 21—>21*
CV10SF	5D	Decimal Floating Point to Floating Point (32)	21—>32 32 x 32—>32
CVBSSF	49	Signed Binary (32) to Floating Point (32)	32—>32
RSTOR	00	Set the Restore Status	
CV10TF	5F	Decimal Floating Point to Floating Point (96)	21—>96 96 x 96—>96
SHRSS	05	Shift Right (32) Sign Fill	32—>32
SHRSZ	09	Shift Right (32) Zero Fill	32—>32
SHLSZ	0D	Shift Left (32) Zero Fill	32—>32
SHRDS	06	Shift Right (64) Sign Fill	64—>64
SHRDZ	0A	Shift Right (64) Zero Fill	64—>64
SHLDZ	0E	Shift Left (64) Zero Fill	64—>64

* The fraction of decimal floating point number is ranged from 18 to 21 digits (hardwired option).

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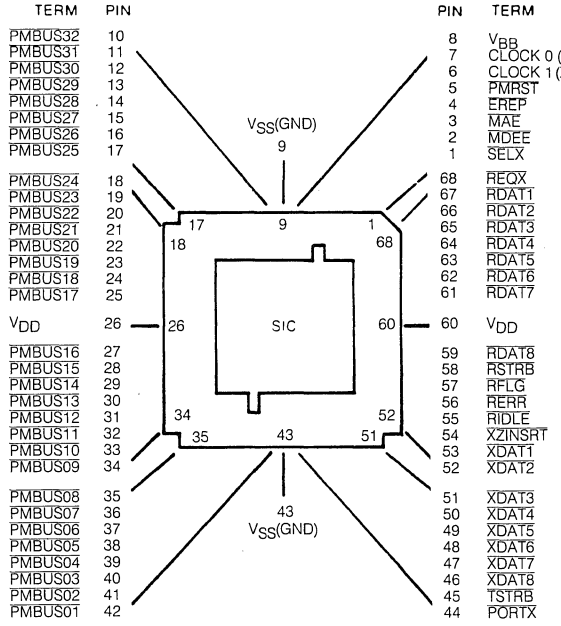
NCR/32-500
SYSTEM INTERFACE CONTROLLER (SIC)

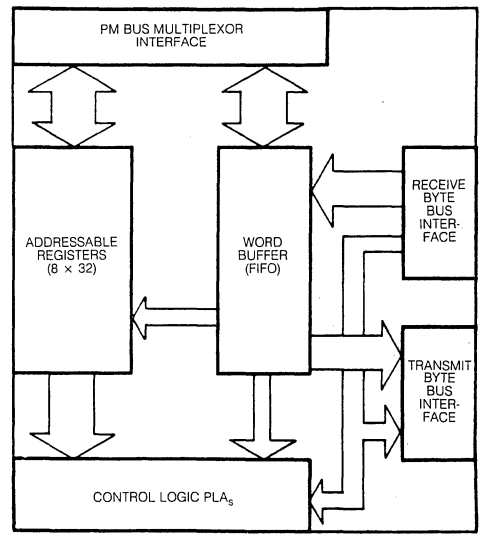
The NCR/32-500 System Interface Controller (SIC) is a serial communication channel controller utilizing a 32-bit architecture. The 32-bit architecture allows the SIC to control transmission of large blocks of data at high transmission rates. It also provides the SIC with a large addressing range for message retrieval and storage.

The NCR/32-500 System Interface Controller (SIC), the NCR/32-580 System Interface Transmitter (SIT), and the NCR/32-590 System Interface Receiver (SIR) combine to form a complete communications subsystem. This subsystem is capable of operating as an eight channel Digital Link Controller or as a high speed, dual channel, bus oriented Local Area Network node using either CSMA/CD or Token Passing network access arbitration.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to 7.0	V
Input Voltage	V_{IN}	-1.0 to 7.0	V
Input Voltage Clock	V_{INC}	-0.3 to 6.0	V
Substrate Bias Voltage	V_{BB}	-7.0 to 0.5	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature	T_{STG}	-40 to 125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance (Ceramic Flat-Pack)	θ_{JA}	25	°C/W

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0 Vdc ± 5%, V_{SS} = OV, V_{BB} = 2.5 Vdc ± 10%, T_A = O°C to 70°C)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	5.25	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Input High Voltage Clock	V_{IHC}	4.0	5.5	V
Input Low Voltage Clock	V_{ILC}	-0.5	0.4	V
Output High Voltage @ 400 mA	V_{OH}	2.4		V
Output Low Voltage @ 8 mA	V_{OL}		0.5	V
Leakage Current (V_{SS} to V_{DD}), Non-clock pins	I_L	-100	100	uA
Leakage Current (V_{SS} to V_{DD}), Clock pins	I_{LC}	-200	200	uA
Supply Current	I_{DD}		400	mA
Substrate Bias Current	I_{BB}	-1.0	0.01	mA
Power Dissipation @ 6.67 MHz	P_D		2.1	W
Capacitance (each Pin, Ceramic Flat-Pack)	C		15	pF

TIMING PARAMETERS

NUMBER	Parameter	Symbol	150 nSec (1) Min	150 nSec (1) Max	180 nSec (2) Min	180 nSec (2) Max	Unit
1	Clock Width High	tCH	50	500	60	500	nS
2	Clock Rise Time	tCR		10		10	nS
3	Clock Fall Time	tCF		10		10	nS
4	Clock Separation	tCS	15	100	20	100	nS
5	PM Bus Input Data Setup Time	tDS	20		25		nS
6	PM Bus Input Data Hold Time	tIDH	0		0		nS
7	$\overline{SELX}$ Setup Time	tSELS	22				nS
8	$\overline{SELX}$ Hold Time	tSELH	5				nS
9	$\overline{MDEE}$ Setup Time	tMDES	20				nS
10	$\overline{MDEE}$ Hold Time	tMDEH	5				nS
11	$\overline{EREP}$ Setup Time	tERES	15				nS
12	$\overline{EREP}$ Hold Time	tEREH	5				nS
13	$\overline{TSTRB}$ (Synchronous) Setup Time	tTSTS	15				nS
14	$\overline{TSTRB}$ (Synchronous) Hold Time	tTSTH	5				nS
15	$\overline{RDAT1\text{-}8}$, $\overline{RERR}$, $\overline{RFLG}$, $\overline{RIDLE}$, $\overline{RSTRB}$ Setup Time	tRBBS	22				nS
16	$\overline{RDAT1\text{-}8}$, $\overline{RERR}$, $\overline{RFLG}$, $\overline{RIDLE}$, $\overline{RSTRB}$ Hold Time	tRBBH	5				nS
17	$\overline{XSTRB}$ Setup Time	tXSTS	30				nS
18	$\overline{XSTRB}$ Hold Time	tXSTH	5				nS
19	PM Bus Reset Setup Time	tRSTS	25				nS
20	PM Bus Reset Hold Time	tRSTH	5				nS
21	PM Bus Address Delay	tPMAD		30			nS
22	PM Bus Address Hold Time	tPMAH	5	25			nS
23	PM Bus Output Data Delay	tODD		30			nS
24	PM Bus Output Data Hold Time	tODH	5	25			nS
25	$\overline{REQX}$ Delay	tREQD		60			nS
26	$\overline{REQX}$ Hold Time	tREQH	5	60			nS
27	$\overline{MAE}$ Delay	tMAED		30			nS
28	$\overline{MAE}$ Hold Time	tMAEH	5	30			nS
29	$\overline{EREP}$ Delay	tERPD		30			nS
30	$\overline{EREP}$ Hold Time	tERPH	5	30			nS
31	$\overline{XDAT1\text{-}8}$, $\overline{XZINSRT}$ Delay	tXBBD		34			nS
32	$\overline{XDAT1\text{-}8}$, $\overline{XZINSRT}$ Hold Time	tXBBH	5	40			nS
33	Clock Period	tCYL	150		180		nS

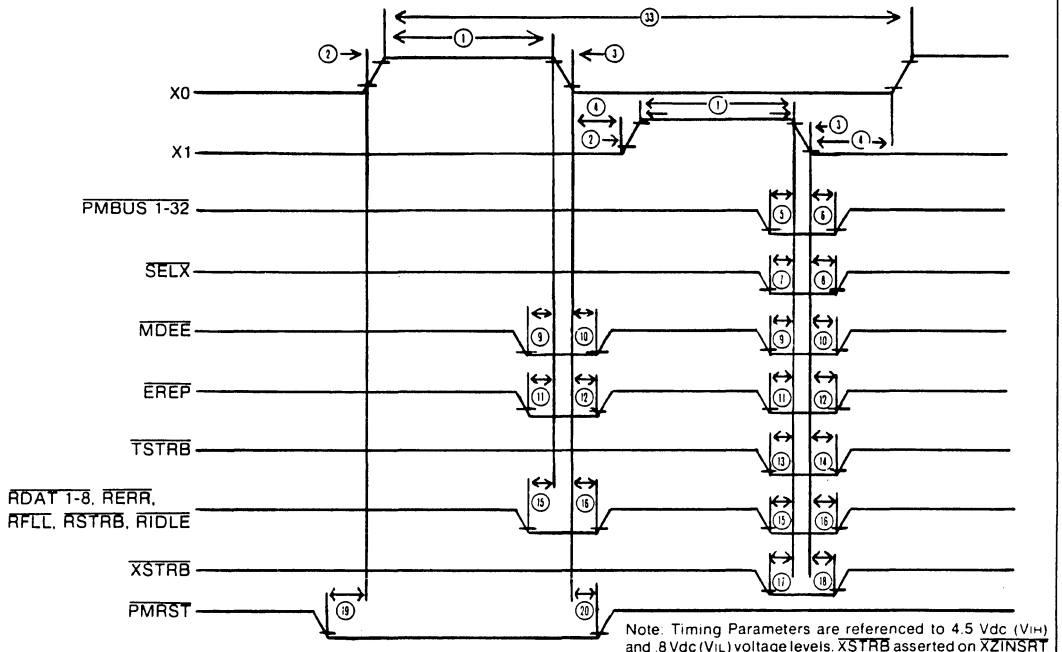
(1) NCR/32-000-5 (2) NCR/32-000-8

(V_{DD} = 5.0 Vdc ± 5%, V_{SS} = 0Vdc, V_{BB} = 2.5 Vdc ± 10%, T_A = 0°C to 70°C)

NOTE: THE TEST LOAD IS A 680Ω PULL UP RESISTOR AND 50 Pf CAPACITANCE

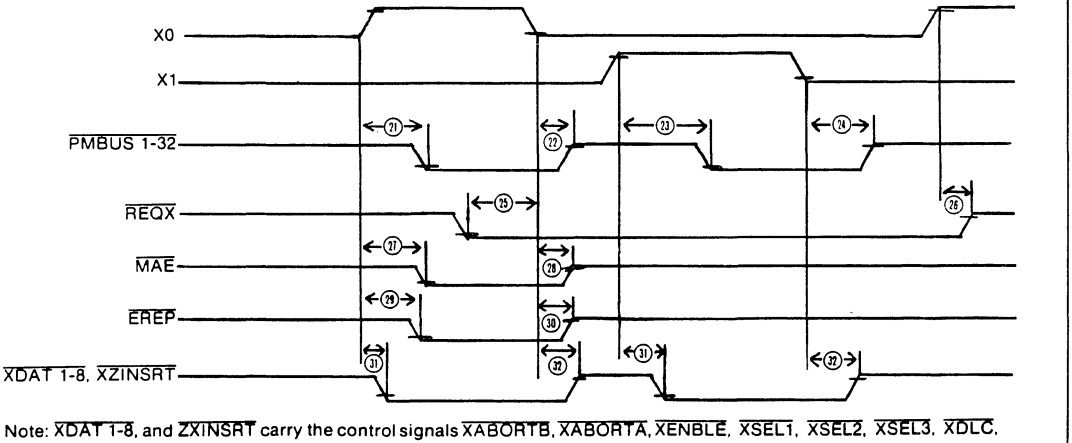
This is advance information and NCR reserves the right to change the specifications without notice.

INPUT TIMING DIAGRAM



Note: Timing Parameters are referenced to 4.5 Vdc (V_{IH}) and .8 Vdc (V_{IL}) voltage levels. XSTRB asserted on XZINSRT during X1.

OUTPUT TIMING DIAGRAM



Note: XDAT 1-8, and ZXINSRT carry the control signals XABORTB, XABORTA, XENBLE, XSEL1, XSEL2, XSEL3, XDLC, XDIAG, and XSTRB during the X1 clock phase.

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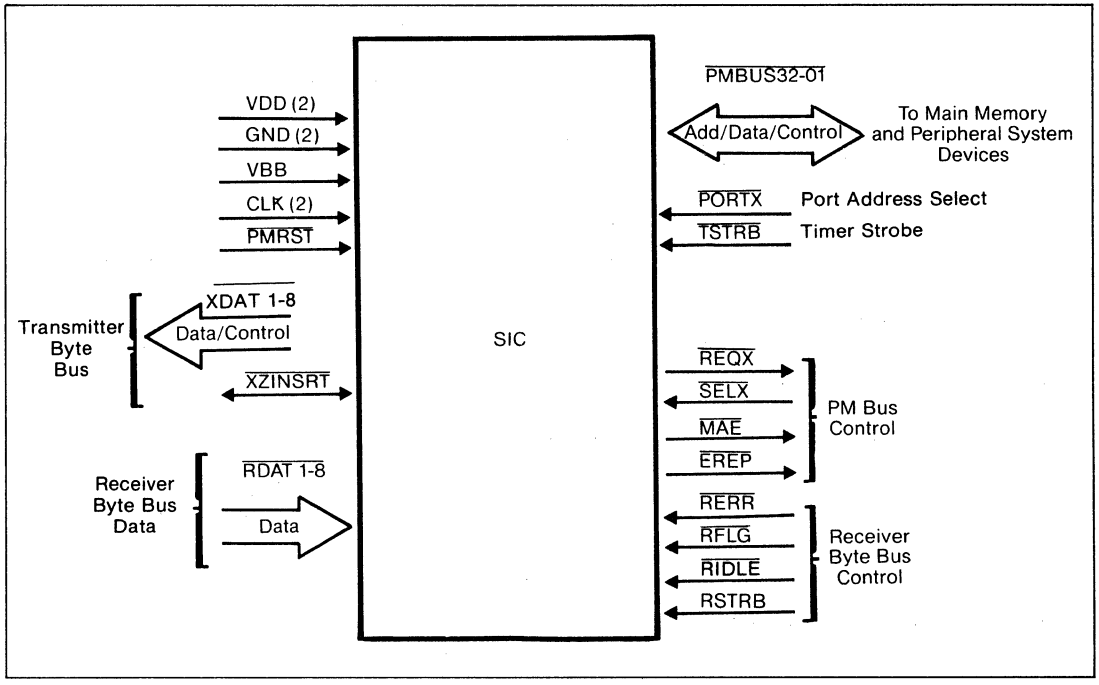
SIGNAL DESCRIPTION

The SIC input and output signals can be organized into groups as shown below. A description of each SIC signal or signal group and a summary of the signals are contained in the following tables.

INPUT AND OUTPUT SIGNALS



SIGNAL DESCRIPTION

Pin	Signal	Description
1	$\overline{SELX}$	Chip Select. A true (low) signal on this input pin during the X1 clock phase will grant PM Bus access to the SIC during the next clock cycle. This signal is asserted by the PM Bus arbitration logic.
2	$\overline{MDEE}$	Memory Data Enable/Error. When this input signal becomes active (low) during the X0 clock phase on fetch operations, it indicates that the valid data will be available on the PM Bus during the corresponding X1 clock phase. When $\overline{MDEE}$ is active during the X1 clock phase, it indicates to the SIC that the data received is either erroneous or invalid. This signal is asserted by the SIC-Memory interface.
3	$\overline{MAE}$	Memory Address Enable. This signal is generated by the SIC during the X0 clock phase to enable a real memory transfer on the PM Bus. This signal is asserted only after the SIC has been granted access to the PM Bus during the previous clock cycle via $\overline{REQX}$ and $\overline{SELX}$.
4	$\overline{EREP}$	External Register Enable/Permit. This bidirectional signal is output from the SIC during the X0 clock phase and input to the SIC during either clock phase. The selected SIC (granted PM Bus access during the previous cycle via $\overline{REQX}$ and $\overline{SELX}$) asserts this signal during the X0 clock phase to enable the transfer of a Register Transfer Message on the PM Bus. A low input signal on $\overline{EREP}$ during the X1 clock phase inhibits SIC output register transfers over the PM Bus during the next clock cycle.
5	$\overline{PMRST}$	PM Bus Reset. When active (low), this signal forces all internal logic into a defined state. It is an asynchronous signal.
6	X1	CLOCK1 (X1) phase input.
7	X0	CLOCK0 (X0) phase input. The SIC uses an externally supplied, dual phase, non-overlapping clock to control all internal operations. The two clock phases are denoted as X0 and X1.
8	VBB	Negative voltage supply.
9, 43	VSS	Ground.
10-25 27-42	$\overline{PMBUS32}$ - $\overline{PMBUS01}$	Processor Memory Bus. This active-low, open drain, time-shared bus is the connecting data/address path between the SIC, memory, and processing devices. The PM Bus carries address information during the X0 clock phase and data during the X1 clock phase.
26,60	VDD	Positive voltage supply.
44	$\overline{PORTX}$	Port Address Select. This signal is used to determine the addresses of the SIC internal registers. It may be tied to VSS, X0, or X1 as shown in Figures 36 and 59. The use of $\overline{PORTX}$ allows the inclusion of up to four SICs within a single system.
45	$\overline{TSTRB}$	Timer Strobe. This input carries the clock signal for a message retry in Network Mode operation. In DLC Mode, $\overline{TSTRB}$ carries the clock signal for the response timer.
46-54		Transmitter Byte Bus. The Transmitter Byte Bus is the data and control link between the SIC and the transmitting unit. These signals are multiplexed, carrying primarily data during the X0 clock phase and carrying control information during the X1 clock phase.
46-53	$\overline{XDAT8}$ - $\overline{XDAT1}$	Transmitter Byte Bus Data. These active low outputs carry parallel data to the transmitting device, one byte at a time.
54	$\overline{XZINSRT}$	Zero Insertion Enable. This control signal is sent with the data byte to define whether or not the byte is to be zero inserted. Activation of this signal causes the corresponding data byte to have a zero inserted following any sequence containing five consecutive ones. The Transmitter Byte Bus (pins 46-54) carries the following signals during the X1 clock phase:

This is advance information and NCR reserves the right to change the specifications without notice.

SIGNAL DESCRIPTION CONT.

Pin	Signal	Description
46		$\overline{\text{XDIAG}}$ (Diagnostic Mode Enable)—This output is used for interfacing with the NCR/32-580 System Interface Transmitter (SIT). A low signal causes the SIT to operate in diagnostic mode.
47		$\overline{\text{XDLC}}$ (Transmission Mode Select)—Also used for interfacing with the SIT. Activation of this signal causes the SIT to operate in DLC mode.
48-50		$\overline{\text{XSEL3}}$-$\overline{\text{XSEL1}}$ (Transmission Channel Selects)—The binary combination of these three signals is used by a SIT operating in DLC mode to determine on which channel the data is to be transmitted.
51		$\overline{\text{XENBLE}}$ (Transmission Enable)—This output signal qualifies the Byte Bus data as valid for transmission.
52-53		$\overline{\text{XABORTA}}$, $\overline{\text{XABORTB}}$ (Transmission Aborts)—These signals are used only when the SIC is operating in Network Mode. Activation of an $\overline{\text{XABORT}}$ signal causes a DC high (i.e., jamming) on network bus channel A or B, as specified.
54		$\overline{\text{XSTRB}}$ (Transmission Strobe)—Activation of this input signal indicates that the transmitter has latched the data byte on the Transmitter Byte Bus.
55	$\overline{\text{RIDLE}}$	Received Idle. This signal is received from the NCR/32-590 SIR when an input channel error (DC low for greater than three bit times) is detected.
56	$\overline{\text{RERR}}$	Received Error. This signal is received from the SIR when an input channel error (DC high for greater than two bit times) is detected.
57	$\overline{\text{RUNQ}}$	Received Unique Character. This signal, also sourced from the SIR, indicates that a unique character (a byte containing six or more consecutive ones) has been received.
58	$\overline{\text{RSTRB}}$	Receiver Strobe. This signal is activated by the receiver when it has a valid byte of data to transfer to the SIC.
59 61-67	$\overline{\text{RDAT8}}$ - $\overline{\text{RDAT1}}$	Receiver Byte Bus Data. These pins contain the data byte, in parallel, being transferred to the SIC by the receiver.
68	$\overline{\text{REQX}}$	PM Bus Request. This output is asserted when the SIC requires access to the PM Bus. It is asserted during the X0 clock phase, and is stable for the remainder of the clock cycle.

This is advance information and NCR reserves the right to change the specifications without notice.

SIGNAL SUMMARY

Signal Name	Pin #	Symbol	Input/Output	Active State	Drive
Chip Select	1	$\overline{SELX}$	Input	Low	Input
Memory Data Enable/Error	2	$\overline{MDEE}$	Input/Output	Low	Open Drain
Memory Address Enable	3	$\overline{MAE}$	Output	Low	Open Drain
External Register Enable/Permit	4	$\overline{EREP}$	Input/Output	Low	Open Drain
PM Bus Reset	5	$\overline{PMRST}$	Input	Low	Input
Clock 1	6	X1	Input	High	Input
Clock 0	7	X0	Input	High	Input
Power Input (Negative Voltage)	8	VBB	Input	-	-
Ground	9, 43	VSS	Input	-	-
Processor - Memory Bus	10-25, 27-42	$\overline{PM\ Bus\ 32\text{-}01}$	Input/Output	Low	Open Drain
Power Input (Positive Voltage)	26, 60	VDD	Input	-	-
Port Address Select	44	$\overline{PORTX}$	Input	Low	Input
Timer Strobe	45	$\overline{TSTRB}$	Input	Low	Input
Transmit Byte Bus	46-53	$\overline{XDAT\ 8\text{-}1}$	Input	Low	Open Drain
	54	$\overline{XZINSRT}$	Input/Output		
Receiver Byte Bus	55-59 61-67	$\overline{RDAT\ 8\text{-}1}$ $\overline{RDAT\ 8\text{-}2}$, $\overline{RERR}$, $\overline{RFLG}$, $\overline{RIDLE}$, $\overline{RSTRB}$	Input	Low	Input
PM Bus Request	68	$\overline{REQX}$	Output	Low	Open Drain

This is advance information and NCR reserves the right to change the specifications without notice.

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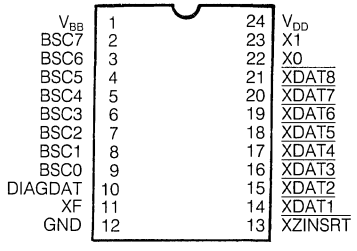
NCR/32-580
SYSTEM INTERFACE TRANSMITTER (SIT)

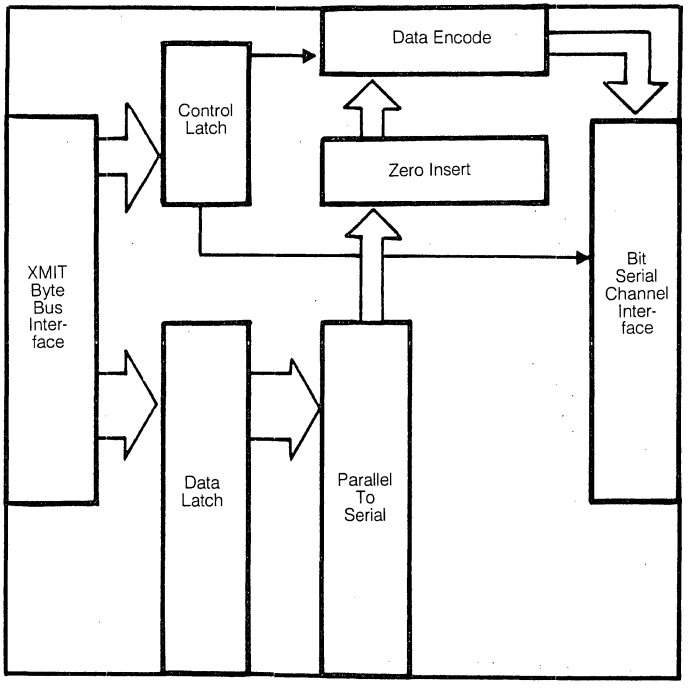
The NCR/32-580 System Interface Transmitter (SIT) is a flexible and powerful transmitting device. Three operating modes enable the use of a variety of system configurations, making the SIT an ideal transmitter for peripheral control as well as for Local Area Network applications.

The SIT, the NCR/32-500 System Interface Controller, and the NCR/32-590 System Interface Receiver form a complete communications subsystem. This system can be used as an eight channel data link controller or as a high speed, data-link level, Local Area Network node using CSMA/CD network access arbitration.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



NCR/32 PROCESSOR FAMILY

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MAXIMUM RATING

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to 7.0	V
Input Voltage	V_{IN}	-1.0 to 7.0	V
Input Voltage Clock	V_{INC}	-0.5 to 7.0	V
Substrate Bias Voltage	V_{BB}	-0.5 to 7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature	T_{STG}	-65 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance (Ceramic Flat-Pack)	θ_{JA}	25	°C/W

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0Vdc ± 5%, V_{SS} = OV. V_{BB} = -2.5Vdc ± 10%, T_A = O°C to 70°C)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	5.25	V
Input Low Voltage	V_{IL}	-0.1	0.8	V
Input High Voltage Clock	V_{IHC}	4.0	5.5	V
Input Low Voltage Clock	V_{ILC}	-1.0	0.0	V
Output High Voltage	V_{OH}	2.4		V
Output Low Voltage	V_{OL}		0.5	V
Leakage Current (V_{SS} to V_{DD}) $\overline{XZINSRT}$ pin	I_L	-10	50	uA
Leakage Current (V_{SS} to V_{DD}), all other pins	I_L	-10	2	uA
Supply Current	I_{DD}		250	mA
Substrate Bias Current	I_{BB}	-1.0	0	mA
Power Dissipation @ 6.67 MHz	P_D		1.8	W
Capacitance	C		10	pF

ELECTRICAL CHARACTERISTICS

NUMBER	Parameter	Symbol	150 nSec (1) Min	150 nSec (1) Max	1180 nSec(2) Min	1180 nSec(2) Max	Unit
1	Clock Width High	t_{CH}	50	500	60	500	nS
2	Clock Rise Time	t_{CR}		10		10	nS
3	Clock Full Time	t_{CF}		10		10	nS
4	Clock Separation	t_{CS}	15	100	20	100	nS
5	Byte Bus Data Setup Time	t_{BDS}	25				nS
6	Byte Bus Data Hold Time	t_{BDH}	5				nS
7	Byte Bus Controls Setup Time	t_{BCS}	25				nS
8	Byte Bus Controls Hold Time	t_{BCH}	25				nS
9	Bit Serial Channel Data Propagation Delay	t_{BSCD}	16	27		180	nS
10	$\overline{XSTRB}$ Delay	t_{XSTD}	5	25			nS
11	$\overline{XSTRB}$ Hold Time	t_{XSTH}	5	25			nS
12	XF Rise Time	t_{XFR}		10		10	nS
13	XF Fall Time	t_{XFF}		10		10	nS
14	XF Cycle Time	t_{FCYC}					nS
15	Clock Cycle Time	t_{CYC}	150		180		

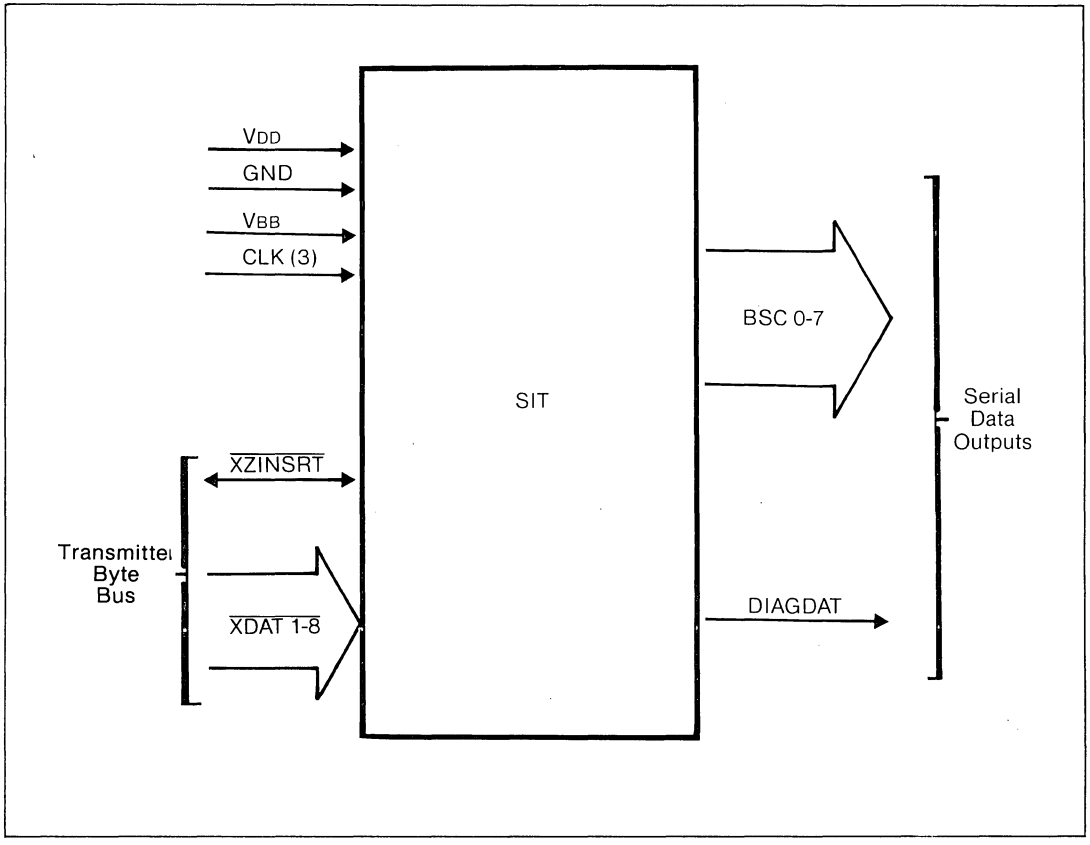
(V_{DD} = 5.0 Vdc ± 5%, V_{SS} = OVdc, V_{BB} = -2.5 Vdc ± 10%, T_A = 0°C to 70°C)
Note: THE TEST LOAD IS A 680Ω PULL UP RESISTOR AND 50 pF CAPACITANCE.

This is advance information and NCR reserves the right to change the specifications without notice.

SIGNAL DESCRIPTION

The SIT input and output signals can be organized into groups as shown below. A description of each SIT signal or signal group and a summary of the signals are contained in the following tables.

INPUT AND OUTPUT SIGNALS



SIGNAL DESCRIPTION

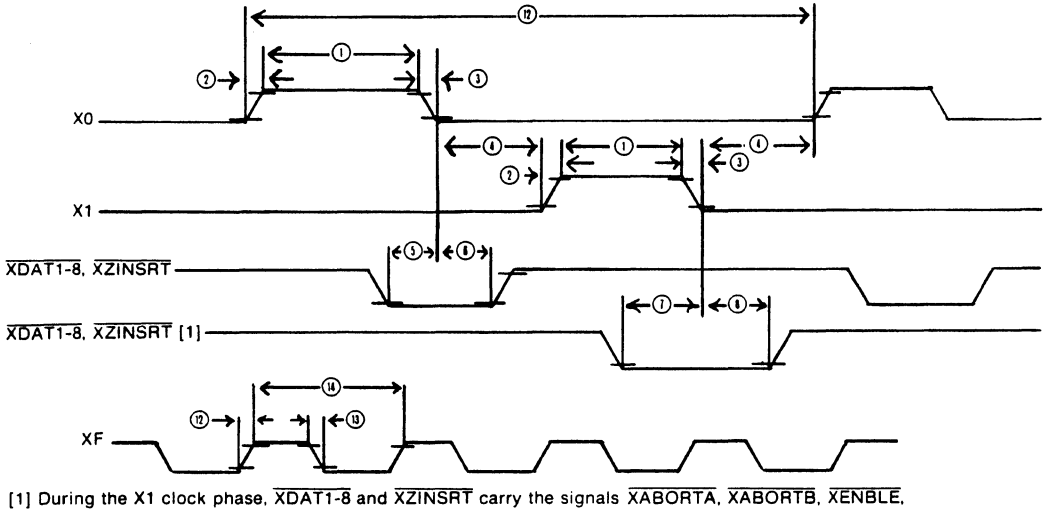
Pin	Signal	Description
1	VBB	Negative Voltage Supply.
2-7	BSC7 - BSC2	Bit serial Channel Output, Channels 7 to 2.
8,9	BSC1, BSC0	Bit Serial Channel Output, Channels 1 and 0. In Network Mode, BSC0 and BSC1 are the serial outputs for network bus channels A and B, respectively.
10	DIAGDAT	Diagnostic Data Output. Data is output on this port when the SIT is operating in diagnostic mode.
11	XF	Transmit Clock. This clock determines the rate of operation of the SIT. One byte time (eight pulses) of XF must be greater than two system clock periods by at least 20 nS.
12	VSS	Ground.
13-21		These pins are known collectively as the Transmitter Byte Bus. The Byte Bus consists of nine multiplexed data/control lines. Data is active during the X0 clock phase and controls are active during the X1 clock phase.
13	$\overline{\text{XZINSRT}}$	Zero Insertion Enable. This control line travels with the data byte to define whether or not the data byte is to be zero inserted.
14-21	$\overline{\text{XDAT1}}$ - $\overline{\text{XDAT8}}$	Transmitter Byte Bus Data. These inputs receive the parallel data which is to be serialized and transmitted.
		During the X1 clock phase the Byte Bus signals have the following definitions:
13		$\overline{\text{XSTRB}}$ (Transmitter Strobe)—When asserted, this output signal indicates that the SIT has accepted the data byte being presented on the Byte Bus.
14, 15		$\overline{\text{XABORTA}}$, $\overline{\text{XABORTB}}$ (Transmission Aborts)—The assertion of these signals, valid only in Network Mode, causes the transmission of a DC high for one to two byte times on network bus channel A or B, as indicated.
16		$\overline{\text{XENBLE}}$ (Transmission Enable)—This signal qualifies the Byte Bus data as valid to transmit. Activation of $\overline{\text{XENBLE}}$ enables encoding and propagation of the input data by the selected channel.
17-19		$\overline{\text{XSEL1}}$-$\overline{\text{XSEL3}}$ (Transmission Channel Selects)—The binary combination of these three signals determines on which Bit Serial Channel data is to be transmitted.
20		$\overline{\text{XDLC}}$ (Transmission Mode Select)—This signal determines the mode of operation of the SIT. Assertion of this signal enables DLC Mode operation.
21		$\overline{\text{XDIAG}}$ (Diagnostic Mode Enable)—This signal is used to select diagnostic operation. Assertion of $\overline{\text{XDIAG}}$ disables serial data output on BSD 0-7, enabling data output on DIAGDAT (pin 10).
22	X0	CLOCK0 Phase Input.
23	X1	CLOCK1 Phase Input. The SIT uses an externally supplied, dual phase, non-overlaping clock to control all internal operations. The two clock phases are denoted as X0 and X1.
24	VDD	Positive Voltage Supply.

This is advance information and NCR reserves the right to change the specifications without notice.

SIGNAL SUMMARY

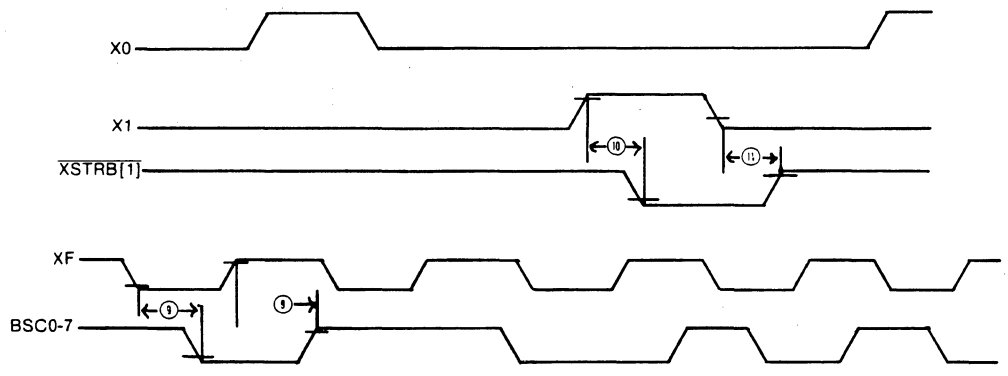
Signal Name	Pin #	Symbol	Input/Output	Active State	Drive
Power Input (Negative Voltage)	1	VBB	Input	—	—
Bit Serial Channels	2-9	BSC 0-7	Output	—	Totem Pole
Diagnostic Output	10	DIAGDAT	Output	—	Totem Pole
Transmit Clock	11	XF	Input	High	Input
Ground	12	VSS	Input	—	—
Zero Insertion Enable	13	$\overline{\text{XZINSRT}}$	Input/Output	Low	Input/Open Drain
Transmit Byte Bus Data	14-21	$\overline{\text{XDAT1-8}}$	Input	Low	Input
Clock0	22	X0	Input	High	Input
Clock1	23	X1	Input	High	Input
Power Input (Positive Voltage)	24	VDD	Input	—	—

INPUT TIMING DIAGRAM



[1] During the X1 clock phase, $\overline{\text{XDAT1-8}}$ and $\overline{\text{XZINSRT}}$ carry the signals $\overline{\text{XABORTA}}$, $\overline{\text{XABORTB}}$, $\overline{\text{XENBLE}}$, $\overline{\text{XSEL1-3}}$, $\overline{\text{XDLC}}$, $\overline{\text{XDIAG}}$, and $\overline{\text{XSTRB}}$.

OUTPUT TIMING DIAGRAM



[1] The $\overline{\text{XSTRB}}$ output is carried on the $\overline{\text{XZINSRT}}$ Port during the X1 clock phase.

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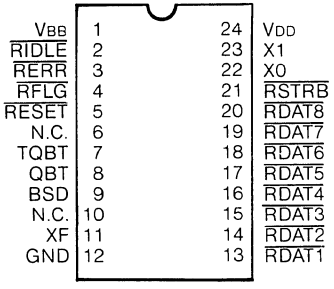
NCR/32-590
SYSTEM INTERFACE RECEIVER (SIR)

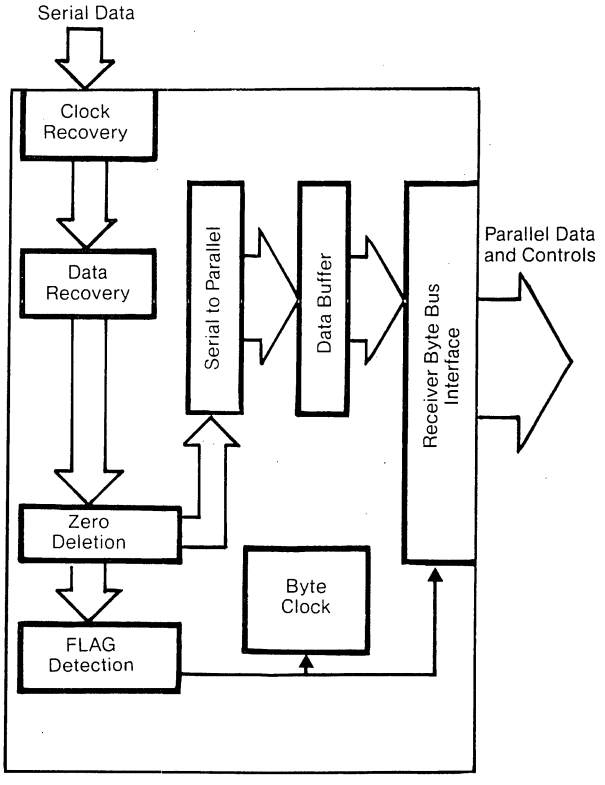
The NCR/32-590 System Interface Receiver (SIR) is a serial bit channel receiving device useful in a wide variety of communications applications. It is capable of operating at very low speeds as well as bit rates as high as 24 Mbit/second, making it useful for peripheral interfacing as well as for Local Area Network accessing.

The SIR, the NCR/32-500 System Interface Controller, and the NCR/32-580 System Interface Transmitter form a complete communications subsystem. This system can be used as an eight channel SDLC compatible peripheral interface or as a high speed, data-link-level, Local Area Network node using CSMA/CD network access arbitration.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to 7.0	V
Input Voltage	V_{IN}	-1.0 to 7.0	V
Input Voltage Clock	V_{INC}	-0.5 to 7.0	V
Substrate Bias Voltage	V_{BB}	-5.0 to 0.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature	T_{STG}	-65 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance (Ceramic D.I.P.)	θ_{JA}	25	°C/W

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0 Vdc ± 5%, V_{SS} = 0V, V_{BB} = 2.5 Vdc ± 10%, T_A = 0°C to 70°C)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	5.25	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Input High Voltage Clock	V_{IHC}	4.0	5.5	V
Input Low Voltage Clock	V_{ILC}	-0.5	0.4	V
Output High Voltage @ 400 uA	V_{OH}	2.4		V
Output Low Voltage @ 8 mA	V_{OL}		0.5	V
Leakage Current (V_{SS} to V_{DD}), clock pins	I_{LC}	-10	20	uA
Leakage Current (V_{SS} to V_{DD}), non-clock pins	I_L	-10	2	uA
Supply Current	I_{DD}		250	mA
Substrate Bias Current	I_{BB}	-1.0	0	mA
Power Dissipation @ 6.67 MHz	P_D		1.8	W
Capacitance	C		10	pF

TIMING PARAMETERS

NUMBER	Parameter	Symbol	150 n Sec (1) Min	150 n Sec (1) Max	180 n Sec (2) Min	180 n Sec (2) Max	Unit
1	Clock Width High	t_{CH}	50	500	60	500	nS
2	Clock Rise Time	t_{CR}		10		10	nS
3	Clock Fall Time	t_{CF}		10		10	nS
4	Clock Separation	t_{CS}	15	100	20	100	nS
5	$\overline{RDAT1\text{-}8}$, $\overline{RFLG}$, $\overline{RERR}$, $\overline{RIDLE}$, $\overline{RSTRB}$ Propagation Delay	t_{RBDD}		25			nS
6	$\overline{RDAT1\text{-}8}$, $\overline{RFLG}$, $\overline{RERR}$, $\overline{RIDLE}$, $\overline{RSTRB}$ Hold Time	t_{RBDH}		45			nS
7	Bit Serial Data Input Rise Time	t_{BSDR}		10			nS
8	Bit Serial Data Input Fall Time	t_{BSDF}		10			nS
9	Clock Cycle Time	t_{CYC}		150		180	nS

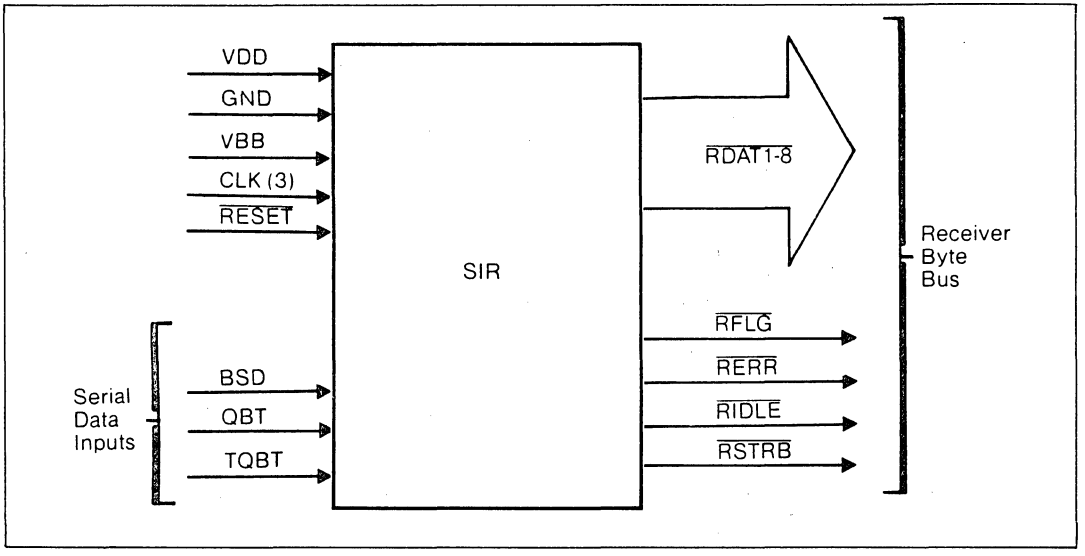
(V_{DD} = 5.0 Vdc ± 5%, V_{SS} = Vdc, V_{BB} = −2.5 Vdc ± 10%, T_A = 0°C to 70°C)
Note: THE TEST LOAD IS A 680Ω PULL UP RESISTOR AND 50 pF CAPACITANCE

This is advance information and NCR reserves the right to change the specifications without notice.

SIGNAL DESCRIPTION

The SIR input and output signals can be organized into groups as shown below. A description of each SIR signal or signal group and a summary of the signals are contained in the following tables.

INPUT AND OUTPUT SIGNALS



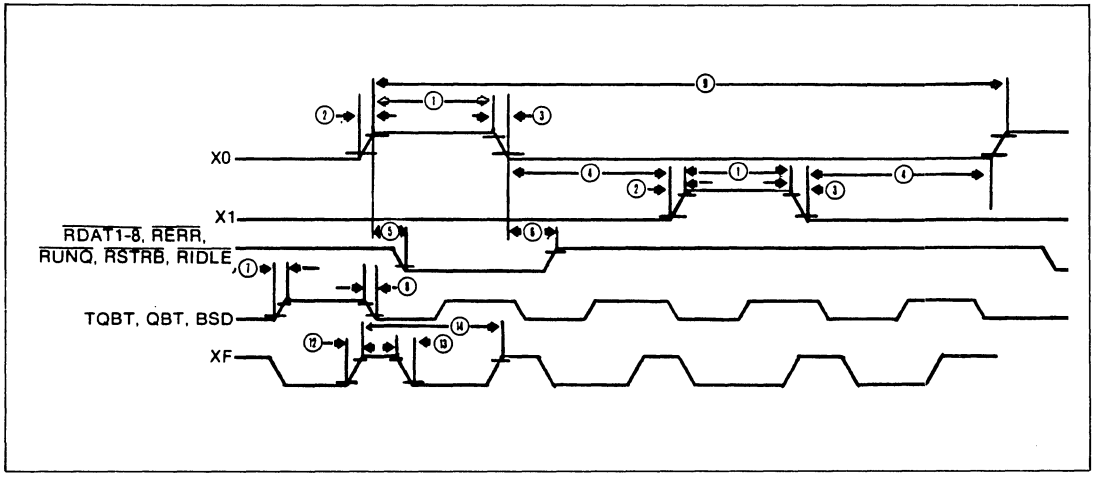
SIGNAL DESCRIPTION

Pin	Signal	Description
1	VBB	Negative Voltage Supply.
2	$\overline{\text{RIDLE}}$	Receiver Idle. This signal is asserted (low) during the X0 clock phase when an idle input channel (BSD low for greater than three consecutive bit times) is detected.
3	$\overline{\text{RERR}}$	Receiver Error. This signal is asserted during the X0 clock phase when an input error is detected. An input error consists of a DC high for two to four bit times.
4	$\overline{\text{RUNQ}}$	Receiver Unique Character. This signal is asserted during the X0 clock phase if a byte containing six or more consecutive ones is received. $\overline{\text{RDAT8}}$ is used along with this signal to determine whether a Flag (bit pattern 01111110) or non-Flag character has been received.
5	$\overline{\text{RESET}}$	Chip Reset. Activation of the $\overline{\text{RESET}}$ signal forces all internal logic into a defined state.
6	NC	Not Connected.
7	TQBT	Three Quarter Bit Time Delay Data. This signal consists of the Bit Serial Data input. delayed externally by a constant equalling three quarters of the bit clock period.
8	QBT	Quarter Bit Time Delay Data. This signal consists of the Bit Serial Data input, delayed externally by a constant equalling one quarter of the bit clock period.
9	BSD	Bit Serial Data. This signal consists of the received diphase encoded data from the transmission channel.
10	NC	Not Connected.
11	XF	Bit Clock. This clock must be set to the same rate as that of the incoming data. One byte time (eight pulses) of XF must be greater than two system clock periods by at least 20 n.
12	VSS	Ground.
13-20	$\overline{\text{RDAT1}}$ $\overline{\text{RDAT8}}$	Receiver Data, 1-8. These pins carry the parallel output data of the SIR. They are active during the X0 clock phase. These outputs are open-drain, and thus require a pullup resistor to VDD.
21	$\overline{\text{RSTRB}}$	Receiver Strobe. This signal qualifies the eight data outputs as valid. An active $\overline{\text{RSTRB}}$ indicates that the parallel data must be latched immediately. This signal may be used in conjunction with the falling edge of X0 to latch the received data being presented on $\overline{\text{RDAT1-8}}$.
22	X0	CLOCK0 phase input.
23	X1	CLOCK1 phase input. The SIR uses an externally supplied, non-overlapping, two phase clock to control all internal operations. The two clock phases are denoted as X0 and X1.
24	VDD	Positive Voltage Supply.

SIGNAL SUMMARY

Signal Name	Pin #	Symbol	Input/Output	Active State	Drive
Power Input (Negative Voltage)	1	VBB	Input	-	-
Receiver Idle	2	$\overline{\text{RIDLE}}$	Output	Low	Open Drain
Receiver Error	3	$\overline{\text{RERR}}$	Output	Low	Open Drain
Received Flag	4	$\overline{\text{RFLG}}$	Output	Low	Open Drain
Chip Reset	5	$\overline{\text{RESET}}$	Input	Low	Input
Three Quarter Bit Time Delayed Data	7	TQBT	Input	-	Input
Quarter Bit Time Delayed Data	8	QBT	Input	-	Input
Bit Serial Data	9	BSD	Input	-	Input
Bit Clock	11	XF	Input	High	Input
Ground	12	VSS	Input	-	-
Receiver Data, 1-8	13-20	$\overline{\text{RDAT1-8}}$	Output	Low	Open Drain
Receiver Strobe	21	$\overline{\text{RSTRB}}$	Output	Low	Open Drain
Clock 0	22	X0	Input	High	Input
Clock 1	23	X1	Input	High	Input
Power Input (Positive Voltage)	24	VDD	Input	-	-

TIMING DIAGRAM



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NCR Microcomputers/Microprocessors

PRODUCT SELECTION GUIDE

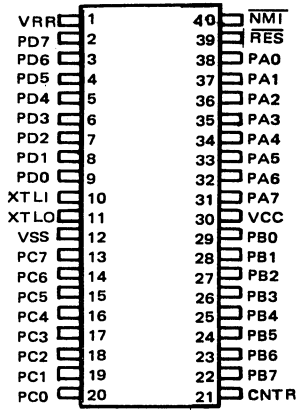
6500/1 and 6500/1E
SINGLE-CHIP MICROCOMPUTER

- 6502 CPU
  - 8-bit parallel processing
  - Software upward / downward compatibility
  - 13 addressing modes
  - Decimal or binary arithmetic
  - True indexing capability
  - Memory addressable I/O
  - Pipeline architecture
- 2048 x 8 mask-programmable ROM
- 64 x 8 static RAM
- Power down mode
- 32 bidirectional TTL compatible I/O lines (1 positive and 1 negative edge sensitive)
- 1 bidirectional TTL compatible counter I/O line
- 16-bit programmable counter / latch
  - Interval timer
  - Pulse generator
  - Event counter
  - Pulse width measurement
- Five interrupts: 4 external and 1 counter overflow
- 4 MHz max crystal or external clock frequency
- 1 or 2 MHz internal clock
- 70% of instructions have execution times less than 2 μs at 2 MHz
- NMOS silicon gate, depletion load technology
- Single +5V power supply
- Emulator device available (NCR 6500/1E)

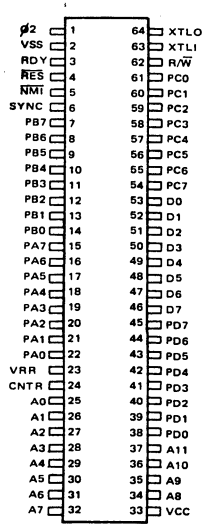
The NCR 6500/1 is a complete, high-performance 8-bit microcomputer on a single chip. It is software compatible with all members of the 6502 and 6500 families. The NCR 6500/1 consists of a 6502 CPU, an internal clock oscillator, 2048 bytes of ROM, 64 bytes of RAM and versatile interface circuitry. The interface circuitry includes a 16-bit programmable counter / latch, 32 bidirectional I/O lines (including 2 edge-sensitive lines), 5 interrupts and 1 counter I/O line.

To aid in designing NCR 6500/1 microcomputer systems, NCR offers a ROM-less PROM-compatible emulator device, the NCR 6500/1E. The architecture of the emulator device is the same as that of the NCR 6500/1, except that the NCR 6500/1E provides 24 additional signals to route the address bus (12 lines), the data bus (8 lines), and control signals (4 lines) off the chip for connection to memory.

PIN CONFIGURATION

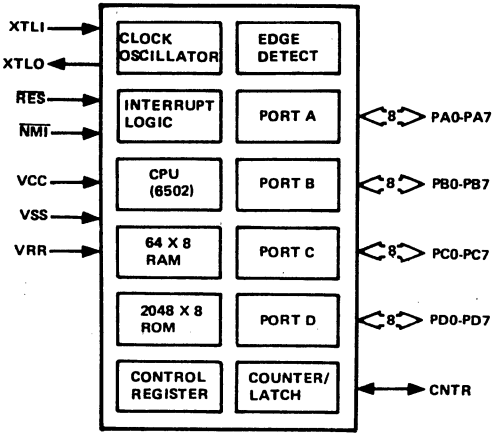


NCR6500/1



NCR6500/1E

FUNCTIONAL BLOCK DIAGRAM



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NCR

PIN DESCRIPTIONS

Pin Name	Pin Number	Description
VCC	30	Main power supply +5V
VRR	1	Separate power pin for RAM. In the event that VCC power is lost, this power retains RAM data.
VSS	12	Signal ground
XTLI	10	Crystal, clock or RC network input for internal clock oscillator.
XTLO	11	Crystal or RC network ouput from internal clock oscillator.
$\overline{RES}$	39	The Reset input is used to initialize the NCR6500/1. This signal must not transition from low to high for at least eight cycles after VCC reaches operating range and the internal oscillator has stabilized.
$\overline{NMI}$	40	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0-PA7 PB0-PB7 PC0-PC7 PD0-PD7	38-31 29-22 20-13 9-2	Four 8-bit ports used for either input/output. Each line consists of an active transistor to VSS and a passive pull-up to +5V. The two lower bits of the PA port (PA0 and PA1) also serve as edge detect inputs with maskable interrupts.
CNTR	21	This line is used as a Counter input/output line. CNTR is an input in the Event Counter and Pulse Width Measurement modes and is an output in the Interval Timer and Pulse Generator modes.

NOTE: All NCR 6500/1 interface signals are provided in the NCR 6500/1E. While the interface electrical characteristics are identical, the NCR 6500/1E pin assignments are different from the NCR 6500/1 in order to accomodate the 64-pin emulator package.

ADDITIONAL NCR 6500/1E PIN DESCRIPTIONS

Pin Name	Pin Number	Description
RDY	3	Ready. The Ready input delays execution of any cycle during which the RDY line is low. This allows the user to halt or single step the CPU on any cycle except a write cycle. A negative transition to the low state during the $\phi 2$ clock low pulse will halt the CPU with the address lines containing the current address being fetched. If RDY is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent $\phi 2$ clock pulse in which the RDY line is low.
SYNC	6	Sync. The Sync signal is provided to identify those cycles in which the CPU is performing an OP CODE fetch. SYNC goes high during $\phi 2$ clock-low pulse during an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the $\phi 2$ clock low pulse in which SYNC went high, the CPU will halt in its current state and will remain in that state until the RDY line goes high. Using this technique, the SYNC signal can be used to control RDY to cause single instruction execution.
$\phi 2$	1	Phase 2 ($\phi 2$) clock pulse. Data transfer can take place only during $\phi 2$ clock pulse.
A0-A11	25-32 34-37	Address Bus Lines. The address bus buffers on the NCR6500/1E are push/pull type drivers capable of driving at least 130 pf and one standard TTL load. The address bus always contains known data. The addressing technique involves putting an address on the address bus which is known to be either in program sequence, on the same page in program memory, or at a known point in memory. The I/O addresses are also placed on these lines.
D0-D7	53-46	Data Bus Lines. All transfers of instructions and data between the CPU and external memory take place on the data bus lines. The buffers driving the data bus lines have full three-state capability. Each data bus pin is connected to an input and an output buffer, with the output buffer remaining in the floating condition.
R/W	62	Read/Write. The Read/Write output controls the direction of data transfer between the NCR6500/1E Emulator CPU and external memory. This line is high when reading data from memory and low when writing data to memory.

DEVICE OPERATION

CENTRAL PROCESSING UNIT (CPU)

The CPU in the NCR 6500/1 and NCR 6500/1E is a standard 6500 configuration with the standard 6500 instructions. All instructions are executed in 2 to 7 clock cycles. The automatic increment/decrement feature of the stack pointer facilitates rapid and flexible subroutine execution and interrupt servicing, including context switching. Two 8-bit index registers permit pre- and post-indexing of indirect addresses. (For details on the CPU operation, see NCR 6500/1 and NCR 6500/1E Data Sheet, Publication Number MC—700).

READ ONLY MEMORY (ROM)

The ROM for the NCR 6500/1 consists of 2048 by 8 bits of mask-programmable memory with an address space from 800 to FFF. The NCR 6500/1E has no ROM.

RANDOM ACCESS MEMORY (RAM)

The RAM for the NCR 6500/1 and NCR 6500/1E consists of 64 by 8 bits of read/write memory. In order to take advantage of efficient zero page addressing capabilities, the RAM is assigned addresses 0 to 03F. A standby power pin, VRR allows RAM memory to be maintained at less than 10% of the operating power in the event that VCC power is lost.

CLOCK OSCILLATOR

The clock oscillator provides the basic timing signals used by the CPU. The reference frequency is provided by an external source, and can be from a crystal, clock or RC network input. The RC network mode is a mask option. (The external frequency reference of the NCR 6500/1E may be a crystal or a clock; the RC option is not available on this emulator device.) The external frequency can vary from 200 KHz to 4 MHz. The internal Phase 2 ($\phi 2$) frequency is one-half the external reference frequency. A 4.7K ohm resistor will provide nominal 2 MHz oscillation and 1 MHz internal operation in the RC mask option ± 35%).

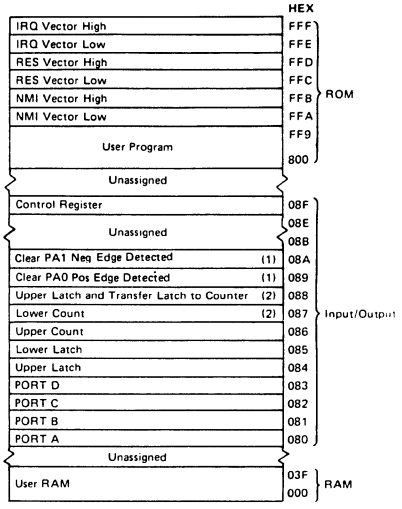
BIDIRECTIONAL I/O PORTS

The NCR 6500/1 and NCR 6500/1E provide four 8-bit I/O ports (PA, PB, PC, and PD). Associated with the I/O ports are four 8-bit registers located on page zero. (See System Memory Maps for specific addresses.) Each I/O line is individually selectable as an input or an output.

COUNTER / LATCH

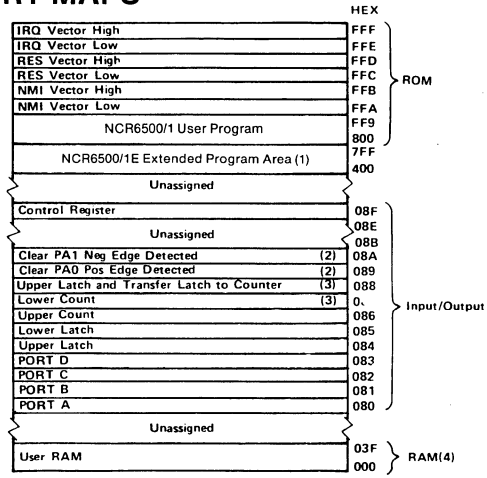
The Counter / Latch consists of a 16-bit decrementing counter and a 16-bit latch. The counter and the latch are each comprised of two 8-bit registers. The counter operates in any of four modes: Interval Timer, Pulse Generator, Event Counter, or Pulse Width Measurement.

DETAILED MEMORY MAPS



Notes:
(1) I/O command only; i.e., no stored data.
(2) Clears Counter Overflow – Bit 7 in Control Register.

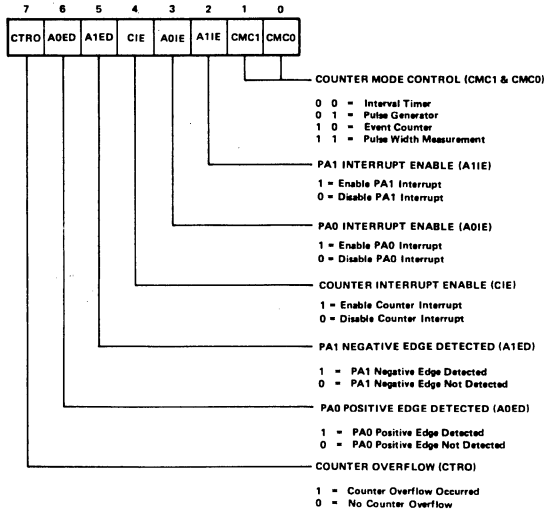
NCR 6500/1



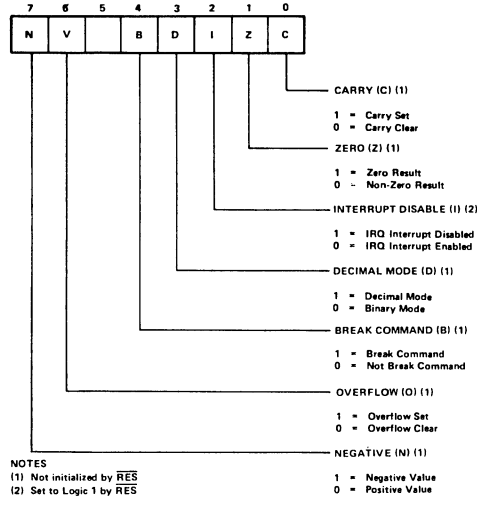
NOTES
(1) Additional 1024 bytes are decoded for external memory addressing by the NCR6500/1E Emulator Device. This area can be used during debug, but cannot be used in a masked ROM NCR6500/1.
(2) I/O command only; i.e., no stored data.
(3) Clears Counter Overflow - Bit 7 in Control Register.
(4) CAUTION: The NCR6500/1E allows RAM mapping into o40-07F, 100-13F, 140-17F, 200-23F, 240-27F, 300-33F, and 340-37F; as well as 000-03F. The production NCR6500/1, however allows RAM mapping only at 000-03F.

NCR 6500/1E

KEY REGISTER SUMMARY



Control Register



NOTES
(1) Not initialized by $\overline{RES}$
(2) Set to Logic 1 by $\overline{RES}$

Processor Status Register

ELECTRICAL SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{in}	−0.3 to +7.0	Vdc
Operating Temperature Range	T_A		°C
Commercial		0 to +70	
Industrial		−40 to +85	
Storage Temperature Range	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

D.C. CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Dissipation (Outputs High)	P_D				mW
0°C to +70°C (NCR 6500/1)		—	500	—	
−40°C to +85°C (NCR 6500/1)		—	550	—	
0°C to +70°C (NCR 6500/1E)		—	750	1200	
RAM Standby Voltage (Retention Mode)	V_{RR}	3.5	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode)	I_{RR}				mAdc
0°C to +70°C		—	10	—	
−40°C to +85°C		—	12	—	
Input High Voltage (PA, PB, PC, CNTR, $\overline{RES}$, $\overline{NMI}$)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage (PA, PB, PC, CNTR, $\overline{RES}$, $\overline{NMI}$)	V_{IL}	−0.3	—	+0.8	Vdc
Input Leakage Current	I_{IN}				μAdc
V_{in} = 0 to 5.0 Vdc				±10	
$\overline{RES}$, $\overline{NMI}$					
Input High Voltage (XTLI)	V_{IHXT}	+4.0	—	V_{CC}	Vdc
Input Low Voltage (XTLI)	V_{ILXT}	−0.3	—	+0.8	Vdc
Input Low Current	I_{IL}				
(V_{IL} = 0.4 Vdc)		—	−1.0	−1.6	mAdc
Output High Voltage	V_{OH}				
(V_{CC} = min, I_{Load} = −100 uAdc)		−2.4	—	—	Vdc
Output High Voltage	V_{CMOS}	V_{CC}−30%	—	—	Vdc
(V_{CC} = min)					
Output Low Voltage	V_{OL}				
(V_{CC} = min, I_{Load} = 1.6 mAdc)		—	—	+0.4	Vdc
Output High Current (Sourcing)	I_{OH}				
(V_{OH} = 2.4 Vdc)		−100		—	μAdc
Output Low Current (Sinking)	I_{OL}				
(V_{OL} = 0.4 Vdc)		1.6	—	—	mAdc
Input Capacitance	C_{in}				pF
(V_{in} -0, T_A = 25°C, f = 1.0 MHz)					
PA, PB, PC, PD CNTR		—	—	10	
XTLI, XTLO		—	—	50	
Output Capacitance	C_{out}				
(V_{in} -0, T_A = 25°C, f = 1.0 MHz)		—	—	10	pF
I/O Port Pull-up Resistance (Optional)	R_L	3.0	6.0	11.5	KΩ
PA0-PA7, PB0-PB7, PC0-PC7,					
PD0-PD7, CNTR					

NOTE: Negative sign indicates outward current flow, positive indicates inward flow. Unless otherwise indicated, characteristic refers to PA, PB, PC, PD and CNTR signals.

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
XTLI Input Clock Cycle Time	T_{cyc}	0.500	5.0	0.250	5.0	μ sec
Internal Write to Peripheral Data Valid (TTL)	T_{PDW}	1.0		0.5		μ sec
Internal Write to Peripheral Data Valid (CMOS)	T_{CMOS}	2.0		1.0		μ sec
Peripheral Data Setup Time	T_{PDSU}	400		200		nsec
Count and Edge Detect Pulse Width	T_{PW}	1.0		0.5		μ sec

NCR 6500/1E ELECTRICAL SPECIFICATIONS

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Threshold Voltage D0-D7, RDY,	V_{IHT}	V_{SS} + 2.4	–	–	Vdc
Input Low Threshold Voltage D0-D7, RDY,	V_{ILT}	–	–	V_{SS} + 0.8	Vdc
Three-State (Off State) Input Current (V = 0.4 to 2.4V, V_{CC} = 5.25V) D0-D7	I_{TSI}	–	–	10	μA
Output High Voltage (I_{LOAD} = 100μ Adc, V_{CC} = 4.75V) D0-D7, SYNC, A0-A11, R/$\overline{W}$, φ2	V_{OH}	V_{SS} + 2.4	–	–	Vdc
Output Low Voltage (I_{LOAD} = 1.6 mAdc, V_{CC} = 4.75V) D0-D7, SYNC, A0-A11, R/$\overline{W}$, φ2	V_{OL}	–	–	V_{SS} + 0.6	Vdc
Capacitance (V_{in} = 0, T_A = 25°C, f = 1 MHz) RDY D0-D7 A0-A11, R/$\overline{W}$, SYNC φ2	C C_{in} C_{out} $C_{\phi 2}$	 – – – –	 – – – 50	 10 15 12 80	pF

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6500/11, 6500/12, 6500/13 and 6500/11E
SINGLE-CHIP MICROCOMPUTER

- Enhanced 6502 CPU
  - 8-bit pipelined architecture
  - 4 new bit manipulation instructions (set memory bit, reset memory bit, branch on bit set, branch on bit reset)
  - 13 addressing modes
  - Decimal and binary arithmetic
  - True indexing capability
- Up to 3K bytes mask-programmable ROM
- 192-byte static RAM (12 mW standby power for 32 bytes)
- Up to 56 bidirectional, TTL - compatible I/O lines
- 2 16-bit programmable counter / timers with latches, each with 4 independent operating modes
- Up to four external bus modes for expansion
- Serial port
  - Full duplex, buffered UART
  - Receiver wake-up and transmitter end of transmission features
  - Synchronous shift register alternate mode (250 KHz @ 2MHz)
- 10 interrupts, 4 internal and 6 external
- 68% of instructions have execution times less than 2 μs @ 2 MHz
- 3 μm. NMOS silicon gate, depletion load technology
- Single +5V power supply
- Emulator device available (NCR 6500/11E)

The NCR 6500/11, NCR 6500/12, NCR 6500/13 and NCR 6500/11E are each complete, high-performance 8-bit microcomputers on a single chip. All four models contain an enhanced 6502 CPU, an internal clock oscillator, 192 bytes of RAM, and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters; at least 32 bidirectional I/O lines (including four edge-sensitive lines and input latching on one 8-bit port); a full-duplex serial I/O channel; 10 interrupts; and bus expandability.

The NCR 6500/11 has 3072 bytes of ROM and four 8-bit I/O ports. The NCR 6500/12 also has 3072 bytes of ROM, plus three additional 8-bit ports. The NCR 6500/13 contains 256 bytes of ROM, four 8-bit I/O ports, plus a full 16-bit address bus and 8-bit data bus to access 64K bytes of external memory. The NCR 6500/13 may be used in multichip systems as a CPU—RAM—I/O counter device that includes 256 bytes of bootstrap ROM. The NCR 6500/11E has all the features of the NCR 6500/13 except that it has no ROM and can thus be used as an emulator device for the NCR 6500/11 family of microcomputers.

FAMILY DIFFERENCES

MODEL	ON-CHIP ROM	EXPANSION BUS	I/O LINES
NCR 6500/11	3K bytes	Access to 16K bytes via multiplexed I/O ports	32
NCR 6500/12	3K bytes	Access to 16K bytes via multiplexed I/O ports	56
NCR 6500/13	256 bytes	Access to additional 64K bytes via address bus and data bus	32
NCR 6500/11E	None	Access to additional 64K bytes via address bus and data bus	32

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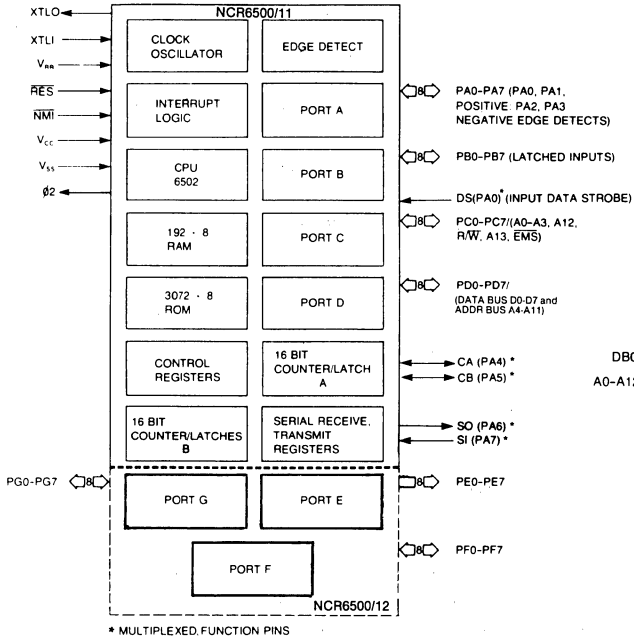
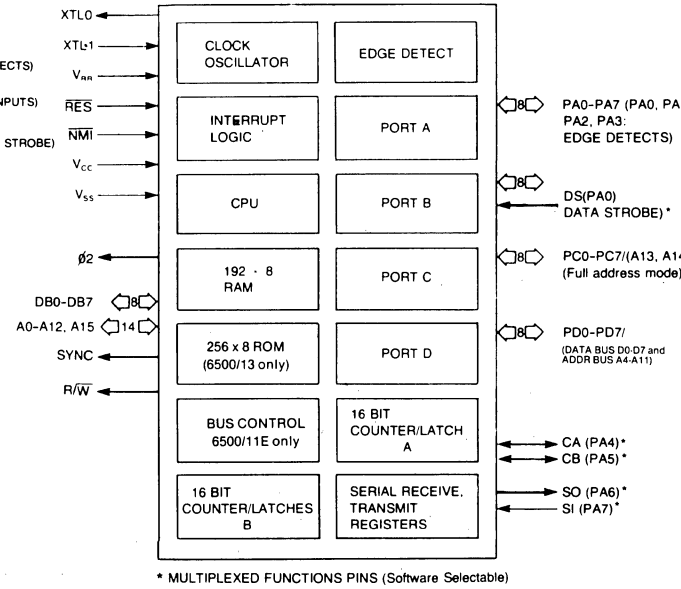
NCR

FUNCTIONAL BLOCK DIAGRAMS

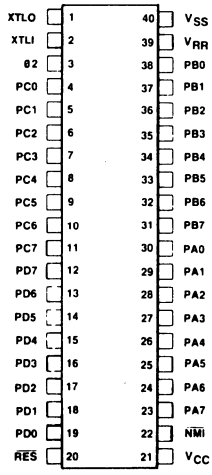


NCR 6500/11 & NCR 6500/12



NCR 6500/13 & NCR 6500/11E

PIN CONFIGURATION



NCR6500/11 Pin Out

PIN DESCRIPTIONS

PIN	DESCRIPTION
VCC	Main Power Supply + 5V.
VRR	Separate power pin for RAM. In the event that VCC power is lost, this power retains the lowest 32 bytes of RAM data.
VSS	Signal and power ground (0V).
XTLI	Crystal or clock input for internal clock oscillator. Also allows input of X1 clock signal if XTLO is connected to VSS, or X2, or X4 clock if XTLO is floated.
XTLO	Crystal output from internal clock oscillator.
$\overline{RES}$	The Reset input is used to initialize the microcomputer. This signal must not transition from low to high for at least eight cycles after VCC reaches operating range and the internal oscillator has stabilized.
ø2	Clock signal output at internal frequency.
$\overline{NMI}$	A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU.
PA0-PA7 PB0-PB7 PC0-PC7 PD0-PD7	Four 8-bit ports used for either input or outputs. Each line of Ports A, B, and C consist of an active transistor to VSS and an optional pullup to VCC. In the abbreviated or multiplexed modes of operation, Port C has active pull-up transistors. Port D functions as either an 8-bit input or 8-bit output port. It has active pull-up and pull-down transistors.
SYNC	A positive going signal for the full clock cycle whenever the CPU is performing an op code fetch. Available on the NCR 6500/13 and NCR 6500/11E only.
R/$\overline{W}$	Dedicated read/write output line for NCR 6500/13 and NCR 6500/11E. Controls the direction of data transfer between the CPU and the external 64K address space. R/$\overline{W}$ is available on NCR 6500/11 and NCR 6500/12 via Port C operating in abbreviated or multiplexed mode.
A0-A12, A15	Fourteen dedicated address bus lines for NCR 6500/13 and NCR 6500/11E are used to address external memory. Note that A13 and A14 are sourced through PC6 and PC7, respectively, when in full address mode. (Some of these lines are available on the NCR 6500/11 and NCR 6500/12 via Port C operations in abbreviated mode and Port C and Port D operating in multiplexed mode.)
DB0-DB7	Eight dedicated data bus lines for NCR 6500/13 and NCR 6500/11E used to transmit data to and from external memory. These lines are also available on NCR 6500/11 and NCR 6500/12 via Port D operating in abbreviated or multiplexed mode.
PE0-PE7 PF0-PF7 PG0-PG7	Additional ports available on NCR 6500/12. Port E may be used as an output port only. Ports F and G can be configured to be inputs or outputs in any combination.

DEVICE OPERATION

CENTRAL PROCESSING UNIT (CPU)

The 6502 CPU in each of these four microcomputers executes instructions in 2 to 7 clock cycles. The automatic increment/decrement feature of the stack pointer facilitates rapid and flexible subroutines and interrupts, including context switching. Two 8-bit index registers permit pre- and post indexing of indirect addresses. (For details on the CPU operation, see NCR 6500/11 - 13 Data Sheet, Publication No. MC - 701.) The standard 6502 instruction set is available in each model; additionally, four new bit manipulation instructions have been added to improve memory utilization efficiency and performance. These bit manipulation instructions include:

- **Set Memory Bit (SMB)** - This instruction sets to "1" one bit of the 8-bit data field specified by the zero page address (memory or I/O port.) The first byte of the instruction specifies the SMB operation and which one of 8 bits is to be set. The second byte of the instruction designates the address (0-255) of the byte to be operated upon.
- **Reset Memory Bit (RMB)** - The RMB instruction is the same operation and in the same format as the SMB instruction, except a reset to "0" of the bit results.
- **Branch on Bit Set Relative (BBS)** - This instruction tests one of 8-bits designated by a 3-bit immediate field within the first byte of the instruction. The second byte is used to designate the location of the byte to be tested within the zero page address range (memory of I/O ports). The third byte of the instruction is used to specify the 8-bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.
- **Branch on Bit Reset Relative (BBR)** - This instruction is the same operation and in the same format as the BBS instruction except that a branch takes place if the bit tested is a "0".

READ ONLY MEMORY (ROM)

The ROM for the NCR 6500/11 and NCR 6500/12 consists of 3072 by 8-bits (3K) of mask-programmable memory with an address space from F400 to FFFF. ROM locations FFFA through FFFF are assigned to interrupt and reset vectors. The ROM for the NCR 6500/13 consists of 256 by 8 bits of mask-progammable memory with an address space from 7F00 to 7FFF. Address locations FFFA, FFFB, FFFE and FFFF are assigned to interrupt vectors. The reset vector is assigned to memory locations FFFC and FFFD. For the NCR 6500/13, the reset vector can be optionally assigned to these locations, but is normally at memory locations 7FFE and 7FFF. The NCR 6500/11E has no ROM.

RANDOM ACCESS MEMORY (RAM)

The RAM consists of 192 by 8 bits of read/write memory with an assigned page zero address of 0040 through 00FF. A separate power pin (VRR) may be used for standby power. In the event of the loss of VCC power, the lowest 32 bytes of RAM data will be retained if standby power is supplied to the VRR pin.

CLOCK OSCILLATOR

The clock oscillator provides the basic timing signals. The reference frequency can be generated with the on board oscillator (with external crystal) or an external source can be driven into the XTLI pin. If the XTLO pin is left floating, the reference frequency is internally divided by two (divide by four is a mask option) to obtain the internal clock. The internal clock is then available as an output at the Ø2 pin. The XTLI pin may be used as an undivided clock input by connecting XTLO to VSS, in which case the internal division circuitry is bypassed and the device operates at the reference frequency.

MODE CONTROL REGISTER (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for Counter A and Counter B.

PARALLEL INPUT/OUTPUT PORTS

The NCR 6500/11, NCR 6500/13 and NCR 6500/11E have 32 I/O lines grouped into four 8-bit ports (PA, PB, PC and PD). The NCR 6500/12 has 56 I/O lines grouped into seven 8-bit ports (PA, PB, PC, PD, PE, PF and PG).

- **Port A (PA)** - Port A can be programmed via the Mode Control and the Serial Communications Control Register as a standard parallel 8-bit, bit-independent I/O port or as serial channel I/O lines, counter I/O lines, or an input data strobe for the Port B input latch option. In addition to their normal I/O functions, PA0 and PA1 can detect positive going edges, and PA2 and PA3 can detect negative going edges.

- **Port B (PB)** - Port B can be programmed as an 8-bit, bit-independent I/O port. It has a latched input capability which may be enabled or disabled via the Mode Control Register.
- **Port C and Port D (PC and PD)** - Port C can be programmed in one of three modes. The first mode is as an 8-bit, bit-independent I/O port. A second mode uses Port D in conjunction with the Mode Control Register as an abbreviated bus to address an additional 64K bytes of nonmultiplexed address and data space. In a third mode Port C uses Port D to effect a multiplexed bus which addresses an additional 16K bytes of multiplexed address and data space.

  Port D can be programmed as an I/O port, an 8-bit tri-state data bus, or as a multplexed bus. Mode selection for Port D is made by the Mode Control Register.

  In addition to the I/O modes of the NCR 6500/11 and NCR 6500/12, the NCR 6500/13 and NCR 6500/11E have an additional full address mode which allows emulation of the NCR 6500/11 or addressing of up to 64K bytes of memory.
- **Ports E,F,G (PE, PF, PG)** - Port E may be used for output only. PF and PG can be configured to be inputs or outputs in any combination.

SERIAL I/O CHANNEL — UART

Each microcomputer model provides a full-duplex asynchronous serial I/O channel with programmable baud rates covering all standard baud rates from 50 to 125K bits/sec, including the SMPTE 422 Standard at 38.4K bits/sec. Character lengths of 5 to 8 bits, with or without parity, are programmable. A full complement of flags provides for Receiver Wake-Up; Receiver Buffer Full; Receiver Error Conditions detecting Framing, Parity and Overrun errors; Transmitter End of Transmission and Transmitter Buffer Empty. In addition, a synchronous shift register mode to 250 KHz @ 2 MHz is available.

WAKE-UP FEATURE

In a multidistributed microcomputer application, a destination address is usually included at the beginning of the message. The wake-up feature allows non-selected CPU's to ignore the remainder of the message until the beginning of the next message by setting the wake-up bit.

COUNTER/LATCH LOGIC

Each microcomputer model contains two 16-bit counters and three 16-bit latches associated with the counters. Counter A has one 16-bit latch and Counter B has two 16-bit latches. Each counter can be indepently programmed to operate in one of four modes:

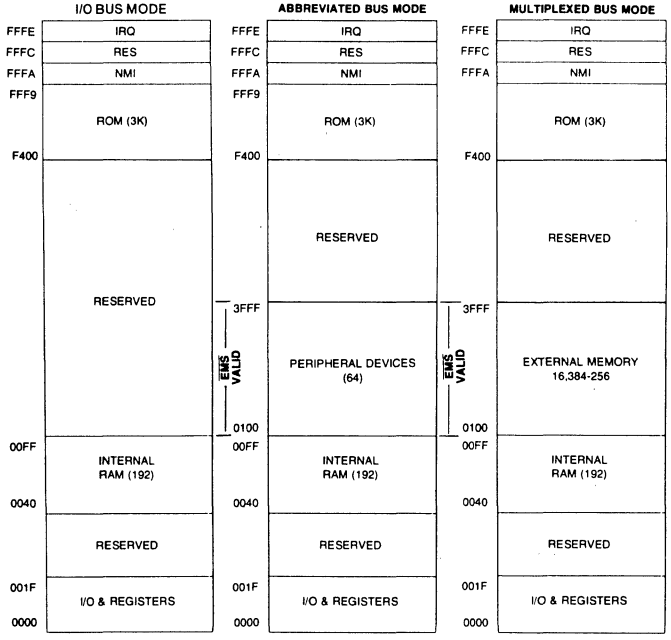
Counter A	Counter B
— Pulse Width Measurement	— Retriggerable Interval Counter
— Pulse Generation	— Asymetrical Pulse Generation
— Interval Timer	— Interval Timer
— Event Counter	— Event Counter

INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

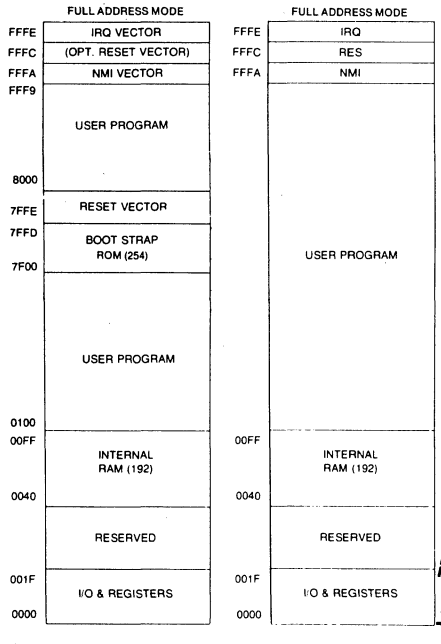
Each microcomputer model includes an IFR and IER which flags and controls I/O and counter status. Each model has ten interrupts: four edge-sensitive lines, two counter underflows, a serial data received, a serial data transmitted, a non-maskable interrupt, and a reset interrupt.

SYSTEM MEMORY MAPS

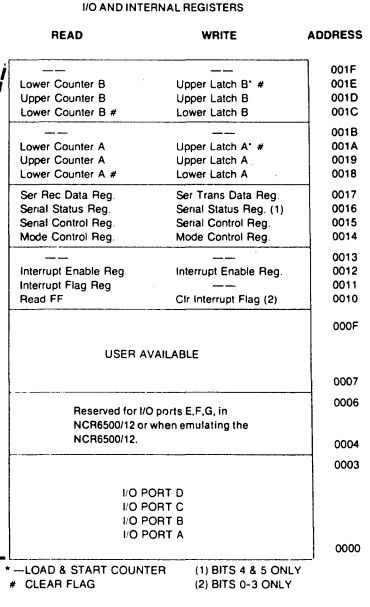
NCR 6500/11 and NCR 6500/12



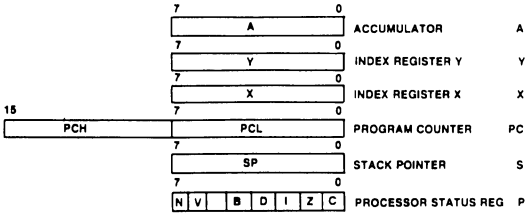
For additional details on the NCR 6500/13 and /11E, see Pub. No. MC-701.



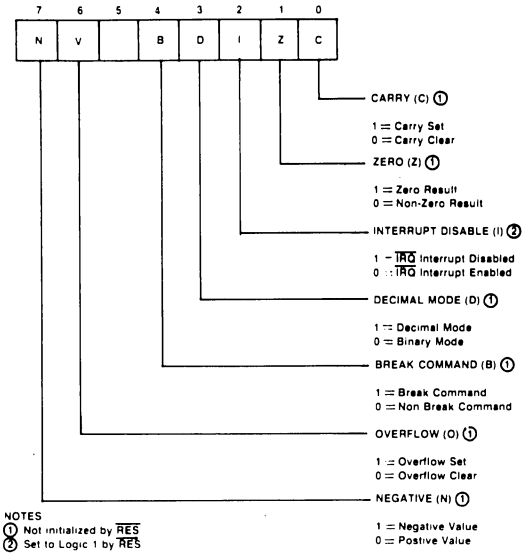
NCR 6500/13 NCR 6500/11E



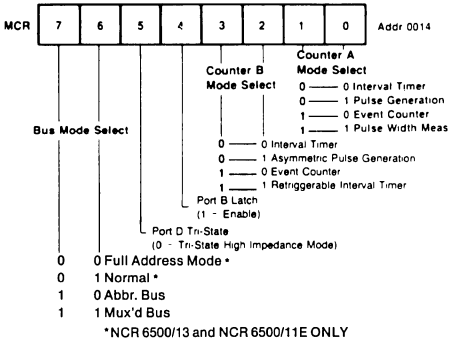
KEY REGISTER SUMMARY



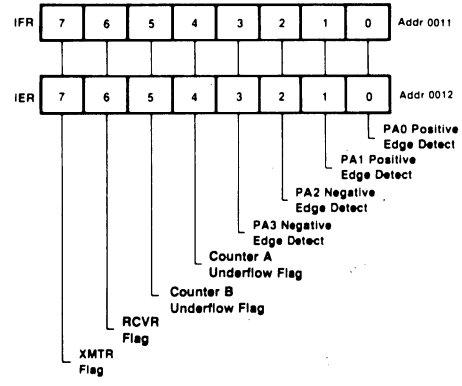
CPU Registers



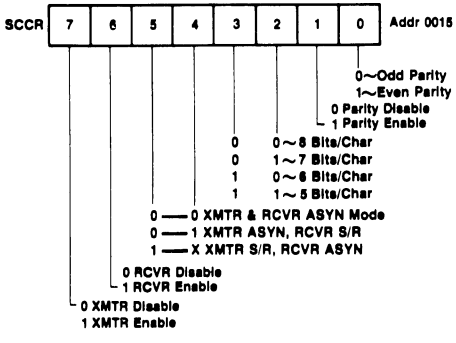
Processor Status Register



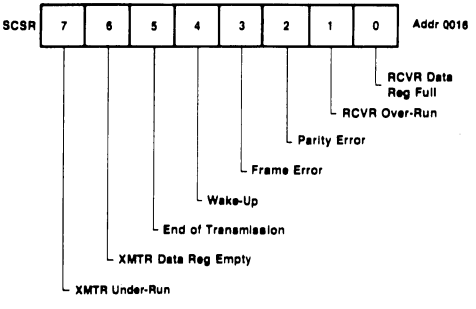
Mode Control Register



Interrupt Enable and Flag Registers



Serial Communications Control Register



Serial Communications Status Register

ELECTRICAL SPECIFICATIONS

Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC} & V_{RR}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range, Commercial	T	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

D.C. Characteristics (V_{CC} = 5V ±5% V_{SS} = 0)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Power Dissipation (Outputs High) Commercial @ 25°C	P_D	—		1200	mW
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode) Commercial @ 25°C	I_{RR}	—	4	—	mAdc
Input High Voltage Except XTLI	V_{IH}	+2.0	—	V_{CC}	Vdc
Input High Voltage (XTLI)	V_{IH}	+4.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	-0.3	—	+0.8	Vdc
Input Leakage Current ($\overline{RES}$, $\overline{NMI}$) V_{in} = 0 to 5.0 Vdc	I_{IN}	—	—	±10	μAdc
Input Low Current PA, PB, PC, PF, and PG (V_{IL} = 0.4 Vdc)	I_{IL}	—	-1.0	-1.6	mAdc
Output High Voltage Except XTLO (I_{Load} = -100 μAdc)	V_{OH}	+2.4	—	V_{CC}	Vdc
Output Low Voltage (I_{Load} = 1.6 mAdc)	V_{OL}	—	—	+0.4	Vdc
Darlington Current Drive, PE (V_o = 1.5 Vdc)	I_{OH}	1.0	—	—	mAdc
Output Low Voltage, PE (I_{Load} = 1.6 mAdc sink)	V_{OL}	—	—	+0.4	Vdc
Input Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz) PA, PB, PC, PD, PF, and PG XTLI, XTLO	C_{in}	— —	— —	10 50	pF
I/O Port Pull-Up Resistance PA0-PA7, PB0-PB7, PC0-PC7, PF0-PF7 & PG0-PG7	R_L	3.0	6.0	11.5	KΩ

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

AC CHARACTERISTICS (V_{CC} = 5V ± 5% V_{SS} = 0)

PARAMETER	SYMBOL	1 MHz MIN	1 MHz MAX	2 MHz MIN	2 MHz MAX	UNIT
XTLI Input Clock Cycle Time	T_{cyc}	1.0	10.0	0.500	10.0	μ sec
Internal Write to Peripheral Data Valid (TTL)	T_{PDW}	1.0		0.5		μ sec
Peripheral Data Setup Time	T_{PDSU}	500		500		nsec
Count and Edge Detect Pulse Width	T_{PW}	1.0		0.5		μ sec

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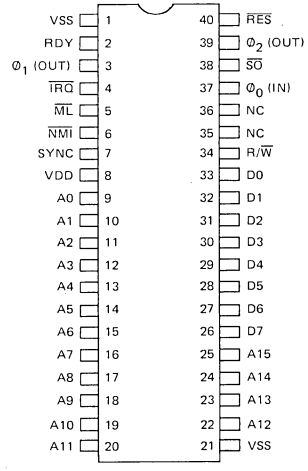
NCR 65C02

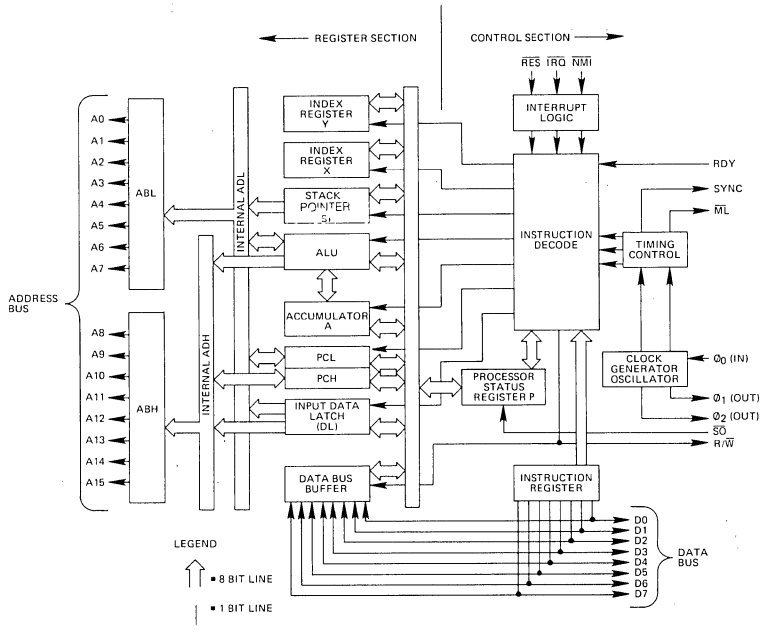
- Enhanced software performance including 27 additional OP codes encompassing ten new instructions and two additional addressing modes.
- 66 microprocessor instructions.
- 15 addressing modes.
- 178 operational codes.
- 1MHz, 2MHz operation.
- Operates at frequencies as low as 200 Hz for even lower power consumption (pseudo-static: stop during $\emptyset_2$ high).
- Compatible with NMOS 6500 series microprocessors.
- 64 K-byte addressable memory.
- Interrupt capability.
- Lower power consumption. 4mA @ 1MHz.
- +5 volt power supply.
- 8-bit bidirectional data bus.
- Bus Compatible with M6800.
- Non-maskable interrupt.
- 40 pin dual-in-line packaging.
- 8-bit parallel processing
- Decimal and binary arithmetic.
- Pipeline architecture.
- Programmable stack pointer.
- Variable length stack.
- Optional internal pullups for (RDY, $\overline{IRQ}$, $\overline{SO}$, $\overline{NMI}$ and $\overline{RES}$)

The NCR CMOS 6502 is an 8-bit microprocessor which is software compatible with the NMOS 6502. The NCR65C02 hardware interfaces with all 6500 peripherals. The enhancements include ten additional instructions, expanded operational codes and two new addressing modes. This microprocessor has all of the advantages of CMOS technology: low power consumption, increased noise immunity and higher reliability. The CMOS 6502 is a low power high performance microprocessor with applications in the consumer, business, automotive and communications market.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



* Specifications are subject to change without notice.

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■ ABSOLUTE MAXIMUM RATINGS:

(V_{DD} = 5.0 V ± 5%, V_{SS} = 0 V, T_A = 0° to + 70°C)

RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	V_{DD}	−0.3 to +7.0	V
INPUT VOLTAGE	V_{IN}	−0.3 to +7.0	V
OPERATING TEMP.	T_A	0 to + 70	°C
STORAGE TEMP.	T_{STG}	−55 to + 150	°C

■ PIN FUNCTION

PIN	FUNCTION
A0 - A15	Address Bus
D0 - D7	Data Bus
$\overline{IRQ}$ *	Interrupt Request
RDY *	Ready
$\overline{ML}$	Memory Lock
$\overline{NMI}$ *	Non-Maskable Interrupt
SYNC	Synchronize
$\overline{RES}$ *	Reset
$\overline{SO}$ *	Set Overflow
NC	No Connection
R/$\overline{W}$	Read/Write
VDD	Power Supply (+5V)
VSS	Internal Logic Ground
$\emptyset_0$	Clock Input
$\emptyset_1, \emptyset_2$	Clock Output

*This pin has an optional internal pullup for a No Connect condition.

■ DC CHARACTERISTICS

	SYMBOL	MIN.	TYP.	MAX	UNIT
Input High Voltage					
$\emptyset_0$ (IN)	V_{IH}	V_{SS} + 2.4	–	V_{DD}	V
Input High Voltage					
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O.		V_{SS} + 2.0	–	–	V
Input Low Voltage					
$\emptyset_0$ (IN)	V_{IL}	V_{SS} −0.3	–	V_{SS} + 0.4	V
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O.		–	–	V_{SS} + 0.8	V
Input Leakage Current					
(V_{IN} = 0 to 5.25V, V_{DD} = 5.25V)	I_{IN}				
With pullups		-30	–	+30	μA
Without pullups		–	–	+1.0	μA
Three State (Off State) Input Current					
(V_{IN} = 0.4 to 2.4V, V_{CC} = 5.25V)					
Data Lines	I_{TSI}	–	–	10	μA
Output High Voltage					
(I_{OH} = −100 μAdc, V_{DD} = 4.75V					
SYNC, Data, A0-A15, R/W)	V_{OH}	V_{SS} + 2.4	–	–	V
Out Low Voltage					
(I_{OL} = 1.6mAdc, V_{DD} = 4.75V					
SYNC, Data, A0-A15, R/W)	V_{OL}	–	–	V_{SS} + 0.4	V
Supply Current f = 1MHz	I_{DD}	–	–	4	mA
Supply Current f = 2MHz	I_{DD}	–	–	8	mA
Capacitance	C				pF
(V_{IN} = 0, T_A = 25°C, f = 1MHz)					
Logic	C_{IN}	–	–	5	
Data		–	–	10	
A0-A15, R/W, SYNC	Cout	–	–	10	
$\emptyset_0$ (IN)	$C\emptyset_0$ (IN)	–	–	10	

■ AC CHARACTERISTICS V_{DD} = 5.0V ± 5%, T_A = 0°C to 70°C, Load = 1 TTL + 130 pF

		1MHz		2MHz		3MHz		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Delay Time, $\emptyset_0$ (IN) to $\emptyset_2$ (OUT)	t_{DLY}	–	60	–	60	20	60	nS
Delay Time, $\emptyset_1$ (OUT) to $\emptyset_2$ (OUT)	t_{DLY1}	–20	20	–20	20	–20	20	nS
Cycle Time	t_{CYC}	1.0	5000*	0.50	5000*	0.33	5000*	μS
Clock Pulse Width Low	t_{PL}	460	–	220	–	160	–	nS
Clock Pulse Width High	t_{PH}	460	–	220	–	160	–	nS
Fall Time, Rise Time	t_F, t_R	–	25	–	25	–	25	nS
Address Hold Time	t_{AH}	20	–	20	–	0	–	nS
Address Setup Time	t_{ADS}	–	225	–	140	–	110	nS
Access Time	t_{ACC}	650	–	310	–	170	–	nS
Read Data Hold Time	t_{DHR}	10	–	10	–	10	–	nS
Read Data Setup Time	t_{DSU}	100	–	60	–	60	–	nS
Write Data Delay Time	t_{MDS}	–	30	–	30	–	30	nS
Write Data Hold Time	t_{DHW}	20	–	20	–	15	–	nS
$\overline{SO}$ Setup Time	t_{SO}	100	–	100	–	100	–	nS
Processor Control Setup Time**	t_{PCS}	200	–	150	–	150	–	nS
SYNC Setup Time	t_{SYNC}	–	225	–	140	–	100	nS
$\overline{ML}$ Setup Time	t_{ML}	–	225	–	140	–	100	nS
Input Clock Rise/Fall Time	$t_{F\emptyset o}$, $t_{R\emptyset o}$	–	25	–	25	–	25	nS

*NCR65C02 can be held static with $\emptyset_2$ high.

**This parameter must only be met to guarantee that the signal will be recognized at the current clock cycle.

■ MICROPROCESSOR OPERATIONAL ENHANCEMENTS

Function	NMOS 6502 Microprocessor	NCR65C02 Microprocessor
Indexed addressing across page boundary.	Extra read of invalid address.	Extra read of last instruction byte.
Execution of invalid op codes.	Some terminate only by reset. Results are undefined.	All are NOPs (reserved for future use). Op Code / Bytes / Cycles X2 / 2 / 2 X3, X7, XB, XF / 1 / 1 44 / 2 / 3 54, D4, F4 / 2 / 4 5C / 3 / 8 DC, FC / 3 / 4
Jump indirect, operand = XXFF.	Page address does not increment.	Page address increments and adds one additional cycle.
Read/modify/write instructions at effective address.	One read and two write cycles.	Two read and one write cycle.
Decimal flag.	Indeterminate after reset.	Initialized to binary mode (D=0) after reset and interrupts.
Flags after decimal operation.	Invalid N, V and Z flags.	Valid flag adds one additional cycle.
Interrupt after fetch of BRK instruction.	Interrupt vector is loaded, BRK vector is ignored.	BRK is executed, then interrupt is executed.

■ MICROPROCESSOR HARDWARE ENHANCEMENTS

Function	NMOS 6502	NCR65C02
Assertion of Ready RDY during write operations.	Ignored.	Stops processor during $\emptyset_2$.
Unused input-only pins ($\overline{IRQ}$, $\overline{NMI}$, RDY, $\overline{RES}$, $\overline{SO}$).	Must be connected to low impedance signal to avoid noise problems.	Connected internally by a high-resistance to V_{DD} (approximately 250 K ohm.)

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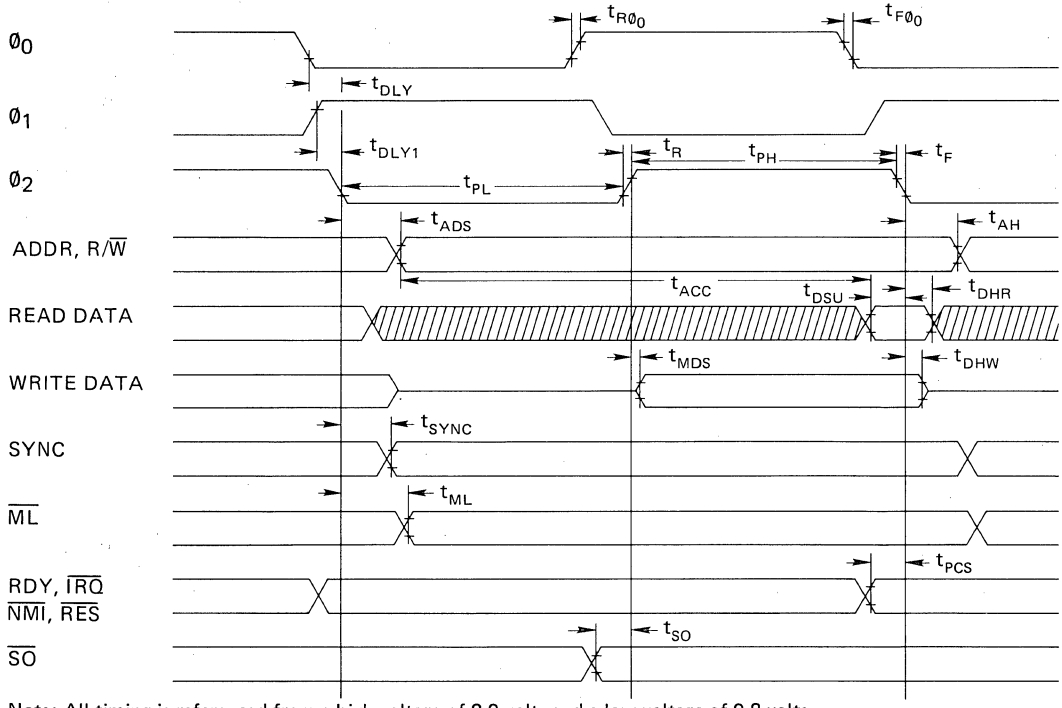
■ TIMING DIAGRAM



Note: All timing is referenced from a high voltage of 2.0 volts and a low voltage of 0.8 volts.

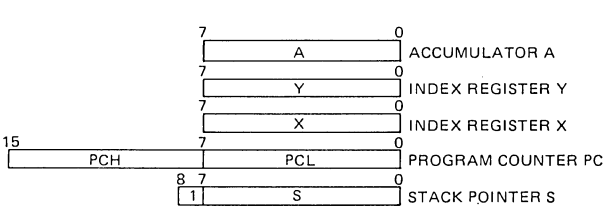
■ NEW INSTRUCTION MNEMONICS

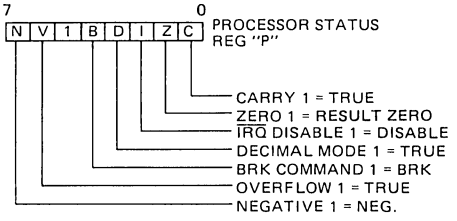
HEX	MNEMONIC	DESCRIPTION
80	BRA	Branch relative always [Relative]
3A	DEA	Decrement accumulator [Accum]
1A	INA	Increment accumulator [Accum]
DA	PHX	Push X on stack [Implied]
5A	PHY	Push Y on stack [Implied]
FA	PLX	Pull X from stack [Implied]
7A	PLY	Pull Y from stack [Implied]
9C	STZ	Store zero [Absolute]
9E	STZ	Store zero [ABS, X]
64	STZ	Store zero [Zero page]
74	STZ	Store zero [ZPG,X]
1C	TRB	Test and reset memory bits with accumulator [Absolute]
14	TRB	Test and reset memory bits with accumulator [Zero page]
0C	TSB	Test and set memory bits with accumulator [Absolute]
04	TSB	Test and set memory bits with accumulator [Zero page]

■ ADDITIONAL INSTRUCTION ADDRESSING MODES

HEX	MNEMONIC	DESCRIPTION
72	ADC	Add memory to accumulator with carry [(ZPG)]
32	AND	"AND" memory with accumulator [(ZPG)]
3C	BIT	Test memory bits with accumulator [ABS, X]
34	BIT	Test memory bits with accumulator [ZPG, X]
D2	CMP	Compare memory and accumulator [(ZPG)]
52	EOR	"Exclusive Or" memory with accumulator [(ZPG)]
7C	JMP	Jump (New addressing mode) [ABS(IND,X)]
B2	LDA	Load accumulator with memory [(ZPG)]
12	ORA	"OR" memory with accumulator [(ZPG)]
F2	SBC	Subtract memory from accumulator with borrow [(ZPG)]
92	STA	Store accumulator in memory [(ZPG)]

MICROPROCESSOR PROGRAMMING MODEL





FUNCTIONAL DESCRIPTION

Timing Control
The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase one clock pulse for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

Program Counter
The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

Instruction Register and Decode
Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register, then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

Arithmetic and Logic Unit (ALU)
All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

Accumulator
The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations, and in addition, the accumulator usually contains one of the two data words used in these operations.

Index Registers
There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address.

When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible (see addressing modes).

Stack Pointer
The stack pointer is an 8-bit register used to control the addressing of the variable-length stack on page one. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts ($\overline{NMI}$ and $\overline{IRQ}$). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer should be initialized before any interrupts or stack operations occur.

Processor Status Register
The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU. The 6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags (see microprocessor programming model).

■ ADDRESSING MODES

Fifteen addressing modes are available to the user of the NCR65C02 microprocessor. The addressing modes are described in the following paragraphs:

Implied Addressing [Implied]
In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

Accumulator Addressing [Accum]
This form of addressing is represented with a one byte instruction and implies an operation on the accumulator.

Immediate Addressing [Immediate]
With immediate addressing, the operand is contained in the second byte of the instruction; no further memory addressing is required.

Absolute Addressing [Absolute]
For absolute addressing, the second byte of the instruction specifies the eight low-order bits of the effective address, while the third byte specifies the eight high-order bits. Therefore, this addressing mode allows access to the total 64K bytes of addressable memory.

Zero Page Addressing [Zero Page]
Zero page addressing allows shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. The careful use of zero page addressing can result in significant increase in code efficiency.

Absolute Indexed Addressing [ABS, X or ABS, Y]
Absolute indexed addressing is used in conjunction with X or Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields, resulting in reduced coding and execution time.

Zero Page Indexed Addressing [ZPG, X or ZPG, Y]
Zero page absolute addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high-order eight bits of memory, and crossing of page boundaries does not occur.

Relative Addressing [Relative]
Relative addressing is used only with branch instructions; it establishes a destination for the conditional branch. The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the program counter when the counter is set at the next instruction. The range of the offset is −128 to +127 bytes from the next instruction.

Zero Page Indexed Indirect Addressing [(IND, X)]
With zero page indexed indirect addressing (usually referred to as indirect X) the second byte of the instruction is added to the contents of the X index register; the carry is discarded. The result of this addition points to a memory location on page zero whose contents is the low-order eight bits of the effective address. The next memory location in page zero contains the high-order eight bits of the effective address. Both memory locations specifying the high- and low-order bytes of the effective address must be in page zero.

***Absolute Indexed Indirect Addressing [ABS(IND, X)]**
(Jump Instruction Only)
With absolute indexed indirect addressing the contents of the second and third instruction bytes are added to the X register. The result of this addition, points to a memory location containing the lower-order eight bits of the effective address. The next memory location contains the higher-order eight bits of the effective address.

Indirect Indexed Addressing [(IND), Y]
This form of addressing is usually referred to as Indirect, Y. The second byte of the instruction points to a memory location in page zero. The contents of this memory location are added to the contents of the Y index register, the result being the low-order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high-order eight bits of the effective address.

***Zero Page Indirect Addressing [(ZPG)]**
In the zero page indirect addressing mode, the second byte of the instruction points to a memory location on page zero containing the low-order byte of the effective address. The next location on page zero contains the high-order byte of the effective address.

Absolute Indirect Addressing [(ABS)]
(Jump Instruction Only)
The second byte of the instruction contains the low-order eight bits of a memory location. The high-order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low-order byte of the effective address. The next memory location contains the high-order byte of the effective address which is loaded into the 16 bit program counter.

NOTE: * = New Address Modes

■ SIGNAL DESCRIPTION

Address Bus (A0-A15)
A0-A15 forms a 16-bit address bus for memory and I/O exchanges on the data bus. The output of each address line is TTL compatible, capable of driving one standard TTL load and 130pF.

Clocks ($\emptyset_0$, $\emptyset_1$, and $\emptyset_2$)
$\emptyset_0$ is a TTL level input that is used to generate the internal clocks in the 6502. Two full level output clocks are generated by the 6502. The $\emptyset_2$ clock output is in phase with $\emptyset_0$. The $\emptyset_1$ output pin is 180° out of phase with $\emptyset_0$. (See timing diagram.)

Data Bus (D0-D7)
The data lines (D0-D7) constitute an 8-bit bidirectional data bus used for data exchanges to and from the device and peripherals. The outputs are three-state buffers capable of driving one TTL load and 130 pF.

Interrupt Request ($\overline{IRQ}$)
This TTL compatible input requests that an interrupt sequence begin within the microprocessor. The $\overline{IRQ}$ is sampled during $\emptyset_2$ operation; if the interrupt flag in the processor status register is zero, the current instruction is completed and the interrupt sequence begins during $\emptyset_1$. The program counter and processor status register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further $\overline{IRQ}$s may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3K ohm external resistor should be used for proper wire OR operation.

Memory Lock ($\overline{ML}$)
In a multiprocessor system, the $\overline{ML}$ output indicates the need to defer the rearbitration of the next bus cycle to ensure the integrity of read-modify-write instructions. $\overline{ML}$ goes low during ASL, DEC, INC, LSR, ROL, ROR, TRB, TSB memory referencing instructions. This signal is low for the modify and write cycles.

Non-Maskable Interrupt ($\overline{NMI}$)
A negative-going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. The $\overline{NMI}$ is sampled during $\emptyset_2$; the current instruction is completed and the interrupt sequence begins during $\emptyset_1$. The program counter is loaded with the interrupt vector from locations FFFA (low byte) and FFFB (high byte), thereby transferring program control to the non-maskable interrupt routine.

Note: Since this interrupt is non-maskable, another $\overline{NMI}$ can occur before the first is finished. Care should be taken when using $\overline{NMI}$ to avoid this.

Ready (RDY)
This input allows the user to single-cycle the microprocessor on all cycles including write cycles. A negative transition to the low state, during or coincident with phase one ($\emptyset_1$), will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two ($\emptyset_2$) in which the ready signal is low. This feature allows microprocessor interfacing with low-speed memory as well as direct memory access (DMA).

Reset ($\overline{RES}$)
This input is used to reset the microprocessor. Reset must be held low for at least two clock cycles after V_{DD} reaches operating voltage from a power down. A positive transistion on this pin will then cause an initialization sequence to begin. Likewise, after the system has been operating, a low on this line of at least two cycles will cease microprocessing activity, followed by initialization after the positive edge on $\overline{RES}$.

When a positive edge is detected, there is an initialization sequence lasting six clock cycles. Then the interrupt mask flag is set, the decimal mode is cleared, and the program counter is loaded with the restart vector from locations FFFC (low byte) and FFFD (high byte). This is the start location for program control. This input should be high in normal operation.

Read/Write (R/$\overline{W}$)
This signal is normally in the high state indicating that the microprocessor is reading data from memory or I/O bus. In the low state the data bus has valid data from the microprocessor to be stored at the addressed memory location.

Set Overflow ($\overline{SO}$)
A negative transition on this line sets the overflow bit in the status code register. The signal is sampled on the trailing edge of $\emptyset_1$.

Synchronize (SYNC)
This output line is provided to identify those cycles during which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during $\emptyset_1$ of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the $\emptyset_1$ clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

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■ INSTRUCTION SET — ALPHABETICAL SEQUENCE

ADC Add Memory to Accumulator with Carry
AND "AND" Memory with Accumulator
ASL Shift One Bit Left
BCC Branch on Carry Clear
BCS Branch on Carry Set
BEQ Branch on Result Zero
BIT Test Memory Bits with Accumulator
BMI Branch on Result Minus
BNE Branch on Result not Zero
BPL Branch on Result Plus
*BRA Branch Always
BRK Force Break
BVC Branch on Overflow Clear
BVS Branch on Overflow Set
CLC Clear Carry Flag
CLD Clear Decimal Mode
CLI Clear Interrupt Disable Bit
CLV Clear Overflow Flag
CMP Compare Memory and Accumulator
CPX Compare Memory and Index X
CPY Compare Memory and Index Y
*DEA Decrement Accumulator
DEC Decrement by One
DEX Decrement Index X by One
DEY Decrement Index Y by One
EOR "Exclusive-or" Memory with Accumulator
*INA Increment Accumulator
INC Increment by One
INX Increment Index X by One
INY Increment Index Y by One
JMP Jump to New Location
JSR Jump to New Location Saving Return Address
LDA Load Accumulator with Memory
LDX Load Index X with Memory
LDY Load Index Y with Memory
LSR Shift One Bit Right
NOP No Operation
ORA "OR" Memory with Accumulator
PHA Push Accumulator on Stack
PHP Push Processor Status on Stack
*PHX Push Index X on Stack
*PHY Push Index Y on Stack
PLA Pull Accumulator from Stack
PLP Pull Processor Status from Stack
*PLX Pull Index X from Stack
*PLY Pull Index Y from Stack
ROL Rotate One Bit Left
ROR Rotate One Bit Right
RTI Return from Interrupt
RTS Return from Subroutine
SBC Subtract Memory from Accumulator with Borrow
SEC Set Carry Flag
SED Set Decimal Mode
SEI Set Interrupt Disable Bit
STA Store Accumulator in Memory
STX Store Index X in Memory
STY Store Index Y in Memory
*STZ Store Zero in Memory
TAX Transfer Accumulator to Index X
TAY Transfer Accumulator to Index Y
*TRB Test and Reset Memory Bits with Accumulator
*TSB Test and Set Memory Bits with Accumulator
TSX Transfer Stack Pointer to Index X
TXA Transfer Index X to Accumulator
TXS Transfer Index X to Stack Pointer
TYA Transfer Index Y to Accumulator

Note: * = New Instruction

■ MICROPROCESSOR OP CODE TABLE

S D	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	BRK	ORA ind, X			TSB* zpg	ORA zpg	ASL zpg		PHP	ORA imm	ASL A		TSB* abs	ORA abs	ASL abs		0
1	BPL rel	ORA ind, Y	ORA*† (zpg)		TRB* zpg	ORA zpg, X	ASL zpg, X		CLC	ORA abs, Y	INA* A		TRB* abs	ORA abs, X	ASL abs, X		1
2	JSR abs	AND ind, X			BIT zpg	AND zpg	ROL zpg		PLP	AND imm	ROL A		BIT abs	AND abs	ROL abs		2
3	BMI rel	AND ind, Y	AND*† (zpg)		BIT* zpg, X	AND zpg, X	ROL zpg, X		SEC	AND abs, Y	DEA* A		BIT*† abs, X	AND abs, X	ROL abs, X		3
4	RTI	EOR ind, X				EOR zpg	LSR zpg		PHA	EOR imm	LSR A		JMP abs	EOR abs	LSR abs		4
5	BVC rel	EOR ind, Y	EOR*† (zpg)			EOR zpg, X	LSR zpg, X		CLI	EOR abs, Y	PHY*			EOR abs, X	LSR abs, X		5
6	RTS	ADC ind, X			STZ* zpg	ADC zpg	ROR zpg		PLA	ADC imm	ROR A		JMP (abs)	ADC abs	ROR abs		6
7	BVS rel	ADC ind, Y	ADC*† (zpg)		STZ* zpg, X	ADC zpg, X	ROR zpg, X		SEI	ADC abs, Y	PLY*		JMP*† abs (ind,X)	ADC abs, X	ROR abs, X		7
8	BRA* rel	STA ind, X			STY zpg	STA zpg	STX zpg		DEY	BIT* imm	TXA		STY abs	STA abs	STX abs		8
9	BCC rel	STA ind, Y	STA*† (zpg)		STY zpg, X	STA zpg, X	STX zpg, Y		TYA	STA abs, Y	TXS		STZ* abs	STA abs, X	STZ* abs, X		9
A	LDY imm	LDA ind, X	LDX imm		LDY zpg	LDA zpg	LDX zpg		TAY	LDA imm	TAX		LDY abs	LDA abs	LDX abs		A
B	BCS rel	LDA ind, Y	LDA*† (zpg)		LDY zpg, X	LDA zpg, X	LDX zpg, Y		CLV	LDA abs, Y	TSX		LDY abs, X	LDA abs, X	LDX abs, Y		B
C	CPY imm	CMP ind, X			CPY zpg	CMP zpg	DEC zpg		INY	CMP imm	DEX		CPY abs	CMP abs	DEC abs		C
D	BNE rel	CMP ind, Y	CMP*† (zpg)			CMP zpg, X	DEC zpg, X		CLD	CMP abs, Y	PHX*			CMP abs, X	DEC abs, X		D
E	CPX imm	SBC ind, X			CPX zpg	SBC zpg	INC zpg		INX	SBC imm	NOP		CPX abs	SBC abs	INC abs		E
F	BEQ rel	SBC ind, Y	SBC*† (zpg)			SBC zpg, X	INC zpg, X		SED	SBC abs, Y	PLX*			SBC abs, X	INC abs, X		F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

Note: * = New OP Codes
Note: † = New Address Modes

■ OPERATIONAL CODES, EXECUTION TIME, AND MEMORY REQUIREMENTS

		IMME-DIATE			ABSO-LUTE			ZERO PAGE			ACCUM			IM-PLIED			(IND, X)			(IND), Y			ZPG, X			ZPG, Y			ABS, X			ABS, Y			RELA-TIVE			(ABS)			ABS (IND, X)			(ZPG)			PROCESSOR STATUS CODES	
MNE	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	7 6 5 4 3 2 1 0 N V . B D I Z C	MNE
ADC	A + M + C → A (1,3)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2				7D	4	3	79	4	3										72	5	2	N V . . . . Z C	ADC
AND	A ∧ M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2				3D	4	3	39	4	3										32	5	2	N . . . . . Z .	AND
ASL	C ← 7 … 0 ← 0 (1)				OE	6	3	06	5	2	0A	2	1										16	6	2				1E	6	3													N . . . . . Z C	ASL
BCC	Branch if C=0 (2)																																	90	2	2												BCC
BCS	Branch if C=1 (2)																																	B0	2	2												BCS
BEQ	Branch if Z=1 (2)																																	F0	2	2												BEQ
BIT	A ∧ M (4,5)	89	2	2	2C	4	3	24	3	2													34	4	2				3C	4	3													M7 M6 . . . Z .	BIT
BMI	Branch if N=1 (2)																																	30	2	2												BMI
BNE	Branch if Z=0 (2)																																	D0	2	2												BNE
BPL	Branch if N=0 (2)																																	10	2	2												BPL
BRA	Branch Always (2)																																	80	2	2												BRA
BRK	Break													00	7	1																																BRK
BVC	Branch if V=0 (2)																																	50	2	2												BVC
BVS	Branch if V=1 (2)																																	70	2	2												BVS
CLC	0 → C													18	2	1																																CLC
CLD	0 → D													D8	2	1																																CLD
CLI	0 → I													58	2	1																																CLI
CLV	0 → V													B8	2	1																																CLV
CMP	A - M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2				DD	4	3	D9	4	3										D2	5	2	N . . . . . Z C	CMP
CPX	X - M	E0	2	2	EC	4	3	E4	3	2																																					N . . . . . Z C	CPX
CPY	Y - M	C0	2	2	CC	4	3	C4	3	2																																					N . . . . . Z C	CPY
DEA	A - 1 → A										3A	2	1																																N . . . . . Z .	DEA
DEC	M - 1 → M (1)				CE	6	3	C6	5	2													D6	6	2				DE	6	3													N . . . . . Z .	DEC
DEX	X - 1 → X													CA	2	1																														N . . . . . Z .	DEX
DEY	Y - 1 → Y													88	2	1																														N . . . . . Z .	DEY
EOR	A ⊻ M → A	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2				5D	4	3	59	4	3										52	5	2	N . . . . . Z .	EOR
INA	A + 1 → A										1A	2	1																																N . . . . . Z .	INA
INC	M + 1 → M (1)				EE	6	3	E6	5	2													F6	6	2				FE	6	3													N . . . . . Z .	INC
INX	X + 1 → X													E8	2	1																														N . . . . . Z .	INX
INY	Y + 1 → Y													C8	2	1																														N . . . . . Z .	INY
JMP	Jump to new loc				4C	3	3																																6C	6	3	7C	6	3					JMP
JSR	Jump Subroutine				20	6	3																																										JSR
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2				BD	4	3	B9	4	3										B2	5	2	N . . . . . Z .	LDA
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																B6	4	2				BE	4	3												N . . . . . Z .	LDX
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2				BC	4	3													N . . . . . Z .	LDY
LSR	0 → 7 … 0 → C (1)				4E	6	3	46	5	2	4A	2	1										56	6	2				5E	6	3													0 . . . . . Z C	LSR
NOP	PC + 1 → PC													EA	2	1																																NOP
ORA	A V M → A (1)	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2				1D	4	3	19	4	3										12	5	2	N . . . . . Z .	ORA
PHA	A → Ms S - 1 → S													48	3	1																																PHA
PHP	P → Ms S - 1 → S													08	3	1																																PHP
PHX	X → Ms S - 1 → S													DA	3	1																																PHX
PHY	Y → Ms S - 1 → S													5A	3	1																																PHY
PLA	S + 1 → S Ms → A													68	4	1																														N . . . . . Z .	PLA
PLP	S + 1 → S Ms → P													28	4	1																														N V . 1 D I Z C	PLP
PLX	S + 1 → S Ms → X													FA	4	1																														N . . . . . Z .	PLX
PLY	S + 1 → S Ms → Y													7A	4	1																														N . . . . . Z .	PLY
ROL	7 … 0 ← C (1)				2E	6	3	26	5	2	2A	2	1										36	6	2				3E	6	3													N . . . . . Z C	ROL
ROR	C → 7 … 0 (1)				6E	6	3	66	5	2	6A	2	1										76	6	2				7E	6	3													N . . . . . Z C	ROR
RTI	Return from Inter.																																													N V . 1 D I Z C	RTI
RTS	Return from Subr.													40	6	1																																RTS
SBC	A - M - C̄ → A (1,3)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2				FD	4	3	F9	4	3										F2	5	2	N V . . . . Z C	SBC
SEC	1 → C													38	2	1																																SEC
SED	1 → D													F8	2	1																																SED
SEI	1 → I													78	2	1																																SEI
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2				9D	5	3	99	5	3										92	5	2		STA
STX	X → M				8E	4	3	86	3	2																96	4	2																			STX
STY	Y → M				8C	4	3	84	3	2																																							STY
STZ	00 → M				9C	4	3	64	3	2													94	4	2				9E	5	3																STZ
TAX	A → X													AA	2	1																														N . . . . . Z .	TAX
TAY	A → Y													A8	2	1																														N . . . . . Z .	TAY
TRB	Ā ∧ M → M (4)				1C	6	3	14	5	2																																					. . . . . Z .	TRB
TSB	A V M → M (4)				0C	6	3	04	5	2																																					. . . . . Z .	TSB
TSX	S → X													BA	2	1																														N . . . . . Z .	TSX
TXA	X → A													8A	2	1																														N . . . . . Z .	TXA
TXS	X → S													9A	2	1																																TXS
TYA	Y → A													98	2	1																														N . . . . . Z .	TYA

Notes:

1. Add 1 to "n" if page boundary is crossed.
2. Add 1 to "n" if branch occurs to same page.
   Add 2 to "n" if branch occurs to different page.
3. Add 1 to "n" if decimal mode.
4. V bit equals memory bit 6 prior to execution.
   N bit equals memory bit 7 prior to execution.

*5. The immediate addressing mode of the BIT instruction leaves bits 6 & 7 (V & N) in the Processor Status Code Register unchanged.

X Index X
Y Index Y
A Accumulator
M Memory per effective address
Ms Memory per stack pointer

\+ Add
− Subtract
∧ And
V Or
⊻ Exclusive or

n No. Cycles
No. Bytes
M6 Memory bit 6
M7 Memory bit 7

NCR

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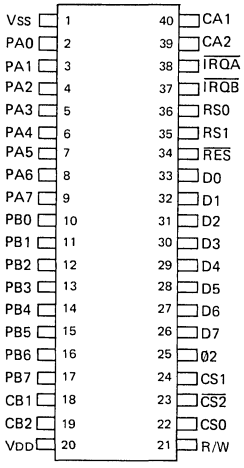
65C21
PERIPHERAL INTERFACE ADAPTER

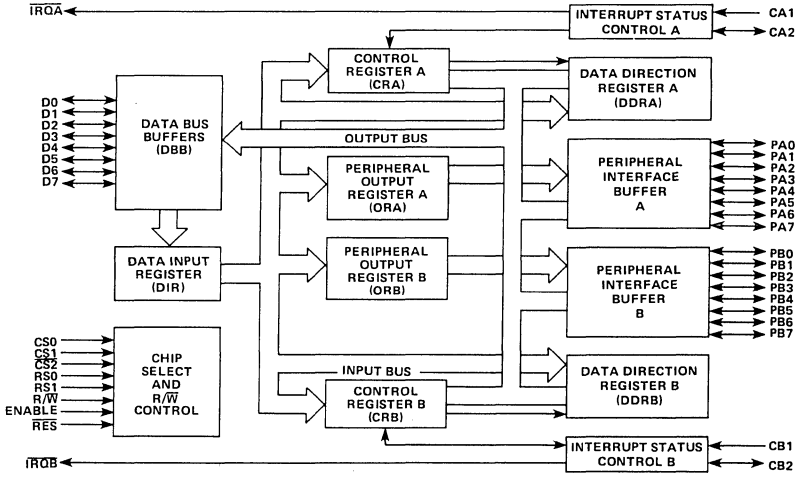
- CMOS process technology for low power consumption.
- Direct replacement for NMOS 6521 and 6821 devices manufactured by others.
- Low power consumption (2 mA at 1 MHz) allows battery operation.
- Two programmable 8-bit bidirectional I/O Ports for peripheral device interfacing.
- Individual Data Direction Registers for each I/O Port.
- Microprocessor/peripheral "handshake" interrupt feature for enhanced data transfer control.
- Programmable interrupt capability.
- Four operating frequencies – 1, 2, 3, and 4 MHz.
- Automatic power-up initialization.
- Single +5 volt power supply.
- Available in 40 pin dual-in-line package.

The NCR65C21 is a flexible Peripheral Interface Adapter for use with NCR and other 8-bit microprocessor families. The NCR65C21 provides programmed microprocessor control of up to two peripheral devices (Port A and Port B). Peripheral device control is accomplished through two 8-bit bidirectional I/O Ports, with individually assigned Data Direction Registers. The Data Direction Registers allow selection of data flow direction (input or output) at each respective I/O Port. Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port. The "handshake" interrupt control feature is provided by four peripheral control lines. This capability provides enhanced control over data transfer functions between the microprocessor and peripheral devices, as well as bidirectional data transfer between NCR65C21 Peripheral Interface Adapters in multiprocessor systems.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

PIN	DESCRIPTION
D0-D7	Data Bus
PA0-PA7	Peripheral I/O Port A
PB0-PB7	Peripheral I/O Port B
Ø2	Phase 2 Internal Clock
$\overline{RES}$	Reset
R/$\overline{W}$	Read/Write
$\overline{IRQA}$	Interrupt Request (Port A)

PIN	DESCRIPTION
$\overline{IRQB}$	Interrupt Request (Port B)
CS0, CS1, $\overline{CS2}$	Chip Select Inputs
RS0, RS1	Register Selects
CA1, CA2	Peripheral A Control Lines
CB1, CB2	Peripheral B Control Lines
V_{DD}	Positive Power Supply (+5V)
V_{SS}	Internal Logic Ground

Specifications are subject to change without notice.

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■ ABSOLUTE MAXIMUM RATINGS: (Note 1)

Rating	Symbol	Value
Supply Voltage	V_{DD}	–0.3V to +7.0V
Input Voltage	V_{IN}	–0.3V to +7.0V
Operating Temperature	T_A	0°C to +70°C
Storage Temperature	T_S	–55°C to +150°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Note:
1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

■ DC CHARACTERISTICS: V_{DD} = 5.0V ± 5%, V_{SS} = ØV, T_A = Ø°C to + 70°C

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	2.0	–	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	–0.3	–	0.8	V
Input Leakage Current, V_{IN} = 0 to 5V, Input Only Pins	I_{IN}	–	–	±2.5	μA
Three-State (Off State), Leakage Current, V_{IN} = 0.4 to 2.4V	I_{TSI}	–	–	±10.0	μA
Input High Current, V_{IH} = 2.4V, Peripheral Inputs with Pullups	I_{IH}	–200	–	–	μA
Input Low Current, V_{IL} = 0.4V, Peripheral Inputs with Pullups	I_{IL}	–	–	2.4	mA
Output Low Voltage, I_{OL} = 3.2 mA	V_{OL}	–	–	0.4	V
Output High Voltage, I_{OH} = -200μA	V_{OH}	2.4	–	–	V
Output Low Current (Sinking), V_{OL} = 0.4V	I_{OL}	3.2	–	–	mA
Output High Current (Sourcing),					
V_{OH_1} = 2.4V	I_{OH_1}	–0.2	–	–	mA
V_{OH_2} = 1.5V, Direct Transistor Drive	I_{OH_2}	–3.0	–	-10.0	mA
Supply Current f = 1 MHz	I_{DD}	–	–	2.0	mA
(No Load) f = 2 MHz	I_{DD}	–	–	4.0	mA
f = 3 MHz	I_{DD}	–	–	6.0	mA
f = 4 MHz	I_{DD}	–	–	8.0	mA
Power Dissipation, V_{DD} = 5.5V, f = 1 MHz	P_D	–	–	11.0	mW
Standby Power Dissipation	P_{SBY}	–	–	11.0	μW
Input Capacitance, f = 1 MHz	C_{IN}	–	–	10.0	pF
Output Capacitance, f = 1 MHz	C_{OUT}	–	–	5.0	pF

■ AC CHARACTERISTICS — PROCESSOR INTERFACE TIMING:

V_{DD} = 5.0V ± 5%, V_{SS} = ØV, T_A = Ø°C to + 70°C

		1MHz		2 MHz		3 MHz		4 MHz		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Cycle Time	t_{CYC}	1000	–	500	–	330	–	250	–	nS
Phase 2 Pulse Width High	t_{PWH}	470	–	240	–	160	–	120	–	nS
Phase 2 Pulse Width Low	t_{PWL}	470	–	240	–	160	–	120	–	nS
Phase 2 Transition	$t_{R,F}$	–	30	–	30	–	30	–	30	nS
Read Timing (Figure 1)										
Select, R/$\overline{W}$ Setup	t_{ACR}	160	–	90	–	65	–	45	–	nS
Select, R/$\overline{W}$ Hold	t_{CAR}	0	–	0	–	0	–	0	–	nS
Data Bus Delay	t_{CDR}	–	320	–	190	–	130	–	90	nS
Data Bus Hold	t_{HR}	10	–	10	–	10	–	10	–	nS
Peripheral Data Setup	t_{PCR}	300	–	150	–	110	–	75	–	nS

AC CHARACTERISTICS (Continued):

Parameter	Symbol	1 MHz Min	1 MHz Max	2 MHz Min	2 MHz Max	3 MHz Min	3 MHz Max	4 MHz Min	4 MHz Max	Unit
Write Timing (Figure 2)										
Select R/$\overline{W}$ Setup	t_{ACW}	160	–	90	–	65	–	45	–	nS
Select, R/$\overline{W}$ Hold	t_{CAW}	0	–	0	–	0	–	0	–	nS
Data Bus Setup	t_{DCW}	195	–	90	–	65	–	45	–	nS
Data Bus Hold	t_{HW}	10	–	10	–	10	–	10	–	nS
Peripheral Data Delay	t_{CPW}	–	1000	–	500	–	330	–	250	nS

Note: Measurement points 0.8V and 2.0V unless otherwise specified.

AC CHARACTERISTICS — PERIPHERAL INTERFACE TIMING:

V_{DD} = 5.0V ± 5%, 1TTL load, V_{SS} = ØV, T_A = 0°C to +70°C

Parameter	Symbol	1 MHz Min	1 MHz Max	2 MHz Min	2 MHz Max	3 MHz Min	3 MHz Max	4 MHz Min	4 MHz Max	Unit
CA2 Delay Time, High-to-Low	t_{CA2}	–	1.0	–	0.5	–	0.33	–	0.25	µS
CA2 Delay Time, Low-to-High	t_{RS1}	–	1.0	–	0.5	–	0.33	–	0.25	µS
CA2 Delay Time, Handshake Mode	t_{RS2}	–	2.0	–	1.0	–	0.67	–	0.50	µS
CB2 Delay Time, High-to-Low	t_{CB2}	–	1.0	–	0.5	–	0.33	–	0.25	µS
CB2 Delay Time, Low-to-High	t_{RS1}	–	1.0	–	0.5	–	0.33	–	0.25	µS
CB2 Delay Time, Handshake Mode	t_{RS2}	–	2.0	–	1.0	–	0.67	–	0.50	µS
CB2 Delay Time from Data Valid	t_{DC}	20	–	20	–	20	–	20	–	nS
Interrupt Input Pulse Width	P_{WI}	500	–	500	–	330	–	250	–	nS
Interrupt Response Time	t_{RS3}	–	1.0	–	1.0	–	0.67	–	0.33	µS
Interrupt Clear Delay	t_{IR}	–	1.6	–	0.85	–	0.67	–	0.33	µS
Rise and Fall Times— CA1, CA2, CB1, CB2	t_R, t_F	–	1.0	–	1.0	–	0.67	–	0.33	µS

TIMING DIAGRAMS

Measurement points of 0.8 V and 2.0 unless otherwise specified.

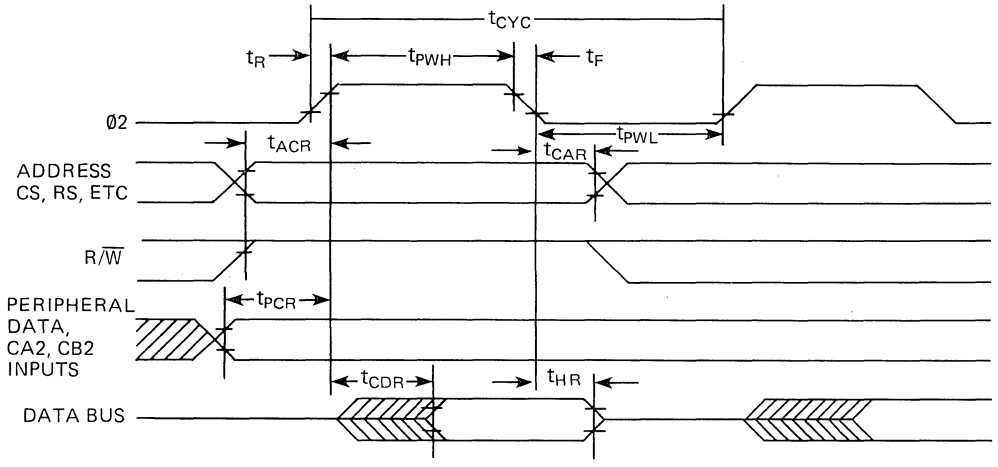


Figure 1. Read Timing

■ TIMING DIAGRAMS (Continued): Measurement points of 0.8V and 2.0V unless otherwise specified.

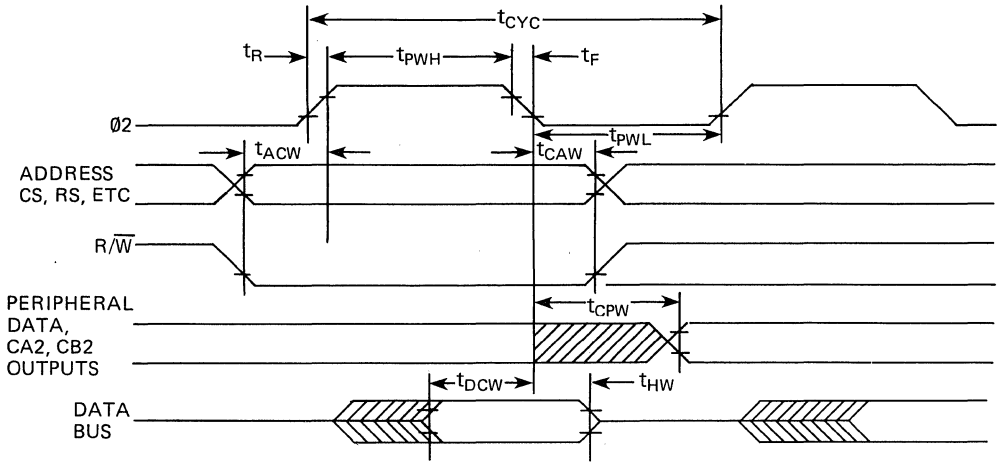


Figure 2. Write Timing

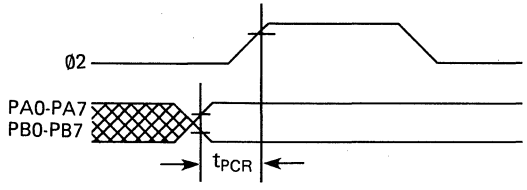


Figure 3. Peripheral Data Setup Time

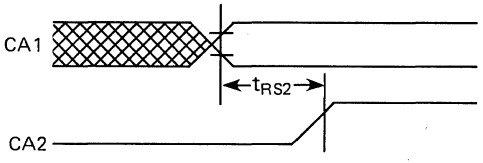


Figure 5. CA1/CA2 Timing

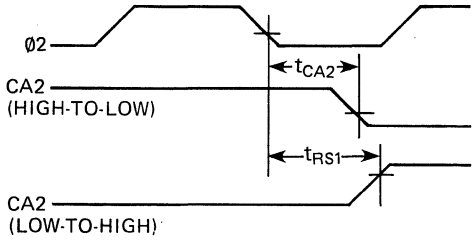


Figure 4. CA2 Timing

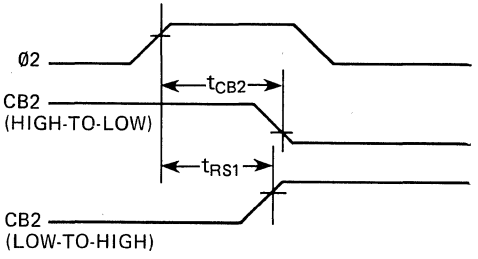


Figure 6. CB2 Timing

■ TIMING DIAGRAMS (Continued): Measurement points of 0.8V and 2.0V unless otherwise specified.

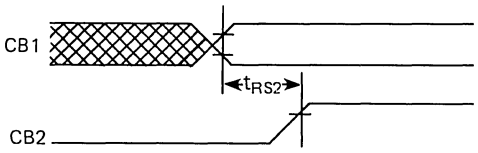


Figure 7. CB1/CB2 Handshake Timing

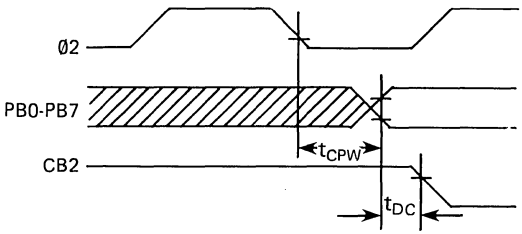


Figure 9. PB Port Delay Time

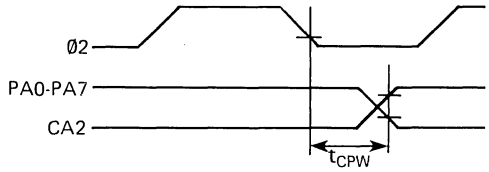


Figure 8. PA Port Delay Time

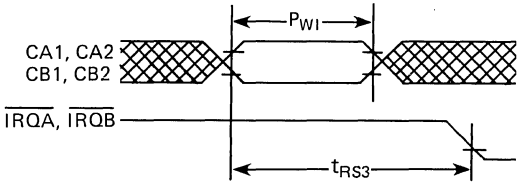


Figure 10. Interrupt Timing

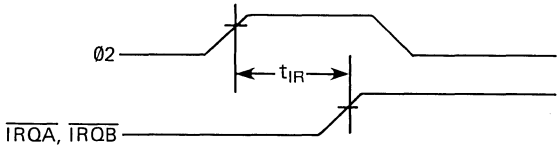


Figure 11. Interrupt Clear Timing

	7	6	5 4 3	2	1 0
CRA	$\overline{IRQA}$1	$\overline{IRQA}$2	CA2 Control	DDRA	CA1 Control
	7	**6**	**5 4 3**	**2**	**1 0**
CRB	$\overline{IRQB}$1	$\overline{IRQB}$2	CB2 Control	DDRB	CB1 Control

Figure 12. Control Registers

REGISTER SELECT PIN		DATA DIRECTION REGISTER ACCESS CONTROL BIT		
RS1	**RS0**	**CRA-2**	**CRB-2**	**REGISTER SELECTED**
0	0	1	–	Peripheral Interface A
0	0	0	–	Data Direction Register A
0	1	–	–	Control Register A
1	0	–	1	Peripheral Interface B
1	0	–	0	Data Direction Register B
1	1	–	–	Control Register B

Figure 13. Register Addressing

■ SIGNAL DESCRIPTION

Data Bus (D0-D7)
The eight bidirectional data bus lines are used to transfer data between the NCR65C21 and the microprocessor.

During a Read operation, the contents of the NCR65C21 internal Data Bus Buffer (DBB) are transferred to the microprocessor via the Data Bus lines. During a Write operation, the Data Bus lines represent high impedance inputs over which data is transferred from the microprocessor to the Data Input Register (DIR). The Data Bus lines are in the high impedance state when the NCR65C21 is unselected.

Chip Select (CS0, CS1, $\overline{CS2}$)
Normally, the three Chip Select lines are connected to the microprocessor address lines. This connection may be either direct or through an external decoder. To access the NCR65C21, CS0 and CS1 must be high (Logic 1) and CS2 must be low (Logic 0).

Register Select (RS0, RS1)
The Register Select inputs allow the microprocessor to select NCR65C21 internal registers as presented in Figure 13.

Read/Write (R/$\overline{W}$)
The Read/Write signal is generated by the microprocessor and is used to control the transfer of data between the NCR65C21 and the microprocessor. When R/$\overline{W}$ is in the high state (Logic1) and the chip is selected, data is transferred from the NCR65C21 to the microprocessor (Read operation). Conversely, when R/$\overline{W}$ is in the low state (Logic 0), data is transferred from the processor to the selected NCR65C21 internal register (Write operation). Read/Write must always be preceded by Chip Select (CS0, CS1 and $\overline{CS2}$).

Input Clock ($\emptyset_2$)
The system $\emptyset_2$ Input Clock synchronizes all data transfers between the NCR65C21 and the microprocessor.

Interrupt Request ($\overline{IRQA}$, $\overline{IRQB}$)
The Interrupt Request ($\overline{IRQA}$ for Port A, and $\overline{IRQB}$ for Port B) output signals become true (Logic 0) whenever an internal interrupt condition is determined by Interrupt Status Control Registers A and B. These two signals are active low and have open-drain outputs. The open-drain configuration allows the Interrupt Request signals to be wire-ORed to a common microprocessor $\overline{IRQ}$ input line.

Reset ($\overline{RES}$)
A low signal (Logic 0) on the Reset line serves to initialize the NCR65C21, clearing all internal registers and placing all peripheral interface lines (PA and PB) in the input state.

Peripheral Data Port A (PA0 - PA7)
Peripheral Data Port A is an 8-line, bidirectional bus used for the transfer of data, control and status information between the NCR65C21 and a peripheral device. Each data port bus line may be individually programmed as either an input or output under control of the Data Direction Register (DDRA). Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port.

Peripheral Data Port B (PB0 - PB7)
Peripheral Data Port B is an 8-line, bidirectional bus used for the transfer of data, control and status information between the NCR65C21 and a peripheral device. Functional operation is identical to Peripheral Data Port A, thus allowing the NCR65C21 to independently control two peripheral devices.

Interrupt Status Control
CA1, CA2 (Port A) and CB1, CB2 (Port B)
The two Interrupt Status Control lines for each Data Port are controlled by the Interrupt Status Control logic (A and B). This logic interprets the contents of the corresponding Control Register (CRA and CRB), allowing the Interrupt Status Control lines to perform various peripheral control functions.

Functional Description
Organization of the NCR65C21 consists of two independent control sections (A and B). Section A and Section B are identical – each consisting of a Control Register (CRA and CRB). Data Direction Register (DDRA and DDRB), Output Register (ORA and ORB), Interrupt Status Control (A and B) and Peripheral Interface Buffers (A and B). The Data Bus Buffers (DBB), Data Input Register (DIR) and the Chip Select and Read/Write control logic is common to both sections. Refer to the Block Diagram on Page 1.

Data Input Register (DIR)
During a Write data operation, the microprocessor writes data into the NCR65C21 by placing data on the Data Bus. This data is then latched into the Data Input Register by the Phase Two ($\emptyset_2$) clock. Once in the Data Input Register, this data byte is transferred into one of six internal registers. This data transfer occurs after the trailing edge of the $\emptyset_2$ clock pulse that latched the data byte into the Data Input Register. This timing delay guarantees that the data on the peripheral output lines (PA or PB) will make a smooth transition from low to high or high to low, and the output voltage will remain stable when there is to be no change in polarity.

Control Registers (CRA and CRB)
The individual Control Registers allow the microprocessor to program the operation of the Interrupt Control inputs (CA1, CA2, CB1, and CB2), and the Peripheral Control outputs (CA2 and CB2). Refer to Figure 4. Bit 2 in each Control Register controls the addressing of the Data Direction Registers (DDRA and DDRB) and also the Output Registers (ORA and ORB). Bits 6 and 7 are interrupt flag bits which indicate the status of the Interrupt Status Control input lines (CA1, CA2, CB1, and CB2). These two interrupt status flags are normally interrogated by the microprocessor during the interrupt service routing to determine the source of an active interrupt. These two interrupt lines drive the interrupt input ($\overline{IRQ}$ and $\overline{NMI}$) of the microprocessor.

Interrupt Status Control Logic (A and B)
The NCR65C21 contains four interrupt/peripheral control lines (CA1, CA2, CB1, and CB2). These lines are controlled by the Interrupt Status Control logic (A and B). The Interrupt Status Control logic serves to interpret the contents of the corresponding Control Register, thus allowing these lines to perform various control functions as described in Figure 16.

Data Direction Registers (DDRA and DDRB)
By use of the Data Direction Registers (DDR), the microprocessor can program each individual peripheral I/O

Port line as an input or output. Each bit within the register controls a corresponding line of the I/O Port, with DDRA controlling peripheral I/O Port A and DDRB controlling I/O Port B. A programmed "0" in any bit position of a DDR results in the corresponding I/O Port line being designated as an input. A "1" results in the line being an output.

Peripheral Output Registers (ORA and ORB)
All output data to a peripheral is stored in the corresponding Output Register (ORA or ORB). This data is then presented to the Peripheral Interface Buffer (A and B) and placed on the respective I/O Port lines. Writing a "0" into any bit position of ORA or ORB results in the corresponding peripheral I/O Port line going low ($<V_{OL}$), providing that particular line is programmed as an output. Writing a "1" into a bit position results in the corresponding output line going high.

Register Access and Selelction
Register Select lines RS0 and RS1 are used in combination with Chip Select to access the six function registers within the NCR65C21. These lines are normally connected to the microprocessor address output lines. As can be seen from Figure 13, the Register Select lines are used in combination with bit 2 of the Control Registers (CRA and CRB) to access the Data Direction Registers (DDRA and DDRB) and the peripheral Interface Output Registers (ORA and ORB). If bit 2 is a Logic 1, the Peripheral Output Register is selected, and if bit 2 is a Logic 0, the Data Direction Register is selected. Thus, with appropriate addressing the microprocessor can write directly into the Control Registers, the Data Direction Registers, and the peripheral interface Output Registers. Also, the microprocessor can read the contents of the Control Registers and the Data Direction Registers.

Data Access—Peripheral I/O Port A
Depending on the contents of Data Direction Register A, the eight lines of Peripheral I/O Port A may be programmed as either inputs or outputs. When a particular line(s) is programmed as an output, it will reflect the contents of the corresponding bit in peripheral Output Register A (ORA). When programmed as inputs, these lines will reflect the logic state of corresponding peripheral input data. Lines programmed as inputs are not affected by the peripheral Output Register (ORA). To perform a Read operation (RS1 = 0, RSO = 0, and Data Direction Register Access Control bit (CRA-2) = 1), data on peripheral I/O Port A lines is directly transferred to the microprocessor via the Data Bus. The transferred byte will contain both input and output data from all eight I/O Port A lines. It is the responsibility of the microprocessor to recognize and interpret only those bits which are important to a particular peripheral operation being performed. Note that the microprocessor always reads the I/O Port A "pins" and not the contents of the ORA. This being the case, the actual data read into the microprocessor may differ from the contents of the peripheral ORA, i.e., for a particular data "output" line. This condition occurs when the I/O pin is not allowed to reach a full V_{IH} for a Logic 1. When this occurs, the microprocessor will read a Logic 0, even though the corresponding bit in the peripheral ORA is a Logic 1.

Data Access—Peripheral I/O Port B
When reading peripheral I/O Port B, a combination of input and output data is read in a similar manner to peripheral I/O Port A above, The major difference is that for I/O Port B, data is read directly from peripheral Output Register B (ORB) for those lines programmed as outputs. This being the case, it is possible to load down I/O Port B lines without causing incorrect data to be transferred to the microprocessor during a Read operation.

Interrupt Request ($\overline{IRQA}$, $\overline{IRQB}$)
Both Interrupt Request ($\overline{IRQA}$, $\overline{IRQB}$) lines are active low, and serve to interrupt the microprocessor either directly or through external interrupt priority circuitry. Each line is "open drain" and is capable of sinking 1.6 milliamps from an external source, thus allowing all interrupts to be tied together in a wired-OR configuration. Each Interrupt Request line is assigned to a particular Peripheral Interface I/O Port ($\overline{IRQA}$ for Port A, and $\overline{IRQB}$ for Port B). Two interrupt flag bits are used with each Interrupt Request line. When true, these flag bits cause the Interrupt Request line to go low. The flag bits (bits 6 and 7 in each of the two Control Registers) act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the microprocessor to enable or disable the interrupts from each of the four interrupt inputs, i.e., CA1, CA2, CB1, and CB2. Each interrupt flag is set by an active transition on the interrupt input (CA1, CA2, CB1 and CB2).

Interrupt A Control ($\overline{IRQA}$)
Bit 7 of Control Register A is always set by a high to low transition of the CA1 interrupt control signal. This flag can be prevented from interrupting (disabled) by clearing bit 0 of Control Register A. Bit 6 of Control Register A is always set by an active transition of the CA2 interrupt control signal. This flag can be prevented from generating an interrupt by clearing bit 3 of Control Register A.

Both bit 6 and bit 7 in Control Register A are reset by reading the Peripheral Output Register A. To perform this Read operation, the proper Chip Select and appropriate Register Select signals must be present.

Interrupt B Control ($\overline{IRQB}$)
The control of Interrupt Request B ($\overline{IRQB}$) is performed in the same manner as that described above for $\overline{IRQA}$, except that for I/O Port B, Control Register bit 7 is set by a high to low transition on CB1 and interrupt enable/disable is controlled by Control Register bit 0. Control Register bit 6 is set by CB2 and its enable/disable is controlled by Control Register bit 3. Here again, both bit 6 and bit 7 in Control Register B are reset by reading the Peripheral Output Register B. Note that the interrupt disable bits (CRB bits 0 and 3) allow the microprocessor to control the interrupt function.

Interrupt Control Summary

$\overline{IRQA}$ goes low when CRA-7 = 1 and CRA-0 = 1 or when CRA-6 = 1 and CRA-3 = 1
$\overline{IRQB}$ goes low when CRB-7 = 1 and CRB-0 = 1 or when CRB-6 = 1 and CRB-3 = 1

Peripheral I/O Ports
The NCR65C21 provides two 8-bit bidirectional Data Ports (PA and PB) and four interrupt/control lines (CA1, CA2, CB1 and CB2) for interfacing to peripheral devices. Peripheral I/O Port A and I/O Port B allow the microprocessor to interface the peripheral device input lines by loading data into the corresponding Peripheral Output Register. The microprocessor interfaces the peri-

pheral device output lines by reading data on the I/O Port input lines directly onto the Data Bus and into the internal register of the microprocessor.

Peripheral I/O Port A (PA0 - PA7)
Each Peripheral I/O Port line can be programmed to act as an input or an output, as determined by the corresponding bits in the Data Direction Register. Within the Data Direction Register, a Logic 1 in a particular bit position represents an output line. Likewise, a Logic 0 in a particular bit position represents an input line. The Data Buffers which drive the I/O Port A lines contain "active" pull-up transistors as shown in Figure 14. Since these pull-ups are p-channel transistors they allow the output voltage to go to V_{DD} for a Logic 1. Also, since these switches can sink a full 1.6 milliamp, the buffers are capable of driving one standard TTL load. In the input mode, the pull-up devices shown in Figure 14 remain connected to the I/O pin and continue to supply current to the pin. For this reason, these lines represent one standard TTL load in the input mode.

Peripheral I/O Port B (PB0 - PB7)
The lines of Peripheral I/O Port B function in a similar manner to the discussion of I/O Port A above. Programmed selection for input/output function is identical. There are, however, several characteristics of the buffers driving these lines which effect their use in peripheral interfacing. Peripheral I/O Port B buffers are push-pull devices as shown in Figure 15.

This active pull-up devices can source up to 1 milliamp at 1.5 volts. This current drive capability is provided to allow direct connection to Darlington transistor switches. This allows convenient control of relays, lamps, etc. Because the I/O Port B outputs are designed to drive transistors directly, the output data is read directly from Peripheral Output Register B for those lines programmed as inputs. The I/O Port B push-pull buffers also provide a high impedance input state. When these lines are programmed as inputs, the output buffer enters the high impedance state.

Interrupt Input/Peripheral Control Lines (CA1, CA2, CB1 and CB2)
The NCR65C21 contains four interrupt input/peripheral control lines (CA1, CA2, CB1 and CB2) which offer a number of special peripheral control functions. These functions greatly enhance the performance of the two I/O Ports. Refer to Figure 16 for a summary of control line operation.

I/O Port A Interrupt Input/Peripheral Control Lines (CA1, CA2)
Line CA1 is an interrupt input only. An active transition on this line will set bit 7 in Control Register A to a Logic 1. This flag bit (bit 7) can be programmed to set on either a positive or negative CA1 transition. Bit 7 will be on a negative transition if bit 1 in the Control Register is cleared. Likewise, bit 7 can be set on a positive transition if bit 1 in the Control Register is set to a Logic 1.

It should be noted that a negative transition is defined as a transition from high to low, and a positive transition is a transition from low to high.

Setting the interrupt flag (bit 7 or the Control Register) will interrupt the microprocessor via $\overline{IRQA}$ if bit 0 in Control Register A is a Logic 1 as described in earlier paragraphs.

Line CA2 can act as a totally independent interrupt input or as a peripheral control output. CA2 acts as an interrupt input when Control Register A bit 5 is a Logic 0. In this case, CA2 will set the interrupt flag (bit 6 of Control Register A) to a Logic 1 on the active transition as selected by bit 4 of the Control Register. The Control Register bits and interrupt inputs serve the same basic function as that described above for CA1. The input transition sets the interrupt flag which serves as the link between the microprocessor interrupt configuration and the peripheral device. The interrupt disable bit allows the microprocessor to exercise control over the system interrupts.

CA2 serves in the output control mode when Control Register A bit 5 is a Logic 1. In this case, CA2 can operate independently to generate a sample pulse each time the microprocessor reads data on I/O Port A. This mode is selected by setting bit 4 of the Control Register to a Logic 0 and bit 3 to a Logic 1. This pulse output is normally used to control counters, shift registers, etc. which provide sequential data to the peripheral input lines.

A second output mode allows CA2 to be used in conjunction with CA1 to "handshake" between the peripheral device and the microprocessor. With respect to I/O Port A, this "handshake" allows positive control of data transfers from the peripheral device into the microprocessor. The "handshake" function operates as follows:

The CA1 input signals the microprocessor that data is available by interrupting the microprocessor. The microprocessor then reads the data and sets CA2 to a Logic 0. This signals the peripheral device that it can now place new data on the I/O Port line.

A third output mode can be selected by setting Control Register bit 4 to a Logic 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting or clearing bit 3 Control Register A.

I/O Port B Interrupt Input/Peripheral Control Lines (CB1, CB2)
The CB1 line operates as an interrupt input only in the same manner as CA1 above. In this case, bit 7 of Control Register B is set by the active transition on CB1 as selected by bit 0 of the Control Register. The CB2 input modes operate identical to the CA2 input modes. However, the CB2 output modes (Control Register B bit 5 set to Logic 1) differ somewhat from those of CA2. That is, the pulse output occurs when the microprocessor writes data into Output Register B. Also, the "handshaking" operates on data transfers from the microprocessor into the peripheral device.

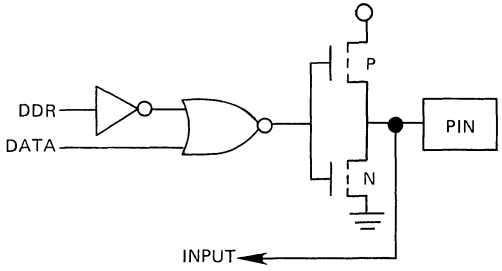


Figure 14. Port A Buffer Circuit (PA0-PA7)

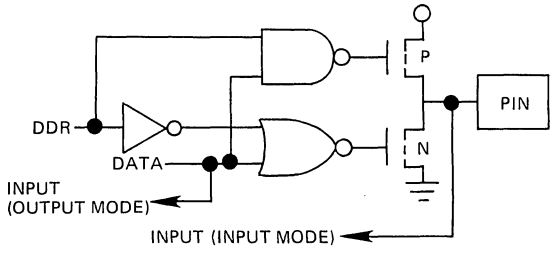


Figure 15. Port B Buffer Circuit (PB0-PB7)

CRA (CRB) BIT 1	CRA (CRB) BIT 0	CA1/CB1 CONTROL: ACTIVE TRANSITION OF INPUT SIGNAL*	CA1/CB1 CONTROL: $\overline{IRQA}$ ($\overline{IRQB}$) INTERRUPT OUTPUTS
0	0	Negative	Disable – remain high
0	1	Negative	Enable – goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1)
1	0	Positive	Disable – remain high
1	1	Positive	Enable – as explained above

*Note: Bit 7 of CRA (CRB) will be set to a Logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of bit 0 in CRA (CRB).

CRA (CRB) BIT 5	CRA (CRB) BIT 4	CRA (CRB) BIT 3	CA2/CB2 INPUT MODES: ACTIVE TRANSITION OF INPUT SIGNAL*	CA2/CB2 INPUT MODES: $\overline{IRQA}$ ($\overline{IRQB}$) INTERRUPT OUTPUTS
0	0	0	Negative	Disable – remain high
0	0	1	Negative	Enable – goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2)
0	1	0	Positive	Disable – remains high
0	1	1	Positive	Enable – as explained above

*Note: Bit 6 of CRA (CRB) will be set to a Logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of bit 0 in CRA (CRB).

CRA BIT 5	CRA BIT 4	CRA BIT 3	CA2 OUTPUT MODES: MODE	CA2 OUTPUT MODES: DESCRIPTION
1	0	0	"Handshake" on Read	CA2 is set high on an active transition of the CA 1 interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor.
1	0	1	Pulse Output	CA2 goes low for one cycle after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken.
1	1	0	Manual Output	CA2 set low
1	1	1	Manual Output	CA2 set high

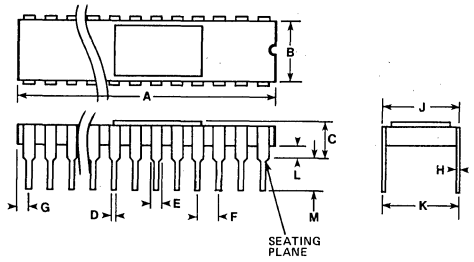
Figure 16. Interrupt Input/Peripheral Control Lines Operation

CB2 OUTPUT MODES				
CRB			MODE	DESCRIPTION
BIT 5	BIT 4	BIT 3		
1	0	0	"Handshake"	CB2 is set low on microprocessor "Write B Data" operation and is set high by an active transition of the CB 1 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device.
1	0	1	Pulse Output	CB2 goes low for one cycle after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available.
1	1	0	Manual Output	CB2 set low
1	1	1	Manual Output	CB2 set high

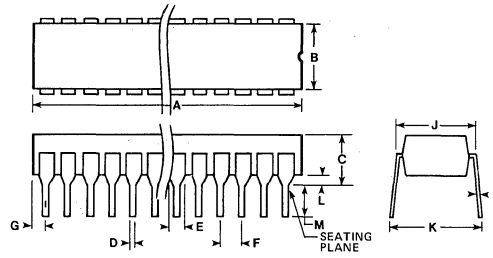
Figure 16. Interrupt Input/Peripheral Control Lines Operation (Continued)

■ PACKAGING INFORMATION

Typical Outline Drawing (Ceramic)



Typical Outline Drawing (Plastic & Cerdip)



40 PIN CERAMIC PACKAGE				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.419	51.181	1.985	2.015
B	14.605	15.367	0.575	0.605
C		3.810		0.150
D	0.381	0.533	0.015	0.021
E	0.889	1.524	0.035	0.060
F	2.286	2.794	0.090	0.110
G	1.016	1.524	0.040	0.060
H	0.203	0.305	0.008	0.012
J	15.113	15.875	0.590	0.620
K	15.24	REF	0.600	REF
L	0.889	1.651	0.035	0.065
M	2.540	3.556	0.100	0.140

40 PIN PLASTIC PACKAGE				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
E	1.02	1.52	0.040	0.060
F	2.54	TYP	0.100	TYP
G	1.65	2.16	0.065	0.085
H	0.20	0.38	0.008	0.015
J	15.24	TYP	0.600	TYP
K				
L	0.51	1.02	0.020	0.040
M	2.92	3.43	0.115	0.135

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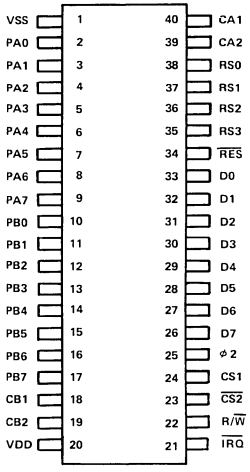
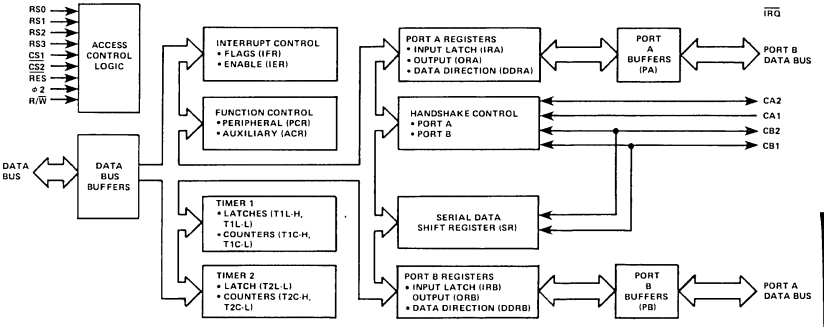
- Single +5 volts power supply.
- Available in 40-pin dual-in-line package.

The NCR65C22 Versatile Interface Adapter (VIA) is a flexible I/O device for use with the NCR65CXX series 8-bit microprocessor family. The NCR65C22 includes functions for programmed control of up to two peripheral devices (Ports A and B). Two program controlled 8-bit bidirectional peripheral I/O ports allow direct interfacing between the microprocessor and selected peripheral units. Each port has input data latching capability. Two programmable Data Direction Registers (A and B) allow selection of data direction (input or output) on an individual line basis. Also provided are two programmable 16-bit Interval Timer/Counters with latches. Timer 1 may be operated in a one-shot Interrupt Mode with interrupts on each count-to-zero, or in a free-run Mode with a continuous series of evenly spaced interrupts. Timer 2 functions as both an interval and pulse counter. Serial data transfers are provided by a serial-to-parallel/parallel-to-serial shift register. Application versatility is further increased by various control registers, including - an Interrupt Flag Register, an Interrupt Enable Register and two Function Control Registers.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

PIN	DESCRIPTION
D0-D7	Data Bus
PA0-PA7	Peripheral I/O Port A
PB0-PB7	Peripheral I/O Port B
Ø2	Phase 2 Internal Clock
$\overline{RES}$	Reset
R/$\overline{W}$	Read/Write
$\overline{IRQA}$	Interrupt Request

PIN	DESCRIPTION
CS1, $\overline{CS2}$	Chip Select Inputs
RS0, RS3	Register Selects
CA1, CA2	Peripheral A Control Lines
CB1, CB2	Peripheral B Control Lines
V_{DD}	Positive Power Supply (+5V)
V_{SS}	Internal Logic Ground

*Specifications are subject to change without notice.

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■ Absolute Maximum Ratings: (Note 1)

Rating	Symbol	Value
Supply Voltage	V_{DD}	−0.3V to +7.0V
Input Voltage	V_{IN}	−0.3V to +7.0V
Operating Temperature	T_A	0°C to +70°C
Storage Temperature	T_S	−55°C to +150°C

This device contains input protection against damage due to high static voltages or electric fields, however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not impled.

■ DC Characteristics: V_{DD} = 5.0V ± 5%, V_{SS} = 0V, T_A = 0°C to + 70°C

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	2.0	–	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	−0.3	–	0.8	V
Input Leakage Current, V_{IN} = 0 to 5V. Input Only Pins	I_{IN}	–	–	± 2.5	μA
Three-State (Off State), Leakage Current V_{IN} = 0.4 to 2.4V	I_{TSI}	–	–	± 10.0	μA
Input High Current, V_{IH} = 2.4V, Peripheral Inputs with Pullups	I_{IH}	−200	–	–	μA
Input Low Current, V_{IL} = 0.4V, Peripheral Inputs with Pullups	I_{IL}	–	–	2.4	mA
Output Low Voltage, I_{OL} - 3.2 mA	V_{OL}	–	–	0.4	V
Output High Voltage, I_{OH} = −200μA	V_{OH}	2.4	–	–	V
Output Low Current (Sinking), V_{OL} = 0.4V	I_{OL}	3.2	–	–	mA
Output High Current (Sourcing), V_{OH1} = 2.4 V	I_{OH1}	−0.2	–	–	mA
V_{OH2} = 1.5V, Direct Transistor Drive	I_{OH2}	−3.0	–	−10.0	mA
Supply Current f = 1 MHz (No Load)	I_{DD}	–	–	2.0	mA
f = 2 MHz	I_{DD}	–	–	4.0	mA
f = 3 MHz	I_{DD}	–	–	6.0	mA
f = 4 MHz	I_{DD}	–	–	8.0	mA
Power Dissipation, V_{DD} = 5.5V, f = 1 MHz	P_D	–	–	11.0	mW
Standby Power Dissipation	P_{SBY}	–	–	11.0	μW
Input Capacitance, f = 1 MHz	C_{IN}	–	–	10.0	pF
Output Capacitance, f = 1 MHz	C_{OUT}	–	–	5.0	pF

■ AC Characteristics — Processor Interface Timing: V_{DD} 5.0V ± 5%, V_{SS} = 0V,

T_A = −0°C to 70°C

		1 MHz		2 MHz		3 MHz		4 MHz		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Cycle Time	t_{CYC}	1000	–	500	–	330	–	250	–	nS
Phase 2 Pulse Width High	t_{PWH}	470	–	240	–	160	–	120	–	nS
Phase 2 Pulse Width Low	t_{PWL}	470	–	240	–	160	–	120	–	nS
Phase 2 Transition	$t_{R,F}$	–	30	–	30	–	30	–	30	nS
Read Timing (Figure 2)										
Select, R/$\overline{W}$ Setup	t_{ACR}	160	–	90	–	65	–	45	–	nS
Select, R/$\overline{W}$ Hold	t_{CAR}	0	–	0	–	0	–	0	–	nS
Data Bus Delay	t_{CDR}	–	320	–	190	–	130	–	90	nS
Data Bus Hold	t_{HR}	10	–	10	–	10	–	10	–	nS
Peripheral Data Setup	t_{PCR}	300	–	150	–	110	–	75	–	nS
Write Timing (Figure 3)										
Select R/$\overline{W}$ Setup	t_{ACW}	160	–	90	–	65	–	45	–	nS
Select R/$\overline{W}$ Hold	t_{ACW}	0	–	0	–	0	–	0	–	nS
Data Bus Setup	t_{DCW}	195	–	90	–	65	–	45	–	nS
Data Bus Hold	t_{HW}	10	–	10	–	10	–	10	–	nS
Peripheral Data Delay	t_{CPW}	–	1000	–	500	–	330	–	250	nS

■ AC Characteristics — Peripheral Interface Timing: V_{DD} = 5.0V ± 5%, V_{SS} = 0V,

T_A = 0°C to + 70°C (See Figures 4 through 12)

Parameter	Symbol	Min	Max	Unit	Figure
Rise and Fall Time for CA1, CB1, CA2 and CB2 Input Signals	t_R, t_F	–	1.0	μS	–
Delay Time, Clock Negative Transition to CA2 Negative Transition (Read Handshake or Pulse Mode)	t_{CA2}	–	1.0	μS	4.5
Delay Time, Clock Negative Transition to CA2 Positive Transition (Pulse Mode)	t_{RS1}	–	1.0	μS	4
Delay Time, CA1 Active Transition to CA2 Positive Transition (Handshake Mode)	t_{RS2}	–	2.0	μS	5
Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (Write Handshake)	t_{WHS}	0.05	1.0	μS	6.7
Delay Time, Peripheral Data Valid to CB2 Negative Transition	t_{DS}	0.20	1.5	μS	6.7
Delay Time, Clock Positive Transition to CA2 or CB2 Positive Transition (Pulse Mode)	t_{RS3}	–	1.0	μS	6
Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (Handshake Mode)	t_{RS4}	–	2.0	μS	7
Delay Time Required from CA2 Output to CA1 Active Transition (Handshake Mode)	t_{21}	400	–	nS	7
Set-up Time, Peripheral Data Valid to CA1 or CB1 Active Transition (Input Latching)	t_{IL}	300	–	nS	8
Shift-Out Delay Time – Time from Ø2 Falling Edge to CB2 Data Out	t_{SR1}	–	300	nS	9
Shift-In Set-up Time – Time from CB2 Data in to Ø2 Rising Edge	t_{SR2}	300	–	nS	10
External Shift Clock (CB1) Set-up Time Relative to Ø2 Trailing Edge	t_{SR3}	100	t_{CYC}	nS	10
Pulse Width – PB6 Input Pulse	t_{IPW}	$2xt_{CYC}$	–		12
Pulse Width – CB1 Input Clock	t_{ICW}	$2xt_{CYC}$	–		11
Pulse Spacing – PB6 Input Pulse	t_{IPS}	$2xt_{CYC}$	–		12
Pulse Spacing – CB1 Input Pulse	t_{ICS}	$2xt_{CYC}$	–		11
CA1, CB1 Set Up Prior to Transition to Arm Latch	t_{AL}	300	–	nS	8
Peripheral Data Hold After CA1, CB1 Transition	t_{PDH}	150	–	nS	8

■ TIMING DIAGRAMS

Measurement points of 0.8 V and 2.0 unless otherwise specified.

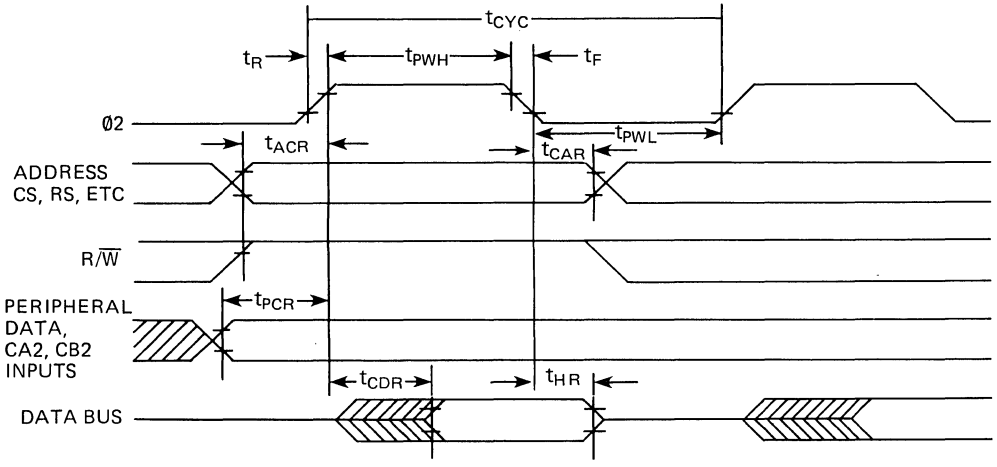


Figure 1. Read Timing

■ TIMING DIAGRAMS (Continued): Measurement points of 0.8V and 2.0V unless otherwise specified.

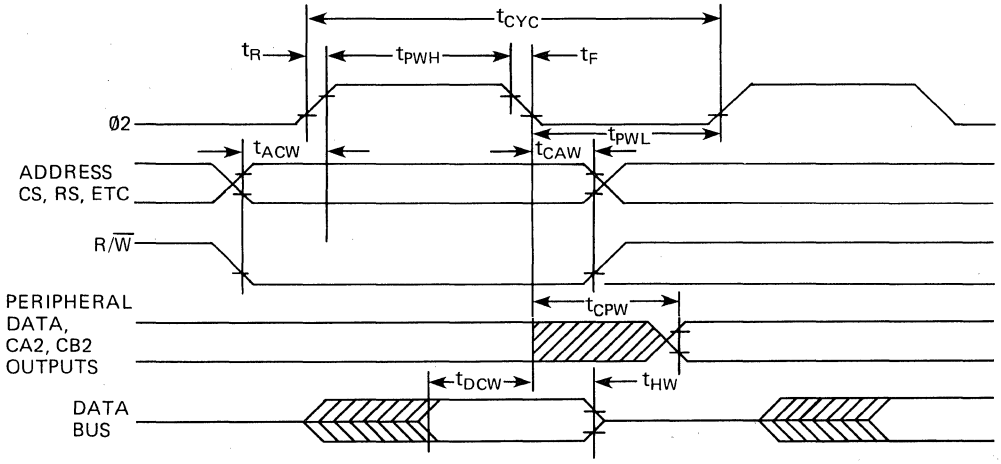


Figure 2. Write Timing

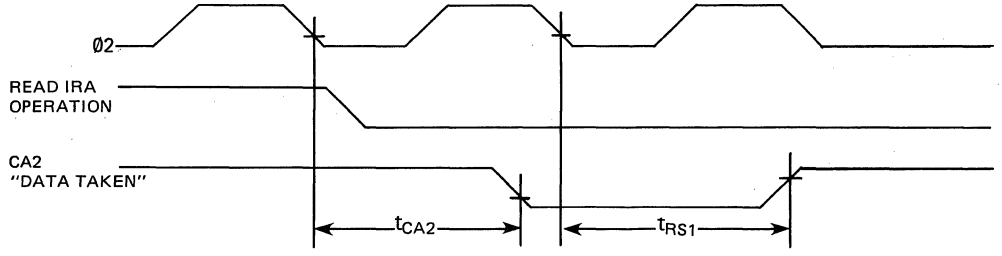


Figure 3. Read Handshake, Pulse Mode Timing (CA2)

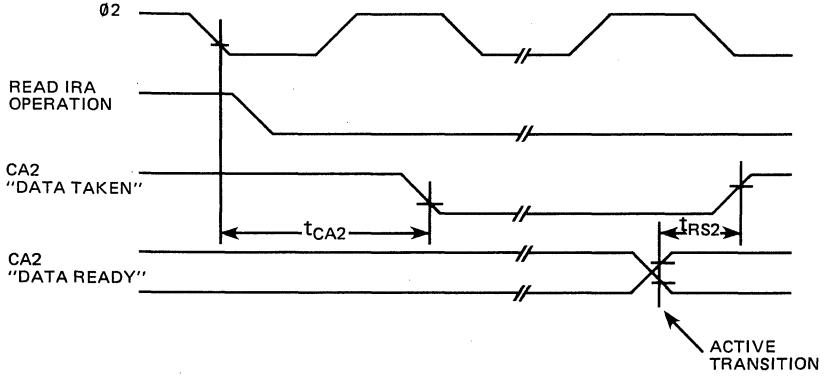


Figure 4. Read Handshake, Handshake Mode Timing (CA2)

■ Timing Diagrams (Continued): Measurement points 0.8V and 2.0V unless otherwise specified.

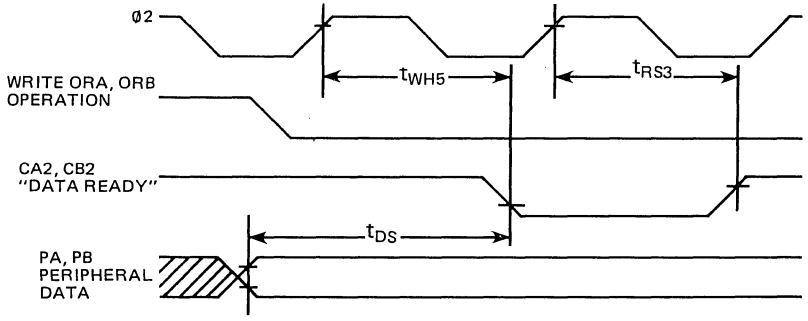


Figure 5. Write Handshake, Pulse Mode Timing (CA2, CB2)

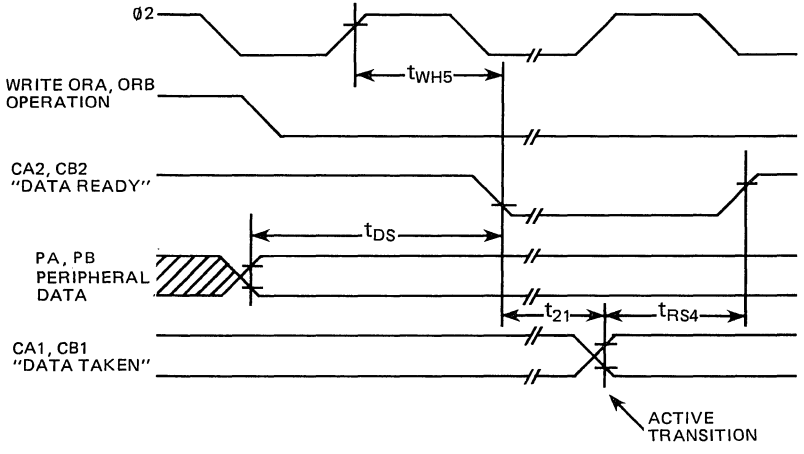


Figure 6. Write Handshake, Handshake Mode Timing (CA2, CB2)

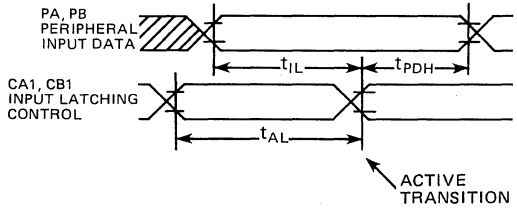


Figure 7. Peripheral Data, Input Latching Timing

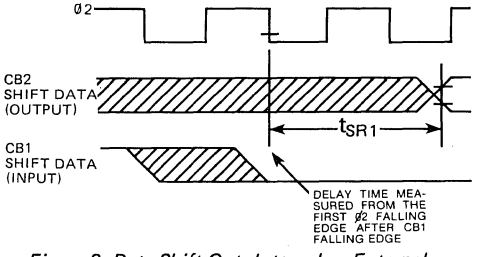


Figure 8. Data Shift Out, Internal or External Shift Clock Timing

■ Timing Diagrams (Continued):

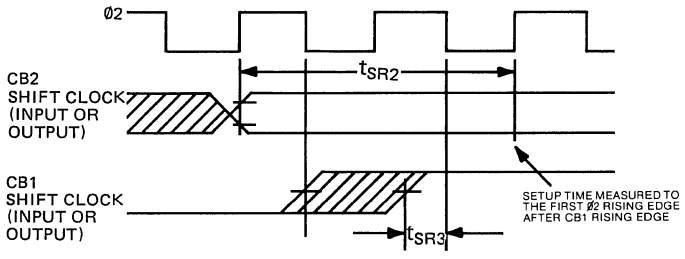


Figure 9. Data Shift In, Internal or External Shift Clock Timing

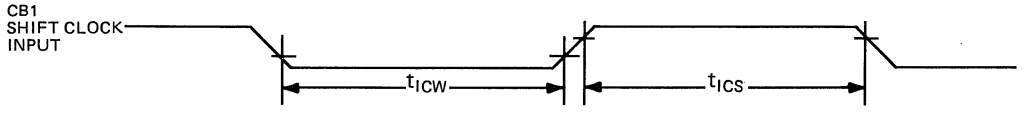


Figure 10. External Shift Clock Timing

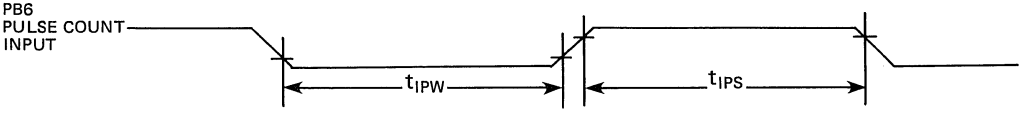


Figure 11. Pulse Count Input Timing

■ Signal Description

Reset ($\overline{RES}$)
Reset ($\overline{RES}$) clears all internal registers except T1 and T2 counters and latches, and the Shift Register (SR). In the $\overline{RES}$ condition, all peripheral interface lines (PA and PB) are placed in the input state. Also, the Timers (T1 and T2), SR and interrupt logic are disabled from operation.

Input Clock ($Ø_2$)
The system $Ø_2$ Input Clock synchronizes all data transfers between the NCR65C22 and the microprocessor.

Read/Write (R/$\overline{W}$)
The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the transfer of data between the NCR 65C22 and the microprocessor. When R/$\overline{W}$ is in the high state (Logic 1) and the chip is selected, data is transferred from the NCR65C22 to the microprocessor (Read operation). Conversely, when R/$\overline{W}$ is in the low state (Logic 0), data is transferred from the processor to the selected NCR65C22 register (Write operation). Read/Write must always be accompanied by a proper Chip Select (CS1, $\overline{CS2}$).

Data Bus (D0 - D7)
The eight bidirectional Data Bus lines are used to transfer data between the NCR65C22 and the microprocessor. During a Read operation, the contents of the selected NCR65C22 internal register are transferred to the microprocessor via the Data Bus lines. During a Write operation, the Data Bus lines serve as high impedance inputs over which data is transferred from the microprocessor to a selected NCR65C22 register. The Data Bus lines are in the high impedance state when the NCR65C22 is unselected.

Chip Select (CS1, $\overline{CS2}$)
Normally, the two Chip Select lines are connected to the microprocessor address lines. This connection may be direct or through decoding. To access a selected NCR-65C22 register, CS1 must be high (Logic 1) and $\overline{CS2}$ must be low (Logic 0). (Refer to figures 1 and 2).

Register Select (RS0 - RS3)
The Register Select inputs allow the microprocessor to select one of 16 internal registers within the NCR65C22. Refer to Table 1 for Register Select coding and a functional description.

Interrupt Request ($\overline{IRQ}$)
The Interrupt Request ($\overline{IRQ}$) output signal is generated (Logic 0) whenever an internal Interrupt Flag bit is set (Logic 1) and the corresponding Interrupt Enable bit is a Logic 1. The Interrupt Request output is an open-drain configuration, thus allowing the $\overline{IRQ}$ signal to be wire-ORed to a common microprocessor $\overline{IRQ}$ input line.

Peripheral Data Port A (PA0 - PA7)
Peripheral Data Port A is an 8-line, bidirectional bus used for the transfer of data, control and status information between the NCR65C22 and a peripheral device. Each Peripheral Data Port bus line may be individually programmed as either an input or output under control of a Data Direction Register. Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port. When a "0" is

Table 1. Internal Registers

Register Number	RS Coding				Register Designation	Description	
	RS3	RS2	RS1	RS0		Write	Read
0	0	0	0	0	ORB/IRB	Output Register "B"	Input Register "B"
1	0	0	0	1	ORA/IRA	Output Register "A"	Input Register "A"
2	0	0	1	0	DDRB	Data Direction Register "B"	
3	0	0	1	1	DDRA	Data Direction Register "A"	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Same As Reg 1 Except No "Handshake"	

written to any bit position of the Data Direction Register, the corresponding line will be programmed as an input. Likewise, when a "1" is written into any bit position of the register, the corresponding data line will serve as an output. Polarity of the data output is determined by the Output Register, while input data may be latched into the Input Register under control of the CA1 line. All modes are program controlled by the microprocessor by way of the NCR65C22's internal control registers. Each Peripheral Data Port line represents one TTL load in the input mode and will drive one standard TTL load in the output mode. A typical output circuit for Peripheral Data Port A is shown in Figure 12.

Peripheral Data Port B (PB0 - PB7)
Peripheral Data Port B is an 8-line, bidirectional bus which is controlled by an Output Register, Input Register and Data Direction Register in a manner much the same as Data Port A. With respect to Port B, the output signal on line PB7 may be controlled by Timer 1 while Timer 2 may be programmed to count pulses on the PB6 line. Port B lines represent one standard TTL load in the input mode and will drive one TTL load in the output mode. Port B lines are also capable of sourcing I_{OH2} mA at V_{OH2} Vdc in the output mode. (See DC characteristics). This allows the outputs to directly drive Darlington transistor circuits. A typical output circuit for Port B is shown in Figure 13.

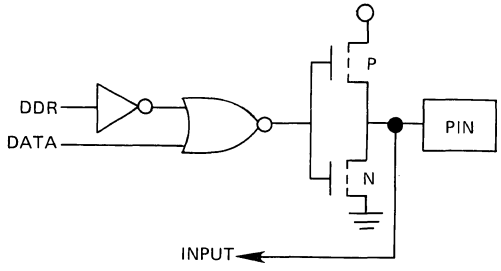


Figure 12. Port A Buffer Circuit (PA0-PA7, CA2)

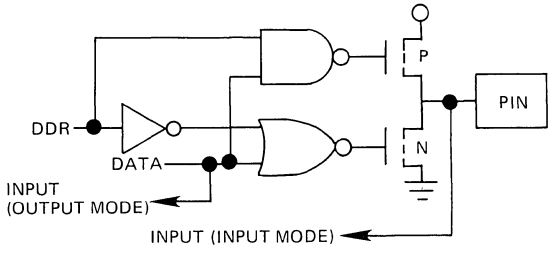


Figure 13. Port B Buffer Circuit (PB0-PB7, CB1, CB2)

Peripheral Data Port A Control Lines (CA1, CA2)
Control lines CA1 and CA2 serve as interrupt inputs or handshake outputs for Peripheral Data Port A. Each line controls an internal Interrupt Flag with a corresponding Interrupt Enable bit. CA1 also controls the latching of Input Data on Port A. CA1 is a high impedance input, while CA2 represents one standard TTL load in the input mode. In the output mode, CA2 will drive one standard TTL load.

Peripheral Data Port B Control Lines (CB1, CB2)
Control lines CB1 and CB2 serve as interrupt inputs or handshake outputs for Peripheral Data Port B. Like Port A, these two control lines control an internal Interrupt Flag with a corresponding Interrupt Enable bit. These lines also serve as a serial data port under control of the Shift Register (SR). Each control line represents one standard TTL load in the input mode and can drive one TTL load in the output mode. Note that CB1 and CB2 cannot drive Darlington transistor circuits.

Peripheral Data Ports (Port A, Port B)
Each Peripheral Data Port operates in conjunction with a Data Direction Register (DDRA or DDRB). Under program control, the Data Direction Registers specify which lines within the port bus are to be designated as inputs or outputs. A Logic 0 in any bit position of the register will cause the corresponding line to serve as an input, while a Logic 1 will cause the line to serve as an output.

When a line is programmed as an output, it is controlled by a corresponding bit in the Output Register (ORA & ORB). A Logic 1 in the Output Register will cause the corresponding output line to go high, while a Logic 0 will cause the line to go low. Under program control, data is written into the Output Register bit positions corresponding to the output lines which have been programmed as outputs. Should data be written into bit positions corresponding to lines which have been programmed as inputs, the lines will be unaffected.

When reading a Peripheral Data Port, the contents of the corresponding Input Register (IRA or IRB) is transferred onto the Data Bus. When the input latching feature is disabled, Input Register A (IRA) will reflect the logic levels present on the Port A bus lines. However, with input latching enabled and the selected active transition on CA1 having occurred, Input Register A will contain the data present on the Port A bus lines at the time of the transition. In this case, once Input Register A has been read, it will appear transparent, reflecting the current state of the Port A bus lines until the next CA1 latching transition.

With respect to Input Register B, it operates in a similar way to Input Register A, except that for those Port B bus lines which have been programmed as outputs, there is a difference. When reading Input Register A, the logic level on the bus line determines whether a Logic 1 or 0 is sensed. However, when reading Input Register B, the logic level stored in Output Register B (ORB) is the logic level sensed. For this reason, those outputs which have large loading effects may cause the reading of Input Register A to result in the reading of a Logic 0 when a 1 was actually programmed, and reading a Logic 1 when a 0 was programmed. However, when reading Input Register B, the logic level read will be correct, regardless of loading on the particular bus line.

For information on formats and operation of the Peripheral Data Port registers, refer to Figures 14, 15 and 16. It should be noted that the input latching modes are controlled by the Auxiliary Control Register (See Figure 22).

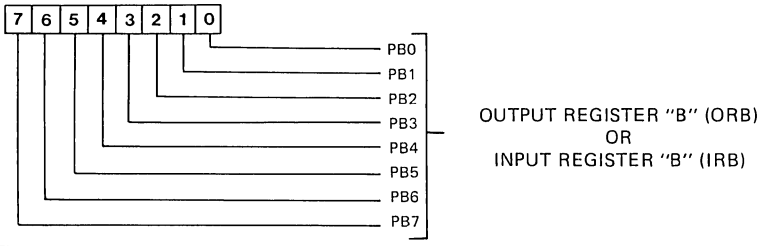
Data Transfer–Handshake Control
A powerful feature of the NCR65C22 is its ability to provide absolute control over data transfers between the microprocessor and peripheral devices. This control is accomplished by way of "handshake" lines. Port A lines (CA1, CA2) handshake data transfers on both Read and Write operations, while Port B lines (CB1, CB2) handshake data on Write operations only.

Read Handshake Control
Read Handshaking provides effective control of data transfers from a peripheral device to the microprocessor. To accomplish the Read Handshake, the peripheral device generates a Data Ready signal to the NCR65C22 which indicates valid data is present on the Peripheral Data Port bus. In most cases, this Data Ready signal will interrupt the microprocessor, which will then read the data and generate a Data Taken signal. Once the peripheral senses the Data Taken signal, new data will be placed on the bus. This process continues until the data transfer is complete.

Automatic Read Handshaking applies to Peripheral Data Port A only. The Data Ready signal is transmitted by the peripheral device over the CA1 interrupt line, while the Data Taken signal is generated and transmitted to the peripheral device over the CA2 line. When the Data Ready signal is received, it sets an internal flag in the Interrupt Flag Register (IFR). This flag may interrupt the microprocessor or it may be polled under program control. As an option, the Data Taken signal may be either a pulse or a level. In either case, it is set low (Logic 0) by the microprocessor and is cleared by the next Data Ready signal. Refer to Figure 17 for Read Handshake timing and operating sequence.

Write Handshake Control
The Write Handshake operation is similar to Read Handshaking. For Write Handshaking, however, the NCR-65C22 generates the Data Ready signal and the peripheral device must generate the Data Taken return signal. Note that Write Handshaking may occur on both Data Ports (A and B). For a Write Handshake, CA2 or CB2 serve as the Data Ready output and can operate in either the Handshake Mode or the Pulse Mode. The Data Taken signal is received by CA1 or CB1. The Data Taken signal sets a flag in the Interrupt Flag Register and clears the Data Ready output signal. Refer to Figure 18 for Write Handshake timing and operating sequence. Note that the selection of Read or Write Handshake operating modes (CA1, CA2, CB1, and CB2) is accomplished by the Peripheral Control Register (PCR). See Figure 19.

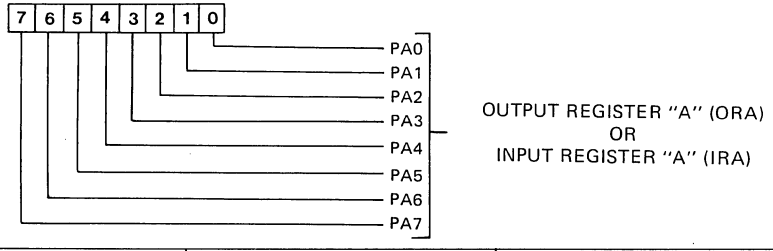
REG 0 – ORB/IRB



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRB = "1" (OUTPUT)	MPU writes Output Level (ORB)	MPU reads output register bit in ORB. Pin level has no effect
DDRB = "0" (INPUT) (Input latching disabled)	MPU writes into ORB, but no effect on pin level, until DDRB changed.	MPU reads input level on PB pin.
DDRB = "0" (INPUT) (Input latching enabled)		MPU reads IRB bit, which is the level of the PB pin at the time of the last CB1 active transition.

Figure 14. Output Register B (ORB), Input Register B (IRB)

REG 1 – ORA/IRA



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRA = "1" (OUTPUT) (Input latching disabled)	MPU writes Output Level (ORA)	MPU reads level on PA pin.
DDRA = "1" (OUTPUT (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA 1 active transition.
DDRA = "0" (INPUT) (Input latching disabled)	MPU writes into ORA, but no effect on pin level, until DDRA changed.	MPU reads level on PA pin.
DDRA = "0" (INPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.

Figure 15. Output Register A (ORA), Input Register A (IRA)

REG – DDRB AND REG 3 – DDRA

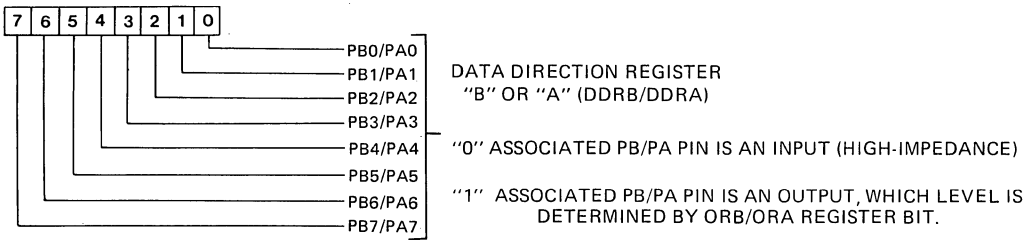


Figure 16. Data Direction Registers (DDRB, DDRA)

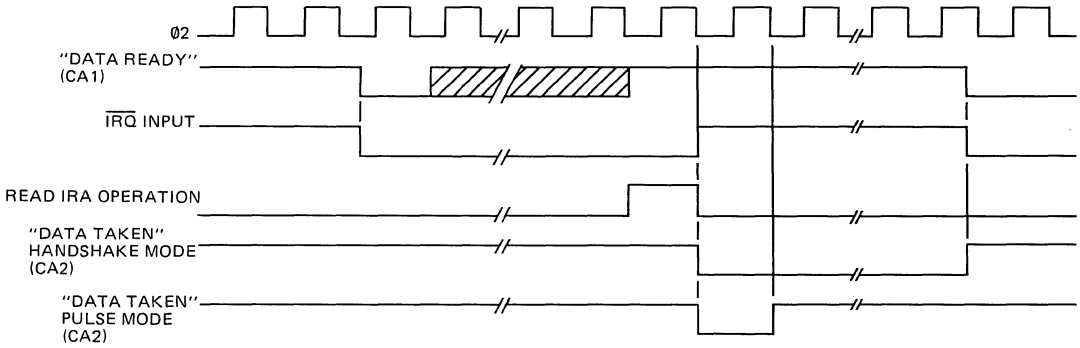


Figure 17. Read Handshake Timing (Port A Only)

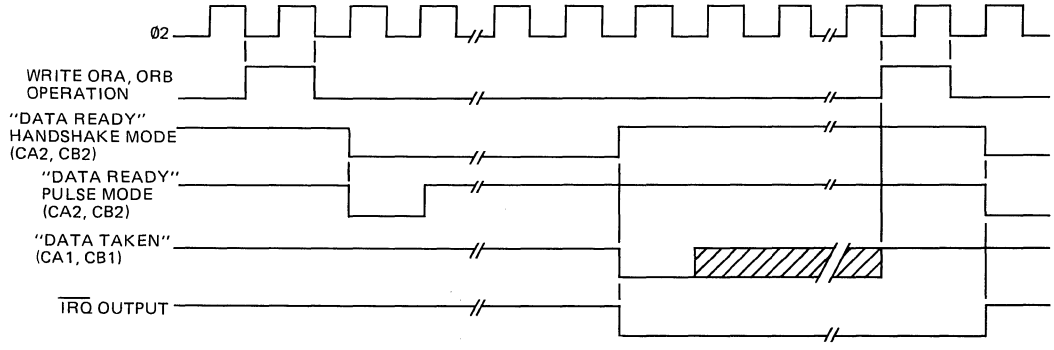
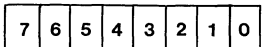


Figure 18. Write Handshake Timing (Ports A and B)

REG 12 — PERIPHERAL CONTROL REGISTER



CB2 CONTROL

7	6	5	Operation
0	0	0	Input-negative action edge
0	0	1	Independent interrupt input-negative edge*
0	1	0	Input-positive active edge
0	1	1	Independent interrupt input-positive edge*
1	0	0	Handshake output
1	0	1	Pulse output
1	1	0	Low output
1	1	1	High output

CB1 INTERRUPT CONTROL

0 = Negative Active Edge
1 = Positive Active Edge

CA1 INTERRUPT CONTROL

0 = Negative Active Edge
1 = Positive Active Edge

CA2 CONTROL

3	2	1	Operation
0	0	0	Input-negative action edge
0	0	1	Independent interrupt input-negative edge*
0	1	0	Input-positive active edge
0	1	1	Independent interrupt input-positive edge*
1	0	0	Handshake output
1	0	1	Pulse output
1	1	0	Low output
1	1	1	High output

*If the CA2/CB2 control in the PCR is selected as "independent" interrupt input, then reading or writing the output register ORA/ORB will not clear the flag bit. Instead, the bit must be cleared by writing into the IFR, as described previously.

Figure 19. CA1, CA2, CB1, CB2 Control

Timer 1: Operation

Interval Timer T1 consists of two 8-bit latches and a 16-bit counter. The latches serve to store data which is to be loaded into the counter. Once the counter is loaded under program control, it decrements at a Phase 2 ($\emptyset_2$) clock rate. Upon reaching zero, an Interrupt Flag is set, causing Interrupt Request ($\overline{IRQ}$) to go low (Logic 0) if the corresponding Interrupt Enable bit is set. Once the Timer reaches a count of zero, it will either disable any further interrupts (provided it has been programmed to do so), or it will automatically transfer the contents of the latches into the counter and proceed to decrement again. The counter may also be programmed to invert the output signal on PB7 each time it reaches a count of zero. Each of these counter modes is presented below. The T1 counter format and operation is shown in Figure 20 with corresponding latch format and operation in Figure 21. Additional control bits are provided in the Auxiliary Control Register (bits 6 and 7) to allow selection of Timer T1 operating modes. The four available modes are shown in Figure 22.

It should be noted that the microprocessor does not write directly into the low-order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low-order register when the microprocessor writes into the high-order register and counter. In fact, it may not be necessary to write to the low-order register in some applications since the timing operation is triggered by writing to the high-order register and counter.

Timer 1: One-Shot Mode

Interval Timer T1 may operate in the One-Shot Mode which allows the generation of a single Interrupt Flag each time the Timer is loaded. The Timer can also be programmed to produce a single negative pulse on Data Port line PB7.

To generate a single interrupt, it is required that bits 6 and 7 of the Auxiliary Control Register be low (Logic 0). The low-order T1 counter (T1C-L) or the low-order T1 latch (T1L-L) must then be loaded with the low-order count value. Note that a load to T1C-L is effectively a load to T1L-L. Next, the high-order count value must be loaded into the high-order T1 counter (T1C-H), at which time the value is simultaneously loaded into high-order T1 latch (T1L-H). During this load sequence, the contents of T1L-L is transferred to T1C-L. The counter will start counting down on the next $\emptyset_2$ clock following the load sequence into T1C-H, and will decrement at the $\emptyset_2$ clock rate. Once the T1 counter reaches a zero count, the Interrupt Flag is set. To generate a negative pulse on Data Port line PB7, the sequence is identical to the above except bit 7 of the Auxiliary Control Register must be high (Logic 1). Data Port line PB7 will then go low (Logic 0) following the load to T1C-H, and will go high (Logic 1) again when the counter reaches a zero count.

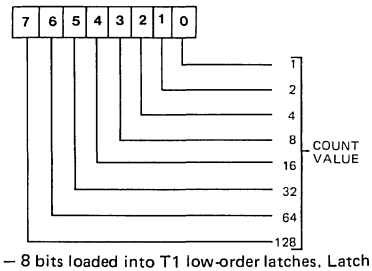
Once set, the T1 Interrupt Flag is reset by either loading T1C-H, which starts a new count, or by reading T1C-L. Refer to Figure 23 for One-Shot Mode timing information.

Timer 1: Free-Run Mode

An important advantage within the NCR65C22 is the ability of the latches associated with the T1 counter to provide a continuous series of evenly spaced interrupts or a square wave on Data Port line PB7. It should also be noted that the continuous series of interrupts and square waves are not effected by variations in the microprocessor interrupt response time. These advantages are all produced in the Free-Run Mode. When operating in the Free-Run Mode, the Interrupt Flag is set and the signal on PB7 is inverted each time the counter reaches a count of zero. In the Free-Run Mode, however, the counter does not continue to decrement after reaching a zero count. Instead, the counter automatically transfers to contents of the latch into the counter (16 bits) and then decrements from the new count value. As can be seen, it is not necessary to reload the timer in order to set the Interrupt Flag on the next count of zero. When set, the Interrupt Flag can be cleared by either reading T1C-L, by writing directly into the Interrupt Flag Register (IFR) as will be discussed later, or by a load into T1C-H when a new count value is desired.

Since the interval timers are all retriggerable, reloading the counter will always reinitialize the time-out period. Should the microprocessor continue to reload the counter before it reaches zero, counter time-out can be prevented. Timer 1 is able to operate in this manner provided the microprocessor writes into the high-order counter (T1C-H). By loading the latches only, the microprocessor can access the timer during each count-down operation without effecting the time-out in progress. In this way, data loaded into the latches will determine the length of the next subsequent time-out period. This capability is of value in the Free-Run Mode with the output enabled. In the Free-Run Mode, the signal on Data Port line PB7 is inverted and the Interrupt Flag is set with each counter time-out. When the microprocessor responds to the interrupts with new data for the latches, it can determine the period of the next half-cycle during each half-cycle of the output signal on line PB7. In this way, complex waveforms can be generated. Refer to Figure 24 for timing information on the Free-Run Mode.

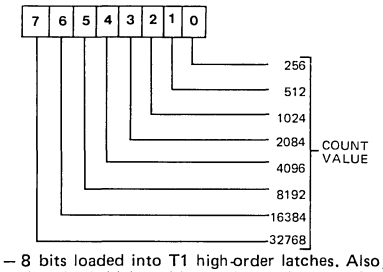
REG 4 – TIMER 1 LOW-ORDER COUNTER



WRITE – 8 bits loaded into T1 low-order latches. Latch contents are transferred into low-order counter at the time the high-order counter is loaded (Reg.5).

READ – 8 bits from T1 low-order counter transferred to MPU. In addition, T1 interrupt flag is reset (bit 6 in interrupt flag register).

REG 5 – TIMER 1 HIGH-ORDER COUNTER

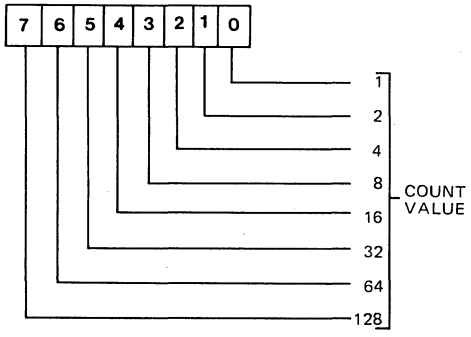


WRITE – 8 bits loaded into T1 high-order latches. Also, at this time both high and low-order latches transferred into T1 counter, and initiates countdown. T1 interrupt flag also is reset.

READ – 8 bits from T1 high-order counter transferred to MPU.

Figure 20. T1 Counter Format and Operation

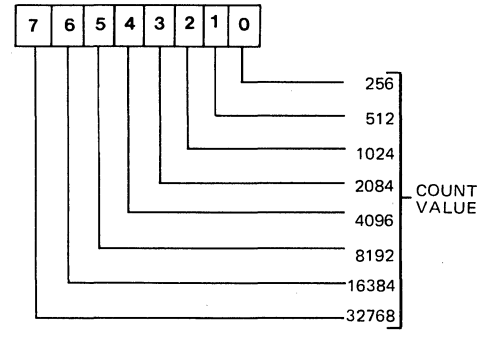
REG 6 – TIMER 1 LOW-ORDER LATCHES



WRITE – 8 bits loaded into T1 low-order latches. This operation is no different than a write into Reg. 4.

READ – 8 bits from T1 low-order latches transferred to MPU. Unlike Reg. 4 operation, this does not cause reset of T1 interrupt flag.

REG 7 – TIMER 1 HIGH-ORDER LATCHES

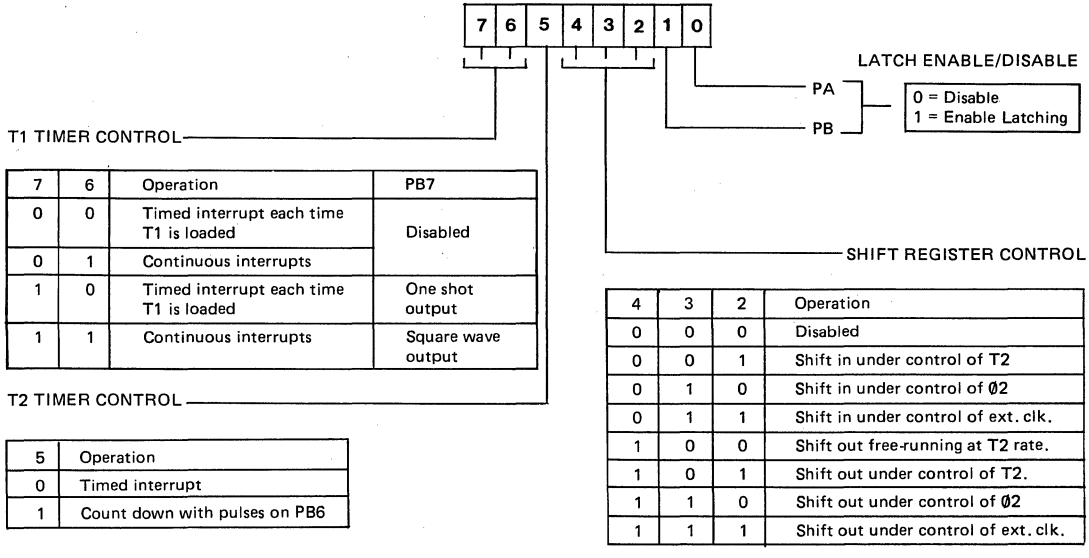


WRITE – 8 bits loaded into T1 high-order latches. Unlike Reg. 4 operation no latch-to-counter transfers take place.

READ – 8 bits from T1 high-order latches transferred to MPU.

Figure 21. T1 Latch Format and Operation

REG 11 – AUXILIARY CONTROL REGISTER



7	6	Operation	PB7
0	0	Timed interrupt each time T1 is loaded	Disabled
0	1	Continuous interrupts	
1	0	Timed interrupt each time T1 is loaded	One shot output
1	1	Continuous interrupts	Square wave output

5	Operation
0	Timed interrupt
1	Count down with pulses on PB6

4	3	2	Operation
0	0	0	Disabled
0	0	1	Shift in under control of T2
0	1	0	Shift in under control of Ø2
0	1	1	Shift in under control of ext. clk.
1	0	0	Shift out free-running at T2 rate.
1	0	1	Shift out under control of T2.
1	1	0	Shift out under control of Ø2
1	1	1	Shift out under control of ext. clk.

Figure 22. Auxiliary Control Register Format and Operation

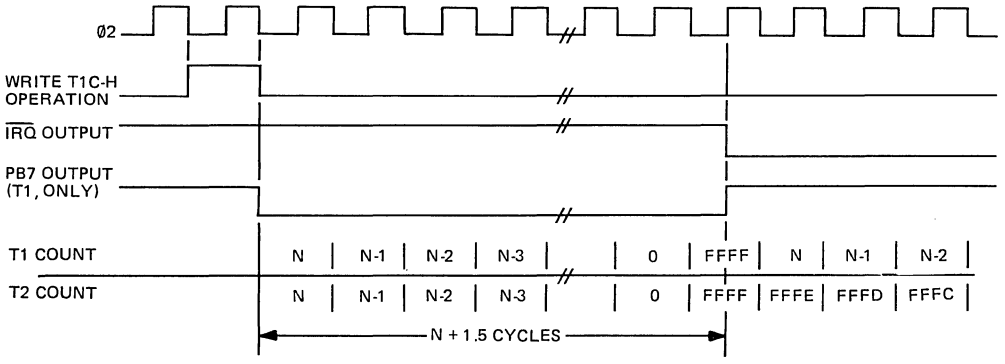
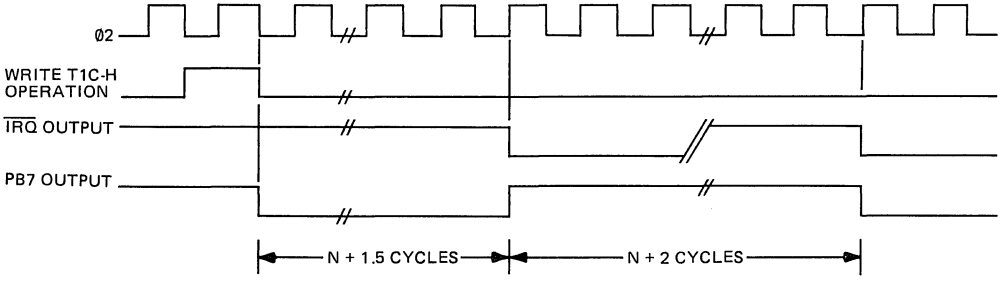


Figure 23. One-Shot Mode Timing (Timer 1 and Timer 2)



Note: A precaution to take in the use of PB7 as the timer output concerns the Data Direction Register contents for PB7. Both DDRB bit 7 and ACR bit 7 must be 1 for PB7 to function as the timer output. If either is a 0, then PB7 functions as a normal output pin, controlled by ORB bit 7.

Figure 24. Free-Run Mode Timing (Timer 1)

Timer 2: Operation
Timer 2 operates in the One-Shot Mode only (as an interval timer), or as a pulse counter for counting negative pulses on Data Port Line PB6. A single control bit within the Auxiliary Control Register is used to select between these two modes. Timer 2 is made up of a write-only low-order latch (T2L-L), a read-only low-order counter (T2C-L), and a read/write high-order counter (T2C-H). This 16-bit counter decrements at a $Ø_2$ clock rate. Refer to Figure 25 for T2 counter format and operation.

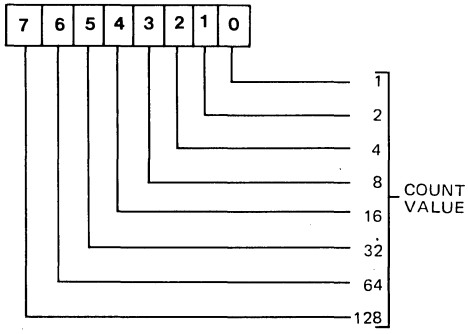
Timer 2: One-Shot Mode
Operation of Timer 2 in the One-Shot Mode is similar to Timer 1. That is, for each load T2C-H operation, Timer 2 sets the Interrupt Flag for each countdown to zero. However, after a time-out, the T2 counters roll over to all 1s ($ FFFF)* and continue to decrement. This two's complement decrement allows the user to determine how long the T2 Interrupt Flag has been set. Since the Interrupt Flag logic is disabled after the initial interrupt set (zero count), further interrupts cannot be set by a subsequent count to zero. To enable the Interrupt Flag logic, the microprocessor must reload T2C-H. The Interrupt Flag is cleared by either reading T2C-L or by loading T2C-H. Refer to Figure 23 for timing information on the One-Shot Mode.

Timer 2: Pulse Counting Mode
In the Pulse Counting Mode, Timer 2 counts a predetermined number of negative-going pulses on Data Port line PB6. To accomplish this, a count number is loaded into T2C-H, which clears the Interrupt Flag logic and starts the counter to decrement each time a negative pulse is applied to Data Port line PB6. When the T2 counter reaches a count of zero, the Interrupt Flag is set and the counter continues to decrement with each pulse on PB6. To enable the Interrupt Flag for subsequent countdowns, it is necessary to reload T2C-H. The decrement pulse on line PB6 must be low (Logic 0) during the leading edge of the $Ø_2$ clock. Refer to Figure 26 for timing information.

Shift Register Operation
The Shift Register performs bidirectional serial data transfers on line CB2. These transfers are controlled by an internal modulo-8 counter. Shift pulses can be applied to the CB1 line from an external source, or (with proper mode selection) shift pulses may be generated internally which will appear on the CB1 line for controlling external devices. Each Shift Register operating mode is controlled by control bits within the Auxiliary Control Register. Refer to Figure 27 for format and control bit information. Also refer to Figures 28 through 34 for operation of the various Shift Register modes.

*$ denotes hexadecimal.

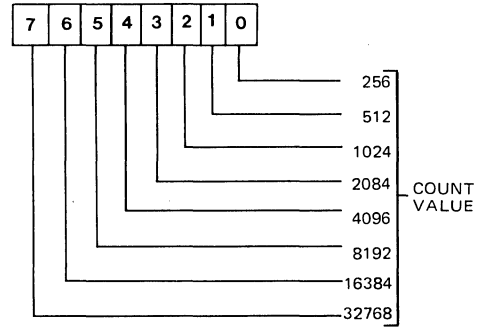
REG 8 – TIMER 2 LOW-ORDER LATCHES



WRITE – 8 bits loaded into T2 low-order latches.

READ – 8 bits from T2 low-order counter transferred to MPU. T2 interrupt flag is reset.

REG 9 – TIMER 2 HIGH-ORDER LATCHES



WRITE – 8 bits loaded into T2 high-order counter. Also low-order latches transferred to low-order counter. In addition, T2 interrupt flag is reset.

READ – 8 bits from T2 high-order counter transferred to MPU.

Figure 25. T2 Counter Format and Operation

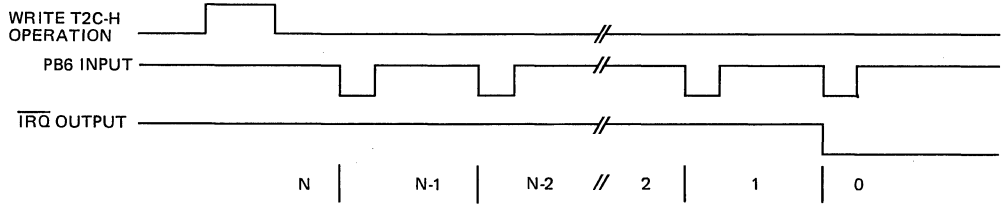


Figure 26. Pulse Counting Mode Timing (Timer 2)

Shift Register Input Modes

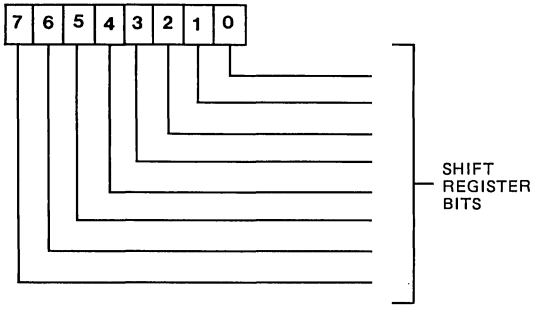
Shift Register Disabled (000) – In the 000 mode, the Shift Register is disabled from all operation. The microprocessor can read or write the Shift Register, but shifting is disabled and both CB1 and CB2 are controlled by bits in the Peripheral Control Register (PCR). The Shift Register Interrupt Flag is held low (disabled).

Shift In – Counter T2 Control (001) – In this mode, the shifting rate is controlled by the low-order eight bits of counter T2. Shift pulses are generated on the CB1 line to control shifting in external devices. The time between transitions of the CB1 output clock is determined by the $\emptyset_2$ clock period and the contents of the low-order T2 latch (N). Shifting occurs by writing or reading the Shift Register. Data is shifted into the low-order bit first, and is then shifted into the next higher order bit on the negative-going edge of each clock pulse. Input data should change before the positive-going edge of the CB1 clock pulse. This data is then shifted into the Shift Register during the $\emptyset_2$ clock cycle following the positive-going edge of the CB1 clock pulse. After eight CB1 clock pulses, the Shift Register Interrupt Flag will set and $\overline{IRQ}$ will go low (Logic 0). Refer to Figure 28.

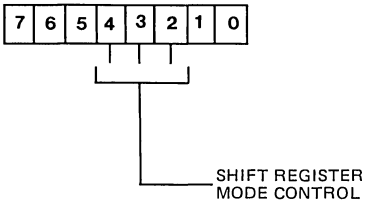
Shift In – $\emptyset_2$ Clock Control (010) – In this mode, the shift rate is controlled by the $\emptyset_2$ clock frequency. Shift pulses are generated on the CB1 line to control shifting in external devices. Timer 2 operates as an independent interval timer and has no influence on the Shift Register. Shifting occurs by reading or writing the Shift Register. Data is shifted into the low-order bit first, and is then shifted into the next higher order bit on the trailing edge of the $\emptyset_2$ clock pulse. After eight clock pulses, the Shift Register Interrupt Flag will be set and output clock pulses on the CB1 line will stop. Refer to Figure 29.

Shift In – External CB1 Clock Control (011) – In this mode CB1 serves as an input to the Shift Register. In this way, an external device can load the Shift Register at its own pace. The Shift Register counter will interrupt the microprocessor after each eight bits have been shifted in. The Shift Register counter does not stop the shifting operation. Its function is simply that of a pulse counter. Reading or writing the Shift Register resets the Interrupt Flag and initializes the counter to count another eight pulses. Note that data is shifted during the first $\emptyset_2$ clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high. Refer to Figure 30.

REG 10 – SHIFT REGISTER



REG 11 – AUXILIARY REGISTER



4	3	2	Operation
0	0	0	Disabled
0	0	1	Shift in under control of T2
0	1	0	Shift in under control of Ø2
0	1	1	Shift in under control of ext. clk
1	0	0	Shift out free-running at T2 rate
1	0	1	Shift out under control of T2
1	1	0	Shift out under control of Ø2
1	1	1	Shift out under control of ext. clk

Notes:
1. When shifting out, bit 7 is the first bit out and simultaneously is rotated back into bit 0.
2. When shifting in, bits initially enter bit 0 and are shifted towards bit 7.

Figure 27. Shift Register and Auxiliary Control Register Control Bits

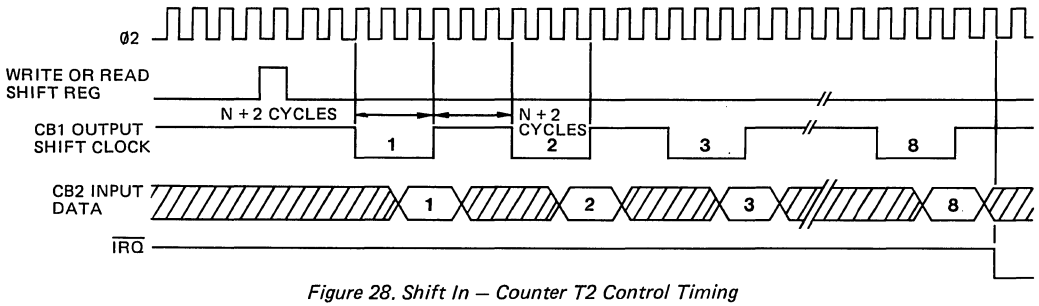


Figure 28. Shift In – Counter T2 Control Timing

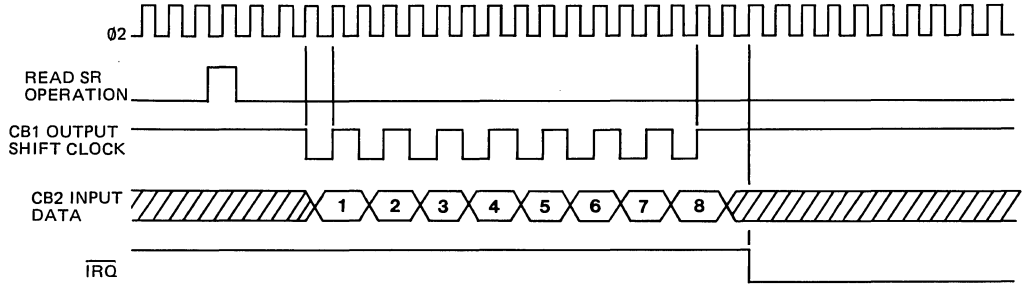


Figure 29. Shift In – Ø2 Clock Control Timing

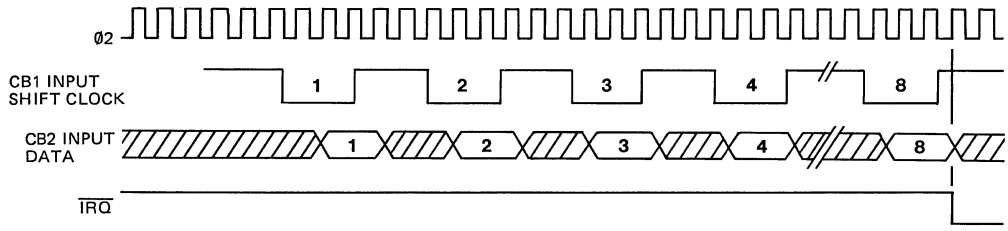


Figure 30. Shift In – External CB1 Clock Control Timing

Shift Register Output Modes

Shift Out – Free Running at T2 Rate (100) – This mode is similar to mode 101 in which the shifting rate is determined by T2. However, in mode 100 the Shift Register Counter does not stop the shifting operation. Since Shift Register bit 7 (SR7) is recirculated back into bit 0, the eight bits loaded into the Shift Register will be clocked onto the CR2 line repetitively. In this mode, the Shift Register Counter is disabled and $\overline{IRQ}$ is never set. Refer to Figure 31.

Shift Out – T2 Control (101) – In this mode, the shift rate is controlled by T2 (as in mode 100). However, with each read or write of the Shift Register, the Shift Register Counter is reset and eight bits are shifted onto the CB2 line. At the same time, eight shift pulses are placed on the CB1 line to control shifting in external devices. After the eight shift pulses, the shifting is disabled, the Interrupt Flag is set, and CB2 will remain at the last data level. Refer to Figure 32.

Shift Out – $Ø_2$ Clock Control (110) – In this mode, the shift rate is controlled by the system $Ø_2$ Clock. Refer to Figure 33.

Shift Out – External CB1 Clock Control (111) – In this mode, shifting is controlled by external pulses applied to the CB1 line. The Shift Register Counter sets the Interrupt Flag for each eight-pulse count, but does not disable the shifting function. Each time the microprocessor reads or writes the Shift Register, the Interrupt Flag is reset and the counter is initialized to begin counting the next eight pulses on the CB1 line. After eight shift pulses, the Interrupt Flag is set. The Microprocessor can then load the Shift Register with the next eight bits of data. Refer to Figure 34.

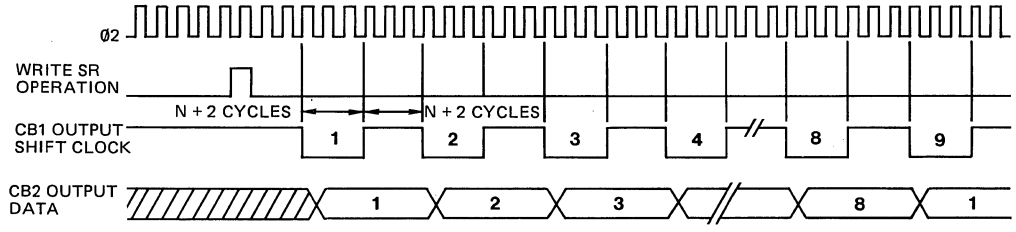


Figure 31. Shift Out – Free Running T2 Rate Timing

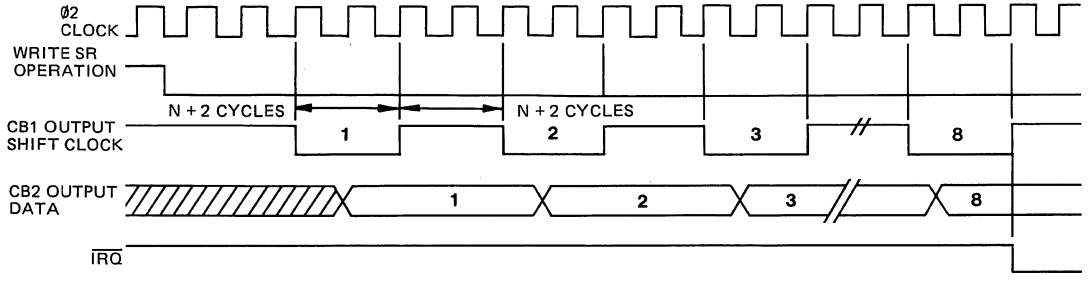


Figure 32. Shift Out – T2 Control Timing

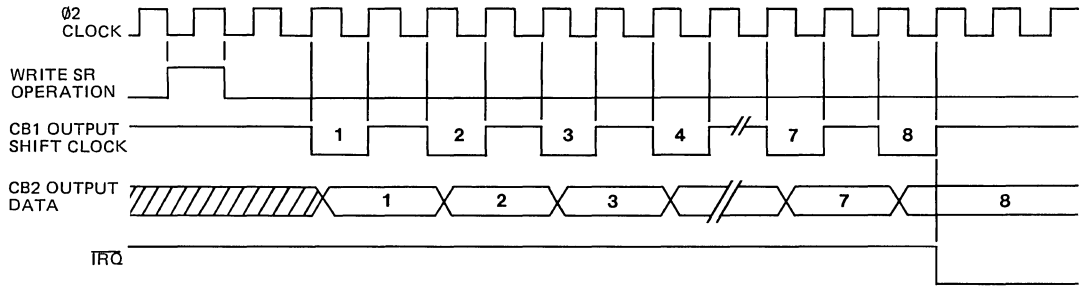


Figure 33. Shift Out – Ø2 Control Timing

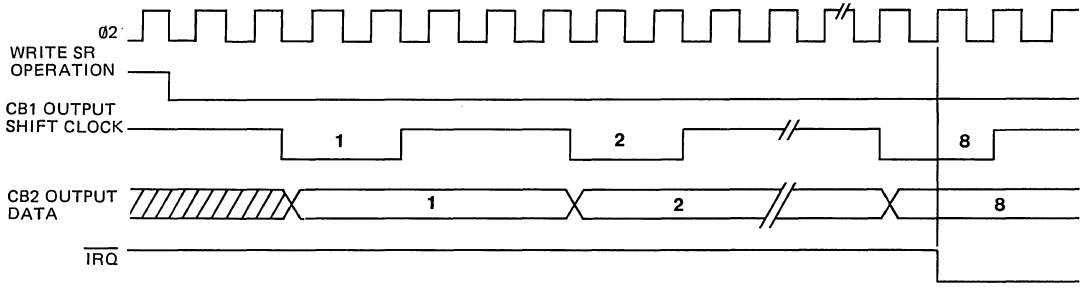


Figure 34. Shift Out – External CB1 Clock Control Timing

Interrupt Operation

There are three basic interrupt operations, including: setting the interrupt flag within the Interrupt Flag Register (IFR), enabling the interrupt by way of a corresponding bit in the Interrupt Enable Register (IER), and signaling the microprocessor with an Interrupt Request ($\overline{IRQ}$). An Interrupt Flag can be set by conditions internal to the chip or by inputs to the chip from external sources. Normally, an Interrupt Flag will remain set until the interrupt is serviced. To determine the source of an interrupt, the microprocessor must examine each flag in order, from highest to lowest priority. This is accomplished by reading the contents of the Interrupt Flag Register into the microprocessor accumulator, shifting the contents either left or right and then using conditional branch instructions to detect an active interrupt. Each Interrupt Flag has a corresponding Interrupt Enable bit in the Interrupt Enable Register. The enable bits are controlled by the microprocessor (set or cleared). If an Interrupt Flag is high (Logic 1), and the corresponding Interrupt Enable bit is high (Logic 1), the Interrupt Request ($\overline{IRQ}$) will go low (Logic 0). $\overline{IRQ}$ is an open-collector output which can be wire-ORed with other devices within the system.

All Interrupt Flags are contained within a single Interrupt Flag Register. Bit 7 of this register will be high (Logic 1) whenever an Interrupt Flag is set, thus allowing convenient polling of several devices within a system to determine the source of the interrupt.

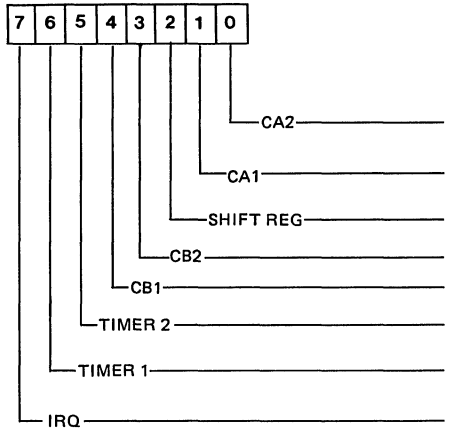
The Interrupt Flag Register (IFR) and Interrupt Enable Register (IER) format and operation is shown in Figures 35 and 36 respectively. The Interrupt Flag Register may be read directly by the microprocessor, and individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. Bit 7 of the IFR indicates the status of the Interrupt Request ($\overline{IRQ}$) output. Bit 7 corresponds to the following logic function: IRQ = IFR6 x IER6 + IFR5 x IER5 + IFR4 x IER4 + IFR3 x IER3 + IFR2 x IER2 + IFR1 x IER1 + IFR0 x IER0. Note: x = Logic AND, + = Logic OR.

Bit 7 is not a flag. For this reason, bit 7 is not directly cleared by writing a "1" into its bit position. It can be cleared, however, by clearing all the flags within the register, or by disabling all active interrupts as presented in the next section.

Each Interrupt Flag within the IFR has a corresponding enable bit in the Interrupt Enable Register (IER). The microprocessor can set or clear selected bits within the IER. This allows the control of individual interrupts without effecting others. To set or clear a particular Interrupt Enable bit, the microprocessor must write to address 1110 (IER address). During this write operation, if bit 7 on the Data Bus is a "0", each "1" in bits 6 through 0 will clear the corresponding bit in the Interrupt Enable Register. For each "0" in bits 6 through 0, the corresponding bit in the IER will be unaffected.

Setting selected bits in the IER is accomplished by writing to the same address with bit 7 on the Data Bus set to a "1". In this case, each "1" in bits 6 through 0 will set the corresponding bit to a "1". For each "0", the corresponding bit will be unaffected. This method of controlling the bits in the Interrupt Enable Register allows convenient user control of interrupt during system operation. The microprocessor can also read the contents of the IER by placing the proper address on the Register Select and Chip Select inputs with the R/$\overline{W}$ line high Bit 7 will be read as a "1".

REG 13 – INTERRUPT FLAG REGISTER

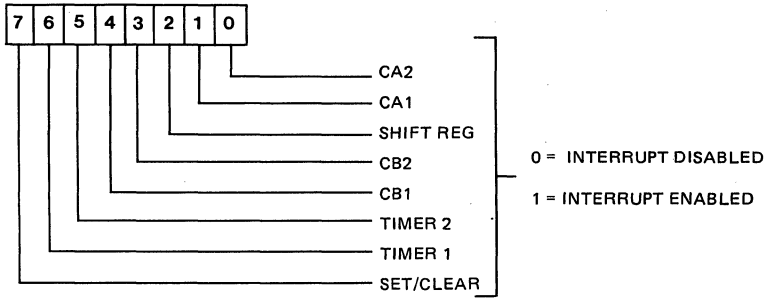


SET BY	CLEARED BY
CA2 active edge	Read or write Reg. 1 (ORA)*
CA1 active edge	Read or write Reg. 1 (ORA)
Complete 8 shifts	Read or write Shift Reg.
CB2 active edge	Read or write ORB*
CB1 active edge	Read or write ORB
Time-out of T2	Read T2 low or write T2 high
Time-out of T1	Read T1 low or write T1 high
Any enabled interrupt	Clear all interrupts

*If the CA2/CB2 control in the PCR is selected as "independent" interrupt input, then reading or writing the output register ORA/ORB will not clear the flag bit. Instead, the bit must be cleared by writing into the IFR, as described previously.

Figure 35. Interrupt Flag Register (IFR)

REG 14 – INTERRUPT ENABLE REGISTER

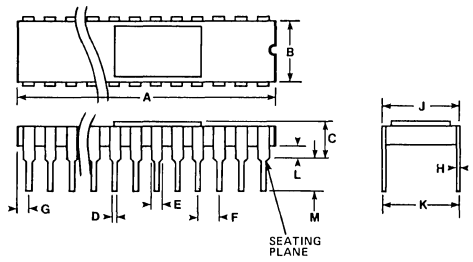


Notes:
1. If bit 7 is a "0", then each "1" in bits 0-6 disables the corresponding interrupt.
2. If bit 7 is a "1", then each "1" in bits 0-6 enables the corresponding interrupt.
3. If a read of this register is done, bit 7 will be "1" and all other bits will reflect their enable/disable state.

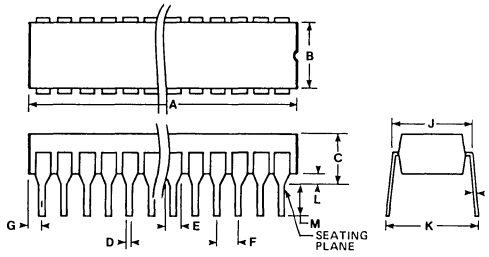
Figure 36. Interrupt Enable Register (IER)

■ PACKAGING INFORMATION

Typical Outline Drawing (Ceramic)



Typical Outline Drawing (Plastic & Cerdip)



40 PIN CERAMIC PACKAGE				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.419	51.181	1.985	2.015
B	14.605	15.367	0.575	0.605
C		3.810		0.150
D	0.381	0.533	0.015	0.021
E	0.889	1.524	0.035	0.060
F	2.286	2.794	0.090	0.110
G	1.016	1.524	0.040	0.060
H	0.203	0.305	0.008	0.012
J	15.113	15.875	0.590	0.620
K	15.24	REF	0.600	REF
L	0.889	1.651	0.035	0.065
M	2.540	3.556	0.100	0.140

40 PIN PLASTIC PACKAGE				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
E	1.02	1.52	0.040	0.060
F	2.54	TYP	0.100	TYP
G	1.65	2.16	0.065	0.085
H	0.20	0.38	0.008	0.015
J	15.24	TYP	0.600	TYP
K				
L	0.51	1.02	0.020	0.040
M	2.92	3.43	0.115	0.135

NCR

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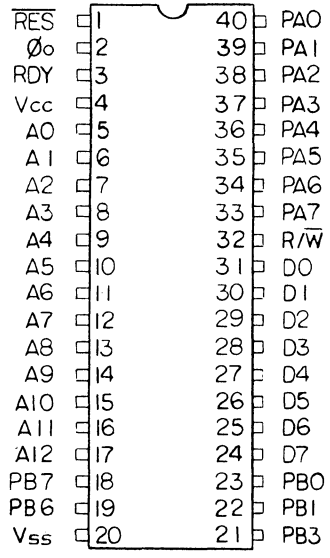
6518 SINGLE-CHIP MICROPROCESSOR WITH RAM AND I/O

PRELIMINARY

- 6507 CPU
  - 8-bit parallel processing
  - 13 addressing modes
  - Decimal and binary arithmetic modes
  - True indexing capability
  - 56 instructions
- 128 x 8 static RAM
- Two bidirectional TTL-compatible programmable I/O ports, one 8-bit, and one 5-bit
- Two programmable peripheral data direction registers
- 8-bit bidirectional data bus
- Programmable stack pointer
- Programmable interval timer with interrupt flag
- Variable length stack
- Addressable memory range of up to 8K bytes
- Bus compatible with M6800
- Pipeline architecture
- Use with any type or speed memory
- Up to 1.25 MHz clock frequency
- NMOS silicon gate, depletion load
- Single +5V power supply

The NCR 6518 is a low-cost microcomputer system capable of solving a broad range of small systems and peripheral control problems. It consists of a 6507 CPU; 128 bytes of RAM; two bidirectional I/O ports: one 8-bit and one 5-bit; and a programmable interval timer with interrupt flag. The internal processor architecture is software compatible with the 6502.

PIN CONFIGURATION



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FUNCTIONAL DESCRIPTION

The NCR 6518 has combined the functions of a 6507 microprocessor along with on-board RAM, I/O and timer logic. The functional block diagram shows the various elements of the device.

To understand the basic operation of the processor, we will briefly consider the register sections of the chip as follows:

- Input Data Latch
- Data Bus Buffers
- Accumulator
- Arithmetic Logic Unit
- Program Counter
- Index Registers X and Y
- Address Bus Latches
- Stack Pointer

At full operating frequency, data which comes into the microprocessor from program or data memory or from a peripheral device, appear on the data bus during one cycle and are transferred into the input data latch during the next cycle. After the data has been trapped on the data bus, it can then be transferred onto one of the internal busses and then into one of the internal registers.

As an example, data being moved from memory to the accumulator (A) will be put on the internal data bus and then transferred into the accumulator. If a logic operation or an arithmetic operation is to be performed using the contents of the accumulator and memory data, then the memory data in the input data latch will be transferred first onto the internal data bus and then into one input of the arithmetic logic unit (ALU). During the same instruction cycle, the contents of the accumulator will be transferred onto a bus and then into the second ALU input. The results of the operation will be transferred back to the accumulator via the bus on the next cycle.

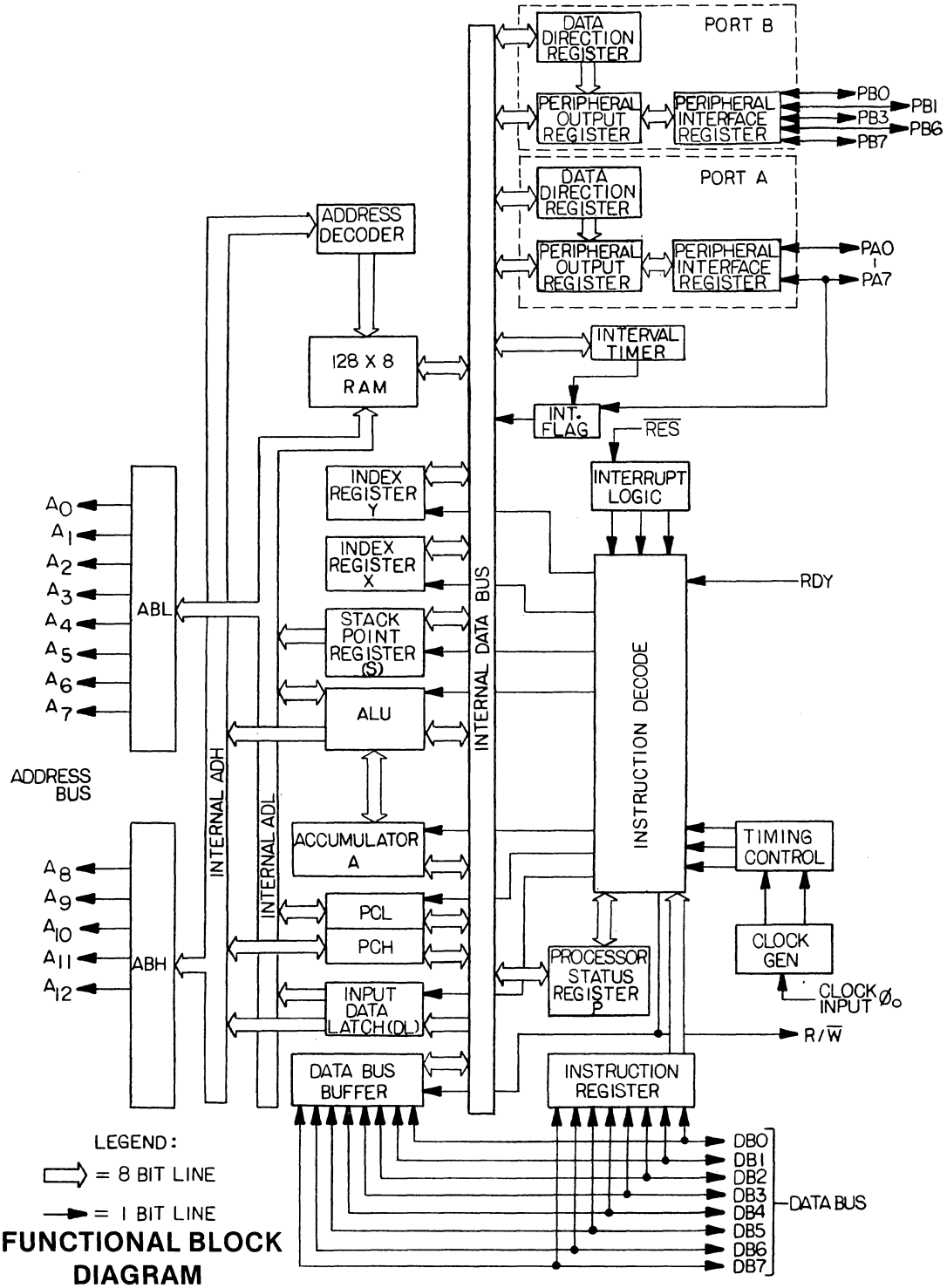
The microprocessor is sequenced through program instructions by the program counter (PCL,PCH) which provides the memory addresses. For each instruction fetch, the contents of PCL are placed on the low-order 8 bits of the address bus and the contents of PCH are placed onto the high order 8 bits. The program counter is automatically incremented with each instruction fetch.

The accumulator is a general purpose 8-bit register which is commonly used for storing the result of a logic or arithmetic operation. The accumulator is also often the source for one of the operands for these operations.

The arithmetic logic unit (ALU) is the site for all arithmetic and logic operations. By tying each of the ALU inputs to one of the several internal busses (or logic zero), various logic or arithmetic functions can be calculated. However, since the ALU cannot store data for more than one cycle, the result of each operation must be sent to one of the storage registers or external memory on the next cycle.

Three other device registers store data which are used for calculating addresses in memory. The X and Y index registers are each 8-bit latches whose values are used for various modes of data memory addressing. The stack pointer (S) is also an 8-bit latch which keeps track of the stack and allows for easy modification of program memory address.

The address bus latches (ABL,ABH) consist of 13 latches which can store the addresses used to access external ROM, RAM or I/O.



FUNCTIONAL BLOCK DIAGRAM

PIN DESCRIPTIONS

Pin	Description
$\overline{RES}$	The $\overline{RES}$ input is used to reset the microprocessor or initialize the device from a power-down condition. During the power up time, this line must be held low for at least two clock cycles after the power supply reaches minimum VCC. While that line is held low, writing to or from the processor is inhibited. When RES goes high, the microprocessor will delay 6 clock cycles and then load the program counter from memory vector locations FFFC and FFFD. This the starting location for the user's program.
ø0	TTL-Compatible single phase clock input.
RDY	The ready input delays execution of any cycle during which the RDY line is pulled low. The primary purpose of this line is to delay the execution of a program fetch cycle until data are available from memory. This allows the microprocessor to interface with both low and high speed memory.
VCC	Main power supply = 5V (+/− 5%)
A0-A12	TTL-Compatible address bus outputs, capable of driving one standard TTL load and 130 PF.
PB0-PB1 PB3 PB6-PB7	Peripheral data port B. I/O lines are each individually software programmable as either an input or output line. The pins are set as inputs by writing a "0" to the corresponding bit in the data direction register (DDRB). Writing a "1" to a bit in the DDRB will set the corresponding pin as an output. The outputs are capable of driving one standard TTL load and 130 PF. Note only 5 PB are available.
VSS	Signal Ground.
PA0-PA7	Peripheral data port A I/O lines. These pins function as do those in port B, but are controlled by a separate data direction register (DDRB). In addition to its function as an I/O line, PA7 can be used as an edge-detecting input.
R/$\overline{W}$	The read/$\overline{write}$ signal is generated by the microprocessor to control the direction of data transfers on the data bus. This line will be high except when the microprocessor is writing to memory, or to a peripheral device.
D0-D7	Bidirectional data bus. The outputs are tri-state buffers capable of driving one standard TTL load and 130 PF.

DEVICE OPERATION

CENTRAL PROCESSING UNIT (CPU)

The CPU is a 6507 configuration with standard 6502 instructions. It features an on-chip clock, 8-bit bidirectional data bus and 8K bytes of addressable memory.

RANDOM ACCESS MEMORY (RAM)

The 128 x 8 read/write memory acts as a conventional static RAM. Data can be written to memory by selecting the RAM (A7 = 1, A12 = 0) and setting A9 to a logic 0. Address lines A0 through A6 then select the desired byte in RAM.

INTERNAL PERIPHERAL REGISTERS

I/O port PA consists of eight lines each of which can be programmed to function as either an input or output. A logic zero in the corresponding bit of the data direction register (DDRA) sets up that line of the PA port as an input. Similarly, a logic one will configure that line as an output. If a line in PA is programmed as an output, the logic level of that output is determined by the corresponding bit in the output register (ORA).

Data is read directly from PA pins during any read operation. For any output pin, data transferred into the microprocessor will be the same as that contained in the output register if the voltage on the pin is allowed to go to a logic one. For input lines, the processor can write into the corresponding bit of the output register. This will not affect the polarity of the pin until the corresponding bit of the DDRA is set to a logic one, changing the pin to an output.

Along with its function as an I/O line, PA7 also can be used as an edge-detecting input. In this mode, an active transition on this pin will set the internal interrupt flag (Bit 6 of the Interrupt Flag Register). The edge-detecting mode of PA7 is controlled by writing to one of two addresses. The polarity of the transition is determined by the state of A0. Any data which is placed on the data bus during this operation is discarded and does not affect control of A7.

An active transition on PA7 will set the internal interrupt flag. Even if pin PA7 is being used as a normal I/O line. The reset signal (RES) will set the polarity of the active transition to negative (high to low). During system initialization, it is possible to set the interrupt flag by a negative transition. Clearing of the PA7 interrupt flag occurs when the interrupt flag register is read.

The second I/O port - PB, functions the same as the normal I/O operation of PA. The five lines (PB0, PB1, PB3, PB6, PB7) are controlled via the DDRB and ORB in similiar fashion to the control of PA.

INTERVAL TIMER

The interval timer can be programmed to count as many as 255 time intervals. Using the divide down, each interval can be T, 8T, 64T, or 1024T where T is the system clock period. When a full count down is complete, the interrupt flag is set and internal clock begins decrementing to a maximum of 255T. Therefore, after the interrupt flag is set, a read of the timer will tell how long it has been since the flag was set (up to a maximum of 255T).

The system data bus is used to transfer data to and from the interval timer. At the same time data is written to the timer, the preliminary divide down value (1, 8, 64, 1024) is decoded from the address lines A0 and A1. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read.

When the timer has counted down through 00 (00000000), an interrupt will occur on the next count and

the counter will read FF (11111111). After the interrupt, the counter will decrement at a divide by "1" rate of the system clock. If the timer is read after an interrupt and, for example, the value E4 (11100100) is obtained, the time elapsed since the interrupt is 27T.

The value read is in two's complement, but remembering that the interrupt occurred at FF (11111111), we simply take this difference.

Value at Interrupt	11111111
- Value Read	11100100
Elapsed Time	00011011 = 27

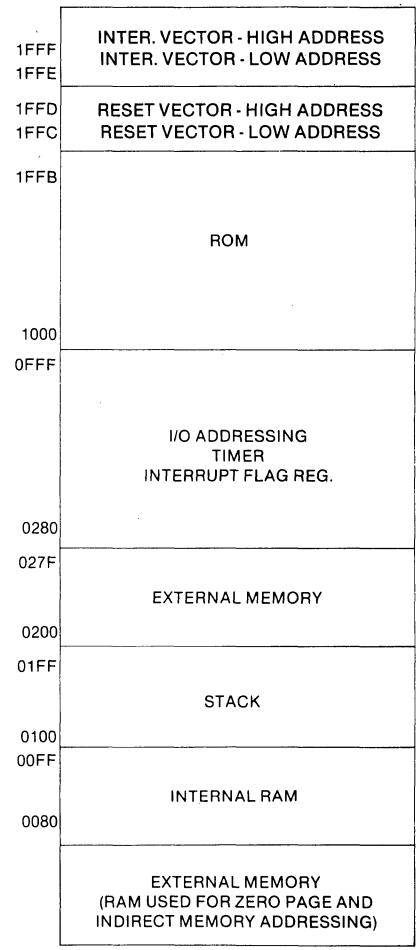
After the interrupt, when the timer is written to or read from, the interrupt flag is reset. However, reading the timer at the same time the interrupt occurs, will not reset the interrupt flag.

ADDRESS BUS DECODE FOR NCR 6518

FUNCTION	A9	A6	A5	A4	A3	A2	A1	A0	R/W	COMMENT
RAM ADDRESSING	0 (RAM ADDRESS SELECT) —									
I/O Addressing Read	1	—	—	—	—	0	0	0	1	PA Data
	1	—	—	—	—	0	0	1	1	PA Data Direction
	1	—	—	—	—	0	1	0	1	PB Data
	1	—	—	—	—	0	1	1	1	PB Data Direction
I/O Addressing Write	1	—	—	—	—	0	0	0	0	PA Data
	1	—	—	—	—	0	0	1	0	PA Data Direction
	1	—	—	—	—	0	1	0	0	PB Data
	1	—	—	—	—	0	1	1	0	PB Data Direction
Write Edge Detect Control	1	—	—	0	—	1	—	1	0	Positive Edge (PA7)
	1	—	—	0	—	1	—	0	0	Negative Edge (PA7)
Read and Clear Interrupt Flag	1	—	—	—	—	1	—	1	1	Bit 7 = Timer Flag Bit 6 = PA7 Flag
Read Interval Timer	1	—	—	—	—	1	—	0	1	
Write Count to Interval Timer	1	—	—	1	—	1	0	0	0	Divide by 1
	1	—	—	1	—	1	0	1	0	Divide by 8
	1	—	—	1	—	1	1	0	0	Divide by 64
	1	—	—	1	—	1	1	1	0	Divide by 1024

NOTE: FOR ALL OPERATIONS, A7 = 1, A12 = 0
—INDICATES A DON'T CARE STATE

NCR 6518 MEMORY MAP



MAXIMUM RATINGS

PRELIMINARY

RATING	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	—0.3 to +7.0	V
Input/Out Voltage	V_{IN}	—0.3 to 7.0	V
Operating Temperature Range	T_{op}	0 to 70	°C
Storage Temperature Range	T_{STG}	—55 to 150	°C

All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside th specification range.

This is advance information and NCR reserves the right to change the specifications without notice.

ELECTRICAL CHARACTERISTICS

D.C. Characteristics

T_A = 25 °C, V_{CC} = 5.0V ± 5%, V_{SS} = 0V

Symbol	Parameter	Min.	Max.	Units	Test Conditions
	Capacitance at				
$C_{0\phi}$	Clock Input ϕ_o		15	pF	V_{in} = 0V f = 1.25 MHz
C_{OUT}	Address A0-A12, R/W		12	pF	
C_{IN}	Data Bus D0-D7		15	pF	
I_{IH}	Input High Current at Peripheral Data Ports				V_{in} = 2.4V
	PA0-PA7, PB (0,1,3,6,7)	—100		uA	
I_{IL}	Input Low Current at Peripheral Data Ports				V_{in} = 0.4V
	PA0-PA7, PB (0,1,3,6,7)		—1.6	mA	
I_{OL}	Output Low Current at Peripheral Data Ports				V_{OL} < 0.4V
	PA0-PA7, PB (0,1,3,6,7)	1.6		mA	
I_{OH}	Output High Current at Peripheral Data Ports				
	PA0-PA7, PB (0,1,3,6,7)	—100		uA	V_{OH} > 2.4V
	PB (0,1,3,6,7)	—3.0		mA	V_{OH} > 1.5V
C_{INP}	Input Capacitance at PA0-PA7, PB (0,1,3,6,7)		10	pF	
C_{OUTP}	Output Capacitance at PA0-PA7, PB (0,1,3,6,7)		10	pF	
V_{IH}	Input High Voltage	V_{SS} + 2.2	V_{CC} + 0.2.5	V	
V_{IL}	Input Low Voltage	V_{SS} —0.3	V_{SS} + 0.8	V	
I_{IN}	Input Leakage Current		2.5	uA	V_{in} = 0 to 5.25V
	for ϕ_o		10	uA	VCC = 0V

This is advance information and NCR reserves the right to change the specifications without notice.

D.C. Characteristics (continued)

Symbol	Parameter	Min.	Max	Units	Test Conditions
I_{TSI}	3-State Input Current		10	uA	V_{in} = 0.4 to 2.4V V_{CC} = 5.25V
V_{OH}	Output High Voltage				
	D0-D7 A0-A12 R/W	V_{SS} + 2.4		V	I_{LOAD} = —100 uADC VCC = 4.75V
	PA0-PA7, PB (0,1,3,6,7)	V_{SS} + 2.4		V	I_{LOAD} = -100 uA
	PB (0,1,3,6,7)	V_{SS} + 1.5		V	I_{LOAD} = —3 mA
V_{OL}	Output Low Voltage		V_{SS} + 0.4	V	I_{LOAD} = 1.6 mA VCC = 4.75V
I_{CC}	Maximum V_{CC}Current		70	mA	T_A = 25 °C
V_{ILC}	ϕ₀Input Low Voltage	0	0.4	V	
V_{IHC}	ϕ₀Input High Voltage	2.4	V_{CC} + 0.25	V	
$V_{IH}(\overline{RES})$	Reset Input High Voltage	V_{SS} + 2.19	V_{CC} + 0.25	V	For increasing V_{IN}
		V_{SS} + 1.20	V_{CC} + 0.25	V	For decreasing V_{IN}
$V_{IL}(\overline{RES})$	Reset Input Low Voltage	V_{SS} —0.3	V_{SS} + 1.87	V	For increasing V_{IN}
		V_{SS} —0.3	V_{SS} + 0.67	V	For decreasing V_{IN}

This is advance information and NCR reserves the right to change the specifications without notice.

A.C. CHARACTERISTICS

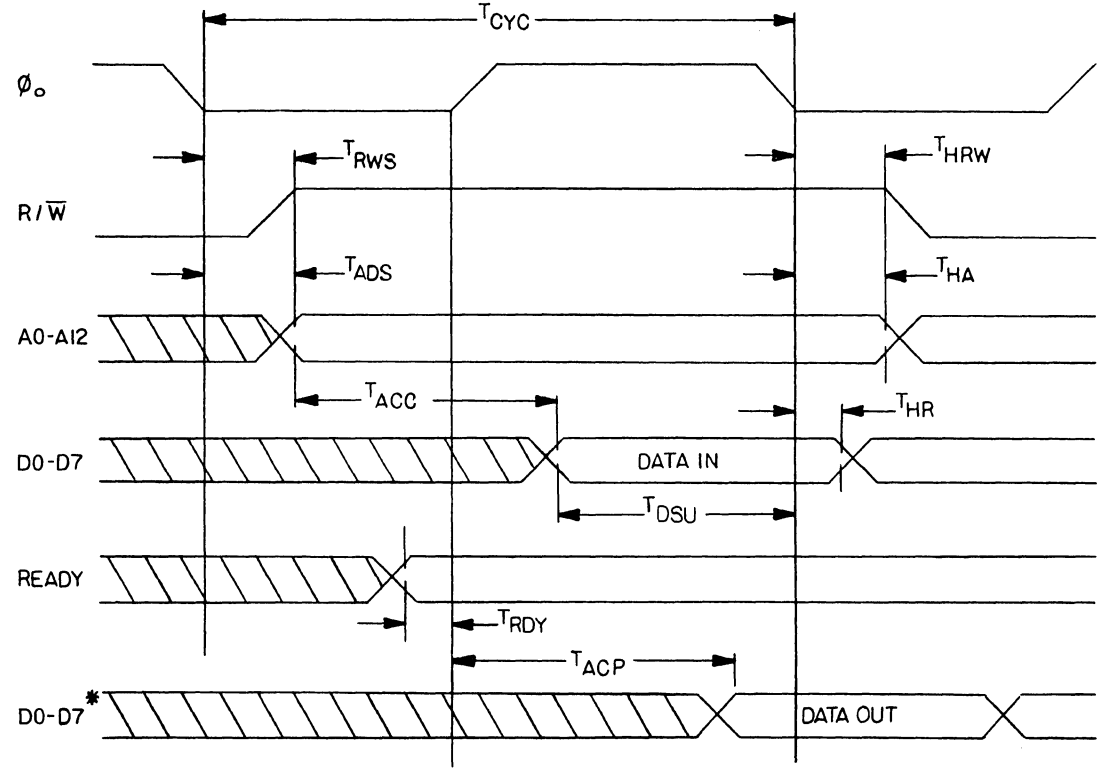
T_A = 25°C, V_{CC} = 5.0V ± 5%, V_{SS} = 0V

Symbol	Parameter	Min.	Max.	Units	Test Conditions
T_{CYC}	Cycle Time	0.8	100	μs	
$TR\phi_o$, $TF\phi_o$	ϕ_o Rise, Fall Time		10	ns	
$PWH\phi_o$	ϕ_o Pulse Width	375	62000	ns	
T_{RWS}	R/$\overline{W}$ Setup Time		280	ns	Loading = 130pF + 1 TTL Load for D0-D7, A0-A12, R/$\overline{W}$
T_{ADS}	Address Setup Time		280	ns	
T_{ACC}	Memory Read Access Time		410	ns	
T_{ACP}	Data Read Access Time for from Internal Logic		375	ns	
T_{DSU}	Data Stability Time Period	110		ns	
T_{HR}	Data Hold Time-Read	50		ns	
T_{HW}	Data Hold Time-Write	50		ns	
T_{MDS}	Data Setup Time		240	ns	
T_{RDY}	Ready Setup Time	130		ns	
T_{HA}	Address Hold Time	50		ns	
T_{HRW}	R/$\overline{W}$ Hold Time	50		ns	
T_{CMOS}	Peripheral Data Valid (writing into CMOS load)		1.6	μs	
T_{CPW}	Peripheral Data Valid after Falling Edge of ϕ_o (Writing)		0.8	μs	Loading = 30pF + 1 TTL Load for PA0-PA7, PB (0,1,3,6,7)
T_{PCR}	Peripheral Data Valid after before Rising Edge of ϕ_o (Reading)	240		ns	
T_{IC}	External interrupt setup time	200		ns	

This is advance information and NCR reserves the right to change the specifications without notice.

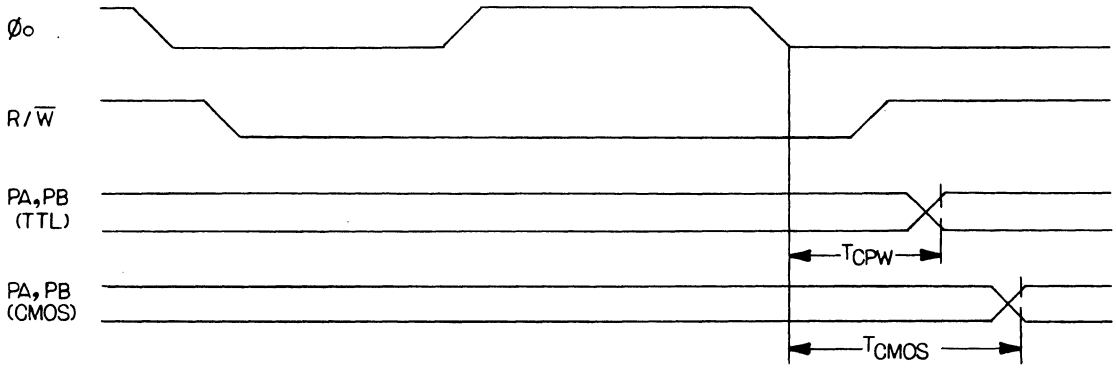
TIMING DIAGRAMS

Read Cycle Timing

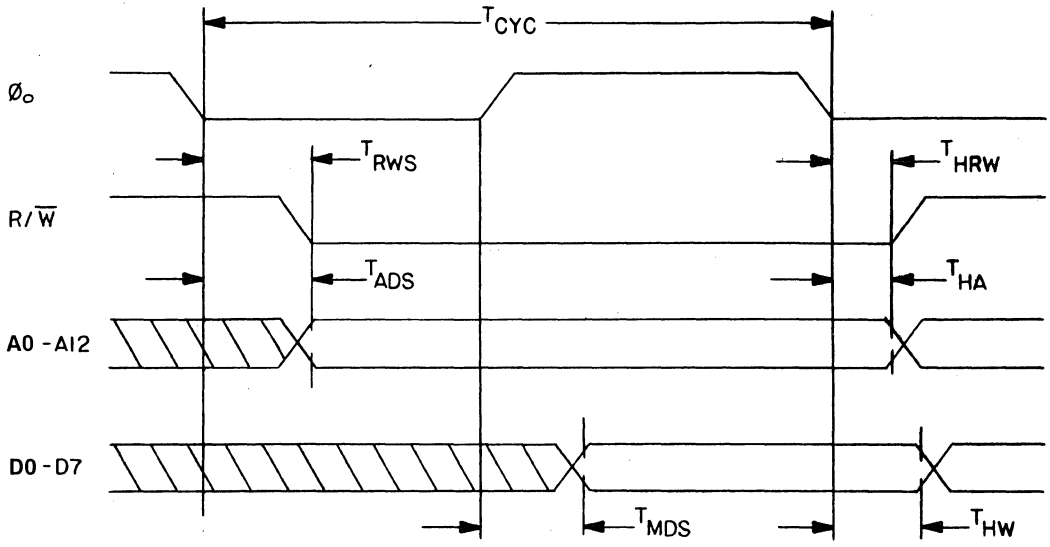


*DATA TRANSFERS FROM INTERNAL RAM, I/O LOGIC, TIMER OR INTERRUPT FLAG REGISTER ONLY.

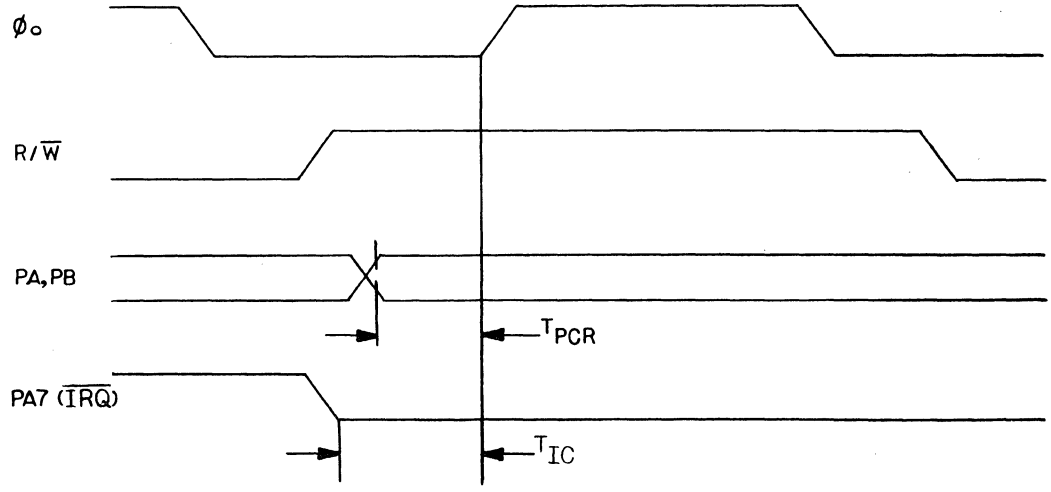
PA, PB Write Timing



Write Cycle Timing



PA, PB Read Timing



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Special Function Chips

PRODUCT SELECTION GUIDE

5385
SCSI PROTOCOL CONTROLLER

SCSI INTERFACE

*Supports ANSI X3T9.2 SCSI Standard

- Asynchronous data transfers to 1.5 MBPS
- Supports both Initiator and Target roles
- Parity generation w/optional checking
- Supports arbitration
- Controls all bus signals except Reset
- Doubly-buffered Data Register

MPU INTERFACE

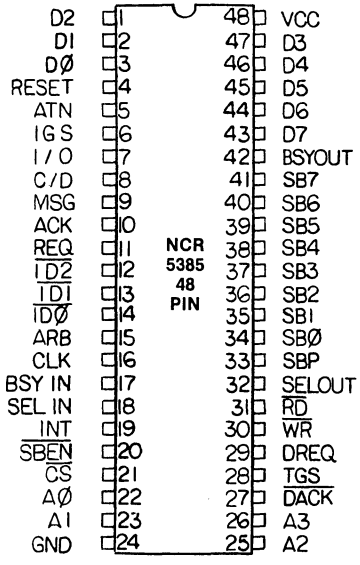
* Versatile MPU Bus Interface

- Memory or I/O mapped MPU interface
- DMA or programmed I/O transfers
- 24-bit Internal Transfer Counter
- Programmable (Re)Selection timeouts
- Interrupts MPU on all bus conditions requiring service

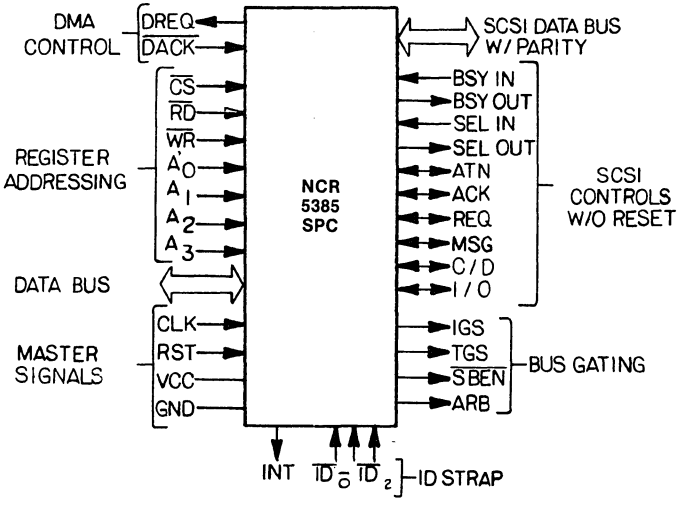
The NCR SCSI Protocol Controller (SPC) is designed to accomodate the Small Computer Systems Interface (SCSI) as defined by the ANSI X3T9.2 committee. The SPC operates in both the Initiator and Target roles and can therefore be used in host adapter and control unit designs. This device supports arbitration, including reselection, and is intended to be used in systems that require either open collector or differential pair transceivers.

The NCR 5385 SCSI Protocol Controller communicates with the system microprocessor as a peripheral device. The chip is controlled by reading and writing several internal registers which may be addressed as standard or memory mapped I/O. A 24-bit Transfer Counter and the appropriate handshake signals accommodate large DMA transfers with minimal processor intervention. Since the NCR 5385 interrupts the MPU when it detects a bus condition that requires servicing, the MPU is freed from polling or controlling any of the SCSI bus signals.

PIN CONFIGURATION



FUNCTIONAL PIN GROUPING



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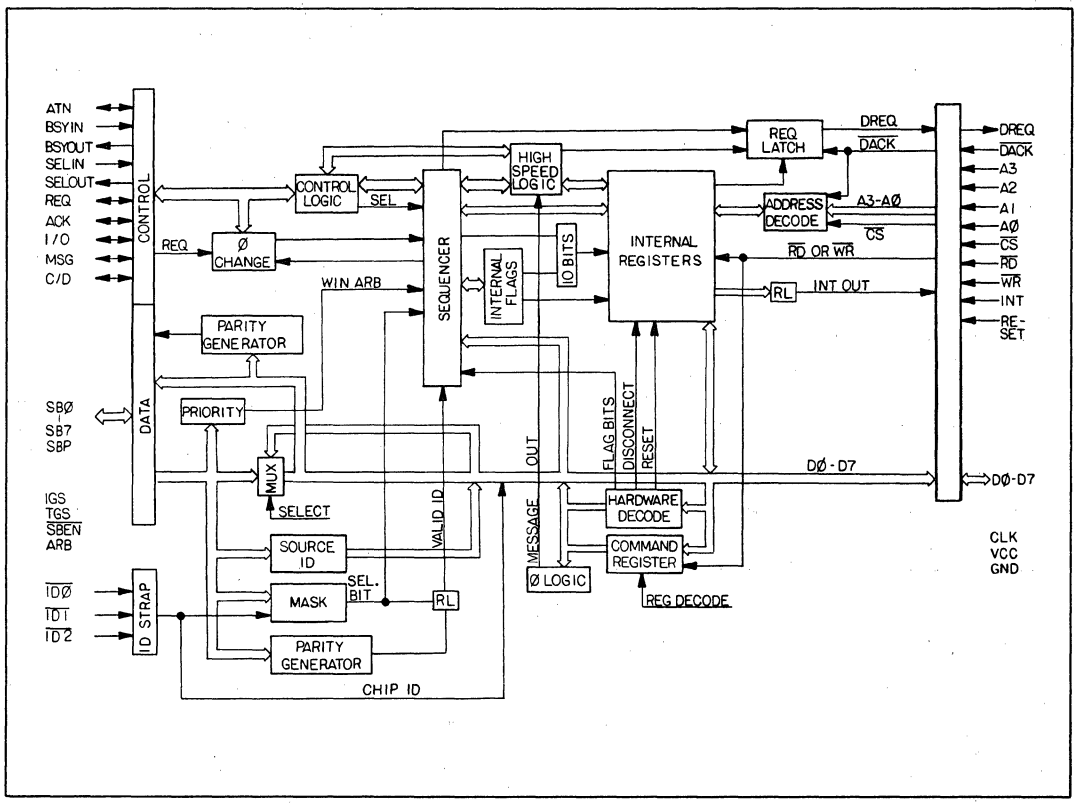
NCR

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

MICROPROCESSOR INTERFACE SIGNALS

CLK	16	Symmetrical square wave signal which generates internal chip timing. Maximum frequency is 10 MHz.
RESET	4	When high (1), this signal forces the chip into a reset state. All current operations are terminated. Internal storage elements are cleared and self-diagnostics are performed.
D0-D7	3-1 47-43	These signals comprise an active high data bus. It is intended that these signals be connected to the microprocessor data bus.
INT	19	This signal is used to interrupt the microprocessor for various bus conditions that require service. INT is set high for request and cleared when the chip is reset or the Interrupt Register is read.
$\overline{WR}$	30	Write pulse (active low) is used to strobe data from the data bus into an internal register which has been selected.
$\overline{RD}$	31	Read pulse (active low) is used to read data from an internal register that has been selected. The contents of the register is strobed onto the data bus.
$\overline{CS}$	21	When low (0), this signal enables reading from or writing to the internal register which has been selected.
A0-A3	22, 23, 25, 26	These signals are used in conjunction with $\overline{CS}$, to address all the internal registers.
DREQ	29	Data request. When high (1), this signal indicates that the internal Data Register has a byte to transfer (inputting from the SCSI bus) or needs a byte to transfer (outputting to the SCSI bus). This signal becomes active only if the DMA mode bit in the Command Register is on. It is cleared when $\overline{DACK}$ becomes active.
$\overline{DACK}$	27	Data acknowledge. When low (0), this signal resets DREQ and selects the Data Register for input or output. $\overline{DACK}$ acts as a chip select for the Data Register when in the DMA mode. $\overline{DACK}$ and $\overline{CS}$ must never be active at the same time.

SCSI INTERFACE SIGNALS

$\overline{ID0}$ -$\overline{ID2}$	14-12	These active low signals determine the three-bit code of the SCSI bus ID assigned to the chip. External pullup resistors are required only if tied to switches or straps.
SB0-SB7, SBP	34-41, 33	Active high data bus. These signals comprise the SCSI data bus and are intended to be connected to the external SCSI bus transceivers.
BSYIN	17	When high (1), this signal indicates to the chip that the SCSI BSY signal is active.
BSYOUT	42	When high (1), the chip is asserting the BSY signal to the SCSI bus.
SELIN	18	When high (1), this signal indicates to the chip that the SCSI SEL signal is active.
SELOUT	32	When high (1), the chip is asserting the SEL signal to the SCSI bus.
ATN	5	INITIATOR ROLE: The chip asserts this signal when the microprocessor requests the attention condition or a parity error has been detected in a byte received from the SCSI bus. TARGET ROLE: This signal is an input which indicates the state of the ATN signal on the SCSI bus.
ACK	10	INITIATOR ROLE: The chip asserts this signal in response to REQ for a byte transfer on the SCSI bus. TARGET ROLE: This signal is an input which, when active, indicates a response to the REQ signal.
REQ	11	INITIATOR ROLE: This signal is an input which, when active, indicates that the Target is requesting a byte transfer on the SCSI bus. TARGET ROLE: Asserted by the chip to request a byte transfer on the SCSI bus.
MSG, C/D, I/O	9, 8, 7	INITIATOR ROLE: These signals are inputs which indicate the current SCSI bus phase. TARGET ROLE: The chip drives these signals to indicate the current bus phase.
IGS	6	Initiator Group Select. When high (1), this signal indicates to the external SCSI drivers and receivers that the chip is operating in the Initiator role. Its purpose is to enable the external drivers for ATN and ACK and the external receivers for REQ, MSG, C/D, and I/O.
TGS	28	Target Group Select. When high (1), this signal indicates to the external SCSI drivers and receivers that the chip is operating in the Target role. Its purpose is to enable the external drivers for REQ, MSG, C/D, and I/O and the external receivers for ATN and ACK.
$\overline{SBEN}$	20	SCSI data Bus Enable. When low (0), this signal directly enables the external SCSI data bus drivers.
ARB	15	Arbitration phase. When high (1), this signal enables the external circuitry to place the ID bit on the SCSI bus for the Arbitration phase.

POWER SIGNALS

VCC	48	+5 V input
GND	24	Signal reference input

ELECTRICAL CHARACTERISTICS

OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}	4.75	5.25	VDC
Supply Current	I_{DD}		300	mA
Ambient Temp.	T_A	0	70	°C

INPUT SIGNAL REQUIREMENTS

PARAMETER	CONDITIONS	MIN	MAX	UNITS
High-level Input, V_{IH}		2.0	5.25	VDC
Low-level Input, V_{IL}		-0.3	0.8	VDC
High-level Input Current, I_{IH}	$V_{IH}=5.25V$		10	μA
Low-level Input Current, I_{IL}	$V_{IL}=0V$		-10	μA

OUTPUT SIGNAL REQUIREMENTS (Except $\overline{SBEN}$, IGS, and TGS)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
High-level Output Voltage, V_{OH}	$V_{DD}=4.75V$ @ $I_{OH}=-400\mu A$	2.4	—	VDC
Low-level Output Voltage, V_{OL}	$V_{DD}=4.75V$ @ $I_{OL}=2.0mA$	—	0.4	VDC

$\overline{SBEN}$, IGS, and TGS SIGNALS

PARAMETER	CONDITIONS	MIN	MAX	UNITS
High-level Output Voltage, V_{OH}	$V_{DD}=4.75V$ @ $I_{OH}=-400\mu A$	2.4	—	VDC
Low-level Output Voltage, V_{OL}	$V_{DD}=4.75V$ @ $I_{OL}=4.0mA$	—	0.4	VDC

INTERNAL REGISTERS

The NCR SCSI Protocol Controller has a set of internal registers which are used by the microprocessor to direct the operation of the SCSI bus. These registers are read (written) by activating $\overline{CS}$ with an address on A3-A0 and then issuing a $\overline{RD}$/($\overline{WR}$) pulse. They can be made to appear to a microprocessor as standard I/O ports or as memory-mapped I/O ports depending on the external circuitry that controls $\overline{CS}$. The following sections describe the operation of these internal registers.

REGISTER SUMMARY

A3	A2	A1	A0	R/W	REGISTER NAME
0	0	0	0	R/W	Data Register
0	0	0	1	R/W	Command Register
o	0	1	0	R/W	Control Register
0	0	1	1	R/W	Destination ID
0	1	0	0	R	Auxiliary Status
0	1	0	1	R	ID Register
0	1	1	0	R	Interrupt Register
0	1	1	1	R	Source ID
1	0	0	1	R	Diagnostic Status
1	1	0	0	R/W	Transfer Counter (MSB)
1	1	0	1	R/W	Transfer Counter (2nd BYTE)
1	1	1	0	R/W	Transfer Counter (LSB)
1	1	1	1	R/W	Reserved for Testability

DATA REGISTER

The Data Register is used to transfer SCSI commands, data, status and message bytes between the microprocessor data bus and the SCSI bus. This is an eight-bit register which is doubly-buffered in order to support maximum throughput. In the non-DMA mode, the microprocessor reads from (writes to) the Data Register by activating $\overline{CS}$ with A3-A0 = 0000 and issuing a $\overline{RD}$/($\overline{WR}$) pulse. A bit has been included in the Auxiliary Status Register to indicate when the Data Register is full. In the DMA mode, the DMA logic reads from (writes to) the Data Register by responding to DREQ with $\overline{DACK}$ and issuing a $\overline{RD}$/($\overline{WR}$) pulse. The SCSI bus reads from or writes to the Data Register when the chip is connected as an Initiator or Target and the bus is in one of the Information Transfer Phases.

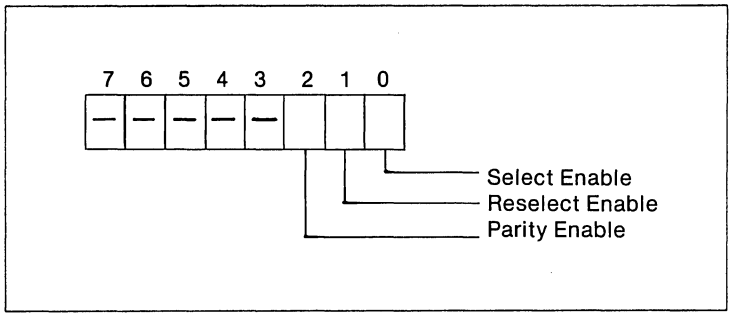
COMMAND REGISTER

The Command Register is an eight-bit register used to give commands to the SCSI chip. The microprocessor can write to (read from) the Command Register by activating $\overline{CS}$ with A3-A0 = 0001 and issuing a $\overline{WR}$/($\overline{RD}$) pulse. Writing to the Command Register causes the chip to execute the command that is written. The Command Register can be read; however, the chip resets the Command Register when it sets an Interrupt. Therefore, one cannot guarantee that the data in the register will be correct after loading an interrupting command or enabling selection or reselection. To be safe, a copy of the last command issued should be stored in the microprocessor's memory. Immediate commands are not stored.

The contents of the Command Register are described in a later section.

CONTROL REGISTER

This eight-bit read/write register is used for enabling certain modes of operation for the SCSI Protocol Controller. The microprocessor reads from (writes to) the Control Register by activating $\overline{CS}$ with A3-A0 = 0010 and issuing a $\overline{RD}$ ($\overline{WR}$) pulse.



BIT 7-3 Reserved

BIT 2 Parity Enable — When the parity enable bit is a "1", the chip generates and checks parity on all transfers on the SCSI bus. When the parity enable bit is a "0", the chip generates but does not check parity on bus transfers.

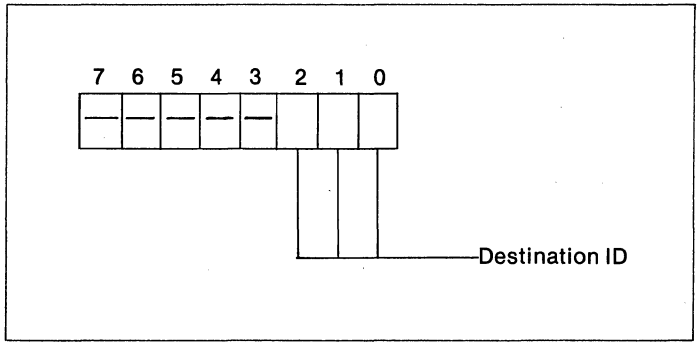
BIT 1 Reselect Enable — When this bit is a "1", the chip will respond to any attempt by a Target to reselect it. When the bit is a "0", the chip will ignore all attempts to reselect it.

BIT 0 Select Enable — When this bit is a "1", the chip will respond to attempt to select it as a Target. When it is a "0", the chip will ignore all selections.

NOTE: After being reset and completing self-diagnostics, the control register will contain all zeros.

DESTINATION ID REGISTER

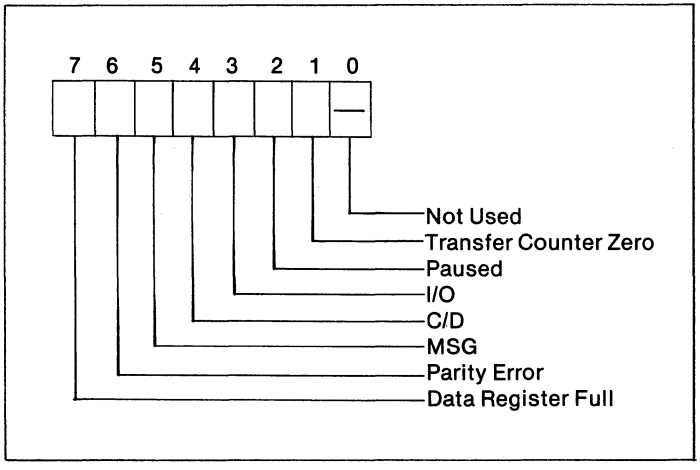
The Destination ID Register is an eight-bit register that is used to program the SCSI bus address of the destination device prior to issuing a Select or Reselect command to the chip. Bits 0-2 specify the address and bits 3-7 are always zeroes. The ID register is written (read) by activating $\overline{CS}$ with A3-A0 equal to "0011" and then pulsing $\overline{WR}$ ($\overline{RD}$).



AUXILIARY STATUS REGISTER

The Auxiliary Status Register is an eight-bit read-only register. It contains bits which indicate the status of the chip's operational condition. Some of these bits are used to determine the reason for interrupts. Therefore, the Auxiliary Status Register should always be read prior to reading the Interrupt Register when servicing interrupts. After the Interrupt Register is read, the Auxiliary Status Register bits needed to service the interrupt may change.

The Auxiliary Status Register is read by activating $\overline{CS}$ with A3-A0 = 0100 and then pulsing $\overline{RD}$. The individual bits of the Auxiliary Status Register are defined below.



BIT 7 Data Register Full

This bit indicates the status of the Data Register and must be monitored by the microprocessor during non-DMA mode commands that use the Data Register. When the DMA mode bit in the Command Register is off (0) and the command being executed is one of Send, Receive or Transfer Info commands (refer to Section 5.0 page 19, COMMANDS), data is transferred to (from) the chip by writing (reading) the Data Register. Data Register Full is set on (1) when data is written and turned off (0) when data is read. Therefore, Data Register Full should be on before taking data from the chip, and off when sending data to the chip.

The Data Register Full bit is always reset (to 0) at the time an interrupting type command is loaded into the Command Register. Therefore, when issuing such commands, the Command Register should be loaded prior to loading the Data Register and monitoring the Data Register Full flag.

BIT 6 Parity Error

When this bit is one, it indicates that the chip has detected a parity error on a byte of data received across the SCSI bus. It can be set when the chip is executing one of the Receive commands or the Transfer Info command (when the transfer is an input). This bit is reset after the Interrupt Register is read.

BIT 3-5 I/O, C/D, MSG

These bits indicate the status of the SCSI I/O, C/D, and MSG signals at all times. They define the Information Phase type being requested by the Target. These signals are significant when servicing interrupts and the chip is logically connected to the bus in the Initiator role. An interrupt will occur with any phase change. This allows the Initiator to prepare for the next phase of data transfer. These bits are only held while INT is active. The bits are coded as follows:

I/O	C/D	MSG	BUS PHASE
0	0	0	Data Out
0	0	1	Unspecified Info Out
0	1	0	Command
0	1	1	Message Out
1	0	0	Data In
1	0	1	Unspecified Info In
1	1	0	Status
1	1	1	Message In

BIT 2 Paused

When on (1), this bit indicates that the chip has aborted the command being executed in response to the Pause command. It is turned off when the interrupting type command code is loaded into the Command Register.

BIT 1 Transfer Counter Zero

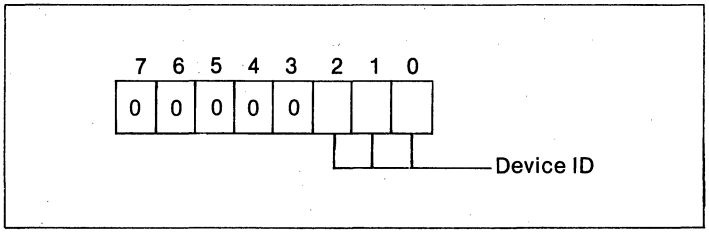
This bit is provided to indicate the status of the 24-bit Transfer Counter. When on (1), it indicates that the Transfer Counter is equal to zero. It is intended to facilitate interrupt servicing.

BIT 0 Not Used

NOTE: The Auxiliary Status Register will contain the following pattern after a Reset and self-diagnostics: 00xxx010.

ID REGISTER

The ID Register is an eight-bit read-only register that indicates the logical SCSI bus address occupied by the chip. Bit 0-2 directly reflect the logical inversion of the chip ID input signals $\overline{ID0}$-$\overline{ID2}$. The ID Register is active high whereas the ID input signals are active low. The ID Register allows the microprocessor to read the chip's SCSI bus address which would normally be strapped in hardware. Bits 3-7 of the ID Register will always be zeroes. The ID Register is read by activating $\overline{CS}$ with A3-A0 = 0101 and then pulsing $\overline{RD}$.

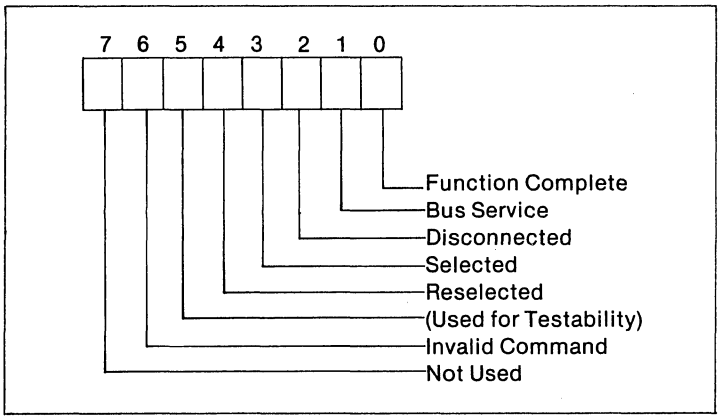


INTERRUPT REGISTER

The Interrupt Register is an eight-bit read-only register. It is used in conjunction with the Auxiliary Status Register to determine the reason for an interrupt condition. This register is read by activating $\overline{CS}$ with A3-A0 = 0110 and then pulsing $\overline{RD}$. When the Interrupt Register is read, it automatically resets itself (after the read is complete) and enables the chip for a new interrupt condition. Since the Parity Error bit in the Auxiliary Status Register is reset after a read of the Interrupt Register, and since I/O, C/D, and MSG are only held while INT is active, the Auxiliary Status Register should always be read prior to reading the Interrupt Register.

If a Selected or Reselected interrupt occurs after issuing a command that would normally cause an interrupt, the chip will ignore the last command issued. This allows the microprocessor to service the Selected or Reselected interrupt prior to proceeding with the other operation. An example of this situation is when the microprocessor issues a command to select a Target at about the same time another Target reselects the chip. If the chip sees the reselection first, the microprocessor will receive an interrupt for the reselection, and the chip will ignore the Select command, which would now be invalid since the chip is now logically connected on the SCSI bus to another device.

Individual interrupt conditions are described below. (Note: that for all cases, an interrupt condition is on, when the corresponding bit is a one (1), and off when zero (0).)



BIT 7	Not Used	May be either (1) or (0).
BIT 6	Invalid Command	When on (1), this bit indicates that the last command loaded into the Command Register is not valid.
BIT 5	Not Used	(Reserved for testability)
BIT 4	Reselected *	This interrupt will be on (1) when the chip has been reselected by another SCSI device. After setting this interrupt, the chip is logically connected to the bus in an Initiator role and is waiting for the Target to send REQ or disconnect from the bus.
BIT 3	Selected *	This interrupt will be on (1) whenever the chip has been selected by another SCSI device. After setting this interrupt, the chip is logically connected to the bus in the Target role and is waiting for a command to be loaded into the Command Register.

* The chip will become selected (reselected) only if the ID data byte put on the SCSI bus during the Selection (Reselection) Phase has good parity and not more than one ID other than the chip's own ID is on.

BIT 2 Disconnected

This interrupt will be set on (1) when the chip is connected to the bus in the Initiator role and the Target disconnects or when the chip is executing a Select or Reselect command and the destination device does not respond before the Transfer Counter times out.

BIT 1 Bus Service

When the chip is logically connected to the bus in the Initiator role, this bit will be set on (1) whenever the Target sends a REQ which the chip cannot automatically handle. This happens when the first REQ for connection is received or when the chip is executing a Transfer Info or Transfer Pad command and either the Transfer Counter is zero or the Target changes the Information Phase type.

A Bus Service interrupt may also be set if a phase change occurs before REQ is seen. This early notification will allow the Initiator extra time to prepare for a phase change in some unbuffered systems. (Note: that the chip may generate Bus Service Interrupts for phases that never request transfers. This is not an error condition, merely transitional status of I/O, C/D, and MSG.)

If the chip is logically connected in the Target role, this bit will be set on (1) whenever the Initiator asserts ATN. When indicating ATN the Bus Service interrupt may occur by itself, with a Selected interrupt, or with a Function Complete interrupt.

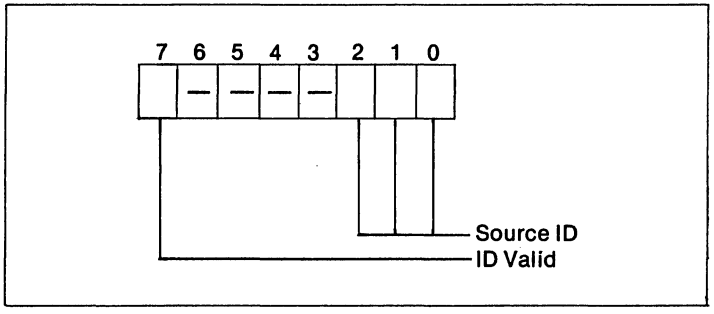
BIT 0 Function Complete

When this bit is on (1), it indicates that the last interrupting command has completed. It is the normal successful completion interrupt for Select, Reselect, Send and Receive commands (Refer to COMMANDS). During any of the Receive commands, it is set on (1) along with the parity error bit as soon as a parity error is detected. A Bus Service Interrupt may also occur simultaneously with the Function Complete if an ATN signal was activated during a Send or a Receive command.

The Function Complete interrupt is also generated at the end of a Message In phase for a Transfer Info command. (See TRANSFER INFO command.)

SOURCE ID REGISTER

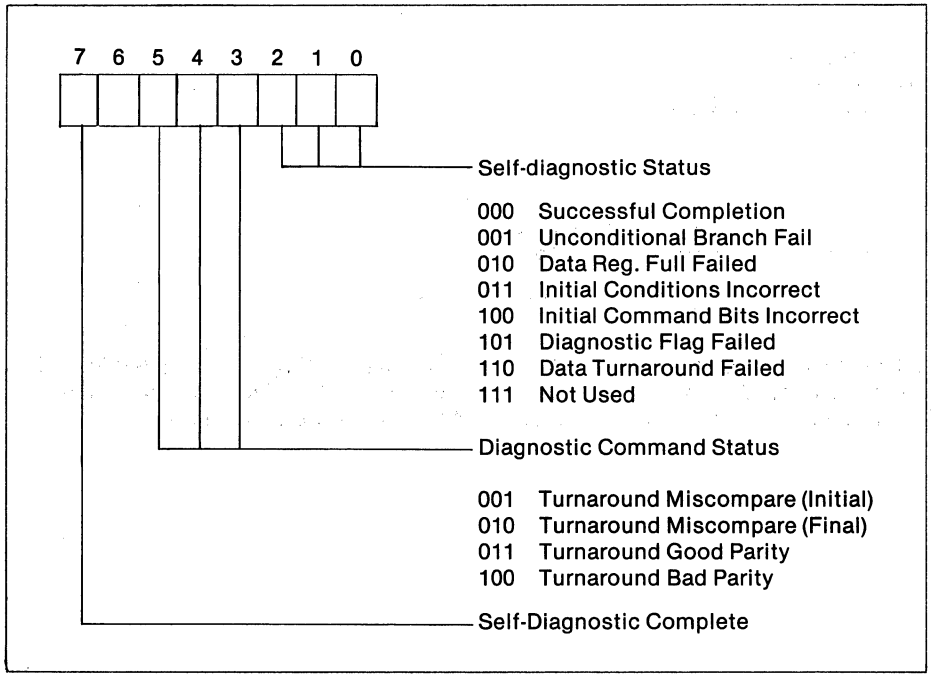
The Source ID Register is an eight-bit read-only register which contains the three-bit encoded ID of the last device which Selected or Reselected the chip. The following is the format of the Source ID Register.



The ID Valid bit indicates that the source device placed its own ID bit on the SCSI bus during the Selection Phase. The SPC chip has encoded the source ID and placed it in bits 2-0. This information remains valid until the chip disconnects from the SCSI bus, at this time the ID Valid bit is reset.

DIAGNOSTIC STATUS REGISTER

The Diagnostic Status Register is an eight-bit read-only register which indicates the result of self-diagnostics and the last diagnostic command issued to the chip. The format of the Diagnostic Status Register is shown below.



Bit 7 = 1 indicates that self-diagnostics have been completed. (NOTE: A reset will clear bits 6-3 if possible). After a reset to the chip, the microprocessor should make sure that the Diagnostic Status Register contains the following pattern before attempting any commands: 10000000. This code indicates self-diagnostics are complete and no errors were detected. After a diagnostic command has been executed, bits 6-3 will contain the resulting status, but bit 7 and bits 2-0 are not affected.

The microprocessor may read the Diagnostic Status Register by activating $\overline{CS}$ with A3-A0 = 1001 and issuing a $\overline{RD}$ pulse.

If an error is detected during self-diagnostics, the proper status is loaded into the Diagnostic Status Register and the chip halts until a Reset command or a Reset signal is asserted. Refer to the Self-Diagnostic Status Code Summary for an explanation of the individual codes.

When a diagnostic command is issued to the chip, the chip will attempt to perform the function, load a status into bits 6-3, and initiate a Function Complete Interrupt.

SELF-DIAGNOSTIC STATUS CODE SUMMARY

000 - Successful Completion. The chip executed all self-diagnostics following a reset and detected no errors.

001 - Unconditional Branch Failed. The chip's internal sequencer attempted an unconditional branch and failed to reach the desired location.

010 - Data Register Full Failed. The chip attempted to set and reset the Data Register Full status bit in the Interrupt Register and failed.

011 - Initial Conditions Incorrect. The chip detected one of its internal initial conditions in the wrong state.

100 - Initial Command Bits Incorrect. The chip tested bits 6,4,2,1 and 0 of the Command Register and found at least one was not zero.

101 - Diagnostic Flag Failed. The chip failed in its attempt to set and reset its internal diagnostic flag.

110 - Data Turnaround Failed. During self-diagnostics the chip attempts to flush several bytes of data through its internal data paths. It also attempts to set and reset the Parity Error bit in the Interrupt Status Register. This status indicates that one of these operations failed.

TRANSFER COUNTER (THREE EIGHT-BIT COUNTERS)

The Transfer Counter is comprised of three, eight-bit register/counters. It is used by the chip for Send, Receive and Transfer commands that require more than a single byte of data to be transferred. It may also be used with Select and Reselect commands to set a timeout for no response. To write to (read from) the Transfer Counter, $\overline{CS}$ is activated with A3-A0 selecting a byte and then pulsing $\overline{WR}$ ($\overline{RD}$). The Transfer Counter is addressed as shown below.

A3	A2	A1	A0	SELECTED BYTE
1	1	0	0	Most Significant Byte
1	1	0	1	Middle Byte
1	1	1	0	Least Significant Byte

For Send, Receive and Transfer commands with single-byte not specified, the Transfer Counter specifies to the chip the maximum number of bytes to be sent or received before interrupting. The Transfer Counter must be loaded prior to issuing the command. When single-byte is specified, the chip neither uses nor alters the Transfer Counter. To facilitate servicing interrupts for commands that use the Transfer Counter, a bit is provided in the Auxiliary Status Register to indicate when the Transfer Counter is zero.

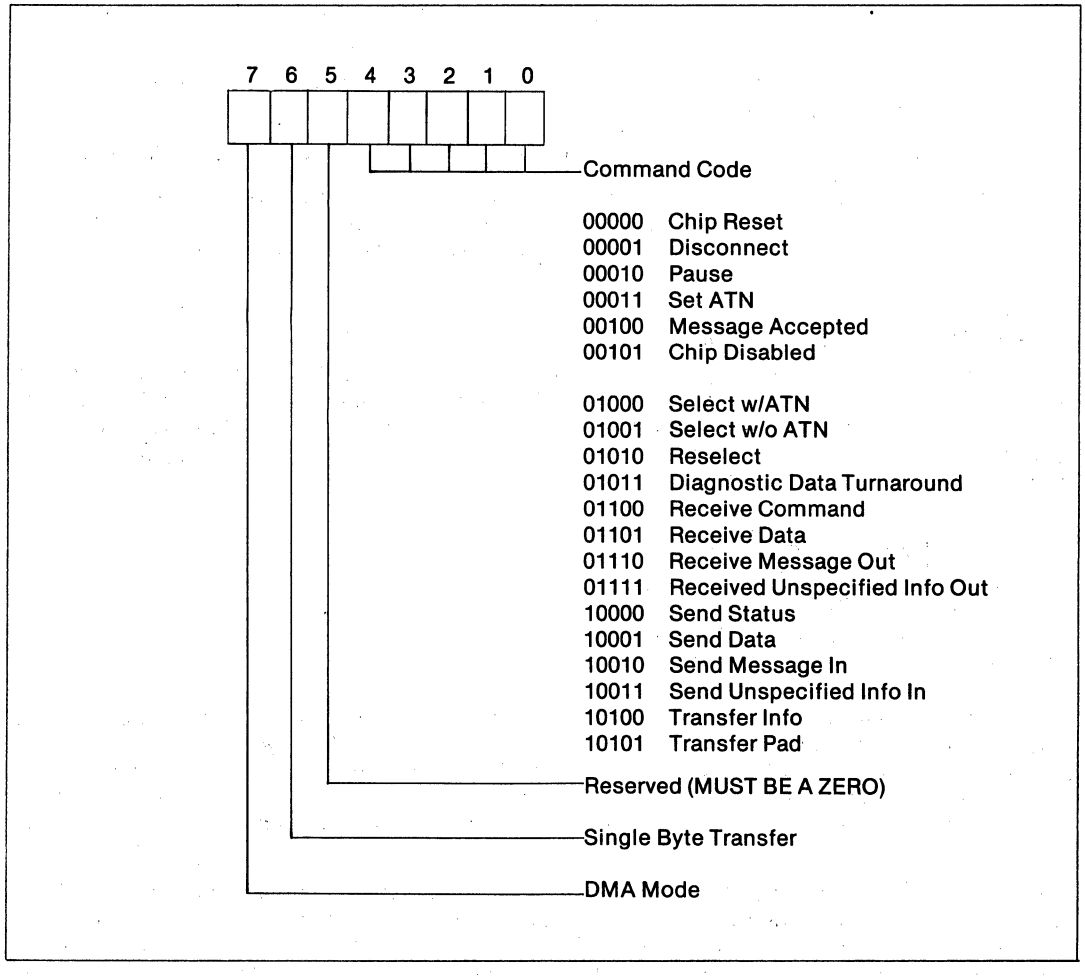
For Select and Reselect commands, the Transfer Counter specifies the number of time intervals (1024 CLK periods) that the chip will wait before automatically aborting the command due to no response (BSY) from the destination device. The Transfer Counter must be loaded prior to issuing the command. If the Transfer Counter is loaded with all zeroes, the timeout logic in the chip will be disabled, and the chip will not automatically abort the command due to no response.

COMMANDS

This section defines command format, types, codes and operation. Commands are given to the chip by loading the Command Register.

COMMAND FORMAT

The bits in the Command Register are defined as follows.



BIT 7	DMA Mode	This bit is applicable only for commands that use the Data Register. When this bit is on (1), it indicates that data will be transferred to (from) the Data Register using the DMA signals DREQ and $\overline{\text{DACK}}$. When it is off (0), the microprocessor must monitor the state of the Data Register Full flag in the Auxiliary Status Register. Data is then transferred by using the appropriate input/output command.
BIT 6	Single Byte Transfer	When on (1), this bit indicates that only one byte of data is to be transferred for this command. The Transfer Counter will not be used or altered by the chip. Therefore, for common single byte message and status transfers, the Transfer Counter does not need to be loaded prior to issuing a command with this bit set. When this bit is off (0). the Transfer Counter is used by the chip to determine the length of the transfer for the command.
BIT 5	Reserved	This bit is not used and should always be programmed off (0).
BIT 4-0	Command Code	These bits are used to specify the command to be executed.

COMMAND TYPES

There are two types of commands; Immediate and Interrupting. All of the Immediate commands, except for pause, cause immediate results within three clock cycles from the time the Command Register is loaded. The Pause command is explained in a later section. Interrupting commands do not result in immediate action. Their completion is always flagged by an interrupt.

Command codes 00000-00111 specify Immediate commands. Immediate commands that are listed as reserved, will be ignored if issued to the SPC chip. Command codes 01000-10101 specify Interrupting commands. When one of these codes is loaded into the Command Register, a second Interrupting command code should not be loaded until after the interrupt has occurred for the first command. However, an Immediate type command may be loaded before the interrupt for an Interrupting command occurs. If a reserved Interrupting command code is issued, the chip will respond with an Invalid Command interrupt.

INVALID COMMANDS

The user of the chip can be in one of three states at any particular time: Disconnected, connected as an Initiator, or connected as a Target. Commands are valid only in specified states. If an invalid Immediate command is issued, the chip will ignore the command. If an Interrupting command is issued in an invalid state, or a reserved Interrupting command code is issued, an Invalid Command interrupt will result. The exceptions are described below:

The microprocessor must never issue any interrupting type command when the chip is not expecting such a command. Unpredictable results will occur in this case. The following is a list of user states in which the chip is not expecting an interrupting command:

1. The chip is currently processing an Interrupting type command and has not yet set the interrupt to signal the completion.
2. The chip is currently processing an Interrupting type command, a Pause command has been issued but the Paused bit in the Auxiliary Status Register has not been set.
3. The chip is connected as an Initiator, but the Target has not yet requested an Information Transfer.
4. The chip has completed a Transfer Info or Transfer Pad command and the Target has not requested additional information or has not changed the Information Phase.

In user states three and four, described above, the microprocessor must wait for a Bus Service, Disconnected, or Function Complete interrupt.

If an interrupting command is illegitimately issued in these states, no interrupt will occur for it, and it is likely that the current function will be altered.

COMMAND SUMMARY

Below is a summary that lists all commands. In the table the following abbreviations are used.

INT = INTERRUPTING D = DISCONNECTED I = CONNECTED AS AN INITIATOR
IMM = IMMEDIATE T = CONNECTED AS A TARGET

COMMAND CODE	COMMAND	TYPE	VALID STATES
00000	Chip Reset	IMM	D,I,T
00001	Disconnect	IMM	I,T
00010	Paused	IMM	D,T
00011	Set ATN	IMM	I
00100	Message Accepted	IMM	I
00101	Chip Disable	IMM	D,I,T
00110-00111	Reserved	IMM	
01000	Select w/ATN	INT	D
01001	Select w/o ATN	INT	D
01010	Reselect	INT	D
01011	Diagnostic	INT	D
01100	Receive Command	INT	T
01101	Receive Data	INT	T
01110	Receive Message Out	INT	T
01111	Receive Unspecified Info Out	INT	T
10000	Send Status	INT	T
10001	Send Data	INT	T
10010	Send Message Out	INT	T
10011	Send Unspecified Info In	INT	T
10100	Transfer Info	INT	I
10101	Transfer Pad	INT	I
10110-11111	Reserved	INT	

COMMAND DEFINITIONS

CHIP RESET

Chip Reset immediately stops any chip operation and resets all registers, counters, etc. on the chip. It performs the same operation as the hardware "reset" input.

DISCONNECT

Upon receipt of this command, the chip immediately releases all SCSI bus signals and returns to a Disconnected idle state. For the Target role, this is the normal method of disconnecting from the bus when a transfer is complete. For the Initiator role, Disconnect may be used to release the bus signals as a result of a timeout condition. In this case, the chip ignores the Target and is left in the Disconnected state. For the Disconnected state, it is not valid to issue a Disconnect command. If issued, the chip will ignore this command.

PAUSE

Pause is an Immediate command that is valid in the Disconnected state or when logically connected to the bus as a Target device. Pause is not valid when connected as an Initiator.

When connected as a Target, the Pause command provides a means of halting a Send or Receive command without having to wait for the transfer to complete. When Pause is issued, it immediately sets a flag in the chip. Within one byte transfer cycle, the chip recognizes the flag, aborts the Send or Receive operation, and then sets the Paused status bit in the Auxiliary Status Register. At this time, the chip is still connected to the bus in the Target role, and it is waiting for another command.

The Pause command stops the Send or Receive command in an orderly manner leaving the Transfer Counter in a valid state that indicates the remaining number of bytes to be transferred. Also no REQ or ACK is asserted on the bus and no data is left in the chip waiting to be transferred. An operation that is paused may be resumed, if desired, simply by reloading the original command into the Command Register. (Note: after issuing the Pause while executing Send or Receive, it is necessary to continue transferring data with the chip (due to double-buffering) until the Paused status bit is set or an interrupt occurs.)

When in the disconnected state, Pause may be issued to abort a Select or Reselect command. After a Select or Reselect command is issued and before an interrupt occurs, a Pause command may be issued to abort the operation. The Pause command immediately sets an internal flag. If the chip has not yet won arbitration, it sets the Paused bit in the Auxiliary Status Register and waits in the disconnected state for another command. If the chip has won arbitration, it releases the bus by dropping the two ID bits with SELOUT on for a minimum of 100 μs, checks for no BSYIN, and then releases the bus. After this procedure, it sets the Paused bit in the Auxiliary Status Register and waits for another command in the Disconnected state.

Since Pause is an Immediate command, it does not cause an interrupt. As previously noted, the chip sets the Paused status bit to indicate that is has been executed. If an interrupt-causing event occurs before the chip sees the pause flag set, the chip will set the interrupt. In this case, the Paused status bit is not set by the chip either before or after the interrupt. In all cases, an interrupt-causing event will take precedence over Pause. For example, in the Target role if ATN is on when Pause is issued, a Bus Service interrupt will occur and the Paused status bit will not be set.

If the Pause command is issued when the chip is Disconnected, the Paused status bit will be set by the chip, provided it has not already detected a Selection or Reselection.

SET ATN

The Set ATN command causes ATN to be asserted immediately if the chip is connected as an Initiator. This command is invalid and ignored if issued when the chip is Disconnected or is operating in a Target role. The ATN signal is de-asserted in a Message Out phase when the transfer count becomes zero or one byte has been transferred (in a one-byte transfer command) during the execution of a Transfer Info command.

The chip automatically sets ATN in two cases:

1. If a Select w/ATN command is issued and arbitration is won.
2. If a parity error is detected on an input byte during execution of a Transfer Info command.

MESSAGE ACCEPTED

The Message Accepted command is an Immediate command that is valid only when connected as an Initiator. It is used after a Transfer Info or Pad command (See TRANSFER INFO and TRANSFER PAD) to indicate to the chip that ACK can be de-asserted for the last byte.

When an Initiator receives a message, a Transfer command is used. If the transfer is an input (I/O = 1) and the information is a message (MSG = 1, C/D = 1), the chip interrupts after receiving the last byte with a Function Complete interrupt. For this one special case, the chip also leaves ACK asserted on the bus. By interrupting and leaving ACK asserted, the chip gives the microprocessor a chance to interpret the message and set ATN, prior to ACK being de-asserted. This allows the chip to properly request a Message Out phase if the Initiator wants to send a "Reject Message" to the Target.

Message Accepted must always be issued after a Transfer Info for a Message In phase, whether or not Set ATN is issued, in order to have the chip de-assert ACK. If the Initiator wants to reject the message, Set ATN would be issued first followed by Message Accepted. If the message is not to be rejected, only Message Accepted is issued. (Note: until Message Accepted is issued, the Target will not send another REQ since ACK is still asserted.)

CHIP DISABLE

Chip Disable immediately stops all chip operations and logically disconnects it from the circuit. All outputs will be placed in a high impedance state and the chip will not respond to any commands (other than chip reset). The chip will also not respond to any activity on the SCSI bus. The only way to exit this condition is to activate the "reset" input or issue a Reset command.

SELECT w/ATN

This command causes the chip to attempt to select a Target. It may only be used if the microprocessor is in the Disconnected state. Any attempt to issue this command in another state will result in an Invalid Command interrupt. Before issuing this command, the microprocessor must load the Transfer Counter for a timeout on the Target's response. This value is computed according to the following formula:

$$\text{Transfer Counter} = \text{Desired Timeout} / (1024 \times \text{Clock Period})$$

If the Transfer Counter is loaded with the value zero, the chip will wait indefinitely for a response from the Target being selected.

The microprocessor must also load the Destination ID Register with the three-bit code of the Target to be selected before issuing the Select w/ATN command.

When the chip detects the Select w/ATN command, it begins by attempting to arbitrate for control of the SCSI bus. If, at any time during arbitration the chip becomes selected or reselected, the Select w/ATN is aborted and forgotten and the chip will interrupt with one of the following conditions:

1. Selected
2. Selected and Bus Service
3. Reselected

If arbitration is won, the chip places the SCSI bus in the Selection phase with ATN asserted, and uses the Destination ID Register to identify the desired Target. At the same time, the chip begins a timer based on the value computed above. If the Target does not respond within the timeout period, the chip will disconnect from the bus and interrupt with the Disconnected flag set in the Interrupt Register. (Note: The microprocessor should never monitor the Transfer Counter Zero flag in the Auxiliary Status Register to determine when a timeout has occurred.) If the Target responds within the allotted time, the chip will interrupt with a Function Complete status. Control of the SCSI bus then belongs to the selected Target and after the interrupt status has been read, another interrupt may occur indicating either that the Target has disconnected or is requesting a transfer.

If the timeout is disabled and the Target does not respond, or if arbitration is not won, the only way to abort the Select w/ATN command is to issue the Pause command. After the Pause command is issued, it is still possible that the Function Complete or Disconnect interrupts may occur. This happens if one of the interrupts get set before the chip detects the Pause command, or if the Target responds while the chip is sequencing off the SCSI bus in a timeout condition. If the chip does not set either interrupt, it will set the Paused bit in the Auxiliary Status Register. If the microprocessor detects this bit after issuing the Pause command, then it is assured that the chip aborted the Select w/ATN command and no connection exists.

SELECT w/0 ATN

The Select w/o ATN is identical to the Select w/ATN command except that the ATN signal is not asserted during the Selection phase.

RESELECT

This command causes the chip to attempt to reselect an Initiator. It may only be used if the microprocessor is in the Disconnected state. Any attempt to issue this command in another state will result in an Invalid Command interrupt. Before issuing this command, the microprocessor must load the Transfer Counter for a timeout on the Initiator's response. This value is computed according to the following formula:

$$\text{Transfer Counter} = \text{Desired Timeout} / (1024 \times \text{Clock Period})$$

If the Transfer Counter is loaded with the value zero, the chip will wait indefinitely for a response from the Initiator being reselected.

The microprocessor must also load the Destination ID Register with the three-bit code of the Initiator to be reselected before issuing the Reselect command.

When the chip detects the Reselect command, it begins by attempting to arbitrate for control of the SCSI bus. If, at any time during arbitration, the chip becomes selected or reselected, the Reselect is aborted and forgotten and the chip will interrupt with one of the following conditions:

1. Selected
2. Selected and Bus Service
3. Reselected

If arbitration is won, the chip places the SCSI bus in the Reselection phase using the Destination ID Register to identify the desired Initiator. At the same time, the chip begins a timer based on the value computed above. If the Initiator does not respond within the timeout period, the chip will disconnect from the bus and interrupt with the Disconnected flag set in the Interrupt Register. (Note: The microprocessor should never monitor the Transfer Counter Zero flag in the Auxiliary Status Register to determine when a timeout has occurred.) If the Initiator responds within the allotted time, the chip will interrupt with a Function Complete status. The chip (acting as the Target) is then in control of the SCSI bus, and waits for the Interrupt Register to be read by the microprocessor. After it has been read, the chip waits for a command from the microprocessor or ATN from the Initiator. If the ATN occurs, the chip will set the Bus Service interrupt. This interrupt may happen immediately after a command has been issued due to internal timing. In this case, the chip waits for the Interrupt Register to be read and the command is ignored. The chip then waits for a new command.

If the timeout is disabled and the Initiator does not respond, or if arbitration is not won, the only way to abort the Reselect command is to issue the Pause command. After the Pause command is issued, it is still possible that the Function Complete or Disconnected interrupts may occur. This happens if one of the interrupts get set before the chip detects the Pause command, or if the Initiator responds while the chip is sequencing off the SCSI bus in a timeout condition. If the chip does not set either interrupt, it will set the Paused bit in the Auxiliary Status Register. If the microprocessor detects this bit after issuing the Pause command, then it is assured that the chip aborted the Reselect command and no connection exists.

DIAGNOSTIC (DATA TURNAROUND)

This Interrupting command causes the chip to attempt to turn a data byte around through its internal data paths. When the command is loaded into the Command Register the Data Register Full bit is reset. The microprocessor then writes one byte into the Data Register. The chip moves the byte to another register and compares the contents of the Data Register. The byte is then moved to a third register (the SCSI output register) and good parity is generated if bit 6 of the command is off (0); bad parity is generated if bit 6 is on (1). Finally, the chip moves the byte back to the Data Register and compares it with the contents of the second register. Based on these comparisons and parity checking, the chip stores a result into the Diagnostic Status Register and sets the Function Complete interrupt. After reading the Interrupt Register, the microprocessor should make sure the Data Register Full bit is on (1) and read the contents of the Data Register. If the Data Register Full bit is not on (0), then an error has occurred. The following is a list of codes which are loaded into bits 6-3 of the Diagnostic Status Register as a result of this command.

BIT 6543	RESULT
0001	Data Miscompare (INITIAL)
0010	Data Miscompare (FINAL)
0011	Good Parity Detected
0100	Bad Parity Detected

RECEIVE COMMANDS

The Receive commands are Interrupting commands that are valid only when connected as a Target device. They are used by the Target to receive commands, data, and message information from an Initiator.

The Receive commands transfer data; therefore, the Single Byte Transfer and DMA mode bits in the Command Register are valid for these commands. If the Single Byte Transfer bit is off (0), the Transfer Counter must be loaded before a Receive command is issued to the chip. In this case, the chip uses the Transfer Counter to determine the number of bytes to receive.

When a Receive command is issued, the chip immediately resets the Data Register Full bit in the Auxiliary Status Register. The chip then drives the I/O, C/D, and MSG outputs for the proper information phase as follows.

COMMAND NAME	I/O	C/D	MSG
Receive Command	0	1	0
Receive Data	0	0	0
Receive Message Out	0	1	1
Receive Unspecified Info Out	0	0	1

The chip then proceeds to request and receive the specified number of information bytes. The DMA mode bit in the Command Register determines how the chip transfers these bytes from its Data Register to the microprocessor.

When a Receive command is terminated, the chip generates an interrupt. The following two events can cause termination:

1. The operation completes succesfully; the Transfer Counter is zero. This event results in a Function Complete interrupt with the Parity Error bit in the Auxiliary Status Register off (0). If the Initiator activated ATN during the operation, the Bus Service interrupt will also be on.

2. A Parity Error occurs. The last byte transferred is the byte that caused the error. This event causes a Function Complete interrupt with the Parity Error bit in the Auxiliary Status Register on (1). If the Initiator activated ATN during the operation, the Bus Service interrupt will also be on.

After any of the interrupts, the chip is always left in the connected Target state. The Transfer Counter indicates the number of bytes remaining to be transferred (zero if completed successfully, and the Data Register is empty (the last byte received is sent to the microprocessor). Also, ACK and REQ are inactive on the bus.

(Note: if a Bus Service interrupt alone occurs after issuing a Send command, the Initiator activated ATN before the chip began executing the command. In this case, the command is ignored by the chip.)

A Receive command may be stopped prior to an interrupt causing event by issuing a Pause command. Operation of the Pause command is explained in an earlier section. In the event the Initiator does not respond, or stops responding, the chip is left in a state where it cannot respond to a Pause command. For this case, a Disconnect command can be used to abort the command and the connection. The Disconnect command is explained in an earlier section.

SEND COMMANDS

The Send commands are Interrupting commands that are valid only when connected to the bus in the Target role. They are used by a Target to send status, data, and message information to an Initiator.

The Send commands transfer data, and therefore, the Single Byte Transfer and DMA mode bits in the Command Register are valid for these commands. If the Single Byte Transfer bit is off (0), the Transfer Counter must be loaded before a Send command is issued to the chip. In this case, the chip uses the Transfer Counter to determine the number of bytes to send.

When a Send command is issued, the chip immediately resets the Data Register Full bit in the Auxiliary Status Register. Therefore, the first byte of data for the transfer cannot be put into the Data Register until after a Send command is loaded into the Command Register.

In executing a Send command, the chip drives the I/O, C/D, and MSG outputs for the proper information phase. These lines are logically driven for each Send command as shown below.

COMMAND NAME	I/O	C/D	MSG
Send Status	1	1	0
Send Data	1	0	0
Send Message In	1	1	1
Send Unspecified Info In	1	0	1

After resetting Data Register Full and driving I/O, C/D, and MSG, the chip then proceeds to monitor Data Register Full, take the data from the Data Register, and send it to the Initiator. The DMA mode bit in the Command Register specifies how the data is loaded into the chip.

After interrupting, the chip is left in the connected Target state, and ACK and REQ are inactive on the bus. When the transfer is complete, the chip interrupts with a Function Complete Interrupt. If the Initiator activated ATN during the transfer, a Bus Service interrupt will also be set by the chip.

(Note: if a Bus Service interrupt alone occurs after issuing a Send command, the Initiator activated ATN before the chip began executing the command. In this case, the command is ignored by the chip.)

A Send command may be stopped prior to an interrupt causing event by issuing a Pause command. Operation of the Pause command is explained in an earlier section. In the event the Initiator does not, or stops responding, the chip is left in a state where it cannot respond to a Pause command. For this case, a Disconnect command can be used to abort the command and the connection. The Disconnect command is explained in an earlier section.

TRANSFER INFO

The Transfer Info command is an Interrupting command that is valid only when connected to the bus in the Initiator role. It is used by the Initiator for all information transfers across the SCSI bus.

A Transfer Info command is issued by an Initiator in response to a Bus Service interrupt. The Bus Service interrupt, as explained in a previous section, is received by the connected Initiator upon the following conditions: receiving the first REQ from a Target, a previous command has completed and the Target changes phases, the Target changes phases before termination, or when a previous command has completed and the Target is requesting more information. It is not valid to issue a Transfer Info command without having a Bus Service interrupt, because the Target requests and controls all transfers. The chip will only permit one Transfer Info or Transfer Pad per Bus Service interrupt.

After an Initiator receives a Bus Service interrupt, and prior to issuing a Transfer Info command, the I/O, C/D, and MSG bits from the Auxiliary Status Register (read prior to reading the Interrupt) should be examined to determine the type of information phase and the direction of transfer requested by the Target. The Initiator then prepares for the transfer. If the Single Byte Transfer bit is not going to be set in the Command Register, the Transfer Counter must be loaded prior to issuing the Transfer Info command. This is done in order to specify to the chip the maximum number of bytes to be transferred.

When a Transfer Info is issued, the chip immediately resets the Data Register Full bit in the Auxiliary Status Register. For this reason, the first byte of data for an output operation cannot be loaded into the Data Register until after the command is loaded into the Command Register. The chip then proceeds with the transfer, expecting data to be read from (input), or written to (output), its Data Register as indicated by the DMA Mode bit in the Command Register. The chip automatically detects the direction of the transfer from the I/O bit which is stored in the Auxiliary Status Register.

The chip continues a transfer until an interrupt causing event occurs. The following four events will cause the chip to terminate and interrupt.

1. The maximum number of bytes specified have been transferred and the Target activated REQ or the Information Phase changed. This event results in a Bus Service Interrupt. Either single byte transfer was specified or the Transfer Counter is zero as indicated by a bit in the Auxiliary Status Register. The Target may or may not have changed the information phase type. The I/O, C/D, and MSG bits in the Auxiliary Status Register need to be examined at the time of the interrupt to determine what phase the Target is requesting.

   (Note: due to early notification of the phase change, a phase may be selected spuriously and not transfer any data. The microprocessor should not consider this an error condition.)

2. The Target changes the information phase type before the maximum number of bytes are transferred. This event also causes a Bus Service interrupt. The new information phase may be determined by examining the I/O, C/D, and MSG bits in the Auxiliary Status Register. The Transfer Counter may be read at the time of the interrupt to determine the number of bytes remaining to be transferred. When this interrupt occurs for an output transfer, the chip may take one more byte from the microprocessor than it transfers, because of pre-fetching. However, the Transfer Counter still reflects the number of bytes remaining to be transferred.

3. The Target releases the bus by dropping BSY. This event results in a Disconnected interrupt. Following this interrupt, the chip is no longer in the Initiator role. It now remains in the Disconnected state.

4. The last byte of a Message Input phase has been received. This event results in a Function Complete interrupt. For this case, ACK is left active on the bus to allow the microprocessor to Set ATN for the purpose of rejecting the message. After this interrupt is received and a Set ATN is issued (if desired), a Message Accepted must be issued to turn off ACK for the last byte of the Message In phase.

For input transfers (I/O = 1), the chip checks parity for each byte received if the Parity Enable bit in the Control Register is on. When checking parity and the parity error occurs, the chip activates ATN prior to deactivating ACK for the byte that causes the error. It also turns on the Parity Error bit in the Auxiliary Status Register. The parity error, however, does not result in an interrupt. The chip waits for one of the four events listed above before interrupting. Therefore, the Parity Error bit should be examined when servicing any interrupt after issuing Transfer Info command for an input transfer.

If ATN is asserted by the chip, either because of a parity error or because a SET ATN command is issued, the ATN will remain asserted until the end of the connection, or until a Message Out is transferred. Therefore, during each cycle of a Transfer Info operation for output, the chip checks for a message phase (C/D = 1, MSG = 1) and also either a single byte transfer or the Transfer Counter set at zero. If these conditions exist, the chip turns off ATN prior to activating ACK for the last byte of the message.

As previously stated, a Transfer Info normally terminates with an interrupt. If a Transfer Info command must be aborted, possibly because of a timeout violation, either a Chip Reset or a Disconnect command can be used. It is noted, however, that although these commands will force the chip into a disconnected state, the Target device is left on the bus. A SCSI bus reset, which is not a chip function, is the only way an Initiator can force a Target to disconnect.

TRANSFER PAD

The Transfer Pad command is an Interrupting command that is valid only when connected to the bus as an Initiator. It is similiar to the Transfer Info command except that the data transfer between the chip and the microprocessor bus will be different.

Transfer Pad can be used by an Initiator to continue handshaking with a Target without giving data to, or taking data from, the chip. This may be useful if the Target requests an invalid Information Transfer Phase. The chip operates in the same manner as it does for a Transfer Info command, except that for output transfers it takes only one byte of data from the microprocessor and sends the same byte repeatedly until the transfer terminates. For input transfers, it accepts data from the SCSI bus but does not check parity or send it to the microprocessor. Though data is not exchanged with the microprocessor bus, the Transfer Counter is still used by the chip so that a maximum number of pad bytes can be specified.

Protocol for using a Transfer Pad command is the same as the Transfer Info except that the DMA Mode bit has significance only for output transfers. The Transfer Pad terminates because of the same four events that cause a Transfer Info command to terminate. Also, similar to the Transfer Info command, Chip Reset and Disconnect can be used to abort the command.

BUS INITIATED FUNCTIONS

SELECTION

If the Select Enable bit in the Control Register is on, the chip may be selected by another SCSI device to be a TARGET for an I/O operation. Selection occurs in the chip only if all the following conditions exist: SELOUT = 0, BSYIN = 0, SELIN = 1, I/O = 0, the chip's ID bit is asserted by the selecting device on the data bus, no more than one other ID bit (the Initiator's) is asserted on the data bus and data bus parity is good.

When all of these conditions exist, the chip is selected. It then encodes the Initiator's ID and loads it into bits 2-0 of the Source ID Register. The chip also detects whether or not the Initiator asserted its ID during selection, and either sets or resets the ID Valid bit in the Source ID Register.

The chip then asserts BSYOUT, waits for SELIN to turn off, and proceeds to take one of the following actions as a result of being selected:

1. If ATN is not asserted by the Initiator during selection, the chip generates a Selected interrupt indicating that the chip is connected as a Target.
2. If ATN is asserted, the chip simultaneously generates Selected, and Bus Service interrupts, indicating that the chip is connected as a Target and ATN is asserted.

RESELECTION

If the Reselect Enable bit in the Control Register is on, the chip may be reselected by a SCSI Target device. Reselection occurs only if SELOUT = 0, SELIN = 1, BSYIN = 0, I/O = 1, the chip's ID bit and the Target's ID bit are asserted on the data bus, no other ID bits are asserted, and data bus parity is good.

When all of these conditions exist, the chip is reselected. It then encodes the Target's ID and loads it into the Source ID Register. The chip also sets the ID Valid bit in the Source ID Register.

The chip then asserts BSYOUT and waits for SELIN to be released by the Target. When the chip detects SELIN = 0, it de-asserts BSYOUT and then generates a Reselected interrupt.

Reselection is now complete and the chip is in the connected Initiator state.

INITIALIZATION

The SCSI device may be initialized by asserting RST for a period of at least 100ns, or by issuing a Chip Reset command to the device. The NCR 5385 will respond to the RST pulse or the Chip Reset command, by immediately disconnecting from the SCSI bus, initializing all storage elements and executing an internal self-diagnostic program. The self-diagnostic is explained in a previous section (See page 17, Diagnostic Status Register). The following table lists the status of all registers after the initialization procedure.

REGISTER INITIALIZATION

	7	6	5	4	3	2	1	0
Data Register	x	x	x	x	x	x	x	x
Command Register	0	0	0	0	0	0	0	0
Control Register	0	0	0	0	0	0	0	0
Destination ID Register	0	0	0	0	0	0	0	0
Auxiliary Status Register	0	0	x	x	x	0	1	0
ID Register	0	0	0	0	0	x	x	x
Interrupt Register	0	0	0	0	0	0	0	0
Source Register	0	0	0	0	0	1	1	1
Diagnostic Status Register	1	x	x	x	x	x	x	x
Transfer Counter (MSB)	0	0	0	0	0	0	0	0
Transfer Counter (2nd)	0	0	0	0	0	0	0	0
Transfer Counter (LSB)	0	0	0	0	0	0	0	0

x = Unknown

The controlling processor should loop on reading the Diagnostic Status Register until the Self-Diagnostic Complete bit (bit 7) is on (1). This should take approximately 350 clock cycles after reset occurs. The processor should then check the remaining bits in this register for all zeroes (no errors), and then load the Control Register enabling the proper bits to begin operation. The SCSI Protocol Controller is now connected to the SCSI bus in a disconnected state. It is ready to receive commands from the controlling processor or respond to (re) selection attempts.

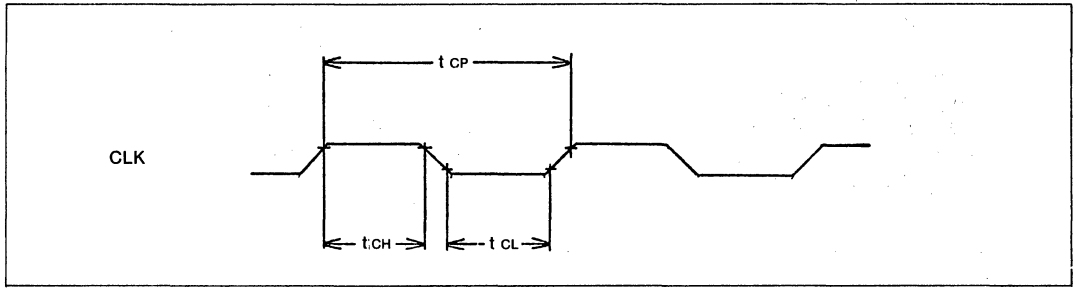
EXTERNAL CHIP TIMING

Timing requirements must be over the operating temperature (0-70°C) and voltage (4.75 to 5.25V) ranges. Loading for all output signals, except $\overline{SBEN}$, is assumed to be four low-power Schottky inputs, including 50 pF capacitance. Loading for $\overline{SBEN}$ is assumed to be ten low-power Schottky inputs, including 100 pF capacitance.

MICROPROCESSOR INTERFACE

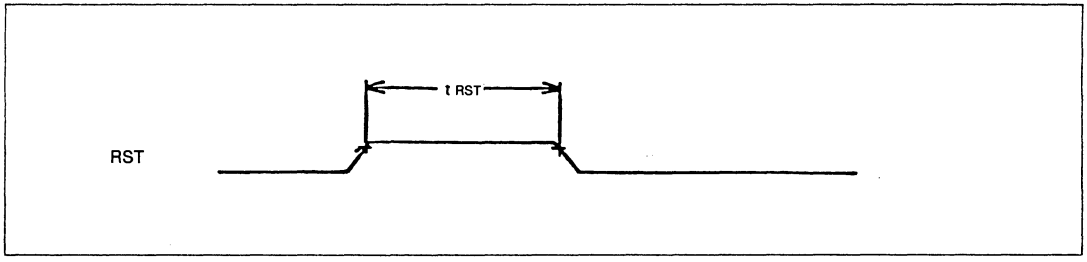
CLK

NAME	DESCRIPTION	MIN	MAX	UNITS
t_{CP}	Clock Period	100	200	ns
t_{CH}	Clock High	.45 t_{CP}	.55 t_{CP}	
t_{CL}	Clock Low	.45 t_{CP}	.55 t_{CP}	



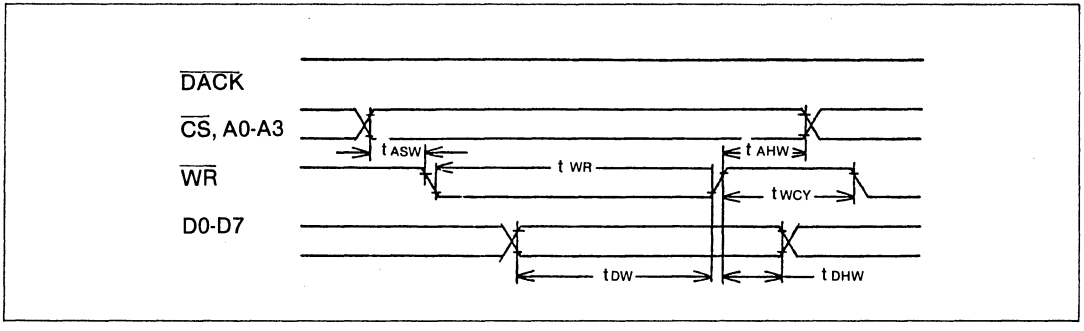
RESET

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{RST}	Reset Pulse Width	100			ns



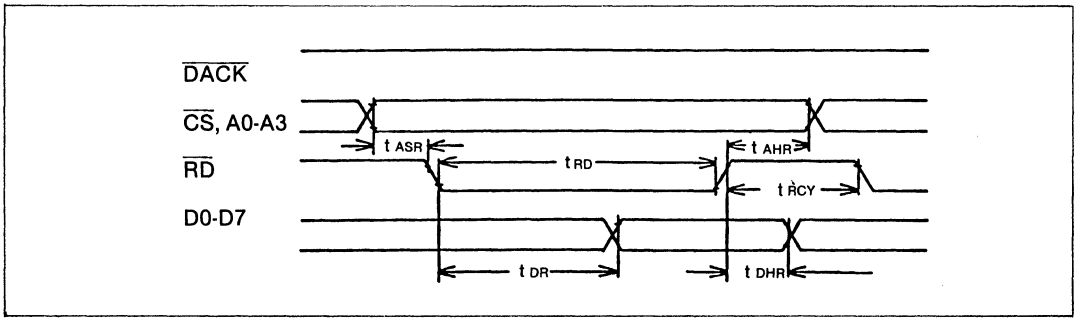
MPU WRITE

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ASW}	Address Set-up Time	0			ns
t_{WR}	$\overline{WR}$ Pulse Width	95			ns
t_{DW}	Data-to $\overline{WR}$ High	50			ns
t_{AHW}	Address Hold Time	0			ns
t_{DHW}	Data Hold Time	20			ns
t_{WCY}	$\overline{WR}$ Off to $\overline{WR}$ or $\overline{RD}$ On	125			ns



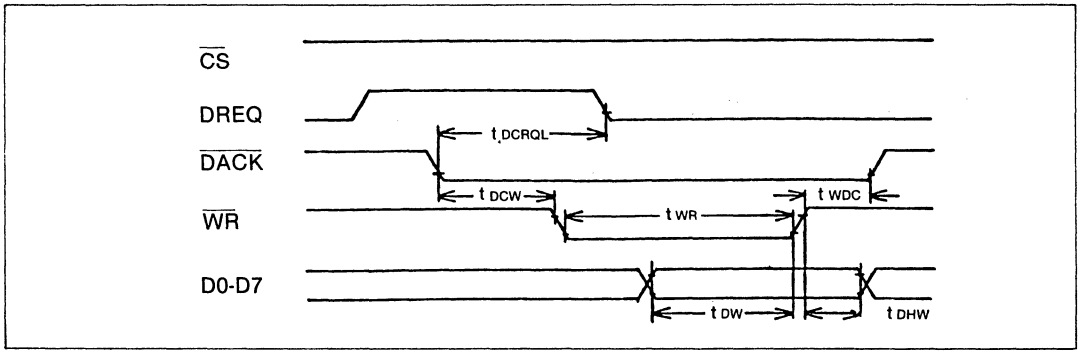
MPU READ

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ASR}	Address Set-up Time to $\overline{RD}$	0			ns
t_{RD}	$\overline{RD}$ Pulse Width	125			ns
t_{DR}	$\overline{RD}$ to Data			90	ns
t_{AHR}	Address Hold Time	0			ns
t_{DHR}	Data Hold Time	10			ns
t_{RCY}	$\overline{RD}$ Off to $\overline{WR}$ or $\overline{RD}$ On	125			ns



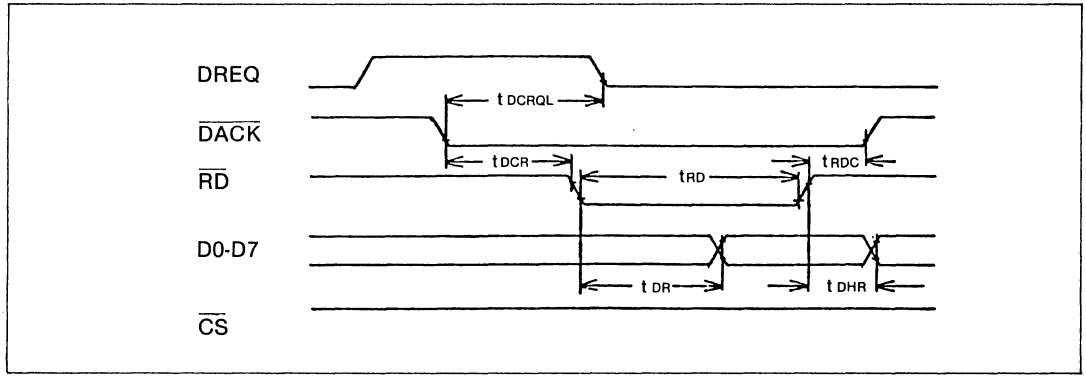
DMA WRITE

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{DCRQL}	$\overline{DACK}$ to DREQ Low	0		40	ns
t_{DCW}	$\overline{DACK}$ to $\overline{WR}$	0			ns
t_{WR}	$\overline{WR}$ Pulse Width	95			ns
t_{WDC}	$\overline{WR}$ High to $\overline{DACK}$ High	0			ns
t_{DHW}	Data Hold Time	20			ns
t_{DW}	Data to $\overline{WR}$ High	50			ns



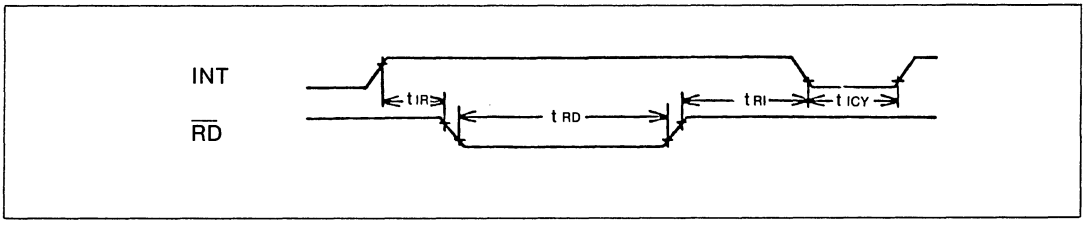
DMA READ

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{DCRQL}	$\overline{DACK}$ to DREQ Low	0		40	ns
t_{DCR}	$\overline{DACK}$ to $\overline{RD}$	0			ns
t_{RD}	$\overline{RD}$ Pulse Width	95			ns
t_{RDC}	$\overline{RD}$ High to $\overline{DACK}$ High	0			ns
t_{DHR}	Data Hold Time	10			ns
t_{DR}	$\overline{RD}$ to Data			80	ns



INTERRUPT

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{IR}	INT to $\overline{RD}$	0			ns
t_{RD}	$\overline{RD}$ Pulse Width	95			ns
t_{RI}	$\overline{RD}$ High to INT Low			125	ns
t_{ICY}	INT Off to INT On	125			ns



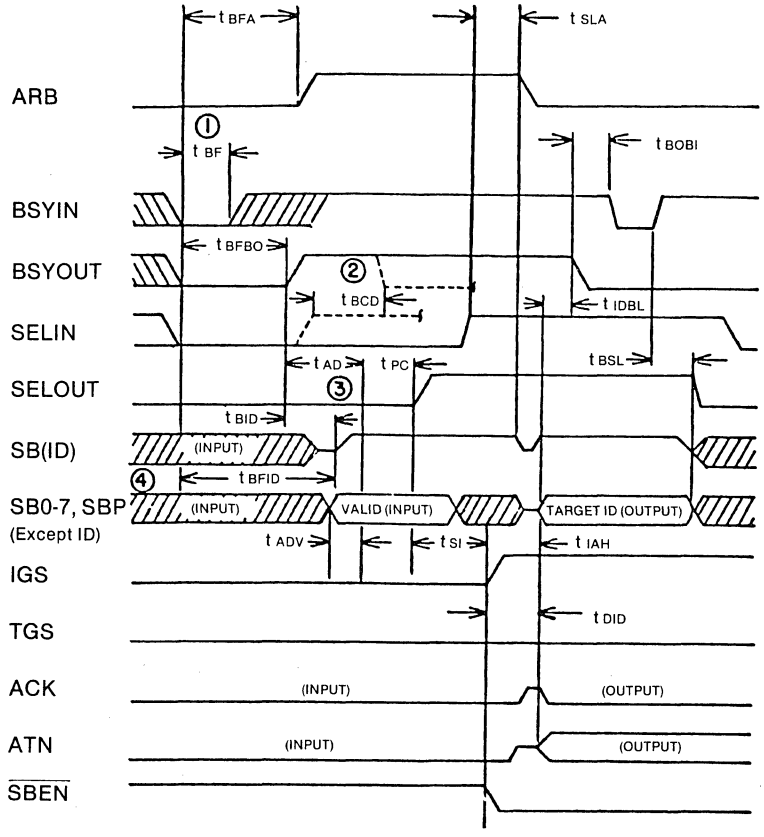
SCSI INTERFACE

SELECTION (INITIATOR)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{BF}	Bus Free	85			ns
t_{BFA}	Bus Free to ARB high	100		800	ns
t_{SLA}	SELIN Active to ARB low & ID bit Disabled	40			ns
t_{BFBO}	Bus Free to BSYOUT	100		800	ns
t_{BCD}	Bus Clear Delay			225	ns
t_{AD}	Arbitration delay	2.0			μs
t_{PC}	Priority check to SELOUT	0			ns
t_{BID}	BSYOUT high to ID bit high	100			ns
t_{BFID}	Bus Free to ID high			900	ns
t_{ADV}	Arbitration Data Valid to Priority Check	0			ns
t_{SI}	SELOUT to IGS & $\overline{SBEN}$	950			ns
t_{IAH}	IGS high to ATN high	85			ns
t_{IDBL}	Target ID & ATN high to BSYOUT low	100			ns
t_{BOBI}	BSYOUT low to BSYIN low	0		450	ns
t_{BSL}	BSYIN high to SELOUT low	100			ns
t_{DID}	$\overline{SBEN}$ active to Bus enabled	85			ns

NOTES:

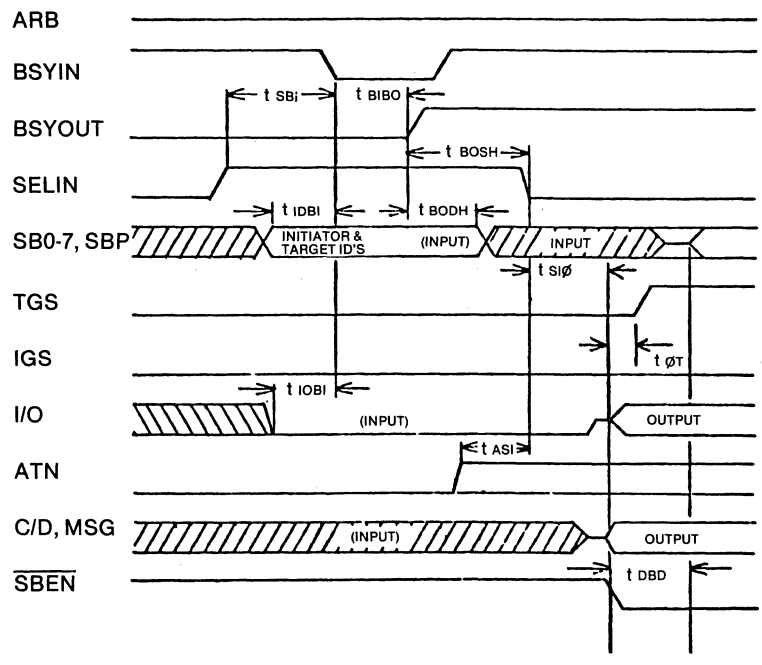
1. The chip ensures that the bus remains free (BSYIN and SELIN inactive) for t_{BF} before attempting arbitration.
2. If SELIN becomes active at any time during arbitration, the chip must deassert BSYOUT within t_{BCD}.
3. The chip waits (t_{AD}), and then checks to see if arbitration is won (t_{PC}). The chip then asserts SELOUT if arbitration is won.
4. One of the data bits is assigned as an ID bit by the $\overline{ID0}$-$\overline{ID2}$ signals. During Bus Free, the chip places all of the data bits, including ID, in a high impedance state. During arbitration the chip enables its ID bit and drives it high, but the remainder of the data bits remain in the high impedance state for reading.


ARB
BSYIN
BSYOUT
SELIN
SELOUT
SB(ID)
SB0-7, SBP
(Except ID)
IGS
TGS
ACK
ATN
SBEN
t BFA
t SLA
t BF
t BOBI
t BFBO
t BCD
t IDBL
t AD
t PC
t BSL
t BID
(INPUT)
t BFID
(INPUT)
VALID (INPUT)
TARGET ID (OUTPUT)
t ADV
t SI
t IAH
t DID
(INPUT)
(OUTPUT)
(INPUT)
(OUTPUT)

NCR

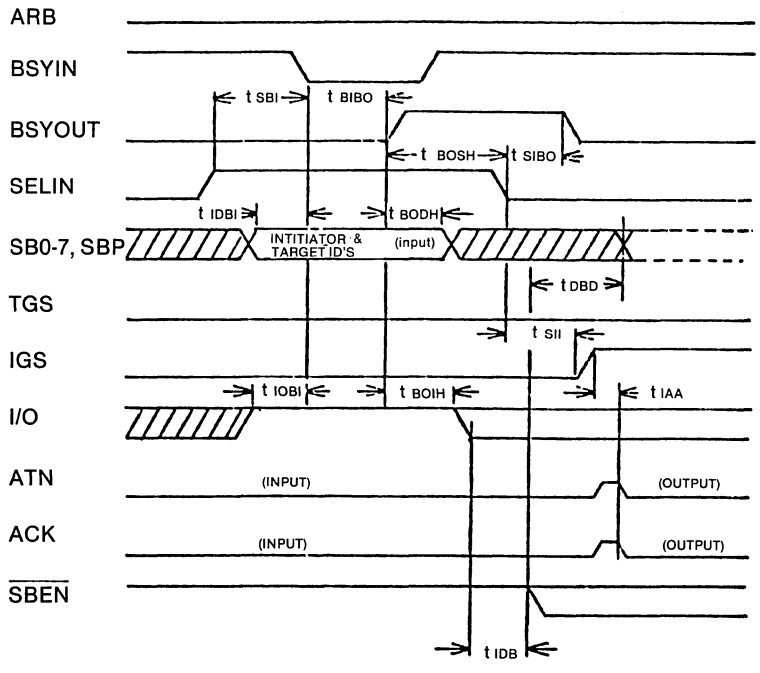
SELECTION (TARGET)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{SBI}	SELIN high to BSYIN low	50			ns
t_{IDBI}	ID's valid to BSYIN low	0			ns
t_{IOBI}	I/O low to BSYIN low	0			ns
t_{BIBO}	BSYIN low to BSYOUT high	0		2.0	μs
t_{BODH}	BSYOUT high Data Hold	0			ns
t_{BOSH}	BSYOUT high SELIN Hold	0			ns
t_{ASI}	ATN high to SELIN low	0			ns
$t_{SI\emptyset}$	SELIN low to Phase signals Enabled	0			ns
$t_{\emptyset T}$	Phase signals enabled to TGS High	85			ns
t_{DBD}	SBEN low to Data Bus Enabled	85			ns



RESELECTION (INITIATOR)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{SBI}	SELIN high to BSYIN low	50			ns
t_{IDBI}	ID's valid to BSYIN low	0			ns
t_{IOBI}	I/O high to BSYIN low	0			ns
t_{BIBO}	BSYIN low to BSYOUT high	0		2.0	μs
t_{BODH}	BSYOUT high Data Hold	0			ns
t_{BOSH}	BSYOUT high SELIN Hold	0			ns
t_{BOIH}	BSYOUT high I/O hold	0			ns
t_{SIBO}	SELIN low to BSYOUT low	0			ns
t_{SII}	SELIN low to IGS high	0			ns
t_{IAA}	IGS high to ACK & ATN enabled	85			ns
t_{IDB}	I/O low to $\overline{SBEN}$ low	0			ns
t_{DBD}	$\overline{SBEN}$ low to Data Bus Enabled	85			ns

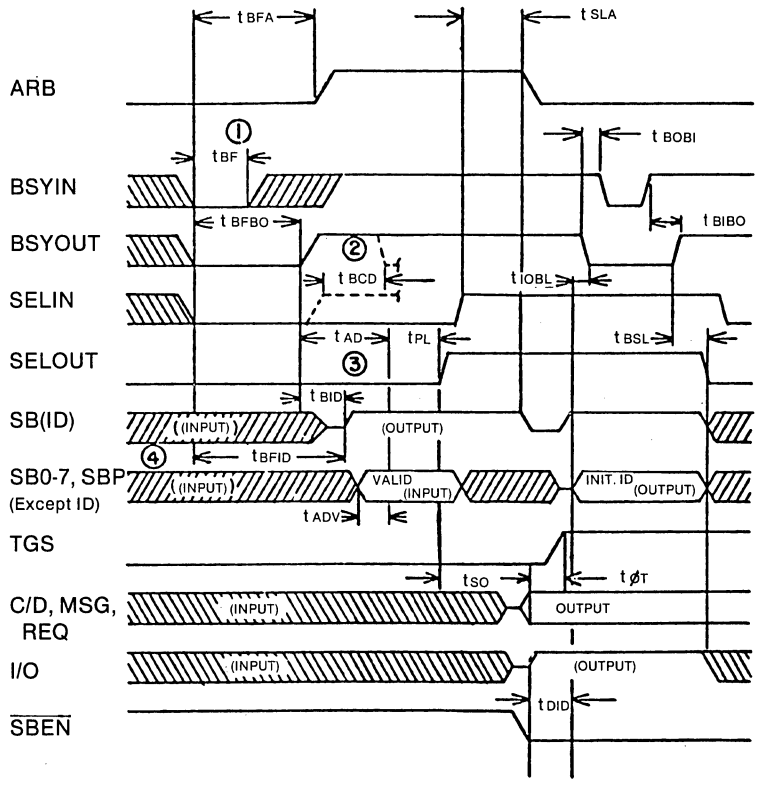


RESELECTION (TARGET)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{BF}	Bus Free	85			ns
t_{BFA}	Bus Free to ARB high	100		800	ns
t_{SLA}	SELIN active to ARB Low and ID bit Disabled	40			ns
t_{BFBO}	Bus Free to ID high	100		800	ns
t_{BCD}	Bus Clear Delay			225	ns
t_{AD}	Arbitration delay	2.0			μs
t_{PC}	Priority check to SELOUT	0			ns
t_{BID}	BSYOUT high to ID bit high	100			ns
t_{BFID}	Bus Free to ID high			900	ns
t_{ADV}	Arbitration Data Valid to Priority Check	0			ns
$t_{S\emptyset}$	SELOUT to Phase signals Enabled & $\overline{SBEN}$ Low	950			ns
$t_{\emptyset T}$	Phase Signals Enabled to TGS High	85			ns
t_{DID}	$\overline{SBEN}$ low to Bus Enabled	85			ns
t_{IDBL}	Target ID & ATN high to BSYOUT low	100			ns
t_{BOBI}	BSYOUT low to BSYIN high	0		450	ns
t_{BIBO}	BSYIN high to BSYOUT high	0		2.0	μs
t_{BSL}	BSYOUT high to SELOUT low	100			ns

NOTES:

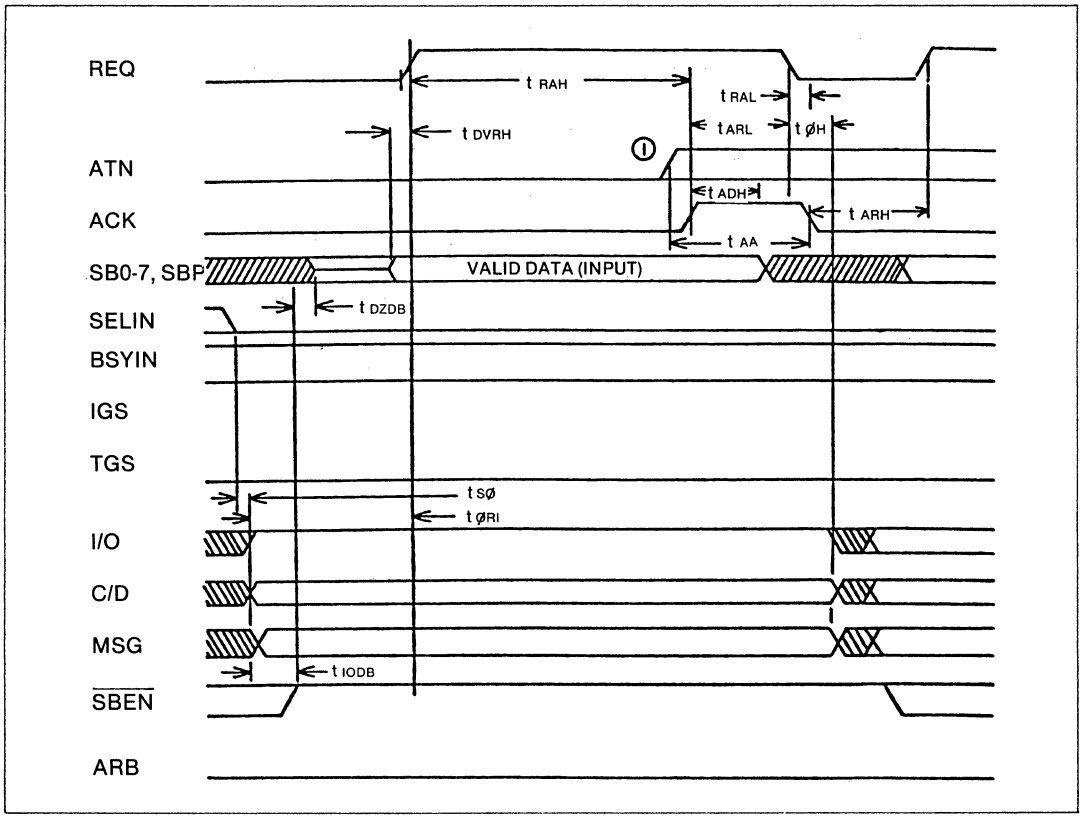
1. The chip ensures that the bus remains free (BSYIN and SELIN inactive) for t_{BF} before attempting arbitration.
2. If SELIN becomes active at any time during arbitration, the chip must deassert BSYOUT within t_{BCD}.
3. The chip waits (t_{AD}), and then checks to see if arbitration is won (t_{PC}). The chip then asserts SELOUT if arbitration is won.
4. One of the data bits is assigned as an ID bit by the $\overline{ID0}$-$\overline{ID2}$ signals. During Bus Free, the chip places all of the data bits, including ID, in a high impedance state. During arbitration the chip enables its ID bit and drives it high, but the remainder of the data bits remain in the high impedance state for reading.


t BFA
t SLA
ARB
①
t BF
t BOBI
BSYIN
t BIBO
t BFBO
BSYOUT
②
t BCD
t IOBL
SELIN
t AD
tPL
t BSL
SELOUT
③
t BID
SB(ID)
(INPUT)
(OUTPUT)
④
t BFID
SB0-7, SBP
(Except ID)
(INPUT)
VALID
(INPUT)
INIT. ID
(OUTPUT)
t ADV
TGS
tSO
t ØT
C/D, MSG,
REQ
(INPUT)
OUTPUT
I/O
(INPUT)
(OUTPUT)
t DID
SBEN

INFORMATION TRANSFER PHASE INPUT (INITIATOR)

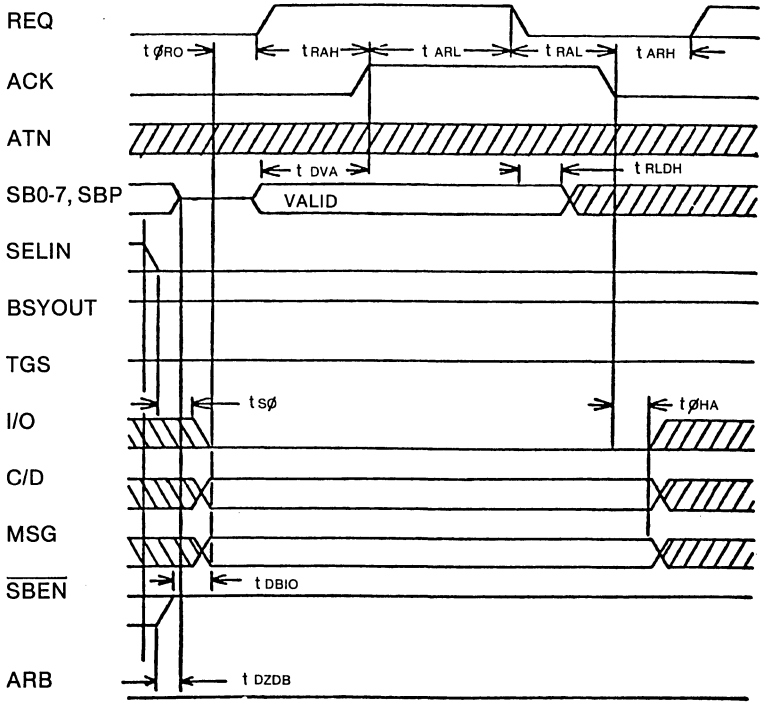
NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{DVRH}	Data Valid to REQ high	0			ns
$t_{\phi RI}$	Phase Valid to REQ high	100			ns
t_{RAH}	REQ high to ACK high	0			ns
t_{RAL}	REQ low to ACK low	0			ns
t_{AA}	ATN high to ACK low	100			ns
$t_{S\phi}$	SELIN low to Phase change	0			ns
$t_{\phi H}$	Phase hold from ACK low	20			ns
t_{ADH}	Data hold from ACK high	0			ns
t_{ARL}	ACK high to REQ low	35			ns
t_{IODB}	I/O high to SBEN high			50	ns
t_{DZDB}	Data Bus disable from SBEN high			10	ns
t_{ARH}	ACK Low to REQ High	35			ns

NOTE 1: If the chip detects a parity error it must assert ATN at least t_{AA} before it de-asserts ACK.



INFORMATION TRANSFER PHASE INPUT (TARGET)

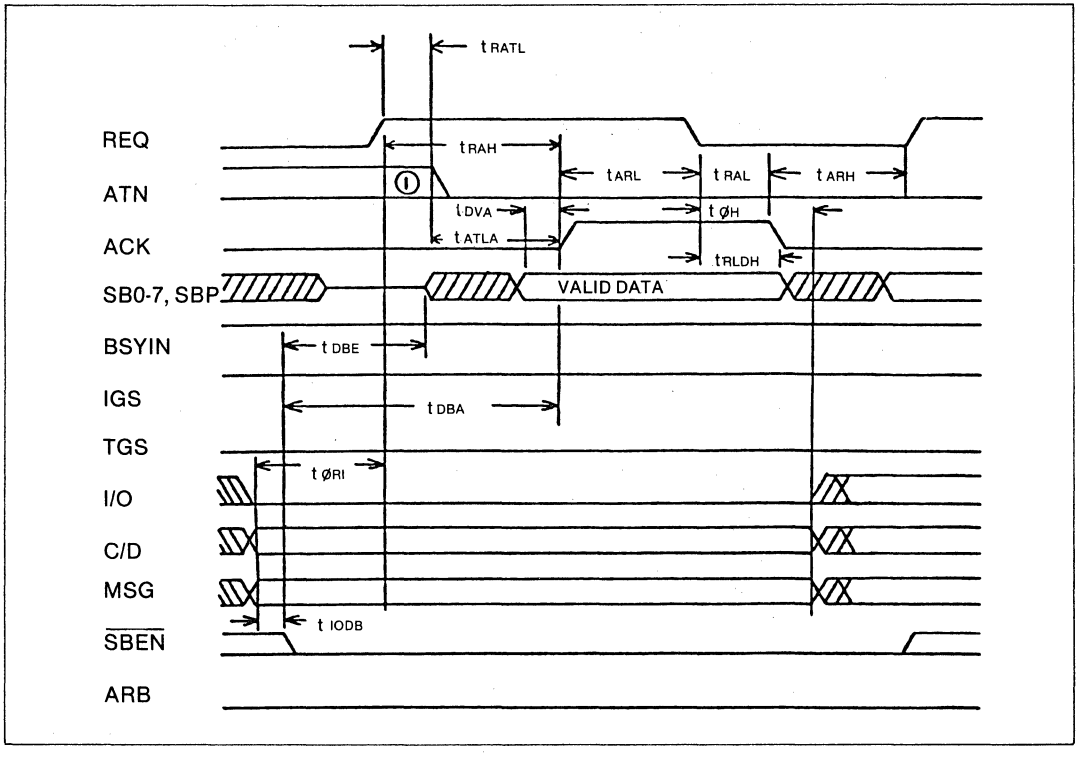
NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_{S\emptyset}$	SELIN low to Phase Change	0			ns
$t_{\emptyset RO}$	Phase Change to REQ out	500			ns
t_{RAH}	REQ high to ACK high	35			ns
t_{ARL}	ACK high to REQ low	0			ns
t_{DVA}	Data Valid to ACK high	0			ns
t_{RAL}	REQ low to ACK low	35			ns
t_{ARH}	ACK low to REQ high	0			ns
t_{RLDH}	REQ low Data Hold	0			ns
$t_{\emptyset HA}$	Phase Hold from ACK low	0			ns
t_{DBIO}	SBEN high to I/O low	0			ns
t_{DZDB}	Data Bus disable to SBEN high	0			ns



INFORMATION TRANSFER PHASE OUTPUT (INITIATOR)

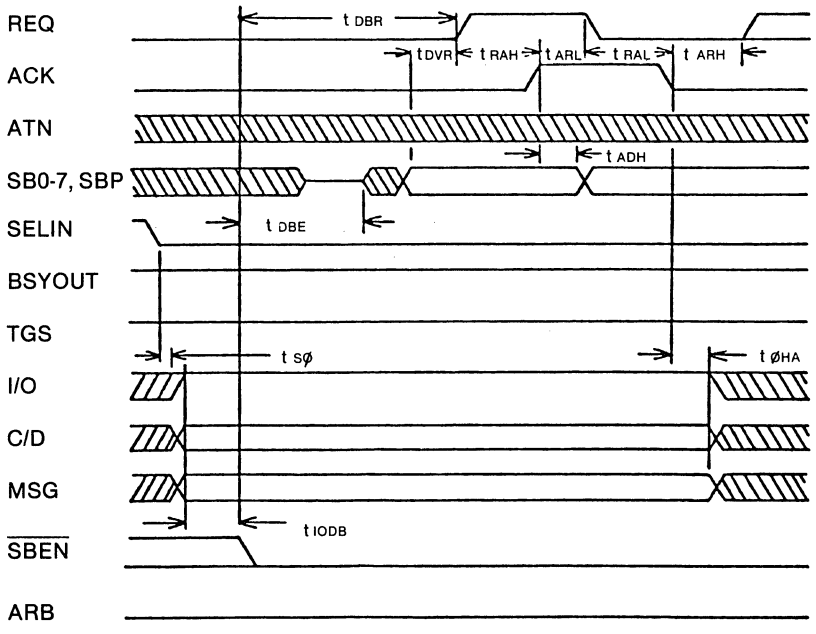
NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_{\phi RI}$	Phase Valid to REQ high	100			ns
t_{RAH}	REQ high to ACK high	35			ns
t_{RAL}	REQ low to ACK low	0			ns
t_{DVA}	Data Valid to ACK high	100			ns
t_{RLDH}	REQ low Data hold	0			ns
$t_{\phi H}$	Phase hold from ACK low	20			ns
t_{ARL}	ACK high to REQ low	0			ns
t_{IODB}	I/O low to $\overline{SBEN}$ low	0			ns
t_{DBE}	$\overline{SBEN}$ low to Data Bus Enable	85			ns
t_{DBA}	$\overline{SBEN}$ low to ACK high	185			ns
t_{RATL}	REQ High to ATN low	0			ns
t_{ATLA}	ATN Low to ACK High	25			ns
t_{ARH}	ACK Low to REQ High	35			ns

NOTE 1: ATN is only de-asserted in this manner during the last byte of a Message Out Phase.



INFORMATION TRANSFER PHASE OUTPUT (TARGET)

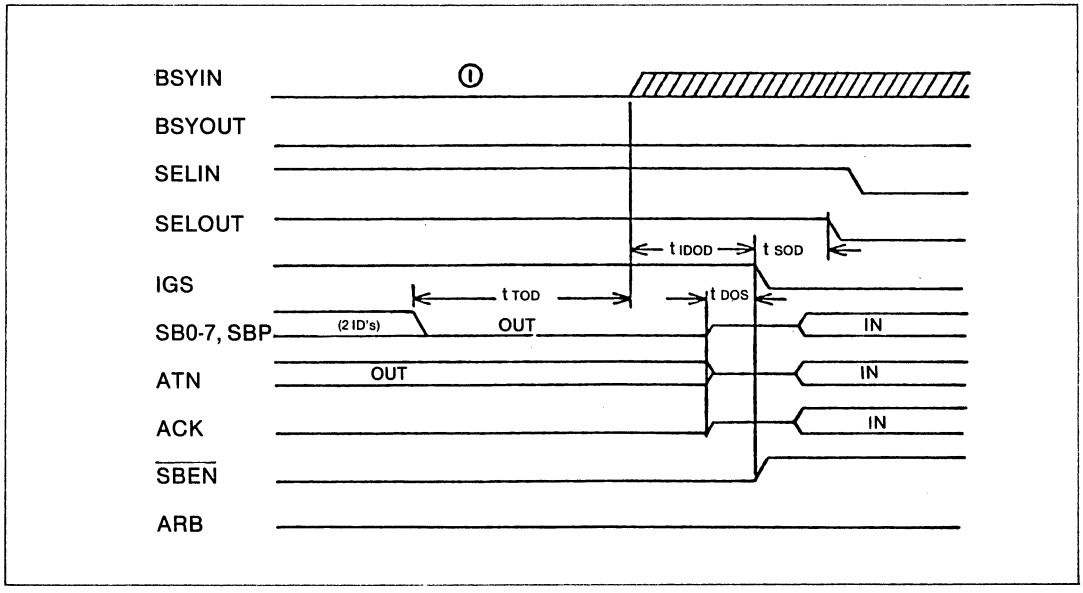
NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_{S\emptyset}$	SELIN low to Phase Change	0			ns
t_{IODB}	I/O high to $\overline{SBEN}$ low	500			ns
t_{DBR}	$\overline{SBEN}$ low to REQ out	185			ns
t_{DVA}	Data Valid to REQ high	100			ns
t_{RAH}	REQ high to ACK high	0			ns
t_{ARL}	ACK high to REQ low	0			ns
t_{RAL}	REQ low to ACK low	0			ns
t_{ARH}	ACK low to REQ high	0			ns
$t_{\emptyset HA}$	Phase hold from ACK low	0			ns
t_{ADH}	Data hold from ACK low	0			ns
t_{DBE}	$\overline{SBEN}$ low to Data Bus Enabled	85			ns



BUS RELEASE FROM SELECTION (INITIATOR)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{TOD}	Bus Release Timeout Delay	100			μs
t_{IDOD}	IGS & $\overline{SBEN}$ Turn-off Delay	0			ns
t_{SOD}	SELOUT Turn-off Delay	0			ns
t_{DOS}	Driver Turn-off set-up to IGS & $\overline{SBEN}$ off	0			ns

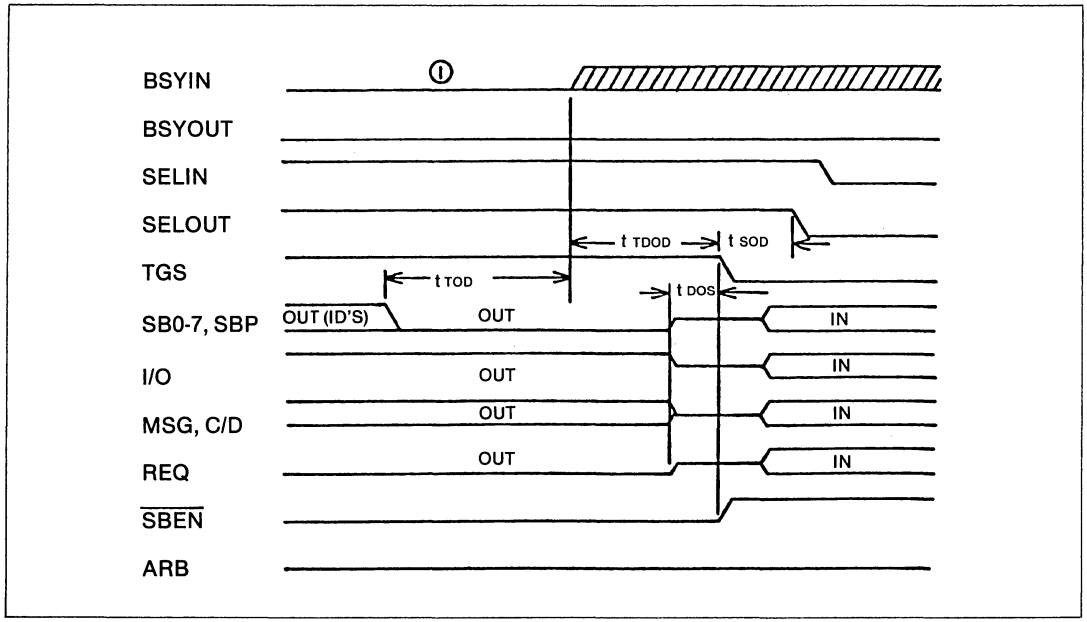
NOTE 1: If the chip detects BSYIN active by the end of the timeout delay, the bus release sequence shall be aborted since selection has been successful.



BUS RELEASE FROM RESELECTION (TARGET)

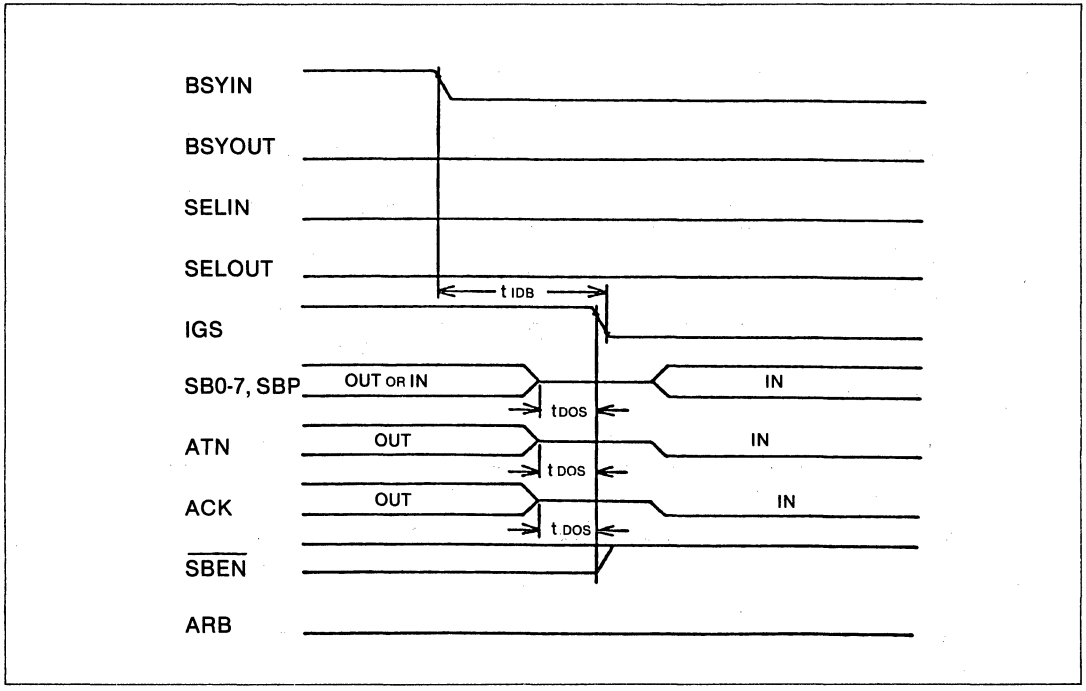
NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{TOD}	Bus Release Timeout Delay	100			*us*
t_{DOD}	TGS & $\overline{SBEN}$ Turn-off Delay	0			ns
t_{SOD}	SELOUT Turn-off Delay	0			ns
t_{DOS}	Driver Turn-off set-up to TGS & $\overline{SBEN}$ off	0			ns

NOTE 1: If the chip detects BSYIN active by the end of the timeout delay, the bus release sequence shall be aborted since reselection has been successful.



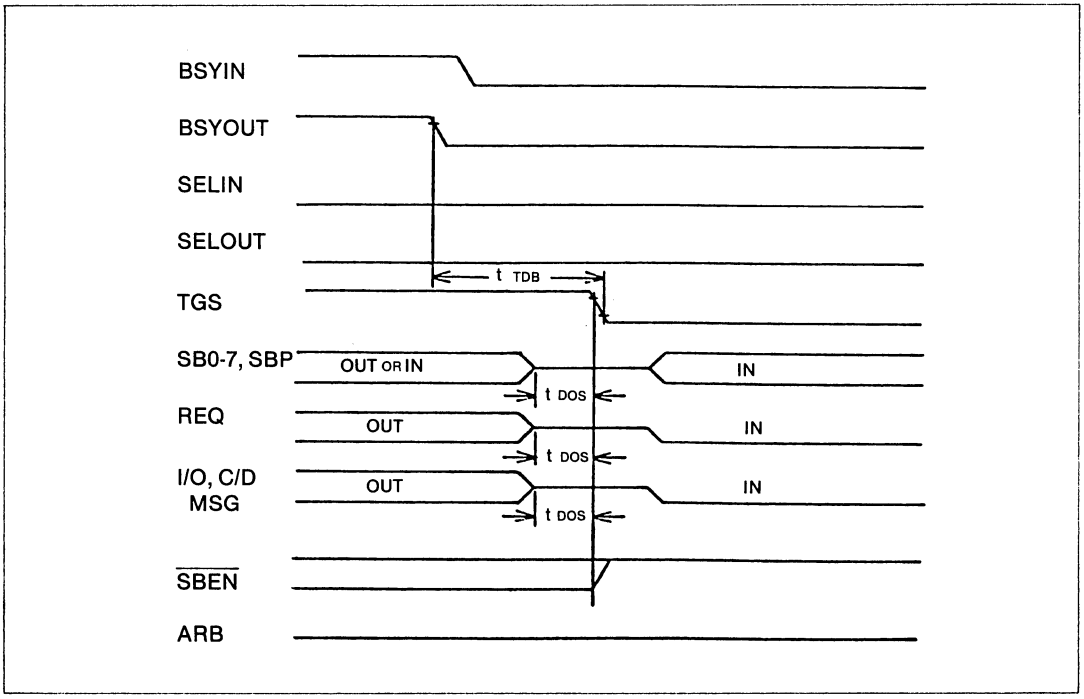
BUS RELEASE FROM INFORMATION PHASE (INITIATOR)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{IDB}	IGS & $\overline{SBEN}$ Turn-off Delay from BSYIN off			225	ns
t_{DOS}	Driver Turn-off set-up to IGS off	0			ns



BUS RELEASE FROM INFORMATION PHASE (TARGET)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{TDB}	TGS & $\overline{SBEN}$ Turn-off from BSYOUT off			225	ns
t_{DOS}	Driver Turn-off set-up to TGS off	0			ns



NCR Microelectronics Division
1635 Aeroplaza Drive
Colorado Springs, Colorado 80916
Telex: 452-457
Phone: 303/596-5612
800/525-2252

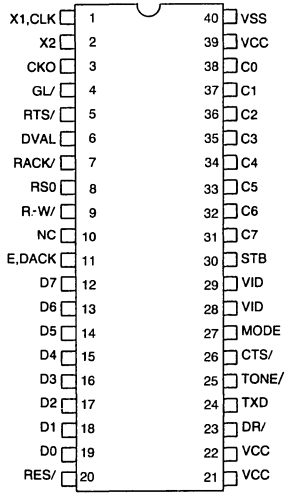
8301
BAR CODE PROCESSOR

- **Recognition of single or multiple codes, mask programmable**
- **Bidirectional decoding**
- **Scan velocity 1 to 50 in/s (.007 inch bar)**
- **32 character tag buffer**
- **Serial ASCII from 300 to 9600 baud**
- **Stand-alone or peripheral use**
- **Parallel interface for ASCII display or microprocessor**
- **Good read output**
- **Audio acknowledge output**
- **TTL-compatible inputs and outputs**
- **Ease of system design and application**
- **Single +5 volt power supply**

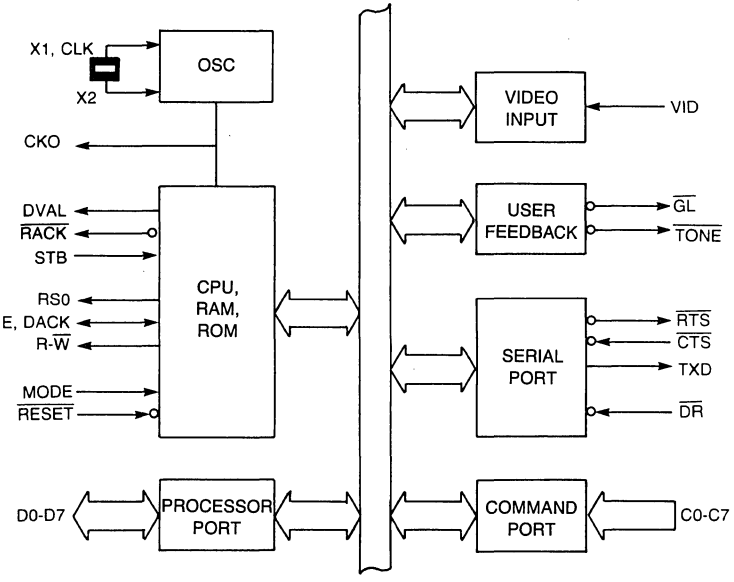
The NCR 8301 Bar Code Processor is a single chip NMOS circuit in a 40-pin DIP. It is designed expressly for decoding bar codes. The 8301 decodes Code 39 and Interleaved 2 of 5.

The NCR 8301 provides an asynchronous serial communications port for ease of system design. A parallel interface is also available. The NCR 8301 accommodates stand-alone or peripheral bar code reading applications.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



SPECIAL FUNCTION CHIPS

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PIN DESCRIPTIONS

The following pin descriptions are for 8301 implementations in either "stand-alone" or "peripheral" mode.

Symbol	Pin No.	Type	Name and Function
VID	28,29	I	VIDEO DATA: Time modulated bar/space stream from wand or other scanning device.
GL/	4	O	GOOD READ LAMP: Normally high, pulls low to indicate a good read.
TONE/	25	O	AUDIO OUTPUT: Normally high, pulls low to create an audio tone of good read (1200 Hz).
TXD	24	O	SERIAL TRANSMITTER OUTPUT: Decoded ASCII tag data.
DR/	23	I	DATA RECEIVED INPUT: Acknowledge from host that correct data was received over the serial port.
RESET/	20	I	RESET: Master reset input. Reset must remain active low for a minimum of eight cycles after VCC reaches operating range and the clock output (CKO) has stabilized.
X1,CLK	2	I	CLOCK CRYSTAL: 4 MHz crystal or 4 MHz TTL clock input generates 2 MHz internal clock.
X2	1	O	CRYSTAL: Crystal connection if crystal is used, otherwise X2 is floated.
CKO	3	O	CLOCK: 2 MHz internal clock output.
D0-D7	12-19	I/O	COMMAND/DATA BUS: Bi-directional data bus. Also, in peripheral mode, used for configuration byte any time reset is asserted.
RS0	8	O	REGISTER SELECT: This output is used to select the command or data registers of the peripheral device, e.g. display.
R-W/	9	O	READ: This pin supplies the read/write handshake.
RTS/	5	O	REQUEST TO SEND: RS-232 handshake for data transmitted by the 8301 BCP.
CTS/	26	I	CLEAR TO SEND: RS-232 handshake for data transmitted by the 8301 BCP. If not provided by the user, CTS/ should be tied to RTS/ or VSS.
MODE	27	I	MODE SELECT: Selects 8301 operating mode at power-up or reset by loading the internal command register from either the data bus or the command port.
VCC	21,22,39		VCC: +5V power supply.
VSS	40		VSS:Power Supply Gnd.

The following pin function descriptions are for the 8301 operation in "stand-alone" mode.

E	11	O	ENABLE: Peripheral device clock.
C0-C7	31-38	I	COMMAND: Input accepts configuration byte at reset.

The following pin function descriptions are for the 8301 operation in "peripheral" mode.

RACK/	7	O	READ ACKNOWLEDGE: This active low output identifies that the BCP has read the processor port.
DVAL	6	O	DATA VALID: This output is intended to interupt the host microprocessor when the BCP has decoded tag data or status.
DACK	11	I	DATA ACKNOWLEDGE: This input informs the BCP that the host has received data.
STB	30	I	STROBE: This input is used to notify the BCP that it should read the data bus.

DEVICE OPERATION

GENERAL DESCRIPTION

The 8301 bar code processor (BCP) is partitioned logically into three sections. The first is the Bar Code/ User interface, the second is the CPU interface, and the third is the Serial Communication interface shown in Figure 1.

This unit is configured to support both stand-alone and peripheral modes through the use of an 8-bit CPU. Bar code tags are decoded in real time, eliminating the need for an external RAM tag buffer.

Tags containing up to 32 characters of information can be buffered by the BCP. Once decoded, the ASCII tag data can be rapidly forwarded to a remote processor at up to 9600 baud over a serial asynchronous interface. The same ASCII data can be output on the data bus for use by a processor.

The state of the MODE input on power-up or reset determines whether the BCP is in "stand-alone" or "peripheral" mode. If MODE is low, then stand-alone mode is selected, otherwise peripheral mode is enabled. The internal command register is loaded via the data bus from the master processor if peripheral mode is selected. Alternatively, means are provided for loading the command register from the command port in stand-alone mode.

The 8301 BCP decodes Code 39 and Interleaved 2-of-5 automatically, without prior code selection. Other codes can be supported by changing the ROM algorithm.

PROCESSOR

The Processor section contains an 8-bit microcomputer. The unique OMNICODE (TM) feature allows full bi-directional decoding of Code 39 and Interleaved 2 of 5. It distinguishes between these bar code standards without a code switch. The processor also coordinates all I/O activity.

WAND INPUT

The wand input section contains edge detection circuitry and a 16-bit counter which measures pulse duration. The video input accepts a TTL signal and provides transition detection that initializes the pulse counter. The value of this count is used in decoding the bar code. Logic sense of the video input is positive, i.e. a bar = 1 and a space = 0.

USER FEEDBACK

Visual and audible feedback is provided with the 8301 BCP. A good read will generate a 1.2 KHz signal at the TONE/ output for a period of 70 msec and will also cause the GL/ output to be activated. The GL/ and TONE/outputs will be activated after the complete tag has been transmitted and host acknowledgement has been received. The BCP will then be ready to read another tag.

It should be noted that during data transmission time and GL/ active time the video input is disabled.

SERIAL PORT

The asynchronous serial I/O port is used for communicating ASCII data from bar code tags to a host station. The serial port is capable of operating at four popular baud rates from 300 to 9600 baud.

PROCESSOR PORT

The 8-bit processor port allows the 8301 BCP to act as a slave processor in the peripheral mode. It provides bi-directional communication of commands, data, and status with the master processor.

When used in the stand-alone mode, the processor port will typically be used to exchange ASCII data with peripherals using proper handshaking (e.g. display).

SELF TEST

The BCP features a self test mode. Upon reset or power-up reset, the BCP verifies operation of the CPU, RAM, ROM and counters. In order to assure the user that selftest was successful, the "good lamp" and tone outputs are activated.

PERIPHERAL MODE

INITIALIZATION

If the mode input is active (high) on power-up, the 8301 BCP will assume the peripheral mode of operation. In the peripheral mode, the 8301 BCP will act as a slave to the master system processor. (See Figure 3 for typical configuration.) At initialization the BCP will need configuration information from the system processor. This information is covered in the description of the command register. Timing Diagram 1 describes the procedure for writing this command byte to the BCP for the circuit shown in Figure 3. This timing diagram also shows how data can be transferred to the BCP.

STATUS AND DATA TRANSFERS ON PROCESSOR PORT (Peripheral Mode)

Once a tag has been successfully decoded, the BCP will assert DVAL, indicating that data is available. The first byte sent to the processor is the status register. Status bit 7 is true. Then bit 5 and bit 6 will indicate which code was scanned, and bits 0-4 will contain the current message length. On a good read, the decoded tag data will follow the status byte. Refer to Timing Diagram 2 for outputting status and data. No check sum is transmitted over the processor port. In a Code 39 message, asterisks are not transmitted before or after the message, nor are they counted in the message length.

No status is sent to the processor on a bad read. Data valid is not asserted in this case.

STATUS AND DATA TRANSFERS ON SERIAL PORT (Peripheral Mode)

Once the status byte has been transferred across the parallel port, the 8301 BCP will transfer the same information across the serial link. The communication will then alternate between parallel and serial transmissions until the entire message has been sent. This assumes that the command register was programmed for serial and parallel operation. Refer to Timing Diagram 4 for serial timing information.

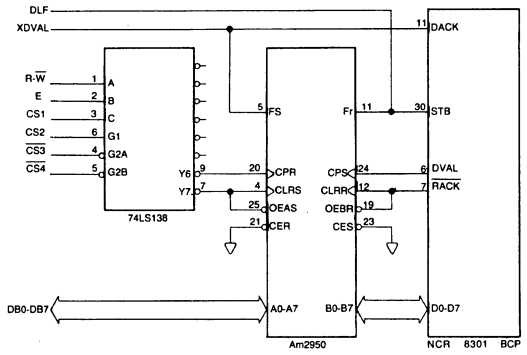
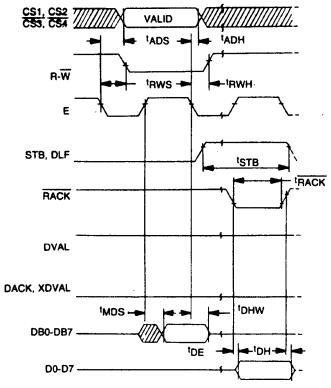
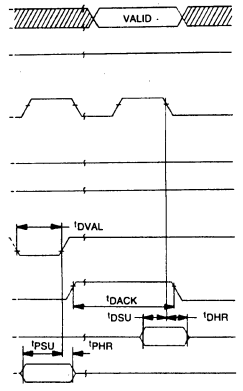


FIGURE 3. TYPICAL PERIPHERAL MODE CONFIGURATION



TIMING DIAGRAM 1. PERIPHERAL COMMAND/DATA WRITE TO BCP.



TIMING DIAGRAM 2. PERIPHERAL STATUS/DATA READ FROM BCP.

TIMING PARAMETERS FOR WRITE AND READ TO BCP

Symbol	Parameter	Min	Max	Units
t_{ADS}	Address Set-Up Time		140	nsec
t_{ADH}	Address Hold Time	30		nsec
t_{RWS}	R,W/ Set-Up Time		140	nsec
t_{RWH}	R,W/ Hold Time	30		nsec
t_{STB}	STB, DLF Width	6.5		μsec
$t_{RACK/}$	RACK/ Width	4.0		μsec
t_{MDS}	Data Bus Write Delay		150	nsec
t_{DHW}	Data Bus Write Hold	30		nsec
t_{DE}	Data Enable		1.0	μsec
t_{DH}	Data Hold Time	0		μsec
t_{DVAL}	DVAL Width	4.0		μsec
t_{PSU}	Periphral Set-Up Time		2.5	μsec
t_{PHR}	Peripheral Hold Time	0		μsec
t_{DACK}	DACK, XDVAL Width	0.5		μsec
t_{DSU}	Data Bus Set-Up	35		nsec
t_{DHR}	Data Bus Read Time	10		nsec

STAND-ALONE MODE

INITIALIZATION

The 8301 BCP is "smart" enough to operate as a stand-alone bar code processor. If the MODE input is active (low) on power-up reset, the BCP will assume the stand-alone operating mode. In this mode the configuration information will be read from the command port. Figure 4 shows a typical stand-alone configuration. The BCP supports 6500 and 6800 peripherals in stand-alone mode.

If an ASCII display is attached to the BCP, unique characters will be output on the parallel bus to distinguish detected errors. Specific error types and corresponding display messages are covered in the status section.

The command bytes used to control the display in the stand-alone mode are compatible with the Hitachi HD43160A LCD display controller/character generator.

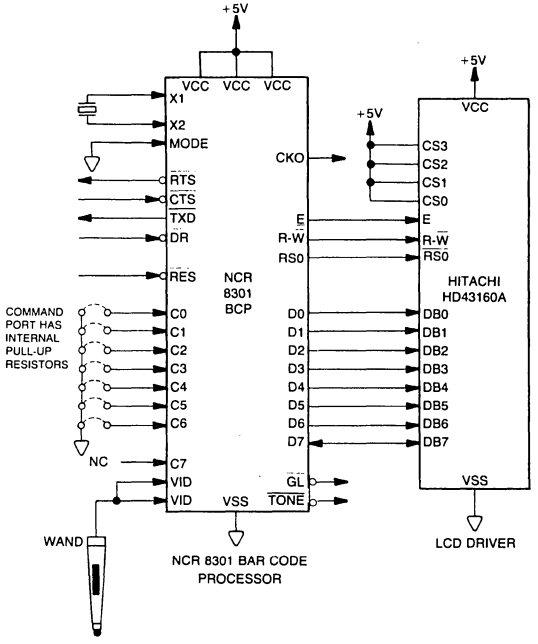


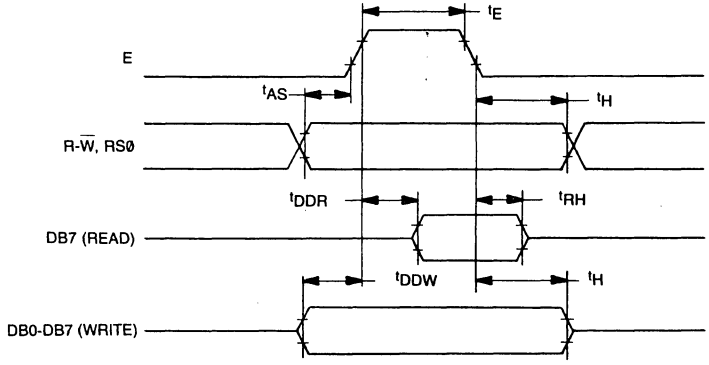
FIGURE 4. TYPICAL STAND-ALONE CONFIGURATION

STATUS AND DATA TRANSFER ON PROCESSOR PORT (Stand-Alone Mode)

A typical configuration may contain a display attached to the parallel port. Timing Diagram 3 provides the necessary timing for outputting this data.

STATUS AND DATA TRANSFER ON SERIAL PORT (Stand-Alone Mode)

Serial communications is performed identically in both the stand-alone and peripheral modes of operation. Refer to Timing Diagram 4 for serial timing information.



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_E	ENABLE pulse width	2.5	-	μs
t_{AS}	Setup time	2.5	-	μs
t_H	Hold time	2.5	-	μs
t_{RH}	READ data hold time	10	-	ns
t_{DDW}	Data delay time (WRITE)	-5000	225	ns
t_{DDR}	Data delay time (READ)		300	ns

TIMING DIAGRAM 3. STAND-ALONE PARALLEL PORT

NCR

SERIAL COMMUNICATIONS

Decoded tag data and status can be passed over the serial port (TXD) if that data output mode is enabled via the command byte. Baud rate and parity options are also determined by the command byte. Baud rates from 300 to 9600 are supported as described in the command register section.

Three serial operating modes are available as described in the following sections.

STANDARD MODE (Status, Data, Checksum)

Characters are transmitted asynchronously, beginning with the status byte. Status and data are not passed when "bad read" conditions occur. Upon capturing a valid tag, the BCP first attempts to transmit status. Status includes code type and message length (1 to 32 characters). Ready to send (RTS/) is activated and the BCP looks for a clear to send (CTS/) response from the host station. Upon receipt of CTS/ the BCP transmits status. The same protocol is followed for each data character from first to last. See Timing Diagram 4 for timing information.

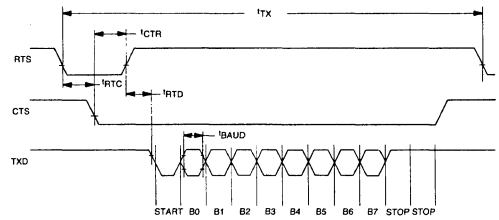
After the last data character has been passed, a 7-bit checksum character is transmitted. The checksum is a straight binary addition without carry over the first 7 bits of status and data. If the host station computes a matching checksum, the data received (DR/) input is asserted to the BCP. Successful completion of this procedure results in a good lamp and tone output for the operator. In the event that verification feedback is not desired, the CTS/ and DR/ inputs can be hard wired. Bit 7 will be determined by the parity bit written in the command byte. If the BCP was configured with "no parity," then the eighth bit (bit 7) of both the status and checksum will be set to 1. Data characters will have bit 7 cleared to 0. If parity was selected, all characters transmitted will have parity in bit 7. Standard mode is selected by writing a 0 to the communications mode bit in the command byte.

ASCII MODE

This serial mode is intended for bar code verifiers and other applications requiring a local ASCII display or printer. No status or checksum is transmitted. Straight ASCII data is sent, and the message is followed by a carriage return and line feed (0D 0A HEX). As with the "standard" mode, the parity control bit in the command byte will determine bit 7. If "no parity" is selected, bit 7 will be cleared to 0. ASCII mode is selected by writing a 1 to the communications mode bit in the command byte.

TRANSPARENT ASCII MODE (ASCII Data)

This mode allows the user to pass 7 bit ASCII data from the processor port to the serial port when the BCP is in peripheral mode. Referring to Figure 3, the host processor asserts chip select and WR/, and sends a command byte (bit 7 set to 1) with bits 5 and 6 cleared to 0 (transparent ASCII mode). The interface logic latches the command byte and returns a busy signal to the host, and passes a STB to the BCP prompting it to read the command byte. The BCP will not respond until it is free. If the BCP was in the middle of a transmitting tag data, it will complete the entire transfer including checksum if that mode was selected. The BCP will then interpret the command byte, including baud rate and parity, and complete the handshake by activating the RACK/output. The BCP adds parity to serial data consistent with the command byte. Following transmission of the message(s) the processor should again transmit an appropriate command byte to the BCP to enable bar code reading.



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{TX}	TXD cycle time	1.26	-	ms
t_{RTC}	RTS to CTS	0	-	μs
t_{CTR}	CTS to RTS	5.0	-	μs
t_{RTD}	RTS to TXD	5.0	-	μs
t_{BAUD}	BAUD period	.104 (9600)	3.3 (300)	ms

TIMING DIAGRAM 4. SERIAL COMMUNICATIONS PORT

STATUS REGISTER

The 8301 BCP contains an 8-bit status register with the following format:

STATUS FOR GOOD READ

(Serial and Processor Ports)

Read Bit	Bar Code Type		Tag Message Length				
1	C1	C0	ML4	ML3	ML2	ML1	ML0
7	6	5	4	3	2	1	0

Bar Code Type		
C1	C0	Code
0	0	39
0	1	Int 2/5
1	0	Reserved
1	1	Reserved

Message length ranges from 1 (i.e. 00000) to 32 characters (11111).

Error Codes and Display Messages

Condition	Display Message
Scan Too Fast	〈 〈 〈
Scan Too Slow	〉 〉 〉
No Start Char	* * *
No Stop Char	⌒ ⌒ ⌒
Too Many Char	• • •
Parity Error	# # #

COMMAND REGISTER

The 8301 contains an 8-bit write-only command register with the following format:

Data Out			Parity		Communications Baud Rate		
CTRL	D1	D0	P1	P0	C0	B1	B0
7	6	5	4	3	2	1	0

If MODE is TRUE (high), indicating peripheral mode, the command register would then be written via the data bus. If bit 7 (CTRL) is high, the word is interpreted as a command byte. In stand-alone mode, the command byte is loaded via the command port. In stand-alone mode, bit 7 is ignored.

Specific configuration option codes comprising the command byte are given in the following tables. One start bit and two stop bits are assumed for all serial communication.

Communications Rate		
B1	B0	Baud Rate
0	0	300
0	1	1200
1	0	2400
1	1	9600

Parity Bits		
P1	P0	Parity
0	0	None
0	1	Odd
1	0	None
1	1	Even

DB7 = 0

Communications Mode	
C0	Mode
0	Standard (Status and Checksum)
1	ASCII with CR/LF

Data Output Mode		
D1	D0	Mode
0	0	Transparent
0	1	Serial
1	0	Parallel
1	1	Serial/Parallel

ELECTRICAL REQUIREMENTS

Preliminary
Notice: This is not a final specification. Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units
VCC	Supply Voltage	−0.3	7.0	VDC (To VSS)
VIN	Input Voltage	−0.3	7.0	VDC (To VSS)
TOP	Operating Temperature	0	70	°C
TS	Storage Temperature	−65	150	°C

D.C. CHARACTERISTICS (TA = 0° C to 70° C, VCC = 5V ± 5%)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PD	Power Dissipation	VOH=HI, 25° C			1000	mW
VIH	Input High Voltage	All but X2	2.0		VCC	VDC
VIH	Input High Voltage	X2 Input	4.0		VCC	VDC
VIL	Input Low Voltage		−0.3		0.8	VDC
IIN	Input Leakage (RES/)	VIN=0 to VDD	−10		+10	μADC
VOH	Output High Voltage	IOH= −50 uA	2.4		VCC	VDC
VOL	Output Low Voltage	IOL= 1.6 mA	VSS		0.4	VDC
IOFF	Output Leakage	D0 − D7			10	μADC
CIN	Input Capacitance	Except X1, X2			10.0	pF
CIN	Input Capacitance	X1, X2 Only			50.0	pF
COUT	Output Capacitance	D0 − D7			20.0	pF
RL	Pullup Resistance	Pin 4-11, 23-38	3.0	6.0	11.5	Ohm
ICC	Supply Current	VCC to VSS			180	mADC

A.C. CHARACTERISTICS (TA = 0° C to 70° C, VCC = 5V ± 5%)

Symbol	Parameter	Min	Typ	Max	Units
^tCY	Clock Period (Ext)		250		ns
^tCLA	Clock Active (Ext)	115	125		ns
^tCR	Clock Rise Time		5		ns
^tCF	Clock Fall Time		5		ns
^tRST	Reset Pulse Width	5*			μs
^tSTB	STB, DLF Width	6.5			μs
$^tRACK/$	RACK/ Width	4.0			μs
^tDE	Data Enable			1.0	μs
^tDH	Data Hold Time	0			μs
^tDVAL	DVAL Width	4.0			μs
^tPSU	Peripheral Set-Up			2.5	μs
^tPHR	Peripheral Hold Time	0			μs
^tTX	TXD character cycle	1.26			ms
^tRTC	RTS/ to CTS/	0			μs
^tCTR	CTS/ to RTS	5.0			μs
^tRTD	RTS to TXD	5.0			μs
^tBAUD	BAUD period	0.104 (9600)		3.3 (300)	ms

* After VCC reaches operating range and the clock output (CKO) has stabilized.

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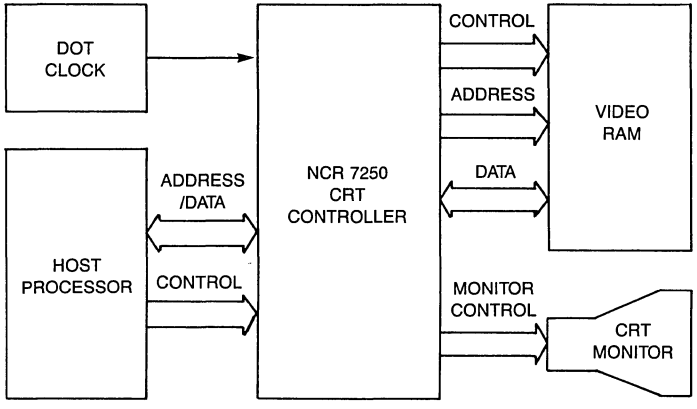
7250
CRT CONTROLLER

- Generates VSYNC, HSYNC, and VIDEO to directly interface with a CRT Monitor
- Eight Screen Functions:
  - —Lines per Page
  - —Screen Blank
  - —Screen Reverse-Video
  - —Video Chop
  - —Split-Screen
  - —Graphics Style
  - —Blank Cursor
  - —Timing Format
- Six Field Functions:
  - —Reverse Video
  - —Highlight
  - —Field Blink
  - —Field Blank
  - —Underline
  - —Graphics Mode
- On-chip character generator (mask programmable) 192 characters standard, up to 256 optional.
- Directly addresses a 2K × 8 Video RAM (VRAM)
- Cursor-address under CPU Control
- Hardware Scrolling for full page or split-screen viewing
- Transparent Refresh for RAM updates at DMA speeds
- Two Timing Formats (including interlace) are available
- Accepts Dot-Clocks up to 20 MHz
- TTL-Compatible signal pins
- Single +5V Power Supply

The NCR 7250 CRT Controller (CRTC) incorporates character generation, video attributes, video timing, RAM interface, and control functions on a single chip. The 7250 provides HSYNC, VSYNC, VIDEO, and HIGHLIGHT (intensity) outputs to directly interface with a raster scan CRT monitor. The character generator produces up to 256 8x12 characters, providing character clarity and variety previously not available in single chip CRT controllers. Features include eight Screen Functions, six Field Functions, hardware scrolling, hardware cursor, and two user-selectable timing formats. The 7250's direct video RAM (VRAM) addressing and transparent refresh permit asynchronous data transfers at DMA speeds without cycle stealing or processor interrupts.

CRTC SYSTEM ENVIRONMENT



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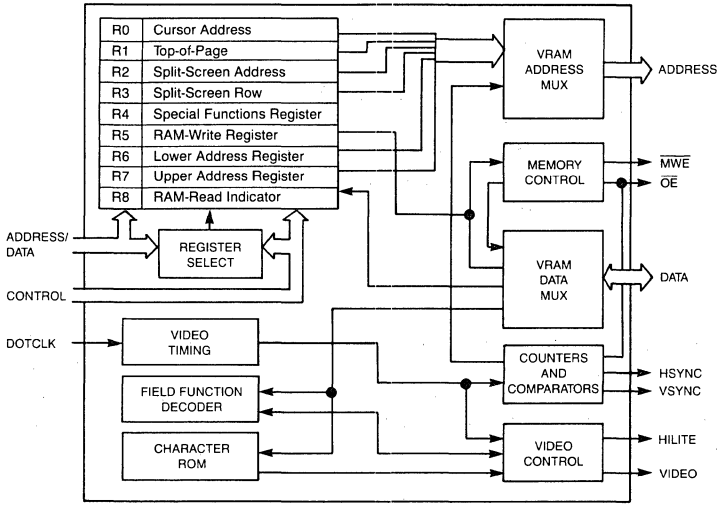
NCR

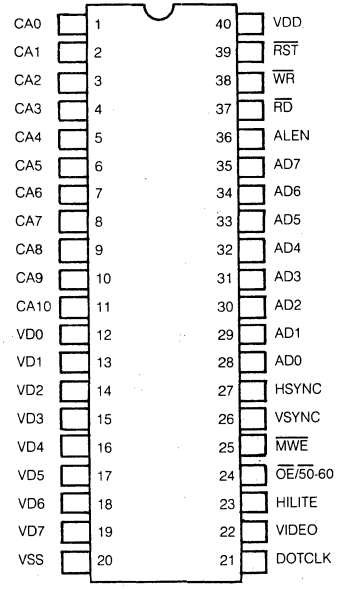
NCR 7250 CRTC ARCHITECTURE

The architecture of the NCR 7250 includes nine software-display control registers, an Address/Data Bus, a VRAM data bus, a VRAM address bus (referred to as the Screen Address Bus), as well as a Character-ROM which holds patterns for 192 characters standard, up to 256 optional.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



CENTRAL PROCESSING UNIT (CPU) INTERFACE

The CPU interface is composed of an 8-bit Address/Data bus (AD0-AD7), nine software display control registers, and three bus control lines ($\overline{RD}$, $\overline{WR}$, ALEN).

At the heart of the CPU interface are the nine software display control registers. These registers enable the CPU to write/read data to the VRAM, position the cursor, vary the size of the split-screen, or select any of the special Screen Functions.

The 8-bit multiplexed Address/Data bus and the three bus controls lines are used by the CPU to designate which of the nine software display control registers is selected. The CPU generates $\overline{RD}$ and $\overline{WR}$ to tell the CRTC that a CPU read or write is occurring. The falling edge of ALEN is used by the CRTC to latch the register address from the address bus. When ALEN is at a low level, the CPU accesses the addressed register. The ability to select the addresses of the display control registers is a mask option.

PIN DESCRIPTION

Pin Name	Pin #	I/O	Description
AD0	28	I/O	Address/Data Bus—Bidirectional bus for interfacing to a multiplexed Address/Data Bus. Used to program internal registers and transfer data to and from the Video RAM.
AD1	29		
AD2	30		
AD3	31		
AD4	32		
AD5	33		
AD6	34		
AD7	35		
$\overline{RD}$	37	I	Bus Read—Control signal generated by the microprocessor. Indicates a CPU read in progress.
$\overline{WR}$	38	I	Bus Write—Control signal generated by the microprocessor. Indicates a CPU write in progress.
$\overline{RST}$	39	I	Reset—Control signal which resets all registers to their default conditions, holds VIDEO to logic 0, but does not affect the generation of VSYNC or HSYNC.
ALEN	36	I	Address Latch Enable—Control Signal, the falling edge of which latches the register addresses from the Address Bus into the CRT. A low level allows CPU access to the CRTC internal registers.
VIDEO	22	O	Video—Contains the DOT stream for the selected row of alphanumeric characters. This DOT stream is modified by various logic conditions (screen and field functions, blank states) which are activated internally by the CRTC.
HILITE	23	O	Highlight Intensity—Used with external circuitry to generate an alternate video intensity level.
VSYNC	26	O	Vertical Sync—Initiates Vertical retrace in the CRT monitor.
HSYNC	27	O	Horizontal Sync—Initiates Horizontal retrace in the CRT monitor.
VD0	12	I/O	RAM Data Bus—Bidirectional bus upon which data is transferred to and from Video RAM. The data represent alphanumeric characters intended for display on the monitor screen, and Special Field Functions which modify the appearance of the characters which follow.
VD1	13		
VD2	14		
VD3	15		
VD4	16		
VD5	17		
VD6	18		
VD7	19		
CA0	1	O	RAM Address Bus—Addresses the Video RAM. (Referred to as the Screen Address Bus.)
CA1	2		
CA2	3		
CA3	4		
CA4	5		
CA5	6		
CA6	7		
CA7	8		
CA8	9		
CA9	10		
CA10	11		
$\overline{MWE}$	25	O	Write Enable—Control signal which tells the VRAM if a write (low level) or a read (high level) is to be executed.
DOTCLK	21	I	Dot Clock—Generated by an external oscillator circuit whose frequency corresponds to the Video Dot Rate. It is asynchronous with the microprocessor interface signals. All other timing signals are derived from this input.
$\overline{OE}/\overline{50}$-60	24	I/O	When $\overline{RST}$ is active, this pin is an input which tells the CRTC which of the two vertical timing counts to use. If $\overline{RST}$ is inactive, this pin is an output for enabling the Video RAM.
VDD	40		Power Supply— + 5 VDC, most positive voltage connection.
VSS	20		Power Supply—0 VDC logic ground, most negative connection.

SOFTWARE DISPLAY CONTROL REGISTERS

The nine software display control registers of the NCR 7250 are addressable by the system and their addresses are selected by the user. Eight of the registers, (R0 through R7) are write-only, while R8 is read-only. The RESET default value of each register is all zeros. This state is assumed after $\overline{RST}$ goes low.

Because R0, R1, and R2 are 11 bits in length, they cannot be loaded directly from the CPU bus. The Screen Address Registers, R6 and R7, are dual purpose registers. They are used as temporary storage registers when R0, R1, or R2 is loaded and contain the VRAM address during VRAM read and write operations. To load an 11 bit register, the 8 lower bits are loaded into R6 and the three upper bits are loaded into R7. The destination register (R0, R1, or R2) is then addressed and a WR command is issued. This WR command causes the value in R6 and R7 to be transferred to the destination register. The data on the CPU bus at the time of this WR command is not used.

CURSOR ADDRESS REGISTER (R0)

The cursor is positioned by writing the desired address to R0 which is an 11-bit register.

TOP-OF-PAGE REGISTER (R1)

This 11-bit register contains the VRAM address of the character that begins the page in the top left corner of the CRT monitor.

SPLIT-SCREEN (SS) ADDRESS REGISTER (R2)

R2 contains the 11-bit VRAM address of the character which begins the designated screen address row.

SPLIT-SCREEN (SS) ROW REGISTER (R3)

The 6-bit SS Row Register contains the value of the row at which the split-screen address is first accessed.

SPECIAL FUNCTIONS REGISTER (R4)

R4 is an 8-bit register that provides CPU control of the eight Screen Functions.

RAM-WRITE REGISTER (R5)

R5 is an 8-bit register used to transfer data bytes from the CPU to VRAM. The screen address (contents of R6 and R7) increments by one after each VRAM write.

LOWER-SCREEN ADDRESS REGISTER (R6)

This 8-bit register comprises the lower 8-bits of the 11-bit Screen Address Bus. This bus addresses VRAM for CPU transfers. R6 is also used in conjunction with R7 to load Registers R0, R1 and R2.

UPPER-SCREEN ADDRESS REGISTER (R7)

R7 is a 3-bit register containing the upper 3-bits of the 11-bit Screen Address Bus. This bus addresses VRAM for CPU transfers. R7 is also used in conjunction with R6 to load Registers R0, R1 and R2.

RAM-READ REGISTER (R8)

The 8-bit RAM-Read Register is used to transfer data bytes from VRAM back to the CPU. The screen address (contents of R6 and R7) increments by one after each VRAM read.

MEMORY

The NCR 7250 CRTC memory information includes the Video RAM interface and the on-chip Character-ROM.

VIDEO RAM INTERFACE

The NCR 7250-VRAM interface is comprised of the Screen Address Bus (CA0-CA10), the VRAM Data Bus (VD0-VD7), and control signals MWE and OE/50-60. The VRAM is a generic 120ns static 2K x 8 RAM used to store display information. The 7250 incorporates a double speed memory technique which permits a refresh access and a CPU access to occur during the time required to display one character. When CPU data is not being written, the CPU access time is used to update the VRAM read register R8 using the VRAM location specified by R6 and R7. If R8 is addressed by the CPU and a RD command issued, the value of R8 will be transferred onto the AD bus and be valid within 120ns. In writing CPU data, CPU data transfers to R5 (RAM Write Register) are asynchronous with respect to VRAM accesses. In order to resolve the possibility of invalid data transfer if a VRAM write is initiated at the end of a VRAM access time, two access times are reserved for the write operation and data is written at both times. At the end of the second VRAM access, indicated by the second pulse edge of $\overline{MWE}$, the Screen Address Register (R6 and R7) increments to the next VRAM location. In order to allow sufficient time for the VRAM write process to occur, a period of 24 t_{cyc} (dot-clks) is required between CPU WR commands. This translates into data transfer rates in excess of 500K bytes/sec for VRAM when using a standard dot-clk frequency of 17.6MHz.

CHARACTER-READ ONLY MEMORY (CHARACTER-ROM)

The on-chip Character-ROM contains dot patterns to generate text, holding patterns for up to 256 alphanumerics. A standard 192 character set is provided in the ROM of each NCR 7250 CRTC. Mask options available for customized character sets are covered under Character Set Options.

NCR

EXTERNAL CLOCK (DOTCLK)

DOTCLK is generated by an external clock generator. The NCR 7250 CRTC accepts Dot-Clocks up to 20 MHz. This Dot Clock provides the basic unit of timing for displaying information on the screen.

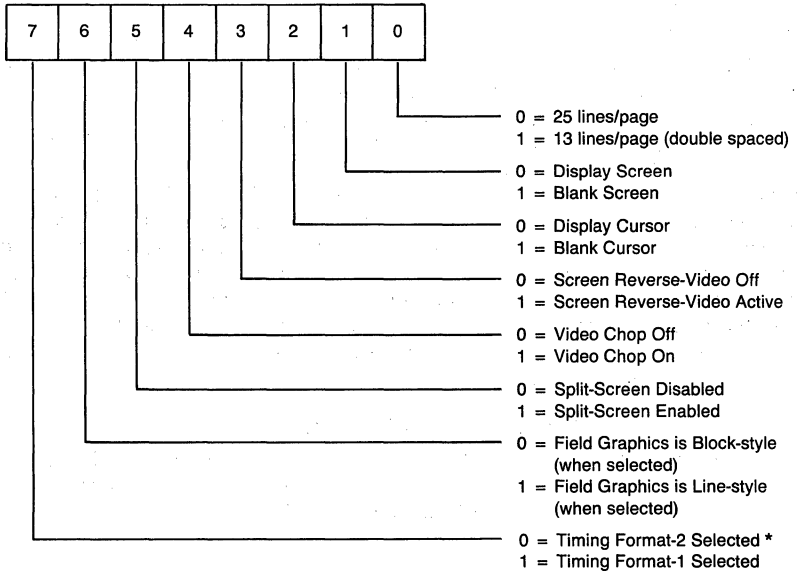
SOFTWARE FUNCTIONS

NCR 7250 CRTC software functions include eight Screen Functions and six Field Functions.

SCREEN FUNCTIONS

The Screen Functions available on the NCR 7250 CRTC are enabled/disabled by CPU command to the Special Functions Register (R4). Changes in R4 are not synchronized with video timing and appear on the screen at the time they are written.

SCREEN FUNCTION BIT ASSIGNMENTS



* The standard 7250 uses the Logic Level on pin 24 during RST to select the timing format. Timing format selection from the special functions register is available as a mask option.

FIELD FUNCTIONS

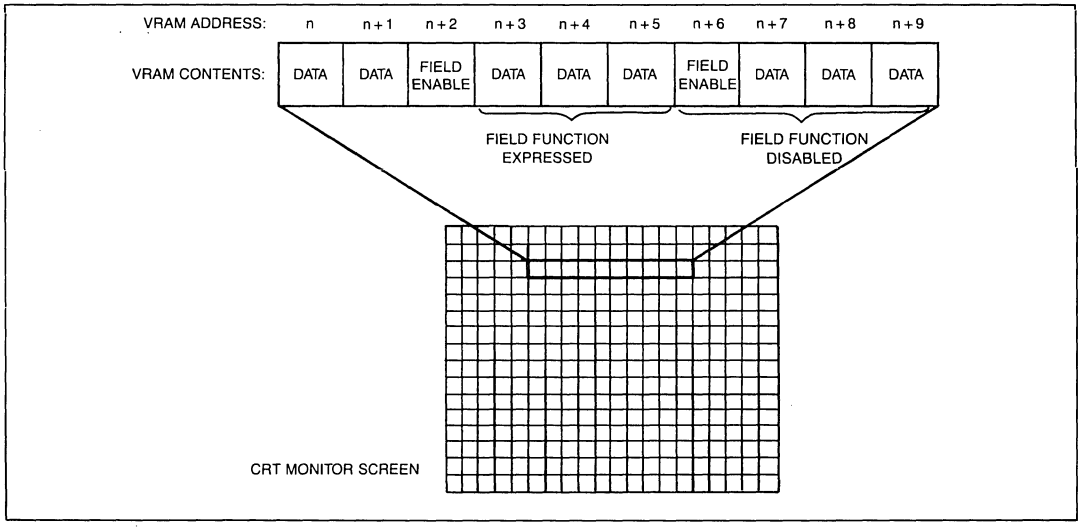
Field functions are selected by "control-bytes" which are loaded into VRAM along with display data. Bytes from VRAM are decoded by the character generator and by the field function control circuitry. Bytes having a value from 80H to BFH (bits 6 and 7 are 0 and 1 respectively) are detected as control bytes and provide the functions listed below. The corresponding location in the character ROM is coded as a blank. This permits the field function control words to be imbedded in the spaces normally occurring between words.

When a control byte is read in during the display process, the attributes selected are handled in three ways. For attributes which are deselected (a 0 in the the corresponding bit position), the attribute is turned off immediately and does not appear in the space occupied by the control byte. For attributes which are newly selected, the attribute will appear in the character position following the space occupied by the control byte. For attributes which were previously selected and again selected by the present control byte, that attribute will appear in a continuous manner, being displayed in the space occupied by the control byte.

FIELD FUNCTION BIT ASSIGNMENTS

Bit	Function
0	0 = Normal, No Reverse Video 1 = Reverse Video with Respect to Screen
1	0 = Normal, No Highlight 1 = Highlight Field with Respect to Screen Intensity
2	0 = Normal, Display Characters 1 = Initiate Field Blank
3	0 = Normal, No Blink 1 = Blink Character Field
4	0 = Normal, No Underline 1 = Underline All Characters within Field
5	0 = Bytes Interpreted as Characters 1 = Bytes Interpreted as Graphics-cells
6	Always 0
7	Always 1

FIELD FUNCTION ENABLED/EXPRESSED/DISABLED EXAMPLE



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GRAPHICS MODE FEATURES

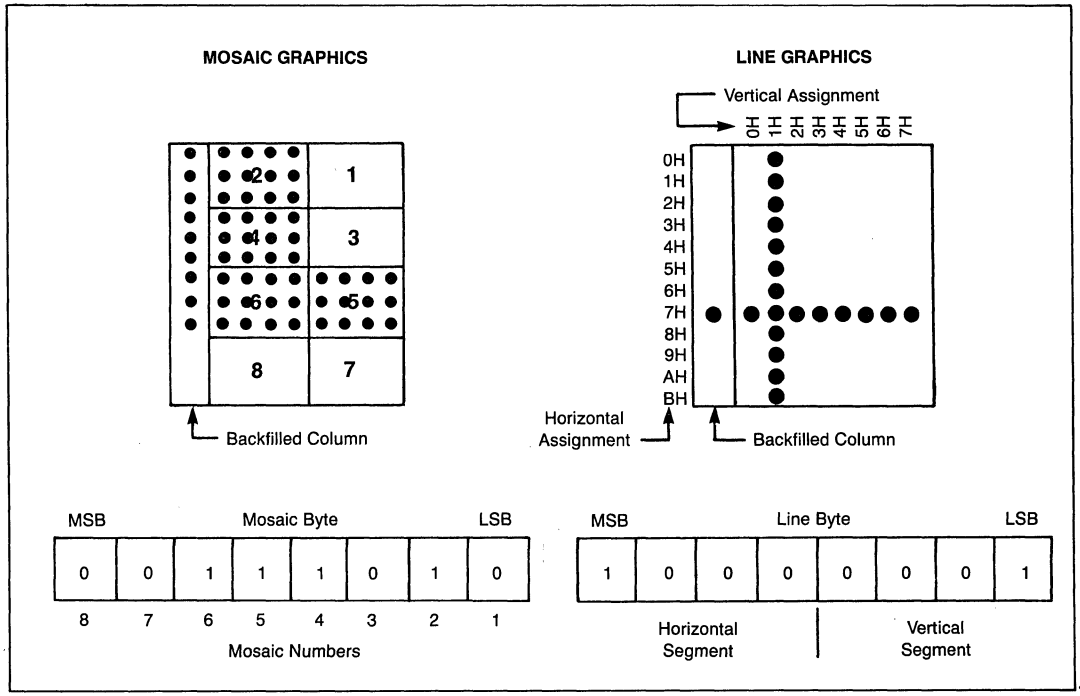
The Graphics capability of the CRTC is a special feature whereby the data bytes coming to the chip from VRAM cause the on-chip Character-ROM to send out special dot patterns. It allows the user to configure unique bar or line arrangements on the CRT monitor.

The Graphics Mode is selected by the Field Function logic. The user may choose one of two graphics styles: block or line. The graphics styles are selected via Bit 6 of the Special Functions Register.

When graphics mode is selected, the attributes selected at that time (blink etc.) are "latched-in" until the graphics mode deselect code is encountered. This permits the display of 255 different codes. The 256th code is reserved as the graphics mode deselect code and cannot be displayed. This code is mask programmable. The default value is C8H. The latching of functions affects only that graphics field. Other graphics field (with different latched attributes) and text with any combination of attributes can be displayed on the same screen.

In line graphics mode, single horizontal or vertical lines are produced by specifying a respective vertical or horizontal value which exceeds the values shown below. Spaces are produced by using values greater than C8H.

EXAMPLES OF BLOCK AND LINE GRAPHICS PATTERNS



MASK OPTIONS
(Available Upon Customer Request)

CHARACTER SET OPTIONS

FIELD FUNCTIONS AND CHARACTER SET SIZE

Because the inclusion of Field Functions means that the corresponding codes in the Character-ROM must be coded as blanks, there are less than 256 characters available to the user. There is a "trade-off" between the number of Field Functions and the size of the character set.

The standard NCR 7250 CRTC is equipped with all six Field Functions. If the user desires less than six functions (i.e., greater than 192 characters), mask options are available that may be changed accordingly.

FIELD FUNCTION/CHARACTER SET RELATIONSHIPS

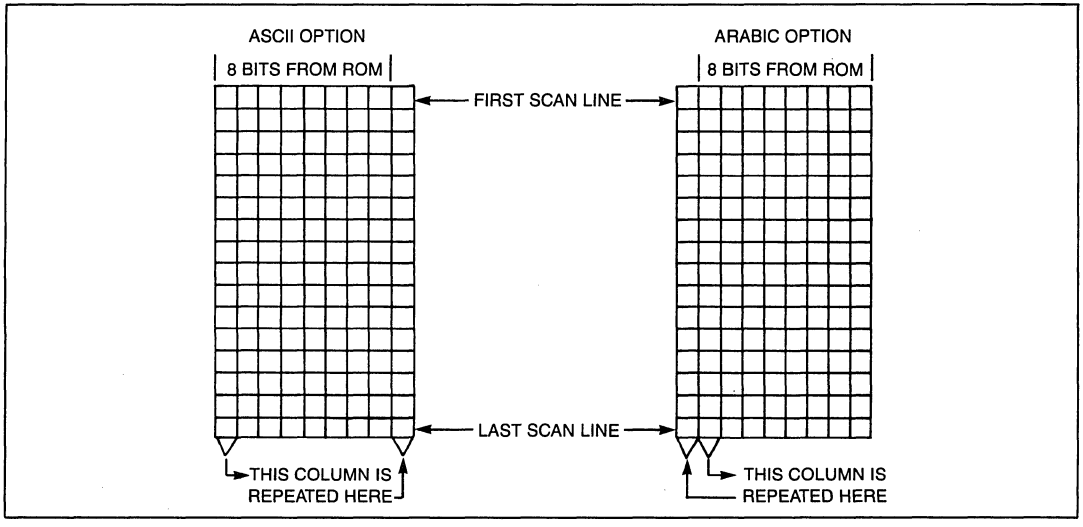
Number of Field Functions	Maximum Character Set Size
4	240
5	224
6	192

CUSTOMIZED CHARACTER SETS AND CHARACTER CODES

Character sets can be customized according to the user's requirements. Any coding for a new character set, however, should take account of the 9th dot derivations described below.

Backfilled Column—Character codes define eight horizontal dots per scan line of a character cell (usually as a hex-byte). The CRTC generates nine dots per scan line in driving the video display. The extra column of dots is derived from the first dot of each character scan line as shown in the following diagrams.

CHARACTER CODE OPTIONS



Note: Characters in a set are displayed under one of the above options only. The user must specify which option to use when a character set is customized.

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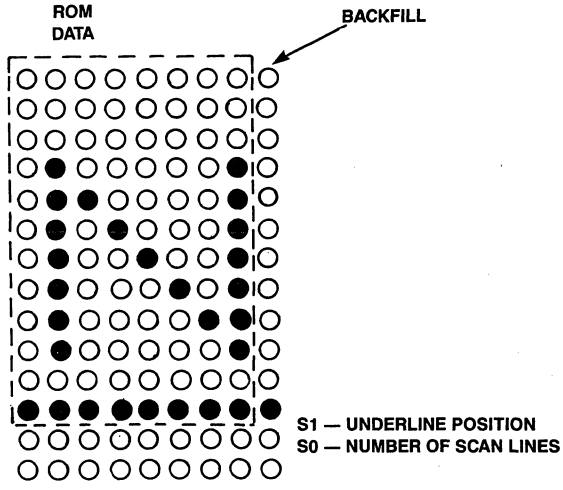
BLINK RATES

The number of frame-times counted in deriving the cursor and field blink rates is also a user-selectable option.

B0	Cursor	Field
1	12.50	3.12
2	6.25	1.56
3	4.17	1.04
4	3.12	0.781
5	2.50	0.625
6	2.08	0.521
7	1.79	0.446
8	1.88	0.469

CHARACTER CELL EXAMPLE

The size of the character cell can be selected by the user and masked into the NCR 7250 CRTC.



NOTE: The number of scan lines comprising a row of characters (16 lines maximum), and the position used for underline (any scan line) are mask programmable. The character generator produces an 8x12 block; backfill provides the 9th dot. In formats using more than 12 scan lines, the additional lines can be used for vertical spacing and underline.

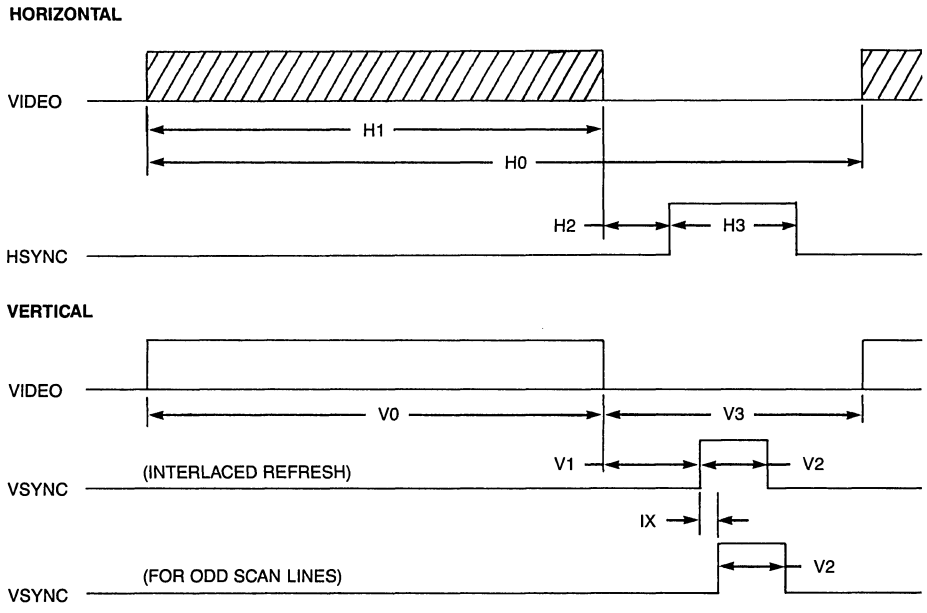
REGISTER OPTIONS

The address of the nine software display control registers are selected by the user and masked into the NCR 7250 CRTC.

GRAPHICS MODE DESELECT OPTION

The Graphics Mode Deselect Code default value may be changed from >C8 to a user-selected value.

MONITOR TIMING DIAGRAM



CRTC MONITOR TIMING

(Mask-Programmable: User selects two sets of the following parameters.)

Symbol	Parameter	Function
H0	Horizontal Scan-time	The duration in characters of a full horizontal period.
H1	Horizontal Character Count	The maximum number of characters that may appear on a displayed row of characters.
H2	Horizontal Front Porch	The delay in character-times between the last displayed row character-position, and the beginning of the HSYNC-pulse.
H3	Horizontal Sync-Width	The duration of the HSYNC-pulse in character-times.
V0	Vertical Row Count	The maximum number of displayed rows of characters.
V1	Vertical Front Porch	The delay in scan-times between the last character-position on the page, and the beginning of VSYNC.
V2	Vertical Sync-Width	The duration of the VSYNC-pulse in scan-times.
V3	Vertical Blank-Time	The duration of the VBLANK condition in scan-times.
S0	Character-Cell Height	The number of scan-lines used for each row of characters.
S1	Character Underline	The scan-line position of the Field Underline within the character cell.
B0	Basic Blink Rate	The number of frame-times counted in deriving the cursor and field blink rates.
IX	Interlace Offset	The number of character-times by which VSYNC (V1) is delayed on alternate frames, interlace modes.

NCR

STANDARD MONITOR TIMINGS

Two timing formats are available in the Standard NCR 7250 CRTC Controller. Neither format is interlaced.

	60 Hz Format	50 Hz Format
H0	918 D[52 uS]	918 D[52 uS]
H1	720 D	720 D
H1	45 d	45 d
H3	81 D [4.6]	81 D [4.6]
V0	300 H	300 H
V1	63 D [.07 H]	29,430 D [32 H]
V2	2,745 D [2.99 H] [156]	3 H
V3	18,567 D [20.2 H] [1024]	77,317 D [84.2 H] [4,383]

NOTE: D = 1 Dot Clock
H = 1 Horizontal Scan Line Time (H0)
[ ] = Time in uS using 17.6 MHz Dot Clock

The following procedure is used to select either the 50 Hz or 60 Hz timing format:

1. Pulse the $\overline{RST}$ (pin 39) low for 10μs.
2. OE (pin 24) is held low to select 50 Hz.
   OE (pin 24) is held high to select 60 Hz.

It is recommended that a 33K ohm resistor be tied to 0 V or +5 V to select the desired timing format.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM STRESS RATINGS

Voltage on any pin with respect to ground (V_{SS}) . . . . . −.03 V to 7.0 V
Power Dissipation . . . . . 840 πW
Operating Temperature Range . . . . . 0°C to 70°C
Storage Temperature Range . . . −65°C to +150°C

The values listed here are absolute maximums which if exceeded could cause permanent damage to the device. All voltages are with respect to circuit ground.

ELECTRICAL CHARACTERISTICS

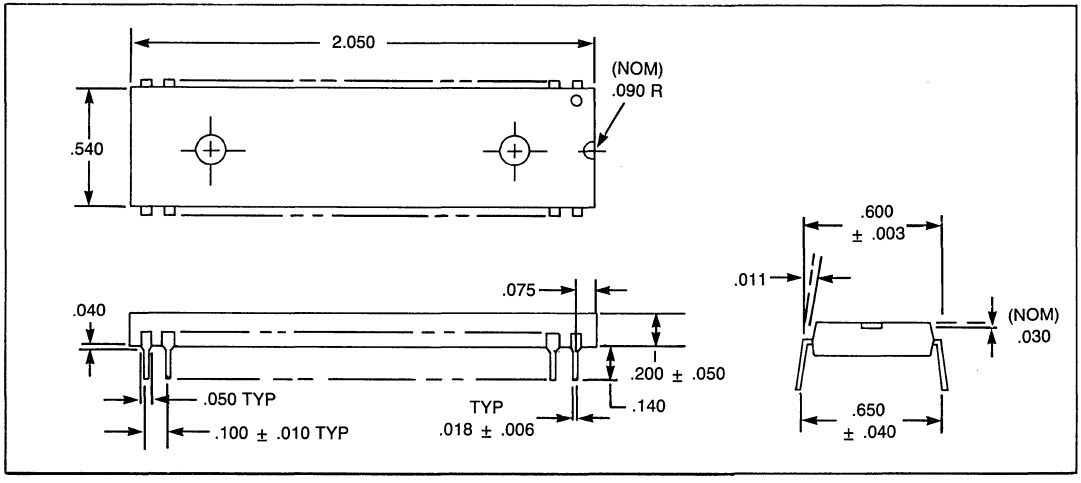
DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
V_{IL}	Input Voltage, Low	V_{SS}−0.3	0.8	V
V_{IH}	Input Voltage, High	2.0	V_{DD}	V
I_I	Input Leakage Current (V_{IN} = 0 to V_{DD})		±2.5	μA
V_{IL}CLK	Clock Input Voltage Low	V_{SS}-0.3	0.4	V
V_{IH}CLK	Clock Input Voltage High	2.4	V_{DD}	V
V_{OH}	Output Voltage, High (I_{OH} = −50μA)	2.7		V
V_{OL}	Output Voltage, Low (I_{OL} = 2 mA)		0.5	V
I_Z	Hi-Z Leakage Current (V_A = 0.4 to 2.4 V)	−10	+10	μA
I_{DD}	Power Supply Current (V_{DD} = 5.5 V)		120	mA

Note: All parameters shall be assured over the 0°C to 70°C temperature range and with $4.75 \leq V_{DD} \leq 5.25$V. Logic "1" is defined as the more positive voltage (V_{IH}, V_{OH}). Logic "0" is defined as the more negative voltage (V_{IL}, V_{OL}). All voltages are with respect to ground (V_{SS}).

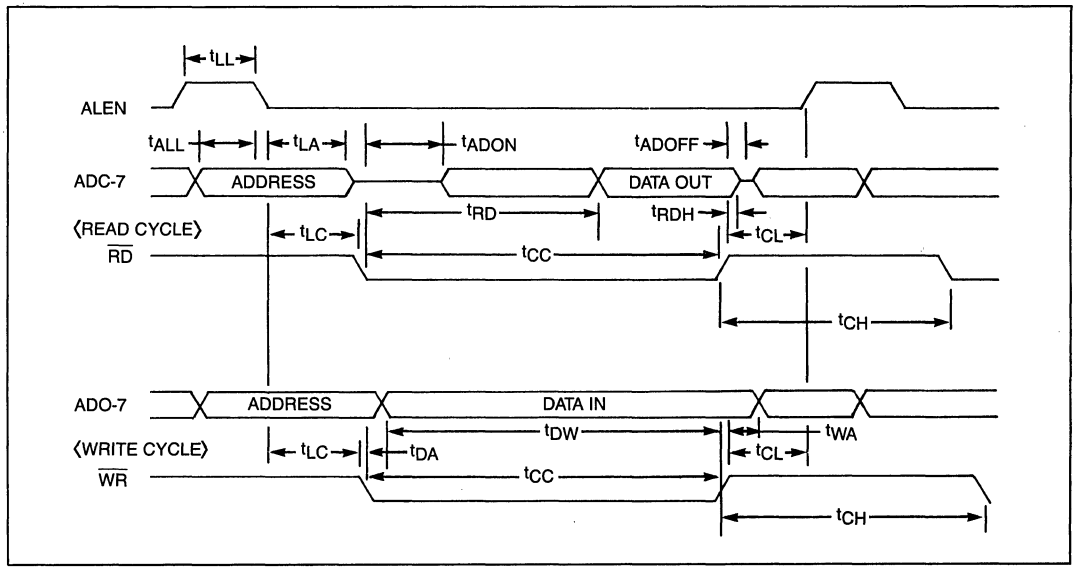
MECHANICAL DATA 40 PIN

PLASTIC DEVICES



MEMORY INTERFACE AND TIMING

PROCESSOR TIMING DIAGRAM



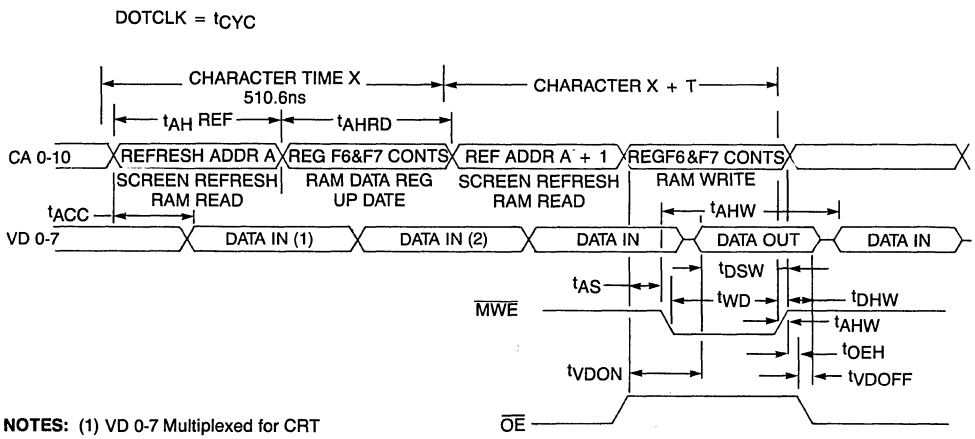
PROCESSOR BUS TIMINGS

Mnemonic	Parameter	Min	Max	Units
t_{LL}	ALEN Width	100		ns
t_{ALL}	Address Valid before ALEN	60		ns
t_{LA}	Address Hold after ALEN	60		ns
t_{LC}	ALEN to Control ($\overline{RD}$, $\overline{WR}$)	140		ns
t_{CC}	Control Width, ($\overline{RD}$, $\overline{WR}$)	350		ns
t_{RD}	Active RD to Valid Data		120	ns
t_{RDH}	Data Hold from $\overline{RD}$	0		ns
t_{CL}	Control ($\overline{RD}$, $\overline{WR}$) to ALEN	60		ns
t_{DW}	Data Valid Before $\overline{WR}$	300		ns
t_{WA}	Data Hold From $\overline{WR}$	55		ns
t_{DA}	Data Valid After $\overline{WR}$		100	ns
t_{ADON}	Address/Data Non-tri-state after $\overline{RD}$	50		ns
t_{ADOFF}	Address/Data tri-state	40	70	ns
t_{CH}	Time between active pulses	24 Dot Clocks - t_{CC}		ns

VRAM INTERFACE CHARACTERISTICS

In the VRAM timing diagram below, note that the second portion of a character-time is used to read VRAM data into the RAM-read register, unless a write command is issued. These CPU accesses (read or write) take place at the address contained in the Screen Address Register. No refresh VRAM accesses occur during blank times.

VRAM TIMING DIAGRAM



NOTES: (1) VD 0-7 Multiplexed for CRT
(2) VD 0-7 Multiplexed for F5 Data Register

Last portion of character time will always be used to continuously read data in the Video RAM into the RAM Data Register unless it is used as a write. The data read or write is at the RAM location specified in Address Register F6 and F7. Screen refresh RAM accesses do not occur during blank times.

VRAM INTERFACE TIMINGS

Symbol	Parameter	Min	Max	Units
t_{AHREF}	Valid Refresh Address Time	4(t_{CYC})	4(t_{CYC})	ns
t_{AHRD}	Valid Current Screen Address Time	5(t_{CYC})	5(t_{CYC})	ns
t_{ACC}	Valid Refresh Address to Valid Data In		150	ns
t_{AHW}	Current Screen Address Hold Time After $\overline{MWE}$	0		ns
t_{AS}	Current Screen Address Setup Time to $\overline{MWE}$	20		ns
t_{VDON}	Video Data Nontri-state from $\overline{OE}$	40		ns
t_{VDOFF}	Video Data Tri-State After $\overline{OE}$		5	ns
t_{DSW}	Valid Video Data Out Before $\overline{MWE}$	50		ns
t_{DHW}	Video Data Out Hold Time from $\overline{MWE}$	5		ns
t_{WD}	$\overline{MWE}$ Width	100		ns
t_{OEH}	OE Hold from $\overline{MWE}$	5		ns

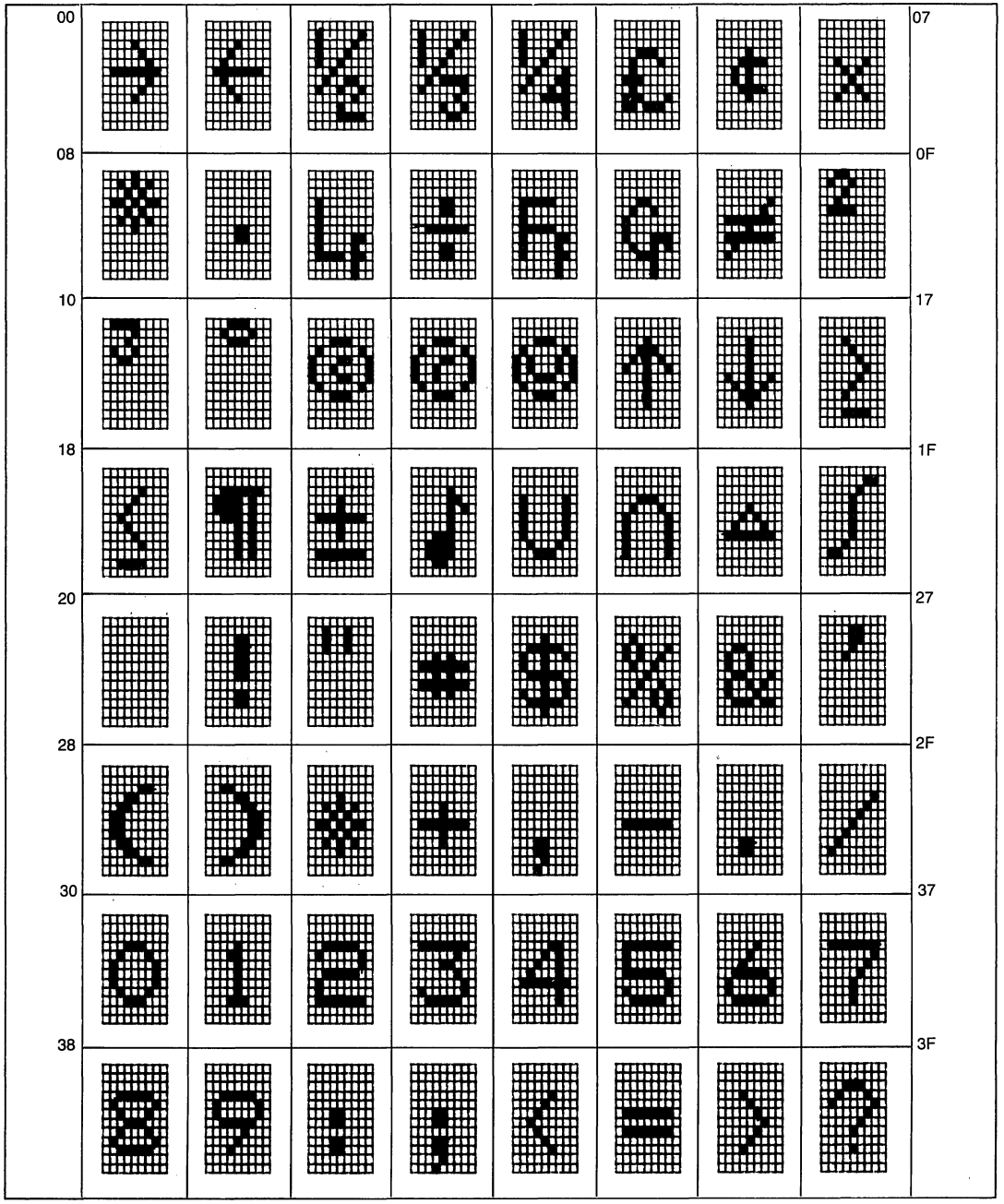
DOTCLK TIMINGS

Symbol	Parameter	Min	Max	Units
t_{CYC}	DOTCLK Period	50	75	ns
	DOTCLK Duty Cycle	45	55	%
t_{DKR}	DOTCLK Rise Time		10	ns
t_{DKF}	DOTCLK Fall Time		10	ns

NCR 7250 CRTC REGISTERS

Name	Address	Length	Function
Cursor Address	F0	11 Bits	Contains the VRAM Address of that character which exhibits the cursor.
Top of Page	F1	11 Bits	Contains the VRAM Address of that character which begins the page (i.e. top left corner).
Split Screen Address	F2	11 Bits	Contains the VRAM Address of the character that begins the designated split screen row.
Split Screen Row	F3	6 Bits	Contains the value of vertical counter at which the split screen address is first accessed.
Special Functions	F4	8 Bits	The bits of this register enable various attributes which affect the entire displayed screen.
Ram Write, Ram Read	F5	8 Bits	These two registers transfer bytes between the CPU and the VRAM. They are distinguished by pulsing either the $\overline{WR}$ or the $\overline{RD}$ pins.
Lower Screen Address	F6	8 Bits	This is the lower portion (stores LSB's) of the full Screen Address Register. It directly addresses the VRAM for CPU transfers.
Upper Screen Address	F7	3 Bits	This register contains the upper 3-bits of the Screen Address Register.

STANDARD CHARACTER SET



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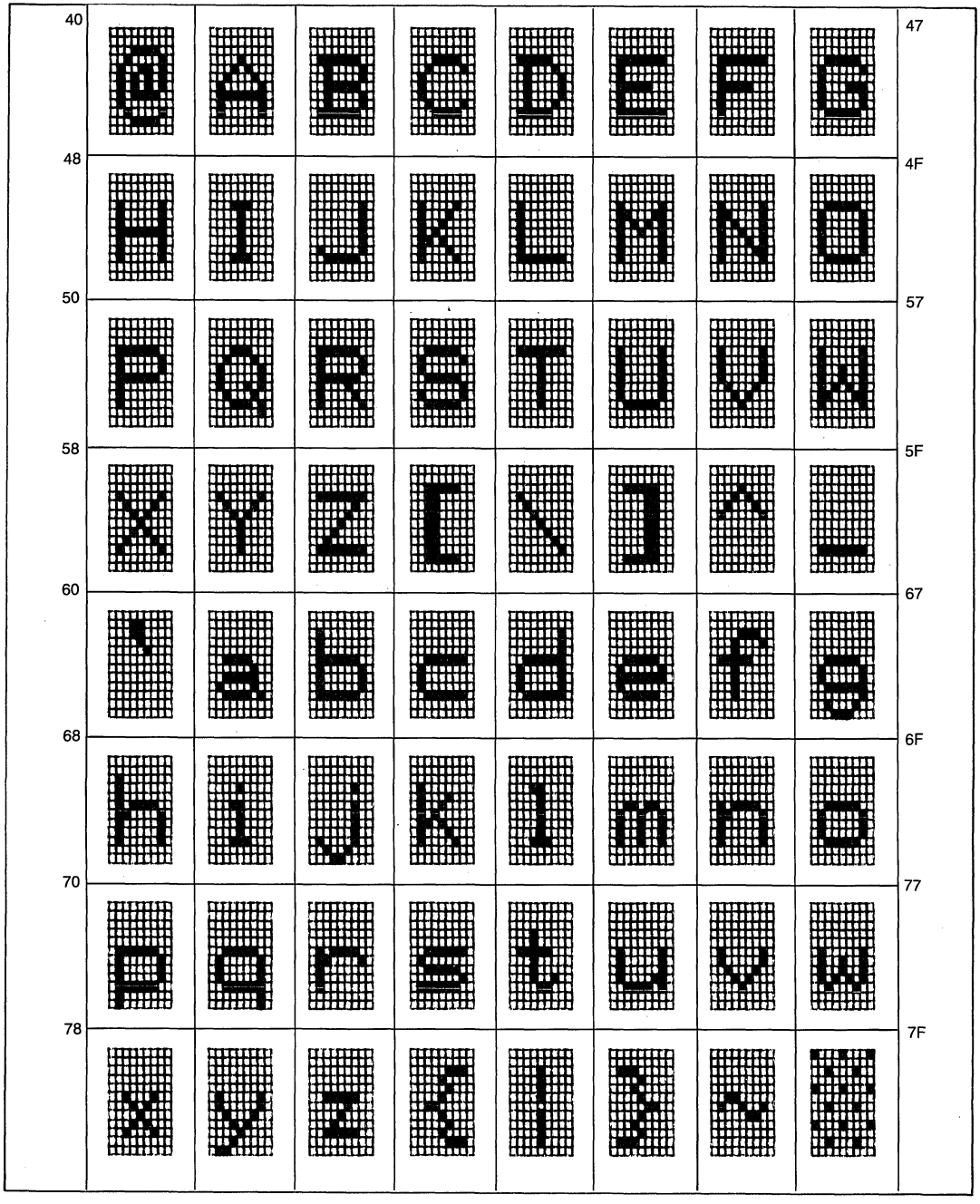
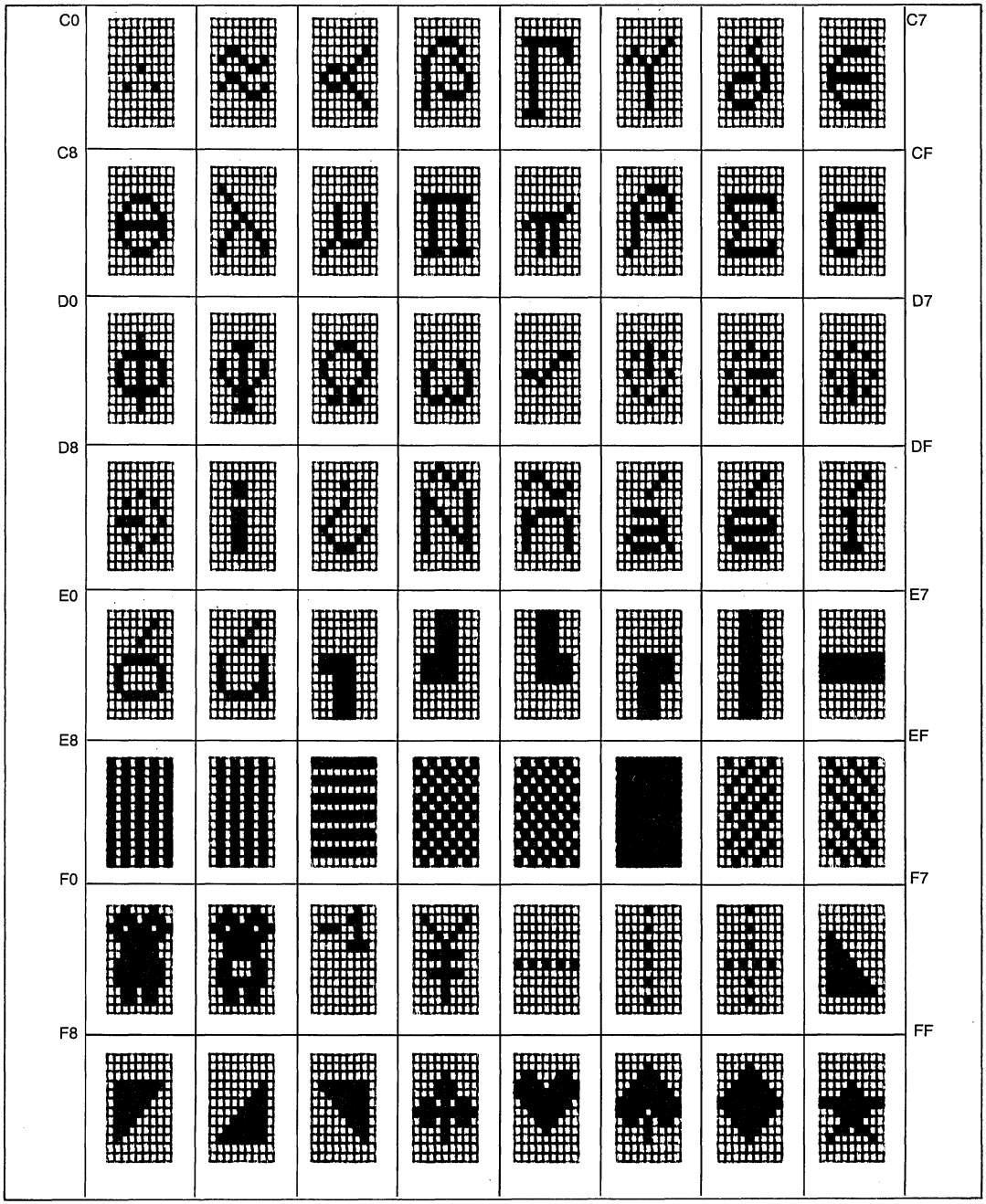
CHARACTER ADDRESS



CHARACTER ADDRESS



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Colorado Springs, Colorado 80916
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Phone: 303/596-5612
800/525-2252

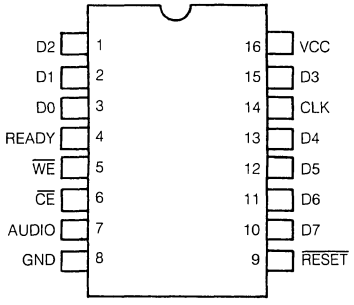
8489
SOUND GENERATOR

PRELIMINARY

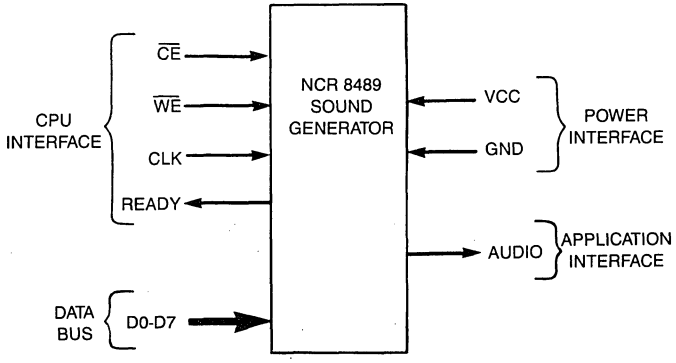
- **Functionally and Pin compatible with the SN76489A**
- **Programmable white or periodic noise generator**
- **Three programmable tone generators**
- **Programmable attenuation values**
- **Simultaneous multiple sound generation**
- **TTL compatible**
- **4 MHZ maximum clock input**

The NCR 8489 is an NMOS digital sound generator capable of providing applications wth a low cost solution for noise and sound generation.

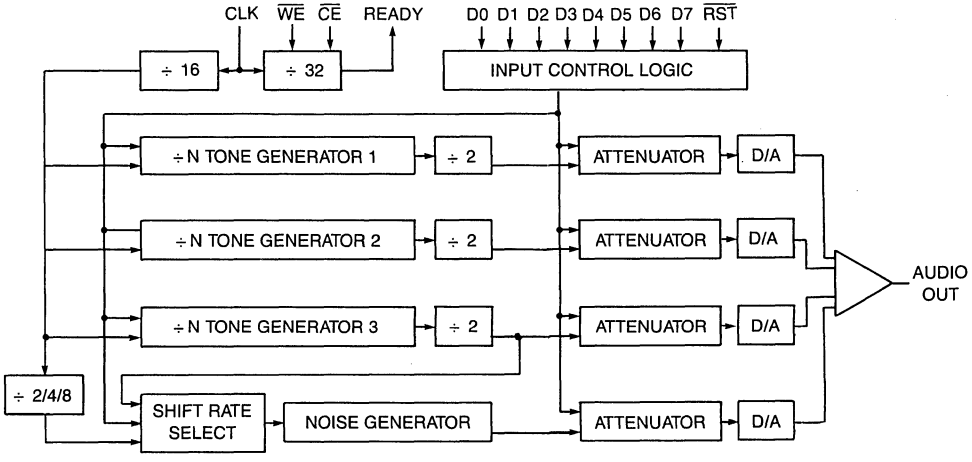
PIN CONFIGURATION



FUNCTIONAL PIN GROUPING



FUNCTIONAL BLOCK DIAGRAM



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CONTROL REGISTERS

The NCR 8489 Sound Generator has eight (8) internal registers used to control three (3) tone generators and one (1) noise generator. A three (3) bit data word used to determine the destination control register is contained in the first byte of data for all data transfers. The internal register designations are as follows:

ADDRESS BITS			REGISTER DESTINATION
R2	R1	R0	Description
0	0	0	Tone 1: Frequency
1	0	0	Tone 1: Attenuation
0	1	0	Tone 2: Frequency
1	1	0	Tone 2: Attenuation
0	0	1	Tone 3: Frequency
1	0	1	Tone 3: Attenuation
0	1	1	Noise: Control
1	1	1	Noise: Attenuation

NOTE: R0 is the most significant address bit

TONE GENERATION

The NCR 8489 sound generator has three (3) programmable tone generators, each with separate frequency synthesis and attenuation sections. The frequency synthesis section requires ten (10) bits of data (F0 to F9) to define half the period of the desired frequency. This data is entered into a ten (10) stage tone counter, which is decremented at a rate of N/16 where N is the clock input frequency. A signal is produced when this tone counter decrements to one, which toggles a divide by two counter and reloads the tone counter. Therefore, the period of the desired frequency is twice the value of the tone generator.

The frequency of each tone generation is calculated using the equation:

$$f = N(32 \times n)$$

N = the clock input frequency

n = a 10 bit binary number [$2 \leq n \leq 1023$]

The divide by two counter is directly connected to a four stage attenuator whose values and bit position in the data word are shown in the following table:

ATTENUATION CONTROL

DATA				VALUE
A3	A2	A1	A0	dB
0	0	0	0	0
1	0	0	0	-2
0	1	0	0	-4
1	1	0	0	-6
0	0	1	0	-8
1	0	1	0	-10
0	1	1	0	-12
1	1	1	0	-14

DATA				VALUE
A3	A2	A1	A0	dB
0	0	0	1	-16
1	0	0	1	-18
0	1	0	1	-20
1	1	0	1	-22
0	0	1	1	-24
1	0	1	1	-26
0	1	1	1	-28
1	1	1	1	OFF

NOTE: A0 is the most significant bit of data

NOISE GENERATION

The NCR 8489 Sound Generator has two (2) noise sources (periodic and white), which share a common attenuator. These noise sources are shift registers with an exclusive NOR feedback network. One (1) of four (4) noise generator shift rates, each rate being derived from the input clock, will be controlled by the two (2) NF bits, as is shown in the Noise Generator Frequency Control Table.

The choice of either periodic or white noise is controlled by the noise feedback control bit FB.

NOISE GENERATOR FREQUENCY CONTROL

NF BITS		FREQUENCY CONTROL
NF1	NF0	Shift Rate
0	0	N/512
1	0	N/1024
0	1	N/2048
1	1	Tone Generator #3 Output

NOTE: NF0 is the least significant bit

NOISE FEEDBACK CONTROL

FB	CONFIGURATION
0	Periodic Noise
1	White Noise

DATA TRANSFER

The NCR 8489 Sound Generator is enabled by the CPU by asserting a low logic level to $\overline{CE}$. $\overline{WE}$ strobes the contents of the data bus to the appropriate control register. Data bus contents must be valid at this time. Data transfers cannot occur unless $\overline{CE}$ is true.

Thirty two (32) clock cycles are required by the NCR 8489 to load data into the control register. The READY output, used as a handshake signal to synchronize the CPU, is asserted to a low logic level immediately following the leading edge of $\overline{CE}$. READY assumes a true state via an external pull up resistor once the data transfer has been completed.

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FORMATS FOR DATA TRANSFER

FREQUENCY UPDATE (DOUBLE BYTE TRANSFER)

FIRST BYTE		
Data	**Register Address**	**Bit 0**
F9 F8 F7 F6	R2 R1 R0	1
D7		D0

SECOND BYTE	
Data	**Bit 0**
F5 F4 F3 F2 F1 F0 X	0
D7	D0

NOISE SOURCE UPDATE (SINGLE BYTE TRANSFER)

Shift Rate	Feedback		Register Address	Bit 0
NF1 NF0	FB	X	R2 R1 R0	1
D7				D0

ATTENUATOR UPDATE (SINGLE BYTE TRANSFER)

Data	Register Address	Bit 0
A3 A2 A1 A0	R2 R1 R0	1
D7		D0

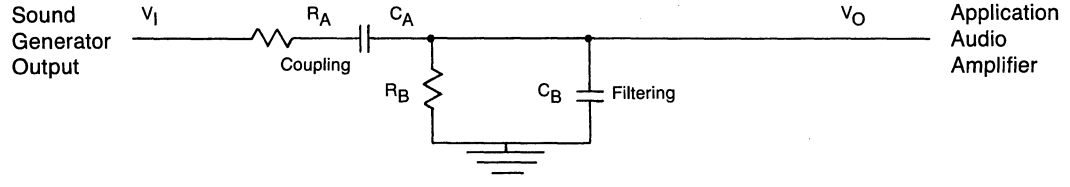
CPU INTERFACE

Eight (8) data lines (D0-D7) and three (3) control lines ($\overline{WE}$, $\overline{CE}$, READY) interface the NCR 8489 Sound Generator to the CPU. Ten (10) bits of data are required by each tone generator in selecting frequency values. Frequency updates require double byte data transfers. An additional four (4) bits of data are required to select the attenuation values. Attenuation updates require only single byte data transfers.

Tone generators can be quickly updated by initially sending both bytes of frequency and register data. This data is followed by the second byte of data for succeeding values only if no other control registers are accessed at the time of generator updating. This action is accomplished by latching the register address and permitting the continued transfer of data into the same register. This updating feature permits the expedited modification of the six (6) most significant bits of data needed for frequency sweeps.

OUTPUT CIRCUITRY

The NCR 8489 Sound Generator output circuitry, emulating a conventional op amp summing circuit, sums the three (3) tone and one (1) noise generator outputs, and will source/sink current to 2 mA. The 0 dB output signal per generator is nominally a 450 mV square wave in the negative direction from a 2V quiescent level. The output should be capacitatively coupled into the application audio circuit via a filtering network similar to the following:



The UPPER and lower frequency poles for the application are determined from the following equations:

Lower Pole

$$f \cong \frac{1}{2\pi(R_A + R_B)\,C_A}$$

Upper Pole

$$f \cong \frac{1}{2\pi(R_A // R_B)\,C_B} \quad \text{if: } R_B >> R_A,\ C_A >> C_B$$

Attenuation of the output signal is:

$$\frac{V_O}{V_I} = \frac{R_B}{R_A + R_B}$$

Typically $R_B \geq 10\ R_A$ so that the attenuation can be small while achieving desired filtering.

INTERFACE DEFINITIONS

MICROPROCESSOR INTERFACE

Signal	Pin	Description
READY	4	OUTPUT: Open collector. READY indicates that data has been read when true (high). Data, $\overline{WR}$, $\overline{CS}$ must remain stable while ready is false (low).
$\overline{WE}$	5	INPUT: Write Enable $\overline{WE}$ indicates that data is available to the NCR 8489 when true (low).
$\overline{CE}$	6	INPUT: Chip Enable $\overline{CE}$ indicates that data may be transferred to the NCR 8489.
$\overline{RST}$	9	INPUT: Master Reset $\overline{RST}$ is used for testing purposes only. This pin is a no connect on the SN 76489A and is internally pulled high.
D7	10	INPUTS: D0-D7 is the data bus through which data is transferred. D0 is the most significant data bit. D7 is the least significant data bit.
D6	11	
D5	12	
D4	13	
D3	15	
D2	1	
D1	2	
D0	3	
CLK	14	Input Clock

AUDIO APPLICATION INTERFACE

Signal	Pin	Description
Audio	7	OUTPUT: Audio signal to application. Refer to Output Circuitry for recommended output connections.

POWER INTERFACE

Signal	Pin	Description
VCC	16	Supply Voltage
GND	8	Ground References

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ELECTRICAL CHARACTERISTICS

OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Supply Voltage		4.5	5.5	V
I_{CC}	Supply Current	Outputs Open		40	mA
T_O	Operating Temperature		0	+70	°C
T_S	Storage Temperature		−65	+150	°C
V_{max}	Absolute Maximum	To Any Pin		7.0	V

INPUT CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Max	Units
V_{IL}	Input Voltage Low	D0-D7, $\overline{WE}$, $\overline{CE}$, CLK		0.8	V
V_{IH}	Input Voltage High	D0-D7, $\overline{WE}$, $\overline{CE}$, CLK	2.0		V
I_I	Input Current	V_{in} = GND→V_{CC}	−10	+10	μA
C_I	Input Capacitance			15	pf

OUTPUT CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Max	Units
V_{OL}	Output Voltage Low	*(READY) I_{OUT} = −2mA		0.4	V

AUDIO CHARACTERISTICS

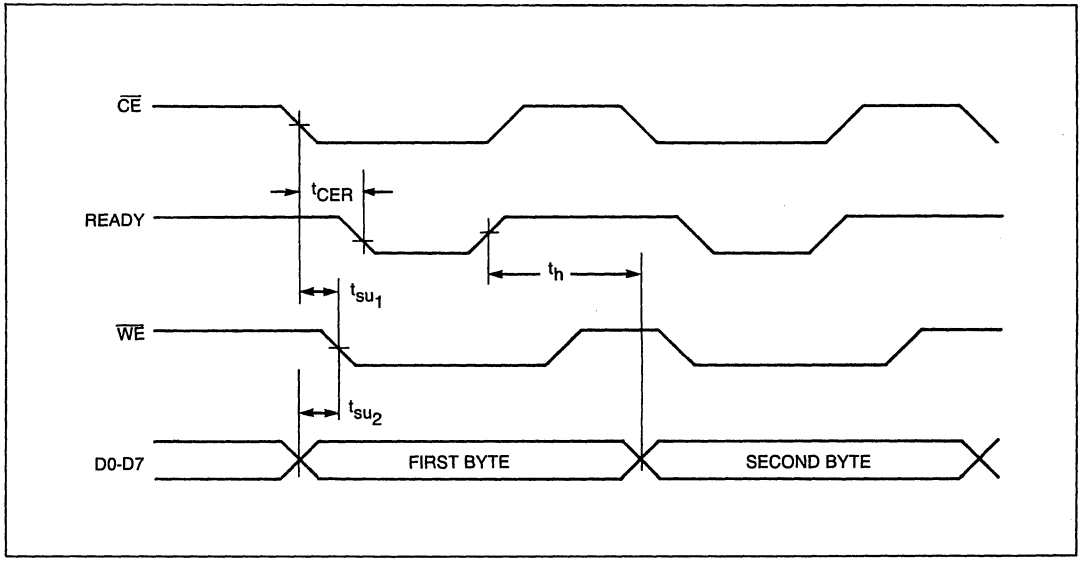
Symbol	Parameter	Conditions	Typ	Max	Units
I_{SO}	Source Current	Over Output Voltage Swing		−3	mA
I_{SO}	Sink Current	Over Output Voltage Swing		2	mA
V_{OQ}	Quiescent Output		2.1		V
V_{OM}	Maximum Output	All Generators at 0dB measured from Peak to Peak	2.0		V
V_{SW}	Signal Swing	One Generator at 0dB measured from Peak to Peak	450		mv
C_{OL}	Capacitance * Loading	From Pin 7 to Ground for Stability		200	pf

* Does not apply to coupling capacitors. It is recommended that capacitors to ground be isolated by a series resistance of 500 ohms for stability.

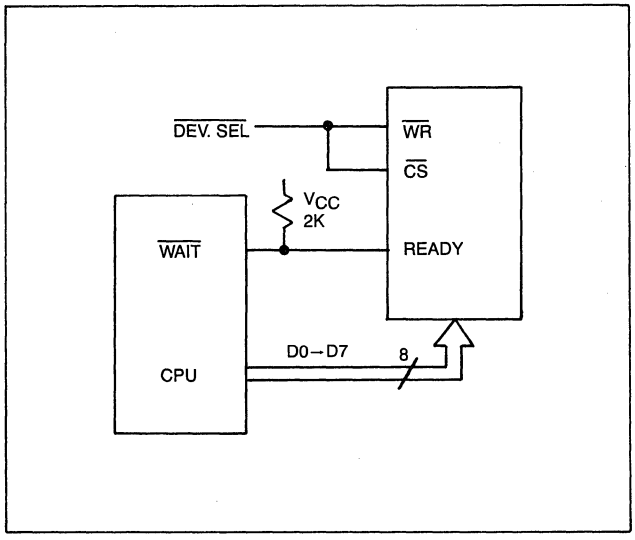
TIMING REQUIREMENTS

Symbol	Parameter	Conditions	Min	Max	Units
t_{CER}	$\overline{CE}$ READY	CL = 225pf RL = 2K to VCC		150	nS
CLOCK	Frequency Input	Transition Time	.05	4	MHZ
t_{su_2}	Set up Time	Data W.R.T. $\overline{WE}$	0		nS
t_{su_1}		$\overline{CE}$ W.R.T. $\overline{WE}$	0		nS
t_h	Hold Time	Data W.R.T. READY	0		nS

DATA TRANSFER TIMING



TYPICAL MICROPROCESSOR INTERFACE SCHEMATIC



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