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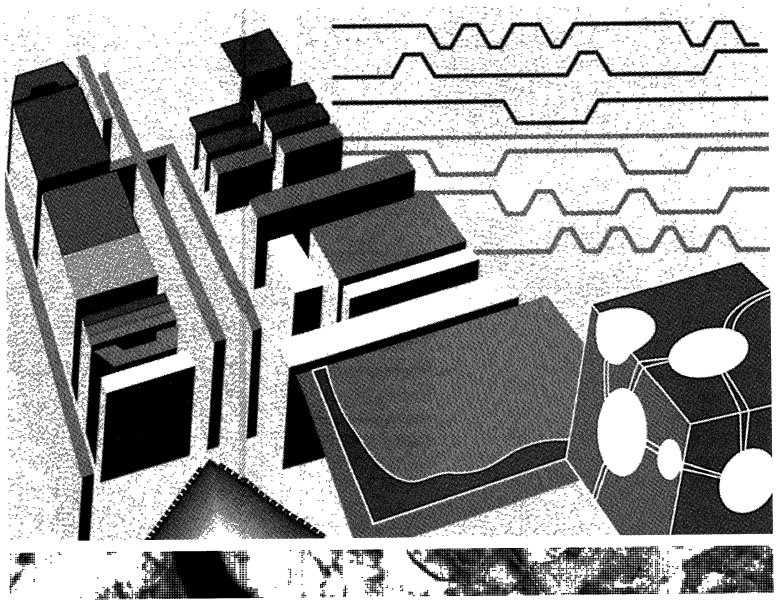


μPD72611 SCSI-2/C Small Computer Systems Interface-2 Controller

Data Sheet

NEC

The uPD72611 is an LSI to control interface protocol of the small computer system interface-2 (SCSI-2). It is compliant with the ANSI X3T9.2/86-109 Rev. 10c. The SCSI-2 controller supports SCSI controller (uPD72111) functions as well as the functions expanded with the SCSI-2 including the high-speed synchronous transfer function and 3-byte message support function by composite commands.

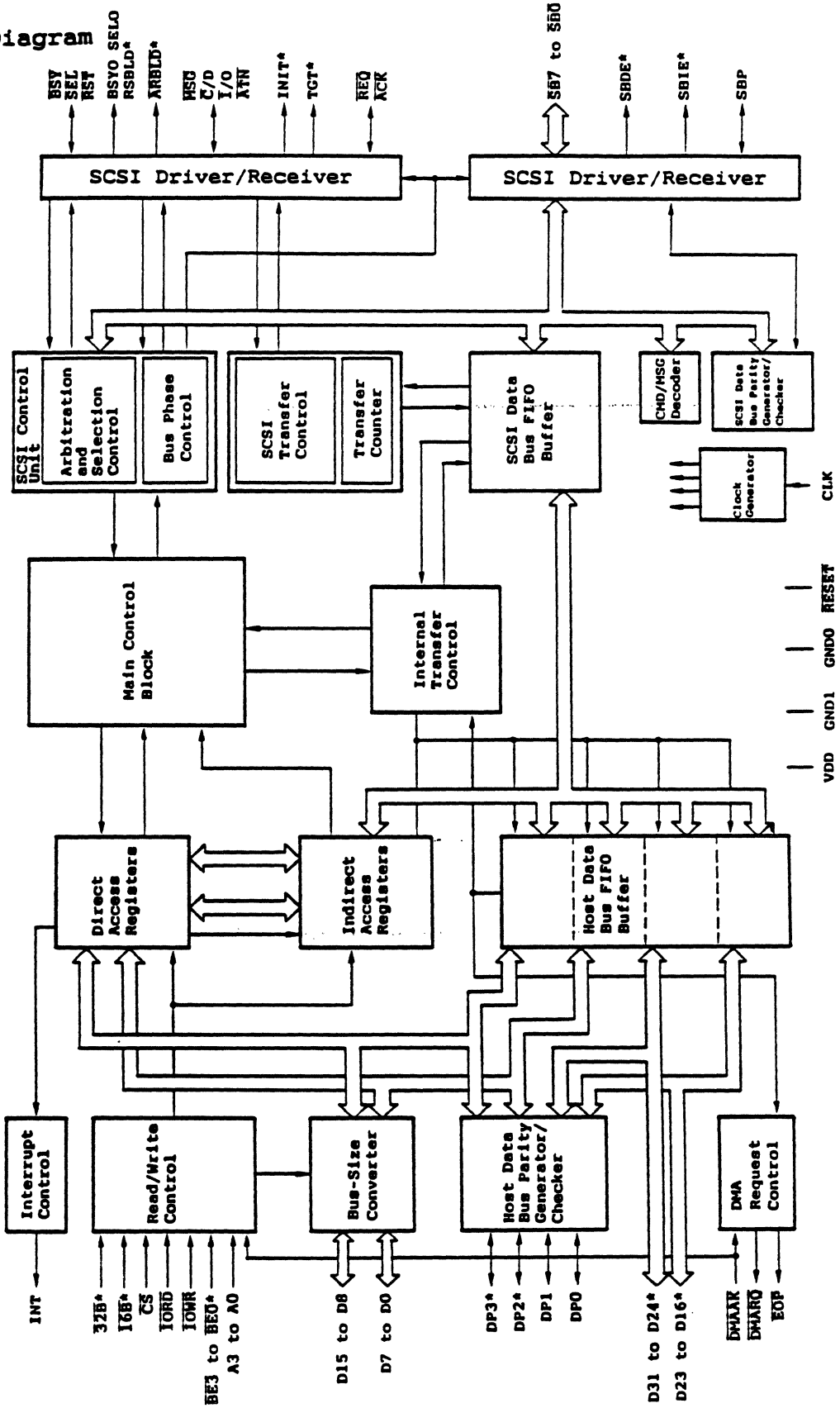
Based on the uPD72111 SCSI controller, the uPD72611 has undergone extensions including an increase of speeds, host side bus width extension and differential driver applications. Thus, the uPD72611 is software upward compatible with the uPD72111.

Features

- o Compliant with ANSI X3T9.2/86-10.9 Rev. 10c (SCSI-2 specifications)
- o System clock: 20 MHz max.
- o Data transfer rate
  - . Asynchronization (5.0M bytes/sec min.)
  - . Synchronization (5.0M bytes/sec max.: Programmable at 7 levels)
  - . High-speed synchronization (10.0M bytes/sec max.: Programmable at 7 levels)
- o Operationable as an initiator and target
- o CPU side bus width can be selected (32-/16-/8-bit)
- o Single-end type SCSI bus driver and Schmitt type receiver are incorporated.
- o External differential driver and receiver are supported.

$\overline{SB0}$ to $\overline{SB7}$	:	SCSI Buses 0 to 7
$\overline{SBP}$	:	SCSI Bus Parity
$\overline{ATN}$	:	Attention
$\overline{ACK}$	:	Acknowledge
$\overline{REQ}$	:	Request
$\overline{MSG}$	:	Message
$\overline{C}$/D	:	Command/Data
$\overline{I}$/O	:	Input/Output
$\overline{BSY}$	:	Busy
$\overline{SEL}$	:	Select
$\overline{RST}$	:	Reset
RSTO	:	Reset Out
BSYO	:	Busy Out
SELO	:	Select Out
IDSTR	:	ID Strobe
INIT	:	Initiator
TGT	:	Target
SBOE	:	SCSI Bus Out Enable
$\overline{SBIE}$	:	SCSI Bus In Enable
INT	:	Interrupt Request
$\overline{IORD}$	:	I/O Read
$\overline{IOWR}$	:	I/O Write
A2 to A3	:	Addresses 2 & 3
A0/$\overline{BE2}$ & A1/$\overline{BE3}$	:	Addresses 0 & 1/Byte Enable 2 & 3
$\overline{BE0}$/$\overline{UBE}$	:	Byte Enable 0/Upper Byte Enable
$\overline{BE1}$	:	Byte Enable 1
$\overline{CS}$	:	Chip Select
D0 to D31	:	Data Buses 0 to 31
DP0 to DP3	:	Data Parity 0 to 3
$\overline{DMARQ}$	:	DMA Request
$\overline{DMAAK}$	:	DMA Acknowledge
$\overline{EOP}$	:	End of Process
$\overline{RESET}$	:	Reset
$\overline{16B}$	:	16-bit Bus
$\overline{32B}$	:	32-bit Bus

Block Diagram



Remarks: Asterisks (*) indicate signals added from the uPD72111.

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CHAPTER 1. PIN FUNCTIONS

The uPD72611 pins are divided into CPU interface pins and SCSI interface pins.

1.1 CPU INTERFACE PINS

Name	Input/ Output	Pin No.	Function
INT	Output	95	Output pin of interrupt request signal to CPU
$\overline{\text{IORD}}$	Input	97	Read signal input pin for CPU to read uPD72611 internal registers
$\overline{\text{IOWR}}$	Input	96	Write signal input pin for CPU to write to uPD72611 internal registers
A2 & A3	Input	4, 3	Address high-order 2-bit input pins. The access target direct register is specified.
A0/$\overline{\text{BE2}}$ & A1/$\overline{\text{BE3}}$	Input	6, 5	. In 32-bit bus mode, . Input pins of signals which indicate the valid bus for data access together with $\overline{\text{BE1}}$ and $\overline{\text{BE0}}$ signals . In 16-/8-bit bus mode, Address low-order 2-bit input pins
$\overline{\text{BE1}}$	Input	7	. In 32-bit bus mode, . Input pin of signals which indicate the valid bus for data access together with $\overline{\text{BE3}}$, $\overline{\text{BE2}}$ and $\overline{\text{BE0}}$ signals
$\overline{\text{BE0}}$/$\overline{\text{UBE}}$	Input	8	. In 32-bit bus mode, . Input pins of signals which indicate the valid bus for data access together with $\overline{\text{BE3}}$, $\overline{\text{BE2}}$ and $\overline{\text{BE1}}$ signals . In 16-bit bus mode, High-order byte data input/output enable signal input pins Only valid in 32-/16-bit bus mode
$\overline{\text{CS}}$	Input	92	Chip select signal input pin. Validates an access to internal registers.

(to be continued)

(cont'd)

Name	Input/ Output	Pin No.	Function
D0 to D31	Input/ output	53, 52, 51, 50, 48, 47, 46, 45, 44, 43, 41, 38, 36, 35, 34, 33, 32, 31, 29, 28, 27, 26, 25, 24, 23, 21, 20, 19, 18, 16, 15, 14	32-bit data input/output pins Function as follows according to bus mode specification. . In 32-bit bus mode, D0 to D7 : Input/output pins of low-order byte of low-order 16 bits of 32-bit data D8 to D15 : Input/output pins of high-order byte of low-order 16 bits of 32-bit data D16 to D31: Input/output pins of high-order 16 bits of 32-bit data . In 16-bit bus mode, D0 to D7 : Input/output pins of low-order byte of 16-bit data D8 to D15 : Input/output pins of high-order byte of 16-bit data D16 to D31: High-impedance (input) state. Fix these pins to the high or low level. . In 8-bit bus mode, D0 to D7 : 8-bit data input/output pins D8 to D31 : High-impedance (input) state. Fix these pins to the high or low level.
DP0 to DP3	Input/ output	12, 11, 10, 9	Parity signal input/output pins added to the data bus . In 32-bit bus mode D0 to D7 : DP0 D8 to D15 : DP1 D16 to D23: DP2 D24 to D31: DP3 . In 16-bit bus mode D0 to D7 : DP0 D8 to D15 : DP1 DP2 and DP3 pins are in high-impedance (input) state. Fix them to the high or low level. . In 8-bit data mode D0 to D7 : DP0 DP1, DP2 and DP3 pins are in high-impedance (input) state. Fix them to the high or low level.

(to be continued)

(cont'd)

Name	Input/ Output	Pin No.	Function
$\overline{DMARQ}$	Output	98	DMA service request signal output pin. The output is low when FIFO is in the following state in the DMA mode specified data-in/data-out phase. Write to FIFO: When data exists only at 6 or less levels of FIFO. Read to FIFO : When data exists at two or more levels of FIFO. If the last transfer data remains in FIFO, the output is also low when data exists only at one level of FIFO.
$\overline{DMAAK}$	Input	99	DMA service enable signal input pin. When this pin becomes active, the data FIFO register is specified as the access target irrespective of signal status of $\overline{CS}$ and A0 to A2. If the DMA mode is not specified, fix this pin to the high level.
$\overline{EOP}$	Output	94	Data transfer termination indicate signal output pin. This pin becomes active upon abnormal termination of the uPD72611 or in the case of break operation. This pin acts as an open-drain output.

1.2 SCSI INTERFACE PINS

Name	Input/ Output	Pin No.	Function
$\overline{SB0}$ to $\overline{SB7}$ *1	Input/ output	56, 57, 59, 60, 62, 63, 65, 66	SCSI data bus input/output pin
$\overline{SBP}$ *1	Input/ output	55	Input/output pin of parity signal added to the SCSI data bus
$\overline{BSY}$ *1	Input/ output	76	Input/output pin connected to $\overline{BSY}$ signal of SCSI control bus. Indicates that another SCSI device is using the SCSI bus.
$\overline{SEL}$ *1	Input/ output	77	Input/output pin connected to $\overline{SEL}$ signal of SCSI control bus. Indicates that select/ reselect operation is being carried out in the selection/reselection phase.
$\overline{REQ}$ *1	Input/ output	70	Input/output pin connected to $\overline{REQ}$ signal of SCSI control bus. Indicates the target information transfer request.
$\overline{ACK}$ *1	Input/ output	69	Input/output pin connected to $\overline{ACK}$ signal of SCSI control bus. Indicates that the initiator has received the target information transfer request.
$\overline{ATN}$ *1	Input/ output	68	Input/output pin connected to $\overline{ATN}$ signal of SCSI control bus. Indicates that the initiator has requested the message-out phase.

(to be continued)

(cont'd)

<table>
<tr><th>Name</th><th>Input/
Output</th><th>Pin No.</th><th>Function</th></tr>
<tr><td>$\overline{MSG}$ *1</td><td>Input/
output</td><td>72</td><td rowspan="3">Input/output pin connected to $\overline{MSG}$, $\overline{C}$/D and $\overline{I}$/O signals of SCSI control bus. Combinations of these signals indicate the SCSI bus phase as follows.

<table><tr><th>$\overline{MSG}$</th><th>$\overline{C}$/D</th><th>$\overline{I}$/O</th><th>Bus Phase</th></tr><tr><td>H</td><td>H</td><td>H</td><td>Data-out phase</td></tr><tr><td>H</td><td>H</td><td>L</td><td>Data-in phase</td></tr><tr><td>H</td><td>L</td><td>H</td><td>Command phase</td></tr><tr><td>H</td><td>L</td><td>L</td><td>Status phase</td></tr><tr><td>L</td><td>L</td><td>H</td><td>Message-out phase</td></tr><tr><td>L</td><td>L</td><td>L</td><td>Message-in phase</td></tr></table></td></tr>
<tr><td>$\overline{C}$/D *1</td><td>Input/
output</td><td>73</td></tr>
<tr><td>$\overline{I}$/O *1</td><td>Input/
output</td><td>74</td></tr>
<tr><td>$\overline{RST}$ *1</td><td>Input/
output</td><td>78</td><td>Input/output pin connected to $\overline{RST}$ signal of SCSI control bus. When this signal is detected, the uPD72611 immediately releases the SCSI bus and activates the INT signal and becomes idle.</td></tr>
<tr><td>RSTO *2</td><td>Output</td><td>87</td><td>This pin outputs a high-level signal while activating $\overline{RST}$ signal and enables the $\overline{RST}$ signal driver for output.</td></tr>
<tr><td>BSYO *2</td><td>Output</td><td>85</td><td>This pin outputs a high-level signal while activating $\overline{BSY}$ signal and enables the $\overline{BSY}$ signal driver for output.</td></tr>
<tr><td>SELO *2</td><td>Output</td><td>86</td><td>This pin outputs a high-level signal while activating $\overline{SEL}$ signal and enables the $\overline{SEL}$ signal driver for output.</td></tr>
<tr><td>IDSTR *2</td><td>Output</td><td>82</td><td>This is a strobe signal output pin to hold its SCSI ID for arbitration when the differential bus is used. It outputs a high-level signal during arbitration and enables the SCSI data bus signal driver corresponding to its ID for output.</td></tr>
</table>

(to be continued)

(cont'd)

Name	Input/ Output	Pin No.	Function
INIT *2	Output	83	This pin outputs a high-level signal while the initiator is in operation and enables the signal ($\overline{ATN}$ and $\overline{ACK}$) drivers to be used during initiator operation for output.
TGT *2	Output	84	This pin outputs a high-level signal during target operation and enables the signal ($\overline{MSG}$, $\overline{C}/D$, $\overline{I}/O$ and $\overline{REQ}$) drivers to be used during target operation for output.
SBOE *2	Output	80	This pin outputs a high-level signal in the data transfer mode and enables the SCSI data bus driver for output.
$\overline{SBIE}$ *2	Output	81	This pin outputs a low-level signal in the data receive mode for arbitration and enables the SCSI data bus receiver for input.

*1: These pins incorporate an output open-drain type driver and an input Schmitt type receiver and can be directly connected to a single-end type SCSI bus.

2: These are enable signal output pins for external differential drivers and output the TTL-level signal. If the external differential driver is not used, leave these pins open.

1.3 OTHER PINS

<table>
<tr><th>Name</th><th>Input/
Output</th><th>Pin No.</th><th>Function</th></tr>
<tr><td>$\overline{\text{RESET}}$</td><td>Input</td><td>89</td><td>System reset input pin</td></tr>
<tr><td>$\overline{\text{16B}}$</td><td>Input</td><td>2</td><td rowspan="2">Bus mode setting input pin
The following bus mode is set depending on the status of this pin.

<table><tr><th>16B</th><th>32B</th><th>Bus Mode</th></tr><tr><td>H</td><td>H</td><td>8-bit bus mode</td></tr><tr><td>L</td><td>H</td><td>16-bit bus mode</td></tr><tr><td>H</td><td>L</td><td>32-bit bus mode</td></tr><tr><td>L</td><td>L</td><td>Use prohibited</td></tr></table></td></tr>
<tr><td>$\overline{\text{32B}}$</td><td>Input</td><td>1</td></tr>
<tr><td>CLK</td><td>Input</td><td>88</td><td>External clock input pin</td></tr>
<tr><td>V_{DD}</td><td>—</td><td>17, 37,
42, 93</td><td>Positive power supply pin</td></tr>
<tr><td>GNDO</td><td>—</td><td>13, 22,
30, 39,
40, 49,
90, 91,
100</td><td>Main ground pin</td></tr>
<tr><td>GND1</td><td>—</td><td>54, 58,
61, 64,
67, 71,
75, 79</td><td>Driver/receiver system ground pin</td></tr>
</table>

1.4 OUTPUT AND INPUT/OUTPUT PIN STATUS AFTER RESET

Pin Name	Status after Reset
$\overline{SB0}$ to $\overline{SB7}$, $\overline{SBP}$	High impedance (input)
$\overline{ANT}$, $\overline{ACK}$, $\overline{REQ}$, $\overline{MSG}$, $\overline{C}$/D, $\overline{I}$/O, $\overline{BSY}$, $\overline{SEL}$, $\overline{RST}$	High impedance (input)
D0 to D31, DP0 to DP3	High impedance (input)
INT	Low level
$\overline{DMARQ}$	High level
$\overline{EOP}$	High impedance (open-drain output)

CHAPTER 2. INTERNAL BLOCK FUNCTIONS

(1) SCSI driver/receiver

This unit consists of an open-drain type driver (with a sink current of 48 mA) to drive the single-end SCSI bus compliant with the SCSI-2 specifications, a Schmitt type receiver having hysteresis characteristics and an external differential drive control signal driver.

(2) Arbitration and selection control

This block controls the execution sequence of the arbitration, selection and reselection phases. It consists of a timing generator and a sequencer.

(3) Bus phase control

This block controls and monitors the bus phase of the SCSI bus. It outputs a signal to specify the bus phase and detects the bus phase transition by monitoring the bus phase.

(4) SCSI transfer control

This block controls data transfer on the SCSI bus in each information transfer phase of the SCSI (data-in, data-out, command, status, message-in and message-out). It controls the transfer protocol using the $\overline{REQ}$ and $\overline{ACK}$ signals and data transfer execution/stop according to the SCSI FIFO state. It incorporates a 24-bit transfer counter and places the number of transfer data on the SCSI bus under management.

(5) SCSI data bus FIFO buffer

This is a 9-bit x 8-level asynchronous FIFO. It absorbs differences in data transfer timing between the SCSI bus and the uPD72611 internal bus. In addition, it is used for receive data queuing for synchronous transfer.

This FIFO shifts data as well as parities in the parity through mode.

(6) CMD/MSC decoder

This unit decodes the received SCSI-2 command and message and generates a decode signal to define the next sequence.

(7) SCSI data bus parity generator/checker

While not in the parity through mode, this unit generates a parity to be added to the data to be transmitted to the SCSI data bus and transmits it to the SCSI bus. In the parity through mode, this unit transmits the parity added from the host CPU to the SCSI bus. It also checks the parity added to the data read from the SCSI data bus.

(8) Main control block

This is a microprogram control sequencer. It exercises control over the operations of each block and generates a series of control sequences.

(9) Internal transfer control

This block controls data transfer between the SCSI FIFO and host FIFO and indirect register. When the host CPU is set to the 16-bit or 32-bit mode, the block controls conversions from 8-bit data to 16-bit/32-bit data and vice versa.

(10) Direct access registers

These are registers such as command and status registers directly accessible from the host CPU.

(11) Indirect access registers

These are registers not directly accessible from the host CPU. They are accessible via a direct register window.

(12) Host data bus FIFO buffer

This is a 32-bit x 8-level asynchronous FIFO. It is a register to improve the host bus use efficiency. In the 8-bit mode this buffer acts as a 9-bit x 8-level FIFO and only low-order 9 bits are used. In the 16-bit mode this buffer acts as an 18-bit x 8-level FIFO and only the low-order 18 bits are used. In the parity through mode it shifts data as well as parities.

(13) Interrupt control

This block controls the set/reset of interrupt signals.

(14) Read/write control

This block controls read/write of various internal registers. It also controls 8-bit access in the 16-/32-bit mode.

(15) Bus-size converter

This unit converts the bus width according to the bus mode.

(16) Host data bus parity generator/checker

While not in the parity through mode, this unit generates a parity to be added to the data to be transmitted to the host bus and transmits it to the host bus. In the parity through mode, this unit transmits the added parity to the host bus. It also checks the parity added to the data read from the host bus.

(17) DMA request control

This block generates the DMA service request signal ($\overline{\text{DMARQ}}$) in accordance with the FIFO state. It also controls the termination of command operations by the $\overline{\text{EOP}}$ signal.

(18) Clock generator

From the system clock input from the CLK pin, this unit generates two 2-phase clock signals for internal block control; one is of same frequency as the system clock signal, and the other, of half the frequency.

CHAPTER 3. INTERNAL REGISTER CONFIGURATION

The uPD72611 has thirty-nine internal 8-bit registers and 8-/16-/32-bit FIFOs. These registers are divided into direct registers which the host CPU can directly access and indirect registers which are indirectly accessed via an address pointer.

3.1 DIRECT ACCESS REGISTERS

These are registers which the CPU can directly access. They are listed below.

Table 3-1 Direct Access Register List

Address				R/W	Symbol	Name
A3	A2	A1	A0			
0	0	0	0	R/W	DF0	Data FIFO 0 register
0	0	0	1	R/W	DF1	Data FIFO 1 register
0	0	1	0	R	CST	Controller status register
0	0	1	1	R/W	ADR	Address register
0	1	0	0	R/W	WIN1	Window 1
0	1	0	1		WIN2	Window 2
0	1	1	0	R	TP	Terminated phase register
				W	DID	Destination ID register
0	1	1	1	R	IST	Interrupt status register
				W	CMD	Command register
1	0	0	0	R	EXST	Extended status register
1	0	0	1	-	——	Use prohibited
1	0	1	0			
1	0	1	1			
1	1	0	0	R/W	DF2	Data FIFO 2 register
1	1	0	1			
1	1	1	0			
1	1	1	1			

NOTE: In the busy state (with CBSY bit of CST register set to 1), write data to DF0, DF1, DF2 and CMD registers only.

3.2 INDIRECT ACCESS REGISTERS

The CPU cannot directly access the indirect registers. The indirect registers are accessible via a direct register window. The address is specified by the low-order 6 bits of the ADR register. The indirect registers are listed below.

Table 3-2 Indirect Access Register List

Address	R/W	Symbol	Name
00H	R/W	TST	Target status register
01H	R	SBST	SCSI bus status register
02H	R	SID	Source ID register
03H	R/W	MSG	Message register
04H to 0FH	R/W	CDB00 to CDB11	Command descriptor block (CDB)
10H	R/W	TMOD	Transfer mode register
11H	R	CTCL	Current counter (low-order 8 bits)
	W	BTCL	Base counter (low-order 8 bits)
12H	R	CTCM	Current counter (intermediate-order 8 bits)
	W	BTCM	Base counter (intermediate-order 8 bits)
13H	R	CTCH	Current counter (high-order 8 bits)
	W	BTCH	Base counter (high-order 8 bits)
14H	R/W	MSG2	Message 2 register
15H	R/W	MSG3	Message 3 register
16H	R/W	EXMOD	Extended mode register
17H to 1FH	-	——	Use prohibited

(to be continued)

Table 3-2 Indirect Access Register List (cont'd)

Address	R/W	Symbol	Name
20H	R/W	BFTOUT	Bus free timeout register
21H	R/W	SRTOUT	Selection/reselection timeout register
22H	R/W	RATOUT	$\overline{REQ}$/$\overline{AKC}$ handshake timeout register
23H	R/w	CDBL	CDB length register
24H	R/W	MOD	Mode register
25H	R/W	PID	Physical ID register
26H to 3FH	-	——	Use prohibited

CHAPTER 4. COMMANDS

The uPD72611 is provided with the following 18 types of commands. These commands are used for the CPU to control the uPD72611. Table 4-1 lists the commands.

4.1 COMMAND CLASSIFICATION

The commands are classified into the following three groups according to applications.

- Group I ..... Commands to be used when acting as an initiator or a target
- Group II .... Commands to be used when acting as an initiator
- Group III ... Commands to be used when acting as a target

Besides the above groups, the commands are also classified into the following three types according to their execution modes.

- Type A ... Commands to control the uPD72611 state
- Type B ... Commands to control SCCI basic protocols
- Type C ... Commands (composite commands) to automatically execute multiple type B commands in a standard sequence

Type A commands are executed immediately after they are issued (irrespective of whether type B and type C commands are being executed). No interrupt are generated upon termination of processing (except the CHIP RESET command).

Type B and C commands inform the CPU of the termination of processing at the interrupt request. While type B and C commands are being executed, the busy state remains set. If type B and C commands are issued in the busy state, they are ignored.

4.2 COMMAND OPERATING STATES

There are three command operating states as follows.

- DISCONNECT: D
- INITIATOR : I
- TARGET : T

A command is valid or invalid depending on the uPD72611 state when it is issued. If a command is issued in an invalid state, it is processed as an invalid command. If a command is issued during uPD72611 internal processing due to state transition on the SCSI bus, the uPD72611 ignores the issued command. In this case, as an interrupt derived from the state transition is generated, check the IST register contents and carry out processing accordingly. After that, if it is desired to execute the previously ignored commands, those commands must be reissued.

Table 4-1 Command Function List

Group	Command Name	Mnemonic	Outline of Operation	State	Type
Group I	CHIP RESET	CRST	uPD72611 inside is reset	D, I, T	A
	BREAK	BRK	Command execution is suspended	D, I, T	A
	DISCONNECT	DIS	SCSI bus is released	D, I, T	A
	CLEAR FIFO	CLRF	FIFO is cleared	D, I, T	A
	SCSI RESET	SRST	SCSI bus is reset	D, I, T	B

(to be continued)

Table 4-1 Command Function List (cont'd)

Group	Command Name	Mnemonic	Outline of Operation	State	Type
Group II	SET ATN	SETAT	$\overline{ATN}$ signal is set (0)	I	A
	RESET ACK	RSTAK	$\overline{ACK}$ signal is set (1)	I	A
	SELECT	SEL	Target is selected	D	B
	TRANSFER	TFR	Information is transmitted/received (when command is acting as initiator)	I	B
	AUTO INITIATOR	AINI	Standard initiator operation is automatically executed	D	C
	AUTO INITIATOR 2	AINI2	Standard initiator operation is automatically executed after reselection	I	C
Group III	RESELECT	RSEL	Initiator is reselected	D	B
	RECEIVE	REC	Information is received (when command is acting as target)	T	B
	SEND	SND	Information is transmitted (when command is acting as target)	T	B
	AUTO TARGET	ATGT	Standard target operation is automatically executed	D	C
	AUTO TARGET 2	ATGT2	Standard target terminating operation is automatically executed	T	C
	RE-RECEIVE	RREC	Reselection → data reception is continuously executed (when command is acting as target)	D	C
	RE-SEND	RSND	Reselection → data transmission is continuously executed (when command is acting as target)	D	C

CHAPTER 5. DIFFERENCES FROM uPD72111 (SCSI CONTROLLER)

The uPD72611 SCSI-2 controller has undergone extensions including an increase of speeds. CPU side bus width extension and differential driver applications on the basis of the uPD72111 SCSI controller. The register and command systems are uPD72111 software upward compatible. The following are differences from the uPD72111.

- o 32-bit CPU bus is supported.

- o External differential driver/receiver is supported.

- o Block transfer mode is supported as CPU side transfer mode

- o Mode for parity error detection only has been added (data transfer is not suspended).

- o Parity through mode has been added

- o A function has been added to set $\overline{\text{ATN}}$ signal due to a CPU bus parity error during type B or C command processing (with CBSY bit set) in addition to SCSI bus parity error.

- o Arbitration delay has been changed by revising the SCSI and SCSI-2 specifications.

  uPD72111: 2.2 ns
  uPD72611: 2.4 ns

- o High-speed synchronous transfer function is supported:

  Max. 10 MB/S

  High-speed synchronous transfer is set with TMOD register

TMOD Format

Address	7	6	5	4	3	2	1	0	
10H	SYNC	TPD2	TPD1	TPD0	HSYNC	TOF2	TOF1	TOF0	(R/W)

	SYNC	HSYNC	TPD2	TPD1	TPD0	Data Transfer Cycle (Clock)	Transfer Rate (Mbyte/s) When Operated at 20 MHz
Synchronous transfer	1	0	0	0	0	16	1.25
					1		
				1	0	4	5.00
					1	6	3.33
			1	0	0	8	2.50
					1	10	2.00
				1	0	12	1.66
					1	14	1.42
High-speed synchronous transfer	1	1	0	0	0	8	2.50
					1		
				1	0	2	10.00
					1	3	6.66
			1	0	0	4	5.00
					1	5	4.00
				1	0	6	3.33
					1	7	2.85

NOTE: When SYNC = 0, data transfer is asynchronous irrespective of HSYNC and TPD0 to TPD2.

TOF2	TOF1	TOF0	$\overline{REQ}$ and $\overline{ACK}$ Pulse Offset Value Specification in Synchronous/High-Speed Synchronous Transfer Mode
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7
0	0	0	8

o The reset default values of INTM bit of destination ID register and DHP bit of mode register have been changed.

Bit	uPD72611	uPD72111
INTM	1	0
DHP	1	0

o EXST, DF2, MSG2, MSG3 and EXMOD registers have been added.

(1) Extended status register (EXST)

This is an 8-bit register to indicate uPD72611 operating state. Because it is a read only register, data is invalid if written to the EXST.

This register is reset to 00H by inputting $\overline{RESET}$, executing CHIP RESET command or writing DISCONNECT (type A), type B or type C command to the CMD register.

EXST Format

Address	7	6	5	4	3	2	1	0	
08H	0	0	0	0	0	0	HBPER	SBPER	(R)

HBPER	Parity Error Detection in the Data Received from CPU Bus
0	Parity error not detected
1	Parity error detected

SBPER	Parity Error Detection in the Data Received from SCSI Bus
0	Parity error not detected
1	Parity error detected

(2) Data FIFO register (DF2)

This is a 32-bit register to read/write information (data, command, status and message) to be accessed via the SCSI data bus. It is used in the 32-bit bus mode. When a data word to be output to the SCSI bus is written, it is output to the SCSI bus starting from the low-order 8-bit data.

When reading data input from the SCSI bus, the setting is made from the low-order byte, starting from the first input 8-bit data. In the 32-bit bus mode, the DF2 register functions as a 32-bit length register. Thus, it is not accessible in byte or half-word units.

This register becomes empty when $\overline{\text{RESET}}$ is input or CHIP RESET or CLEAR FIFO command is executed.

DF2 Format

Address	7	6	5	4	3	2	1	0	
0CH	D7	D6	D5	D4	D3	D2	D1	D0	(R/W)
0DH	D15	D14	D13	D12	D11	D10	D9	D8	(R/W)
0EH	D23	D22	D21	D20	D19	D18	D17	D16	(R/W)
0FH	D31	D30	D29	D28	D27	D26	D25	D24	(R/W)

(3) Message 2 register (MSG2)

This is an 8-bit register to set and store the 1st byte (queue tag code) of a queue tag message to be transmitted/ received when a type C command including queue tag message transmission/reception is executed.

MSG2 Format

Address	7	6	5	4	3	2	1	0	
14H	Message 2								(R/W)

(4) Message 3 register (MSG3)

This is an 8-bit register to set and store the 2nd byte (queue tag) of a queue tag message to be transmitted/ received when a type C command including queue tag message transmission/reception is executed.

MSG3 Format

Address	7	6	5	4	3	2	1	0	
15H	Message 3								(R/W)

(5) Extended mode register (EXMOD)

This register is used to set the operation mode of functions of uPD72611 extended from the uPD72111. Be sure to write 0 to bits 4 through 7. This register is reset to 00H by inputting $\overline{\text{RESET}}$ or executing CHIP RESET command.

EXMOD Format

Address	7	6	5	4	3	2	1	0	
16H	0	0	0	0	MSG3	PTHR	PERP	BLKT	(R/W)

MSG3	QUEUE TAG Message Support
0	QUEUE TAG message is not supported
1	QUEUE TAG message is supported

PTHR	Parity Through Mode Specification
0	Parity through mode is not specified
1	Parity through mode is specified

PERP	Continued Data Transfer Specification after Parity Error Detection
0	Transfer is suspended upon detection of a parity error
1	Transfer is continued after detection of a parity error

BLKT	DMA Transfer Mode Specification
0	Demand transfer mode
1	Block transfer mode (transfer of data corresponding to eight FIFO levels)

o Composite command extension and addition

(1) 10-byte commands of group 2 are added to SCSI-2 commands supported by AUTO INITIATOR and AUTO TARGET commands

(2) Command queuing function is supported by all composite commands

With the EXMOD register added, the queue tag message is supported by the MSG3 bit using the type C command.

Command processing sequences with the MSG3 bit set are described below together with additional codes.

<AUTO INITIATOR command>

. When both AT bit and MSG3 bit are 1

(a) Bus arbitration
(b) Target selection — SELECT command
(c) Message register content transmission (Identify message) — TRANSFER command-1
(d) Message 2 register content transmission (1st byte queue tag code of queue tag message) — TRANSFER command-2
(e) Message 3 register content transmission (2nd byte queue tag of queue tag message) — TRANSFER command-3
(f) CDB register content transmission (SCSI-2 command) — TRANSFER command-4
(g) Data transmission/reception — TRANSFER command-5
(h) Status reception — TRANSFER command-6
(i) Command complete message reception — TRANSFER command-7

. When AT bit is 0 and MSG3 bit is 1

Message register content transmission is not carried out (same as when both AT bit and MSG bit are 0).

TP7 to TP0	HEX	Execution Phase
0 0 1 1 1 0 0 0	38H	Queue tag message 1 transmit phase
0 0 1 1 1 0 0 1	39H	Queue tag message 2 transmit phase

<AUTO TARGET command>

. When $\overline{\text{ATN}}$ signal is active and MSG3 bit is 1 for selection

(a) Response to selection
(b) Identify message reception RECEIVE command-1
(Storage into message register)
(c) Queue tag message 1st byte reception
(Storage into message 2 register)
RECEIVE command-2
(d) Queue tag message 2nd byte reception
(Storage into message 3 register)
RECEIVE command-3
(e) SCSI-2 command reception RECEIVE command-4

TP7 to TP0	HEX	Execution Phase
0 1 1 1 0 1 0 0	74H	Parity error termination upon reception of 1st byte of SCSI-2 command (CDB)*
0 1 1 1 0 1 0 1	75H	Queue tag message 1st byte receive phase
0 1 1 1 0 1 1 0	76H	Queue tag message 2nd byte receive phase
0 1 1 1 0 1 1 1	77H	Command receive phase (when 3-byte message is received)
0 1 1 1 1 0 0 0	78H	Parity error termination upon reception of 1st byte of SCSI-2 command (CDB) (when 3-byte message is received)*

*: Set only when a parity error occurs in the 1st byte of a command with PERP = 1.

<RE-RECEIVE command>

. When MSG3 bit is 1

(a) Bus arbitration
(b) Initiator reselection — RESELECT command
(c) Identify message transmission — SEND command-1 (MG = 1, CD = 1)
(d) Queue tag message 1st byte transmission — SEND command-2 (MG = 1, CD = 1)
(e) Queue tag message 2nd byte transmission — SEND command-3 (MG = 1, CD = 1)
(f) Data reception — RECEIVE command (MG = 0, CD = 0)

TP7 to TP0	HEX	Execution Phase
1 0 0 0 0 1 0 1	85H	Queue tag message 1 transmit phase
1 0 0 0 0 1 1 0	86H	Queue tag message 2 transmit phase

<RE-SEND command>

. When MSG3 bit is 1

(a) Bus arbitration
(b) Initiator reselection — RESELECT command
(c) Identify message transmission — SEND command-1 (MG = 1, CD = 1)
(d) Queue tag message 1st byte transmission — SEND command-2 (MG = 1, CD = 1)
(e) Queue tag message 2nd byte transmission — SEND command-3 (MG = 1, CD = 1)
(f) Data transmission — SEND command (MG = 0, CD = 0)

TP7 to TP0	HEX	Execution Phase
1 0 0 1 0 1 0 1	95H	Queue tag message 1 transmit phase
1 0 0 1 0 1 1 0	96H	Queue tag message 2 transmit phase

(3) Addition of composite commands (AUTO INITIATOR 2 and AUTO TARGET 2 commands)

<AUTO INITIATOR 2 command>

Type : C

Command code : 7 0

C1	C0	0	1	0	1	0	1

C1	C0	Data Set Operation to Current Transfer Counter	No. of Transfer Bytes and Transfer Byte Unit
0	0	CTCH, CTCM, CTCL ← BTCH, BTCM, BTCL	0 to 16,777,215 bytes Bytewise setting
0	1	CTCH, CTCM ← BTCH, BTCM CTCL ← 00H	0 to 16,776,960 bytes Setting in 256-byte units
1	0	CTCL ← BTCL CTCH, CTCM ← 0000H	0 to 255 bytes Setting in byte units
1	1	CTCH, CTCM, CTCL ← 000001H	Fixed to 1 (not affected by BTCH, BTCM and BTCL contents)

State transition: D → D, I

Outline : Standard initiator operation after reselection is automatically executed. This command continuously executes combinations of multiple TRANSFER commands.

Setting necessary before command generation:

TOMD register ← Transfer mode
BTCL, BTCM and BTCH registers
← No. of data transfer bytes

Operation : The command processing sequence is as follows.

(a) Data transmission/reception
TRANSFER command
(b) Status reception
TRANSFER command-2
(c) Command complete message reception
TRANSFER command-3

However, the identify message cannot automatically be received. Thus, if the reselect target requests the message-in phase before this command is issued, it is necessary to check which logical unit has been reselected by issuing the TRANSFER command to the initiator and fetching the identify message.

Operation in each sequence is described below.

(1) Data transmission/reception (corresponding to TRANSFER command operation)

After the command is written, transmission/reception of data with the number of transfer data bytes set using C1 and C0 is started with the BTCH, BTCM and BTCL registers via the host FIFO within a maximum of 16 clock cycles. This operation is equivalent to that of the TRANSFER command.

The data transfer direction is specified by the $\overline{I}$/O signal on the SCSI bus. Processing proceeds to (2) upon termination of the transfer of the set number of transfer data bytes. When the number of data transfer bytes is set to 0 (000000H to BTCH, BTCM and BTCL), data transmission/ reception is not carried out and processing proceeds to (2) except when C1 = 1 and C0 = 1.

(2) SCSI-2 status reception (corresponding to TRANSFER command operation)

1-byte SCSI status reception corresponding to TRANSFER command operation is started. The received SCSI status is stored in the TST register. Upon successful reception of the SCSI status, processing proceeds to (3).

(3) Command complete message reception (corresponding to TRANSFER command operation)

1-byte message reception corresponding to TRANSFER command operation is started. The received command complete message is stored in the MSG register. Upon successful reception of the command complete message, processing proceeds to (4).

(4) Termination

After command complete message reception succeeds and a series of command processing sequences are terminated normally, the system waits for command reception in the DISCONNECT state after it has generated an interrupt request.

Break operation : When the BREAK command is written, command processing is immediately suspended and an interrupt request is generated and the system waits for command reception in the INITIATOR state. The $\overline{EOP}$ signal remains active during the DMA service after breaking.

Abnormal termination:

o Processing

Command processing is suspended and an interrupt request is generated and the system waits for command reception in the INITIATOR state.

o Command generating condition

. FIFO overrun/underrun
If host FIFO overrun/underrun is detected during data transfer

. Synchronous transfer offset error
If the $\overline{REQ}$ and $\overline{ACK}$ signal offset values get out of the set range during data transfer in the synchronous transfer mode

. SCSI bus parity error
If a parity error is detected in the data, status or message read from the SCSI bus. When a parity error is detected, the $\overline{ATN}$ signal is automatically set.

. CPU bus parity error
If a parity error is detected in the data written from the CPU bus. When a parity error is detected, the $\overline{ATN}$ signal is automatically set.

- $\overline{REQ}/\overline{ACK}$ timeout error
  If the information transfer handshake operation continues to be paused for more than the period set using the RATOUT register.
- Information transfer phase error
  If the bus phase changes during information transfer or the bus phase is different from one assumed from the command sequence.

Service Request : In the command complete message receive sequence, a 1-byte message is received. The uPD72611 reads the message from the SCSI bus and simultaneously transfers it to the MSG register and decodes it. Except for the command complete message, the transfer operation is terminated with the $\overline{ACK}$ signal remaining active and a service interrupt request is issued to the CPU. The CPU reads and decodes the message stored in the MSG register as interrupt servicing and then decides to accept or reject the message. To accept the message, the CPU must immediately complete handshaking by the RESET ACK command. To reject the message, the CPU must activate the $\overline{ATN}$ signal by the SET ATN command and then complete handshaking by the RESET ACK command.

Operation upon parity error detection:

- If PERP bit of EXMOD register has not been set
  If a parity error is detected, command execution is immediately suspended and an interrupt request is generated. At this point the system waits for command reception in the INITIATOR state. And during DMA service after error detection, the $\overline{EOP}$ signal remains active. Upon detection of a parity error, the $\overline{ATN}$ signal is automatically set.
- If PERP bit of EXMOD register has been set
  If a parity error is detected during information transfer, the transfer operation continues until the end of the phase. After termination of the transfer, whether a parity error has occurred or not is checked. If a parity error has occurred, an interrupt request is generated and the system waits for command reception in the INITIATOR state. Occurrence of a parity error can be checked by reading the EXST register. The parity error generated phase can be checked by reading the TP register.

Interrupts to be set upon termination of command execution (except reset and break during execution)

- Command normal termination interrupt
  If a parity error occurs upon normal termination or with PERP bit set

- Invalid command interrupt
  If command is written with the uPD72611 placed in a state other than initiator.
- Host FIFO overrun/underrun interrupt
  If an FIFO overrun/underrun occurs during command execution
- Synchronous transfer offset error interrupt
  If a synchronous transfer offset error occurs during command execution
- SCSI bus parity error interrupt
  If a parity error is detected in the data received from the SCSI bus
- CPU bus parity error interrupt
  If a parity error is detected in the data received from the CPU bus
- $\overline{REQ}/\overline{ACK}$ timeout error interrupt
  If a $\overline{REQ}/\overline{ACK}$ timeout error occurs
- Information transfer phase error interrupt
  If the phase changes during command execution or a phase different from the expected phase is generated
- SCSI reset condition interrupt
  If pending has occurred before command generation or a reset condition is set during command execution. In the former case, since a command is acknowledged, another interrupt is generated after the SCSI reset condition interrupt.

- Disconnected interrupt
  If pending has occurred before command generation or the target has released the bus during command execution. In the former case, an invalid command interrupt is generated after the disconnected interrupt.
- Message receive interrupt
  If a message except the command complete message is received in the message receive phase.

Execution phase code:

TP7 to TP0	HEX	Execution Phase
0 0 1 1 0 1 0 1	35H	Data transmit/receive phase
0 0 1 1 0 1 1 0	36H	Status receive phase
0 0 1 1 0 1 1 1	37H	Command complete message receive phase

<AUTO TARGET 2 command>

Type : C

Command code : 7 0

0	0	1	1	0	0	0	1

State transition: T → D, T

Outline : This is a command to automatically execute the standard sequence to terminate the SCSI-2 command which the target has acknowledged from the initiator.

This command automatically executes two SEND command processing to be executed to terminate the SCSI-2 command acknowledged from the initiator.

Setting necessary before command generation:

MSG register ← Command complete message
STS register ← Terminate status

Operation : The command processing sequence is as follows.

(a) Terminate status transmission
SEND command-1 (MG = 0, CD = 1)
(b) Command complete message transmission
SEND command-2 (MG = 1, CD = 1)

Operation in each sequence is described below.

(1) Terminate status transmission (corresponding to SEND command operation)

When a command is written, 1-byte status transmission corresponding to SEND command operation is started within a maximum of 12 clock cycles. Upon successful status transmission, processing proceeds to (2).

(2) Command complete message transmission (corresponding to SEND command operation)

1-byte message transmission corresponding to SEND command operation is started. Upon successful message transmission, processing proceeds to (3).

(3) Termination

After message transmission succeeds and a series of processing sequences are terminated normally, the system waits for command reception in the DISCONNECT state after it has carried out processing corresponding to DISCONNECT command operation to release the SCSI bus and generated an interrupt request.

Break operation : When the BREAK command is written during command execution, command processing is immediately suspended and an interrupt request is generated and the system waits for command reception in the TARGET state.

Abnormal termination:

o Processing

Command processing is suspended and an interrupt request is generated and the system waits for command reception in the TARGET state.

o Command generating condition

. Invalid command
  If a command has been generated in the DISCONNECT and INITIATOR state.

. CPU bus parity error
  If a parity error has been detected in the command code written from the CPU bus.

. $\overline{REQ}/\overline{ACK}$ timeout error
  The information transfer handshake operation has not proceeded for more than the period set using the RATOUT register.

Interrupts to be set upon execution termination (except for reset and break during execution)

. Command normal terminate interrupt
  This interrupt is generated in the following cases. Each interrupt is identified by the TP register value.
  ① Normal termination (TP = A3H)
  ② If $\overline{ATN}$ signal becomes active after transmission of terminate status (TP = A1H)
  ③ If $\overline{ATN}$ signal becomes active after transmission of command complete message (TP = A2H)

. Invalid command interrupt
  If a command is written with the uPD72611 placed in a state other than target state.

. Host FIFO overrun/underrun interrupt
  If a host FIFO overrun/underrun occurs during command execution

. CPU bus parity error interrupt
  If a parity error is detected in the data received from the CPU bus

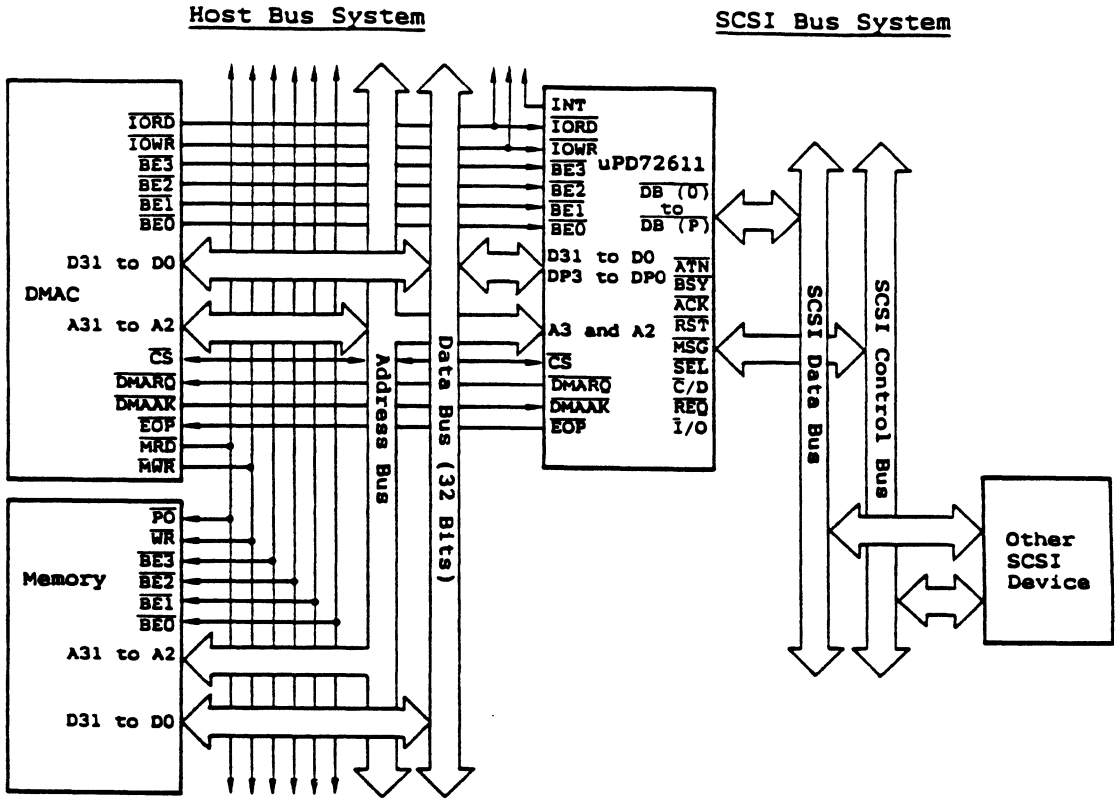
- $\overline{REQ}/\overline{ACK}$ timeout error interrupt
  If $\overline{REQ}/\overline{ACK}$ timeout error occurs
- SCSI reset condition interrupt
  If pending has occurred before command generation or a reset condition is set during command execution. In the former case, since the uPD72611 is in the DISCONNECT state, an invalid command interrupt is generated after the SCSI reset condition interrupt.

Execution phase code:

TP7 to TP0	HEX	Execution Phase
1 0 1 0 0 0 0 1	A1H	Terminate status transmit phase
1 0 1 0 0 0 1 0	A2H	Command complete message transmit phase
1 0 1 0 0 0 1 1	A3H	Disconnect state

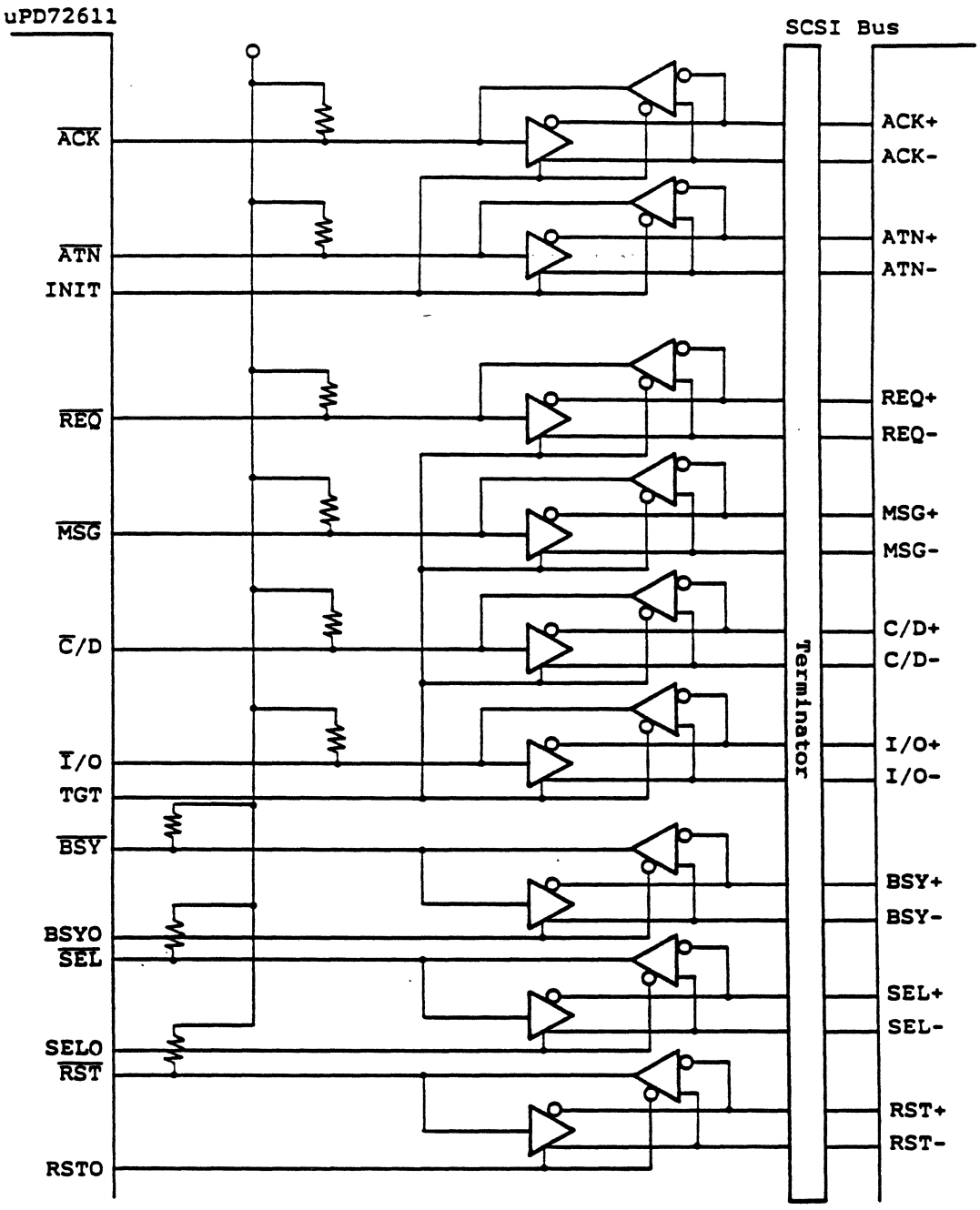
CHAPTER 6. SYSTEM CONFIGURATION EXAMPLE

(1) System configuration example

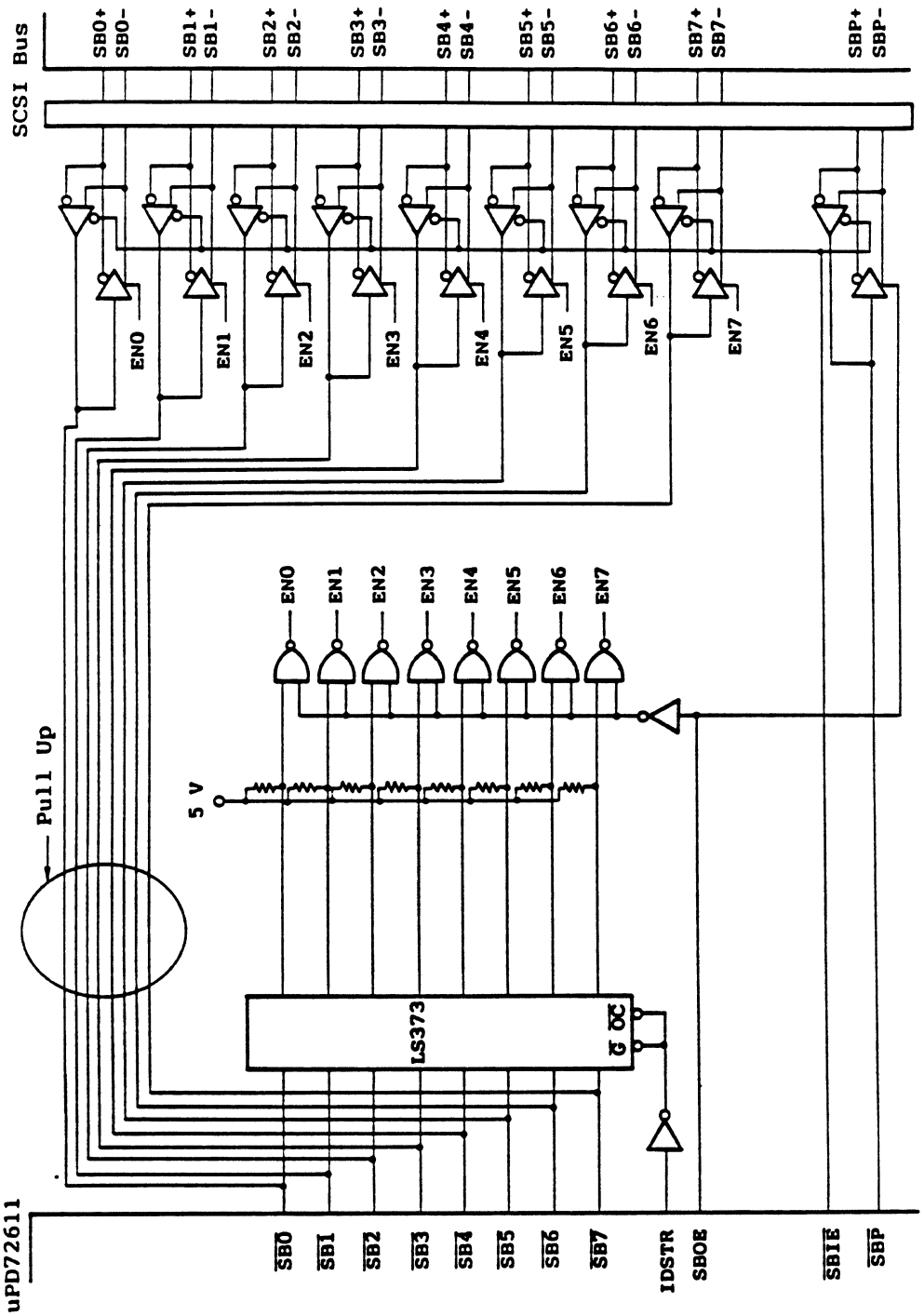


(2) External differential driver configuration example

(a) SCSI control bus



(b) SCSI data bus



CHAPTER 7. ELECTRICAL SPECIFICATIONS (TARGET)

NOTE: These specifications are target values and the specifications of samples and volume products may differ from them.

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Test Conditions	Rating	Unit
Power supply voltage	V_{DD}		-0.5 to +7.0	V
Input voltage	V_I		-0.5 to V_{DD} +0.5	V
Output voltage	V_O		-0.5 to V_{DD} +0.5	V
Operating temperature	T_{opt}		-10 to +70	°C
Storage temperature	T_{stg}		-65 to +150	°C

DC Characteristics (Ta = -10°C to +70°C, V_{DD} = +5.0 V ±10%)

CPU interface signal pins

INT, $\overline{IORD}$, $\overline{IOWR}$, A2 & A3, A0/$\overline{BE2}$ & A1/$\overline{BE3}$, $\overline{BE0}$/$\overline{UBE}$, $\overline{BE1}$, $\overline{CS}$, D0 to D31, DP0 to DP3, $\overline{DMARQ}$, $\overline{DMAAK}$, $\overline{EOP}$, $\overline{RESET}$, $\overline{16B}$, $\overline{32B}$, CLK, RST0*, BSY0*, SEL0*, IDSTR*, INIT*, TGT*, SBOE*, $\overline{SBIE}$*

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Input voltage high	V_{IH1}		2.2	V_{DD} +0.5	V
Input voltage low	V_{IL1}		-0.5	0.8	V
CLK input voltage high	V_{IH3}		3.3	V_{DD} +0.5	V
CLK input voltage low	V_{IL2}		-0.5	0.6	V
Output voltage high	V_{OH}	I_{OH1} = -400 uA	0.7 V_{DD}		V
Output voltage low	V_{OL1}	I_{OL1} = 2.5 mA		0.4	V
Input leakage current high	I_{LIH1}	V_I = V_{DD}		10	uA
Input leakage current low	I_{LIL1}	V_I = 0 V		-10	uA
Output leakage current high	I_{LOH1}	V_O = V_{DD}		10	uA
Output leakage current low	I_{LOL}	V_O = 0 V		-10	uA
Supply current	I_{DD}	At 20 MHz operation		120	mA

*: These are SCSI interface signal pins. Their DC characteristics are the same as those of the CPU interface.

SCSI interface signal pins

$\overline{SB0}$ to $\overline{SB7}$, $\overline{SBP}$, $\overline{RST}$, $\overline{BSY}$, $\overline{SEL}$, $\overline{MSG}$, $\overline{C/D}$, $\overline{I/O}$, $\overline{ATN}$, $\overline{ACK}$, $\overline{REQ}$

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Input voltage high	V_{IH2}		2.0	V_{DD} +0.5	V
Input voltage low	V_{IL2}		-0.5	0.8	V
Input hysteresis	V_{HI}		0.2		V
Output voltage low	V_{OL2}	I_{OL2} = 48 mA		0.5	V
Input leakage current high	I_{LIH2}	$V_I = V_{DD}$		0.1	mA
Input leakage current low	I_{LIL2}	V_I = 0 V		-0.1	mA
Output leakage current high	I_{LOH2}	$V_O = V_{DD}$		0.25	mA

Capacitance (Ta = 25°C, V_{DD} = 0 V)

Host bus interface

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz Unmeasured pins returned to 0 V		20	pF
Output capacitance	C_O			20	pF
I/O capacitance	C_{IO1}			20	pF

SCSI bus interface

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
I/O capacitance	C_{IO2}	f = 1 MHz, unmeasured pins returned to 0 V		20	pF

AC Characteristics (Ta = -10°C to +70°C, V_{DD} = +5 V ±10%)

Host bus interface

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
CLK input cycle time	t_{CYK}		50	125	ns
CLK input high-level width	t_{KKH}		20		ns
CLK input low-level width	t_{KKL}		20		ns
CLK input rise time	t_{KR}			10	ns
CLK input fall time	t_{KF}			10	ns
$\overline{RESET}$ low-level width	t_{RSRSL}		16		t_{CYK}
$\overline{CS}$ setup time (to $\overline{IORD}$↓)	t_{SCSR}		0		ns
$\overline{CS}$ hold time (from $\overline{IORD}$↑)	t_{HRCS}		0		ns
Address setup time (to $\overline{IORD}$↓)	t_{SAR}		10		ns
Address hold time (from $\overline{IORD}$↑)	t_{HRA}		0		ns
$\overline{DMAAK}$ setup time (to $\overline{IORD}$↓)	t_{SDAR}		0		ns
$\overline{DMAAK}$ hold time (from $\overline{IORD}$↑)	t_{HRDA}		0		ns
$\overline{IORD}$ low-level width	t_{RRL}		50		ns
$\overline{IORD}$↓, $\overline{IOWR}$↓ recovery time from $\overline{IORD}$↑	t_{RVR}		50		ns
Data output delay time from $\overline{IORD}$↓	t_{DRD}			35	ns
Data float time from $\overline{IORD}$↑	t_{FRD}		0	30	ns
$\overline{DMARQ}$↑ delay time from $\overline{IORD}$↑	t_{DRDQ}			60	ns
$\overline{CS}$ setup time (to $\overline{IOWR}$↓)	t_{SCSW}		0		ns
$\overline{CS}$ hold time (from $\overline{IOWR}$↑)	t_{HWCS}		0		ns

(to be continued)

(cont'd)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Address setup time (to $\overline{IOWR}\downarrow$)	t_{SAW}		10		ns
Address hold time (from $\overline{IOWR}\uparrow$)	t_{HWA}		0		ns
$\overline{DMAAK}$ setup time (to $\overline{IOWR}\downarrow$)	t_{SDAW}		0		ns
$\overline{DMAAK}$ hold time (from $\overline{IOWR}\uparrow$)	t_{HWDA}		0		ns
$\overline{IOWR}$ low-level width	t_{WWL}		50		ns
$\overline{IORD}\downarrow$, $\overline{IOWR}\downarrow$ recovery time from $\overline{IOWR}\uparrow$	t_{RVW}		50		ns
Data setup time (to $\overline{IOWR}\uparrow$)	t_{SDW}		35		ns
Data hold time (from $\overline{IOWR}\uparrow$)	t_{HWD}		5		ns
$\overline{DMARQ}\uparrow$ delay time from $\overline{IOWR}\uparrow$	t_{DWDQ}			60	ns
$\overline{EOP}\uparrow$ delay time from $\overline{IORD}\uparrow$	t_{DRE}			40	ns
$\overline{EOP}\uparrow$ delay time from $\overline{IOWR}\uparrow$	t_{DWE}			40	ns
$INT\downarrow$ delay time from $\overline{IORD}\uparrow$	t_{DRI}			40	ns
$INT\downarrow$ delay time from $\overline{IOWR}\uparrow$	t_{DWI}			40	ns
$INT\uparrow$ recovery time from $INT\downarrow$	t_{IIL}		2		t_{CYK}

SCSI bus interface

Arbitration timing

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{BSY}$↓ response time from bus free detection	t_{DBFBY}		27		t_{CYK}
$\overline{BSY}$↓ output delay time from ID output	t_{DIDBY1}		1		t_{CYK}
$\overline{SEL}$↓ output delay time from $\overline{BSY}$↓	t_{DBYSL1}		45		t_{CYK}
ID output delay time from bus free detection	t_{DBFID}		26		t_{CYK}
$\overline{SBIE}$↑ output delay time from $\overline{BSY}$↑, $\overline{SEL}$↑	t_{DBFIE}	When a differential driver is used	24		t_{CYK}
$\overline{SBIE}$↓ output delay time from IDSTR↑	t_{DSTIE}		1		t_{CYK}
BSYO↑, ID output delay time from $\overline{SBIE}$↑	t_{DIEID1}		2		t_{CYK}
IDSTR↑ output delay time from ID	t_{DIDST}		1		t_{CYK}
$\overline{BSY}$↓ output delay time from BSYO↑	t_{DBOBY1}		1		t_{CYK}
SELO↑ output delay time from $\overline{BSY}$↓	t_{DBYSO}		44		t_{CYK}
$\overline{SEL}$↓ output delay time from SELO↑	t_{DSOSL}		1		t_{CYK}

Selection timing (with initiator)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ID output delay time from $\overline{SEL}$↓	t_{DSLID1}		26		t_{CYK}
$\overline{ATN}$↓ output delay time from $\overline{SEL}$↓	t_{DSLAT1}		25		t_{CYK}
$\overline{BSY}$↑ output time from $\overline{ATN}$↓	t_{DATBY}		3		t_{CYK}
$\overline{BSY}$↓ input valid delay time from $\overline{BSY}$↑	t_{DBYBY1}		8		t_{CYK}
$\overline{SEL}$↑ response time from $\overline{BSY}$↓	t_{DBYSL2}		6		t_{CYK}
$\overline{BSY}$↑ output delay time from ID output	t_{DIDBY2}		2		t_{CYK}
INIT↑ output delay time from $\overline{SEL}$↓	t_{DSLIN1}	When a differential driver is used	24		t_{CYK}
$\overline{ATN}$ output delay time from INIT↑	t_{DINAT1}		1		t_{CYK}
$\overline{SBIE}$↑ output delay time from $\overline{SEL}$↓	t_{DSLIE1}		25		t_{CYK}
ID output delay time from $\overline{SBIE}$↑	t_{DIEID2}		1		t_{CYK}
$\overline{SBIE}$↓ output delay time from SBOE↓	t_{DOEIE1}		1		t_{CYK}
SBOE↑ output delay time from $\overline{SBIE}$↑	t_{DIEOE1}		1		t_{CYK}
SBOE↓ response time from $\overline{BSY}$↓	t_{DBYOE1}		6		t_{CYK}
IDSTR↓ output delay time from $\overline{SBIE}$↑	t_{DIEST1}		1		t_{CYK}
BSYO↓ output delay time from $\overline{BSY}$↑	t_{DBYBO1}		1		t_{CYK}
SELO↓ output delay time from $\overline{SEL}$↑	t_{DSLSO1}		1		t_{CYK}

Selection timing (with target)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{BSY}$ hold time (from $\overline{SEL}\downarrow$)	t_{HSLBY1}		0		ns
ID setup time (to $\overline{BSY}\uparrow$)	t_{SIDBY1}		0		ns
$\overline{BSY}\downarrow$ output delay time from $\overline{BSY}\uparrow$	t_{DBYBY2}		9		t_{CYK}
ID hold time (from $\overline{BSY}\downarrow$)	t_{HBYID1}		0		ns
$\overline{SEL}$ hold time (from $\overline{BSY}\downarrow$)	t_{HBYSL1}		0		ns
$\overline{ATN}$ setup time (to $\overline{SEL}\uparrow$)	t_{SATSL}		0		ns
Target output delay time from $\overline{SEL}\uparrow$	t_{DSLTG1}		3		t_{CYK}
BSYO$\uparrow$ response time from $\overline{BSY}\uparrow$	t_{DBYBO2}	When a differential driver is used	8		t_{CYK}
$\overline{BSY}\downarrow$ delay time from BSYO$\uparrow$	t_{DBOBY2}		1		t_{CYK}
TGT$\uparrow$ output response time from $\overline{SEL}\uparrow$	t_{DSLTT1}		2		t_{CYK}
Target output delay time from TGT$\uparrow$	t_{DTTTG1}		1		t_{CYK}

Reselection timing (with initiator)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{BSY}$ hold time (from $\overline{SEL}\downarrow$)	t_{HSLBY2}		0		ns
ID setup time (to $\overline{BSY}\uparrow$)	t_{SIDBY2}		0		ns
$\overline{I}$/O setup time (to $\overline{BSY}\uparrow$)	t_{SIOBY}		0		ns
$\overline{ATN}$ output delay time from $\overline{SEL}\uparrow$	t_{DSLAT2}		3		t_{CYK}
$\overline{BSY}\downarrow$ output delay time from $\overline{BSY}\uparrow$	t_{DBYBY3}		9		t_{CYK}
ID hold time (from $\overline{BSY}\downarrow$)	t_{HBYID2}		0		ns
$\overline{SEL}$ hold time (from $\overline{BSY}\downarrow$)	t_{HBYSL2}		0		ns
$\overline{BSY}\uparrow$ output delay time from $\overline{SEL}\uparrow$	t_{DSLBY}		2		t_{CYK}
BSYO$\uparrow$ response time from $\overline{BSY}\uparrow$	t_{DBYBO3}	When a differential driver is used	8		t_{CYK}
$\overline{BSY}\downarrow$ delay time from BSYO$\uparrow$	t_{DBOBY3}		1		t_{CYK}
INIT$\uparrow$ output response time from $\overline{SEL}\uparrow$	t_{DSLIN2}		2		t_{CYK}
BSYO$\downarrow$ output delay time from $\overline{BSY}\uparrow$	t_{DBYBO4}		1		t_{CYK}
$\overline{ATN}$ output delay time from INIT$\uparrow$	t_{DINAT2}		1		t_{CYK}

Reselection timing (with target)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ID output delay time from $\overline{SEL}\downarrow$	t_{DSLID2}		26		t_{CYK}
Target output delay time from $\overline{SEL}\downarrow$	t_{DSLTG2}		25		t_{CYK}
$\overline{BSY}\uparrow$ delay time from $\overline{I}$/O output	t_{DIOBY}		2		t_{CYK}

(to be continued)

(cont'd)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{BSY}$ ↓ input valid delay time from $\overline{BSY}$ ↑	t_{DBYBY4}		8		t_{CYK}
$\overline{SEL}$ ↑ delay time from $\overline{BSY}$ ↓	t_{DBYSL3}		6		t_{CYK}
$\overline{SEL}$ ↑ delay time from $\overline{BSY}$ (target) ↓	t_{DBYSL4}		3		t_{CYK}
$\overline{BSY}$ ↑ output delay time from ID output	t_{DIDBY3}		2		t_{CYK}
$\overline{I/O}$ output delay time from $\overline{SEL}$ ↓	t_{DSLIO}		25		t_{CYK}
Target output delay time from TGT ↑	t_{DTTTG2}	When a differential driver is used	1		t_{CYK}
TGT ↑ output delay time from $\overline{SEL}$ ↓	t_{DSLTT2}		24		t_{CYK}
$\overline{SBIE}$ ↑ output delay time from $\overline{SEL}$ ↓	t_{DSLIE2}		25		t_{CYK}
ID output delay time from $\overline{SBIE}$ ↑	t_{DIEID3}		1		t_{CYK}
SBOE ↑ output delay time from $\overline{SBIE}$ ↑	t_{DIEOE2}		1		t_{CYK}
IDSTR ↓ output delay time from $\overline{SBIE}$ ↑	t_{DIEST2}		1		t_{CYK}
SBOE ↓ delay time from $\overline{BSY}$ ↓	t_{DBYOE2}		3		t_{CYK}
$\overline{SBIE}$ ↓ delay time from SBOE ↓	t_{DOEIE2}		1		t_{CYK}
BSYO ↓ output delay time from $\overline{BSY}$ ↑	t_{DBYBO5}		1		t_{CYK}
BSYO ↑ response time from $\overline{BSY}$ ↓	t_{DBYBO6}		2		t_{CYK}
$\overline{BSY}$ ↓ delay time from BYSO ↑	t_{DBOBY4}		1		t_{CYK}
SELO ↓ delay time from $\overline{SEL}$ ↑	t_{DSLSO2}		1		t_{CYK}

Asynchronous mode initiator receive timing
(Data-in, status and message-in phases)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Phase input valid delay time from $\overline{SEL}$↑	t_{DSLPH1}		0		ns
Data float delay time from $\overline{I}/O$↓	t_{FIOD1}		0		ns
Phase setup time (to $\overline{REQ}$↓)	t_{SPHRQ1}		400		ns
Data setup time (to $\overline{REQ}$↓)	t_{SDRQ1}		5		ns
$\overline{ACK}$↓ output delay time from $\overline{REQ}$↓	t_{DRQAK1}		0		ns
Data hold time (from $\overline{ACK}$↓)	t_{HAKD1}		0		ns
$\overline{REQ}$ hold time (from $\overline{ACK}$↓)	t_{HAKRQ1}		0		ns
$\overline{ACK}$↑ output delay time from $\overline{REQ}$↑	t_{DRQAK2}		0		ns
Phase hold time (from $\overline{ACK}$↑)	t_{HAKPH1}		0		ns
SBOE↓ output delay time from $\overline{I}/O$↓	t_{DIOOE1}	When a differential driver is used	0		ns
$\overline{SBIE}$↓ output delay time from SBOE↓	t_{DOEIE3}		1		t_{CYK}

Asynchronous mode target transmit timing
(Data-in, status and message-in phases)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Phase output delay time from $\overline{SEL}$ ↑	t_{DSLPH2}		2		t_{CYK}
Data output delay time from $\overline{I}/O$ ↓	t_{DIOD1}		1		t_{CYK}
Phase setup time (to $\overline{REQ}$ ↓)	t_{SPHRQ2}		8		t_{CYK}
Data setup time (to $\overline{REQ}$ ↓)	t_{SDRQ2}		55		ns
$\overline{ACK}$ ↓ input valid delay time from $\overline{REQ}$ ↓	t_{DRQAK3}		0		ns
$\overline{REQ}$ ↑ output delay time from $\overline{ACK}$ ↓	t_{DAKRQ1}		0		ns
Data hold time (from $\overline{ACK}$ ↓)	t_{HAKD2}		0		ns
$\overline{ACK}$ hold time (from $\overline{REQ}$ ↑)	t_{HRQAK1}		0		ns
$\overline{REQ}$ ↓ output time from $\overline{ACK}$ ↑	t_{DAKRQ2}		55		ns
Phase hold time (from $\overline{ACK}$ ↑)	t_{HAKPH2}		2		t_{CYK}
$\overline{SBIE}$ ↑ output delay time from $\overline{I}/O$ ↓	t_{DIOIE1}	When a differential driver is used	0		ns
SBOE ↑ output delay time from $\overline{SBIE}$ ↑	t_{DIEOE3}		1		t_{CYK}

Asynchronous mode initiator transmit timing
(Data-in, status and message-in phases)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Phase input valid delay time from $\overline{SEL}$↑	t_{DSLPH3}		0		ns
Data output delay time from $\overline{I/O}$↑	t_{DIOD2}		3		t_{CYK}
Phase setup time (to $\overline{REQ}$↓)	t_{SPHRQ3}		400		ns
Data setup time (to $\overline{ACK}$↓)	t_{SDAK1}		55		ns
$\overline{ACK}$↓ output delay time from $\overline{REQ}$↓	t_{DRQAK4}		55		ns
Data hold time (from $\overline{REQ}$↑)	t_{HRQD1}		0		ns
$\overline{REQ}$ hold time (from $\overline{ACK}$↓)	t_{HAKRQ2}		0		ns
$\overline{ACK}$↑ output delay time from $\overline{REQ}$↑	t_{DRQAK5}		0		ns
Phase hold time (from $\overline{ACK}$↑)	t_{HAKPH3}		0		ns
$\overline{SBIE}$↑ output delay time from $\overline{I/O}$↑	t_{DIOIE2}	When a differential driver is used	2		t_{CYK}
SBOE↑ output delay time from $\overline{SBIE}$↑	t_{DIEOE4}		1		t_{CYK}

Asynchronous mode target receive timing
(Data-in, status and message-in phases)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Phase output response time from $\overline{SEL}\uparrow$	t_{DSLPH4}		2		t_{CYK}
Data float delay time from $\overline{I/O}\uparrow$	t_{FIOD2}		0		ns
Phase setup time (to $\overline{REQ}\downarrow$)	t_{SPHRQ4}		8		t_{CYK}
Data setup time (to $\overline{ACK}\downarrow$)	t_{SDAK2}		5		ns
$\overline{ACK}\downarrow$ input valid delay time from $\overline{REQ}\downarrow$	t_{DRQAK6}		0		ns
$\overline{REQ}\uparrow$ output delay time from $\overline{ACK}\downarrow$	t_{DAKRQ3}		0		ns
Data hold time (from $\overline{REQ}\uparrow$)	t_{HRQD2}		0		ns
$\overline{ACK}$ hold time (from $\overline{REQ}\uparrow$)	t_{HRQAK2}		0		ns
$\overline{REQ}\downarrow$ output delay time from $\overline{ACK}\uparrow$	t_{DAKRQ4}		0		ns
Phase hold time (from $\overline{ACK}\uparrow$)	t_{HAKPH4}		2		t_{CYK}
$\overline{SBIE}\downarrow$ output delay time from SBOE$\downarrow$	t_{DOEIE4}	When a differential driver is used	1		t_{CYK}
SBOE$\downarrow$ output delay time from $\overline{I/O}\uparrow$	t_{DIOOE2}		0		ns

Synchronous mode initiator receive timing (Data-in phase)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Phase input valid delay time from $\overline{SEL}$ ↑	t_{DSLPH5}		0		ns
Data float delay time from $\overline{I}/O$ ↓	t_{FIOD3}		0		ns
Phase setup time (to $\overline{REQ}$ ↓)	t_{SPHRQ5}		400		ns
Data setup time (to $\overline{REQ}$ ↓)	t_{SDRQ3}		5		ns
Data hold time (from $\overline{REQ}$ ↓)	t_{HRQD3}		5		ns
$\overline{REQ}$ input low-level width	t_{RQRQL1}		50		ns
$\overline{REQ}$ ↓ recovery time from $\overline{REQ}$ ↑	t_{RVRQ1}		2		t_{CYK}
$\overline{REQ}$ input cycle time	t_{RQCY1}		4		t_{CYK}
$\overline{ACK}$ output low-level width	t_{AKAKL1}		2		t_{CYK}
Phase hold time (from $\overline{ACK}$ ↑)	t_{HAKPH5}		0		ns
$\overline{ACK}$ ↓ recovery time from $\overline{ACK}$ ↑	t_{RVAK1}		2 to 16		t_{CYK}
SBOE ↓ output delay time from $\overline{I}/O$ ↓	t_{DIOOE3}	When a differential driver is used	0		ns
$\overline{SBIE}$ ↓ output delay time from SBOE ↓	t_{DOEIE5}		1		t_{CYK}

Synchronous mode target transmit timing (Data-in phase)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Phase output delay time from $\overline{SEL}\uparrow$	t_{DSLPH6}		2		t_{CYK}
Data output delay time from $\overline{I}/O\downarrow$	t_{DIOD3}		1		t_{CYK}
Phase setup time (to $\overline{REQ}\downarrow$)	t_{SPHRQ6}		8		t_{CYK}
Data setup time (to $\overline{REQ}\downarrow$)	t_{SDRQ4}		55		ns
Data hold time (from $\overline{REQ}\downarrow$)	t_{HRQD4}		2		t_{CYK}
$\overline{REQ}$ output low-level width	t_{RQRQL2}		2		t_{CYK}
$\overline{ACK}$ input low-level width	t_{AKAKL2}		50		ns
$\overline{ACK}\downarrow$ recovery time from $\overline{ACK}\uparrow$	t_{RVAK2}		2		t_{CYK}
$\overline{ACK}$ input cycle time	t_{AKCY1}		4		t_{CYK}
Phase hold time (from $\overline{ACK}\uparrow$)	t_{HAKPH6}		1		t_{CYK}
$\overline{REQ}\downarrow$ recovery time from $\overline{REQ}\uparrow$	t_{RVRQ2}		2 to 16		t_{CYK}
$\overline{SBIE}\uparrow$ output delay time from $\overline{I}/O\downarrow$	t_{DIOIE3}	When a differential driver is used	0		ns
SBOE $\uparrow$ output delay time from $\overline{SBIE}\uparrow$	t_{DIEOE5}		1		t_{CYK}

Synchronous mode initiator transmit timing (Data-out phase)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Phase input valid delay time from $\overline{SEL}$↑	t_{DSLPH7}		0		ns
Data output delay time from $\overline{I}/O$↑	t_{DIOD4}		3		t_{CYK}
Phase setup time (to $\overline{REQ}$↓)	t_{SPHRQ7}		400		ns
Data setup time (to $\overline{ACK}$↓)	t_{SDAK3}		55		ns
Data hold time (from $\overline{ACK}$↓)	t_{HAKD3}		2		t_{CYK}
$\overline{REQ}$ input low-level width	t_{RQRQL3}		50		ns
$\overline{REQ}$↓ recovery time from $\overline{REQ}$↑	t_{RVRQ3}		2		t_{CYK}
$\overline{REQ}$ input cycle time	t_{RQCY2}		4		t_{CYK}
$\overline{ACK}$ output low-level width	t_{AKAKL3}		2		t_{CYK}
Phase hold time (from $\overline{ACK}$↑)	t_{HAKPH7}		0		ns
$\overline{ACK}$↓ recovery time from $\overline{ACK}$↑	t_{RVAK3}		2 to 16		t_{CYK}
$\overline{SBIE}$↑ output delay time from $\overline{I}/O$↑	t_{DIOIE4}	When a differential driver is used	2		t_{CYK}
SBOE↑ output delay time from $\overline{SBIE}$↑	t_{DIEOE6}		1		t_{CYK}

Synchronous mode target receive timing (Data-out phase)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Phase output delay time from $\overline{SEL}\uparrow$	t_{DSLPH8}		2		t_{CYK}
Data float delay time from $\overline{I}/O\uparrow$	t_{FIOD4}		0		ns
Phase setup time (from $\overline{REQ}\downarrow$)	t_{SPHRQ8}		8		t_{CYK}
Data setup time (to $\overline{ACK}\downarrow$)	t_{SDAK4}		5		ns
Data hold time (from $\overline{ACK}\downarrow$)	t_{HAKD4}		5		ns
$\overline{REQ}$ output low-level width	t_{RQRQL4}		2		t_{CYK}
$\overline{ACK}$ input low-level width	t_{AKAKL4}		50		ns
$\overline{ACK}\downarrow$ recovery time from $\overline{ACK}\uparrow$	t_{RVAK4}		2		t_{CYK}
$\overline{ACK}$ input cycle time	t_{AKCY2}		4		t_{CYK}
Phase hold time (from $\overline{ACK}\uparrow$)	t_{HAKPH8}		1		t_{CYK}
$\overline{REQ}\downarrow$ recovery time from $\overline{REQ}\uparrow$	t_{RVRQ4}		2 to 16		t_{CYK}
SBOE$\downarrow$ output delay time from $\overline{I}/O\uparrow$	t_{DIOOE4}	When a differential driver is used	0		ns
$\overline{SBIE}\downarrow$ output delay time from SBOE$\downarrow$	t_{DOEIE6}		1		t_{CYK}

High-speed synchronous mode initiator receive timing (Data-in phase)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Phase input valid delay time from $\overline{SEL}$ ↑	t_{DSLPH9}		0		ns
Data float delay time from $\overline{I}/O$ ↓	t_{FIOD5}		0		ns
Phase setup time (to $\overline{REQ}$↓)	t_{SPHRQ9}		400		ns
Data setup time (to $\overline{REQ}$↓)	t_{SDRQ5}		5		ns
Data hold time (from $\overline{REQ}$ ↓)	t_{HRQD5}		5		ns
$\overline{REQ}$ input low-level width	t_{RQRQL5}		30		ns
$\overline{REQ}$↓ recovery time from $\overline{REQ}$↑	t_{RVRQ5}		1		t_{CYK}
$\overline{REQ}$ input cycle time	t_{RQCY3}		2		t_{CYK}
$\overline{ACK}$ output low-level width	t_{AKAKL5}		1		t_{CYK}
Phase hold time (from $\overline{ACK}$↑)	t_{HAKPH9}		0		ns
$\overline{ACK}$↓ recovery time from $\overline{ACK}$↑	t_{RVAK5}		1 to 8		t_{CYK}
SBOE↓ output delay time from $\overline{I}/O$↓	t_{DIOOE5}	When a differential driver is used	0		ns
$\overline{SBIE}$↓ output delay time from SBOE↓	t_{DOEIE7}		1		t_{CYK}

High-speed synchronous mode target transmit timing (Data-in phase)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Phase output delay time from $\overline{SEL}$↑	$t_{DSLPH10}$		2		t_{CYK}
Data output delay time from $\overline{I/O}$↓	t_{DIOD5}		1		t_{CYK}
Phase setup time (to $\overline{REQ}$↓)	$t_{SPHRQ10}$		8		t_{CYK}
Data setup time (to $\overline{REQ}$↓)	t_{SDRQ6}		25		ns
Data hold time (from $\overline{REQ}$↓)	t_{HRQD6}		1		t_{CYK}
$\overline{REQ}$ output low-level width	t_{RQRQL6}		1		t_{CYK}
$\overline{ACK}$ input low-level width	t_{AKAKL6}		30		ns
$\overline{ACK}$↓ recovery from $\overline{ACK}$↑	t_{RVAK6}		1		t_{CYK}
$\overline{ACK}$ input cycle time	t_{AKCY3}		2		t_{CYK}
Phase hold time (from $\overline{ACK}$↑)	$t_{HAKPH10}$		1		t_{CYK}
$\overline{REQ}$↓ recovery time from $\overline{REQ}$↑	t_{RVRQ6}		1 to 8		t_{CYK}
$\overline{SBIE}$↑ output delay time from $\overline{I/O}$↓	t_{DIOIE5}	When a differential driver is used	0		ns
SBOE↑ output delay time from $\overline{SBIE}$↑	t_{DIEOE7}		1		t_{CYK}

High-speed synchronous mode initiator transmit timing (Data-out phase)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Phase input valid delay time from $\overline{SEL}$↑	$t_{DSLPH11}$		0		ns
Data output delay time from $\overline{I}/O$↑	t_{DIOD6}		3		t_{CYK}
Phase setup time (to $\overline{REQ}$↓)	$t_{SPHRQ11}$		400		ns
Data setup time (to $\overline{ACK}$↓)	t_{SDAK5}		25		ns
Data hold time (from $\overline{ACK}$↓)	t_{HAKD5}		1		t_{CYK}
$\overline{REQ}$ input low-level width	t_{RQRQL7}		30		ns
$\overline{REQ}$↓ recovery time from $\overline{REQ}$↑	t_{RVRQ7}		1		t_{CYK}
$\overline{REQ}$ input cycle time	t_{RQCY4}		2		t_{CYK}
$\overline{ACK}$ output low-level width	t_{AKAKL7}		1		t_{CYK}
Phase hold time (from $\overline{ACK}$↑)	$t_{HAKPH11}$		0		ns
$\overline{ACK}$↓ recovery time from $\overline{ACK}$↑	t_{RVAK7}		1 to 8		t_{CYK}
$\overline{SBIE}$↑ output delay time from $\overline{I}/O$↑	t_{DIOIE6}	When a differential driver is used	2		t_{CYK}
SBOE↑ output delay time from $\overline{SBIE}$↑	t_{DIEOE8}		1		t_{CYK}

High-speed synchronous mode target receive timing (Data-out phase)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Phase output delay time from $\overline{SEL}\uparrow$	$t_{DSLPH12}$		2		t_{CYK}
Data float delay time from $\overline{I}/O\uparrow$	t_{FIOD6}		0		ns
Phase setup time (to $\overline{REQ}\downarrow$)	$t_{SPHRQ12}$		8		t_{CYK}
Data setup time (to $\overline{ACK}\downarrow$)	t_{SDAK6}		5		ns
Data hold time (from $\overline{ACK}\downarrow$)	t_{HAKD6}		5		ns
$\overline{REQ}$ output low-level width	t_{RQRQL8}		1		t_{CYK}
$\overline{ACK}$ input low-level width	t_{AKAKL8}		30		ns
$\overline{ACK}\downarrow$ recovery time from $\overline{ACK}\uparrow$	t_{RVAK8}		1		t_{CYK}
$\overline{ACK}$ input cycle time	t_{AKCY4}		2		t_{CYK}
Phase hold time (from $\overline{ACK}\uparrow$)	$t_{HAKPH12}$		1		t_{CYK}
$\overline{REQ}\downarrow$ recovery time from $\overline{REQ}\uparrow$	t_{RVRQ8}		1 to 8		t_{CYK}
SBOE$\downarrow$ output delay time from $\overline{I}/O\uparrow$	t_{DIOOE6}	When a differential driver is used	0		ns
$\overline{SBIE}\downarrow$ output delay time from SBOE$\downarrow$	t_{DOEIE8}		1		t_{CYK}

Selection/reselection → Bus free

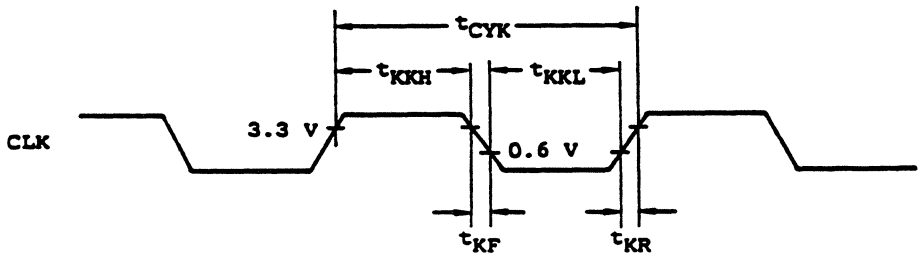
Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{SEL}$↑ delay time from ID float	t_{DIDSL}		4096		t_{CYK}
Control float delay time from $\overline{SEL}$↑	t_{FSLCTL}		0		ns
$\overline{SELO}$↓ delay time from $\overline{SEL}$↑	t_{DSLSO3}	When a differential driver is used	1		t_{CYK}
$\overline{INIT}$↓ delay time from control float	t_{DCTLIN}		1		t_{CYK}
$\overline{SBOE}$↓ delay time from ID float	t_{DIDOE}		0		ns
$\overline{SBIE}$↓ delay time from $\overline{SBOE}$↓	t_{DOEIE9}		1		t_{CYK}

AC Timing Test Points (except CLK)

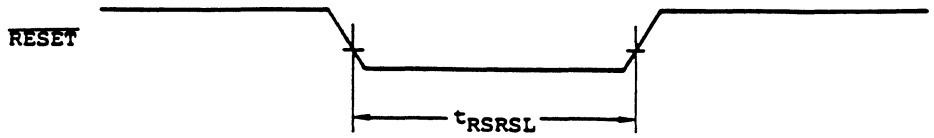
(a) CPU bus interface pin

(b) SCSI bus interface pin

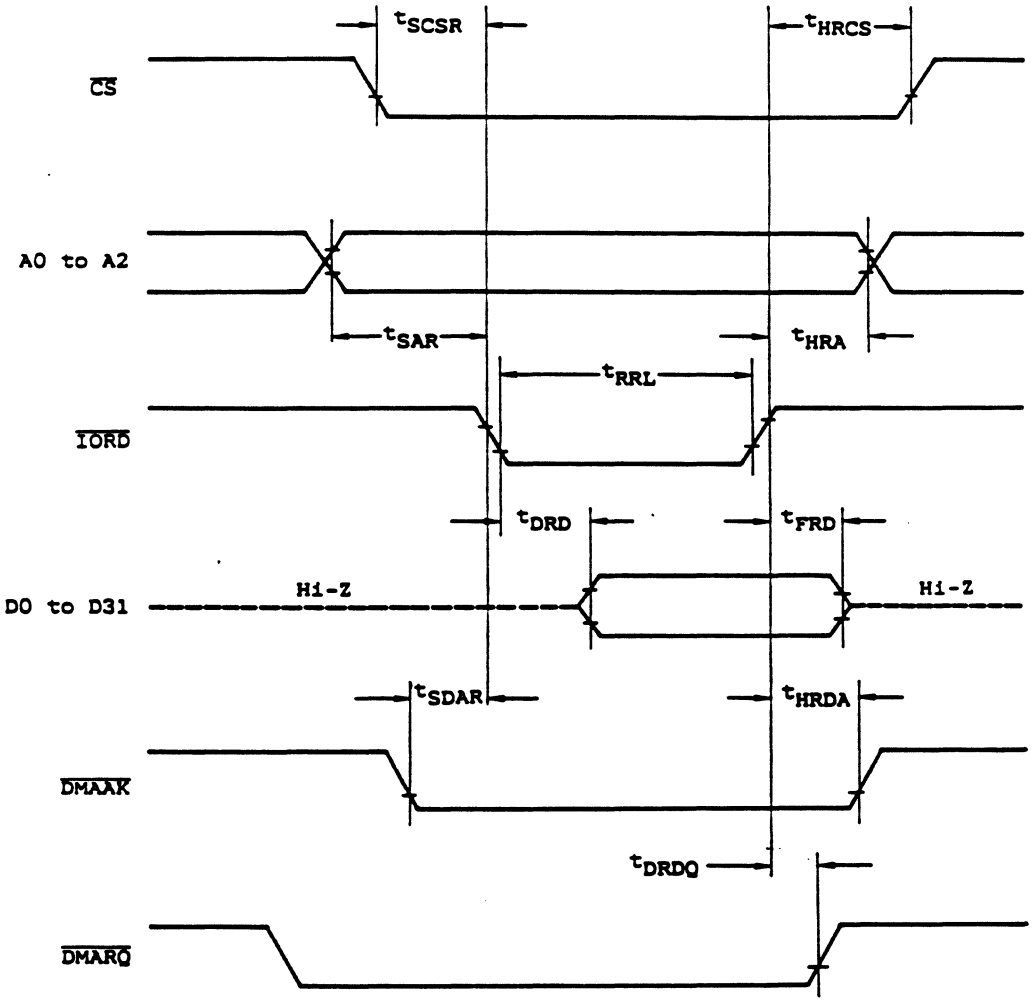
Clock Timing



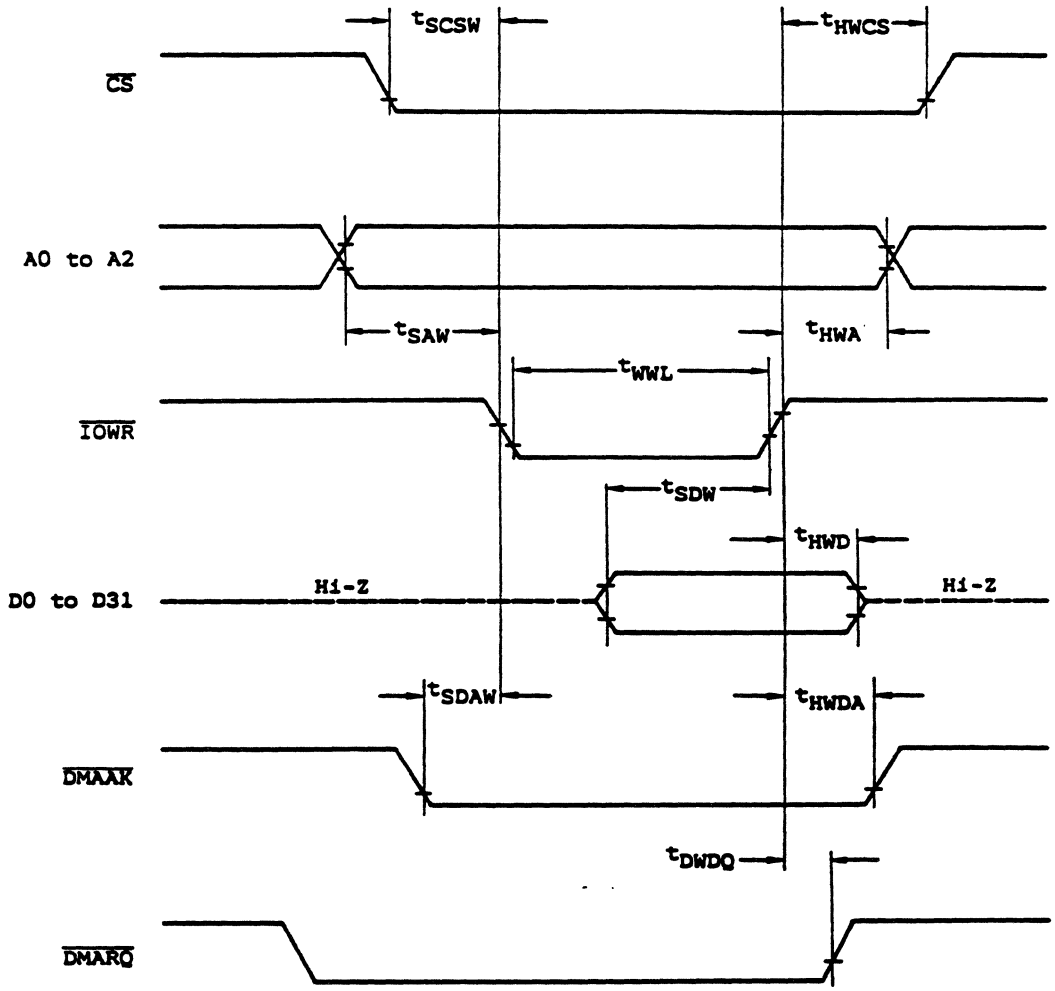
Reset Timing



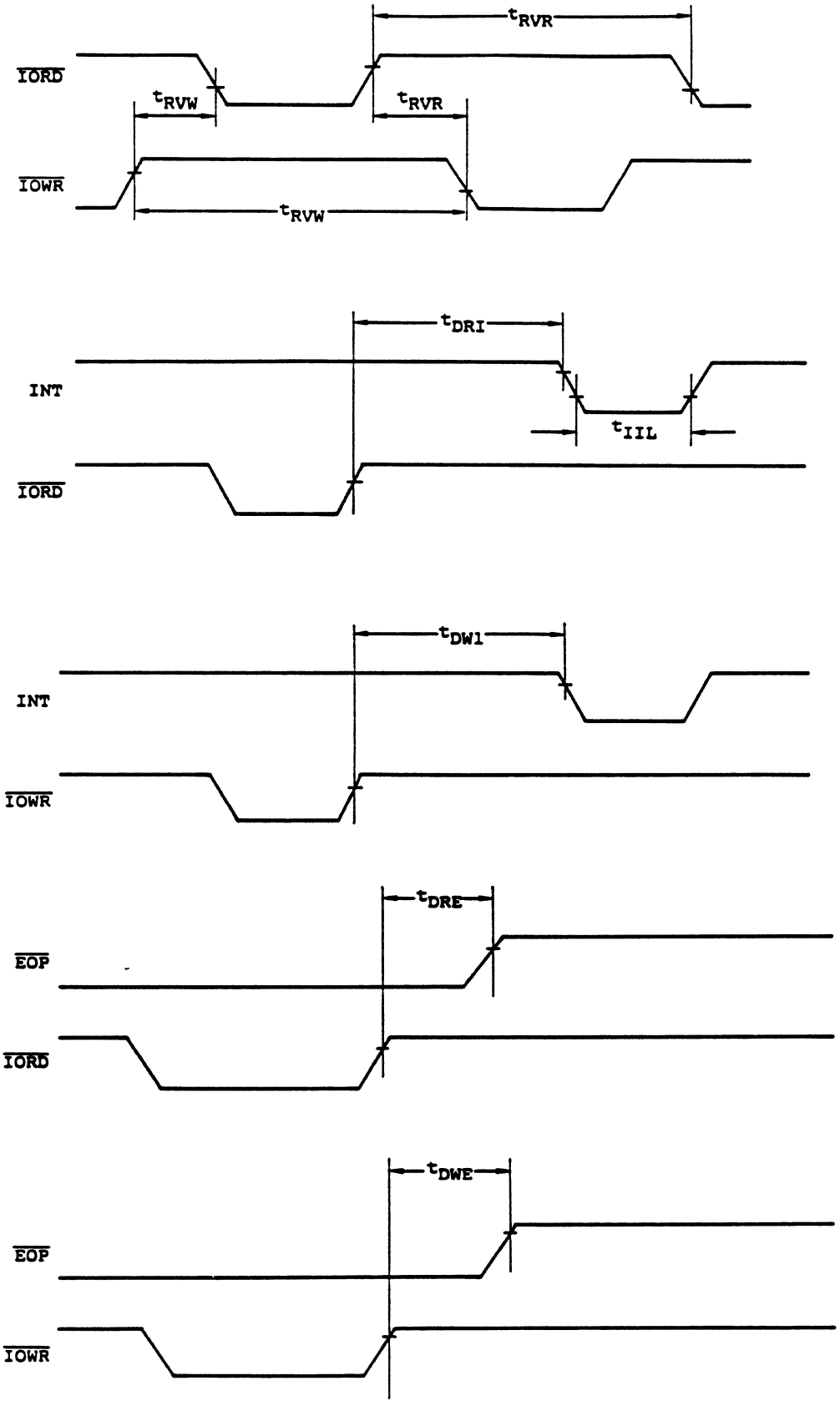
CPU Bus Read Timings



CPU Bus Write Timings

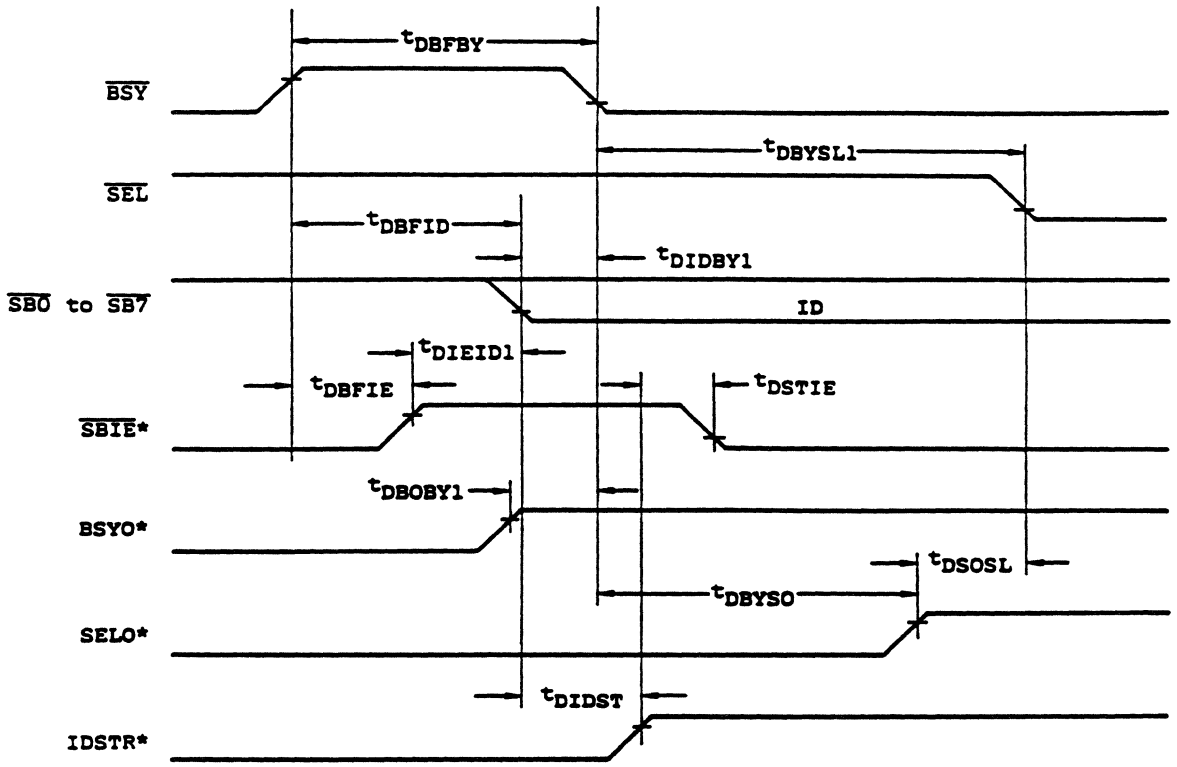


Other CPU Bus Timings



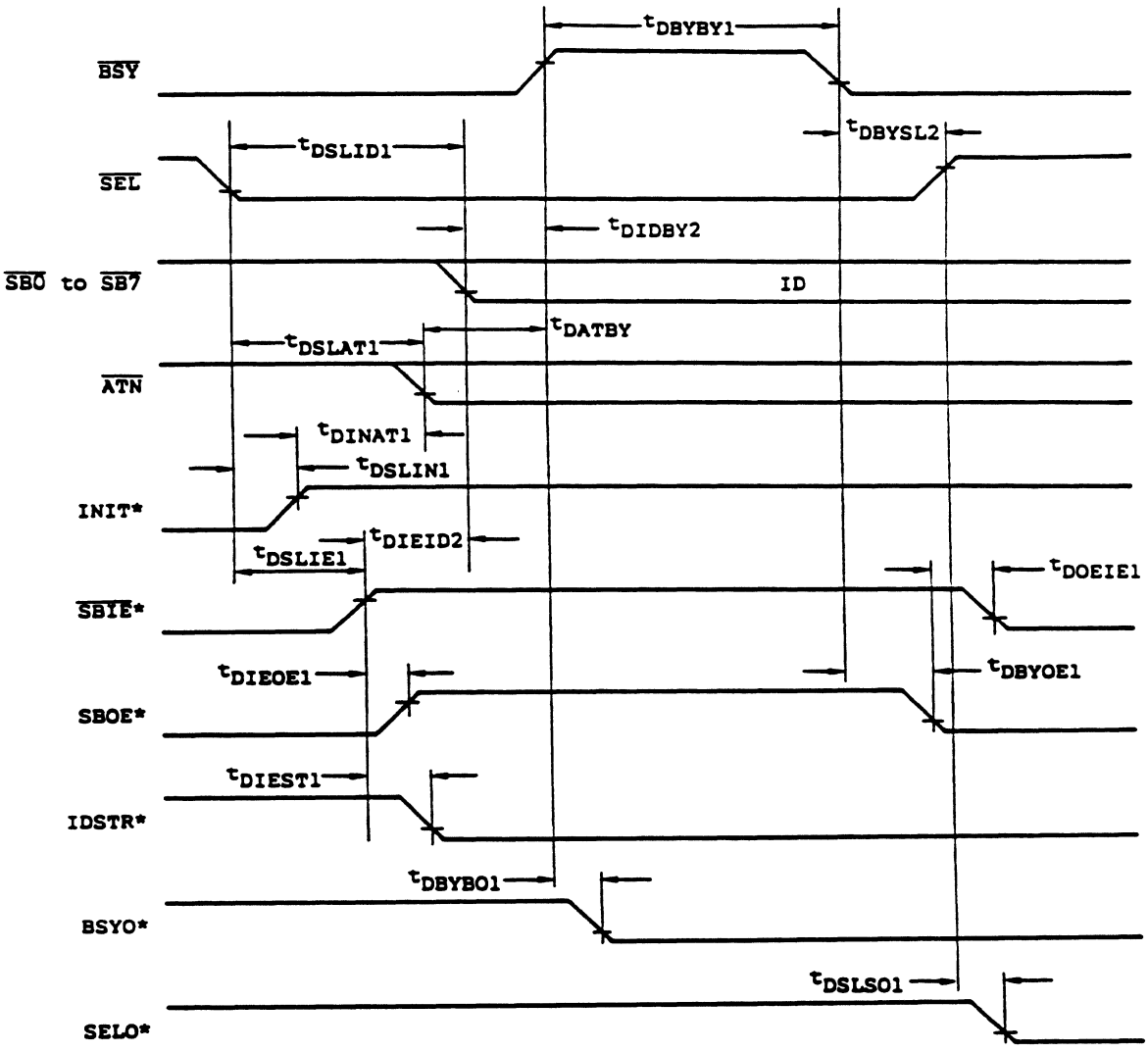
SCSI Bus Timings:

Arbitration



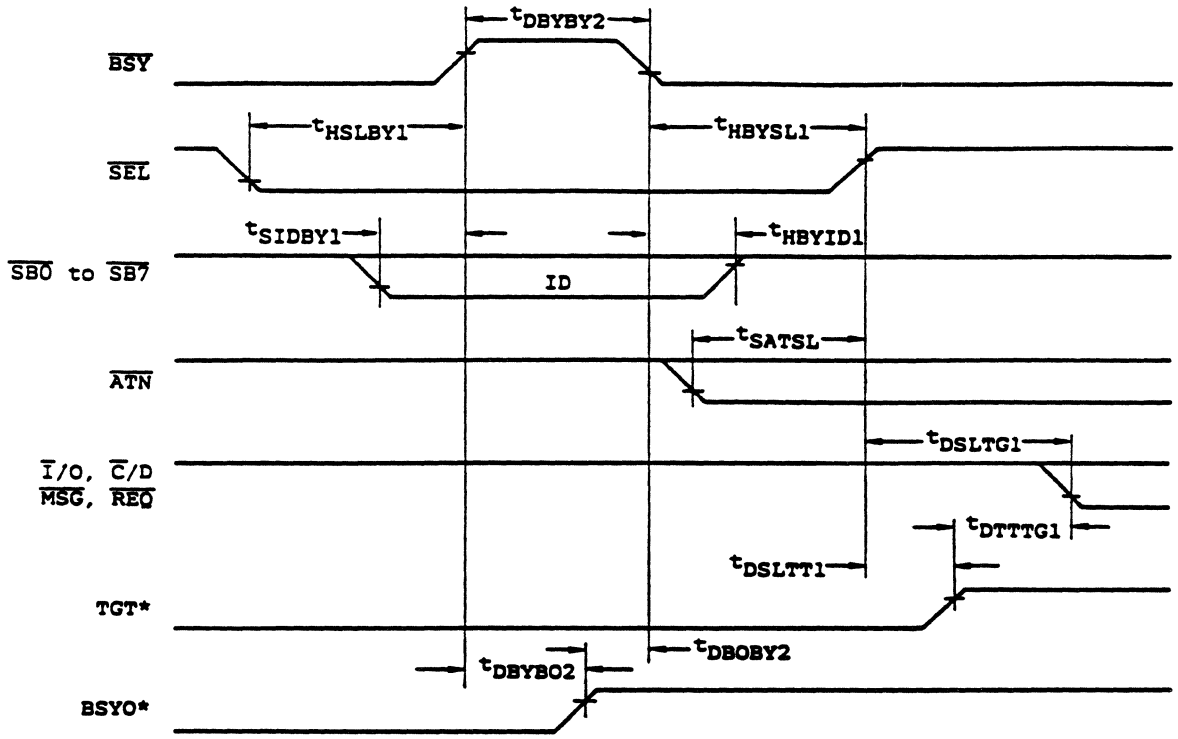
*: Differential driver control signal

Selection (initiator)



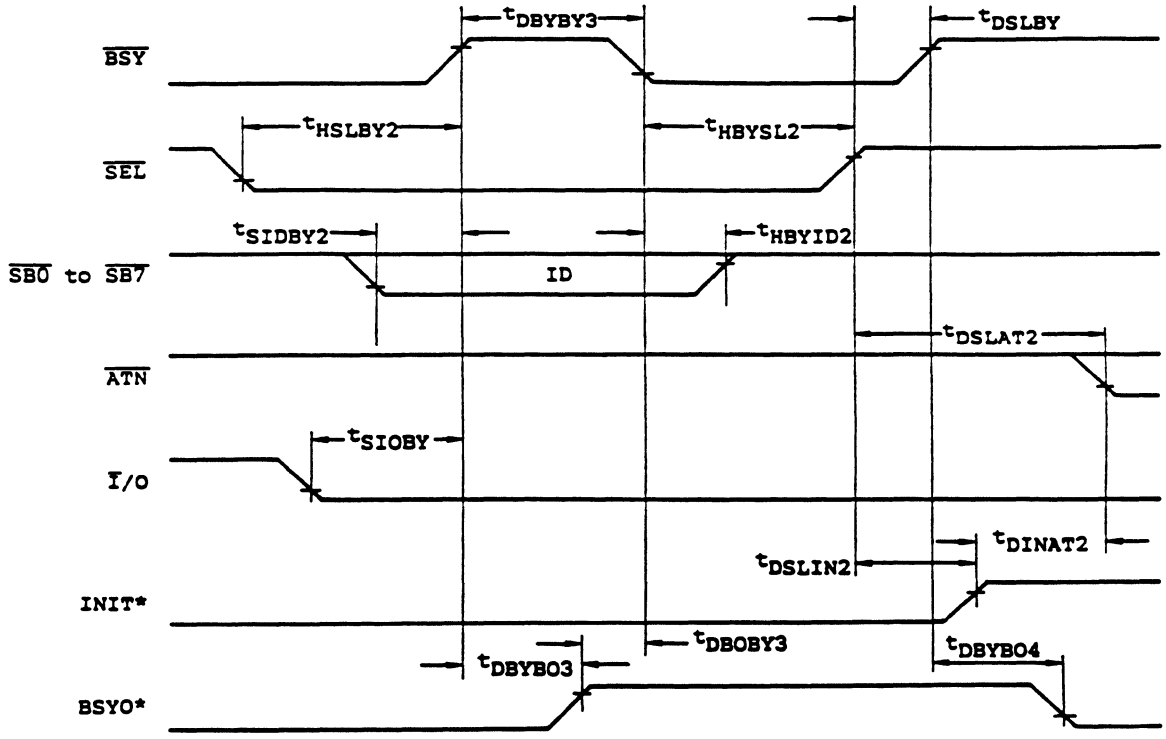
*: Differential driver control signal

Selection (target)



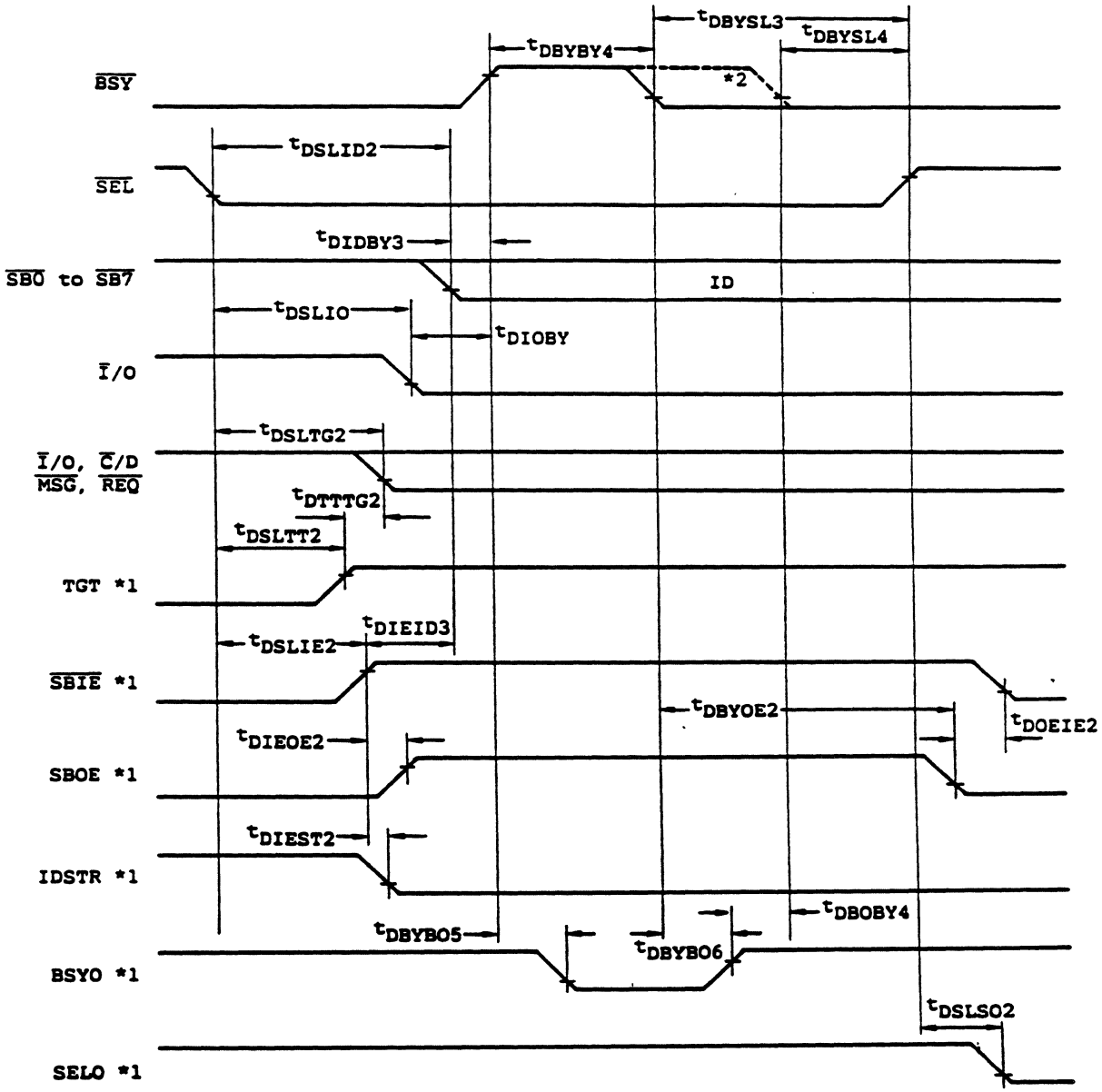
*: Differential driver control signal

Reselection (initiator)



*: Differential driver control signal

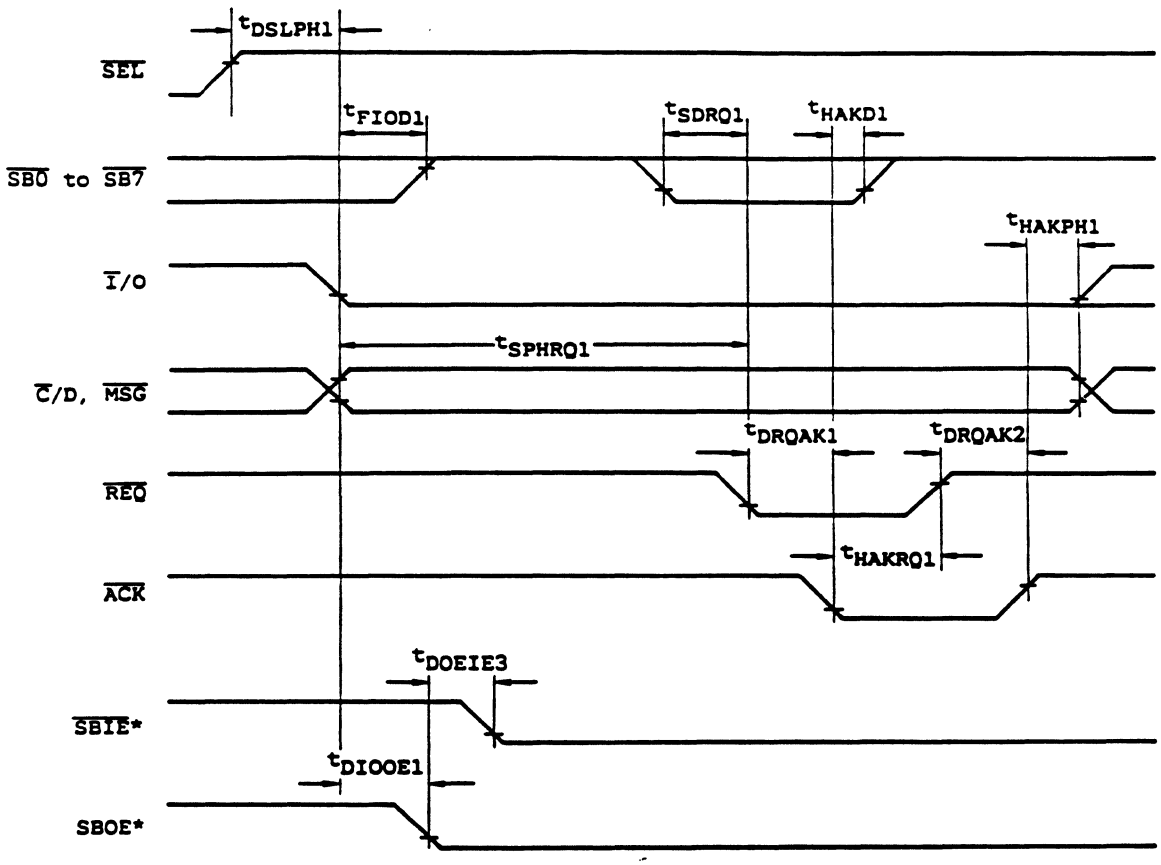
Reselection (target)



*1: Differential driver control signal

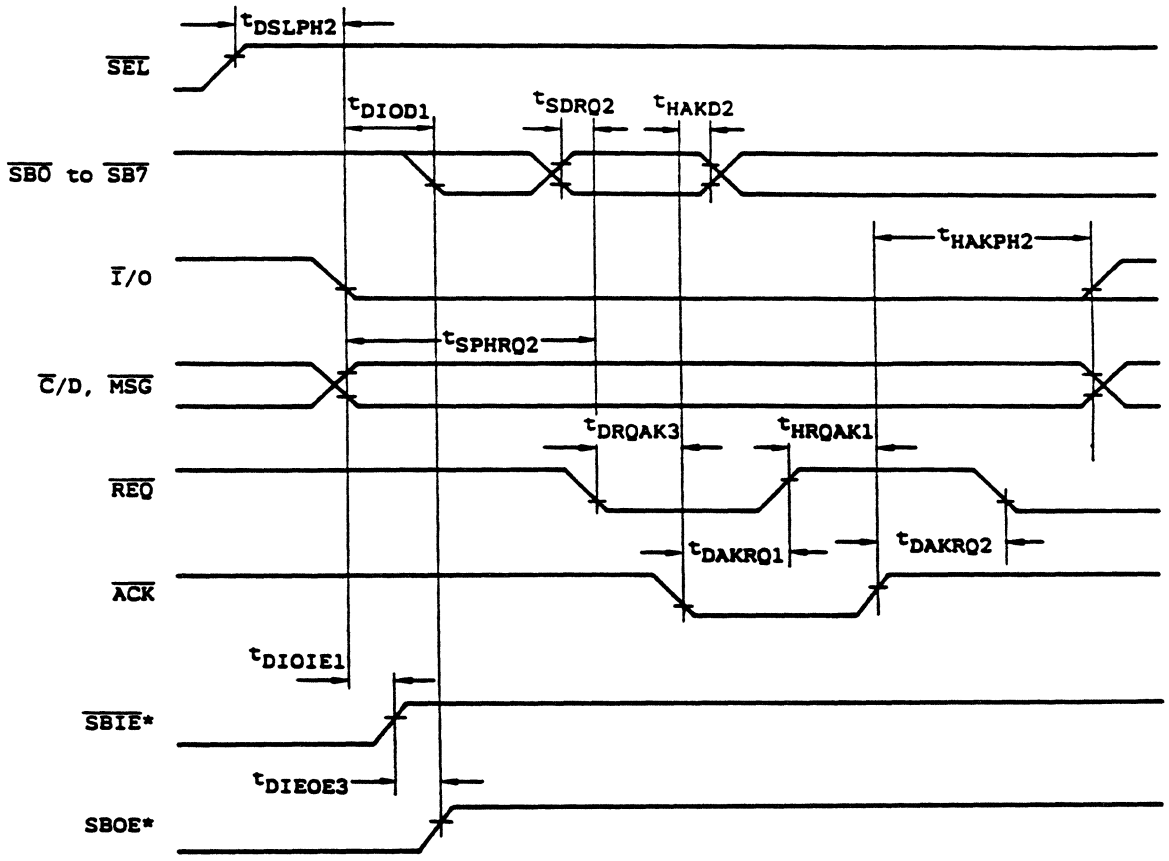
2: Target output

Asynchronous mode initiator reception
(data-in, status and message-in phases)



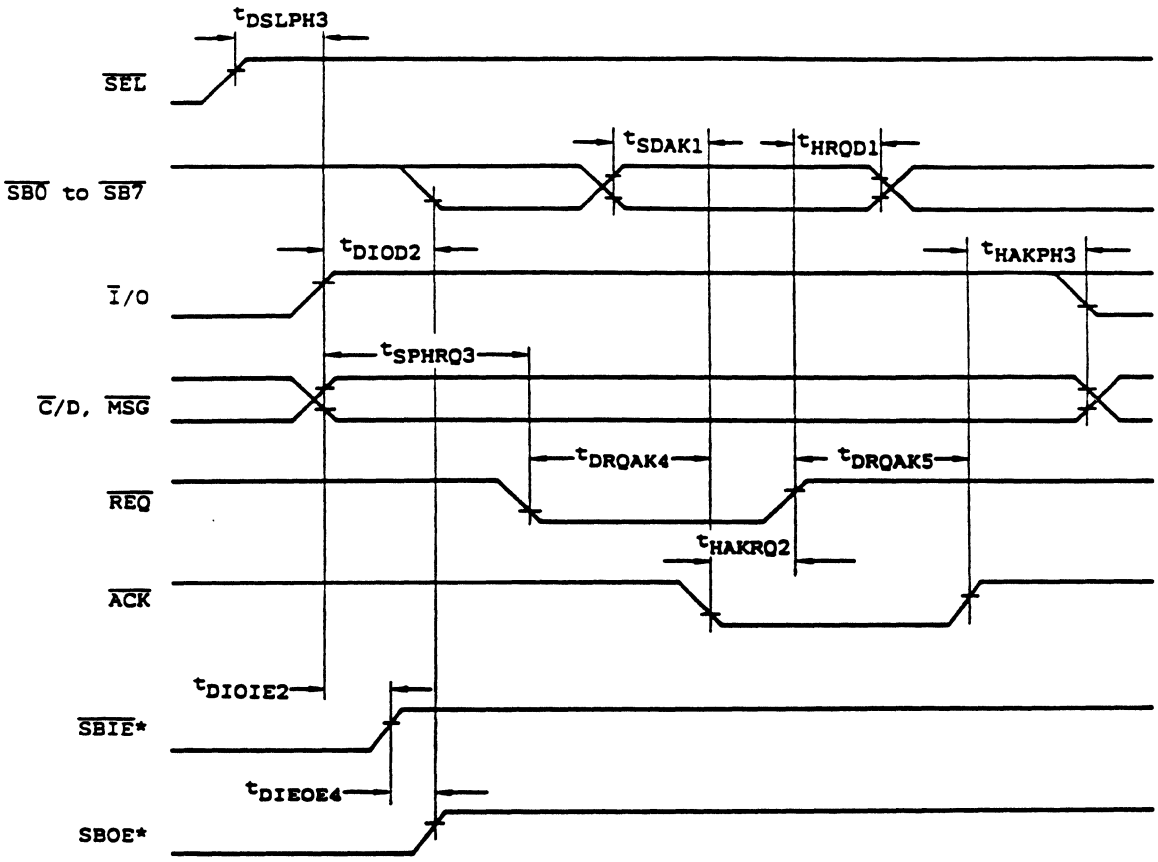
*: Differential driver control signal

Asynchronous mode target transmission
(data-in, status and message-in phases)



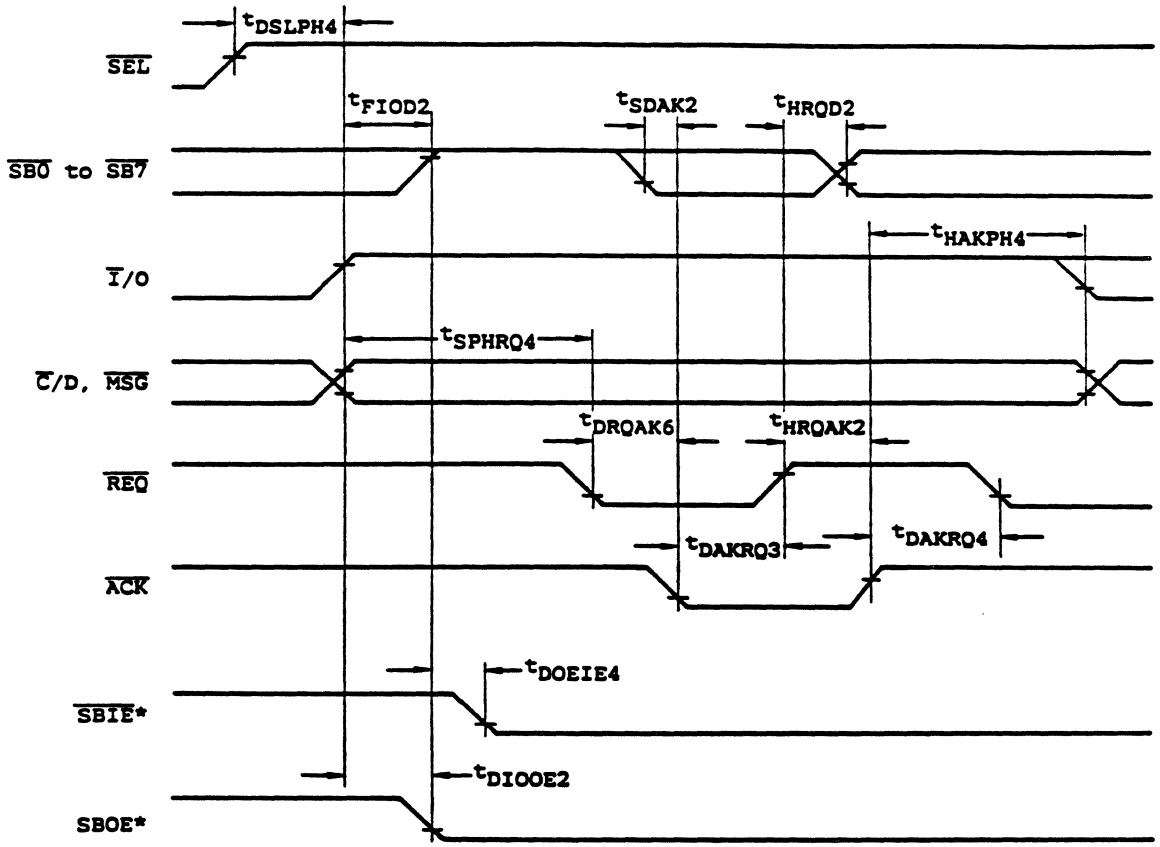
*: Differential driver control signal

Asynchronous mode initiator transmission
(data-in, status and message-in phases)



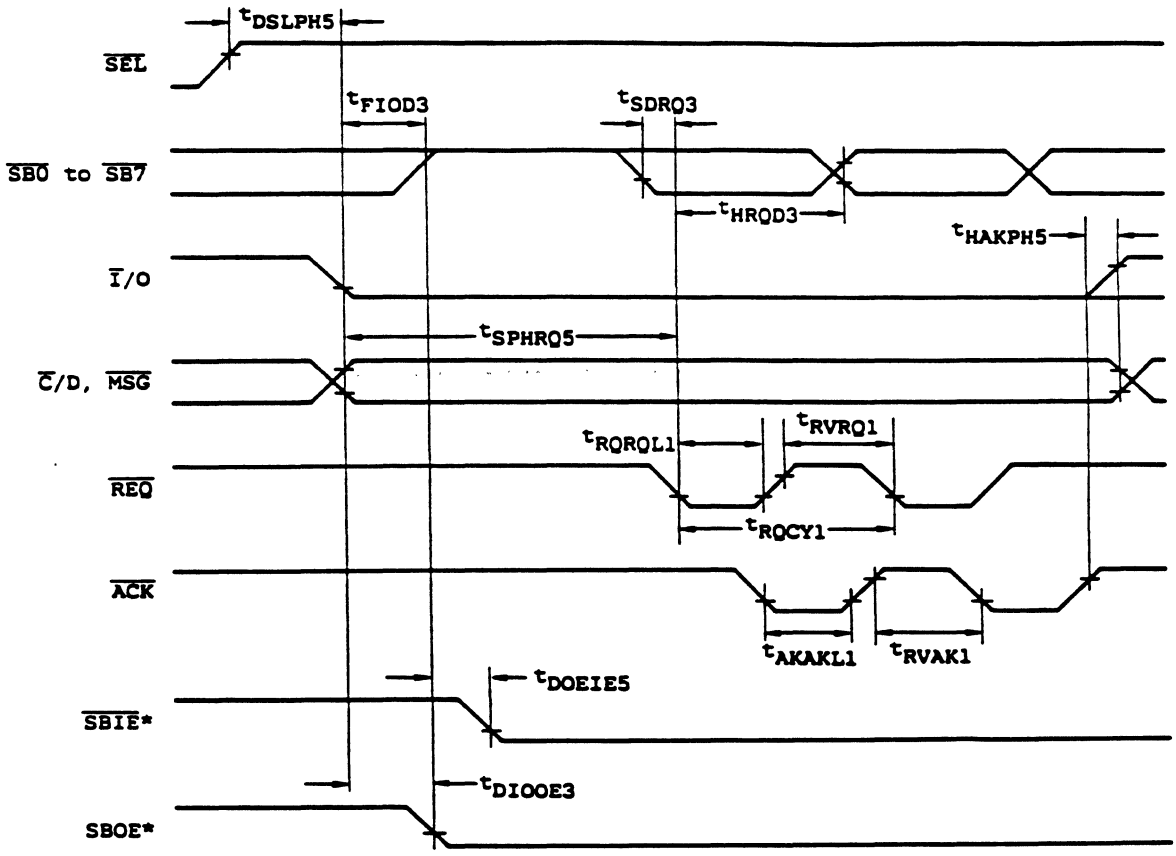
*: Differential driver control signal

Asynchronous mode target reception
(data-in, status and message-in phases)



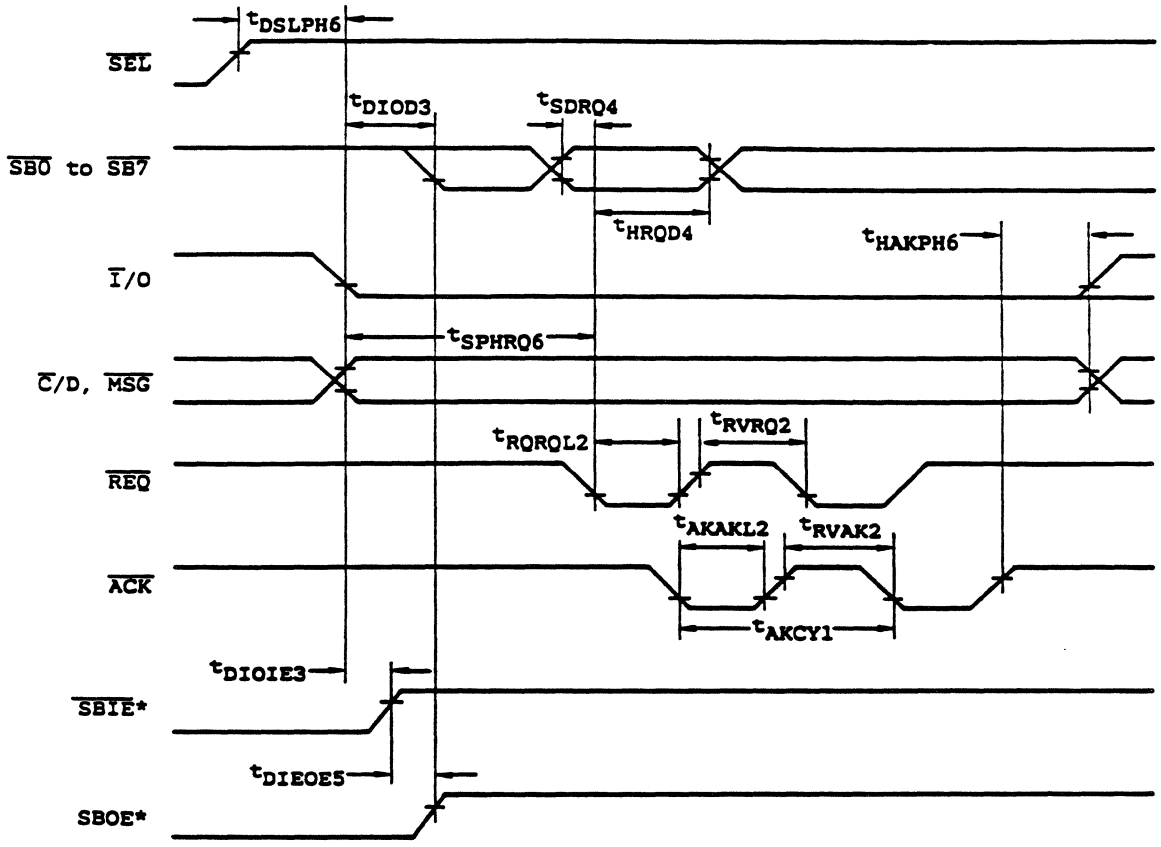
*: Differential driver control signal

Synchronous mode initiator reception (data-in phase)



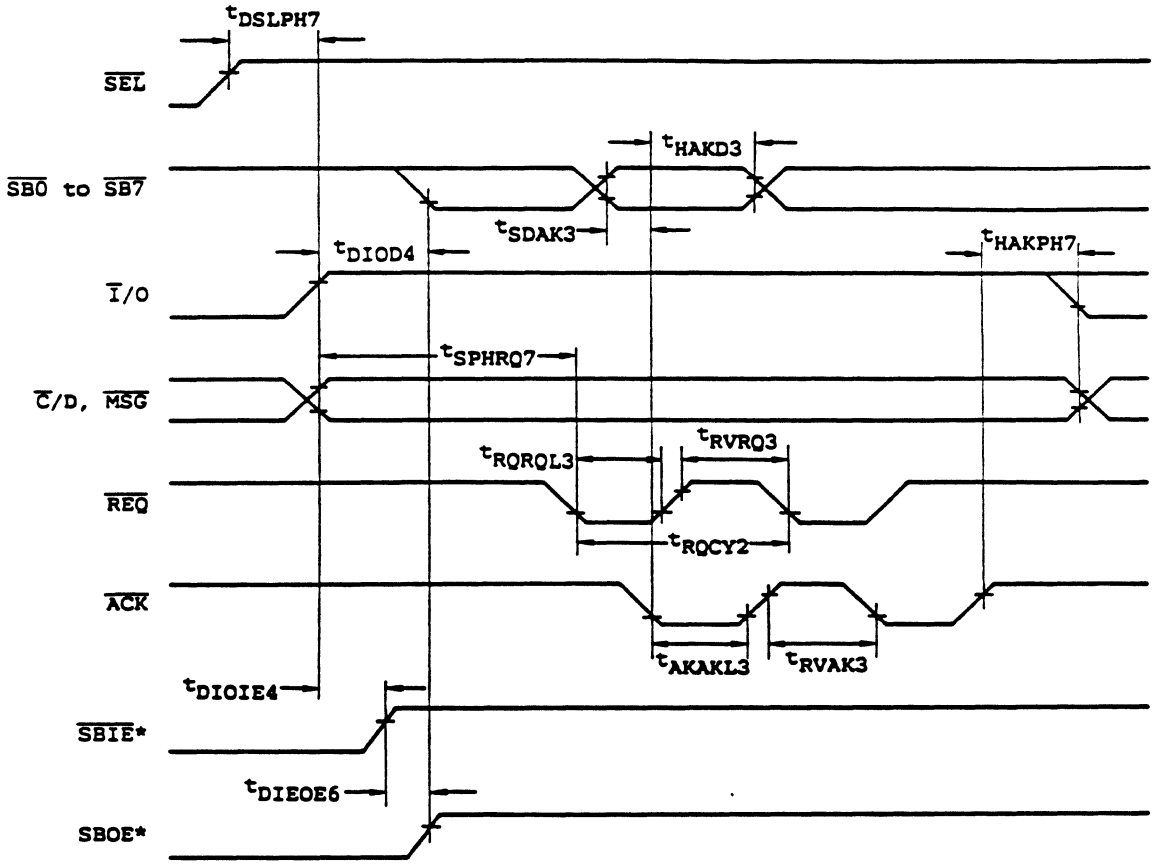
*: Differential driver control signal

Synchronous mode target transmission (data-in phase)



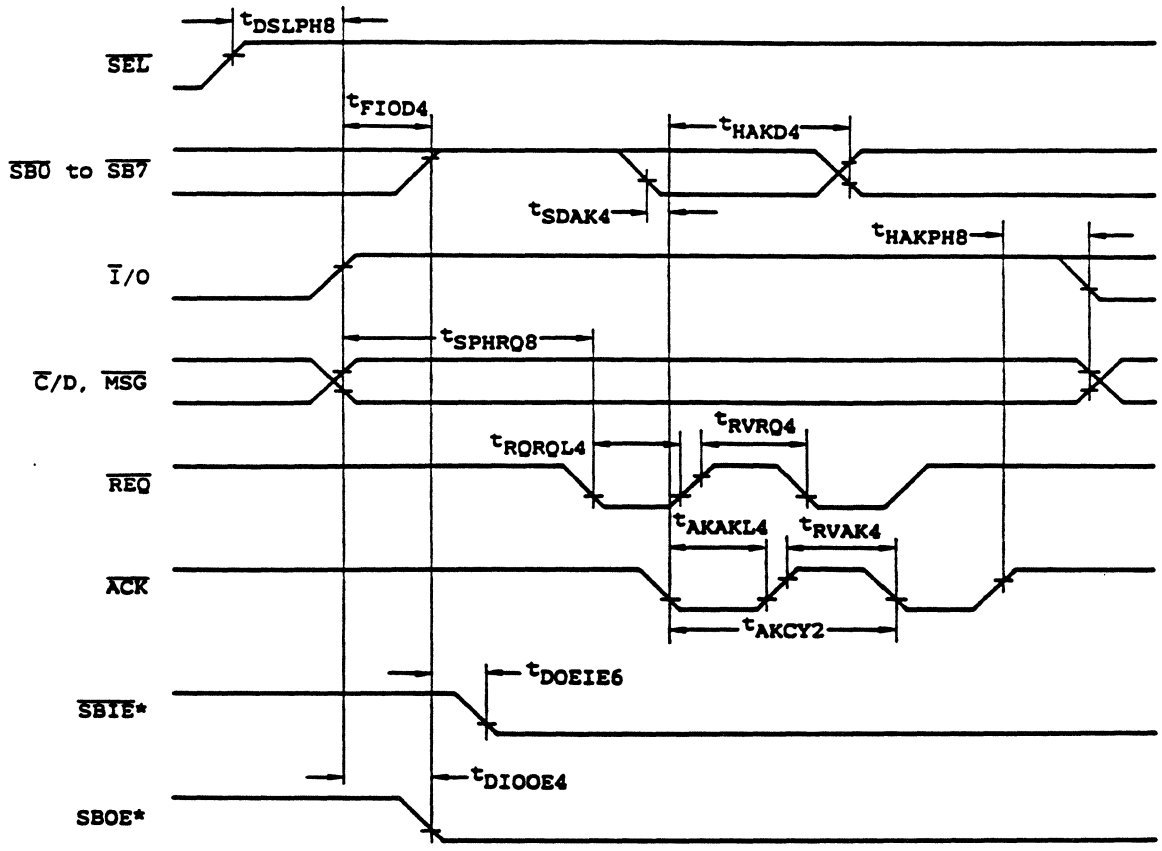
*: Differential driver control signal

Synchronous mode initiator transmission (data-out phase)



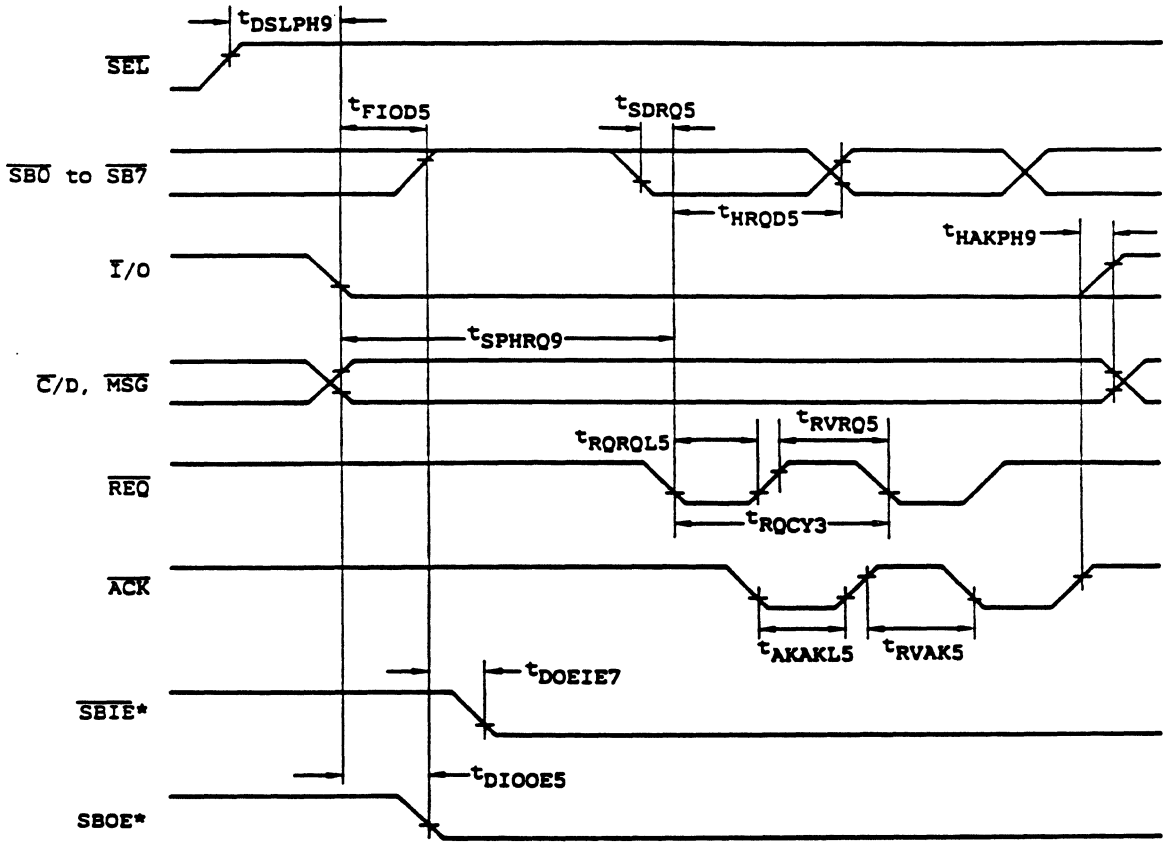
*: Differential driver control signal

Synchronous mode target reception (data-out phase)



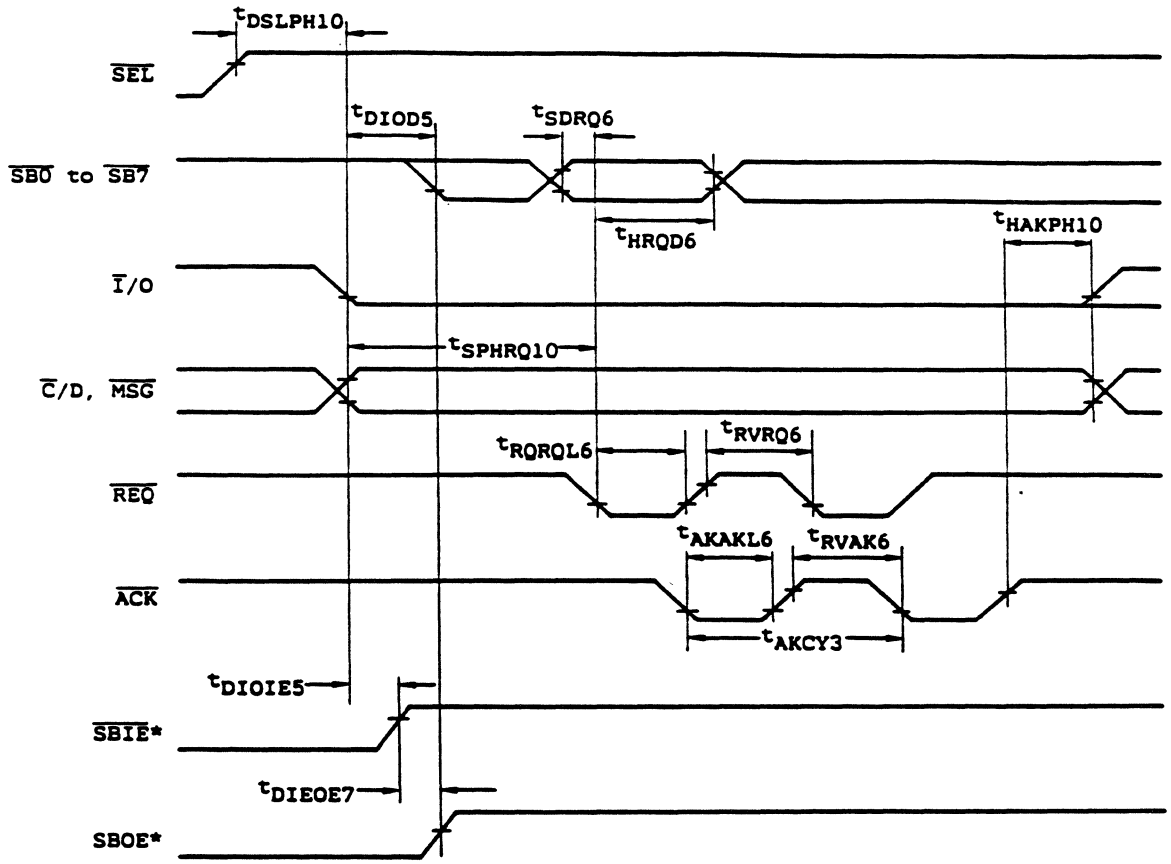
*: Differential driver control signal

High-speed synchronous mode initiator reception (data-in phase)



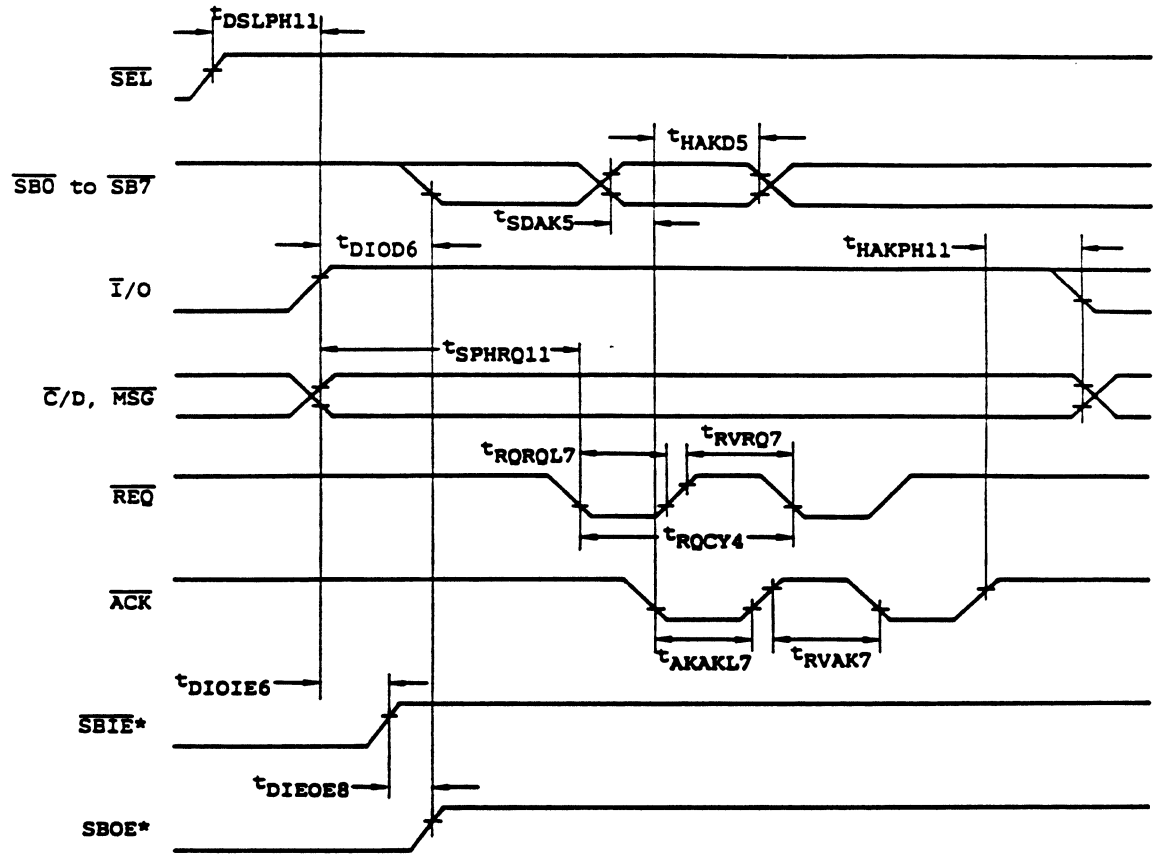
*: Differential driver control signal

High-speed synchronous mode target transmission (data-in phase)



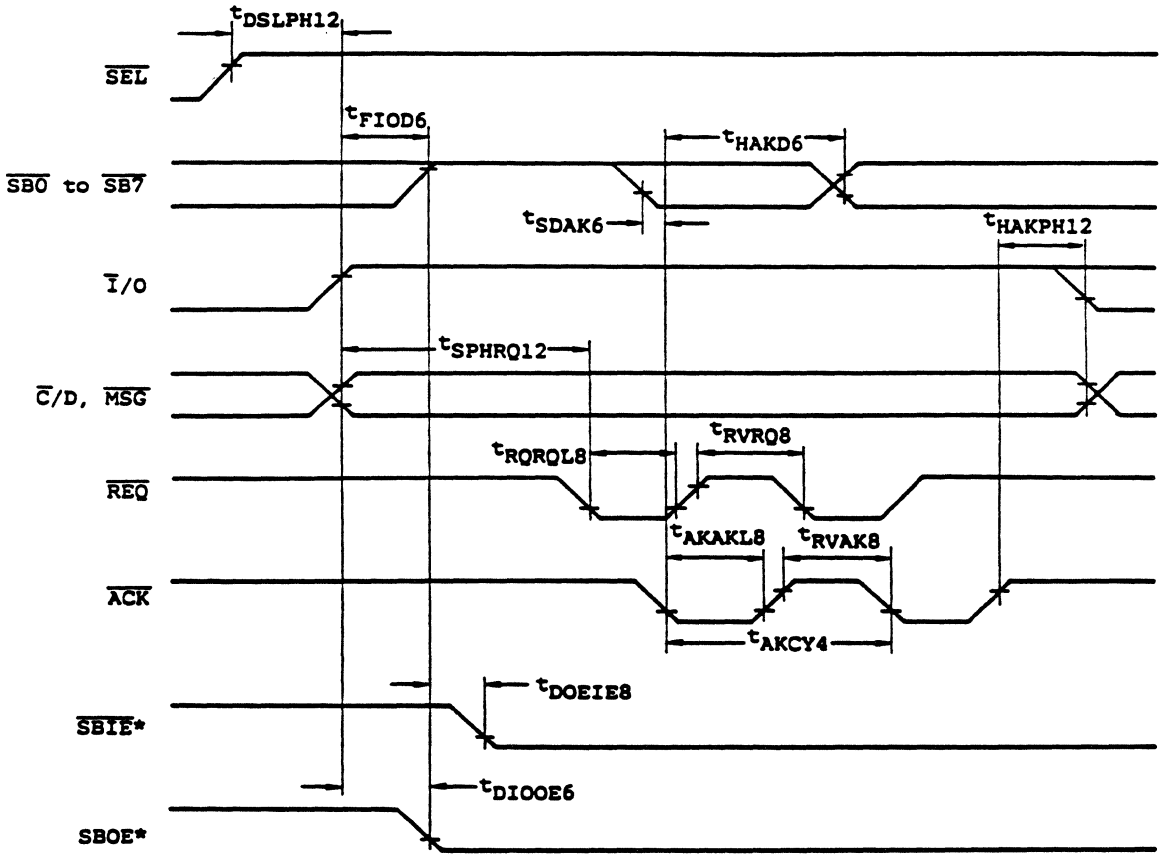
*: Differential driver control signal

High-speed synchronous mode initiator transmission (data-out phase)



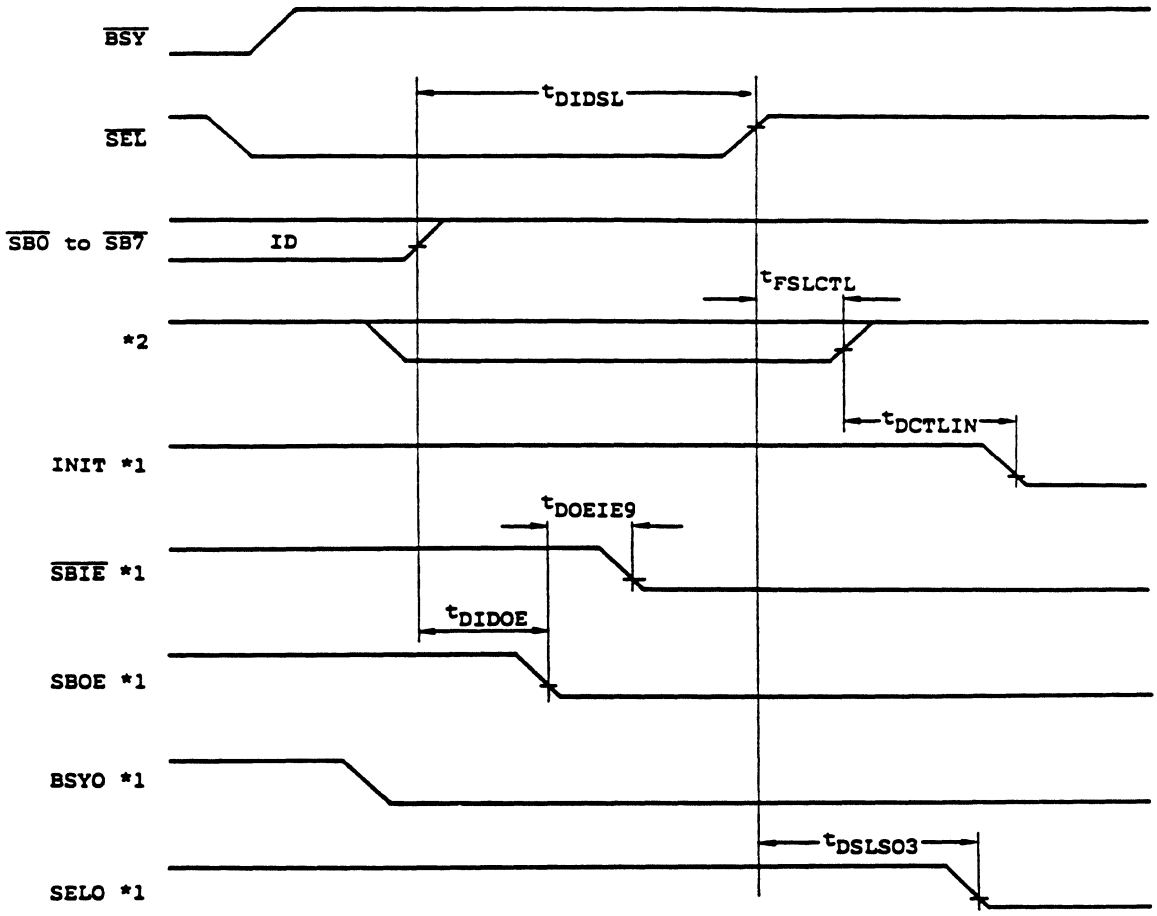
*: Differential driver control signal

High-speed synchronous mode target reception (data-out phase)



*: Differential driver control signal

Selection/reselection → bus free

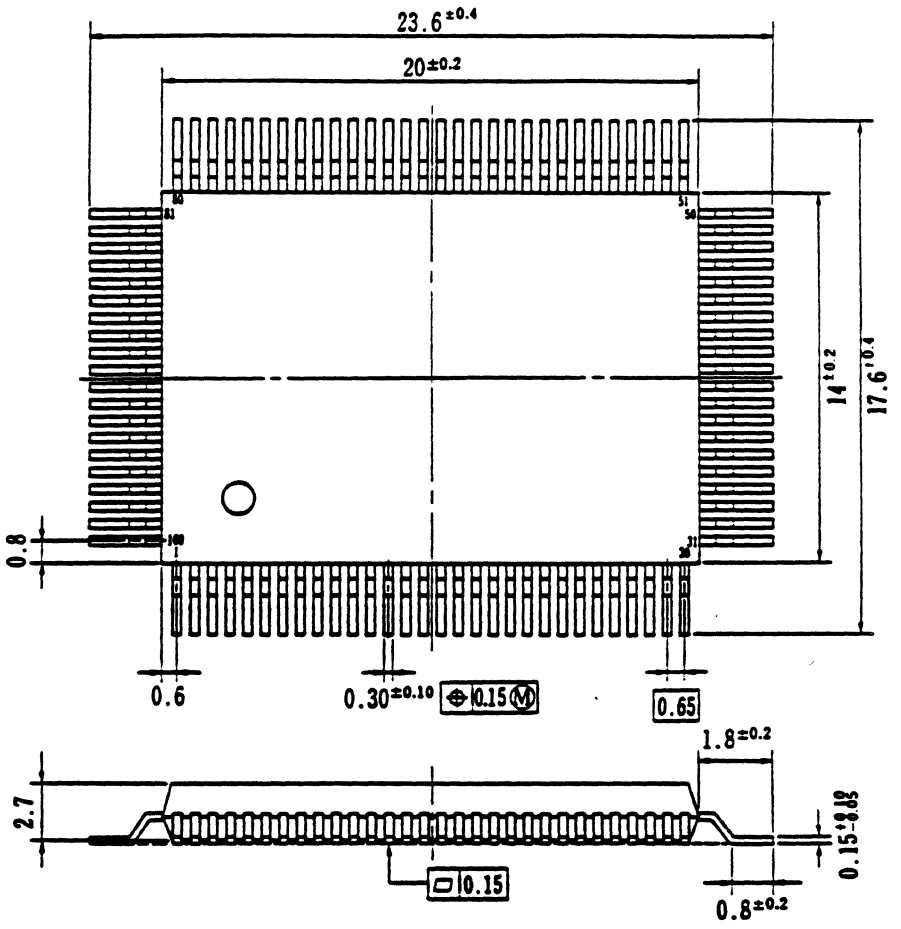


*1: Differential driver control signal

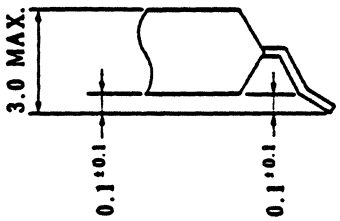
2: ATN and ACK to be output by the initiator or I/O, C/D, MSG and REQ to be output by the target

CHAPTER 8. PACKAGE INFORMATION

100-Pin Plastic QFP (Unit: mm)



Detail Drawing of Pin Tip Shape



P100GF-65-3BA

CHAPTER 9. RECOMMENDED SOLDERING CONDITIONS

Soldering and mounting for this product have not yet been defined. Contact our sales man.

NEC
NEC Electronics Inc.
CORPORATE HEADQUARTERS
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P.O. Box 7241
Mountain View, CA 94039
TEL 415-960-6000
TLX 3715792

For literature, call toll-free 8 a.m. to 4 p.m. Pacific time:
1-800-632-3531

ID-8343