NEC ELECTRONICS (EUROPE) GMBH

SYSTEM SPECIFICATION

μPD 7762

μPD 7761

MC 4760

1/83 V1.0

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1. System Configuration

NEC's voice recognition LSI has been developed with the goal of simplifying the normally highly complicated voice recognition process.

Voice recognition consists of an analysis process, which analyzes input voice data, and a recognition process, which performs matching calculation of registered voice data against input voice data that has been analyzed by the first process. These processes are performed by two voice recognition LSIs and an HIC. The HIC (MC-4760) integrates amplifier, equalizer and A/D converter functions and serves as an analog interface.

As for the two voice recognition LSIs, one is the control LSI (μPD7762) which controls operation of the system and the other is the calculation LSI (μPD7761) which performs analysis and matching calculations using an 8-channel band-pass filter.

By employing the compression DP matching algorithm, the voice recognition system consisting of the abovementioned three chips recognizes a maximum of 128 words of single-word input by a specific speaker with an average recognition response time of 0.7 sec. and a minimum recognition rate of 98% when using a 16K-byte memory.

A system configuration using a 64K-byte memory accordingly allows a maximum of 512 words to be registered in the system.

Fig. 1.1 shows a system configuration.

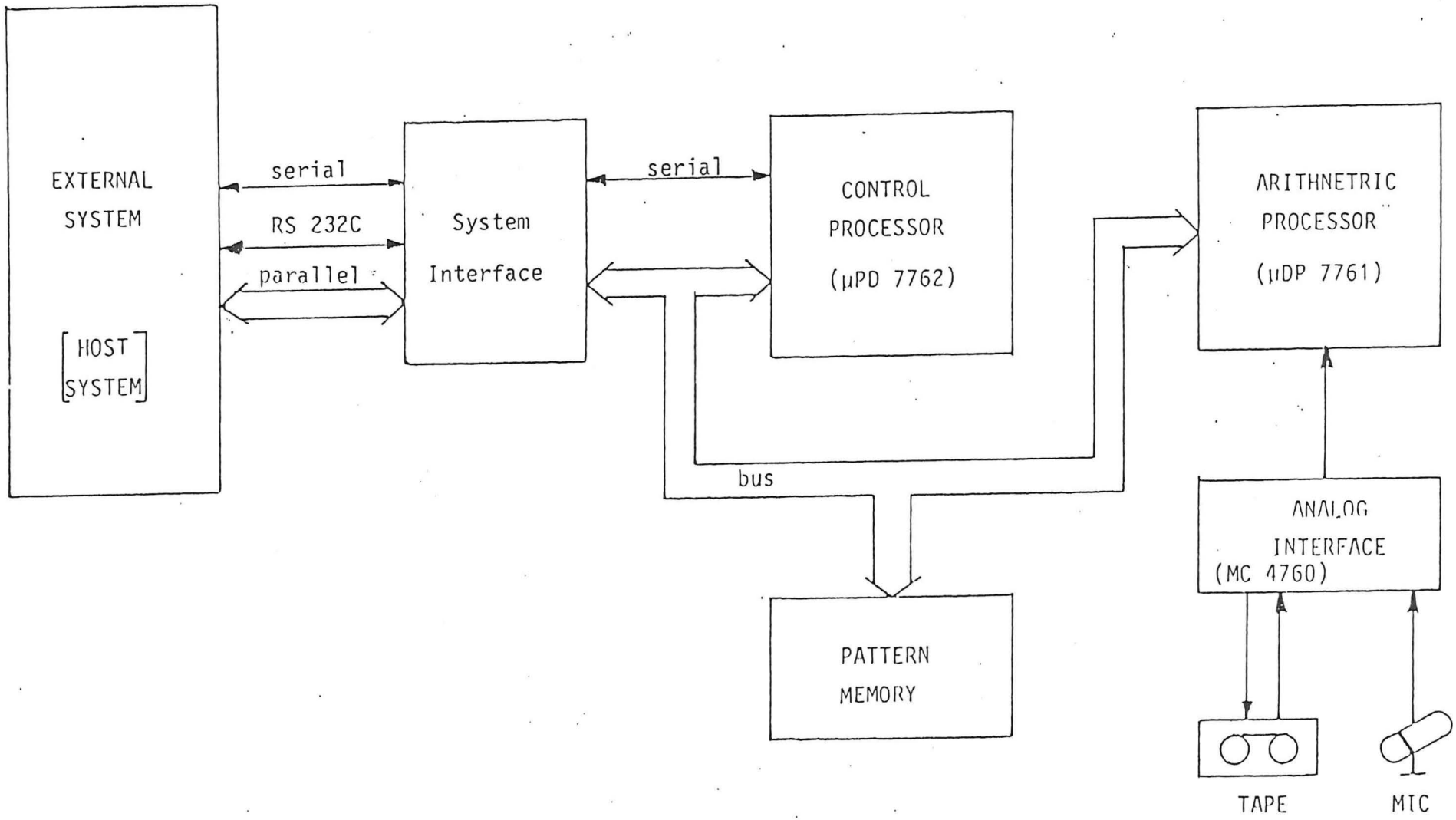


Fig. 1.1 System Block

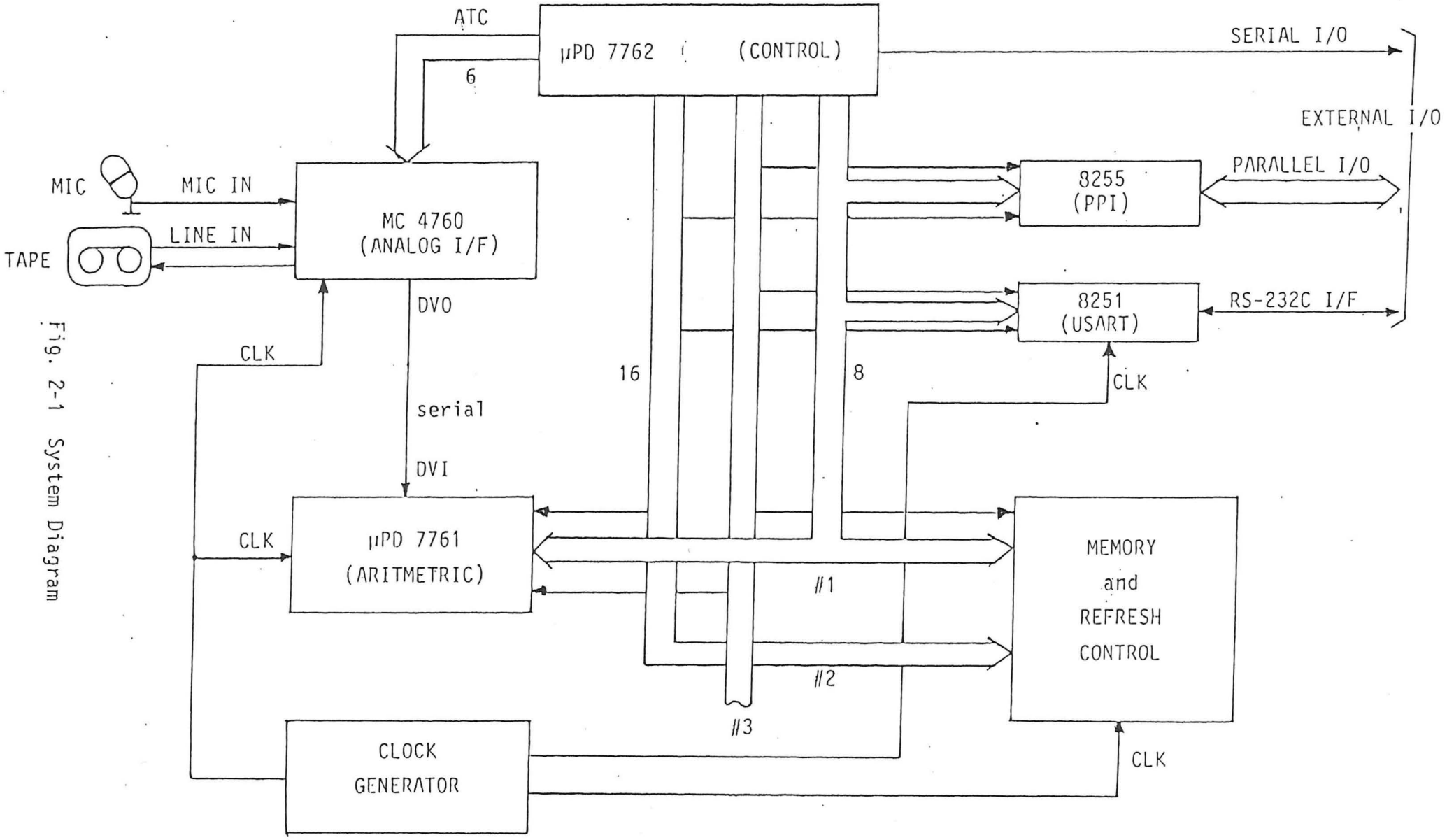


Fig. 2-1 System Diagram

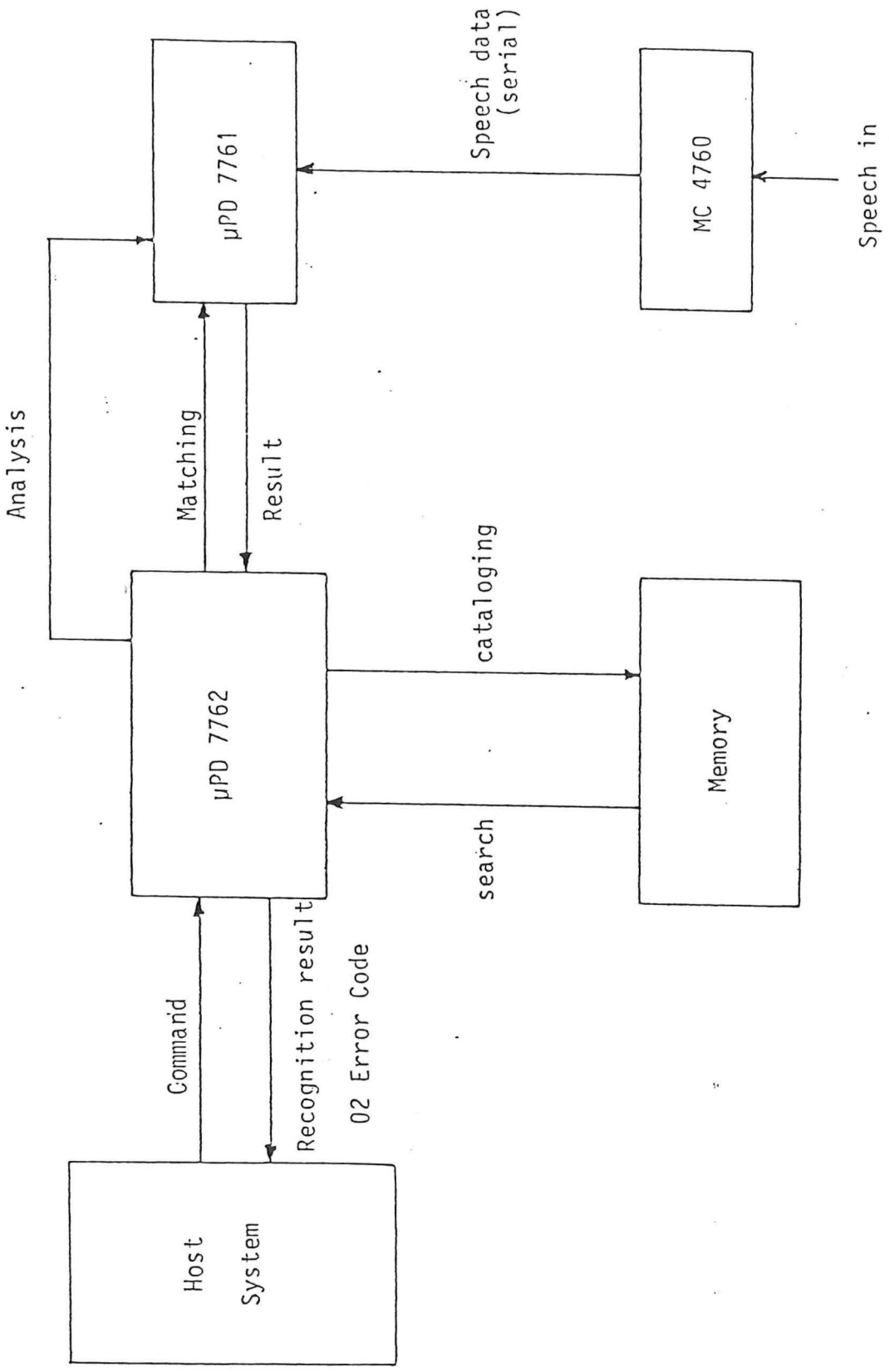


Fig. 2.2 Functional Relation of Voice Recognition Chips

° Baud rate : 64 rates (max. 9,600 bps)
° Character length : 8 bits
° Parity : Disabled
° Parity check : ODD
° Stop bits : 2 bits
° Asynchronous mode :

2.1.3 Serial interface (7762)

Since the 7762 is provided with a built-in serial port, it can be controlled directly when connected to a host system equipped with a compatible serial port.
The serial clock for this kind of I/O operation must be provided externally.
A configuration example and basic timing are shown in Figs. 2.9 and 2.10, respectively.
I/O of control commands through the serial port of the 7762 have the following points that require special attention. (Refer to Fig. 2.4.)
Input operation (Host to 7762)
After the host system has sent the control commands and terminator to the 7762, it must also send dummy data (00H). If this dummy data is not sent, the wrong data may be output. (For descriptions of the commands and the terminator, refer to 2.2.)
Output operation
The 7762 outputs a response (recognition result or error code) to the host system. Unlike the input operation, dummy data will not be sent. (For details of the response of 7762, refer to 2.2.)

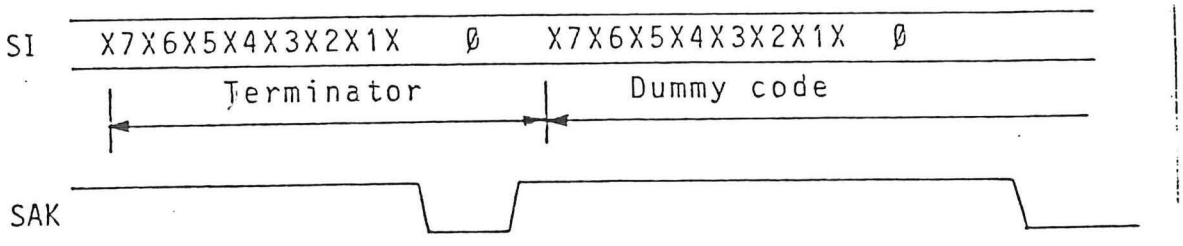
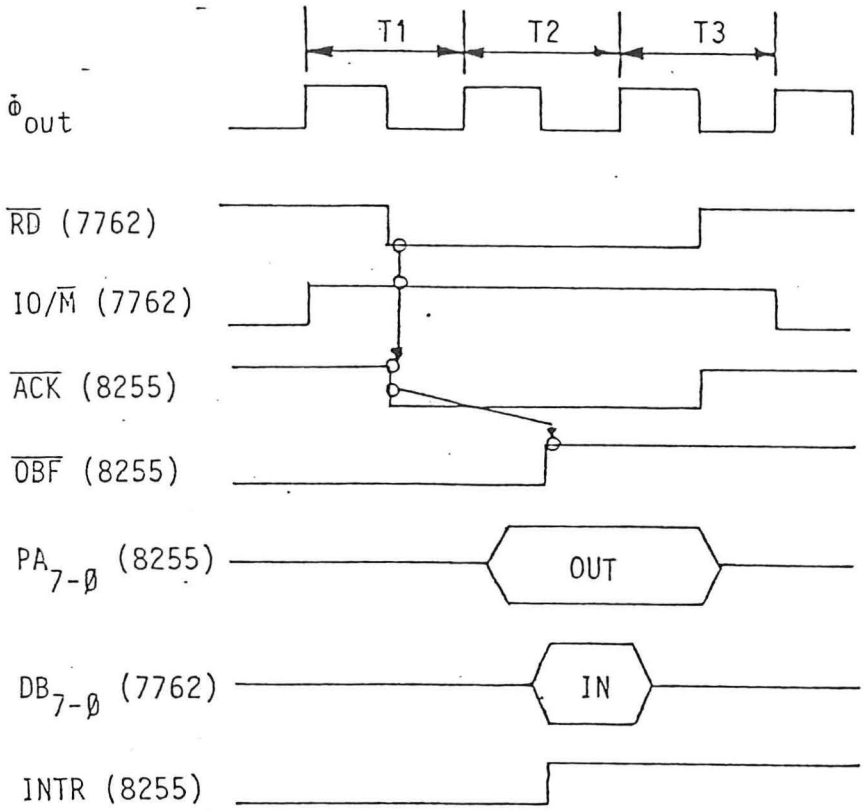


Fig. 2.4 Dummy Data of 7762 Serial Interface and SAK

NOTE: Input of the dummy data causes the SAK to be low level.

(1) Read cycle



NOTE: T1 means 1 machine cycle

(2) Write cycle

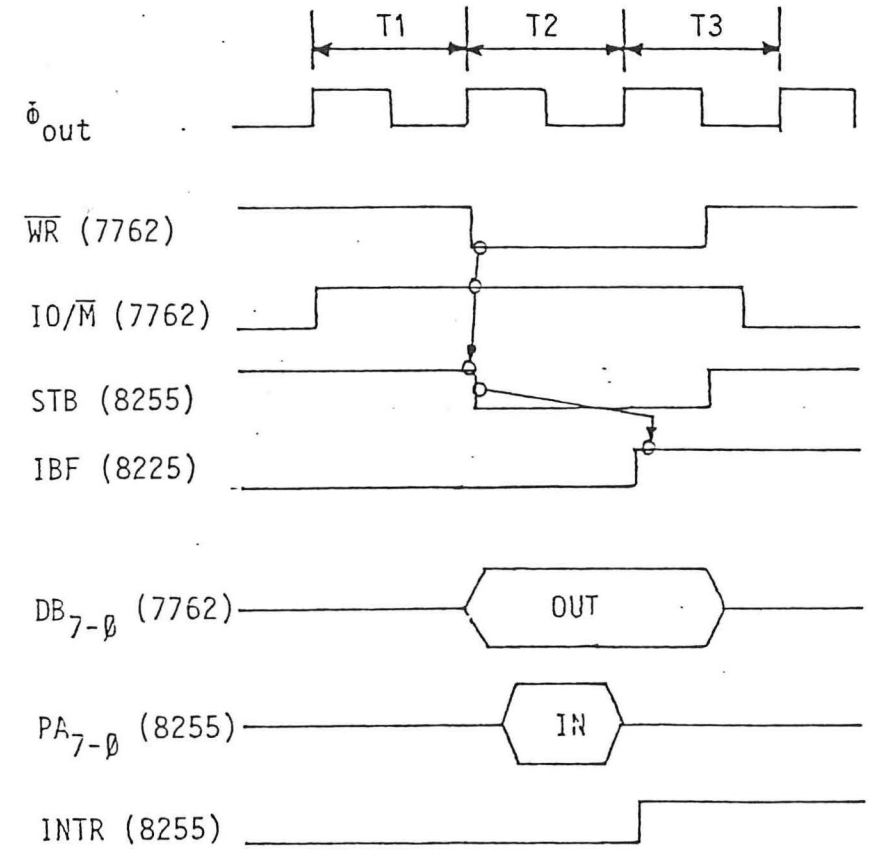
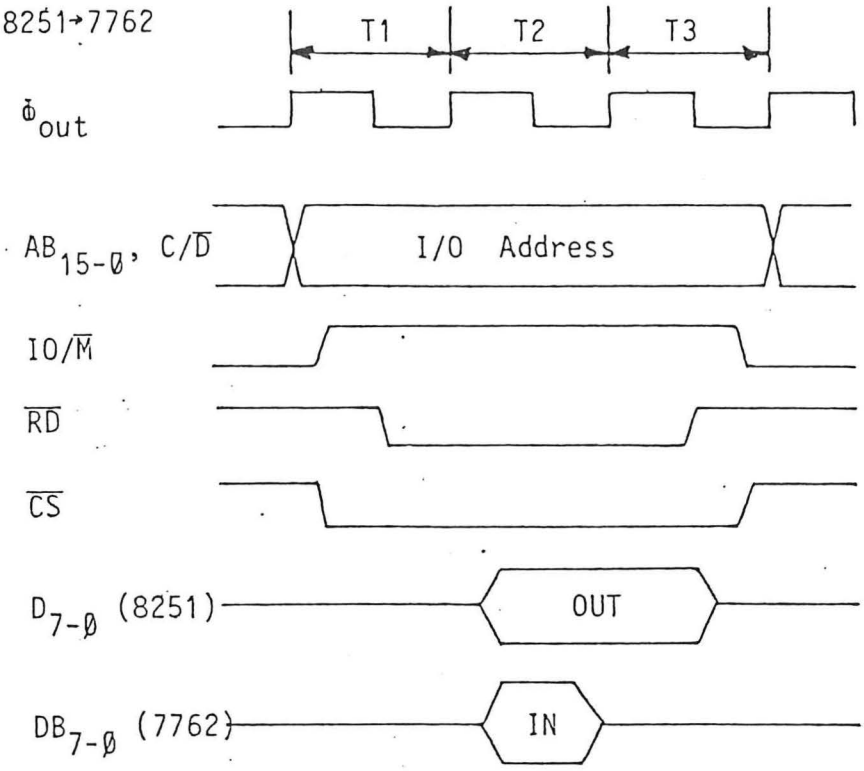


Fig. 2.6 Basic Timing of Parrallel Interface (8255)

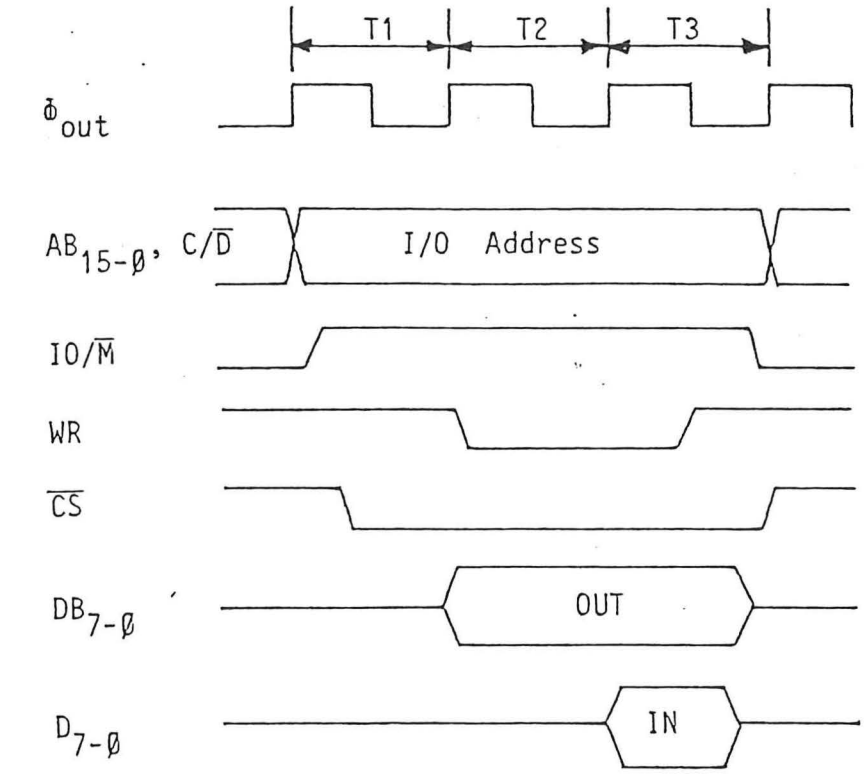
(1) Read cycle

8251→7762

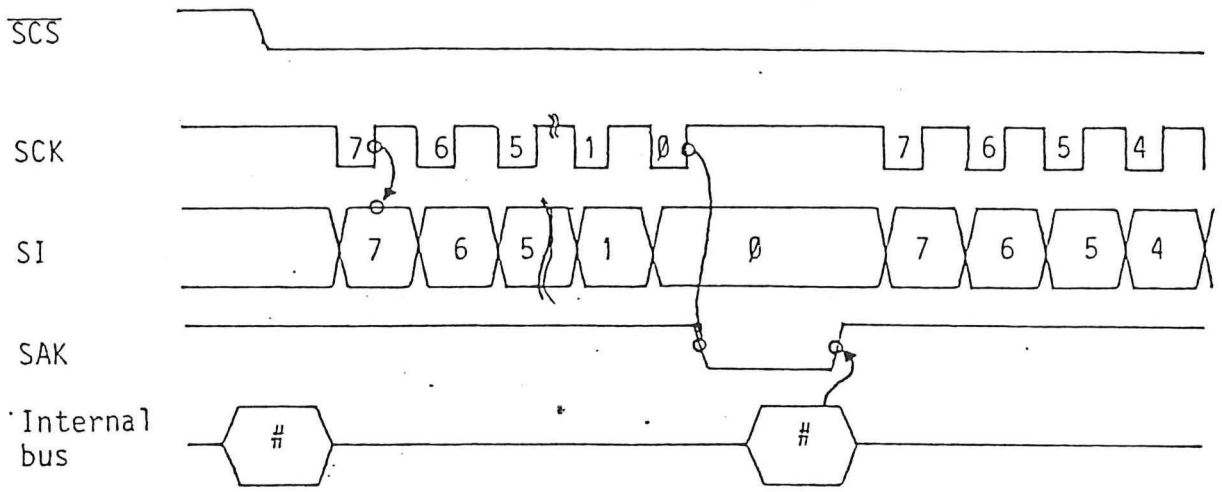


(2) Write cycle

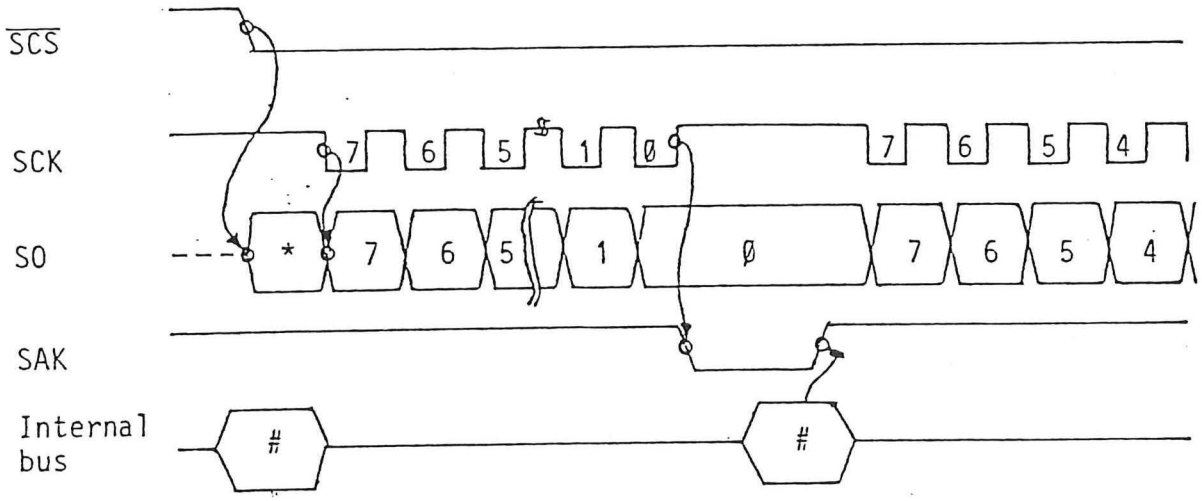
8251←7762



(1) Serial Input Host system to 7762



(2) Serial output 7762 to Host system



NOTES: # indicates the data transfer inside of the 7762.
will be the status of the last output. This
* becomes 0 immediately after the reset operation.

Fig. 2.10 Basic Timing of 7762 Serial Interface.

Table 2.1 μPD7762 Command Summary

Command Name	Command Format	Byte
INITIALIZE	00H, 0FFH	2
LEVEL ADJUST	01H [Bank No.] [Bank No.] [Bank No.] [Bank No.] 0FFH	6 max.
TRAINING	02H, Record No. [Syntax No. Word reject value] 0FFH	5 max.
RECOGNITION	03H, (Syntax No.][ ] [Syntax No.] 0FFH	33 max.
SECOND DECISION	04H, 0FFH	2
HOT START	05H, 0FFH	2
DOWN LOAD	06H, Registration No., &FFH, Parameter	No. of parameter + 3
UP LOAD	07H, 0FFH (Used with DOWN LOAD in a pair.)	2
CHANGE REJECT LEVEL	08H, Word reject value, 0FFH	3
MEMORY TEST	09H, 0FFH	2
BANK SELECT	0AH, Bank No., 0FFH	3
TIMER SET	0BH, Timer value, 0FFH	4
WORD REJECT	0CH, Record No., Word reject value, 0FFH	4
ARO SET	0DH, 0FFH	2
LOAD DATA	0EH, Address, No. of data, 0FFH, data, , data	10 + No. of data
EXECUTE	0FH, Address, 0FFH	6

NOTES: 1. 0FFH: Terminator

2. The items enclosed in brackets ([ ]) can be omitted.

Function: Registering the voice pattern

° Voice data is input through the MC-4760 and analyzed by the μPD7761.

° In accordance with the record No., the registered voice pattern and the representative data are set in the table and the syntax No. and word reject value are entered in the dictionary.

* Syntax No. and word reject value are used during voice recognition.

Output code: 00H (acknowledge): Normal completion
All other outputs are error codes.

NOTE: See System Configuration Drawing Fig. 2.12.

(4) RECOGNITION

Command format: 03H [syntax No.] [syntax No.] [---] 0FFH

0 ≤ syntax No. ≤ 128

However, the maximum number of syntax Nos. that can be set is 31.

If syntax No. is omitted, 0 is assumed.

Function: To input voice data, perform DP matching calculations against the registered voice patterns and output the result to the host system.

° Voice data is input through the MC-4760 and analysis is performed by the μPD7761.

° DP matching calculations are performed to compare the input voice pattern against each of the registered voice patterns with the specified syntax No(s).

(5) SECOND DECISION

Command format: 04H, 0FFH

Function: To output the registered voice pattern found to have the second smallest distance from the input voice pattern. Valid only after execution of RECOGNITION command.

Output code: 00H (Acknowledge): Normal completion
After output of the acknowledge code, the record No. and the distance will be output.
Any output other than the acknowledge code will be an error code. However, in the case of error code 0AH, record No. and distance will also be output.
In all other cases, only the error code will be output.

(6) HOT START

Command format: 05H, 0FFH

Function: To initialize all elements of the chip set system except the memory.

- Initializes serial ports 8251 and 8255.
- Resets the 7761.
- Initializes the gain of the MC-4760.

Output code: 00H (Acknowledge): Normal completion
Any other output will be an error code.

(7) DOWN LOAD

Command format: 06H No. of registered patterns, 0FFH, parameters
$1 \leq$ No. of registered patterns ≤ 128
Parameters are described below.

Function: To load the registered voice pattern data from the host system to the current memory bank.

- Erases the registered voice pattern data in the current bank memory.

Output code: 00H (Acknowledge): Normal completion
Any other output will be an error code.

(12) TIMER SET

Command format: 0BH, timer value, 0FFH
Timer value in 2 bytes is transmitted in the order of low- to high- order bits. 12 bits are effective.

Function: To set a value in the timer of the 7762 and to activate the timer.
° The timer is a 12-bit down counter and counts at speeds of 4μS to 16ms, with a resolution of 4μS. Causes the output of a time-out signal from the T0 terminal of the 7762.

Output code: 00H (Acknowledge): Normal completion
Any other output will be an error code.

(13) WORD REJECT

Command format: 0CH, record No., word reject value, 0FFH

Function: To set the word reject value for the specified record No.

Output code: 00H (Acknowledge): Normal completion
Any other output will be an error code.

(14) ARO SET

Command format: 0DH, 0FFH

Function: A data setting command to be used for the record/reproduction board (PC-8012-04).
° Outputs D, P, R and E.

Output code: 00H (Acknowledge): Normal completion
Any other output will be an error code.

(15) LOAD DATA

Command format: 0EH, address, No. of data, 0FFH, data address and No. of data are input in units of 4 bytes. The first 2 bytes input the low byte and the next 2 bytes, the high byte, respectively.

to set very strict conditions for recognition of a single word (a code word, for example,) so that it will only be recognized when it is carefully and accurately pronounced.

2.2.4 Parameters for UP LOAD and DOWN LOAD

Input of UP LOAD or DOWN LOAD command enables I/O of registered voice pattern data with the host system.

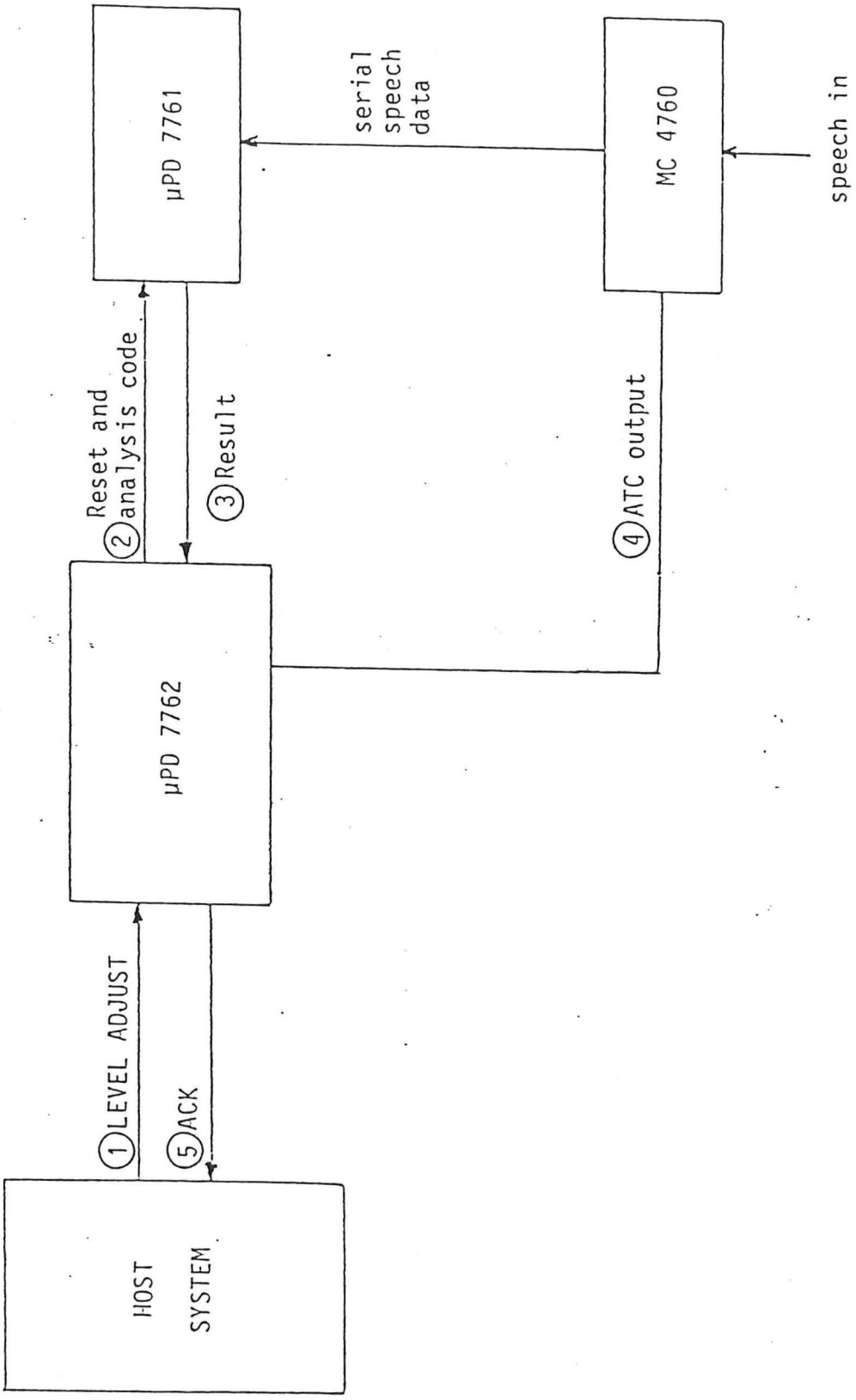
The UP LOAD command, outputs the acknowledge code, and then causes output of the No. of registered voice patterns, reject value table, record No., dictionary table, registered voice pattern table, extraction table, and next record No., in the above order. This operation may be repeated as many times as the number of the registered data.

Input of the DOWN LOAD command, on the other hand, after outputting the acknowledge code, causes the reject value table, record No., dictionary table, registered voice table, representative data table, and the next record No. to be output in that order and this output may be repeated for each registered voice pattern.

* Reject value table	2 bytes	**
Record No.	1 byte	
Dictionary table	6 bytes	
Registered voice pattern table ..	64 bytes (16 frames)	
Representative data table	16 bytes (16 frames)	

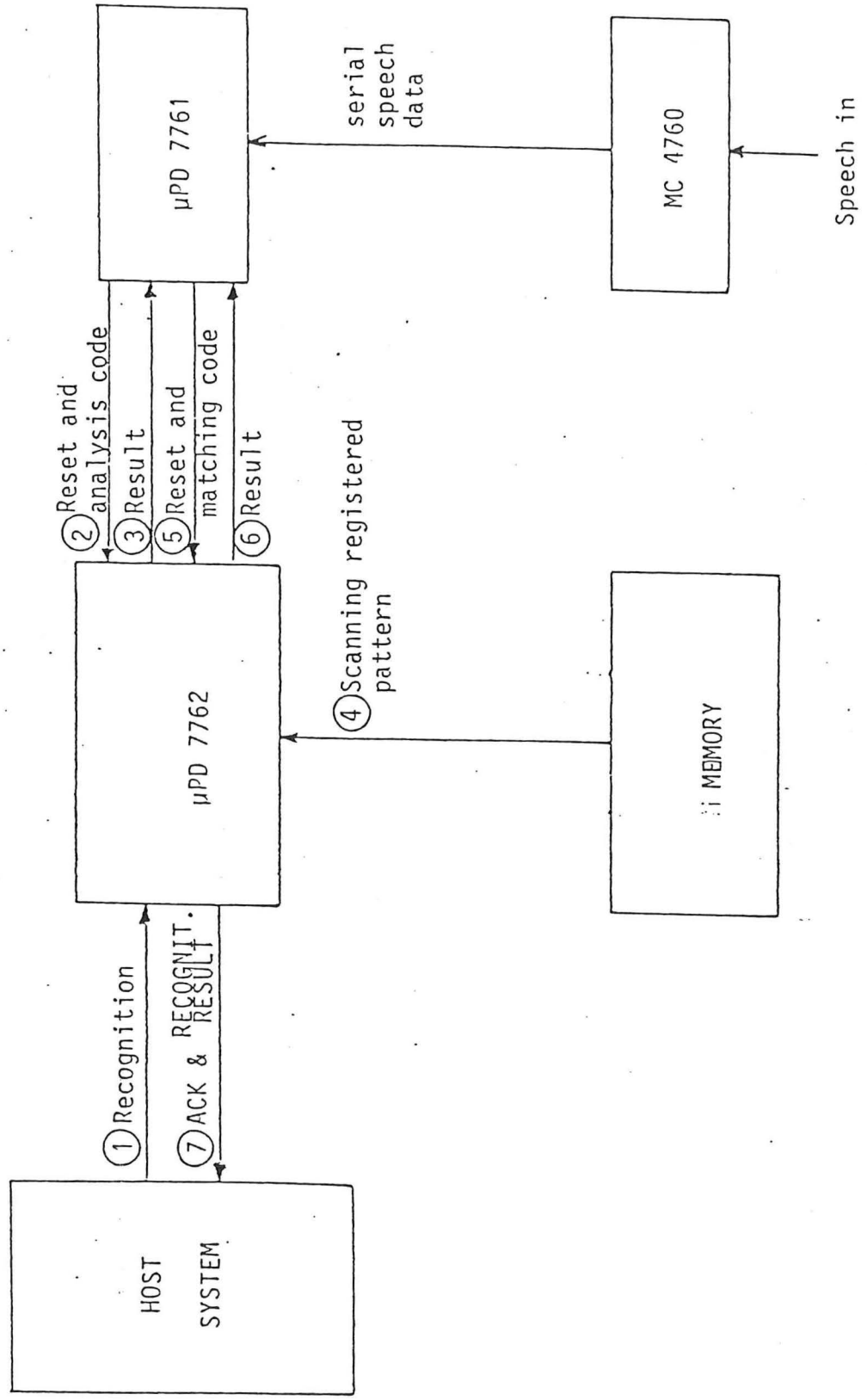
Output of items marked ** may be repeated for the number of registered voice patterns.

* Reject value table referred to here is for the bank reject value.



NOTE: The numbers indicate the phase

Fig. 2.11 Block Diagram of LEVEL ADJUST Command



NOTE: The status of each phase is shown in Figs. 2.14 to 2.16

Fig. 2.13 Block Diagram of RECOGNITION Command

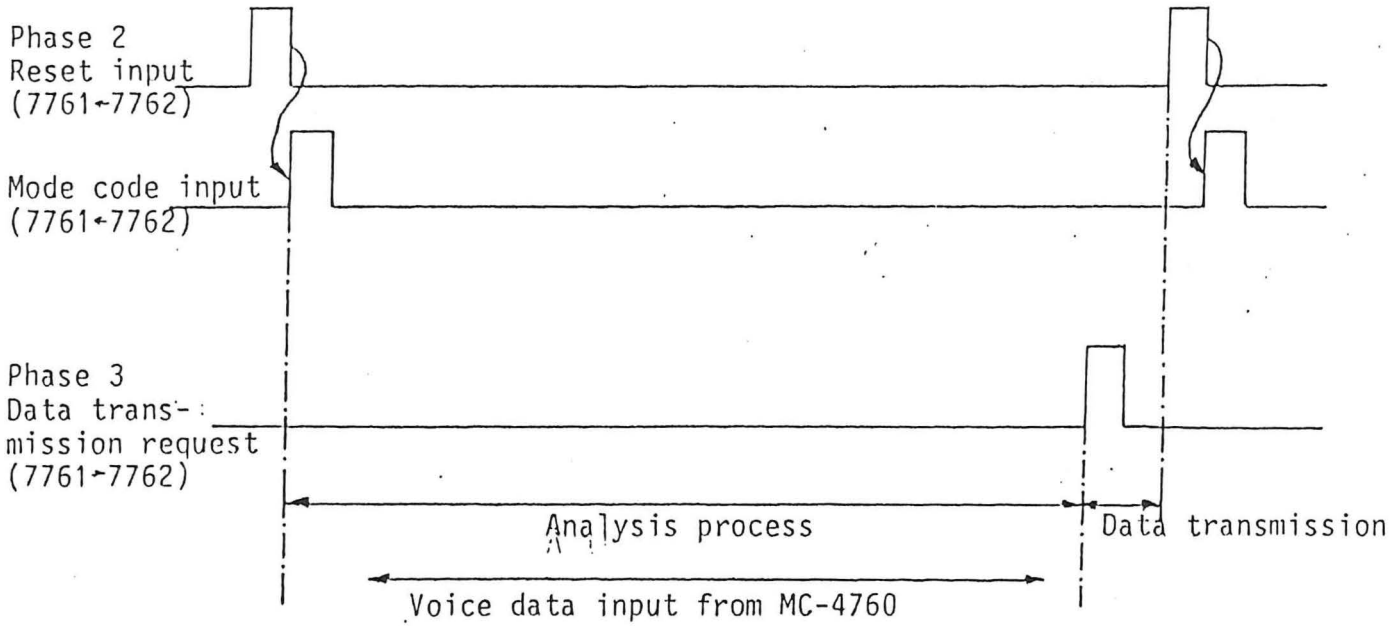


Fig. 2.15 Analysis Process of 7761

NOTE: Data transmitted, power and channel data: Total 10 bytes.
Phase No.s correspond to those in Fig.2.13

3. System Configuration

This chapter describes the features, terminal connections and functions of the μPD7762, μPD7761 and MC-4760 chips which make up the voice recognition chip set system. Brief explanations of the memories and clock are also presented.

3.1 μPD7762

3.1.1 Introduction

The μPD7762 is the control LSI of the voice recognition chip set and performs interfacing with the host system, receives commands from the host system, performs memory management and controls the μPD7762 and MC-4760.

3.1.2 Features

- Control LSI for the voice recognition LSI set.
- Connectable to an external memory of 64K bytes max. (addresses 1000H to FF7FH)
- μPD8255 interface port (fixed I/O addresses)
- μPD8251 interface port (fixed I/O addresses)
- Built-in serial interface
- Built-in clock oscillator (external drive (1 to 4MHz) also possible.)
- N-channel MOS
- 5V single power supply
- 64-pin QUIP plastic package

3.1.4 Terminal functions

(1) DB_0 to DB_7 (Data bus) 3-state input/output

8-bit bidirectional data bus.

Output becomes high during input mode and reset operation.

(2) AB_0 to AB_{15} (Address bus) output

16-bit address bus for setting memory and specifying I/O addresses. Memory addresses are from 1000H to FF7FH.

(3) SAK (Serial acknowledged) output

Outputs data transfer status when the serial port is used.

(4) $\overline{SCS}$ (Serial chip select) input

This pin should be connected to the GND terminal when the serial port is used.

(5) IO/M (I/O or memory) output

This pin outputs low level during memory access; at all other times, high level is output.

(6) ATC_0 - ATC_5 (Attenuator control) output

Output signal for control of the MC-4760 attenuator.

(7) SEL0, SEL1 (I/F Select) input

Input terminal for selection of the external interface.

SEL0	SEL1	I/F
0	0	μPD8255 parallel
0	1	μPD7762G serial
1	1	μPD8251 RS-232C

(8) MM0, MM1 (Memory mode) input

Input terminal for specification of the memory area

MM0	MM1	Memory area
0	0	64K bytes
0	1	16K bytes
1	0	32K bytes
1	1	48K bytes

(9) $\overline{OBF}$, IBF input

When the μPD8255 is used, these terminals are used for input of control signals $\overline{OBF}$ and IBF from the μPD8255, and are left open when μPD8255 is not used.

(20) RE (Refresh enable) output

Output terminal for refresh enable when using the DRAM in the μPD7762G memory. While this signal is high level, the memory of μPD7762G will not be accessed.

(21) $\overline{\text{WAIT}}$ input

Input terminal for wait signal when using the slow RAM in the memory. The wait signal is checked at the end of the T2 cycle and if it is low, the wait cycle (Tw) will be repeated until it becomes high.

(22) C.G. (Contact ground) input

This pin is connected to the GND terminal.

(23) DORQ (Data output request) input

Input terminal for data transfer request signal from the μPD7761. When this signal is high, the 7762 receives data from the 7761 via the data bus.

(24) HST (Hot start) input

Input terminal for hot start request signal from the hardware. After detection of the rising edge, if high level on this signal is maintained for 4 μS (4MHz clock), a request signal will be assumed.

(25) Vcc

+5V power supply.

(26) GND

0v

3.1.5 Reset operation of 7762

When a low level signal is applied to the RESET terminal for more than 4 μS (4MHz clock), internal reset of the 7762 will be performed. After reset, the 7762 will perform the following operations.

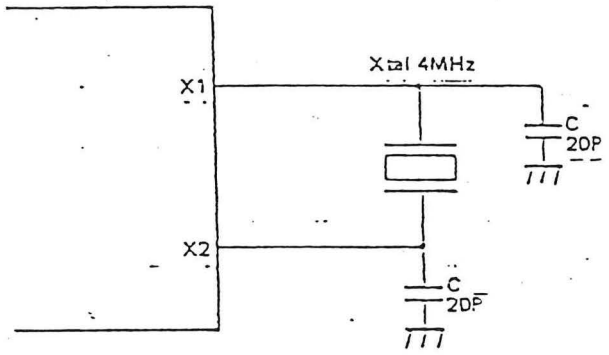
- Outputs a high level signal to the RST terminal for at least 3 clock pulses to reset the 7761.
- Performs mode setting of the 8251.
- Reads the dummy data in the PA port of the 8255 and initializes the timing with the 8255. (Mode setting of the 8255 must be complete before timing can be initialized.)
- Sets the serial port of the 7762 in the input mode.

3.1.10 7762 clock signal generator

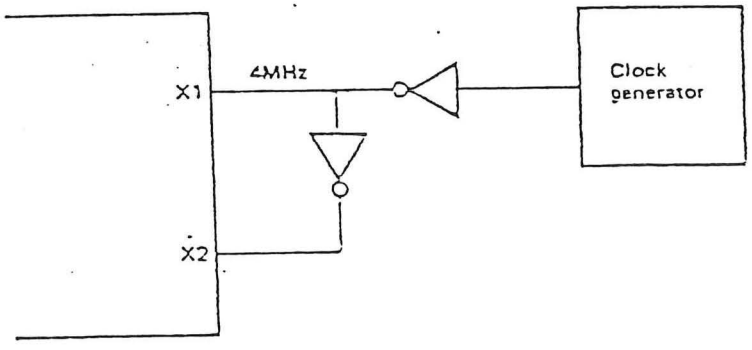
The clock signal for the μPD7762G is provided either by the internal crystal oscillator circuit or by an external clock signal generator.

The circuit examples for internal and external clocks are shown below.

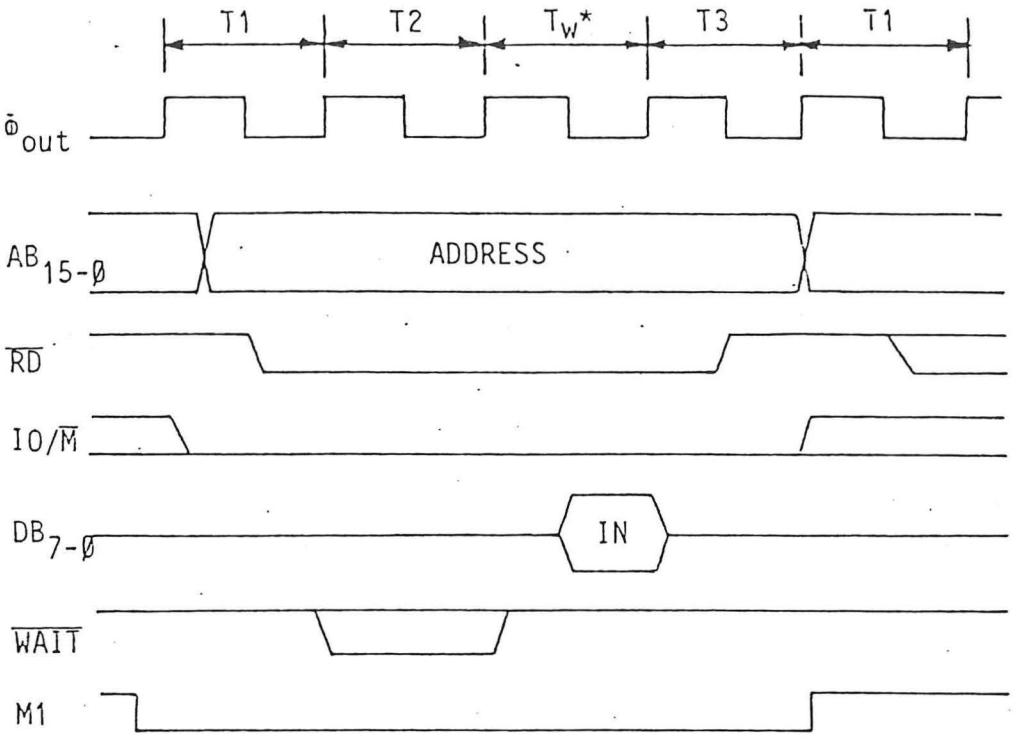
(1) Internal clock circuit (reference)



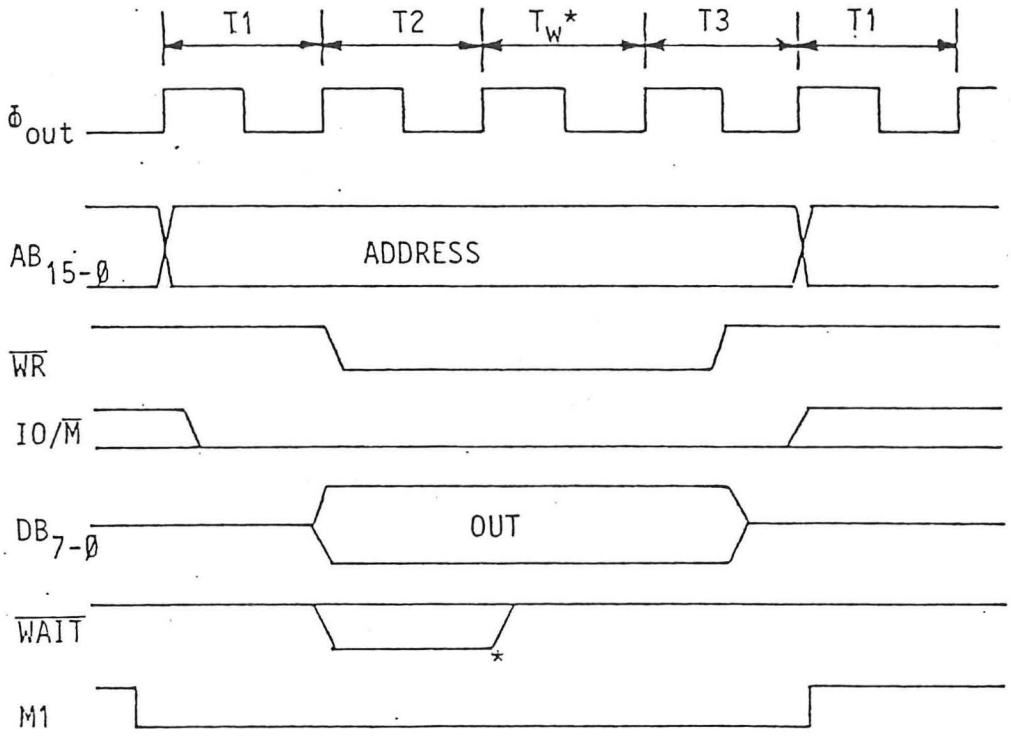
(2) External clock circuit (reference)



(i) Memory read (From memory to 7762)



(ii) Memory write (From 7762 to memory)



NOTE: *Input the wait cycle when a slow memory is being used.

Fig. 3.2 Access Timing of Memory

3.2 μPD7761

3.2.1 Introduction

The μPD7761 performs calculation process such as analysis of voice data, matching calculation of input voice patterns against registered voice patterns, and so forth.

3.2.2 7761 features

- Analysis and matching calculation processor for the voice recognition LSI set.
- Data communications with the 7762 are performed through the data bus using a handshake signal.
- Voice analysis is performed by an 8-channel biquad digital filter.
- Control is by 16-bit mode code from the 7762.
- Built-in serial port for input of voice data from MC-4760
- Fixed I/O addresses (as viewed from the 7762)
- Clock signal frequency: 8MHz ~ 1MHz
- N-channel MOS
- +5V single power supply
- 28-pin DIP ceramic package

3.2.4 Terminal functions

(1) D_0 ~ D_7 (Data bus) 3-state I/O
8-bit bidirectional data bus for I/O of data and mode codes with the 7762.

(2) A_0 (Address select) input
Input terminal used to select between access of the data register (DR) and the status register (SR) of the 7761.
When A_0 is 0, DR is selected and when A_0 is 1, SR is selected.

(3) $\overline{CS}$ (Chip select) input
When this signal is high, D_0 ~ D_7 are enabled for I/O.

(4) $\overline{RD}$ (Read) input
Read control signal used when reading the contents of either DR or SR.

(5) $\overline{WR}$ (Write) input
Write control signal used when writing to DR.

(6) DORQ (Data output request) output
Output signal to request data transfer from the 7762.

(7) DVI (Digitized voice input) input
Input for voice data after it has been converted to 8-bit digital data by MC-4760.

(8) CG (Contact ground) input
Connects to GND.

(9) SMPL0, SMPL1 (Sampling clock) input
Inputs terminal for A/D strobe signal. Signal input is 10 KHz sampling clock; normally, this is the reverse phase of the signal input to the SMPL terminal of the MC-4760.

(10) SCLK (Serial clock) input
The reverse phase of the signal input to the CLK terminal of the MC-4760 is input. This signal is synchronized with that clock and provides timing for the input of voice data from DVI.

(11) RST (Reset) Input
Input terminal for reset signal to initialize the internal system of the μPD7761D. To initialize the

° The 7761 is first synchronized with the SCLK (serial clock) signal; 8-bit digitized voice data from the MC-4760 is then input to the 7761 through the DVI terminal.

° The frequency of the voice data input is analyzed by an 8-channel digital filter and the power is calculated.

° After all analysis processes have been completed, the 7761 sends a DORQ signal to the 7762, indicating the end of the process.

° Through the data bus, the 7761 then sends a 2-byte code (00H) to the 7762 which indicates that the result to be output is that of the analysis process. (The code is sent starting from the lower-order byte.)

° Then, power data and data for CH1 to CH8 is sent to the 7762 in units of 2 bytes in the order of the lower-order byte to the higher-order byte.

° When the data transmission is completed, the 7761 will re-enter the WAIT state, and wait for input of the next reset signal from the 7762.

(4) Matching calculation mode (mode code = 8xxxH)

When the 7761 is set in matching calculation mode by input of a mode code from the 7762, the following operations will be performed.

° The number of frames of input voice pattern data is sent from the 7762 to the 7761 as 1 byte of data.

° Input voice pattern data (4 bytes) and representative data (1 byte) are input from the 7762 for the number of frames of voice data.

° Number of frames of registered voice pattern data is input from the 7762 as 1 byte of data

° Registered voice pattern (4 bytes), cutoff parameters and representative data (1 byte) are input for the above number of frames.

° Matching calculation will be performed for the two sets of data (input and registered voice patterns).

The voice data sent from the 4760 to the 7761 through the DVI terminal of the 7761 is synchronized with SCLK. Although the data from the 4760 normally flows to the DVI terminal of the 7761, the selection of whether or not to accept data is made internally at the 7762.

For input timing for serial data, refer to the section on the MC-4760.

3.2.8 Serial clock and reset of 7761 and 4760

Serial voice data input to the 7761 from the 4760 is synchronized with the serial clock input to the SCLK terminal of the 7761 and the terminal CLK of the 4760. Therefore, when the 7761 is reset, it is also necessary to reset the serial clock at the same time. If this reset operation is not performed, normal data transmission may not be possible.

3.3 MC-4760

3.3.1 Introduction

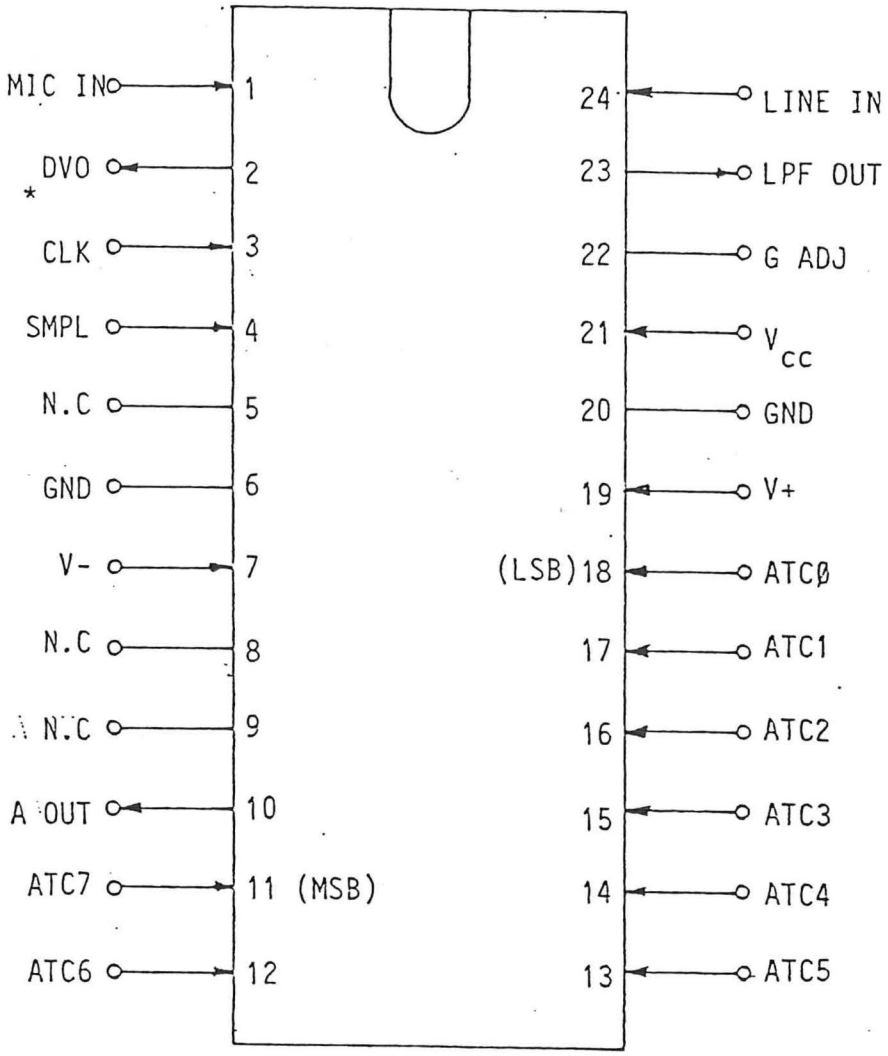
The MC-4760 is an integrated voice input circuit designed to perform optimum analysis of voice band signals. Voice signals are input from a microphone or a tape, amplified and equalized. They are then converted from analog to digital signals by the A/D converter and output as serial data. Furthermore, the built-in digital attenuator enables the 7762 to perform gain adjustment.

3.3.2 Features

- IC performs analog interfacing for the voice recognition LSI set.
- Built-in variable amplifier with external resistor
- Built-in equalizer
- 8-bit TTL control digital attenuator incorporated
- 8-bit A/D serial output (MSB first)
- Built-in lowpass filter for elimination of foldover noise

3.3.3 MC-4760 Terminal connections

MC-4760 pin connection



Top view

N.C: Non connection

* DVO: Digital Voice Out

(13) LPF OUT (Lowpass filter output) output

Observation terminal for the analog signal immediately before A/D conversion. Do not connect the load to this terminal.

(14) LINE IN (Line input) input

For voice input from a tape. Input impedance: 10KΩ.

Maximum input level: $\pm 0.6_{o-p}$

(when sin wave calculation: EQL AMP: 20dB, Attenuator valve: 7FH)

3.3.7 Others

(1) G ADJ

The G ADJ terminal is an external resistance terminal which determines the gain of the variable amplifier in the MC-4760. The relation of the external resistance to gain, and the mounting method of the resistor are shown in Table 3.1 and Fig. 3.4, respectively.

Table 3.1 Changes Effected in Gain by External Resistance

Resistance (Ω)	Gain (dB)
Open	0.6
1100	10
505	15
258	20
138	25
75 *	30

Gain is obtained by the following formula.

$$G = 20\left\{\log \frac{\frac{(4.3)^2}{R} + 8.6}{10}\right\} + 1.9$$

where:

G: gain (dB)

R: resistance (KΩ)

* Do not use a resistance of less than 75Ω.

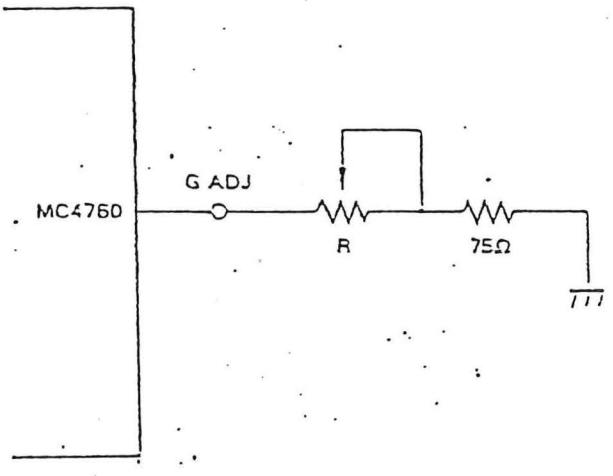


Fig. 3.4 Connecting External Resistor

Table 3.2 ATC Value and Output Voltage

ATC value (HEX)	Output voltage (V)
FF	$-V_{REF}\ (\frac{255}{256})$
81	$-V_{REF}\ (\frac{129}{256})$
80	$-V_{REF}\ (\frac{128}{256}) = -\frac{1}{2} V_{REF}$
7F	$-V_{REF}\ (\frac{127}{256})$
01	$-V_{REF}\ (\frac{1}{256})$
00	$-V_{REF}\ (\frac{0}{256}) = 0$

V_{REF} = Input voltage to internal attenuator
1LSB = $(2^{-8})\ V_{REF}$

(3) MIC input amplifier and A/D converter

The abbreviation 'AMP' in the block diagram in 3.3.5 denotes the MIC input amplifier, which is used to amplify voice signals as they are input from a microphone. The specifications of this amplifier are as follows:

Gain : 40dB
Input impedance: 1KΩ
Band : BPF of 100Hz to 10KHz

The A/D converter is used to convert voice signals input from a microphone or tape into digital signals. The ratings of the A/D converter conform to CODEC standards.

(6) Cautions in using memory

Although both SRAM and DRAM memories can be used, the memory capacity must be large enough to derive the bank configuration described on the preceding page. There are difficulties involved in the adoption of commercially available memories in that the read cycle of the 7762 is very fast and the minimum delay time until data read begins after the RD signal becomes high is only 350ns. Therefore, it is necessary to insert one "wait" in the read cycle (this will result in a delay time of 850ns.). In comparison, the write cycle does not require the insertion of any wait time. Timing calculations are based on CLK of 4MHz and ϕout of 2MHz.

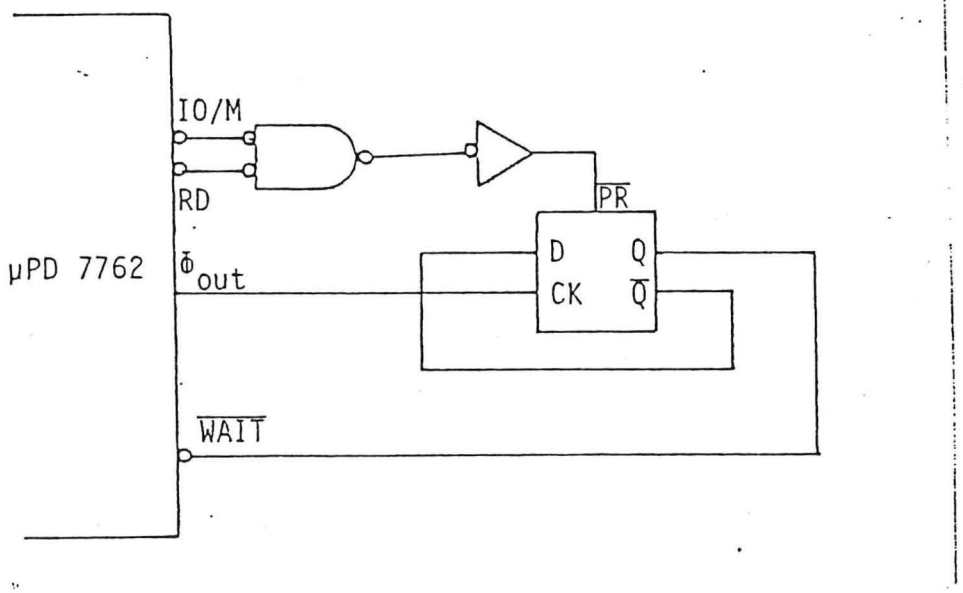


Fig. 3.5 Circuit Example to Generate One "Wait" in Read Cycle

4. Specifications

4.1 Introduction

This voice recognition system comprises three LSI chips: μPD7762, μPD7761 and MC-4760.

The detailed specifications for each chip are presented below.

AC Characteristics (T_a = −10 ~ +70°C, V_{CC} = +5.0V±10%)

Clock timing:

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
X1 — Input cycle time	t_{CYX}		227	1000	ns
X1 Input low pulse width	t_{XXL}		105		ns
X1 Input high pulse width	t_{XXH}		105		ns
φOUT Cycle time	$t_{CY\phi}$		454	2000	ns
φOUT Low pulse width	$t_{\phi\phi L}$		150		ns
φOUT High pulse width	$t_{\phi\phi H}$		150		ns
φOUT Raise/fall time	tr,tf			40	ns

Read/write operation:

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{RD}$ L.E. — φOUT L.E.	$t_{R\phi}$	$t_{CY\phi}$ = 500ns	100		ns
Address (AB0—15) — Data input	t_{ADI}			550+500xN	ns
$\overline{RD}$ T.E. — Address	t_{RA}		200		ns
$\overline{RD}$ L.E. — Data input	t_{RD}			350+500xN	ns
$\overline{RD}$ T.E. — Data hold time	t_{RDH}		0		ns
$\overline{RD}$ Low pulse width	t_{RR}		850+500xN		ns
$\overline{RD}$ L.E. — $\overline{WAIT}$ L.E.	t_{RWT}			450	ns
Address (AB0—15) — $\overline{WAIT}$ L.E.	t_{AWT1}			650	ns
$\overline{WAIT}$ Setup time (for φOUT L.E.)	t_{WTS}		290		ns
$\overline{WAIT}$ Hold time (for φOUT L.E.)	t_{WTH}		0	120	ns
RE — $\overline{RD}$ L.E.	t_{MR}		200		ns
$\overline{RD}$ T.E. — RE	t_{RM}		200		ns
IO/$\overline{M}$ — $\overline{RD}$ L.E.	t_{IR}		200		ns
$\overline{RD}$ T.E. — IO/$\overline{M}$	t_{RI}		200		ns
φOUT L.E. — $\overline{WR}$ L.E.	$t_{\phi W}$		40	125	ns
Address (AB0—15) — φOUT T.E.	$t_{A\phi}$		100		ns
Address (AB0—15) — Data output	t_{ADZ}		450		ns
Data output — $\overline{WR}$ T.E.	t_{DW}		600+500xN		ns
$\overline{WR}$ T.E. — Data stable time	t_{WD}		150		ns
Address (AB0—15) — $\overline{WR}$ L.E.	t_{AW}		400		ns
$\overline{WR}$ T.E. — Address stable time	t_{WA}		200		ns
$\overline{WR}$ Low pulse width	t_{WW}		600+500xN		ns
IO/$\overline{M}$ — $\overline{WR}$ L.E.	t_{IW}		500		ns
$\overline{WR}$ T.E. — IO/$\overline{M}$	t_{WI}		250		ns

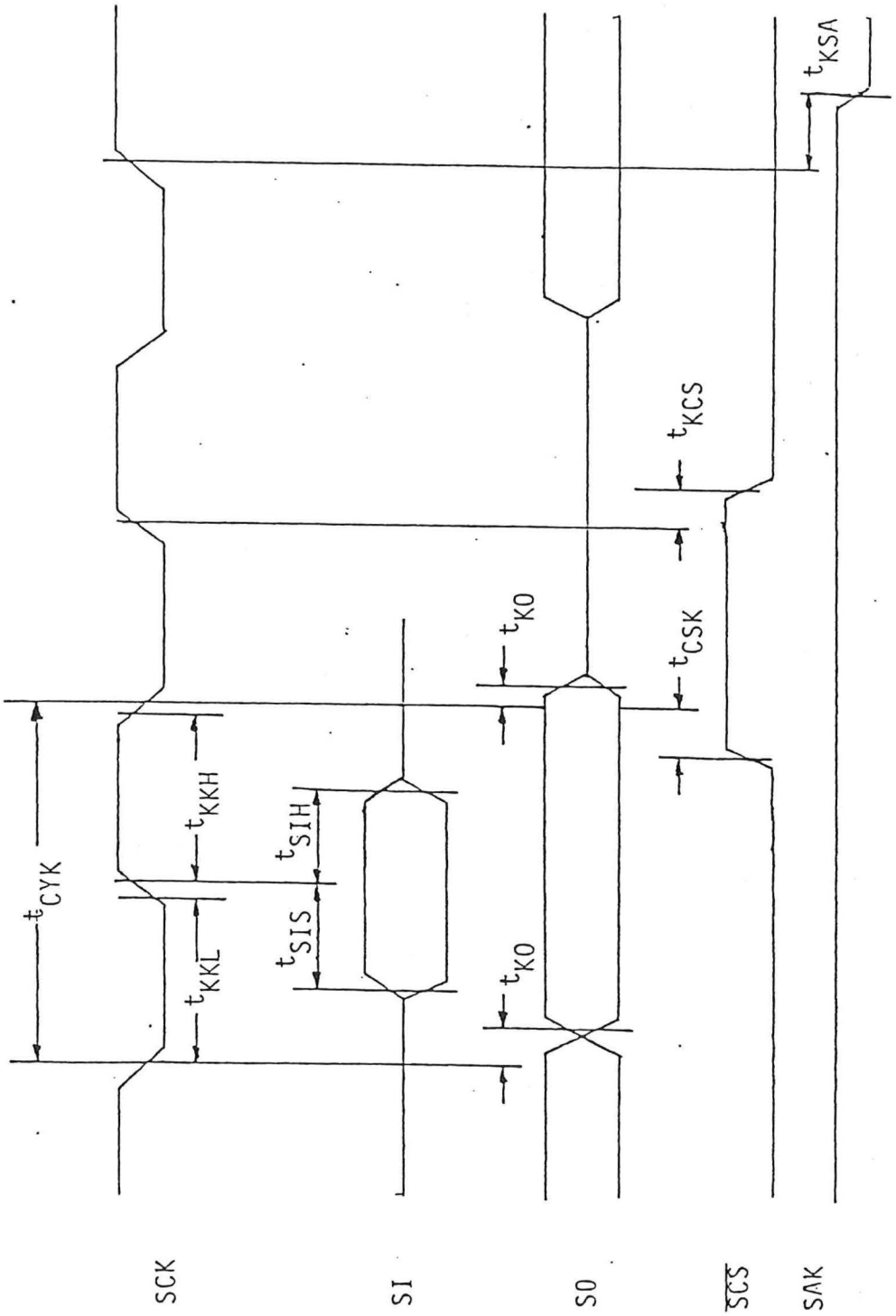
Timing of $t_{CY\phi}$-dependent bus parameters

Parameter	Formula	MIN./MAX.	Unit
t_{Ro}	(1/5) T	MIN.	ns
t_{ADI}	(3/2+N) T−200	MAX.	ns
t_{RA}	(1/2) T−50	MIN.	ns
t_{RD}	(1+N) T−150	MAX.	ns
t_{RR}	(2+N) T−150	MIN.	ns
t_{RWT}	(3/2) T−300	MAX.	ns
t_{AWTI}	(2) T−350	MAX.	ns
t_{ER}	(1/2) T−50	MIN.	ns
t_{RE}	(1/2) T−50	MIN.	ns
t_{IR}	(1/2) T−50	MIN.	ns
t_{RI}	(1/2) T−50	MIN.	ns
$t_{\phi W}$	(1/4) T	MAX.	ns
$t_{A\phi}$	(1/5) T	MIN.	ns
t_{ADZ}	T−50	MIN.	ns
t_{DW}	(3/2+N) T−150	MIN.	ns
t_{WD}	(1/2) T−100	MIN.	ns
t_{AW}	T−100	MIN.	ns
t_{WA}	(1/2) T−50	MIN.	ns
t_{WW}	(3/2+N) T−150	MIN.	ns
t_{IW}	T	MIN.	ns
t_{WI}	(1/2) T	MIN.	ns

NOTES: 1. No. of wait states

2. $T = t_{CY\phi}$

Serial operation

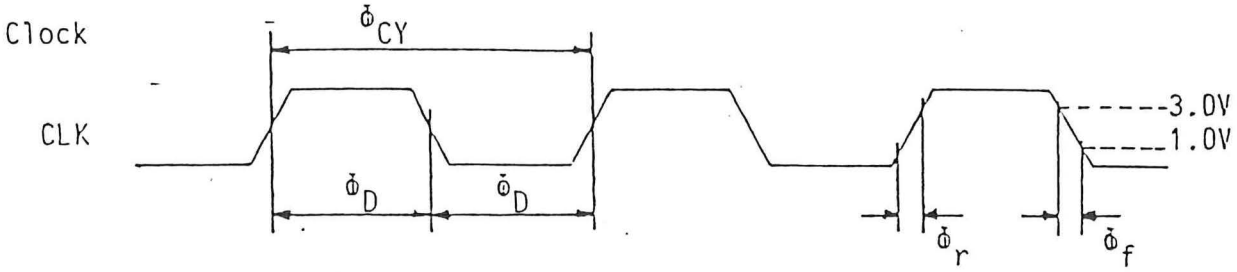


AC characteristics (T_a = -10 ~ +70 °C, V_{cc} = +5.0 V ±5 %)

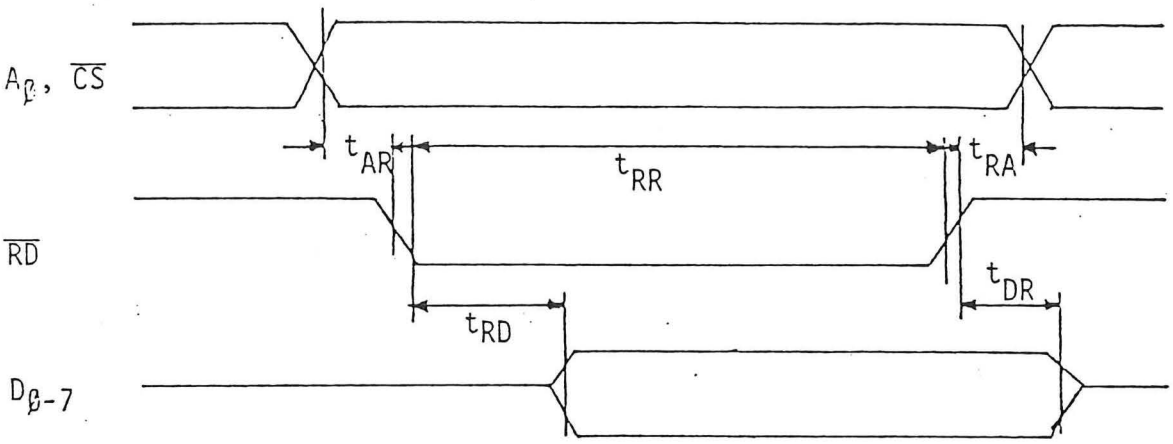
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CLK cycle time	Φ_{CY}		122		1000	ns
CLK pulse width	Φ_D		60			ns
CLK rise time	Φ_r	Voltage at timing measured point 1.0 V & 3.0 V			10	ns
CLK fall time	Φ_f				10	ns
A_0, $\overline{CS}$ set time for $\overline{RD}$	t_{AR}		0			ns
A_0, $\overline{CS}$ hold time for $\overline{RD}$	t_{RA}		0			ns
$\overline{RD}$ pulse width	t_{RR}		250			ns
Data access time for $\overline{RD}$	t_{RD}	C_L = 100 pF			150	ns
Data float time for $\overline{RD}$	t_{DR}		10		100	ns
A_0, $\overline{CS}$ set time for $\overline{WR}$	t_{AW}		0			ns
A_0, $\overline{CS}$ hold time for $\overline{WR}$	t_{WA}		0			ns
$\overline{WR}$ pulse width	t_{WW}		250			ns
Data set time for $\overline{WR}$	t_{DW}		150			ns
Data hold time for $\overline{WR}$	t_{WD}		0			ns
$\overline{RD}$, $\overline{WR}$ reset time	t_{RV}		250			ns

(Continued next page.)

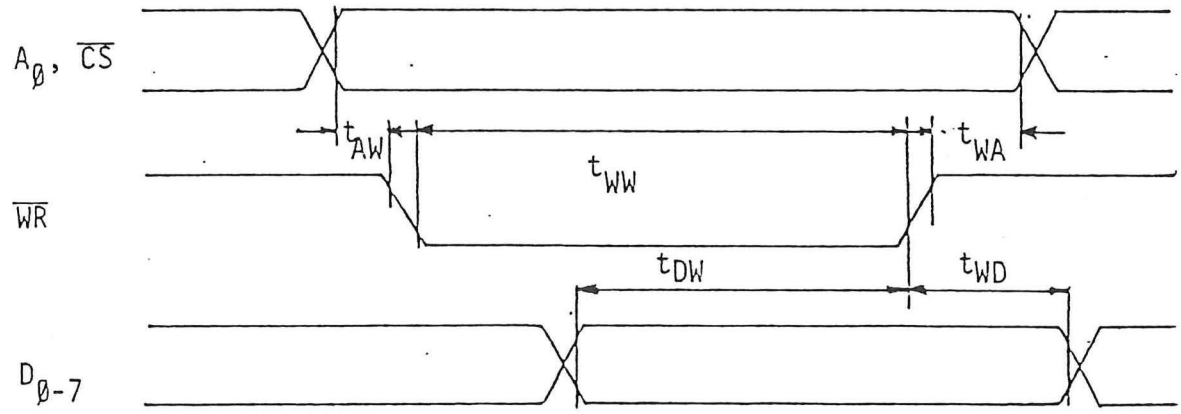
-Timing diagram (7761)



Read operation



Write operation



MC-4760

Absolute maximum ratings (T_a = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	V_{CC}		−0.3 ~ +7.0	V
Power supply voltage	V+		−0.3 ~ +18.0	V
Power supply voltage	V−		−18.0 ~ +0.3	V
Digital input terminal voltage	V_{IT}		−0.3 ~ V_{CC} +0.3	V
Current consumption	P_d		1000	mW
Operating temperature	T_{opt}		−20 ~ +75	°C
Storage temperature	T_{stg}		−40 ~ +85	°C

Recommend operating range

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Input high voltage	V_{IH}	2.0	3.0	V_{CC}	V
Input low voltage	V_{IL}	0.0		0.8	V
Clock frequency	f_{CLK}	1.9	2.0	2.1	MHz
Sampling signal frequency	f_{SMPL}	9.5	10.0	11.0	kHz
Mic input impedance	Z_{INM}	0	600	1000	Ω
Line input impedance	Z_{INL}	0	1000	2000	Ω
Power supply voltage	V_{CC}	4.75	5.00	5.25	V
Power supply voltage (rating: 12V)	1V ±1	11.40	12.00	12.60	V
Power supply voltage (rating: 15V)	1V +1, −2	14.25	15.00	15.75	V

Electrical characteristics (T_a = 25±3°C, 1V±1 = 12V±5%)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
MIC IN input impedance	Z_{MIN}	V_{IN} = * mVrms, f = 1kHz	850	1000	1150	Ω
LINE IN input impedance	Z_{LIN}	V_{IN} = * mVrms, f = 1kHz	8.5	10.0	11.5	kΩ
MIC IN non-distortion input voltage	V_{MIN}	R_{GAPJ} = −, f = 1kHz	120			mVp-p
LINE IN non-distortion input voltage	V_{LIN}	R_{GAPJ} = −, f = 1kHz	12.0			Vp-p
MIC IN min. effective input voltage	$V_{MIN\ min}$	R_{GAPJ} = 75.0Ω, f = 1kHz	2.0			mVp-p
LINE IN min. effective input voltage	$V_{LIN\ min}$	ATC 7~8 = FFH, V_{LPFO} = 5.0 V_{p-p}	200			mVp-p
A_{out} max. output voltage	V_{AOUT}	R_L = 10kΩ	5.0			Vp-p
LPF $_{out}$ max. output voltage	V_{LPFO}	R_L = 100kΩ	5.0			Vp-p
LPF out noise voltage	V_{NS}	R_L = 100kΩ, R_{GAPJ} = 75Ω V_{IN} = 0V, ATC = FFH			3.0	mVp-p

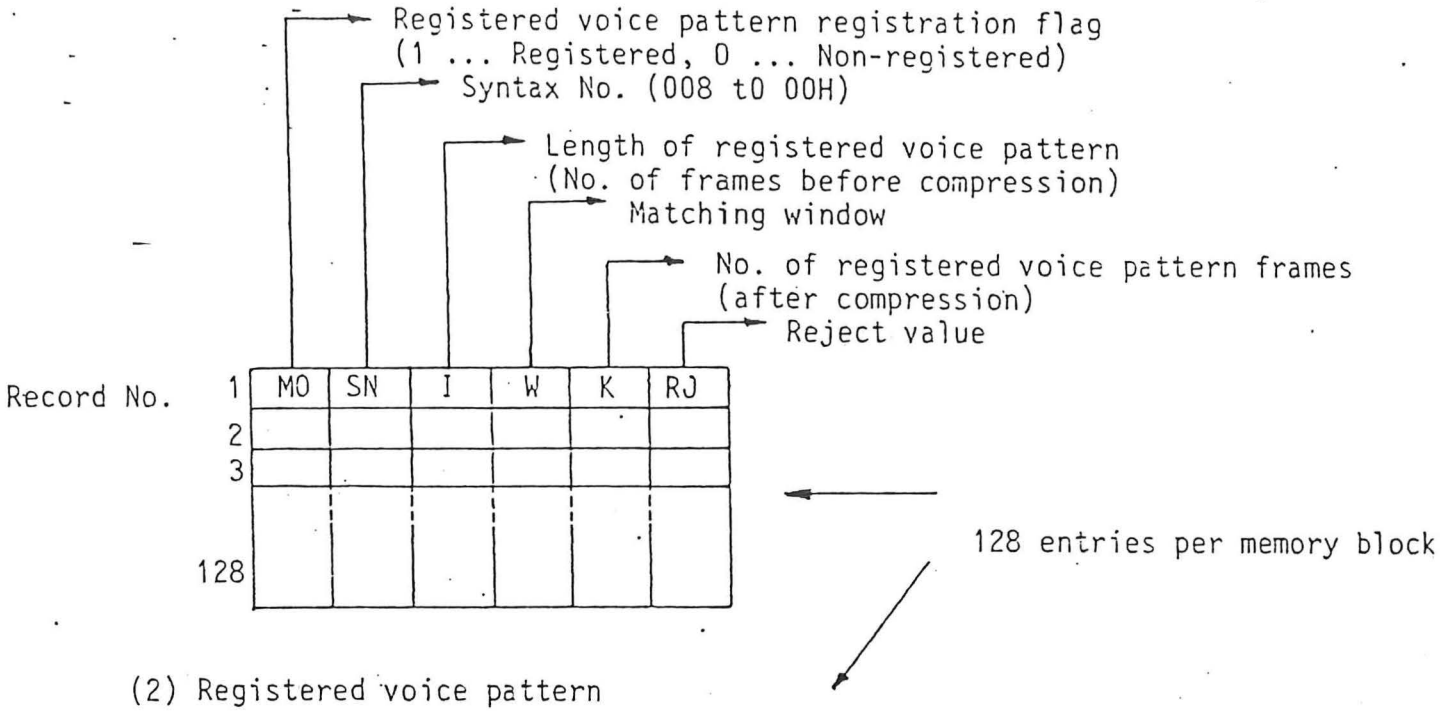
APPENDIX

A. Registered Voice Pattern Data Format

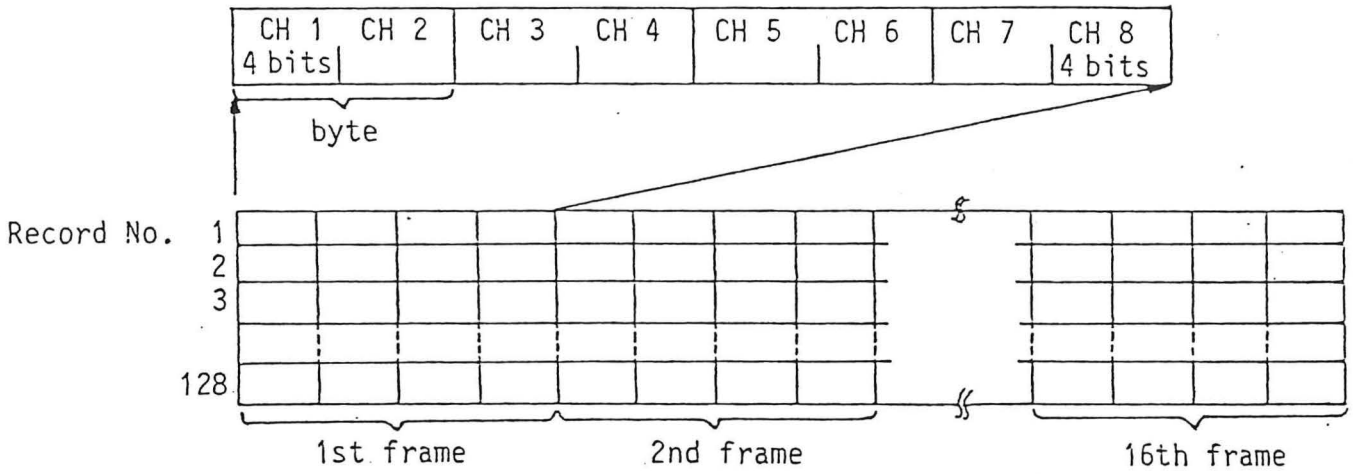
B. Outline of DP Matching Method

C. Example of System Configuration (Circuit Drawings)

(1) Dictionary



(2) Registered voice pattern



(3) Representative data

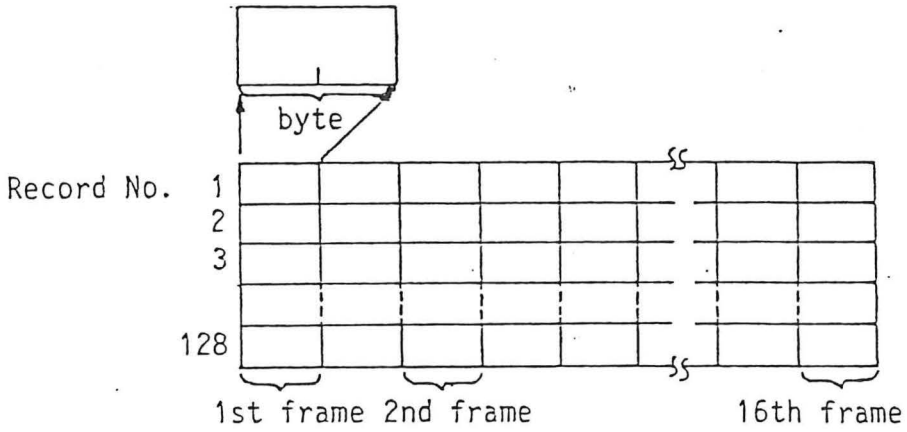


Fig. A.1 Registered Voice Data Configuration

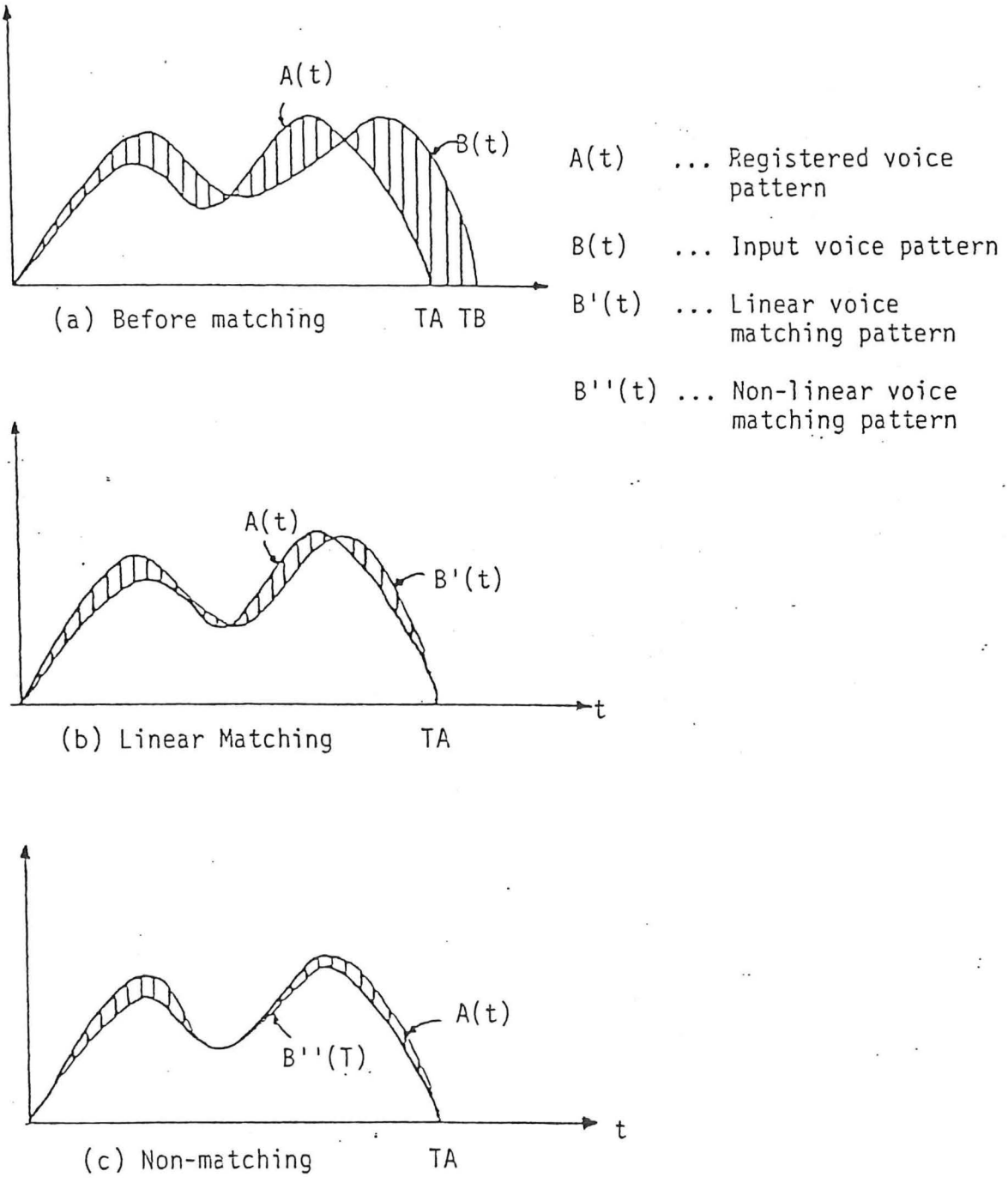


Fig. B.1 Distance between Two Pattern of Unequal Length

This can be expressed by the following formula.

$$D(A, B) = \min_{j = J(i)} \left[\sum_{i} d(i, j) \right] \quad \ldots\ldots (2)$$

In this formula d(i,j) represents the distance $|ai - bj|$ of the vectors between ai and bj. The symbol "min." denotes that a value enclosed in the brackets [ ] will be minimized by the function J(i).

The DP (dynamic programming) method is applied to resolve this kind of problem.

By performing graduated formula calculation with DP method on the i - j plane as shown in Fig. B.2 under the initial conditions g(1,1) = d(1,1), the distance between patterns A and B, D(A, B) can be obtained as D(A,B) = G(I,J).

$$G(i,j) = d(i,j) + \min. \begin{Bmatrix} g(i-1,j) \\ g(i-1, j-1) \\ g(i-1,j-2) \end{Bmatrix} \quad \ldots\ldots (3)$$

The matching window in Fig. B.2 prevents unnecessarily flexible matching and reduces the calculation load.

The function of the DP matching method is, as can be seen, to model the fluctuation of the time axis by using mapping function (ji) and to calculate the simplfied problem.

In comparison with conventional linear matching methods, the DP matching method reduces the erroneous recognition rate to 1/4 to 1/7 and dramatically improves the operating precision.

However, since its calculation load is very large, a special processor is required to perform real-time processing.

History of Modifications

Edition	Page	Modifications
1		Prepared by Mr. Tanaka on March 8, 1982
2		Prepared by Mr. Tanaka on June 5, 1982
3		Prepared by Mr. Ikeda (NIMS Software Div.) on August 31, 1982
	6	Description of the MC-4760 added to system configuration.
	9 to 12	Description of memory configuration, diagrams and drawings concerning the system added to the functional configuration.
	13 to 21	Section on external interfaces established independently.
	22 to 24	Description of command functions established independently and simplified. Diagrams and drawings concerning the system added.
	41 to 53	Description of the 7762 rewritten focusing on external interfaces and signals within the system. Terminal names modified; names and explanations of terminal descriptions modified. Descriptions concerning initial operation and basic timing added.
	54 to 62	Description of the 7762 focusing on the system level added. Terminal names; names and explanations of terminal descriptions modified. Description concerning the initial operation of the 7761 added. Description concerning data I/O and clocks added.
	63 to 71	Description of the MC-4760 entirely modified.