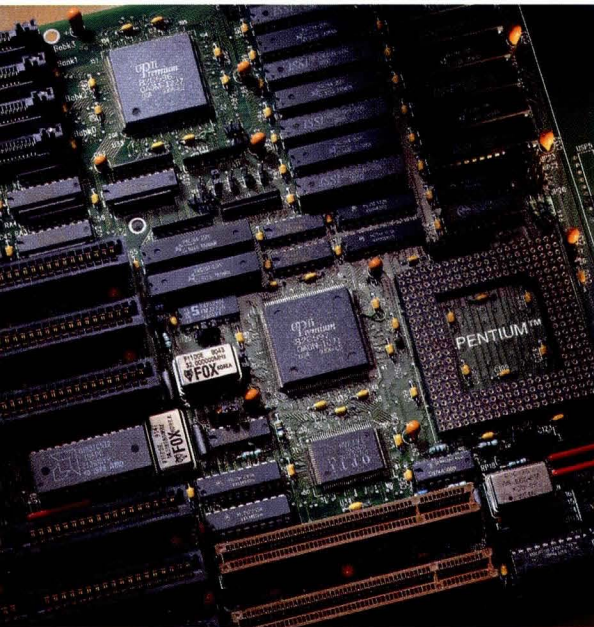
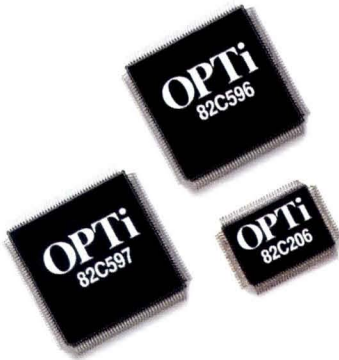


PENTIUM

P
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.....Pentium™ Adaptive Write Back.....

The OPTi design team is proud to present the 64-bit Pentium AT solution with VESA Local bus. As always, the product emphasis is on value. The OPTi PTMAWB is crafted to provide the highest performance but most cost-effective system solution without compromising quality, compatibility or reliability.

The PTMAWB is a top-of-the-line solution for the server/power user market. Flexibility of design without using the most expensive support parts has been given key importance. This ensures the total system cost to be at the high-end 486 level - yet with the high-end Pentium performance.

The PTMAWB has the state-of-the-art AWB cache controller for up to 2 MB of Adaptive Write-back cache support. The DRAM controller also supports posted writes for faster performance on write cycles.

The OPTi PTMAWB-V provides PC servers and PC power users the horsepower of the 64-bit Pentium at 60 MHz and 66 MHz—immediately.

Features/Benefits

- 100% PC/AT compatible
- Fully supports the Intel Pentium microprocessor
- Three chip PC/AT solution: 82C596, 82C597 and 82C206
- Supports Intel Pentium CPU address pipelining
- IX clock source, supporting systems running up to 66 MHz
- Adaptive Write Back, direct-mapped cache with size selections: 64K, 128K, 256K, 512K, 1Mb, 2Mb
- Programmable cache write policy: adaptive write back (AWB), write-back or write through
- Fully programmable cache and DRAM read/write cycles
- Supports 3-2-2-2 cache burst read cycle at 66 MHz
- Built-in TAG auto-invalidation circuitry
- Support for two programmable non-cacheable/system memory "hole" regions
- Supports two banks of 64-bit wide DRAMs with 256K, 512K, 1M, 2M, 4M, and 8M x 36 page-mode DRAMs
- Supports DRAM configurations up to 128 Mb
- Supports 3-3-3-3 pipeline DRAM burst cycles
- DRAM post write buffer
- Provides Flash ROM support
- 33 MHz asynchronous 32-bit VESA VL Local Bus support
- Performance oriented snoop-line comparator for VL/ISA bus masters
- Extended DMA page register
- Asynchronous CPU and VL bus interface
- AT bus clock speed programmability
- Low power, high speed CMOS technology



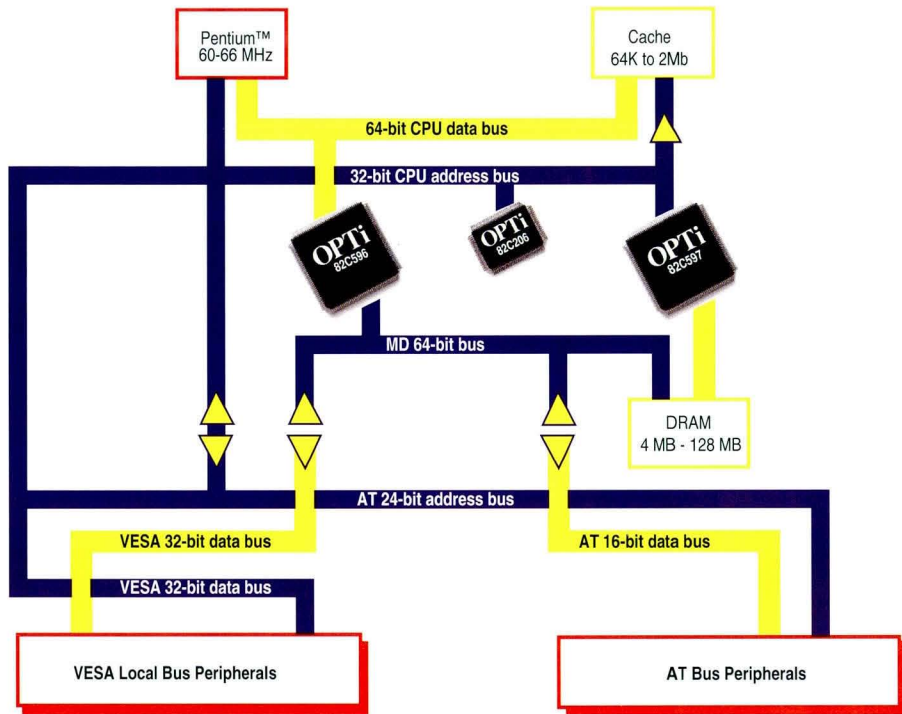
The OPTi PTMAWB-V chipset provides a highly integrated solution for fully compatible, high performance PC/AT platforms. Together with the 82C206 integrated peripherals controller, this chipset supports the Intel Pentium processor in the most cost effective and feature-rich designs available today.

The OPTi PTMAWB-V chipset is comprised of the 82C596 and the 82C597 controllers. The 82C597 SYSC provides the control functions for the host CPU interface, the 33 MHz

asynchronous 32-bit Local bus interface, burst read and write to secondary cache memory and the 64-bit DRAM bus. It also controls the data flow between the CPU bus, the DRAM bus, the Local bus, and the 16/8-bit ISA bus.

The 82C596 ATC integrates the AT bus interface and the data buffers for transfers between the CPU data bus, Local data bus and the DRAM data bus. It also provides ISA to Local bus command translation.

**OPTi
PTMAWB:
The solution
for your high
performance
needs.**



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