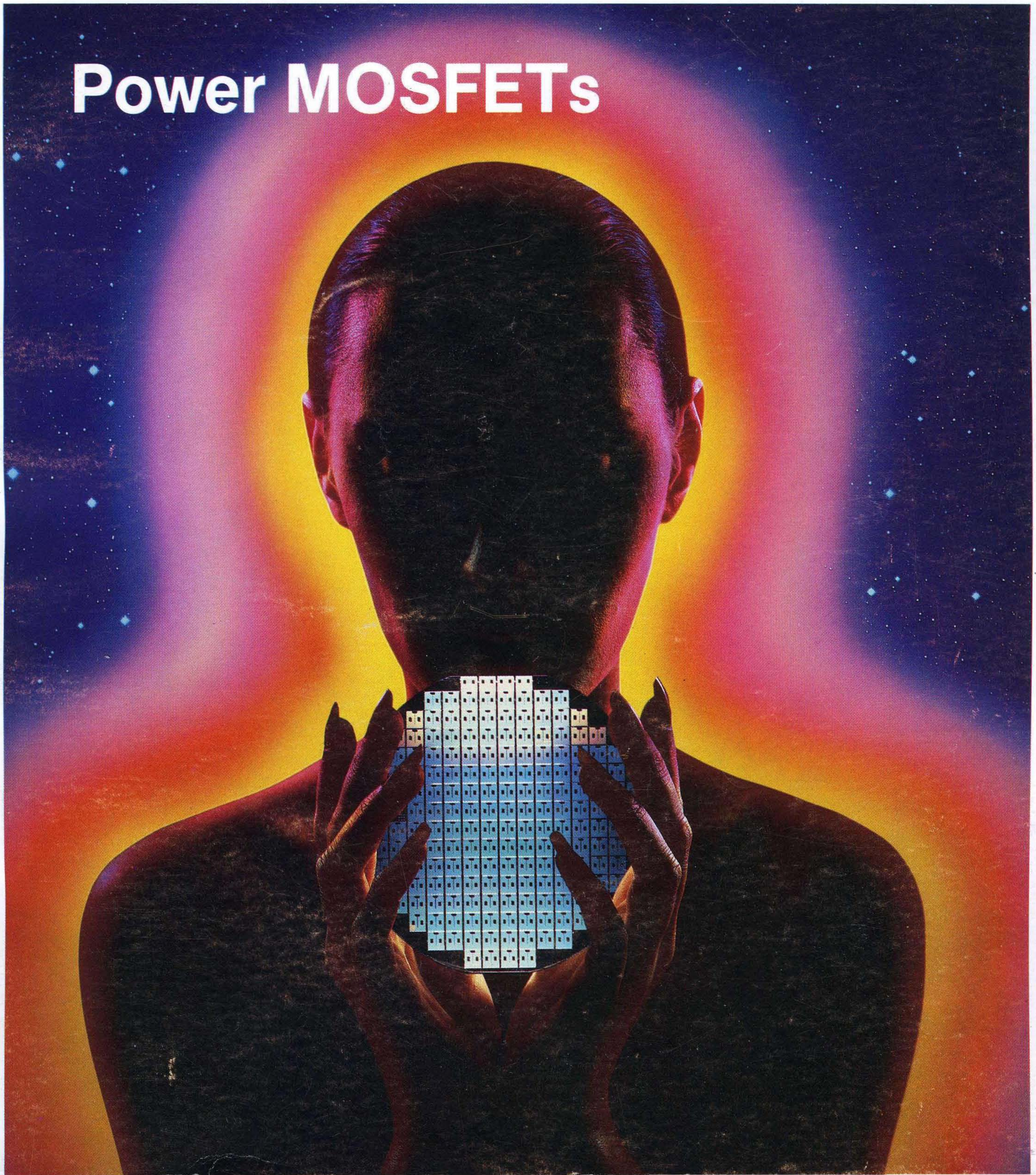
RCA

- Standard Types
- L^2FETs
- COMFETs

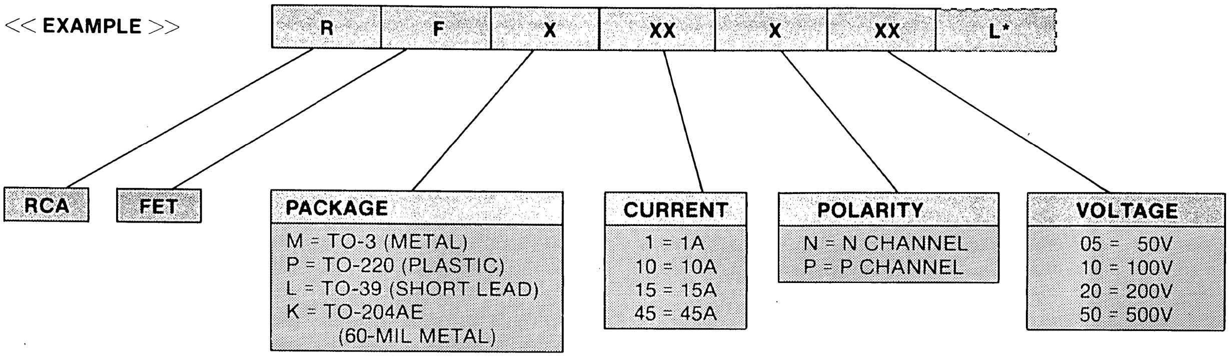
Power MOSFETs



RCA Solid State

Contents

RCA Power MOSFET Nomenclature System



*An "L" suffix is added for Logic-Level FETS.

When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices". Form No. 1CE-402 available from RCA Solid State Division, Box 3200, Somerville, NJ 08876.

Form No. PMP-411A
Printed in USA/4-84

RCA Power MOSFET Products

RCA power MOS field-effect transistors offer unique features that make them especially useful in a wide variety of power-switching applications at frequencies up to several hundred kilohertz. Innovative design techniques and advanced processing technology are used to produce these state-of-the-art power switching devices. The RCA power MOSFET line includes the standard line of power MOSFETs, a newly announced line of low-threshold FETs, called logic-level field-effect transistors, or more simply, L^{2}FETS, and a series of conductivity-modulated FETs, called COMFETs, that considerably extend the voltage and current capabilities of the power MOSFET technology.

Because of its electrically isolated gate, a MOSFET can be described as a high-input-impedance, voltage-controlled device. As a majority-carrier semiconductor, a MOSFET stores no charge, and so can switch fast, faster than a bipolar device. But majority-carrier semiconductors also become more resistive as temperature increases. This effect, brought about by a phenomenon called carrier mobility (where mobility is a term that defines the average velocity of a carrier in terms of the electrical field imposed on it) causes the individual cells of the MOSFET to become more resistive at elevated temperatures and, therefore, makes the over-all MOSFET much less susceptible to the on-chip, localized thermal-runaway problems experienced by bipolar devices.

RCA power MOSFETs are available in both n and p-channel enhancement-mode types (L^{2}FETs are currently available in n-type only) with drain-current (I_{DS}) ratings from 1 to 45 amperes, drain-to-source voltage (V_{DS}) ratings of 50 to 500 volts, and switching times in the nanosecond range. Additional application advantages are offered by exceptionally low drain-to-source on resistances, r_{DS}(on), excellent thermal stability, and safe-operating-area ratings that are limited only by the dissipation capabilities of the devices.

Operation

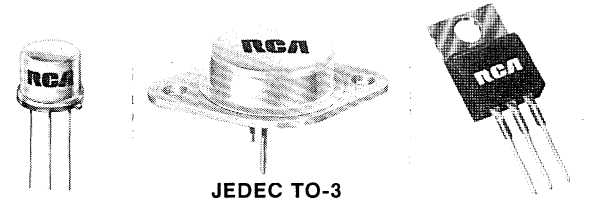
A positive voltage applied to the gate of an n-type MOSFET creates an electric field in the channel region beneath the gate; that is, the positive electric charge on the gate converts the p-region beneath the gate to an n-type region. This surface-inversion phenomenon allows current to flow between the drain and source through an n-type material. In effect, the MOSFET becomes an n-n-n device when in this state. The region between the drain and source can then be represented as a temperature-dependent resistor.

Features

- **Fast switching speeds and low switching losses, both of which are independent of temperature.**
- **No storage time and, thus, no temperature-dependent delay times.**
- **High resistance to thermal runaway.**
- **Simple drive circuitry.**
- **Safe operating area limited only by device dissipation ratings.**
- **Stable gain and switching response over a wide temperature range.**

Packaged Devices and Chips

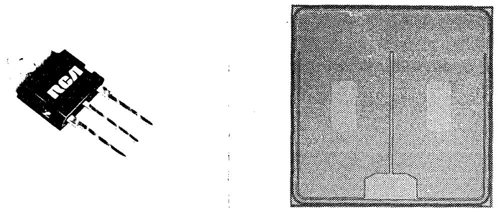
The RCA power MOSFET product line currently includes more than 150 types. A coded type number indicates the current and voltage ratings, identifies n- or p-channel types, and specifies the package for RCA power MOSFETs. The devices are supplied in four basic package styles: TO-39, TO-220AB, TO-3/TO-204MA/TO-204AE, and TO-218. Power MOSFET chips are also available for use in hybrid circuits. Chips may be purchased either in wafer form or as separated die.



JEDEC TO-39

JEDEC TO-3
JEDEC TO-204MA
JEDEC TO-204AE

JEDEC
TO-220AB



JEDEC TO-218AC

Chip

RCA Power MOSFETs are available as packaged devices and in chip form.

RCA Power MOSFET Products

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RFK25N20	104	1500
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RFK25P10	100	1516
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RFK30N15	108	1455
RFK35N08	112	1499
RFK35N10	112	1499
RFK45N05	116	1498
RFK45N06	116	1498
RFL1P08	—	—
RFL1N08L	124	1510
RFL1P10	—	—
RFL1N10L	124	1513
RFL1P12	—	—
RFL1N12L	128	1513
RFL1N15	—	—
RFL1N15L	128	1513
RFL1N18	—	—
RFL1N18L	132	1511
RFL1N20	—	1442
RFL1N20L	132	1511
RFL2N05	—	—
RFL2N06	—	—
RFL4N12	—	—
RFL4N15	—	—
RFM3N45	—	—
RFM3N50	—	—
RFM4N35	174	—
RFM4N40	174	—
RFM6N45	175	—
RFM6N50	174	—
RFM5P12	50	1463
RFM5P15	50	1463
RFM6P08	54	1490
RFM6P10	54	1490
RFM8N18	62	1447
RFM8N18L	136	1514
RFM8N20	62	1447
RFM8N20L	136	1514
RFM8P08	58	1496
RFM8P10	58	1496
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RFM10N15	71	1445
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RFM12N10	76	1386
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RFM12N20	84	1461
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RFM12P10	80	1495
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RFM15N06	88	1478
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RFM15N15	92	1443
RFM18N08	100	1446
RFM18N10	100	1446
RFM25N05	176	—
RFM25N06	176	—
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RFP2N08L	124	1510
RFP2N10	—	—
RFP2N10L	124	1510
RFP2N12	—	—
RFP2N12L	128	1513
RFP2N15	—	—
RFP2N15L	128	1513
RFP2N18	—	—
RFP2N18L	132	1511
RFP2N20	—	—
RFP2N20L	132	1511
RFP3N45	—	—
RFP3N50	—	—
RFP4N05L	174	—
RFP4N06L	174	—
RFP4N35	174	—
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RFP6N45	175	—
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RFP6P08	54	1490
RFP6P10	54	1490
RFP8N18	62	1447
RFP8N18L	136	1514
RFP8N20	62	1447
RFP8N20L	136	1514
RFP8P08	58	1496
RFP8P10	58	1496
RFP10N12	71	1445
RFP10N15	71	1445
RFP12N08	76	1386
RFP12N08L	140	1512
RFP12N10	76	1386
RFP12N10L	140	1512
RFP12N18	84	1461
RFP12N20	84	1461
RFP12P08	80	1495
RFP12P10	80	1495
RFP15N05	88	1478
RFP15N06	88	1478
RFP15N12	92	1443
RFP15N15	92	1443
RFP18N08	96	1446
RFP18N10	96	1446
RFP25N05	100	1492
RFP25N06	100	1492

Logic-Level Power MOSFETs

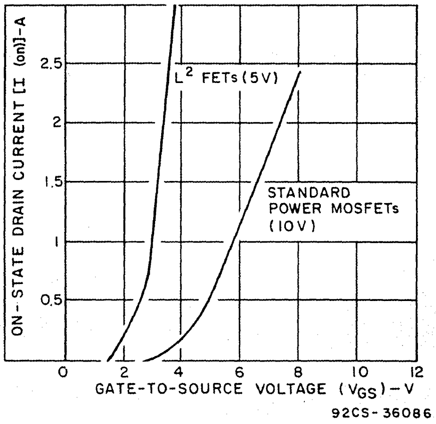
RCA has developed a new series of power MOSFETs that feature a gate-oxide insulation only 50 nm thick — one-half the industry standard for power MOSFETs. The surface inversion of the MOS channel is a direct function of the gate-oxide thickness; consequently, the gate-to-source threshold voltage — i.e., the applied gate voltage required for uncompromised drain characteristics — on the new series of devices is only half that of conventional power MOSFETs.

The reduced gate-drive requirement allows on-off switching of the new MOSFETs directly from logic-level voltage of 5 volts, rather than the nominal 10 volts required for conventional power MOSFETs with 100-nm-thick gate oxides. For this reason, the new devices are called *logic-level Fets* (or more simply L^2FETs). The L^2FETs feature the same low on-resistance characteristics, drain-current ratings, and blocking-voltage capability of corresponding types with the higher gate-drive requirements. In addition, the L^2FETs offer twice the transconductance and half the threshold-voltage temperature coefficient of conventional types having the same on resistance and voltage ratings and demonstrate a comparable switching speed for the same gate drive power.

The initial series of L^2FETs includes 32 n-channel types with drain-current ratings that range from 1 to 15 amperes, drain-to-source voltage ratings of 50 to 200 volts, and are totally interchangeable with corresponding standard power MOSFETs, but offer twice the gate sensitivity. They are supplied in three basic package styles: TO-3, TO-39, and TO-220 (plastic).

Special Features

- 5-Volt Gate Drive
- Compatible with CMOS, QMOS, TTL, PMOS, and NMOS Logic Circuits
- Compatible with Automotive Drive Requirements



Comparison of standard power MOSFETs and L^2FETs.

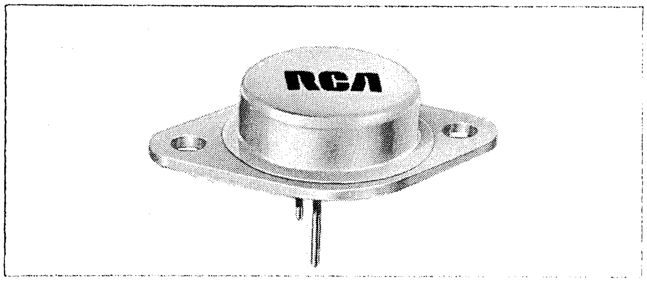
L^2FETs — N-Channel Types

RCA TYPE	PKG	I_D (A)	V_{DSS} (V)	P_D (W)	$r_{DS(ON)}$ OHMS
•RFL1N08L	TO-39	1	80	8.33	1.40
•RFL1N10L	TO-39	1	100	8.33	1.40
•RFL1N12L	TO-39	1	120	8.33	2.15
•RFL1N15L	TO-39	1	150	8.33	2.15
•RFL1N18L	TO-39	1	180	8.33	3.65
•RFL1N20L	TO-39	1	200	8.33	3.65
RFL2N05L	TO-39	2	50	8.33	0.80
RFL2N06L	TO-39	2	60	8.33	0.80
RFP2N08L	TO-220	2	80	25	1.25
RFP2N10L	TO-220	2	100	25	1.25
RFP2N12L	TO-220	2	80	25	2.00
RFP2N15L	TO-220	2	100	25	2.00
•RFP2N18L	TO-220	2	180	25	3.50
•RFP2N20L	TO-220	2	200	25	3.50
RFP4N05L	TO-220	4	50	25	0.80
RFP4N06L	TO-220	4	60	25	0.80
•RFM8N18L	TO-3	8	180	60	0.60
•RFM8N20L	TO-3	8	200	60	0.60
•RFP8N18L	TO-220	8	180	60	0.60
•RFP8N20L	TO-220	8	200	60	0.60
RFM10N12L	TO-3	10	120	60	0.30
RFM10N15L	TO-3	10	150	60	0.30
RFP10N12L	TO-220	10	120	60	0.30
RFP10N15L	TO-220	10	150	60	0.30
•RFM12N08L	TO-3	12	80	100	0.20
•RFM12N10L	TO-3	12	100	100	0.20
•RFP12N08L	TO-220	12	80	75	0.20
•RFP12N10L	TO-220	12	100	75	0.20
RFM15N05L	TO-3	15	50	60	0.15
RFM15N06L	TO-3	15	60	60	0.15
RFP15N05L	TO-220	15	50	60	0.15
RFP15N06L	TO-220	15	60	60	0.15

•Available from stock others available second half of 1984.

RCA Power MOSFET Products

Standard Power MOSFETs in TO-3 Package

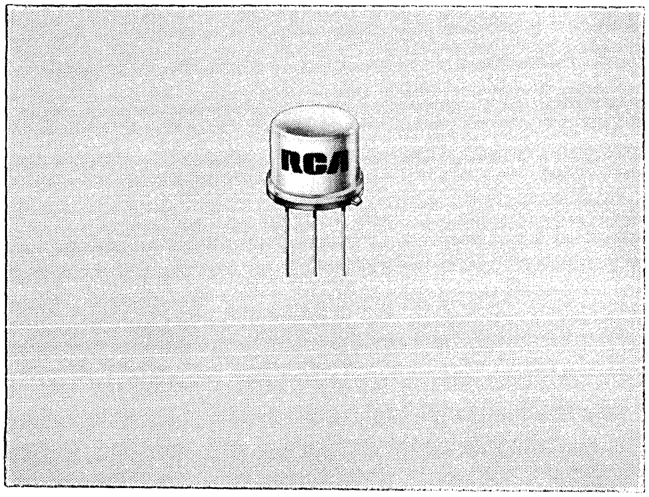


TYPE	CHANNEL	I_D	V_{DSS}	$r_{DS(ON)}$
50V — 100V				
RFM6P08	P	6.0	80	0.60
RFM6P10	P	6.0	100	0.60
RFM8P08	P	8.0	80	0.40
RFM8P10	P	8.0	100	0.40
IRF132	N	12.0	100	0.25
IRF133	N	12.0	60	0.25
RFM12N08	N	12.0	80	0.20
RFM12N10	N	12.0	100	0.20
RFM12P08	P	12.0	80	0.30
RFM12P10	P	12.0	100	0.30
IRF130	N	14.0	100	0.18
IRF131	N	14.0	60	0.18
RFM15N05	N	15.0	50	0.15
RFM15N06	N	15.0	60	0.15
RFM18N08	N	18.0	80	0.12
RFM18N10	N	18.0	100	0.12
RFK25P08	P	25.0	80	0.20
RFK25P10	P	25.0	100	0.20
*RFM25N05	N	25.0	50	.085
*RFM25N06	N	25.0	60	.085
RFK35N08	N	35.0	80	0.06
RFK35N10	N	35.0	100	0.06
RFK45N05	N	45.0	50	0.04
RFK45N06	N	45.0	60	0.04
120V — 200V				
RFM5P12	P	5.0	120	1.00
RFM5P15	P	5.0	150	1.00
RFM8N18	N	8.0	180	0.60
RFM8N20	N	8.0	200	0.60
RFM10N12	N	10.0	120	0.30
RFM10N15	N	10.0	150	0.30
*RFM10P12	P	10.0	120	0.50
*RFM10P15	P	10.0	150	0.50
RFM12N18	N	12.0	180	0.25
RFM12N20	N	12.0	200	0.25
RFM15N12	N	15.0	120	0.15
RFM15N15	N	15.0	150	0.15
IRF252	N	25.0	150	0.12
RFK25N18	N	25.0	180	0.15
RFK25N20	N	25.0	200	0.15
IRF251	N	30.0	150	.085
RFK30N12	N	30.0	120	.085
RFK30N15	N	30.0	150	.085
350V — 500V				
IRF422	N	2.0	500	4.00
IRF423	N	2.0	450	4.00
IRF420	N	2.5	500	3.00
IRF421	N	2.5	450	3.00
RFM3N45	N	3.0	450	3.00
RFM3N50	N	3.0	500	3.00
*RFM4N35	N	4.0	350	2.00
*RFM4N40	N	4.0	400	2.00
*RFM6N45	N	6.0	450	1.50
*RFM6N50	N	6.0	500	1.50
*RFM7N35	N	7.0	350	1.00
*RFM7N40	N	7.0	400	1.00
RFK10N45	N	10.0	450	0.85
RFK10N50	N	10.0	500	0.85
*RFK12N35	N	12.0	350	0.50
*RFK12N40	N	12.0	400	0.50

Standard Power MOSFETs in TO-39 Package

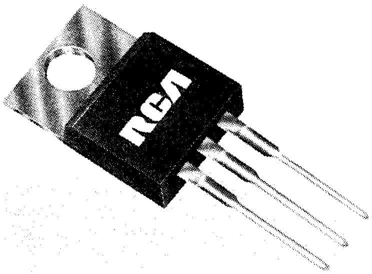
TYPE	CHANNEL	I_D	V_{DSS}	$r_{DS(ON)}$
50V — 100V				
RFL1N08	N	1.0	80	1.25
RFL1N10	N	1.0	100	1.25
*RFL1P08	P	1.0	80	3.50
*RFL1P10	P	1.0	100	3.50
RFL2N05	N	2.0	50	0.80
RFL2N06	N	2.0	60	0.80
120V — 200V				
RFL1N12	N	1.0	120	2.00
RFL1N15	N	1.0	150	2.00
RFL1N18	N	1.0	180	3.00
RFL1N20	N	1.0	200	3.00
RFL4N12	N	4.0	120	0.30
RFL4N15	N	4.0	150	0.30

*Planned for second half of 1984.



Standard Power MOSFETs in TO-220 Package

TYPE	CHANNEL	I_D	V_{DSS}	$r_{DS(ON)}$
50V — 100V				
RFP2N08	N	2.0	80	1.25
RFP2N10	N	2.0	100	1.25
*RFP2P08	P	2.0	80	3.50
*RFP2P10	P	2.0	100	3.50
IRF512	N	3.5	100	0.80
IRF513	N	3.5	60	0.80
IRF510	N	4.0	100	0.60
IRF511	N	4.0	60	0.60
RFP4N05	N	4.0	50	0.80
RFP4N06	N	4.0	60	0.80
RFP6P08	P	6.0	80	0.60
RFP6P10	P	6.0	100	0.60
IRF522	N	7.0	100	0.40
IRF523	N	7.0	60	0.40
IRF520	N	8.0	100	0.30
IRF521	N	8.0	60	0.30
RFP8P08	P	8.0	80	0.40
RFP8P10	P	8.0	100	0.40
IRF532	N	12.0	100	0.25
IRF533	N	12.0	60	0.25
RFP12N08	N	12.0	80	0.20
RFP12N10	N	12.0	100	0.20
RFP12P08	P	12.0	80	0.30
RPF12P10	P	12.0	100	0.30
IRF530	N	14.0	100	0.18
IRF531	N	14.0	60	0.18
RFP15N05	N	15.0	50	0.15
RFP15N06	N	15.0	60	0.15
RFP18N08	N	18.0	80	0.12
RFP18N10	N	18.0	100	0.12
*RFP25N05	N	25.0	50	.085
*RFP25N06	N	25.0	60	.085
120V — 200V				
RFP2N12	N	2.0	120	2.00
RFP2N15	N	2.0	150	2.00
RFP2N18	N	2.0	180	3.00
RFP2N20	N	2.0	200	3.00
RFP5P12	P	5.0	120	1.00
RFP5P15	P	5.0	150	1.00
RFP8N18	N	8.0	180	0.60
RFP8N20	N	8.0	200	0.50
RPF10N12	N	10.0	120	0.30
RFP10N15	N	10.0	150	0.30
*RFP10P12	P	10.0	120	0.50
*RFP10P15	P	10.0	150	0.50
RFP12N18	N	12.0	180	0.25
RPF12N20	N	12.0	200	0.25
RFP15N12	N	15.0	120	0.15
RFP15N15	N	15.0	150	0.15
350V — 500V				
*RFP1N35	N	1.0	350	9.00
*RFP1N40	N	1.0	400	9.00
RFP3N45	N	3.0	450	3.00
RFP3N50	N	3.0	500	3.00
*RFP4N35	N	4.0	350	2.00
*RFP4N40	N	4.0	400	2.00
*RFP6N45	N	6.0	450	1.50
*RFP6N50	N	6.0	500	1.50
*RFP7N35	N	7.0	350	1.00
*RFP7N40	N	7.0	400	1.00



Conductivity-Modulated Field-Effect Transistors — COMFETS

RCA Dev. No.	CHANNEL	I_D	V_{DSS}	$V_{DS(ON)}$
In TO-204 Package				
TA9437A	N	10 A	350 V	2 V
TA9437B	N	10 A	400 V	2 V
In TO-220 Package				
TA9438A	N	10 A	350 V	2 V
TA9438B	N	10 A	400 V	2 V

High-Reliability Power MOSFETs

RCA has developed an aggressive program to qualify power MOSFETs to MIL-S-19500. This plan includes qualification to the TXV level. This program has two parts, (a) a plan to qualify RCA devices to existing QPL specifications, and (b) a plan to proprose new QPL types to fill "product holes" in the existing MIL type matrix.

Authorization has already been received from DESC for RCA to generate data for qualification of types 2N6764 and 2N6766. This program is well underway and we anticipate qualification from DESC in June 1984.

Also, in the plan are seven additional RCA candidates for types already on the QPL, four original RCA QPL submissions on 60-volt N-channel types, four P-channel 100-V types and six logic-level N-channel types for 60-V, 100-V, and 200-V applications.

In addition to planned QPL types, RCA will offer high-reliability custom selections of all hermetic Power MOSFETs.

RCA Power MOSFET Products

1984 Product Matrix

N-Channel Types

Drain Current I_D

Voltage, V_{DSS}	50 V	60 V	80 V	100 V	120 V	150 V	180 V	200 V	350 V	400 V	450 V	500 V
1A			RFL1N08 TO-39 1.40 Ω•	RFL1N10 TO-39 1.40 Ω•	RFL1N12 TO-39 2.15 Ω•	RFL1N15 TO-39 2.15 Ω•	RFL1N18 TO-39 3.65 Ω•	RFL1N20 TO-39 3.65 Ω•	RFP1N35 TO-220 9.00 Ω•	RFP1N40 TO-220 9.00 Ω•		
2A	RFL2N05 TO-39 0.80 Ω•	RFL2N06 TO-39 0.80 Ω•	RFP2N08 TO-220 1.25 Ω•	RFP2N10 TO-220 1.25 Ω•	RFP2N12 TO-220 2.00 Ω•	RFP2N15 TO-220 2.00 Ω•	RFP2N18 TO-220 3.50 Ω•	RFP2N20 TO-220 3.50 Ω•				
3A											RFP3N45 TO-220 3.00 Ω• RFM3N45 TO-3 3.00 Ω•	RFP3N50 TO-220 3.00 Ω• RFM3N50 TO-3 3.00 Ω•
4A	RFP4N05 TO-220 0.80 Ω•	RFP4N06 TO-220 0.80 Ω•			RFL4N12 TO-39 0.40 Ω•	RFL4N15 TO-39 0.40 Ω•			RFP4N35 TO-220 2.0 Ω• RFM4N35 TO-3 2.0 Ω•	RFP4N40 TO-220 2.0 Ω• RFM4N40 TO-3 2.0 Ω•		
6A											RFP6N45 TO-220 1.50 Ω• RFM6N45 TO-3 1.50 Ω•	RFP6N50 TO-220 1.50 Ω• RFM6N50 TO-3 1.50 Ω•
7A									RFP7N35 TO-220 1.00 Ω• RFM7N35 TO-3 1.00 Ω•	RFP7N40 TO-220 1.00 Ω• RFM7N40 TO-3 1.00 Ω•		
8A							RFP8N18 TO-220 0.60 Ω• RFM8N18 TO-3 0.60 Ω•	RFP8N20 TO-220 0.60 Ω• RFM8N20 TO-3 0.60 Ω•				
10A					RFP10N12 TO-220 0.30 Ω• RFM10N12 TO-3 0.30 Ω•	RFP10N15 TO-220 0.30 Ω• RFM10N15 TO-3 0.30 Ω•					RFK10N45 TO-204AE 0.85 Ω•	RFK10N50 TO-204AE 0.85 Ω•
12A			RFP12N08 TO-220 0.20 Ω• RFM12N08 TO-3 0.20 Ω•	RFP12N10 TO-220 0.20 Ω• RFM12N10 TO-3 0.20 Ω•			RFP12N18 TO-220 0.25 Ω• RFM12N18 TO-3 0.25 Ω•	RFP12N20 TO-220 0.25 Ω• RFM12N20 TO-3 0.25 Ω•	RFK12N35 TO-204AE 0.50 Ω•	RFK12N40 TO204AE 0.50 Ω•		
15A	RFP15N05 TO-220 0.15 Ω• RFM15N05 TO-3 0.15 Ω•	RFP15N06 TO-220 0.15 Ω• RFM15N06 TO-3 0.15 Ω•			RFP15N12 TO-220 0.15 Ω• RFM15N12 TO-3 0.15 Ω•	RFP15N15 TO-220 0.15 Ω• RFM15N15 TO-3 0.15 Ω•						
18A			RFP18N08 TO-220 0.12 Ω• RFM18N08 TO-3 0.12 Ω•	RFP18N10 TO-220 0.12 Ω• RFM18N10 TO-3 0.12 Ω•								
25A	RFP25N05 TO-220 0.085 Ω• RFM25N05 TO-3 0.085 Ω•	RFP25N06 TO-220 0.085 Ω• RFM25N06 TO-3 0.085 Ω•					RFK25N18 TO-204AE 0.15 Ω•	RFK25N20 TO-204AE 0.15 Ω•				
30A					RFK30N12 TO-204AE 0.085 Ω• RFH30N12 TO-218 0.085 Ω•	RFK30N15 TO-204AE 0.085 Ω• RFH30N15 TO-218 0.085 Ω•						
35A			RFK35N08 TO-204AE 0.06 Ω•	RFK35N10 TO-204AE 0.06 Ω•								
45A	RFK45N05 TO-204AE 0.04 Ω•	RFK45N06 TO-204AE 0.04 Ω•										

1984 Product Matrix

P-Channel Types

Voltage, V_{DSS} Drain Current I_D	80 V	100 V	120 V	150 V
1A	RFL1P08 TO-39 3.50 Ω•	RFL1P10 TO-39 3.50 Ω•		
2A	RFP2P08 TO-220 3.50 Ω•	RFP2P10 TO-220 3.50 Ω•		
3A				
4A				
5A			RFP5P12 TO-220 1.00 Ω• RFM5P12 TO-3 1.00 Ω•	RFP5P15 TO-220 1.00 Ω• RFM5P15 TO-3 1.00 Ω•
6A	RFP6P08 TO-220 0.60 Ω• RFM6P08 TO-3 0.60 Ω•	RFP6P10 TO-220 0.60 Ω• RFM6P10 TO-3 0.60 Ω•		
7A				
8A	RFP8P08 TO-220 0.40 Ω• RFM8P08 TO-3 0.40 Ω•	RFP8P10 TO-220 0.40 Ω• RFM8P10 TO-3 0.40 Ω•		
10A			RFP10P12 TO-220 0.50 Ω• RFM10P12 TO-3 0.50 Ω•	RFP10P15 TO-220 0.50 Ω• RFM10P15 TO-3 0.50 Ω•
12A	RFP12P08 TO-220 0.30 Ω• RFM12P08 TO-3 0.30 Ω•	RFP12P10 TO-220 0.30 Ω• RFM12P10 TO-3 0.30 Ω•		
15A				
18A				
25A	RFK25P08 TO-204AE 0.20 Ω• RFH25P08 TO-218 0.20 Ω•	RFK25P10 TO-204AE 0.20 Ω• RFH25P10 TO-218 0.20 Ω•		
30A				
35A				

Logic-Level FET's

	50 V	60 V	80 V	100 V	120 V	150 V	180 V	200 V
1A			RFL1N08L TO-39 1.40 Ω•	RFL1N10L TO-39 1.40 Ω•	RFL1N12L TO-39 2.15 Ω•	RFL1N15L TO-39 2.15 Ω•	RFL1N18L TO-39 3.65 Ω•	RFL1N20L TO-39 3.65 Ω•
2A	RFL2N05L TO-39 0.80 Ω•	RFL2N06L TO-39 0.80 Ω•	RFP2N08L TO-39 1.25 Ω•	RFP2N10L TO-220 1.25 Ω•	RFP2N12L TO-220 2.00 Ω•	RFP2N15L TO-220 2.00 Ω•	RFP2N18L TO-220 3.50 Ω•	RFP2N20L TO-220 3.50 Ω•
3A								
4A	RFP4N05L TO-220 0.80 Ω•	RFP4N06L TO-220 0.80 Ω•						
5A								
6A								
7A								
8A							RFP8N18L TO-220 0.60 Ω• RFM8N18L TO-3 0.60 Ω•	RFP8N20L TO-220 0.60 Ω• RFM8N20L TO-3 0.60 Ω•
10A					RFP10N12L TO-220 0.30 Ω• RFM10N12L TO-3 0.30 Ω•	RFP10N15L TO-220 0.30 Ω• RFM10N15L TO-3 0.30 Ω•		
12A			RFP12N08L TO-220 0.20 Ω• RFM12N08L TO-3 0.20 Ω•	RFP12N10L TO-220 0.20 Ω• RFM12N10L TO-3 0.20 Ω•				
15A	RFP15N05L TO-220 0.15 Ω• RFM15N05L TO-3 0.15 Ω•	RFP15N06L TO-220 0.15 Ω• RFM15N06L TO-3 0.15 Ω•						
18A								
25A								
30A								
35A								

☐ Available from stock ▨ Planned for 1984 announcement

Design and Performance Characteristics

Power MOSFET structure

The RCA power MOSFET structure integrates vertical and horizontal geometries to achieve its unique characteristics. RCA's power MOSFETs are manufactured using the vertical double-diffused process called VDMOS, or simply DMOS. A DMOS MOSFET silicon chip is structured with a large number of closely packed hexagonal cells. The number of cells varies according to the dimensions of the chip. For example, 240-by-240-mil chips contain 25,000 hexagonal cells. The area of each cell is 1000 square microns, and the total packing density may be as high as 113,000 cells (with as much as 7.5 meters of channel periphery) per square centimeter of active area.

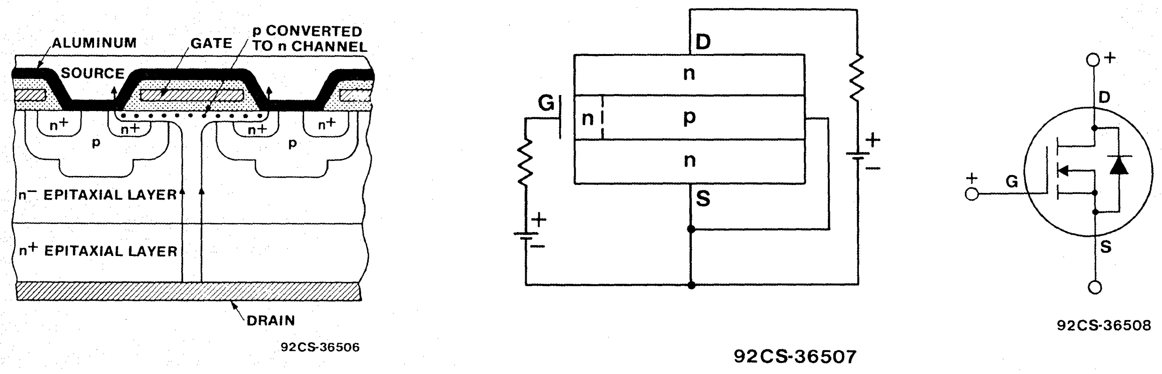
The structures of the standard, L^2FET, and COMFET n-channel devices are basically the same. Both the standard power MOSFET and the L^2FET are based on an n^+ substrate, the COMFET on a p^+ substrate. In addition, the COMFET structure includes a median n^+ epitaxial layer. (The reason for this layer is explained in a later section.) The channel regions for all MOSFETs are created by a double (DMOS) diffusion of p and n-type material into the top epitaxial layer of the substrate. A thin oxide then covers these regions.

The industry standard thickness of this oxide, or gate insulator, is 100 nanometers, the oxide thickness used in both standard MOSFETs and COMFETs. In L^2FETs, however, the thickness of this insulator is only 50 nanometers, the chief structural difference between this device and conventional 10-volt MOSFETs, and is the prime reason for lower-voltage gate-drive requirement of the L^2FET.

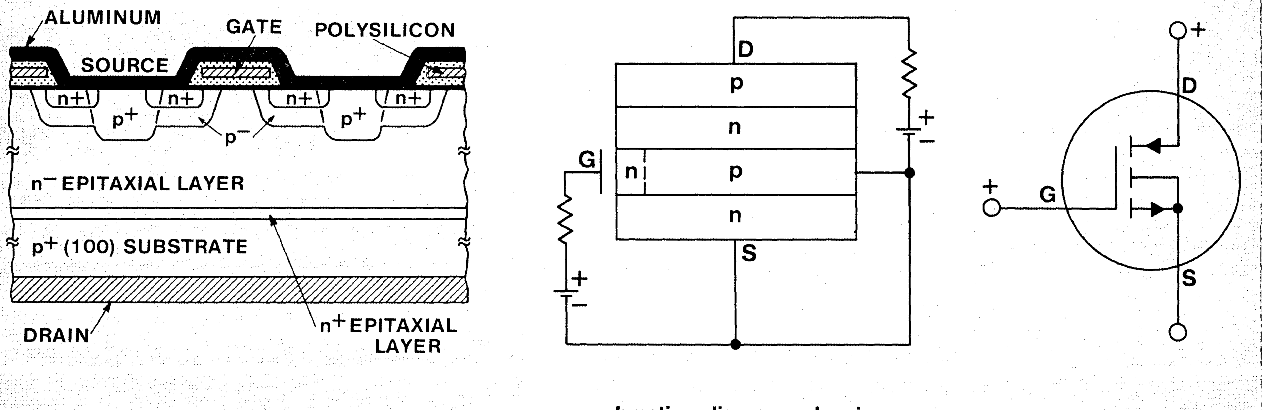
A polysilicon layer is deposited on the oxide. This layer serves as the gate electrode for the device and creates the electric field over the channel. An insulating oxide and glass layer is then deposited over the polysilicon layer. Finally, all the source cells are connected together by a single metallization layer to form the source terminal, and the back side of the chip is metallized to form the drain terminal.

The designs of RCA power MOSFET structures are optimized to achieve simultaneously high voltage, current, and dissipation capability, together with fast

RCA N-CHANNEL POWER MOSFET (STANDARD TYPE OR L²FET)



COMFET (CONDUCTIVITY-MODULATED FIELD-EFFECT TRANSISTOR)



Cross sections of chip structures.

Junction diagrams showing biasing arrangements

Schematic symbols

RCA n-channel standard power MOSFET or L^2FET (top) and COMFET (bottom).

switching speeds, on competitively sized chips. The critical considerations are:

1. A low resistance, $r_{DS}(on)$, from the drain to the source.
2. The resistivity and spacings of the silicon layers necessary to assure the required drain-to-source voltage breakdown capability.
3. A uniform gate-to-source threshold voltage.
4. Minimizing the effect of device junction capacitances on switching speed.

The standard MOSFET and the L^2FET geometries form an inherent diode in an inverse parallel connection. This diode is very useful as the clamp diode in inductive-load switching circuits. The COMFET geometry yields the equivalent of an MOS-gated thyristor circuit except for the presence of the shunting resistance R_s in each unit cell. This resistance has the effect of preventing latching over a wide current and voltage operating range.

The resultant structures feature low leakage currents, good thermal characteristics (low thermal resistance and excellent thermal stability), large safe-operating areas, and high operating efficiencies.

Drain-to-Source On Resistance, $r_{DS}(on)$

The multiple-cell construction used in RCA power MOSFETs substantially reduces the resistance from drain to source when the device is in the on state. The on resistance $r_{DS}(on)$, of the standard MOSFET and L^2FET devices, which is specified at one-half the rated drain current, typically range from 0.04 ohm for a 60-volt, 6-by-6-mm chip to 20 ohms for a 500-volt, 1.5-by-1.5-mm chip. When $r_{DS}(on)$ is minimized, the device provides superior power-switching performance because the voltage drop from drain to source is also minimized for a given value of drain-to-source current.

Since the path between drain and source is essentially resistive, because of the surface-inversion phenomenon, each cell in the device can be assumed to contribute an amount, r_N, to the total resistance. An individual cell has a fairly low resistance, but to minimize $r_{DS}(on)$, it is necessary to put a large number of cells in parallel on a chip. In general, therefore, the greater the number of paralleled cells on a chip, the lower its $r_{DS}(on)$ value:

$$r_{DS}(on) = r_N/N \qquad (1)$$

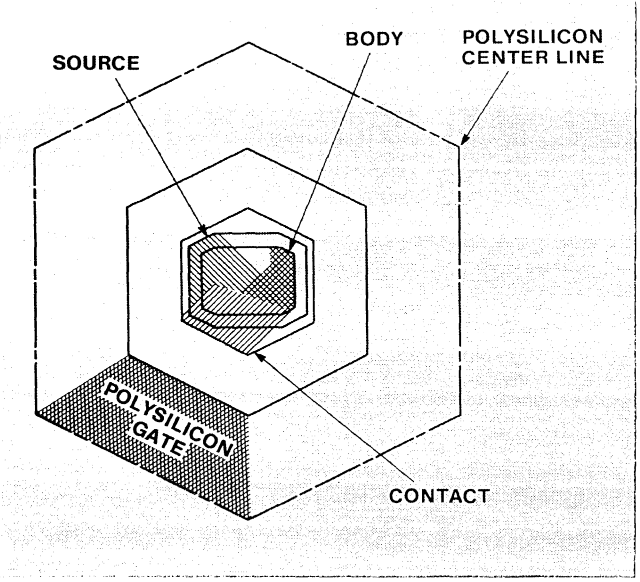
where N is the number of cells.

In reality, $r_{DS}(on)$ is composed of three separate resistances. The value of $r_{DS}(on)$ at any point on the curve is found by adding the values of the three components at that point:

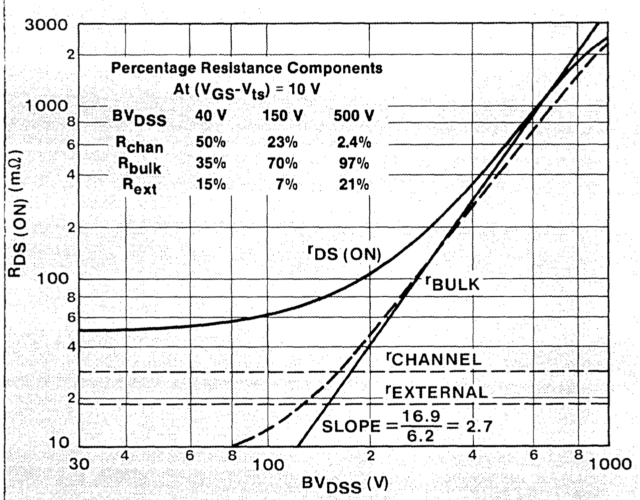
$$r_{DS}(on) = r_{bulk} + r_{chan} + r_{ext}$$

where r_{chan} represents the resistance of the channel beneath the gate, and r_{ext} includes all resistances resulting from the substrate, solder connections, leads, and the package. r_{bulk} represents the resistance resulting from the narrow neck of n material between the two p layers, plus the resistance of the current path below the neck and through the body of the device to the drain.

The resistances r_{chan} and r_{ext} are completely independent of voltage, while r_{bulk} is highly dependent on applied voltage. Below about 150 volts, $r_{DS}(on)$ is dominated by the sum of r_{chan} and r_{ext}. Above 150 volts, $r_{DS}(on)$ is increasingly dominated by r_{bulk}. Obviously, $r_{DS}(on)$ must increase with increasing breakdown-voltage capability of a MOSFET or chip size must be increased to accommodate more cells.



Hexagonal unit cell used in RCA power MOSFET chips.



Three resistive components contribute to over-all value of the on resistance $r_{DS(on)}$.

Design and Performance Characteristics

Use of CAD Techniques to Optimize Power MOSFET Design

An RCA-developed computer program is used to optimize the many variables involved in the design of the hexagonal MOS/FET chip. (See sample program on page 5.) This optimization must be consistent with practical tradeoffs of tolerances, processing yields, and other factors. Accordingly, the computer-aided-design (CAD) techniques employed are reviewed continuously as new processing equipment and techniques become available. In this way, the end-user is assured that state-of-the-art products will always be available.

On-Resistance Calculations — The on-resistance is a complex function of many contributing resistances. All computer calculations of the total on-resistance quantity are carried out at zero drain voltage in order to obtain a meaningful result.

Wire resistance and substrate resistance are usually small, typically in the order of 5 per cent of the over-all total. The metal resistance used in the calculation of on-resistance is a lumped-constant approximation in which certain assumptions are made relative to the placement of the source pad and the size of the wire-bond "foot print." Provisions are included for multiple source pads.

The channel resistance, which consists of several parts, has a complex effect on the on-resistance calculation. The first part consists of the metal channel length provided by the body lateral diffusion and bounded by the source and epitaxial regions. In this part, the surface concentration varies by one or more orders of magnitude and results in a graded threshold voltage along the length of the channel. The second includes the added channel length that results from the zero-bias depletion width. For high-voltage devices, the depletion-width channel-resistance component may exceed the diffused-channel resistance component. The third part of the channel resistance is a distributed portion that is attributable to the combination of the lateral current through the accumulation beneath the gate in the "neck" region and the vertical current in this same region. Finally, a fourth component results solely from the resistance of the epitaxial material. This component is usually larger than one would expect because the current is confined by the device geometry.

Metal contact resistances, package lead resistances, and the resistance of the nonmetallized source silicon material are neglected in the on-resistance calculation.

Equivalent-Model Analyses — At low current levels, the accumulation layer beneath the gate, in effect, becomes a source for a depletion-mode vertical junction field-effect transistor (J-FET), and the neck becomes most of the J-FET channel. The body serves as the J-FET drain. As drain voltage is applied, the depletion channel and the depletion layer adjacent to the body both lengthen; at a sufficiently high voltage, this vertical J-FET may pinch off. The equivalent J-FET model, in essence, is the key to understanding the hexagonal power MOS/FET design. This cascode configuration clearly demonstrates that most of the drain voltage is supported by the J-FET. CAD programs are used to predict pinch-off voltages for the analyzed structure.

Further study of the cascode equivalent model reveals that the dominant factors in the determination of switching speed are gate drive current, gate-to-J-FET-source capacitance (Cx), and pinch-off voltage of the J-FET. All other capacitive effects are buffered by the cascode circuitry provided drain current is present. CAD techniques

```
OPTIMIZING PROGRAM FOR MOSFET
 VOLTS          =  165.  DIE MILS        =   120.  EDGE MILS      =   8.9  WIRE MILS        =  10.0
 PAD W.D        =  4.00  PAD H/D         =   2.00  SOURCE PADS =     1.00  METAL MICR       =  4.00
 P+ P-          =  1.50  N+/P-           =  0.250  UP/P-          = 0.375  SUB OHM-CM       = 0.150
 SUB MILS       = 12.00  RHO NECK/EPI    =  1.000  MOBILITY       =  400.  CHANNEL TYPE=        1.
 POLY HEX MIC   = 22.40  DIELECTRIC      =   4.00  GATE VOLTS     = 10.00  THRESHOLD V =      3.00
 CELL PITCH     = 36.30  P- DEPTH MIC    =   4.00  GATE ANGS      = 1000.
 ON RESISTANCE (OHMS x 0.001)     = 195.702  = 100.00%  P+ DEPTH            =    6.00
 WIRE RESISTANCE                  =   2.820  =   1.44%  N+ DEPTH            =    1.00
 SUBSTRATE RESISTANCE             =   6.485  =   3.31%  UP DIFFUSION        =    1.50
 METAL RESISTANCE                 =   2.355  =   1.19%  CHANNEL LENGTH      =    2.40
 DIFFUSED CHANNEL RESISTANCE      =  44.038  =  22.50%  0 VOLT DEPLETION    =    0.85
 0 VOLT DEPLETION CHANNEL         =  11.663  =   5.96%  EPI RESISTIVITY     =    2.59
 DISTRIBUTED NECK RESISTANCE      =  33.128  =  16.93%  NECK RESISTIVITY    =    2.59
 EPITAXIAL RESISTANCE             =  95.293  =  48.69%  EPI THICKNESS       =   17.21
 (LATERAL NECK RESISTANCE)        =  24.629             NUMBER OF CELLS     =   5001.
 (VERTICAL NECK RESISTANCE)       =  24.787             ACTIVE SQUARE CM    = 0.05528
 V PINCH (VOLTS)                  =    18.5             EDGE EFFICIENCY %   =    72.5
 CAP. G TO D(INT) PF              =  1101.9             PAD EFFICIENCY %    =    84.7
 SWITCH TIME (APPROX) AMP NSEC    =  20.410             POLY SQUARE CM      = 0.03423
                                                        POLY EDGE CM        =    38.8
```

Typical design chart for optimization of $r_{DS(on)}$. This chart represents one of many design possibilities. The top of the chart lists 23 input possibilities. The 13 parameters in the lower left column are expected electrical characteristics consistent with the inputs, and the 14 parameters in the lower right column are physical characteristics.

are used to optimize for the required capacitance-frequency relationships.

Excellent agreement exists between the parameters calculated from the computer model and measurements on finished devices.

Breakdown Voltage

Both low- and high-voltage designs have shields for the source field (to minimize the peak electric field in this region) and the drain field (to terminate the electric field within the n-type material). The high-voltage design includes a diffused guard ring that assures a more even distribution of the drain voltage and thereby reduces the peak electric field. The edges of the MOSFET structure are designed so that a uniform bulk breakdown occurs under the active area instead of at the edge. The power density at voltage breakdown is, therefore, reduced, and device reliability is improved.

Because the on resistance of a standard MOSFET must increase with increasing drain-source voltage capability, these devices are commonly used in applications up to 500 volts. The COMFET, in which the conductivity of the n-type expitaxial drain region is greatly increased (modulated) by the injection of minority carriers from the p-type substrate offers significant advantages in $r_{DS(on)}$ at higher voltage levels. However, a trade off is involved and the on resistance depends to some extent on other factors dictated by the intended application. However, even for the shortest switching times (100 nanoseconds), the on resistance value of 0.2 ohms is approximately a factor of ten less in the COMFET than in a comparably sized standard n-channel MOSFET.

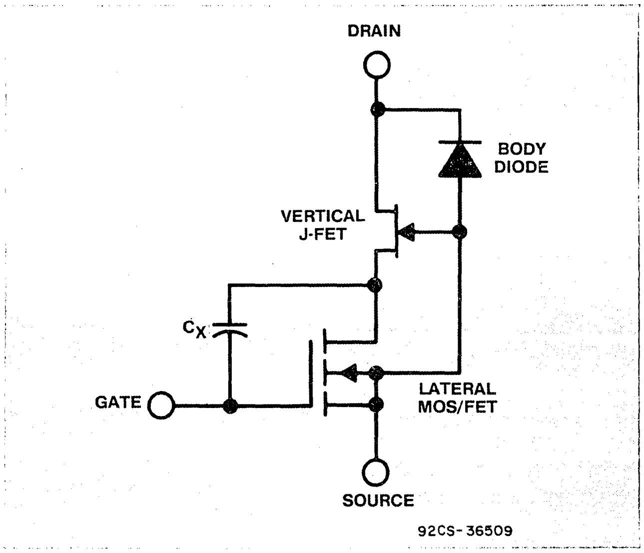
Gate Voltage

To permit the flow of drain-to-source current in an n-channel MOSFET, a positive voltage must be applied between the gate and source terminal. Since, as described above, the gate is electrically isolated from the body of the device, theoretically no current can flow from the driving source into the gate. In reality, however, a very small current, in the range of tens of nanoamperes, does flow, and is identified on data sheets as a leakage current, I_{GSS}. Because the gate current is so small, the input impedance of a MOSFET is extremely high (in the megohm range) and, in fact, is largely capacitive rather than resistive (because of the isolation of the gate terminal).

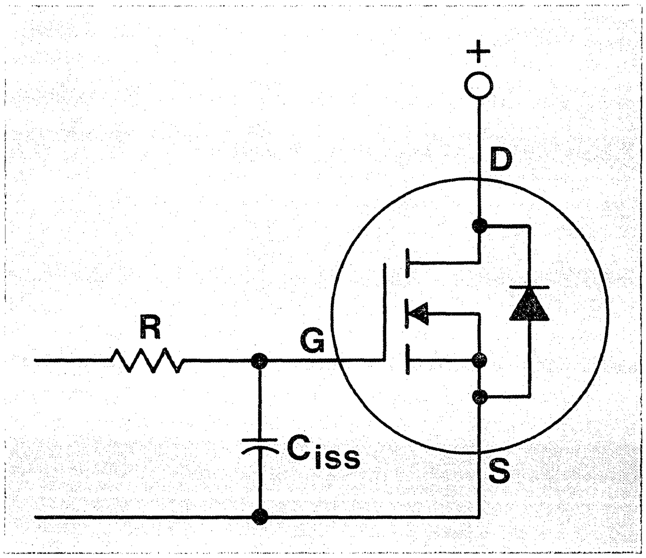
The basic input circuit of a MOSFET can be represented by an equivalent resistance and capacitance. The capacitance, called C_{iss} on MOSFET data sheets, is a combination of the device's internal gate-to-source and gate-to-drain capacitance. The resistance, R, represents the resistance of the material in the gate circuit. Together, the equivalent R and C of the input circuit determine the upper frequency limit of MOSFET operation.

Gate Threshold Voltage, $V_{gs}(th)$ — When considering the V_{gs} level required to operate a MOSFET, the device is not turned on (no drain current flows) unless V_{gs} is greater than a certain level (called the threshold voltage). In other words, the threshold voltage must be exceeded before an appreciable increase in drain current can be expected. Generally, V_{gs} for standard power MOSFETs is at least 2 volts. This is an important consideration when selecting devices or designing circuits to drive a MOSFET gate. The gate-drive circuit must provide at least the threshold-voltage level but, preferably, a much higher one.

The gate threshold voltage is determined on the basis of relative diffusion profiles of the source and the drain required for the body concentration that must be inverted. In addition, the diffusion from the points of the hexagon, the gate-oxide thickness, and the drain-neck resistivity must be optimized to assure a voltage threshold in the range of from 2 to 4 volts. For L^2FETs, this range is reduced from 1 to 2 volts.



Computer equivalent model of RCA power MOSFET consists of cascode connection of vertical J-FET and horizontal MOSFET.



Basic power MOSFET input circuit.

Design and Performance Characteristics

On-State Gate Voltage, $V_{gs}(on)$ — The halving of the gate-oxide thickness in the L^2FET, as compared with the standard 10-volt MOSFET and COMFET types, reduces the threshold voltage of the L^2FET by a factor of two over the other devices. Since the surface inversion of the MOS channel is determined by the gate insulator voltage field, the reduction of the gate insulator thickness from 100 nanometers to 50 nanometers in the L^2FET also halves the applied gate drive voltage required for the L^2FET to sustain the same drain characteristics as the standard 10-volt and COMFET devices.

Operating Frequency

Most DMOS processes develop the polysilicon gate structure rather than the older metal-gate type. If the resistance of the gate structure is high, the switching time of the DMOS device is increased, thereby reducing its upper operating frequency. Compared to a metal gate, a polysilicon gate has higher gate resistance. This property accounts for the frequent use of metal-gate MOSFETs in high-frequency (greater than 20 MHz) applications, and polysilicon-gate MOSFETs in higher-power but lower-frequency systems.

Since the frequency response of a MOSFET is controlled by the effective R and C of its gate terminal, a rough estimate can be made of the upper operating frequency from data-sheet parameters. The resistive portion depends on the sheet resistance of the polysilicon-gate overlay structure, a value of approximately 20 ohms per square. But whereas the total R value is not found on data sheets, the C value (C_{iss}) is; it is recorded as both a maximum value and in graphical form as a function of drain-to-source voltage. The value of C_{iss} is closely related to chip size; the larger the chip, the greather the value. Since the RC combination of the input circuit must be charged and discharged by the driving circuit, and since the capacitance dominates, larger chips will have slower switching times than smaller chips, and are, therefore, more useful in lower-frequency circuits. In general, the upper frequency limit of most power MOSFETs spans a fairly broad range, from 1 to 10 MHz.

Device Capacitances

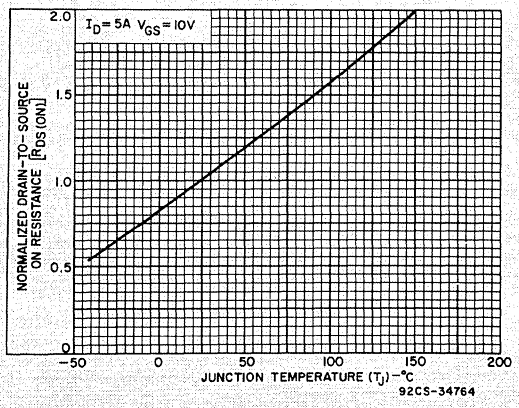
Power MOSFETs are majority-carrier devices and are, therefore, innately capable of high-speed switching. However, this switching capability is limited by the charging and discharging time of the gate-to-source capacitance C_{GS} and the gate-to-drain capacitance C_{GD}. In RCA power MOSFETs, the gate-to-source capacitance is reduced by minimizing the polysilicon area of the gate and by controlling the oxide dielectric under all gate- and source-pad runners. The resistance of the gate is minimized by close control of the doped polysilicon and by use of metallized gate runners.

Measurements of the switching speeds of the L^2FET devices indicate that the 50% reduction in gate oxide thickness, compared with standard MOSFETs and COMFETs, produces approximately a 2:1 increase in switching speed for any given value of gate-drive power.

Thermal Stability

The "hot-spotting" phenomenon, manifest in bipolar transistors by the localized high temperatures that can result from the tendency of current to concentrate in areas around the emitter, a phenomenon that can lead to device failure from the mechanism of thermal runaway, is not a factor in MOSFET operation because the current flow in these devices is in the form of majority carriers. The mobility of majority carriers is temperature dependent in silicon: mobility decreases with increasing temperature. This inverse relationship dictates that the carriers slow down as the chip gets hotter. In effect, the resistance of the silicon path is increased, which prevents the concentrations of current that lead to hot spots. In fact, if hot spots do attempt to form in a MOSFET, the local resistance increases and defocuses or spreads out the current, rerouting it to cooler portions of the chip.

Because of the character of its current flow, a MOSFET has a positive temperature coefficient of resistance. The positive temperature coefficient of resistance means that a MOSFET is inherently stable with temperature fluctuation, and provides its own protection against thermal runaway and second breakdown. Another benefit of this characteristic is that MOSFETs can be operated in parallel without the need for ballasting resistors and without fear that one device will rob current from the others. If any device begins to overheat, its resistance increases and its current is directed away to cooler chips.

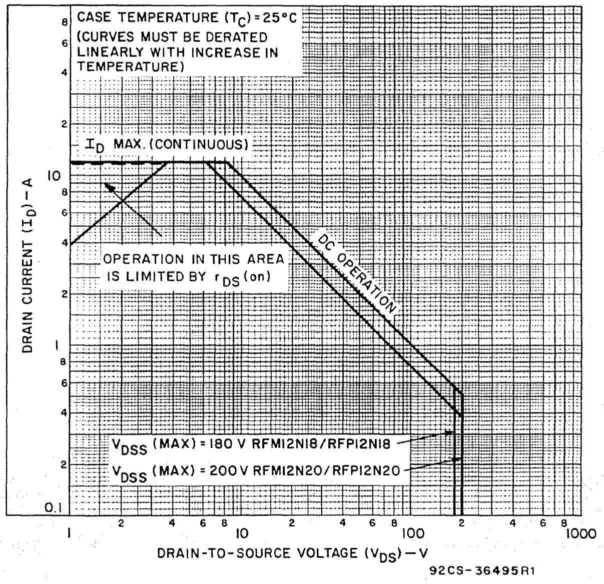


Normalized drain-to-source on resistance $r_{DS(on)}$ as a function of junction temperature.

The positive temperature coefficient of the MOSFET on resistance is a result of the proximity of the channel region to the gate. A bias on the gate can pull additional mobile charge carriers into the channel and, in this way, control the resistance and, in turn, the current in this region. However, carriers in this section are all of a single polarity, and the concentration of these carriers, which is primarily a function of the gate bias, is essentially independent of temperature. Therefore, the temperature coefficient of the on resistance is positive over the entire length of the current path, and the current always tends to defocus away from hot spots.

Safe Operating Area

The differences in the thermal characteristics of MOSFETs and bipolar transistors result in a fundamental difference in the safe-operating areas of these devices. Both types of device are limited only by thermal dissipation considerations when operated at high current and low voltage. In the high-voltage/low-current region of the safe-operating area, the positive-temperature-coefficient portion of the current path in bipolar transistors cannot counterbalance the negative-temperature-coefficient portion of the current path, which is higher in this region. Therefore, bipolar transistors must be derated more rapidly to avoid the high current concentration that may lead to second breakdown. In RCA power MOSFETs, the total current path has a positive temperature coefficient of resistivity, and the MOSFETs are rated for a constant thermal-dissipation limit over the entire area defined by the maximum current and voltage ratings.

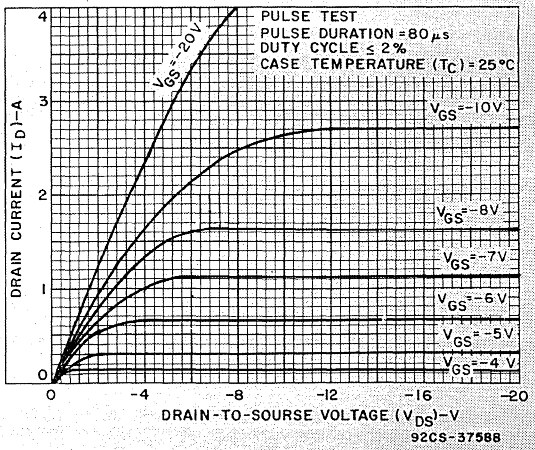


Safe-operating-area curve for an RCA power MOSFET.

Output Characteristics

Probably the most used MOSFET graphical data is the output characteristic or plot of drain-to-source voltage (V_{DS}) as a function of drain-to-source current (I_D). A typical characteristic shows the drain current, at various V_{DS} values, as a function of the gate-to-source voltage (V_{gs}). The curve is divided into two regions: a linear region in which V_{DS} is small and drain current increases linearly with drain voltage, and a saturated region in which increasing drain voltage has no effect on drain current (the device acts as a constant-current source). The current level at which the linear portion of the curve joins with the saturated portion is called the pinch-off region.

A standard power MOSFET must be driven by a fairly high voltage, on the order of 10 volts, to ensure maximum saturated drain-current flow. However, integrated circuits, such as TTL types, cannot deliver the necessary voltage level unless they are modified with external pull-up resistors. Even with a pull-up to 5 volts, a TTL driver cannot fully saturate most MOSFETs. Thus, TTL drivers are most suitable when the current to be switched is far less than the rated current of the MOSFET. CMOS ICs can run from supplies of 10 volts, and these devices are capable of driving a MOSFET into full saturation. On the other hand, a CMOS driver will not switch the MOSFET gate circuit as fast as a TTL driver. The best results, whether TTL or CMOS ICs provide the drive, are achieved when special buffering chips are inserted between the IC output and gate input to match the needs of the MOSFET gate. Of course, this limitation is eliminated with the use of the L^2FET.



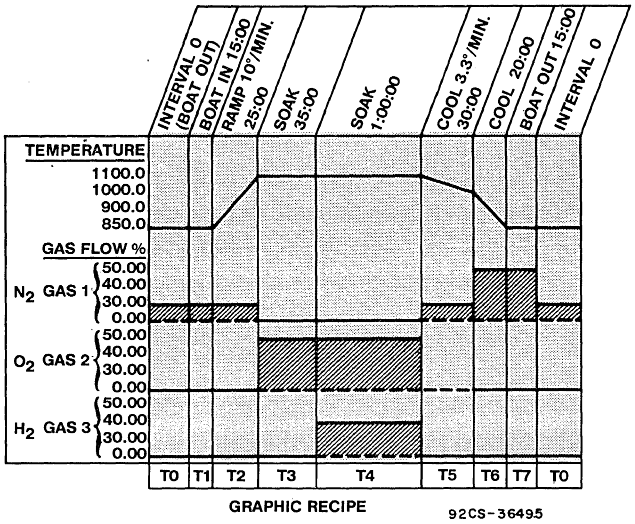
Typical output characteristic for an RCA power MOSFET.

Manufacturing Operations

The process technology and disciplines required to fabricate Power MOSFETs are very similar to LSI processing of integrated circuits. Current design rules accommodate 575,000 individual MOS cells per square inch of active die area. Projected design rules for 1984 will increase the density of active cells to 725,000 per square inch.

To manufacture Power MOS devices effectively, RCA has funded a multi-million dollar wafer fabrication facility specifically for MOS. Features of this facility include:

- 125-mm wafer capacity.
- Fully automated wafer transfer and handling.
- Microprocessor-controlled diffusion/LPCVD/metallization operation.
- Plasma etching of polysilicon and oxide films.
- Direct step on wafer-projection lithography.
- LPCVD polysilicon/doped oxides/undoped oxides.
- Ion implantation (low and high dose).
- Microprocessor-controlled photolithography operations.
- Computer-aided design and process simulation.
- Automated TO-220 and TO-3 Packaging.
- Automated pellet/finished-goods testing.



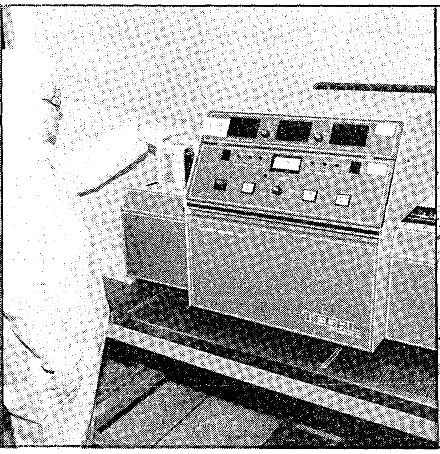
Micrographic recipe for a typical diffusion sequence.

Diffusion Operations

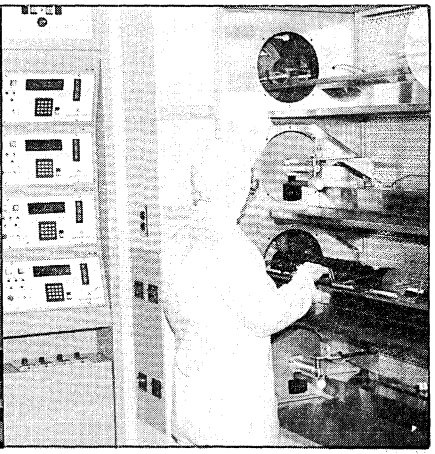
RCA power MOSFETs are processed in a Class 100 environment using state-of-the-art computer-controlled diffusion, LPCVD, and monitoring equipment. All diffusion and LPCVD tubes have a dedicated microcontroller specifically designed to control furnaces engaged in semiconductor wafer processing. The microcontrollers provide complete recipe creation and storage capabilities, constant monitoring of furnace conditions, automatic control of all furnace functions (time sequencing, temperature profiling/ramping, mass-flow controlled gases, and wafer-boat movements), alert/alarm provisions, and extensive diagnostic capabilities. The microcontrollers are supervised by a central computer console which provides additional recipe storage, inventory control, and centralized process monitoring.

Wafers are handled by first-generation robotics (cassette-to-cassette) at all stages of processing to eliminate human-handling induced defects. In addition, only the purest available gases, chemicals, and ultra filtered water are used to process RCA Power MOS/FETs. Ion implantation is used exclusively for all diffusion dopant sources to achieve exceptional uniformity and repeatability.

Ion-implantation system used for all diffusion operations.



System used for polysilicon plasma-etch operation.



Computer controlled system provides direct digital control of all furnace operations.

Lithography Operations

The Power MOSFET Lithography is performed in a temperature and humidity-controlled Class 100 environment using the most recent static-neutralizing equipment. Both coating and developing is performed on microprocessor controlled tracks. Each step is designed for cassette-to-cassette operation.

Mix and match exposure tools employ automatic laser alignment schemes throughout. Proximity machines are used for non-critical levels, while the registration and critical defect layers are printed by use of a 1.1 direct wafer stepper.

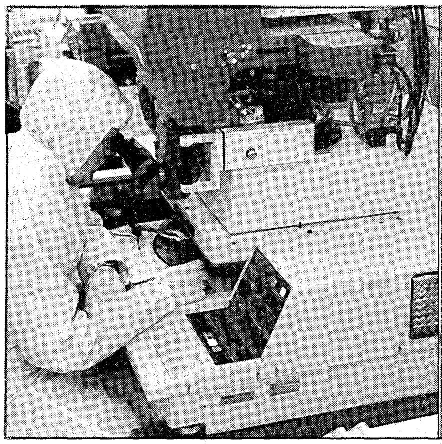
A metal ion-free developer is used exclusively to guard against any trace impurities. Inspection and critical dimension control are handled in a cassette-to-cassette manner by the successful marriage of the Nanometrics line-width computer with the OSI inspection station incorporating automatic laser focusing.

A high temperature positive resist is used on all product to assure line-width fidelity through high-current ion implantation. Plasma etching is used for pattern delineation using the single-wafer approach with end-point detection.

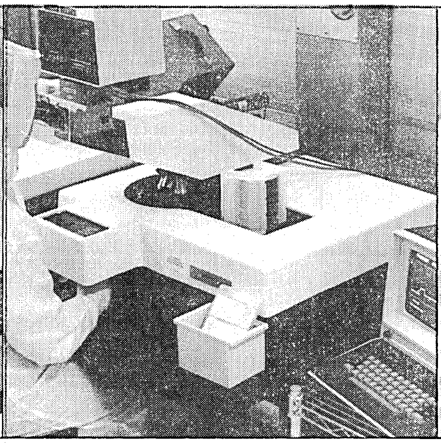
Assembly

Automation is being introduced improve product quality and reliability.

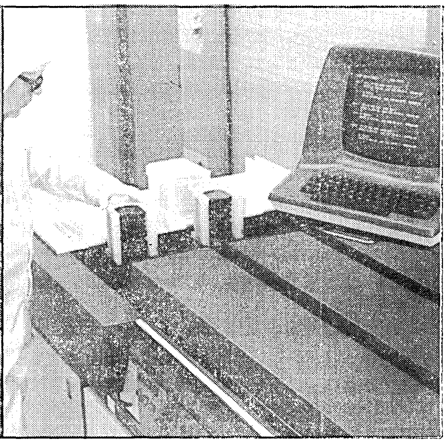
Automatic equipment has been installed to assemble the TO-220; additional equipment currently being installed will fully automate assembly of TO-3 devices. Both of these assembly lines utilize the latest state-of-the-art techniques, such as pattern recognition systems, to identify "good" pellets for automatic transfer from a sawed wafer array and also to identify and locate the bond pads for automatic placement of the interconnect bond wires. Wire bond integrity is determined automatically be resonant frequency values



Direct wafer stepper (1X) used for critical lithography alignment.

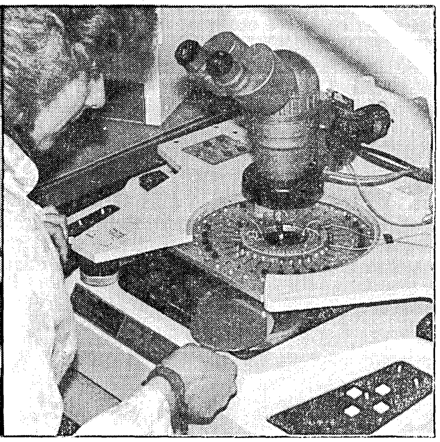


OSI inspection system provides resolution to nanoline widths.



Microprocessor-controlled macronetic coating track.

Microprocessor-controlled automatic wafer dicing system.



Wafer circuit probe test station.

registered after each ultrasonic bond. Oxygen level sensors and moisture monitors are used at the sealing operation for TO-3 devices to guarantee the proper environment to assure reliable hermetic product. In addition, the latest state-of-the-art electronic tests have been instituted for all dc static tests, hot switching, inductive testing, Is/b and other tests required to assure that product does indeed meet specifications.

TO-3 Assembly System

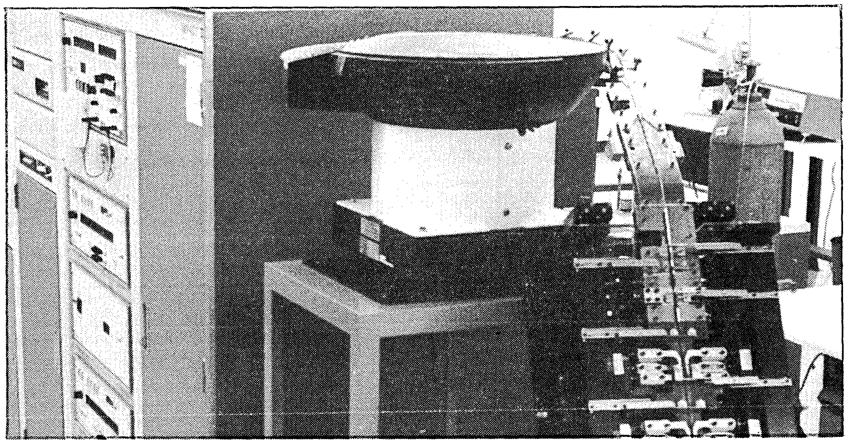
The TO-3 manufacturing system is fully automatic from wafer sawing through brand and pack operations. This system is designed to eliminate all handling of product by the operator. It reduces cycle time, improves reliability levels, and is potentially capable of a 30 parts-per-million quality level.

System operation begins with the feeding of TO-3 stems from vibratory bowls into an automatic chip-mounting machine. Stems with chips mounted are then output to a storage cart. The storage cart provides the input to the automatic aluminum-wire bond machine, which ultrasonically bonds the wires to the chip and leads on the TO-3 stems. After wire bonding, the product is auto-loaded into the storage carts, which are then loaded into the automatic sealing machine. This machine processes the product through a one-hour bake prior to weld sealing. Sealing is done in a nitrogen atmosphere to assure device hermeticity; the product then moves again to a storage cart. The sealed product is next loaded into a machine that automatically coats the TO-3 leads with solder and then loads the product back into the storage cart for transportation to the test handlers. At the test-handler station, the devices are automatically dispensed into one of twenty bins according to test specifications, and then stored in an automatic storage and retrieval system. A robot stores the product automatically and keeps track of it through a bar code system that identifies each test bin. The bins are stored at random locations by the robot and retrieved when needed to satisfy an order from a customer. When retrieved, a bin is brought to a brand and pack machine where the bin bar code is verified by a code reader. If the bar code is correct, the product is fed from a vibratory feed bowl into the machine where it is tested again to assure compliance to tests specifications, branded, and packed for shipment to the customer.

Quality audits are taken on-line after each operation to assure the quality level of the product. Checks for voids under the pellet, bonded wire pull strengths, hermeticity after sealing, solder coverage of leads, correlation of test specifications at testing, and the final test at branding to guarantee the integrity of the device to the customer are all monitored on a scheduled basis throughout the production process.

Testing

All MOSFET testing is done on a Lorlin Impact II Test System, which can handle up to 100 amperes forward current and 2,000 volts reverse voltage. Stations are provided for both wafer probe and finished-goods testing. All finished devices in TO-220 and TO-3 packages are automatically handled and tested to assure the highest possible quality levels at the final-test operation. The wafer prober is attached to a wafer mapper so that device parameters can be mapped to determine variation across the wafer. This data can then be compared with the statistical information that is generated. Given the proper command, statistical tables and histograms are printed out.



Automatic TO-3 and TO-220 power MOSFET test set.

Quality and Reliability Assurance

The ability to build and maintain the high levels of quality and reliability required today, depends on inherent design and process capability, and not the degree of test and inspection. Both the design and production facilities for RCA's Power MOSFET are totally new, with state-of-the-art equipment and process techniques which deliver this needed capability.

In-Process Quality Control

All critical phases of the highly automated power MOSFET manufacturing cycle have been characterized with respect to their intrinsic variability. Statistical limits have been established to give early warning of abnormal process trends and fluctuations, based on this intrinsic capability. These limits are constantly tightened as the process improves and are well within the engineering specifications. The emphasis at RCA is to employ statistical methods at the point of control, rather than an inspection point at the end of a process.

Control of Outgoing Product

The quality control lot acceptance sampling of finished product is performed after manufacturing has performed 100% inspection of all specified electrical characteristics. The current sampling level is 0.1% AQL for electrical parameters, and is constantly being improved. However, due to tight parameter distributions gained through process control and inherent design capability, the average outgoing quality level (AOQ) to the customer has been in the order of 100 PPM (0.01%).

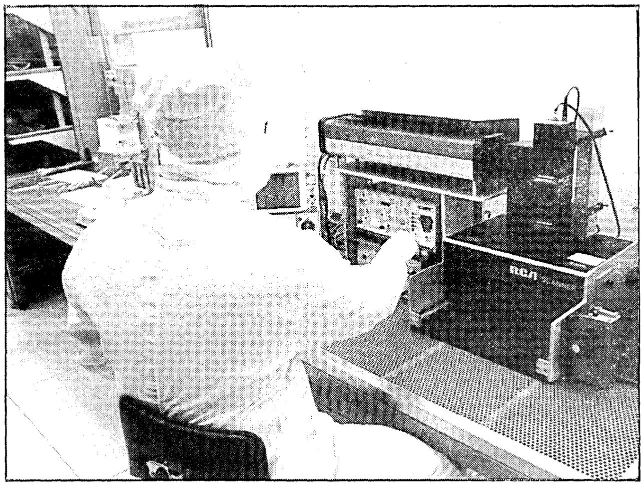
Reliability Assurance

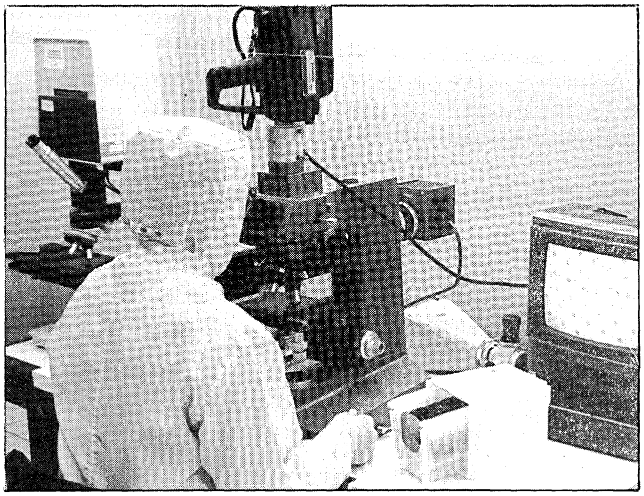
RCA Solid State has a world-wide reliability program that helps to shape the direction of new product development, assures that the reliability level is maintained throughout the production cycle, and develops specific models to predict the reliability in the end-use application. In order to meet these objectives, a reliability facility is maintained at each manufacturing location for real-time feedback. A centralized reliability engineering organization develops all new test methods and supports new product/process development. Each group is fully trained in the reliability and applied statistics disciplines, as well as failure analysis, and are responsible for using these techniques to monitor and improve product capability.

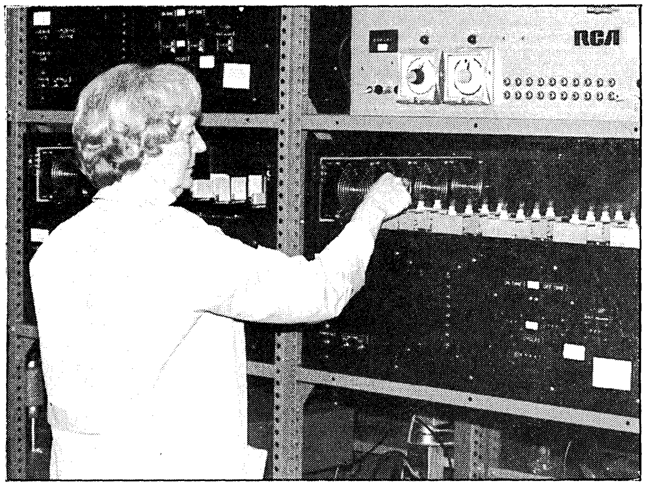
The Reliability program

The reliability-assurance program operates at all stages of production, using the following four-pronged approach:

Product Design and Development — During early development, initial product lots are characterized through accelerated reliability tests which establish the product capability. Once the design has been fine-tuned,


Laser scanner used to detect processing defects.


Electronic microscope with TV monitor used for visual inspection of wafers.


Thermal-fatigue and operating-life test racks.

multiple production runs are initiated and samples are subjected to a full range of standardized accelerated tests. All lots must meet pre-established reliability standards before any new design or process can be released for production.

Wafer HTRB — RCA has developed a totally unique in-line reliability test performed at the wafer level. Samples from each wafer lot receive a 24-hour 150°C bias-life test to measure passivation integrity and surface cleanliness.

Real Time Indicators (RTI) — RTI's are short-duration accelerated-stress tests used to control the occurrence of specific failure mechanisms that can significantly affect product reliability. The stress levels are designed to induce failures, so that product-capability shifts can be detected and corrected. They are performed weekly at each manufacturing location. In this real-time method of determining reliability, a continuous flow of data is provided to indicate how well the manufacturing process is producing product.

Table I — Typical MOSFET RTI Tests

TEST	CONDITIONS	PACKAGE	TYPICAL DURATION
Power Cycling	PD = 4.75 Watts Tj = 35°-175°C (approx.)	Plastic	10-15K cycles
Power Cycling	PD = 56 Watts Tj = 90°-168°C (approx.)	TO-3	20-50K cycles
D-S Bias Life	TA = 150°C 80% of Drain-Source	All	168 hrs.
G-S Bias Life	G - S = 16 V, TA = 150°C	All	168 hrs.

Requalification Program (RQP) — Each product is requalified every six to twelve months to the same matrix of tests required for the initial production release. This operation measures the changes in the total capability of each MOS/FET family to meet the original reliability design objectives. Table II is typical of the data generated for RQP.

Table II — Accelerated Power MOSFET Test Reliability Summary

PACKAGE	TEST AND CONDITIONS	DURATION	CUM. HOURS OR CYCLES	% NON-FUNCTIONAL
All	Bias Life Drain-Source = 80% of rated TA = 150°C	500 hrs.	300,000	0.33
All	Bias Life Gate-Source = 16V, TA = 150°C	500 hrs.	270,000	0.00
All	Operating Life TA = 150°C, Free Air	500 hrs.	230,000	0.00
TO-31 TO-39	Thermal Cycling -65°C to +150°C	400 cycles	133,600	0.30
TO-220	Thermal Shock -65°C to +150°C	400 cycles	100,000	0.00
TO-31 TO-39	Power Cycling Delta Tj = 78°C PD = 56 W (TO-3) or 2 W (TO-39)	20,000 cycles	5,480K	0.73
TO-220	Power Cycling Delta Tj = 135°C, PD = 4.75 W	10,000 cycles	1,850K	0.00
TO-220	Pressure Cooker	24 hrs.	3,072	0.00

Failure Rate in %/1000 Hours at 60% UCL

TEST	TA = 125°C	TA = 90°C	TA = 75°C
Bias Life	0.09	0.005	0.001
Operating Life	0.07	0.004	0.001

NOTE: Failure rate based on Nonfunctional performance in an operating mode, extrapolated from 150°C data using 1.0 eV activation energy.

Explanation of Ratings and Characteristics

RCA power MOSFETs operate with very high efficiencies and modest drive requirements at switching frequencies up to several hundred kilohertz. At the lower frequencies, they can be driven directly from the signal levels of CMOS and other logic integrated circuits.

Switching losses in power MOSFETs are independent of temperature, and a major contributor to thermal runaway is thereby eliminated. The on-resistance in power MOSFETs has a positive temperature coefficient so that localized "hot spots" are defocused; the devices, therefore, can be readily operated in parallel without the need for costly compensating and balancing techniques.

The published data on RCA power MOSFETs fully characterize these devices with respect to the maximum stresses that they can safely withstand and the performance levels they are expected to achieve.

Maximum Ratings

Maximum ratings define the extreme limits of the electrical, mechanical, and environmental stresses that the devices are rated to withstand. These limits should not be exceeded under any operating condition of the devices; otherwise, reliable operation cannot be assured and irreversible damage to the devices is possible. Worst-case system design conditions should assure that the devices are operated within these limits.

Electrical Characteristics

Characteristics data for RCA power MOSFETs are based on the determination of the inherent qualities and traits of the device. These data, which are usually obtained by direct measurements, provide information that a circuit designer needs to predict the performance capabilities of his circuit and form the basis for the ratings that define the safe operating limits of the device.

Maximum Ratings

Drain-Source Voltage, V_{DS}	The maximum voltage that may be applied from drain to source.
Drain-Gate Voltage, V_{DG}	The maximum voltage that may be applied from drain to gate.
Gate-Source Voltage, V_{GS}	Standard RCA power MOSFETs have a maximum gate-to-source voltage rating of ±20 volts. Under some circumstances a higher voltage can be supported. In general, however, if this rating is exceeded, even momentarily, irreversible degradation of device performance may result.
Drain Current, RMS Continuous, I_D	The maximum rating for the total effective, or rms, drain current also includes the contribution of the body-drain diode. This current is limited by the maximum allowable power dissipation P_T, the on-state resistance $r_{DS(on)}$, and the size of the bond wire.
Drain Current, Pulsed, I_{DM}	The pulsed drain-current rating defines the maximum allowable limit for any transient peak current value in either direction.
Total Device Power Dissipation, P_T	The total dissipation rating is established to assure that the maximum allowable junction temperature T_J (max) is not exceeded. The dissipation limit is specified at 25°C so that $T_J(\text{max}) = T_C + P_T R\theta_{JC}$ At case temperature T_C above 25°C, the dissipation limit value must be derated linearly.
Operating and Storage Temperature, T_J, T_{stg}	All RCA power MOSFETs are rated for a maximum junction temperature of 150°C. Operating conditions which assure that the junction temperature is maintained below the maximum rating will contribute to long-term operating life.

Explanation of Ratings and Characteristics

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C)=25° C

Drain-Source Breakdown Voltage, BV_{DSS}	The min. limit indicates the max. voltage which may be applied drain-to source.
Gate-Threshold Voltage, $V_{GS(th)}$	The gate voltage that must be applied to initiate conduction.
Zero-Gate-Voltage Drain Current, I_{DSS}	Specified at 80% of rated V_{DSS}. Specified at 25° C and 125° C. Gate terminated to source.
Gate-Source Leakage Current, I_{GSS}	Specified as an absolute value at max. rated V_{GSS}, plus or minus polarity.
On-State Gate Voltage, $V_{GS(on)}$	Max. gate voltage required to support specified I_{DS} (analogous to max. I_B, i.e., min. h_{FE}, for bipolar devices).
Static Drain-Source On Resistance, $r_{DS(on)}$	Specified at ½ max. rated I_D and with V_{GS} at 10 V (for TO-39 packaged devices, $r_{DS(on)}$ is specified at max. rated I_D). Positive temperature coefficient promotes current sharing when devices are paralleled.
Forward Transconductance, g_{fs}	Equal to the slope of the transfer characteristic $g_{fs} = \Delta I_d/\Delta V_{gs}$, with V_{DS} constant. Analogous to h_{fe} for a bipolar device.
Input Capacitance, C_{iss}	The capacitance between the input terminals (gate and source) with the drain short-circuited to the source for alternating current.
Output Capacitance, C_{oss}	The capacitance between the output terminals (drain and source) with the gate short-circuited to the source for alternating current.
Reverse-Transfer Capacitance, C_{rss}	The capacitance between the drain and gate terminals with the source connected to the guard terminal of a three-terminal bridge.
Turn-On Delay Time, $t_{d(on)}$	The time interval during which an input pulse that is switching the transistor from a nonconducting to a conducting state rises from 10% of its peak amplitude and the drain current waveform rises to 10% of its on-state amplitude, ignoring spikes that are not charge-carrier induced.
Rise Time, t_r	The time interval during which the drain current changes from 10% to 90% of its peak on-state value, ignoring spikes that are not charge-carrier induced.
Turn-Off Delay Time, $t_{d(off)}$	The time interval during which an input pulse that is switching the transistor from a conducting to a nonconducting state falls from 90% of its peak amplitude and the drain current waveform falls to 90% of its on-state amplitude, ignoring spikes that are not charge-carrier induced.
Fall Time, t_r	The time interval during which the drain current changes from 90% to 10% of its peak on-state value, ignoring spikes that are not charge-carrier induced.
Thermal Resistance, Junction-to-Case, $R_{\theta JC}$	The thermal resistance (steady state) from the semiconductor junction(s) to a stated location on the case.
Source-Drain Diode	An integral p-n junction diode whose anode and cathode are common with the MOSFET source and drain terminals respectively.
Forward-Voltage Drop, V_F	The voltage developed across the p-n junct diode due to the forward current flow.
Reverse Recovery Time, t_{rr}	The time required to allow dissipation of the excess charge that accumulates due to the forward conduction of the p-n diode.

Switching Characteristic's

A Power MOSFET is usually considered as a gate-voltage controlled device. In reality, an appreciable current must be provided in order to switch the device. In measurements of the switching characteristics of RCA power MOSFETs, the gate current is used as the input parameter.

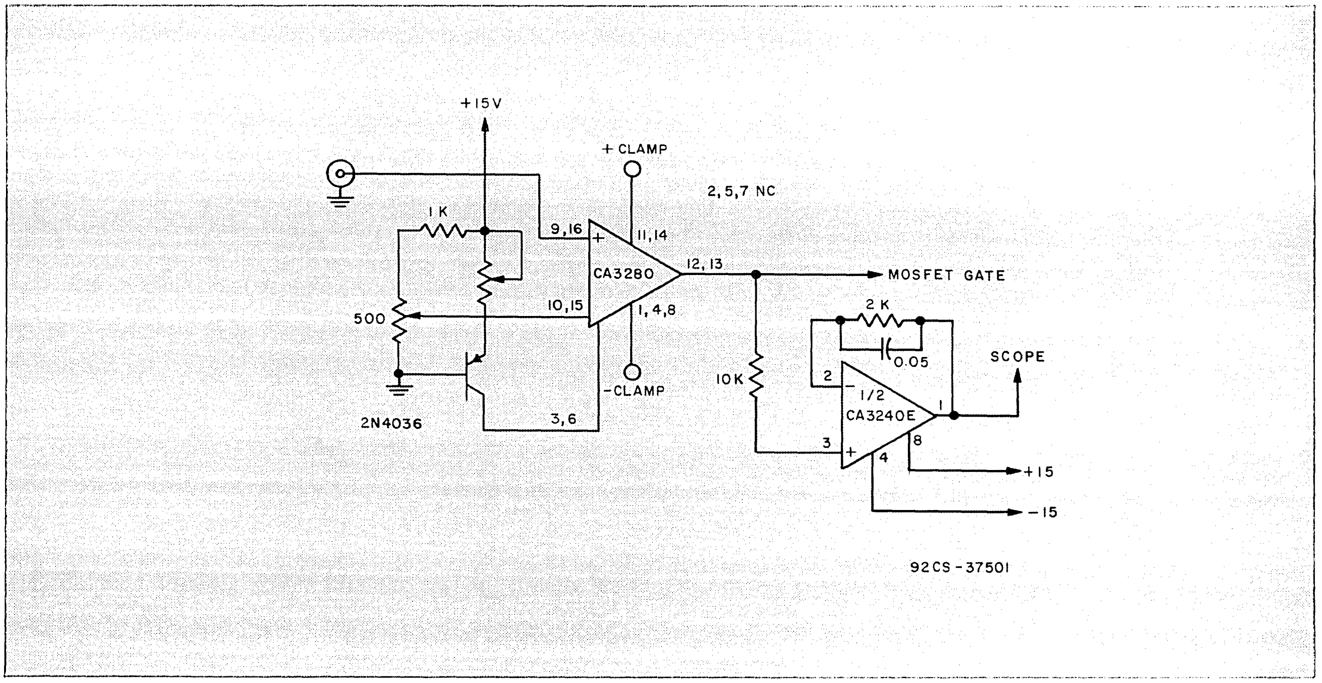
A family of curves is presented for a constant load resistance with V_{DD} varied. Gate drive during switching transitions is a constant current with voltage compliance limits of 0 and 10 volts (0 and 5 volts for L^{2}FETs). This new format is a plot of drain voltage and gate voltage as a function of normalized time. Time is normalized by the value of gate driving current. The normalization shows excellent agreement with data over five orders of magnitude, and is bounded on one extreme by gate propagation effects and on the other by transition time self-heating (typically tens of nanoseconds to hundreds of microseconds).

Test Circuit — The heart of the switching-time test circuit is an RCA CA3280 integrated-circuit operational transconductance amplifier (OTA) operated as a comparator. An OTA is a current output circuit where the output current and output transconductance are programmed by the amplifier bias current (I_{ABC}). Internal chip circuit feedback assures an extremely high output impedance within a compliance range established by the supply voltages. The CA3280 is actually two OTA's in parallel.

A value of I_{ABC} is established from the collector of a 2N4036 transistor. The current into the load (the gate of the MOSFET under test) may be varied between $+ I_{ABC}$ and $-I_{ABC}$ times a constant of proportionality (approx. a0.9). The actual value depends upon the input differential input voltage. As a comparator, the differential voltage is large, resulting in saturated behavior of $\pm I_{ABC}$. If the gate voltage comes within a volt of the rail voltages, this current goes to zero, producing a clamping voltage. These supply voltages are adjusted to clamp 0 volts and +10 volts for the normal n-channel MOSFET (0 volts and +5 volts for L^{2}FETs). The behavior of the CA3280 IC is excellent from submicroamperes to about 2-1/2 ma. Higher current may be achieved by stacking many CA3280 packages atop one another and soldering the leads to parallel the chips rather than wiring many sockets. This arrangement may require an increase in the bypass capacitor values.

An RCA CA3240E BiMOS input op amp is used as a unity-gain follower. Otherwise, the 1-megohm or 10-megohm shunting impedance of the scope would load the high-impedance circuitry associated with the MOSFET gate.

Test Conditions and Waveforms — The input test signal applied to the CA3280 OTA is supplied by a pulse generator set for an on-time duration of 50 μs and a repetition rate of approximately 25-ms (about 0.2% duty cycle). The ± clamp voltages are set to the appropriate values. The power MOSFET load resistor is chosen to equal the maximum rated voltage divided by the maximum rated current.



Test circuit used to measure switching characteristics of RCA power MOSFETs.

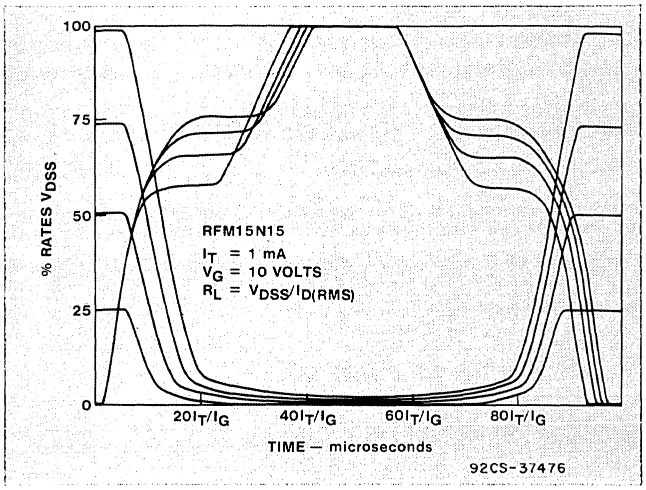
With a low value of drain supply voltages, the gate voltage is observed while adjusting I_{ABC}. A convenient set of conditions occurs when a short dwell time of several microseconds exists at the + 10-volt level (+ 5-volt level for L^2FETs). Minor adjustments may be desired for I_{ABC} as the drain supply voltage is increased to the maximum rate value.

There are some features of the gate and drain voltage waveforms which should be noted.

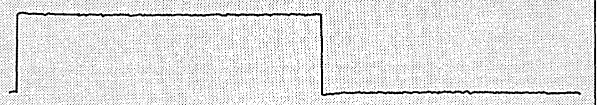
1. The waveforms during the positive gate current time are symmetrical to those during the negative gate current time.

   Exceptions occur for very fast or very slow switching, and for non-symmetrical current drive.
2. The drain voltage waveform contains a rather steep slope with a fairly constant dv/dt over most of the drain voltage excursion.
3. The drain voltage contains a rather shallow slope with a fairly constant dv/dt over the remainder of the drain voltage excursion.
4. The drain transition voltage (defined as the intercept of the gate and drain voltage curves above two near straight lines) typically occurs when the drain voltage equals the sum of the gate voltage (at that instant of time) plus the product of the drain current times $r_{DS(on)}$.
5. The gate voltage waveform contains three near straight line segments during the positive gate current transition time.

Family of Characterization Curves — The published switching data on RCA power MOSFETs include a family of gate and drain voltage curves in which the drain supply voltage is fixed at four values. The ordinate is 10 volts (5 volts for L^2FETs) full scale for the gate voltage and is normalized to 100% of the maximum rated drain-voltage curves. All four sets of

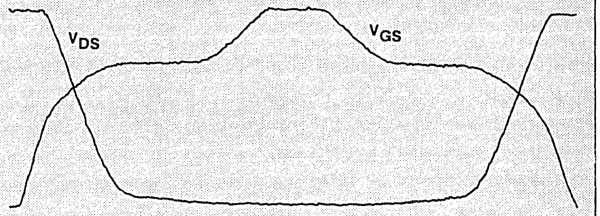


Family of switching-characterization curves for an RCA power MOSFET.

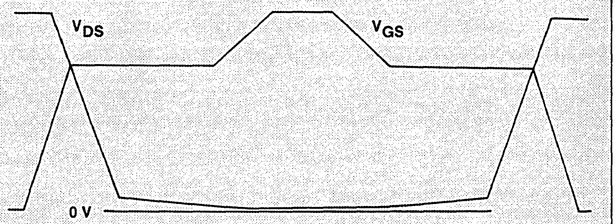


Input test signal applied to CA3280 (2 volts peak).

Power MOSFET gate-current waveform (±1 mA).



Power MOSFET gate voltage (10 volts peak) and drain voltage (150 volts peak-to-peak) waveforms.



Linear approximation of power MOSFET gate- and drain-voltage waveforms.

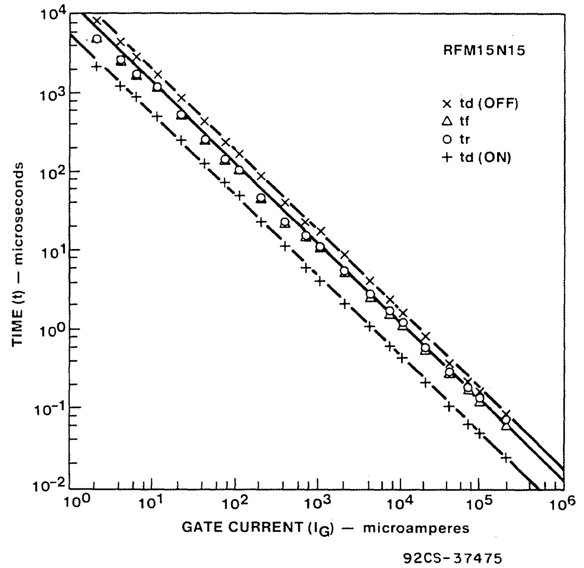
Test waveforms for measurement of switching characteristics of standard power MOSFETs. (Time base for waveforms is 100 microseconds full scale.)

curves are taken with a predetermined gate current, $\pm I_T$. The abscissa is also normalized to 100 (I_T/I_G) microseconds full scale, where I_G is the actual gate drive current. With this family of characteristic curves, switching behavior may be readily predicted for almost any driving circuit provided the load is resistive.

Characterization-Curve Limits — The gate and drain voltage switching waveforms can be scaled in an inverse manner with gate current. This scaling shows that the switching-time range over which the characterization can be applied is very impressive. For gate currents of the order of amperes, the device response will be slowed by gate propagation delay. This delay, of course, degrades the linear switching relationship to gate current. The characterization, however, is valid over many decades of gate current so that all but a very few applications can be described by the family of switching characterization curves.

Asymmetrical Current Drive — The positive and negative gate drive will often be dissimilar. The scaling of course must reflect this condition. At other times, the gate current varies with amplitude. This is always true when driving from a pulse generator of fixed resistance. Piece-wise linear methods will yield the gate current, which will permit the proper piece-wise linear scaling. This could be done in the following manner:

1. Mark eleven small x's along the gate waveform, dividing it into 10 equal voltage segments; for example, $V_S = 0, 1, 2, \ldots 9, 10$ volts.
2. Draw a vertical line through each X the full height of the gate waveform, creating 10 time segments.
3. If the driving-pulse amplitude is 0 to 10 volts with an internal resistance of 100 ohms, the piece-wise linear gate current for each time segment can be calculated, $I_{g1} = (10\text{-}0.5)/100 = 95$ mA, $I_{g2} = (10\text{-}1.5)/100 = 85$ mA, etc.
4. Then each waveform is scaled within the pertinent time segment by the proper gate current.
5. Smooth the curves.
6. Create 10 more time segments for the right half of the gate waveform corresponding to an average gate voltage of 9.5, 8.5, . . . 1.5, 0.5 volts. Call these segments 11, 12, . . . 19, 20.



Linearly, sealed correlation curves show that switching characterization curves are valid over five decades of gate current.

7. In that the pulse-generator voltage is now zero volts, calculate I_g as:
   $I_g11 = (0\text{-}9.5)/100 = -95$ mA, $I_{g12} = (0\text{-}8.5)/100 = -85$ mA, etc.
8. Repeat 4 and 5. L^2FETs would be treated with smaller voltage segments.

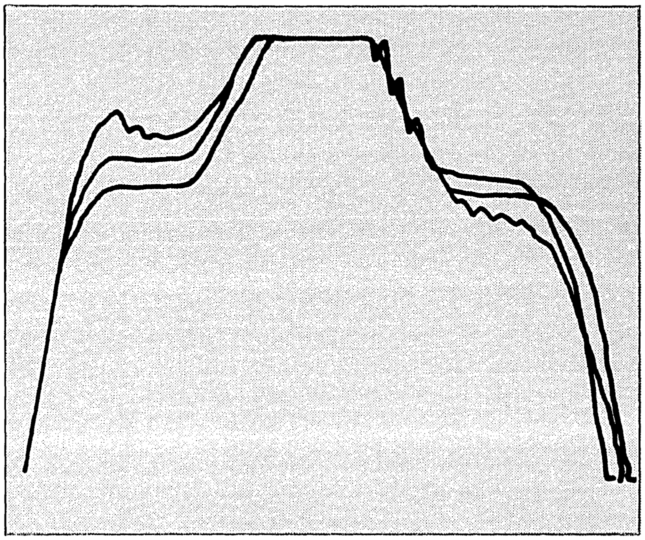
Generally, the gate-voltage plateau will not be located at the middle of the pulse-generator amplitude (5 volts). As a result, rise and fall times measured this way experience differing gate currents and are "non-symmetrical". This type of measurement will also lead one to observe temperature sensitivities, load-current sensitivities, and device-to-device variability, all of which are more circuit dependent than device dependent.

Explanation of Ratings and Characteristics

Gate-Voltage Propagation Effects — Most power-MOSFET applications need switch no faster than tenths of a microsecond. Should faster switching be required, it must be understood that the power MOSFET appears as a distributed network of many cells when used for very fast switching.

The thousands of individual MOSFET cells are connected in parallel with highly conductive metal for the sources and drains. However, the gates are paralleled with a moderately conductive film of doped polysilicon. As a result, a very steep voltage wavefront applied to the gate pad will bias those cells close by, but a delay will occur for turn on or turn off. Because of the nonlinear "input capacitance" of each call, the delay cannot be characterized by a pure number of so many nanoseconds.

At present, most manufacturers characterize typical switching speed for a single test condition. The test conditions are usually chosen to present the most favorable result. Therefore, this is usually near the upper limit of usefulness.



Curves show the increasing effect of gate-voltage propagation.

Handling Precautions for MOSFETs

Insulated-Gate Field-Effect Transistors (MOSFETs) are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling a MOSFET, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applications, with virtually no damage problems due to electrostatic discharge.

MOSFETs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive materials such as "ECCOSORB* LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hands being used should be grounded by any suitable means — for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. Gate Voltage Rating — Never exceed the gate-voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.
6. Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.
7. Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. If gate protection is required an external zener is recommended.

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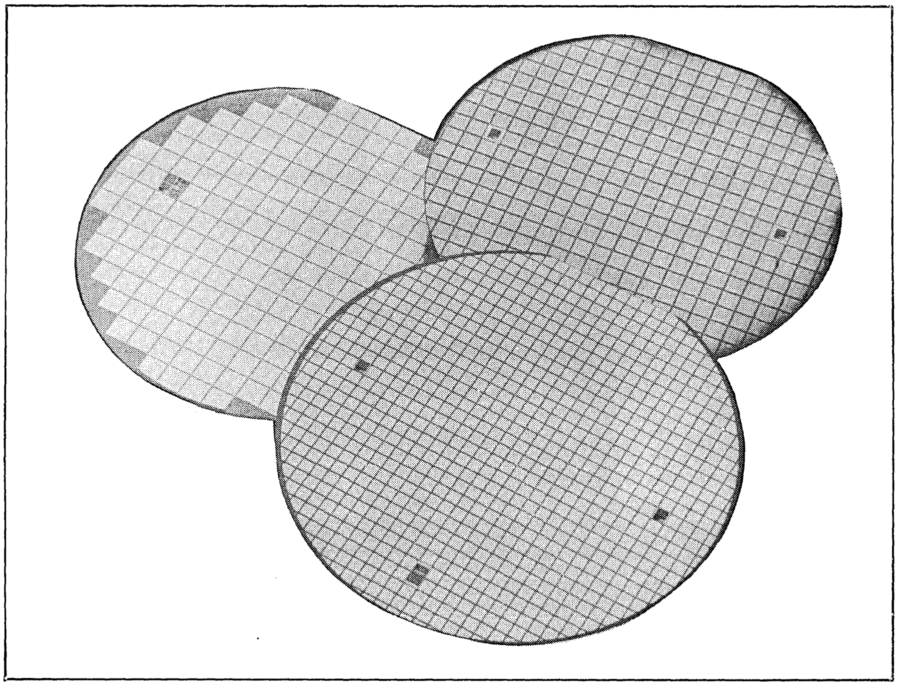
*Trademark Emerson and Cumming, Inc.

Standard Power MOSFETs

This section provides detailed technical data on the RCA conventional 10-volt power MOSFETs currently available as standard product. Key features, recommended applications, maximum ratings, limit values for critical electrical characteristics, and characteristic curves are shown for each type. The technical data for specific types are presented in ascending order of the drain-current ratings.

A useful feature of the MOSFET fabrication process is, as mentioned above, the internal diode formed between source and drain. In n-channel MOSFETs, this internal drain-to-source diode conducts when the source is positive with respect to the drain. The diode can handle forward current equal to the drain-current rating, has a reverse blocking-voltage capability that matches the drain-to-source breakdown rating, and exhibits fast turn-off switching. These features make the internal diode especially useful as the clamp diode in inductive-load switching circuits.



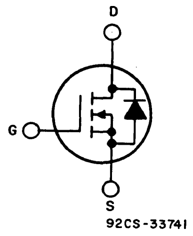
Power MOSFET wafers for chip sizes of 6, 4.5, and 3 square millimeters.

N-Channel Enhancement-Mode Power Field-Effect Transistors

1 and 2 A, 80 and 100 V

$r_{DS(on)}$: 1.25Ω and 1.4Ω

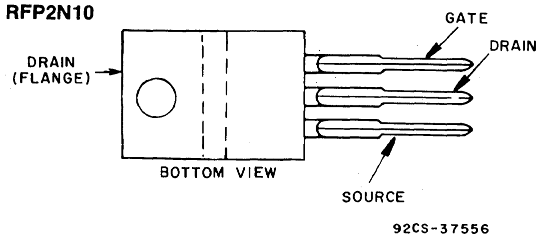
Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

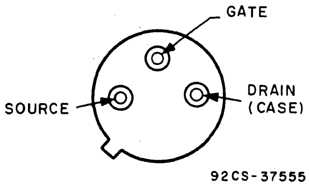
RFP2N08
RFP2N10

TERMINAL DESIGNATIONS



JEDEC TO-220AB

RFL1N08
RFL1N10



JEDEC TO-39

The RFL1N08 and RFL1N10 and the RFP2N08 and RFP2N10 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-39 metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFL and RFP series were formerly RCA developmental numbers TA9282 and TA9283, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFL1N08	**RFL1N10**	**RFP2N08**	**RFP2N10**	
DRAIN-SOURCE VOLTAGE	V_{DSS}	80	100	80	100	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)	V_{DGR}	80	100	80	100	V
GATE-SOURCE VOLTAGE	V_{GS}	±20				V
DRAIN CURRENT RMS Continuous	I_D	1	1	2	2	A
Pulsed	I_{DM}	5				A
POWER DISSIPATION @ T_C=25° C	P_T	8.33	8.33	25	25	W
Derate above T_C=25° C		0.0667	0.0667	0.2	0.2	W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150				° C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL1N08 RFP2N08		RFL1N10 RFP2N10		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	100	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V	—	1	—	—	μA
		V_{DS}=80 V	—	—	—	1	
		T_C=125° C					
		V_{DS}=65 V	—	50	—	—	
		V_{DS}=80 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)^a$	I_D=1 A V_{GS}=10 V	—	1.25	—	1.25	V
		I_D=2 A V_{GS}=10 V	—	3	—	3	
Static Drain-Source On Resistance	$r_{DS}(on)^a$	I_D=1 A RFP	—	1.25	—	1.25	Ω
		V_{GS}=10 V RFL	—	1.4	—	1.4	
Forward Transconductance	g_{fs}^a	V_{DS}=10 V I_D=1 A	400	—	400	—	mmho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	150	—	150	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	80	—	80	
Reverse-Transfer Capacitance	C_{rss}	f = 0.1 MHz	—	20	—	20	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V	17(Typ)	25	17(Typ)	25	ns
Rise Time	t_r	I_D=1 A	30(Typ)	45	30(Typ)	45	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	30(Typ)	45	30(Typ)	45	
Fall Time	t_f	V_{GS}=10 V	17(Typ)	25	17(Typ)	25	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFL1N08, RFL1N10	—	15	—	15	°C/W
		RFP2N08, RFP2N10	—	5	—	5	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL1N08 RFP2N08		RFL1N10 RFP2N10		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}^a	I_{SD} = 1A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 2A d_{IF}/d_t = 50A/μs	100(typ.)		100(typ.)		ns

[a] Pulsed: Pulse duration=300 μs max., duty cycle=2%.

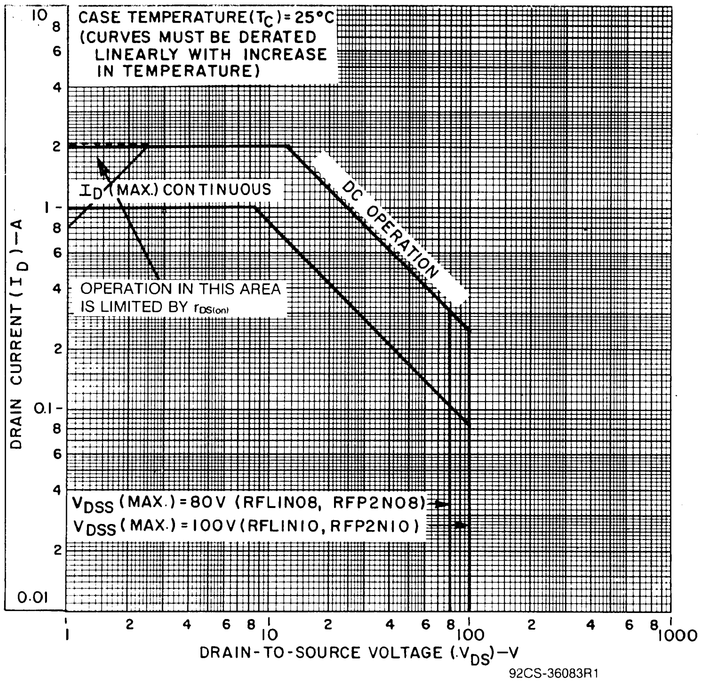


Fig. 1 - Maximum operating areas for all types.

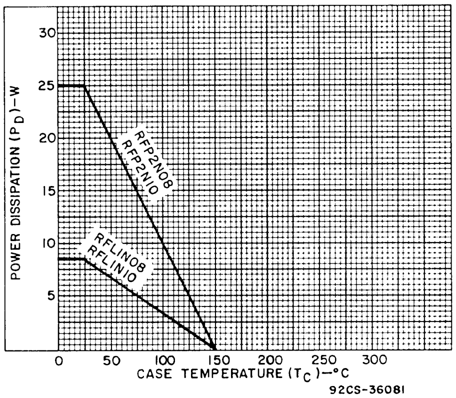


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

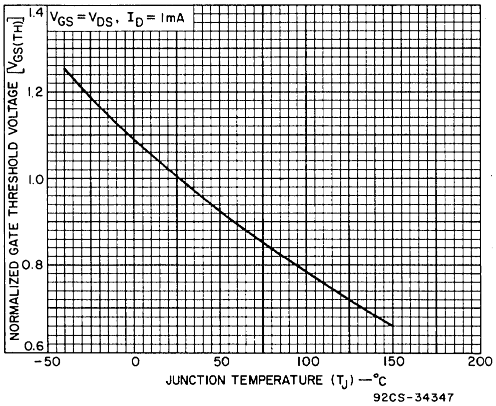


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

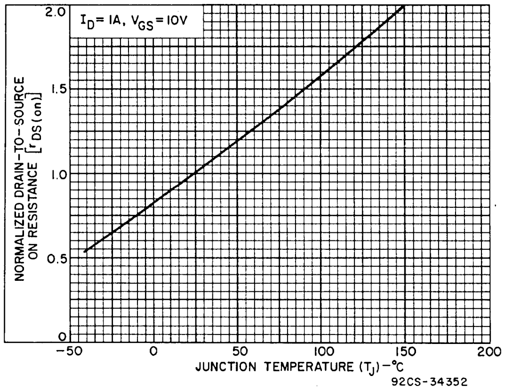


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

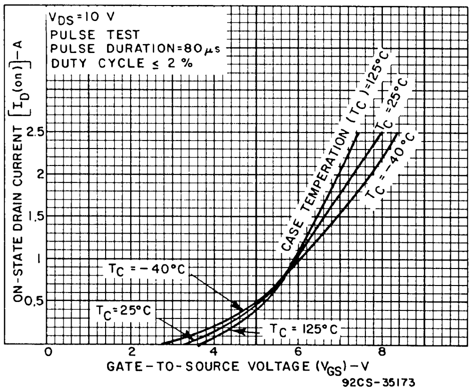


Fig. 5 - Typical transfer characteristics for all types.

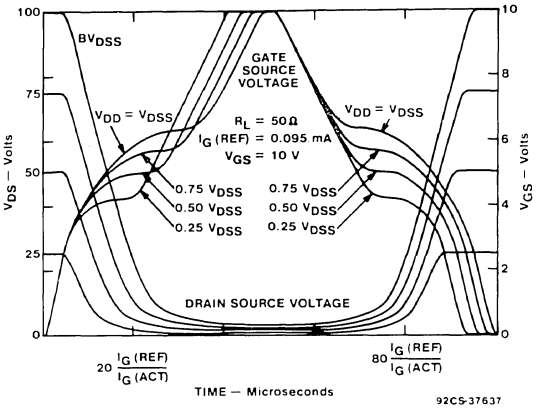


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

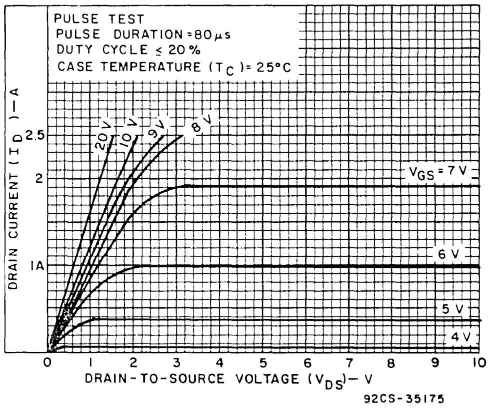


Fig. 7 - Typical saturation characteristics for all types.

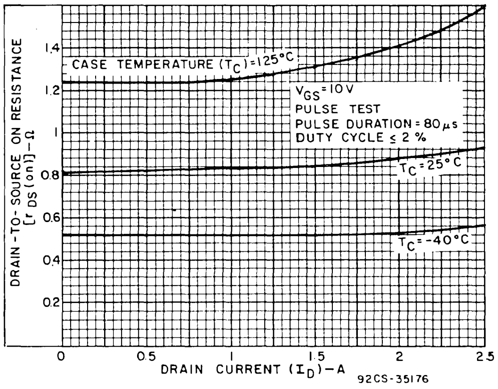


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

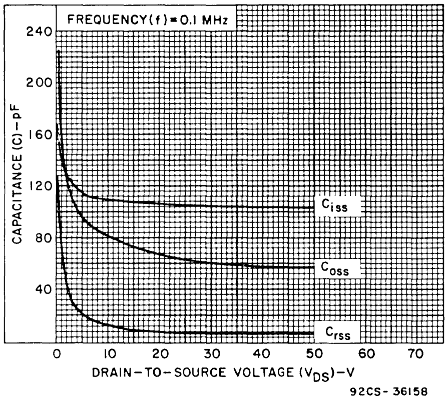


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

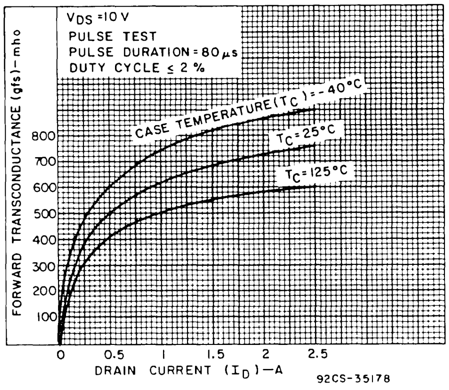


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

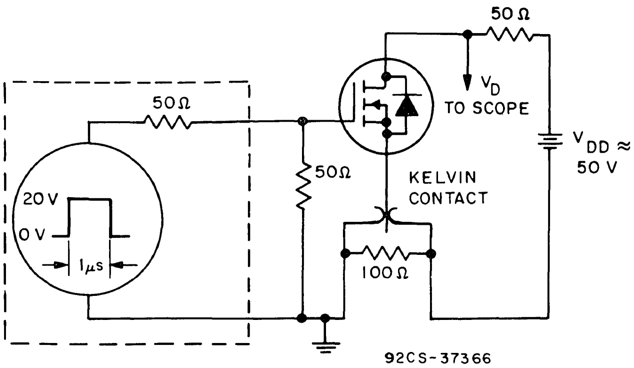


Fig. 11 - Switching Time Test Circuit.

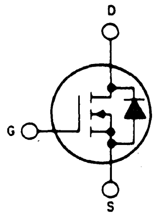
N-Channel Enhancement-Mode Power Field-Effect Transistors

1 and 2 Amperes 120 V — 150 V

$r_{DS}(on)$: 2.0Ω and 2.15Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-Channel Enhancement Mode

The RFL1N12 and RFL1N15 and the RFP2N12 and RFP2N15* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-39 metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

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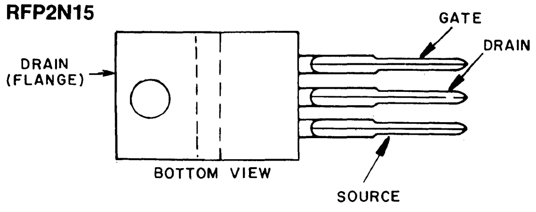
*The RFL and RFP series were formerly RCA developmental numbers TA9196 and TA9213, respectively.

RFP2N12
RFP2N15

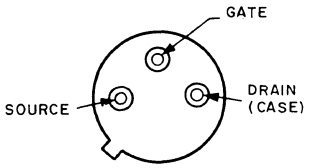
TERMINAL DESIGNATIONS



92CS-37556

JEDEC TO-220AB

RFL1N12
RFL1N15



92CS-37555

JEDEC TO-39

MAXIMUM RATINGS, *Absolute-Maximum Values (T_c=25°C):*

		RFL1N12	RFL1N15		RFP1N12	RFP2N15	
DRAIN-SOURCE VOLTAGE	V_{DSS}	120	150		120	150	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)	V_{DGR}	120	150		120	150	V
GATE-SOURCE VOLTAGE	V_{GS}			±20			V
DRAIN CURRENT RMS Continuous	I_D	1A	1A		2A	2A	A
Pulsed	I_{DM}			5			A
POWER DISSIPATION							
@ T_C=25°C	P_T	8.33	8.33		25	25	W
Derate above T_C=25°C		0.0667	0.0667		0.2	0.2	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}			-55 to +150			°C

ELECTRICAL CHARACTERISTICS *at Case Temperature (T_c) = 25° C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL1N12 RFP2N12		RFL1N15 RFP2N15		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 1$ mA $V_{GS} = 0$	120	—	150	—	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$ $I_D = 2$ mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100$ V	—	1	—	—	μA
		$V_{DS} = 120$ V	—	—	—	1	
		$T_C = 125°$C					
		$V_{DS} = 100$ V	—	50	—	—	
		$V_{DS} = 120$ V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20$ V $V_{DS} = 0$	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	$I_D = 1$ A $V_{GS} = 10$ V	—	2	—	2	V
		$I_D = 2$ A $V_{GS} = 10$ V	—	6	—	6	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	$I_D = 1$ A $V_{GS} = 10$ V RFP	—	2	—	2	Ω
		RFL	—	2.15	—	2.15	
Forward Transconductance	g_{fs}[a]	$V_{DS} = 10$ V $I_D = 1$ A	400	—	400	—	mmho
Input Capacitance	C_{iss}	$V_{DS} = 25$ V	—	150	—	150	pF
Output Capacitance	C_{oss}	$V_{GS} = 0$ V	—	80	—	80	
Reverse Transfer Capacitance	C_{rss}	f = 0.1 MHz	—	20	—	20	
Turn-On Delay Time	$t_d(on)$	$V_{DD} = 75$ V	17(typ.)	25	17(typ.)	25	ns
Rise Time	t_r	$I_D = 1$ A	30(typ.)	45	30(typ.)	45	
Turn-Off Delay Time	$t_d(off)$	$R_{gen} = R_{gs} = 50\ \Omega$	30(typ.)	45	30(typ.)	45	
Fall Time	t_f	$V_{GS} = 10$ V	17(typ.)	25	17(typ.)	25	
Thermal Resistance Junction-to-Case	$R\theta JC$	RFL1N12, RFL1N15	—	15	—	15	°C/W
		RFP2N12, RFP2N15	—	5	—	5	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL1N12 RFP2N12		RFL1N15 RFP2N15		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}[a]	$I_{SD} = 1$A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	$I_F = 2$A $d_{IF}/d_t = 50$A/μs	150(typ.)		150(typ.)		ns

[a] Pulsed: Pulse duration = 300 μs duty cycle = 2%.

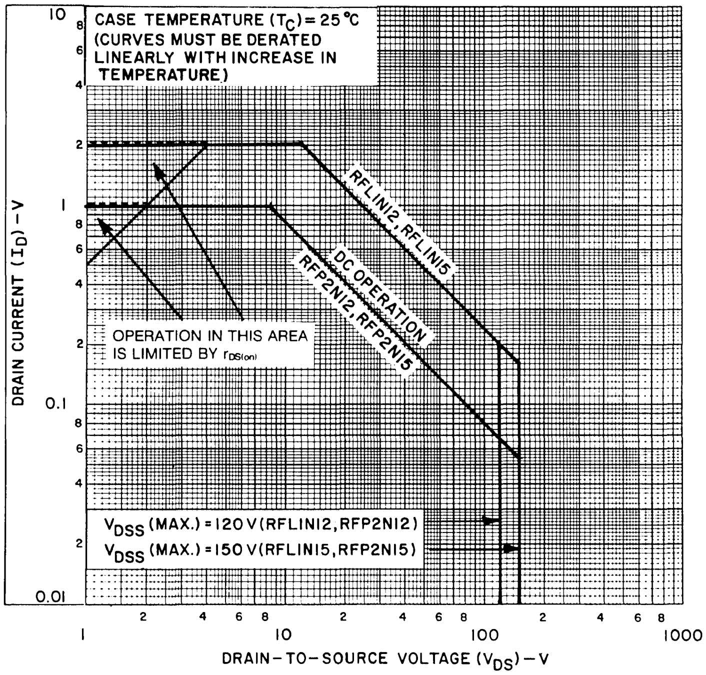


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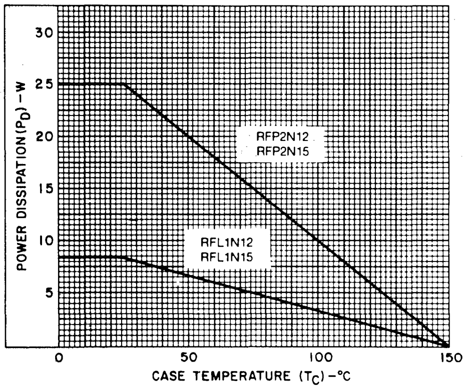
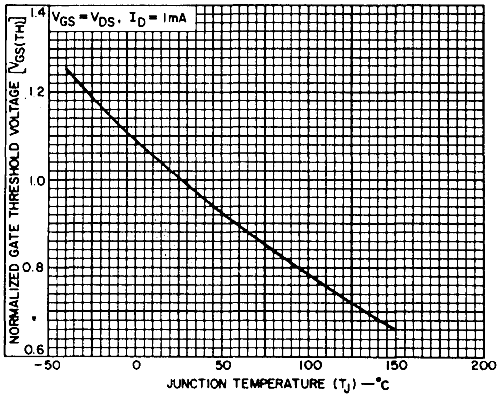
Fig. 1 — Maximum operating areas for all types.



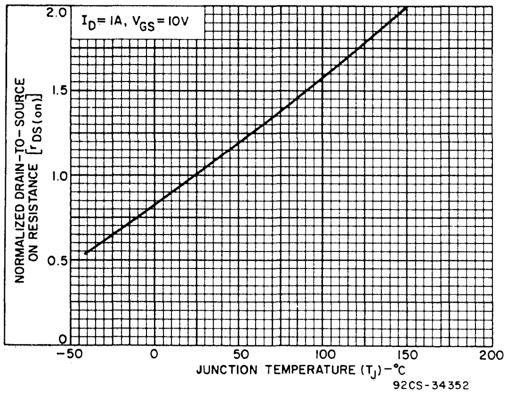
92CS-36354R1



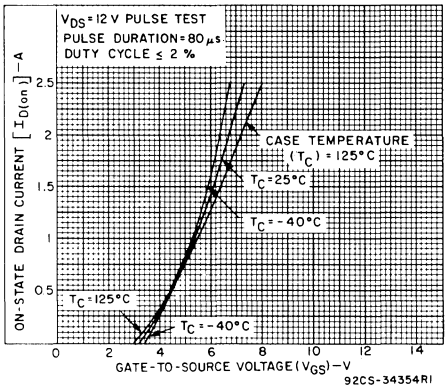
92CS-34347

Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.



92CS-34352



92CS-34354R1

Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

Fig. 5 — Typical transfer characteristics for all types.

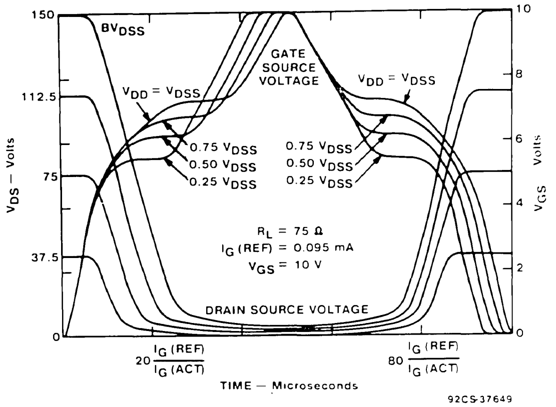


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

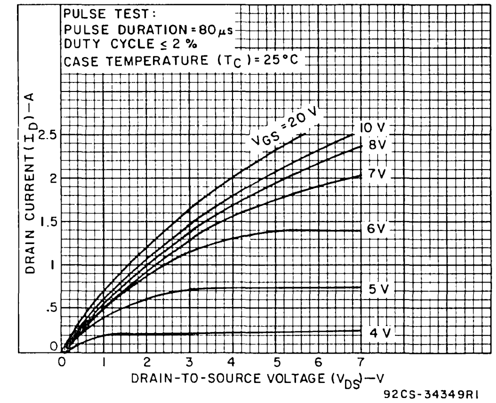


Fig. 7 — Typical saturation characteristics for all types.

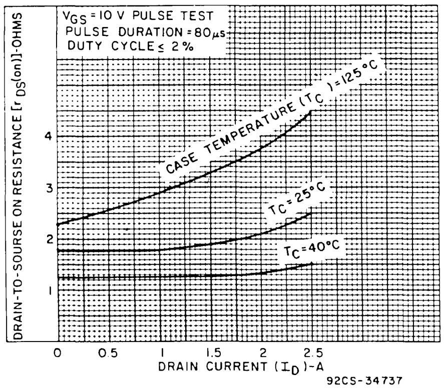


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

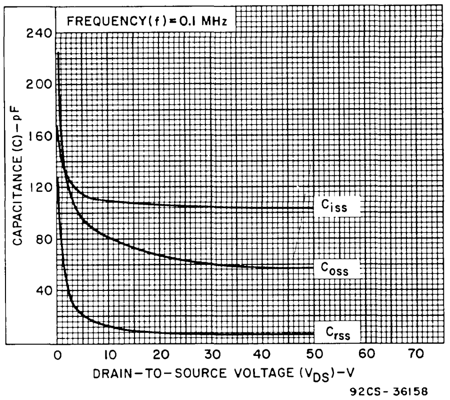


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

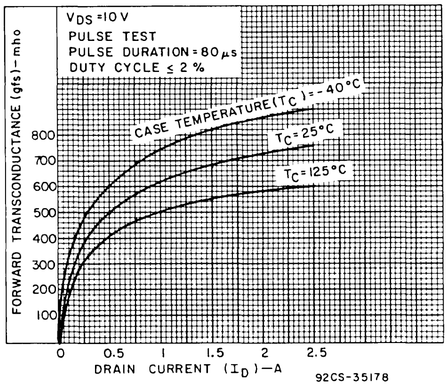


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

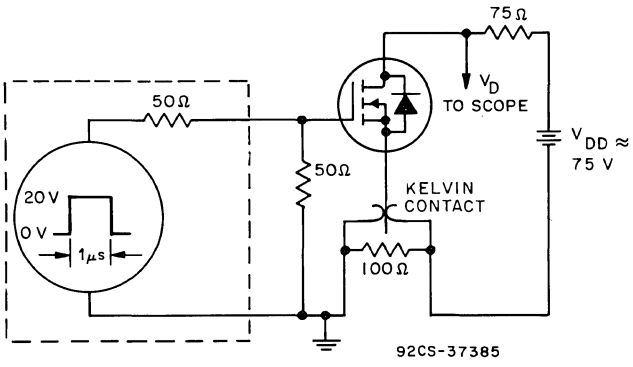


Fig. 11 — Switching Time Test Circuit.

RFL1N18, RFL1N20, RFP2N18, RFP2N20 File Number **1442**

N-Channel Enhancement-Mode Power Field-Effect Transistors

1 and 2 A, 180 and 200 V
r_{DS}(on): 3Ω and 3.15Ω

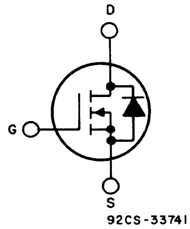
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The RFL1N18 nd RFL1N20 and the RFP2N18 and RFP2N20 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-39 metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

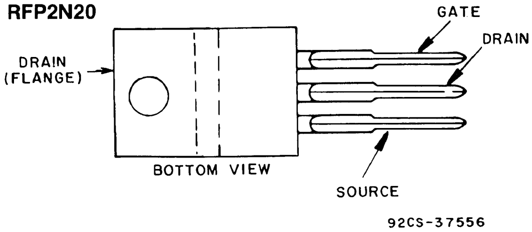
The RFL and RFP series were formerly RCA developmental numbers TA9289 and TA9290, respectively.



N-CHANNEL ENHANCEMENT MODE

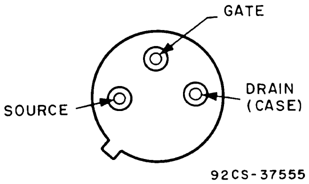
RFP2N18
RFP2N20

TERMINAL DESIGNATIONS



JEDEC TO-220AB

RFL1N18
RFL1N20



JEDEC TO-39

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFL1N18	RFL1N20	RFP2N18	RFP2N20	
DRAIN-SOURCE VOLTAGE	V_{DSS}	180	200	180	200	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)	V_{DGR}	180	200	180	200	V
GATE-SOURCE VOLTAGE	V_{GS}	±20				V
DRAIN CURRENT RMS Continuous	I_D	1	1	2	2	A
Pulsed	I_{DM}	5				A
POWER DISSIPATION	P_T					
@ T_C=25° C		8.33	8.33	25	25	W
Derate above T_C=25° C		0.0667	0.0667	0.2	0.2	W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150				° C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL1N18 RFP2N18		RFL1N20 RFP2N20		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	180	—	200	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V	—	1	—	—	μA
		V_{DS}=160 V	—	—	—	1	
		T_C=125° C					
		V_{DS}=145 V	—	50	—	—	
		V_{DS}=160 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)^a$	I_D=1 A V_{GS}=10 V	—	3	—	3	V
		I_D=2 A V_{GS}=10 V	—	8	—	8	
Static Drain-Source On Resistance	$r_{DS}(on)^a$	I_D=1 A RFP	—	3	—	3	Ω
		V_{GS}=10 V RFL	—	3.15	—	3.15	
Forward Transconductance	$g_{fs}{}^a$	V_{DS}=10 V I_D=1 A	400	—	400	—	mmho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	200	—	200	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	60	—	60	
Reverse-Transfer Capacitance	C_{rss}	f = 0.1 MHz	—	20	—	20	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 100 V	15(Typ)	25	15(Typ)	25	ns
Rise Time	t_r	I_D=1 A	20(Typ)	30	20(Typ)	30	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	25(Typ)	40	25(Typ)	40	
Fall Time	t_f	V_{GS}=10 V	15(Typ)	25	15(Typ)	25	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFL1N18, RFL1N20	—	15	—	15	°C/W
		RFP2N18, RFP2N20	—	5	—	5	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL1N18 RFP2N18		RFL1N20 RFP2N20		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	$V_{SD}{}^a$	I_{SD} = 1A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 2A d_{IF}/d_t = 50A/μs	200(typ.)		200(typ.)		ns

[a] Pulsed: Pulse duration=300 μs max., duty cycle=2%.

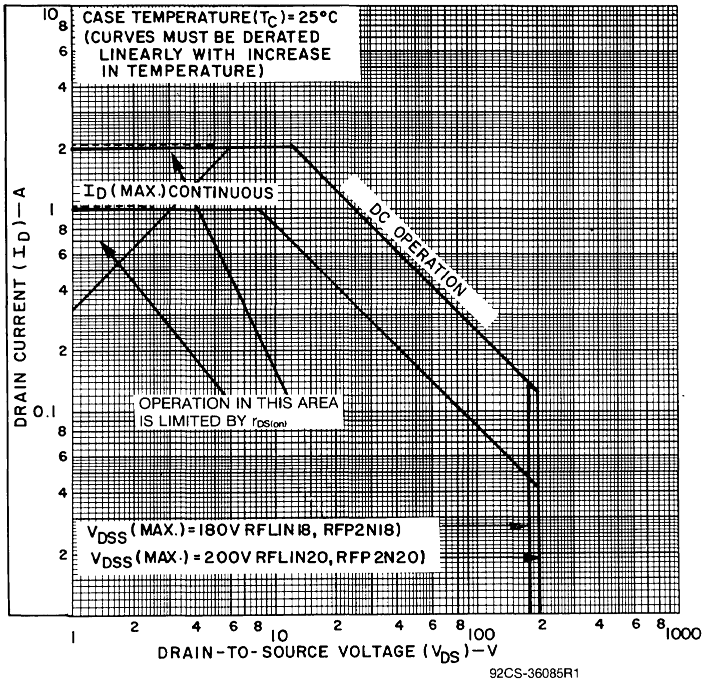


Fig. 1 - Maximum operating areas for all types.

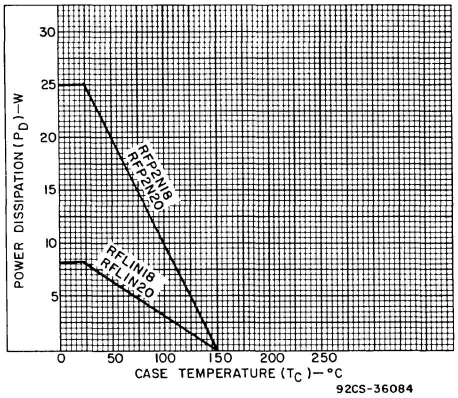


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

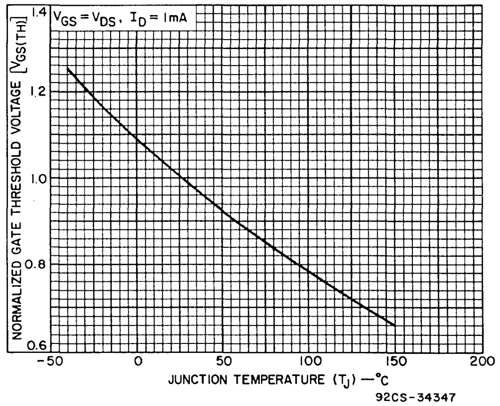


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

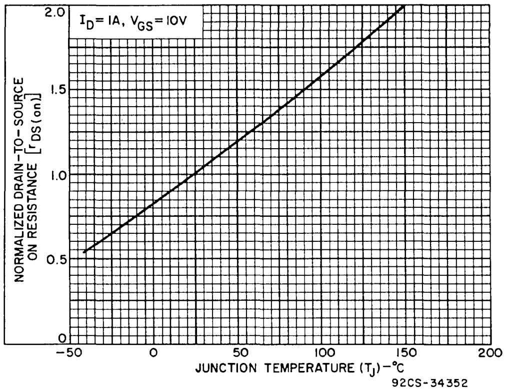


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

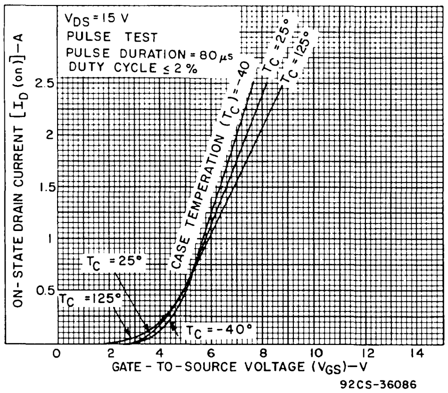


Fig. 5 - Typical transfer characteristics for all types.

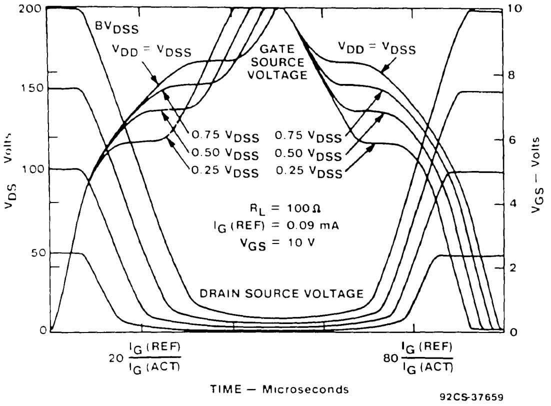


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

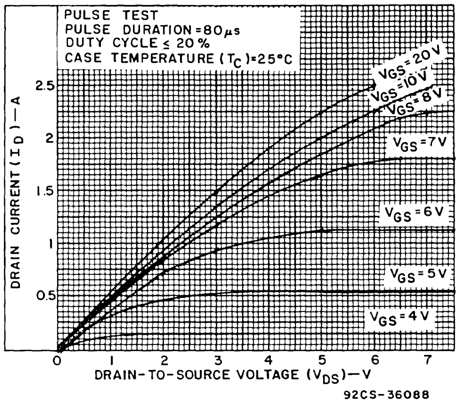


Fig. 7 - Typical saturation characteristics for all types.

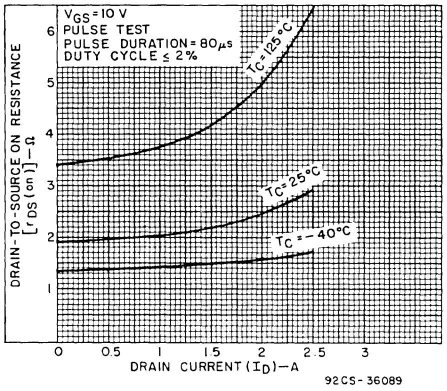


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

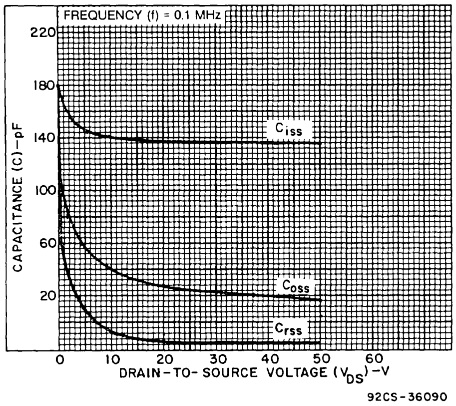


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

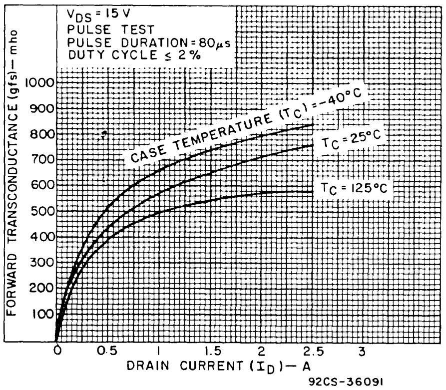


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

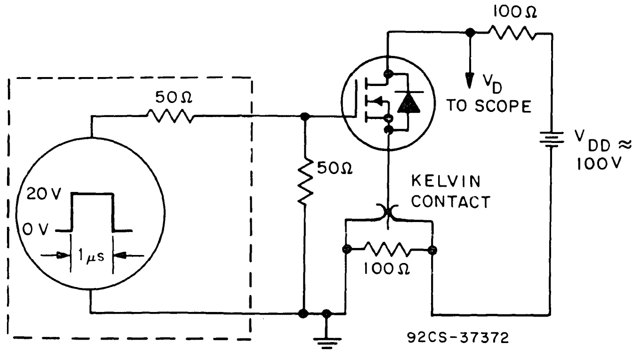
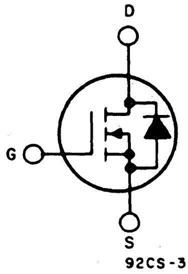


Fig. 11 — Switching Time Test Circuit.

N-Channel Enhancement-Mode Power Field-Effect Transistors

2 and 4 Amperes, 50 V - 60 V
$r_{DS}(on) = 0.80\Omega$ and 0.95Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

The RFL2N05 and RFL2N06 and the RFP4N05 and RFP4N06* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-39 metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

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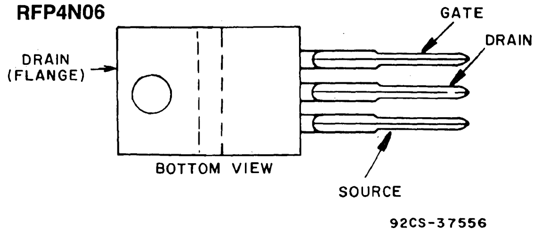
*The RFL and RFP series were formerly RCA developmental numbers TA9378 and TA9379, respectively.

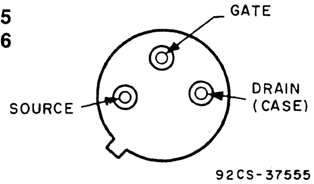
TERMINAL DESIGNATIONS

RFP4N05
RFP4N06



JEDEC TO-220AB

RFL2N05
RFL2N06



JEDEC TO-39

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFL2N05	RFL2N06		RFP4N05	RFP4N06	
DRAIN-SOURCE VOLTAGE .... V_{DSS}	50	60		50	60	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) .... V_{DGR}	50	60		50	60	V
GATE-SOURCE VOLTAGE .... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ...... I_D	2	2		4	4	A
Pulsed .... I_{DM}			10			A
POWER DISSIPATION @ T_C=25° C .... P_T	8.33	8.33		25	25	W
Derate above T_C=25° C	0.0667	0.0667		0.2	0.2	W/° C
OPERATING AND STORAGE TEMPERATURE .... T_j, T_{stg}			-55 to +150			° C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

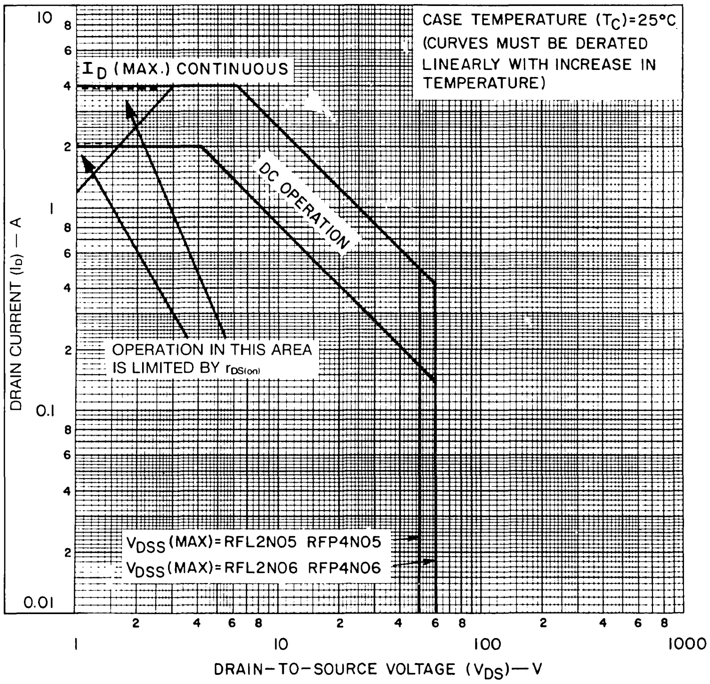
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL2N05 RFP4N05		RFL2N06 RFP4N06		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	60	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40 V V_{DS}=50 V	— —	1 —	— —	— 1	µA
		T_C=125° C V_{DS}=40 V V_{DS}=50 V	— —	50 —	— —	— 50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)^a$	I_D=1 A V_{GS}=10 V	—	.8	—	.8	V
		I_D=2 A V_{GS}=10 V	—	2.0	—	2.0	
		I_D=4 A V_{DS}=15 V	—	4.8	—	4.8	
Static Drain-Source On Resistance	$r_{DS}(on)^a$	I_D=1 A RFP	—	.8	—	.8	Ω
		V_{GS}=10 V RFL	—	.95	—	.95	
Forward Transconductance	g_{fs}^a	V_{DS}=10 V I_D=1 A	400	—	400	—	mmho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	150	—	150	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	85	—	85	
Reverse Transfer Capacitance	C_{rss}	f=0.1 MHz	—	30	—	30	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 30 V	6(typ)	15	6(typ)	15	ns
Rise Time	t_r	I_D=1 A	14(typ)	30	14(typ)	30	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	16(typ)	30	16(typ)	30	
Fall Time	t_f	V_{GS}=10 V	14(typ)	25	14(typ)	25	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFL2N05, RFL2N06	—	15	—	15	°C/W
		RFP4N05, RFP4N06	—	5	—	5	

[a] Pulsed: Pulse duration = 300 µs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

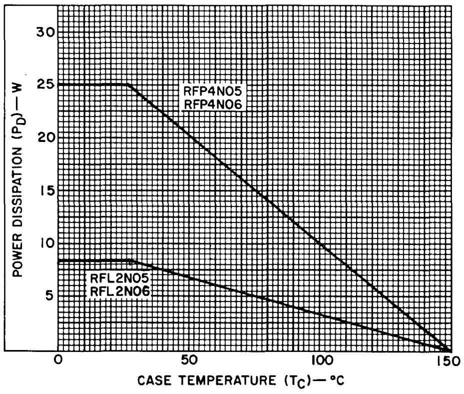
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL2N05 RFP4N05		RFL2N06 RFP4N06		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 1A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 2A d_{IF}/d_t = 50A/µs	100(typ.)		100(typ.)		ns

*Pulse Test: Width ≤ 300 µs, Duty Cycle ≤ 2%.



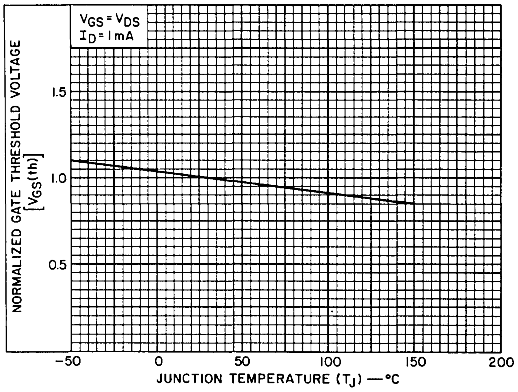
92CS-37097R1

Fig. 1 — Maximum operating areas for all types.



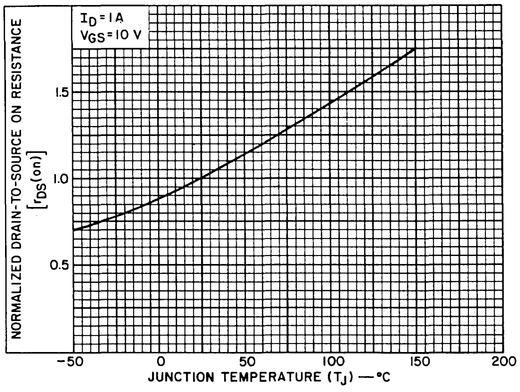
92CS-37098

Fig. 2 — Power dissipation vs. case temperature derating curve for all types.



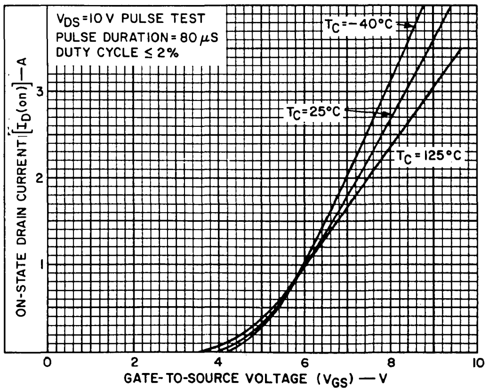
92CS-37099

Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.



92CS-37100

Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.



92CS-37101

Fig. 5 — Typical transfer characteristics for all types.

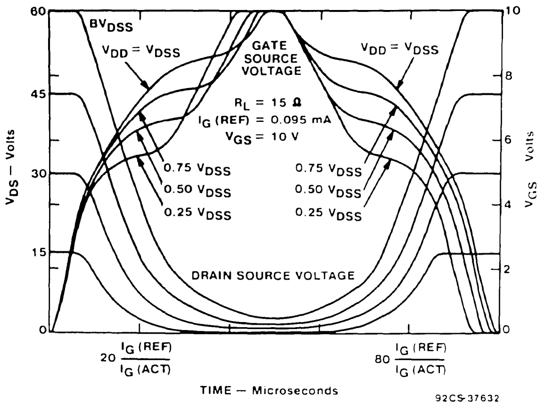


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

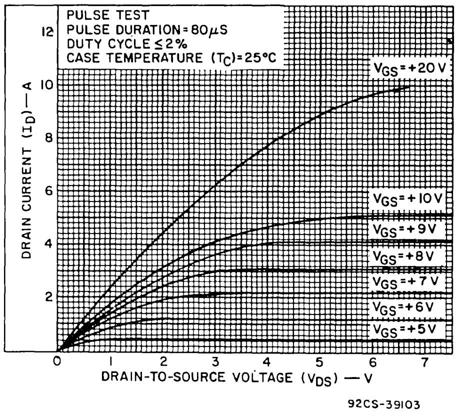


Fig. 7 — Typical saturation characteristics for all types.

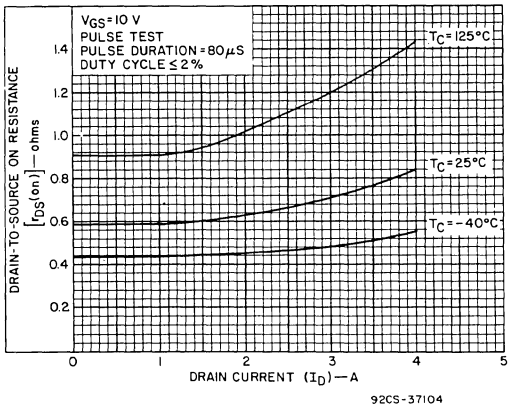


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

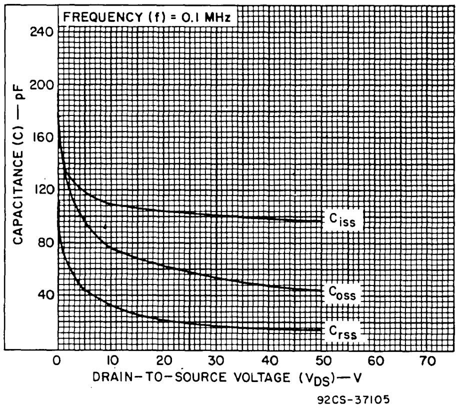


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

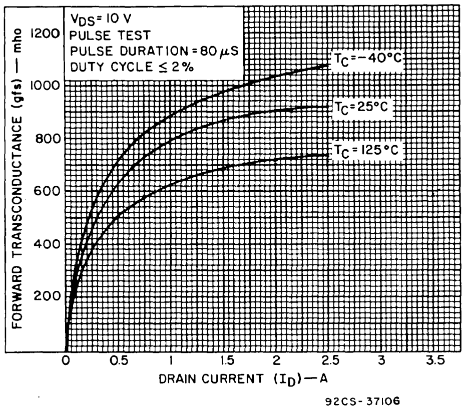


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

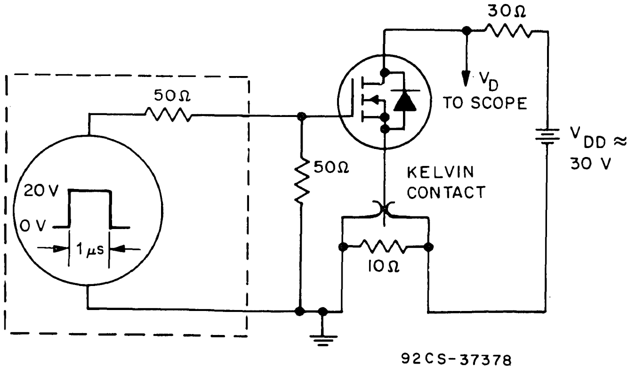


Fig. 11 — Switching Time Test Circuit.

RFM3N45, RFM3N50, RFP3N45, RFP3N50

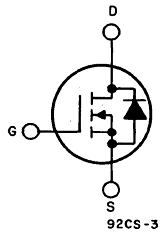
File Number **1384**

N-Channel Enhancement-Mode Power Field-Effect Transistors

3 A, 450 and 500 V

$r_{DS\ (on)}$: 3 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

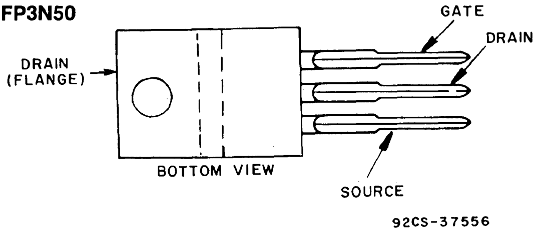
The RFM3N45 and RFM3N50 and the RFP3N45 and RFP3N50 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-series types are supplied in the JEDEC TO-204MA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFM and RFP series were formerly RCA developmental numbers TA9193 and TA9232, respectively.

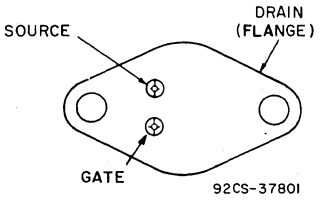
TERMINAL DESIGNATIONS

RFP3N45
RFP3N50



JEDEC TO-220AB

RFM3N45
RFM3N50



JEDEC TO-204MA

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM3N45	RFM3N50		RFP3N45	RFP3N50	
DRAIN-SOURCE VOLTAGE .... V_{DSS}	450	500		450	500	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) ... V_{DGR}	450	500		450	500	V
GATE-SOURCE VOLTAGE .... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			3			A
Pulsed .... I_{DM}			5			A
POWER DISSIPATION @ T_C=25°C .... P_T	75	75		60	60	W
Derate above T_C=25°C	0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE .... T_j, T_{stg}			-55 to +150			°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM3N45 RFP3N45		RFM3N50 RFP3N50		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	450	—	500	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	$V_{GS}=V_{DS}$ I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=360 V	—	10	—	—	μA
		V_{DS}=400 V	—	—	—	10	
		T_C=125° C V_{DS}=360 V	—	50	—	—	
		V_{DS}=400 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)^a$	I_D=1.5 A V_{GS}=10 V	—	4.5	—	4.5	V
		I_D=3 A V_{GS}=10 V	—	10.5	—	10.5	
Static Drain-Source On Resistance	$r_{DS}(on)^a$	I_D=1.5 A V_{GS}=10 V	—	3	—	3	Ω
Forward Transconductance	g_{fs}^a	V_{DS}=10 V I_D=1.5 A	1	—	1	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	600	—	600	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	150	—	150	
Reverse-Transfer Capacitance	C_{rss}	f=0.1 MHz	—	50	—	50	
Turn-On Delay Time	$t_d(on)$	V_{DD}=250 V	30(Typ)	45	30(Typ)	45	ns
Rise Time	t_r	I_D=1.5 A	40(Typ)	60	40(Typ)	60	
Turn-Off Delay Time	$t_d(off)$	$R_{gen}=R_{gs}$=50 Ω	90(Typ)	135	90(Typ)	135	
Fall Time	t_f	V_{GS}=10 V	50(Typ)	75	50(Typ)	75	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM3N45, RFM3N50	—	1.67	—	1.67	°C/W
		RFP3N45, RFP3N50	—	2.083	—	2.083	

[a] Pulsed: Pulse duration=300 μs max., duty cycle=2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM3N45 RFP3N45		RFM3N50 RFP3N50		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=1.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	800(typ)		800(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

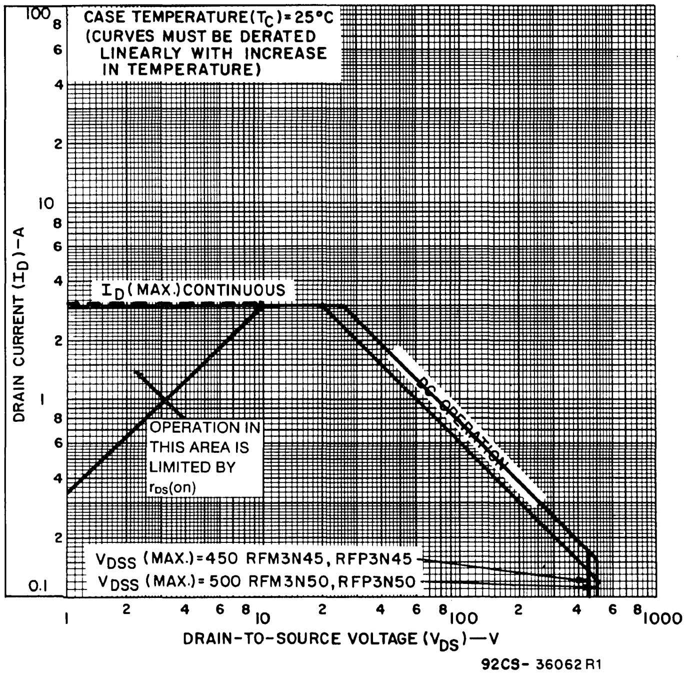


Fig. 1 - Maximum operating areas for all types.

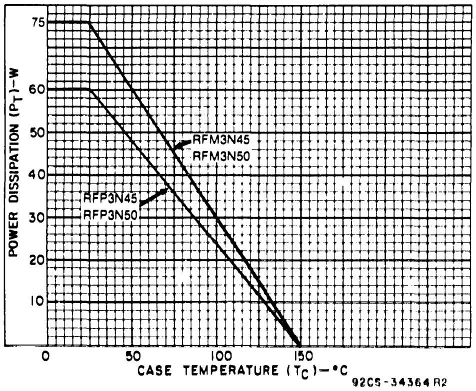


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

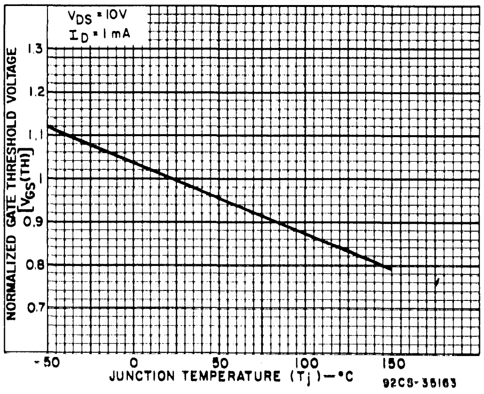


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

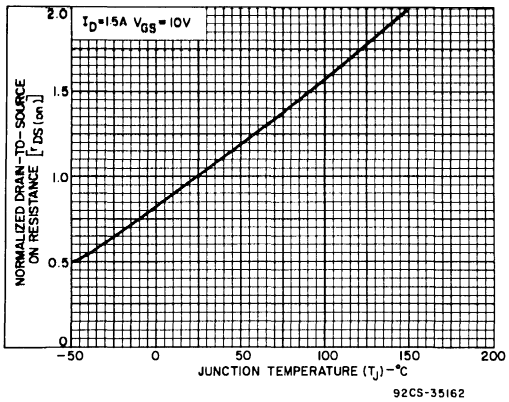


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

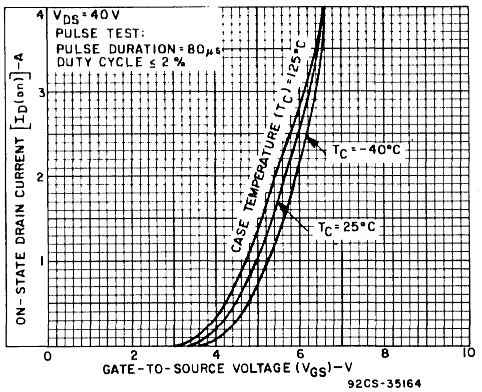


Fig. 5 - Typical transfer characteristics for all types.

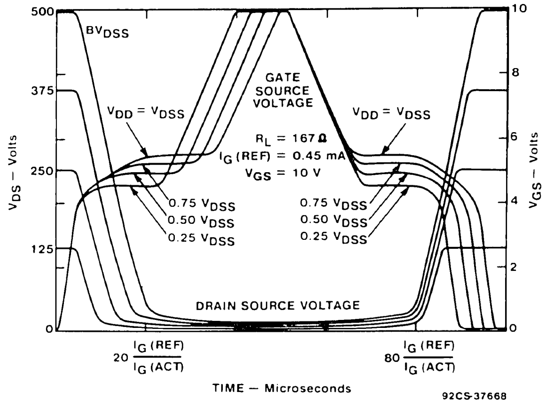


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

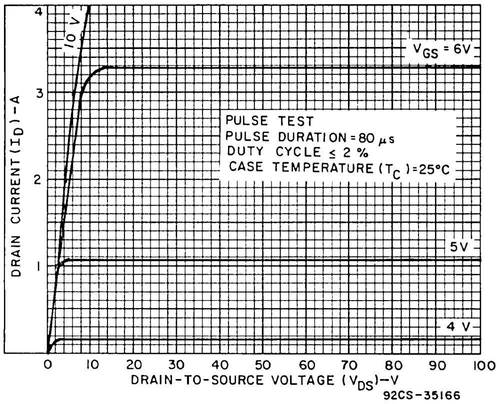


Fig. 7 - Typical saturation characteristics for all types.

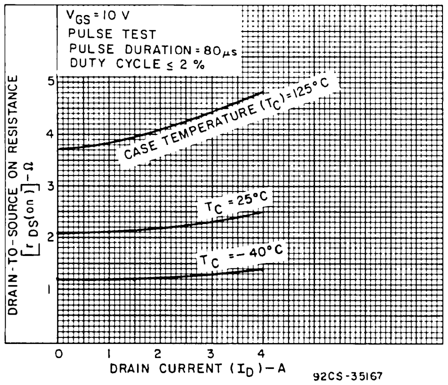


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

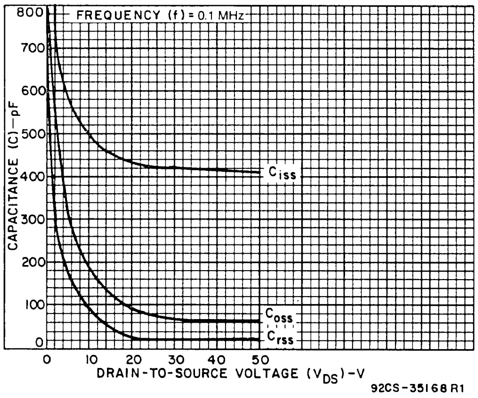


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

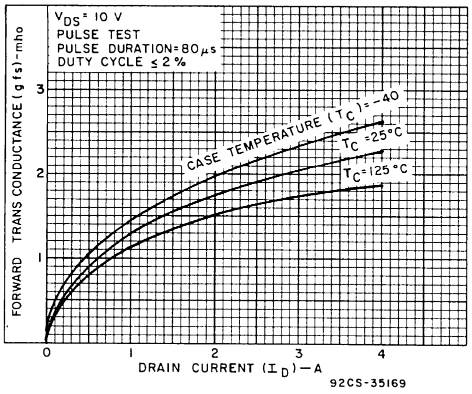


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

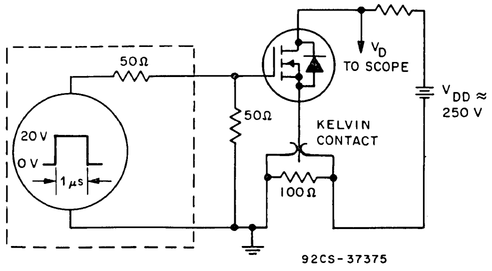
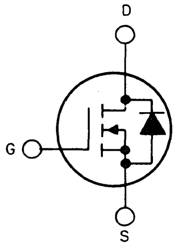


Fig. 11 — Switching Time Test Circuit

N-Channel Enhancement-Mode Power Field-Effect Transistors

4 A, 120 and 150 V
$r_{DS}(on)$: 0.45Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

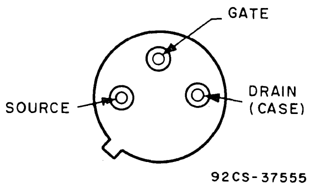


N-CHANNEL ENHANCEMENT MODE

The RFL4N12 and RFL4N15* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-39 metal package.

TERMINAL DESIGNATIONS



JEDEC TO-39

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFL4N12	RFL4N15	
DRAIN-SOURCE VOLTAGE	V_{DSS}	120	150	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)	V_{DGR}	120	150	V
GATE-SOURCE VOLTAGE	V_{GS}	±20	±20	V
DRAIN CURRENT RMS Continuous	I_D	4	4	A
Pulsed	I_{DM}	15	15	A
POWER DISSIPATION @ T_C=25° C	P_T	8.33	8.33	W
Derate above T_C=25° C		0.0667	0.0667	W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150	-55 to +150	° C

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*The RFL4N12 and RFL4N15 series were formerly RCA developmental numbers TA9256A and TA9256B, respectively.

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL4N12		RFL4N15		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	150	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=100 V	—	1	—	—	μA
		V_{DS}=120 V	—	—	—	1	
		T_C=125° C V_{DS}=100 V	—	50	—	—	
		V_{DS}=120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)^a$	I_D=2 A V_{GS}=10 V	—	0.8	—	0.8	V
		I_D=4 A V_{GS}=10 V	—	3	—	3	
Static Drain-Source On Resistance	$r_{DS}(on)^a$	I_D=2 A V_{GS}=10 V	—	.45	—	.45	Ω
Forward Transconductance	$g_{fs}{}^a$	V_{DS}=10 V I_D=2 A	1.5	—	1.5	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f = 0.1MHz	—	650	—	650	pF
Output Capacitance	C_{oss}		—	230	—	230	
Reverse-Transfer Capacitance	C_{rss}		—	60	—	60	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 75 V I_D=2 A R_{gen}=R_{gs}=50 Ω V_{GS}=10 V	40(typ)	60	40(typ)	60	ns
Rise Time	t_r		165(typ)	250	165(typ)	250	
Turn-Off Delay Time	$t_d(off)$		90(typ)	135	90(typ)	135	
Fall Time	t_f		90(typ)	135	90(typ)	135	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFL4N12, RFL4N15	—	15	—	15	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL4N12		RFL4N15		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	$V_{SD}{}^a$	I_{SD} = 2A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	200(typ.)		200(typ.)		ns

[a] Pulsed: Pulse duration=300 μs max., duty cycle=2%.

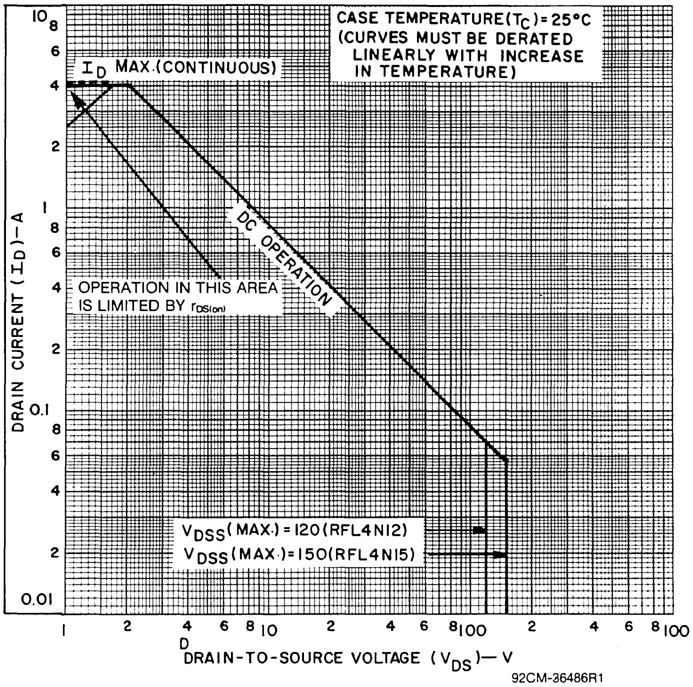

Fig. 1 - Maximum safe operating areas for all types.

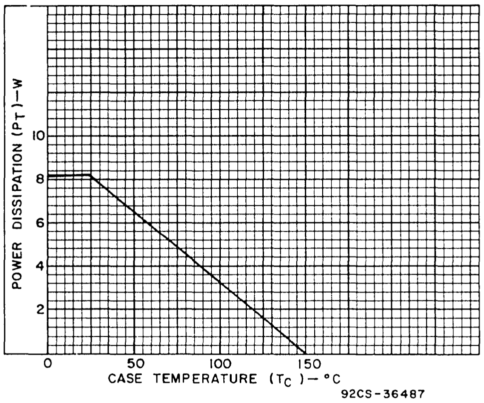

Fig. 2 - Power vs. temperature derating curve for all types.

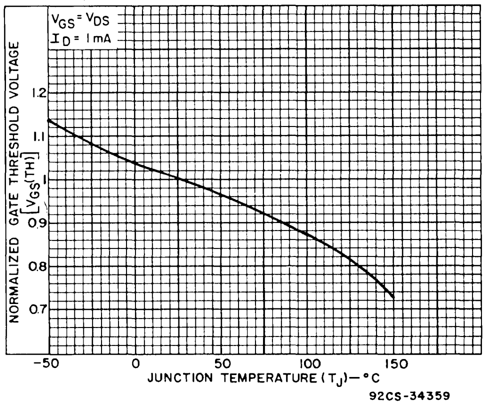

Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

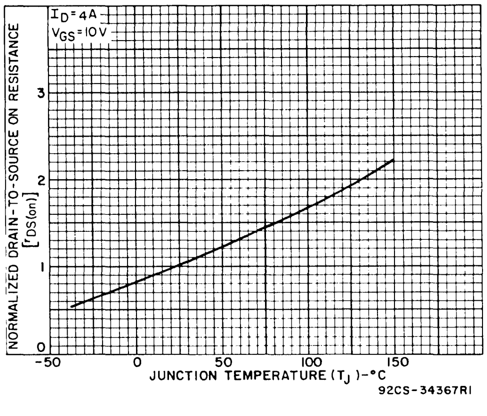

Fig. 4 - Normalized drain-to-source on resistance as a function of junction temperature for all types.

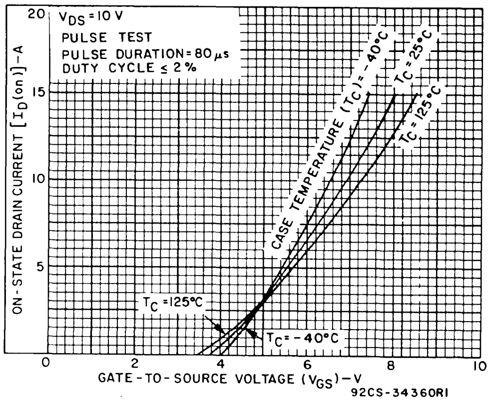

Fig. 5 - Typical transfer characteristics for all types.

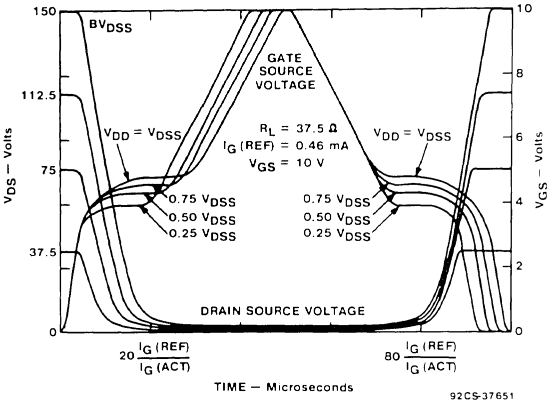

Fig. 6 - Normalized switching waveforms for constant gate-current drive.

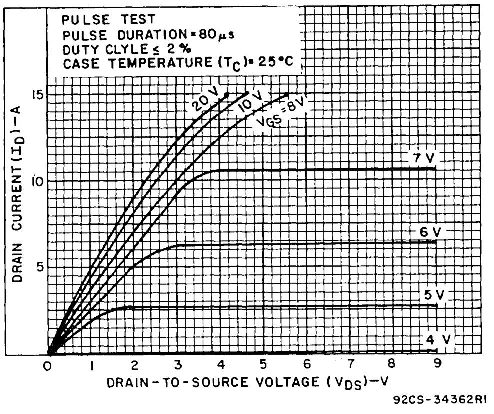

Fig. 7 - Typical saturation characteristics for all types.

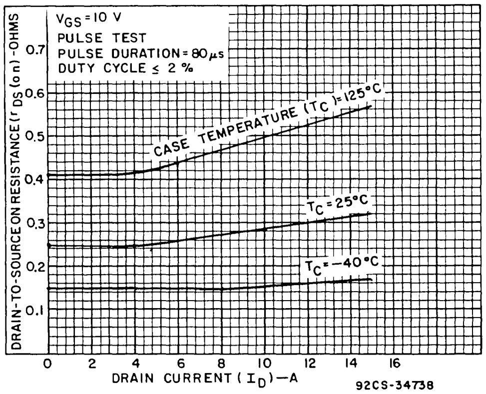

Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

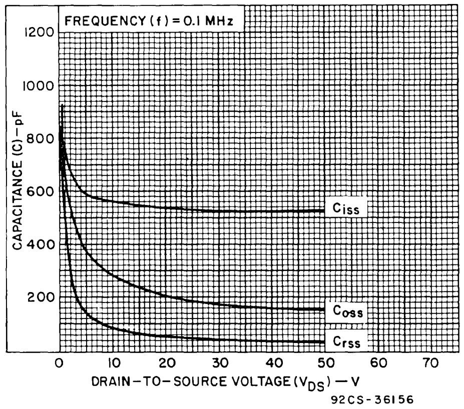

Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

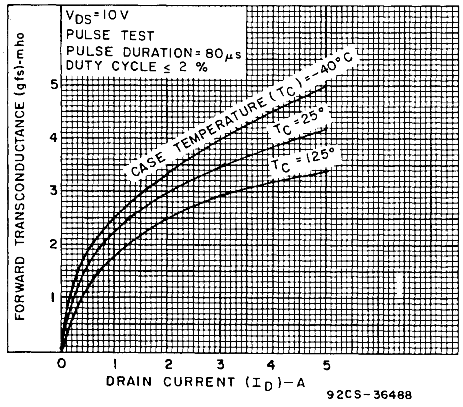

Fig. 10 - Typical forward transconductance as a function of drain current for all types.

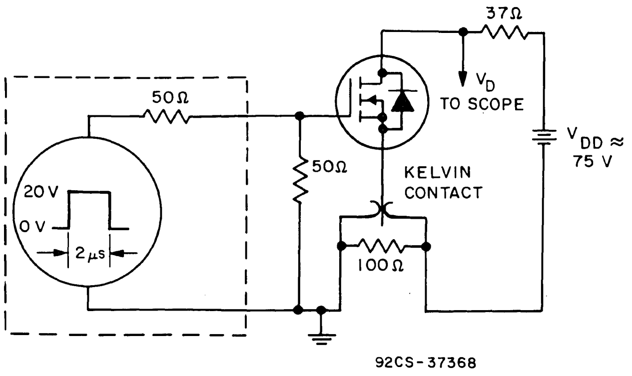

Fig. 11 - Switching Time Test Circuit.

RFM5P12, RFM5P15, RFP5P12, RFP5P15

File Number **1463**

P-Channel Enhancement-Mode Power Field-Effect Transistors

5 A, 120 V — 150 V

$r_{DS}(on)$: 1Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The RFM5P12 and RFM5P15 and the RFP5P12 and RFP5P15 * are P-Channel enhancement-mode silicon gate power field-effect transistors designed for high-speed applications such as switching regulators, switching converters, relay drivers, and drivers for high-power bipolar switching transistors.

The RFM-Series types are supplied in the JEDEC TO-204MA metal package and the RFP-Series types in the JEDEC TO-220AB plastic package. All these types are supplied without an internal gate Zener diode.

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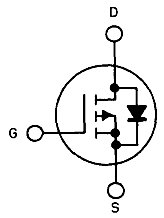
* The RFM and RFP series were formerly RCA developmental numbers TA9320 and TA9321 respectively.

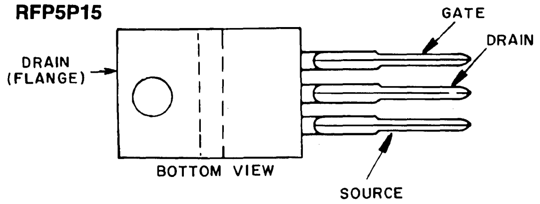


92CS-36485

P-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATIONS

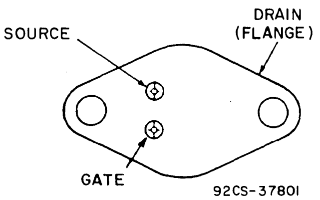
RFP5P12
RFP5P15



92CS-37556

JEDEC TO-220AB

RFM5P12
RFM5P15



92CS-37801

JEDEC TO-204MA

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

		RFM5P12	RFM5P15	RFP5P12	RFP5P15	
DRAIN-SOURCE VOLTAGE	V_{DSS}	-120	-150	-120	-150	V
DRAIN-GATE VOLTAGE (R_{GS} = 1MΩ)	V_{DGR}	-120	-150	-120	-150	V
GATE-SOURCE VOLTAGE	V_{GS}	±20				V
DRAIN CURRENT RMS Continuous	I_D	5				A
Pulsed	I_{DM}	15				A
POWER DISSIPATION	P_T					
@ T_C = 25°C		75	75	60	60	W
Derate above T_C = 25°C		0.6	0.6	0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150				°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM5P12 RFP5P12		RFM5P15 RFP5P15		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 1$ mA $V_{GS} = 0$	-120	—	-150	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$ $I_D = 1$ mA	-2	-4	-2	-4	V
Zero-Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -100$ V	—	1	—	—	μA
		$V_{DS} = -120$ V	—	—	—	1	
		$T_C = 125°C$ $V_{DS} = -100$ V	—	50	—	—	
		$V_{DS} = -120$ V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20$ V $V_{DS} = 0$	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	$I_D = 2.5$ A $V_{GS} = -10$ V	—	-2.5	—	-2.5	V
		$I_D = 5$A $V_{GS} = -10$ V	—	-8	—	-8	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	$I_D = 2.5$ A $V_{GS} = -10$ V	—	1	—	1	Ω
Forward Transconductance	g_{fs}[a]	$V_{DS} = 10$ V $I_D = 2.5$ A	0.75	—	0.75	—	mho
Input Capacitance	C_{iss}	$V_{DS} = 25$ V	—	700	—	700	pF
Output Capacitance	C_{oss}	$V_{GS} = 0$ V	—	300	—	300	
Reverse-Transfer Capacitance	C_{rss}	f = 0.1 MHz	—	100	—	100	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 1/2\ BV_{DSS}$	20(typ.)	60	20(typ.)	60	ns
Rise Time	t_r	$I_D = 2.5$ A	36(typ.)	100	36(typ.)	100	
Turn-Off Delay Time	$t_{d(off)}$	$R_{gen} = R_{gs} = 50\Omega$	63(typ.)	150	63(typ.)	150	
Fall Time	t_f	$V_{GS} = 10$ V	40(typ.)	100	40(typ.)	100	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM5P12, RFM5P15	—	1.67	—	1.67	°C/W
		RFP5P12, RFP5P15	—	2.083	—	2.083	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM5P12 RFP5P12		RFM5P15 RFP5P15		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	$I_{SD} = 2.5$A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	$I_F = 4$A $d_{IF}/d_t = 100$A/μs	300(typ.)		300(typ.)		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

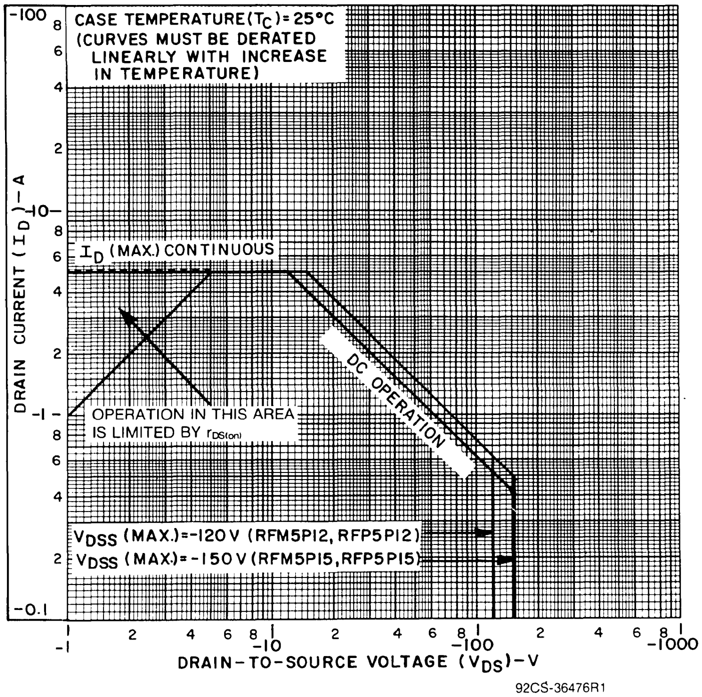


Fig. 1 - Maximum safe operating areas for all types.

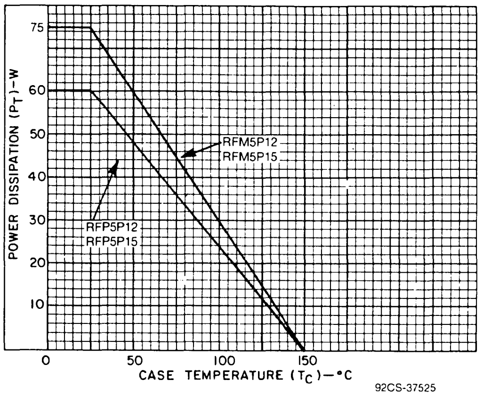


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

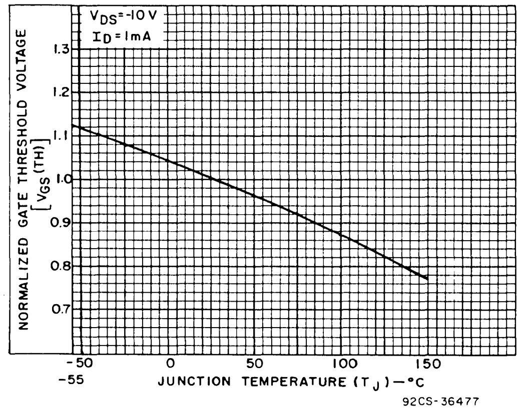


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

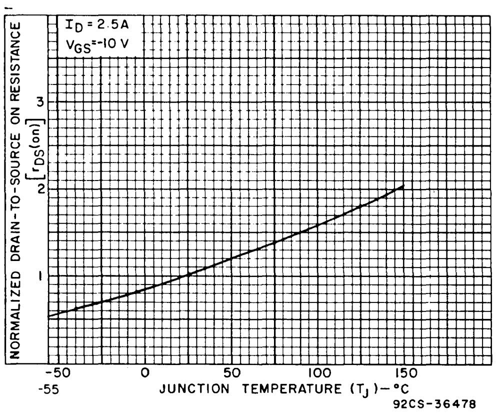


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

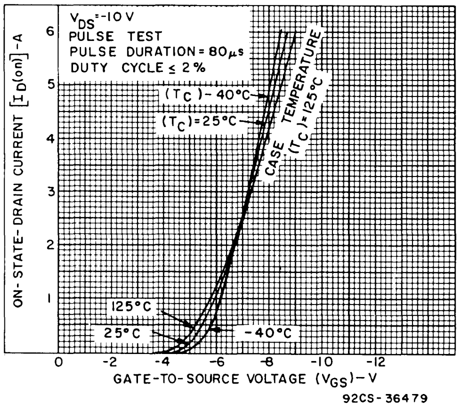


Fig. 5 - Typical transfer characteristics for all types.

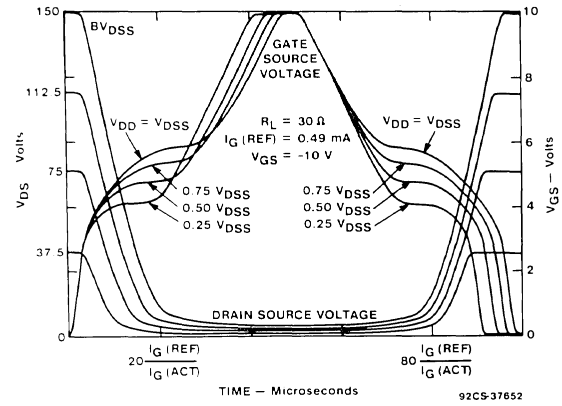


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

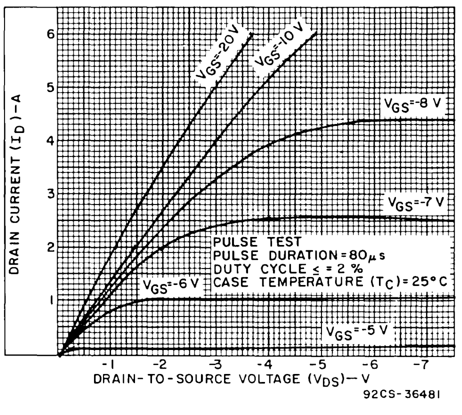


Fig. 7 - Typical saturation characteristics for all types.

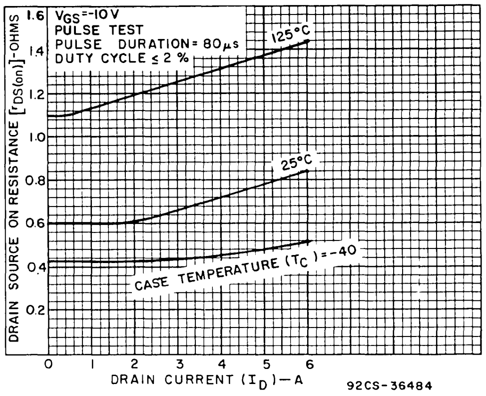


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

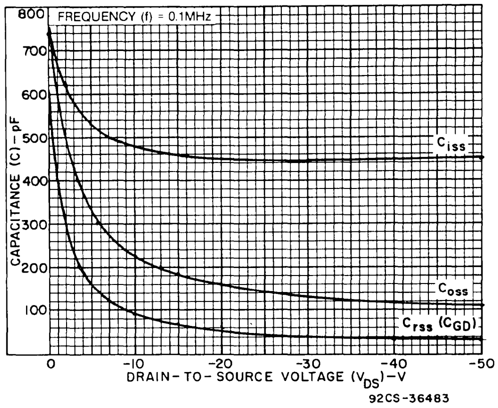


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

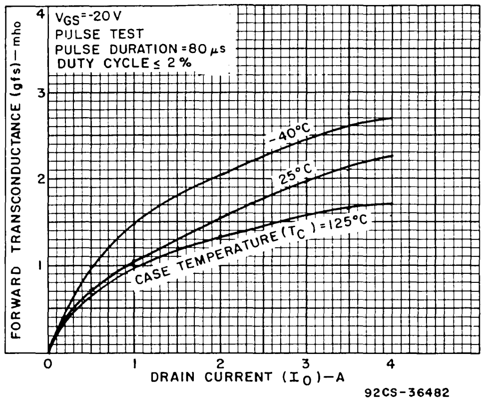


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

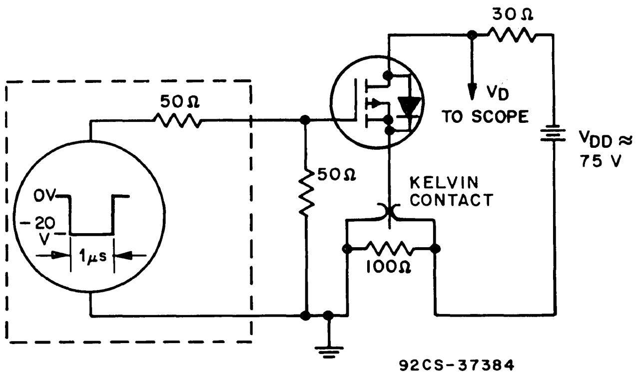
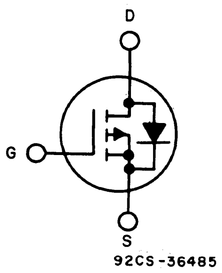


Fig. 11 - Switching Time Test Circuit.

P-Channel Enhancement-Mode Power Field-Effect Transistors

6 A, 80 V — 100 V
$r_{DS}(on) = 0.6\ \Omega$

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



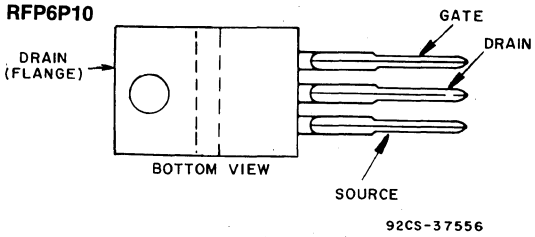
P-CHANNEL ENHANCEMENT MODE

The RFM6P08 and RFM6P10 and the RFP6P08 and RFP6P10* are P-Channel enhancement-mode silicon-gate power field-effect transistors designed for high-speed applications such as switching regulators, switching converters, relay drivers, and drivers for high-power bipolar switching transistors.

The RFM-Series types are supplied in the JEDEC TO-204MA metal package and the RFP-Series types in the JEDEC TO-220AB plastic package. All these types are supplied without an internal gate Zener diode.

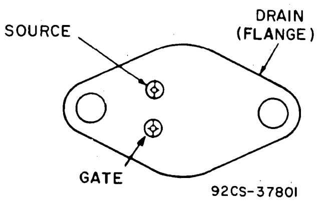
TERMINAL DESIGNATIONS

RFP6P08
RFP6P10



JEDEC TO-220AB

RFM6P08
RFM6P10



JEDEC TO-204MA

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM6P08	RFM6P10		RFP6P08	RFP6P10	
DRAIN-SOURCE VOLTAGE .... V_{DSS}	80	100		80	100	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) ... V_{DGR}	80	100		80	100	V
GATE-SOURCE VOLTAGE .... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			6			A
Pulsed .... I_{DM}			20			A
POWER DISSIPATION @ T_C=25°C .... P_T	75	75		60	60	W
Derate above T_C=25°C	0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE .... T_j, T_{stg}			-55 to +150			°C

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*The RFM and RFP series were formerly RCA developmental numbers TA9406 and TA9407, respectively.

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

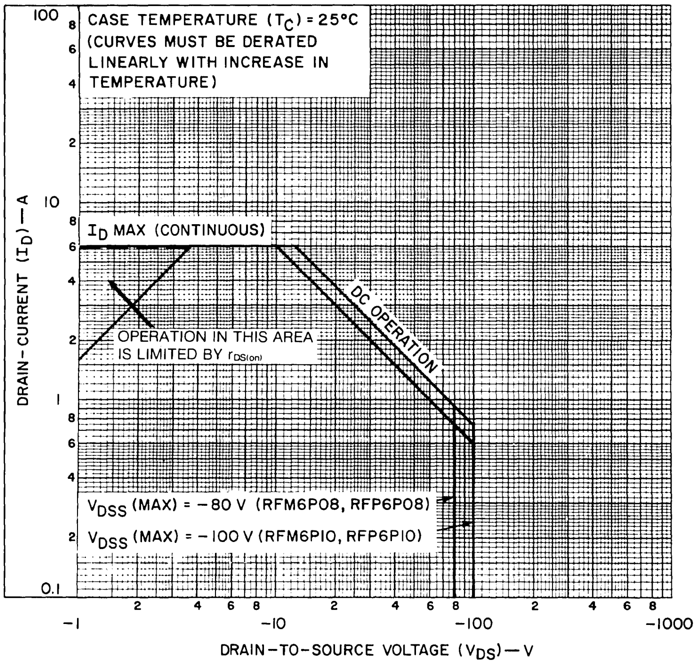
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS RFM6P08 RFP6P08 MIN.	LIMITS RFM6P08 RFP6P08 MAX.	LIMITS RFM6P10 RFP6P10 MIN.	LIMITS RFM6P10 RFP6P10 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	-100	—	V
Gate Threshold Voltage	V_{GS}(th)	V_{GS}=V_{DS} I_D=1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-65 V	—	1	—	—	µA
		V_{DS}=-80 V	—	—	—	1	
		T_C=125° C V_{DS}=-65 V	—	50	—	—	
		V_{DS}=-80 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)^a$	I_D=3 A V_{GS}=-10 V	—	-1.8	—	-1.8	V
		I_D=6 A V_{GS}=-10 V	—	-6	—	-6	
Static Drain-Source On Resistance	$r_{DS}(on)^a$	I_D=3 A V_{GS}=-10 V	—	0.6	—	0.6	Ω
Forward Transconductance	g_{fs}^a	V_{DS}=10 V I_D=3 A	1	—	1	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	800	—	800	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	350	—	350	
Reverse Transfer Capacitance	C_{rss}	f=0.1 MHz	—	150	—	150	
Turn-On Delay Time	t_d(on)	V_{DD} = 50 V	11(typ)	60	11(typ)	60	ns
Rise Time	t_r	I_D=3 A	48(typ)	100	48(typ)	100	
Turn-Off Delay Time	t_d(off)	R_{gen}=R_{gs}=50 Ω	102(typ)	150	102(typ)	150	
Fall Time	t_f	V_{GS}=10 V	70(typ)	100	70(typ)	100	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM6P08, RFM6P10	—	1.67	—	1.67	°C/W
		RFP6P08, RFP6P10	—	2.083	—	2.083	

[a]Pulsed: Pulse duration = 300 µs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

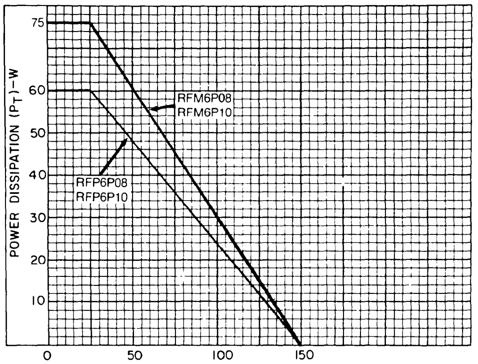
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFM6P08 RFP6P08 MIN.	LIMITS RFM6P08 RFP6P08 MAX.	LIMITS RFM6P10 RFP6P10 MIN.	LIMITS RFM6P10 RFP6P10 MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=3 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=50 A/µs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 µs, duty cycle ≤ 2%.



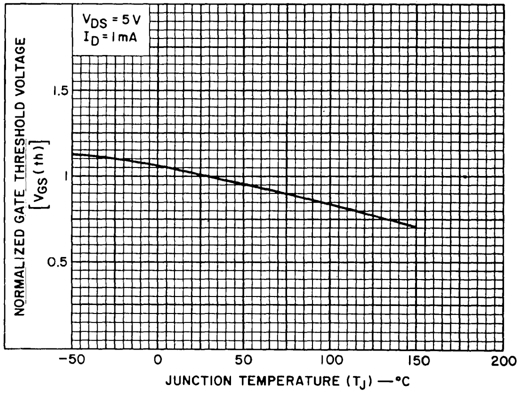
92CS-37039R1

Fig. 1 — Maximum safe operating areas for all types.



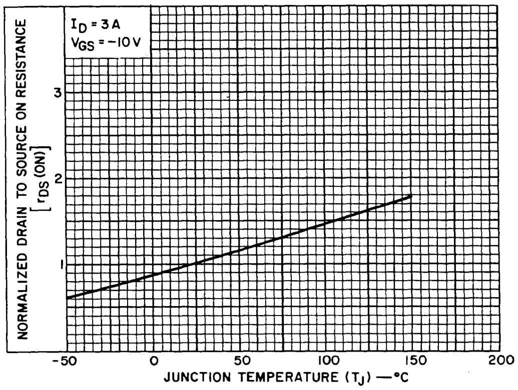
92CS-37528

Fig. 2 — Power dissipation vs. temperature derating curve for all types.



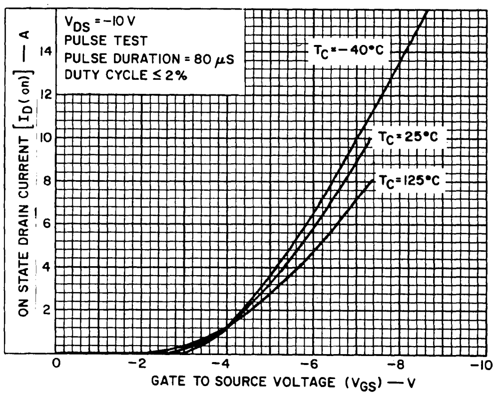
92CS-37047

Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.



92CS-37042

Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.



92CS-37045

Fig. 5 — Typical transfer characteristics for all types.

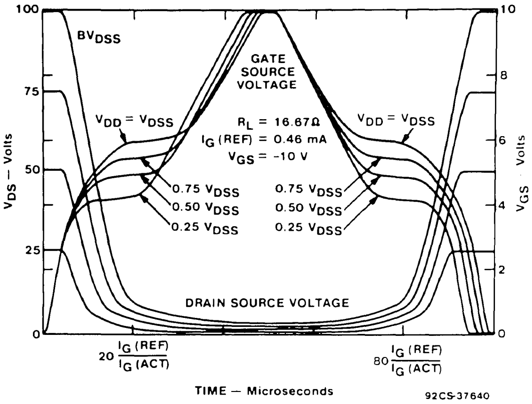


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

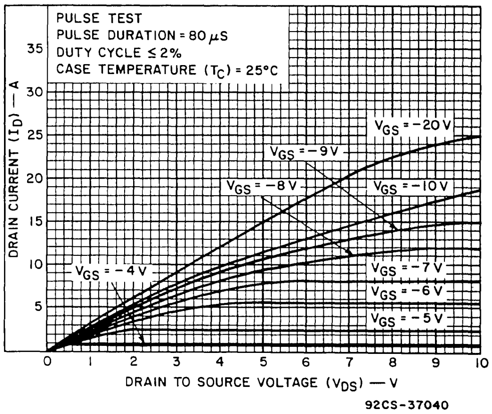


Fig. 7 — Typical saturation characteristics for all types.

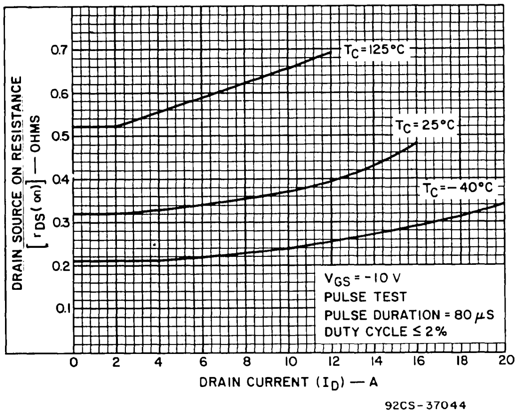


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

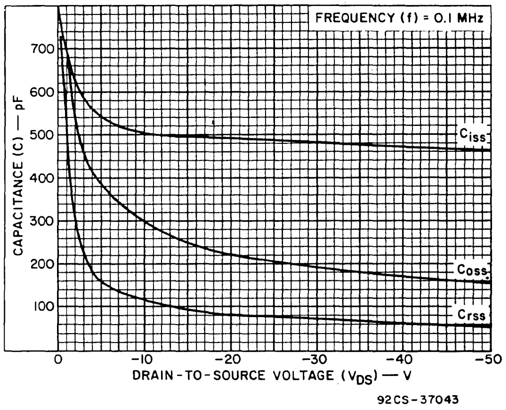


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

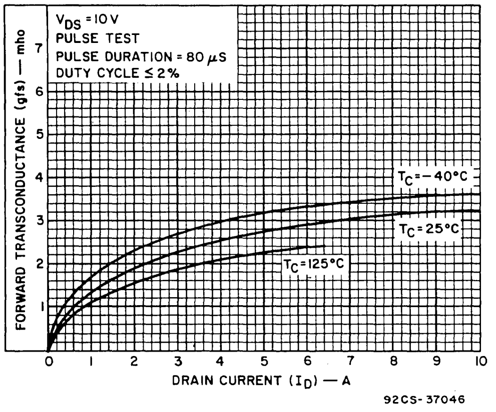


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

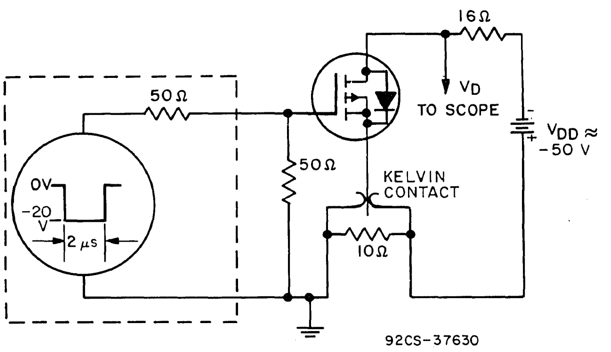
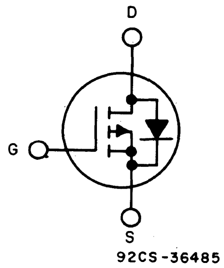


Fig. 11 - Switching Time Test Circuit.

P-Channel Enhancement-Mode Power Field-Effect Transistors

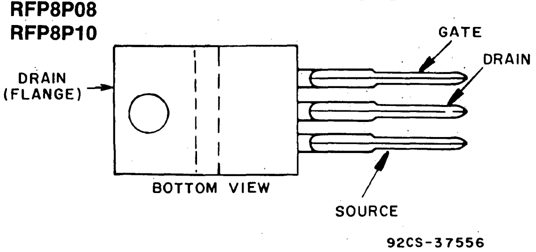
8 A, -80 V and -100 V
$r_{DS}(on) = 0.4\ \Omega$

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

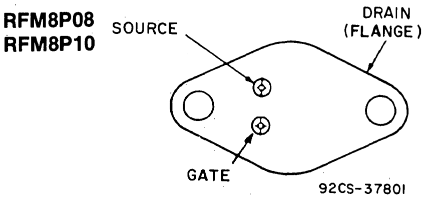


P-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATIONS



JEDEC TO-220AB



JEDEC TO-204MA

The RFM8P08 and RFM8P10 and the RFP8P08 and RFP8P10* are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204MA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

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*The RFM and RFP series were formerly RCA developmental numbers TA9410 and TA9411, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFM8P08	**RFM8P10**		**RFP8P08**	**RFP8P10**	
DRAIN-SOURCE VOLTAGE	V_{DSS}	-80	-100		-80	-100	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ)	V_{DGR}	-80	-100		-80	-100	V
GATE-SOURCE VOLTAGE	V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous	I_D			8			A
Pulsed	I_{DM}			20			A
POWER DISSIPATION @ T_C=25°C	P_T	100	100		75	75	W
Derate above T_C=25°C		0.8	0.8		0.6	0.6	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}			-55 to +150			°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8P08 RFP8P08		RFM8P10 RFP8P10		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	-100	—	V
Gate Threshold Voltage	V_{GS}(th)	V_{GS}=V_{DS} I_D=1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-65 V	—	1	—	—	µA
		V_{DS}=-80 V	—	—	—	1	
		T_C=125° C V_{DS}=-65 V	—	50	—	—	
		V_{DS}=-80 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)^a$	I_D=4 A V_{GS}=-10 V	—	-1.6	—	-1.6	V
		I_D=8 A V_{GS}=-10 V	—	-4.0	—	-4.0	
Static Drain-Source On Resistance	$r_{DS}(on)^a$	I_D=4 A V_{GS}=-10 V	—	.4	—	.4	Ω
Forward Transconductance	$g_{fs}{}^a$	V_{DS}=-10 V I_D=4 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	1500	—	1500	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	700	—	700	
Reverse Transfer Capacitance	C_{rss}	f=0.1 MHz	—	240	—	240	
Turn-On Delay Time	t_d(on)	V_{DD} = 50 V	18(typ)	60	18(typ)	60	ns
Rise Time	t_r	I_D=4 A	70(typ)	150	70(typ)	150	
Turn-Off Delay Time	t_d(off)	R_{gen}=R_{gs}=50 Ω	166(typ)	275	166(typ)	275	
Fall Time	t_f	V_{GS}=-10 V	94(typ)	175	94(typ)	175	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM8P08, RFM8P08	—	1.25	—	1.25	°C/W
		RFP8P10, RFP8P10	—	1.67	—	1.67	

[a]Pulsed: Pulse duration = 300 µs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8P08 RFP8P08		RFM8P10 RFP8P10		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 4A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/µs	200(typ.)		200(typ.)		ns

*Pulse Test: Width ≤ 300 µs, Duty Cycle ≤ 2%.

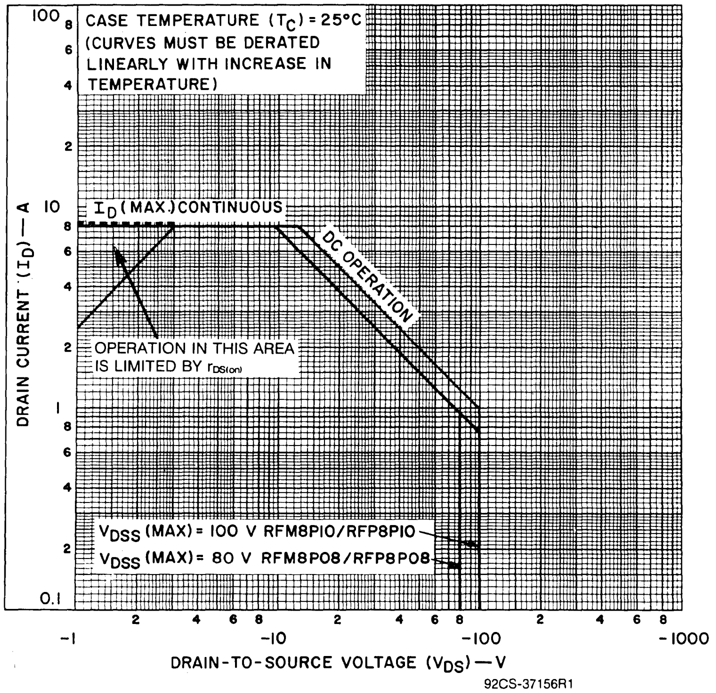


Fig. 1 — Maximum operating areas for all types.

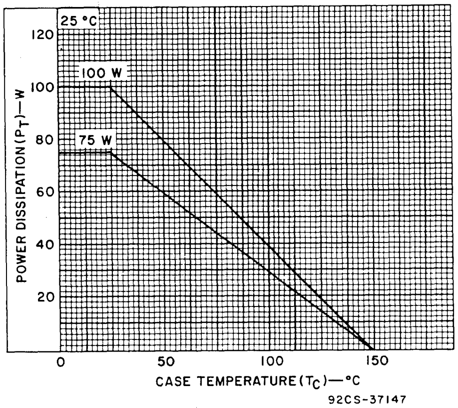


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

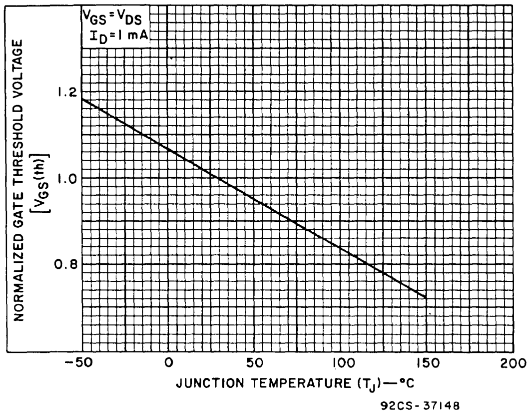


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

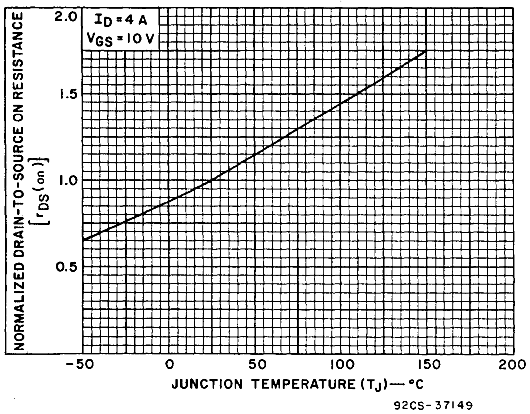


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

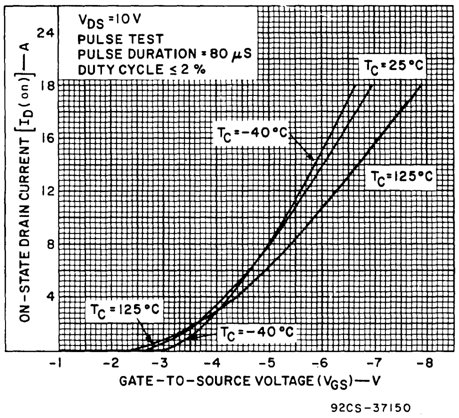


Fig. 5 — Typical transfer characteristics for all types.

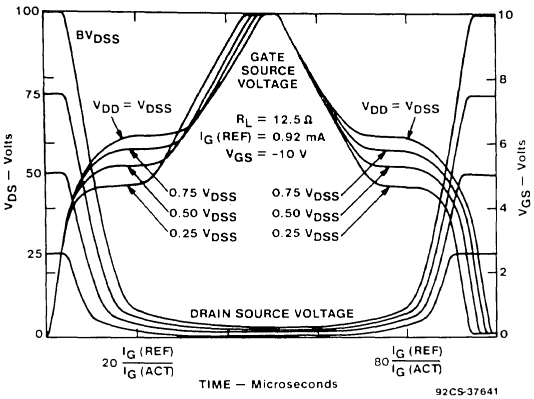


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

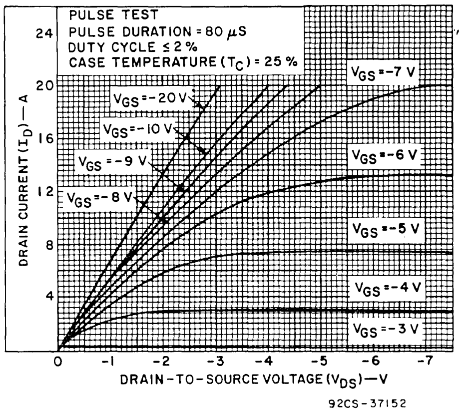


Fig. 7 — Typical saturation characteristics for all types.

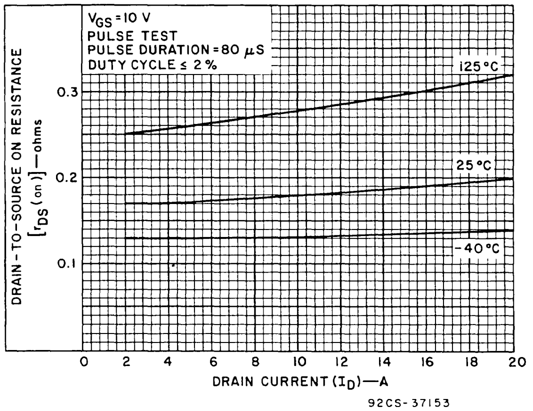


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

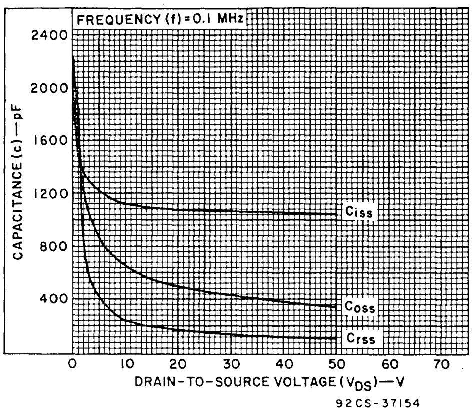


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

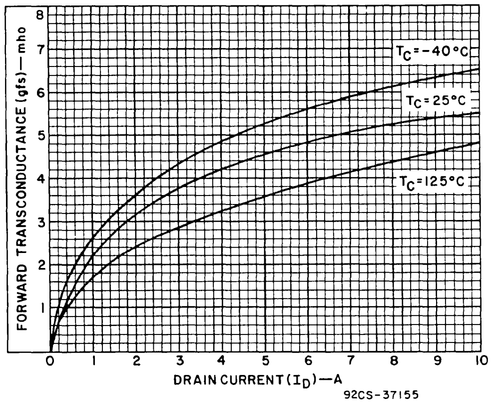


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

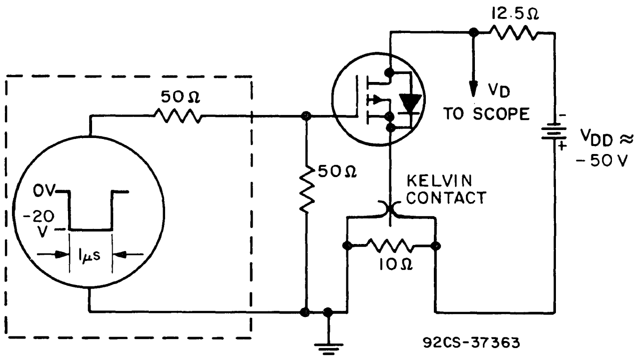


Fig. 11 — Switching Time Test Circuit.

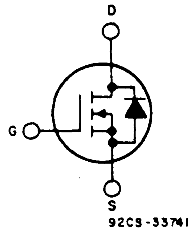
N-Channel Enhancement-Mode Power Field-Effect Transistors

8 A, 180 V — 200 V

r_{DS}(on): 0.5 Ω

Features:

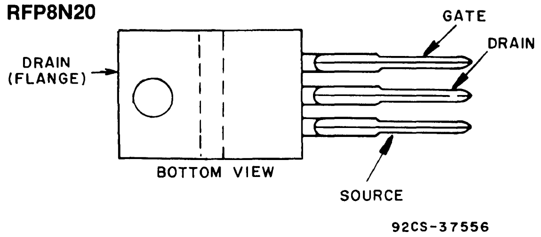
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-Channel Enhancement Mode

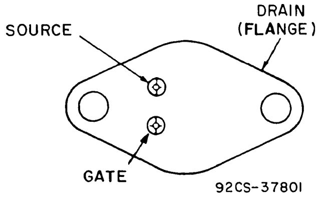
RFP8N18
RFP8N20

TERMINAL DESIGNATIONS



JEDEC TO-220AB

RFM8N18
RFM8N20



JEDEC TO-204MA

The RFM8N18 and RFM8N20 and the RFP8N18 and RFP8N20* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204MA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

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*The RFM and RFP series were formerly RCA developmental numbers TA9291 and TA9292, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25°C):*

		RFM8N18	RFM8N20	RFP8N18	RFP8N20	
DRAIN-SOURCE VOLTAGE	V_{DSS}	180	200	180	200	V
DRAIN-GATE VOLTAGE (R_{GS} = 1MΩ)	V_{DGR}	180	200	180	200	V
GATE-SOURCE VOLTAGE	V_{GS}	±20				V
DRAIN CURRENT RMS Continuous	I_D	8				A
Pulsed	I_{DM}	20				A
POWER DISSIPATION						
@ T_C = 25°C	P_T	75	75	60	60	W
Derate above T_C = 25°C		0.6	0.6	0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150				°C

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_c) = 25° C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8N18 RFP8N18		RFM8N20 RFP8N20		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 1$ mA $V_{GS} = 0$	180	—	200	—	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$ $I_D = 1$ mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 145$ V	—	1	—	—	μA
		$V_{DS} = 160$ V	—	—	—	1	
		$T_C = 125°$C					
		$V_{DS} = 145$ V	—	50	—	—	
		$V_{DS} = 160$ V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20$ V $V_{DS} = 0$	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)^a$	$I_D = 4$ A $V_{GS} = 10$ V	—	2.0	—	2.0	V
		$I_D = 8$ A $V_{GS} = 10$ V	—	5.5	—	5.5	
Static Drain-Source On Resistance	$r_{DS}(on)^a$	$I_D = 4$ A $V_{GS} = 10$ V	—	0.5	—	0.5	Ω
Forward Transconductance	g_{fs}^a	$V_{DS} = 10$ V $I_D = 4$ A	1.5	—	1.5	—	mho
Input Capacitance	C_{iss}	$V_{DS} = 25$ V	—	750	—	750	pF
Output Capacitance	C_{oss}	$V_{GS} = 0$ V	—	250	—	250	
Reverse Transfer Capacitance	C_{rss}	f = 0.1MHz	—	70	—	70	
Turn-On Delay Time	$t_d(on)$	$V_{DD} = 100$ V	30(typ.)	45	30(typ.)	45	ns
Rise Time	t_r	$I_D = 4$ A	100(typ.)	150	100(typ.)	150	
Turn-Off Delay Time	$t_d(off)$	$R_{gen} = R_{gs} = 50\ \Omega$	90(typ.)	135	90(typ.)	135	
Fall Time	t_f	$V_{GS} = 10$ V	70(typ.)	105	70(typ.)	105	
Thermal Resistance Junction-to-Case	$R\theta JC$	RFM8N18, RFM8N20	—	1.67	—	1.67	°C/W
		RFP8N18, RFP8N20	—	2.083	—	2.083	

ELECTRICAL CHARACTERISTICS (cont'd)

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8N18 RFP8N18		RFM8N20 RFP8N20		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 4A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/µs	225(typ.)		225(typ.)		ns

[a] Pulsed: Pulse duration = 300 µs max., duty cycle = 2%.

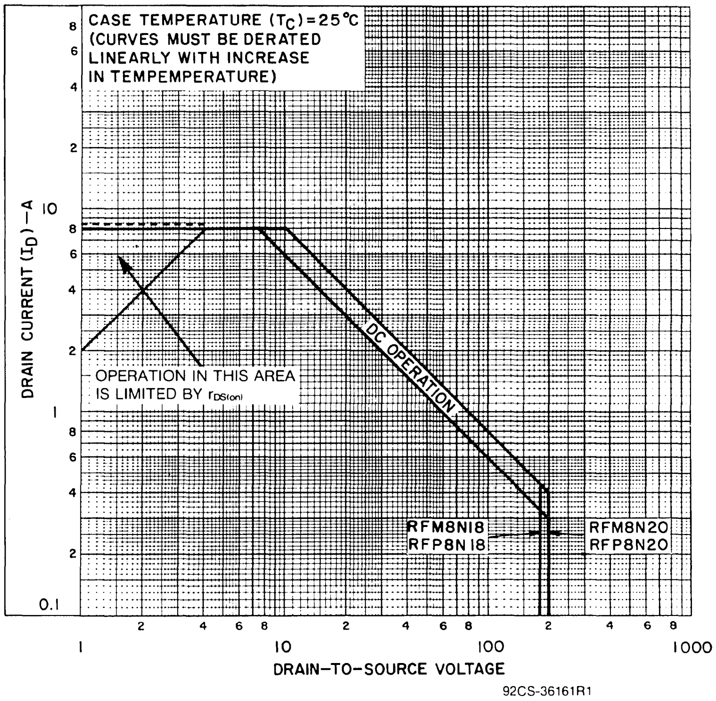


Fig. 1 — Maximum safe operating areas for all types.

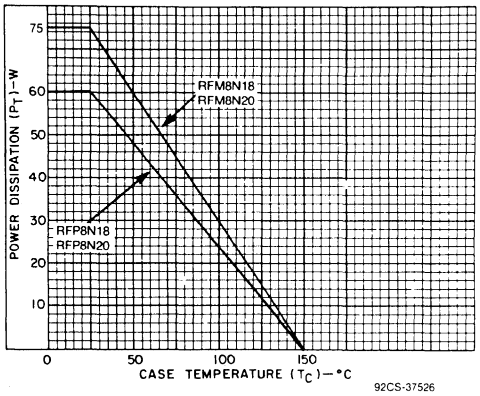


Fig. 2 — Power vs. temperature derating curve for all types.

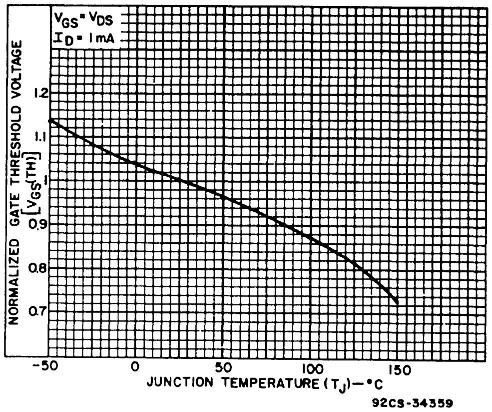


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

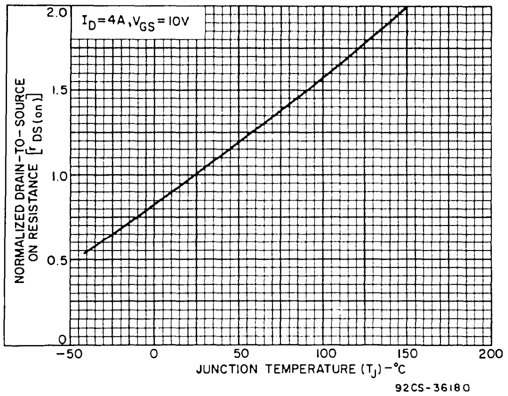


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

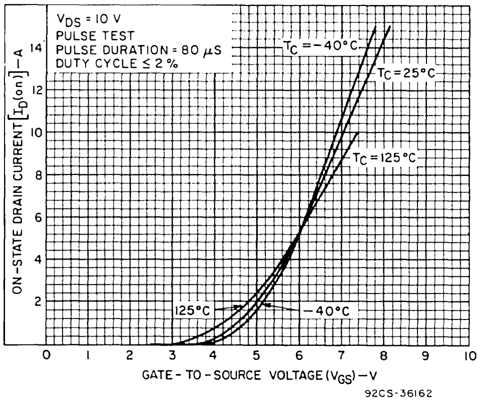


Fig. 5 — Typical transfer characteristics for all types.

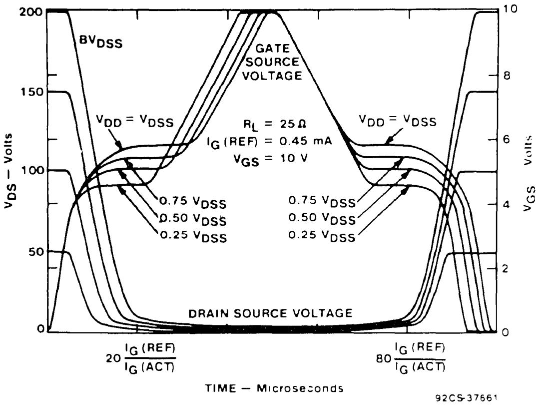


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

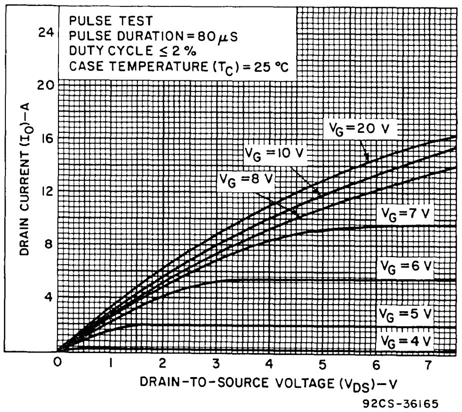


Fig. 7 — Typical saturation characteristics for all types.

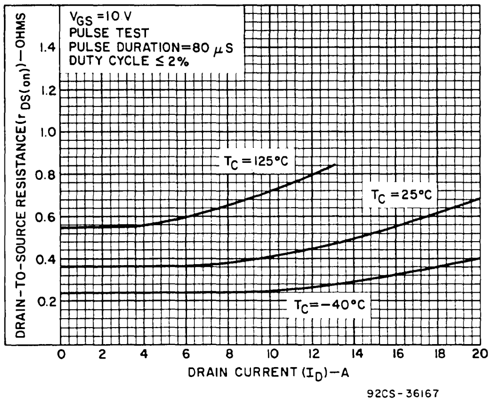


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

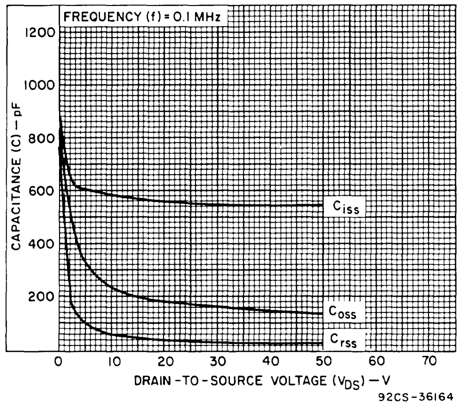


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

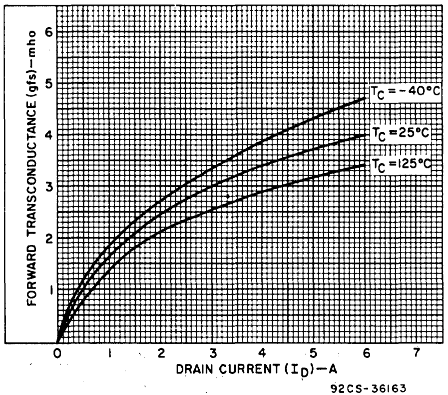


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

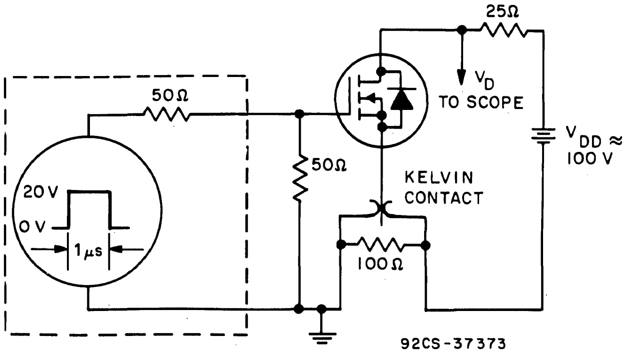
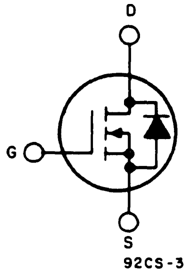


Fig. 11 — Switching Time Test Circuit.

N-Channel Enhancement-Mode Power Field-Effect Transistors

10 A, 450 V - 500 V
$r_{DS}(on) = 0.85\ \Omega$

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

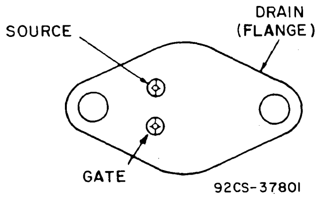


N-CHANNEL ENHANCEMENT MODE

The RFK10N45 and RFK10N50* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

TERMINAL DESIGNATIONS



JEDEC TO-204AE

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*The RFK10N45 and RFK10N50 types were formerly RCA developmental numbers TA9189A and TA9189B, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFK10N45		RFK10N50	
DRAIN-SOURCE VOLTAGE	V_{DSS}	450		500	V
DRAIN-GATE VOLTAGE, R_{gs}=1 MΩ	V_{DGR}	450		500	V
GATE-SOURCE VOLTAGE	V_{GS}		±20		V
DRAIN CURRENT, RMS Continuous	I_D		10		A
Pulsed	I_{DM}		20		A
POWER DISSIPATION @ T_C=25°C	P_T		150		W
Derate above T_C=25°C			1.2		W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}		-55 to +150		°C

RFK10N45, RFK10N50

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

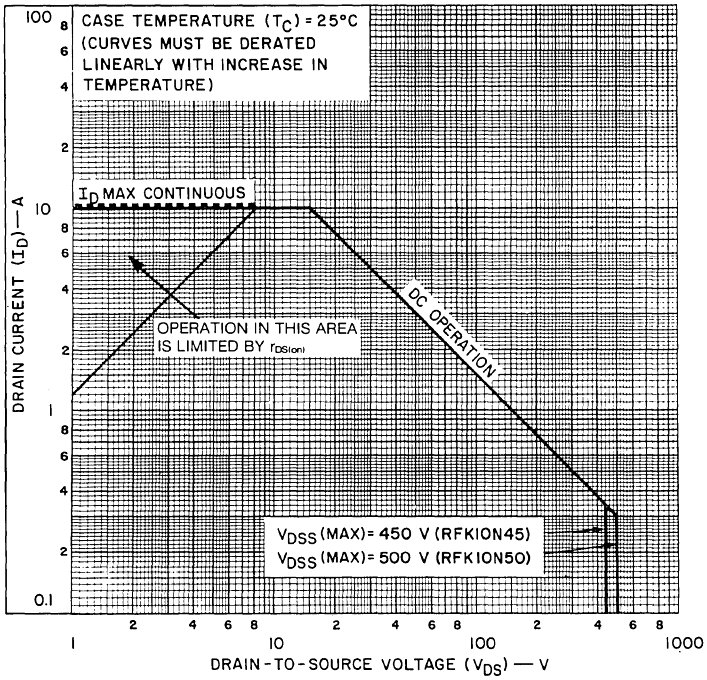
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK10N45		RFK10N50		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=1$ mA $V_{GS}=0$	450	—	500	—	V
Gate Threshold Voltage	$V_{GS}(th)$	$V_{GS}=V_{DS}$ $I_D=1$ mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=360$ V $V_{DS}=400$ V	— —	10 —	— —	— 10	μA
		$T_C=125$° C $V_{DS}=360$ V $V_{DS}=400$ V	— —	50 —	— —	— 50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm20$ V $V_{DS}=0$	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)^a$	$I_D=5$ A $V_{GS}=10$ V	—	4.25	—	4.25	V
		$I_D=10$ A $V_{GS}=10$ V	—	10	—	10	
Static Drain-Source On Resistance	$r_{DS}(on)^a$	$I_D=5$ A $V_{GS}=10$ V	—	0.85	—	0.85	Ω
Forward Transconductance	g_{fs}^a	$V_{DS}=10$ V $I_D=5$ A	5	—	5	—	mho
Input Capacitance	C_{iss}	$V_{DS}=25$ V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	$V_{GS}=0$ V	—	600	—	600	
Reverse Transfer Capacitance	C_{rss}	f=0.1 MHz	—	200	—	200	
Turn-On Delay Time	$t_d(on)$	$V_{DD}=0.5\ BV_{DSS}$	26(typ)	60	26(typ)	60	ns
Rise Time	t_r	$I_D=5$ A	50(typ)	100	50(typ)	100	
Turn-Off Delay Time	$t_d(off)$	$R_{gen}=R_{gs}=50\ \Omega$	525(typ)	900	525(typ)	900	
Fall Time	t_f	$V_{GS}=10$ V	105(typ)	180	105(typ)	180	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFK10N45, RFK10N50 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

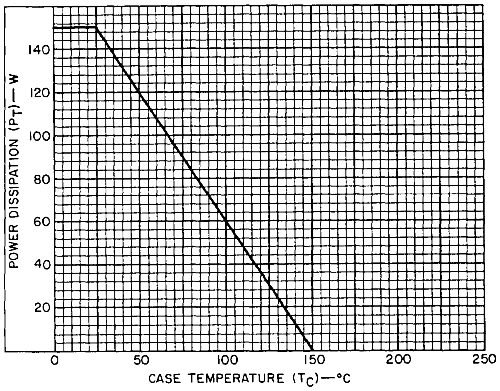
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK10N45		RFK10N50		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	950(typ.)		950(typ.)		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.



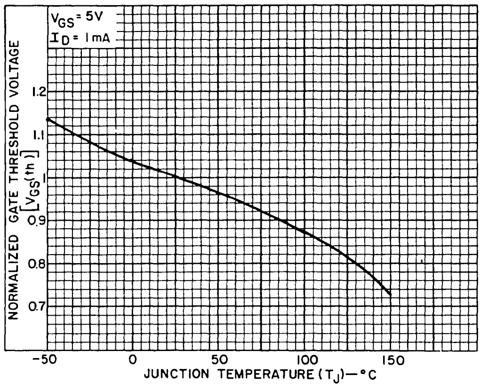
92CS-37056R1

Fig. 1 — Maximum safe operating areas for all types.



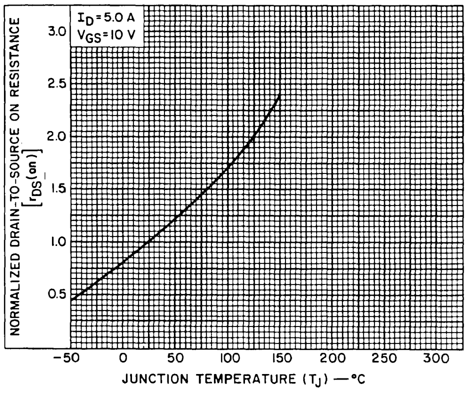
92CS-37057

Fig. 2 — Power vs. temperature derating curve for all types.



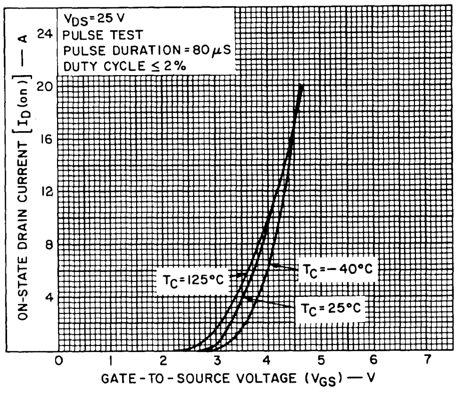
92CS-34359

Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.



92CS-37058

Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.



92CS-37059

Fig. 5 — Typical transfer characteristics for all types.

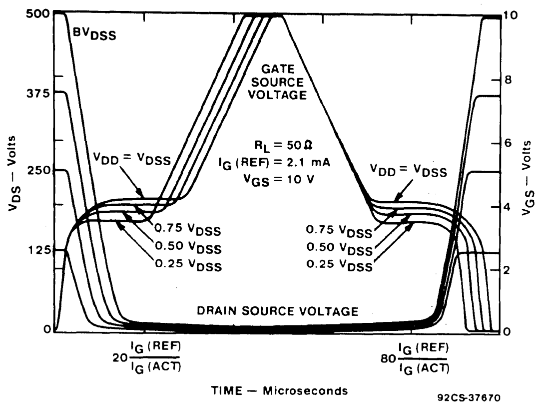


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

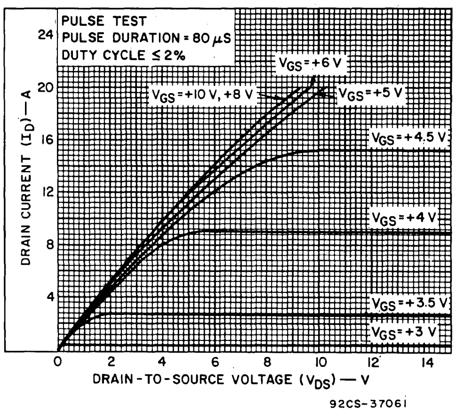


Fig. 7 — Typical saturation characteristics for all types.

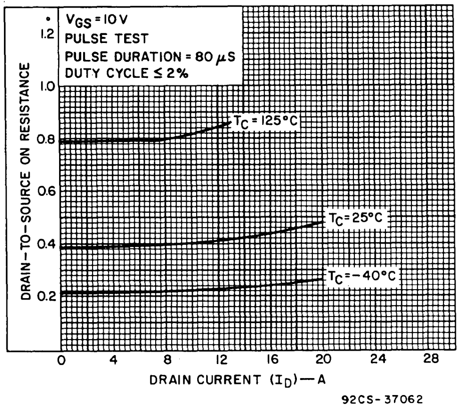


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

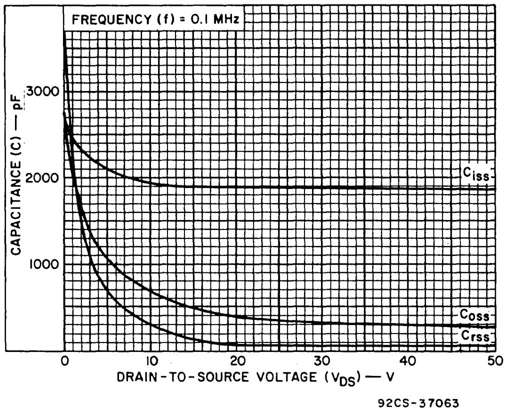


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

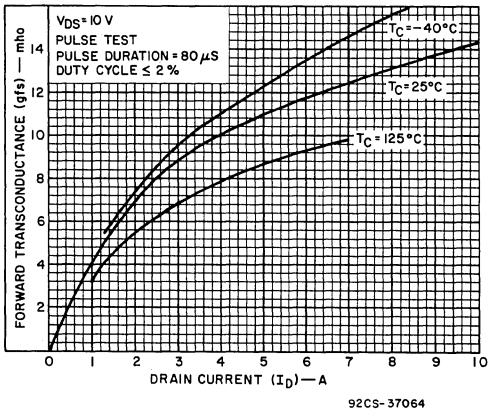


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

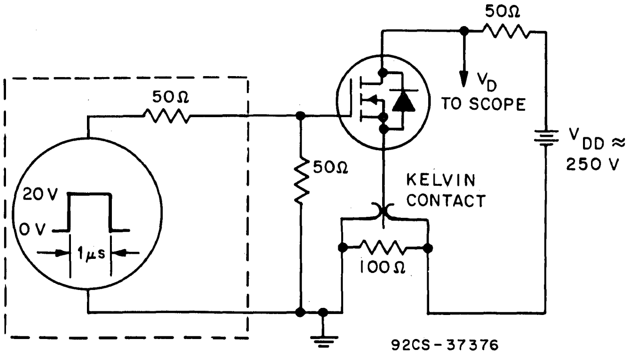


Fig. 11 - Switching Time Test Circuit.

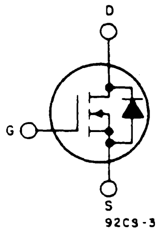
N-Channel Enhancement-Mode Power Field-Effect Transistors

10 A, 120 V — 150 V

$r_{DS}(on)$: 0.3 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-Channel Enhancement Mode

The RFM10N12 and RFM10N15 and the RFP10N12 and RFP10N15* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204MA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

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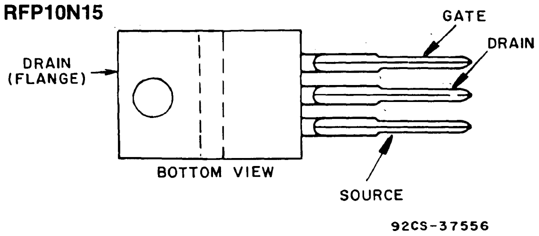
*The RFM and RFP series were formerly RCA developmental numbers TA9192 and TA9212, respectively.

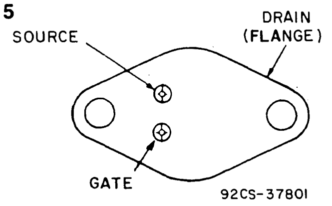
TERMINAL DESIGNATIONS

RFP10N12
RFP10N15



JEDEC TO-220AB

RFM10N12
RFM10N15



JEDEC TO-204MA

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C=25° C):

		RFM10N12	RFM10N15		RFP10N12	RFP10N15	
DRAIN-SOURCE VOLTAGE	V_{DSS}	120	150		120	150	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ)	V_{DGR}	120	150		120	150	V
GATE-SOURCE VOLTAGE	V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous	I_D			10			A
Pulsed	I_{DM}			25			A
POWER DISSIPATION @ T_C=25°C	P_T	75	75		60	60	W
Derate above T_C=25°C		0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}			-55 to +150			°C

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_c) = 25° C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10N12 RFP10N12		RFM10N15 RFP10N15		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 1$ mA $V_{GS} = 0$	120	—	150	—	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$ $I_D = 2$ mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100$ V	—	1	—	—	μA
		$V_{DS} = 120$ V	—	—	—	1	
		$T_C = 125°$C					
		$V_{DS} = 100$ V	—	50	—	—	
		$V_{DS} = 120$ V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20$ V $V_{DS} = 0$	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	$I_D = 5$ A $V_{GS} = 10$ V	—	1.5	—	1.5	V
		$I_D = 10$ A $V_{GS} = 10$ V	—	4	—	4	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	$I_D = 5$ A $V_{GS} = 10$ V	—	0.3	—	0.3	Ω
Forward Transconductance	g_{fs}[a]	$V_{DS} = 10$ V $I_D = 5$ A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	650	—	650	pF
Output Capacitance	C_{oss}	$V_{GS} = 0$ V	—	230	—	230	
Reverse Transfer Capacitance	C_{rss}	f=0.1 MHz	—	60	—	60	
Turn-On Delay Time	$t_d(on)$	V_{DD}=75 V	40(typ.)	60	40(typ.)	60	ns
Rise Time	t_r	$I_D = 5$ A	165(typ.)	250	165(typ.)	250	
Turn-Off Delay Time	$t_d(off)$	$R_{gen} = R_{gs} = 50$ Ω	90(typ.)	135	90(typ.)	135	
Fall Time	t_f	$V_{GS} = 10$ V	90(typ.)	135	90(typ.)	135	
Thermal Resistance Junction-to-Case	RθJC	RFM10N12, RFM10N15	—	1.67	—	1.67	°C/W
		RFP10N12, RFP10N15	—	2.083	—	2.083	

[a] Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

ELECTRICAL CHARACTERISTICS (cont'd)

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10N12 RFP10N12		RFM10N15 RFP10N15		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD}=5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

[a] Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

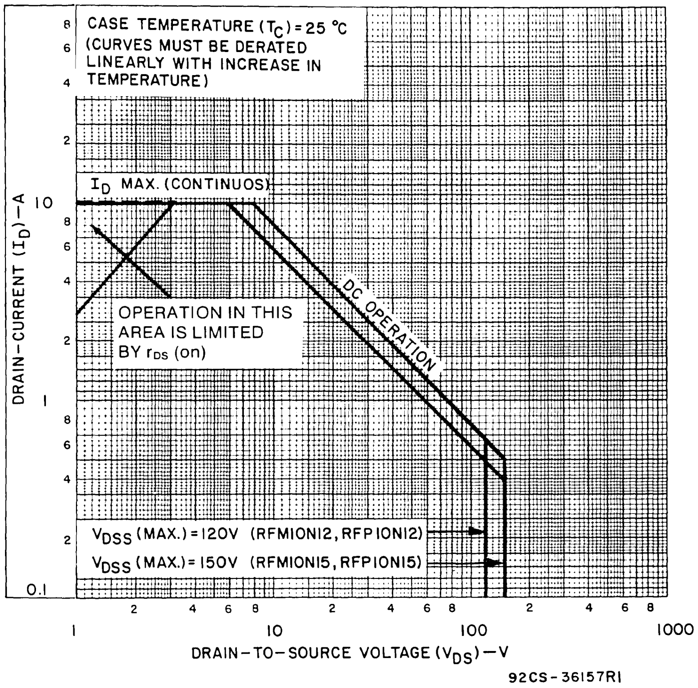


Fig. 1 — Maximum safe operating areas for all types.

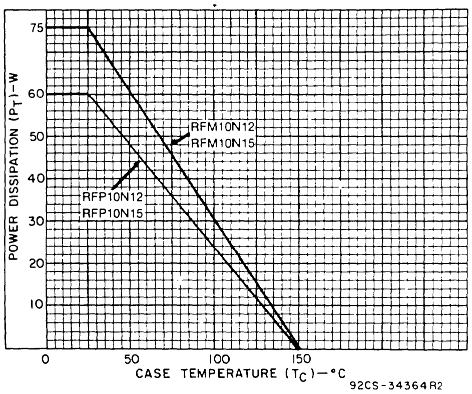


Fig. 2 — Power vs. temperature derating curve for all types.

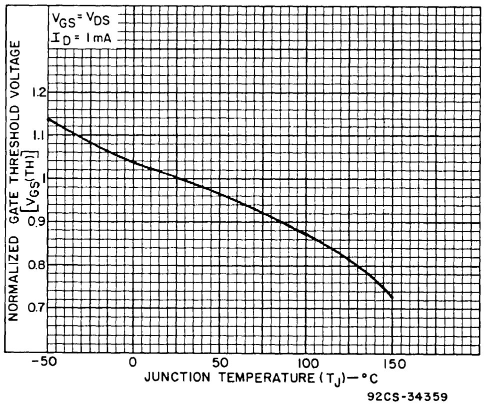


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

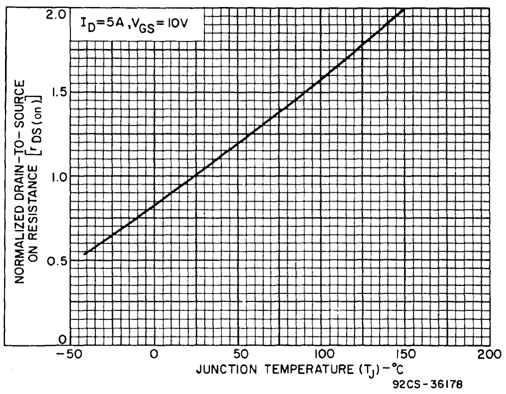


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

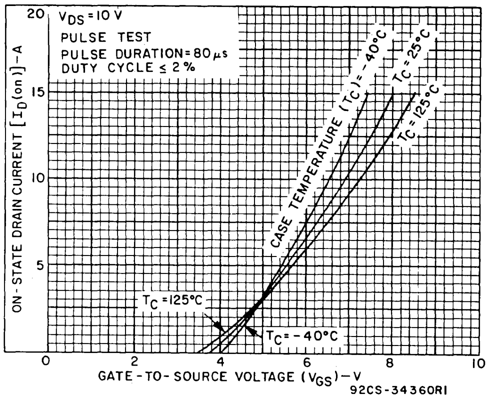


Fig. 5 — Typical transfer characteristics for all types.

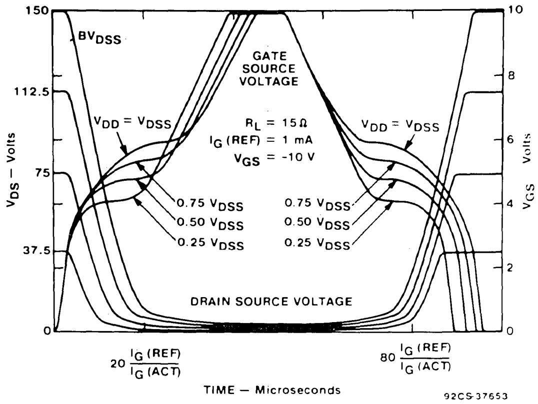


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

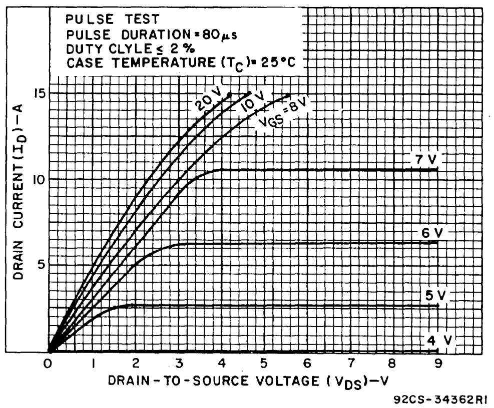


Fig. 7 — Typical saturation characteristics for all types.

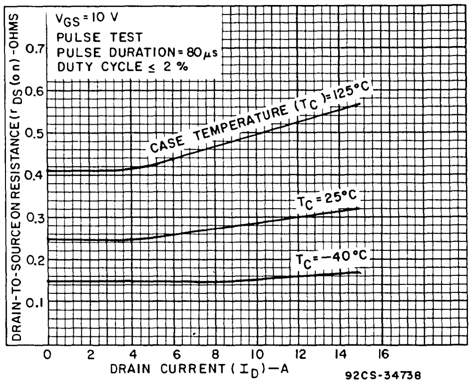


Fig. 8 - Typical drain-to-source on resistance as a function drain current for all types.

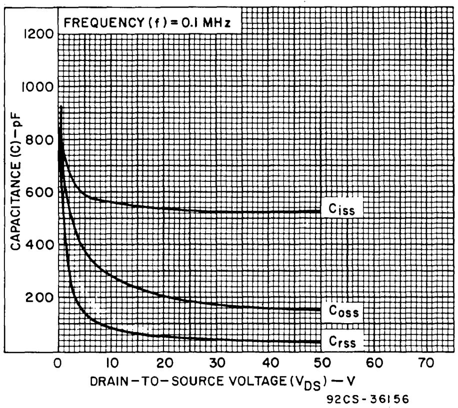


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

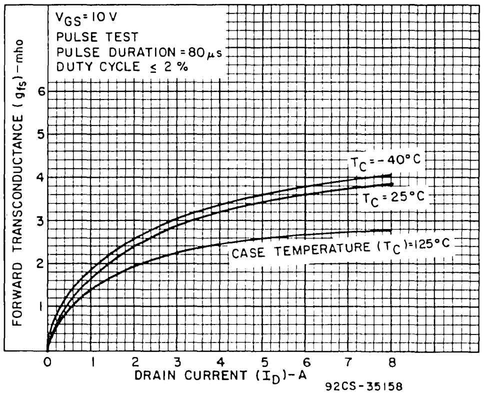


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

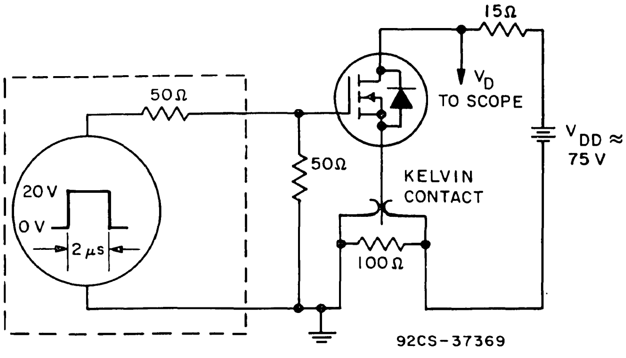


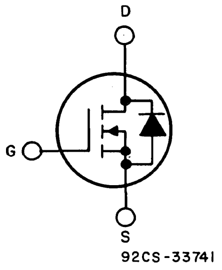
Fig. 11 — Switching Time Test Circuit

N-Channel Enhancement-Mode Power Field-Effect Transistors

12 A, 80 and 100 V

$r_{DS(on)}$: 0.2 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

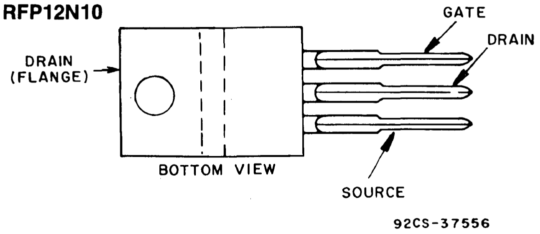
The RFM12N08 and RFM12N10 and the RFP12N08 and RFP12N10 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-series types are supplied in the JEDEC TO-204MA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFM and RFP series were formerly RCA developmental numbers TA9284 and TA9285.

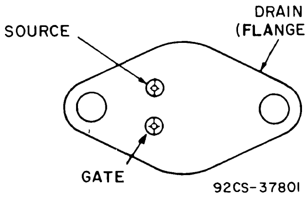
TERMINAL DESIGNATIONS

RFP12N08
RFP12N10



JEDEC TO-220AB

RFM12N08
RFM12N10



JEDEC TO-204MA

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFM12N08	RFM12N10		RFP12N08	RFP12N10	
DRAIN-SOURCE VOLTAGE	V_{DSS}	80	100		80	100	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ)	V_{DGR}	80	100		80	100	V
GATE-SOURCE VOLTAGE	V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous	I_D			12			A
Pulsed	I_{DM}			30			A
POWER DISSIPATION @ T_C=25°C	P_T	75	75		60	60	W
Derate above T_C=25°C		0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}			-55 to +150			°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N08 RFP12N08		RFM12N10 RFP12N10		
			Min.	Max.	Min.	Max.	
Drain Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	100	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V	—	1	—	—	µA
		V_{DS}=80 V	—	—	—	1	
		T_C=125° C V_{DS}=65 V	—	50	—	—	
		V_{DS}=80 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=6 A V_{GS}=10 V	—	1.2	—	1.2	V
		I_D=12 A V_{GS}=10 V	—	3.3	—	3.3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=6 A V_{GS}=10 V	—	0.2	—	0.2	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=6 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f=0.1 MHz	—	650	—	650	pF
Output Capacitance	C_{oss}		—	300	—	300	
Reverse-Transfer Capacitance	C_{rss}		—	100	—	100	
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V I_D=6 A R_{gen}=R_{gs}=50 Ω V_{GS}=10 V	45(Typ)	70	45(Typ)	70	ns
Rise Time	t_r		250(Typ)	375	250(Typ)	375	
Turn-Off Delay Time	$t_d(off)$		85(Typ)	130	85(Typ)	130	
Fall Time	t_f		100(Typ)	150	100(Typ)	150	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM12N08, RFM12N10	—	1.67	—	1.67	°C/W
		RFP12N08, RFP12N10	—	2.083	—	2.083	

[a] Pulsed: Pulse duration=300 µs max., duty cycle=2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N08 RFM12N10		RFP12N08 RFP12N10		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/µs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 µs, duty cycle ≤ 2%.

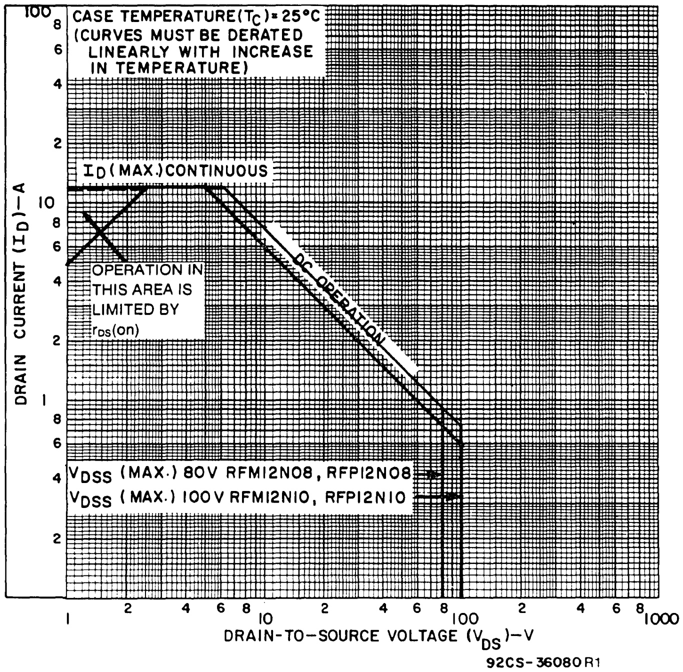


Fig. 1 - Maximum operating areas for all types.

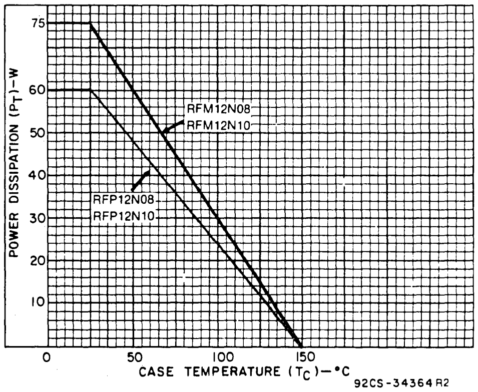


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

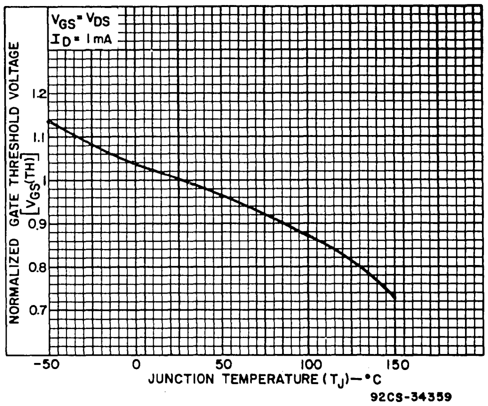


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

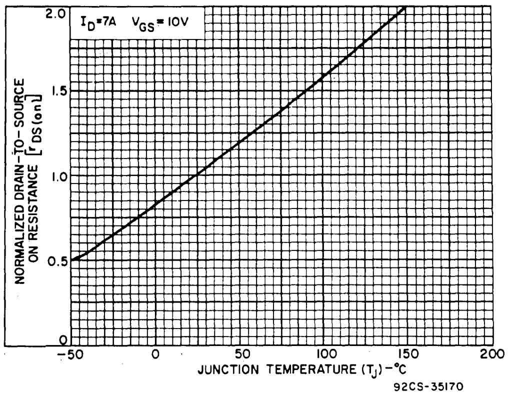


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

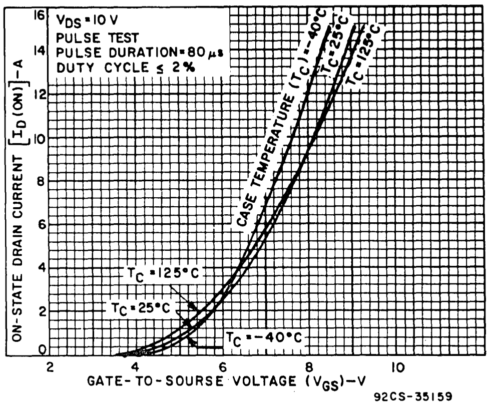


Fig. 5 - Typical transfer characteristics for all types.

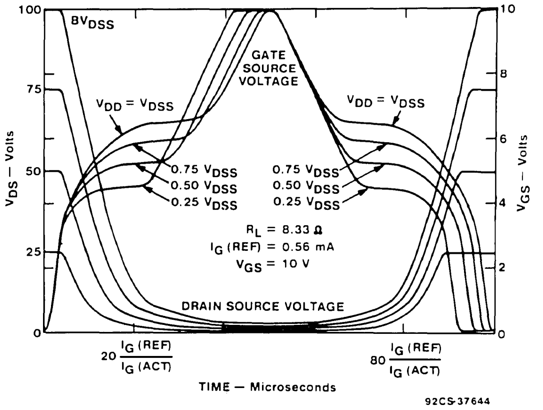


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

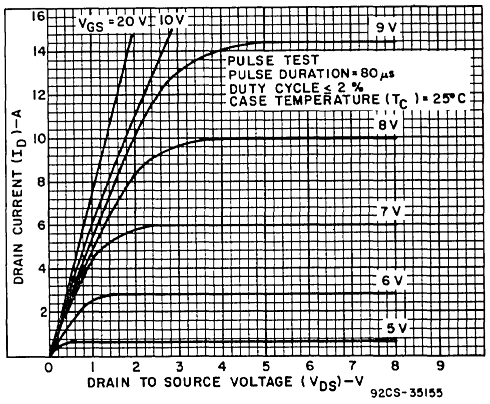


Fig. 7 - Typical saturation characteristics for all types.

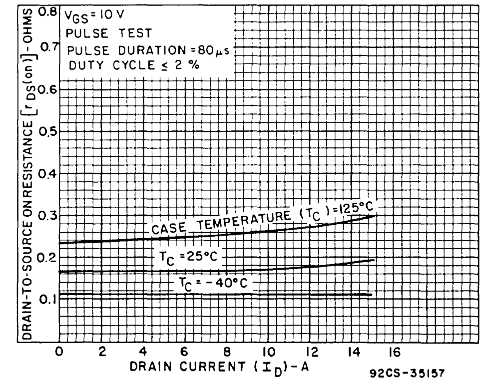


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

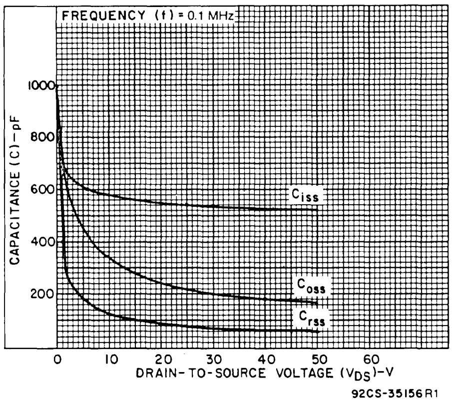


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

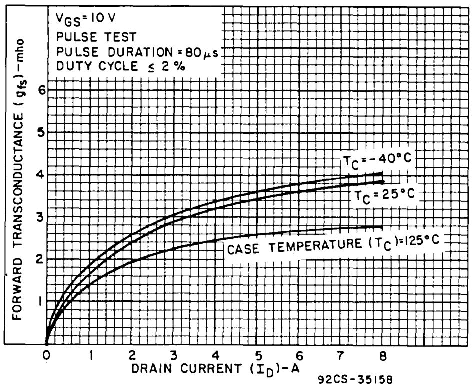


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

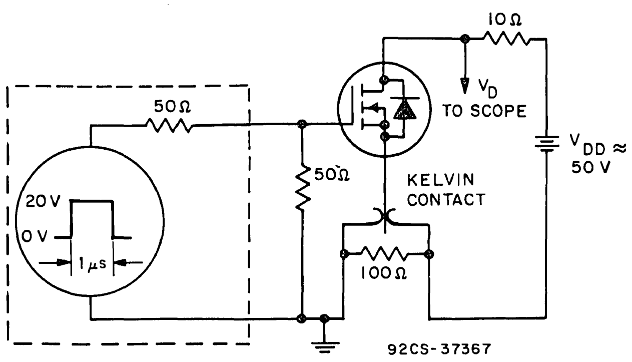


Fig. 11 — Switching Time Test Circuit

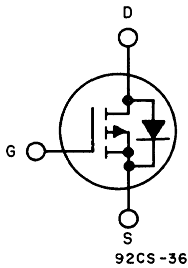
P-Channel Enhancement-Mode Power Field-Effect Transistors

12 A, -80 V and -100 V
r_{DS}(on) = 0.3 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The RFM12P08 and RFM12P10 and the RFP12P08 and RFP12P10* are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

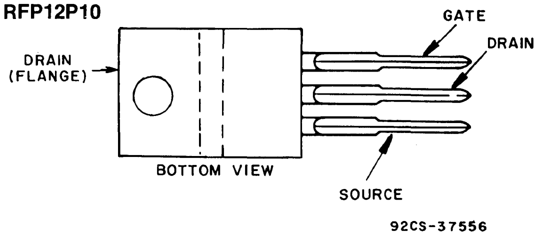
The RFM-types are supplied in the JEDEC TO-204MA steel package and the RFP-types in the JEDEC TO-220AB plastic package.



P-CHANNEL ENHANCEMENT MODE

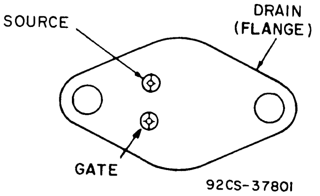
TERMINAL DESIGNATIONS

RFP12P08
RFP12P10



JEDEC TO-220AB

RFM12P08
RFM12P10



JEDEC TO-204MA

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFM12P08	**RFM12P10**		**RFP12P08**	**RFP12P10**	
DRAIN-SOURCE VOLTAGE	V_{DSS}	-80	-100		-80	-100	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ)	V_{DGR}	-80	-100		-80	-100	V
GATE-SOURCE VOLTAGE	V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous	I_D			12			A
Pulsed	I_{DM}			30			A
POWER DISSIPATION @ T_C=25° C	P_T	100	100		75	75	W
Derate above T_C=25° C		0.8	0.8		0.6	0.6	W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}			-55 to +150			° C

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*The RFM and RFP series were formerly RCA developmental numbers TA9410 and TA9411, respectively.

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

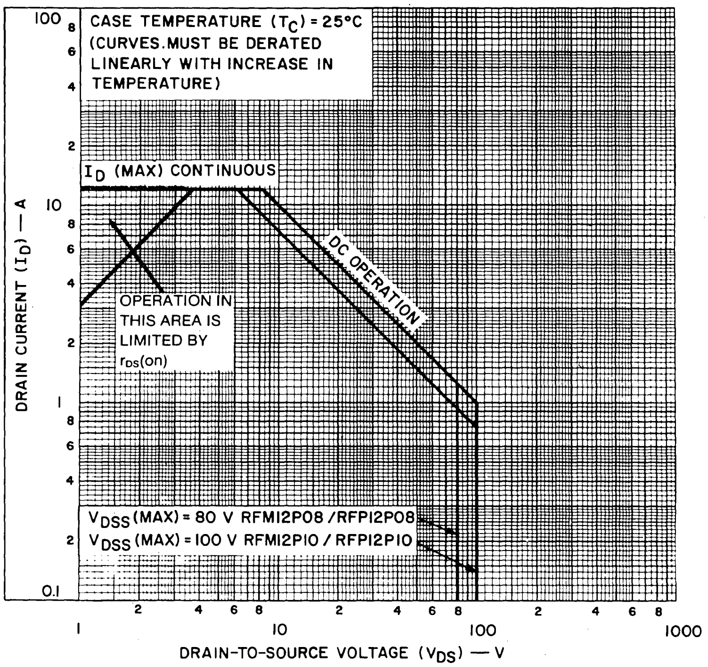
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12P08 RFP12P08		RFM12P10 RFP12P10		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	-100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-65 V	—	1	—	—	µA
		V_{DS}=-80 V	—	—	—	1	
		T_C=125° C V_{DS}=-65 V	—	50	—	—	
		V_{DS}=-80 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)^a$	I_D=6 A V_{GS}=-10 V	—	-1.8	—	-1.8	V
		I_D=12 A V_{GS}=-10 V	—	-4.8	—	-4.8	
Static Drain-Source On Resistance	$r_{DS}(on)^a$	I_D=6 A V_{GS}=-10 V	—	.3	—	.3	Ω
Forward Transconductance	g_{fs}^a	V_{DS}=-10 V I_D=6 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=-25 V	—	1500	—	1500	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	700	—	700	
Reverse Transfer Capacitance	C_{rss}	f=0.1 MHz	—	240	—	240	
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V	18(typ)	60	18(typ)	60	ns
Rise Time	t_r	I_D=6 A	90(typ)	175	90(typ)	175	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	144(typ)	275	144(typ)	275	
Fall Time	t_f	V_{GS}=-10 V	94(typ)	175	94(typ)	175	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM12P08, RFM12P10	—	1.25	—	1.25	°C/W
		RFP12P08, RFP12P10	—	1.67	—	1.67	

[a] Pulsed: Pulse duration = 300 µs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

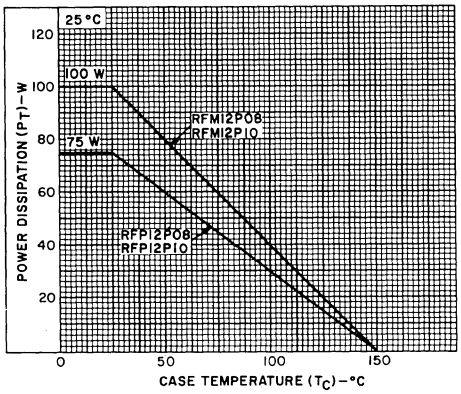
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12P08 RFP12P08		RFM12P10 RFP12P10		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/µs	200(typ)		200(typ)		ns

*Pulse Test: Width ≤ 300 µs, duty cycle ≤ 2%.



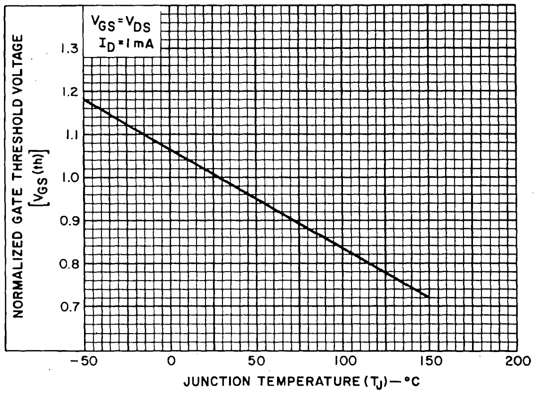
92CS-37106 R1

Fig. 1 — Maximum safe operating areas for all types.



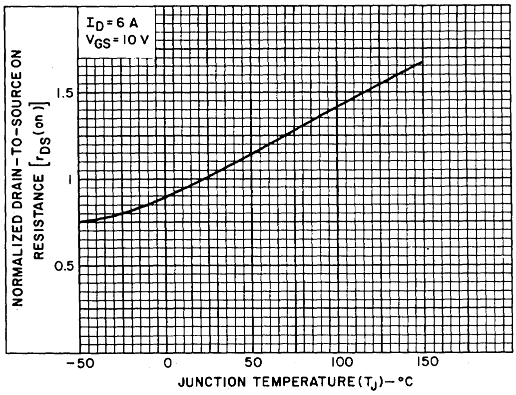
92CS-37107

Fig. 2 — Power dissipation vs. case temperature derating curve for all types.



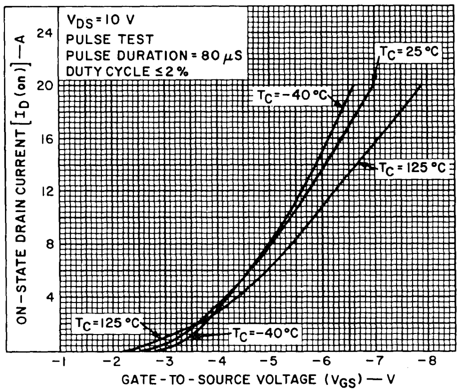
92CS-37115

Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.



92CS-37108

Fig. 4 — Normalized drain-to-source on resistance as a function of junction temperature for all types.



92CS-37114

Fig. 5 — Typical transfer characteristics for all types.

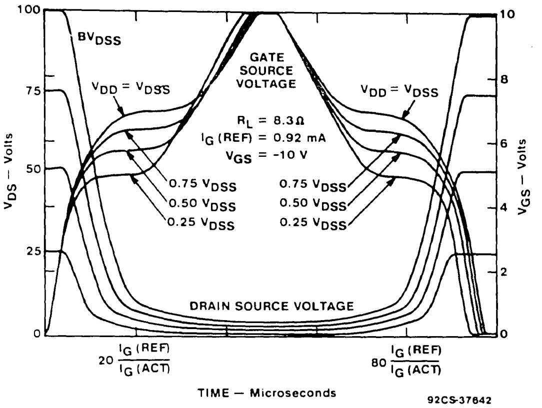


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

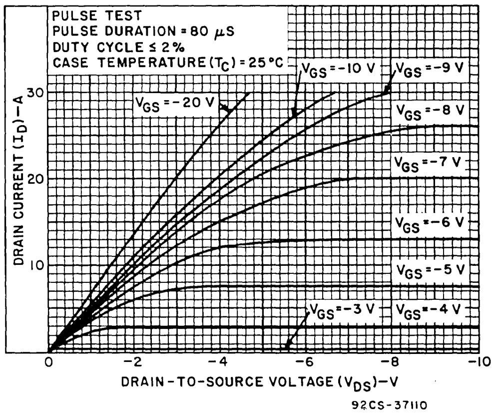


Fig. 7 — Typical saturation characteristics for all types.

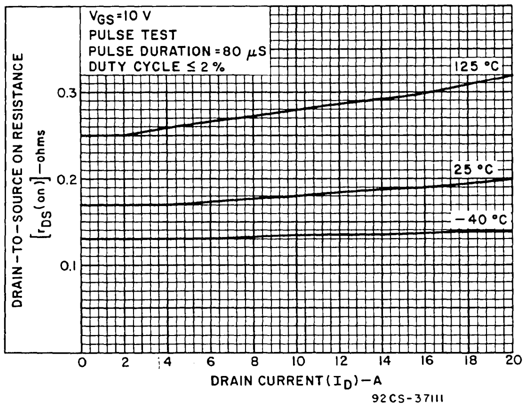


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

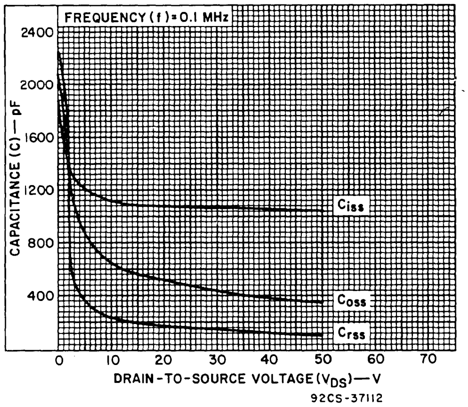


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

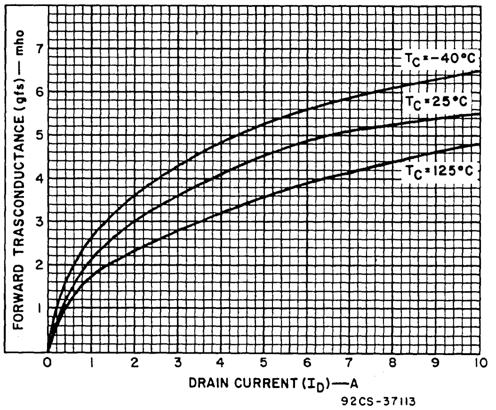


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

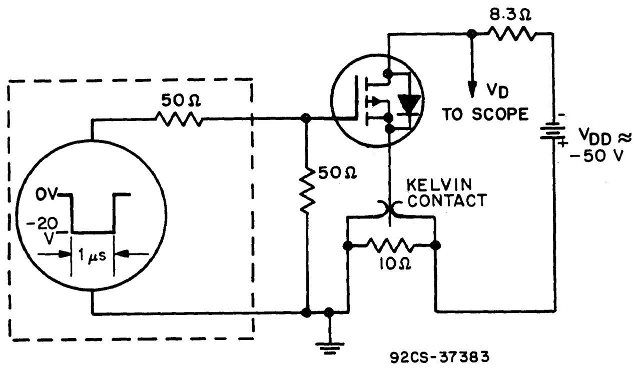
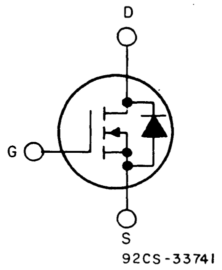


Fig. 11 — Switching Time Test Circuit

N-Channel Enhancement-Mode Power Field-Effect Transistors

12 A, 180 and 200 V
$r_{DS}(on)$: 0.25 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



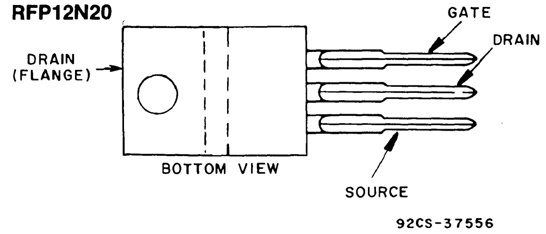
N-CHANNEL ENHANCEMENT MODE

The RFM12N18 and RFM12N20 and the RFP12N18 and RFP12N20* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204MA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

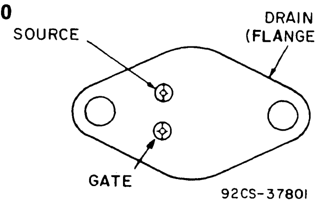
TERMINAL DESIGNATIONS

RFP12N18
RFP12N20



JEDEC TO-220AB

RFM12N18
RFM12N20



JEDEC TO-204MA

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM12N18	RFM12N20		RFP12N18	RFP12N20	
DRAIN-SOURCE VOLTAGE .... V_{DSS}	180	200		180	200	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ) .. V_{DGR}	180	200		180	200	V
GATE-SOURCE VOLTAGE .... V_{GS}			±20			V
DRAIN CURRENT						
RMS Continuous...................... I_D			12			A
Pulsed .... I_{DM}			30			A
POWER DISSIPATION						
@ T_C=25° C .... P_T	100	100		75	75	W
Derate above T_C=25° C	0.8	0.8		0.6	0.6	W/° C
OPERATING AND STORAGE						
TEMPERATURE ....T_j, T_{stg}			-55 to +150			° C

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*The RFM and RFP series were formerly RCA developmental numbers TA9293 and TA9294, respectively.

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N18 RFP12N18		RFM12N20 RFP12N20		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	180	—	200	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V	—	1	—	—	μA
		V_{DS}=160 V	—	—	—	1	
		T_C=125° C V_{DS}=145 V	—	50	—	—	
		V_{DS}=160 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=6 A V_{GS}=10 V	—	1.5	—	1.5	V
		I_D=12 A V_{GS}=10 V	—	3.6	—	3.6	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=6 A V_{GS}=10 V	—	0.25	—	0.25	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=6 A	4	—	4	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f=1 MHz	—	1250	—	1250	pF
Output Capacitance	C_{oss}		—	425	—	425	
Reverse-Transfer Capacitance	C_{rss}		—	125	—	125	
Turn-On Delay Time	$t_d(on)$	V_{DD}=100 V I_D=6 A R_{gen}=R_{gs}=50 Ω V_{GS}=10 V	35(typ)	50	35(typ)	50	ns
Rise Time	t_r		130(typ)	200	130(typ)	200	
Turn-Off Delay Time	$t_d(off)$		120(typ)	180	120(typ)	180	
Fall Time	t_f		105(typ)	160	105(typ)	160	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM12N18, RFM12N20	—	1.25	—	1.25	°C/W
		RFP12N18, RFP12N20	—	1.67	—	1.67	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N18 RFP12N18		RFM12N20 RFP12N20		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD}=6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	325(typ)		325(typ)		ns

[a] Pulsed: Pulse duration=300 μs max., duty cycle=2%.

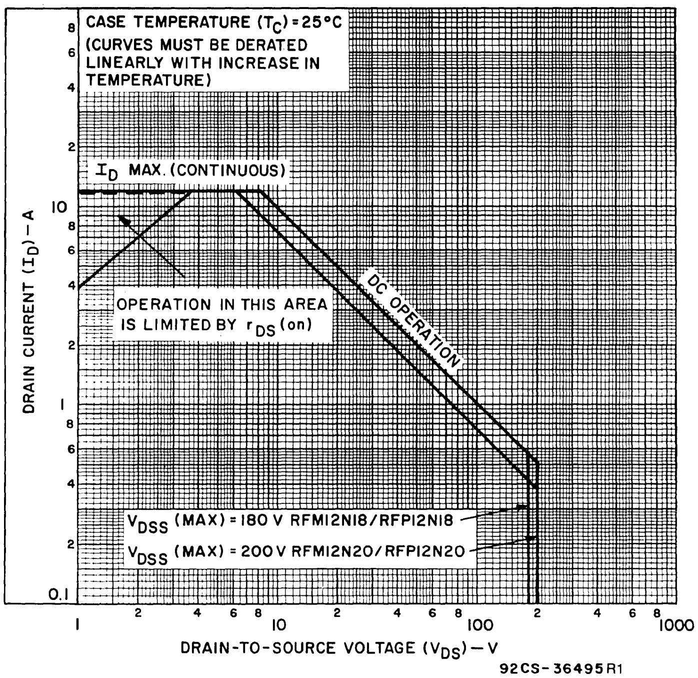


Fig. 1 - Maximum safe operating areas for all types.

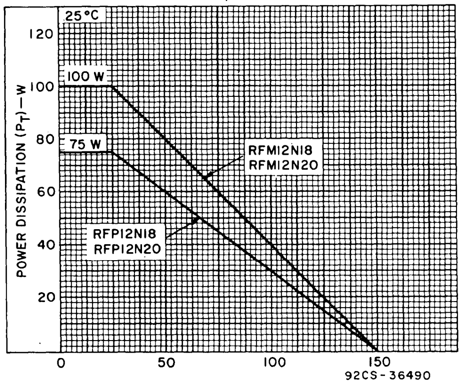


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

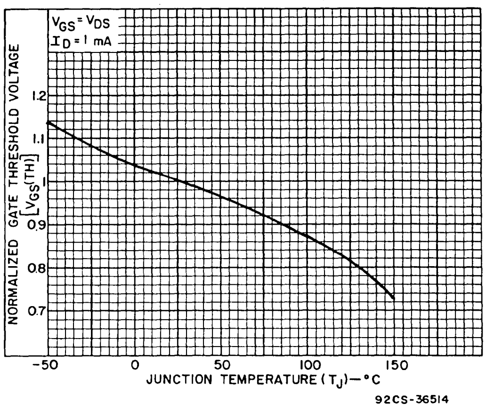


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

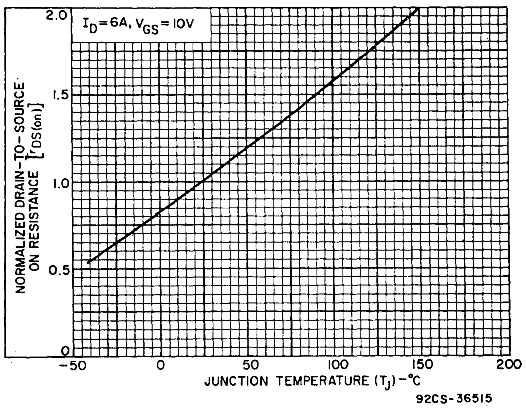


Fig. 4 - Normalized drain-to-source on resistance as a function of junction temperature for all types.

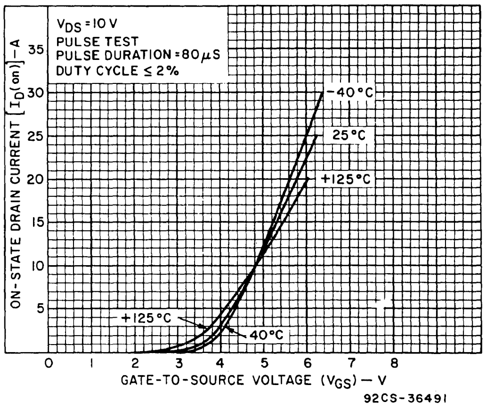


Fig. 5 - Typical transfer characteristics for all types.

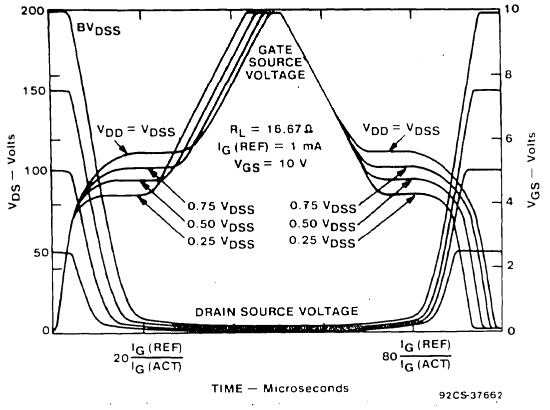


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

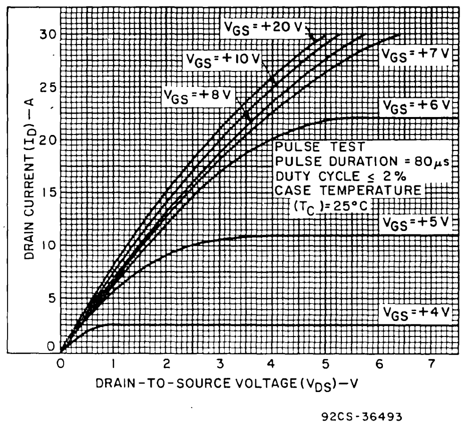


Fig. 7 - Typical saturation characteristics for all types.

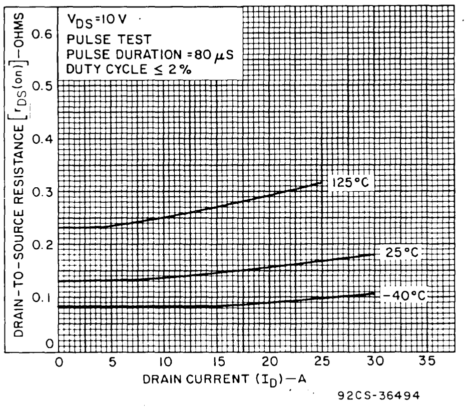


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

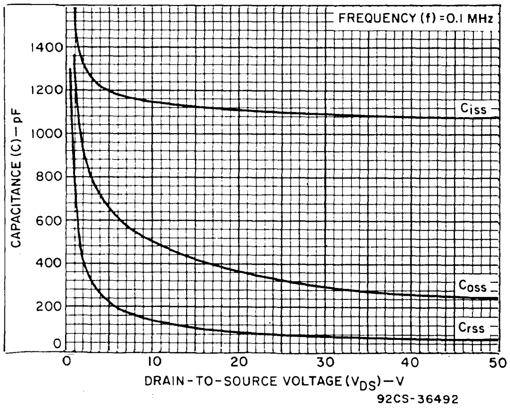


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

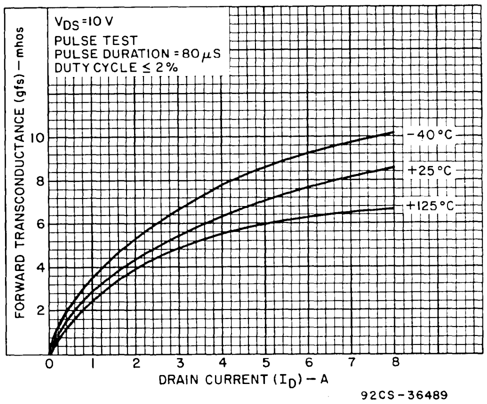


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

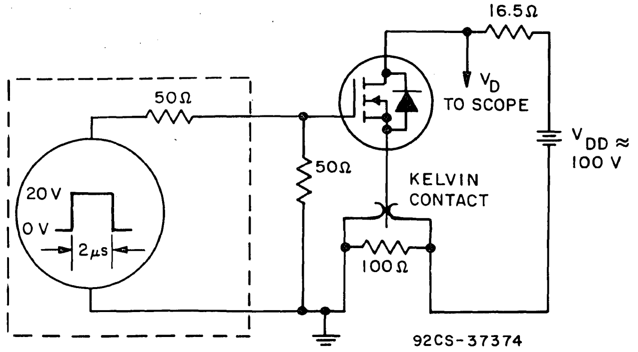


Fig. 11 — Switching Time Test Circuit

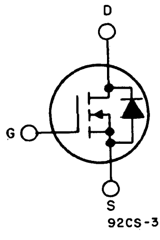
N-Channel Enhancement-Mode Power Field-Effect Transistors

15 A, 50 and 60 V
r_{DS}(on): 0.15 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The RFM15N05 and RFM15N06 and the RFP15N05 and RFP15N06* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

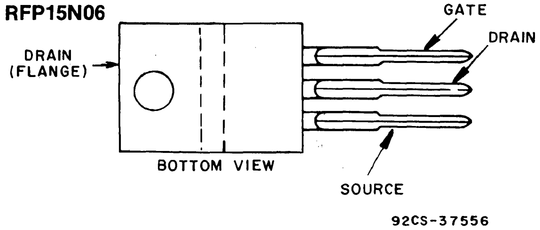
The RFM-series types are supplied in the JEDEC TO-204MA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.



N-CHANNEL ENHANCEMENT MODE

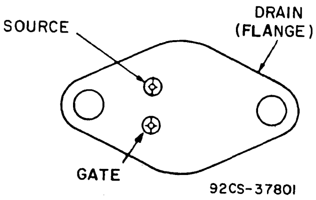
TERMINAL DESIGNATIONS

RFP15N05
RFP15N06



JEDEC TO-220AB

RFM15N05
RFM15N06



JEDEC TO-204MA

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM15N05	RFM15N06		RFP15N05	RFP15N06	
DRAIN-SOURCE VOLTAGE .... V_{DSS}	50	60		50	60	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) ... V_{DGR}	50	60		50	60	V
GATE-SOURCE VOLTAGE .... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			15			A
Pulsed .... I_{DM}			40			A
POWER DISSIPATION @ T_C=25°C .... P_T	75	75		60	60	W
Derate above T_C=25°C	0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE .... T_j, T_{stg}			-55 to +150			°C

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*The RFM and RFP series were formerly RCA developmental numbers TA9382 and TA9383, respectively.

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25° C unless otherwise specified*

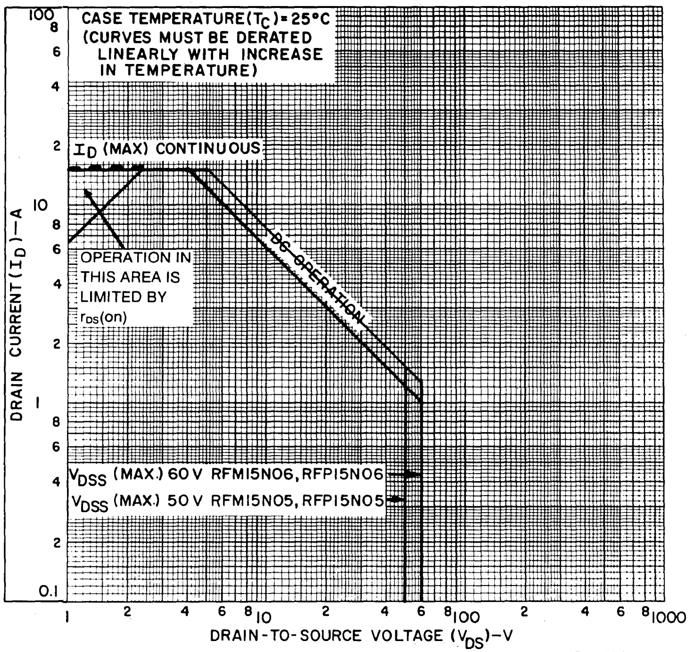
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N05 RFP15N05		RFM15N06 RFP15N06		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	60	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=40 V	—	1	—	—	µA
		V_{DS}=50 V	—	—	—	1	
		T_C=125° C					
		V_{DS}=40 V	—	50	—	—	
		V_{DS}=50 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)^a$	I_D=7.5 A V_{GS}=10 V	—	1.125	—	1.125	V
		I_D=15 A V_{GS}=10 V	—	2.5	—	2.5	
Static Drain-Source On Resistance	$r_{DS}(on)^a$	I_D=7.5 A V_{GS}=10 V	—	0.15	—	0.15	Ω
Forward Transconductance	g_{fs}^a	V_{DS}=10 V I_D=7.5 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	750	—	750	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	450	—	450	
Reverse-Transfer Capacitance	C_{rss}	f=0.1 MHz	—	180	—	180	
Turn-On Delay Time	$t_d(on)$	V_{DD}=30 V	16(typ)	40	16(typ)	40	ns
Rise Time	t_r	I_D=7.5 A	100(typ)	175	100(typ)	175	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	72(typ)	175	72(typ)	175	
Fall Time	t_f	V_{GS}=10 V	66(typ)	140	66(typ)	140	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM15N05, RFM15N06	—	1.67	—	1.67	° C/W
		RFP15N05, RFP15N06	—	2.083	—	2.083	

[a] Pulsed: Pulse duration=300 µs max., duty cycle=2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

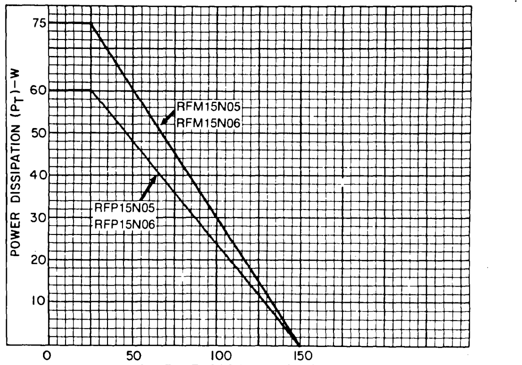
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N05 RFP15N05		RFM15N06 RFP15N06		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=7.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/µs	100 (typ)		100(typ)		ns

*Pulse Test: Width ≤ 300 µs, duty cycle ≤ 2%.



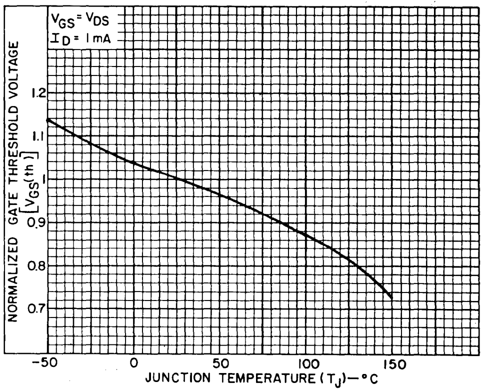
92CM-36962R1

Fig. 1 - Maximum safe operating areas for all types.



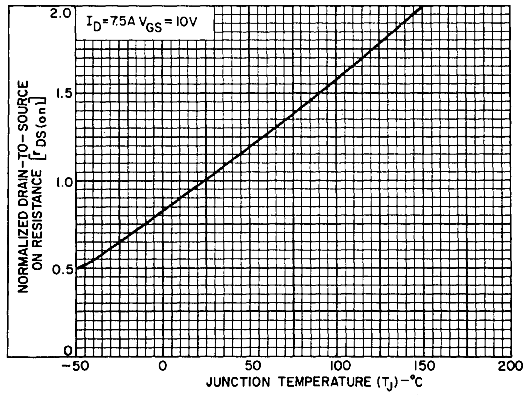
92CS-34364R2

Fig. 2 - Power dissipation vs. case temperature derating curve for all types.



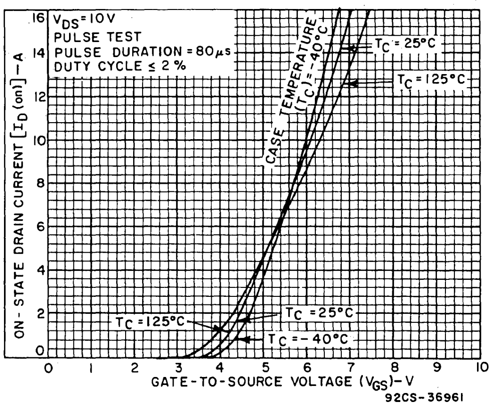
92CS-34359

Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.



92CS-36963

Fig. 4 - Normalized drain-to-source on resistance as a function of junction temperature for all types.



92CS-36961

Fig. 5 - Typical transfer characteristics for all types.

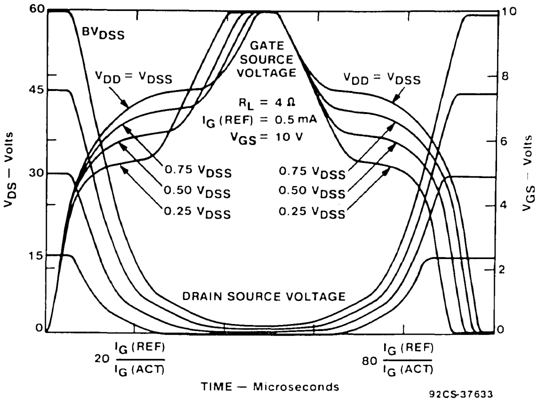


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

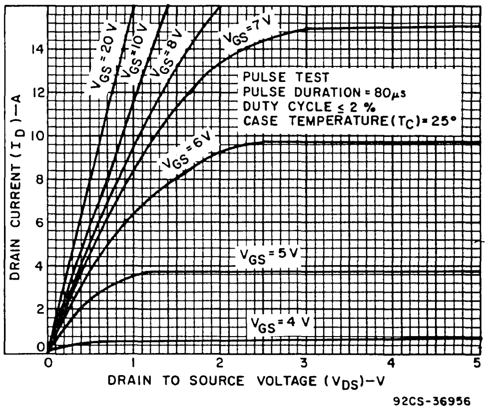


Fig. 7 - Typical saturation characteristics for all types.

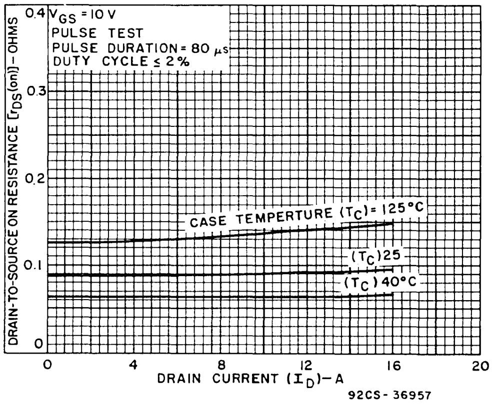


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

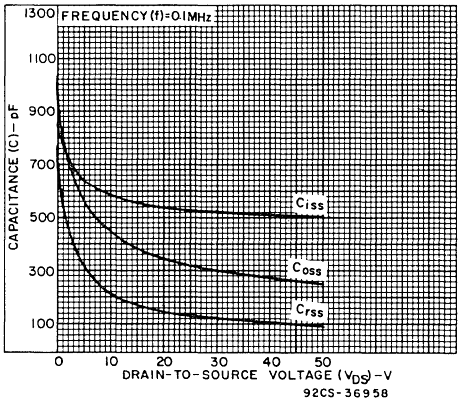


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

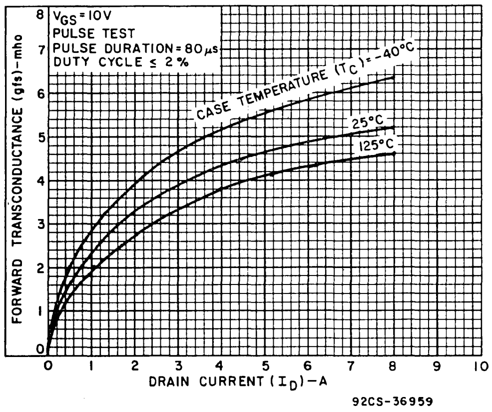


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

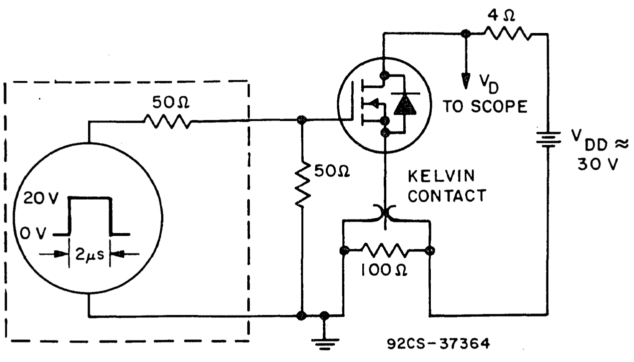


Fig. 11 — Switching Time Test Circuit

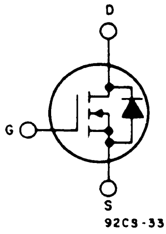
N-Channel Enhancement-Mode Power Field-Effect Transistors

15 A, 120 V — 150 V

r_{DS}(on): 0.15 Ω

Features:

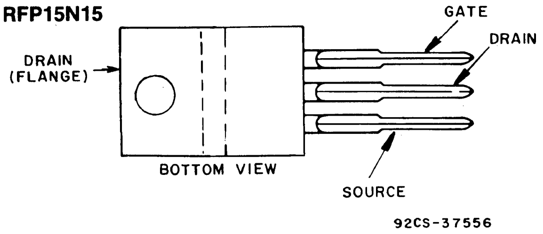
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-Channel Enhancement Mode

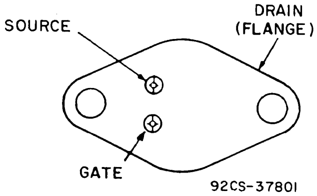
TERMINAL DESIGNATIONS

RFP15N12
RFP15N15



JEDEC TO-220AB

RFM15N12
RFM15N15



JEDEC TO-204MA

The RFM15N12 and RFM15N15 and the RFP15N12 and RFP15N15* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204MA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

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*The RFM and RFP series were formerly RCA developmental numbers TA9195 and TA9230, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_c=25°C):*

		RFM15N12	RFM15N15	RFP15N12	RFP15N15	
DRAIN-SOURCE VOLTAGE	V_{DSS}	120	150	120	150	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)	V_{DGR}	120	150	120	150	V
GATE-SOURCE VOLTAGE	V_{GS}	±20	±20	±20	±20	V
DRAIN CURRENT RMS Continuous	I_D	15	15	15	15	A
Pulsed	I_{DM}	40	40	40	40	A
POWER DISSIPATION						
@ T_c=25°C	P_T	100	100	75	75	W
Derate above T_c=25°C		0.80	0.80	0.6	0.6	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	−55 to +150	−55 to +150	−55 to +150	−55 to +150	°C

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_c) = 25° C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N12 RFP15N12		RFM15N15 RFP15N15		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	120	—	150	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V	—	1	—	—	μA
		V_{DS} = 120 V	—	—	—	1	
		T_C = 125° C					
		V_{DS} = 100 V	—	50	—	—	
		V_{DS} = 120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)^a$	I_D = 7.5 A V_{GS} = 10 V	—	1.125	—	1.125	V
		I_D = 15 A V_{GS} = 10 V	—	3	—	3	
Static Drain-Source On Resistance	$r_{DS}(on)^a$	I_D = 7.5 A V_{GS} = 10 V	—	0.15	—	0.15	Ω
Forward Transconductance	$g_{fs}{}^a$	V_{DS} = 10 V I_D = 7.5 A	5	—	5	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f=0.1 MHz	—	1450	—	1450	pF
Output Capacitance	C_{oss}		—	450	—	450	
Reverse Transfer Capacitance	C_{rss}		—	150	—	150	
Turn-On Delay Time	$t_d(on)$	V_{DD}=75 V I_D = 7.5 A R_{gen} = R_{gs} = 50 Ω V_{GS} = 10 V	50(typ.)	75	50(typ.)	75	ns
Rise Time	t_r		150(typ.)	225	150(typ.)	225	
Turn-Off Delay Time	$t_d(off)$		185(typ.)	280	185(typ.)	280	
Fall Time	t_f		125(typ.)	190	125(typ.)	190	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM15N12, RFM15N15	—	1.25	—	1.25	° C/W
		RFP15N12, RFP15N15	—	1.67	—	1.67	

[a] Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N12 RFP15N12		RFM15N15 RFP15N15		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=7.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

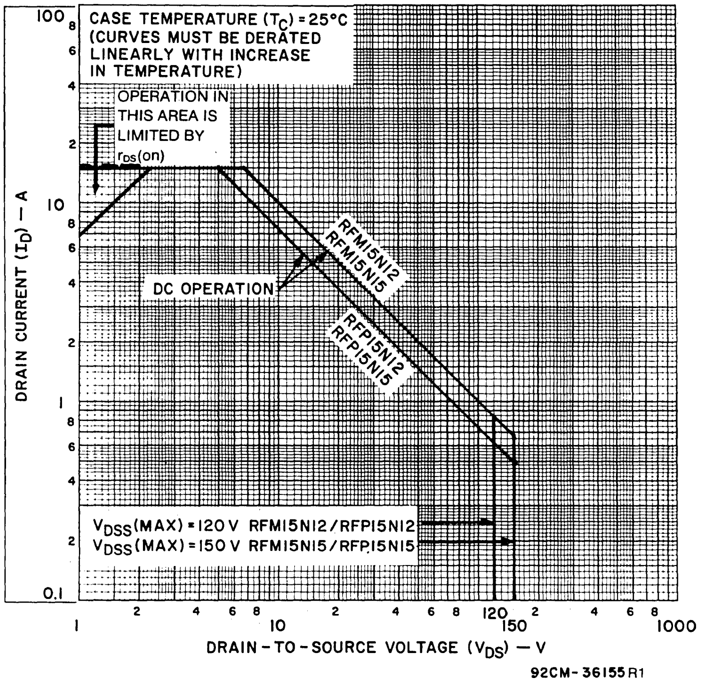

Fig. 1 — Maximum operating areas for all types.

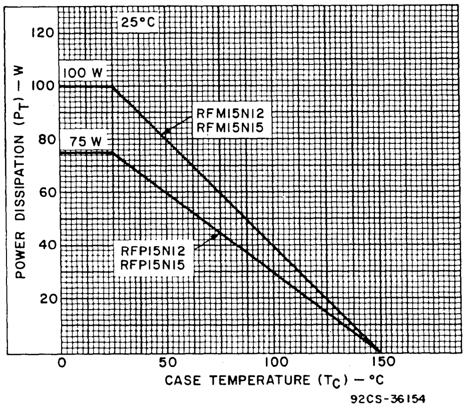

Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

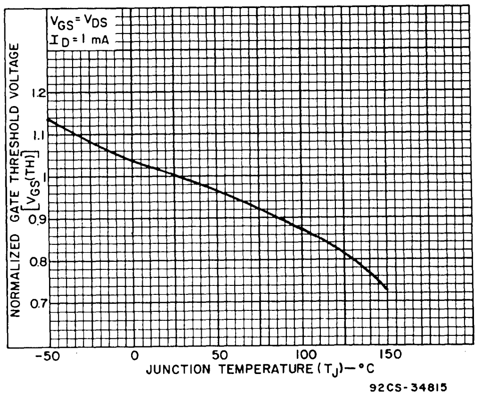

Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

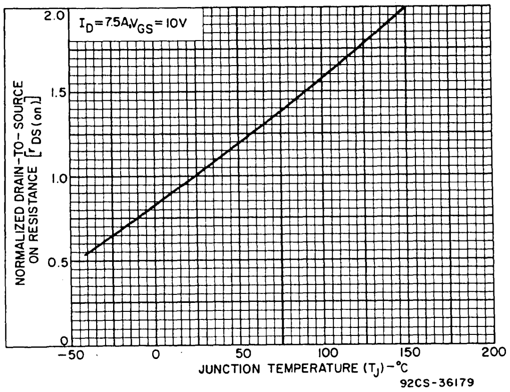

Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

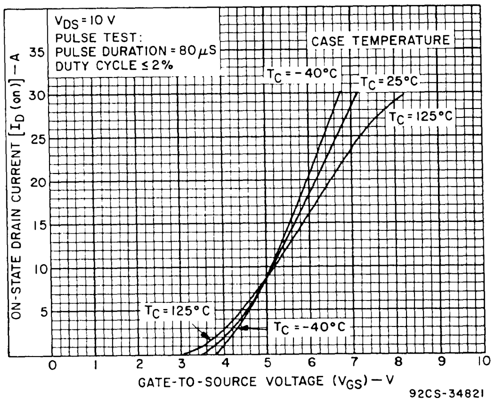

Fig. 5 — Typical transfer characteristics for all types.

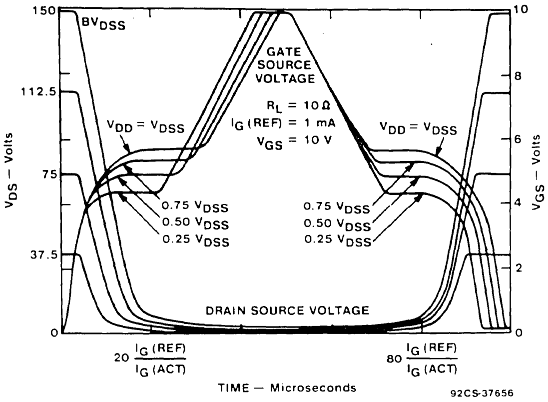

Fig. 6 - Normalized switching waveforms for constant gate-current drive.

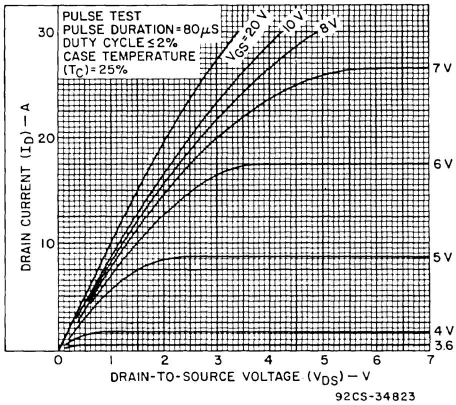

Fig. 7 — Typical saturation characteristics for all types.

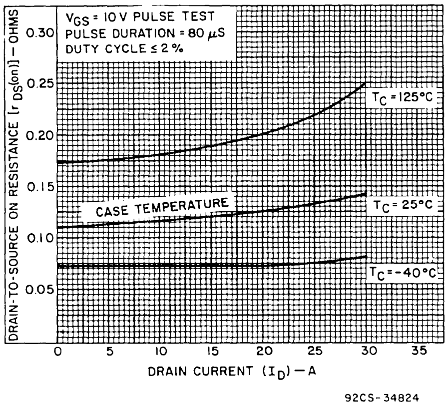

Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

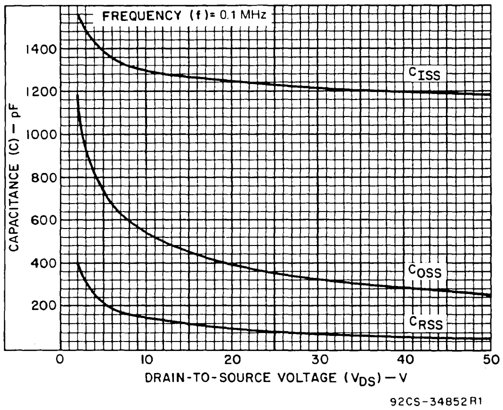

Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

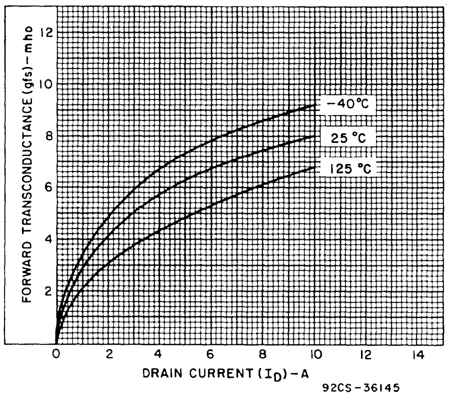

Fig. 10 - Typical forward transconductance as a function of drain current for all types.

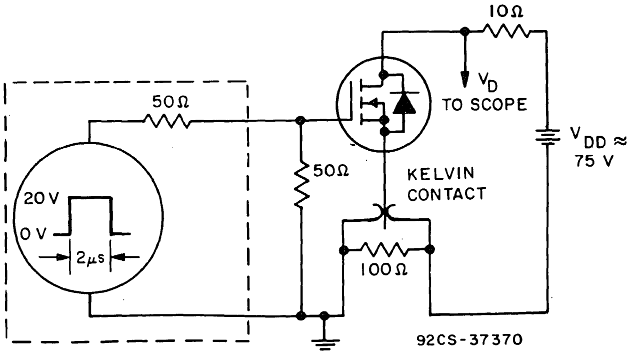

Fig. 11 — Switching Time Test Circuit

RFM18N08, RFM18N10, RFP18N08, RFP18N10 File Number **1446**

N-Channel Enhancment-Mode Power Field-Effect Transistors

18 A, 80 V — 100 V

r_{DS}(on): 0.12 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The RFM18N08 and RFM18N10 and the RFP18N08 and RFP18N10* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204MA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

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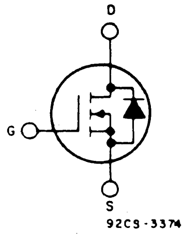
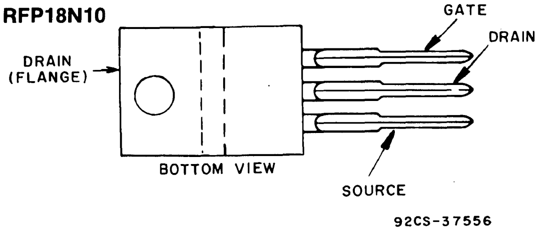
*The RFM and RFP series were formerly RCA developmental numbers TA9286 and TA9287, respectively.



N-Channel Enhancement Mode

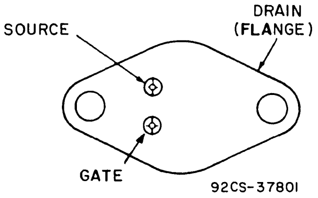
TERMINAL DESIGNATIONS

RFP18N08
RFP18N10



JEDEC TO-220AB

RFM18N08
RFM18N10



JEDEC TO-204MA

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25°C):*

		RFM18N08	RFM18N10	RFP18N08	RFP18N10	
DRAIN-SOURCE VOLTAGE	V_{DSS}	80	100	80	100	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)	V_{DGR}	80	100	80	100	V
GATE-SOURCE VOLTAGE	V_{GS}	±20				V
DRAIN CURRENT RMS Continuous	I_D	18				A
Pulsed	I_{DM}	45				A
POWER DISSIPATION						
@ T_C=25° C	P_T	100	100	75	75	W
Derate above T_C=25° C		0.8	0.8	0.6	0.6	W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	−55 to +150				° C

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_c) = 25° C unless otherwise specified*

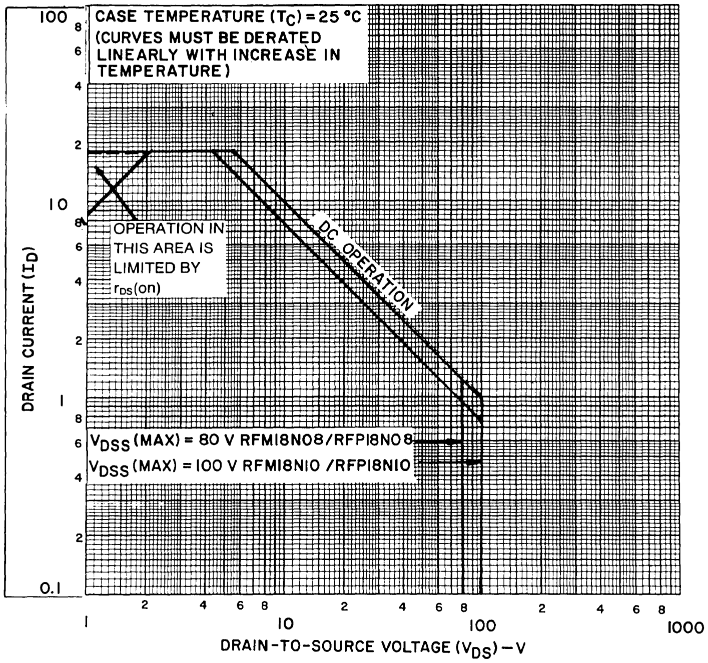
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS RFM18N08 RFP18N08 MIN.	 MAX.	 RFM18N10 RFP18N10 MIN.	 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 1$ mA $V_{GS} = 0$	80	—	100	—	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}$ $I_D = 1$ mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 65$ V	—	1	—	—	μA
		$V_{DS} = 80$ V	—	—	—	1	
		$T_C = 125°$ C					
		$V_{DS} = 65$ V	—	50	—	—	
		$V_{DS} = 80$ V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20$ V $V_{DS} = 0$	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)^a$	$I_D = 9$ A $V_{GS} = 10$ V	—	1.08	—	1.08	V
		$I_D = 18$ A $V_{GS} = 10$ V	—	3.0	—	3.0	
Static Drain-Source On Resistance	$r_{DS}(on)^a$	$I_D = 9$ A $V_{GS} = 10$ V	—	0.12	—	0.12	Ω
Forward Transconductance	$g_{fs}{}^a$	$V_{DS} = 10$ V $I_D = 9$ A	5	—	5	—	mho
Input Capacitance	C_{iss}	$V_{DS} = 25$ V	—	1500	—	1500	pF
Output Capacitance	C_{oss}	$V_{GS} = 0$ V	—	750	—	750	
Reverse Transfer Capacitance	C_{rss}	f=0.1 MHz	—	300	—	300	
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V	60(typ.)	90	60(typ.)	90	ns
Rise Time	t_r	$I_D = 9$ A	300(typ.)	450	300(typ.)	450	
Turn-Off Delay Time	$t_d(off)$	$R_{gen} = R_{gs} = 50\ \Omega$	150(typ.)	225	150(typ.)	225	
Fall Time	t_f	$V_{GS} = 10$ V	150(typ.)	225	150(typ.)	225	
Thermal Resistance Junction-to-Case	RθJC	RFM18N08, RFM18N10	—	1.25	—	1.25	°C/W
		RFP18N08, RFP18N10	—	1.67	—	1.67	

[a] Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

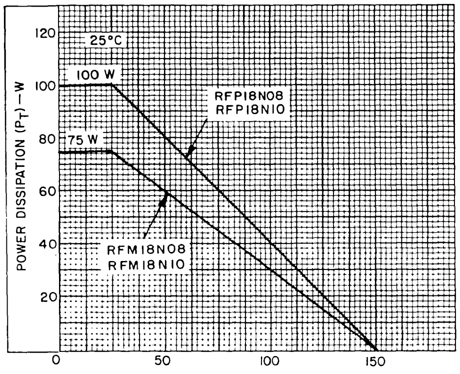
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFM18N08 RFM18N10 MIN.	 MAX.	 RFP18N08 RFP18N10 MIN.	 MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=9 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.



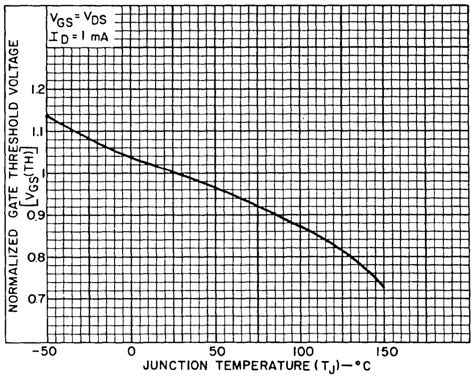
92CM- 36150R1

Fig. 1 — Maximum operating areas for all types.



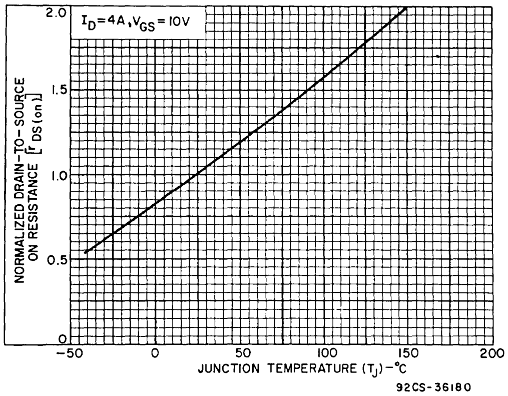
92CS-34818

Fig. 2 — Power dissipation vs. case temperature derating curve for all types.



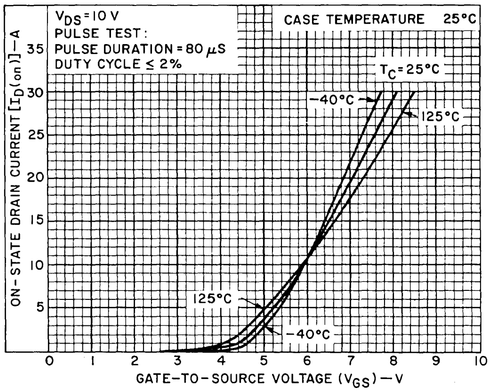
92CS-34815

Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.



92CS-36180

Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.



92CS-36149

Fig. 5 — Typical transfer characteristics for all types.

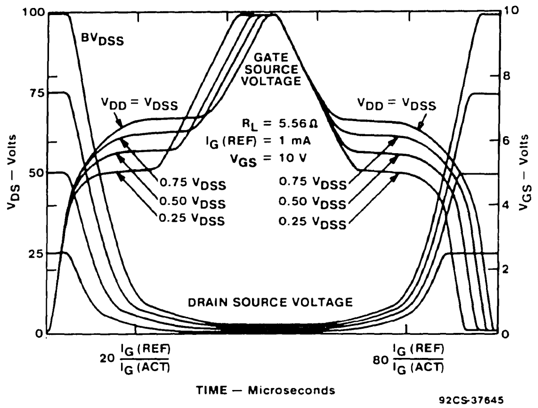


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

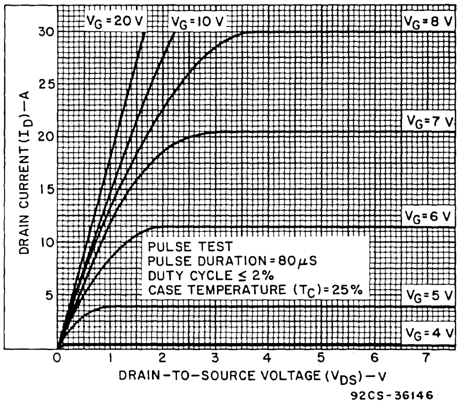


Fig. 7 — Typical saturation characteristics for all types.

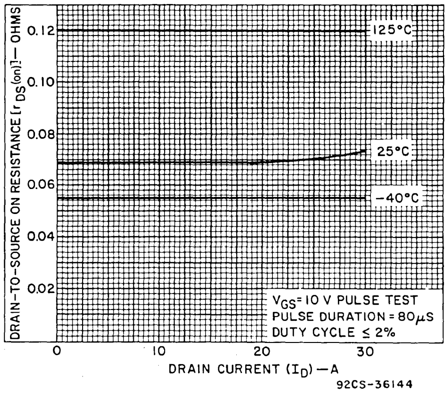


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

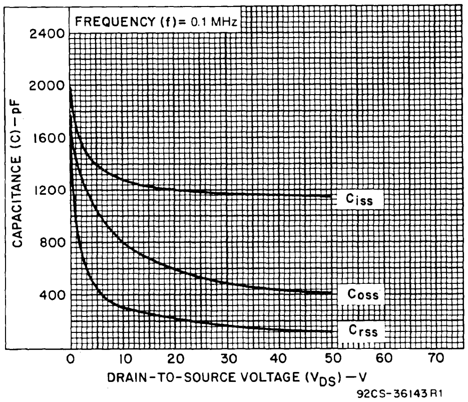


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

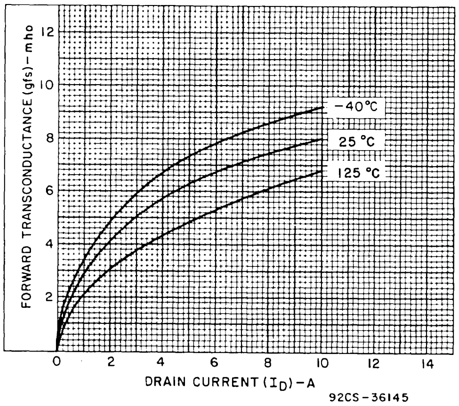


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

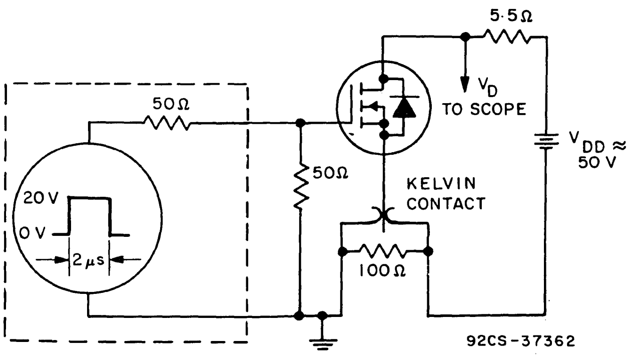


Fig. 11 — Switching Time Test Circuit

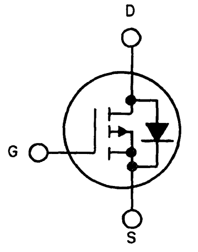
P-Channel Enhancement-Mode Power Field-Effect Transistors

25 A, -100 V - -80 V

$r_{DS}(on)=0.20\ \Omega$

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



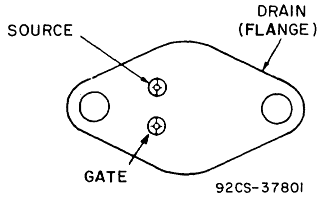
92CS-36485

P-CHANNEL ENHANCEMENT MODE

The RFK25P10 and RFK25P08* are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

TERMINAL DESIGNATIONS



92CS-37801

JEDEC TO-204AE

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*The RFK25P10 and RFK25P08 types were formerly RCA developmental numbers TA9412A and TA9412B, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFK25P10	RFK25P08	
DRAIN-SOURCE VOLTAGE	V_{DSS}	-100	-80	V
DRAIN-GATE VOLTAGE, R_{GS}=1 MΩ)	V_{DGR}	-100	-80	V
GATE-SOURCE VOLTAGE	V_{GS}	±20	±20	V
DRAIN CURRENT, RMS Continuous	I_D	25	25	A
Pulsed	I_{DM}	60	60	A
POWER DISSIPATION	P_T			
@ T_C = 25° C		150	150	W
Derate above T_C=25° C		1.2	1.2	W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150	-55 to +150	° C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK25P10		RFK25P08		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	-100	—	-80	—	V
Gate Threshold Voltage	$V_{GS}(th)$	$V_{GS}=V_{DS}$ I_D=1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-80 V	—	1	—	—	μA
		V_{DS}=-65 V	—	—	—	1	
		T_C=125° C V_{DS}=-80 V	—	50	—	—	
		V_{DS}=-65 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20$ V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)^a$	I_D=12.5 A V_{GS}=-10 V	—	-2.5	—	-2.5	V
		I_D=25 A V_{GS}=-10 V	—	-6	—	-6	
Static Drain-Source On Resistance	$r_{DS}(on)^a$	I_D=12.5 A V_{GS}=-10 V	—	0.2	—	0.2	Ω
Forward Transconductance	g_{fs}^a	V_{DS}=-10 V I_D=12.5 A	4	—	4	—	mho
Input Capacitance	C_{iss}	V_{DS}=-25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	1500	—	1500	
Reverse Transfer Capacitance	C_{rss}	f=0.1 MHz	—	500	—	500	
Turn-On Delay Time	t_d (on)	V_{DD}=-50 V	35(typ)	50	35(typ)	50	ns
Rise Time	t_r	I_D=12.5 A	165(typ)	250	165(typ)	250	
Turn-Off Delay Time	t_d (off)	$R_{gen}=R_{gs}$=50 Ω	270(typ)	400	270(typ)	400	
Fall Time	t_f	V_{GS}=-10 V	165(typ)	250	165(typ)	250	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFK25P10, RFK25P08	—	0.83	—	0.83	°C/W

[a] Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK25P10		RFK25P08		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage*	V_{SD}	I_{SD}=12.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	300 typ.		300 typ.		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

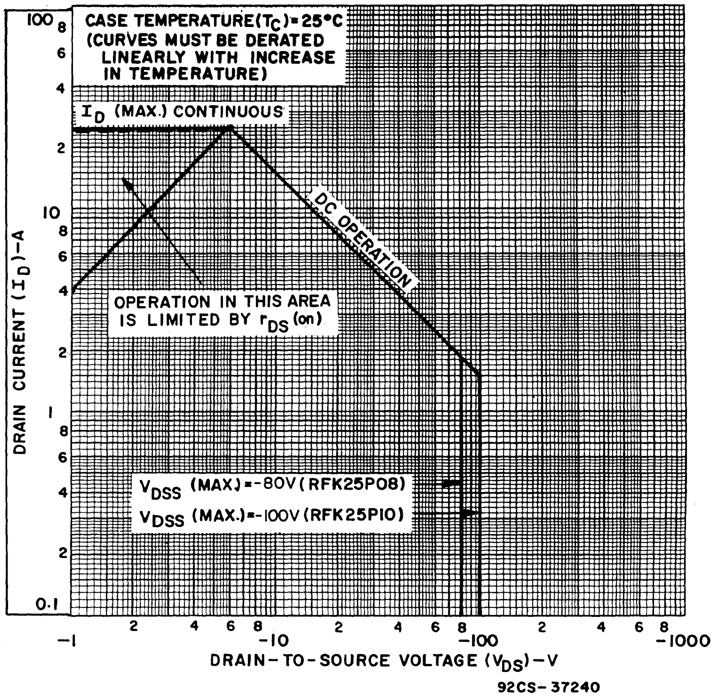


Fig. 1 - Maximum safe operating areas for all types.

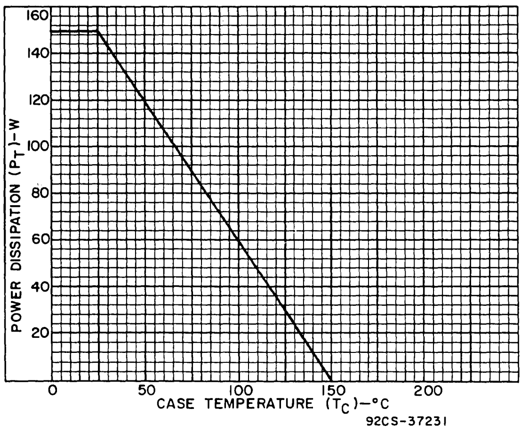


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

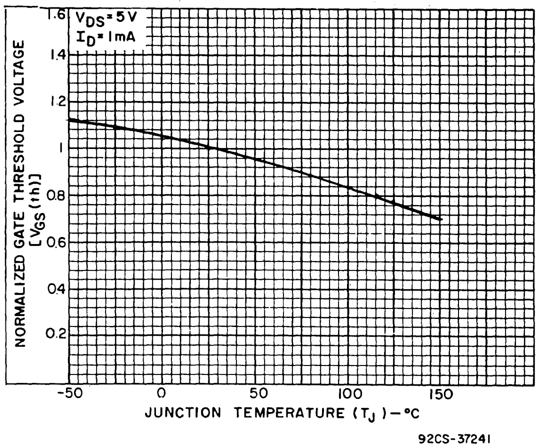


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

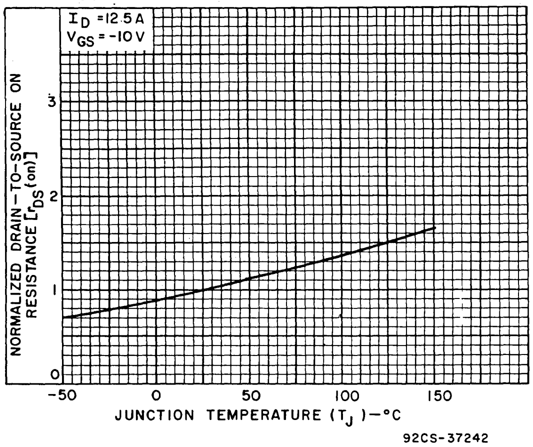


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

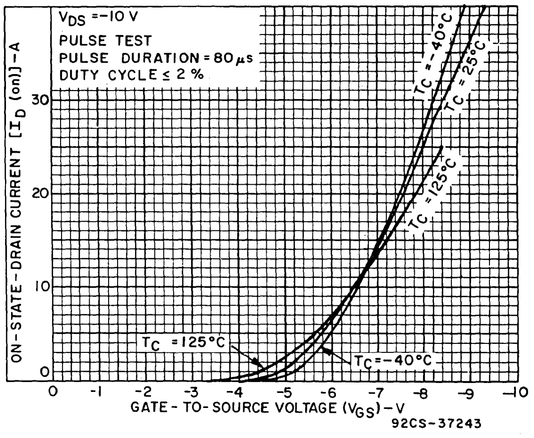


Fig. 5 - Typical transfer characteristics for all types.

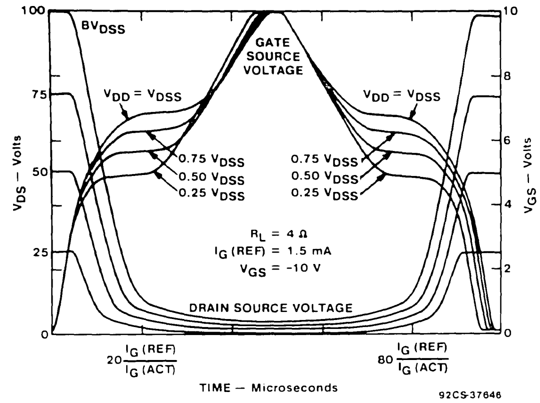


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

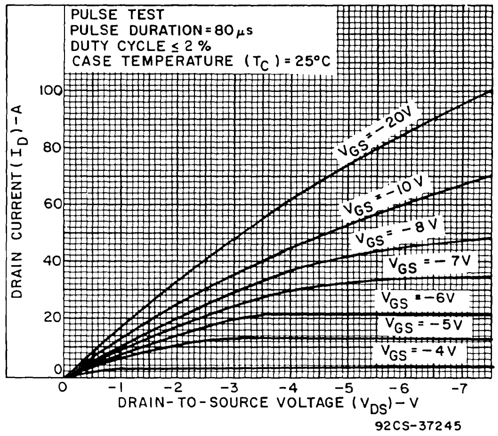


Fig. 7 - Typical saturation characteristics for all types.

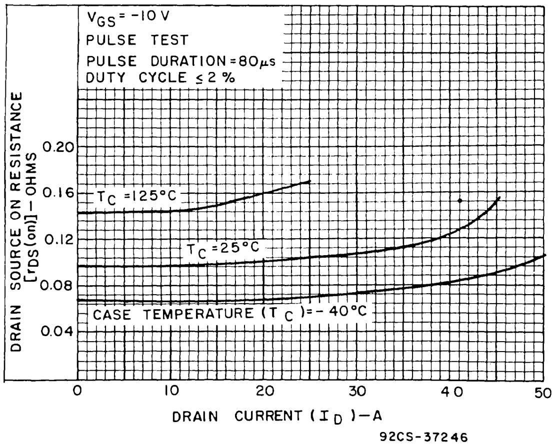


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

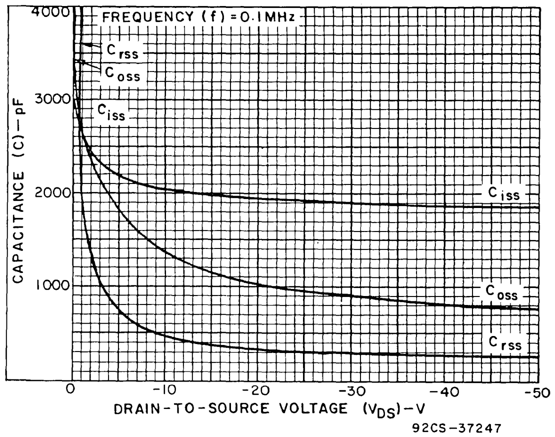


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

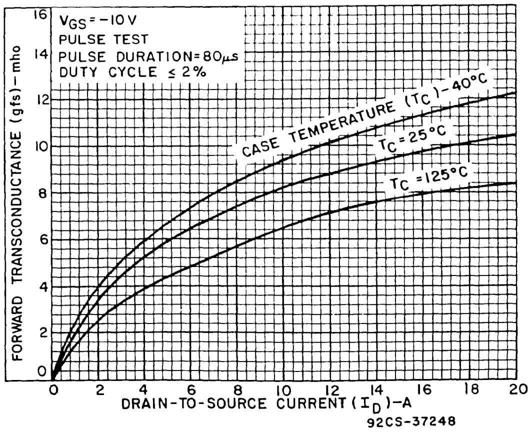


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

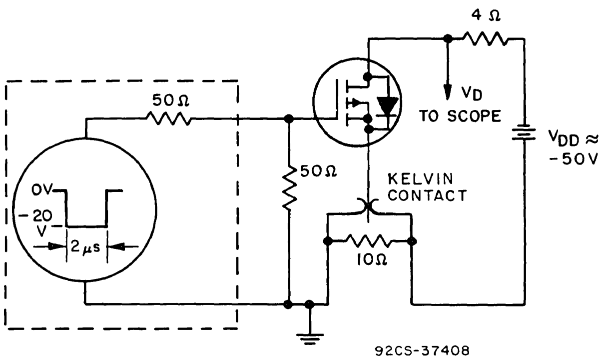


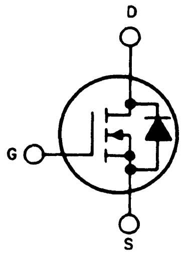
Fig. 11 - Switching time test circuit.

N-Channel Enhancement-Mode Power Field-Effect Transistors

25 A, 180 V - 200 V

$r_{DS}(on) = 0.15\ \Omega$

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

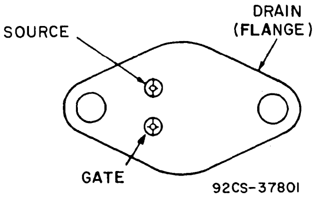


N-CHANNEL ENHANCEMENT MODE

The RFK25N18 and RFK25N20* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

TERMINAL DESIGNATIONS



JEDEC TO-204AE

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFK25N18		RFK25N20	
DRAIN-SOURCE VOLTAGE	V_{DSS}	180		200	V
DRAIN-GATE VOLTAGE, R_{gs}=1 MΩ	V_{DGR}	180		200	V
GATE-SOURCE VOLTAGE	V_{GS}		±20		V
DRAIN CURRENT, RMS Continuous	I_D		25		A
Pulsed	I_{DM}		60		A
POWER DISSIPATION @ T_C=25°C	P_T		150		W
Derate above T_C=25°C			1.2		W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}		-55 to +150		°C

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*The RFK25N18 and RFK25N20 types were formerly RCA developmental numbers TA9295A and TA9295B, respectively.

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK25N18		RFK25N20		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	180	—	200	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V V_{DS}=160 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=145 V V_{DS}=160 V	— —	50 —	— —	— 50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=12.5 A V_{GS}=10 V	—	1.875	—	1.875	V
		I_D=25 A V_{GS}=10 V	—	5	—	5	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=12.5 A V_{GS}=10 V	—	.15	—	.15	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=12.5 A	7	—	7	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	3500	—	3500	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	900	—	900	
Reverse Transfer Capacitance	C_{rss}	f=0.1 MHz	—	400	—	400	
Turn-On Delay Time	$t_d(on)$	V_{DD}=100 V	40(typ)	80	40(typ)	80	ns
Rise Time	t_r	I_D=12.5 A	150(typ)	225	150(typ)	225	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	300(typ)	400	300(typ)	400	
Fall Time	t_f	V_{GS}=10 V	120(typ)	200	120(typ)	200	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFK25N18, RFK25N20 Series	—	0.83	—	0.83	°C/W

[a] Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK25N18		RFK25N20		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=12.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	300(typ)		300(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

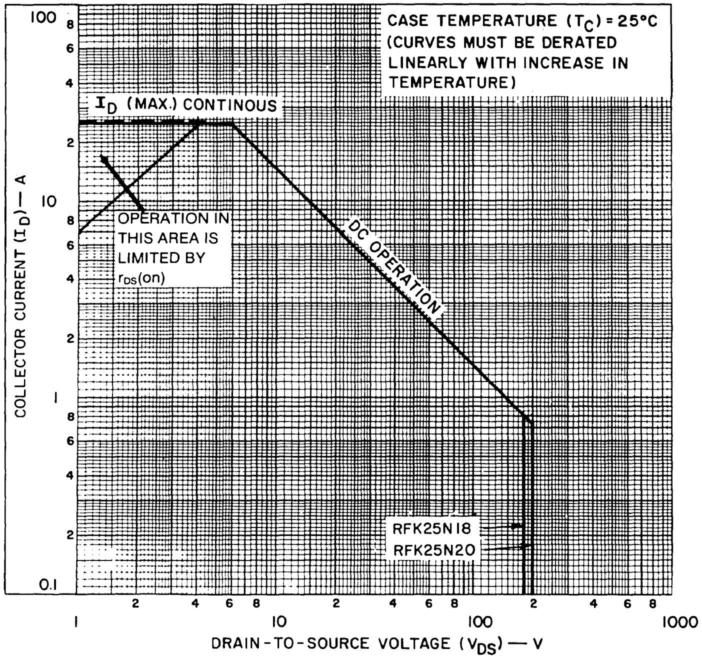


Fig. 1 — Maximum safe operating areas for all types.

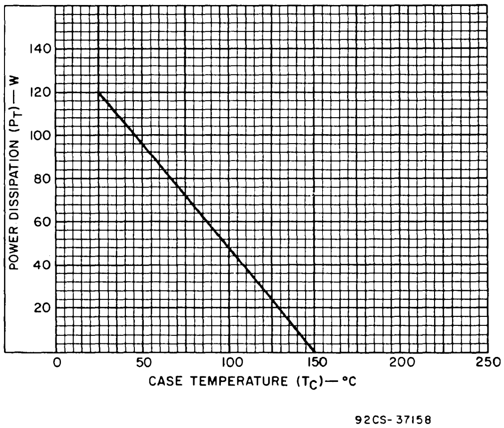


Fig. 2 — Power vs. temperature derating curve for all types.

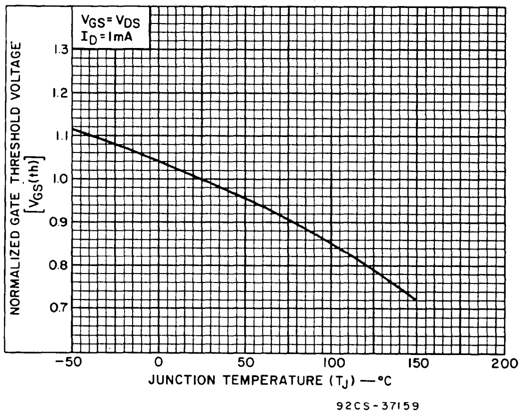


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

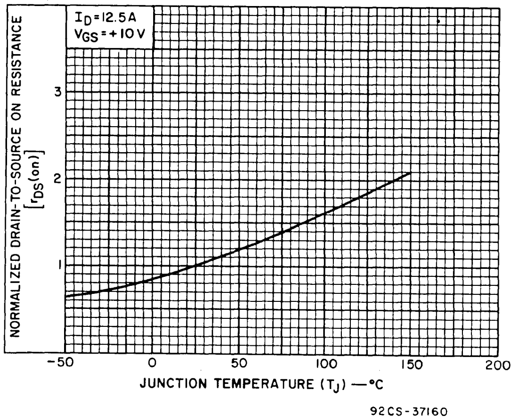


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

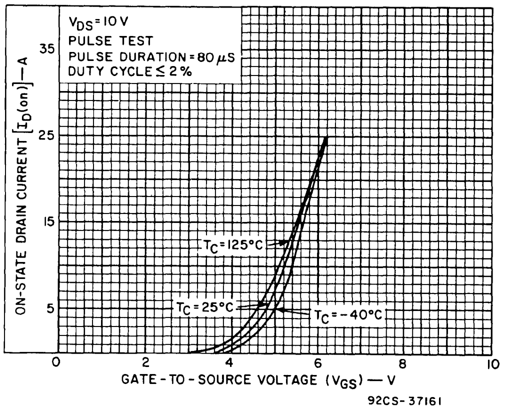


Fig. 5 — Typical transfer characteristics for all types.

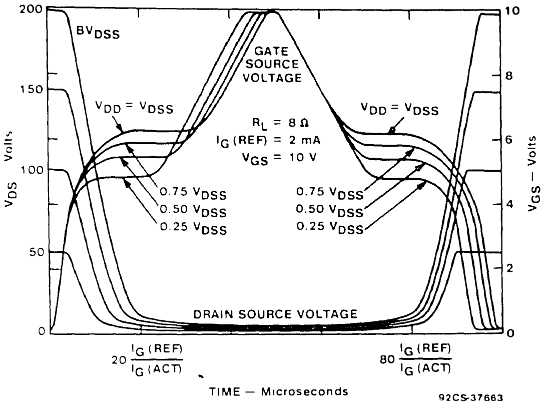


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

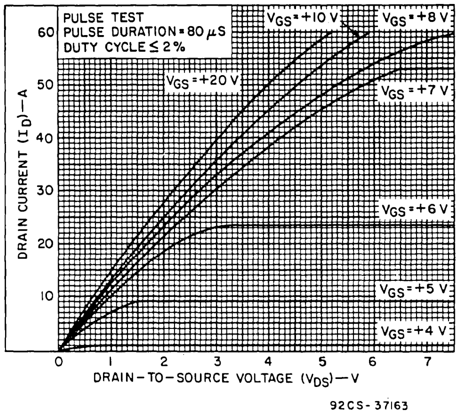


Fig. 7 — Typical saturation characteristics for all types.

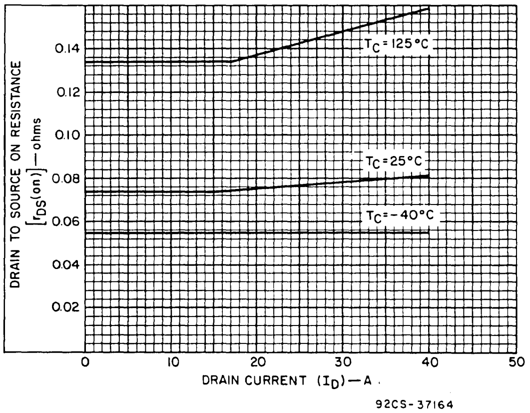


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

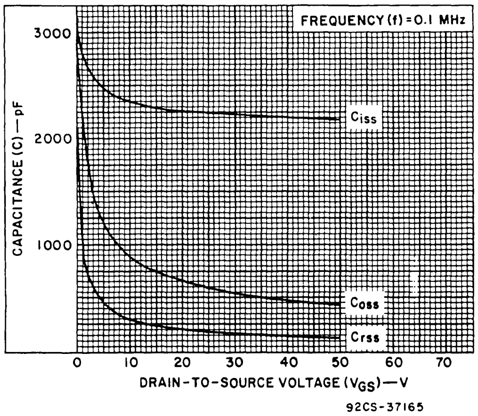


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

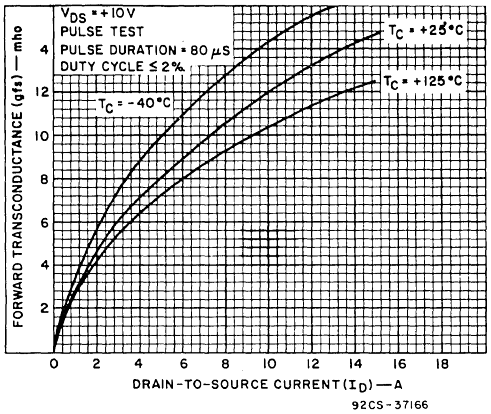


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

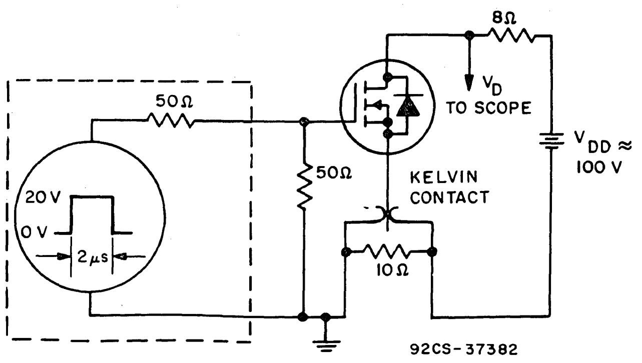


Fig. 11 — Switching Time Test Circuit

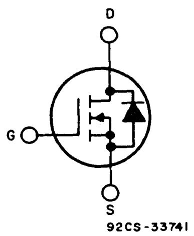
RFK30N12, RFK30N15 File Number **1455**

N-Channel Enhancement-Mode Power Field-Effect Transistors

30 A, 120 V - 150 V
$r_{DS}(on)=0.085\ \Omega$

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

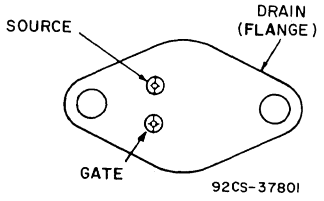


N-CHANNEL ENHANCEMENT MODE

The RFK30N12 and RFK30N15* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

TERMINAL DESIGNATIONS



JEDEC TO-204AE

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*The RFK30N12 and RFK30N15 types were formerly RCA developmental numbers TA9188A and TA9188B, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFK30N12	RFK30N15	
DRAIN-SOURCE VOLTAGE	V_{DSS}	120	150	V
DRAIN-GATE VOLTAGE, R_{gs}=1 MΩ	V_{DGR}	120	150	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	30		A
Pulsed	I_{DM}	100		A
POWER DISSIPATION @T_C=25° C	P_T	120		W
Derate above T_C=25° C		1.2		W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +125		°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK30N12		RFK30N15		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	150	—	V
Gate Threshold Voltage	$V_{GS}(th)$	$V_{GS}=V_{DS}$ I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100 V	—	1	—	—	μA
		V_{DS}=120 V	—	—	—	1	
		T_C=125° C					
		V_{DS}=100 V	—	50	—	—	
		V_{DS}=120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20$ V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=15 A V_{GS}=10 V	—	1.275	—	1.275	V
		I_D=30 A V_{GS}=10 V	—	3	—	3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=15 A V_{GS}=10 V	—	0.085	—	0.085	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=15 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	1200	—	1200	
Reverse Transfer Capacitance	C_{rss}	f=0.1 MHz	—	500	—	500	
Turn-On Delay Time	$t_d(on)$	V_{DD}=75V	75(typ)	115	75(typ)	115	ns
Rise Time	t_r	I_D=15 A	420(typ)	630	420(typ)	630	
Turn-Off Delay Time	$t_d(off)$	$R_{gen}=R_{gs}$=50 Ω	300(typ)	450	300(typ)	450	
Fall Time	t_f	V_{GS}=10 V	250(typ)	375	250(typ)	375	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFK30N12, RFK30N15 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK30N12		RFK30N15		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=15 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

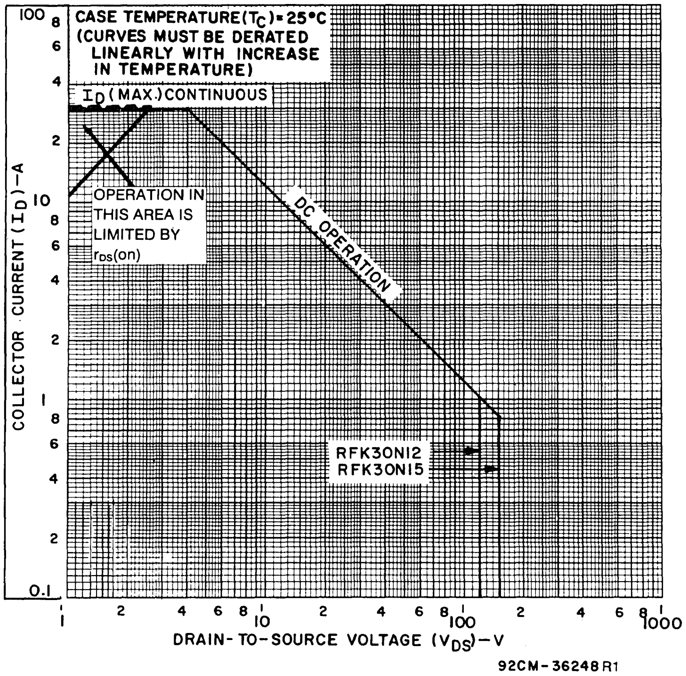


Fig. 1 - Maximum safe operating areas for all types.

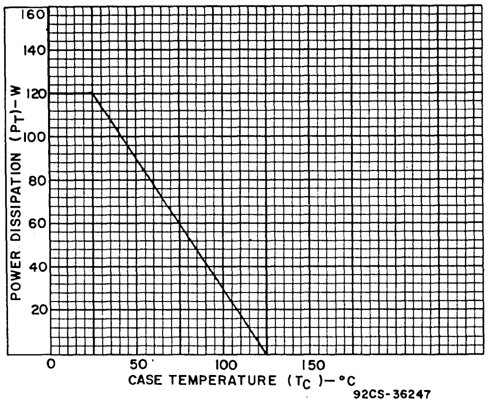


Fig. 2 - Power vs. temperature derating curve for all types.

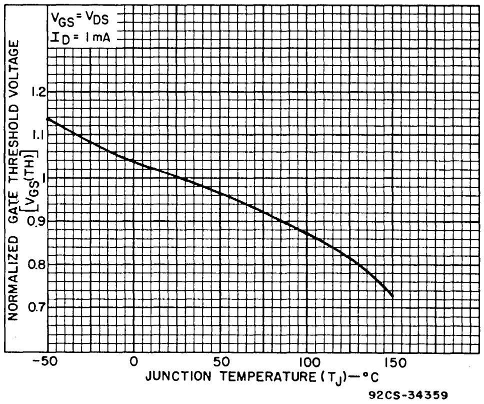


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

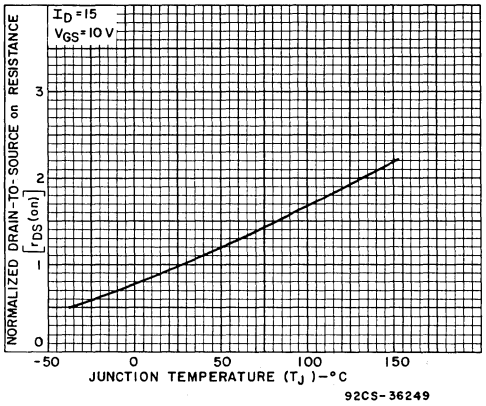


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

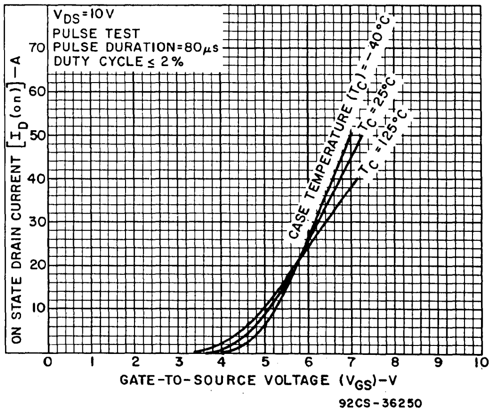


Fig. 5 - Typical transfer characteristics for all types.

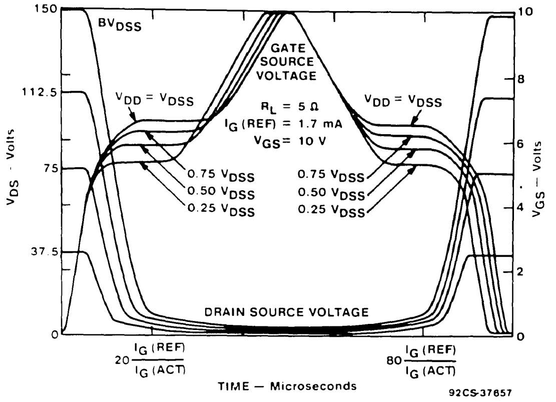


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

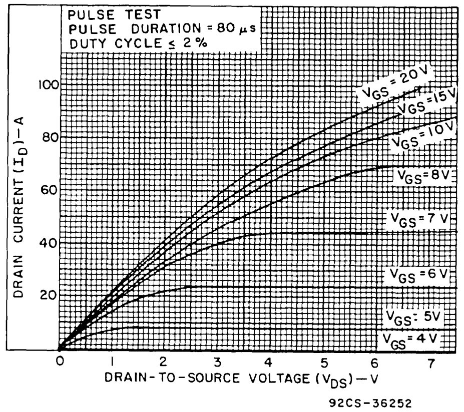


Fig. 7 - Typical saturation characteristics for all types.

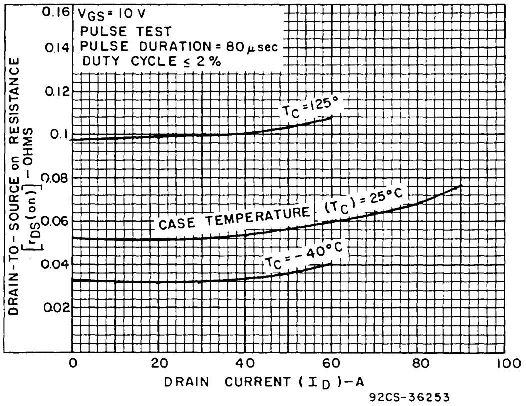


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

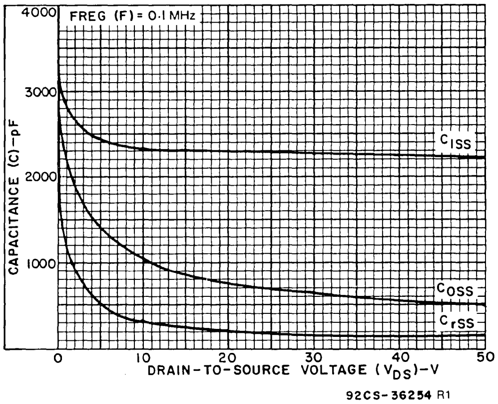


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

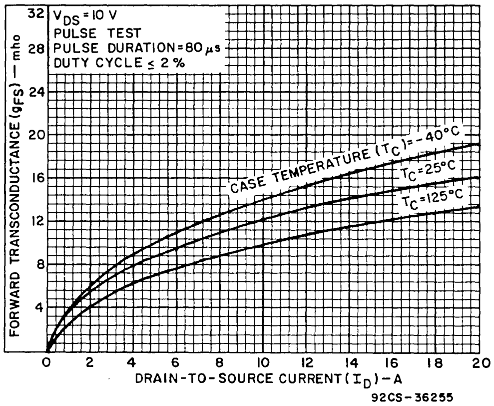


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

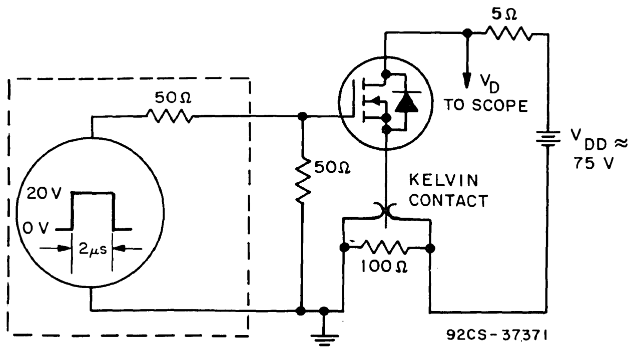
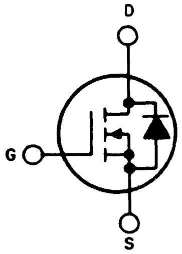


Fig. 11 — Switching Time Test Circuit

N-Channel Enhancement-Mode Power Field-Effect Transistors

35 A, 80 V - 100 V
$r_{DS}(on) = 0.06\ \Omega$

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



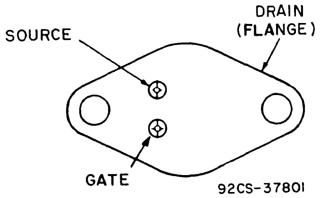
92CS-33741

N-CHANNEL ENHANCEMENT MODE

The RFK35N08 and RFK35N10* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

TERMINAL DESIGNATIONS



92CS-37801

JEDEC TO-204AE

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*The RFK35N08 and RFK35N10 types were formerly RCA developmental numbers TA9288A and TA9288B, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFK35N08		RFK35N10	
DRAIN-SOURCE VOLTAGE	V_{DSS}	80		100	V
DRAIN-GATE VOLTAGE, R_{gs}=1 MΩ	V_{DGR}	80		100	V
GATE-SOURCE VOLTAGE	V_{GS}		±20		V
DRAIN CURRENT, RMS Continuous	I_D		35		A
Pulsed	I_{DM}		100		A
POWER DISSIPATION @ T_C=25°C	P_T		150		W
Derate above T_C=25°C			1.2		W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}		-55 to +150		°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

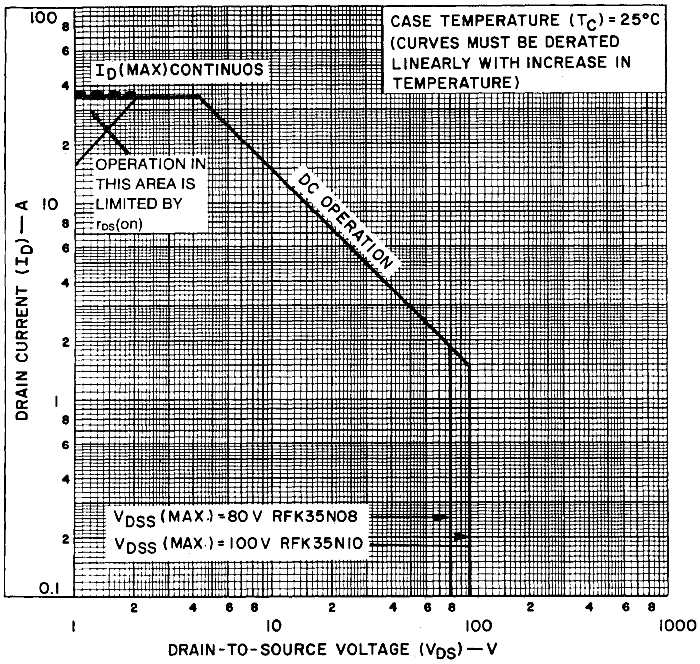
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK35N08		RFK35N10		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	100	—	V
Gate Threshold Voltage	V_{GS}(th)	$V_{GS}=V_{DS}$ I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V	—	1	—	—	μA
		V_{DS}=80 V	—	—	—	1	
		T_C=125° C V_{DS}=65 V	—	50	—	—	
		V_{DS}=80 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)^a$	I_D=17.5 A V_{GS}=10 V	—	1.05	—	1.05	V
		I_D=35 A V_{GS}=10 V	—	3.5	—	3.5	
Static Drain-Source On Resistance	$r_{DS}(on)^a$	I_D=17.5 A V_{GS}=10 V	—	.06	—	.06	Ω
Forward Transconductance	g_{fs}^a	V_{DS}=10 V I_D=17.5 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	1500	—	1500	
Reverse Transfer Capacitance	C_{rss}	f=0.1 MHz	—	600	—	600	
Turn-On Delay Time	t_d(on)	V_{DS}=50 V	45(typ)	100	45(typ)	100	ns
Rise Time	t_r	I_D=17.5 A	225(typ)	450	225(typ)	450	
Turn-Off Delay Time	t_d(off)	$R_{gen}=R_{gs}$=50 Ω	240(typ)	450	240(typ)	450	
Fall Time	t_f	V_{GS}=10 V	165(typ)	350	165(typ)	350	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFK35N08, RFK35N10 Series	—	0.83	—	0.83	°C/W

[a] Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

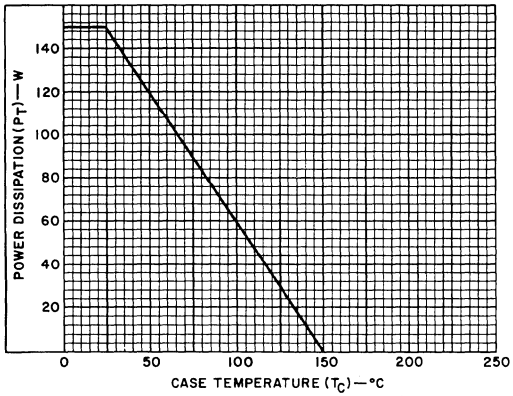
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK35N08		RFK35N10		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=17.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.



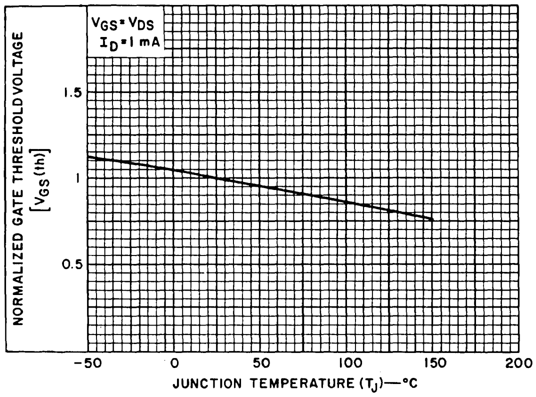
92CS-37167R1

Fig. 1 — Maximum safe operating areas for all types.



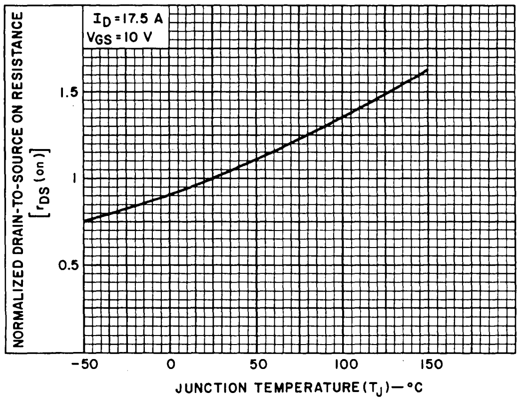
92CS-37168

Fig. 2 — Power vs. temperature derating curve for all types.



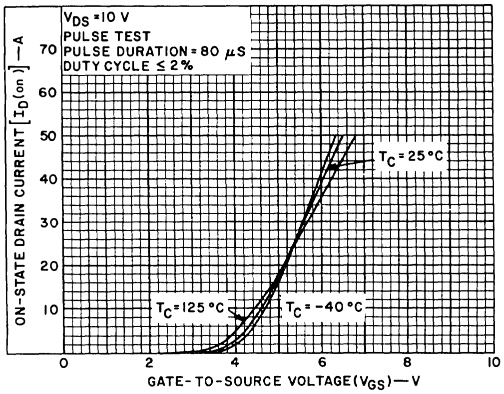
92CS-37169

Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.



92CS-37170

Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.



92CS-37171

Fig. 5 — Typical transfer characteristics for all types.

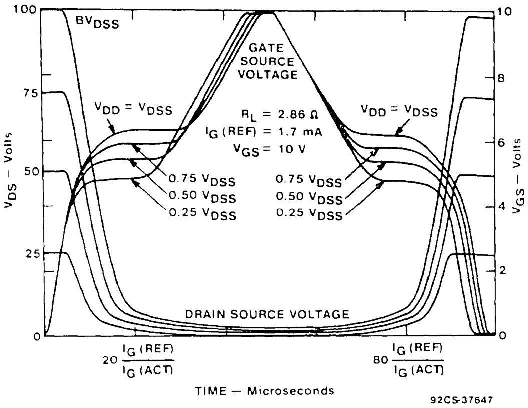


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

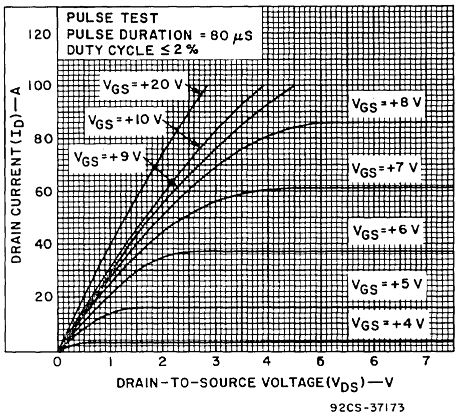


Fig. 7 — Typical saturation characteristics for all types.

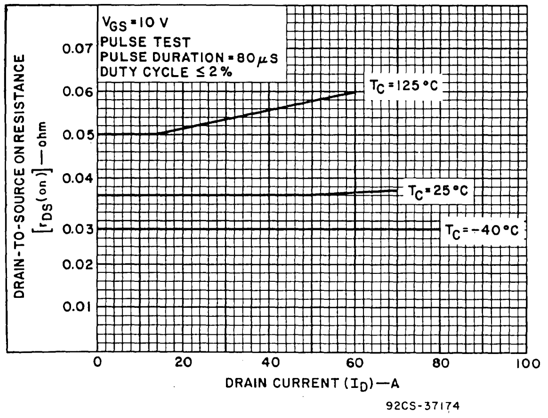


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

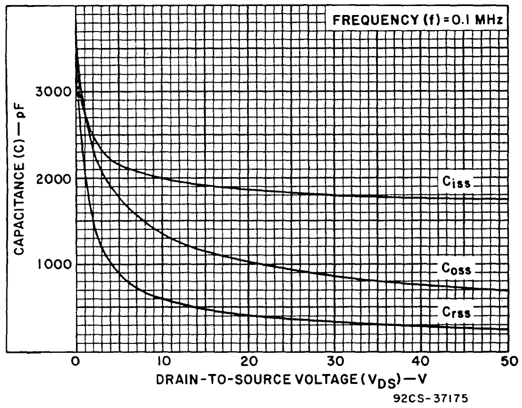


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

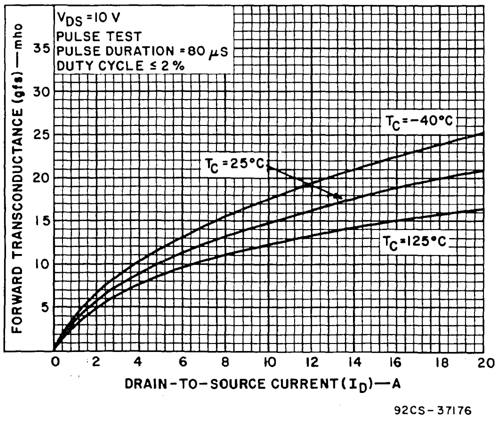


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

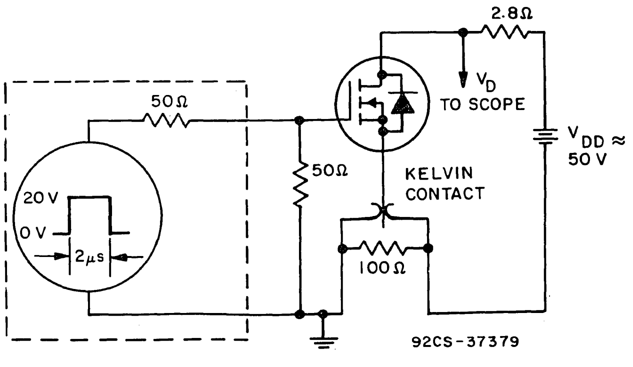
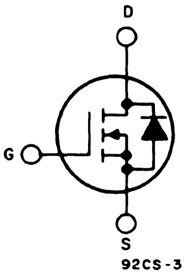


Fig. 11 — Switching Time Test Circuit.

N-Channel Enhancement-Mode Power Field-Effect Transistors

45 A, 50 V - 60 V
$r_{DS}(on) = 0.040\ \Omega$

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

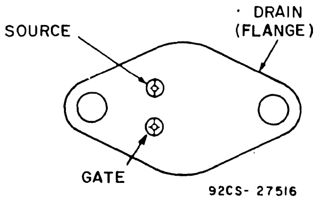


N-CHANNEL ENHANCEMENT MODE

The RFK45N05 and RFK45N06* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

TERMINAL DESIGNATIONS



JEDEC TO-204AE

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*The RFK45N05 and RFK45N06 types were formerly RCA developmental numbers TA9388A and TA9388B, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFK45N05		RFK45N06	
DRAIN-SOURCE VOLTAGE	V_{DSS}	50		60	V
DRAIN-GATE VOLTAGE, R_{gs}=1 MΩ	V_{DGR}	50		60	V
GATE-SOURCE VOLTAGE	V_{GS}		±20		V
DRAIN CURRENT, RMS Continuous	I_D		45		A
Pulsed	I_{DM}		100		A
POWER DISSIPATION @ T_C=25°C	P_T		150		W
Derate above T_C=25°C			1.2		W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}		-55 to +150		°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

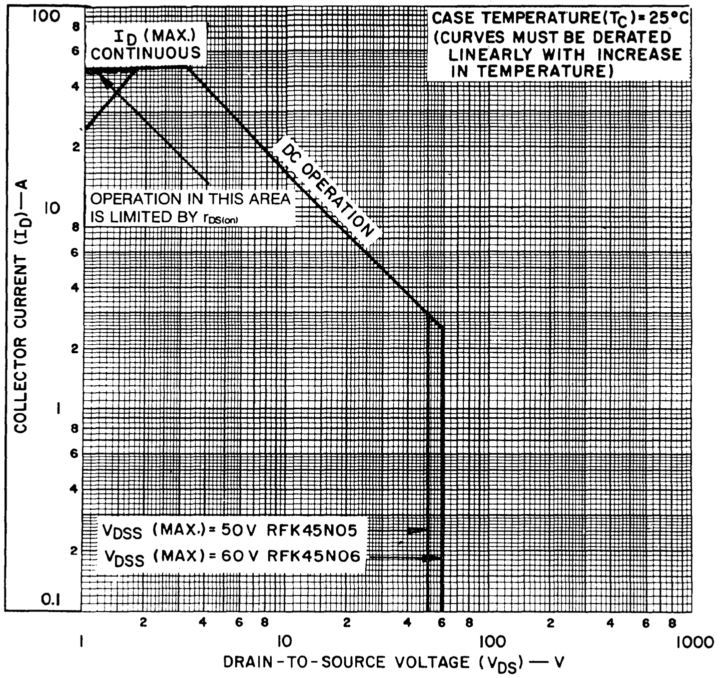
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK45N05		RFK45N06		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	60	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40 V	—	1	—	—	μA
		V_{DS}=50 V	—	—	—	1	
		T_C=125°c V_{DS}=40 V	—	50	—	—	
		V_{DS}=50 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)^a$	I_D=22.5 A V_{GS}=10 V	—	0.9	—	0.9	V
		I_D=45 A V_{GS}=10 V	—	3.6	—	3.6	
Static Drain-Source On Resistance	$r_{DS}(on)^a$	I_D=22.5 A V_{GS}=10 V	—	.04	—	.04	Ω
Forward Transconductance	$g_{fs}{}^a$	V_{DS}=10 V I_D=22.5 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	1800	—	1800	
Reverse Transfer Capacitance	C_{rss}	f=0.1 MHz	—	750	—	750	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 30 V	40(typ)	80	40(typ)	80	ns
Rise Time	t_r	I_D=22.5 A	310(typ)	475	310(typ)	475	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	220(typ)	350	220(typ)	350	
Fall Time	t_f	V_{GS}=10 V	240(typ)	375	240(typ)	375	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFK45N05, RFK45N06 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

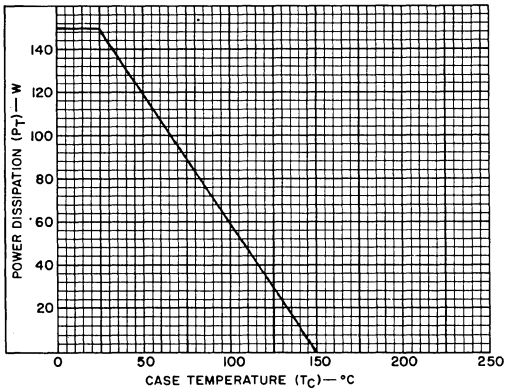
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK45N05		RFK45N06		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 22.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	150(typ.)		150(typ.)		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.



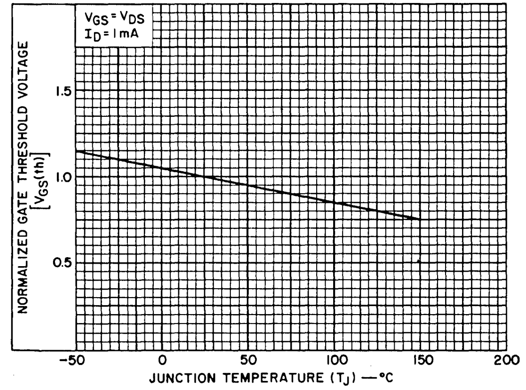
92CS-37137

Fig. 1 — Maximum safe operating areas for all types.



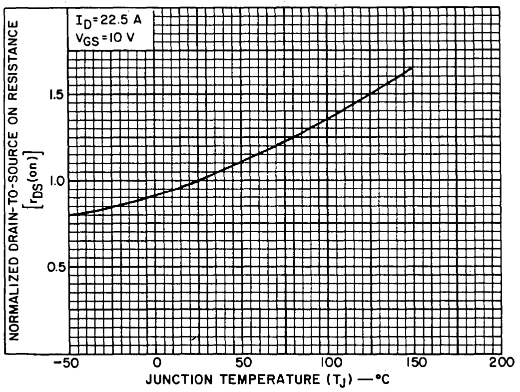
92CS-37138

Fig. 2 — Power vs. temperature derating curve for all types.



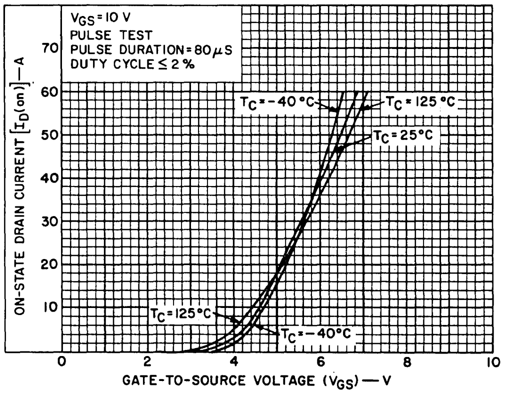
92CS-37144

Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.



92CS-37139

Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.



92CS-37140

Fig. 5 — Typical transfer characteristics for all types.

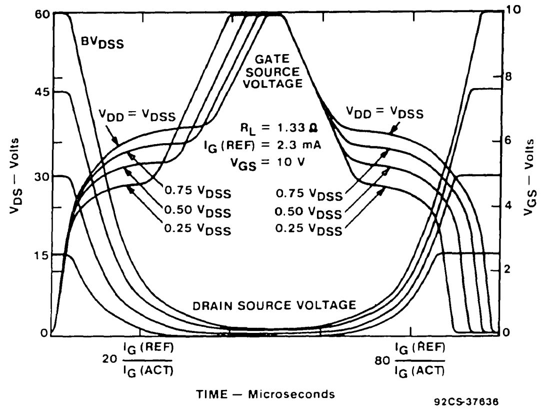


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

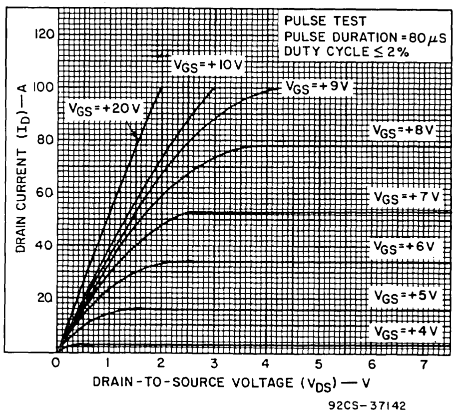


Fig. 7 — Typical saturation characteristics for all types.

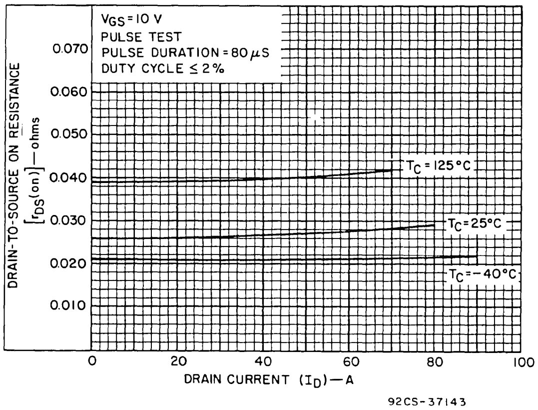


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

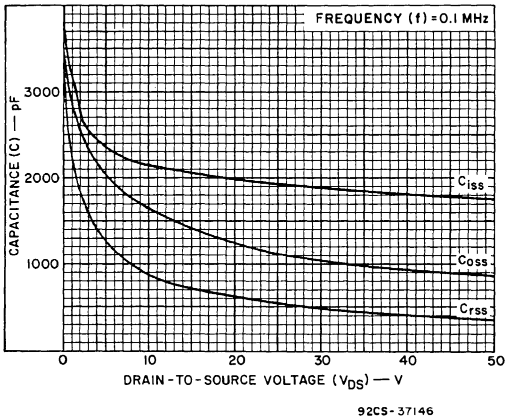


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

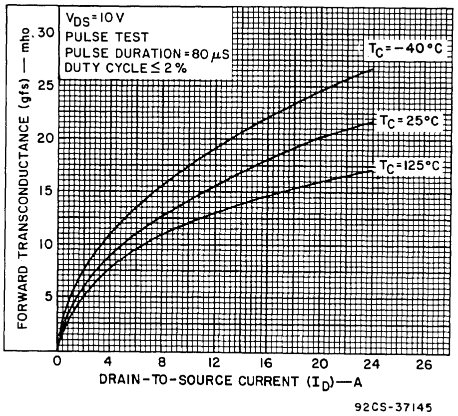


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

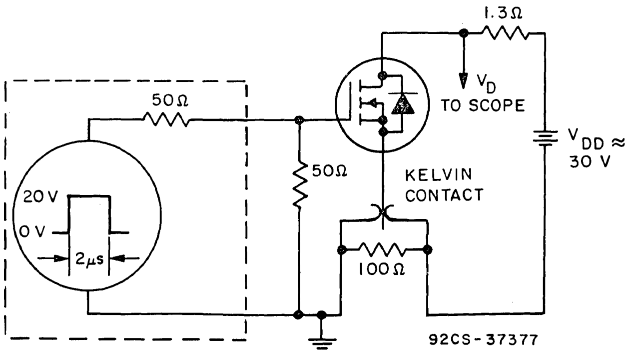


Fig. 11 - Switching Time Test Circuit.

IRF130-133, IRF251-253, IRF420-423,
IRF510-513, IRF520-523, IRF530-533

File Number **1469**

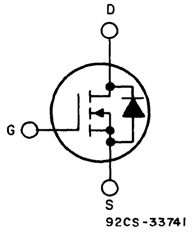
N-Channel Enhancement-Mode Silicon Gate Power Field-Effect Transistors

3.5-14 A, 60-500 V

Features:

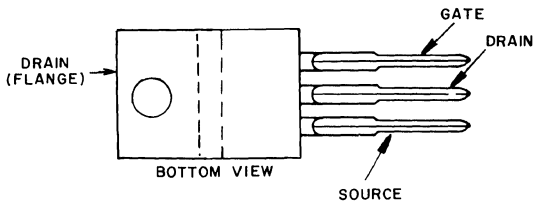
- *Silicon gate for fast switching speeds - specified switching times at elevated temperatures*
- *Rugged - SOA is power-dissipation limited*
- *Low drive requirement, $V_{GS(th)}$ = 4 V (max.)*

The n-channel enhancement-mode silicon-gate power field-effect transistors are designed for high-voltage, high-speed power-switching applications, such as line-operated switching regulators, converters, solenoid and relay drivers.

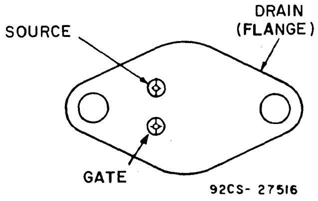


N-CHANNEL ENHANCEMENT MODE

TERMINAL DESIGNATIONS



JEDEC TO-220AB



JEDEC TO-204AE, AA

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

DRAIN-SOURCE VOLTAGE	V_{DSS}	See Table 2, TO-204AA, AE	V
		See Table 3, TO-220AB	V
GATE-SOURCE VOLTAGE	V_{GS}	± 20	V
DRAIN CURRENT	I_D	See Table 2, TO-204AA, AE	A
		See Table 3, TO-220AB	A
POWER DISSIPATION @ T_C = 25°C	P_T	See Table 2, TO-204AA, AE	W
		See Table 3, TO-220AB	W
Derate above T_C = 25°C		See Table 2, TO-204AA, AE	W/°C
		See Table 3, TO-220AB	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150	°C
THERMAL CHARACTERISTICS			
THERMAL RESISTANCE (Junction-to-Case)	$R_{\theta JC}$	See Table 2, TO-204AA, AE	°C/W
		See Table 3, TO-220AB	°C/W
MAXIMUM LEAD TEMPERATURE FOR SOLDERING PURPOSES, 1/8 in. from case for 5 seconds	T_L	275	°C

Table 2 - TO-204AA, AE (Formerly TO-3)

Device	MAXIMUM RATINGS					ELECTRICAL CHARACTERISTICS						
	V_{DSS} (Volts)	I_D (Amp)	P_T (Watts)	Derating Factor W/°C	$R_{\theta JC}$ °C/W	$r_{DS(on)}$ (Ohm) Max.	@ I_D (Amp)	$V_{GS(th)}$ (Volts) Min./Max.	g_{fs} (mho) Min.	t_{on} (ns) Typ.	t_{off} (ns) Typ.	@ I_D (Amp)
IRF130	100	14	75	0.6	1.67	0.18	8	2/4	4	115	130	8
IRF131	60											
IRF132	100	12				0.25						
IRF133	60											
* IRF251	150	30	150	1.2	0.833	.085	15		8	500	550	15
* IRF253	150	25				.120						
IRF420	500	2.5	40	0.32	3.12	3.0	1.5		1	105	210	1.5
IRF421	450											
IRF422	500	2.0										
IRF423	450											

* 60 mil leads

Table 3 - TO-220AB

Device	MAXIMUM RATINGS					ELECTRICAL CHARACTERISTICS						
	V_{DSS} (Volts)	I_D (Amp)	P_T (Watts)	Derating Factor W/°C	$R_{\theta JC}$ °C/W	$r_{DS(on)}$ (Ohm) Max.	@ I_D (Amp)	$V_{GS(th)}$ (Volts) Min./Max.	g_{fs} (mho) Min.	t_{on} (ns) Typ.	t_{off} (ns) Typ.	@ I_D (Amp)
IRF510	100	4	20	0.16	6.25	0.6	2	2/4	1	75	155	2
IRF511	60											
IRF512	100	3.5				0.8						
IRF513	60											
IRF520	100	8	40	0.32	3.12	0.3	4		1.5	90	145	4
IRF521	60											
IRF522	100	7				0.4						
IRF523	60											
IRF530	100	14	75	0.6	1.67	0.18	8		4	115	130	8
IRF531	60											
IRF532	100	12				0.25						
IRF533	60											

Logic-Level FETs

Compatibility of L^2FETs with Logic Circuits

The "Logic-Level," or L^2, portion of the name for the L^2FET MOSFETs reflects their compatability with the 5-volt power-supply requirement of logic circuitry. An L^2FET does not require an interface circuit between it and the CMOS logic driver; therefore, the extra cost of the interface circuit power supply is eliminated.

The chief physical structural difference between the L^2FET and other MOSFETs, and the electrical reason for its difference in performance, is its gate insulation thickness, which has been reduced from the 100 nanometers standard in the industry to 50 nanometers (500 angstroms), yet which retains the dynamic strength to handle the high voltages applied to power transistors. Since the surface inversion of the MOS channel is determined by the gate-insulator voltage field, the halving of the gate-oxide thickness should be expected to have a major effect on the gate voltage required. In fact, the reduction in gate insulator thickness is the reason for the reduction in voltage to 5 volts from the 10 volts of the standard MOSFET.

Tight control of the temperature-versus-time and oxygen-versus-time profiles applied to the silicon substrate during oxide growth assures consistent L^2FET performance through the development of good transition regions between the oxide, the silicon below it, and the polysilicon above it. The reduction in gate insulator thickness makes possible easy on/off control of the L^2FETs by CMOS logic alone, and by microprocessors. Yet the on-resistance, drain current rating, and blocking voltage capability are consistent with other RCA MOSFETs.

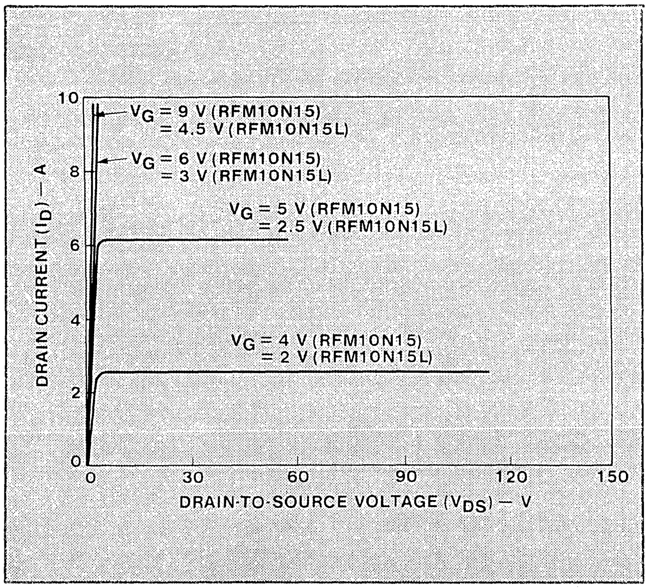
Although it might be expected that halving the gate-oxide thickness would double the gate capacitance and halve the switching speed, measurements demonstrate a 2:1 increase in switching speed for the L^2FET over the 10-volt MOSFET when gate drive power is the same for both devices. For example, the rise time of a 10-volt MOSFET is typically 120 ns, that of an L^2FET, 60ns, even though drain-to-gate feedback capacitance is higher than in the 10-volt type.

Comparison of L^2FET and standard Power MOSFET Characteristics

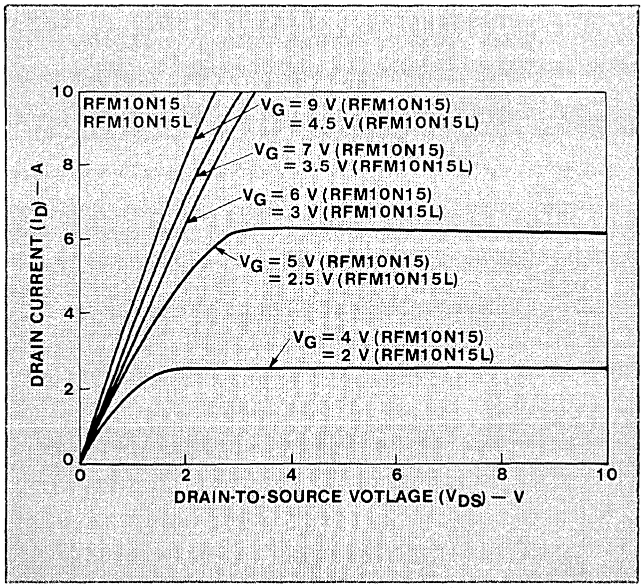
A comparison of L^2FETs with standard power MOSFETs show that for L^2FETs the threshold voltage-temperature coefficient is half that of a standard MOSFET having the same drain-to-source on resistance and voltage rating, the threshold temperature in mV/° C is scaled down, the current level for zero temperature coefficient is unchanged, and that the transconductance is twice that of a standard MOSFET.

A plot of the drain voltage as a function of time of the RFM10N15 standard power MOSFET and the RFM10N15L L^2FET, when each is driven with a 5 ampere, 75-volt resistive load line, shows that the rise and fall times of the devices are not symmetrical, and that the L^2FET is faster. Moreover, the dynamic saturation voltage of the L^2FET is 4 volts instead of the 8 volts typical of standard MOSFETs.

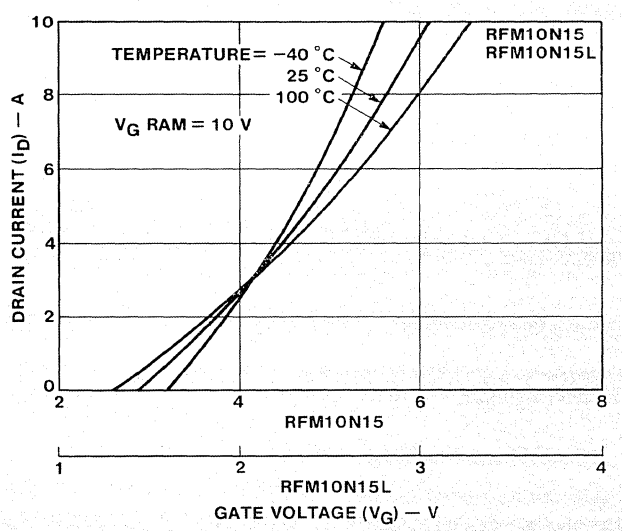
If the standard MOSFET and the L^2FET are both driven from a current generator, where $I_g(on)=I_g(off)$ with gate voltage limits of zero and 10 or 5 volts, the rise and fall times of the devices are the same with current drive, and the two devices have similar output waveforms in most regions.



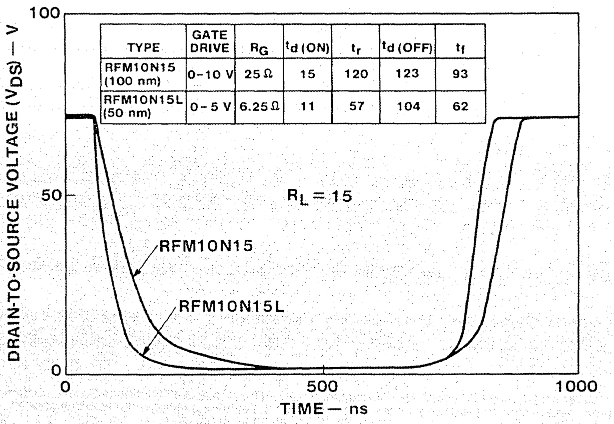
Drain current as a function of drain voltage for L^2FETs and standard MOSFETs at high voltage.



Drain current as a function of drain voltage for L^2FETs and standard MOSFETs at low voltages.

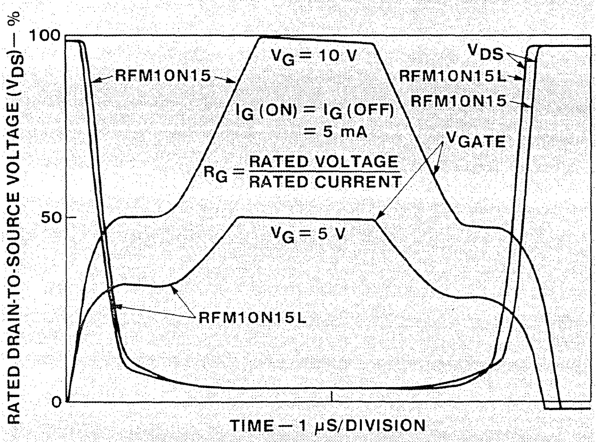


Drain current as a function of gate voltage for L²FETs and standard MOSFETs.



TYPE	GATE DRIVE	R_G	$t_{d(ON)}$	t_r	$t_{d(OFF)}$	t_f
RFM10N15 (100 nm)	0-10 V	25 Ω	15	120	123	93
RFM10N15L (50 nm)	0-5 V	6.25 Ω	11	57	104	62

Drain voltage turn-on waveforms for L²FETs and standard MOSFETs.



Drain voltage switching waveforms for L²FETs and standard MOSFETs.

RFL1N08L, RFL1N10L, RFP2N08L, RFP2N10L

File Number **1510**

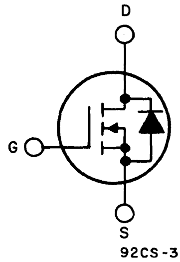
N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

1 and 2 A, 80 V and 100 V

$r_{DS(on)}$: 1.25 Ω and 1.4 Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

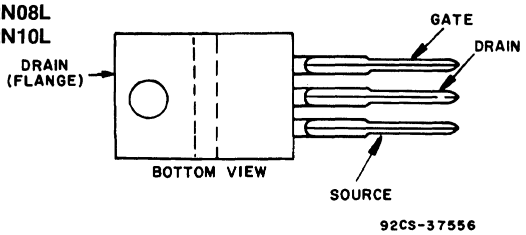
The RFL1N08L and RFL1N10L and the RFP2N08L and RFP2N10L are n-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFL-series types are supplied in the JEDEC TO-39 metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFL and RFP series were formerly RCA developmental numbers TA9524 and TA9525.

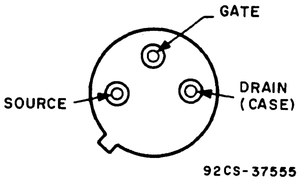
TERMINAL DESIGNATIONS

RFP2N08L
RFP2N10L



JEDEC TO-220AB

RFL1N08L
RFL1N10L



JEDEC TO-39

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFL1N08L	RFL1N10L		RFP2N08L	RFP2N10L	
DRAIN-SOURCE VOLTAGE .... V_{DSS}	80	100		80	100	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) .... V_{DGR}	80	100		80	100	V
GATE-SOURCE VOLTAGE .... V_{GS}			±10			V
DRAIN CURRENT, RMS Continuous ...... I_D	1	1		2	2	A
Pulsed .... I_{DM}			5			A
POWER DISSIPATION @ T_C=25° C .... P_T	8.33	8.33		25	25	W
Derate above T_C=25° C	0.0667	0.0667		0.2	0.2	W/° C
OPERATING AND STORAGE TEMPERATURE .... T_j, T_{stg}			-55 to +150			° C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS				UNITS
				RFL1N08L RFP2N08L		RFL1N10L RFP2N10L		
				MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DDS}	I_D=1 mA V_{GS}=0		80	—	100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA		1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V		—	1	—	—	µA
		V_{DS}=80 V		—	—	—	1	
		T_C=125° C V_{DS}=65 V		—	50	—	—	
		V_{DS}=80 V		—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±10 V V_{DS}=0		—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)^a$	I_D=1 A	RFP	—	1.25	—	1.25	V
		V_{GS}=5 V	RFL	—	1.4	—	1.4	
		I_D=2 A	RFP	—	3.0	—	3.0	
		V_{GS}=5 V	RFL	—	3.3	—	3.3	
Static Drain-Source On Resistance	$r_{DS}(on)^a$	I_D=1 A	RFP	—	1.25	—	1.25	Ω
		V_{GS}=5 V	RFL	—	1.4	—	1.4	
Forward Transconductance	g_{fs}^a	V_{DS}=15 V I_D=1 A		1400 (typ)		1400 (typ)		mmho
Input Capacitance	C_{iss}	V_{DS}=25 V		—	200	—	200	pF
Output Capacitance	C_{oss}	V_{GS}=0 V		—	80	—	80	
Reverse-Transfer Capacitance	C_{rss}	f=0.1 MHz		—	20	—	20	
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V I_D=1 A R_{gen}=∞ R_{gs}=6.25 Ω V_{GS}=5 V		10(typ)	25	10(typ)	25	ns
Rise Time	t_r			15(typ)	45	15(typ)	45	
Turn-Off Delay Time	$t_d(off)$			25(typ)	45	25(typ)	45	
Fall Time	t_f			20(typ)	25	20(typ)	25	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFL1N08L, RFL1N10L		—	15	—	15	°C/W
		RFP2N08L, RFP2N10L		—	5	—	5	

[a]Pulsed: Pulse duration = 300 µs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL1N08L RFP2N08L		RFL1N10L RFP2N10L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=1 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=2 A d_{IF}/d_t=50 A/µs	100(typ)		100(typ)		ns

*Pulse Test: Width ≤ 300 µs, duty cycle ≤ 2%.

RFL1N08L, RFL1N10L, RFP2N08L, RFP2N10L

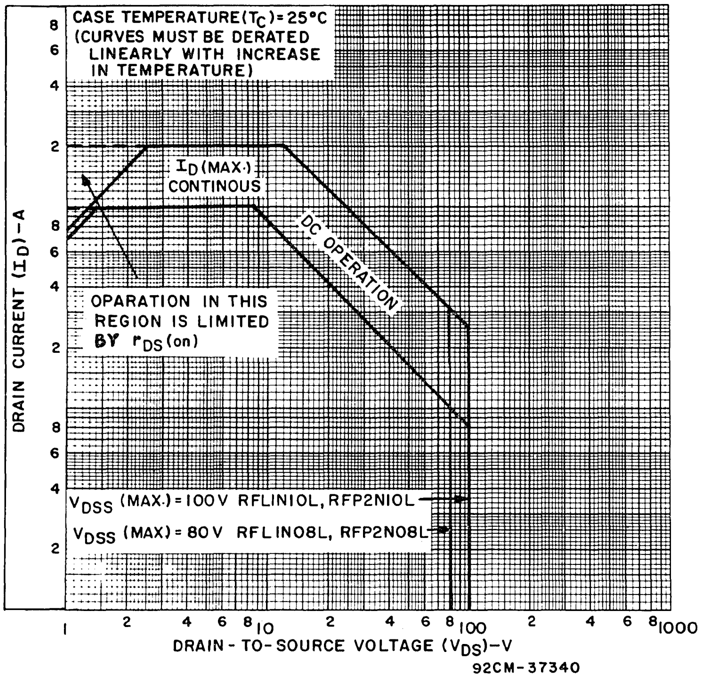


Fig. 1 — Maximum operating areas for all types.

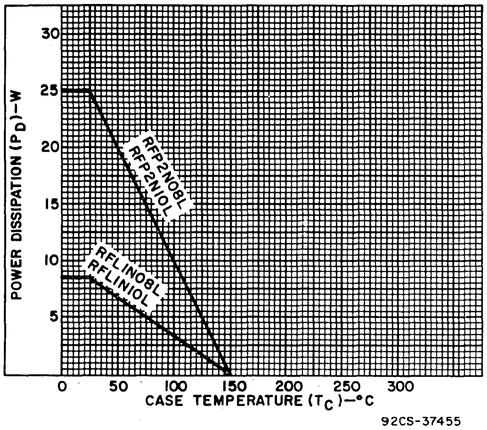


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

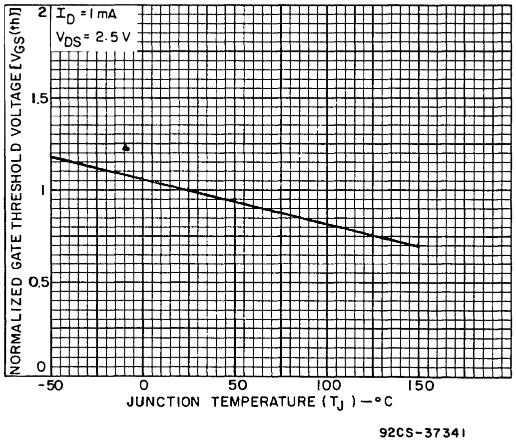


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

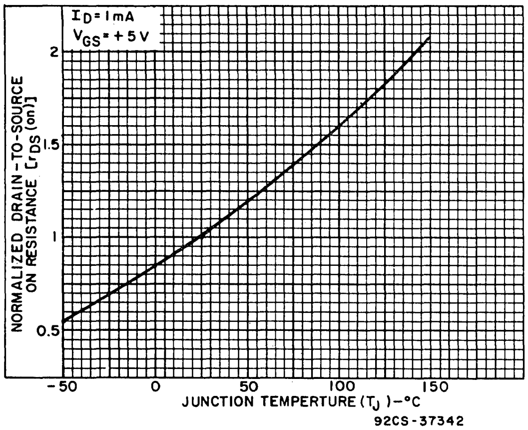


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

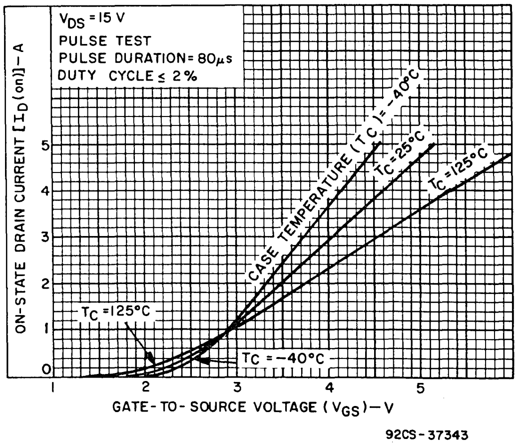


Fig. 5 — Typical transfer characteristics for all types.

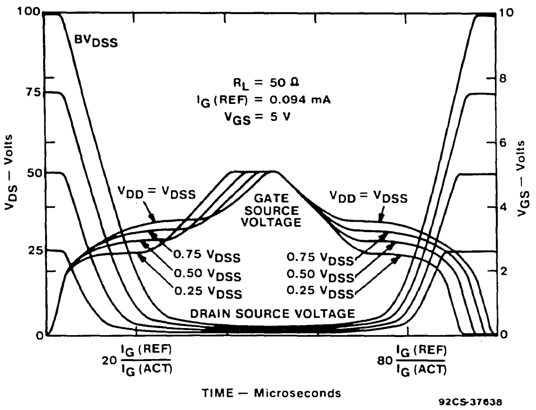


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

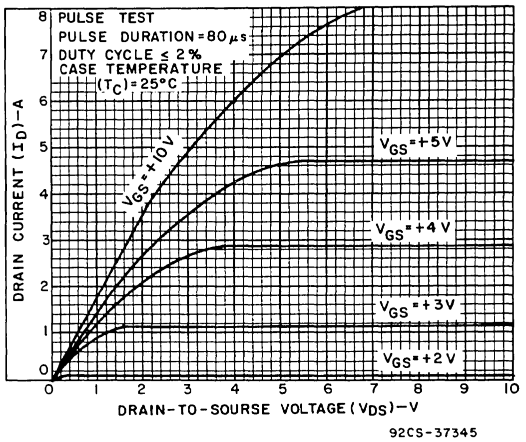


Fig. 7 — Typical saturation characteristics for all types.

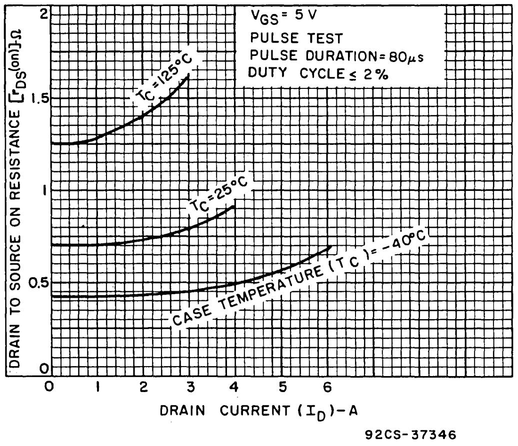


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

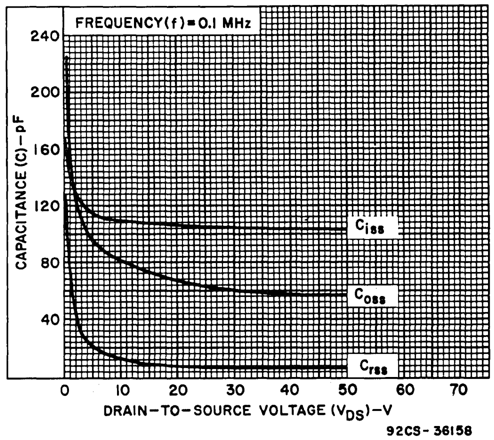


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

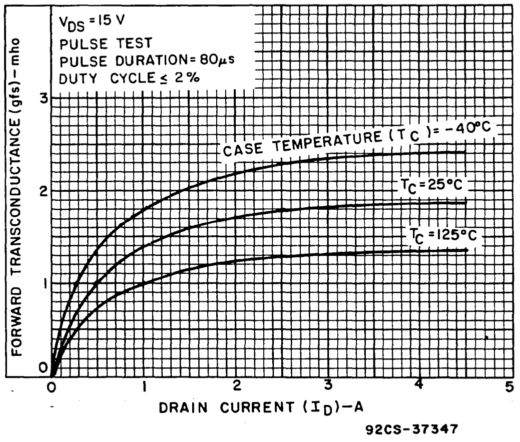


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

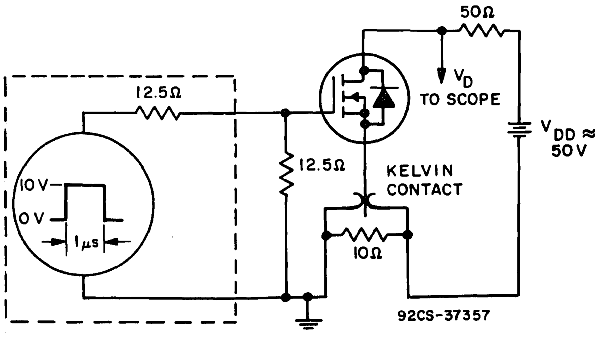


Fig. 11 — Switching Time Test Circuit.

RFL1N12L, RFL1N15L, RFP2N12L, RFP2N15L

File Number **1513**

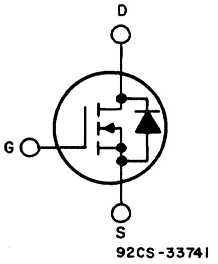
N-Channel Logic Level Power Field-Effect Transistors (L² FET)

1 and 2 A, 120 V and 150 V

$r_{DS(on)}$: 2 Ω and 2.15 Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

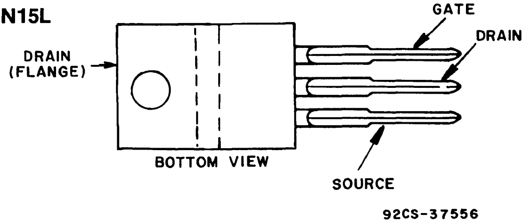
The RFL1N12L and RFL1N15L and the RFP2N12L and RFP2N15L are n-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFL-series types are supplied in the JEDEC TO-39 metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFL and RFP series were formerly RCA developmental numbers TA9528 and TA9529.

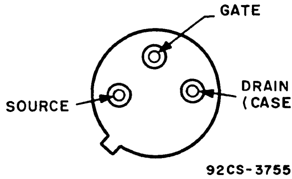
TERMINAL DESIGNATIONS

RFP2N12L
RFP2N15L



JEDEC TO-220AB

RFL1N12L
RFL1N15L



JEDEC TO-39

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFL1N12L	RFL1N15L		RFP1N12L	RFP2N15L	
DRAIN-SOURCE VOLTAGE	V_{DSS}	120	150		120	150	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ)	V_{DGR}	120	150		120	150	V
GATE-SOURCE VOLTAGE	V_{GS}			±10			V
DRAIN CURRENT, RMS Continuous	I_D	1	1		2	2	A
Pulsed	I_{DM}			5			A
POWER DISSIPATION @ T_C=25° C	P_T	8.33	8.33		25	25	W
Derate above T_C=25° C		0.0667	0.0667		0.2	0.2	W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}			–55 to +150			° C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS				UNITS
				RFL1N12L RFP2N12L		RFL1N15L RFP2N15L		
				MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DDS}	I_D=1 mA V_{GS}=0		120	—	150	—	V
Gate Threshold Voltage	V_{GS}(th)	V_{GS}=V_{DS} I_D=2 mA		1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100 V		—	1	—	—	μA
		V_{DS}=120 V		—	—	—	1	
		T_C=125° C V_{DS}=100 V		—	50	—	—	
		V_{DS}=120 V		—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±10 V V_{DS}=0		—	100	—	100	nA
Drain-Source On Voltage	V_{DS}(on)[a]	I_D=1 A	RFP	—	2	—	2	V
		V_{GS}=5 V	RFL	—	2.15	—	2.15	
		I_D=2 A	RFP	—	6	—	6	
		V_{GS}=5 V	RFL	—	6.3	—	6.3	
Static Drain-Source On Resistance	r_{DS}(on)[a]	I_D=1 A	RFP	—	2	—	2	Ω
		V_{GS}=5 V	RFL	—	2.15	—	2.15	
Forward Transconductance	g_{fs}[a]	V_{DS}=15 V I_D=1 A		1400 (typ)		1400 (typ)		mmho
Input Capacitance	C_{iss}	V_{DS}=25 V		—	200	—	200	pF
Output Capacitance	C_{oss}	V_{GS}=0 V		—	80	—	80	
Reverse-Transfer Capacitance	C_{rss}	f=0.1 MHz		—	20	—	20	
Turn-On Delay Time	t_d(on)	V_{DD}=75 V		10(typ)	25	10(typ)	25	ns
Rise Time	t_r	I_D=1 A		10(typ)	45	10(typ)	45	
Turn-Off Delay Time	t_d(off)	R_{gen}=∞ R_{gs}=6.25 Ω		24(typ)	45	24(typ)	45	
Fall Time	t_f	V_{GS}=5 V		20(typ)	25	20(typ)	25	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFL1N12L, RFL1N15L		—	15	—	15	°C/W
		RFP2N12L, RFP2N15L		—	5	—	5	

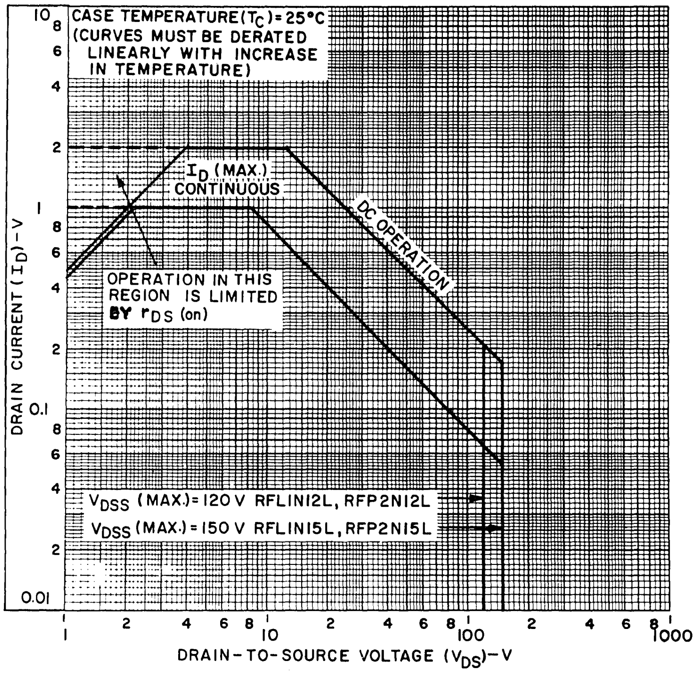
[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL1N12L RFP2N12L		RFL1N15L RFP2N15L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=1 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=2 A d_{IF}/d_t=50 A/μs	150(typ)		150(typ)		ns

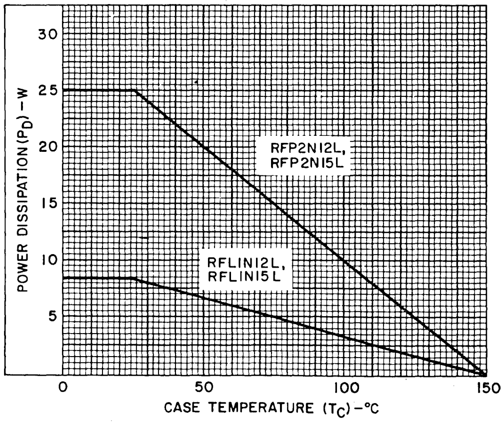
*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFL1N12L, RFL1N15L, RFP2N12L, RFP2N15L



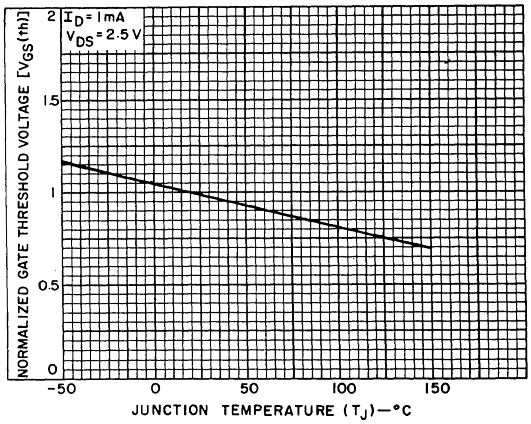
92CM-37332

Fig. 1 — Maximum operating areas for all types.



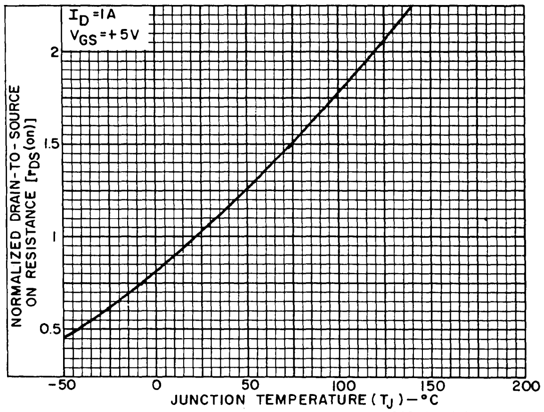
92CS-37503

Fig. 2 — Power dissipation vs. case temperature derating curve for all types.



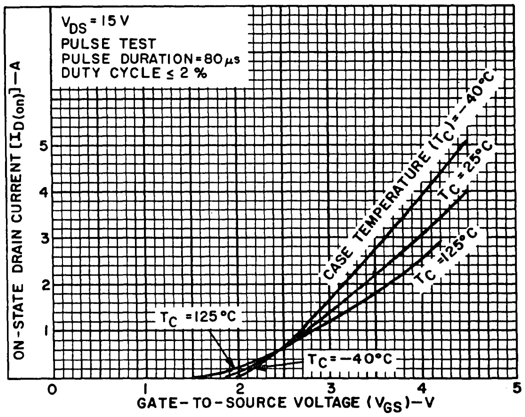
92CS-37333

Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.



92CS-37334

Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.



92CS-34335

Fig. 5 — Typical transfer characteristics for all types.

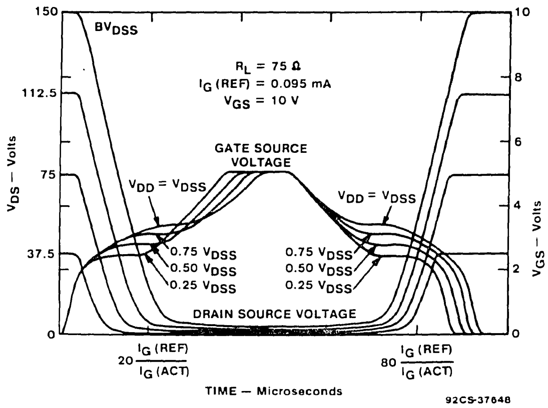


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

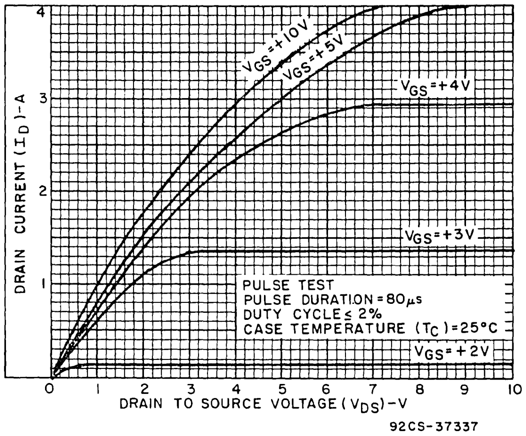


Fig. 7 — Typical saturation characteristics for all types.

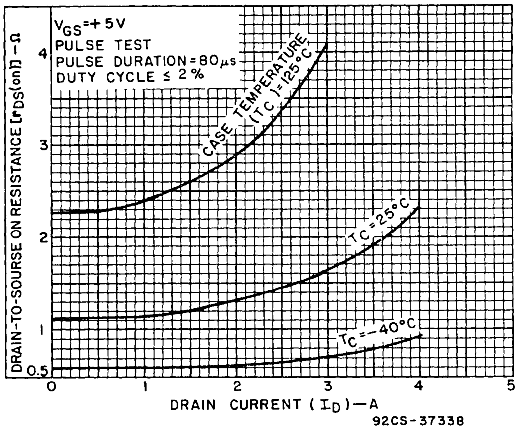


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

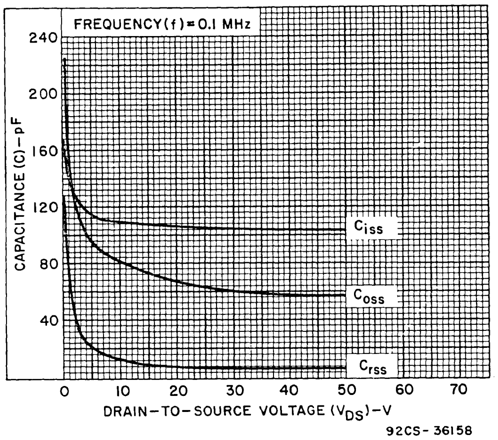


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

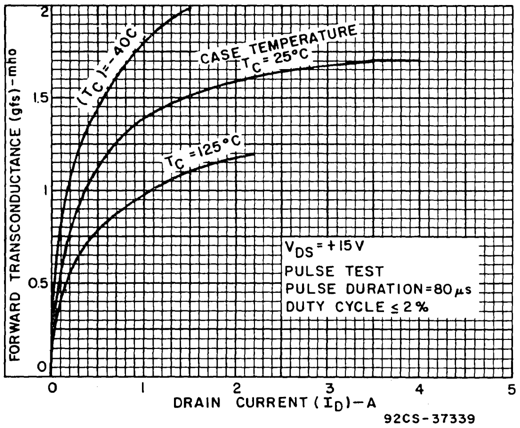


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

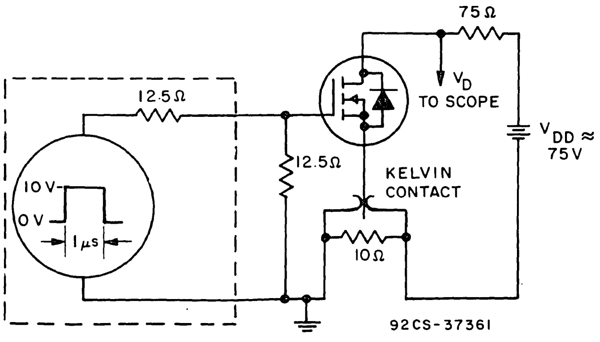


Fig. 11 — Switching Time Test Circuit.

RFL1N18L, RFL1N20L, RFP2N18L, RFP2N20L

File Number **1511**

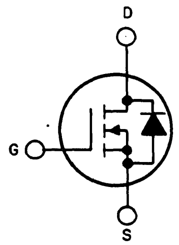
N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

1 and 2 A, 180 V and 200 V

$r_{DS(on)}$: 3.5 Ω and 3.65 Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



92CS-33741

N-CHANNEL ENHANCEMENT MODE

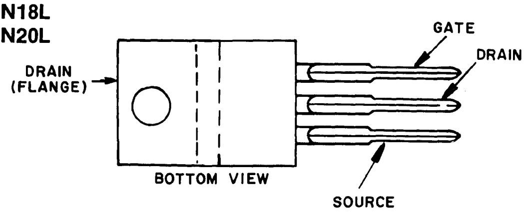
The RFL1N18L and RFL1N20L and the RFP2N18L and RFP2N20L are n-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFL-series types are supplied in the JEDEC TO-39 metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFL and RFP series were formerly RCA developmental numbers TA9532 and TA9533.

TERMINAL DESIGNATIONS

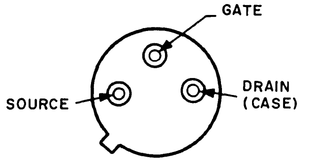
RFP2N18L
RFP2N20L



92CS-37556

JEDEC TO-220AB

RFL1N18L
RFL1N20L



92CS-37555

JEDEC TO-39

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFL1N18L	RFL1N20L		RFP2N18L	RFP2N20L	
DRAIN-SOURCE VOLTAGE	V_{DSS}	180	200		180	200	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ)	V_{DGR}	180	200		180	200	V
GATE-SOURCE VOLTAGE	V_{GS}			±10			V
DRAIN CURRENT, RMS Continuous	I_D	1	1		2	2	A
Pulsed	I_{DM}			4			A
POWER DISSIPATION @ T_C=25°C	P_T	8.33	8.33		25	25	W
Derate above T_C=25° C		0.0667	0.0667		0.2	0.2	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}			-55 to +150			°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS				UNITS
				RFL1N18L RFP2N18L		RFL1N20L RFP2N20L		
				MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DDS}	I_D=1 mA V_{GS}=0		180	—	200	—	V
Gate Threshold Voltage	$V_{GS}(th)$	$V_{GS}=V_{DS}$ I_D=1 mA		1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V		—	1	—	—	µA
		V_{DS}=160 V		—	—	—	1	
		T_C=125° C V_{DS}=145 V		—	50	—	—	
		V_{DS}=160 V		—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm10$ V V_{DS}=0		—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)^a$	I_D=1 A	RFP	—	3.5	—	3.5	V
		V_{GS}=5 V	RFL	—	3.65	—	3.65	
		I_D=2 A	RFP	—	9	—	9	
		V_{GS}=5 V	RFL	—	9.3	—	9.3	
Static Drain-Source On Resistance	$r_{DS}(on)^a$	I_D=1 A	RFP	—	3.5	—	3.5	Ω
		V_{GS}=5 V	RFL	—	3.65	—	3.65	
Forward Transconductance	g_{fs}^a	V_{DS}=15 V I_D=1 A		1200 (typ)		1200 (typ)		mmho
Input Capacitance	C_{iss}	V_{DS}=25 V		—	200	—	200	pF
Output Capacitance	C_{oss}	V_{GS}=0 V		—	60	—	60	
Reverse-Transfer Capacitance	C_{rss}	f=0.1 MHz		—	20	—	20	
Turn-On Delay Time	$t_d(on)$	V_{DD}=100 V		10(typ)	25	10(typ)	25	ns
Rise Time	t_r	I_D=1 A		10(typ)	30	10(typ)	30	
Turn-Off Delay Time	$t_d(off)$	$R_{gen}=\infty$ R_{gs}=6.25 Ω		25(typ)	40	25(typ)	40	
Fall Time	t_f	V_{GS}=5 V		20(typ)	25	20(typ)	25	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFL1N18L, RFL1N20L		—	15	—	15	°C/W
		RFP2N18L, RFP2N20L		—	5	—	5	

[a]Pulsed: Pulse duration = 300 µs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL1N18L RFP2N18L		RFL1N20L RFP2N20L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=1 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=2 A d_{IF}/d_t=50 A/µs	200(typ)		200(typ)		ns

*Pulse Test: Width ≤ 300 µs, duty cycle ≤ 2%.

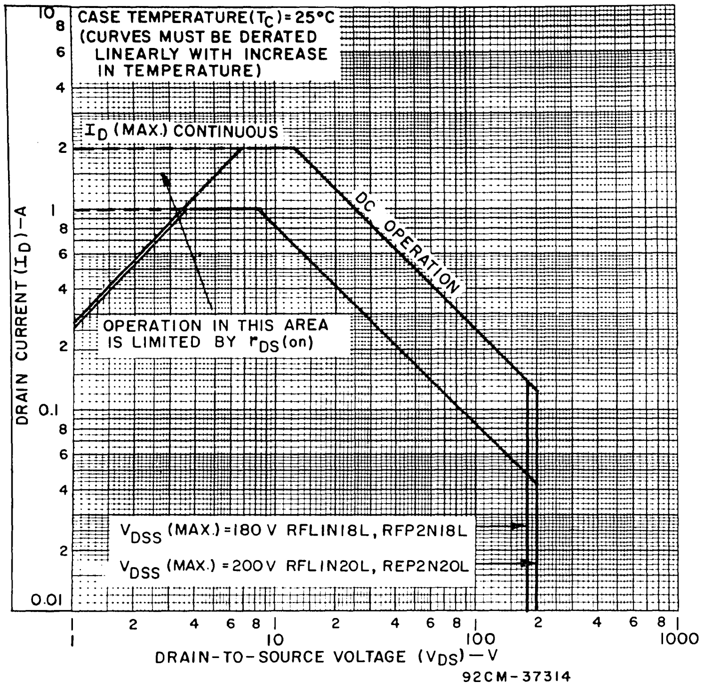


Fig. 1 — Maximum operating areas for all types.

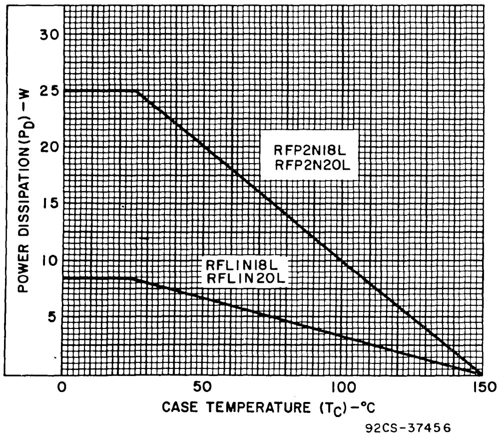


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

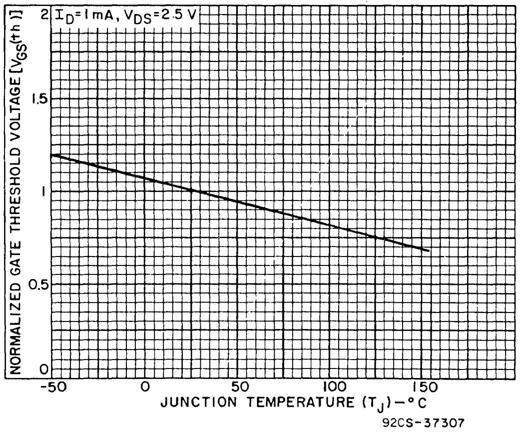


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

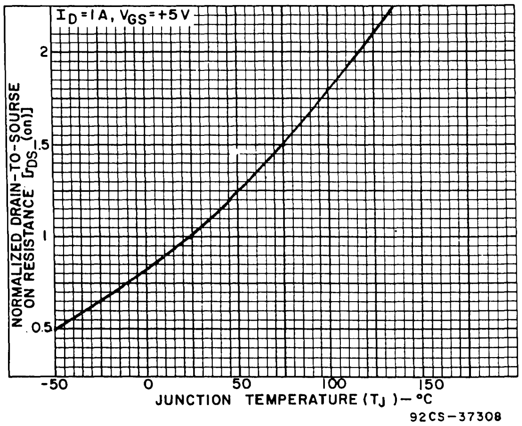


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

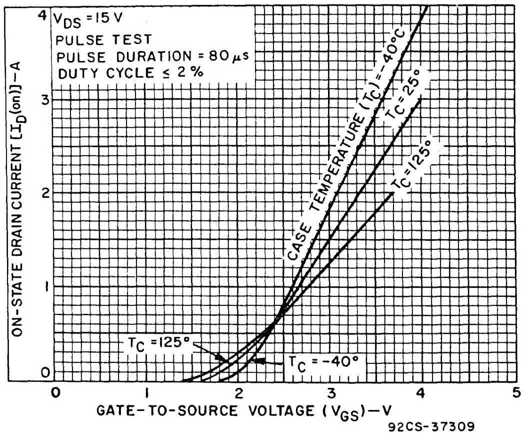


Fig. 5 — Typical transfer characteristics for all types.

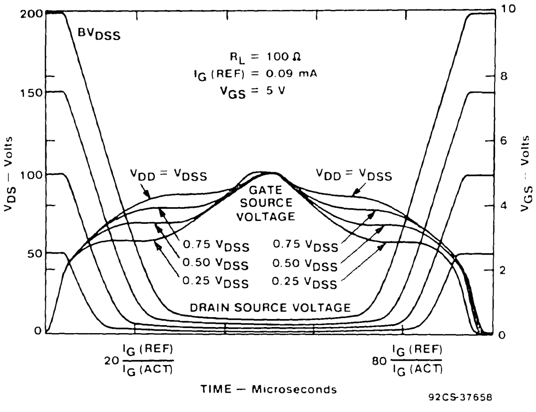


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

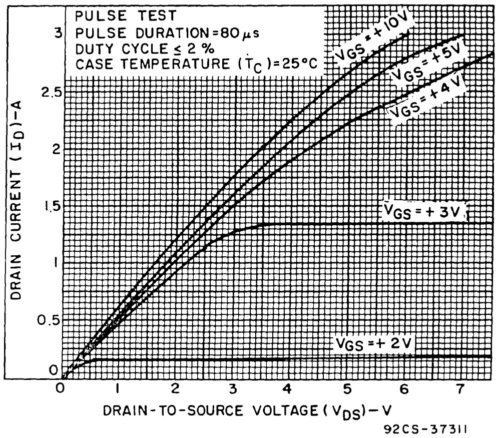


Fig. 7 — Typical saturation characteristics for all types.

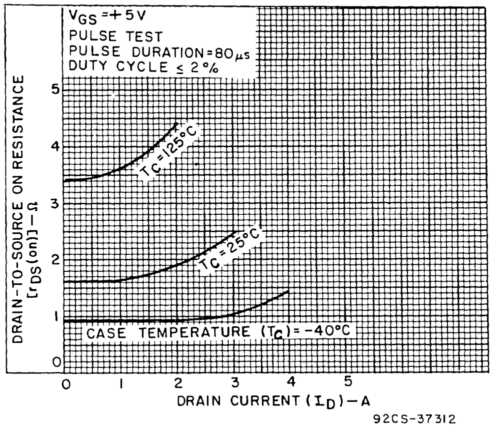


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

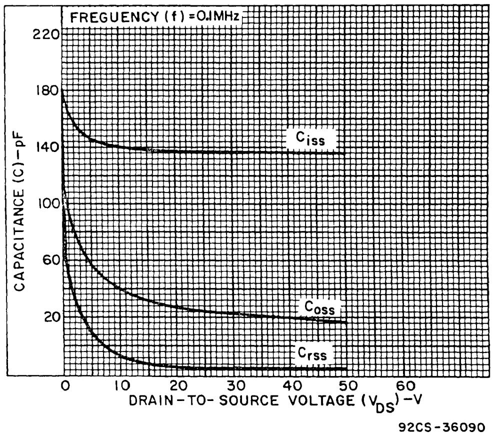


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

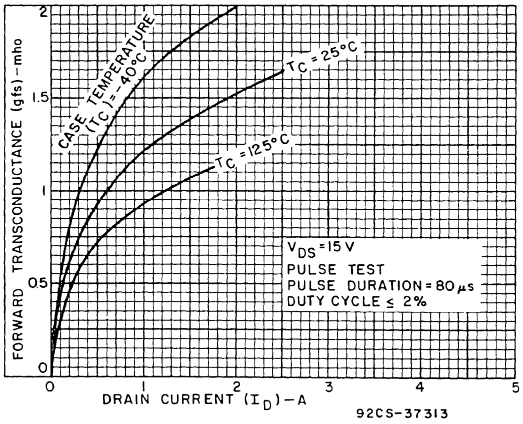


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

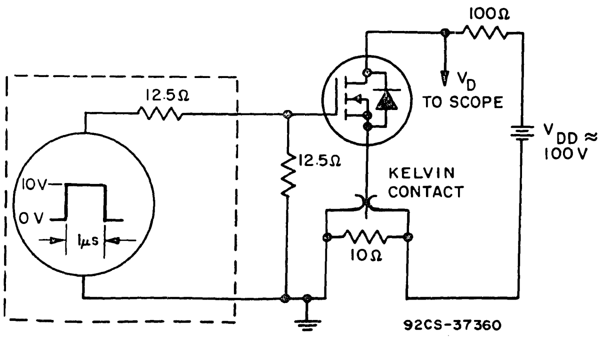


Fig. 11 — Switching Time Test Circuit.

RFM8N18L, RFM8N20L, RFP8N18L, RFP8N20L

File Number **1514**

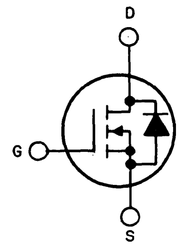
N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

12 A, 80 V and 100 V

$r_{DS(on)}$: 0.2 Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



92CS-33741

N-CHANNEL ENHANCEMENT MODE

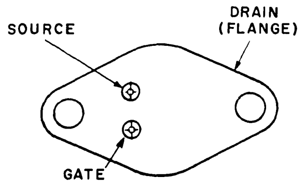
The RFM8N18L and RFM8N20L and the RFP8N18L and RFP8N20L are n-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFM-series types are supplied in the JEDEC TO-204MA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFM and RFP series were formerly RCA developmental numbers TA9534 and TA9535.

TERMINAL DESIGNATIONS

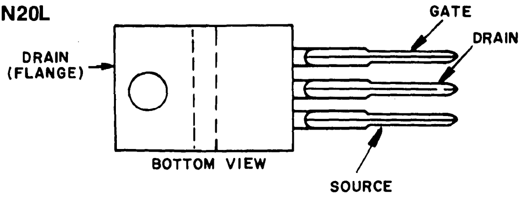
RFM8N18L
RFM8N20L



92CS-37553

JEDEC TO-204MA

RFP8N18L
RFP8N20L



92CS-37556

JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM8N18L	RFM8N20L		RFP8N18L	RFP8N20L	
DRAIN-SOURCE VOLTAGE .... V_{DSS}	180	200		180	200	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) .... V_{DGR}	180	200		180	200	V
GATE-SOURCE VOLTAGE .... V_{GS}			±10			V
DRAIN CURRENT, RMS Continuous ...... I_D			8			A
Pulsed .... I_{DM}			20			A
POWER DISSIPATION @ T_C=25° C .... P_T	75	75		60	60	W
Derate above T_C=25° C	0.6	0.6		0.48	0.48	W/° C
OPERATING AND STORAGE TEMPERATURE .... T_j, T_{stg}			-55 to +150			° C

RFM8N18L, RFM8N20L, RFP8N18L, RFP8N20L

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8N18L RFP8N18L		RFM8N20L RFP8N20L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DDS}	I_D=1 mA V_{GS}=0	180	—	200	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V	—	1	—	—	μA
		V_{DS}=160 V	—	—	—	1	
		T_C=125° C V_{DS}=145 V	—	50	—	—	
		V_{DS}=160 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)^a$	I_D=4 A V_{GS}=5 V	—	2.4	—	2.4	V
		I_D=8 A V_{GS}=5 V	—	5.5	—	5.5	
Static Drain-Source On Resistance	$r_{DS}(on)^a$	I_D=4 A V_{GS}=5 V	—	0.6	—	0.6	Ω
Forward Transconductance	g_{fs}^a	V_{DS}=10 V I_D=4 A	5.9 (typ)		5.9 (typ)		mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	750	—	750	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	250	—	250	
Reverse-Transfer Capacitance	C_{rss}	f=0.1 MHz	—	70	—	70	
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V	15(typ)	45	15(typ)	45	ns
Rise Time	t_r	I_D=6 A	45(typ)	150	45(typ)	150	
Turn-Off Delay Time	$t_d(off)$	$R_{gen}=\infty$ R_{gs}=6.25 Ω	100(typ)	135	100(typ)	135	
Fall Time	t_f	V_{GS}=5 V	60(typ)	105	60(typ)	105	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM8N18L, RFM8N20L	—	1.67	—	1.67	°C/W
		RFP8N18L, RFP8N20L	—	2.083	—	2.083	

[a] Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8N18L RFP8N18L		RFM8N20L RFP8N20L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=4 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	250(typ)		250(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM8N18L, RFM8N20L, RFP8N18L, RFP8N20L

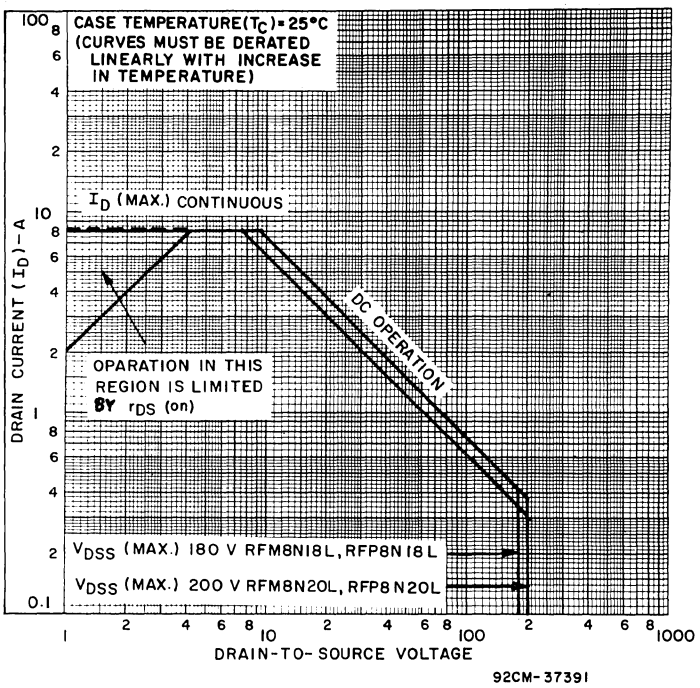


Fig. 1 — Maximum safe operating areas for all types.

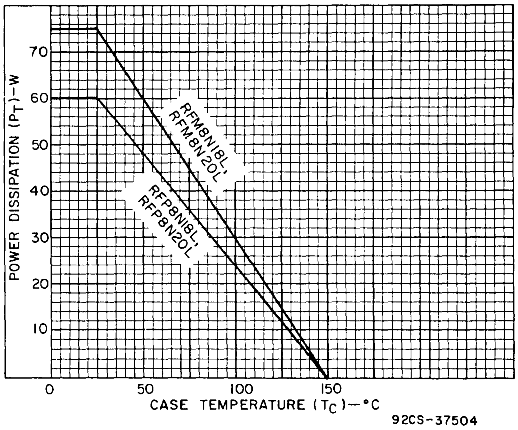


Fig. 2 — Power vs. temperature derating curve for all types.

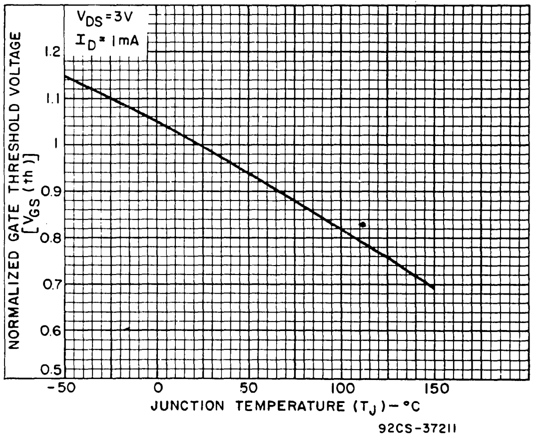


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

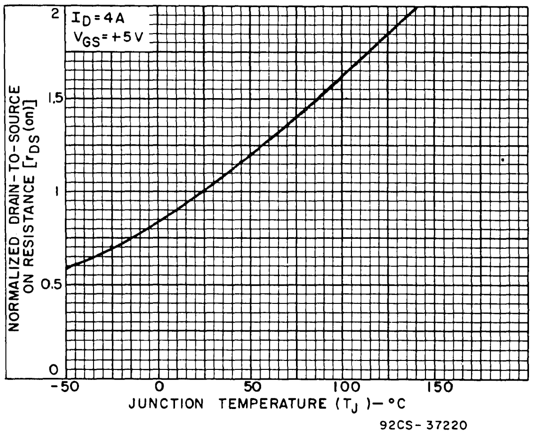


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

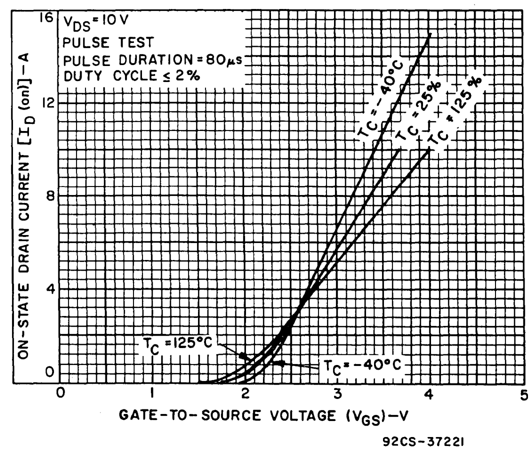


Fig. 5 — Typical transfer characteristics for all types.

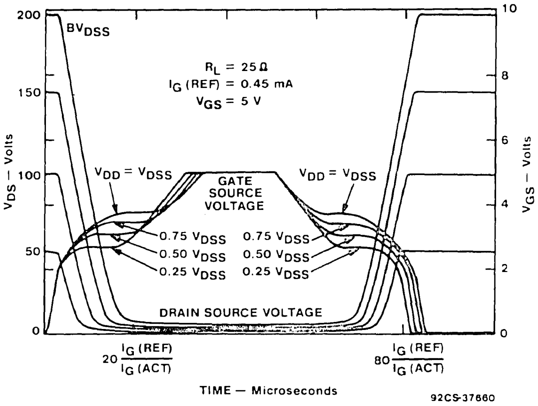


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

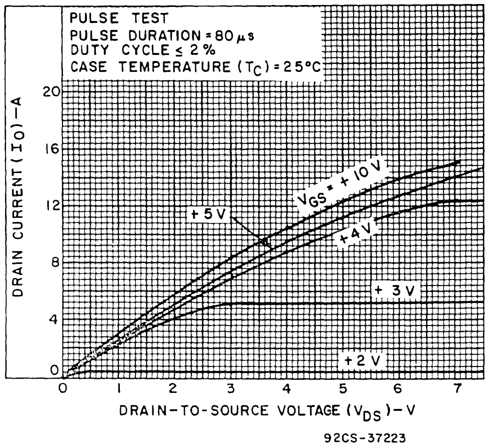


Fig. 7 — Typical saturation characteristics for all types.

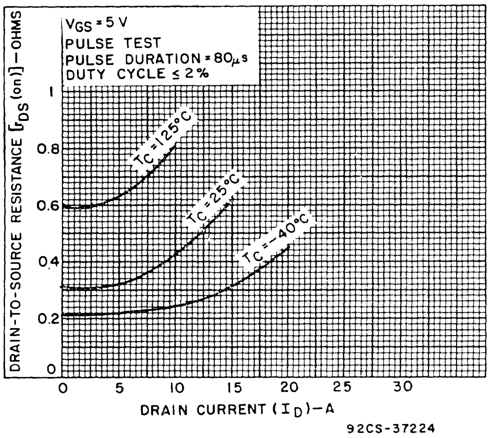


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

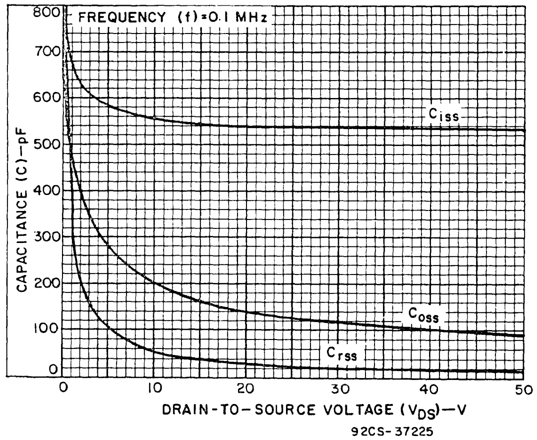


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

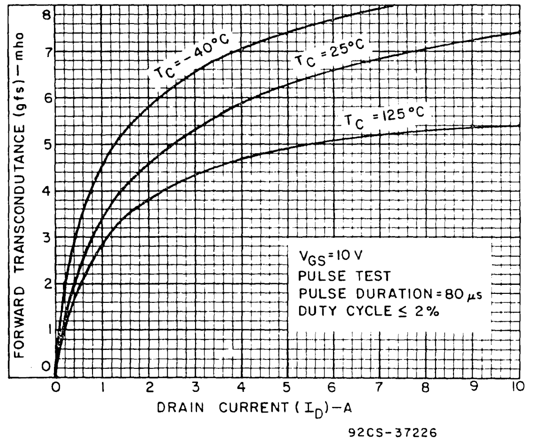


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

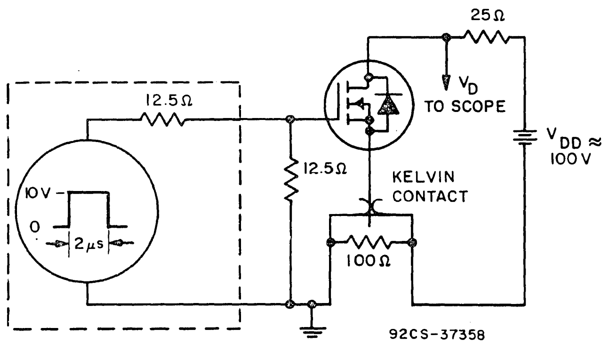


Fig. 11 — Switching Time Test Circuit.

RFM12N08L, RFM12N10L, RFP12N08L, RFP12N10L

File Number **1512**

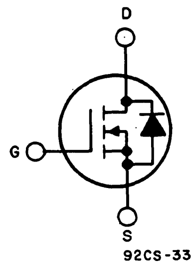
N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

8 A, 180 V and 200 V

$r_{DS(on)}$: 0.6 Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

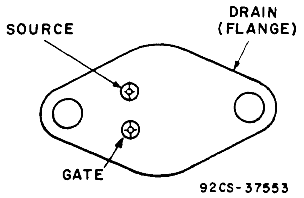
The RFM12N08L and RFM12N10L and the RFP12N08L and RFP12N10L are n-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFM-series types are supplied in the JEDEC TO-204MA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFM and RFP series were formerly RCA developmental numbers TA9526 and TA9527.

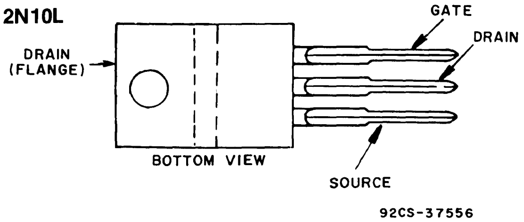
TERMINAL DESIGNATIONS

RFM12N08L
RFM12N10L



JEDEC TO-220AB

RFP12N08L
RFP12N10L



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFM12N08L	RFM12N10L		RFP12N08L	RFP12N10L	
DRAIN-SOURCE VOLTAGE	V_{DSS}	80	100		80	100	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ)	V_{DGR}	80	100		80	100	V
GATE-SOURCE VOLTAGE	V_{GS}			±10			V
DRAIN CURRENT, RMS Continuous	I_D			12			A
Pulsed	I_{DM}			30			A
POWER DISSIPATION @ T_C=25°C	P_T	75	75		60	60	W
Derate above T_C=25°C		0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}			-55 to +150			°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N08L RFP12N08L		RFM12N10L RFP12N10L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DDS}	I_D=1 mA V_{GS}=0	80	—	100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	$V_{GS}=V_{DS}$ I_D=1 mA	1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V V_{DS}=80 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=65 V V_{DS}=80 V	— —	50 —	— —	— 50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)^a$	I_D=6 A V_{GS}=5 V	—	1.2	—	1.2	V
		I_D=12 A V_{GS}=5 V	—	3.3	—	3.3	
Static Drain-Source On Resistance	$r_{DS}(on)^a$	I_D=6 A V_{GS}=5 V	—	0.2	—	0.2	Ω
Forward Transconductance	$g_{fs}{}^a$	V_{DS}=10 V I_D=6 A	7 (typ)		7 (typ)		mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	750	—	750	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	325	—	325	
Reverse-Transfer Capacitance	C_{rss}	f=0.1 MHz	—	100	—	100	
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V	15(typ)	50	15(typ)	50	ns
Rise Time	t_r	I_D=6 A R_{gen}=∞	70(typ)	150	70(typ)	150	
Turn-Off Delay Time	$t_d(off)$	R_{gs}=6.25 Ω	100(typ)	130	100(typ)	130	
Fall Time	t_f	V_{GS}=5 V	80(typ)	150	80(typ)	150	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM12N08L, RFM12N10L	—	1.67	—	1.67	°C/W
		RFP12N08L, RFP12N10L	—	2.083	—	2.083	

[a] Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N08L RFP12N08L		RFM12N10L RFP12N10L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

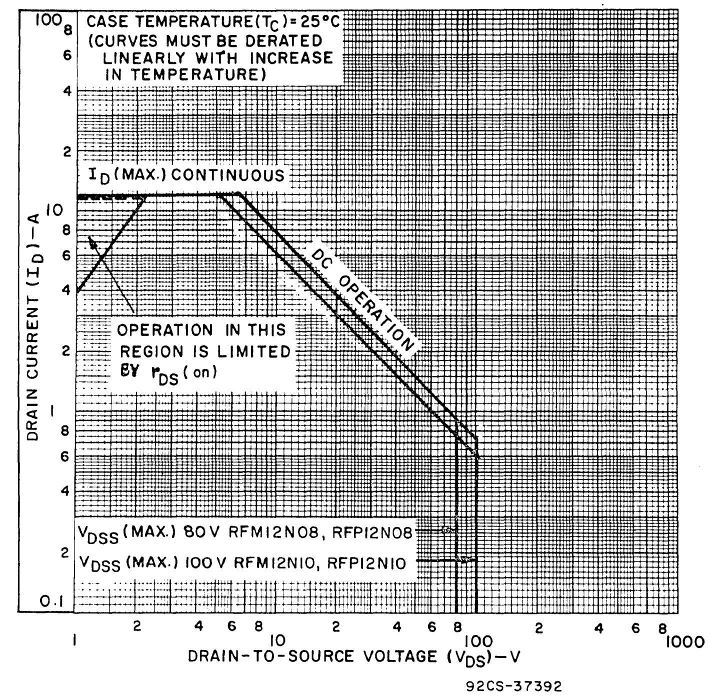


Fig. 1 — Maximum operating areas for all types.

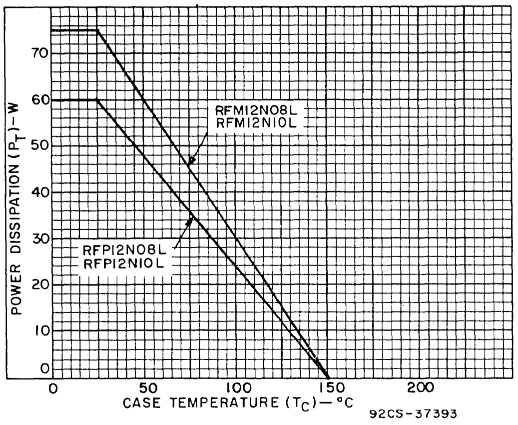


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

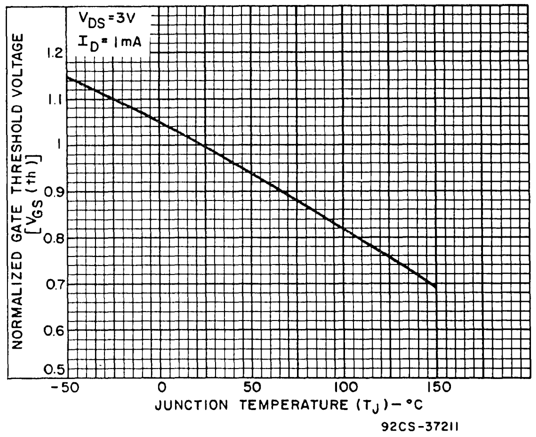


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

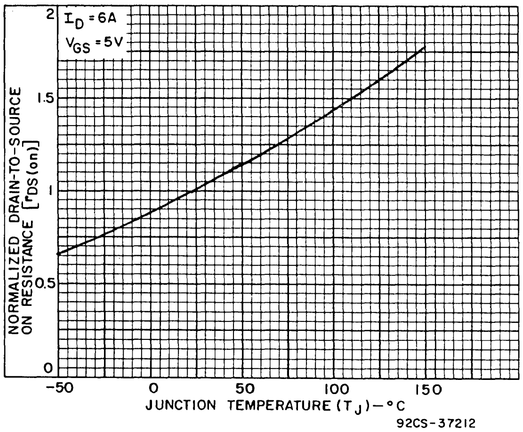


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

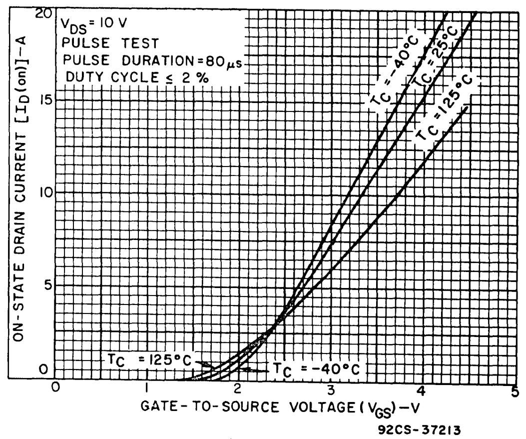


Fig. 5 — Typical transfer characteristics for all types.

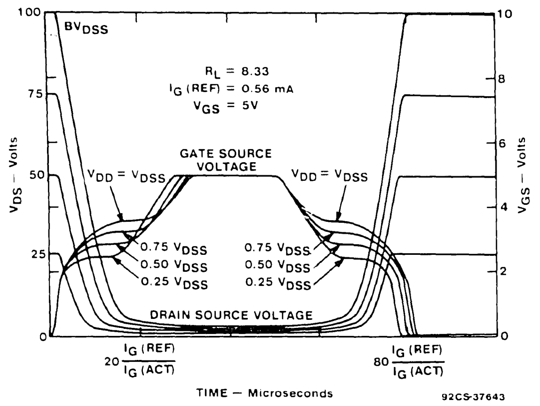


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

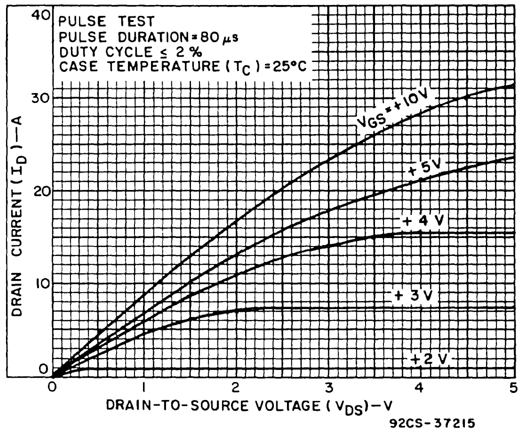


Fig. 7 — Typical saturation characteristics for all types.

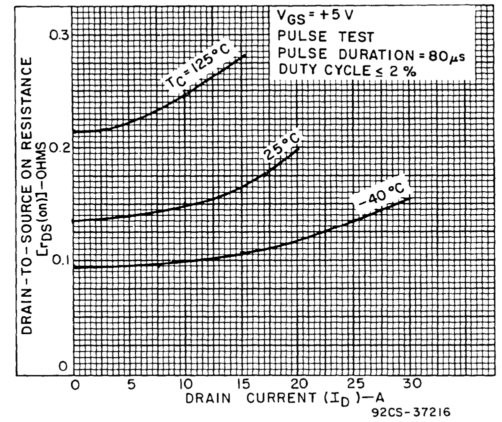


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

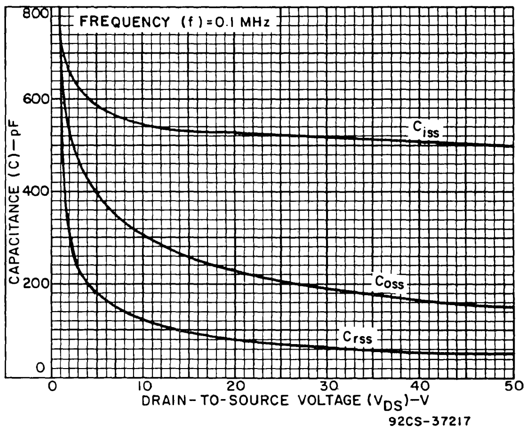


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

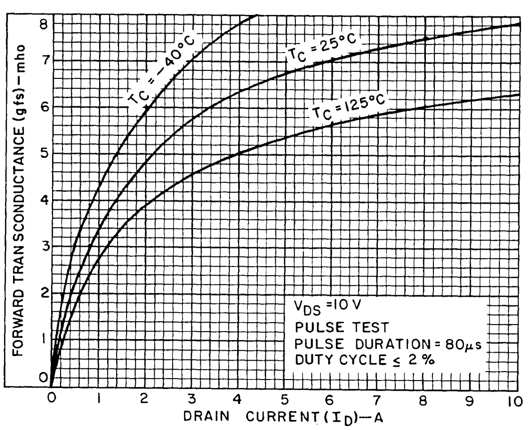


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

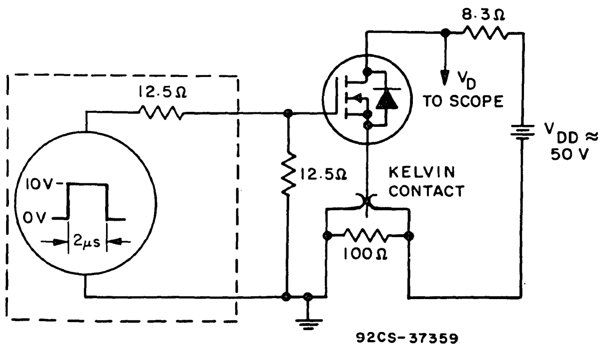


Fig. 11 — Switching Time Test Circuit.

COMFETs

Although vertical MOSFETs have become increasingly important in discrete power-device applications (primarily because of their high input impedance, rapid switching times, and low on-resistance), the fact that their on-resistance increases with increasing drain-source voltage capability has limited their practical value to applications below a few hundred volts. This limitation is effectively overcome in the COMFET or COnductivity Modulated Field Effect Transistor, a device in which the conductivity of the n-type epitaxial drain region is greatly increased (modulated) by the injection of minority carriers from a p-type substrate.

The COMFET operates basically the same as a standard MOSFET and combines the characteristics of a power MOS transistor, a bipolar transistor, and a thyristor in a single device. The COMFET has an exceptionally low on resistance, $r_{DS(on)}$, which permits improved utilization of silicon chip area. This resistance is less than 0.2 ohms for a 0.09 cm^2 chip area, a factor of ten less than that of comparably sized MOSFETs. The on resistance of COMFETs has been measured at less than 0.1 ohm with full drain current, 20 amperes, flowing through the device, and the conductivity-modulated device blocks 400 to 600 volts in the forward direction and 100 volts in the reverse direction. These characteristics combine to make the COMFET an ideal power device for high-voltage, high-power applications.

By modifying the epitaxial structure of the MOSFET and adding recombination centers to the epitaxial drain region, drain-current fall times, t_f, as low as 100 nanoseconds and latching-current values, I_L, as high as 50 amperes with rapid gate turn off have been achieved. The techniques used for the introduction of recombination centers include electron, gamma-ray, and neutron irradiation, as well as heavy metal doping.

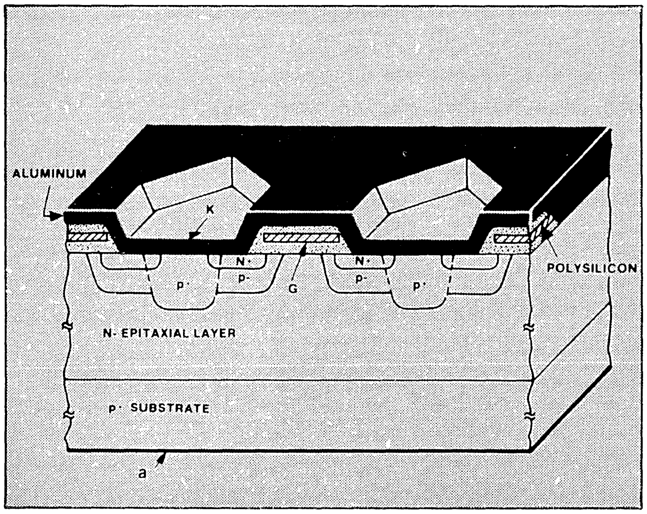
Features
- Low on-state resistance
- Microsecond switching speed
- High input impedance

Applications
- Motor drives
- Power supplies
- Crowbar circuits
- Protective circuits

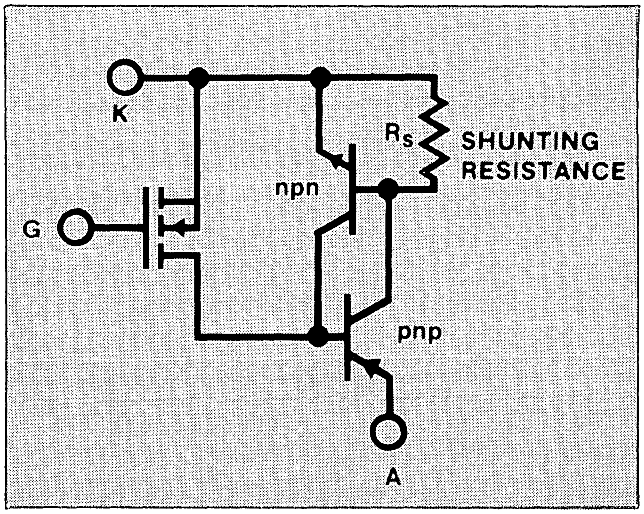
Structure

The unique high-voltage, low-resistance characteristics of the COMFET are achieved by use of a p-type substrate on the drain side of a conventional n-channel power MOSFET. When a positive voltage is applied to the gate terminal, electrons enter the n-type drain region and cause a corresponding hole injection into the drain from the p-type substrate. The carriers, or holes, modulate the conductivity of the high-resistance drain and thereby substantially reduce the overall r_{DS}(on) value.

The cross-sectional structure of the COMFET is similar to that of an MOS-gated thyristor, except for the presence of the equivalent shunting resistance, R_S, in each unit cell. The fabrication of the COMFET is like that of a standard n-channel power MOSFET, except that the n^--epitaxial layer is grown on a p^+ substrate instead of an n^+ substrate, and a thin n^+ layer is added.



Cross section of COMFET structure



Equivalent circuit of a COMFET

The heavily doped p^+ region in the center of each unit cell, combined with the aluminum contact shorting the n^+ and p^+ regions, provides the shunting resistance R_S. This resistance has the effect of lowering the current gain of the n-p-n transistor in the equivalent circuit, so that the individual gains of both the n-p-n and p-n-p transistor equivalents are less than 1, thereby preventing latching over a large operating range of drain voltage, V_D, and drain current, i_D.

For sufficiently large i_D, emitter injection in the n-p-n transistor increases and is accompanied by an increase in the n-p-n transistor's current gain. When the total gain for both transistors increases to 1, the four-layer device latches. The level of i_D at which this latching occurs is the latching current level, I_L.

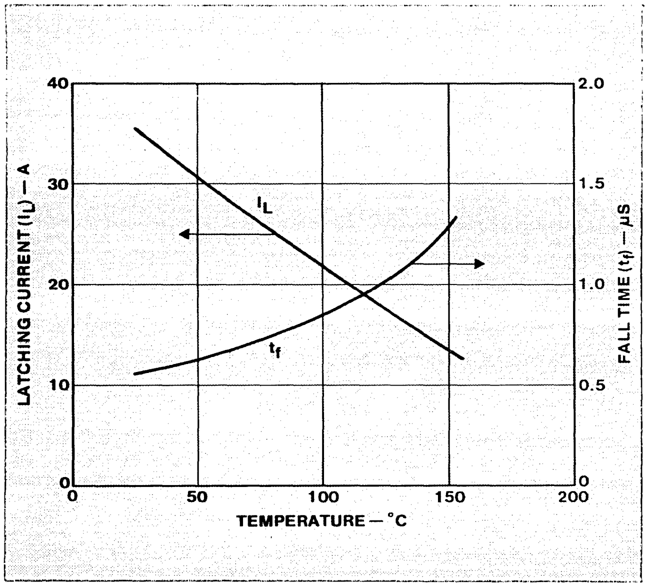
The addition of the thin (approximately 10 nanometer) layer of n^+ silicon in the epitaxial structure between the n^- region and the p^+ substrate lowers the gain of the equivalent p-n-p and allows a greater range of i_D without latching. A reduction in the current gain of the p-n-p equivalent corresponds to an increase in I_L; in fact, the added n^+ layer lowers the emitter injection efficiency of the p-n-p transistor in the equivalent circuit, and results in an increase in I_L by a factor of 2 to 3.

There is also a reduction in fall time, t_f. The COMFETs can block the high voltage only in the forward voltage direction since the emitter junction (p^+-n^+) of the p-n-p equivalent transistor breaks down at a low level when the polarity of the applied voltage is reversed. The smallest values of t_f that have been obtained for COMFETs are in the range of 100 to 200 ns.

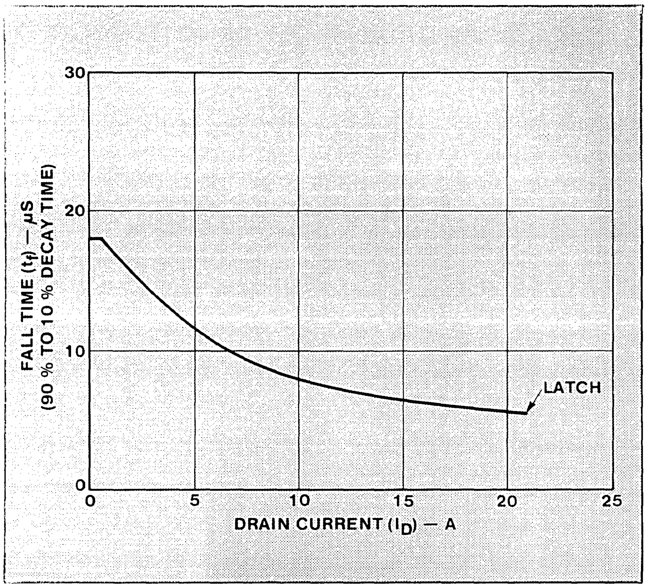
The reduction in minority-carrier lifetime that allows faster switching in a COMFET also carries with it a penalty: higher forward voltage drop when the device is turned on, i.e., higher on-resistance. Clearly, there is a tradeoff involved, and the optimum choice of a value for t_f and the corresponding on-resistance value will depend, to some extent, on the intended application. However, even for the shortest switching times shown (100ns), the on-resistance value of 0.2 ohms is, again, approximately ten times less than that of a comparably-sized n-channel MOSFET.

Thermal Considerations

Because power devices are often operated at elevated temperatures, it is important to determine how their performance varies with temperature. A plot of the variation of t_f and I_L for a COMFET as a function of temperature in the range of 25° C to 150° C shows that t_f increases and I_L decreases with increasing temperature, both by a factor of between 2 and 3 in the interval of 25° C to 150° C.



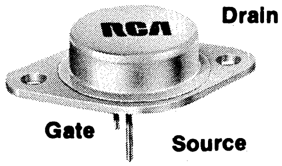
Variation in drain-current fall time t_f and latching current I_L as a function of temperature.



Drain current fall time as a function of drain current magnitude.

TA9437A
TA9437B

Developmental Types



H-1570

JEDEC TO-204MA
(Formerly JEDEC TO-3)

N-Channel Enhancement Mode Conductivity-Modulated Power Field-Effect Transistors

10A, 350V and 400V
V_{DS}(on): 2V

Features:

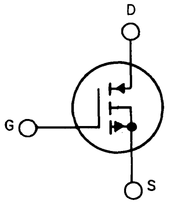
- *Low on-state resistance*
- *Microsecond switching speeds*
- *High input impedance*

Applications:

- *Motor drives*
- *Power supplies*
- *Crowbar circuits*
- *Protective circuits*

The TA9437A and TA9437B are n-channel enhancement-mode conductivity-modulated power field-effect transistors designed for applications such as switching regulators, switching converters and motor drivers.

TERMINAL DIAGRAM



92CS-37694

N-CHANNEL ENHANCEMENT MODE

MAXIMUM RATINGS, *Absolute-Maximum Values* (*T_C = 25° C*):

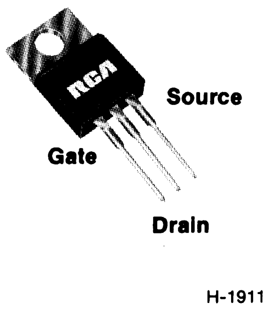
		TA9437A	TA9437B	
Drain-Source Voltage	V_{DSS}	350	400	V
Gate-Source Voltage	V_{GS}	±20		V
Drain Current	I_D	10		A
Gate Threshold Voltage	$V_{GS(TH)}$	2-4		V
Drain Current (80% of Rated V_{DSS})	I_{DSS}	10		μA
Gate-Source Leakage Current	I_{GSS}	100		nA
Drain-Source ON Voltage (At Rated I_D, V_{GS} = 10 V)	$V_{DS(ON)}$	2		V
Thermal Resistance (J-C)		1.67		°C/W
T_{stg}, T_j(max)		-55 to +150		°C

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			TA9437A		TA9437B		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	350	—	400	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 280 V	—	10	—	—	μA
		V_{DS} = 320 V	—	—	—	10	
		T_C = 125° C V_{DS} = 280 V	—	500	—	—	
		V_{DS} = 300 V	—	—	—	500	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
On-State Gate Voltage	$V_{GS}(on)$[a]	V_{DS} = 2 V I_D = 10 A	—	10	—	10	V
		V_{DS} = 1.5 V I_D = 5 A	—	10	—	10	
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 10 A V_{GS} = 10 V	—	2	—	2	V
		I_D = 5 A V_{GS} = 10 V	—	1.5	—	1.5	
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	650	—	650	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	230	—	230	
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	—	60	—	60	
Turn-On Delay Time	$t_d(on)$	V_{DS} = 30	—	0.5	—	0.5	μs
Rise Time	t_r	I_D = 10 A	—	0.5	—	0.5	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	—	0.5	—	0.5	
Fall Time	t_f	V_{GS} = 10 V	—	2.5	—	2.5	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	TA9437A, TA9437B	—	1.67	—	1.67	°C/W

[a] Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

Developmental Types



JEDEC TO-220AB

N-Channel Enhancement Mode Conductivity-Modulated Power Field-Effect Transistors

10A, 350V and 400V
V_{DS}(on): 2V

Features:

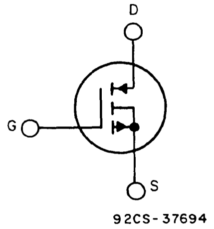
- *Low on-state resistance*
- *Microsecond switching speeds*
- *High input impedance*

Applications:

- *Motor drives*
- *Power supplies*
- *Crowbar circuits*
- *Protective circuits*

The TA9438A and TA9438B are n-channel enhancement-mode conductivity-modulated power field-effect transistors designed for applications such as switching regulators, switching converters and motor drivers.

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

		TA9438A	**TA9438B**	
Drain-Source Voltage	V_{DSS}	350	400	V
Gate-Source Voltage	V_{GS}	±20		V
Drain Current	I_D	10		A
Gate Threshold Voltage	$V_{GS(TH)}$	2-4		V
Drain Current (80% of Rated V_{DSS})	I_{DSS}	10		µA
Gate-Source Leakage Current	I_{GSS}	100		nA
Drain-Source ON Voltage (At Rated I_D, V_{GS} = 10 V)	$V_{DS(ON)}$	2		V
Thermal Resistance (J-C)		2.08		°C/W
T_{stg}, T_j(max)		-55 to +150		°C

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			TA9438A		TA9438B		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	350	—	400	—	V
Gate Threshold Voltage	$V_{GS}(th)$	$V_{GS} = V_{DS}$ I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 280 V	—	10	—	—	μA
		V_{DS} = 320 V	—	—	—	10	
		T_C = 125° C V_{DS} = 280 V	—	500	—	—	
		V_{DS} = 300 V	—	—	—	500	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
On-State Gate Voltage	$V_{GS}(on)^a$	V_{DS} = 2 V I_D = 10 A	—	10	—	10	V
		V_{DS} = 1.5 V I_D = 5 A	—	10	—	10	
Drain-Source On Voltage	$V_{DS}(on)^a$	I_D = 10 A V_{GS} = 10 V	—	2	—	2	V
		I_D = 5 A V_{GS} = 10 V	—	1.5	—	1.5	
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	650	—	650	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	230	—	230	
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	—	60	—	60	
Turn-On Delay Time	$t_d(on)$	V_{DS} = 30	—	0.5	—	0.5	μs
Rise Time	t_r	I_D = 10 A	—	0.5	—	0.5	
Turn-Off Delay Time	$t_d(off)$	$R_{gen}=R_{gs}$=50Ω	—	0.5	—	0.5	
Fall Time	t_f	V_{GS} = 10 V	—	2.5	—	2.5	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	TA9438A, TA9438B	—	2.08	—	2.08	°C/W

[a] Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

Power MOSFET Chips

Index to Types

Type No.	Channel	Description	Data Sheet File No.	Page No.
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PCF2N12	N	120V, 2A, 2 ohms	1425	155
PCF2N18	N	180V, 2A, 3 ohms	1459	156
PCF3N45	N	450V, 3A, 3 ohms	1460	157
PCF5P12	P	120V, 5A, 1 ohm	1523	158
PCF6P08	P	80V, 6A, 0.6 ohm	1518	159
PCF8N18	N	180V, 8A, 0.6 ohm	1520	160
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PCF18N08	N	80V, 18A, 0.12 ohm	1527	169
PCF25N18	N	180V, 25A, 0.15 ohm	1528	170
PCF30N12	N	120V, 30A, 0.085 ohm	1529	171
PCF35N08	N	80V, 35A, 0.06 ohm	1530	172
PCF45N05	N	50V, 45A, 0.04 ohm	1531	173

Ordering Information

RCA offers power chips in three (3) different form factors:

Suffix Letter	Form Factor Definition
H	Chips: Individual test-accepted chips.
W	Unsawed Wafer: Wafter not sawed; 100% tested; reject chips are inked out for easy identification.
WS	Sawed Wafer: Wafer completely sawed after mounting on tape; 100% tested; rejects are inked out for easy identification.

Specify the proper suffix letter when ordering as follows:

Order Option	Example
Chip	PCF2N08H
Unsawed Wafer	PCF2N08W
Sawed Wafer	PCF2N08WS

All quoted and stated prices are per chip regardless of form factor. Actual shipments may vary ±5% of purchase order quantity. Shipments will conform to RCA Terms and Conditions found at the end of this booklet.

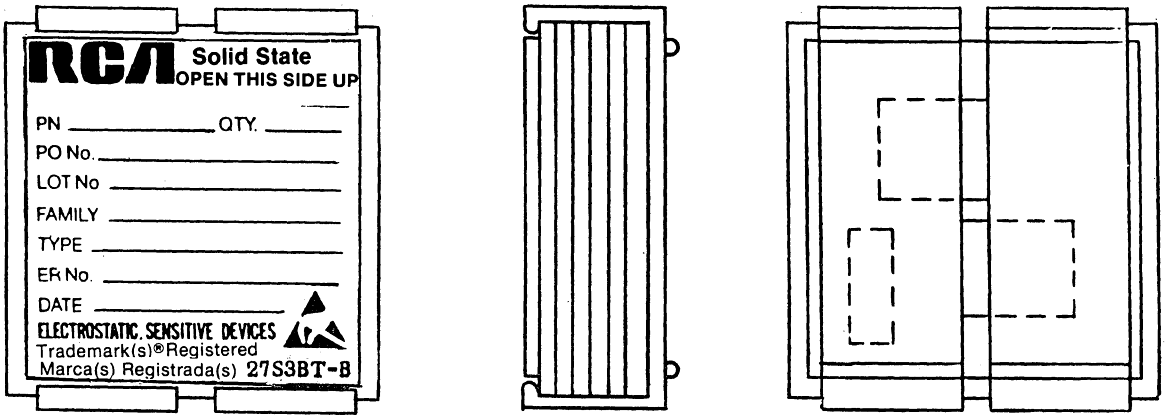
Power MOSFET Chips

Packing for Shipment

RCA chips and wafers are packed in protective enclosures to assure reliability.

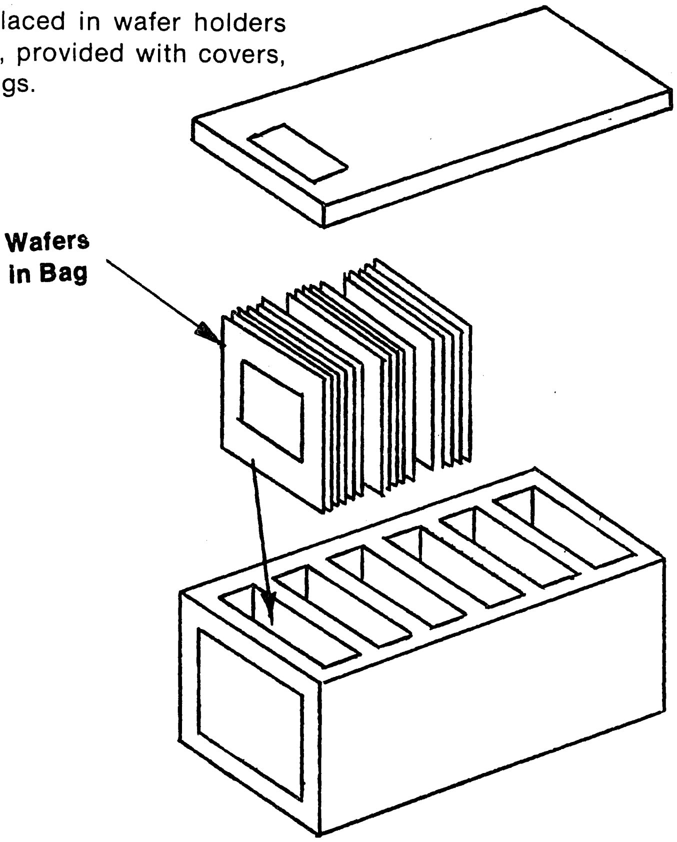
A. **Chips** — H Suffix

Chips are packed in 2" x 2" (waffle pack) trays in which the chips are placed in individual pockets for easy use. The number of chips per tray depends upon the chip size and may be anywhere from 36 to 400. The trays are provided with covers and sealed in plastic bags.



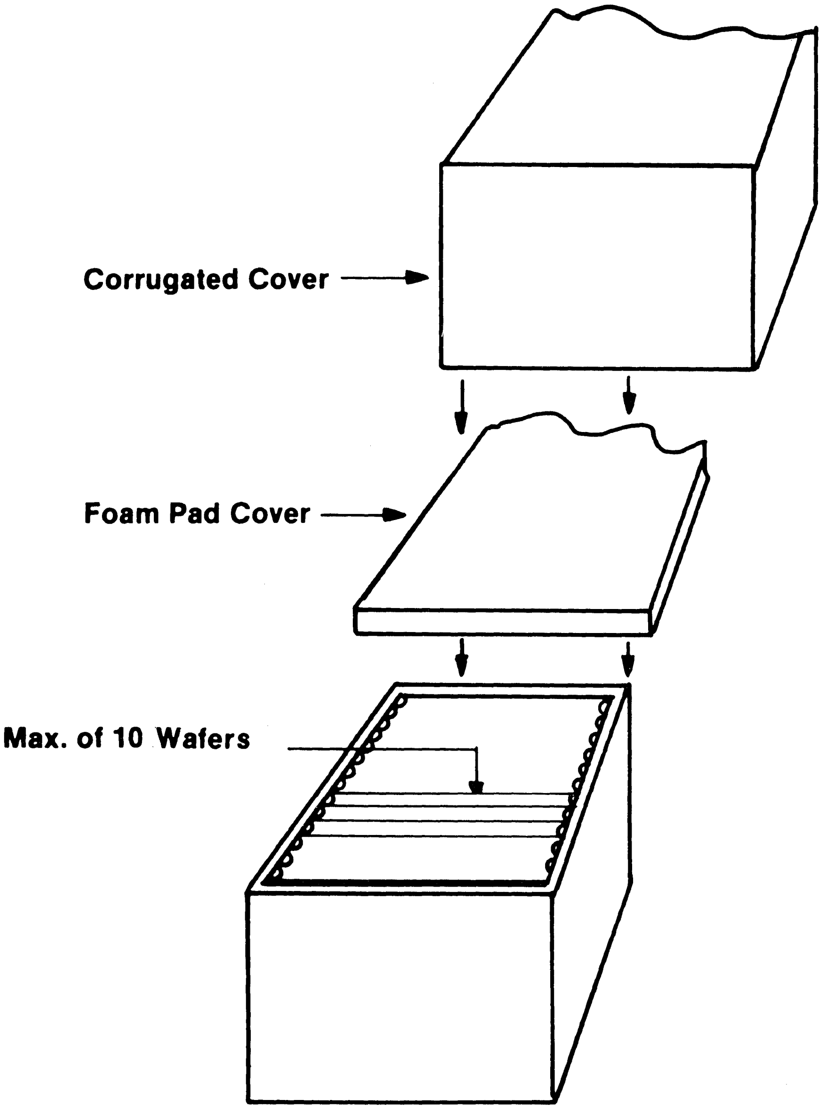
B. **Unsawed Wafers** — W Suffix

Unsawed wafers are placed in wafer holders (fitting in depressions), provided with covers, and sealed in plastic bags.



C. **Sawed Wafers** — WS Suffix

Unsawed wafers are mounted on tape and then sawed. The sawed wafers are placed in sealed plastic bags.

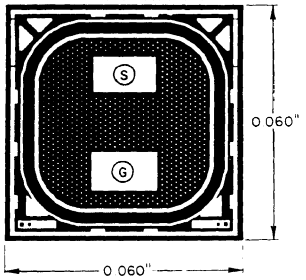


Reliability and Quality Assurance

Electrical Parameters — RCA 100% electrical tests each chip on each wafer to the electrical tests specified in the Technical Data section under the individual RCA power chip device type number. All rejects are inked out. Product is guaranteed to an LTPD of 10%.

Visual Inspection — RCA 100% visually inspects each chip on each wafer in accordance with the chip visual inspection criteria of MIL-STD-750, Test Method 2072. All rejects are inked out.

PCF2N05



Ⓢ SOURCE ATTACH AREA 0.010" x 0.020"
Ⓖ GATE ATTACH AREA 0.010" x 0.020"
BACK SIDE – DRAIN

92CS-35309

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

50 V, 2 A, 0.8 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF2N05-*
  RFL2N05 RFP4N05
  RFL2N06 RFP4N06

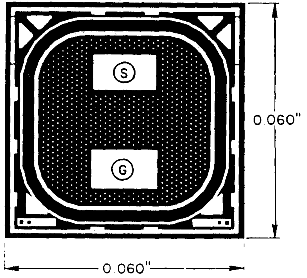
Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	**Test Conditions**	**Limits PCF2N05 Min.**	**Limits PCF2N05 Max.**	**Units**
BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=40 V	—	1	*u*A
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
V_{DS}(ON)[a]	I_D=1 A V_{GS}=10 V	—	0.8	V
g_{fs}[a]	V_{DS}=10 V I_D=1 A	400	—	mmho

[a] Pulsed; pulse duration = 300 *u*s max., duty factor = 2%.

PCF2N08



Ⓢ SOURCE ATTACH AREA 0.010" x 0.020"
Ⓖ GATE ATTACH AREA 0.010" x 0.020"
BACK SIDE – DRAIN

92CS-35309

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

80 V, 2 A, 1.25 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF2N08-*
  RFL1N08 RFP2N08
  RFL1N10 RFP2N10

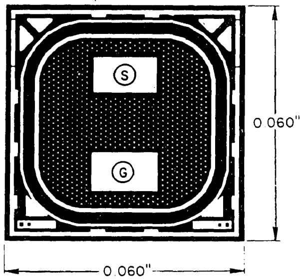
Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF2N08 Min.	Limits PCF2N08 Max.	Units
BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=65 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
V_{DS}(ON)[a]	I_D=1 A V_{GS}=10 V	—	1.25	V
g_{fs}[a]	V_{DS}=10 V I_D=1 A	400	—	mmho

[a] Pulsed; pulse duration = 300 us max., duty factor = 2%.

PCF2N12



Ⓢ SOURCE ATTACH AREA 0.010" x 0.020"
Ⓖ GATE ATTACH AREA 0.010" x 0.020"
BACK SIDE – DRAIN

92CS-35309

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

120 V, 2 A, 2 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF2N12-*
  RFL1N12 RFP2N12
  RFL1N15 RFP2N15

Electrical Characteristics at 25° C

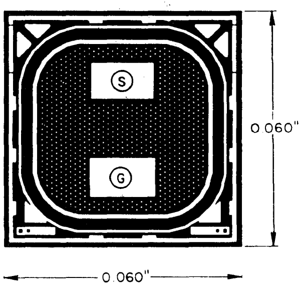
The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF2N12 Min.	Limits PCF2N12 Max.	Units
BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=100 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
V_{DS}(ON)[a]	I_D=1 A V_{GS}=10 V	—	2	V
g_{fs}[a]	V_{DS}=10 V I_D=1 A	400	—	mmho

[a] Pulsed; pulse duration = 300 us max., duty factor = 2%.

File Number **1425**

PCF2N18



Ⓢ SOURCE ATTACH AREA 0.010" x 0.020"
Ⓖ GATE ATTACH AREA 0.010" x 0.020"
BACK SIDE – DRAIN

92CS-35309

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

180 V, 2 A, 3 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF2N18-*

RFL1N18	*RFP2N18*
RFL1N20	*RFP2N20*

Electrical Characteristics at 25° C

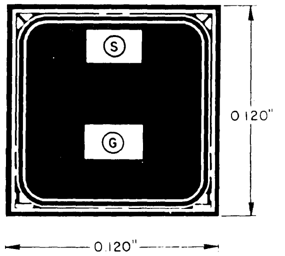
The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF2N18 Min.	Limits PCF2N18 Max.	Units
BV_{DSS}	I_D=1 mA V_{GS}=0	180	—	V
$V_{GS(th)}$	$V_{GS}=V_{DS}$ I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=145 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=1 A V_{GS}=10 V	—	3	V
g_{fs}[a]	V_{DS}=10 V I_D=1 A	400	—	mmho

[a] Pulsed; pulse duration = 300 *u*s max., duty factor = 2%.

File Number **1459**

PCF3N45



Ⓢ SOURCE ATTACH AREA 0.020" x 0.040"
Ⓖ GATE ATTACH AREA 0.020" x 0.040"
BACK SIDE – DRAIN

92CS-35311

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

450 V, 3 A, 3 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF3N45-*
  RFM3N45 RFP3N45
  RFM3N50 RFP3N50

Electrical Characteristics at 25° C

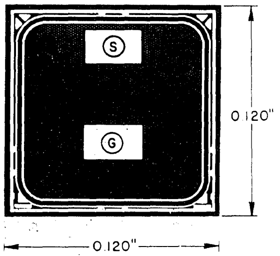
The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF3N45 Min.	Limits PCF3N45 Max.	Units
BV_{DSS}	I_D=1 mA V_{GS}=0	450	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=360 V	—	10	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)^a$	I_D=1.5 A V_{GS}=10 V	—	4.5	V
g_{fs}^a	V_{DS}=10 V I_D=1.5 A	1	—	mho

[a] Pulsed; pulse duration = 300 *u*s max., duty factor = 2%.

File Number **1460**

PCF5P12



Ⓢ SOURCE ATTACH AREA 0.020" x 0.040"
Ⓖ GATE ATTACH AREA 0.020" x 0.040"
BACK SIDE – DRAIN

92CS-35311

P-Channel Enhancement-Mode Power Field-Effect Transistor Chip

5 A, 120 V, 1 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF5P12-*
  RFM5P12 RFP5P12
  RFM5P15 RFP5P15

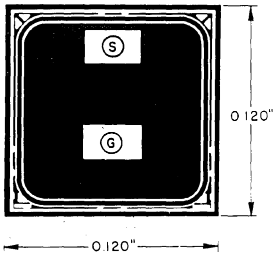
Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF5P12 Min.	Limits PCF5P12 Max.	Units
BV_{DSS}	I_D=1 mA V_{GS}=0	-120	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	V
I_{DSS}	V_{DS}=-100 V	—	1	*u*A
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
V_{DS}(ON)[a]	I_D=2.5 A V_{GS}=-10 V	—	-2.5	V
g_{fs}[a]	V_{DS}=-10 V I_D=2.5 A	0.75	—	mho

[a] Pulsed; pulse duration = 300 *u*s max., duty factor = 2%.

PCF6P08



Ⓢ SOURCE ATTACH AREA 0.020" x 0.040"
Ⓖ GATE ATTACH AREA 0.020" x 0.040"
BACK SIDE – DRAIN

92CS-35311

P-Channel Enhancement-Mode Power Field-Effect Transistor Chip

80 V, 6 A, 0.6 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF6P08-*
  RFM6P08 RFP6P08
  RFM6P10 RFP6P10

Electrical Characteristics at 25° C

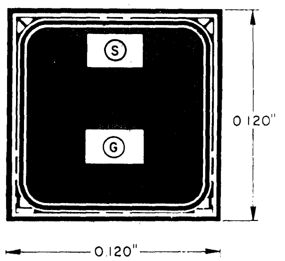
The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF6P08 Min.	Limits PCF6P08 Max.	Units
BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	V
I_{DSS}	V_{DS}=-65 V	—	1	*u*A
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
V_{DS}(ON)[a]	I_D=3 A V_{GS}=-10 V	—	-1.8	V
g_{fs}[a]	V_{DS}=-10 V I_D=3 A	1	—	mho

[a] Pulsed; pulse duration = 300 *u*s max., duty factor = 2%.

File Number **1518**

PCF8N18



Ⓢ SOURCE ATTACH AREA 0.020" x 0.040"
Ⓖ GATE ATTACH AREA 0.020" x 0.040"
BACK SIDE – DRAIN

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

180 V, 8 A, 0.6 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF8N18-*
  RFM8N18 RFP8N18
  RFM8N20 RFP8N20

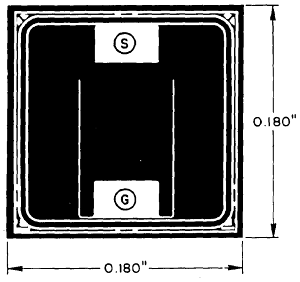
Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF8N18 Min.	Limits PCF8N18 Max.	Units
BV_{DSS}	I_D=1 mA V_{GS}=0	180	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=145 V	—	1	*u*A
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=4 A V_{GS}=10 V	—	2.4	V
g_{fs}[a]	V_{DS}=10 V I_D=4 A	1.5	—	mho

[a] Pulsed; pulse duration = 300 *u*s max., duty factor = 2%.

PCF8P08



Ⓢ SOURCE ATTACH AREA 0.030" x 0.060"
Ⓖ GATE ATTACH AREA 0.030" x 0.060"
BACK SIDE — DRAIN

92CS-35310

P-Channel Enhancement-Mode Power Field-Effect Transistor Chip

80 V, 8 A, 0.4 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF8P08-*
  RFM8P08 RFP8P08
  RFM8P10 RFP8P10

Electrical Characteristics at 25° C

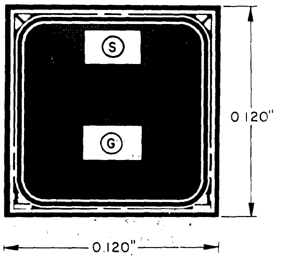
The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF8P08		Units
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	V
I_{DSS}	V_{DS}=-65 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)^a$	I_D=4 A V_{GS}=-10 V	—	-1.6	V
$g_{fs}{}^a$	V_{DS}=-10 V I_D=4 A	2	—	mho

[a] Pulsed; pulse duration = 300 us max., duty factor = 2%.

File Number **1524**

PCF10N12



Ⓢ SOURCE ATTACH AREA 0.020" x 0.040"
Ⓖ GATE ATTACH AREA 0.020" x 0.040"
BACK SIDE — DRAIN

92CS-35311

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

10 A, 120 V, 0.3 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF10N12-*
  RFM10N12 RFP10N12
  RFM10N15 RFP10N15

Electrical Characteristics at 25° C

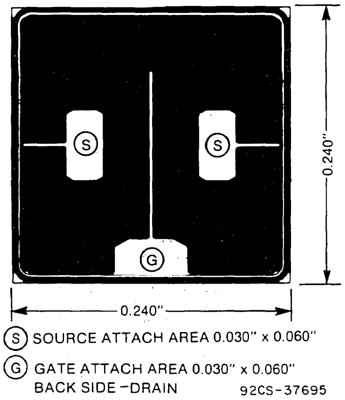
The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF10N12 Min.	Limits PCF10N12 Max.	Units
BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=100 V	—	1	*u*A
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=5 A V_{GS}=10 V	—	1.5	V
g_{fs}[a]	V_{DS}=10 V I_D=5 A	2	—	mho

[a] Pulsed; pulse duration = 300 *u*s max., duty factor = 2%.

File Number **1422**

PCF10N45



N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

450 V, 10 A, 0.75 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF10N45-*
  RFK10N45
  RFK10N50

Electrical Characteristics at 25° C

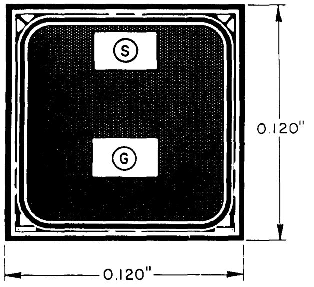
The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF10N45 Min.	Limits PCF10N45 Max.	Units
BV_{DSS}	I_D=1 mA V_{GS}=0	450	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=360 V	—	10	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
V_{DS}(ON)^a	I_D=5 A V_{GS}=10 V	—	3.75	V
g_{fs}^{a}	V_{DS}=10 V I_D=5 A	5	—	mho

[a] Pulsed; pulse duration = 300 *u*s max., duty factor = 2%.

File Number **1525**

PCF12N08



Ⓢ SOURCE ATTACH AREA 0.020" x 0.040"
Ⓖ GATE ATTACH AREA 0.020" x 0.040"
BACK SIDE – DRAIN

92CS-35311

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

80 V, 12 A, 0.2 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF12N08-*
  RFM12N08 RFP12N08
  RFM12N10 RFP12N10

Electrical Characteristics at 25° C

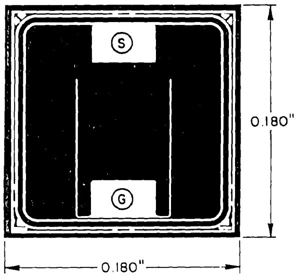
The chip is 100% probed to the actual conditions and limits specified.

Characteristic	**Test Conditions**	**Limits PCF12N08 Min.**	**Limits PCF12N08 Max.**	**Units**
BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=65 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=6 A V_{GS}=10 V	—	1.2	V
g_{fs}[a]	V_{DS}=10 V I_D=6 A	2	—	mho

[a] Pulsed; pulse duration = 300 us max., duty factor = 2%.

File Number **1457**

PCF12N18



Ⓢ SOURCE ATTACH AREA 0.030" x 0.060"
Ⓖ GATE ATTACH AREA 0.030" x 0.060"
BACK SIDE — DRAIN

92CS-35310

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

180 V, 12 A, 0.3 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF12N18-*
  RFM12N18 RFP12N18
  RFM12N20 RFP12N20

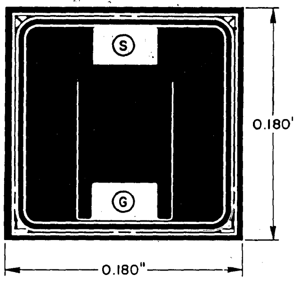
Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF12N18 Min.	Limits PCF12N18 Max.	Units
BV_{DSS}	I_D=1 mA V_{GS}=0	180	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=145 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=6 A V_{GS}=10 V	—	1.8	V
g_{fs}[a]	V_{DS}=10 V I_D=6 A	4	—	mho

[a] Pulsed; pulse duration = 300 us max., duty factor = 2%.

PCF12P08



Ⓢ SOURCE ATTACH AREA 0.030" x 0.060"
Ⓖ GATE ATTACH AREA 0.030" x 0.060"
BACK SIDE — DRAIN

92CS-35310

P-Channel Enhancement-Mode Power Field-Effect Transistor Chip

80 V, 12 A, 0.3 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF12P08-*
  RFM12P08 RFP12P08
  RFM12P10 RFP12P10

Electrical Characteristics at 25° C

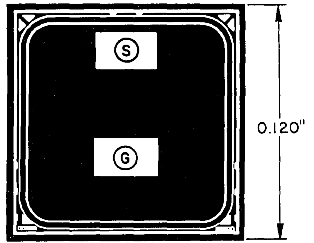
The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF12P08 Min.	Limits PCF12P08 Max.	Units
BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	V
I_{DSS}	V_{DS}=-65 V	—	1	*u*A
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
V_{DS}(ON)[a]	I_D=6 A V_{GS}=-10 V	—	-1.8	V
g_{fs}[a]	V_{DS}=-10 V I_D=6 A	2	—	mho

[a] Pulsed; pulse duration = 300 *u*s max., duty factor = 2%.

File Number **1519**

PCF15N05



(S) SOURCE ATTACH AREA 0.020" x 0.040"
(G) GATE ATTACH AREA 0.020" x 0.040"
BACK SIDE — DRAIN

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

50 V, 15 A, 0.15 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF15N05-*
  RFM15N05 RFP15N05
  RFM15N06 RFP15N06

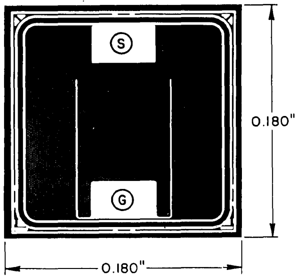
Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF15N05		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=40 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)^a$	I_D=7.5 A V_{GS}=10 V	—	1.125	V
$g_{fs}{}^a$	V_{DS}=10 V I_D=7.5 A	2	—	mho

[a] Pulsed; pulse duration = 300 us max., duty factor = 2%.

PCF15N12



Ⓢ SOURCE ATTACH AREA 0.030" x 0.060"
Ⓖ GATE ATTACH AREA 0.030" x 0.060"
BACK SIDE— DRAIN

92CS-35310

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

120 V, 15 A, 0.15 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-15-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF15N12-*
  RFM15N12 RFP15N12
  RFM15N15 RFP15N15

Electrical Characteristics at 25° C

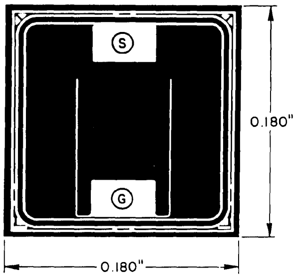
The chip is 100% probed to the actual conditions and limits specified.

Characteristic	**Test Conditions**	**Limits**		**Units**
		PCF15N12		
		Min.	**Max.**	
BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=2 mA	2	4	V
I_{DSS}	V_{DS}=100 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=7.5 A V_{GS}=10 V	—	1.125	V
g_{fs}[a]	V_{DS}=10 V I_D=7.5 A	5	—	mho

[a] Pulsed; pulse duration = 300 *u*s max., duty factor = 2%.

File Number **1424**

PCF18N08



Ⓢ SOURCE ATTACH AREA 0.030" x 0.060"
Ⓖ GATE ATTACH AREA 0.030" x 0.060"
BACK SIDE — DRAIN

92CS-35310

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

80 V, 18 A, 0.12 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF18N08-*
  RFM18N08 RFP18N08
  RFM18N10 RFP18N10

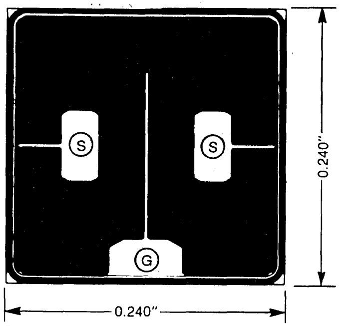
Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF18N08		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=65 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=9 A V_{GS}=10 V	—	1.08	V
g_{fs}[a]	V_{DS}=10 V I_D=9 A	5	—	mho

[a] Pulsed; pulse duration = 300 *u*s max., duty factor = 2%.

PCF25N18



Ⓢ SOURCE ATTACH AREA 0.030" x 0.060"
Ⓖ GATE ATTACH AREA 0.030" x 0.060"
BACK SIDE –DRAIN

92CS-37695

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

180 V, 25 A, 0.15 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF25N18-*
  RFK25N18
  RFK25N20

Electrical Characteristics at 25° C

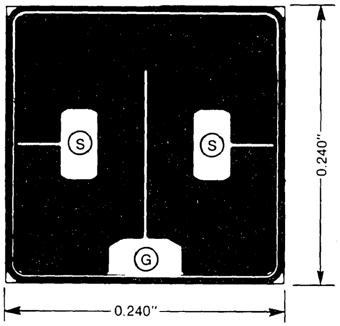
The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF25N18 Min.	Limits PCF25N18 Max.	Units
BV_{DSS}	I_D=1 mA V_{GS}=0	180	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=145 V	—	1	*u*A
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
V_{DS}(ON)[a]	I_D=12.5 A V_{GS}=10 V	—	1.875	V
g_{fs}[a]	V_{DS}=10 V I_D=12.5 A	7	—	mho

[a] Pulsed; pulse duration = 300 *u*s max., duty factor = 2%.

File Number **1528**

PCF30N12



Ⓢ SOURCE ATTACH AREA 0.030" x 0.060"
Ⓖ GATE ATTACH AREA 0.030" x 0.060"
BACK SIDE –DRAIN

92CS-37695

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

30 A, 120 V, 0.085 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF30N12-*
  RFK30N12
  RFK30N15

Electrical Characteristics at 25° C

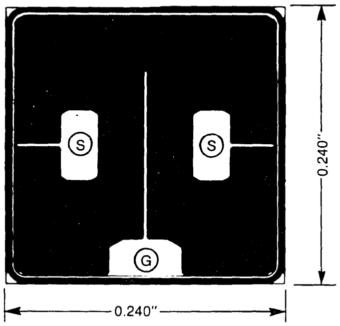
The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF30N12 Min.	Limits PCF30N12 Max.	Units
BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=100 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
V_{DS}(ON)[a]	I_D=15 A V_{GS}=10 V	—	1.275	V
g_{fs}[a]	V_{DS}=10 V I_D=15 A	10	—	mho

[a] Pulsed; pulse duration = 300 us max., duty factor = 2%.

File Number **1529**

PCF35N08



Ⓢ SOURCE ATTACH AREA 0.030" x 0.060"
Ⓖ GATE ATTACH AREA 0.030" x 0.060"
BACK SIDE –DRAIN

92CS-37695

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

80 V, 35 A, 0.06 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF35N08-*
  RFK35N08
  RFK35N10

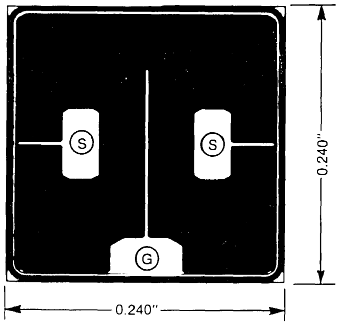
Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF35N08		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=65 V	—	1	*u*A
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
V_{DS}(ON)[a]	I_D=17.5 A V_{GS}=10 V	—	1.05	V
g_{fs}[a]	V_{DS}=10 V I_D=17.5 A	10	—	mho

[a] Pulsed; pulse duration = 300 *u*s max., duty factor = 2%.

PCF45N05



Ⓢ SOURCE ATTACH AREA 0.030" x 0.060"
Ⓖ GATE ATTACH AREA 0.030" x 0.060"
BACK SIDE -DRAIN 92CS-37695

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

50 V, 45 A, 0.04 Ω

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die thickness-17 ± 1 mils*
- *Device types that are derived from PCF45N05-*
  RFK45N05
  RFK45N06

Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF45N05 Min.	Limits PCF45N05 Max.	Units
BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=40 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)^a$	I_D=22.5 A V_{GS}=10 V	—	0.9	V
g_{fs}^a	V_{DS}=10 V I_D=22.5 A	10	—	mho

[a] Pulsed; pulse duration = 300 *u*s max., duty factor = 2%.

File Number **1531**

Power MOSFET Product Preview

In addition to the currently available RCA power MOSFETs described in the preceding pages, new types, including both n-and p-channel devices, are planned for announcement during the second half of 1984. The following data charts show the detailed ratings for the various types.

Features

- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device

Applications

- Switching regulators
- Switching converters
- Relay drivers

RFP1N35, RFP1N40 N-Channel MOSFETs

MAXIMUM RATINGS, Absolute-Maximum Values (T_C = 25°C):

		RFP1N35		RFP1N40	
DRAIN-SOURCE VOLTAGE	V_{DSS}	350		400	V
GATE-SOURCE VOLTAGE	V_{GS}		±20		V
DRAIN CURRENT	I_D		1.0A		A
GATE THRESHOLD VOLTAGE	$V_{GS(TH)}$		2-4		V
DRAIN CURRENT (80% OF RATED V_{DSS})	I_{DSS}		1.0		μA
GATE-SOURCE LEAKAGE CURRENT	I_{GSS}		100		nA
DRAIN-SOURCE ON RESISTANCE (AT 50% RATED I_D, V_{GS} = 10V)	$r_{DS(on)}$		9.0		Ohm
STORAGE AND OPERATING TEMPERATURE	T_{stg}, $T_{j(max.)}$		-55 to 150		°C
THERMAL RESISTANCE, JUNCTION-TO-CASE	$R\theta_{JC}$		6.25		°C/W

RFL2N05L, RFL2N06L; RFP4N05L, RFP4N06L N-Channel Logic Level (L^{2}FET)

MAXIMUM RATINGS, Absolute-Maximum Values (T_C = 25°C):

		RFL2N05L	RFL2N06L		RFP4N05L	RFP4N06L	
DRAIN-SOURCE VOLTAGE	V_{DSS}	50	60		50	60	V
GATE-SOURCE VOLTAGE	V_{GS}			±10			V
DRAIN CURRENT	I_D	2	2		4	4	A
GATE THRESHOLD VOLTAGE	$V_{GS(TH)}$			1-2			V
DRAIN CURRENT (80% OF RATED V_{DSS})	I_{DSS}			1			μA
GATE-SOURCE LEAKAGE CURRENT	I_{GSS}			100			nA
DRAIN-SOURCE ON RESISTANCE (AT 50% RATED I_D, V_{GS} = 10V)	$r_{DS(on)}$	0.95	0.95		0.80	0.80	Ohm
STORAGE AND OPERATING TEMPERATURE	T_{stg}, $T_{j(max.)}$			-55 to 150			°C
THERMAL RESISTANCE, JUNCTION-TO-CASE	$R\theta_{JC}$	15.0	15.0		6.25	6.25	°C/W

RFM4N35, RFM4N40; RFP4N35, RFP4N40 N-Channel MOSFETs

MAXIMUM RATINGS, Absolute-Maximum Values (T_C = 25°C):

		RFM4N35	RFM4N40		RFP4N35	RFP4N40	
DRAIN-SOURCE VOLTAGE	V_{DSS}	350	400		350	400	V
GATE-SOURCE VOLTAGE	V_{GS}			±20			V
DRAIN CURRENT	I_D			4			A
GATE THRESHOLD VOLTAGE	$V_{GS(TH)}$			2-4			V
DRAIN CURRENT (80% OF RATED V_{DSS})	I_{DSS}			1.0			μA
GATE-SOURCE LEAKAGE CURRENT	I_{GSS}			100			nA
DRAIN-SOURCE ON RESISTANCE (AT 50% RATED I_D, V_{GS} = 10V)	$r_{DS(on)}$			2.0			Ohm
STORAGE AND OPERATING TEMPERATURE	T_{stg}, $T_{j(max.)}$			-55 to 150			°C
THERMAL RESISTANCE, JUNCTION-TO-CASE	$R\theta_{JC}$			2.083			°C/W

Information on these devices is intended for engineering evaluation. The type designations and data are subject to change, unless otherwise arranged. No obligations are assumed for notice of change or future manufacture of these devices.

Power MOSFET Product Preview

RFM6N45, RFM6N50; RFP6N45, RFP6N50 N-Channel MOSFETs

MAXIMUM RATINGS, Absolute-Maximum Values (T_C = 25°C):

		RFM6N45	RFM6N50		RFP6N45	RFP6N50	
DRAIN-SOURCE VOLTAGE	V_{DSS}	450	500		450	500	V
GATE-SOURCE VOLTAGE	V_{GS}	————	————	±20	————	————	V
DRAIN CURRENT	I_D	————	————	6	————	————	A
GATE THRESHOLD VOLTAGE	$V_{GS(TH)}$	————	————	2-4	————	————	V
DRAIN CURRENT (80% OF RATED V_{DSS})	I_{DSS}	————	————	10	————	————	μA
GATE-SOURCE LEAKAGE CURRENT	I_{GSS}	————	————	100	————	————	nA
DRAIN-SOURCE ON RESISTANCE (AT 50% RATED I_D, V_{GS} = 10V)	$r_{DS(on)}$	————	————	1.50	————	————	Ohm
STORAGE AND OPERATING TEMPERATURE	$T_{stg}, T_{j(max.)}$	————	————	-55 to 150	————	————	°C
THERMAL RESISTANCE, JUNCTION-TO-CASE	$R\theta_{JC}$	1.25	1.25		1.67	1.67	°C/W

RFM10N12L, RFM10N15L; RFP10N12L, RFP10N15L N-Channel Logic Level (L²FET)

MAXIMUM RATINGS, Absolute-Maximum Values (T_C = 25°C):

		RFM10N12L	RFM10N15L		RFP10N12L	RFP10N15L	
DRAIN-SOURCE VOLTAGE	V_{DSS}	120	150		120	150	V
GATE-SOURCE VOLTAGE	V_{GS}	————	————	±10	————	————	V
DRAIN CURRENT	I_D	————	————	10	————	————	A
GATE THRESHOLD VOLTAGE	$V_{GS(TH)}$	————	————	1-2	————	————	V
DRAIN CURRENT (80% OF RATED V_{DSS})	I_{DSS}	————	————	1	————	————	μA
GATE-SOURCE LEAKAGE CURRENT	I_{GSS}	————	————	100	————	————	nA
DRAIN-SOURCE ON RESISTANCE (AT 50% RATED I_D, V_{GS} = 10V)	$r_{DS(on)}$	————	————	0.30	————	————	Ohm
STORAGE AND OPERATING TEMPERATURE	$T_{stg}, T_{j(max.)}$	————	————	-55 to 150	————	————	°C
THERMAL RESISTANCE, JUNCTION-TO-CASE	$R\theta_{JC}$	————	————	2.083	————	————	°C/W

RFK12N35, RFK12N40 N-Channel MOSFETs

MAXIMUM RATINGS, Absolute-Maximum Values (T_C = 25°C):

		RFK12N35		RFK12N40	
DRAIN-SOURCE VOLTAGE	V_{DSS}	350		400	V
GATE-SOURCE VOLTAGE	V_{GS}	————	±20	————	V
DRAIN CURRENT	I_D	————	12	————	A
GATE THRESHOLD VOLTAGE	$V_{GS(TH)}$	————	2-4	————	V
DRAIN CURRENT (80% OF RATED V_{DSS})	I_{DSS}	————	10	————	μA
GATE-SOURCE LEAKAGE CURRENT	I_{GSS}	————	100	————	nA
DRAIN-SOURCE ON RESISTANCE (AT 50% RATED I_D, V_{GS} = 10V)	$r_{DS(on)}$	————	0.50	————	Ohm
STORAGE AND OPERATING TEMPERATURE	$T_{stg}, T_{j(max.)}$	————	-55 to 150	————	°C
THERMAL RESISTANCE, JUNCTION-TO-CASE	$R\theta_{JC}$	————	0.83	————	°C/W

Information on these devices is intended for engineering evaluation. The type designations and data are subject to change, unless otherwise arranged. No obligations are assumed for notice of change or future manufacture of these devices.

RFM15N05L, RFM15N06L; RFP15N05L, RFP15N06L N-Channel Logic Level (L²FET)

MAXIMUM RATINGS, Absolute-Maximum Values (T_C = 25°C):

		RFM15N05L	RFM15N06L		RFP15N05L	RFP15N06L	
DRAIN-SOURCE VOLTAGE	V_{DSS}	50	60		50	60	V
GATE-SOURCE VOLTAGE	V_{GS}	—	—	±10	—	—	V
DRAIN CURRENT	I_D	—	—	15	—	—	A
GATE THRESHOLD VOLTAGE	$V_{GS(TH)}$	—	—	1-2	—	—	V
DRAIN CURRENT (80% OF RATED V_{DSS})	I_{DSS}	—	—	1	—	—	µA
GATE-SOURCE LEAKAGE CURRENT	I_{GSS}	—	—	100	—	—	nA
DRAIN-SOURCE ON RESISTANCE (AT 50% RATED I_D, V_{GS} = 10V)	$r_{DS(on)}$	—	—	0.15	—	—	Ohm
STORAGE AND OPERATING TEMPERATURE	T_{stg}, $T_{j(max.)}$	—	—	-55 to 150	—	—	°C
THERMAL RESISTANCE, JUNCTION-TO-CASE	$R\theta_{JC}$	—	—	2.083	—	—	°C/W

RFM25N05, RFM25N06; RFP25N05, RFP25N06 N-Channel MOSFETs

MAXIMUM RATINGS, Absolute-Maximum Values (T_C = 25°C):

		RFM25N05	RFM25N06		RFP25N05	RFP25N06	
DRAIN-SOURCE VOLTAGE	V_{DSS}	50	60		50	60	V
GATE-SOURCE VOLTAGE	V_{GS}	—	—	±20	—	—	V
DRAIN CURRENT	I_D	—	—	25	—	—	A
GATE THRESHOLD VOLTAGE	$V_{GS(TH)}$	—	—	2-4	—	—	V
DRAIN CURRENT (80% OF RATED V_{DSS})	I_{DSS}	—	—	1.0	—	—	µA
GATE-SOURCE LEAKAGE CURRENT	I_{GSS}	—	—	100	—	—	nA
DRAIN-SOURCE ON RESISTANCE (AT 50% RATED I_D, V_{GS} = 10V)	$r_{DS(on)}$	—	—	0.085	—	—	Ohm
STORAGE AND OPERATING TEMPERATURE	T_{stg}, $T_{j(max.)}$	—	—	-55 to 150	—	—	°C
THERMAL RESISTANCE, JUNCTION-TO-CASE	$R\theta_{JC}$	1.25	1.25		1.67	1.67	°C/W

RFH30N12, RFH30N15 N-Channel MOSFETs

MAXIMUM RATINGS, Absolute-Maximum Values (T_c = 25°C):

		RFH30N12		RFH30N15	
DRAIN-SOURCE VOLTAGE	V_{DSS}	120		150	V
GATE-SOURCE VOLTAGE	V_{GS}	—	±20	—	V
DRAIN CURRENT	I_D	—	30	—	A
GATE THRESHOLD VOLTAGE	$V_{GS(TH)}$	—	2,4	—	V
DRAIN CURRENT (80% OF RATED V_{DSS})	I_{DSS}	—	1	—	µA
GATE-SOURCE LEAKAGE CURRENT	I_{GSS}	—	100	—	nA
DRAIN-SOURCE ON RESISTANCE (AT 50% RATED I_D, V_{GS} = 10V)	$r_{DS(on)}$	—	0.085	—	Ohm
STORAGE AND OPERATING TEMPERATURE	T_{stg}, $T_{j(max.)}$	—	-55 to 150	—	°C
THERMAL RESISTANCE, JUNCTION-TO-CASE	$R\theta_{JC}$	—	0.83	—	°C/W

Information on these devices is intended for engineering evaluation. The type designations and data are subject to change, unless otherwise arranged. No obligations are assumed for notice of change or future manufacture of these devices.

Power MOSFET Product Preview

RFL1P08, RFL1P10; RFP2P08, RFP2P10 P-Channel MOSFETs

MAXIMUM RATINGS, Absolute-Maximum Values (T_C = 25°C):

		RFL1P08	RFL1P10		RFP2P08	RFP2P10	
DRAIN-SOURCE VOLTAGE	V_{DSS}	-80	-100		-80	-100	V
GATE-SOURCE VOLTAGE	V_{GS}			±20			V
DRAIN CURRENT	I_D	-1	-1		-2	-2	A
GATE THRESHOLD VOLTAGE	$V_{GS(TH)}$			-2,-4			V
DRAIN CURRENT (80% OF RATED V_{DSS})	I_{DSS}			-1.0			μA
GATE-SOURCE LEAKAGE CURRENT	I_{GSS}			100			nA
DRAIN-SOURCE ON RESISTANCE (AT 50% RATED I_D, V_{GS} = 10V)	$r_{DS(on)}$			3.5			Ohm
STORAGE AND OPERATING TEMPERATURE	T_{stg}, $T_{j(max.)}$			-55 to 150			°C
THERMAL RESISTANCE, JUNCTION-TO-CASE	$R\theta_{JC}$	15.0	15.0		6.25	6.25	°C/W

RFM10P12, RFM10P15; RFP10P12, RFP10P15 P-Channel MOSFETs

MAXIMUM RATINGS, Absolute-Maximum Values (T_C = 25°C):

		RFM10P12	RFM10P15		RFP10P12	RFP10P15	
DRAIN-SOURCE VOLTAGE	V_{DSS}	-120	-150		-120	-150	V
GATE-SOURCE VOLTAGE	V_{GS}			±20			V
DRAIN CURRENT	I_D			-10			A
GATE THRESHOLD VOLTAGE	$V_{GS(TH)}$			-2,-4			V
DRAIN CURRENT (80% OF RATED V_{DSS})	I_{DSS}			-1.0			μA
GATE-SOURCE LEAKAGE CURRENT	I_{GSS}			100			nA
DRAIN-SOURCE ON RESISTANCE (AT 50% RATED I_D, V_{GS} = 10V)	$r_{DS(on)}$			0.5			Ohm
STORAGE AND OPERATING TEMPERATURE	T_{stg}, $T_{j(max.)}$			-55 to 150			°C
THERMAL RESISTANCE, JUNCTION-TO-CASE	$R\theta_{JC}$	1.25	1.25		1.67	1.67	°C/W

RFH25P08, RFH25P10 P-Channel MOSFETs

MAXIMUM RATINGS, Absolute-Maximum Values (T_C = 25°C):

		RFH25P08		RFH25P10	
DRAIN-SOURCE VOLTAGE	V_{DSS}	-80		-100	V
GATE-SOURCE VOLTAGE	V_{GS}		±20		V
DRAIN CURRENT	I_D		25		A
GATE THRESHOLD VOLTAGE	$V_{GS(TH)}$		-2,-4		V
DRAIN CURRENT (80% OF RATED V_{DSS})	I_{DSS}		1		μA
GATE-SOURCE LEAKAGE CURRENT	I_{GSS}		100		nA
DRAIN-SOURCE ON RESISTANCE (AT 50% RATED I_D, V_{GS} = 10V)	$r_{DS(on)}$		0.2		Ohm
STORAGE AND OPERATING TEMPERATURE	T_{stg}, $T_{j(max.)}$		-55 to 150		°C
THERMAL RESISTANCE, JUNCTION-TO-CASE	$R\theta_{JC}$		0.83		°C/W

Information on these devices is intended for engineering evaluation. The type designations and data are subject to change, unless otherwise arranged. No obligations are assumed for notice of change or future manufacture of these devices.

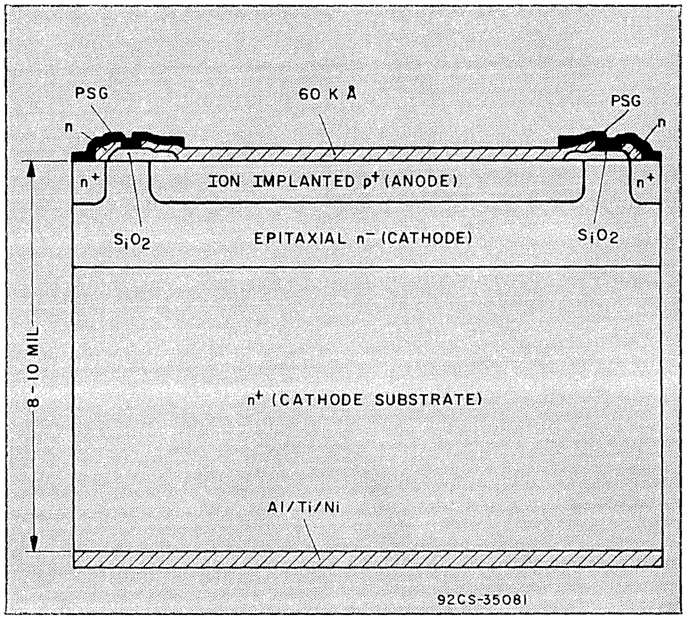
Ultra-Fast-Recovery Rectifiers

Basic Design Features

The latest state-of-the-art processing technology is employed in the manufacture of the new series of RCA ultra-fast-recovery (35-ns) rectifiers. The cathode region is created by the growth of an n^- epitaxial layer onto a low-resistivity n^+ substrate. The anode region is formed by ion implantation and high-temperature diffusion. Aluminum metal on the anode provides for aluminum wire bonding. Trimetal (aluminum-titanium-nickel) evaporated onto the cathode surface provides cathode metallization for high-temperature solder mounting.

Modern planar technology is used to form the edges of the rectifier structure. The structure features an n^+ "channel stopper," an evaporated metal field shield, and an ion trap to assure reverse-bias stability. The p-n junction is insulated by a silicon-dioxide (SiO_2) layer. A phosphorous-doped silicon-glass overcoat provides mechanical protection during assembly.

The resultant structure features low forward voltage drops, excellent bias stability, low dissipation, and very short reverse-recovery times (less than 35 ns).



Planar, high-speed, glass-passivated pellet structure used in RCA ultra-fast-recovery rectifiers.

Hybrid-Circuit Compatibility

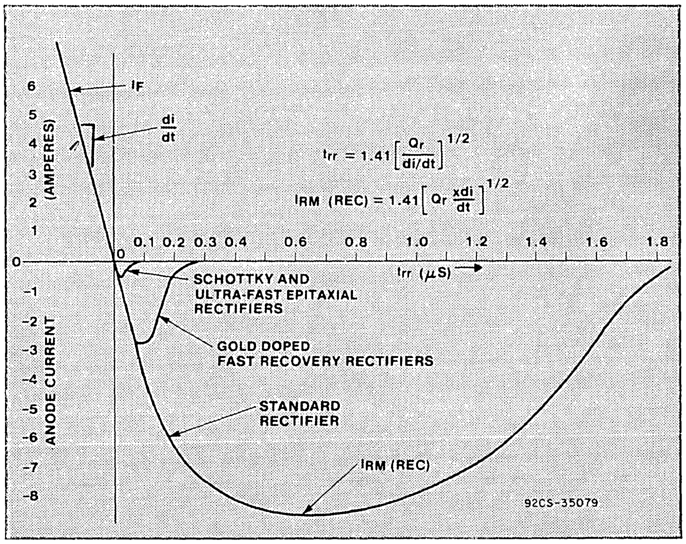
RCA ultra-fast-recovery rectifiers incorporate several construction features that are ideal for mounting the rectifier pellets in hybrid circuits, as follows:

- The trimetal cathode metallization is particularly suited for high-temperature solder mounting. (A eutectic solder bond formed with 95/5 lead-tin solder at a temperature of 320°C is recommended.)
- The aluminum anode metallization facilitates aluminum wire bonding.
- The glass-passivated planar structure assures excellent mechanical protection during processing.
- Large bonding surfaces (3600 mils^2 on 8-ampere types, 10,000 mils^2 on 15-ampere types) are available.

Circuit Benefits

RCA ultra-fast-recovery rectifiers offer several important benefits for use in high-speed power-switching circuits. These benefits include:

- Decrease in the short-circuit energy that impinges on the power switches
- Less RFI generation in the rectifier filter system
- Reduction in, or elimination of, the RC damping networks frequently required with Schottky and ordinary fast-recovery rectifiers
- Dissipations that are 20 to 30 percent less than those in ordinary fast-recovery rectifiers
- Breakdown voltages three to five times greater than those of Schottky rectifiers



$$t_{rr} = 1.41\left[\frac{Q_r}{di/dt}\right]^{1/2}$$

$$I_{RM}\ (REC) = 1.41\left[Q_r\ \frac{x\,di}{dt}\right]^{1/2}$$

Relative reverse-recovery-time (t_{rr}) characteristics of various rectifier structures. Curves show the excellent recovery behavior of the RCA ultra-fast epitaxial structure.

Special Attributes

The RUR series of ultra-fast-recovery rectifiers feature a passivated epitaxial structure that combines the advantages of fast switching speed, low forward-voltage drop, good breakdown capability, and wide operating temperature range. The low stored charge and attendant fast reverse-recovery behavior of these rectifiers minimize electrical noise generation and, in many circuits, markedly reduce the turn-on dissipation of associated power switching transistors. These attributes make RUR-series types excellent choices for use in switching power supplies.

Fast Switching Speeds

Thin anode and cathode regions in the RUR series of RCA ultra-fast-recovery rectifiers limit the build up of excess charge during forward conduction. Gold doping causes this minimal charge to be dissipated quickly during the recovery period so that the recovery time of RUR-series rectifiers is comparable to that of Schottky rectifiers.

Low Forward-Voltage Drop

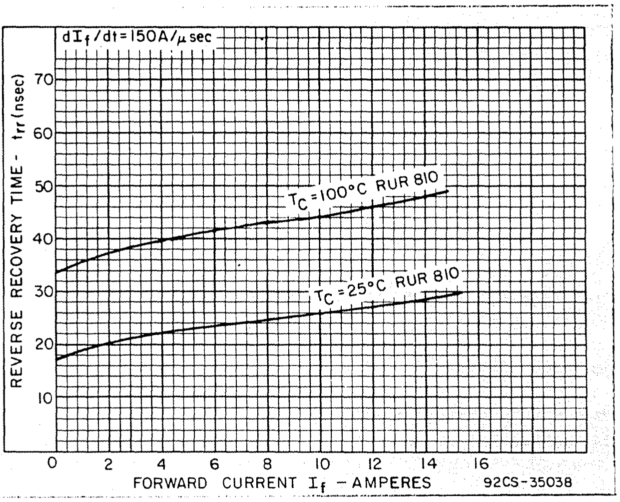
Precise manufacturing control of the anode and cathode vertical structure makes possible low forward-voltage drops — typically less than 0.9 volt at the rated current — significantly lower than those of conventional high-voltage fast-recovery rectifiers.

Breakdown-Voltage Tradeoff

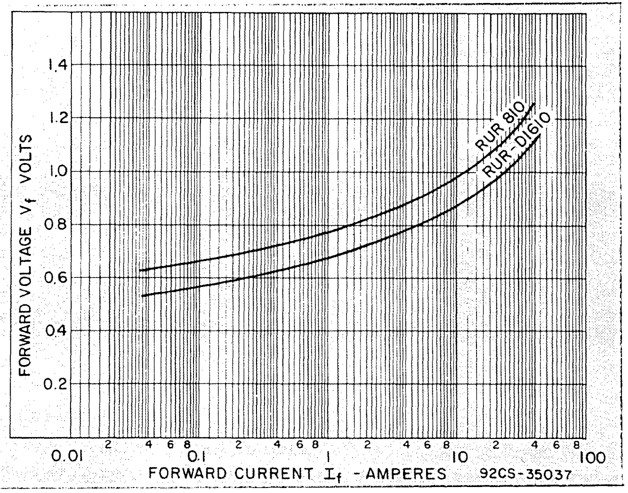
The vertical structure used in RCA ultra-fast rectifiers is optimized for high-speed switching capability, achieved as a tradeoff against reverse-voltage breakdown capability. As a result, the ultra-fast-recovery series are suitable for use as output rectifiers in 100-kHz switching power supplies that provide outputs of 5 to 48 volts. Despite the trade-off for switching speed, the RUR-series rectifiers have a breakdown capability three to five times greater than that of Schottky rectifiers with similar recovery times.

Temperature Capability

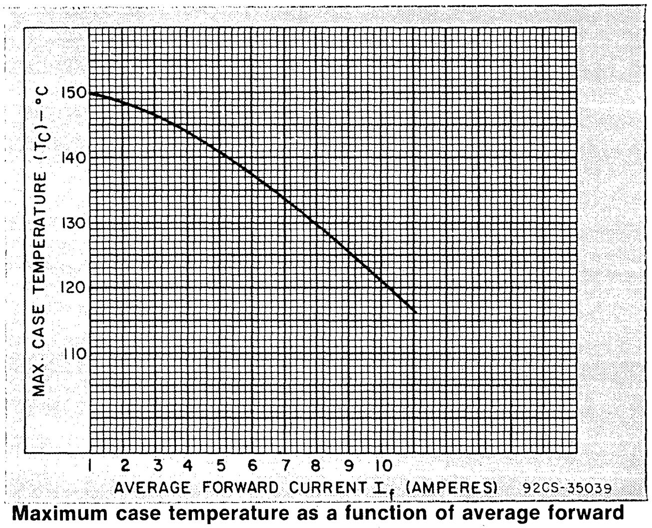
The low forward voltage drop of the ultra-fast-recovery rectifiers permit safe operation of these devices at case temperatures of 125°C at the rated average forward current. At this case temperature, the RUR-810 series rectifiers can operate safely at average currents up to 8 amperes or at peak currents up to 16 amperes in an output circuit with a 50 per cent duty cycle.



Typical reverse-recovery-time as a function of forward current.



Maximum forward voltage as a function of forward current.



Maximum case temperature as a function of average forward current.

Ultra-Fast-Recovery Rectifiers

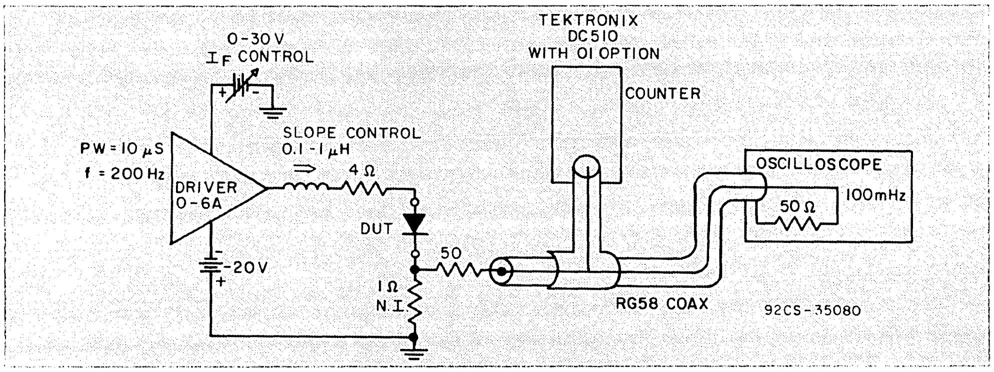
Product Matrix

Rectifier Series	RUR-810	RUR-D810	BYW51	RUR-D1610
100 V	RUR-810	RUR-D810	BYW51-100	RUR-D1610
150 V	RUR-815	RUR-D815	BYW51-150	RUR-D1615
200 V	RUR-820	RUR-D820	BYW51-200	RUR-D1620
Maximum Reverse — Recovery Time, t_{rr}	35 ns	35 ns	35 ns	35 ns
Average Forward Current, $I_{F(AV)}$	8 A	2 x 8 A*	2 x 8 A*	2 x 16 A°
Maximum Surge Current, I_{TSM}	150 A	150 A	150 A	350 A
Junction Capacitance (C_j) at V_{RM} = 10 V	40 pF	40 pF	40 pF	80 pF
Case	TO-220AC	TO-220AB	TO-220AB	TO-3/TO-204MA

*8 A average per junction °16 A average per junction

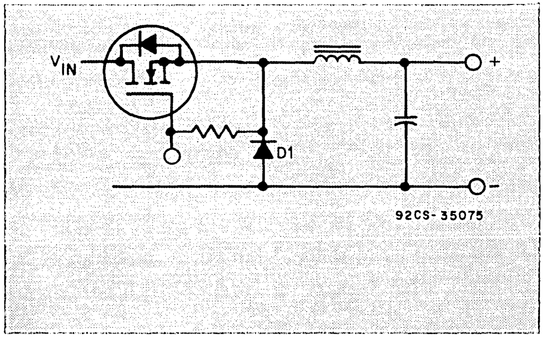
Recovery-Time Measurement Method

Reverse-recovery-time (t_{rr}) measurements are, to some extent, dependent upon the circuit configuration in which the measurement is made and the level of current from which the device must recover. The test-circuit configuration and the test method used in the recovery measurements on the RCA ultra-fast-recovery rectifiers assures realistic current levels and various rates of change of current (-di/dt).

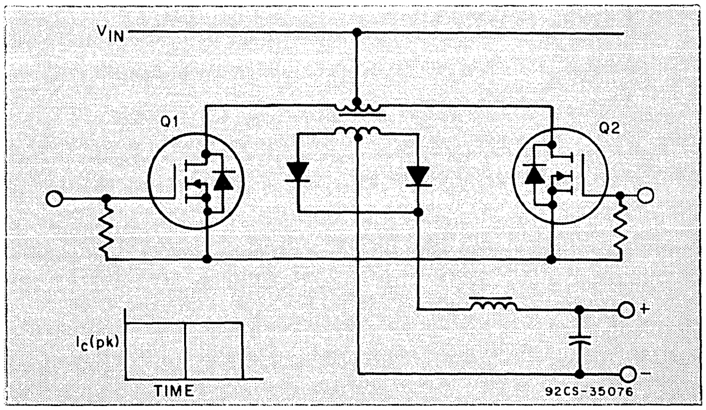


Test circuit used for reverse-recovery-time measurements.

Circuit Examples



Buck-type Switching Regulator



Push-Pull Converter

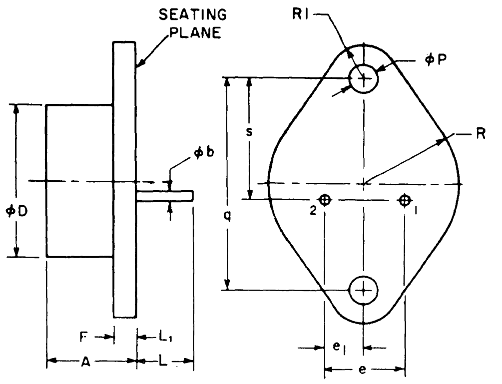
Ultra-Fast-Recovery Rectifiers

Cross-Reference Guide

Rectifier Type	RCA Replacement Type
BYV32-50	RUR-D810, BYW51-100
BYV32-100	RUR-D810, BYW51-100
BYV32-150	RUR-D815, BYW51-150
BYV32-200	RUR-D820, BYW51-200
BYW29-50	RUR-810
BYW29-100	RUR-810
BYW29-150	RUR-815
BYW29-200	RUR-820
BYW51-50	RUR-D810, BYW51-100
BYW51-100	RUR-D810, BYW51-100
BYW51-150	RUR-D815, BYW51-150
BYW80-50	RUR-810
BYW80-100	RUR-810
BYW80-150	RUR-815
BYW80-200	RUR-820
BYW99-50	RUR-D1610
BYW99-100	RUR-D1610
BYW99-150	RUR-D1615
FE8A	RUR-810
FE8B	RUR-810
FE8C	RUR-815
FE8D	RUR-820
FE16A	RUR-D810, BYW51-100
FE16B	RUR-D810, BYW51-100
FE16C	RUR-D815, BYW51-150
FE16D	RUR-D820, BYW51-200
FE30A	RUR-D1610
FE30B	RUR-D1610
FE30C	RUR-D1615
FE30D	RUR-D1620
MUR805	RUR-810
MUR810	RUR-810
MUR815	RUR-815
MUR1605CT	RUR-D810, BYW51-100
MUR1610CT	RUR-D810, BYW51-100
MUR1615CT	RUR-D815, BYW51-150
SES5401	RUR-810
SES5402	RUR-810
SES5403	RUR-815
SES5401C	RUR-D810, BYW51-100
SES5402C	RUR-D810, BYW51-100
SES5403C	RUR-D815, BYW51-150
SES5601C	RUR-D1610
SES5602C	RUR-D1610
SES5603C	RUR-D1615
UES1401	RUR-810
UES1402	RUR-810
UES1403	RUR-815
UES2401	RUR-D810
UES2402	RUR-D810
UES2403	RUR-D815
UES2601	RUR-D1610
UES2602	RUR-D1610
UES2603	RUR-D1615
VHE1401	RUR-810
VHE1402	RUR-810
VHE1403	RUR-815
VHE1404	RUR-820

Dimensional Outlines

JEDEC TO-204MA
(Formerly JEDEC TO-3)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.35	11.35	
φb	0.038	0.043	0.96	1.092	1
φD	—	0.875	—	22.22	
e	0.420	0.440	10.67	11.17	2
e_1	0.205	0.225	5.21	5.71	2
F	0.060	0.135	1.53	3.42	
L	0.312	0.500	7.93	12.70	
L_1	—	0.050	—	1.27	1
φP	0.151	0.161	3.836	4.089	
q	1.177	1.197	29.90	30.40	
R	0.495	0.525	12.58	13.33	
R_1	0.131	0.188	3.33	4.77	
s	0.655	0.675	16.64	17.14	

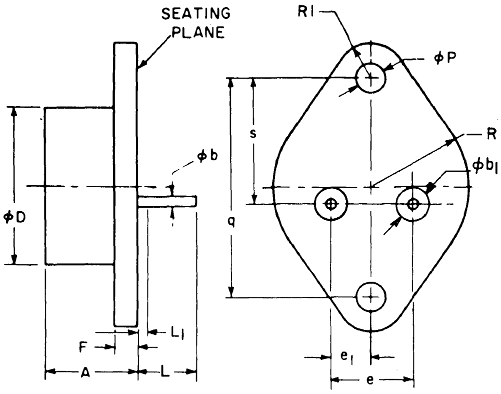
92CS-15222R3

Notes:

1: φb applies between L_1 and L. Diameter is uncontrolled in L_1.

2: These dimensions should be measured at points 0.050 in. (1.270 mm) to 0.055 in. (1.397 mm) below seating plane. When gage is not used, measurement will be made at seating plane.

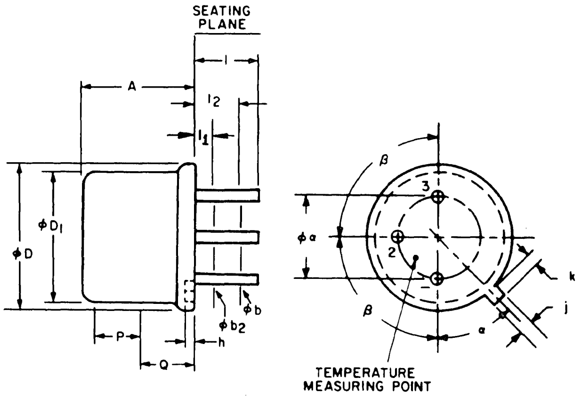
JEDEC TO-204AE
141 mil diameter pin isolation



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.4	11.4	
φb	0.057	0.063	1.45	1.60	
$φb_1$	0.141 NOM.		3.58 NOM.		
φD	—	0.875	—	22.22	
e	0.420	0.440	10.67	11.17	
e_1	0.205	0.225	5.21	5.71	
F	0.060	0.135	1.53	3.42	
L	0.440	0.480	11.18	12.19	
φP	0.151	0.161	3.84	4.08	
q	1.187	BSC	30.15	BSC	
R	0.495	0.525	12.58	13.33	
R_1	0.131	0.188	3.33	4.77	
s	0.655	0.675	16.64	17.14	

92CS-37523

TO-205MD/TO-39



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
φa	0.190	0.210	4.83	5.33	
A	0.240	0.260	6.10	6.60	
φb	0.016	0.021	0.406	0.533	2
$φb_2$	0.016	0.019	0.406	0.483	2
φD	0.350	0.370	8.89	9.40	
$φD_1$	0.305	0.335	8.00	8.51	
h	0.009	0.041	0.229	1.04	
j	0.028	0.034	0.711	0.864	
k	0.029	0.040	0.737	1.02	3
L	0.500	0.750	12.70	19.05	2
l_1	—	0.050	—	1.27	2
l_2	0.250	—	6.35	—	2
P	0.100	—	2.54	—	1
Q					4
α	45° NOMINAL		—	—	
β	90° NOMINAL		—	—	

92CS-22334R2

Notes:

1: This zone is controlled for automatic handling. The variation in actual diameter within this zone shall not exceed 0.010 in. (0.254 mm).

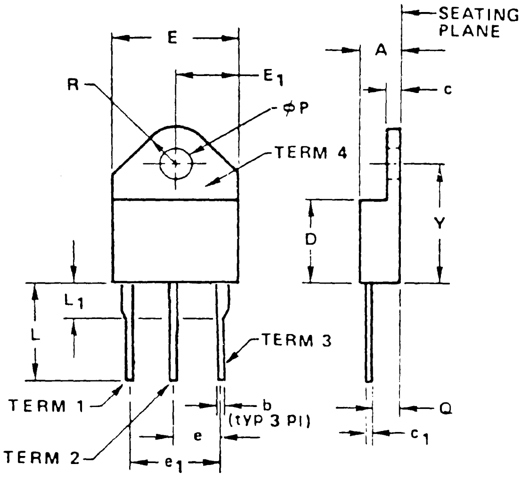
2: (Three leads) $φb_2$ applies between l_1 and l_2. φb applies between l_2 and l. Diameter is uncontrolled in l_1.

3: Measured from maximum diameter of the actual device.

4: Details of outline in this zone optional.

Dimensional Outlines

TO-218AC



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.165	.200	4.191	5.080	
b	.040	.063	1.016	1.600	
c	.053	.065	1.346	1.651	
c_1	.018	.030	.457	.762	
D	.485	.505	12.319	12.827	
E	.610	.640	15.494	16.256	1
E_1	.305	.320	7.747	8.128	
e	.205	.225	5.207	5.715	
e_1	.420	.440	10.668	11.176	
L	.500	.610	12.700	15.494	
L_1	—	.125	—	3.175	2
ϕP	.157	.167	3.988	4.241	
Q	.094	.126	2.388	3.200	
R	.170	.190	4.318	4.826	
Y	.626	.670	15.900	17.018	

92CS-37698

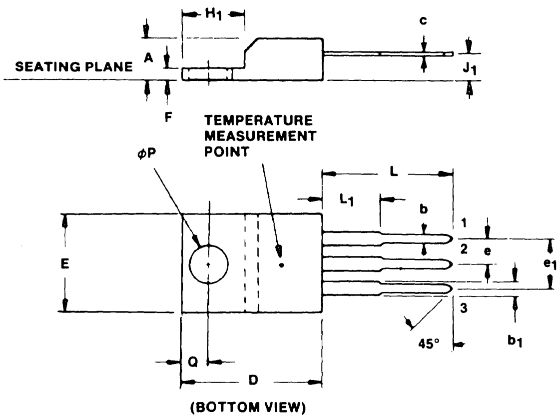
Notes:

1: Tab outline optional within boundaries of dimensions E and R.

2: Lead dimensions uncontrolled in L_1.

3: Controlling dimensions: inch.

TO-220AB VERSAWATT



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.140	0.190	3.56	4.82	
b	0.020	0.045	0.51	1.14	
b_1	0.045	0.070	1.14	1.77	
c	0.015	0.025	0.38	0.63	
D	0.560	0.625	14.23	15.87	
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	
e_1	0.190	0.210	4.83	5.33	2
F	0.045	0.055	1.14	1.39	
H_1	0.230	0.270	5.85	6.85	1
J_1	0.080	0.115	2.04	2.92	
L	0.500	0.562	12.70	14.27	
L_1	—	0.250	—	6.35	
ϕP	0.139	0.161	3.531	4.089	
Q	0.100	0.120	2.54	3.04	

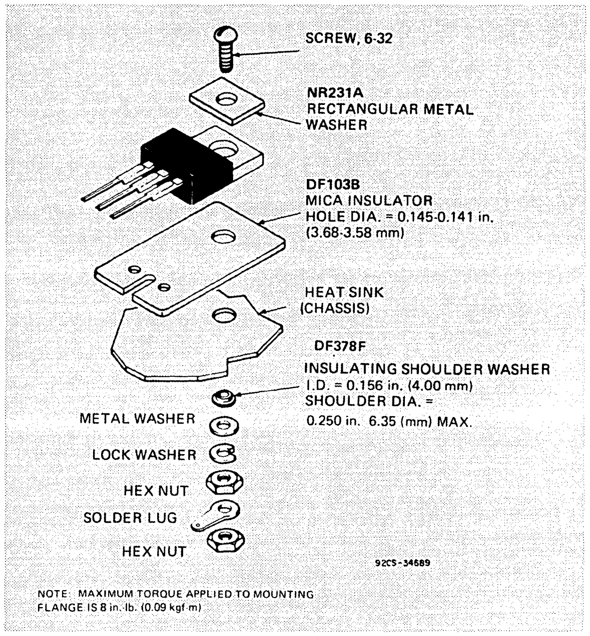
92CS-34697

Notes:

1: Tab contour optional within H_1 and E.

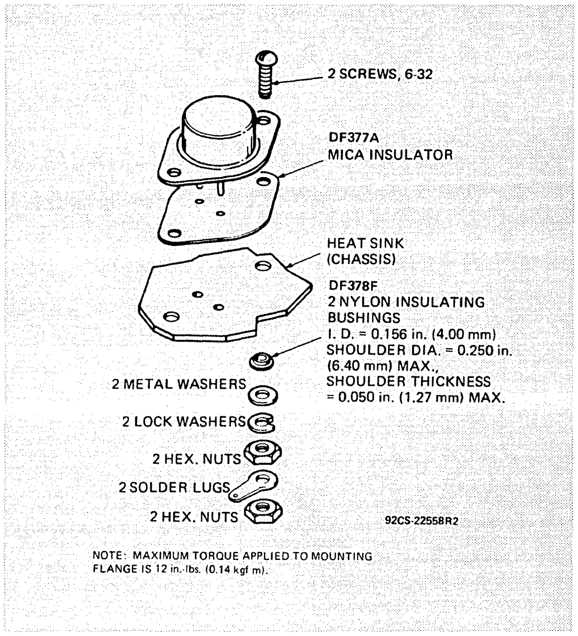
2: Position of lead to be measured 0.250 - 0.255 in. (6.350 -6.477 mm) from case.

Mounting Hardware



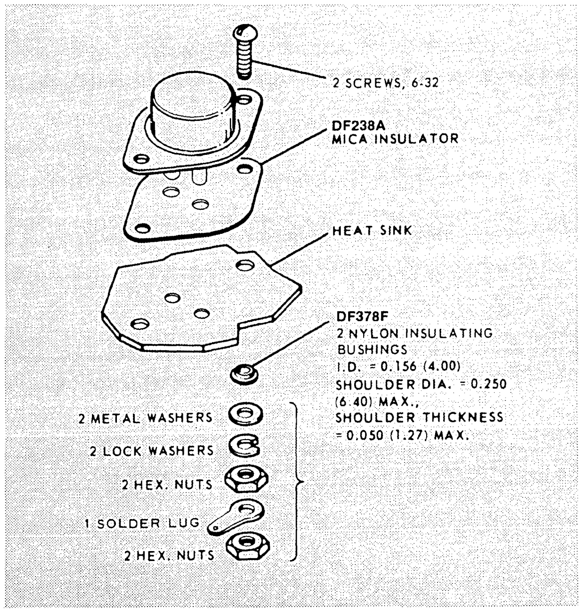
NOTE: MAXIMUM TORQUE APPLIED TO MOUNTING FLANGE IS 8 in.-lb. (0.09 kgf·m)

Suggested mounting hardware for JEDEC TO-220AB.



NOTE: MAXIMUM TORQUE APPLIED TO MOUNTING FLANGE IS 12 in.-lbs. (0.14 kgf m).

Suggested mounting hardware for JEDEC TO-204MA (Formerly JEDEC TO-3).



Suggested mounting hardware for JEDEC TO-204AE

INDUSTRY REPLACEMENT GUIDE

INDUSTRY TYPE	CH	RCA REPLACEMENT TYPE
SIEMENS		
BUZ 10B	+N	RFP15N05
BUZ 14	+N	RFK45N05
BUZ 14A	+N	RFK45N05
BUZ 14B	+N	*RFM25N05
BUZ 14C	+N	RFM15N05
BUZ 14D	+N	RFM15N05
BUZ 20	+N	RFP12N10
BUZ 20A	+N	RFP12N10
BUZ 20B	+N	RFP12N10
BUZ 23	+N	RFM12N10
BUZ 23A	+N	RFM15N12
BUZ 23B	+N	RFM10N12
BUZ 24B	+N	RFK30N12
BUZ 30	+N	RFP8N20
BUZ 32	+N	RFP12N20
BUZ 32A	+N	RFP10N15
BUZ 32B	+N	RFP8N20
BUZ 32C	+N	RFP8N18
BUZ 33	+N	RFM8N20
BUZ 33A	+N	RFM8N20
BUZ 33B	+N	RFM10N15
BUZ 35	+N	RFM12N20
BUZ 35A	+N	RFM10N15
BUZ 41A	+N	*RFP6N50
BUZ 41B	+N	*RFP6N45
BUZ 42	+N	*RFP6N50
BUZ 42A	+N	*RFP6N45
BUZ 42B	+N	RFP3N50
BUZ 42C	+N	RFP3N45
BUZ 42D	+N	RFP3N50
BUZ 44A	+N	*RFM6N50
BUZ 44B	+N	*RFM6N45
BUZ 45A	+N	RFK10N50
BUZ 46	+N	*RFM6N50
BUZ 46A	+N	*RFM6N45
BUZ 46B	+N	RFM3N50
BUZ 60	+N	*RFP7N40
BUZ 60A	+N	*RFP7N35
BUZ 60B	+N	*RFP7N40
BUZ 60C	+N	*RFP7N35
BUZ 60D	+N	*RFP7N40
BUZ 63	+N	*RFM7N40
BUZ 63A	+N	*RFM7N35
BUZ 63B	+N	*RFM7N40
BUZ 63C	+N	*RFM7N35
BUZ 63D	+N	*RFM7N40
BUZ 71A	+N	RFP15N05
GENERAL ELECTRIC		
D84CK1	+N	RFP15N05
D84CK2	+N	RFP15N06
D84CL1	+N	RFP12N08
D84CL2	+N	RFP12N10
D84CM1	+N	RFP8N18
D84CM2	+N	RFP8N18
D84CN1	+N	RFP8N18
D84CN2	+N	RFP8N20
D84CQ1	+N	*RFP4N35
D84CQ2	+N	*RFP4N40
D84CR1	+N	RFP3N45
D84CR2	+N	RFP3N50
D84DK1	+N	RFP15N05
D84DK2	+N	RFP15N06
D84DL1	+N	RFP18N08
D84DL2	+N	RFP18N10
D84DM1	+N	RFP10N12
D84DM2	+N	RFP10N15
D84DN1	+N	RFP12N18
D84DN2	+N	RFP12N20
D84DQ1	+N	*RFP7N35
D84DQ2	+N	*RFP7N40
D84DR1	+N	*RFP6N45
D84DR2	+N	*RFP6N50
D84EK1	+N	*RFP25N05
D84EK2	+N	*RFP25N06
D84EM1	+N	RFP15N12
D84EM2	+N	RFP15N15
D86DK1	+N	RFM15N05
D86DK2	+N	RFM15N06
D86DL1	+N	RFM18N08
D86DL2	+N	RFM18N10
D86DM1	+N	RFM10N12
D86DM2	+N	RFM10N15
D86DN1	+N	RFM12N18
D86DN2	+N	RFM12N20
D86DQ1	+N	*RFM7N35
D86DQ2	+N	*RFM7N40
D86DR1	+N	*RFM6N45
D86DR2	+N	*RFM6N50
D86EK1	+N	*RFM25N05
D86EK2	+N	*RFM25N06
D86EL1	+N	*RFM35N08
D86EL2	+N	*RFM35N10
D86EM1	+N	RFM15N12
D86EM2	+N	RFM15N15
D86EN1	+N	*RFK25N18
D86EN2	+N	*RFK25N20
D86EQ1	+N	*RFK12N35
D86EQ2	+N	*RFK12N40
D86ER1	+N	RFK10N45
D86ER2	+N	RFK10N50
D86FK1	+N	RFK45N05
D86FK2	+N	RFK45N06
D86FL1	+N	RFK35N08
D86FL2	+N	RFK35N10
D86FM1	+N	RFK30N12
D86FM2	+N	RFK30N15
D86FQ1	+N	*RFK12N35
D86FQ2	+N	*RFK12N40
INTER RECTIFIER		
IRFF110	+N	RFL4N12
IRFF111	+N	RFL4N12
IRFF112	+N	RFL4N12
IRFF113	+N	RFL4N12
IRFF120	+N	RFL4N12
IRFF121	+N	RFL4N12
IRFF122	+N	RFL4N12
IRFF123	+N	RFL4N12
IRF120	+N	RFM12N10
IRF121	+N	RFM15N06
IRF122	+N	RFM12N10
IRF123	+N	RFM15N06
IRF130	+N	IRF130
IRF541	+N	*RFP25N06
IRF543	+N	*RFP25N06
IRF131	+N	IRF131
IRF132	+N	IRF132
IRF133	+N	IRF133
IRF140	+N	RFK35N10
IRF141	+N	*RFM25N06
IRF142	+N	RFK35N10
IRF143	+N	*RFM25N06
IRF150	+N	RFK35N10
IRF151	+N	RFK45N06
IRF152	+N	RFK35N10
IRF153	+N	RFK45N06
IRF220	+N	RFM8N20
IRF221	+N	RFM10N15
IRF222	+N	RFM8N20
IRF223	+N	RFM10N15
IRF230	+N	RFM12N20
IRF231	+N	RFM10N15
IRF232	+N	RFM8N20
IRF233	+N	RFM10N15
IRF240	+N	RFK25N20
IRF241	+N	RFM15N15
IRF242	+N	RFM12N20
IRF243	+N	RFM15N15
IRF251	+N	IRF251
IRF252	+N	RFK25N20
IRF253	+N	IRF253
IRF320	+N	*RFM7N40
IRF321	+N	*RFM7N35
IRF322	+N	*RFM7N40
IRF323	+N	*RFM7N35
IRF330	+N	*RFM7N40
IRF331	+N	*RFM7N35
IRF332	+N	*RFM7N40
IRF333	+N	*RFM7N35
IRF340	+N	*RFK12N40
IRF341	+N	*RFK12N35
IRF342	+N	*RFK12N40
IRF343	+N	*RFK12N35
IRF420	+N	IRF420
IRF421	+N	IRF421
IRF422	+N	IRF422
IRF423	+N	IRF423
IRF430	+N	*RFM6N50
IRF431	+N	*RFM6N45
IRF432	+N	*RFM6N50
IRF433	+N	*RFM6N45
IRF440	+N	RFK10N50
IRF441	+N	RFK10N45
IRF442	+N	RFK10N50
IRF443	+N	RFK10N45
IRF510	+N	IRF510
IRF511	+N	IRF511
IRF512	+N	IRF512
IRF513	+N	IRF513
IRF520	+N	IRF520
IRF521	+N	IRF521
IRF522	+N	IRF522
IRF523	+N	IRF523
IRF530	+N	IRF530
IRF531	+N	IRF531

Industry Replacement Guide

INDUSTRY TYPE	CH	RCA REPLACEMENT TYPE
INTER RECTIFIER		
IRF532	+N	IRF532
IRF533	+N	IRF533
IRF610	+N	RFP8N20
IRF611	+N	RFP10N15
IRF612	+N	RFP8N20
IRF613	+N	RFP10N15
IRF620	+N	RFP8N20
IRF621	+N	RFP8N18
IRF622	+N	RFP8N20
IRF623	+N	RFP8N18
IRF631	+N	RFP10N15
IRF632	+N	RFP8N20
IRF633	+N	RFP10N15
IRF641	+N	RFP15N15
IRF643	+N	RPF15N15
IRF710	+N	*RFP4N40
IRF711	+N	*RFP4N35
IRF712	+N	*RFP4N40
IRF713	+N	*RFP4N35
IRF722	+N	*RFP4N40
IRF723	+N	*RFP4N35
IRF730	+N	*RFP7N40
IRF731	+N	*RFP7N35
IRF732	+N	*RFP7N40
IRF733	+N	*RFP7N35
IRF820	+N	RFP3N50
IRF821	+N	RFP3N45
IRF822	+N	RFP3N50
IRF823	+N	RFP3N45
IRF830	+N	*RFP6N50
IRF831	+N	*RFP6N45
IRF832	+N	*RFP6N50
IRF833	+N	*RFP6N45
IRF9130	-P	RFM12P10
IRF9131	-P	RFM12P08
IRF9132	-P	RFM8P10
IRF9133	-P	RFM8P08
IRF9510	-P	RFP5P12
IRF9511	-P	RFP5P12
IRF9512	-P	RFP5P12
IRF9513	-P	RFP5P12
IRF9520	-P	RFP6P10
IRF9521	-P	RFP6P08
IRF9522	-P	RFP6P10
IRF9523	-P	RFP6P08
IRF9530	-P	RFP12P10
IRF9531	-P	RFP12P08
IRF9532	-P	RFP8P10
IRF9533	-P	RFP8P08
IRF9611	-P	RFP5P15
IRF9613	-P	RFP5P15
IRF9621	-P	RFP5P15
IRF9623	-P	RFP5P15
IRF9631	-P	*RFP8P15
IRF9633	-P	RFP5P15
MOTOROLA		
MTM10N05	+N	RFM15N05
MTM10N06	+N	RFM15N06
MTM10N08	+N	RFM12N08

INDUSTRY TYPE	CH	RCA REPLACEMENT TYPE
MOTOROLA		
MTM10N10	+N	RFM12N10
MTM10N12	+N	RFM10N12
MTM10N15	+N	RFM10N15
MTM12N05	+N	RFM15N05
MTM12N06	+N	RFM15N06
MTM12N08	+N	RFM12N08
MTM12N10	+N	RFM12N10
MTM12N18	+N	RFM12N18
MTM12N20	+N	RFM12N20
MTM15N05	+N	RFM15N05
MTM15N06	+N	RFM15N06
MTM15N12	+N	RFM15N12
MTM15N15	+N	RFM15N15
MTM15N35	+N	*RFK12N35
MTM15N40	+N	*RFK12N40
MTM2N45	+N	RFM3N45
MTM2N50	+N	RFM3N50
MTM20N08	+N	RFM18N08
MTM20N10	+N	RFM18N10
MTM25N05	+N	*RFM25N05
MTM25N06	+N	*RFM25N06
MTM3N35	+N	*RFM4N35
MTM3N40	+N	*RFM4N40
MTM4N45	+N	*RFM6N45
MTM4N50	+N	*RFM6N50
MTM5N18	+N	RFM8N18
MTM5N20	+N	RFM8N20
MTM5N35	+N	*RFM7N35
MTM5N40	+N	*RFM7N40
MTM7N12	+N	RFM8N18
MTM7N15	+N	RFM8N18
MTM7N18	+N	RFM8N18
MTM7N20	+N	RFM8N18
MTM8N08	+N	RFM8N18
MTM8N10	+N	RFM8N18
MTM8N12	+N	RFM10N12
MTM8N15	+N	RFM10N15
MTM8N18	+N	RFM8N18
MTM8N20	+N	RFM8N20
MTP1N45	+N	RFP3N45
MTP1N50	+N	RFP3N50
MTP10N05	+N	RFP15N05
MTP10N06	+N	RFP15N06
MTP10N08	+N	RFP12N08
MTP10N10	+N	RFP12N10
MTP10N12	+N	RFP10N12
MTP10N15	+N	RFP10N15
MTP12N05	+N	RFP15N05
MTP12N06	+N	RFP15N06
MTP12N08	+N	RFP12N08
MTP12N10	+N	RFP12N10
MTP12N18	+N	RFP12N18
MTP12N20	+N	RFP12N20
MTP15N05	+N	RFP15N05
MTP15N06	+N	RFP15N06
MTP15N12	+N	RFP15N12
MTP15N15	+N	RFP15N15
MTP2N35	+N	*RFP4N35
MTP2N40	+N	*RFP4N40
MTP2N45	+N	RFP3N45

INDUSTRY TYPE	CH	RCA REPLACEMENT TYPE
MOTOROLA		
MTP2N50	+N	RFP3N50
MTP20N08	+N	RFP18N08
MTP20N10	+N	RFP18N10
MTP25N05	+N	*RFP25N05
MTP25N06	+N	*RFP25N06
MTP3N35	+N	*RFP4N35
MTP3N40	+N	*RFP4N40
MTP4N45	+N	*RFP6N45
MTP4N50	+N	*RFP6N50
MTP5N18	+N	RFP8N18
MTP5N20	+N	RFP8N20
MTP5N35	+N	*RFP7N35
MTP5N40	+N	*RFP7N40
MTP7N12	+N	RFP8N18
MTP7N15	+N	RFP8N18
MTP7N18	+N	RFP8N18
MTP7N20	+N	RFP8N20
MTP8N08	+N	RFP8N18
MTP8N10	+N	RFP8N18
MTP8N12	+N	RFP10N12
MTP8N15	+N	RFP10N15
MTP8N18	+N	RFP8N18
MTP8N20	+N	RFP8N20

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Jermyn Distribution
Vestry Industrial Estate
Sevenoaks, Kent TN14 5EU
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Macro Marketing Ltd.
Burnham Lane,
Slough, Berkshire SL1 6LN
Tel: Burnham (06286) 4422

Power Technology Ltd.
Norbain House
Boulton Road
Reading, Berkshire RG2 0LT
Tel: (0734) 866766

STC Electronic Services
Edinburgh Way, Harlow
Essex, CM20 2DE
Tel: Harlow (0279) 26777

VSI Electronics Ltd.
Roydonbury Industrial Park
Horsecroft Road, Harlow
Essex CM19 5BY
Tel: Harlow (0279) 29666

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Avtotehna
P.O. Box 593, Celovska 175
Ljubljana 61000
Tel: 552 341

Zambia

African Technical Associates Ltd.
Stand 5196 Luanshya Road
Lusaka

Zimbabwe

BAK Electrical Holdings (Pvt) Ltd.
P.O. Box 2780
Salisbury

Asia Pacific

Australia

AWA Microelectronics
348 Victoria Road
Rydalmere N.S.W. 2116

Amtron Tyree Pty. Ltd.
176 Botany Street, Waterloo,
N.S.W. 2017

Bangladesh

Electronic Engineers & Consultants Ltd.
103 Elephant Road, 1st Floor
Dacca 5

Hong Kong

Gibb Livingston & Co., Ltd.
77 Leighton Road
Leighton Centre
P.O. Box 55

Hong Kong Electronic Components Co.
Flat A Yun Kai Bldg. 1/Fl
466-472 Nathan Road
Kowloon

India

Photophone Ltd.
179-5 Second Cross Road
Lower Palace Orchards
Bangalore 560 003

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NVPD Soedarpo Corp.
Samudera Indonesia Building
JL Letten, Jen. S
Parman No. 35 Slipi
Jakarta Barat

Japan

Okura & Company Ltd.
3-6 Ginza, Nichome, Chuo-Ku
Tokyo 104

Korea

Panwest Company, Ltd.
C.P.O. Box 3358
Room 603, Sam Duk Building
131, Da-Dong, Chung-Ku
Seoul, Republic of South Korea

Nepal

Continental Commercial Distributors
Durbar Marg.
Kathmandu

New Zealand

AWA NZ Ltd.
N.Z. P.O. Box 50-248
Porirua

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Philippine Electronics Inc.
P.O. Box 498
3rd Floor, Rose
Industrial Bldg., 11 Pioneer St.
Pasig, Metro Manila

Semitronics Philippines
216 Ortego Street
San Juan 3134, Metro Manila

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Device Electronics Pte. Ltd.
101 Kitchener Road No. 02-04
Singapore 0820

Microtronics Asso. Pte. Ltd.
Block 1003, Unit 35B
Aljunied Avenue 5
Singapore 1438

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C.W. Mackie & Co. Ltd.
36 D.R. Wijewardena Mawatha
Colombo 10

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Delta Engineering Ltd.
No. 42 Hsu Chang Street
8th Floor, Taipei

Multitech International Corp.
No. 315, Fu Shing North Road
Taipei

Thailand

Anglo Thai Engineering Ltd.
2160 Ramkambaeng Road
Highway Hua Mark, Bangkok

Better Pro Co. Ltd.
71 Chakkawat Road
Wat Tuk, Bangkok

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Tucuman 299,
1049 Buenos Aires
Tel: 31-3363

Radiocom S.A.
Conesa 1003,
1426 Buenos Aires
Tel: 551-2780

Tecnos S.R.L.
Independencia 1861
1225 Buenos Aires
Tel: 37-0239

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Commercial Bezerra Ltda.
Rua Costa Azevedo, 139,
CEP-69.000 Manaus/AM
Tel: (092) 232-5363

Panamericana Comercial Importadora Ltda.
Rua Aurora, 263,
01209, Sao Paulo, SP
Tel: (011) 222-3211

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Raylex Ltda.
Av Providencia 1244,
Depto.D, 3er Piso
Casilla 13373, Santiago
Tel: 749835

Industria de Radio y Television S.A. (IRT)
Vic. MacKenna 3333
Casilla 170-D, Santiago
Tel: 561667

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Carrera 12 #1906
Bogota

Electronica Moderna
Carrera 9A, NRO 19-52
Apartado Aereo 5361
Bogota, D.E.1

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J. G. Valldeperas, S.A.
Calle 1, Avenidas 1-3,
Apartado Postal 3923
San Jose
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Humberto Garcia, C. por A.
El Conde 366
Apartado de Correos 771
Santo Domingo
Tel: 682-3645

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Francisco J. Yones
3A Avenida S.O. 5
San Pedro Sula,
Honduras, Central America
Tel: 52-00-10

Ecuador

Elecom, S.A.
Padre Solano 202-OF. 8,
P.O. Box 9611, Guayaquil

El Salvador

Radio Electrica, S.A.
4A Avenida Sur Nb. 228
San Salvador
Tel: 21-5609

Radio Parts, S.A.
2A C. O. No. 319 Postal la
Dalia, P.O. Box 1262
San Salvador
Tel: 21-3019

Guatemala

Electronics Guatemalteca
13 Calle 5-59, Zona 1
P.O. Box 514
Guatemala City
Tel: 25-649

Tele-Equipos, S.A.
10A Calle 5-40, Zona 1
Apartado Postal 1798
Guatemala City
Tel: 29-805

Haiti

Societe Haitienne D'Automobiles, S.A.
P.O. Box 428,
Port-Au-Prince
Tel: 2-2347

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Republica del Salvador No. 30-102, Mexico City 1, D.F.
Tel: 510-47-49

Mexicana de Bulbos, S.A.
Michoacan No. 30
Mexico 11, D.F.
Tel: 564-92-33

Partes Electronicas, S.A.
Republica Del Salvador 30-50
Mexico City
Tel: (905) 585-3640

Raytel, S.A.
Sullivan 47 Y 49
Mexico 4, D.F.
Tel: 566-67-86

Netherland Antilles

El Louvre, S.A.
P.O. Box 138, Curacao
Tel: 54004

Nicaragua

Comercial F. A. Mendieta, S.A.
Apartado Postal No. 1956
C.S.T. 5c Al Sur 2c 1/2 Abajo
Managua

Panama

Tropelco, S.A.
Via Espana 20-18, Panama 7
Rep. de Panama

Paraguay

Compania Comercial Del Paraguay, S.A.
Casilla de Correo 344
Chile 877, Asuncion

Peru

Arven S.A.
PSJ Adan Mejia 103, OF. 33
Lima 11
Tel: 716229

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17-27 Maagdenstreet,
P.O. Box 251, Paramaribo
Tel: 71-400

Surinam Electronics
Keizerstreet 206
P.O. Box 412
Paramaribo
Tel: 76-555

Trinidad

Kirpalani's Limited
Kirpalani's Komplex
Churchill Roosevelt Highway
San Juan, Port-of-Spain
Tel: 638-2224/9

Uruguay

American Products S.A. (APSA)
Casilla de Correo 1438
Canelones 1133
Montevideo
Tel: 594210

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Residencies Camarat, Local 7
La Candelaria, Caracas
MAIL ADDRESS: Apartado Postal 20.249
San Martin, Caracas
Tel: (58-2) 571-21-46

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Residencies Camarat, Local 7
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San Diego, CA 92111
Tel: (619) 279-0420

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New England Technical Sales (NETS)
240 Pomeroy Avenue
Meriden, CT 06450
Tel: (203) 237-8827

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G.F. Bohman Assoc., Inc.
130 N. Park Avenue
Apopka, FL 32703
Tel: (305) 886-1882

G.F. Bohman Assoc., Inc.
2020 W. McNab Road
Ft. Lauderdale, FL 33309
Tel: (305) 979-0008

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Electronic Sales, Inc.(ESI)
3188 Terrace Court
Norcross, GA 30092
Tel: (404) 448-6554

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Electri-Rep
7070 W. 107th Street
Suite 160
Overland Park, KS 66212
Tel: (913) 649-2168

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New England Technical Sales (NETS)
135 Cambridge Street
Burlington, MA 01803
Tel: (617) 272-0434

Minnesota

Comprehensive Technical Sales
8053 Bloomington Freeway
Minneapolis, MN 55420
Tel: (612) 888-7011

New Jersey

Astrorep, Inc.
717 Convery Blvd.
Perth Amboy, NJ 08861
Tel: (201) 826-8050

New York

Astrorep, Inc.
103 Cooper Street
Babylon, L.I., NY 11704
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Cary, NC 27511
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Lyons Corporation
4812 Frederick Road
Suite 101
Dayton, OH 45414
Tel: (513) 278-0714

Lyons Corporation
4615 W. Streetsboro Road
Richfield, OH 44286
Tel: (216) 659-9224

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Simpson Assocs.
7324 So. 1300 E.
Suite 350
Midvale, UT 84047
Tel: (801) 566-3691

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Vantage Corp.
300 120th Avenue N.E.
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Los Altos, CA94022
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RCA
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