# RT424A

128 Mbyte DRAM Memory Module

The RT424A is a dynamic random access memory (DRAM) module organized as 33,554,432 x 144 bits. The module is compatible with 200-pin single-in-line memory module (SIMM) used in Sun SS10 and SS20 systems. It is composed of two banks of 36 4-Mbit x 4 DRAMs housed in thin small outline packages (TSOP II). Buffering is provided for all address and control pins.

FEATURES

- **Sun SS20-style 200 pin SIMM package**
- **Single 5V supply**
- **TTL compatible inputs and outputs**
- **Supports RAS-only, CAS before RAS, and hidden refresh**
- **Utilizes 4-Mbit x 4 CMOS TSOP II DRAMs**
- **60 and 70ns RAS access time versions available**

Pin Name	Function
A[11:0]	Address Inputs
CB[15:0]	Check Bits Input/Output
D[127:0]	Data Input/Output
CAS*	Column Address Strobe
OE*	Output Enable
WE*	Write Enable
BANK[1:0]*	Bank Select
RAS*	Row Address Strobe
VCC	Power (+5V)
GND	Ground
NC	No Connect

RT424A
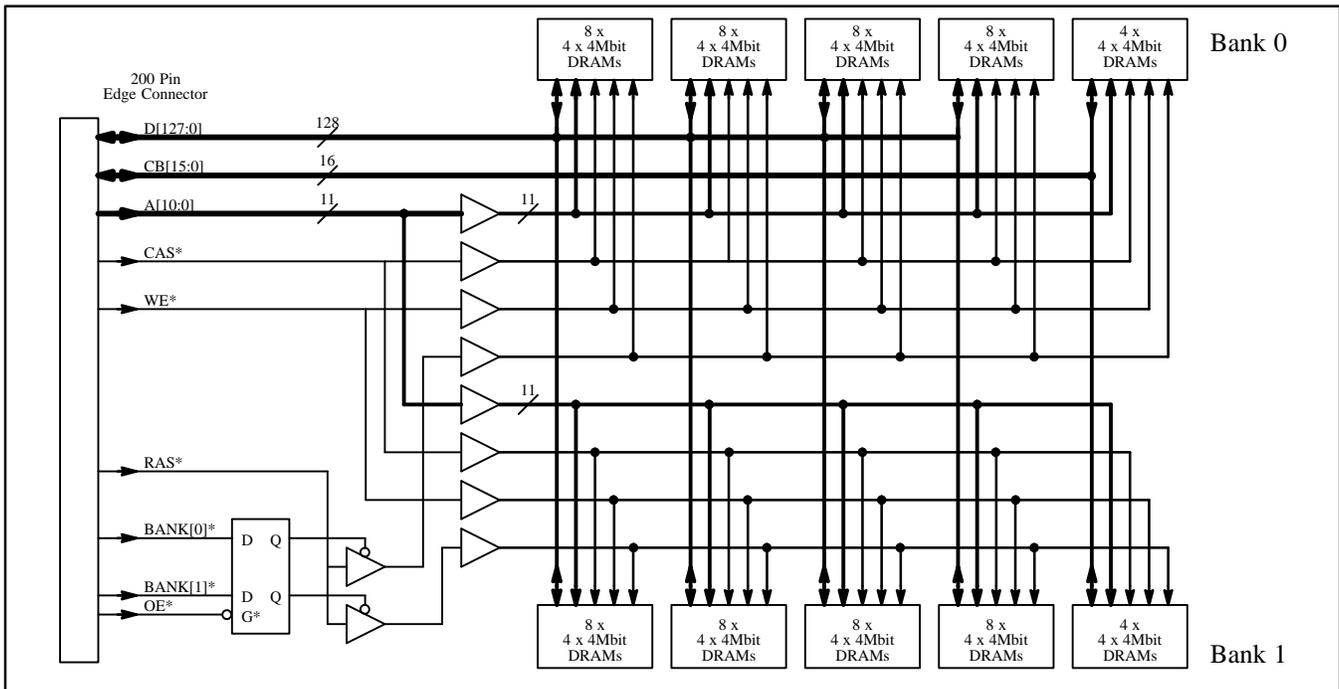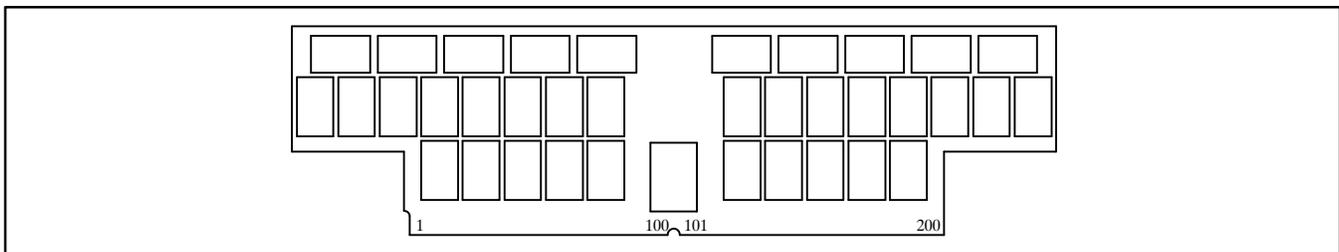
FUNCTIONAL DESCRIPTION

Device Initialization

On power-up, an initial pause of 200 microseconds is required for the DRAMs' internal bias generators to reach the correct bias voltage. This must be followed by a minimum of eight active RAS* cycles to assure all nodes have been initialized. Following any extended inactive state (greater than 32 milliseconds), a wake-up sequence of at least eight active RAS* cycles is necessary to assure proper operation.

Addressing the RAM

The eleven address pins on the SIMM are time multiplexed at the beginning of a memory cycle by two strobe signals, RAS* and CAS*, into two separate 11-bit address fields. A total of 22 address bits, eleven rows and eleven columns, will decode one of the 16,777,216 word locations in each bank.

Normal read or write cycles are initiated by providing a row address, asserting RAS*, changing the address pins to the column address, and then asserting CAS*. There are three variations in addressing the module which will be described separately below: RAS-only refresh, CAS before RAS refresh, and fast page mode.

Read Cycle

The SIMM may be read with four different types of cycles: "normal" random read cycles, fast page mode read cycles, read-write cycles, and fast page mode read-write cycles.

The normal read cycle begins as described above, with RAS* and CAS* active transitions latching the address of the desired data word. The WE* input must be inactive (high) before the fall of CAS* to enable read mode.

Write Cycle

The SIMM may be written with any of three different types of cycles: early write, fast page mode early write, and fast page mode read-write. Late write cycles are not supported, since OE* is not implemented.

A write cycle begins as described in Addressing the RAM above. Write mode is enabled by the assertion of WE* prior to the assertion of CAS*.

Fast Page Mode Cycles

Fast page mode allows faster memory operations within a row addressed page boundary. A fast page cycle is initiated by a RAS* assertion followed by a CAS* assertion. Once RAS* is asserted, CAS* may be toggled (within DRAM timing specifications), strobing new column addresses. Typically, fast page mode cycles start as normal read or write cycles. Once the timing requirements for the first cycle are met, RAS* is held low while CAS* is toggled to begin the next page mode cycle. Page mode operation is ended when RAS* and CAS* are both negated.

RAS-Only Refresh

RAS-only refresh consists of supplying the address of the row to be refreshed and toggling RAS* while CAS* remains high. An external refresh counter is required to supply the successive row addresses.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS* low before RAS*. This strobe order activates an internal refresh counter that generates the row address of the row to be refreshed. The value on all external address lines are ignored, and the data output buffer remains in the state it was in during the previous cycle. WE* must remain inactive throughout the refresh cycle.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pins. Holding CAS* active at the end of a read or write cycle while RAS* is toggled triggers a hidden refresh cycle. This is essentially the execution of a CAS before RAS refresh from a cycle already in progress. WE* must be deasserted prior to the assertion of the RAS* which triggers the hidden refresh.

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RT424A

PIN ASSIGNMENTS

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	GND	51	D[49]	101	GND	151	VCC
2	GND	52	D[54]	102	GND	152	VCC
3	D[0]	53	D[50]	103	A[6]	153	D[75]
4	D[7]	54	D[53]	104	A[7]	154	D[76]
5	D[1]	55	D[51]	105	A[8]	155	D[104]
6	D[6]	56	D[52]	106	A[9]	156	D[111]
7	D[2]	57	D[24]	107	A[10]	157	D[105]
8	D[5]	58	D[31]	108	A[11]	158	D[110]
9	D[3]	59	D[25]	109	NC	159	D[106]
10	D[4]	60	D[30]	110	WE*	160	D[109]
11	D[32]	61	D[26]	111	BANK[0]*	161	D[107]
12	D[39]	62	D[29]	112	BANK[1]*	162	D[108]
13	D[33]	63	D[27]	113	GND	163	D[80]
14	D[38]	64	D[28]	114	GND	164	D[87]
15	D[34]	65	GND	115	GND	165	D[81]
16	D[37]	66	GND	116	GND	166	D[86]
17	VCC	67	D[56]	117	CB[8]	167	GND
18	VCC	68	D[63]	118	CB[15]	168	GND
19	D[35]	69	D[57]	119	VCC	169	D[82]
20	D[36]	70	D[62]	120	VCC	170	D[85]
21	D[8]	71	D[58]	121	CB[9]	171	D[83]
22	D[15]	72	D[61]	122	CB[14]	172	D[84]
23	D[9]	73	D[59]	123	CB[10]	173	D[112]
24	D[14]	74	D[60]	124	CB[13]	174	D[119]
25	D[10]	75	CB[0]	125	CB[11]	175	D[113]
26	D[13]	76	CB[7]	126	CB[12]	176	D[118]
27	D[11]	77	CB[1]	127	D[64]	177	D[114]
28	D[12]	78	CB[6]	128	D[71]	178	D[117]
29	D[40]	79	CB[2]	129	D[65]	179	D[115]
30	D[47]	80	CB[5]	130	D[70]	180	D[116]
31	D[41]	81	VCC	131	D[66]	181	D[88]
32	D[46]	82	VCC	132	D[69]	182	D[95]
33	GND	83	CB[3]	133	D[67]	183	VCC
34	GND	84	CB[4]	134	D[68]	184	VCC
35	D[42]	85	CAS[0]*	135	GND	185	D[89]
36	D[45]	86	CAS[1]*	136	GND	186	D[94]
37	D[43]	87	RAS*	137	D[96]	187	D[90]
38	D[44]	88	RAS*	138	D[103]	188	D[93]
39	D[16]	89	NC	139	D[97]	189	D[91]
40	D[23]	90	NC	140	D[102]	190	D[92]
41	D[17]	91	NC	141	D[98]	191	D[120]
42	D[22]	92	GND	142	D[101]	192	D[127]
43	D[18]	93	A[0]	143	D[99]	193	D[121]
44	D[21]	94	A[1]	144	D[100]	194	D[126]
45	D[19]	95	A[2]	145	D[72]	195	D[122]
46	D[20]	96	A[3]	146	D[79]	196	D[125]
47	D[48]	97	A[4]	147	D[73]	197	D[123]
48	D[55]	98	A[5]	148	D[78]	198	D[124]
49	VCC	99	GND	149	D[74]	199	GND
50	VCC	100	GND	150	D[77]	200	GND

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RT424A

ABSOLUTE MAXIMUM RATINGS [1]
(Provided as guidelines; not tested.)

Parameter	Description	Rating	Units
V_{CC}	Supply Voltage Range	–0.5 to +7.0	V
P_D	Maximum Power Dissipation	47	W
V_{IN}, V_{OUT}	Input Voltage Range	–0.3 to +7.0	V
T_{STG}	Storage Temperature	–20 to +75	°C

RECOMMENDED OPERATING CONDITIONS [2]

Parameter	Description		Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
V_{IH}	Input HIGH Voltage		2.4		V_{CC} + 0.5V	V
V_{IL}	Input LOW Voltage		–0.5		0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 5.0 mA	2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.2 mA			0.4	V
I_{IZ}	Input Leakage Current	V_{CC} = Max., $V_{SS} \leq V_{IN} \leq V_{CC}$	–200		200	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \leq V_{OUT} \leq V_{CC}$	–20		20	μA
T_A	Operating Ambient Air Temperature [3]		0		50	°C

CAPACITANCE [4]

Parameter	Description		Max.	Units
C_{I1}	Input Capacitance: A[11:0], WE*		12	pF
C_{I2}	Input Capacitance: RAS*, CAS[1:0]*	V_{CC} = 5.0V	12	pF
C_{I3}	Input Capacitance: BANK[1:0]*, OE*	T_A = 25°C f = 1 MHz	8	pF
C_{IO}	Input/Output Capacitance: D[127:0], CB[15:0]		20	pF

Notes:
1. All power and ground pins must be connected to other pins of the same type before any power is applied. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Exposure to voltages above those recommended may lead to lower device reliability.
2. Recommended use of this module does not include "hot-socketing" or "live-insertion" (i.e., it is not recommended that the RT424A be placed in a socket with power applied).
3. Non-condensing.
4. Tested initially and after any design or process changes that may affect these parameters.

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ORDERING INFORMATION

RT   424A   –   XX   F

Type (F = Fast page mode)

Speed (60 = 60ns, 70 = 70ns)

Part Number

ROSS Technology Prefix
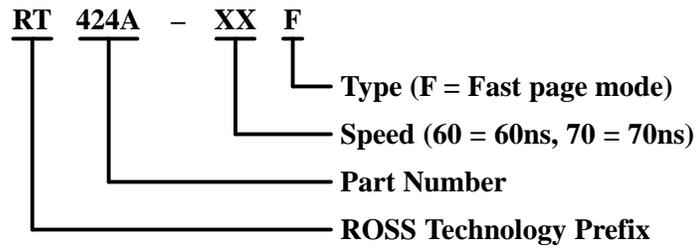
For up-to-date ordering and sales information call (512) 436−2555.