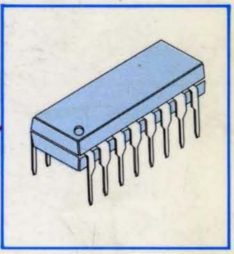
SAMSUNG

Data Book

Linear IC

Vol. 1, 1990



- Audio
- CDP
- Toy Radio Control Actuator

SAMSUNG
DATA BOOK LIST

I. Semiconductor Product Guide

II. Transistor Data Book

Vol. 1: Small Signal TR
Vol. 2: Bipolar Power TR
Vol. 3: TR Pellet

III. Linear IC Data Book

Vol. 1: Audio/CDP/Toy
Vol. 2: Video
Vol. 3: Telecom
Vol. 4: Industrial
Vol. 5: Data Converters

IV. CMOS Consumer IC Data Book

V. High Speed CMOS Logic Data Book

VI. MOS Memory Data Book

VII. SFET Data Book

VIII. MPR Data Book

IX. CPL Data Book

X. Dot Matrix Data Book

TABLE OF CONTENTS

Audio Application

Device	Function	Package	Page
KA1222	Dual Low Noise Equalizer Amplifier	8 DIP	55
KA2201	1.2W Audio Power Amplifier	8 DIP	59
KA2201B	0.5W Audio Power Amplifier	8 DIP	63
KA2206	2.3W Dual Audio Power Amplifier	12 DIP IF	66
KA22062	4.5W Dual Power Amplifier	12 SIP H/S	74
KA22063	4.5W Dual Power Amplifier	12 SIP H/S	81
KA22065	4.6W Dual Power Amplifier	12 SIP H/S	87
KA2209	Dual Low Voltage Power Amplifier	8 DIP	90
KA2210	5.5W Dual Power Amplifier	12 SIP H/S	93
KA22101	23W Power Amplifier	12 ZIP H/S	98
KA22102	15W Dual Power Amplifier	17 ZIP H/S	105
KA22103	19W Dual Power Amplifier	17 ZIP H/S	111
KA2211	5.8W Dual Power Amplifier	12 SIP H/S	117
KA2212	0.5W Audio Power Amplifier	9 SIP	122
KA2213	One-Chip Tape Recorder System	14 DIP H/S	127
KA22130	One-Chip Tape Recorder System	16 DIP	134
KA22131	Dual Pre-Power Amplifier for Auto Reverse	24 SOP	138
KA22134	Dual Pre-Power Amplifier with DC Volume Control	16 DIP	145
KA22135	Dual Pre-Power Amplifier and DC Motor Speed Controller	22 SDIP	150
KA22136	Dual Pre-Power Amplifier, Volume Controller and DC Motor Speed Controller	28 SDIP/28 SOP	155
KA2214	1W Dual Power Amplifier	14 DIP H/S	159
KA2220	Equalizer Amplifier with ALC	9 SIP	164
KA2221	Dual Low Noise Equalizer Amplifier	8 SIP	169
KA22211	Dual Low Noise Equalizer Amplifier	8 SIP	173
KA2223	5-Band Graphic Equalizer Amplifier	16 DIP	177
KA22231	5-Band Dual Graphic Equalizer Amplifier	28 SOP	183
KA22232	3-Band Dual Graphic Equalizer Amplifier	20 SOP	187
KA22233	3-Band Dual Graphic Equalizer Amplifier	22 DIP	191
KA22234	5-Band Dual Graphic Equalizer Amplifier	24 ZSIP	195
KA22235	5-Band Graphic Equalizer Amplifier	18 ZIP	199
KA2224	Dual Equalizer Amplifier with ALC	14 DIP	204
KA22241	Dual Equalizer Amplifier with ALC	9 SIP	211
KA22242	Dual Equalizer Pre-Amplifier with ALC	10 SIP	216
KA2225	Dual Pre-Amplifier for 3V Using	16 DIP/16 SOP	224
KA22261	Dual Equalizer Amplifier with Ree AMP	16 DIP	229
KA2228	Dual Equalizer Amplifier System	21 ZSIP	235
KA22291	Quad Equalizer Amplifier for Double Cassette	24 SDIP	245
KA2230	9-Program Music Selector	22 DIP	250
KA2231	Audio Level Sensor	9 SIP	257
KA22421	AM 1-Chip Radio	16 DIP/16 SOP	262
KA22426	AM/FM One-Chip Radio	28 DIP/28 SOP	272
KA22427	AM/FM 1-Chip Radio	16 DIP	276
KA22429	FM One-Chip Radio	16 SOP	285
KA2243	AM/FM IF System	16 DIP	290
KA2244	FM IF System for Car Radio	9 DIP	296
KA22441	FM IF System for Car Stereo	16 ZSIP	300

Audio Application (Continued)

Device	Function	Package	Page
KA2245	FM IF System for Car Radio	7 SIP	308
KA22461	Electronic Tuning AM Radio Receiver for Car Stereo	19 ZSIP	312
KA2247	FM IF/AM Tuner System	16 DIP	317
KA22471	FM IF/AM Tuner System	16 DIP	322
KA2248	3V FM IF/AM Tuner System	16 DIP/20 SOP	327
KA2249	FM Front End Portable Radio	7 SIP/8 SOP	332
KA22495	FM Front End for FM Band	9 SIP/14 SOP	336
KA22496	FM Front End for TV Band	9 SIP	344
KA2261	FM Stereo Multiplex Decoder	16 DIP	352
KA2262	FM Stereo Multiplex Decoder for Car Stereo	16 ZSIP	357
KA2263	FM Stereo Multiplex Decoder	9 SIP	367
KA2264	FM Stereo Multiplex Decoder	9 SIP/16 SOP	371
KA2265	Vco Non-Adjusting FM Stereo Multiplex Decoder	16 DIP	376
KA2266	MPX for Car Stereo	16 ZIP	382
KA2271	Dolby B-Type Noise Reduction Processor	16 DIP	386
KA22711	Dolby B-Type Noise Reduction Processor	16 DIP	393
KA22712	Dolby B-Type Noise Reduction Processor	16 DIP	400
KA2272	FM Noise Canceller	16 ZSIP/16 SOP	407
KA2281	5-Dot Dual Led Level Meter Driver	16 DIP	413
KA2283	5-Dot Dual Led Level Meter Driver	16 DIP	416
KA2284/85	5-Dot Led Level Meter Driver	9 SIP	420
KA2286/87	5-Dot Led Linear Level Meter Driver	9 SIP	423
KA2288	7-Dot Led Level Meter Driver	16 DIP	426
KA2292	AM/FM Tuner + MPX	24 SDIP	429
KA2293	AM/FM Tuner + MPX	24 SDIP	433
KA2401	DC Motor Speed Controller	8 DIP	437
KA2402	Low Voltage DC Motor Speed Controller	8 DIP	443
KA2404	DC Motor Speed Controller	TO-92L	450
KA2407	DC Motor Speed Controller	TO-126	456
KA7226	Dual Equalizer Amplifier with ALC	14 DIP	460
KA8602	Low Voltage Audio Amplifier	8 DIP/8 SOP	466
LM386	Low Voltage Audio Power Amplifier	8 DIP/8 SOP	473

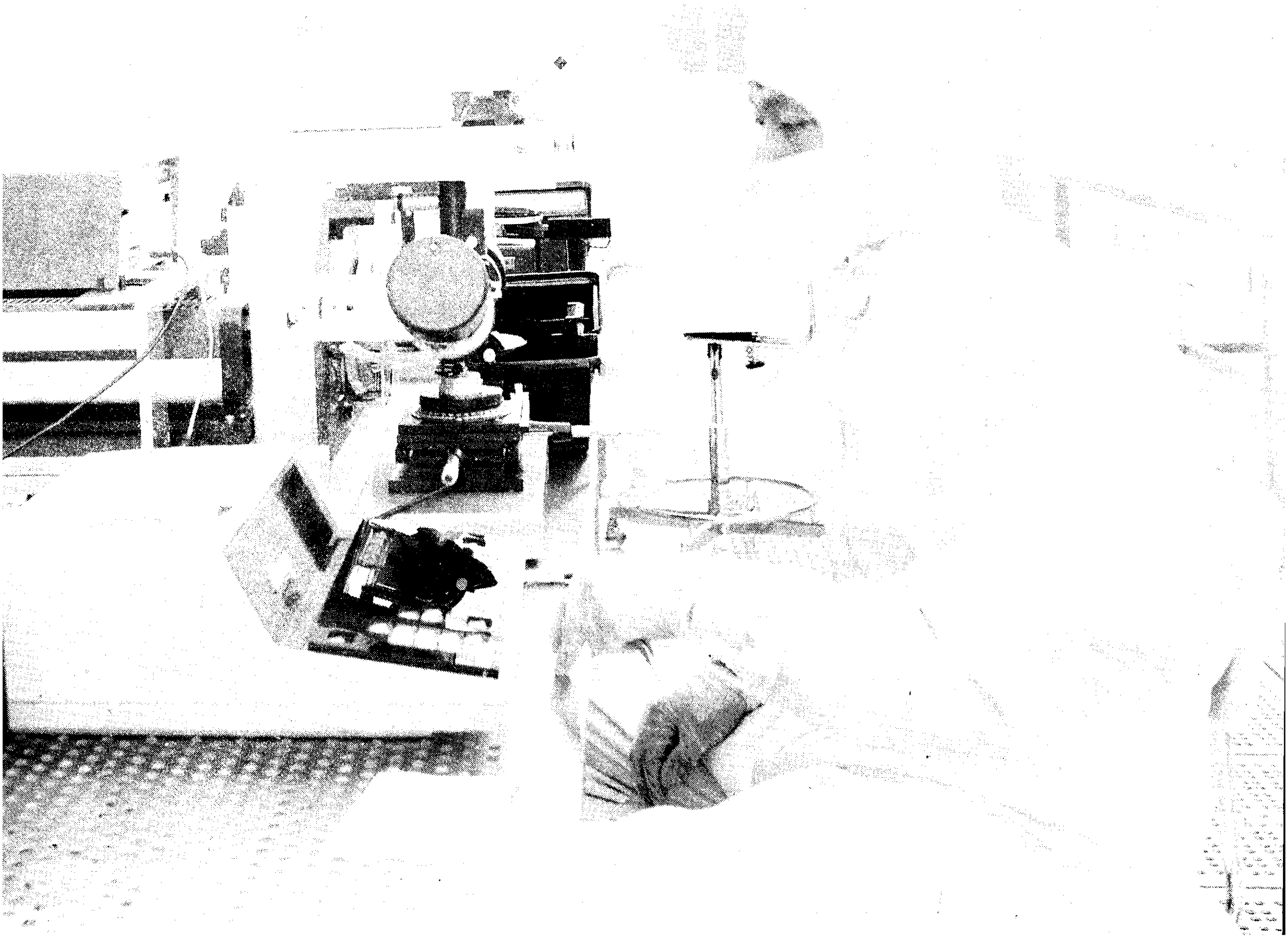
CDP Application

Device	Function	Package	Page
KA9201	RF and for CDP	30 SOP	551
KS5990	Digital Signal Processor	80 FQP	449
KS5991	Digital Signal Processor	80 FQP	508
KA8309	Servo Signal Processor	48 FQP	537
KA9255	PWM Motor Driver	22 SOP	568
KA9256	Dual Power Operational Amplifier	10 SIP H/S	573
KA9257	Dual Power Operational Amplifier	12 SIP H/S	575
KDA0316	16-bit D/A Converter for CDP	20 DIP/20 SOP	579
KS56C820	4-bit Microcontroller	80 FQP	588

Toy Application

Device	Function	Package	Page
KA2303	Toy Radio Control Actuator	9 SIP	595
KA2304	Toy Radio Control Actuator	9 SIP	601
KA2305A	Toy Radio Control Actuator (Rx)	12 SIP-SH	603
KA2306A	Toy Radio Control Actuator (Rx)	14 DIP	609
KA2309	Toy Radio Control Actuator (Rx)	16 DIP	614
KA2310	Toy Radio Control Actuator (Tx)	9 SIP	622
KA2311	Toy Radio Control Actuator (Rx)	16 DIP	625
KA2312	Toy Radio Control Actuator (Tx)	9 SIP	630
KA2314	Toy Radio Control Actuator (Tx)	9 SIP	633
KA2303	Application Note		638
KA2309	Application Note		645
KA2311	Application Note		655
KA2312	Application Note		666

QUALITY & RELIABILITY 1



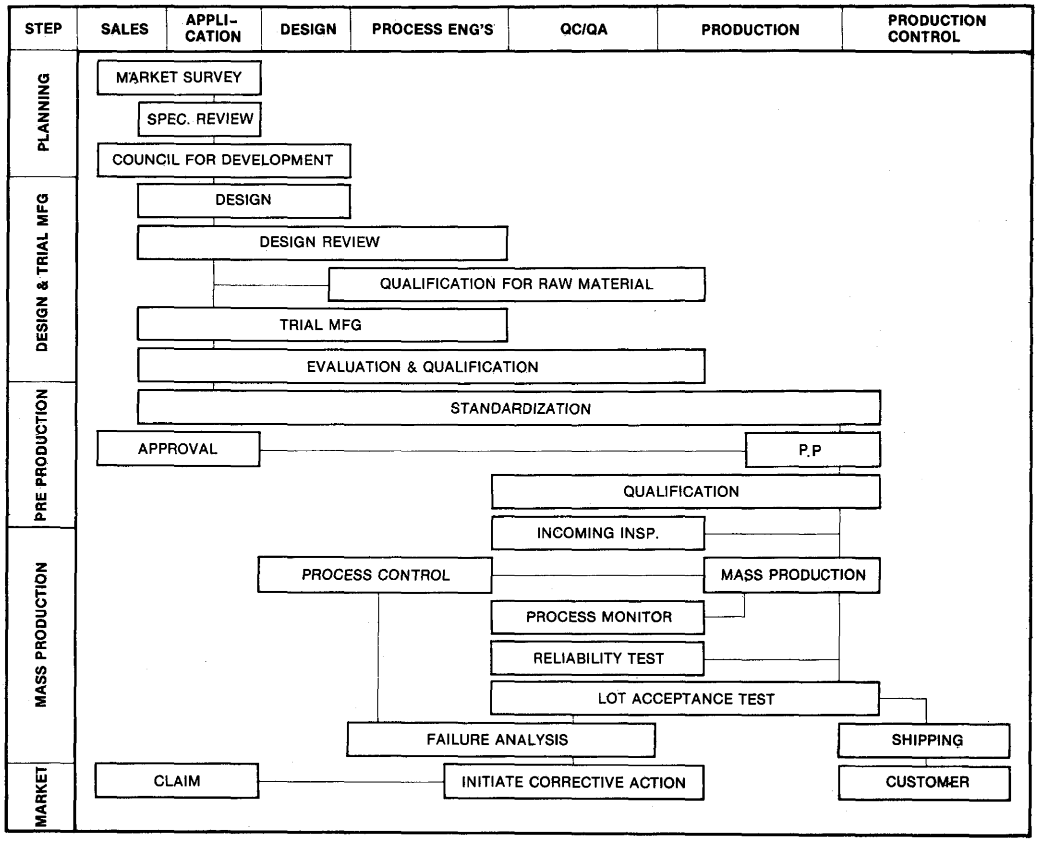
1. INTRODUCTION

SEC has been providing a wide variety of semiconductor products to the world since 1974. Since this time, extensive in-sights have been gained to create methods which most effectively result in reliable products. The worldwide customers of SEC have encouraged and helped develop the existing manufacturing and quality philosophy that is a way of life for SEC management and it's employees. This philosophy dictates the need for a zero defect environment through out SEC's processes leading ultimately to total customer satisfaction. By developing and using methods of Statistical Process Control and Statistical Quality Control, SEC has made great strides in improving product quality & reliability. The direct result of these improvements has been reduced product DPM (Defects Per Million) to levels below customer requirements. SEC's repeated ability to exceed requirements for customer's "Dock to Stock" programs and our commitment to all our customers needs, has made SEC the company to watch as we move ahead into the 1990's and beyond.

SEC's linear IC products are among the most reliable in the industry. SEC has always made a commitment to achieve the highest possible quality, reliability, and customer satisfaction with its products. Extensive qualification, monitor and outgoing programs are used to scrutinize product quality and reliability. Stringent controls are applied to every wafer fabrication and assembly lot to achieve reproducibility, and therefore maintain product reliability.

In this chapter, the quality and reliability programs established at SEC will be discussed. In addition, a description of reliability theory, reliability tests and various support efforts provides a broad framework from which to comprehend SEC quality and reliability.

To better understand the Quality Department's role in product development and manufacturing, a detailed diagram is listed below. As can be noted, Quality Engineering is involved in all phases, save that of initial product planning.



Quality Assurance During Development

2. QUALITY & RELIABILITY PROGRAM

2.1 QUALIFICATION

Procedures to qualify devices are listed below. There are both general and product-specific requirements. Procedures are detailed for new products, die-only qualifications, and package-only qualifications. The latter two are for products and/or packages already qualified, but where there is room for further product optimization.

Qualification Program

* New Product	* New Process Wafer-fabrication	Package Sub-assembly	** Other
• HOPL 1000HR • HTRB 1000HR • IOPL 1000HR • HTS 1000HR • PCT 168HR • WHOPL 1000HR • WHTRB 1000HR • T/C, T/S 200CYC. • P/C 20000CYC. • Solderability • Other as applicable	• HOPL 1000HR • HTRB 1000HR • HTS 1000HR • PCT 168HR • WHOPL 1000HR • WHTRB 1000HR • T/C, T/S 200CYC.	• HOPL 500HR • HTRB 500HR • T/C 200CYC. • T/S 200CYC. • PCT 168HR • Other as applicable	• Same as New product Qual.

*Testing time for each test items depends on the grade (group) of devices. (see the device group list 2.1 2))

** Design, Equipment, Material(s), etc....

1) PROCESS DEVELOPMENT QUALIFICATION

Purpose: To investigate the change of a process parameter and then apply it to a production process by reliability testing of a process which has been newly developed.

New Process, Wafer Fabrication Qualification

No	Test Item	Test Condition	Package	
			L-IC	Discrete
1	High Temperature Operating Life (HOPL)	$T_a = T_{opr}(max)$ $V_{CC} = V_{CC}(max)$ STATIC, DYNAMIC 1000HRS	YES	—
2	High Temperature Reverse Bias (HTRB)	$T_a = T_j(max)$ $V_{CB} = 0.8 \times V_{CBO}$ 1000HRS	—	YES
3	High Temperature Storage (HTS)	$T_a = T_j(max)$ 1000HRS	YES	YES
4	Pressure Cooker Test (PCT)	$T_a = 121°C \pm 2°C$ RH = 100% 15 PSIG 168HRS	YES	YES
5	Wet High Temperature Operating Life (WHOPL)	$T_a = 85°C$, RH = 85% $V_{CC} = V_{CC}(min)$ 1000HRS	YES	—
6	Wet High Temperature Reverse Bias (WHTRB)	$T_a = 85°C$, RH = 85% $V_{CB} = 0.8 \times V_{CBO}$ 1000HRS	—	YES
7	Thermal Shock (T/S)	$-65°C \rightleftharpoons 150°C$ (Liquid) 5min, <10sec, 5min 200 cycles	YES	YES
8	Temperature Cycle (T/C)	$-65°C \rightleftharpoons 150°C$ (Air) 10min, 10min 200 Cycles	YES	YES

When the results of a reliability test are good, the process characteristics good and the yield level is satisfied, the process can be applied to production. If there are any problems found in a process after it has been applied to production, the problem will be investigated in detail and the process will be revised. Once the process has been revised and approved it will again be applied to production.

2) PRODUCT DEVELOPMENT QUALIFICATION

Purpose: To develop a stable and uniform product that satisfies the customer's requirements for quality by using the exact reliability test specification called out for the new product.

Products are grouped according to the importance of their application.

Group 1	Group 2	Group 3
1. A/D, D/A Converter 2. IC for LCD 3. IC for PC 4. ASIC Master 5. Codec 6. MPR 7. IC for Exchange 8. New Products	1. Transistor 2. Regulator/OP AMP 3. IC for Telephone 4. Comparator/Timer 5. MICOM 6. Audio/Video IC 7. General Mos IC	1. ASIC Opinion Product 2. Toy/Melody IC 3. MICOM family 4. Products Except Group 1, Group 2 Products

New Product Qualification Test Items

No.	Test Item	Test Condition	Part		Reference Method	Note
			L-IC	Discrete		
1	High Temperature Reverse Bias (HTRB)	$Ta = T_j(max)$ $V_{CB} = 0.8 \times V_{CBO}$ 1000HRS	—	YES		
2	High Temperature Operating Life (HOPL)	$Ta = T_{opr}(max)$ $V_{CC} = V_{CC}(max)$ Static, Dynamic 1000HRS	YES	—	MIL-STD-883 1005	
3	High Temperature Storage (HTS)	$Ta = T_{stg}(max)$ 1000HRS	YES	YES		
4	Operating Life (OPL)	Ta = 25°C $P_C = P_C(max)$ 1000HRS	—	YES	MIL-STD-750 1026.3	For Small-Signal Device
5	Intermittent OPL (IOPL)	Ta = 25°C $P_C = P_C(max)$ 2min/2min On/Off 1000HRS	—	YES	MIL-STD-750 1036.3	
6	Power Cycle (P/C)	$\Delta T_j = 125°C$ 120Sec/120Sec On/Off 10000CYC.	YES	YES		For PWR TR, PWR IC
7	Pressure Cooker Test (PCT)	Ta = 121°C ± 2°C RH = 100% 15PSIG 168HRS	YES	YES		
8	Wet High Temperature Reverse Bias (WHTRB)	Ta = 85°C, RH = 85% $V_{CB} = 0.8 \times V_{CBO}$ 1000HRS	—	YES		
9	Wet High Temperature Operating Life (WHOPL)	Ta = 85°C, RH = 85% $V_{CC} = V_{CC}(min)$ Pdmin 1000HRS	YES	—		
10	Thermal Shock (T/S) (Liquid)	−65°C↔150°C 5min, <10Sec, 5min 200 Cycles	YES	YES	MIL-STD-883 1011	
11	Temperature Cycle (T/C) (Air)	−65°C↔150°C 10min, 10min 200 Cycles	YES	YES	MIL-STD-883 1011	
12	Solder Heat Resistance (S/H)	Ta = 260°C ± 5°C t = 10 ± 2Sec	YES	YES	MIL-STD-750 2031.1	
13	Solderability	Ta = 245°C ± 5°C t = 5 ± 0.5sec Reject is >10% uncovered surface	YES	YES	MIL-STD-883 2003	
14	Salt Atmosphere	Ta = 35°C, 5% NaCl 24HRS	YES	YES	MIL-STD-883 1009A	

New Products Qualification Test Item (Continued)

No.	Test Item	Test Condition	Part		Reference Method	Note
			L-IC	Discrete		
15	Mechanical Shock	1500G, 0.5ms 3 Times Each direction of X, Y and Z Axis	YES	YES	MIL-STD-750 2016	For Hermetic
16	Vibration	20G, 3 Axis f=20 to 2000 cps for 4 min, 4 cycles	YES	YES	MIL-STD-883 2007	For Hermetic
17	Constant Acceleration	2000G X,Y,Z Axis 1min for each Axis	YES	YES	MIL-STD-883 2001	For Hermetic
18	ESD (Human Body Model)	$R=1.5k\Omega$ $C=100pF$ 5 Discharge $V \geq \pm 1000V$	YES	YES	MIL-STD-883 3015	
19	Latch-up Test		YES	—	—	For CMOS
20	Fine Leak Gross Leak	Helium Fluoro Carbon	YES	YES	MIL-STD-883 1014	For Hermetic

Note) • SOT-23, TO-92S PKG: PCT-48HR

3) PACKAGE DEVELOPMENT QUALIFICATION

Purpose: Whenever a new package type is developed, it must meet the specifications for devices that have been qualified and have maintained certain specified quality levels before the new package type may be applied to production.

Flow	Contents	Remarks
	Beginning of PKG development	Select representative device for product group (proceed at least 2 lots)
	Ass'y Qual	• Push Test • Die Thick • Bond Pull • Lead Torque • MPT • Dimension • X-Ray • Solderability
	Reliability Qual	• HTRB (TR) • HOPL (IC) • T/C • PCT • LTS • S/H • Vibration • M/S • Const
	Approvement of Qual	• New PKG Development will be approved when Rel qual is good for 500HR.

Package Sub-Assembly Qualification Test Items

No.	Test Item	Test Condition	Package		Notes
			Plastic	Hermetic	
1	High Temperature Reverse Bias (HTRB)	$Ta = T_j(max)$ $V_{CB} = 0.8 \times V_{CBO}$ 500HRS	YES	YES	For Discrete
2	High Temperature Operating Life (HOPL)	$Ta = T_{opr}(max)$ $V_{CC} = V_{CC}(max)$ Static, Dynamic, 500HRS	YES	YES	For IC
3	Temperature Cycle (T/C)	$-65°C \rightleftharpoons 25°C \rightleftharpoons 150°C$ 10min, 5min, 10min 200 CYCLES	YES	YES	
4	Pressure Cooker Test (PCT)	$Ta = 121°C \pm 2°C$ RH = 100%, 15PSIG 168HRS	YES	—	
5	Thermal Shock (T/S)	$-65°C \rightleftharpoons 150°C$ (Liquid) 5min, < 10sec, 5min 200 CYCLES	YES	YES	
6	Solder Heat Resistance (S/H)	$260°C \pm 5°C$ 10 ± 1 sec Once without Flux	YES	YES	
7	Vibration (Variable-Frequency)	100 ~ 2000 ~ 100Hz 20G, 5min, 5Times, X, Y, Z	—	YES	For Discrete, others as applicable
8	Mechanical Shock (M/S)	1500G, 0.5ms 3 Times, X, Y, Z	—	YES	same as above
9	Constant Acceleration	20000G X, Y, Z Axis 1 min for each Axis	—	YES	same as above

4) CHANGE QUALIFICATIONS:

Purpose: To apply changes to production processes and designs by evaluating the quality levels for those processes and designs of devices in production.

Classification		Change
Design		Change of more than 1EA MASK for the product in production.
Process	Ass'y	• D/A • Coating • W/B • Mold
	Diffusion	• Diffusion/Photo/Etch, etc. • Metalization • Passivation

Procedure: Issuance of EIN for the change → Review of initial characteristics → Reliability test → Issuance of ECN (register of specification) → Application for production. Evaluation level: LTPD 10% (1/2)

2.2 MONITOR PROGRAM

1) ON GOING PROCESS CONTROL

All parameters of each process are controlled by SPC (Statistical Process Control). All resultant SPC data is gathered by computers and recorded automatically. Trends of each parameter are plotted on control charts by the computer and corrective actions are immediately taken whenever a parameter goes "out-of-control" beyond the control limits.
Whenever a parameter goes "out-of-control" in a process, engineers involved with that particular process have meetings to decide the disposition of those lots that were effected by the out-of-control process and corrective actions are implemented. In the case of critical defects, all lots are scrapped by MRB (Material Review Board).
As the key item of ongoing process control, Cp or Cpk value is controlled by computer for each process. The UCL and LCL for each process is then determined by the computer generated Cp or Cpk value. Cp or Cpk values are continually upgraded to insure the stabilization of process and a QIP (quality improvement plan) is made out to drive defects down to zero.
Process capabilities of each process are totaled and analyzed and those results of analysis are reflected on the QIP. The stabilization and maximization of process capabilities are driven by SPC.

2) PRODUCT RELIABILITY MONITOR

The reliability monitor program begins where the qualification program ends, at the start-up of limited production. Everything that is subject to qualification is considered subject to the monitor program. Generally, the product to be used for reliability monitors is gathered from each fab lot each month, where the product selected is representative of:

1) each fab process technology
2) each generic product type
3) each package technology
4) each subassembly plant

The product is shipped directly to the appropriate Q & R group, which puts the product through a series of electrical, mechanical, thermal, and environmental tests that usually are identical to those used initially for qualifying the product. Most tests are of short duration, but some may extend out to thousands of hours. Each month the test results are evaluated and problems, should they exist, identified.
Each monitor failure is analyzed. If a problem is detected where the failure rate is greater than that considered acceptable, or a reliability problem is suspected, a Material Review Board (MRB) is called. This meeting is attended by appropriate Q & R personnel, scheduling personnel, engineering, and any other affected group.
This group reviews the data, decides on disposition of the affected material, decides on appropriate corrective action, and basically controls the problem or issue until it is satisfactorily resolved.

3) FINAL QUALITY ASSURANCE PROGRAM

After the completion of the entire manufacturing process a sample of each lot is pulled and the data sheet verification test is repeated. This final verification objective is to ensure that test system to test system variations are not compromising the quality, and that inadvertent system or handling problems have not occurred.

4) ENVIRONMENT MONITOR

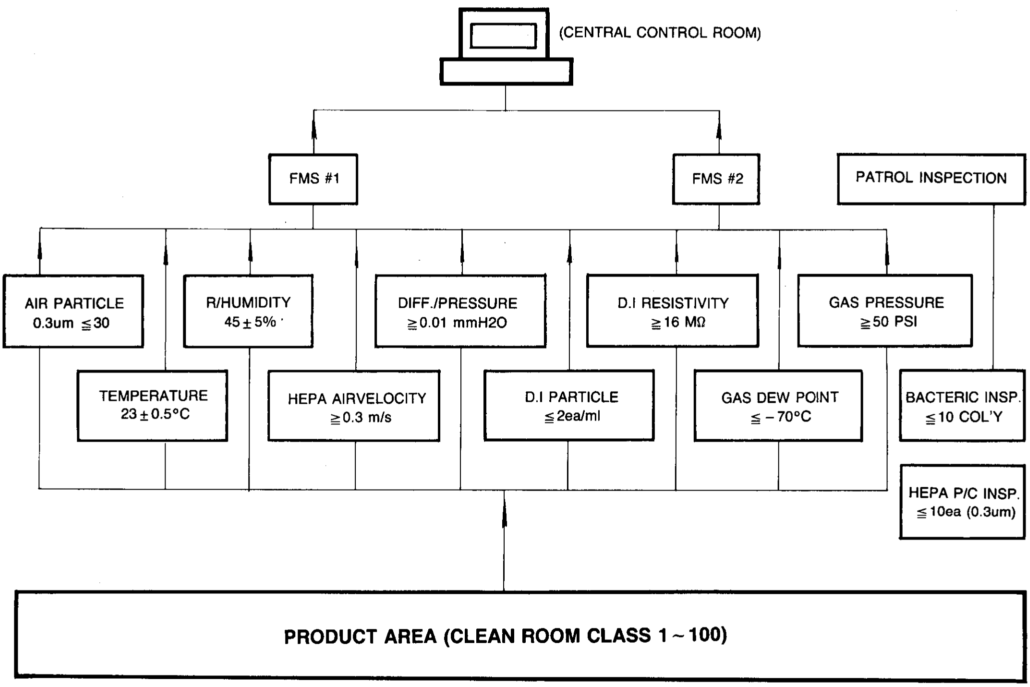
- **Instruments**

- F.M.S #1 (HIAC/ROYCO System 1 Set)
- F.M.S #2 (P.M.S System 1 Set)
- Control Particle Monitoring System (2 Set)

(the above three: On line monitoring system (Central control room))

- Portable Particle Counter, Sensors

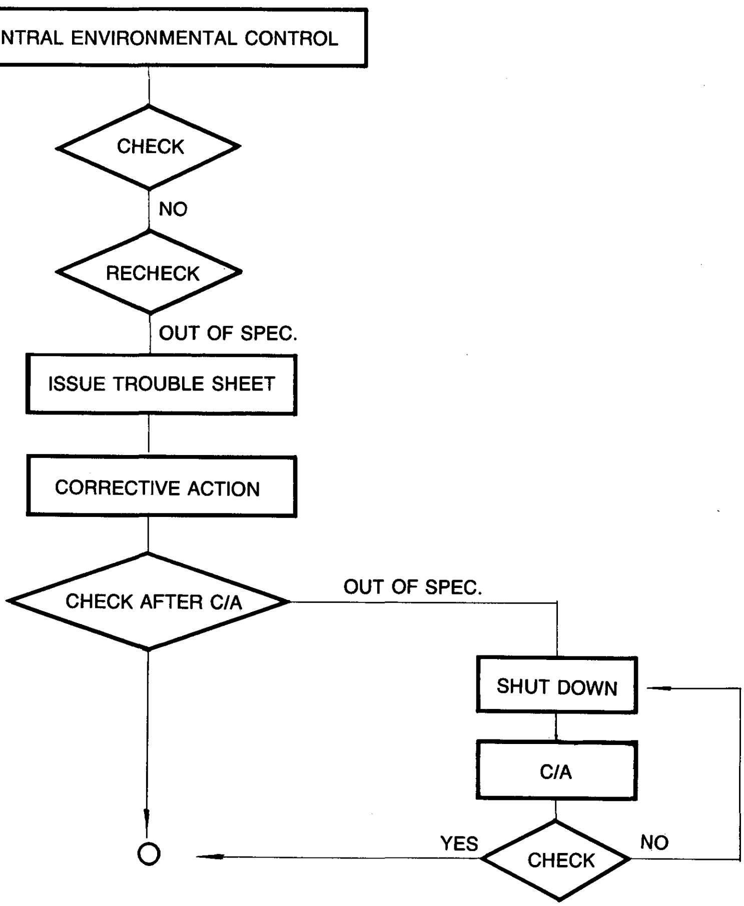
- **Block Diagram**



- **Environment Monitor**

Item	Frequency
1. Particle (Air, D-I Water)	5 min
2. Temperature, Relative Humidity	5 min
3. D.I Resistivity	5 min
4. Differential Pressure	5 min
5. HEPA Air Velocity	5 min
6. Gas (H_2, O_2, N_2, Air) Dew Point	5 min
7. Gas Pressure	5 min
8. HEPA Filter Particle	All HEPAs/1 room/Day
9. D-I Bacteria Main Lot	Weekly
10. D-I Bacteria Using Lot	Monthly

Corrective Action Requirement



2.3 QUALITY CONFORMANCE PROGRAM

1) DESCRIPTION

SEC has established a comprehensive reliability program to monitor and ensure the ongoing reliability of the Linear IC family. This program involves not only reliability data collection and analysis on existing parts, but also rigorous in-line quality controls for all products.
Listed below are details of tests performed to ensure that manufactured product continues to meet SEC's stringent quality standards. In line quality controls are reviewed extensively in later sections.
The tests run by the quality department are accelerated tests, serving to model "real world" applications through boosted temperature, voltage, and/or humidities. Accelerated conditions are used to derive device knowledge through means quicker than that of typical application situations. These accelerated conditions are then used to assess differing failure rate mechanisms that correlate directly with ambient conditions. Following are summaries of various stresses (and their conditions) run by SEC on Linear IC products.

2) HIGH TEMPERATURE OPERATING LIFE TEST (HOPL)

(T_j = 125°C, $V_{CC} = V_{CC}$ max, static)

High temperature operating life test is performed to measure actual field reliability. Life tests of 1000HR to 2000HR durations are used to accelerate failure mechanisms by operating the device at an elevated ambient temperature (125°C). Data obtained from this test are used to predict product infant mortality, early life, and random failure rates. Data are translated to standard operating temperatures via failure analysis to determine the activation energy of each of the observed failures, using the Arrhenius relationship as previously discussed.

3) WET HIGH TEMPERATURE OPERATING LIFE TEST (WHOPL)

(Ta = 85°C, R.H. = 85%, $V_{CC} = V_{CC}$ opt, static)
Wet high temperature operating life test is performed to evaluate the moisture resistance characteristics of plastic encapsulated components. Long time testing is performed under static bias conditions at 85°C/85 percent relative humidity with nominal voltages. To maximize metal corrosion, the biasing configuration utilizes low power levels.

4) INTERMITTENT OPERATING LIFE (IOPL)

(Pmax, 25°C, 2min on/2 min off)

This test is normally applied to scrutinize die bond thermal fatigue. A stressed device undergoes an "ON" cycle, where there is thermal heating due to power dissipation, and an "OFF" cycle, where there is thermal cooling due to lack of inputted power. Die attach (between die and package) and bond attach (between wire and die) are the critical areas of concern.

5) HIGH TEMPERATURE STORAGE TEST (HTS)

(Ta = 125°C, UNBIASED)

High temperature storage is a test in which devices are subjected to elevated temperatures with no applied bias. The test is used to detect mechanical instabilities such as bond integrity, and process wearout mechanisms.

6) PRESSURE COOKER TEST (PCT)

(121°C, 15PSIG, 100% R.H., UNBIASED)

The pressure cooker test checks for resistance to moisture penetration. A highly pressurized vessel is used to force water (thereby promoting corrosion) into packaged devices located within the vessel.

7) TEMPERATURE CYCLING (T/C)

(−65°C to +150°C, AIR, UNBIASED)

This stess uses a chamber with alternating temperatures of −65°C and +150°C (air ambient) to thermally cycle devices within it. No bias is applied. The cycling checks for mechanical integrity of the packaged device, in particular bond wires and die attach, along with metal/polysilicon microcracks.

8) THERMAL SHOCK (T/S)

(−65°C to +150°C, LIQUID, UNBIASED)
This stress uses a chamber with alternating temperatures of −65°C to +150°C (liquid ambient) to thermally cycle devices within it. No bias is applied. The cycling is very rapid, and primarily checks for die/package compatibility.

9) RESISTANCE TO SOLDER HEAT

(UNBIASED, 260°C, 10 sec)

Solder Heat Resistance is performed to establish that devices can withstand the thermal effects of solder dip, soldering iron, or solder wave operations.

10) MECHANICAL SHOCK

(UNBIASED, 1500g, Pulse = 0.5msec)

This test determines the suitability of a device to be used in equipment where mechanical "shocks" may occur. Such shocks result from sudden or abrupt changes produced by rough (non-standard) handling, transportation, or field operations.

11) VARIABLE FREQUENCY VIBRATION

(UNBIASED, Range = 100 to 2000Hz)

Variable Frequency Vibration is done to model the effects of differential vibration in the specified range. Die attach and bonding integrity are particularly stressed, testing the mechanical soundness of device packaging.

12) CONSTANT ACCELERATION

(UNBIASED, 10kg to 20kg)

This is an accelerated test designed to indicate types or modes of structural and mechanical weaknesses not necessarily detectable in Mechanical Shock and Variable Frequency Vibration stressing.

13) RELATIVE STRESS COMPARISONS

Many stresses are run at SEC on many different devices. Through both theoretical and actual results, it was clearly determined which stresses were most effective. Also established were the stresses which weren't fully effective.

Comparisons have been made on the basis of defects able to be determined, efficiency in detection, and cost. For the reader's benefit, SEC provides the results of its conclusions on the following pages.

3. CUSTOMER SUPPORT SYSTEM

3.1 INTRODUCTION

Manufacturing companies have developed customer support systems for the purpose of uniting communications. Through these communications pass the information and knowledge required to satisfy the customers needs in areas such as quality and reliability, customer claims, customer training, field service technical issues, pricing or availability and above all, trust. Open lines of communication establishes thorough trust between the customer and vendor and are essential for such programs as dock-to-stock in order to achieve the ultimate in customer/vendor relations. SEC, in its commitment to customer satisfaction, has installed within its organization a support system that is designed to produce the open lines of communication between all facets of relations for both the customer and SEC.

3.2 POLICY

SEC has developed within its organization, a customer support system. SEC's policy requires that this system be manned with the proper personnel that are thoroughly trained in the areas that each represent and are dedicated to opening and maintaining lines of communication with the customer. Technical data used by SEC to support the customer must be up to date and always available for use by the customer (privileged or confidential information maybe excluded). Customer training is provided to the customer by only the most knowledgeable SEC personnel. SEC will provide customer field service in the form of periodic goodwill visits to customer sites or specialized problem solving services as required. Process change notification procedures as well as safety standards are also strictly adhered to.

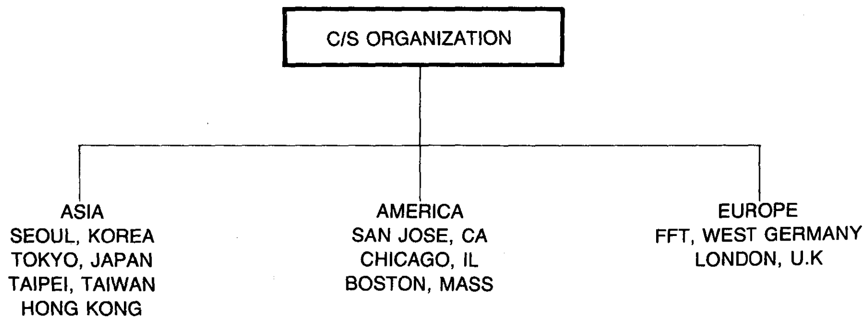
3.3 CUSTOMER SUPPORT SYSTEM

1) QUALITY ASSURANCE SERVICE

SEC has felt the need to reorganize its current Quality Assurance Sections in order to better service our customers. From this new organizational change, a new QA section was born. This new QA section, known as QA Section 3, was developed specifically for the customer. The customer service team in QA3, was organized to respond prombtly to customers quality requirements. The purpose of this team is to form a more responsive communication channel between plant R & D, the sales department and the customer. Customers will achieve satisfaction with our company's products by use of the newly organized customer service system. This service system is openly available to customers for comments concerning problems or opinions about SEC's devices. An 800 number is published on the inside of the handbooks cover.

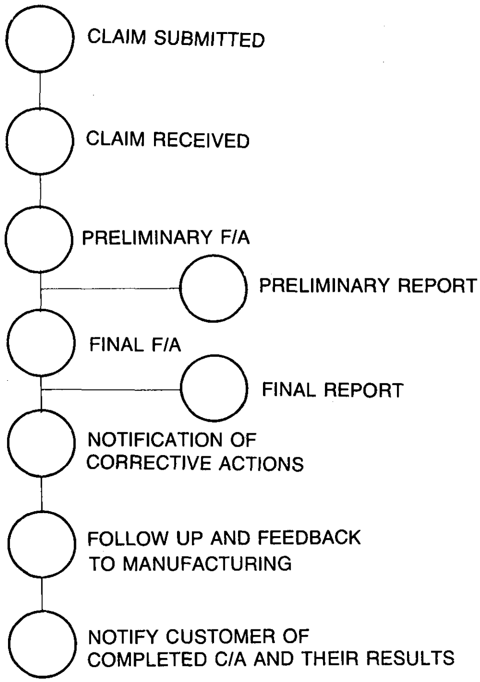
2) CUSTOMER SERVICE TEAM

The following organizational chart illustrates the world-wide base that the customer service team of SEC has established. Maintaining continuity between all of SEC's worldwide customer service teams is accomplished through the use of a newly installed computer network which allows constant communication between all teams.



3) CUSTOMER CLAIM SUPPORT SYSTEM

Information from the field concerning quality is an essential factor for the improvement of product quality. Equally important, is the investigation of field failures. Timely feedback of the results from the analysis is required to better service customers properly. This data also serves as a direct guide to the improvement of reliability and quality for both SEC and our customers.
The flowchart below demonstrates the process in which SEC currently follows for customer claims.



4) CUSTOMER TRAINING SYSTEM

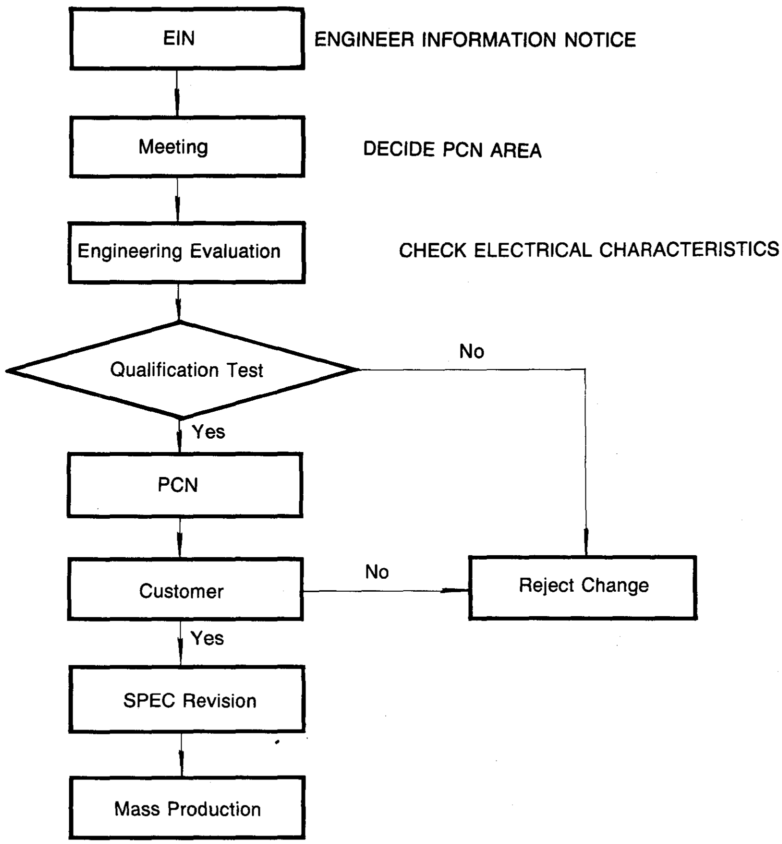
SEC has recently established a training team for the purpose of teaching SEC's customers the methods currently used by SEC to insure the product quality and reliability at the customers site. SEC offers this training in the form of group seminars or presentations and when requested or deemed necessary, individualized training is offered. In some cases, the training will take place at the customers site at the customers convenience while in other cases, SEC will extend on invitation to the customer to visit our manufacturing site.

5) CUSTOMER FIELD SERVICE

SEC has developed field service teams that are devoted to making customer contact when there aren't any problems. In other words, SEC is interested in making periodic goodwill visits. The visiting team would be comprised of those managers and engineers that are involved with the product types that the customer currently uses. The main goal of this team is to establish customer trust through communication.

3.4 PROCESS CHANGE NOTIFICATION SYSTEM (PCN)

Changes in a process are sometimes required to produce a higher quality product at a lower price. These changes can include new or different types of material, new or modified designs and new or different processes. SEC has developed a PCN procedure that is followed whenever a major or critical change is to be considered for any process. The idea behind the PCN is to allow change to a process by submitting the planned change for qualification by SEC engineering and then presenting the PCN to the customer for final approval. By following this procedure, the customer is assured that no major or critical change will occur to the process without the customers consent.



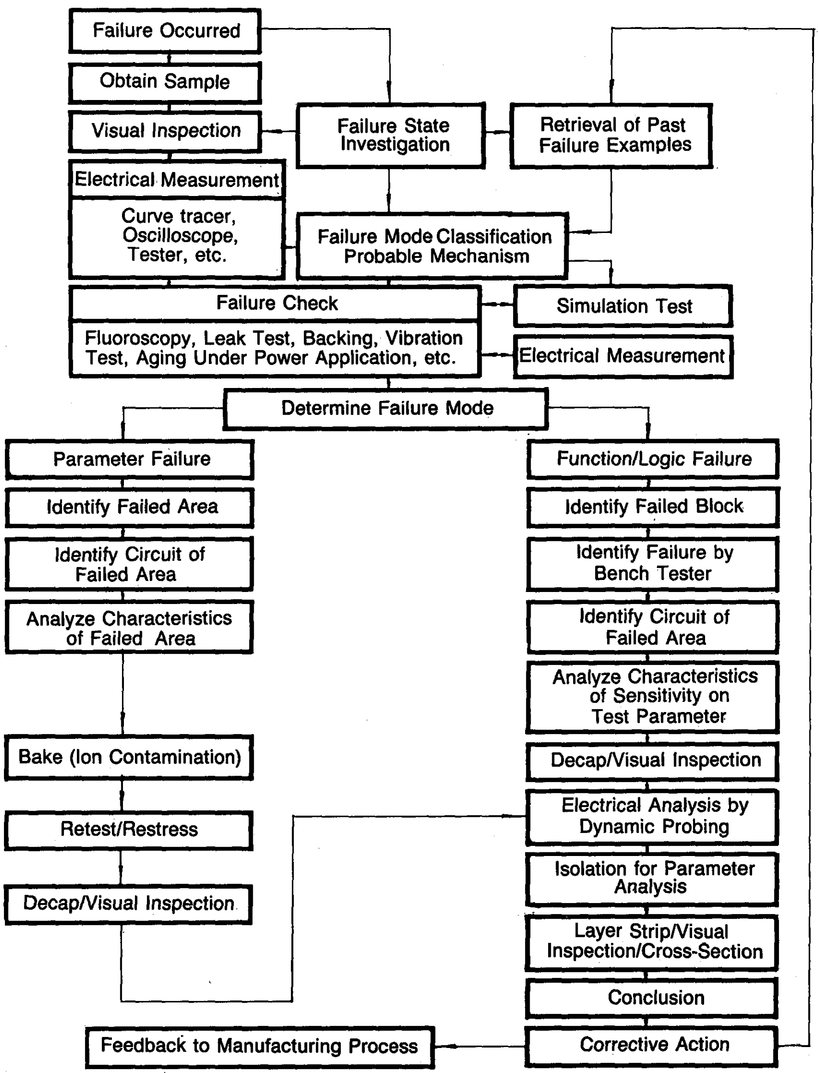
3.5 SAFETY STANDARDS

Most customers express the desire to use only products which have been manufactured with materials that meet the safety specifications of the Underwriters Laboratories. SEC has chosen to adhere to the specifications called out in the UL standard 94 by purchasing and using only those plastic materials that conform to this standard. UL 94 tests for a number of different flammability conditions that effect the plastic material used in semiconductor devices including horizontal burning, vertical burning and flame spread.

4. FAILURE ANALYSIS

4.1 PROCEDURE

A general failure analysis procedure is shown below. The method demonstrated in the flow chart applies to all rejects. However, each analysis is specific unto itself, so that a completely exhaustive analytical flow is impossible for the limits of this manual. Specific instances and examples of interest are provided later in the chapter. Also included in this section is a typical day-by-day accounting of a failure analysis in progress. A two-week turnaround is the objective, with greater than 90% of analysis lasting equal to or less than this duration. A sample analysis plan and report are attached at the conclusion of this section.



Failure Analysis Procedure Flow Chart

Applicable Comments for the above flow chart are made below.

1) DETERMINATION OF FAILURE MODE

The basic failure mode shall be determined with data from computer and bench testing. As a defect can represent various electrical failure modes, it is critical to determine the most basic failure mode. (For example, a V_{OL}/V_{OH} parameter failure may be also analyzed as a functional failure. However, it is very important to determine V_{OL}/V_{OH} as the basic failure mode.)

2) IDENTIFICATION AND ANALYSIS OF FAILED CIRCUIT AREA

Correlation shall be derived with general (macroscopic) failure phenomenon through circuit interpretation of the failed area.

3) SENSITIVITY OF TEST

Parametric value of failed sample shall be determined through adjusting DC and AC parameters, temperature range, etc.

4) ION CONTAMINATION

For a sample assumed to have an inversion phenomenon caused by ionic contamination, characteristics shall be identified by conducting a Ta = 150°C, 24 hour cure and repeating test/restress.
Contamination of a specific layer shall be determined by stripping each layer.

5) DECAPSULATION

There are 5 decap methods with respective merits and demerits. The appropriate method must be utilized on the basis of the characteristics and potential cause for each failure.

6) ISOLATION AND DYNAMIC PROBING

It is essential to isolate the probable failing part of the circuit for its electrical failure mode. Without isolation, exact detection of a failed part can not be accurately accomplished as an electrical failure mode has an influence on other parts of the circuit.

7) LAYER STRIPPING

Each layer strip should meet specification requirements with respect to time. It should never be the case that chemical attack is mistaken for causing the failure of a part.

8) GENERATION OF ACTIVATION ENERGY

Accelerated life testing requires generation of actual activation energies based upon establishing a definitive failure mode. This generation has a great effect in determining the acceleration factor of Arrehenius' model.

9) CORRECTIVE ACTION

Failure analysis is fully completed only by establishing a future plan and corrective action, which are taken to resolve a problem and prevent its recurrence.

4.2 Failure Modes and Mechanisms

1) Failure mechanisms for devices vary widely. They are caused by both front-end (wafer) and back-end (assembly) processing. To classify problems and their instigations, the table listed below is provided.

Items and Causes of Failure Modes

Item	Type of Failure	Failure Mode	Cause
Wire Bonding	Wire Disconnection	Open	Incomplete Manufacture or Misuse
	Wire Short	Short	
	Purple Plague	Open, High Resistance	
	Bond Detaching	Open, High Resistance	
	Misplaced Bonding, Loose Contact	Open, High Resistance Short	Incomplete Manufacture
	Improper Bond Shape Erroneous Bonding	Open, High Resistance Open, High Resistance	
Junction Region	Destruction by Surge	Low Breakdown Voltage, Short, Open	Incomplete Manufacture or Misuse
	Hot Spot		
Case	Lead Disconnection	Open, High Resistance	Same as above
	Lead Short	Short, High Leakage	
Seal	Incomplete Seal	Breakdown Voltage Deterioration, High Leakage	Same as above
	Enclosed High Humidity Gas		
	Contamination of Surface		
	Dust and Dirt	Short, Low Breakdown Voltage Large Leakage	
Metallization	High Current Density	Open, Short	Misuse
	Electromigration	Open, High Resistance	
	Scratch	Open, Short	Incomplete Manufacture
	Insufficient Thickness Excessive Etching	Open, High Resistance	
	Contamination, Dust and Dirt	Open, High Resistance	Incomplete Manufacture or Misuse
	Poor Wiring and Element Connection		
Chip Mounting	Chip Crack	Open, Short	Same as above
	Chip Detaching	Open, Short, High Thermal Resistance	
Oxidized Film	Pinhole, Crack	Low Breakdown Voltage, Short	Incomplete Manufacture
	Insufficiently Oxidized Film Thickness	Low Breakdown Voltage	
Surface Treatment	Channel Formation	Low Breakdown Voltage High Leakage	Same as above
	Contamination		
Mask	Insufficient Photoresist	Low Breakdown Voltage Short, Open, High Leakage	Same as above
	Mask Misalignment		
Material and Diffusion	Improper Impurity Density	Same as above	Same as above

2) Standard product reliability tests can naturally generate failures. Here, in this section, a table is given which lists tests and their associated rejects. Each test has a specific purpose, and if there exists a particular product weakness, a given test will expose it. In this manner, by knowing a test and it's function, a clear determination can be made as to the relevance of a failure for that particular test.

Reliability Tests and Associated Failure Modes

	Failure Cause	Diffusion	Oxide	Metalization	Wire Bonding	Package Environment	Package Seal	Lead Fatigue	Solderability	Mark	Die bonding
Item	Test Condition	•Contamination •Crystal Defect •Photoresist Reject	•Contamination •Pin Hole •Crack •Thickness Unstable	•Conpos. •Scratch •Void •Open	•Interface •Corrosion •Misbonding •Wire Open •Chemical Interface	•Conductive ions •Inadequate •Environments	•Sealing Reject	•Conpos.	•Marking	•Themal Reject	Resistance Reject •Crack •Chip Position Reject
T/C	−65°C→150°C 200 Cycles		0	0	0		0				0
T/S	−65°C→125°C 200 Cycles		0	0	0		0				0
Moisture Resistance	90-98%R.H./65°C3HRS 80-98%R.H./25°C8HRS 90-98%R.H./65°C3HRS 10 Cycles		0	0	0	0	0				
Vibration Fatigue	20G-3 Axis Orientation f=20 to 2000 cpe for 4 min. 4 cycles				0	0					0
Constant Acceleration	Pulse Duration: 0.1-1m sec Shock pulse: 0.5-3Kg				0						0
Mechanical Shock	1500g, 0.5ns Each Direction of X, Y and Z Axis				0						0
Lead Integrity	W=227g 90°C 3 times						0				
Marking	Isoprophylalcohol									0	
Solderability	Ta=230° 5 Sec. Once With Flux								0		
Salt Spray	Ta=35°C, 5% NaCl				0				0		
OPL	Individual Spec	0	0	0	0	0					0
IOPL	Individual Spec	0	0	0	0	0					0
HTRB	Individual Spec	0	0	0	0	0					0
HTS	Individual Spec		0		0	0			0		
WHTS	80°C, 90% RH 85°C, 85% RH		0	0			0	0	0		
WHTRB	85°C, 85% RH Bias	0	0	0	0	0	0	0	0		0

3) An anomalous manufacturing step can manifest itself in many ways with respect to product reliability. The chart below depicts process steps, the types of rejects they can generate, and the way to defect such failures. Of course, there are numerous QC and Production checks along all stages of the manufacturing process. However, a semiconductor product typically involves so many operations it's nearly impossible to detect all potential reliability hazards. Thus, there are final electrical and visual tests, reliability tests, and statistical analyses which are run prior to product releasal. The chart below speaks to the electrical, visual, and reliability tests.

Failure Mechanisms of Integrated Circuits

Process Step Affecting Reliability	Failure Mechanism	Failure Mode	Failure Detection Method
Wafer Fabrication	Dislocation and Stacking Fault	Degradation of Function Characteristics	Electrical Test Operation Life
	Non-Uniform Resistivity	Unpredictable Characteristic Values	Electrical Test
	Surface Abnormalities	Improper Electrical Characteristics, Short and Open	Electrical Test Operation Test
	Cracks, Chips, Scratches (Usually Caused During Handling)	Open and Short	Electrical Test Visual Inspection (Before Seal) Temperature Cycling
	Contamination	Degradation of Junction Characteristics	Visual Inspection (Before Seal), Temperature Cycling, High Temperature Storage, Reverse Bias
Passivation	Cracks and Pin Holes	Shorts, Low Breakdown Voltage	Temperature Cycling High Temperature Storage High-Voltage Test, Operation Life Visual Inspection (Before Seal)
	Non-Uniformity of Film Thickness	Low Breakdown Voltage Increase of Leakage Current in Oxide Film	Same as Above
Mask	Scratch, Crack, Scar of Photo Mask	Open, Short	Visual Inspection (Before Seal), Electrical Test
	Misalignment	Open, Short	Same as Above
	Abnormality of Photo-Resist Pattern (Line-Width, Space, Pin Hole)	Degradation of Characteristics Due to Parameter Drift Open, Short	Same as Above
Etching	Improper Elimination of Oxide Film	Open, Short, Intermittent Failure	Visual Inspection (Before Seal) Electrical Test Operation Life
	Under-Cut	Short or Open in Metallization	Visual Inspection (Before Seal) Electrical Test

Failure Mechanisms of Integrated Circuits (Continued)

Process Step Affecting Reliability	Failure Mechanism	Failure Mode	Failure Detection Method
Etching	Spotting (Smear) Inhomogeneous Etching	Latent Short	Visual Inspection (Before Seal) Temperature Cycle, High Temperature Storage Operation Life
	Contamination (Photo Resist, Residue of Chemical Substance)	Low Breakdown Voltage Increase of Leak Current	Same as Above Reverse Bias
Diffusion	Improper Control of Doping Profile	Performance Degradation Caused by Instability and Fault	High Temperature Storage Temperature Cycling Operation Life Electrical Test
Metallization	Scratched and Smeared Metallization (Caused During Handling)	Open and Short	Visual Inspection (Before Seal) Temperature Cycling Operation Life
	Thin Metallization Due to Insufficient Deposition or Oxide Film Step	Open or High Impedance Internal Connection	Electrical Test Operation Life Temperature Cycle
	Oxid Film Contamination Material Incompatibility	Open Metallization Caused by Poor Adhesion	High Temperature Storage Temperature Cycling Operation Life Test
	Corrosion (Residue of Chemical Substance)	Open Metallization	Visual Inspection (Before Seal), High Temperature Storage Temperature Cycle, Operation Life
	Displacement Contaminated Contact	High Contact Resistance, Open	Visual Inspection (Before Seal), Electrical Test, High Temperature Storage Temperature Cycle, Operation Life
	Improper Temperature and Period for Metallization	Peeled Metallization Poor Adhesion Short	Electrical Test High Temperature Storage Temperature Cycle Operation Life
Die Separation	Cracks and Chips Caused by Improper Dicing	Open	Visual Inspection (Before Seal) Temperature Cycling Thermal Shock Vibration Shock

Failure Mechanisms of Integrated Circuits (Continued)

Process Step Affecting Reliability	Failure Mechanism	Failure Mode	Failure Detection Method
Die Bonding	Void Between Header and Die	Degradation Due to Overheating	Radiography, Operation Life Constant Acceleration Shock, Vibration
	Over-Spreading of Eutectic Solder	Short, Intermittent Short	Visual Inspection (Before Seal), Radiography, Vibration Shock
	Poor Bonding of Die to Header	Die Crack and Lifting	Visual Inspection (Before Sealing), Constant Acceleration, Shock, Vibration
	Mismatching of Materials	Crack or Peeling of Die	Temperature Cycling High Temperature Storage Constant Acceleration
Wire Bonding	Poor Bonding Strength	Open Wire, Open, Lifting Vibration Shock	Constant Acceleration
	Mismatched Material and Contaminated Bonding Pad	Lead Bond Peeling	Temperature Cycling High Temperature Storage Constant Acceleration Shock, Vibration
	Formation of Intermetallic Plague	Open Bonding	High temperature storage, Temperature Cycling. Constant Acceleration Shock, Vibration
	Insufficient Bonding Area or Spacing	Open Bonding Short	Operation Life Test, Constant Acceleration, Shock Vibration, Visual Inspection (Before Seal)
	Improper Bonding Arrangement	Open, Short	Visual Inspection (Before Seal) Electrical Test
	Die Cracks or Chips	Open, Shock	Visual Inspection (Before Seal) High Temperature Storage Temperature Cycling Constant Acceleration, Shock Vibration
	Excessive Loop or Sag in Wire	Short to the Case, Substrate or other Parts of the Leads	Visual Inspection (Before Seal), Radiography, Constant Acceleration, Vibration
	Crack, Scratch, or Scar on Lead	Wire Disconnection Causing Open, Short	Visual Inspection (Before Seal), Constant Acceleration, Shock Vibration

Failure Mechanisms of Integrated Circuits (Continued)

Process Step Affecting Reliability	Failure Mechanism	Failure Mode	Failure Detection Method
	Insufficent Elimination of Tail Wire	Short, Intermittent Short	Same as Above Radiography
Sealing	Incomplete Hermetic Seal	Performance Degradation, Shorts and Opens Caused by Chemical Corrosion and Moisture	Fine Leak, Gross Leak
	Bad Atmosphere in Package	Performance Degradation Due to Inversion Layer Channeling	Operation Life Reverse Bias, High Temp. Storage, Temperature Cycling
	Bending or Breaking of the External Lead	Open	Visual Inspection, Lead Fatique
	Crack or Void in Seal Glass	Short or Open in Metallization Due to Leak	Seal, Electrical Test High Temperature Storage Temperature Cycling High Voltage Test
	Migration on Seal between Outer Lead and Metal Case	Intermittent Short	Low Voltage Test
	Electro-Conducting Particles Floating in Package	Same as Above	Constant Acceleration, Vibration Radiography
	Mismarking	Inoperable	Electrical Test

4) Equipment

A listing of important equipment used for failure analysis is shown below in tabular from, SEC's committment to comprehensive analysis of all relevant rejects necessarily implies a usefulness for key analytical instruments. Constant efforts are made to both use and modify equipment to meet specialized investigations. However, only standard equipment, not a listing of hybrids (for confidential development purposes), is listed below.

Equipment for failure analysis

Category	Item	Application
Visual	1. Stereo Microscope	Use for visual inspection
	2. SEM (Scanning Electron Microscope)	Use to inspect the surface or cross-section of a device at high magnification. Through voltage contrast techniques, it is possible to analyze voltage levels while the device is operating
	3. Infrared Microscope	Using the infrared radiation emitted by a functioning device, a thermal map can be produced.
	4. X-Ray	Use to inspect the bonding wire of encapsulated devices.
	5. Metallugical Microscope	Inspect interconnects, contacts, bonds
	6. Radiographic Scope	Inspect bond wires, die attach

Equipment for failure analysis (Continued)

Category	Item	Application
Elemental Analysis	1. Auger Electron Spectrometer (AES)	Used to detect and analyze contamination on the surface of a die
	2. EDX Spectrometer	Used with SEM to analyze elements present in a device. This is done by measuring the energy distribution of X-rays produced by the interaction of primary electrons and the sample.
	3. Differential Interference Microscope	Used for elemental analysis
	4. Electron Probe Micro Analyzer (EPMA)	Used for current analysis
	5. Ion Micro Mass Analyzer (IMMA)	Spectral analysis of chemical constituents
	6. Surface Eveness Micrometer	Measures planarity
	7. Differential Scanning Calorimeter (DSC)	Permits the analysis of glasses and polymers-especially encapsulation resins-through the measurement of reaction heat
	8. Thermo Gravimetric Analyser	Used to determine the thermal stability of polymers and glasses by measuring variations in mass with temperature.
	9. Plasma Etcher	Used to open devices encapsulated in epoxy resins, to remove silicon nitride, and to remove thin oxide films
	10. Transmission Electron Microscope (TEM)	Used for elemental analysis and high resolution surface on spectron
	11. Surface Tunneling Microscope (STM)	Used for elemental analysis
	12. Electron Spectrometry for Chemical Analysis (ESCA)	Used for elemental analysis
	13. Secondary Ion Mass Spectroscope	Used for elemental analysis
Decapsulation System	1. Grinding Machines 2. Angle Lapping 3. Evaporation 4. Diamond Cutter (Cross Section Cutter) 5. Molding System 6. Jet-Etching System 7. Etching Solution 8. Hot Plates 9. Ventilation Hoods	Used to decapsulate devices, to cut the cross section of die, to remove a surface layer.

Equipment for failure analysis (Continued)

Category	Item	Application
Electrical Test	1. Curve Tracer 2. TR, IC, MOS Tester 3. ESD Simulator 4. LCR Meter 5. DC-Analyzer 6. Noise Tester 7. Logic State Analyzer 8. Manipulator Probe Ssytem 9. Electron Beam Tester 10. Hot Electron Analyzer 11. I.R Scope	Used to measure electrical characteristic of devices, to establish the cause of failure.
Stress Test	1. Temperature Probe System 2. Constant Temperature Oven 3. Ovenn for Oper Life Test 4. Humidity Oven 5. Vibration System	Used to stress or cure the failed devices to identify a failure mechanism. This is a very important tool for analyzing degradation phenomena and intermittent failures.

Methods and Equipment for Failure Analysis

Item	Contents of Inspection	Equipment for Analysis
External Visual Check	• Condition of Lead, Plating, Soldering, Welding Area • Mark, Date Code • Package damage • Solderability • Sealing	Stereo-Optical-Scope x 40 Optical Microscope x 100 Helium Leak Detector Gross Leak Detector (Using Fluorocarbon)
Electrical Test	• DC Parameter, AC Parameter Test • Function Test • Margin Test of Voltage and Temp. • Diode Characteristics between Each Pin • Disconnection, Short Circuit and / or Electrical Characteristic detected by the above Inspection	IC Tester Curve Tracer (HP4145) Oscilloscope DC Power Supply Oscillator (Sine Wave Pulse) Heat-Gun, Cooling Gas Spray Thermo-Spot
Radiography	• Internal Structure of Device is Checked Non-Destructively	Soft X-Ray
Decapping	• Internal Structure is observed after decapping	Metal Cutting Scissors, Nippers Cap opener, plastic etcher, Hot plate, Drill, HNO_3
Internal Visual Check	• Detection of Defective Spot on the Chip Surface • Detection of Discrepancy of Internal Connection (Metallization, Wire Bond -ing, Etc.) • Electrical Characteristics are Checked by Mechanical Prober • Detection of Hot Spot • Existence of Foreign Material	Optical Microscope Micro-Prober SEM Laser Cutter Infrared Micro Scanner Thermal Plotter Infrared Microscope
Internal Structure Analysis	• Cross Sectional Analysis of Chips to Observe Diffusion Layer of Oxide Film • Analysis of Metallic Elements • Removing of Over-Coating Glass and Aluminum Metallization	Optical Microscope SEM, MAX, AES, SAM, IMA Spectrometer Micro-Prober
Simulation Test	• Operational Test on Actual Equipment	Actual Electronic Equipment

4.3 FAILURE MODE EFFECT ANALYSIS (FMEA)

Failure Mode Effect Analysis is a method used for checking if measures are taken against every possible failure in the design, the manufacturing process, the operating method, etc. For this analysis, factors such as design, manufacturing process, packaging, and operating method are divided into small units, and its functions are clearly defined. All possible failure modes are listed for each item, its effect on the product and the cause of each failure is examined. Each item is then evaluated to clarify the corrective actionto be taken.
Table shows an example of FMEA in the manufacturing process of plastic encapsulated MOS LSI. The incident column pertaining to the Evaluation Points show the failure rate; Effectiveness column shows the impact of the effect by the failure of the product, device, or system; and Detectability shows the rate of detection of the failure. These are individually graded on the basis of ten points. The result is then evaluated by multiplying the points. The larger value indicates the importance of the item. A counterplan for each item is then specified and action taken.

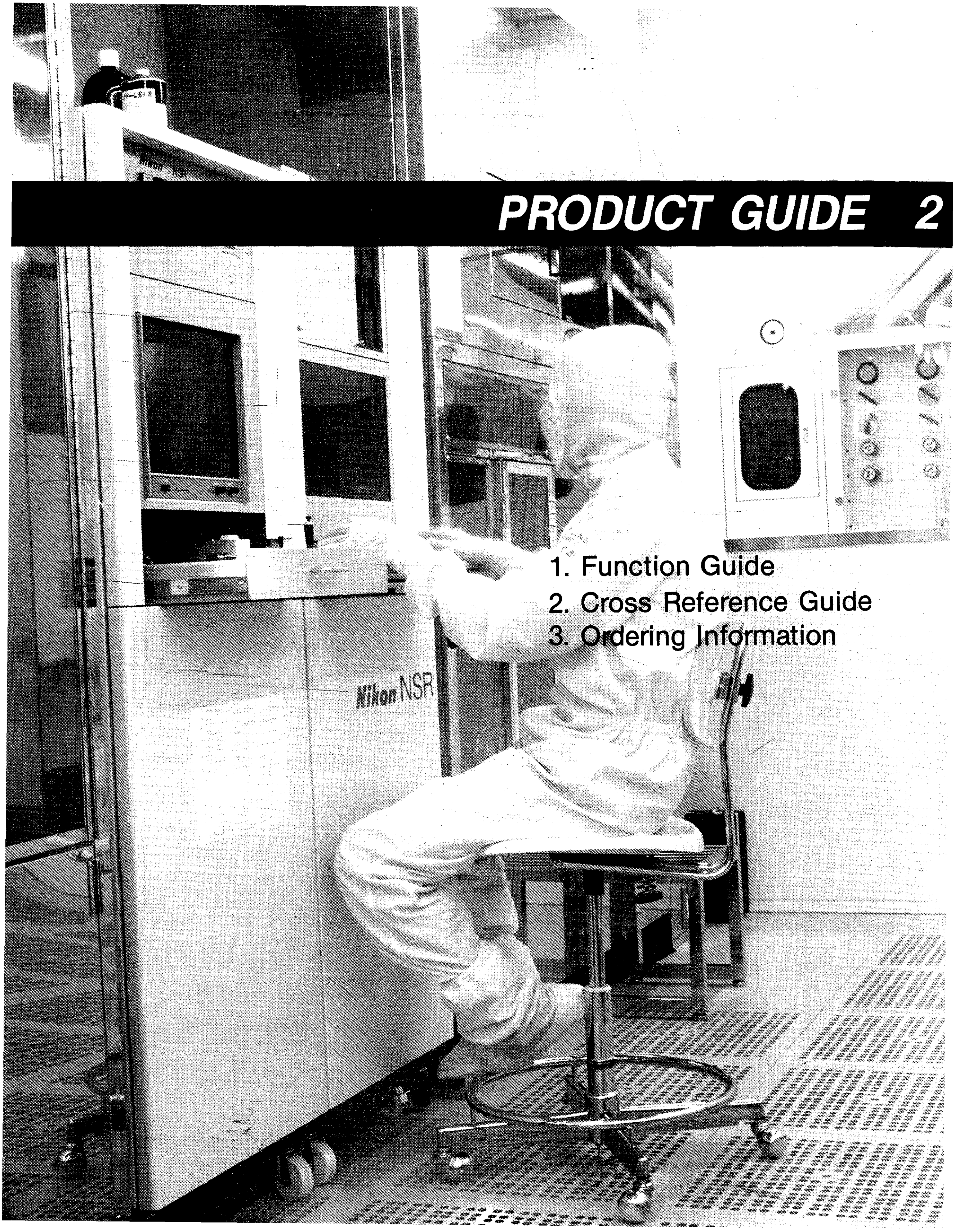
Manufacturing Process FMEA Example (Plastic Encapsulated Products)

Process Name (Process Function)	Failure Mode	Failure Effect	Failure Cause	Counterplan
Al metallization	Improper thickness Lack of Al wiring Breakage defect	Electromigration open circuit	Operator's mis-handling, dirt/foreign matter attachment, poor adjustment of equipment	Improvement and adjustment of written working process, dust control of clean room, SEM test in the process
Glassivation	Lack of glassivation film, failure film thickness	Increased leak current, improper operation	Dirt/foreign matter attachment, operator's mishandling	Dust control of clean room, improvement and adjustment of written working process
Visual Inspection	Scratch, die crack, dirt, spot, residual resist	Open circuit, increased junction leak current	Mishandling of wafer, Misclearning of water	Improvement and adjustment of written working process
Assembly Process Die Selection	Die crack	Increased junction leak current, improper operation	Poor adjustment of equipment, operator's mishandling	Corrective action to device control operator, improvement and adjustment of written working process
Die Bonding	Die crack Die floating	Open circuit, increased junction leak current, improper operation	Operator's mishandling temperature too low	Corrective action to device control operator, improvement and adjustment of written working process, visual inspection
Wire Bonding	Open bonding, improper bonding position, shorted bonding wire	Open circuit, short circuit	Poor bonding strength, operator's mishandling, poor adjustment of equipment, looped bonding wire, shape defact	Improvement and adjustment of written working process, corrective action to device control operator, visual inspection

Manufacturing Process FMEA Example (Plastic Encapsulated Products) (Continued)

Process Name (Process Function)	Failure Mode	Failure Effect	Failure Cause	Counterplan
Sealing (Resin)	Open bonding wire, shorted bonding wire, package crack, corrosion	Open circuit, short circuit, defective appearance	Poor adjustment of equipment, insufficient cure	Ditto
Lead Surface Treatment (plating)	Poor metal-plating thickness, dirt	Poor soldering, poor contact	Operator's mishandling poor adjustment of equipment, insufficient cleaning	Adjustment of written working process, corrective action to control operator
Lead Formation	Abnormal shape, broken lead	Failure inserting in the printed substrate poor operation	Operator's mishandling poor adjustment of equipment	Ditto
Marking	Marking error illegible marking	Operating destruction	Operator's mishandling insufficient cure	Improvement and adjustment of written working process

PRODUCT GUIDE 2



1. FUNCTION GUIDE

1.1 Audio Application

A. FM Front End

Type	Package	Function			Use			Remark
		RF	OSC	MIXER	R/C	Car	Hi-Fi	
KA2249/D	7 SIP/8 SOP	*	*	*	*			$V_{CC}=2\sim7V$
KA22495	9 SIP/14 SOP	*	*	*	*		*	$V_{CC}=1.6\sim6V$
KA22496	9 SIP	*	*	*	*		*	$V_{CC}=1.6\sim6V$

B. FM/AM RF, IF and Detector System, AM Tuner System

Type	Package	Function						Use			Remark
		AM RF CONV	AM IF AMP	AM DET	FM IF AMP	FM DET	S/M	R/C	Car	Hi-Fi	
KA22461	19 ZSIP	*	*	*					*		$V_{CC}=8\sim15V$
KA2243	16 DIP		*	*	*	*	*	*		*	$V_{CC}=3\sim14V$
KA2244	9 SIP				*	*	*		*		$V_{CC}=8\sim16V$
KA22441	16 ZSIP				*	*	*		*		$V_{CC}=6\sim14V$
KA2245	7 SIP				*	*			*		$V_{CC}=8\sim15V$
KA2247	16 DIP	*	*	*	*	*	*	*			$V_{CC}=3\sim8V$
KA22471	16 DIP	*	*	*	*	*	*	*			$V_{CC}=3\sim8V$
KA2248A/D	16 DIP/16 SOP	*	*	*	*	*	*	*			$V_{CC}=1.8\sim6V$

C. FM Stereo Multiplex Decoder

Type	Package	PLL	Lamp Driver	VCO Stop	Sep. Cont.	Use			Remark
						R/C	Car	Hi-Fi	
KA2261	16 DIP	*	*	*	*	*	*		Sep = 45dB
KA2262	16 ZSIP	*	*	*	*		*		SNC/HCC
KA2263	9 SIP	*	*	*		*	*		Sep = 45dB
KA2264/D	9 SIP/16 SOP	*	*	*		*			$V_{CC}=1.8\sim5V$
KA2265	16 DIP	*	*	*	*			*	VCO Non-Adjusting MPX
KA2266	16 ZSIP	*	*	*	*		*		Pilot Canceller SNC/HCC

† New Product
†† Under Development

D. Audio Power Amplifier

Type	Package	V_{CC} (V)	Output Power $R_L = 4$ ohm	Output Power $R_L = 8$ ohm	Use R/C	Use Car	Use Hi-Fi	Remark
KA2201/N/B	8 DIP	6		0.5W	*			$V_{CC} = 3 \sim 14V$
		9		1.2W				
KA2206	12 DIP/F	9	2.3W × 2		*			$V_{CC} = 4.5 \sim 11V$
KA22062S	12 SIP H/S	12	4.5W × 2		*			$V_{CC} = 6 \sim 15V$
KA22063S	12 SIP H/S	12	4.5W × 2		*			$V_{CC} = 6 \sim 15V$
††KA22065	12 SIP H/S	12	4.6W × 2		*			$V_{CC} = 6 \sim 15V$
KA2214	14 DIP H/S	9		1.2W × 2	*			$V_{CC} = 3 \sim 13V$
KA2209	8 DIP	3	110mW × 2		*			$V_{CC} = 1.8 \sim 9V$
KA2210	12 SIP H/S	13.2	5.5W × 2			*		$V_{CC} = 10 \sim 16V$
KA22101	12 ZSIP H/S	13.2	23W			*		$V_{CC} = 9 \sim 18V$
†KA22102	17 ZSIP H/S	13.2	15W × 2			*		$V_{CC} = 9 \sim 18V$
†KA22103	17 ZSIP H/S	13.2	19W × 2			*		$V_{CC} = 9 \sim 18V$
KA2211	12 SIP H/S	13.2	5.8W × 2			*		$V_{CC} = 10 \sim 18V$
KA2212	9 SIP	6		0.5W	*			$V_{CC} = 3.5 \sim 12V$
LM386/S/D	8 DIP/9 SIP/8 SOP	6		0.325W	*			$V_{CC} = 4 \sim 12V$
KA2213	14 DIP H/S	6	1W		*			Included Pre-Amp with ALC
†KA22130	16 DIP	6	1W		*			Included Pre-Amp with ALC
KA22131	24 SOP	3	69mW × 2($R_L = 16\Omega$)		*			$V_{CC} = 1.8 \sim 3.6V$ Included Auto Reverse Pre-AMP
KA22134	16 DIP	3	27mW × 2($R_L = 32\Omega$)		*			$V_{CC} = 1.8 \sim 6V$ Dual PRE + POWER AMP with Volume Control
KA22135	22 SDIP	3	28mW × 2($R_L = 32\Omega$)		*			$V_{CC} = 2 \sim 7.5V$ Dual PRE-POWER AMP and DC Motor Speed Controller
†KA22136	28 SOP	3	28mW × 2 ($R_L = 32\Omega$)		*			$V_{CC} = 2 \sim 5V$ Dual PRE-POWER AMP with Volume Control and DC Motor Speed Controller
KA8602	8 DIP/8 SOP	6	300mW ($R_L = 32\Omega$)		*			$V_{CC} = 2 \sim 16V$ $R_L = 8\Omega \sim 100\Omega$

† New Product
†† Under Development

E. Pre-Amplifier

Type	Package	Function	Use			Remark
			R/C	Car	Hi-Fi	
KA1222	8 SIP	Dual Pre-amplifier	*			$V_{CC}=2.5\sim6V$
KA2220	9 SIP	Pre-amplifier with ALC	*		*	$V_{CC}=3.5\sim14V$
KA2221	8 SIP	Dual Pre-amplifier	*	*	*	Included Voltage Regulator
KA22211	8 SIP	Dual Pre-amplifier	*	*	*	$V_{CC}=5\sim14V$
KA2223	16 DIP	5 Band Mono Graphic EQ AMP	*	*	*	$V_{CC}=5\sim13V$
KA22231	28 SOP	5 Band Dual Graphic EQ AMP	*			$V_{CC}=1.6\sim6V$
KA22232	20 SOP	3 Band Dual Graphic EQ AMP	*			$V_{CC}=1.6\sim6V$
KA22233	22 DIP	3 Band Dual Graphic EQ AMP	*	*	*	$V_{CC}=5\sim15V$
KA22234	24 ZSIP	5 Band Dual Graphic EQ AMP	*	*	*	$V_{CC}=3.5\sim14V$
KA22235	18 ZSIP	5 Band Mono Graphic EQ AMP	*	*	*	$V_{CC}=3.5\sim16V$
KA2224	14 DIP	Dual Pre-amplifier with ALC	*		*	$V_{CC}=4\sim13V$
KA22241	9 SIP	Dual Pre-amplifier with ALC	*			$V_{CC}=4.5\sim14V$
KA22242	10 SIP	Dual Pre-amplifier with ALC	*			$V_{CC}=4\sim12V$
KA2225/D	16 DIP/16 SOP	Dual Pre-amplifier with Mute	*			$V_{CC}=1.6\sim5V$
KA22261	16 DIP	Dual Pre-amplifier with ALC	*		*	Included REC AMP
KA2228	21 ZSIP	Dual Pre-amplifier system	*		*	$V_{CC}=3.5\sim7V$
††KA22291	24 SDIP	Quad Pre-amplifier system	*		*	$V_{CC}=5\sim14V$
KA7226	14 DIP	Dual Pre-amplifier with ALC	*		*	$V_{CC}=3\sim16V$

F. LED Level Meter Driver

Type	Package	Function	Remark
KA2281	16 DIP	5 Dot dual red/yellow/green LED driver	VU scale, input amplifier Reference voltage included
KA2283	16 DIP	5 Dot dual red/yellow/green LED driver	VU scale, input amplifier Reference voltage included
KA2284	9 SIP	5 Dot mono green LED driver	VU scale Reference voltage included
KA2285	9 SIP	5 Dot mono red LED driver	VU scale Reference voltage included
KA2286	9 SIP	5 Dot mono red LED driver	Linear scale Reference voltage included
KA2287	9 SIP	5 Dot mono green LED driver	Linear scale Reference voltage included
KA2288	16 DIP	7 Dot mono LED driver	VU scale Reference voltage included

† New Product
†† Under Development

G. Music Selector

Type	Package	Function	Remark
KA2230	22 DIP	9-Program Random Selector	$V_{CC}=5\sim14V$
KA2231	9 SIP	Audio Level Sensor	$V_{CC}=3.5\sim14V$

H. 1 Chip Radio

Type	Package	Function	Remark
KA22421/D	16 DIP/16 SOP	AM 1 Chip Radio	$V_{CC}=2\sim5V$
††KA22426	28 SOP	AM/FM 1 Chip Radio	$V_{CC}=1.6\sim6V$
KA22427	16 DIP	AM/FM 1 Chip Radio	$V_{CC}=3\sim12V$
†KA22429	16 SOP	FM 1 Chip Radio	$V_{CC}=1.8\sim6V$
††KA2292	24 SDIP	AM/FM TUNER+MPX	$V_{CC}=1.8\sim7V$
††KA2293	24 SDIP	AM/FM TUNER+MPX	$V_{CC}=1.8\sim7V$

I. Noise Reduction

Type	Package	Function	Remark
KA2271	16 DIP	Dolby B Type	$V_{CC}=8\sim16V$
†KA22711	16 DIP	Dolby B Type	$V_{CC}=5\sim16V$
†KA22712	16 DIP	Dolby B Type	$V_{CC}=6.5\sim16V$
KA2272/D	16 ZSIP/16 SOP	FM Noise Canceller	$V_{CC}=8\sim15V$
KA2273	14 DIP	DNR for Car Stereo	$V_{CC}=4.4\sim18V$

J. DC Motor Speed Control

Type	Package	Function	Remark
KA2401	8 DIP	DC Motor Speed Controller	$V_{CC}=4\sim12V$
KA2402	8 DIP	DC Motor Speed Controller	$V_{CC}=1.8\sim8V$
KA2404	TO-92L	DC Motor Speed Controller	$V_{CC}=4\sim12V$
KA2407	TO-126	DC Motor Speed Controller	$V_{CC}=3.5\sim14.4V$

2

1.2 Digital Audio Application

A. CD Player

Type	Package	Function	Remark
KA9256	10 SIP H/S	Dual Amp for CDP Motor Driver	$V_{CC}=15V$, $V_{EE}=-15V$
KA9257	12 SIP H/S	Dual Amp for CDP Motor Driver	$V_{CC}=5V$
KA9255	22 SOP	PWM Motor Driver for CDP	$V_{CC}=3.5\sim12V$
†KS5990	80 FQP	16K SRAM + Digital Signal Processor	$V_{CC}=5V$
†KS5991	80 FQP	Processor	$V_{CC}=3.4V$
††KA9210	80 FQP	16K SRAM + DSP + Digital Out 1	$V_{CC}=5V$
†KA8309	48 QFP	Servo Signal Processor	$V_{CC}=5V$
†KA9201	30 SOP	RF AMP for CDP	$V_{CC}=5V$
††KDA0313	20 SOP	13 Bit D/A Converter	$V_{CC}=5V$
†KDA0316	20 DIP/20 SOP	16 Bit D/A Converter	$V_{CC}=5V$

B. DAT

Type	Package	Function	Remark
††KA9301	44 FQP	Pre Signal Processor	$V_{CC}=5V$
††KA9302	28 FQP	Data Strobe	$V_{CC}=5V$
††KA9310	100 FQP	Digital Signal Processor	$V_{CC}=5V$
††KA9320	80 FQP	Servo Control	$V_{CC}=5V$

C. μ-COM

Type	Package	Function	Remark
††KS55C232	64 FQP	Digital Tuning System (DTS) for Car Stereo	$V_{CC}=5V$, $V_{EE}=-5V$
††KS56C820	80 FQP	System Control for CDP	$V_{CC}=5V$, $V_{EE}=-5V$
††KS56C460	64 SDIP	System Control for CDP	$V_{CC}=5V$, $V_{EE}=-5V$

† New Product
†† Under Development

1.3 Toy Application

Device	Function					Package	V_{CC}(V)	A_V (dB)	Operating Mode	Application
	F/W	B/W	Stop	L/R Turn	Turbo					
KA2303	O	O	O			9 SIP	2.5-10	65	RF	3 Function RC TOY CAR (RX)
KA2304	O	O				9 SIP	2.5-10	65	RF	2 Function RC TOY CAR (RX)
KA2305A	O	O	O			12 SIP	3-18	58	RF + PWM	3 Function RC TOY CAR (RX)
KA2306A	O	O	O		O	14 DIP	3-18	58	RF + FM	3 Function + Turbo (RX)
KA2309	O	O	O	O	O	16 DIP	3-18	58	RF + FM + PWM	7 Function RC TOY CAR (RX)
KA2310	O	O	O	O	O	9 SIP	6-12		RF + FM + PWM	KA2309 Transmitter
KA2311	O	O	O	O	O	16 DIP	3-18	65	RF + FM + PWM	Full Function RC TOY CAR (RX) (L/R Turn on stop state)
KA2312	O	O	O	O	O	9 SIP	6-12		RF + FM + PWM	KA2311 Transmitter
†KA2314	O	O	O	O	O	9 SIP	6-12		RF + FM + PWM	KA2309/11 Transmitter

† New Product
†† Under Development

2. CROSS REFERENCE GUIDE

Application	SAMSUNG	SANYO	TOSHIBA	MATSUSHITA	ROHM	Others
Power Amplifier	KA2201/N	LA4145		AN7116	BA527	*TBA820M
	KA2201B	LA4145		AN7116	BA527	*TBA820M
	KA2212	*LA4140	*TA7313AP	*AN7112	BA526	
	KA22101		*TA7250BP			
	KA8602					MC34119
	LM386		TA7336P		BA546	*LM386/*NJM386
Dual Power Amplifier	KA2206	*LA4182/3	TA7769P	AN7143	BA534	TEA2025
	KA22062		*TA7283AP		BA5406	
	KA22063		*TA7282			
	††KA22065		*TA8207			
	KA2209	LA4530	TA7376P	AN7118		*TDA2822M
	KA2210	*LA4445	TA7227P	AN7147	BA532	
	†KA22102		*TA8205			
	†KA22103		*TA8210			
	KA2211	LA4440	*TA7240AP	AN7178	BA532	
	KA2214					*μPC1263C
EQ AMP + Power	KA2213	*LA4160	TA7628P			μPC1165C
	KA22130	*LA4160	TA7628			
Dual EQ AMP + Power	KA22131	LA4560M			*BA3502F	
	KA22134		*TA8119P			
	KA22135					*LAG637D
	†KA22136					*LAG665
EQ AMP + ALC	KA2220	*LA3210	*TA7137P	AN7320	*BA333	μPC1158H
Dual EQ AMP	KA1222	*LA3160	TA7312P			*M51521L
	KA2221	*LA3161	*TA7375P	AN7310	*BA328	*M5152L
	KA22211	*LA3160	TA7312P			*M51521L
Graphic EQ AMP	KA2223	*LA3600	*TA7796P			*M5226P
	KA22231	LA3610M				TK10586M
	KA22232					TK10580M
	KA22233			AN7330K		
	KA22234				*BA3822L	
	KA22235				*BA3812L	
Dual EQ AMP + ALC	KA2224	*LA3220		AN7312	BA343	
	KA22241	LA3225/6N			*BA3308	M51544L
	KA22242	LA3225/6N			*BA3312N	M51544L
	KA22261		*TA7668BP			
	KA7226		*TA7658P	AN7312	BA343	
	KA2228		*TA7417P		BA3416BL	
Quad EQ AMP	††KA22291		TA8189N			M51166P
Dual EQ AMP + Mute	KA2225	LA3230	*TA7709P/F	AN7315	BA3304	
Music Selector	KA2230	LC7517	TC9167P			*IR3R24
	KA2231	*LA2010	TA7341P	AN6262N/3N	BA335	
AM 1 Chip Radio	KA22421		*TA7641BP			*CIC7641
AM/FM 1 Chip Radio	††KA22426					*CXA1019
	KA22427		*TA7613AT			*TDA1083/*ULN2204
	KA22429		*TDA7021T			
AM/FM IF + DET	KA2243				*BA4220	*HA12413

† New Product †† Under Development * Direct Replacement

Audio ICs (Continued)

Application	SAMSUNG	SANYO	TOSHIBA	MATSUSHITA	ROHM	Others
FM IF+DET	KA2244		*TA7303P	AN278	*BA404	
	KA22441	*LA1140		AN7277	*BA4110	
	KA2245	*LA1150	*TA7130P		*BA403	*μPC1028H
AM Tuner System	KA22461	LA1135	TA7402P	AN7250S		*μPC1215V
AM Tuner+AM/FM IF +DET	KA2247	*LA1260		AN7223	*BA4260	
	KA22471		*TA7640AP	AN7223		
	KA2248A	LA1270	*TA7687AP		BA4228L	
FM Front End	KA2249	LA1180	TA7335P	*AN7213	BA4402	
	KA22495	*LA1185	*TA7358AP	*AN7205		
	KA22496		*TA7358P			
FM Stereo Multiplex Decoder	KA2261	*LA3361	*TA7604P	*AN7410	*BA1330	*HA11227/*μPC1197C
	KA2262	*LA3370	TA7401AP	AN7417	BA1356	
	KA2263		*TA7343AP	*AN7420		
	KA2264	LA3330	*TA7342P	*AN7421	BA1360	
	KA2265	*LA3410	TA7413AP	AN7470		
	KA2266	*LA3375	TA7401AP			
Noise Reduction	KA2271		TA7719P			*CXA1101P
	†KA22711					*CXA1163
	†KA22712					*CXA1102
	KA2272	*LA2110				
	KA2273					*LM1894
μ-COM	††KS55C232					*μPD1719
	††KS56C820					CXP5024
	††KS56C460	LC652001				
LED Lever Meter Driver	KA2281		*TA7666P			IR2E27
	KA2283		*TA7667P			
	KA2284	*LB1403	TA7366P	*AN6884	*BA6124	
	KA2285	*LB1423	TA7366P		*BA6137	
	KA2286	*LB1433			BA656	
	KA2287	*LB1413			*BA6125	
	KA2288					*IR2E02
AM Tuner+MPX	††KA2292		*TA8167			
	††KA2293		*TA8122			
Motor Speed Controller	KA2401					*μPC1470H
	KA2402	*LA5521D				
	KA2404					μPC1470H
	KA2407			*AN6651		μPC1470H
CDP	KA9256		*TA7256			
	†KA9257				*BA6290	
	†KA9255				*BA6280	
	†KA9201					*CXA1081Q
	†KA8309					*CXA1082Q
	†KS5990	LC7860				CXD1167
	†KS5991					CXD1247
	††KA9210					CXD1135+SRAM
	††KDA0313					*CXD1140
	KDA0316	*LC7881				*CXD1161
DAT	††KA9301					*HA12133MP
	††KA9302					*HA12062
	††KA9310					*HD49212
	††KA9320					*HD49011A

† New Product †† Under Development * Direct Replacement

3. ORDERING INFORMATION

KA **0000X** **X** **X**

- X (last) — PACKAGE TYPE (SEE BELOW)
- X — OPERATING TEMP IC'S ONLY
  BLANK: SEE INDIVIDUAL SPEC
  C: 0~70°C
  I : −40~85°C
  M: −55~ +125°C
- 0000X — DEVICE NUMBER AND SUFFIX (OPTIONAL)
  X: IMPROVED VERSION
- KA — DEVICE FAMILY (SEE BELOW)

DEVICE FAMILY

TRANSISTOR / FET

DKS	DALINGTON TR
• IRF	MOS POWER
• IRFA	MOS POWER, TO-126
• IRFP	MOS POWER, TO-3P
• KSA	PNP TR
KSB	PNP TR
KSC	NPN TR
KSD	NPN TR
• MMBT	TR, SOT-23
• MMBTA	TR, SOT-23
• MMBTH	TR, SOT-23
• MPS	TR, SOT-23
• MPSA	TR, TO-92
• MPSH	TR, TO-92
• PN	TR, TO-92
SSH	MOS POWER, TO-3P
SSM	MOS POWER, TO-3
SSP	MOS POWER, TO-220
• TIP	BIPOLAR TR
• 2N	TR

INTEGRATED CIRCUIT

KA	LINEAR IC
KF	J-FET OP AMP
KG	GATE ARRAY
KS	CMOS IC
KT	TELECOM
• LM	NATIONAL
• MC	MOTOROLA
• NE	SIGNETICS
SA	LINEAR ARRAY
SD	H.D AND LINEAR ARRAY
KSV	A/D-D/A CONVERTER
KAD	A/D CONVERTER
KDA	D/A CONVERTER

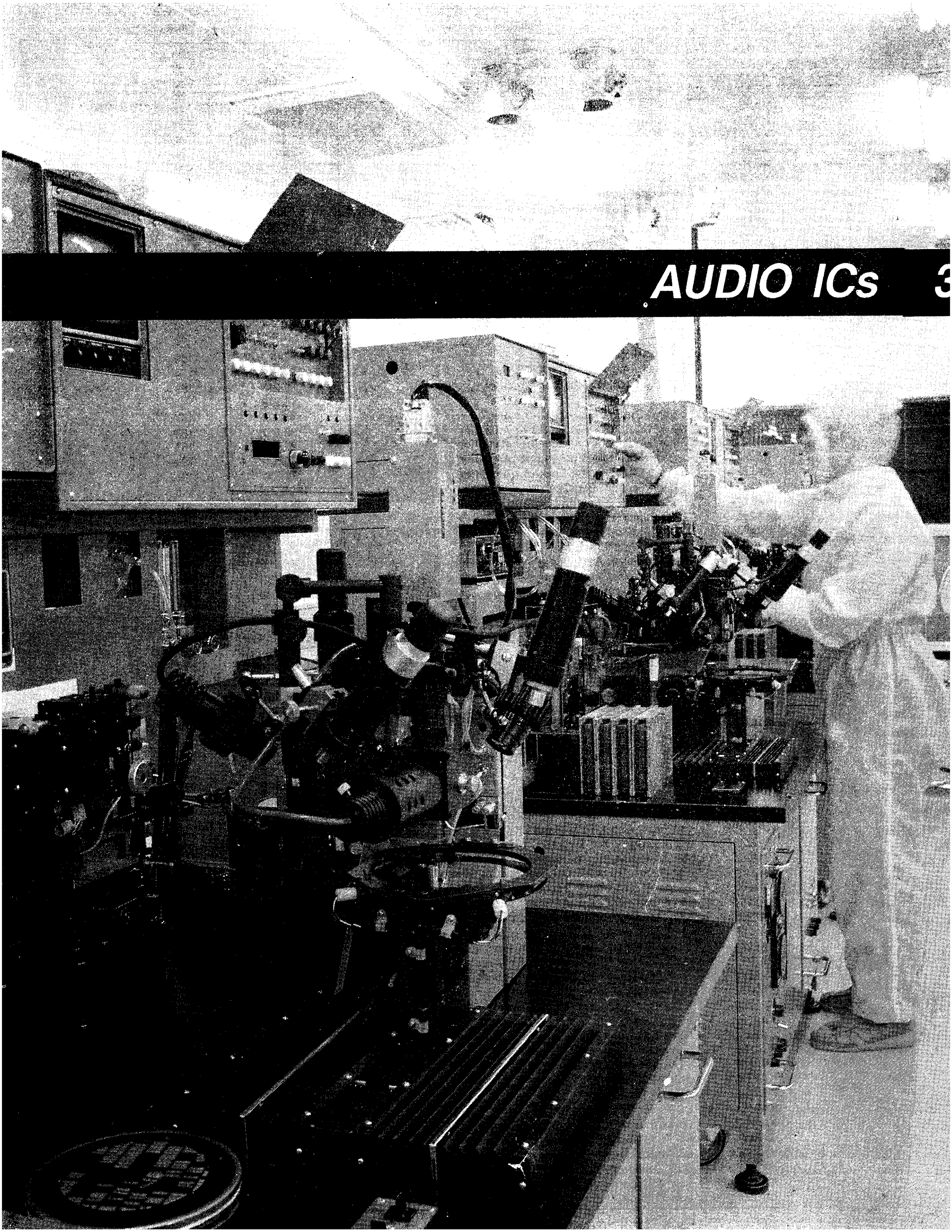
PACKAGE TYPE

IC'S ONLY

D	SOP
DT	D-PACK
J	CERAMIC
K	TO-3P
L	LCCC
N	PLASTIC
PL	PLCC
R	TO-126
T	TO-220
Z	TO-92
V	TO-92L
W	ZIP
S	SIP
G	BARE CHIP
E	SSM

• NOTE: Direct-Replacement parts for products initiated by other manufacturers.

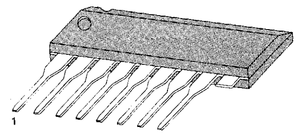
NOTES


AUDIO ICs 3

DUAL LOW NOISE EQUALIZER AMPLIFIER

The KA1222 is a monolithic integrated circuit consisting of a 2-channel pre-amplifier in a 8-pin plastic single in line package. Minimum operating voltage is 2.5 volts, thus it is suitable for low voltage application.

8 SIP



FEATURES

- Wide operating supply voltage range (2.5V ~ 6V).
- Low noise (V_{NI} = 1.0μ V: Typ).
- High channel separation.
- Good ripple rejection ratio.
- Minimum number of external parts required.

ORDERING INFORMATION

Device	Package	Operating Temperature
KA1222	8 SIP	−20 ~ +70°C

SCHEMATIC DIAGRAM

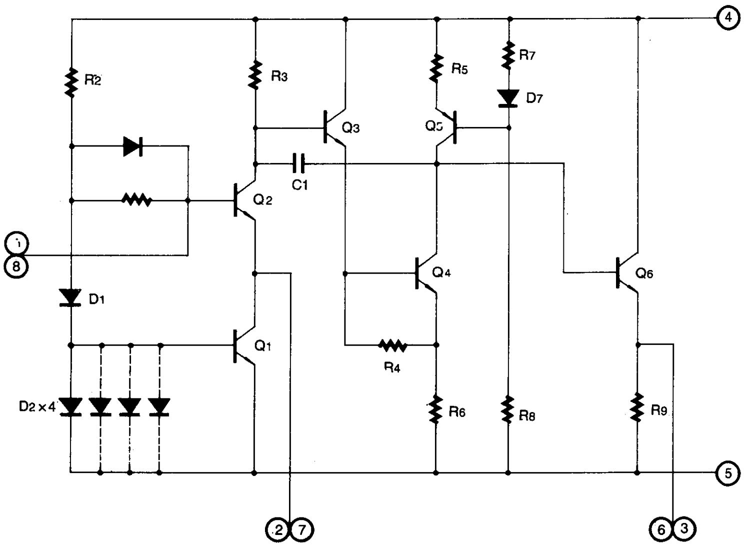


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.5	V
Power Dissipation	P_d	200	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=4V, R_L=10KΩ, R_g=600Ω, f=1KHz, NAB, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i=0		2.0	6.0	mA
Voltage Gain (Open Loop)	A_{VO}		65	80		dB
Voltage Gain (Closed Loop)	A_V	V_O=0.2V	33	35	37	dB
Output Voltage	V_O	THD=1%	0.4	0.7		V
Total Harmonic Distortion	THD	V_O=0.2V		0.1	0.3	%
Input Resistance	R_i			150		KΩ
Equivalent Input Noise Voltage	V_{NI}	R_g=2.2KΩ BW (−3dB)=15Hz ~ 30KHz		1.0	2.0	μV
Cross Talk	CT	R_g=2.2KΩ	50	65		dB

TEST CIRCUIT

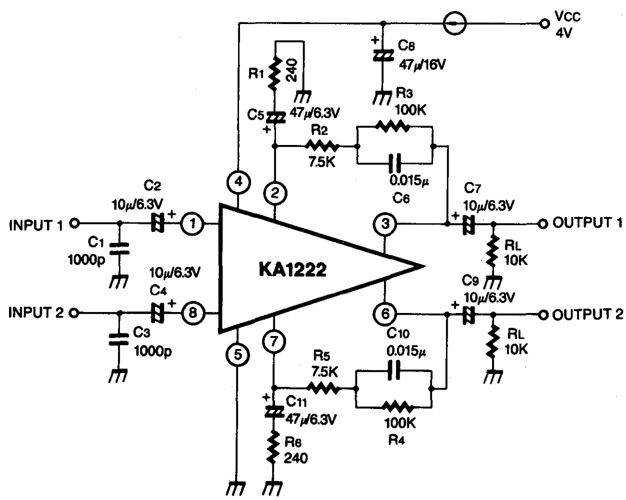
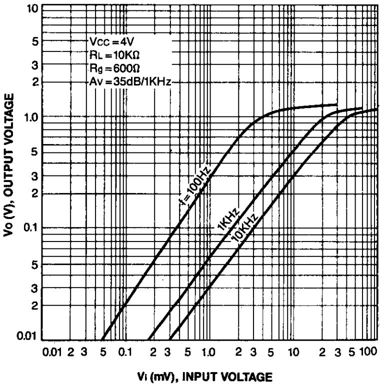
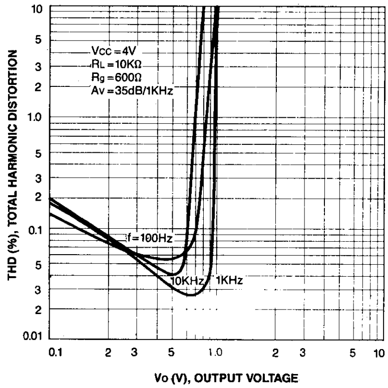


Fig. 2

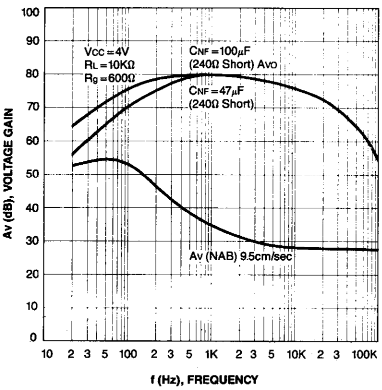
OUTPUT VOLTAGE-INPUT VOLTAGE



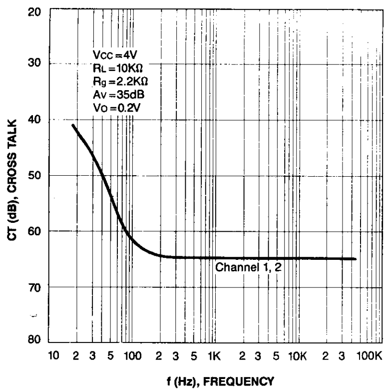
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



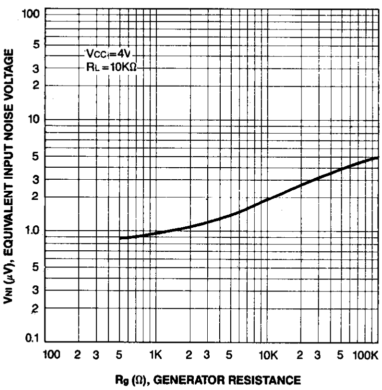
VOLTAGE GAIN-FREQUENCY



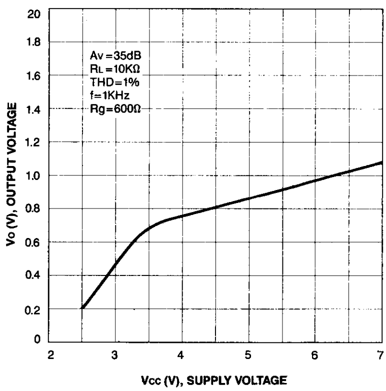
CROSS TALK-FREQUENCY



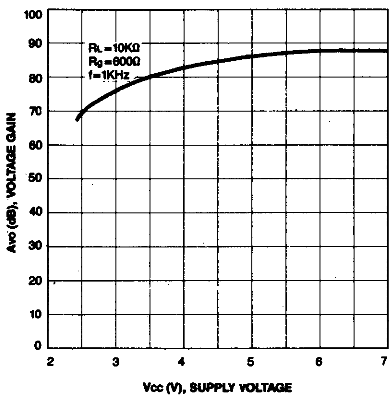
EQUIVALENT INPUT NOISE VOLTAGE
GENERATOR RESISTANCE



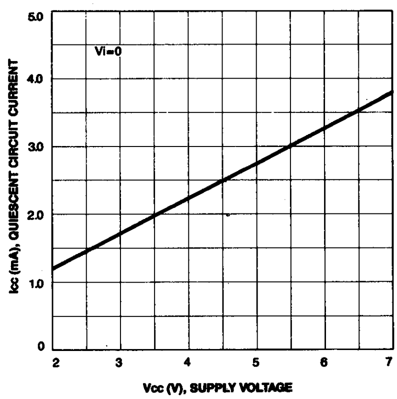
OUTPUT VOLTAGE-SUPPLY VOLTAGE



VOLTAGE GAIN-SUPPLY VOLTAGE



QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



TYPICAL APPLICATION CIRCUIT

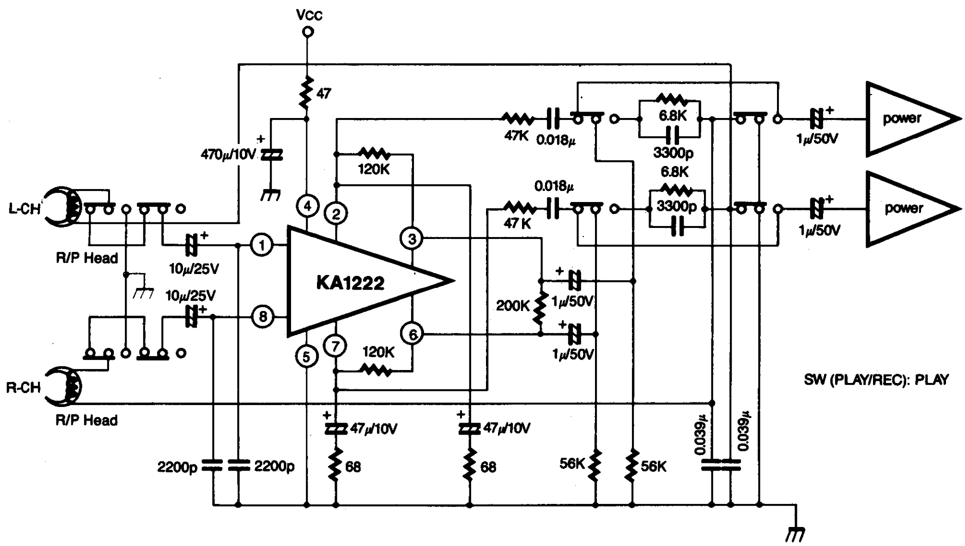
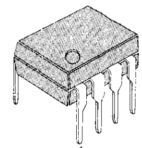


Fig. 3

1.2W AUDIO POWER AMPLIFIER

The KA2201 is a monolithic integrated audio amplifier in a 8-pin plastic dual in line package designed for audio frequency class B amplifiers.

8 DIP



FEATURES

- Wide operating supply voltage (3V ~ 14V)
- Medium output power.
  P_O=1.2W at V_{CC}=9V, R_L=8Ω, THD=10%.
- Low quiescent circuit current (I_{CC}=4mA: Typ).
- Good ripple rejection.
- Minimum number of external parts required.

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2201	8 DIP	−20 ~ +70°C
KA2201N		
KA2201G	PELLET	

SCHEMATIC DIAGRAM

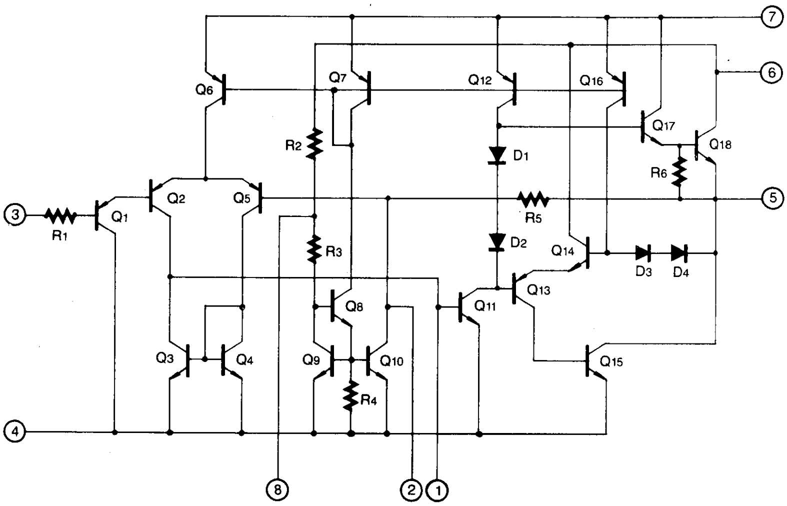


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Output Peak Current	I_O	1.5	A
Power Dissipation	P_d	1.25	W
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 9V, f = 1KHz, R_g = 600Ω, R_f = 120Ω, R_L = 8Ω unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i = 0		4	12	mA
Output Power	P_O	V_{CC} = 9V, R_L = 4Ω, THD = 10%		1.6		W
		V_{CC} = 9V, R_L = 8Ω, THD = 10%	0.9	1.2		
		V_{CC} = 6V, R_L = 4Ω, THD = 10%		0.75		
		V_{CC} = 6V, R_L = 8Ω, THD = 10%	0.4	0.5		
		V_{CC} = 12V, R_L = 8Ω, THD = 10%		2		
Total Harmonic Distortion	THD	P_O = 500mW		0.3	1.0	%
Voltage Gain (Open Loop)	A_{VO}	R_f = 0		75		dB
Voltage Gain (Closed Loop)	A_V	R_f = 120Ω	33	36	39	dB
Input Resistance	R_i			5		MΩ
Output Noise Voltage	V_{NO}	Rg = 10KΩ BW (−3dB) = 50Hz ~ 20KHz		0.3	1.0	mV

TEST CIRCUIT

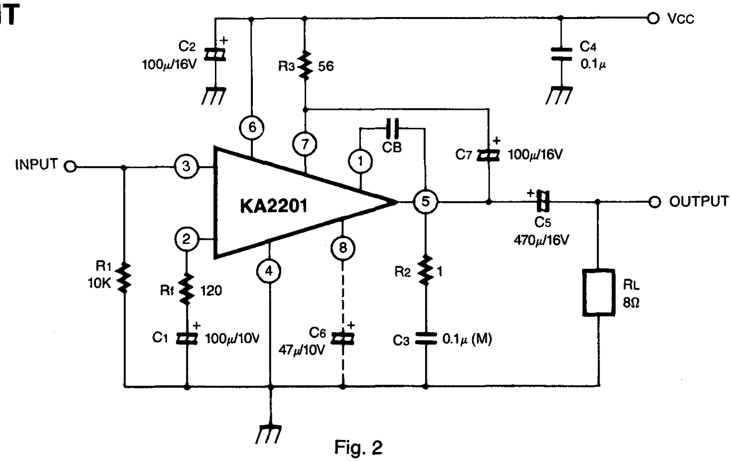
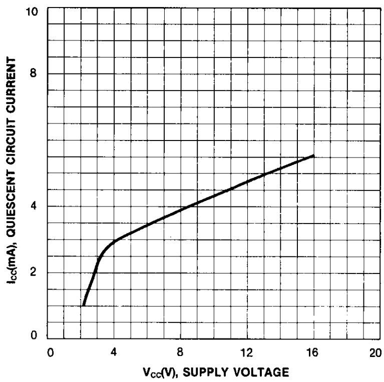
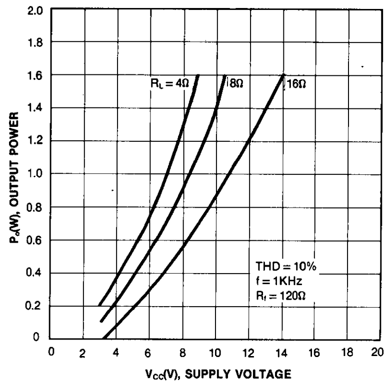


Fig. 2

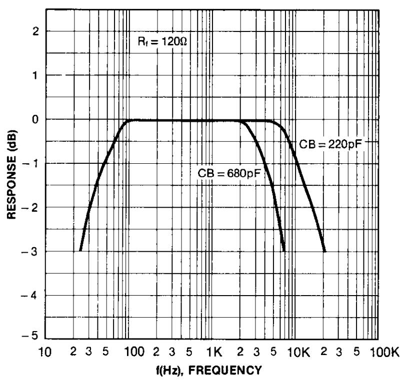
QUIESCENT CIRCUIT CURRENT—SUPPLY VOLTAGE



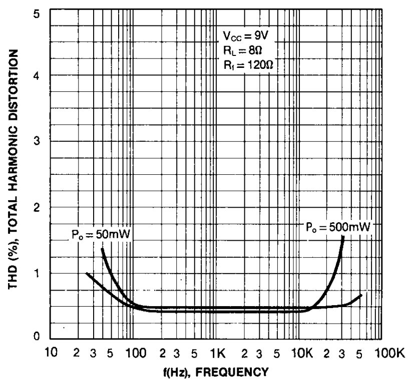
OUTPUT POWER-SUPPLY VOLTAGE



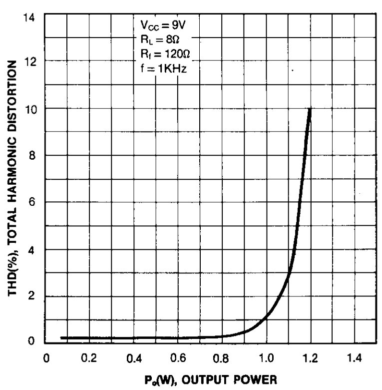
FREQUENCY RESPONSE



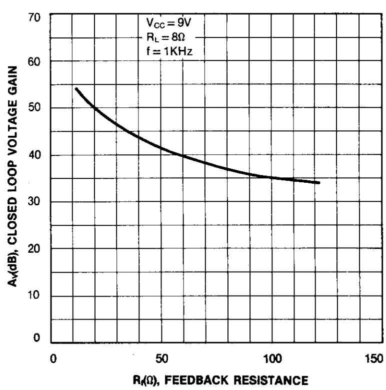
TOTAL HARMONIC DISTORTION-FREQUENCY

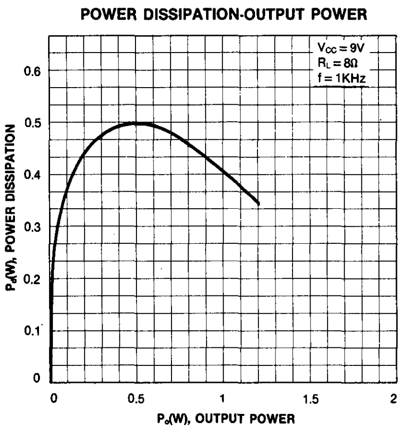


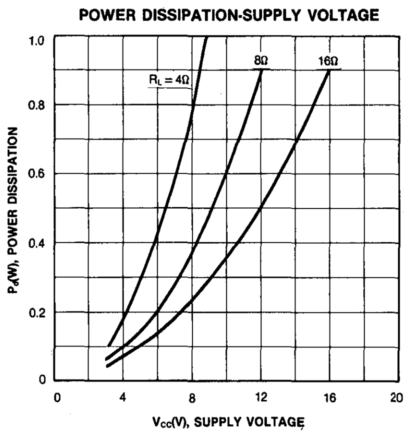
TOTAL HARMONIC DISTORTION-OUTPUT POWER



VOLTAGE GAIN-FEEDBACK RESISTANCE



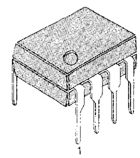

POWER DISSIPATION-OUTPUT POWER
Vcc = 9V
RL = 8Ω
f = 1KHz
0.6
0.5
0.4
0.3
0.2
0.1
0
Pd(W), POWER DISSIPATION
0
0.5
1
1.5
2
Po(W), OUTPUT POWER


POWER DISSIPATION-SUPPLY VOLTAGE
1.0
0.8
0.6
0.4
0.2
0
RL = 4Ω
8Ω
16Ω
Pd(W), POWER DISSIPATION
0
4
8
12
16
20
Vcc(V), SUPPLY VOLTAGE

0.5W AUDIO POWER AMPLIFIER

The KA2201B is a monolithic integrated audio amplifier in a 8-pin plastic dual in line package, designed for audio frequency class B amplifiers.

8 DIP



FEATURES

- Wide operating supply voltage (3V ~ 12V).
- Medium output power.
  P_O=0.5W at V_{CC}=6V, R_L=8Ω, THD=10%.
- Low quiescent circuit current (I_{CC}=3.5mA: Typ).
- Good ripple rejection.
- Minimum number of external parts required.
- Built-in bootstrap resistor R_7 (External resistor R_3 (56Ω) of the KA2201)

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2201B	8 DIP	−20 ~ +70°C

SCHEMATIC DIAGRAM

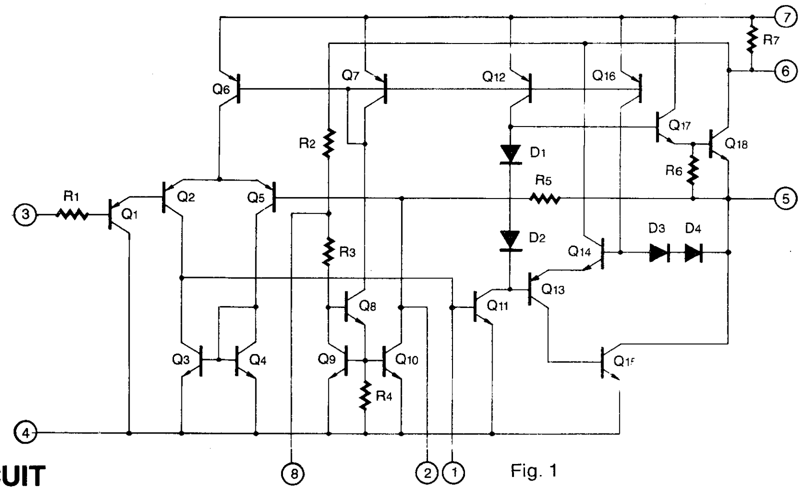


Fig. 1

TEST CIRCUIT

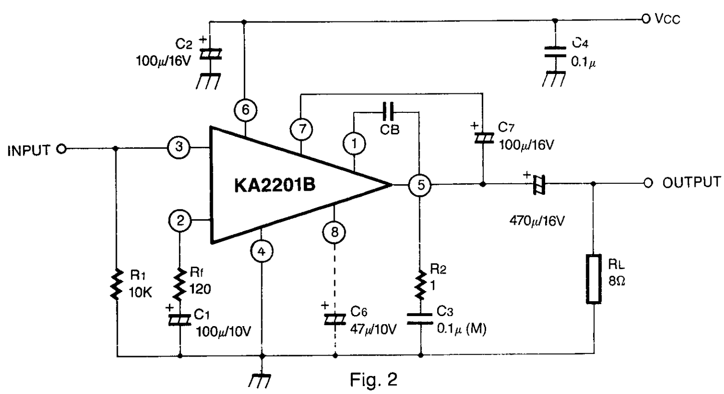


Fig. 2

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

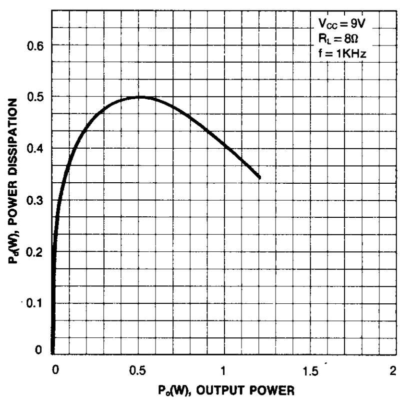
Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Output Peak Current	I_O	1.5	A
Power Dissipation	Pd	1.25	W
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

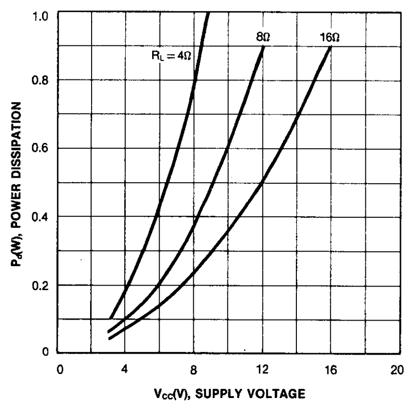
(T_a=25°C, V_{CC}=6V, f=1KHz, Rg=600Ω, R_L=8Ω unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i = 0		3.5	7.0	mA
Output Power	P_O	V_{CC} = 6V, R_L = 8Ω, THD = 10%	0.4	0.5		W
		V_{CC} = 6V, R_L = 4Ω, THD = 10%		0.75		
		V_{CC} = 9V, R_L = 8Ω, THD = 10%	0.9	1.2		
		V_{CC} = 9V, R_L = 4Ω, THD = 10%		1.6		
		V_{CC} = 12V, R_L = 8Ω, THD = 10%		2		
Total Harmonic Distortion	THD	P_O = 100mW		0.3	1.0	%
Voltage Gain (Open Loop)	A_{VO}	R_f = 0		75		dB
Voltage Gain (Closed Loop)	A_V	R_f = 120Ω	33	36	39	dB
Input Resistance	R_i			5		MΩ
Output Noise Voltage	V_{NO}	Rg = 10KΩ BW (−3dB) = 50Hz ~ 20KHz		0.3	1.0	mV

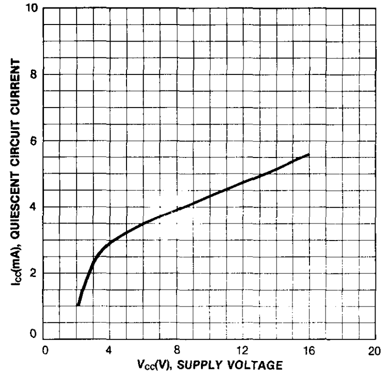
POWER DISSIPATION-OUTPUT POWER



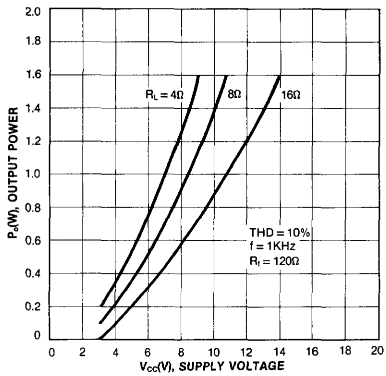
POWER DISSIPATION-SUPPLY VOLTAGE



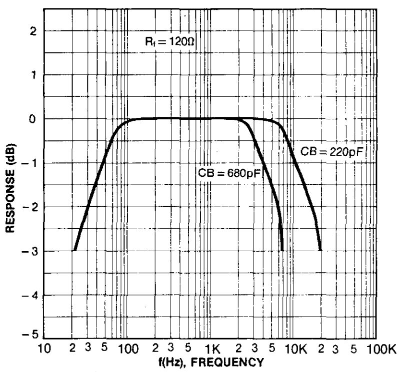
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



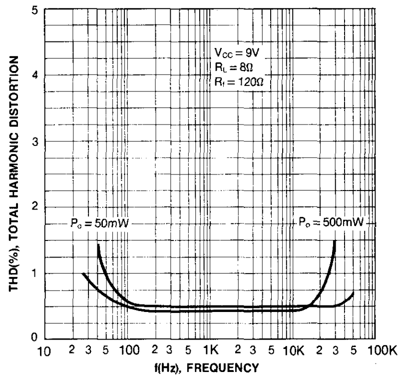
OUTPUT POWER-SUPPLY VOLTAGE



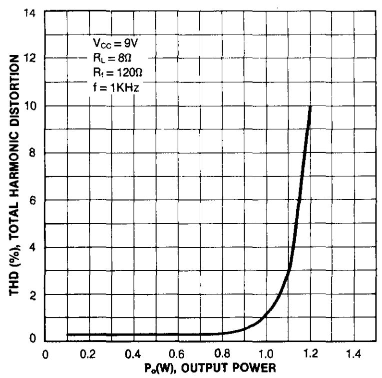
FREQUENCY RESPONSE



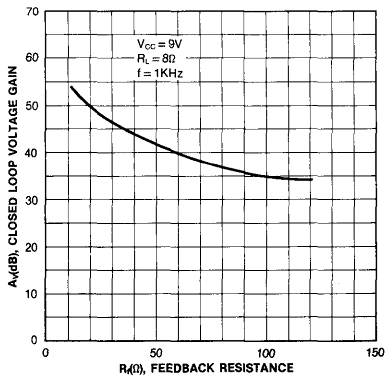
TOTAL HARMONIC DISTORTION-FREQUENCY



TOTAL HARMONIC DISTORTION-OUTPUT POWER



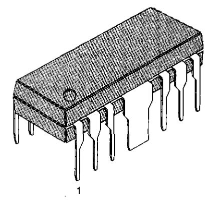
VOLTAGE GAIN-FEEDBACK RESISTANCE



2.3W DUAL AUDIO POWER AMPLIFIER

The KA2206 is a monolithic integrated circuit consisting of a 2-channel power amplifier. It is suitable for stereo and bridge amplifier application of radio cassette tape recorders.

12 DIP/F



FEATURES

- **High output power**
  Stereo: P_O=2.3W (Typ) at V_{CC}=9V, R_L=4Ω.
  Bridge: P_O=4.7W (Typ) at V_{CC}=9V, R_L=8Ω.
- **Low switching distortion at high frequency.**
- **Small shock noise at the time of power on/off due to a built-in muting circuit**
- **Good ripple rejection due to a built-in ripple filter.**
- **Good channel separation.**
- **Soft tone at the time of output saturation.**
- **Closed loop voltage gain fixed 45dB (Bridge: 51dB) but availability with external resistor added.**
- **Minimum number of external parts required.**
- **Easy to design radiator fin.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2206	12 DIP/F	−20 ~ +70°C

BLOCK DIAGRAM

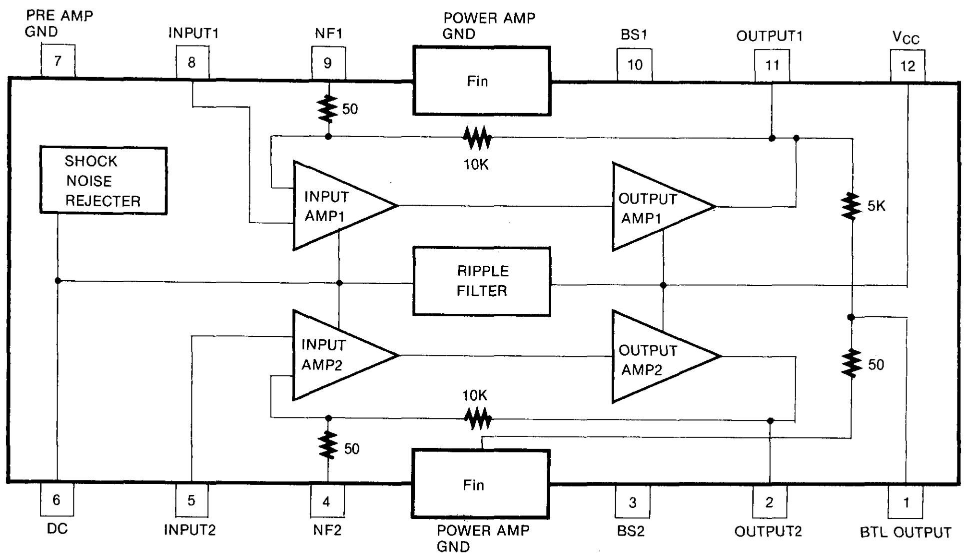


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Power Dissipation	P_d	4*	W
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +150	°C

* Fin is soldering on the PCB

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 9V, f=1KHz R_g =600Ω, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Operating Supply Voltage	V_{CC}				9	11	V
Quiescent Circuit Current	I_{CC}	V_i =0, Stereo			40	55	mA
Closed Loop Voltage Gain	A_V	Stereo	V_i = −45dBm	43	45	47	dB
		Bridge		49	51	53	dB
Channel Balance	CB	Stereo		−1	0	+1	dB
Output Power	P_O	Stereo	R_L =4Ω, THD=10%,	1.7	2.3		W
			R_L =8Ω, THD=10%		1.3		W
		Bridge	R_L =8Ω, THD=10%		4.7		W
Total Harmonic Distortion	THD	Stereo	P_O =250mW, R_L =4Ω		0.3	1.5	%
		Bridge			0.5		%
Input Resistance	R_i			21	30		KΩ
Ripple Rejection	RR	Stereo, R_g =0Ω, V_r = 150mV f=100Hz		40	46		dB
Output Noise Voltage	V_{NO}	Stereo, R_g =0Ω			0.3	1.0	mV
		Stereo, R_g =10KΩ			0.5	2.0	mV
Cross Talk	CT	Stereo, R_g =10KΩ, V_o =0dBm		40	55		dB

TYPICAL APPLICATION CIRCUIT: Stereo Amplifier

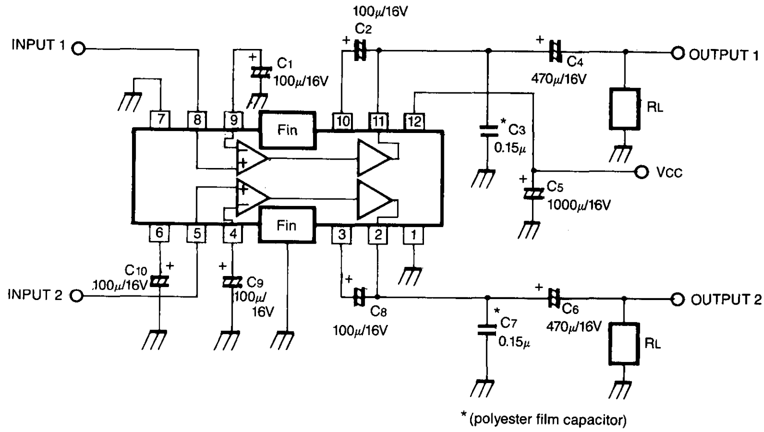


Fig. 2

TYPICAL APPLICATION CIRCUIT: Bridge Amplifier

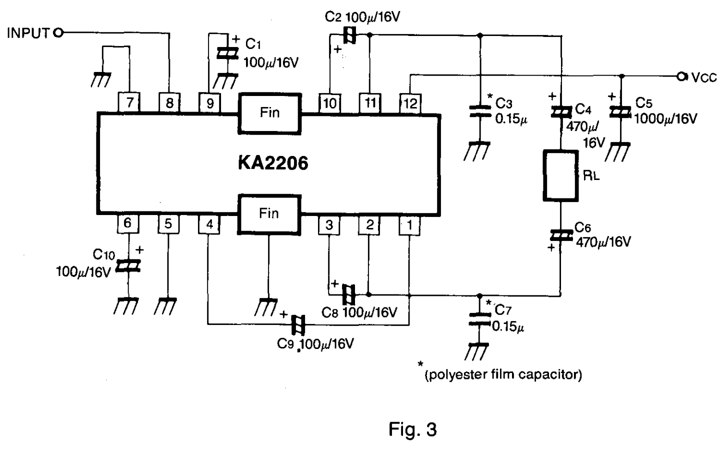
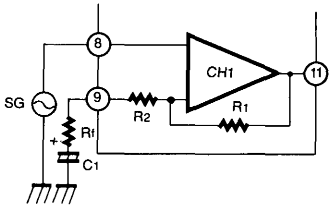


Fig. 3

VOLTAGE GAIN ADJUSTMENT

1. Stereo application



i) **Fixed voltage gain**
(Pin 9 connected to GND directly)

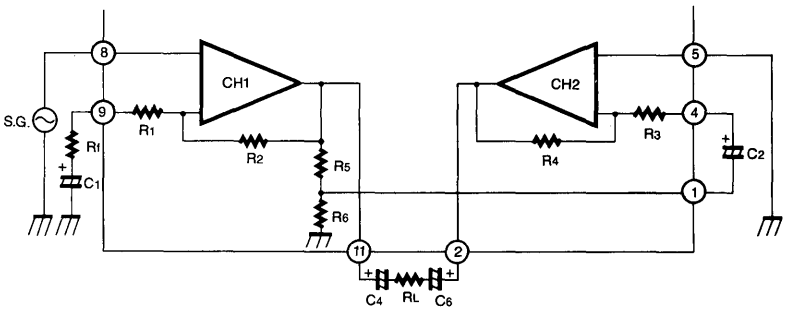
$$Av = 20 \log \frac{R_1}{R_2} (dB)$$

ii) **Variable voltage gain**
(Rf and C1 connected with pin 9)

$$Av = 20 \log \frac{R_1}{R_2 + R_f} (dB)$$

3

2. Bridge application



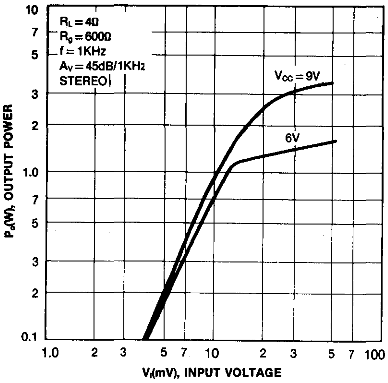
i) **Fixed voltage gain** (Pin 9 connected to GND directly)

$$Av = 20 \log \frac{R_2}{R_1} + 6 (dB)$$

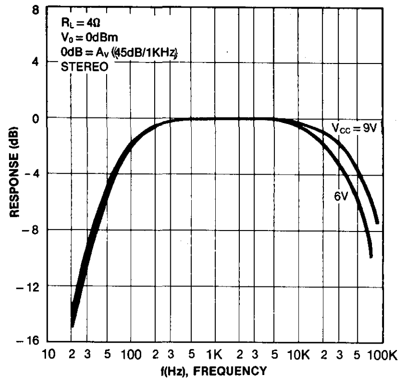
ii) **Variable voltage gain** (R_f and C_1 connected with pin 9)

$$Av = 20 \log \frac{R_2}{R_1 + R_f} + 6 (dB)$$

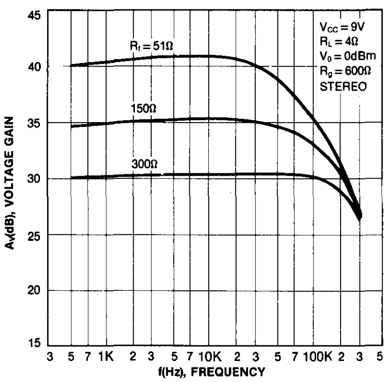
OUTPUT POWER-INPUT VOLTAGE



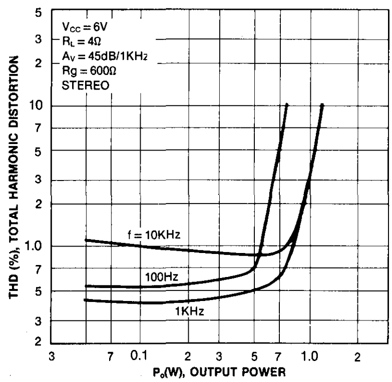
FREQUENCY RESPONSE



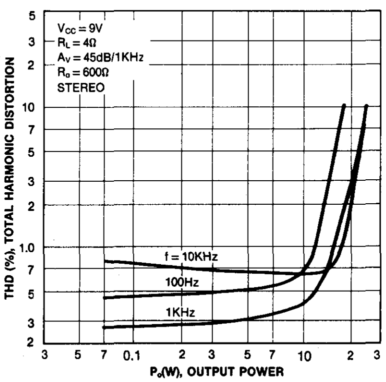
VOLTAGE GAIN-FREQUENCY



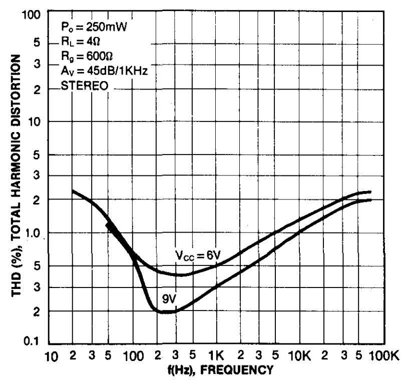
TOTAL HARMONIC DISTORTION-OUTPUT POWER



TOTAL HARMONIC DISTORTION-OUTPUT POWER

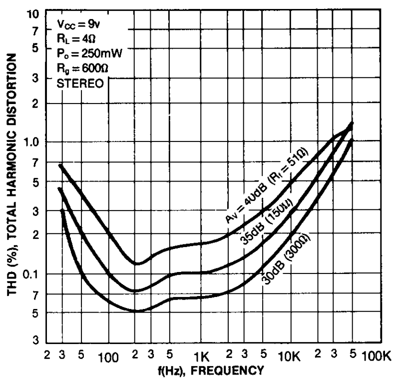


TOTAL HARMONIC DISTORTION-FREQUENCY

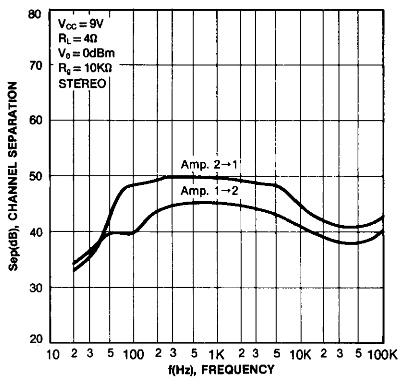


3

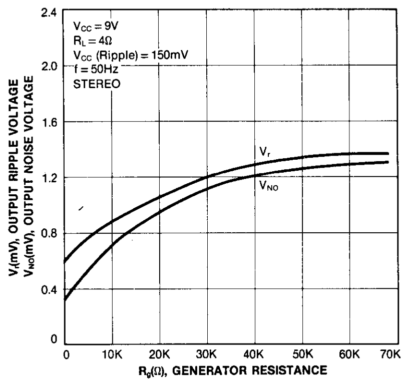
TOTAL HARMONIC DISTORTION-FREQUENCY



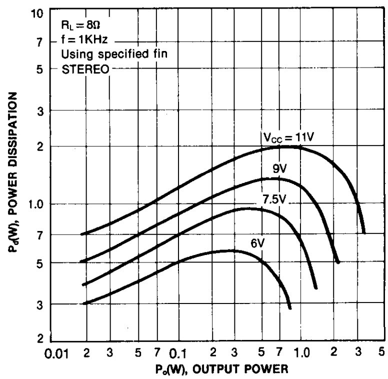
CHANNEL SEPARATION-FREQUENCY



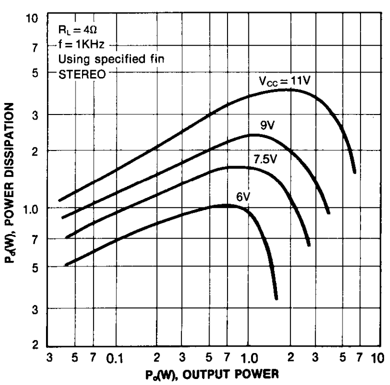
OUTPUT RIPPLE VOLTAGE / OUTPUT NOISE VOLTAGE -GENERATOR RESISTANCE



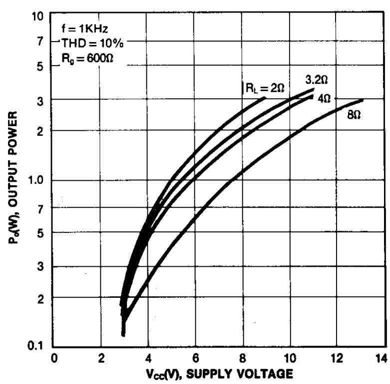
POWER DISSIPATION-OUTPUT POWER



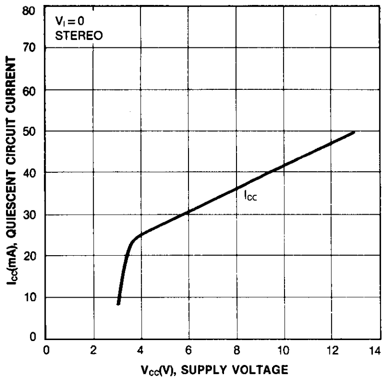
POWER DISSIPATION -OUTPUT POWER



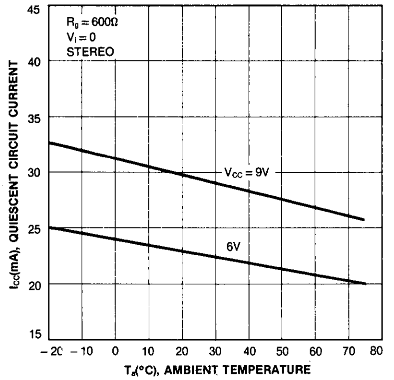
OUTPUT POWER-SUPPLY VOLTAGE



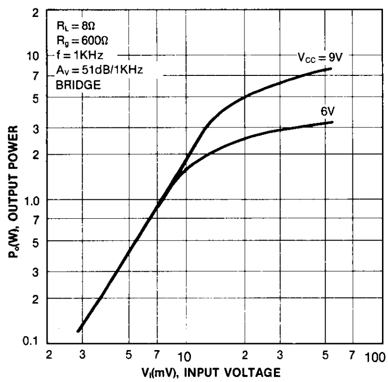
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



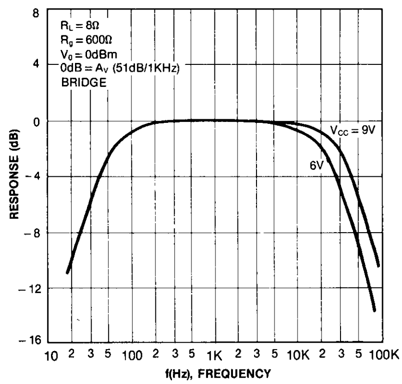
QUIESCENT CIRCUIT CURRENT-AMBIENT TEMPERATURE



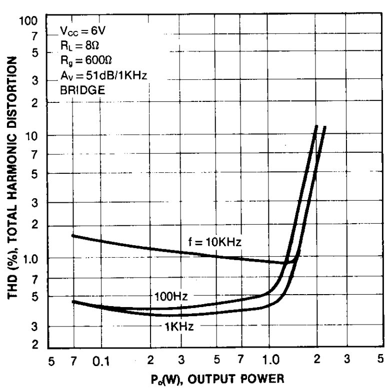
OUTPUT POWER-INPUT VOLTAGE



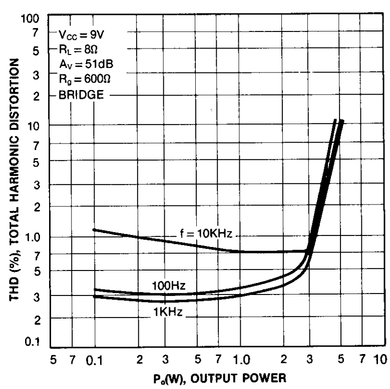
FREQUENCY RESPONSE



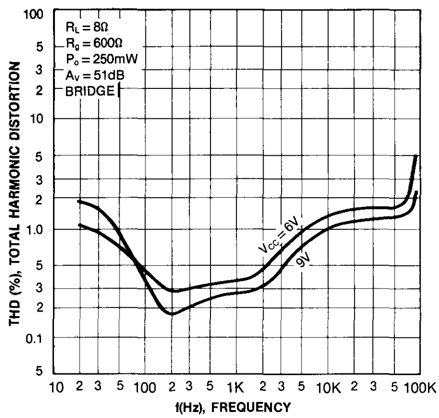
TOTAL HARMONIC DISTORTION-OUTPUT POWER



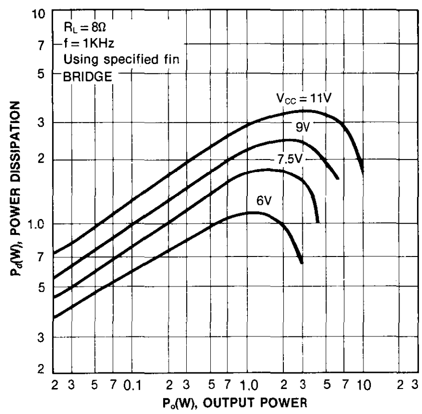
TOTAL HARMONIC DISTORTION-OUTPUT POWER



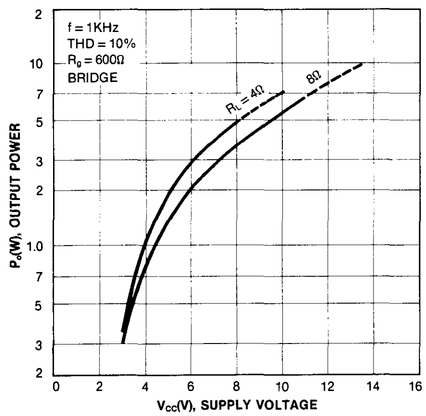
TOTAL HARMONIC DISTORTION-FREQUENCY



POWER DISSIPATION-OUTPUT POWER



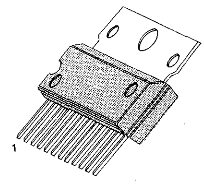
OUTPUT POWER-SUPPLY VOLTAGE



4.5W DUAL POWER AMPLIFIER

The KA22062 is a monolithic integrated circuit consisting of a dual power amplifier. It is suitable for portable radio cassette recorders.

12 SIP H/S



FEATURES

- **Dual power amplifier: 4.5W x 2 (Typ)**
- **Low quiescent circuit current; I_{CC} = 19mA (Typ)**
- **High output**
- **Small pop noise at the power on**
- **Minimum external parts required**
- **Supply voltage range: V_{CC} = 6V ~ 15V**
- **Including the thermal)tection circuit**
- **Connect H/S to GND**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22062S	12 SIP H/S	−20 ~ +70°C
KA22062G	PELLET	

BLOCK DIAGRAM

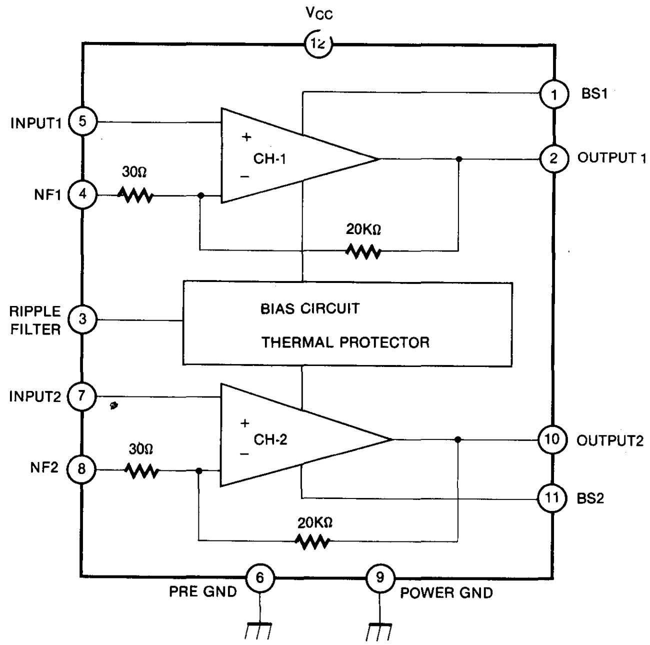


Fig. 1

3

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Output Current (1CH)	I_o (peak)	2.5	A
Power Dissipation	P_d	12.5	W
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 9V, R_L = 4Ω, f = 1KHz, R_g = 600Ω, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i = 0		19	45	mA
Output Power	P_O	THD = 10%	2.0	2.5		W
		THD = 10%, V_{CC} = 12V		4.5		W
Total Harmonic Distortion	THD	P_o = 1W		0.2	1.0	%
Voltage Gain (Closed Loop)	A_V	R_f = 82Ω, V_o = 0.775V	43	45	47	dB
		R_f = 0Ω, V_o = 0.775V		56		dB
Input Resistance	R_i			30		KΩ
Output Noise Voltage	V_{NO}	R_g = 10KΩ, BW(−3 dB) = 20Hz ~ 20KHz		0.3	1.0	mV
Ripple Rejection Ratio	RR	R_g = 600Ω, f = 120Hz, V_r = 300mV		54		dB
Cross Talk	CT	R_g = 10KΩ, V_o = 0dBm		60		dB
Input Offset Voltage	V_5, V_7			20	60	mV

TEST CIRCUIT

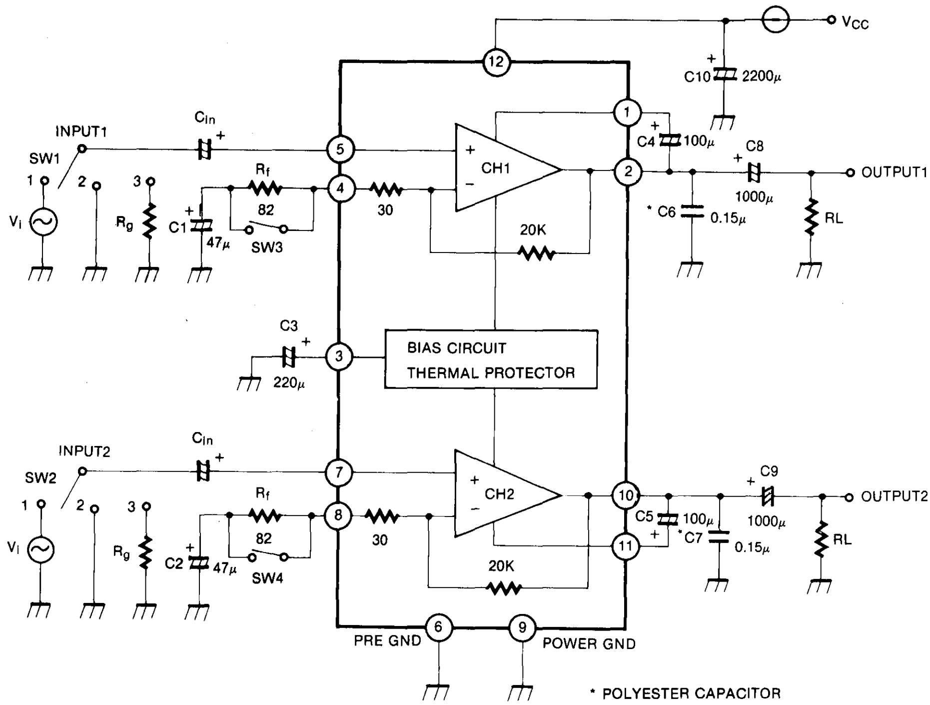
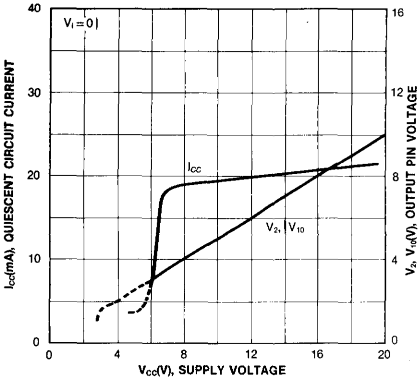
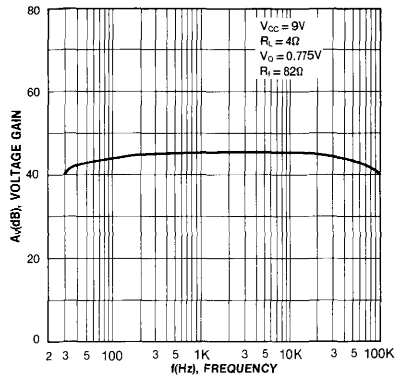


Fig. 2

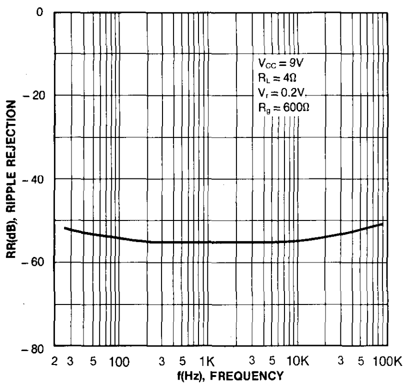
QUIESCENT CIRCUIT CURRENT·SUPPLY VOLTAGE
OUTPUT PIN VOLTAGE



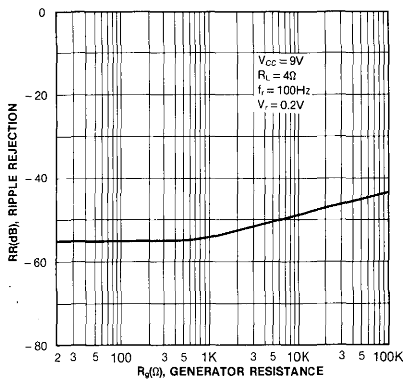
VOLTAGE GAIN-FREQUENCY



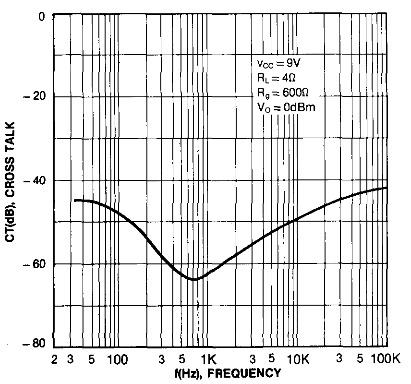
RIPPLE REJECTION-FREQUENCY



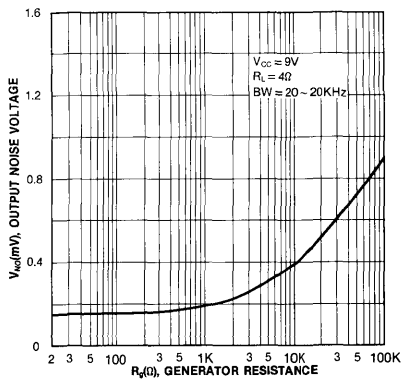
RIPPLE REJECTION-GENERATOR RESISTANCE



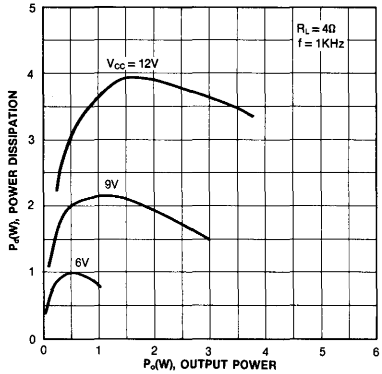
CROSS TALK-FREQUENCY



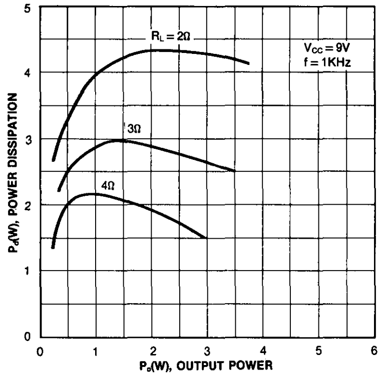
OUTPUT NOISE VOLTAGE-GENERATOR RESISTANCE



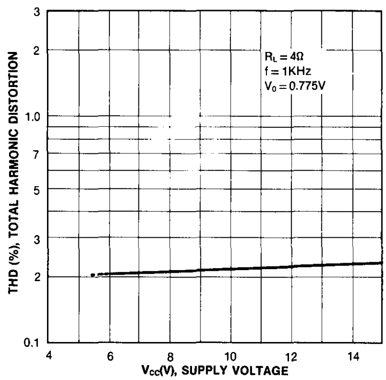
POWER DISSIPATION-OUTPUT POWER



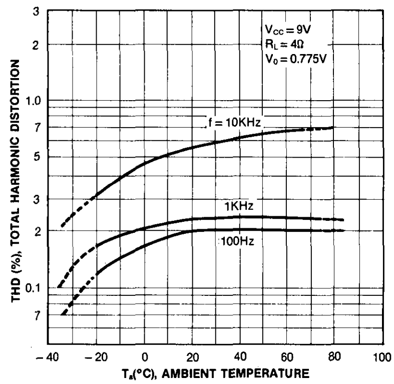
POWER DISSIPATION-OUTPUT POWER



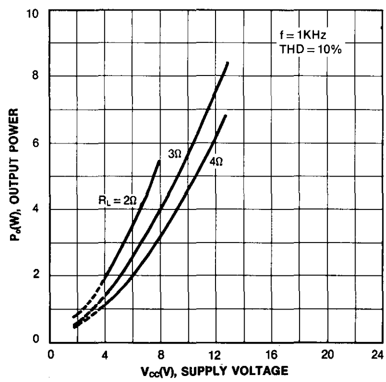
TOTAL HARMONIC DISTORTION-SUPPLY VOLTAGE



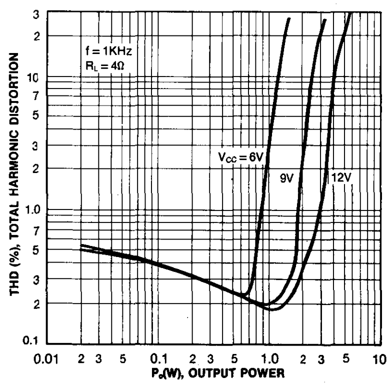
TOTAL HARMONIC DISTORTION-AMBIENT TEMPERATURE



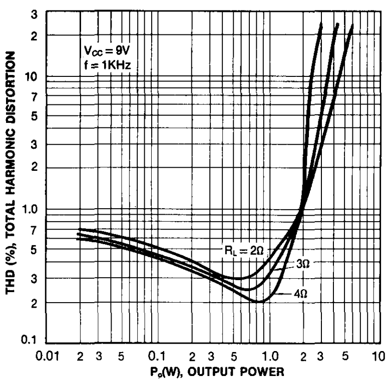
OUTPUT POWER-SUPPLY VOLTAGE



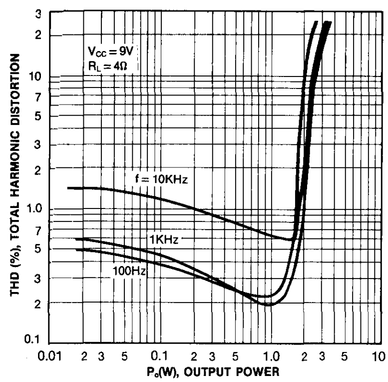
TOTAL HARMONIC DISTORTION-OUTPUT POWER



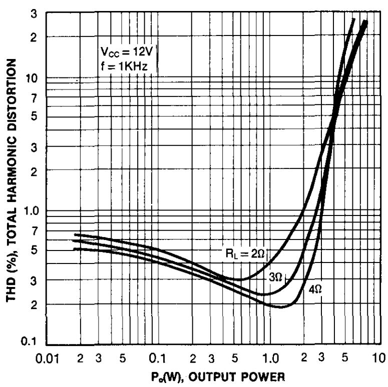
TOTAL HARMONIC DISTORTION-OUTPUT POWER



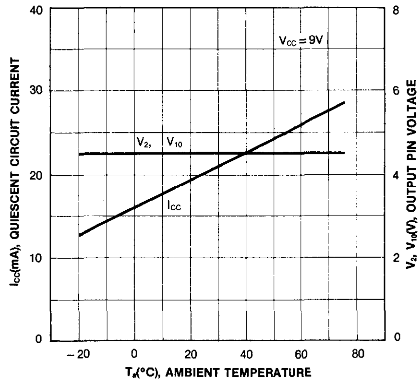
TOTAL HARMONIC DISTORTION-OUTPUT POWER



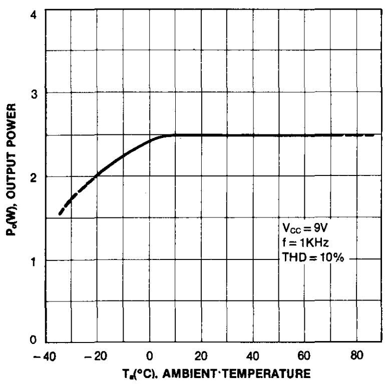
TOTAL HARMONIC DISTORTION-OUTPUT POWER



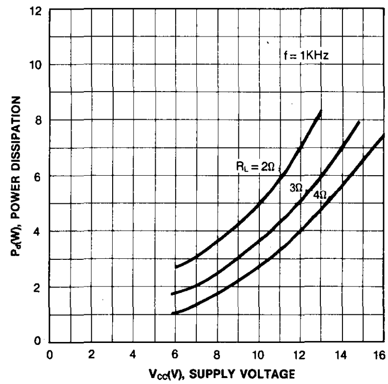
QUIESCENT CIRCUIT CURRENT / OUTPUT PIN VOLTAGE -AMBIENT TEMPERATURE



OUTPUT POWER-AMBIENT TEMPERATURE



POWER DISSIPATION-SUPPLY VOLTAGE



APPLICATION CIRCUIT

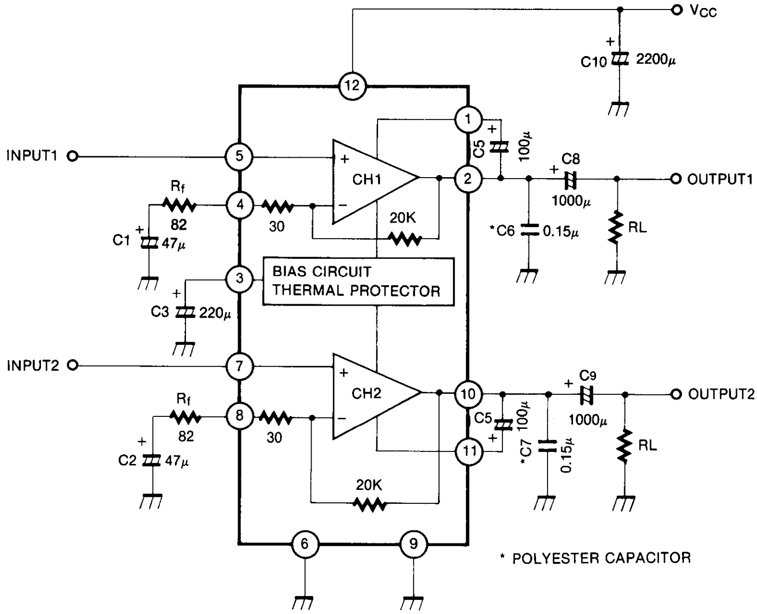
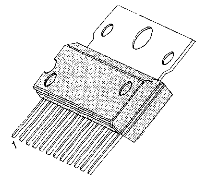


Fig. 3

4.5W DUAL POWER AMP

The KA22063 is a monolithic integrated circuit consisting of a 2-channel power amplifier with a power on/off (stand-by switch) function. It is suitable for portable radio cassette recorders.

12 SIP H/S



3

FEATURES

- **2-channel amplifier: 4.5W × 2 (typ.)**
- **Low quiesent circuit current: I_{CC} = 16mA (typ.)**
- **High output**
- **Small pop noise at the power on**
- **Minimum external parts required**
- **Supply voltage: 6V to 15V**
- **Including the thermal protection circuit**
- Connect H/S to GND

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22063S	12 SIP H/S	− 20 ~ + 70°C

BLOCK DIAGRAM

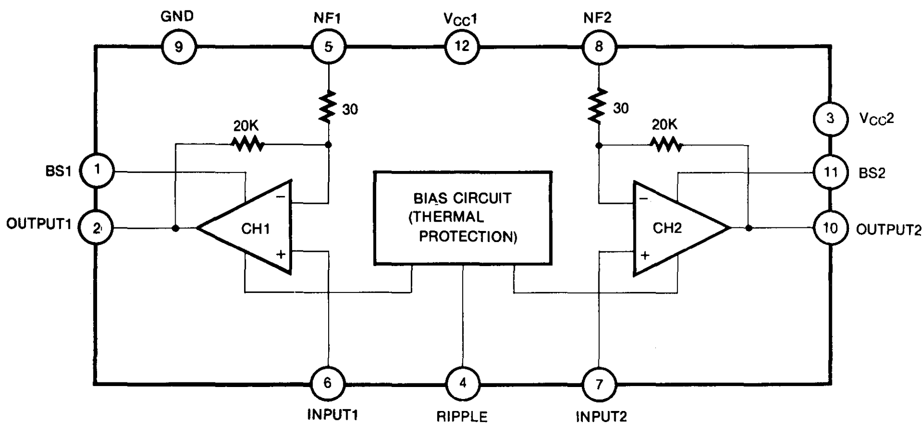


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Output Current (Channel)	I_O (peak)	2.5	A
Power Dissipation	P_d	12.5	W
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 9V, R_L = 4Ω, f = 1KHz, R_g = 600Ω, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i = 0		16	28	mA
Output Power	P_O1	THD = 10%	2.0	2.5		W
	P_O2	THD = 10%, V_{CC} = 12V		4.5		W
Total Harmonic Distortion	THD	P_O = 1W/CH		0.2	1.0	%
Voltage Gain (Closed Loop)	AV_1	R_f = 82Ω, V_o = 0.775V	43	45	47	dB
	AV_2	R_f = 0Ω, V_o = 0.775V		56		dB
Input Resistance	R_i			30		KΩ
Output Noise Voltage	V_{NO}	R_g = 10KΩ, BW = 20Hz – 20KHz		0.3	1.0	mV
Ripple Rejection Ratio	RR	R_g = 600Ω, f = 120Hz		54		dB
Cross Talk	C.T	R_g = 10KΩ, V_O = 0dBm, f = 1KHz		45		dB
Input Offset Voltage	V_5, V_7			20	60	mV

APPLICATION CIRCUIT

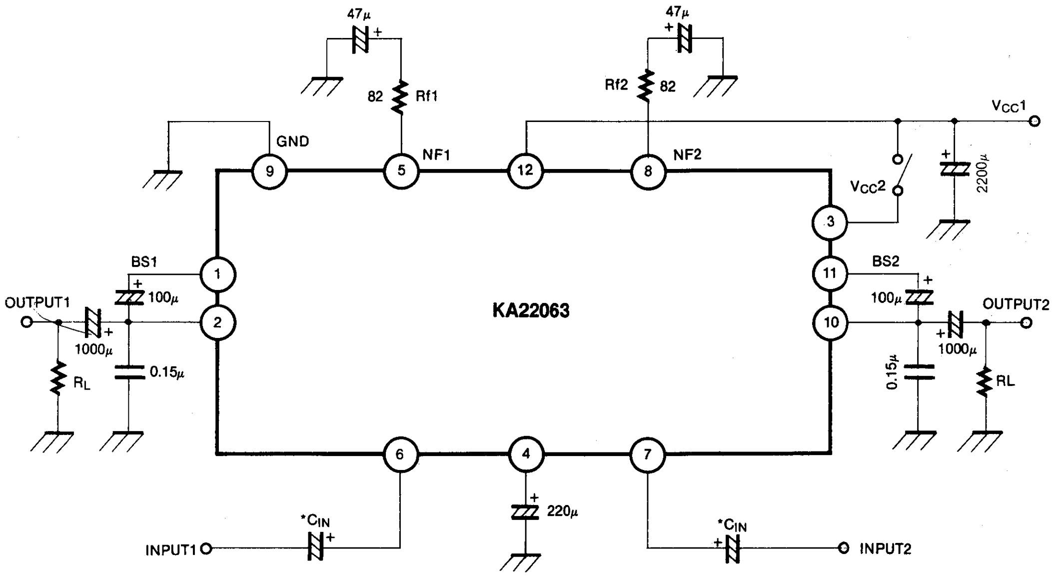
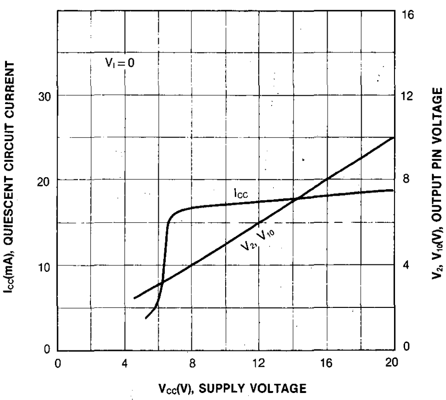
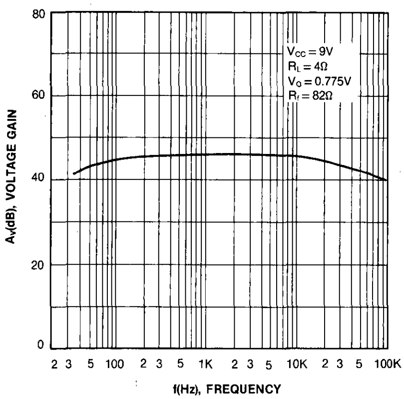


Fig. 2

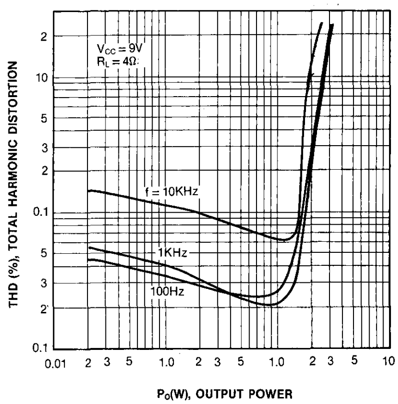
QUIESCENT CIRCUIT CURRENT
OUTPUT PIN VOLTAGE-SUPPLY VOLTAGE



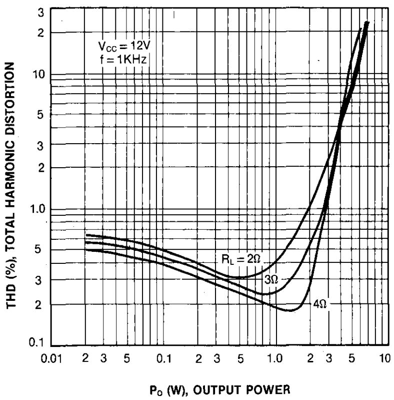
VOLTAGE GAIN-FREQUENCY



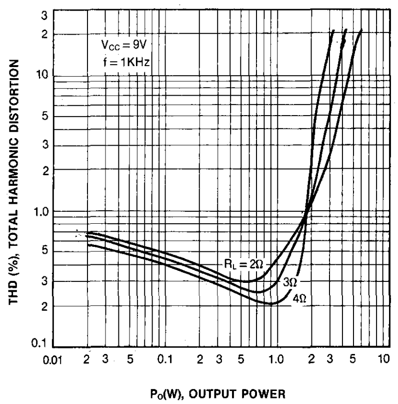
TOTAL HARMONIC DISTORTION-OUTPUT POWER



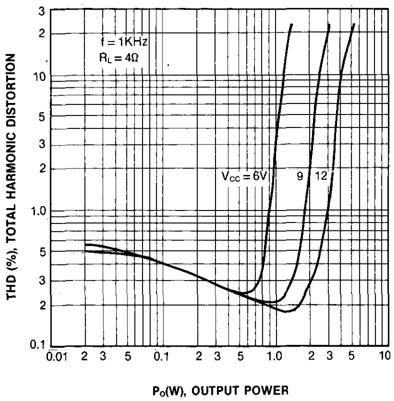
TOTAL HARMONIC DISTORTION-OUTPUT POWER



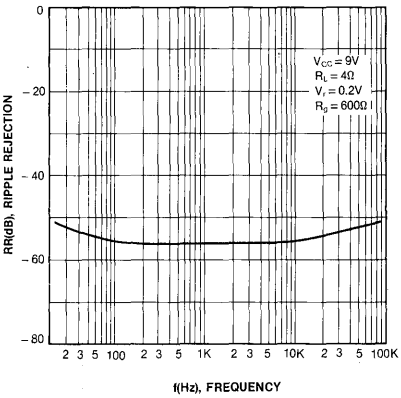
TOTAL HARMONIC DISTORTION-OUTPUT POWER



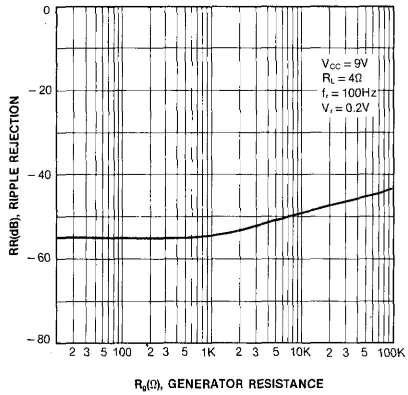
TOTAL HARMONIC DISTORTION-OUTPUT POWER



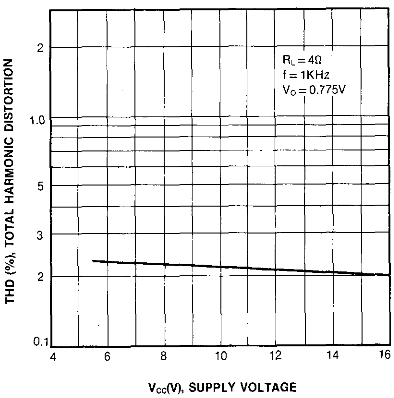
RIPPLE REJECTION-FREQUENCY



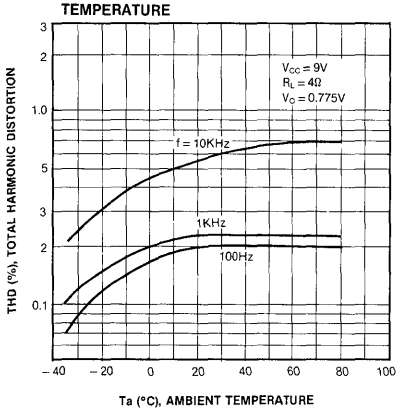
RIPPLE REJECTION-GENERATOR RESISTANCE



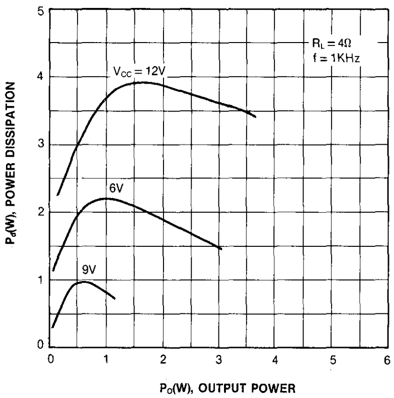
TOTAL HARMONIC DISTORTION-SUPPLY VOLTAGE



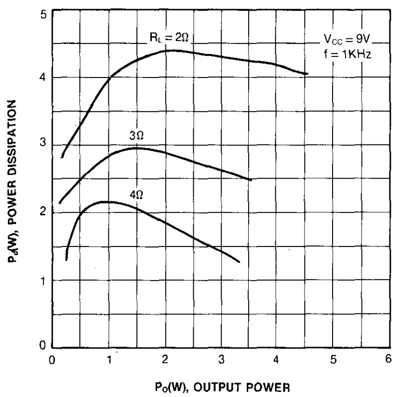
TOTAL HARMONIC DISTORTION-AMBIENT TEMPERATURE



POWER DISSIPATION-OUTPUT POWER



POWER DISSIPATION-OUTPUT POWER



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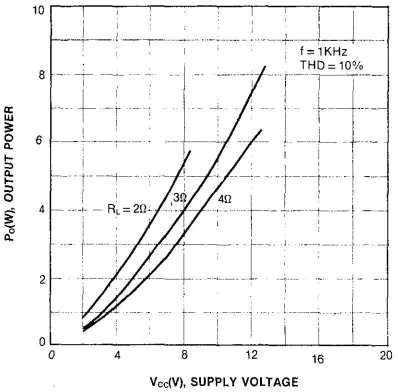
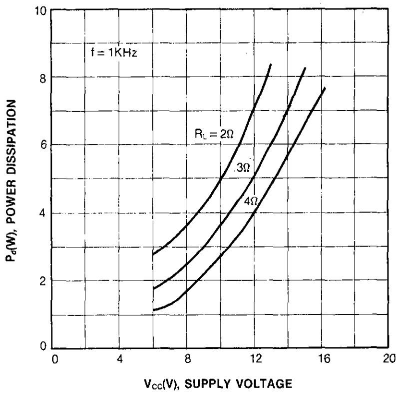
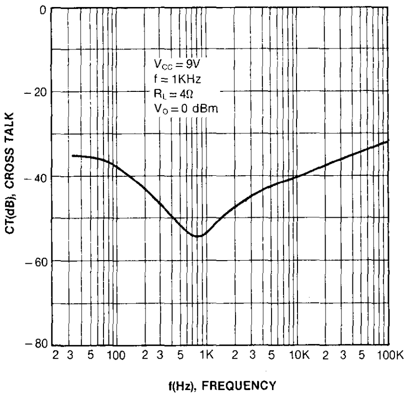
OUTPUT POWER-SUPPLY VOLTAGE



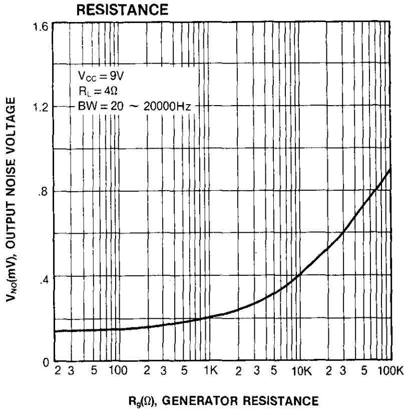
POWER DISSIPATION-SUPPLY VOLTAGE



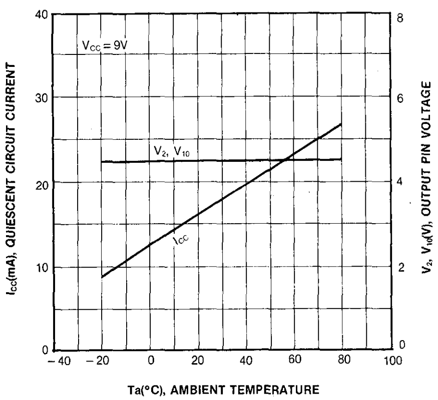
CROSS TALK-FREQUENCY



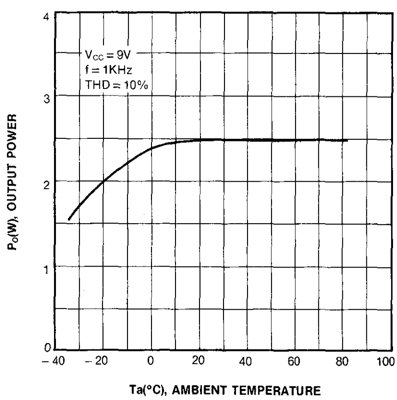
OUTPUT NOISE VOLTAGE-GENERATOR RESISTANCE



QUIESCENT CIRCUIT CURRENT
OUTPUT PIN VOLTAGE-AMBIENT TEMPERATURE



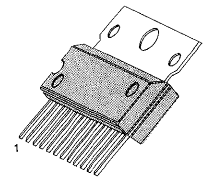
OUTPUT POWER-AMBIENT TEMPERATURE



4.6W DUAL POWER AMP

The KA22065 is a monolithic integrated circuit consisting of a 2-channel power amplifier with power on/off (stand-by switch) function. It is suitable for portable radio cassette recorders.

12 SIP H/S



FEATURES

- **2-channel amplifier: 4.6W x 2 (typ.)**
- **Low quiescent circuit current: I_{CC} = 21mA (typ.)**
- **High output (P_O = 4.6W, V_{CC} = 12V/8W)**
- **Small pop noise at power on**
- **Minimum external parts required**
- **Supply voltage: 6 V to 15 V**
- **Includes the thermal protection circuit**
- **Connect H/S to GND**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22065	12 SIP H/S	−20 ~ +70°C

BLOCK DIAGRAM

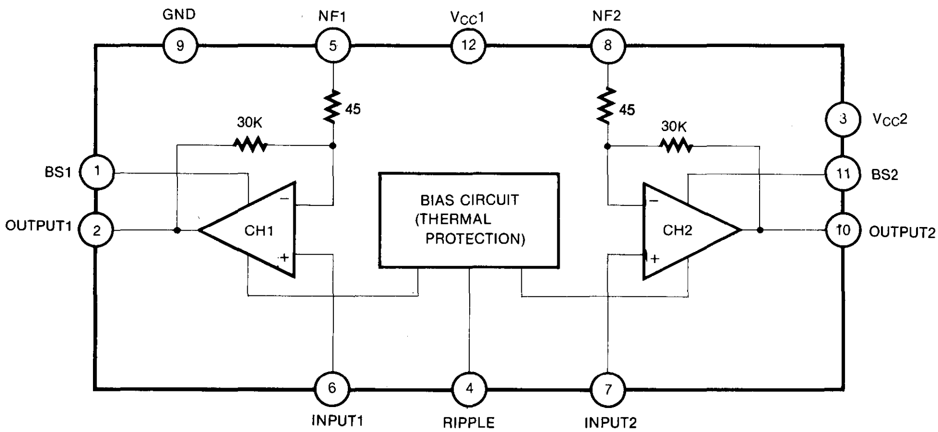


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	20	V
Output Current (Channel)	I_O (peak)	2.5	A
Power Dissipation	P_d	12.5	W
Operating Temperature	T_{opr}	− 20 ~ + 70	°C
Storage Temperature	T_{stg}	− 40 ~ + 150	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 9V, R_L = 4Ω, f = 1KHz, R_g = 600Ω, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i = 0		21	45	mA
Output Power	P_O1	THD = 10%	2.0	2.5		W
	P_O2	THD = 10%, V_{CC} = 12V	4.0	4.6		W
Total Harmonic Distortion	THD	P_O = 1W/CH		0.2	0.9	%
Voltage Gain (Closed Loop)	AV_1	R_f = 120Ω, V_O = 0.775V	43	45	47	dB
	AV_2	R_f = 0Ω, V_O = 0.775V	54.5	56.5	58.5	dB
Input Resistance	R_i		24	30	36	KΩ
Output Noise Voltage	V_{NO}	R_g = 10KΩ, BW = 20Hz-20KHz		0.3	1.0	mV
Ripple Rejection Ratio	R R	R_g = 600Ω, f = 120Hz	44	52		dB
Cross Talk	C.T	R_g = 10KΩ, V_O = 0dBm, f = 1KHz	40	50		dB
Input Offset Voltage	V_5, V_7			30	60	mv
Stand By Current	I_{sb}	SW1 Off		1	20	μA

TEST AND APPLICATION CIRCUIT

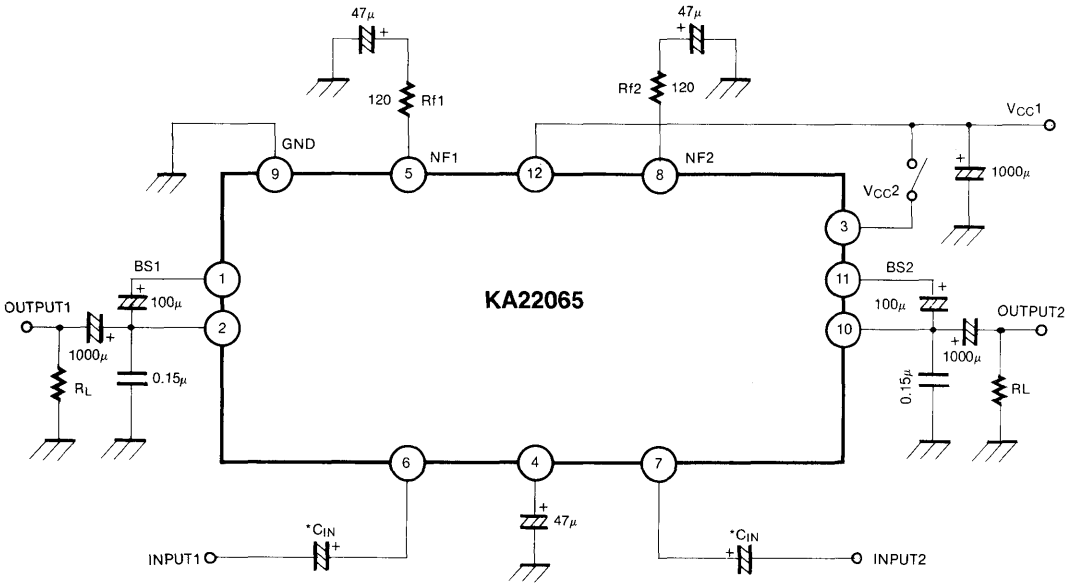
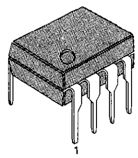


Fig. 2

DUAL LOW VOLTAGE POWER AMPLIFIER

The KA2209 is a monolithic integrated audio amplifier in a 8-pin plastic dual in line package. It is designed for portable cassette players and radios.

8 DIP



FEATURES

- **Wide operating supply voltage: V_{CC}=1.8V ~ 9V**
- **Low crossover distortion**
- **Low quiescent circuit current**
- **Bridge/stereo configuration**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2209	8 DIP	−20 ~ +70°C

BLOCK DIAGRAM

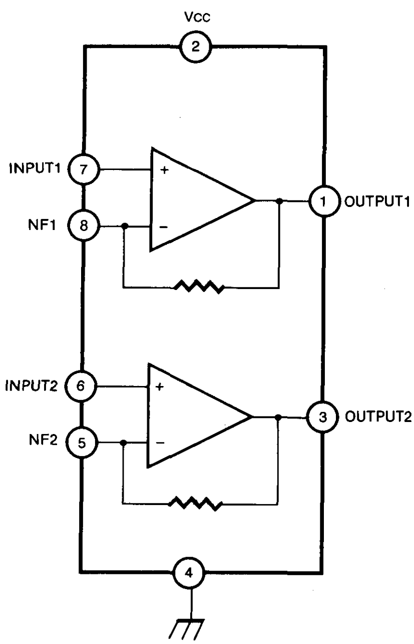


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Output Peak Current	I_O (peak)	1	A
Power Dissipation	P_d	at $T_{amb}=50°C$ 1.0 at $T_{case}=50°C$ 1.4	W
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

($T_a=25°C$, $V_{CC}=6V$, f=1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Operating Supply Voltage	V_{CC}			1.8		9	V
Quiescent Circuit Current	I_{CC}	$V_i=0$			9		mA
Closed Loop Voltage Gain	A_V	Stereo			40		dB
		Bridge			40		dB
Channel Balance	CB	Stereo		−1	0	1	dB
Output Power	P_O	Stereo	$V_{CC}=6V$, $R_L=4\Omega$, THD=10%	0.4	0.65		W
			$V_{CC}=3V$, $R_L=4\Omega$, THD=10%		0.11		W
		Bridge	$V_{CC}=6V$, $R_L=8\Omega$, THD=10%	0.9	1.35		W
			$V_{CC}=3V$, $R_L=4\Omega$, THD=10%		0.35		W
Total Harmonic Distortion	THD	Stereo, $R_L=8\Omega$, $P_O=0.2W$			0.5		%
		Bridge, $R_L=8\Omega$, $P_o=0.5W$			0.5		%
Ripple Rejection	RR	Stereo, f=100Hz, $C_3=100\mu F$		24	30		dB
Output Noise Voltage	V_{NO}	Stereo, BW(−3dB)=20Hz~20KHz			0.5	2.0	mV
Cross Talk	CT	Stereo, f=1KHz			50		dB
Input Resistance	R_i			100			KΩ

TEST CIRCUIT 1: STEREO

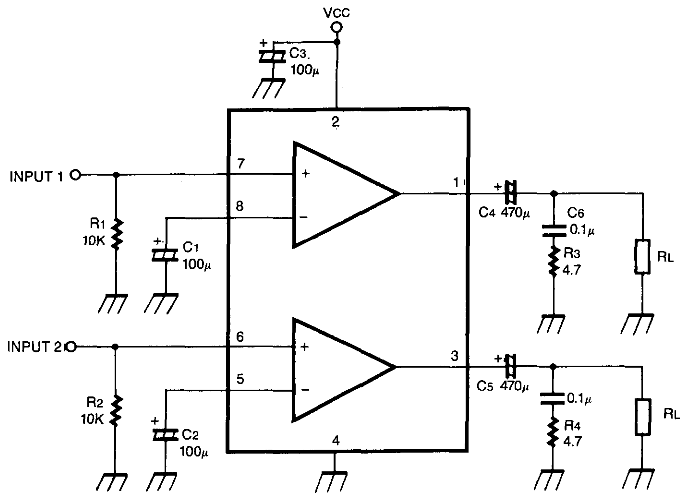


Fig. 2

TEST CIRCUIT 2: BRIDGE

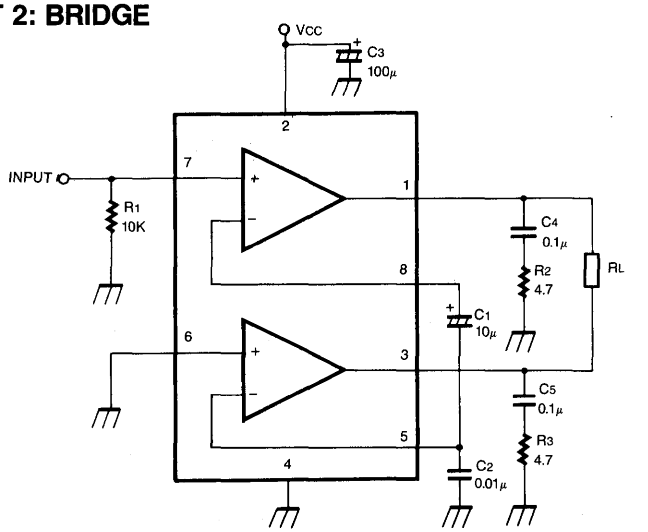
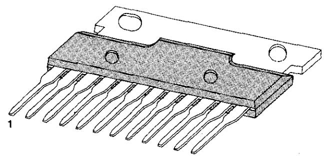


Fig. 3

5.5W DUAL POWER AMPLIFIER

The KA2210 is a monolithic integrated circuit consisting of a 2-channel power amplifier. It is suitable for stereo and bridge amplifier application in car stereos.

12 SIP H/S



FEATURES

- **2-channel amplifier: 5.5W × 2 (Typ).**
- **Minimum number of external parts required.**
- **Small shock noise at the time of power on/off and good starting balance.**
- **High ripple rejection ratio: 46dB (Typ).**
- **Good channel separation.**
- **Small residual noise. (Rg=0)**
- **Include various kinds of protector;**
  Thermal protector.
  Surge and over-voltage protector.
  V_{CC} and output short protector.
- **Connect H/S to GND**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2210	12 SIP H/S	− 20 ~ + 70°C
KA2210G	PELLET	

BLOCK DIAGRAM

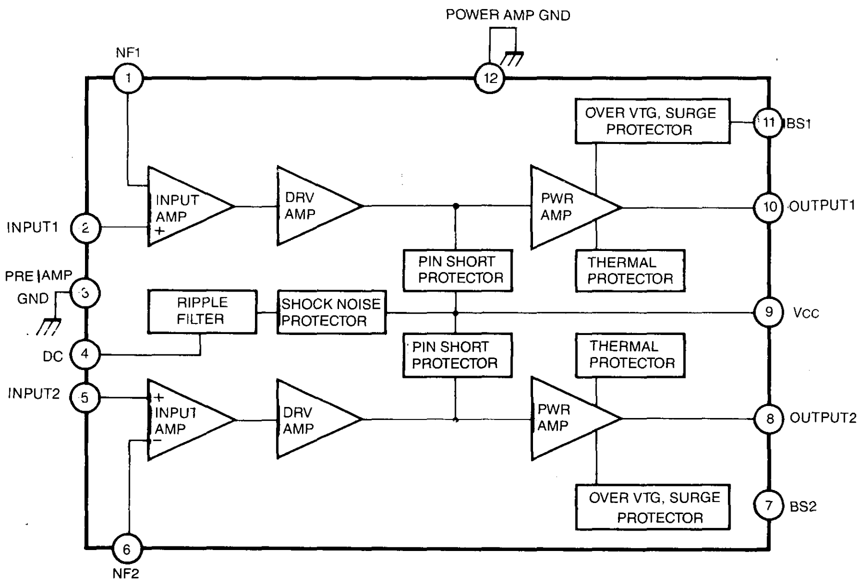


Fig. 1

3

ABSOLUTE MAXIMUM RATINGS ($T_a = 25°C$)

Characteristic	Symbol	Value	Unit
Maximum Supply Voltage (Quiescent)	V_{CC} (max 1)	25	V
Maximum Supply Voltage (with Signal)	V_{CC} (max 2)	18	V
Surge Voltage ($t \leq 0.2$ sec)	V_{CC} (Surge)	50	V
Maximum Output Current (1-Channel)	I_O (peak)	3.5	A
Power Dissipation	P_d (max)	15	W
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

($T_a = 25°C$, $V_{CC} = 13.2V$, $R_L = 4\Omega$, f = 1KHz, $R_g = 600\Omega$, 100×100×1.5mm^3 Al H/S, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Supply Voltage	V_{CC}		10	13.2	16	V
Quiescent Circuit Current	I_{CC}	$V_i = 0$		75	150	mA
Output Power	P_O	THD = 10%, Stereo	5.0	5.5		W
Voltage Gain	A_V	$P_O = 1W$	49.5	51.5	53.5	dB
Total Harmonic Distortion	THD	$P_O = 1W$		0.15	1.0	%
Input Resistance	R_i			30		KΩ
Output Noise Voltage	V_{NO}	$R_g = 0$, BW(−3dB) = 20Hz ~ 20KHz		0.6	1.0	mV
		$R_g = 10K\Omega$, BW(−3dB) = 20Hz ~ 20KHz		1.0	2.0	mV
Ripple Rejection Ratio	RR	$R_g = 0$, $V_r = 200mV$, f = 100Hz		46		dB
Channel Separation	Sep	$R_g = 10K\Omega$, $V_o = 0dBm$	45	55		dB

TYPICAL APPLICATION CIRCUIT: STEREO

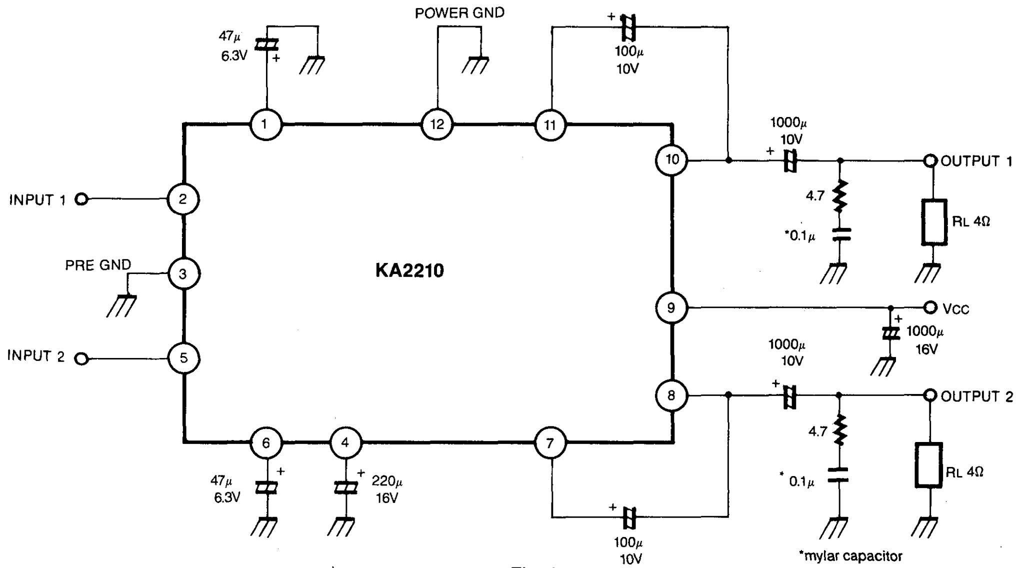


Fig. 2

APPLICATION CIRCUIT: BRIDGE

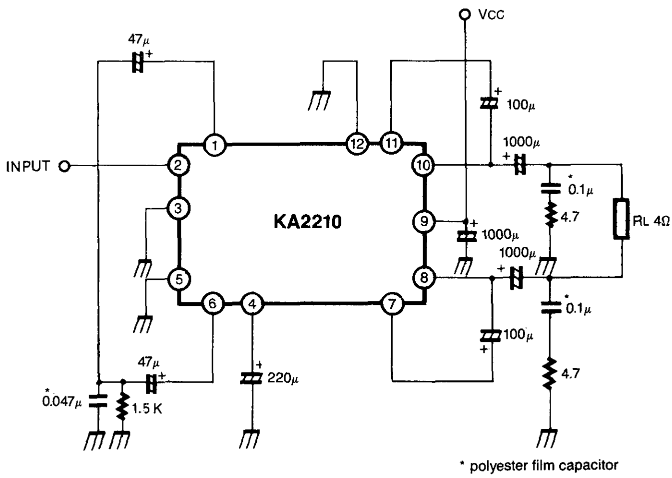
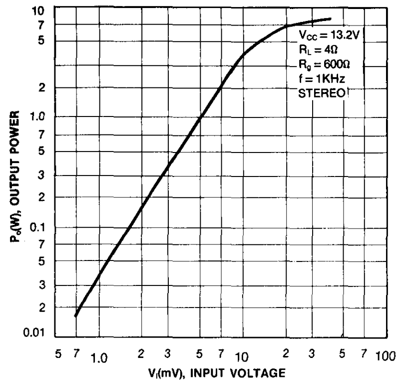
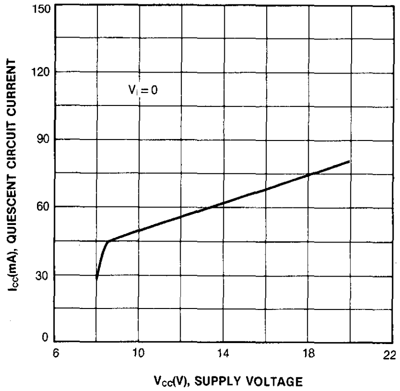


Fig. 3

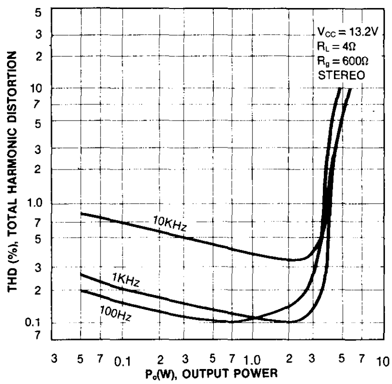
OUTPUT POWER-INPUT VOLTAGE



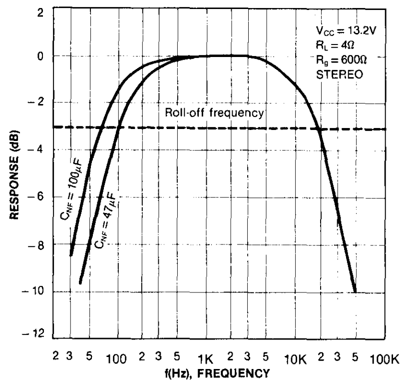
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



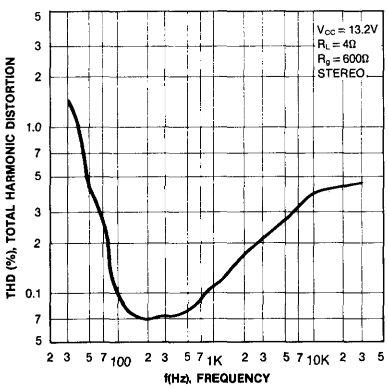
TOTAL HARMONIC DISTORTION-OUTPUT POWER



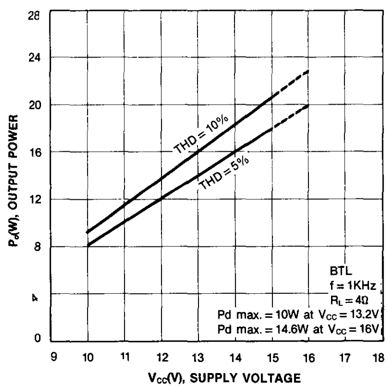
FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION-FREQUENCY

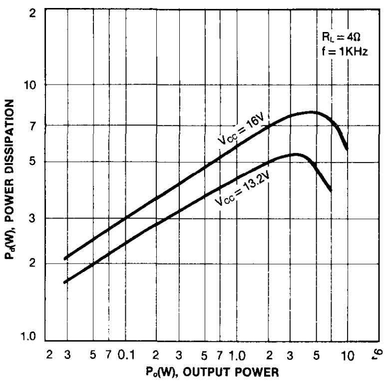


OUTPUT POWER-SUPPLY VOLTAGE

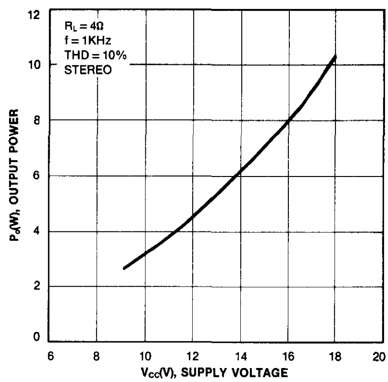


3

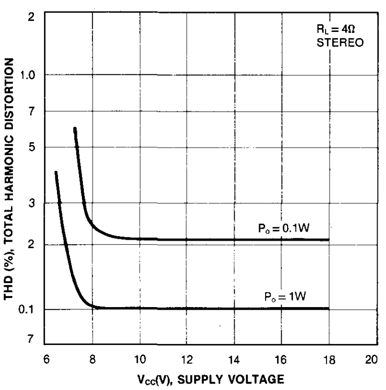
POWER DISSIPATION-OUTPUT POWER



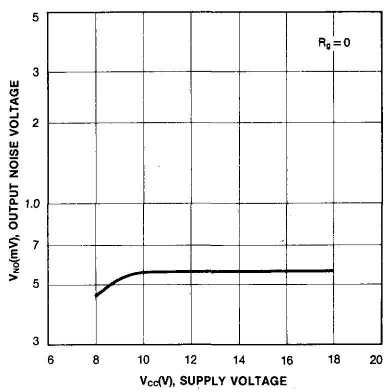
OUTPUT POWER-SUPPLY VOLTAGE



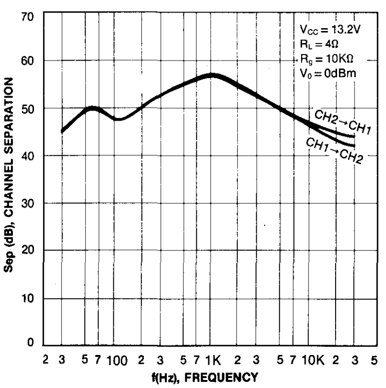
TOTAL HARMONIC DISTORTION-SUPPLY VOLTAGE



OUTPUT NOISE VOLTAGE-SUPPLY VOLTAGE



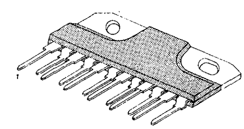
CHANNEL SEPARATION-FREQUENCY



23W POWER AMPLIFIER

The KA22101 is a 23W power amplifier suitable for car audio and it can be used in bridge applications.
It is designed for high power, low distortion and low noise, in step with trends in new hi-fi car stereo systems.
And this device includes various kinds of protection circuit for car.

12 ZIP H/S



FEATURES

- **High Power**
  P_{O1} = 23W (Typ) at V_{CC} = 13.2V, R_L = 4Ω, THD = 10%, f = 1KHz
  P_{O2} = 26W (Typ) at V_{CC} = 13.2V, R_L = 3.2Ω, THD = 10%, f = 1KHz
- **Wide Output Range**
  P_{O3} = 18W (Typ) at V_{CC} = 13.2V, R_L = 4Ω, THD = 1%, f = 50Hz ~ 20KHz
- **Low Distortion**
  THD = 0.015% (Typ) at V_{CC} = 13.2V, f = 1KHz, P_O = 4W, R_L = 4Ω
- **Include various kinds of protection circuit : Temperature, Overvoltage, Output pin to V_{CC} short, Output pin to GND short, Load short protection.**
- **Wide Operating Voltage: V_{CC} = 9V ~ 18V**
- **Connect H/S to GND**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22101	12 ZIP H/S	−20 ~ +70°C

BLOCK DIAGRAM

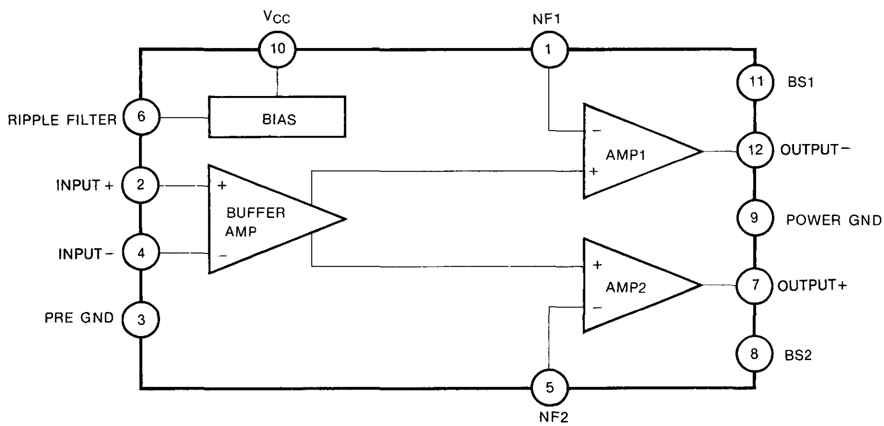


Fig. 1

3

ABSOLUTE MAXIMUM RATINGS ($T_a = 25°C$)

Characteristic	Symbol	Test Condition	Value	Unit
Surge Voltage	V_{CC} (surge)	t = 0.2 sec	50	V
Maximum Supply Voltage	V_{CC} (max. 1)	$V_i = 0$	25	V
Maximum Supply Voltage	V_{CC} (max. 2)	with signal	18	V
Maximum Output Current	I_O (peak)		9	A
Power Dissipation	P_d		25	W
Operating Temperature	T_{opr}		−20 ~ +70	°C
Storage Temperature	T_{stg}		−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

($T_a = 25°C$, $V_{CC} = 13.2V$, $R_L = 4\Omega$, $R_g = 600\Omega$, f = 1KHz, unless otherwise specified)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	$V_i = 0$		120	200	mA
Output Power	P_{O1}	THD = 10%	20	23		W
	P_{O2}	THD = 10%, $R_L = 3.2\Omega$	22	26		W
	P_{O3}	THD = 1%, f = 50Hz ~ 20KHz	15	18		W
Total Harmonic Distortion	THD	$P_O = 4W$		0.015	0.1	%
Voltage Gain	A_V	$V_i = -50dBm$	39.5	41	42.5	dB
Output Noise Voltage	V_{NO1}	$R_g = 0$, DIN45405 (Noise Filter)		0.25		mV
	V_{NO2}	$R_g = 10K\Omega$, BW = 20Hz ~ 20KHz		0.35	0.9	mV
Ripple Rejection Ratio	RR	f = 100Hz, $V_r = 0dBm$	40	47		dB

TEST AND APPLICATION CIRCUIT

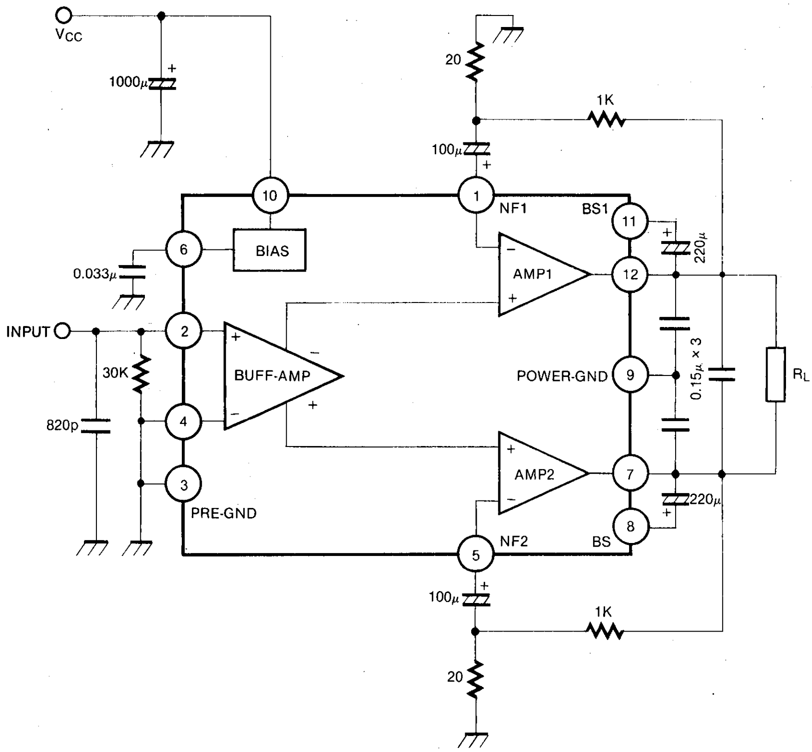


Fig. 2

PIN DC VOLTAGE

(Typical value in the test circuit, V_{CC} = 13.2V, Ta = 25°C)

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12
DC Voltage (V)	1.95	0.01	GND	0	1.95	6.6	6.6	12.5	GND	V_{CC}	12.5	6.6

PRECAUTIONS AND APPLICATION METHODS

1. VOLTAGE GAIN CONTROL

When feedback resistor R_{f1} couples with the external parts, as the temperature characteristic is better than being built into the I.C., and the KA22101 obtains stabilized gain.
If $R_O >> R_{f1} > R_{f2}$, voltage gain (A_V) is

$$A_V = 20 \log \frac{R_{f1}}{R_{f2}} + 6 \text{ (dB) } (R_O = 20K\Omega)$$

Because Pin 12 has the center voltage level of the output and the current I is supplyed with R_{f1} and R_{f2}, it is recommend that R_{f1} and R_{f2} are not use a at values that are too small.

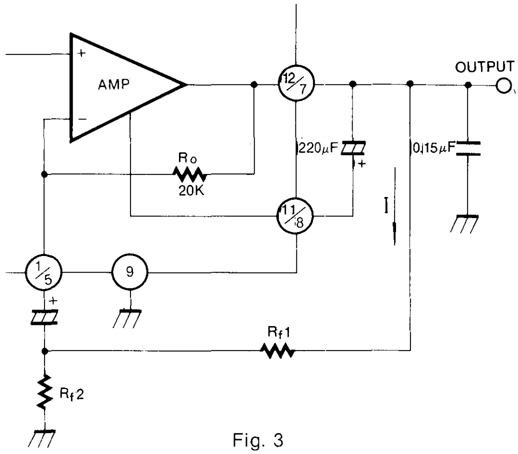


Fig. 3

2. OSCILLATION SUPPRESS

For using a capacitor for getting rid of oscillation between the output and GND or another output, in order to reduce the temperature influence (especially when uses the ceramic capacitor), a polyester film capacitor is recommended. Also, the value of this capacitor must not exceed the recommended value and oscillation margin range (temperature assurance range) should be confirmed through a temperature test.
Especially when an IC is used with the low voltage gain and with the amount of feedback increased, so the phase inverses at a high frequency range and the oscillation is liable to be produced, the value, type and mounting position of the capacitor must be considered before using it above $A_V = 40$dB.

3. ASO CIRCUIT

The IC contains protection circuits of an output-V_{CC} fault, output-GND fault, and output-output fault.

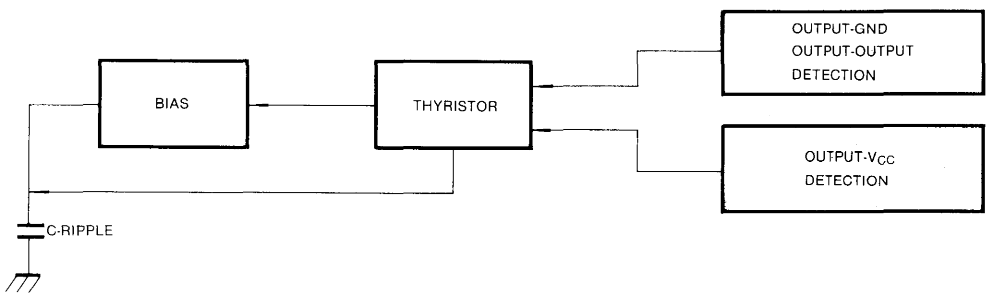


Fig. 4

4. RIPPLE REJECTION

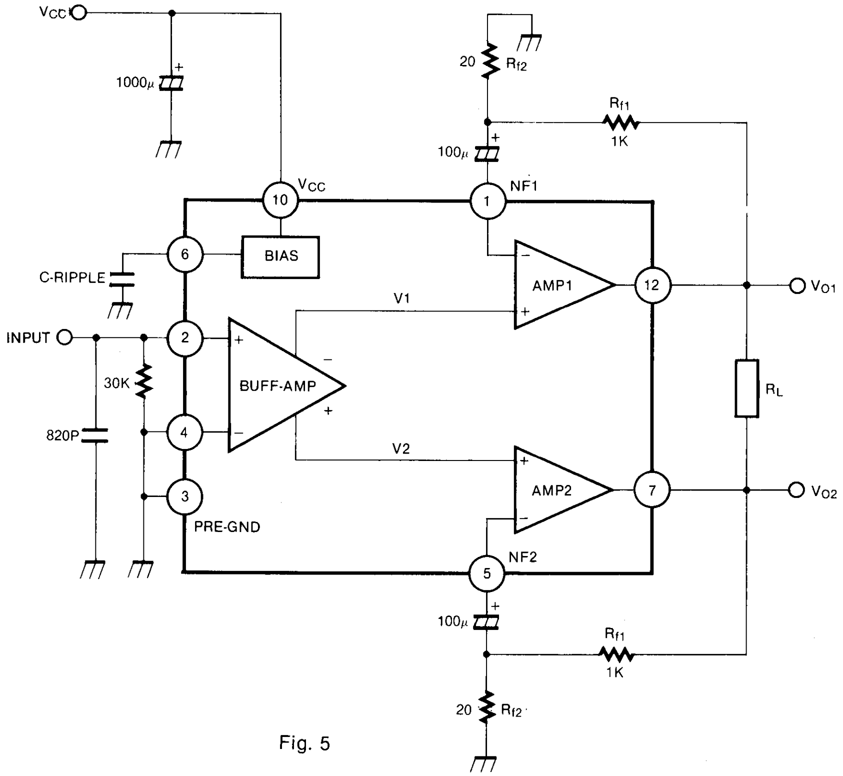


Fig. 5

When the value of the ripple capacitor is small, the following influences are expected:

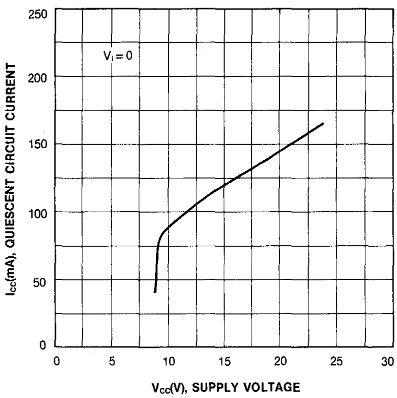
(1) If the C-ripple is small (recommended value = 0.033μF), a ripple figure is produced equal to the output of gain 1 through the phase inversion amp of the primary stage.
This becomes input signal V_1 & V_2 at the power amp stage.

(2) V_1 and V_2 are amplified to V_1 and V_2 at the power stage and $|V_{O1} - V_{O2}|$ appears as output ripple voltage when the BTL is operated.
The characteristics of ripple rejection is determined by:
1. gain dispersion of power stages CH1 and CH2
2. the dispersion between the external feedback resistance (R_{f1}, R_{f2}, $R_{f1'}$, $R_{f2'}$) and the internal resistance.
So, as the pair characteristics (CH1, CH2) of external feedback resistance control the ripple characteristics, it must be used with highly precise resistance which has both characteristics.

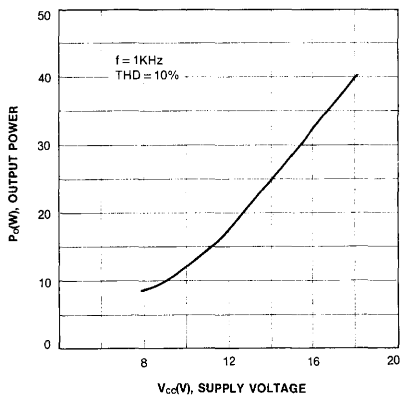
5. CAPACITY OF RIPPLE FILTER

The protector ON/OFF time constant of the KA22101 is determined by the capacity of Pin 6 (ripple fitter).
If the capacity of ripple capacitor increases, the ripple rejection improves, but it is achieved at the risk of two problems:
1. Sound interruption at over-input.
2. Reduction in the protector strength for the short of output-V_{CC}, output-GND, output-output.
So a ripple capacity of 0.033μF is recommended.

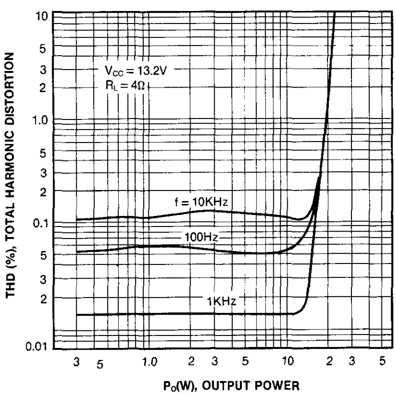
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



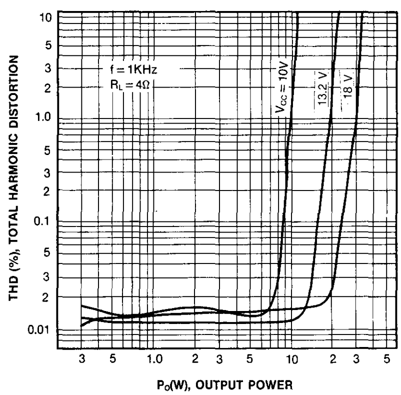
OUTPUT POWER-SUPPLY VOLTAGE



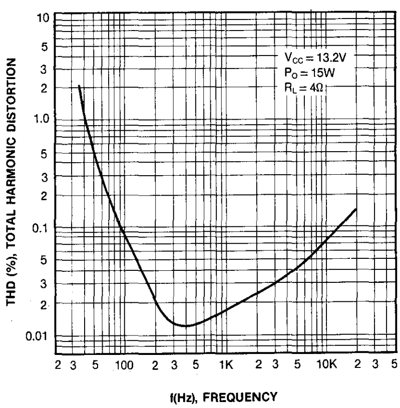
TOTAL HARMONIC DISTORTION-OUTPUT POWER



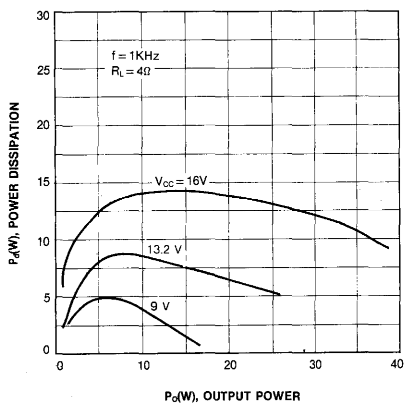
TOTAL HARMONIC DISTORTION-OUTPUT POWER



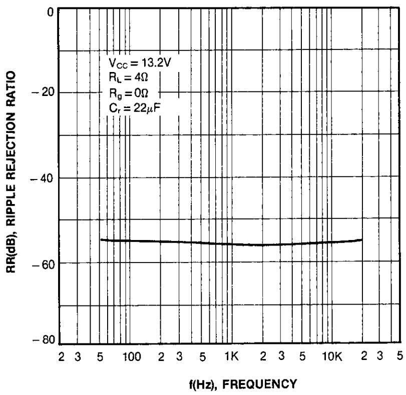
TOTAL HARMONIC DISTORTION-FREQUENCY



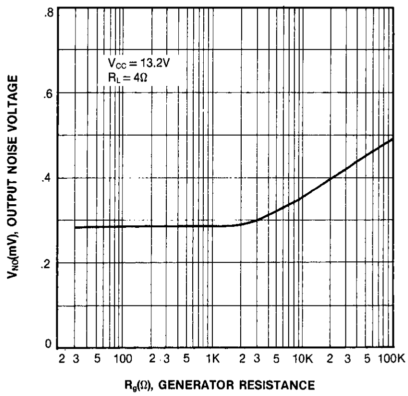
POWER DISSIPATION-OUTPUT POWER



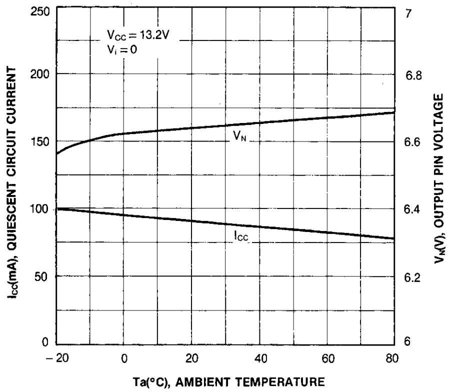
RIPPLE REJECTION RATIO-FREQUENCY



OUTPUT NOISE VOLTAGE-GENERATOR RESISTANCE



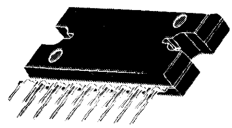
QUIESCENT CIRCUIT CURRENT
OUTPUT PIN VOLTAGE-AMBIENT TEMPERATURE



15W DUAL POWER AMP

The KA22102 is a monolithic integrated circuit consisting of a 2-channel 15W power amplifier for car stereos. It is designed for high power, low distortion and multi functions. Since it uses an excellent 17-pin package, thermal characteristics are good with high performance.

17ZSIP H/S



FEATURES

- High power: 15W/2-Ch
  (V_{CC} = 13.2V, f = 1KHz, THD = 10%, R_L = 4Ω)
- Minimum number of external parts required
- Low distortion: THD = 0.04%
- Low noise: Vno = 0.25mVrms
  (V_{CC} = 13.2V, R_L = 4Ω, R_g = 10KΩ, A_V = 40dB, BW = 20 ~ 20KHz)
- Built-in stand-by and mute function
- Protector: Thermal shut down
  Over voltage protection
  DC short protection with V_{CC}-output and GND
  AC short protection with each output channel
- Operating voltage range: V_{CC} = 9 ~ 18V
- Connect H/S to GND

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22102	17ZSIP H/S	−30 ~ +85°C

BLOCK DIAGRAM

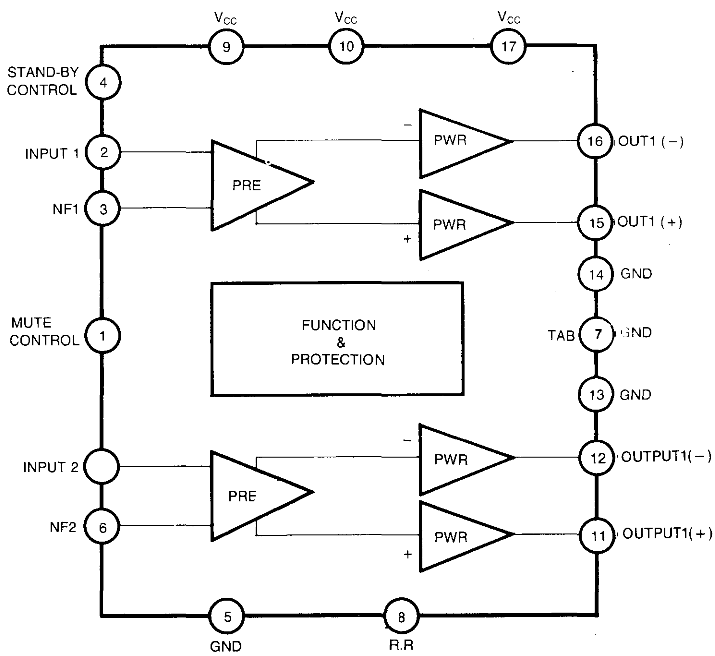


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC} (surge)	50	V
Maximum Supply Voltage	V_{CC} (DC)	25	V
Operating Supply Voltage	V_{CC} (opr)	18	V
Maximum Output Current	I_O (peak)	9	A
Power Dissipation	P_d	50	W
Operating Temperature	T_{opr}	−30 ~ +85	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 13.2V, R_L = 4Ω, f = 1KHz, Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	$V_i = 0$		100	180	mA
Output Power	P_O	THD = 10%	13	15		W
Total Harmonic Distortion	THD	P_O = 1W		0.04	0.3	%
Voltage Gain	A_V	R_f = 470	38	40.5	43	dB
Output Noise Voltage	V_{NO}	R_g = 10KΩ, BPF		0.25	1	mV
Ripple Rejection Ratio	R.R	f_r = 120Hz, R_g = 0	43	50		dB
Input Resistance	R_i			30		KΩ
Output Offset Voltage	V_{offset}	$V_i = 0$	−80	0	+80	mV
Standby Current	I_{sd}	At stand-by		1		μA
Cross Talk	C.T	$R_g = 0$	65	75		dB
Saturation Voltage	VTH(SB)	Pin 4, Po = 1W > 100mW	1.8	2.1	2.4	V
Saturation Voltage	VTH(Mute)	Pin 1, Po = 1W > 100mW	1.4	1.7	3.0	V

TEST AND APPLICATION CIRCUIT

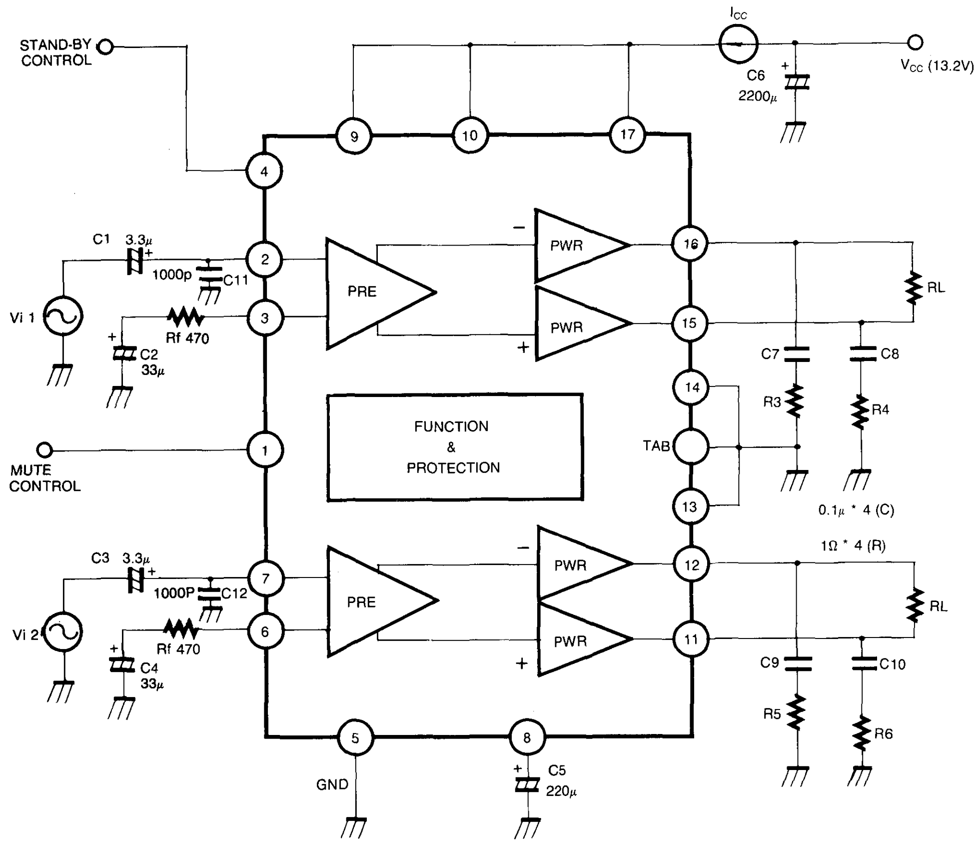


Fig. 2

EXTERNAL COMPONENTS

Parts	Recommended Value	Used for	Condition		Remark
			Small value	Large value	
C1, C3	3.3μF	DC coupling	Reduce the pop noise at V_{CC}-ON		Caution with gain
C2, C4	33μF	Feedback capacitor	Reduce the pop noise at V_{CC}-ON		
			Concerned with the low cut-off frequency $C2 = 1/(6.28 \times f_L \times Rf)$		
C5	220μF	Reduce the ripple			
C7, C8, C9, C10	0.1μF	Compensation osc.	Easy to get oscillation	Increase the compensation	
C6	2200μF	Ripple filter	Used for ripple filter and Hum noise filter		
C11, C12	1000pF	Compensation osc	Reduction of noise increase the compensation		

NOTICES FOR DESIGNING

1. SELECTION OF FEEDBACK RESISTANCE

Since the KA22102 has a built-in pre-amp and power-amp, the amp gain is similar to the following equation.

Pre-amp gain = A_V (PRE)
Power-amp gain = A_V (PWR)
$A_V = A_V (PRE) + A_V (PWR)$

So, that voltage gain in next equation at BTL type.
$A_V \text{ total} = A_V (PRE) + A_V (PWR) + 6$ (dB)

Depending on the internal circuit.
$A_V (PRE) = 20 \log [(3.2K + Rf) / (Rf + 200)]$ (dB)
$A_V (PWR) = 20$ (dB)

So, A_V total is
$A_V \text{ total} = 20 \log [(3.2K + Rf) / (Rf + 200)] + 20$ (dB)

By using the last equation, Rf for total gain can be selected.

2. STAND-BY FUNCTION

It is available with supply voltage ON and OFF by using pin 4.
Because of the small control current, it can use a small capacitance switching relay and it can be controlled by micom directly (except the relay).
Operating voltage of pin 4 is 2.1 V typically and operating supply current is 1 μA typically in stand-by ON mode.

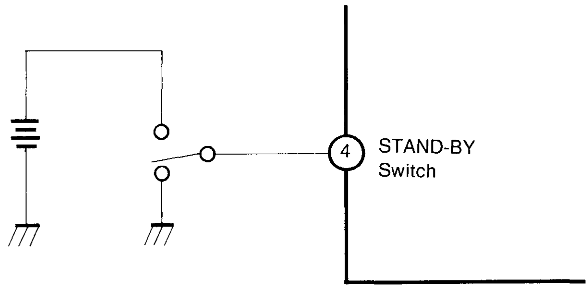


Fig. 3 STAND-BY FUNCTION

3. PREVENTION OF OSCILLATION

The sources of oscillation are listed bellow:

1. Gain of amplifier
2. Capacitance of capacitor
3. Kind of capacitor
4. Location of external components on the printed circuit board

Capacitor C4 for compensation of the OSC must use a polyester film capacitor to get better temperature and frequency variation characteristics.
Especially, if the feedback capacity is higher at low gain; the oscillation at high frequency of audio must be watched.

4. PREVENTION OF INPUT OFFSET AT V_{CC}-ON.

The input pin and negative feedback pin are the same voltage level with each pre-amp at V_{CC}-ON.
The KA22102 presses the offset voltage of the input stage and prevents pop noise of the supply voltage. So, C1 and C2 of the input stage and the NFB capacitor are varied by amp-gain.

<Example> At $A_V = 53.5$ (dB) (Rf = 0)
C1 = 4.7μF, C2 = 47μF.
At $A_V = 40.5$dB (Rf = 470Ω)
C1 = 3.3μF, C2 = 33μF.

5. PROTECTION CIRCUIT

The KA22102 consists of a short protection circuit between the output and GND, output-V_{CC}, output-output (each CH).

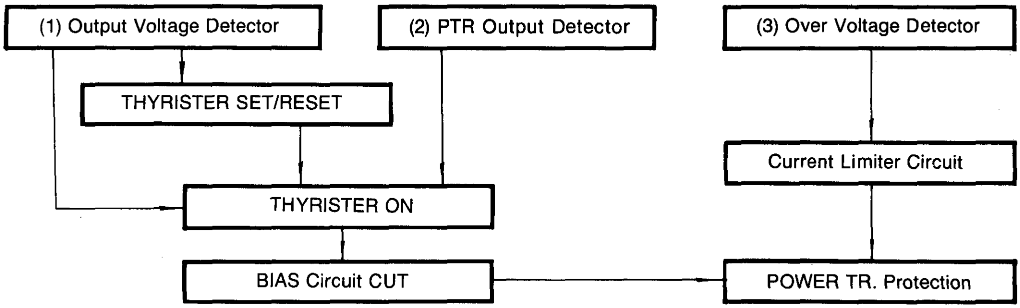


Fig. 4 FLOW CHART OF PROTECTIOIN CIRCUIT

At Fig. 5, the output voltage detector divides the THYRISTER SET with RESET areas and sets on-mode by setting the THYRISTER circuit. When of released because of an output shortage the THYRISTER returns to the reset mode again and KA22102 is returned to the normal mode.

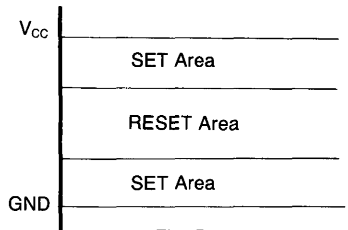


Fig. 5

6. MUTE FUNCTION

Mute is available by setting pin 1 at low level.
In Fig. 6 when the level is low, Q1 and Q2 is in turn-on and the ripple capacitor of Pin 8 is discharged. So, it cuts the bias voltage in the internal circuit. The mute attenuation radio is above 60 dB.

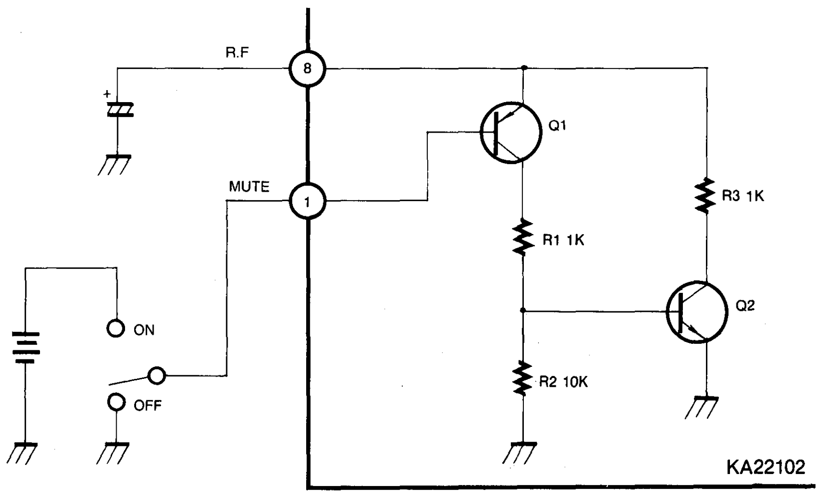
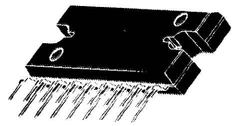


Fig. 6 MUTE Circuit

19W DUAL POWER AMP

The KA22103 is a monolithic integrated circuit consisting of a 2-channel 19W power amplifier for car stereos. It is designed for high power, low distortion and multi functions. Since it uses an excellent 17-pin package, thermal characteristics are good with high performance.

17ZSIP H/S



FEATURES

- **High power: 19W/2-Ch**
  (V_{CC} = 13.2V, f = 1KHz, THD = 10%, R_L = 4Ω)
- **Minimum number of external parts required**
- **Low distortion: THD = 0.04%**
- **Low noise: Vno = 0.25mVrms**
  (V_{CC} = 13.2V, R_L = 4Ω, R_g = 10KΩ, A_V = 40dB, BW = 20Hz ~ 20KHz)
- **Built-in stand-by and mute function**
- **Protector: Thermal shut down**
  Over voltage protection
  DC short protection with V_{CC}-output and GND
  AC short protection with each output channel
- **Operating voltage range: V_{CC} = 9 ~ 18V**
- **Connect H/S to GND**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22103	17ZSIP H/S	− 30 ~ + 85°C

BLOCK DIAGRAM

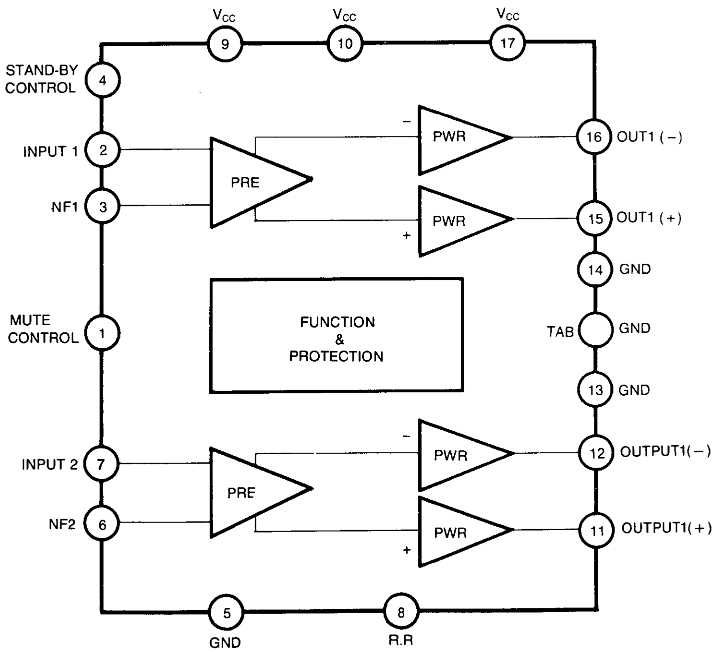


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC} (surge)	50	V
Maximum Supply Voltage	V_{CC} (DC)	25	V
Operating Supply Voltage	V_{CC} (opr)	18	V
Maximum Output Current	I_O (peak)	9	A
Power Dissipation	P_d	50	W
Operating Temperature	T_{opr}	−30 ~ +85	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC}=13.2V, R_L=4Ω, f=1KHz, Ta=25°C)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i=0		100	180	mA
Output Power	Po	THD=10%	16	19		W
Total Harmonic Distortion	THD	Po=1W		0.04	0.3	%
Voltage Gain	Av	R_f=0	48	50	52	dB
Output Noise Voltage	V_{NO}	R_g=10KΩ, BPF		0.25	1	mV
Ripple Rejection Ratio	R.R	f_r=120Hz, R_g=0	43	50		dB
Input Resistance	R_i			30		KΩ
Output Offset Voltage	V_{offset}	V_i=0	−80	0	+80	mV
Standby Current	I_{sd}	At stand-by		1		μA
Cross Talk	C.T	R_g=0	65	75		dB
Saturation Voltage	VTH(SB)	Pin 4, Po=1W>100mW	1.8	2.1	2.4	V
Saturation Voltage	VTH(Mute)	Pin 1, Po=1W>100mW	1.4	1.7	3.0	V

TEST AND APPLICATION CIRCUIT

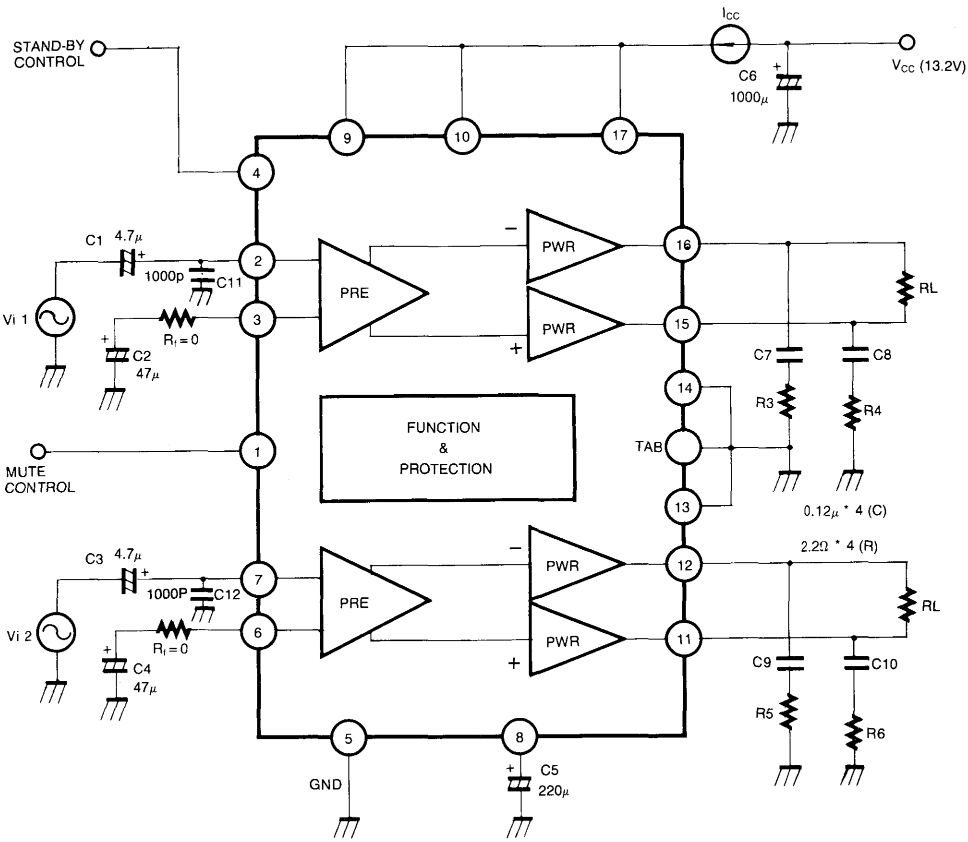


Fig. 2

EXTERNAL COMPONENTS

Parts	Recommended Value	Used for	Condition		Remark
			Small value	Large value	
C1, C3	4.7μF	DC coupling	Reduce the pop noise at V_{CC}-ON		Caution with gain
C2, C4	47μF	Feedback capacitor	Reduce the pop noise at V_{CC}-ON		
			Concerned with the low cut-off frequency $C2 = 1/(6.28 \times f_L \times Rf)$		
C5	220μF	Reduce the ripple			
C7, C8, C9, C10	0.12μF	Compensation osc.	Easy to get oscillation	Increase the compensation	
C6	1000μF	Ripple filter	Used for ripple filter and Hum noise filter		
C11, C12	1000pF	Compensation osc	Reduction of noise increase the compensation		

NOTICES FOR DESIGNING

1. SELECTION OF FEEDBACK RESISTANCE

Since the KA22103 has a built-in pre-amp and power-amp, the amp gain is similar to the following equation.

Pre-amp gain = A_V (PRE)
Power-amp gain = A_V (PWR)
$A_V = A_V (PRE) + A_V (PWR)$

So, that voltage gain in next equation at BTL type.
A_V total $= A_V (PRE) + A_V (PWR) + 6$ (dB)

Depending on the internal circuit.
$A_V (PRE) = 20 \log [(3.2K + Rf) / (Rf + 200)]$ (dB)
$A_V (PWR) = 20$ (dB)

So, A_V total is
A_V total $= 20 \log [(3.2K + Rf) / (Rf + 200)] + 20$ (dB)

By using the last equation, Rf for total gain can be selected.

2. STAND-BY FUNCTION

It is available with supply voltage ON and OFF by using pin 4.
Because of the small control current, it can use a small capacitance switching relay and it can be controlled by micom directly (except the relay).
Operating voltage of pin 4 is 2.1 V typically and operating supply current is 1 μA typically in stand-by ON mode.

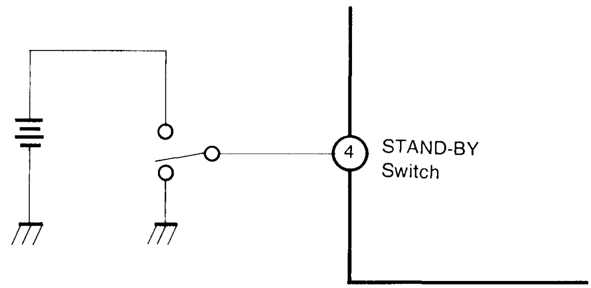


Fig. 3 STAND-BY FUNCTION

3. PREVENTION OF OSCILLATION

The sources of oscillation are listed bellow:
1. Gain of amplifier
2. Capacitance of capacitor
3. Kind of capacitor
4. Location of external components on the printed circuit board

Capacitor C4 for compensation of the OSC must use a polyester film capacitor to get better temperature and frequency variation characteristics.
Especially, if the feedback capacity is higher at low gain; the oscillation at high frequency of audio must be watched.

4. PREVENTION OF INPUT OFFSET AT V_{CC}-ON.

The input pin and negative feedback pin are the same voltage level with each pre-amp at V_{CC}-ON.
The KA22103 presses the offset voltage of the input stage and prevents pop noise of the supply voltage. So, C1 and C2 of the input stage and the NFB capacitor are varied by amp-gain.

<Example> At $A_V = 53.5$ (dB) ($Rf = 0$)
$C1 = 4.7\mu F$, $C2 = 47\mu F$.
At $A_V = 40.5dB$ ($Rf = 470\Omega$)
$C1 = 3.3\mu F$, $C2 = 33\mu F$.

5. PROTECTION CIRCUIT

The KA22103 consists of a short protection circuit between the output and GND, output-V_{CC}, output-output (each CH).

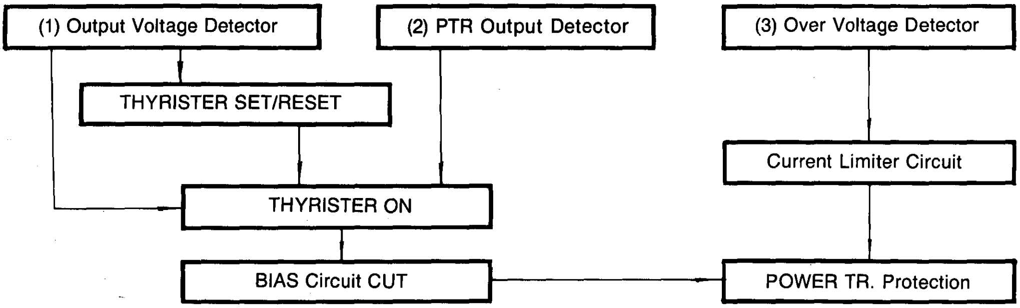


Fig. 4 FLOW CHART OF PROTECTIOIN CIRCUIT

At Fig. 5, the output voltage detector divides the THYRISTER SET with RESET areas and sets on-mode by setting the THYRISTER circuit. When of released because of an output shortage the THYRISTER returns to the reset mode again and KA22103 is returned to the normal mode.

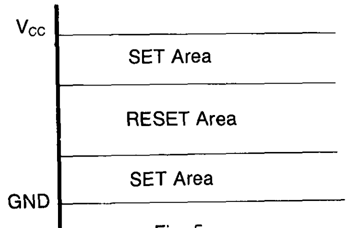


Fig. 5

6. MUTE FUNCTION

Mute is available by setting pin 1 at low level.
In Fig. 6 when the level is low, Q1 and Q2 is in turn-on and the ripple capacitor of Pin 8 is discharged. So, it cuts the bias voltage in the internal circuit. The mute attenuation radio is above 60 dB.

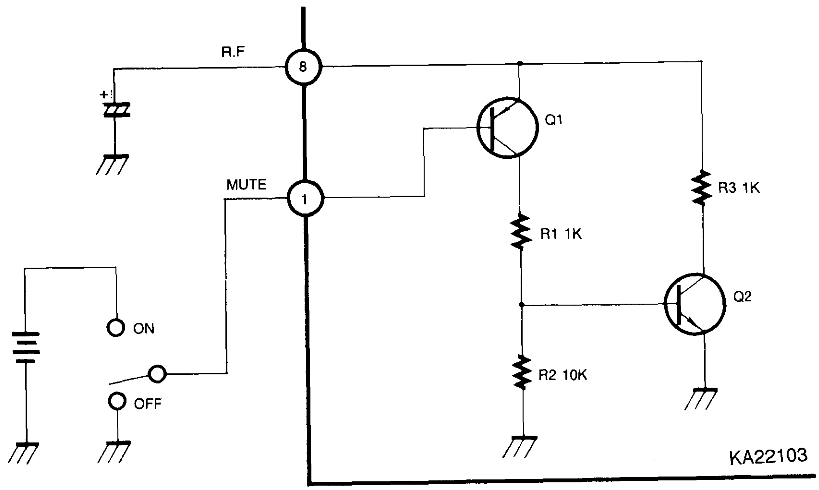
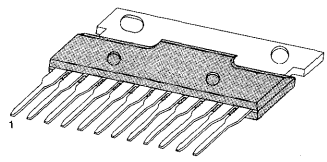


Fig. 6 MUTE Circuit

5.8W DUAL POWER AMPLIFIER

The KA2211 is a dual audio power amplifier for consumer application. It is designed for high power, low dissipation and low noise.
It also contains various kinds of protector. It is suitable for high performance car-audio power amplifiers.

12 SIP H/S



FEATURES

- Operating supply voltage range: $V_{CC}=9V\sim18V$
- High power (Dual)
  $P_o=5.8W$ (Typ) at $V_{CC}=13.2V$, $R_L=4\Omega$, THD = 10%
- Low distortion (Dual)
  THD = 0.06% (Typ) at $V_{CC}=13.2V$, $R_L=4\Omega$, $P_o=1W$, $A_V=52dB$
- Low noise (Dual)
  $V_{NO}=0.7mV$ (Typ) at $V_{CC}=13.2V$, $R_L=4\Omega$, $R_g=10K\Omega$,
  $A_V=52dB$, BW(−3dB) = 20Hz ~ 20KHz
- Protector, thermal shut down
  Over voltage protection
  DC short protection
- Connect H/S to GND

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2211	12 SIP H/S	−20 ~ +70°C

BLOCK DIAGRAM

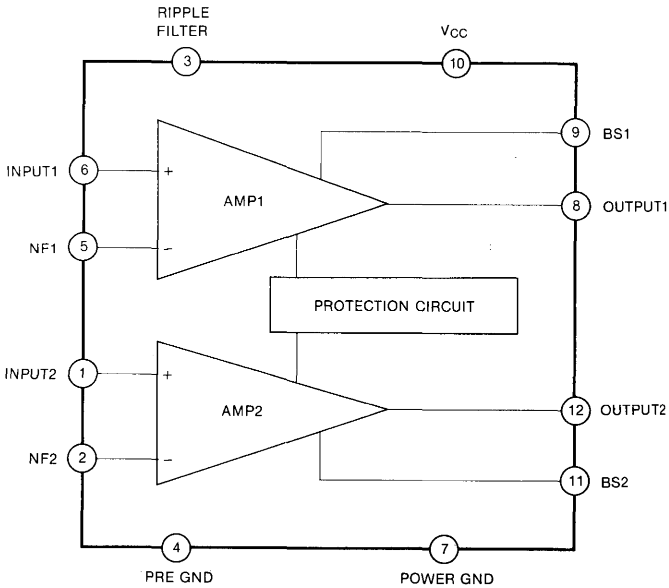


Fig. 1

3

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Condition	Value	Unit
Surge Voltage	V_{CC} (surge)	t = 0.2 sec	45	V
Maximum Supply Voltage	V_{CC} (max 1)	$V_i = 0$	25	V
Maximum Supply Voltage	V_{CC} (max 2)	with signal	18	V
Maximum Output Current	I_o (peak)		3.5	A
Power Dissipation	P_d		15	W
Operating Temperature	T_{opr}		−20 ~ +70	°C
Storage Temperature	T_{stg}		−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

($T_a = 25°C$, $V_{CC} = 13.2V$, $R_L = 4\Omega$, $R_g = 600\Omega$, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	$V_i = 0$		80	145	mA
Output Power	P_o	THD = 10%	5	5.8		W
Total Harmonic Distortion	THD	$P_o = 1W$		0.06	0.3	%
Voltage Gain	A_V	$V_o = 0dBm$	50	52	54	dB
Channel Balance	CB	$V_o = 0dBm$	−1	0	1	dB
Output Noise Voltage	V_{NO}	$R_g = 10K\Omega$, BW(−3dB) = 20Hz ~ 20KHz		0.7	1.5	mV
Ripple Rejection Ratio	RR	f = 120Hz, $V_r = 0dBm$	40	52		dB
Cross Talk	CT	$V_o = 0dBm$		57		dB
Input Resistance	R_i	f = 1KHz		33		KΩ

TEST AND APPLICATION CIRCUIT

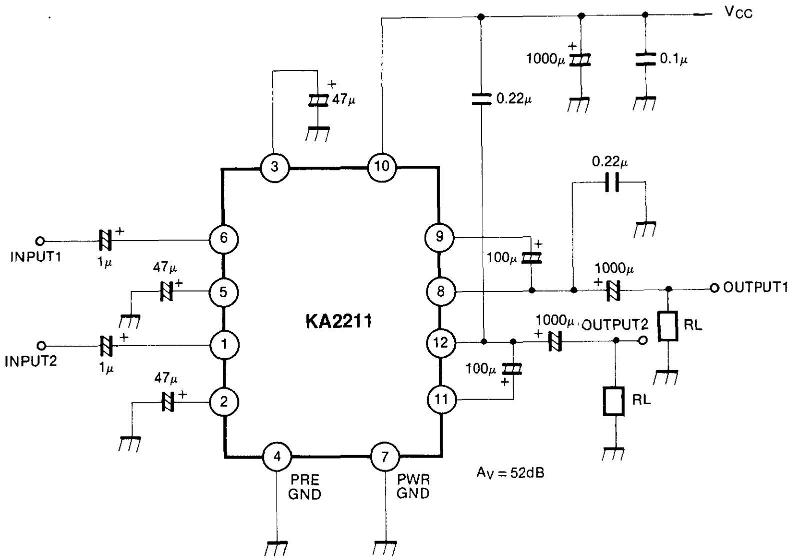
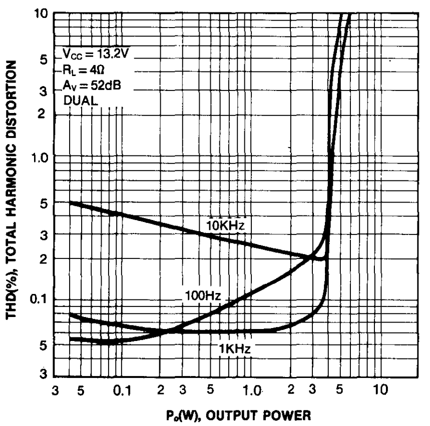
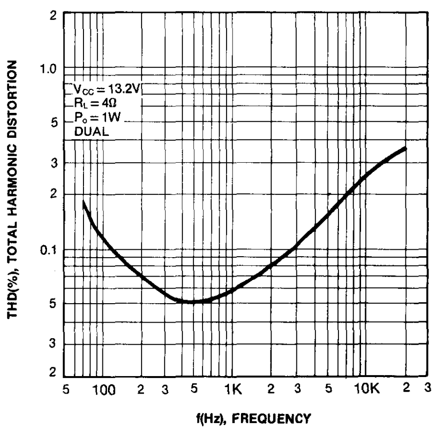


Fig. 2

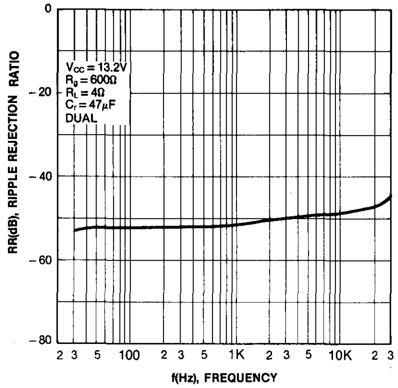
TOTAL HARMONIC DISTORTION-OUTPUT POWER



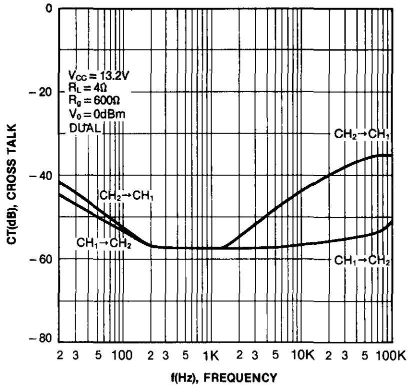
TOTAL HARMONIC DISTORTION-FREQUENCY



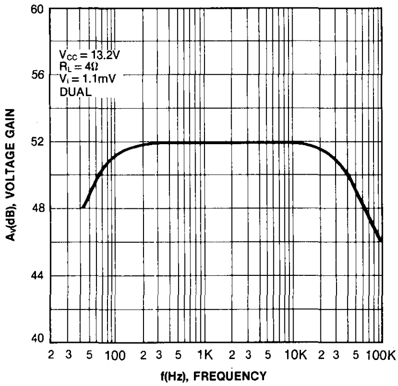
RIPPLE REJECTION RATIO-FREQUENCY



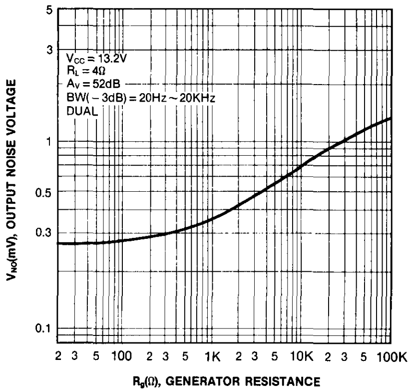
CROSS TALK-FREQUENCY



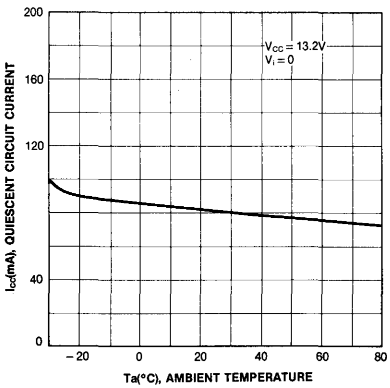
VOLTAGE GAIN-FREQUENCY



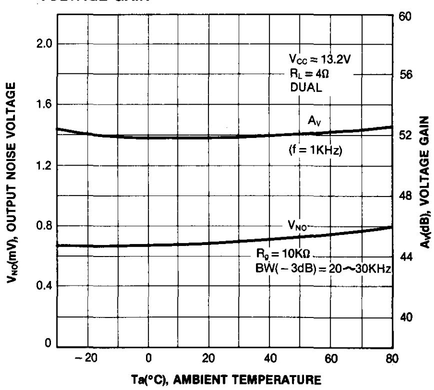
OUTPUT NOISE VOLTAGE-GENERATOR RESISTANCE



QUIESCENT CIRCUIT CURRENT-AMBIENT TEMPERATURE



OUTPUT NOISE VOLTAGE / VOLTAGE GAIN -AMBIENT TEMPERATURE



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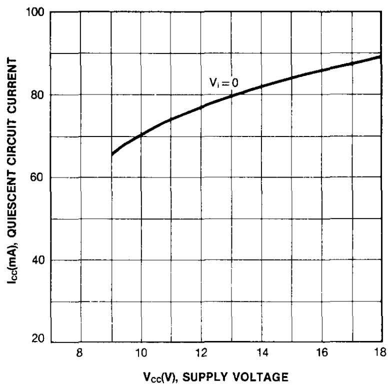
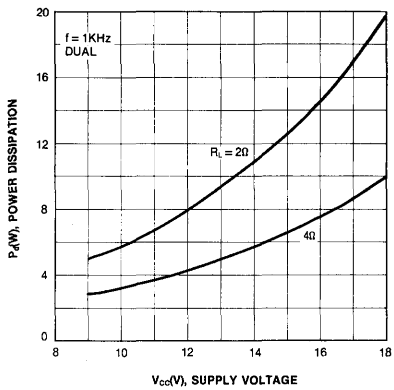
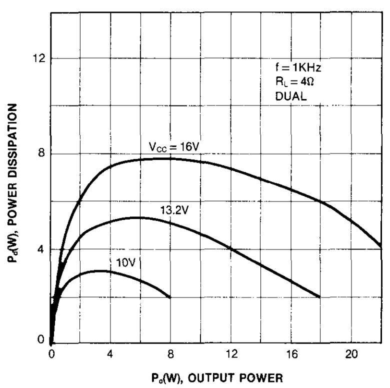
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



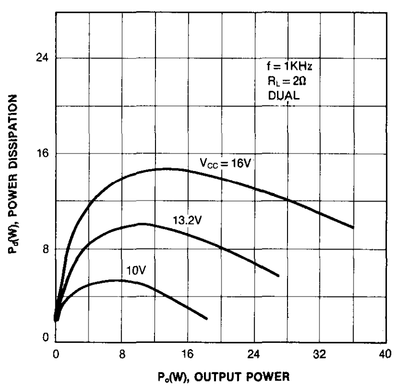
POWER DISSIPATION-SUPPLY VOLTAGE



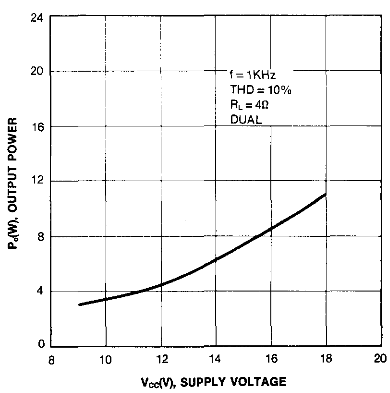
POWER DISSIPATION-OUTPUT POWER



POWER DISSIPATION-OUTPUT POWER



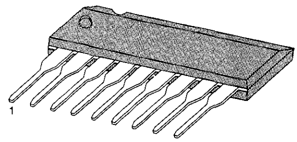
OUTPUT POWER-SUPPLY VOLTAGE



0.5W AUDIO POWER AMPLIFIER

The KA2212 is a monolithic integrated audio power amplifier in a 9-pin plastic single in line package, designed for audio frequency class B amplifiers.

9 SIP



FEATURES

- **Suitable for portable radios, cassette tape recorders.**
- **Medium output power.**
  P_O=0.5W (Typ) at V_{CC}=6V, R_L=8Ω, THD=10%.
- **Wide operating supply voltage range (3.5V ~ 12V).**
- **Low quiescent circuit current.**
- **Excellent thermal stability.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2212	9 SIP	−20 ~ +70°C

SCHEMATIC DIAGRAM

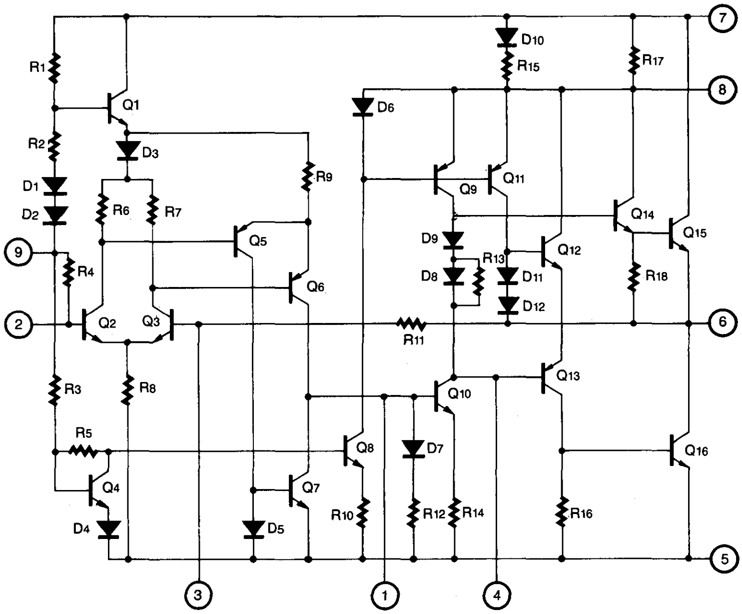


Fig. 1

ABSOLUTE MAXIMUM RATINGS ($T_a = 25°C$)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	14	V
Power Dissipation	P_d	750	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

($T_a = 25°C$, $V_{CC} = 6V$, $R_L = 8\Omega$, $R_g = 600\Omega$, $Rf = 68\Omega$, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	$V_i = 0$		14		mA
Voltage Gain (Open Loop)	A_{VO}	$R_f = 0\Omega$	60	75		dB
Voltage Gain (Closed Loop)	A_V	$R_f = 68\Omega$	47	50	52	dB
Output Power	P_O	THD=10%	0.45	0.5		W
Total Harmonic Distortion	THD	P_O =100mW		0.3	1.0	%
Input Resistance	R_i			15		KΩ
Output Noise Voltage	V_{NO}	$R_g = 10K\Omega$ BW (−3dB)=50Hz ~ 20KHz		0.4	1.0	mV

TEST CIRCUIT

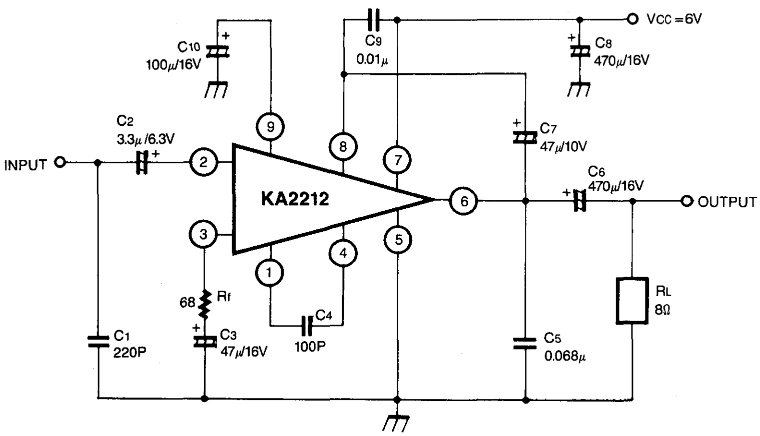
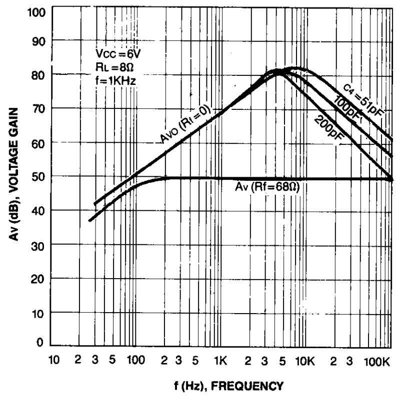
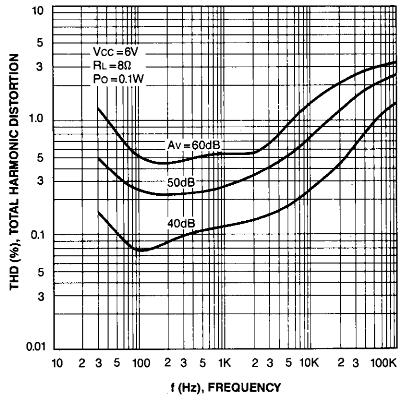


Fig. 2

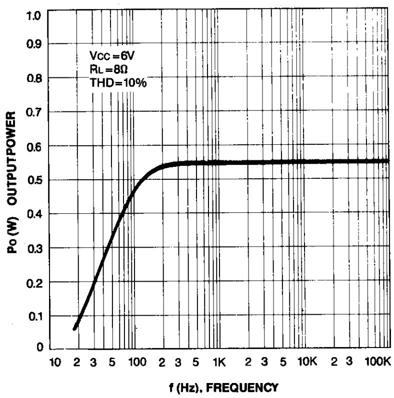
VOLTAGE GAIN-FREQUENCY



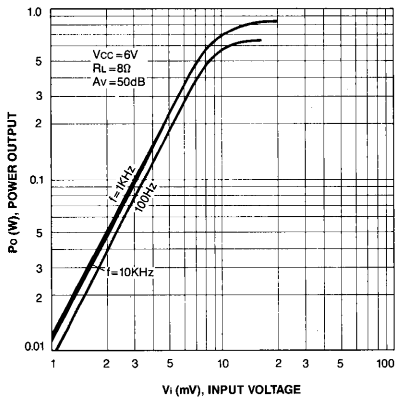
TOTAL HARMONIC DISTORTION-FREQUENCY



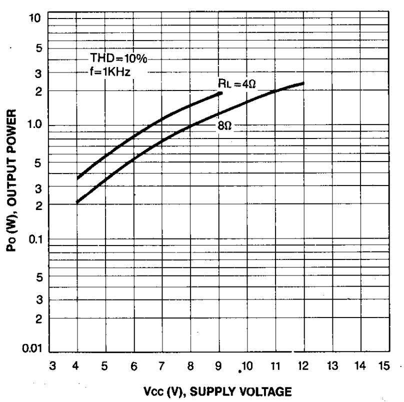
OUTPUT POWER-FREQUENCY



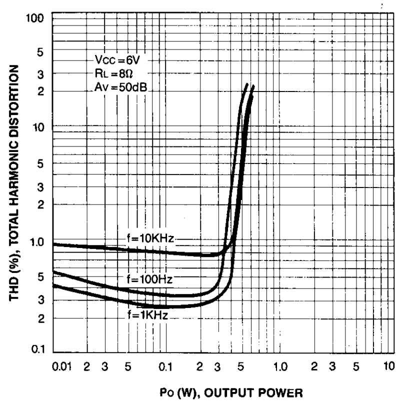
OUTPUT POWER-INPUT VOLTAGE



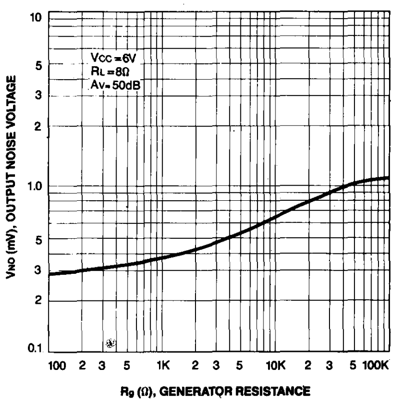
OUTPUT POWER-SUPPLY VOLTAGE



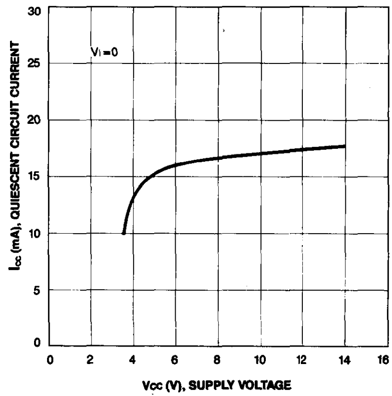
TOTAL HARMONIC DISTORTION-OUTPUT POWER



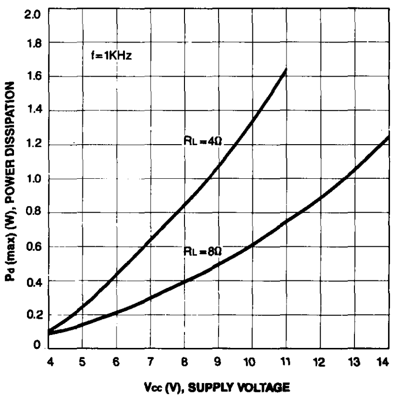
OUTPUT NOISE VOLTAGE-GENERATOR RESISTANCE



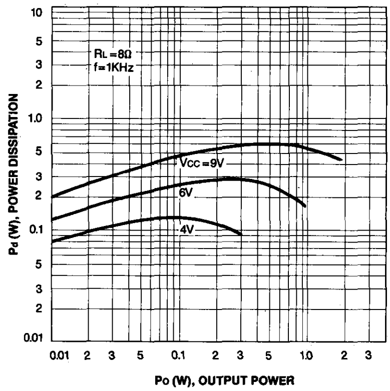
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



POWER DISSIPATION-SUPPLY VOLTAGE



POWER DISSIPATION-OUTPUT POWER



External Components (Refer to test circuits)

C_1: Noise filter

C_2: Input coupling capacitor
The recommended value for this capacitor is 3.3μF.
If made too small, the low frequency characteristic changes for the worse. Too large a capacitance value will increase the rise time when power is applied and may generate noise due to the charging current when the volume control is adjusted.

R_f, C_3: Feedback components
The variation of the closed loop gain depends on the components which are determined as follows:

$$C_3 = \frac{1}{2\pi f_L \cdot R_f} \qquad A_V = 20 \log \frac{20000}{R_f} \text{ (dB)}$$

Where f_L: low cut-off frequency
A_v: closed loop gain

C_4: Compensation capacitor
The high cut-off frequency is determined by C_4, which helps to suppress the oscillatioin in the higher frequency ranges.

C_5, C_9: Oscillation supression capacitors
The mylar capacitor is be used for C_5 to get a better characteristic for temperature and frequency.

C_6: Output coupling capacitor
It decides the output power level of low frequency.

C_7: Boostrap capacitor
For low value reduced rated output power and increased distortion at low frequency.

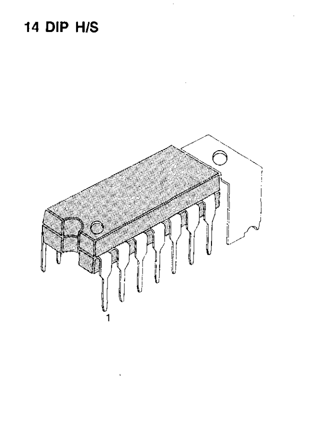
C_8: Ripple filter for power supply
The large value is required to get an excellent ripple characteristic under the line operation, but the small models can be used with a battery.

C_{10}: Filter capacitor
Rejects power line hum.

3

ONE-CHIP TAPE RECORDER SYSTEM

The KA2213 is a monolithic integrated circuit consisting of a preamplifier, ALC circuit, power amplifier in a 14-pin plastic dual in line package with heat sink.



FEATURES

- Suitable for the play and recording functions of mono cassette tape recorders.
- **Wide operating supply voltage range (4V~12V).**
- **High gain preamplifier and power amplifier.**
- **Output power of power amplifier state P_O=1W at V_{CC}=6V, R_L=4Ω, THD=10%.**
- **Soft tone quality at the time of output saturation.**
- **Wide ALC range and small variation in output voltage.**
- **Small shock noise at the time of power on/off due to built-in prevention circuit.**
- **Variable monitor capability due to recording amplifier consisting of preamplifier alone.**
- **Minimum number of external parts required.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2213	14 DIP H/S	−20 ~ +70°C
KA2213G	PELLET	

BLOCK DIAGRAM

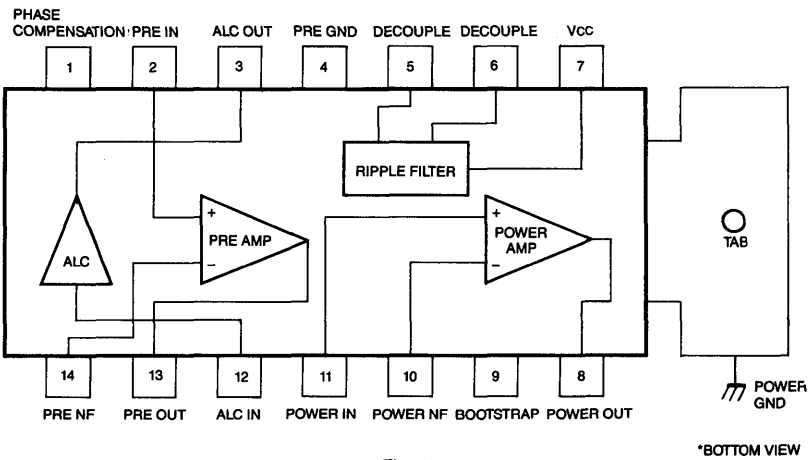


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	13	V
Power Dissipation	P_d	1.2 2.25*	W W
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +150	°C

* Mounted and soldered on a 50mm × 50mm copper foil of PCB

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 6V, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_{CC} = 6V, V_i = 0		18	30	mA
		V_{CC} = 9V, V_i = 0		23	40	mA
Pre-amplifier						
Voltage Gain (Open Loop)	A_{VO}	Open loop		85		dB
Voltage Gain (Closed Loop)	A_V	Closed loop, Play		40		dB
Output Voltage	V_O	THD=1%, Play	0.9	1.2		V
Input Resistance	R_i		21	30		KΩ
Equivalent Input Noise Voltage	V_{NI}	Play		1.0	2.0	μV
ALC Input Level	ALC	THD = 1%, Rec	−20	−12		dBm
Power Amplifier						
Voltage Gain (Closed Loop)	A_V	R_f=51Ω	43	45	47	dB
Output Power	P_O	V_{CC}=6V, R_L=4Ω, THD=10%	0.7	1.0		W
		V_{CC}=7.5V, R_L=4Ω, THD=10%	1.0	1.5		W
		V_{CC}=9V, R_L=4Ω, THD=10%	1.7	2.2		W
Total Harmonic Distortion	THD	P_O=250mW		0.3	1.5	%
Input Resistance	R_i			30		KΩ
Output Noise Voltage	V_{NO}	R_g=10KΩ		0.6	1.8	mV
Ripple Rejection	RR	R_g=0Ω, V_r=150mV, f=100Hz	40	45		dB

3

TEST CIRCUIT

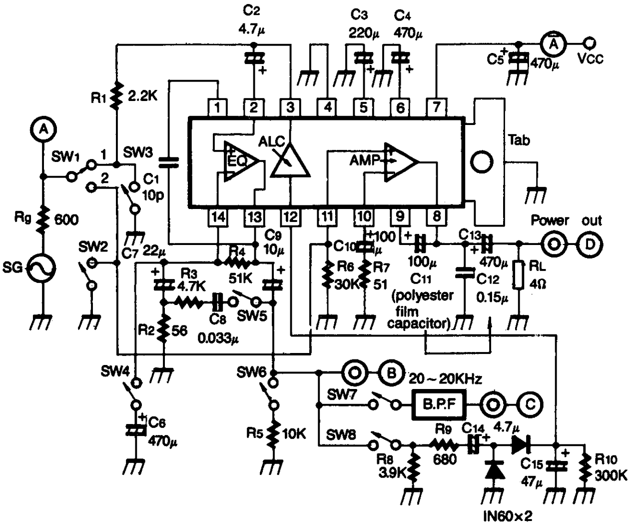


Fig. 2

TEST CONDITION

	Characteristic	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Test Point	Test Method
Power Amplifier	I_{CC}		on	on	off	on	on	off	off		Test circuit current
	A_V	2	off	off	off	on	on	off	off	A.D	$A_V = 20 \log V_O/V_i$ (dB)
	P_O	2	off	off	off	on	on	off	off	D	Test output voltage at THD = 10%
	THD	2	off	off	off	on	on	off	off	D	Test THD at output voltage $V_O = 1V$
	V_{NO}		on	off	off	on	on	off	off	D	Test output noise voltage
	RR		on	off	off	on	on	off	off	D	RR = 20 log V_{ro}/150 (dB) Test output ripple voltage (V_{ro})
Pre-amplifier	A_{VO}	1	off	off	on	off	on	off	off	A.B	$A_{VO} = 20 \log V_O/V_i$ (dB)
	V_O	1	off	off	off	on	on	off	off	B	Test output voltage at THD = 1%
	V_{NI}		off	on	off	on	on	on	off	C	Convert output noise voltage at R_g = 2.2KΩ, $V_{NI} = V_{NO}/A_V$
	ALC Input level	1	off	off	off	off	off	off	on	A.B	Test input voltage at THD = 1%

TYPICAL APPLICATION CIRCUITS

1. Mono cassette tape recorder

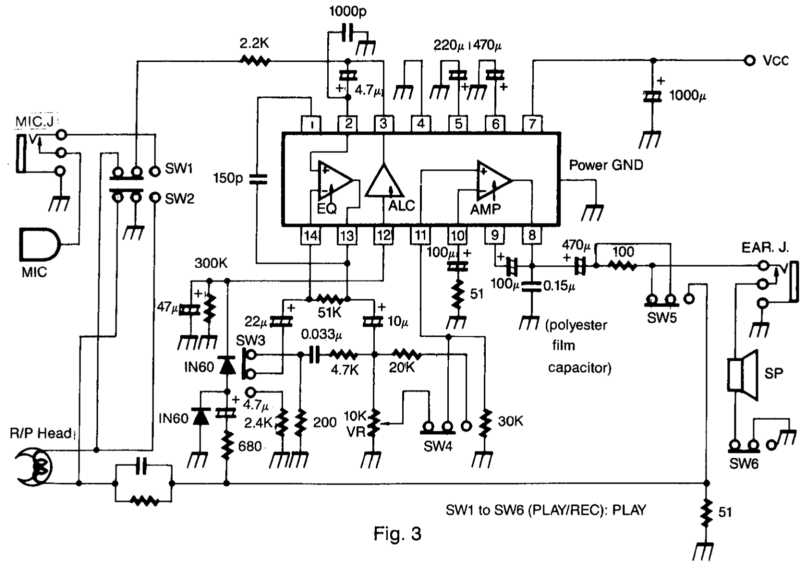


Fig. 3

2. Radio cassette tape recorder

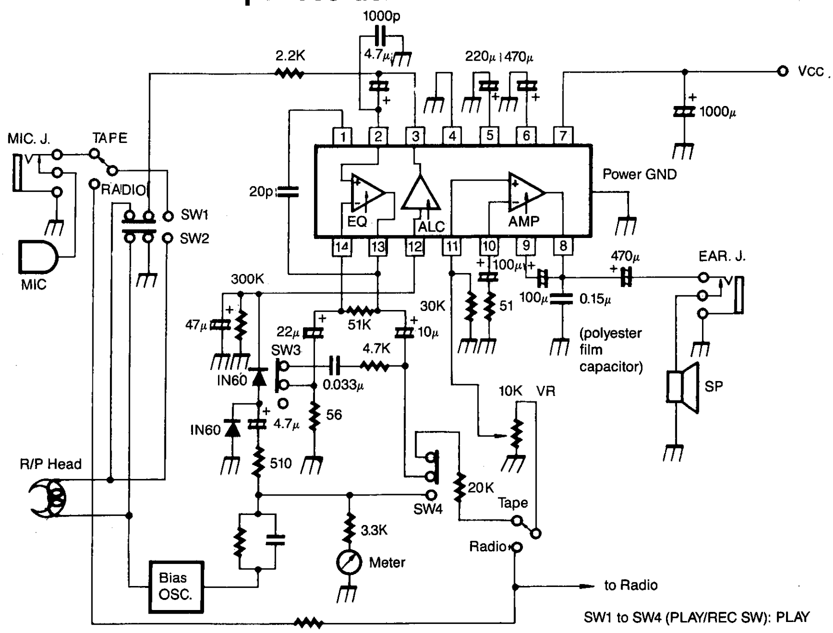
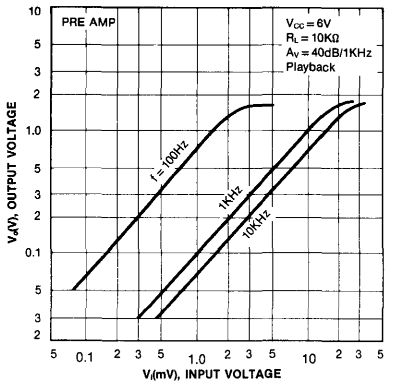
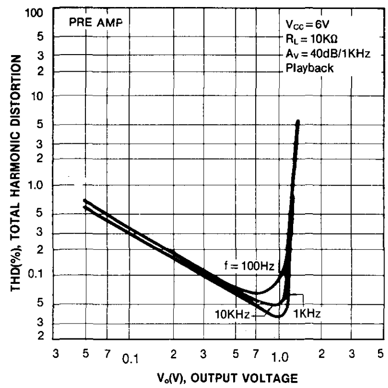


Fig. 4

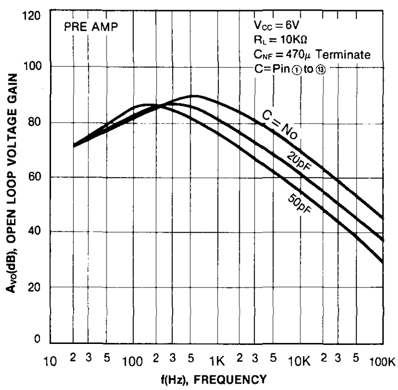
OUTPUT VOLTAGE-INPUT VOLTAGE



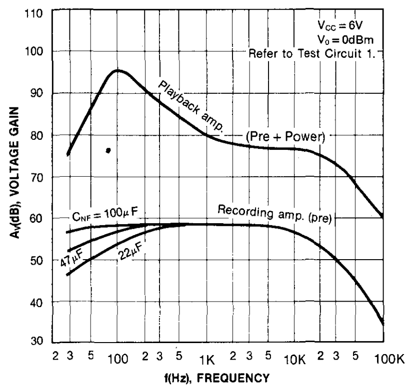
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



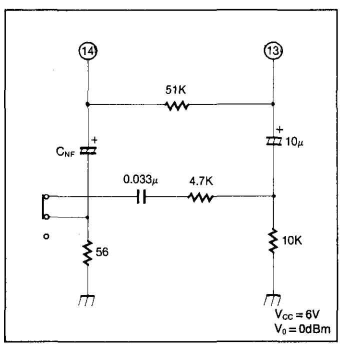
OPEN LOOP VOLTAGE GAIN-FREQUENCY



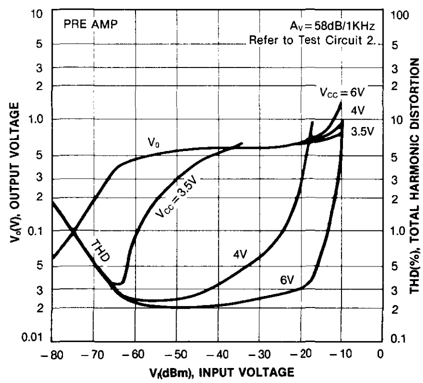
VOLTAGE GAIN-FREQUENCY



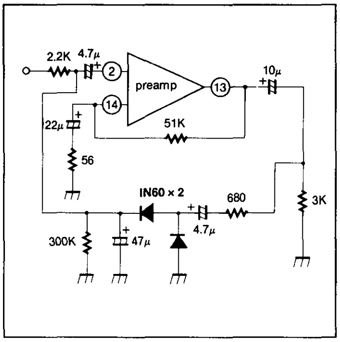
TEST CIRCUIT 1



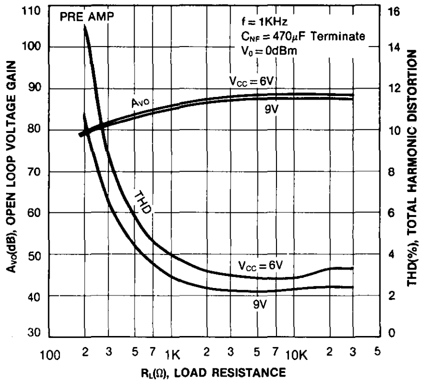
OUTPUT VOLTAGE · TOTAL HARMONIC DISTORTION - INPUT VOLTAGE



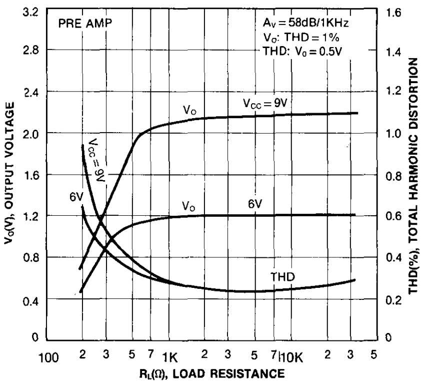
TEST CIRCUIT 2



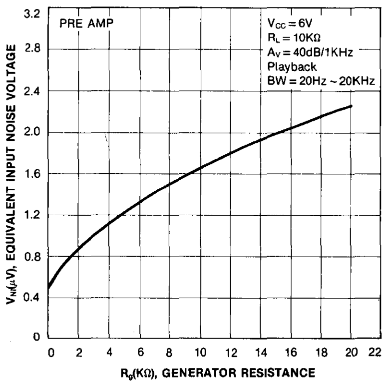
VOLTAGE GAIN / TOTAL HARMONIC DISTORTION ·LOAD RESISTANCE



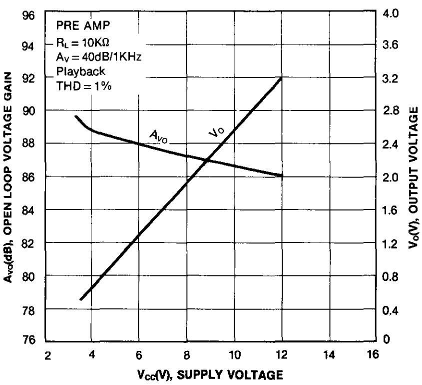
OUTPUT VOLTAGE / TOTAL HARMONIC DISTORTION ·LOAD RESISTANCE



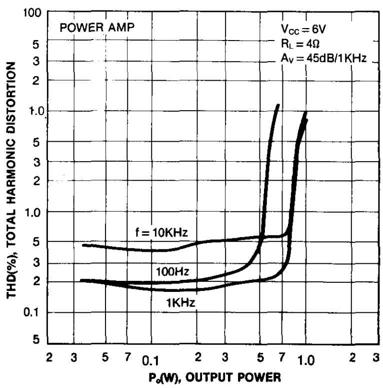
EQUIVALENT INPUT NOISE VOLTAGE ·GENERATOR RESISTANCE



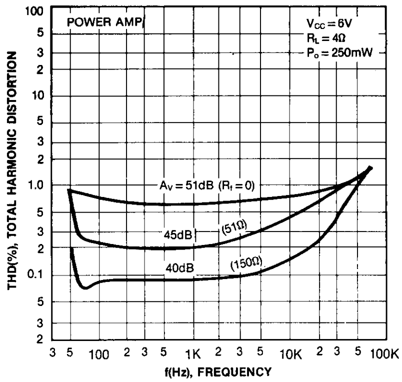
OPEN LOOP VOLTAGE GAIN / OUTPUT VOLTAGE ·SUPPLY VOLTAGE



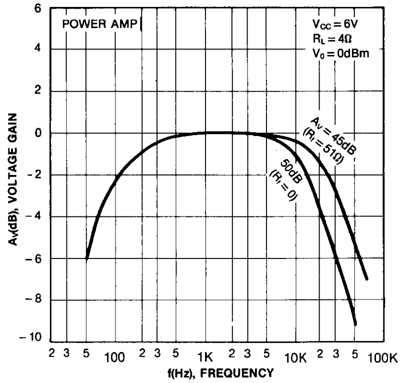
TOTAL HARMONIC DISTORTION·OUTPUT POWER



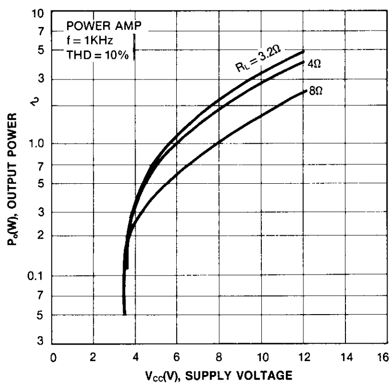
TOTAL HARMONIC DISTORTION-FREQUENCY



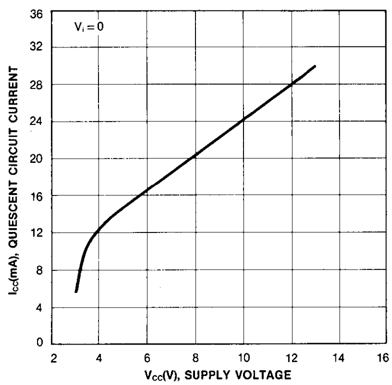
VOLTAGE GAIN-FREQUENCY



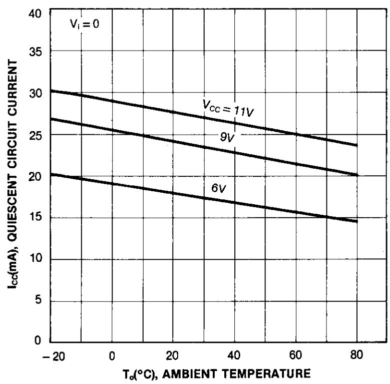
OUTPUT POWER-SUPPLY VOLTAGE



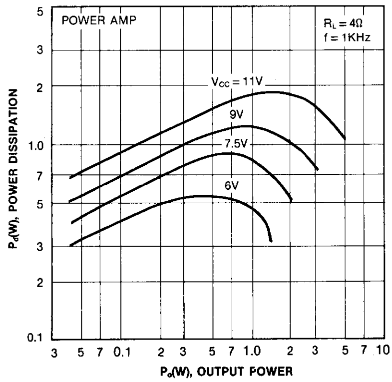
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



QUIESCENT CIRCUIT CURRENT-AMBIENT TEMPERATURE

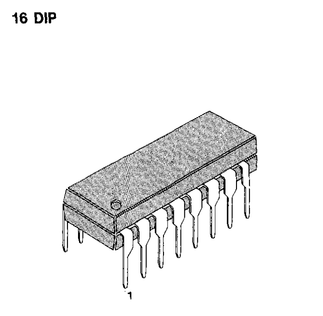


POWER DISSIPATION-OUTPUT POWER



ONE CHIP TAPE RECORDER SYSTEM

The KA22130 is a monolithic integrated circuit consisting of preamplifier, ALC circuit, power amplifier in 16 pin plastic dual in line package.



FEATURES

- **Suitable for play and recording mono cassette tape recorder.**
- **Wide operating supply voltage range (4V ~ 12V).**
- **High gain preamplifier and power amplifier.**
- **Output power of power amplifier state P_O =1W at V_{CC} =6V, R_L =4Ω, THD= 10%.**
- **Soft tone quality at the time of output saturation.**
- **Wide ALC range and small variation in output voltage.**
- **Small shock noise at the time of power on/off due to built-in prevention circuit.**
- **Variable monitor capability due to recording amplifier consisting of preamplifier alone.**
- **Minimum number of external parts required.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22130	16 DIP	−20 ~ +70°C

BLOCK DIAGRAM

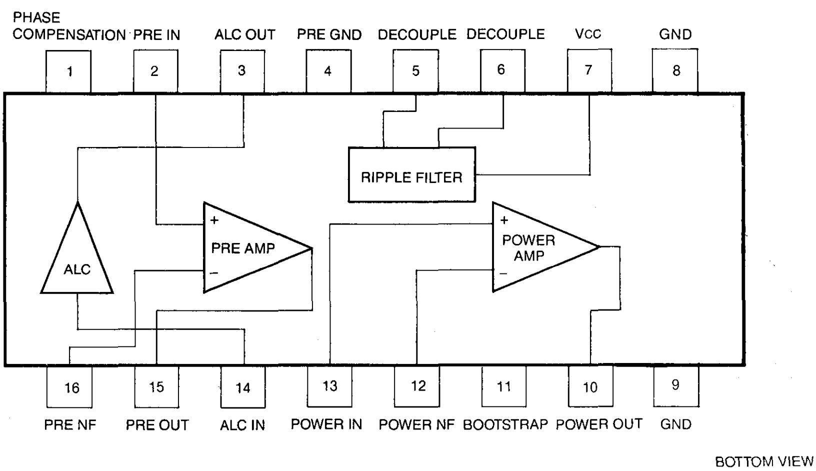


Fig. 1

3

ABSOLUTE MAXIMUM RATINGS ($T_a = 25°C$)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	13	V
Power Dissipation	P_d	1.5	W
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−40 ~ +150	°C

ELECTRICAL CHARACTERISTIC

($T_a = 25°C$, $V_{CC} = 6V$, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	$V_{CC} = 6V$, $V_i = 0$		18	30	mA
		$V_{CC} = 9V$, $V_i = 0$		23	40	mA
Pre-amplifier						
Voltage Gain (Open Loop)	A_{VO}	Open loop		85		dB
Voltage Gain (Closed Loop)	A_V	Closed loop, Plan		40		dB
Output Voltage	V_O	THD = 1%, Play	0.9	1.2		V
Input Resistance	R_i		21	30		KΩ
Equivalent Input Noise Voltag.	V_{NI}	Play		1.0	2.0	μV
ALC Input Level	ALC	THD = 1%, Play	−20	−12		dBm
Power Amplifier						
Voltage Gain (Closed Loop)	A_V	$R_f = 51Ω$	43	45	47	dB
Output Power	P_O	$V_{CC} = 6V$, $R_L = 4Ω$, THD = 10%	0.7	1.0		W
		$V_{CC} = 7.5V$, $R_L = 4Ω$, THD = 10%	1.0	1.5		W
		$V_{CC} = 9V$, $R_L = 4Ω$, THD = 10%	1.7	2.2		W
Total Harmonic Distortion	THD	$P_O = 250mW$		0.3	1.5	%
Input Resistance	R_i			30		KΩ
Output Noise Voltage	V_{NO}	$R_g = 10KΩ$		0.6	1.8	mV
Ripple Rejection	RR	$R_g = 0Ω$, $V_r = 150mV$, f = 100Hz	40	45		dB

TEST CIRCUIT

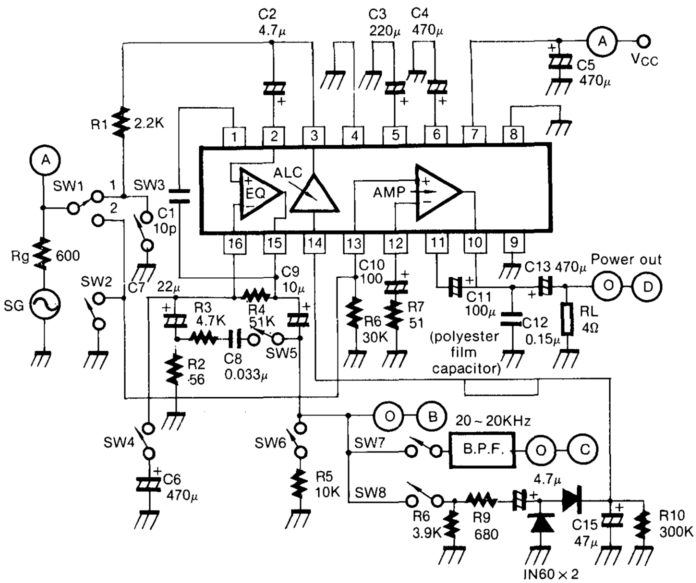


Fig. 2

TEST CONDITION

Characteristic	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	Test Point	Test Method
I_{CC}		on	on	off	on	on	off	off		Test circuit current
A_V	2	off	off	off	on	on	off	off	A.D.	$A_V = 20 \log V_O/V_I$ (dB)
P_O	2	off	off	off	on	on	off	off	D	Test output voltage at THD = 10%
THD	2	off	off	off	on	on	off	off	D	Test THD at output voltage $V_O = 1V$
V_{NO}		on	off	off	on	on	off	off	D	Test output noise voltage
RR		on	off	off	on	on	off	off	D	RR = 20 log V_{ro}/150 (dB) Test output ripple voltage (V_{ro})
A_{VO}	1	off	off	on	off	on	off	off	A.B	$A_{VO} = 20 \log V_O/V_I$ (dB)
V_O	1	off	off	off	on	on	off	off	B	Test output voltage at THD = 1%
V_{NI}		off	on	off	on	on	on	off	C	Convert output noise voltage at $R_g = 2.2K\Omega$, $V_{NI} = V_{NO}/A_V$
ALC Input Level	1	off	off	off	off	off	off	on	A.B	Test input voltage at THD = 1%

TYPICAL APPLICATION CIRCUIT

1. Mono cassette tape recorder

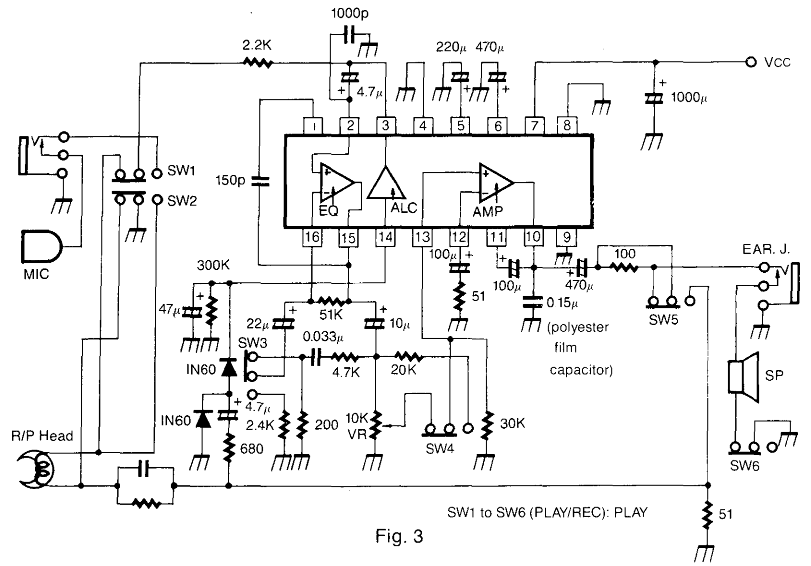


Fig. 3

2. Radio cassette tape recorder

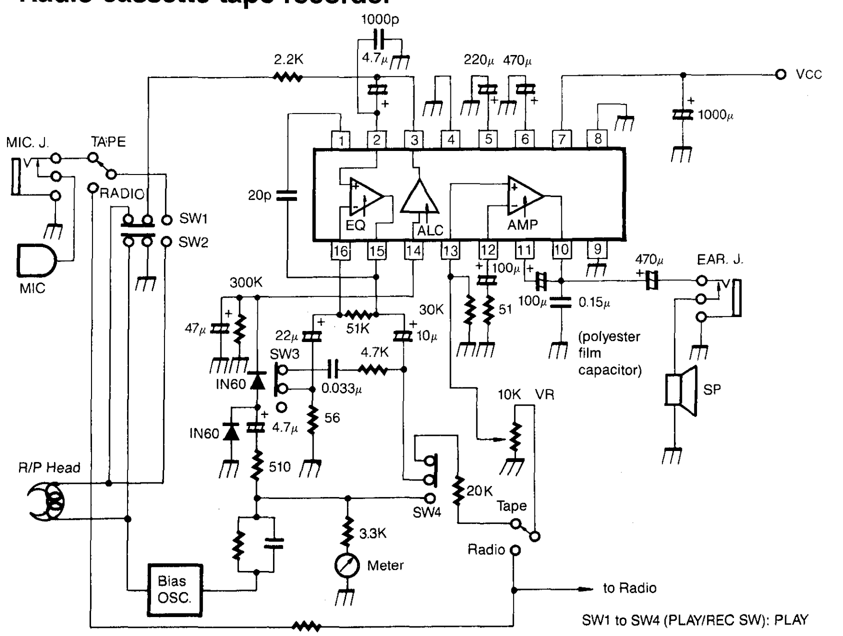
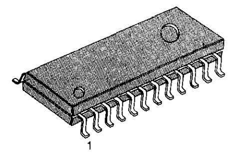


Fig. 4

DUAL PRE-POWER AMPLIFIER FOR AUTO REVERSE

The KA22131 is a monolithic integrated circuit consisting of an autoreverse dual pre and power amplifier. It is suitable for 3V portable radio cassettes with an auto-reverse function.

24 SOP



FEATURES

- **Dual pre-power amplifier on 1 chip**
- **Auto-reverse switch included**
- **Muting circuit included for Metal/Normal gain control**
- **LED drive circuit included for tape direction indication**
- **Power ON muting circuit inclued for suppression of shock-noise at the power ON time.**
- **Operating supply voltage range: V_{CC} = 1.8V ~ 3.6V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22131D	24 SOP	−20 ~ +70°C

BLOCK DIAGRAM

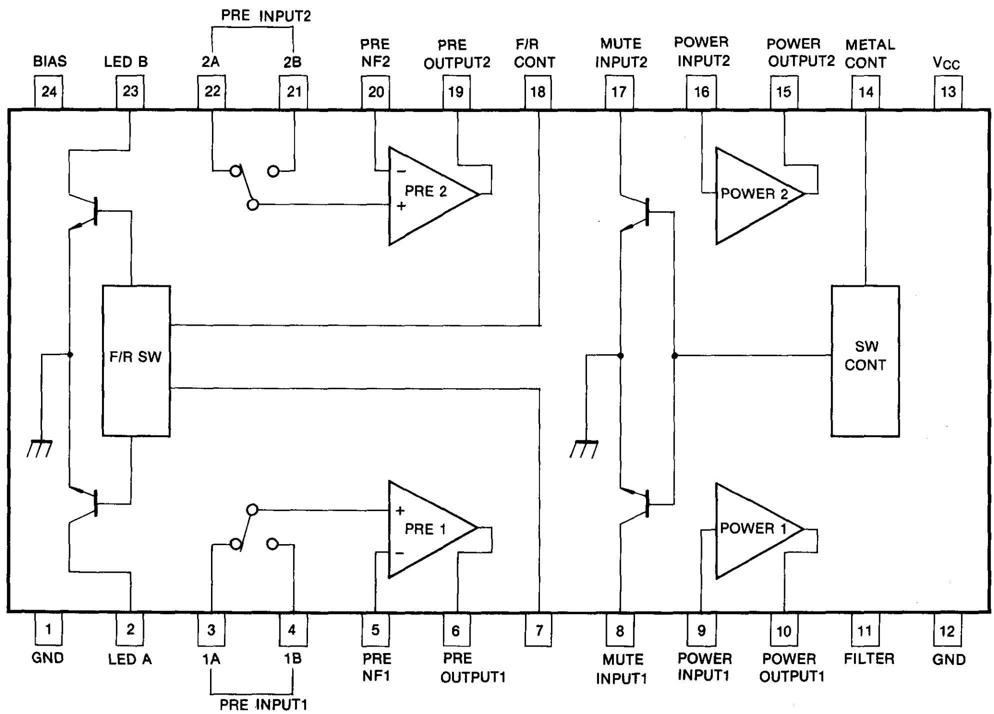


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	4.5	V
Power Dissipation	P_d	600	mW
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−55 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 3V, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i = 0V, Pin 14, 18: Open	4	9	15	mA
PRE-AMP (R_L = 10KΩ)						
Open Loop Voltage Gain	A_{VO}	V_o = −10dBm	72	83		dB
Output Voltage	V_o	THD = 1%	300	450		mV
Total Harmonic Distortion	THD	V_o = 0.2V, NAB = 33dB		0.03	0.08	%
Equivalent Input Noise Voltage	V_{NI}	R_g = 2.2KΩ BW(−3dB) = 20Hz ~ 20KHz		0.9	1.2	μV
Ripple Rejection Ratio	RR	V_r = −20dBm, f = 100Hz NAB = 33dB	43	53		dB
FWD-REV Cross Talk	CT_{F-R}	V_o = −10dBm, R_g = 2.2KΩ BW = 20Hz ~ 20KHz	65	75.5		dB
Input Bias Current	I_B	V_i = 0V		130	500	nA
POWER-AMP (R_L = 16Ω)						
Output Power	P_o	THD = 10%	50	69		mW
Closed Loop Voltage Gain	A_V	V_i = −40dBm	24.6	26.6	28.6	dB
Total Harmonic Distortion	THD	P_o = 1mW		0.27	0.5	%
Output Noise Voltage	V_{NO}	R_g = 0Ω, BW(−3dB) = 20Hz ~ 20KHz		27	39	μV
Ripple Rejection Ratio	RR	V_r = −20dBm, f = 100Hz , R_g = 0Ω	45	61		dB
Input Resistance	R_i		21.4	30	38.6	KΩ
Input Bias Current	I_B	V_i = 0V, R_g = 100KΩ		10	90	nA
Channel Balance	CB	V_o = −10dBm		0.1	0.7	dB
LED Maximum Current	I_{LED}	V_{CE}(sat) = 0.3V	5			mA
PRE + POWER AMP						
L-R Cross Talk	CT_{L-R}	VR: Max, PRE: R_g = 2.2KΩ BW = 20Hz ~ 20KHz, Power: V_o = −5dBm	40	48		dB
Signal Leakage	SL	PRE: V_o = −12dBm VR: Min		−66	−60	dBm

TEST CIRCUIT

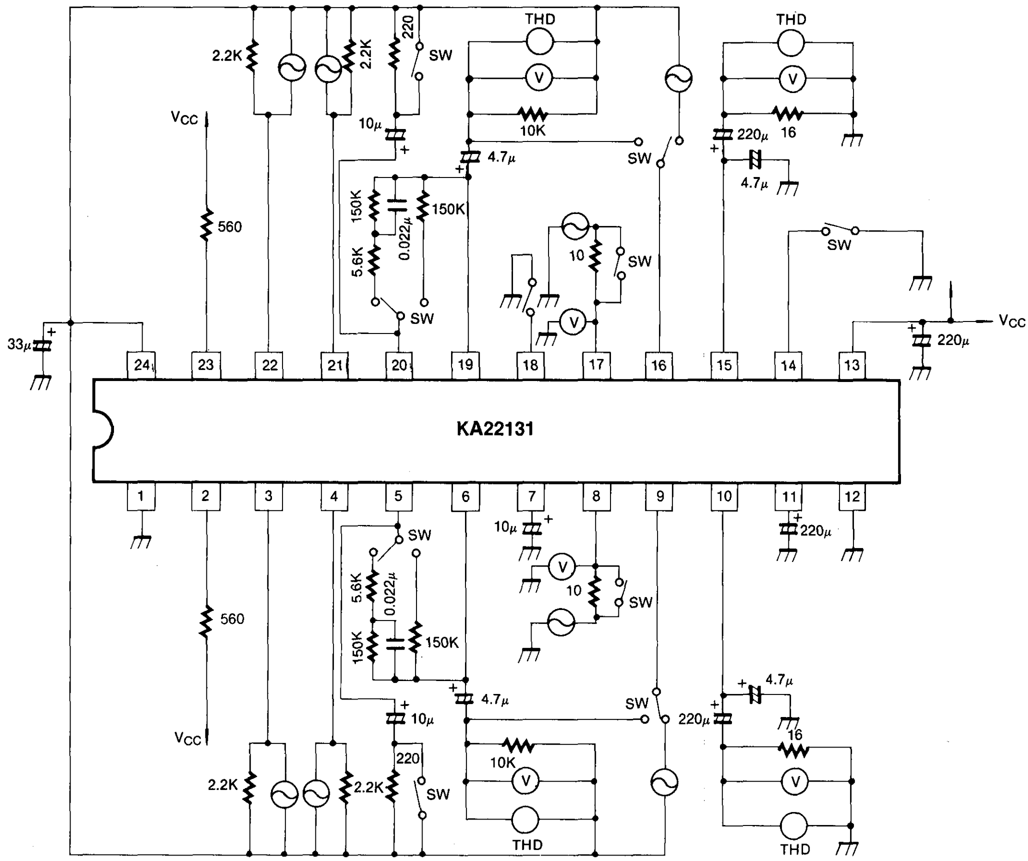


Fig. 2

APPLICATION CIRCUIT

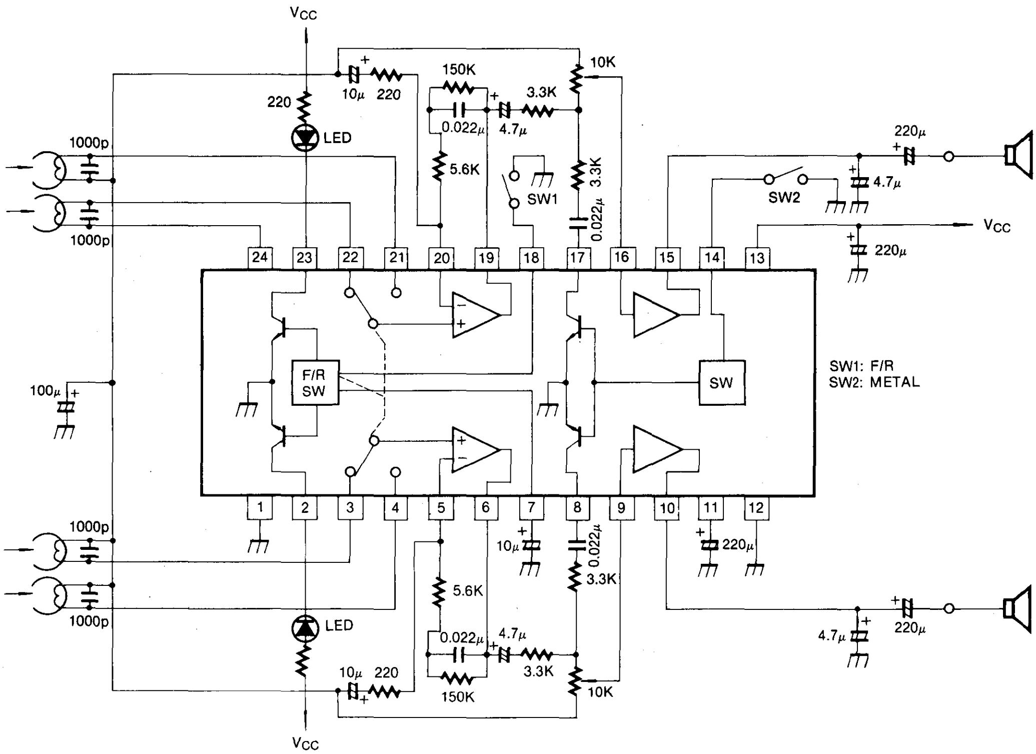
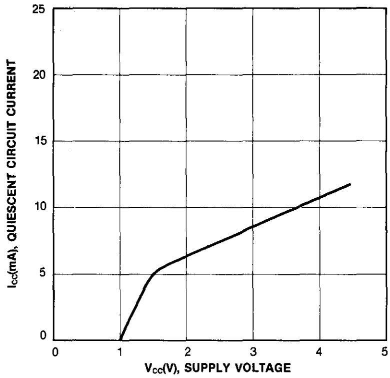
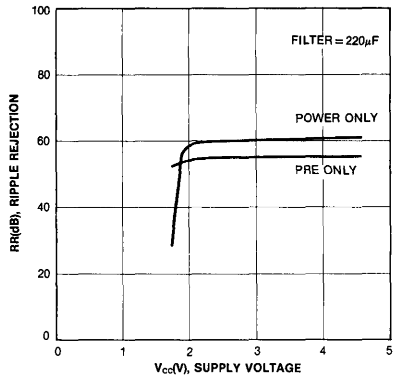


Fig. 3

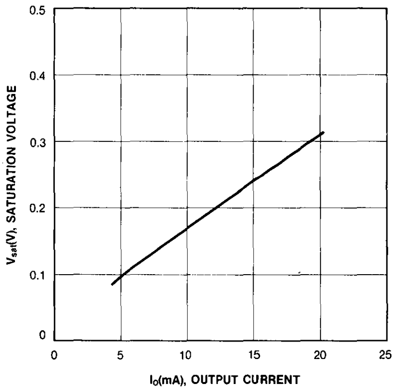
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



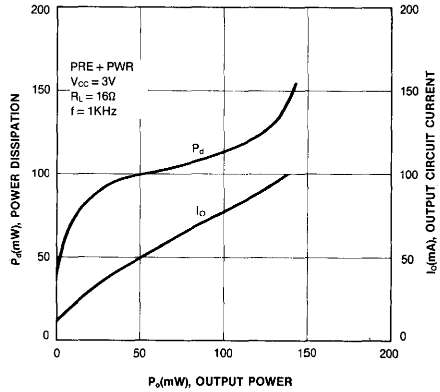
RIPPLE REJECTION-SUPPLY VOLTAGE



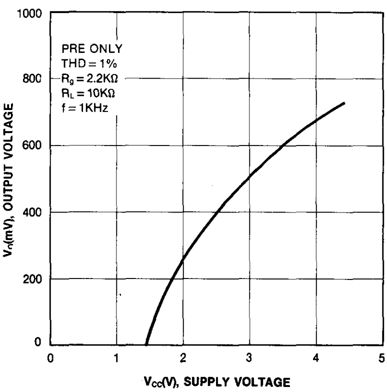
SATURATION VOLTAGE-OUTPUT CURRENT



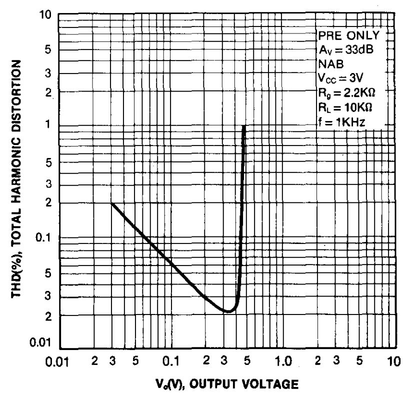
POWER DISSIPATION OUTPUT CIRCUIT CURRENT -OUTPUT POWER



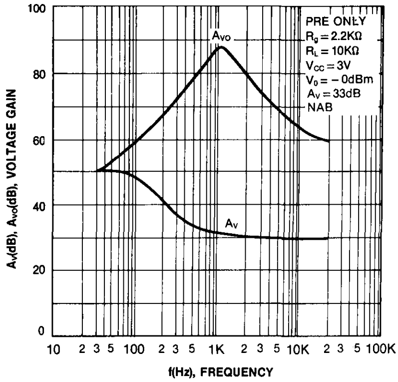
OUTPUT VOLTAGE-SUPPLY VOLTAGE



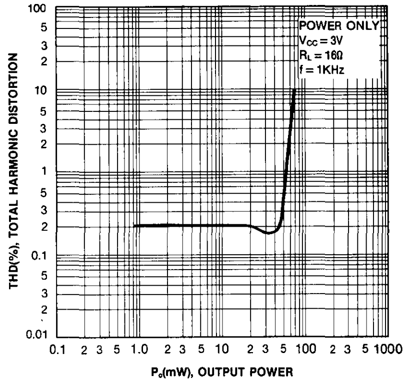
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



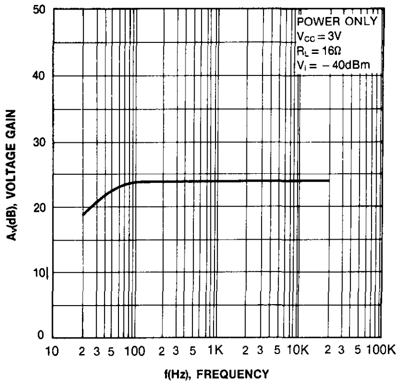
VOLTAGE GAIN-FREQUENCY



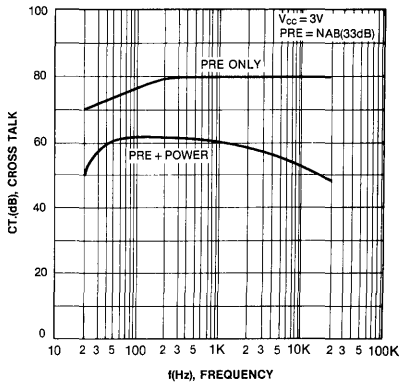
TOTAL HARMONIC DISTORTION-OUTPUT POWER



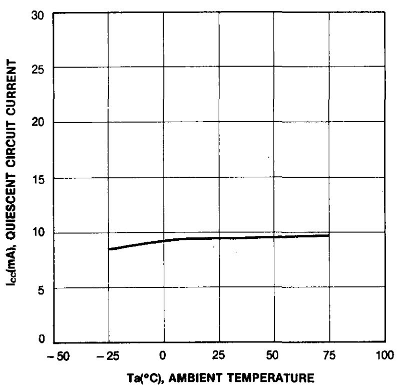
VOLTAGE GAIN-FREQUENCY



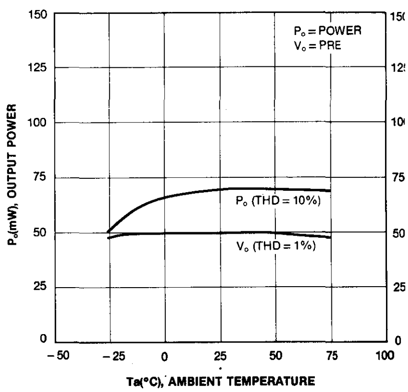
CROSS TALK-FREQUENCY



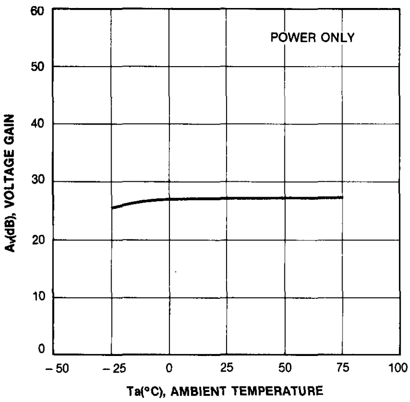
QUIESCENT CIRCUIT CURRENT-AMBIENT TEMPERATURE



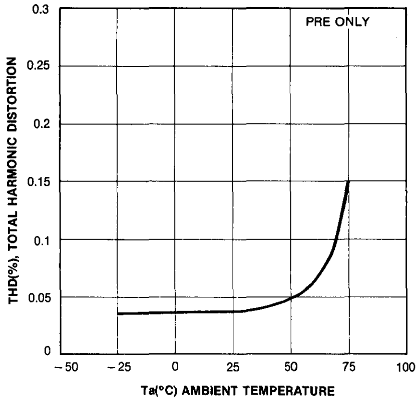
OUTPUT POWER-AMBIENT TEMPERATURE



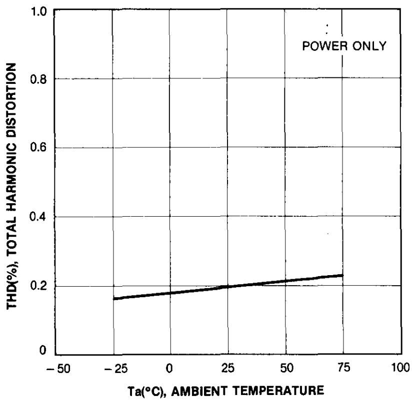
VOLTAGE GAIN-AMBIENT TEMPERATURE



TOTAL HARMONIC DISTORTION-AMBIENT TEMPERATURE



TOTAL HARMONIC DISTORTION-AMBIENT TEMPERATURE

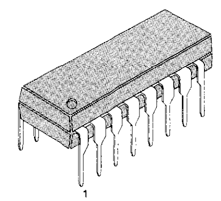


DUAL PRE-POWER AMPLIFIER WITH DC VOLUME CONTROL

The KA22134 is a monolithic integrated circuit designed for use in low voltage and low power applications. It has all functions including a dual audio pre-power amplifier, DC volume control and headphone drive circuits.

It is suitable for portable tape recorders or headphone cassette recorders.

16 DIP



FEATURES

- **Built-in DC volume control circuit.**
- **Wide operation supply voltage: $V_{CC}=1.8 \sim 6V$**
- **Only a few components to build headphone cassette tape recorders.**
- **Built-in ripple filter.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22134	16 DIP	$-20 \sim +75°C$

BLOCK DIAGRAM

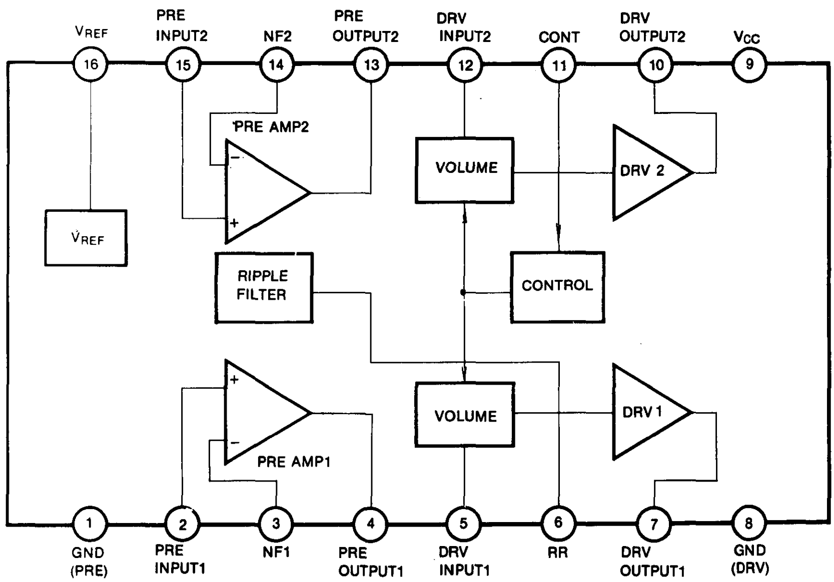


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	7	V
Power Dissipation	P_d	750	mW
Operating Temperature	T_{opr}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3V, Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC1}	$V_i = 0$, V_{OL} = min		9	13	mA
	I_{CC2}	$V_i = 0$, V_{OL} = max		11.0		mA
Cross Talk	CT	R_g = 2.2KΩ, V_O = −10dBm	34	40		dB

PRE-AMPLIFIER SECTION

(V_{CC} = 3V, Ta = 25°C, f = 1KHz, RL_1 = 10KΩ, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Open Loop Voltage Gain	A_{VO}	V_i = 0.2mV	55	62		dB
Closed Loop Voltage Gain	A_{V1}	V_O = −10dBm, NAB 1KHz		33		dB
Output Voltage	V_{om}	THD = 1%	600	720		mV
Total Harmonic Distortion	THD_1	V_O = −10dBm		0.04	0.1	%
Ripple Rejection Ratio	RR_1	R_g = 2.2KΩ V_r = −20dBm, f_r = 100Hz		46		dB
Equivalent Input Noise Voltage	V_{NI}	R_g = 2.2KΩ, BW = 30 ~ 20KHz Gain for NAB 1KHz		1.2	2.0	μV

POWER AMPLIFIER SECTION

(V_{CC} = 3V, Ta = 25°C, f = 1KHz, RL_2 = 32Ω, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Power	P_{O1}	THD_2 = 10%	20	27		mW
	P_{O2}	THD_2 = 10%, R_L = 16Ω		39		mW
Total Harmonic Distortion	THD_2	P_O = 10mW, Volume: 100%		0.5	1.2	%
	THD_3	P_O = 10mW, Volume: 50%		0.3		%
Closed Loop Voltage Gain	A_{V2}	V_O = −10dBm, Volume: 100%	28	30	32	dB
	A_{V3}	V_O = −10dBm		15		dB
Channel Balance	CB	V_O = −10dBm	−1.5	0	−1.5	dB
Volume Rejection Ratio	V_{min}	V_O = −10dBm, Volume: 100% to 0%	66	72		dB
Output Noise Voltage	V_{NO}	BW = 30 − 20KHz, R_g = 600Ω		250	320	μV
Ripple Rejection Ratio	RR_2	R_g = 600Ω, f_r = 100Hz V_r = −20dBm		46		dB

TEST CIRCUIT

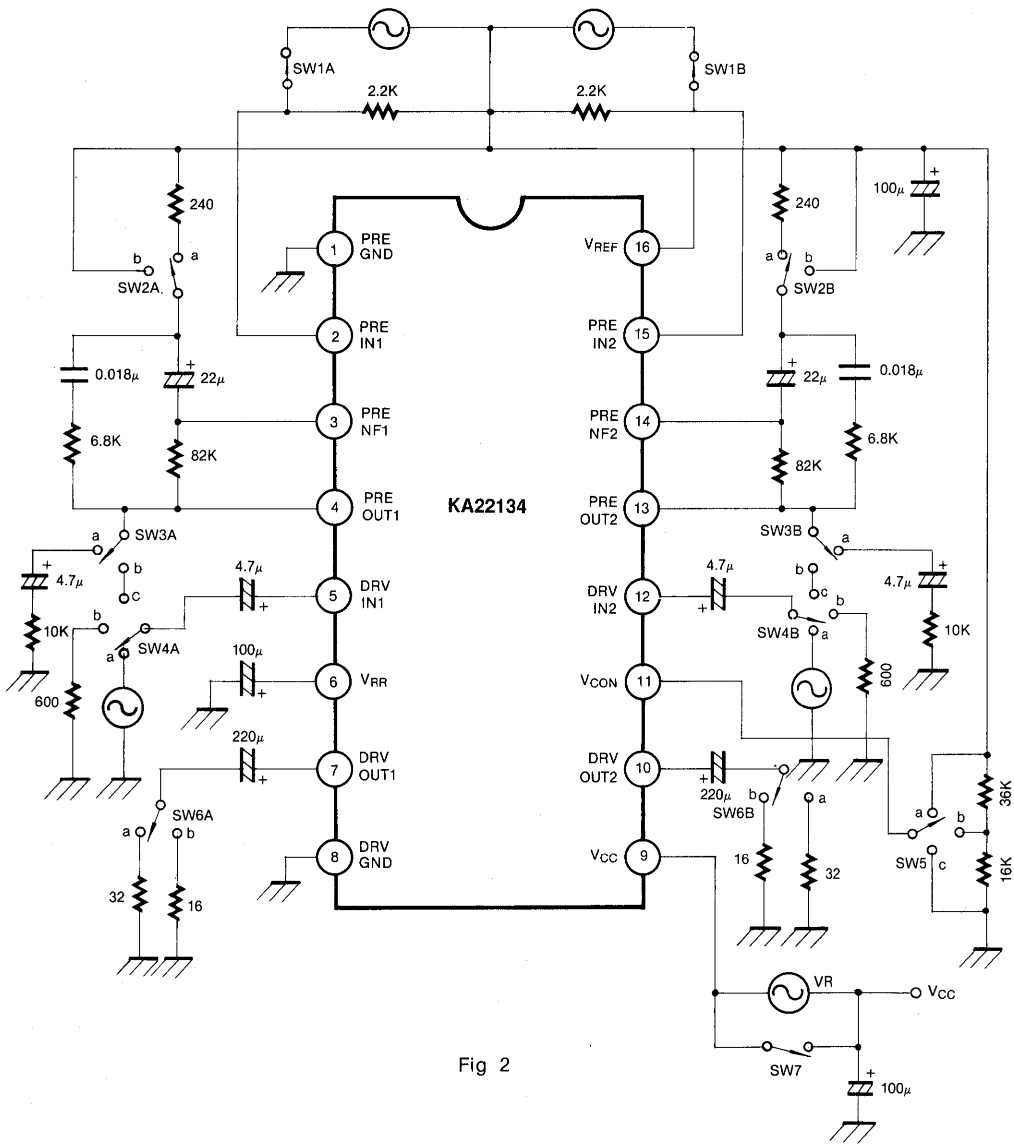


Fig 2

TEST CONDITIONS

Item	SW1A	SW1B	SW2A/B	SW3A/B	SW4A/B	SW5	SW6A/B	SW7
I_{CC1}	x	x	a	a	b	c	a	0
I_{CC2}	x	x	a	a	b	a	a	0
A_{V0}	0	0	b	a	b	c	a	0
A_{V1}	0	0	a	a	b	c	a	0
V_{om}	0	0	a	a	b	c	a	0
THD_1	0	0	a	a	b	c	a	0
V_{NI}	x	x	a	a	b	c	a	0
RR_1	x	x	a	a	b	c	a	x
P_{O1}	x	x	a	a	a	a	a	0
P_{O2}	x	x	a	a	a	a	b	0
A_{V2}	x	x	a	a	a	a	a	0
A_{V3}	x	x	a	a	a	b	a	0
CB	x	x	a	a	a	a	a	0
THD_2	x	x	a	a	a	a	a	0
THD_3	x	x	a	a	a	b	a	0
V_{no}	x	x	a	a	b	a	a	0
V_{min}	x	x	a	a	a	a→c	a	0
RR_2	x	x	a	a	b	c	a	x
CT	x/0	0/x	a	b	c	a	a	0

Note: 0 = close, x = open

APPLICATION CIRCUIT

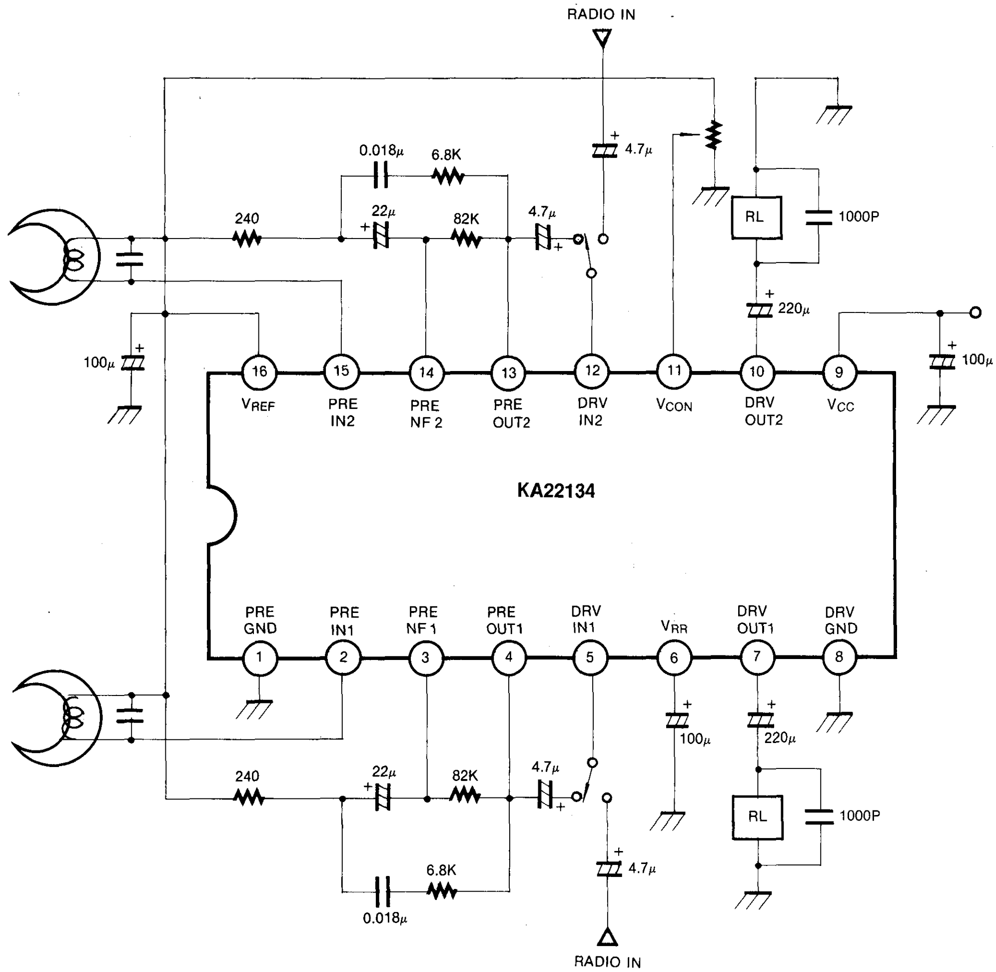
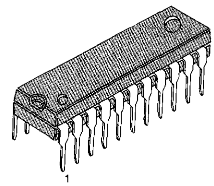


Fig. 3

DUAL PRE-POWER AMPLIFIER AND DC MOTOR SPEED CONTROLLER

The KA22135 is a monolithic integrated circuit designed for use in low voltage and low power applications. It has all functions including a dual audio pre-power amplifier and motor speed controller in a single chip. It is suitable for portable tape recorders, head phone cassette tape recorders or battery-powered radios.

22 SDIP



FEATURES

- **Low current consumption in a operating voltage range.**
- **Wide operating supply voltage range; V_{CC} = 2V ~ 7.5V.**
- **Only a few components to build headphone cassette tape recorders.**
- **Dual audio pre-power amplifier and motor speed controller in a single chip.**
- **Reduced input and output coupling capacitors because of 1/2 V_{CC} AMP adoption on chip as AC GND.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22135	22 SDIP	−20 ~ +70°C

BLOCK DIAGRAM

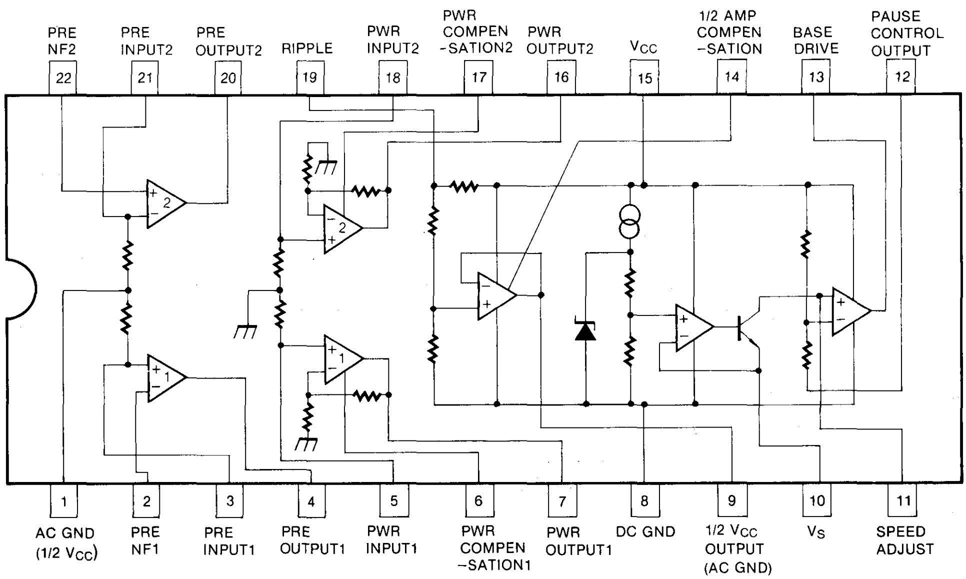


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	10	V
Power Dissipation	P_d	600	mW
Operating Temperature	T_{opr}	− 20 ~ + 70	°C
Storage Temperature	T_{stg}	− 40 ~ + 125	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_{CC} = 3V, V_i = 0, I_m = 0mA		15	25	mA

PRE AMPLIFIER SECTION
(Ta = 25°C, V_{CC} = 3V, f = 1KHz, R_{L1} = 10KΩ, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Open Loop Voltage Gain	A_{VO}	V_O = − 10dBm, R_L = ∞		72		dB
Closed Loop Voltage Gain	A_V	V_o = − 10dBm	40	42	44	dB
Output Voltage	V_o	THD = 1%	0.35	0.6		V
Total Harmonic Distortion	THD	V_o = 400mV		0.05	0.5	%
Output Noise Voltage	V_{NO}	V_i = 0, R_g = 2.2KΩ BW(− 3dB) = 30Hz ~ 20KHz		70	300	μV
Input Resistance	R_i	V_o = − 10dBm	18	22		KΩ
Cross Talk	CT	R_g = 2.2KΩ, V_o = − 10dBm	45	62		dB

POWER AMPLIFIER SECTION
(Ta = 25°C, V_{CC} = 3V, f = 1KHz, R_{L2} = 32Ω, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Closed Loop Voltage Gain	A_V	P_o = 5mW	26	28	30	dB
Output Power	P_o	THD = 10%	20	28		mW
Total Harmonic Distortion	THD	P_o = 5mW		0.2	2.0	%
Output Noise Voltage	V_{NO}	R_g = 10KΩ, BW(− 3dB) = 30Hz ~ 20KHz		0.25	1.0	mV
Input Resistance	R_i	P_o = 5mW	10	20		KΩ
Cross Talk	CT	P_o = 5mW, R_g = 10KΩ	35	50		dB

MOTOR SPEED CONTROLLER SECTION
(Ta = 25°C, V_{CC} = 3V, I_m = 100mA, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Base Driving Current	I_B		10	18		mA
Reference Voltage	V_{ref}		0.22	0.26	0.30	V
Reference Voltage Regulation 1	ΔV_{ref1}	V_{CC} = 2.0 ~ 6.5V		0.05		%/V
Reference Voltage Regulation 2	ΔV_{ref2}	I_m = 25 ~ 200mA		0.1		%/mA
Reference Voltage Regulation 3	ΔV_{ref3}	Ta = −10 ~ +60°C		0.01		%/°C
Current Coefficient	K	$K = \frac{V_L - V_{R2}}{V_{R1} + V_{R2}}$	3.7	4	4.3	
Current Coefficient Regulation 1	ΔK_1	V_{CC} = 2.0 ~ 6.5V		0.05		%/V
Current Coefficient Regulation 2	ΔK_2	I_m = 25 ~ 200mA		0.1		%/mA
Current Coefficient Regulation 3	ΔK_3	Ta = −10 ~ +60°C		0.1		%/°C

TEST CIRCUIT

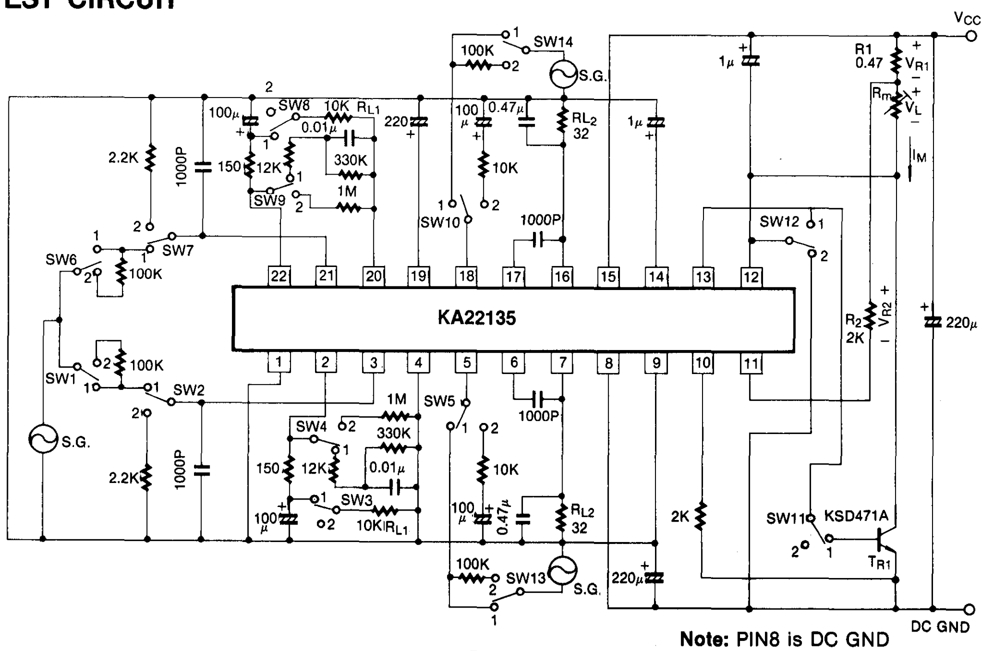


Fig. 2

TEST METHODS

TEST ITEM \ SWITCH		1	2	3	4	5	6	7	8	9	10	11	12	13	14
	I_{CC}	1	2	1	1	2	1	2	1	1	2	1	2	1	1
PRE AMP	CH1 A_{vo}	〃	1	2	2	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃
	CH1 A_V	〃	〃	1	1	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃
	CH1 V_O	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃
	CH1 THD	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃
	CH1 V_{no}	〃	2	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃
	CH1 R_i	2	1	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃
	CH2 A_{vo}	1	2	〃	〃	〃	〃	1	2	2	〃	〃	〃	〃	〃
	CH2 A_V	〃	〃	〃	〃	〃	〃	〃	1	1	〃	〃	〃	〃	〃
	CH2 V_O	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃
	CH2 THD	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃
	CH2 V_{no}	〃	〃	〃	〃	〃	〃	2	〃	〃	〃	〃	〃	〃	〃
	CH2 R_i	〃	〃	〃	〃	〃	2	1	〃	〃	〃	〃	〃	〃	〃
	C.T1 (2→1)	〃	〃	〃	〃	〃	1	1	〃	〃	〃	〃	〃	〃	〃
	C.T2 (1→2)	〃	1	〃	〃	〃	〃	2	〃	〃	〃	〃	〃	〃	〃
POWER AMP	CH1 A_V	〃	2	〃	〃	1	〃	〃	〃	〃	〃	〃	〃	〃	〃
	CH1 P_O	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃
	CH1 THD	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃
	CH1 V_{no}	〃	〃	〃	〃	2	〃	〃	〃	〃	〃	〃	〃	〃	〃
	CH1 R_i	〃	〃	〃	〃	1	〃	〃	〃	〃	〃	〃	〃	2	〃
	CH2 A_V	〃	〃	〃	〃	2	〃	〃	〃	〃	1	〃	〃	1	〃
	CH2 P_O	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃
	CH2 THD	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃
	CH2 V_{no}	〃	〃	〃	〃	〃	〃	〃	〃	〃	2	〃	〃	〃	〃
	CH2 R_i	〃	〃	〃	〃	〃	〃	〃	〃	〃	1	〃	〃	〃	2
	C.T1 (2→1)	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	1
	C.T2 (1→2)	〃	〃	〃	〃	1	〃	〃	〃	〃	2	〃	〃	〃	〃
M.S.C.	I_b	〃	〃	〃	〃	2	〃	〃	〃	〃	〃	2	1	〃	〃
	V_{ref}	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	1	〃	〃	〃
	$\triangle V_{ref}$	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃
	K	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃
	$\triangle K$	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃	〃

APPLICATION CIRCUIT

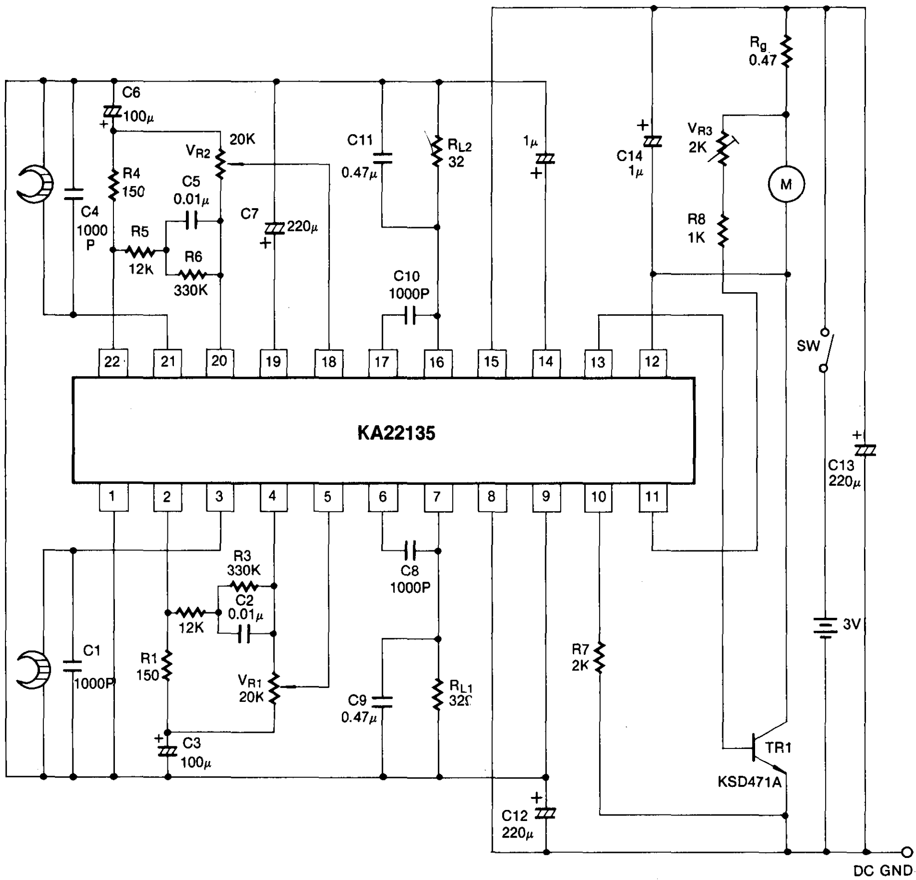


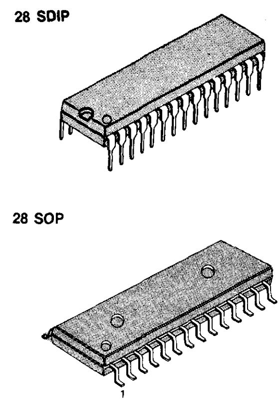
Fig. 3

Note: 1. For C12, use a capacitor of Low TANδ

2. For C9 and C11, use solid state capacitors with better characteristics at low temperature
3. Locate C7 just around the emitter TR1, KSD471A.

DUAL PRE-POWER AMPLIFIER, VOLUME CONTROLLER AND DC MOTOR SPEED CONTROLLER

The KA22136 is a molithic integrated circuit designed for use in low voltage and low power applications. It has all functions including dual audio pre-power amplifier, electronic volume controller and DC motor speed controller in a single chip. It is suitable for portable tape recorders headphone cassette tape recorders or radios by batteries.



FEATURES

- **Low current consumption in a operating voltage range.**
- **Operating supply voltage range: V_{CC} = 2.1 V ~ 5 V**
- **Only a few components in composing headphone cassette tape recorder.**
- **Dual audio pre-power amplifier, electronic volume controller and DC motor speed controller in a single chip.**
- **Reduced input and output coupling capacitors because of ½ V_{CC} AMP adoption on chip as AC GND.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22136	28SDIP	−20 ~ +65°C
KA22136D	28SOP	−20 ~ +65°C

BLOCK DIAGRAM

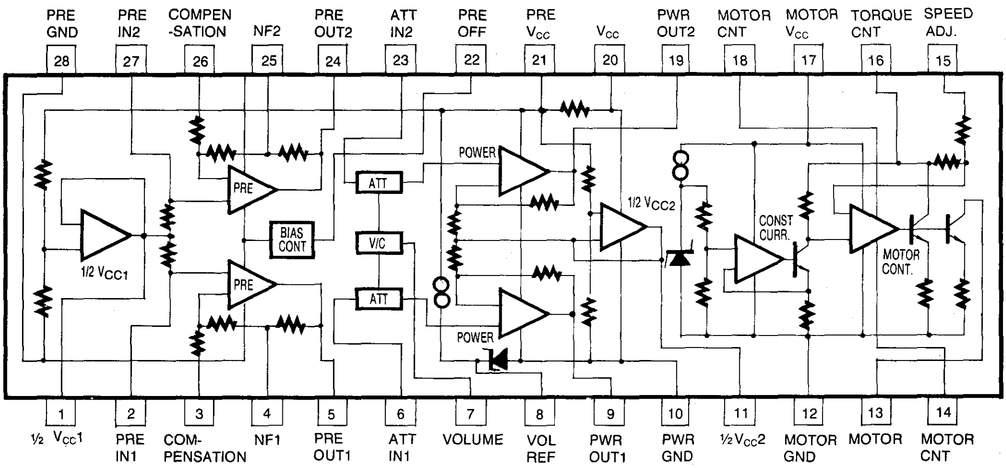


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.5	V
Power Dissipation	P_d	450	mW
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta=25°C, V_{CC}=3V, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent circuit current	I_{CC}	V_{CC}=3V, V_i=0, I_m=0		18	25	mA

PRE AMPLIFIER SECTION (V_{CC}=3V, f=1KHz, RL_1=10KΩ, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Open Loop Voltage Gain	A_{VO}	V_O= −10dBm, R_L=∞		72		dB
Closed Loop Voltage Gain	A_V(1)	V_O= −10dBm	40	42	44	dB
Output Voltage	V_O	THD=10%	0.45	0.6		V
Total Harmonic Distortion	THD(1)	V_O=400mV		0.05	0.5	%
Output Noise Voltage	V_{NO}(1)	V_i=0, R_g=2.2KΩ, BPF (30 ~ 20KHz)		150	300	μV
Input Resistance	R_i (1)	Vo=10dBm	18	22		KΩ
Cross Talk	CT(1)	R_g=2.2KΩ, V_O= −10dBm	30			dB
Output Voltage In Pre OFF	V_O(off)	V_i=100mV Pre OFF (pin 22)=V_{CC}			−50	dB

POWER AMPLIFIER SECTION (Ta=25°C, V_{CC}=3V, f=1KHz, R_L2=16Ω, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Closed Loop Voltage Gain	Av(2)	Po=5mW	26	28	30	dB
Voltage Gain Difference	ΔA_V	Vcont=Max		0	3	dB
Output Power 1	Po(1)	THD=10%, R_L=32Ω	20	28		mW
Output Power 2	Po(2)	THD=10%, R_L=16Ω	30			mW
Total Harmonic Distortion	THD(2)	Po=5mW		0.2	2.0	%
Pre+Power Noise	V_{NO}(2)	V_i=0, R_g=2.2KΩ, V_{cont}=Max		6	10	mV
Output Noise Voltage	V_{NO}(3)	R_g=2.2KΩ, V_{cont}=Min		0.25	1.0	mV
Cross Talk	CT(2)	Po=5mW	20	30		dB
Ripple Rejection Ratio	RR	Vcc=3V, 100Hz, 100mVp-p	34	40		dB

3

ATTENUATOR SECTION (Ta = 25°C, V_{CC} = 3V, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum input voltage	V_i (Max)		0.2			V
Maximum attenuation	Va (max)	Vcont = Min	66			dB
Attenuation error	Va (err)	Vcont = Max		0		dB
Input impedance	R_i (2)		15	20		KΩ

MOTOR SPEED CONTROLLER (Ta = 25°C, V_{CC} = 3V, I_m = 100mA, unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Consumption Current	I_{mc}			3.0	5.0	mA
Starting Current	I_{ms}		500			mA
Reference Voltage	Vref	V (pin 15, 16)	0.72	0.80	0.87	V
Reference Voltage Regulation 1	ΔVref (1)	* V_{CC} = 2.1 ~ 5.0V		0.05		%/V
Reference Voltage Regulation 2	ΔVref (2)	Im = 25 ~ 250mA		0.01		%/mA
Reference Voltage Regulation 3	ΔVref (3)	Ta = −10 ~ 50°C		0.01		%/°C
Current Coefficient	K		32	38	43	
Current Coefficient Regulation 1	ΔK(1)	V_{CC} = 2.1 ~ 5.0V		0.50		%/V
Current Coefficient Regulation 2	ΔK(2)	Im = 25 ~ 250mA		0.05		%/mA
Current Coefficient Regulation 3	ΔK(3)	Ta = −10 ~ 50°C		0.02		%/°C
Saturation Voltage	Vsat	Im = 200mA, Pin14 = V_{CC}			0.6	V
Leakage Current	I_{LK}	Pin 18 = V_{CC}		50	200	μA

*Voltage across Pin 13, 17

TEST CIRCUIT

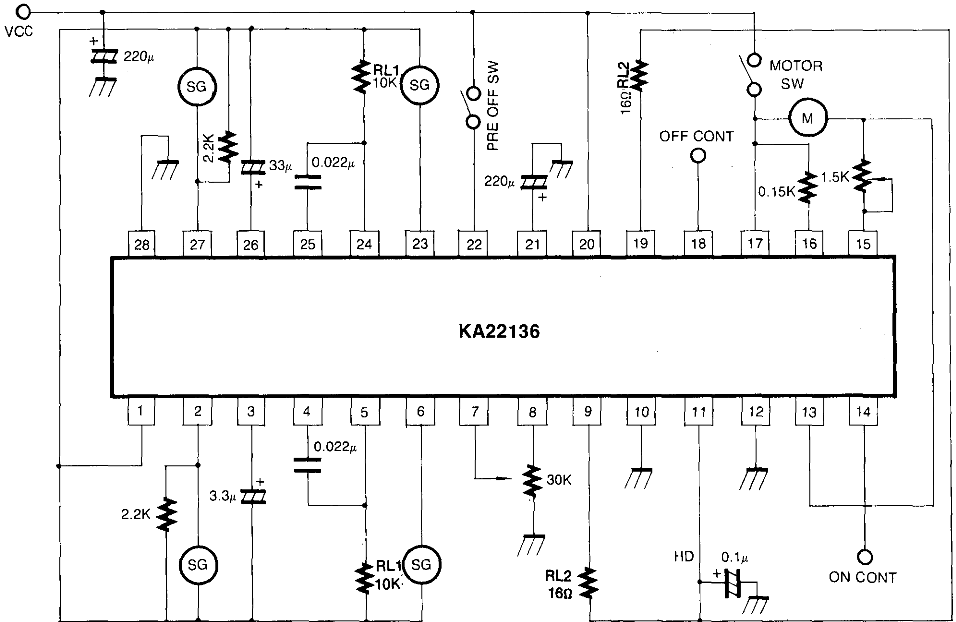


Fig. 2

APPLICATION CIRCUIT

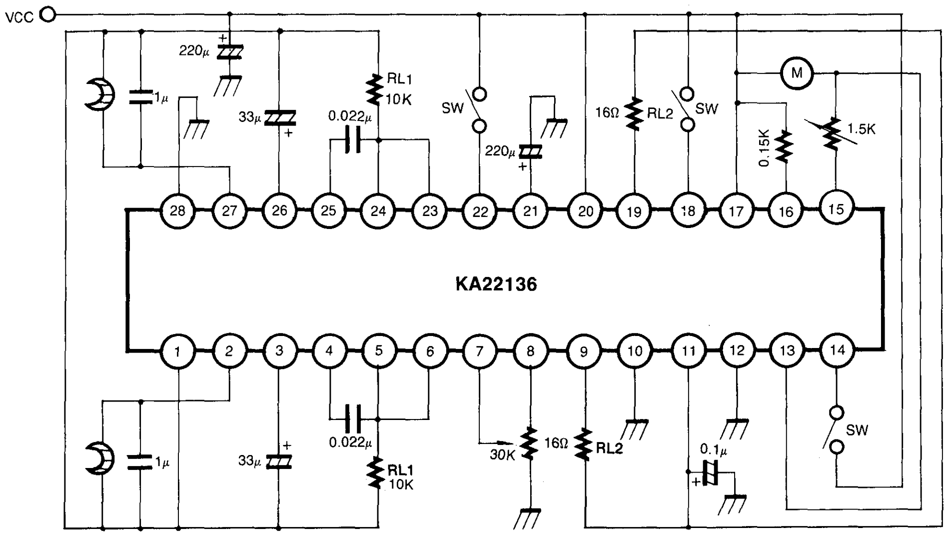
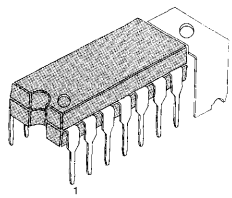


Fig. 3

1.2W DUAL POWER AMPLIFIER

The KA2214 is a dual audio power amplifier in a 14-pin dual in line package. It is designed for portable audio sets.

14 DIP H/S



FEATURES

- **Wide operating voltage; V_{CC} = 3V ~ 13V**
- **High output power; P_o = 2W at 12V/8Ω/THD = 10%**
  P_o = 1.6W at 9V/4Ω/THD = 10%
  P_o = 1.2W at 9V/8Ω/THD = 10%
  P_o = 0.7W at 6V/4Ω/THD = 10%
  P_o = 0.5W at 6V/8Ω/THD = 10%
  P_o = 50mW at 4.5V/32Ω/THD = 10%
- **High ripple rejection ratio; 50dB (Typ)**
- **Low quiescent current; 10mA (V_{CC} = 9V)**
- **Easy assembly so that two power amplifiers are built in a package.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2214	14 DIP H/S	−20 ~ +70°C

BLOCK DIAGRAM

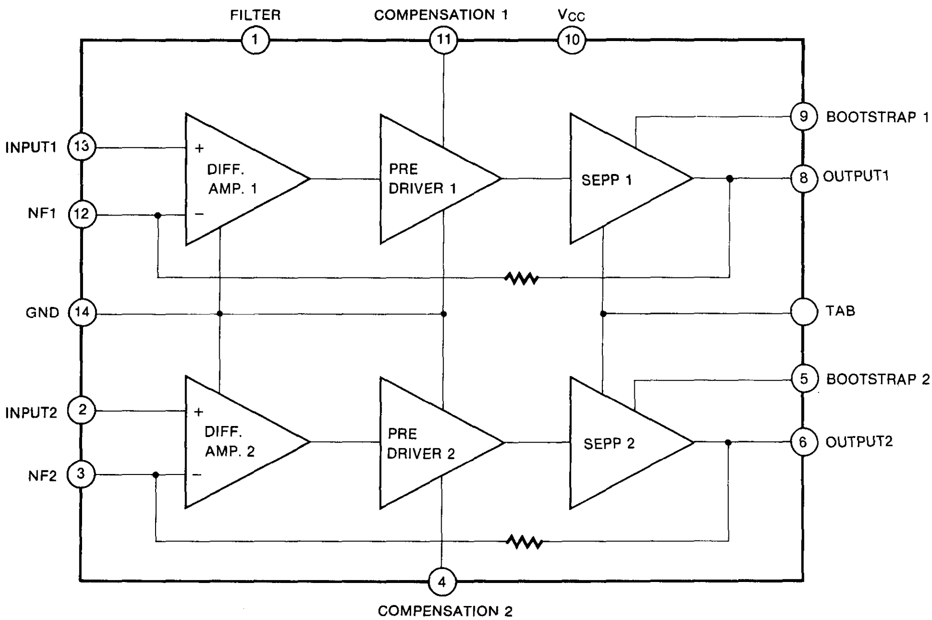


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage (No Signal)	V_{CC}	18	V
Supply Voltage (Operating)	V_{CC}	16	V
Power Dissipation ·	P_d	2.4	W
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 9V, R_f = 33Ω, f = 1KHz, R_L = 8Ω, R_g = 600Ω, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i = 0		10		mA
Voltage Gagin	A_{V1}	P_o = 0.25W, R_f = 33Ω		44		dB
	A_{V2}	P_o = 0.25W, R_f = 120Ω		34		dB
Output Power	P_{o1}	V_{CC} = 12V, R_L = 8Ω, THD = 10%		2		W
	P_{o2}	V_{CC} = 9V, R_L = 4Ω, THD = 10%		1.6		W
	P_{o3}	V_{CC} = 9V, R_L = 8Ω, THD = 10%	0.9	1.2		W
	P_{o4}	V_{CC} = 6V, R_L = 4Ω, THD = 10%		0.7		W
	P_{o5}	V_{CC} = 6V, R_L = 8Ω, THD = 10%		0.5		W
	P_{o6}	V_{CC} = 4.5V, R_L = 32Ω, THD = 10%		50		mW
Total Harmonic Distortion	THD_1	P_o = 0.5W, R_f = 33Ω		0.8		%
	THD_2	P_o = 0.5W, R_f = 120Ω		0.4		%
Output Noise Voltage	V_{NO}	R_g = 10KΩ, BW(−3dB) = 20Hz ~ 20KHz		0.6		mV
Ripple Rejection Ratio	RR	R_g = 0, f = 120Hz, V_r = 0.3V		50		dB
Cross Talk	CT	R_g = 0, P_o = 0.25W		55		dB
Channel Balance	CB	P_o = 0.25W	−2	0	2	dB
Input Resistance	R_i			5		MΩ

APPLICATION CIRCUIT

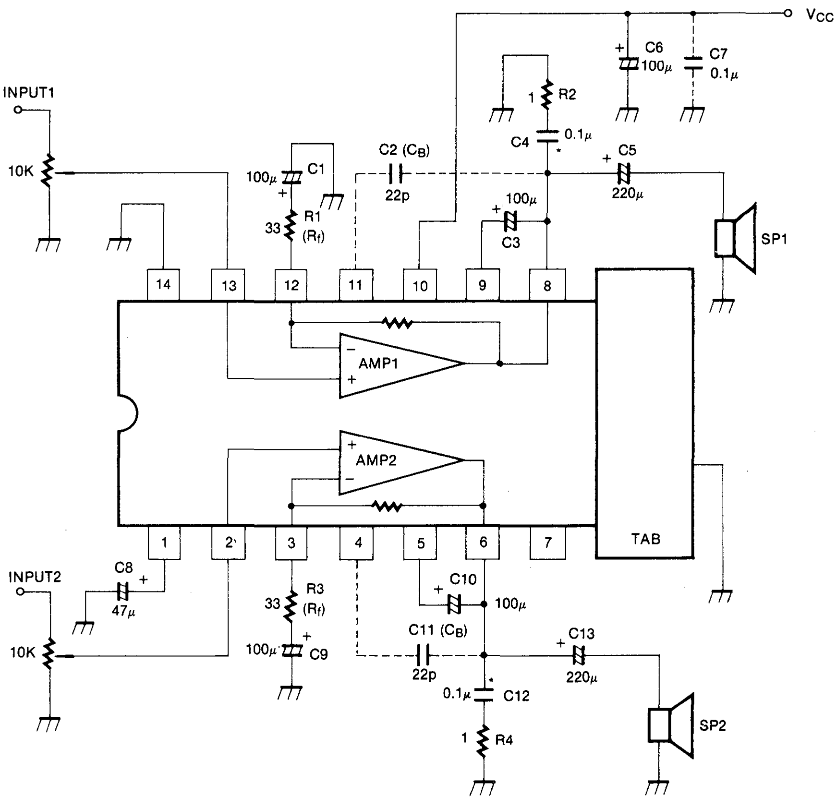


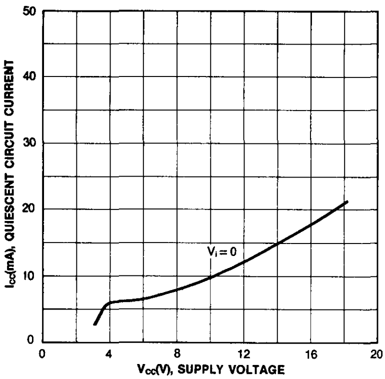
Fig. 2

* Mylar Capacitor

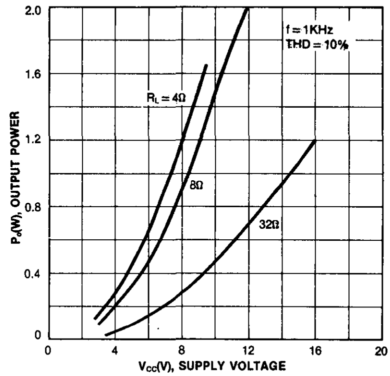
APPLICATION NOTES

(1) Mylar capacitor is recommended for C4, C12.
(2) Add C2, C11, for reducing voltage gain at high frequency.
(3) Add C7 or increase capacitance of C4, C12, when a oscillation may occur due to the pattern on the PCB.
(4) Voltage gain can be changed by the values of R1, R3.

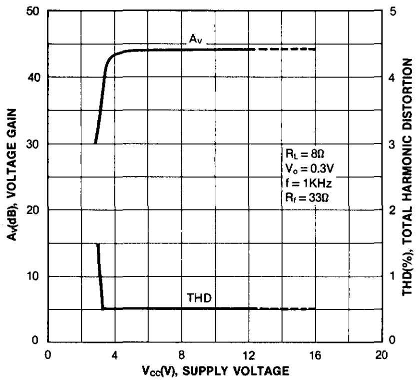
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



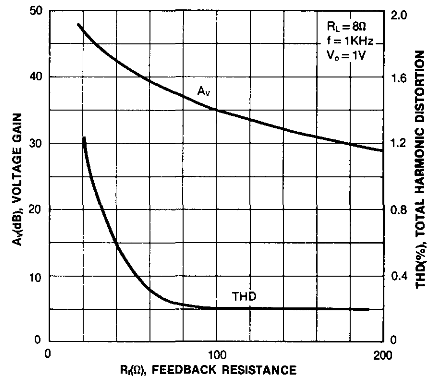
OUTPUT POWER-SUPPLY VOLTAGE



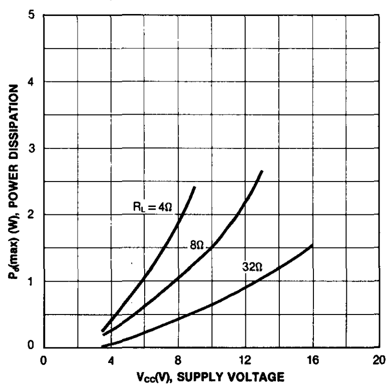
VOLTAGE GAIN / TOTAL HARMONIC DISTORTION -SUPPLY VOLTAGE



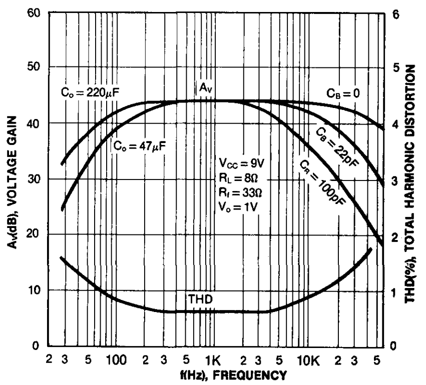
VOLTAGE GAIN / TOTAL HARMONIC DISTORTION -FEEDBACK RESISTANCE



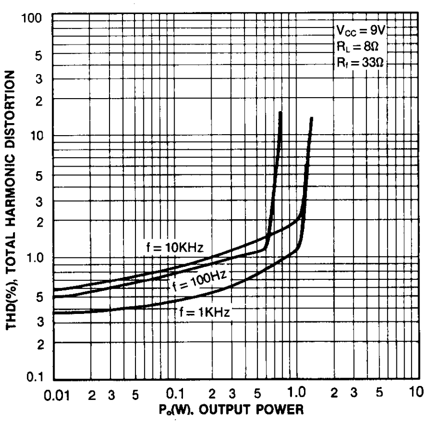
POWER DISSIPATION-SUPPLY VOLTAGE



VOLTAGE GAIN / TOTAL HARMONIC DISTORTION -FREQUENCY



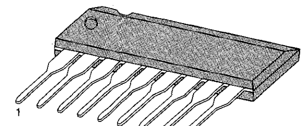
TOTAL HARMONIC DISTORTION-OUTPUT POWER



EQUALIZER AMPLIFIER WITH ALC

The KA2220 is a monolithic integrated circuit consisting of a preamplifier and ALC circuit for cassette tape recorders

9 SIP



FEATURES

- **Low noise amplifier.**
- **Wide operating supply voltage range: V_{CC} = 3.5V ~ 14V**
- **High output voltage.**
- **Low distortion.**
- **Wide ALC range.**
- **KA2220 ST: Good ALC pair characteristic for stereo tape recorders**

SCHEMATIC DIAGRAM

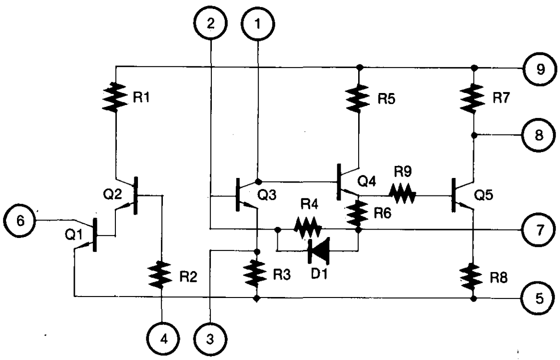
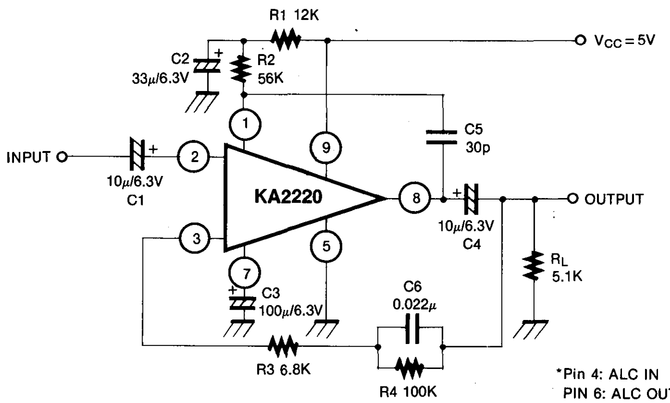


Fig. 1

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2220	9 SIP	−20 ~ +70°C

TEST CIRCUIT



*Pin 4: ALC IN
PIN 6: ALC OUT

Fig. 2

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Power Dissipation	P_d	200	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=5V, R_L=5.1KΩ, R_g=600Ω, f=1KHz, NAB, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i=0, ALC OFF		1.4	2.0	mA
Voltage Gain (Open Loop)	A_{VO}		66	69		dB
Voltage Gain (Closed Loop)	A_V	V_O=0.7V	33	35	37	dB
Output Voltage	V_O	THD=1%	0.7	1.0		V
Total Harmonic Distortion	THD	V_O=0.2V		0.1		%
Input Resistance	R_i		60	100		KΩ
Equivalent Input Noise Voltage	V_{NI}	R_g=2.2KΩ, NAB BW (−3dB)=15Hz ~ 30KHz		1.0		μV
ALC Transistor Saturation Voltage	V_{SAT}			75	100	mV

ALC GRADE BINNING TEST CIRCUIT

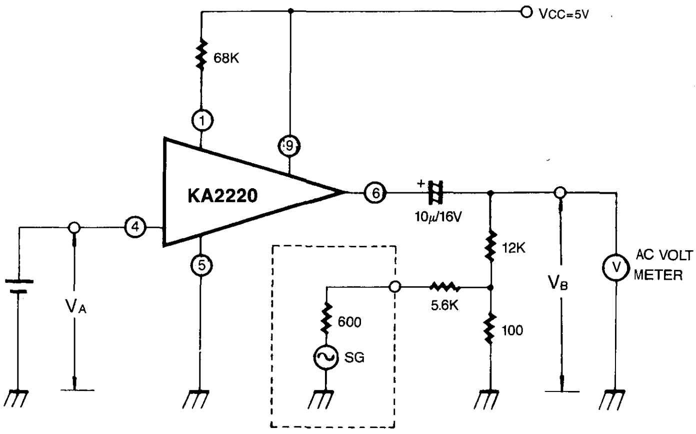


Fig. 3

Test condition: S.G output level should be adjusted to be 13.8mV of the AC voltmeter reading (V_B) when the D.U.T is not connected from the test circuit (V_{CC}=5V, V_A=1.16V, T_a=25°C)
ALC RANK is defined as ALC-G.R=20log V_{B2}/V_{B1}
where
V_{B1}: AC voltmeter reading when the D.U.T is not connected
V_{B2}: AC voltmeter reading whn the D.U.T is connected

ALC-G.R BINNING TABLE

Symbol	A_V (dB)		ALC Grade (dB)	
	Min	Max	Min	Max
KA2220 H	34	36	−16.0	−20.0
KA2220 J			−18.5	−22.5
KA2220 K			−21.0	−25.0
KA2220 L			−24.0	−28.0
KA2220 M			−27.0	−31.0
KA2220 N			−30.0	−34.0

External Components (Refer to test circuits)

C_1: Input coupling capacitor
The recommended value is 10μF. If made too small the low frequency characteristics will change for the worse, and too large a capacitance value will increase the rising time when power is applied.

C_2: Ripple filter for power supply
A large value is required to get an excellent ripple characteristic under the line operation, but must be made smaller to shorten the starting time.

C_3: Bypass capacitor
Short emitter resistor on the AC and prevents an AC signal from feedback to input.

C_4: Output coupling capacitor
C_4 is determined as follows:

$$C_4 = \frac{1}{2\pi \cdot f_L \cdot R_L}$$

f_L: low cut-off frequency
R_L: load resistance

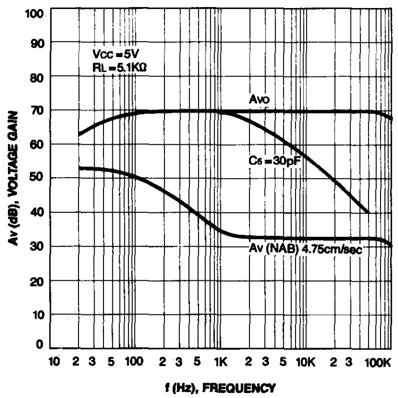
C_5: Phase compensation capacitor.
Prevents high frequency oscillation by phase error when feedback is heavy.

C_6, R_3, R_4: Equalizer network
The closed loop voltage gain is determined by these components in relation to the internal resistance at Pin 3.

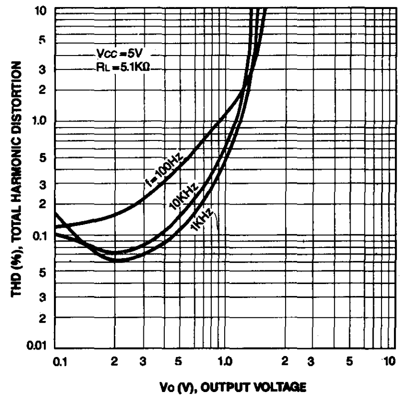
R_1: Filter resistance.

R_2: Collector resistor of first stage transistor of the IC
Low voltage characteristic can be improved by adjusting this resistance.

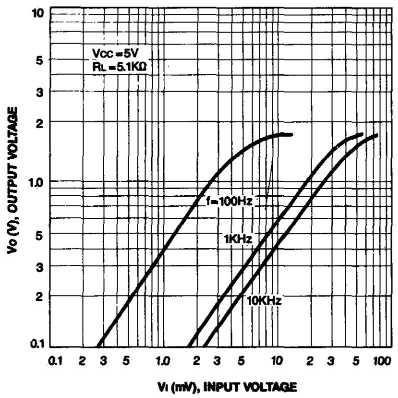
VOLTAGE GAIN-FREQUENCY



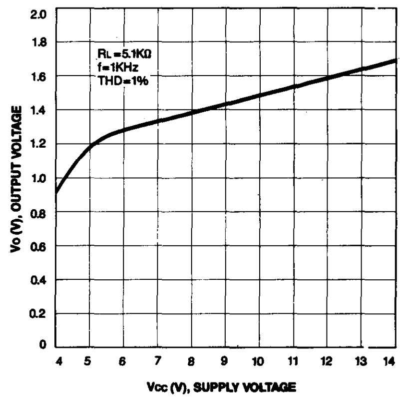
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



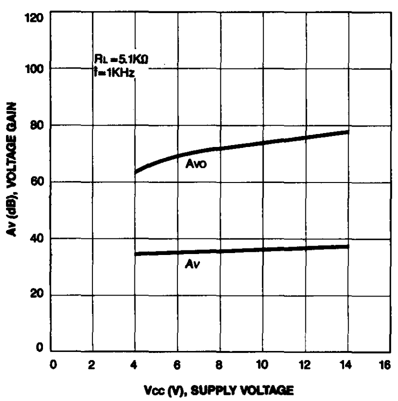
OUTPUT VOLTAGE-INPUT VOLTAGE



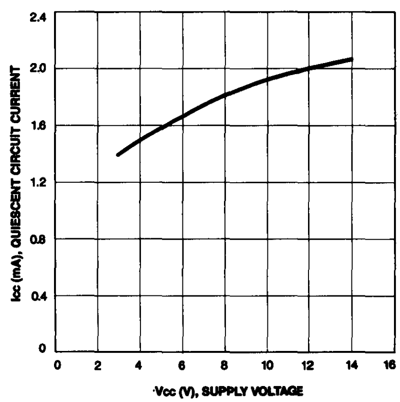
OUTPUT VOLTAGE-SUPPLY VOLTAGE



VOLTAGE GAIN-SUPPLY VOLTAGE



QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



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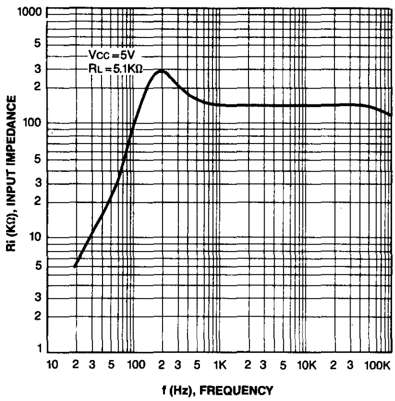
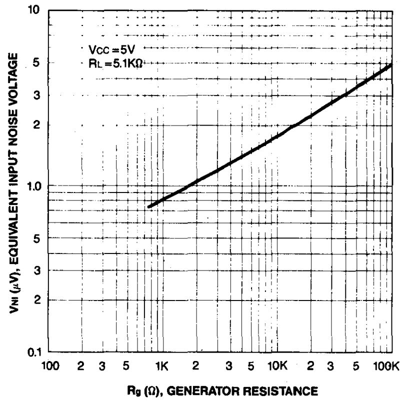
INPUT IMPEDANCE-FREQUENCY



EQUIVALENT INPUT NOISE VOLTAGE — GENERATOR RESISTANCE



TYPICAL APPLICATION CIRCUIT

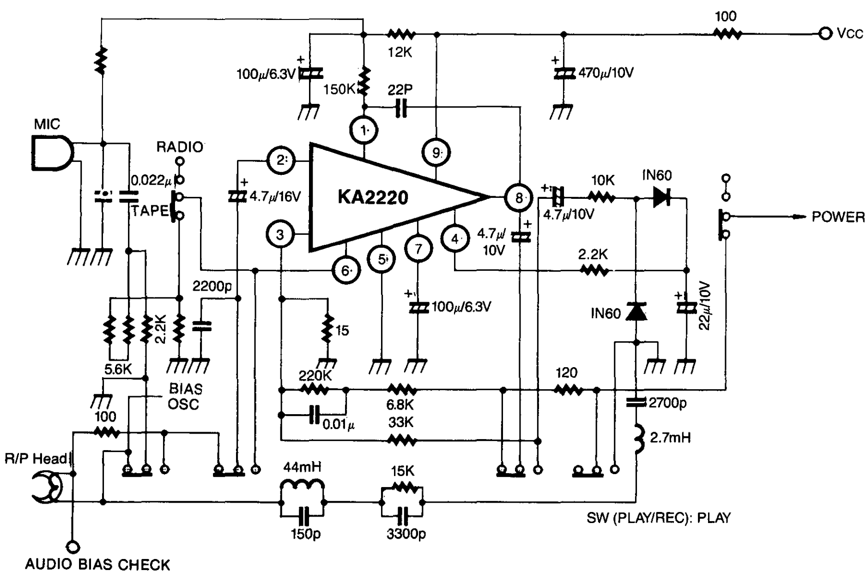


Fig. 4

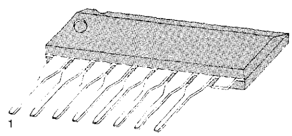
DUAL LOW NOISE EQUALIZER AMPLIFIER

The KA2221 is a monolithic integrated circuit consisting of 2-channel low noise amplifiers and regulated power supply for car stereos.

FEATURES

- Suitable for car stereos.
- **Low noise amplifier.**
- **Voltage regulator included.**
- **Good ripple rejection.**
- **High channel separation (65dB Typ).**
- **Minimum number of external parts required.**

8 SIP



ORDERING INFORMATION

Device	Package	Operating Temperature
KA2221	8 SIP	−20 ~ +70°C
KA2221G	PELLET	

SCHEMATIC DIAGRAM

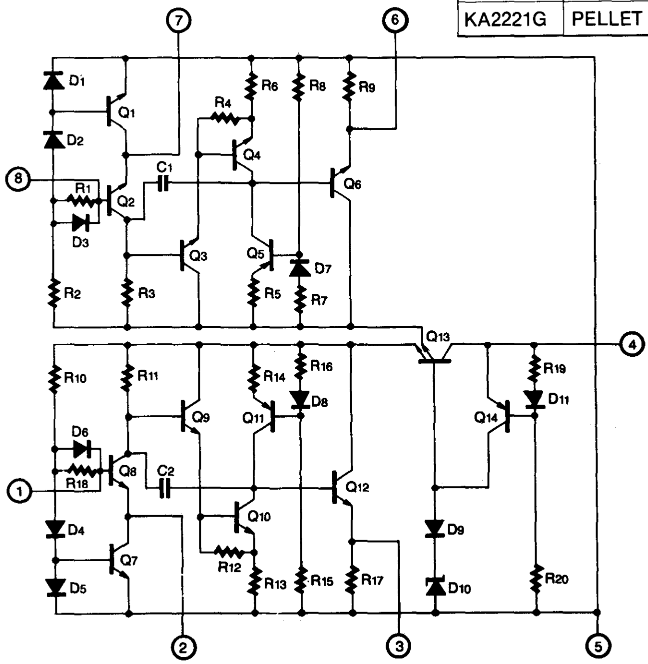


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Power Dissipation	P_d	200	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC}=12V, R_L=10KΩ, f=1KHz, NAB, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i=0		6.0	9.0	mA
Voltage Gain (Open Loop)	A_{VO}		65	80		dB
Voltage Gain (Closed Loop)	A_V	V_O=0.5V	33	35	37	dB
Output Voltage	V_O	THD=1%	0.6	1.0		V
Total Harmonic Distortion	THD	V_O=0.5V		0.1	0.3	%
Input Resistance	R_i			150		KΩ
Equivalent Input Noise Voltage	V_{NI}	R_g=2.2KΩ BW (−3dB) = 15Hz ~ 30KHz		1.0	2.0	μV
Cross Talk	CT	R_g = 2.2KΩ	50	65		dB

TEST CIRCUIT

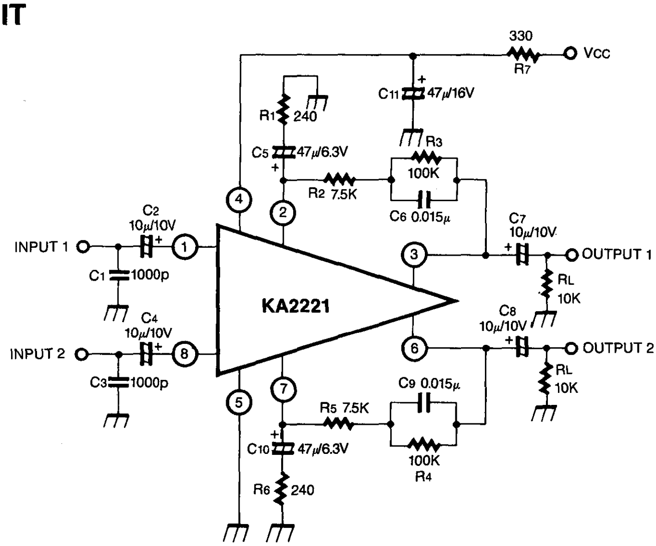
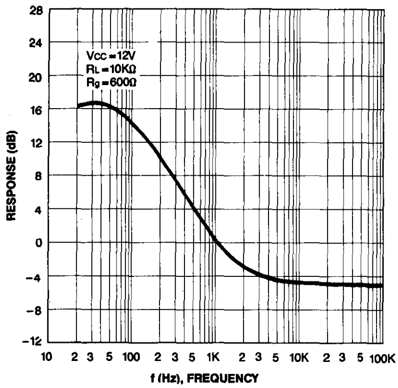
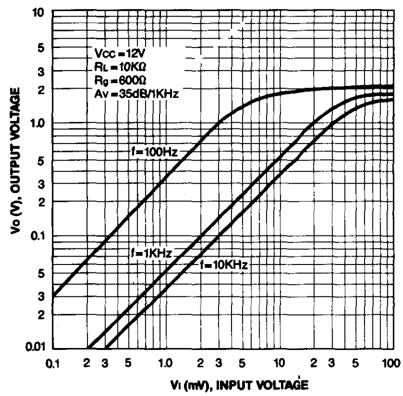


Fig. 2

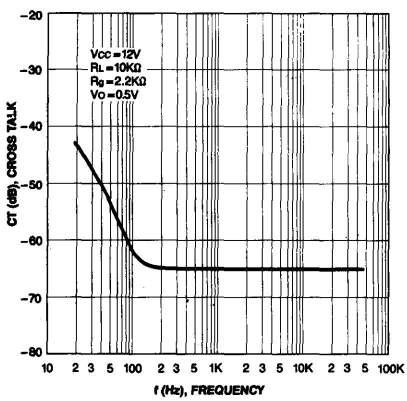
FREQUENCY RESPONSE



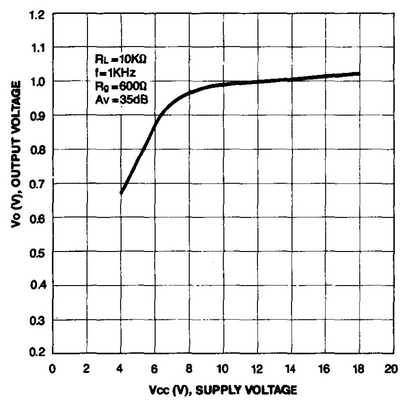
OUTPUT VOLTAGE-INPUT VOLTAGE



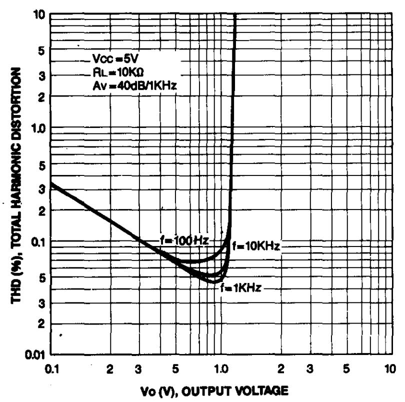
CROSS TALK-FREQUENCY



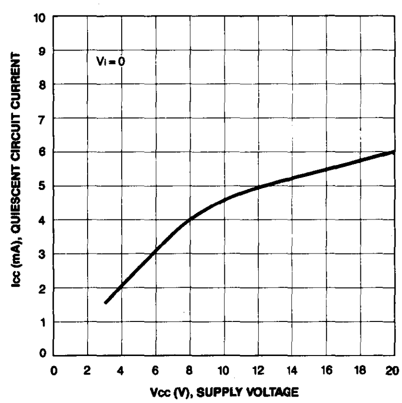
OUTPUT VOLTAGE-SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



External components (Refer to test circuits)

C_1 (C_3): Noise filter
These capacitors prevent radio interference in strong electric fields. The recommended value is 1000pF.

C_2 (C_4): Input coupling capacitor
The recommanded value is 10μF. If made too small, the low frequency characteristics will change for the worse, but too large a value will increase the rising time when power is applied.

C_5 (C_{10}): Negative feedback capacitor
The lower cut-off frequency depends on the value of these capacitors and is determined as follows:

$$C_5\ (C_{10}) = \frac{1}{2\pi f_L \cdot R_1\ (R_6)}$$

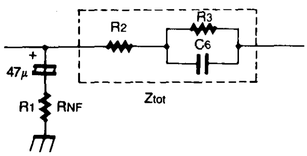
f_L: Low cut-off frequency
If the value of these capacitors is made larger, the starting time of amplifier is delayed further.

C_7 (C_8): Output coupling capacitor
The recommended value is 10μF.

R_2, R_3, C_6 (R_4, R_5, C_9): Equalizer network
The time constants of standard NAB characteristic are follow.

Tape speed	9.5cm/sec	4.75cm/sec
C_6 (R_2 + R_3)	3180μsec	1590μsec
R_2, C_6	90μsec	120μsec

R_1 (R_6): Feedback component
The closed loop gain is determined approximately by the following relationship:



$$A_v = 20 \log \frac{Z_{tot}}{R_{NF}} (dB)$$

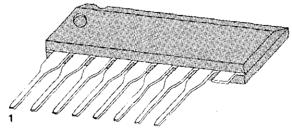
$$Z_{tot} = R_2 + R_3 // C_6$$

* Choose R_2, R_3, (DC resistance of NAB element) as 100KΩ approximately.

DUAL LOW NOISE EQUALIZER AMPLIFIER

The KA22211 is a monolithic integrated circuit consisting of a 2-channel pre-amplifier in a 8-pin plastic single in-line package.

8 SIP



FEATURES

- **Recommended operating supply voltage range (5V ~ 14V)**
- **Low noise (V_{NI} = 1.0μV: Typ)**
- **High channel separation**
- **Minimum number of external parts required**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22211	8 SIP	−20 ~ +70°C

SCHEMATIC DIAGRAM

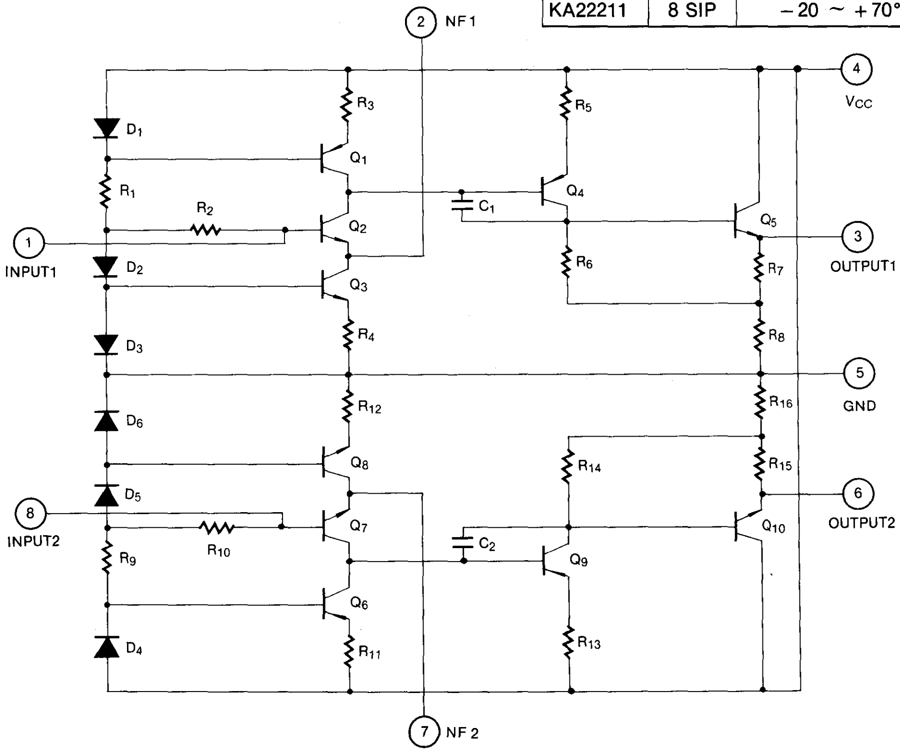


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Power Dissipation	P_d	200	mW
Operating Temperature	T_{opr}	− 20 ~ + 70	°C
Storage Temperature	T_{stg}	− 40 ~ + 125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 9V, R_L = 10KΩ, R_g = 600Ω, f = 1KHz, NAB, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i = 0		4.0	6.0	mA
Voltage Gain (Open Loop)	A_{VO}		65	80		dB
Voltage Gain (Closed Loop)	A_V	V_o = 0.5V	33	35	37	dB
Output Voltage	V_o	THD = 1%	1.1	1.3		V
Total Harmonic Distortion	THD	V_o = 0.5V		0.1	0.3	%
Input Resistance	R_i		70	100		KΩ
Equivalent Input Noise Voltage	V_{NI}	R_g = 2.2KΩ BW (− 3dB) = 15Hz ~ 30KHz		1.0	2.0	μV
Cross Talk	CT	R_g = 2.2KΩ	50	65		dB

TEST CIRCUIT

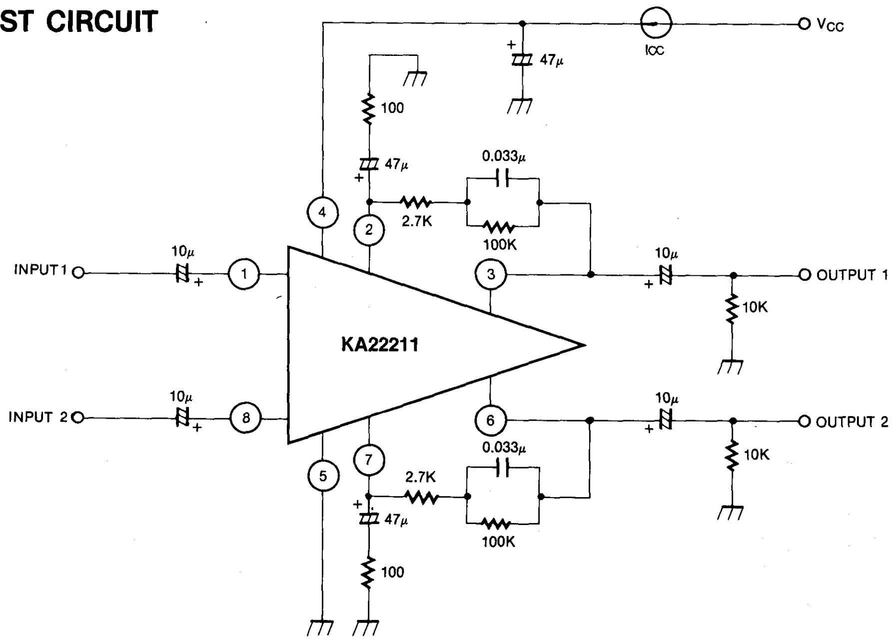


Fig. 2

APPLICATION CIRCUIT

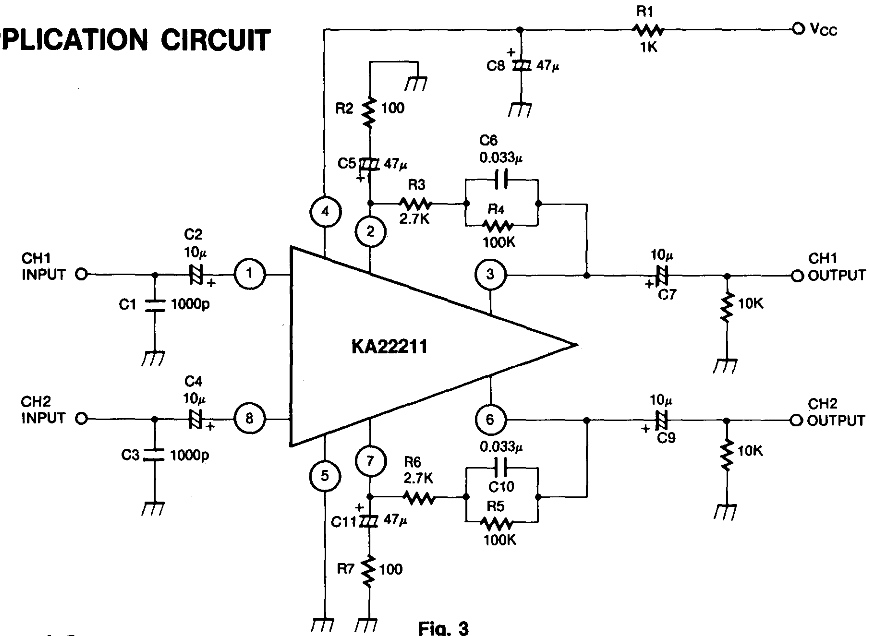


Fig. 3

External Components

C_2 (C_4): Input coupling capacitor
These components are concerned with the output noise and operation starting time, and its capacitance is adequate for 10μF.
As C_2 (C_4) below 4.7μF extends the operation starting time, a capacitance of over 4.7μF is recommended.

C_5 (C_{11}): Negative feedback capacitor
These components decide the low cut-off frequency, which is determined as follows:

$$C_5\ (C_{11}) = \frac{1}{2\pi f_L \cdot R_2 (R_7)}$$ where, f_L: low cut-off frequency.

A large C_5 (C_{11}) makes the operation starting time of an amplifier late. It's capacitance is adequate for 47μF.

C_6, R_4, R_3 (C_{10}, R_5, R_6): Equalizer network
This components decide the frequency response of an equalizer amplifier. The time constant of standard NAB characteristic is as follows:

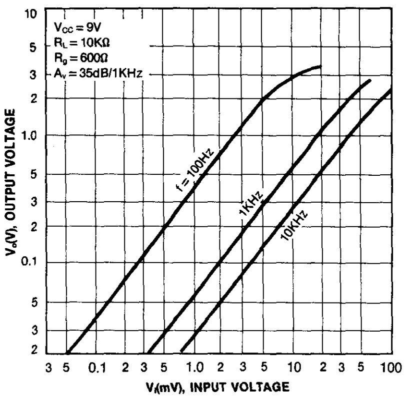
Tape Speed / Time Constant	9.5cm/sec	4.75cm/sec
C_6 ($R_3 + R_4$)	3,180μsec	1,590μsec
C_6, R_3	90μsec	120μsec

C_8: Filter capacitor of the power line
This should be located as close to the supply voltage pin (Pin 4) as possible. The recommended value is 47μF:

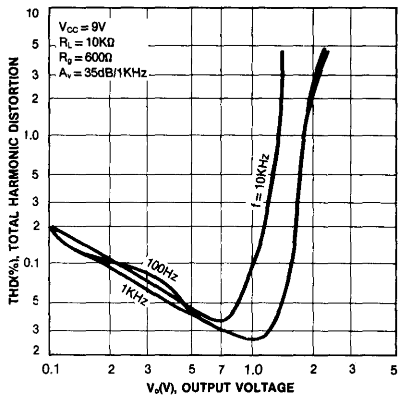
C_1 (C_3): Protection capacitor
These components protect against wave damage is strong electric fields and engine noise damage and block oscillation at high amplifying operation.

C_7 (C_9): Output coupling capacitor
The recommended value is 10μF.

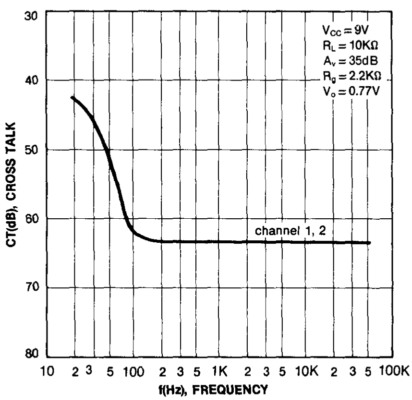
OUTPUT VOLTAGE-INPUT VOLTAGE



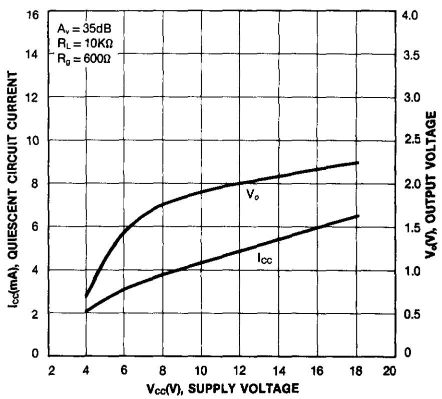
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



CROSS TALK-FREQUENCY



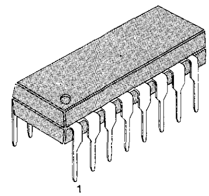
QUIESCENT CIRCUIT CURRENT·SUPPLY VOLTAGE
OUTPUT VOLTAGE



5-BAND GRAPHIC EQUALIZER AMPLIFIER

The KA2223 is a monolithic integrated circuit consisting of an operational amplifier with five resonant circuits and a active filter, and it is suitable for radio-cassette tape recorders, car stereos or music center audio systems.

16 DIP



FEATURES

- **Tone control with independent adjustment of each band through an external capacitor.**
- **Gain control through an external variable resistor.**
- **Increasing the bands by adding resonant circuit or using two KA2223 in series.**
- **Low noise (V_{NO} =7μV: Typ. Flat).**
- **Low distortion (THD=0.02% Typ. f=1KHz Flat).**
- **Large allowable input (V_i = 2.3V: Typ, V_{CC} =9V, f=1KHz Flat).**
- **Operating supply voltage (5V ~ 13V)**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2223	16 DIP	−20 ~ +70°C
KA2223G	PELLET	

SCHEMATIC DIAGRAM

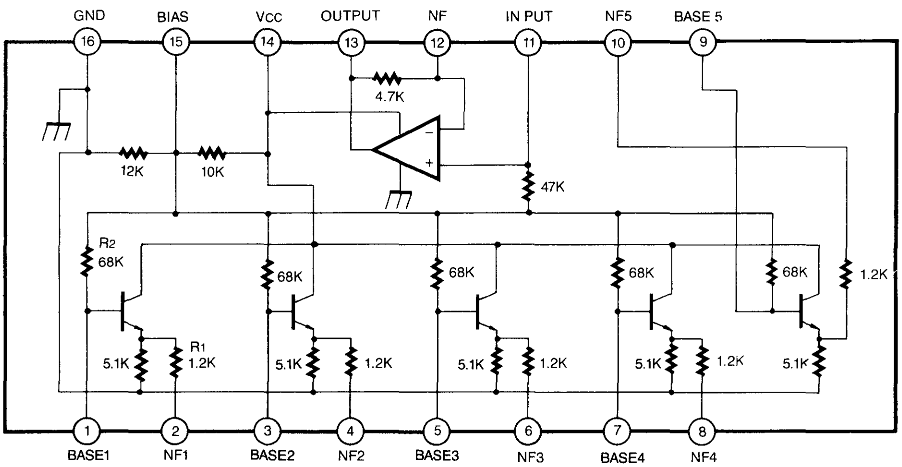


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	20	V
Power Dissipation	P_d	700	mW
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−55 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 9V unless otherwise specified)

Characteristic		Symbol	Test		Min	Typ	Max	Unit
			f(Hz)	Conditions				
Quiescent Circuit Current		I_{CC}		$V_i = 0$	3.0	5.2	8.0	mA
Voltage Gain	Flat	A_V (Flat)	1K	$V_i = -10dBm$	−3.8	−0.8	2.2	dB
	Boost	A_V (Boost)	108	$V_i = -10dBm$	8	10.5	12	dB
			343					dB
			1.08K					dB
			3.43K					dB
			10.8K					dB
	Cut	A_V (Cut)	108	$V_i = -10dBm$	−12	−10.5	−8	dB
			343					dB
			1.08K					dB
			3.43K					dB
			10.8K					dB
Total Harmonic Distortion		THD	1K	$V_i = 1V$		0.02	0.1	%
Output Noise Voltage		V_{NO}	Flat, Input Short BW(−3dB) = 10Hz ~ 30KHz			7.0	30	μV

TYPICAL APPLICATION CIRCUIT

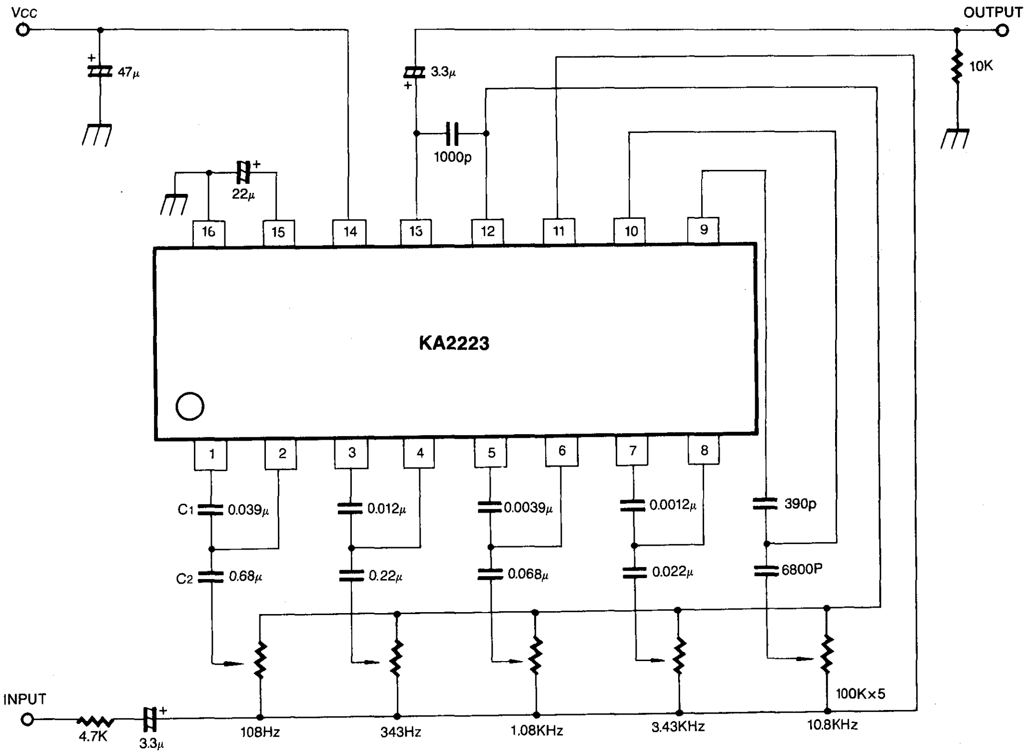


Fig. 4

$$\text{Resonant frequency } f_O = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

(R_1 =1.2K, R_2=68K on-chip resistor)

APPLICATION CIRCUIT 1 (7-Band)

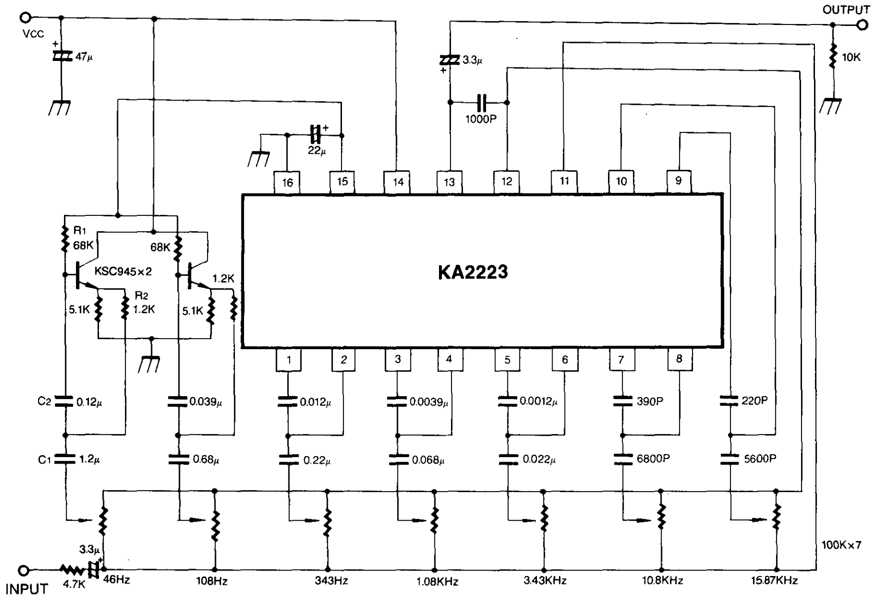


Fig. 2

APPLICATION CIRCUIT 2 (10-Band)

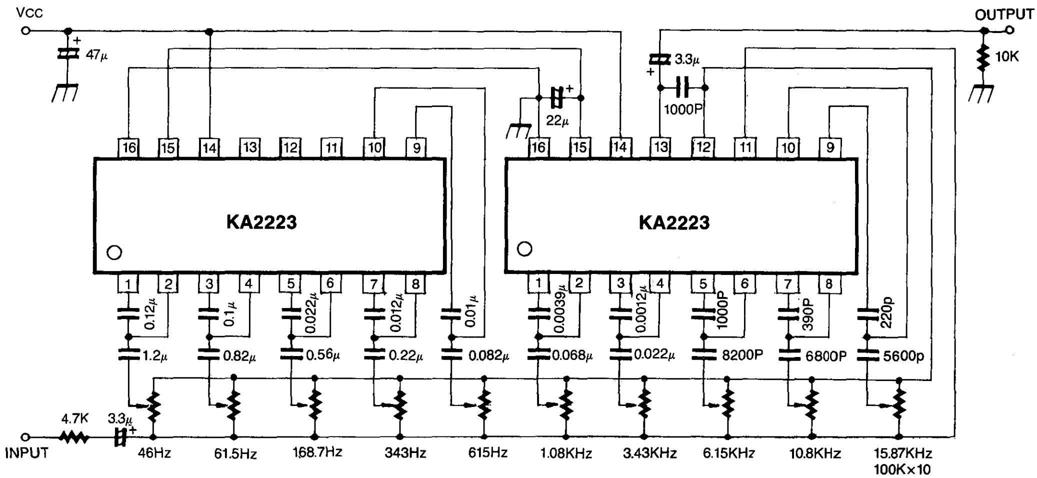
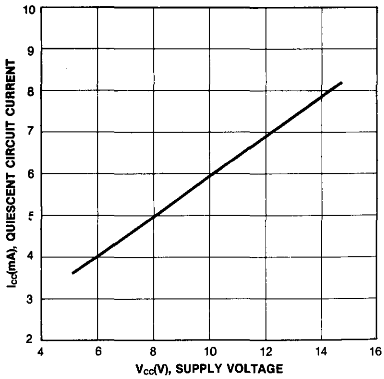
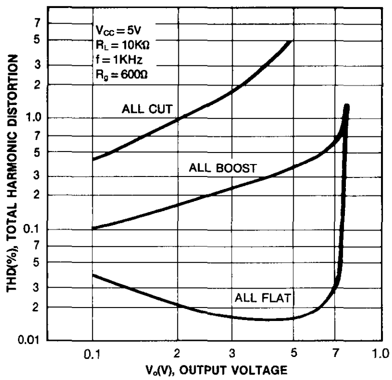


Fig. 3

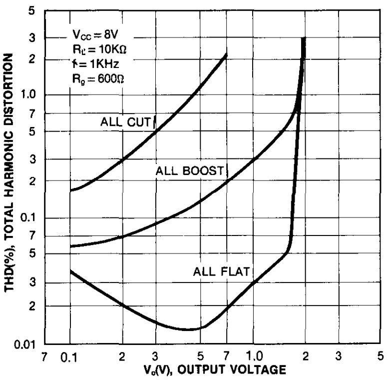
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



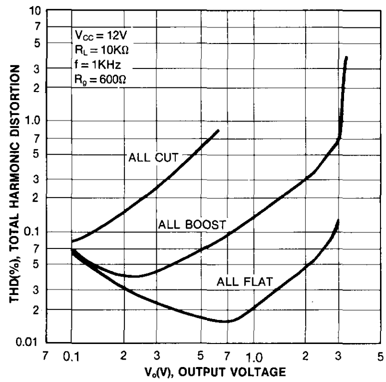
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



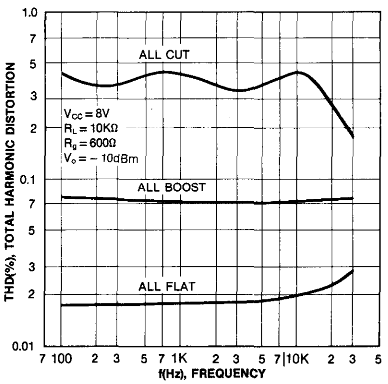
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



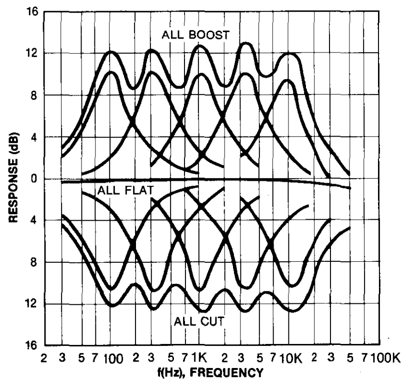
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



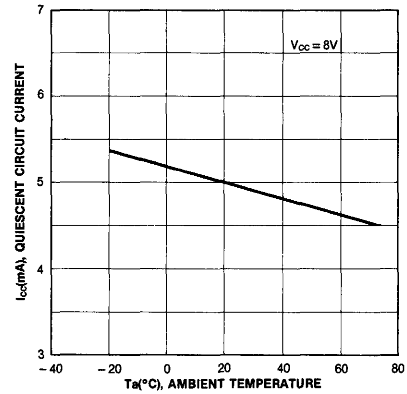
TOTAL HARMONIC DISTORTION-FREQUENCY



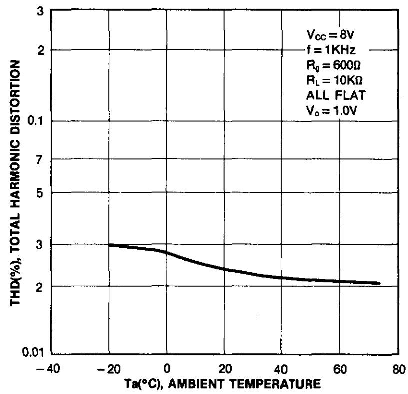
FREQUENCY RESPONSE



QUIESCENT CIRCUIT CURRENT-AMBIENT TEMPERATURE



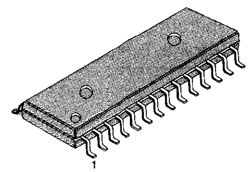
TOTAL HARMONIC DISTORTION -AMBIENT TEMPERATURE



5-BAND DUAL GRAPHIC EQUALIZER AMPLIFIER

The KA22231 is a monolithic integrated circuit consisting of an operational amplifier and 5 resonant circuits with an active filter.
It is suitable for 3V headphone stereos and mini radio cassette tape recorders.

28 SOP



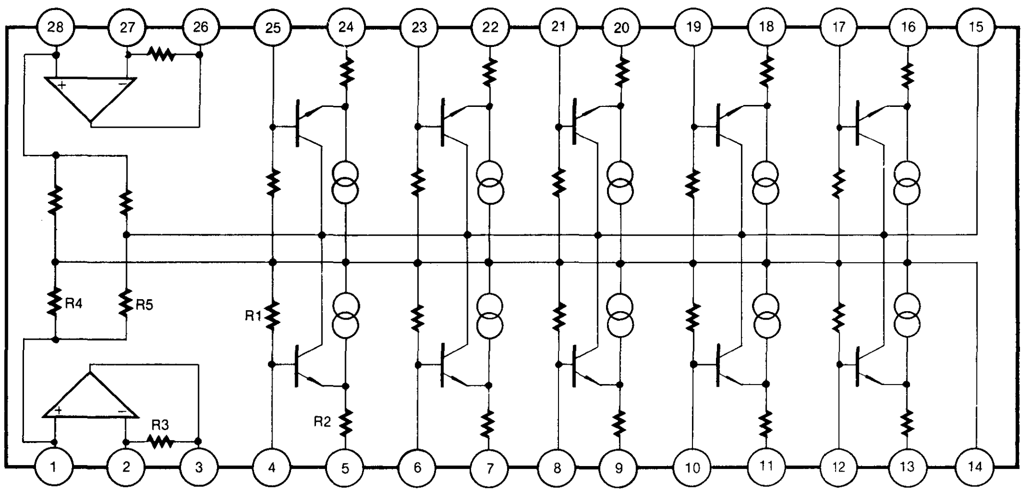
FEATURES

- **Tone control with independent adjustment of each band through external an capacitor**
- **Gain control through an external variable resistor (Gain = ±9dB)**
- **Low noise (V_{NO} = 4μV, Typ at f = 1KHz, Flat)**
- **Low distortion (THD = 0.04% Typ. at f = 1KHz, Flat)**
- **Low current dissipation (I_{CC} = 4mA Typ at Vi = 0)**
- **Operating supply voltage range: V_{CC} = 1.6V ~ 6V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22231D	28 SOP	−20 ~ +70°C

BLOCK DIAGRAM



Note: R1 = 68K R2 = 1.2K R3 = 4.7K R4 = 13.5K R5 = 13K

Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

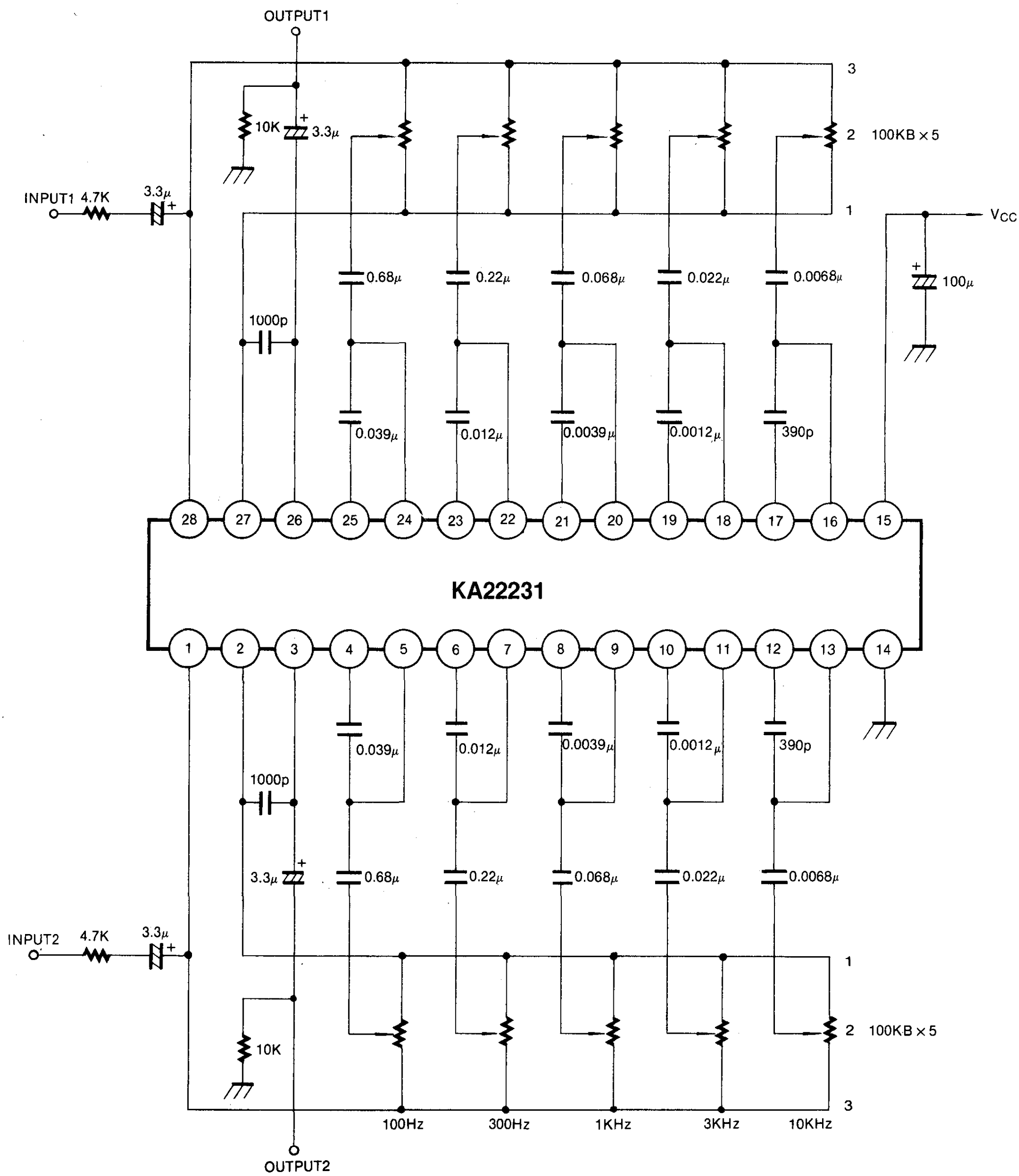
Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	8	V
Power Dissipation	P_d	300	mW
Operating Temperature	T_{opr}	− 20 ~ + 70	°C
Storage Temperature	T_{stg}	− 40 ~ + 125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 3V, R_L = 10KΩ, unless otherwise specified)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
			f(Hz)	Condition				
Quiescent Circuit Current		I_{CC}		$V_i = 0$	2.0	4.0	8.0	mA
Output Voltage		V_O	1K	THD = 1%	500	800		mV
Total Harmonic Distortion		THD	1K	V_O = 300mV		0.04	0.1	%
Channel Balance		CB	1K		− 1.0	0	1.0	dB
Cross Talk		CT	1K	$R_g = 0$	40	50		dB
Output Noise Voltage		V_{NO}	Flat, Input Short BW(− 3dB) = 10Hz ~ 30KHz			4.0	20	μV
Voltage Gain	Flat	A_V(Flat)	1K	V_i = 100mV	− 4.0	− 1.0	2.0	dB
	Boost	A_V(Boost)	100 340 1K 3.4K 10K	V_i = 100mV	8.0	10.0	12.0	dB
	Cut	A_V(Cut)	100 340 1K 3.4K 10K	V_i = 100mV	− 12.0	− 10.0	− 8.0	dB

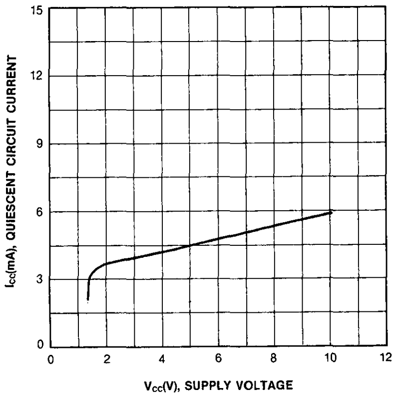
TYPICAL APPLICATION CIRCUIT



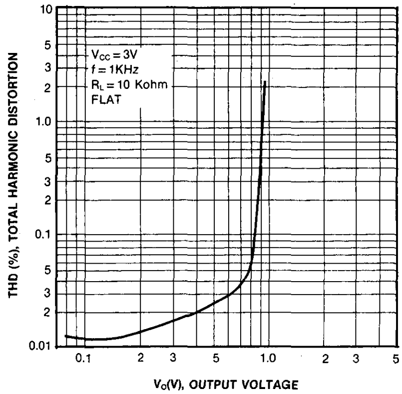
Note. Point 1: Boost, Point 2: Flat, Point 3: Cut

Fig. 2

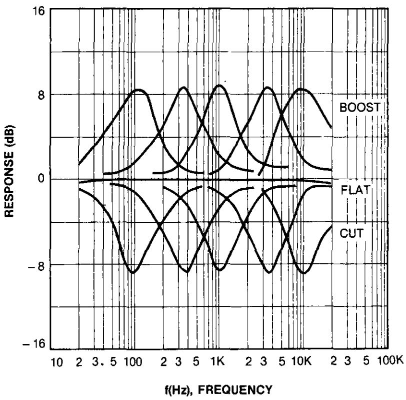
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



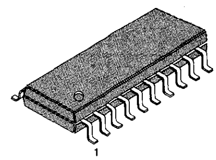
FREQUENCY RESPONSE



3-BAND DUAL GRAPHIC EQUALIZER AMPLIFIER

The KA22232 is a monolithic integrated circuit consisting of an operational amplifier and three resonant circuits with an active filter.
It is suitable for 3V headphone stereos and mini radio cassette tape recorders.

20 SOP



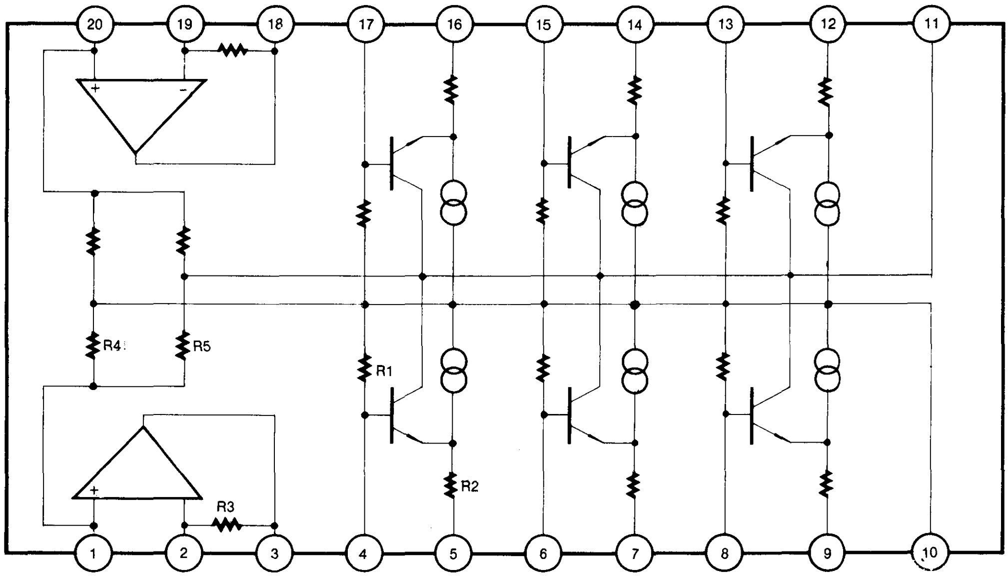
FEATURES

- **Tone control with independent adjustment of each band through an external capacitor**
- **Gain control through an external variable resistor (Gain = ± 9dB)**
- **Low noise ($V_{NO} = 4\mu V$, Typ at Flat)**
- **Low distortion (THD = 0.04% Typ. at f = 1KHz, Flat)**
- **Low current dissipation ($I_{CC} = 4mA$ Typ at Vi = 0)**
- **Operating supply voltage range: $V_{CC} = 1.6V \sim 6V$**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22232D	20 SOP	− 20 ~ + 70°C

BLOCK DIAGRAM



Note:R1 = 68K R2 = 1.2K R3 = 4.7K R4 = 13.5K R5 = 13K

Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

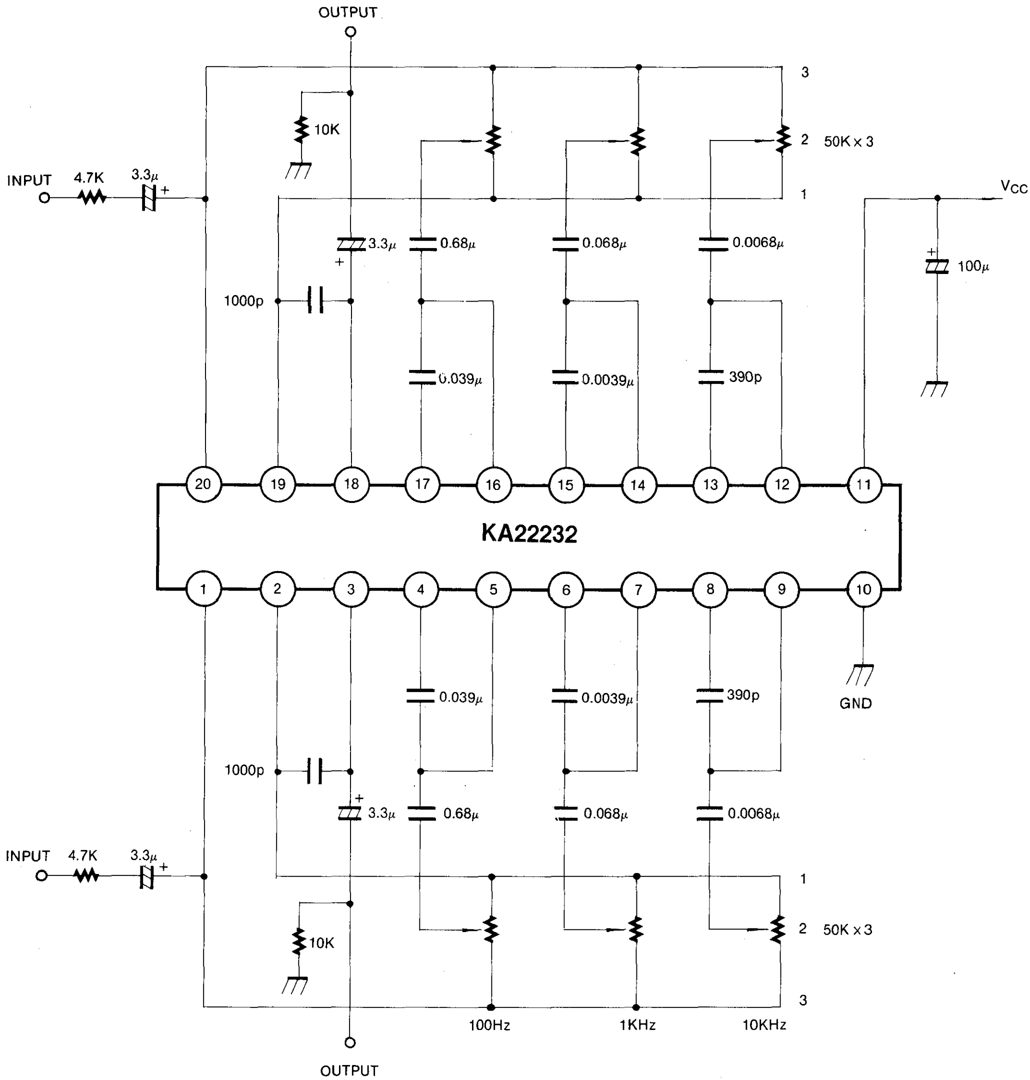
Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	8	V
Power Dissipation	P_d	300	mW
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 3V, f = 1KHz, V_i = 100mV, R_L = 10KΩ, VR = Flat, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	$V_i = 0$	2	4	8	mA
Maximum Input Voltage	V_i (max)	THD = 1%	500	800		mV
Total Harmonic Distortion	THD			0.04	0.1	%
Voltage Gain	A_V		−4	−1	2	dB
Control Range	CR		±7	±9	±11	dB
Cross Talk	CT	$R_g = 0$	40	50		dB
Channel Balance	CB		−1	0	1	dB
Output Noise Voltage	V_{NO}	BW (−3dB) = 20Hz ~ 20KHz		4	20	μV

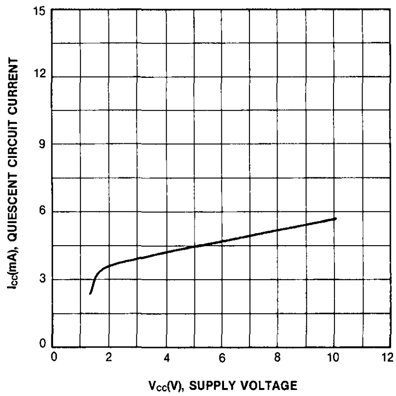
TYPICAL APPLICATION CIRCUIT



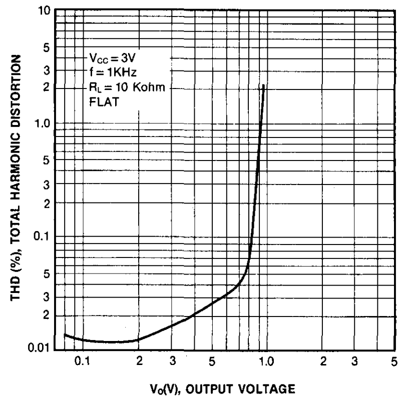
Note. Point 1: Boost,
Point 2: Flat,
Point 3: Cut

Fig. 2

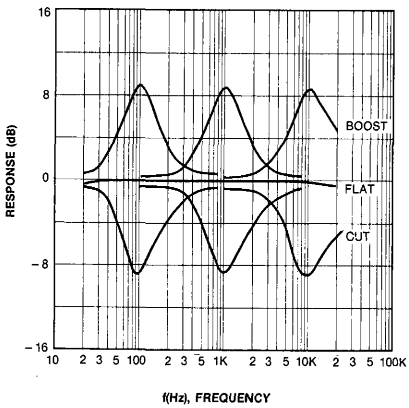
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



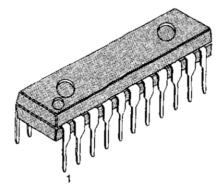
FREQUENCY RESPONSE



3-BAND DUAL GRAPHIC EQUALIZER AMPLIFIER

The KA22233 is a monolithic integrated circuit consisting of an operational amplifier, three resonant circuits with an active filter, and it is suitable for radio cassette recorders, car stereos or music centers and audio systems.

22 DIP



FEATURES

- **Tone control with independent adjustment of each band through an external capacitor.**
- **Gain control through an external variable resistor.**
- **Increasing the bands by adding resonant circuit or using two KA22233 in series.**
- **Low noise (V_{NO}=7μV Typ, at Flat).**
- **Low distortion (THD=0.02% Typ, at f=1KHz, Flat).**
- **Large allowable input (V_i=2.3V Typ, at V_{CC}=9V, f=1KHz, Flat).**
- **Wide operating supply voltage range: V_{CC}=5V ~ 15V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22233	22 DIP	−20 ~ +70°C

SCHEMATIC DIAGRAM

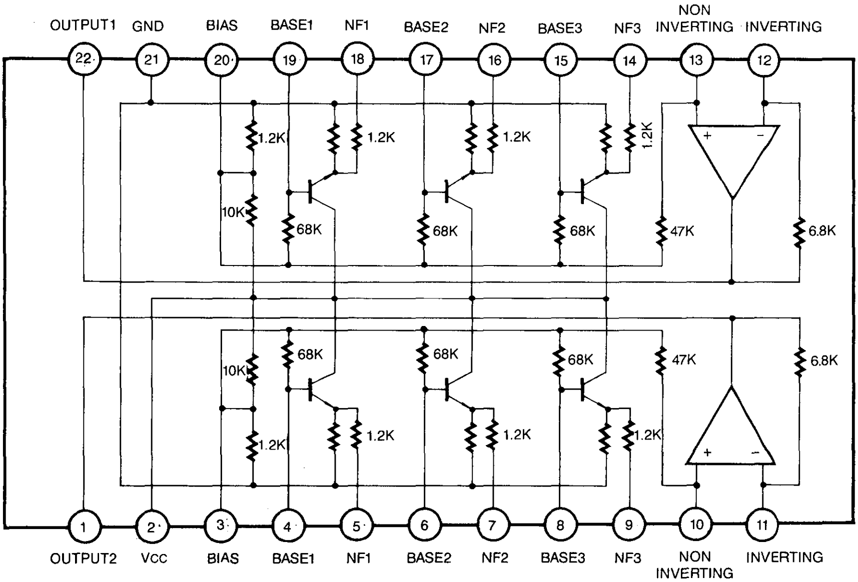


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	20	V
Power Dissipation	P_d	700	mW
Operating Temperature	T_{opr}	− 20 ~ + 70	°C
Storage Temperature	T_{stg}	− 40 ~ + 125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 9V, Rg = 600Ω, R_L = 10KΩ, unless otherwise specified)

Characteristic		Symbol	Test		Min	Typ	Max	Unit
			f (Hz)	Conditions				
Quiescent Circuit Current		I_{CC}		V_i = 0	5.0	7.2	10.0	mA
Voltage Gain	Flat	A_V (Flat)	1K	V_i = − 10dBm	− 2.5	− 0.5	+ 1.5	dB
	Boost	A_V (Boost)	108	V_i = − 10dBm	10.5	12.5	14.5	dB
			1.08K					
			10.8K					
	Cut	A_V (Cut)	108	V_i = − 10dBm	− 14.5	− 12.5	− 10.5	dB
			1.08K					
			10.8K					
Total Harmonic Distortion		THD	1K	V_i = 1V		0.02	0.1	%
Output Noise Voltage		V_{NO}	Flat, Input Short BW(− 3dB) = 10Hz ~ 30KHz			7.0	30	μV
Channel Balance		CB	1K	V_i = 1V	− 2.0	0	+ 2.0	dB
Cross Talk		CT	1K	V_i = 1V		70		dB

3

APPLICATION CIRCUIT

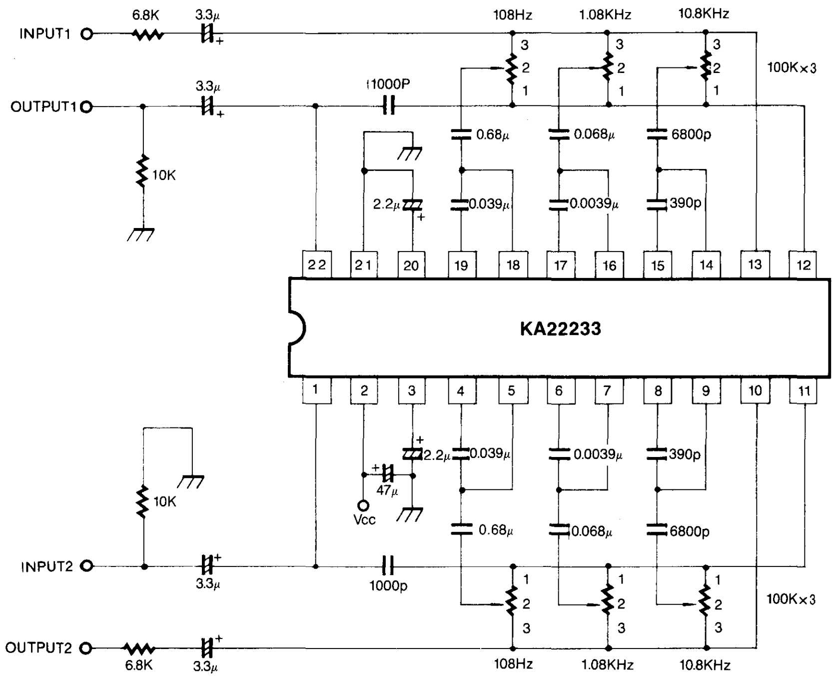
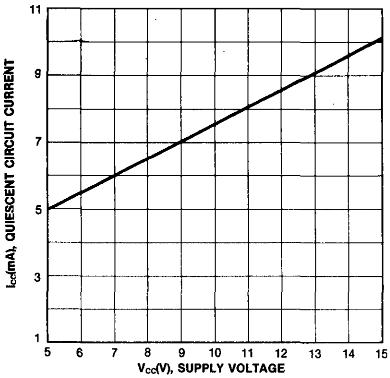


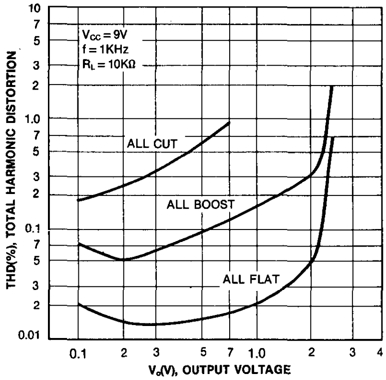
Fig. 2

Note: Volume Function
Position 1: Boost
Position 2: Flat
Position 3: Cut

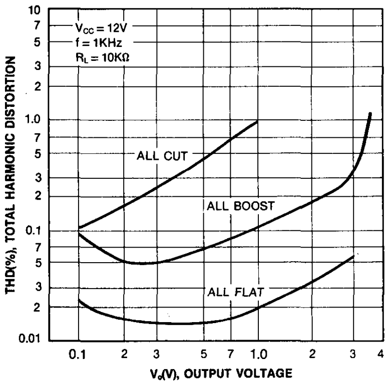
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



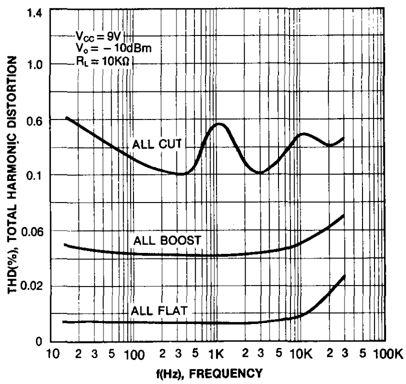
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



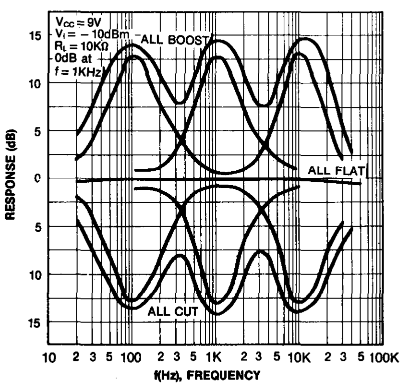
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



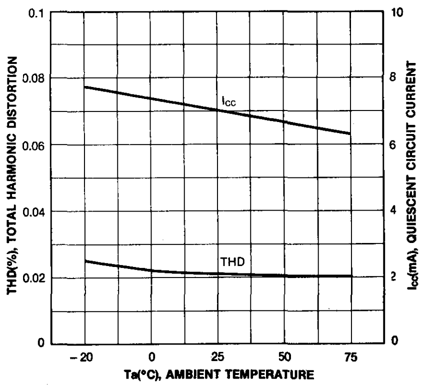
TOTAL HARMONIC DISTORTION-FREQUENCY



FREQUENCY RESPONSE



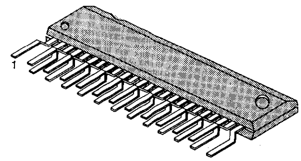
TOTAL HARMONIC DISTORTION·AMBIENT TEMPERATURE
QUIESCENT CIRCUIT CURRENT



5-BAND DUAL GRAPHIC EQUALIZER AMPLIFIER

The KA22234 is a monolithic integrated circuit developed for the stereo 5 band graphic equalizer amplifier. It is consisting of an operational amplifier, four resonant circuits with an active filter, and it is suitable for radio cassettes, car stereos or music centers.

24 ZSIP



FEATURES

- **Tone control with independent adjustment of each band through an external capacitor**
- **Gain control through an external variable resistor (Gain = ±11dB)**
- **Excellent cross talk characteristic (CT = 70dB Typ, at $R_g = 0$)**
- **Wide operating supply voltage range: V_{CC} = 3.5V ~ 14V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22234	24 ZSIP	−20 ~ +70°C

BLOCK DIAGRAM

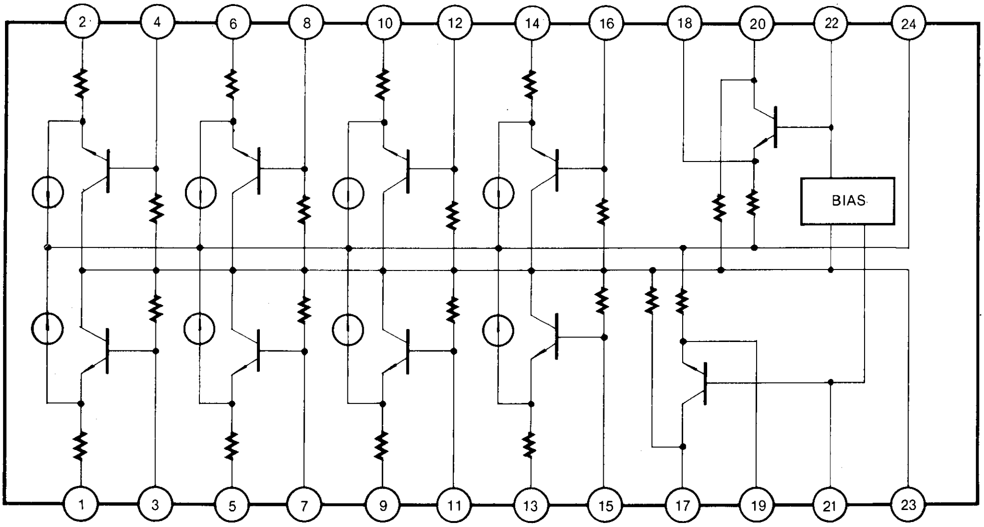


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Power Dissipation	P_d	500	mW
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 8V, R_L = 20KΩ, Flat Mode, unless otherwise specified)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
			f(Hz)	Condition				
Quiescent Circuit Current		I_{CC}		$V_i = 0$	4.0	7.0	10.0	mA
Output Voltage		V_O	1K	THD = 1%	500	600		mV
Total Harmonic Distortion		THD	1K			0.1	0.3	%
Channel Balance		CB	1K		−1.0	0	1.0	dB
Cross Talk		CT	1K		50	70		dB
Output Noise Voltage		V_{NO}	Flat, R_g = 2.2KΩ BW(−3dB) = 10Hz ~ 30KHz			10	20	μV
Voltage Gain	Flat	A_V(Flat)	1K	V_i = 100mV	−2.0	−1.5	1.0	dB
	Boost	A_V(Boost)	100	V_i = 100mV	9.0	11.0	14.0	dB
			300					
			1K					
			3K					
			10K					
	Cut	A_V(Cut)	100	V_i = 100mV	−14.0	−11.0	−9.0	dB
			300					
			1K					
			3K					
			10K					

TYPICAL APPLICATION CIRCUIT

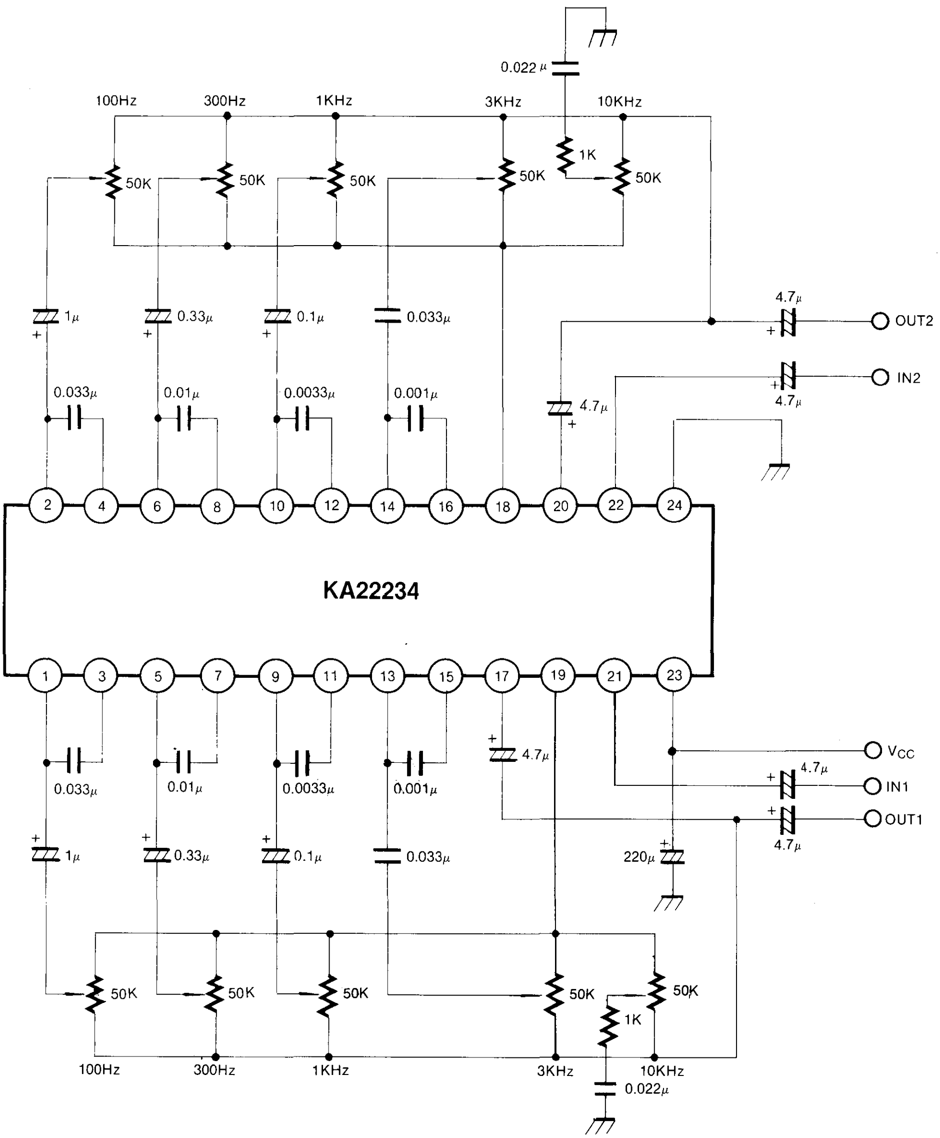
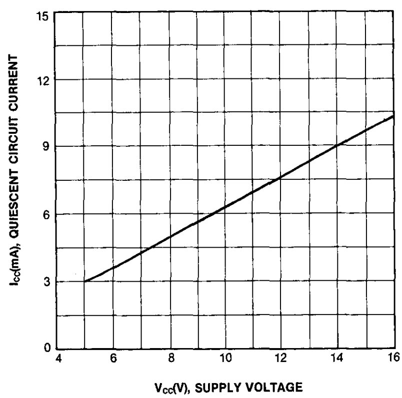
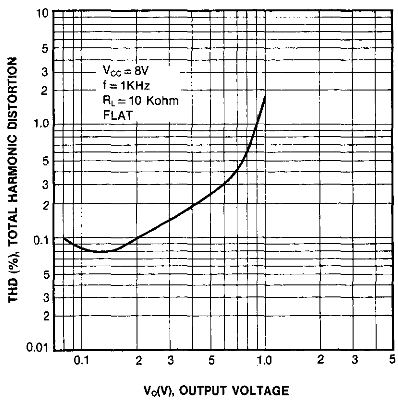


Fig. 2

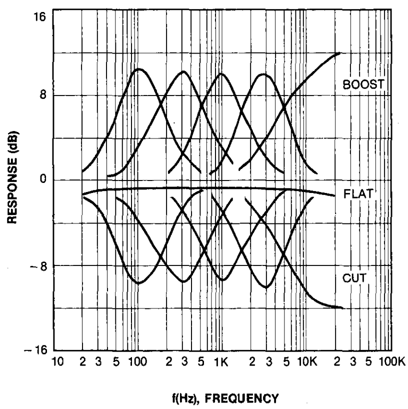
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



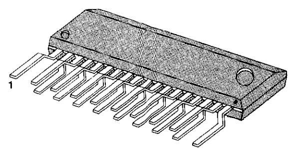
FREQUENCY RESPONSE



5-BAND GRAPHIC EQUALIZER AMPLIFIER

The KA22235 is a monolithic integrated circuit consisting of an operational amplifier, five resonant circuits with an active filter, and it is suitable for radio cassette tape recorders, car stereos or music center audio systems.

18 ZSIP



FEATURES

- **Low peripheral parts.**
- **Low distortion (THD = 0.01% Typ. f = 1KHz Flat).**
- **Low noise (V_{NO} = 7μV Typ. Flat).**
- **Wide operating voltage range: V_{CC} = 3.5V ~ 16V.**
- **Recommended supply voltage: V_{CC} = 5V ~ 14V.**
- **Low current: I_{CC} = 5mA (Typ).**
- **Large allowable input (V_i = 2.1V Typ. V_{CC} = 8V, f = 1KHz Flat).**
- **Increasing the bands by adding resonant circuit or using two KA22235 in series.**
- **Built in input buffer, output buffer.**

APPLICATIONS

- Radio Cassettes
- Home Stereos
- Car Stereos

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22235	18 ZSIP	− 20 ~ + 70°C

BLOCK DIAGRAM

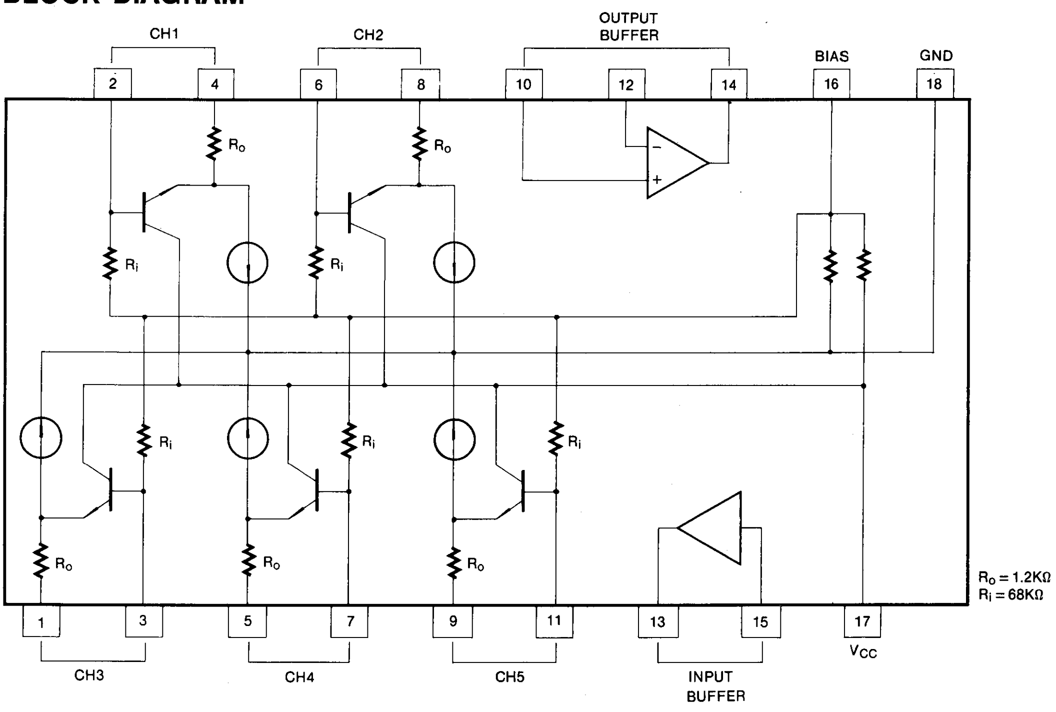


Fig. 1

ABSOLUTE MAXIMUM RATINGS ($Ta = 25°C$)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_d	550	mW
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

($Ta = 25°C$, $V_{CC} = 8V$, unless otherwise specified)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
			f(Hz)	Condition				
Circuit Current		I_{CC}		$V_i = 0$	3.0	5.0	8.0	mA
Output Voltage		V_o	1K	THD = 1%	1.5	2.1		V
Total Harmonic Distortion		THD	1K	$V_o = 120mV$		0.01	0.1	%
Output Noise Voltage		V_{NO}		$R_g = 0$, Flat BW(−3dB)=10Hz ~ 30KHz		7.0	30	μV
Voltage Gain	Flat	A_V (Flat)	1K	$V_i = 200mV$	−2.5	0.5	1.5	dB
	Boost	A_V (Boost)	100, 300, 1K, 3K, 10K	$V_i = 200mV$	10.5	12.5	14.5	dB
	Cut	A_v (Cut)	100, 300, 1K, 3K, 10K	$V_i = 200mV$	−14.5	−12.5	−10.5	dB

TEST CIRCUIT

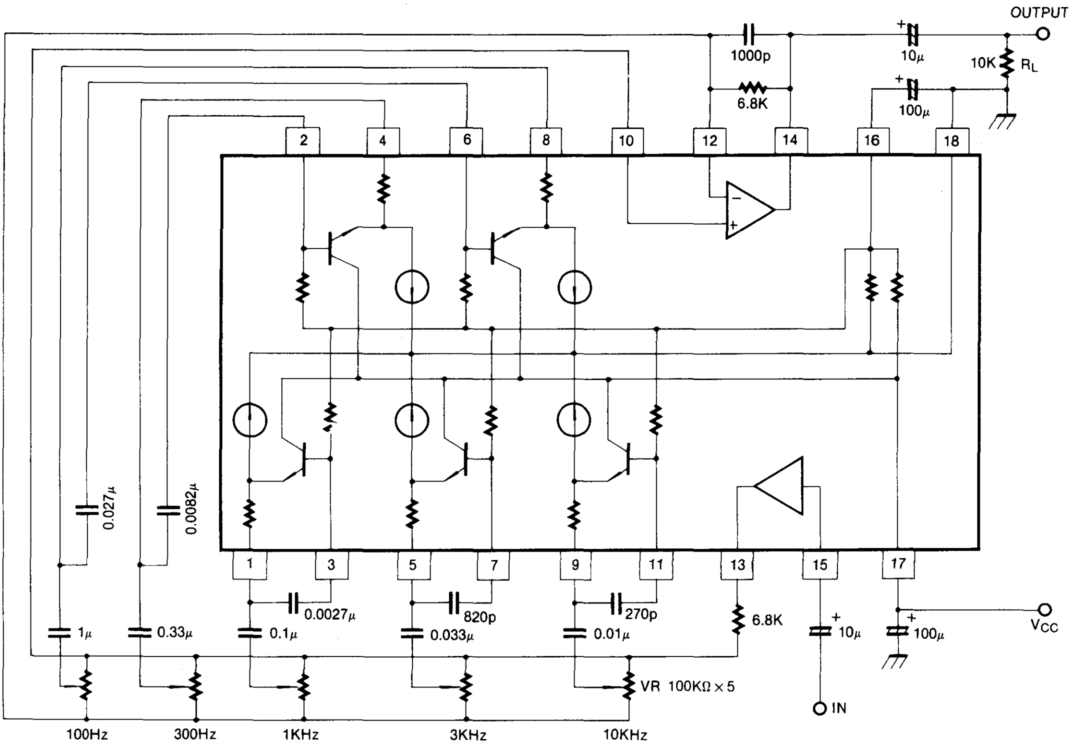


Fig. 2

APPLICATION CIRCUIT

(1) 10-Band Graphic Equalizer

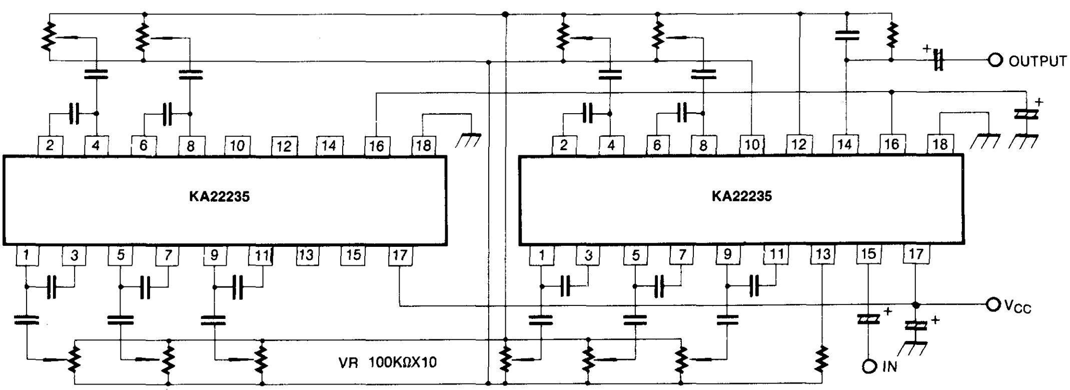


Fig. 3

(2) 7-Band Dual Graphic Equalizer

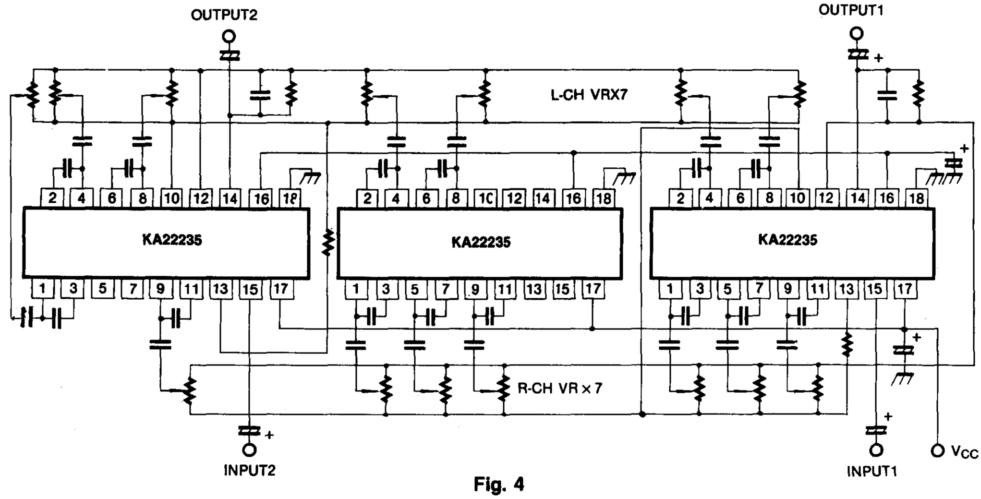


Fig. 4

SIMULATED INDUCTOR

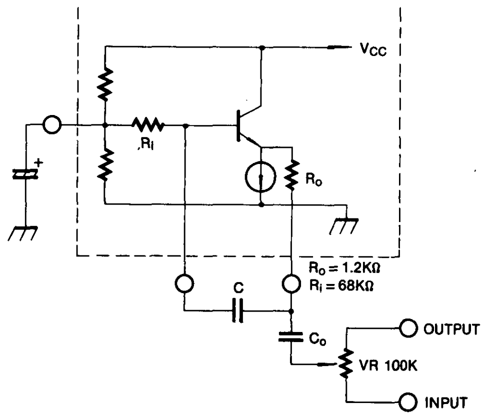


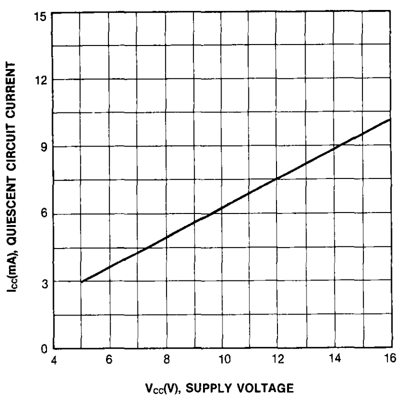
Fig. 5

As shown in Fig. 5, resonant frequency fo, and selectivity Q are determined by the external capacitor, C, C_o, and built-in resistor, R, R_o, as follows:

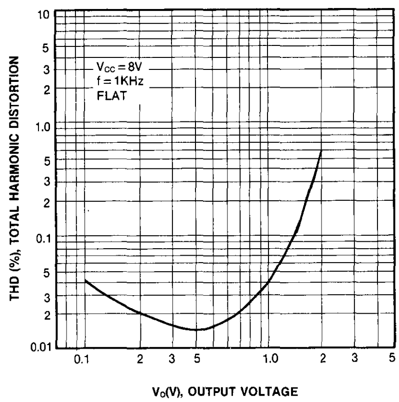
$$f_o(\text{Hz}) = \frac{1}{2\pi\sqrt{R_o R_i C C_o}} \qquad Q = \sqrt{\frac{CR_o}{C_o R_i}}$$

where $R_i = 68K\Omega$, $R_o = 1.2K\Omega$

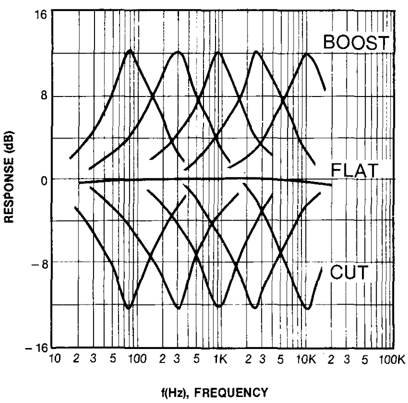
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



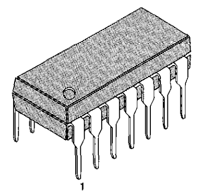
FREQUENCY RESPONSE



DUAL EQUALIZER AMPLIFIER WITH ALC

The KA2224 is a monolithic integrated circuit consisting of a dual equalizer amplifier with ALC, and it is suitable for stereo radio cassettes.

14 DIP



FEATURES

- Dual equalizer amplifier with a built-in ALC circuit.
- **Recording amp available because of high gain characteristic (Variable monitor possible).**
- **Good channel separation (Sep=50dB Typ).**
- **Quick stabilization after power on.**
- **Capable of direct meter driving and ALC transistor.**
- **Good ALC response balance between channels.**
- **Wide operating supply voltage range (4V ~ 13V).**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2224	14 DIP	−20 ~ +70°C
KA2224G	PELLET	

BLOCK DIAGRAM

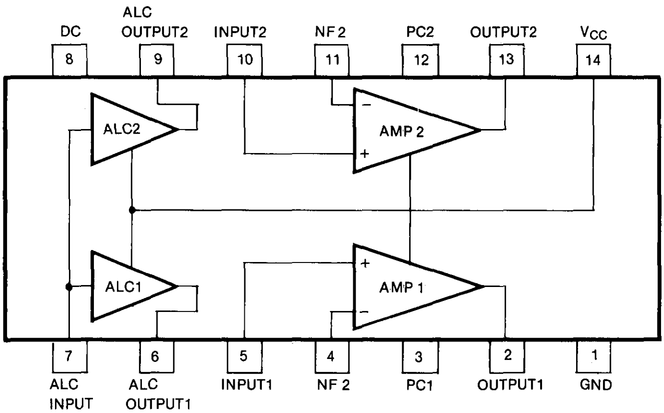


Fig. 1

3

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	14	V
Power Dissipation	P_d	600	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C
ALC TR Maximum Current		3.5	mA

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 5V, R_L = 10KΩ, f = 1KHz: play, R_L = 680Ω: Recording)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i=0		4.5	10	mA
Voltage Gain (Open Loop)	A_{VO}			85		dB
Voltage Gain (Closed Loop)	A_{V1}	Play		40		dB
	A_{V2}	Record		58		dB
Output Voltage	V_O	THD=1%, Play	0.9	1.2		V
Total Harmonic Distortion	THD	V_O=0.5V, Play		0.1	1.0	%
Input Resistance	R_i		21	30		KΩ
Equivalent Input Noise Voltage	V_{NI}	BW (−3dB) =20Hz ~ 20KHz		1.0	2.0	μV
Cross Talk	CT	Rg=2.2KΩ	40	50		dB
ALC Range	ALC (R)	V_i=−60dBm, Record	35	45		dB
ALC Balance	ALC (B)	V_i=−20dBm, Record		0	2.0	dB
ALC Distortion	ALC (THD)	V_i=−20dBm, Record		0.5	2.0	%

TEST CIRCUIT

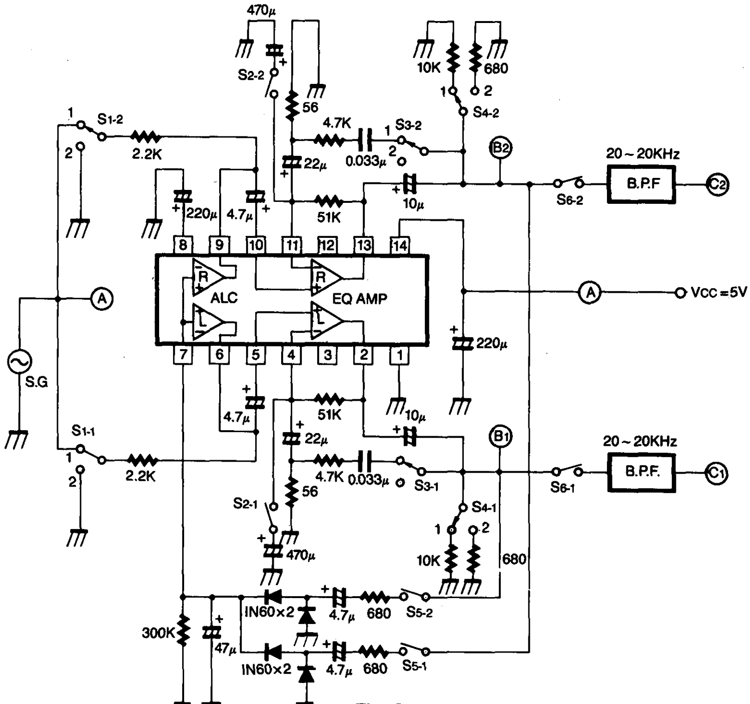


Fig. 2

TEST METHODS

Characteristic	S1	S2	S3	S4	S5	S6	Test Point	Test Method
I_{CC}	2	off	off	1	off	off		
A_{VO}	1	on	off	1	off	off	A, B	$A_{VO}=20 \log V_O/V_i$ (dB) with Input voltage V_i, output voltage at V_O
A_V	1	off	on	1	off	off	A, B	$A_V=20 \log V_O/V_i$ (dB)
V_O	1	off	on	1	off	off	B	Measure output voltage V_O at THD=1%
THD	1	off	on	1	off	off	B	Measure distortion factor at $V_O=0.5V$
CT	S1-1 S1-2 1 2 2 1	off	on	1	off	off	B	Measure crosstalk of amp 1,2 at output voltage $V_O=0$ dBm
V_{NI}	2	off	on	1	off	on	C	Convert output noise voltage at 1KHz gain when $R_g=2.2K\Omega$
ALC Range	1	off	off	2	on	off	B	Input voltage range from when input voltage $V_i=-60$dBm until output voltage V_O goes up 3 dB.
ALC Balance	1	off	off	2	on	off	B	Output voltage V_O level difference of amp 1, 2 when input voltage $V_i=-20$dBm is applied.
ALC Distortion	1	off	off	2	on	off	B	Measure distortion factor when input voltage $V_i=-20$dBm is applied.

TYPICAL APPLICATION CIRCUIT

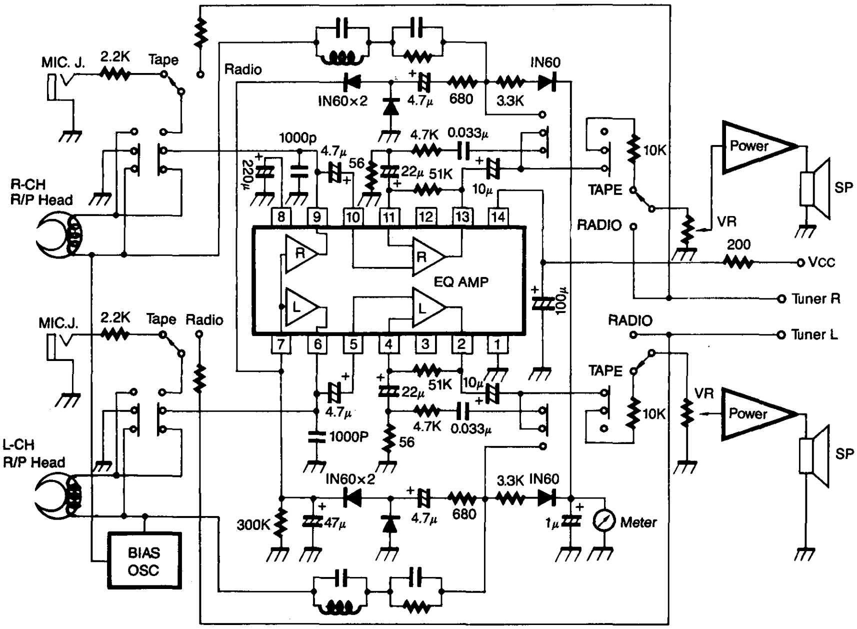


Fig.3

GENERAL OPERATING CONSIDERATIONS

1. Closed loop voltage gain

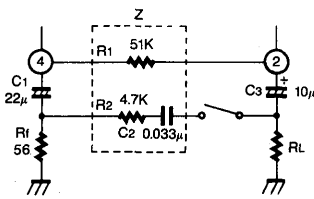


Fig. 4

SW on: play
off: record

A. Playback amplifier

$$Av = 20 \log \frac{Z}{Rf} \text{ (dB) at f=1KHz, Av=42dB (Typ)} \quad Z = R_1 // (R_2 + \frac{1}{2\pi f \cdot C_2})$$

B. Recording amplifier

$$Av = 20 \log \frac{R_1}{Rf} \text{ (dB) at f=1KHz, Av=58dB (Typ)}$$

2. ALC Circuit

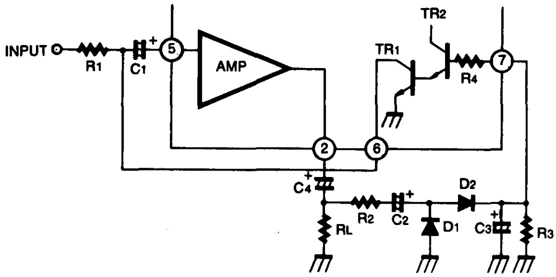


Fig. 5

The ALC circuit is consist of TR_1, TR_2 and some external components. The output level of the amplifier is rectified by external circuits. Since this DC level is applied to the ALC input terminal (Pin 7), the impedance between the collector and emitter of TR1 can change its value, therefore the pre-amplifier input level can be controlled.

3. Oscillation Suppression

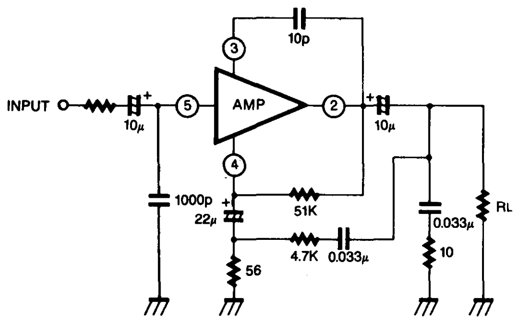
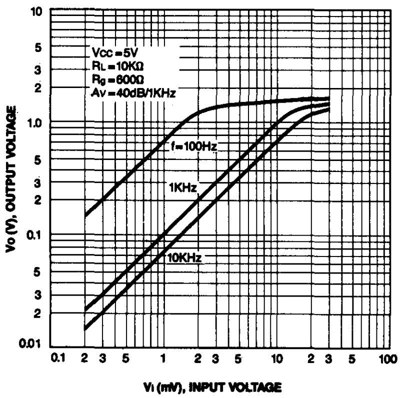


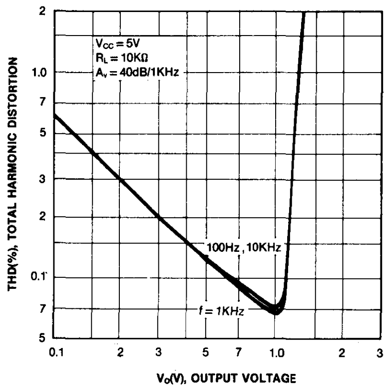
Fig. 6

If the closed loop gain of the amplifier is designed lower than 40dB, the circuit should be compensated by connecting 10pF between Pin 3 and Pin 2, and 0.033μF (mylar) + 10Ω to the load end.

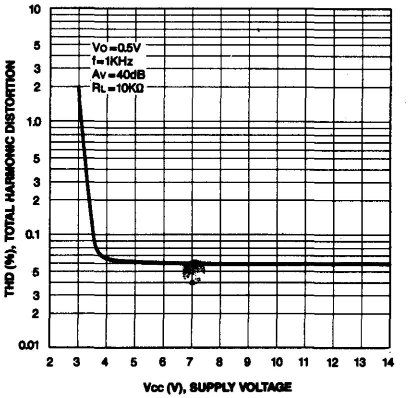
OUTPUT VOLTAGE-INPUT VOLTAGE



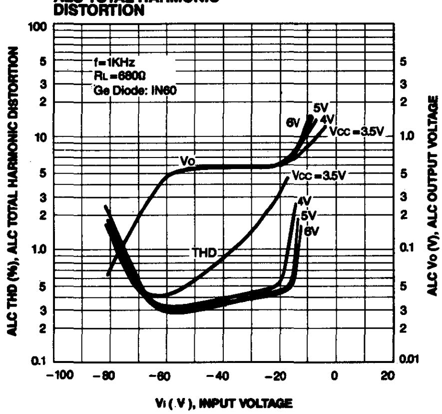
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



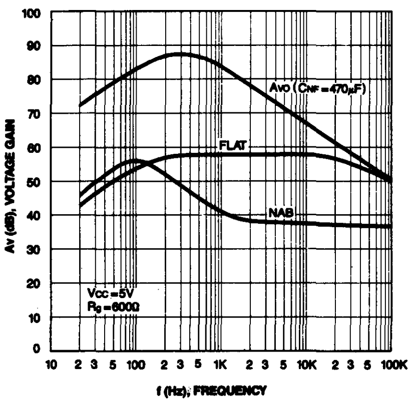
TOTAL HARMONIC DISTORTION-SUPPLY VOLTAGE



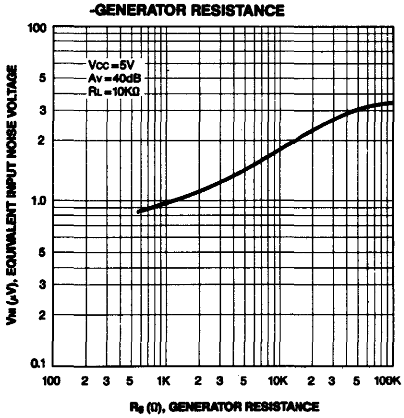
ALC OUTPUT VOLTAGE / ALC TOTAL HARMONIC DISTORTION — INPUT VOLTAGE



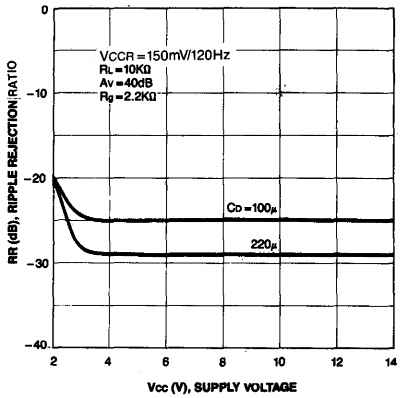
VOLTAGE GAIN-FREQUENCY



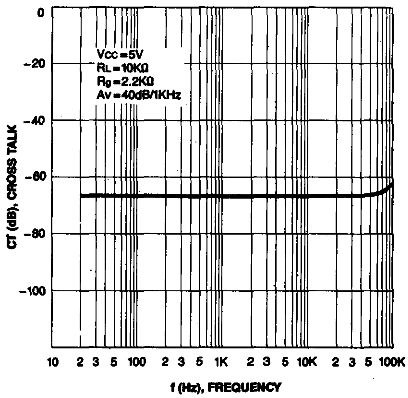
EQUIVALENT INPUT NOISE VOLTAGE -GENERATOR RESISTANCE



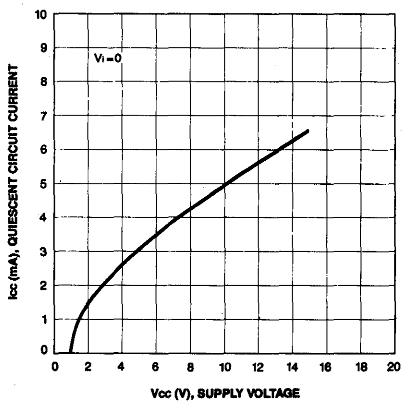
RIPPLE REJECTION RATIO-SUPPLY VOLTAGE



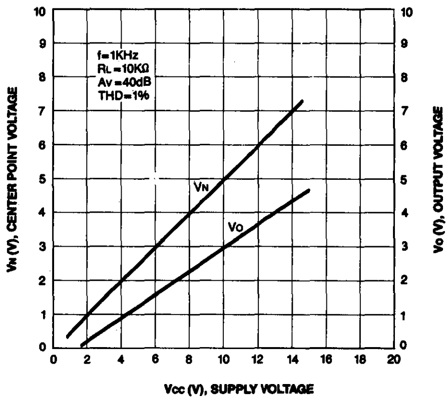
CROSS TALK-FREQUENCY



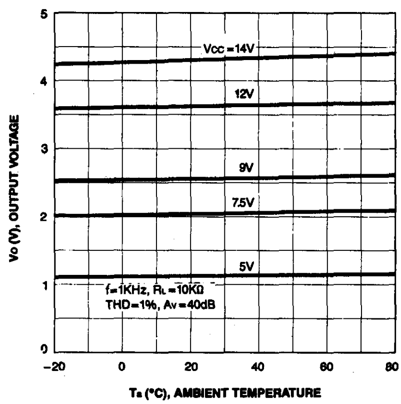
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



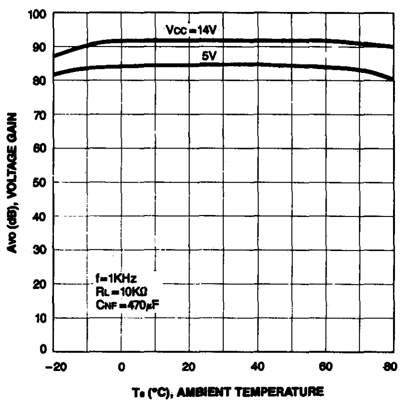
CENTER POINT VOLTAGE, OUTPUT VOLTAGE -SUPPLY VOLTAGE



OUTPUT VOLTAGE-AMBIENT TEMPERATURE



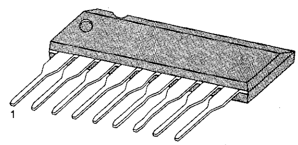
VOLTAGE GAIN-AMBIENT TEMPERATURE



DUAL EQUALIZER AMPLIFIER WITH ALC

The KA2224 is a monolithic integrated circuit consisting of a dual equalizer amplifier with ALC, and it is suitable for stereo radio cassette tape recorders.

9 SIP



FEATURES

- **Dual equalizer amplifier with built-in ALC circuit**
- **Low noise; $V_{NI} = 1.0\mu V$ (Typ)**
- **High open loop voltage gain; 80 dB (Typ)**
- **Wide operating supply voltage range; $V_{CC} = 4.5V \sim 14V$**
- **Good ALC response balance between channels**
- **Not necessary the input coupling capacitor**
- **Not necessary diode or transistor for ALC**
- **Built in power supply muting circuit**
- **Minimum number of external parts required**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22241	9 SIP	− 20 ~ + 75°C

BLOCK DIAGRAM

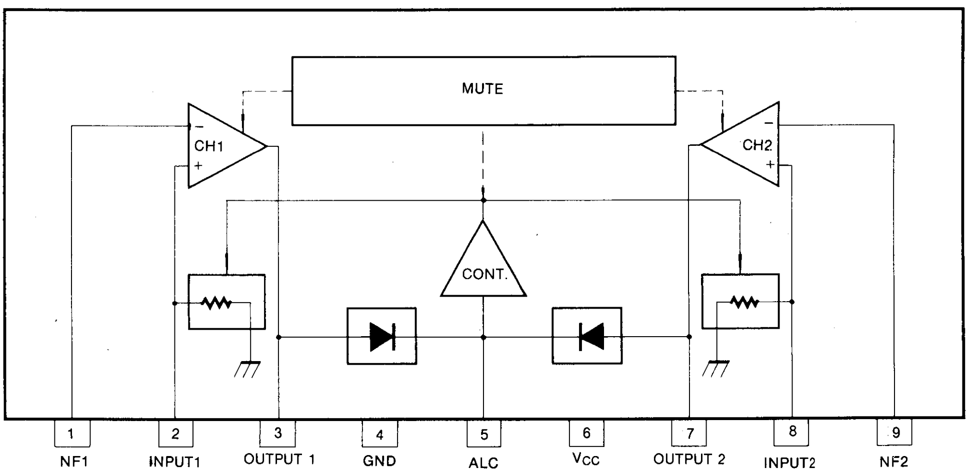


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_d	*550	mW
Operating Temperature	T_{opr}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

* : Derated avobe Ta = 25°C in the propotion of 5.5mW/°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 7V, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	$V_i = 0$	1.5	3.5	4.5	mA
Open Loop Voltage Gain	A_{VO}	$V_o = 0.3V$	70	80		dB
Closed Loop Voltage Gain	A_V	$V_o = 0.3V$	45	48	50	dB
Output Voltage	V_o	THD = 1%	0.6	1.2		V
Total Harmonic Distortion	THD	$V_o = 0.3V$		0.1	0.3	%
Equivalent Input Noise Voltage	V_{NI}	$R_g = 2.2K\Omega$, BW(−3dB) = 20Hz ~ 20KHz		1.0	2.0	μV
Input Resistance	R_i		15	25	45	KΩ
ALC Range	ALC(R)	$R_g = 3.9K$, THD = 10%	40	45		dB
ALC Balance	ALC(B)	$V_i = 1mV$		0	2.5	dB

TEST CIRCUIT

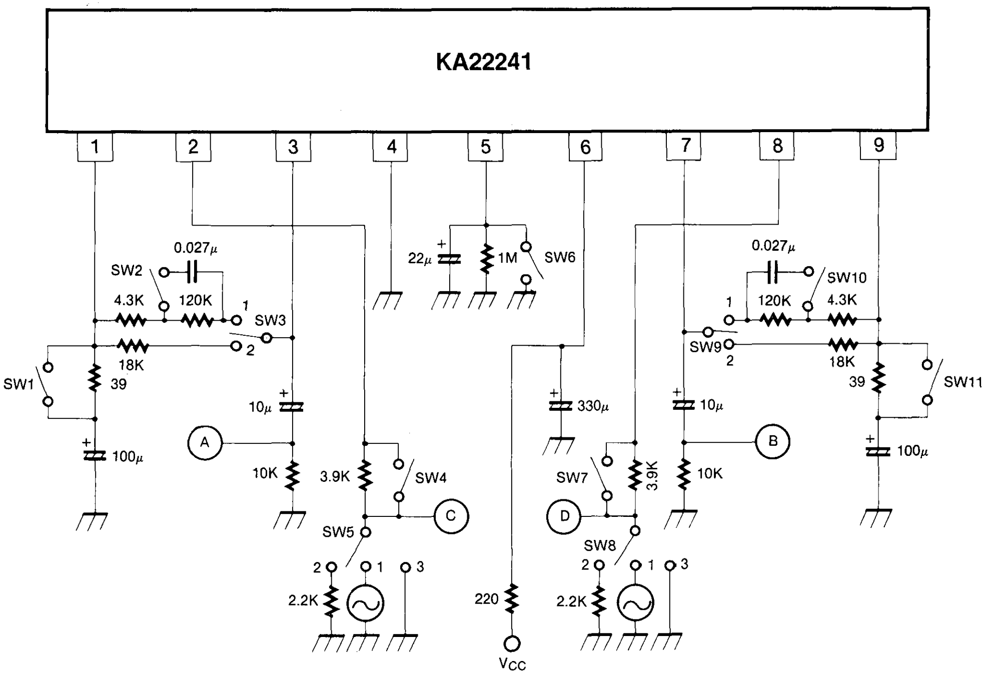


Fig. 2

TEST METHOD

Symbol		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11
I_{CC}		ON	OFF	1	ON	3	ON	ON	3	1	OFF	ON
A_{vo}		ON	OFF	1	ON	1	ON	ON	3	1	OFF	ON
A_v	CH-1	OFF	ON	1	ON	1	ON	ON	3	1	OFF	ON
THD	CH-1	OFF	ON	1	ON	1	ON	ON	3	1	OFF	ON
V_o	CH-1	OFF	ON	1	ON	1	ON	ON	3	1	OFF	ON
V_{NI}	CH-1	OFF	ON	1	ON	2	ON	ON	3	1	OFF	ON
	CH-2	ON	OFF	1	ON	3	ON	ON	2	1	ON	OFF
ALC(R)	CH-1	OFF	OFF	2	OFF	1	OFF	ON	3	1	OFF	ON
ALC(B)		OFF	OFF	2	OFF	1	OFF	OFF	1	2	OFF	OFF

APPLICATION CIRCUIT 1

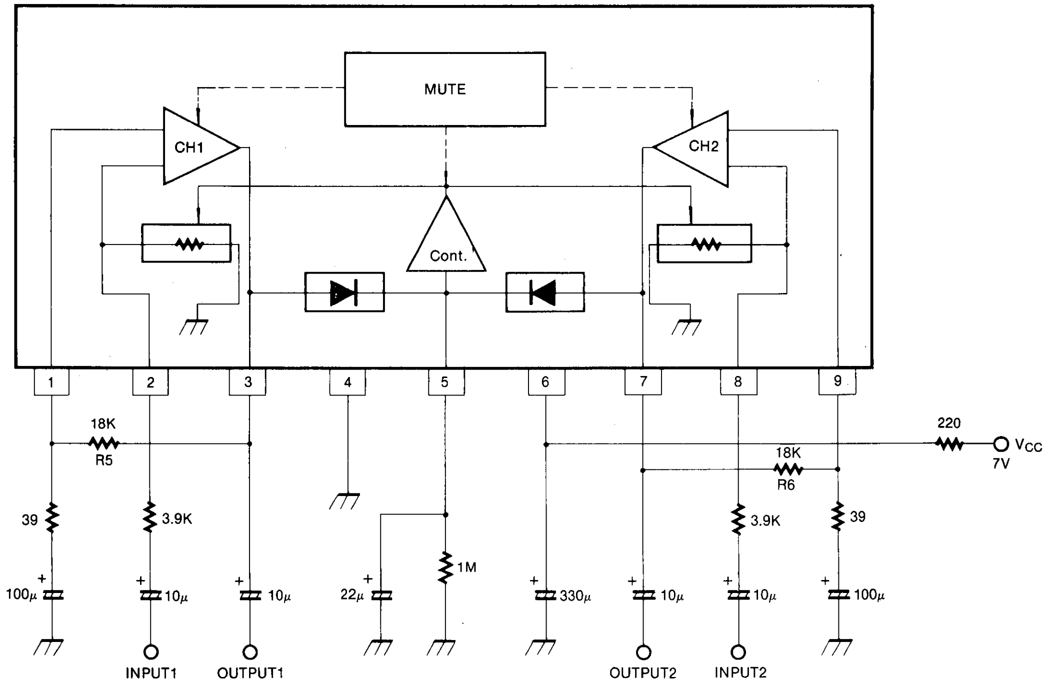
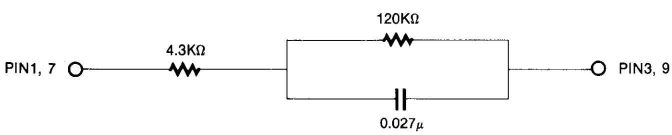


Fig. 3

NOTE

ON recording, connect the time constant circuit as shown below, instead of R5, R6 of Pins 1-3, 7-9, which are used in the NAB.



APPLICATION CIRCUIT 2

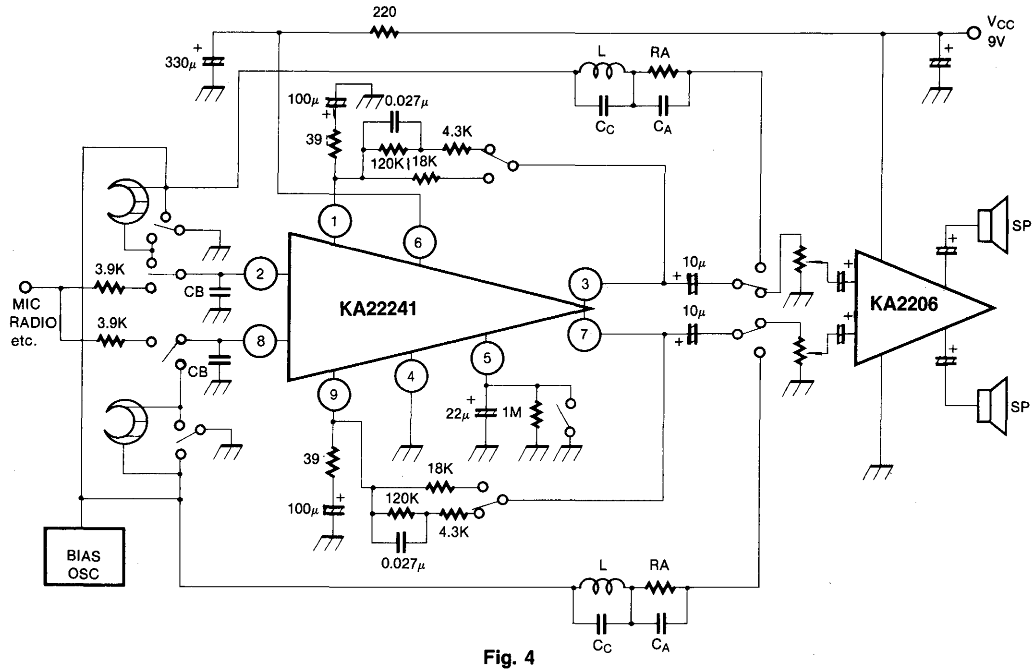
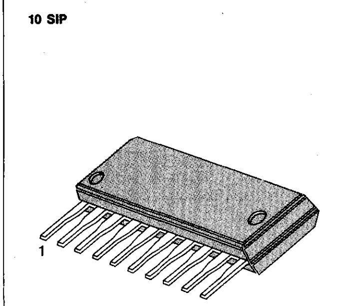


Fig. 4

DUAL EQUALIZER PRE-AMPLIFIER WITH ALC

The KA22242 is a monolithic integrated circuit consisting of a dual equalizer amplifier with ALC and Mute function, and it is suitable for stereo radio cassette tape recorders.



FEATURES

- **Dual equalizer amplifier with ALC circuit**
- **Direct coupling system of input circuit**
- **High open loop voltage gain ($A_{VO}=85dB$ at $f=1KHz$)**
- **Wide operating supply voltage range ($V_{CC}=4 \sim 12V$)**
- **Low noise ($V_{NI}=1.0\mu V$ at $R_g=2.2K\Omega$)**
- **Ripple rejection filter**
- **High input impedance ($R_i=62K\Omega$)**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22242	10 SIP	−20 ~ +75°C

BLOCK DIAGRAM

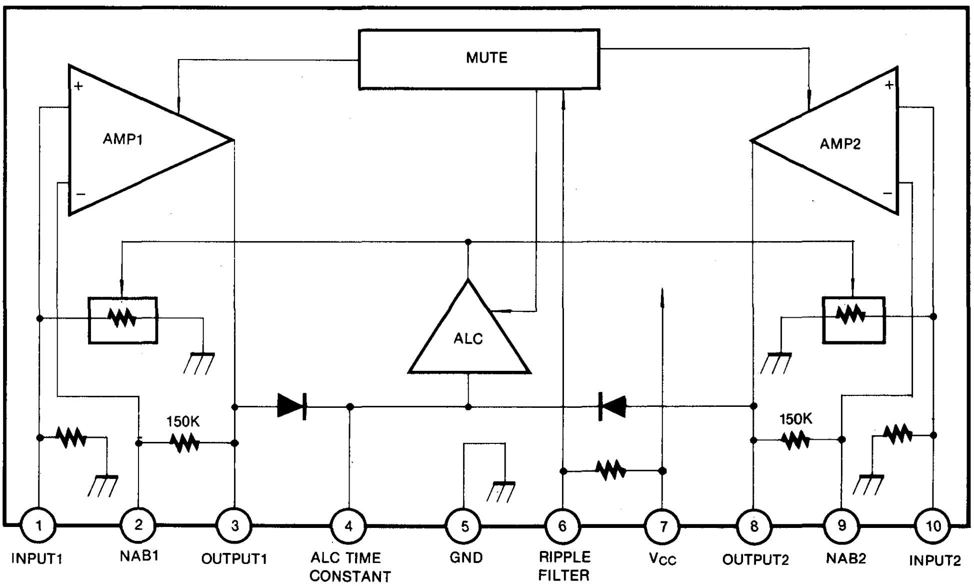


Fig. 1

3

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	14	V
Power Dissipation	P_d	550	mW
Operating Temperature	T_{opr}	− 20 ~ + 75	°C
Storage Temperature	T_{stg}	− 55 ~ + 125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 8V, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}		2.5	3.3	4.0	mA
Open-loop Voltage Gain	A_{VO}	V_O = 1V	75	85		dB
Total Harmonic Distortion	THD	V_O = 0.3V		0.5	1.0	%
Max Output Voltage	V_{OM}	THD = 1%	1.9	2.2		V
Equivalent Input Noise Voltage	V_{NI}	R_g = 2.2KΩ		1.0	2.5	μV
Input Resistance	R_i			62		KΩ
Channel Cross Talk	CT	R_g = 2.2KΩ, V_O = 1V	45	55		dB
ALC Range	ALC(R)	V_i = − 52dBm, 3dB up	40	45		dB
ALC Balance	ALC(B)	V_i = − 45dB		0	2.0	dB
ALC Distortion	THD(ALC)	V_i = − 45dB		0.2	0.6	%
ALC Output Voltage	V_O(ALC)	V_i = − 45dB	0.6	0.7	0.85	V

TEST CIRCUIT

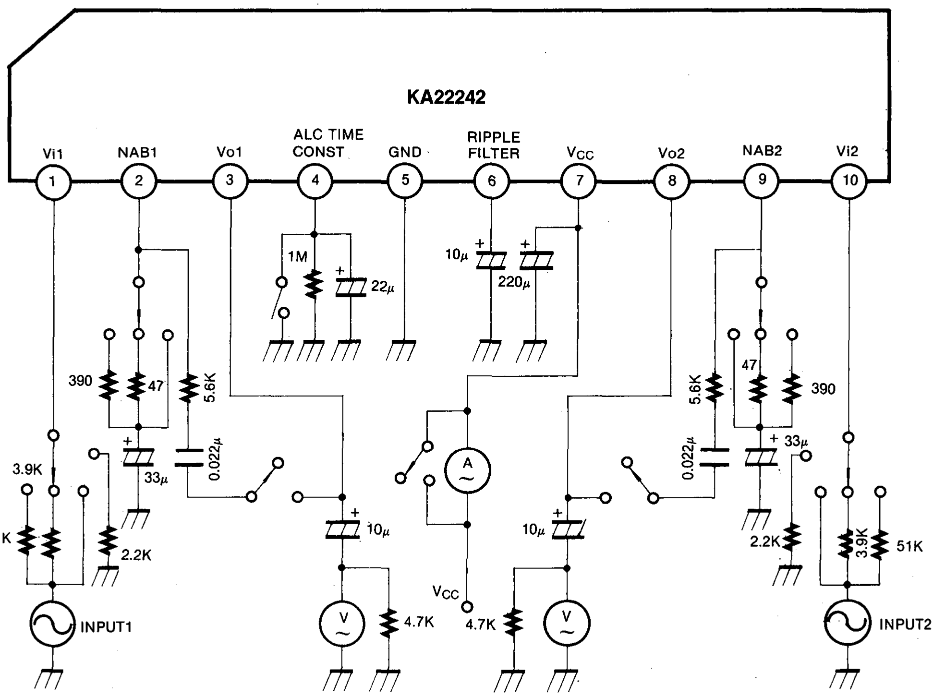


Fig. 2

APPLICATION CIRCUIT

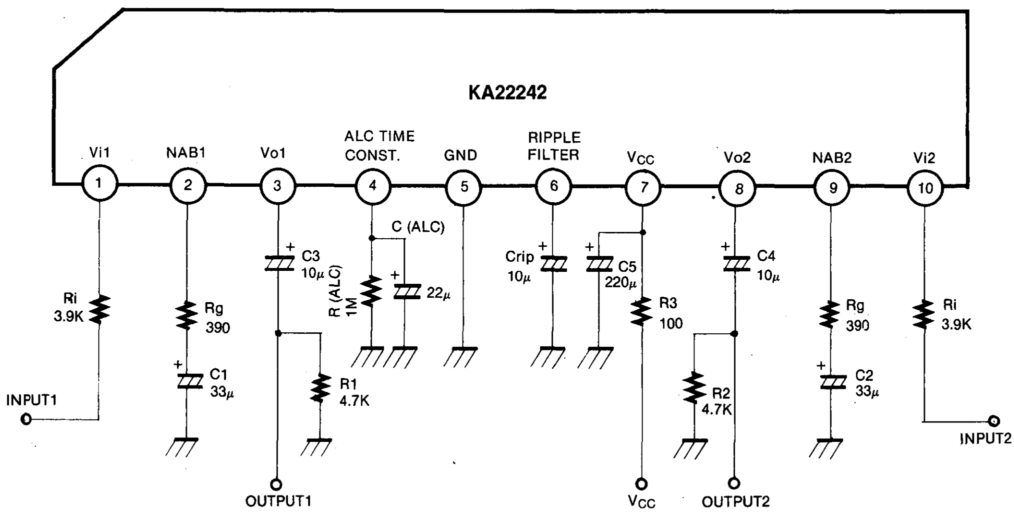


Fig. 3

DESCRIPTION OF KA22242

The KA22242 has a simple package, 10-pin and built-in ALC detector, mute circuit and ripple rejection filter developed for cassette tape recorders. To provide a stereo function, it has been developed into a 2-channel pre-amplifier for recording and playback. Also to provide high speed dubbing and recording gain, its gain is high (f = 1KHz, A_{VO} = 85dB) and the total harmonic distortion is low (f = 1KHz, THD = 0.5%). An input circuit is used as a direct coupling system to eliminate the input coupling capacitor and prevent tape head magnetization and pop noise. A built-in ripple circuit (ripple rejection transistor) improves the ripple rejection ratio. And the ALC circuit can achieve a wide dynamic range by simply attaching a time-constant circuit.

3

APPLICATION DESCRIPTION

1. Playback Amplifier

To use the playback mode, the KA22242 can be applied for an NAB equalizer amplifier. The NAB characteristic is obtained by installing a NAB circuit in the Negative Feedback section (between Pins 2 and 3). In this case, Pin 4 is connected with the GND to eliminate the ALC effect.

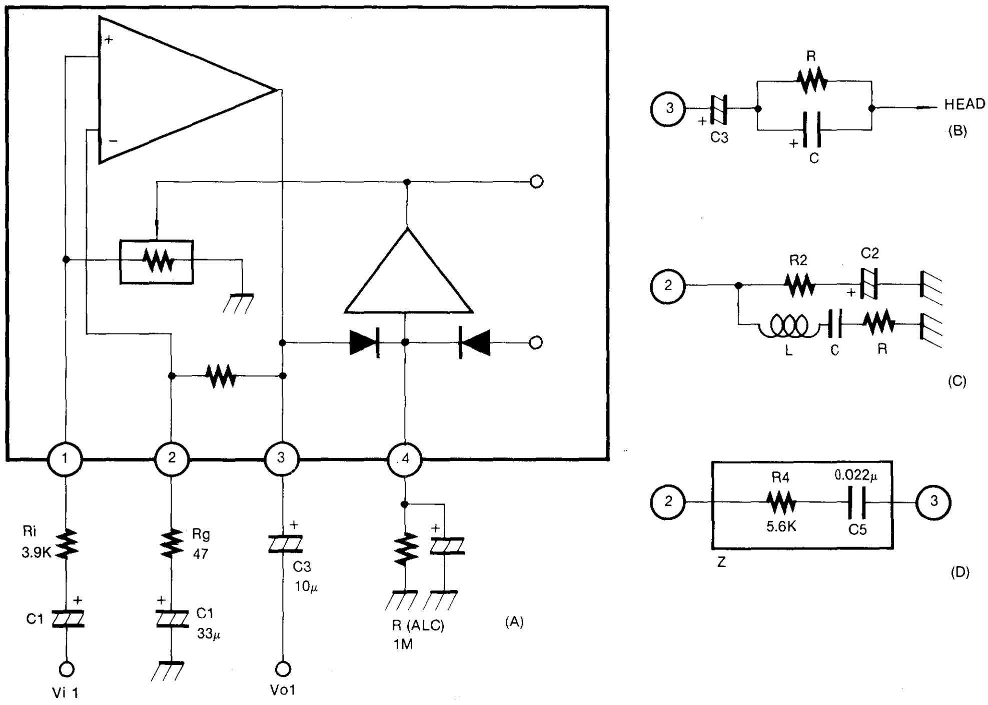


Fig. 4

2. Recording Amplifier (Figure 1 (A))

The recording amplifier's voltage gain is determined by the ratio of the internal 150KΩ to R2

$G_V = 150K\Omega/R2$

The recording amplifier requires a compensation circuit to correct loss at high frequencies. The compensation circuit may be either CR or LC resonance. The frequency response of the resonance circuit is fixed at 1 ~ 4KHz. An example using a CR is shown in Figure 1(B), and one using LC resonance is shown in Figure 1(C).

2. ALC Circuit

For the dynamic range, the ALC circuit uses the simple time-constant circuit. ALC operation of the KA22242 is accomplished with a signal rectifier and electronic volume control. The signal rectifier uses the comparator circuit and the comparator circuit compares the DC voltage of the output signal with the reference voltage. If the output voltage is higher than the reference voltage, the comparator turns on to charge smoothing capacitor C4.
For the dynamic range, a turn-off level $(0.7V_{rms}) + 6dB$ is ensured at $V_{CC} = 6V$. When the peak voltage of the output signal is $0.7V_{rms}$, the comparator comes on and the electronic volume control is connected between the input line and GND. The input signal is attenuated by the ratio of the external resistance R1 to the electronic volume control resistance and ALC circuit is operated. The ALC range can be varied by changing R1. If R1 is too large, the S/N ratio may degrade, so several Kohm is proper. The ALC attack time and recovery time are set at Pin 4 by C4 and R3. Note that the greater the time constant (C4, R3), the longer the recovery time, and the greater C4, the shorter the attack time.

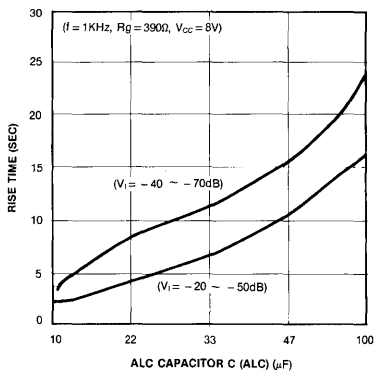
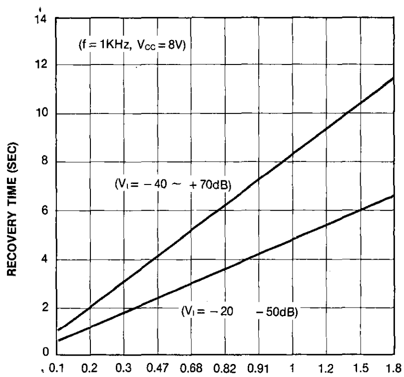


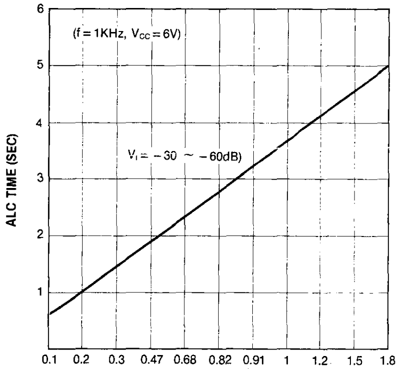
Fig. 5

Figure 2 is a ALC Time graph of the KA22242 at R2 = 390ohm.
At R2 = 390ohm, Vi = −40dB,
ALC recovery time is about 8 seconds and when the ALC capacitor is increased, it is increased also. And it is can be adjusted to fix the design point. But as the recovery time varies by the input level, the value of this capacitor must be considered when the set is designed.



R (ALC) (MΩ)
(A) Rg = 390Ω

Fig. 6



R (ALC) (MΩ)
(B) Rg = 47Ω

Fig. 7

As the Figure 3, because the Rg range is 47 ~ 100 ohm normally at the set application, the matching between R3 and C4 occurs.

4. Mute Function

The KA22242 has a mute function to mute at the power switch on/off. To prevent a malfunction of the ALC circuit, the KA22242 is muted at this time. If the ALC is not muted, the supply voltage charges the ALC capacitor and generates error-operations. The muting time is varied by the time-constant of the ripple filter.
C3*R internal (15K)
If C3 is too large, the rise time gets too slow and pop noises occur when other IC begins to operate faster than the KA22242 in some application circuit. In this case, if the combination with resistance is about 1Kohm, the DC voltage (V_{ODC}) at the output terminal is nearly constant.

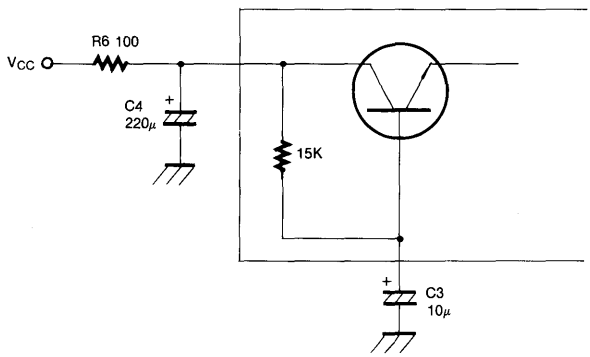
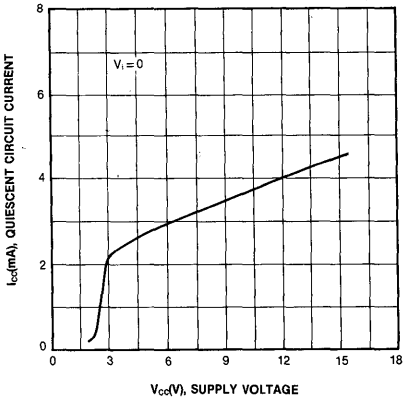
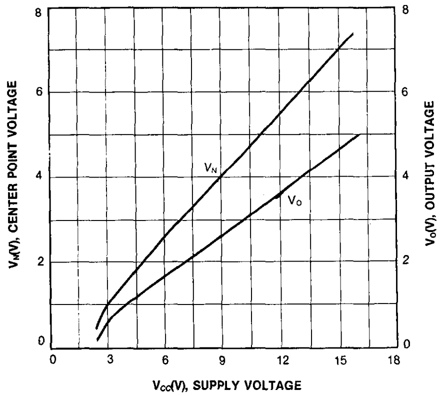


Fig. 8

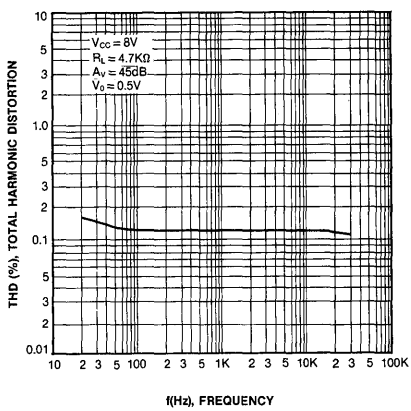
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



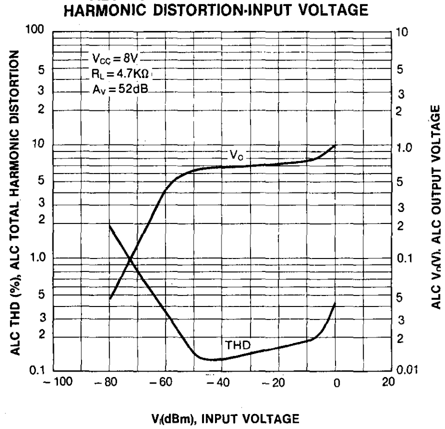
CENTER POINT VOLTAGE
OUTPUT VOLTAGE-SUPPLY VOLTAGE



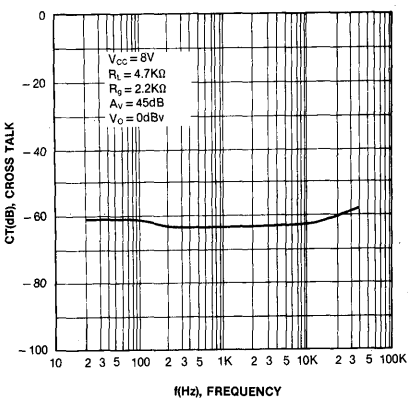
TOTAL HARMONIC DISTORTION-FREQUENCY



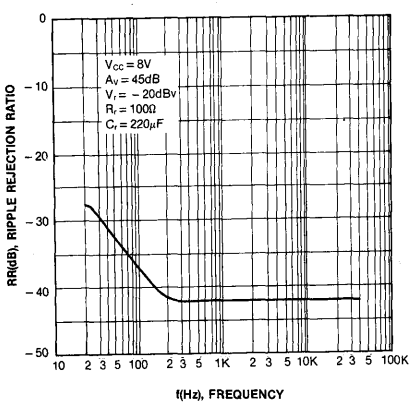
ALC OUTPUT VOLTAGE ALC TOTAL
HARMONIC DISTORTION-INPUT VOLTAGE



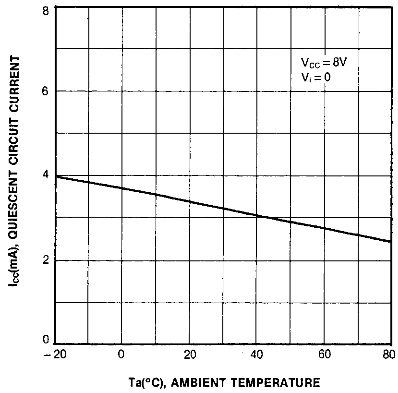
CROSS TALK-FREQUENCY



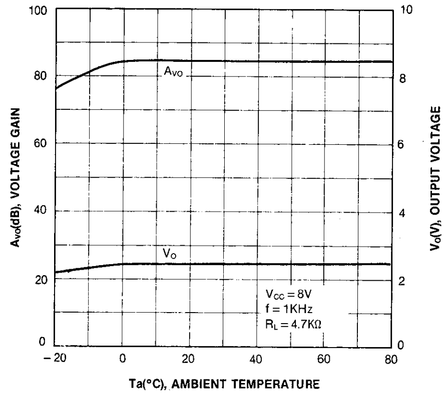
RIPPLE REJECTION RATIO-FREQUENCY



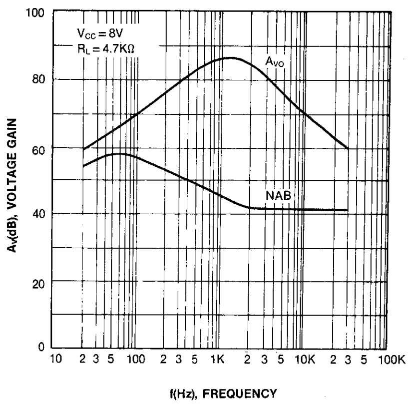
QUIESCENT CIRCUIT CURRENT-AMBIENT TEMPERATURE



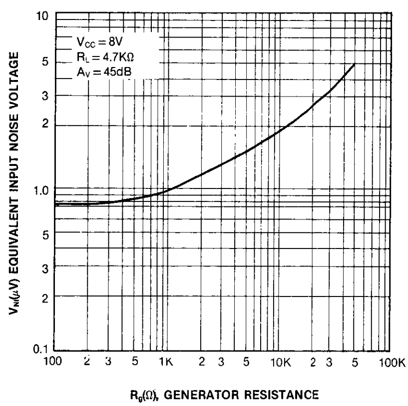
VOLTAGE GAIN OUTPUT VOLTAGE-AMBIENT TEMPERATURE



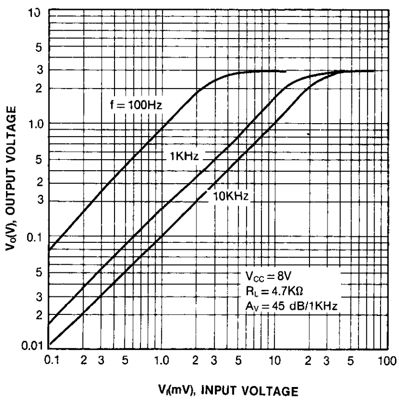
VOLTAGE GAIN-FREQUENCY



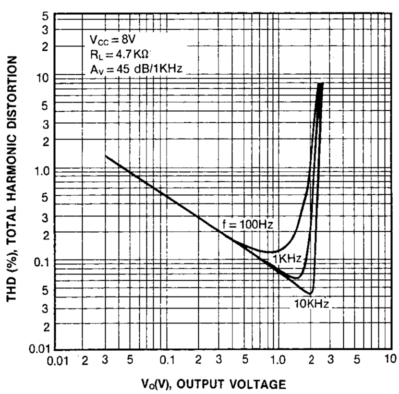
EQUIVALENT INPUT NOISE VOLTAGE-GENERATOR RESISTANCE



OUTPUT VOLTAGE-INPUT VOLTAGE

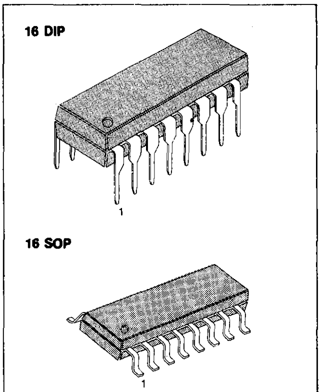


TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



DUAL PREAMPLIFIER FOR 3V USING

The KA2225 is a monolithic integrated circuit consisting of a dual equalizer amplifier, and it is suitable for 3V stereo radio cassettes.



FEATURES

- **High open loop gain: 85dB (Typ) (V_{CC}=3V, f=1kHz).**
- **Not necessary the input coupling capacitors.**
- **Operating supply voltage range: V_{CC}=1.6V ~ 5V.**
- **Good channel separation: 60dB (Typ).**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2225	16 DIP	−20 ~ +70°C
KA2225D	16 SOP	

BLOCK DIAGRAM

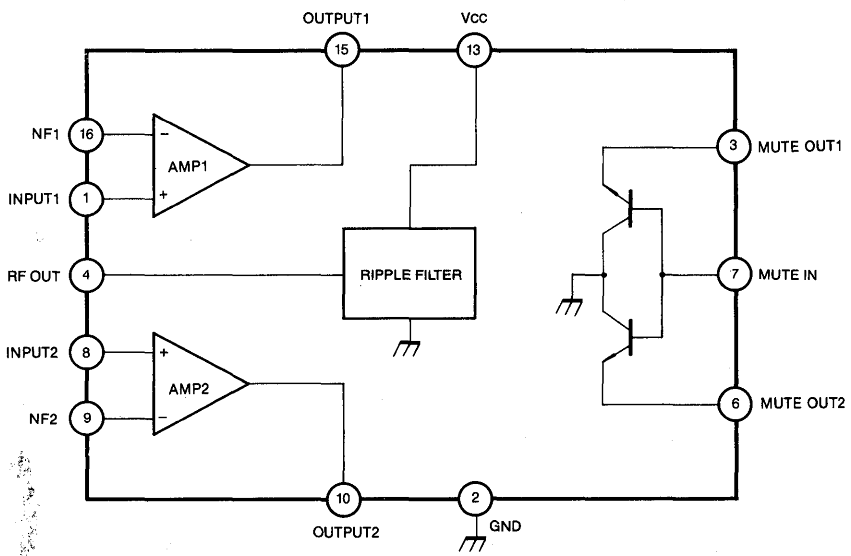


Fig. 1

ABSOLUTE MAXIMUM RATINGS ($T_a = 25°C$)

Characteristic		Symbol	Value	Unit
Supply Voltage		V_{CC}	7	V
Power Dissipation	KA2225	P_d	750	mW
	KA2225D		350	
Operating Temperature		T_{opr}	−20 ~ +70	°C
Storage Temperature		T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=3V, f = 1KHz, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Circuit Current		I_{CC}	V_i=0		2	3.4	mA
Voltage Gain	Open Loop	A_{VO}		70	85		dB
	Closed Loop	A_V			40		dB
Output Voltage		V_O	THD=1%	0.5	0.8		V
Total Harmonic Distortion		THD	V_O=0.1V,		0.07	0.5	%
Output Noise Voltage		V_{NO}	R_g=2.2KΩ, A_V=40dB BW(−3dB)=50Hz~20KHz		0.14	0.22	mV
Cross Talk		CT	R_g=600Ω, V_O=−10dBv		60		dB
Muting Attenuation		M (att)	V_{MUTE}=1V		43		dB
Input Resistance		R_i		20	30		KΩ

TEST CIRCUIT

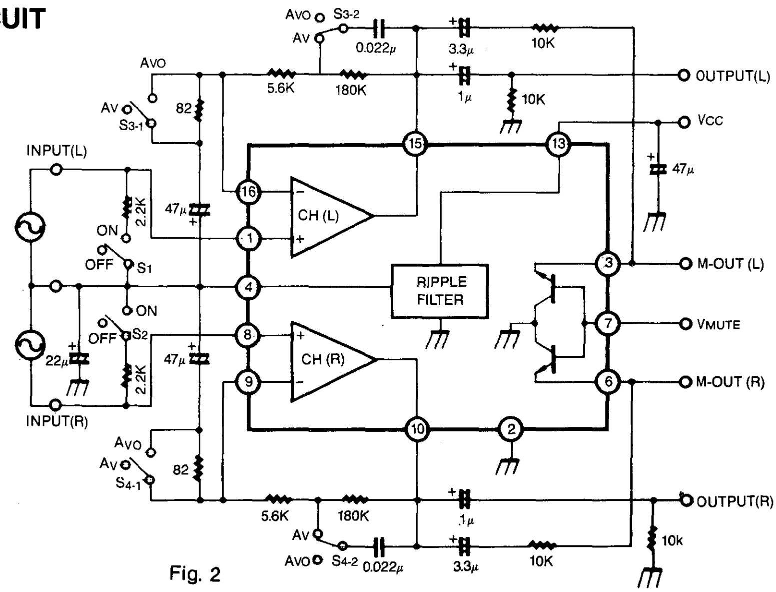
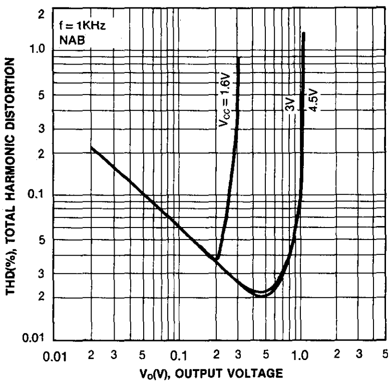
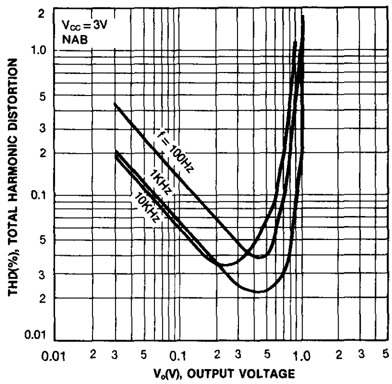


Fig. 2

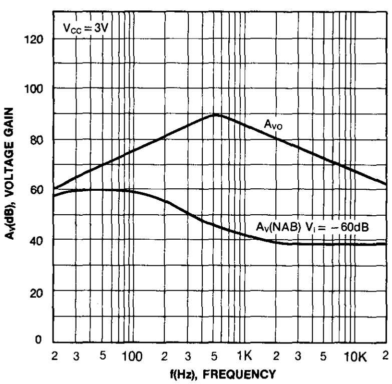
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



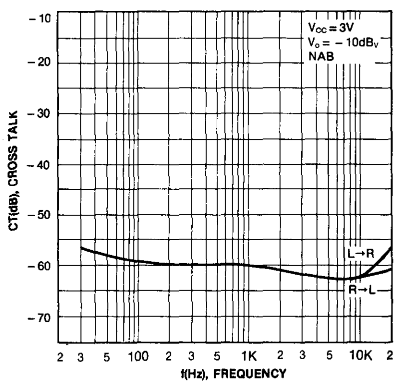
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



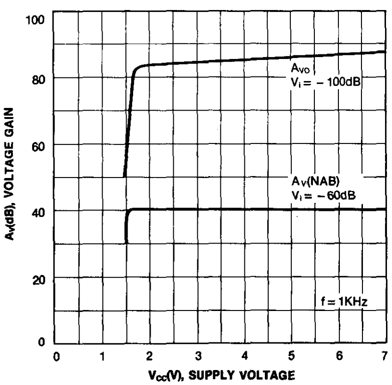
VOLTAGE GAIN-FREQUENCY



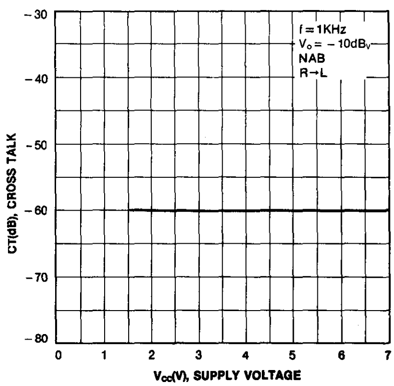
CROSS TALK-FREQUENCY



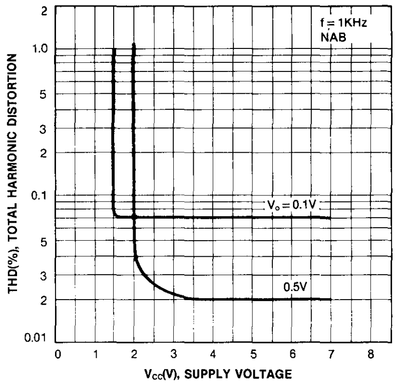
VOLTAGE GAIN-SUPPLY VOLTAGE



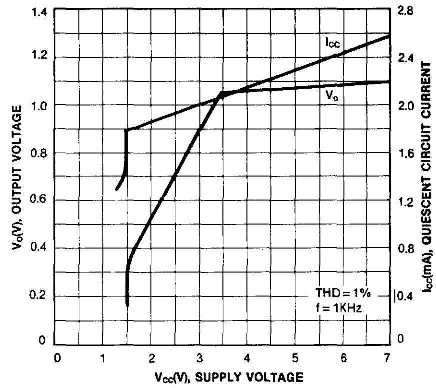
CROSS TALK-SUPPLY VOLTAGE



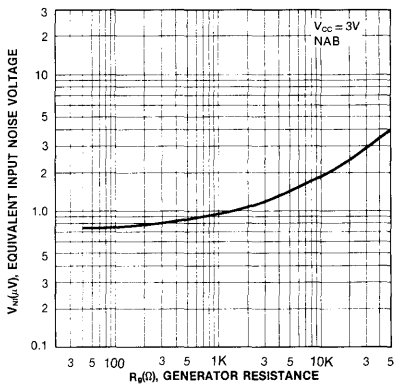
TOTAL HARMONIC DISTORTION-SUPPLY VOLTAGE



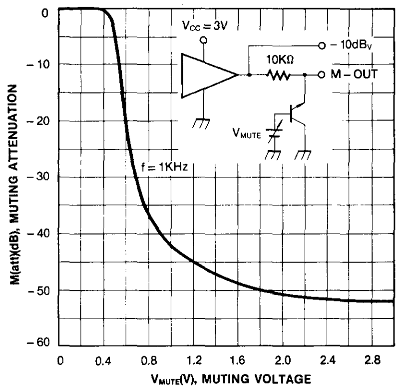
OUTPUT VOLTAGE
QUIESCENT CIRCUIT CURRENT -SUPPLY VOLTAGE



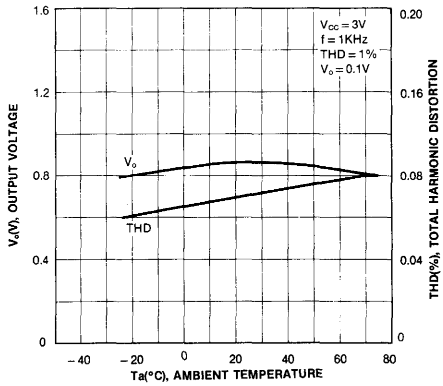
EQUIVALENT INPUT
NOISE VOLTAGE -GENERATOR RESISTANCE



MUTING ATTENUATION-MUTING VOLTAGE



OUTPUT VOLTAGE
TOTAL HARMONIC DISTORTION -AMBIENT TEMPERATURE



APPLICATION CIRCUIT

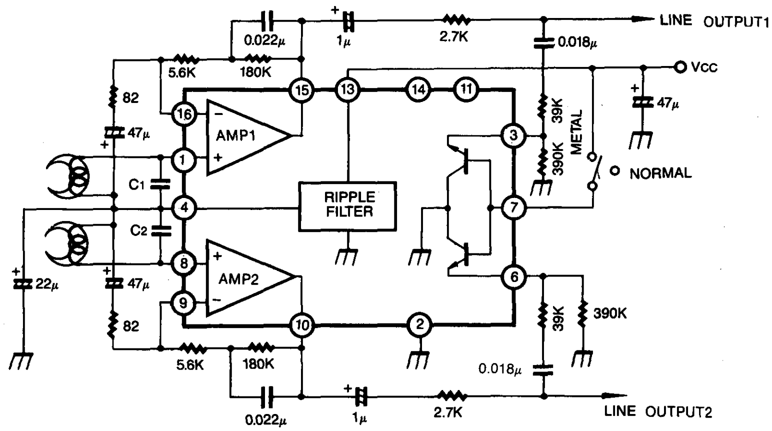


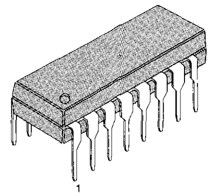
Fig. 3

- Capacitor C_1 and C_2 may be required to prevent instability caused by the pattern layout or interference of external high frequency signals.

DUAL EQUALIZER AMPLIFIER WITH REC AMP

The KA22261 is a monolithic integrated circuit consisting of a dual equalizer amplifier with REC AMP, and it is suitable for stereo radio cassettes.

16 DIP



FEATURES

- **Dual equalizer amplifier with ALC circuit.**
- **High open loop voltage gain: 78dB (Typ).**
- **Recording amplifier available because of high open loop voltage gain.**
- **Not necessary diode or transistor for ALC.**
- **Good channel separation: 60dB (Typ).**
- **Good ALC response balance between channels.**
- **Wide operating supply voltage range: V_{CC} = 6V ~ 15V.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22261	16 DIP	−20 ~ +70°C

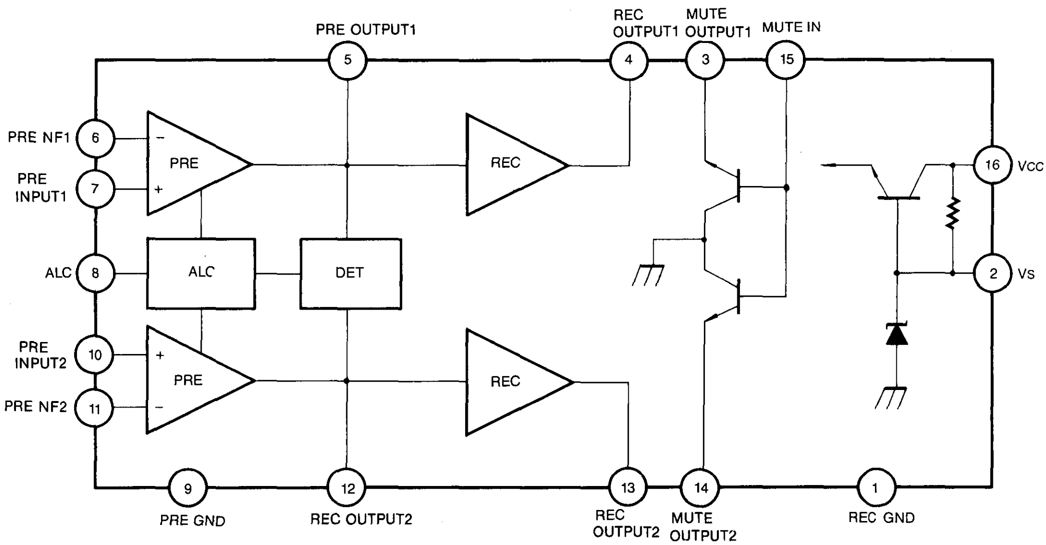


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_d	750	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=9V, f=1KHz, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Circuit Current		I_{CC}	V_i=0		8.5	10.5	mA
PRE AMP	Open Loop Gain	A_{VO}	V_i=−80dBm	65	78		dB
	Output Voltage	Vo_1	THD=1%	0.5	0.8		V
	Total Harmonic Distortion	THD (1)	V_O=0.2V		0.15	0.5	%
	Output Noise Voltage	V_{NO}	Rg=2.2KΩ. NAB BW(−3dB)=30Hz ~20KHz		0.26	0.6	mV
	Cross Talk	CT	Rg=2.2KΩ	47	60		dB
REC AMP	Closed Loop Gain	A_V	R_L=10KΩ	12.7	14.7	16.7	dB
	Output Voltage	Vo_2	THD=1%	2.0	2.5		V
	Total Harmonic Distortion	THD (2)	V_O=1.5V		0.3	1.0	%
	ALC Range (Note 1)	ALC (R)	V_i=−60dB, Rg=2.2KΩ		45		dB
	ALC Distortion	ALC THD	V_i=−20dBm, Rg=2.2KΩ		0.3	1.0	%
	ALC Voltage	ALC V_O	V_i=−20dBm, Rg=2.2KΩ	0.9	1.1	1.42	V
Muting Attenuation		M(att)		45	55		dB
ALC Balance		ALC (B)	V_i=−20dBm		0	2	dB

Note 1: Input voltage range from V_i=−60dB to output voltage V_O=3dB up.

TEST CIRCUIT

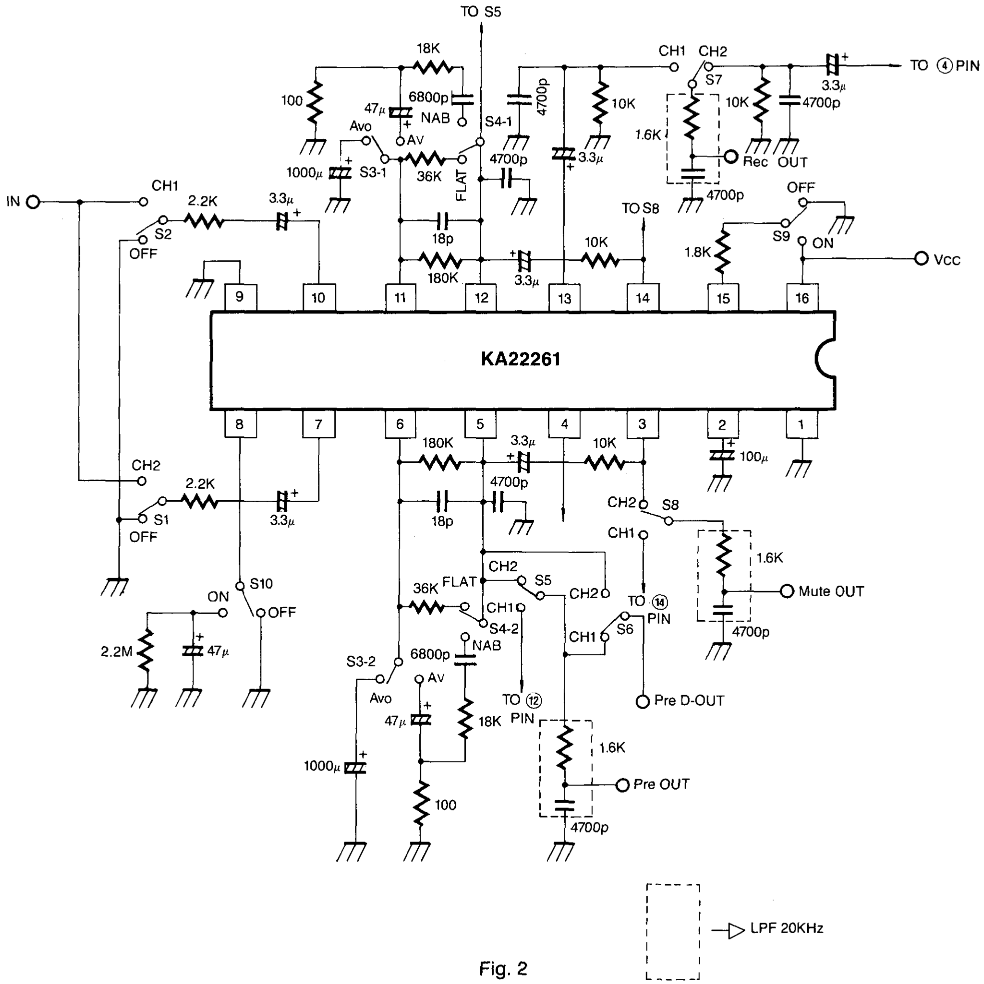


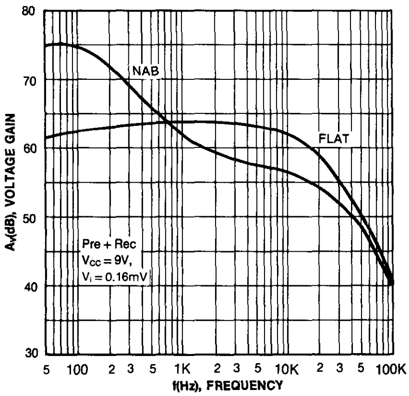
Fig. 2

TEST METHOD

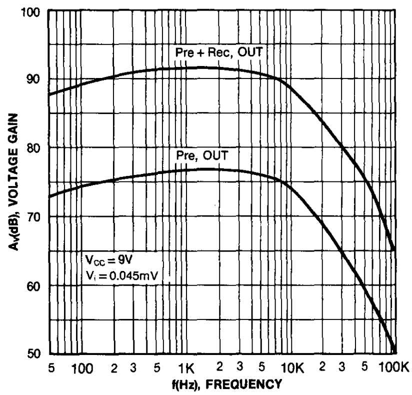
*: NO specified.

SW / Symbol	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	Measure Terminal
I_{CC}	*	*	*	*	*	*	*	*	OFF	*	V_{CC}
A_{VO}	OFF	CH1	A_{VO}	FLAT	CH1	*	*	*	OFF	OFF	Pre OUT
V_O (1)	OFF	CH1	A_V	NAB	CH1	*	*	*	OFF	OFF	Pre OUT
THD (1)	OFF	CH1	A_V	NAB	CH1	*	*	*	OFF	OFF	Pre OUT
V_{NO}	OFF	OFF	A_V	NAB	CH2	CH1	*	*	OFF	OFF	Pre D-OUT
C.T.	OFF	CH1	A_V	FLAT	CH1→CH2	*	*	*	OFF	OFF	Pre OUT
A_V	OFF	CH1	A_V	FLAT	CH1	*	CH1	CH2	OFF	OFF	Pre OUT→Rec OUT
V_O (2)	OFF	CH1	A_V	FLAT	CH2	*	CH1	CH2	OFF	OFF	Rec OUT
THD (2)	OFF	CH1	A_V	FLAT	CH2	*	CH1	CH2	OFF	OFF	Rec OUT
ALC (R)	OFF	CH1	A_V	FLAT	CH2	*	CH1	CH2	OFF	ON	Rec OUT
ALC (THD)	OFF	CH1	A_V	FLAT	CH2	*	CH1	CH2	OFF	ON	Rec OUT
ALC (V_O)	OFF	CH1	A_V	FLAT	CH2	*	CH1	CH2	OFF	ON	Rec OUT
ATT	OFF	CH1	A_V	FLAT	CH1	*	*	CH1	OFF→ON	OFF	Mute OUT
ALC (B)	CH2	CH1→CH2	A_V	FLAT	*	*	CH1→CH2	*	OFF	ON	Rec OUT

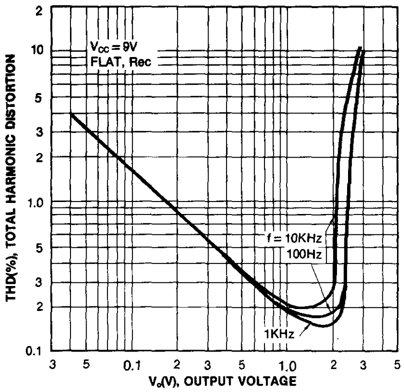
VOLTAGE GAIN-FREQUENCY



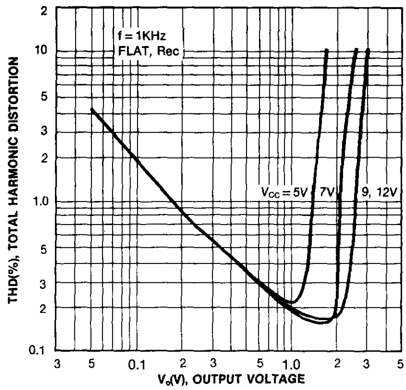
VOLTAGE GAIN-FREQUENCY



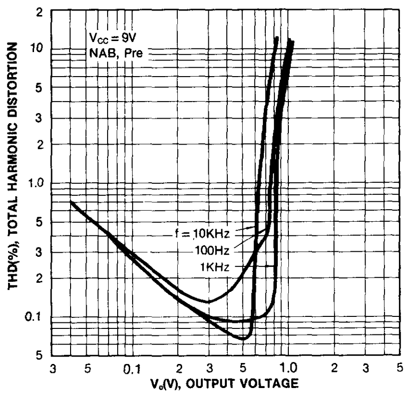
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



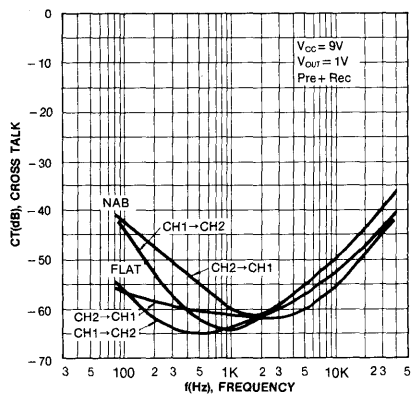
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



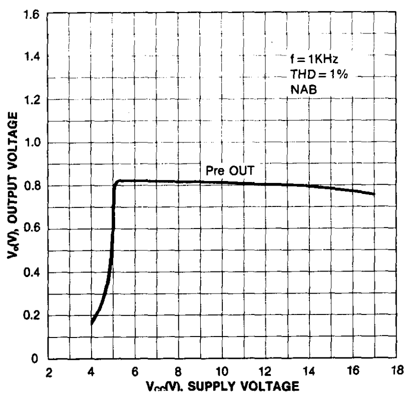
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



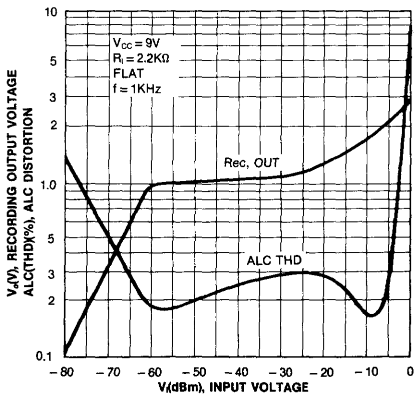
CROSS TALK-FREQUENCY



OUTPUT VOLTAGE-SUPPLY VOLTAGE



RECORDING OUTPUT VOLTAGE
ALC DISTORTION -INPUT VOLTAGE



APPLICATION CIRCUIT

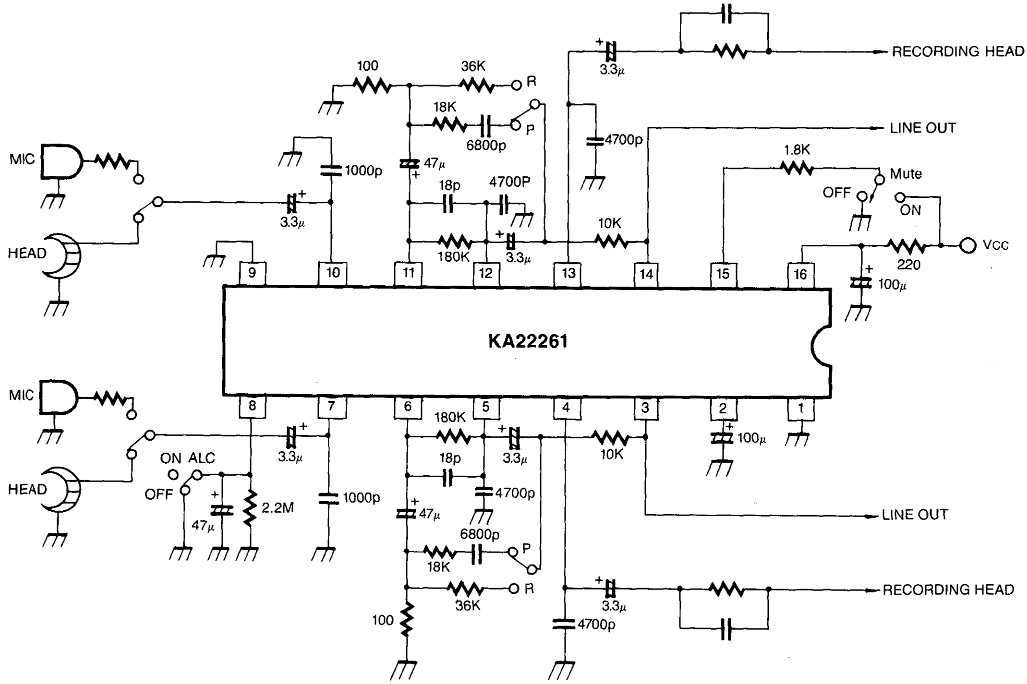
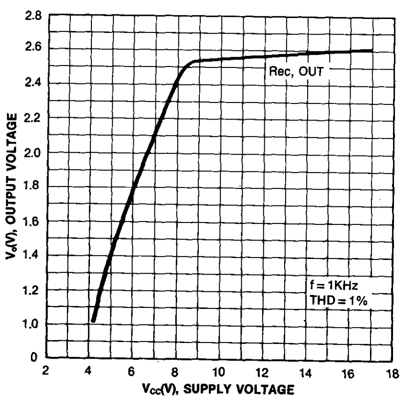
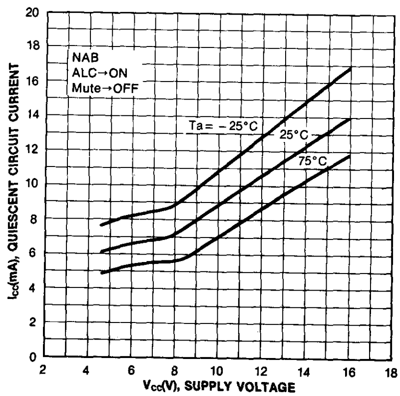


Fig. 3

OUTPUT VOLTAGE-SUPPLY VOLTAGE



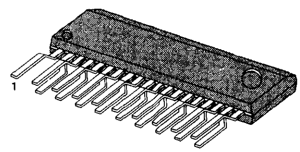
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



DUAL EQUALIZER AMPLIFIER SYSTEM

The KA2228 is a monolithic integrated circuit consisting of play back AMP, REC AMP with ALC, mic AMP with ALC and monitor AMP. It is dual EQ AMP system built-in switch for selecting REC/PLAY mode, tape or radio (Aux) modes. It is used for radio cassette players and can be applicated easily by getting rid of the conventional mechanism REC/PLAY switch.

21 ZSIP



FEATURES

- **Following 4 modes can be operated by a combination of external switches: radio (Aux), radio (Aux) recording, mic recording and tape play back**
- **Built-in switch for selecting REC/PLAY mode.**
- **Built-in switch for selecting radio (Aux) or tape input.**
- **Few external parts.**
- **Small package: 21 shrink ZSIP type.**
- **Operating supply voltage range: 3.5 ~ 7.0V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2228	21 ZSIP	−25 ~ +75°C

BLOCK DIAGRAM

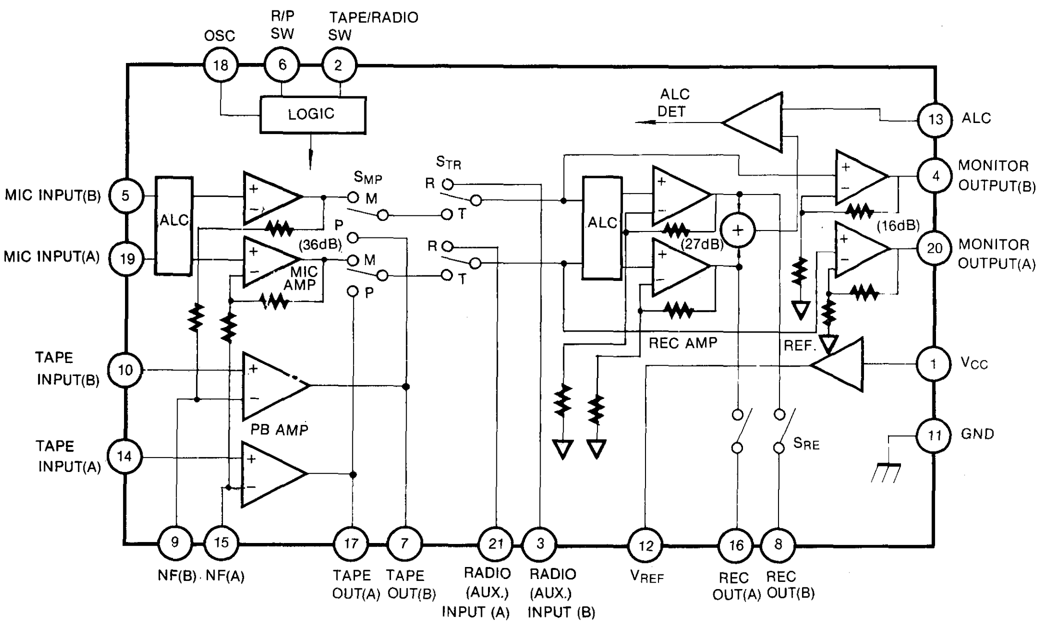


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	8	V
Power Dissipation	P_d	750	mW
Operating Temperature	T_{opr}	−25 ~ +75	°C
Storage Temperature	T_{stg}	−55 ~ +155	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 5V, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC1}	Radio, $V_i = 0$	7	10	14	mA
	I_{CC2}	Radio REC, $V_i = 0$	10	13	16	mA
	I_{CC3}	Tape PB, $V_i = 0$	7	10	14	mA
	I_{CC4}	Mic REC, $V_i = 0$	6	9	12	mA
Reference Voltage	V_{ref}		1.8	2.0	2.3	V
MONITOR AMP						
Voltage Gain	A_{V1}	$V_i = -50dBv$	14	16	18	dB
Maximum Output Voltage	V_{OM1}	THD = 1%	1.0	1.3		V
Total Harmonic Distortion	THD_1	$V_O = -10dBv$		0.06	0.2	%
Output Noise Voltage	V_{NO1}	Audio Band		14	30	μV
Cross Talk	CT_1	$V_O = 0dBv$	45	60		dB
Ripple Rejection Ratio	RR_1	$V_r = -20dBv$ f = 120Hz		50		dB
PLAY BACK AMP						
Closed Loop Voltage Gain	A_{V2}	$V_i = -50dBv$	35	38	41	dB
Open Loop Voltage Gain	A_{VO2}	$V_i = -90dBv$	70	78		dB
Maximum Output Voltage	V_{OM2}	THD = 1%	1.0	1.3		V
Total Harmonic Distortion	THD_2	$V_O = -10dBv$		0.02		%
Output Noise Voltage	V_{NO2}	Audio Band		80	150	μV
Cross Talk	CT_2	$V_O = 0dBv$	55	65		dB
Ripple Rejection Ratio	RR_2	$V_R = -20dBv$ f = 120Hz	34	42		dB

3

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
RECORDING AMP						
Voltage Gain	A_{V3}	$V_i = -50dBv$	24	27	30	dB
Total Harmonic Distortion	THD_3	$V_O = -10dBv$		0.04		%
Output Noise Voltage	V_{NO3}	Audio Band		120	250	μV
Cross Talk	CT_3	$V_O = -10dBv$, Audio Band	55	65		dB
Ripple Rejection Ratio	RR_3	$V_r = -20dBv$, $f = 120Hz$	34	42		dB
ALC Voltage	ALC_{31}	$V_i = -20dBv$	−4.4	−2.7	0	dBv
ALC Voltage	ALC_{32}	$V_i = -15dBv$	−4.2	−2.5	0.2	dBv
ALC Voltage	ALC_{33}	$V_i = -5dBv$	−4.0	−2.2	0.5	dBv
MIC + REC AMP						
Voltage Gain	A_{V4}	$V_i = -80dBv$	60	63	66	dB
Total Harmonic Distortion	THD_4	$V_O = -10dBv$		0.7	2.0	%
Output Noise Voltage	V_{NO4}	Audio Band		3.5	7.0	mv
Cross Talk	CT_4	$V_O = -10dBv$	30	43		dB
Ripple Rejection Ratio	RR_4	$V_R = -20dBv$, $f = 120Hz$	13	20		dB
ALC Voltage	ALC_{41}	$V_i = -60dBv$	−4.0	−2.0	0.5	dBv
ALC Voltage	ALC_{42}	$V_i = -40dBv$	−4.0	−2.0	0.5	dBv
ALC Voltage	ALC_{43}	$V_i = -10dBv$	−4.0	−2.0	0.5	dBv

OPERATION MODE BY EXTERNAL SWITCHES (S1, S2) COMBINATION

CIRCUIT BLOCK (S2 / S1)	S2 = REC		S2 = PLAY	
	S1 = RADIO	S1 = TAPE	S1 = RADIO	S1 = TAPE
MIC AMP	ON	ON	OFF	OFF
PB AMP	OFF	OFF	ON	ON
REC AMP	ON	ON	OFF	OFF
MONITOR AMP	ON	OFF	ON	ON
SMP	M	M	P	P
STR	R	T	R	T
SRE	ON	ON	OFF	OFF
OPERATION MODE	RADIO REC	MIC REC	RADIO PLAY	TAPE PLAY BACK

CONTROL SWITCH TERMINAL (2-, 6-PIN) THRESHOLD VOLTAGE

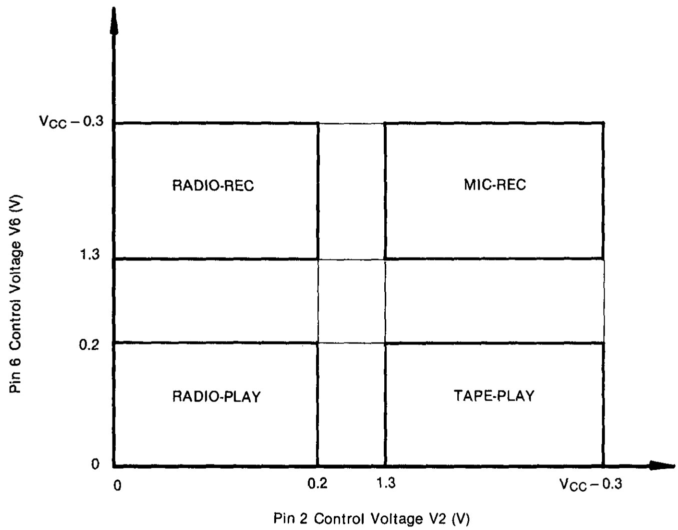


Fig. 2

TEST METHOD (See Test Circuit)

Symbol	S1	S2	S3	S4
I_{CC1}	RADIO	PLAY	a	DC
I_{CC2}	RADIO	REC	〃	〃
I_{CC3}	TAPE	PLAY	〃	〃
I_{CC4}	TAPE	REC	〃	〃
V_{REF}	—	—	〃	〃
A_{V1}	RADIO	REC	a	DC
V_O m1	〃	〃	〃	〃
V_{NO1}	〃	〃	〃	〃
THD_1	〃	〃	〃	〃
CT_1	〃	〃	〃	〃
RR_1	RADIO	REC	a	AC
A_{VO2}	TAPE	PLAY	b	DC
A_{V2}	TAPE	PLAY	a	DC
V_{OM2}	〃	〃	〃	〃
V_{NO2}	〃	〃	〃	〃
THD_2	〃	〃	〃	〃
CT_2	〃	〃	〃	〃
RR_2	TAPE	PLAY	a	AC

Symbol	S1	S2	S3	S4
A_{V3}	RADIO	REC	a	DC
V_{NO3}	〃	〃	〃	〃
THD_3	〃	〃	〃	〃
CT_3	〃	〃	〃	〃
RR_3	RADIO	REC	a	AC
ALC_{31}	RADIO	REC	a	DC
ALC_{32}	〃	〃	〃	〃
ALC_{33}	〃	〃	〃	〃
A_{V4}	TAPE	REC	a	DC
V_{NO4}	〃	〃	〃	〃
THD_4	〃	〃	〃	〃
CT_4	〃	〃	〃	〃
RR_4	TAPE	REC	a	AC
ALC_{41}	TAPE	REC	a	DC
ALC_{42}	〃	〃	〃	〃
ALC_{43}	〃	〃	〃	〃

TEST CIRCUIT

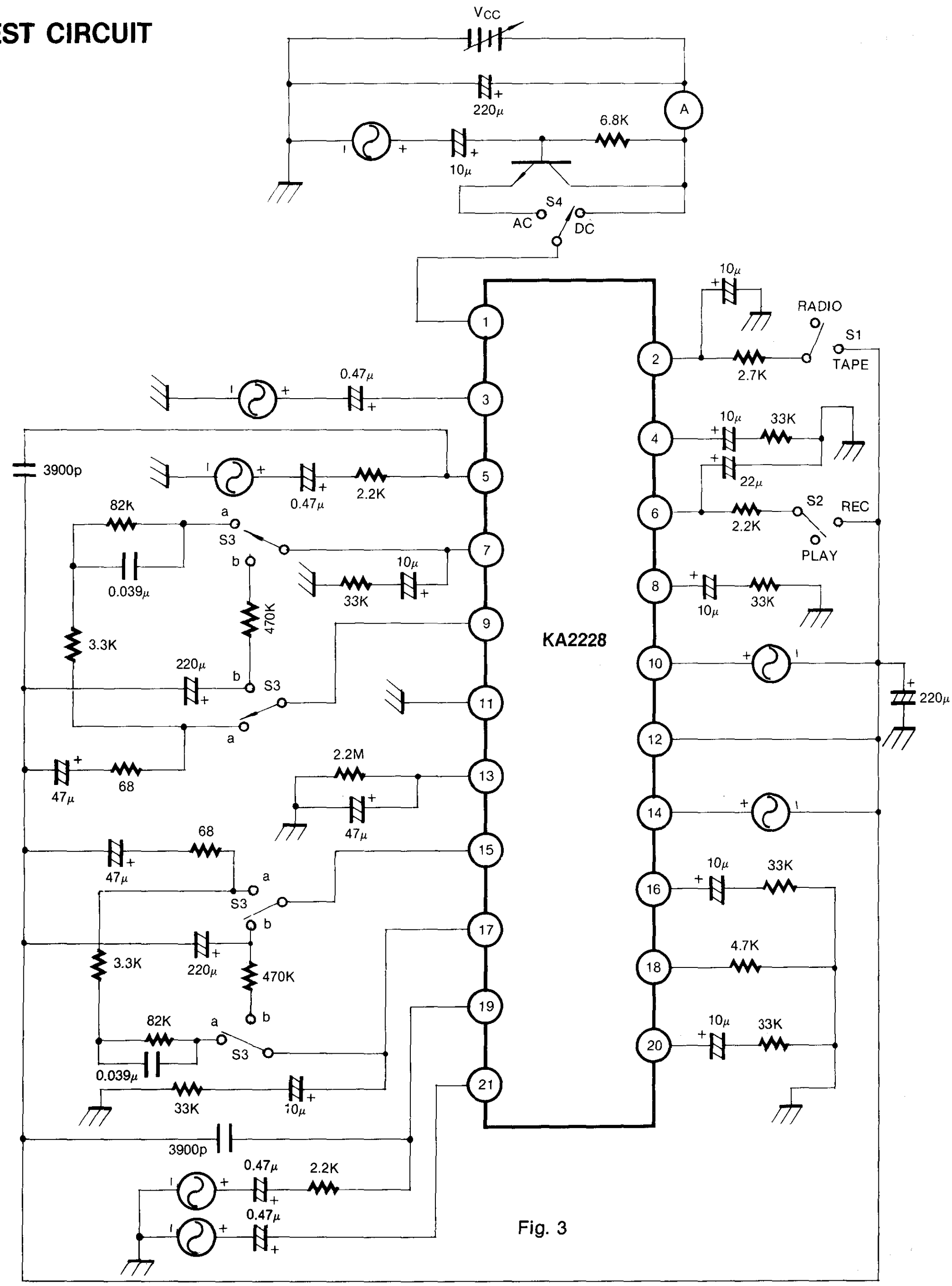


Fig. 3

APPLICATION CIRCUIT

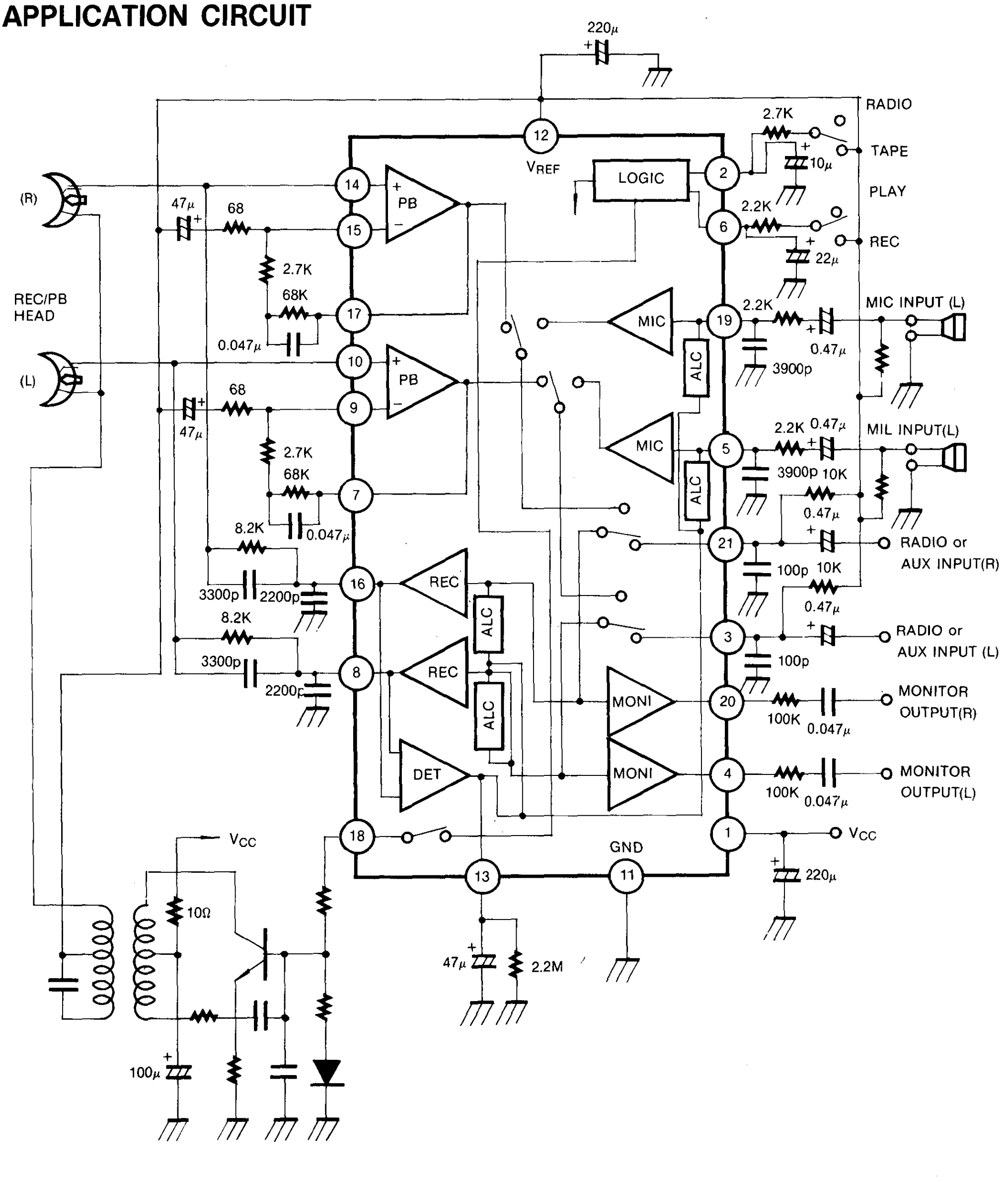
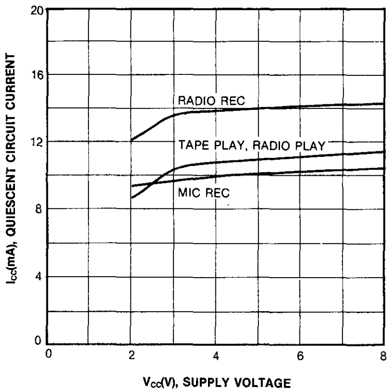
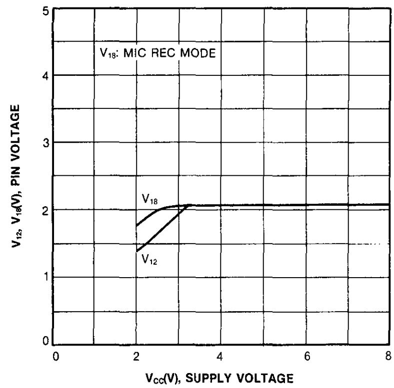


Fig. 4

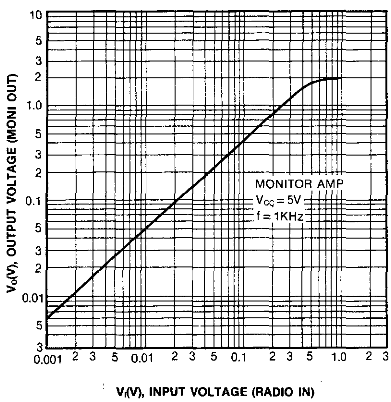
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



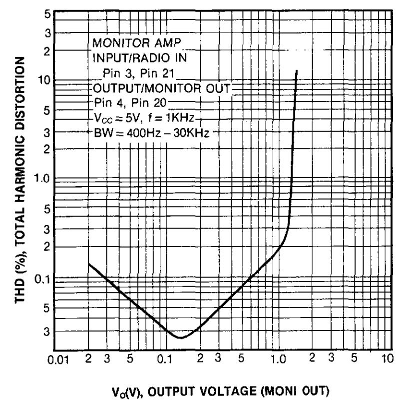
PIN VOLTAGE-SUPPLY VOLTAGE



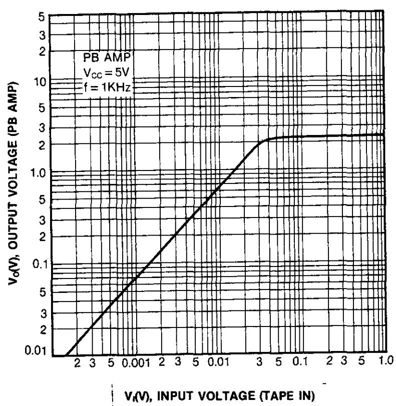
OUTPUT VOLTAGE-INPUT VOLTAGE



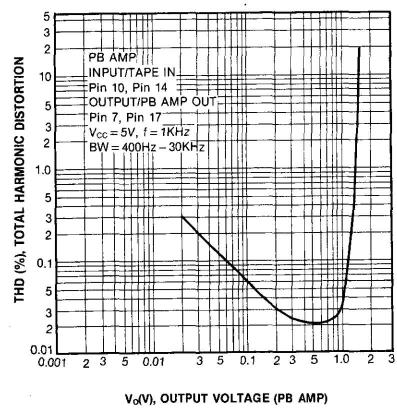
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



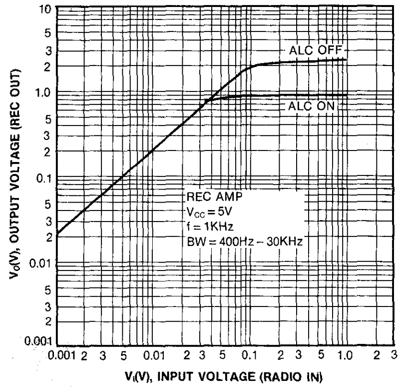
OUTPUT VOLTAGE-INPUT VOLTAGE



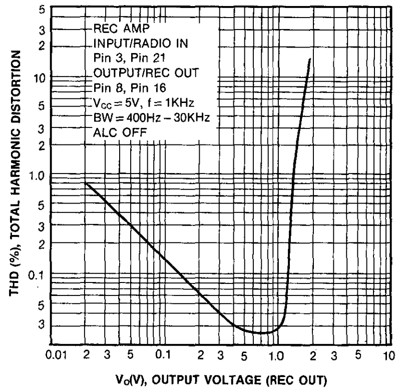
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



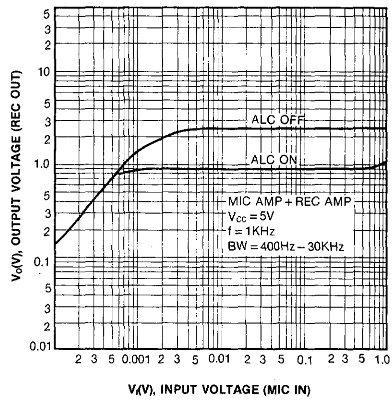
OUTPUT VOLTAGE-INPUT VOLTAGE



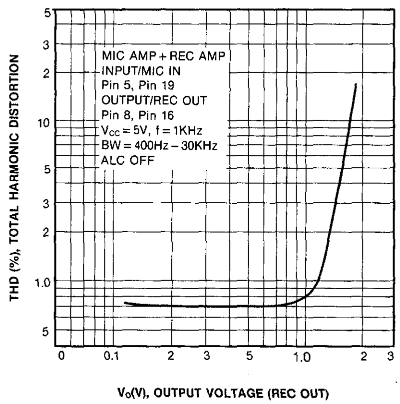
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



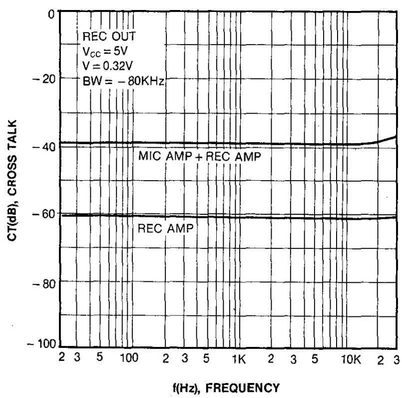
OUTPUT VOLTAGE-INPUT VOLTAGE



TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



CROSS TALK-FREQUENCY



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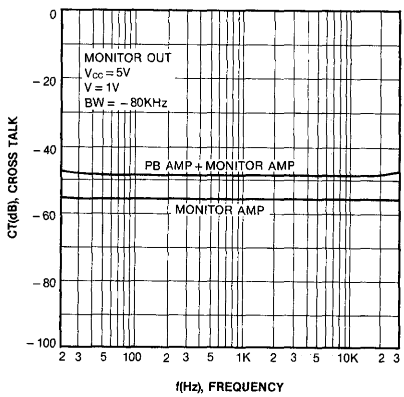
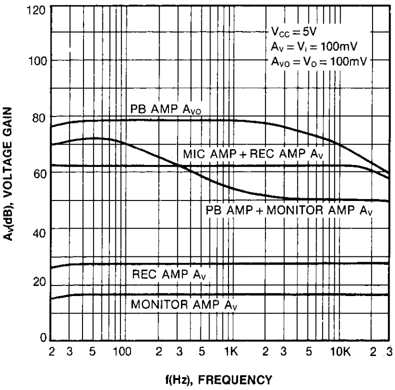
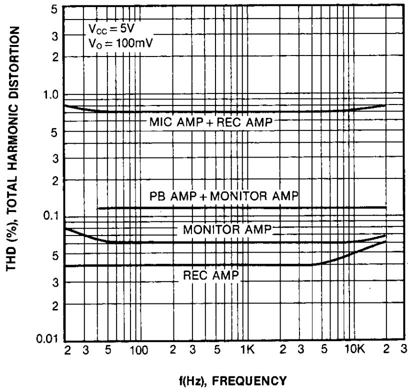


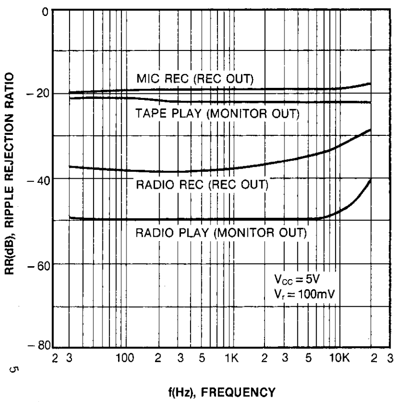
VOLTAGE GAIN-FREQUENCY



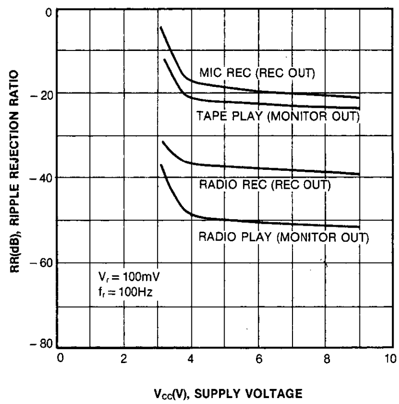
TOTAL HARMONIC DISTORTION-FREQUENCY



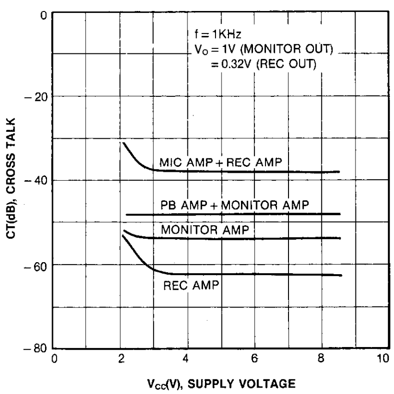
RIPPLE REJECTION RATIO-FREQUENCY



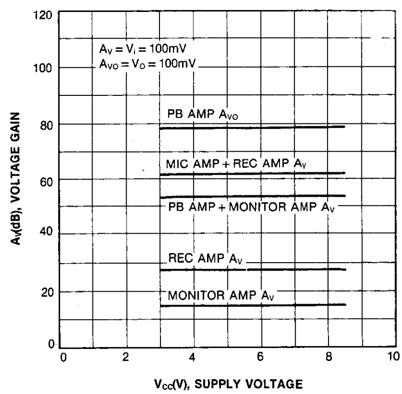
RIPPLE REJECTION RATIO-SUPPLY VOLTAGE



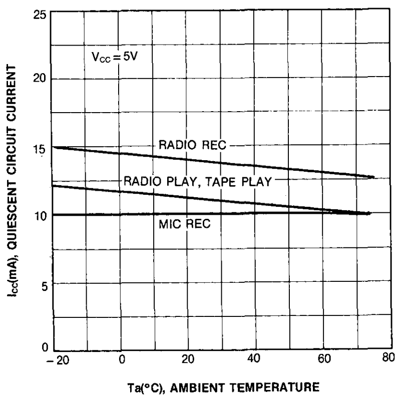
CROSS TALK-SUPPLY VOLTAGE



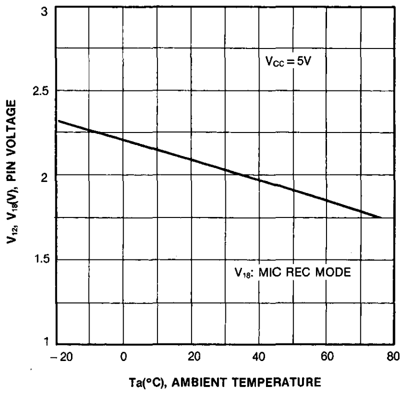
VOLTAGE GAIN SUPPLY-VOLTAGE



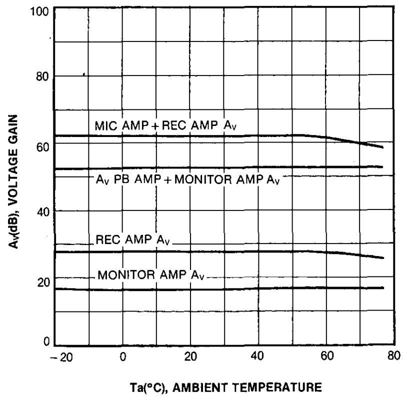
QUIESCENT CIRCUIT CURRENT -AMBIENT TEMPERATURE



PIN 12, 18 VOLTAGE-AMBIENT TEMPERATURE



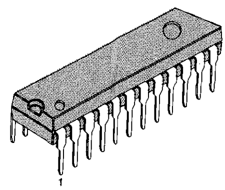
VOLTAGE GAIN AMBIENT TEMPERATURE



PLAYBACK/RECORD PRE AMPLIFIER FOR DOUBLE DECK

The KA22291 is a monolithic integrated circuit consisting of a dual input playback amplifier, a channel for double or auto-reverse operation and a two-channel record amplifier.
It is suitable for 6V-9V double deck or auto-reverse cassette applications.

24 SDIP



FEATURES

- **Dual input two-channel playback amplifier**
- **Two-channel record amplifier**
- **Built in ALC and Muting circuit**
- **PB/REC and playback input select switch included**
- **Power ON ALC discharge circuit included**
- **Operating supply voltage: 4V-12V**
- **REC/PB power on quick start circuit**
- **Few external part required.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22291	24 SDIP	−25∼ +75°C

BLOCK DIAGRAM

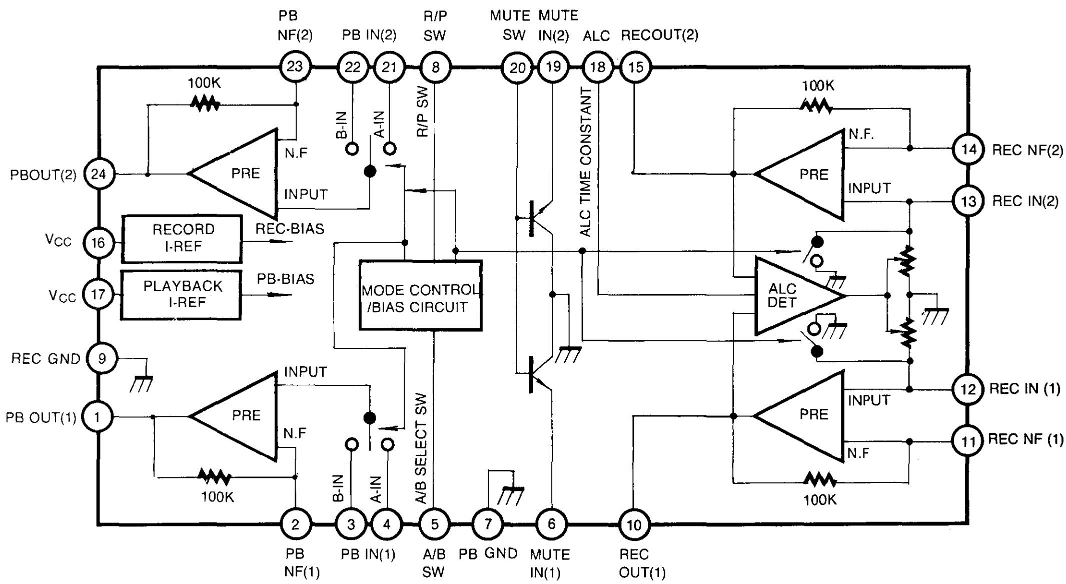


Fig. 1

* These specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	12	V
Power Dissipation	P_d	1000	mW
Operating Temperature	T_{opr}	−25 ~ +75	°C
Storage Temperature	T_{stg}	−55 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 9V, f = 1KHz, unless otherwise specified)

Characteristic			Symbol	Test Condition	Min	Typ	Max	Unit
Circuit Current			I_{CC}	V_i = 0, REC MODE	10	18	26	mA
PLAYBACK	Open Loop Voltage Gain		A_{VO}	V_i = −80dBm	60	90		dB
	Max. Output Voltage		$V_O(1)$	THD = 1%, NAB	0.75	1.2		V
	Total Harmonic Distortion		THD(1)	V_O = 0.2V, NAB		0.05	0.3	%
	Cross Talk	Ch to Ch	CT(1)	V_O = 0.5V, NAB		−55	−45	dB
		Ain to Bin	CT(2)	V_O = 0.5V, NAB		−55	−45	dB
	Equivalent Input Noise Voltage		V_{NI}	Filter: 20Hz ~ 20KHz R_g = 2.2K, V_i = 0		1.2	2.2	μV
RECORD	Close Loop Voltage Gain		A_V	V_i = 68dBm, ALC off	58	60	62	dB
	Max. Output Voltage		$V_O(2)$	THD = 1%, ALC off	1.2	1.6		V
	Total Harmonic Distortion		THD(2)	V_O = 0dBm, ALC off		0.2	1	%
	ALC Output Voltage		ALC V_O	V_i = −20dBm	0.75	0.95	1.35	V
	ALC THD		THD(ALC)	V_i = −20dBm		0.2	1.0	%
	ALC Range		ALC(R)	V_i = −60dBm, +3dB UP	40	50		dB
	Cross Talk (ALC)		CT(3)	V_i = −50dBm		−55	−40	dB
RECORD TO PLAYBACK Cross Talk			CT(4)	REC input = 0 PLAY output = 0.5V		−55	−40	dB
Muting Range			Rmute	V_i = −20dBm		−55	−40	dB

*These specification are subject to change without notice.

TEST CIRCUIT

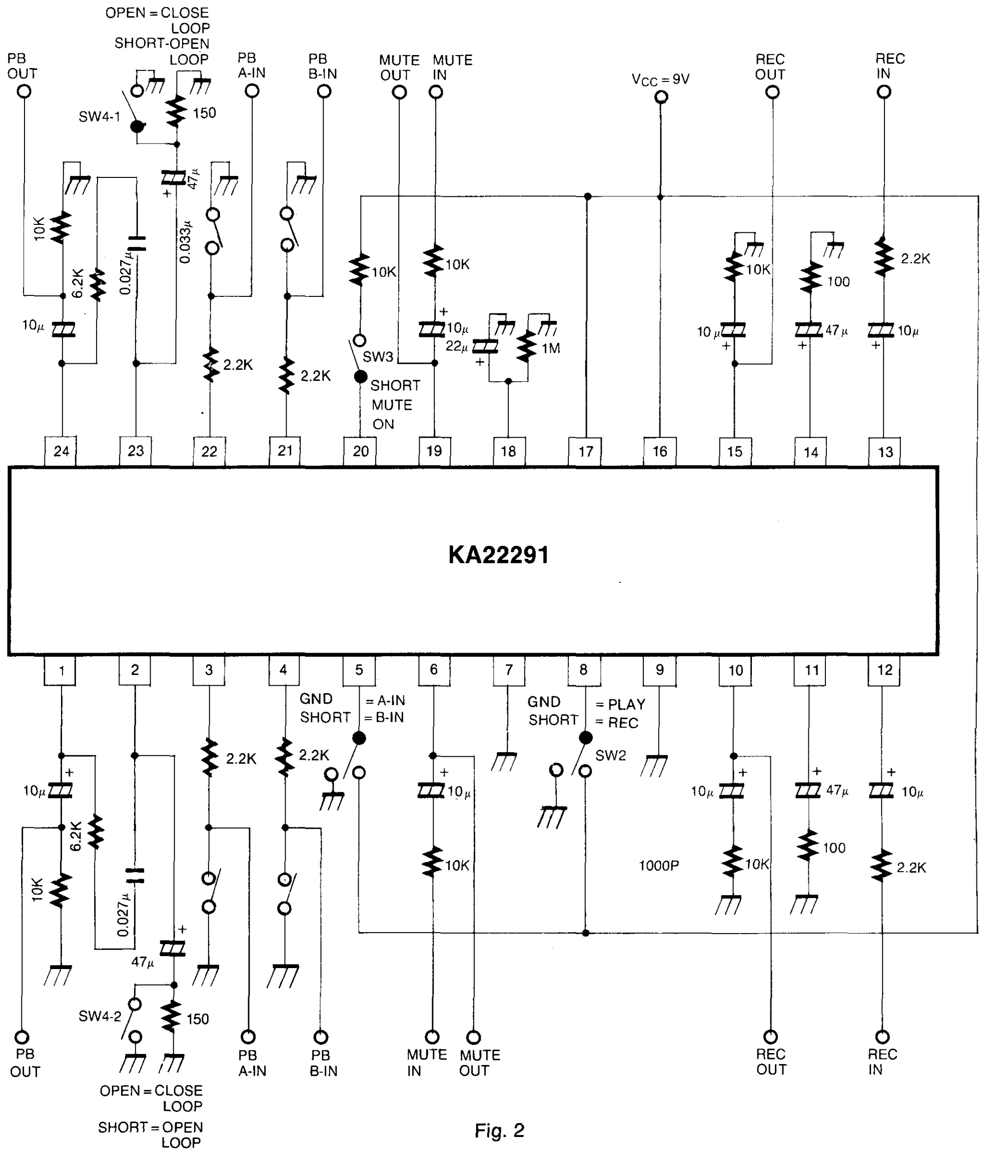


Fig. 2

* These specifications are subject to change without notice.

*INFORMATION OF MODE CHANGE

1. R/P SWITCH

Apply R/P input voltage at PIN 8.
PLAY: 0V (GND)
REC: 4.5V ~ 12V (Don't apply 13V above).
Only valid A/B input select in playback mode.
In record mode, the playback A-input was available and the ALC was turned on by record bias.

A. RECORD MODE SCHEMATIC

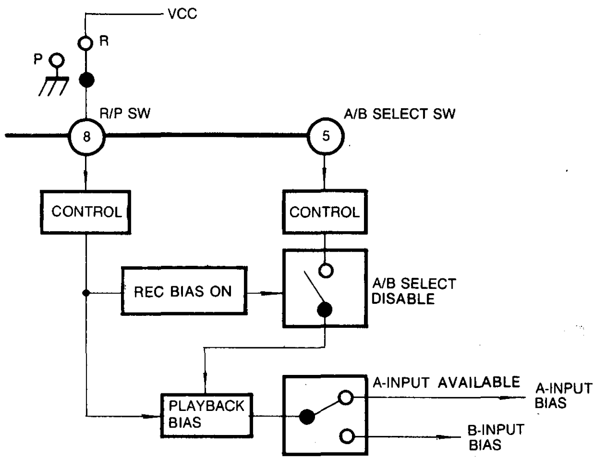


Fig. 3

B. PLAYBACK MODE SCHEMATIC

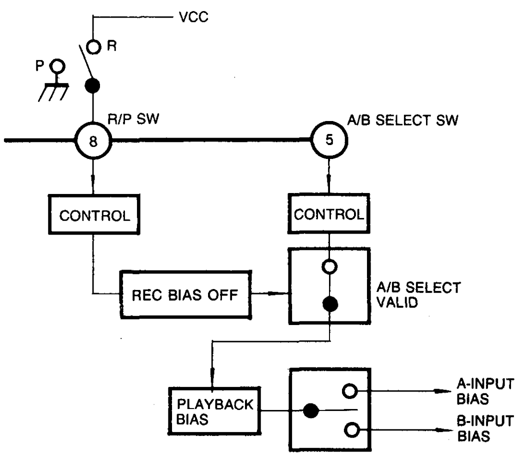


Fig. 4

* These specifications are subject to change without notice.

2. PLAYBACK A/B INPUT SELECT SWITCH (only playback mode)

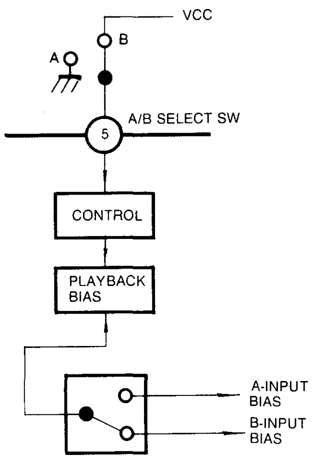


Fig. 5

3. MUTE SWITCH

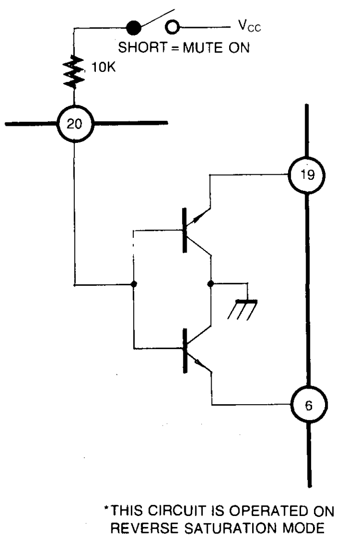


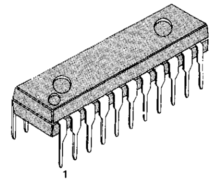
Fig. 6

*These specification are subject to change without notice.

9-PROGRAM MUSIC SELECTOR

The KA2230 is an automatic music selector IC which can scan and detect the start point of up to 9-programs. Selection of the program number can be taken by pressing the select button number times in succession. After, the setting of the program count, the display changes one program at a time until the preselected program is reached, at which point the control output is set on. The display is a 7-segment numeric display. It is suitable for radio cassettes, cassette decks and car stereos.

22 DIP



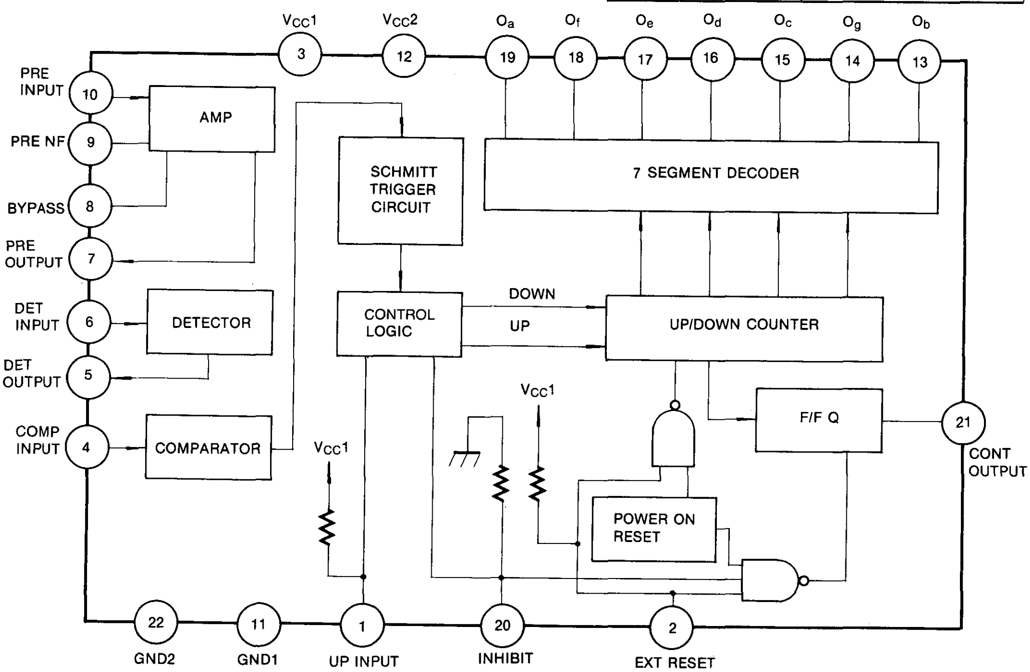
FEATURES

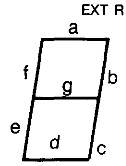
- **Maximum 9-program random search**
- **On-chip amplifier, detector, comparator**
- **On-chip automatic reset circuit**
- **7-segment of numerical display**
- **Operating supply voltage: $V_{CC}=5\sim14V$**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2230	22 DIP	$-20\sim+70°C$

BLOCK DIAGRAM





The segment output pins $O_a\sim O_g$ accord to the numerical display segment a$\sim$g.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Condition	Value	Unit
Supply Voltage	$V_{CC}1$		16	V
Supply Voltage	$V_{CC}2$		20	V
Input Voltage	V_i	Except for the pre-amp or the detector input	$0 \sim V_{CC}1$	V
7-Segment Display Current	I_d		20	mA
Control Output Voltage	V_o		20	V
Control Output Current	I_o		50	mA
Power Dissipation	P_d	Ta = 25°C	850	mW
Derating		Ta ≤ 25°C	12.5	mW/°C
Operating Temperature	T_{opr}		−20 ~ +70	°C
Storage Temperature	T_{stg}		−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 9V, f = 10KHz, R_g = 600Ω, 0dB = 1Vrms, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	T/F
Operating Supply Voltage	V_{CC}	−20 ~ +60°C	5	9	14	V	
Quiescent Circuit Current	$I_{CC}1$	$V_i = 0$		8	12	mA	1
	I_{CC2}*	I_d = 20mA, at the reset		125	130		
Input Level							
Input Threshold Level	V_{ith}	A_v = 53dB	−60	−58	−55	dBv	2.3
Frequency Characteristics	F_{vih}	V_{ih}, $V_{il} = V_{ith}$ + 3dB	40	56		KHz	
	F_{vil}			600	800	Hz	
Input Threshold Level Variation by a Supply Voltage	V_{id}	The difference of V_{ith} between V_{CC} = 9V and 5V		1	2	dB	
Maximum Input Voltage	V_i (max)		350			mV	
Release Time	T_{dl}	V_i = −37dB ~ −97dB		250		ms	2.3
Release Time Variation by a Supply Voltage	T_{dld}	Difference of T_{dl}, V_{CC} = 9V and 5V		10		ms	
Attact Time	T_{dh}	V (pin6) = 0V − 3V		5		ms	4
Attact Time Variation by a Supply Voltage	T_{dhd}	Difference of T_{dh}, V_{CC} = 9V and 5V'		0.1		ms	
Pre-Amp							
Input Resistance	R_i	A_v = 53dB	37	47	57	KΩ	5
Output Noise Voltage	V_{no}	A_v = 53dB, R_g = 100KΩ			20	mV	6
Open Loop Voltage Gain	A_{vo}	V_i = −90dB	65	68	72	dB	7

* I_{CC} = 5mA + XId, X: The number of 7-segment display Bit-on at the reset.

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	T/F
Control-Output							
Saturation VTG (turn on)	V_o (sat)	$I_o = 50mA$			0.5	V	
Leakage Current (turn off)	I_o (leak)				5	μA	
7-Segment Display Output							
Output Voltage (turn on)	V_{dh}	$I_o = 20mA$	7			V	
Leakage Current (turn off)	I_o (leak)				1	μA	
Up Input, Reset Input							
Input Voltage (H)	V_{ih}		2			V	
Input Voltage (L)	V_{il}				1	V	
Input Current	I_{il}			250	500	μA	
Inhibit							
Input Voltage (H)	V_{ih}		1.8			V	
Input Voltage (L)	V_{il}				1	V	
Input Current	I_{ih}			350	700	μA	
Hysteresis Width				100		mV	

PIN CONNECTIONS

Pin No.	Pin Name	Pin No.	Pin Name
1	Up Input	12	$V_{CC}2$
2	Reset	13	7-Segment Display Output (b)
3	$V_{CC}1$	14	7-Segment Display Output (g)
4	Comparator Input	15	7-Segment Display Output (c)
5	Detector Output	16	7-Segment Display Output (d)
6	Detector Input	17	7-Segment Display Output (e)
7	Pre-Amp Output	18	7-Segment Display Output (f)
8	Bypass	19	7-Segment Display Output (a)
9	Pre-Amp Negative Feedback	20	Inhibit
10	Pre-Amp Input	21	Control Output
11	GND 1	22	GND 2

TEST CIRCUIT

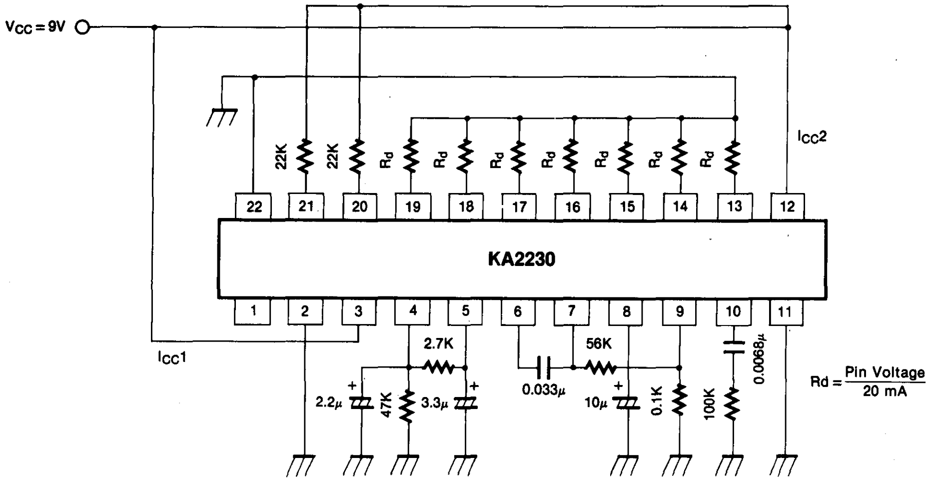


Fig. 1

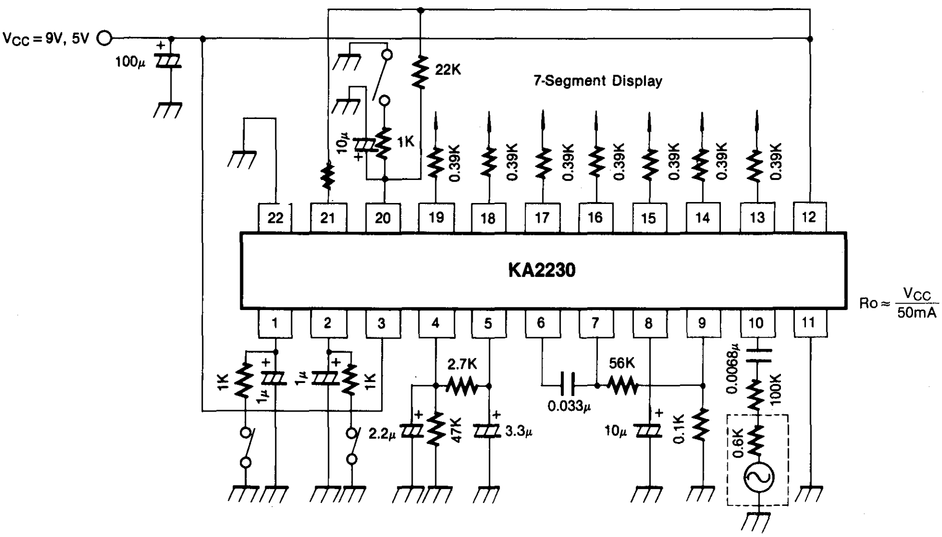


Fig. 2

TEST CIRCUIT (Continued)

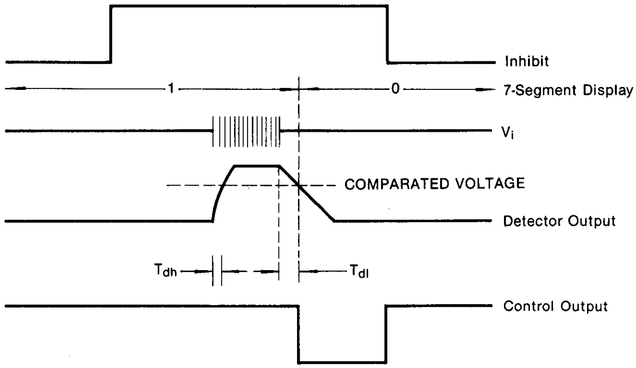


Fig. 3

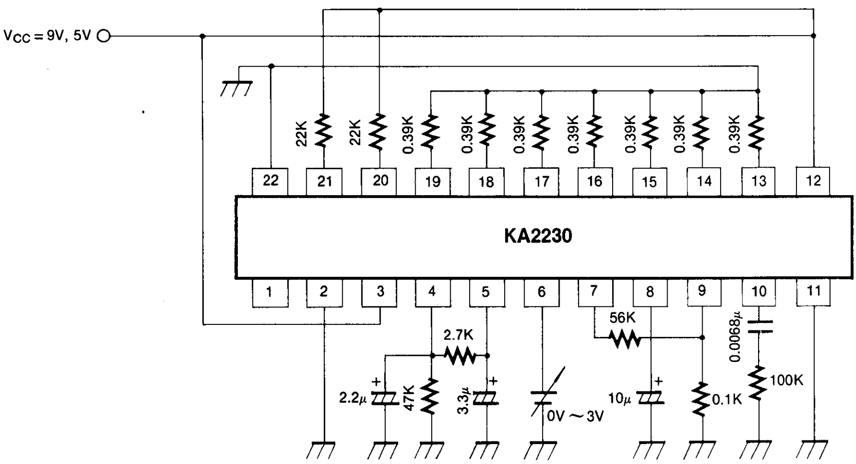


Fig. 4

TEST CIRCUIT (Continued)

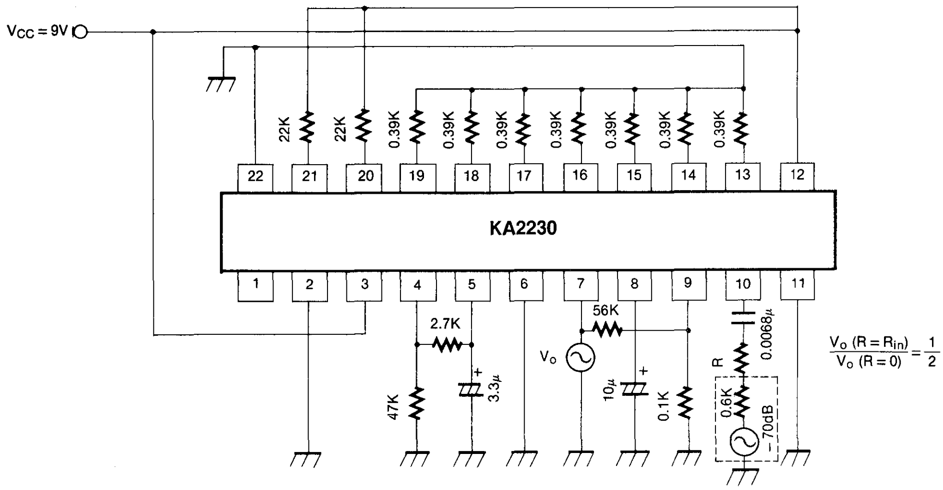


Fig. 5

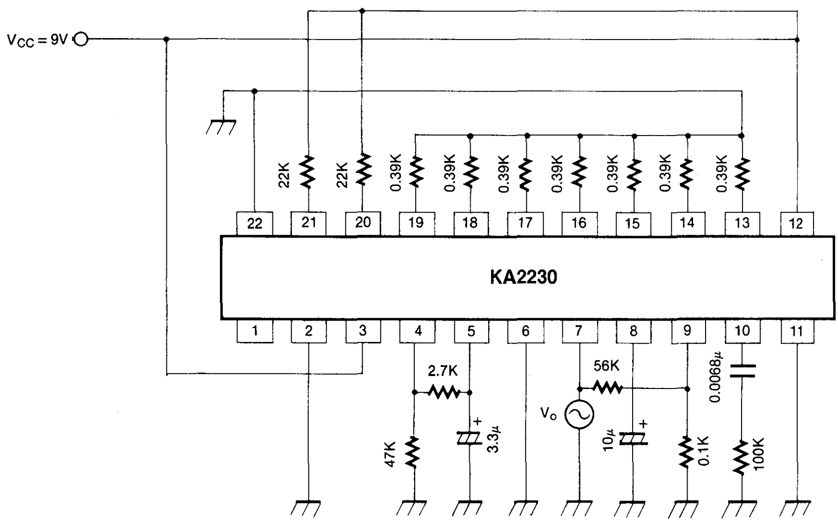


Fig. 6

TEST CIRCUIT (Continued)

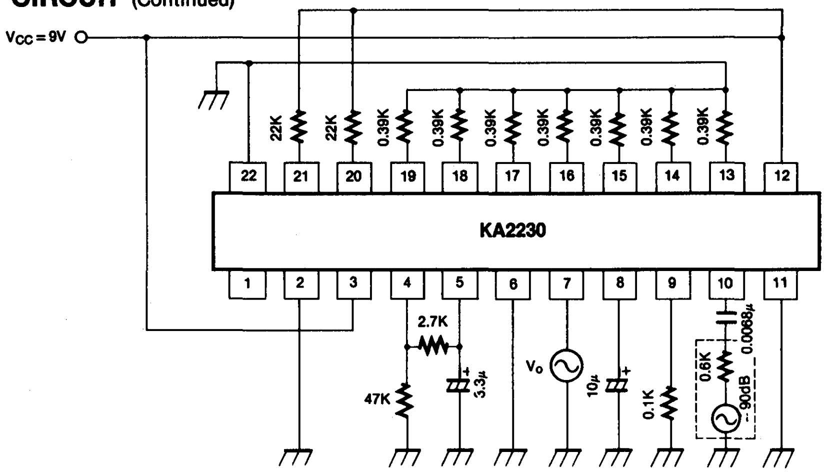


Fig. 7

FUNCTION DESCRIPTION

(1) Auto Reset

The Power-on reset circuit is reset between V_{CC} = 1.7~4V on the rise of the supply voltage, while the control output turns off with the segment output initialized to 0 PROGRAM.

(2) Up

The UP-input pin going from "High" to "Low" level counts up on its rise.
(The segment output goes PROGRAM 0~1→PROGRAM 2→PROGRAM 3→PROGRAM 4→PROGRAM 5→PROGRAM 6→PROGRAM 7→PROGRAM 8→PROGRAM 9→PROGRAM 1→PROGRAM 2)

(3) Down

The signal input, amplified and detected, is supplied as DC voltage to the comparator circuit. The down-count takes place when the comparator circuit input falls from the "High" to "Low" level.
(The segment output goes PROGRAM 9→PROGRAM 8→PROGRAM 7→PROGRAM 6→PROGRAM 5→PROGRAM 4→PROGRAM 3→PROGRAM 2→PROGRAM 1→PROGRAM 0→PROGRAM 0)
For down-count to proceed, INHIBIT should be at "High" level.

(4) Inhibit

Inhibits the down-count at the "Low" level and resets the control output.
The "High" level enables the down-count.

(5) Reset

Resets the segment output to Program 0 and control output to OFF.

(6) Control Output

The control output turns ON on the next down-count when the segment output is Programs 0 or 1. It can be reset again to OFF using the INHIBIT or RESET pin.

(7) Power Supply

Only the power supply for the segment output circuit is V_{CC2}, while the others are V_{CC1}.

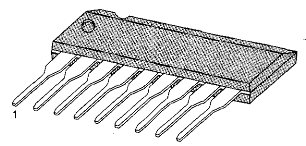
(8) GND

Only the GND of the control output circuit is GND2, while the others are GND1.
GND1 and GND2 should be at the same voltage.

AUDIO LEVEL SENSOR

The KA2231 is an interprogram spaces detection IC with the function of music selection and can be used for radio cassettes, cassette decks, and car stereos.

9 SIP



FEATURES

- **Built-in plunger driver TR (Max: 600mA).**
- **Built-in protection diode to prevent induced reverse voltage.**
- **Built-in protection circuit to prevent the error operation of the plunger, when power switching on.**
- **Built-in detector for detecting recorded area.**
- **Capable of desired timing setting by using external C.R.**
- **Detects unrecorded areas of tape and drives plunger.**
- **Wide operating supply voltage range: V_{CC} = 3.5V ~ 14V.**
- **Recommended operating supply voltage: V_{CC} = 9V.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2231	9 SIP	−20 ~ +70°C

BLOCK DIAGRAM

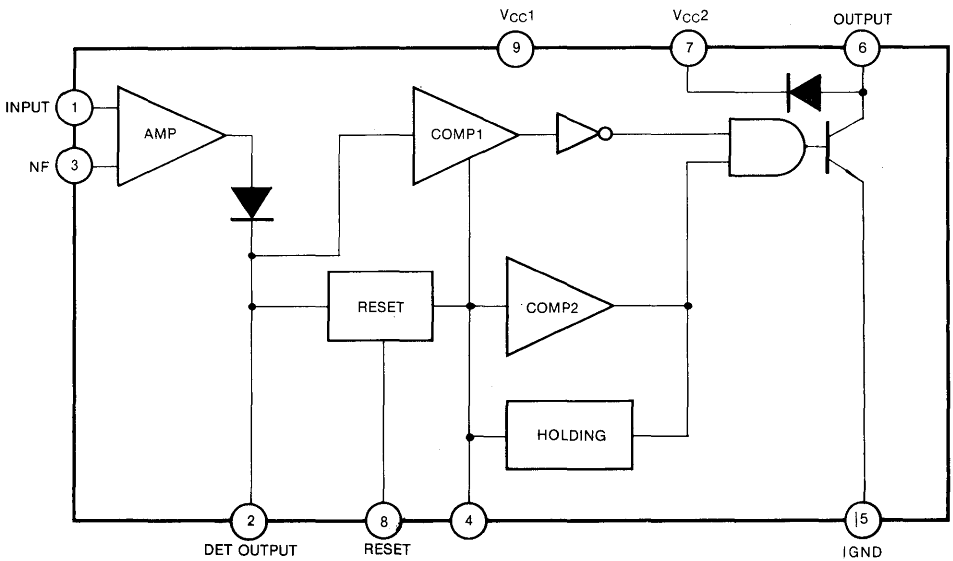


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Flow-in Current	I6	600	mA
Power Dissipation	P_D	540	mW
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 9V, f = 1KHz, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Circuit Current		I_{CC}	V_I = −30dBv		11	22	mA
Output TR Saturation VTG		V_{CE} (sat)	I_6 = 600mA		1.1	1.6	V
Output Diode Forward VTG		V_F	I_F = 600mA		1.5	2.0	V
Input Sensitivity		V_I (sen)	Pin6: L→H	−47	−50	−53	dBv
Comparator Level (1)	ON	V_{th} 1-H	Pin6 Inverted	3.0	3.5	4.0	V
	OFF	V_{th} 1-L	Pin6 Inverted	1.8	2.2	2.6	V
Comparator Level (2)	ON	V_{th} 2-H	Pin6 Inverted	4.7	5.5	6.3	V
	OFF	V_{th} 2-L	Pin6 Inverted	3.6	4.0	4.6	V
Pin4 Reset Level		V4	V_I = −30dBv, Pin8 = 1.0V		0.02	0.1	V
Pin8 Reset Voltage	1	V8R-1	Pin1 Inverted, R_g = 0	0.6	0.7	0.8	V
	2	V8R-2	V_I = −30dBv, Pin4 Inverted	1.1	1.3	1.5	V

TEST CIRCUIT

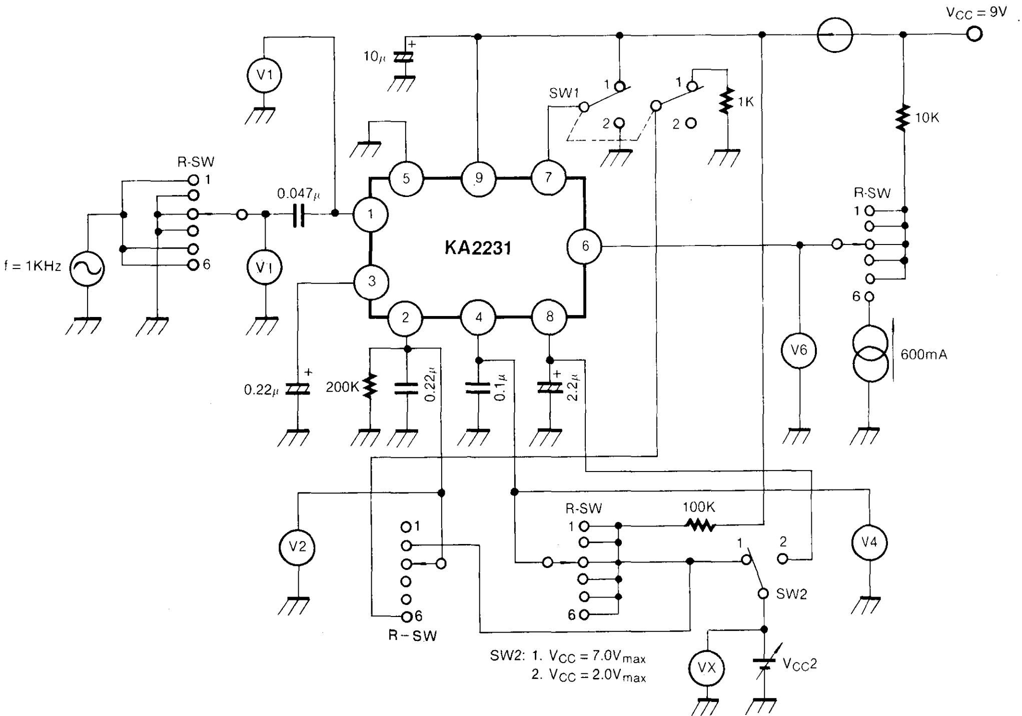


Fig. 2

TEST METHOD

Characteristic	R-SW	SW-1	SW-2	Test Method
Input Sensitivity	1	1	1	Measure AC input level V_I at Pin 6 L→H inversion mode
Circuit Current	5	1	1	Measure supply current
Output TR Saturation VTG	6	1	1	Measure Pin 6 voltage V6 at 600mA
Output diode forward VTG	6	2	1	Measure Pin 6 voltage V6 at 600mA
Comparator (1) ON Level	2	1	1	Measure Pin 2 V2 at Pin 6 L→H inversion mode
Comparator (1) OFF Level	2	1	1	Measure Pin 2 V2 at Pin 6 H→L inversion mode
Comparator (2) ON Level	3	1	1	Measure Pin 4 V4 at Pin 6 H→L inversion mode
Comparator (2) OFF Level	3	1	1	Measure Pin 4 V4 at Pin 6 L→H inversion mode
Pin 4 Reset Voltage	5	1	2	Measure Pin 4 voltage V4 at VX = 1V
Pin 8 Reset Voltage 1	4	1	2	Measure VX voltage at Pin 1 inversion mode
Pin 8 Reset Voltage 2	5	1	2	Measure VX voltage at Pin 4 inversion mode

APPLICATION CIRCUIT

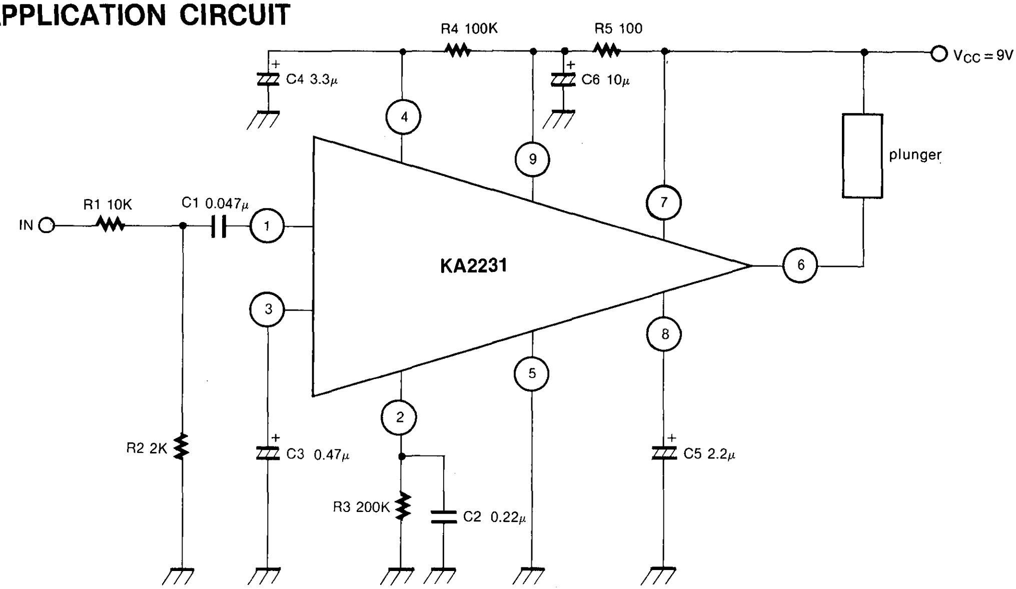


Fig. 4

EXTERNAL COMPONENTS

C1 : Input coupling capacitor
The recommended value is 0.047μF.

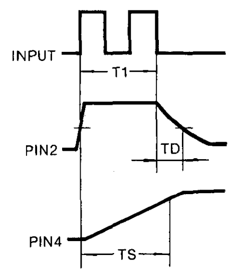
R1, R2 : Input level control resistor
Pin 1 is high in input impedance; in order to be free from external effect, R2 must not exceed 10KΩ and must be GND.

C2, R3 : Interprogram space detect time (TD)—setting capacitor and resistor
TD = 1.34 * C2 * R3 (sec)
It is recommended to use R3 of 150KΩ to 500KΩ.
It is recommended to use C2 of 0.22μF (Mylar Capacitor).

C3 : Negative feedback capacitor
The lower cut-off frequency depends on the value of this capacitor, and determined as follows:

$$C3 = \frac{1}{0.942 * f_L} (\mu F)$$

The recommended value is 0.47μF.



C4, R4 : Recorded area detect time (TS)—setting capacitor and resistor
The recorded area detect time is set by:
TS = C4 * R4 (msec)
It is recommended to use R4 of 100KΩ.
(The resistance value of R4 must be 50KΩ to 200KΩ)
It is recommended to use C4 of 1μF to 3.3μF.
(The capacitance value of C4 must not exceed 4.7μF)
For recorded area TS < T1 + TD
For unrecorded area TS > T1 + TD
Therefore, if the recorded area detect time (TS) is longer than the input signal time (T1) + the unrecorded area detect time (TD), no program is present.

C5 : For setting reset time.
The capacitor is used to set the time for initializing the circuit at the time of application power.
The reset pulse is generated for a certain period of time TR = 14.4 * C5 (msec), that is set each time power is applied.

C6, R5 : For power ripple filter.

TIMING CHART

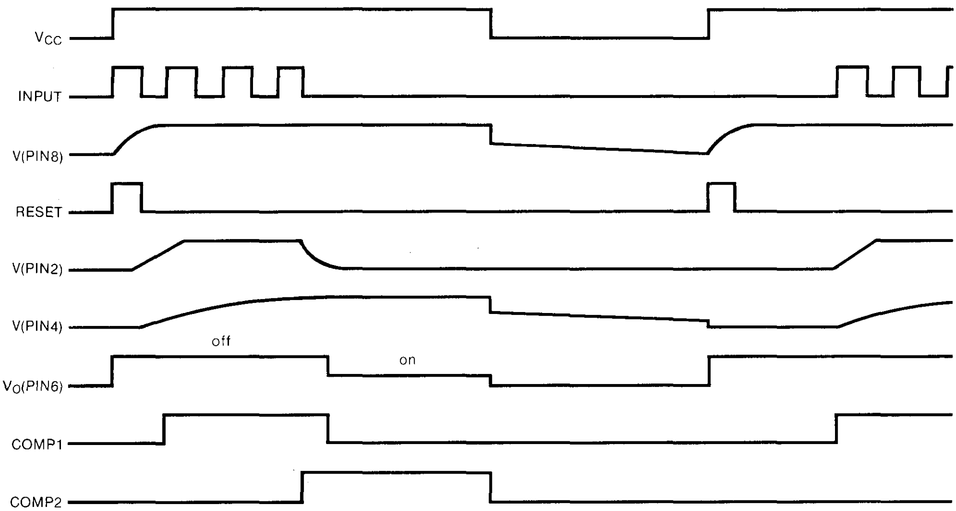


Fig. 5

DESCRIPTION OF OPERATION (See Timing Chart)

When the power supply is applied, the reset circuit operates to initialize the inner circuit. The reset time is determined by the capacitance value of C5 on Pin 8, and input signal is not accepted while the reset circuit is operating.

When the reset mode is released and the input signal exceeds the input check level, C2 and R3 on Pin 2 are charged and the potential on Pin 2 rises, therefore the comparator (1) is inverted.

When the comparator (1) is inverted, C4 on Pin 4 charged and the potential on Pin 4 begins rising.

When this potential exceeds the threshold voltage, the comparator (2) is inverted and program presence mode is memorized; thus the potential on Pin 4 is held at the high level. During this period of time, the output terminal (Pin 6) is held at the high level.

When the input signal disappears and the comparator (1) is inverted, the output terminal (Pin 6) turns to the low level, therefore causing the plunger to be driven.

The reset pulse is generated for a certain period of time whenever the power supply is applied, therefore causing the inner circuit to be initialized.

PROPER CARE IN USING ICs

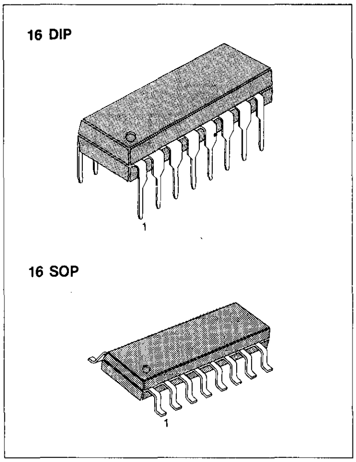
- Maximum Ratings
  If the maximum ratings are exceeded, breakdown or deterioration may result.
  Use the IC in the range where the maximum ratings are not exceeded.
- Pin to Pin Short and Inverted Insertion
  These may cause breakdown or deterioration to occur.
  Be extremely careful when mounting the IC on the board.
- The voltage on Pin 1 must not exceed that on Pin 9.
- The current flowing into Pin 2 and Pin 4 must not exceed +0.5mA continuously.
- The voltage on Pin 8 is 2.5V max. and must not exceed that on Pin 7.
- Electrolytic capacitors are used to set the recorded area detect time and reset time. The actual time constants are 15 to 20% larger than the calculated values obtained by using the catalog values of such capacitors.
  For polyester film capacitors and tantalum electrolytic capacitors, the calculated values hold to a fairly good approximation.

AM 1-CHIP RADIO

The KA22421 is a monolithic integrated circuit designed for the portable AM radio.

FUNCTIONS

- Converter
- IF Amp
- AM DET
- Power Amp



FEATURES

- **Portable AM 1-chip radio.**
- **Low quiescent current: I_{CC} = 1.6mA (Typ) at V_{CC} = 3V.**
- **Operating supply voltage range: V_{CC} = 2V ~ 5V.**
- **High power efficiency**
- **Power output: P_O = 100mW (Typ) at THD = 10%.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22421	16 DIP	−20 ~ +70°C
KA22421D	16 SOP	

BLOCK DIAGRAM

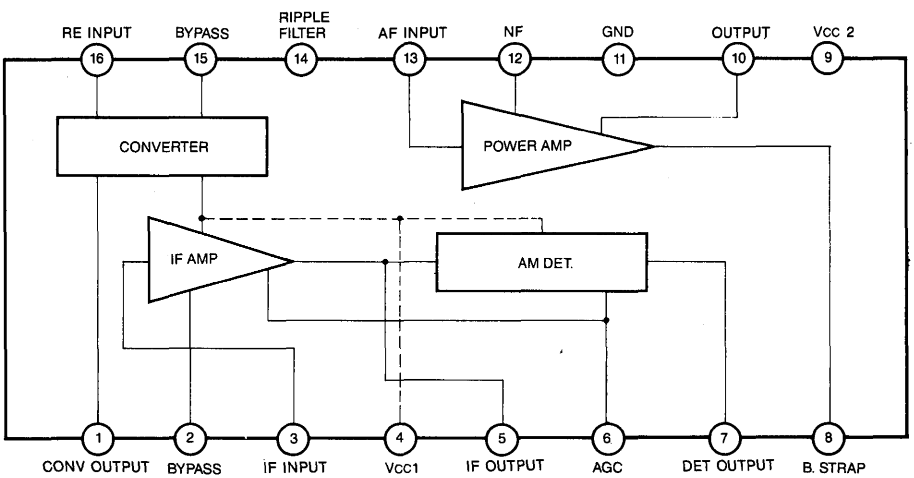


Fig. 1

3

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic		Symbol	Value	Unit
Supply Voltage		V_{CC}	6	V
Power Dissipation	KA22421	P_d	750	mW
	KA22421D		350	
Output Current		I_o (Peak)	0.2	A
Operating Temperature		T_{opr}	−20∼+70	°C
Storage Temperature		T_{stg}	−55∼+150	°C

Note: Derated above T_a=25°C in the proportion of 6mW/°C (KA22421D: 2.8mW/°C)

ELECTRICAL CHARACTERISTICS

(V_{CC}=3V, f=1MHz, f_m=1KHz, 30% Mod, R_g=50Ω, R_L=8Ω, T_a=25°C)

Characteristic	Symbol	Test Circuit	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	1	V_i=0	0.7	1.6	3.0	mA
Maximum Sensitivity	Max (Sen)	1	V_i=20dBμ, VR=Max	200			mV
Output Power	P_O	1	V_i=42dBμ, VR=Max	80	100		mW
Total Harmonic Distortion	THD	1	V_i=42dBμ V_O=200mV		2	6	%
Signal to Noise Ratio	S/N	1			44		dB
Output Noise Voltage	V_{NO}	1	V_i=0, VR=Max		3.5		mV
16-Pin Parallel Input Impedance	R_{IP} (16)	2	f=1MHz		500		KΩ
	C_{IP} (16)				2.5		pF
1-Pin Parallel Output Impedance	R_{OP} (1)	3	f=1MHz		500		KΩ
	C_{OP} (1)				3.9		pF
3-Pin Parallel Input Impedance	R_{IP} (3)	4	f=500KHz		60		KΩ
	C_{IP} (3)				2.2		pF
5-Pin Parallel Output Impedance	R_{OP} (5)	5	f=500KHz		100		KΩ
	C_{OP} (5)				3.0		pF

TEST CIRCUIT 1

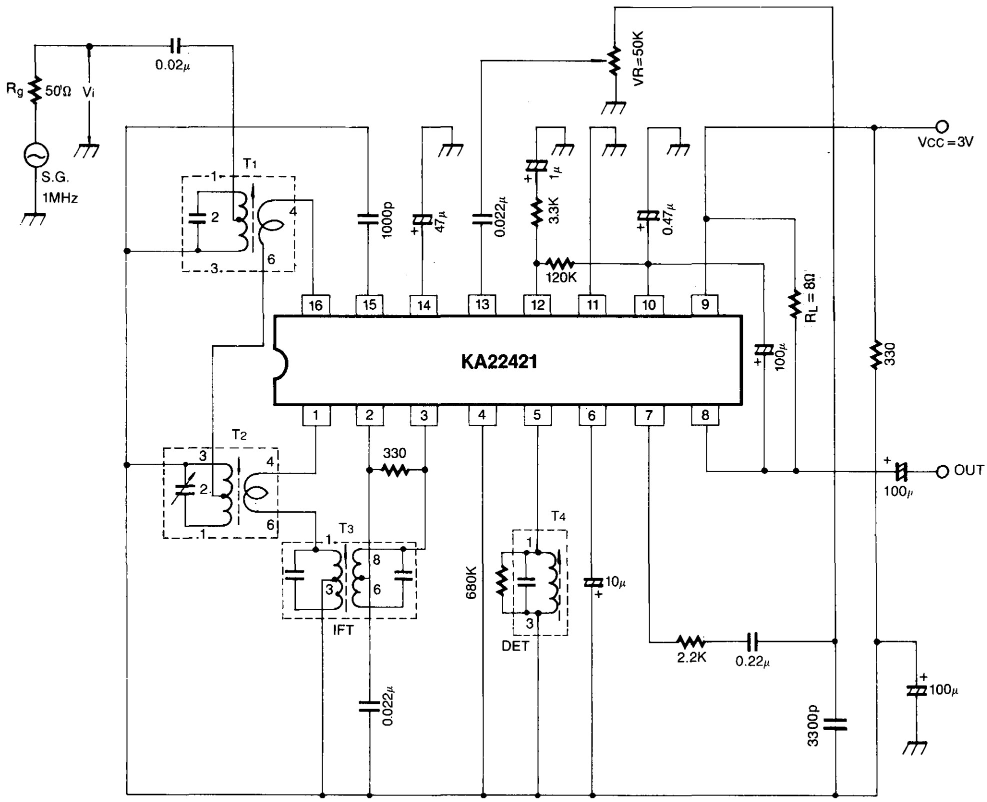


Fig. 2

TEST CIRCUIT 2

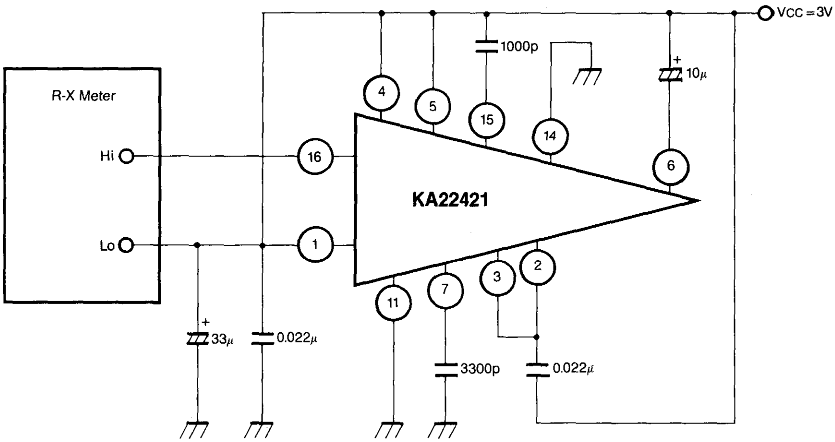


Fig. 3

TEST CIRCUIT 3

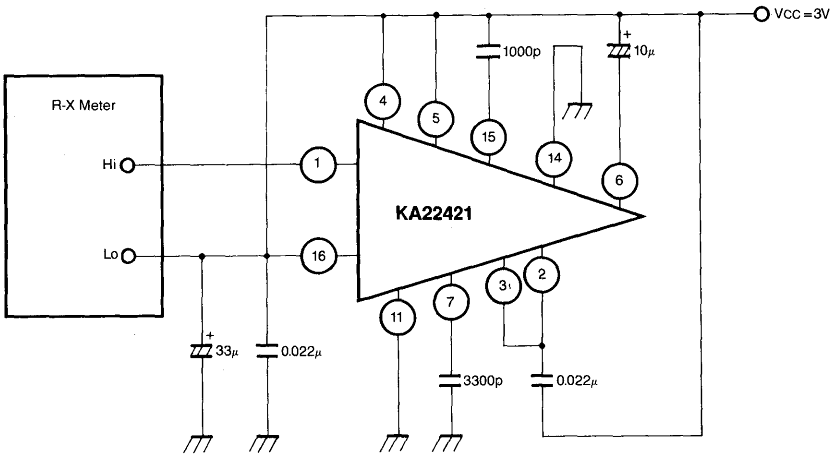


Fig. 4

TEST CIRCUIT 4

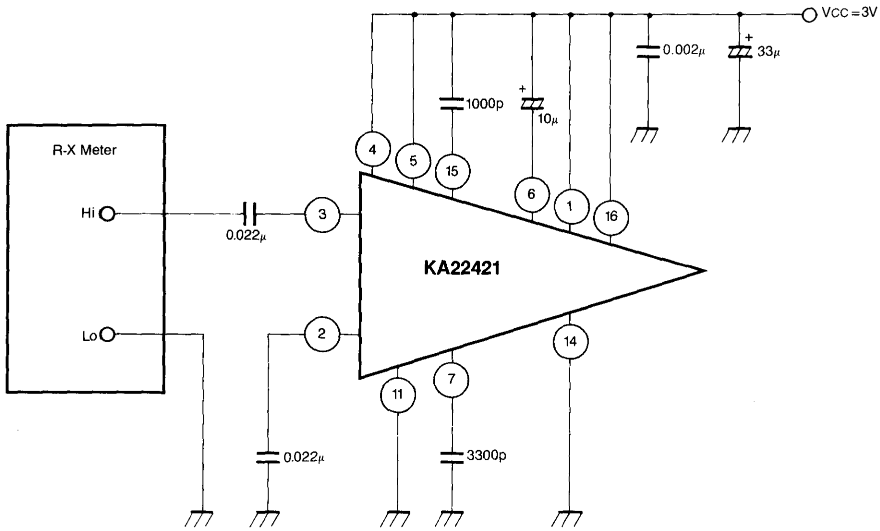


Fig. 5

TEST CIRCUIT 5

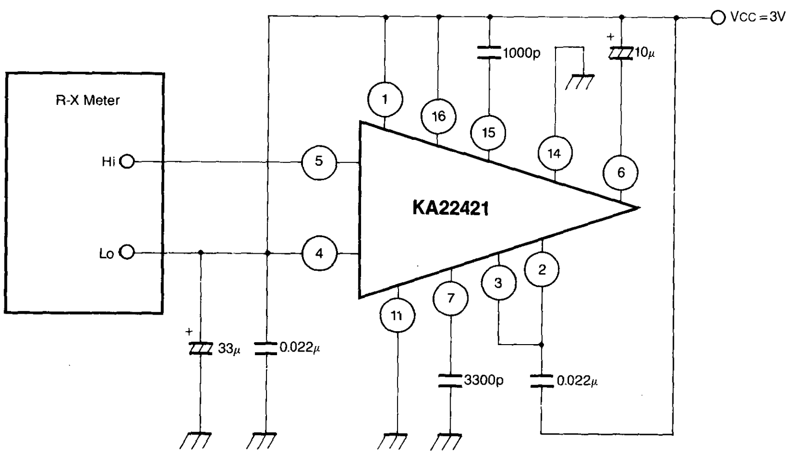


Fig. 6

APPLICATION CIRCUIT

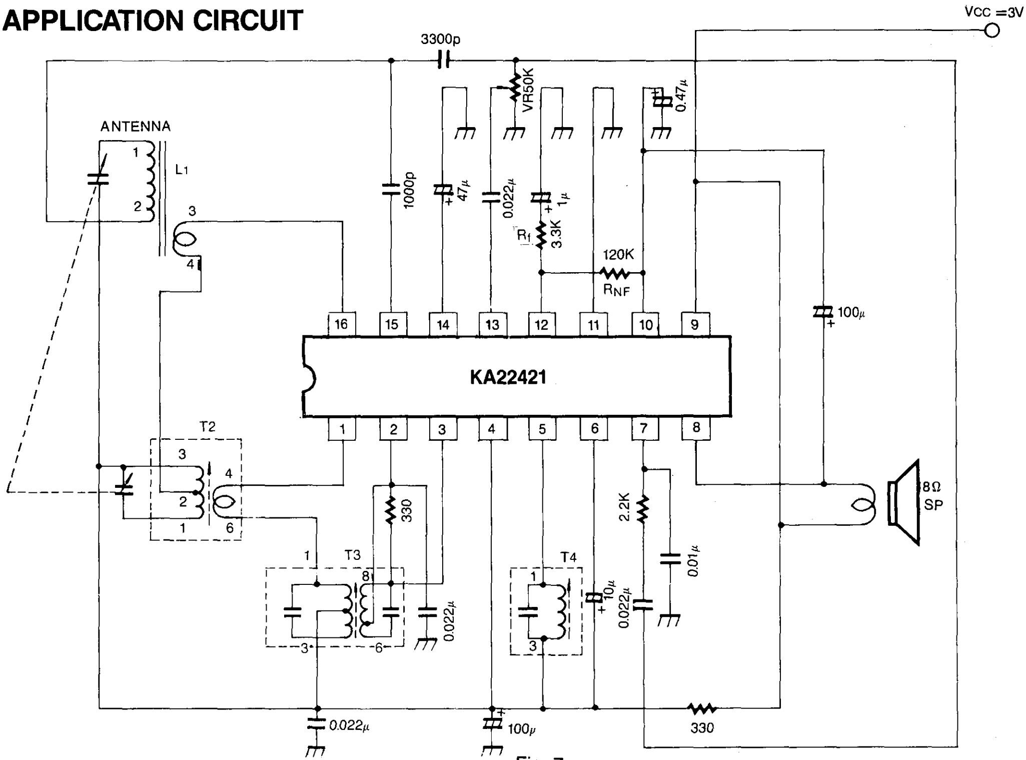


Fig. 7

ELECTRICAL CHARACTERISTICS (at application circuit)

(Unless otherwise specified T_a=25°C, V_{CC}=3V, f=1MHz, 30% Mod, R_L=8Ω, f_m=1KHz, R_g=50Ω)

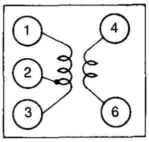
Characteristic	Symbol	Test Conditions	Typ. Value	Unit
Quiescent Circuit Current	I_{CC}	V_i=0	1.6	mA
Maximum Sensitivity	Max (Sen)	P_O=5mW	41	dB/m
Usable Sensitivity	Use (Sen)	S/N=20dB	49	dB/m
Signal to Noise Ratio	S/N	V_i=74dB/m	44	dB
AGC Ratio (Note 1)	AGC	−10dB Output Reduction (from 100dB/m)	50	dB
Recovered Output Voltage	V_{OD}	V_i=74dB/m Measure Pin 7	131	mV
Power Amplifier Voltage Gain (Note 2)	A_V	R_{NF}=120KΩ, R_f=3.3KΩ	26	dB
Output Power	P_O	THD=10%	100	mW
Total Harmonic Distortion	THD	V_i=74dB/m	2	%

Note 1. The AGC Ratio is defined as the input electric intensity ratio between the output voltage at 100dB/m and −10dB output voltage.

2. The open loop voltage gain of the power amplifier is typical 33dB.

COIL SPECIFICATIONS

T1 Antenna Coil



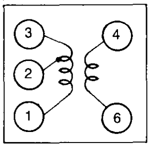
(Bottom View)

f (kHz)	L (μH)	Q_O	TURNS		
	1-3	1-3	1-2	2-3	4-6
300	600	115	2	130	8

KOREA TOKO

Wire: 0.07mmϕUEW

T2 OSC Coil



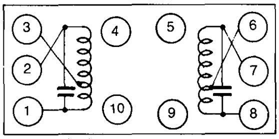
(Bottom View)

f (kHz)	L (μH)	Q_O	TURNS		
	1-3	1-3	1-2	2-3	4-6
796	360	125	$92\frac{1}{2}$	8	$10\frac{1}{2}$

KOREA TOKO

Wire: 0.08mmϕUEW

T3 AM IFT



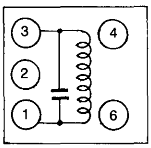
(Bottom View)

C_O (pF)		f (kHz)	Q_O	TURNS			
1-2	7-8		1-2 / 7-8	1-3	2-3	6-7	6-8
150	150	455	65	80	148	196	32

KOREA TOKO

Wire: 0.08mmϕUEW

T4 Detector Coil



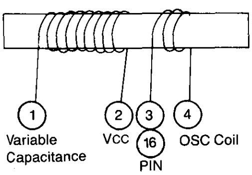
(Bottom View)

C_O (pF)	f (kHz)	Q_O	TURNS
1-3		1-3	1-3
180	455	65	142

KOREA TOKO

Wire: 0.08mmϕUEW

L1 Bar Antenna Coil



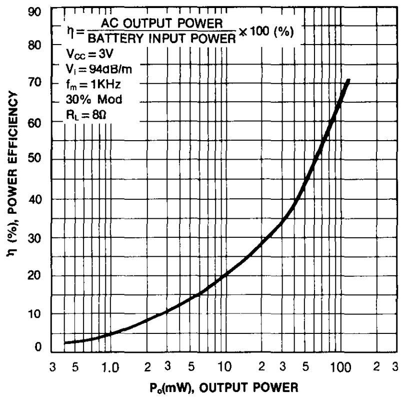
f (kHz)	L (μF)	Q_O	TURNS	
	1-2	1-2	1-2	3-4
796	625	200 Min	105	20

Core: 12mmϕ x 52mmϕ

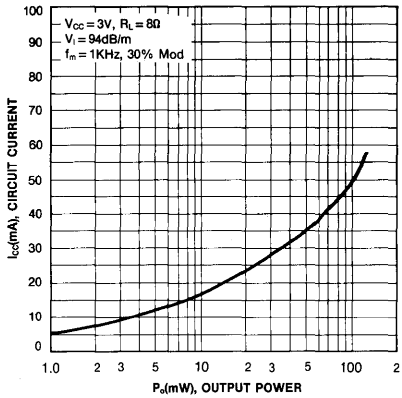
Wire: USTC-0.1mmϕ

3

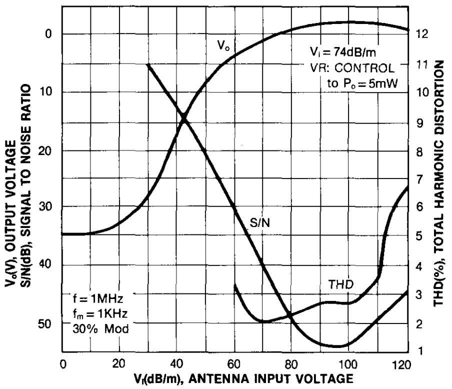
POWER EFFICIENCY-OUTPUT POWER



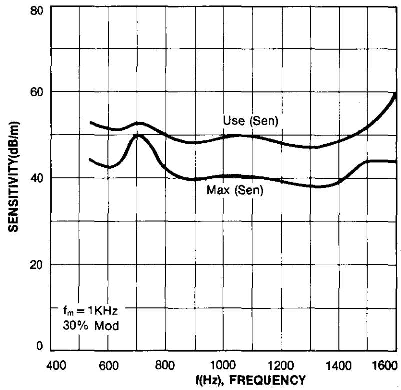
CIRCUIT CURRENT-OUTPUT POWER



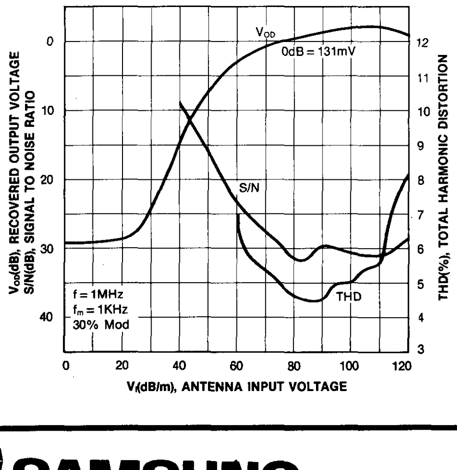
TOTAL HARMONIC DISTORTION SIGNAL TO NOISE RATIO OUTPUT VOLTAGE -ANTENNA INPUT VOLTAGE



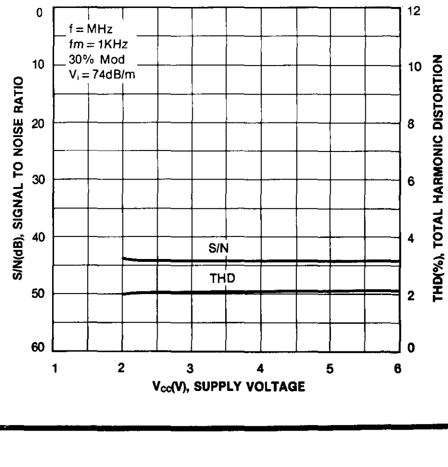
SENSITIVITY-FREQUENCY



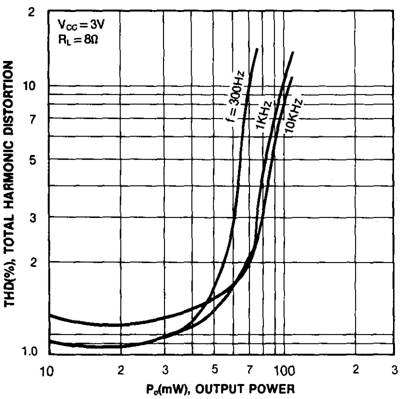
RECOVERED OUTPUT VOLTAGE SIGNAL TO NOISE RATIO TOTAL HARMONIC DISTORTION -ANTENNA INPUT VOLTAGE



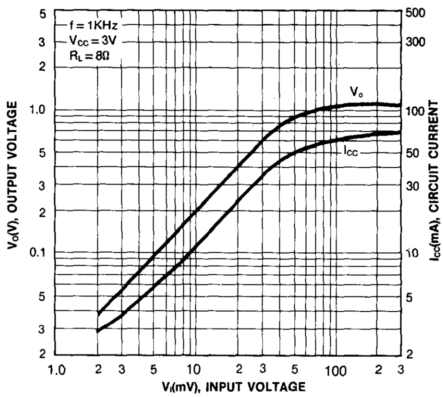
SIGNAL TO NOISE RATIO TOTAL HARMONIC DISTORTION -SUPPLY VOLTAGE



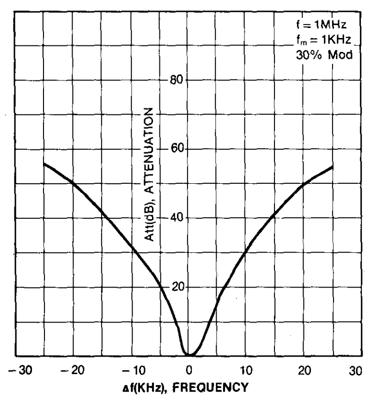
TOTAL HARMONIC DISTORTION-OUTPUT POWER



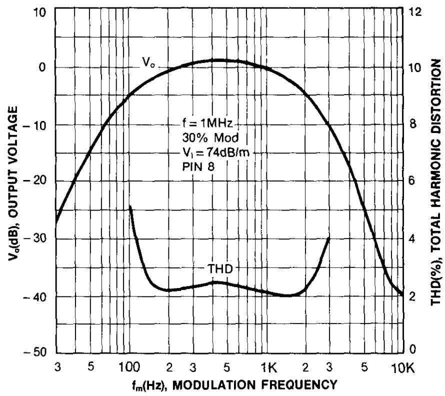
OUTPUT VOLTAGE / CIRCUIT CURRENT -INPUT VOLTAGE



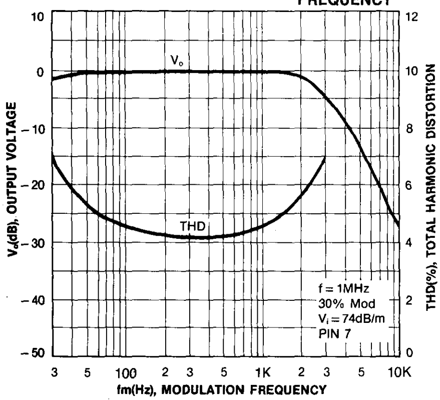
ATTENUATION-FREQUENCY



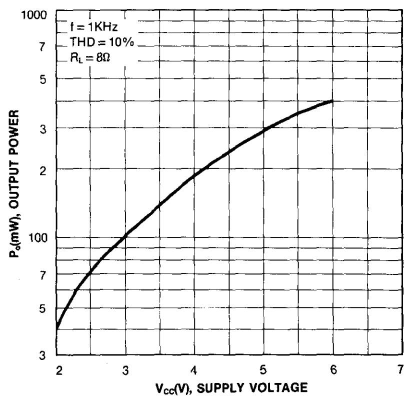
TOTAL HARMONIC DISTORTION / OUTPUT VOLTAGE -MODULATION FREQUENCY



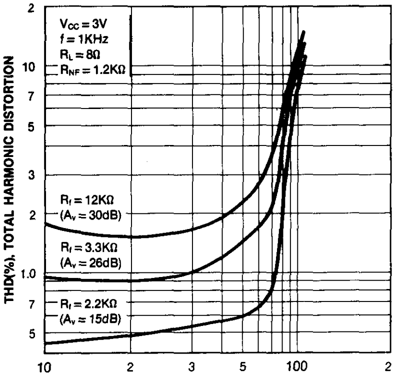
TOTAL HARMONIC DISTORTION / OUTPUT VOLTAGE -MODULATION FREQUENCY



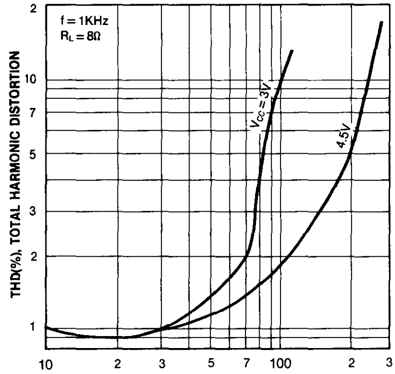
OUTPUT POWER-SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION-OUTPUT POWER

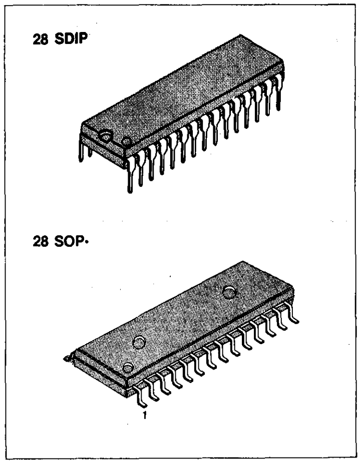


TOTAL HARMONIC DISTORTION-OUTPUT POWER



AM/FM ONE-CHIP RADIO

The KA22426 is a monolithic integrated circuit designed for radio-cassette tape recorders, clock radios and headphone radios.



FUNCTIONS

- AM/FM RF AMP
- Local OSC
- AM AGC Control
- FM AFC Control
- Audio Power AMP
- Tuning Indicator
- DC Volume
- AM/FM IF AMP
- FM Quadrature DET
- AM DET

FEATURES

- **Built-in AM/FM Switching Circuit**
- **Wide operating supply voltage: V_{CC} = 2 ~ 8.5 V**
- **Low current consumption (V_{CC} = 3V)**
  FM: I_{CC} = 5.3mA(typ)
  AM: I_{CC} = 3.4mA(typ)
- **High Power Audio Amplifier: 0.5W(typ) at V_{CC} = 6V, RL = 8Ω, THD = 10%**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22426	28 DIP	−20 ~ +70°C
KA22426P	28 SOP	−20 ~ +70°C

BLOCK DIAGRAM

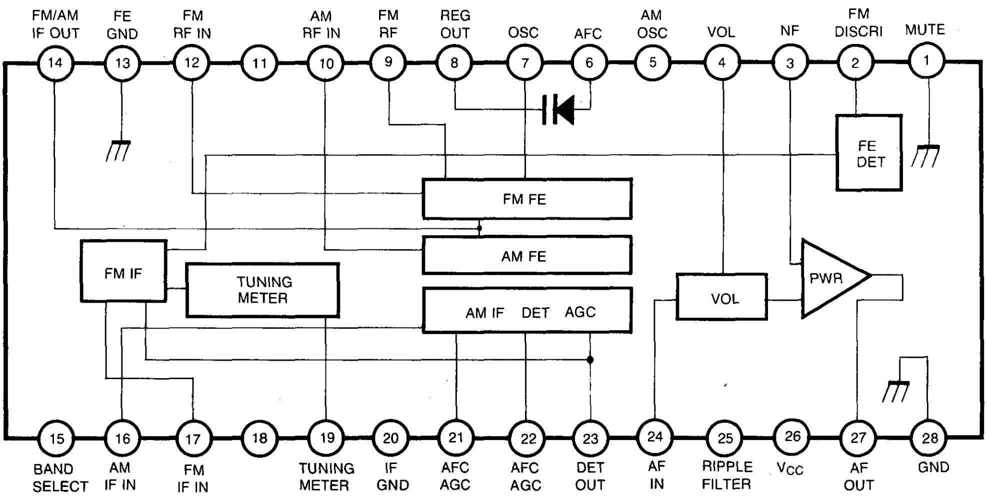


Fig. 1

3

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	9	V
Power Dissipation	P_d	1000	mW
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 6V, Ta = 25°C, FM; △f = 22.5KHz, fm = 1KHz, AM; 30% Mod unless otherwise specified)

	Characteristic	Symbol	Test Condition	SW Condition 1	2	3	4	5	6	Test point	Min	Typ	Max	Unit
FM	Quiescent Circuit Current	$I_{CC}(1)$	$V_i = 0$	A	B	A	A	B	A	Ⓐ		7.0	14.0	mA
	F/E Voltage Gain	$A_V(1)$	$V_i(1) = 40dB\mu$, f = 100MHz, △f = 0	A	B	A	A	B	A	$V_O(1)$	32	39	46	dB
	Detect Output Gain	$V_O(1)$	$V_i(3) = 90dB\mu$, f = 10.7 MHz	A	—	—	A	B	A	$V_O(3)$	−26	−20	−14	dBm
	IF-3dB Sensitivity	Vi (lim)	$V_O(V_i(3) = 90dB\mu) - 3dB$, f = 10.7 MHz	A	—	—	A	B	A	$V_O(3)$		24	32	dBμ
	Total Harmonic Distortion	THD (1)	$V_i(3) = 90dB\mu$, f = 10.7MHz (△f = 75KHz)	A	—	—	A	B	A	$V_O(3)$		0.3	2.0	%
	Meter Drive Current	IL(1)	$V_i(3) = 60dB\mu$, f = 10.7MHz	A	—	—	A	B	A	IM	1.8	3.5	7.0	mA
AM	Quiescent Circuit Current	$I_{CC}(2)$	$V_i = 0$	A	B	A	A	A	A	Ⓐ		3.5	10.0	mA
	F/E Voltage Gain	$A_V(2)$	$V_i(2) = 60dB\mu$, f = 1660KHz, m = 0%	A	A	A	A	A	A	$V_O(2)$	15	22	29	dB
	IF Voltage Gain	$A_V(3)$	$V_O(3) = -34dBm$, f = 455KHz	A	A	—	A	A	A	$V_O(3)$	14	20	27	dBμ
	Detect Output Voltage	$V_O(2)$	$V_i = (3) = 85dB\mu$, f = 455KHz	A	A	—	A	A	A	$V_O(3)$	−26	−20	−14	dBm
	Total Harmonic Distortion	THD(2)	$V_i(2) = 95dB\mu$, f = 1660KHz, $V_{CC} = 7.8V$	A	A	B	B	A	A	$V_O(3)$		0.6	2.0	%
	Meter Drive Current	IL(2)	$V_i(3) = 85dB\mu$, f = 455KHz	A	A	—	A	A	A	IM	1.3	3.0	7.0	mA
AF	Closed Loop Voltage Gain	$A_V(4)$	$V_O(4) = 0dBm$, f = 1KHz	A	—	—	—	—	B	$V_O(4)$	27	31.5	36	dB
	Total Harmonic Distortion	THD(3)	$P_O = 50mW$, f = 1KHz	A	—	—	—	—	B	$V_O(4)$		0.3	2.5	%
	Output Power	P_O	$R_L = 8\Omega$, THD = 10%, f = 1KHz	A	—	—	—	—	B	$V_O(4)$	0.4	0.5		W

TEST CIRCUIT

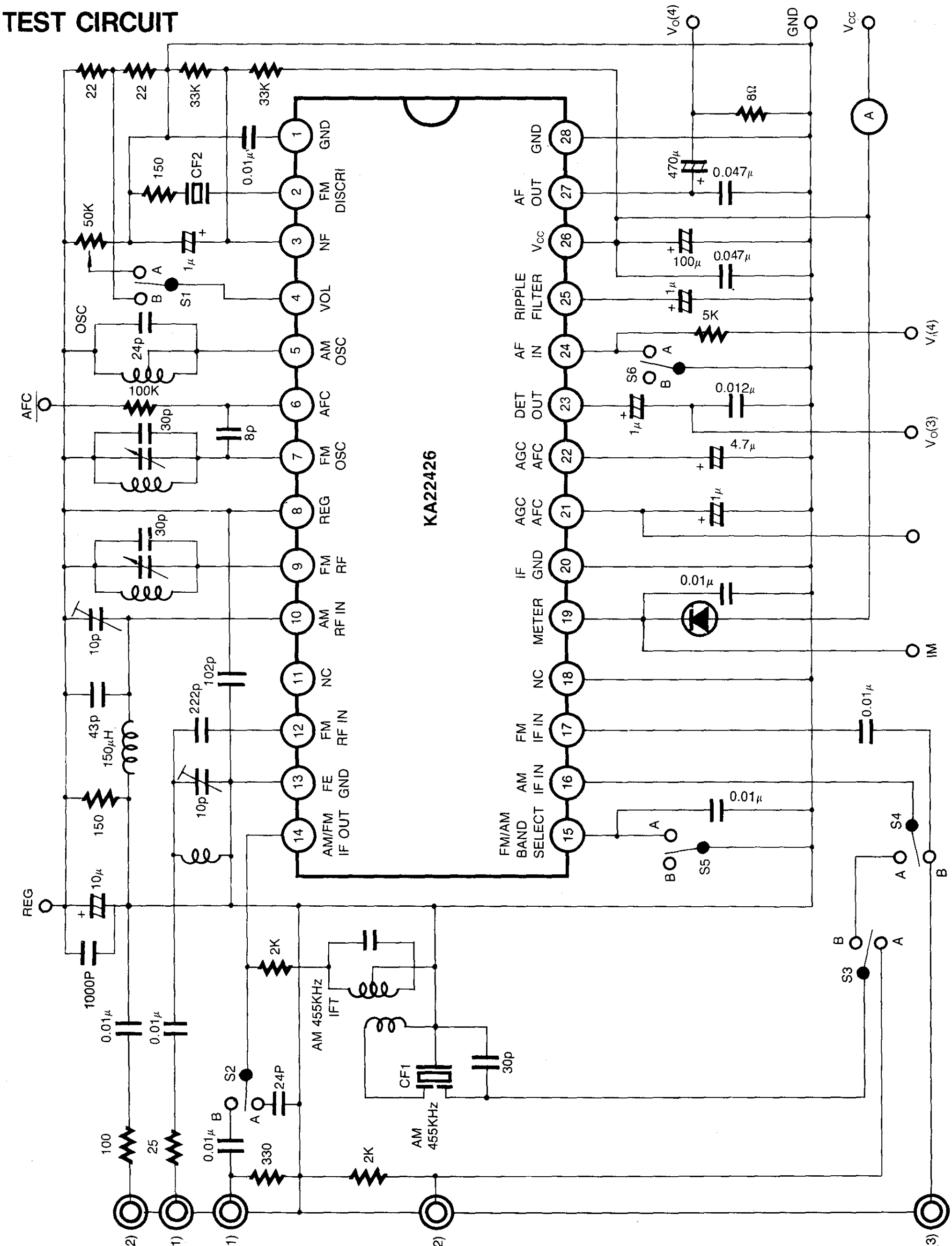


Fig. 2

APPLICATION CIRCUIT

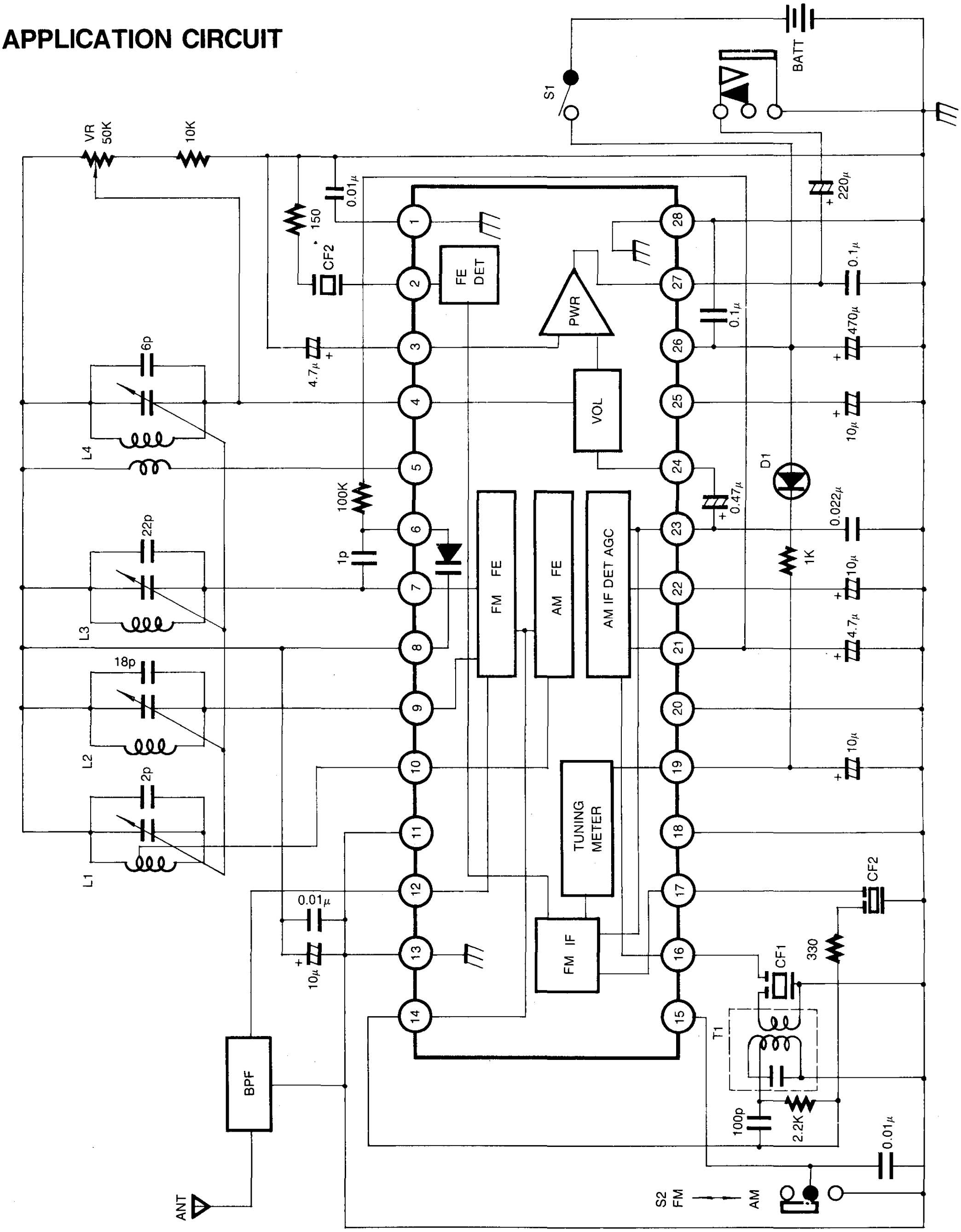
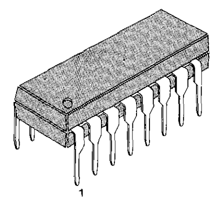


Fig. 3

AM/FM 1-CHIP RADIO

KA22427 is a monolithic integrated circuit designed for the portable AM/FM radio or AM/FM clock radios.

16 DIP



FUNCTIONS

- AM RF & MIX
- AM AGC
- AM/FM DET
- Regulator
- AM Local OSC
- AM/FM IF AMP
- Audio Power AMP
- FM AFC Control

FEATURE

- **Portable AM/FM 1-chip radio**
- **Wide operating supply voltage range; $V_{CC}=3\sim12V$ (Approximately) (Depending on the internal regulator tolerance)**
- **Recommended operating supply voltage; $V_{CC}=4.5\sim9V$**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22427	16 DIP	$-20\sim+70°C$

R_L \ V_{CC}	4.5V	6.0V	7.5V	9.0V	Line Operated
8Ω	O	O	O	X	X
16Ω	O	O	O	O	X
45Ω	O	O	O	O	O

- On using AC line as an internal shunt regulator mode, it is possible to use low cost application without a transformer (approximately 42mA)
- IF AMP gain is determined by DC voltage appeared at IC Pin 16.
- Power output: $P_o=0.28W$ (Min.) at THD = 10% ($V_{CC}=5.5V/8Ω$).

BLOCK DIAGRAM

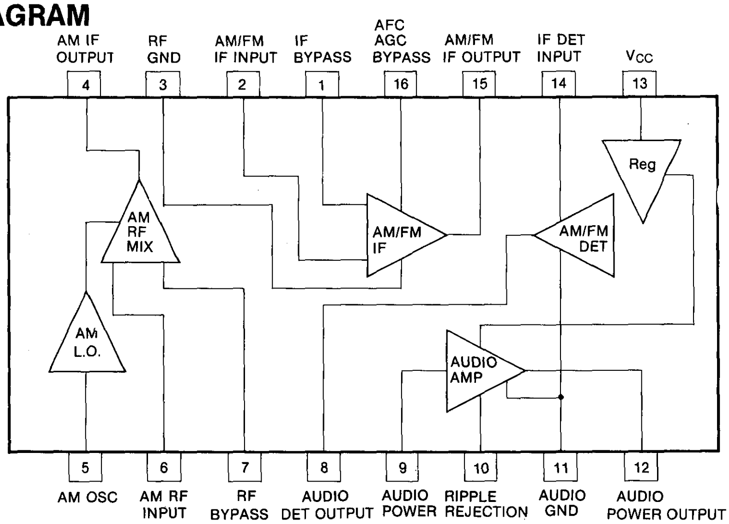


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	13	V
Power Dissipation (Note) Ta≤65°C	P_d	600	mW
Supply Current	I_{CC}	44	mA
Thermal Resistance	R_{j-a}	100	°C/W
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

3

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 5.5V, f_m = 1KHz, AM: f = 1MHz, 30% Mod, FM: f = 10.7MHz
△f = 22.5KHz, Unless otherwise specified)

	Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
FM	Quiescent Circuit Current	I_{CC}	SW: FM, V_{CC} = 3V	10	15	20	mA
			SW: FM, V_{CC} = 9V	13	20	26	
	Pin 16 Terminal Voltage	V_{16} (FM)	SW: FM, V_{CC} = 9V, V_i = 0	2.0	2.4	3.1	V
	Input Limiting Sensitivity	V_i (lim)	SW: FM, −3dB V_{16} = 2.4V, V_R Min		57		dBμ
AM	Internal Regulated Vtg.	V_{CC}	SW: AM, I_{CC} = 42mA	12	13.2	14.0	V
	Pin 16 Voltage	V_{16} (AM)	SW: AM, V_{CC} = 9V, V_i = 0	1.4		1.9	V
	Maximum Sensitivity	Max (Sen)	SW: AM, V_{CC} = 12V V_i = 37dBμ, R_L = 45Ω	1.5	3.0		V
	Signal to Noise Ratio	S/N	V_i = 37.5dBμ, R_L = 8Ω P_o = 50mW	15	20		dB
PWR AMP	Output Power	P_o	f = 1KHz, THD = 10% V_R Min, R_L = 8Ω	0.28			W
	Total Harmonic Distortion	THD	I_{CC} = 42mA, R_L = 45Ω f = 1KHz, V_o = 2V V_R Min		0.5	4.0	%
	Voltage gain	A_v	f = 1KHz, R_L = 8Ω P_o = 50mW		41		dB

TEST CIRCUIT

1. CIRCUIT

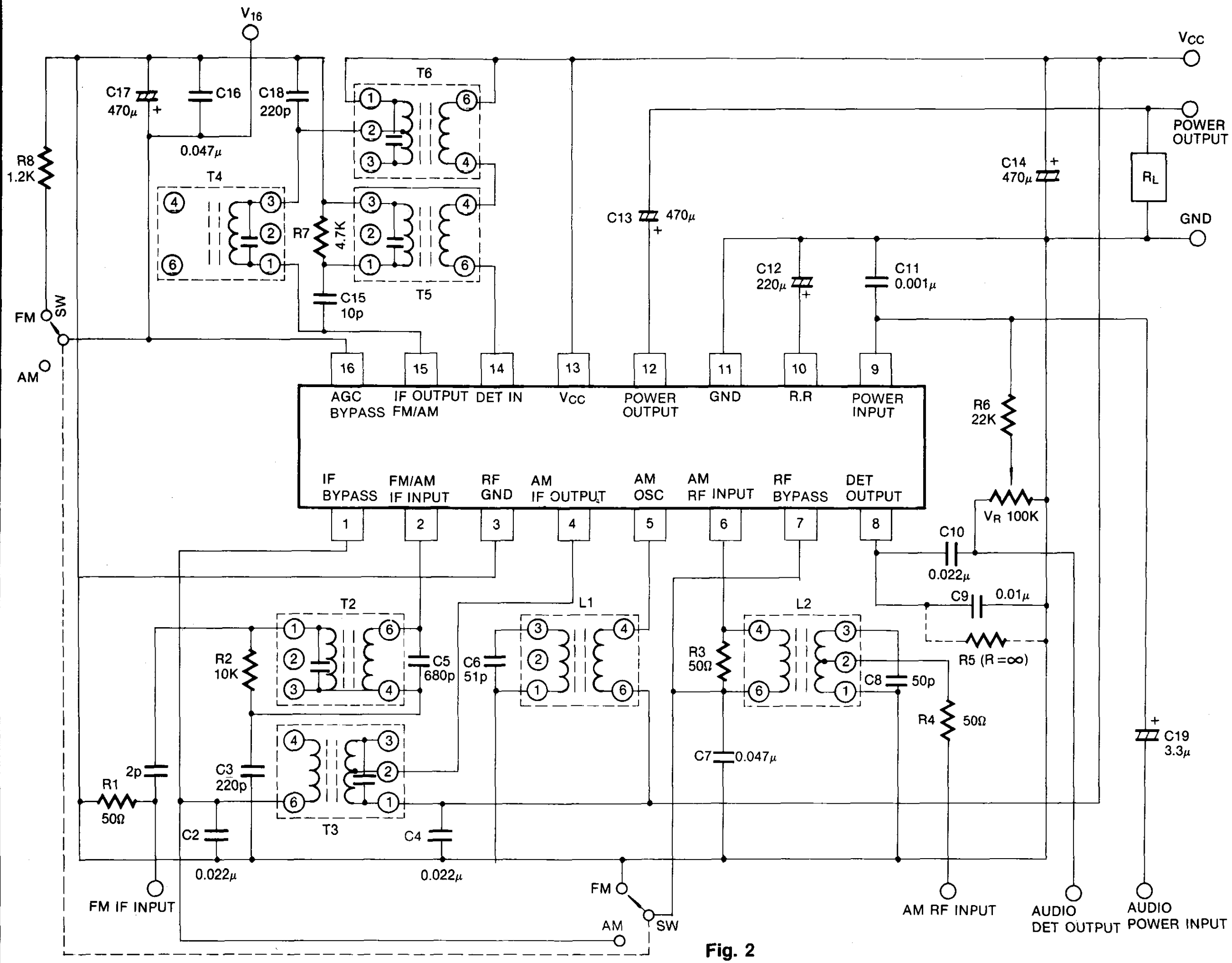


Fig. 2

EXTERNAL PARTS TABLE

Parts Number	Purpose	Typical	Influence	
			Smaller Than Typ	Greater Than Typ
R5	AM Gain Control	47KΩ (33K~∞)	Low AM Gain	AGC Distortion Increase, High Gain
R7	FM Detector Damper	4.7KΩ	Low Detector Output, Stable IF Gain, Low FM Gain	Sharp IF AMP Curve
R8	FM Gain Adjust	470	Low FM Gain	High Gain, but Noise Increases
C2	IF Bypass	0.022μF	Should Not Be Less Than 0.005μF	High IF Gain, S/N Ratio Degrade
C4	IF Filter	0.022μF	Removal May Cause IF Oscillation	No Influence
C7	AM Bypass	0.047μF	Low Gain	Using over 1μF Will Cause FM Distortion at Small Signal
C9	Detector Filter	0.01μF	Unstable IF AMP Oscillation	Poor FM Frequency Response
C10	Audio Coupling	0.022μF	Lower Sensitivity, Poor Low Frequency Response	Bass Boost Affects De-emphasis Curve
C11	Audio Input High-Cut	0.001μF	Audio Oscillation	Poor Response
C12	Ripple Filter	220μF	Poor Frequency Response & Low Gain	Improves AC Hum
C13	Audio Output Coupling	470μF	Poor Low Frequency Response	Can Achieve Optimum Output Power
C14	Power Line Filter	470μF	Poor AC Hum	Improves AC Hum
C15	FM Detector Phase-Shift	10pF	Narrow IF Bandwidth	Wide IF Bandwidth
C16	High Freq. (IF) Bypass	0.047μF	Removal Will Cause FM Oscillation	No Influence
C17	AM AGC Time Constant and High Frequency (IF) Bypass	0.047μF	Not Recommend to Charge	

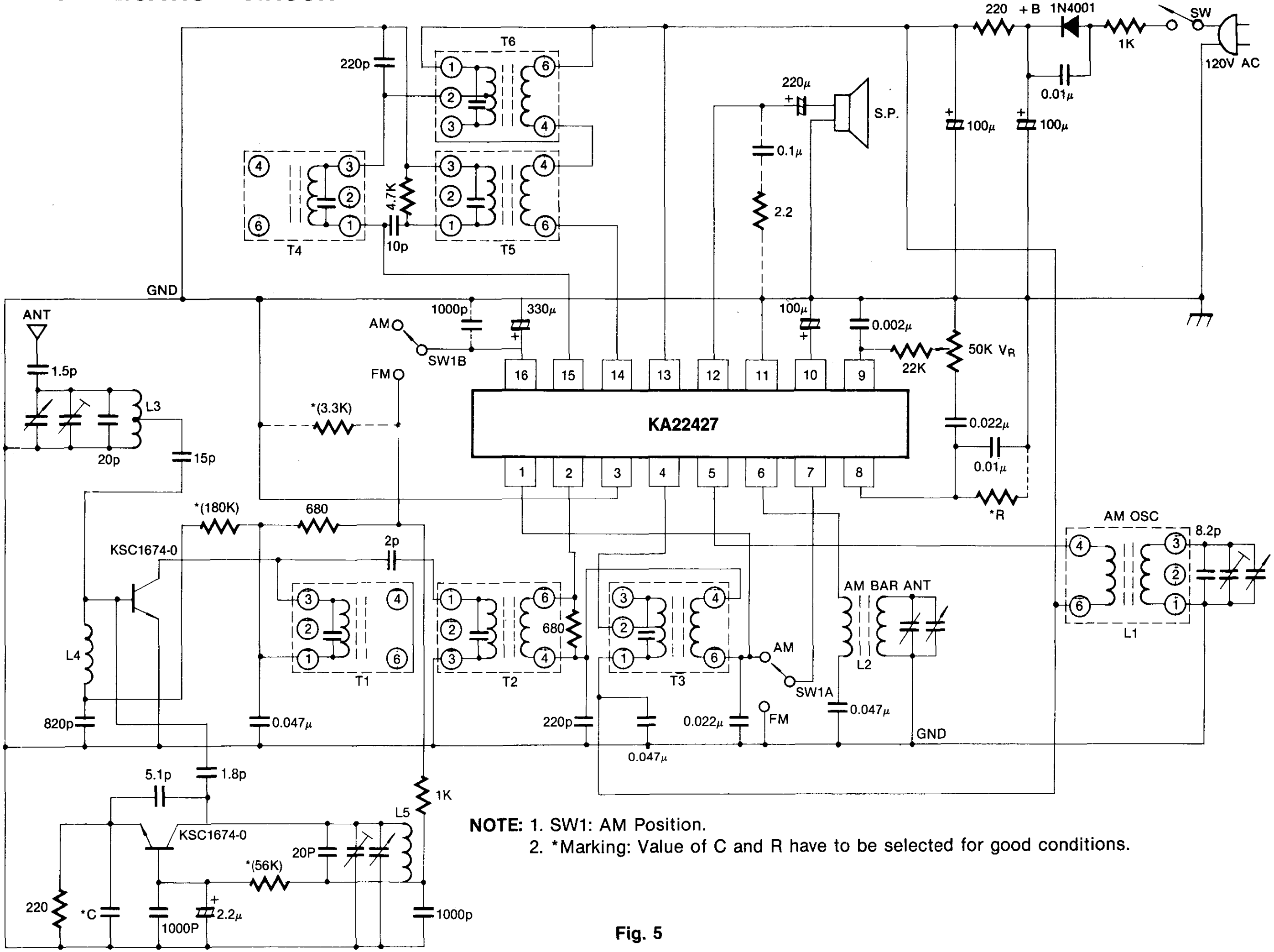
APPLICATION NOTE (Pin 16 DC Voltage)

1. IF Gain Grouping Table
   (1) Test Condition: V_{CC} = 9V (Pin 13).
   Pin 8 resistance (AM) = 47KΩ.
   Pin 16 resistance (FM) = 1.2KΩ.
   (2) Grouping Table

V16 (AM) / V16 (FM)	1.4 – 1.7V	1.7 – 1.9V
2.6 – 3.0V	C1	C2

2. IF gain is determined by DC voltage appeared at IC Pin 16.
   The DC voltage at Pin 16 to the following values:
   AM = 1.4 ~ 1.65V (DC)
   FM = 1.9 ~ 2.10V (DC)
   AM gain can be adjusted by the loading resistor value of Pin 8 (AM) from 33KΩ to infinity.
   FM gain can be adjusted by the loading resistor vale of Pin 16 (FM) from 390Ω to 680Ω.
   Recommended resistance (Pin 8, Pin 16).
   Pin 8 (AM) = 47KΩ
   Pin 16 (FM) = 470Ω

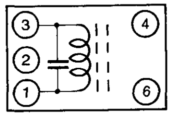
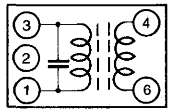
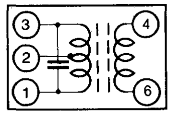
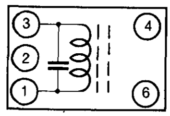
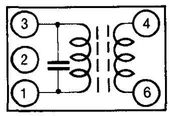
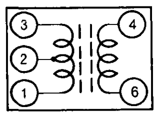
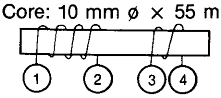
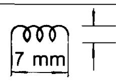
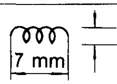
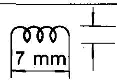
APPLICATION CIRCUIT 1



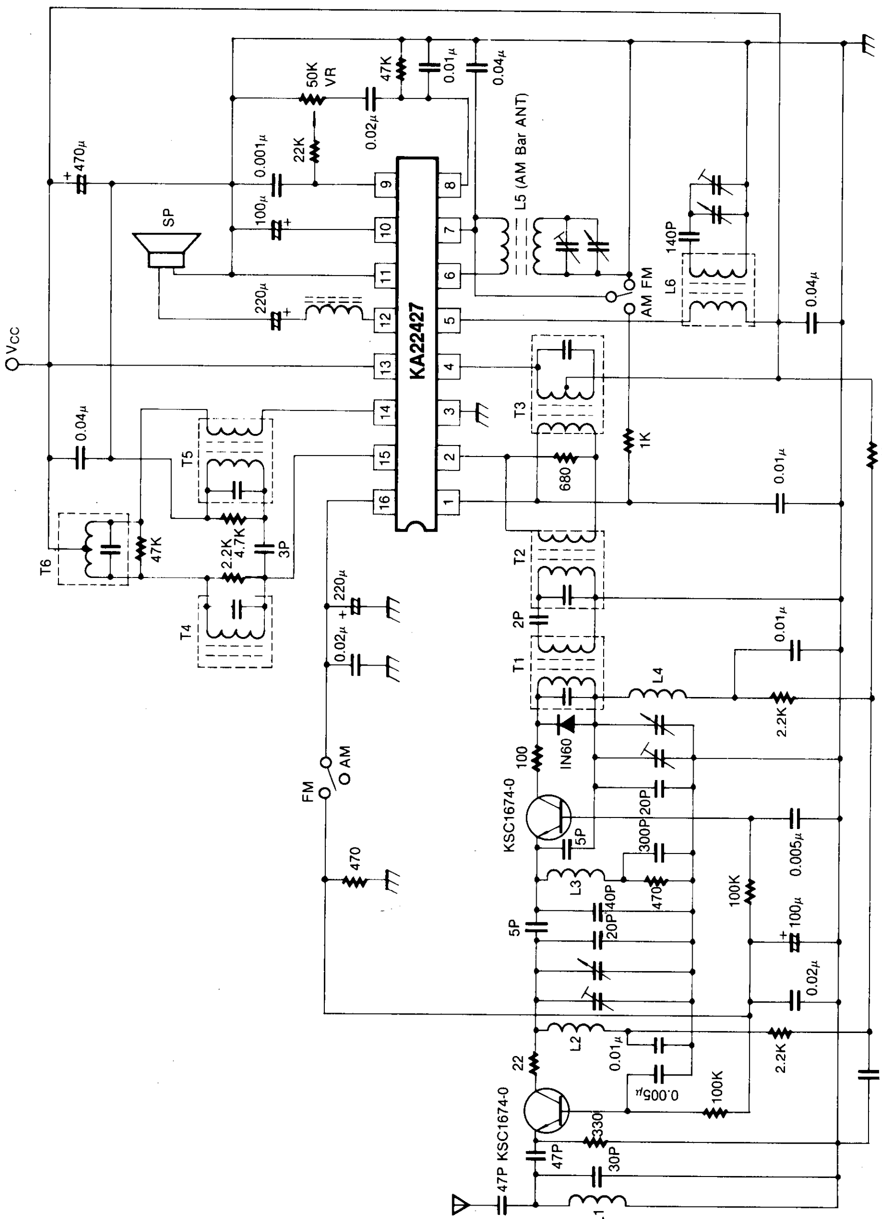
NOTE: 1. SW1: AM Position.
2. *Marking: Value of C and R have to be selected for good conditions.

Fig. 5

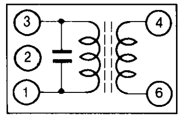
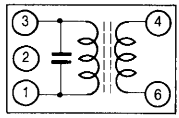
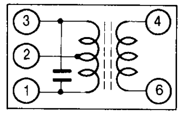
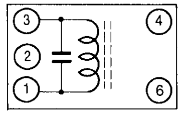
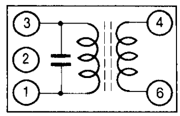
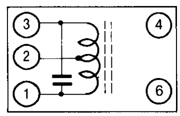
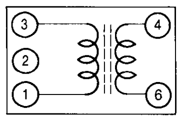
COIL SPECIFICATION 1

Coil No.	f	Q_o	Turns		C_o	Connections
T1	10.7MHz	120	1 – 3	8T	150pF	
T2	10.7MHz	70 min	1 – 3 4 – 6	11T 2T	75 ± 5pF	
T3 (T6)	455KHz	80 min	1 – 2 2 – 3 4 – 6	91T 55T 6T	180 ± 5pF	
T4	10.7MHz	45 min	1 – 3	11T	82 ± 3pF	
T5	10.7MHz	25 min	1 – 3 4 – 6	7T 7T	180pF	
L1	AM Local Oscillator	90 min	1 – 3 4 – 6	86T 7T		
L2	AM ANT	200	1 – 2 (L = 560μH) 3 – 4	138T 9T		Core: 10 mm ø × 55 mm  V.C GND Pin 6 GND
L3	FM ANT		0.8 mm ø UEW TAP	5T 0.5T		 5 mm, 7 mm
L4	Trap		0.32 mm ø UEW	10T		 5 mm, 7 mm
L5	FM Oscillator		0.8 mm ø UEW	4T	—	 5 mm, 7 mm

APPLICATION CIRCUIT 2



COIL SPECIFICATION 2

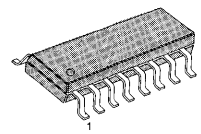
Coil No.	f	Q_0	Turns		C.L.	Connections
T1	10.7MHz	90	1 – 3	11	82pF	
			4 – 6	3		
T2	10.7MHz	60	1 – 3	5	390pF	
			4 – 6	2		
T3	455KHz	100	1 – 2	127	180pF	
			2 – 3	28		
			4 – 6	10		
T4	10.7MHz	45 (Min)	1 – 3	11	82pF	
T5	10.7MHz	25 (Min)	1 – 3	7	180pF	
			4 – 6	7		
T6	455KHz	100	1 – 2	50	390pF	
			2 – 3	50		
L6	796KHz	100	1 – 3	100	360μH	
			4 – 6	10		

FM ONE-CHIP RADIO

The KA22429 is an integrated circuit for FM portable radios, stereo as well as mono, where a minimum periphery is important in terms of small dimensions and low cost. It is fully compatible for applications using the low voltage micro tuning system IC (MTS). The IC has a frequency of 76KHz, locked loop (FLL) system with an intermediate frequency.

The selectivity is obtained by active RC filters. The only function to be tuned is the resonant frequency of the oscillator. Interstation noise as well as noise from receiving weak signals is reduced by a correlation mute system.

16 SOP



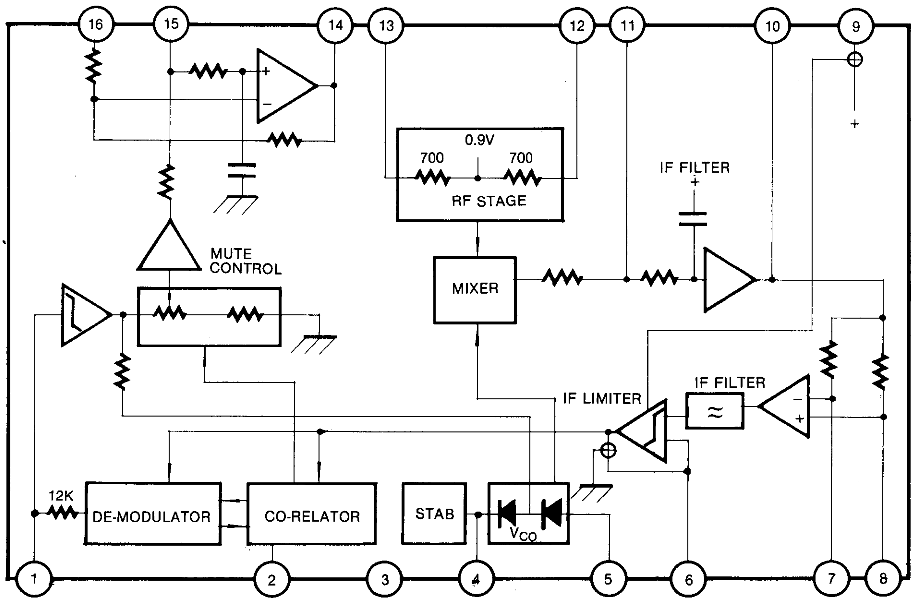
FEATURES

- **Rf input stage**
- **Local oscillator**
- **Frequency detector**
- **MTS compatible**
- **Internal reference circuit**
- **LF amplifier for mono earphone amplifier or mux filter**
- **Field strength dependent channel separation control facility**
- **Mixer**
- **IF amplifier/limiter**
- **Mute circuit**
- **Loop amplifier**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22429D	16 SOP	−10 ~ +70°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	7	V
Oscillator Voltage	V5	−0.5 ~ +0.5	V
Operating Temperature	T_{opr}	−10 ~ +70	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C
Thermal Resistance	θja	300	K/W

DC ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 3V, unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	1.8	3.0	6	V
Quiescent Circuit Current	I_{CC}		6.3		mV
Oscillator Current	I_5		250		μA
Voltage at Pin 13	V_{13}		0.9		V
Output Voltage	V_{14}		1.3		V

3

AC ELECTRICAL CHARACTERISTICS

MONO OPERATION

(f_{RF} = 96MHz, f_m = 1KHz, $\triangle f = \pm 22.5$KHz, EMF = 300μV
(EMF Voltage at Source Impedance of 75ohm), Ta = 25°C, V_{CC} = 3V unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Sensitivity	EMF_1	−3dB: Mute Disable		4.0		μV
	EMF_2	−3dB: Mute Enable		5.0		μV
	EMF_3	S/N = 26dB: Mute Enable		7.0		μV
Signal Handling	V_{OM}	THD < 10%, $\triangle f = \pm 75$KHz		200		mV
Signal to Noise Ratio	S/N_1			60		dB
Total Harmonic Distortion	THD_1	$\triangle f = \pm 22.5$KHz		0.7		%
	THD_2	$\triangle f = \pm 75$KHz		2.3		%
Am Rejection Ratio	AMR	AM: fm = 1KHz, m = 80% FM: fm = 1KHz, $\triangle f = \pm 75$KHz		50		dB
Ripple Rejection	RR	$\triangle V_{CC}$ = 100mV, f = 1KHz		30		dB
Oscillator Voltage	V_{OSC}			250		mV
Variation of Oscillator Frequency	$f_{osc}/\triangle V_{CC}$	$\triangle V_{CC}$ = 1V		5		KHz/V
	$f_{OSC}/\triangle T$	With Temperature		0.2		KHz/°C
Selectivity	S + 300	Without Modulation ; Test Circuit Fig. 3		30		dB
	S − 300			46		dB
AFC Range	$\pm \triangle f_{RF1}$			160		KHz
Mute Range	$\pm \triangle f_{RF2}$			120		KHz
Band Width	BW	$\triangle V_O$ = 3dB Pre-Emphasis t = 50μs		10		KHz
AF Output Voltage	V_{o1}			90		mV
AF Output Current	I_O (DC)	Max DC LOAD	−100		+100	μA
	I_O (AC)	THD = 10%, PEAK VALUE		3		mA

STEREO OPERATING

(f_{RF} = 96MHz Modulated with Pilot $\triangle f = \pm 6.75$KHz
and AF Signal $\triangle f = \pm 22.5$KHz; fm = 1KHz; EMF = 1mV (EMF Voltage at a Source Impedance of 75ohm)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Sensitivity	EMF_4	S/N = 46dB		300		μV
Signal to Noise Ratio	S/N_2			53		dB
Channel Separation	Sep			20		dB
Pilot Voltage of Pin 14	V_{p14}			13.5		mV
AF Output Voltage	V_{o2}			80		mV
Selectivity	S + 300	Without Modulation ; Test Circuit Fig. 3		22		dB
	S − 300			40		dB

TEST CIRCUIT

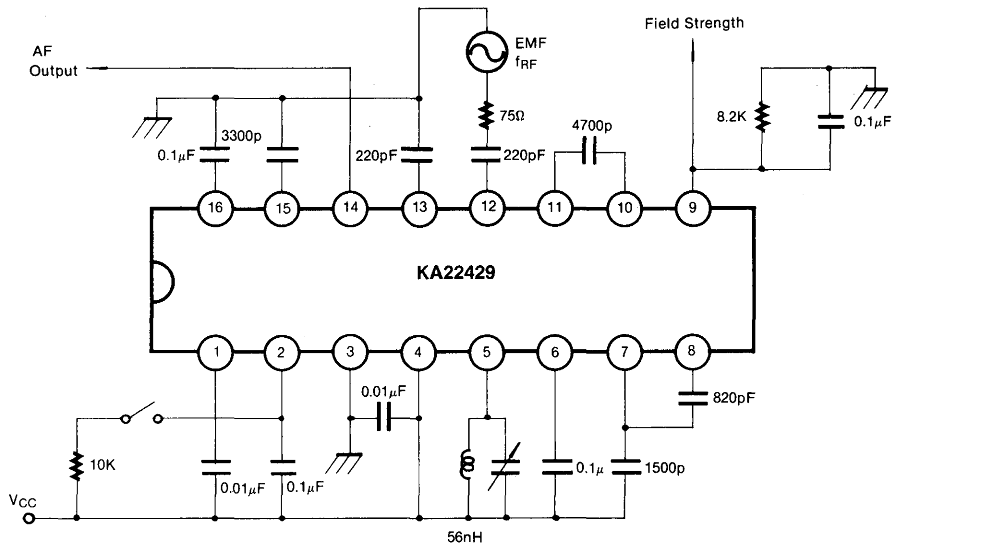


Fig. 1 Test Circuit for Mono Operation

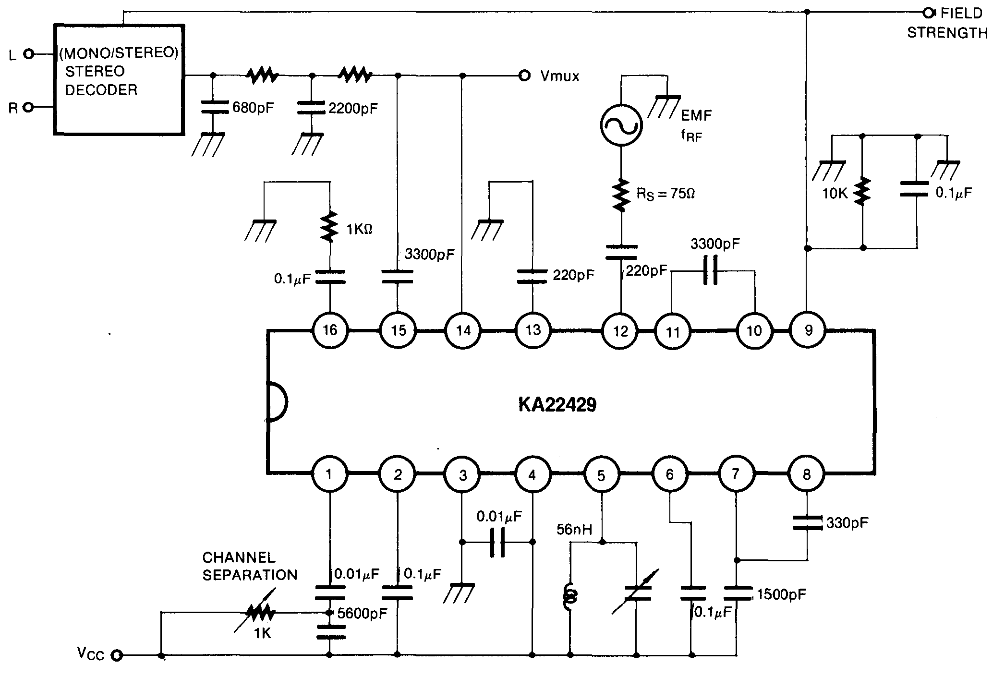


Fig. 2 Test Circuit for Stereo Operation

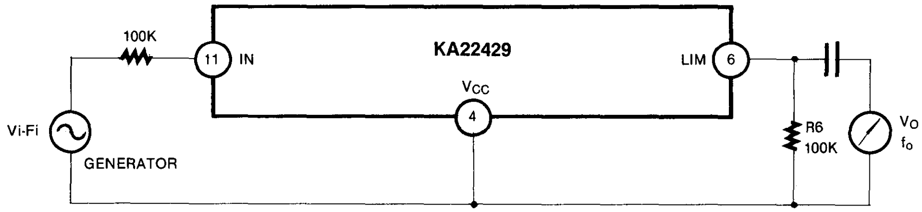


Fig. 3 Test Circuit

NOTES:

Setup with circuitry as Fig. 1 as Fig. 2
C_6 (0.1μF) deleted and replaced by $R_6 = 100$Kohm; Vi = 30mV: fi = 76KHz output selective voltmeter $R_1 \geq 1M\Omega$; $Ci \leq 8pF$; fo = fi

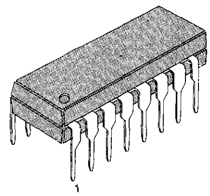
SELECTIVITY

$$S_{+300} = 20\text{Log}\frac{V_{o1}/(300KHz - fi)}{Vo/fi} \qquad S_{-300} = 20\text{Log}\frac{Vol/(300KHz + fi)}{Vo/fi}$$

AM/FM IF SYSTEM

The KA2243 is a monolithic integrated circuit developed for radio cassette tape recorders which include AM/FM IF amplifier and detector.

16 DIP



FUNCTIONS

- AM Section:
  IF amplifier with AGC detector.
  Signal meter driver circuit.
  Voltage regulator for RF external circuit.
- FM Section:
  IF amplifier.
  Quadrature detector.
  Post amplifier.
  Signal meter driver circuit.

FEATURES

- **Suitable for radio cassettes and home stereos.**
- **Wide operating supply voltage range. (3.0V ~ 14V).**
- **Low quiescent circuit current.**
- **AM section.**
  Simplified input circuit IFT (Ceramic filter type).
  RF AGC available.
- **FM section.**
  High limiting sensitivity (33dBμ, Typ).
  Low residual noise (45dB at V_i = −10dBμ).
  Small side peak of detuned output voltage.

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2243	16 DIP	−20 ~ +70°C

TEST CIRCUIT

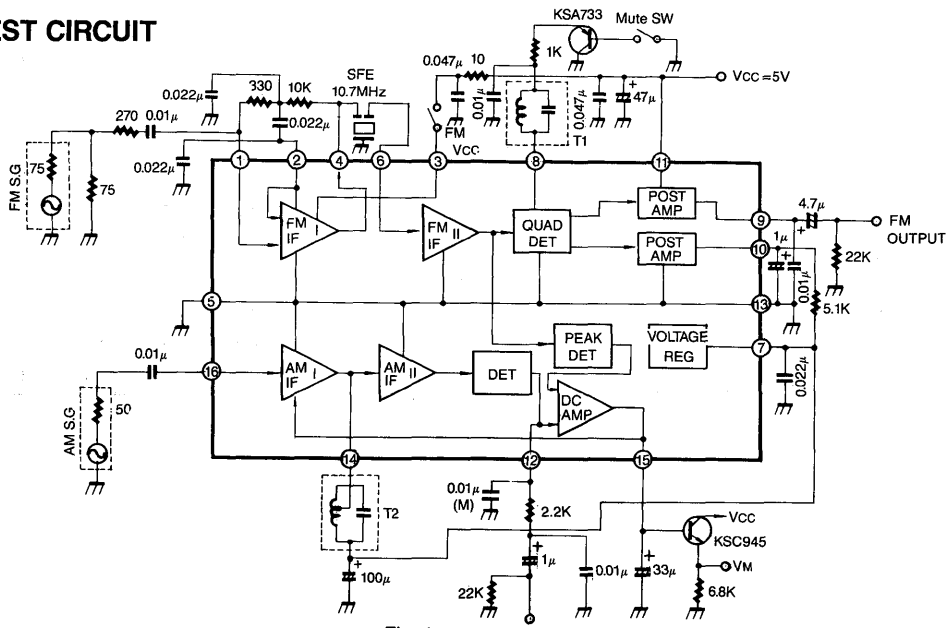


Fig. 1

3

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_d	600	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

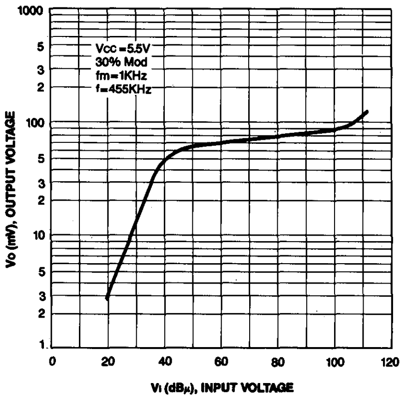
ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 5.5V, unless otherwise specified)

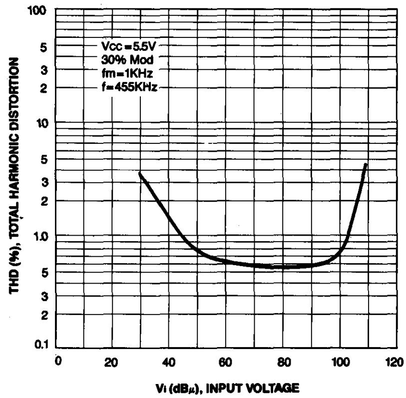
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
FM Section (f = 10.7MHz, fm = 1KHz, Δf = ±75KHz)						
Quiescent Circuit Current	I_{CC}	V_i = 0	7	11	16.5	mA
Input Limiting Sensitivity	V_i (lim)	V_O (V_i =100dBμ)−3dB		33	38	dBμ
Detector Output Voltage	V_O	V_i =100dBμ	180	245	310	mV
Total Harmonic Distortion	THD	V_i =100dBμ		0.3	1.0	%
AM Rejection Ratio	AMR	V_i =100dBμ	50	60		dB
Signal to Noise Ratio	S/N	V_i =100dBμ	72	83		dB
Signal Meter Output	V_M	V_i =100dBμ	1.05	1.5	2.05	V
Residual Noise	V_N	V_O (AF) (V_i =100dBμ) :V_O (AF) (V_i = −10dBμ)		45		dB
Muting Attenuation	M (att)	V_i =37dBμ,Mute SW on		35		dB
AM Section (f=455KHz, fm=1KHz, 30% Mod)						
Quiescent Circuit Current	I_{CC}	V_i =0		8		mA
Maximum Sensitivity	V_i (sen)	V_O (AF)=10mV		29		dBμ
Detector Output Voltage	V_O	V_i =74dBμ	45	65	85	mV
Total Harmonic Distortion	THD	V_i =74dBμ		0.3	2.0	%
		V_i =100dBμ		0.7	3.5	%
Signal to Noise Ratio	S/N	V_i =74dBμ	45	55		dBμ
Signal Meter Output	V_M	V_i =100dBμ	1.2	1.4	1.6	V
Input Impedance (Pin 16)	R_i	Pin 16 0.8−0.9V_{DC}	1.45	2.12	2.8	KΩ

(AM Section)

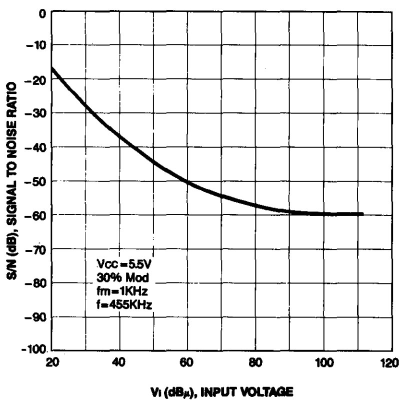
OUTPUT VOLTAGE-INPUT VOLTAGE



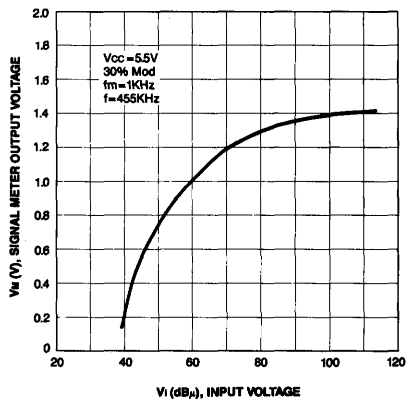
TOTAL HARMONIC DISTORTION-INPUT VOLTAGE



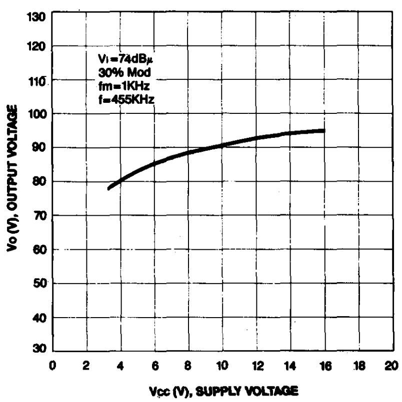
SIGNAL TO NOISE RATIO-INPUT VOLTAGE



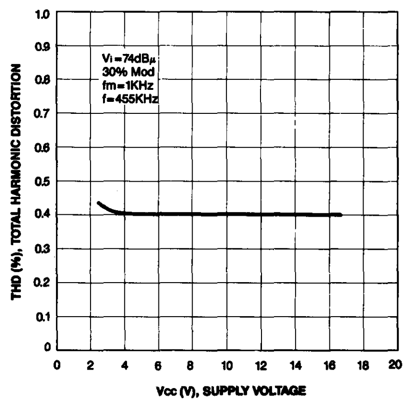
SIGNAL METER OUTPUT VOLTAGE-INPUT VOLTAGE



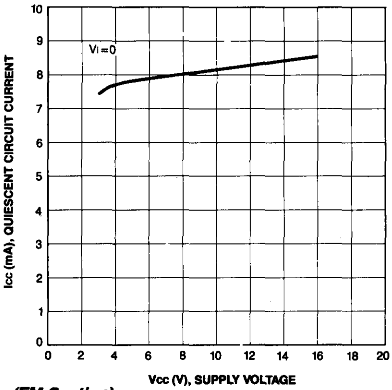
OUTPUT VOLTAGE-SUPPLY VOLTAGE



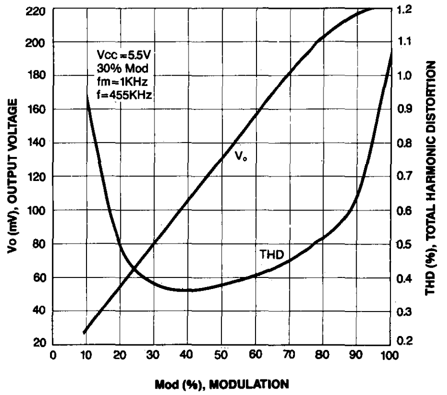
TOTAL HARMONIC DISTORTION-SUPPLY VOLTAGE



QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE

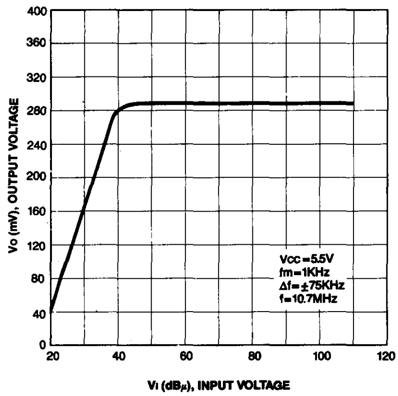


OUTPUT VOLTAGE — MODULATION
TOTAL HARMONIC DISTORTION — MODULATION

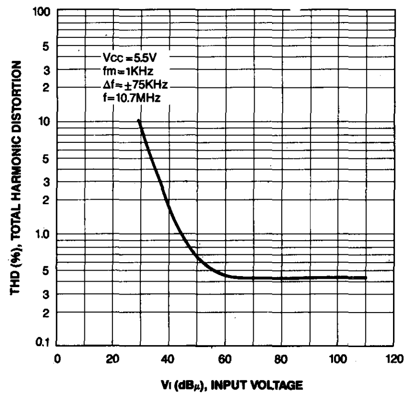


(FM Section)

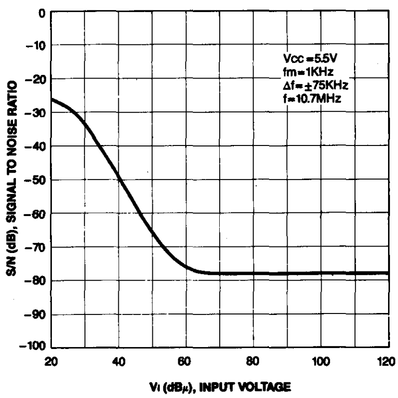
OUTPUT VOLTAGE-INPUT VOLTAGE



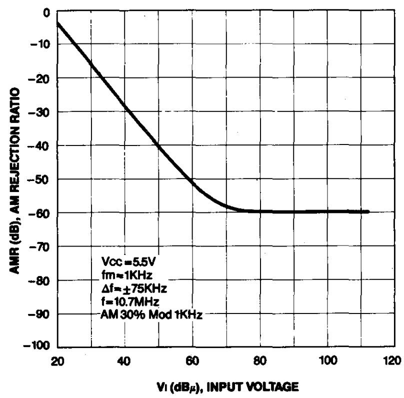
TOTAL HARMONIC DISTORTION-INPUT VOLTAGE



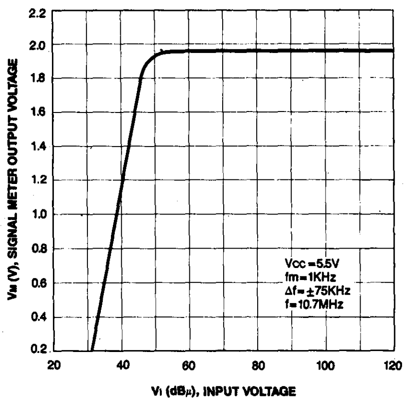
SIGNAL TO NOISE RATIO-INPUT VOLTAGE



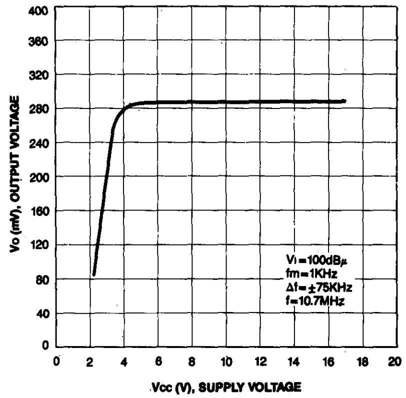
AM REJECTION RATIO-INPUT VOLTAGE



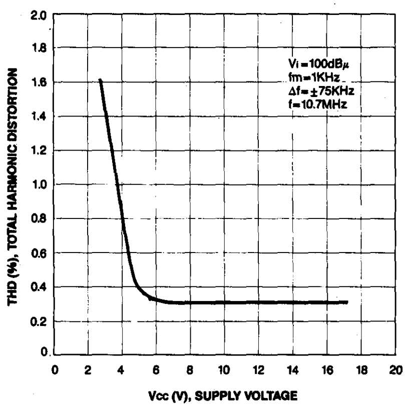
SIGNAL METER OUTPUT VOLTAGE-INPUT VOLTAGE



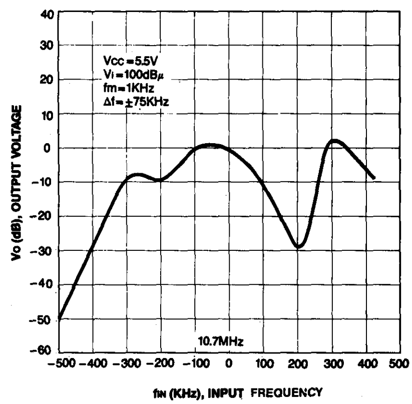
OUTPUT VOLTAGE-SUPPLY VOLTAGE



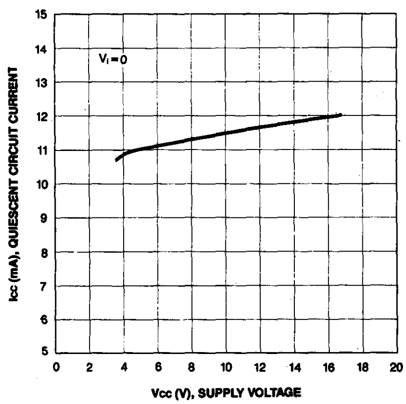
TOTAL HARMONIC DISTORTION-SUPPLY VOLTAGE



OUTPUT VOLTAGE-INPUT FREQUENCY



QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



TYPICAL APPLICATION CIRCUIT

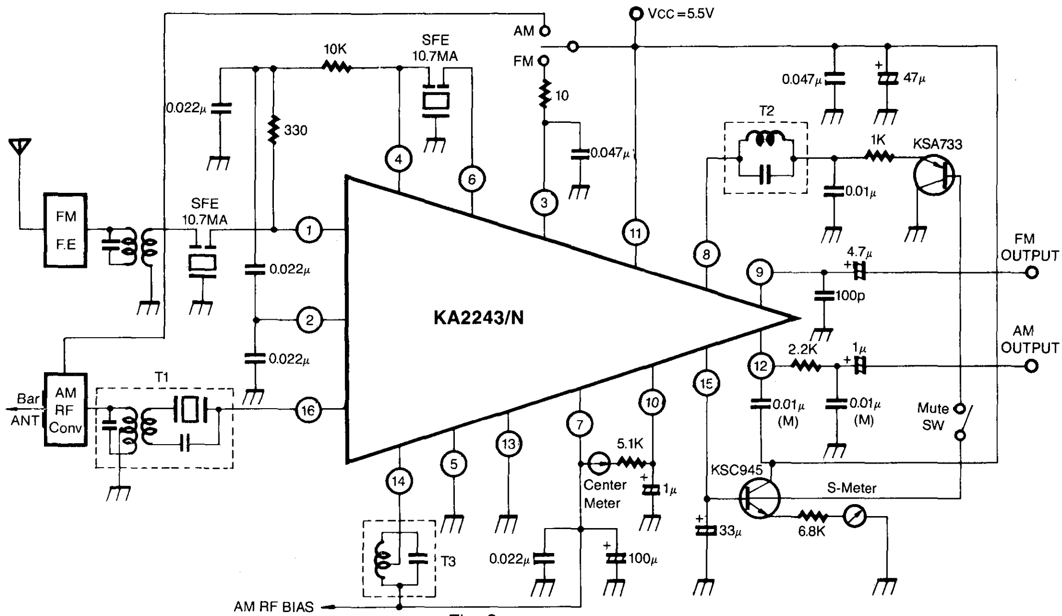
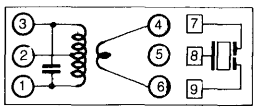


Fig. 2

COIL SPECIFICATION

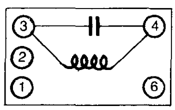
1. T1



Co (pF)	f (KHz)	Qo (%)	TURNS 4-6	TURNS 3-2	TURNS 2-1
180	455	105	6	93	55

Seoul Jupa
SJ-015-552
0.06mmφ UEW

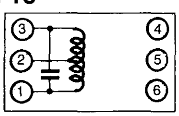
2. T2



Co (pF)	f (MHz)	Qo (%)	TURNS 3-4		
82	10.7	65	9		

Seoul Jupa
SJ-59JG-043
0.07mmφ UEW

3. T3



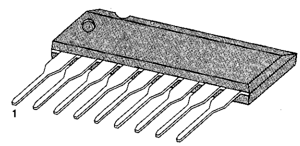
Co (pF)	f (KHz)	Qo (%)	TURNS 1-2	TURNS 2-3	
180	455	120	51	92	

Seoul Jupa
SJ-015-521
0.07mmφ UEW

FM IF SYSTEM FOR CAR RADIOS

The KA2244 is a monolithic integrated circuit consisting of FM IF amplifier, detector, muting circuit and signal meter driver. It is suitable for car radios.

9 SIP



FUNCTIONS

- 3-stage IF amplifiers.
- Peak detector.
- Muting circuit.
- Signal meter drive circuit.

FEATURES

- **Suitable for FM car radios.**
- **Wide operating supply voltage range (8V ~ 15V).**
- **High detector output voltage (V_O =500mV, Typ).**
- **Variable muting level.**
- **Muting off by Pin 4 open.**
- **Simplified single coil tuning.**
- **Low distortion (THD=0.1%; Typ).**
- **Minimum number of external parts required.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2244	9 SIP	−20 ~ +70°C

TYPICAL APPLICATION CIRCUIT

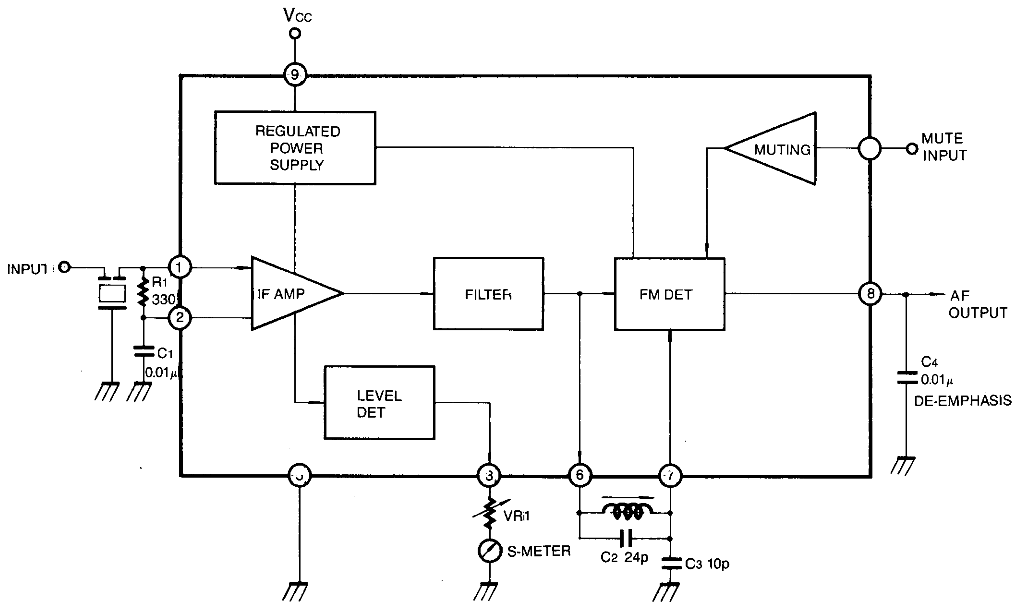


Fig. 1

3

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Input Voltage	V_i	0.7	V
Power Dissipation	*P_d	750	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

*: Derated above Ta = 25°C in the proportion of 4mW/°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =12V, f=10.7MHz, fm=400Hz, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current		I_{CC}	V_i=0	10	14	18	mA
Input Limiting Sensitivity		V_i (lim)	−3dB point from V_O (V_i=80dBμ, Δf=±75KHz)		50	55	dBμ
AM Rejection Ratio		AMR	FM: Δf=±75KHz dev AM: 30% Mod, fm=1KHz V_i=80dBμ		50		dB
Detector Output Voltage		V_O	Δf=±75KHz dev V_i=80dBμ	300	500	700	mV
Total Harmonic Distortion		THD	Δf=±22.5KHz dev V_i=80dBμ		0.1		%
Signal to Noise Ratio		S/N	Δf=±75KHz dev V_i=80dBμ		75		dB
Muting Attenuation		M (att)	Δf=±75KHz dev V_i=80dBμ, V_4=0		70		dB
Meter Driver Voltage		V_3 (max)	V_i=110dBμ		4.0		V
Input Impedance	Resistance	Rip	f=10.7MHz 1 PIN-GND		5		KΩ
	Capacitance	Cip			4.5		pF
Output Impedance	Resistance	Rop	f=10.7MHz 6 PIN-GND		1.3		KΩ
	Capacitance	Cop			4		pF
Output Resistance		R_O	f=400Hz 8 PIN-GND		7.7		KΩ

TEST CIRCUIT

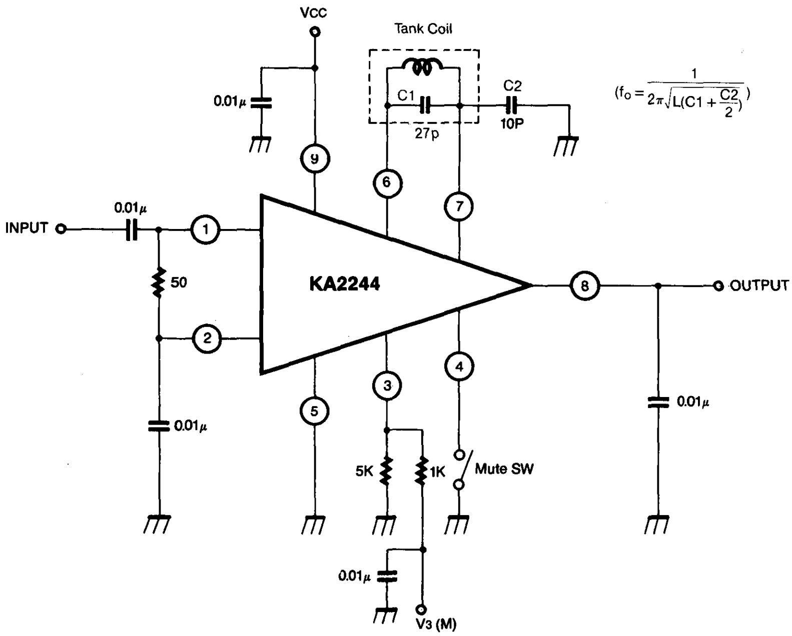
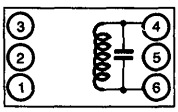


Fig. 2

COIL SPECIFICATIONS

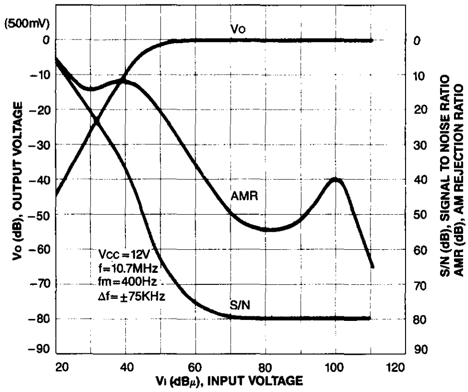


C_o (pF)	f (MHz)	Q_o (%)	TURNS		
			4-6		
27	10.7	150	18		

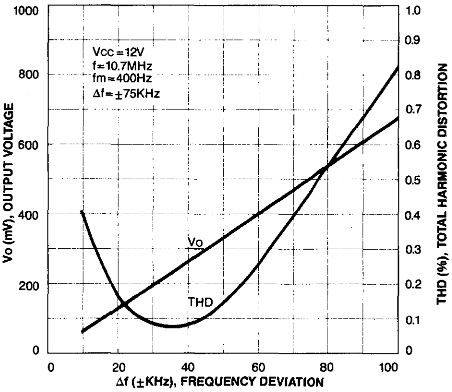
Seoul Jupa SJ-59JG-045 0.1mmϕ UEW

3

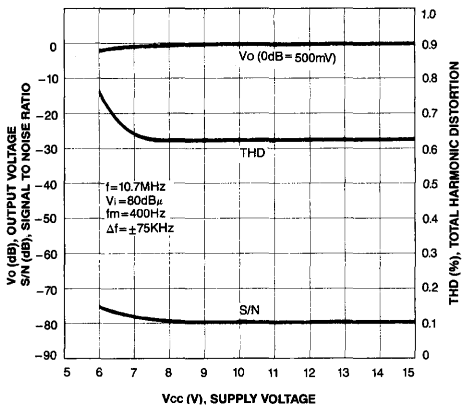
OUTPUT VOLTAGE
SIGNAL TO NOISE RATIO — INPUT VOLTAGE
AM REJECTION RATIO



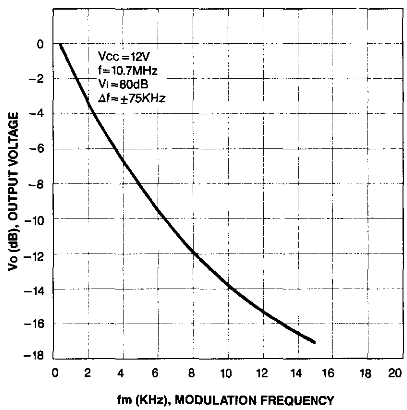
OUTPUT VOLTAGE, TOTAL HARMONIC DISTORTION —FREQUENCY DEVIATION



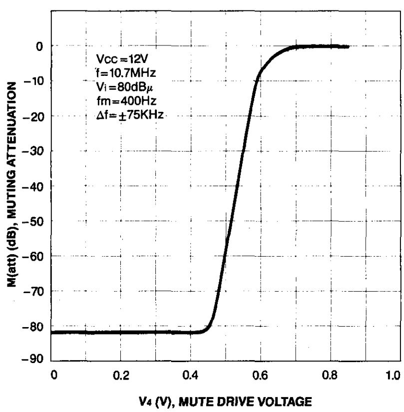
OUTPUT VOLTAGE
TOTAL HARMONIC DISTORTION —SUPPLY VOLTAGE
SIGNAL TO NOISE RATIO



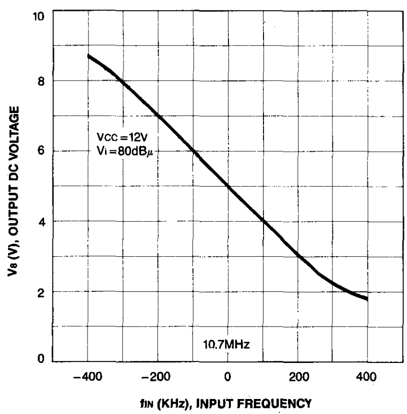
OUTPUT VOLTAGE-MODULATION FREQUENCY



MUTING ATTENUATION-MUTE DRIVE VOLTAGE



OUTPUT DC VOLTAGE-INPUT FREQUENCY

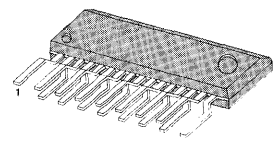


FM IF SYSTEM FOR CAR STEREOS

The KA22441 is a monolithic integrated circuit consisting of an FM IF system suitable for use in car stereos and music centers.

It features practically all of the functions used in an FM tuner, including an AGC output, AFC output, level meter output in a single package.

16 ZSIP



FUNCTIONS

- FM IF amplifier.
- Quadrature detector.
- AFC output.
- AGC output.
- Level meter output.
- Muting for weak signal.
- Muting for detuned condition.

FEATURES

- **Soft muting function.**
- **Variable muting maximum attenuation.**
- **Variable muting attack input signal.**
- **Variable muting slope with respect to input signal level.**
- **Level meter output.**
- **AFC output.**
- **AGC output.**
- **High sensitivity (V_i (lim)=25dBμ: Typ).**
- **High output level.**
- **Good S/N ratio (78dB: Typ).**
- **Low distortion (0.05%: Typ).**
- **Wide operating supply voltage range (6V ~ 14V).**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22441	16 ZSIP	−20 ~ +70°C

BLOCK DIAGRAM

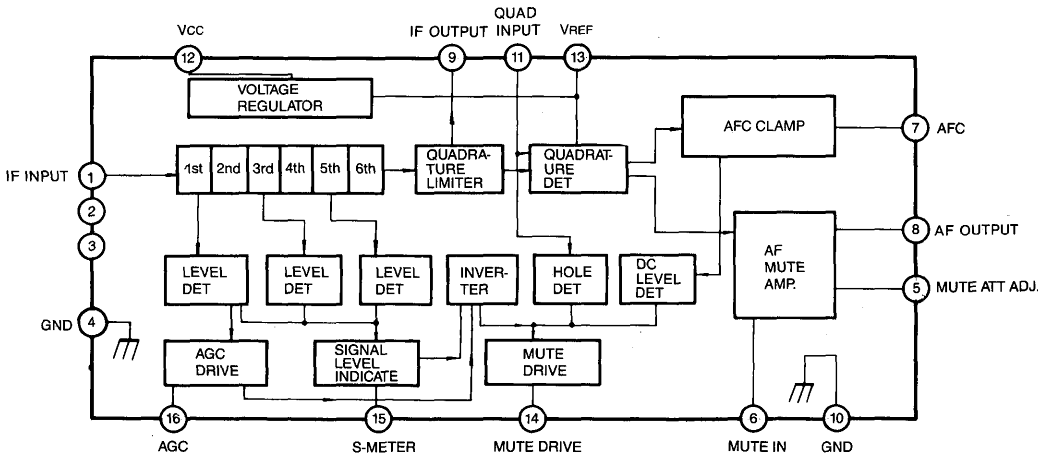


Fig. 1

3

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	Pd	640	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=8V, Δf=±75KHz, V_i=100dBμ, fm=400Hz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		6	8	14	V
Quiescent Circuit Current	I_{CC}	V_i=0	15	21	27	mA
Input Limiting Sensitivity	V_i (lim)	V_O (V_i=100dBμ) −3dB down		25	29	dBμ
Dectector Output Voltage	V_O		200	260	320	mV
Total Harmonic Distortion	THD			0.05	0.2	%
Signal to Noise Ratio	S/N		70	78		dB
AM Rejection Ratio	AMR	AM: fm=1KHz, 30% Mod	50	63		dB
Signal Meter Output Voltage	V_M	V_i=0	0	0.1	0.3	V
		V_i=100dBμ	4.5	5.3	6.0	
AGC Output Voltage	$V_{(AGC)}$	V_i=0	3.5	4.1	4.5	V
		V_i=100dBμ	0	0.02	0.3	
Muting Sensitivity	M (sen)	V_{14}=2V	22	26	32	dBμ
Muting Attenuation	$M_{(att)}$	V_6=2V	10	15	20	dB
		V_6=5V	24	28	32	
Muting Bandwidth	$M_{(BW)}$	V_{14}=2V	140	210	370	KHz

TEST CIRCUIT

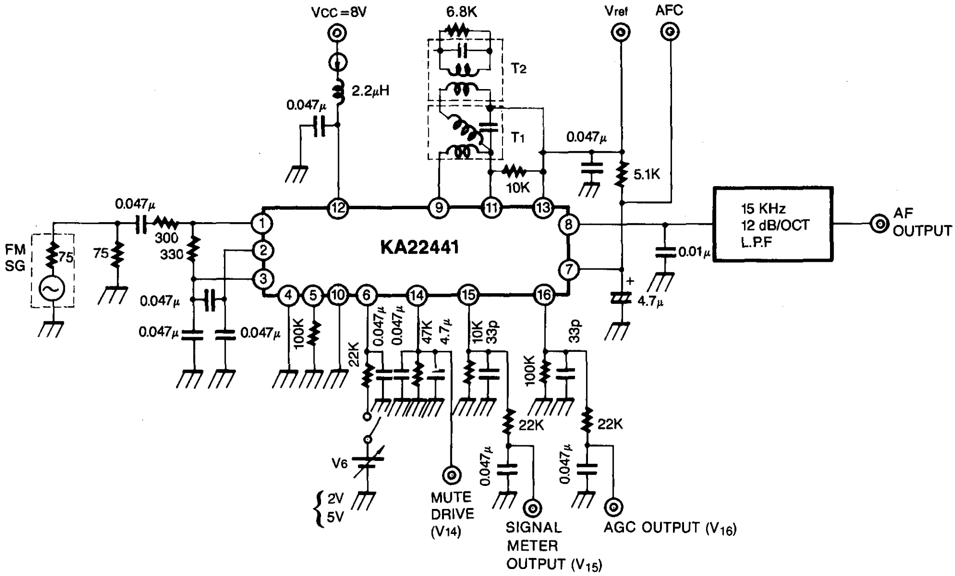
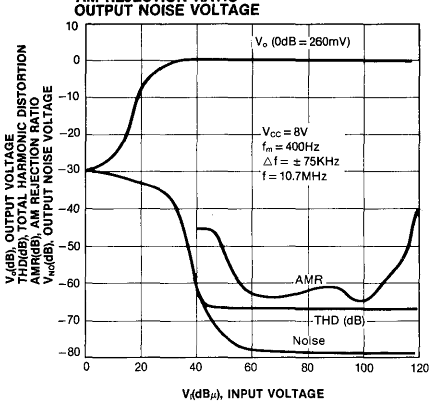
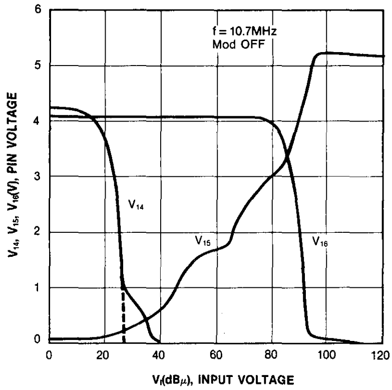


Fig. 2

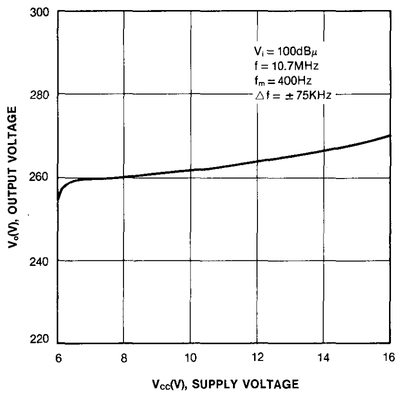
OUTPUT VOLTAGE
TOTAL HARMONIC DISTORTION
AM REJECTION RATIO
OUTPUT NOISE VOLTAGE -INPUT VOLTAGE



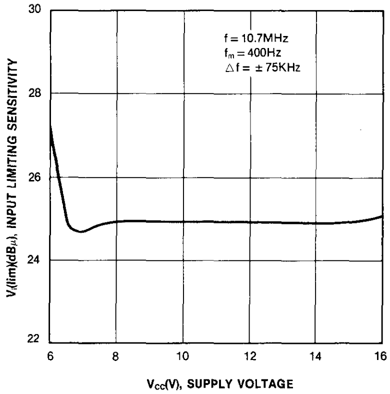
PIN VOLTAGE-INPUT VOLTAGE



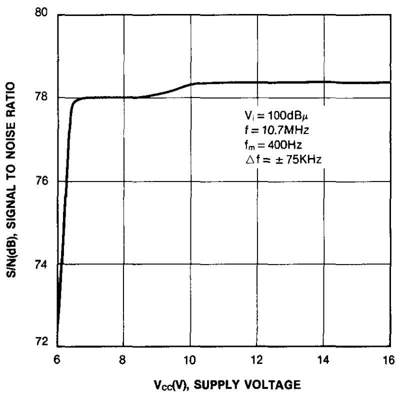
OUTPUT VOLTAGE-SUPPLY VOLTAGE



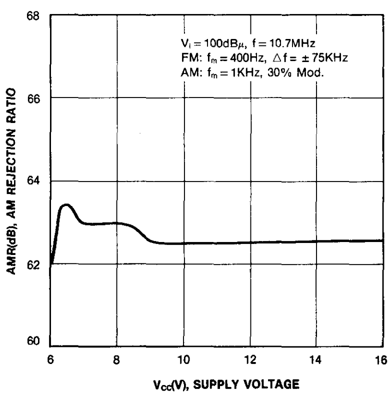
INPUT LIMITING SENSITIVITY-SUPPLY VOLTAGE



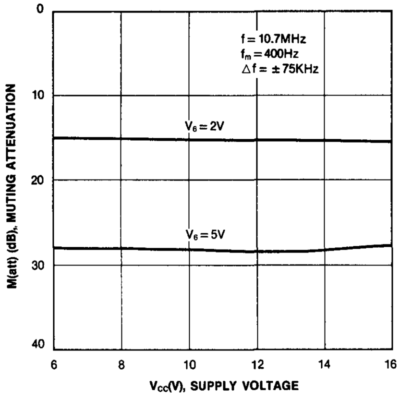
SIGNAL TO NOISE RATIO-SUPPLY VOLTAGE



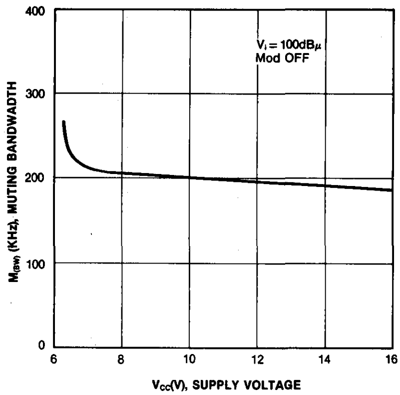
AM REJECTION RATIO-SUPPLY VOLTAGE



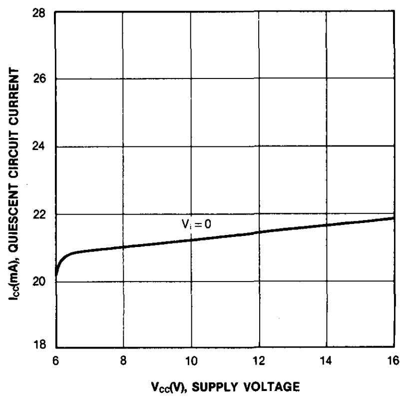
MUTING ATTENUATION-SUPPLY VOLTAGE



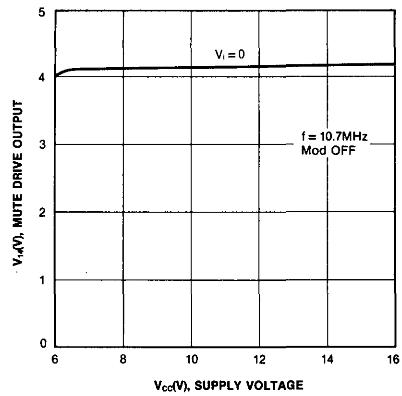
MUTING BANDWIDTH-SUPPLY VOLTAGE



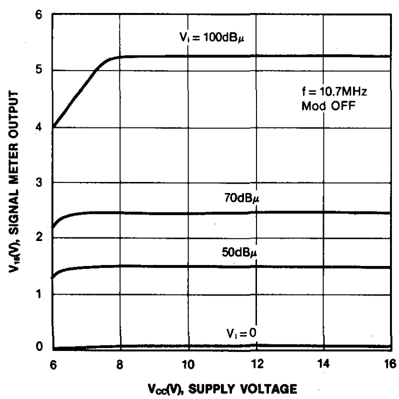
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



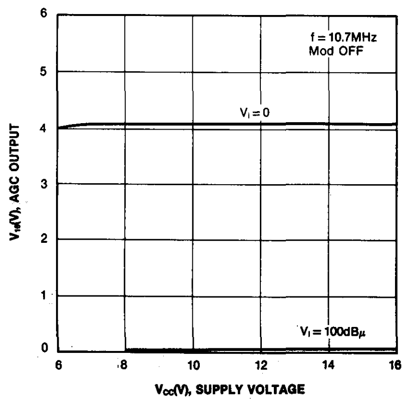
MUTE DRIVE OUTPUT-SUPPLY VOLTAGE



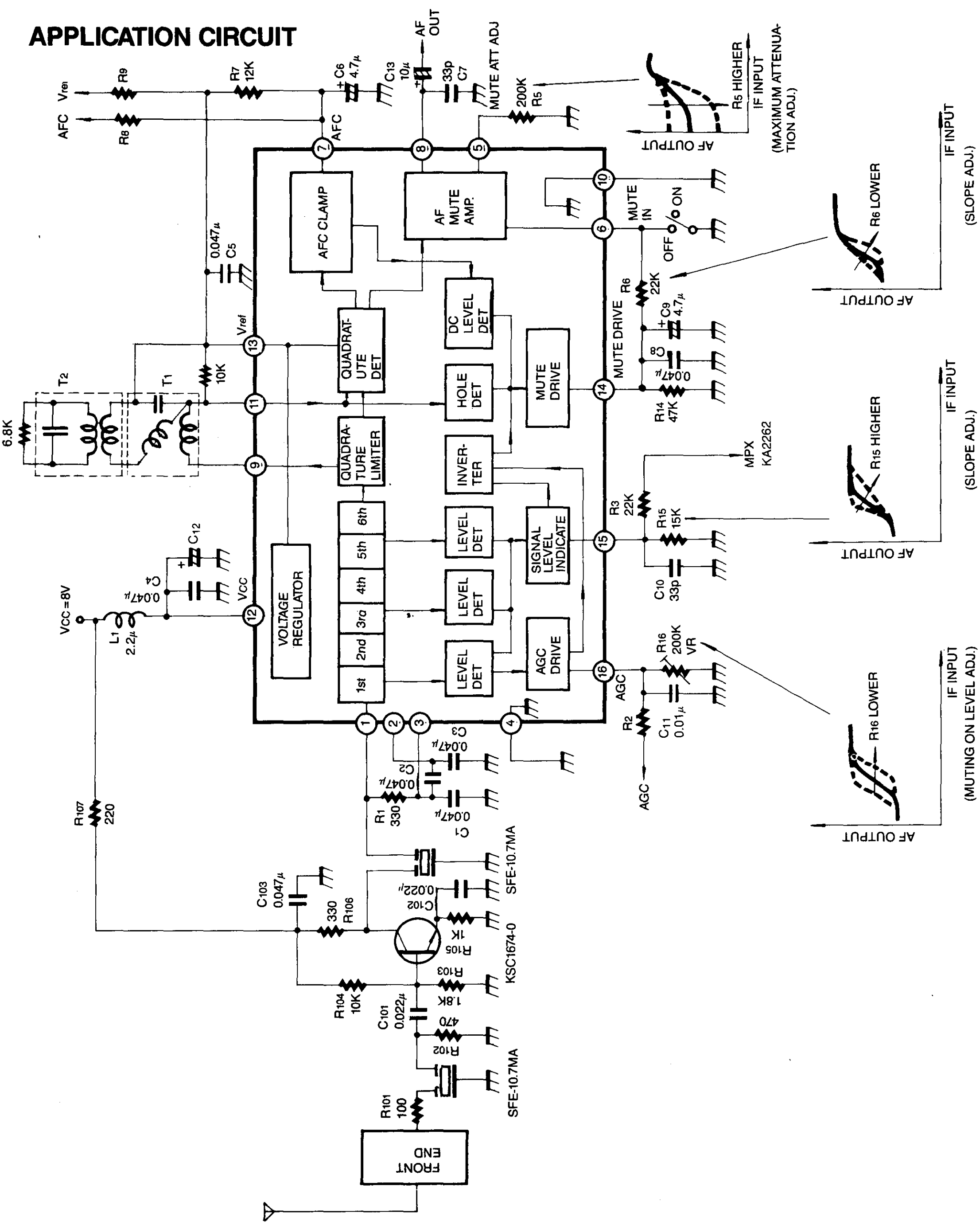
SIGNAL METER OUTPUT-SUPPLY VOLTAGE



AGC OUTPUT-SUPPLY VOLTAGE



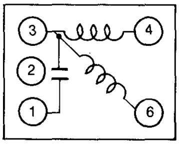
APPLICATION CIRCUIT



3

COIL SPECIFICATIONS

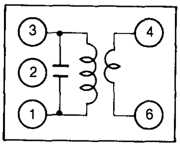
1. T1



C_o (pF)	f (MHz)	Q_o (%)	Turns	
			3 – 4	6 – 3
120	10.7	20 (Min)	89 1/2	17 1/2

KOREA TOKO 292MEA-K5018FKG-KR 0.07Ø 2UEW

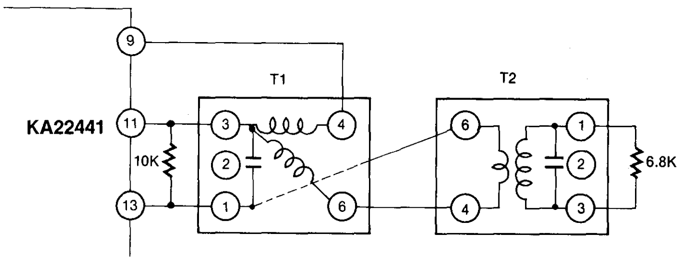
2. T2



C_o (pF)	f (MHz)	Q_o (%)	Turns	
			1 – 3	6 – 4
62	10.7	20 (Min)	24	1

KOREA TOKO 292MEA-K5019AN-KR 0.07Ø 2UEW

COIL COMBINATION



EXTERNAL COMPONENTS

C_1, C_2, C_3: **IF amplifier bypass capacitors**
These capacitors bypass to the ground both the carrier signal and the high-frequency components of the amplifier output.

C_4 : **Power supply bypass capacitor**

C_5 : **Internal regulated power supply bypass capacitor**

C_6 : **AFC output smoothing capacitor**
This capacitor bypasses to the ground the detector signal output at Pin 7.

C_7 : **De-emphasis capacitor**
The value of the C_8 determines the de-emphasis time constant.

C_8 : **Mute drive output smoothing capacitor**
This capacitor bypasses to the ground high-frequency noise components included in the muting output.

C_{10} : **Signal meter output voltage smoothing capacitor**
This capacitor is used to reduce any IF carrier signal components or other high-frequency components remaining on the level meter output voltage.

C_{11} : **AGC voltage smoothing capacitor**
If C_{11} is not connected, the AGC output will contain residual IF carrier frequency components.

R_1 : **IF amplifier resistor**
The IF amplifier input impedance is determined by the value of this resistance.

R_5 : **Muting maximum attenuation adjustment resistor**
The value of this resistor sets the maximum muting attenuation which is used when no signal is present or in the detuned condition. If the value of R_5 is made small, the maximum muting attenuation is decreased.

R_6 : **Mute drive current adjusting resistor**
This resistor is used to adjust the slope of the muting attenuation. If the value of this resistor is made small, the muting slope for the input signal level is increased.

R_7 : **Muting bandwidth adjustment resistor**
This resistor is capable of adjusting the muting bandwidth and AFC sensitivity. If the value of R_7 is made small, the muting bandwidth widens and the AFC sensitivity decreases.

R_{11} : **Damping resistor**
If the value of R_{11} is made small, the Q of the tuned circuit decreases with an accompanying decrease in gain.

R_{12} : **Damping resistor**

R_{14} : **Mute drive load resistor**
If R_{14} is made large, the time required for muting to be removed will increase.

R_{15} : **Signal meter output load resistor**
This resistor is used to adjust the slope of the muting attenuation. If the value of this resistor is made small, the slope of the muting attenuation is increased.

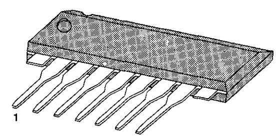
R_{16} : **AGC output load resistor**
This resistor is used to set the weak-signal muting starting point. If the value of this resistor is made small, the starting point of input signal level for muting is raised.

L_1 : **Power supply chock coil**

T_1, T_2 : **IF transformer**
The detector output voltage and total harmonic distortion are determined by the Q of this quadrature detector coil.

FM IF SYSTEM FOR CAR RADIOS

The KA2245 is a monolithic integrated circuit consisting of an FM IF amplifier and detector.
It is suitable for car radios.



FUNCTIONS

- 3-stage IF amplifier.
- Peak detector.

FEATURES

- **Suitable for FM car radios.**
- **Wide operating supply voltage range: V_{CC} = 8V ~ 14V).**
- **High detector output voltage (V_O = 500mV, Typ).**
- **Excellent AM rejection: AMR=50dB (Typ).**
- **High sensitivity: V_I (lim)=50dBμV (Typ).**
- **Simplified single coil tuning.**
- **Low distortion (THD=0.1%: Typ).**
- **Minimum number of external parts required.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2245	7 SIP	− 20 ~ + 70°C

BLOCK DIAGRAM

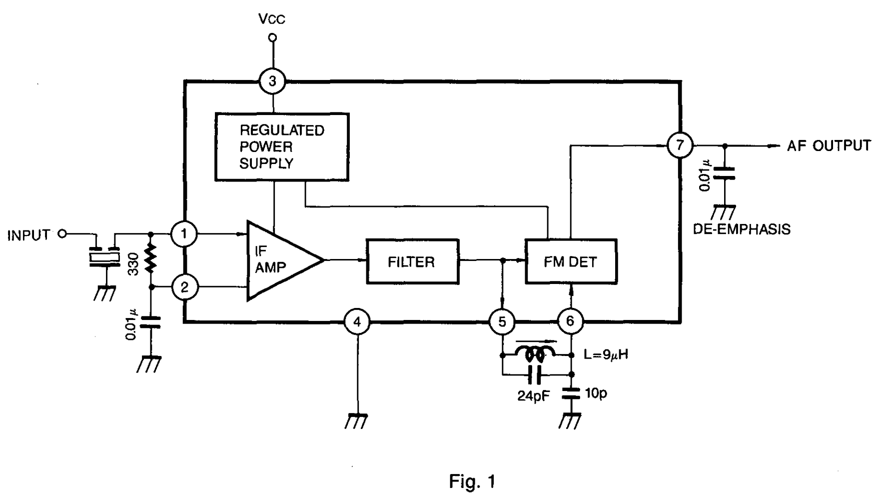


Fig. 1

3

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Input Voltage	V_i	0.7	V
Power Dissipation	*P_d	400	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

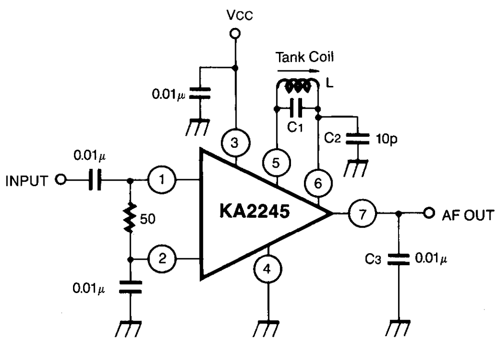
* : Derated above Ta=25°C in the proportion of 4mW/°C

ELECTRICAL CHARACTERISTICS

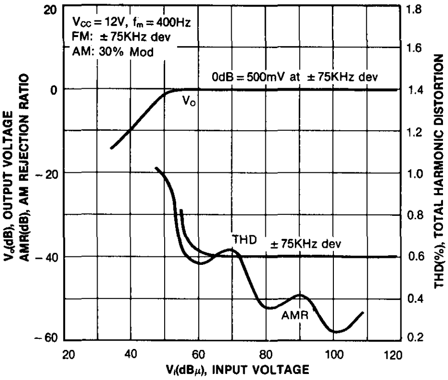
(T_a = 25°C, V_{CC} = 12V, f = 10.7MHz, fm = 400Hz)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current		I_{CC}	V_i=0	8	12	15	mA
Input Limiting Sensitivity		V_i (lim)	−3dB point from V_O V_i=80dBμ, Δf=±75KHz		50	55	dBμ
AM Rejection Ratio		AMR	FM: Δf=±75KHz dev AM: 30% Mod V_i=80dBμ		50		dB
Detector Output Voltage		V_O	Δf=±75KHz dev V_i=80dBμV	300	500	700	mV
Total Harmonic Distortion		THD	Δf=±22.5KHz dev V_i=80dBμV		0.2		%
Signal to Noise Ratio		S/N	Δf=±75KHz dev V_i=80dBμV		60		dB
Input Impedance	Resistance	R_{ip}	f=10.7MHz 1PIN-GND		5		KΩ
	Capacitance	C_{iP}			4.5		pF
Output Impedance	Resistance	R_{OP}	f=10.7MHz 5 PIN-GND		1.3		KΩ
	Capacitance	C_{OP}			4		pF
Output Resistance		R_O	f=400Hz 7 PIN-GND	6.2	7.7	9.5	KΩ

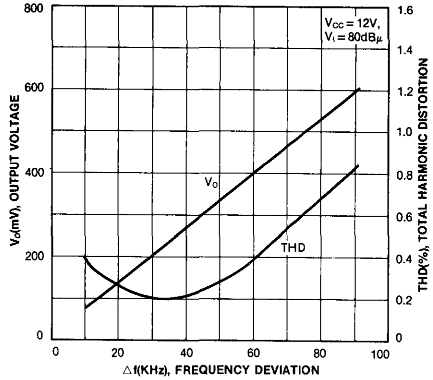
TEST CIRCUIT



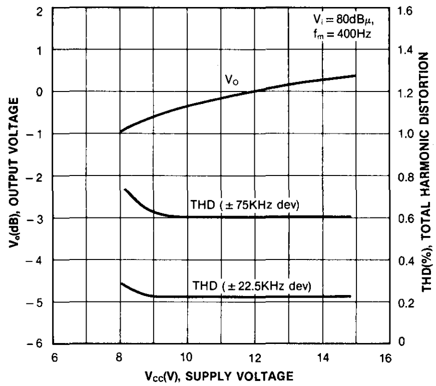
**OUTPUT VOLTAGE
TOTAL HARMONIC DISTORTION-INPUT VOLTAGE
AM REJECTION RATIO**



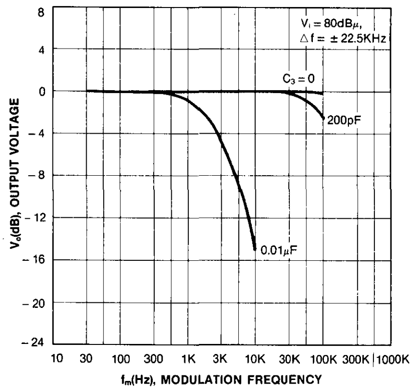
**OUTPUT VOLTAGE
TOTAL HARMONIC DISTORTION -FREQUENCY DEVIATION**



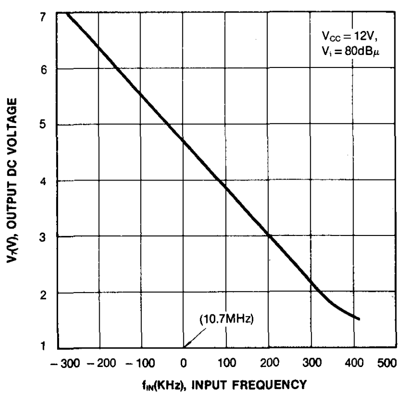
**OUTPUT VOLTAGE
TOTAL HARMONIC DISTORTION -SUPPLY VOLTAGE**



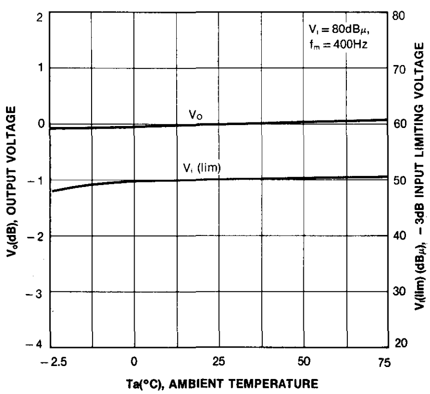
OUTPUT VOLTAGE-MODULATION FREQUENCY



OUTPUT DC VOLTAGE-INPUT FREQUENCY



**OUTPUT VOLTAGE -AMBIENT
-3dB INPUT LIMITING VOLTAGE TEMPERATURE**



APPLICATION CIRCUIT

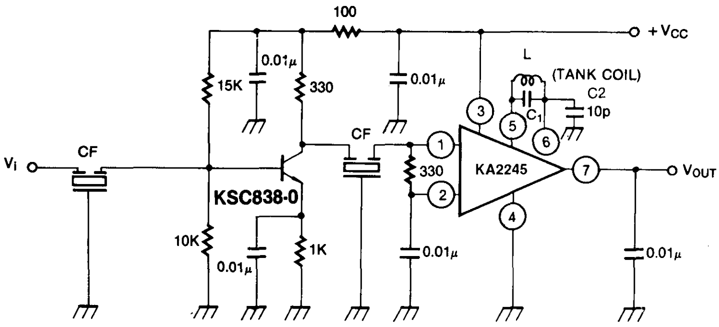
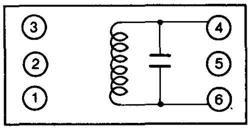


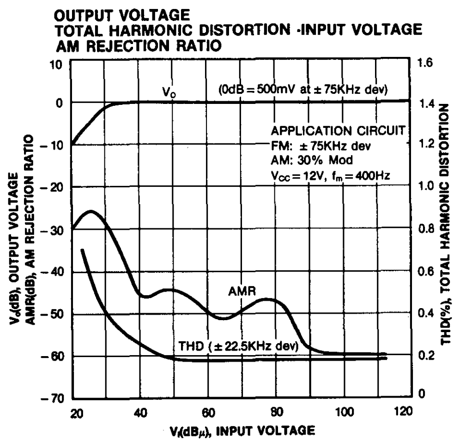
Fig. 3

$$\left(f_o = \frac{1}{2\pi\sqrt{L(C1 + \frac{C2}{2})}}\right)$$

COIL SPECIFICATIONS



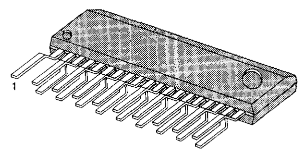
C_o (pF)	f (MHz)	O_o (%)	Turns		
			4 – 6		
27	10.7	150	18		



ELECTRONIC TUNING AM RADIO RECEIVER FOR CAR STEREOS

The KA22461 is a monolithic integrated circuit for the AM tuner system of car stereos.
It contains a subsystem that provides the mixer, oscillator, IF AMP, detector and ON channel detector for electronic tuning of the AM radio receiver.
It is suitable for the radio receiver in car audio sets.

19 ZSIP



FEATURES

- **Varactor-diode tuning**
- **Excellent overload characteristics**
- **Wide AGC range and good sensitivity**
- **On channel detector for auto scan stop**
- **Local/distance selector**
- **Oscillator buffer output**
- **Delayed AGC for RF amplifier**
- **Special low level oscillator to reduce tracing error**
- **Wide operating supply voltage range (8V ~ 15V)**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22461	19 ZSIP	−20 ~ +70°C

BLOCK DIAGRAM

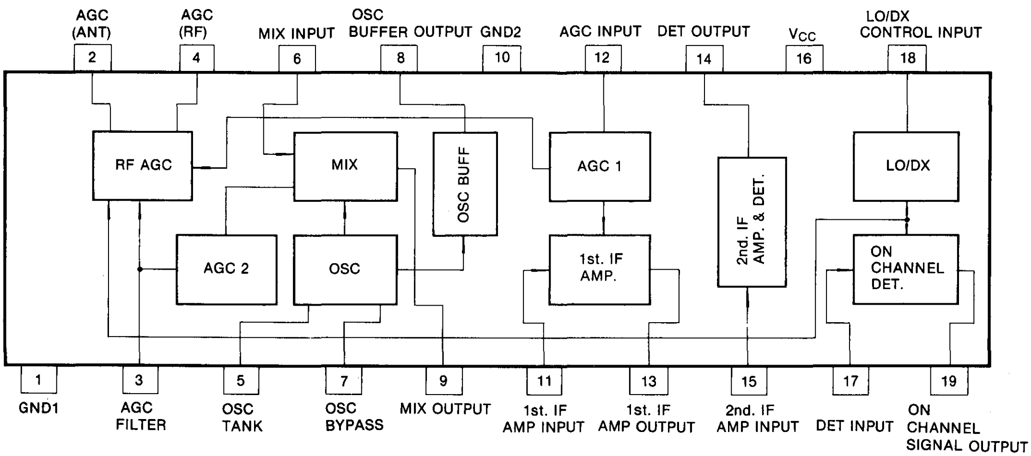


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Input Voltage	V_i	3.0	V
Power Dissipation	P_d	430 (Ta = 75°C)	mW
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 10V, f = 1MHz, f_m = 400Hz, 30% Mod)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i = 0	10	14	21	mA
Maximum Sensitivity	V_i (Sen)	V_o = 30mV	14	21	28	dBμ
Signal to Noise Ratio	S/N	V_i = 21dBμ	8	13		dB
Detector Output Voltage	V_o	V_i = 74dBμ	70	100	130	mV
Total Harmonic Distortion	THD1	V_i = 74dBμ		0.3	1.0	%
	THD2	V_i = 120dBμ		0.5	1.0	
ON Channel Signal	V_{19} (L)	V_i = 0dBμ, R_L = 18K			0.5	V
	V_{19} (H)	V_i = 74dBμ, R_L = 18K	8.0			

TUNER PERFORMANCE CHARACTERISTICS

(Ta = 25°C, V_{CC} = 10V, f = 1MHz, f_m = 400Hz, 30% Mod)

Characteristic	Test Conditions		Value	Unit
Maximum Sensitivity	V_o = 30mV		22	dBμ
Usable Sensitivity	S/N = 20dB		28	dBμ
Detector Output Voltage	V_i = 74dBμ		100	mV
Total Harmonic Distortion	V_i = 74dBμ		0.3	%
	V_i = 126dBμ		0.6	
	V_i = 74dBμ, 80% Mod		1.2	
Signal to Noise Ratio	V_i = 74dBμ		52	dB
IF Rejection Ratio	V_o = 30mV, IF = 450KHz		56	dB
Image Rejection Ratio	V_o = 30mV, f + 2IF		57	dB
Selectivity	△f = ±10KHz		39	dB
Tweet	V_i = 74dBμ	2IF = 900KHz	40	dB
		3IF = 1350KHz	47	
DX Sensitivity	V_{19} = 8V		26	dBμ
ON Channel Bandwidth	V_i = 74dBμ		5	KHz
Oscillation Voltage	at pin 5		150	mV
	at pin 8		4	V

TEST CIRCUIT

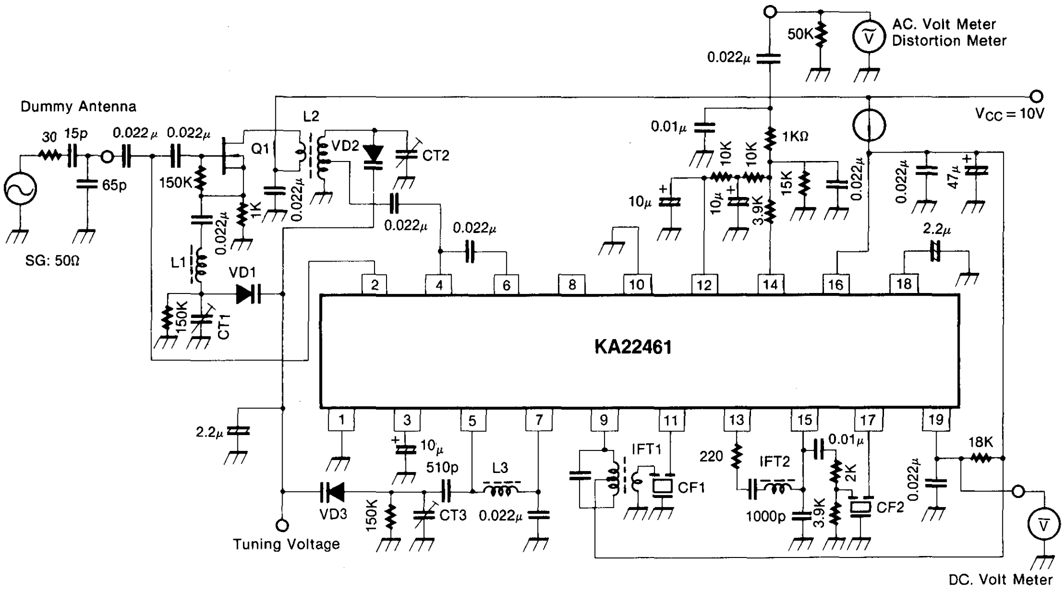


Fig. 2

APPLICATION CIRCUIT

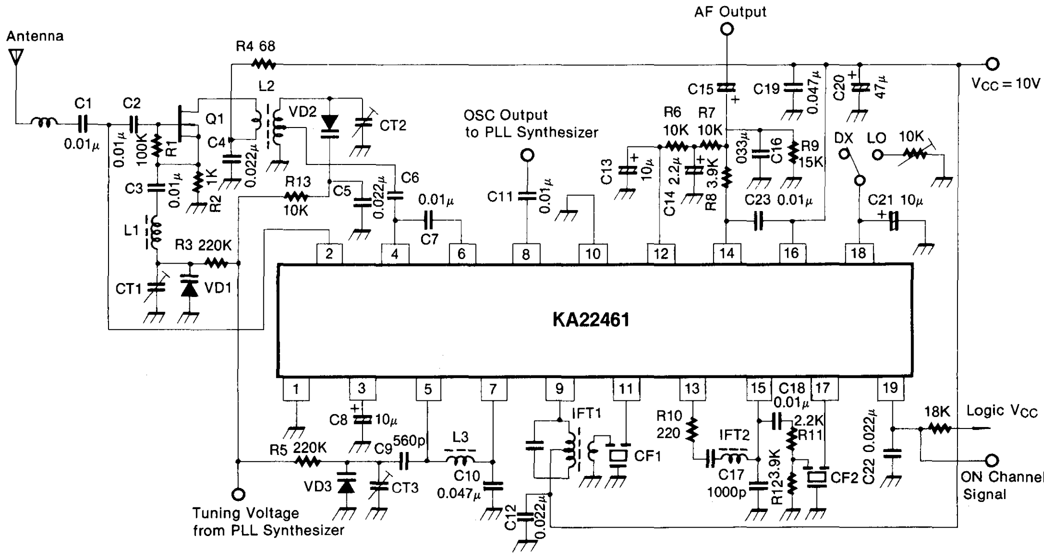
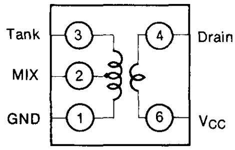


Fig. 3

3

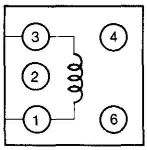
COIL SPECIFICATIONS

L1 & L2: Ant. & RF Coil



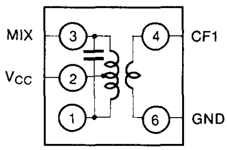
Q_u (%)	L (µH)	Turns		
80 min	170	1 – 2	2 – 3	4 – 6
		7	62	14

L3: OSC Coil



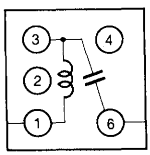
Q_u (%)	L (µH)	Turns		
60 min	95	1 – 3		
		48		

IFT1: IFT



Q_u (%)	C (pF)	Turns		
115 ± 20	180	1 – 2	2 – 3	4 – 6
		69	77	14

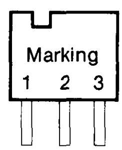
IFT2: IFT



L (µH)	C (pF)	L (µH)		
680	180	1 – 3		
		680		

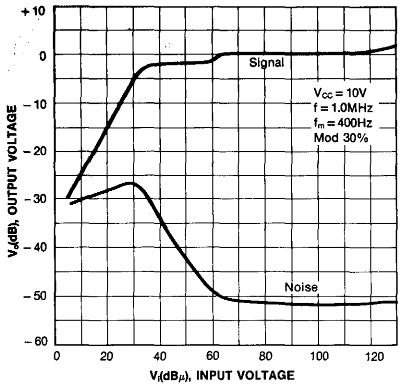
CERAMIC FILTER

	CFM2-450BL	CFM2-450ZL
Center Frequency	450KHz	450KHz
6dB Bandwidth	6KHz min.	4KHz min.
Selectivity ±9KHz	16dB min.	18dB min.
Insertion Loss	6dB max.	6dB max.
Input Impedance	1.5KΩ	1.0KΩ
Output Impedance	2.0KΩ	1.5KΩ

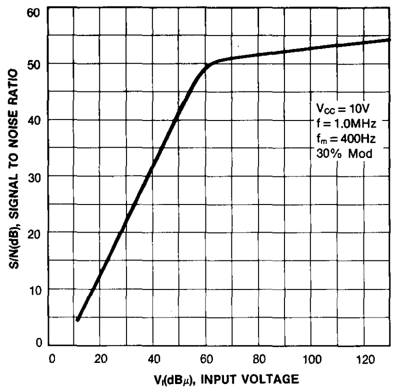


1: Input
2: GND
3: Output

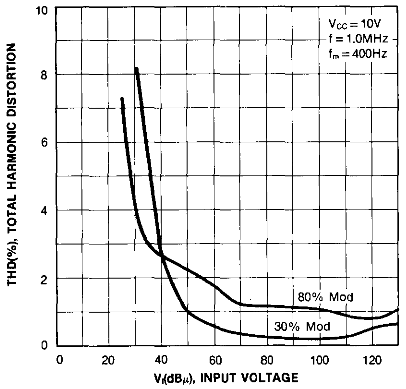
OUTPUT VOLTAGE-INPUT VOLTAGE



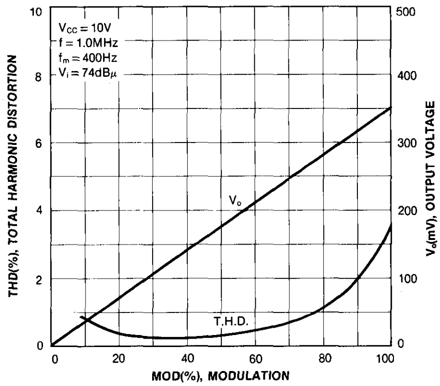
SIGNAL TO NOISE RATIO-INPUT VOLTAGE



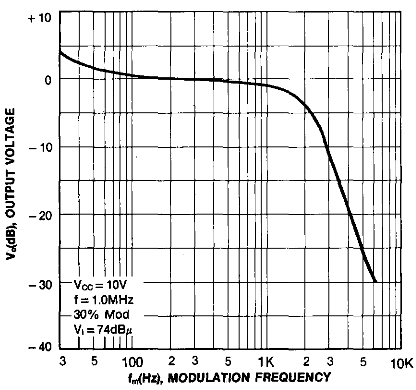
TOTAL HARMONIC DISTORTION-INPUT VOLTAGE



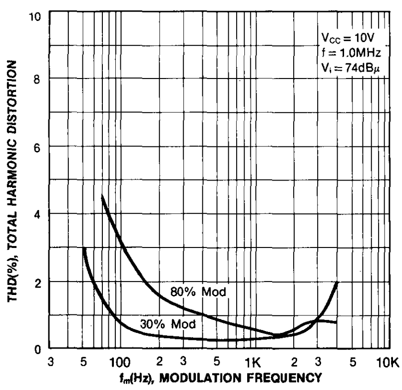
OUTPUT VOLTAGE / TOTAL HARMONIC DISTORTION -MODULATION



OUTPUT VOLTAGE-MODULATION FREQUENCY



TOTAL HARMONIC DISTORTION -MODULATION FREQUENCY

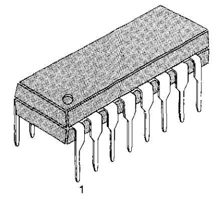


3

FM IF/AM TUNER SYSTEM

The KA2247 is a monolithic integrated circuit developed for the radio cassette tape recorder.

16 DIP



FUNCTIONS

- AM SECTION: RF amplifier, Mixer, OSC (with ALC), IF amplifier, Detector, AGC, Tuning indicator.
- FM SECTION: IF amplifier, Quadrature detector, AF preamplifier, Tuning indicator.

FEATURES

- **Minimum number of external parts required.**
- **Very good S/N: FM (81dB), AM (53dB).**
- **AM oscillator circuit with ALC: Oscillation output voltage of pin 16.**
  MW 130mV
  SW 70mV ~ 90mV
  (7MHz) ~ (24MHz)
- **Excellent AM whistle performance: Whistle 1% at V_i=100dB/m.**
- **Built-in tuning indicator.**
- **Built-in AM/FM function switch.**
- **Operating supply voltage range: V_{CC} = 3V ~ 8V.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2247	16 DIP	−20 ~ +70°C

BLOCK DIAGRAM

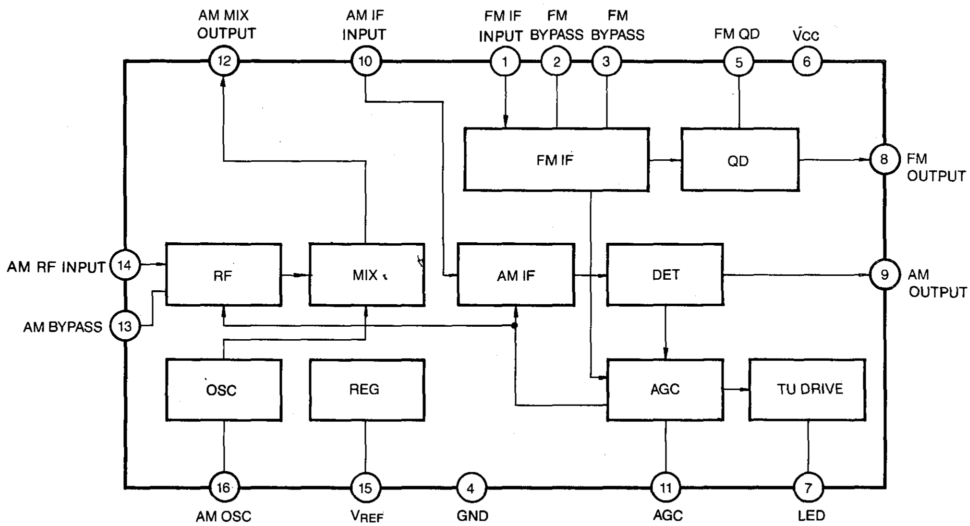


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	9	V
Circuit Current	I_{CC}	50	mA
Input Current (Pin 7)	I_7	20	mA
Output Current (Pin 15)	I_{15}	0.1	mA
Power Dissipation	P_d	450	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=4.5V)

FM Section (f=10.7MHz, Δf=±75KHz, fm=400Hz)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i=0		8.5	12.0	mA
Input Limiting Sensitivity	V_i (lim)	V_O (V_i=80dBμ) −3dB down		35	42	dBμ
Detector Output Voltage	V_O	V_i=80dBμ	183	260	367	mV
Total Harmonic Distortion	THD 1	V_i=80dBμ		0.55	1.2	%
	THD 2	V_i=80dBμ, Δf=±22.5KHz		0.05		
AM Rejection Ratio	AMR	V_i=80dBμ, AM: fm=1KHz, 30% Mod		60		dB
Signal to Noise Ratio	S/N 1	V_i=80dB μ	77	81		dB
	S/N 2	V_i=80dB μ, Δf=±22.5KHz		71		
Tuning Indication Voltage	V_L	I_L=1mA		39	49	dBμ

AM Section (f=1MHz, fm=400Hz, 30% Mod)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i=0		7.5	10.5	mA
Detector Output Voltage	V_O 1	V_i=23dBμ	17.3	31	55	mV
Detector Output Voltage	V_O 2	V_i=60dBμ	87	122	174	mV
Total Harmonic Distortion	THD 1	V_i=60dBμ		0.45	1.3	%
	THD 2	V_i=100dBμ		1.5	3.0	
Signal to Noise Ratio	S/N 1	V_i=23dBμ	18.0	21.5		dB
	S/N 2	V_i=60dBμ	48	53		
Tuning Indication Voltage	V_L	I_L=1mA	22	30	38	dBμ
Oscillation Output Voltage	V_{OSC}	f=24MHz	60	86	120	mV

TEST CIRCUIT

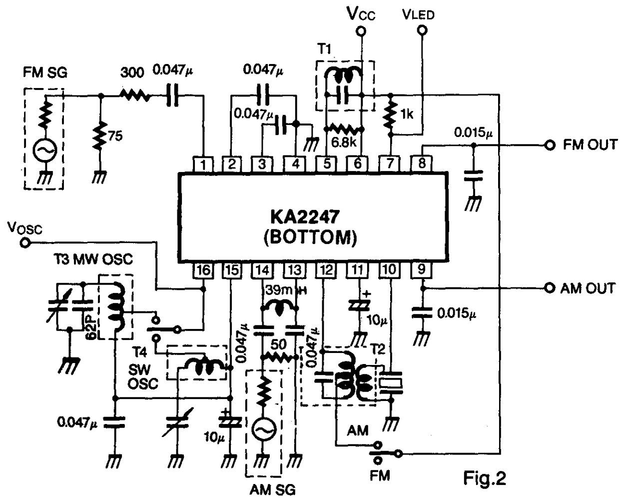
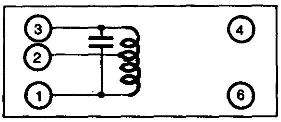


Fig.2

COIL SPECIFICATIONS

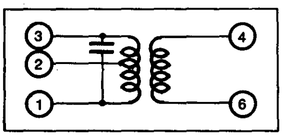
T1 FM IF (DET)



C_o (PF)	f (MHz)	Q_o	TURNS
1-3		1-3	1-3
56	10.7	95	12

Seoul Jupa
0.12mmϕ UEW

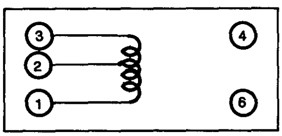
T2 AM IFT (MIX OUT)



C_o (PF)	f (KHz)	Q_o	TURNS		
1-3		1-3	1-2	2-3	4-6
180	455	110	90	62	8

Seoul Jupa
0.07mmϕ UEW

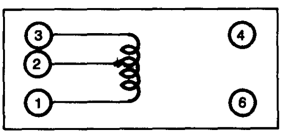
T3 (MW OSC)



f (KHz)	L (μH)	Q_o	TURNS	
	1-3	1-3	1-2	2-3
796	140	140	32	32

Seoul Jupa
0.07mmϕ UEW

T4 (SW OSC)

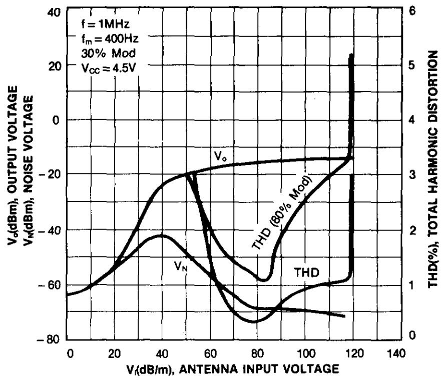


L (μH)	Q_o	TURNS	
1-3	1-3	1-2	2-3
12	80	12	12

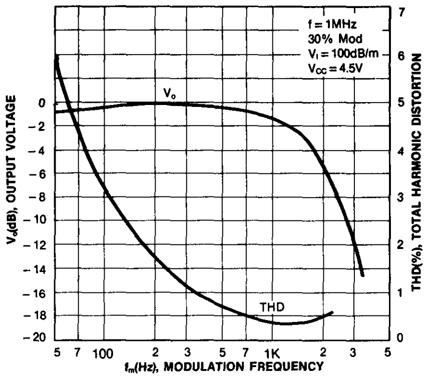
Seoul Jupa
0.1mmϕ UEW

(AM SECTION)

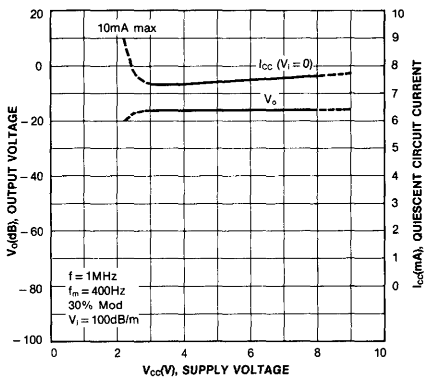
OUTPUT VOLTAGE
NOISE VOLTAGE ·ANTENNA INPUT VOLTAGE



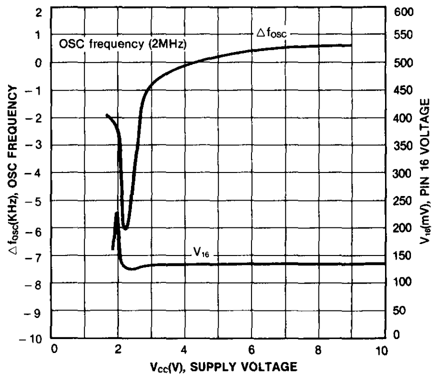
OUTPUT VOLTAGE
TOTAL HARMONIC DISTORTION ·MODULATION FREQUENCY



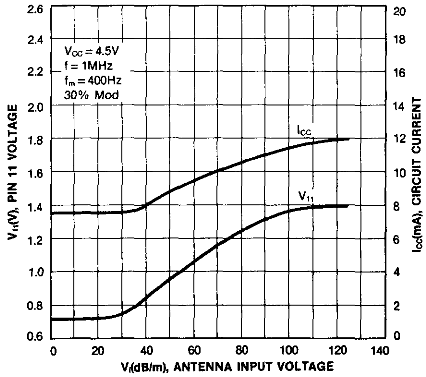
OUTPUT VOLTAGE
QUIESCENT CIRCUIT CURRENT ·SUPPLY VOLTAGE



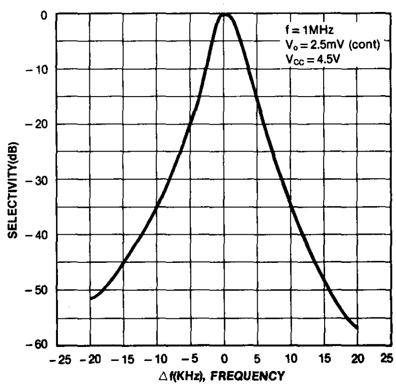
OSC FREQUENCY
PIN 16 VOLTAGE ·SUPPLY VOLTAGE



PIN 11 VOLTAGE
CIRCUIT CURRENT ·ANTENNA INPUT VOLTAGE

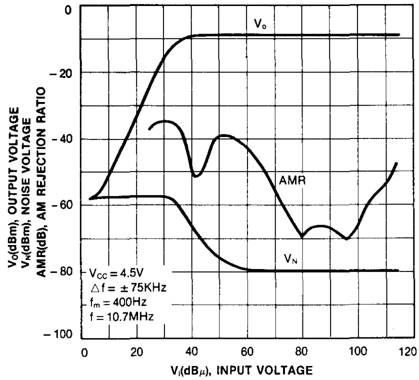


SELECTIVITY·FREQUENCY

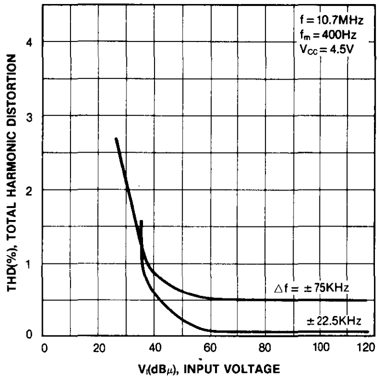


(FM SECTION)

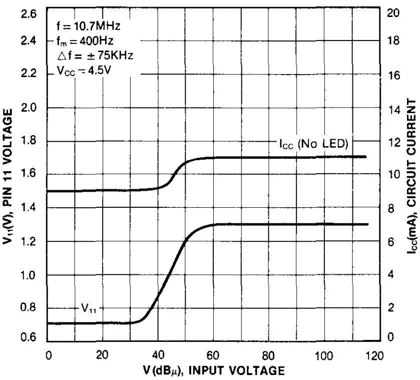
OUTPUT VOLTAGE
AM REJECTION RATIO · INPUT VOLTAGE
NOISE VOLTAGE



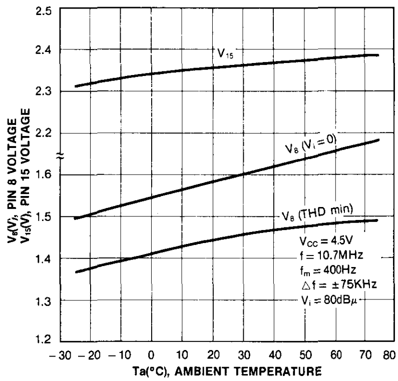
TOTAL HARMONIC DISTORTION-INPUT VOLTAGE



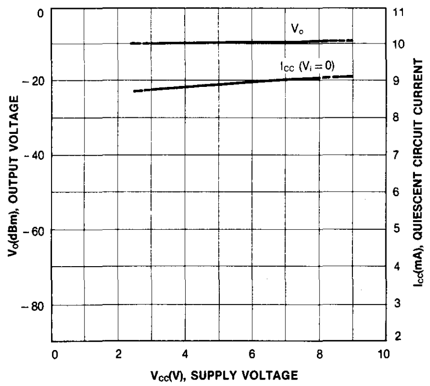
PIN 11 VOLTAGE
CIRCUIT CURRENT **·INPUT VOLTAGE**



PIN 8 VOLTAGE
PIN 15 VOLTAGE **·AMBIENT TEMPERATURE**



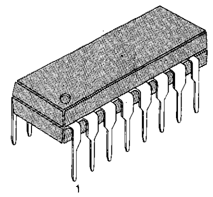
OUTPUT VOLTAGE
QUIESCENT CIRCUIT CURRENT **·SUPPLY VOLTAGE**



FM IF/AM TUNER SYSTEM

The KA22471 is a monolithic integrated circuit developed for the radio cassette tape recorder.

16 DIP



FUNCTIONS

- AM SECTION: Converter, IF amplifier, Detector, Tuning indicator.
- FM SECTION: IF amplifier, Quadrature detector, Tuning indicator.

FEATURES

- **Low quiescent circuit current.**
  AM: 7mA (Typ) FM: 10mA (Typ)
- **A minimum number of external parts required.**
- **Built-in AM/FM function switch.**
- **Tuning indicator: direct LED driving capability (I_L =10mA$_{(MAX)}$).**
- **One terminal AM/FM detector output.**
- **Advanced performance at high input signal.**
- **Operating supply voltage range: V_{CC}=3V ~ 8V.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22471	16 DIP	−20 ~ +70°C

BLOCK DIAGRAM

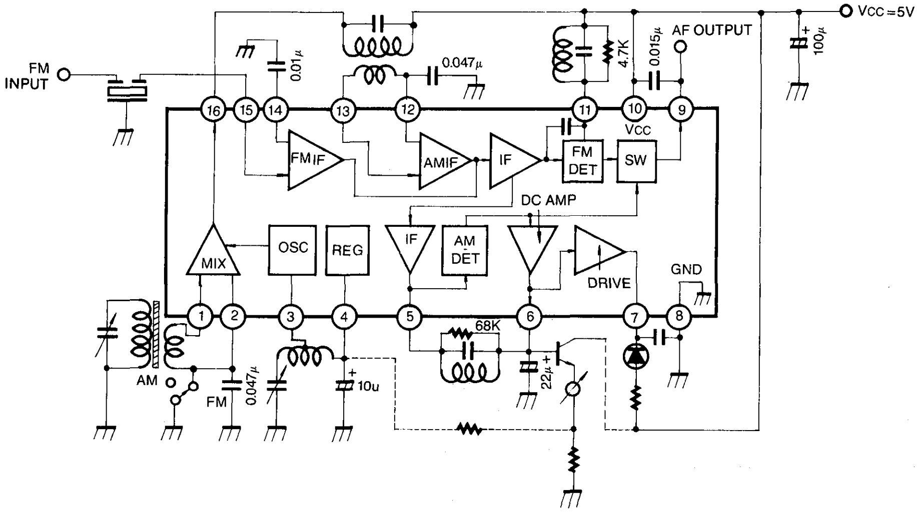


Fig. 1

Note: The dot line denotes a tuning meter application.

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	8	V
Power Dissipation	P_d	600	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=5V, unless otherwise specified)

FM Section (f=10.7MHz, fm=400Hz, Δf= ±22.5KHz)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i=0		10	15	mA
Input Limiting Sensitivity	V_i (lim)	V_O (V_i=80dBμ) −3dB down		40	46	dBμ
Detector Output Voltage	V_O	V_i=66dBμ, R_{DUMP}=4.7KΩ	57	85	114	mV
Total Harmonic Distortion	THD	V_i=80dBμ		0.05		%
AM Rejection Ratio	AMR	V_i=80dBμ, AM: fm=1KHz, 30% Mod		38		dB
Signal to Noise Ratio	S/N	V_i=80dBμ		65		dB
Signal Meter Output	V_M	V_i=100dBμ	1.55	1.7	1.85	V
Tuning Indication Voltage	V_L	I_L=1mA		46	52	dBμ

AM Section (f=1MHz, 30% Mod, fm=400Hz)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i=0		7	10	mA
Voltage Gain	A_V	V_i=26dBμ	20	30	60	mV
Detector Output Voltage	V_O	V_i=60dBμ	65	95	125	mV
Total Harmonic Distortion	THD	V_i=60dBμ		1.0		%
Signal to Noise Ratio	S/N	V_i=60dBμ		47		dB
Signal Meter Output	V_M	V_i=100dBμ	1.55	1.7	1.85	V
Tuning Indication Voltage	V_L	I_L=1mA		32		dBμ
Oscillator Stop Voltage	V_{stop}	R_{DUMP}= ∞		1.5		V

TEST CIRCUIT

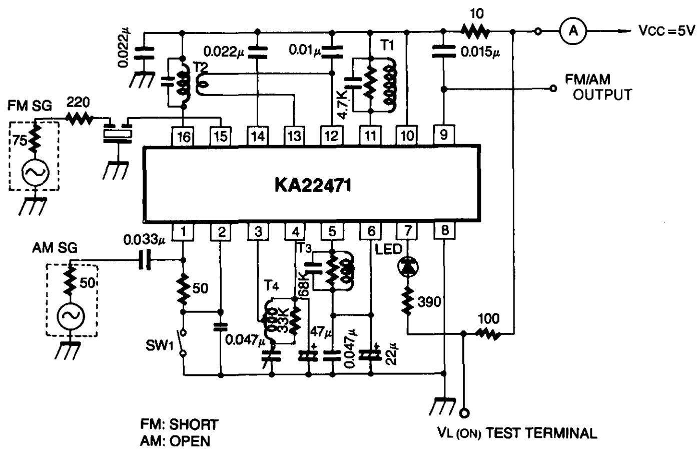
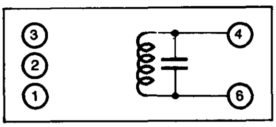


Fig. 2

COIL SPECIFICATIONS

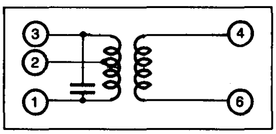
T1 FM IF (DET)



C_o (pF)	f (MHz)	Q_o	TURNS
4-6		4-6	4-6
47	10.7	150	14

Seoul Jupa
0.12mmφ UEW

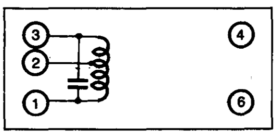
T2 AM IFT (MIX OUT)



C_o (PF)	f (KHz)	Q_o	TURNS		
1-3		1-3	1-2	2-3	4-6
180	455	110	90	62	8

Seoul Jupa
0.07mmφ UEW

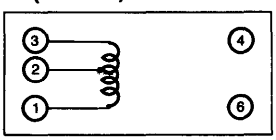
T3 AM IFT (DET)



C_o (pF)	f (KHz)	Q_o	TURNS
1-3		1-3	1-3
180	455	110	152

Seoul Jupa
0.07mmφ UEW

T4 (MW OSC)



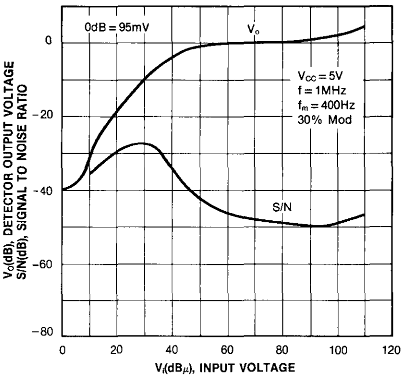
f (KHz)	L (μH)	Q_o	TURNS	
	1-3	1-3	1-2	2-3
796	288	120	13	75

Seoul Jupa
0.08mmφ UEW

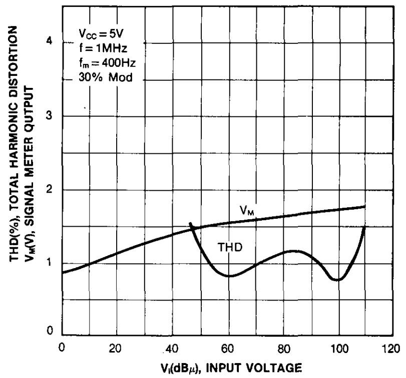
3

(AM SECTION)

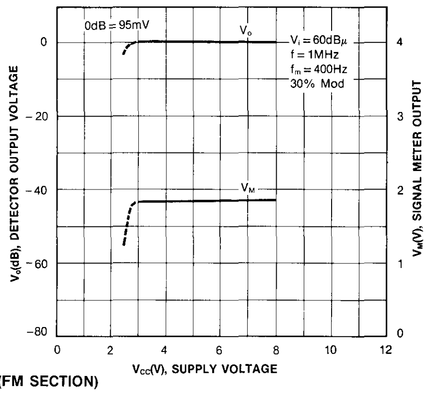
DETECTOR OUTPUT VOLTAGE
SIGNAL TO NOISE RATIO -INPUT VOLTAGE



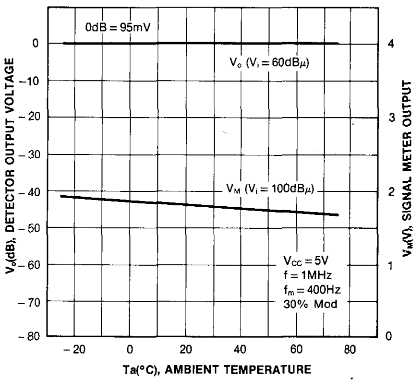
TOTAL HARMONIC DISTORTION
SIGNAL METER OUTPUT -INPUT VOLTAGE



DETECTOR OUTPUT VOLTAGE
SIGNAL METER OUTPUT -SUPPLY VOLTAGE

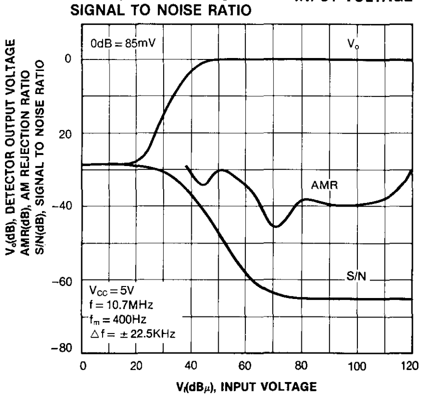


DETECTOR OUTPUT VOLTAGE -AMBIENT
SIGNAL METER OUTPUT TEMPERATURE

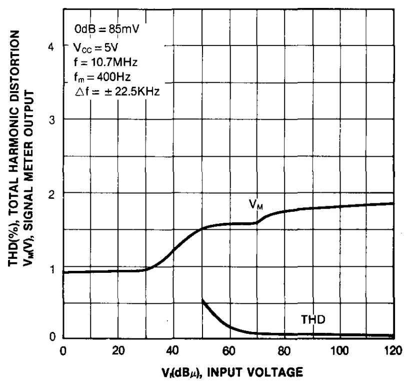


(FM SECTION)

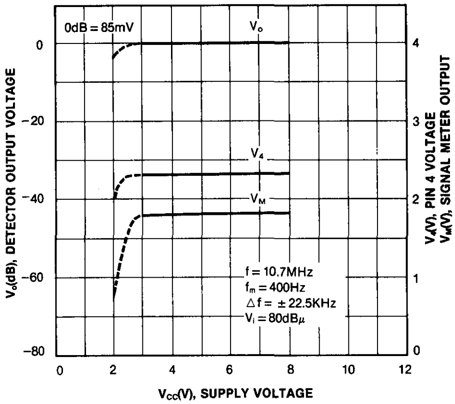
DETECTOR OUTPUT VOLTAGE
AM REJECTION RATIO -INPUT VOLTAGE
SIGNAL TO NOISE RATIO



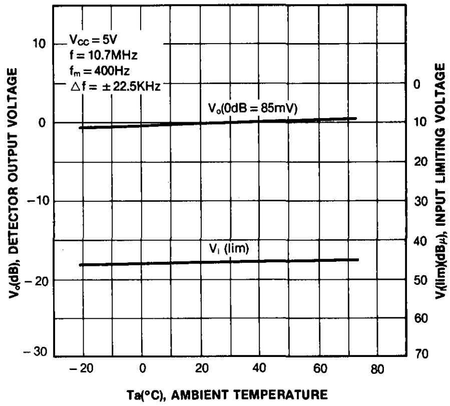
TOTAL HARMONIC DISTORTION
SIGNAL METER OUTPUT -INPUT VOLTAGE



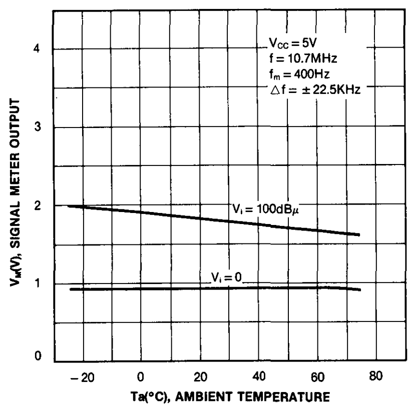
DETECTOR OUTPUT VOLTAGE
SIGNAL METER OUTPUT -SUPPLY VOLTAGE
PIN 4 VOLTAGE



DETECTOR OUTPUT VOLTAGE -AMBIENT
INPUT LIMITING VOLTAGE TEMPERATURE

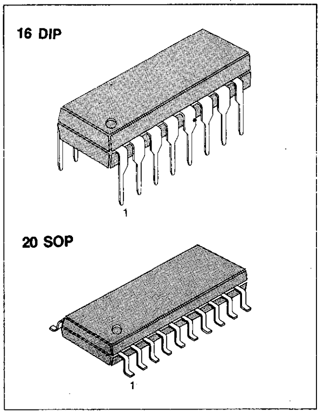


SIGNAL METER OUTPUT-AMBIENT TEMPERATURE



3V FM IF/AM TUNER SYSTEM

The KA2248 is a monolithic integrated circuit developed the for headphone stereo.



FUNCTIONS

- AM SECTION: Converter, IF amplifier, Detector, Tuning indicator
- FM SECTION: IF amplifier, Quadrature detector, Tuning indicator

FEATURES

- **Low quiescent current: AM; I_{CC}=3mA (Typ), V_{CC}=3V**
  FM; I_{CC}=8mA (Typ), V_{CC}=3V
- **Wide operating voltage range: V_{CC}=1.8V ~ 6V.**
- **Built-in AM/FM function switch.**
- **Tuning indicator: direct LED driving capability: 10mA (Max).**
- **One terminal AM/FM detector output.**
- **A minimum number of external parts required.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2248A	16 DIP	−20 ~ +70°C
KA2248D	20 SOP	

BLOCK DIAGRAM

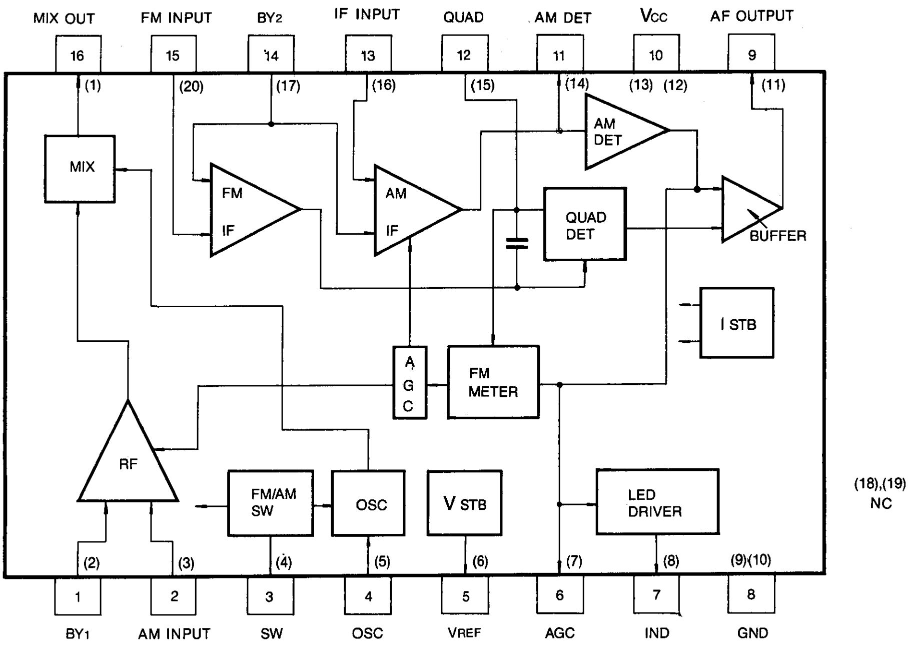


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Characteristic		Symbol	Value	Unit
Supply Voltage		V_{CC}	6	V
Power Dissipation	KA2248A	P_d	600	mW
	KA2248D		350	
Operating Temperature		T_{opr}	−20 ~ +70	°C
Storage Temperature		T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=3V, unless otherwise specified)

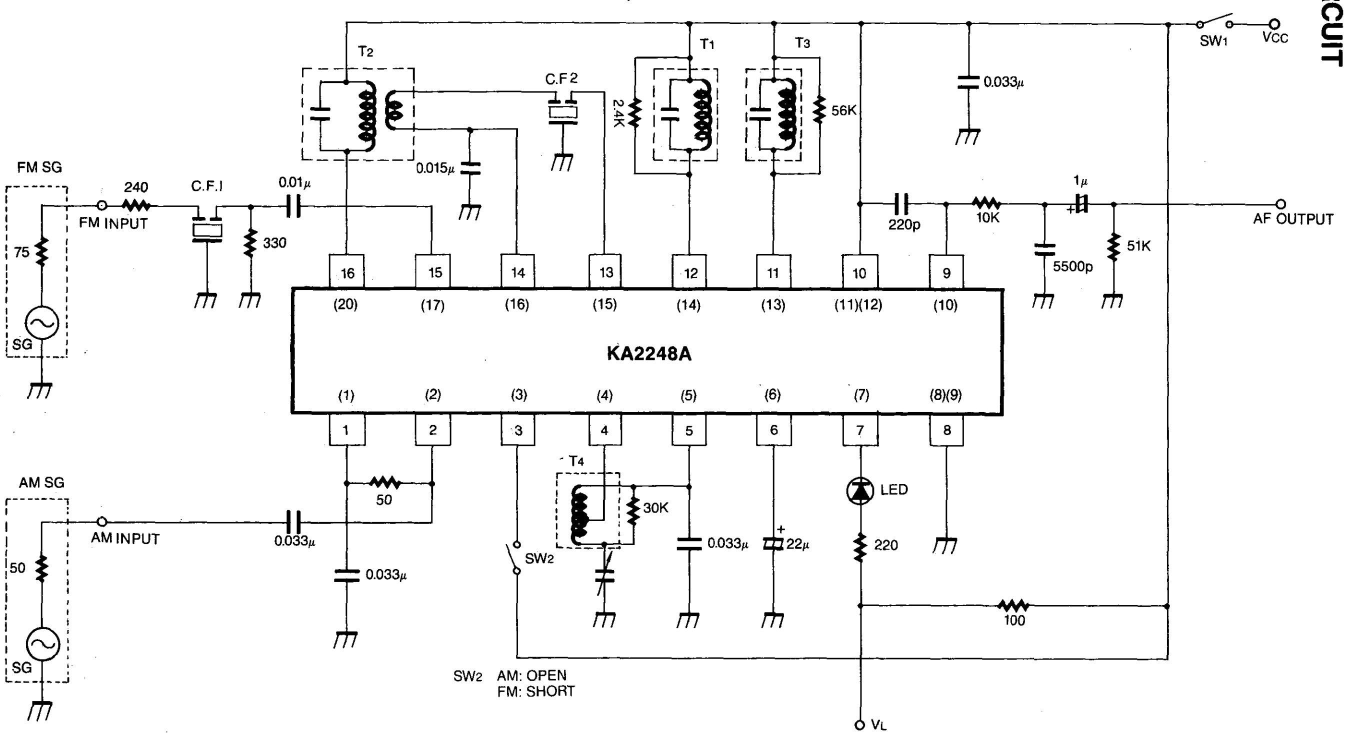
* **FM Section** (f=10.7MHz, fm=1KHz, Δf=22.5KHz)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i =0		8	13	mA
Input Limiting Sensitivity	V_i (lim)	V_i =86dBμ		46	52	dBμ
Detector Voltage	V_o	V_i =86dBμ	60	85	120	mV
Signal to Noise Ratio	S/N	V_i =86dBμ	50	65		dB
Total Harmonic Distortion	THD	V_i =86dBμ		0.1	1.0	%
AM Rejection Ratio	AMR	V_i =86dBμ	30	45		dB
Tuning Indication Voltage	V_L	I_L=1mA		50	58	dBμ
Output Resistance	R_O	f=1KHz		0.7		KΩ

* **AM Section** (f=1MHz, fm=1KHz, 30% Mod)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Current	I_{CC}	V_i =0		3	7	mA
Voltage Gain	A_V	V_i =26dBμ	15	30	50	mV
Detector Voltage	V_O	V_i =60dBμ	35	50	70	mV
Signal to Noise Ratio	S/N	V_i =60dBμ	35	45		dB
Total Harmonic Distortion	THD	V_i =60dBμ		1.0	3.5	%
Oscillator Stop Voltage	Vstop			1.2		V
Output Resistance	R_O	f=1KHz		8.3		KΩ
Tuning Indication Voltage	V_L	I_L=1mA		26	40	dBμ

TEST CIRCUIT

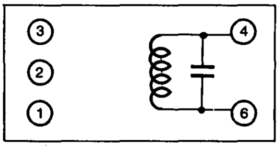


( ): KA2248D

Fig. 2

COIL SPECIFICATIONS (BOTTOM VIEW)

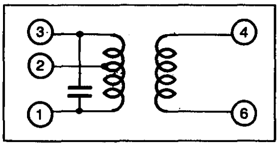
T1 FM IF (DET)



C_O (pF)	f (MHz)	Q_O	TURNS
4-6		4-6	4-6
100	10.7	150	14

Seoul Jupa
0.12mmφ UEW

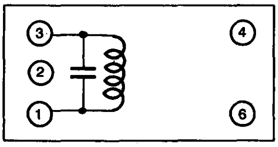
T2 AM IFT (MIX OUT)



C_O (PF)	f (KHz)	Q_O	TURNS		
1-3		1-3	1-2	2-3	4-6
180	455	110	90	62	8

Seoul Jupa
0.07mmφ UEW

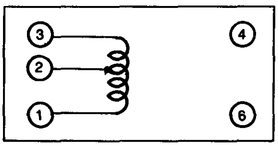
T3 AM IFT (DET)



C_O (pF)	f (KHz)	Q_O	TURNS
1-3		1-3	1-3
180	455	110	152

Seoul Jupa
0.07mmφ UEW

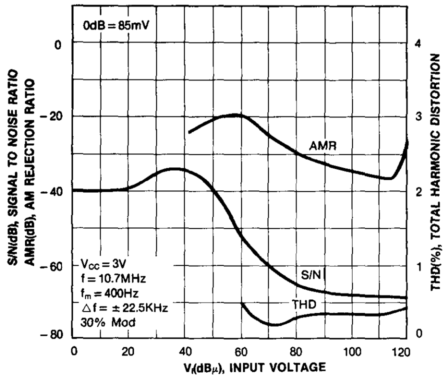
T4 (MW OSC)



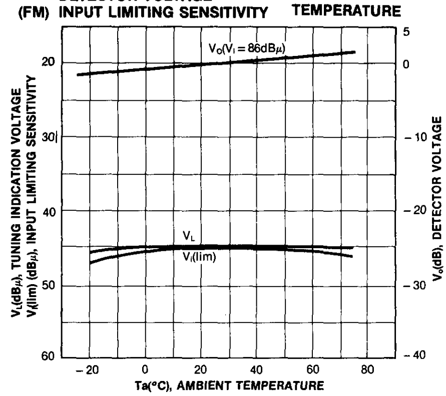
f (KHz)	L (μH)	Q_O	TURNS	
	1-3	1-3	1-2	2-3
796	288	120	13	75

Seoul Jupa
0.08mmφ UEW

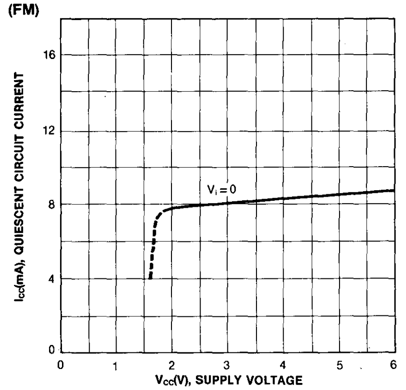
(FM) AM REJECTION RATIO / SIGNAL TO NOISE RATIO / TOTAL HARMONIC DISTORTION -INPUT VOLTAGE



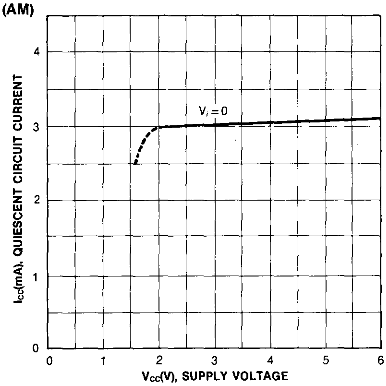
(FM) TUNING INDICATION VOLTAGE / DETECTOR VOLTAGE / INPUT LIMITING SENSITIVITY -AMBIENT TEMPERATURE



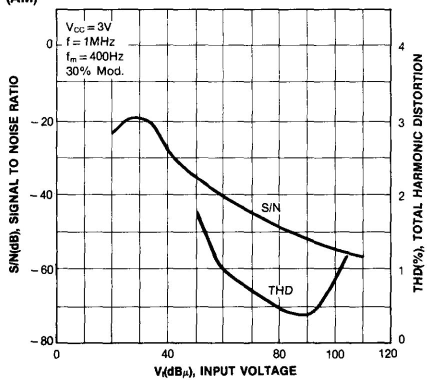
(FM) QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



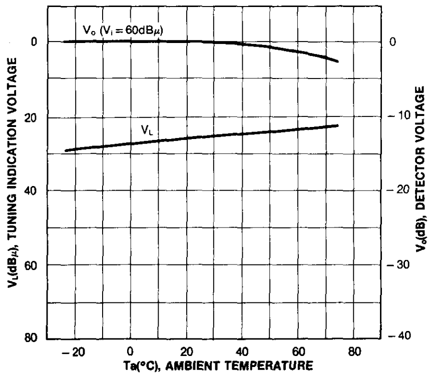
(AM) QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



(AM) SIGNAL TO NOISE RATIO / TOTAL HARMONIC DISTORTION -INPUT VOLTAGE

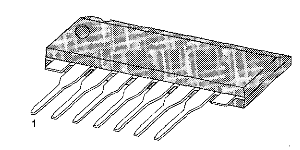


(AM) TUNING INDICATION VOLTAGE / DETECTOR VOLTAGE -AMBIENT TEMPERATURE



FM FRONT END FOR PORTABLE RADIO

The KA2249 is a monolithic integrated circuit designed for the FM front end of portable radios.



FEATURES

- **High frequency amplifier, frequency converter, local oscillator.**
- **Wide operating voltage: V_{CC} = 2V ~ 7V (KA2249)**
  V_{CC} = 2V ~ 5V (KA2249D)
- **Low current consumption: Typ. 2mA (V_{CC} = 4V).**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2249	7 SIP	− 20 ~ + 70°C

SCHEMATIC DIAGRAM

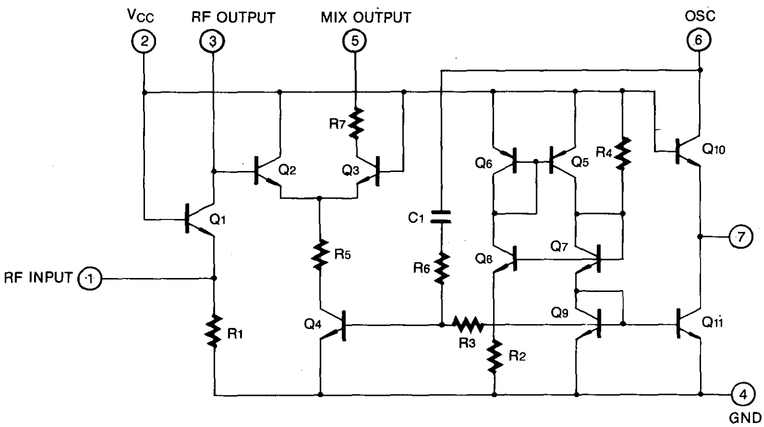


Fig. 1

3

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	7	V
Terminal Voltage	V (3~4)	14	V
	V (5~4)		
	V (6~4)		
Power Dissipation (Ta=70°C)	P_d	30	mW
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−55 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta=25°C, V_{CC}=4V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Fig
Circuit Current	I_{CC}	V_i=0	1.4		3.0	mA	2
Output Voltage	V_O	V_i=70dBμ, 106MHz	30.5		68.5	mV	3
Oscillation Voltage	V_{OSC}	V_{CC}=2V	130			mV	3

TEST CIRCUIT 1

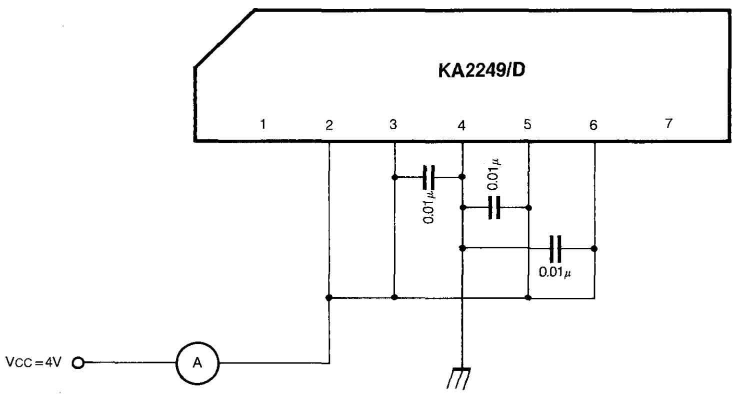


Fig. 2

TEST CIRCUIT 2 (V_o, V_{osc})

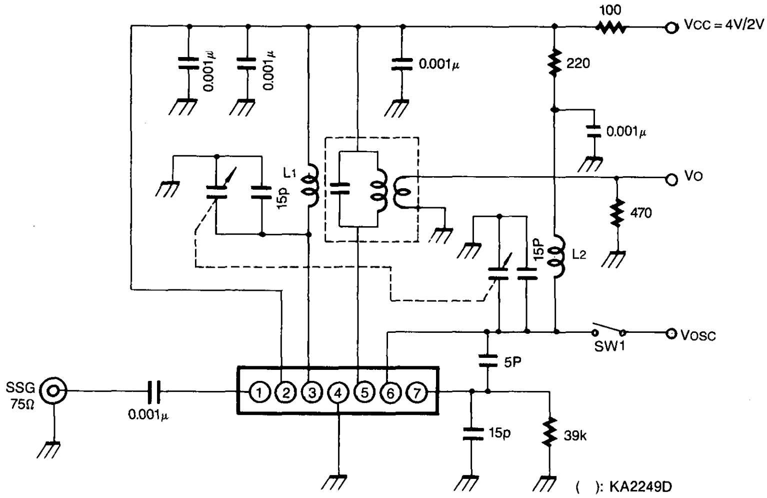
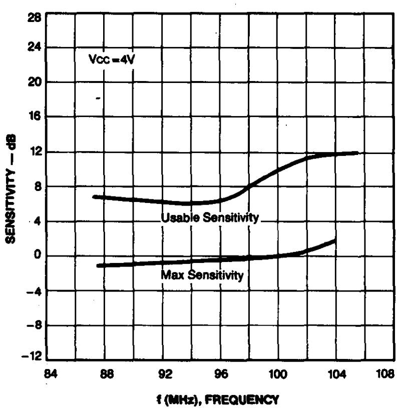
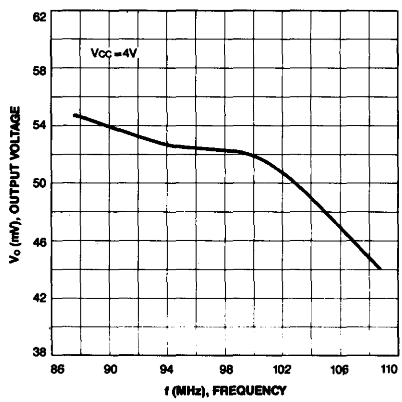


Fig. 3

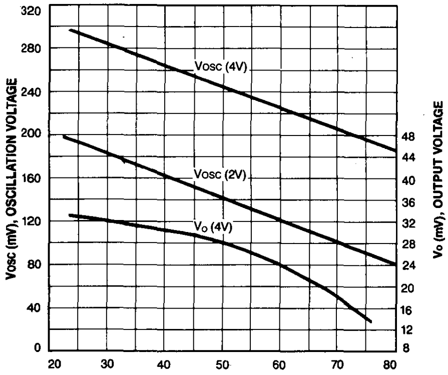
SENSITIVITY — FREQUENCY



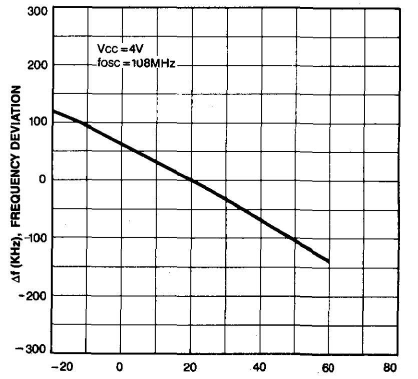
OUTPUT VOLTAGE — FREQUENCY



OSCILLATION VOLTAGE
OUTPUT VOLTAGE — AMBIENT TEMPERATURE



FREQUENCY DEVIATION — AMBIENT TEMPERATURE



APPLICATION CIRCUIT

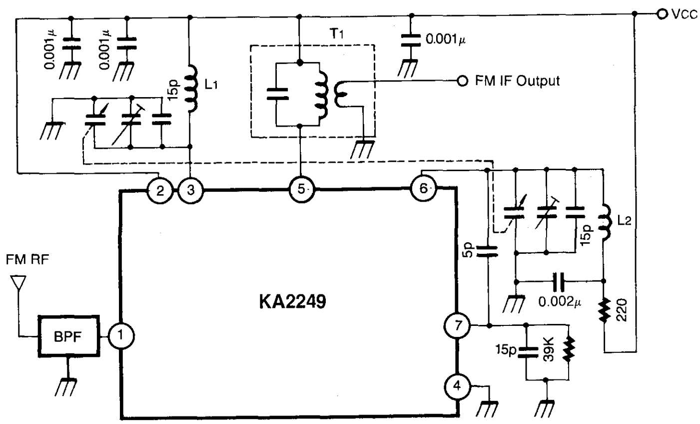
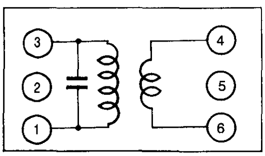


Fig. 4

COIL SPECIFICATIONS

T1 FM IFT



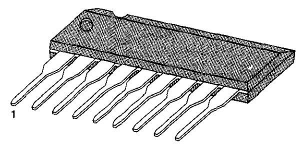
C_O (pF)	f (MHz)	Q_O (%)	TURNS		
			1-3	4-6	
56	10.7	95	12	2	

Seoul Jupa
SJ-015-382
0.1mmϕ UEW

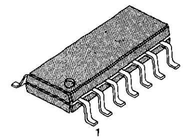
FM FRONT END

The KA22495 is a monolithic integrated circuit designed for the FM front end of portable radio cassettes or music centers.
It consists of RF AMP, local OSC, OSC buffer and mixer.
Compared with conventional types, it is improved in the following characteristics:
1) Low supply voltage.
2) Strong input.
3) Spurious radiation.

9 SIP



14 SOP



FEATURES

- **Wide supply voltage range: $V_{CC}=1.6V \sim 6.0V$**
- **Low local oscillation stop voltage: $V_{CC}=0.9V$ (Typ)**
- **Improved inter-modulation characteristics by double balanced type mixer circuit.**
- Low spurious radiation.
- **Built-in clamping diode in the mixer output stage.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22495	9 SIP	−25 ~ +75°C
KA22495D	14 SOP	

BLOCK DIAGRAM

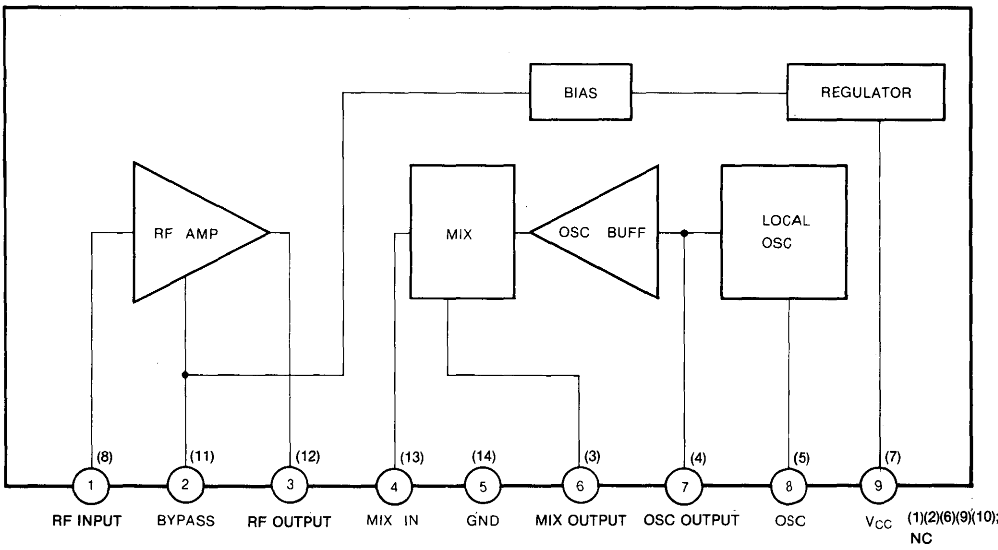


Fig. 1

( ): KA22495D

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol		Value	Unit
Supply Voltage	V_{CC}		8	V
Power Dissipation	P_d	KA22495	600	mW
		KA22495D	300	
Operating Temperature	T_{opr}		−25 ~ +75	°C
Storage Temperature	T_{stg}		−55 ~ +150	°C

*: Derated above Ta = 25°C in the proportion of 4mW/°C.

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 5V, f = 98MHz, fm = 1KHz, △f = ±22.5KHz, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current		I_{CC}	$V_i = 0$		5.2	8.0	mA
−3dB Limiting Sensitivity		V_i (lim)	V_D (V_i = 60dBμ) − 3dB Down		3.0	7.0	dBμ
Conversion Gain		A_{VC}	V_i = 60dBμ	25	31		dB
Usable Sensitivity		Use (Sen)	S/N = 30dB		11		dBμ
Oscillation Voltage		V_{OSC}	f_{OSC} = 108MHz	90	165	250	mV
Oscillation Stop Voltage		V_{STOP}			0.9	1.3	V
Pin 1 Impedance	Parallel Input Resistance	$R_{IP}1$	f = 98MHz		57		Ω
Pin 3 Impedance	Parallel Output Resistance	$R_{OP}3$			25		KΩ
	Parallel Output Capacitance	$C_{OP}3$			2.0		pF
Pin 4 Impedance	Parallel Input Resistance	$R_{IP}4$			2.7		KΩ
	Parallel Input Capacitance	$C_{IP}4$			3.3		pF
Pin 6 Impedance	Parallel Output Resistance	$R_{OP}6$	f = 10.7MHz		100		KΩ
	Parallel Output Capacitance	$C_{OP}6$			4.8		pF

TEST CIRCUIT 1

(I_{CC}, V_i(lim), Use (Sen), A_{VC}, V_{OSC}, V_{STOP})

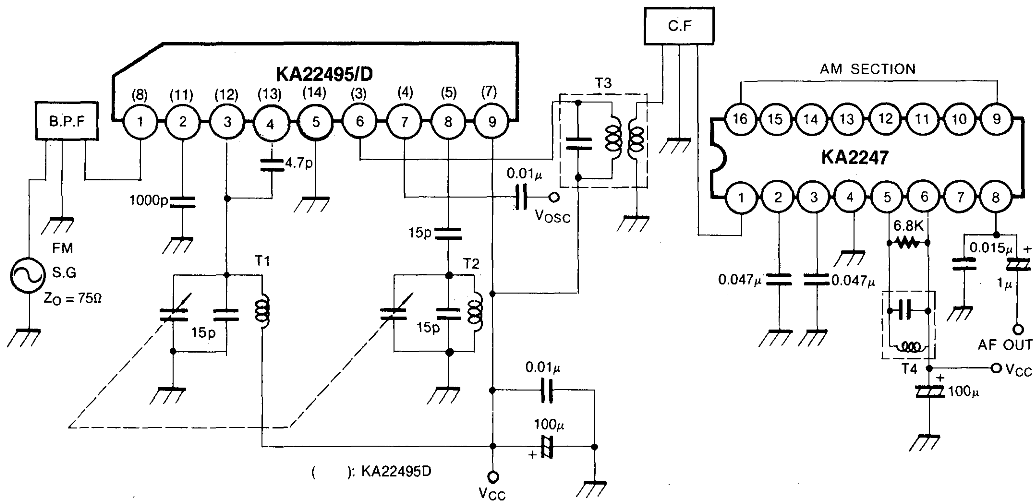


Fig. 2

When using the KA22471 for the IF stage.

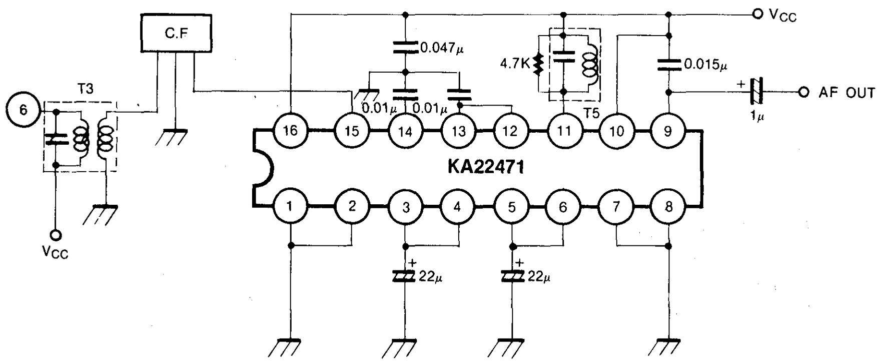


Fig. 3

TEST CIRCUIT 2

1. $R_{iP}1$

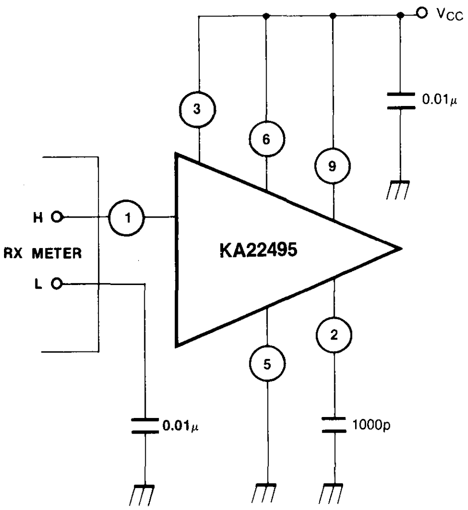


Fig. 4

2. $R_{OP}3$, $C_{OP}3$

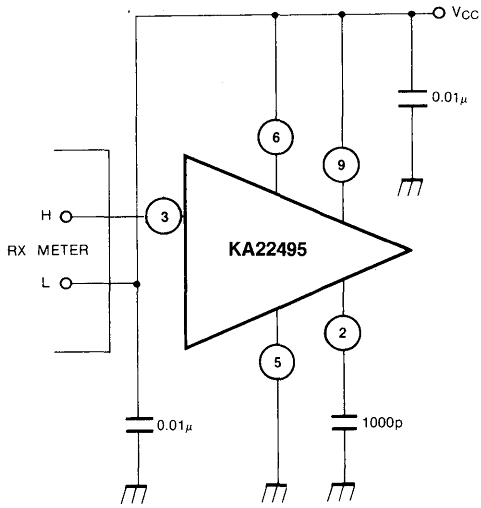


Fig. 5

3. $R_{iP}4$, $C_{iP}4$

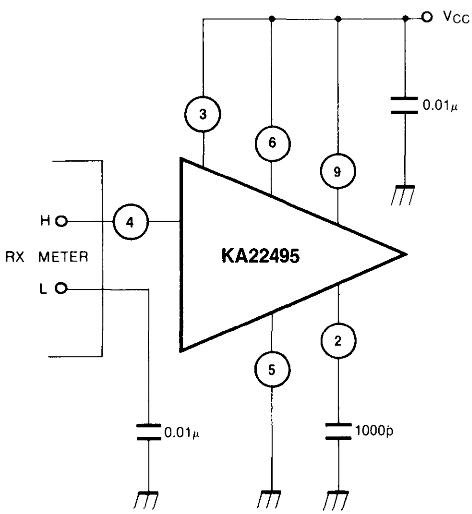


Fig. 6

4. $R_{OP}6$, $C_{OP}6$

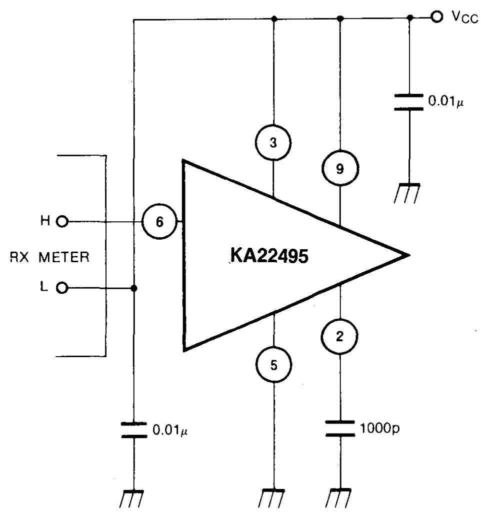
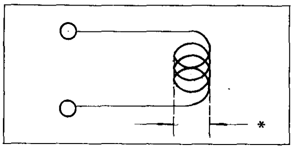


Fig. 7

COIL SPECIFICATIONS (BOTTOM VIEW)

T1 FM RF

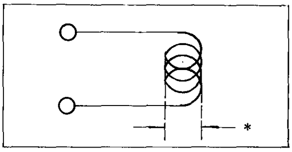


f (MHz)	Q_O	Turns
98	100	4

* In a Diameter of 5.5mm

0.8mm ø UEW

T2 FM OSC

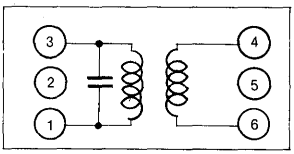


f (MHz)	Q_O	Turns
98	100	3

* In a Diameter of 5.5mm

0.8mm ø UEW

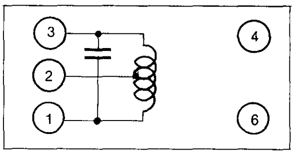
T3 FM IFT



C_O (pF)	f (MHz)	Q_O	Turns	
1 – 3		1 – 3	1 – 3	4 – 6
75	10.7	115	12	1

KOREA TOKO
0.12mm ø UEW

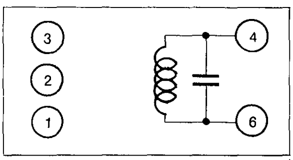
T4 FM IFT (DET)



C_O (pF)	f (MHz)	Q_O	Turns
1 – 3		1 – 3	1 – 3
56	10.7	95	12

KOREA TOKO
0.12mm ø UEW

T5 FM IFT (DET)



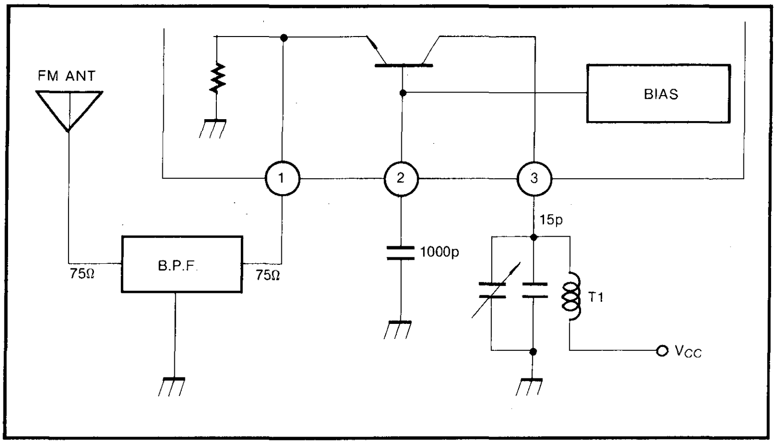
C_O (pF)	f (MHz)	Q_O	Turns
4 – 6		4 – 6	4 – 6
47	10.7	115	14

KOREA TOKO
0.12mm ø UEW

DESCRIPTION

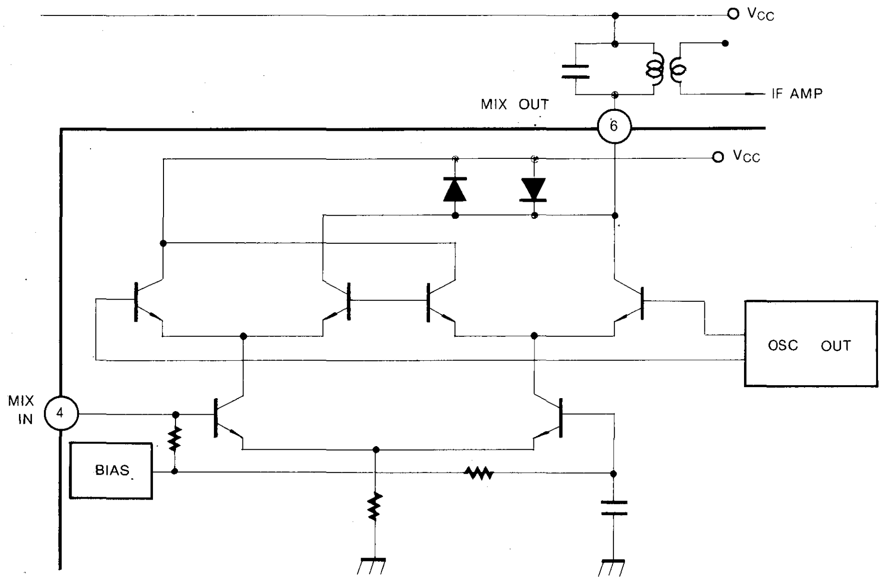
1. RF AMP

The RF AMP is a common base type, so the operating frequency range is improved. The GND of the bypass capacitor (Pin2) should be located closely at Pin 5 (GND). When using the bypass capacitor at V_{CC}-line of Pin 3, we can expect an improvement of the S/N ratio.



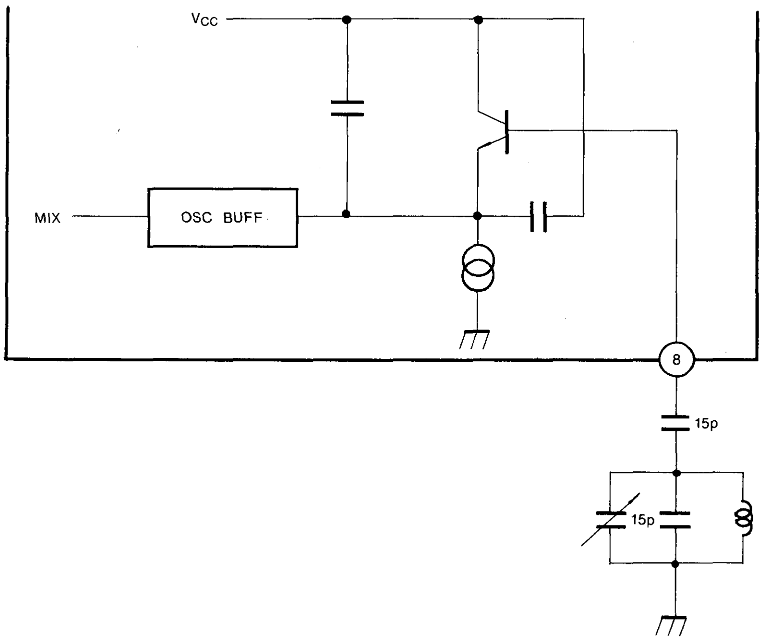
2. MIXER

The mixer stage uses a double balanced type in order to protect the leakage of OSC, spurious radiation. Also, this is built into the limiter in order to improve the strong input characteristic.

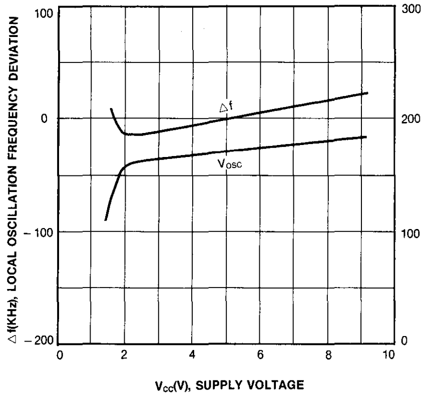


LOCAL OSCILLATION

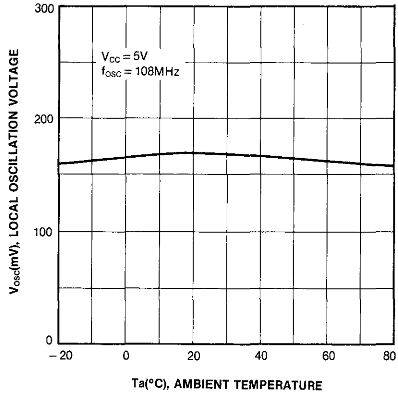
The local oscillator uses a colpitts oscillator for stable oscillation at high frequency. This is built into the OSC buffer in order to stably operate the OSC frequency and OSC voltage at strong input.



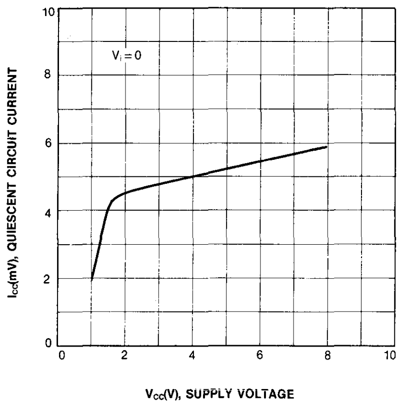
LOCAL OSCILLATION FREQUENCY DEVIATION, LOCAL OSCILLATION VOLTAGE-SUPPLY VOLTAGE



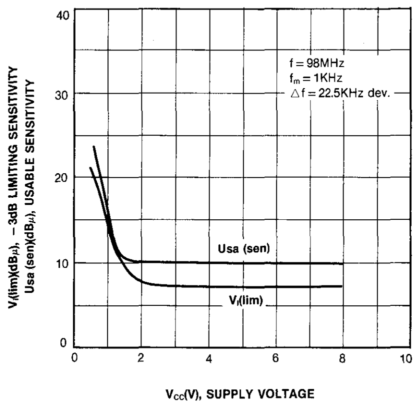
LOCAL OSCILLATION VOLTAGE -AMBIENT TEMPERATURE



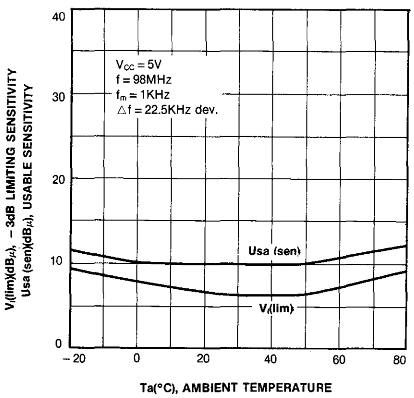
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



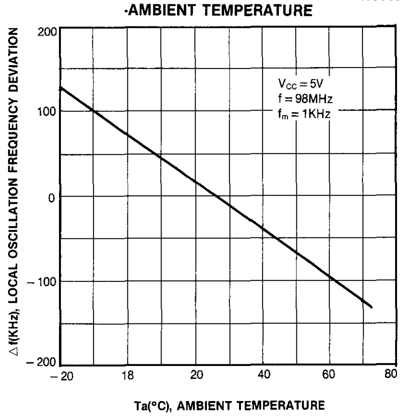
SENSITIVITY-SUPPLY VOLTAGE



SENSITIVITY-AMBIENT TEMPERATURE



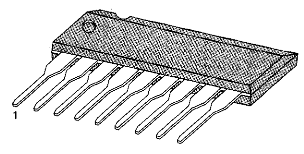
LOCAL OSCILLATION FREQUENCY DEVIATION -AMBIENT TEMPERATURE



FM FRONT END

The KA22496 is a monolithic integrated circuit designed for the FM front end of portable radio cassettes or music centers.
It consists of RF AMP, local OSC, OSC buffer and mixer. Compared with the conventional type, it has improved on the following characteristics:
1) Low supply voltage
2) Strong input
3) Spurious radiation

9 SIP



FEATURES

- **Wide supply voltage range: V_{CC} = 1.6V ~ 6.0V**
- **Low local oscillation stop voltage: V_{CC} = 0.9V (Typ)**
- **Improved inter-modulation characteristics by double balanced type mixer circuit.**
- **Low spurious radiation.**
- **Built-in clampping diode in the mixer output stage.**
- **It can receive the TV Band.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22496	9 SIP	−25 ~ +75°C

BLOCK DIAGRAM

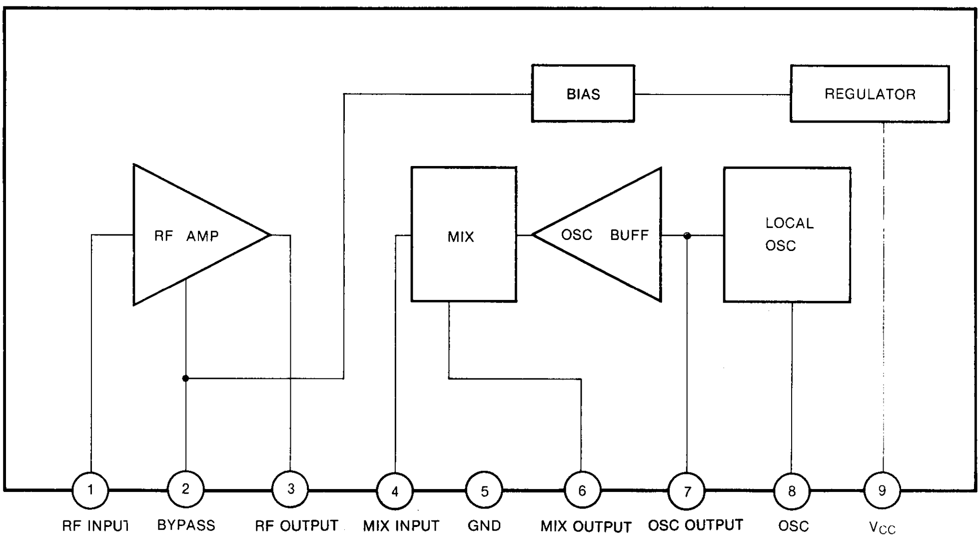


Fig. 1

3

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	8	V
Power Dissipation	P_d*	600	mW
Operating Temperature	T_{opr}	−25 ~ +75	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

*: Derated above Ta = 25°C in the proportion of 4mW/°C.

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 5V, f = 98MHz, fm = 1KHz, △f = ±22.5KHz, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current		I_{CC}	$V_i = 0$		5.2	8.0	mA
−3dB Limiting Sensitivity		V_i (lim)	V_D (V_i = 60dBμ) − 3dB Down		3.0	7.0	dBμ
Conversion Gain		A_{VC}	V_i = 60dBμ	25	31		dB
Usable Sensitivity		Use (Sen)	S/N = 30dB		11		dBμ
Oscillation Voltage		V_{OSC}	f_{osc} = 108MHz	150	230	350	mV
Oscillation Stop Voltage		V_{STOP}			0.9	1.3	V
Pin 1 Impedance	Parallel Input Resistance	$R_{IP}1$	f = 98MHz		57		Ω
Pin 3 Impedance	Parallel Output Resistance	$R_{OP}3$	f = 98MHz		25		KΩ
Pin 3 Impedance	Parallel Output Capacitance	$C_{OP}3$	f = 98MHz		2		pF
Pin 4 Impedance	Parallel Input Resistance	$R_{ip}4$	f = 98MHz		2.7		KΩ
Pin 4 Impedance	Parallel Input Capacitance	$C_{ip}4$	f = 98MHz		3.3		pF
Pin 6 Impedance	Parallel Output Resistance	$R_{OP}6$	f = 10.7MHz		100		KΩ
Pin 6 Impedance	Parallel Output Capacitance	$C_{OP}6$	f = 10.7MHz		4.8		pF

TEST CIRCUIT 1

(I_{CC}, V_i(lim), Use (Sen), A_{VC}, V_{OSC}, V_{STOP})

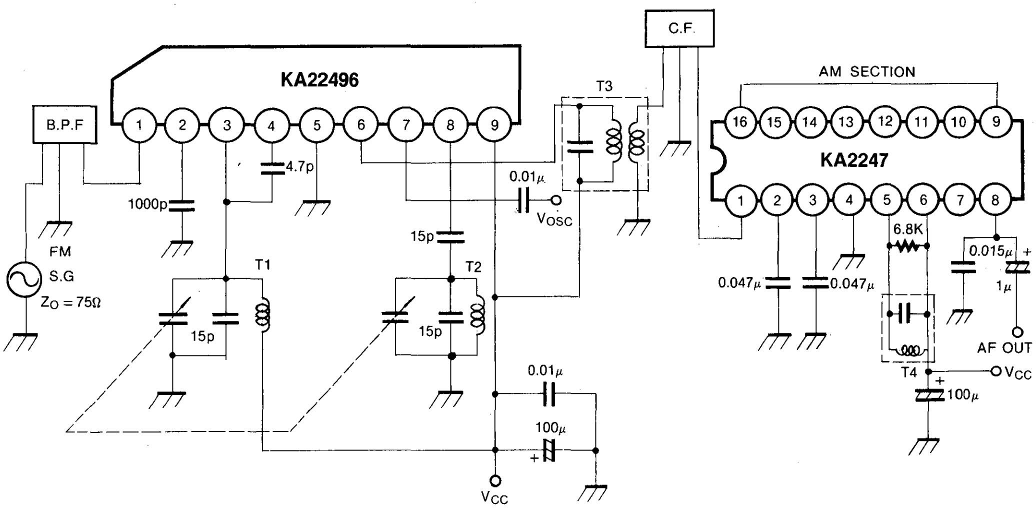


Fig. 2

When using the KA22471 for IF stage.

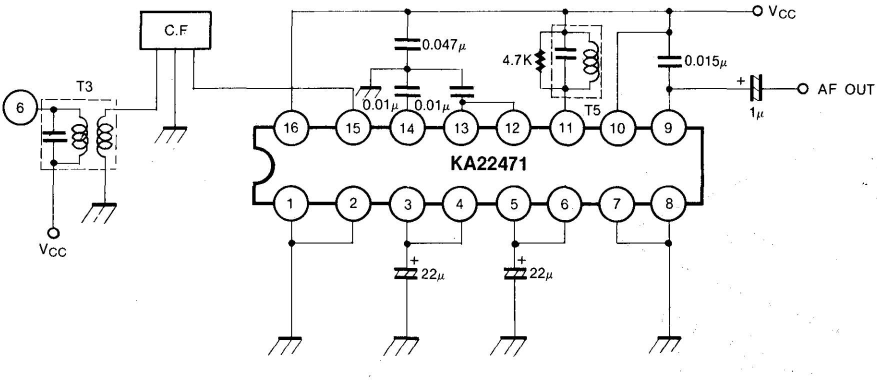


Fig. 3

TEST CIRCUIT 2

1. $R_{iP}1$

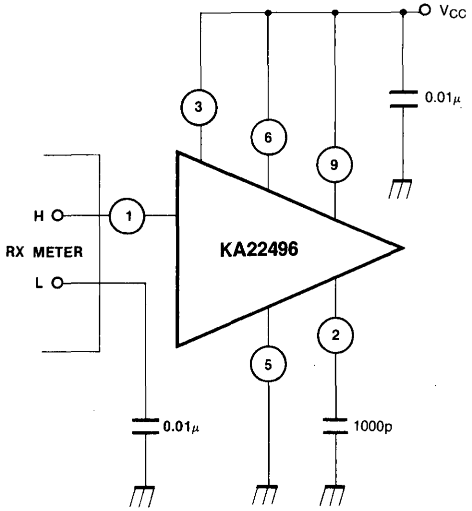


Fig. 4

2. $R_{OP}3$, $C_{OP}3$

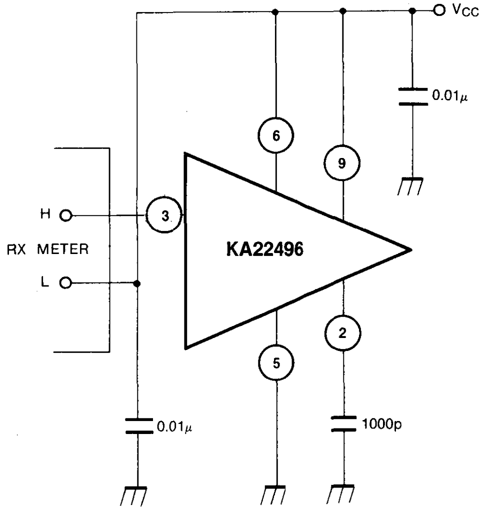


Fig. 5

3. $R_{iP}4$, $C_{iP}4$

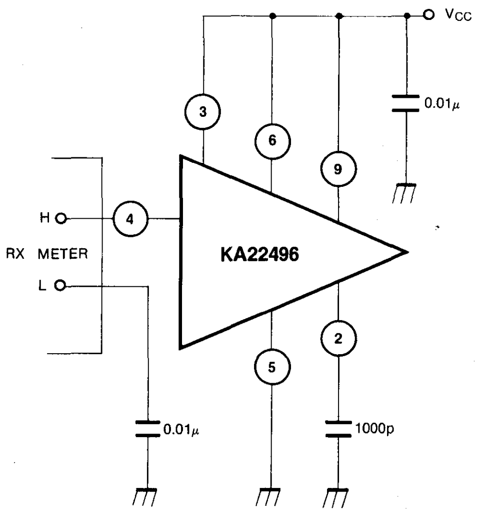


Fig. 6

4. $R_{OP}6$, $C_{OP}6$

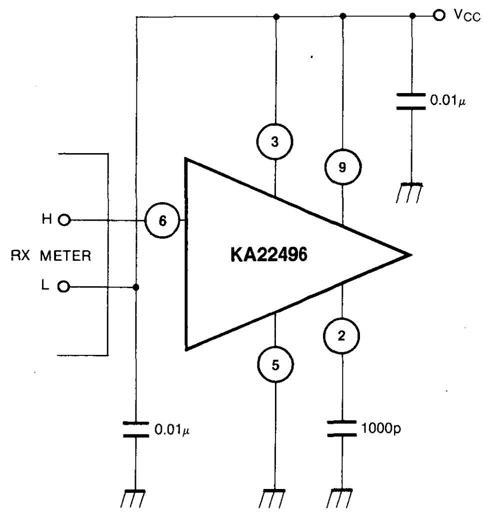
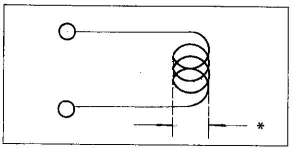


Fig. 7

COIL SPECIFICATION (BOTTOM VIEW)

T1 FM RF

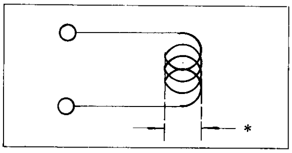


f (MHz)	Q_O	Turns
98	100	4

* In a Diameter: 5.5mm

0.8mm ø UEW

T2 FM OSC

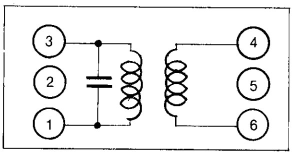


f (MHz)	Q_O	Turns
98	100	3

* In a Diameter: 5.5mm

0.8mm ø UEW

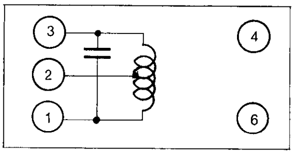
T3 FM IFT



C_O (pF)	f (MHz)	Q_O	Turns	
1 – 3		1 – 3	1 – 3	4 – 6
75	10.7	115	12	1

KOREA TOKO
0.12mm ø UEW

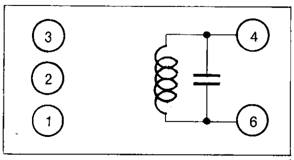
T4 FM IFT (DET)



C_O (pF)	f (MHz)	Q_O	Turns
1 – 3		1 – 3	1 – 3
56	10.7	95	12

KOREA TOKO
0.12mm ø UEW

T5 FM IFT (DET)



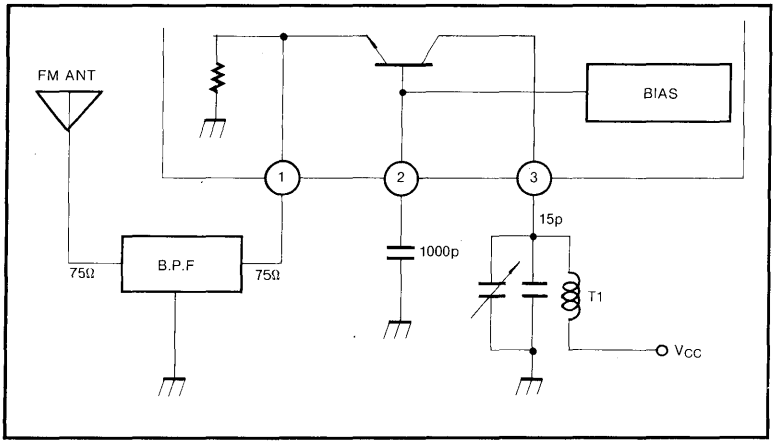
C_O (pF)	f (MHz)	Q_O	Turns
4 – 6		4 – 6	4 – 6
47	10.7	115	14

KOREA TOKO
0.12mm ø UEW

DESCRIPTION

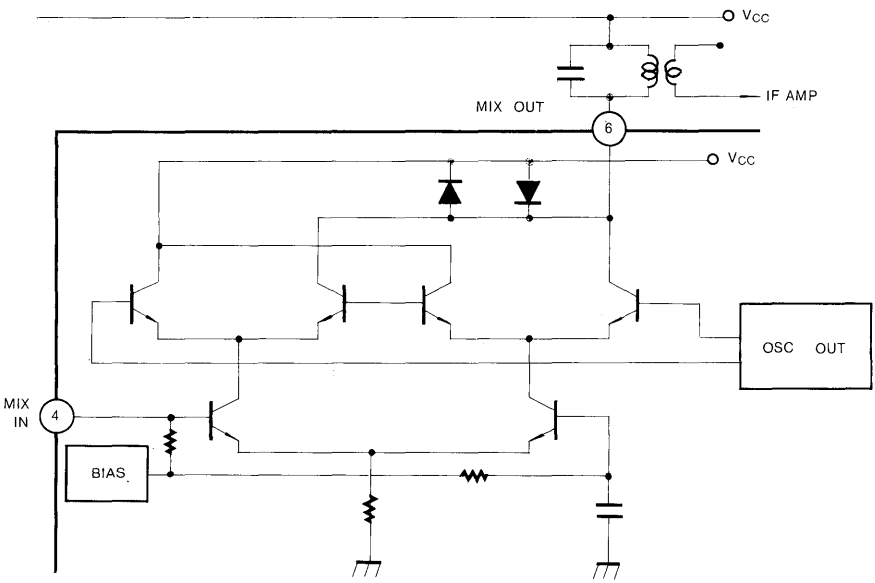
1. RF AMP

The RF AMP is a common base type, so the operating frequency range is improved. The GND of bypass capacitor (Pin2) should be located closely at the pin5 (GND). In case of using the bypass capacitor at V_{CC}-line of pin3, we can expect improvement of S/N ratio.



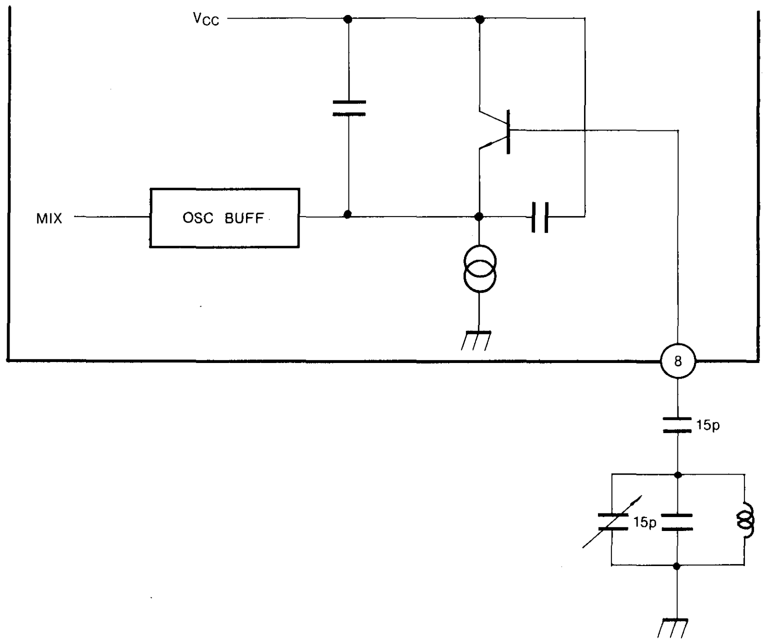
2. MIXER

The MIXER stage used a DOUBLE BALANCED TYPE in order to protect the leakage of OSC and spurious radiation. Also, this is built-in the limiter in order to improve strong input characteristic.

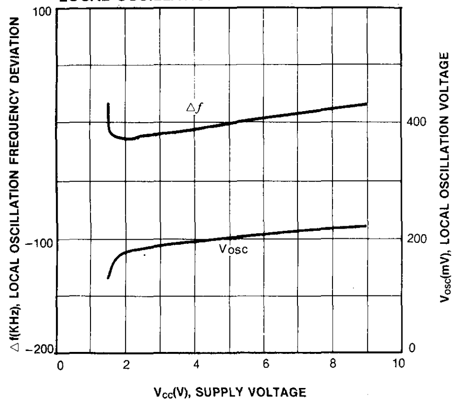


LOCAL OSCILLATION

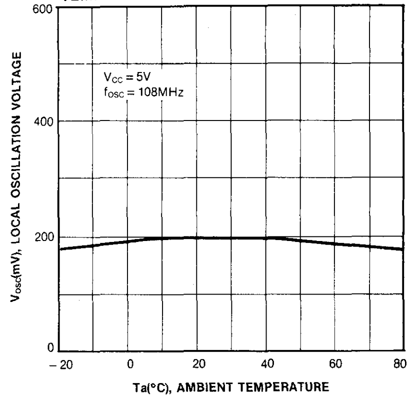
The local oscillator adopted colpitts oscillator for stable oscillation at high frequency. This is built in OSC BUFFER in order to operate stably OSC frequency and OSC voltage at strong input.



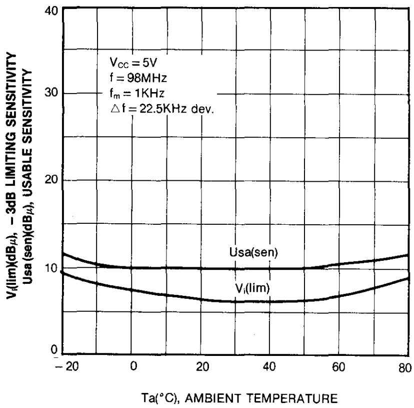
LOCAL OSCILLATION FREQUENCY DEVIATION, LOCAL OSCILLATION VOLTAGE-SUPPLY VOLTAGE



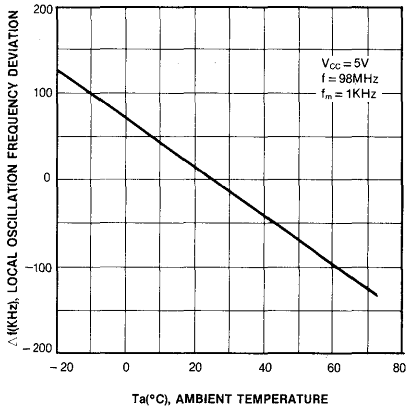
LOCAL OSCILLATION VOLTAGE-AMBIENT TEMPERATURE



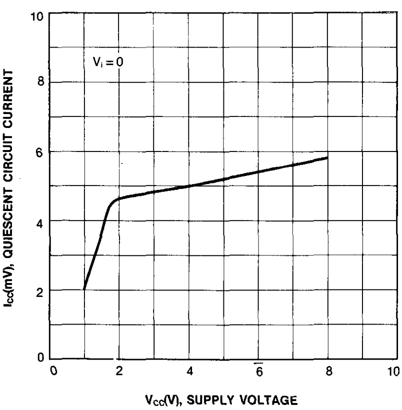
SENSITIVITY-AMBIENT TEMPERATURE



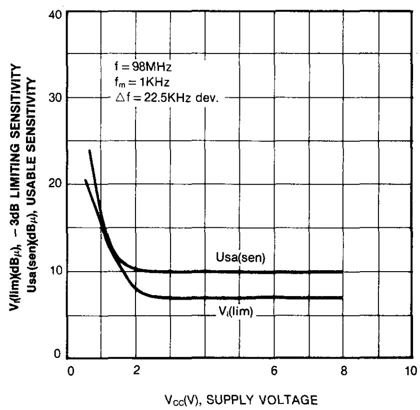
LOCAL OSCILLATION FREQUENCY DEVIATION -AMBIENT TEMPERATURE



QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



SENSITIVITY-SUPPLY VOLTAGE



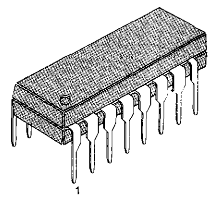
FM STEREO MULTIPLEX DECODER

The KA2261 is a monolithic integrated circuit consisting of a phase locked loop FM stereo demodulator. It was designed for use in car stereos, cassette recorders and other equipment.

FEATURES

- **A PLL is used for high multiplexing performance.**
- **Wide operating supply voltage range (3V ~ 14V).**
- **Low quiescent circuit current (I_{CC} = 8.5mA, Typ).**
- **High SCA rejection ratio.**
- **High channel separation (45dB, Typ) and can be controlled by an external resistor.**
- **Built-in VCO disable and monaural muting circuits.**
- **Built-in stereo indicator lamp drive circuit.**

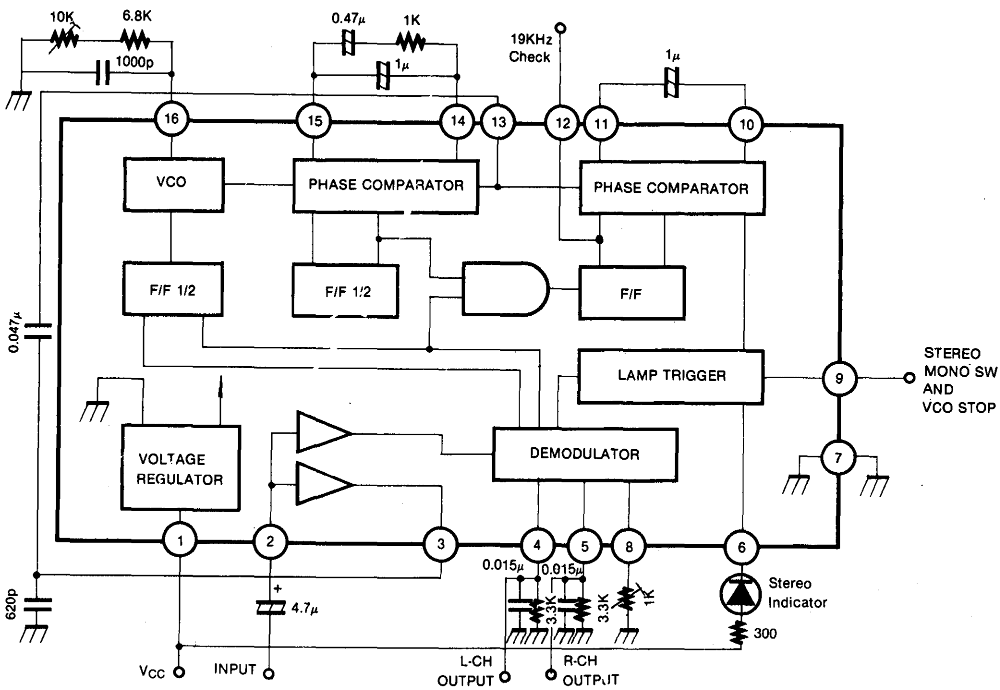
16 DIP



ORDERING INFORMATION

Device	Package	Operating Temperature
KA2261	16 DIP	− 20 ~ + 70°C

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Lamp Current	I_L	40	mA
Power Dissipation	P_d	400	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temepraturе	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=6V, f=1KHz, R_L=3.3KΩ, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current		I_{CC}	V_i=o		8.5	12	mA
Channel Separation		Sep	V_i=100mV, L+R=90% P=10%, f=1KHz	35	45		dB
Total Harmonic Distortion	Mono	THD 1	V_i=100mV		0.2		%
	Stereo	THD 2	L+R=90mV, P=10mV		0.7		%
Output Voltage		V_O	V_i=100mV, f=1KHz	66	85	115	mV
Channel Balance		CB	V_i=100mV, f=1KHz		0.5	1.5	dB
Lamp on Level		V_L(on)	L+R=90%, P=10%		65		mV
Lamp Hysteresis		HY			3.5	6.0	dB
Maximum Input Level		V_i(max)	THD=2%		450		mV
SCA Rejection Ratio		SCA R_{ej}	L+R=90%, P=10%		70		dB
Signal to Noise Ratio		S/N	V_i=100mV, f=1KHz		75		dB
Carrier Leak		CL	V_i=100mV, L+R=90% P=10%		32		dB
Capture Range		CR	V_i=100mV, L+R=90% P=10%		±3		%
Input Impedance		R_i		15	20		KΩ

TEST CIRCUIT

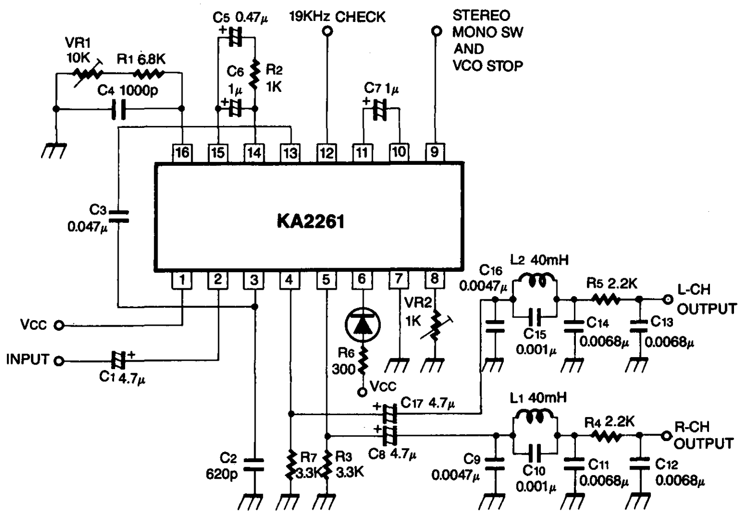
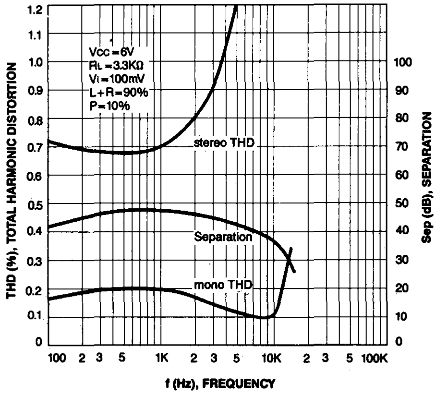
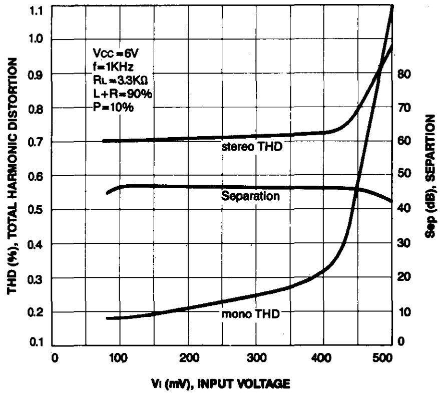


Fig. 2

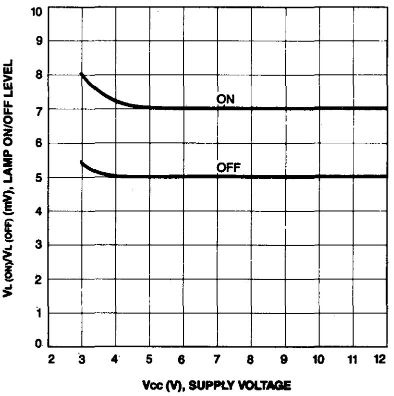
SEPARATION / TOTAL HARMONIC DISTORTION —FREQUENCY



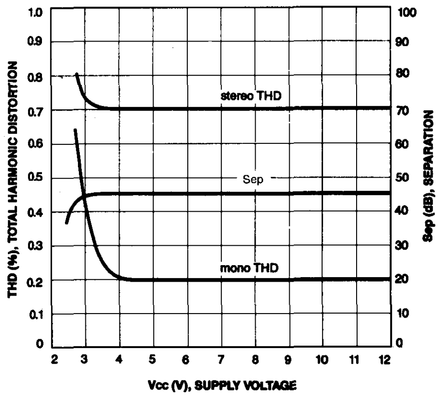
SEPARATION / TOTAL HARMONIC DISTORTION — INPUT VOLTAGE



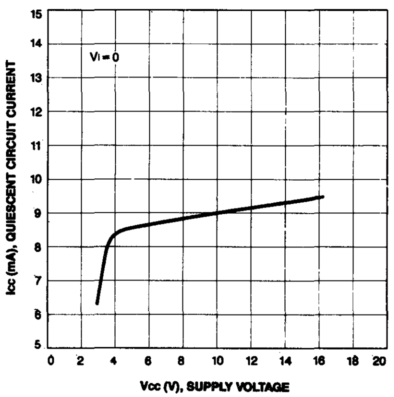
LAMP ON/OFF LEVEL-SUPPLY VOLTAGE



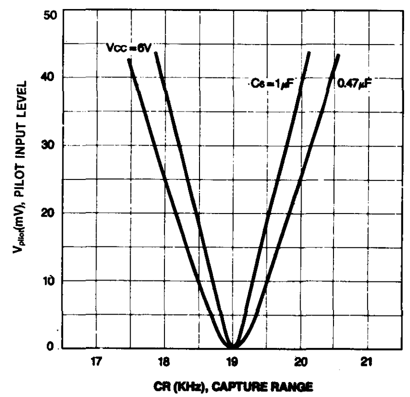
SEPARATION / TOTAL HARMONIC DISTORTION — SUPPLY VOLTAGE



QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE

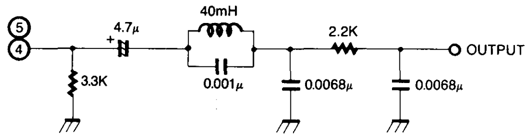


CAPTURE RANGE



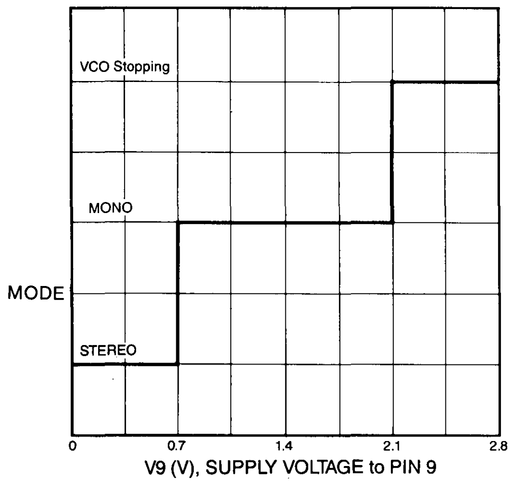
External Components (Refer to Test Circuit)

1. Input coupling capacitor (Pin 2)
   The recommended value is 4.7μF. If smaller values than 4.7μF are used, low frequency separation will worsen, and if larger values are used, the DC operating point will require time for stabilization.
2. Demodulator output (Pin 4, 5)
   These components provide R and L channel output load circuits. The recommended circuits are follows:



3. Separation control (Pin 8)
   This component is a variable resistor used to adjust the out signal separation.
4. Low pass filter (Pins 10, 11)
   This capacitor is used to filter the 19KHz signal detected by the phase comparator. The recommended value is 1μF. If made too small, the lamp may light improvely when a large mono input signal or external noise is received, too large a capacitance value will take more time to switch between mono and stereo modes.
5. Preamplifier output capacitor (Pins 3, 13)
   This capacitor coupled preamplified with phase comparator. The recommanded value is 0.047μF.
6. Phase compensation capacitor (Pin 3, GND)
   This capacitor is prepared in order to compensate the phase advanced.
7. Loop filter (Pins 14, 15)
   This is the low pass filter for the PLL, which is determined the capture range. The recommended value as follows:
   $V_i \leq 250mV$ $C_{14\text{-}15} = 0.47\mu F$
   $V_i \geq 250mV$ $C_{14\text{-}15} = 1\mu F$
8. Control of Pin 9
   Function of Pin 9 is a change-over of stereo/mono and VCO stopping.

SCHEMATIC DIAGRAM of PIN 9 CONTROL



9. VCO network (Pin 16)
   Since the VCO has a negative temperature coefficient, the RC network compensates by using a polyester film capacitor and a resistor.

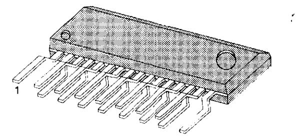
FM STEREO MULTIPLEX DECODER FOR CAR STEREOS

The KA2262 is a multiplex IC for FM car stereos, and it has the following 2 functions through its utilization of the IF meter output voltage:

1. Stereo noise control (SNC) under which the noise particular on the FM stereo unit in the weak electric field is reduced smoothly.
2. High-cut control (HCC) under which the high frequency is smoothly attenuated.

   In addition, the KA2262 can be, due to its low distortion factor, an IC for multiplex stereo demodulators which is appropriate for car component stereo units.

16 ZSIP



FUNCTIONS

- Stereo noise control (SNC Terminal).
- High-cut control (HCC Terminal).
- Stereo/Monaural automatic conversion.
- Stoppage of VCO oscillation.
- With separation control terminal.

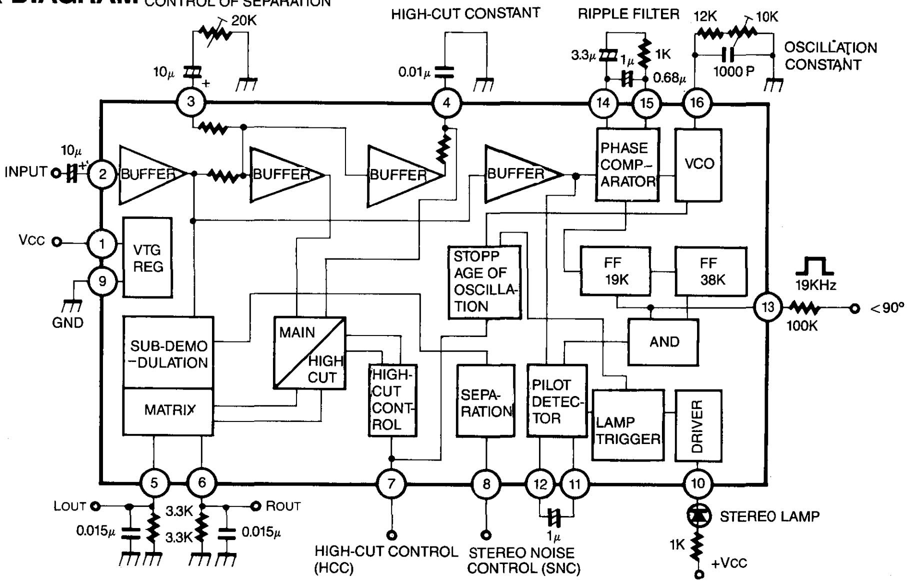
FEATURES

- **Low distortion (0.05%: Typ).**
- **Good ripple rejection (35dB: Typ).**
- **Wide operating supply voltage range (6.5V ~ 14V).**
- **The space factor is advantageous because of the ZSIP.**
- **High channel separation (50dB: Typ).**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2262	16 ZSIP	−20 ~ +70°C
KA2262G	PELLET	

BLOCK DIAGRAM



Note: There exists a possibility of change on the VCO Oscillation Constant.

Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

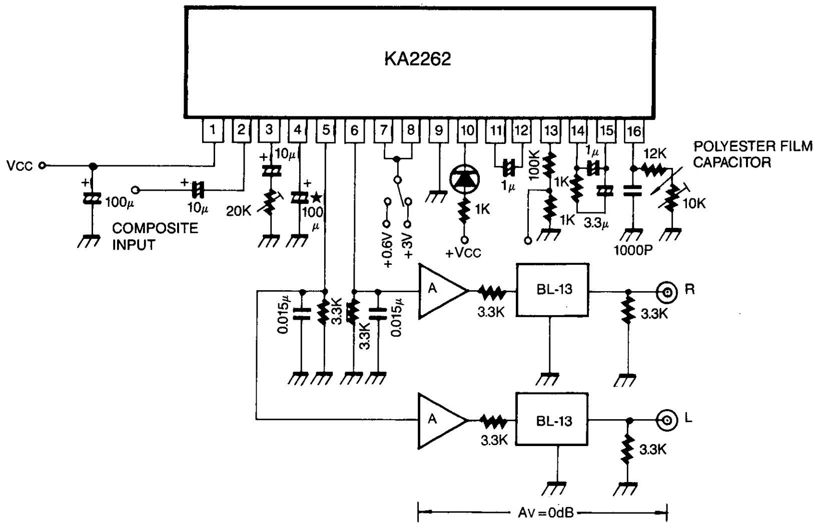
Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Lamp Current	I_L	40	mA
Power Dissipation	Pd ($T_a \leqq 45°C$)	520	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =10V, f=1KHz, R_L =3.3KΩ, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current		I_{CC}	V_i =0		21	27	mA
Channel Separation		Sep	V_i =300mV, L+R=90%, P=10%	40	50		dB
Total Harmonic Distortion	Mono	THD1	V_i =300mV		0.05	0.2	%
	Stereo	THD2	V_i =300mV, L+R=90%, P=10%		0.05	0.2	%
Output Voltage		V_O	V_i =300mV, Sub	140	200	280	mV
Channel Balance		CB	V_i =300mV		0.5	1.5	dB
Lamp on Level		V_L (on)	L+R=90%, P=10%	60	85	120	mV
Lamp Hysteresis		HY			3	6	dB
Maximum Input Level		V_I (max)	L+R=90%, P=10%, THD=1%	700	800		mV
SCA Rejection Ratio		SCA Rej	L+R=90%, P=10%		80		dB
Signal to Noise Ratio		S/N	V_i =300mV	70	78		dB
Ripple Rejection		RR			35		dB
Capture Range		CR	P=30mV		±3		%
Input Impedance		Ri			20		KΩ
SNC Output Attenuation		SNC (ATT)	V_8 =0.6V, L−R=90%, P=10%	−8.5	−3.0	−0.3	dB
SNC Output Voltage		SNC V_O	V_8 =0.1V, L−R=90%, P=10%			5	mV
HCC Output Attenuation		$HCC_{(ATT)}$ 1	V_7 =0.6V, L+R=90%, P=10%	−15.0	−6.0	−0.5	dB
		$HCC_{(ATT)}$ 2	V_7 =1V, L+R=90%, P=10%	−2.0		0	dB

TEST CIRCUIT



★:100μF connected between pin 4 and GND is for measurement of SNC output voltage, HCC output voltage.

Fig. 2

SNC (STEREO NOISE CONTROL) AND HCC (HIGH-CUT CONTROL)

In order to ameliorate the signal to noise (S/N) ratio in the weak electric field, both SNC and HCC Terminals are installed in the KA2262. When the SNC Terminal is controlled, the noise particular on the stereo reception in the weak electric field can be decreased.

By using the HCC Terminal, the FM noise at the high-frequency level can be reduced, resulting in the effective improvement of the S/N ratio. (Refer to Fig. 4)

As shown in Fig. 4 the deterioration of the S/N ratio is larger by approx. 21.7dB in the stereo mode than in the monaural mode, as far as the weak electric field is concerned.

In general, the noise is considerably harsh (offensive) to the ear if the S/N ratio is lower than 30~40dB. So, the Areas "A", "B" and "C" have, in this study, been prepared, as shown in Fig. 4, according to the intensity of the electric field on a provisional criteria of 30~40dB (S/N ratio).

The procedures of setting SNC and HCC are described below on the presumption of SNC operation in Area "A" and of HCC operation in Area "B".

Regarding the Area "C", a light level of muting is made at the IF stage.

1. SNC (Stereo Noise Control)

The S/N ratio of stereo reception is worse by 21.7dB than with the monaural reception. However, such an S/N ratio can be ameliorated if the separation of the stereo reception is changed. The effect of S/N-ratio amelioration can become significant when the separation is less the approx. 20dB. The relationships between this separation and the degree of S/N improvement are shown in Fig. 5.

Under the SNC utilized in the KA2262, the S/N ratio improvement is accomplished in the weak electric field by the alteration of the separation mentioned above. In detail, the separation of stereo reception is controlled by changing the demodulation level of this sub-signal.

If the level output of the signal meter in the IF stage is utilized as the source of control signal, the S/N ratio can be made lower than approx. 40dB in the Area "A" Shown in Fig. 4.

In the case of an idealistic S/N-ratio improvement, a gradual conversion should be made from the stereo mode to monaural mode so that the S/N ratio may be constant from the point of stereo S/N ratio, 40dB, to that of monaural S/N ratio, 40dB. The procedures of setting the control level will be described later.

In Fig. 6 are shown the relationships between the voltage applied to Pin 8 (SNC Terminal) of the KA2262 and the characteristics of separation (SNC characteristics).

Since Pin 8 is positioned at the base of common-collector PNP transistor, the unit is set in the stereo mode if Pin 8 is open. In contrast, it is set in the monaural mode when Pin 8 is grounded.

The control through the use of SNC Terminal is available only when the stereo indicator lights on by the locking to the pilot signal.

Since the SNC control current is less large, the constant of the outer circuit can be set at a large amount, resulting in no influence on the meter output circuit of the IF stage. Thus, the designing work of this circuit can easily be made.

2. Design of Outer Circuit for SNC Characteristics (Setting Charactristics through Drawings)

The SNC characteristics can be set in order to change the separation smoothly from stereo mode to monaural mode in Area A shown in Fig. 4. The following procedures are preferable for such a setting:

Relationships between separation and improvement of the S/N ratio .... Fig. 5

Relationships between the voltage applied to the SNC terminal and separation characteristics .... Fig. 6

If both the "graph" showing the relationships between signal meter output (in IF stage) and antenna input and the "graph" which shows the relationships between antenna input and S/N ratio improvement characteristics are obtained by using Figs. 5 and 6, the relationships between the antenna input and S/N ratio improvement characteristics can be obtained through the preparation of drawings.

Also, the characteristics of SNC-terminal application voltage can adversely be obtained from the S/N characteristics which are desirable for the user.

An example of drawing preparation is shown in Fig. 8. In order to simplify the recognition, all of "SNC characteristics," "IF meter characteristics" and "stereo S/N-ratio characteristics" are made similar to one another with straight lines. The example of the preparation is as follows:

The stereo S/N-ratio improvement characteristics are obtained from the SNC characteristics. In the chart diagram, (a) of the 2nd sector is a base for the SNC characteristics. Through the projection to the 3rd sector from (a), the separation is 20dB at Point "1", while the level of the S/N-ratio improvement is 1dB.

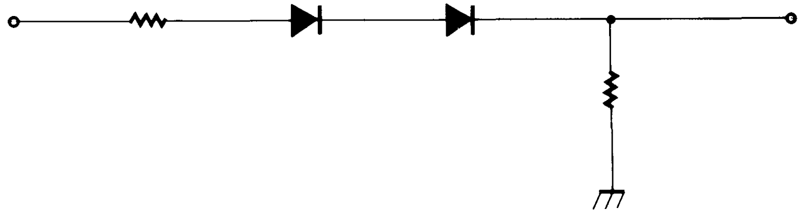
When projection is made from the 1st sector to the 4th sector, the point where the S/N ratio is improved by 1dB from the line of stereo S/N ratio in the 4th sector corresponds with Poin 1.

Similarly, Point 2 on the SNC characteristics in the 2nd sector corresponds with Point 2 in the 4th sector as well as Point 3 in the 2nd sector with Point 3 in the 4th sector. Thus, the individual S/N-ratio improvement characteristics can be obtained.

Similarly to the above, the characteristics (b) of the 2nd sector is projected like characteristics (b) of the 4th sector, while the characteristics (c) of the 2nd sector is projected like characteristics (c) of the 4th sector. Thus, the drawing of improvement characteristics can be prepared.

As a result of preparation of drawing, the S/N-ratio improvement characteristics of Fig. (b) in the 4th sector is ideal. However, the SNC characteristics corresponding there with becomes the characteristics shown with Fig. (b) of the 2nd sector. It is difficult to realize such characteristics.

From the viewpoint of practical characteristics, the one like Fig. (c) seems to be appropriate. The SNC characteristics shown in Fig. (c) are obtained by the use of both the shifting operation made by 2 diodes and a 1/2 bleeder.



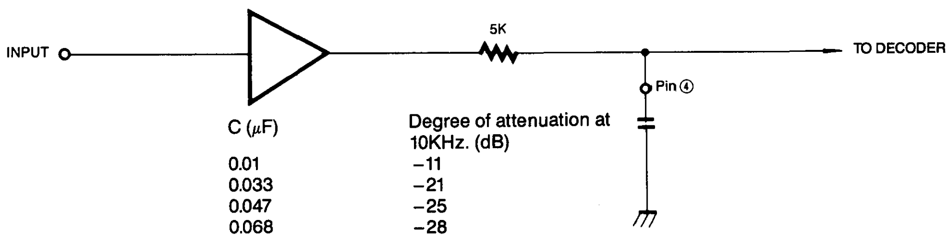
3. HCC (High-Cut Control)

In Area B where the S/N ratio is lower than 40dB even in the monaural mode, the S/N ratio can be improved from the acoustic standpoint if the leel of high frequency (at about 7KHz) is lowered.

When the signal meter output voltage of the IF stage is given to the HCC Terminal (Pin 7) of KA2262, a smooth high-level attenuation (high-cut control) can be made according to the meter's voltage.

In Fig. 9, are shown the frequency characteristics (monaural) of the MPX output caused from the voltage applied to Pin 7. The frequency characteristics obtained when 100% high cut is made can freely be set by the 4-pin outer capacitor.

The equivalent circuit at this stage is determined by the time constant of "5KΩ" and "C", as shown in the following diagram. By the approx. amount of C, the degree of attenuation at 10KHz is as follows:



C (μF)	Degree of attenuation at 10KHz. (dB)
0.01	−11
0.033	−21
0.047	−25
0.068	−28

The relationships (HCC characteristics) between Pin 7's applied voltage and high-cut rate (%) are shown in Fig. 10.

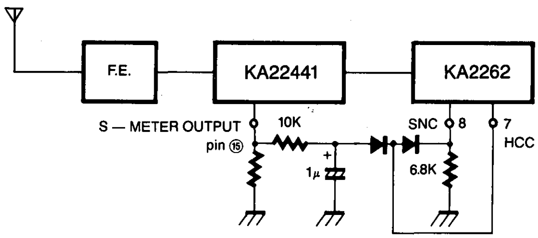
When the characteristics of the IF meter output voltage and the S/N-ratio characteristics of Area B (shown in Fig. 4) are obtained in addition to Fig. 10, the characteristics of the S/N-ratio improvement which is implemented by HCC can be drawn.

The output of meter of IF amplifier IC used for quadrature detection is usually the one shown in Fig. 4. (Fig. 3 shows the data of the KA22441). Thus, the HCC characteristics (Fig. 10) are set so that the Area B may be ameliorated when the output mentioned above is directly connected with the HCC Terminal (Pin 7) of the KA2262.

Being very small similarly to the control current of Pin 8, such a control current of Pin 7 gives no influence to the output of the meter.

4. SNC/HCC Connectio Circuit when they are connected with the IF Stage

In Fig. 3, is shown an example of S/N-ratio characteristics caused from the antenna input when SNC and HCC are connected with the IF stage through the outer circuit shown below.



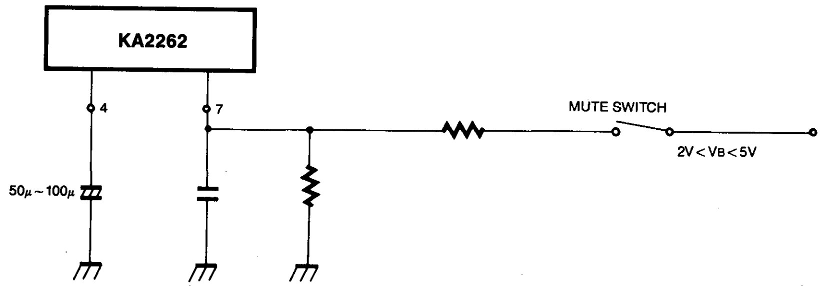
5. Improvement of S/N Ratio in Area C shown in Fig. 3

In Area C shown in Fig. 3, the S/N ratio is further worsened. Its improvement should be performed by the IF muting. The KA22441 can be enumerated as an IC which can vary ghi IF muting linearly. The S/N-ratio improvement effect of the KA2262 can further be enhanced if the KA2262 is used together with the KA22441.

6. Use of HCC Terminal for the Muting Functioin

In the event that the removal of high-frequency noise is not required when the HCC Terminal is used for a home stereo unit, the muting can be accomplished by approx. 37dB if this HCC function is utilized for the muting function.

If the time constant is applied on the control of Pin 7, the "Fade in" and "Fade Out" operations can be performed on the muting. The muting can be performed without offensiveness to the ear as alien factors such as shock noise, are removed thereby.



7. Stop Method of VCO

When a voltage higher than 7V is applied to the HCC Terminal (Pin 7), the oscillation of VCO can be discontinued, resulting in the monaural mode. At this stage, both the SNC and HCC are in the OFF status.

The relationships between the incoming current and Pin 7 applied voltage are shown in Fig. 11.

8. Separation Control Terminal

The control of separation is implemented by controlling the level of the main signal.

The range of separation of the controllable input compost signal (Sub-signal/main signal ratio) is approx. the one shown in the following formula:

$$m = \frac{\text{Sub signal level}}{\text{Main signal level}} \qquad 0.7 < m < 1.25 \text{ (At peak level)}$$

AN EXAMPLE OF S/N IMPROVEMENT IN A WEAK ELECTRIC FIELD MADE BY THE KA2262 SYSTEM

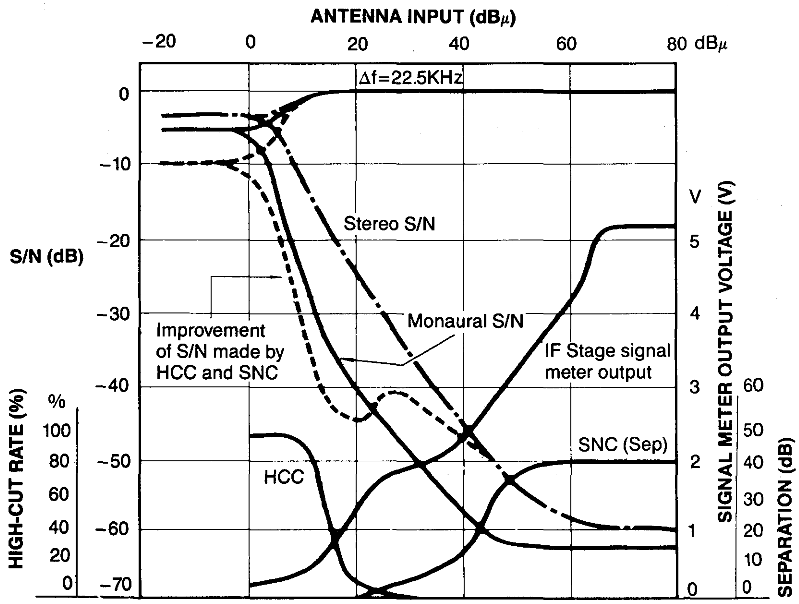


Fig. 3

3

CHART DIAGRAM USED FOR OBTAINING STEREO CHARACTERISTICS FROM SNC CHARACTERISTICS

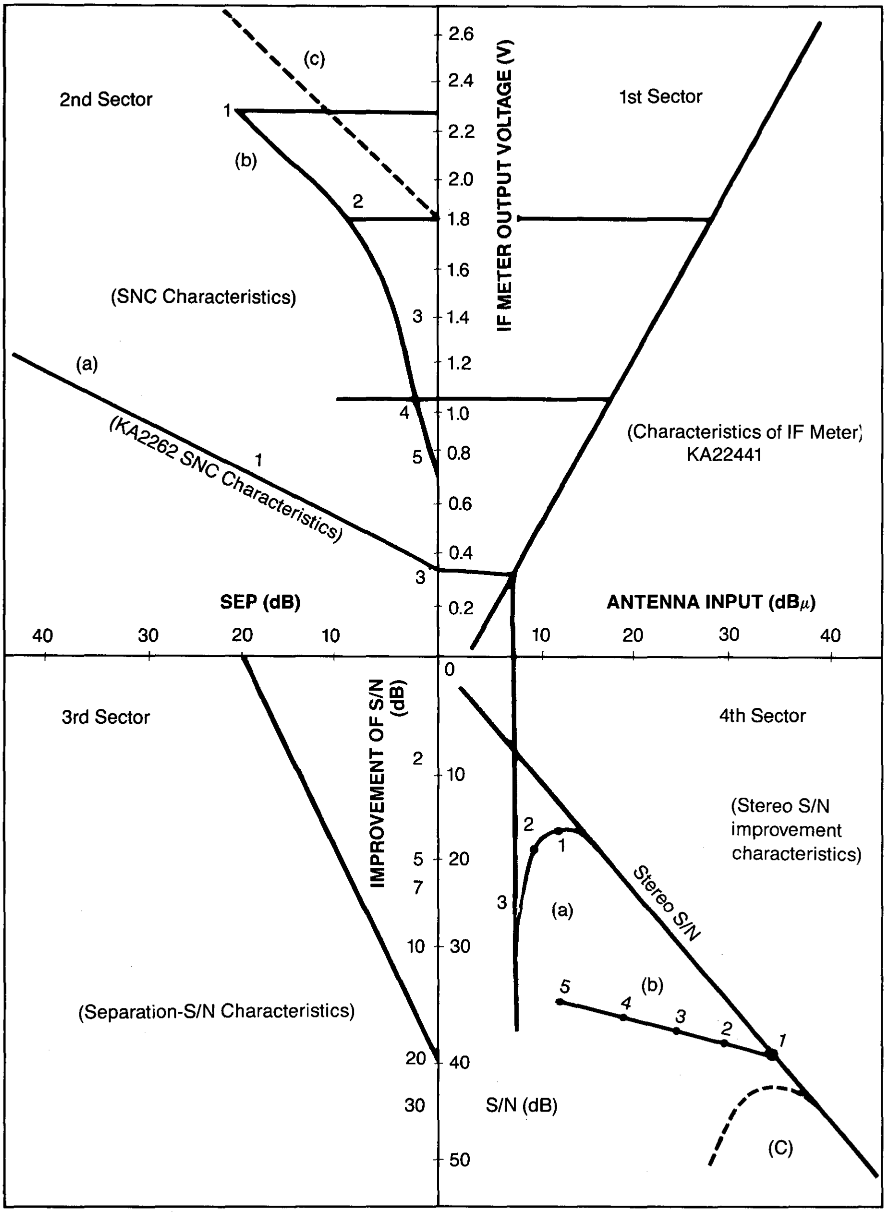


Fig. 8

WORKING AREA OF SNC AND HCC

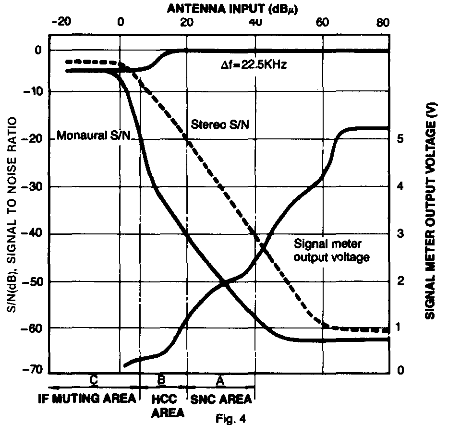


Fig. 4

RELATIONSHIPS BETWEEN SEPARATION AND S/N IMPROVEMENT

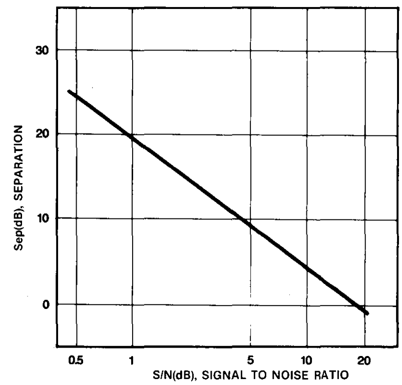
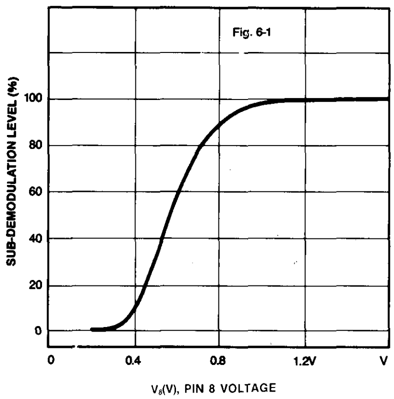


Fig. 5

SNC CHARACTERISTICS (SUB-LEVEL) **KA2262 SNC CHARACTERISTICS** **SNC CHARACTERISTICS (SEPARATION)**



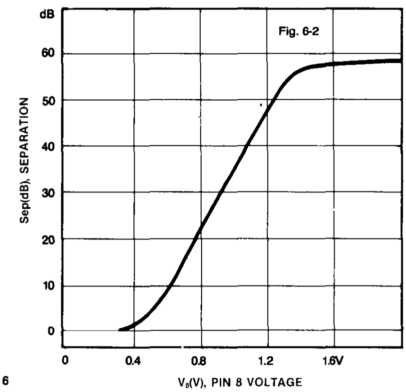


Fig. 6

SNC/HCC CONTROL PIN CURRENT

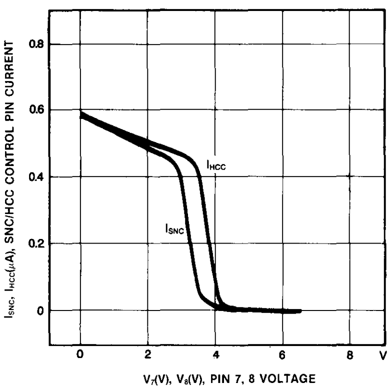


Fig. 7

KA2262 HIGH-CUT CONTROL CHARACTERISTICS

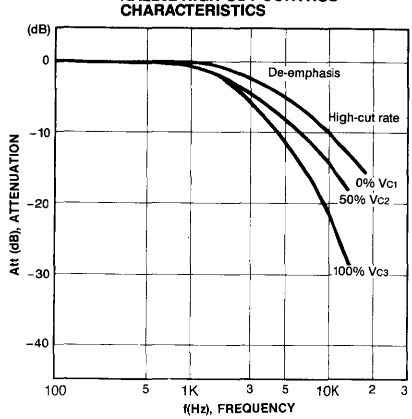


Fig. 9

KA2262 HCC CHARACTERISTICS

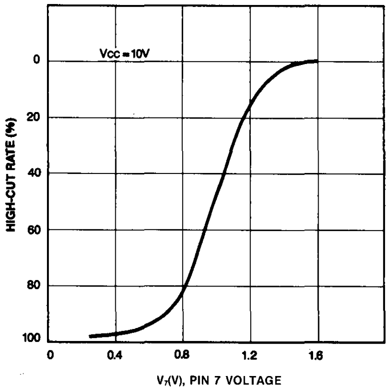


Fig. 10

CHARACTERISTICS OF CURRENT AT VCO STOP FUNCTION CONTROL TERMINAL

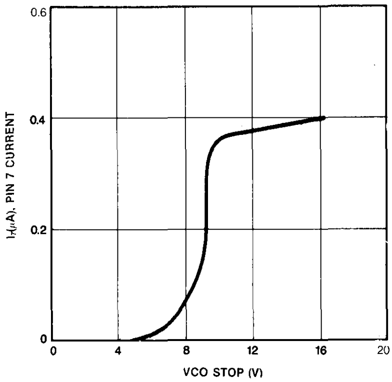
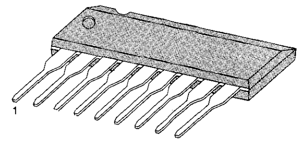


Fig. 11

FM STEREO MULTIPLEX DECODER

The KA2263 is a monolithic integrated circuit consisting of a phase locked loop FM stereo demodulator. It was designed for use in car stereos, cassette recorders and other equipment.

9 SIP



FEATURES

- **Wide operating supply voltage range (3V ~ 12V).**
- **High pilot lamp ON sensitivity.**
  V_L (on)=9mV (Typ).
- **Built-in stereo indicator lamp drive circuit.**
  Maximum lamp current: 20mA (continuous).
- **High channel separation: Sep=45dB (Typ).**
- **Low distortion**
  THD=0.08% (Typ) at V_i=200mV.
- **VCO stop and stereo lamp turn off are simultaneously operated by connected pin 7 to V_{CC}.**
- **Minimum number of external parts required.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2263	9 SIP	−20 ~ +70°C
KA2263G	PELLET	

TYPICAL APPLICATION CIRCUIT

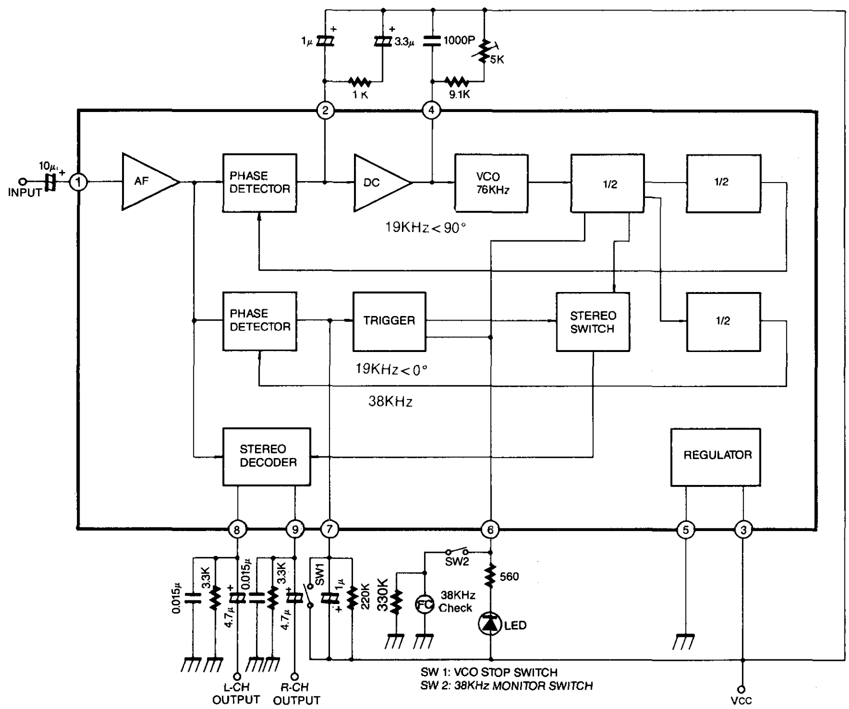


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	12	V
Lamp Voltage	V_{LAMP}	16	V
Lamp Current	I_L (continuous)	20	mA
	I_L (peak)	40	mA
Power Dissipation	P_d	500*	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temeprature	Tstg	−40 ~ +125	°C

*Derated above T_a=25°C in the proportion of 4mW/°C

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=8V, f=1KHz, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current		I_{CC}	V_i=0		11	18	mA
Input Impedance		R_i			33		KΩ
Maximum Input Level		V_i (max)	L+R=90%, P=10%, THD=1%		550		mV
Channel Separation		Sep	L+R=180mV P=20mV	36	45		dB
Total Harmonic Distortion	Mono	THD 1	V_i=200mV		0.08	0.3	%
	Stereo	THD 2	L+R=180mV P=20mV		0.08		%
Voltage Gain		A_V	V_i=200mV	−2.0	0	+2.0	dB
Channel Balance		C B	V_i=200mV		0	1.5	dB
Lamp ON Level		V_L (on)	Pilot only		9	15	mV
Lamp OFF Level		V_L (off)	Pilot only	2	6		mV
Lamp Hysteresis		HY			3		mV
Carrier Leak	19KHz	CL	L+R=180mV		34		dB
	38KHz		P=20mV		42		dB

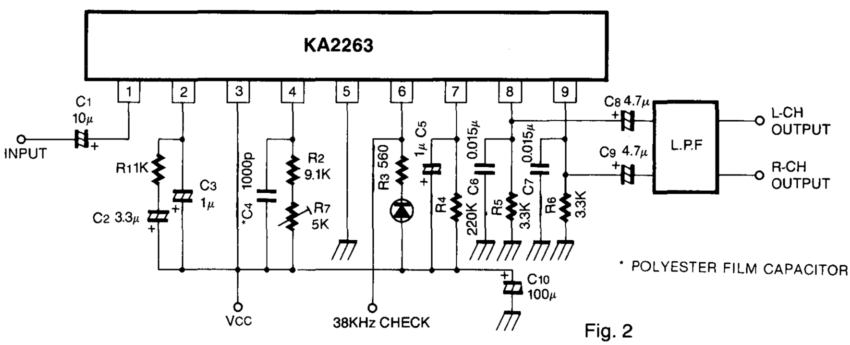
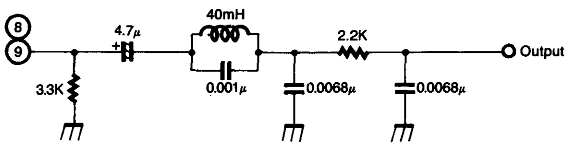


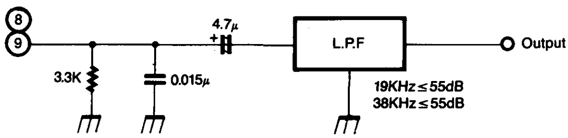
Fig. 2

3

External Components (Refer to Test Circuit)

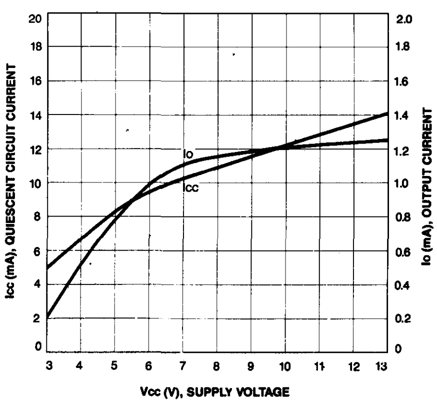
1. Input coupling capacitor (C_1)
   The recommended value is 10μF. If smaller values than 10μF are used, low frequency separation will worsen, and if larger values are used, pop noise occurs strongly.
2. Low pass filter (C_2, C_3, R_7)
   This is the low pass filter fr the PLL, which is determined the capture range and THD at low frequency.
3. VCO network (C_4, R_2, R_7)
   The VCO free running frequency is adjusted by connecting a frequency counter to monitor the 38KHz output of Pin 6.
4. Decoder output (Pins 8, 9)
   These components provide R and L channel output load circuits. The recommended circuits as follows:



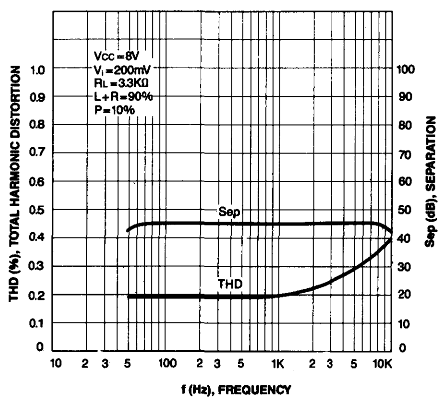


5. **Lamp sensitivity control (R_4)**
   Lamp on level can be controlled by this resistor.

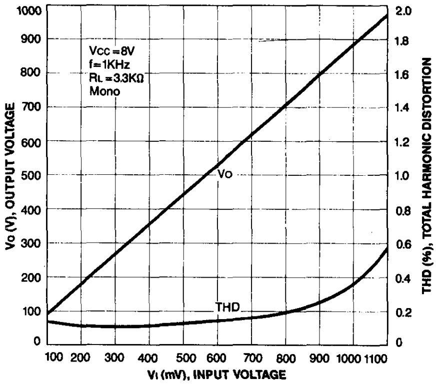
OUTPUT CURRENT / QUIESCENT CIRCUIT CURRENT —SUPPLY VOLTAGE



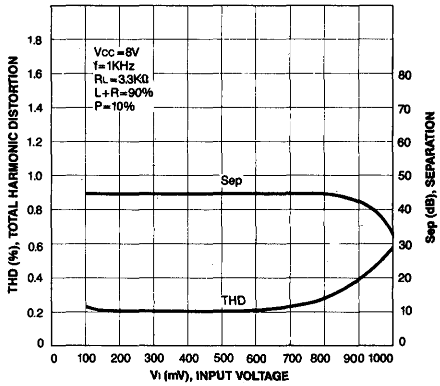
SEPARATION / TOTAL HARMONIC DISTORTION —FREQUENCY



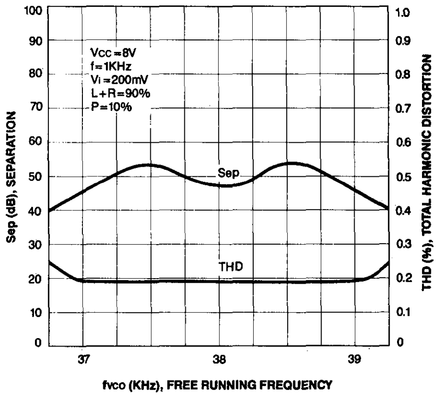
OUTPUT VOLTAGE / TOTAL HARMONIC DISTORTION —INPUT VOLTAGE



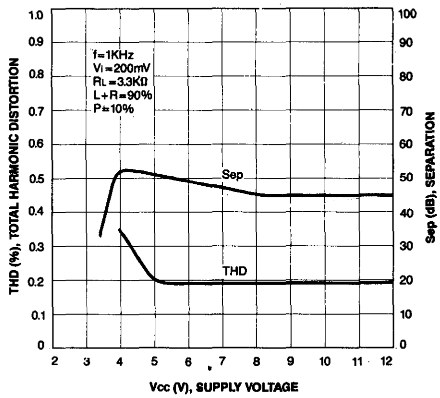
SEPARATION / TOTAL HARMONIC DISTORTION —INPUT VOLTAGE



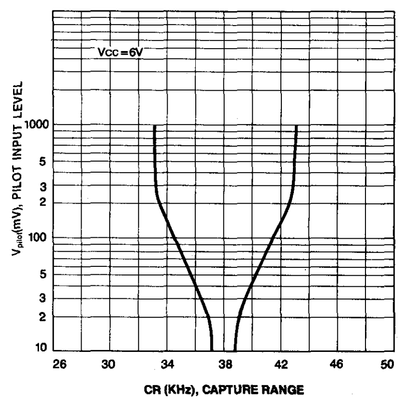
SEPARATION / TOTAL HARMONIC DISTORTION —FREE RUNNING FREQUENCY



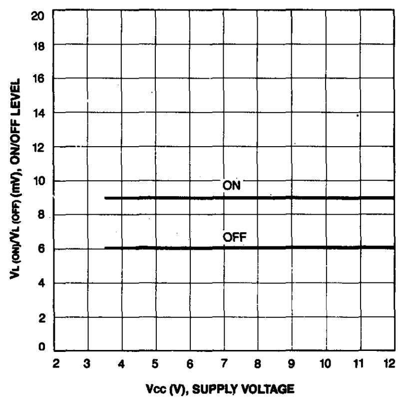
SEPARATION / TOTAL HARMONIC DISTORTION —SUPPLY VOLTAGE



CAPTURE RANGE

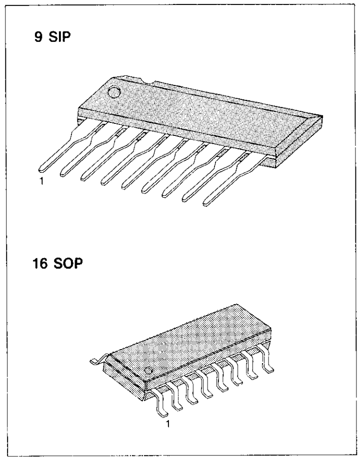


LAMP ON/OFF LEVEL-SUPPLY VOLTAGE



FM STEREO MULTIPLEX DECODER

The KA2264 is a monolithic integrated circuit consisting of a phase locked loop FM stereo demodulator. It is designed for use in 3V radio cassette recorders.



FEATURES

- **Low voltage operation: V_{CC}=1.8V ~ 5V.**
- **Excellent space-factor: 9 SIP/16 SOP.**
- **Minimum number of external parts required.**
- **Easy monitoring of VCO free running frequency is available at Pin 6.**
- **High pilot sensitivity: V_L (on)=9mV (Typ).**
- **Lamp drive current: max lamp current=8mA.**
- **VCO stop and stereo lamp turn-off are simultaneously operated by connecting Pin 7 to V_{CC}.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2264	9 SIP	−20 ~ +70°C
KA2264D	16 SOP	
KA2264G	PELLET	

BLOCK DIAGRAM

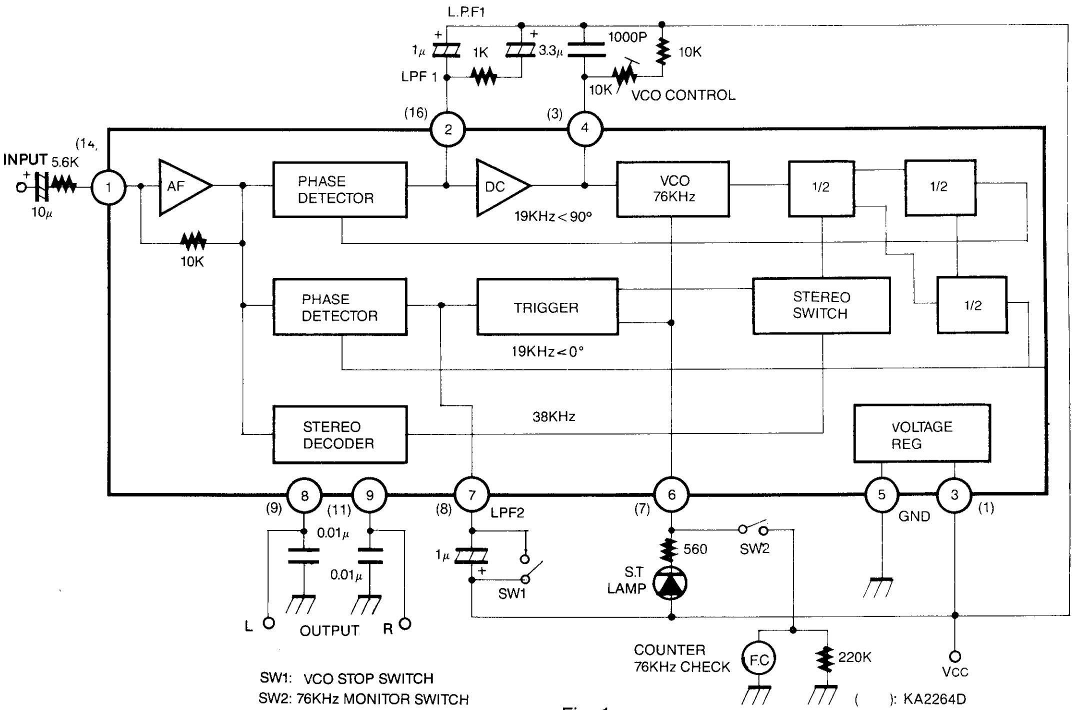


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic		Symbol	Value	Unit
Supply Voltage		V_{CC}	6	V
Lamp Voltage		V_{LAMP}	8	V
Lamp Current		I_{LAMP}	8	mA
Power Dissipation	KA2264	P_d	500	mW
	KA2264D		350	
Operating Temperature		T_{opr}	−20 ~ +70	°C
Storage Temperature		T_{stg}	−40 ~ +125	°C

* Derated above T_a=25°C in the proportion of 4mW/°C (KA2264D: 2.8mW/°C)

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=3V, f=1KHz, unless otherwise specified)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Circuit Current		I_{CC}	V_i=0			4.5	8.0	mA
Input Resistance		R_i				10		KΩ
Output Resistance		R_o			4.0	5.0	6.0	KΩ
Maximum Input Level		V_i (max) Stereo	L+R=90%, P=10% f=1KHz, THD=5%			400		mV
Channel Separation		Sep	L+R=180mV P=20mV	f=100Hz		35		dB
				f=1KHz	30	35		
				f=10KHz		35		
Total Harmonic Distortion	Mono	THD 1	V_i=200mV			0.4	1.0	%
	Stereo	THD 2	L+R=180mV, P=20mV			0.5		
Voltage Gain		A_V	V_i=200mV		−6.5	−5.0	−3.5	dB
Channel Balance		CB	V_i=200mV			0	1.5	dB
Lamp Level	ON	V_L(on)	Pilot only			9	15	mV
	OFF	V_L(off)			2	6		
Lamp Hysteresis		HY				3		mV
Capture Range		CR	P=20mV			±3		%
Carrier Leak	19KHz	CL	P=20mV			32		dB
	38KHz		L+R=180mV			60		
SCA Rejection Radio		SCA R_{ej}	P=20mV L+R=160mV SCA=20mV f_{SCA}=67KHz			80		dB
Signal to Noise Ratio		S/N	V_i=200mV R_g=620Ω			82		dB

TEST CIRCUIT 1

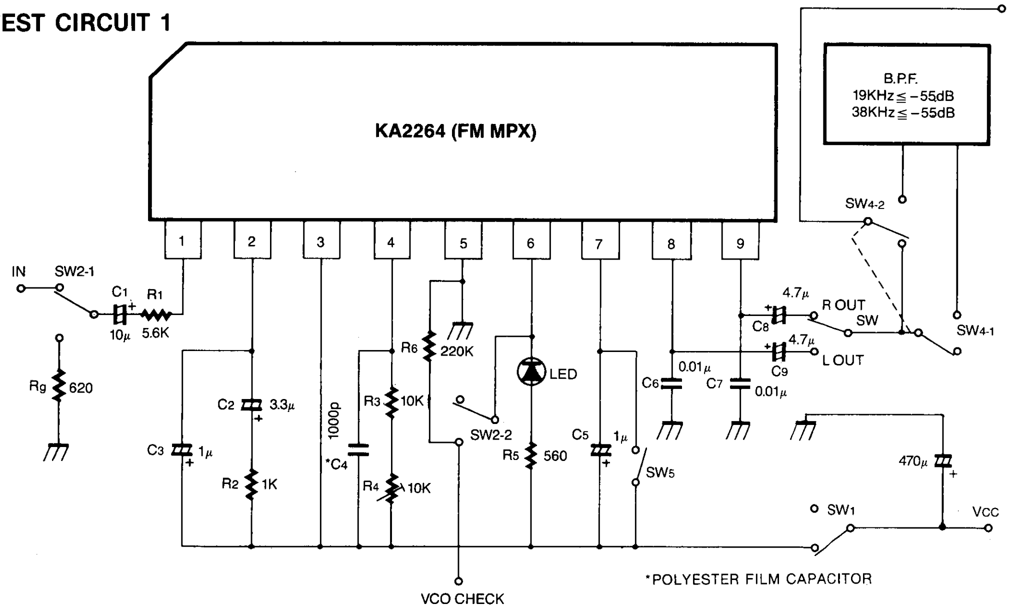


Fig. 2

TEST CIRCUIT 2

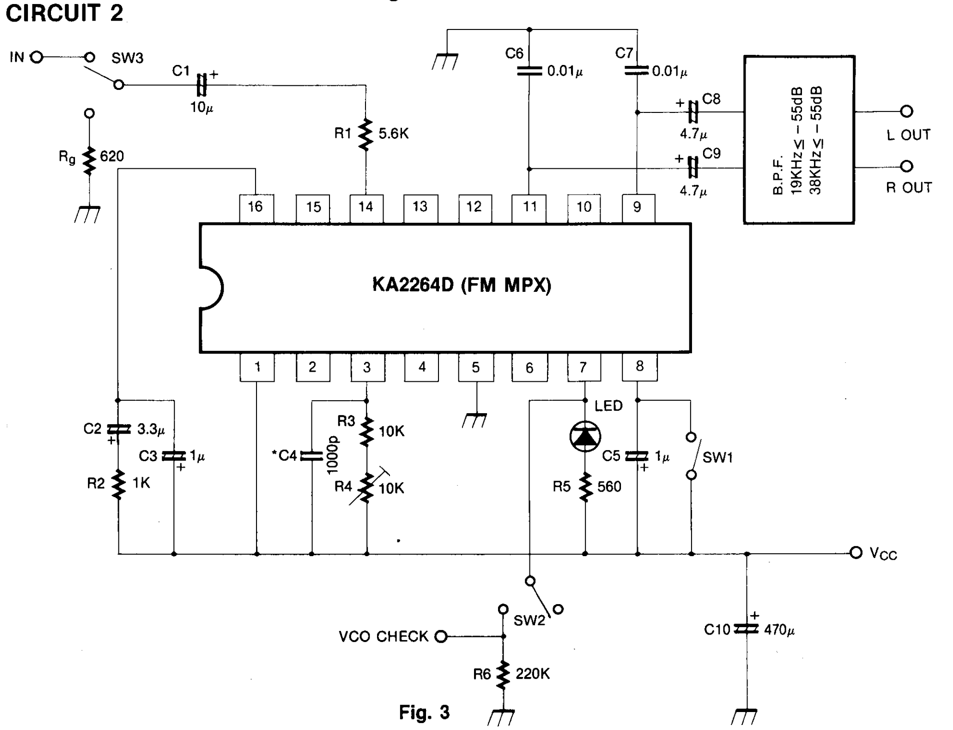
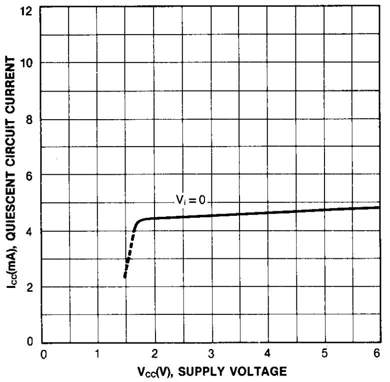
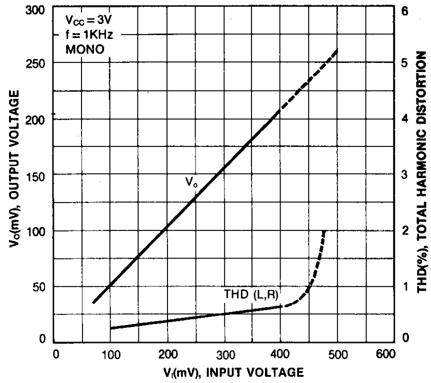


Fig. 3

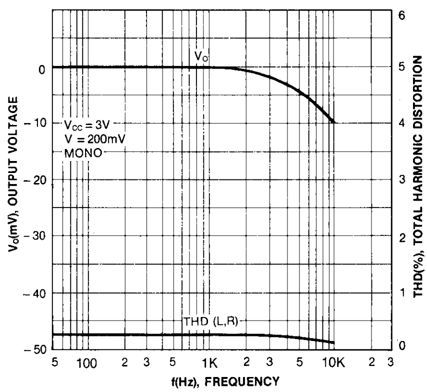
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



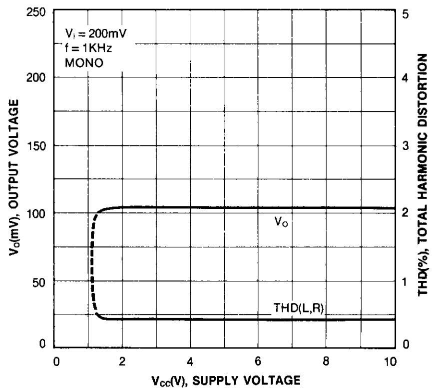
OUTPUT VOLTAGE / TOTAL HARMONIC DISTORTION ·INPUT VOLTAGE



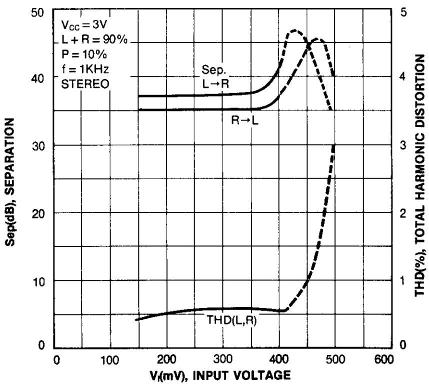
OUTPUT VOLTAGE / TOTAL HARMONIC DISTORTION ·FREQUENCY



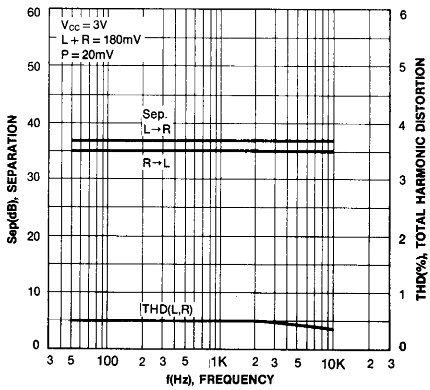
OUTPUT VOLTAGE / TOTAL HARMONIC DISTORTION ·SUPPLY VOLTAGE



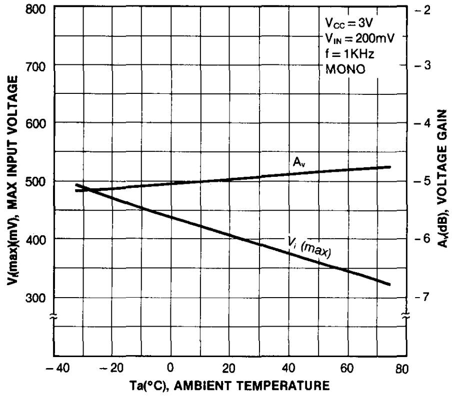
SEPARATION / TOTAL HARMONIC DISTORTION · INPUT VOLTAGE



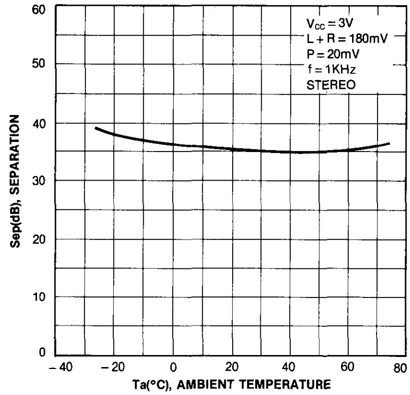
SEPARATION / TOTAL HARMONIC DISTORTION ·FREQUENCY



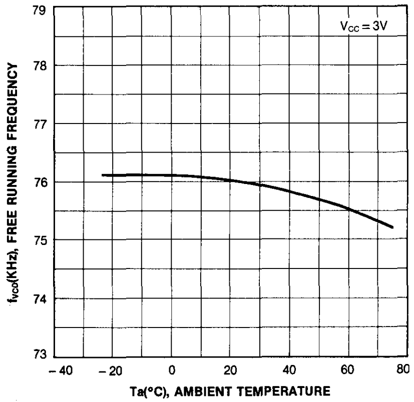
MAX INPUT VOLTAGE / VOLTAGE GAIN -AMBIENT TEMPERATURE



SEPARATION-AMBIENT TEMPERATURE



FREE RUNNING FREQUENCY -AMBIENT TEMPERATURE

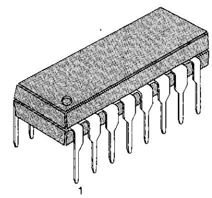


3

VCO NON-ADJUSTING FM STEREO MULTIPLEX DECODER

The KA2265 is a monolithic integrated circuit consisting of a VCO non-adjusting FM stereo demodulator with a phase locked loop. It is designed for use in home stereos and portable Hi-Fi systems.

16 DIP



FEATURES

- **Non-adjusting VCO: non-adjusting of free-running frequency.**
- **Excellent temperature characteristics of VCO: ±0.1% (Typ) at ±50°C.**
- **Excellent stereo high frequency distortion. (f=10KHz: 0.06% (Typ)).**
- **Excellent distortion: f=1KHz, V_i=300mV, mono: 0.025% (Typ).**
  stereo: 0.02% (Typ).
- **High S/N: 91dB (Typ) (mono V_i=300mV, LPF).**
  92dB (Typ)(mono V_i=300mV, IHF BPF).
- **High gain: about 8.5dB.**
- **Wide dynamic range: mono 800mV (f=1KHz, THD=1%)**
- **Good ripple rejection: 34dB (Typ).**
- **Operating voltage range: V_{CC}=6.5V ~ 14V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2265	16 DIP	−20 ~ +70°C

BLOCK DIAGRAM

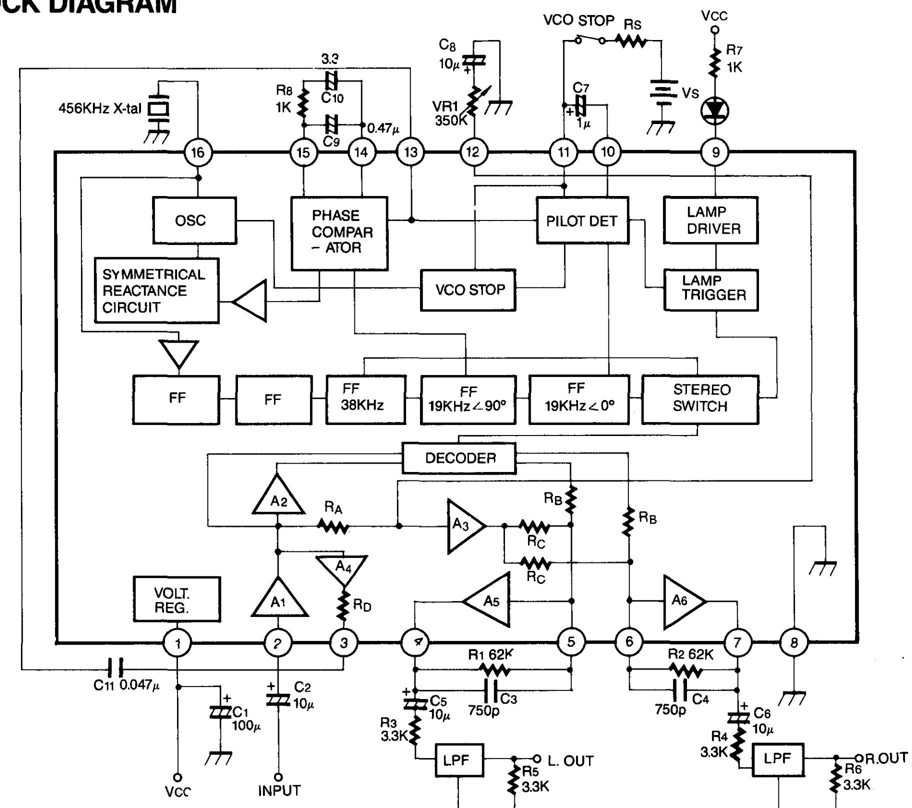


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	16	V
Lamp Current	I_L	30	mA
Power Dissipation	P_d	480	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

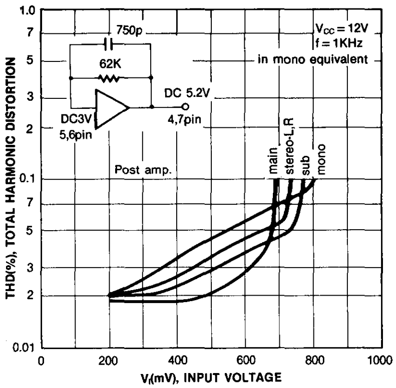
3

ELECTRICAL CHARACTERISTICS

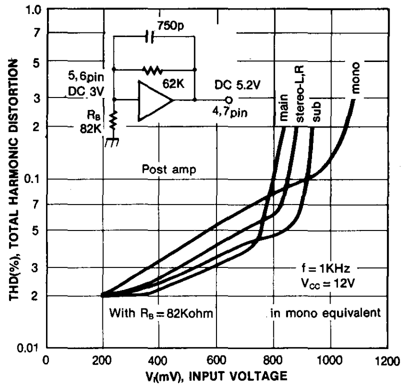
(V_{CC} = 12V, f = 1KHz, T_a = 25°C, unless otherwise specified)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Circuit Current		I_{CC}	V_i=0			18.5	28	mA
Channel Separation		Sep	P=30mV, L+R=270mV	f=100Hz		45		dB
				f=1KHz	40	55		
				f=10KHz		42		
Total Harmonic Distortion	Stereo	THD 1	P=30mV L+R=270mV	f=100Hz		0.025	0.15	%
				f=1KHz		0.02		
				f=10KHz		0.06	0.15	
	Mono	THD 2	V_i=300mV			0.025	0.15	
Output Voltage		V_O	V_i=300mV		500	730	1000	mV
Channel Balance		CB	V_i=300mV			0	1	dB
Lamp ON Level		V_L (on)	Pilot Level		4	8	17	mV
Lamp Hysteresis		HY				3		dB
Capture Range		CR	P=30mV			+0.8 −1.2		%
Signal to Noise Ratio		S/N	V_i=300mV R_g=5.1KΩ		80	91		dB
Input Impedance		Ri				20		KΩ
Maximum Input Level		Vi (max)	Mono, THD=1%		700	800		mV
Carrier Leak		CL	P=30mV, L+R=270mV			31		dB
VCO Stop Voltage		VCO_{stop}			5.5		V_{CC}-3	V
Ripple Rejection		RR				34		dB

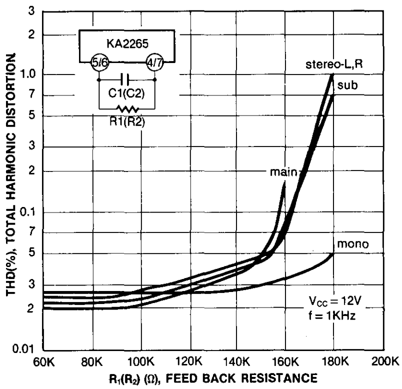
TOTAL HARMONIC DISTORTION-INPUT VOLTAGE



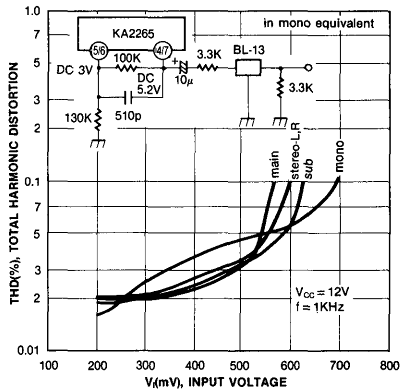
TOTAL HARMONIC DISTORTION-INPUT VOLTAGE



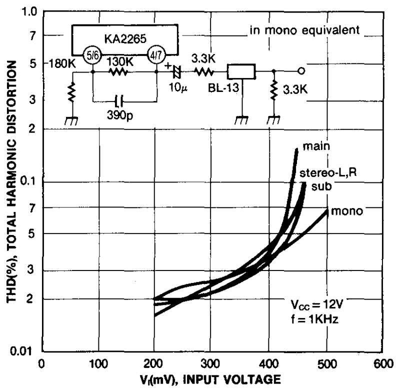
TOTAL HARMONIC DISTORTION-FEED BACK RESISTANCE $R_1(R_2)$



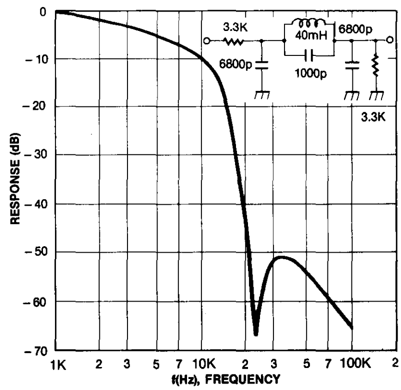
TOTAL HARMONIC DISTORTION-INPUT VOLTAGE



TOTAL HARMONIC DISTORTION-INPUT VOLTAGE

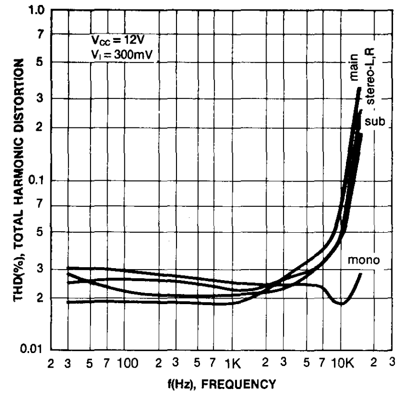


FREQUENCY RESPONSE (INCLUDING DE-EMPHASIS)

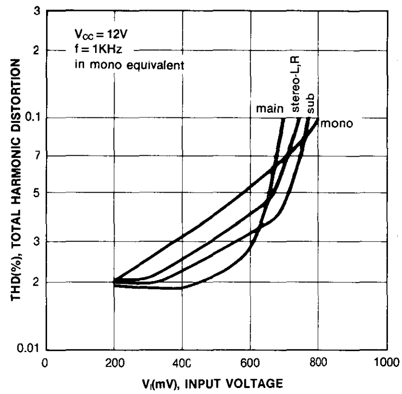


3

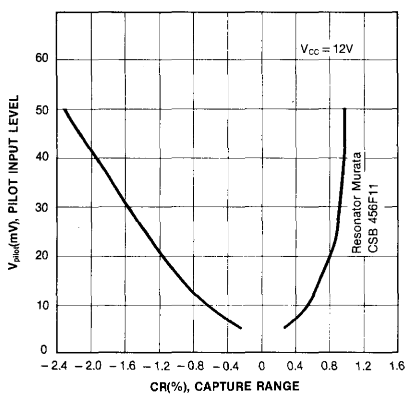
TOTAL HARMONIC DISTORTION-FREQUENCY



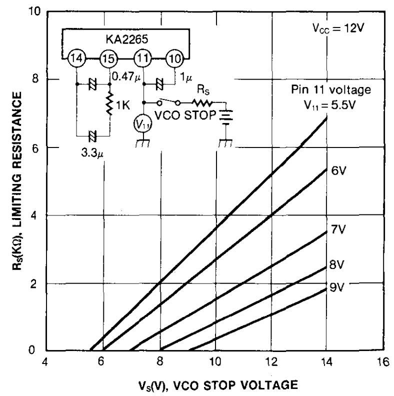
TOTAL HARMONIC DISTORTION-INPUT VOLTAGE



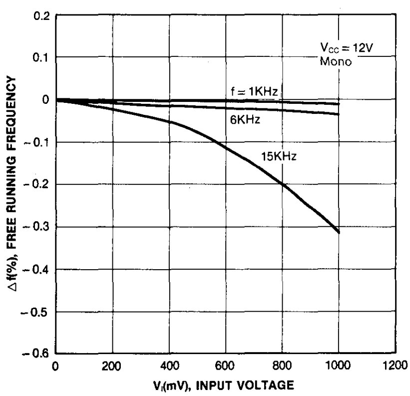
CAPTURE RANGE



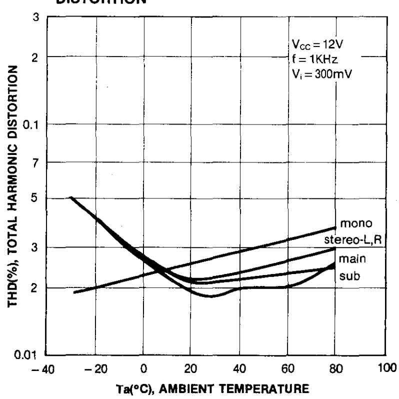
LIMITING RESISTANCE-VCO STOP VOLTAGE



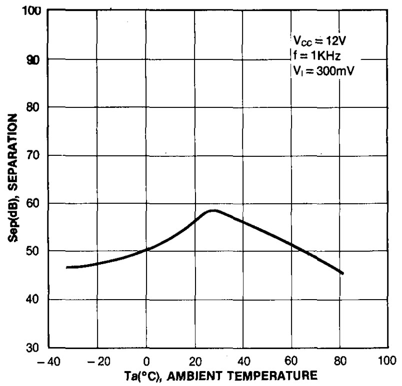
FREE RUNNING FREQUENCY-INPUT VOLTAGE



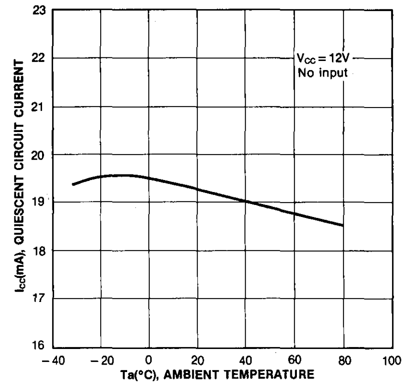
TOTAL HARMONIC DISTORTION -AMBIENT TEMPERATURE



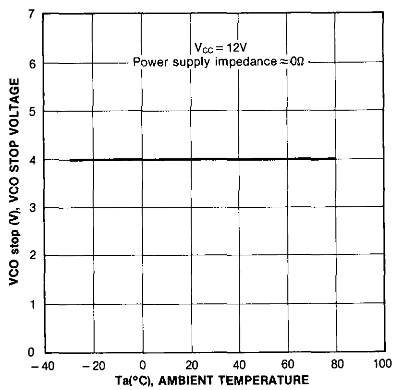
SEPARATION-AMBIENT TEMPERATURE



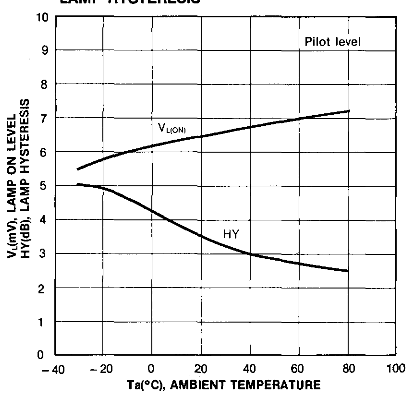
QUIESCENT CIRCUIT CURRENT -AMBIENT TEMPERATURE



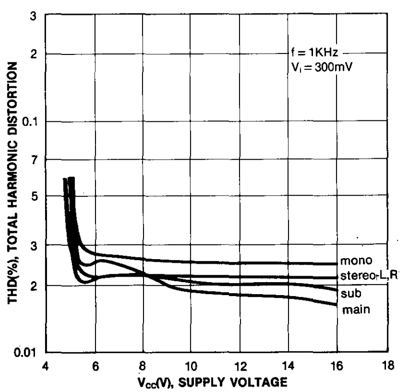
VCO STOP VOLTAGE-AMBIENT TEMPERATURE



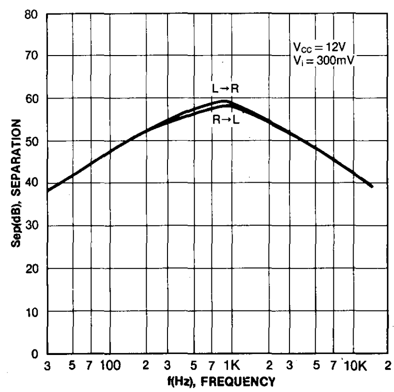
LAMP ON LEVEL
LAMP HYSTERESIS -AMBIENT TEMPERATURE



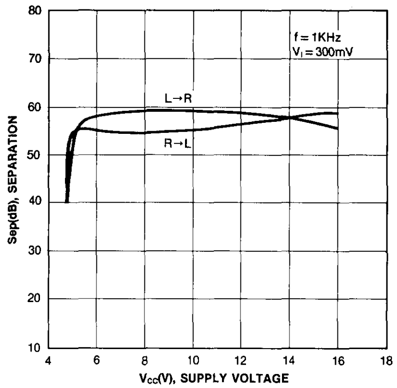
TOTAL HARMONIC DISTORTION-SUPPLY VOLTAGE



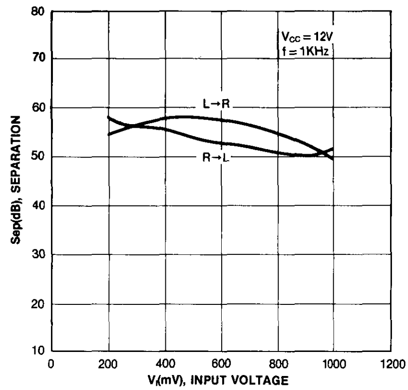
SEPARATION-FREQUENCY



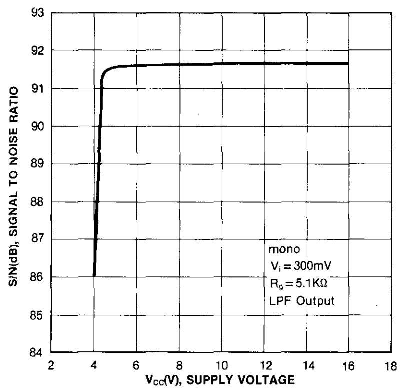
SEPARATION-SUPPLY VOLTAGE



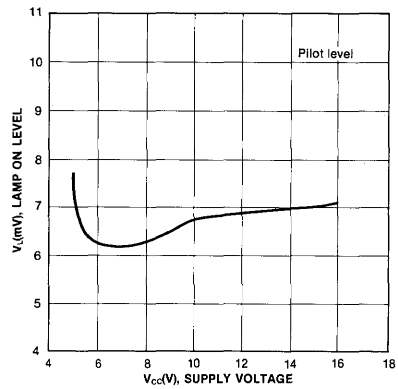
SEPARATION-INPUT VOLTAGE



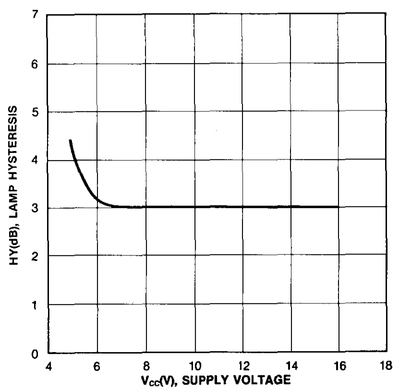
SIGNAL TO NOISE RATIO-SUPPLY VOLTAGE



LAMP ON LEVEL-SUPPLY VOLTAGE



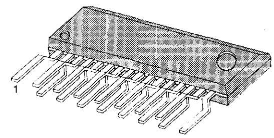
LAMP HYSTERESIS-SUPPLY VOLTAGE



MPX FOR CAR STEREOS

The KA2266 is a monolithic integrated circuit consisting of a phase locked loop FM stereo demodulator with pilot canceller. It is designed for use in car stereos.

16 ZSIP



FEATURES

- **Built-in pilot-cancelling circuit**
- **Stereo noise controlling (SNC)**
- **High-cut controlling (HCC)**
- **With separation control terminal**
- **Stereo-monaural automatic conversion**
- **Stopping of VCO oscillation**
- **Power supply ripple rejection: 35dB typ.**
- **Low distortion: THD = 0.05% typ. at V_I = 300mV, mono.**
- **Wide operating voltage range: V_{CC} = 6.5V ~ 14V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2266	16 ZSIP	−20 ~ +70°C

BLOCK DIAGRAM

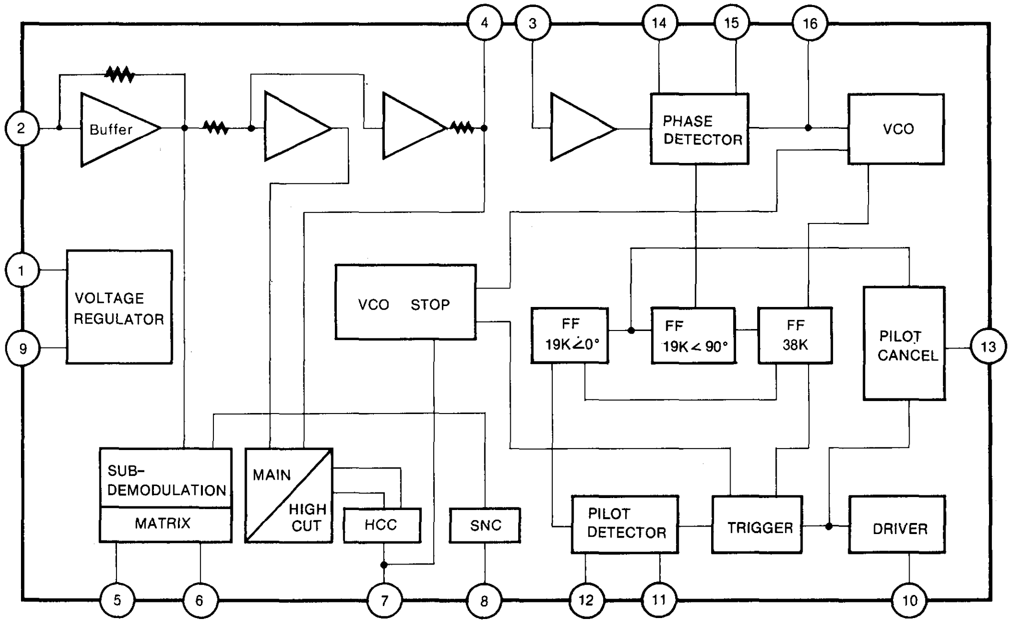


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

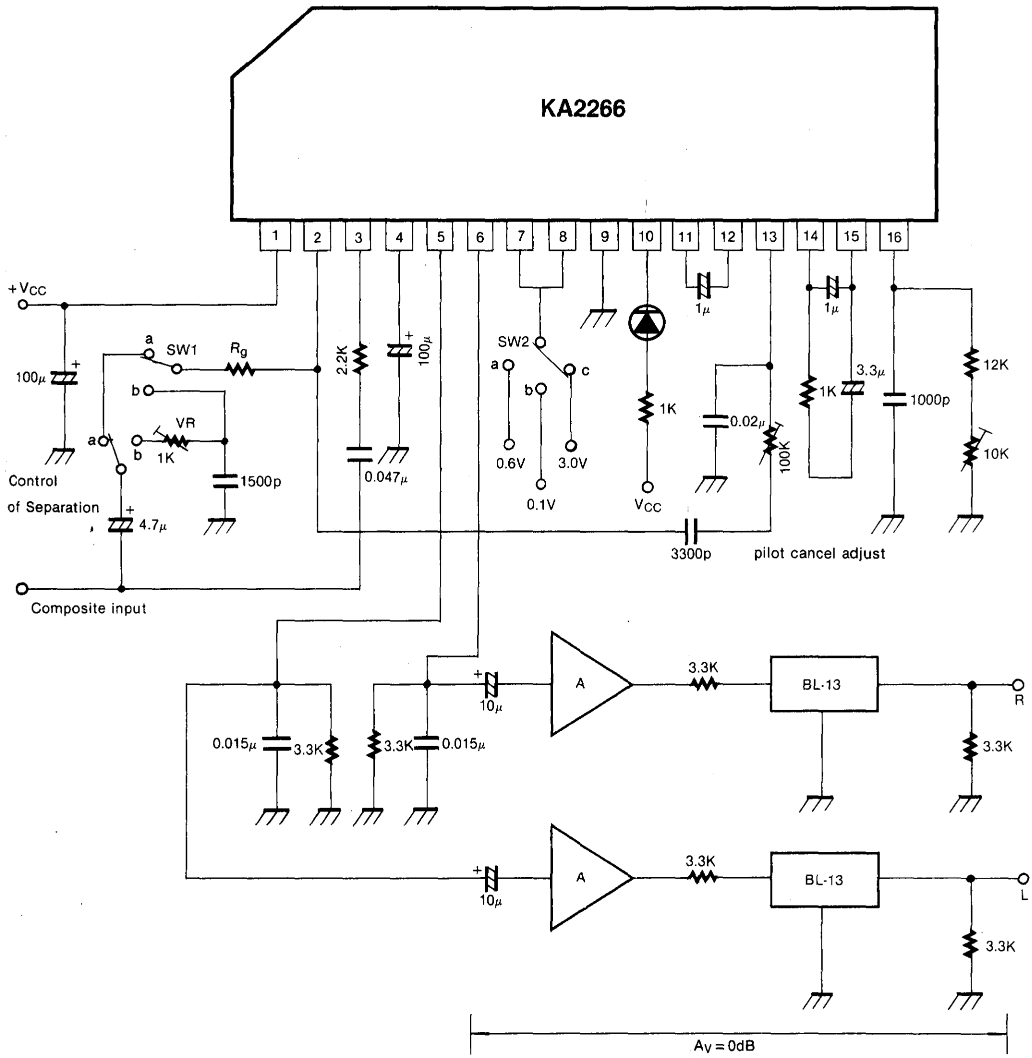
Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Lamp Driving Current (Ta≤45°C)	I_L	40	mA
Power Dissipation	P_d	520	mW
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

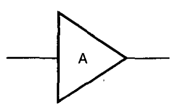
ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 10V, f = 1KHz, V_i = 300mV, L+R = 90%, pilot = 10%, R_g = 20KΩ, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Circuit Current		I_{CC}	V_i = 0		22	28	mA
Channel Separation		Sep		40	50		dB
Total Harmonic Distortion	Mono	THD_1	V_i = 300mV		0.05	0.2	%
	Stereo	THD_2	Main		0.05	0.2	%
Lamp on Level		V_L (on)	L + R = 90%, P = 10%	60	85	120	mV
Hysteresis		HY			3	6	dB
Capture Range		CR	P = 30mV		±3		%
Output Signal Level		V_O	Sub	150	215	300	mV
S/N Ratio		S/N	R_g = 20KΩ	68	74		dB
			R_g = 10KΩ	70	78		dB
Input Resistance (Pin 3)		R_i			20		KΩ
SCA Rejection Ratio		SCA_{Rej}			80		dB
Maximum Input Level		V_i (max)	THD = 1%, R_g = 20KΩ	700	900		mV
			THD = 1%, R_g = 10KΩ		450		mV
SNC Output Attenuation		$SNC_{(ATT)}$	V8 = 0.6V, L − R = 90% P = 10%	−8.5	−3.0	−0.3	dB
SNC Output Voltage		SNC V_O	V8 = 0.1V, L − R = 90% P = 10%			5	mV
HCC Output Attenuation		$HCC_{(ATT)}1$	V7 = 1V, L + R = 90%, P = 10%	−1.5	−0.9	−0.5	dB
		$HCC_{(ATT)}2$	V7 = 1V, L + R = 90%, P = 10%	−2.0		0	dB
Ripple Rejection		RR			35		dB
VCO Stopping Voltage		VCO_{stop}			7.3		V
Channel Balance		CB			0.5	1.5	dB
Carrier Leak		CL		20	25		dB

TEST CIRCUIT





; It has a 100KHz bandwidth, 0.01% or better distortion factor, and 330K or higher input impedance.

Fig. 2

3

APPLICATION CIRCUIT

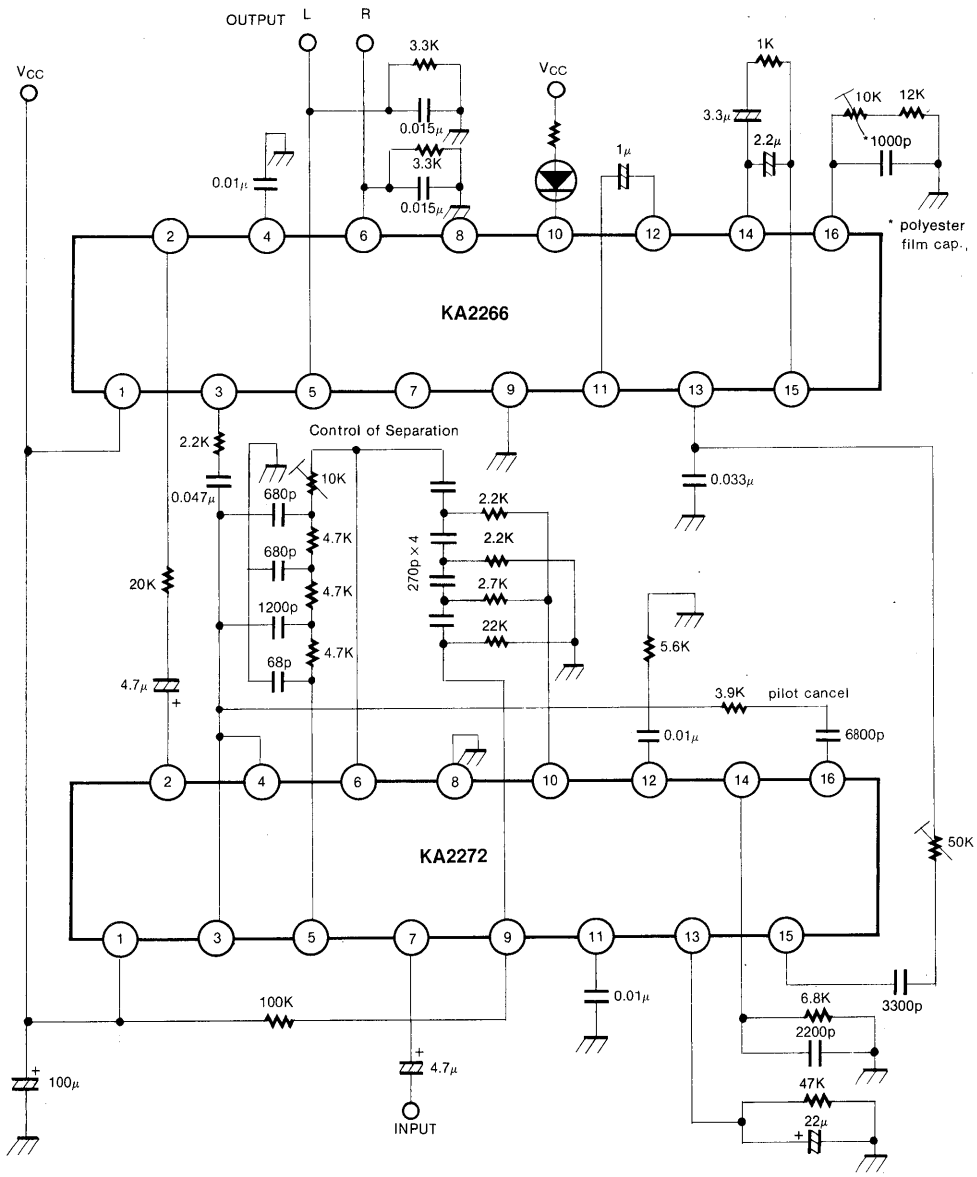
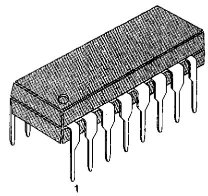


Fig. 3

DOLBY* B-TYPE NOISE REDUCTION PROCESSOR

The KA2271 is a monolithic integrated circuit designed for use in Dolby*B-type noise reduction systems.

16 DIP



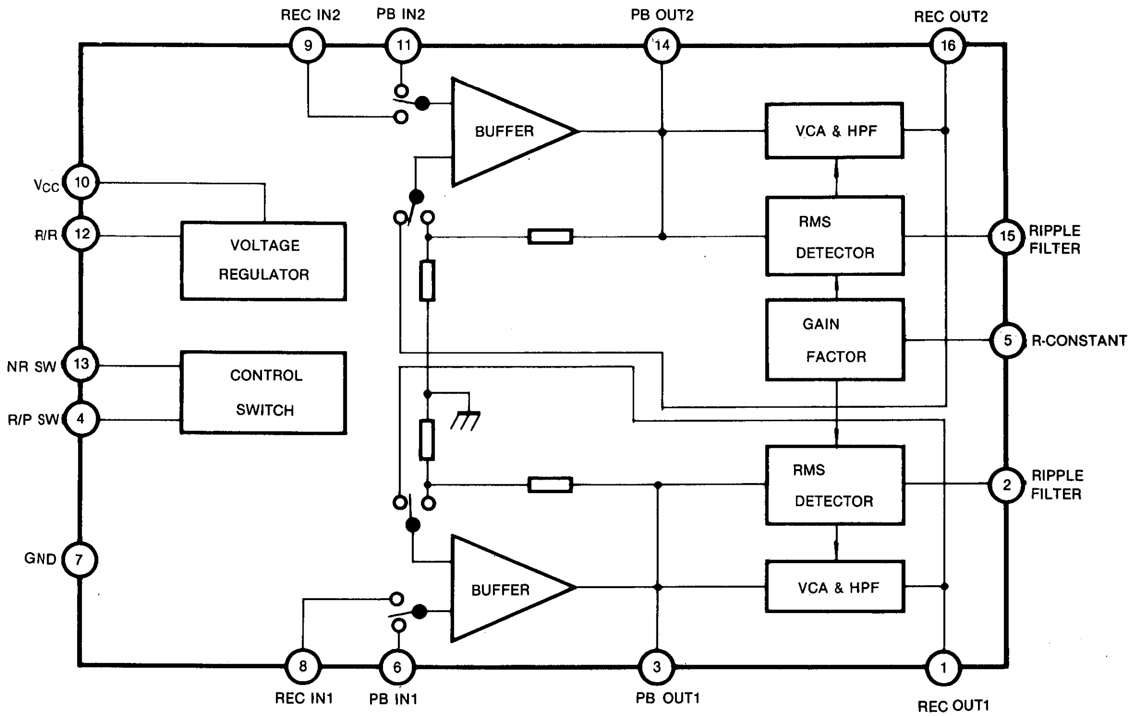
FEATURES

- **Few external components**
- **Low power consumption (typ I_{CC} = 4.3mA)**
- **High crosstalk rejection ratio**
- **Built in NR-switch, REC/PB-switch**
- **Recommended supply voltage: 8V ~ 16V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2271	16 DIP	−30 ~ +85°C

BLOCK DIAGRAM



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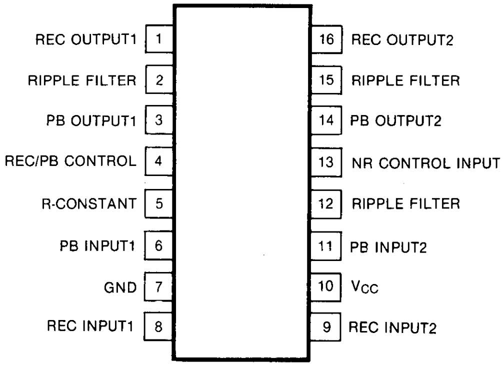
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V	16	V
Power Dissipation	P_d	750	mW
Operating Temperature	T	−30 ~ +85	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

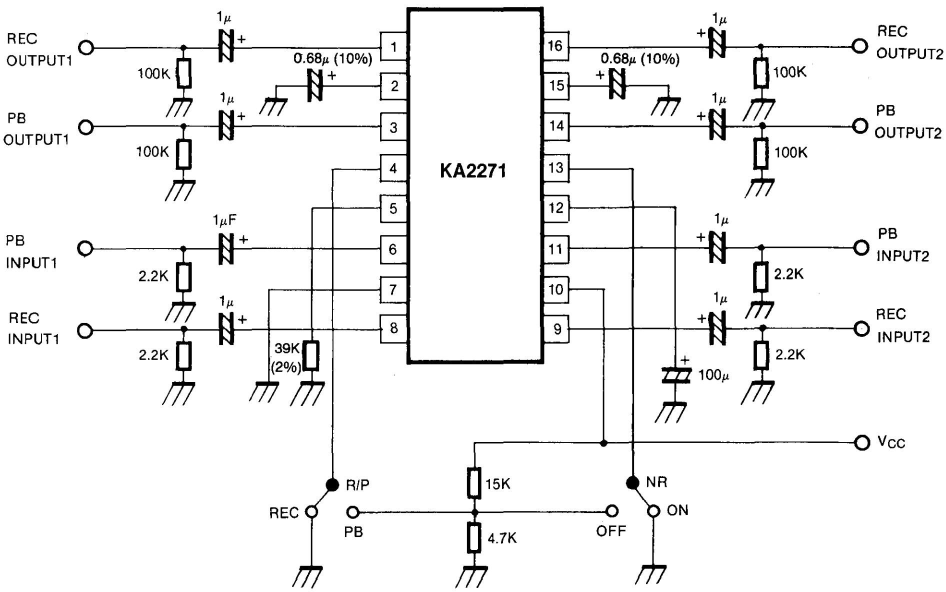
Note: Derated above Ta = 25°C in the propation of 10mW/°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 12V, f = 1KHz, 0dB = 245mV (−10dBm). at REC OUT, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Circuit Current	I_{CC}	REC mode, NR-off, V_{IN} = 0	3.5	4.3	6	mA
Buffer Voltage Gain	A_V	REC mode, PBout = 0dB	25	27	29	dB
NR-REC Boost	BST	RECout = −25dB, f = 500Hz	1.4	2.5	4.4	dB
		RECout = −25dB, f = 2KHz	5.5	7.0	8.5	dB
		RECout = −25dB, f = 5KHz	3.9	5.4	6.9	dB
		RECout = −40dB, f = 10KHz	9.7	10.4	11.9	dB
		RECout = 0dB, f = 10KHz	−1.1	0.4	1.9	dB
NR-Boost Balance	BL	NR-REC boost CH to CH ratio		0	1	dB
MAX. RECout level	$V_{o(max)}$	REC mode, NR-off THD = 1%	14	16		dB
RECout Distortion	THD	REC mode, NR-off RECout = 10dB		0.04	0.1	%
		REC mode, NR-on RECout = 10dB		0.04	0.1	%
NR-effect S/N	S/N	REC mode, Rg = 2.2K Filter = CCIR/ARM	65	69		dB
Crosstalk	CT	NR-off OUTPUT = 0dB PB to REC		−70	−65	dB
		CH to CH, NR-off OUTPUT = 0dB		−70	−65	dB
Input Impedance	Zin		30	47	60	KΩ
Switch Control Voltage	VC	High mode	2.4			V
		Low mode	0		0.4	V
Input Level	REC Vi	REC mode, NR-off RECout = 0dB	19.5	24.5	31.0	mV
	PB Vi	PB mode, NR-off RECout = 0dB	19.5	24.5	31.0	mV
Output Level	Vout	REC mode, NR-off RECout = 0dB Testpoint = PB output	489	549	616	mV

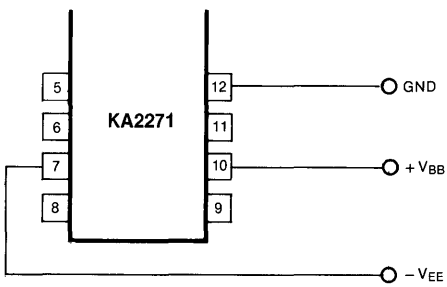
TEST CIRCUIT



APPLICATION NOTE

1) POWER SUPPLY

The KA2271 can be operated at 8V – 16V in case of single and ±4V – ±8V in dual power supply.



Dual power connection

2) SWITCH CONTROL VOLTAGE

All function of KA2271 are controlled by internal electronic switchs. The function switch is operated by D.C. voltage of NR and R/P control pins.

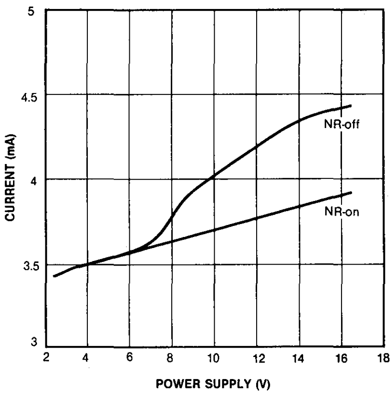
NR, R/P	V_H	V_L
Condition	PB	REC
	NR-off	NR-on

Single Power	Dual Power
$2.4V \leq V_H$ $0.4V \geq V_L$	$V_H \geq V_{EE} + 2.4V$ $V_{EE} + 0.4V \geq V_L$

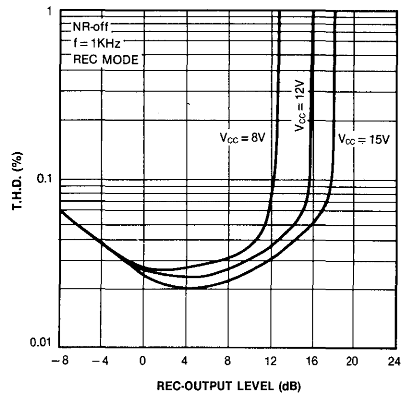
3) REFERENCE LEVEL

The reference output level of Dolby noise reduction system is defined as Dolby level. The Dolby level of KA2271 is 245mV (−10dBm) at f = 400Hz.

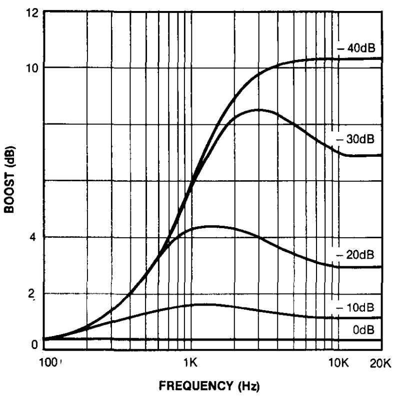
CIRCUIT CURRENT



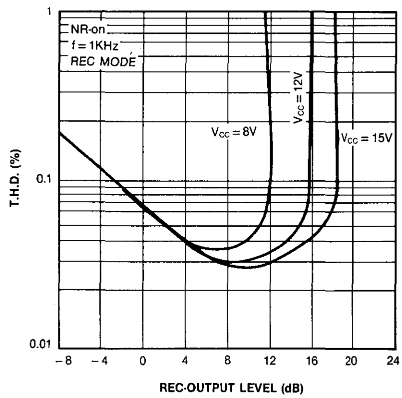
TOTAL HARMONIC DISTORTION (REC)



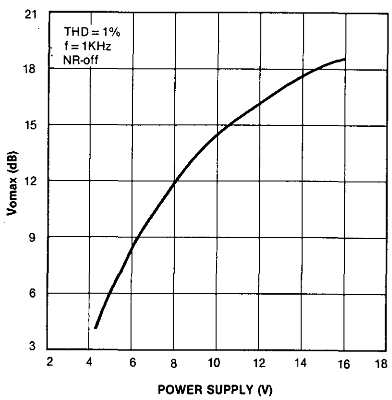
REC (ENCODE) CHARACTERISTIC



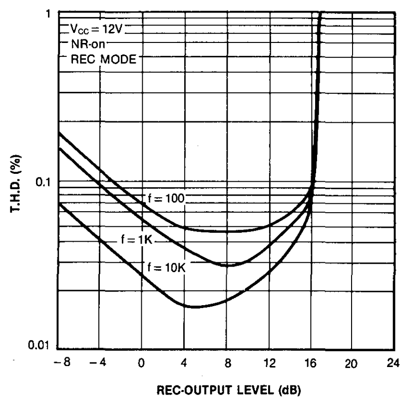
TOTAL HARMONIC DISTORTION (REC)



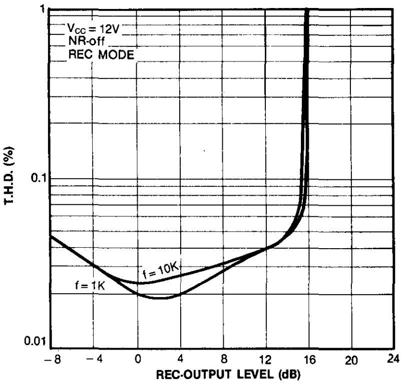
MAX REC-OUTPUT LEVEL



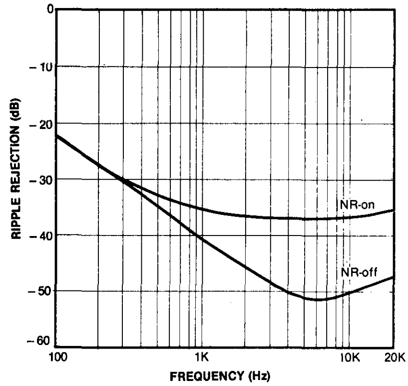
TOTAL HARMONIC DISTORTION (REC)



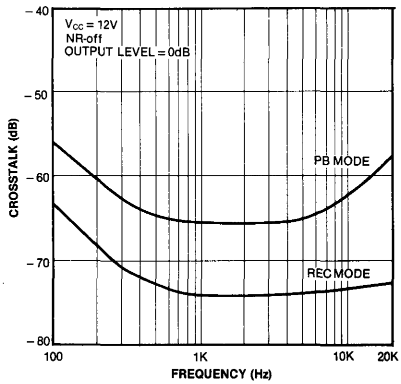
TOTAL HARMONIC DISTORTION (REC)



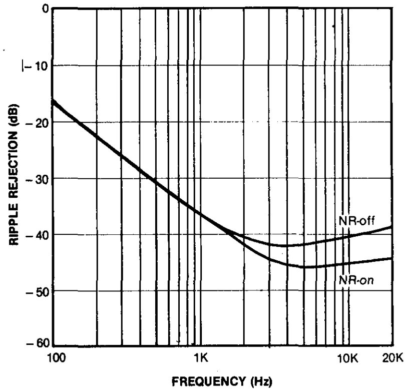
RIPPLE REJECTION (REC)



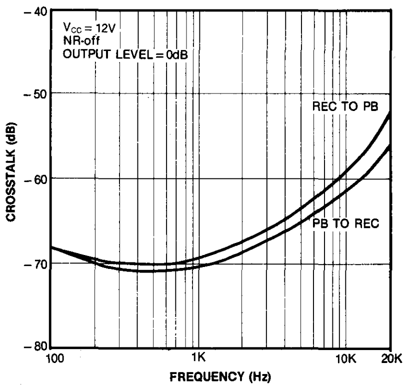
CROSSTALK (CH TO CH)



RIPPLE REJECTION (PB)



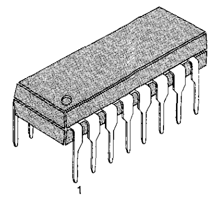
CROSSTALK (BETWEEN REC TO PB)



DOLBY* B-TYPE NOISE REDUCTION PROCESSOR

The KA22711 is a monolithic integrated circuit designed for use in Dolby*B-type noise reduction systems.

16 DIP



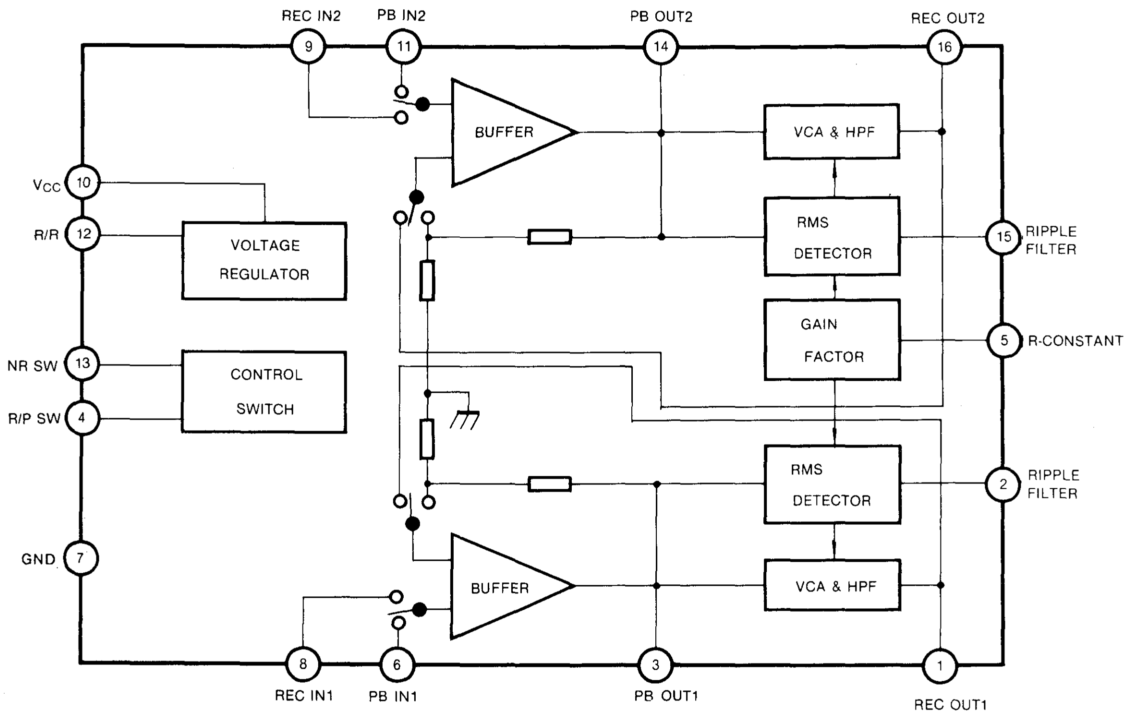
FEATURES

- **Few external components**
- **Low power consumption (typ $I_{CC}=4.5mA$)**
- **High crosstalk rejection ratio**
- **Built in NR-switch, REC/PB-switch**
- **Recommended supply voltage: 5V ~ 16V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA22711	16 DIP	−30 ~ +85°C

BLOCK DIAGRAM



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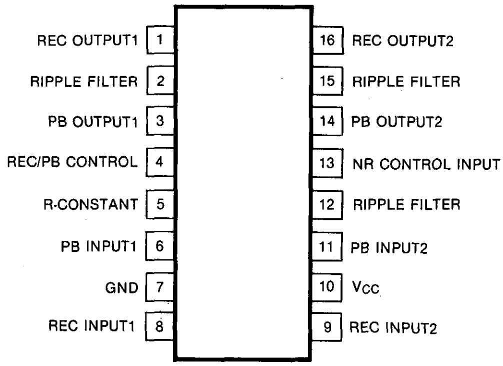
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_d	750	mW
Operating Temperature	T_{opr}	−30 ~ +85	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

Note: Derated above Ta = 25°C in the propation of 10mW/°C

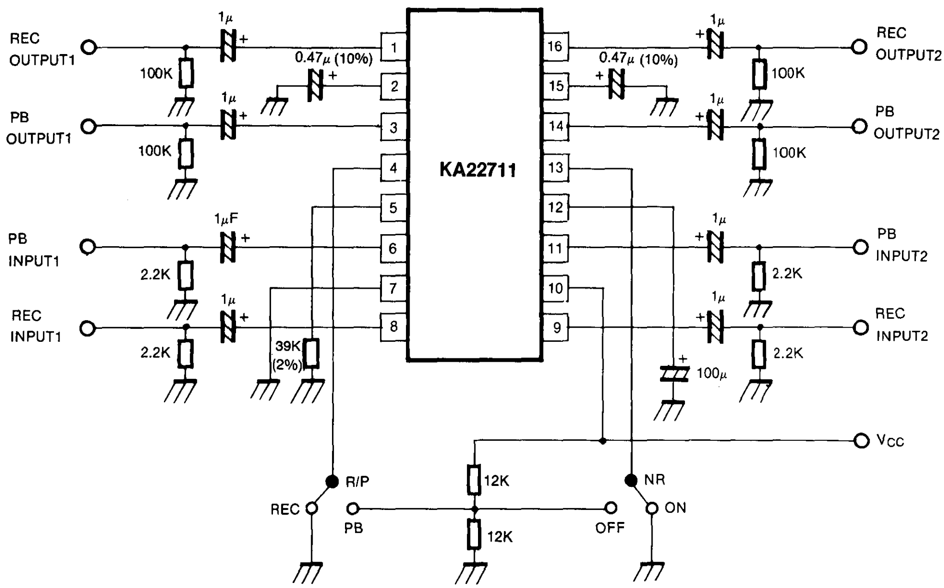
3

ELECTRICAL CHARACTERISTICS

($Ta=25°C$, $V_{CC}=6V$, $f=1KHz$, $0dB=245mV$ ($-10dBm$) at REC OUT, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Circuit Current	I_{CC}	REC mode, NR-off, $V_{IN}=0$	3.5	4.5	6	mA
Buffer Voltage Gain	A_V	REC mode, PBout = 0dB	19	21	23	dB
NR-REC Boost	BST	RECout = −25dB, f = 500Hz	1.4	2.9	4.4	dB
		RECout = −25dB, f = 2KHz	5.5	7.0	8.5	dB
		RECout = −25dB, f = 5KHz	3.9	5.4	6.9	dB
		RECout = −40dB, f = 10KHz	9.1	10.4	11.9	dB
		RECout = 0dB, f = 10KHz	−1.1	0.4	1.9	dB
NR-Boost Balance	BL	NR-REC boost CH to CH ratio		0	1	dB
MAX. RECout level	$V_{o(max)}$	REC mode, NR-off THD = 1%	14	15		dB
RECout Distortion	THD	REC mode, NR-off RECout = 10dB		0.04	0.1	%
		REC mode, NR-on RECout = 10dB		0.04	0.1	%
NR-effect S/N	S/N	REC mode, Rg = 2.2K Filter = CCIR/ARM	65	69		dB
Crosstalk	CT	NR-off OUTPUT = 0dB PB to REC		−75	−65	dB
		CH to CH, NR-off OUTPUT = 0dB		−68	−62	dB
Input Impedance	Zin		30	47	60	KΩ
Switch Control Voltage	VC	High mode	2.4			V
		Low mode	0		0.4	V
Input Level	REC Vi	REC mode, NR-off RECout = 0dB	19.5	24.5	31.0	mV
	PB Vi	PB mode, NR-off RECout = 0dB	19.5	24.5	31.0	mV
Output Level	Vout	REC mode, NR-off RECout = 0dB Testpoint = PB output	218	245	275	mV

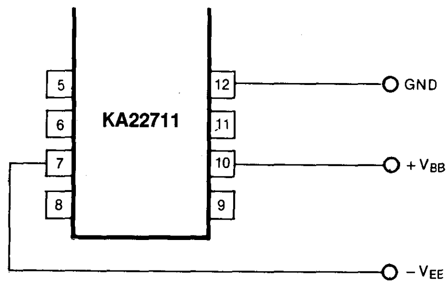
TEST CIRCUIT



APPLICATION NOTE

1) POWER SUPPLY

The KA22711 can be operated at 8V—16V in case of single and ±2.5V – ±8V in dual power supply.



Dual power connection

3

2) SWITCH CONTROL VOLTAGE

All function of KA22711 are controlled by internal electronic switches. The function switch is operated by D.C. voltage of NR and R/P control pins.

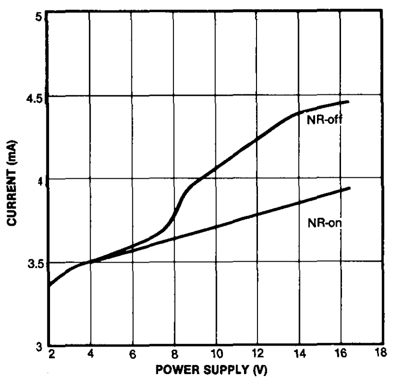
NR, R/P	V_H	V_L
Condition	PB	REC
	NR-off	NR-on

Single Power	Dual Power
$2.4V \leq V_H$ $0.4V \geq V_L$	$V_H \geq V_{EE} + 2.4V$ $V_{EE} + 0.4V \geq V_L$

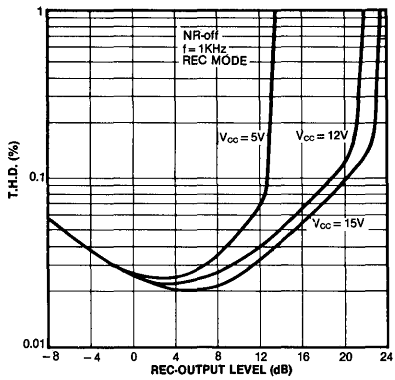
3) REFERENCE LEVEL

The reference output level of Dolby noise reduction system is defined as Dolby level. The Dolby level of KA22711 is 245mV (−10dBm) at f = 400Hz.

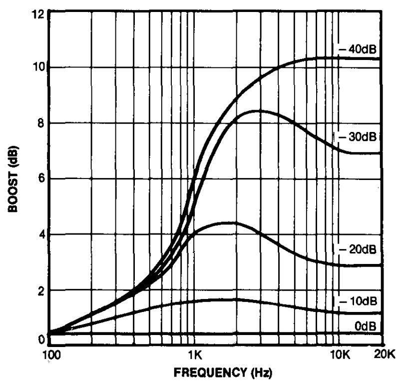
CIRCUIT CURRENT



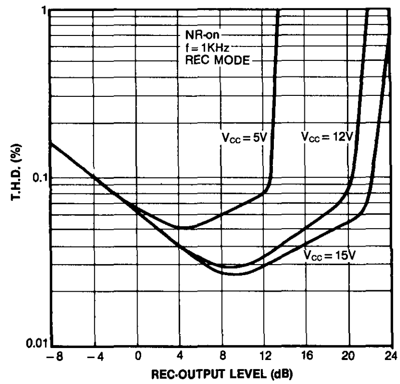
TOTAL HARMONIC DISTORTION (REC)



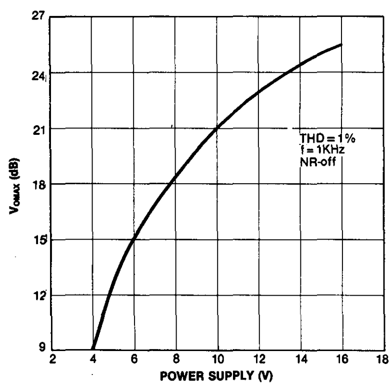
REC (ENCODE) CHARACTERISTIC



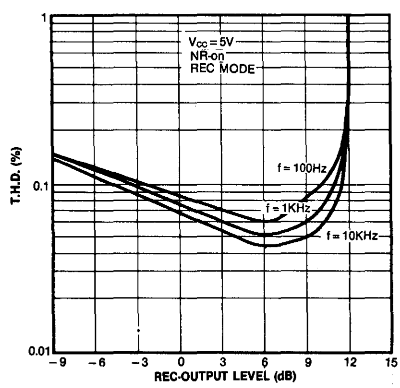
TOTAL HARMONIC DISTORTION (REC)



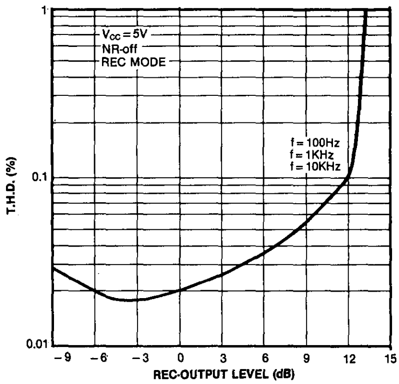
MAX REC-OUTPUT LEVEL



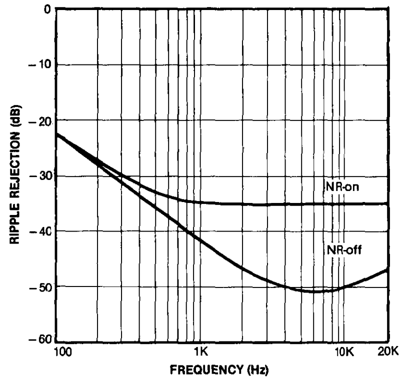
TOTAL HARMONIC DISTORTION (REC)



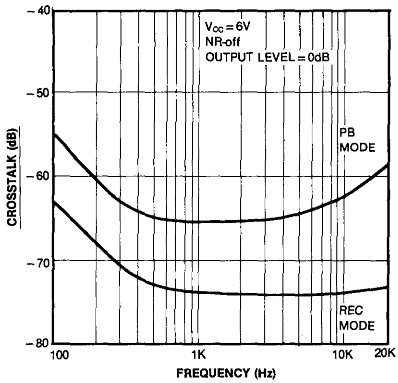
TOTAL HARMONIC DISTORTION (REC)



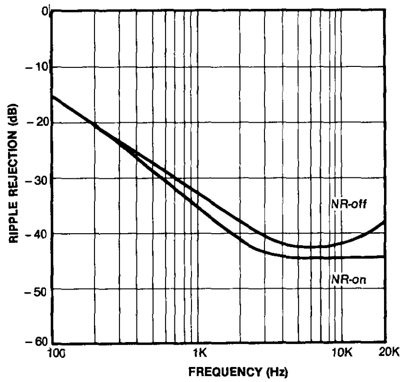
RIPPLE REJECTION (REC)



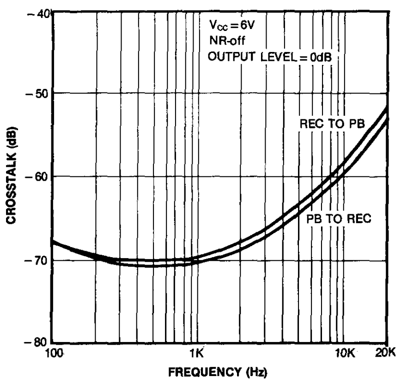
CROSSTALK (CH TO CH)



RIPPLE REJECTION (PB)



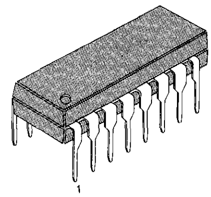
CROSSTALK (BETWEEN REC TO PB)



DOLBY* B-TYPE NOISE REDUCTION PROCESSOR

The KA22712 is a monolithic integrated circuit designed for use in Dolby*B-type noise reduction systems.

16 DIP



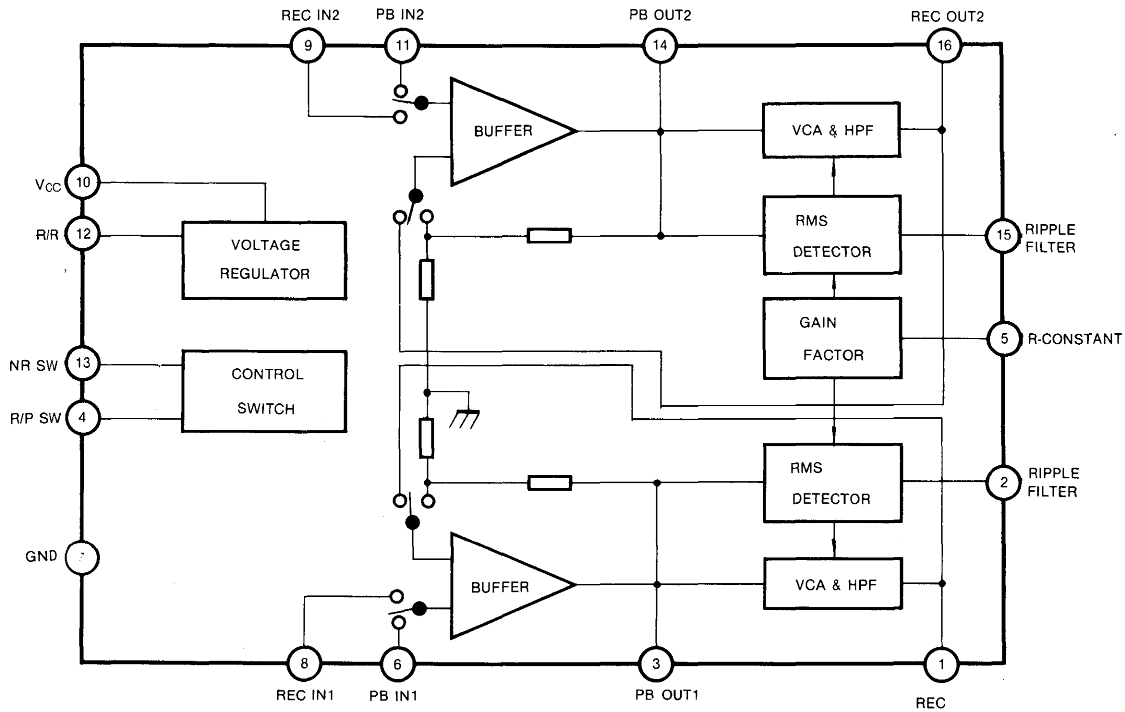
FEATURES

- Few external components
- Low power consumption (typ I_{CC} = 4.5mA)
- High crosstalk rejection ratio
- Built in NR-switch, REC/PB-switch
- Recommended supply voltage: 6.5V ~ 16V

ORDERING INFORMATION

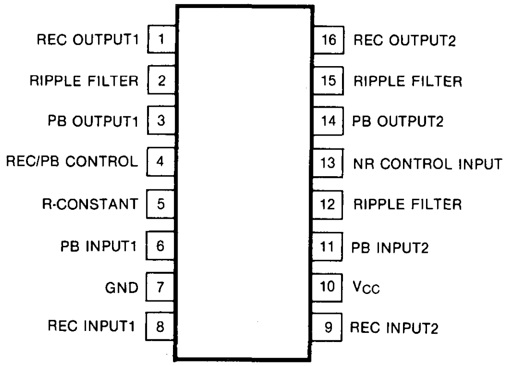
Device	Package	Operating Temperature
KA22712	16 DIP	− 30 ~ + 85°C

BLOCK DIAGRAM



*; "Dolby" and double-D symbol are trademarks of Dolby Laboratories Licensing Corporation.
This I.C. is available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, from whom licensing and application information must be obtained.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_d	750	mW
Operating Temperature	T_{opr}	−30~ +85	°C
Storage Temperature	T_{stg}	−40~ +125	°C

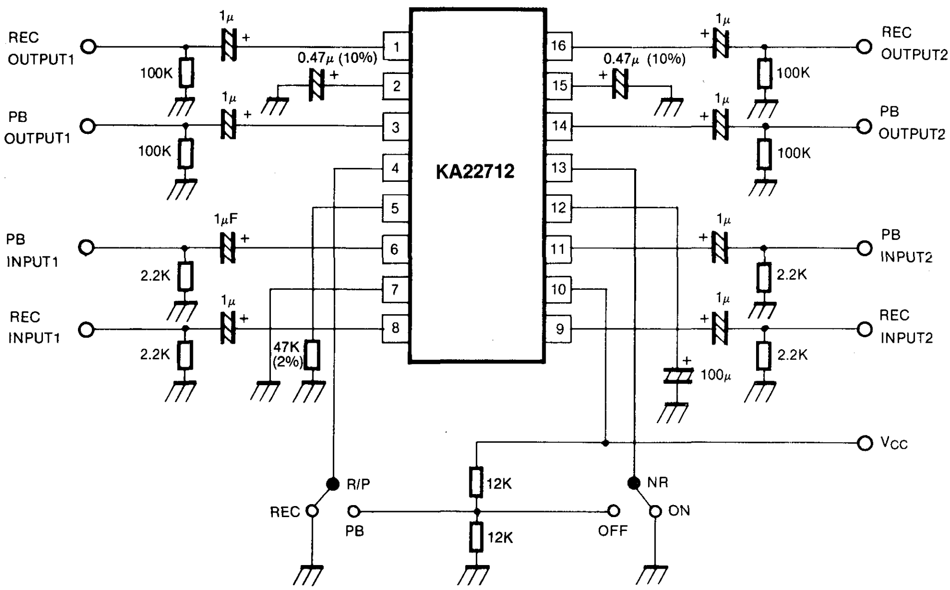
Note: Derated above Ta = 25°C in the propation of 10mW/°C

ELECTRICAL CHARACTERISTICS

($T_a = 25°C$, $V_{CC} = 9V$, f = 1KHz, 0dB = 245mV (−10dBm) at REC OUT, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Circuit Current	I_{CC}	REC mode, NR-off, $V_{IN} = 0$	3.5	4.5	6	mA
Buffer Voltage Gain	A_V	REC mode, PBout = 0dB	22	24	26	dB
NR-REC Boost	BST	RECout = −25dB, f = 500Hz	1.4	2.9	4.4	dB
		RECout = −25dB, f = 2KHz	5.5	7.0	8.5	dB
		RECout = −25dB, f = 5KHz	3.9	5.4	6.9	dB
		RECout = −40dB, f = 10KHz	9.1	10.4	11.9	dB
		RECout = 0dB, f = 10KHz	−1.1	0.4	1.9	dB
NR-Boost Balance	BL	NR-REC boost CH to CH ratio		0	1	dB
MAX. RECout level	$V_{o(max)}$	REC mode, NR-off THD = 1%	14	16		dB
RECout Distortion	THD	REC mode, NR-off RECout = 10dB		0.04	0.1	%
		REC mode, NR-on RECout = 10dB		0.04	0.1	%
NR-effect S/N	S/N	REC mode, Rg = 2.2K Filter = CCIR/ARM	65	69		dB
Crosstalk	CT	NR-off OUTPUT = 0dB PB to REC		−75	−65	dB
		CH to CH, NR-off OUTPUT = 0dB		−68	−62	dB
Input Impedance	Zin		30	47	60	KΩ
Switch Control Voltage	VC	High mode	2.4			V
		Low mode	0		0.4	V
Input Level	REC Vi	REC mode, NR-off RECout = 0dB	19.5	24.5	31.0	mV
	PB Vi	PB mode, NR-off RECout = 0dB	19.5	24.5	31.0	mV
Output Level	Vout	REC mode, NR-off RECout = 0dB Testpoint = PB output	346	388	436	mV

TEST CIRCUIT

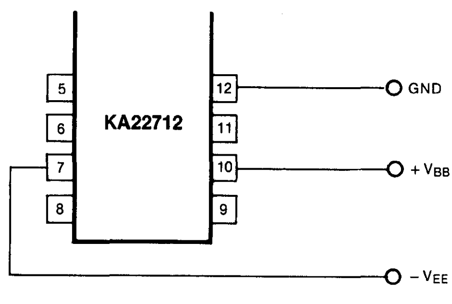


3

APPLICATION NOTE

1) POWER SUPPLY

The KA22712 can be operated at 6.5V—16V in case of single and ±3.25V– ±8V in dual power supply.



Dual power connection

2) SWITCH CONTROL VOLTAGE

All function of KA22712 are controlled by internal electronič switches. The function switch is operated by D.C. voltage of NR and R/P control pins.

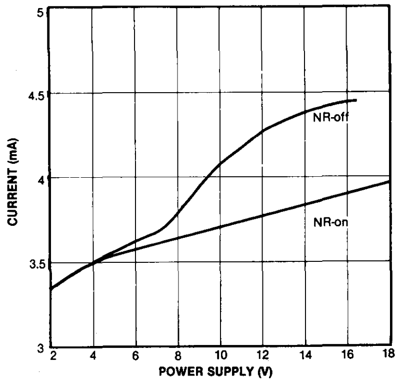
NR, R/P	V_H	V_L
Condition	PB	REC
	NR-off	NR-on

Single Power	Dual Power
$2.4V \leq V_H$ $0.4V \geq V_L$	$V_H \geq V_{EE} + 2.4V$ $V_{EE} + 0.4V \geq V_L$

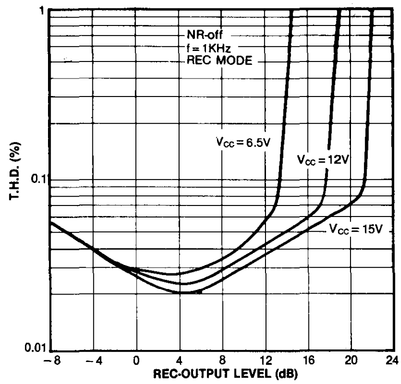
3) REFERENCE LEVEL

The reference output level of Dolby noise reduction system is defined as Dolby level. The Dolby level of KA22712 is 245mV (– 10dBm) at f = 400Hz.

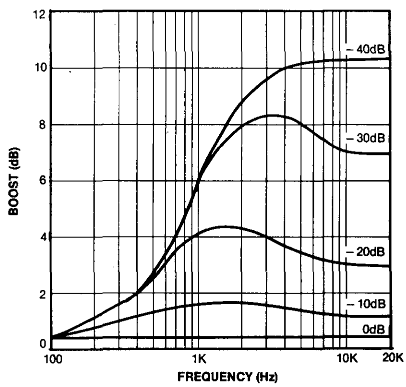
CIRCUIT CURRENT



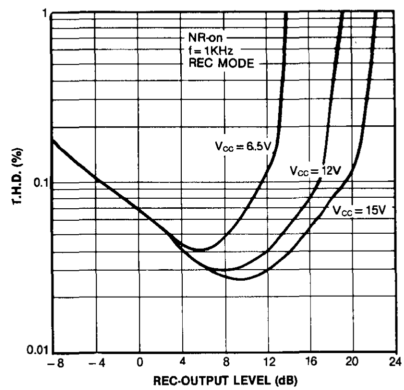
TOTAL HARMONIC DISTORTION (REC)



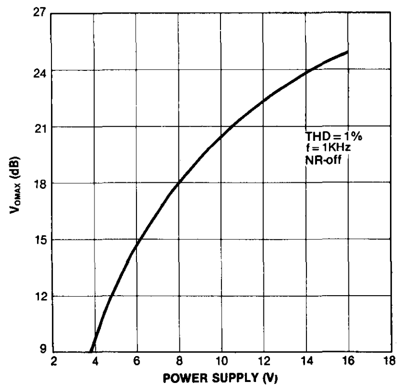
REC (ENCODE) CHARACTERISTIC



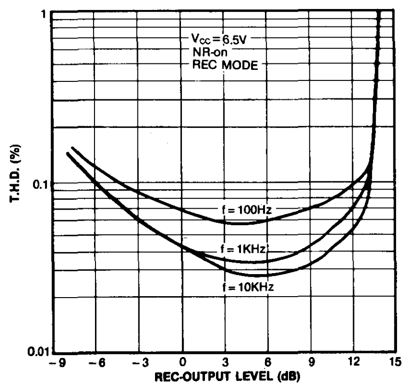
TOTAL HARMONIC DISTORTION (REC)



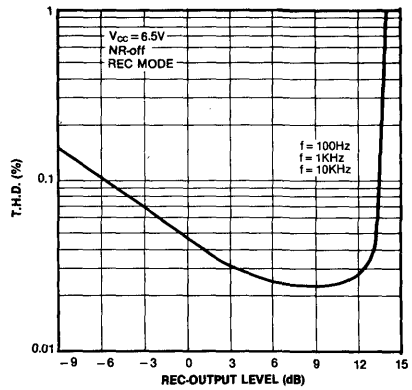
MAX REC-OUTPUT LEVEL



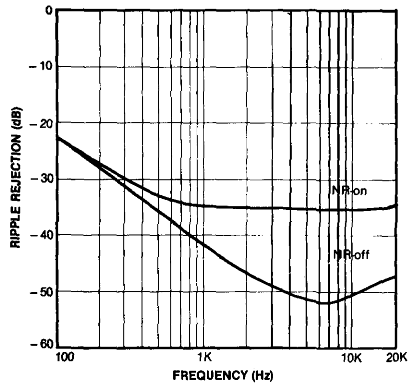
TOTAL HARMONIC DISTORTION (REC)



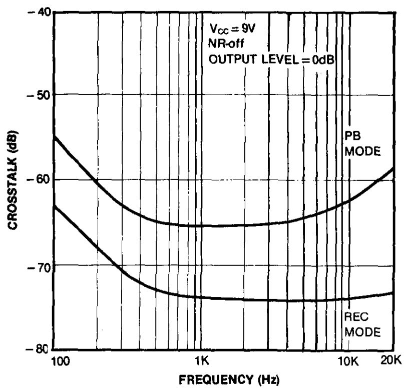
TOTAL HARMONIC DISTORTION (REC)



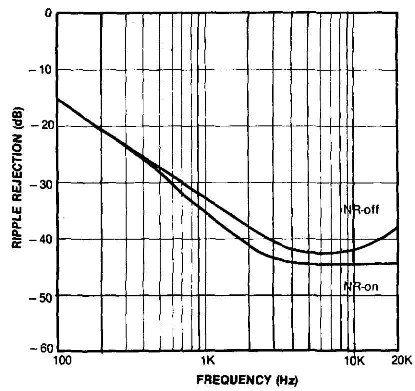
RIPPLE REJECTION (REC)



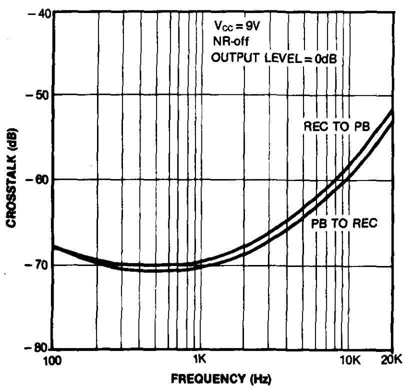
CROSSTALK (CH TO CH)



RIPPLE REJECTION (PB)



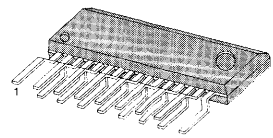
CROSSTALK (BETWEEN REC TO PB)



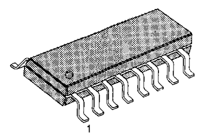
FM NOISE CANCELLER

The KA2272 is a monolithic integrated circuit for the FM noise canceller used in car stereos.
It is used in combination with a PLL FM multiplex demodulator (such as the KA2266) with a pilot signal canceller.

16 ZSIP



16 SOP



FEATURES

- **Operation voltage range: 8V ~ 15V**
- **Low power dissipation**
- **Low distortion: THD = 0.02% at V_i = 300mV**
- **Pilot signal compensation**
- **The space factor is advantageous because of the signal-end-package.**
- **Built-in monostable multivibrator.**
- **Variable input type noise AGC system.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2272	16 ZSIP	−20 ~ +75°C
KA2272D	16 SOP	

BLOCK DIAGRAM

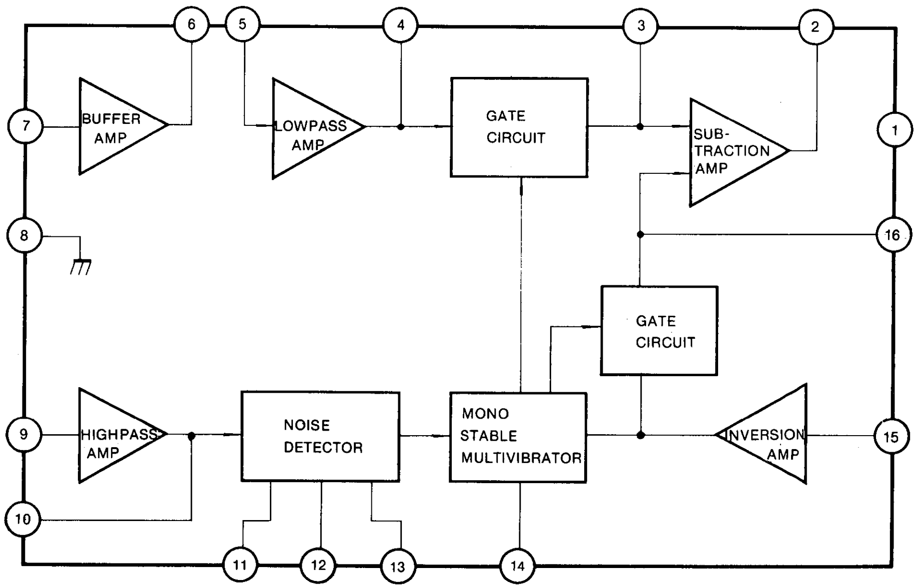


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic		Symbol	Value	Unit
Supply Voltage		V_{CC}	16	V
Power Dissipation	KA2272	P_d	450	mW
	KA2272D		300	mW
Operating Temperature		T_{opr}	−20 ~ +75	°C
Storage Temperature		T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 12V, V_7 = 300mV, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
		Input Pin	Output Pin				
Circuit Current	I_{CC}				16	25	mA
Voltage Gain	A_V	V_7 = 300mV, f = 1KHz	Output	−0.2	0.8	1.8	dB
Output Voltage	V_O	V_7, f = 1KHz	Output THD = 1%	1.3			V
Total Harmonic Distortion	THD	V_7 = 300mV, f = 1KHz	Output		0.01	0.03	%
Input Resistance	R_I	V_7 = 300mV, f = 1KHz		36	51	67	KΩ
Lowpass AMP Gain	A_{VL}	V_5 = 300mV, f = 1KHz	V_4	0	0.83	1.58	dB
Highpass AMP Gain	A_{VH}	V_9 = 100mV f = 200KHz	V_{10}	1.58	2.92	4.35	dB
Inverted Amp Distortion	THD_I	f = 19KHz	Output			0.1	%
Inverted Amp Dynamic Range	Vo_I	V_{15} = 100mV f = 19KHz	Output THD = 1%	300			mV
Inverted Amp Gain	A_{VI}	V_{15} = 100mV f = 19KHz	Output	0	2.28	4.08	dB
Output Noise Voltage	V_{NO}	Bypass V_7, V_{15} to GND	Output, 100KHz LPF		30	60	μV
Gate Time	T_G	V_7 = 100m$V_{p\text{-}p}$, 1μs, f = 1KHz	Output	13	21	30	μsec
Noise Sensitivity	SN	V_7, 1μs, f = 1KHz	Output			30	m$V_{p\text{-}0}$

TEST CIRCUIT

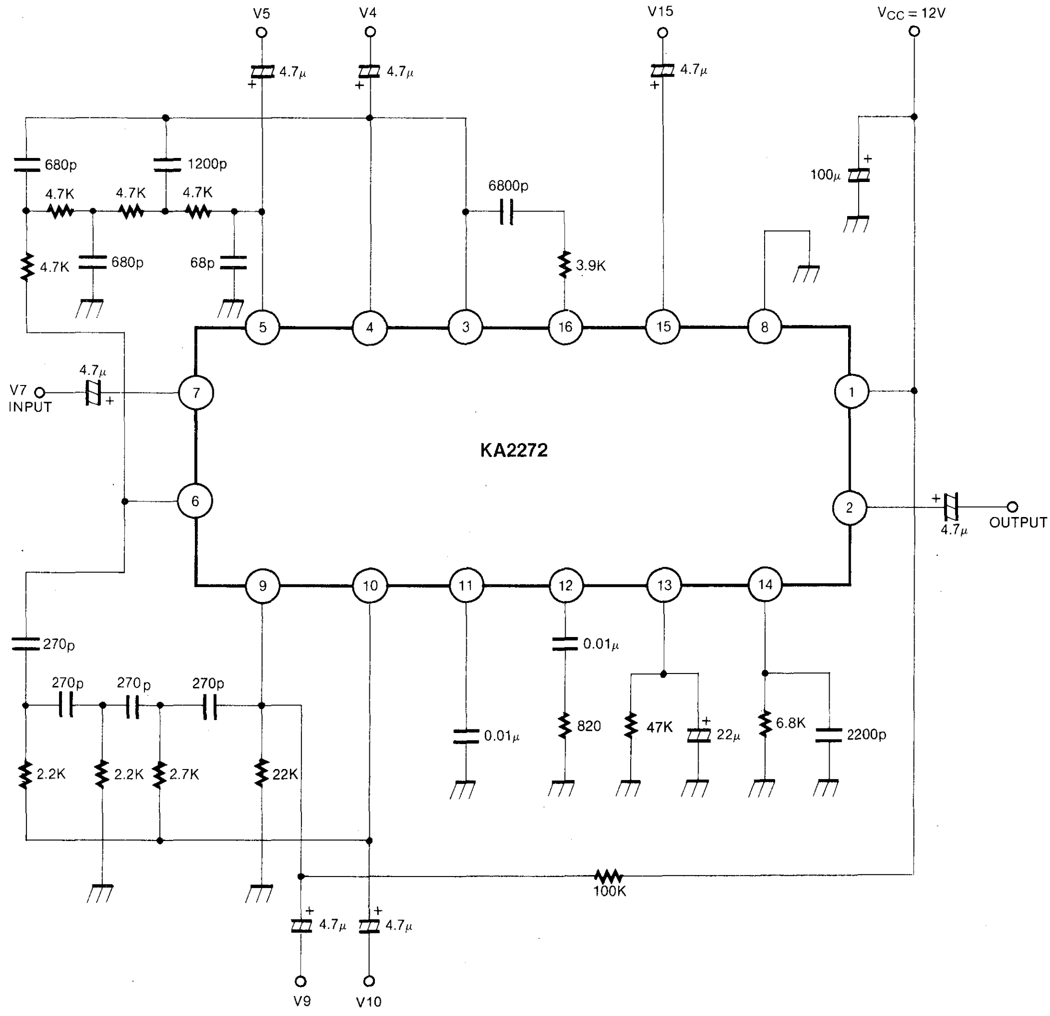


Fig. 2

APPLICATION CIRCUIT

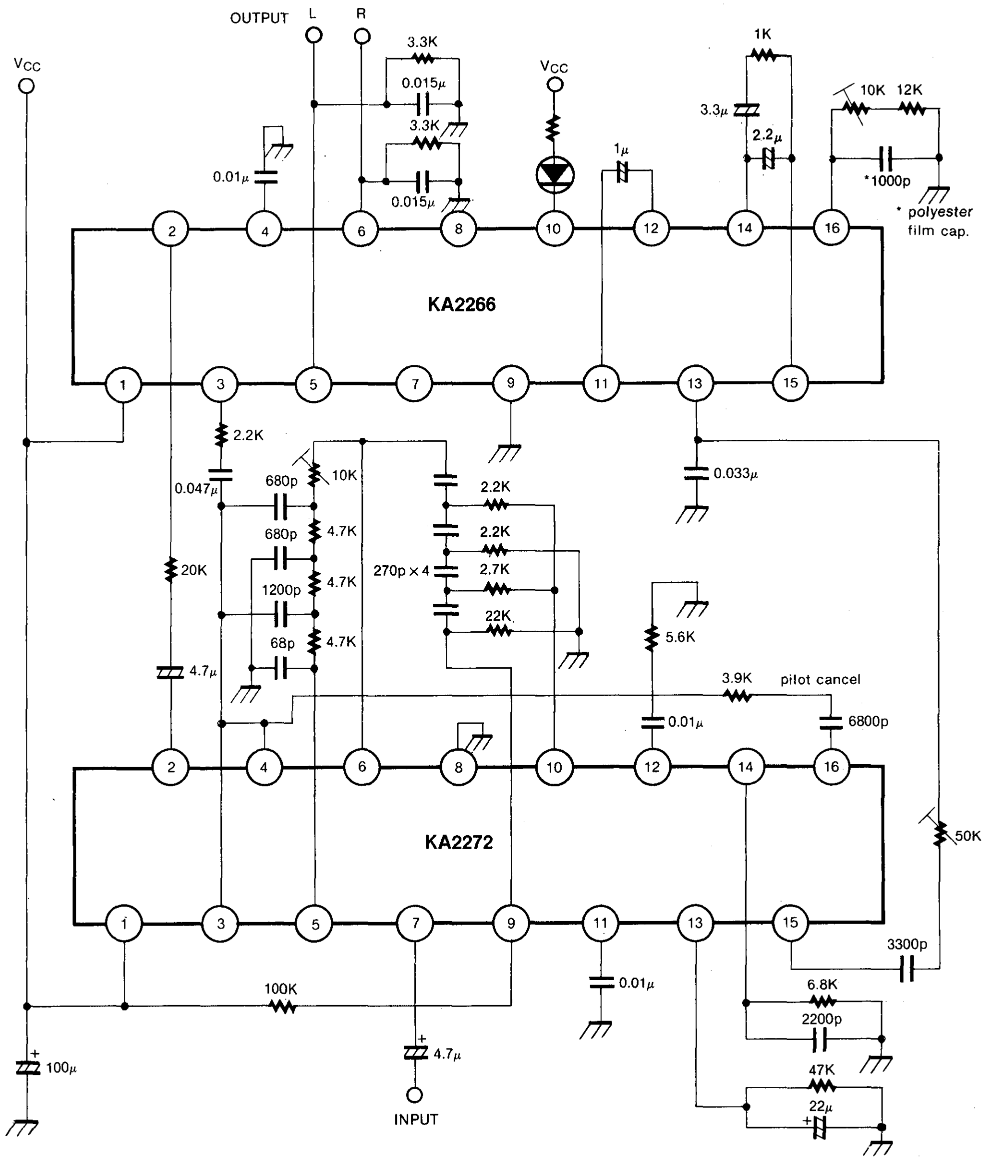
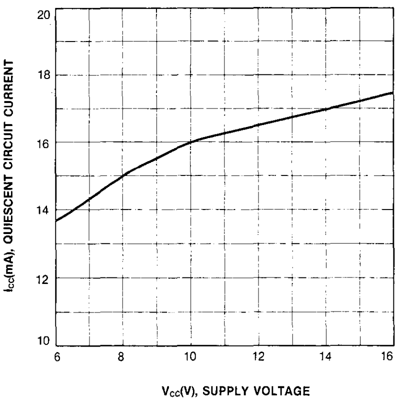
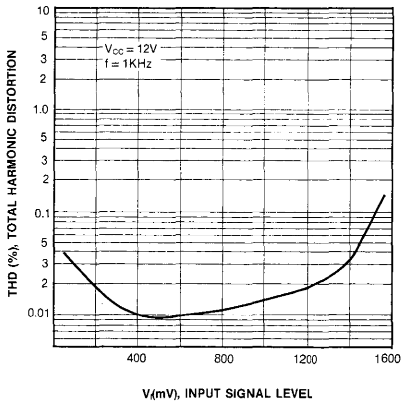


Fig. 3

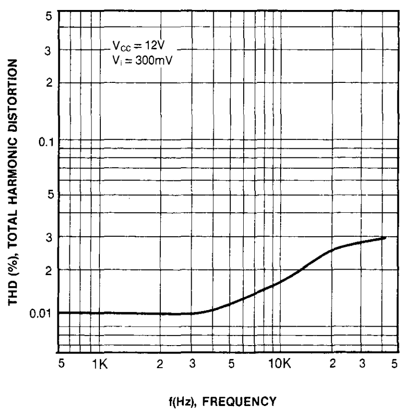
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



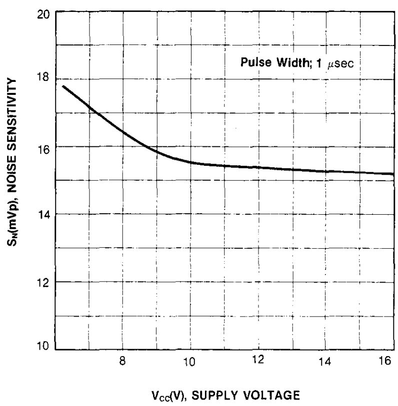
TOTAL HARMONIC DISTORTION-INPUT SIGNAL LEVEL



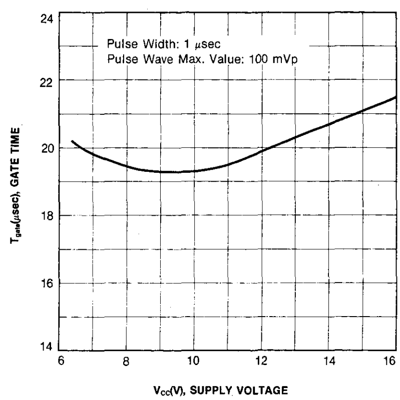
TOTAL HARMONIC DISTORTION-FREQUENCY



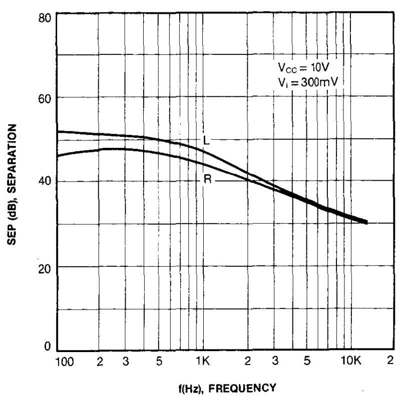
NOISE SENSITIVITY-SUPPLY VOLTAGE



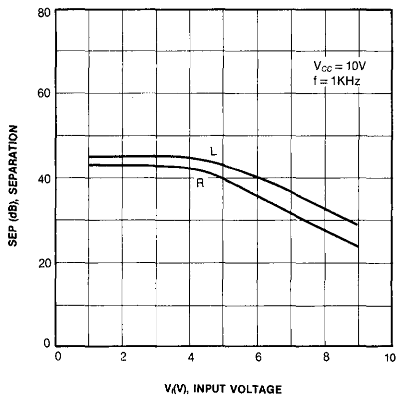
GATE TIME-SUPPLY VOLTAGE



SEPARATION-FREQUENCY



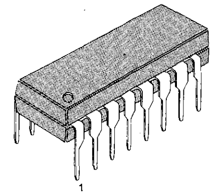
SEPARATION-INPUT VOLTAGE



5-DOT DUAL LED LEVEL METER DRIVER

The KA2281 is a monolithic integrated circuit consisting of a 2-channel LED level meter driver which was designed for use in stereo radio cassette tape recorders and home stereos.

16 DIP



FEATURES

- Comparator AC level (−16, −11, −6, −3, 0dB)×2.
- Capable of driving red/green/yeollow LEDs.
- Externally adjustable gain of input amplifier.
- Wide operating supply voltage range (5V ~ 14V).
- 10-dot dual output combinated with the KA2283.
- Applicable to 10-dot mono output.
- High input impedance.
- A minimum number of external parts required.

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2281	16 DIP	−20 ~ +70°C
KA2281G	PELLET	

TYPICAL APPLICATION CIRCUIT

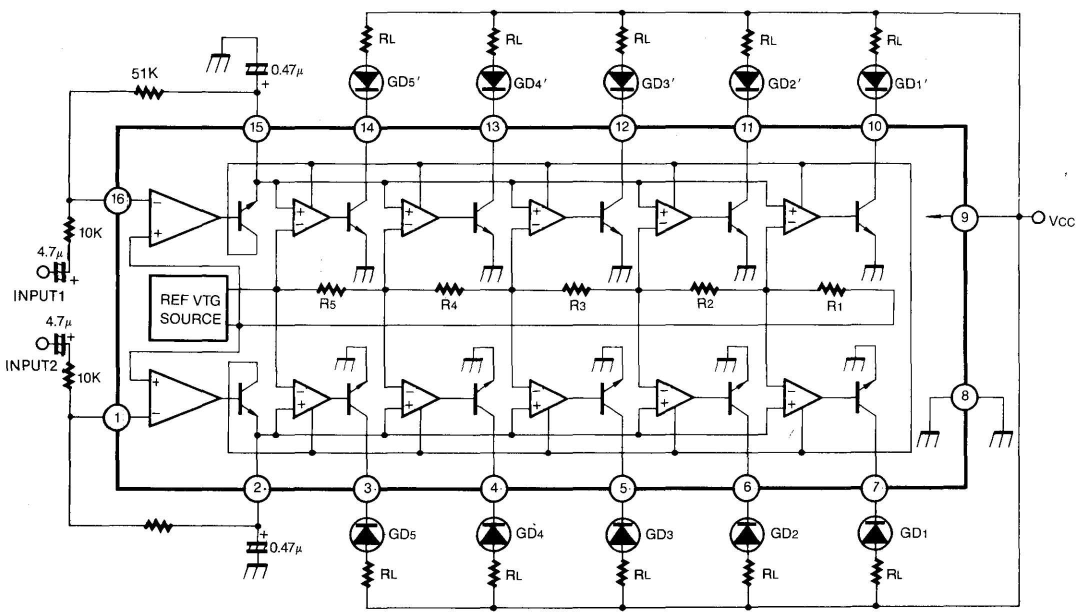


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
D Terminal Output Current	I_D	30	mA
Power Dissipation	P_d	600	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =12V, f=1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i =0		4		mA
D Terminal ON Voltage	V_{OL}	I_O =20mA		1.5		V
D Terminal Leakage Current	I_O (off)	V_i =0			50	μA
Voltage Gain (Closed Loop)	A_V			13.4		dB
Comparator ON Level	GD_5 GD_5'	A_V =13.4dB	−1	0	1	dB
	GD_4 GD_4'		−4	−3	−2	
	GD_3 GD_3'		−7.5	−6	−4.5	
	GD_2 GD_2'		−13	−11	−9	
	GD_1 GD_1'		−19	−16	−13	
LED ON Level Difference	$\Delta GD_{1\text{-}5}$	$GD_{1\text{-}5}$-$GD'_{1\text{-}5}$ A_V = 13.4dB	−1	0	1	dB
Input Impedance of Amp	R_i			200		KΩ

* Definition of 0dB: when the value of Input voltage is 218mVrms

TYPICAL APPLICATIONS

1. 5-dot dual application

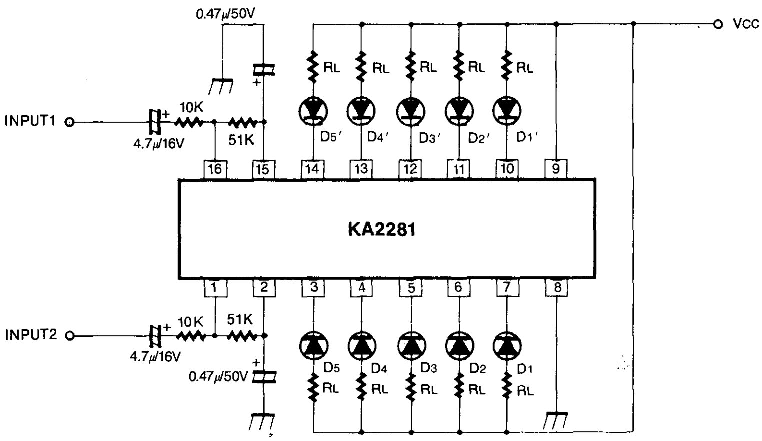


Fig. 2

2. 10-dot mono application

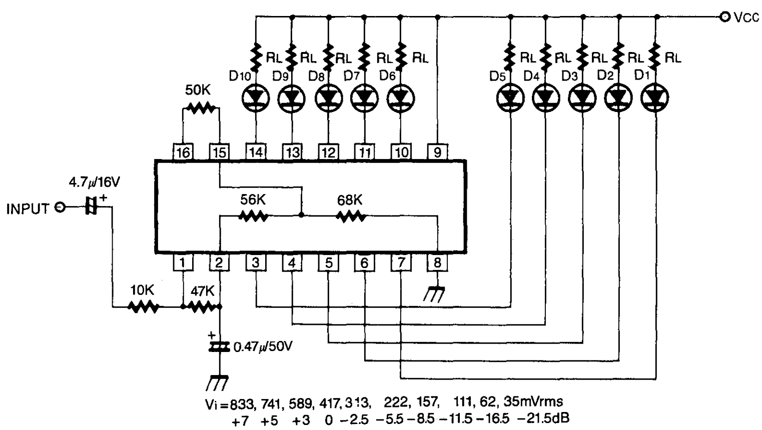
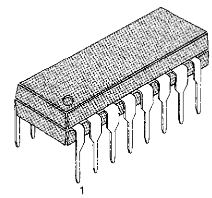


Fig. 3

5-DOT DUAL LED LEVEL METER DRIVER

The KA2283 is a monolithic integrated circuit consisting of a 2-channel LED level meter driver which was designed for use in stereo radio cassette tape recorders and home stereos.

16 DIP



FEATURES

- **Suitable for AC level meter driver.**
- **Comparator level (−8, −6, −4, −2, 0dB)×2.**
- **Capable of driving red/green/yellow LEDs.**
- **Externally adjustable gain of input amp.**
- **Wide operating supply voltage range (5V ~ 14V).**
- **10-dot dual output combinated with KA2281.**
- **Applicable to 10 dot mono output.**
- **High input inpedance.**
- **A minimum number of external parts required.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2283	16 DIP	−20 ~ +70°C

BLOCK DIAGRAM

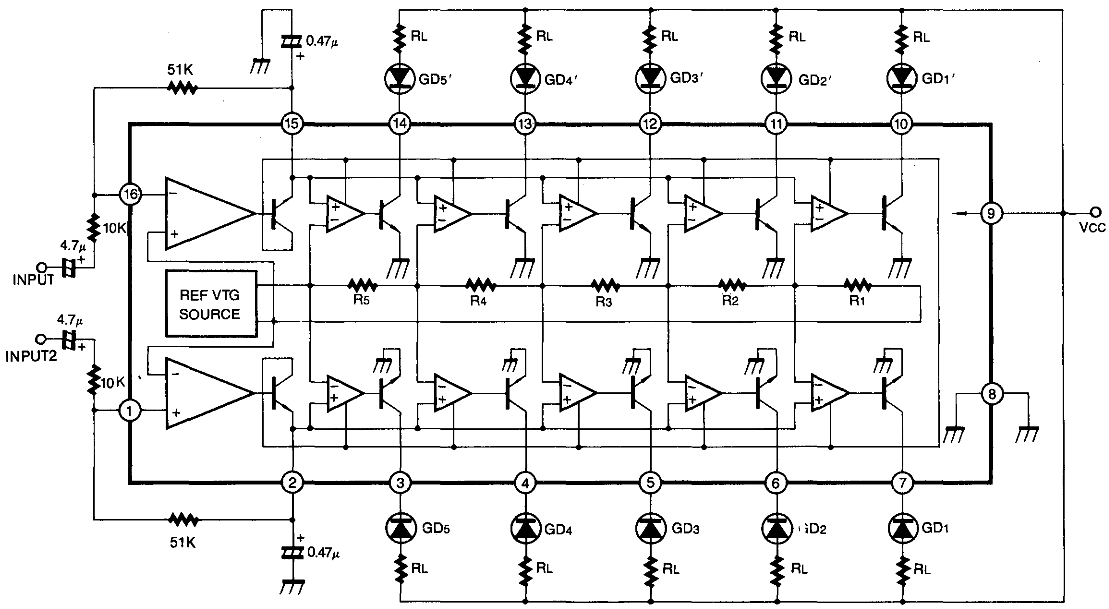


Fig. 1

3

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
D Terminal Output Current	I_D	30	mA
Power Dissipation	P_d	600	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=12V, f=1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	V_i=0		4		mA
D Terminal ON Voltage	V_{OL}	I_O=20mA		1.5		V
D Terminal Leakage Current	I_O (off)	V_i=0			50	μA
Voltage Gain (Closed Loop)	A_V			13.4		dB
Comparator ON Level	GD_5 GD_5'	A_V=13.4dB	−1	0	1	dB
	GD_4 GD_4'		−3	−2	−1	
	GD_3 GD_3'		−5	−4	−3	
	GD_2 GD_2'		−7	−6	−5	
	GD_1 GD_1'		−9	−8	−7	
LED ON Level Difference	ΔGD_{1-5}	GD_{1-5}-GD'_{1-5} A_V=13.4dB	−1	0	1	dB
Input Impedance of Amp	R_i			200		KΩ

* Definition of 0dB: when the value of Input voltage is 218mVrms

APPLICATION CIRCUIT

1. 5-dot dual application

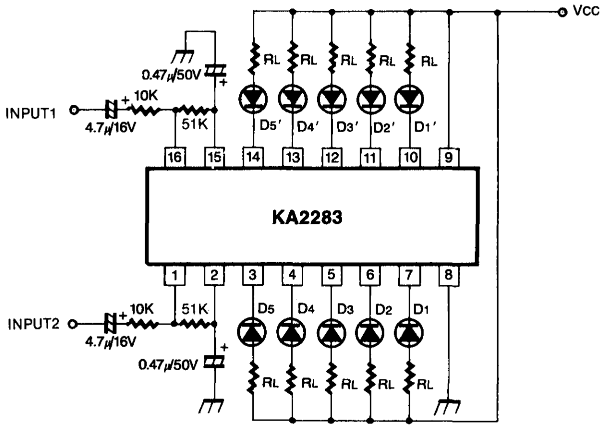
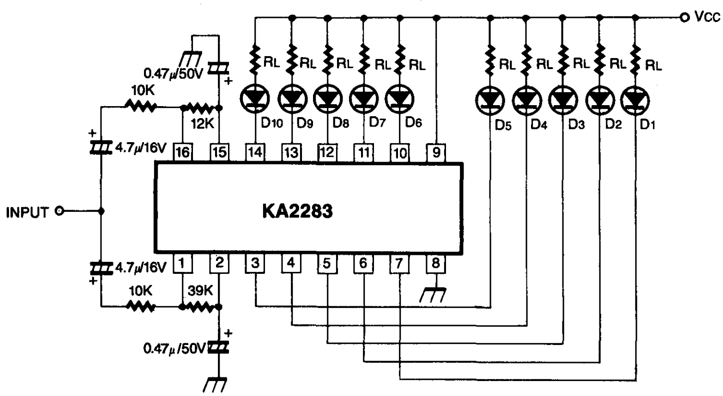


Fig. 2

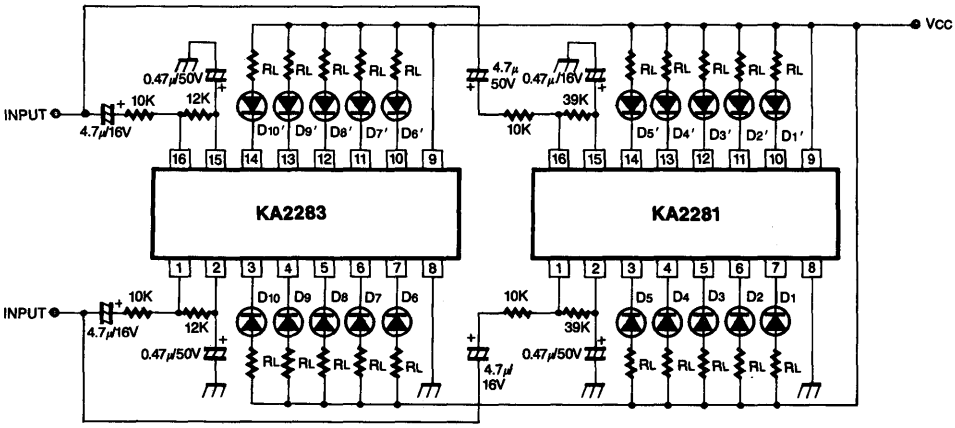
2. 10-dot mono application



Vi =822, 653, 519, 412, 327, 260, 206, 163, 129, 102mVrms
+6, +4, +2, 0. −2, −4, −6, −8, −10, −12dB

Fig. 3

3. 10-dot dual application with KA2281



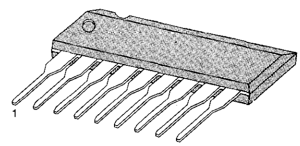
Vi =830, 660, 524, 417, 331, 263, 184, 130, 73, 41mVrms
+6, +4, +2, 0. −2, −4, −7, −10, −15, −20dB

Fig. 4

5-DOT DUAL LED LEVEL METER DRIVER

The KA2284/KA2285 are a monolithic integrated circuits designed for 5-dot LED level meter drivers with a built-in rectifying amplifier; it is suitable for AC/DC level meters such as VU meters or signal meters.

9 SIP



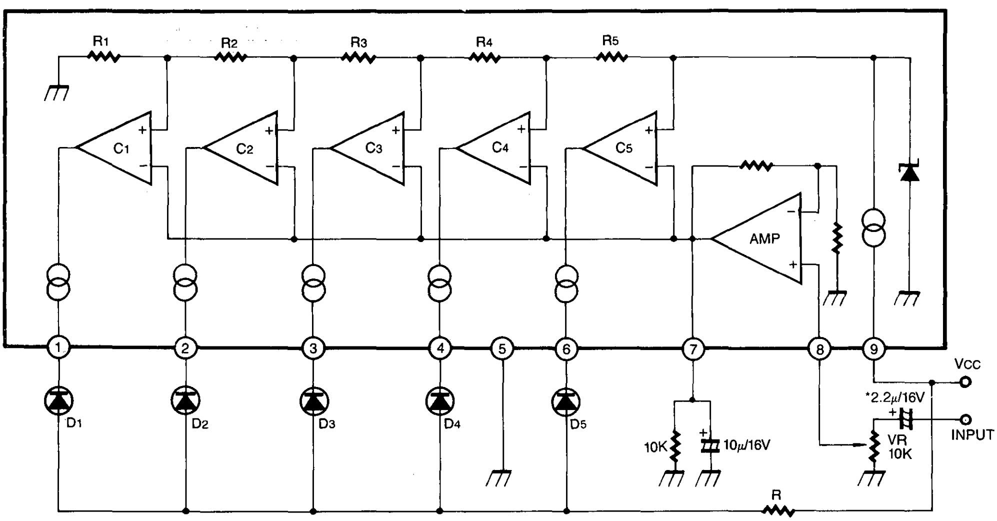
FEATURES

- **High gain rectifying amplifier included (A_V=26dB).**
- **Low radiation noise when LED turns on.**
- **Logarithmic indicator for 5-dot LED of bar type. (−10, −5, 0, 3, 6dB)**
- **Constant current output.**
  KA2284: I_o=15mA Typ.
  KA2285: I_o=7mA Typ.
- **Wide operating supply voltage range (3.5V ~ 16V).**
- **Minimum number of external parts required.**

ORDERING INFORMATION

Device	Package	Operating Temperature	I_D
KA2284	9 SIP	−20 ~ +80°C	15 mA
KA2285			7 mA

BLOCK DIAGRAM



*Capacitor to be omitted when used as a DC input signal meter

Fig. 1

3

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Amp Input Voltage	V_{8-5}	$-0.5 \sim V_{CC}$	V
Pin 7 Voltage	V_{7-5}	6	V
D Terminal Output Voltage	V_D	18	V
Circuit Current	I_{CC}	12	mA
D Terminal Output Current	I_D	20	mA
Power Dissipation	P_d	1100	mW
Operating Temperature	Topr	$-20 \sim +80$	°C
Storage Temperature	Tstg	$-40 \sim +125$	°C

−11mW/°C is decreased at higher temperature than T_a =25°C.

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =6V, f=1KHz, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Circuit Current		I_{CC}	V_i =0V		6	8.5	mA
D Output Current	KA2284	I_O	V_i =0.15V	11	15	18.5	mA
	KA2285			5	7	9.5	
Input Bias Current		I_8		−1		0	μA
Amp Gain		A_V	V_i =0.1V	24	26	28	dB
Comparator ON Level		GD_1		−12	−10	−8	dB
		GD_2		−6	−5	−4	
		GD_3			0		
		GD_4		2.5	3	3.5	
		GD_5		5	6	7	

* Definition of 0dB: input voltage level when GD_3 turn ON. (50mV)

TYPICAL APPLICATION CIRCUIT

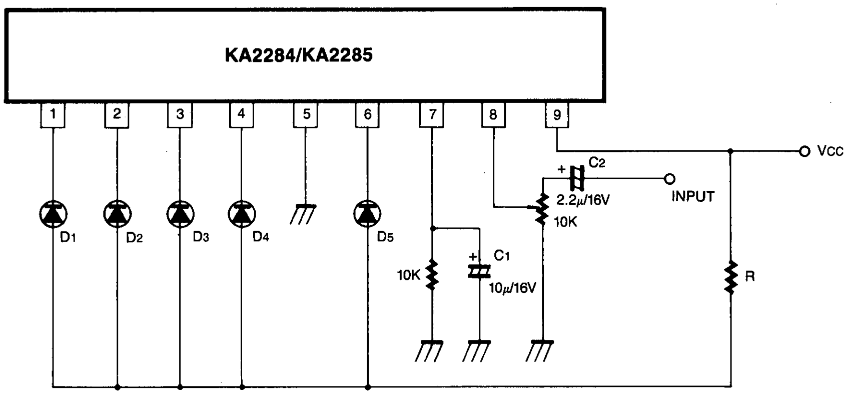


Fig. 2

C2: AC in, 2.2μ is used.
DC in, 2.2μ is shorted

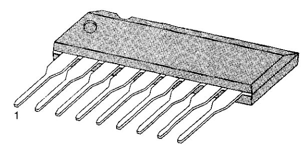
The recommended value of R at T_a (max)=60°C.

V_{CC} (V)	8 ~ 12	10 ~ 14	12 ~ 16
R (Ω)	47	68	91

By changing the time constant C_1 and C_2, the response, attack and release time, may be varied. In the above application conditions, power dissipation may be operated at higher levels than the absolute maximum ratings. The wattage of R is to be determined by the total LED current and R value recommended by the R table.

5-DOT LED LINEAR LEVEL METER DRIVER

The KA2286/KA2287 are a monolithic integrated circuit designed for 5-dot LED level meter drivers with a built-in rectifying amplifier; it is suitable for AC/DC level meters such as VU meters or signal meters.



FEATURES

- **High gain rectifying amplifier included (A_v=26dB).**
- **Low radiation noise when LED turns on.**
- **Linear indicator for 5-dot LED of bar type. (0.33, 0.67, 1, 1.33, 1.67)**
- **Constant current output.**
  KA2286: I_o=7mA Typ.
  KA2287: I_o=15mA Typ.
- **Wide operating supply voltage range (3.5V ~ 16V).**
- **Minimum number of external parts required.**

ORDERING INFORMATION

Device	Package	Operating Temperature	I_D
KA2286	9 SIP	−20 ~ +80°C	7 mA
KA2287			15 mA

BLOCK DIAGRAM

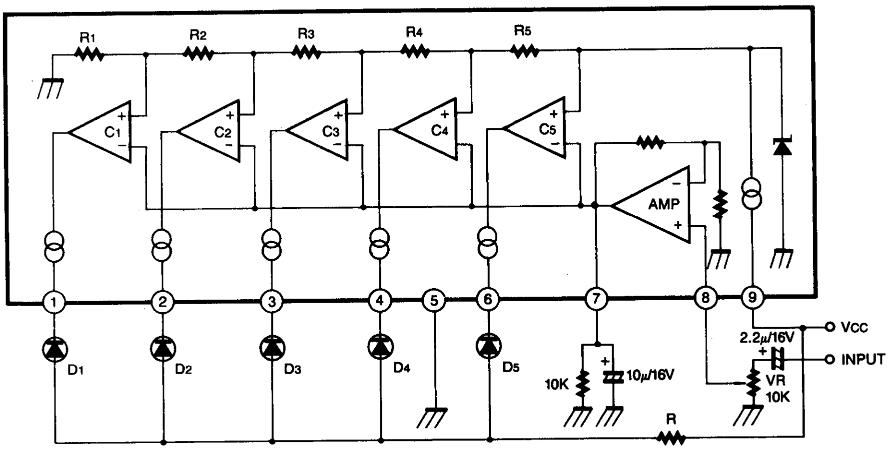


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Amp Input Voltage	V_{8-5}	$-0.5 \sim V_{CC}$	V
Pin 7 Voltage	V_{7-5}	6	V
D Terminal Output Voltage	V_D	18	V
Circuit Current	I_{CC}	12	mA
D Terminal Output Current	I_D	20	mA
Power Dissipation	P_d	1100	mW
Operating Temperature	Topr	$-20 \sim +80$	°C
Storage Temperature	Tstg	$-40 \sim +125$	°C

-11mW/°C is decreased at higher temperature than T_a=25°C.

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=6V, f=1KHz, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current		I_{CC}	V_i=0V		6	8.5	mA
D Output Current	KA2286	I_O	V_i=0.15V	5	7	9.5	mA
	KA2287			11	15	18.5	
Input Bias Current		I_8		-1		0	μA
Amp Gain		A_V	V_i=0.1V	24	26	28	dB
Comparator On Level		GD_1		0.28	0.33	0.40	V_3
		GD_2		0.59	0.67	0.75	
		GD_3			1		
		GD_4		1.25	1.33	1.42	
		GD_5		1.48	1.67	1.87	

* Definition of 1; Pin 3 voltage when GD_3 turn on. (65mV)

TYPICAL APPLICATION CIRCUIT

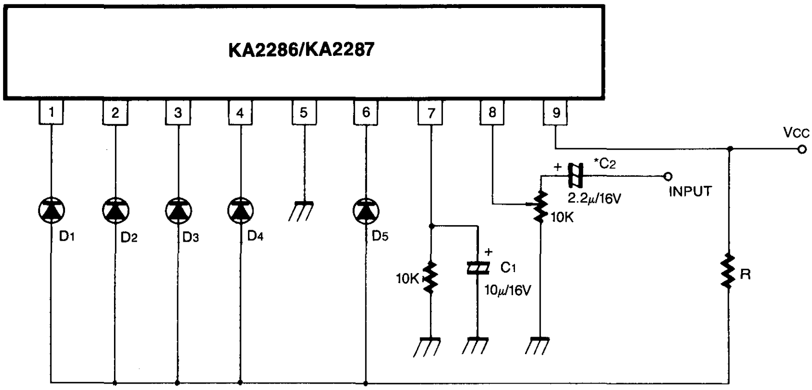


Fig. 2

*C2: AC in, 2.2μ is used
DC in, 2.2μ is shorted

The recommended value of R at T_a (max)=60°C.

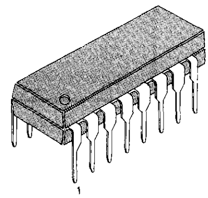
V_{CC} (V)	8~12	10~14	12~16
R (Ω)	47	68	91

By changing the time constant C_1 and C_2, the response, attack and release time may be varied. In the above application conditions, power dissipation may be operated at higher levels than the absolute maximum ratings. The wattage of R is to be determined by the total LED current and R value recommended by the R table.

7-DOT LED LEVEL METER DRIVER

The KA2288 is a monolithic integrated circuit consisting of 7-dot LED level meter drivers. The KA2288 employs a low noise comparator which provides 10dB lower noise in the LW, MW band than the previously mentioned LED drivers.

16 DIP



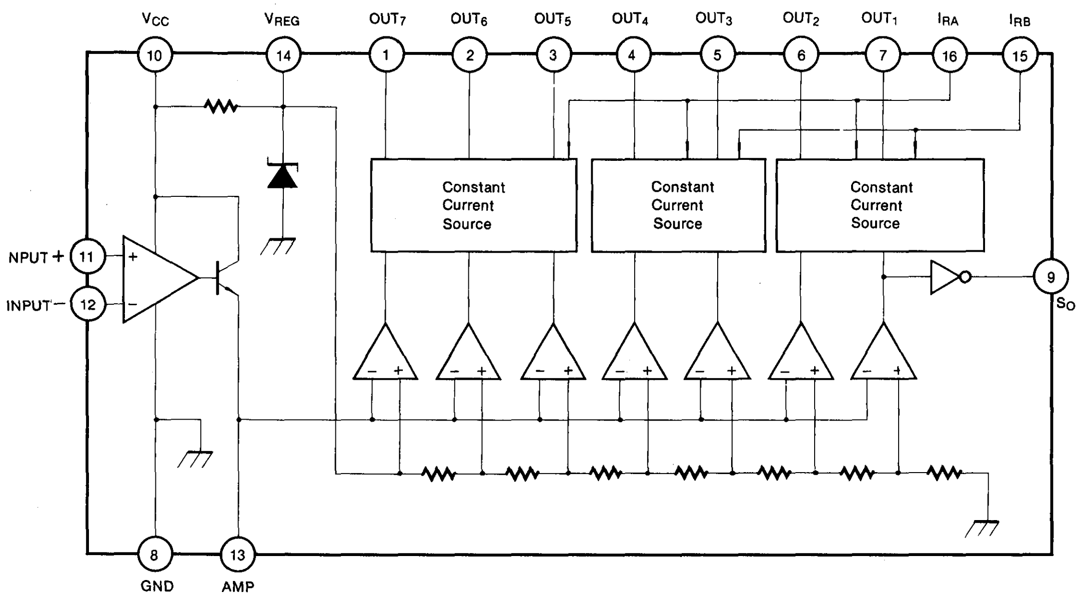
FEATURES

- **LED current can be set by an external resistor**
- **Internal detection amplifier**
- **Internal voltage regulator**
- **Constant current output**
- **Fitted with a signal detect output pin**
- **VU meter scale**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2288	16 DIP	−20 ~ +70°C

BLOCK DIAGRAM



3

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Input Voltage (AMP)	V_i	$0 \sim V_{CC}$	V
Output Current (AMP)	I_o (AMP)	10	mA
LED Output Current	I_D	30	mA
LED Output Voltage	V_D	V_{CC}	V
Signal Detection Output Current	I_{SO}	10	mA
Input Current	I_{RA}, I_{RB}	10	mA
Reference Voltage Output Current	I_{ref}	10	mA
Power Dissipation	P_d ($Ta \leq +70°C$)	650	mW
Operating Temperature	T_{opr}	$-20 \sim +70$	°C
Storage Temperature	T_{stg}	$-40 \sim +125$	°C

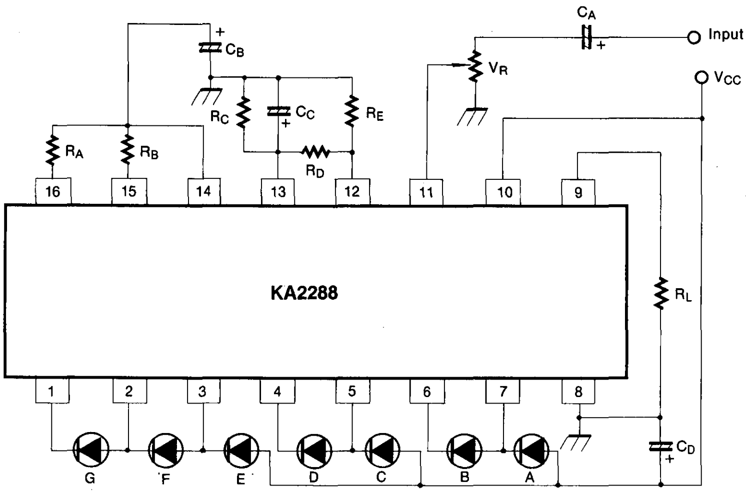
ELECTRICAL CHARACTERISTICS

(Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	$V_{CC} = 12V$, $R_A = 4.7K$, $R_B = \infty$		8	12	mA
Input Bias Current	I_b	$V_{CC} = 12V$		−200	−800	nA
Input Offset Voltage	V_{io}	$V_{CC} = 12V$		2	10	mV
In-Phase Input Voltage	V_{ICM}	$V_{CC} = 12V$	0		10	V
Voltage Gain	A_{VO}	$V_{CC} = 12V$, open loop	50	70		dB
Reference Voltage	V_{ref}	$V_{CC} = 6.2 \sim 16V$, $R_L = 10K$	2.4	2.6	2.9	V
Reference Voltage Fluctuation	$\triangle V_{ref}$	$V_{CC} = 6.2 \sim 16V$, $R_L = \infty \rightarrow 1K$	−0.5	−0.3		V
Signal Detection Output High Level	V_{oh}	$V_{CC} = 12V$, $R_L = 10K$	10	10.3		V
Signal Detection Output Leakage Current	I_{DL}	$V_{CC} = 12V$, $V_{SO} = 0V$			1	μA
Output Current 1	I_o (1)	$V_{CC} = 12V$, $R_A = 10K$, $R_B = \infty$	4.2	7.1	10.0	mA
Output Current 2*	I_o (2)	$V_{CC} = 12V$, $R_A = 10K$, $R_B = 22K$	6.3	10.6	15.0	mA
Output Leakage Current	I_{OL}	$V_{CC} = 12V$, $R_A = 4.7K$, $R_B = \infty$			20	μA
Comparator Level	CL1	$V_{CC} = 6.2V \sim 16V$ CL5 shall be taken for 0dB	−22	−20	−18	dB
	CL2		−11	−10	−9	
	CL3		−6.5	−6	−5.5	
	CL4		−3.5	−3	−2.5	
	CL5			0		
	CL6		+2.5	+3	+3.5	
	CL7		+5	+6	+7	
0dB Level	CL5	$V_{CC} = 6.2 \sim 16V$, $V_{ref} = 2.4 \sim 2.9V$	1.2	1.3	1.45	V

* : Applied pin: 4, 5, 6, 7

TEST CIRCUIT



* **NOTE:** Following values of the elements are for a typical test circuit.
R_C: 18K, R_D: 90K, R_E: 10K, VR: 22K
C_A: 3.3μ, C_B: 10μ, C_C: 4.7μ, C_D: 10μ

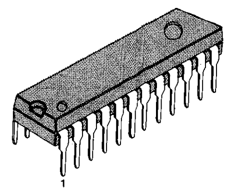
INTRODUCTION TO OPERATION

The KA2288 has 7 built-in comparators to each of which is applied the reference voltage corresponding to each step. (The step for this reference voltage is VU. For the LED switch-over level, refer to the comparator level in the electrical characteristics.)
Each of these comparators compares its reference voltage inherent to the IC and the input DC voltage applied to its input terminal and if the input DC voltage is higher than the internal reference voltage, it will turn on the steady current driver transistor connected to the comparator output to drive the LED.
The output terminal S_o goes "High" when the bottom most LED glows.

AM/FM TUNER + MPX

The KA2292 is a monolithic integrated circuit which consists of a 3V one chip tuner and FM multiplex for AM/FM radios and headphone radios.

24 SDIP



FUNCTIONS

FM Stage : RF/IF/AF amp, Quadrature Detector, MIX, OSC, Tuning Indicator.
AM Stage : RF/IF/AF amp, Detector, MIX, OSC, AGC, Tuning Indicator.
MPX Stage : PLL amp, Decoder, Flip Flop, VCO Stop, Phase Detector, Stereo Indicator.

FEATURES

- **3 V one chip tuner with built-in FM Multiplex**
- **No AM detect coil, IF coupling capacitor, FM IF by-pass capacitor needed.**
- **Built-in tuning indicator function.**
- **Built-in AM/FM selection switch.**
- **Minimum number of external parts required.**
- **Wide operating voltage range: V_{CC} = 1.8 ~ 7V**
- **Low distortion (FM IF: 0.4%, AM IF: 1%, MPX: 0.2% (Typ)).**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2292	24 SDIP	−20 ~ +75°C

BLOCK DIAGRAM

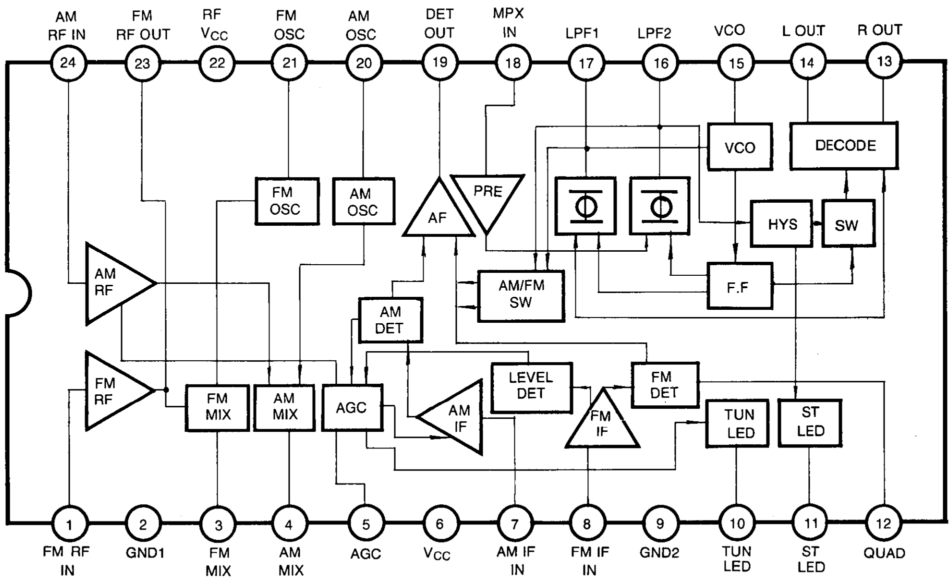


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	8	V
Power Dissipation	P_d	1200	mW
Operating Temperature	T_{opr}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C
LED Drive Voltage	V_{LED}	10	V
LED Drive Current	I_{LED}	10	mA

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 3V, unless otherwise specified)
FM F/E : f = 98MHz, fm = 1KHz, △f = 22.5KHz AM : f = 1MHz, fm = 1KHz, 30% Mod
FM IF : f = 10, 7MHz, fm = 1KHz, △f = 22.5KHz MPX : f = 1KHz, L + R = 90%, P = 10%, V_i = 150mV

	Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit	Test Circuit
	Circuit Current	$I_{CC}(1)$	FM, V_i = 0	8.4	13.2	20.0	mA	1
		$I_{CC}(2)$	AM, F_i = 0	4.4	8.4	13.4	mA	1
F/E	Input Limiting Sensitivity	$V_i(lim)(1)$	V_O = −3dB		10		dBμ	1
	Oscillation Voltage	V_{OSC}	fosc = 98MHz	40	70	110	mV	2
FM IF	Input Limiting Sensitivity	$V_i(lim)(2)$	V_O = −3dB	40	46	53	dBμ	1
	Detector Output Voltage	$V_O(1)$	V_i = 80dBμ	55	80	110	mV	1
	Signal to Noise Ratio	S/N(1)	V_i = 80dBμ	60	70		dB	1
	Total Harmonic Distortion	THD(1)	V_i = 80dBμ		0.4	1	%	1
	AM Rejection Ratio	AMR	V_i = 80dBμ	22	32		dB	1
	Tuning Indication Voltage	$V_L(1)$	I_L = 1mA	45	51	56	dBμ	1
AM IF	Voltage Gain	$A_V(1)$	V_i = 26dBμ	40	70	110	mV	1
	Detector Output Voltage	$V_O(2)$	V_i = 60dBμ	55	80	110	mV	1
	Signal to Noise Ratio	S/N(2)	V_i = 60dBμ	32	42		dB	1
	Total Harmonic Distortion	THD(2)	V_i = 60dBμ		1	2	%	1
	Tuning Indication Voltage	$V_L(2)$	I_L = 1mA	20	25	30	dBμ	1
MPX	Maximum Input Voltage	$V_i(max)$	Stereo, THD = 3%	250	350		mV	1
	Channel Separation	Sep(1)	Stereo, f = 100Hz	32	42		dB	1
		Sep(2)	Stereo, f = 1KHz	32	42		dB	1
		Sep(3)	Stereo, f = 10KHz	32	42		dB	1
	Total Harmonic Distortion	THD(3)	Mono		0.2	1	%	1
		THD(4)	Stereo		0.2	1	%	1
	Voltage Gain	$A_V(2)$	Mono	−5	−3	−1	dB	1
	Channel Balance	CB	Mono	−2	0	2	dB	1
	Lamp on Level	$V_L(on)$	Pilot only		8	16	mV	1
		$V_L(off)$	Pilot only	2	6		mV	1
	Lamp Hysteresis	HY			2		mV	1
	Capture Range	CR	Pilot only	±1	±3	±5	%	1
	Signal to Noise Ratio	S/N(3)	Mono	60	70		dB	1

TEST CIRCUIT 1

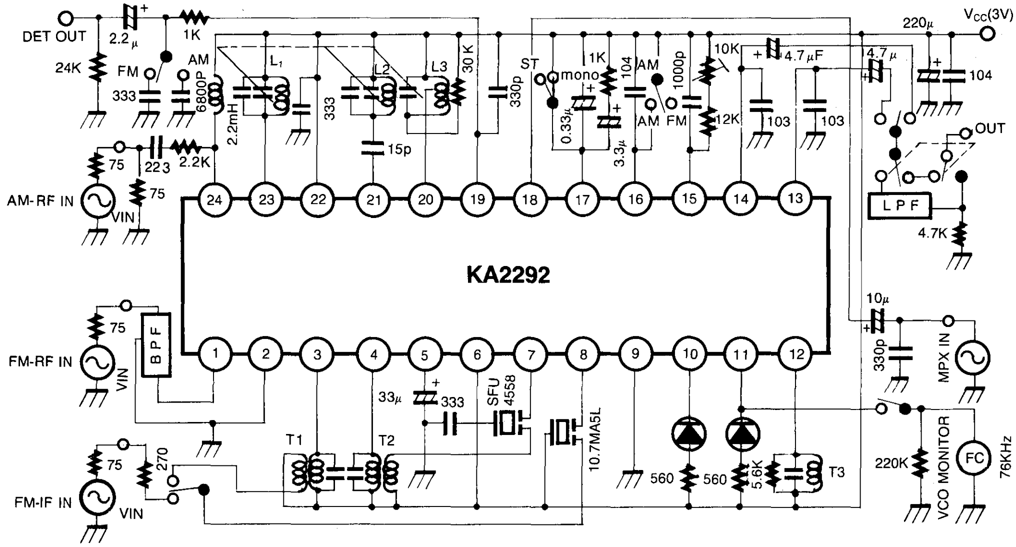


Fig. 2

*POLYESTER FILM CAPACITOR

TEST CIRCUIT 2

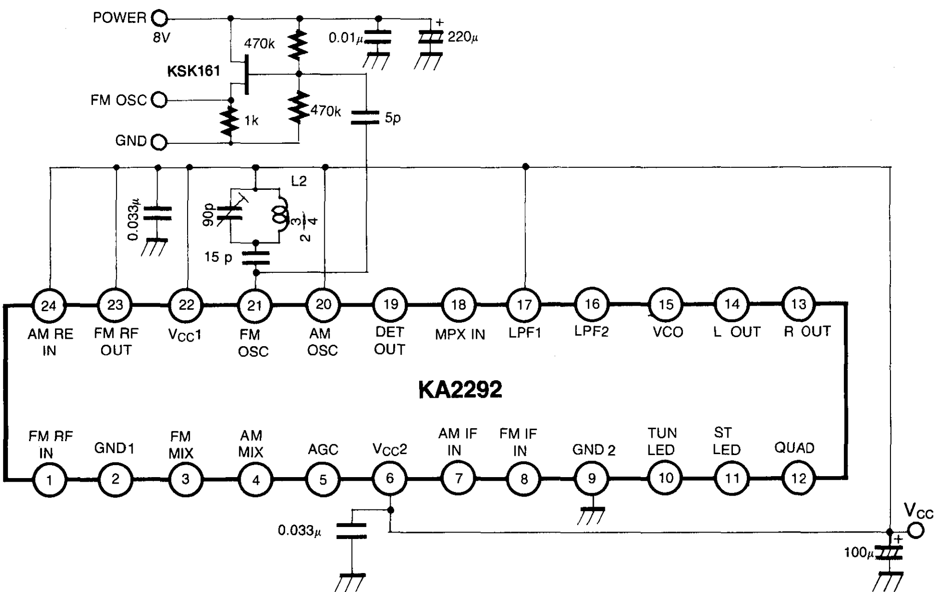
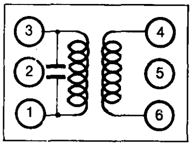


Fig. 3

COIL SPECIFICATIONS

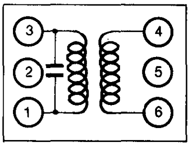
T1 FM IFT (MIX OUT)



C_O(pF)	f (MHz)	Q_O	TURNS		
1-3			1-3	4-6	
75	10.7	70(min)	11	2	

KOREA TOKO
0.1mmφ

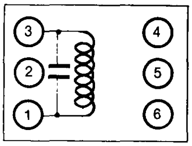
T2 AM IFT (MIX OUT)



C_O(pF)	f (MHz)	Q_O	TURNS		
1-3			1-3	4-6	
180	455	70(min)	180	15	

KOREA TOKO
0.08mmφ

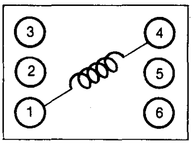
T3 FM IFT (DET)



C_O(pF)	f (MHz)	Q_O	TURNS		
1-3			1-3		
47	10.7	80(min)	14		

KOREA TOKO
0.1mmφ

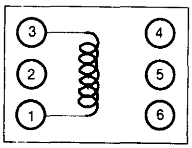
L1 FM RF



f (MHz)	Q_O	TURNS		
		1-4		
100	100	2½		

0.5mmφ

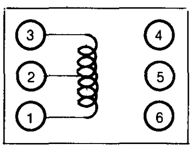
L2 FM OSC



f (MHz)	Q_O	TURNS		
		1-3		
100	100	2¾		

0.5mmφ

L3 AM OSC

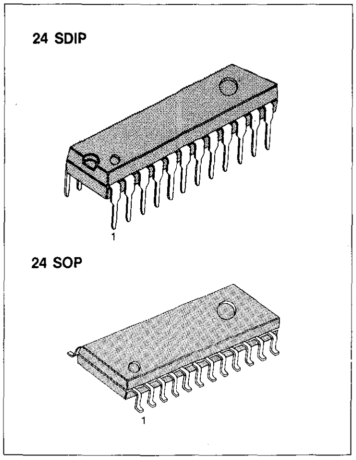


f (KHz)	Q_O	TURNS			L (μH)
		1-2	2-3		
796	80(min)	13	73		288

KOREA TOKO
0.08mmφ

FM/AM TUNER + MPX

The KA2293 is a monolithic integrated circuit which consists of a one chip tuner and no adjustment FM multiplex for AM/FM radios and headphone radios.



FEATURES

- **One-chip tuner with built-in FM multiplex.**
- **No adjustment for FM detector and VCO.**
- **No AM detect coil, IF coupling capacitor, FM IF bypass capacitor needed.**
- **Built-in AM/FM selection switch.**
- **Minimum number of external parts required.**
- **Wide operating voltage range: $V_{CC} = 1.8 \sim 7V$**
- **Low distortion (FM IF: 0.4%, AM IF: 1%, MPX: 0.2% (Typ)).**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2293	24 SDIP	−20 ~ +75°C
KA2293D	24 SOP	−20 ~ +75°C

BLOCK DIAGRAM

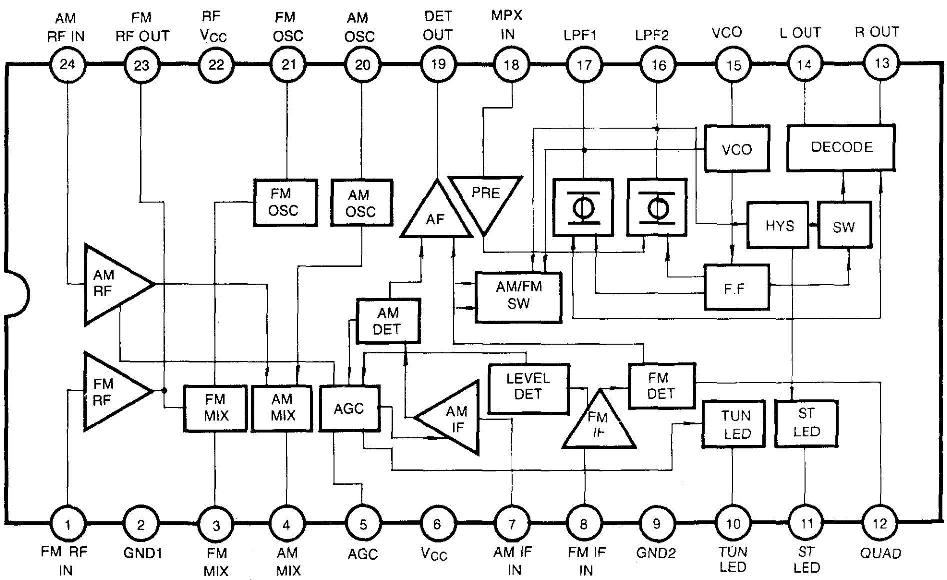


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	8	V
Power Dissipation	P_d	1200	mW
Operating Temperature	T_{opr}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C
LED Drive Voltage	V_{LED}	10	V
LED Drive Current	I_{LED}	10	mA

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 3V, unless otherwise specified)
FM F/E : f = 98MHz, fm = 1KHz, △f = 22.5KHz
FM IF : f = 10, 7MHz, fm = 1KHz, △f = 22.5KHz
AM : f = 1MHz, fm = 1KHz, 30% Mod
MPX : f = 1KHz, L + R = 90%, P = 10%, V_i = 150mV

	Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit	Test Circuit
	Circuit Current	$I_{CC}(1)$	FM, V_i = 0	10	14	18	mA	1
		$I_{CC}(2)$	AM, Vi = 0	3.5	6.0	9	mA	1
F/E	Input Limiting Sensitivity	V_i(lim)(1)	V_O = −3dB	10	14	18	dBμ	1
	Oscillation Voltage	V_{OSC}	f_{OSC} = 72.3MHz	70	105	140	mV	2
FM IF	Input Limiting Sensitivity	V_i(lim)(2)	V_O = −3dB	39	44	49	dBμ	1
	Detector Output Voltage	$V_O(1)$	V_i = 80dBμ	55	80	110	mV	1
	Signal to Noise Ratio	S/N(1)	V_i = 80dBμ	60	70		dB	1
	Total Harmonic Distortion	THD(1)	V_i = 80dBμ		0.4	1	%	1
	AM Rejection Ratio	AMR	V_i = 80dBμ	40	50		dB	1
	Tuning Indication Voltage	$V_L(1)$	I_L = 1mA	43	48	53	dBμ	1
AM IF	Voltage Gain	$A_V(1)$	V_i = 23dBμ	20	40	80	mV	1
	Detector Output Voltage	$V_O(2)$	V_i = 60dBμ	50	60	100	mV	1
	Signal to Noise Ratio	S/N(2)	V_i = 60dBμ	34	44		dB	1
	Total Harmonic Distortion	THD(2)	V_i = 60dBμ		1	2	%	1
	Tuning Indication Voltage	$V_L(2)$	I_L = 1mA	19	24	30	dBμ	1
MPX	Maximum Input Voltage	V_i(max)	Stereo, THD = 3%	250	350		mV	1
	Channel Separation	Sep(1)	Stereo, f = 100Hz	35	42		dB	1
		Sep(2)	Stereo, f = 1KHz	35	42		dB	1
		Sep(3)	Stereo, f = 10KHz	35	42		dB	1
	Total Harmonic Distortion	THD(3)	Mono		0.2	1	%	1
		THD(4)	Stereo		0.2	1	%	1
	Voltage Gain	$A_V(2)$	Mono	−5	−3	−1	dB	1
	Channel Balance	CB	Mono	−2	0	2	dB	1
	Lamp on Level	V_L(on)	Pilot only		8	16	mV	1
		V_L(off)	Pilot only	2	6		mV	1
	Lamp Hysteresis	HY			2		mV	1
	Capture Range	CR	Pilot only		±3		%	1
	Signal to Noise Ratio	S/N(3)	Mono	60	70		dB	1

TEST CIRCUIT 1

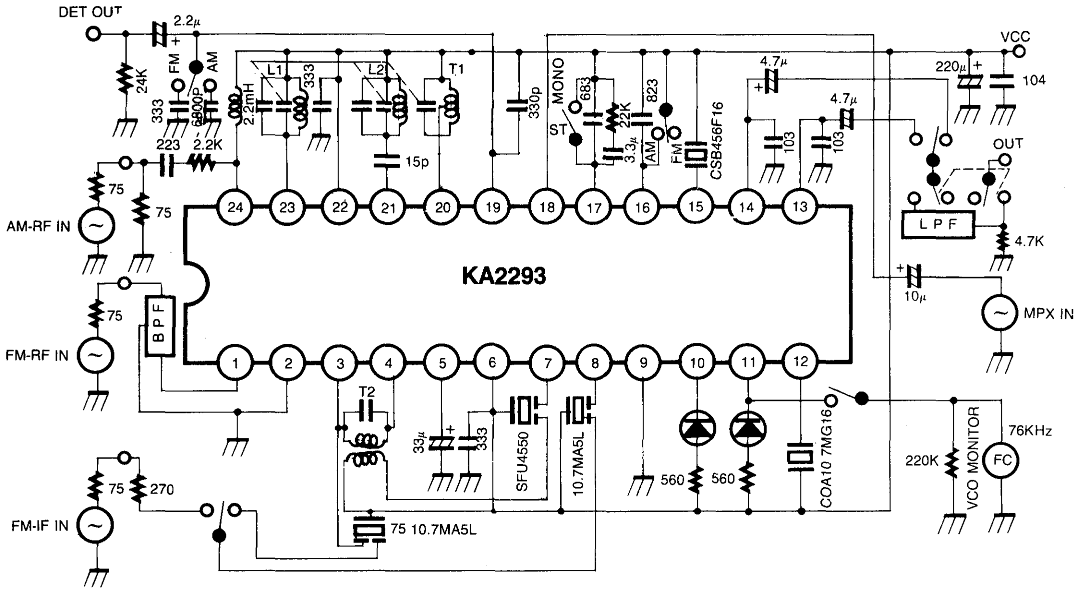


Fig. 2

TEST CIRCUIT 2

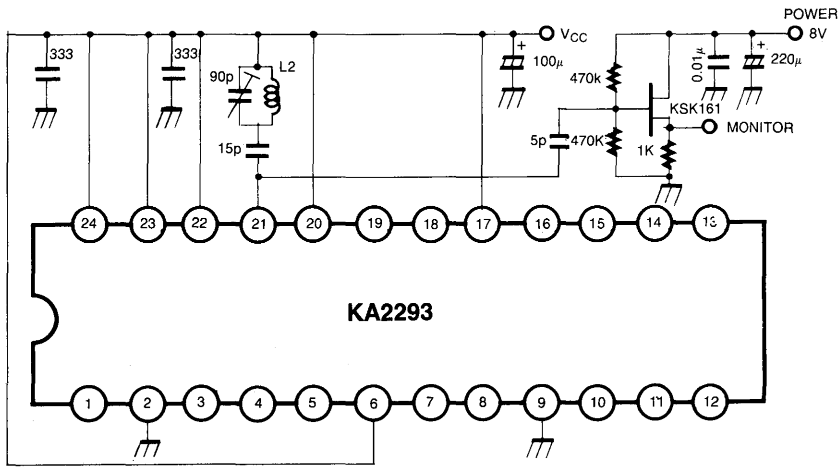
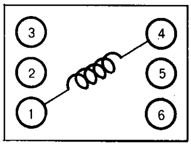


Fig. 3

COIL SPECIFICATIONS

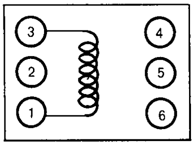
L1 FM RF



f (MHz)	Qo	TURNS		
		1-4		
100	100	2½		

0.5mmϕ

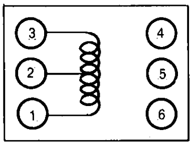
L2 FM OSC



f (MHz)	Qo	TURNS		
		1-3		
100	100	2¾		

0.5mmϕ

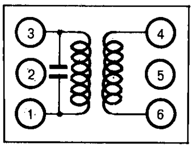
T1 AM OSC



f (MHz)	Qo	TURNS			L (μH)
		1-2	2-3		
796	115	13	73		288

KOREA TOKO
0.08mmϕ

T2 AM IFT (MIX OUT)

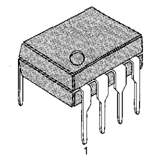


Co(pF)	f (KHz)	Qo	TURNS		
1-3			1-3	4-6	
180	455	120	180	15	

KOREA TOKO
0.08mmϕ

DC MOTOR SPEED CONTROLLER

The KA2401 is a monolithic integrated circuit designed for DC motor speed controllers.



FEATURES

- Suitable for DC motor speed controllers of cassette tape recorders and radio cassettes.
- Excellent stability of each characteristics against ambient temperature.
- Low quiescent current (0.8mA; Typ).
- Low reference voltage.
- Wide operating supply voltage range (4V ~ 12V).

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2401	8 DIP	−20 ~ +70°C

EQUIVALENT CIRCUIT BLOCK DIAGRAM

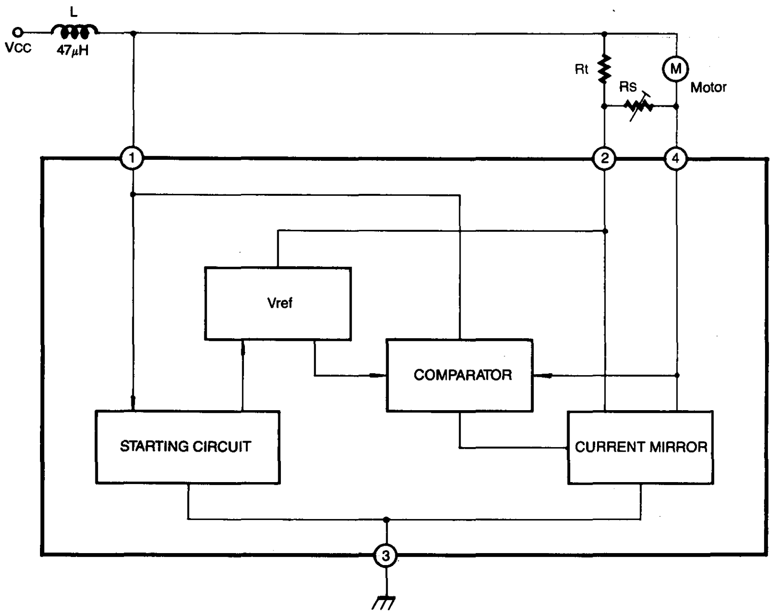


Fig. 1

3

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Circuit Current	I_4	*2	A
Power Dissipation	P_d	600	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

*t<5 sec

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=6V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Fig
Reference Voltage	Vref	I_4=10mA	1.10	1.27	1.40	V	2
Quiescent Current	Id	Rm=180Ω	0.5	0.8	1.2	mA	5
Reflection-Coefficient	K	Rm_1=44Ω, Rm_2=33Ω	18	20	22		3
Saturation Voltage	V_4 (sat)	V_{CC}=4.2V, Rm=4.4Ω		1.5	20	V	4
Voltage Characteristic	$\frac{\Delta K}{K}/\Delta V_{CC}$	I_4=100mA, V_{CC}=4 ~ 12V		0.4		%/V	3
	$\frac{\Delta Vref}{Vref}/\Delta V_{CC}$	I_4=100mA, V_{CC}=4 ~ 12V		0.06		%/V	2
Current Characteristic	$\frac{\Delta K}{K}/\Delta I_4$	I_4=30 ~ 200mA		−0.02		%/mA	3
	$\frac{\Delta Vref}{Vref}/\Delta I_4$	I_4=30 ~ 200mA		−0.02		%/mA	2
Temperature Characteristic	$\frac{\Delta K}{K}/\Delta T_a$	I_4=100mA T_a=−20 ~ +75°C		0.01		%/°C	3
	$\frac{\Delta Vref}{Vref}/\Delta T_a$	I_4=100mA T_a=−20 ~ +75°C		0.01		%/°C	2

TEST CIRCUIT 1

Reference Voltage

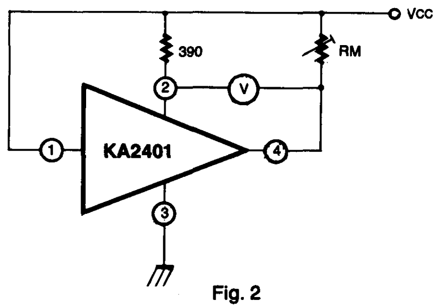


Fig. 2

$$Vref,\ \frac{\Delta Vref}{Vref}/\Delta Vcc,\ \frac{\Delta Vref}{Vref}/\Delta I_4,\ \frac{\Delta Vref}{Vref}/\Delta T_a$$

TEST CIRCUIT 2

Reflection Coefficient

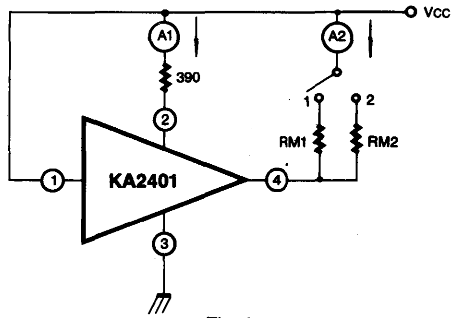


Fig. 3

$$K,\ \frac{\Delta K}{K}/\Delta Vcc,\ \frac{\Delta K}{K}/\Delta I_4,\ \frac{\Delta K}{K}/\Delta T_a$$

$$K=\frac{I_4\,(SW\,2)-I_4\,(SW\,1)}{I_2\,(SW\,2)-I_2\,(SW\,1)}$$

TEST CIRCUIT 3

Saturation Voltage

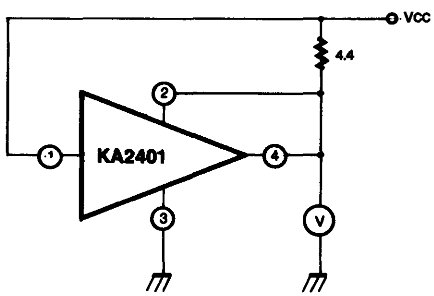
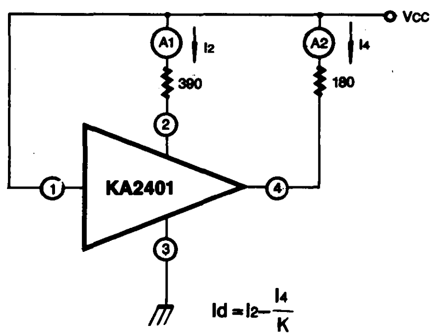


Fig. 4

TEST CIRCUIT 4

Quiescent Current



$$Id=I_2-\frac{I_4}{K}$$

Fig. 5

TYPICAL APPLICATION

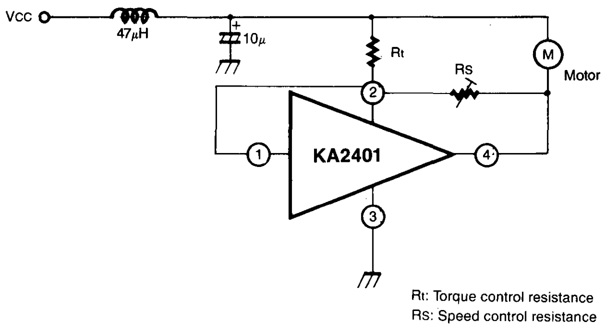


Fig. 6

BASIC EQUATION

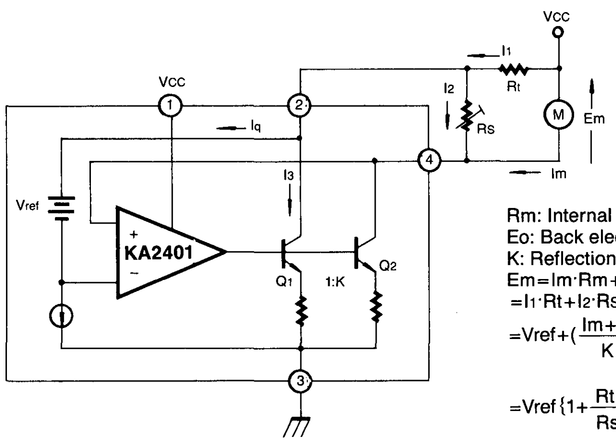


Fig. 7

Rm: Internal resistance of the motor
Eo: Back electronic force
K: Reflection coefficient

$Em = Im \cdot Rm + Eo$

$= I_1 \cdot Rt + I_2 \cdot Rs$

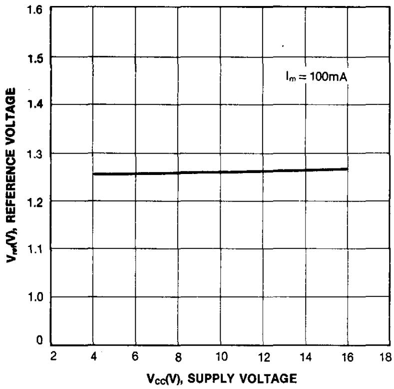
$= Vref + \left(\frac{Im + I_2}{K} + Iq + \frac{Vref}{Rs}\right) \cdot Rt$

$= Vref\left\{1 + \frac{Rt}{Rs}\left(1 + \frac{1}{K}\right)\right\} + Rt \cdot Iq + \frac{Rt}{K} Im$

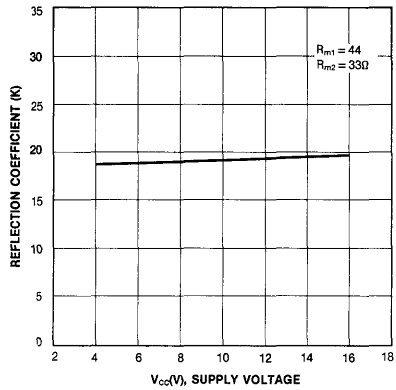
If, $Rm = \frac{Rt}{K}$ then

$Eo = Vref\left\{1 + \frac{Rt}{Rs}\left(1 + \frac{1}{K}\right)\right\} + Rt \cdot Iq$

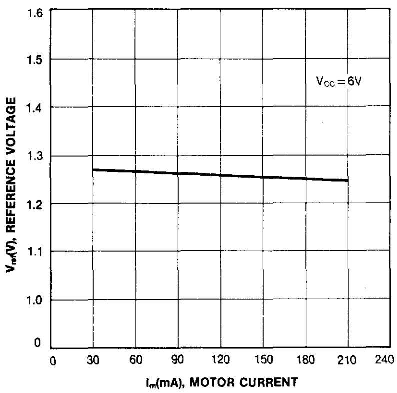
REFERENCE VOLTAGE-SUPPLY VOLTAGE



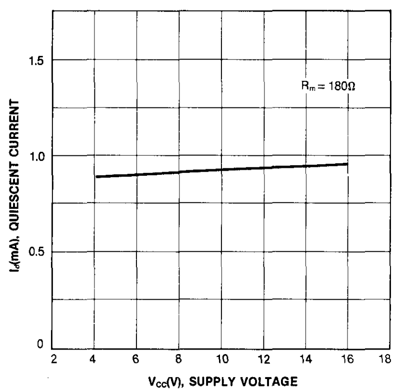
REFLECTION COEFFICIENT-SUPPLY VOLTAGE



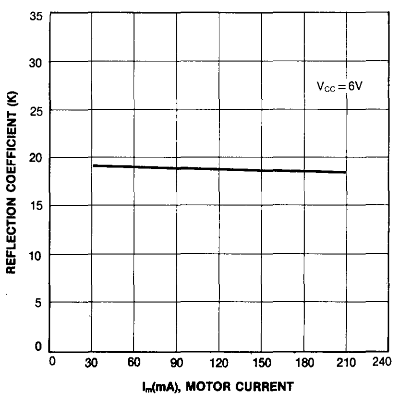
REFERENCE VOLTAGE-MOTOR CURRENT



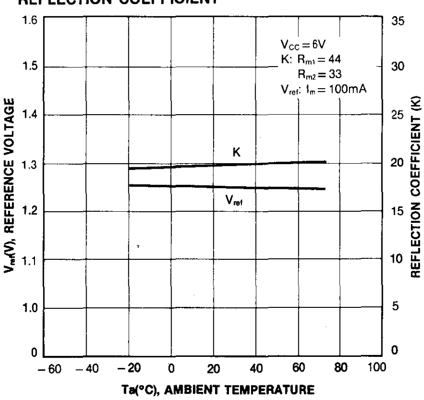
QUIESCENT CURRENT-SUPPLY VOLTAGE



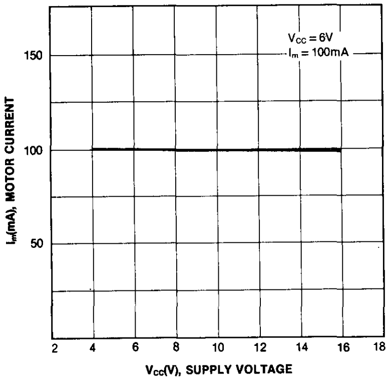
REFLECTION COEFFICIENT-MOTOR CURRENT



REFERENCE VOLTAGE / REFLECTION COEFFICIENT -AMBIENT TEMPERATURE



MOTOR CURRENT-SUPPLY VOLTAGE



LOW VOLTAGE DC MOTOR SPEED CONTROLLER

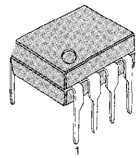
USE

- Speed control or general-purpose low-voltage compact DC motor for microcassette tape recorders, radio cassettes and their equivalents.

FEATURES

- **Wide operating supply voltage range (1.8V ~ 8V).**
- **Capable of making the applicable set compact because of a minimum to adjust speed.**
- **Easy to adjust speed.**
- **Built-in stable low reference power meeting the requirements for 2 speeds.**
- **Vref=0.2V**

8 DIP



EQUIVALENT CIRCUIT BLOCK DIAGRAM

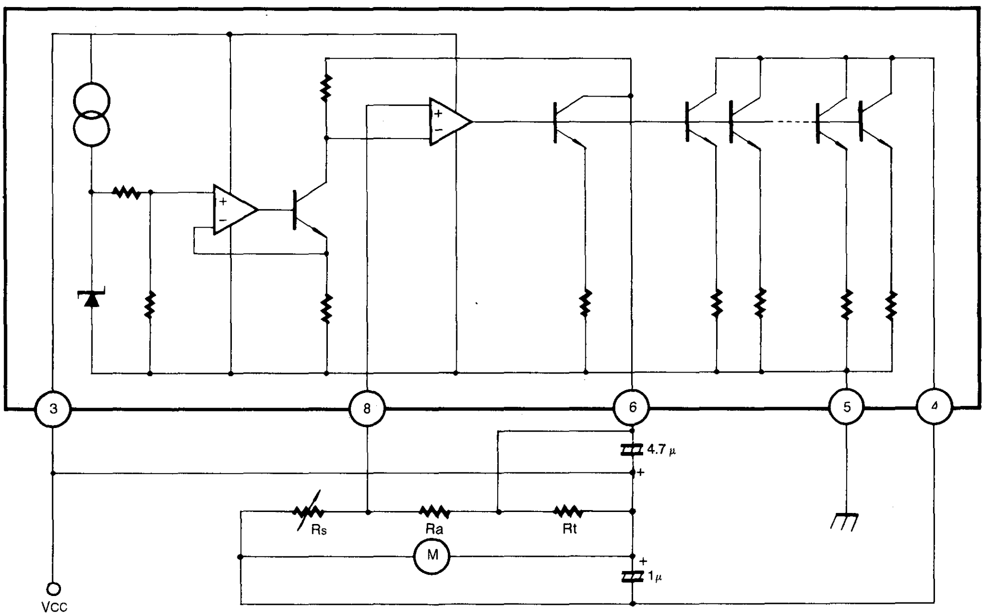


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Maximum Supply Voltage	V_{CC}	10	V
Maximum Motor Current	I_m	700	mA
Power Dissipation	P_d	600	mW
Operating Temperature	Topr	−20 ~ +80	°C
Storage Temperature	Tstg	−40 ~ +125	°C

RECOMMENDED OPERATING CONDITIONS (T_a=25°C)

Supply Voltage	V_{CC}	1.8 ~ 8	V
Operating Temperature	Topr	−20 ~ +60	°C

ELECTRICAL CHARACTERISTICS (T_a=25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference Voltage	Vref	V_{CC}=3V, I_m=100mA	0.18	0.2	0.22	V
Circuit Current	I_{CC}	V_{CC}=3V, I_m=100mA		2.4	6.0	mA
Shunt Ratio	K	V_{CC}=3V, I_m=50mA I_m=100mA	45	50	55	
Saturation Voltage	V (sat)	V_{CC}=3V, I_m=100mA		0.13	0.3	V
Voltage Characteristic of Reference Voltage	$\frac{\Delta Vref}{Vref} / \Delta V_{CC}$	I_m=100mA V_{CC}=1.8 ~ 8V		0.1		%/V
Voltage Characteristic of Shunt Ratio	$\frac{\Delta K}{K} / \Delta V_{CC}$	I_m=50, 150mA V_{CC}=1.8 ~ 8V		0.3		%/V
Current Characteristic of Reference Voltage	$\frac{\Delta Vref}{Vref} / \Delta I_m$	V_{CC}=3V I_m=20 ~ 200mA		0.005		%/mA
Current Characteristic of Shunt Ratio	$\frac{\Delta K}{K} / \Delta I_m$	V_{CC}=3V, I_m=20, 50mA ~ 170, 200mA		−0.07		%/mA
Temperature Characteristic of Reference Voltage	$\frac{\Delta Vref}{Vref} / \Delta T_a$	V_{CC}=3V, I_m=100mA T_a=−20 ~ +80°C		−0.008		%/°C
Temperature Characteristic of Shunt Ratio	$\frac{\Delta K}{K} / \Delta T_a$	V_{CC}=3V, I_m=50, 150mA T_a=−20 ~ +80°C		0.02		%/°C

TEST CIRCUIT

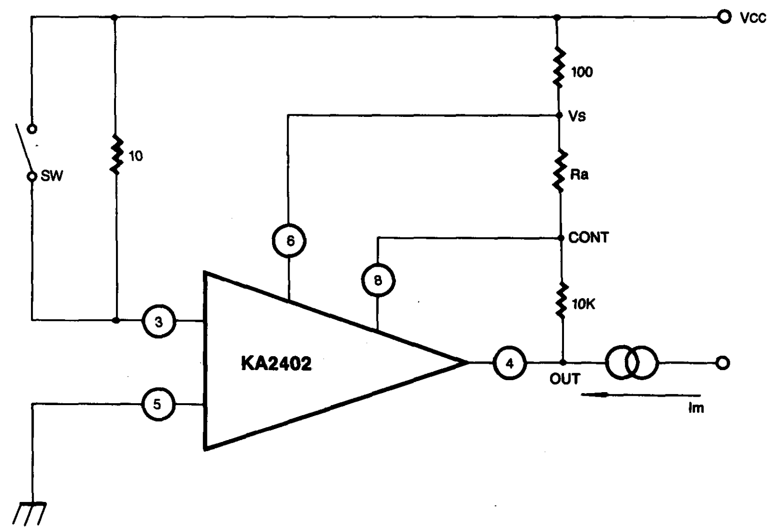


Fig. 2

TEST METHOD

1. V_{ref} : With SW turned on, measure the voltage developed across Ra.
2. I_{CC} : With SW turned off, measure I_{CC} for the voltage developed across resistor 10.00 ohm.
3. K : With SW turned on, measure current I_{50} flowing through resistor 100 ohm at I_m =50mA and current I_{150} flowing through resistor 100 ohm at I_m =150mA, and obtain K by use of the following equation.

$$K = \frac{100mA}{(I_{150} - I_{50})\ (mA)}$$

4. V (sat) : With SW turned on, set V_{CC} = V_S =CONT=3V and feed I_m =100mA, and measure the voltage developed across pins 4 and 5.

Application Circuit 1

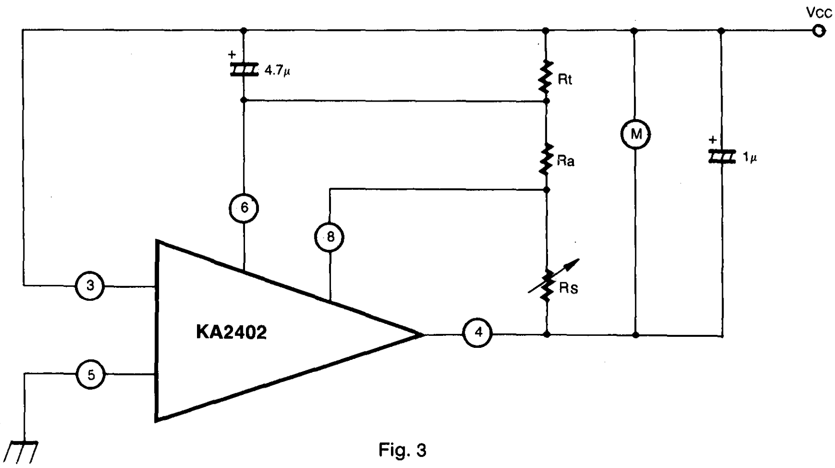
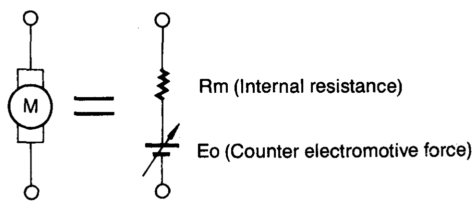


Fig. 3

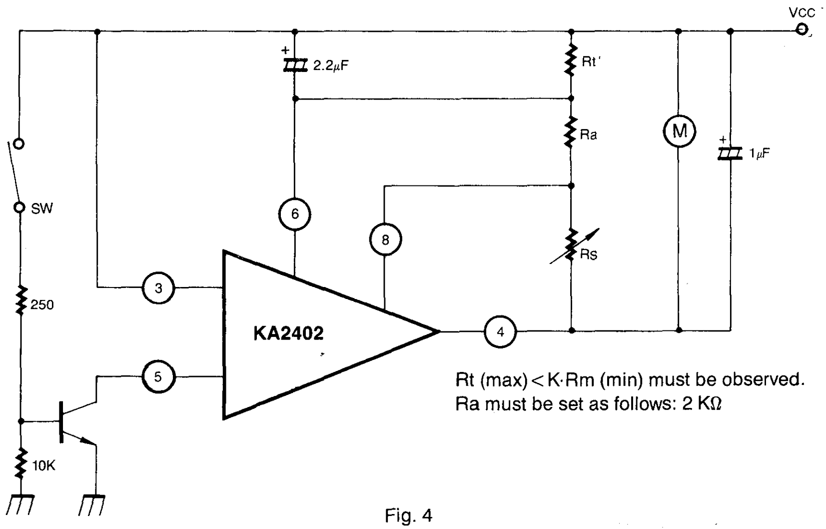
Unless Rt (max) < K·Rm (min), the operation becomes unstable.
Ra must be set as follows: 2KΩ
Rm = Motor internal resistance



The values of the electrolytic capacitors depend on the type of the motor to be used.

3

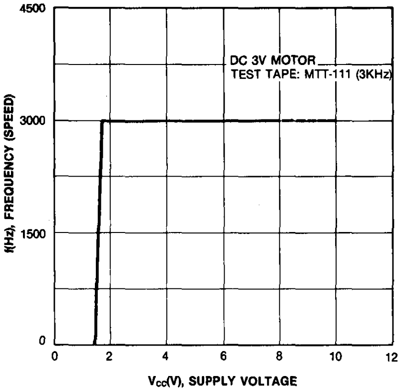
Application Circuit 2: with stop circuit



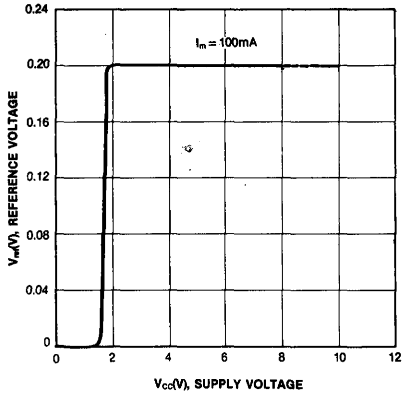
Rt (max) < K·Rm (min) must be observed.
Ra must be set as follows: 2 KΩ

Fig. 4

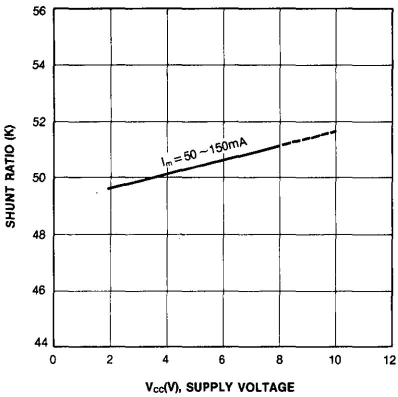
FREQUENCY (SPEED)-SUPPLY VOLTAGE



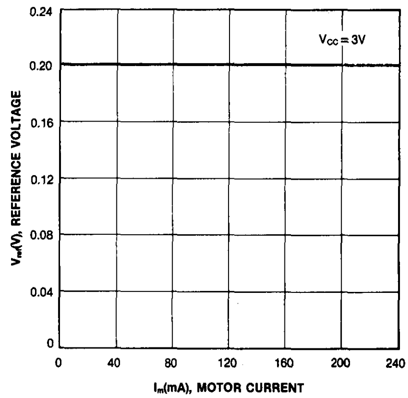
REFERENCE VOLTAGE-SUPPLY VOLTAGE



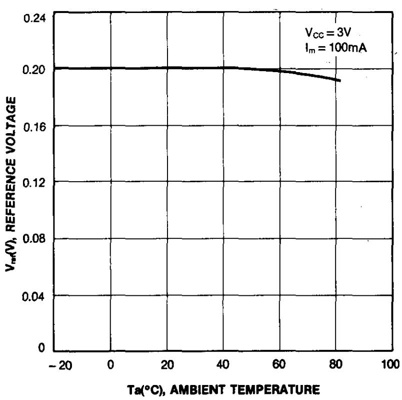
SHUNT RATIO-SUPPLY VOLTAGE



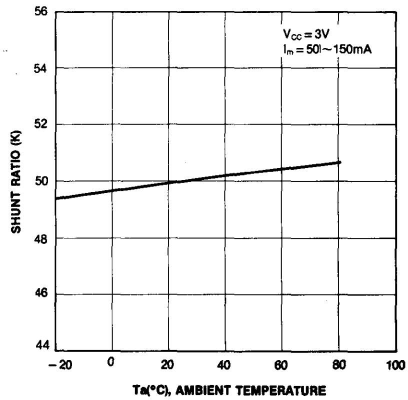
REFERENCE VOLTAGE-MOTOR CURRENT



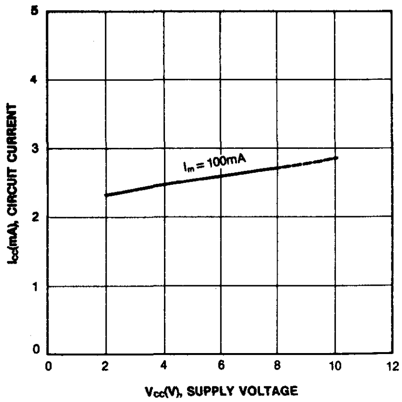
REFERENCE VOLTAGE-AMBIENT TEMPERATURE



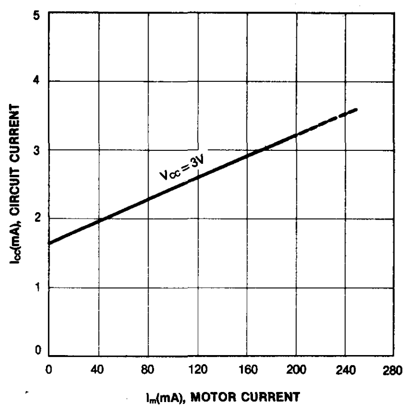
SHUNT RATIO-AMBIENT TEMPERATURE



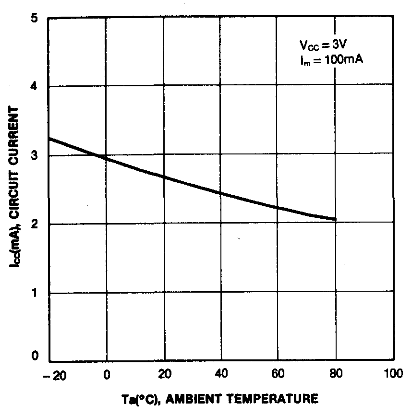
CIRCUIT CURRENT-SUPPLY VOLTAGE



CIRCUIT CURRENT-MOTOR CURRENT



CIRCUIT CURRENT-AMBIENT TEMPERATURE

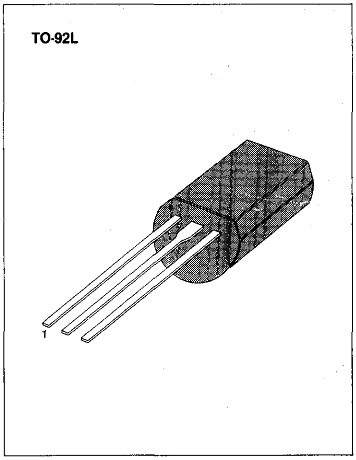


DC MOTOR SPEED CONTROLLER

The KA2404 is a monolithic integrated circuit designed for DC motor speed controllers.

FEATURES

- Suitable for DC motor speed controllers of cassette tape recorders and radio cassettes.
- Excellent stability of each characteristics against ambient temperature.
- High output current.
- Low quiescent current (1.3mA: typ).
- Low reference voltage.
- Wide operating supply voltage range (4V ~ 12V).



EQUIVALENT CIRCUIT BLOCK DIAGRAM

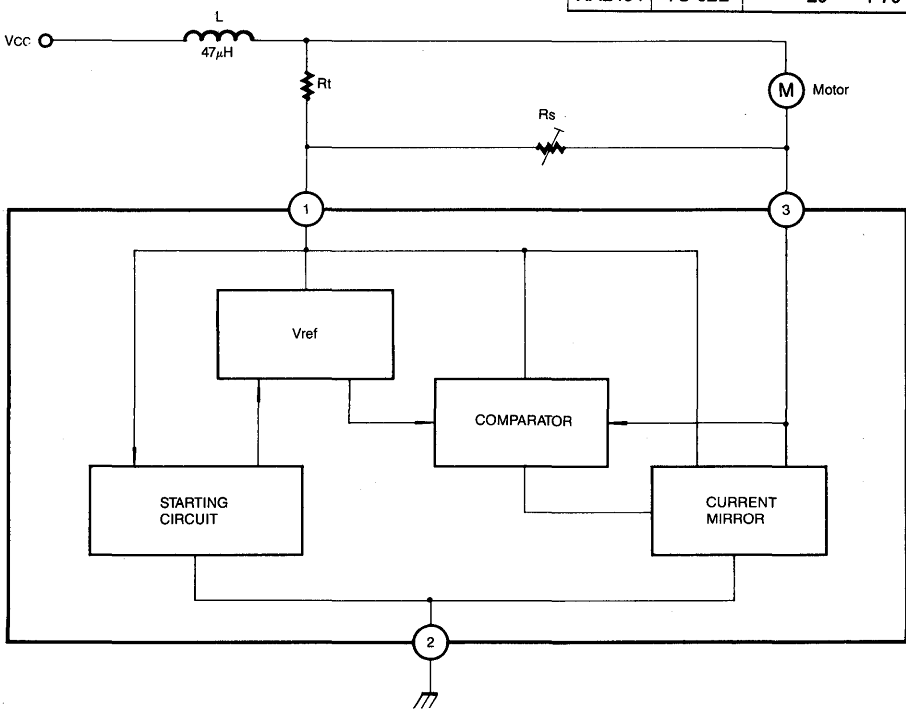


Fig. 1

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2404	TO-92L	−20 ~ +70°C

3

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Circuit Current	I_3	*2	A
Power Dissipation	P_d	800	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−40 ~ +125	°C

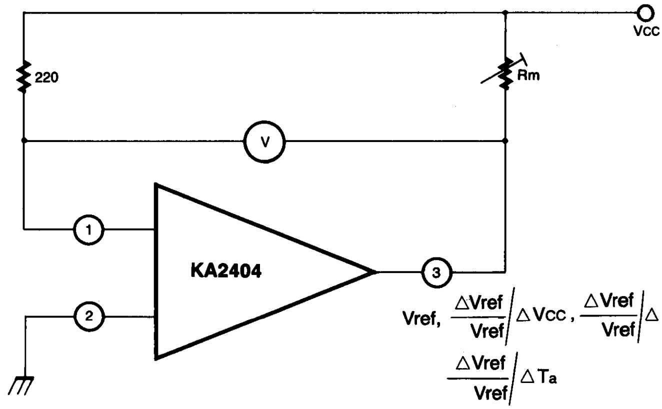
* t<5 sec

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=9V unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Fig
Reference Voltage	Vref	I_3=10mA	1.10	1.27	1.40	V	2
Quiescent Current	Id	Rm=180Ω	0.8	1.3	1.8	mA	4
Reflection Coefficient	K	Rm_1=44Ω, Rm_2=33Ω	16	18	20		3
Voltage Characteristic	$\frac{\Delta K}{K} / \Delta V_{CC}$	I_3=100mA, V_{CC}=4 ~ 12V		0.4		%/V	3
	$\frac{\Delta Vref}{Vref} / \Delta V_{CC}$	I_3=100mA, V_{CC}=4 ~ 12V		0.06		%/V	2
Current Characteristics	$\frac{\Delta K}{K} / \Delta I_3$	I_3=30 ~ 200mA		−0.02		%/mA	3
	$\frac{\Delta Vref}{Vref} / \Delta I_3$	I_3=30 ~ 200mA		−0.02		%/mA	2
Temperature Characteristics	$\frac{\Delta K}{K} / \Delta T_a$	I_3=100mA, T_a=20 ~ +75°C		0.01		%/°C	3
	$\frac{\Delta Vref}{Vref} / \Delta T_a$	I_3=100mA, T_a=−20 ~ +75°C		0.01		%/°C	2

TEST CIRCUIT 1
Reference Voltage

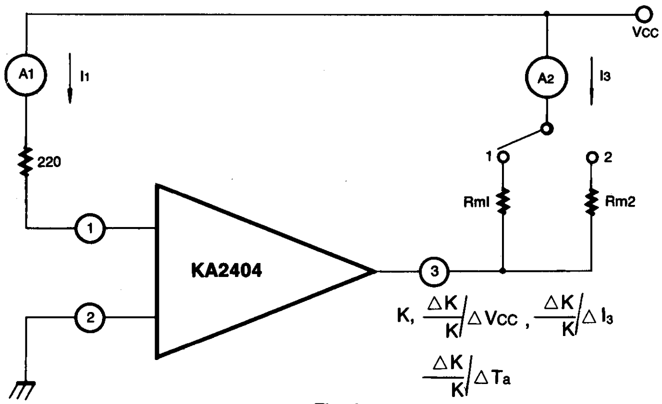


$$V_{ref},\ \frac{\Delta V_{ref}}{V_{ref}}\Big/\Delta V_{CC},\ \frac{\Delta V_{ref}}{V_{ref}}\Big/\Delta I_3$$

$$\frac{\Delta V_{ref}}{V_{ref}}\Big/\Delta T_a$$

Fig. 2

TEST CIRCUIT 2
Reflection Coefficient



$$K,\ \frac{\Delta K}{K}\Big/\Delta V_{CC},\ \frac{\Delta K}{K}\Big/\Delta I_3$$

$$\frac{\Delta K}{K}\Big/\Delta T_a$$

Fig. 3

$$K=\frac{I_3\ (SW\ 2)-(SW\ 1)}{I_1\ (SW\ 2)-(SW\ 1)}$$

TEST CIRCUIT 3
Quiescent Current

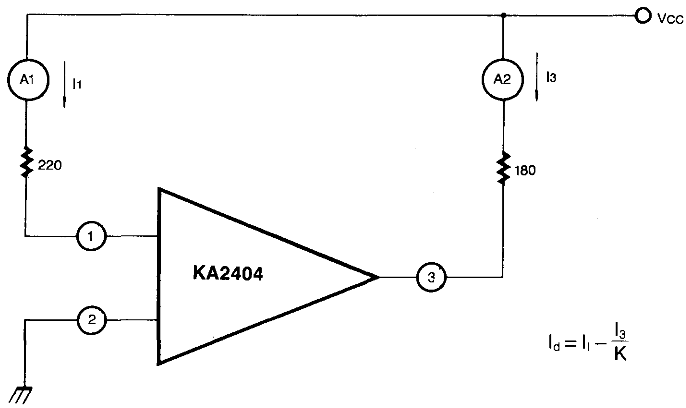


Fig. 4

TYPICAL APPLICATION

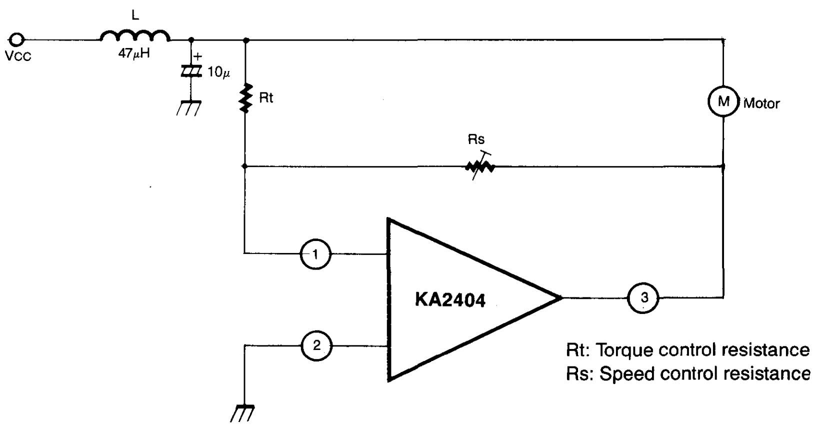
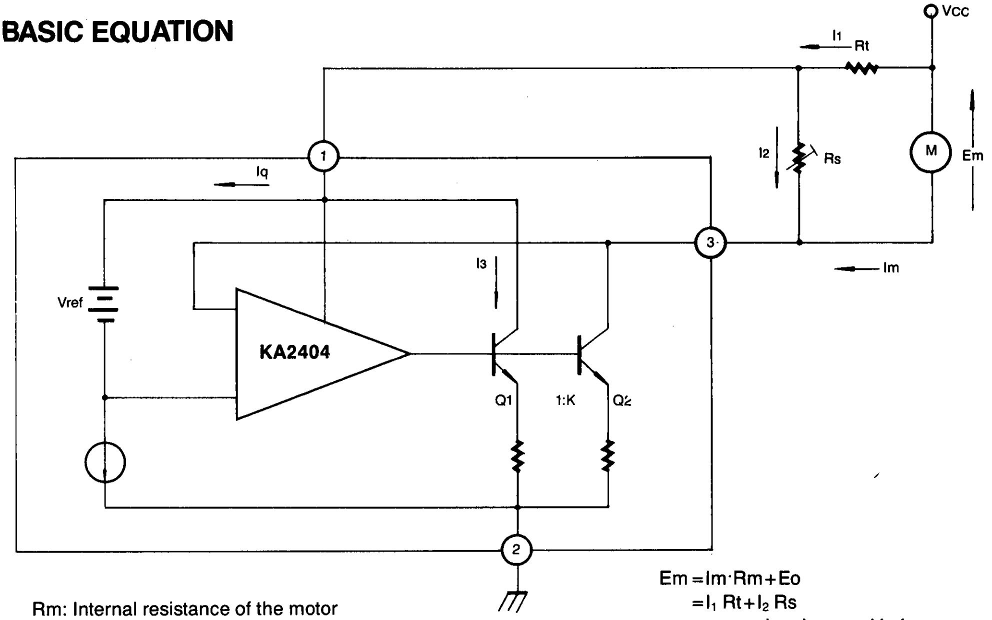


Fig. 5

BASIC EQUATION



Rm: Internal resistance of the motor
Eo: Back electronic force
K: Reflection coefficient

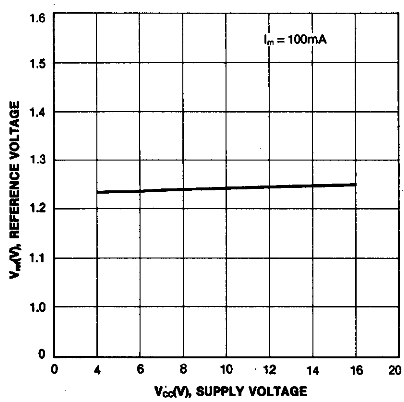
$$\begin{aligned} Em &= Im \cdot Rm + Eo \\ &= I_1\,Rt + I_2\,Rs \\ &= Vref + \left(\frac{Im + I_2}{K} + Iq + \frac{Vref}{Rs}\right)\cdot Rt \\ &= Vref\left(1 + \frac{Rt}{Rs}\left(1 + \frac{1}{K}\right)\right) + Rt \cdot Iq + \frac{Rt}{K} Im \end{aligned}$$

If. $Rm = \frac{Rt}{K}$ then

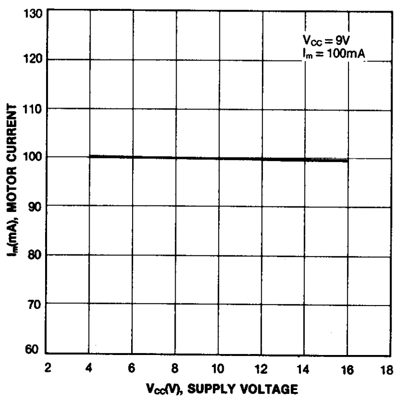
$$Eo = Vref\left(1 + \frac{Rt}{Rs}\left(1 + \frac{1}{K}\right)\right) + Rt \cdot Iq$$

Fig. 6

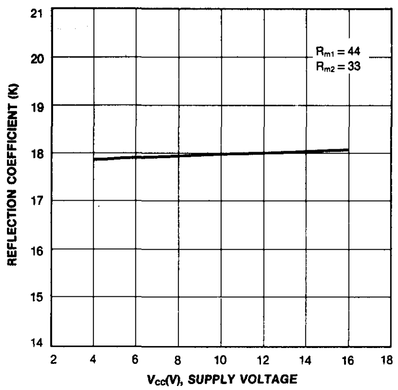
REFERENCE VOLTAGE-SUPPLY VOLTAGE



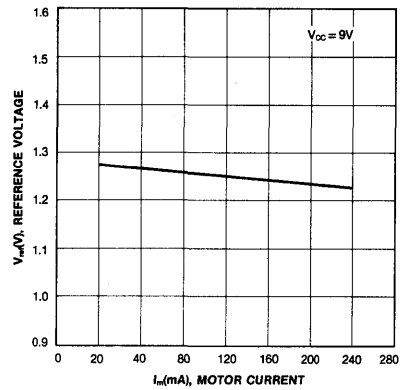
MOTOR CURRENT-SUPPLY VOLTAGE



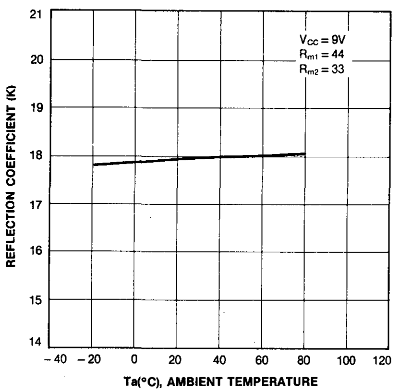
REFLECTION COEFFICIENT-SUPPLY VOLTAGE



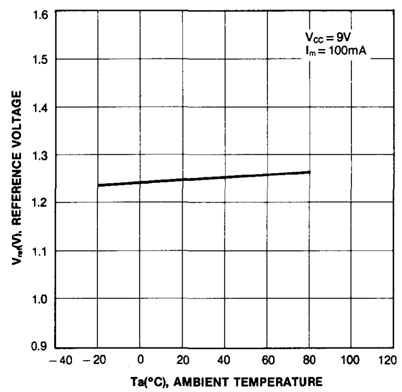
REFERENCE VOLTAGE-MOTOR CURRENT



REFLECTION COEFFICIENT-AMBIENT TEMPERATURE

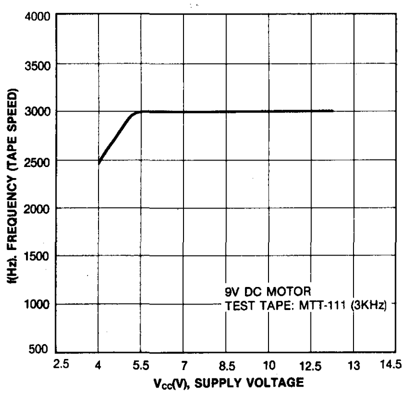


REFERENCE VOLTAGE-AMBIENT TEMPERATURE

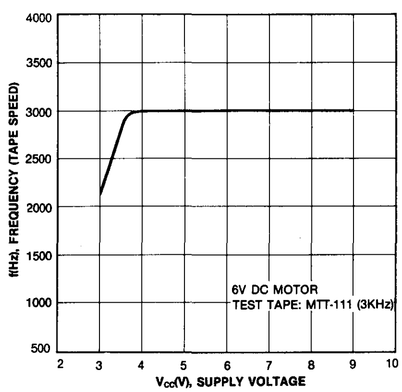


(APPLICATION CHARACTERISTICS)

FREQUENCY(TAPE SPEED)-SUPPLY VOLTAGE

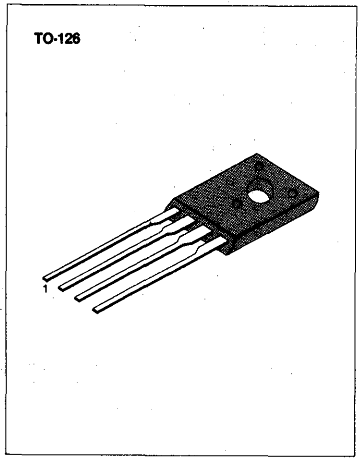


FREQUENCY (TAPE SPEED) SUPPLY VOLTAGE



DC MOTOR SPEED CONTROLLER

The KA2407 is a monolithic integrated circuit designed for DC motor speed controllers.



FEATURES

- **High stable operation over a wide range of supply voltage; V_{CC} = 3.5V ~ 14.4V**
- **Stable low reference voltage (1.0V Typ) for wide motor speed setting**
- **A minimum number of external parts required**
- **Small four-lead plastic package for compact motor**
- **Reverse voltage protection circuit**

APPLICATIONS

- Tape recorders & recorder players
- Home stereos
- Car components

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2407	TO-126	−20 ~ +70°C

BLOCK DIAGRAM

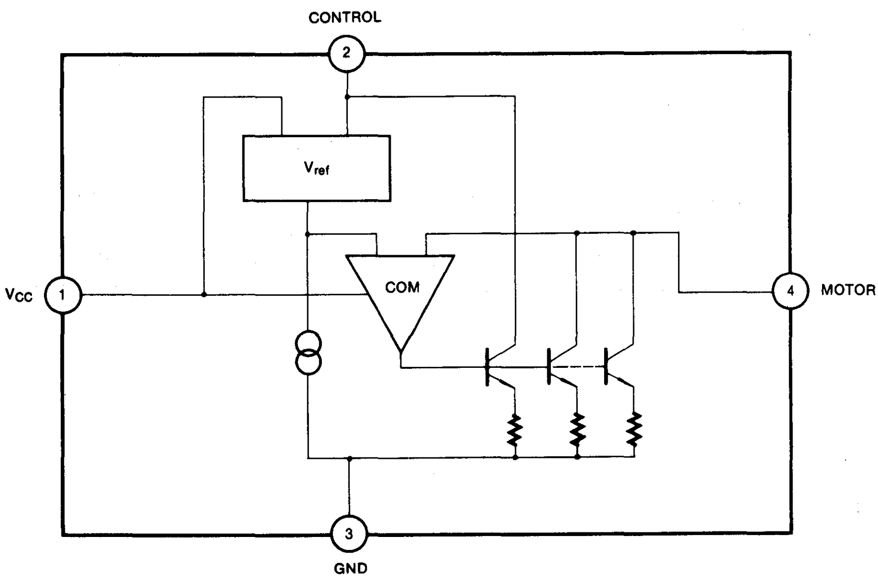


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	14.4	V
Supply Current	I_{CC} (Note 1)	2	A
Power Dissipation	P_d (Note 2)	1.3	W
Operating Temperature	T_{opr}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−40 ~ +150	°C

(Note 1): $t \leq 5$ sec
(Note 2): Ta = 25°C, With a 100 × 100mm bakelite printed circuit board (35μm Cu leaf)

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 6V)

Characteristic	Symbol	Test Circuit	Test Conditions	Min	Typ	Max	Unit
Reference Voltage	V_{ref}	1	Ra = 1KΩ	0.85	1.0	1.15	V
Bias Current	I_B	3			0.8	1.8	mA
Current Shunt Ratio	K	2	ΔI_4 = 40mA	35	40	45	
Saturation Voltage	V_{sat}	1	V_{CC} = 4.2V, Ra = 5Ω		1.15	2	V
Voltage Characteristic 1	$\frac{\Delta V_{ref}}{V_{ref}}/V_{CC}$	1	V_{CC} = 3.5V ~ 14V, Ra = 1KΩ		−0.1		%/V
Voltage Characteristic 2	$\frac{\Delta K}{K}/V_{CC}$	2	V_{CC} = 3.5V ~ 14V, ΔI_4 = 40mA		0.1		%/V
Current Characteristic 1	$\frac{\Delta V_{ref}}{V_{ref}}/I_4$	1	I_4 = 50mA ~ 200mA		−0.02		%/mA
Current Characteristic 2	$\frac{\Delta K}{K}/I_4$	2	I_4 = 50mA ~ 200mA		−0.01		%/mA
Temperature Characteristic 1	$\frac{\Delta V_{ref}}{V_{ref}}/Ta$	1	Ta = −20 ~ +75°C, Ra = 1KΩ		0.01		%/°C
Temperature Characteristic 2	$\frac{\Delta K}{K}/Ta$	2	Ta = −20 ~ +75°C, ΔI_4 = 40mA		0.01		%/°C

TEST CIRCUIT 1

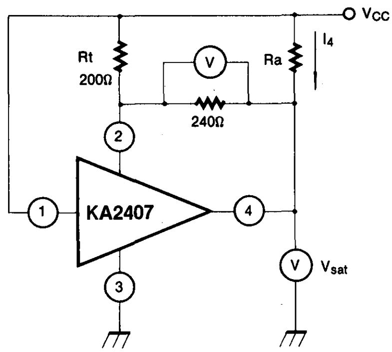


Fig. 2

V_{ref}, V_{sat}, $\frac{\Delta V_{ref}}{V_{ref}}/V_{CC}$, $\frac{\Delta V_{ref}}{V_{ref}}/I_4$ $\frac{\Delta V_{ref}}{V_{ref}}/Ta$,

TEST CIRCUIT 2

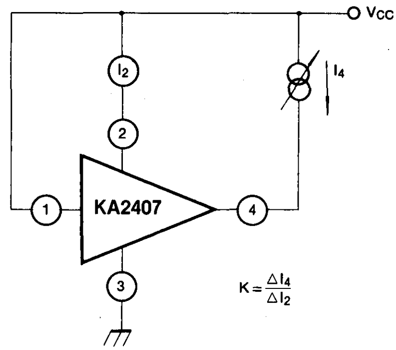


Fig. 3

K, $\frac{\Delta K}{K}/V_{CC}$, $\frac{\Delta K}{K}/I_4$, $\frac{\Delta K}{K}/Ta$

TEST CIRCUIT 3

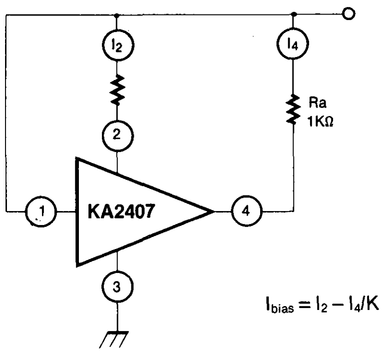


Fig. 4

APPLICATION CIRCUIT

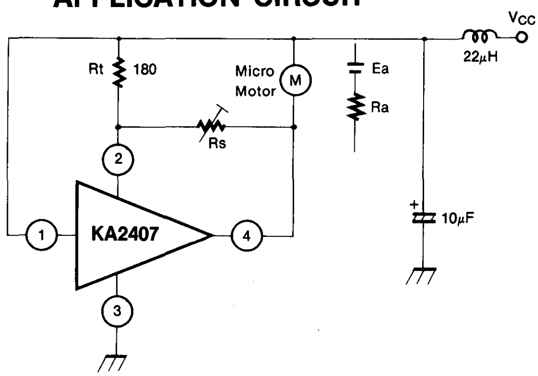
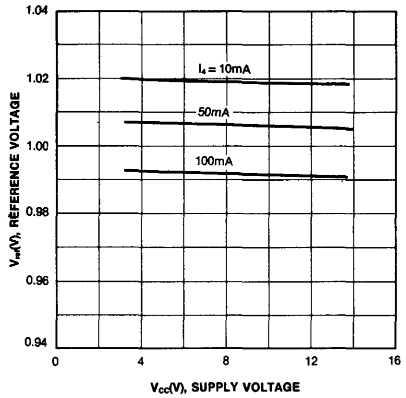


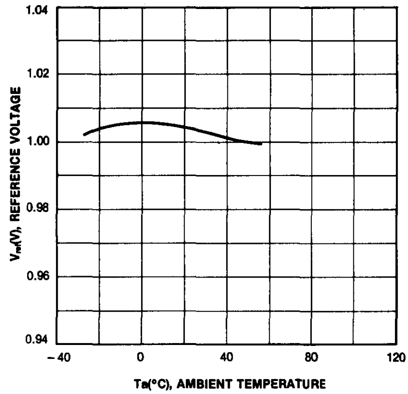
Fig. 5

* Motor Constant Ka: Electromotive force constant = 1.1mV/rpm
Ra = Internal Resistance = 5Ω
K_T: Torque Constant = 100g.cm/A

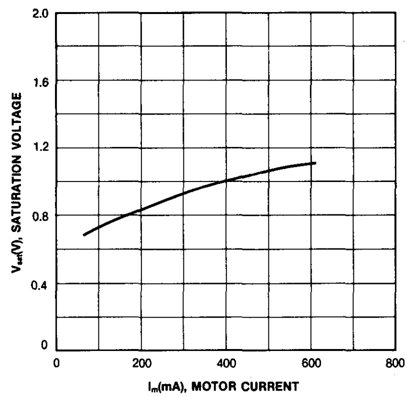
REFERENCE VOLTAGE-SUPPLY VOLTAGE



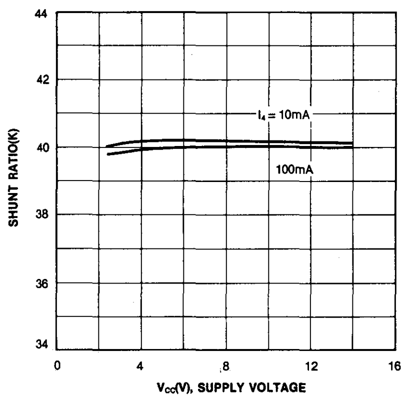
REFERENCE VOLTAGE-AMBIENT TEMPERATURE



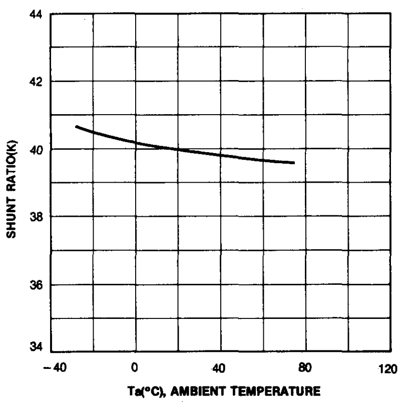
SATURATION VOLTAGE-MOTOR CURRENT



SHUNT RATIO-SUPPLY VOLTAGE



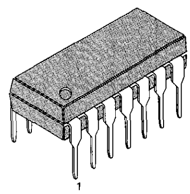
SHUNT RATIO-AMBIENT TEMPERATURE



DUAL EQUALIZER AMPLIFIER WITH ALC

The KA7226 is a monolithic integrated circuit consisting of a dual equalize amplifier with ALC. It is suitable for use in the record/ playback amplifier of stereo radio cassettes.

14 DIP



FEATURES

- Dual equalizer amplifier with ALC circuit
- Built-in buffer amplifier
- Not necessary input coupling capacitor
- Quick stabilization after power on
- High output voltage: $V_O = 1.7V$ (Typ) at THD = 1%
- Wide operating supply voltage range: $V_{CC} = 3V \sim 16V$

ORDERING INFORMATION

Device	Package	Operating Temperature
KA7226	14 DIP	− 25 ~ + 75°C

BLOCK DIAGRAM

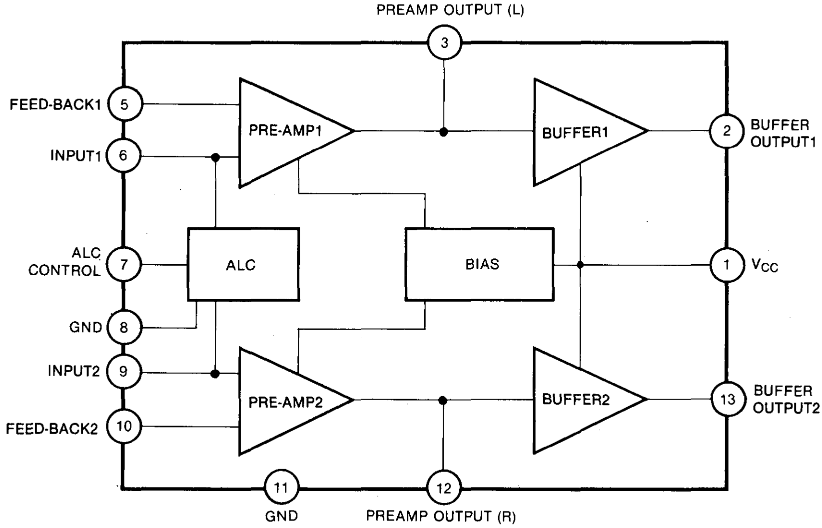


Fig. 1

3

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Output Current (Buffer AMP: Pin 2, 13)	I_2, I_{13}	3	mA
Output Current (Pre AMP: Pin 6, 9)	I_6, I_9)	2	mA
Power Dissipation	*P_d	600	mW
Operating Temperature	T_{opr}	− 25 ~ + 75	°C
Storage Temperature	T_{stg}	− 40 ~ + 125	°C

* : Derated above Ta = 25°C in the propotion of 5mW/°C.

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 5V, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Test Circuit
Quiescent Circuit Current	I_{CC}	$V_i = 0$	6	10	15	mA	1
Input Terminal DC Voltage	V_6, V_9			20	100	mV	1
Output Terminal DC Voltage	V_3, V_{12}		2.2	2.5	2.8	V	1
Buffer Output DC Voltage	V_2, V_{13}		1.4	1.7	2	V	1
ALC Bias Voltage	V_7		0.4	0.55	0.7	V	1
ALC ON Voltage	V_I (ALC)	$V_7 = 1.4V$		5	30	mV	1
ALC Range	ALC (R)	$V_i = -60dBm$	35	40		dB	2
ALC Level	ALC (L)	$V_i = -20dBm$	− 3	− 1	1	dBm	2
Total Harmonic Distortion	ALC (THD)	$V_i = -20dBm$		0.6	2.0	%	2
ALC Balance	ALC (B)	$V_i = -20dBm$		0	2	dB	2
Output Voltage	V_O	THD = 1%	1.3	1.7		V	2
Cross Talk	CT	$R_g = 2.2K\Omega$, $V_O = 0dBm$	40	60		dB	2
Open Loop Voltage Gain	A_{VO}	$V_i = -80dBm$	67	75		dB	2
Equivalent Input Noise Voltage	V_{NI}	$R_g = 2.2K\Omega$		1.3	2.7	μV	2

TEST CIRCUIT 1

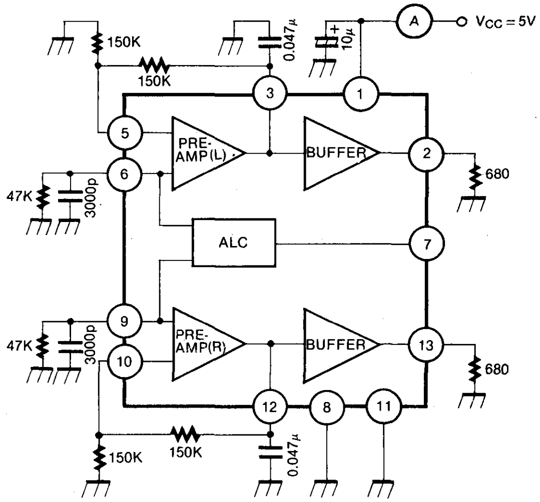


Fig. 2

TEST CIRCUIT 2

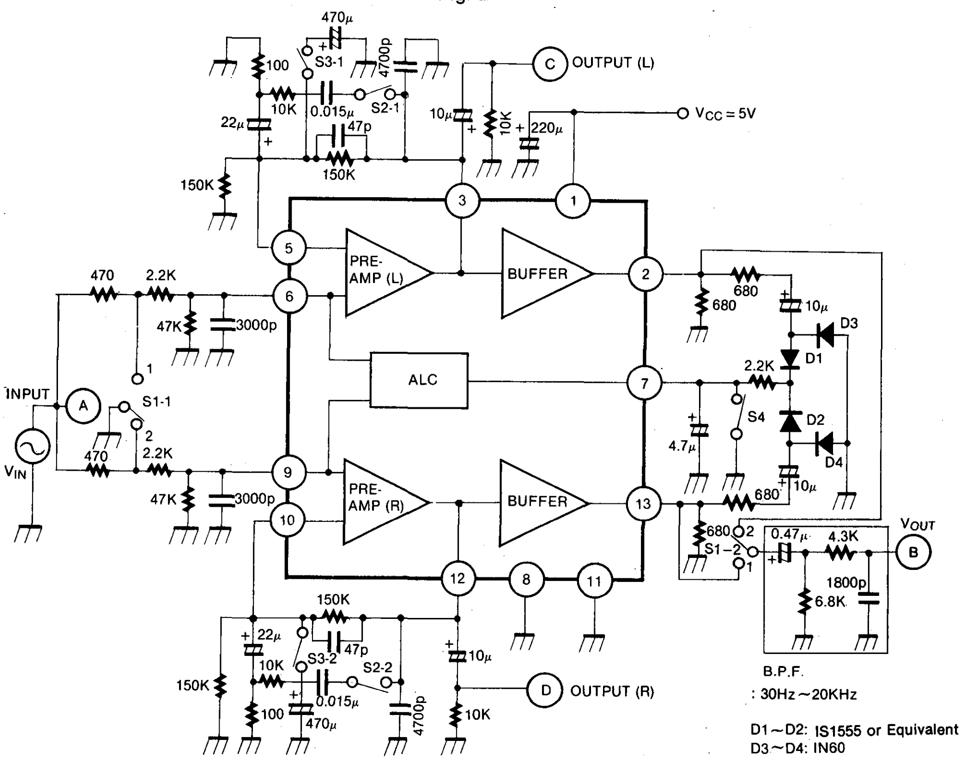


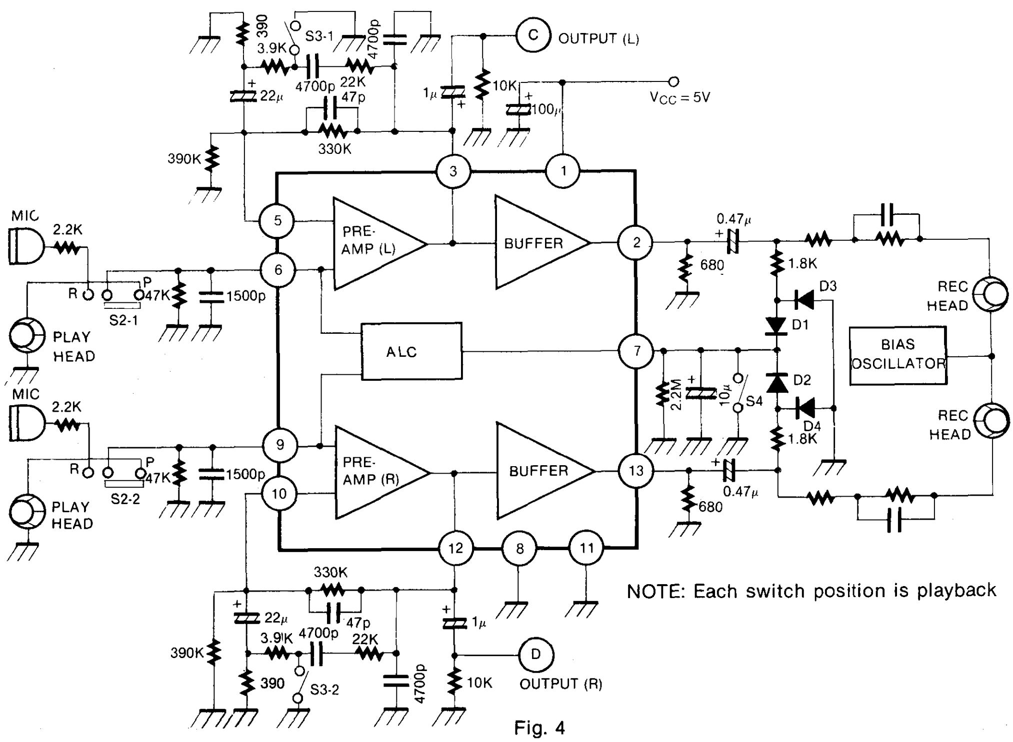
Fig. 3

3

TEST METHOD OF TEST CIRCUIT 2

Symbol	S1		S2	S3	S4	Test Point	Test Method
A_{VO}	1	2	OFF	ON	ON	A.C.D.	$A_{VO}=20 \log V_O/V_I$ (dB) with input voltage V_I, output voltage at V_O
V_O (ALC)	1	2	OFF	OFF	OFF	B	Measure output voltage V_O at input voltage $V_I=-20$ dBm
THD (ALC)	1	2	OFF	OFF	OFF	B	Measure distortion factor at input voltage $V_I=-20$dBm
V_{NI}	S1-1=1 S1-2=2	S1-1=2 S1-2=1	ON	OFF	ON	B	Convert output noise voltage at 1KHz gain when $R_g=2.2K\Omega$
V_{OM}	1	2	ON	OFF	ON	C, D	Measure output voltage V_O at THD=1%
CT	1	2	ON	OFF	ON	B	Measure crosstalk of amplifier 1, 2 at output voltage V_O=0dBm
ALC Range	1	2	OFF	OFF	OFF	B	Input voltage range from $V_I=-60$dBm to output voltage V_O 3dB up
ALC Balance	1	2	OFF	OFF	OFF	B	Output voltage V_O level difference of amp 1, 2 when $V_I=-20$dBm is applied

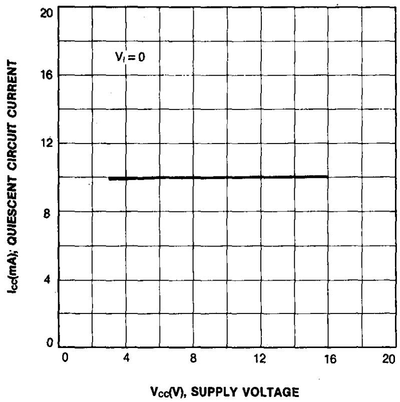
TYPICAL APPLICATION CIRCUIT



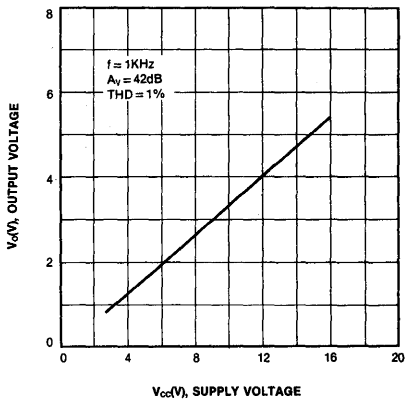
NOTE: Each switch position is playback

Fig. 4

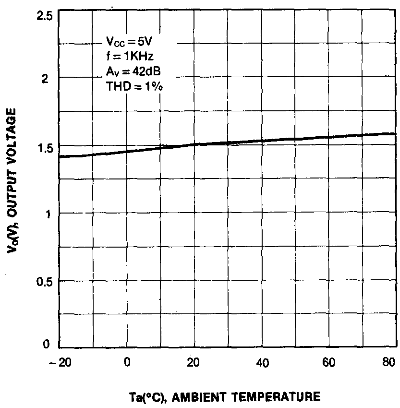
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



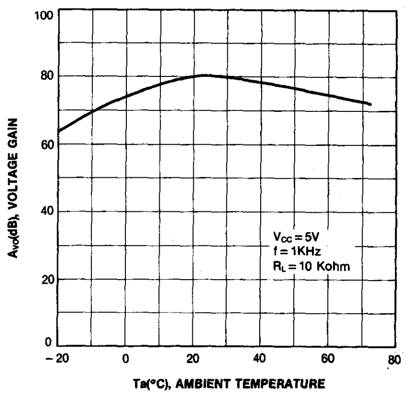
OUTPUT VOLTAGE-SUPPLY VOLTAGE



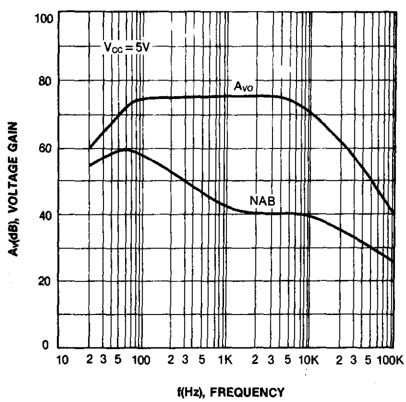
OUTPUT VOLTAGE-AMBIENT TEMPERATURE



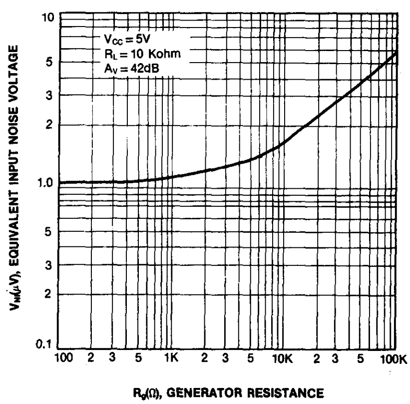
VOLTAGE GAIN-AMBIENT TEMPERATURE



VOLTAGE GAIN-FREQUENCY

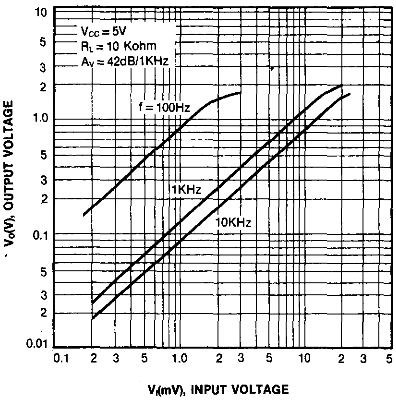


EQUIVALENT INPUT NOISE VOLTAGE -GENERATOR RESISTANCE

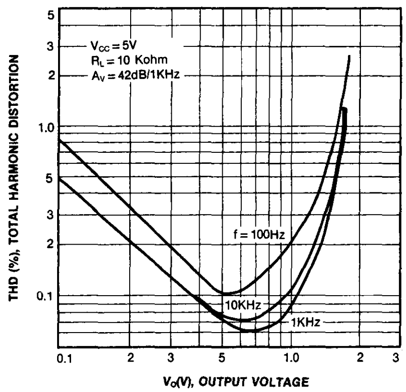


3

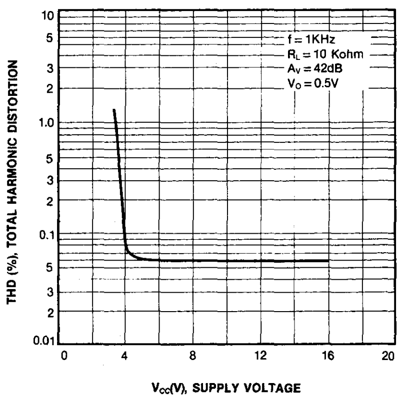
OUTPUT VOLTAGE-INPUT VOLTAGE



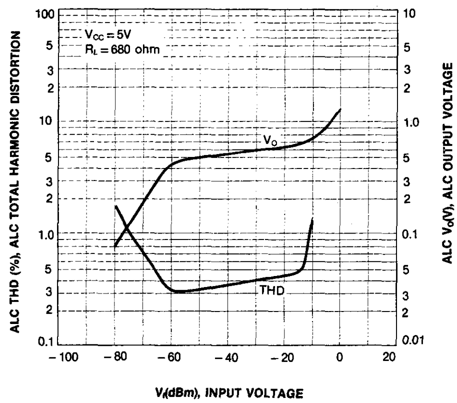
TOTAL HARMONIC DISTORTION-OUTPUT VOLTAGE



TOTAL HARMONIC DISTORTION-SUPPLY VOLTAGE



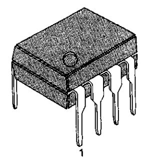
ALC OUTPUT VOLTAGE ALC TOTAL HARMONIC DISTORTION-INPUT VOLTAGE



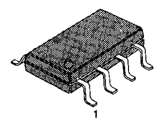
LOW VOLTAGE AUDIO AMPLIFIER

The KA8602 is a audio power amplifier available for low voltage. This amplifier supplies differential outputs for maximizing output swing at low voltages. The KA8602 doesn't need coupling capacitors to the speaker. The gain of this amp is controlled easily by two external resistors.

8 DIP



8 SOP



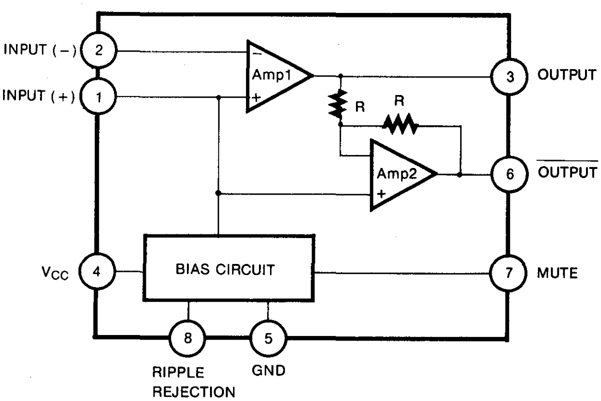
FEATURES

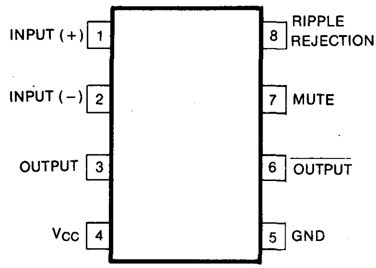
- Wide Supply Voltage (2V ~ 16V)
- Low Quiescent Supply Current (I_{CC} = 3mA)
- Easy Gain Control
- Medium Output Power
  P_O = 250mW at V_{CC} = 6V, R_L = 32Ω, THD = 10%
- Minimum External Parts
- Load Impedance Range (8Ω ~ 100Ω)
- Low Distortion
- Mute Function (I_{CC} = 75μA)

ORDERING INFORMATION

Device	Package	Operating Temperature
KA8602N	8DIP	− 20 ~ + 70°C
KA8602D	8SOP	

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	$-1.0 \sim +18$	V
Output Current (output pin)	I_O	± 250	mA
Maximum Voltage (input, RR, Mute pin)	V_{IR}	$-1.0 \sim V_{CC}+1.0$	V
Applied Output Voltage (output pin) when disabled	V_{OR}	$-1.0 \sim V_{CC}+1.0$	V
Junction Temperature	T_j	$-55 \sim +140$	°C

ELECTRICAL CHARACTERISTICS

($V_{CC}=6$ V, Ta=25°C, unless otherwise noted)

Characteristic		Symbol	Test Condition		Min	Typ	Max	Unit
DC ELECTRICAL CHARACTERISTICS								
Power Supply Current ($R_L=0$)		I_{CC}	$V_{CC}=3.0V$, Mute=0.8V $V_{CC}=16.0V$, Mute=0.8V $V_{CC}=3.0V$, Mute=2.0V			2.7 3.3 65	4.0 5.0 100	mA mA μA
Output Voltage (output Pin)		V_O	$R_L=16\Omega$ $R_1=75K\Omega$	$V_{CC}=3.0V$ $V_{CC}=6.0V$ $V_{CC}=12.0V$	1.0	1.15 2.65 5.65	1.25	V
Output Offset Voltage		ΔV_O	$V_{CC}=6.0V$, $R_I=75K\Omega$, $R_L=32\Omega$		−30	0	+30	mV
Output High Level		V_{OH}	$2.0V \le V_{CC} \le 16V$, $I_{out}=-75mA$			$V_{CC}-1.0$		V
Output Low Level		V_{OL}	$2.0V \le V_{CC} \le 16V$, $I_{out}=75mA$			0.16		V
Input Bias Current (pin 2)		I_M				−100	−200	mA
Equipment Resistance		R_E	pin 1 pin 8		100 18	150 25	220 40	KΩ
Mute	Input Low Voltage	V_{IL}					0.8	V
	Input High Voltage	V_{IH}			2.0			V
	Input Resistance	R_I	V_{CC}=Mute=16V		50	90	175	KΩ
AC ELECTRICAL CHARACTERISTICS								
Open Loop Gain (Amp 1)		A_{OL}			80			dB
Closed Loop Gain (Amp 2)		A_{CL}	f=1.0KHz, $R_L=32\Omega$		−0.35	0	+0.35	dB
Output Power		P_O	$V_{CC}=3.0V$, $R_L=16\Omega$, THD≤10% $V_{CC}=6.0V$, $R_L=32\Omega$, THD≤10% $V_{CC}=12V$, $R_L=100\Omega$, THD≤10%		55 250 400			mW
Total Harmonic Distortion (f=1.0 KHz)		THD	$V_{CC}=6.0V$, $R_L=32\Omega$, $P_O=125mW$ $V_{CC} \le 3.0V$, $R_L=8\Omega$, $P_O=20mW$ $V_{CC} \le 12V$, $R_L=32\Omega$, $P_O=200mW$			0.5 0.5 0.6	1.0	%
Gain Bandwidth Product		GBP				1.5		MHz
Power Supply Rejection ($V_{CC}=6.0V$, $\Delta V_{CC}=3.0V$)		PSRR	$C_1=00$, $C_2=0.01\mu F$ $C_1=0.1\mu F$, $C_2=0$, f=1.0KHz $C_1=1.0\mu F$, $C_2=5.0\mu F$, f=1.0KHz		50	 12 52		dB
Muting		GMT	Mute=2.0V, 1.0KHz≤f≤20KHz			>70		dB

PIN DESCRIPTION

Pin No.	Name	Function
1	Input (+)	Analog Ground for the amplifiers. A 1.0μF capacitor at this pin (with a 5.0μF capacitor at pin 8) provides 52dB (Typ) of power supply rejection. Turn-on time of the circuit is affected by the capacitor on this pin. This pin can be used as an alternate input.
2	Input (−)	Amplifier input. The input capacitor and resistor set low frequency rolloff and input impedance. The feedback resistor is connected to this pin and output.
3	Output	Amplifier 1's output. The DC Level is ≈ $(V_{CC} - 0.7V)/2$
4	V_{CC}	DC supply voltage (+2.0 ~ +16V) is applied to this pin.
5	GND	Ground pin.
6	$\overline{\text{Output}}$	Amplifier 2's output. This signal is equal in amplitude, but 180° out of phase with that at output pin. The DC level is ≈ $(V_{CC} - 0.7V)/2$.
7	Mute	This pin can be used to power down the IC to conserve power, or for muting, or both. When at a logic "Low" (0 to 0.8 volts), the KA8602 is enabled for normal operation. When at a logic "High" (2.0 to V_{CC} volts), the IC is disabled. If Mute is open, that is equivalent to a logic "Low".
8	Ripple Rejection	A capacitor at this pin increases power supply rejection, and affects turn-on time. This pin can be left open if the capacitor at pin 1 is sufficient.

TYPICAL APPLICATION CIRCUIT

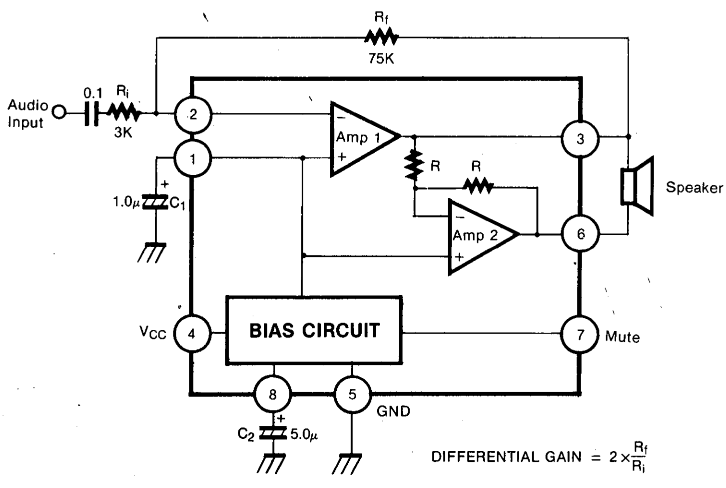


Fig. 1 AUDIO AMPLIFIER (HIGH INPUT IMPEDANCE)

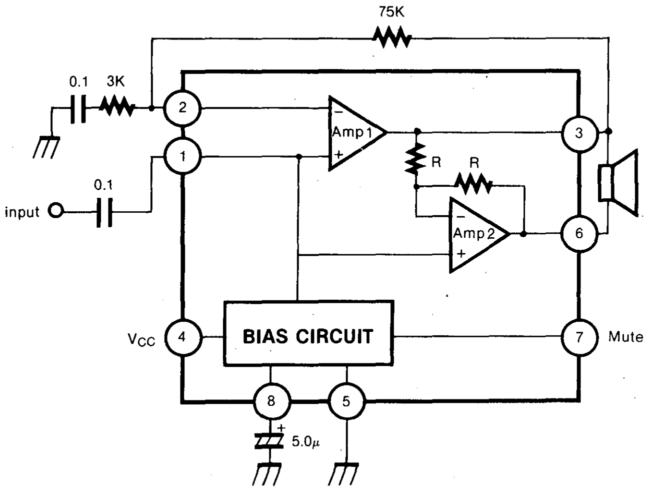


Fig. 2 DUAL SUPPLY OPERATION

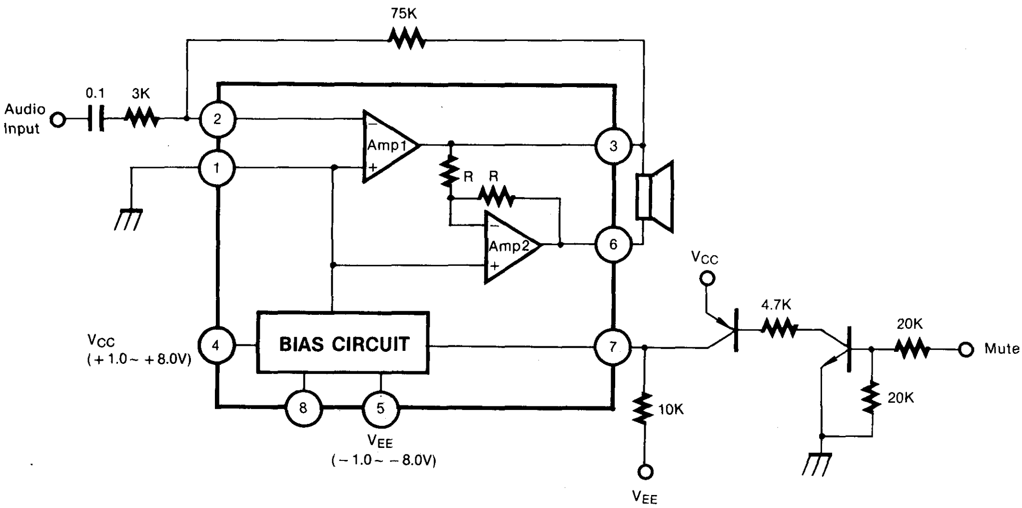


Fig. 3 AUDIO AMPLIFIER (BASS SUPPRESSION)

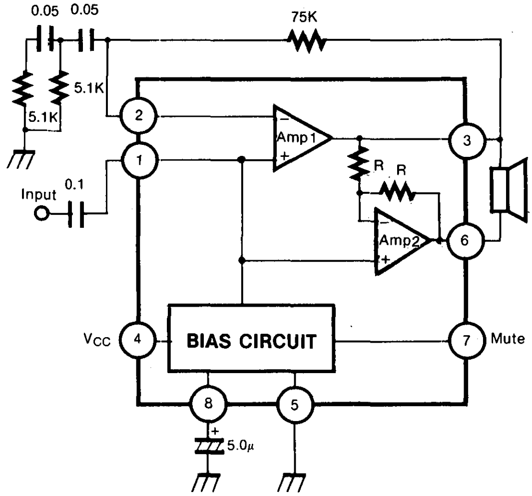


Fig. 4 AUDIO AMPLIFIER (BANDPASS)

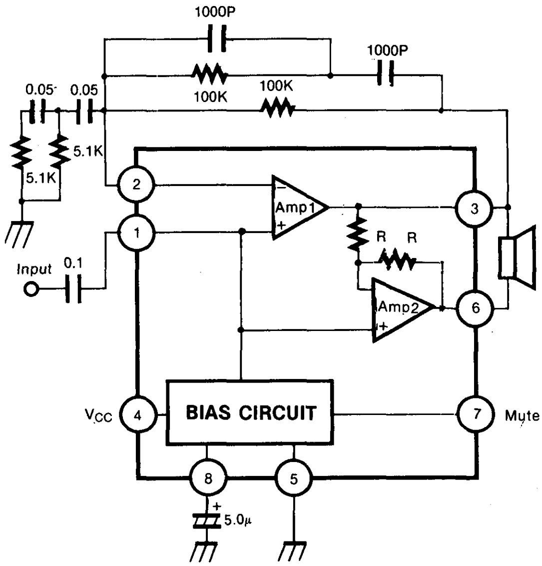


Fig. 5 FREQUENCY RESPONSE OF Fig. 3

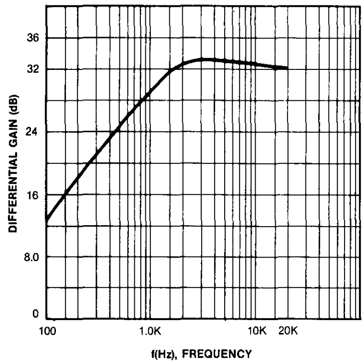


Fig. 6 FREQUENCY RESPONSE OF Fig. 4

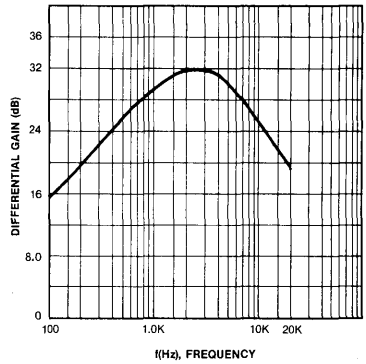


Fig. 7 OPEN LOOP GAIN & PHASE (AMP 1)

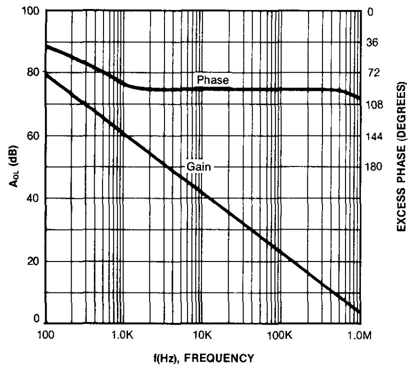


Fig. 8 DIFFERENTIAL GAIN vs FREQUENCY

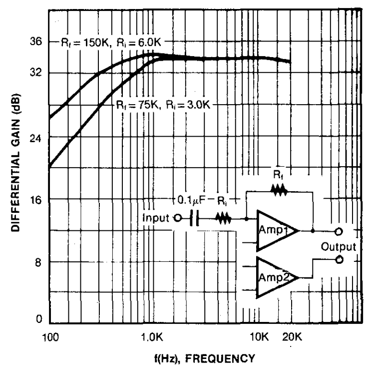


Fig. 9 POWER SUPPLY CURRENT

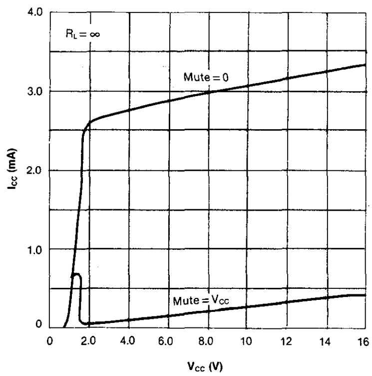


Fig. 10 MAXIMUM ALLOWABLE LOAD POWER

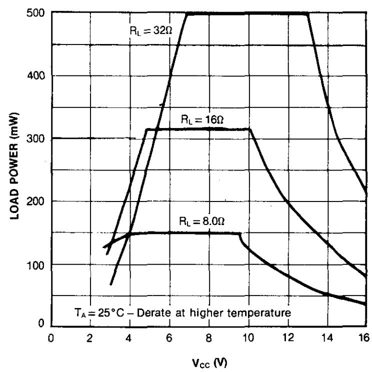


Fig. 11 PSRR vs FREQUENCY ($C_2 = 10\mu F$)

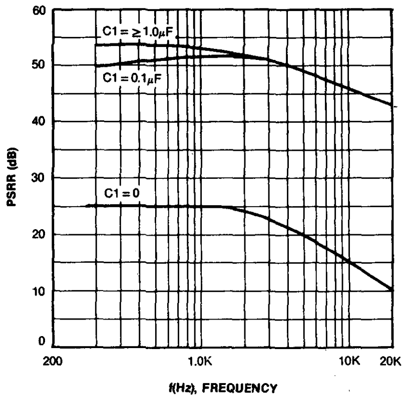


Fig. 12 PSRR vs FREQUENCY ($C_2 = 5.0\mu F$)

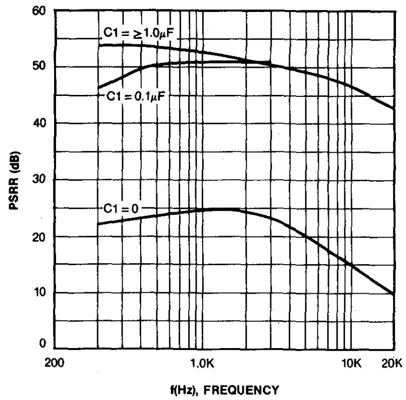


Fig. 13 PSRR vs FREQUENCY ($C_2 = 1.0\mu F$)

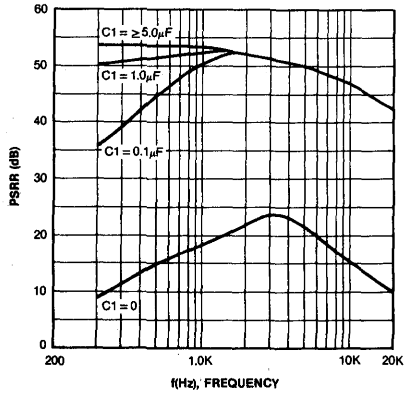
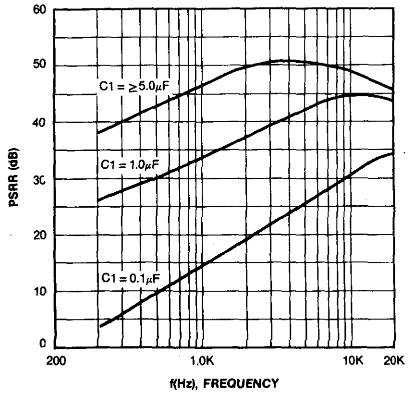


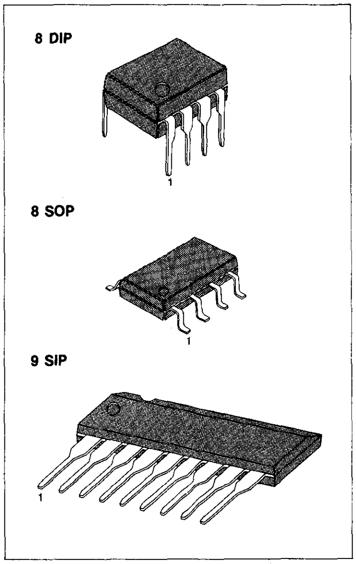
Fig. 14 PSRR vs FREQUENCY ($C_2 = 0$)



LOW VOLTAGE AUDIO POWER AMPLIFIER

The LM386/S/D is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep the external part count low, but the addition of an external resistor and capacitor between Pins 1 and 8 will increase the gain to any value up to 200.

The inputs are ground referenced, while the output is automatically biased to one half the supply voltage. The quiescent power drain is only 30 milliwatts when operating from a 6-volt supply, making the LM386 ideal for battery operation.



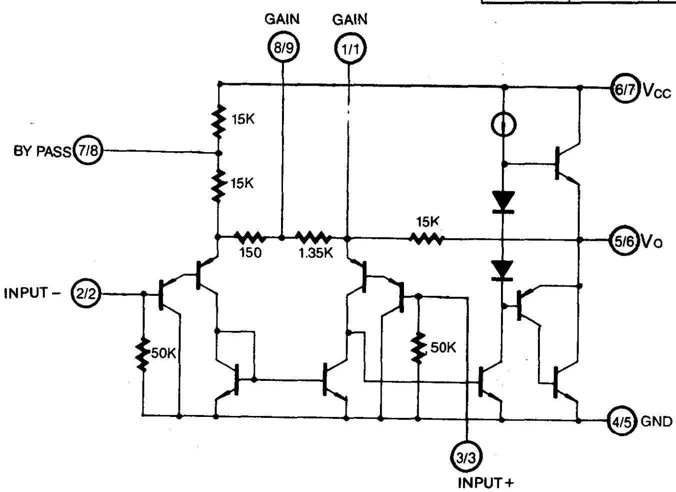
FEATURES

- **Battery operation.**
- **Minimum external parts.**
- **Wide supply voltage range: 4V ~ 12V (LM386)**
  4V ~ 9V (LM386S/D)
- **Low quiescent current drain (4mA.)**
- **Voltage gains : 20 ~ 200.**
- **Ground referenced input.**
- **Self-centering output quiescent voltage.**
- **Low distortion.**
- **3 kinds of package types**
  LM386 (8 Dip), LM386S (9 Sip), LM386D (8 Sop)

ORDERING INFORMATION

Device	Package	Operating Temperature
LM386	8 DIP	−20 ~ +70°C
LM386S	9 SIP	
LM386D	8 SOP	
LM386G	PELLET	

SCHEMATIC DIAGRAMS



◯/ : LEFT (LM386/D)
RIGHT (LM386S)

Fig. 1

CONNECTION DIAGRAM

(LM386/D)

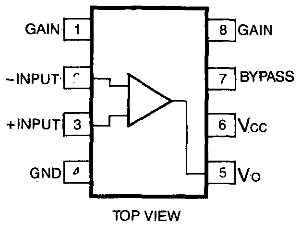


Fig. 2

(LM386S)

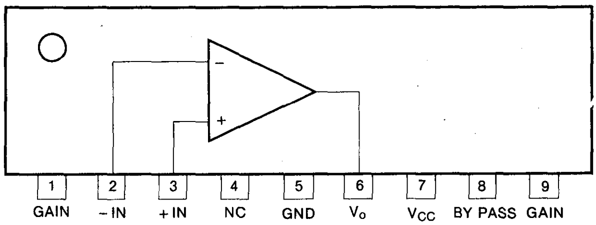


Fig. 3

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic		Symbol	Value	Unit
Supply Voltage		V_{CC}	15	V
Power Dissipation	LM386	P_d	660	mW
	LM386S		500	
	LM386D		300	
Input Voltage		V_i	±0.4	V
Operating Temperature		T_{opr}	−20 ~ +70	°C
Storage Temperature		T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 6V, R_L = 8Ω, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescient Circuit Current	I_{CC}	$V_i = 0$		4	8	mA
Output Power	P_o	V_{CC} = 6V, THD = 10%	250	325		mW
		V_{CC} = 9V, THD = 10%	500	700		mW
Voltage Gain (D-Type)	A_V	Pins 1 and 8 Open		26		dB
		10μF from Pin 1 to 8		46		
Bandwidth (D-Type)	BW	Pins 1 and 8 Open		300		KHz
		10μF from Pin 1 to 8		60		
Total Harmonic Distortion (D-Type)	THD	P_o = 125mW, Pins 1 and 8 Open		0.2		%
Input Resistance	R_i			50		KΩ
Input Bias Current	I_b	Pins 1 and 8 Open		250		nA

TYPICAL APPLICATIONS (LM386)

Amplifier with Gain=50 (34 dB)

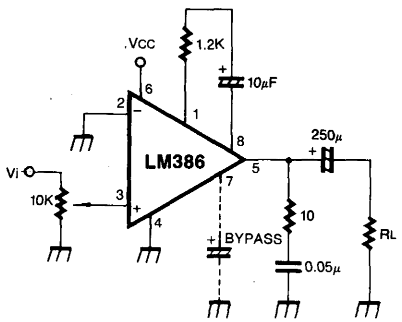


Fig. 4

Low Distortion Power Wienbridge Oscillator

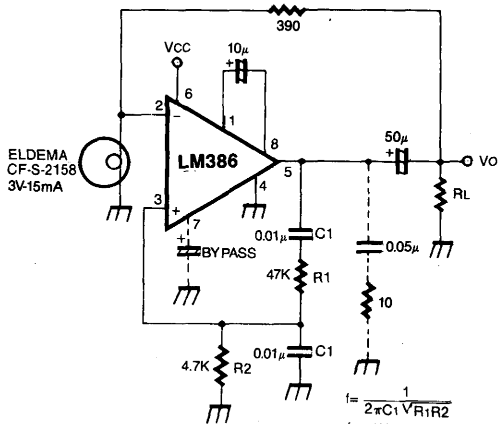


Fig. 5

Square Wave Oscillator

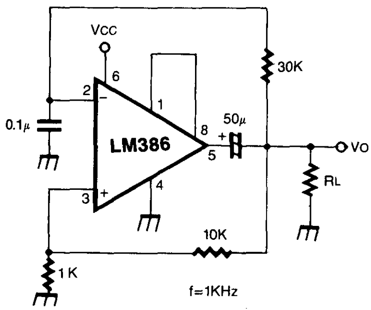


Fig. 6

Amplifier with Bass Boost

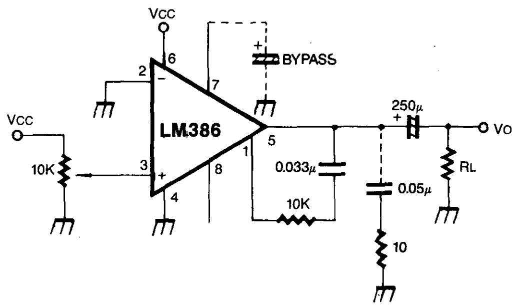


Fig. 7

AM Radio Power Amplifier

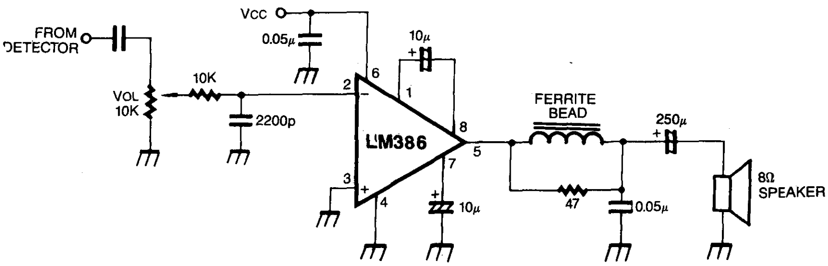
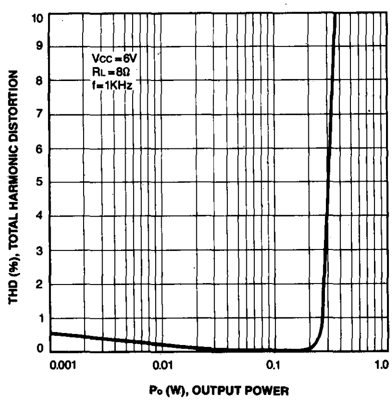
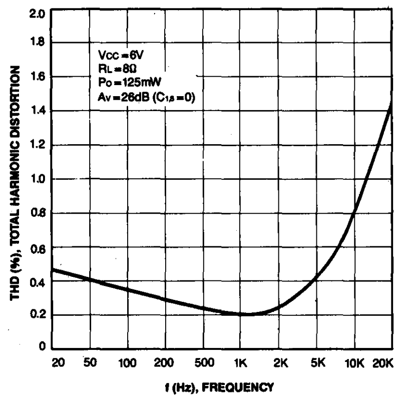


Fig. 8

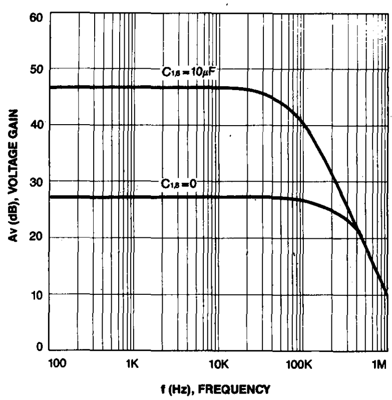
TOTAL HARMONIC DISTORTION-OUTPUT POWER



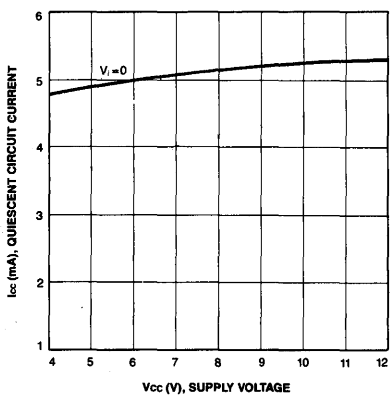
TOTAL HARMONIC DISTORTION-FREQUENCY



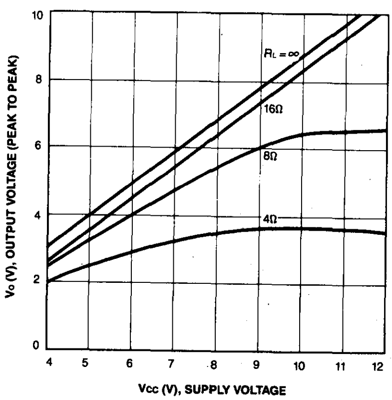
VOLTAGE GAIN—FREQUENCY



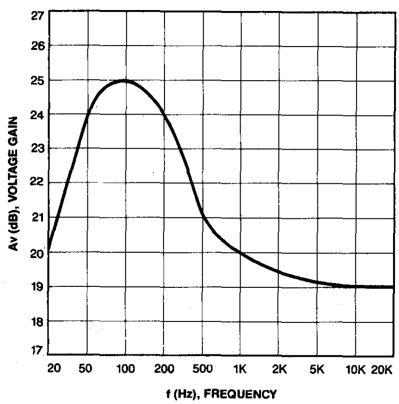
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE



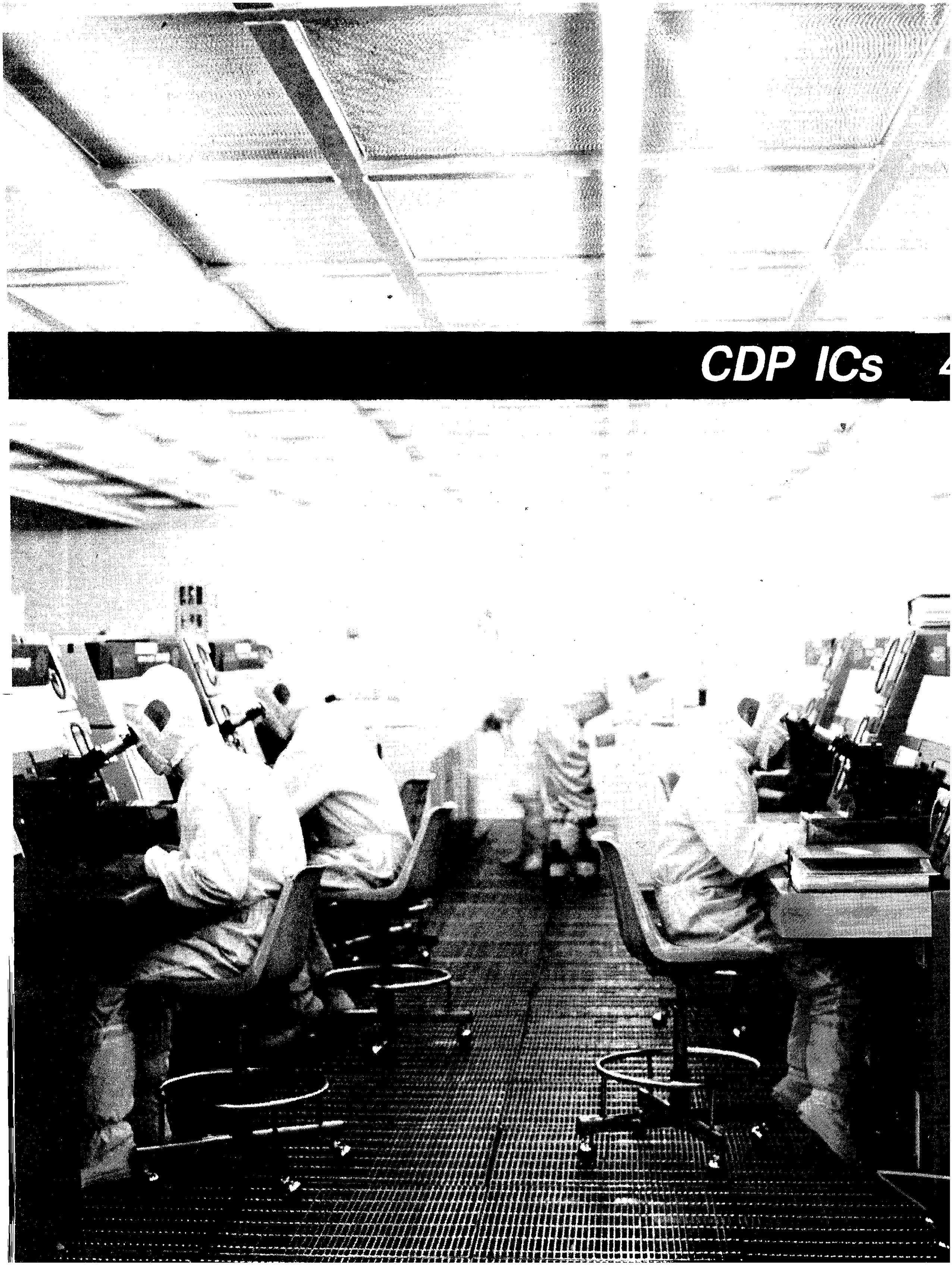
OUTPUT VOLTAGE SWING-SUPPLY VOLTAGE



FREQUENCY RESPONSE WITH BASS BOOST



CDP ICs 4

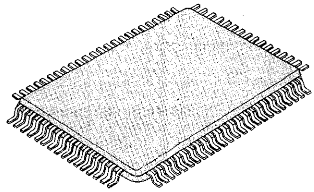


CDP APPLICATION

DIGITAL SIGNAL PROCESSOR

The KS5990 is a monolithic integrated circuit designed for compact disc players application. It is consisting of 16KSRAM, digital filter and digital signal processing circuits.

80 FQP



FEATURES

- **All digital signals for regeneration are processed using one chip.**
- **Internal aperture compensation digital filter**
- **EFM-PLL circuit for bit clock regeneration**
- **EFM data demodulation**
- **Frame synchronous signal detection, protection**
- **Compensation using mean value, prior value retention**
- **Subcode signal demodulation subcode Q detection**
- **CLV servo for spindle motor**
- **8-bit tracking counter**
- **CPU interface with serial bus**
- **Subcode Q reaister**
- **Built-in 17th digital filter**
- **Built-in 16KSRAM**
- **80 Quad flat package type**

4

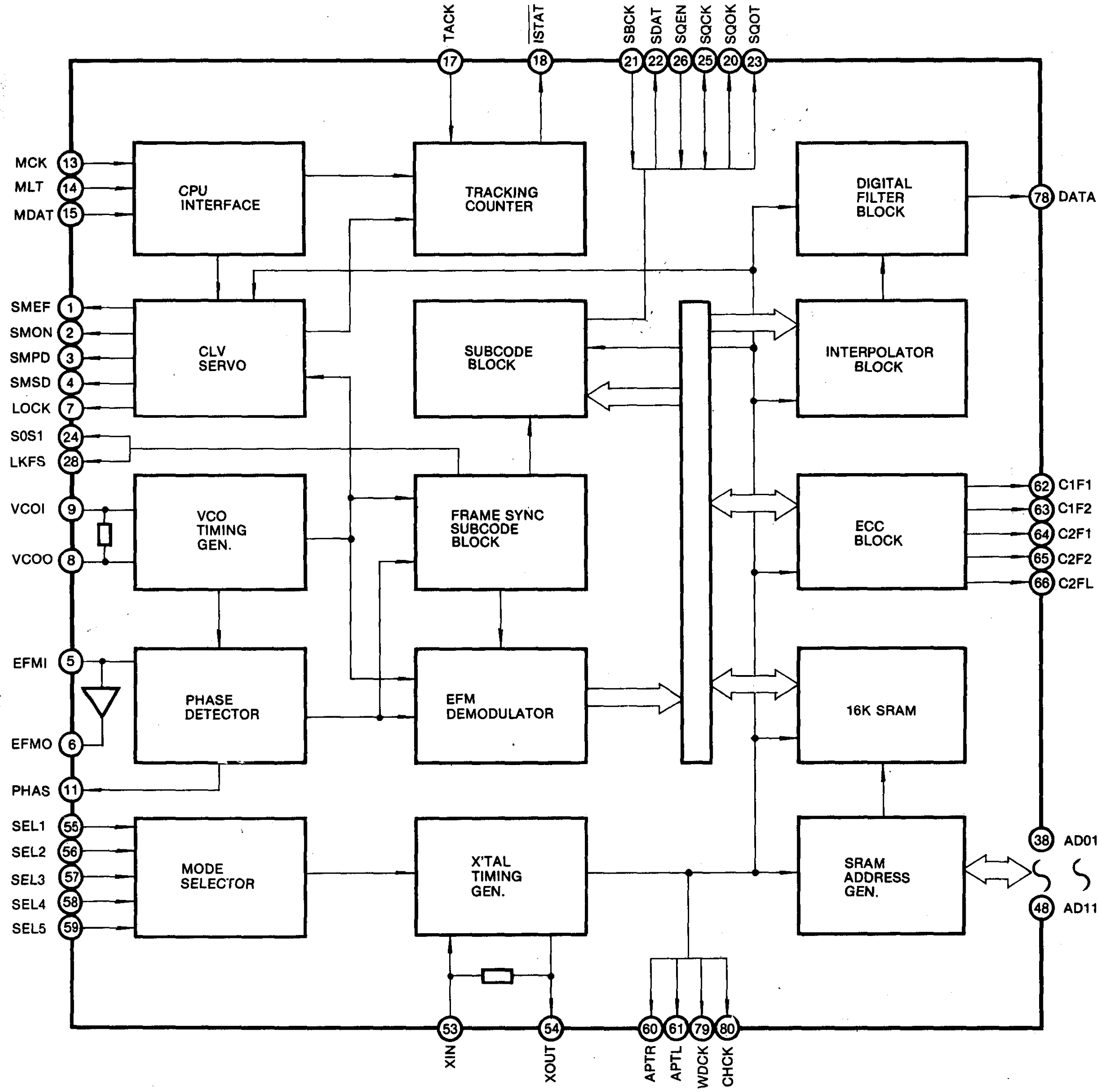
ORDERING INFORMATION

Device	Package	Operating Temperature
KS5990	80 FQP	−20 ~ +75°C

ABSOLUTE MAXIMUM RATING (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 ~ +7	V
Input Voltage	V_I	−0.3 ~ +7	V
Output Voltage	V_O	−0.3 ~ +7	V
Operating Temperature	T_{opr}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input High Level Voltage	$V_{IH}1$	Note 1	0.7 V_{DD}		V_{DD}	V
Input Low Level Voltage	$V_{IL}1$	Note 1	0		0.3 V_{DD}	V
Input High Level Voltage	$V_{IH}2$	Note 2	0.8 V_{DD}			V
Input Low Level Voltage	$V_{IL}2$	Note 2			0.2 V_{DD}	V
Output High Level Voltage	V_{OH}	I_{OH} = −1mA	V_{DD} − 0.5		V_{DD}	V
Output Low Level Voltage	V_{OL}	I_{OL} = 1mA	0		0.4	V
Input Leak Current	I_{LC}	V_{IN} = 0 ~ 5.5V	−5		+5	μA
Three-State Pin Output Leak Current	I_{LD}	V_{OUT} = 0 ~ 5.5V	−5		+5	μA
SRAM Input Leak Current	I_{SLC}	V_{IN} = 0 ~ 5.5V	−5		+200	μA

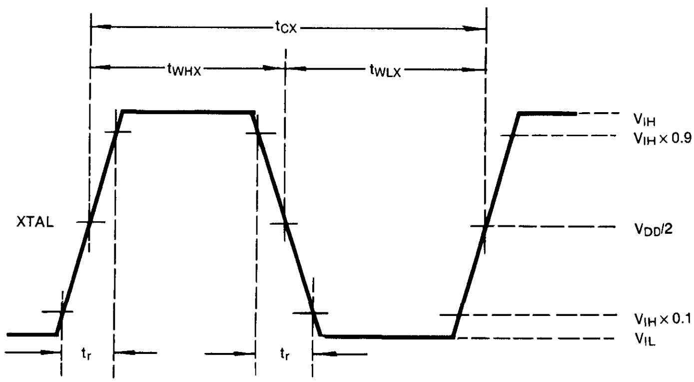
Note 1. Related pins—EFMI, RESET, TEST, MUTE, SEL 2 ~ 5, MLT, MDAT, SQEN, SQCK.
Note 2. Related pins—TRCK, MCK, SRAM.

2. AC Characteristics

A. XIN Pin, VCOI Pin

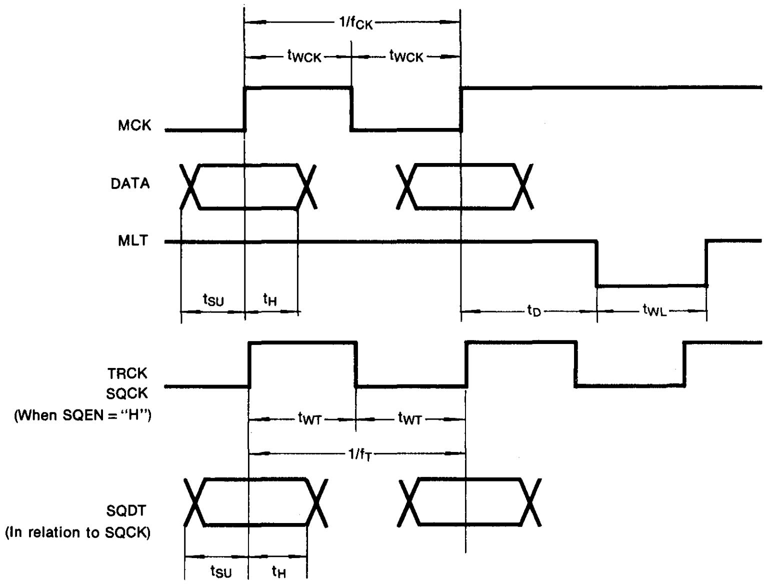
(1) When pulse applied to XIN and VCO (V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 25°C, unless otherwise specified)

Item	Symbol	Min	Typ	Max	Unit
"H" Level Pulse Width	t_{WHX}	20			ns
"L" Level Pulse Width	t_{WLX}	20			ns
Pulse Frequency	t_{CX}	55			ns
Input "H" Level	V_{IH}	V_{DD} − 1.0			V
Input "L" Level	V_{IL}			0.8	V
Rising Time Breaking Time	t_R, t_F			15	ns



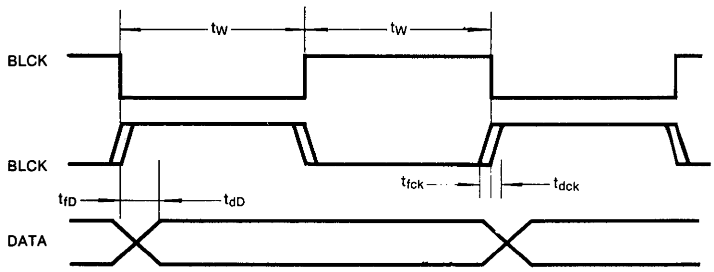
B. Pins MCK, DATA, MLT, TRCK, SQCK
($V_{DD} = 5.0V \pm 10\%$, $V_{SS} = 0V$, $T_{opr} = 25°C$)

Item	Symbol	Min	Typ	Max	Unit
Clock Frequency	f_{CK}			1	MHz
Clock Pulse Width	t_{WCK}	300			ns
Setup Time	t_{SU}	-300			ns
Hold Time	t_H	300			ns
Delay Time	t_D	300			ns
Latch Pulse Width	t_{WL}	300			ns
CNIN SQCK Frequency	f_T			1	MHz
CNIN SQCK Pulse Width	t_{WT}	300			ns



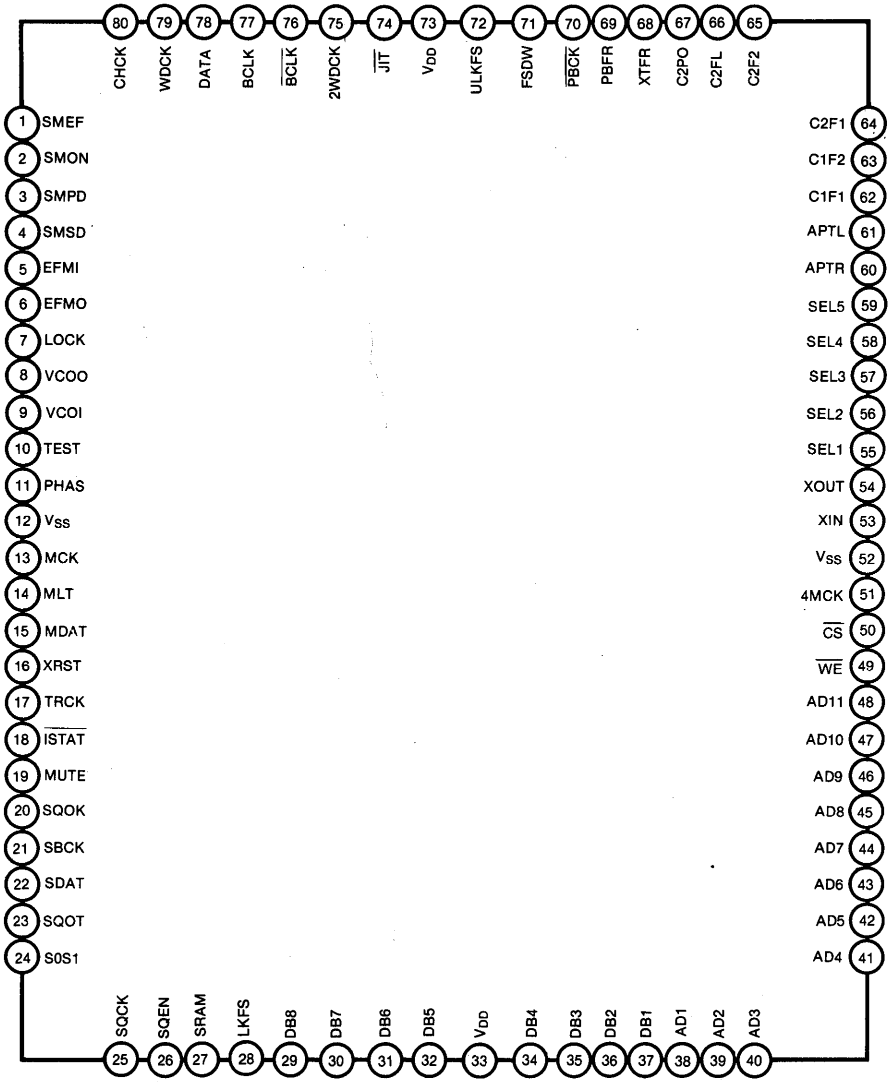
C. DAC Interface ($V_{DD}=5V \pm 10\%$, $V_{SS}=0V$, $T_{opr}=25°C$, $C_L=50pF$)

Item	Symbol	DF is OFF			When DF ON			Unit
		Min	Typ	Max	Min	Typ	Max	
Clock Pulse Width	t_W		236			118		ns
Clock Skew (Fast)	t_{fck}			40			40	ns
Clock Skew (Delay)	t_{dck}			40			40	ns
Data Skew (Fast)	t_{fD}			0			0	ns
Data Skew (Delay)	t_{dD}			80			80	ns



*Note: CHCK, WDCK, APTR, APTL
DA01 through DA16 during parallel DA conversion or C1F1, C1F2, C2F1, C2F2, C2FL, C2PO, XTFR, 2WDCK, DATA during serial conversion.

PIN CONFIGURATION



PIN DESCRIPTION

No.	Symbol	I/O	Description
1	SMEF	O	Pin 1 output is switched constant when output filter of the spindle motor is energized.
2	SMON	O	ON/OFF control for spindle motor.
3	SMPD	O	Spindle motor drive. Provides rough control during CLV-S mode and phase control during CLV-P mode.
4	SMSD	O	Spindle motor drive. Controls speed during CLV-P mode.
5	EFMZ	I	EFM signal from RF amplifier.
6	EFMO	O	Controls slice level of the EFM signal.
7	LOCK	O	The output of pin 7 reflects the status of the GFS signal which is sampled at PBFR/16. When the GFS signals is "H", but, when the signal has remained "L" for at least 8 samples, the output of pin 7 is "L".
8	VCOO	O	VCO output. The frequency is f = 8.6436MHz, when locked by the DBFR signal.
9	VCOI	I	VCO input.
10	TEST	I	(0V).
11	PHAS	O	The output of Pin 11 provides phase comparison of EFM signal and VCO/2.
12	V_{SS}	—	GND (0V).
13	MCK	I	Pin 13 provides serial transmission clock from the CPU. Data is latched on the leading edge of the clock.
14	MLT	I	Pin 14 provides latch input from the CPU. 8-bit shift register data (serial data received from the CPU) is latched in each of the registers.
15	MDAT	I	Serial data from the CPU.
16	XRST	I	System reset ("L").
17	TRCK	I	Tracking pulse input.
18	$\overline{\text{ISTAT}}$	O	Output reflecting internal condition as designated by address.
19	MUTE	I	Muting input. MUTE is "L" when ATTM of internal register A is "L" (normal condition). MUTE is "H" when meting condition is set.
20	SQOK	O	Output the results CRC check of subcode Q.
21	SBCK	I	Clock input for subcode serial output.
22	SDAT	O	Serial output of subcode.
23	SQDT	O	Output of subcode Q.
24	S0S1	O	Output of subcode sync S0 + S1.
25	SQCK	I/O	Clock for reading subcode Q.
26	SQEN	I	Input for selecting SQCK (L; SQCK is output, H; SQCK is input)
27	SRAM	I	SRAM is "H" in Nomal, SRAM is "L" when system is testing.
28	LKFS	O	Display output for frame sync lock status.

4

PIN DESCRIPTION (Continued)

No.	Symbol	I/O	Description
29	DB8	I/O	Data pin for external RAM. DATA8 (MSB) in test mode. Hi-Z in nomal
30	DB7	I/O	Data pin for external RAM. DATA7 in test mode. Hi-Z in nomal
31	DB6	I/O	Data pin for external RAM. DATA6 in test mode. Hi-Z in nomal
32	DB5	I/O	Data pin for external RAM. DATA5 in test mode. Hi-Z in nomal
33	V_{DD}	—	Power supply (+ 5V).
34	DB4	I/O	Data pin for external RAM. DATA4 in test mode. Hi-Z in nomal
35	DB3	I/O	Data pin for external RAM. DATA3 in test mode. Hi-Z in nomal
36	DB2	I/O	Data pin for external RAM. DATA2 in test mode. Hi-Z in nomal
37	DB1	I/O	Data pin for external RAM. DATA1 (LSB) in test mode. Hi-Z in nomal
38	AD01	O	(LSB)
39	AD02	O	In nomal mode (TEST = 'L', SRAM = 'H'), these pins are High impedance (Hi-Z) In test mode (TEST = 'H', SRAM = 'L'), these pins are Output address of external RAM
40	AD03	O	
41	AD04	O	
42	AD05	O	
43	AD06	O	
44	AD07	O	
45	AD08	O	
46	AD09	O	
47	AD10	O	
48	AD11	O	(MSB)
49	$\overline{WE}$	I/O	In nomal mode, this is WE output. In test mode, write enable input.
50	$\overline{CE}$	I/O	In nomal mode, this is CE output. in test mode, chip enable input.
51	4MCK	O	Divider output for crystal. f = 4.2336MHz
52	V_{SS}	—	GND (0V)
53	XIN	I	Input to crystal oscillator circuit. Depending on the mode the frequency is either f = 8.4672 r 16.9344MHz.
54	XOUT	O	Output from crystal oscillator circuit. Depending on the mode the frequency is either f = 8.4672 or 16.9344MHz.
55	SEL1	I	Mode selection input 1.
56	SEL2	I	Mode selection input 2.
57	SEL3	I	Mode selection input 3.
58	SEL4	I	Mode selection input 4. Code switch input for audio data output. 2's complement output when "L", offset binary output when "H".
59	SEL5	I	Mode selection input 5. Code switch input for audio data output. Serial output when "L", parallel output when "H".

PIN DESCRIPTION (Continued)

No.	Symbol	I/O	Description
60	APTR	O	Output for aperture compensation. "H" when R-ch.
61	APTL	O	Output for aperture compensation. "H" when L-ch.
62	C1F1	O	Monitor output reporting status of error correction for C1 decoder. When SEL5 = 'L', DA01 (LSB of parallel audio data) is output when SEL5 = 'H'.
63	C1F2	O	Monitor output reporting status of error correction for C1 decoder when SEL5 = 'L', DA02 is output when SEL5 = 'H'.
64	C2F1	O	Monitor output reporting status of error correction for C2 decoder when SEL5 = 'L', DA03 is output when SEL5 = 'H'.
65	C2F2	O	Monitor output reporting status of error correction for C2 decoder when SEL5 = 'L', DA04 is output when SEL5 = 'H'.
66	C2FL	O	When SEL5 = 'L', output of status condition. C2FL is set 'H' when the C2 sequence. Presently being corrected becomes impossible to correct. DA05 is output when SEL5 = 'H'.
67	C2PO	O	Display output of the C2 pointer when SEL5 = 'L', DA06 is output when SEL5 = 'H'.
68	XTFR	O	When SEL5 = 'L', output of read frame dock which is 7.35KHz of the crystal system. DA07 is output when SEL5 = 'H'.
69	PBFR	O	When SEL5 = 'L', output of write frame clock which is 7.35KHz when locked by the crystal system. DA08 is output when SEL5 = 'H'.
70	$\overline{PBCK}$	O	When SEL5 = 'L', output of VCO/2 (f = 4.3218MHz when locked by the EFM signal). DA09 is output when SEL5 = 'H'.
71	FSDW	O	When SEL5 = 'L', output for unprotected frame sync patterns. DA10 is output when SEL5 = 'H'.
72	ULKFS	O	Output for display of status of frame sync protection when SEL5 = 'L', DA11 is ouput when SEL5 = 'H'.
73	V_{DD}	—	Power supply (+5V).
74	$\overline{JIT}$	O	When SEL5 = 'L', output for display of either RAM overflow or underflow for +4 frame jitter absorption. DA12 is output when SEL5 = 'H'.
75	ZWDCK	O	When SEL5 = 'L', output for strobe signal (352.8KHz when DF is ON, 176.4KHz when DF is OFF). DA13 is output when SEL5 = 'H'.
76	$\overline{BLCK}$	O	When SEL5 = 'L', inverse output of BLCK. DA14 is output when SEL5 = 'H'.
77	BLCK	O	When SEL5 = 'L', bit clock output (4.2336MHz when DF is ON, 2.1168MHz when DF is OFF) DA15 is output when SEL5 = 'H'.
78	DATA	O	Serial data output of audio signal when SEL5 = 'L'. DA16 is output when SEL5 = 'H'.
79	WDCK	O	Strobe signal output. Output is 176.4KHz when DF is on. Output is 88.2KHz when DF is off.
80	CHCK	O	Strobe signal output. Output is 88.2KHz when DF is on. Output is 44.1KHz when DF is off.

DESCRIPTION OF FUNCTION

MODE SELECTOR

To control several blocks in KS5991, there are 5 selecting pin signals. Table 1. Shows selected mode by these signals.

Input Pins					Function*				
SEL1	SEL2	SEL3	SEL4	SEL5	XIN	DF	P/S	OB/2'S	CD ROM/Audio
0	1	0	0	0	16M	ON	S	2'S	Audio
0	1	0	1	1	16M	ON	P	OB	Audio
0	1	1	0	0	16M	OFF	S	2'S	Audio
0	1	1	1	1	16M	OFF	P	OB	Audio
1	0	0	0	0	8M	ON	S	2'S	Audio
1	0	0	1	1	8M	ON	P	OB	Audio
1	0	1	0	0	8M	OFF	S	2'S	Audio
1	0	1	1	1	8M	OFF	P	OB	Audio
1	1	1	1	0	8M	OFF	S	2'S	CD ROM

Table 1. Mode Selection

* Note:
- 8M/16M: Selection of either the XIN or XOUT clocks will provide either a 8.4672MHz or 16.9344MHz signal.
- DF: Digital Filter
- P/S: Parallel mode/serial mode
- OB/2'S: Offset

- Clock selection
  Selectioin of an 16.9344MHz or 8.4672MHz oscillator clock is possible at pins XIN and XOUT. However only 16.9344MHz clocks are provided for digital out usage.
- Digital filter selection
  When the digital filter function is switched to ON, all signals on the DAC interface are handled at twice the normal speed.
- Parallel/Serial output selection
  When the output is parallel, 16-bit parallel data is output from pins DA01 through DA16.
  When the output is serial, the following signals are output at pin DA01 through DA16.

DATA (DA16)	Serial data output (MSB or LSB first output)
BLCK (DA15)	Internal system clock (with DF ON 4.2336MHz and with DF OFF 2.1168MHz)
$\overline{\text{BLCK}}$ (DA14)	Bit clock (BLCK inversion signal)
2WDCK (DA13)	4X multiplied CHLK signal
$\overline{\text{JIT}}$ (DA12)	Jitter Margin Overflow/Underflow signal
ULKFS (DA11)	Display output of frame sync protection status
FSDW (DA10)	Unguarded (unprotected) frame sync signal
PBCK (DA09)	Signal at 1/2 V_{CO} pin cycle times. When locked 4.3218MHz
PBFR (DA08)	Write Frame Clock signal. When locked 7.35KHz.
XTFR (DA07)	Read Frame Clock signal. Crystal system 7.35KHz.
C2PO (DA06)	C2 Pointer signal
C2FL (DA05)	Correction mode output, C2FL = C2F1, C2F2
C2F2 (DA04) C2F1 (DA03)	Monitor Output of Error Correction Mode for C2 Decode
C1F2 (DA02) C1F1 (DA01)	Monitor Output of Error Correction Mode for C1 Decode

- OFFSET Binary/2's Complement Selection
  When pin SEL4 is at "H" output occurs at OFFSET BINARY; when it is at "L" output occurs at 2's complement.
- CDROM/AUDIO Selection
  When SEL1 = SEL2 = SEL3 = "H", CDROM is selected. Then the C2 pointer is output with each byte (8 bits) and neither the mean value interpolation nor the preceding value hold are exercised. That is, if an error occurs in the upper 8 bits of a 16-bit data, only the C2 pointer related to those upper 8 bits switches to "H" while the lower 8 bits are handled as correct data.

Microcomputer Interface

Data from microcomputer are inputed through MDAT pin by MCK which is clock signal of microcomputer and pulse signal through MLT pin is for inputed data load one of 6 kinds of control registers.

Fig. 1 Shows the timing diagram of data input from microcomputer

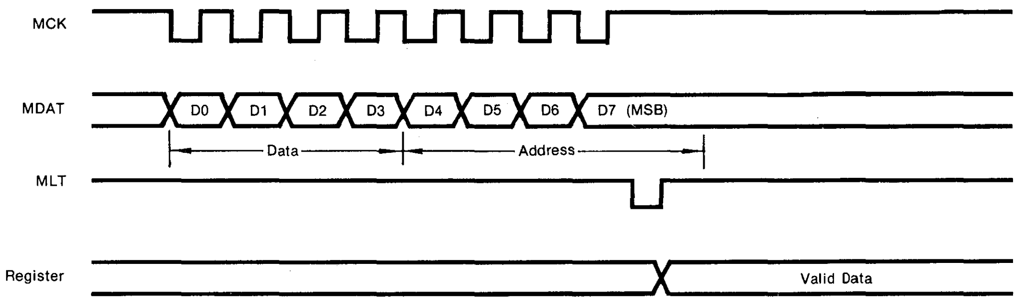


Fig. 1 Data Input Timing Diagram

According to the address of MDAT, control register is selected as below table 1.

Control Register	Comment	Address D7~D4	Data				$\overline{ISTAT}$ Pin
			D3	D2	D1	D0	
CNTL-Z	Data Control	1 0 0 1	ZCMT	HIPD	NCLV	CRCD	Hi-Z
CNTL-S	Frame Sync Protection Attenuation Control	1 0 1 0	FSEM	FSEL	WSEL	ATTM	Hi-Z
CNTL-L	Tracking Counter Lower 4 Bit	1 0 1 1	TRC3	TRC2	TRC1	TRC0	$\overline{\text{Complete}}$
CNTL-U	Tracking Counter Upper 4 Bit	1 1 0 0	TRC7	TRC6	TRC5	TRC4	$\overline{\text{COUNT}}$
CNTL-W	CLV Control	1 1 0 1	COM	WB	WP	GAIN	Hi-Z
CNTL-C	CLV Mode	1 1 1 0	CLV Mode				$\overline{PW \geq 64}$

Table 1. Data of Selected Control Register

According to D0 through D1 DAA,
The function of each control registers is described below

1) CNTL-Z Register

This is a control register for the zero cross mute of audio data, PHAS, the control signal of phase servo and CRCF data.

		Data = 0	Data = 1
ZCMT	D3	Zero cross mute "OFF"	Zero cross mute "ON"
HIPD	D2	Phase normally active	Phase convert "L" to "Hi-Z" by LKFS
NCLV	D1	Phase servo driven by frame sync	Phase servo be controlled by base counter
CRCQ	D0	SQDT output without SQOK	SQDT = CRCF during the rising time of S0S1

2) CNTL-S Control Register

This is a control register for frame sync. Protection and attenuation.

FSEM	FSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	Clock
0	±3
1	±7

ATTM	MUTE	dB
0	0	0
0	1	–
1	0	−12
1	1	−12

3) CNTL-L, U Control Register

When the numbers of tract will be counted is inputed from microcomputer, data loaded these registers. (See tracking counter)

4) CNTL-W Control Register

This is a control register for CLV-Servo

		Data = 0	Data = 1	Comments
COM	D3	XTFR/4 & PBFR/4	XTFR/4 & PBFR/4	Phase comparative frequency during PHASE-mode
WB	D2	XTFR/32	XTFR/16	Bottom hold period during SPEED and HSPEED-mode
WP	D1	XTFR/4	XTFR/2	Peak hold period during SPEED-mode
GAIN	D0	−12dB	0dB	SMPD gain during SPEED & HSPEED-mode

5) CNTL-C Control Register

This is a control register for CLV-Servo

Mode	D7 ~ D4	D3 ~ D0	SMDP	SMSD	SMEF	SMON
Forward	1 1 1 0	1 0 0 0	H	Hi-Z	L	H
Reverse		1 0 1 0	L	Hi-Z	L	H
SPEED		1 1 1 0	SPEED mode	Hi-Z	L	H
HSPEED		1 1 0 0	HSPEED mode	Hi-Z	L	H
PHASE		1 1 1 1	PHASE mode	PHASE mode	Hi-Z	H
XPHSP		0 1 1 0	SPEED, PHASE mode	Hi-Z or PHASE mode	L or Hi-Z	H
VPHSP		0 1 0 1	SPEED PHASE mode	Hi-Z or PHASE mode	L or Hi-Z	H
STOP		0 0 0 0	L	Hi-Z	L	L

TRACKING COUNTER

This counter is used to improve track-jumping characteristics. The number of tracks that are to be jumped are loaded into either register CNTL-L or CNTL-U. After either register CNTL-L or CNTL-U have been loaded and at the rising edge of the next MLT, TRCK pulse count begins. n (if register CNTL-L = register = CNTL-U = 0, then n = 256) is loaded into the register, and when the address is set in CNTL-L, the signal ($\overline{\text{COMPLETE}}$) is output from pin SENS at high level until the "n"th pulse and then at low level for succeeding pulses. When the address is set in CNTL-U, the signal ($\overline{\text{COUNT}}$) TRCK/2n is output. Fig. 2 shows the timing of the tracking counter.

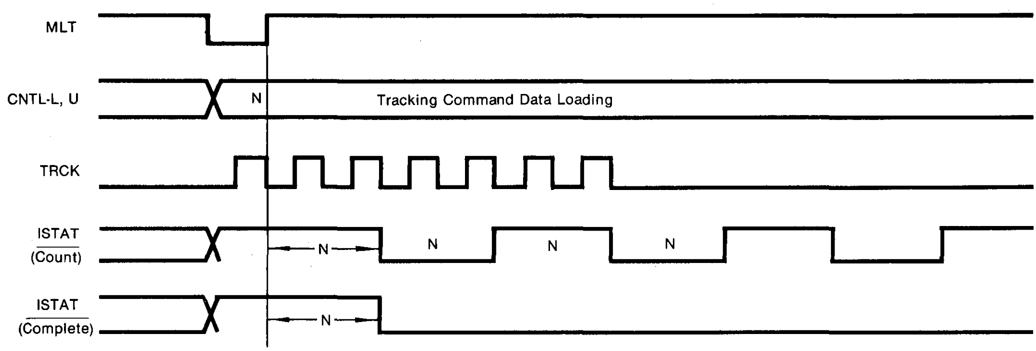


Fig. 2 Tracking Count Timing Chart

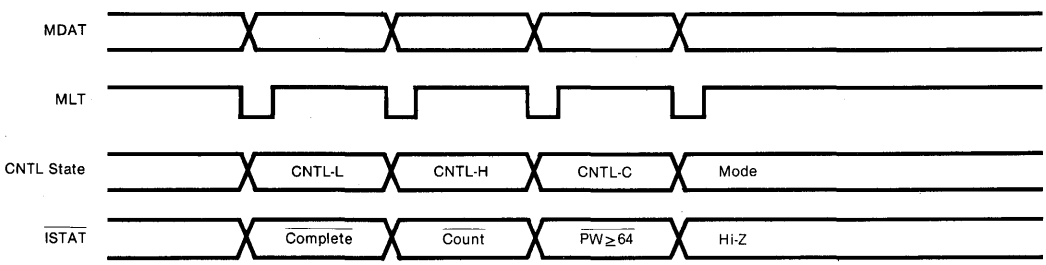
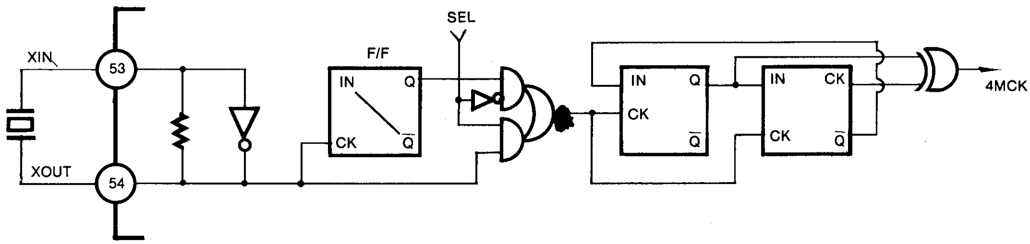


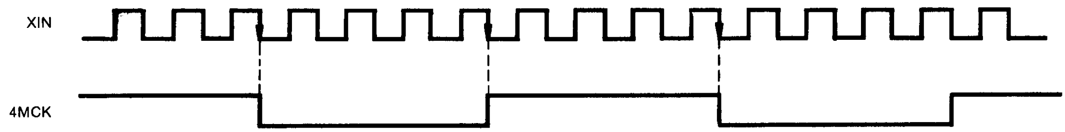
Fig. 3 $\overline{\text{ISTAT}}$ Output Signal by CNTL Register

X'TAL OSCILLATION

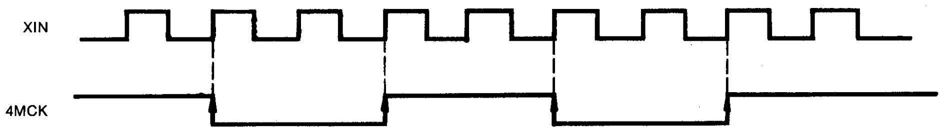
1) Block Diagram



2) Timing Chart (SEL = 0) in Use f = 16.9344MHz X'tal OSC.



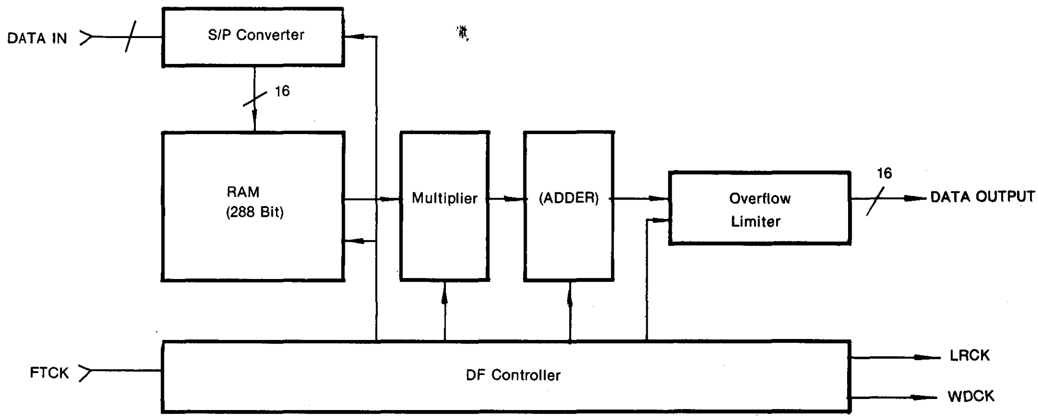
3) Timing Chart (SEL = 1) in use f = 8.4672MHz X'tal OSC.



DIGITAL FILTER

KS5990 is built-in 17th FIR Digital Filter.
The digital filter consists of RAM, multiplier, serial to parallel and parallel to serial converter and controller.

1) Block Diagram

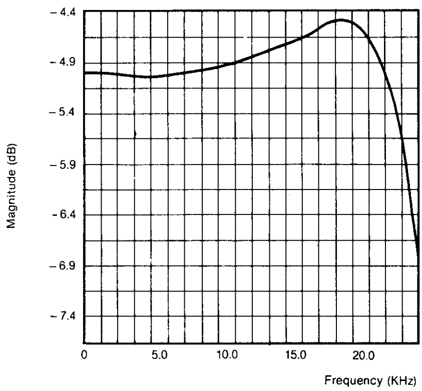


2) Specification

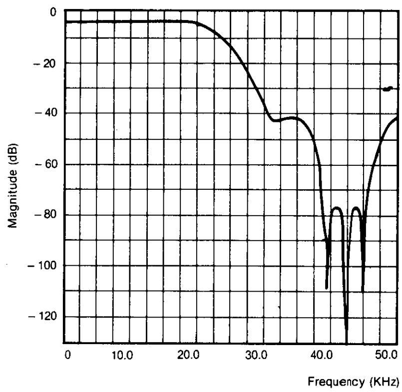
	DC through 18KHz ripple 20KHz of attenuation against 1KHz	±0.07dB max 0.65dB max
	44.1±1KHz attenuation against 1KHz 44.1±5KHz attenuation against 1KHz 44.1±10KHz attenuation against 1KHz 44.1±20KHz attenuation against 1KHz −30dB frequency range against 1KHz −60dB frequency range against 1KHz	87dB min 58dB min 44dB min 10dB min 44.1±14KHz 44.1±4KHz

3) Frequency Characteristic

A. Ripple Characteristic Graph



B. Low Pass Filter Frequency Characteristic Graph



4

EFM BLOCK

The EFM Block is made up of an EFM Demodulator which demodulates the EFM data inputted from a recorded disc, EFM Phase Detector, Frame Sync Detector/Protector/Inserter, Subcode Sync Detector, and Controller for the EFM Block.

1) EFM Phase Detector

AS the EFM signal inputted from the disc contains 2.16 MHz component, a 4.32 MHz bit clock is generated to detect the phase of the signal. The PBCK outputs the result to the PHAS terminal after detecting the phase on the edge of the EFM signal. The relationship between the EFM signal and the PBCK is explained in the following Timing Chart.

A. In normal operation

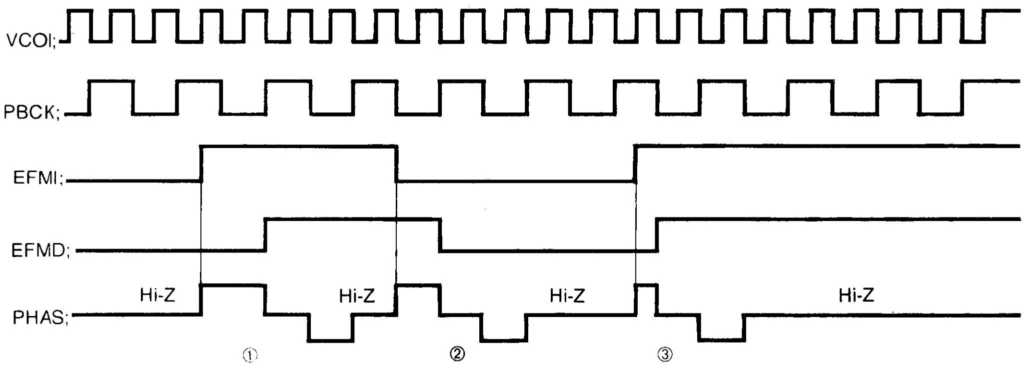


Fig. 5 EFM Phase Detection Timing Chart

Case ①: When the EFM signal is slower than the VCO
Case ②: When the EFM signal is locked up the VCO
Case ③: When the EFM signal is faster than the VCO

B. In abnormal operation

When the HIPD of CNTL-Z is chosen as 'L' from M-COM, the detector of the EFM phase operates as in Fig. 5. When the HIPD is 'H' and the time 'L' of LKFS is below 3.5T against a PBFS period T, it outputs Hi-Z to the PHAS terminal as long as 'L''. When it is above 3.5T, it outputs Hi-Z as long as 3.5T

2) EFM (Eight to Fourteen) Demodulator

The modulated 14 bit Data is inputted from a disc, then it is inputted into a NRZ-I circuit. As the EFM Data passes by the NRZ-I circuit which converts 14 bit data into 8 bit data, it gets demodulated 8 bit Data. There are two kinds of demodulated data: subcode and PCM data. The subcode data is inputted into the subcode Block, and the PCM Data is written into 16KSRAM by, with both $\overline{CE}$ signal and $\overline{WE}$ signal.

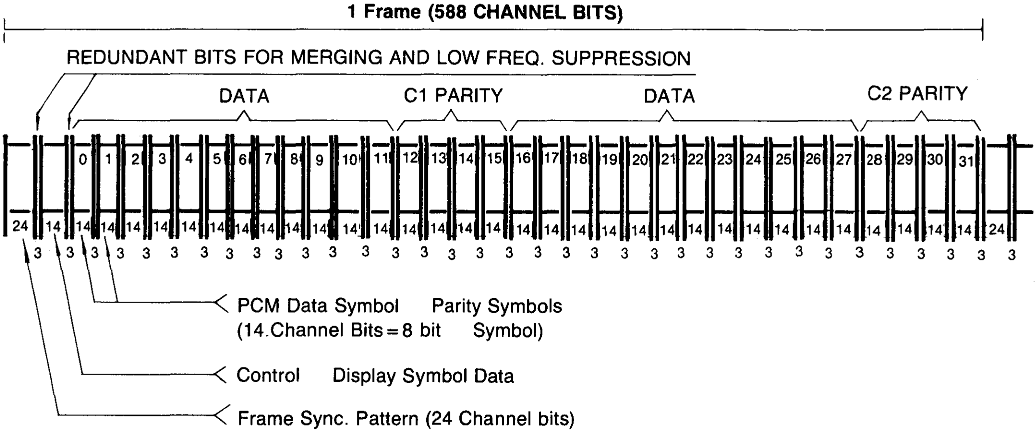
3) Frame Sync Detector/Inserter/Protector

A. Frame Sync Detector

A CDP data is composed of units of frame. A frame is made up of Frame Sync, Subcode Data, PCM Data, Redundancy Data. A Frame sync is detected per frame against this format.

B. Frame Sync Protector/Inserter

There are cases in which the Frame Sync is left out or detected from the data besides the frame sync because of the effects of an error on the disk or Jitter. In this case the frame sync needs to be protected and inserted. To protect the frame sync, a window is made by the use of WSEL signal of CNTL-S Reg. The frame sync which comes into the window is true data, and the frame sync deviating from the window is disregarded.



(Frame Format)

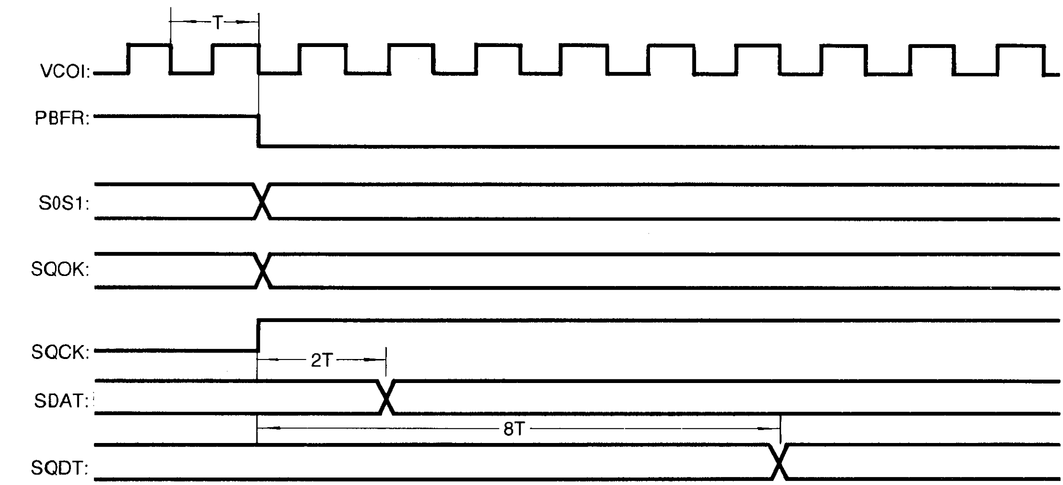
The width of the window is determined by the WSEL signal from the CNTL-S Reg. (cf. CNTL-S) Being inserted frame syncs continuously. If the frame sync is not detected inside a frame sync protection window, insert a frame sync. When the fame sync reaches the number of a frame designated by the FSEM and FSEL by the CNTL-S Reg ULKFS becomes 'L' and the frame sync protection window is disregarded. In this case an outputted frame sync is unconditionally accepted. After the frame sync is received, the ULKFS signal becomes 'H' and accepts a frame sync detected inside the window.

LKFS	ULKFS	Explanation
I	I	When a play back frame sync coincides with a generated frame sync.
O	I	① When a PBFR sync is detected in the window chosen by WSEL even if a play back frame sync does not coincide with a generated frame sync ② In the case of sync insertion because PBFR sync does not coincide with a XTER sync and a frame sync in the window chosen by WSEL is not detected.
O	O	① After inserting a sync as many as the number of frames decided by the FSEM and FSEL of the CNTL-S Reg. because Frame Sync is not detected in a window. ② When PBFR sync is not continuously detected after situation ① happens.

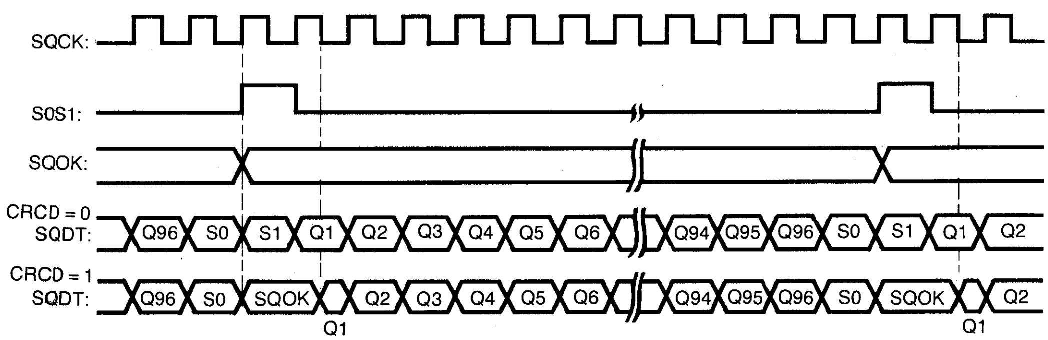
SUBCODE BLOCK

The 14 bit subcode sync signal S0, S1 is detected in the Subcode Sync Block. In a frame delay after the output of S0, S1 is detected. In this case, the signal os S0 + S1 is outputted through the S0S1 terminal, and the signal of S0·S1 is outputted through the SDAT terminal, when the signal S0S1 becomes 'H'. After the 14 bit Subcode Data inputted into the EFMI terminal get EFM Demodulation, an 8 bit P, Q, R, S, T, U, V, W subcode data are outputted to SDAT by SBCK clock after it syncronizes with the signal PBFR. Only Q data is chosen among the 8 subcode data, and it is loaded into 80 shift registers. The CRC-checked results of the loaded data is synchronized with the S0S1 rising edge, and is outputted to the SQCK terminal.
If the result of CRC checking is an error, 'L' is outputted to the SQCK terminal. If it is true, 'H' is outputted to the SQOK terminal. If the CRCD of CNTL-Z mode is 'H', the result of CRC checking is outputted to the SQDT terminal from the Section "H" of S0S1 section 'H' during the SQCK falling edge.
The timing chart of a subcode block is as follows:

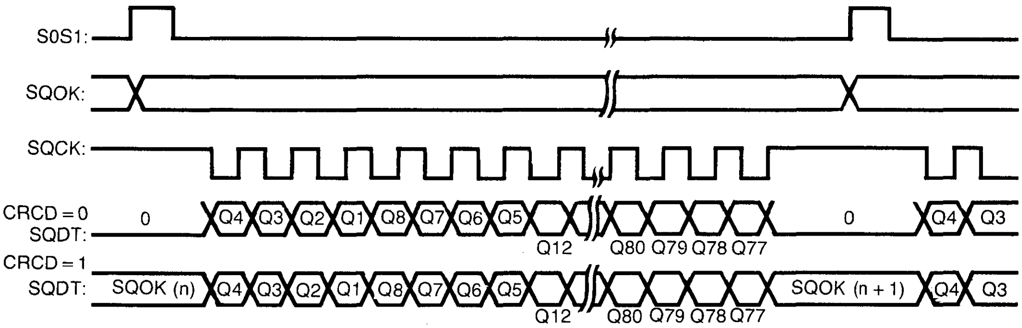
1) In SQEN = 'L': SDAT, SQDT, S0S1, SQOK, VCOI Timing Relation



2) In SQEN = 'L': SQOK, SQDT, S0S1, Timing Chart

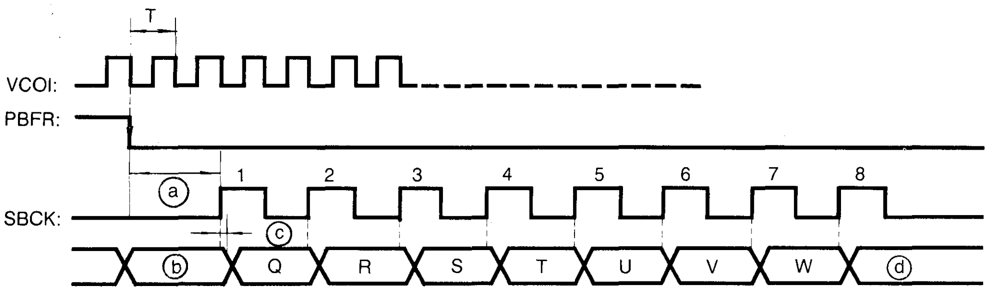


3) In SQEN = 'H': SQOK, SQDT, S0S1, SQCK Timing Chart



Comment: When a SQOK of subcode Q Data is 'H', subcode data is outputted to SQDT according to SQCK. When SQOK is 'L', 'L' is outputted to the SQDT terminal.

4) VCO1, SDAT, SBCK Timing Chart



ⓐ: SBCK is set to "L" for about 10μS after PBFR becomes a falling edge.

ⓑ: When S0S1 is 'L', a subcode P is outputted. When S0S1 is 'H', S0S1 is outputted.

ⓒ: When a cycle of VCO1 is 'T', the width of ⓒ is 4T ~ 6T.

ⓓ: When the pulse inputted into the SBCK terminal is above 7, subcode data P, Q, R, S, T, U, V, W is repeated.

ECC (Error-Correction Code) Block

The function of ECC Block is to recover the damage of data to some extent when the data on the disk was lost by damage. By using CIRC (Crossed-Interleave Reed-Solomon Code), C1 (32, 28) and C2 (28, 24) errors are corrected. ECC is performed with a 8 bit as a symbol unit. In correcting C1, a C1 Pointer is generated, and in correcting C2, a C2 pointer is generated.
C1, C2 Pointers send error information on the data to which ECC is given. After correcting C2, against can't corrected Data, Error Data is sent by outputing C2 Flag.
The signal C2FL is AND signal of C2F1 and C2F2. By using this information, Data is treated in the interpolator block.

C1F1	C1F2	C1, C2 Error	C2F1	C2F2	C2FL
0	0	No Error	0	0	0
0	1	Single Error	0	1	0
1	0	Double Error	1	0	0
1	1	Irretrievable Error	1	1	1

C1F1, C1F2 — Output the state of an error correction by C1 Decoder

C2F1, C2F2 — Output the state of an error correction by C2 Decoder

C2FL — Becomes 'L' when an error correction by C2 Decoder is possible and an 'H' error correction is impossible.

16K SRAM BLOCK

After EFM demodulation of EFM modulated data inputted from disc, when the Data is written into RAM or data is outputted to Read/Write and D/A Converters in ECC Processing, for reading, SRAM Address Generator and a 16K SRAM have installed in there.
SRAM terminal must be 'H' in 16K SRAM application.

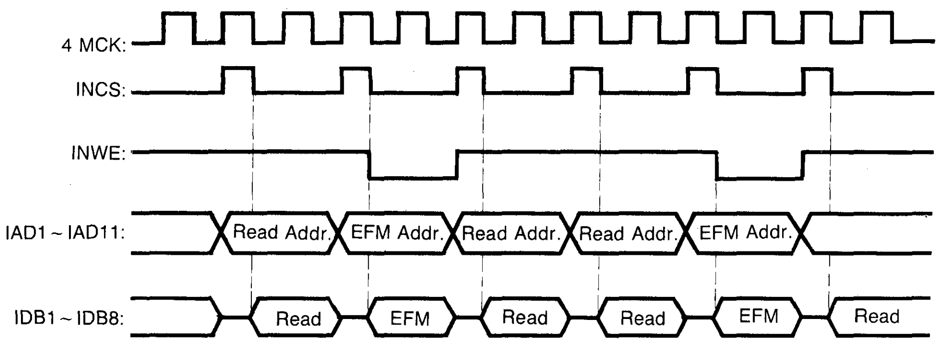
1) Address Generation Priority Control

Writing in EFM demodulation, reading the data with R/W, D/A Converter in ECC process, sometimes these processes are required at the same time.
When 3 signals are demanded at the same time, priority of the data process needs to be controlled. Priority is D/A Converter Read demand > EFM Write demand > ECC R/W demand.

2) EFM Demodulation Data Write Demand

EFM demodulated data mube be written to SRAM, priority is controlled when the write demand signal is transmitted to the SRAM Address Generator, and the Enable signal is transmitted to the EFM Block. The generated address is transmitted to the SRAM Interface circuit.
Generated address is data which deinterleave is considered, and in a frame 32 addresses are generated.

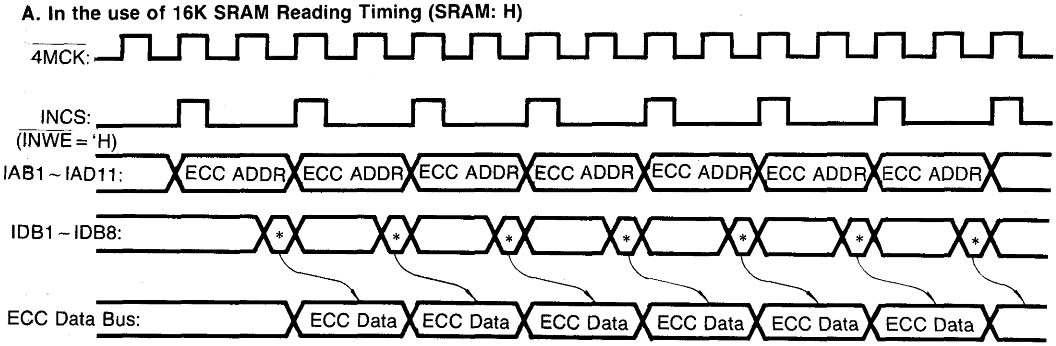
A. In the use of 16K SRAM (in EFM & ECC Write): SRAM terminal 'H'
DB1 ~ DB8 and AD1 ~ AD11 terminals are in a state of Hi-Z. $\overline{CE}$ and $\overline{WE}$ are 'Don't Care.'



3) R/W Demand of ECC Data

For C1 and C2 ECC treatment 129 times of Address demand signals generated due to an R/W operation must be given to 64 PCM data and 65 Pointers during a frame.
The write of FCC processing is the same as 2) EFM Write operation.
In reading it is as follows:

A. In the use of 16K SRAM Reading Timing (SRAM: H)



*: Valid ECC Data

4) D/A Converter Read Demand

Since each 6 sampling data on the left and right channel and 12 C2 Pointer data must be read for a frame, 36 read enable demand signals are caused. The timing chart for D/A Converter Read is the same as the R/W demand block of ECC data. As a result the number of the maximum R/W operation action demanded for a frame is 179 times.

5) Address Generated Block

The interleaving data in encoding is deinterleaved in decoding. The data of 108 frames is needed to get 8 frame of PCM data in a CDP format. To get data suitable for a CDP format 2 counters are needed. A write base counter is used to write EFM demodulation data are hindered in storing data in SRAM due to disk shaking, the instability of a servo system etc.

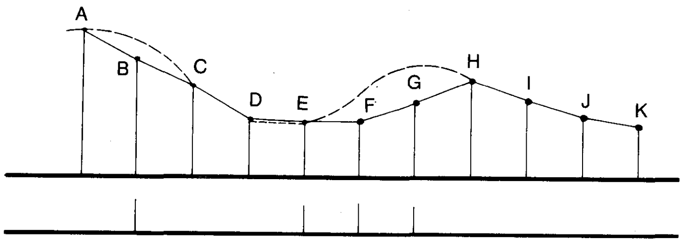
6) Jitter Margin

EFM demodulation data are hindered in storing data in SRAM due to disk shaking, the instability of a servo system etc. Now that the data that must be kept is limited by the size of SRAM in view of time, data is destroyed if the value of read/write base counter has a difference above ± 5 frames. Being loading into the value of write base counter with enforcement, the value of read base counter has a jitter margin below ± 4 frames when there is a difference over ± 5 frames in the read/write base counter value.

A read base counter value is baded into a write base counter with enforcement when data on the left and right channels are all muting, or when NCLV is 'H', and CLV-Servo is stop, forward and reverse. When the difference between read/write base counter is above ± 4 frame, a 'H' signal is outputted to the $\overline{JIT}$ terminal for a period.

INTERLEAVE, MUTE BLOCK

When a burst error occurs on a disk, sometimes the data can't be corrected even if a ECC process is conducted. An interpolator block revises data by using C2 Pointer outputted through the ECC Block. PCM data inputted into a data bus are inputted to the left and right channels respectively in order of 8 bit C2 Pointer, Lower 8 bit and Upper 8 bit. A pre-hold method is taken when a DA Flag is 'H' continuously. In case of the occurrence of a single error, a mean value interpoalting method is carried out with the range of PCM Data before and after an error happens. When a check against a checked cycle is 'L', R-CH Data is outputted. L-CH Data is outputted when the check is 'H'. As to the timing chart of a interpolator block see figure 6.



$B = \frac{A+C}{2}$: Mean value interpolation

F = E = D : Pre-hold interpolation

G = F + H : Mean value interpolation

2) Mute and Attenuation

By a Mute terminal and a ATTM signal by the CNTL-S Reg., AUDIO data is muted or reduced. There are two kinds of mute: zero cross muting, muting.

A. Zero Cross Muting
Audio data is muted when a mute terminal is 'H' and when 6 bits in a high position of Audio Data is all 'H' or 'L'.

B. Muting
Audio data is muting when ZCMT of the CNTL-Z Reg. is 'L' and when a mute terminal is 'H'.

C. Attenuation
By means of the ATTM signal of the CNTL-S Reg. and the signal of Mute terminal, a audio signal attenuation occurs as the following.

ATTM	MUTE	Degree of Attenuation
0	0	0 dB
0	1	– dB
1	0	– 12 dB
1	1	– 12 dB

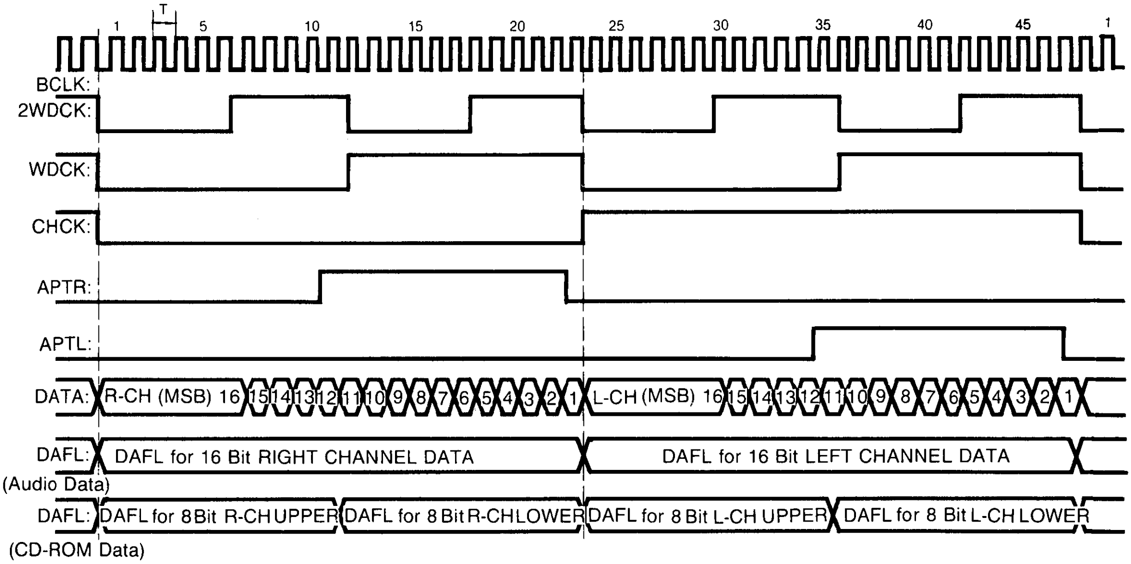


Fig. 6. When Sel. 5 is 'L', and DF is off, the Timing Chart of PCM Data

CLV SERVO

CNTL-C Reg. is selected to control CLV Servo by the Data inputted from μ-COM. In CNTL-C Reg, the data from μ-com appoint CLV servo action mode and control spindle motor.

1) Forward

The states of output terminal related to the mode to rotate a spindle motor forward are SMDP = 'H', SMSD = Hi-Z, SMEF = 'L' and SMON = 'H' respectively.

2) Reverse

The modes to rotate a spindle motor reversly are SMDP = 'L', SMSD = 'Hi-Z', SMEF = 'L', and SMOD = 'H'.

3) SPEED-Mode

The SPEED-Mode is the mode for the rough control of a spindle motor when a track jumping or a EFM phase is unlocked. If a cycle of VCO is 'T', the pulse width of a frame sync is '22T'. Sometimes EFM signal is above 22T due to noises on a disc, etc. A correct frame sync cannot be detected when the signal is not removed. In this case, the pulse width of EFM signal is detected at a cycle of XTFR/2 or XTFR/4 which are peak hold clocks. The pulse width of EFM signal is detected at a cycle of XTFR/16 or XTFR/32 which are bottom hold clock. The value detected is used for a frame synchronization signal. When the frame synchronization signal is smaller than 21T, the SMPD terminal outputs 'L'. When it is 22T, Hi-Z is outputted. 'H' is outputted when it is above 23T.
When the GAIN signal of CNTL-W Reg. is 'L', the SMDP terminal is outputted after being attenuated at − 12dB when the signal is 'H', the terminal is outputted without any attenuation. <cf. figure 7>
In SMSD, SMEF, and SMON terminals Hi-Z, 'L', and 'H' are outputted.

4) HSPEED-Mode

The rough servo mode which moves 20,000 tracks in high speed acts between inside of CD and outside of CD. In the domain of a mirror of the track without a pit EFM and the signal of 20KHz overlap. In the case, since in the speed-mode the peak range of a longer mirror signal than the original frame sync is detected, the servo operation become unstable. In HSPEED-mode a peak hold uses a 8.4672/256 MHz signal, and a bottom hold removes a mirror component and stabilizes the high speed servo operation by using XTFR/16 or XFFR/32 period signal.
In SMSD, SMEF, and SMON terminals, Hi-Z, 'L', and 'H' are outputted.

5) PHASE-Mode

A PHASE Mode is the mode to control an EFM Phase. When NCLV of CNTL-Z is 'L', it detects a phase difference between PBFR/4 and XTFR/4, and when NCLV is 'H', it detects the phase difference between. Read base Counter/4, write base Counter/4, and then output to SMPD terminal. See figure 8.
If the VCO/2 signal cycle is put as 'T' and the PBFR during a 'H' period as a W_{pb}, it outputs 'H' to a SMSD terminal from the falling edge of PBFR for (W_{pb}-278T) x 32, and later outputs 'L' to the falling edge of PBFR. Refer to figure 9.

6) XPHSP-Mode

A XPHSP mode is the mode used in normal operation. It samples a LKFS signal made in the frame sync block at a cycle of PBFR/16. After sampling 'H', DHASE mode is carried out. When 'L' is sampled continuously 8 times, it goes over to speed-mode. CNTL-W Reg. decides the choice of the peak hold of speed-mode, the bottom hold cycle of SPEED and HSPEED-Mode and the choice of a gain.

7) VPHSP-Mode

A VPHSP-Mode is the mode used for rough servo control. It uses VCO instead of X'tal in the EFM pattern test. When the range of VCO center changes, VCO is easily loaded because the rotation of a spindle motor changes in the same direction.

8) STOP

Stop is the mode to stop a spindle motor.
SMDP = 'L', SMSD = Hi-Z, SMEF = 'L', SMON = 'L'

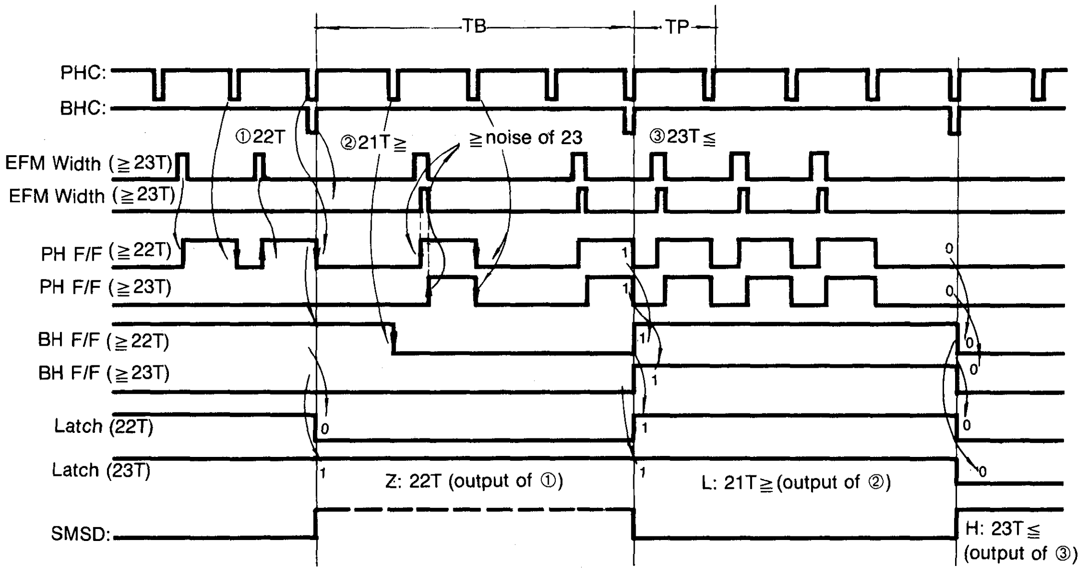


Fig. 7 When gain is 'H' in a speed-mode Timing Charg of SMSD output

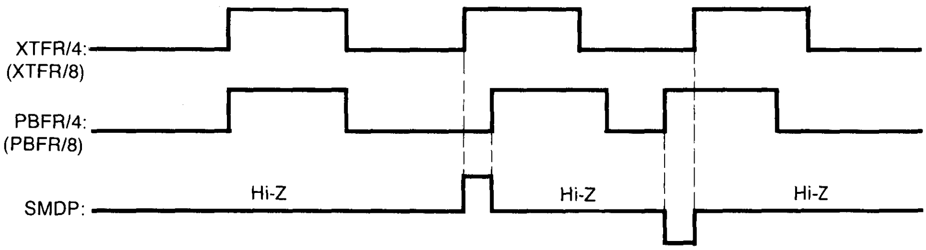
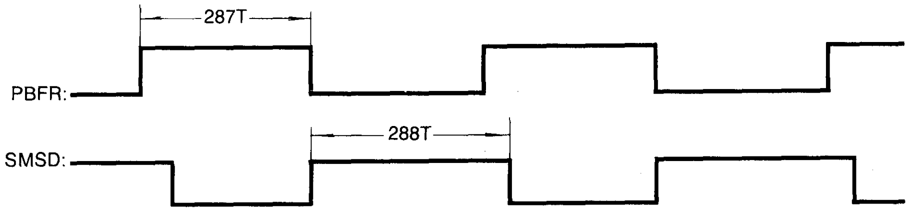
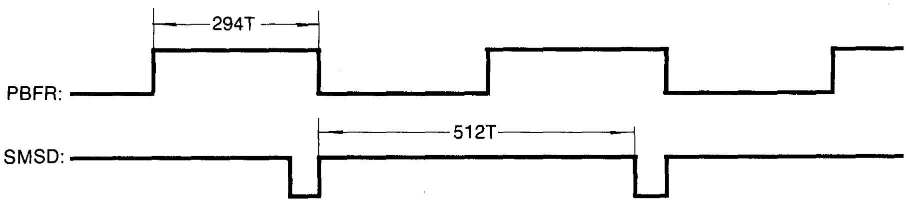


Fig. 8 Output Timing Chart of a SMDP terminal



(a) When PBFR is 287T, Timing Chart of SMSD output



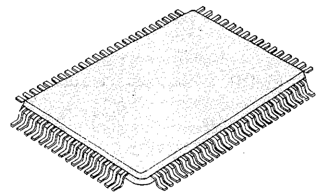
(b) When PBFR is 294T, Timing Chart of SMSD output

Fig. 9 In a PHASE Mode Timing Chart of SMSD output (T: VCO/2)

DIGITAL SIGNAL PROCESSOR

The KS5991 is a monolithic integrated circuit designed for compact disc player application. It is consisting of 16KSRAM, digital filter and digital signal processing circuits, and it is suitable for headphone stereo CDP.

80 FQP



FEATURES

- **All digital signals for regeneration are processed using one chip.**
- **Internal aperture compensation digital filter**
- **EFM-PLL circuit for bit clock regeneration**
- **EFM data demodulation**
- **Frame synchronous signal detection, protection**
- **Compensation using mean value, prior value retention**
- **Subcode signal demodulation subcode Q detection**
- **CLV servo for spindle motor**
- **8-bit tracking counter**
- **CPU interface with serial bus**
- **Subcode Q reaister**
- **Built-in 17th digital filter**
- **Built-in 16KSRAM**
- **80 Quad flat package type**
- **Operating supply voltage: V_{CC} = 3.4V ~ 5.5V**

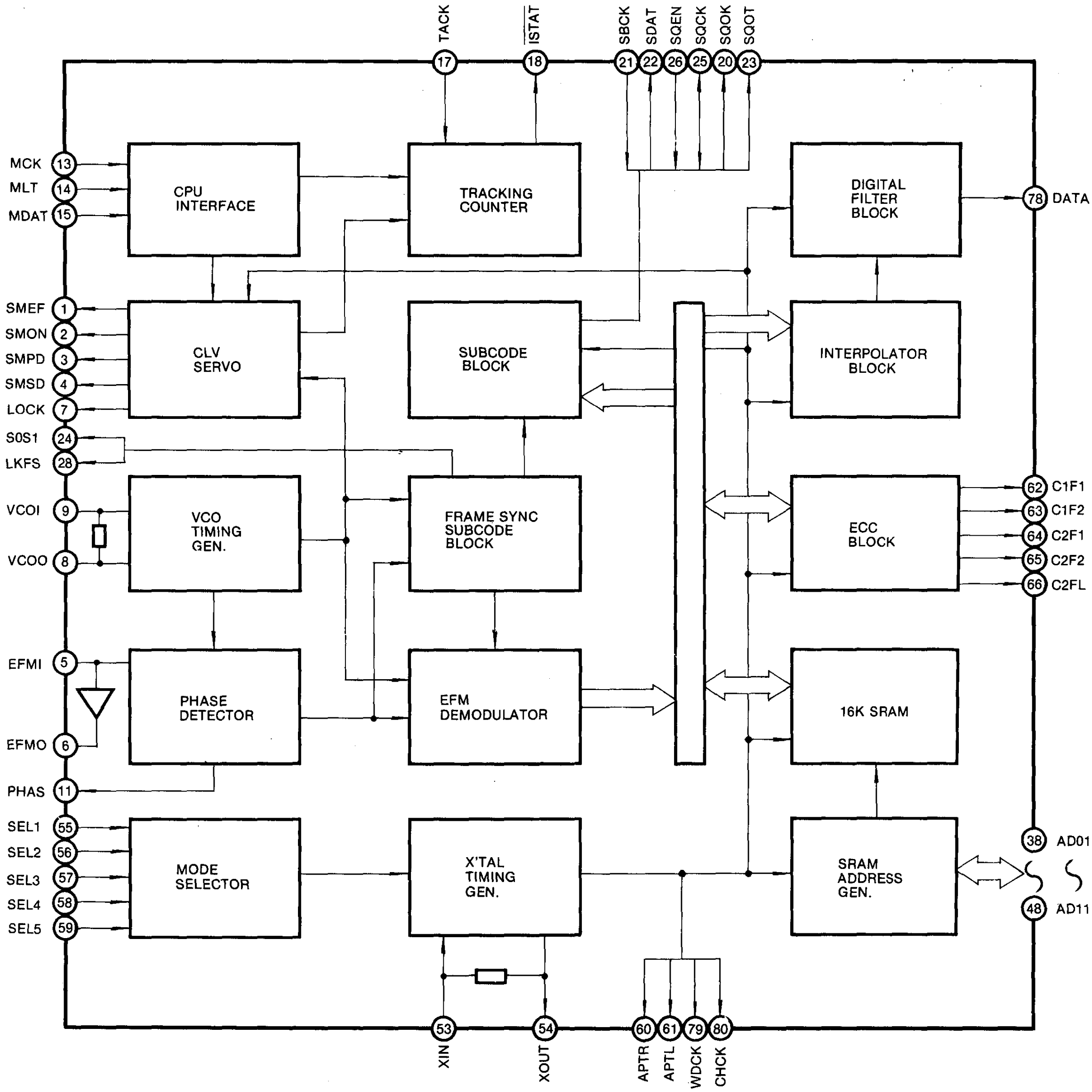
ORDERING INFORMATION

Device	Package	Operating Temperature
KS5991	80 FQP	−20 ~ +70°C

ABSOLUTE MAXIMUM RATING (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 ~ +7	V
Input Voltage	V_1	−0.3 ~ +7	V
Output Voltage	V_0	−0.3 ~ +7	V
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

1. DC Characteristics

($V_{DD}=5V \pm 10\%$, $V_{SS}=0V$, Ta = 25°C, unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Input High Level Voltage	V_{IH1}	Note 1	0.7 V_{DD}		V_{DD}	V
Input Low Level Voltage	V_{IL1}	Note 1	0		0.3 V_{DD}	V
Input High Level Voltage	V_{IH2}	Note 2	0.8 V_{DD}			V
Input Low Level Voltage	V_{IL2}	Note 2			0.2 V_{DD}	V
Output High Level Voltage	V_{OH}	$I_{OH}=-1mA$	$V_{DD}-0.5$		V_{DD}	V
Output Low Level Voltage	V_{OL}	$I_{OL}=1mA$	0		0.4	V
Input Leak Current	I_{LC}	$V_{IN}=0\sim5.5V$	−5		+5	μA
Three-State Pin Output Leak Current	I_{LD}	$V_{OUT}=0\sim5.5V$	−5		+5	μA
SRAM Input Leak Current	I_{SLC}	$V_{IN}=0\sim5.5V$	−5		+200	μA

($V_{DD}=3.4V$, $V_{SS}=0V$, Ta = 25°C)

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input High Level Voltage	V_{IH3}	Note 1	0.7 V_{DD}		V_{DD}	V
Input Low Level Voltage	V_{IL3}	Note 1	0		0.3 V_{DD}	V
Input High Level Voltage	V_{IH4}	Note 2	0.8 V_{DD}			V
Input Low Level Voltage	V_{IL4}	Note 2			0.2 V_{DD}	V
Output High Level Voltage	V_{OH}	$I_{OH}=-0.5mA$	$V_{DD}-0.5$		V_{DD}	V
Output Low Level Voltage	V_{OL}	$I_{OL}=0.5mA$	0		0.3	V
Input Leak Current	I_{LC}	$V_{IN}=0\sim5.5V$	−5		+5	μA
Three-State Pin Output Leak Current	I_{LO}	$V_{OUT}=0\sim5.5V$	−5		+5	μA
SRAM Input Leak Current	I_{SLC}	$V_{IN}=0\sim5.5V$	−5		+200	μA

Note 1. Related pins—EFMI, XRST, TEST, MUTE, SEL1~5, MLT, MDAT, SBCK, SQEN, SQCK
Note 2. Related pins—CNIN, MCK.

2. AC Characteristics

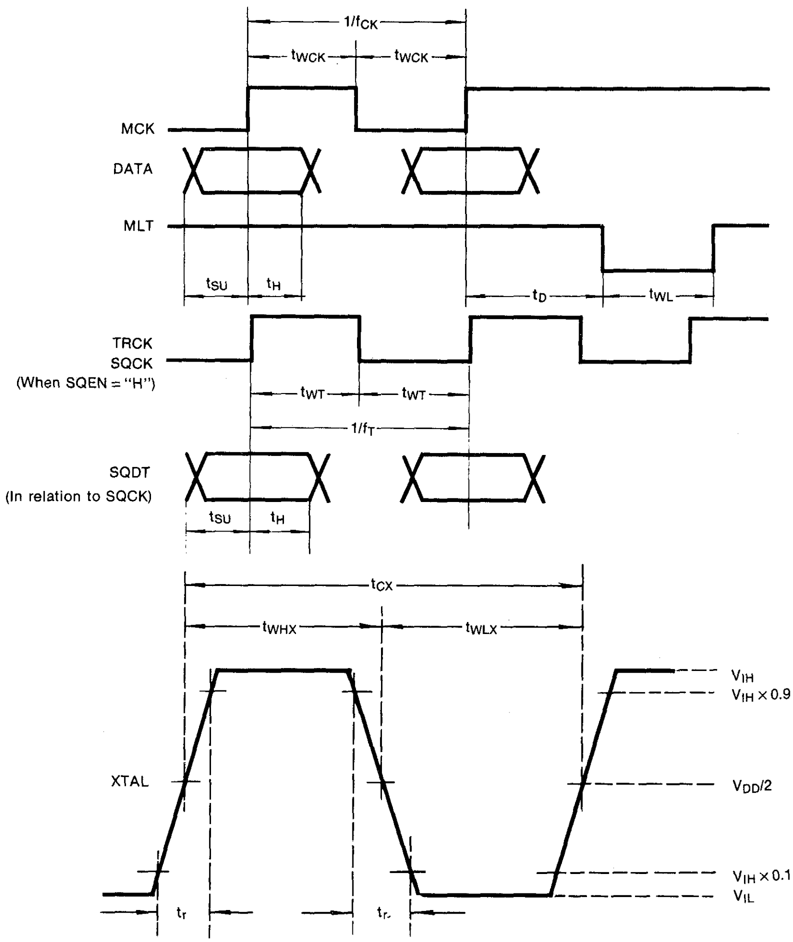
A. XIN Pin, VCOI Pin

(1) When pulse applied to XIN and VCO ($V_{DD}=5V \pm 10\%$, $V_{SS}=0V$, Ta = 25°C, unless otherwise specified)

Item	Symbol	Min	Typ	Max	Unit
"H" Level Pulse Width	t_{WHX}	20			ns
"L" Level Pulse Width	t_{WLX}	20			ns
Pulse Frequency	t_{CX}	55			ns
Input "H" Level	V_{IH}	$V_{DD}-1.0$			V
Input "L" Level	V_{IL}			0.8	V
Rising Time Breaking Time	t_R, t_F			15	ns

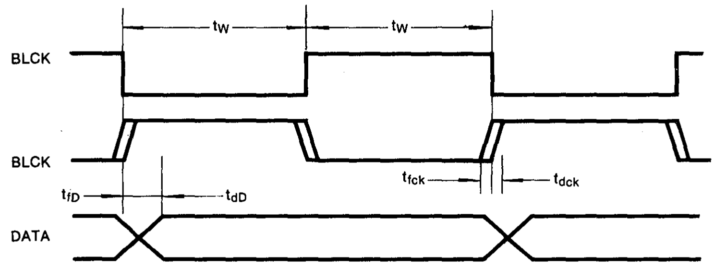
B. Pins MCK, DATA, MLT, TRCK, SQCK
($V_{DD}=5.0V \pm 10\%$, $V_{SS}=0V$, $T_{opr}=0$ to $+75°C$)

Item	Symbol	Min	Typ	Max	Unit
Clock Frequency	f_{CK}			1	MHz
Clock Pulse Width	t_{WCK}	300			ns
Setup Time	t_{SU}	300			ns
Hold Time	t_H	300			ns
Delay Time	t_D	300			ns
Latch Pulse Width	t_{WL}	300			ns
CNIN SQCK Frequency	f_T			1	MHz
CNIN SQCK Pulse Width	t_{WT}	300			ns



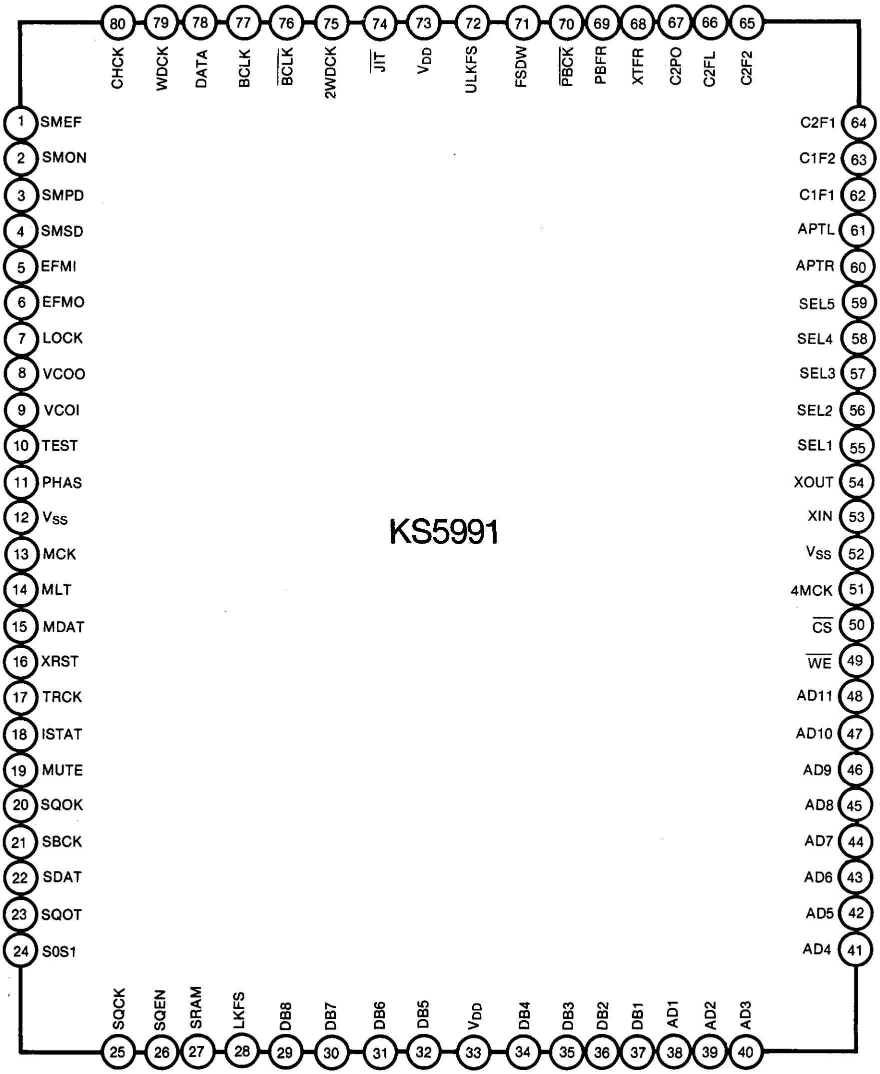
C. DAC Interface ($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, $T_{opr}=0$ to $+75°C$, $C_L=50pF$)

Item	Symbol	DF is OFF			When DF ON			Unit
		Min	Typ	Max	Min	Typ	Max	
Clock Pulse Width	t_W		236			118		ns
Clock Skew (Fast)	t_{fck}			40			40	ns
Clock Skew (Delay)	t_{dck}			40			40	ns
Data Skew (Fast)	t_{fD}			0			0	ns
Data Skew (Delay)	t_{dD}			80			80	ns



*Note: CHCK, WDCK, APTR, APTL
DA01 through DA16 during parallel DA conversion or C1F1, C1F2, C2F1, C2F2, C2FL, C2PO, XTFR, 2WDCK, DATA during serial conversion.

PIN CONFIGURATION



PIN DESCRIPTION

No.	Symbol	I/O	Description
1	SMEF	O	Pin 1 output is switched constant when output filter of the spindle motor is energized.
2	SMON	O	ON/OFF control for spindle motor.
3	SMPD	O	Spindle motor drive. Provides rough control during CLV-S mode and phasse control during CLV-P mode.
4	SMSD	O	Spindle motor drive. Controls speed during CLV-P mode.
5	EFMZ	I	EFM signal from RF amplifier.
6	EFMO	O	Controls slice level of the EFM signal.
7	LOCK	O	The output of pin 7 reflects the status of the GFS signal which is sampled at PBFR/16. When the GFS signals is "H", but, when the signal has remained "L" for at least 8 samples, the output of pin 7 is "L".
8	VCOO	O	VCO output. The frequency is f = 8.6436MHz, when locked by the DBFR signal.
9	VCOI	I	VCO input.
10	TEST	I	(0V).
11	PHAS	O	The output of Pin 11 provides phase comparison of EFM signal and VCO/2.
12	V_{SS}	—	GND (0V).
13	MCK	I	Pin 13 provides serial transmission clock from the CPU. Data is latched on the leading edge of the clock.
14	MLT	I	Pin 14 provides latch input from the CPU. 8-bit shift register data (serial data received from the CPU) is latched in each of the registers.
15	MDAT	I	Serial data from the CPU.
16	XRST	I	System reset ("L").
17	TRCK	I	Tracking pulse input.
18	$\overline{\text{ISTAT}}$	O	Output reflecting internal condition as designated by address.
19	MUTE	I	Muting input. MUTE is "L" when ATTM of internal register A is "L" (normal condition). MUTE is "H" when meting condition is set.
20	SQOK	O	Output the results CRC check of subcode Q.
21	SBCK	I	Clock input for subcode serial output.
22	SDAT	O	Serial output of subcode.
23	SQDT	O	Output of subcode Q.
24	S0S1	O	Output of subcode sync S0 + S1.
25	SQCK	I/O	Clock for reading subcode Q.
26	SQEN	I	Input for selecting SQCK (L; SQCK is output, H; SQCK is input)
27	SRAM	I	SRAM is "H" in Nomal, SRAM is "L" when system is testing.
28	LKFS	O	Display output for frame sync lock status.

PIN DESCRIPTION (Continued)

No.	Symbol	I/O	Description
29	DB8	I/O	Data pin for external RAM. DATA8 (MSB) in test mode. Hi-Z in nomal
30	DB7	I/O	Data pin for external RAM. DATA7 in test mode. Hi-Z in nomal
31	DB6	I/O	Data pin for external RAM. DATA6 in test mode. Hi-Z in nomal
32	DB5	I/O	Data pin for external RAM. DATA5 in test mode. Hi-Z in nomal
33	V_{DD}	—	Power supply (+5V).
34	DB4	I/O	Data pin for external RAM. DATA4 in test mode. Hi-Z in nomal
35	DB3	I/O	Data pin for external RAM. DATA3 in test mode. Hi-Z in nomal
36	DB2	I/O	Data pin for external RAM. DATA2 in test mode. Hi-Z in nomal
37	DB1	I/O	Data pin for external RAM. DATA1 (LSB) in test mode. Hi-Z in nomal
38	AD01	I/O	(LSB)
39	AD02	I/O	In nomal mode (TEST = 'L', SRAM = 'H'), these pins are High impedance (Hi-Z) In test mode (TEST = 'H', SRAM = 'L'), these pins are Output address of external RAM
40	AD03	I/O	
41	AD04	I/O	
42	AD05	I/O	
43	AD06	I/O	
44	AD07	I/O	
45	AD08	I/O	
46	AD09	I/O	
47	AD10	I/O	
48	AD11	I/O	(MSB)
49	$\overline{WE}$	I/O	In nomal mode, this is WE output. In test mode, write enable input.
50	$\overline{CE}$	I/O	In nomal mode, this is CE output. In test mode, chip enable input.
51	4MCK	O	Divider output for crystal. f = 4.2336MHz
52	V_{SS}	—	GND (0V)
53	XIN	I	Input to crystal oscillator circuit. Depending on the mode the frequency is either f = 8.4672 r 16.9344MHz.
54	XOUT	O	Output from crystal oscillator circuit. Depending on the mode the frequency is either f = 8.4672 or 16.9344MHz.
55	SEL1	I	Mode selection input 1.
56	SEL2	I	Mode selection input 2.
57	SEL3	I	Mode selection input 3.
58	SEL4	I	Mode selection input 4. Code switch input for audio data output. 2's complement output when "L", offset binary output when "H".
59	SEL5	I	Mode selection input 5. Code switch input for audio data output. Serial output when "L", parallel output when "H".

PIN DESCRIPTION (Continued)

No.	Symbol	I/O	Description
60	APTR	O	Output for aperture compensation. "H" when R-ch.
61	APTL	O	Output for aperture compensation. "H" when L-ch.
62	C1F1	O	Monitor output reporting status of error correction for C1 decoder. When SEL5 = 'L', DA01 (LSB of parallel audio data) is output when SEL5 = 'H'.
63	C1F2	O	Monitor output reporting status of error correction for C1 decoder when SEL5 = 'L', DA02 is output when SEL5 = 'H'.
64	C2F1	O	Monitor output reporting status of error correction for C2 decoder when SEL5 = 'L', DA03 is output when SEL5 = 'H'.
65	C2F2	O	Monitor output reporting status of error correction for C2 decoder when SEL5 = 'L', DA04 is output when SEL5 = 'H'.
66	C2FL	O	When SEL5 = 'L', output of status condition. C2FL is set 'H' when the C2 sequence. Presently being corrected becomes impossible to correct. DA05 is output when SEL5 = 'H'.
67	C2PO	O	Display output of the C2 pointer when SEL5 = 'L', DA06 is output when SEL5 = 'H'.
68	XTFR	O	When SEL5 = 'L', output of read frame dock which is 7.35KHz of the crystal system. DA07 is output when SEL5 = 'H'.
69	PBFR	O	When SEL5 = 'L', output of write frame clock which is 7.35KHz when locked by the crystal system. DA08 is output when SEL5 = 'H'.
70	$\overline{\text{PBCK}}$	O	When SEL5 = 'L', output of VCO/2 (f = 4.3218MHz when locked by the EFM signal). DA09 is output when SEL5 = 'H'.
71	FSDW	O	When SEL5 = 'L', output for unprotected frame sync patterns. DA10 is output when SEL5 = 'H'.
72	ULKFS	O	Output for display of status of frame sync protection when SEL5 = 'L', DA11 is ouput when SEL5 = 'H'.
73	V_{DD}	—	Power supply (+5V).
74	$\overline{\text{JIT}}$	O	When SEL5 = 'L', output for display of either RAM overflow or underflow for +4 frame jitter absorption. DA12 is output when SEL5 = 'H'.
75	ZWDCK	O	When SEL5 = 'L', output for strobe signal (352.8KHz when DF is ON, 176.4KHz when DF is OFF). DA13 is output when SEL5 = 'H'.
76	$\overline{\text{BLCK}}$	O	When SEL5 = 'L', inverse output of BLCK. DA14 is output when SEL5 = 'H'.
77	BLCK	O	When SEL5 = 'L', bit clock output (4.2336MHz when DF is ON, 2.1168MHz when DF is OFF) DA15 is output when SEL5 = 'H'.
78	DATA	O	Serial data output of audio signal when SEL5 = 'L'. DA16 is output when SEL5 = 'H'.
79	WDCK	O	Strobe signal output. Output is 176.4KHz when DF is on. Output is 88.2KHz when DF is off.
80	CHCK	O	Strobe signal output. Output is 88.2KHz when DF is on. Output is 44.1KHz when DF is off.

DESCRIPTION OF FUNCTION

MODE SELECTOR

To control several blocks in KS5991, there are 5 selecting pin signals. Table 1. Shows selected mode by these signals.

Input Pins					Function*				
SEL1	SEL2	SEL3	SEL4	SEL5	XIN	DF	P/S	OB/2'S	CD ROM/Audio
0	1	0	0	0	16M	ON	S	2'S	Audio
0	1	0	1	1	16M	ON	P	OB	Audio
0	1	1	0	0	16M	OFF	S	2'S	Audio
0	1	1	1	1	16M	OFF	P	OB	Audio
1	0	0	0	0	8M	ON	S	2'S	Audio
1	0	0	1	1	8M	ON	P	OB	Audio
1	0	1	0	0	8M	OFF	S	2'S	Audio
1	0	1	1	1	8M	OFF	P	OB	Audio
1	1	1	1	0	8M	OFF	S	2'S	CD ROM

Table 1. Mode Selection

* Note:
- 8M/16M: Selection of either the XIN or XOUT clocks will provide either a 8.4672MHz or 16.9344MHz signal.
- DF: Digital Filter
- P/S: Parallel mode/serial mode
- OB/2'S: Offset

- Clock selection
  Selectioin of an 16.9344MHz or 8.4672MHz oscillator clock is possible at pins XIN and XOUT. However only 16.9344MHz clocks are provided for digital out usage.
- Digital filter selection
  When the digital filter function is switched to ON, all signals on the DAC interface are handled at twice the normal speed.
- Parallel/Serial output selection
  When the output is parallel, 16-bit parallel data is output from pins DA01 through DA16.
  When the output is serial, the following signals are output at pin DA01 through DA16.

DATA (DA16)	Serial data output (MSB or LSB first output)
BLCK (DA15)	Internal system clock (with DF ON 4.2336MHz and with DF OFF 2.1168MHz)
$\overline{BLCK}$ (DA14)	Bit clock (BLCK inversion signal)
2WDCK (DA13)	4X multiplied CHLK signal
$\overline{JIT}$ (DA12)	Jitter Margin Overflow/Underflow signal
ULKFS (DA11)	Display output of frame sync protection status
FSDW (DA10)	Unguarded (unprotected) frame sync signal
PBCK (DA09)	Signal at 1/2 V_{CO} pin cycle times. When locked 4.3218MHz
PBFR (DA08)	Write Frame Clock signal. When locked 7.35KHz.
XTFR (DA07)	Read Frame Clock signal. Crystal system 7.35KHz.
C2PO (DA06)	C2 Pointer signal
C2FL (DA05)	Correction mode output, C2FL = C2F1, C2F2
C2F2 (DA04) C2F1 (DA03)	Monitor Output of Error Correction Mode for C2 Decode
C1F2 (DA02) C1F1 (DA01)	Monitor Output of Error Correction Mode for C1 Decode

- OFFSET Binary/2's Complement Selection
  When pin SEL4 is at "H" output occurs at OFFSET BINARY; when it is at "L" output occurs at 2's complement.
- CDROM/AUDIO Selection
  When SEL1 = SEL2 = SEL3 = "H", CDROM is selected. Then the C2 pointer is output with each byte (8 bits) and neither the mean value interpolation nor the preceding value hold are exercised. That is, if an error occurs in the upper 8 bits of a 16-bit data, only the C2 pointer related to those upper 8 bits switches to "H" while the lower 8 bits are handled as correct data.

Microcomputer Interface

Data from microcomputer are inputed through MDAT pin by MCK which is clock signal of microcomputer and pulse signal through MLT pin is for inputed data load one of 6 kinds of control registers.

Fig. 1 Shows the timing diagram of data input from microcomputer

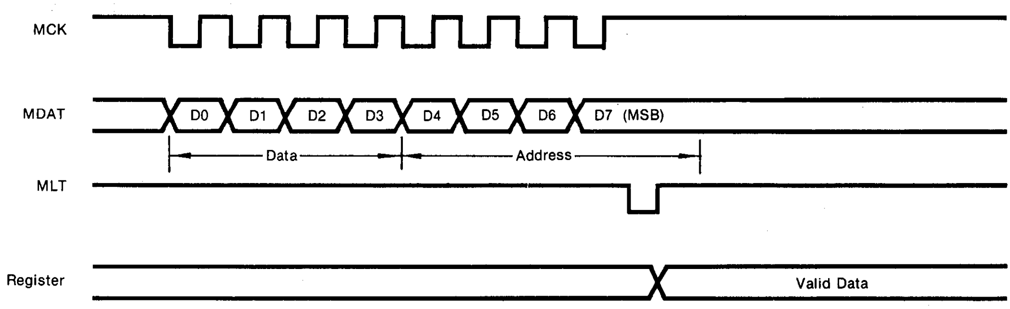


Fig. 1 Data Input Timing Diagram

According to the address of MDAT, control register is selected as below table 1.

Control Register	Comment	Address D7 ~ D4	Data				$\overline{\text{ISTAT}}$ Pin
			D3	D2	D1	D0	
CNTL-Z	Data Control	1 0 0 1	ZCMT	HIPD	NCLV	CRCD	Hi-Z
CNTL-S	Frame Sync Protection Attenuation Control	1 0 1 0	FSEM	FSEL	WSEL	ATTM	Hi-Z
CNTL-L	Tracking Counter Lower 4 Bit	1 0 1 1	TRC3	TRC2	TRC1	TRC0	$\overline{\text{Complete}}$
CNTL-U	Tracking Counter Upper 4 Bit	1 1 0 0	TRC7	TRC6	TRC5	TRC4	$\overline{\text{COUNT}}$
CNTL-W	CLV Control	1 1 0 1	COM	WB	WP	GAIN	Hi-Z
CNTL-C	CLV Mode	1 1 1 0	CLV Mode				$\overline{PW \geq 64}$

Table 1. Data of Selected Control Register

According to D0 through D7.
The function of each control registers is descriped below

1) CNTL-Z Register

This is a control register for the zero cross mute of audio data, PHAS, the control signal of phase servo and CRCF data.

		Data = 0	Data = 1
ZCMT	D3	Zero cross mute "OFF"	Zero cross mute "ON"
HIPD	D2	Phase normally active	Phase convert "L" to "Hi-Z" by LKFS
NCLV	D1	Phase servo driven by frame sync	Phase servo be controlled by base counter
CRCQ	D0	SQDT output without SQOK	SQDT = CRCF during the rising time of S0S1

2) CNTL-S Control Register

This is a control register for frame sync. Protection and attenuation.

FSEM	FSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	Clock
0	±3
1	±7

ATTM	MUTE	dB
0	0	0
0	1	–
1	0	–12
1	1	–12

3) CNTL-L, U Control Register

When the numbers of tract will be counted is inputed from microcomputer, data loaded these registers. (See tracking counter)

4) CNTL-W Control Register

This is a control register for CLV-Servo

		Data = 0	Data = 1	Comments
COM	D3	XTFR/4 & PBFR/4	XTFR/4 & PBFR/4	Phase comparative frequency during PHASE-mode
WB	D2	XTFR/32	XTFR/16	Bottom hold period during SPEED and HSPEED-mode
WP	D1	XTFR/4	XTFR/2	Peak hold period during SPEED-mode
GAIN	D0	−12dB	0dB	SMPD gain during SPEED & HSPEED-mode

5) CNTL-C Control Register

This is a control register for CLV-Servo

Mode	D7 ~ D4	D3 ~ D0	SMDP	SMSD	SMEF	SMON
Forward	1 1 1 0	1 0 0 0	H	Hi-Z	L	H
Reverse		1 0 1 0	L	Hi-Z	L	H
SPEED		1 1 1 0	SPEED mode	Hi-Z	L	H
HSPEED		1 1 0 0	HSPEED mode	Hi-Z	L	H
PHASE		1 1 1 1	PHASE mode	PHASE mode	Hi-Z	H
XPHSP		0 1 1 0	SPEED, PHASE mode	Hi-Z or PHASE mode	L or Hi-Z	H
VPHSP		0 1 0 1	SPEED PHASE mode	Hi-Z or PHASE mode	L or Hi-Z	H
STOP		0 0 0 0	L	Hi-Z	L	L

TRACKING COUNTER

This counter is used to improve track-jumping characteristics. The number of tracks that are to be jumped are loaded into either register CNTL-L or CNTL-U. After either register CNTL-L or CNTL-U have been loaded and at the rising edge of the next MLT, TRCK pulse count begins. n (if register CNTL-L = register = CNTL-U = 0, then n = 256) is loaded into the register, and when the address is set in CNTL-L, the signal ($\overline{\text{COMPLETE}}$) is output from pin SENS at high level until the "n"th pulse and then at low level for succeeding pulses. When the address is set in CNTL-U, the signal ($\overline{\text{COUNT}}$) TRCK/2n is output. Fig. 2 shows the timing of the tracking counter.

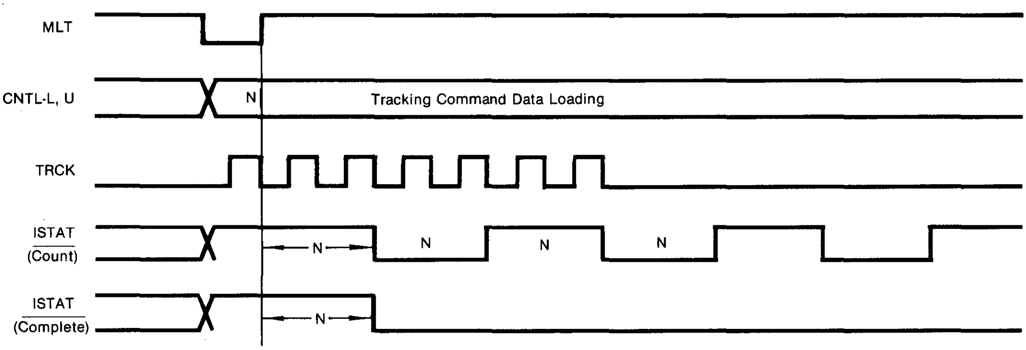


Fig. 2 Tracking Count Timing Chart

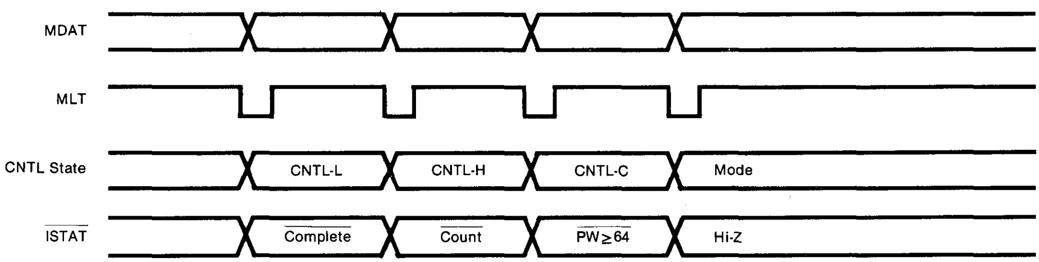
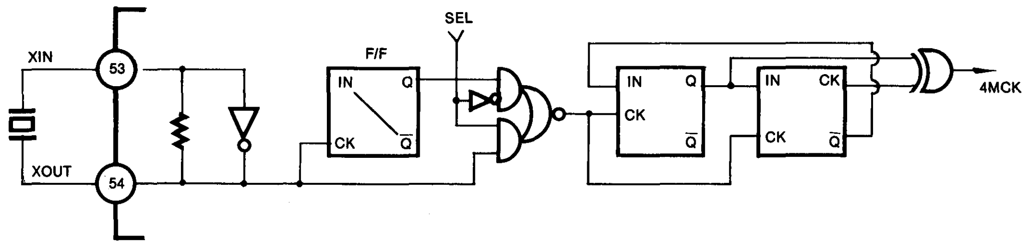


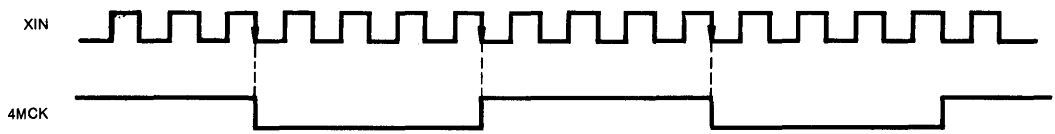
Fig. 3 $\overline{\text{ISTAT}}$ Output Signal by CNTL Register

X'TAL OSCILLATION

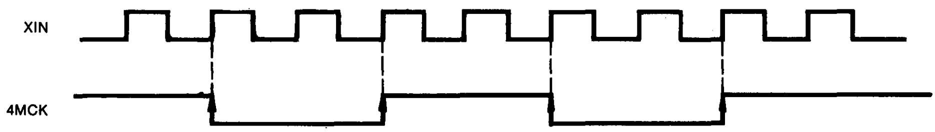
1) Block Diagram



2) Timing Chart (SEL = 0) in Use f = 16.9344MHz X'tal OSC.



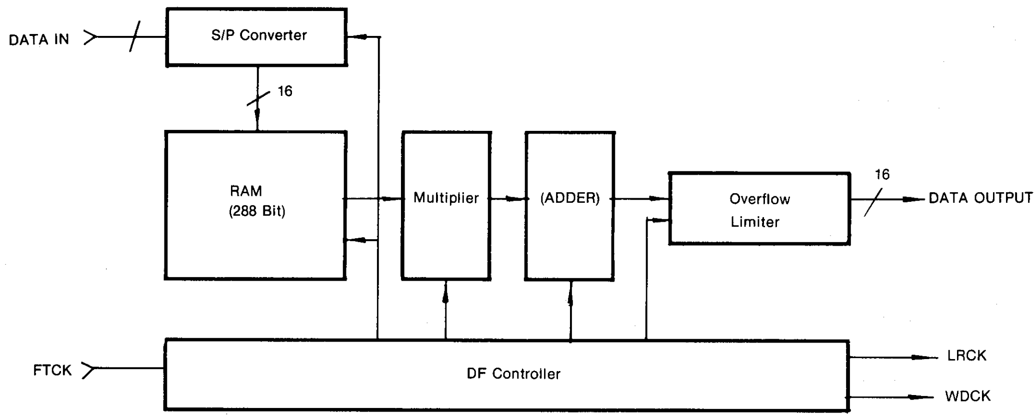
3) Timing Chart (SEL = 1) in use f = 8.4672MHz X'tal OSC.



DIGITAL FILTER

KS5990 is built-in 17th FIR Digital Filter.
The digital filter consists of RAM, multiplier, serial to parallel and parallel to serial converter and controller.

1) Block Diagram



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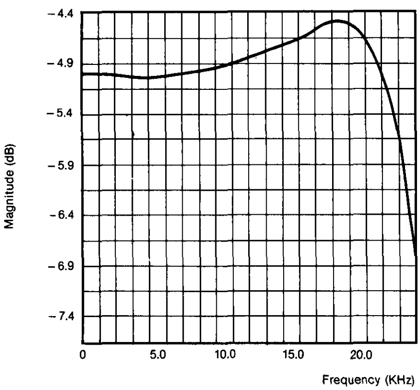
2) Specification

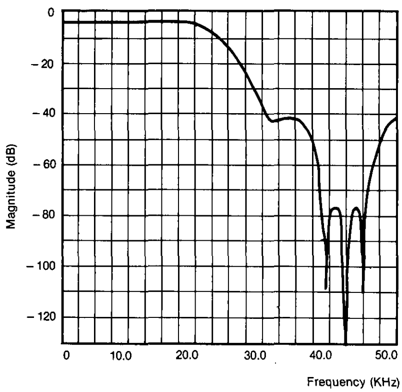
	DC through 18KHz ripple 20KHz of attenuation against 1KHz	±0.07dB max 0.65dB max
	44.1±1KHz attenuation against 1KHz 44.1±5KHz attenuation against 1KHz 44.1±10KHz attenuation against 1KHz 44.1±20KHz attenuation against 1KHz −30dB frequency range against 1KHz −60dB frequency range against 1KHz	87dB min 58dB min 44dB min 10dB min 44.1±14KHz 44.1±4KHz

3) Frequency Characteristic

A. Ripple Characteristic Graph



B. Low Pass Filter Frequency Characteristic Graph



EFM BLOCK

The EFM Block is made up of an EFM Demodulator which demodulates the EFM data inputted from a recorded disc, EFM Phase Detector, Frame Sync Detector/Protector/Inserter, Subcode Sync Detector, and Controller for the EFM Block.

1) EFM Phase Detector

AS the EFM signal inputted from the disc contains 2.16 MHz component, a 4.32 MHz bit clock is generated to detect the phase of the signal. The PBCK outputs the result to the PHAS terminal after detecting the phase on the edge of the EFM signal. The relationship between the EFM signal and the PBCK is explained in the following Timing Chart.

A. In normal operation

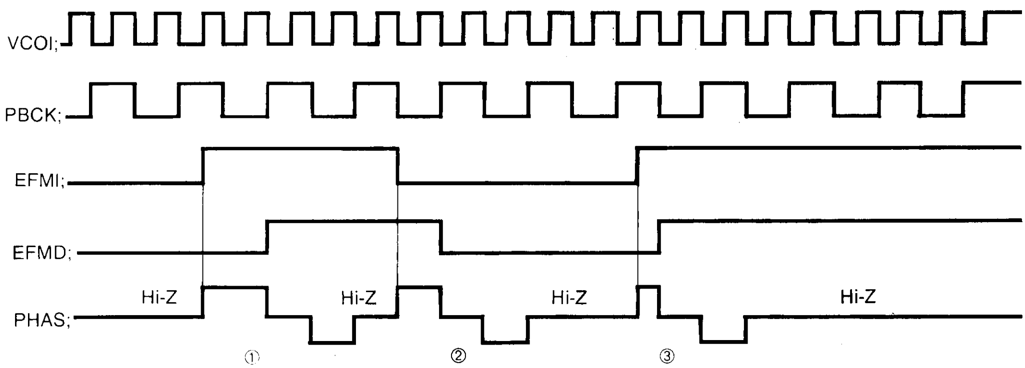


Fig. 5 EFM Phase Detection Timing Chart

Case ①: When the EFM signal is slower than the VCO
Case ②: When the EFM signal is locked up the VCO
Case ③: When the EFM signal is faster than the VCO

B. In abnormal operation

When the HIPD of CNTL-Z is chosen as 'L' from M-COM, the detector of the EFM phase operates as in Fig. 5. When the HIPD is 'H' and the time 'L' of LKFS is below 3.5T against a PBFS period T, it outputs Hi-Z to the PHAS terminal as long as 'L''. When it is above 3.5T, it outputs Hi-Z as long as 3.5T

2) EFM (Eight to Fourteen) Demodulator

The modulated 14 bit Data is inputted from a disc, then it is inputted into a NRZ-I circuit. As the EFM Data passes by the NRZ-I circuit which converts 14 bit data into 8 bit data, it gets demodulated 8 bit Data. There are two kinds of demodulated data: subcode and PCM data. The subcode data is inputted into the subcode Block, and the PCM Data is written into 16KSRAM by, with both $\overline{CE}$ signal and $\overline{WE}$ signal.

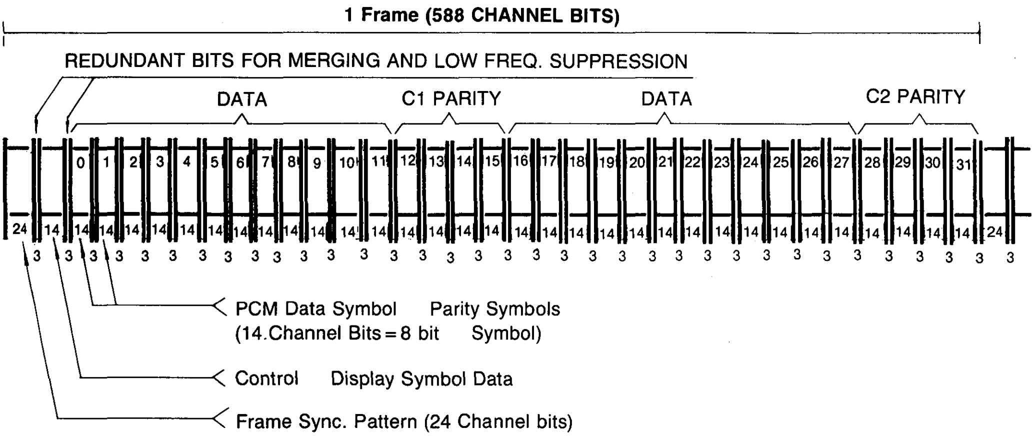
3) Frame Sync Detector/Inserter/Protector

A. Frame Sync Detector

A CDP data is composed of units of frame. A frame is made up of Frame Sync, Subcode Data, PCM Data, Redundancy Data. A Frame sync is detected per frame against this format.

B. Frame Sync Protector/Inserter

There are cases in which the Frame Sync is left out or detected from the data besides the frame sync because of the effects of an error on the disk or Jitter. In this case the frame sync needs to be protected and inserted. To protect the frame sync, a window is made by the use of WSEL signal of CNTL-S Reg. The frame sync which comes into the window is true data, and the frame sync deviating from the window is disregarded.



(Frame Format)

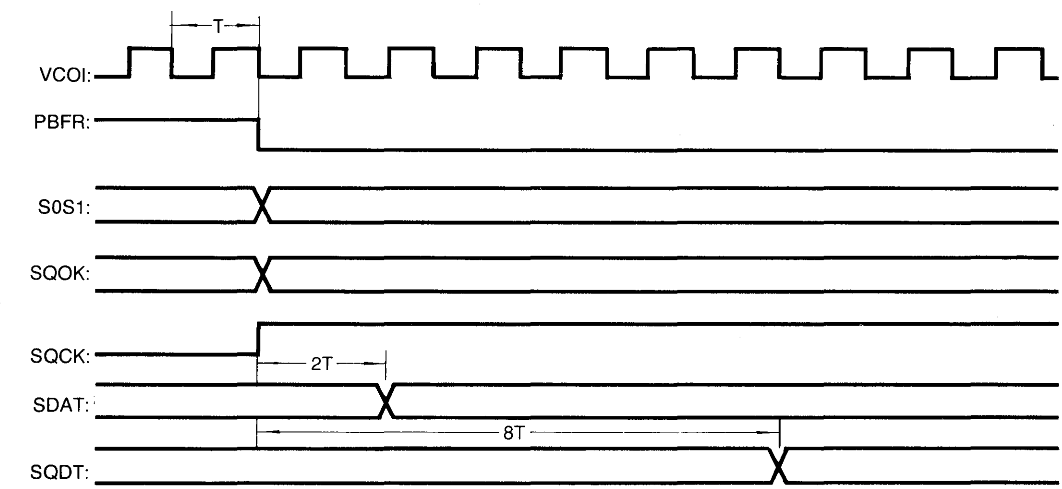
The width of the window is determined by the WSEL signal from the CNTL-S Reg. (cf. CNTL-S) Being inserted frame syncs continuously. If the frame sync is not detected inside a frame sync protection window, insert a frame sync. When the fame sync reaches the number of a frame designated by the FSEM and FSEL by the CNTL-S Reg ULKFS becomes 'L' and the frame sync protection window is disregarded. In this case an outputted frame sync is unconditionally accepted. After the frame sync is received, the ULKFS signal becomes 'H' and accepts a frame sync detected inside the window.

LKFS	ULKFS	Explanation
I	I	When a play back frame sync coincides with a generated frame sync.
O	I	① When a PBFR sync is detected in the window chosen by WSEL even if a play back frame sync does not coincide with a generated frame sync ② In the case of sync insertion because PBFR sync does not coincide with a XTER sync and a frame sync in the window chosen by WSEL is not detected.
O	O	① After inserting a sync as many as the number of frames decided by the FSEM and FSEL of the CNTL-S Reg. because Frame Sync is not detected in a window. ② When PBFR sync is not continuously detected after situation ① happens.

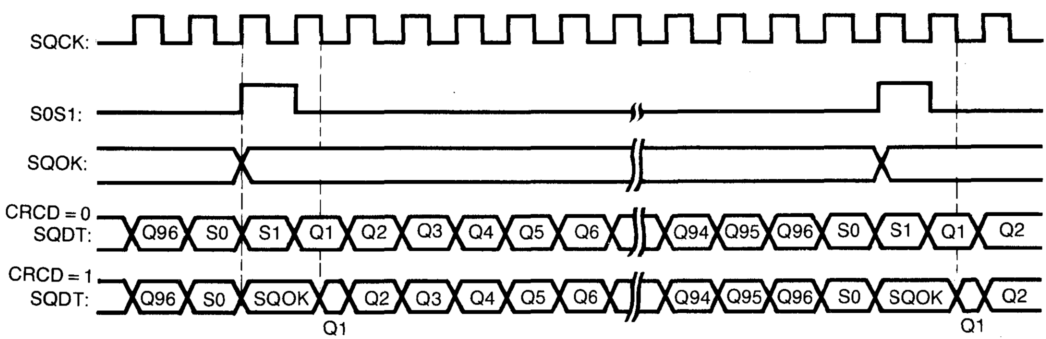
SUBCODE BLOCK

The 14 bit subcode sync signal S0, S1 is detected in the Subcode Sync Block. In a frame delay after the output of S0, S1 is detected. In this case, the signal os S0 + S1 is outputted through the S0S1 terminal, and the signal of S0·S1 is outputted through the SDAT terminal, when the signal S0S1 becomes 'H'. After the 14 bit Subcode Data inputted into the EFMI terminal get EFM Demodulation, an 8 bit P, Q, R, S, T, U, V, W subcode data are outputted to SDAT by SBCK clock after it syncronizes with the signal PBFR. Only Q data is chosen among the 8 subcode data, and it is loaded into 80 shift registers. The CRC-checked results of the loaded data is synchronized with the S0S1 rising edge, and is outputted to the SQCK terminal.
If the result of CRC checking is an error, 'L' is outputted to the SQCK terminal. If it is true, 'H' is outputted to the SQOK terminal. If the CRCD of CNTL-Z mode is 'H', the result of CRC checking is outputted to the SQDT terminal from the Section "H" of S0S1 section 'H' during the SQCK falling edge.
The timing chart of a subcode block is as follows:

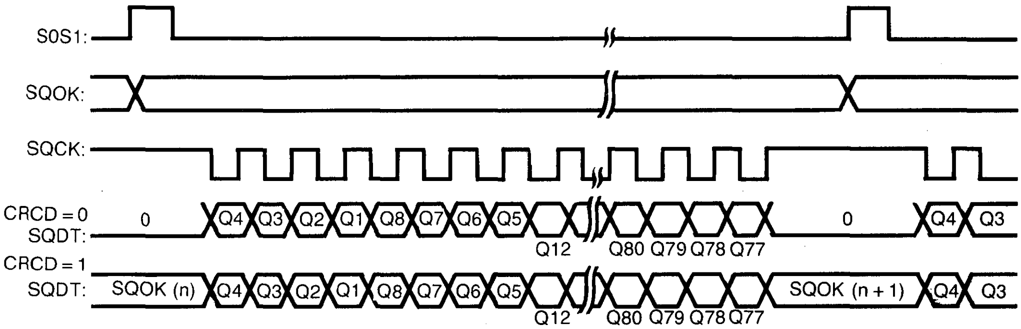
1) In SQEN = 'L': SDAT, SQDT, S0S1, SQOK, VCOI Timing Relation



2) In SQEN = 'L': SQOK, SQDT, S0S1, Timing Chart

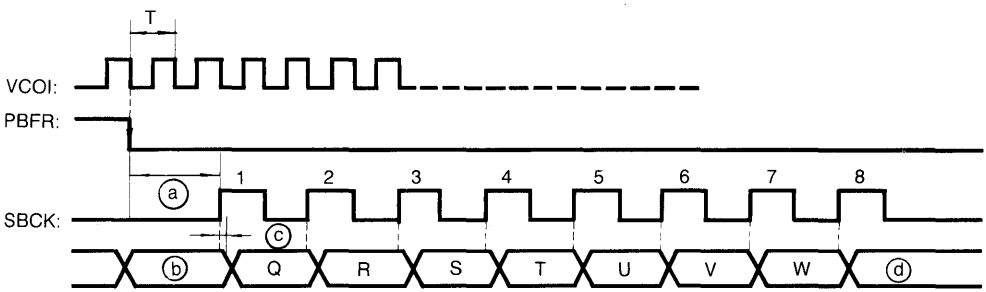


3) In SQEN = 'H': SQOK, SQDT, S0S1, SQCK Timing Chart



Comment: When a SQOK of subcode Q Data is 'H', subcode data is outputted to SQDT according to SQCK. When SQOK is 'L', 'L' is outputted to the SQDT terminal.

4) VCO1, SDAT, SBCK Timing Chart



ⓐ: *SBCK is set to "L" for about 10μS after PBFR becomes a falling edge.*

ⓑ: When S0S1 is 'L', a subcode P is outputted. When S0S1 is 'H', S0S1 is outputted.

ⓒ: When a cycle of VCO1 is 'T', the width of ⓒ is 4T ~ 6T.

ⓓ: When the pulse inputted into the SBCK terminal is above 7, subcode data P, Q, R, S, T, U, V, W is repeated.

ECC (Error-Correction Code) Block

The function of ECC Block is to recover the damage of data to some extent when the data on the disk was lost by damage. By using CIRC (Crossed-Interleave Reed-Solomon Code), C1 (32, 28) and C2 (28, 24) errors are corrected. ECC is performed with a 8 bit as a symbol unit. In correcting C1, a C1 Pointer is generated, and in correcting C2, a C2 pointer is generated.
C1, C2 Pointers send error information on the data to which ECC is given. After correcting C2, against can't corrected Data, Error Data is sent by outputing C2 Flag.
The signal C2FL is AND signal of C2F1 and C2F2. By using this information, Data is treated in the interpolator block.

C1F1	C1F2	C1, C2 Error	C2F1	C2F2	C2FL
0	0	No Error	0	0	0
0	1	Single Error	0	1	0
1	0	Double Error	1	0	0
1	1	Irretrievable Error	1	1	1

C1F1, C1F2 — Output the state of an error correction by C1 Decoder

C2F1, C2F2 — Output the state of an error correction by C2 Decoder

C2FL — Becomes 'L' when an error correction by C2 Decoder is possible and an 'H' error correction is impossible.

16K SRAM BLOCK

After EFM demodulation of EFM modulated data inputted from disc, when the Data is written into RAM or data is outputted to Read/Write and D/A Converters in ECC Processing, for reading, SRAM Address Generator and a 16K SRAM have installed in there.
SRAM terminal must be 'H' in 16K SRAM application.

1) Address Generation Priority Control

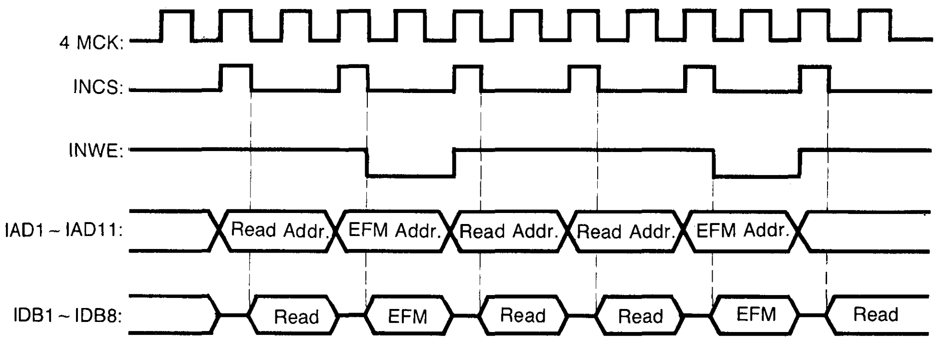
Writing in EFM demodulation, reading the data with R/W, D/A Converter in ECC process, sometimes these processes are required at the same time.
When 3 signals are demanded at the same time, priority of the data process needs to be controlled. Priority is D/A Converter Read demand > EFM Write demand > ECC R/W demand.

2) EFM Demodulation Data Write Demand

EFM demodulated data mube be written to SRAM, priority is controlled when the write demand signal is transmitted to the SRAM Address Generator, and the Enable signal is transmitted to the EFM Block. The generated address is transmitted to the SRAM Interface circuit.
Generated address is data which deinterleave is considered, and in a frame 32 addresses are generated.

A. In the use of 16K SRAM (in EFM & ECC Write): SRAM terminal 'H'

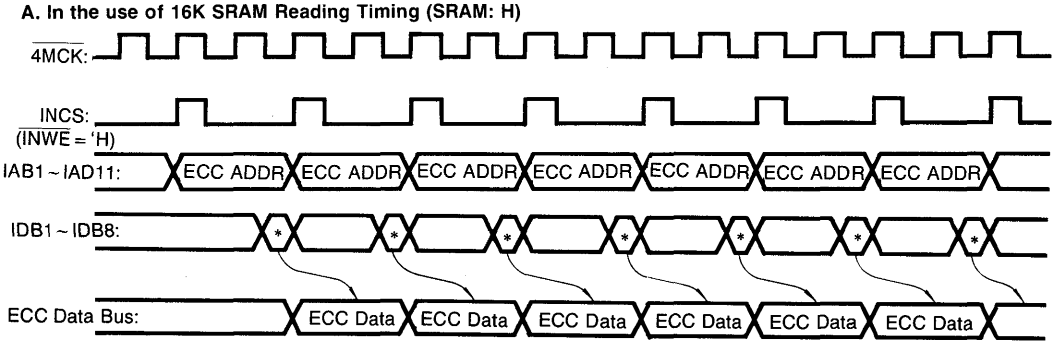
DB1 ~ DB8 and AD1 ~ AD11 terminals are in a state of Hi-Z. $\overline{CE}$ and $\overline{WE}$ are 'Don't Care.'



3) R/W Demand of ECC Data

For C1 and C2 ECC treatment 129 times of Address demand signals generated due to an R/W operation must be given to 64 PCM data and 65 Pointers during a frame.
The write of FCC processing is the same as 2) EFM Write operation.
In reading it is as follows:

A. In the use of 16K SRAM Reading Timing (SRAM: H)



*: Valid ECC Data

4) D/A Converter Read Demand

Since each 6 sampling data on the left and right channel and 12 C2 Pointer data must be read for a frame, 36 read enable demand signals are caused. The timing chart for D/A Converter Read is the same as the R/W demand block of ECC data. As a result the number of the maximum R/W operation action demanded for a frame is 179 times.

5) Address Generated Block

The interleaving data in encoding is deinterleaved in decoding. The data of 108 frames is needed to get 8 frame of PCM data in a CDP format. To get data suitable for a CDP format 2 counters are needed. A write base counter is used to write EFM demodulation data are hindered in storing data in SRAM due to disk shaking, the instability of a servo system etc.

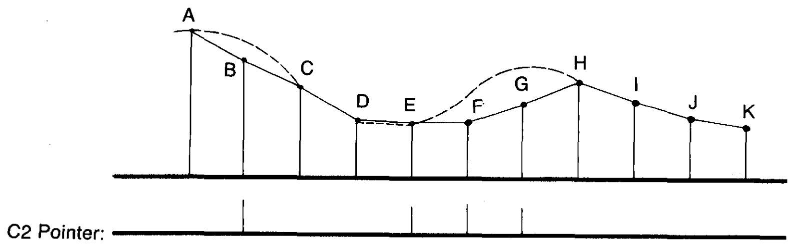
6) Jitter Margin

EFM demodulation data are hindered in storing data in SRAM due to disk shaking, the instability of a servo system etc. Now that the data that must be kept is limited by the size of SRAM in view of time, data is destroyed if the value of read/write base counter has a difference above ±5 frames. Being loading into the value of write base counter with enforcement, the value of read base counter has a jitter margin below ±4 frames when there is a difference over ±5 frames in the read/write base counter value.

A read base counter value is baded into a write base counter with enforcement when data on the left and right channels are all muting, or when NCLV is 'H', and CLV-Servo is stop, forward and reverse. When the difference between read/write base counter is above ±4 frame, a 'H' signal is outputted to the $\overline{JIT}$ terminal for a period.

INTERLEAVE, MUTE BLOCK

When a burst error occurs on a disk, sometimes the data can't be corrected even if a ECC process is conducted. An interpolator block revises data by using C2 Pointer outputted through the ECC Block. PCM data inputted into a data bus are inputted to the left and right channels respectively in order of 8 bit C2 Pointer, Lower 8 bit and Upper 8 bit. A pre-hold method is taken when a DA Flag is 'H' continuously. In case of the occurrence of a single error, a mean value interpoalting method is carried out with the range of PCM Data before and after an error happens. When a check against a checked cycle is 'L', R-CH Data is outputted. L-CH Data is outputted when the check is 'H'. As to the timing chart of a interpolator block see figure 6.



$B = \frac{A+C}{2}$: Mean value interpolation

F = E = D : Pre-hold interpolation

G = F + H : Mean value interpolation

2) Mute and Attenuation

By a Mute terminal and a ATTM signal by the CNTL-S Reg., AUDIO data is muted or reduced. There are two kinds of mute: zero cross muting, muting.

A. Zero Cross Muting
Audio data is muted when a mute terminal is 'H' and when 6 bits in a high position of Audio Data is all 'H' or 'L'.

B. Muting
Audio data is muting when ZCMT of the CNTL-Z Reg. is 'L' and when a mute terminal is 'H'.

C. Attenuation
By means of the ATTM signal of the CNTL-S Reg. and the signal of Mute terminal, a audio signal attenuation occurs as the following.

ATTM	MUTE	Degree of Attenuation
0	0	0 dB
0	1	– dB
1	0	– 12 dB
1	1	– 12 dB

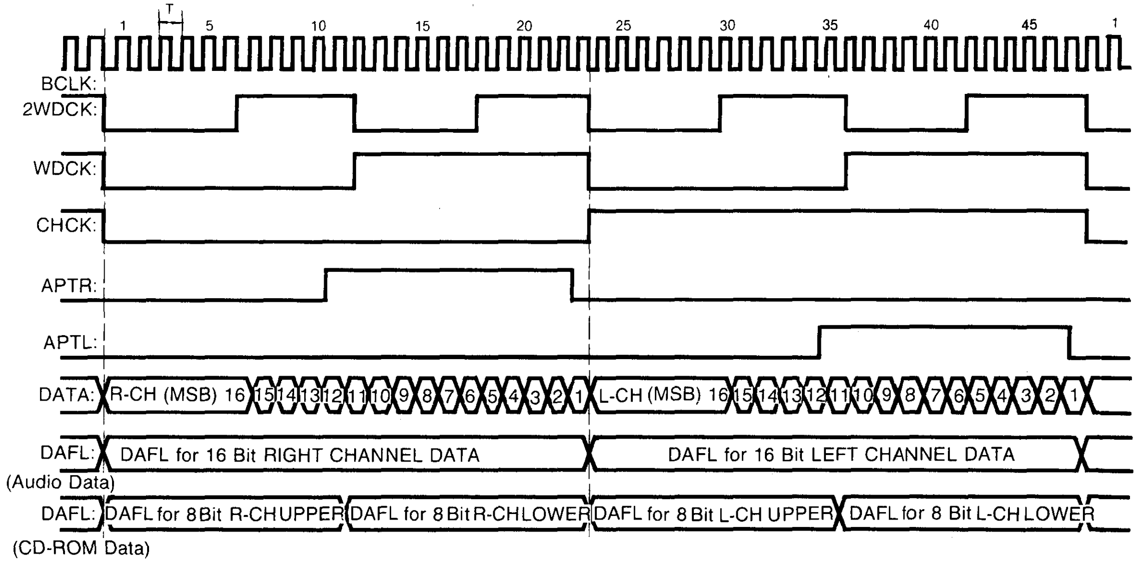


Fig. 6. When Sel. 5 is 'L', and DF is off, the Timing Chart of PCM Data

CLV SERVO

CNTL-C Reg. is selected to control CLV Servo by the Data inputted from μ-COM. In CNTL-C Reg, the data from μ-com appoint CLV servo action mode and control spindle motor.

1) Forward

The states of output terminal related to the mode to rotate a spindle motor forward are SMDP = 'H', SMSD = Hi-Z, SMEF = 'L' and SMON = 'H' respectively.

2) Reverse

The modes to rotate a spindle motor reversly are SMDP = 'L', SMSD = 'Hi-Z', SMEF = 'L', and SMOD = 'H'.

3) SPEED-Mode

The SPEED-Mode is the mode for the rough control of a spindle motor when a track jumping or a EFM phase is unlocked. If a cycle of VCO is 'T', the pulse width of a frame sync is '22T'. Sometimes EFM signal is above 22T due to noises on a disc, etc. A correct frame sync cannot be detected when the signal is not removed. In this case, the pulse width of EFM signal is detected at a cycle of XTFR/2 or XTFR/4 which are peak hold clocks. The pulse width of EFM signal is detected at a cycle of XTFR/16 or XTFR/32 which are bottom hold clock. The value detected is used for a frame synchronization signal. When the frame synchronization signal is smaller than 21T, the SMPD terminal outputs 'L'. When it is 22T, Hi-Z is outputted. 'H' is outputted when it is above 23T.
When the GAIN signal of CNTL-W Reg. is 'L', the SMDP terminal is outputted after being attenuated at − 12dB when the signal is 'H', the terminal is outputted without any attenuation. <cf. figure 7>
In SMSD, SMEF, and SMON terminals Hi-Z, 'L', and 'H' are outputted.

4) HSPEED-Mode

The rough servo mode which moves 20,000 tracks in high speed acts between inside of CD and outside of CD. In the domain of a mirror of the track without a pit EFM and the signal of 20KHz overlap. In the case, since in the speed-mode the peak range of a longer mirror signal than the original frame sync is detected, the servo operation become unstable. In HSPEED-mode a peak hold uses a 8.4672/256 MHz signal, and a bottom hold removes a mirror component and stabilizes the high speed servo operation by using XTFR/16 or XFFR/32 period signal.
In SMSD, SMEF, and SMON terminals, Hi-Z, 'L', and 'H' are outputted.

5) PHASE-Mode

A PHASE Mode is the mode to control an EFM Phase. When NCLV of CNTL-Z is 'L', it detects a phase difference between PBFR/4 and XTFR/4, and when NCLV is 'H', it detects the phase difference between. Read base Counter/4, write base Counter/4, and then output to SMPD terminal. See figure 8.
If the VCO/2 signal cycle is put as 'T' and the PBFR during a 'H' period as a W_{pb}, it outputs 'H' to a SMSD terminal from the falling edge of PBFR for (W_{pb}-278T) x 32, and later outputs 'L' to the falling edge of PBFR. Refer to figure 9.

6) XPHSP-Mode

A XPHSP mode is the mode used in normal operation. It samples a LKFS signal made in the frame sync block at a cycle of PBFR/16. After sampling 'H', DHASE mode is carried out. When 'L' is sampled continuously 8 times, it goes over to speed-mode. CNTL-W Reg. decides the choice of the peak hold of speed-mode, the bottom hold cycle of SPEED and HSPEED-Mode and the choice of a gain.

7) VPHSP-Mode

A VPHSP-Mode is the mode used for rough servo control. It uses VCO instead of X'tal in the EFM pattern test. When the range of VCO center changes, VCO is easily loaded because the rotation of a spindle motor changes in the same direction.

8) STOP

Stop is the mode to stop a spindle motor.
SMDP = 'L', SMSD = Hi-Z, SMEF = 'L', SMON = 'L'

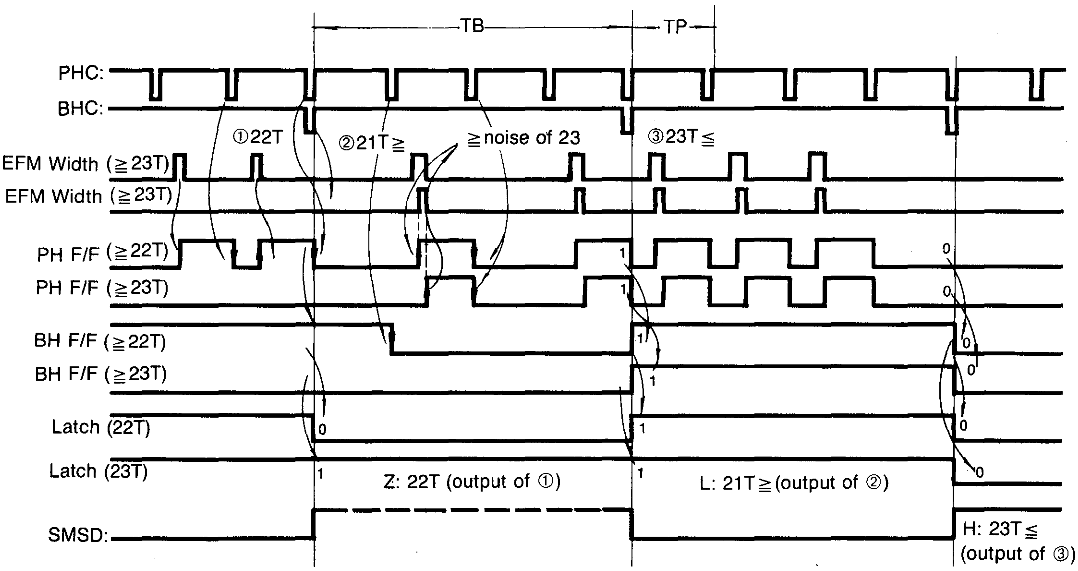


Fig. 7 When gain is 'H' in a speed-mode Timing Charg of SMSD output

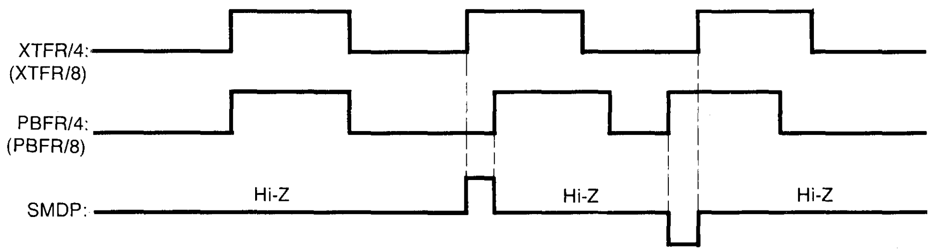
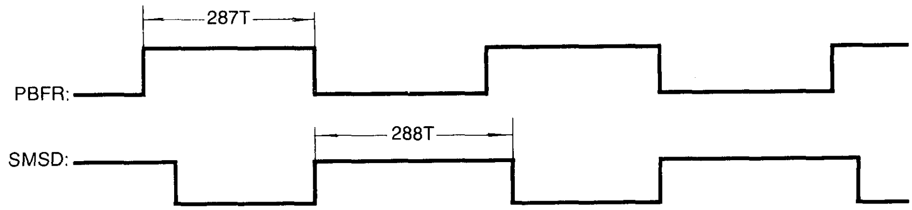
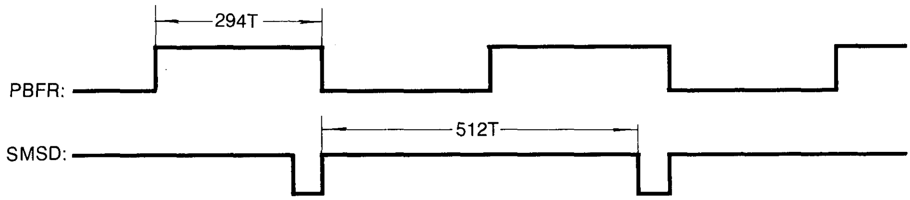


Fig. 8 Output Timing Chart of a SMDP terminal



(a) When PBFR is 287T, Timing Chart of SMSD output



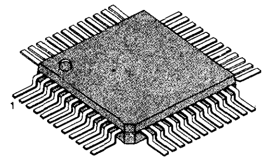
(b) When PBFR is 294T, Timing Chart of SMSD output

Fig. 9 In a PHASE Mode Timing Chart of SMSD output (T: VCO/2)

SERVO SIGNAL PROCESSOR

The KA8309 is BiCMOS integrated circuit designed for the servo control of the compact disc player application.

48 FQP



FEATURES

- **Servo control functions; (focus, tracking, seld servo control)**
- **Loop filter and VCO for EFM clock reproduction PLL**
- **Provide function**
  Preventing sled runaway
  Anti-shock
  Spindle servo
  Auto-sequencer
- **Provide adjustable peak of focus search, track jump and sled kick with external resistor**
- **Low power consumption (100mW typ; ±5V, 80mW, 5V)**
- **Single power supply, 5V**
- **Split power supply, ±5V**

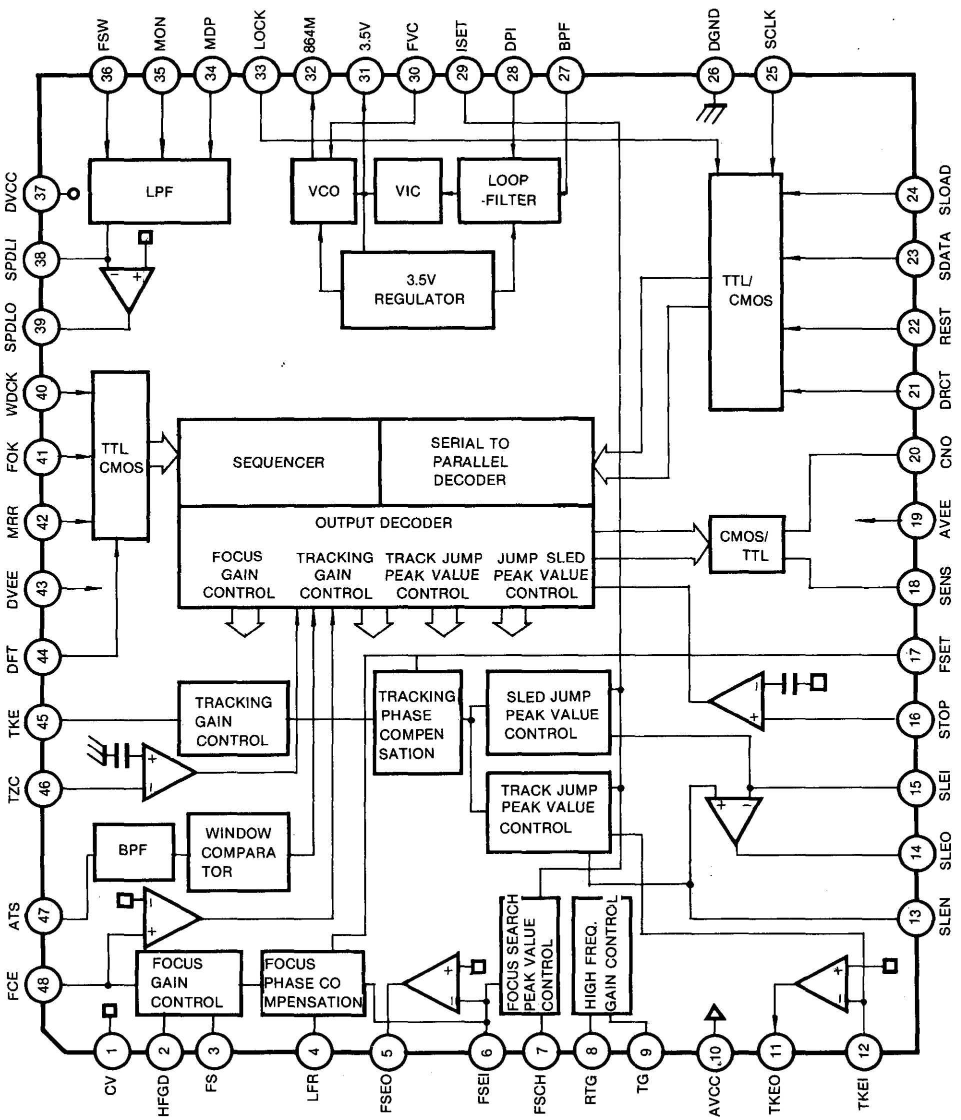
ORDERING INFORMATION

Device	Package	Operating Temperature
KA8309	48 FQP	−20 ~ +75°C

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	$V_{CC} - V_{EE}$	12	V
Power Dissipation	P_d	600	mW
Operating Temperature	T_{opr}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Descriptions
1	CV	Center voltage.
2	HFGD	Reduce high frequency gain with capacitor connected between pin 2 and pin 3.
3	FS	High frequency gain of focus servo can be changed by switching FS3 on or off.
4	LFR	Rising low frequency bandwidth of focus loop.
5	FSEO	Focus servo error output.
6	FSEI	Inverting input pin for focus amplifier.
7	FSCH	Time constant external pin to generate focus search waveform.
8	RTG	Time constant external pin to switch the tracking gain of high frequency.
9	TG	Provide time constant to change the high frequency tracking gain.
10	AV_{CC}	Analog positive power supply.
11	TKEO	Tracking error output.
12	TKEI	Inverting input pin for tracking amplifier.
13	SLEN	Non-inverting input pin for tracking amplifier.
14	SLEO	Sled output.
15	SLEI	Inverting input pin for sled amplifier.
16	STOP	Pin for detecting a signal for the on/off limit switch of the innermost part of the disc.
17	FSET	Setting the peak frequency of the focus, tracking phase compensation and to fo the CLV LPF.
18	SENS	Output pin for FZC, AS, TZC, STOP and BUSY by command from CPU.
19	AV_{EE}	Analog negative power supply.
20	CNO	Track number count output.
21	DRCT	Control pin for one track jump.
22	REST	Reset input pin, reset at "L".
23	SDATA	Serial data input.
24	SLOAD	Latch input.
25	SCLK	Serial data transfer clock.
26	DGND	Digital ground.
27	BPF	Provide time constant for the loop filter.

PIN DESCRIPTION (Continued)

Pin No.	Symbol	Descriptions
28	DPI	Input pin for detected phase.
29	ISET	Current is input, determining the peaks of focus search, track jump, and sled kick.
30	FVC	External resistor to adjust free running frequency of VCO.
31	3.5V	Regulated output voltage.
32	864M	Output pin of 8.64MHz VCO.
33	LOCK	Pin for the operation of the sled runaway prevention circuit at "L".
34	MDP	Pin for connecting the DSP.
35	MON	Pin for connecting the DSP.
36	FSW	Providing an external LPF time constant of the CLV servo.
37	DV_{CC}	Digital positive power supply.
38	SPDLI	Inverting input for spindle servo amplifier.
39	SPDLO	Spindle servo error output.
40	WDCK	Clock input for auto-sequence.
41	FOK	Focus ok signal input pin.
42	MRR	Mirror signal input pin.
43	DV_{EE}	Digital negative power supply.
44	DFT	Defect signal input pin.
45	TKE	Tracking error signal input pin.
46	TZC	Input pin for the zero cross tracking comparator.
47	ATS	Input pin for detect ATSC.
48	FCE	Input pin for focus error signal.

4

ELECTRICAL CHARACTERISTICS

($T_a = 25°C$, $V_{CC} = 2.5V$, $V_{DD} = 2.5V$, $V_{EE} = -2.5V$, GND = 0V, unless otherwise specified)

	Characteristic	No.	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current 1		1	I_{CCA}		2	6	10	mA
Supply Current 2		2	I_{CCD}		5	10	15	mA
Supply Current 3		3	I_{EF}		2	4.5	8	mA
Supply Current 4		4	I_{GND}		4.8	8	11	mA
Focus Servo	DC Voltage Gain	5	A_{FEO}	SG = 10Hz, 200mV	18	21	24	dB
	Feed Through	6	V_{FEOF}	SG = 10KHz, 40mV Gain difference between 08 and 00 of SD			−35	dB
	Max. Output Voltage 1	7	V_{FE01}	SG = 0.5V_{DC}	1.98			V
	Max. Output Voltage 2	8	V_{FE02}	SG = 0.5V_{DC}			−1.98	V
	Max. Output Voltage 3	9	V_{FE03}	SG = 0.5V_{DC}	1.18			V
	Max. Output Voltage 4	10	V_{FE04}	SG = 0.5V_{DC}			−1.18	V
	Search Output Voltage 1	11	V_{SRCH1}		−0.64	−0.55	−0.36	V
	Search Output Voltage 2	12	V_{SRCH2}		0.36	0.55	0.64	V
Tracking Servo	DC Voltage Gain	13	A_{TEO}	SG = 10Hz, 200mV	11.6	14.6	17.6	dB
	Feed Through	14	V_{TEOF}	SG = 10KHz, 10mV Gain difference between 25 and 20 of SD			−39	dB
	Max. Output Voltage 1	15	V_{TEP1}	SG = 0.5V_{DC}	1.98			V
	Max. Output Voltage 2	16	V_{TEP2}	SG = −0.5V_{DC}			−1.98	V
	Max. Output Voltage 3	17	V_{TEP3}	SG = 0.5V_{DC}	1.18			V
	Max. Output Voltage 4	18	V_{TEP4}	SG = −0.5V_{DC}			−1.18	V
	Jump Output Voltage 1	19	V_{JUMP1}		−0.64	−0.55	−0.36	V
	Jump Output Voltage 2	20	V_{JUMP2}		0.36	0.55	0.64	V
Sled Servo	DC Voltage Gain	21	A_{SLD}	SG = 10Hz, open loop gain	50	56	62	dB
	Max. Output Voltage 1	22	V_{SLP1}	SG = 0.4V_{DC}	1.09			V
	Max. Output Voltage 2	23	V_{SLP2}	SG = −0.4V_{DC}			−1.98	V
	Max. Output Voltage 3	24	V_{SLP3}	SG = 0.4V_{DC}	1.18			V
	Max. Output Voltage 4	25	V_{SLP4}	SG = −0.4V_{DC}			−1.18	V
	Feed Through	26	V_{SLOF}	SG = 10KHz, 200mV Gain difference between 25 and 20 of SD			−34	dB
	Kick Output Voltage 1	27	V_{KICK1}		−0.75	−0.6	−0.45	V
	Kick Output Voltage 2	28	V_{KICK2}		0.45	0.6	0.75	V

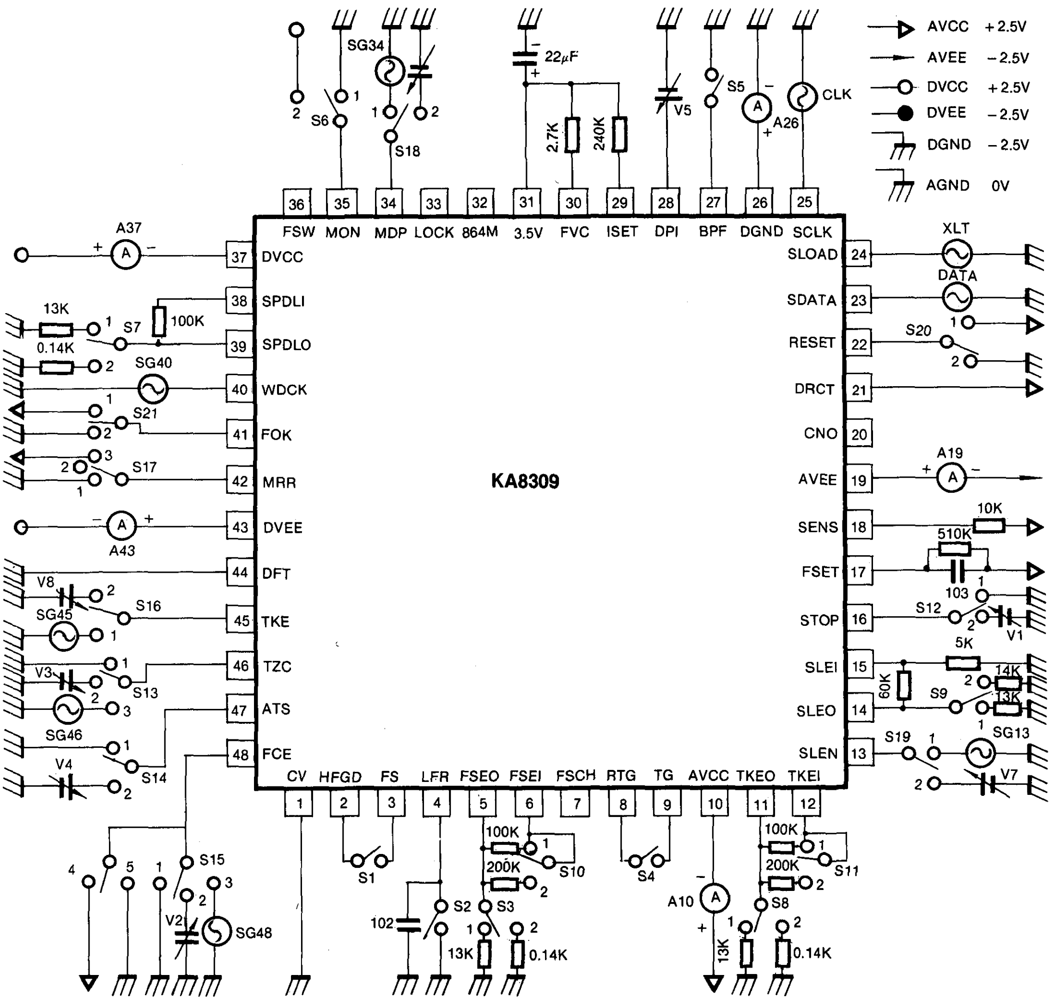
ELECTRICAL CHARACTERISTICS (Continued)

	Characteristic	No.	Symbol	Test Conditions	Min	Typ	Max	Unit
Spindle Servo	Spindle Servo Gain	29	A_{SPO}	SG = 10Hz, 20mV	14	16.5	19	dB
	Max. Output Voltage 1	30	V_{SPP1}	SG = 1.0V_{DC}	1.78			V
	Max. Output Voltage 2	31	V_{SPP2}	SG = − 10V_{DC}			− 1.78	V
	Max. Output Voltage 3	32	V_{SPP3}	SG = 1.0V_{DC}	1.13			V
	Max. Output Voltage 4	33	V_{SPP4}	SG = − 10V_{DC}			− 1.13	V
PLL	PLL Reg. Output Voltage	34	V_{reg}		3.3	3.5	3.85	V
	Self-running Frequency	35	F_{VCO}	V1 = 0mV	7.4	8.6	9.7	MHz
	Frequency Deviation 1	36	△F1	Frequency deviation from F_{VCO}, V1 = 148mV	7	11	15	%
	Frequency Deviation 2	37	△F2	V1 = 148mV	− 15	− 11	− 7	%
	Sexs Low Level	38	V_{SENS}				− 1.98	V
COUT Low Level		39	V_{COUT}				− 1.98	V
FZC Threshold Value		40	V_{TZC}	Value of E when SENS becomes high (= 1.1V) by E1 to E4 Varying SG = 0V	39	50	61	mV
ATSC Threshold Value		41	V_{ATSC1}		− 45	− 26	− 7	mV
ATSC Threshold Value		42	V_{ATSC2}		7	26	45	mV
TZC Threshold Value		43	V_{TZC}		− 20	0	20	mV
SSTOP Threshold Value		44	V_{SSTOP}		− 65	− 50	− 35	mV

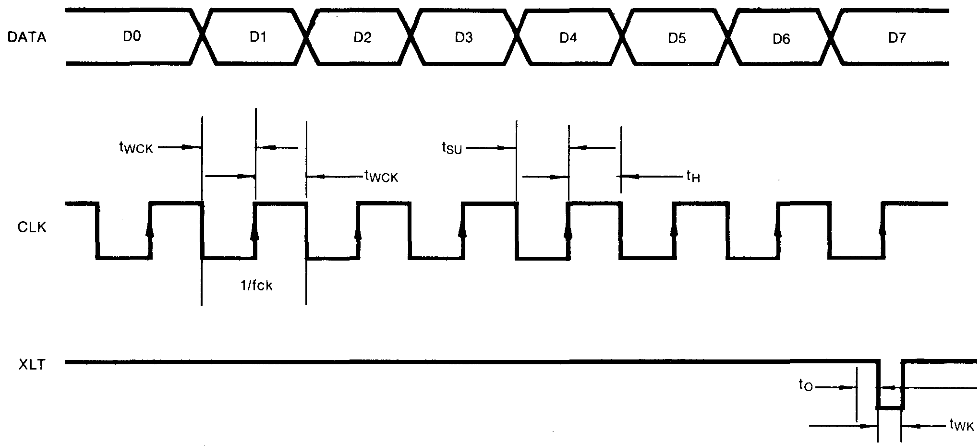
TEST METHODE (SWITCH CONDITIONS)

No.	Symbol	SW Conditions											I	Bias Conditions				Input Point	Test Point
		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	SD	E1	E2	E3	E4		
1	AI_{CC}												00	○	○	○	○		10
2	DI_{CC}													○	○	○	○		37
3	$A.D_{IEF}$													○	○	○	○		19 43
4	ID_{GND}													○	○	○	○		26
5	G_{FED}												08	○	○	○	○	48	5
6	V_{FEOF}	○	○											○	○	○	○	48	5
7	V_{FEO1}										○		08	○	○	○	○	48	5
8	V_{FEO2}										○		08	○	○	○	○	48	5
9	V_{FEO3}			○							○		08	○	○	○	○	48	5
10	V_{FEO4}			○							○		08	○	○	○	○	48	5
11	V_{SRCH1}												02	○	○	○	○		5
12	V_{SRCH2}												03	○	○	○	○		5
13	G_{TEO}				○								26	○	○	○	○	45	11
14	V_{TEOF}				○								13	○	○	○	○	45	11
15	V_{TEP1}											○	25	○	○	○	○	45	11
16	V_{TEP2}											○	25	○	○	○	○	45	11
17	V_{TEP3}								○			○	25	○	○	○	○	45	11
18	V_{TEP4}								○			○	25	○	○	○	○	45	11
19	V_{JUMP1}												2C	○	○	○	○		11
20	V_{JUMP2}												28	○	○	○	○		11
21	G_{SLO}												25	○	○	○	○	13	14
22	V_{SL1}												25	○	○	○	○	13	14
23	V_{ALP2}												25	○	○	○	○	13	14
24	V_{SLP3}									○			25	○	○	○	○	13	14
25	V_{SLP4}									○			25	○	○	○	○	13	14
26	V_{SLOF}													○		○	○	13	14
27	V_{KICK1}												22	○		○	○		14
28	V_{KICK2}												23	○		○	○		14
29	G_{SPO}						○							○		○	○	34	39
30	V_{SPP1}						○							○		○	○	34	39
31	V_{SPP2}						○							○		○	○	34	39
32	V_{SPP3}						○	○						○		○	○	34	39
33	V_{SPP4}						○	○						○		○	○	34	39
34	V_{reg}													○		○	○		31
35	F_{VCO}													○	○	○	○		32
36	△F1													○	○	○	○		32
37	△F2													○	○	○	○		32
38	V_{SENS}													○	○	○	○		18
39	V_{COUT}													○	○	○	○		20
40	V_{TZC}												00	○	*	○	○	48	18
41	V_{ATSC1}												10	○	○	○	*	47	18
42	V_{ATSC2}												10	○	○	○	*	47	18
43	V_{TZC}												20	○	○	*	○	46	18
44	V_{SSTOP}												30	*	○	○	○	16	18

TEST CIRCUIT



CPU Serial Interface Timing Chart



$DV_{CC} - D_{GND} = 4.5$ to $5.5V$

Item	Symbol	Min	Typ	Max	Unit
Clock Frequency	f_{CK}			1	MHz
Clock Pulse Width	f_{WCK}	500			ns
Hold Time	t_{SU}	500			ns
Setup Time	t_H	500			ns
Delay Time	t_D	500			ns
Latch Pulse Width	t_{WL}	1000			ns

SYSTEM CONTROL

Item		Address				Data				Sens Output
		D7	D6	D5	D4	D3	D2	D1	D0	
Focus Control		0	0	0	0	FS4 Focus On	FS3 Gain Down	FS2 Search On	FS1 Search Up	FZC
Tracking Control		0	0	0	1	Anti Shock	Brake On	TG2 Gain Set *1	TG1	A.S
Tracking Mode		0	0	1	0	Tracking Mode *2		Sled Mode *3		TZC
Select		0	0	1	1	PS4 Focus Search+2	PS3 Focus Search+1	PS2 Sled Kick+2	PS1 Sled Kick+1	SSTOP
Auto Sequence *4		0	1	0	0	AS3	AS2	AS1	AS0	BUSY
	Blind(A,E)/Overflow(C)	0	1	0	1	0.18ms	0.09ms	0.045ms	0.022ms	Hi-Z
	Brake(B)					0.36ms	0.18ms	0.09ms	0.045ms	
	Kick(D)	0	1	1	0	11.6ms	5.8ms	2.9ms	1.45ms	
	Track Jump(N)	0	1	1	1	64	32	16	8	
	Track Move(M)					128	64	32	16	

Note: ***1. GAIN SET**
It is possible to set TG1 and TG2 independently.
When the anti-shock is 1 (00011xxx), invert both TG1 and TG2 when the internal anti-shock is H.

*5 RAM SET

***2 TRACKING MODE**

	D3	D2
OFF	0	0
ON	0	1
FWD JUMP	1	0
REV JUMP	1	1

***3 SLED MODE**

	D1	D0
OFF	0	0
ON	0	1
FWD MOVE	1	0
REV MOVE	1	1

***4 AUTO SEQUENCE**

	AS3	AS2	AS1	AS0
CANCEL	0	0	0	0
FOCUS ON	0	1	1	1
1 TRACK JUMP	1	0	0	X
10 TRACK JUMP	1	0	1	X
2N TRACK JUMP	1	1	0	X
M TRACK MOVE	1	1	1	X

X=0 FORWARD
X=1 REVERSE

- When CANCEL $40 is sent, the status immediately preceding the auto sequence mode (just before $4X is sent) is reset.
- The auto sequence mode starts with the first falling of the pin 40 input pulse (WDCK) after the $4X transfer and the falling of latch pulse.

***5 RAM SET**
- Values $0 to $E (not $F) can be set.
- The above set values are ones when WDCK (88.2KHz) is input to pin 40.
- The RAM is preset when the power is switched on and the internal initial/set values are as follows:

Address				Data			
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	1
0	1	1	1	1	1	1	0

- The actual count values are slightly different from the set values.

A	set value + 4 to 5	WDCK
B,D,E	set value + 3	WDCK
C	set value + 5	WDCK
N,M	set value + 3	Count out

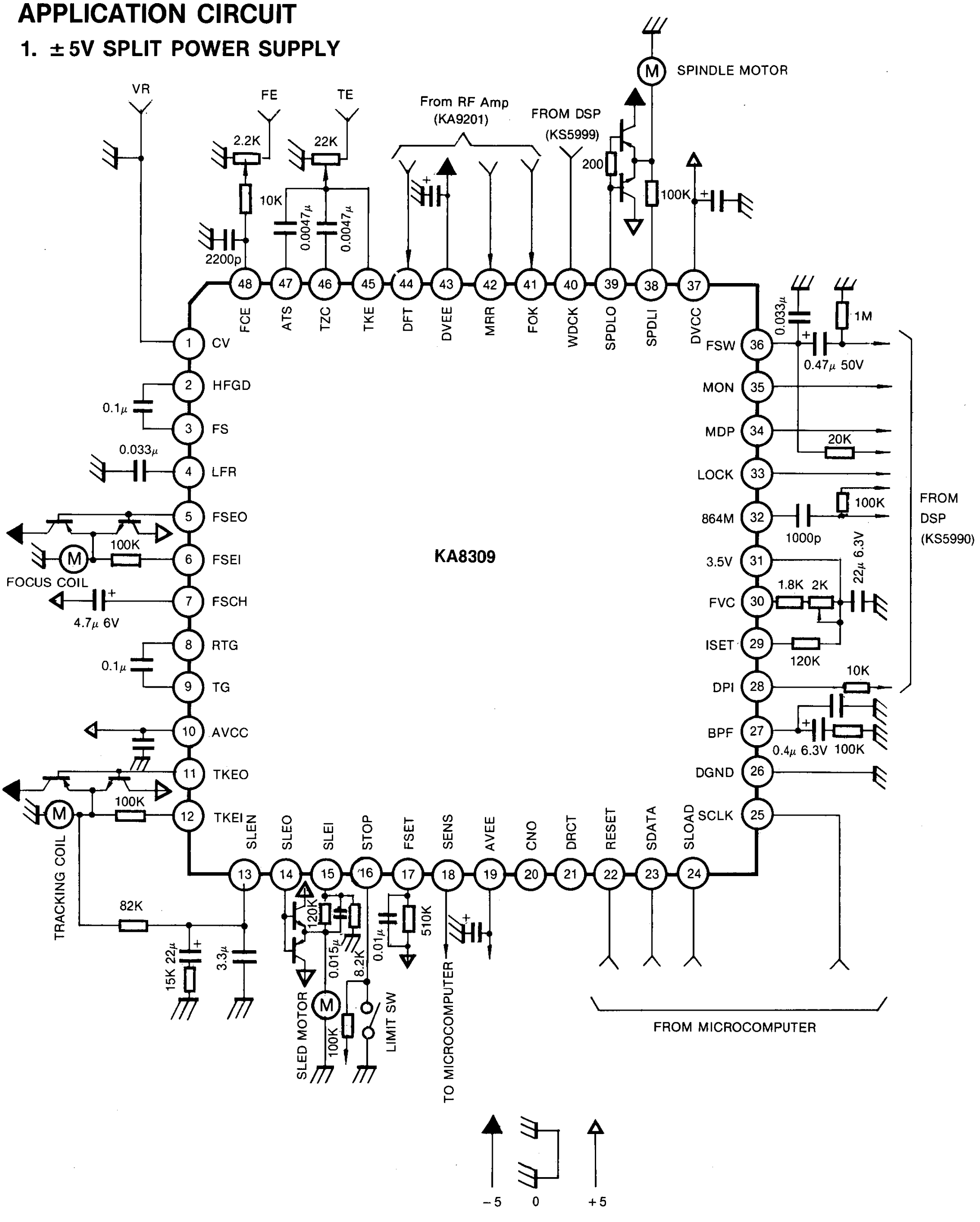
SERIAL DATA TRUTH TABLE

Serial Data								Hexa.	Function			
FOCUS CONTROL									FS = 4321			
0	0	0	0	0	0	0	0	$00	0	0	0	0
0	0	0	0	0	0	0	1	$01	0	0	0	1
0	0	0	0	0	0	1	0	$02	0	0	1	0
0	0	0	0	0	0	1	1	$03	0	0	1	1
0	0	0	0	0	1	0	0	$04	0	1	0	0
0	0	0	0	0	1	0	1	$05	0	1	0	1
0	0	0	0	0	1	1	0	$06	0	1	1	0
0	0	0	0	0	1	1	1	$07	0	1	1	1
0	0	0	0	1	0	0	0	$08	1	0	0	0
0	0	0	0	1	0	0	1	$09	1	0	0	1
0	0	0	0	1	0	1	0	$0A	1	0	1	0
0	0	0	0	1	0	1	1	$0B	1	0	1	1
0	0	0	0	1	1	0	0	$0C	1	1	0	0
0	0	0	0	1	1	0	1	$0D	1	1	0	1
0	0	0	0	1	1	1	0	$0E	1	1	1	0
0	0	0	0	1	1	1	1	$0F	1	1	1	1
TRACKING CONTROL									AS = 0		AS = 1	
									TG = 2	1	TG = 2	1
0	0	0	1	0	0	0	0	$10	0	0	0	0
0	0	0	1	0	0	0	1	$11	0	1	0	1
0	0	0	1	0	0	1	0	$12	1	0	1	0
0	0	0	1	0	0	1	1	$13	1	1	1	1
0	0	0	1	0	1	0	0	$14	0	0	0	0
0	0	0	1	0	1	0	1	$15	0	1	0	1
0	0	0	1	0	1	1	0	$16	1	0	1	0
0	0	0	1	0	1	1	1	$17	1	1	1	1
0	0	0	1	1	0	0	0	$18	0	0	1	1
0	0	0	1	1	0	0	1	$19	0	1	1	0
0	0	0	1	1	0	1	0	$1A	1	0	0	1
0	0	0	1	1	0	1	1	$1B	1	1	0	0
0	0	0	1	1	1	0	0	$1C	0	0	1	1
0	0	0	1	1	1	0	1	$1D	0	1	1	0
0	0	0	1	1	1	1	0	$1E	1	0	0	1
0	0	0	1	1	1	1	1	$1F	1	1	0	0

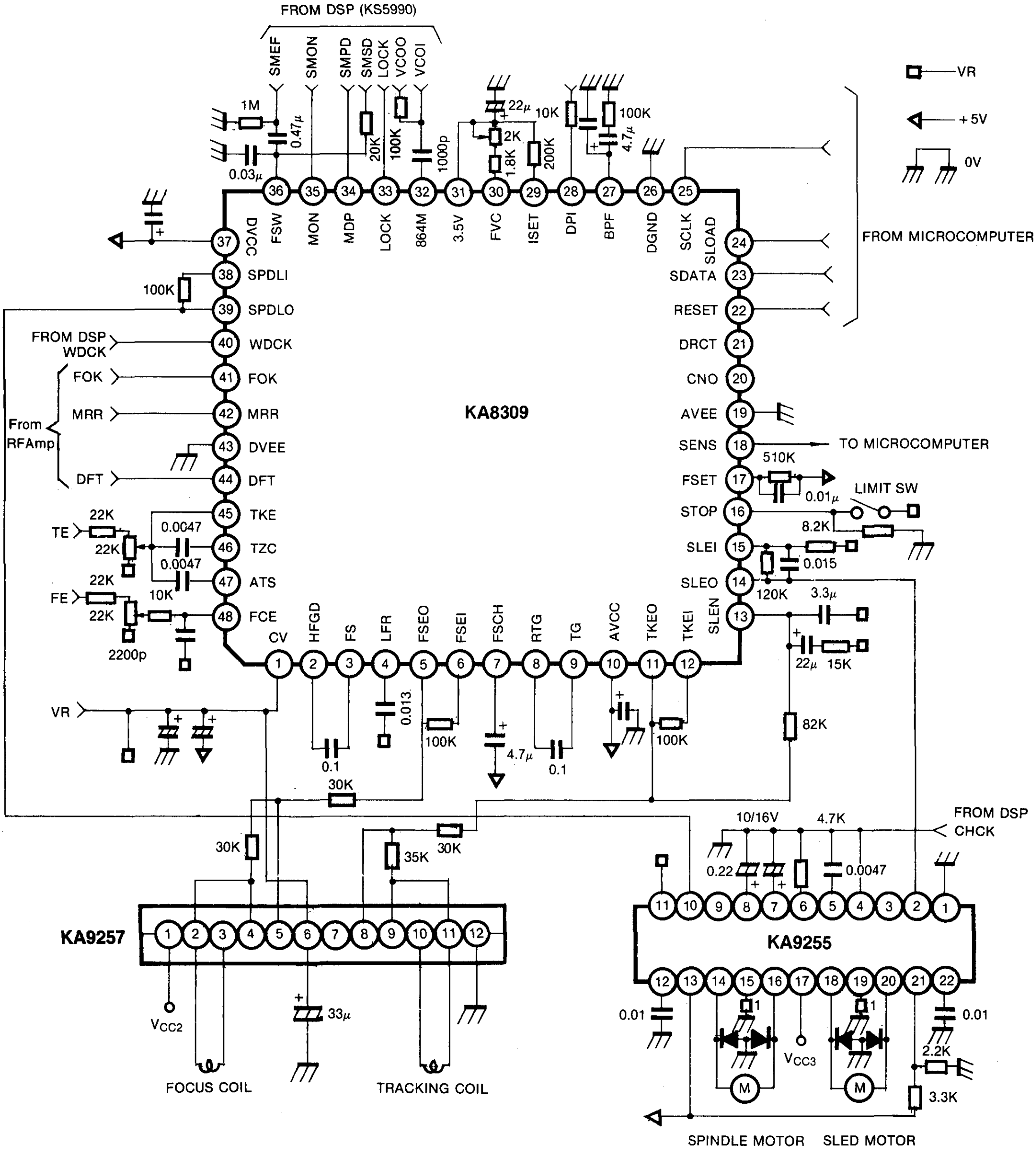
Serial Data	Hexa.	Function		
TRACKING MODE		DIRC = 1 TM = 654321	DIRC = 0 654321	DIRC = 1 654321
0 0 1 0 0 0 0 0	$20	000000	001000	000011
0 0 1 0 0 0 0 1	$21	000010	001010	000011
0 0 1 0 0 0 1 0	$22	010000	011000	100001
0 0 1 0 0 0 1 1	$23	100000	101000	100001
0 0 1 0 0 1 0 0	$24	000001	000100	000011
0 0 1 0 0 1 0 1	$25	000011	000110	000011
0 0 1 0 0 1 1 0	$26	010001	010100	100001
0 0 1 0 0 1 1 1	$27	100001	100100	100001
0 0 1 0 1 0 0 0	$28	000100	001000	000011
0 0 1 0 1 0 0 1	$29	000110	001010	000011
0 0 1 0 1 0 1 0	$2A	010100	011000	100001
0 0 1 0 1 0 1 1	$2B	100100	101000	100001
0 0 1 0 1 1 0 0	$2C	001000	000100	000011
0 0 1 0 1 1 0 1	$2D	001010	000110	000011
0 0 1 0 1 1 1 0	$2E	011000	010100	100001
0 0 1 0 1 1 1 1	$2F	101000	100100	100001

APPLICATION CIRCUIT

1. ±5V SPLIT POWER SUPPLY



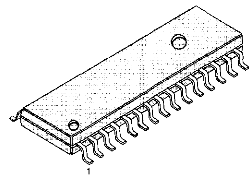
2. +5V SINGLE POWER SUPPLY



RF AMP FOR CDP

The KA9201 which is the RF amplifier is a monolithic integrated circuit designed for three-spot type optical pick-up of the compact disc player.
It is consisting of RF signal processing circuit, Focus Error AMP, Tracking Error AMP, Focus OK Detector, Mirror Detector, Defect Detector, EFM Comparator and automatic power controller for laser diode.

30 SOP



FEATURES

- **Functions: RF AMP**
  Focus Error AMP
  Tracking Error AMP
  Focus OK Detector
  Mirror Detector
  Defect Detector
  EFM (Eight to Fourteen Modulation) Comparator
  Automatic Asymmetry Control AMP
  Center Voltage Buffer
  APC (Automatic Power Control) AMP for Photo- Diode and Laser-Diode drive

ORDERING INFORMATION

Device	Package	Operating Temperature
KS9201D	30 SOP	$-25 \sim +75°C$

- **Single power supply operation (+5V) as well as split power supply operation (±5V)**
- **Low power consumption (100mW at ±5V, 50mW at +5V)**
- ***Built-in automaticpower controller use for P-sub and N-sub of the laser diode***
- **Minimum number of external components required**
- **Built-in disc defect detection circuit for improvement to play ability**
- **Recommend operation supply voltage range: $V_{CC}-V_{EE}$: 4~11V**
  $V_{CC}-D_{GND}$: 4~5.5V
- **Power Supply Condition:**

	V_{CC}	V_{EE}	V_C	V_R (V_{ref})	D_{GND}
Single Power Supply	Power Supply	GND	V_R	VC	GND
Split Power Supply	+Power Supply	−Power Supply	D_{GND}	No Connecting	GND

BLOCK DIAGRAM

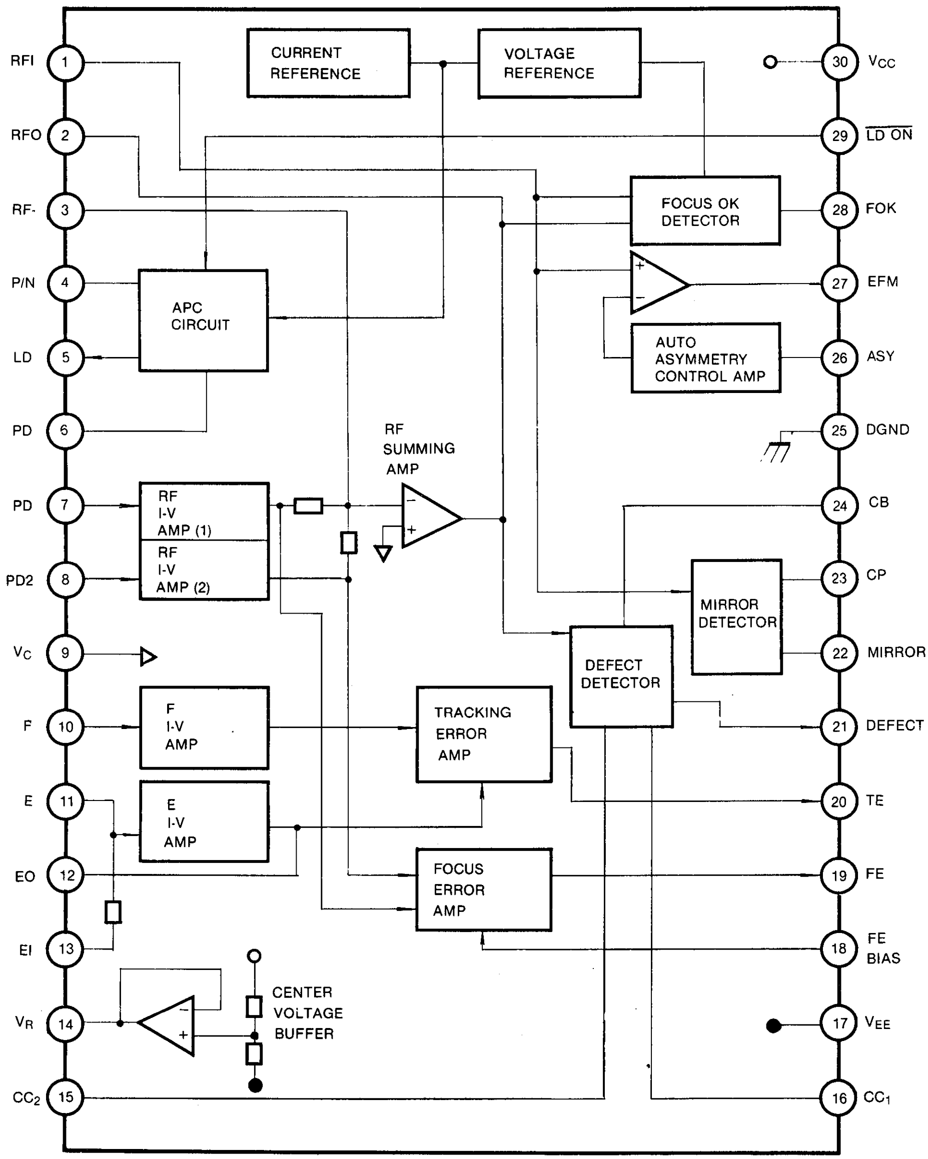


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	$V_{CC} - V_{EE}$	12	V
Power Dissipation	P_d	800	mW
Operating Temperature	T_{opr}	−25 ~ +75	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 2.5V, V_{EE} = D_{GND} = −2.5V, VC = GND, unless otherwise specified)

Stage	No	Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Current	1	V_{CC} Current	I_{CC}	DC Current	8.0	11.4	15.5	mA
	2	V_{EE} Current	I_{EE}		−15.0	−11.0	−7.5	mA
	3	D_{GND} Current	ID_{GND}		−1.1	−0.85	−0.6	mA
RF AMP	4	Offset Voltage	V_{RF}(offset)	DC voltage	−50	0	50	mV
	5	Voltage Gain	A_{VRF}	V_i = 2KHz, 40mV sinewave, Output; sinewave	25.1	28.1	31.1	dB
	6	Maximum Output Amplitude	V_{RFpp1}	V_i = 0.2V DC Output; +peak voltage	1.3			V
	7	Maximum Output Amplitude	V_{RFpp2}	V_i = −0.2V DC Output; −peak voltage			−0.3	V
Focus Error AMP	8	Offset Voltage	V_{FE}(offset)	DC voltage	−120		120	mV
	9	Voltage Gain	A_{VFE1}	V_i = 1KHz, 32mV sinewave, Output; sinewave	27	30	33	dB
	10	Voltage Gain	A_{VFE2}		27	30	33	dB
	11	Gain Unbalance	$\triangle A_{VFE}$		−3	0	3	dB
	12	Maximum Output Amplitude H	V_{FEpp1}	V_i = −0.2V DC Output; −peak voltage	1.9			V
	13	Maximum Output Amplitude L	V_{FEpp2}	V_i = 0.2V DC Output; −peak voltage			−1.9	V
Tracking Error AMP	14	Offset Voltage	V_{TE}(offset)	DC voltage	−50		50	mV
	15	Voltage Gain F	A_{VTE}(F)	V_i = 1KHz, 0.3V sinewave, input to output ratio Output; sinewave	7	10	13	dB
	16	Voltage Gain E	A_{VTE}(E)		7	10	13	dB
	17	Gain Unbalnce	$\triangle A_{VTE}$		−3	0	3	dB
	18	Maximum Output Amplitude H	V_{TEpp}(H)	V_i = 2.0V DC Output; +peak voltage	1.9			V
	19	Maximum Output Amplitude L	V_{TEpp}(L)	V_i = −2.0V DC Output; −peak voltage			−1.9	V

ELECTRICAL CHARACTERISTICS (Continued)

Stage	No	Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
APC AMP	20	Output Voltage 1	V_{APC1}	V_i = 190mV DC	1.4			V
	21	Output Voltage 2	V_{APC2}	V_i = 90mV DC			−1.4	V
	22	Output Voltage 3	V_{APC3}	V_i = 100mV DC	1.4			V
	23	Output Voltage 4	V_{APC4}	V_i = 170mV DC			−1.4	V
	24	Output Voltage 5	V_{APC5}	V_i = 0V DC	1.4			V
	25	Output Voltage 6	V_{APC6}	V_i = 0V DC			−1.4	V
	26	Maximum Output Amplitude H	V_{APCpp}(H)	Va = 0V, Ia = −0.8mA Output; +peak voltage	0			V
	27	Maximum Output Amplitude L	V_{APCpp}(L)	Va = 0.6V, Ia = 0.8mA Output; −peak voltage			0	V
Focus OK	28	Threshold Voltage	V_{FOK}(th)	V_i = output (V_{CC} + D_{GND})/2 must be adjusted by the DC voltage across RFI and RFO	−430	−390	−350	mV
	29	High Level Output Voltage	V_{FOK}(H)	Input across RFI and RFO 1V, 375mV(DC) sinewave, Output; pulse	2.2			V
	30	Low Level Output Voltage	V_{FOK}(L)				1.8	V
	31	Maximum Operating Frequency	f_{FOK}(max)		45			KHz
Mirror AMP	32	High Level Output Voltage	V_{MIR}(H)	V_i = 10KHz 0.8V, −0.4V(DC) sinewave, Output; pulse	1.8			V
	33	Low Level Output Voltage	V_{MIR}(L)				−2.2	V
	34	Mirror Hold Frequency Response	f_{MIR}(M)	V_i = 0.8V, 0.2V(DC), f(carrier) = 500KHz AM modulation Output; pulse		400	600	Hz
	35	Bottom Hold Frequency Response	f_{MIR}(B)	V_i = 0.8V, 0.4V(DC) sinewave, Output; pulse		500	900	Hz
	36	Maximum Input Operating Frequency	f_{MIR}(max)		30	70		KHz
	37	Minimum Input Operating Voltage	V_{MIR}(min)	V_i = 10KHz, 0.4V(DC) sinewave, Output; pulse		0.1	0.2	V
	38	Maximum Input Operating Voltage	V_{MIR}(max)		1.8			V
Defect AMP	39	High Level Output Voltage	V_{DEF}(H)	V_i = 32mV, +15mV(DC) sinewave, Output; pulse	1.8			V
	40	Low Level Output Voltage	V_{DEF}(L)				−2.2	V

ELECTRICAL CHARACTERISTICS (Continued)

Stage	No	Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Defect AMP	41	Minimum Input Operating Frequency	$f_{DEF}(min)$	$V_i = 32mV$, $+15mV(DC)$ sinewave, Output; pulse		670	1000	Hz
	42	Maximum Input Operating Frequency	$f_{DEF}(max)$		2.0	4.7		KHz
	43	Minimum Input Operating Voltage	$V_{DEF}(min)$	$V_i = 50Hz$, 15mV(DC) pulsewave, symmetry; 95% Output; pulse		0.3	0.5	V
	44	Maximum Input Operating Voltage	$V_{DEF}(max)$		1.8			V
EFM Comparator	45	Duty 1	D_{EFM1}	$V_i = 750KHz$, 0.7V sinewave, Output; DC voltage	−50	0	50	mV
	46	Duty 2	D_{EFM2}	$V_i = 750KHz$, 0.7V, +0.25V(DC) sinewave Output; DC voltage	0	50	100	mV
	47	High Level Output Voltage	$V_{EFM}(H)$	$V_i = 750KHz$, 0.7V sinewave Output; pulse	1.2			V
	48	Low Level Output Voltage	$V_{EFM}(L)$				−1.2	V
	49	Minimum Input Operating Voltage	$V_{EFM}(min)$	$V_i = 750KHz$ sinewave Output; pulse			0.12	V
	50	Maximum Input Operating Voltage	$V_{EFM}(max)$		1.8			V
	51	Maximum Input Operating Frequency	$f_{EFM}(max)$	$V_i = 750KHz$, 0.7V sinewave, Output; pulse	4.0			MHz
Center Voltage Buffer	52	Offset Voltage	$V_{CV}(offset)$	DC voltage	−100	0	100	mV
	53	Maximum Output Current (+)	$I_{CVpp}(+)$		5			mA
	54	Maximum Output Current (−)	$I_{CVpp}(-)$				−5	mA
($Ta = 25°C$, $V_{CC} = 5.0V$, $V_{EE} = -5.0V$, $D_{GND} = VC = GND$, unless otherwise specified)								
RF AMP	55	Maximum Output Amplitude (H)	$V_{RFpp}(H)$	$V_i = 0.2V$ DC Output; DC voltage	3.5			V
	56	Maximum Output Amplitude (L)	$V_{RFpp}(L)$	$V_i = -0.2V$ DC Output; DC voltage			0.3	V
Focus Error AMP	57	Maximum Output Amplitude (H)	$V_{RFpp}(H)$	$V_i = -0.2V$ DC Output; DC voltage	4.2			V
	58	Maximum Output Amplitude (L)	$V_{RFpp}(L)$	$V_i = 0.2V$ DC Output; DC voltage			−2.2	V
Tracking Error AMP	59	Maximum Output Amplitude (H)	$V_{TEpp}(H)$	$V_i = 2.0V$ DC Output; DC voltage	4.2			V
	60	Maximum Output Amplitude (L)	$V_{TEpp}(L)$	$V_i = -2.0V$ DC Output; DC voltage			−2.2	V

ELECTRICAL CHARACTERISTICS (Continued)

Stage	No	Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
APC AMP	61	Output Voltage 7	V_{APC7}	V_i = 190mV DC Output DC voltage	1.4			V
	62	Output Voltage 8	V_{APC8}	V_i = 90mV DC Output DC voltage			−1.4	V
	63	Output Voltage 9	V_{APC9}	V_i = 100mV DC Output DC voltage	1.4			V
	64	Output Voltage 10	V_{APC10}	V_i = 170mV DC Output DC voltage			−1.4	V
	65	Output Voltage 11	V_{APC11}	V_i = 0V DC Output DC voltage	3.8			V
	66	Output Voltage 12	V_{APC12}	V_i = 190mV DC Output DC voltage			−3.8	V
	67	Maximum Output Amplitude H	V_{APC}(H)	Va = 0V DC, Ia = −0.8mA Output; DC voltage	2.5			V
	68	Maximum Output Amplitude L	V_{APC}(L)	Va = 0.6V DC, Ia = 0.8mA Output; DC voltage			−2.5	V
Focus OK AMP	69	Threshold	V_{FOK}(th)	Input DC voltage; output (V_{CC} + D_{GND})/2 must be adjusted by the DC voltage across RFI and RFO	−430	−390	−350	mV
	70	High Level Output Voltage	V_{FOK}(H)	V_i = 1V, −375mV(DC) across RFI and RFO; sinewave, Output; pulse	4.7			V
	71	Low Level Output Voltage	V_{FOK}(L)				0.7	V
Mirror AMP	72	High Level Output Voltage	V_{MIR}(H)	V_i = 10KHz 0.8V, −0.4V(DC) sinewave, Output; pulse	4.3			V
	73	Low Level Output Voltage	V_{MIR}(L)				0.3	V
Defect AMP	74	High Level Output Voltage	V_{DEF}(H)	V_i = 1KHz 32mV, +15mV(DC) sinewave, Output; pulse	4.3			V
	75	Low Level Output Voltage	V_{DEF}(L)				−0.3	V
EFM Comparator	76	Duty 3	D_{EFM3}	V_i = 750KHz 0.7V sinewave Output; DC voltage	2.45	2.50	2.55	V
	77	Duty 4	D_{EFM4}	V_i = 750KHz 0.7V, +0.25V(DC) sinewave Output; pulse	2.50	2.55	2.60	V
	78	High Level Output Voltage	V_{EFM}(H)	V_i = 750KHz 0.7V, sinewave, Output; pulse	3.7			V
	79	Low Level Output Voltage	V_{EFM}(L)				1.3	V

TEST CIRCUIT

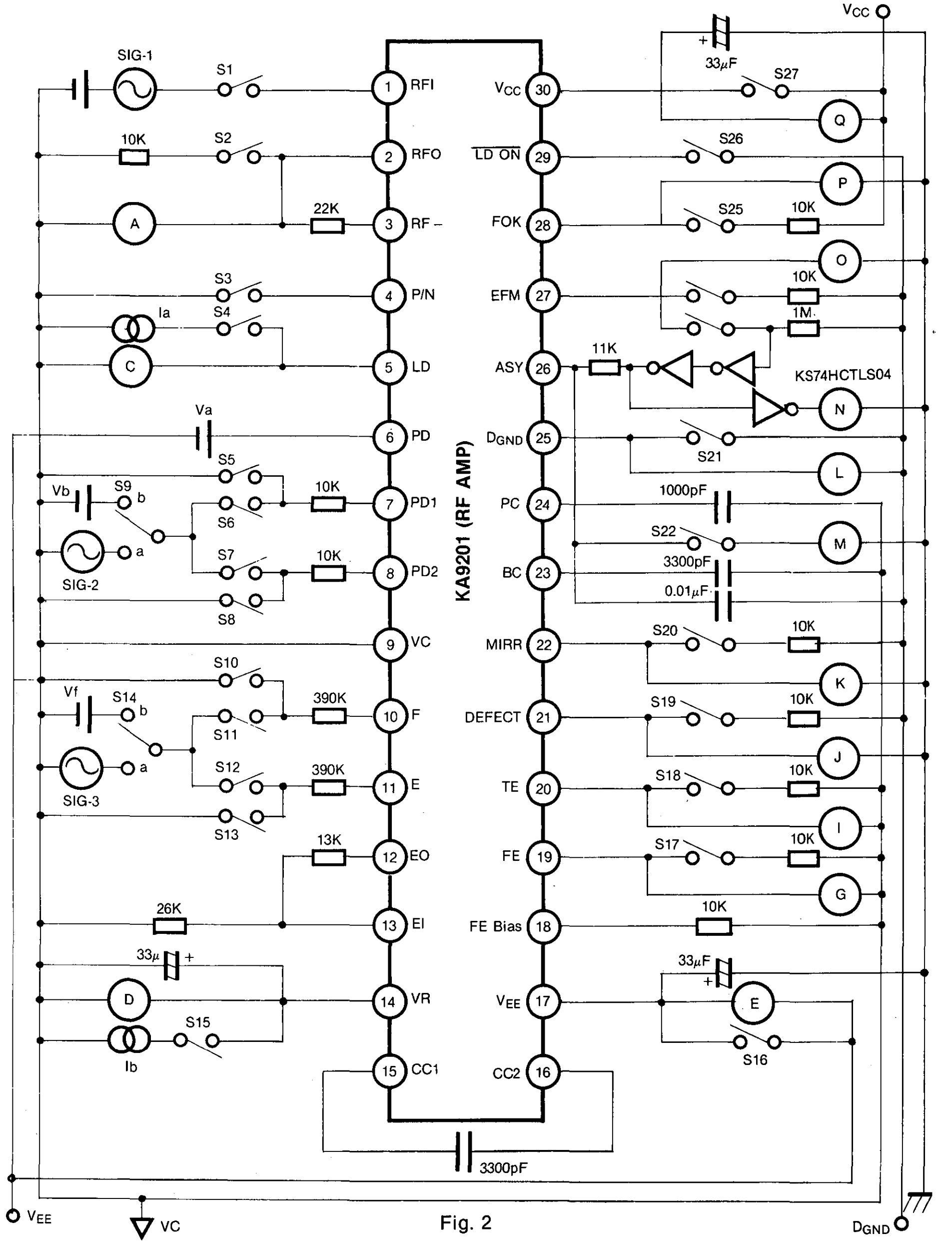


Fig. 2

*) Note: KS74HCTLS04: Supply Voltage = 5V

TEST METHODE (SWITCH CONDITION) (V_{CC} = 2.5V, V_{EE} = D_{GND} = −2.5V, V_C = GND)

Stage	No	Characteristic	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	S21	S22	S23	S24	S25	S26	S27	Input	Test Point
Power Supply Current	1	I_{CC}			ON													ON	ON	ON	ON	ON	ON				ON	ON		—	Q
	2	I_{EE}			ON														ON	ON	ON	ON	ON				ON	ON	ON	—	E
	3	ID_{GND}																ON	ON	ON	ON	ON					ON		ON	—	L
RF AMP	4	V_{RF}(offset)			ON													ON					ON					ON	ON	—	A
	5	Av_{RF}						ON	ON									ON					ON						ON	SIG-2	A
	6	V_{RFpp1}		ON				ON	ON		b							ON					ON						ON	V_b	A
	7	VRF_{pp2}		ON				ON	ON		b							ON					ON						ON	V_b	A
Focus Error AMP	8	V_{FE}(offset)																ON					ON					ON	ON	—	G
	9	Av_{FE1}						ON		ON	a							ON					ON						ON	SIG-2	G
	10	Av_{FE2}					ON		ON		a							ON					ON						ON	SIG-2	G
	11	Av_{FE}																													
	12	V_{FEpp1}						ON		ON	b							ON	ON				ON						ON	V_b	G
	13	V_{FEpp2}						ON		ON	b							ON	ON				ON						ON	V_b	G
Tracking Error AMP	14	V_{TE}(offset)			ON													ON					ON					ON	ON	—	I
	15	Av_{TE}(F)											ON		ON	a		ON					ON						ON	SIG-3	I
	16	Av_{TE}(E)										ON		ON		a		ON					ON						ON	SIG-3	I
	17	Av_{TE}																													
	18	V_{TEpp}(H)											ON		ON	b		ON		ON			ON						ON	Vt	I
	19	A_{TEpp}(L)											ON		ON	b		ON		ON			ON						ON	Vt	I
APC AMP	20	V_{APC1}																ON					ON					ON	ON	Va	C
	21	V_{APC2}																ON					ON					ON	ON	Va	C
	22	V_{APC3}			ON													ON					ON					ON	ON	Va	C
	23	V_{APC4}			ON													ON					ON					ON	ON	Va	C
	24	V_{APC5}																ON					ON						ON	Va	C
	25	V_{APC6}			ON													ON					ON						ON	Va	C
	26	V_{APCpp}(H)			ON	ON												ON					ON					ON	ON	Va, Ia	C
	27	V_{APCpp}(L)			ON	ON												ON					ON					ON	ON	Va, Ia	C
Focus OK AMP	28	V_{FOK}(th)	ON															ON					ON				ON		ON	SIG-1	P
	29	V_{FOK}(H)	ON															ON					ON				ON		ON	SIG-1	P
	30	V_{FOK}(L)	ON															ON					ON				ON		ON	SIG-1	P
	31	t_{FOK}(max)	ON															ON					ON				ON		ON	SIG-1	P
Mirror AMP	32	V_{MIR}(H)	ON															ON				ON	ON						ON	SIG-1	K
	33	V_{MIR}(L)	ON															ON				ON	ON						ON	SIG-1	K
	34	f_{MIR}(M)	ON															ON				ON	ON						ON	SIG-1	K
	35	f_{MIR}(B)	ON															ON				ON	ON						ON	SIG-1	K
	36	f_{MIR}(max)	ON															ON				ON	ON						ON	SIG-1	K
	37	V_{MIR}(min)	ON															ON				ON	ON						ON	SIG-1	K
	38	V_{MIR}(max)	ON															ON				ON	ON						ON	SIG-1	K

TEST METHODE (SWITCH CONDITION) (Continued)

Stage	No	Characteristic	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	S21	S22	S23	S24	S25	S26	S27	Input	Test Point
Defect AMP	39	V_{DEF}(H)						ON	ON		a							ON			ON		ON						ON	SIG-2	J
	40	V_{DEF}(L)						ON	ON		a							ON			ON		ON						ON	SIG-2	J
	41	t_{DEF}(min)						ON	ON		a							ON			ON		ON						ON	SIG-2	J
	42	t_{DEF}(max)						ON	ON		a							ON			ON		ON						ON	SIG-2	J
	43	V_{DEF}(min)						ON	ON		a							ON			ON		ON						ON	SIG-2	J
	44	V_{DEF}(max)						ON	ON		a							ON			ON		ON						ON	SIG-2	J
EFM Comparator	45	D_{EFM1}	ON		ON													ON					ON	ON	ON				ON	SIG-1	M
	46	D_{EFM2}	ON		ON													ON					ON	ON	ON				ON	SIG-1	M
	47	V_{EFM}(H)	ON															ON					ON		ON	ON			ON	SIG-1	O
	48	V_{EFM}(L)	ON															ON					ON		ON	ON			ON	SIG-1	O
	49	V_{EFM}(min)	ON															ON					ON	ON					ON	SIG-1	N
	50	V_{EFM}(max)	ON															ON					ON	ON					ON	SIG-1	N
	51	t_{EFM}(max)	ON															ON					ON	ON					ON	SIG-1	N
Center Voltage Buffer	52	V_{CV}(offset)			ON													ON					ON						ON	—	D
	53	$I_{CVpp(+)}$			ON												ON	ON					ON						ON	Ib	D
	54	$I_{CVpp(-)}$			ON												ON	ON					ON						ON	Ib	D
($V_{CC}=5.0V$, $V_{EE}=-5.0V$, $D_{GND}=V_C=GND$)																															
RF AMP	55	V_{RFpp}(H)		ON				ON	ON		b							ON					ON						ON	Vb	A
	56	V_{RFpp}(L)		ON				ON	ON		b							ON					ON						ON	Vb	A
Focus Error AMP	57	V_{FEpp}(H)						ON		ON	b							ON	ON				ON						ON	Vb	G
	58	V_{FEpp}(L)						ON		ON	b							ON	ON				ON						ON	Vb	G
Tracking Error AMP	59	V_{TEpp}(H)											ON		ON	b		ON		ON			ON						ON	Vt	I
	60	V_{TEpp}(L)											ON		ON	b		ON		ON			ON						ON	Vt	I
APC AMP	61	V_{APC7}																ON					ON					ON	ON	Va	C
	62	V_{APC8}																ON					ON					ON	ON	Va	C
	63	V_{APC9}			ON													ON					ON					ON	ON	Va	C
	64	V_{APC10}			ON													ON					ON					ON	ON	Va	C
	65	V_{APC11}																ON					ON						ON	Va	C
	66	V_{APC12}			ON													ON					ON						ON	Va	C
	67	V_{APCpp}(H)			ON	ON												ON					ON					ON	ON	Va, Ia	C
	68	V_{APCpp}(L)			ON	ON												ON					ON					ON	ON	Va, Ia	C
Focus OK AMP	69	V_{FOK}(thres)	ON															ON					ON				ON		ON	SIG-1	P
	70	V_{FOK}(K)	ON															ON					ON				ON		ON	SIG-1	P
	71	V_{FOK}(L)	ON															ON					ON				ON		ON	SIG-1	P
Mirror AMP	72	V_{MIR}(H)	ON															ON				ON	ON						ON	SIG-1	K
	73	V_{MIR}(L)	ON															ON				ON	ON						ON	SIG-1	K
Defect AMP	74	V_{DEF}(H)						ON	ON		a							ON			ON		ON						ON	SIG-2	J
	75	V_{DEF}(L)						ON	ON		a							ON			ON		ON						ON	SIG-2	J
EFM Comparator	76	D_{EFM3}	ON		ON													ON					ON	ON	ON				ON	SIG-1	M
	77	D_{EFM4}	ON		ON													ON					ON	ON	ON				ON	SIG-1	M
	78	V_{EFM}(H)	ON															ON					ON		ON	ON			ON	SIG-1	O
	79	V_{EFM}(L)	ON															ON					ON		ON	ON			ON	SIG-1	O

APPLICATION NOTE

1. Description

The KA9201 is a RF amplifier for compact disc player. It is designed for 3-spot type optical pick-up assembly. The photo detector is composited of 6 light sensor (A through F). The photo detector A, B, C and D detectors for detecting audio modulation on the disc and also utilizing to develop focus error signal, the E and F photo detectors to detecting of tracking error signal.

2. Operating Theory

1) RF AMP

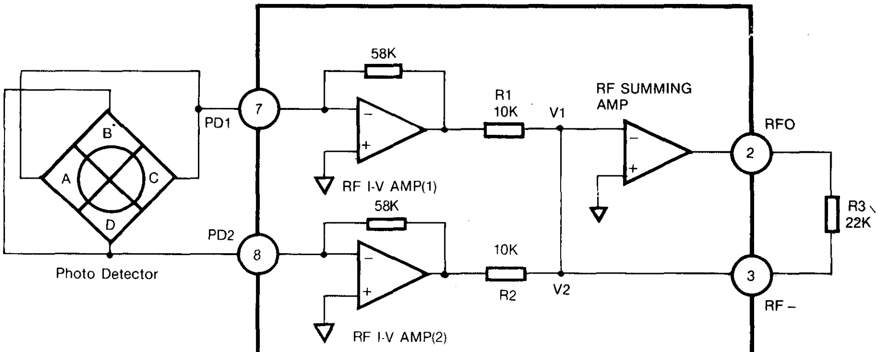
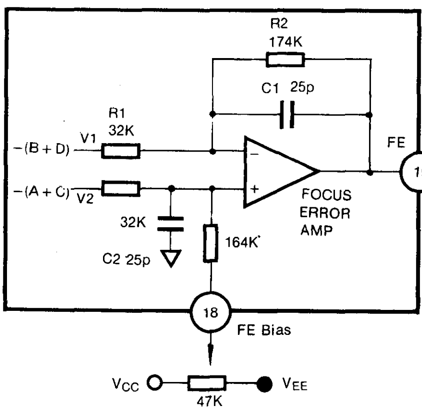


Fig. 3

RF I-V AMP(1) and RF I-V AMP(2) are converted into voltage from current signal of PD1(A + C) and PD2(B + D) through the 58Kohm internal resistor. Furthermore, it is added in RF summing amplifier, this signal (A + B + C + D) is output at RFO (pin 2). The RF output voltage (low frequency) is as follow.

$$
\begin{aligned}
V_{RF} &= -R3^* (iPD1 + iPD2) \\
&= -R3^* (V1/R1 + V2/R2) \\
&= -22K^* (V1/10K + V2/10K) \\
&= -2.2^* (V1 + V2)
\end{aligned}
$$

2) Focus Erros AMP



The Focus Error AMP is the difference between RF I-V AMP(1) output (A + C) and RF I-V AMP(2) output (B + D). This two [– (A + C), – (B + D)] signals are each applied to the (–) and (+) input of Focus Error AMP.

As the result of differential voltage, Focus Error signal is appeared at FE pin (pin 19).

This FE output voltage (low frequency) become [(A + C) – (B + D)], as follow.

$$
\begin{aligned}
V_{FE} &= R2/R1^*(V2 - V1) \\
&= 5.4\ (V2 - V1)
\end{aligned}
$$

The focus error voltage is directed to the focus servo circuit, to maintain optimum focusing at all times.

3) Tracking Error AMP

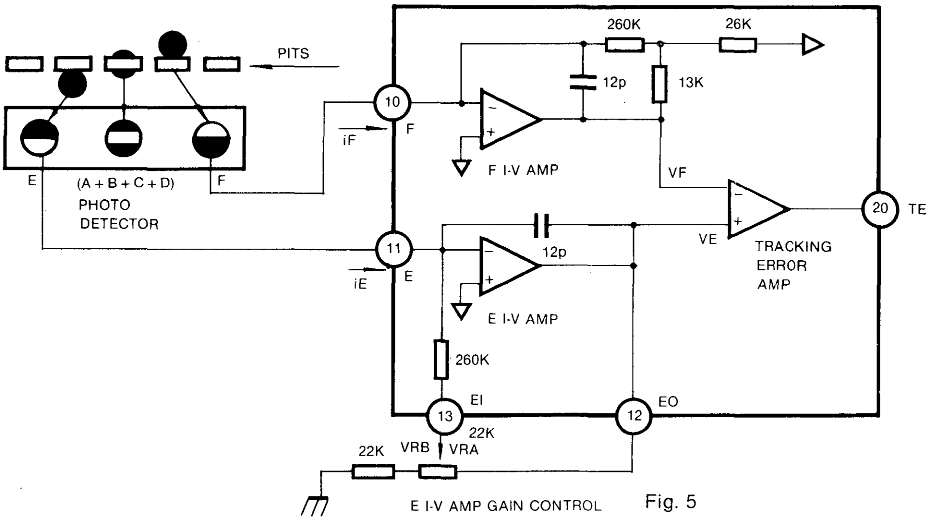


Fig. 5

The output of photo detector F is directed to the (−) input of F I-V amp, and output of photo detector E is directed to the (−) input of F I-V amp. These input signals are current. E I-V AMP and F I-V AMP are converted into voltage from the current signal. When correct tracking, two input (VF, VE) signals are equal. The occurence of tracking error is due to difference between F I-V amp output and E I-V amp output, and the TE output voltage is as follow.

$VF = iF*[(260K*13K/26K) + 273K]$
$= iF*403K$
$VE = iE*[260K*(VRA/VRB + 22K) + (VRA + 260K)]$
accordingly, $V_{TE} = (iE - iF)*1290K$

4) Focus OK Circuit

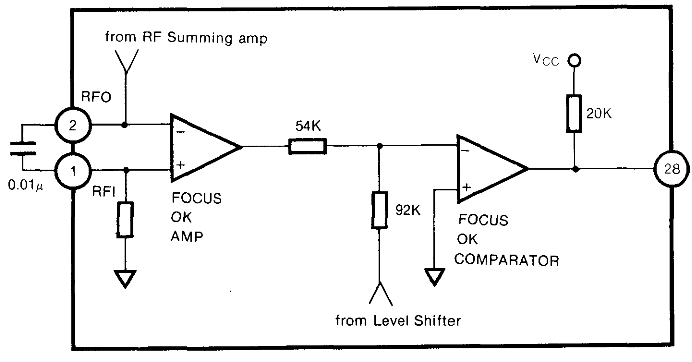


Fig. 6

The focus OK circuit generates a timing window to look on the focus servo at focus search status. When RFO (Pin 2) voltage is more than −0.37 volt, the focus amp output is inverted. The RFI pin (Pin 1) will get the HPF output from a RF signal of RFO (Pin 2), and the Pin 2 is LPF output opposite for focus OK amplifier output. Time constants of HPF in EFM comparator and in mirror circuit, and that of LPF in focus OK amp are determined by the capacitor (0.01μ) between RFI and RFO.
In case of 0.01μF, cut-off frequency will be 1KHz. This capacitor reduce error due to damaged RF envelop result from the scratched disc, and so on.

5) Mirror Circuit

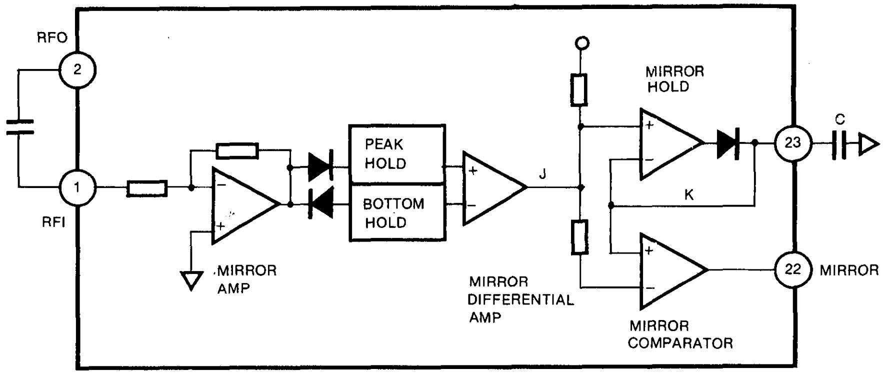


Fig. 7

After RF input signal is amplified by Mirror Amp, it is held in Bottom & Peak hold circuit. Such a hold is determined by the time constant. Envelop signal J (demodulated to DC) is two-thirds of the peak value of this signal the time constant of J signal is held when it is larger than that of K signal. Therefore, mirror output is; Low at track on disc, High at between tracks on disc, High when defect is detected. The time constant of mirror hold required to be larger enough than that of traverse signal traverse signal.

6) EFM (Eight to Fourteen) Comparator

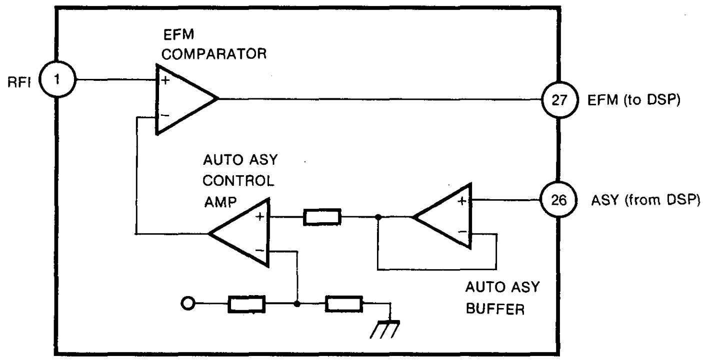


Fig. 8

The EFM comparator convert a RF signal to a binary signal. A processing of disc production be occured disproportion because by modification of disc, that is not reduced by only AC coupling. The reference voltage of EFM comparator is controlled utilizing the fact that the generation-probability 1, 0 is 50%. In the binary EFM signal,
As this comparator is a current switching type, each of the high and low levels are differention feedback through power supply and C-MOS buffer. R1, R2, C1 and C2 is for get (V_{CC} + D_{GND})/2 Volt. When the cut-off frequency is larger than 500Hz, EFM low frequency may be deterioration, and black error rate may be bad.

7) Defect Circuit

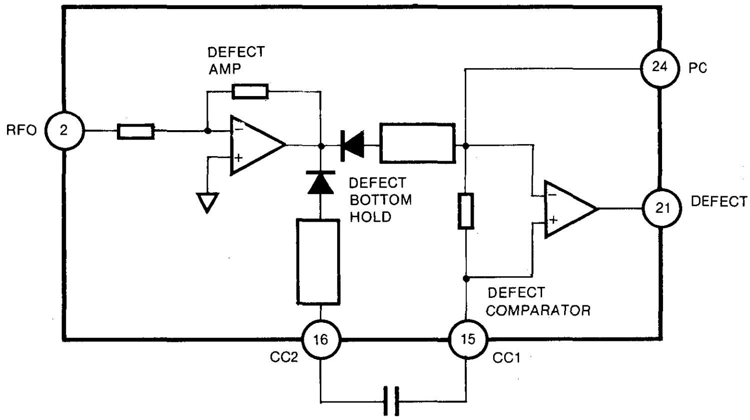


Fig. 9

The bottom hold has had two time constant of long and short, after than the RFI signal inverted. The short time constant of bottom hold is generated by shoter than 0.1msec of disc mirror defect, and long time constant is generated by previous mirror level. Mirror defect detection signals are generated by differentiate on capacitor coupling and then transfor level.

8) APC (Automatic Power Control) Circuit

As the laser diode has had large negative temperature characteristic when do something for regularly supply current on laser diode. Therefore, the output on processing monitor photo diode, must be a controlled current for get regularly output power. Thus APC circuit composed, this circuit use for P-sub and N-sub of laser diode, single power supply operation as well as split power supply operation.

(1) +5V Single Power Supply P-sub Laser

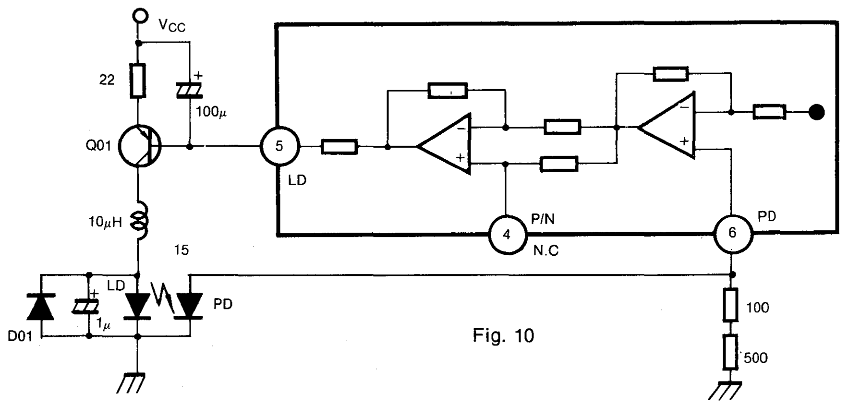


Fig. 10

4

(2) −5V Single Power Supply N-sub Laser

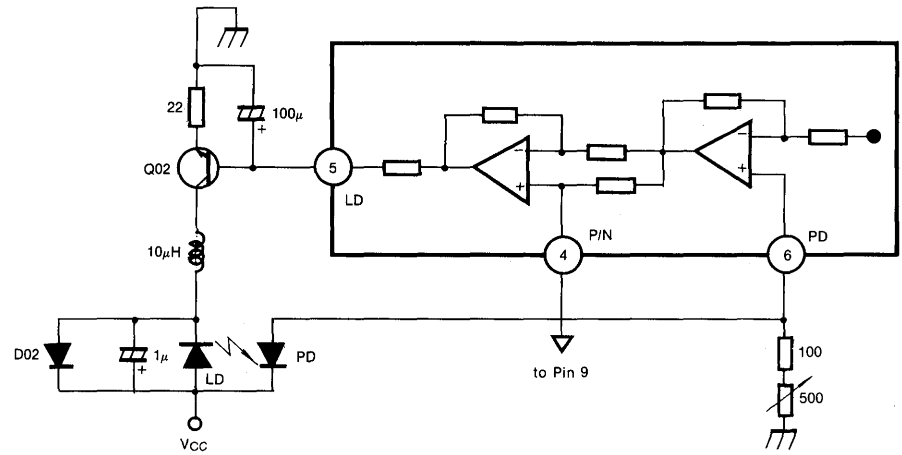


Fig. 11

(3) ±5V Split Power Supply P-sub Laser

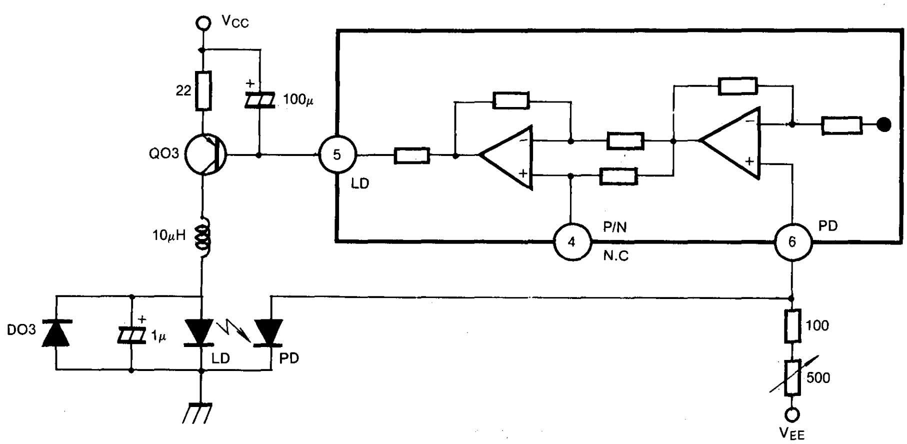


Fig. 12

(4) ±5V Split Power Supply N-sub Laser

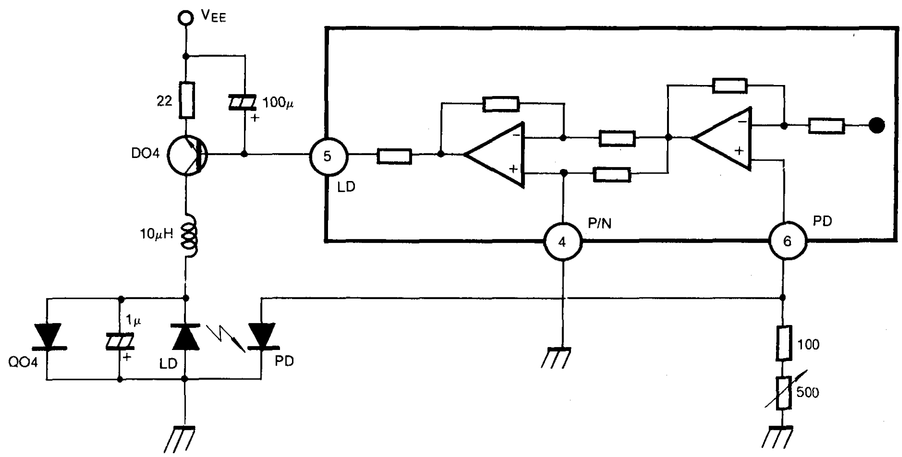


Fig. 13

(5) Voltage Reference Circuit

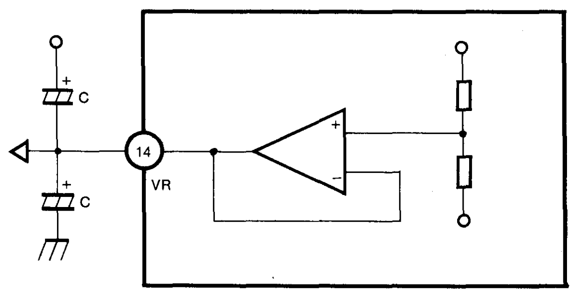


Fig. 14

This circuit generates a center voltage when the KA9201 and KA8309 is driven with a +5V single power supply. The motor or acturator is no connected when the maximum current output current is approximatly ±5mA.

APPLICATION CIRCUIT

1) +5V Single Power Supply for P-sub Laser Diode

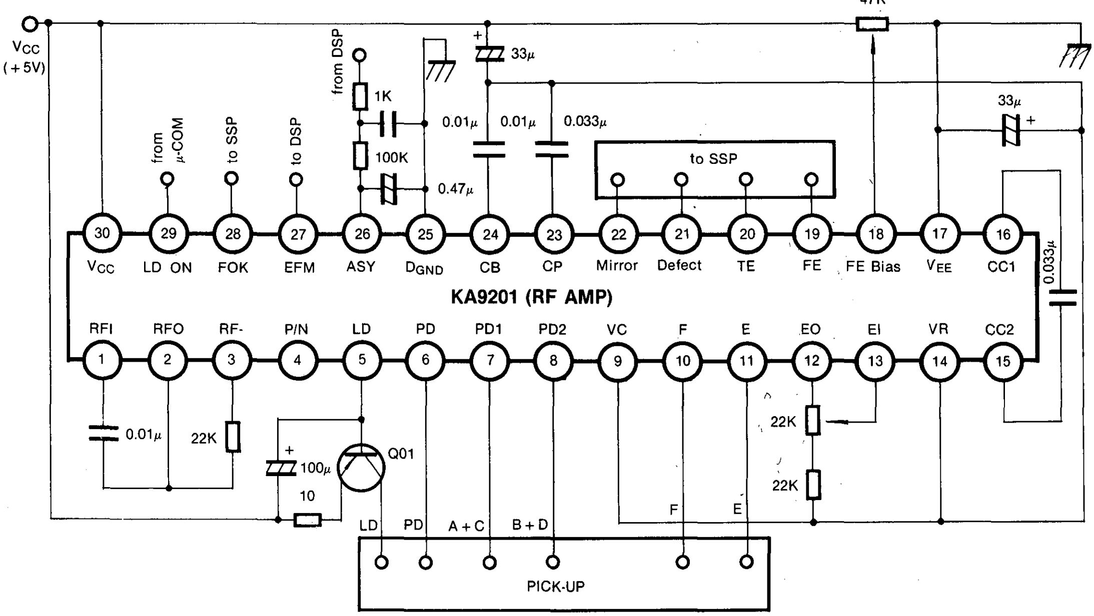


Fig. 15

2) +5V Single Power Supply for N-sub Laser Diode

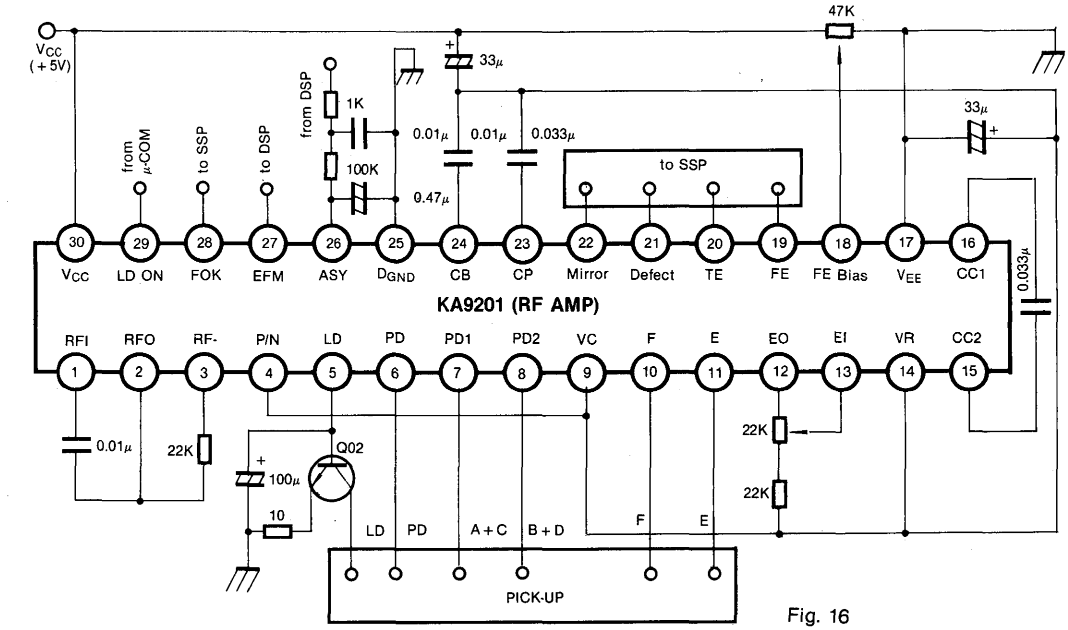


Fig. 16

APPLICATION CIRCUIT

3) ±5V Split Power Supply for P-sub Laser Diode

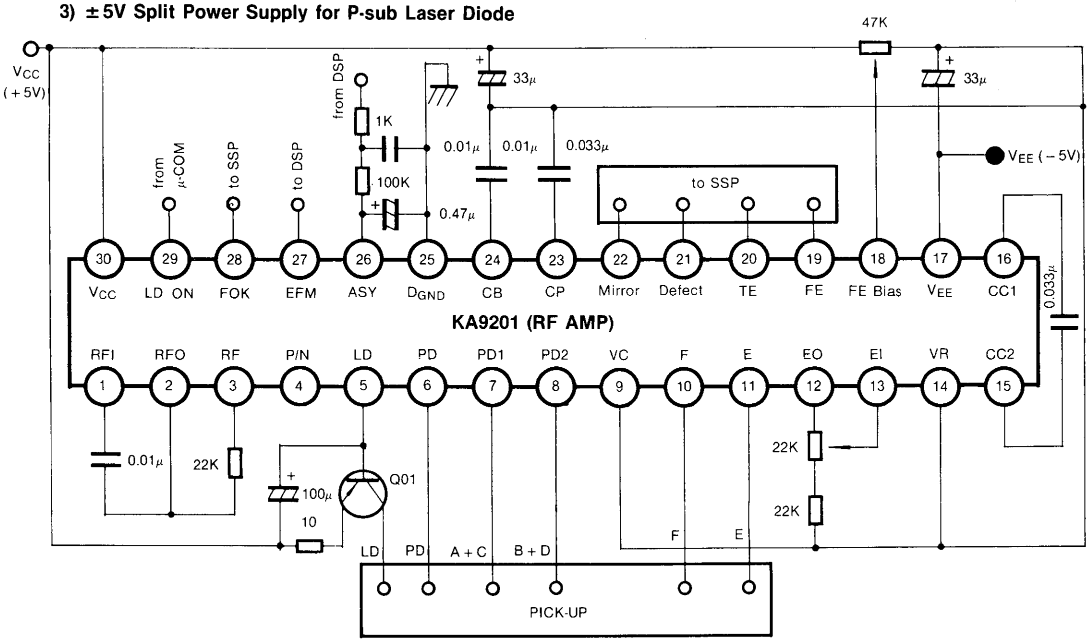


Fig. 17

4) ±5V Split Power Supply for N-sub Laser Diode

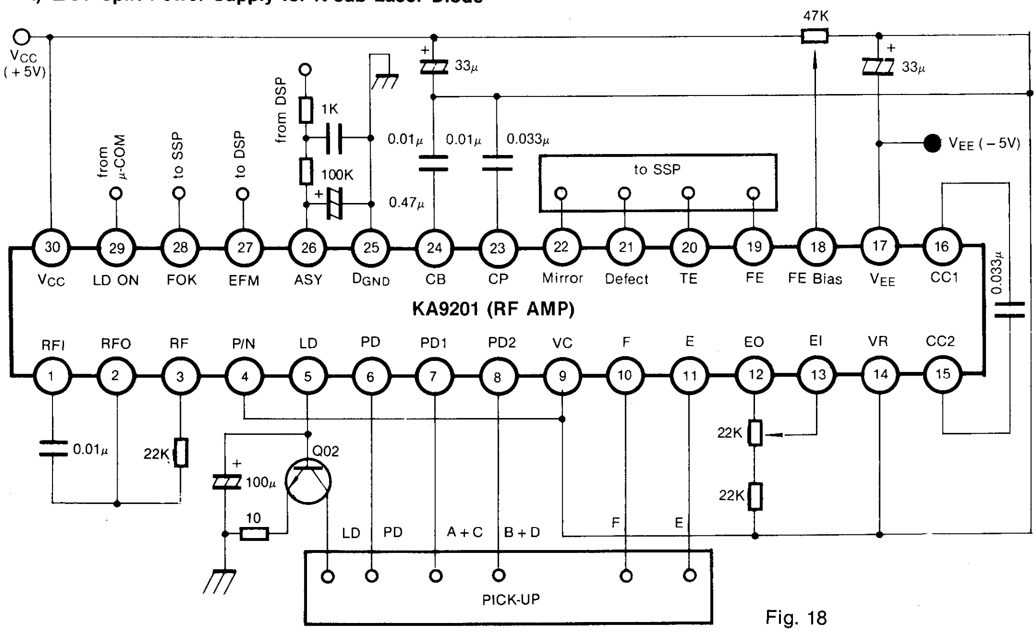
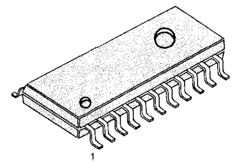


Fig. 18

PWM MOTOR DRIVER

The KA9255, a monolithic integrated circuit, is a dual pulse width modulation (PWM) driver.
It is designed for potable compact disk players, and is capable of driving sled and spindle motor.

22 SOP



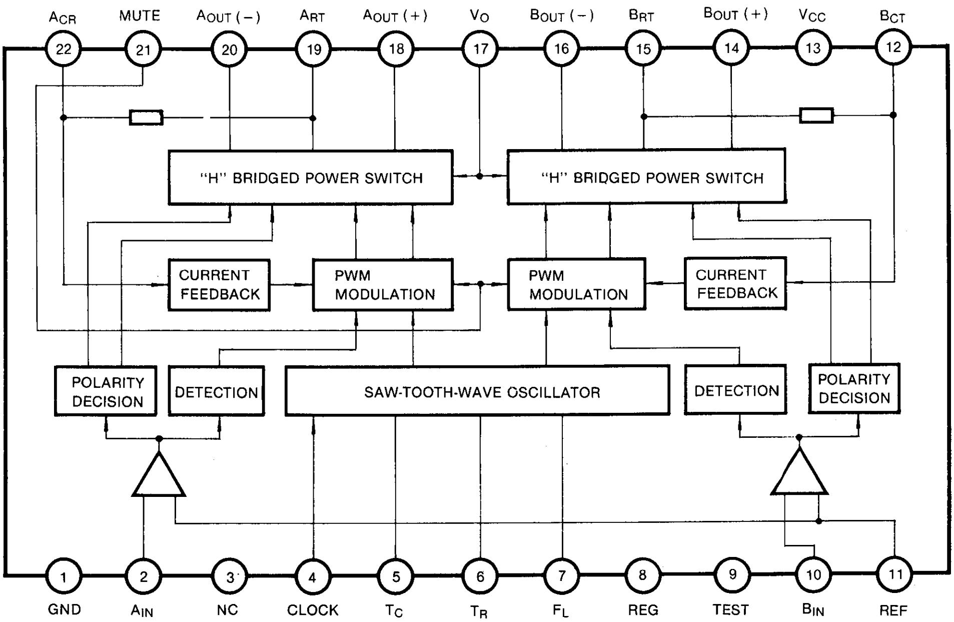
FEATURES

- 2 channel PWM driver
- Maximum output current is 0.5A
- Wide operating supply voltage range (3.5V to 12V)
- Capability of controlling modulation index
- The servo loop gain stabilized by a current feed back loop
- Internal thermal overload protection
- 22 SOP type package

ORDERING INFORMATION

Device	Package	Operating Temperature
KA9255D	22 SOP	−25~ +75°C

BLOCK DIAGRAM



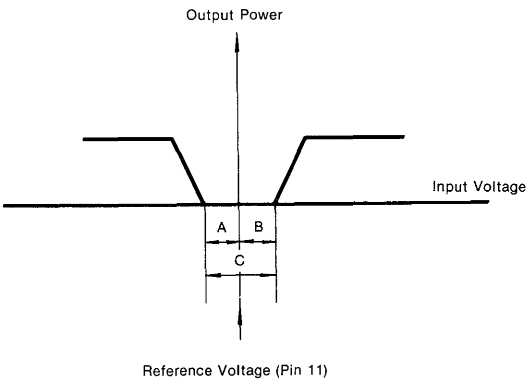
ABSOLUTE MAXIMUM RATING (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	12	V
	V_D	12	V
Output Current	I_O	0.5	A
Power Dissipation	P_D	550	mW
Operating Temperature	T_{opr}	− 25 ~ + 75	°C
Storage Temperature	T_{stg}	− 55 ~ + 125	°C

ELECTRICAL CHARACTERISTIC

(Ta = 25°C, V_{CC} = 5.0V, V_D = 9V, V_B = 1/2 V_{CC})

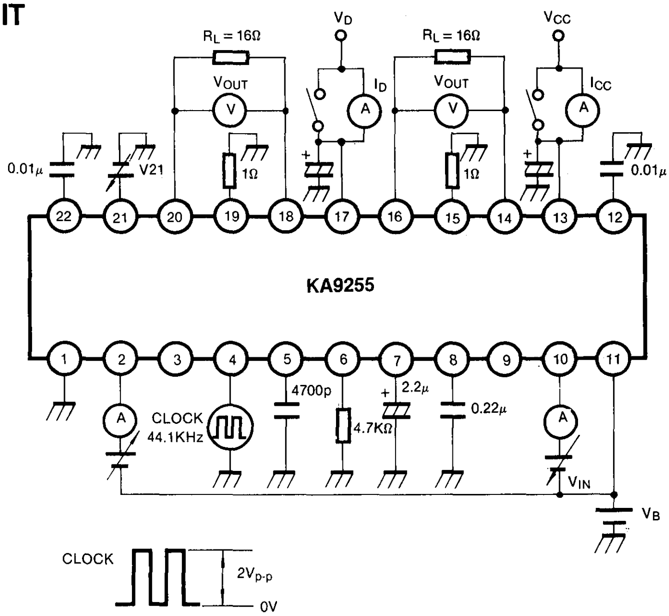
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Current (Control Stage)	I_{CC}	V_{IN} = 0V	8.5	18	24	mA
Quiescent Current (Output Stage)	I_D	V_{IN} = 0V	80	240	500	μA
Output Saturation Voltage	V_{sat}	R_L = 16Ω, V_{IN} = 1.5V		2.1	3.0	V
Input vs. Output Pulse Width	W_{IN}	V_{IN} = 1V, V_{21} = V_{CC}	2.7	5.0	7.3	μsec
Input Deadband Offset	$V_{th\ IN}$	See the figure below	20	80	150	mV
Input Deadband Width Offset	$V_{off\ IN}$	See the figure below	− 50	0	+ 50	mV
Input Resistance	R_{IN}	V_{IN} = 1V	10.8	15.5	20.2	KΩ
Clock Threshold Voltage	V_{tc}	V_{IN} = 1V	0.56	0.64	0.72	V
Muting Pin Voltage to Output Pulse Width	W_M	V_{IN} = 1.5V, V_{21} = 0.5V	2.0	3.8	5.6	μsec



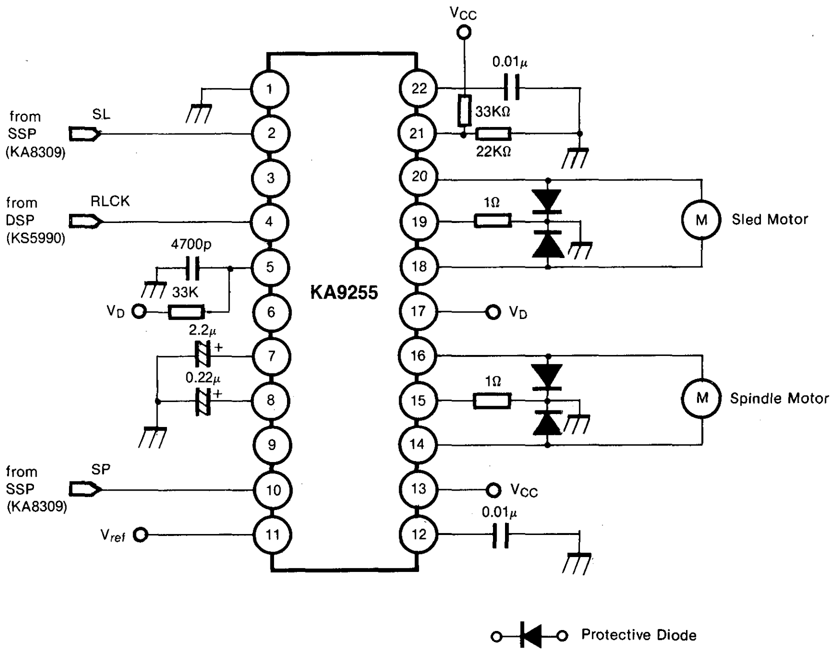
A; Negative input deadband width
B; Positive input deadband width
C; Input deadband width

$V_{th\ IN}$ = abs(A) + abs(B) = C
$V_{off\ IN}$ = (abs(B) − abs(A)) × 1/2

TEST CIRCUIT



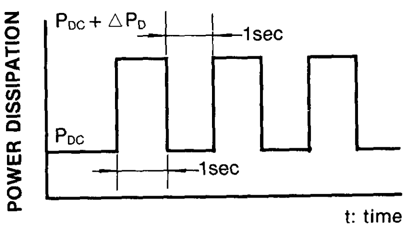
APPLICATION CIRCUIT



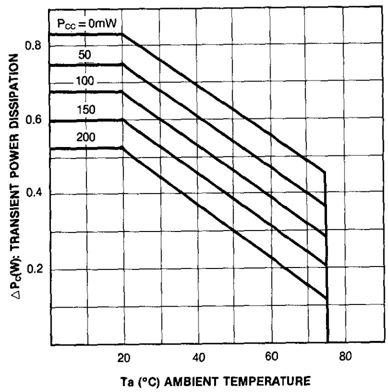
Allowable Power Dissipation

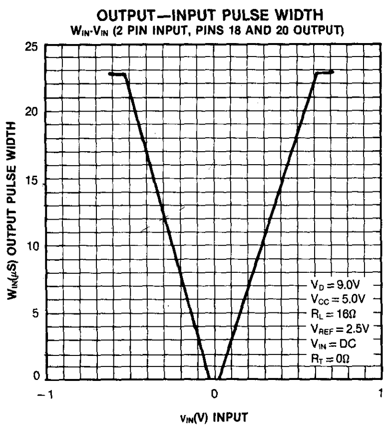
When internal power is consumed intermittently, the allowable power dissipation is the value corresponding to the power application condition.
The figure below shows an example of the heat reduction curve when the $\triangle P_D$ power is repeatedly applied three times in one second width and at one second interval while the P_{DC} power consumption is consistent.

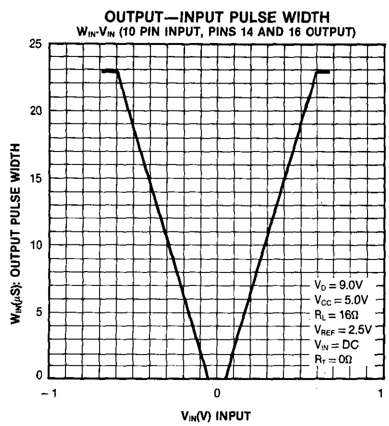
(When 50mm × 50mm, t = 1.6mm glass epoxy circuit board is mounted.)



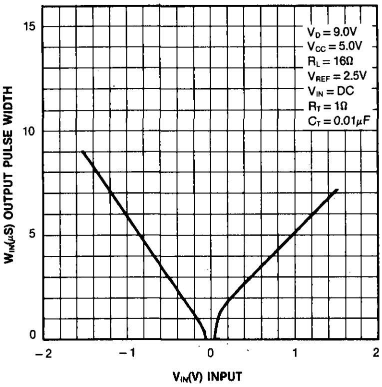
P_{DC}: Constant internal power consumption
$\triangle P_D$: internal transient power consumption



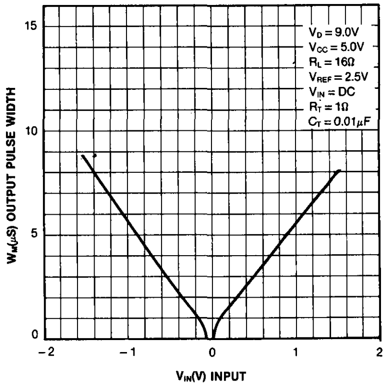




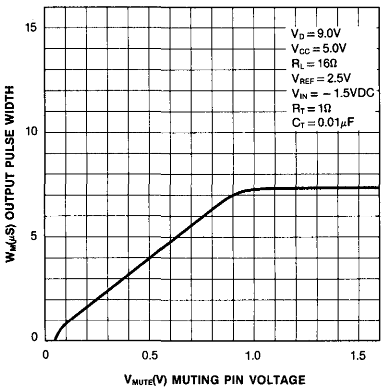
OUTPUT—INPUT PULSE WIDTH
W_{IN}-V_{IN} (10 PIN INPUT, PINS 14 AND 16 OUTPUT)



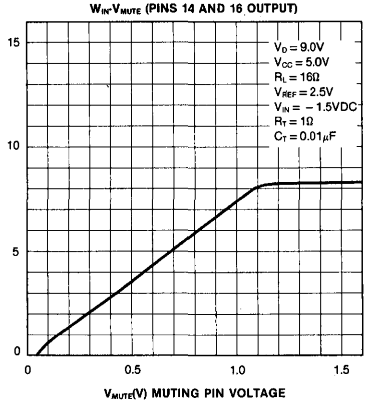
OUTPUT—INPUT PULSE WIDTH
W_{IN}-V_{IN} (2 PIN INPUT, PINS 18 AND 20 OUTPUT)



OUTPUT PULSE WIDTH—MUTING PIN VOLTAGE
W_{IN}-V_{MUTE} (PINS 18 AND 20 OUTPUT)



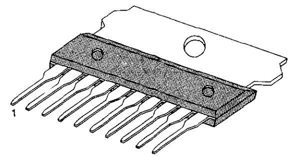
OUTPUT PULSE WIDTH—MUTING PIN VOLTAGE
W_{IN}-V_{MUTE} (PINS 14 AND 16 OUTPUT)



DUAL POWER OPERATIONAL AMPLIFIER

The KA9256 is a dual power operational amplifier and its output maximum current is 1.0A ($V_S = \pm 15V$). It can be used in arm driver for player, driver for brush motors forward and reverse rotation control and output driver for hole motor.

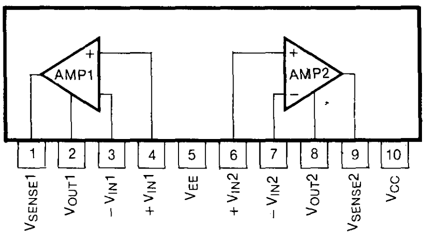
10 SIP H/S



FEATURES

- **Interal current limiting: $I_{SC} = 350mA$ ($R_{SC} = 2.2$)**
- **High output current: $I_O = 500mA$ max**
- **10 SIP H/S package**
- **Internal phase compensation type**

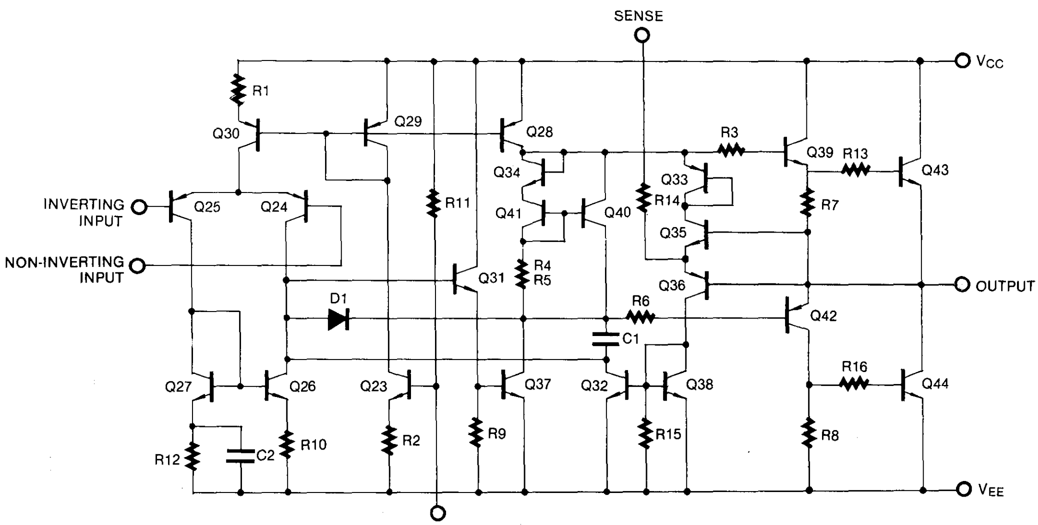
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
KA9256	10 SIP H/S	$-25 \sim +75°C$

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_S	±8	V
Output Current	I_O	1.0	A
Power Dissipation	P_D	12.5	W
Operating Temperature Range	T_{opr}	−25 ~ +75	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

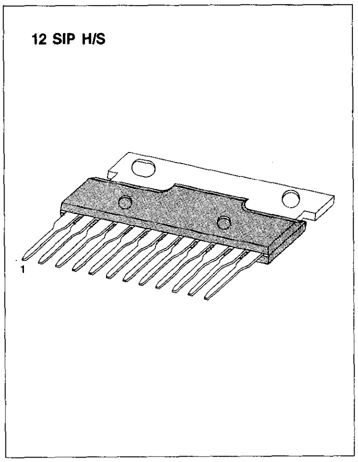
ELECTRICAL CHARACTERISTICS

(V_{CC} = +15V, V_{EE} = −15V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}			2	6	mV
Input Offset Current	I_{IO}			10	200	nA
Input Bias Current	I_{IB}			100	700	nA
Supply Current	I_S			10	20	mA
Output Voltage Swing	V_{OUT}	$R_L = 33\Omega$	±12	±13		V
Large Signal Voltage Gain	A_V			100		dB
Input Voltage Range	V_{ICR}		±12	±14		V
Common Mode Rejection Ratio	CMRR		70	90		dB
Power Supply Rejection Ratio	PSRR			50	150	μV/V
Bandwidth	BW			1.0		MHz
Slew Rate	SR	$A_V = 1$, $R_L = 33\Omega$, $R = 10\Omega$, $C = 0.1\mu F$		0.15		V/μS
Limiting Current	I_{OS}	$R_{SC} = 2.2\Omega$		0.35		A
Cross Talk	CT	$R_L = 33\Omega$, $V_O = 1V_{p\text{-}p}$		60		dB

DUAL POWER OPERATIONAL AMPLIFIER

The KA9257, a monolithic integrated circuit, is a dual power operational amplifier with maximum output current of 0.5A. Since it consists of balance transless, both forward and reverse operation of the motor can be a achieved on a single power. The device is suitable for a CD player.



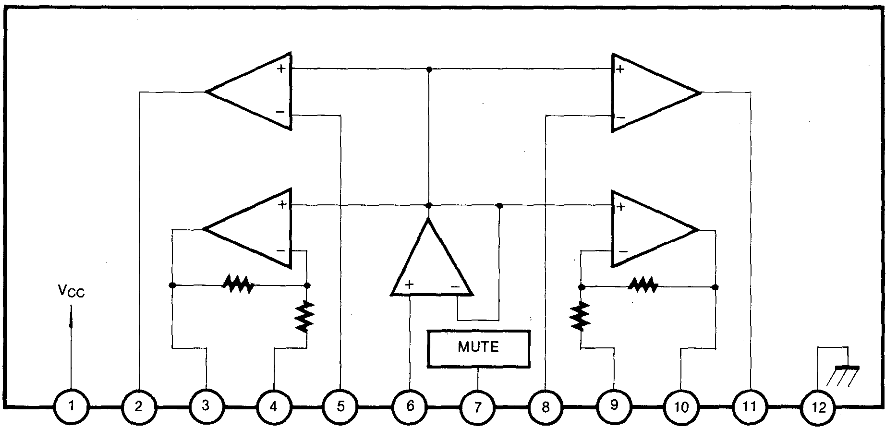
FEATURES

- 2 channel BTL driver
- Low input bias (lib = 30nA)
- Built in phase compensation capacitor
- Housed in a 12SIP H/S package for easy heat discharge
- Improved crosstalk: (CT = 80dB)
- High output current: (Io = 0.5A)

ORDERING INFORMATION

Device	Package	Operating Temperature
KA9257	12 SIP H/S	−25 ~ +75°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

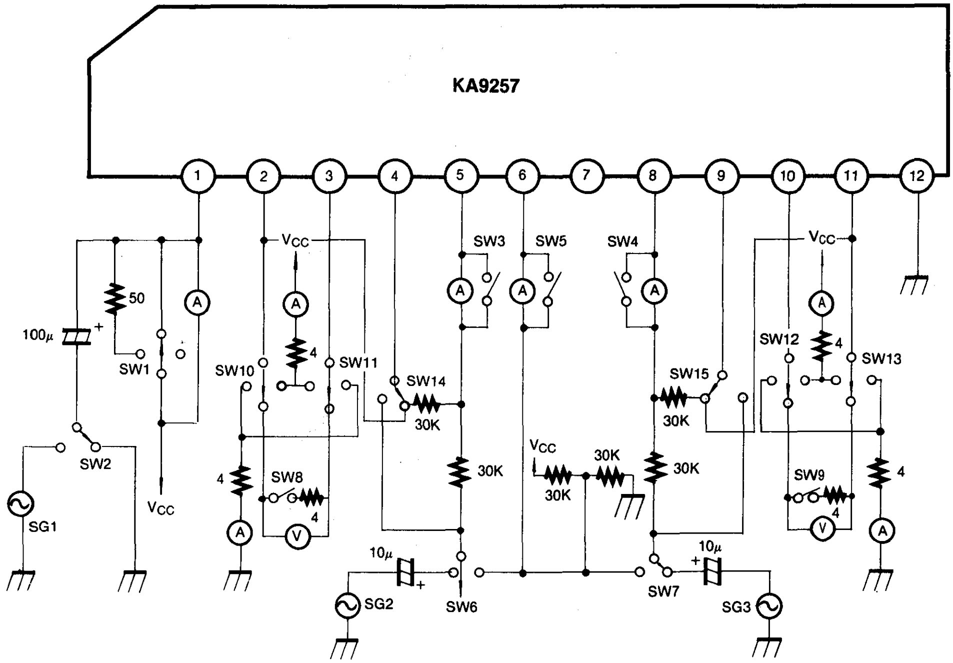
Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Power Dissipation	P_d	15	W
Operating Temperature	T_{opr}	−25 ~ +75	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

ELECTRICAL CHARACTERISTIC

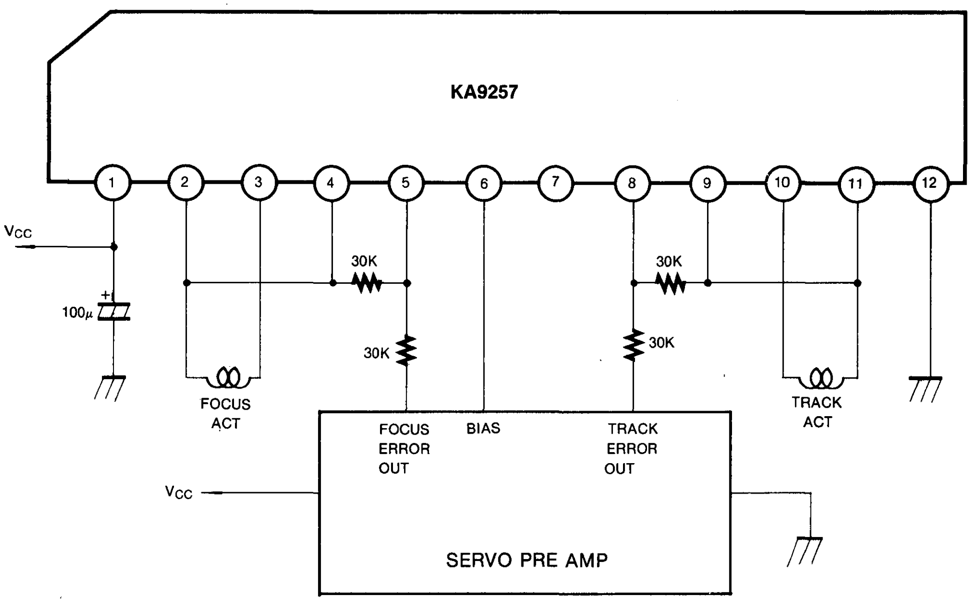
(Ta = 25°C, V_{CC} = 12V, f = 1KHz, R_L = 4ohm, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Circuit Current	I_{CC}	$V_{in} = 0$	—	3	10	mA
Input Bias Current	I_{ib}	$V_{in} = 0$	—	30	100	nA
Input Bias Pin Current	I_b	$V_{in} = 0$	—	100	300	nA
Output Offset Voltage	V_{oo}	$V_{in} = 0$	−50	0	50	mV
Maximum Source Current	I_{sou}	R_L = 4ohm, V_{out} = GND	0.7	1.4	—	A
Maximum Sink Current	I_{snk}	R_L = ohm, $V_{out} = V_{CC}$	0.4	0.8	—	A
Maximum Output Voltage	V_{om}	$V_{in} = 2V_{rms}$	1.8	2.5	—	V_{rms}
Closed Loop Gain	A_{vc}	$V_{in} = 0.1V_{rms}$	5.0	6.0	7.0	dB
Cut-off Frequency	f_T	V_{in} = 0.1rms, 3dB Down	15	20	—	KHz
Cross-Talk	CT	V_{in} = 0.1rms, BPF: 20-20KHz	40	80	—	dB
Ripple Rejection Ratio	RR	$V_{RR} = 0.1V_{rms}$ F_{RR} = 120Hz	30	40	—	dB
Slew-Rate	SR	$V_{in} = 0.3V_{pp}$ squarwave	—	0.3	—	V/μS

TEST CIRCUIT



APPLICATION CIRCUIT

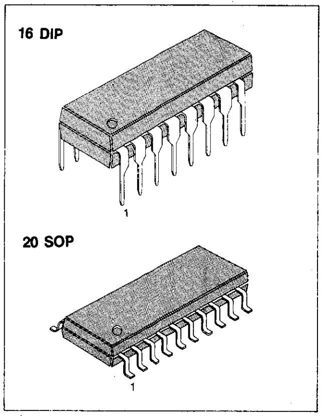


Precautions

1. In designing the board, minimum 6cms of segregation should be allowed between motor drive ICs (KA9257, KA9256) and other components such as Micom and/or Recorder/Player ICs.
2. To get stable supply of voltage and shield effect of radiation, the CD Deck needs to be grounded.

16-BIT D/A CONVERTER FOR CDPs

The KDA0316 is a CMOS 16-bit digital-to-analog converter for compact disc player that uses a dynamic level shift conversion method combining R-string, Pulse Width Modulation and level shift.



FEATURES

- **2's complement serial data input**
- **Contains two-channel D/A converter**
- **Can output L out and R out in phase**
- **To 176.4kHz maximum sampling frequency (corresponding to four oversampling)**
- **No deglich circuit needed**
- **Si-gate CMOS process (low power consumption)**
- **Single 5V supply voltage**
- **Built-in test circuit for PWM DAC**
- **Output swing level can be adjusted by the V_R input voltage**
- **MSB first and LSB first mode of input digital audio data is available**

TYPICAL APPLICATIONS

- Portable cassette radios with CDP
- Home audio component systems
- Electronic keyboards
- Music centers
- Mini CDPs
- Car CDPs

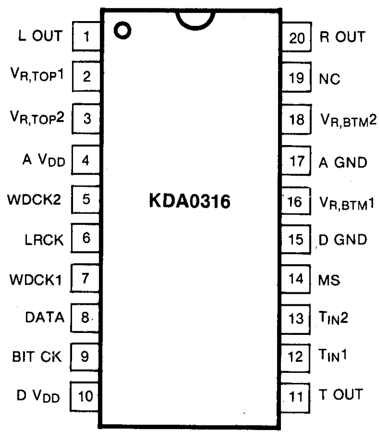
ORDERING INFORMATION

Device	THD(Max)(%)	Package	Temperature Range	Max Oversampling
KDA0316LN	0.05	20 DIP	−30°C ~ +75°C	4Fs
KDA0316N	0.08			
KDA0316LD	0.05	20 SOP		
KDA0316D	0.08			

Fs: sampling frequency (44.1KHz)

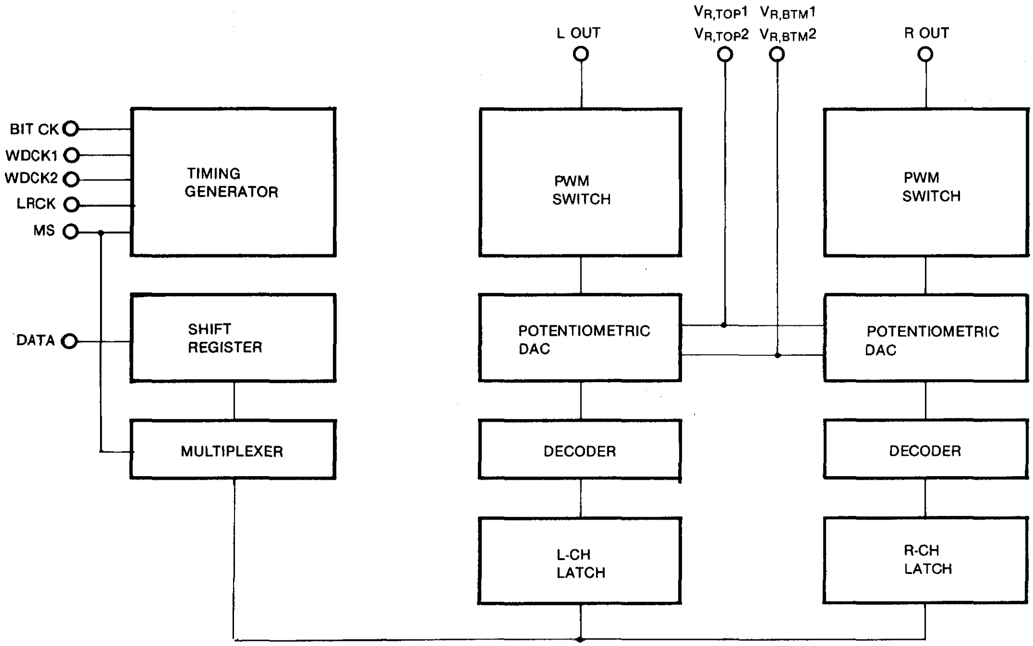
PIN CONFIGURATION

Dual-in-line Package &
Small Outline Package



Top View

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1 & 2)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	$-0.3 \sim +7.0$	V
Input Voltage	V_{IN}	$-0.3 \sim V_{DD}+0.3$	V
Output Voltage	V_{OUT}	$-0.3 \sim V_{DD}+0.3$	V
Operating Temperature Range	V_{opr}	$-30 \sim +75$	°C
Storage Temperature Range	T_{stg}	$-40 \sim +125$	°C
ESD Susceptibility (Note 3)	V_{ESD}	±900	V
Latch-up Current	I_{lat}	50	mA

4

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Operating Temperature Range	T_{opr}	−30		75	°C
Input "H" Voltage	V_{IH}	2.2		$V_{DD}+0.3$	V
Input "L" Voltage	V_{IL}	−0.3		0.8	V
Reference "H" Voltage	$V_{R,TOP}$	$V_{DD}-0.5$		V_{DD}	V
Reference "L" Voltage	$V_{R,BTM}$	0		0.5	V
Sampling Frequency	fs			176.4	KHz

ELECTRICAL CHARACTERISTICS

(Converter Specifications: $V_{DD}=5V$, $V_{ref}H=5V$, $V_{ref}L=$ A GND, IF=0V, $f_S=176.4KHz$, Ta=25°C, unless otherwise noted)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{CC}	$V_{DD}=5V$		3.5	5.5	mA
		$V_{DD}=5.5V$		4.0	7.0	
Total Harmonic Distortion	THD	MS=0V or 5V Data=1KHz, 0dB			0.05*1 0.08	%
		MS=0V or 5V Data=1KHz, −20dB			0.2	
Signal to Noise Ratio	SNR	Data=1KHz, 0dB		92		dB
		$V_{DD}=4.5V$ Data=1KHz, 0dB		87		
		MS=5V Data=1KHz, 0dB		92		
		MS=5V, $V_{DD}=4.5V$ Data=1KHz, 0dB		87		
Crosstalk	CT	Data=1KHz, 0dB		−85		dB

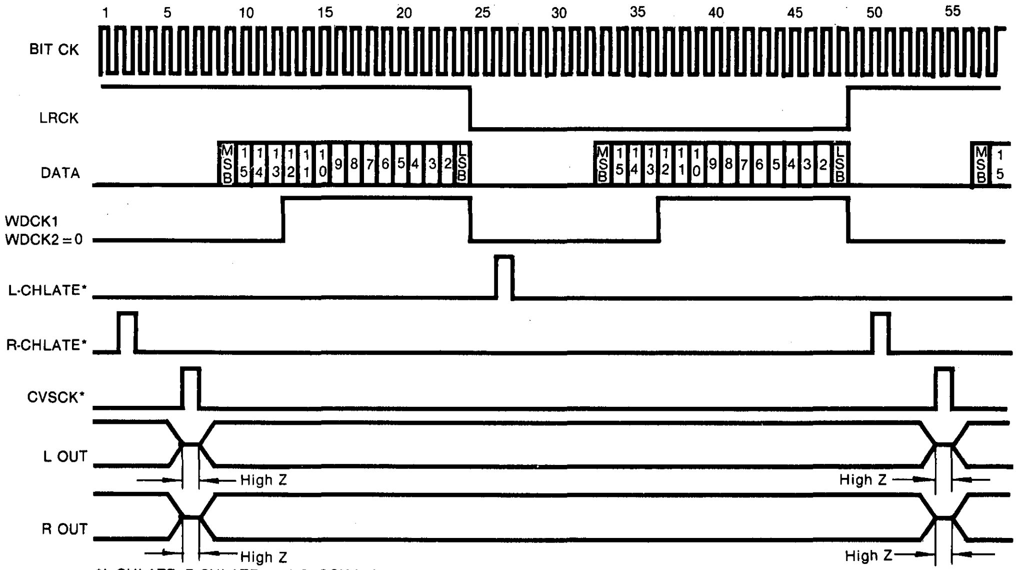
*1: User's option value (KDA016LN, KDA0316LD)

Note 1: ABSOLUTE MAXIMUM RATINGS are those values beyond which the life of the device may be impaired. Normal operation is not guaranteed at these extremes.

Note 2: All voltage are measured with respect to the GND, unless otherwise noted. The separate A GND point should always be wired to the D GND.

Note 3: 100pF discharged through a 1.5KΩ resistor.

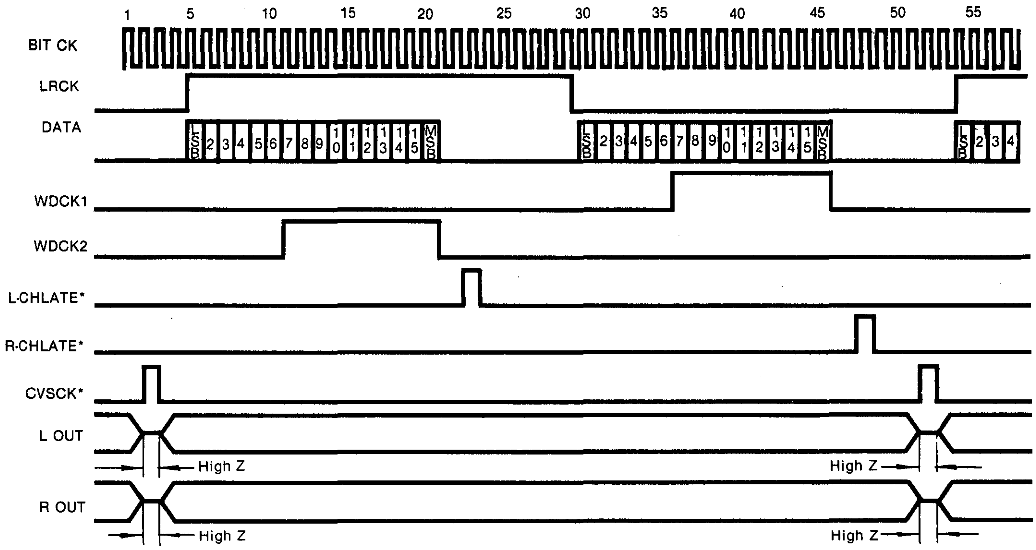
TIMING DIAGRAM 1 (When MS = "H")



*L-CHLATE, R-CHLATE, and CVSCK is internal signal.

BIT CK = 8.4672MHz (f_S = 176.4KHz)
4.2336MHz (f_S = 88.2KHz)
2.1168MHz (f_S = 44.1KHz)

TIMING DIAGRAM 2 (When MS = "L")



*L-CHLATE, R-CHLATE, and CVSCK is internal signal.

BIT CK = 8.6436MHz (f_S = 176.4KHz)
4.3218MHz (f_S = 88.2KHz)
2.1609MHz (f_S = 44.1KHz)

PIN DESCRIPTION

Pin No	Symbol	Function
1	L OUT	Left channel output pin
2	$V_{R,TOP}1$	Top reference voltage 1 pin
3	$V_{R,TOP}2$	Top reference voltage 2 pin
4	A V_{DD}	Analog supply voltage pin
5	WDCK2	Word clock 2 input pin
6	LRCK	Left/right clock input pin
7	WDCK1	Word clock 1 input pin
8	DATA	Digital audio data input pin
9	BIT CK	Bit clock input pin
10	D V_{DD}	Digital supply voltage pin
11	T OUT	Test output pin
12	$T_{IN}1$	Test input pin
13	$T_{IN}2$	Test input pin
14	MS	Mode selecting pin
15	D GND	Digital ground pin
16	$V_{R,BTM}1$	Bottom reference voltage 1 pin
17	A GND	Analog ground pin
18	$V_{R,BTM}2$	Bottom reference voltage 2 pin
19	NC	No connection
20	R OUT	Right channel output pin

FUNCTIONAL DESCRIPTION

1. Calling for Digital Audio Data

Digital audio data is a 16-bit serial 2's complement signal. The KDA0316 corresponds to MSB first code or LSB first code of digital audio data: the mode can be changed by the level of the MS pin. Data through the DATA pin is applied to the LCH latch and RCH latch of the two D/A converters built in the separate LCH and RCH.

(1) When MSB First (MS = "H" level) (see Timing Diagram 1)

Digital audio data is carried in MSB first sequence from the data pin to the Shift Register in synchronization with the BIT CK rising edge (Data transition occurs at the BIT CK falling edge.).
LCH data and RCH data are carried to the LCH latch and RCH latch by both the LCH latchable (L-CHLATE) and RCH latchable (R-CHLATE).

(2) When LSB First (MS = "L" level) (see Timing Diagram 2)

Digital audio data is carried in LSB first sequence from data pin to Shift Register in synchronization with BIT CK falling edge (Data transition is occurred at the BIT CK falling edge.).
LCH data and RCH data are carried to the LCH latch and RCH latch by both the LCH latchable (L-CHLATE) and RCH latchable (R-CHLATE).

2. D/A Conversion Circuit (see Fig. 1)

The KDA0316 has two D/A conversion circuits in the LCH and RCH independently. The two conversion methods are the same: a Complex Potentiometric Method, combining Resistor-Ladder D/A conversion, PWM (Pulse Width Modulation) D/A conversion, and Variable Resistor D/A conversion. After storing in the latch, the upper 9 bits of data (D15 ~ D7) inputs into the Resistor-Ladder DAC, the middle 3 bits of data (D6 ~ D4) into the PWM DAC and the lower 4 bits of data (D3 ~ D0) into the Variable Resistor DAC of the whole 16 bits of digital audio data (D15 ~ D0), respectively.
The Digital audio data of the LCH and RCH, which were inputted by the time division multiplexing method from the DATA pin, synchronize with the conversion clock and after being converted by the D/A converters the respective analog signals in phase are outputted from the L OUT and R OUT pins.

(1) Resistor-Ladder DAC

The 9-bit D/A conversion circuit, which has a 512 ($=2^9$) unit resistor string, divides the whole voltage ($V_{R,TOP}$, $V_{R,BTM}$) across a Resistor-Ladder into 512 steps. The two adjoining Va and Vb of the whole voltage, which are divided into 512 steps according to the upper 9 bits of data (D15 ~ D7), are outputted by a switching circuit of PWM DAC, where $Vb - Va = (V_{R,TOP} - V_{R,BTM})/512$.

(2) PWM DAC

The 3-bit PWM DAC makes the differential voltage between Va and Vb, which is applied from a Resistor-Ladder DAC, divided into 8 steps by pulse width modulation.
According to the value of the upper 3 bits of data (D6 ~ D4), Va and Vb is outputted through the LCH or RCH terminal. A PWM DAC clock uses the BIT CK, and a relationship of sampling frequency and BIT CK frequency is shown in the Timing Diagrams.

(3) Variable Resistor DAC

The 4-bit Variable Resistor DAC has two variable resistors, VR_{TOP} and VR_{BTM}, in series with the Resistor-Ladder. According to the lower 4 bits of data (D3 ~ D0), VR_{TOP} and VR_{BTM} vary as follows:

1) Irrespective of the value of data, $(VR_{TOP} + VR_{BTM})$ is constant.
2) According to the value of data, VR_{TOP} and VR_{BTM} ranges from zero to 15R/128 (R is a unit resistor of the Resistor-Ladder): in R/128 steps. Therefore according to the lower 4 bits of data (D3 ~ D0), Va and Vb of an R-string DAC outputs range from zero to $15\triangle V/128$ $\{\triangle V = (V_{TOP} - V_{BTM})/512\}$ in $\triangle V/128$ steps.

3. How to Use V_R (see Fig. 1)

V_R, the reference voltage across a Resistor-Ladder, is usually recommended with $V_{R,TOP}1 = 5V$, $V_{R,BTM}1 = 0V$. One way of avoiding an amplitude mismatching between the V_R and OP amp input connected to the output of the KDA0316 is to reduce the analog output amplitude with $V_{R,TOP}2 = 5V$ and $V_{R,BTM}2 = 0V$ (at this time about 47μF ~ 100μF capacitors should be connected from $V_{R,TOP}1$ and $V_{R,BTM}1$ to GND.). By the effect of built-in R_{TOP} and R_{BTM} with this choice, the maximum analog output amplitude results in a narrow range of about 1.5 ~ 3.5V for 0dB playback.

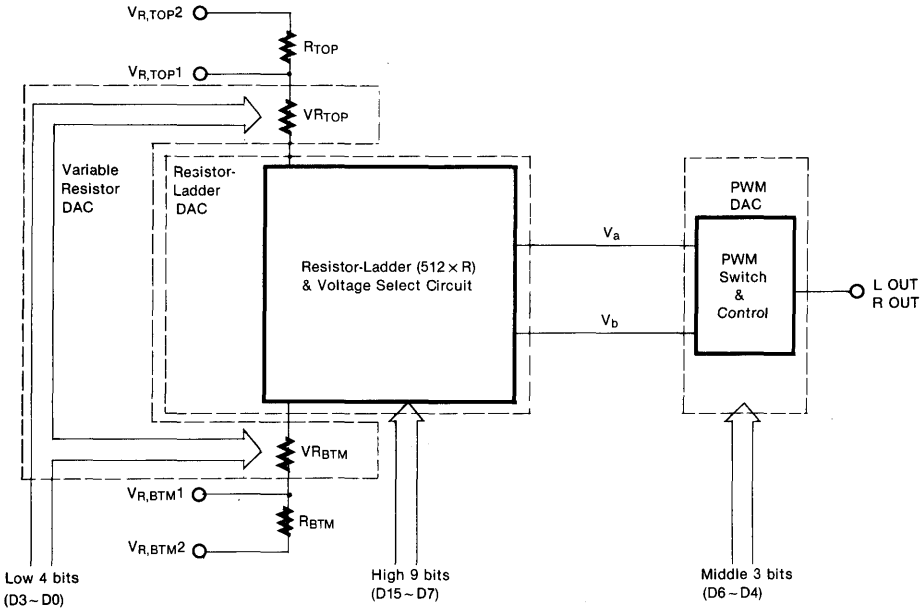
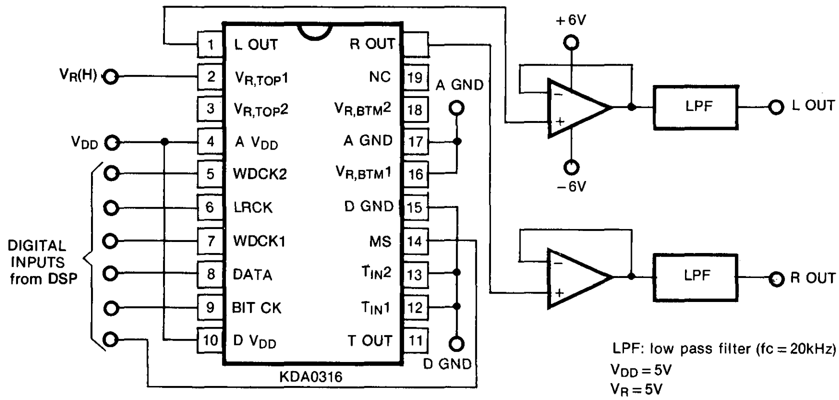


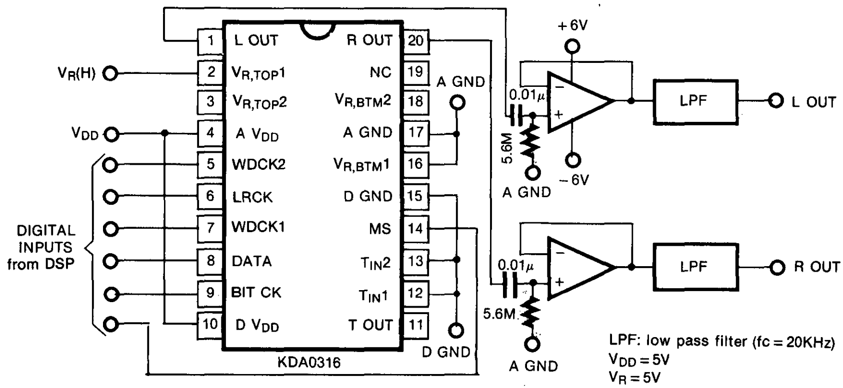
Fig. 1

TYPICAL APPLICATIONS

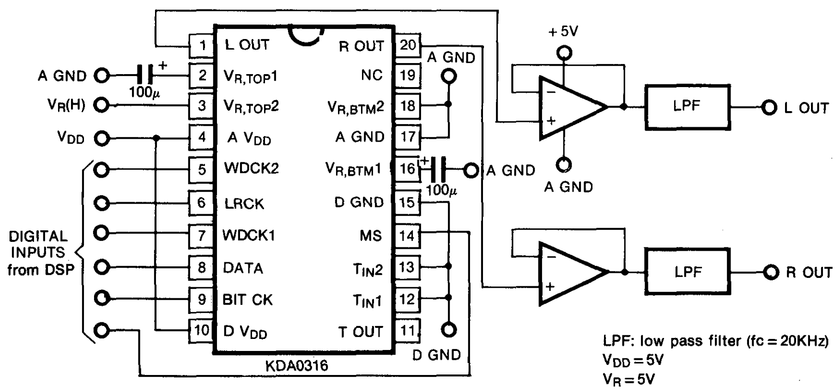
(1)



(2)

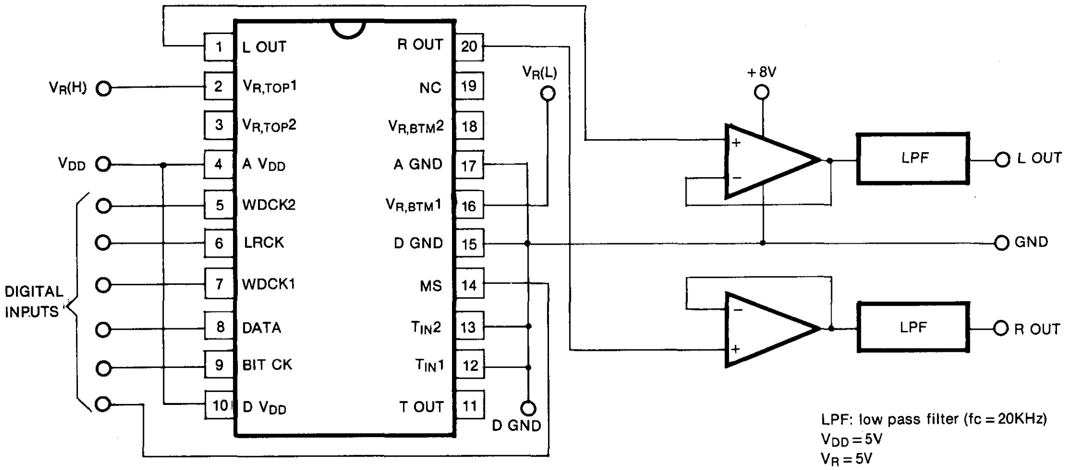


(3)



Note: (1) D GND should be wired to the digital ground group and A GND to the analog ground group.
(2) V_{DD} and V_R power supply should be low impedance and high stable (for example, three-terminal voltage regulator).
(3) Because of the low output impedance and weak noise immunity of Pin 1 or Pin 20, noise reduction should be done by reducing the lead-wire length to the next OP amp stage.

TEST CIRCUIT



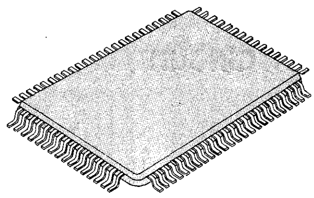
LPF: low pass filter (fc = 20KHz)
V_{DD} = 5V
V_R = 5V
fs = 176.4KHz

4-BIT MICROCONTROLLER

KS56C820 is an SMCS56 core-based 4 bit CMOS Microcomputer with LCD drivers, various peripherals that allows a high level control of target products, and numerous I/O's. The flexible I/O control commands that can handle 1, 4, and 8 bit data manipulations will allow diverse applications control.

KS56C820 has enough LCD drivers, and many CPU clock modes that minimizes current that it is suitable for applications on portable products like CDP, DAT, camera, and LCD remote controllers.

80 FQP

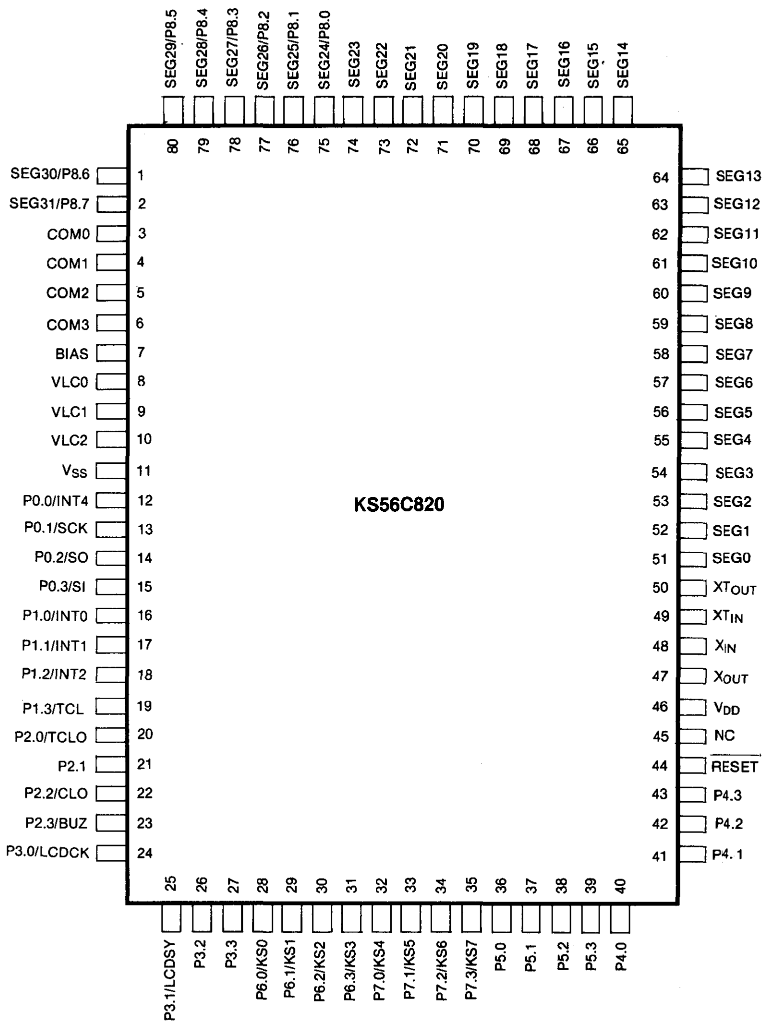


FEATURES

- Memory Mapped I/O
- ROM: 8064 x 8 bits
- RAM: 512 x 4 bits
- One 8-bit timer/counter input source: 2 external, and 4 internal inputs
- Watch timer
- One 8-bit SIO
  - — Can send either from LSB or MSB.
  - — Can choose either transmit and receive, or receive only modes
- Multiple vector interrupts
  - — Three external source interrupts: INT0, INT1, INT4
  - — Three internal source interrupts: Basic Timer, Timer/counter, SIO
  - — One external edge detectable quasi-interrupt: INT2
  - — One quasi-interrupt for clock: INTW
- 32 I/O bits (max 40 I/O bits)
  - — Inputs: 8 bits
  - — I/O: 16 bits; built-in LED driver.
  - — N-channel open drain I/O: 8 bitgs; can handle up to 10 volts.
  - — Output: Maximum 8 bits (including segment driver output)
- Max. 16 digits of LCD driver
  - — Static, 1/2, 1/3, 1/4 duty selectable.
  - — 24, 28, 32 segment output selectable.
- 2KHz output for buzzer
- 16-bit Bit Sequential Carrier useful for remote controller.
- Two types of power-down mode
  - — Idle: Only the CPU clock stops.
  - — Stop: All internal clocks stop.
- Can choose from various instruction cycle time for power saving.
  - — Using Main-system clock: 1, 2, 16μS/4MHz
  - — Using Sub-system clock: 122μS/32.768KHz
- Built-in crystal/ceramic oscillator circuits for clock.
  - — Crystal/ceramic oscillator circuit for main-system clock.
  - — Crystal oscillator circuit for sub-system clock.
- 3/5V single power supply
- 80 Plastic Quad Flat Package

4

PIN CONFIGURATION



PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th colspan="2">Pin Description</th></tr>
<tr><td>P1.0-P1.3</td><td>4-bit Input</td><td rowspan="3">Internal pull-up resistor can be specified in 4-bit unit by software</td></tr>
<tr><td>P2, P7</td><td>4-bit Input/Output</td></tr>
<tr><td>P3, P6</td><td>I/O mode selectable in 1-bit unit by software</td></tr>
<tr><td>P4, P5</td><td colspan="2">4-bit input/output, N-ch open drain</td></tr>
<tr><td>P8.0-P8.7</td><td colspan="2">Outputs in 1-bit unit (shared with segment outputs)</td></tr>
<tr><td>SEG0-SEG23</td><td colspan="2">Segment output for LCD display</td></tr>
<tr><td>SEG24-SEG31</td><td colspan="2">Segment output for LCD display (shared with Port 8)</td></tr>
<tr><td>COM0-COM3</td><td colspan="2">Common signal output for LCD display</td></tr>
<tr><td>VLC0-VLC2</td><td colspan="2">LCD power supply pin</td></tr>
<tr><td>BIAS</td><td colspan="2">LCD power supply control pin for 3/5V operating</td></tr>
<tr><td>LCDCK</td><td colspan="2">LCD clock output for display expansion</td></tr>
<tr><td>LCDSY</td><td colspan="2">LCD sync. clock output for display expansion</td></tr>
<tr><td>TCL</td><td colspan="2">Timer/Counter external clock input</td></tr>
<tr><td>TCLO</td><td colspan="2">Timer/Counter clock output</td></tr>
<tr><td>INT0, 1, 2, 4</td><td colspan="2">External interrupt input</td></tr>
<tr><td>CLO</td><td colspan="2">Clock output</td></tr>
<tr><td>BUZ</td><td colspan="2">2KHz clock output for buzzer</td></tr>
<tr><td>KS0-KS7</td><td colspan="2">Semi-interrupt input detecting external falling edge</td></tr>
<tr><td>SCK, SI, SO</td><td colspan="2">SCK: serial clock, SI: serial input, SO: serial output</td></tr>
<tr><td>X_{IN}, X_{OUT}</td><td colspan="2">Crystal/Ceramic or RC clock I/O for Main-system clock</td></tr>
<tr><td>XT_{IN}, XT_{OUT}</td><td colspan="2">Crystal clock I/O for sub-system clock</td></tr>
</table>

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

<table>
<tr><th>Characteristic</th><th>Symbol</th><th colspan="2">Test Conditions</th><th>Value</th><th>Unit</th></tr>
<tr><td>Supply Voltage</td><td>V_{DD}</td><td colspan="2"></td><td>$-0.3 \sim +7.0$</td><td>V</td></tr>
<tr><td>Input Voltage</td><td>V_I</td><td colspan="2"></td><td>$-0.3 \sim V_{DD}+0.3$</td><td>V</td></tr>
<tr><td>Output Voltage</td><td>V_O</td><td colspan="2"></td><td>$-0.3 \sim V_{DD}+0.3$</td><td>V</td></tr>
<tr><td rowspan="2">High Level Output Current</td><td rowspan="2">I_{OH}</td><td colspan="2">1 Port</td><td>-15</td><td>mA</td></tr>
<tr><td colspan="2">All Ports</td><td>-30</td><td>mA</td></tr>
<tr><td rowspan="6">Low Level Output Current</td><td rowspan="6">I_{OL}</td><td rowspan="2">1 Port</td><td>MAX.</td><td>30</td><td>mA</td></tr>
<tr><td>TYP.</td><td>15</td><td>mA</td></tr>
<tr><td rowspan="2">Port 2, Port 3</td><td>MAX.</td><td>100</td><td>mA</td></tr>
<tr><td>TYP.</td><td>60</td><td>mA</td></tr>
<tr><td rowspan="2">Port 6</td><td>MAX.</td><td>100</td><td>mA</td></tr>
<tr><td>TYP.</td><td>60</td><td>mA</td></tr>
<tr><td>Operating Temperature</td><td>T_{opr}</td><td colspan="2"></td><td>$-20 \sim +75$</td><td>°C</td></tr>
<tr><td>Storage Temperature</td><td>T_{stg}</td><td colspan="2"></td><td>$-55 \sim +125$</td><td>°C</td></tr>
</table>

4

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (Ta = −40 ~ +85°C, V_{DD} = 4.0 ~ 6.0V)

Characteristic	Symbol	Test Conditions			Min	Typ	Max	Unit
High Level Input Voltage	V_{IH1}	Port 2, 3			0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Port 1, 6, RESET			0.8 V_{DD}		V_{DD}	V
	V_{IH3}	Port 4, 5	built in pull up re-		0.7 V_{DD}		V_{DD}	V
			-sistor open drain		0.7 V_{DD}		10 V_{DD}	V
	V_{IH4}	X_{IN}, X_{OUT}, XT_{IN}			$V_{DD}-0.5$		V_{DD}V	
Low Level Input Voltage	V_{IL1}	Port 2, 3			0		0.3 V_{DD}	V
	V_{IL2}	Port 1, 6, RESET			0		0.2 V_{DD}	V
	V_{IL3}	X_{IN}, X_{OUT}, XT_{IN}			0		0.4	V
High Level Output Voltage	V_{OH1}	Port 2, 3, 6, BIAS	$I_{OH}=-1mA$		$V_{DD}-1.0$			V
			$I_{OH}=-100\mu A$		$V_{DD}-0.5$			V
	V_{OH2}	P8.0-7	$I_{OH}=-100\mu A$		$V_{DD}-2.0$			V
			$I_{OH}=-30\mu A$		$V_{DD}-1.0$			V
Low Level Output Voltage	V_{OL1}	Port 2, 3, 6, BIAS	$I_{OL}=15mA$			0.4	2.0	V
			$I_{OL}=1.6mA$				0.4	V
			$I_{OL}=400\mu A$				0.5	V
	V_{OL2}	P8.0-7	$I_{OL}=100\mu A$				1.0	V
			$I_{OL}=50\mu A$				1.0	V
Supply Current	I_{DD1}	4.19MHz	$V_{DD}=5V+10\%$			2.5	8	mA
			$V_{DD}=3V+10\%$			0.35	1.2	mA
	I_{DD2}		IDLE	$V_{DD}=5V$		500	1500	μA
				$V_{DD}=3V$		150	450	μA
	I_{DD3}	32.768 KHz	$V_{DD}=3V+10\%$			30	90	μA
	I_{DD4}		IDLE	$V_{DD}=3V$		5	15	μA

AC CHARACTERISTICS (Ta = −40 ~ +85°C, V_{DD} = 4.0 ~ 6.0V)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Cycle Time	t_{CY}	Main-system Clock	0.95		64	μS
		Sub-system Clock	114	122	125	μS
TCL Input Frequency	f_{TI}	$V_{DD}=4.5\sim6.0V$	0		1	MHz
			0		275	KHz
TCL Input High & Low Level Width	t_{TIH}	$V_{DD}=4.5\sim6.0V$	0.48			μS
	t_{TIL}		1.8			μS
Ext. Interrupt High & Low Level Width	t_{INTH}					μS
		INT1, INT2	10			μS
	t_{INTL}	KS0 − KS3	10			μS
RESET Low Level Width	t_{RSL}		10			μS

NOTES

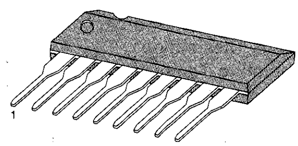
TOY RADIO CONTROL ACTUATORS 5

TOY APPLICATION

TOY RADIO CONTROL ACTUATOR

The KA2303 is a monolithic integrated circuit having 3 functions (forward, stop, backward) designed for radio-controlled toy cars.

9 SIP



FEATURES

- **Includes**
  Amplifier, Detector, Comparator, Latch, Voltage Regulator, Actuator.
- **Wide operating supply voltage range (2.5V ~ 10V)**
- **Very low quiescent circuit current (Stop: I_{CC} = 5mA)**
- **Capable of driving small DC motors in both directions.**
- **A minimum numbe rof external parts are required.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2303	9 SIP	−20 ~ +70°C

BLOCK DIAGRAM

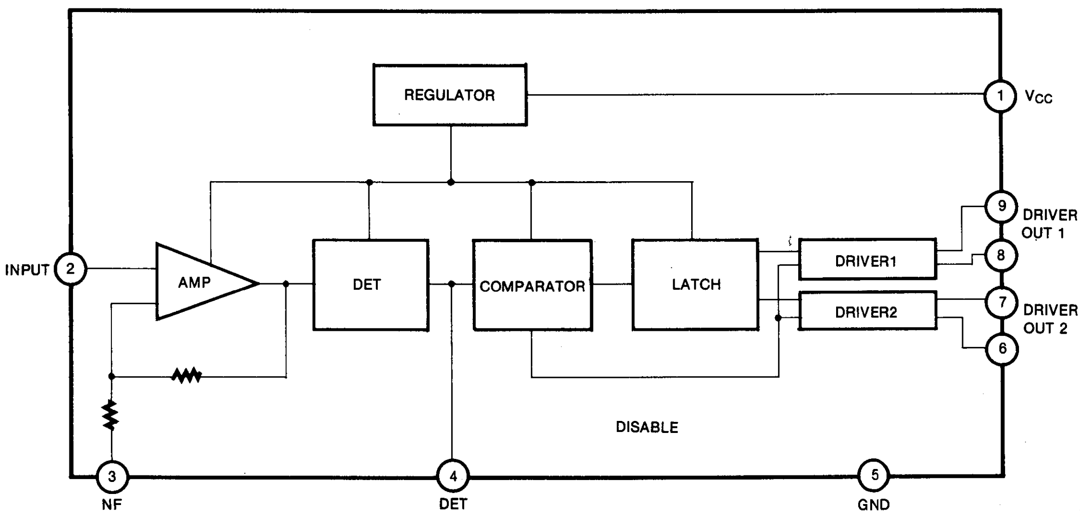


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	11	V
Output Current (Continuous)	I_O (cont)	0.7	A
Output Current (Surge)	I_O (surge)	1.2	A
Power Dissipation	P_d	500	mW
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=5V)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Circuit Current	$I_{CC}1$	Without Load, $V_i=0$		40	50	mA
	$I_{CC}2$	Stop, $V_i=10mV$		5		mA
Input Impedance	R_i			10		KΩ
Output Saturation Voltage	V_{SAT}	$I_O=400mA$, Pin 7, Pin 8		0.25	0.45	V
Output Sink Current	I_{SINK}	$V_i=0$, Pin 6, Pin 9		10		mA
Sensitivity	V_i (sen)	f=1KHz	3.5	6	9	mV
Comparator Hysteresis	HY		4	8	14	dB

TEST CIRCUIT

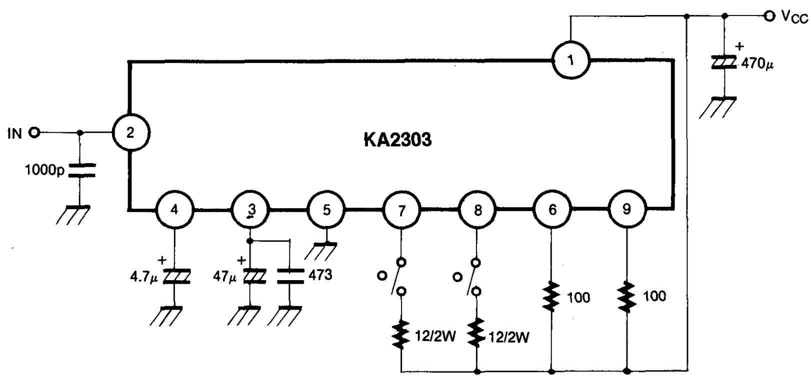


Fig. 2

TYPICAL APPLICATION CIRCUIT

1. Low Voltage Application Circuit

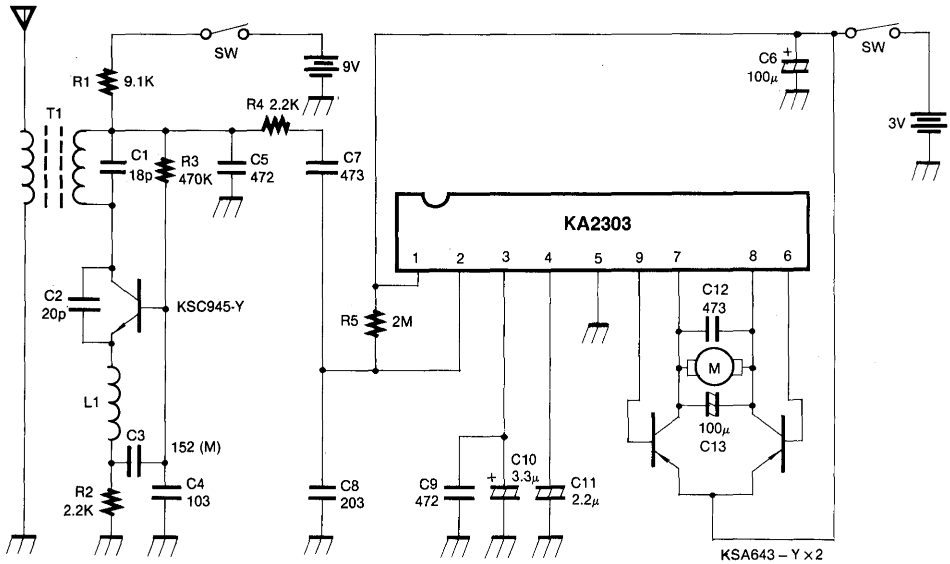


Fig. 3

2. High Voltage Application Circuit

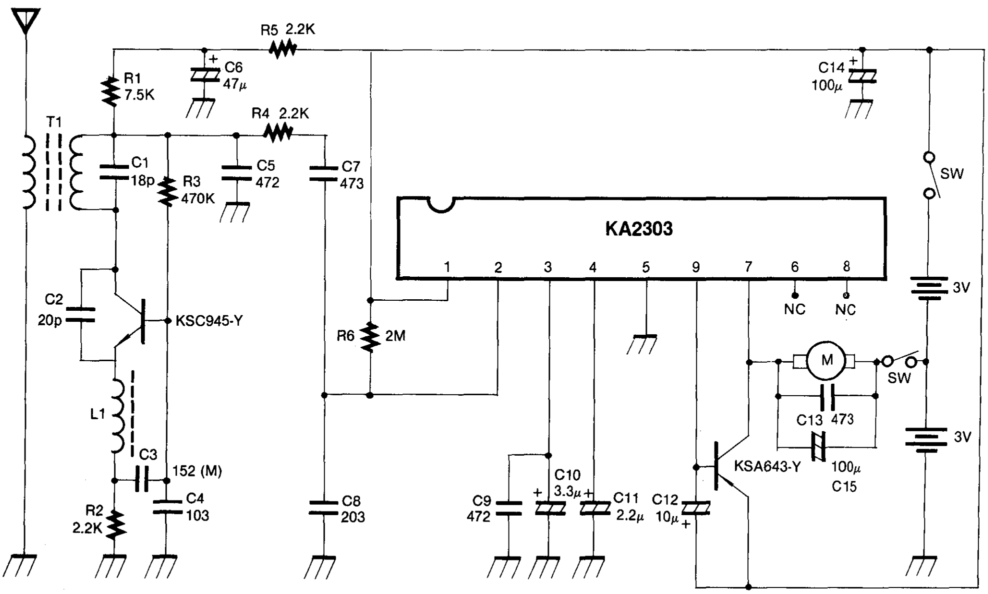
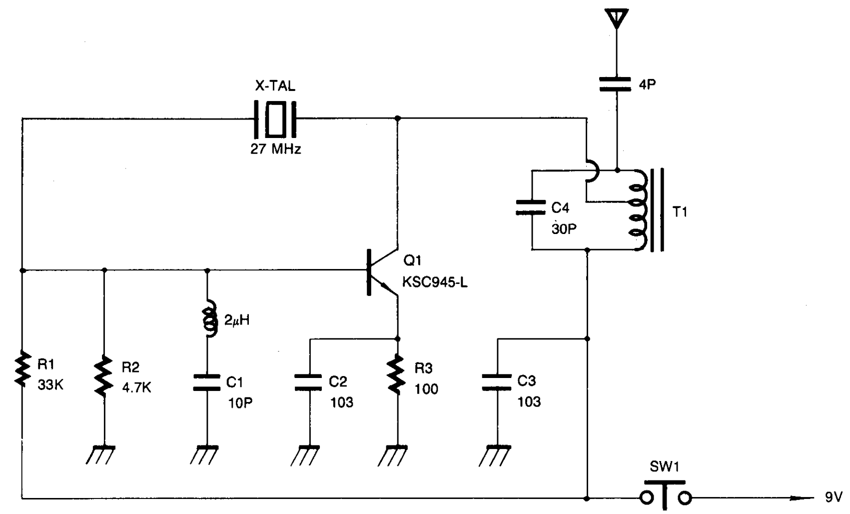


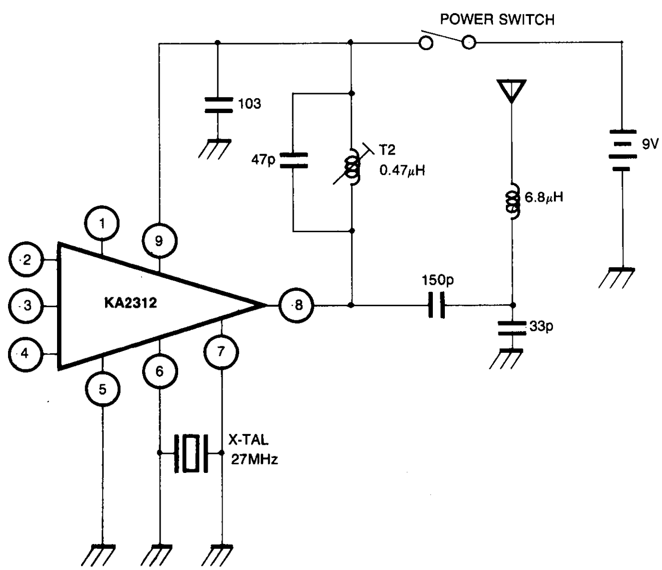
Fig. 4

TYPICAL APPLICATION CIRCUIT (TX)

1. Discrete Transmitter Application Circuit for KA2303, KA2304



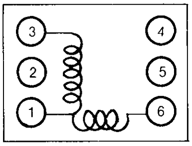
2. KA2312 Application Circuit for KA2303, KA2304



COIL SPECIFICATION

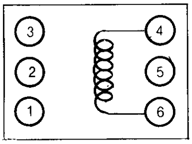
1. Transmitter

T1



Inductance	Q_O	TURNS		f_O (MHz)	Wire
		3-1	1-6		
0.7μH ± 10%	60 (min)	$2\frac{7}{8}$ T	$5\frac{7}{8}$T	25.2	0.3ϕ UEW

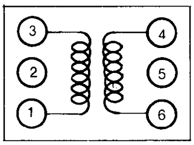
T2



Inductance	Q_O	TURNS	f_O (MHz)	Wire
0.52μH ± 10%	60 (min)	$6\frac{7}{8}$T	25.2	0.3ϕUEW

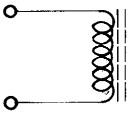
2. Receiver

T1



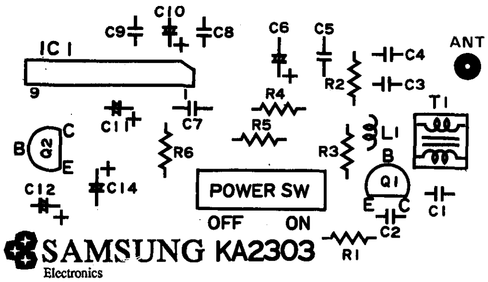
Inductance	Q_O	TURNS		f_O (MHz)	Wire
		1-3	4-6		
1.15μH ± 10%	60 (min)	$8\frac{3}{8}$ T	$2\frac{3}{8}$T	7.96	0.3ϕ UEW

L1



Inductance	Q_O	TURNS	f_O (MHz)	Wire
33μH ± 10%	60 (min)	45T	2.52	0.14d2UEW

DEMO BOARD (1:1 SCALE)



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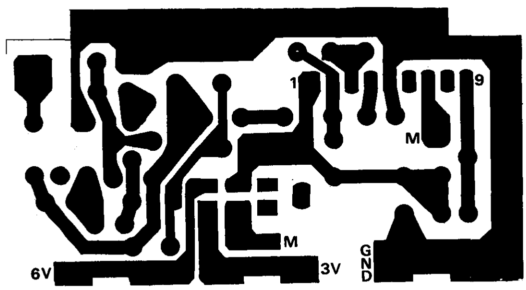


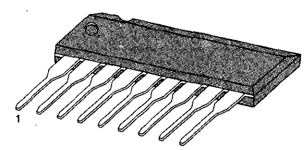
(BOTTOM VIEW)

TOY RADIO CONTROL ACTUATOR

The KA2304 is a monolithic integrated circuit designed for remote-controlled 2-function (forward, backward) actuators.
It is suitable for radio-controlled toy cars.

FEATURES

- Include
  Amplifier, Detector, Comparator, Latch, Voltage Regulator, Actuator
- Wide operating supply voltage range (V_{CC}=2.5V ~ 10 V)
- Minimum number of external parts required.



5

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2304	9 SIP	−20 ~ +70°C

BLOCK DIAGRAM

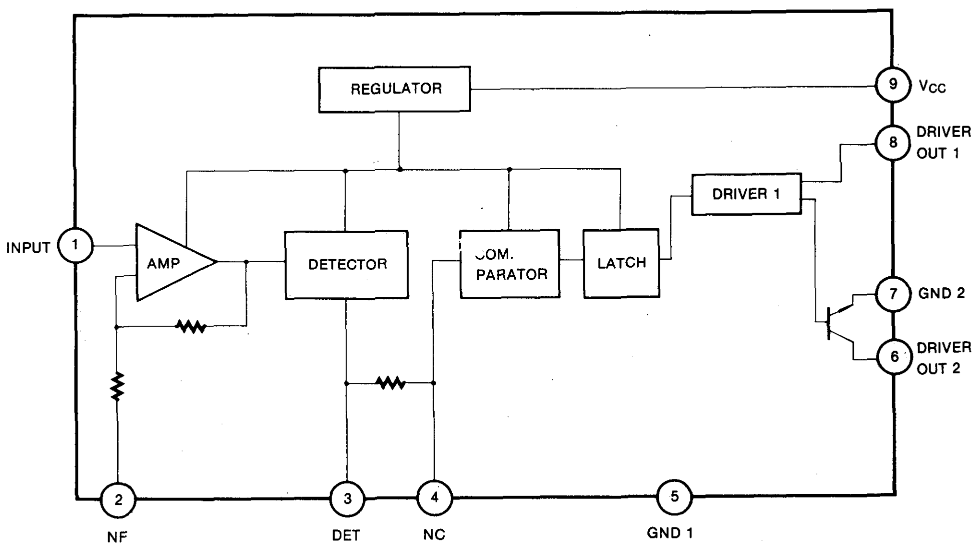


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	11	V
Power Dissipation	P_d	500	mW
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−40 ~ +150	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 5V)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{CC}		2.5	5	10	V
Circuit Current	I_{CC}	V_{CC} = 5V	10	20	40	mA
Input Impedance	Z_i	V_{CC} = 5V		10		KΩ
Output Sink Current	I_{SINK}	Pin 8 is actuated	6	15	20	mA
Output Saturation Voltage	V_{SAT}	Pin 6 is actuated		0.25	0.45	V
Sensitivity	V_i (sen)	Output is actuated	2	4	6	mV
Comparator Hysteresis	HY		5	8	11	dB

TYPICAL APPLICATION CIRCUIT

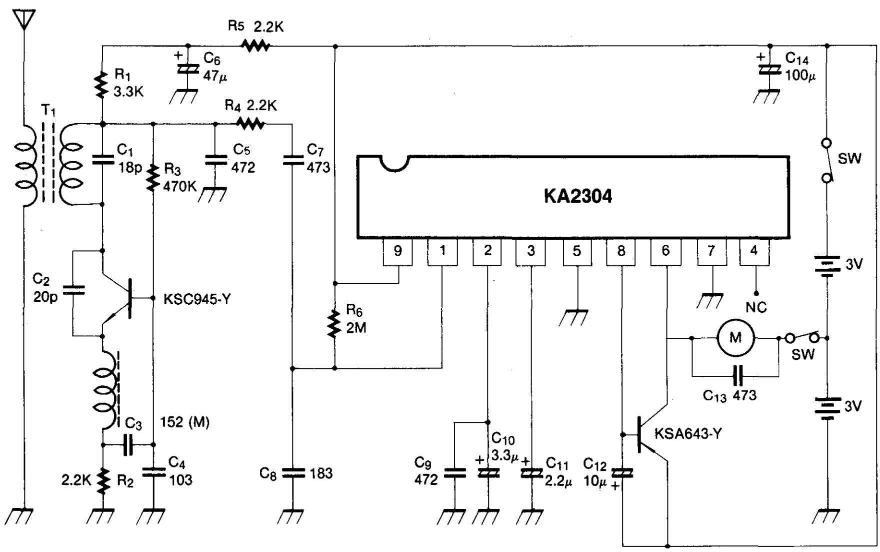
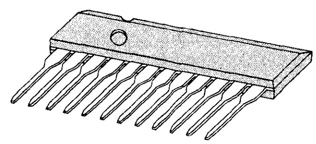


Fig. 2

TOY RADIO CONTROL ACTUATOR (RX)

The KA2305A is a monolithic integrated circuit having 3 function designed for receiving signals for radio-controlled toy cars.

12 SIP S H



FEATURES

- **Includes regulator for super regeneration circuit.**
- **Simple 3 function on nonsequencial mode : forward, backward, stop**
- **Wide operating supply voltage range: V_{CC} = 3V ~ 18V**
- **Low quiescent circuit current (I_{CC} = 10.5mA: Typ)**
- **Low operating supply voltage (V_{CC} = 3V)**
- **A minimum number of external parts are required**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2305A	12 SIP-SH	−20 ~ +75°C

BLOCK DIAGRAM

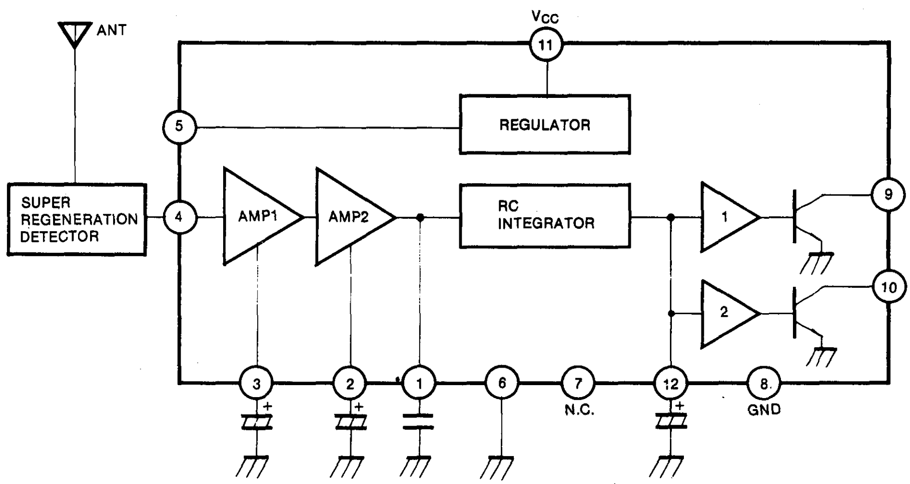


Fig. 1

ABSOLUTE MAXIMUM RATINGS ($Ta=25°C$)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	20	V
Drive Voltage	V_d	20	V
Drive Current	I_d	40	mA
Regulator Output Current	I_{reg}	15	mA
Power Dissipation	P_d	625	mW
Operating Temperature	T_{opr}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS ($Ta=25°C$, $V_{CC}=6V$)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Circuit Current	I_{CC}	$V_{CC}=6V$, $V_i=0$		10.5	13.5	mA
Saturation Voltage	V_9(sat)	$D_t=25\%$, $I_9=30mA$		0.9	1.2	V
	V_{10}(sat)	$D_t=75\%$, $I_{10}=30mA$				
Regulator Output Voltage	V_{reg}	$V_{CC}=6V$	2.3	2.5	2.7	V
Low Operating Voltage	V_{CCL}	$V_{reg}=2.3V$			3	V
High Operating Voltage	V_{CCH}	$V_{reg}=2.3V$(min) ~ 2.7V(max)	20			V
Sensitivity (V_i = square wave)	V_9(sen)	$D_t=25\%$		2	4	$mV_{p\text{-}p}$
	V_{10}(sen)	$D_t=75\%$				
Voltage Gain	A_V	$V_i=0.8mV_{rms}$, $f=1KHz$	55	58	61	dB

TEST CIRCUIT

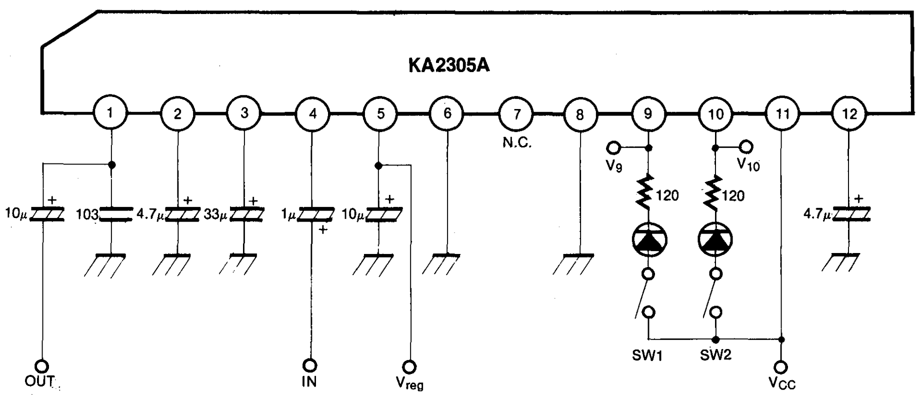


Fig. 2

PIN DESCRIPTION

Pin No.	Symbol	Function
1	OUT2	The 2'nd AMP. OUTPUT
2	BY2	The 2'nd AMP. BY-PASS
3	BY1	The 1'st AMP. BY-PASS
4	INPUT	Signal Input
5	V_{reg}	Regulator Output (V_{reg} = 2.5V)
6	GND	GND
7	N.C.	N.C.
8	GND	GND
9	OUTPUT1	Output of FORWARD (25% duty)
10	OUTPUT2	Output of BACKWARD (75% duty)
11	V_{CC}	Supply Voltage (3-18V)
12	RC-INT.	Output of RC INTEGRATOR

APPLICATION CIRCUIT

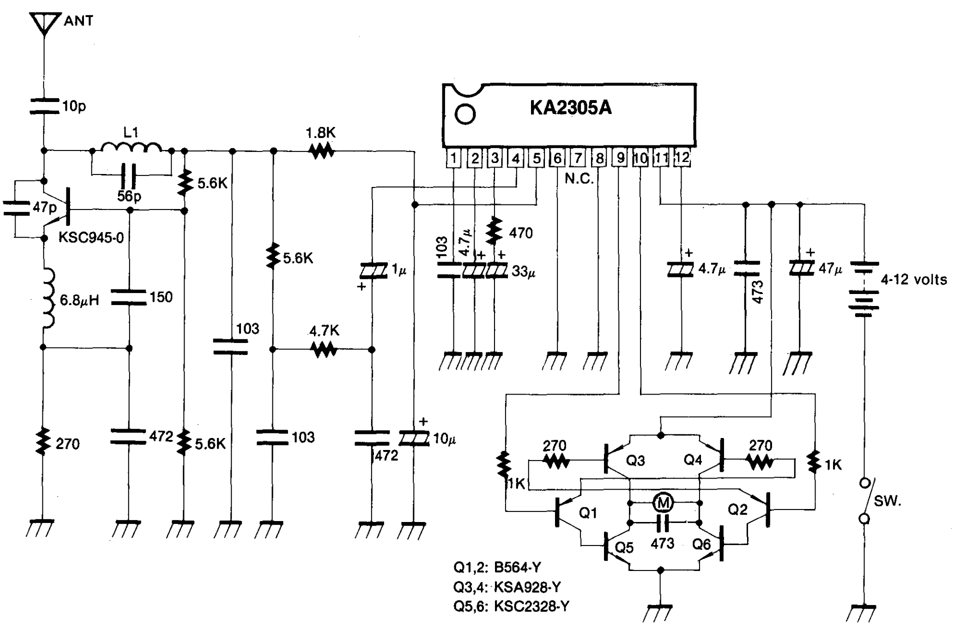


Fig. 3

5

TRANSMITTER APPLICATION CIRCUIT FOR KA2305A

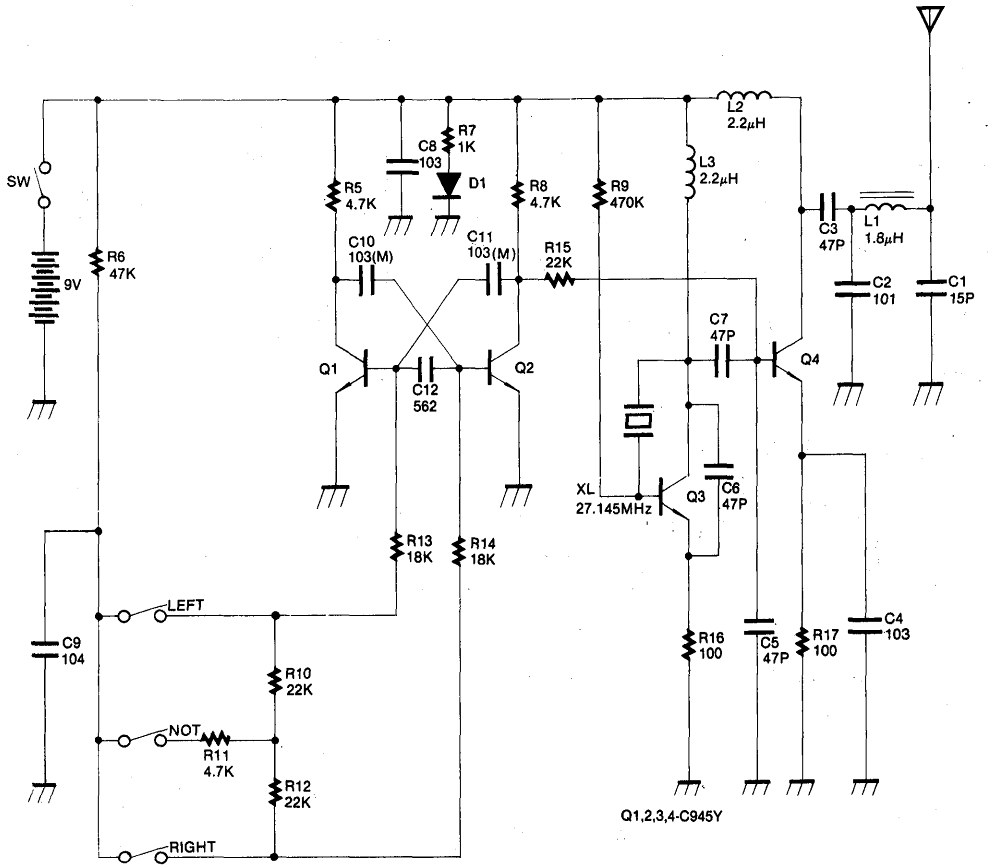
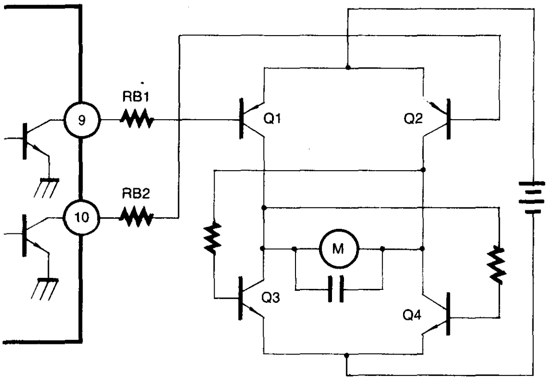
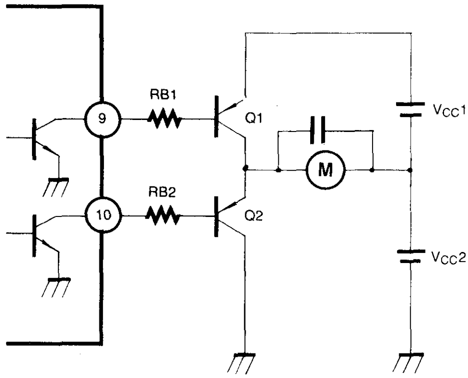


Fig. 4

KA2305 DRIVER OUTPUT APPLICATION STAGE

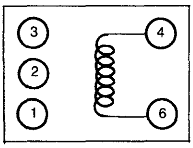
①APPLICATION I ②APPLICATION II





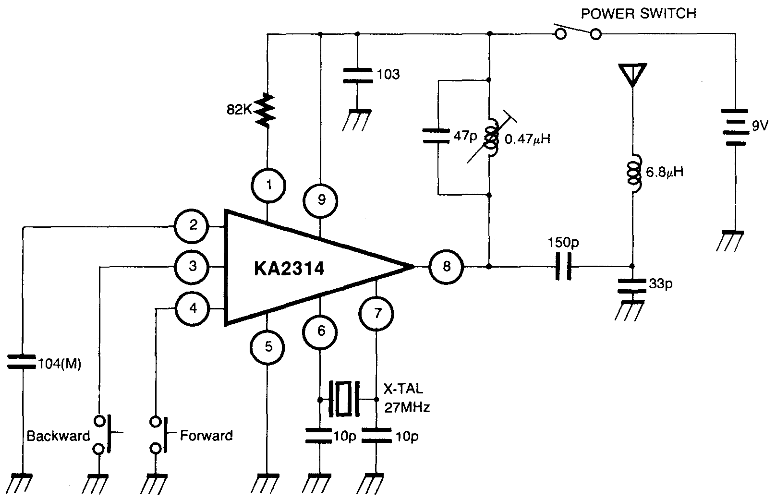
5

• COIL SPECIFICATION

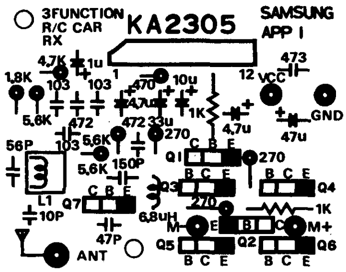


Inductance	Q_o	Turns	f_o (MHz)	Wire
0.52μH ± 10%	60 (min)	6 7/8T	25.2	0.3φ UEW

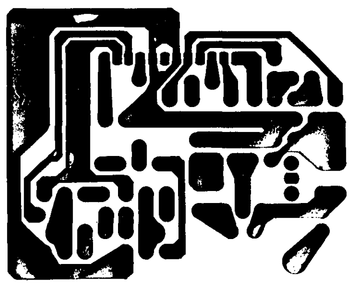
• KA2314 APPLICATION CIRCUIT FOR KA2305A



DEMO BOARD (1:1 SCALE)



(TOP)

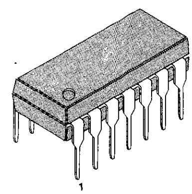


(BOTTOM VIEW)

TOY RADIO CONTROL ACTUATOR (RX)

The KA2306A is a monolithic integrated circuit having 3 functions designed for receiving signals for radio-controlled toy cars.

14 DIP



FEATURES

- **Includes regulator for super regeneration circuit.**
- **Simple 3 functions**
  : forward, backward, stop
- **Wide operating supply voltage range:**
  V_{CC} = 3V ~ 18V
- **Low quiescent circuit current (I_{CC} = 10.5mA: Typ)**
- **Low operating supply voltage (V_{CC} = 3V)**
- **A minimum number of external parts required**
- **Internal TURBO circuit**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2306A	14 DIP	−20 ~ +75°C

BLOCK DIAGRAM

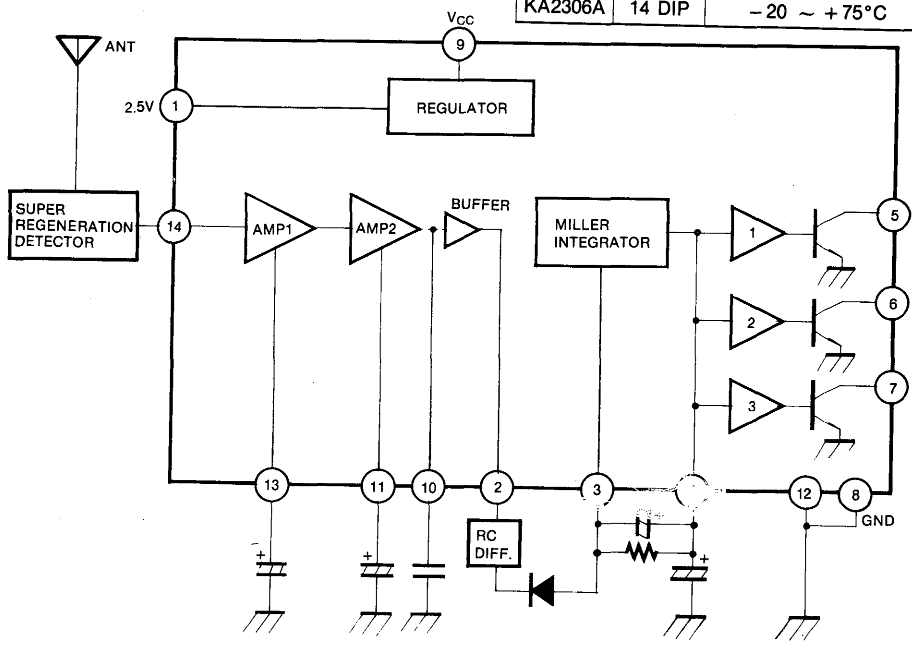


Fig. 1

5

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	20	V
Drive Voltage	V_d	20	V
Drive Current	I_d	40	mA
Regulator Output Current	I_{reg}	15	mA
Power Dissipation	P_d	625	mW
Operating Temperature	T_{opr}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 6V)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Circuit Current	I_{CC}	$V_{CC}=6V$, $V_i=0$		10.5	13.5	mA
Saturation Voltage	$V_5(sat)$	$V_4=0.8V$, $I_5=30mA$		0.9	1.2	V
	$V_6(sat)$	$V_4=2.0V$, $I_6=30mA$				
	$V_7(sat)$	$V_4=1.5V$, $I_7=30mA$				
Regulator Output Voltage	V_{reg}	$V_{CC}=6V$	2.3	2.5	2.7	V
Low Operating Voltage	V_{CCL}	$V_{reg}=2.3V$			3	V
High Operating Voltage	V_{CCH}	$V_{reg}=2.3V(min) \sim 2.7V(max)$	20			V
Sensitivity (V_i = square wave)	$V_5(sen)$	$V_{CC}=6V$, $f=300Hz$		2	4	mV_{p-p}
	$V_6(sen)$	$V_{CC}=6V$, $f=900Hz$				
	$V_7(sen)$	$V_{CC}=6V$, $f=600Hz$				
Voltage Gain	A_V	$V_i=0.8mV_{rms}$, $f=1KHz$	55	58	61	dB

TEST CIRCUIT

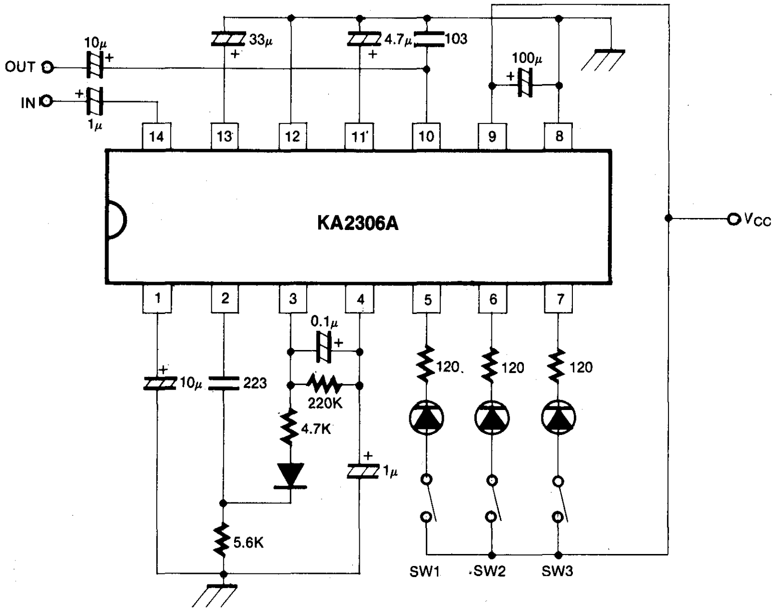


Fig. 2

PIN DESCRIPTION

Pin No.	Symbol	Function
1	V_{reg}	Output of REGULATOR (V_{reg} = 2.5V)
2	BU	Output of BUFFER
3	INT-I	Input of Miller Integrator
4	INT-O	Output of Miller Integrator
5	OUTPUT1	Output of BACKWARD
6	OUTPUT2	Output of TURBO
7	OUTPUT3	Output of FORWARD
8	GND	GND
9	V_{CC}	V_{CC}
10	AMP-0	Output of the 2'nd AMP.
11	BY-2	BY-PASS of the 2'nd AMP.
12	GND	GND
13	BY-1	BY-PASS of the 1'st AMP.
14	INPUT	Signal INPUT

APPLICATION CIRCUIT

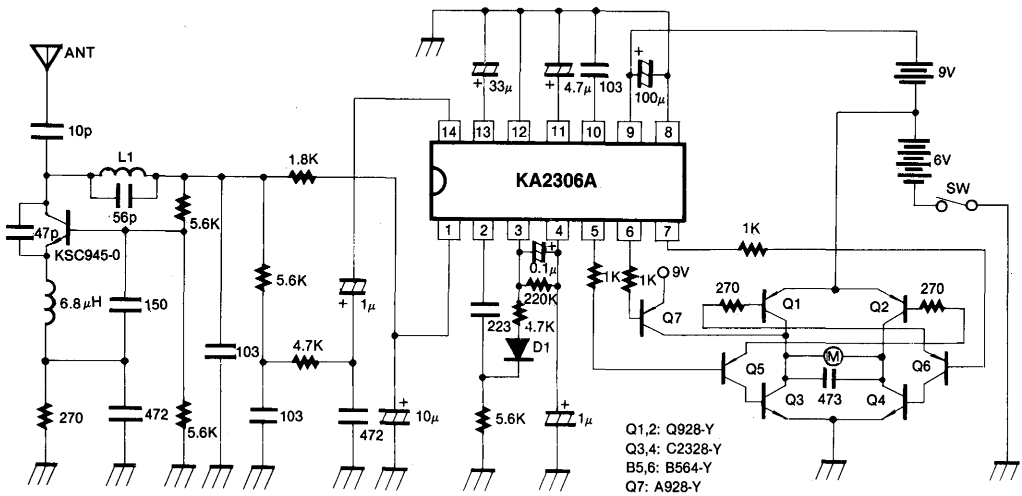


Fig. 3

TRANSMITTER APPLICATION CIRCUIT FOR KA2306A

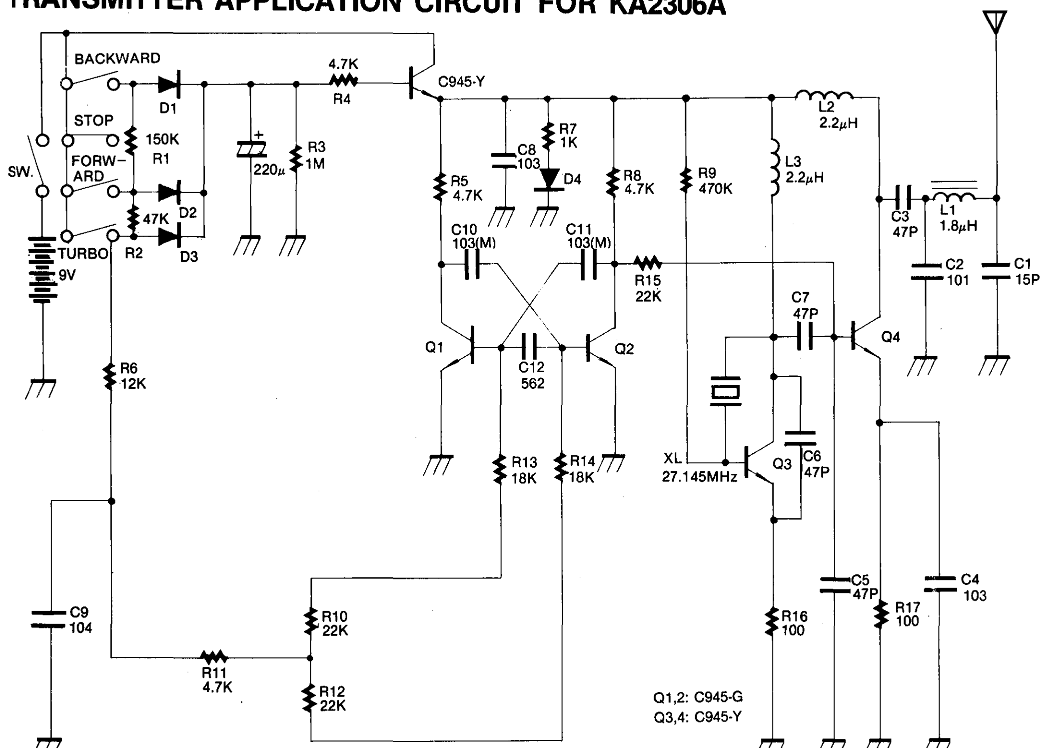
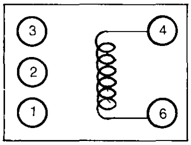


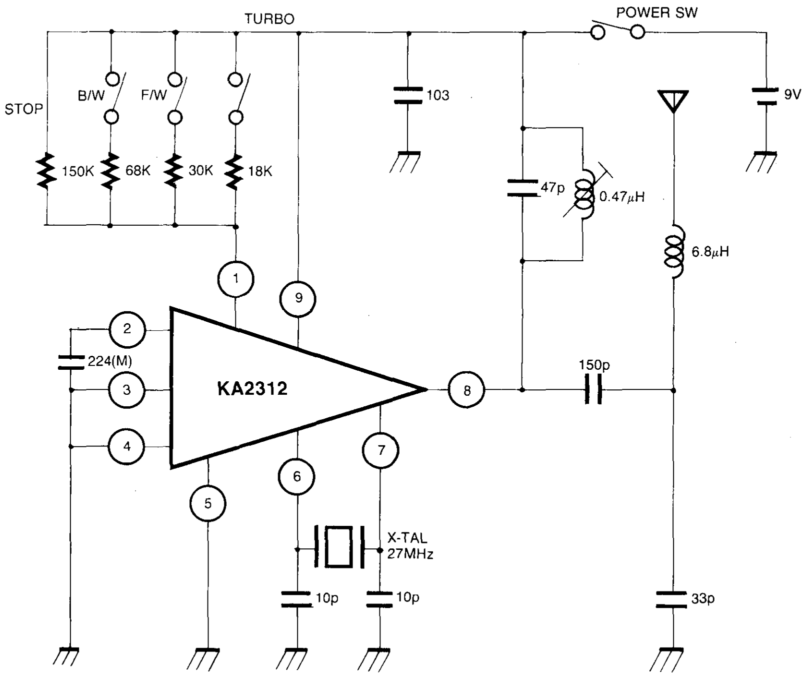
Fig. 4

COIL SPECIFICATION



Inductance	Q_O	Turns	f_O (MHz)	Wire
0.52μH ± 10%	60 (min)	6 7/8T	25.2	0.3φ UEW

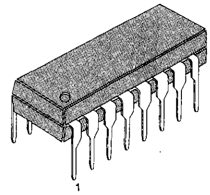
KA2312 APPLICATION CIRCUIT FOR KA2306A



TOY RADIO CONTROL ACTUATOR (RX)

The KA2309 is a monolithic integrated circuit having 7 functions designed for receiving signals for radio-controlled toy cars.
In order to obtain a suitable radio control system for toys, KA2309 (Receiver IC) should be used in combination with a KA2310 (Transmitter IC).

16 DIP



FEATURES

- **Includes regulator, Amp. RC integrator, miller integrator**
- **Wide operating supply voltage range: $V_{CC}=3V \sim 18V$**
- **Low quiescent circuit current ($I_{CC}=10.5mA$: Typ)**
- **Low operating supply voltage ($V_{CC}=3V$)**
- **Minimum number of external parts required (Includes TURBO circuit)**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2309	16 DIP	−20 ~ +75°C

BLOCK DIAGRAM

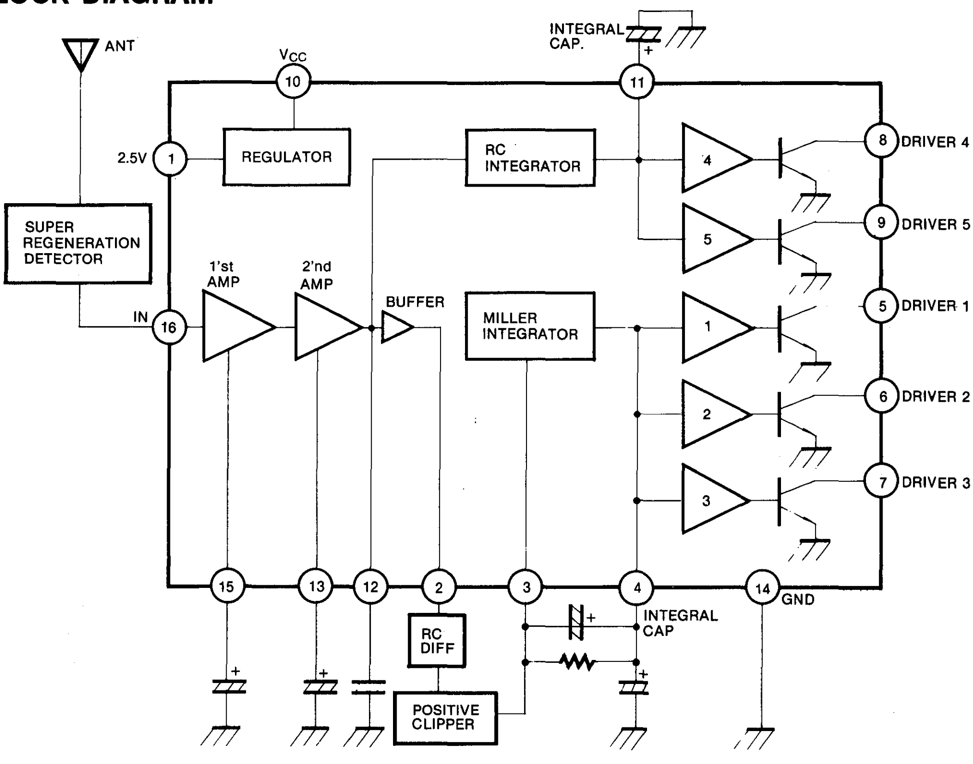
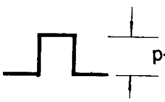


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	20	V
Drive Voltage	V_d	20	V
Drive Current	I_d	40	mA
Regulator Output Current	I_{reg}	15	mA
Power Dissipation	P_d	625	mW
Operating Temperature	T_{opr}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 6V)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Circuit Current	I_{CC}	V_{CC} = 6V, V_i = 0		10.5	13.5	mA
Saturation Voltage	V_5(sat)	f = 300Hz, D_t = 50%				
(V_i = 10m$V_{p\text{-}p}$, I_S = 30mA)	V_6(sat)	f = 900Hz, D_t = 50%				
	V_7(sat)	f = 600Hz, D_t = 50%		0.9	1.2	V
	V_8(sat)	f = 300Hz, D_t = 25%				
	V_9(sat)	f = 900Hz, D_t = 75%				
Regulator Output Voltage	V_{reg}	V_{CC} = 6V	2.3	2.5	2.7	V
Low Voltage Operating	V_{CCL}	V_{reg} = 2.3V			3	V
High Voltage Operating	V_{CCH}	V_{reg} = 2.3V(min) ~ 2.7V(max)	20			V
Sensitivity	V_5(sen)	V_{CC} = 6V, f = 300Hz				
(V_i = square wave)	V_6(sen)	V_{CC} = 6V, f = 900Hz		2	4	m$V_{p\text{-}p}$
	V_7(sen)	V_{CC} = 6V, f = 600Hz				
Voltage Gain	A_V	V_i = 0.8mV_{rms}, f = 1KHz	55	58	61	dB

TEST CIRCUIT

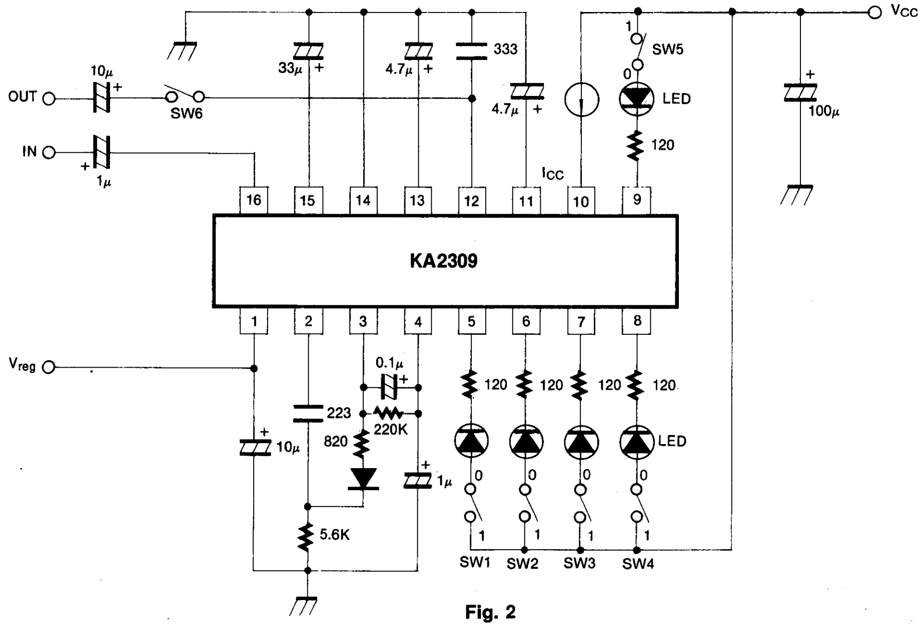


Fig. 2

PIN DESCRIPTION

Pin No.	Symbol	Function
1	V_{reg}	Regulator Output (V_{reg}=2.5V)
2	BU	Buffer Output
3	INT-I	Miller Integrator Input
4	INT-O	Miller Integrator Output
5	D1	Backward Output (I_{sink}=30mA)
6	D2	Turbo Output (I_{sink}=30mA)
7	D3	Forward Output (I_{sink}=30mA)
8	D4	Left Turn Output, DUTY 25% (I_{sink}=30mA)
9	D5	Right Turn Output, DUTY 75% (I_{sink}=30mA)
10	V_{CC}	V_{CC}
11	INT-O	Integrator Output
12	OUT2	The 2'nd AMP Output
13	BY2	The 2'nd AMP By-Pass
14	GND	GND
15	BY1	The 1'st AMP By-Pass
16	IN	Super Regenerator Signal Input

APPLICATION CIRCUIT

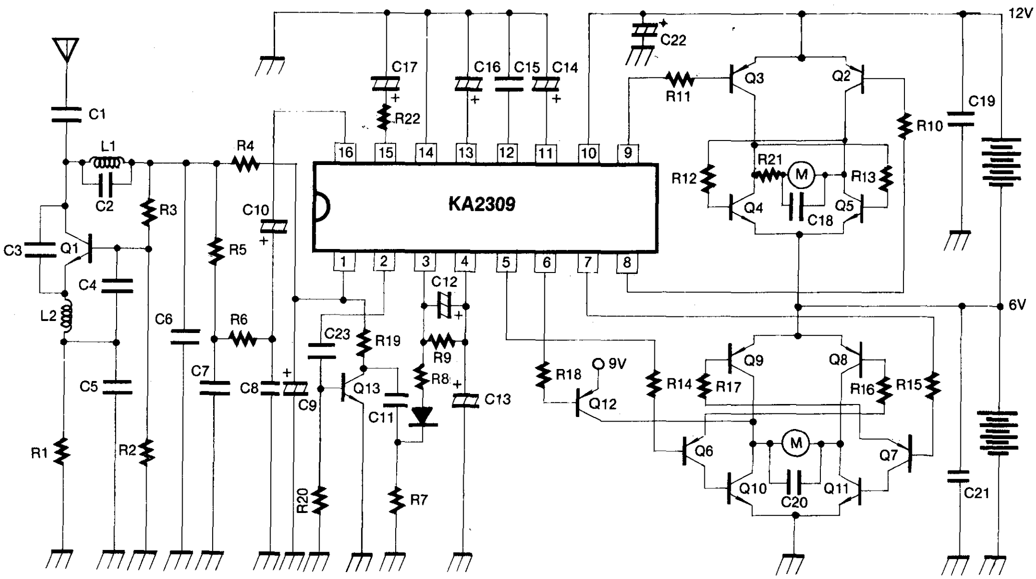


Fig. 3

PARTS LIST & VALUE

Resistors (Unit: Ω)	Capacitors	Transistors	Coil
R1 = 390	C1 = 10pF	Q1 = C838 – O/Y	L1 = tank coil
R2 = 4.7K	C2 = 56pF/4pF	Q2 = B564 – O/Y/G	L2 = 3.3μH
R3 = 5.6K	C3 = 47pF	Q3 = B564 – O/Y/G	
R4 = 1.8K	C4 = 150pF	Q4 = D471 – O/Y/G	
R5 = 5.6K	C5 = 0.0047μF	Q5 = D471 – O/Y/G	
R6 = 4.7K	C6 = 0.01μF	Q6 = B564 – O/Y/G	Diodes
R7 = 5.6K	C7 = 0.01μF	Q7 = B564 – O/Y/G	
R8 = 3.3K	C8 = 0.0047μF	Q8 = B772 – O/Y/G	IN4148
R9 = 150K	C9 = 10μF	Q9 = B772 – O/Y/G	Motors
R10 = 1K	C10 = 4.7μF	Q10 = D882 – O/Y/G	
R11 = 1K	C11 = 0.022μF	Q11 = D882 – O/Y/G	DC motor
R12 = 270	C12 = 0.1μF	Q12 = B772 – O/Y/G	
R13 = 270	C13 = 1μF	Q13 = C945 – O/Y/G	
R14 = 1K	C14 = 4.7μF		
R15 = 1K	C15 = 0.01μF		
R16 = 270	C16 = 4.7μF		
R17 = 270	C17 = 33μF	*C2	
R18 = 100	C18 = 0.056μF	27MHz: 56pF	
R19 = 1.5K	C19 = 0.047μF	49MHz: 4pF	
R20 = 5.6K	C20 = 0.1μF		
R21 = 4.7 (0.5 Watt)	C21 = 0.047μF		
R22 = 470	C22 = 100μF		
	C23 = 0.022μF		

TIME BASE

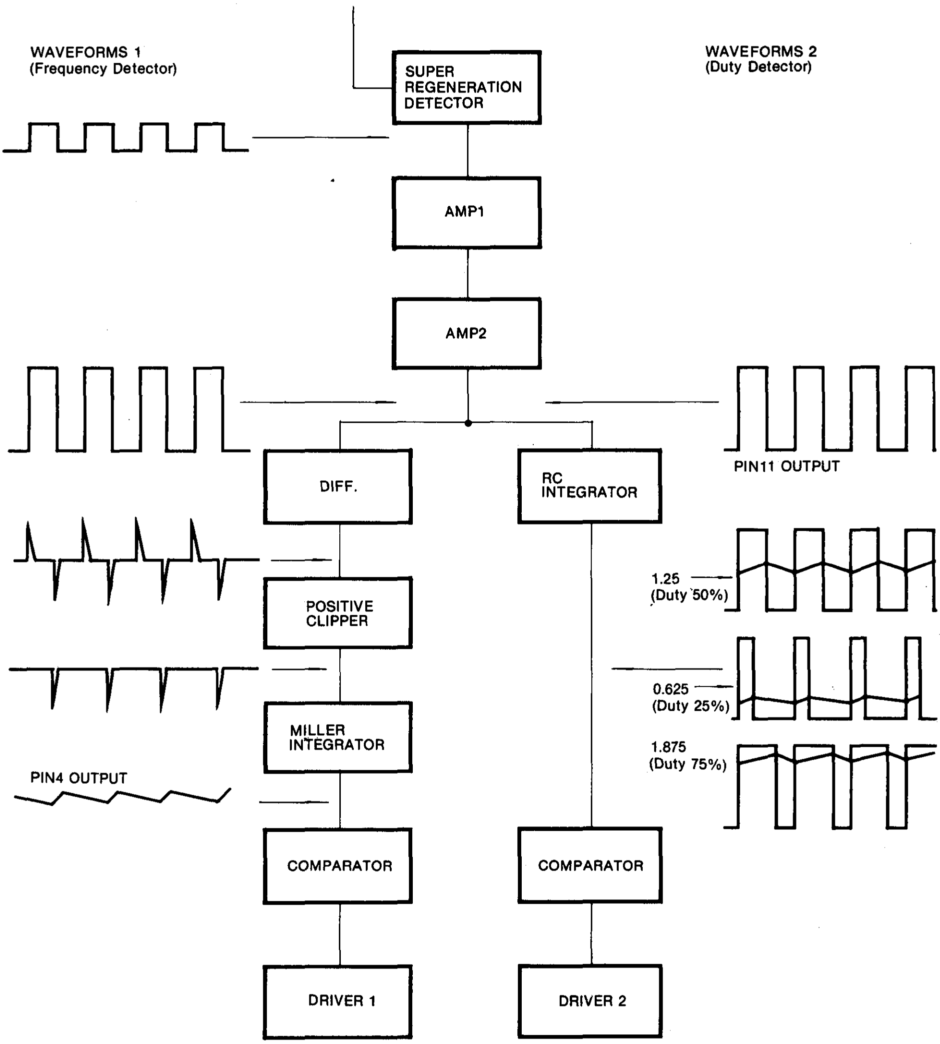


Fig. 4

MODULATION FREQUENCY (TX) & PIN4 DC LEVEL (RX)

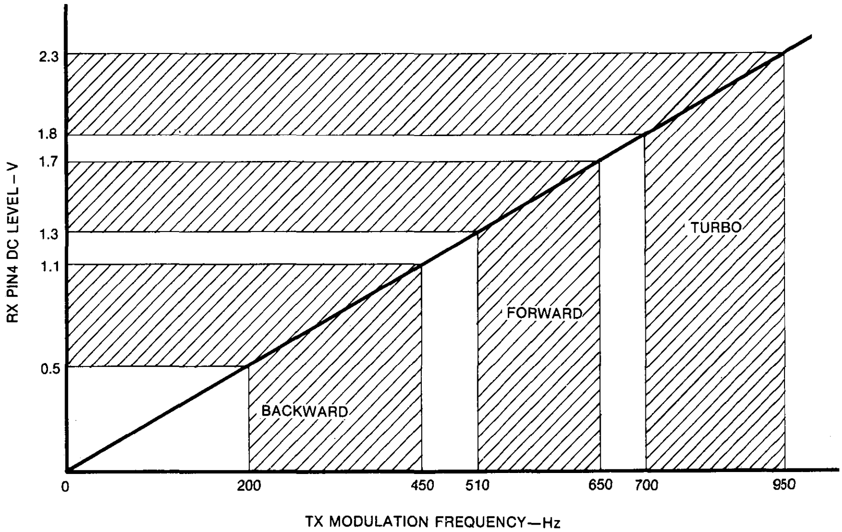


Fig. 5

7 FUNCTION TRANSMITTER APPLICATION CIRCUIT (KA2310)

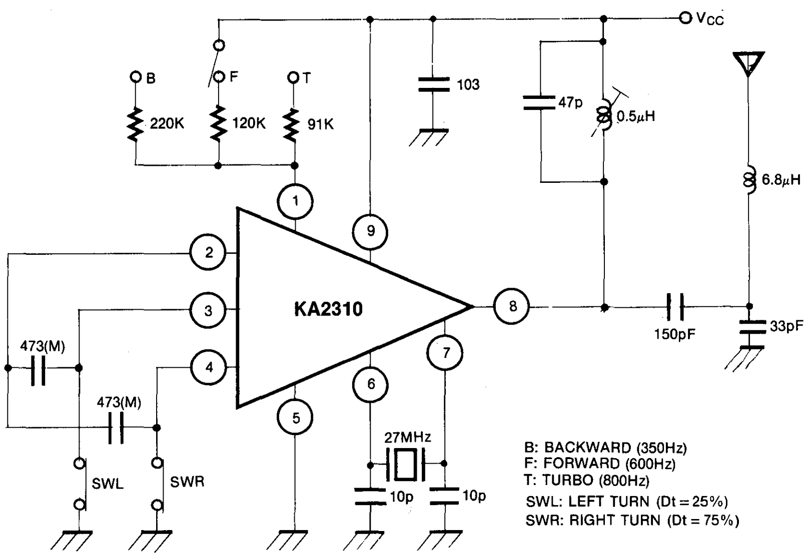
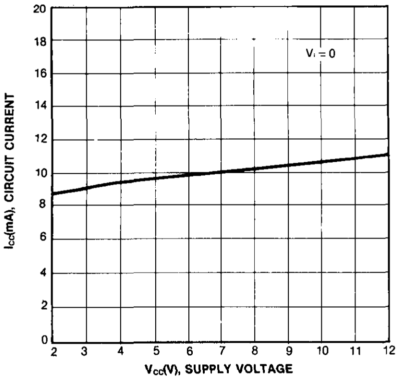


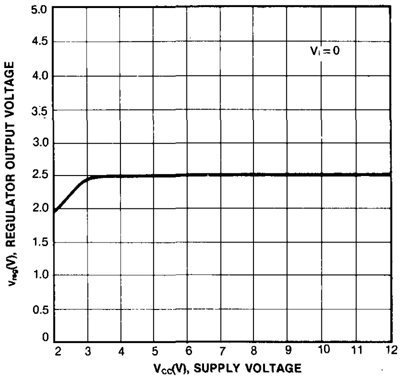
Fig. 6

5

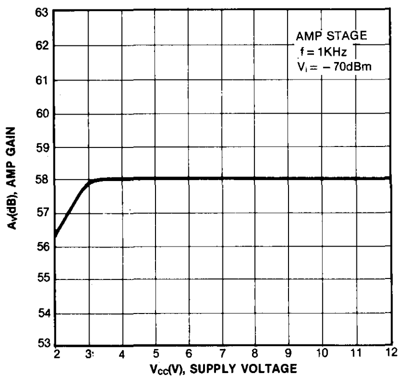
CIRCUIT CURRENT-SUPPLY VOLTAGE



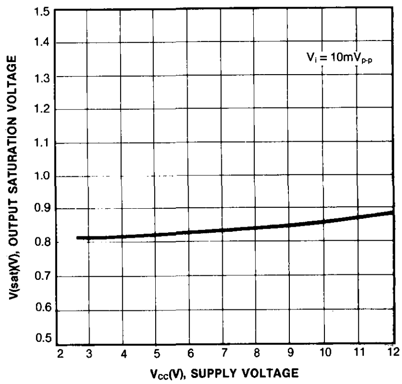
REGULATOR OUTPUT VOLTAGE-SUPPLY VOLTAGE



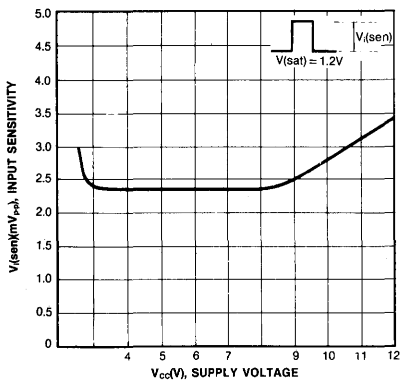
AMP GAIN-SUPPLY VOLTAGE



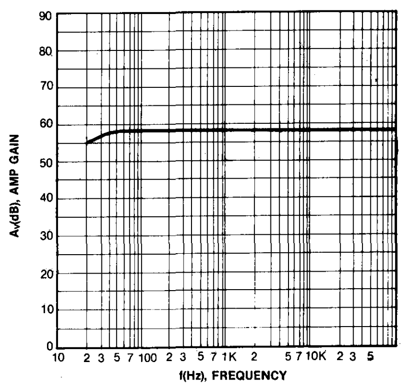
OUTPUT SATURATION VOLTAGE-SUPPLY VOLTAGE



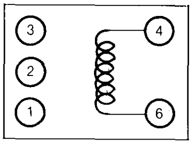
INPUT SENSITIVITY-SUPPLY VOLTAGE



AMP GAIN-FREQUENCY

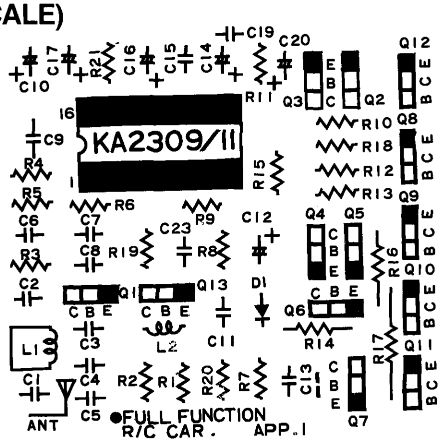


COIL SPECIFICATION

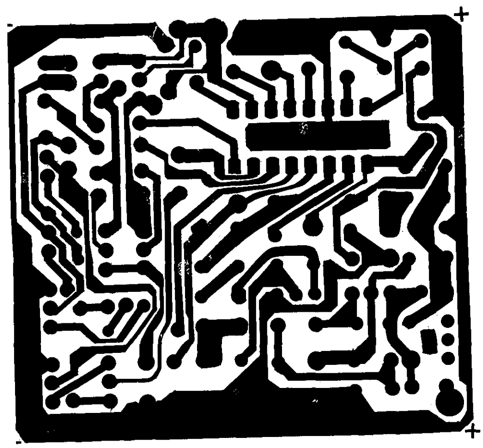


Inductance	Q_O	Turns	f_O (MHz)	Wire
0.52μH ± 10%	60 (min)	6 7/8T	25.2	0.3φ UEW

DEMO BOARD (1:1 SCALE)



(TOP)

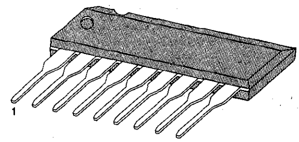


(BOTTOM VIEW)

TOY RADIO CONTROL ACTUATOR (TX)

The KA2310 is a monolithic integrated circuit having 7 functions designed for transmitting signals for radio-controlled toy cars.
In order to obtain a suitable radio control system for toys, the KA2310 (Transmitter IC) should be used in combination with a KA2309 (Receiver IC).

9 SIP



FEATURES

- **Includes Auto power switch,**
  Pulse generator, Modulator
  High frequency amplifier,
  Pulse width controller,
  Transmitting signal oscillator.
- **Wide operating supply voltage range:**
  V_{CC} = 6V ~ 12V
- **Minimum number of external parts required**
- **Low current dissipation**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2310	9 SIP	−20 ~ +70°C

BLOCK DIAGRAM

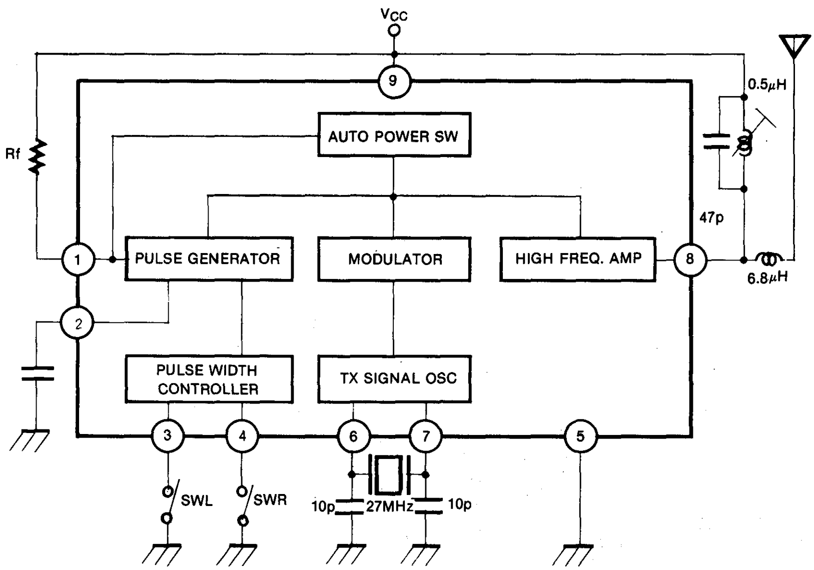


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	12	V
Supply Voltage (PIN 8)	V_8	18	V
Acceptable Load (PIN 8)	R_L	300	Ω
Power Dissipation	P_d	600	mW
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=9V)

Characteristic	Symbol	Test Condition				Test Point	Min	Typ	Max	Unit
		SW1	SW2	SWL	SWR					
Stand By Current	I_{sb}	OFF	OFF	ON	ON	A1		0	0.1	mA
Circuit Current	$I_{CC}(1)$	ON	B	ON	OFF	A1	8	12	17	mA
	$I_{CC}(2)$	ON	B	OFF	ON	A1	10	16	22	mA
	$I_{CC}(3)$	ON	B	ON	ON	A1	10	15	22	mA
Output Sink Current	I_S	ON	A	ON	ON	A2	2	3		mA
Modulation Frequency	fm(1)	ON	A	ON	OFF	F/M		1.8		KHz
	fm(2)	ON	A	ON	ON	F/M		3.6		KHz
Duty Cycle	Dt(1)	ON	A	ON	OFF	F/M	20	25	30	%
	Dt(2)	ON	A	OFF	ON	F/M	70	75	80	%
	Dt(3)	ON	A	ON	ON	F/M	45	50	55	%
Oscillator Frequency	fosc	ON	B	ON	ON	H/F		27		MHz
Transmitting Power	Po(1)	ON	B	fc=27MHz		H/F	15	20		mW
	Po(2)	ON	B	fc=40MHz		H/F		17		mW

TEST CIRCUIT

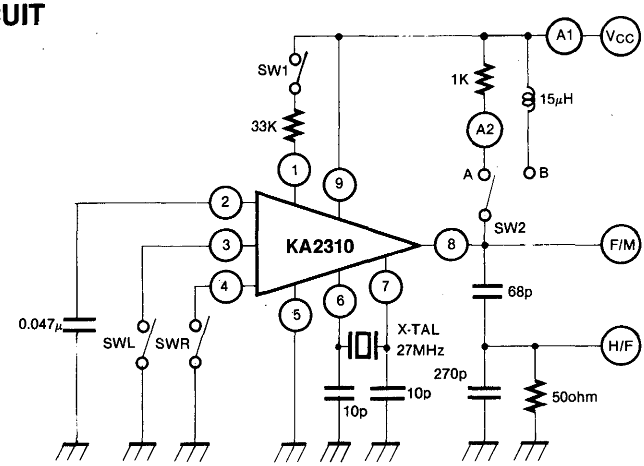


Fig. 2

PIN DESCRIPTION

Pin No.	Symbol	Function
1	PS	Auto Power switch function and modulating signal oscillation. Backward, Turbo, Forward input (DUTY 50%)
2	FM	Modulating signal oscillation.
3	DL	Translation pulse width of modulating signal. Left turn input (DUTY 25%)
4	DR	Translation pulse width of modulating signal. Right turn input (DUTY 75%)
5	GND	GND
6	FC1	Transmitting signal oscillation.
7	FC2	Transmitting signal oscillation.
8	V_O	The output signal of modulating and transmitting.
9	V_{CC}	V_{CC} (6-12V)

APPLICATION CIRCUIT

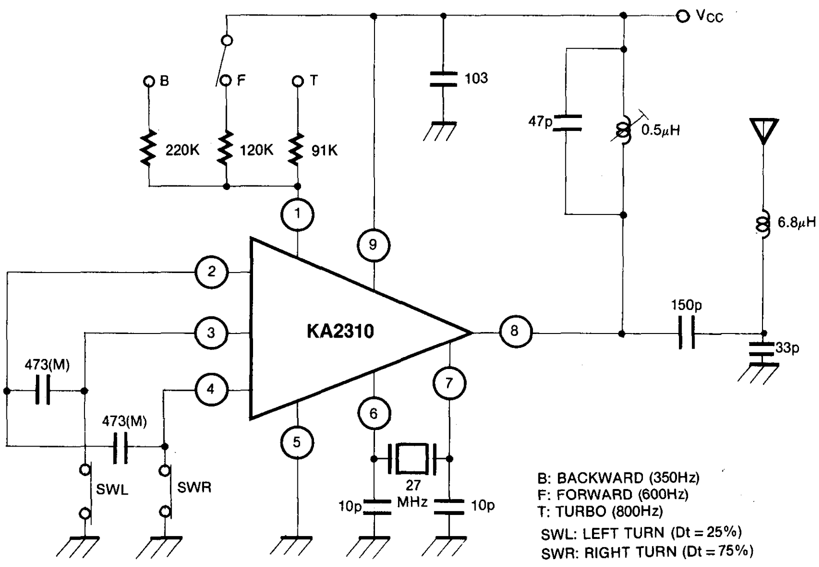
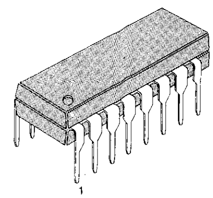


Fig. 3

TOY RADIO CONTROL ACTUATOR (RX)

The KA2311 is monolithic integrated circuit having full functions designed for receiving signals for radio-controlled toy cars.
In order to obtain a suitable radio control system for toys, the KA2311 (Receiver IC) should be used in combination with a KA2312 (Transmitter IC).

16 DIP



FEATURES

- It is possible to turn left or right on stop state.
- Includes Regulator, Amp, Duty Integrator, Miller Integrator
- Wide operating supply voltage range: V_{CC} = 3V ~ 18V
- Low operating supply voltage (V_{CC} = 3V)
- A Minimum number of external parts are required (Includes turbo circuit)

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2311	16 DIP	−20 ~ +75°C

BLOCK DIAGRAM

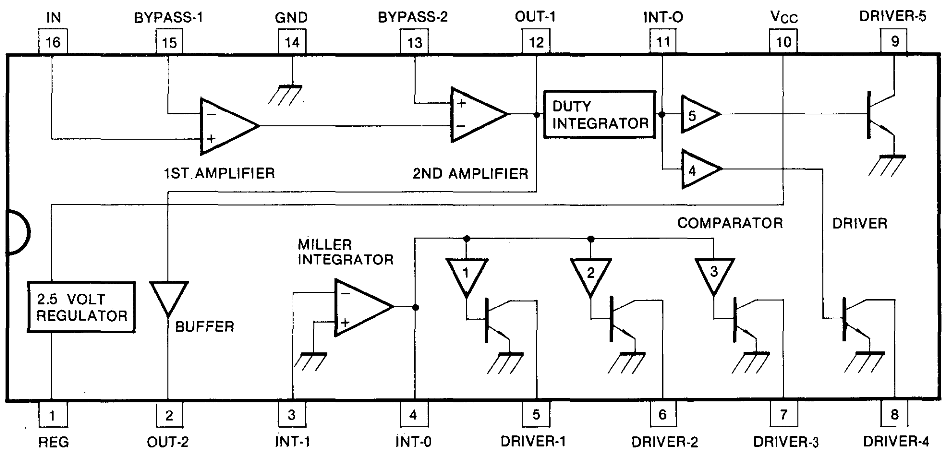


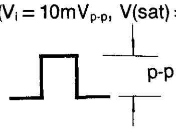
Fig. 1

5

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Condition	Value	Unit
Supply Voltage	V_{CC}	V_1 = 2.3V ~ 2.7V	20	V
Drive Voltage	V_d	I_{LK} = 100μA	20	V
Drive Current	I_d	V_{sat} = 1.2V	150	mA
Regulator Output Current	I_{reg}	V_1 = 2.3V	20	mA
Power Dissipation	P_d		625	mW
Operating Temperature	T_{opr}		−20 ~ +75	°C
Storage Temperature	T_{stg}		−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 6V)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Circuit Current	I_{CC}	V_{CC} = 6V, V_i = 0		15	20	mA
Leakage Current	I_{LK}	V_{CC} = 6V, V_i = 0		0	100	μA
Saturation Current (V_i = 10m$V_{p\text{-}p}$, V(sat) = 1.2V) 	I_5(sat)	f = 300Hz, V_5(sat) = 1.2V	100	150		mA
	I_6(sat)	f = 900Hz, V_6(sat) = 1.2V				
	I_7(sat)	f = 600Hz, V_7(sat) = 1.2V				
	I_8(sat)	f = 900Hz, V_8(sat) = 1.2V				
	I_9(sat)	f = 300Hz, V_9(sat) = 1.2V				
Regulator Output Voltage	V_{reg}	V_{CC} = 6V	2.3	2.5	2.7	V
Low Voltage Operating	V_{CCL}	V_{reg} = 2.3V			3	V
High Voltage Operating	V_{CCH}	V_{reg} = 2.3(min) ~ 2.7V(max)	20			V
Sensitivity (V_i = square wave)	V_5(sen)	V_{CC} = 6V, f = 300Hz		2	4	m$V_{p\text{-}p}$
	V_6(sen)	V_{CC} = 6V, f = 900Hz				
	V_7(sen)	V_{CC} = 6V, f = 600Hz				
Voltage Gain	A_V	Vi = 0.3mV_{rms}, f = 1KHz	60	65	70	dB

TEST CIRCUIT

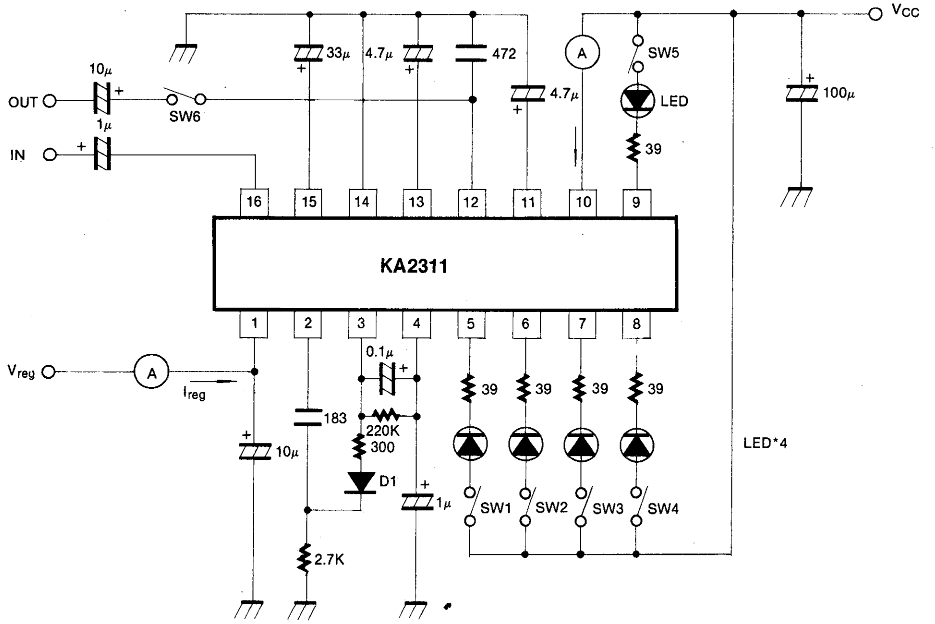


Fig. 2

PIN DESCRIPTION

Pin No.	Symbol	Function
1	V_{reg}	Regulator Output ($V_{reg}=2.5V$)
2	BU	Buffer Output
3	INT-I	Miller Integrator Input
4	INT-O	Miller Integrator Output
5	D1	Backward Output ($I_{sink}=30mA$)
6	D2	Turbo Output ($I_{sink}=30mA$)
7	D3	Forward Output ($I_{sink}=30mA$)
8	D4	Left Turn Output, DUTY 25% ($I_{sink}=30mA$)
9	D5	Right Turn Output, DUTY 75% ($I_{sink}=30mA$)
10	V_{CC}	V_{CC}
11	INT-O	Integrator Output
12	OUT2	The 2'nd AMP Output
13	BY2	The 2'nd AMP By-Pass
14	GND	GND
15	BY1	The 1'st AMP By-Pass
16	IN	Super Regenerator Signal Input

APPLICATION CIRCUIT

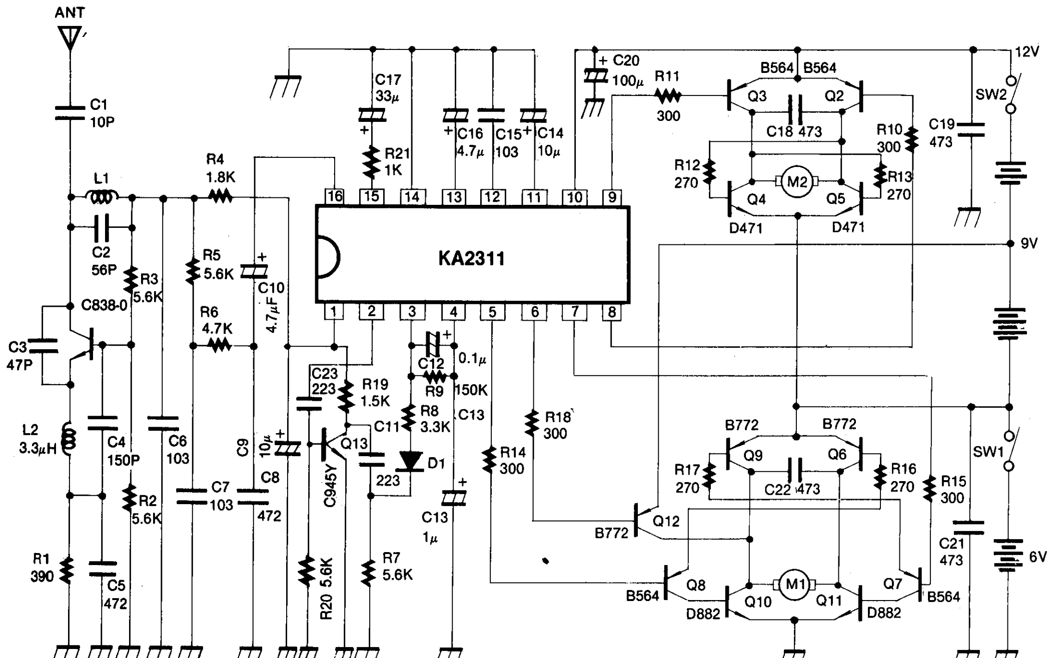


Fig. 3

TRANSMITTER APPLICATION CIRCUIT FOR KA2311

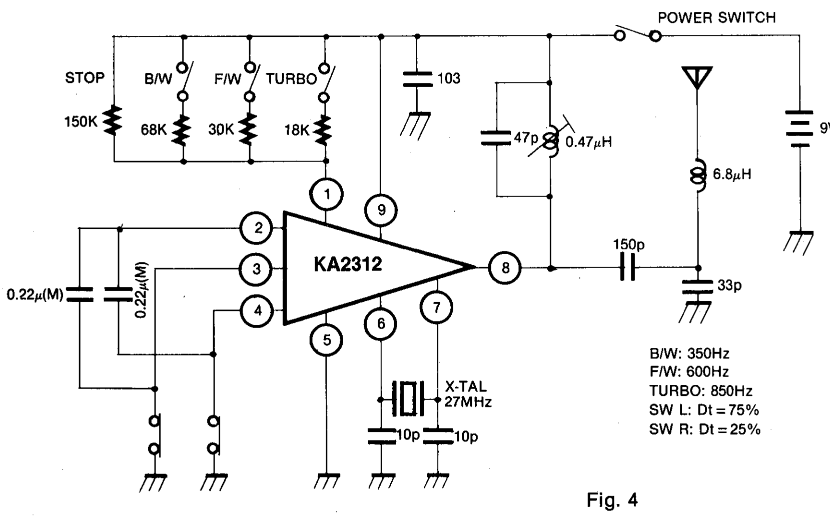


Fig. 4

TIME BASE

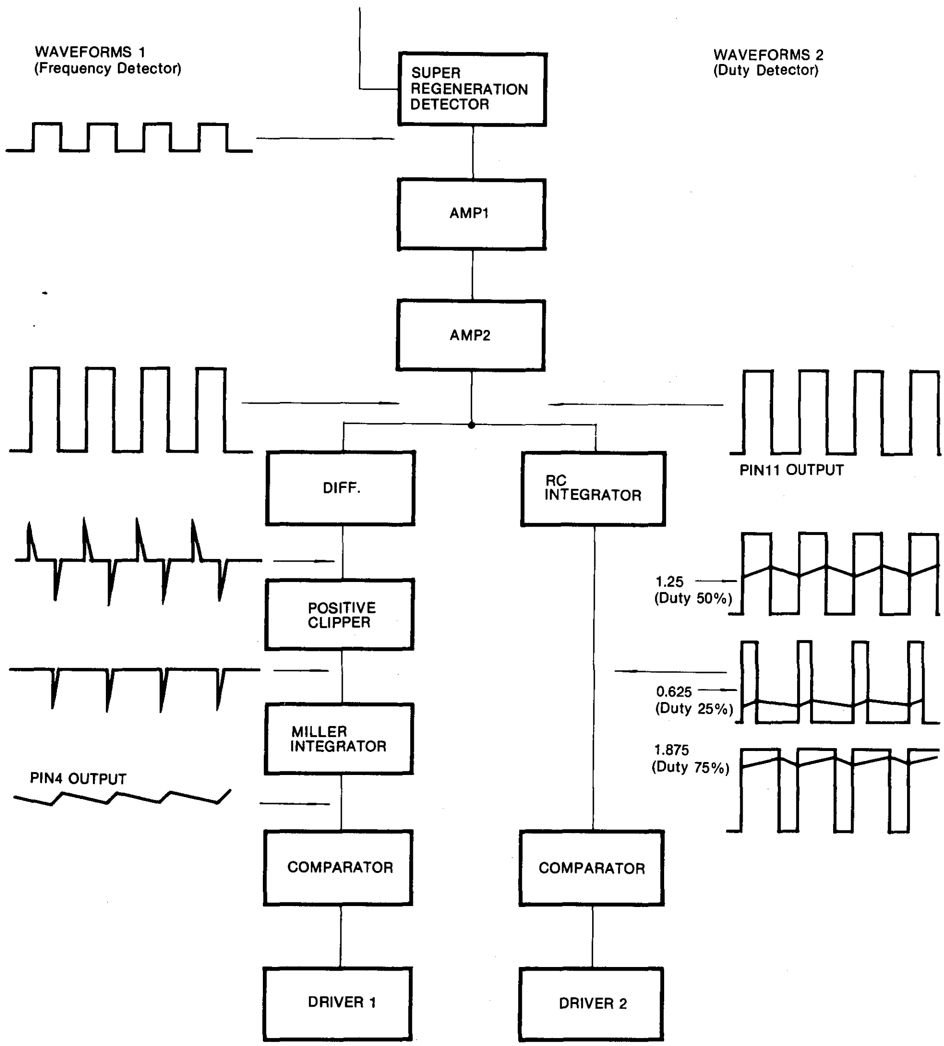
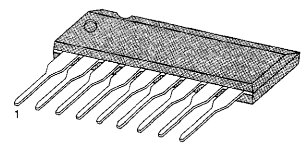


Fig. 4

TOY RADIO CONTROL ACTUATOR (TX)

The KA2312 is monolithic integrated circuit having full functions designed for transmitting signals for radio controlled toy cars.
In order to obtain a suitable radio control system for toys, the KA2312 (Transmitter IC) should be used in combin ation with a KA2311 (Receiver IC).

9 SIP



FEATURES

- **Includes Pulse generator, Modulator**
  High frequency amplifier,
  Pulse width controller,
  Transmitting signal oscillator.
- **Wide operating supply voltage range:**
  $V_{CC}=6V \sim 12V$
- **Minimum number of external parts required**
- It is possible for the user to select the modulating frequency

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2312	9 SIP	$-20 \sim +70°C$

BLOCK DIAGRAM

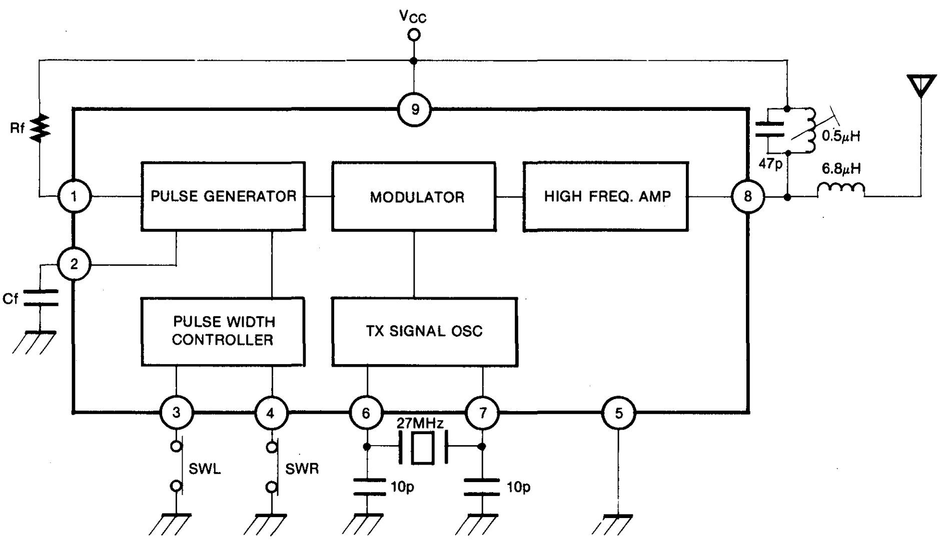


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	12	V
Supply Voltage (PIN 8)	V_8	18	V
Acceptable Load (PIN 8)	R_L	300	Ω
Power Dissipation	P_d	600	mW
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 9V)

Characteristic	Symbol	Test Condition				Test Point	Min	Typ	Max	Unit
		SW1	SW2	SWL	SWR					
Circuit Current	$I_{CC}(1)$	OFF	B	ON	ON	A1	15	20	25	mA
	$I_{CC}(2)$	ON	B	ON	OFF	A1	13	18	23	mA
	$I_{CC}(3)$	ON	B	OFF	ON	A1	7	12	17	mA
	$I_{CC}(4)$	ON	B	ON	ON	A1	11	16	21	mA
Output Sink Current	I_S	ON	A	ON	ON	A2	2	5	8	mA
Modulation Frequency	fm(1)	ON	A	ON	OFF	F/M		2		KHz
	fm(2)	ON	A	ON	ON	F/M		4		KHz
Duty Cycle	Dt(1)	ON	A	ON	OFF	F/M	70	75	80	%
	Dt(2)	ON	A	OFF	ON	F/M	20	25	30	%
	Dt(3)	ON	A	ON	ON	F/M	45	50	55	%
Oscillator Frequency	fosc	ON	B	ON	ON	H/F		27		MHz
Transmitting Power	Po(1)	ON	B	fc = 27MHz		H/F	15	20		mW
	Po(2)	ON	B	fc = 40MHz		H/F		17		mW

TEST CIRCUIT

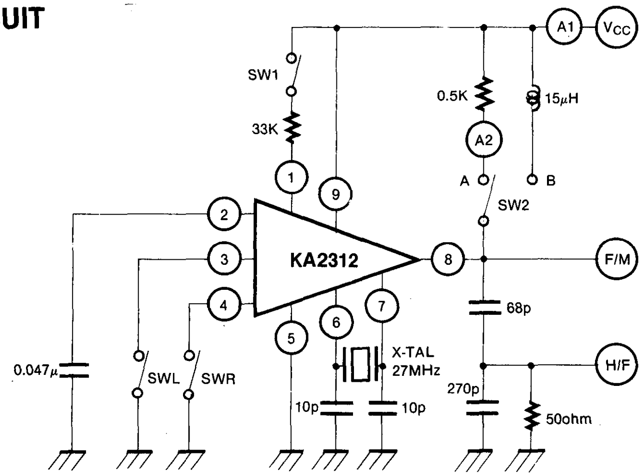


Fig. 2

PIN DESCRIPTION

Pin No.	Symbol	Function
1	FM1	Modulating signal oscillation. Backward, Turbo, Forward input (DUTY 50%)
2	FM2	Modulating signal oscillation.
3	DL	Translation pulse width of modulating signal. Left turn input (DUTY 75%)
4	DR	Translation pulse width of modulating signal. Right turn input (DUTY 25%)
5	GND	GND
6	FC1	Transmitting signal oscillation.
7	FC2	Transmitting signal oscillation.
8	V_O	The output signal of modulating and transmitting.
9	V_{CC}	V_{CC} (6-12V)

APPLICATION CIRCUIT Fig. 3 KA2312

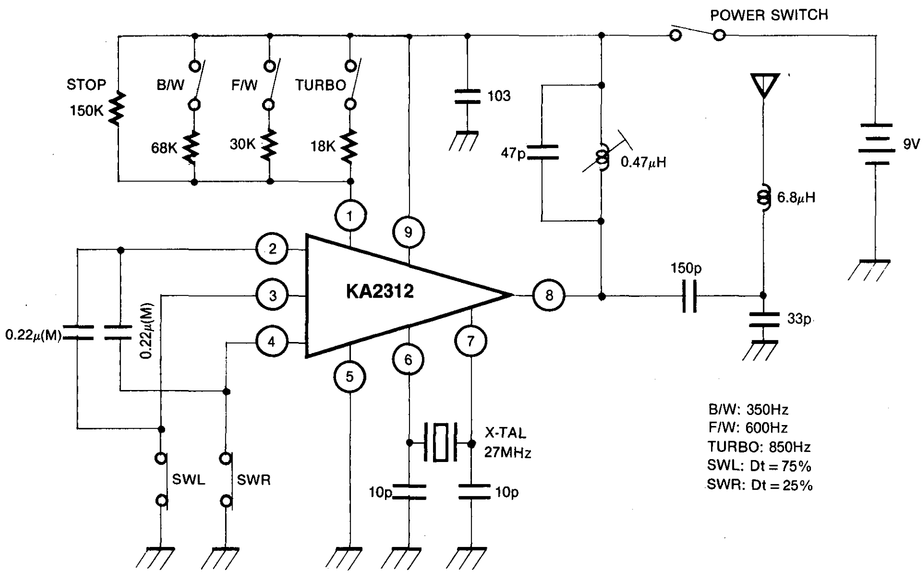
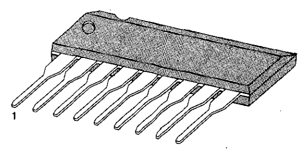


Fig. 3

TOY RADIO CONTROL ACTUATOR (TX)

The KA2314 is an integrated circuit designed to transmitter of full function R/C toy car which consists of a pulse generator, pulse width controller, modulator, TX signal osc, and high frequency amp. The KA2314 TX IC is used as one kit with the KA2311 (or KA2309) RX IC. The main application is a TX set of full function R/C toy car or some other kinds of TX for R/C toy car.

9 SIP



FEATURES

- **Includes Pulse generator, Modulator High frequency amplifier, Pulse width controller, Transmitting signal oscillator.**
- **Wide operating supply voltage range: V_{CC} = 6V ~ 12V**
- **Minimum number of external parts required**
- **It is possible for user to select modulating frequency**
- **It is possible of applicate for GUN TX. (The duty SW is open method)**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2314	9DIP	- 20 ~ + 70°C

BLOCK DIAGRAM

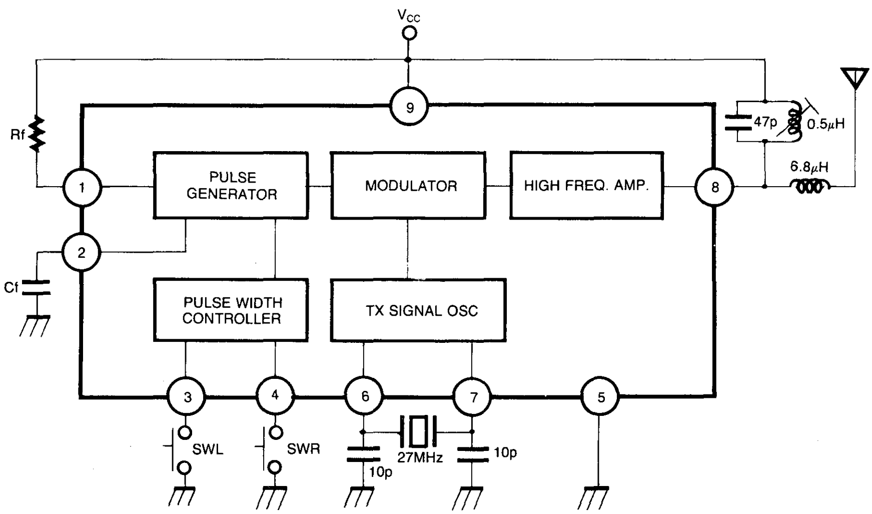


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	12	V
Supply Voltage (PIN 8)	V_a	18	V
Acceptable Load (PIN 8)	R_L	300	Ω
Power Dissipation	P_d	600	mW
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature Range	T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 9V)

Characteristic	Symbol	Test Condition				Test Point	Min	Typ	Max	Unit
		SW1	SW2	SWL	SWR					
Circuit Current	$I_{CC}(1)$	OFF	B	ON	ON	A1	15	20	25	mA
	$I_{CC}(2)$	ON	B	ON	OFF	A1	13	18	23	mA
	$I_{CC}(3)$	ON	B	OFF	ON	A1	7	12	17	mA
	$I_{CC}(4)$	ON	B	ON	ON	A1	11	16	21	ma
	$I_{CC}(5)$	ON	B	OFF	OFF	A1	11	16	21	mA
Output Sink Current	I_S	ON	A	ON	ON	A2	2	5	8	mA
Modulation Frequency	fm(1)	ON	A	ON	OFF	F/M		2		KHz
	fm(2)	ON	A	ON	ON	F/M		4		KHz
	fm(3)	ON	A	OFF	OFF	F/M		1.5		KHz
Duty Cycle	Dt(1)	ON	A	ON	OFF	F/M	20	25	30	%
	Dt(2)	ON	A	OFF	ON	F/M	70	75	80	%
	Dt(3)	ON	A	ON	ON	F/M	45	50	55	%
	Dt(4)	ON	A	OFF	OFF	F/M	45	50	55	%
Oscillator Frequency	f_{OSC}	ON	B	ON	ON	H/F		27		MHz
Transmitting Power	$P_O(1)$	ON	B	f_C = 27MHz		H/F	15	20		mW
	$P_O(2)$	ON	B	f_C = 40MHz		H/F		17		mW

TEST CIRCUIT

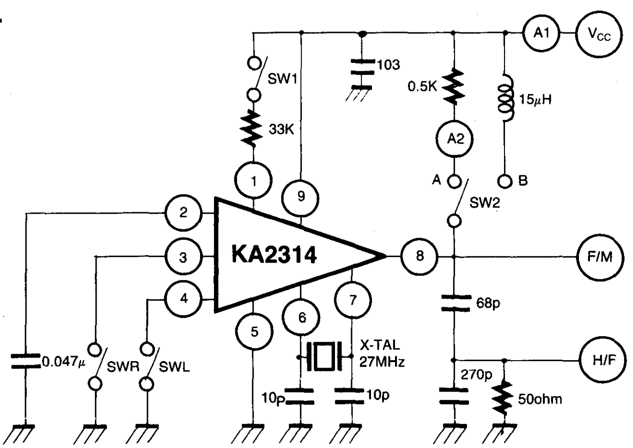


Fig. 2

PIN DESCRIPTION

Pin No.	Symbol	Function
1	FM1	Modulating signal oscillation. Backward, Turbo, Forward Input (DUTY 50%)
2	FM2	Modulating signal oscillation.
3	DL	Translation pulse width of modulating signal. Left turn input (DUTY 25%)
4	DR	Translation pulse width of modulating signal. Right turn input (DUTY 75%)
5	GND	GND
6	FC1	Transmitting signal oscillation.
7	FC2	Transmitting signal oscillation.
8	V_O	The output signal of modulating and transmitting.
9	V_{CC}	V_{CC} (6-12V)

APPLICATION CIRCUIT AND DESCRIPTION

1) APPLICATION CIRCUIT FOR KA2311 (Duty SW: Open type)

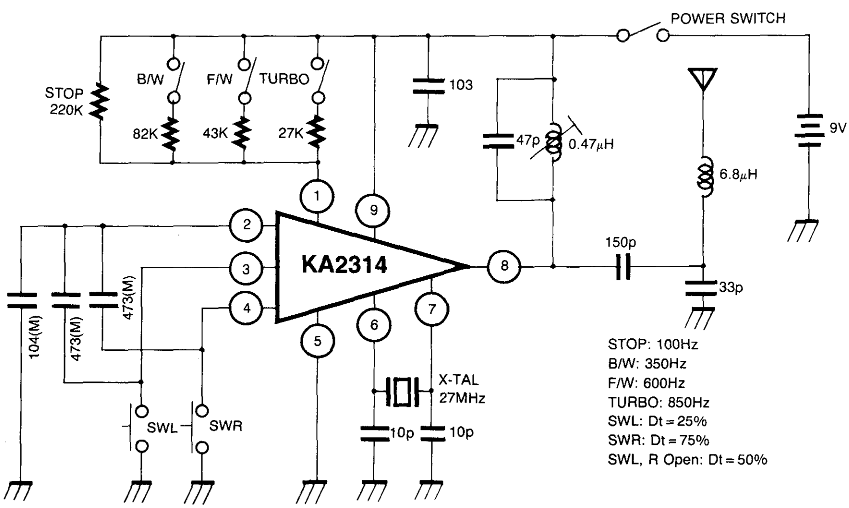


Fig. 3

2) DESCRIPTION (Duty SW: Open type)

Modulation frequency is determined by both external resistor of pin 1 and capacitor of pin 2. Therefore the modulation frequency according to their functions depends on the resistor of pin 1. Duty percent is determined by pin 3, pin 4 and when both pin 3, pin 4 are open. Duty percent is 50%. When pin 3 open and pin 4 GND, Duty 75%. When pin 3 GND and pin 4 open, then Duty percent becomes 25%. In the case of both pin 3, pin 4 open, the modulation frequency appears low value compared with that of Duty 25% or 75%. In order to obtain the same value of frequency, for this reason, the external proper capacitor must be connected in parallel to the pin 2. X-TAL, which has the equal value of the desired RF signal, must be connected between pin 6 and pin 7. When 27MHz X-TAL is used, 10pF capacitor should be connected between both pins and GND, but when 49MHz X-TAL, 10pF capacitor may be connected between pin 6 and GND. Through these preparations, when the desired signal is made completely then outputted through pin 8. Output level of pin 8 can be optimized by controlling the tank coil between pin 8 and V_{CC}.

① DUTY FUNCTION

DUTY SW		DUTY	FUNCTION	OUTPUT WAVEFORM
SW L	SW R			
OFF	OFF	50%	STOP, B/W, F/W, TURBO	
ON	OFF	25%	LEFT TURN	
OFF	ON	75%	RIGHT TURN	

② MODULATION FREQUENCY

FUNCTION	STOP	B/W	F/W	TURBO
fm (Hz)	100	350	600	850

3) APPLICATION CIRCUIT FOR KA2311 (Duty SW: Short type)

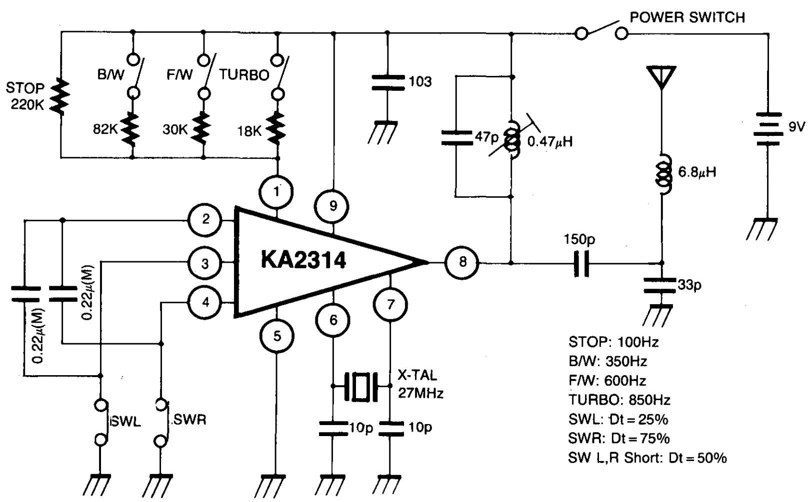


Fig. 4

4) APPLICATION CIRCUIT FOR KA2309 (Duty SW: Open type)

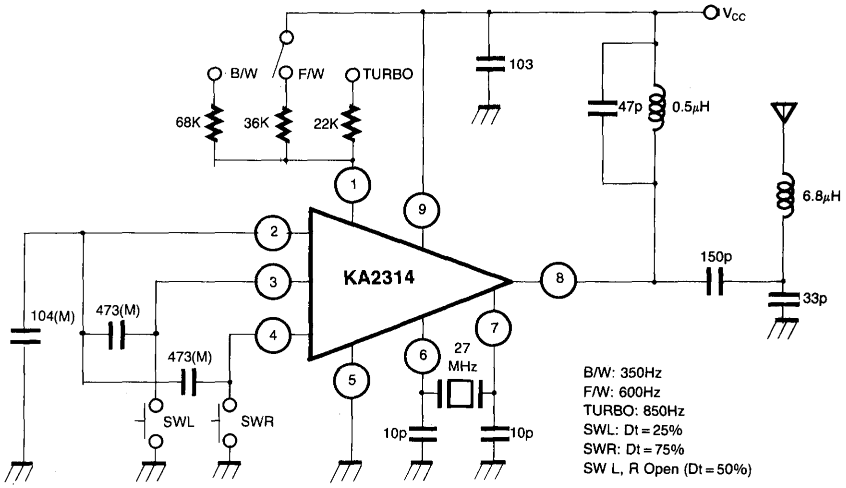


Fig. 5

ATTENTION FOR PROPER USAGE

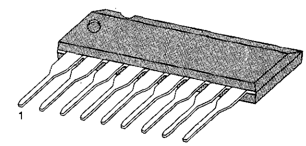
1) It is desirable that the lowest error capacitor connected to pin 2 should be used in order to get the stable modulation frequency characteristics. (below ±2% recommended)
   Mylar capacitor is better than electrolytic capacitor in characteristics. If a high error capacitor is used, the deviation of modulation frequency appears severe according to the individual device.
2) In case that the transmitted signal was over the occupied band width (20KHz/Max) of FCC standard, the modulation frequency should be lowered and used.
3) In the event of mismatching impedance between the external transmitter ANT and output circuit, duty cycle may be changed. At this event, it is necessary that the choke coil, which is connected to the TX ANT in tandem, should be changed to another one.
   (27MHz – 6.8μH, 49MHz – 2.2μH recommended).

KA2303 APPLICATION NOTE

1. INTRODUCTION

The KA2303 is an integrated circuit intend to drive remote controlled toy cars. By obtaining the 27MHz (or 49MHz) non-modulated signal from wireless transmitter through a super regenerative detection circuit, the IC is designed to control the 3 functions (forward, stop, backward) of the DC motor.

The circuit consists of amplifier, detector, comparator, latch, driver, and regulator. Reduced components surrounding the circuit enable an easily-designed circuit.



2. BLOCK DIAGRAM AND OPERATIONAL OF EACH BLOCK

1) A SIMPLIED BLOCK DIAGRAM AND OPERATION

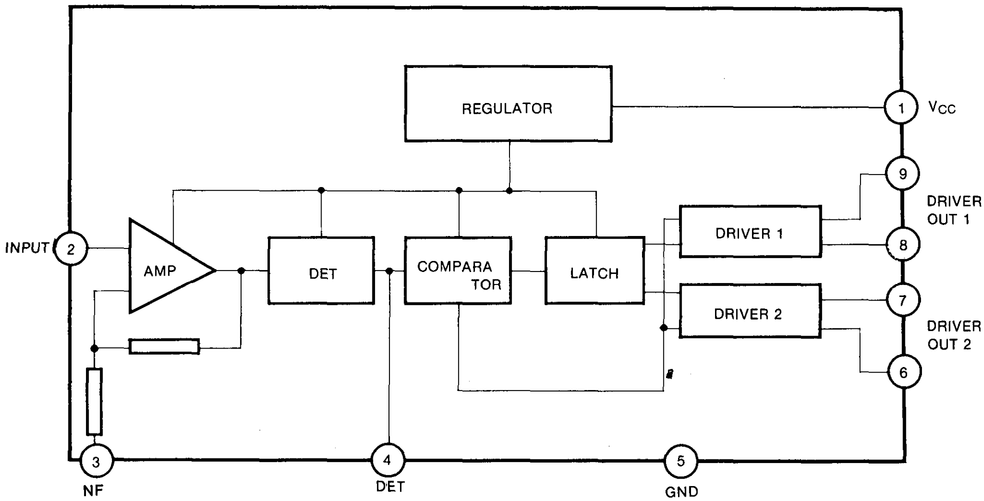


Fig. 1

A) AMPLIFIER : As an AC amplifier, it only amplifies noise signals within an audio frequency range.
B) DETECTOR : With capacitor connected to Pin 4, a peak detector is formed. The low frequency noise signal amplified in the previous block is converted into DC.
C) COMPARATOR : A schmitter trigger circuit with hysteresis characteristic.
D) LATCH : Through the switching operation, it generates the signal to determine the direction of the motor.
E) DRIVER 1, 2 : With output from direction control circuit, the driver 1 & 2 control the direction of the motor. The motor is connected to Pins 6—9.
F) REGULATOR : As a constant voltage supplier circuit, it stabilizes the operation of the device against the ripple and noise generated when the motor is set.

2) DETAILED BLOCK DIAGRAM AND OPERATION DESCRIPTION

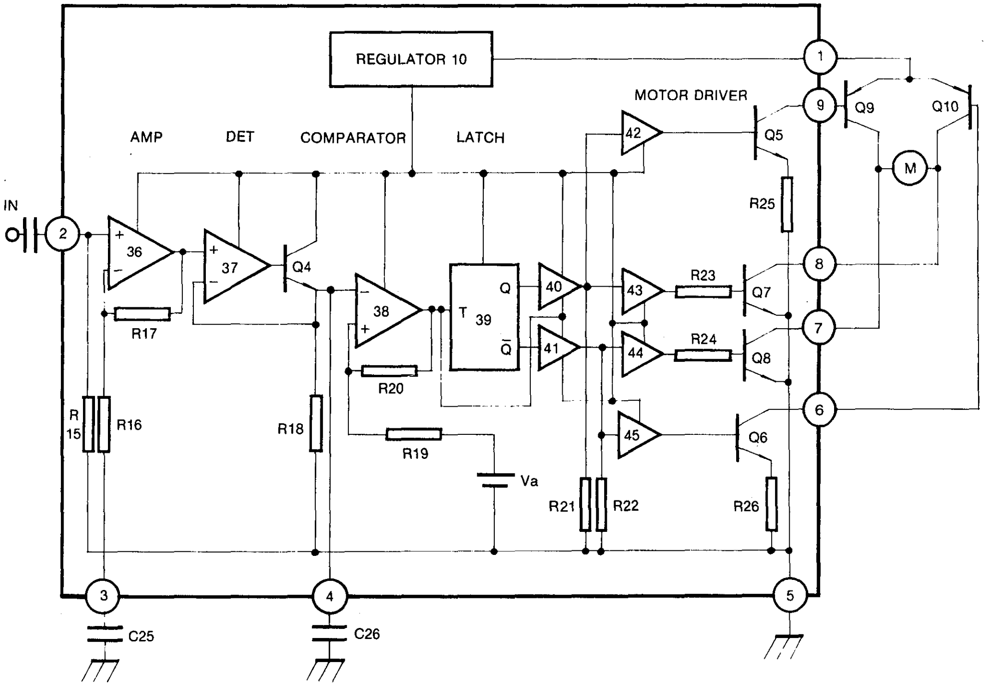


Fig. 2

A) AMPLIFIER
  a) Consists of operational amplifier (36), resistors (R25, R16 and R17), and a capacitor C25.
  b) Input signal is fed to a non-inverting terminal (+) of the operational amplifier.
  c) Since Pin 3 couples with capacitor C25, DC output is kept "0" in spite of offset voltage of operational amplifier.
  d) Amplification rate of alternative voltage should be (R17/R16) + 1.

B) DETECTOR
  a) Consists of operational amplifier (37), Transistor Q4, Resistor R18 and Capacitor C26.
  b) The output voltage of the amplifier stage is supplied to the non-inverting terminal (+) of the operational amplifier, while the terminal voltage of capacitor C26 is fed to the inverting terminal (−).
  c) When input voltage of the non-inverting terminal is bigger than that of the inverting terminal, transistor Q4 is turned on and the output voltage of the operational amplifier is charged to capacitor C26.
  d) If the condition of input voltage is reversed to c), Transistor Q4 is turned off while the voltage charged at capacitor C26 is discharged through resistor R18.
  e) As a result, the low frequency peak voltage fed to the non-inverting terminal of the operational amplifier is detected at this stage.

C) COMPARATOR

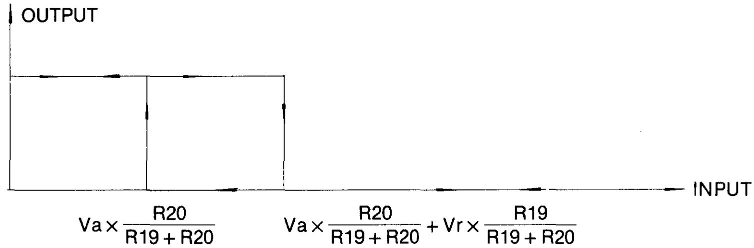
a) Consists of operational amplifier (38), resistors (R19 and R20) and reference voltage (Va).

b) When the comparator output is high (Vr), the input voltage becomes:

$$Va \times \frac{R20}{R19 + R20}$$

c) If the comparator output is low, the input voltage is:

$$Va \times \frac{R20}{R19 + R20} + Vr \times \frac{R19}{R19 + R20}$$



d) The hysteresis characteristic prevents any misoperation caused by noise from the motor, ripple from the detector, or the fluctuation of the input signal.

D) LATCH (DIRECTION CONTROL CIRCUIT)

a) Consists of T flip-flop (39) and transistor buffer (40 & 41)

b) The T flip-flop has its logic output Q converted when the output from the comparator is elevated from low (0) to high (1).

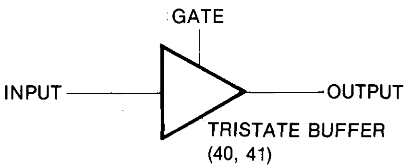
c) When the comparator output is lowered from high (1) to low (0), the T flip-flop maintains up edge operation to keep output Q constant.

d) The output Q′ of T flip-flop is generated as non-inverted logic output.

e) The output from the comparator becomes the gate signal of tristate buffer (40 & 41).

f) When gate signal is "1" (high), the input of tristate buffer is delivered to the output.

g) If gate signal is "0" (low), the output from tristate buffer becomes "0."



GATE	INPUT	OUTPUT
L (0)	L (0)	L (0)
L (0)	H (1)	L (0)
H (1)	L (0)	L (0)
H (1)	H (1)	H (1)

E) MOTOR DRIVER CIRCUIT

a) Consists of buffers (42, 43, 44 & 45), resistors (R21, R22, R23, R24, R25 & R26) and transistors (Q5, Q6, Q7 & Q8).

b) The buffer has a role of driving the transistors.

c) Transistor Q7 and Q8 are saturated by Resistors R23 and R24 when input of the buffer is "1."

d) By Resistors R25 and R26, Transistors Q5 and Q6 operate as constant current suppliers.

e) Pins 1, 6, 7, 8 & 9 of the motor driver circuit are connected to the motor circuit consisting of Transistors Q9 and Q10 the motor (M) and voltage (V) supplier.

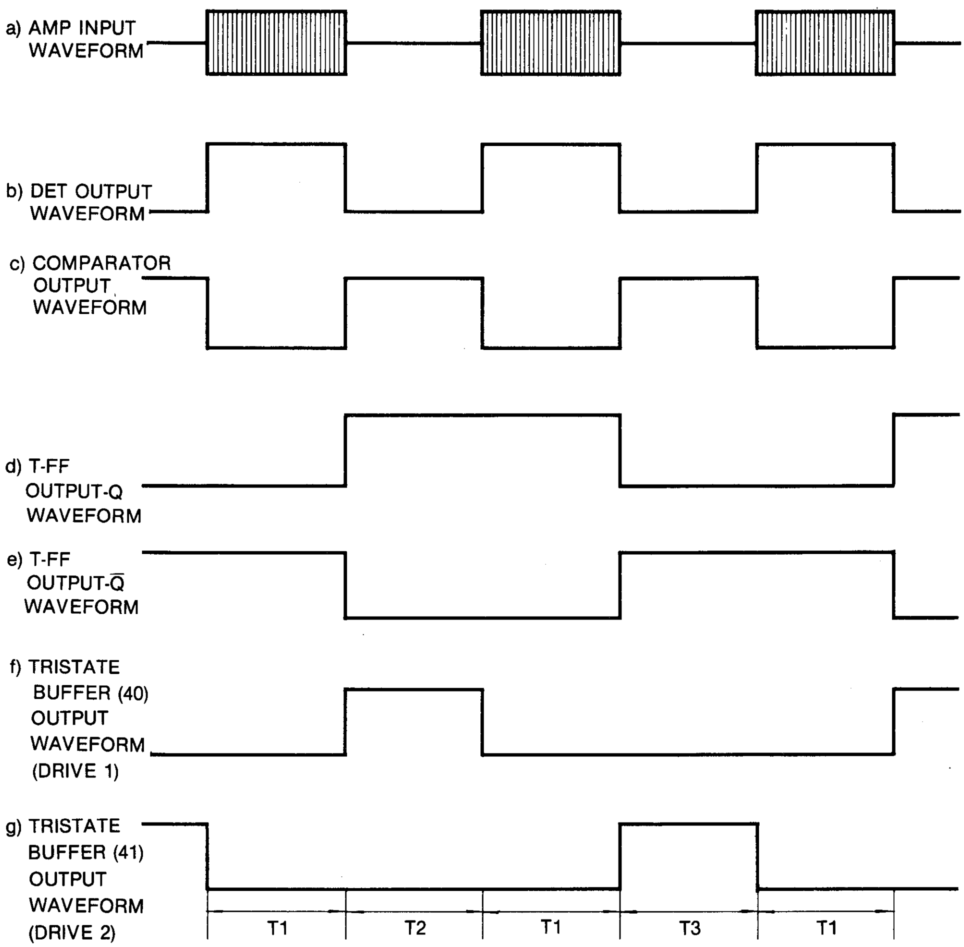
f) When the driver 1 input is "1" and Driver 2 input is "0", Transistors Q5 and Q7 are turned on while Q6 and Q8 are turned off. As a result motor driver current flows through Transistor Q9, motor (M) and Transistor (Q7). ("Forward")

g) When both inputs of Drivers 1 & 2 are in the opposite condition to f), Transistors Q5 and Q7 are turned off whereas Q6 and Q8 are on. Therefore, the motor driver current flows through Transistor Q10, motor (M) and Q8. The motor is driven "backward".

h) When the input of T flip-flop is "0", output of Tristate Buffers 40 and 41 also becomes "0". Since the transistors *from Q5 to Q8 are turned off, the motor stops functioning.*

3) DYNAMIC WAVEFORM OF EACH BLOCK.

A) DYNAMIC WAVEFORMS



B) OPERATION OF DYNAMIC WAVEFORMS

a) For waveform (f) and (g), input signals of the motor driver circuit become "0" during period T1. So the transistors from Q5 to Q8 are turned off and the motor stops its operation.

b) In period T2, Motor Driver 1 input becomes high whereas that of Motor Driver 2 is low. So Transistors Q5 and Q7 are activated while Q6 and Q8 are turned off. As a result, the motor is driven forward.

c) In period T3, Motor Driver 1 has low input while high input is provided to Motor Driver 2. So Transistors Q5 and Q7 are turned off while Q6 and Q8 are turned on. The direction of the motor is "backward."

3. APPLICATION CIRCUIT AND THEIR OPERATIONS

1) APPLICATION CIRCUIT 1

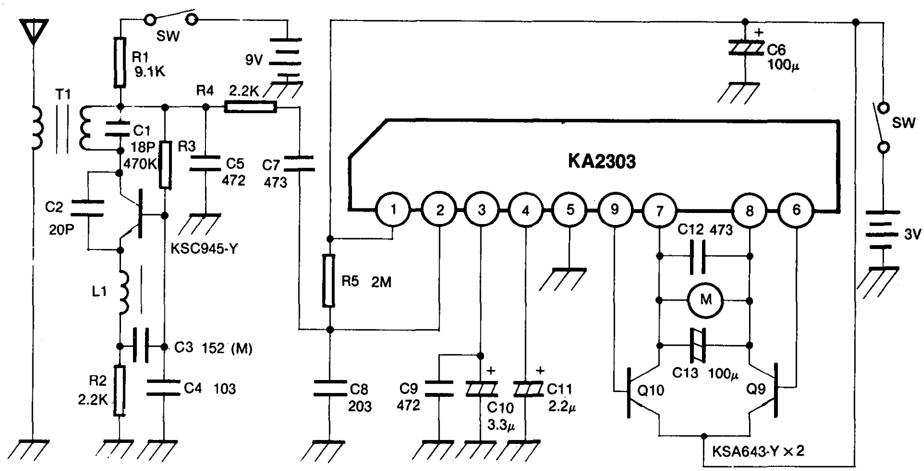


Fig. 3

2) APPLICATION CIRCUIT 2

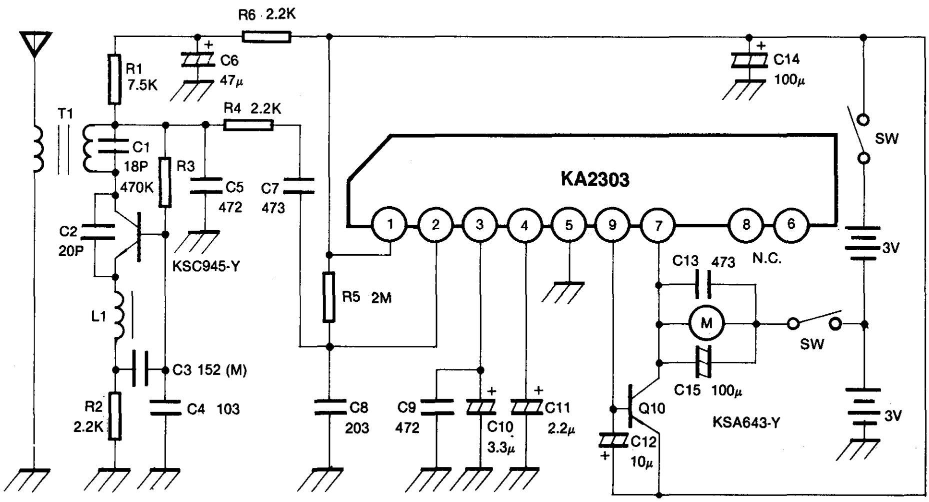


Fig. 4

3) OPERATIONAL DESCRIPTION (Please refer to above block diagrams)

A) WHEN NO SIGNAL IS TRANSMITTED ("Stop" motion of the motor).
  a) Noise signal within audio frequency range is obtained at the antenna.
  b) Quenching signal is generated by Transistor Q1, Capacitor C2 and Coil L1 of the super regeneration receiver circuit. (Quenching frequency of 100KHz to 500KHz).
  c) The Quenching signal and noise signal are mixed before entering Pin 2 through L.P.F. (R4 and C5).
  d) In the amplifier stage, an AC amplifier, only the noise signal is amplified to be delivered to the detector stage. The amplification rate should be about 43dB.
  e) The peak voltage of the low frequency noise signal fed to non-inverting terminal (+) of the operational amplifier is detected at the detector stage. Here the noise component of AC voltage is converted into DC voltage so the size of the DC voltage is determined by the amount of noise input. The amplification rate is about 24.6dB.
  f) Detected peak voltage should be "1" (High condition: the voltage detected should be above 0.7V) and it is input to the inverting terminal (−) of the operational amplifier in the comparator stage.
  g) The high signal fed to the inverting terminal (−) of the comparator is generated as low output to be delivered to the latch.
  h) Since low (0) input is provided to the T flip-flop of the latch stage, the original output from the T flip-flop remains unchanged. Both gate signals of the tristate buffer and the output of latch stage are low.
  i) As the low input is fed to the motor driver stage, transistors from Q5 to Q8 are turned off so the motor stops its function.

5

B) WHEN SIGNAL IS TRANSMITTED FROM THE TRANSMITTER (Forward/Backward)
  a) A non-modulated high frequency signal (in the KA2303: 27-49MHz) resonated by the coil (T1) of the super generation receiver circuit and by Capacitor C1 is obtained at the antenna.
  b) The non-modulated high frequency signal organized at the antenna and the quenching signal are fed to the L.P.F. of R4 and C5.
  c) The only signal passing through the L.P.F. is the quenching signal and it is impressed on Pin 2.
  d) Only noise signal can be amplified at the amplifier stage. However, only the signal provided to the stage is the quenching signal, so no noise can be generated.
  e) Without any noise signal input, the detector stage has low (0) output. (To be low, the detector voltage should be less than 0.3V).
  f) With low input, the inverting terminal of the comparator generates high output which will enter the latch stage.
  g) The T flip-flop of the latch stage has high input which will be inverted into a previous one. Since the gate signal of the triste buffer is high, the output of T flip-flop is delivered to the tristate buffer output.

Tn	Qn+1
0	Qn
1	$\overline{Qn}$

Here Tn: Input of T-FF
Qn: Previous output is maintained
$\overline{Qn}$: Inversion of previous output
Qn+1: Present output condition

  h) When the T flip-flop output is high (1), Transistors Q5 and Q7 are turned on while Q6 and Q8 are turned off. So the operational current flows through Transistor Q9, motor (M) and Transistor Q8.
  i) With low output (Q) of the T flip-flop, Transistors Q5 and Q7 are turned off while Q6 and Q8 are turned on. So the operational current flows through Transistor Q10, motor (M) and Transistor Q8.
  Consequently, the motor is driven backwards.

4) EXTERNAL COMPONENTS

A) R5: INPUT RESISTOR
Misoperation (When the motor maintains only one direction) caused by low input noise is prevented by R5. If its value is small, the sensitivity of the receiver drops, whereas excessive value blunts the prevention of a misoperation. Therefore a value of 2MOhm is recommended.

B) C8: INPUT BYPASS CAPACITOR
If the capacitor value is reduced, the sensitivity of the receiver is also reduced. However, a large value may result a misoperation. So an appropriate value of 0.02μF is recommended.

C) C9, C10: FEEDBACK CAPACITOR
They control the forward/backward converting time of the motor. When their values are small, the motor either stops or misoperates when encountered with an obstacle. Also their voltage are low (V_{CC} = less then 2.5V). On the other hand, a large value delays the forward/backward conversion time. In addition, if a weak signal is obtained due to remote transmission, a misoperation can be expected.
Therefore 0.0047μF for C9 and 2.2μF – 3.3μF for C10 are recommend.

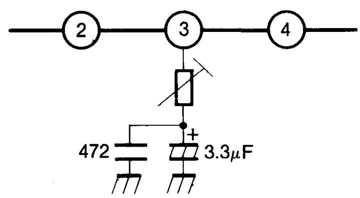
D) C11: PEAK DETECTOR CAPACITOR
A misoperation is expected if a weak signal is provided. On the other hand, a large value stabilizes DC voltage of Pin 4 but it delays the forward/backward time of the motor. Also when it encounters with an obstacle and voltage is low, the motor can misoperate. Satisfying results can be achieved with a value within the range of 2.2μF to 3.3μF.

5) PROPER CARE IN USING THE IC.

A) Since the KA2303 is operated by the noise within audio frequency range, it is sensitive to noise. If it does not match properly with the super regeneration receiver circuit, misoperation of the motor can be expected. Therefore, care is required when designing the set.

B) Input noise voltage can be easily modulated by the DC voltage difference of Pin 4. That is, an easy design of a set is provided if the DC voltage of Pin 4 is 0.7V – 1.0V when the motor stops, and less than 0.3V when motor is driven either backward or forward. Therefore, whether the input noise is present in the device determines the conversion of the motor. Also the motor can be activated by directly feeding DC voltage to Pin 4.

C) By inserting a proper DC resistor between Pin 3 terminal and feedback capacitor, the amplifier gain is controlled to obtain a desirable sensitivity of the receiver.



D) In order to apply the device in a low voltage (3V) circuit, super regeneration receiver circuit and power supply should be used separately.
If they share same power source, the motor may misoperate.
*.super regeneration receiver circuit: V_{CC} = 9V, KA2303: V_{CC} = 3V.

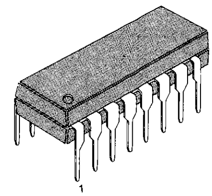
E) If your circuit design contrasts with our recommendation, characteristics deviation should be reviewed.

KA2309 APPLICATION NOTE

1. INTRODUCTION

The KA2309 is an integrated circuit designed for 7 function R/C toy car. This I.C. consists of a regulator, an amplifier, a frequency detector, a duty detector, a comparator and two stages of drivers.
The device operates on low voltage (3V) due to its structure requiring only minimum number of external parts and having 2.5V as regulator output. It is also free from any misoperation expected when power is switched ON/OFF. Built-in Turbo function is also available.
For a best performance, the device is recommended to be used with a transmitter I.C. KA2310.

16 DIP



2. BLOCK DIAGRAM & OPERATIONAL DESCRIPTION

2-1. BLOCK DIAGRAM

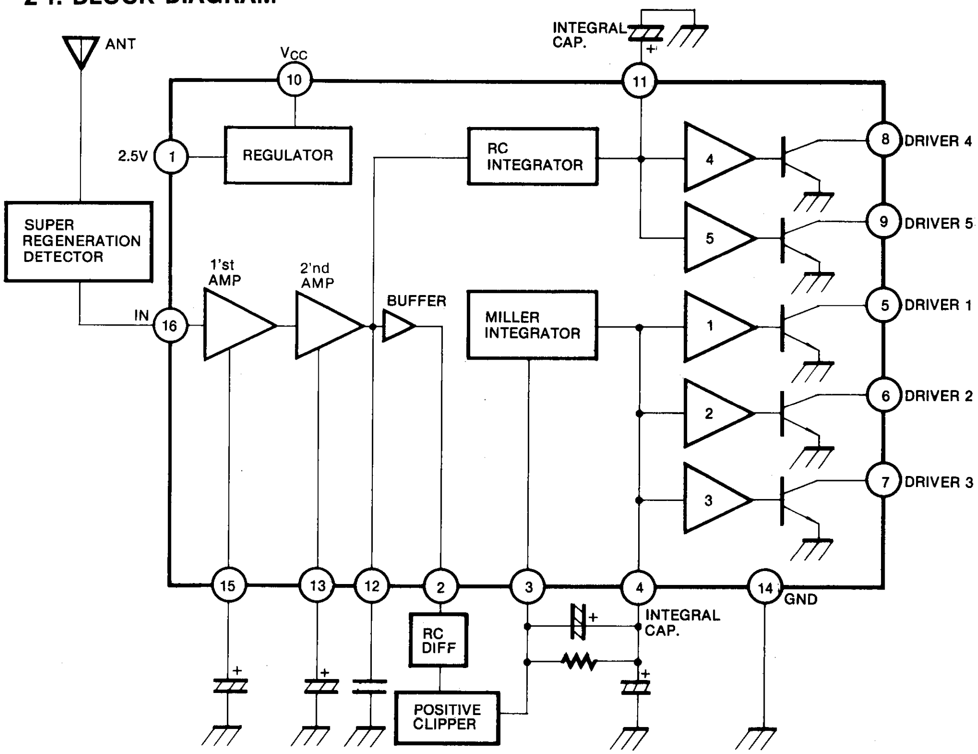
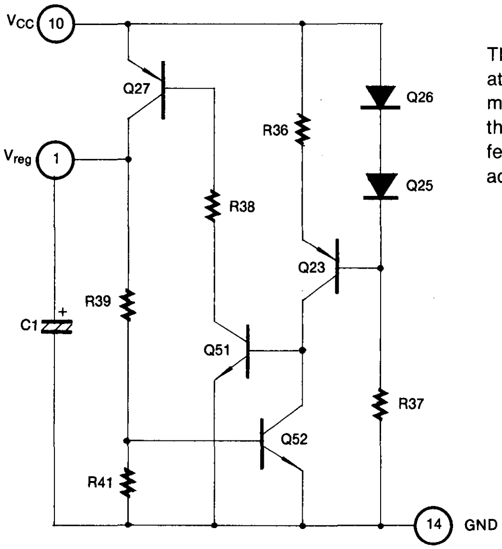


Fig. 1

2-2. OPERATIONAL DESCRIPTION

1) Regulator



The circuit is used as current biasing for the super regeneration detector and other circuits. Constant 2.5V is always maintained in the circuit against changes in power or load, therefore a stable operation is guaranteed. As a negative feedback, Q51-Q27-Q52 loop maintains continuous control action after being initiated by Q26-Q25-Q23.

Fig. 2

2) Amplifier

By amplifing the signal divided at the super regeneration detector, the signal can be separated into noise and functional signal at the detector.

Equivalent circuit of the 1st Amp

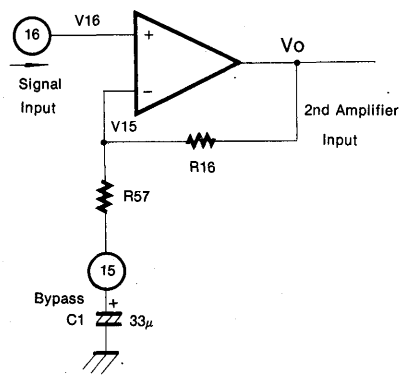


Fig. 3

Equivalent circuit of the 2nd Amp

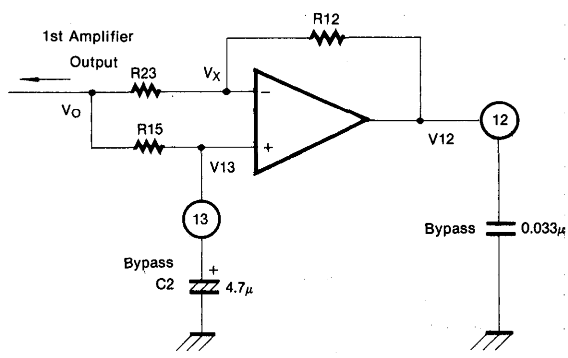


Fig. 4

$$Av1 \fallingdotseq 20 \log \left(1 + \frac{R16}{R57}\right) \fallingdotseq 29.5dB$$

$$Av2 \fallingdotseq 20 \log \left(\frac{R12}{R23}\right) \fallingdotseq 28.5dB$$

$$Av = Av1 + Av2 = 58dB$$

Frequency Characteristic

(i) The low frequency characteristic is determined by R57, R15, and external C1 and C2.

$$f_L(1)=\frac{1}{2\pi\cdot R57\cdot C1}\ (Hz)$$

$$f_L(2)=\frac{1}{2\pi\cdot R15\cdot C2}\ (Hz)$$

For example, when lowest frequency of the signal to be amplified is 50Hz, C1 becomes larger than 17.7μF $\{1/(2\pi\times50\times180)\}$.

(ii) The high frequency is determined by the frequency characteristic of the amplifier. The 3dB cutoff frequency is,

$$f_H(1)=\frac{G.B}{2\pi\cdot Av1}\ (Hz)$$

$$f_H(2)=\frac{G.B}{2\pi\cdot Av2}\ (Hz)$$

*G.B = Avo-Wc Avo: open loop gain
Wc: −3dB corner frequency

3) Miller Integrator (Frequency Detector)

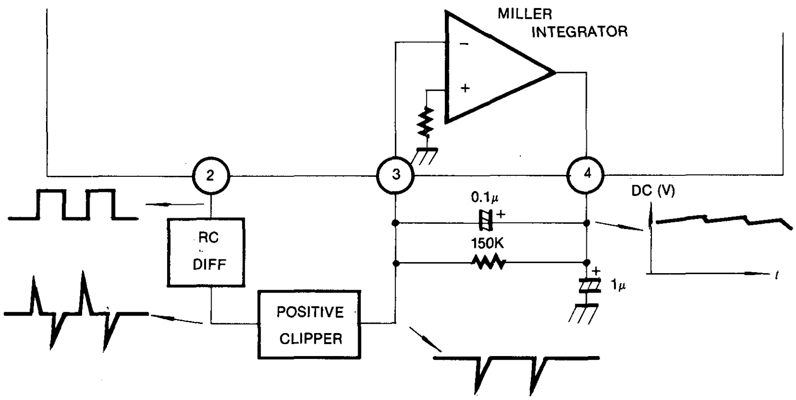


Fig. 5

The Miller Integrator converts functional signals into the DC level. After the Pin 2 square wave is differentiated to pass through the positive clipper, only negative spikes remain. Therefore no matter what the duty is, negative spikes are generated in certain intervals.

If functional signals (square wave) are not available, the DC level of Pin 3 becomes more than zero and that of Pin 4 is kept nearly grounded. When the negative spikes at a certain interval are impressed on Pin 3 a negative spike proportional to frequency is generated at Pin 4 to drive the subsequential drive stage.

Since the integrator has a high gain due to its structure, the output voltage can easily drift from the '0' level. In order to prevent such a drift, a large resistor like R9 is connected between the output and inverting input. The integrator at low frequency is not affected by the DC gain that is cut down by R9. If the input frequency is too low, that capacitance impedance becomes higher than R9, and the integrator becomes disabled even though the capacitor is not affected. Therefore, C12 should be Xc12«R9. Generally Xc12 is set as R9/10.

$$\frac{1}{2\pi f_L C12} = \frac{R9}{10}$$

$$f_L = \frac{10}{2\pi C12R9}$$

4) RC Integrator (Duty Detector)

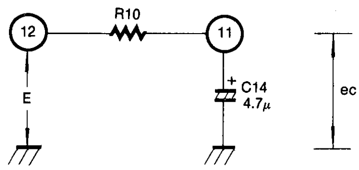


Fig. 6

Certain levels of DC in respect to duty is generated by the RC integrator. The output waveform of the RC serial circuit relies on the relationship between the time constant (CR) and pulse width (PW). This circuit, a CR //·(10 x PW), obtains output from both ends of the capacitor.

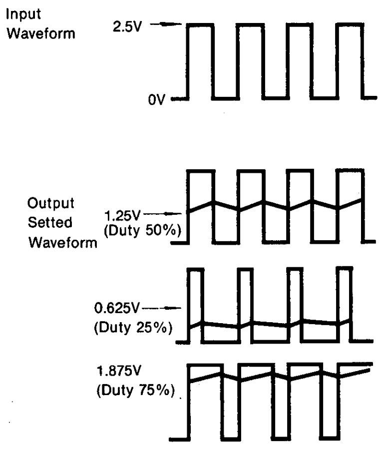


Fig. 7

5) Driver Stage

(1) Driver 1

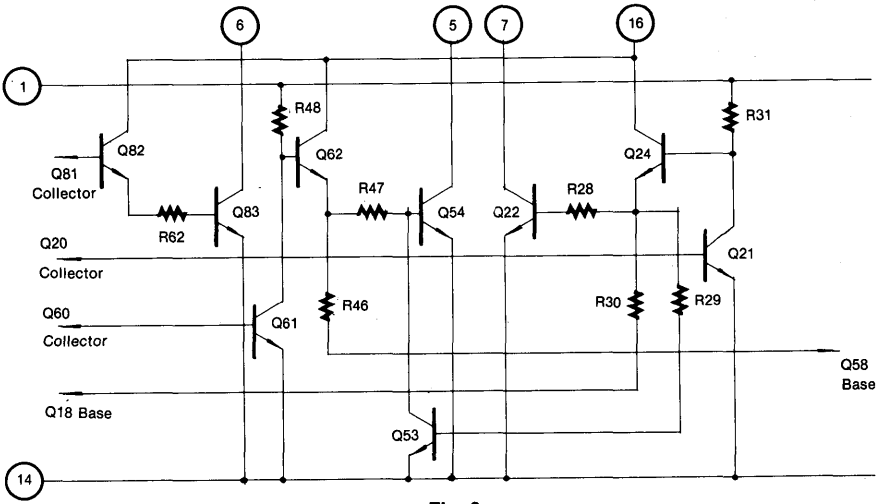


Fig. 8

i) When the Pin 4 DC level is 0.5-1.3V: Q61 is turned off Q62, Q54 and Q58 are turned on, So the Pin 5 DC level becomes low.

ii) When the DC level is 1.3-1.85V: Q21 is turned off, Q24, Q22, Q53, Q18 and Q58 are turned on. Q53 is turned on, Q54 becomes turned off and the Pin 7 voltage becomes low.

iii) When the DC level is above 1.85V: Q81 is turned off. Q82 and Q83 are turned on. Then Pin 6 and Pin 7 can not be operated at the same time, but Pin 7 operation is not disturbed owing to external application circuit. Q58 holds the operation of Driver 2 while Driver 1 is inhibited. In order words, Driver 2 is active only when the operation of Driver 1 is determined.

(2) Driver 2

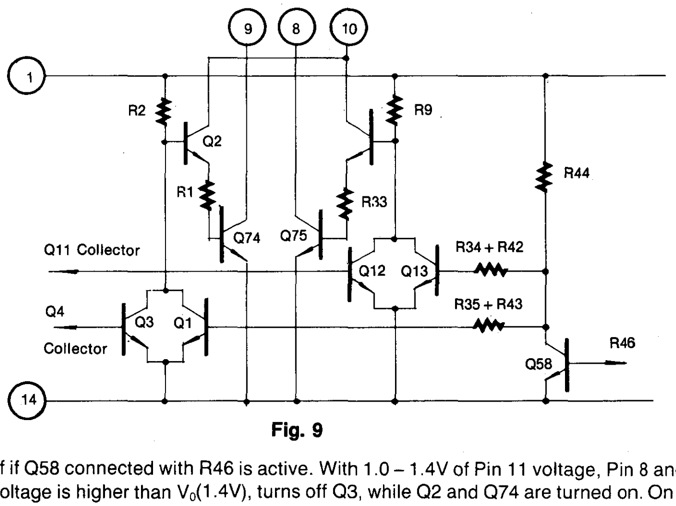


Fig. 9

Q1 and Q13 are turned off if Q58 connected with R46 is active. With 1.0 – 1.4V of Pin 11 voltage, Pin 8 and Pin 9 become high. However, If Pin 11 voltage is higher than V_0(1.4V), turns off Q3, while Q2 and Q74 are turned on. On the other hand, Pin 11 voltage lower than V_E (1.0V) turns off Q12 and turns on Q14 and Q75. As a result Pin 8 voltage becomes low. When current sinking is 30mA, Output Terminals 5, 6, 7, 8 and 9 of both drivers are designed to be less than 1.2V.

3. APPLICATION CIRCUIT & OPERATIONAL DESCRIPTION

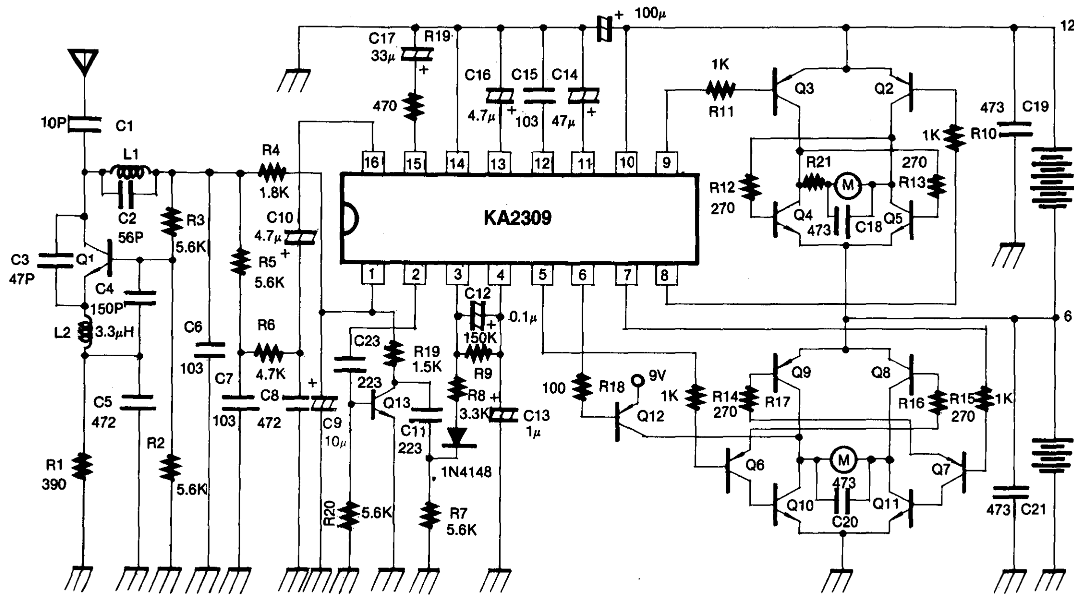


Fig. 10

Q1: C838-0
Q2, Q3, Q6, Q7: B564-Y
Q4, Q5: D471-Y
Q8, Q9, Q12: B772-Y
Q10, Q11: D882-Y
Q13: C945-Y

OPERATIONAL DESCRIPTION

The square wave inputted and detected by the super regeneration receiver is impressed to the input stage of the KA2309 Pin 16. The super regeneration receiver power is supplied by the regulator output voltage (2.5V) and the oscillator consists of TR Q1, L2, C3, C4, C5 and R1.

The Pin 16 input signal is sufficiently amplified by the AMP ($A_V = 52dB$) to be divided into a noise component and functional signal. The functional signal is fed to the Miller integrator through a buffer, RC differential and positive clipper circuit. Also, it is fed to the RC integrator stage.

The functional signal is outputted through Pin 2 of the buffer circuit and then differentiated by the RC differentiator consisting of C23 and R20. A positive differential waveform of over 0.6V is inverted against the collector of Q13 and then generated through Q13.

The waveform appearing at the Q13 collector is fed to the Miller Integrator via the positive clipper circuit of D1. DC level proportional to the frequency of function signal appears at the Miller integrator output stage at Pin 4. Here, the R9 is connected to minimize drifting of output voltage generated by the high gain of the operational amplifier. Therefore operation of the integrator is disturbed at low frequency.

The Pin 4 DC level proportional to frequency is determined by R8, R9 and C12. The relationship between function frequency and Pin 4 DC level is as below:

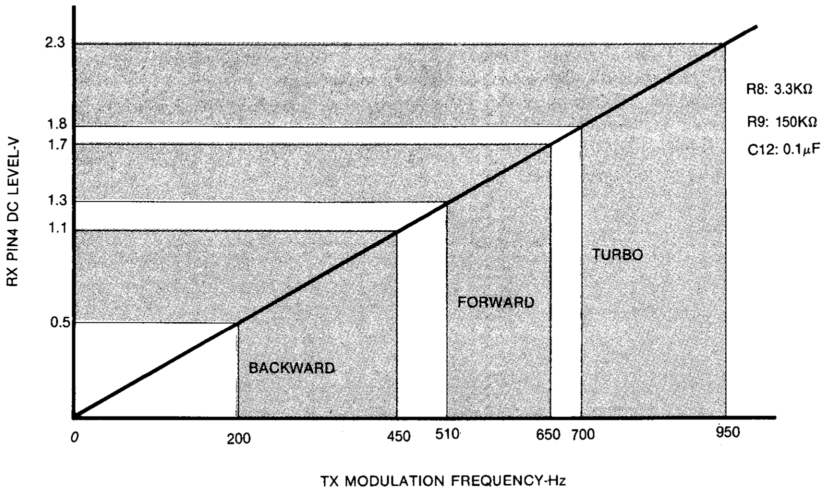


Fig. 11

Operation of each driver stage is determined by the DC level of Pin 4.

— When the level is less than 0.5V (zero signal: Tx off): The driver stages stop functioning. Accordingly, transistors of the external driver stage are turned off. Therefore the Reel Motor STOPS.

— When the level is 0.5V-1.1V: Driver 1 is turned on (Pin 5 is low) while external driver transistors Q6, Q8, Q10 are turned on. Therefore the Reel Motor turns Backward.

— When the level is 1.3-1.7V: Driver 3 is turned on (Pin 7 is low) and external driver transistors Q7, Q9, Q11 are turned on. Therefore the Reel Motor turns forward.

— When the level is above 1.8V. Driver 2 is turned on (Pin 6 is low) and active Driver 3 turns on driver transistors Q7, Q9, Q12, Q11 on. Therefore the Reel Motor repeats Forward of Turbo function.

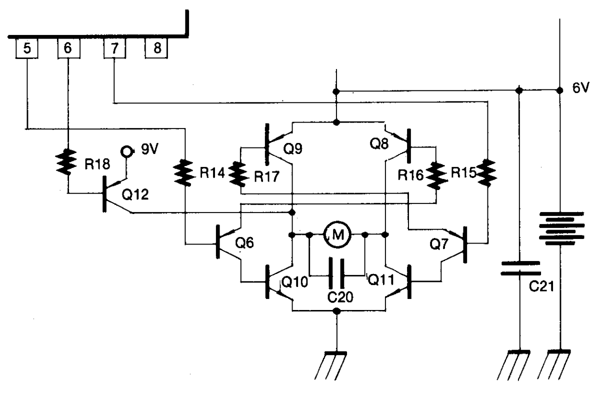


Fig. 12

5

The amplified functional signal fed to the RC integrator is converted into a DC level proportional to duty.

— Duty = 50%: DC level of Pin 11 becomes approximately 1.25V. So Drivers 4 & 5 are disabled. Accordingly, the external steering motor driver TR is turned off. Therefore the steering motor stops.
— Duty = 25%: Driver 4 is active if DC level of Pin 11 is approximately 0.625V (Pin 8 is low). Then external driver TRs Q2 and Q4 are turned on. Therefore the steering motor turns left.
— Duty = 75%: Driver 5 is active when DC level of Pin 11 is approximately 1.875V (Pin 9 is low). TRQ3 and Q5 are turned on. Therefore the steering motor turns right.

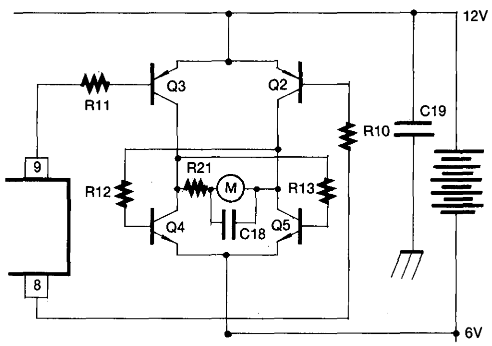


Fig. 13

4. REMARK

1) Adjustment of Receiver Sensitivity

Pin 12 square wave of the amplifier output terminal should adjust L1 and C2 resonance circuit of super regeneration receiver to an optimum point where waveform is free from noise.

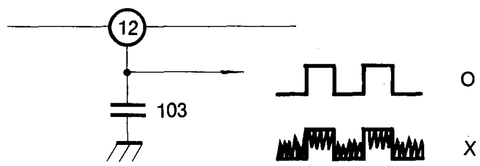


Fig. 14

2) Operational Mode (Forward, Backward, Turbo) Check

Pin 4 DC level and pin voltage of each driver stage need to be checked.

Function	Pin 4 VTG (DC)	Driver Pin (H→L)
Stop	0.5V↓	Pin 5, 6, 7: High
Backward	0.5 ~ 1.1V	Pin 5
Forward	1.3 ~ 1.7V	Pin 7
Turbo	1.8V↑	Pin 6

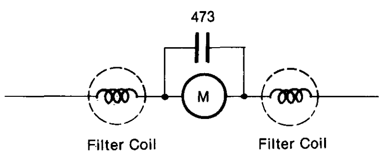
3) Left-Turn and Right Turn

Pin 12 DC level and pin voltage of each driver stage need to be checked.

Function	Pin 12 VTG (DC)	Driver Pin (H→L)
Stop	1.0 ~ 1.4V	Pin 8, 9: High
Left Turn	1.0V↓ (Typ: 0.625V)	Pin 8
Right Turn	1.4V↑ (Typ: 1.875V)	Pin 9

4) Motor Noise Causing a Misoperation can be Eliminated as Below

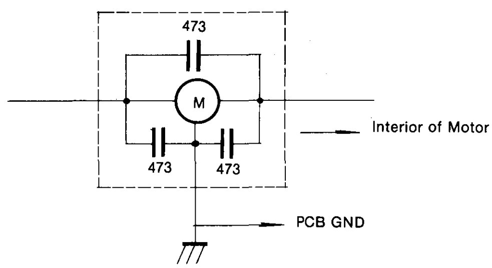
Steering Motor



Recommended Applications of Steering Motor.

Fig. 15

Reel Motor



Recommended Application of Reel Motor.

Fig. 16

5) When the device is applied with transmitter I.C. KA2310: Tx modulation frequency should be adjusted to center frequency of each operation mode (forward, backward, turbo) after checking the range of each functional frequency.

Function	KA2309 (RX)		KA2310 (TX) Modulation Frequency
	Frequency (Hz)	Pin 4 VTG (V)	
Backward	200 ~ 450	0.5 ~ 1.1	320Hz
Forward	510 ~ 650	1.3 ~ 1.7	580Hz
Turbo	700 ~ 950	1.8 ~ 2.3	820Hz

* Frequency range against KA2309 Pin 4 voltage changes in respect to surrounding time constant (R8, R9, C12). Therefore the modulation frequency of T_X should be adjusted properly.

6) Each base resistor value of the steering motor driver stage and the reel motor driver stage should be set according to the type of the motor and operation voltage. If the values are too small, driver TR may be distracted by being overloaded. If it is large, performance of the driver is inhibited.

7) If the external driver TRs are not used properly according to voltage, current and the capacity of the motor, especially when they exceed Absolute Maximum Rating the driver TR can be destroyed.

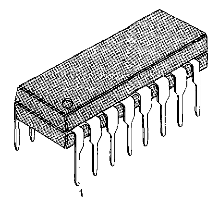
Recommended Driver TR

TR \ I_C (max)	1A	2A	3A
PNP	B564A	A928A	B772
NPN	D471A	C2328A	D882

1. INTRODUCTION

The KA2311 is an integrated circuit designed for full function radio-controlled toy cars. This I.C. consists of a regulator, an amplifier, a frequency detector, a duty detector, a comparator and two stages of drivers.
The device operates on low voltage (3V) due to its structure requiring only minimum number of external parts and having 2.5V as regulator output. It is also free from any misoperation expected when power is switched ON/OFF. A built-in Turbo function is also available.
For a best performance, the device should be used with a transmitter I.C., KA2312.

16 DIP



2. BLOCK DIAGRAM & OPERATIONAL DESCRIPTION

2-1 BLOCK DIAGRAM

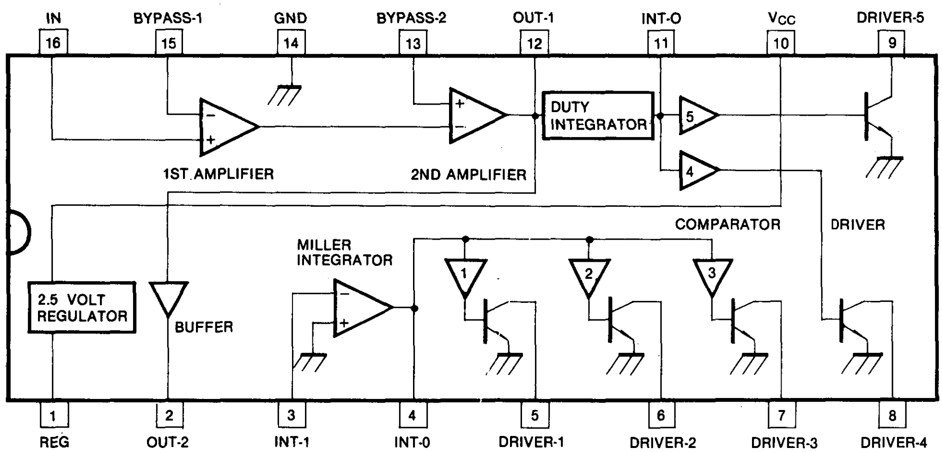
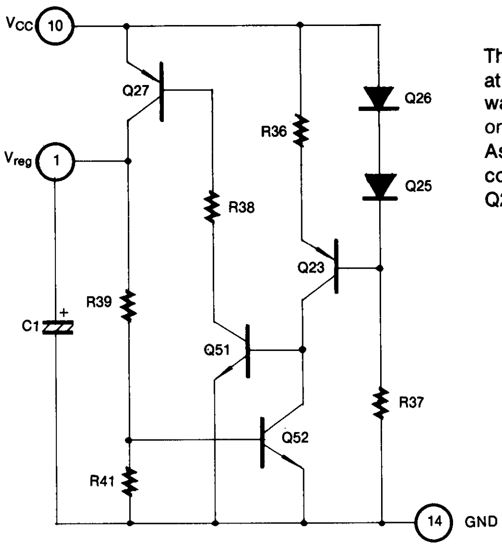


Fig. 1

2-2 OPERATIONAL DESCRIPTION

1) Regulator



The circuit is used as current biasing for super regeneration detector and other circuits. Constant 2.5V is always maintained in the circuit against changes in power or load, therefore stable operation is guaranteed.
As a negative feedback, Q51-Q27-Q52 loop maintains continuous control action after being initiated by Q26-Q25-Q23.

Fig. 2

2) Amplifier

By amplifing the signal divided at the super regeneration detector, the signal can be separated into noise and functional signal at the detector.

Equivalent circuit of the 1st Amp

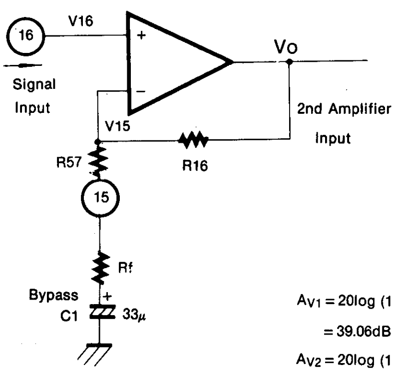


Fig. 3

$$A_{V1} = 20\log\left(1 + \frac{R_{16}}{R_{57} + R_f}\right)$$
$$= 39.06\text{dB } (R_f = 0)$$
$$A_{V2} = 20\log\left(1 + \frac{R_{12}}{R_{23}}\right)$$
$$= 27.6\text{dB}$$

Equivalent circuit of the 2nd Amp

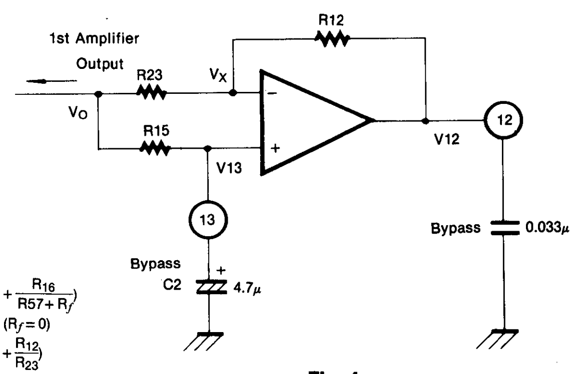


Fig. 4

$$A_V = 20\log|A_{vf1}| + 20\log|A_{vf2}|$$
$$= 39.06 + 27.6 = 66.66\text{dB}$$

Frequency Characteristic

(i) Low frequency characteristic is determined by R57, R15, and external C1 and C2.

$$f_L(1) = \frac{1}{2\pi \cdot R57 \cdot C1} \text{ (Hz)}$$

$$f_L(2) = \frac{1}{2\pi \cdot R15 \cdot C2} \text{ (Hz)}$$

For example, when lowest frequency of the signal to be amplified is 50Hz, C1 becomes larger than 17.7μF $\{1/(2\pi \times 50 \times 180)\}$.

(ii) High frequency is determined by the frequency characteristic of the amplifier. The 3dB cutoff frequency is,

$$f_H(1) = \frac{G.B}{2\pi \cdot Av1} \text{ (Hz)}$$

$$f_H(2) = \frac{G.B}{2\pi \cdot Av2} \text{ (Hz)}$$

*G.B = Avo-Wc Avo: open loop gain
Wc: −3dB corner frequency

5

3) Miller Integrator (Frequency Detector)

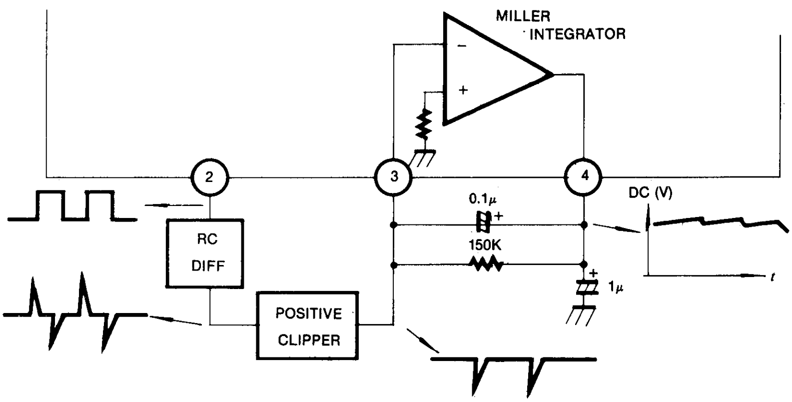


Fig. 5

The Miller Integrator converts functional signal into the DC level. After the Pin 2 square wave is differentiated to pass through the positive clipper, only negative spikes remain. Therefore no matter what the duty is, negative spikes are generated at certain intervals.

If a functional signal (square wave) is not available, the DC level of Pin 3 becomes more than zero and that of Pin 4 is kept nearly grounded. When the negative spikes at a certain interval are impressed on Pin 3, negative spikes proportional to frequency are generated at Pin 4 to drive subsequential drive stage.

Since the integrator has a high gain due to its structure, the output voltage can easily drift from the '0' level. In order to prevent such a drift, a large resistor like R9 is connected between the output and inverting input. The integrator at a low frequency is not affected by the DC gain that is cut down by R9. If the input frequency is too low that capacitance impedance becomes higher than R9, the integrator becomes disabled even though the capacitor is not affected. Therefore, C12 should be $X_C12 \ll R9$. Generally X_C12 is set at R9/10.

$$\frac{1}{2\pi f_L C12} = \frac{R9}{10}$$

$$f_L = \frac{10}{2\pi C12R9}$$

4) RC Integrator (Duty Detector)

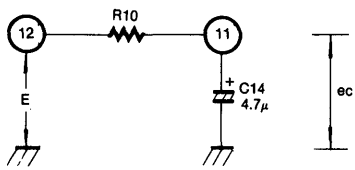


Fig. 6

A certain level of the DC in respect to duty is generated by RC integrator. The output waveform of the RC serial circuit relies on the relationship between the time constant (CR) and pulse width (PW). This circuit, a CR // (10 × PW), obtains output from both ends of the capacitor.

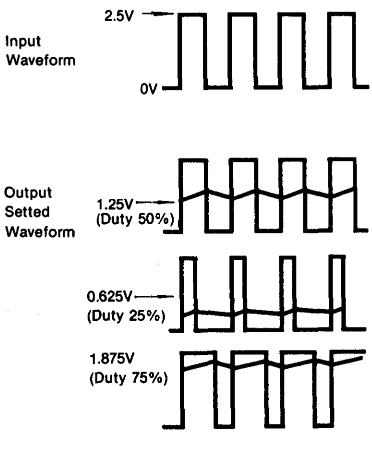


Fig. 7

5) Driver Stage

(1) Driver 1

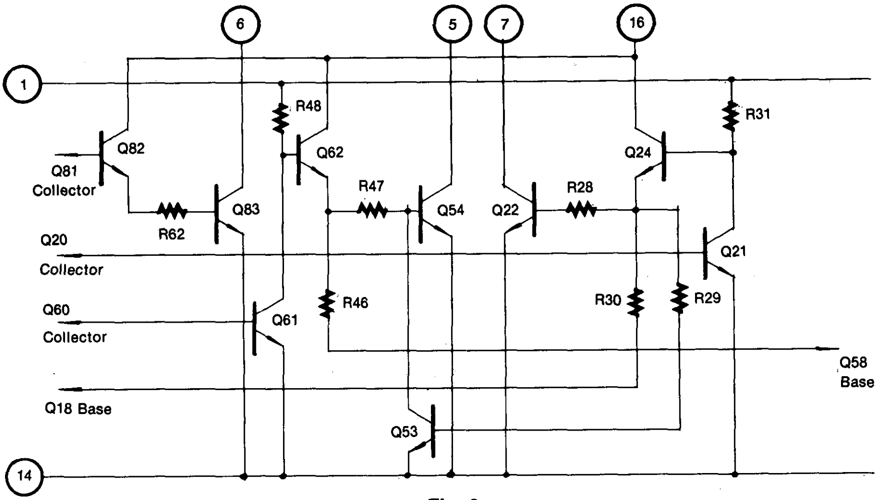


Fig. 8

i) When the Pin 4 DC level is 0.5-1.3V: Q61 is turned off Q62, Q54 and Q58 are turned on. So the Pin 5 DC level becomes low.

ii) When the DC level is 1.3-1.85V: Q21 is turned off. Q24, Q22, Q53, Q18 and Q58 are turned on. Q53 is turned on, Q54 becomes turned off and Pin 7 voltage becomes low.

iii) When the DC level is above 1.85V: Q81 is turned off. Q82 and Q83 are turned on. Then Pin 6 and Pin 7 can not be operated at the same time, but Pin 7 operation is not disturbed owing to an external application circuit. Q58 holds the operation of Driver 2 while Driver 1 is inhibited. In order words, Driver 2 is active only when the operation of Driver 1 is determined.

(2) Driver 2

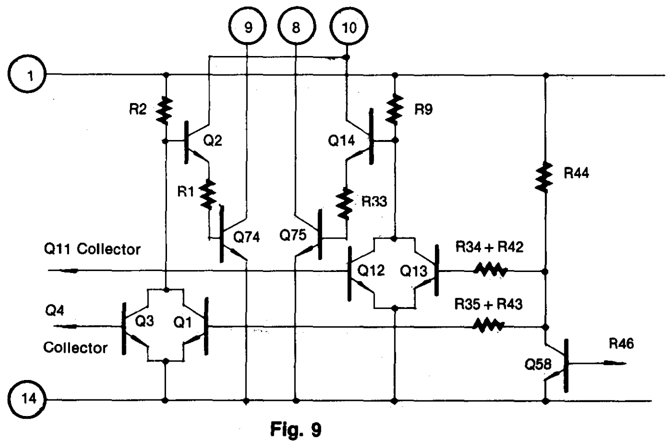


Fig. 9

Q1 and Q13 are turned off if Q58 connected with R46 is active. With 1.0 – 1.4V of Pin 11 voltage, Pin 8 and Pin 9 become high. However, Pin 11 voltage higher than V_d (1.4V) turns off Q3 while Q2 and Q74 are turned on. On the other hand, Pin 11 voltage lower than V_E (1.0V) turns off Q12 and turns on Q14 and Q75. As a result Pin 8 voltage becomes low. When current sinking is 30mA, Output Terminals 5, 6, 7, 8 and 9 of both drivers are designed to be less than 1.2V.

3. APPLICATION CIRCUIT & OPERATIONAL DESCRIPTION

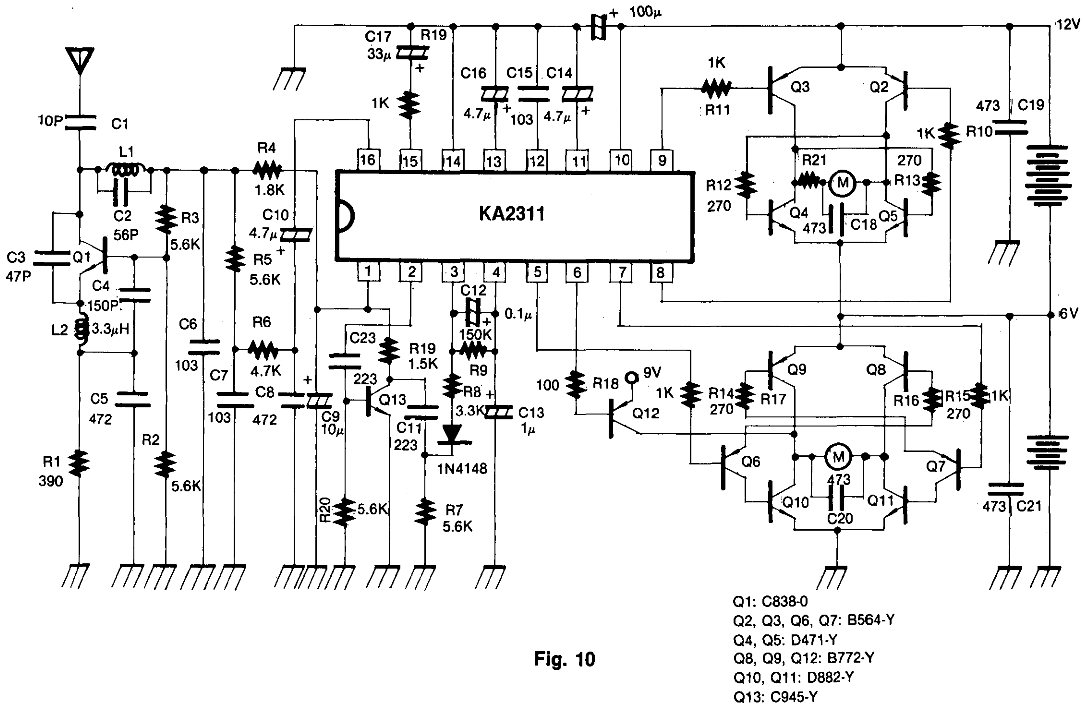


Fig. 10

OPERATIONAL DESCRIPTION

The square wave inputted and detected by the super regeneration receiver is impressed to the input stage of the KA2311 Pin 16. The super regeneration receiver power is supplied by the regulator output voltage (2.5V) and the oscillator consists of TR Q1, L2, C3, C4, C5 and R1.

The Pin 16 input signal is sufficiently amplified by the AMP ($A_V = 56dB$) to be divided into noise component and functional signal, the functional signal is fed to the Miller integrator through the buffer, RC differential and positive clipper circuit. Also, it is fed to the RC integrator stage.

The functional signal is outputted through Pin 2 of the buffer circuit and then differentiated by the RC differentiator consisting of C23 and R20. A Positive differential waveform of over 0.6V is inverted against the collector of Q13 and then generated through Q13.

The Waveform appearing at Q13 collector is fed to the Miller integrator via the positive clipper circuit of D1. A DC level proportional to the frequency of the function signal appears at the Miller integrator output stage at Pin 4. Here, R9 is connected to minimize drifting of the output voltage generated by the high gain of the operational amplifier. Therefore, operation of the integrator is disturbed at low frequency.

A Pin 4 DC level proportional to frequency is determined by R8, R9 and C12. The relationship between the function frequency and Pin 4 DC level is as below:

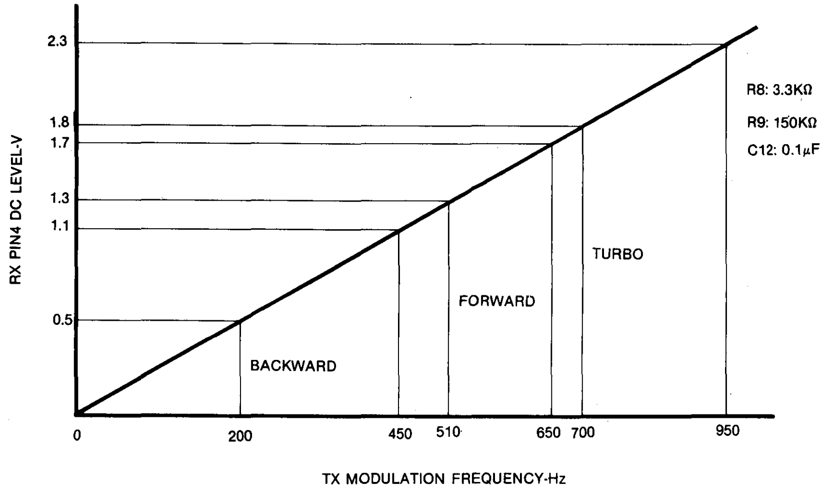


Fig. 11

Operation of each driver stage is determined by the DC level of Pin 4.

— When the level is less than 0.5V (zero signal: T_X off): The driver stages stop functioning. Accordingly, the transistors of the external driver stage are turned off. Therefore the Reel Motor stops.

— When the level is 0.5V-1.1V: Driver 1 is turned on (Pin 5 is low) while external driver transistors Q6, Q8, Q10 are turned on. Therefore the Reel Motor turns Backward.

— When the level is 1.3-1.7V: Driver 3 is turned on (Pin 7 is low) and external driver transistors Q7, Q9, Q11 are turned on. Therefore the Reel Motor turns Forward.

— When the level is above 1.8V. Driver 2 is turned on (Pin 6 is low) and active Driver 3 turns on driver transistors Q7, Q9, Q12, Q11 on. Therefore the Reel Motor repeats forward of Turbo function.

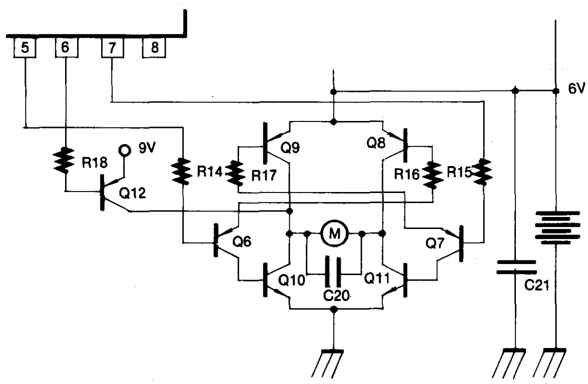


Fig. 12

The amplified functional signal fed to RC integrator is converted into DC level proportional to duty.

— Duty = 50%: DC level of Pin 11 becomes approximately 1.25V. So Drivers 4 & 5 are disabled. Accordingly, the external steering motor driver TR is turned off. Therefore the steering motor stops.
— Duty = 25%: Driver 4 is active if DC level of Pin 11 is approximately 0.625V (Pin 8 is low). Then external driver TRs Q2 and Q4 are turned on. Therefore the steering motor turns left.
— Duty = 75%: Driver 5 is active when the DC level of Pin 11 is approximately 1.875V (Pin 9 is low). TRQ3 and Q5 are turned on. Therefore the steering motor turns right.

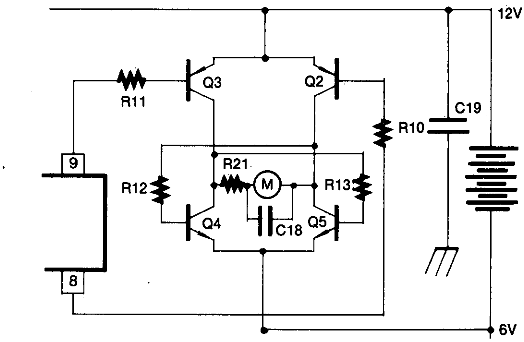


Fig. 13

4. REMARK

1) Adjustment of Receiver Sensitivity

Pin 12 square wave of the amplifier output terminal should adjust the L1 and C2 resonance circuit of the super regeneration receiver to an optimum point where the waveform is free from noise.

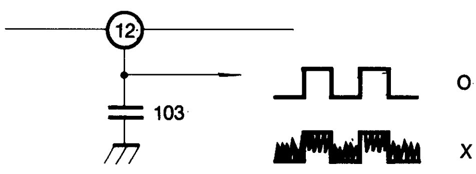


Fig. 14

2) Operational Mode (Forward, Backward, Turbo) Check

Pin 4 DC level and pin voltage of each driver stage need to be checked.

Function	Pin 4 VTG (DC)	Driver Pin (H→L)
Stop	0.5V↓	Pin 5, 6, 7: High
Backward	0.5 ~ 1.1V	Pin 5
Forward	1.3 ~ 1.7V	Pin 7
Turbo	1.8V↑	Pin 6

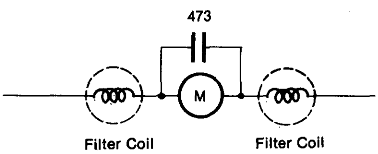
3) Left·Turn and Right Turn

Pin 12 DC level and pin voltage of each driver stage need to be checked.

Function	Pin 12 VTG (DC)	Driver Pin (H→L)
Stop	1.0 ~ 1.4V	Pin 8, 9: High
Left Turn	1.0V↓ (Typ: 0.625V)	Pin 8
Right Turn	1.4V↑ (Typ: 1.875V)	Pin 9

4) Motor Noise Causing a Misoperation can be Eliminated as Below

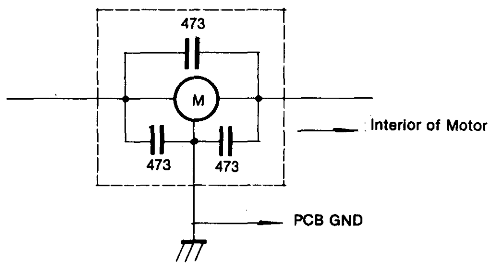
Steering Motor



Recommended Applications of Steering Motor.

Fig. 15

Reel Motor



Recommended Application of Reel Motor

Fig. 16

5) When the device is applied with transmitter I.C. KA2312, the T_X modulation frequency should be adjusted to center on a frequency of each operation mode (forward, backward, turbo) after checking the range of each functional frequency.

Function	KA2311 (RX)		KA2312 (TX) Modulation Frequency
	Frequency (Hz)	Pin 4 VTG (V)	
Backward	200 ~ 450	0.5 ~ 1.1	320Hz
Forward	510 ~ 650	1.3 ~ 1.7	580Hz
Turbo	700 ~ 950	1.8 ~ 2.3	820Hz

* The frequency range against KA2311 Pin 4 voltage changes in respect to surrounding time constant (R8, R9, C12). Therefore the modulation frequency of Tx should be adjusted properly.

6) Each base resistor value of the steering motor driver stage and the reel motor driver stage should be set according to the type of the motor and operation voltage. If the values are too small, the driver TR may be distracted by being overloaded. If it is large, performance of the driver is inhibited.

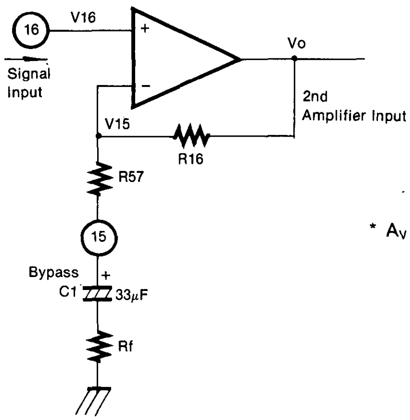
If the external driver TRs are not used properly according to voltage, current and the capacity of the motor, especially when they exceed Absolute Maximum Rating, the driver TR can be destroyed.

7) Recommended Driver TR

TR \ I_C (max)	1A	2A	3A
PNP	B564A	A928A	B772
NPN	D471A	C2328A	D882

8) AMP GAIN

Equivalent circuit of the 1st Amp

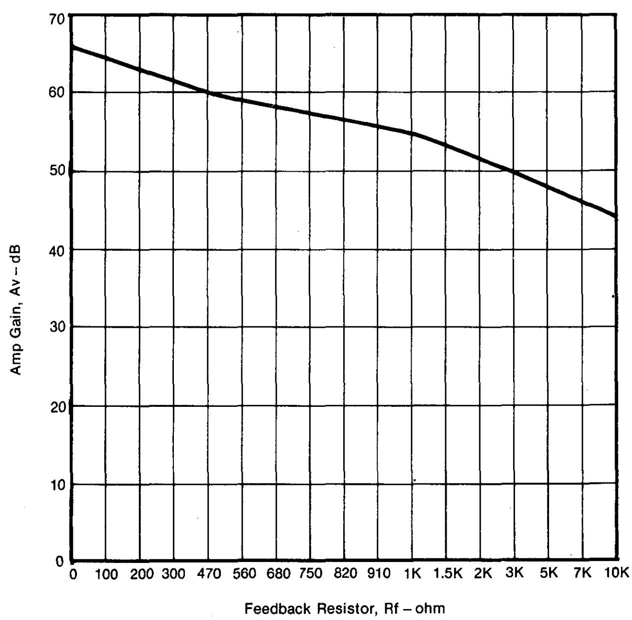


The gain of amp stage can be controlled with the insertion of an external resistor in tandem.
Because the amp stage of the KA2311 is high and the value of reference voltage is low, it is necessary that the gain should be adjusted by the insertion of a feedback resistor in order to get stable operation. (Without using an R_f resistor, malfunctions would appear. Accordingly R_f must be used and the value of 1Kohm is recommended.)

$$* \ A_V = 20\log\left(1 + \frac{R_{16}}{R_{57} + R_f}\right)$$

The graph of Amp Gain according to the value of feedback resistors is as follows;

$(A_V - R_f)$

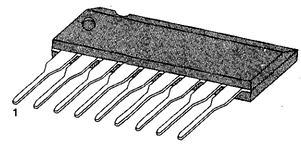


KA2312 APPLICATION NOTE

1. INTRODUCTION

The KA2312 is an integrated circuit designed for the transmitter of full function radio-controlled toy cars. It consists of a pulse generator, pulse width controller, modulator, TX signal osc, and high frequency amp.
The KA2312 TX IC is used as one kit with the KA2311 RX IC. The main application is a TX set of full function radio-controlled toy cars or some other kinds of TX for radio-controlled toy cars.

9 SIP



2. BLOCK DIAGRAM & OPERATIONAL DESCRIPTION

2-1 BLOCK DIAGRAM

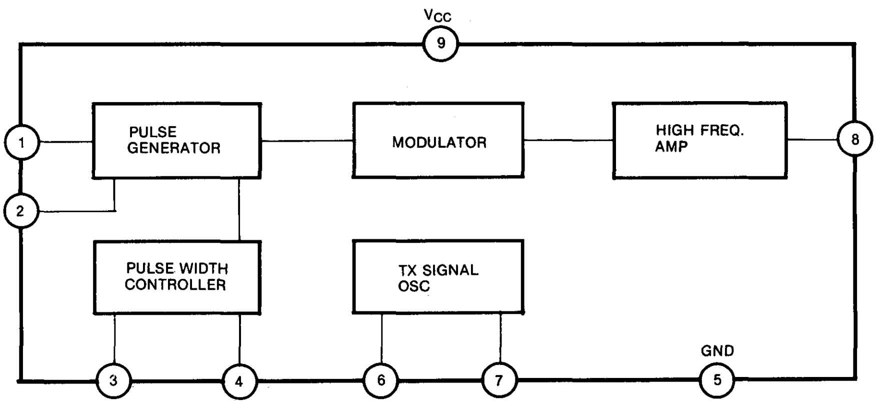


Fig. 1

2-2. OPERATIONAL DESCRIPTION

1) PULSE GENERATOR

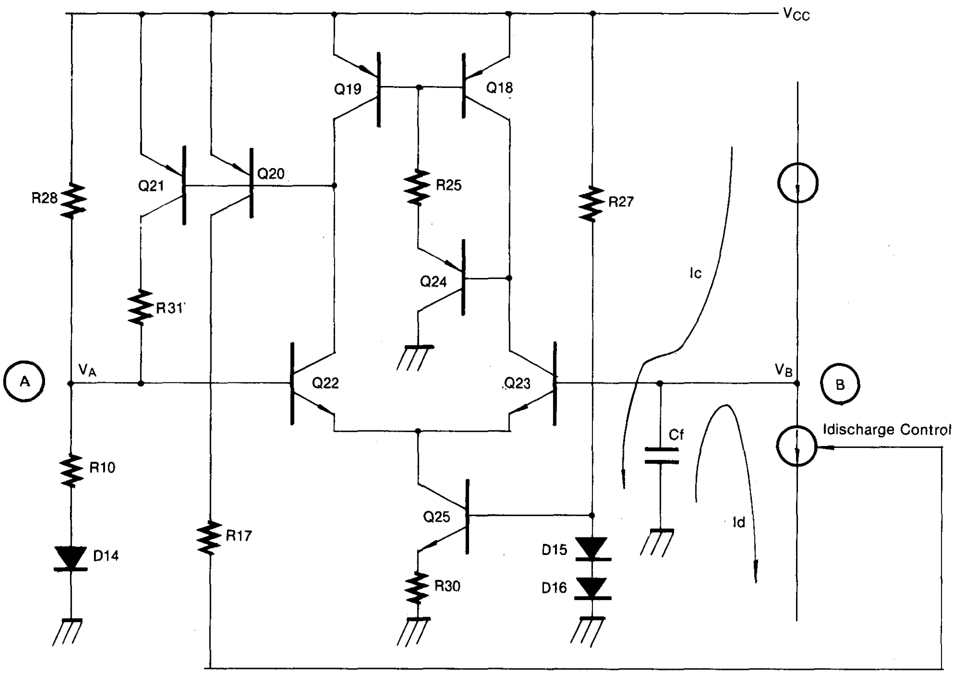
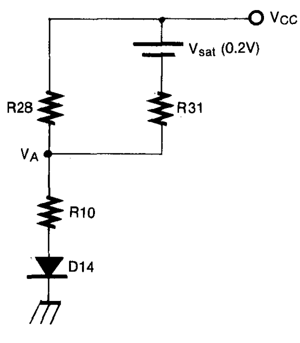


Fig. 2

The capacitor C_f charges or discharges according to the state Nodes A and B.

1. Charge

When V_A is larger than V_{B1} Q22 turns on and off, and at this moment Q21 is saturated ($V_{sat}=0.2V$).



To calculate the voltage value of node A, V_A is as follows:

$$V_A = V_{d14} + \frac{R10}{R10 + R28/R31} \times (V_{CC} - 0.7)$$
$$= 0.7 + 5.01 = 5.71V$$

Where $V_{sat}=0.2V$ is neglected.
At this time, Q20 makes the discharge control terminal turn off and the charge.

2. Discharge
When V_A is less than V_{B1} Q23 turns on and Q20, Q21, Q22, off according as the charge voltage of capacitor is larger than 5.71V. After that Q20 turns off and discharge control terminal on, as the last currents charged on the capacitor discharge.

3. Recharge
When Q21 turns OFF, the voltage of Node A is as follows:

$$V_A = 0.7 + \frac{R10}{R10 + R28}(V_{CC} - 0.7) = 0.7 + 2.79 = 3.49V$$

After capacitor discharges, when the voltage of Node B is less than 3.49V, then Q22 turns on and Q23 off. There-after, the capacitor is in the charge-state again.

2) DUTY CONTROLLER

Duty is controlled by the current ratio of Q2, Q4, Q10, Q11 current mirror in which the collector current of Q3 is reference.

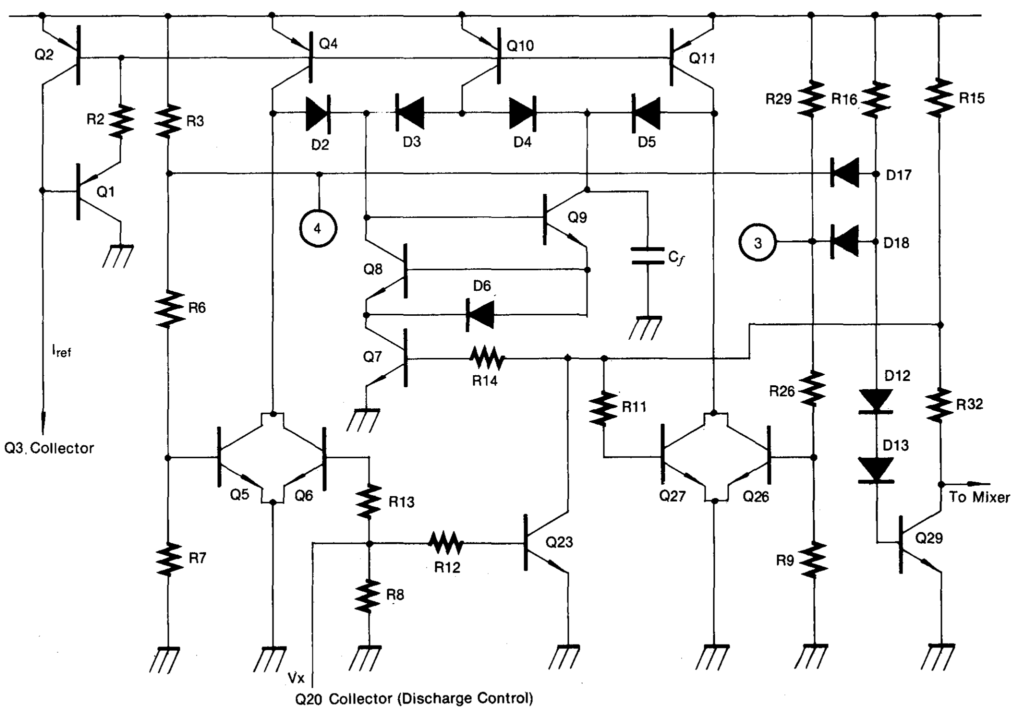


Fig. 3

The amplified functional signal fed to the RC integrator is converted into the DC level proportional to duty.

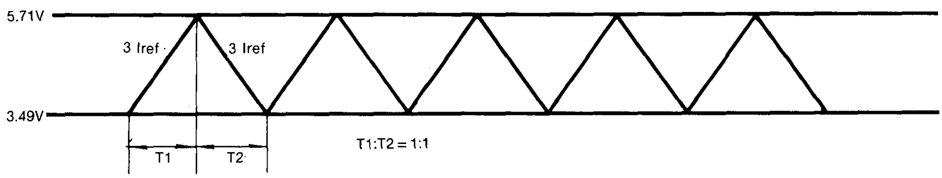
I_C (Q2): I_{ref}
I_C (Q4): 2 I_{ref}
I_C (Q10): I_{ref}
I_C (Q11): 2 I_{ref}

1. DUTY 50% (Charge:Discharge = 50:50)

Condition: Pin 3 = GND
Pin 4 = GND

1. Charge Current
When Q20 is on, V_X become high stage.
When Pin 3, Pin 4 are connected to the GND, Q5 and Q26 turns off.
The high state of V_X makes Q6, Q28 become in saturation and then Q28 is saturated and Q7, Q27, are off.
Therefore the charge current of Cf at Node B is as follows:
$I\ charge = I_C(10) + I_C(11) = I_{ref} + 2\ I_{ref} = 3\ I_{ref}$
at this time, I_C (Q4) flows through Q6, but I_C (10) cannot flow because Q7 is off.

2. Discharge Current
When Q20 turns off because of a voltage increase above 5.71V.
V_X falls into a low state, and when V_X low, then Q6 and Q28 are off.
When Q28 turns off, Q7 and Q27 on.
At this moment, the discharge current is as follows:
$I\ discharge = I_C\ (Q4) + I_C\ (10) = 2\ I_{ref} + I_C\ (10) = 3\ I_{ref}$
Therefore, it is obvious that charge current equals the discharge current.
I charge = I discharge (Duty 50%)



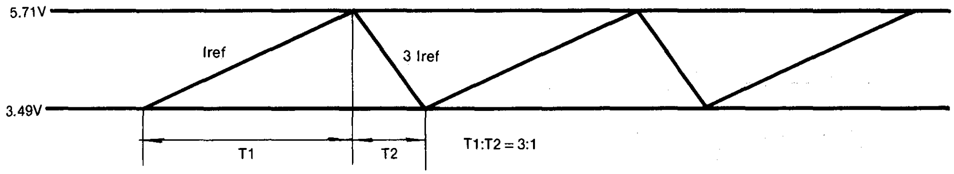
2. DUTY 25% (Charge:Discharge = 75:25)

Condition: Pin 3 = Open
Pin 4 = GND

1. Charge Current
*Q20 ON: Vx High
*Q26 turns ON in Pin 3 open state and I_C (Q11) flows through Q26.
*I charge = Ic (Q4) + Ic (Q10) = Iref

2. Discharge Current
*Q20 OFF: Vx Low
*I discharge = Ic (Q4) + Ic (Q10) = 2 Iref + Iref − 3 Iref
= 3 Iref

∴ 3 I charge = I discharge (Duty 25%)

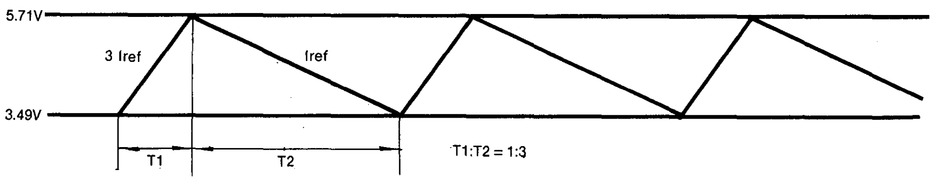


3. DUTY 75% (Charge:Discharge = 25:75)

Condition: Pin 3 = GND
Pin 4 = Open

1. Charge Current
   *Q20 ON: Vx High
   *Q5 turns ON in Pin 4 open state and I_C (Q4) flows through Q5.
   *I charge = Ic (Q10) + Ic (Q11) = Iref + 2 Iref = 3 Iref

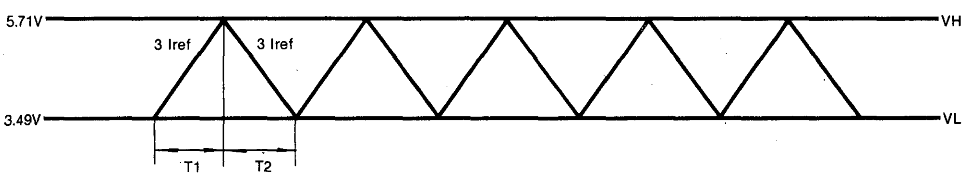
2. Discharge Current
   *Q20 OFF: Vx Low
   *I discharge = Ic (Q10) = Iref
   ∴ I charge = 3 I discharge (Duty 75%)



4. Pulse Generator Frequency

Condition: V_{CC} = 9V, Rf = 33KΩ, Cf = 0.047μF

1. Duty 50%



$Q = CV,\ Q = IT$

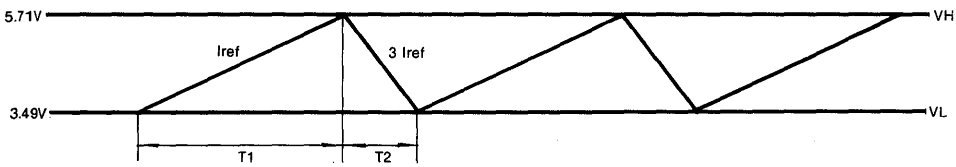
$$\therefore\ T = \frac{CV}{I}$$

$$\therefore\ T1 = \frac{(VH - VL)}{3\ Iref}C = \frac{(5.71 - 3.49)}{3 \times 285\mu A}0.047\mu F = 1.22 \times 10^{-4}\ Sec$$

$$T2 = \frac{(VH - VL)}{3\ Iref}C = \frac{(5.71 - 3.49)}{3 \times 285\mu A}0.047\mu F = 1.22 \times 10^{-4}\ Sec$$

$$\therefore\ f = \frac{1}{T} = \frac{1}{T1 + T2} = \frac{1}{2.44 \times 10^{-4}} = 4.098KHz$$

2. Duty 25%



$$T1 = \frac{(5.71 - 3.49)}{285\mu A}0.047\mu F = 3.661 \times 10^{-4}\ Sec$$

$$T2 = \frac{(5.71 - 3.49)}{3 \times 285\mu A}0.047\mu F = 1.22 \times 10^{-4}\ Sec$$

$$\therefore\ f = \frac{1}{T} = \frac{1}{T1 + T2} = \frac{1}{(3.661 + 1.22) \times 10^{-4}} = 2.049KHz$$

3. Duty 75%

$$f=\frac{1}{T}=\frac{1}{T1+T2}=\frac{1}{(1.22+3.661)\times10^{-4}}=2.049KHz$$

When Duty = 50%, the frequency doubles compared with that of 25% or 75%. Therefore, one more capacitor must be connected in parallel to use properly in an application circuit.
If so, the frequency of Duty = 50% equals that of 25% or 75%.

3) RF OSCILLATOR AND RF AMP

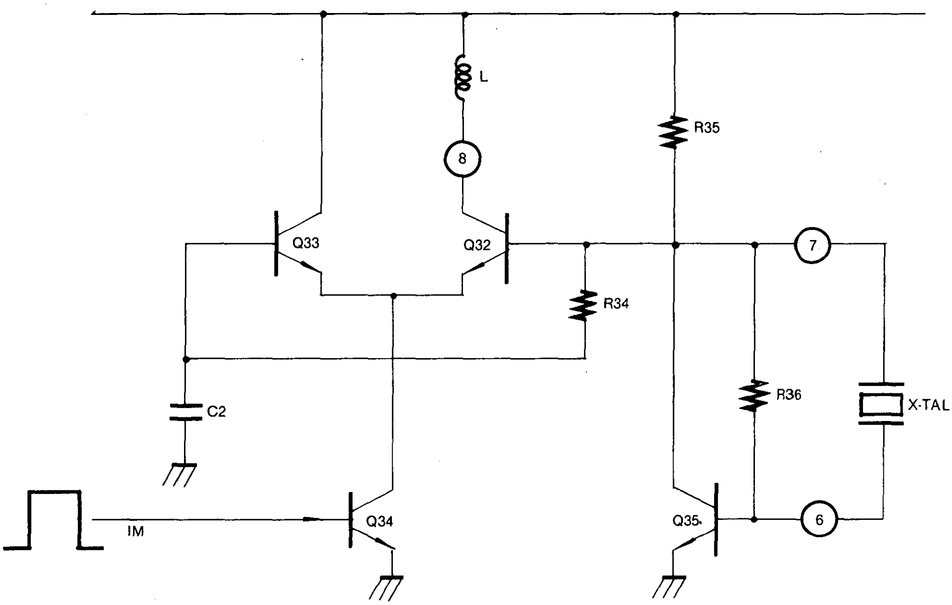


Fig. 4

RF oscillator circuit is constituted easily by Q35, R35, R36.
27MHz high frequency is amplified by Q33 and the amplified high frequency is outputted through Pin 8 when 27MHz X-TAL is external connected across Pin 6 and Pin 7.
Collector current through Q33 is controlled by Q34.
While IM flows into the base of Q34 by the signal made by pulse generator, RF signal oscillated from X-TAL is amplified and outputted through Pin 8. On the contrary when IM doesn't flow, Q34 turns off, therefore RF signal is not outputted owing to Q33 off alos.

4) WAVEFORM OF INDIVIDUAL BLOCK

Condition: $V_{CC}=9V$, Pin $3=$ Open, Pin $4=$ GND (Duty $=25\%$)

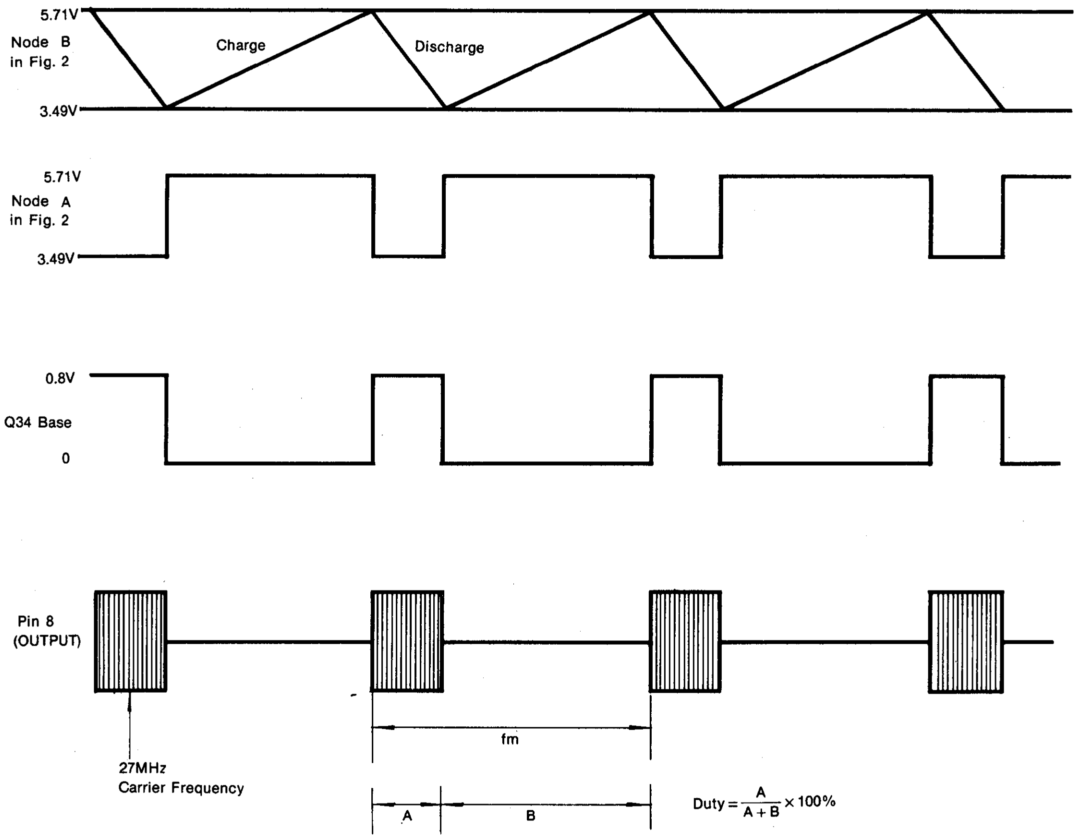


Fig. 5

27MHz signal is outputted when the capacitor connected between Pin 2 and GND discharges.

3. APPLICATION CIRCUIT AND DESCRIPTION

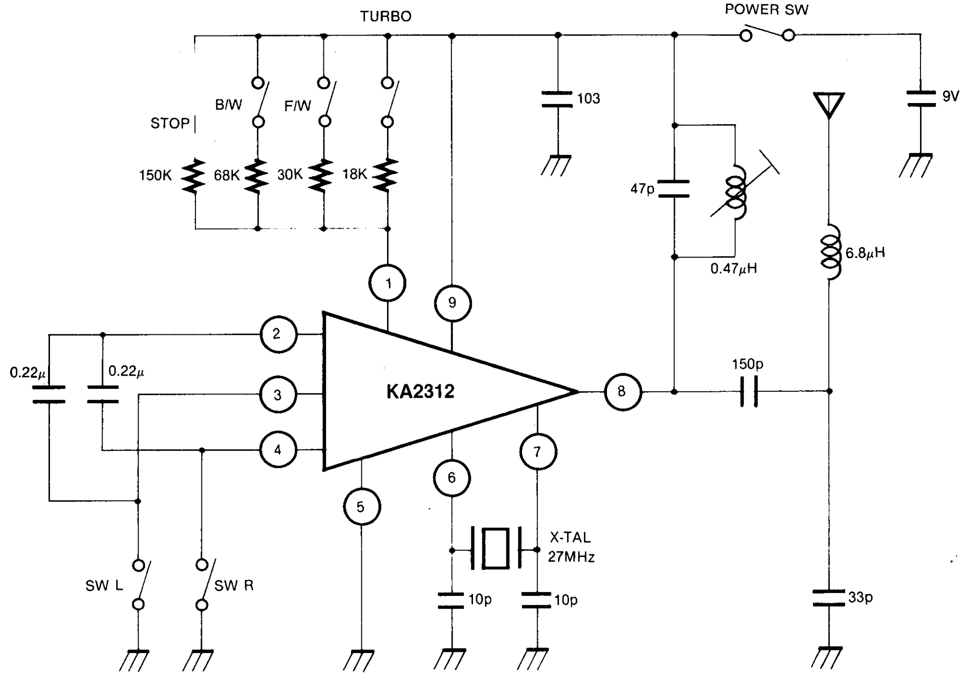


Fig. 6

Modulation frequency is determined by both the external resistor of Pin 1 and capacitor of Pin 2. Therefore the modulation frequency according to their functions depends on the resistor of Pin 1. Duty percent is determined by Pin 3, Pin 4 and when both are Pin 3 and Pin 4 are grounded, Duty percent is 50%. When Pin 3 is open and Pin 4 is grounded, Duty 25%. When Pin 3, GND and Pin 4 open, then Duty percent becomes 75%. In the case of both Pin 3, Pin 4 is ground, the modulation frequency appears double the value when of Duty = 25% or 75%. In order to obtain the same value of frequency, for this reason, the external same capacitor must be connected in parallel to Pin 2. X-TAL, which has the equal value of the desired RF signal, must be connected between Pin 6 and Pin 7. When 27MHz X-TAL is used, a 10pF capacitor should be connected between both pins and grounded, but when 49MHz X-TAL, 10pF capacitor may be connected between Pin 6 and the ground. Through these preparations, when the desired signal is made completely then outputted through Pin 8. Output level of Pin 8 can be optimized by controlling the tank coil between Pin 8 and V_{CC}.

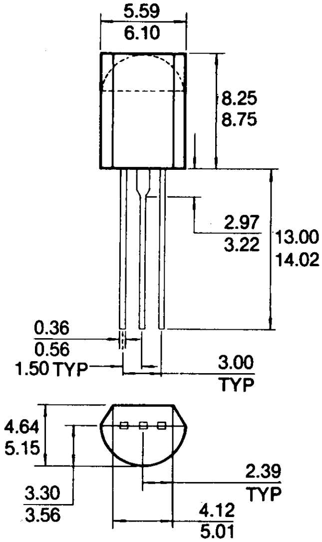
4. ATTENTION FOR PROPER USAGE

1) It is desirable that the lowest error capacitor connected to Pin 2 should be used in order to get the stable modulation frequency characteristics. (below ±2% recommended)
   Mylar capacitor is better than electrolytic capacitor in characteristics. If a high error capacitor is used, the deviation of the modulation frequency appears severe according to the individual device.
2) When the transmitted signal is over the occupied bandwidth (20KHz/Max) of FCC standard, the modulation frequency should be lowered and used.
3) In the event of mismatching impedance between the external transmitter antenna and output circuit, the duty cycle may be changed. At this event, it is necessary that the choke coil, which is connected to the TX antenna in tandem, should be changed.
   (27MHz – 6.8μH, 49MHz – 2.2μH recommended).

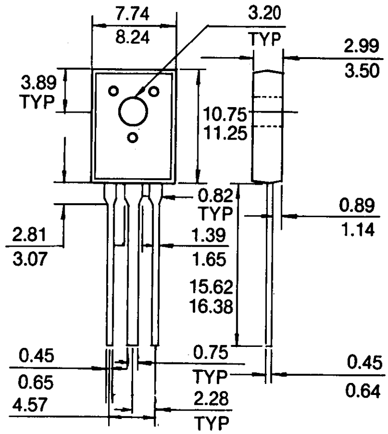
PACKAGE DIMENSIONS 6

PACKAGE DIMENSIONS

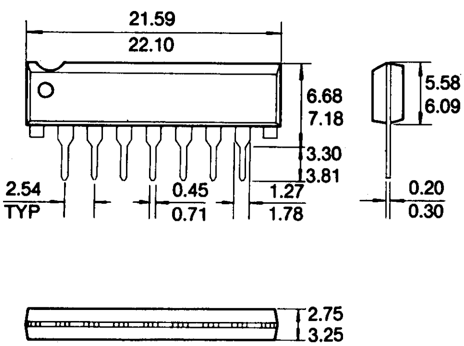
TO-92L **Unit: mm**



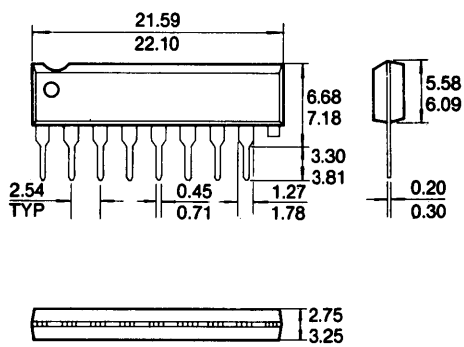
TO-126 **Unit: mm**



7 SIP **Unit: mm**

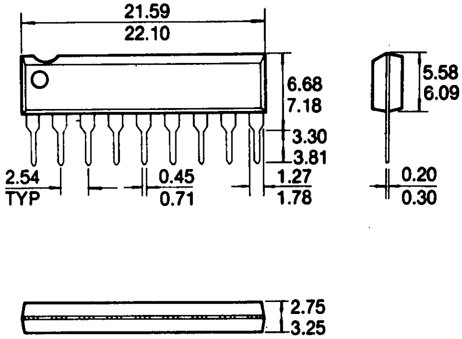


8 SIP **Unit: mm**

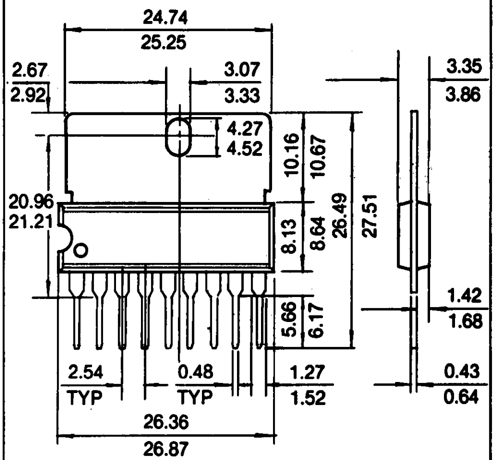


PACKAGE DIMENSIONS

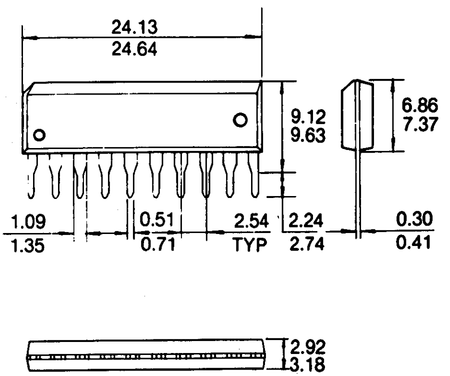
9 SIP **Unit: mm**



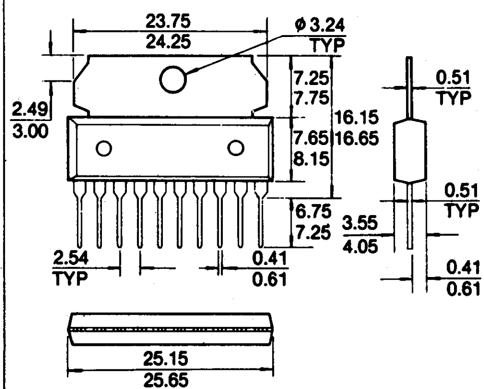
9 SIP H/S **Unit: mm**



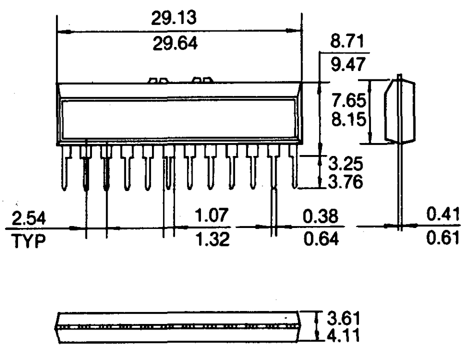
10 SIP **Unit: mm**



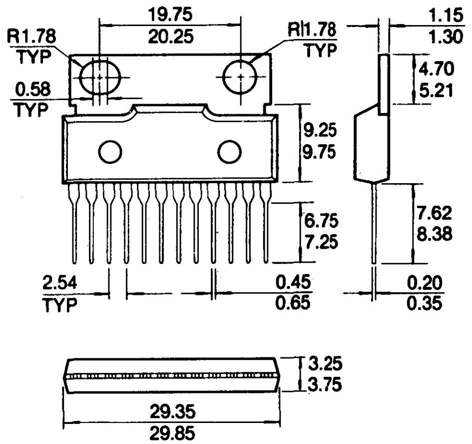
10 SIP H/S **Unit: mm**



12 SIP
Unit: mm

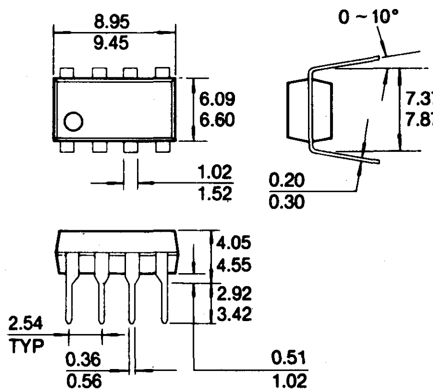


12 SIP H/S
Unit: mm

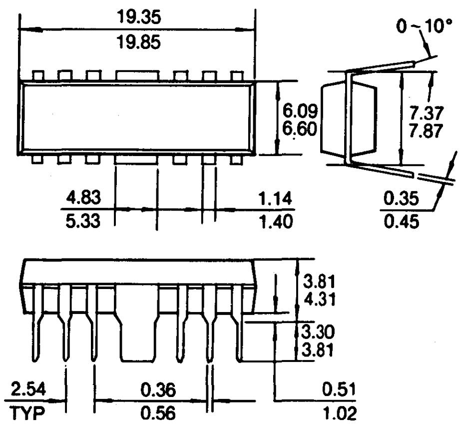


6

8 DIP
Unit: mm



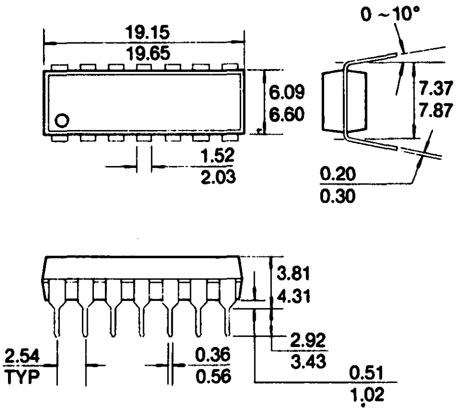
12 DIP/F
Unit: mm



PACKAGE DIMENSIONS

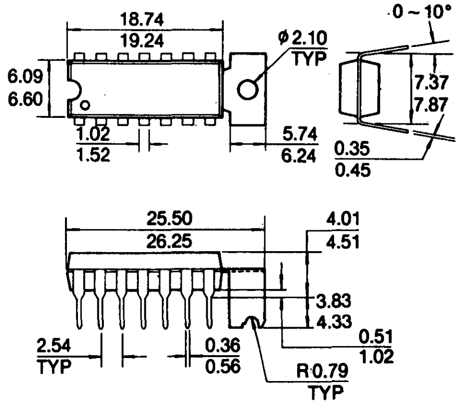
14 DIP

Unit: mm



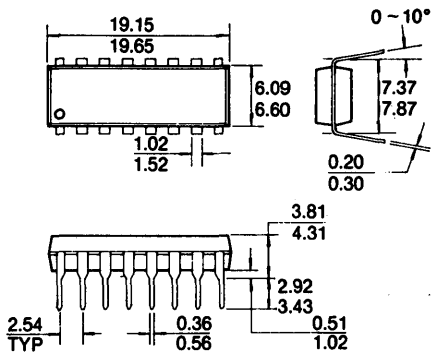
14 DIP H/S

Unit: mm



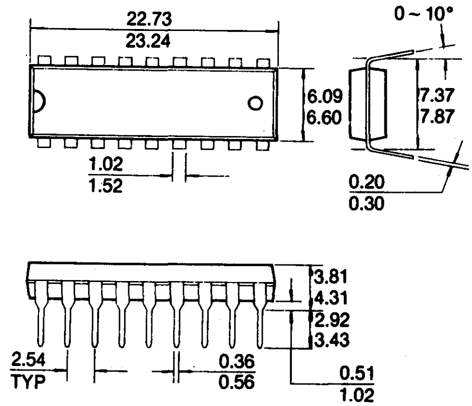
16 DIP

Unit: mm



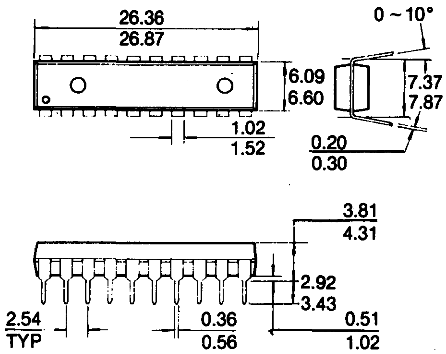
18 DIP

Unit: mm



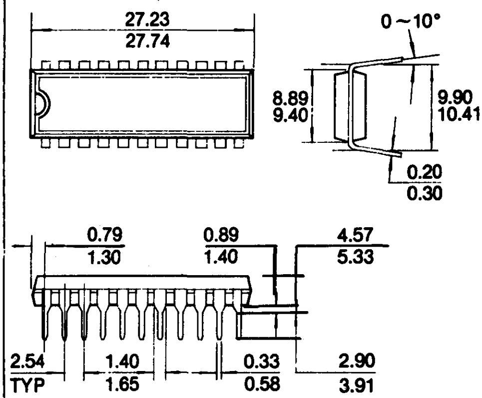
20 DIP

Unit: mm



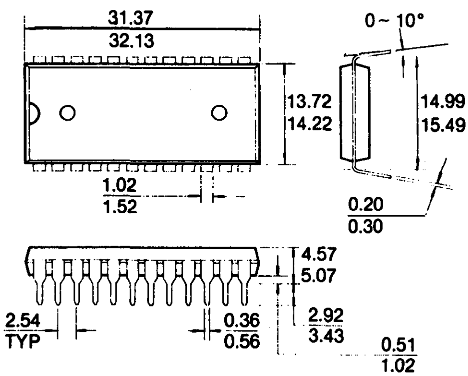
22 DIP (400)

Unit: mm



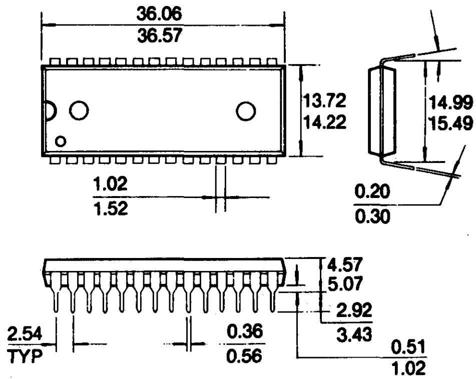
24 DIP

Unit: mm



28 DIP

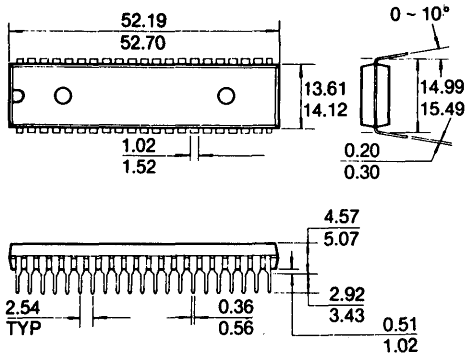
Unit: mm



PACKAGE DIMENSIONS

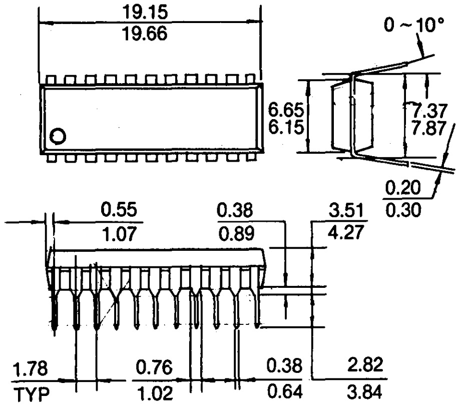
42 DIP

Unit: mm

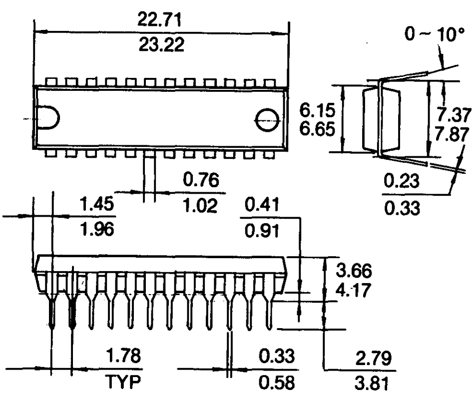


22 SDIP

Unit: mm

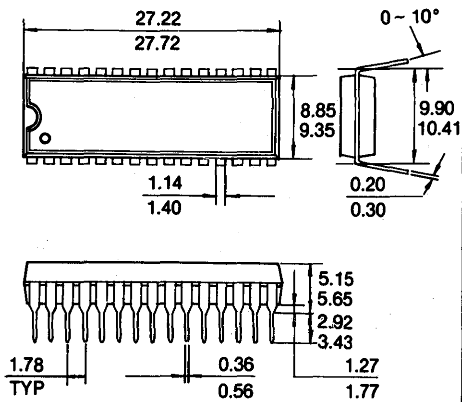


24 SDIP



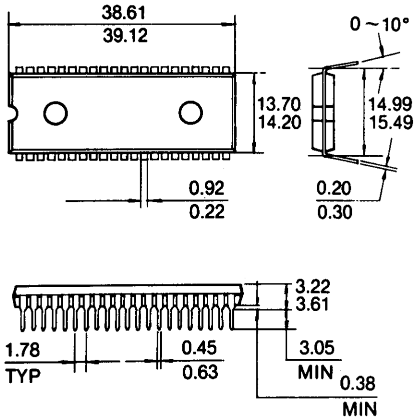
30 SDIP

Unit: mm

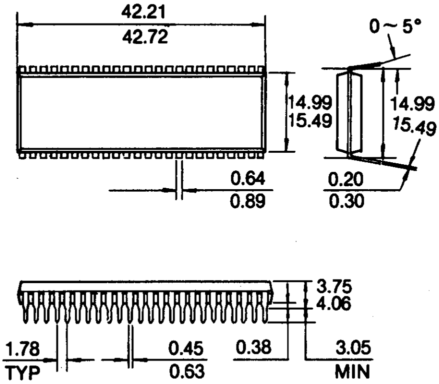


PACKAGE DIMENSIONS

42 SDIP Unit: mm

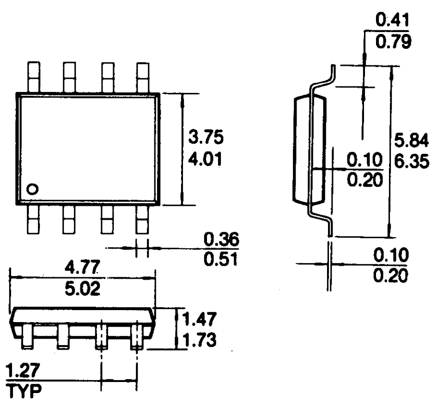


48 SDIP Unit: mm

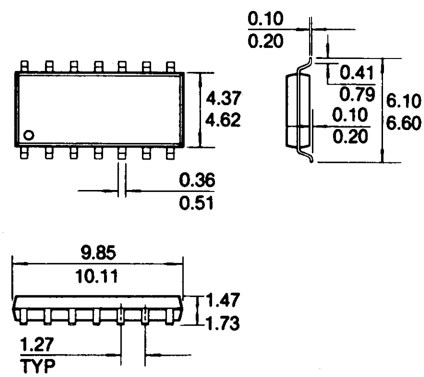


6

8 SOP Unit: mm



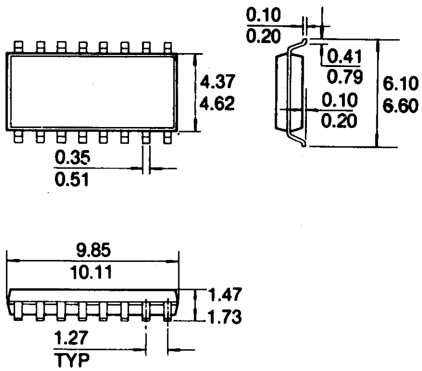
14 SOP Unit: mm



PACKAGE DIMENSIONS

16 SOP

Unit: mm



22 SOP

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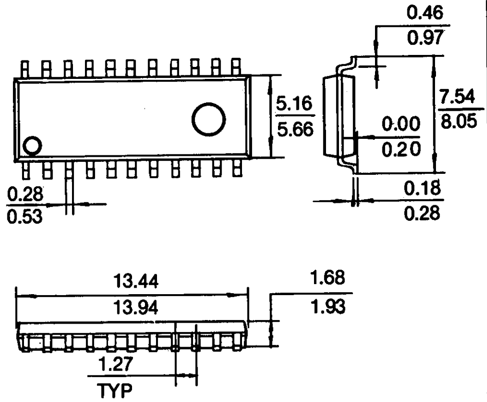
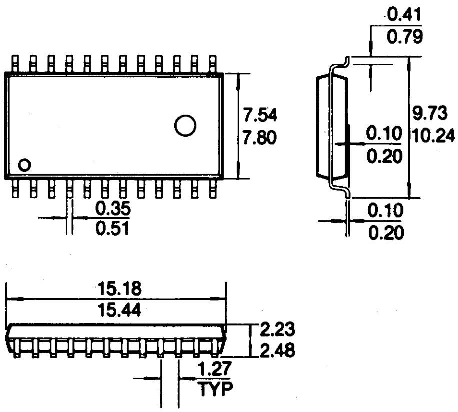


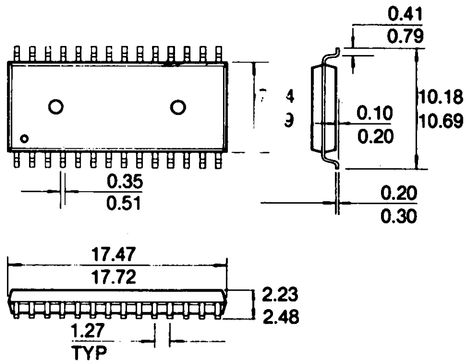
24 SOP

Unit: mm

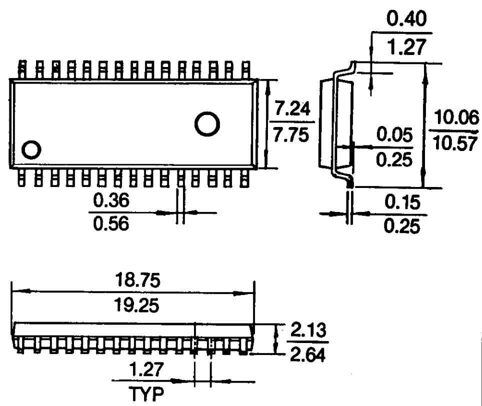


28 SOP

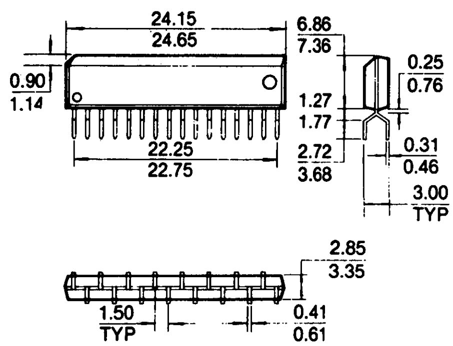
Unit: mm



30 SOP Unit: mm



16 ZIP Unit: mm



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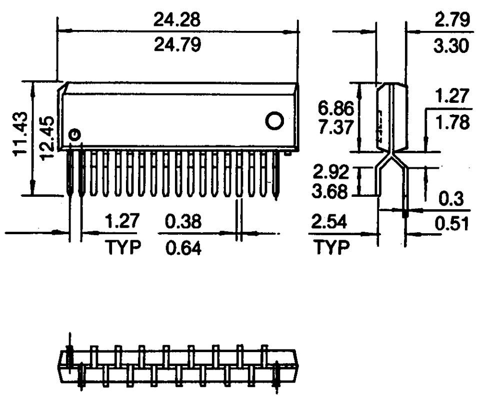

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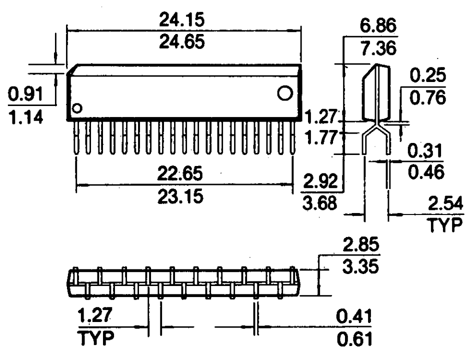

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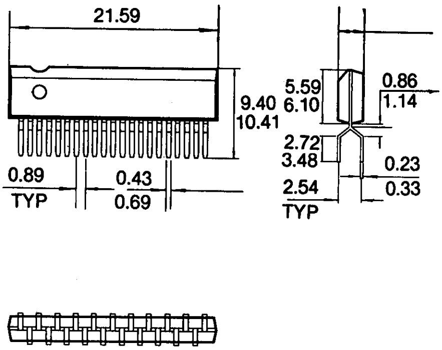

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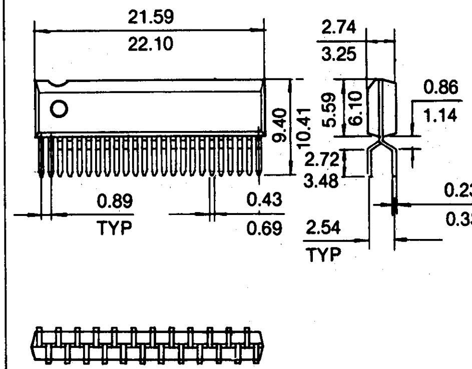

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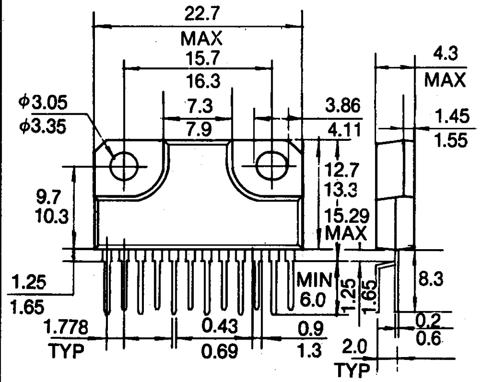

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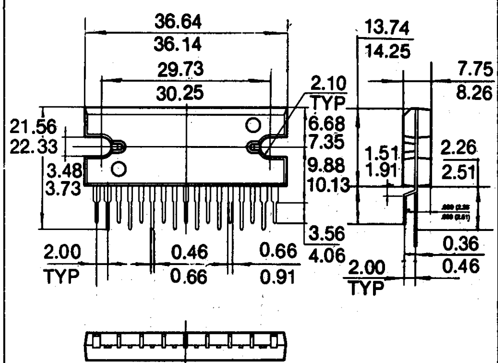

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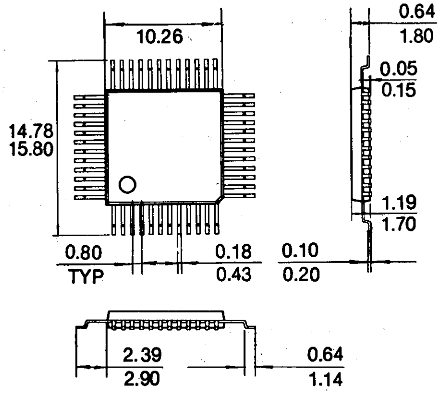

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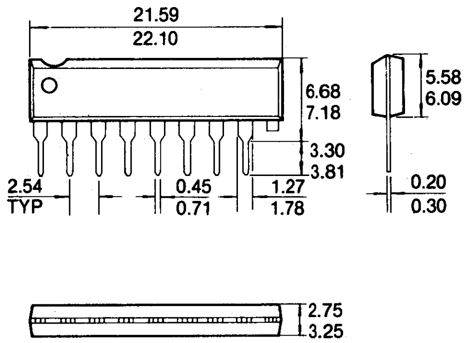

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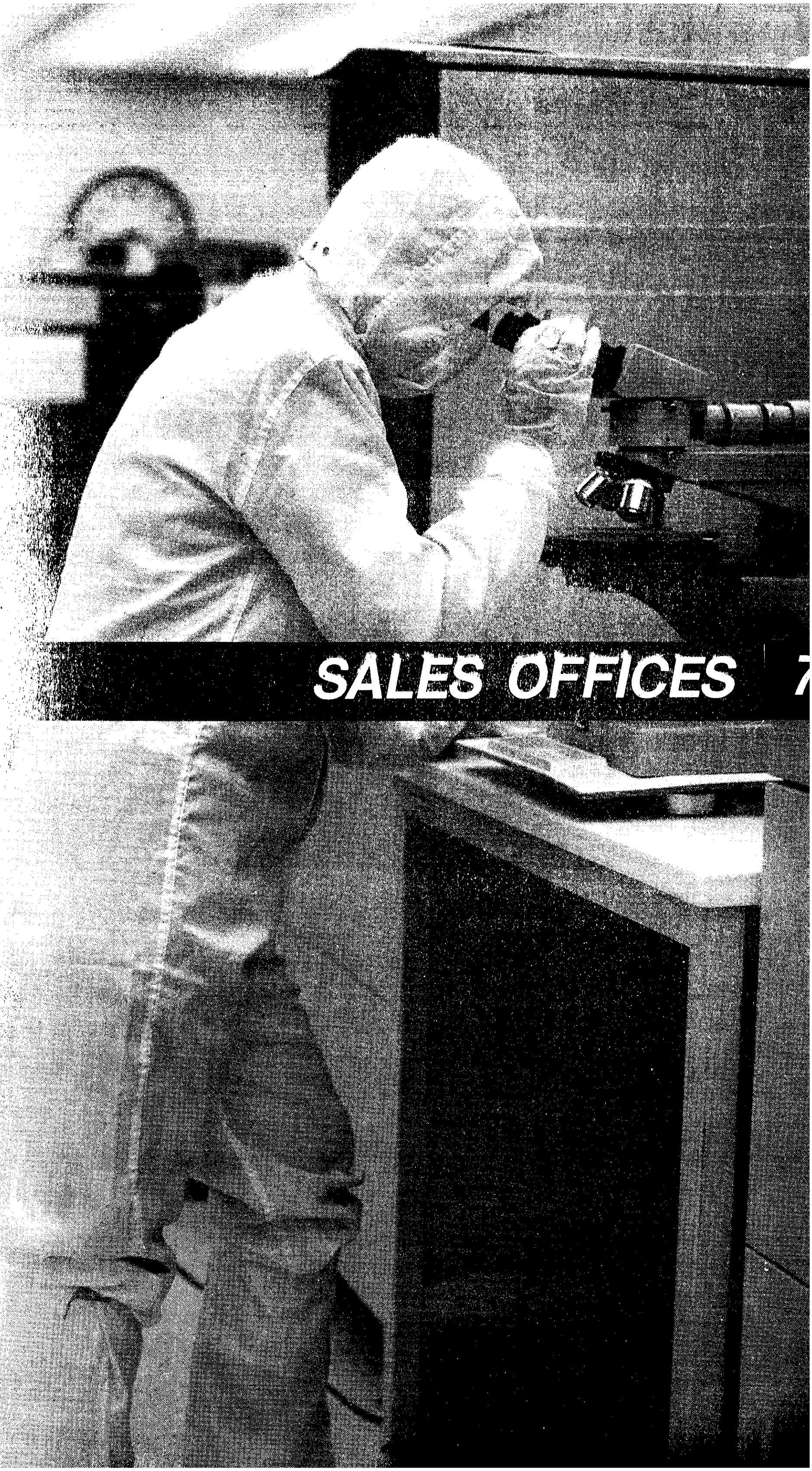

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7

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PRINTED IN KOREA
JULY, 1990