



LC89512W

CD-ROM Error Correction LSI with Built-In SCSI Interface

Preliminary

Overview

The LC89512W integrates a real-time error correction circuit and a SCSI interface in a single chip.

Functions

- CD-ROM error correction function, subcode readout function, SCSI interface

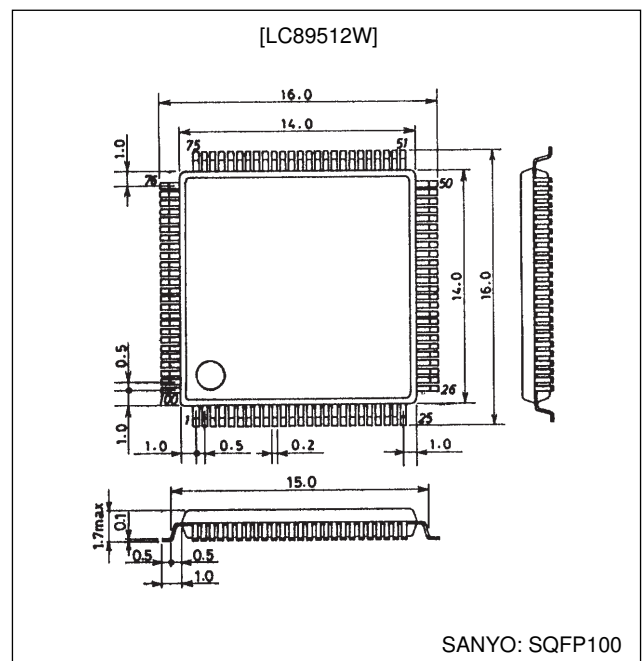
Features

- Support for double-speed drives at an operating frequency of 16.9344 MHz
Either SRAM (120 ns), DRAM (80 ns) or pseudo SRAM (85 ns) can be used.
- Support for quad-speed drives at an operating frequency of 33.8688 MHz
SRAM (70 ns) must be used.
- Built-in SCSI interface with built-in 48 mA sink buffer (Only the TARGET function is supported.)
- Built-in 12-byte output FIFO for sub-CPU to host computer data transmission
- Built-in 12-byte input FIFO for host computer to sub-CPU data transmission
- Subcode data can be written to buffer RAM and the sub-CPU can read the subcode values by connecting the LC89512 to the CD-DSP subcode pin.
- Sub-CPU access of buffer RAM through the LC89512
- Built-in function for buffer RAM internal data transfer
- Pseudo-SRAM (128-kword × 8-bit and smaller) can be used.
- DRAM (two 256-kword × 4-bit chips or two 1-Mword × 4-bit chips) can be used.
- Transfer speeds:
2.8 MB/second (asynchronous mode) (for CD-ROM decode only operation)
4.2 MB/second (synchronous mode) (CD-ROM decode operation is not supported in synchronous mode)
Both of these transfer modes use a 16.9344 MHz clock. (The transfer speed depends on the frequency used.)
- Operating frequencies: 16.9344 MHz (up to double speed), 33.8688 (quad speed)

Package Dimensions

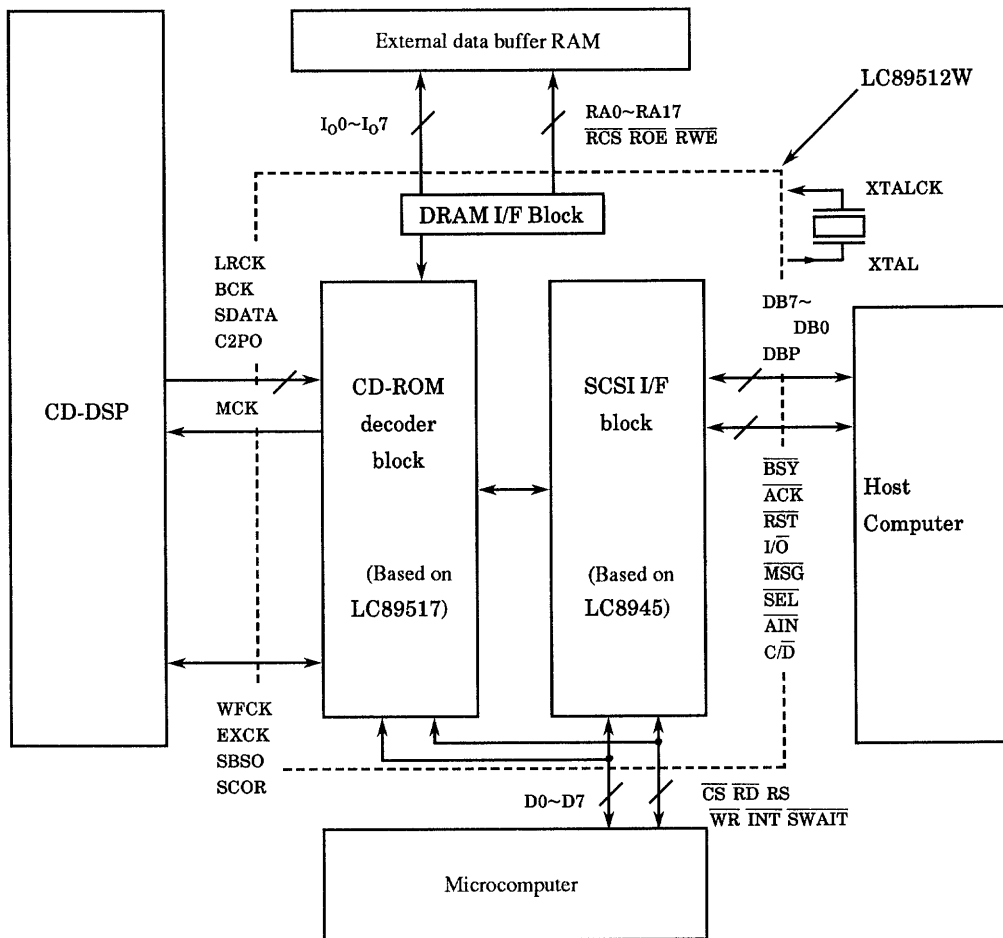
unit: mm

3181A-SQFP100



LC89512W

Block Diagram



LC89512W

Pin Functions

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Pin	Type	Function
1	$\overline{\text{DB7}}$	B	SCSI connection
2	V_{SS1}	P	
3	$\overline{\text{DBP}}$	B	SCSI connection
4	$\overline{\text{ATN}}$	B	SCSI connection
5	V_{SS1}	P	
6	$\overline{\text{BSY}}$	B	SCSI connection
7	$\overline{\text{ACK}}$	B	SCSI connection
8	V_{SS1}	P	
9	$\overline{\text{RST}}$	B	SCSI connection
10	$\overline{\text{MSG}}$	B	SCSI connection
11	V_{SS1}	P	
12	$\overline{\text{SEL}}$	B	SCSI connection
13	C/D	B	SCSI connection
14	V_{SS1}	P	
15	$\overline{\text{REQ}}$	B	SCSI connection
16	I/O	B	SCSI connection
17	V_{SS0}	P	
18	I_{O0}	B	Data buffer RAM data signals These pins have built-in pull-up resistors.
19	I_{O1}	B	
20	I_{O2}	B	
21	I_{O3}	B	
22	I_{O4}	B	
23	I_{O5}	B	
24	I_{O6}	B	
25	I_{O7}	B	
26	$\overline{\text{INT1}}$	O	SCSI block interrupt request signal output (set using a register)
27	V_{SS0}	P	
28	V_{SS0}	P	
29	D0	B	Microprocessor data signals These pins have built-in pull-up resistors.
30	D1	B	
31	D2	B	
32	D3	B	
33	D4	B	
34	D5	B	
35	D6	B	
36	D7	B	
37	$\overline{\text{INT0}}$	O	Microprocessor interrupt request signal output
38	XTALCK	I	Crystal oscillator circuit input
39	XTAL	O	Crystal oscillator circuit output
40	V_{SS0}	P	
41	V_{DD}	P	
42	RA0	O	Data buffer RAM address signal outputs
43	RA1	O	
44	RA2	O	
45	RA3	O	
46	RA4	O	
47	RA5	O	
48	RA6	O	
49	RA7	O	
50	RA8	O	
51	RA9	O	
52	RA10	O	
53	RA11	O	

Continued on next page.

LC89512W

Continued from preceding page.

Pin No.	Pin	Type	Function
54	RA12	O	Data buffer RAM address signal outputs
55	RA13	O	
56	RA14	O	
57	RA15	O	
58	RA16	O	
59	RA17	O	
60	V _{DD}	P	
61	V _{SS0}	P	
62	$\overline{\text{RESET}}$	I	Reset
63	TEST1	I	Test inputs. These pins should be tied low in normal operation.
64	TEST2	I	
65	TEST3	I	
66	WFCK	I	Subcode I/O
67	SBSO	I	
68	SCOR	I	
69	SDATA	I	Serial data input
70	BCK	I	Serial data input clock
71	LRCK	I	44.1 kHz strobe signal input
72	C2PO	I	C2 pointer input
73	$\overline{\text{RD}}$	I	Microprocessor data read signal input
74	$\overline{\text{WR}}$	I	Microprocessor data write signal input
75	$\overline{\text{CS}}$	I	Chip select signal input (from the microprocessor)
76	RS	I	Register selection signal input
77	V _{SS0}	P	
78	$\overline{\text{SWAIT}}$	O	Sub-CPU wait signal
79	EXCK	O	Sub code I/O
80	MCK	O	Crystal oscillator frequency output
81	TEST0	I	Test inputs. These pins should be tied low in normal operation
82	$\overline{\text{RCS}}$	O	RAM chip select
83	$\overline{\text{RWE}}$	O	RAM data write signal output
84	$\overline{\text{ROE}}$	O	RAM data read signal output
85		NC	
86		NC	
87		NC	
88		NC	
89	V _{DD}	P	
90	V _{SS1}	P	
91	$\overline{\text{DB0}}$	B	SCSI connection
92	$\overline{\text{DB1}}$	B	SCSI connection
93	V _{SS1}	P	
94	$\overline{\text{DB2}}$	B	SCSI connection
95	$\overline{\text{DB3}}$	B	SCSI connection
96	V _{SS1}	P	
97	$\overline{\text{DB4}}$	B	SCSI connection
98	$\overline{\text{DB5}}$	B	SCSI connection
99	V _{SS1}	P	
100	$\overline{\text{DB6}}$	B	SCSI connection

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Note: 1. NC must be left open. Do not connect any signals to these pins.

2. V_{SS0} is the logic system ground and V_{SS1} is the SCSI interface ground. (from the standard cell version)

Continued on next page.

Specifications

Absolute Maximum Ratings at $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$	$T_a = 25^\circ\text{C}$	-0.3 to +7.0	V
I/O voltages	V_I, V_O	$T_a = 25^\circ\text{C}$	-0.3 to $V_{DD} + 0.3$	V
Allowable power dissipation	$P_d\text{ max}$	$T_a \leq 70^\circ\text{C}$	350	mW
Operating temperature	T_{opr}		-30 to +70	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +125	$^\circ\text{C}$
Soldering thermal stress limit (pins only)		10 seconds	260	$^\circ\text{C}$

Allowable Operating Ranges at $T_a = -30\text{ to }+70^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage range	V_{IN}		0		V_{DD}	V

DC Characteristics at $T_a = -30\text{ to }+70^\circ\text{C}$, $V_{SS} = 0\text{ V}$, $V_{DD} = 4.5\text{ to }5.5\text{ V}$

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high level voltage	V_{IH1}	All input pins other than (1), (3), and XTALCK	2.2			V
Input low level voltage	V_{IL1}				0.8	V
Input high level voltage	V_{IH2}	$\overline{\text{RESET}}$, I_{O0} to I_{O7} , $D0$ to $D7$, $\overline{\text{RD}}$, $\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{WFCK}}$, $\overline{\text{SBSO}}$ and $\overline{\text{SCOR}}(1)$	2.5			V
Input low level voltage	V_{IL2}				0.6	V
Input high level voltage	V_{IH3}	$\overline{\text{ACK}}$, $\overline{\text{ATN}}$ and the input pins (3)	2.0			V
Input low level voltage	V_{IL3}				0.8	V
Output high level voltage	V_{OH1}	$I_{OH1} = -3\text{ mA}$: I_{O0} to I_{O7} , $D0$ to $D7$ and all output pins other than (2), (3) and XTALCK	2.4			V
Output low level voltage	V_{OL1}	$I_{OL1} = 3\text{ mA}$: I_{O0} to I_{O7} , $D0$ to $D7$ and all output pins other than (2), (3) and XTALCK			0.4	V
Output low level voltage	V_{OL2}	$I_{OL2} = 3\text{ mA}$: $\overline{\text{INT1}}$ and $\overline{\text{INT0}}$ (pull-up resistor open drain) (2)			0.4	V
Output low level voltage	V_{OL3}	$I_{OL3} = 48\text{ mA}$: $\overline{\text{DB0}}$ to $\overline{\text{DB7}}$, $\overline{\text{DBP}}$, $\overline{\text{BSY}}$, I/O , $\overline{\text{MSG}}$, $\overline{\text{SEL}}$, $\overline{\text{RST}}$, $\overline{\text{REQ}}$, C/D (2)			0.4	V
Input leakage current	I_L	$V_I = V_{SS}$, V_{DD} : All input pins	-25		+25	μA
Pull-up resistance	R_{UP}	I_{O0} to I_{O7} , $D0$ to $D7$, $\overline{\text{INT1}}$ and $\overline{\text{INT0}}$	40	80	160	$\text{k}\Omega$

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of February, 1997. Specifications and information herein are subject to change without notice.