

SANYO**ATAPI/IDE-Interface CD-ROM decoder IC****Preliminary****Functions**

Fully CAV compatible CD-DSP function, CD-ROM function, built-in ATAPI (IDE) I/F, built-in DVD-RAM I/F

Features**CD-ROM decoder, ATAPI (IDE) I/F block**

- 24x speed fully CAV compatible
- Built-in ATAPI (IDE) I/F
- 16-bit DRAM (FPM, EDO) connectable (8-bit DRAM connectable)
- Up to 32 Mbits of buffer RAM connectable (when using DVD I/F) (CD-ROM connectable up to 4 Mbits)
- CD main channel and C2 flag areas in buffer RAM can be freely set by user
- Built-in batch transfer function (function for sending CD main channel, C2 flag, etc. at one time)
- Built-in multi block transfer function (function for sending several blocks at one time)
- Built-in DVD-ECC I/F
- Built-in intelligent functions
- Inter-memory transfer function
- Fixed data embedding function

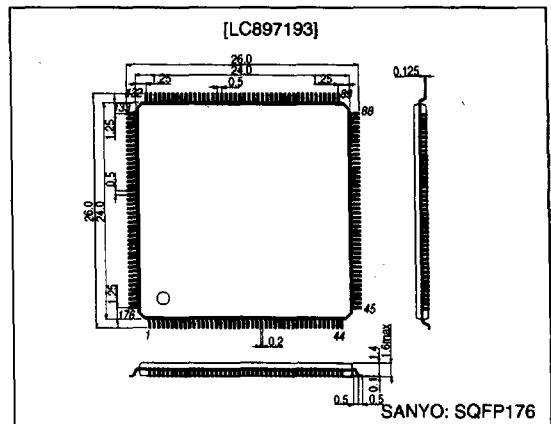
CD-DSP Block

- Slices the interface input signal at precision levels, converts the result to the EFM signal, and compares the phase with the built-in Vage-controlled oscillator.
- Generates the standard clock and other internal timing signals necessary from an external 16.9344-MHz crystal oscillator
- Detects, protects, and inserts frame synchronization signals to ensure stable data readout
- Demodulates the EFM signal to derive 8-bit symbol data
- Checks the CRC of the subcode Q signal and communicates with the microcontroller using parallel I/O
- Descrambles and de-interleaves by rearranging the demodulated EFM signal in the specified order
- Detects and corrects error signals and processes flags (C1 : dual error correction, C2 : quadruple error correction)

- Derives the C2 flag from the C1 flag and C2 check and uses it to interpolate the signal for muting. The interpolation circuit uses binary interpolation so that the C2 flag converges to the muting level at least two points.
- Uses 8-bit parallel input to receive commands from the microcontroller for jumping tracks, starting/stopping the disc motor, enabling/disabling muting, determining the track count, etc
- Supports arbitrary track count
- Built-in CAV-AUDIO support
- Uses zero cross muting
- Built-in eightfold oversampling and digital filter
- Built-in digital-to-analog converter (PWM output)
- Separate built-in digital attenuators (with 8-bit precision) for left and right channels
- Built-in digital de-emphasis
- Bilingual support

Package Dimensions

unit: mm

3230-SQFP176**SANYO Electric Co., Ltd. Semiconductor Company**

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Specifications

Absolute Maximum Ratings at $V_{SS} = 0$ V

| Parameter | Symbol | Conditions | Ratings | Unit |
|---------------------------------------|--------------|-----------------------------|------------------------|------------------|
| Maximum supply voltage | V_{DD} max | $T_a = 25^\circ\text{C}$ | -0.3 to +7.0 | V |
| Input/output voltage | V_I/V_O | $T_a = 25^\circ\text{C}$ | -0.3 to $V_{DD} + 0.3$ | V |
| Allowable power dissipation | P_d max | $T_a \leq 70^\circ\text{C}$ | 500 *2 | mW |
| Operating temperature | T_{opr} | | -30 to +70 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -55 to +125 | $^\circ\text{C}$ |
| Soldering temperature (pin part only) | | 10s | 235 | $^\circ\text{C}$ |
| Input/output current | I_I, I_O | | ± 20 *1 | mA |

Note: *1 Per 1 input/output reference cell

*2 Implement heat dissipation measures, for example by inserting a radiating sheet.
For details, contact a SANYO sales representative.

Allowable Operating Ranges at $T_a = -30$ to $+70^\circ\text{C}$, $V_{SS} = 0$ V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|------------------------------|----------|------------|---------|-----|----------|------|
| | | | min | typ | max | |
| Supply voltage | V_{DD} | | 4.75 | 5.0 | 5.25 | V |
| Input voltage range | V_{IN} | | 0 | | V_{DD} | V |
| [Internal Cell Power Supply] | | | | | | |
| Supply voltage | V_{DD} | | 3.9 | | 4.1 | V |
| Input voltage range | V_{IN} | | 0 | | V_{DD} | V |

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DC Characteristics at $T_a = -30$ to $+70^\circ\text{C}$, $V_{SS} = 0\text{ V}$, $V_{DD} = 4.75$ to 5.25 V

| Parameter | Symbol | Conditions | Ratings | | | Unit | Applicable pins* |
|---------------------------|----------|------------------------------|----------------|-----|--------------|------------------|---------------------|
| | | | min | typ | max | | |
| High-level input voltage | V_{IH} | TTL levels | 2.2 | — | — | V | 10, 13 |
| Low-level input voltage | V_{IL} | | — | — | 0.8 | V | |
| High-level input voltage | V_{IH} | TTL levels | 2.2 | — | — | V | 1 |
| Low-level input voltage | V_{IL} | with pull-up resistor | — | — | 0.8 | V | |
| High-level input voltage | V_{IH} | TTL levels | 2.2 | — | — | V | 15 |
| Low-level input voltage | V_{IL} | With pull-down resistor | — | — | 0.8 | V | |
| High-level input voltage | V_{IH} | TTL levels | 2.4 | — | — | V | 2, 3 |
| Low-level input voltage | V_{IL} | Schmitt | — | — | 0.8 | V | |
| High-level input voltage | V_{IH} | CMOS levels | $0.7 V_{DD}$ | — | — | V | 14 |
| Low-level input voltage | V_{IL} | | — | — | $0.3 V_{DD}$ | V | |
| High-level input voltage | V_{IH} | CMOS levels | $0.8 V_{DD}$ | — | — | V | 4 |
| Low-level input voltage | V_{IL} | Schmitt | — | — | $0.2 V_{DD}$ | V | |
| High-level output voltage | V_{OH} | $I_{OH} = -2\text{ mA}$ | $V_{DD} - 2.1$ | — | — | V | 5, 1, 9, 10, 15 |
| Low-level output voltage | V_{OL} | $I_{OL} = 2\text{ mA}$ | — | — | 0.4 | V | |
| High-level output voltage | V_{OH} | $I_{OH} = -4\text{ mA}$ | $V_{DD} - 2.1$ | — | — | V | 3, 6 |
| Low-level output voltage | V_{OL} | $I_{OL} = 24\text{ mA}$ | — | — | 0.4 | V | |
| High-level output voltage | V_{OH} | $I_{OH} = 2\text{ mA}$ | — | — | 0.4 | V | 7, 11 |
| Low-level output voltage | V_{OL} | $I_{OL} = 24\text{ mA}$ | — | — | 0.4 | V | 12 |
| Input leak current | I_{IL} | $V_i = V_{SS}, V_{DD}$ | -10 | — | +10 | μA | 2, 3, 4, 10, 15 |
| Output leak current | I_{OZ} | During high-impedance output | -10 | — | +10 | μA | 3, 6, 7, 10, 12, 15 |
| Pull-up resistance | R_{UP} | | 40 | 80 | 160 | $\text{k}\Omega$ | 1, 11 |
| Pull-down resistance | R_{DN} | | 40 | 80 | 160 | $\text{k}\Omega$ | 10, 15 |

Note: * Applicable pin sets are as follows.

INPUT

- 2: ZRESET, ZDMACK, ZHRST, DA0 to DA2, ZCS1FX, ZCS3FX, ZDIOR, ZDIOW, FG
- 4: ZCCTRL, ZCS, ZRD, ZWR, HFL, TES
- 14: DEFI
- 13: SUA0 to SUA6

OUTPUT

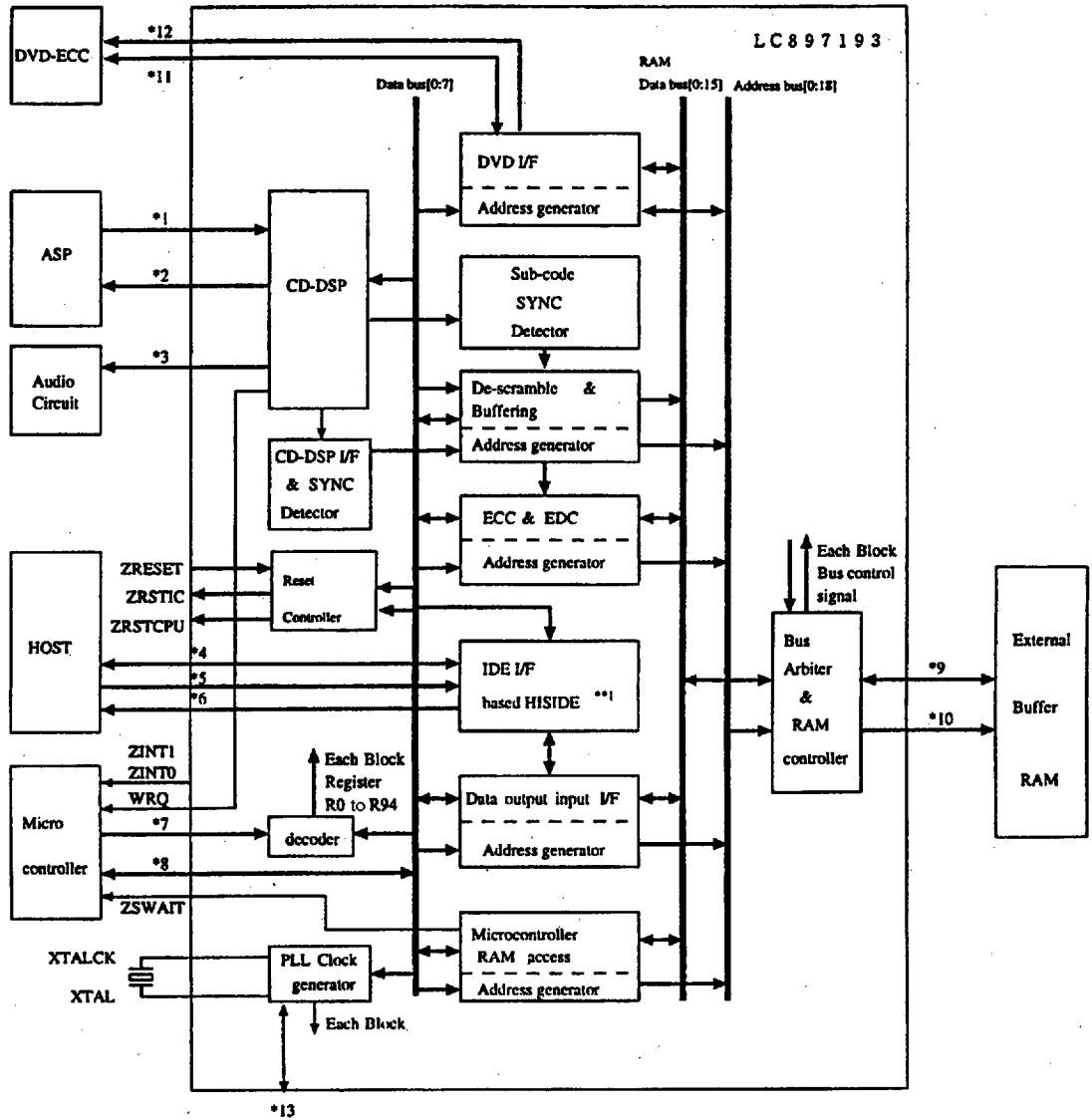
- 6: DMARQ, HINTRQ
- 5: RA0 to RA8, ZRAS0, ZCAS0, ZOE, ZUWE, ZLWE, C2F, ROMXA, FSX, EFLG, PCK, FSEQ, TOFF, TGL, 4.2M, WRQ, RWC, COIN, ZCQCK, RCHP, RCHN, LCHP, LCHN
- 7: ZRSTCPU, ZRSTIC
- 9: JP+, JP-, SPO
- 11: ZINT0, ZINT1, ZSWAIT
- 12: IORDY, ZIOCS16

INPUT/OUTPUT

- 1: D0 to D7, IO0 to IO15
- 3: DD0 to DD15, ZDASP, ZPDIAG
- 10: IOP0 to IOP7
- 15: DRESP, DREQ

Note: Pins XTAL, XTALCK, R0, VCNT0, PD00, R1, VCNT1, P011, P021, BSN1, R2, VCNT2, P012, P022, and BSN2 are not included in DC characteristics. For 1-bit DAC, measurement was made using only a logic tester, and analog measurement was not performed.

Block Diagram



- *1 DEFI, EFMI, HFL, TES
- *2 4.2M, EFMO, PCK; FSEQ, TOFF, TGL, JP+, JP-, RWC, COIN, ZCQCK
- *3 RCHP, RCHN, LCHP, LCHN
- *4 DD0 to DD15, ZDASP, ZPDIAG
- *5 ZCS1FX, ZCS3FX, DA0 to DA2, ZDIOR, ZDIOW, ZDMACK, ZHRST
- *6 DMARQ, HINTRQ, ZIOCS16, IORDY
- *7 ZRD, ZWR, ZCS, ZCCTRL, SUA0 to 6
- *8 D0 to D7
- *9 IO0 to IO15
- *10 RA0 to RA8 (RA9), ZRAS0 (ZRAS1), ZCAS0, ZOE, ZUWE, ZLWE
- *11 IOP0 to IOP7 (HDB0 to HDB7), DREQ, DRESP
- *12 (HDBDIR)
- *13 R0, VCNT0, PDO0
- **1 HISIDE (WD25C32) is made by WESTERN DIGITAL.