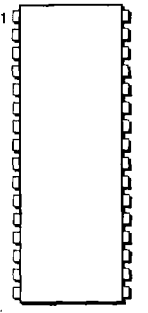
FEATURES

- ☐ Aria Synthesis
- ☐ Enhanced General MIDI Sound Samples
- ☐ Ad Lib Emulation
- ☐ Sound Blaster Emulation
- ☐ 4:1 ADPCM Compression/ Decompression
- ☐ Record and Playback
- ☐ Single 5 Volt Power Supply
- ☐ 32 pin Plastic Dip
- ☐ Low Power Dissipation
- ☐ Fully Static Operation

32 PIN DIP PACKAGE



SC18052CN

GENERAL DESCRIPTION

The SC18052 contains samples of sounds that form an enhanced General MIDI sound library and that can be run on the Aria synthesizer. The larger size of the SC18052 sound ROM translates into richer, fuller sound samples. This chip is used in conjunction with Sierra's SC18005 Audio System Controller and the SC18025 Audio Processor to make up the ST8002 Chip set.

The SC18052 is organized as 1,048,576 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and uses a single 5 Volt power supply. The device is fully static, requiring no clock operation. When the chip is not enabled, the power supply current is reduced to a 30 uA maximum.

BLOCK DIAGRAM

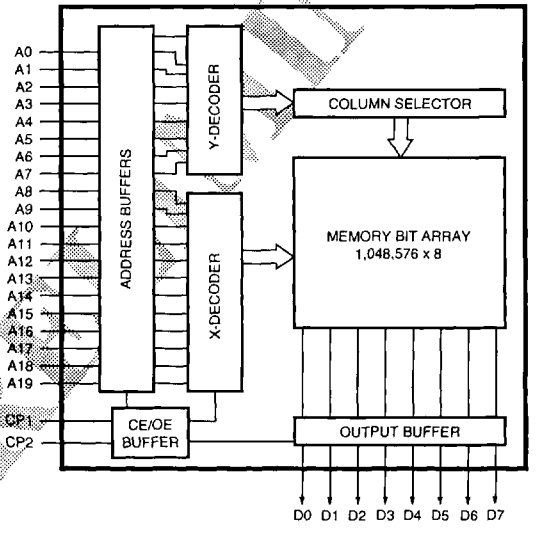


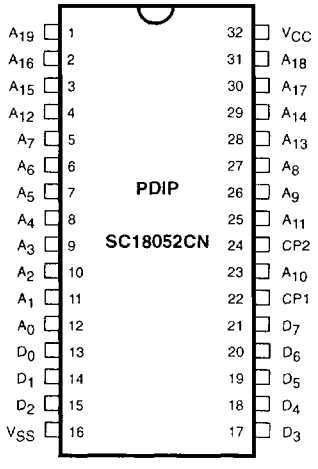
Figure 1. SC18052 (1,048,576 x 8) ROM

ıund Blaster is a registered trademark of Creative Labs Inc.
lLib is a registered trademark AdLib Inc.
llA is a trademark of Sierra Semiconductor.

PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	DESCRIPTION
A_0–A_{19}	12–5, 27–26, 23, 25, 4, 28–29, 3–2, 30–31, 1	Address inputs.
D_0–D_7	13–15, 17–21	Data outputs.
CP1, CP2	22, 24	Control pins.
V_{CC}	32	+5V supply.
V_{SS}	16	Ground.

CONNECTION DIAGRAM



CAPACITANCE $T_A = 25°C$, f = 1.0MHz

SYMBOL	PARAMETER	TEST CONDITIONS	TYP	MAX	UNIT
C_{IN}	Input capacitance	$V_{IN} = 0V$	5	5	pF
C_{OUT}	Output capacitance	$V_{IN} = 0V$	7	8	pF

TRUTH TABLE

(For simplicity, all control functions in the truth table are defined as active high.)

CP1 = CE/OE	CP2 = CE/OE	OUTPUTS	POWER
CE/OE active	CE/OE active	Data out	I_{CC}
CE inactive	X	High Z	I_{SB}
OE inactive	CE active	High Z	I_{CC}
X	CE inactive	High Z	I_{SB}
CE active	OE inactive	High Z	I_{CC}

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias – T_A	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Operating Temperature	+125°C
Input or Output Voltages	-0.3 to V_{CC}+0.3V
Maximum V_{DD}	-0.3V to 7V
Maximum Power	500mW

NOTE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those listed in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ± 10%, T_A = 0°C to 70°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{OL}	Output LOW voltage	3.2mA I_{OL}		0.4	V
V_{OH}	Output HIGH voltage	-1.0mA I_{OH}	2.4		V
V_{IL}	Input LOW voltage		-0.3	0.8	V
V_{IH}	Input HIGH voltage		2.2	V_{CC}+0.3	V
I_{LI}	Input leakage current	V_{IN} = 0V V_{CC}	-10	10	µA
I_{LO}	Output leakage current	V_0 = 0V to V_{CC}, outputs deselected	-10	10	µA
I_{CC1}	Power supply current – active	I_0 = 0, TR = t_{CYC}, duty = 100% V_I = 0.8V or 2.2V		40	mA
I_{CC2}	Power supply current – active	I_0 = 0, TR = t_{CYC}, duty = 100% V_I = GND or V_{CC}		35	mA
I_{SB}	Power supply current – standby	Chip in standby mode, V_I = GND to V_{CC}		150	µA

NOTE: It is recommended that a high frequency bypass capacitor between the power supply pin and the ground pin be utilized.

AC TIMING DIAGRAMS

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{AA}	Address access time		200	ns
t_{OH}	Output hold time	0		ns

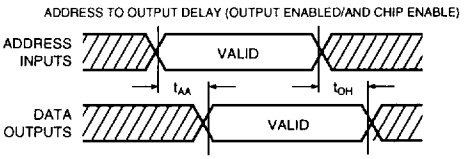


Figure 3.

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{OE}	Output enable access		80	ns
t_{OEO}	Disable time from Output Enable	0	70	ns

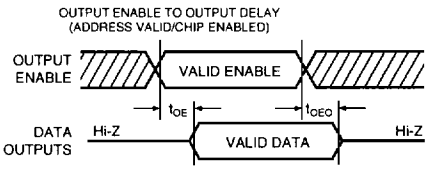


Figure 4.

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{CEO}	Disable time fromChip Enable	0	70	ns
t_{ACE}	Chip enable access time		200	ns

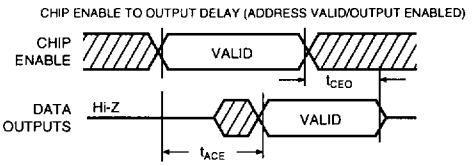
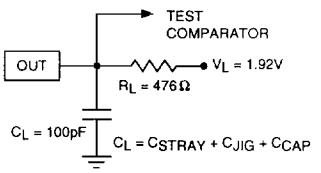


Figure 5.



AC TEST CONDITIONS

OUTPUT REFERENCE LEVELS:
LOW 0.8V
HIGH 2.0V

INPUT LEVEL:
0.6V AND 2.4V

Figure 6. Test Load