SONY® CXK78V4861BQ-33/40

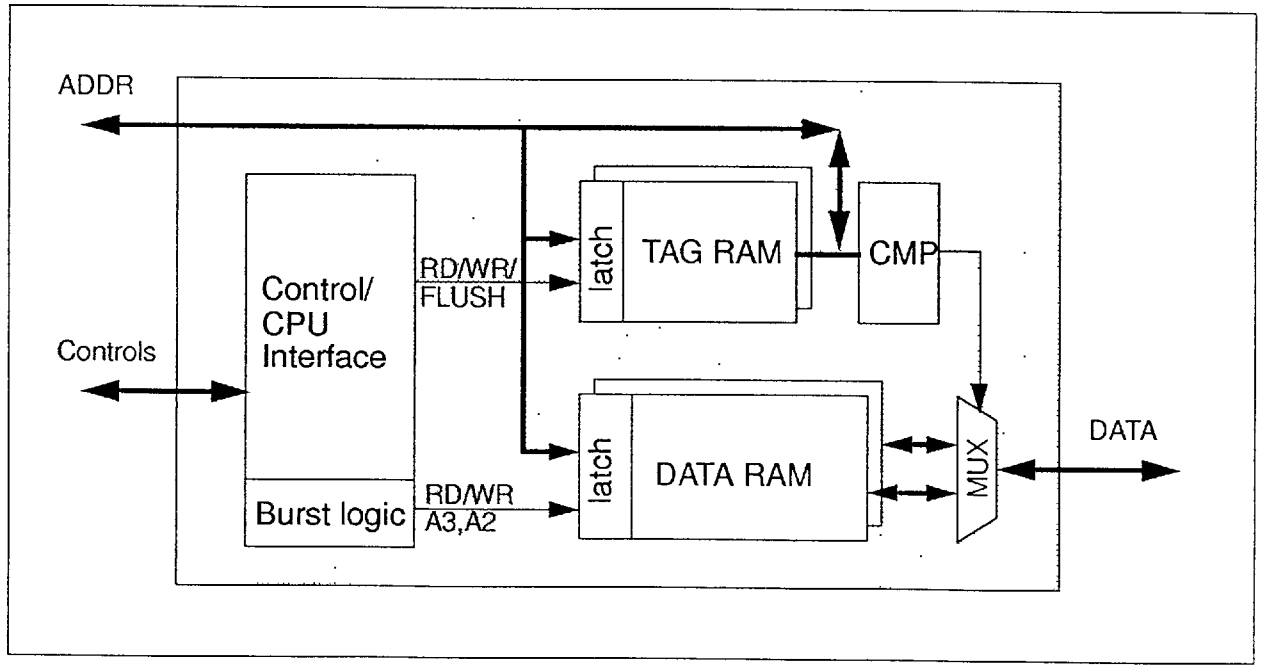
FEATURES

- Single Chip Cache Subsystem for 486-class microprocessors
- Look-aside Architecture
- Write-back and Write-through Cache Operations
- 33/40 Mhz Operating Frequency
- Zero Wait State Burst Mode (2-1-1-1)
- Single 3.3V power supply
- Low power consumption
- Power-down mode.
- 128K byte two-way-set associativity
- Supports MESI protocol
- Cascadable to 256K bytes
- Enhanced Cascade Mode
- Supports both 486 and linear burst modes
- 160-pin PQFP

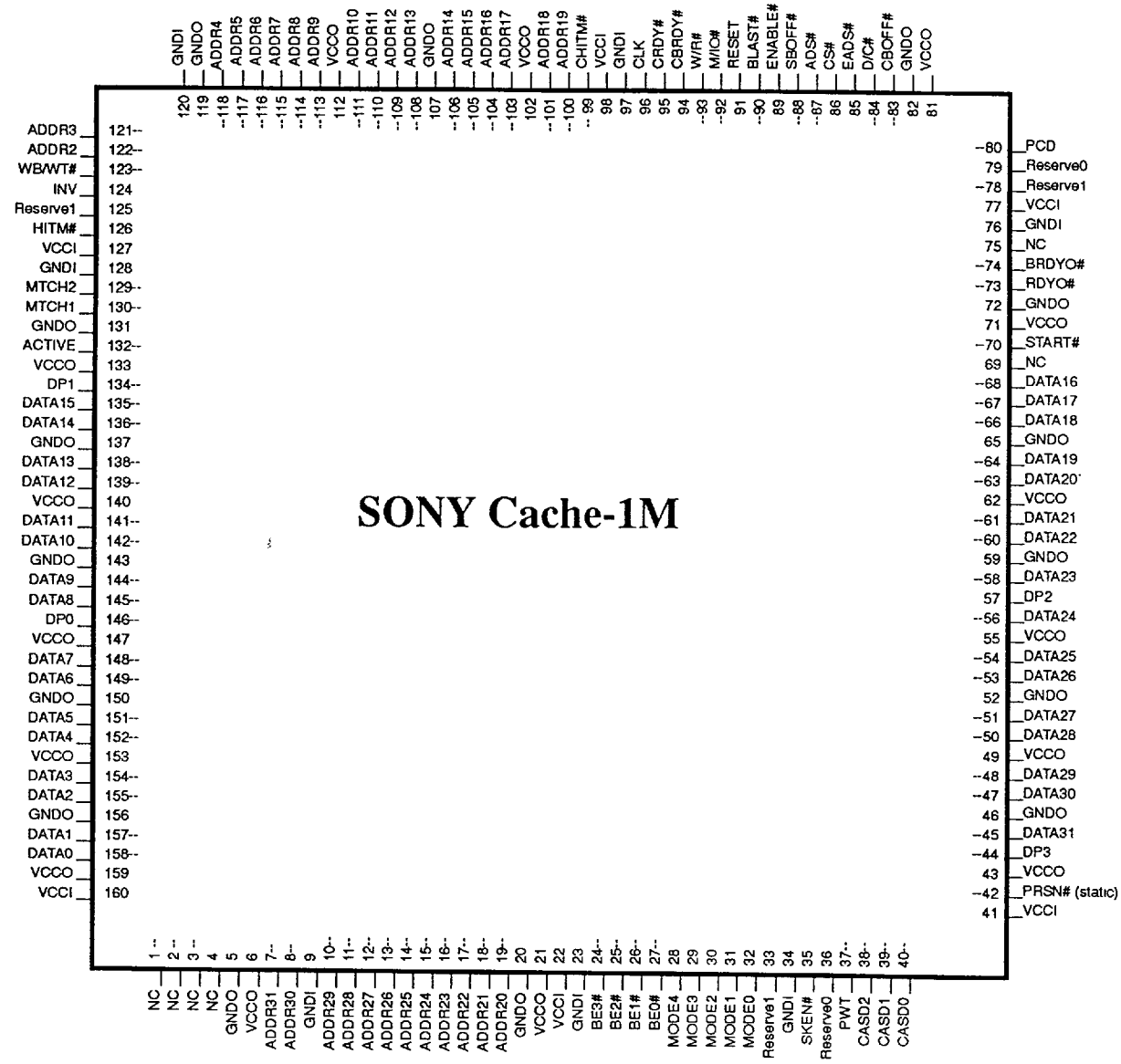
DESCRIPTION

The SONY Cache-1M is a single chip cache subsystem designed to work with various 486-class microprocessors. The SONY Cache-1M is designed specifically for mobile computing applications with 3.3V operation and very low power consumption. It is designed utilizing SONY's proprietary Memory-intensive ASIC (MASIC™) technology. Using MASIC, the SONY Cache-1M integrates 128K bytes of cache memory, tag ram and associated control logic on a single chip. As a look-aside secondary cache, this device can be designed onto a motherboard as a standard or an upgrade feature. Systems designed with the SONY Cache-1M can be upgraded seamlessly to 256K bytes by cascading two SONY Cache-1M chips using the built-in Enhanced Cascade feature. The write back mode improves bus utilization and reduces power consumption of the system DRAM. High performance, high integration, low power and 3.3V characteristics render this device ideal for mobile computing applications

SONY Cache-1M BLOCK DIAGRAM



1 SONY Cache-1M Pinout



Notes

VCCO and VCCI should both be connected to the 3.3V power supply. VCCO is used for outputs and VCCI is used for internal and input buffers.

GNDO and GNDI should both be connected to the ground reference. GNDO is used for outputs and GNDI is used for internal and input buffers.

Figure 1.1. SONY Cache-1M Pin Assignment (160-pin PQFP)

Top View

1.1 Table of Package Pin Numbers & Pin Names

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	(static) ID2	41	VCCI	81	VCCO	121	ADDR3
2	(static) ID1	42	(static) PRSN#	82	GNDO	122	ADDR2
3	(static) ID0	43	VCCO	83	CBOFF#	123	WB/WT#
4	NC	44	DP3	84	D/C#	124	INV
5	GNDO	45	DATA31	85	EADS#	125	FLUSH#
6	VCCO	46	GNDO	86	CS#	126	HITM#
7	ADDR31	47	DATA30	87	ADS#	127	VCCI
8	ADDR30	48	DATA29	88	SBOFF#	128	GNDI
9	GNDI	49	VCCO	89	ENABLE#	129	MTCH2
10	ADDR29	50	DATA28	90	BLAST#	130	MTCH1
11	ADDR28	51	DATA27	91	RESET	131	GNDO
12	ADDR27	52	GNDO	92	M/IO#	132	ACTIVE
13	ADDR26	53	DATA26	93	W/R#	133	VCCO
14	ADDR25	54	DATA25	94	CBRDY#	134	DP1
15	ADDR24	55	VCCO	95	CRDY#	135	DATA15
16	ADDR23	56	DATA24	96	CLK	136	DATA14
17	ADDR22	57	DP2	97	GNDI	137	GNDO
18	ADDR21	58	DATA23	98	VCCI	138	DATA13
19	ADDR20	59	GNDO	99	CHITM#	139	DATA12
20	GNDO	60	DATA22	100	ADDR19	140	VCCO
21	VCCO	61	DATA21	101	ADDR18	141	DATA11
22	VCCI	62	VCCO	102	VCCO	142	DATA10
23	GNDI	63	DATA20	103	ADDR17	143	GNDO
24	BE3#	64	DATA19	104	ADDR16	144	DATA9
25	BE2#	65	GNDO	105	ADDR15	145	DATA8
26	BE1#	66	DATA18	106	ADDR14	146	DP0
27	BE0#	67	DATA17	107	GNDO	147	VCCO
28	MODE4	68	DATA16	108	ADDR13	148	DATA7
29	MODE3	69	NC	109	ADDR12	149	DATA6
30	MODE2	70	START#	110	ADDR11	150	GNDO
31	MODE1	71	VCCO	111	ADDR10	151	DATA5
32	MODE0	72	GNDO	112	VCCO	152	DATA4
33	Reserve1	73	RDYO#	113	ADDR9	153	VCCO
34	GNDI	74	BRDYO#	114	ADDR8	154	DATA3
35	SKEN#	75	NC	115	ADDR7	155	DATA2
36	Reserve0	76	GNDI	116	ADDR6	156	GNDO
37	PWT	77	VCCI	117	ADDR5	157	DATA1
38	CASD2	78	LOCK#	118	ADDR4	158	DATA0
39	CASD1	79	LOCKEN	119	GNDO	159	VCCO
40	CASD0	80	PCD	120	GNDI	160	VCCI

2 PIN LIST

2.1 Address:

ADDR[31:2]	I/O	Address pins shared by the CPU and the cache subsystem on the host bus. The address pins are normally inputs and are driven by the SONY Cache-1M only during write-back cycles.
BE#[3:0]	I/O	Byte enable. These signals allows individual bytes within a double-word to be written independently during write hit operations. They are ignored in read hit cycles because all fours bytes are transferred regardless of BE#. During read miss cycles, BE# is ignored if the miss cycle is not converted to line fill. If the miss cycle is converted to line fill, the system logic must return all four bytes with valid data regardless of BE#. The BE# signals are also used by the SONY Cache-1M to decode flush special bus cycle driven by the CPU. All BE# signals are driven active(low) by the SONY Cache-1M during write-back cycles.

2.2 Data:

DATA[31:0]	I/O	Data pins on the host bus.
DP[3:0]	I/O	Data parity. One parity bit for each data byte. The SONY Cache-1M does not perform parity check. These bits are read and written like other data bits. The parity bits are associated with each data byte in the following order: DATA[31:24] DP[3] DATA[23:16] DP[2] DATA[15:8] DP[1] DATA[7:0] DP[0]

2.3 Control (input and I/O):

ADS#	I/O	Address strobe. Should be connected to the ADS# signal of the CPU. Used by the CPU to indicate the beginning of an memory or I/O cycle. During write-back operation, ADS# is driven by the SONY Cache-1M to indicate the beginning of a write-back cycle.
BLAST#	I/O	End-of-Burst indicator. Indicates the end of a burst cycle. This signal is normally driven by the CPU and is driven by the SONY Cache-1M only during write-back cycles.

BRDYO#	I/O	Burst data ready. It is asserted during read hit to indicate that data is available to the CPU. It is also asserted during write hit to write back lines to indicate that the SONY Cache-1M is ready to receive the next burst data. It can be connected externally with CBRDY# to form an IO pin. When BRDYO# is not asserted, it is driven high for one cycle and then tri-stated.
CASD[2:0]	I/O	These pins are reserved for communications between the SONY Cache-1M chips when used in cascade mode. Currently only CASD[1] and CASD[0] are used. See section 4.11 for more detail.
CBOFF#	I/O	(Previously called WBACK#) This signal is driven by the SONY Cache-1M to indicate that it needs to acquire the host bus in order to start a write-back cycle. This pin is used as an I/O pin during cascade mode for inter-chip communication. The CBOFF# signals of the two cascaded chips must be connected together to form an output pin. In stand-alone and in cascade mode, this pin must not be driven by any external device even if the pin is not used.
CBRDY#	I	Cache data burst ready. Generated by the system logic to indicate that data are available from the system memory and that burst mode transfer is used. This pin can be connected externally to BRDYO# to form an I/O pin that can be directly connected to the BRDY# input of the CPU. See section 4.1 for more detail.
CLK	I	System clock. Same as the 486 1X clock.
CRDY#	I	Cache data ready. Terminates the current bus cycle and stops the burst transfer. CRDY# can be connected externally to RDYO# to form an I/O pin. See section 4.2 for more detail. CRDY# has precedence over CBRDY#. If both are asserted at the same cycle during a burst transfer, the burst transfer is terminated.
CS#	I	Chip Select. This signal must be asserted with ADS# and EADS#; otherwise ADS# and EADS# are ignored. When the SONY Cache-1M is used in enhanced cascade mode, CS# must be tied low.
D/C#	I/O	Data/Code select. This signal is used together with M/IO#, W/R# and BE#'s to decode special bus cycles for flush. In other memory accesses, this signal is ignored. This signal is driven high during SONY Cache-1M generated write-back cycles.

EADS#	I	External Address Strobe. The SONY Cache-1M performs a snoop cycle when EADS# is active. The snoop address is sampled at the same time as EADS# is sampled low. If the snoop address hits a cache line that contains modified data, the cache line is written back to the system memory. EADS# can be asserted every other cycle. When the cache is operated in write-back mode, EADS# should be asserted no faster than once every three cycles because the snooping device must interpret the snoop output (on CHITM#) before generating another EADS# cycle. EADS# is not allowed during data transfer and during write-back cycles. See section 3.4 for more detail. When EADS# is asserted at the same time as ADS#, it becomes a special case. See section 3.5 for more detail.
ENABLE#	I	If this signal is inactive, the cache is in power down mode; otherwise the system is in normal operation mode. During power down, all external signals including RESET are ignored.
FLUSH#	I	When FLUSH# is asserted, the SONY Cache-1M sets an internal flag and then waits for a flush acknowledge cycle generated by the CPU or level one (L1) cache. When the flush acknowledge cycle is detected, the SONY Cache-1M starts its flush sequence in the same way as a software flush operation. See section 3.6 on software flush for more detail. Flush acknowledge cycle is defined as any I/O cycle that follows after FLUSH# has been asserted. The ADS# assertion for the acknowledge cycle must be at less two cycles after the assertion of FLUSH# in order for the acknowledge cycle to be recognized. FLUSH# is double synchronized internally by the SONY Cache-1M and the signal is edge sensitive.
HITM#	I	This signal should be driven by the L1 cache to indicate snoop hit on modified data there. HITM# is sampled two cycles after EADS# is asserted. If it is active, the SONY Cache-1M cancels its snoop write-back cycle and allows the L1 cache to proceed with its own write-back. The SONY Cache-1M also preserves its cache status until the write-back from the L1 cache has taken placed. HITM# is also sampled during write cycles. If it is active, the SONY Cache-1M assumes that the CPU is performing a snoop write-back. It updates the cache line and forces the cache line to write-through state after the write cycle is completed. If the previous snoop cycle was driven with INV active, the modified cache line within the SONY Cache-1M is invalidated.
INV	I	Snoop and invalidate. It is sampled at the same time as EADS#. If INV is active and the snoop address is hit, the cache line is invalidated. If write back is required due to modified data, invalidation takes place after write-back is completed. If INV is inactive, the cache line is converted into write-through state.

LOCK#	I/O	The LOCK# signal is sampled at the same time as ADS# is asserted and it is qualified by the LOCKEN signal. If LOCK# is asserted, read miss will not trigger a line fill. If it is a read hit to clean data, the SONY Cache-1M will not provide data. Instead the cycle will be treated as non-cacheable read miss. If it is a read hit to modified data, a special coordinate read cycle is created. The cache will signal a read miss by asserting START# and then monitor the BRDY# input and at the same time drive the modified data on to the data bus. Locked write hit will always be treated as write to write-through lines and the cache line status is unchanged. The lock feature can be disabled by connecting LOCK# or LOCKEN to inactive. During write-back cycles generated by the SONY Cache-1M, LOCK# is driven high.
LOCKEN	I	Lock enable. This signal qualifies the LOCK# input. See LOCK# definition for more detail. Systems not designed to handle coordinate read should have LOCKEN connected to logic zero.
M/IO#	I/O	Memory and I/O selector. Memory is selected if this signal is high, otherwise I/O is selected. Only memory data can be cached. I/O access are not cacheable and I/O cycles are not paced. The M/IO# is also used for decoding flush special cycle and flush acknowledge cycles. M/IO# is driven high during SONY Cache-1M generated write-back cycles.
MODE[4:0]	I	Operation mode selector. Selects between normal, cascade and test mode and between linear and 486 burst mode. MODE[4] = 0: 486 burst mode. MODE[4] = 1: Linear burst mode. Normal, enhanced cascade and test mode can be selected by MODE[3:0] independent of burst mode: MODE[3:0[= 0000: normal mode. MODE[3:0] = 1100: enhanced cascade, chip 0. MODE[3:0] = 1101: enhanced cascade, chip 1. Other combinations: reserved.
NC		"No connect" pins. The NC pins should not be driven by any external logic. Some of the NC pins may be driven by the SONY Cache-1M

PCD	I/O	Page Cache Disable. This signal is connected to the PCD output of the CPU. If PCD is active during line fill, the cache line is not cacheable in SONY Cache-1M. PCD is ignored during read hit cycles. If it is active during write hit, the write cycle is handled by the SONY Cache-1M like a write-through cycle, regardless of the cache line status. PCD is ignored during write miss. This signal is driven by the CPU and is sampled at the same time as ADS#. During write-back cycles initiated by the SONY Cache-1M, PCD is driven inactive.
PWT	I/O	Page Write-through. If PWT is active during line fill, the data is cached in as write-through, regardless of the status of the WB/WT# signal. A line fill is cached in as write-back only if PWT sampled low and WB/WT# sampled high. If PWT is active during write hit, the write cycle is treated as write-through regardless of cache line status. It is ignored in write miss cycles. PWT is driven by the CPU and is sampled at the same time as ADS#. During write-back cycles initiated by the SONY Cache-1M, PWT is driven inactive.
RESET	I	Resets the SONY Cache-1M to the initial state and invalidates all the tag entries. Modified data, if any, are not written back to system memory.
Reserve0	I	These pins must be tied to a 10K ohm pull-down resistor.
Reserve1	I	These pins must be tied to a 10K ohm pull-up resistor.
SBOFF#	I	The SBOFF# signal is driven active by the system when it need to back off both the CPU and the SONY Cache-1M. The system should not back off the CPU and the SONY Cache-1M if it is running a burst sequence after one or more data transfer has taken place. SBOFF# must also remain de-asserted once a snoop write-back or cast-out write-back operation has started. ADS# is ignored when SBOFF# is active.
SKEN#	I	Cacheability indicator. This signal is sampled by the SONY Cache-1M to determine if a line fill is cacheable. It is sampled twice during a line fill. It is first sampled during the clock cycles between ADS# and the first CBRDY#. It is sampled again one clock cycles before the last CBRDY# of the line fill. SKEN# must be active during both sampling point; otherwise the line fill is not cacheable. The system logic must assert the KEN# input to the CPU during read hit cycles so that read hit on the SONY Cache-1M is cacheable to the L1 cache.

START#	I/O	Driven by the SONY Cache-1M to start a memory access for read miss, write miss, or write-through cycles. When the access is initiated by the CPU, START# is asserted one cycle after ADS# if needed. When the access is initiated by the SONY Cache-1M for write-back, START# is asserted at the same time as ADS# is asserted by the SONY Cache-1M. START# is de-asserted (driven high) during reset cycles so that it can be used by the system to detect the present of the SONY Cache-1M.
W/R#	I/O	Read/Write select. High indicates a write cycle and low indicates a read cycle. It is driven high during a SONY Cache-1M initiated write-back.
WB/WT#	I/O	WB and WT indicator. This signal is driven by the system memory during line fill to indicate the cache policy. It is also driven by the SONY Cache-1M during read hit or write hit to write back lines to indicate the cache policy of the cache line. When SONY Cache-1M releases this signal, it is first driven high for one cycle and then tri-stated. This signal is sampled at the same time as the first CBRDY#/ CRDY# of the line fill by the SONY Cache-1M. If it is sampled low, the cache line is write-through (shared).

2.4 Control (output):

ACTIVE	O	This pin indicates if the chip is active or inactive state. It is used for trouble shooting only and should not be used by the system.
CHITM#	O	Cache hit indicator. This signal indicates if a cache access hits a modified cache line in the SONY Cache-1M cache. Specifically, it is asserted in the following cases: 1. During read hit to modified data. 2. During coordinate read cycles. 3. During read miss cycles when cast-out is pending. 4. Two cycles after EADS# if it is a hit to modified data. 5. During snoop write-back cycles generated by the SONY Cache-1M.
ID0, ID1, ID2	O	State output, ID0 = ID1 = 1, ID2 = 0
MTCH1, MTCH2	O	These signals are used for internal testing only and should not be used in the system.
PRSN#	O	Static output, always low.
RDYO#	O	Data ready. It is asserted at the last cycle of a read hit or write hit to write-back lines with BRDYO# to indicate that the burst sequence is completed. It can be connected externally with CRDY# to form an I/O pin. When RDYO# is not asserted, it is driven high for one cycle and then tri-stated.

3 Functional Descriptions

The SONY Cache-1M is a second level cache subsystem designed for 486-class microprocessors. It interfaces directly to the microprocessor in look-aside configuration. It monitors all memory cycles on the host bus to check for cache hit. If it is a hit, the SONY Cache-1M handles the data transfer directly with the CPU, resulting in zero wait transfer. If it is a cache miss and the conditions allow, a line fill will be performed when data returns from the system memory. Data can be stored in the cache as either write-back or write-through data. Snooping is supported to allow an external bus master to access memory data and maintain data consistency.

The SONY Cache-1M stays transparent on the host bus most of the time. It becomes a bus master only to write back modified data. Modified data write-back can be triggered under three conditions: 1) snoop hit on modifed data, 2) cast-out due to incoming line fill, and 3) flush.

The following is a high level block diagram of the look-aside design.

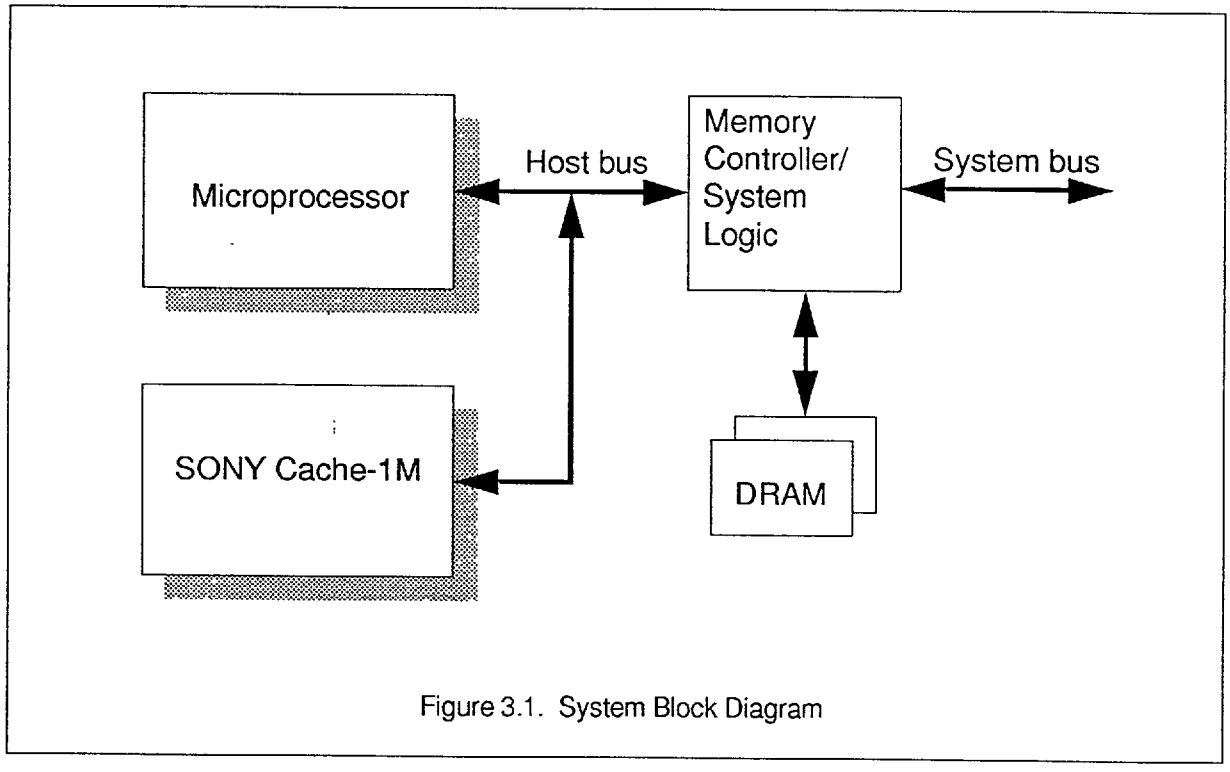
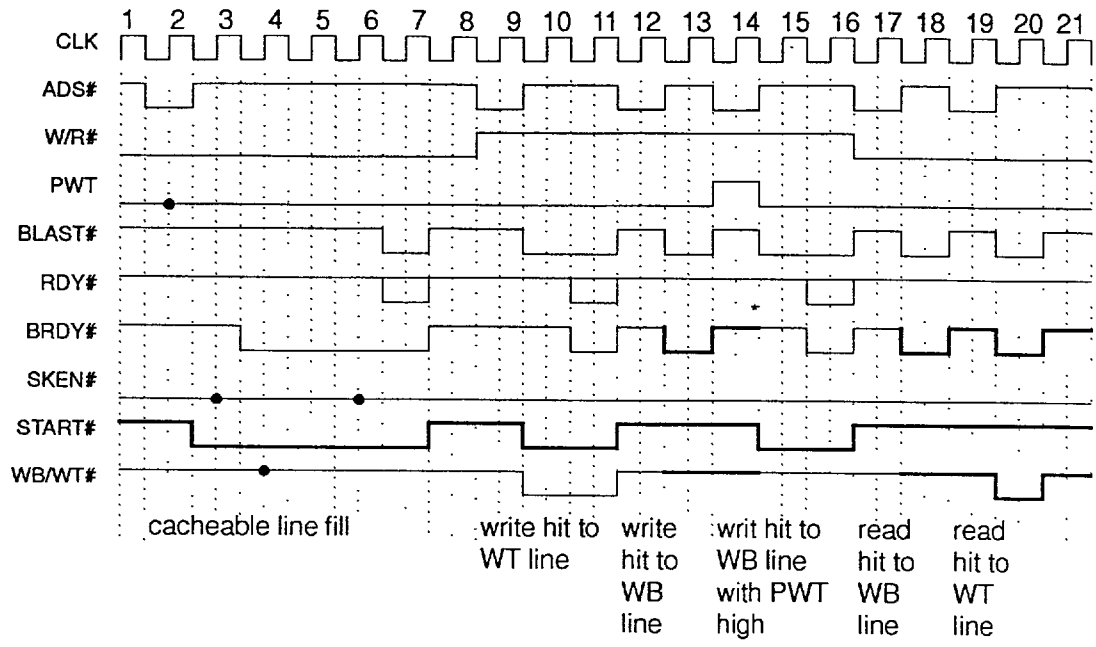


Figure 3.1. System Block Diagram

The following sections describes the cache function in detail.

3.1 Line fill, write hit and read hit



* A thick signal line indicates that the signal is driven by the SONY Cache-1M
* BRDY# and RDY# are connected as shown in section 4.1 and 4.2.

Figure 3.2. Line fill and hit cycles

In the above diagram, a line fill is initiated by the CPU as memory read at cycle 1. The accessed data is not in the SONY Cache-1M so it is a read miss. The SONY Cache-1M samples SKEN# during the cycles between ADS# and the first BRDY# to determine if the line fill is cacheable. If the memory read is cacheable, the SONY Cache-1M monitors BRDY#/RDY# and stores the return data in its internal data ram. The line fill ends when the fourth BRDY#/RDY# is sampled. If the CPU terminates the line fill by asserting BLAST# before reading the last data, the SONY Cache-1M would also abort its line fill. SKEN# is sampled again one cycle before the last BRDY#/RDY# to determine the cacheability of the line fill.

In order for the cache line to be stored as a write-back line, the PWT signals must be low when ADS# is asserted and the WB/WT# signals must be high with the first BRDY#. If either one of these requirement is not met, the line is stored as a write-through line.

When the CPU generates a write cycle, the SONY Cache-1M checks to see if it is a write hit. If it is a write hit to a write through line, as indicated in cycle 9, the SONY Cache-1M asserts START# to activate the system memory. When the system memory returns BRDY# or RDY#, the SONY Cache-1M updates its internal data ram and the cache line remains as write through. The above example shows a write through with one wait state. The SONY Cache-1M can also handle write cycles with any number of wait states including zero wait state. With zero wait state, the BRDY# signal is asserted one cycle earlier than what is shown in the above example.

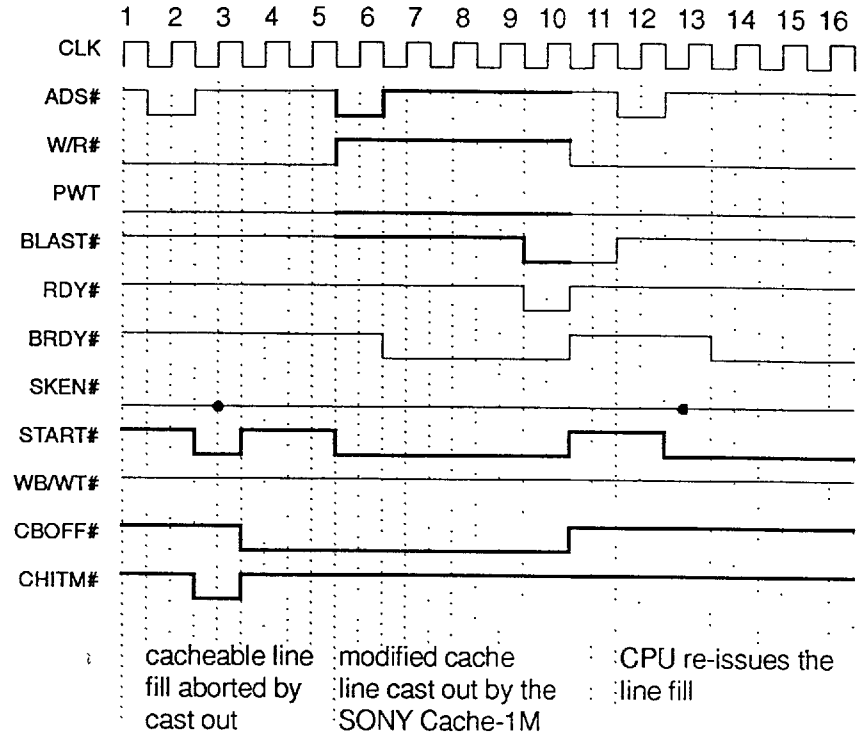
In cycle 12, the write cycle generates a write hit to a write back line. The SONY Cache-1M asserts BRDY# in the following cycle to complete the write

cycle. The BLAST# signal indicates to the SONY Cache-1M that only one doubleword is written by the CPU. If BLAST# is not asserted, the SONY Cache-1M process the write cycle as a burst write and continue to write to the cache line until either four doublewords has been written or BLAST# is asserted, whichever occurs earlier. WB/WT# is driven high by the SONY Cache-1M to indicate a write back hit. Write back hit cycle is always processed by the SONY Cache-1M with zero wait state.

In cycle 14, the write cycle also generates a write hit to a write-back line. But since PWT is driven high by the CPU, the SONY Cache-1M process the write cycle as write through

When the CPU reads from the memory, the SONY Cache-1M looks up the address to determine if it is a read hit. If it is a read hit, as indicated in cycle 17 and cycle 19, the SONY Cache-1M provides the read data, asserts BRDY#, and drives WB/WT# according to the write policy of the cache line. The read cycle is terminated when the CPU asserts BLAST# or after four doublewords has been returned by the SONY Cache-1M, whichever occurs earlier. Read hit cycle is always processed by the SONY Cache-1M with with zero wait state.

3.2 Line fill with cast out due to modified data



* A thick signal line indicates that the signal is driven by the SONY Cache-1M
* BRDY# and RDY# are connected as shown in section 4.1 and 4.2.

Figure 3.3. Line fill with cast out

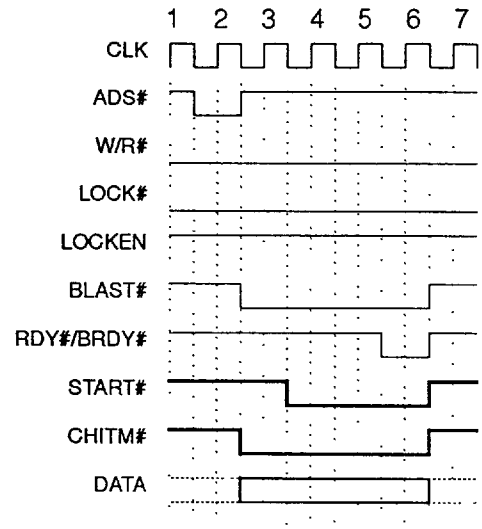
When the CPU starts a cacheable line fill, the SONY Cache-1M writes the new data into its internal data ram. If the same entry in the data ram already contains modified data, the SONY Cache-1M must first cast out the modified line to the system memory before processing the line fill. When this condition is detected, the SONY Cache-1M asserts CBOFF# as soon as cacheability can be determined. In the example shown in figure 3.3, CBOFF# is asserted at cycle 3 after SKEN# is sampled active at the end of cycle 2.

CBOFF# should be connected to the CPU so that it aborts the read cycle and relinquish control of the host bus to the SONY Cache-1M. The SONY Cache-1M asserts ADS# and START# in cycle 6 to start the cast out cycle. It samples BRDY# and RDY# to determine when the write data is accepted by the system memory. BLAST# is asserted when the last doubleword is cast out to the system memory.

Non-burst write-back is also allowed if the system memory asserts RDY# instead of BRDY# to terminate each data transfer. In order to avoid ambiguous burst sequence, the system memory should not switch between burst and non-burst write-back within one cache line.

CBOFF# is de-asserted after the cast out is completed. Upon seeing CBOFF# becomes inactive, the CPU re-issues the memory read. Since the modified cache line is already cast out, the line fill proceeds normally.

3.3 Coordinate read



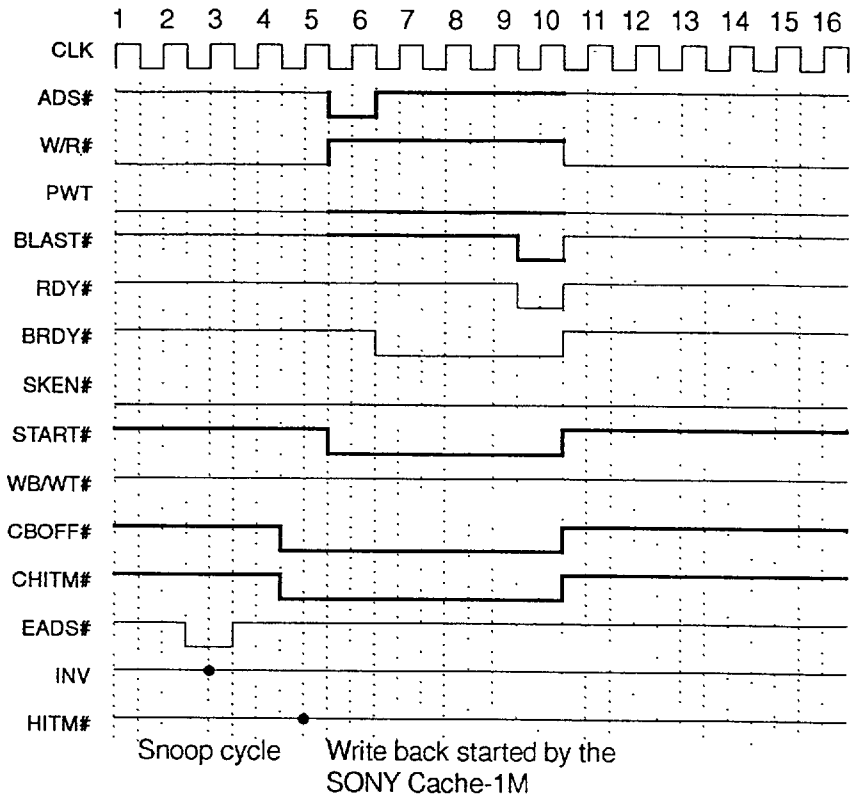
* A thick signal line indicates that the signal is driven by the SONY Cache-1M
* BRDY# and RDY# are connected as shown in section 4.1 and 4.2.

Figure 3.4. Coordinate read

Coordinate read occurs only during locked read hit cycle to modified data with LOCKEN active. The coordinate read cycle should be used with chipsets that are specifically designed for the purpose. When the SONY Cache-1M is used with other chipsets, the LOCKEN pin should be connected to logic zero (inactive) to disable coordinate read. When LOCKEN is inactive, the LOCK# input is ignored.

In coordinate read, since the SONY Cache-1M contains the most up-to-date data, it drives the data output starting at the cycle immediately after ADS#. However, it does not drive the BRDY#/RDY# output as in regular read hit cycles. The BRDY#/RDY# pins are driven by the system logic. When BRDY#/RDY# is asserted with BLAST# active, the cycle is completed.

3.4 EADS cycle



* A thick signal line indicates that the signal is driven by the SONY Cache-1M
* BRDY# and RDY# are connected as shown in section 4.1 and 4.2.

Figure 3.5. EADS cycle

The SONY Cache-1M supports EADS# snoop in back off cycles and in normal cycles when the SONY Cache-1M is not processing a burst operation. Figure 3.5 shows the timing of a snoop cycle. When EADS# is sampled active, the SONY Cache-1M looks up the address to determine if it is a hit and if the cache line contains modified data. If it is a snoop miss, the SONY Cache-1M would not take any action. If it is a snoop hit, the way it is handled is determined by the state of INV pin when EADS# is sampled and by whether the cache line contains modified data.

If the cache line contains modified data, the SONY Cache-1M will write-back the entire cache line to the system memory. The SONY Cache-1M indicates a write-back cycle by asserting both CHITM# and CBOFF# in cycle 4. The SONY Cache-1M samples HITM# at the end of the same cycle. HITM# is driven by the CPU to indicate modified cache line hit in the L1 cache. If it is active, the SONY Cache-1M aborts the write-back immediately because the CPU contains the most updated data of the cache line. The CPU will perform a write-back cycle and keeps HITM# asserted until the write-back is completed. The SONY Cache-1M monitors the write-back cycle like all other ADS# cycles and updates the cache line during the write-back cycle.

If HITM# is sampled inactive, the write-back cycle is continued by the SONY Cache-1M. It becomes the bus master at cycle 5 and asserts ADS# and START# and other control signals to indicate a memory write cycle. All four doubleword of the cache line are written back to the system memory.

CBOFF# and CHITM# are de-asserted when write-back is completed.

Similar to CPU write cycles, the system memory can insert wait states by de-asserting BRDY#/ RDY# during the burst transfer. Non-burst write-back is also allowed if the system memory asserts RDY# instead of BRDY# to terminate each data transfer. In order to avoid ambiguous burst sequence, the system memory should not switch between burst and non-burst write-back within one cache line.

The status of the cache line is updated after the write-back cycle. If INV is active, the cache line is invalidated after the write-back is completed by either the CPU or the SONY Cache-1M. If INV is not active, the cache line is changed to write-through.

EADS# is sampled by the SONY Cache-1M except during the following conditions when EADS# must remain de-asserted:

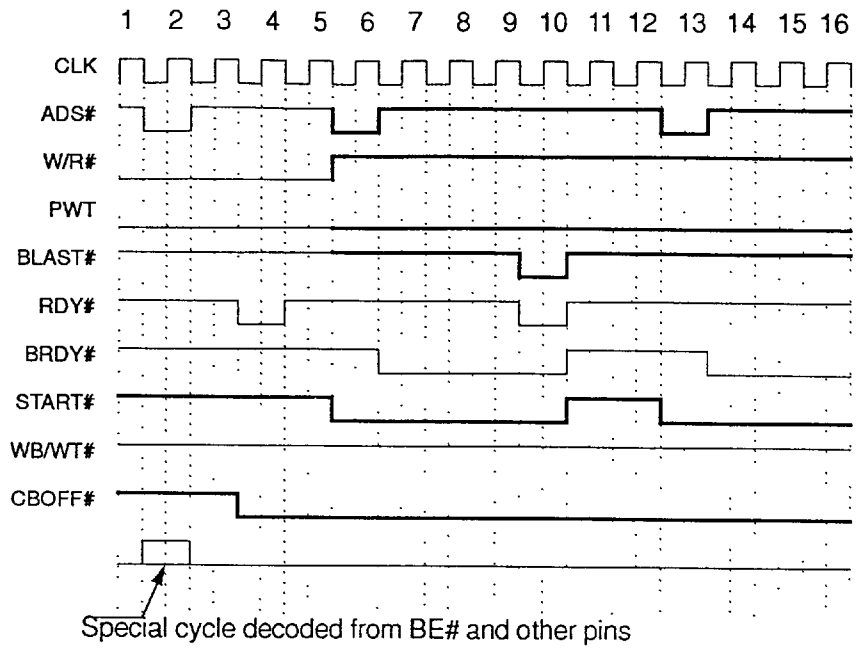
1) Between and during the first and last BRDY# of any burst transfer.
2) One cycle immediately after EADS# is asserted.
3) When there is a write-back in progress or pending in the SONY Cache-1M due to snoop hit or cast-out.
4) During flush sequence unless flush is interrupted by SBOFF#.

3.5 EADS# and ADS# at the same time

Snoop and regular memory access normally does not start at the same cycle. It is considered a special case when both accesses are started at the same cycle by an external master. When EADS# and ADS# are asserted at the same time and the following rules are followed by the SONY Cache-1M.

1. If SBOFF# is asserted, ADS# is always ignored and the snoop cycle is processed.
2. If SBOFF# is not asserted and the ADS# access is for memory read, EADS# is ignored.
3. If SBOFF# is not asserted and the ADS# access is for memory write and it is a write hit to a write-through line, both the ADS# and EADS# cycles are processed in parallel. In other words, if INV is active, the write-hit line is invalidated in parallel to the write operation. If INV is not active, the write hit operation continues while the EADS# operation does not modify the cache status.
4. If SBOFF# is not asserted and the ADS# access is for memory write other than write-through hit, the snoop operation is ignored.

3.6 Software Flush cycle



* A thick signal line indicates that the signal is driven by the SONY Cache-1M
* BRDY# and RDY# are connected as shown in section 4.1 and 4.2.

Figure 3.6. Software FLUSH cycle

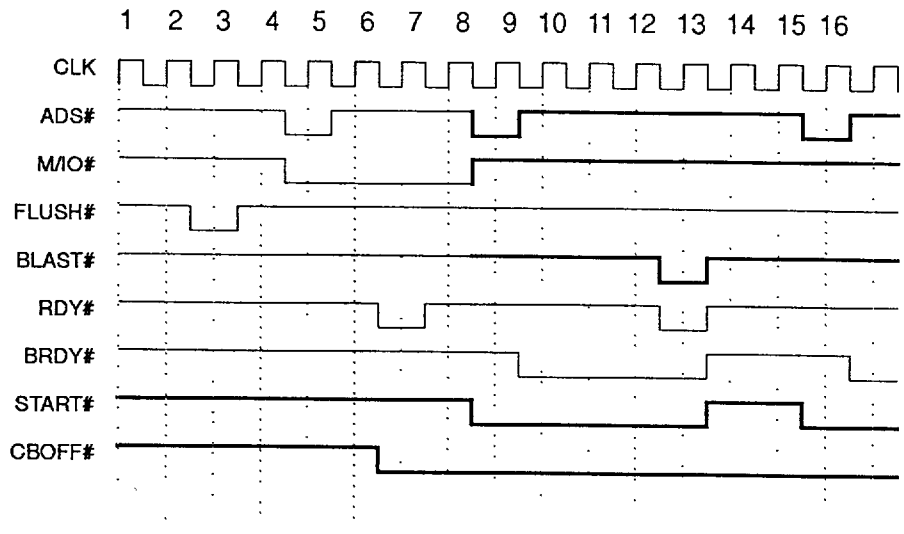
The SONY Cache-1M decodes the flush special bus cycle. The flush special bus cycle is identified by BE#[3:0] = 1101, D/C# = 0, M/IO# = 0, W/R# = 1, and ADDR[2] = 0. The SONY Cache-1M asserts CBOFF# as soon as the flush cycle is detected. It then wait until the system logic returns either the RDY# or BRDY# signals. The SONY Cache-1M then sequences through its internal tag ram looking for modified data. It writes back each modified cache line by initiating a burst write sequence. Each cache line requires two clock cycles to verify and the cache entry is invalidated regardless whether write back is required.

After all the cache lines has been verified or written back, CBOFF# is de-asserted to return to normal state. The SONY Cache-1M does not start the flush write back sequence if it has not created any modified cache line since the last reset or flush, but the internal cache line is always flushed.

When CBOFF# is removed, the CPU re-issues the flush cycle again. Since the cache is now clean, the flush cycle is not backed-off and terminates normally.

3.7 Hardware Flush

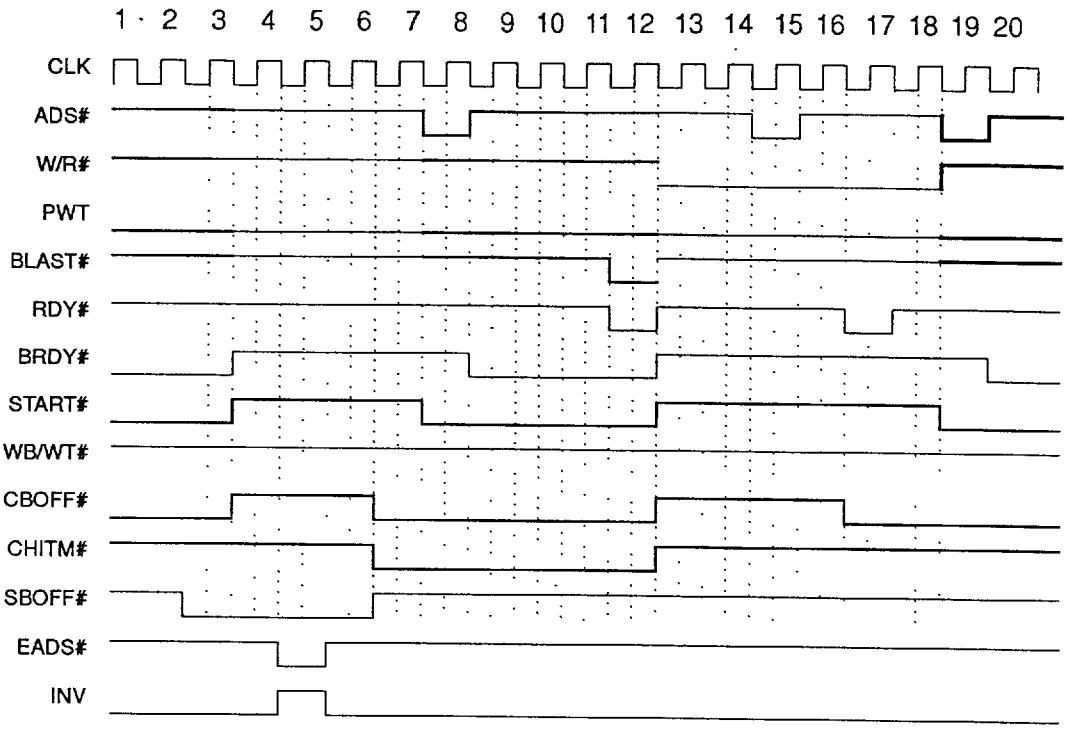
The flush cycle listed in previous section can also be triggered by the hardware FLUSH# input. The falling edge of the FLUSH# input, when sampled by the clock, sets an internal flag in the SONY Cache-1M. Once the internal flag is set, the next I/O access generated by ADS# will trigger the flush write back operation in exactly the same way as a software flush. It is required that the FLUSH# and ADS# signals must be separated by at least two clock cycles. Memory access between the FLUSH# and the I/O access is also allowed.



* A thick signal line indicates that the signal is driven by the SONY Cache-1M
* BRDY# and RDY# are connected as shown in section 4.1 and 4.2.

Figure 3.7. Hardware FLUSH cycle

3.8 Interrupted Flush



* A thick signal line indicates that the signal is driven by the SONY Cache-1M
* BRDY# and RDY# are connected as shown in section 4.1 and 4.2.

Figure 3.8. Interrupted FLUSH cycle

Flush write-back is a very long process since a tag look-up must be performed on each tag entry. The look-up itself takes 8192 clock cycles and write-back of modified data takes additional cycles. The flush write-back sequence can be interrupted by SBOFF# to perform snoop cycles. Other operations are not allowed during flush write-back.

When a snoop operation is needed, SBOFF# must be asserted first to abort the flush write-back cycle. In the above example, SBOFF# is asserted at cycle 2 and the SONY Cache-1M is backed-off immediately. EADS# can then be asserted to start the snoop cycle. If the snoop operation hits modified data in either L1 or L2 cache, the normal snoop write-back sequence is allowed, including snoop write-back started by L1 cache.

In the above example, the snoop hits modified data in the SONY Cache-1M so a snoop write-back sequence is started. When the snoop write-back is completed, both CBOFF# and SBOFF# are de-asserted so the CPU re-started the flush operation because the original flush special cycle or the I/O cycle that triggered the flush operation was backed-off by the SONY Cache-1M. When flush is re-started, the SONY Cache-1M continue the tag look-up from its current location.

3.9 Flush in cascade mode

When two SONY Cache-1M are configurated in cascade mode, the hardware or software flush is detected by both SONY Cache-1M at the same time. If only one chip contains modified data since the last flush, that chip will start the flush sequence while the other one becomes inactive. If both chips contain modified data, the two chips coordinate between themselves through the CASD pins to make sure that only one chip is actually running the flush sequence while the second chip goes into the inactive state.

When the first chip finishes flushing, it de-asserts the CBOFF# signal. The BOFF# input of the CPU is derived from the CBOFF# signal of the SONY Cache-1M (see section 4.6) so the CPU, seeing BOFF# is de-asserted, re-issues the flush cycle again. At this time the second chip will start the flush sequence while the first chip becomes in active.

3.10 Power management

The Sony Cache-1M is designed for low power consumption. Static CMOS design technique is used throughout the memory and control blocks of the chip to minimize power consumption. The system clock can be slowed down to any frequency or even completely stopped to conserve power without suffering data loss. Further more, power consumption is tied directly to the activity level of the system. If memory activity is reduced due to various reasons such as CPU internal cache hit or system halt, the power consumption of the Sony Cache-1M is also reduced automatically, even with the clock running a fully frequency.

As a result of the SONY Cache-1M low power design, systems using this cache chip benefit from the power saving whenever system activity is reduced, regardless of how the system chipset reduce bus activity. No special decode of the stop clock or stop grant bus state is required.

In addition, a special power down mode is also provided to reduce power consumption to the absolute minimum. The following diagram shows the relationship between power consumption are other parameters.

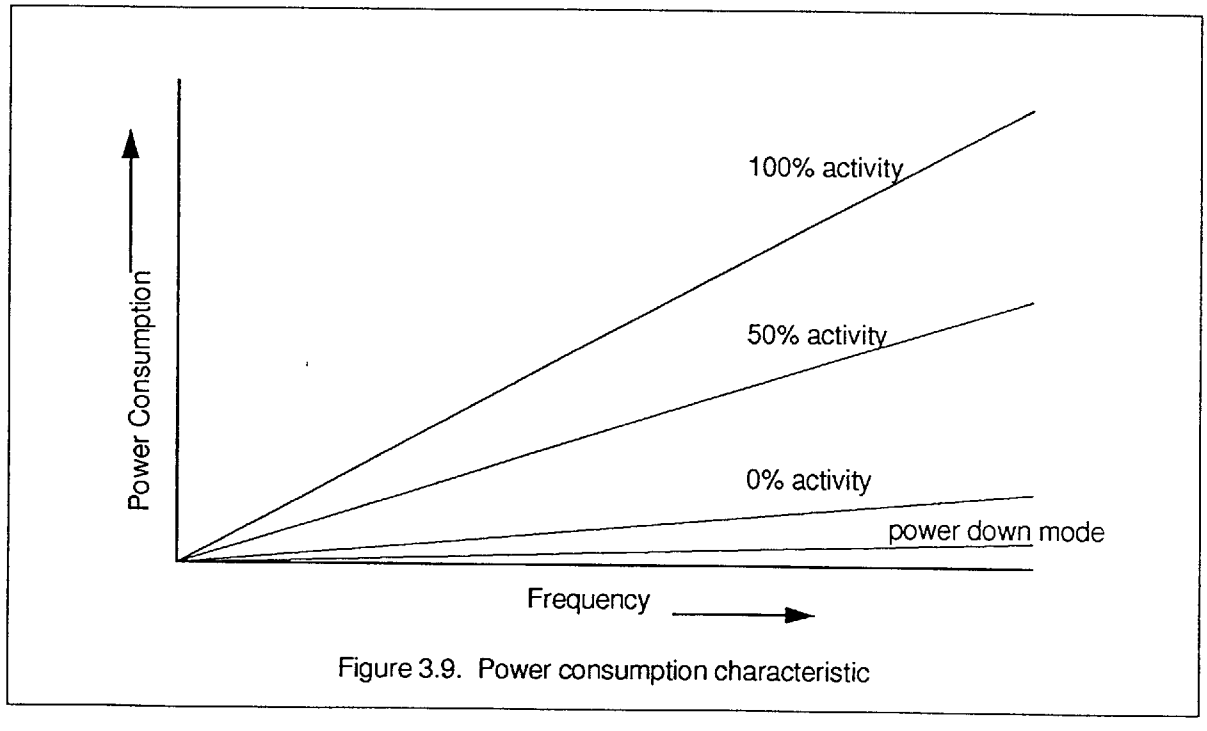


Figure 3.9. Power consumption characteristic

3.11 Power down mode

Power-down mode is designed to reduce power consumption to the absolute minimum. It is controlled by the ENABLE# input signal. During normal operation, ENABLE# must be asserted (low). If ENABLE# is de-asserted, the SONY Cache-1M will enter power down mode in four cycles. During power down, the SONY Cache-1M does not respond to any external inputs, including RESET, but the internal RAM data is preserved. Most of the internal blocks, including the clock buffer, are shut down to conserve power. The SONY Cache-1M returns to normal operation mode two cycles after ENABLE# is re-asserted.

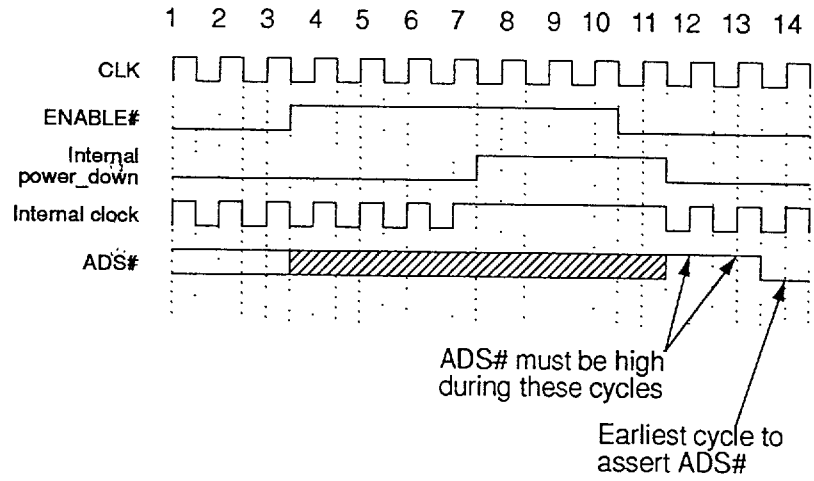


Figure 3.10. Power-down Timing

3.12 Reset and idle states

The following table lists the states of all I/O and output pins during reset, idle and power_down. The chip enters reset state one cycle after RESET pin is asserted. It enters power_down state four cycles after ENABLE# is de-asserted. Idle state is defined as the cycles when there is no active memory or snoop cycles on the bus.

Pin Name	Type	Reset / Idle / Power down	Notes
ACTIVE	O	--	1
ADDR[31:2]	I/O	high Z	
ADS#	I/O	high Z	
BE#[3:0]	I/O	high Z	
BLAST#	I/O	high Z	
BRDYO#	I/O	high Z	
CASD[2:0]	I/O	--	2
CHITM#	I/O	1	
D/C#	I/O	high Z	
DATA[31:0]	I/O	high Z	
DP[3:0]	I/O	high Z	

Pin Name	Type	Reset / Idle / Power down	Notes
M/IO#	I/O	high Z	
MTCH1/2	O	--	3
PCD	I/O	high Z	
PRSN#	O	0	
PWT	I/O	high Z	
RDYO#	O	high Z	
START#	I/O	1	
W/R#	I/O	high Z	
WB/WT#	I/O	high Z	
CBOFF#	I/O	1	

Notes

1. Equals zero only in cascade mode after the chip has been de-selected by a previous instruction. Otherwise equals one. This pin is used for internal testing and should not be used by any external device.
2. CASD signals varies between zero, one or high Z depends on the internal state of the cache and whether cascade mode is asserted. These pins should be used between the SONY Cache chips during cascade mode and should not be sampled by any external device.
3. MTCH1/2 varies between zero or one depends on reset or power_down mode. These signals should not be used by any external device.

4 I/O Signals Generation

This section describes most of the control signals in typical system configurations.

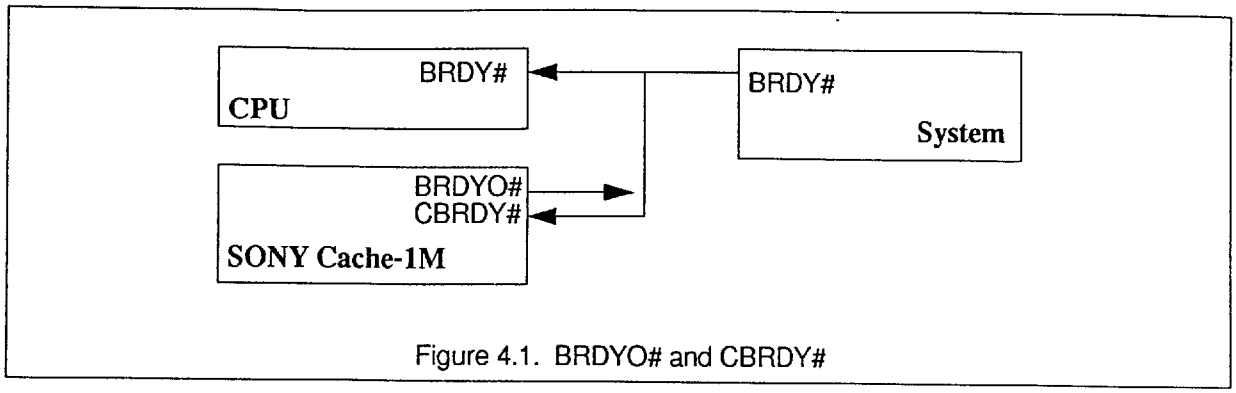


Figure 4.1. BRDYO# and CBRDY#

4.1 CBRDY# and BRYO#

The CBRDY# and BRDYO# pins of the SONY Cache-1M should be connected together externally to form an I/O pin. This pair of I/O pin should be wired-OR with the BRDY# pin driven by the system memory. The BRDYO# output of the SONY Cache-1M is normally tri-stated. During read hit and write hit to write back lines, the SONY Cache-1M drives this signal low to indicate a hit cycle. At the end of the hit cycle, this signal is driven high for one cycle and then tri-stated. The system logic should tri-state its BRDY# output when it is driven by the SONY Cache-1M cycles. In read miss and write-through cycles, the SONY Cache-1M samples CBRDY# at the same time as the CPU samples BRDY#.

4.2 CRDY# and RDYO#

The CRDY# and RDYO# pins of the SONY Cache-1M should be connected together externally to form an I/O pin in the same way CBRDY# and BRDYO# are connected together. These signals are used to indicate non-burst ready for external access cycles.

4.3 START#

START# is used by the SONY Cache-1M to signal any cycle that requires services from the system memory. These cycles are read miss, write miss and write through cycles. The system memory controller can monitor this signal instead of the ADS# signal from the CPU to activate the system memory. The system logic should still monitor the ADS# signal from the CPU to detect I/O cycles.

4.4 SKEN#

The signal is driven by the system logic and sampled by both the CPU and the SONY Cache-1M to determine cacheability of any read data. The system logic should drive this signal low during read hit cycles so that read hit in the SONY Cache-1M become cacheable in the CPU's internal cache.

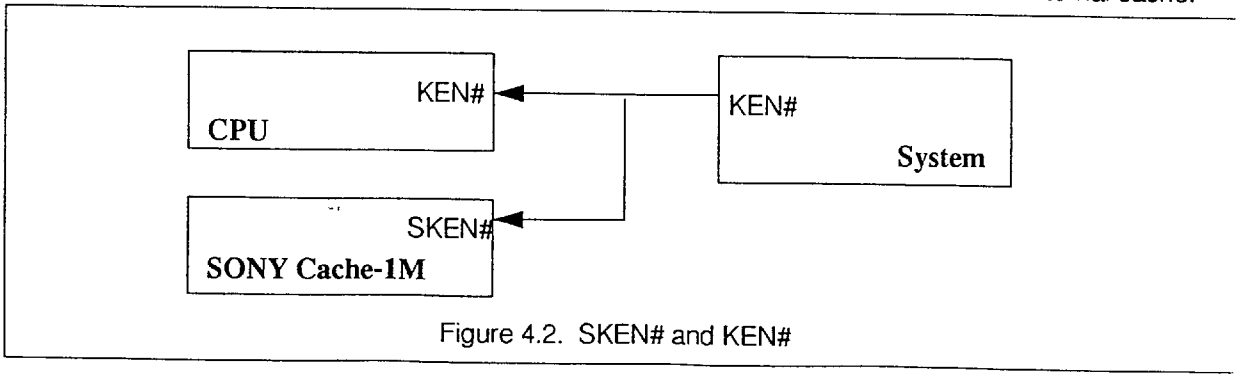


Figure 4.2. SKEN# and KEN#

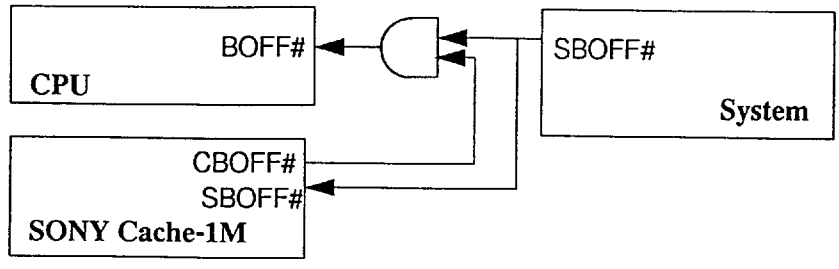


Figure 4.3. SBOFF# and CBOFF#

4.5 CS#

The Chip Select signal should be tied low (active) during normal operation. If CS# is driven high, the SONY Cache-1M does not responds to any memory access or snoop cycle.

4.6 CBOFF and SBOFF#

CBOFF# is driven by the SONY Cache-1M when it needs to control the host bus to write-back a cache line. Write-back is required when a snoop or flush cycle hits a modified cache line or data eviction is needed before a line fill. If the system logic also needs to back-off the CPU, it should drives the SBOFF# input to indicate to the SONY Cache-1M that the CPU is back-off. The CBOFF# and SBOFF# signals should be combined together externally to form the BOFF# input to the CPU.

4.7 HITM#

This is an input signal designed to used with CPU that contains internal write-back cache. Since the 486 has write-through internal cache, this signal should be tied high at all time.

4.8 CHITM#

The CHITM# signal is driven active by the SONY Cache-1M to indicate that a snoop cycle hits a modified cache line. It should be sampled by the system logic two cycles after EADS# is asserted.

4.9 INV

The INV input controls the type of snoop cycle to be performed. It is sampled at the same time as EADS#. If it is active (high) and the snoop cycle is hit, the cache line will be invalidated. If INV is low, the snooped cache line will be changed to write-through. Regardless of INV, the snooped cache line is always written-back to the system memory if it contains modified data.

4.10 MODE[4:0]

The mode pins are used to select between 486 burst and linear burst mode and to select between cascade or stand-alone mode.

486 Burst sequence: MODE[4] = 0
Linear Burst sequence: MODE[4] = 1

The cascade mode allows two SONY Cache-1M chips to work together to provide 256K bytes of cache memory. Stand-alone mode requires only one SONY Cache-1M chip and it provides 128K bytes of cache memory. In cascade mode, the mode pins of one of the SONY Cache-1M chip should be set to

MODE[3:0] = 1100

while the second SONY Cache-1M chip should have the mode pins set to

MODE[3:0] = 1101

In stand-alone mode, the mode pins should be set to

MODE[3:0] = 0000

All other combinations are reserved.

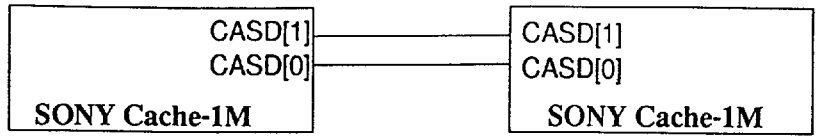


Figure 4.4. CASD signals

4.11 CASD[1:0]

The CASD pins are used for communication between the SONY Cache-1M chips during cascade mode. They should be connected together as shown in Figure 4.4. When the SONY Cache-1M is operating in stand-alone mode, the CASD[1:0] pins should be left unconnected.

4.12 Signals in Cascade Mode

When two SONY Cache-1M chips connected together in Cascade Mode to form a 256K cache subsystem, most of the pins are connected in parallel to both SONY Cache-1M chips. From the system hardware's point of view, the two chip subsystem has the same interface as a single SONY Cache-1M chip. The MODE pins connected to both SONY Cache-1M chip should indicate Cascade Mode and one of the chip is designated as chip1 while the other is designated as chip0. The static output and the debug outputs, PRSN#, CASD[2] and ACTIVE, should not be connected. The CASD[1] and CASD[0] pins should be connected between the SONY Cache-1M chips. These pins are used for inter-chip communication and are not used by the system logic.

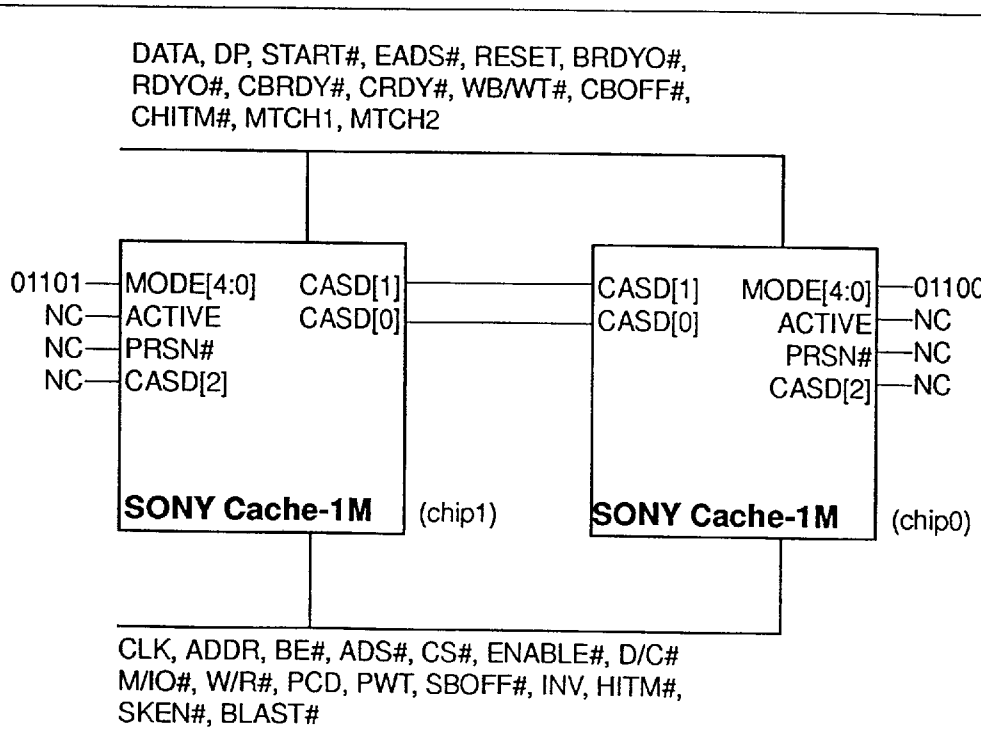


Figure 4.5. Two SONY Cache-1M chips connected in Cascade Mode

5 Electrical Characteristics

5.1 Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.5 to +4.6	V
Input Voltage	VIN	-0.5 to Vcc+0.5	V
Junction (Operating) Temperature	TJ	0 to +125	°C
Ambient (Operating) Temperature	TOPR	0 to +70	°C
Storage Temperature	TSTG	-65 to +150	°C

5.2 D.C. Characteristics

Item	Symbol	Min	Max	Unit
Supply Voltage	Vcc	3.135	3.465	V
Input low voltage	VIL	-0.3	+0.8	V
Input high voltage	VIH	2.0	Vcc + 0.3	V
Output low voltage @4.5mA	VOL		0.4	V
Output high voltage @-1.0mA	VOH	2.4		V
Input leakage current	ILI	-1	1	µA
Output leakage current	ILO	-1	1	µA
Supply current	See Section 5.3			
Power down current	I_{ccpd}		2	mA
Capacitance: CQFP	C_{in}			
Clock pin			6	pF
Other input pins			6	pF
Output pins			6	pF
I/O pins			6	pF

5.3 Power Consumption

Power Consumption of the SONY Cache-1M is characterized in terms of internal power and external (I/O buffer) power. Internal power is consumed by the SONY Cache-1M internal core, input buffer, and the input section of any I/O buffer. External power is dissipated by the intrinsic pin capacitance and the external output capacitance loading and is drawn through the last stage of the output buffer. Internal power is supplied through the VCCI pins while external power is supplied through the VCCO pins.

Internal power consumption table

Parameter	Activity Level	Internal Power Consumption at Different Frequencies				
		40Mhz	33Mhz	8Mhz	4Mhz	0Mhz
P_1	100%	680mW	560mW	140mW	70mW	6mW
P_2	50%	370mW	305mW	75mW	40mW	6mW
P_3	0% (idle)	50mW	40mW	15mW	10mW	6mW
P_{pd}	Power down mode	6mW	6mW	6mW	6mW	6mW

Internal power consumption is highly dependent on operating frequency and activity level of the SONY Cache-1M. Operating frequency is the frequency of the clock input pin. Activity level is defined as the worst case of any read, write, write-back or snoop cycles. 100% active level implies that the SONY Cache-1M is constantly running the worst case power consumption cycle even though the device may not be subjected to such operation cycles in actual application. 50% active level implies that on the average the SONY Cache-1M is running the worst cycle half of the time (clock cycle) and idle for the rest of the time.

I/O buffer power consumption table

Output Capacitance (including C_{in})	External Power Consumption at Different Frequencies				
	40Mhz	33Mhz	8Mhz	4Mhz	0Mhz
30pF	275mW	225mW	54mW	27mW	0mW
20pF	182mW	150mW	36mW	18mW	0mW

I/O buffer power consumption is measured at continuous burst read hit with half of the data output change state each burst cycle.

5.4 A.C. Characteristics

Symbol	Parameter	40MHz		33MHz		Fig
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	
t_1	CLK Period	25		30		5.1
t_2	CLK High Time	8		11		5.1
t_3	CLK Low Time	8		11		5.1
t_4	CLK Fall Time		3		3	5.1
t_5	CLK Rise Time		3		3	5.1
t_{6a}	ADDR, BE0#-BE3# Setup	6		6		5.2
t_{6b}	ADDR, BE0#-BE3# Hold	2		2		5.2
t_{7a}	ADS#, M/IO#, W/R#, D/C#, PCD, PWT, LOCK# LOCKEN Setup	8		10		5.2
t_{7b}	ADS#, M/IO#, W/R#, D/C#, PCD, PWT, LOCK#, LOCKEN Hold	2		2		5.2
t_{8a}	RESET Setup	6		6		5.2
t_{8b}	RESET Hold	2		2		5.2
t_{9a}	BLAST# Setup	7		7		5.2
t_{9b}	BLAST# Hold	2		2		5.2
t_{10a}	CRDY#, CBRDY# Setup	5.5		5.5		5.2
t_{10b}	CRDY#, CBRDY# Hold	2		2		5.2
t_{11a}	SKEN#, INV Setup	5		5		5.2
t_{11b}	SKEN#, INV Hold	2		2		5.2
t_{12a}	DATA, DP0-DP3 Setup	5		5		5.2
t_{12b}	DATA, DP0-DP3 Hold	2		2		5.2
t_{13a}	WB/WT# Setup	5		5		5.2
t_{13b}	WB/WT# Hold	2		2		5.2
t_{14a}	SBOFF# ENABLE# Setup	7		7		5.2
t_{14b}	SBOFF#, ENABLE# Hold	2		2		5.2
t_{15a}	EADS#, FLUSH# Setup	5		5		5.2
t_{15b}	EADS#, FLUSH# Hold	2		2		5.2
t_{16a}	HITM# setup	7		8		5.2

Symbol	Parameter	40MHz		33MHz		Fig
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	
t_{16b}	HITM# Hold	2		2		5.2
t_{17a}	CS# Setup	7		7		5.2
t_{17b}	CS# Hold	2		2		5.2
t_{19a}	ADDR, BE# Valid delay	3	14	3	16	5.3,5.4
t_{19b}	ADDR, BE# Float delay	3	18	3	20	5.5
t_{20a}	ADS#, M/IO#, W/R#, D/C#, PCD, PWT Valid delay	3	14	3	16	5.3,5.4
t_{20b}	ADS#, M/IO#, W/R#, D/C#, PCD, PWT Float delay	3	18	3	20	5.5
t_{21a}	LOCK# Valid delay	3	14	3	16	5.3,5.4
t_{21b}	LOCK# Float delay	3	18	3	20	5.5
t_{22a}	BLAST# Valid delay	3	16	3	16	5.3,5.4
t_{22b}	BLAST# Float delay	3	20	3	20	5.5
t_{23a}	BRDYO#, RDYO# Valid delay	3	16	3	16	5.3,5.4
t_{23b}	BRDYO#, RDYO# Float delay	3	20	3	20	5.5
t_{24a}	DATA, DP Valid delay	3	16	3	18	5.3,5.4
t_{24b}	DATA, DP Float delay	3	20	3	22	5.5
t_{25}	CBOFF# Valid delay	3	15	3	18	5.3,5.4
t_{27}	START# Valid delay	3	14	3	16	5.3,5.4
t_{28}	CHITM# Valid delay	3	16	3	18	5.3,5.4
t_{29a}	WB/WT# Valid delay	3	16	3	18	5.3,5.4
t_{29b}	WB/WT# Float delay	3	20	3	22	5.5
t_{30}	ACTIVE Valid delay	3	25	3	33	5.3,5.4
t_{31}	MTCH1, MTCH2 Valid delay	3	25	3	33	5.3,5.4
t_{32}	CASD[1:0] Valid delay	3	17	3	21	5.3,5.4
t_{33a}	CASD[1:0] setup	6		7		5.2
t_{33b}	CASD[1:0] hold	2		2		5.2

* For all AC characteristics, VIL to VIH is 0V to 3V. Input and Output references are at 1.5V, except

float delay

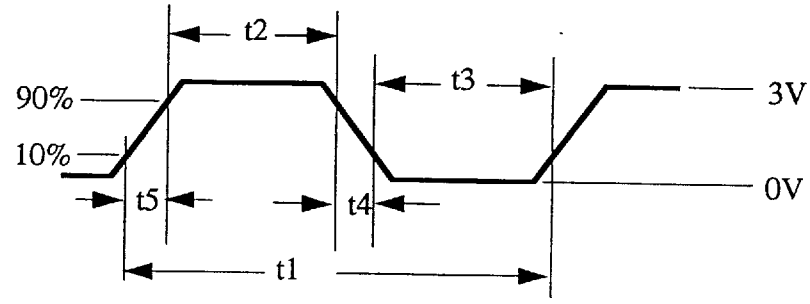
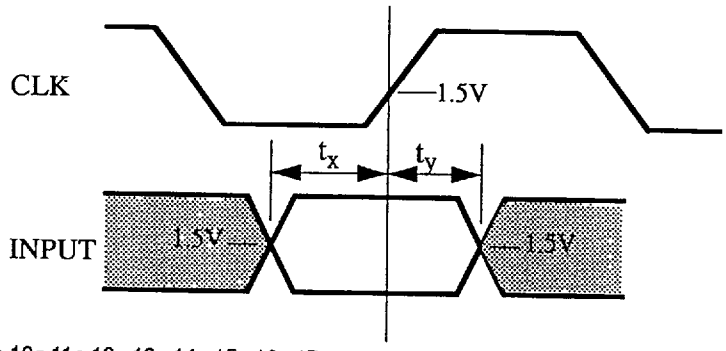


Figure 5.1. Clk Waveform



$t_x = t_{6a,7a,8a,9a,10a,11a,12a,13a,14a,15a,16a,17a}$
$t_y = t_{6b7b,8b,9b,10b,11b,12b,13b,14b,15b,16b,17b}$

Figure 5.2. Setup and Hold Timings

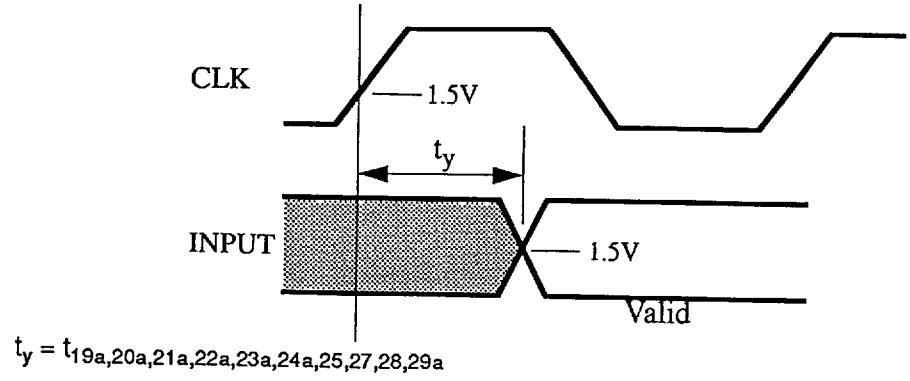


Figure 5.3. Valid Delay Timings

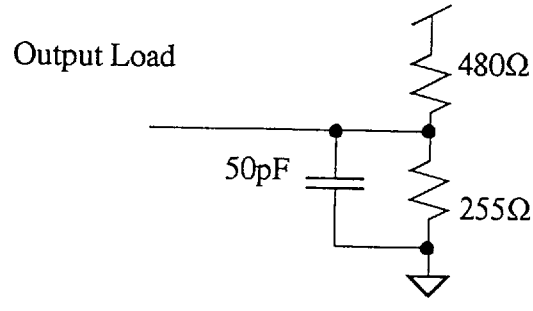
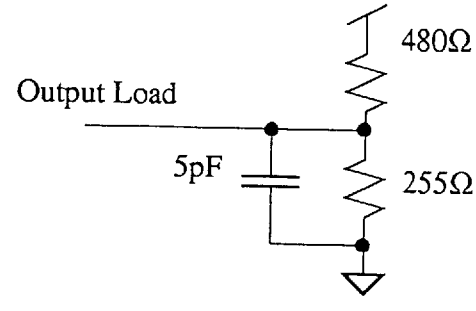


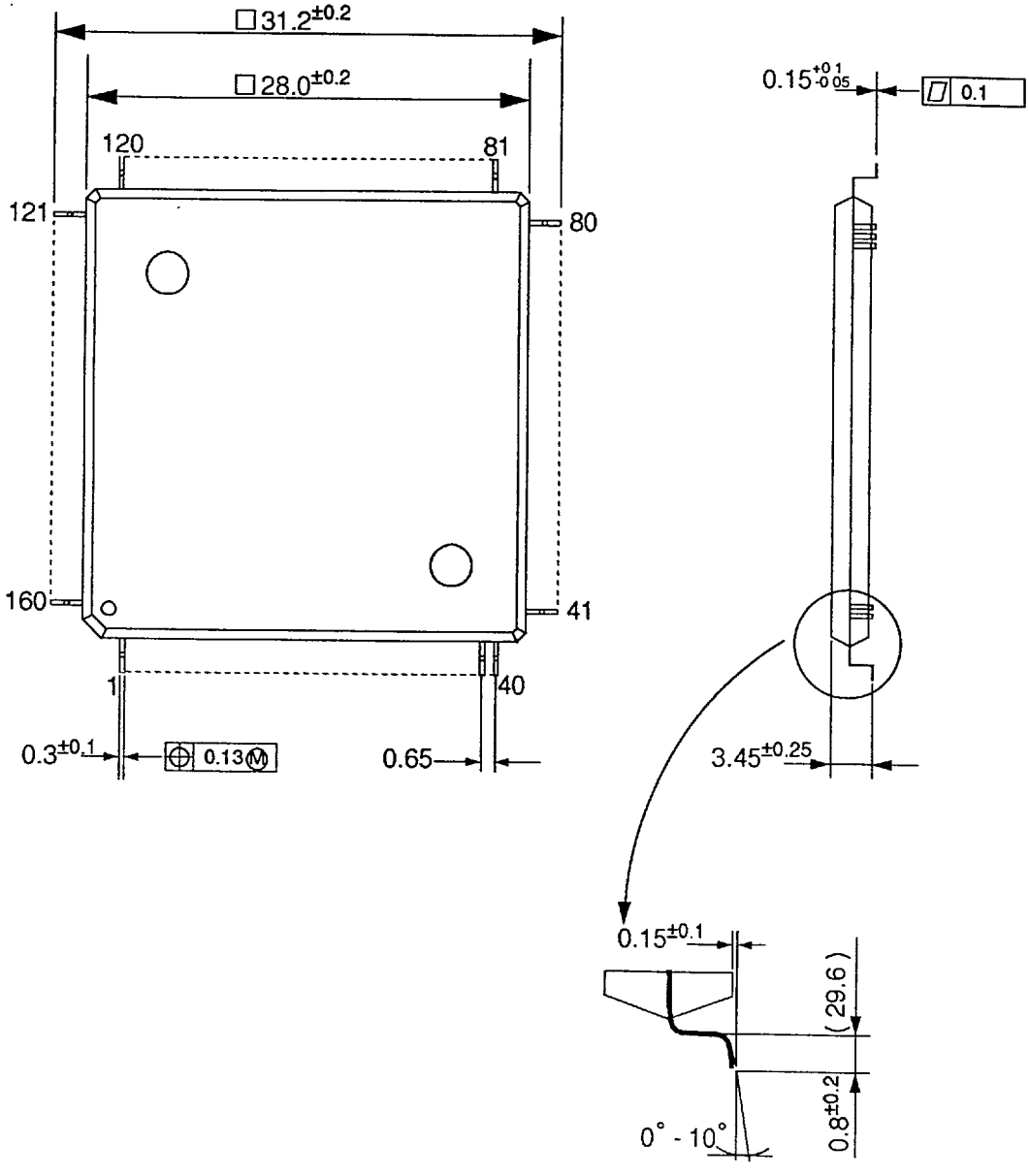
Figure 5.4. Output Load for Valid Delay



- Transition is measured ±200mV from steady voltage with specified loading
- Float delay is not tested.

Figure 5.5. Output Load for Float Delay

6 Mechanical Specification



SONY NAME	QFP-160P-L01
EIAJ NAME	*QFP160-P-2828-A
JEDEC CODE	