AN 8.9

LAN91C96 Motorola 68000 Bus Mode

1 Introduction

The LAN91C96 is the most recent device in the LAN9000 family of fully integrated 10BaseT Ethernet controllers targeted for PC, mobile and embedded networking applications. Because of the LAN9000 family's broad use in embedded applications, the LAN91C96 implements a subset of the Motorola 68000 interface, allowing bus connections to Motorola 68000 family processors which also sees popular success in embedded applications. This application note provides details of the LAN91C96 Motorola 68000 interface, targeting developers with an understanding of ISA or Motorola 68000 bus interfaces. The application note begins with an overview of the LAN91C96 Ethernet controller followed by Motorola 68000 bus limitations of the LAN91C96. Pin functionality differences between ISA and Motorola 68000 bus modes are consolidated into easily read tables for quick reference. Configurations with popular Motorola 68000 processors provide a means of easy application integration. Finally, known LAN91C96 Motorola 68000 interface anomalies are detailed.

2 LAN91C96 Features

The LAN91C96 is an Ethernet controller implementing all MAC and physical layer functions required for 10BASE-T operation. By combining ISA, PCMCIA and Motorola 680000 bus interfaces, the LAN91C96 provides a cross platform solution with a flexible on board RAM and a flat memory structure. Advanced power management features and Magic Packet™ conserve power, while an AUI interface expands physical media compatibility through the use of external 10BASE5, 10BASE2, and 10BASE-F transceivers. The LAN91C96 is pin and software compatible with the LAN91C94 and LAN91C92 allowing an easy upgrade path for earlier generation applications. Full duplex operation maximizes network performance. With serial EEPROM and ROM or Flash ROM interfaces, the LAN91C96 provides jumper less setup for ISA, PCMCIA or Motorola 68000 buses.

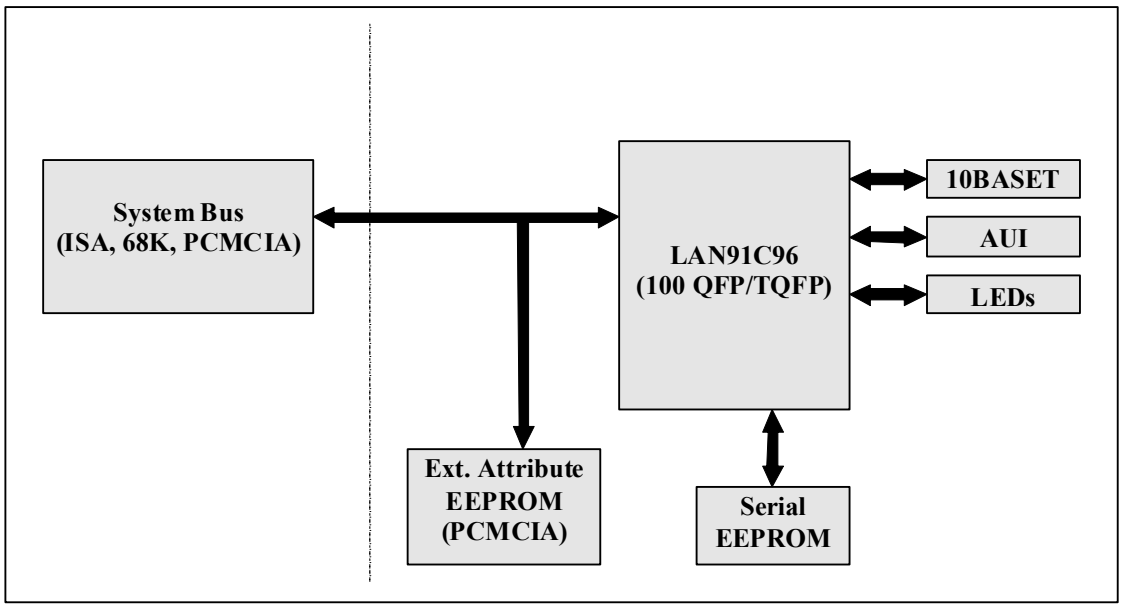


Figure 2.1 LAN91C96 SYSTEM BLOCK DIAGRAM

2.1 Motorola 68000 Bus Mode on the LAN91C96

When Motorola 68000 mode is entered (refer to section titled “Motorola 68000 Bus Mode Entry / Exit Sequence” for mode entry requirements), the functions of key ISA bus pins are replaced with Motorola 68000 signal functions. However, the LAN91C96 incorporates only a subset of the Motorola 68000 bus interface. The following limitations exist in Motorola 68000 bus mode:

Address Bus

The Motorola 68000 family of processors supports up to 16MB of byte addressable space. The LAN91C96 can only support word addressing in Motorola 68000 mode. For this reason, the A[0] pin should be tied low to limit all data accesses to 16-bit words. Additionally, the LAN91C96 uses only address lines A[15:0] for decode into the register space, limiting the device to the lower 32KB of addressable space.

Asynchronous Bus Control

The 16-bit processors in the Motorola 68000 family of processors implement the Lower Data Strobe (nLDS) and Upper Data Strobe (nUDS) signals. The LAN91C96 implements only one input, xDS, to replace these signals. Because the LAN91C96 bus interface is limited to 16-bit accesses, the signal xDS should be connected to nLDS on 16-bit processors. The LAN91C96 will not work with 8-bit processors such as the MC68008.

Data Bus

The LAN91C96 does not swap the low and high bytes of the data bus in Motorola 68000 mode. It is the responsibility of the user to wire the pins as needed (Little Endian or Big Endian ordering).

Bus Arbitration Control

Motorola 68000 family processors support bus arbitration for master and slave devices. Bus arbitration is not supported with the LAN91C96. As a result, the LAN91C96 should be implemented as a slave device. If no other devices exist in the system, the Motorola 68000 Bus Arbitration signals must be dealt with accordingly through the use of 10K pull-ups on nBR and nBGACK.

Interrupt Control

Interrupt control on a Motorola 68000 processor uses an encoded bit scheme. The LAN91C96 does not directly support and encoded interrupt scheme. Instead, a single interrupt pin is provided (INTR) that can be connected to any one of the available Motorola 68000 interrupt lines (IPL[2:0]) The remaining two interrupt lines should be encoded to zero through 10K pull-downs. When INTR is low, the Motorola 68000 will view the value on IPL[2:0] as no interrupt. When INTR is high, the Motorola 68000 will view the value on IPL[2:0] as an encoded interrupt where 7 is the highest priority.

System Reset

The Motorola 68000 family of processors defines reset as an active low state. The LAN91C96 defines reset as an active high state. In order to correctly wire the reset circuit, the reset signal from the Motorola 68000 processor must first be inverted.

2.2 ISA and Motorola 68000 Bus Mode Differences

The LAN91C96 supports asynchronous bus operation in ISA and Motorola 68000 bus. When the LAN91C96 is configured for ISA or Motorola 68000 bus mode, pin signal definitions change. Table 1 below details pin function differences between the two modes.

Table 2.1 Bus Interface Signal Cross Reference

ISA BUS MODE		MOTOROLA 68000 BUS MODE	
SIGNAL	**DESCRIPTION**	**SIGNAL**	**DESCRIPTION**
A[19:1] *Input*	**Address Bus**	**A[19:1]** *Input*	**Address Bus**
A[0] *Input*	**Address Bus Low Bit**	*Not Used*	*Pull-down pin*
D[15:0] *Input / Output*	**Data Bus**	**D[15:0]** *Input / Output*	**Data Bus**
AEN *Input*	**Address Enable** Signifies a valid address is on the address bus	**nAS** *Input*	**Address Strobe** Signifies a valid address on the address bus
nIORD *Input*	**IO Space Read** Signifies cycle is a IO Read Cycle	**xDS** *Input*	**Data Strobe** Signifies valid data on data bus
nIOWR *Input*	**IO Space Write** Signifies cycle is a IO Write Cycle	**R/nW** *Input*	**Read / Write** Signifies a read cycle if high or a write cycle if low
nSBHE *Input*	**Byte High Enable** Low value indicates valid data on the upper data byte	*Not Used*	*Pull-down pin*
nMEMR *Input*	**External ROM Memory Read** Signifies cycle is a ROM Memory Read	*Not Used*	*Float pin*
BALE *Input*	**Input Address Strobe** Falling edge latches address and nSBHE	*Not Used*	*Pull-up pin*
IOCHRDY *Output*	**IO Channel Ready** Optionally used to extend host cycles if wait states required	*Not Used*	*Float pin*
nIOCS16 *Output*	**IO Chip Select** Asserted when A[15:4] decoded to the value in the Base Address Register	*Not Used*	*Float pin*
RESET *Input*	**Chip Reset** Active high	**RESET** *Input*	**Chip Reset** Active low
INTR0 *Output*	**Interrupt 0** Single line interrupt	**INT** *Output*	**Interrupt** Unencoded interrupt tied to IPL0, IPL1 or IPL2
INTR1 *Output*	**Interrupt 1** Single line interrupt	*Not Used*	*Float pin*
INTR2 *Output*	**Interrupt 2** Single line interrupt	**nDTACK/0** *Output*	**Data Transfer Acknowledge** Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated.
INTR3 *Output*	**Interrupt 3** Single line interrupt	**nDTACK/1** *Output*	**Data Transfer Acknowledge** Indicates data transfer complete. If processor is reading data is latched. If processor is writing, bus cycle is terminated.

It is important to note that all other LAN91C96 signals retain the same function in all bus modes. Some of these signals can effect operation of the controller in Motorola 68000 bus mode and must be correctly wired. Table 2 details signals that have uses in ISA bus mode, but will negatively impact operation when configured for the Motorola 68000 bus mode.

Table 2.2 Noteworthy Controller Signals In Motorola 68000 Bus Mode

SIGNAL	ISA BUS MODE USE	WIRING FOR MOTOROLA 68000 BUS MODE
nEN16 *Input*	When low, the LAN91C96 is performs 16-bit operations. When high, the LAN91C96 is performs for 8-bit operations.	*Provide 10K Pull-down*
nROM *Input / Output*	If this pin is sampled low at the end of RESET the bus interface is configured in PCMCIA mode. In ISA mode, the pin is used as a ROM chip select output.	*Float pin*
nDTACK/0 and nDTACK/1 *Output*	These pins represent interrupts. When not selected through the INTSEL0 and INTSEL1 bits these pins are tri-stated.	*Provide 10K pull-ups*

2.3 MOTOROLA 68000 BUS MODE ENTRY / EXIT SEQUENCE

Entering Motorola 68000 bus mode requires a specific sequence. Once entered, only a hard reset will take the part out of Motorola 68000 bus mode.

2.3.1 Bus Mode Entry

1. **Power device up in ISA 16-Bit Bus Mode**. To configure the LAN91C96 up in ISA 16-Bit Bus Mode, nEN16 must be low and nROM must float when samples at the end of reset (RESET signal's falling edge). Table 2 details the pin configuration necessary to accomplish this.
2. **Assert nIORD and nIOWR simultaneously**. After reset, assert nIORD and nIOWR (both driven low) simultaneously to configure the device in Motorola 68000 Bus Mode. Executing a Motorola 68000 bus write sequence is an easy way to accomplish this.
3. **Write to the LAN91C96 using a Motorola 68000 bus write cycle**. The first access to the device after assertion of nIORD and nIOWR must be a Motorola 68000 write cycle. This allows the device to verify the bus mode. Executing a second Motorola 68000 bus write sequence will accomplish this.

2.3.2 Bus Mode Exit

1. **Assert RESET**. Pulling RESET low will reset the device and allow reconfiguration of the bus operating mode.

2.4 MOTOROLA 68000 BUS MODE SOFTWARE CONSIDERATIONS

When configured in Motorola 68000 bus mode, use of the device is the same as in ISA mode, that is all features of the LAN91C96 remain active. Although the ability to access all registers remains, functions related to the system bus must be carefully handled. The following functions need to be considered whenever accessing the device:

PCMCIA Register Functions

The Ethernet Configuration Option Register (8000h) and Ethernet Configuration and Status Register (8002h) are reserved for PCMCIA functions. These registers should be left in the reset state and not changed when operating in Motorola 68000 bus mode.

16-Bit Data Accesses

The Configuration Register 16BIT bit (Bank 1, Offset 0, Bit 7) controls the data bus width. Out-of-reset this bit will reflect the inverted value on the nEN16 pin. When correctly configured for Motorola 68000 bus mode, the bit will read as a high, reflecting a pull-down on the nEN16 bit. This bit should only be written with a high value.

Wait States

The Configuration Register NOWAIT bit (Bank 1, Offset 0, Bit 12) controls whether or not the LAN91C96 will request ISA bus wait states. The default value of zero will negate the IOCHRDY signal for two or three 20MHz clocks on any cycle to the LAN91C96. Writing a one to this bit will prevent the LAN91C96 from requesting wait states. Because the IOCHRDY is not used in Motorola 68000 bus mode, this bit can be ignored.

Interrupts

The Configuration Register INTSEL1 and INTSEL0 bits (Bank 1, Offset 0, Bits 2 and 1) define which interrupt pin (INTR0, INTR1, INTR2 or INTR3) to use when requesting service. Because only INTR0 is used for Motorola 68000 bus mode, these bits should both be written to zero.

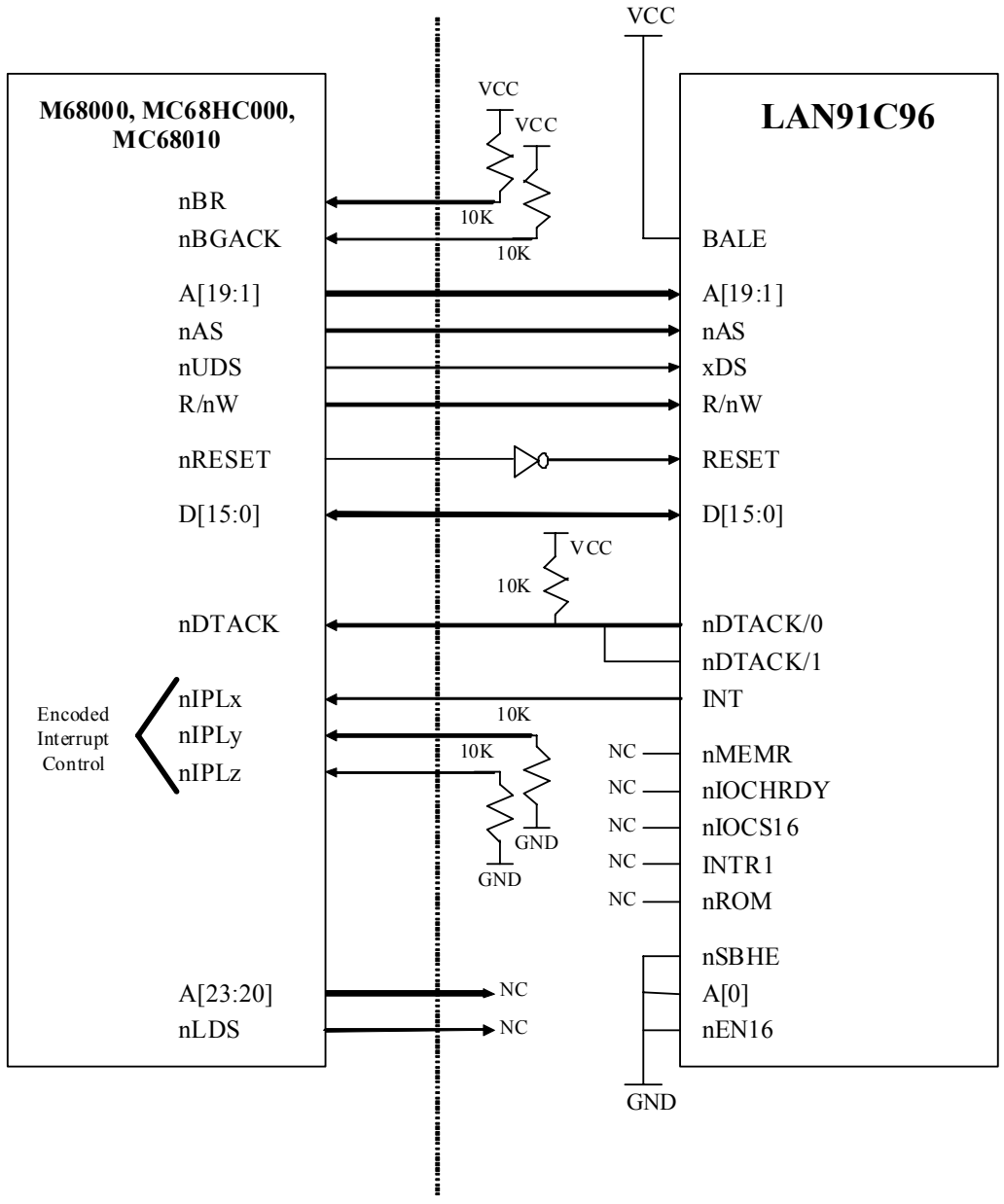
Little Endian / Bit Endian

The LAN91C96 does not swap the lower and upper bytes of the data bus when in Motorola 68000 bus mode. This means any access to the device must consider byte ordering. It is up to the application and hardware layout as to whether the bytes should or should not be swapped.

Boot ROM

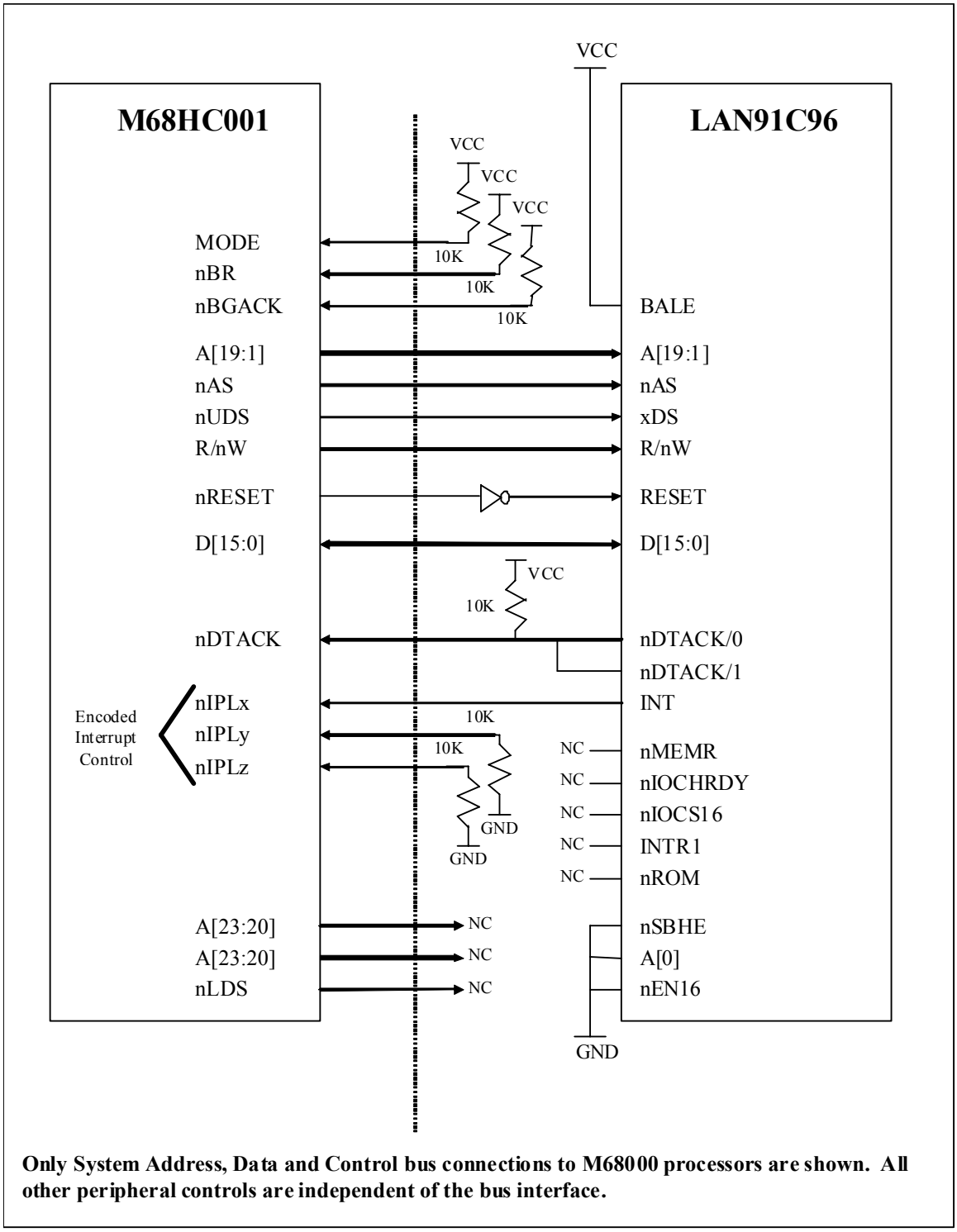
The Base Address Register ROMSIZE bits (Bank 1, Offset 2, Bits 6 and 7) define the size of the external boot ROM and the address lines to use for decode. The nMEMR signal is also required when using an external boot ROM. Because the Motorola 68000 bus interface does not support I/O and Memory cycles, the ROMSIZE bits should always be programmed low to disable address decoding to an external ROM. Address lines A[19:16] will then be ignored and the chip select output nROM will remain high through the internal pull-up.

2.5 BUS CONFIGURATIONS WITH POPULAR M68000 PROCESSORS



Only System Address, Data and Control bus connections to M68000 processors are shown. All other peripheral controls are independent of the bus interface.

Figure 2.2 – MC68000, MC68HC000, AND MC680 10 (16-BIT PROCESSORS)



Only System Address, Data and Control bus connections to M68000 processors are shown. All other peripheral controls are independent of the bus interface.

Figure 2.3 MC68HC001 (8-/16 BIT PROCESSOR)

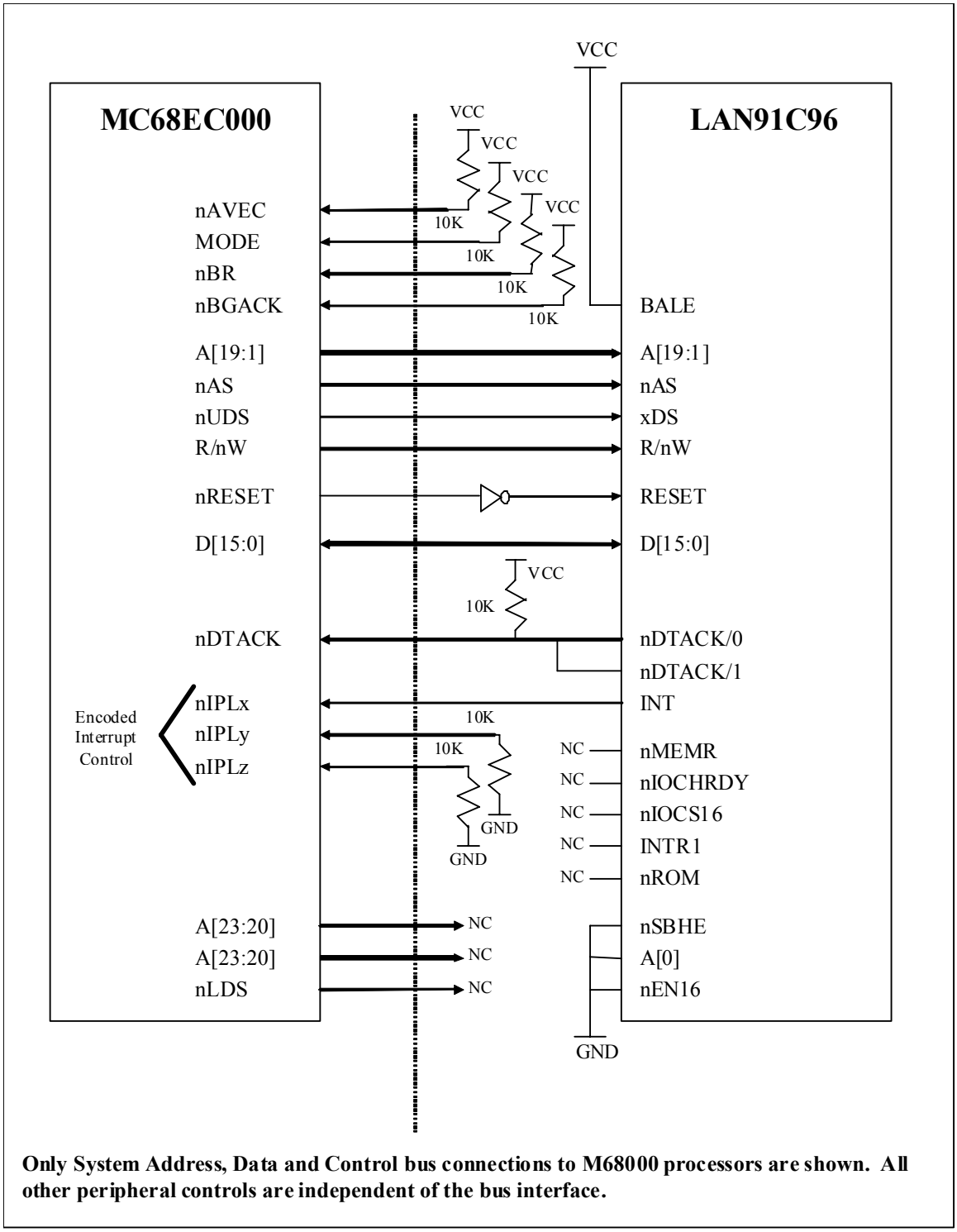


Figure 2.4 - MC68EC000 (8-/16-BIT PROCESSOR)

2.6 MOTOROLA 68000 BUS MODE ANOMALIES

2.6.1 nDTACK/0 and nDTACK/1 Do Not Acknowledge Data Transfers

2.6.2 Problem

nDTACK/0 and nDTACK/1 are specified as data transfer acknowledgment pins. These are output pins from the LAN91C96 that communicate the status of data on the data bus to the host Motorola 68000 processor. For read and write operations these signals are specified to have the following meaning:

2.6.3 Read Operation

During a read operation the LAN91C96 places valid data on the D[15:0] pins. When this data is valid, the LAN91C96 lowers the nDTACK/0 and nDTACK/1 pins to signify to the host processor that data is valid and read to be latched.

2.6.4 Write Operation

During a write operations, the LAN91C96 reads data into its registers. When the data on the data bus has been latched within the LAN91C96, nDTACK/0 and nDTACK/1 are lowered to signify to the host processor that the data has been read and the write cycle can be terminated.

2.6.5 Actual Behavior

All aspects of a read and write operation work except for the nDTACK/0 and nDTACK/1 response. These pins do not go low as expected and as a result the LAN91C96 can not feedback to the host processor that a data transfer has completed.

2.6.6 Solution

The LAN91C96 does not require wait states for read and write operations so the use of nDTACK/0 and nDTACK/1 is not required. These pins can be wired as specified and will not interfere with normal operation.