TPC12 SERIES
CMOS FIELD-PROGRAMMABLE GATE ARRAYS

SRFS002C – D3963, DECEMBER 1991 – REVISED FEBRUARY 1993

- **Three Arrays With Increased Densities**
- **Up to 8000 Equivalent Gate Array Gates**
- **Supported by TI Action Logic™ System (TI-ALS) Software**
- **Desktop Programmable**
- **Reliable, Nonvolatile Antifuse Interconnect**
- **Design Library With Over 250 Macros**
- **User-Programmable I/O Pins**
- **Enhanced Architecture**
  - **Supports Single-Module Sequential Functions**
  - **Supports Wide-Input Combinatorial Functions**
- **Two In-Circuit Diagnostic Probe Pins Support 50-MHz Analysis**
- **Low-Power CMOS Technology**
- **Two High-Speed, Low-Skew Clock Networks**
- **I/O Drive to 10 mA**

description

The TPC12 Series is the next generation of field programmable gate arrays from TI. Based on channeled array architecture, the TPC12 Series provides significant enhancements to gate density and performance while maintaining upward compatibility from TPC10 series designs. The devices are implemented in silicon gate, two-level metal CMOS, and they employ antifuse technology. The unique architecture offers gate array flexibility, high performance and instant turnaround through user programming. Designs of up to 8000 gates can be implemented with the TPC1280 device. The TPC12 Series is supported by the Action Logic System (ALS). ALS is available on Sun™, HP/Apollo™, and 386/486 PC platforms, with CAE interfaces to Cadence™/Valid™, View*logic*™, Mentor Graphics™, and OrCAD™.

Product Family Profile

DEVICE	TPC1280	TPC1240	TPC1225A
Capacity			
Gate array equivalent gates	8000	4000	2500
TTL equivalent packages	210	105	70
CMOS Process	1.2 µm	1.2 µm	1.0 µm
Logic Modules	1232	684	451
Flip-Flops (maximum)	998	565	382
Antifuses	750,000	400,000	250,000

Action Logic, Activator, and Actionprobe are trademarks of Actel Corporation.
Cadence and Valid are trademarks of Cadence Design Systems, Inc.
HP/Apollo is a trademark of HP/Apollo Computer, Inc.
Mentor is a trademark of Mentor Graphics Corporation.
Sun is a trademark of Sun Microsystems, Inc.
OrCAD/SDT III is a trademark of OrCad Systems Corporation.
Viewlogic is a trademark of Viewlogic Systems, Incorporated.

enhanced architecture

Routing efficiency with large gate counts is accomplished with increased routing resources, increased antifuse programming elements, and architectural enhancements. Horizontal routing tracks per channel increase to 36 (vs 25 for TPC10); vertical routing tracks per column increase to 15 (vs 13 for TPC10). All speed-critical module-to-module connections are accomplished with only two low-resistance antifuse elements. Most connections are implemented with either two or three antifuse elements (as shown in Figure 1). No connections are allowed with more than four antifuse elements in the path. The result is predictable performance with fully automatic placement and routing. Device utilization is typically 85% to 95% of available logic modules and 80% of gates.

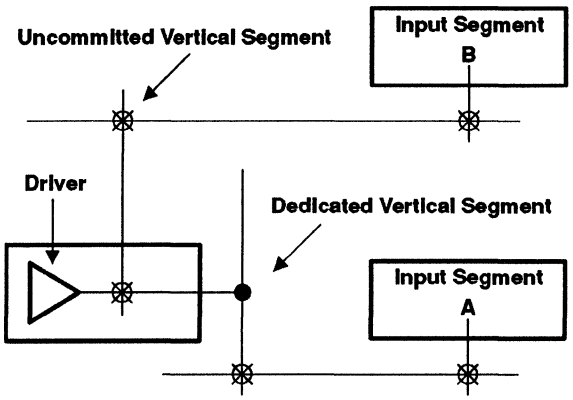


Figure 1. TPC12 Enhanced Routing Architecture

two module design: C modules and S modules

The TPC12 Series offers dedicated combinatorial and combinatorial-sequential modules. The combinatorial module, C Module, has been enhanced to implement high fan-in combinatorial macros, such as 5-input AND, OR, NAND and NOR gates. Additionally, AND-OR gates, XOR gates, AND-XOR gates, and many other combinatorial functions are available.

The combinatorial-sequential module, S Module, has been optimized to implement high-speed flip-flops within a single module. Furthermore, S Modules also include combinatorial logic within the S Module allowing an additional level of logic to be implemented with no additional propagation delay.

hard and soft macros

Designing with TI FPGAs is accomplished through a building-block approach. Over 250 schematic representations of widely used logic functions are stored within the macro library. Each macro represents one of the basic to complex building blocks from which you may build your design. These macros range from simple logic functions such as AND gates to more complex logic functions, such as 16-bit counters and accumulators.

The macros are implemented within the FPGA architecture by utilizing one or more C Modules and/or S Modules. Over 150 of these macros are implemented within single modules, and an additional 25 macros are implemented by connecting only two modules. One-module and two-module macros have a small propagation delay variance providing accurate performance prediction capabilities. These are called hard macros and their propagation delays are specified within the data sheet.

More complex logic functions are also included in the macro library. These soft macros are implemented by using several hard macros. The propagation delays of soft macros are not specified within the data sheet.

programmable I/O pins

Each I/O pin can be configured as an input, output, 3-state, or bidirectional buffer. Inputs are TTL- and CMOS-compatible. Output drive levels meet 10-mA TTL and 6-mA HCT standards.

Optional transparent latches at the I/O pins are provided for both inputs and outputs. I/O latches can be combined with latches in the array to implement master-slave flip-flops as depicted in Figure 2. A selection of registered I/O macros are included in the macro library.

clock distribution network

Two low-skew distribution networks are provided. Each network can be driven by either of two dedicated I/O pins or from internal logic.

enhanced programming and test

The TPC12 Series provides the same type of specifications as the TPC10 Series. All routing tracks, logic modules, program, debug, and test circuits are fully tested prior to customer shipment. Verification of correct antifuse programming is performed automatically with Activator™ 2 programming and debug hardware. The TPC12 Series architecture implements an enhanced programming and test algorithm.

probe pins

TPC12 Series devices have two independent diagnostic probe pins, PRA and PRB. These pins allow the user to observe any internal signals by entering the appropriate net name in the diagnostic software. Signals may be viewed on a logic analyzer using Actionprobe™ diagnostic tools. The probe pins can be used as user-defined I/Os when debugging has been completed.

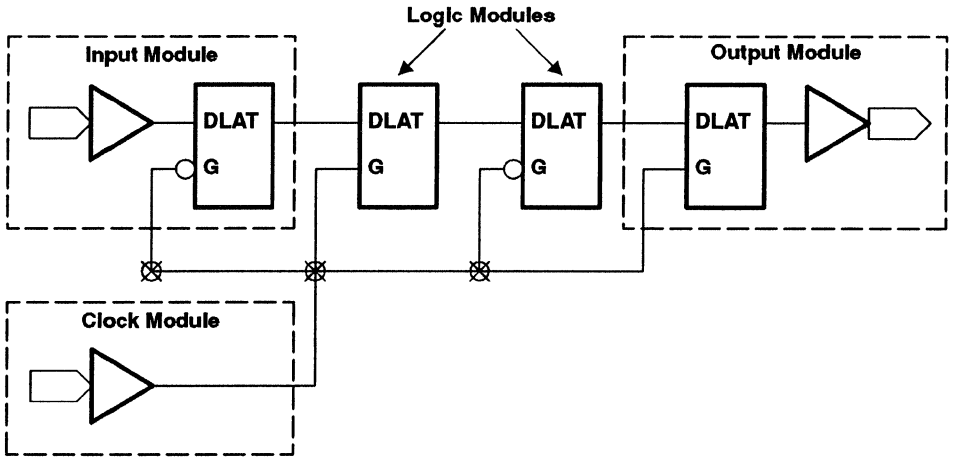


Figure 2. Latched User I/Os

TERMINAL FUNCTIONS

PIN NAME	I/O	DESCRIPTION
CLKA	I	Clock A. TTL clock input for clock distribution networks. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.
CLKB	I	Clock B. TTL clock input for clock distribution networks. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.
DCLK	I	Diagnostic clock. TTL clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is high. This pin functions as an I/O when the MODE pin is low.
GND	I	Ground. Input low supply voltage.
I/O	I/O	Input/output. I/O pins function as an input, output, 3-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically set low by the ALS software.
MODE	I	Mode. The MODE pin controls the use of multifunction pins (DCLK, PRA, PRB, SDI, SDO). When the MODE pin is high, the special functions are active. When the MODE pin is low, the pins function as I/Os.
NC		No connection. This pin is not connected to circuitry within the device.
PRA	O	Probe A. The probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the probe B pin to allow real-time diagnostic output of any signal path within the device. The probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect the programmed design's confidentiality. PRA is active when the MODE pin is high. This pin functions as an I/O when the MODE pin is low.
PRB	O	Probe B. The probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the probe A pin to allow real-time diagnostic output of any signal path within the device. The probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect the programmed design's confidentiality. PRB is active when the MODE pin is high. This pin functions as an I/O when the MODE pin is low.
SDI	I	Serial data input. Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is high. This pin functions as an I/O when the MODE pin is low.
SDO	O	Serial data output for diagnostic probe. SDO is active when the MODE pin is high. This pin functions as an I/O when the MODE pin is low.
V_{CC}	I	Supply voltage. Input high supply voltage.
V_{KS}	I	Programming voltage. Input supply voltage used for device programming. This pin must be connected to GND during normal operation.
V_{PP}	I	Programming voltage. Input supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.
V_{SV}	I	Programming voltage. Input supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range , V_{CC} (see Notes 1, 2, and 3) ..... – 0.5 V to 7 V
Input voltage range, V_I ..... – 0.5 to V_{CC} + 0.5 V
Output voltage range, V_O ..... – 0.5 to V_{CC} + 0.5 V
Input clamp current‡ , I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ± 20 mA
Output clamp current§, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ± 20 mA
Continuous output current§, (V_O = 0 to V_{CC}) ..... ± 25 mA
Operating free-air temperature range, T_A: Commercial ..... 0°C to 70°C
Industrial ..... – 40°C to 85°C
Operating case temperature range, T_C: Military ..... – 55°C to 125°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ Applies for input and bidirectional buffers
§ Applies for bidirectional and output buffers
NOTES: 1. $V_{PP} = V_{CC}$ except during device programming
2. $V_{SV} = V_{CC}$ except during device programming
3. V_{KS} = GND except during device programming

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Commercial	4.75	5	5.25	V
		Industrial	4.5	5	5.5	
		Military	4.5	5	5.5	
V_{PP}	Program pin voltage (while not programming)		V_{CC}		V_{CC}	V
V_{IH}	High-level input voltage		2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
T_A	Operating free-air temperature	Commercial	0		70	°C
		Industrial	−40		85	
T_C	Operating case temperature	Military	−55		125	°C

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	COMMERCIAL			INDUSTRIAL			MILITARY			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage (see Note 4)	I_{OH} = −10 mA	2.4									V
		I_{OH} = −6 mA	3.84									
		I_{OH} = −4 mA				3.7			3.7			
V_{OL}	Low-level output voltage (see Note 4)	I_{OL} = 10 mA			0.5							V
		I_{OL} = 6 mA			0.33			0.4			0.4	
I_I	Input current	V_I = V_{CC} or 0			±10			±10			±10	µA
I_{OZ}	Off-state output current	V_O = V_{CC} or 0			±10			±10			±10	µA
I_{CC}	Standby supply current (see Note 5)				10			20			25	mA
C_{io}	I/O capacitance (see Notes 6 and 7)			7			7			7		pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 4. Only one output tested at a time. V_{CC} = minimum value in recommended operating conditions.
5. All outputs unloaded. All inputs = V_{CC} or GND.
6. Not tested, for information only
7. Includes worst-case 176 CPGA package capacitance. V_O = 0, f = 1 MHz

timing characteristics

Timing characteristics for TPC12 Series arrays fall into three categories: family dependent, device dependent, and design dependent. The output buffer characteristics are common to all TPC12 Series devices. Internal module delays are device dependent. Internal wiring delays between modules are design dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the ALS timer utility or performing simulation with post-layout delays. The macro propagation delays in the switching characteristics tables include the module delay plus estimates derived from statistical analysis for wiring delay. This statistical estimate is based on 90% module utilization.

critical and typical nets

Propagation delays are expressed for two types of nets: critical and typical. Critical nets are determined by net property assignment before placement and routing. Up to 6% of the nets in a design may be designated critical.

fan-out dependency

Propagation delays are dependent on the fan-out (number of loads) driven by a macro. Delay increases with increasing fan-out due to capacitive loading of the macro inputs and the resistance and capacitance of the interconnect.

long tracks

Some nets in the design will utilize long tracks. Long tracks are special routing resources that span multiple rows or columns of modules. Long tracks are most frequently used in large fan-out (> 10) situations. Long tracks will utilize three and sometimes four antifuse connections. The increased capacitance and resistance will result in longer net delays for macros connected to long tracks. Typically up to 6% of the nets in a fully utilized device will require long tracks. Long tracks add an additional 10-ns to 15-ns delay.

slow input transition (rise and fall) times

Slow signal transition is a condition that commonly occurs even in today's high-performance systems. A typical example is the signal degradation encountered with signals coming off of a highly capacitive bus. These slow signal transitions can cause undesirable results when traveling through the threshold region of a CMOS input. Texas Instruments recommends that input signal transitions be limited to 500 ns or less to ensure device integrity.

timing derating

Operating temperature, operating voltage, and device processing conditions, along with device die size and speed grade, account for variations in array timing characteristics. These variations are summarized into a derating factor for TPC12 array typical timing specifications. The derating factors as shown in table are based on the recommended operating conditions for TPC12 applications. The derating curves in Figure 3 and Figure 4 show worst-to-best case operating voltage range and best-to-worst case operating temperature range. The temperature derating curves are based on device junction temperature. Actual junction temperature is determined from ambient temperature, power dissipation, and package thermal characteristics.

Table 1. Timing Derating Factor (x typical) (see Note 8)

C SUFFIX		I SUFFIX		M SUFFIX	
BEST CASE	WORST CASE	BEST CASE	WORST CASE	BEST CASE	WORST CASE
0.40	1.40	0.37	1.50	0.35	1.60

NOTE 8: Best case reflects maximum operating voltage, minimum operating temperature, and best case processing. Worst case reflects minimum operating voltage, maximum operating temperature, and worst case processing. Best case derating is based on sample data only and is not guaranteed.

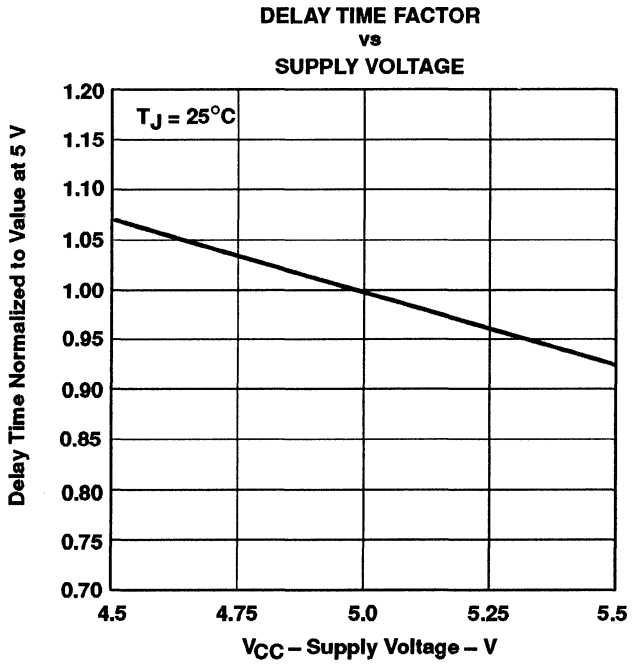


Figure 3

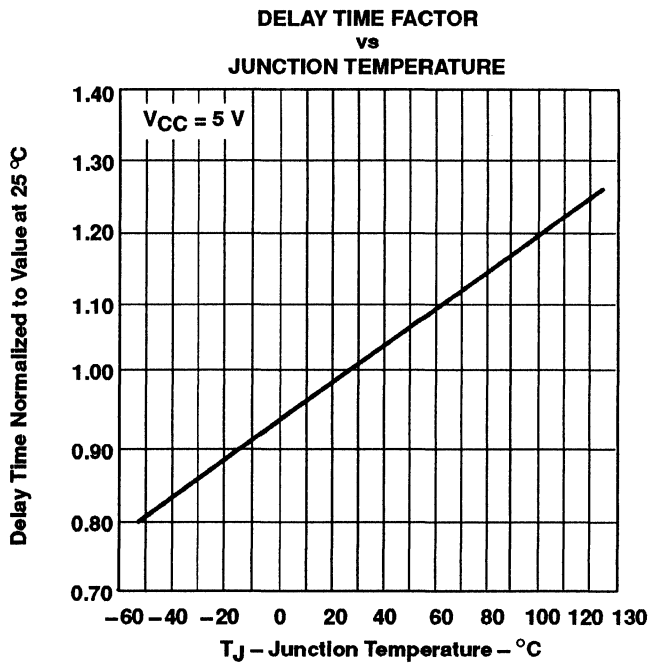


Figure 4

TPC1225A timing requirements over recommended operating conditions, no further derating required (see Note 9)

			COMMERCIAL		INDUSTRIAL		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	Flip-flop		75		66	MHz
t_{cp}	Clock period	Flip-flop	13		13		ns
t_w	Pulse duration (active pulse)	Flip-flop CLK	4		4.5		ns
		Flip-flop PRE or CLR	4		4.5		
		Latch G	4		4.5		
		Latch PRE or CLR	4		4.5		
t_{su}	Setup time	Flip-flop data inputs (A, B, D, J, K, S, or T) before CLK	0.4		0.5		ns
		Flip-flop PRE or CLR (inactive) before CLK	1		1.5		
		Flip-flop E before CLK	1		1.5		
		Latch data inputs (A, B, D, or S) before G	0.4		0.5		
		Latch PRE or CLR (inactive) before G	1		1.5		
		Latch E before G	1		1.5		
		Input buffer latch pad input	−2.5		−3		
		Output buffer latch D before G	0.4		0.5		
t_h	Hold time	Flip-flop data inputs (A, B, D, J, K, S, or T) after CLK	0		0		ns
		Flip-flop E after CLK	0		0		
		Latch data inputs (A, B, D, or S) after G	0		0		
		Latch E after G	0		0		
		Input buffer latch pad input after G	2		2.5		
		Output buffer latch D after G	0		0		

NOTE 9: Data applies to macros based on the sequential module (S Module). Timing parameters for sequential macros constructed from combinatorial modules (C Module) can be obtained from the TI-ALS timer utility.

TPC1225A switching characteristics

propagation delays, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		OUTPUT NET	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{pd}	Single module	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	Single module	Typical net	4.9	5.3	5.7	7	10	ns
t_{pd}	Dual module	Critical net	7.5	8	8.5	9	—	ns
t_{pd}	Dual module	Typical net	7.9	8.3	8.7	10	13	ns
t_{pd}	CLK to Q	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	CLK to Q	Typical net	4.9	5.3	5.7	7	10	ns
t_{pd}	G to Q	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	G to Q	Typical net	4.9	5.3	5.7	7	10	ns
t_{pd}	PRE or CLR to Q	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	PRE or CLR to Q	Typical net	4.9	5.3	5.7	7	10	ns

NOTE 10: FO means fan out.

TPC1225A switching characteristics (continued)

Input buffer, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{PLH}	Pad	Y or Q	6.1	6.5	6.9	7.4	10.5	ns
t_{PHL}			5.9	6.4	6.8	7.3	10.4	
t_{PLH}	G	Q	6.1	6.5	6.9	7.4	10.5	ns
t_{PHL}			5.9	6.4	6.8	7.3	10.4	

NOTE 10: FO means fan out.

output buffer, V_{CC} = 5 V, T_J = 25°C, process = typical

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DRIVING CMOS LOADS	DRIVING TTL LOADS	UNIT
t_{PLH}	D	Pad	C_L = 50 pF	6.7	4.6	ns
t_{PHL}				4.9	6.5	
t_{PZH}	E	Pad		8.3	8.3	ns
t_{PZL}				5.5	5.5	
t_{PHZ}	E	Pad		4.5	4.5	ns
t_{PLZ}				6	6	
t_{PLH}	G	Pad		4.6	4.6	ns
t_{PHL}				6.5	6.5	
Δt_{PLH}	D	Pad		0.11	0.06	ns/pF
Δt_{PHL}				0.08	0.11	

global clock network, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		FO = 32	FO = 128	FO = 256	UNIT
t_{PLH}	Propagation delay time, low-to-high output	7.8	8.7	9.3	ns
t_{PHL}	Propagation delay time, high-to-low output	7.8	8.8	9.4	ns
t_{wH}min	Pulse duration, high, minimum	4.5	5.1	5.5	ns
t_{wL}min	Pulse duration, low, minimum	4.5	5.1	5.5	ns
t_{sk}max	Maximum skew	0.5	1	2.5	ns
$t_{su(ext)}$†	Setup time, external input latch	0	0	0	ns
$t_{h(ext)}$†	Hold time, external input latch	7	8	11.2	ns
t_C	Minimum cycle time	9.1	9.5	10	ns
f_{max}	Maximum clock frequency	110	105	100	MHz

† Derating does not apply to this parameter.
NOTE 10: FO means fan out.

ADVANCE INFORMATION

TPC1225A-1 timing requirements over recommended operating conditions, no further derating required (see Note 9)

			C SUFFIX		I SUFFIX		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	Flip-flop		85		75	MHz
t_{cp}	Clock period	Flip-flop	11.7		13.3		ns
	Pulse duration (active pulse)	Flip-flop CLK	4		4.5		ns
		Flip-flop PRE or CLR	4		4.5		
		Latch G	4		4.5		
		Latch PRE or CLR	4		4.5		
t_{su}	Setup time	Flip-flop data inputs (A, B, D, J, K, S, or T) before CLK	0.4		0.5		ns
		Flip-flop PRE or CLR (inactive) before CLK	1		1.5		
		Flip-flop E before CLK	1		1.5		
		Latch data inputs (A, B, D, or S) before G	0.4		0.5		
		Latch PRE or CLR (inactive) before G	1		1.5		
		Latch E before G	1		1.5		
		Input buffer latch pad input	−2.5		−3		
		Output buffer latch D before G	0.4		0.5		
t_h	Hold time	Flip-flop data inputs (A, B, D, J, K, S, or T) before CLK	0		0		ns
		Flip-flop E after CLK	0		0		
		Latch data inputs (A, B, D, or S) after G	0		0		
		Latch E after G	0		0		
		Input buffer latch pad input after G	2		2.5		
		Output buffer latch D after G	0		0		

NOTE 9: Data applies to macros based on the sequential module (S Module). Timing parameters for sequential macros constructed from combinatorial modules (C Module) can be obtained from the TI-ALS timer utility.

TPC1225A-1 switching characteristics

propagation delays, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		OUTPUT NET	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{pd}	Single module	Critical net	3.5	3.9	4.3	4.8	—	ns
t_{pd}	Single module	Typical net	4.4	4.8	5.1	6.3	9	ns
t_{pd}	Dual module	Critical net	7.5	8	8.5	9	—	ns
t_{pd}	Dual module	Typical net	7.4	7.8	8.1	9.3	12	ns
t_{pd}	CLK to Q	Critical net	3.5	3.9	4.3	4.8	—	ns
t_{pd}	CLK to Q	Typical net	4.4	4.8	5.1	6.3	9	ns
t_{pd}	G to Q	Critical net	3.5	3.9	4.3	4.8	—	ns
t_{pd}	G to Q	Typical net	4.4	4.8	5.1	6.3	9	ns
t_{pd}	PRE or CLR to Q	Critical net	3.5	3.9	4.3	4.8	—	ns
t_{pd}	PRE or CLR to Q	Typical net	4.4	4.8	5.1	6.3	9	ns

NOTE 10: FO means fan out.

TPC1225A-1 switching characteristics (continued)

Input buffer, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{PLH}	Pad	Y or Q	5.5	5.9	6.3	6.7	9.5	ns
t_{PHL}			5.3	5.8	6.1	6.6	9.4	
t_{PLH}	G	Q	5.5	5.9	6.3	6.7	9.5	ns
t_{PHL}			5.3	5.8	6.1	6.6	9.4	

NOTE 10: FO means fan out.

output buffer, V_{CC} = 5 V, T_J = 25°C, process = typical

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DRIVING CMOS LOADS	DRIVING TTL LOADS	UNIT
t_{PLH}	D	Pad	C_L = 50 pF	6.7	4.6	ns
t_{PHL}				4.9	6.5	
t_{PZH}	E	Pad		8.3	8.3	ns
t_{PZL}				5.5	5.5	
t_{PHZ}	E	Pad		4.5	4.5	ns
t_{PLZ}				6	6	
t_{PLH}	G	Pad		4.6	4.6	ns
t_{PHL}				6.5	6.5	
Δt_{PLH}	D	Pad		0.11	0.06	ns/pF
Δt_{PHL}				0.08	0.11	

global clock network, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		FO = 32	FO = 128	FO = 256	UNIT
t_{PLH}	Propagation delay time, low-to-high output	7	7.8	8.6	ns
t_{PHL}	Propagation delay time, high-to-low output	7	7.8	8.6	ns
t_{wH}min	Pulse duration, high, minimum	4.2	4.5	5	ns
t_{wL}min	Pulse duration, low, minimum	4.2	4.5	5	ns
t_{sk}max	Maximum skew	0.5	1	2.5	ns
$t_{su(ext)}$†	Setup time, external input latch	0	0	0	ns
$t_{h(ext)}$†	Hold time, external input latch	7.0	8	11.2	ns
t_C	Minimum cycle time	9.3	8.7	9.1	ns
f_{max}	Maximum clock frequency	120	115	110	MHz

† Derating does not apply to this parameter.
NOTE 10: FO means fan out.

ADVANCE INFORMATION

TPC1240 timing requirements over recommended operating conditions, no further derating required (see Note 9)

			C SUFFIX		I SUFFIX		M SUFFIX		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	Flip-flop		66		55		50	MHz
t_{cp}	Clock period	Flip-flop	15		18		20		ns
t_w	Pulse duration (active pulse)	Flip-flop CLK	4		4.5		5		ns
		Flip-flop PRE or CLR	4		4.5		5		
		Latch G	4		4.5		5		
		Latch PRE or CLR	4		4.5		5		
t_{su}	Setup time	Flip-flop data inputs (A, B, D, J, K, S, or T) before CLK	0.4		0.5		1		ns
		Flip-flop PRE or CLR (inactive) before CLK	1		1.5		2		
		Flip-flop E before CLK	1		1.5		2		
		Latch data inputs (A, B, D, or S) before G	0.4		0.5		1		
		Latch PRE or CLR (inactive) before G	1		1.5		2		
		Latch E before G	1		1.5		2		
		Input buffer latch pad input	−2.5		−3		−3.5		
		Output buffer latch D before G	0.4		0.5		1		
t_h	Hold time	Flip-flop data inputs (A, B, D, J, K, S, or T) after CLK	0		0		0		ns
		Flip-flop E after CLK	0		0		0		
		Latch data inputs (A, B, D, or S) after G	0		0		0		
		Latch E after G	0		0		0		
		Input buffer latch pad input after G	2		2.5		2.5		
		Output buffer latch D after G	0		0		0		

NOTE 9: Data applies to macros based on the sequential module (S Module). Timing parameters for sequential macros constructed from combinatorial modules (C Module) can be obtained from the TI-ALS timer utility.

TPC1240 switching characteristics

propagation delays, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		OUTPUT NET	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{pd}	Single module	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	Single module	Typical net	4.9	5.3	5.7	7	10	ns
t_{pd}	Dual module	Critical net	7.5	8	8.5	9	—	ns
t_{pd}	Dual module	Typical net	7.9	8.3	8.7	10	13	ns
t_{pd}	CLK to Q	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	CLK to Q	Typical net	4.9	5.3	5.7	7	10	ns
t_{pd}	G to Q	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	G to Q	Typical net	4.9	5.3	5.7	7	10	ns
t_{pd}	PRE or CLR to Q	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	PRE or CLR to Q	Typical net	4.9	5.3	5.7	7	10	ns

NOTE 10: FO means fan out.

TPC1240 switching characteristics (continued)

Input buffer, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{PLH}	Pad	Y or Q	6.1	6.5	6.9	7.4	10.5	ns
t_{PHL}			5.9	6.4	6.8	7.3	10.4	
t_{PLH}	G	Q	6.1	6.5	6.9	7.4	10.5	ns
t_{PHL}			5.9	6.4	6.8	7.3	10.4	

NOTE 10: FO means fan out.

output buffer, V_{CC} = 5 V, T_J = 25°C, process = typical

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DRIVING CMOS LOADS	DRIVING TTL LOADS	UNIT
t_{PLH}	D	Pad	C_L = 50 pF	6.7	4.6	ns
t_{PHL}				4.9	6.5	
t_{PZH}	E	Pad		8.3	8.3	ns
t_{PZL}				5.5	5.5	
t_{PHZ}	E	Pad		4.5	4.5	ns
t_{PLZ}				6	6	
t_{PLH}	G	Pad		4.6	4.6	ns
t_{PHL}				6.5	6.5	
Δt_{PLH}	D	Pad		0.11	0.06	ns/pF
Δt_{PHL}				0.08	0.11	

global clock network, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		FO = 32	FO = 128	FO = 256	UNIT
t_{PLH}	Propagation delay time, low-to-high output	9.1	10.1	11.2	ns
t_{PHL}	Propagation delay time, high-to-low output	9.1	10.2	11.3	ns
t_{wH}min	Pulse duration, high, minimum	4	4.5	5	ns
t_{wL}min	Pulse duration, low, minimum	4	4.5	5	ns
t_{sk}max	Maximum skew	0.5	1	2.5	ns
$t_{su(ext)}$†	Setup time, external input latch	0	0	0	ns
$t_{h(ext)}$†	Hold time, external input latch	7	8	11.2	ns
t_C	Minimum cycle time	11.1	11.5	11.8	ns
f_{max}	Maximum clock frequency	90	87	85	MHz

† Derating does not apply to this parameter.
NOTE 10: FO means fan out.

TPC1240-1 timing requirements over recommended operating conditions, no further derating required (see Note 9)

			C SUFFIX		I SUFFIX		M SUFFIX		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	Flip-flop		75		66		55	MHz
t_{cp}	Clock period	Flip-flop	13		15		18		ns
	Pulse duration (active pulse)	Flip-flop CLK	4		4.5		5		ns
		Flip-flop PRE or CLR	4		4.5		5		
		Latch G	4		4.5		5		
		Latch PRE or CLR	4		4.5		5		
t_{su}	Setup time	Flip-flop data inputs (A, B, D, J, K, S, or T) before CLK	0.4		0.5		1		ns
		Flip-flop PRE or CLR (inactive) before CLK	1		1.5		2		
		Flip-flop E before CLK	1		1.5		2		
		Latch data inputs (A, B, D, or S) before G	0.4		0.5		1		
		Latch PRE or CLR (inactive) before G	1		1.5		2		
		Latch E before G	1		1.5		2		
		Input buffer latch pad input	–2.5		–3		–3.5		
		Output buffer latch D before G	0.4		0.5		1		
t_h	Hold time	Flip-flop data inputs (A, B, D, J, K, S, or T) before CLK	0		0		0		ns
		Flip-flop E after CLK	0		0		0		
		Latch data inputs (A, B, D, or S) after G	0		0		0		
		Latch E after G	0		0		0		
		Input buffer latch pad input after G	2		2.5		2.5		
		Output buffer latch D after G	0		0		0		

NOTE 9: Data applies to macros based on the sequential module (S Module). Timing parameters for sequential macros constructed from combinatorial modules (C Module) can be obtained from the TI-ALS timer utility.

TPC1240-1 switching characteristics

propagation delays, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		OUTPUT NET	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{pd}	Single module	Critical net	3.5	3.9	4.3	4.8	—	ns
t_{pd}	Single module	Typical net	4.4	4.8	5.1	6.3	9	ns
t_{pd}	Dual module	Critical net	7.5	8	8.5	9	—	ns
t_{pd}	Dual module	Typical net	7.4	7.8	8.1	9.3	12	ns
t_{pd}	CLK to Q	Critical net	3.5	3.9	4.3	4.8	—	ns
t_{pd}	CLK to Q	Typical net	4.4	4.8	5.1	6.3	9	ns
t_{pd}	G to Q	Critical net	3.5	3.9	4.3	4.8	—	ns
t_{pd}	G to Q	Typical net	4.4	4.8	5.1	6.3	9	ns
t_{pd}	PRE or CLR to Q	Critical net	3.5	3.9	4.3	4.8	—	ns
t_{pd}	PRE or CLR to Q	Typical net	4.4	4.8	5.1	6.3	9	ns

NOTE 10: FO means fan out.

ADVANCE INFORMATION

TPC1240-1 switching characteristics (continued)

input buffer, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{PLH}	Pad	Y or Q	5.5	5.9	6.3	6.7	9.5	ns
t_{PHL}			5.3	5.8	6.1	6.6	9.4	
t_{PLH}	G	Q	5.5	5.9	6.3	6.7	9.5	ns
t_{PHL}			5.3	5.8	6.1	6.6	9.4	

NOTE 10: FO means fan out.

output buffer, V_{CC} = 5 V, T_J = 25°C, process = typical

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DRIVING CMOS LOADS	DRIVING TTL LOADS	UNIT
t_{PLH}	D	Pad	C_L = 50 pF	6.7	4.6	ns
t_{PHL}				4.9	6.5	
t_{PZH}	E	Pad		8.3	8.3	ns
t_{PZL}				5.5	5.5	
t_{PHZ}	E	Pad		4.5	4.5	ns
t_{PLZ}				6	6	
t_{PLH}	G	Pad		4.6	4.6	ns
t_{PHL}				6.5	6.5	
Δt_{PLH}	D	Pad		0.11	0.06	ns/pF
Δt_{PHL}				0.08	0.11	

global clock network, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		FO = 32	FO = 128	FO = 256	UNIT
t_{PLH}	Propagation delay time, low-to-high output	7.8	8.7	9.3	ns
t_{PHL}	Propagation delay time, high-to-low output	7.8	8.8	9.4	ns
t_{wH}min	Pulse duration, high, minimum	4	4.5	5	ns
t_{wL}min	Pulse duration, low, minimum	4	4.5	5	ns
t_{sk}max	Maximum skew	0.5	1	2.5	ns
$t_{su(ext)}$†	Setup time, external input latch	0	0	0	ns
$t_{h(ext)}$†	Hold time, external input latch	7	8	11.2	ns
t_C	Minimum cycle time	9.1	9.5	10	ns
f_{max}	Maximum clock frequency	110	105	100	MHz

† Derating does not apply to this parameter.
NOTE 10: FO means fan out.

ADVANCE INFORMATION

TPC1280 timing requirements over recommended operating conditions, no further derating required (see Note 9)

			C SUFFIX		I SUFFIX		M SUFFIX		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	Flip-flop		48		43		39	MHz
t_{cp}	Clock period	Flip-flop	18		20		22		ns
t_w	Pulse duration (active pulse)	Flip-flop CLK	4		4.5		5		ns
		Flip-flop PRE or CLR	4		4.5		5		
		Latch G	4		4.5		5		
		Latch PRE or CLR	4		4.5		5		
t_{su}	Setup time	Flip-flop data inputs (A, B, D, J, K, S, or T) before CLK	0.4		0.5		1		ns
		Flip-flop PRE or CLR (inactive) before CLK	1		1.5		2		
		Flip-flop E before CLK	1		1.5		2		
		Latch data inputs (A, B, D, or S) before G	0.4		0.5		1		
		Latch PRE or CLR (inactive) before G	1		1.5		2		
		Latch E before G	1		1.5		2		
		Input buffer latch pad input	−2.5		−3		−3.5		
		Output buffer latch D before G	0.4		0.5		1		
t_h	Hold time	Flip-flop data inputs (A, B, D, J, K, S, or T) after CLK	0		0		0		ns
		Flip-flop E after CLK	0		0		0		
		Latch data inputs (A, B, D, or S) after G	0		0		0		
		Latch E after G	0		0		0		
		Input buffer latch pad input after G	2		2.5		2.5		
		Output buffer latch D after G	0		0		0		

NOTE 9: Data applies to macros based on the sequential module (S Module). Timing parameters for sequential macros constructed from combinatorial modules (C Module) can be obtained from the TI-ALS timer utility.

TPC1280 switching characteristics

propagation delays, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		OUTPUT NET	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{pd}	Single module	Critical net	4.5	5	5.5	6	—	ns
t_{pd}	Single module	Typical net	5.7	6.2	6.7	8.2	11.7	ns
t_{pd}	Dual module	Critical net	7.5	8	8.5	9	—	ns
t_{pd}	Dual module	Typical net	8.7	9.2	9.7	11.2	14.7	ns
t_{pd}	CLK to Q	Critical net	4.5	5	5.5	6	—	ns
t_{pd}	CLK to Q	Typical net	5.7	6.2	6.7	8.2	11.7	ns
t_{pd}	G to Q	Critical net	4.5	5	5.5	6	—	ns
t_{pd}	G to Q	Typical net	5.7	6.2	6.7	8.2	11.7	ns
t_{pd}	PRE or CLR to Q	Critical net	4.5	5	5.5	6	—	ns
t_{pd}	PRE or CLR to Q	Typical net	5.7	6.2	6.7	8.2	11.7	ns

NOTE 10: FO means fan out.

TPC1280 switching characteristics (continued)

input buffer, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{PLH}	Pad	Y or Q	6.7	7.2	7.7	8.2	11.7	ns
t_{PHL}			6.6	7.1	7.6	8.1	11.5	
t_{PLH}	G	Q	6.6	7.2	7.7	8.2	11.7	ns
t_{PHL}			6.4	6.9	7.5	8	11.4	

NOTE 10: FO means fan out.

output buffer, V_{CC} = 5 V, T_J = 25°C, process = typical

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DRIVING CMOS LOADS	DRIVING TTL LOADS	UNIT
t_{PLH}	D	Pad	C_L = 50 pF	6.7	4.6	ns
t_{PHL}				4.9	6.5	
t_{PZH}	E	Pad		8.3	8.3	ns
t_{PZL}				5.5	5.5	
t_{PHZ}	E	Pad		4.5	4.5	ns
t_{PLZ}				6	6	
t_{PLH}	G	Pad		4.6	4.6	ns
t_{PHL}				6.5	6.5	
Δt_{PLH}	D	Pad		0.11	0.06	ns/pF
Δt_{PHL}				0.08	0.11	

global clock network, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER	DESCRIPTION	FO = 32	FO = 128	FO = 384	UNIT
t_{PLH}	Propagation delay time, low-to-high output	9.1	10.1	12.3	ns
t_{PHL}	Propagation delay time, high-to-low output	9.1	10.2	12.5	ns
t_{WH}min	Pulse duration, high, minimum	4	4.5	5	ns
t_{WL}min	Pulse duration, low, minimum	4	4.5	5	ns
t_{sk}max	Maximum skew	0.5	1	2.5	ns
$t_{su(ext)}$†	Setup time, external input latch	0	0	0	ns
$t_{h(ext)}$†	Hold time, external input latch	7	8	11.2	ns
t_C	Minimum cycle time	13.3	14.3	15.3	ns
f_{max}	Maximum clock frequency	75	70	65	MHz

† Derating does not apply to this parameter.
NOTE 10: FO means fan out.

TPC1280-1 timing requirements over recommended operating conditions, no further derating required (see Note 9)

			C SUFFIX		I SUFFIX		M SUFFIX		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	Flip-flop		65		60		50	MHz
t_{cp}	Clock period	Flip-flop	15		18		20		ns
t_w	Pulse duration (active pulse)	Flip-flop CLK	4		4.5		5		ns
		Flip-flop PRE or CLR	4		4.5		5		
		Latch G	4		4.5		5		
		Latch PRE or CLR	4		4.5		5		
t_{su}	Setup time	Flip-flop data inputs (A, B, D, J, K, S, or T) before CLK	0.4		0.5		1		ns
		Flip-flop PRE or CLR (inactive) before CLK	1		1.5		2		
		Flip-flop E before CLK	1		1.5		2		
		Latch data inputs (A, B, D, or S) before G	0.4		0.5		1		
		Latch PRE or CLR (inactive) before G	1		1.5		2		
		Latch E before G	1		1.5		2		
		Input buffer latch pad input	−2.5		−3		−3.5		
		Output buffer latch D before G	0.4		0.5		1		
t_h	Hold time	Flip-flop data inputs (A, B, D, J, K, S, or T) after CLK	0		0		0		ns
		Flip-flop E after CLK	0		0		0		
		Latch data inputs (A, B, D, or S) after G	0		0		0		
		Latch E after G	0		0		0		
		Input buffer latch pad input after G	2		2.5		2.5		
		Output buffer latch D after G	0		0		0		

NOTE 9: Data applies to macros based on the sequential module (S Module). Timing parameters for sequential macros constructed from combinatorial modules (C Module) can be obtained from the TI-ALS timer utility.

TPC1280-1 switching characteristics

propagation delays, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		OUTPUT NET	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{pd}	Single module	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	Single module	Typical net	4.9	5.3	5.7	7	10	ns
t_{pd}	Dual module	Critical net	7.5	8.0	8.5	9	—	ns
t_{pd}	Dual module	Typical net	7.9	8.3	8.7	10	13	ns
t_{pd}	CLK to Q	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	CLK to Q	Typical net	4.9	5.3	5.7	7	10	ns
t_{pd}	G to Q	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	G to Q	Typical net	4.9	5.3	5.7	7	10	ns
t_{pd}	PRE or CLR to Q	Critical net	3.9	4.3	4.8	5.3	—	ns
t_{pd}	PRE or CLR to Q	Typical net	4.9	5.3	5.7	7	10	ns

NOTE 10: FO means fan out.

TPC1280-1 switching characteristics (continued)

Input buffer, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FO = 1	FO = 2	FO = 3	FO = 4	FO = 8	UNIT
t_{PLH}	Pad	Y or Q	6.1	6.5	6.9	7.4	10.5	ns
t_{PHL}			5.9	6.4	6.8	7.3	10.4	
t_{PLH}	G	Q	6.1	6.5	6.9	7.4	10.5	ns
t_{PHL}			5.9	6.4	6.8	7.3	10.4	

NOTE 10: FO means fan out.

output buffer, V_{CC} = 5 V, T_J = 25°C, process = typical

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	DRIVING CMOS LOADS	DRIVING TTL LOADS	UNIT
t_{PLH}	D	Pad	C_L = 50 pF	6.7	4.6	ns
t_{PHL}				4.9	6.5	
t_{PZH}	E	Pad		8.3	8.3	ns
t_{PZL}				5.5	5.5	
t_{PHZ}	E	Pad		4.5	4.5	ns
t_{PLZ}				6	6	
t_{PLH}	G	Pad		4.6	4.6	ns
t_{PHL}				6.5	6.5	
Δt_{PLH}	D	Pad		0.11	0.06	ns/pF
Δt_{PHL}				0.08	0.11	

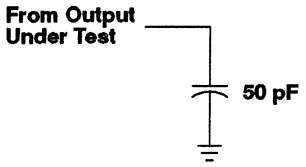
global clock network, V_{CC} = 5 V, T_J = 25°C, process = typical (see Note 10)

PARAMETER		FO = 32	FO = 128	FO = 384	UNIT
t_{PLH}	Propagation delay time, low-to-high output	7.8	8.7	10.4	ns
t_{PHL}	Propagation delay time, high-to-low output	7.8	8.8	10.6	ns
t_{wH}min	Pulse duration, high, minimum	4	4.5	5	ns
t_{wL}min	Pulse duration, low, minimum	4	4.5	5	ns
t_{sk}max	Maximum skew	0.5	1	2.5	ns
$t_{su(ext)}$†	Setup time, external input latch	0	0	0	ns
$t_{h(ext)}$†	Hold time, external input latch	7	8	11.2	ns
t_C	Minimum cycle time	11.4	12	13	ns
f_{max}	Maximum clock frequency	89	83	77	MHz

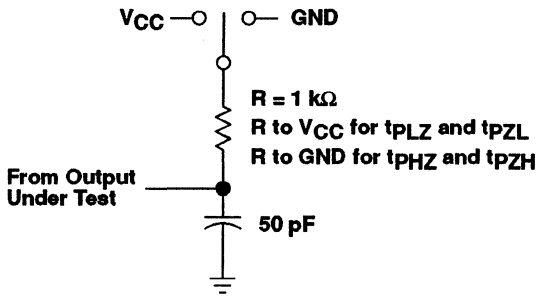
† Derating does not apply to this parameter.
NOTE 10: FO means fan out.

PARAMETER MEASUREMENT INFORMATION

AC test loads



LOAD CIRCUIT 1
Used to measure propagation delay



LOAD CIRCUIT 2
Used to measure rising/falling edges

output buffer delays

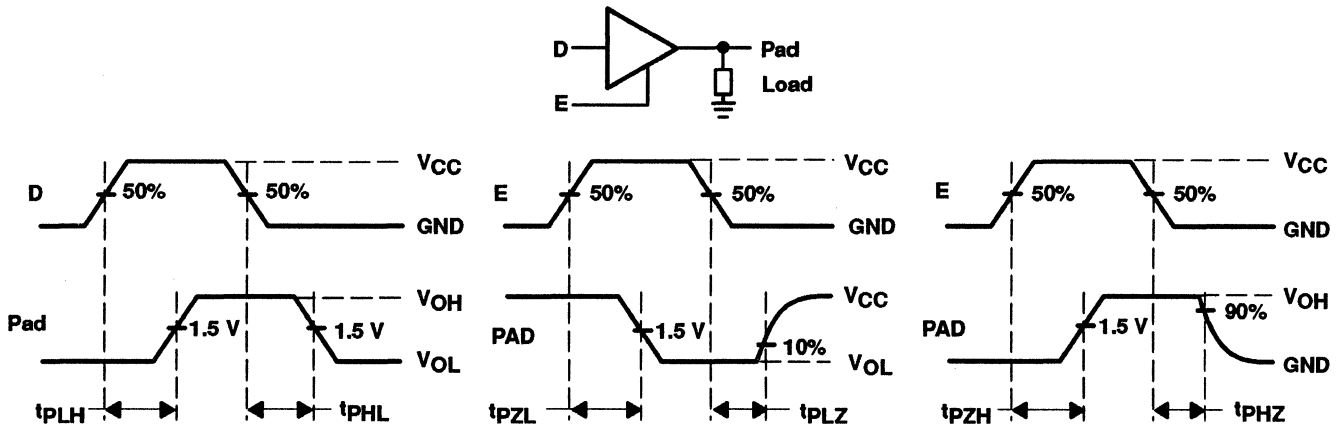
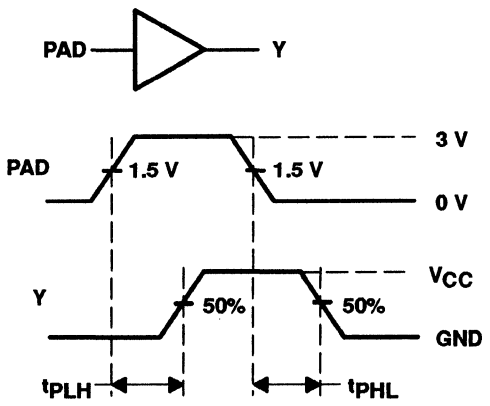


Figure 5. Symbols, Test Loads, and Waveforms

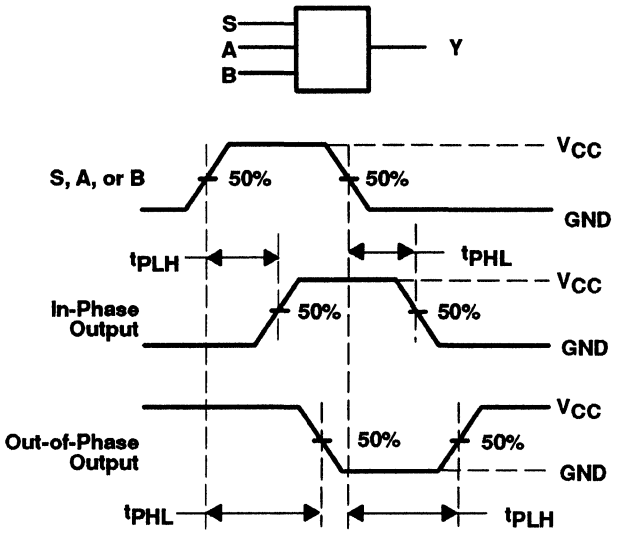
PARAMETER MEASUREMENT INFORMATION

Input buffer delays

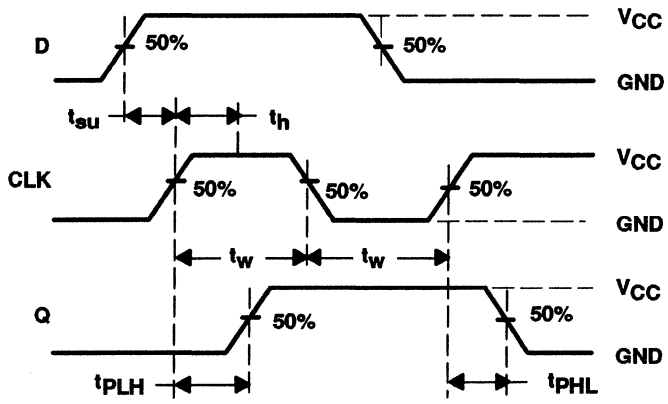


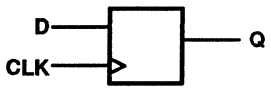
NOTE: Measurements made with $t_r = t_f = 3$ ns to pads only.

module delays



D-type flip-flop and clock delays





D FLIP-FLOP SHOWING POSITIVE-EDGE TRIGGERED CLOCK

Figure 5. Symbols, Test Loads, and Waveforms (continued)

power dissipation

To calculate power consumption, the total device power is broken into two components. These components are:

- Static or nonswitching power
- Active or switching power

$$P = \left[\left(I_{CC} + I_{active}\right) \times V_{CC}\right] + \left(I_{OL} \times V_{OL} \times N\right) + \left[I_{OH} \times \left(V_{CC} - V_{OH}\right) \times M\right]$$

Where:

I_{CC} = current flowing when no inputs or outputs are changing
I_{active} = current flowing due to CMOS switching
I_{OL}, I_{OH} = TTL sink/source currents
V_{OL}, V_{OH} = TTL level output voltages
N = number of outputs driving TTL loads to V_{OL}
M = number of outputs driving TTL loads to V_{OH}

An accurate determination of N and M is problematical because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

static power

Static power dissipation is typically a small component of the overall power. From the values provided in the electrical specifications, the maximum static power (commercial) dissipation is:

$$\text{Static power} = 10\ \text{mA} \times 5.25\ \text{V} = 52.5\ \text{mW}$$

The static power dissipated by TTL loads depends on the number of outputs that drive high or low and the DC lead current flowing. Again, this number is typically small. For instance, a 32-bit bus driving TTL loads will generate 42 mW with all outputs driving low or 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

active power

The active power component in CMOS devices is frequency dependent and depends on the user's logic and the external I/O. Active power dissipation results from charging internal chip capacitance such as that associated with the interconnect, unprogrammed antifuses, module inputs, and module outputs plus external capacitance due to PC board traces and load device inputs. An additional component of active power dissipation is due to totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

equivalent capacitance

The active power dissipated by a CMOS circuit can be expressed by Equation 1.

$$\text{Active power } (\mu W) = C_{EQ} \times V_{CC}^{\ 2} \times f \qquad (1)$$

Where:

C_{EQ} = equivalent capacitance in pF
V_{CC} = power supply voltage in volts
f = switching frequency in MHz

equivalent capacitance (continued)

Equivalent capacitance is calculated by measuring I_{active} at a specified frequency and voltage for each circuit component of interest. The results for TPC12 devices are:

	C_{EQ} (pF)
Modules	7.7
Input buffers	18.0
Output buffers	25.0
Clock buffer loads	2.5

To calculate the average active power that is dissipated from the complete design, you must solve Equation 1 for each component. In order to do this, you must know the switching frequency of each part of the logic circuit. The exact equation is piece-wise linear summation over all components, as shown in Equation 2.

$$\text{Active power} = \left[\left(n \times 7.7 \times f_1\right) + \left(m \times 18.0 \times f_2\right) + \left(p \times \left(25.0 + C_L\right) \times f_3\right) + \left(q \times 2.5 \times f\right)\right] \times V_{CC}{}^2 \qquad (2)$$

Where:

n = number of logic modules switching at frequency f_1
m = number of input buffers switching at frequency f_2
p = number of output buffers switching at frequency f_3
q = number of clock loads on the global clock network
f = frequency of global clock
f_1 = average logic module switching rate in MHz
f_2 = average input buffer switching rate in MHz
f_3 = average output buffer switching rate in MHz
C_L = output load capacitance

determining average switching frequency

In order to determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following rules will help you to determine average switching frequency in logic circuits. These rules are meant to represent worst case scenarios so that they can be generally used for predicting the upper limits of power dissipation. These rules are as follows:

Module utilization = 80% of combinatorial modules
Average module frequency = f/10
1/3 of I/Os are inputs
Average input frequency = f/5
2/3 of I/Os are outputs
Average output frequency = f/10
Clock Net 1 loading = 40% of sequential modules
Clock Net 1 frequency = f
Clock Net 2 loading = 40% of sequential modules
Clock Net 2 frequency = f/2

estimated power

The results of estimating active power based on the preceeding rules are displayed in Figure 6. The graphs provide a simple guideline for estimating power. The tables may be interpolated when your application has different resource utilizations or frequencies.

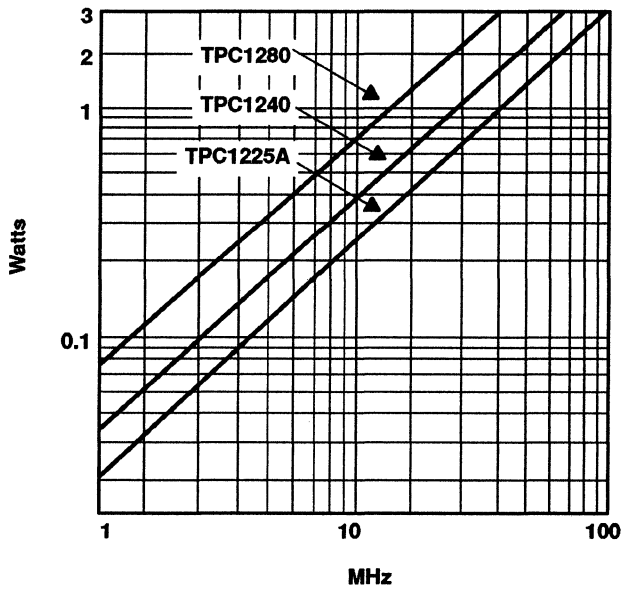


Figure 6. TPC12 Series Power Estimates

ESD rating

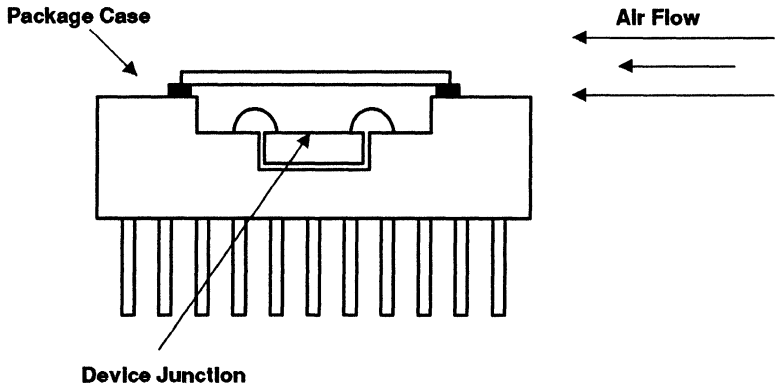
ESD characterization of Texas Instruments FPGAs is performed in accordance with MIL-STD 883C, Method 3015. This calls out the human body model which included discharging a 10-pF capacitor through a 1.5-kΩ resistor. Three positive and three negative pulses are discharged into each pin at each voltage level. After pulsing, the units are tested on a VLSI tester. Testing is performed for initial device qualification and product redesign only. All devices have been designed for ESD protection.

package thermal characteristics

The device junction to case thermal characteristic is $R_{\theta JC}$ and the junction to ambient air characteristic is $R_{\theta JA}$. The thermal characteristics for $R_{\theta JA}$ are shown with two different air-flow rates. Maximum junction temperature is 150°C. However, a maximum junction temperature of 140°C is recommended for continuous operation. A sample calculation of the maximum power dissipation for a CPGA 176-pin package at commercial temperature in still air is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. commercial temp. (°C)}}{R_{\theta JA}\ (°C/W)} = \frac{150°C - 70°C}{20°C/W} = 4\ W$$

PACKAGE TYPE	PIN COUNT	$R_{\theta JC}$	$R_{\theta JA}$ STILL AIR	$R_{\theta JA}$ 300 FT/MIN	UNIT
Ceramic Pin Grid Array (CPGA)	133 160 176 / 177	5 7 2	30 35 20	15 28 8	°C/W
Plastic Quad Flat Package (PQFP)	100 144	10 7	60 35	38 28	°C/W
Plastic Leaded Chip Carrier (PLCC)	84	10	40	27	°C/W



TPC1225A device availability and resources

Commercial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
84-pin PLCC	451	2500	72	P	P
100-pin PQFP			83	P	P

Industrial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
100-pin PQFP	451	2500	83	P	P

R = released
P = planned, consult your local TI sales representative for current availability.

TPC1240 device availability and resources

Commercial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
133-pin CPGA	684	4000	92	R	P
144-pin PQFP			104	R	P

Industrial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
133-pin CPGA	684	4000	92	R	P
144-pin PQFP			104	P	P

Military

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
133-pin CPGA	684	4000	92	P	P

R = released
P = planned, consult your local TI sales representative for current availability.

TPC1280 device availability and resources

Commercial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
160-pin PQFP	1232	8000	140	P	P
176-pin CPGA				R	R
177-pin CPGA				R	R

Industrial

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
176-pin CPGA	1232	8000	140	R	R
177-pin CPGA				R	R

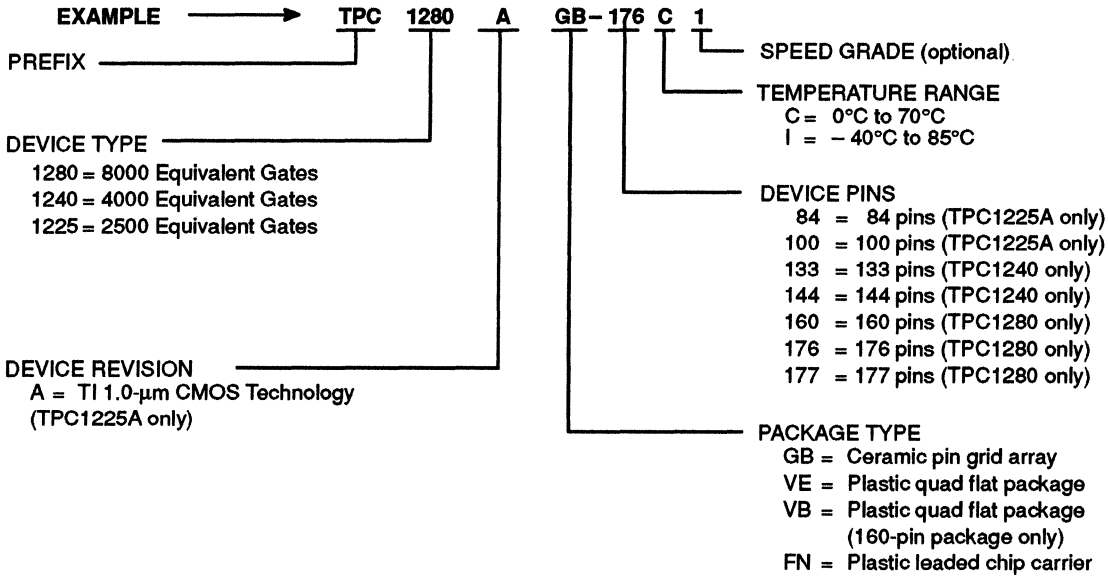
Military

PACKAGE TYPE	LOGIC MODULES	GATES	USER I/Os	SPEED GRADE	
				STD	–1
172-pin CQFP	1232	8000	140	P	P
177-pin CPGA				R	P

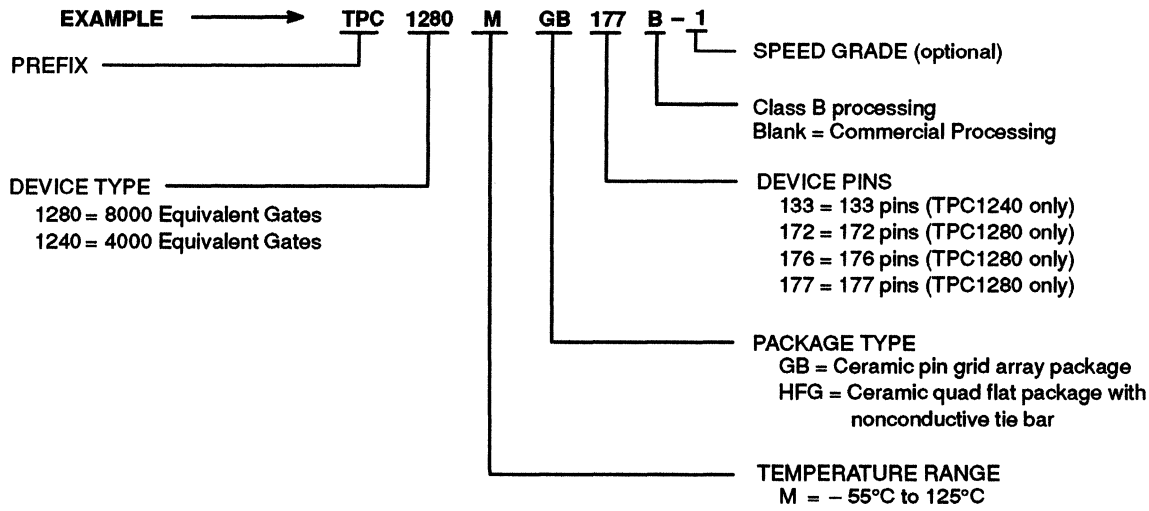
R = released
P = planned, consult your local TI sales representative for current availability.

ordering information

Various configurations of the TPC12 Series devices can be orderd using the part numbers in the examples below. Commercial and industrial versions can be ordered as follows:



Military versions can be ordered as follows:



DEFENSE ELECTRONIC SYSTEM CENTER (DESC) NUMBER

DEVICE NAME	AVAILABLE PROCESSING	DESC NUMBER
TPC1240M	Class B	To be determined
TPC1280M	Class B	5962-9215601M

MACRO LIBRARY

overview

This section describes TPC12 Series macros, which are building blocks for designing with TI field programmable gate arrays (FPGAs) with the Texas Instruments Action Logic System (TI-ALS) and your Computer Aided Engineering (CAE) interface.

The macros are divided into five categories: I/O macros, combinable hard marcos, uncombinable hard macros, soft macros, and TTL macros.

equation statement elements

combinational elements

All equations for combinational logic elements use the following operators:

OPERATOR	SYMBOL
AND	See Note 11
NOT	!
OR	+
XOR	^

NOTES: 11. A space between the 'A' and 'B' in the equation Y = A B means A AND B.
12. Order of operators in decreasing precedence is: NOT, AND, XOR and OR,
13. Signals expressed in bold have a dual module delay.

sequential elements

All equations for sequential logic elements use the following formula:

Q = <!> (<!> CLK or G, <data equation>, <!> CLR, <!> PRE)

<!>	optional inversion
CLK	flip-flop clock pin
G	latch gate pin
CLR	asynchronous clear pin
PRE	asynchronous preset pin

I/O hard macros

MACRO NAME	NO. OF MODULE(S)		DESCRIPTION
	I/O	CLOCK	
INBUF	1		Input
IBDL	1		Input with input latch
BBDLHS	1		Bidirectional with input latch and output latch
BBHS	1		Bidirectional
BIBUF	1		Bidirectional
CLKBIBUF	1	1	Bidirectional with input dedicated to clock network
CLKBUF	1	1	Input for dedicated clock network
OBDLHS	1		Output with output latch
OBHS	1		Output
OUTBUF	1		Output
TBDLHS	1		3-state output with latch
TBHS	1		3-state output
TRIBUFF	1		3-state output

I/O firm macros

MACRO NAME	I/O	DESCRIPTION
ORH	I	Output with register
ORIH	I	Inverted output with register
ORITH	I	3-state inverted output with register
ORTH	I	3-state output with register
IR	I	Input with register

combinable hard macros

DF1, DF1B, DFC1B, DFC1D, DL1, DL1B, DLC, and DLCA

FUNCTION	DESCRIPTION	MACRO NAME	EQUATION(S)	NO. OF MODULE(S)	
				SEQUENTIAL	COMBINATIONAL
AND	2-input AND	AND2	Y = A B		1
		AND2A	Y = !A B		1
		AND2B	Y = !A !B		1
	3-input AND	AND3B	Y = !A !B C		1
AND-OR		AO1A	Y = ((!A) B) + C		1
		AO1D	Y = (!A !B) + C		1
AND-OR-Invert		AOI1D	Y = !((!A !B) + !C)		1
Buffers and Inverters		BUF	Y = A		1
		BUFA	Y = !(!A)		1
		INV	Y = !A		1
		INVA	Y = !A		1
Clock Net Interface		GAND2	Y = A G		1
		GNOR2	Y = !(A + G)		1
		GOR2	Y = A + G		1
Multiplexer	2:1 Multiplexers	MX2	Y = (A !S) + (B S)		1
NAND	2-input NAND	NAND2A	Y = !(!A B)		1
		NAND2B	Y = !(!A !B)		1
	3-input NAND	NAND3C	Y = !(!A !B !C)		1
NOR	2-input NOR	NOR2	Y = !(A + B)		1
		NOR2A	Y = !(!A +B)		1
		NOR2B	Y = !(!A + !B)		1
	3-input NOR	NOR3A	Y = !(!A + B + C)		1
OR-AND		OA1	Y = (A + B) C		1
OR	2-input OR	OR2	Y = A + B		1
		OR2A	Y = !A + B		1
	3-input OR	OR3	Y = A + B + C		1

combinable hard macros (continued)

DF1, DF1B, DFC1B, DFC1D, DL1, and DL1B

FUNCTION	DESCRIPTION	MACRO NAME	EQUATION(S)	NO. OF MODULE(S)	
				SEQUENTIAL	COMBINATIONAL
AND	3-input	AND3	Y = A B C		1
		AND3A	Y = !A B C		1
		AND3C	Y = !A !B !C		1
	4-input	AND4B	Y = !A !B C D		1
		AND4C	Y = !A !B !C D		1
AND-OR		AO1	Y = (A B) + C		1
		AO11	Y = AB + ((A + B) C)		1
		AO1B	Y = (A B) + (!C)		1
		AO1C	Y = ((!A) B) + (!C)		1
		AO1E	Y = (!A!B) + !C		1
		AO2	Y = ((A B) + C + D)		1
		AO2A	Y = ((!A B) + C + D)		1
		AO2B	Y = (!A!B) + C + D		1
		AO2C	Y = (!AB) + !C + D		1
		AO2D	Y = (!A!B) + !C + D		1
		AO3	Y = (!A B C) + D		1
		AO3B	Y = (!A!BC) + D		1
		AO3C	Y = (!A!B!C) + D		1
		AO4A	Y = (!A B C) + (A C D)		1
		AO5A	Y = (!A B) + (A C) + D)		1
AND-OR-Invert		AOI1A	Y = !((!A B) + C)		1
		AOI1B	Y = !((A B) + !C)		1
		AOI1C	Y = !((!A !B) + C)		1
		AOI2A	Y = !((!A B) + C + D)		1
		AOI3A	Y = !((!A !B !C) + (!A !D))		1
Exclusive OR	AND-XOR	AX1B	Y = (!A !B) ^ C		1
Boolean		CS2	Y = !((A + S) B) C + ((A + S) B) D		1
		CY2B	Y = A1 B1 + (A0+B0) A1 + (A0+B0) B1		1
Clock Net Interface		GMX4	Y = (D0 !S0 !G) + (D1 !G S0) + (D2 G !S0) + (D3 S0 G)		1
		GNAND2	Y = !(A G)		1
		GXOR2	Y = A ^ G		1
AND-OR		MAJ3	Y = (A B) + (B C) + (A C)		1
Multiplexer	2:1 Multiplexers	MX2A	Y = (!A !S) + (B S)		1
		MX2B	Y = (A !S) + (!B S)		1
		MX2C	Y = (!A !S) + (!B S)		1
	4:1 Multiplexers	MX4	Y = (D0 !S0 !S1) + (D1 S0 !S1) + (D2 !S0 S1) + (D3 S0 S1)		1

combinable hard macros (continued)

DF1, DF1B, DFC1B, DFC1D, DL1, and DL1B (continued)

FUNCTION	DESCRIPTION	MACRO NAME	EQUATION(S)	NO. OF MODULE(S)	
				SEQUENTIAL	COMBINATIONAL
NAND	2-input NAND	NAND2	Y = !(A B)		1
	3-input NAND	NAND3A	Y = !(!A B C)		1
		NAND3B	Y = !(!A !BC)		1
	4-input NAND	NAND4C	Y = !(!A !B C D)		1
		NAND4D	Y = !(!A !B !C !D)		1
NOR	3-input NOR	NOR3	Y = !(A + B + C)		1
		NOR3B	Y = !(!A + !B + C)		1
		NOR3C	Y = !(!A + !B + !C)		1
	4-input NOR	NOR4A	Y = !(!A + B + C + D)		1
		NOR4B	Y = !(!A + !B + C + D)		1
OR-AND		OA1A	Y = (!A + B) C		1
		OA1B	Y = (A + B) (!C)		1
		OA1C	Y = (!A + B) (!C)		1
		OA2	Y = (A + B) (C + D)		1
		OA2A	Y = (!A + B) (C + D)		1
		OA3	Y = ((A + B) C D)		1
		OA3A	Y = ((A + B) !C D)		1
		OA4	Y = (A + B + C) D		1
		OA4A	Y = ((A + B + !C) D)		1
		OA5	Y = (A + B + C) (A + D)		1
OR-AND-Invert		OAI1	Y = !((A + B) C)		1
		OAI2A	Y = !((A + B + C) !D)		1
		OAI3A	Y = !((A + B) !C !D)		1
OR	3-input OR	OR3A	Y = !A + B + C		1
		OR3B	Y = !A + !B + C		1
	4-input OR	OR4	Y = A + B + C + D		1
		OR4A	Y = !A + B + C + D		1
Exclusive OR	XOR, XOR-OR	XOR	Y = A ^ B		1
		XO1	Y = (A ^ B) + C		1
		XO1A	Y = !(A ^ B) + C		1
	XNOR, XOR-AND	XNOR	Y = !(A ^ B)		1
		XA1	Y = (A ^ B) C		1
		XA1A	Y = !(A ^ B) C		1

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

non-combinable hard macros

FUNCTION	DESCRIPTION	MACRO NAME	EQUATION(S)	NO. OF MODULE(S)	
				SEQUENTIAL	COMBINATIONAL
AND	4-input AND	AND4	Y = A B C D		1
		AND4A	Y = (!A B C D)		1
		AND4D	Y = **!A !B** !C !D		2
	5-input AND	AND5B	Y = !A !B C D E		1
OR	2-input OR	OR2B	Y = !A + !B		1
	3-input OR	OR3C	Y = !A + !B + !C		1
	4-input OR	OR4B	Y = !A + !B + C + D		1
		OR4C	Y = !A + !B + !C + D		1
		OR4D	Y = **!A** + **!B** + !C + !D		2
	5-input OR	OR5B	Y = !A + !B + C + D + E		1
NAND	3-input NAND	NAND3	Y = !(A B C)		1
	4-input NAND	NAND4	Y = !(**A B** C D)		2
		NAND4A	Y = !(!A B C D)		1
		NAND4B	Y = !(!A !B C D)		1
	5-input NAND	NAND5C	Y = !(!A !B !C D E)		1
NOR	4-input NOR	NOR4	Y = !(**A** + **B** + C + D)		2
		NOR4C	Y = !(!A + !B + !C + D)		1
		NOR4D	Y = !(!A + !B + !C + !D)		1
	5-input NOR	NOR5C	Y = !(!A + !B + !C + D + E)		1
Exclusive OR	AND-XOR	AX1	Y = (!A B) ^ C		1
		AX1A	Y = !(!A B) ^ C		2
		AX1C	Y = (A B) ^ C		1
AND-OR		AO10	Y = ((AB) + C) (D + E)		1
		AO2E	Y = (!A!B) + !C + !D		1
		AO3A	Y = (A B C) + D		1
		AO6	Y = A B + C D		1
		AO6A	Y = A B + C !D		1
		AO7	Y = A B C + D + E		1
		AO8	Y = (AB) + (!C!D) + E		1
		AO9	Y = (AB) + C + D + E		1
AND-OR-Invert		AOI1	Y = !(A B + C)		1
		AOI2B	Y = !((!A B) + !C + D)		1
		AOI4	Y = !((A B) + (**C D**))		2
		AOI4A	Y = !(A B + !C D)		1
OR-AND		OA3B	Y = ((!A + B) !C D)		1
OR-AND-Invert		OAI3	Y = !((A + B) C D)		1

non-combinable hard macros (continued)

FUNCTION	DESCRIPTION	MACRO NAME	EQUATION(S)	NO. OF MODULE(S)	
				SEQUENTIAL	COMBINATIONAL
Adders	Half adders	HA1	CO = A B S = A ^ B		2
		HA1A	CO = !A B S = !(A ^ B)		2
		HA1B	CO = !(A B) S = !(A ^ B)		2
		HA1C	CO = !(A B) S = (A ^B)		2
	Full adders	FA1A	CO = (CI !B !A) + (A !B) + (B CI A) S = (B !A !CI) + (CO !A CI) + (CO A !CI) + (B A CI)		2
		FA1B	CO = !A(!B + B CI) + A(!B CI) S = !A(!CI CO + CI B) + A(!CI B + CI CO)		2
		FA2A	CO = (CI !B !(A0+A1)) + (!B (A0+A1)) + (B CI (A0+A1)) S = (B !(A0+A1) !CI) + (CO !(A0+A1) CI) + (CO(A0+A1) !CI) + (B(A0+A1)CI)		2
Boolean		CS1	Y = !(A + S B) C + D (A + S B)		1
		CY2A	Y = A1 B1 + A0 B0 A1 + A0 B0 B1		1
Flip-Flops	D-type	DF1	Q = (CLK, D, –, –)	1	
		DF1A	QN = !(CLK, D, –, –)	1	
		DF1B	Q = (!CLK, D, –, –)	1	
		DF1C	QN = !(!CLK, D, –, –)	1	
	D-type with clear	DFC1	Q = (CLK, D, CLR, –)	1	1
		DFC1A	Q = (!CLK, D, CLR, –)	1	1
		DFC1B	Q = (CLK, D, !CLR, –)	1	
		DFC1D	Q = (!CLK, D, !CLR, –)	1	
		DFC1E	QN = !(CLK, D, !CLR, –)	2	1
		DFC1G	QN = !(!CLK, D, !CLR, –)		2
	D-type with enable	DFE	Q = (CLK, !E Q + E D, –, –)	1	
		DFE1B	Q = (CLK, !E D + E Q, –, –)	1	
		DFE1C	Q = (!CLK, D !E + Q E, –, –)	1	
		DFE3A	Q = (CLK, D E + Q !E, !CLR, –)	1	
		DFE3B	Q = (!CLK, D E + Q !E, !CLR, –)	1	
		DFE3C	Q = (CLK, D !E + Q E, !CLR, –)	1	
		DFE3D	Q = (!CLK, D !E + Q E, !CLR, –)	1	
		DFEA	Q = (!CLK, !E Q + E D, –, –)	1	1
Multiplexers	Logic module	CM8	Y = (D0 !(S00 S01) + D1(S00 S01)) !(S10 + S11) + (D2 !(S00 S01) + D3(S00 S01)) (S10 + S11)		1
		MXT	Y = (!S1 (!S0A D0) + (S0A D1)) + (S1 (!S0B D2 + S0B D3))		2
		MXC1	Y = !(!S A + S B) C + (!S A + S B) D		2

non-combinable hard macros (continued)

FUNCTION	DESCRIPTION	MACRO NAME	EQUATION(S)	NO. OF MODULE(S)	
				SEQUENTIAL	COMBINATIONAL
Flip-Flops (continued)	D-type with multiplexed data	DFM	Q = (CLK, A !S + B S, –, –)	1	
		DFM1B	QN = !(CLK, A !S + B S, –, –)	1	
		DFM1C	QN = !(!CLK, A !S + B S, –, –)	1	
		DFM3	Q = (CLK, A !S + B S, CLR, –)	1	1
		DFM3B	Q = (!CLK, A !S + B S, !CLR, –)	1	
		DFM3E	Q = (!CLK, A !S + B S, CLR, –)	1	1
		DFM4C	QN = !(!CLK, !A !S + !B S, –, !PRE)	1	
		DFM4D	QN = !(!CLK, A !S + B S, –, !PRE)	1	
		DFM6A	Q = (CLK, (D0 !S0 !S1 + D1 S0 !S1 + D2 !S0 S1 + D3 S0 S1), !CLR, –)	1	
		DFM6B	Q = (!CLK, (D0 !S0 !S1 + D1 S0 !S1 + D2 !S0 S1 + D3 S0 S1), !CLR, –)	1	
		DFM7A	Q = (CLK, (0 !S0 + D1 S0) !(S10 + S11) + (D2 !S0 + D3 S0) (S10 + S11), !CLR, –)	1	
		DFM7B	Q = (!CLK, (D0 !S0 + D1 S0) !(S10 + S11) + (D2 !S0 +D3 S0) (S10 + S11), !CLR, –)	1	
		DFMA	Q = (!CLK, A !S + B S, –, –)	1	
		DFMB	Q = (CLK, A !S + B S, !CLR, –)	1	
		DFME1A	Q = (CLK, !E A !S + !E B S + E Q, –, –)	1	
	D-type flip-flops with preset	DFP1	Q = (CLK, D, –, PRE)		2
		DFP1A	Q = (!CLK, D, –, PRE)		2
		DFP1B	Q = (CLK, D, –, !PRE)		2
		DFP1C	QN = !(CLK, D, –, PRE)	1	1
		DFP1D	Q = (!CLK, D, –, !PRE)		2
		DFP1E	QN = !(CLK, D, –, !PRE)	1	
		DFP1F	Q = (!CLK, D, –, PRE)	1	1
		DFP1G	QN = !(!CLK, D, –, !PRE)		1
	D-type flip-flops w/ clear and preset	DFPC	Q = (CLK, D, CLR, PRE)		2
		DFPCA	Q = (!CLK, D, !CLR, PRE)		2
	J-$\overline{K}$ flip-flops	JKF	Q = (CLK, !Q J + Q K, –, –)	1	
		JKF1B	Q = (!CLK, !Q J + Q K, –, –)	1	
		JKF2A	Q = (CLK, !Q J + Q K, !CLR, –)	1	
		JKF2B	Q = (!CLK, !Q J + Q K, !CLR, –)	1	
		JKF2C	Q = (CLK, !Q J + Q K, CLR, –)	1	1
		JKF2D	Q = (!CLK, !Q J + Q K, CLR, –)	1	1
	Toggle flip-flops	TF1A	Q = (CLK, T !Q + !T Q, !CLR, –)	1	
		TF1B	Q = (!CLK, T !Q + !T Q, !CLR, –)	1	

non-combinable hard macros (continued)

FUNCTION	DESCRIPTION	MACRO NAME	EQUATION(S)	NO. OF MODULE(S)	
				SEQUENTIAL	COMBINATIONAL
Data Latch	D-type latch	DL1	Q = (G, D, –, –)	1	
		DL1A	QN = !(G, D, –, –)	1	
		DL1B	Q = !(!G, D, –, –)	1	
		DL1C	QN = !(!G, D, –, –)	1	
	With clear	DLC	Q = (G, D, !CLR, –)	1	
		DLC1	Q = (G, D, CLR, –)		1
		DLC1A	Q = (!G, D, CLR, –)		1
		DLC1F	QN = !(G, D, CLR, –)		1
		DLC1G	QN = !(!G, D, CLR, –)		1
		DLCA	Q = (!G, D, !CLR, –)	1	
	With enable	DLE	Q = (G, Q !E + D E, –, –)	1	
		DLE1D	QN = !(!G, !E !D + E QN, –, –)	1	
		DLE2B	Q = (!G, D !E + Q E, !CLR, –)	1	
		DLE2C	Q = (!G, !E D + Q E, CLR, –)		1
		DLE3B	Q = (!G, !E D + Q E, –, PRE)		1
		DLE3C	Q = (!G, !E D + Q E, –, !PRE)		1
		DLEA	Q = (G, Q E + D !E, –, –)	1	
		DLEB	Q = (!G, Q !E + D E, –, –)	1	
		DLEC	Q = (!G, Q E + D !E, –, –)	1	
	With multiplexed data	DLM	Q = (G, A !S + B S, –, –)	1	
		DLM3	Q = (G, D0 !S0 !S1 + D1 S0 !S1 + D2 !S0 S1 + D3 S0 S1, –, –)	1	
		DLM3A	Q = (!G, D0 !S0 !S1 + D1 S0 !S1 + D2 !S0 S1 + D3 S0 S1, –, –)	1	
		DLM4	Q = (G, (D0 !S0 + D1 S0) !(S10 + S11) + (D2 !S0 + D3 S0) (S10 + S11), –, –)	1	
		DLM4A	Q = (!G, (D0 !S0 + D1 S0) !(S10 + S11) + (D2 !(S0 + D3 S0) (S10 + S11), –, –)	1	
		DLMA	Q = (!G, A !S + B S, –, –)	1	
	With multiplexed data and enable	DLME1A	Q = (!G, A !S !E + B S !E + E Q, –, –)	1	
	With preset	DLP1	Q = (G, D, –, PRE)		1
		DLP1A	Q = (!G, D, –, PRE)		1
		DLP1B	Q = (G, D, –, !PRE)		1
		DLP1C	Q = (!G, D, –, !PRE)		1
		DLP1D	QN = !(G, D, –, !PRE)	1	
		DLP1E	QN = !(!G, D, –, !PRE)	1	
Clock Net Interface		CLKINT		clock modules = 1	
Tie-Off		V_{CC}		modules = 0	
		GND		modules = 0	

soft macros

FUNCTION	DESCRIPTION	MACRO NAME	LOGIC LEVELS	NO. OF MODULE(S)	
				SEQUENTIAL	COMBINATIONAL
Counters	4-bit binary counter with load, clear	CNT4A	4	4	8
	4-bit binary counter with load, clear, carry in, carry out	CNT4B	4	4	7
	Fast 16-bit down counter, parallel loadable	FCTD16C	2	19	33
	Fast 8-bit down counter, parallel loadable	FCTD8A	1	10	18
	Fast 8-bit down counter, parallel loadable	FCTD8B	1	9	13
	Fast 16-bit up counter, parallel loadable	FCTU16C	2	19	31
	Fast 8-bit up counter, parallel loadable	FCTU8A	1	10	17
	Fast 8-bit up counter, parallel loadable	FCTU8B	1	9	12
	4-bit up/down counter with load, carry in, and carry out	UDCNT4A	5	4	13
	Very fast 16-bit down counter, delay after load, registered control input	VCTD16C	1	34	41
	2-bit down counter, prescaler, delay after load, use to build VCTD counters	VCTD2CP	1	5	2
	2-bit down counter, upper bits, delay after load, use to build VCTD counters	VCTD2CU	1	2	3
	4-bit down counter, lower bits, delay after load, use to build VCTD counters	VCTD4CL	1	4	7
	4-bit down counter, middle bits, delay after load, use to build VCTD counters	VCTD4CM	1	4	8
Decoders	2-to-4 decoder	DEC2X4	1		4
	2-to-4 decoder with active low outputs	DEC2X4A	1		4
	3-to-8 decoder	DEC3X8	1		8
	3-to-8 decoder with active low outputs	DEC3X8A	1		8
	4-to-16 decoder with active low outputs	DEC4X16A	2		20
	2-to-4 decoder with enable	DECE2X4	1		4
	2-to-4 decoder with enable and active low outputs	DECE2X4A	1		4
	3-to-8 decoder with enable	DECE3X8	2		11
	3-to-8 decoder with enable and active low outputs	DECE3X8A	2		11
Registers	Octal latch with clear	DLC8A	1	8	
	Octal latch with enable	DLE8	1	8	
	Octal latch with multiplexed data	DLM8	1	8	
	4-bit shift register with clear	SREG4A	1	4	
	8-bit shift register with clear	SREG8A	1	8	
Adders	8-bit adder	FADD8	3		44
	9-bit adder	FADD9	3		49
	10-bit adder	FADD10	3		56
	12-bit adder	FADD12	4		69
	16-bit adder	FADD16	5		97
	Very fast 16-bit adder	VAD16C	3		97
	Very fast 16-bit adder with carry in	VADC16C	1		97

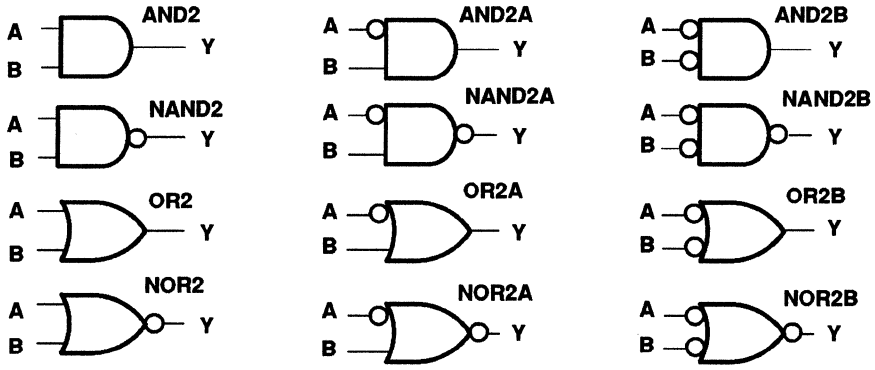
soft macros (continued)

FUNCTION	DESCRIPTION	MACRO NAME	LOGIC LEVELS	NO. OF MODULE(S)	
				SEQUENTIAL	COMBINATIONAL
Comparators	4-bit identity comparator	ICMP4	2		5
	8-bit identity comparator	ICMP8	3		9
	2-bit magnitude comparator with enable	MCMPC2	3		9
	4-bit magnitude comparator with enable	MCMPC4	4		18
	8-bit magnitude comparator with enable	MCMPC8	6		36
Multiplexer	8-to-1 multiplexer	MX8	2		3
	8-to-1 multiplexer with active low outputs	MX8A	2		3
	16-to-1 multiplexer	MX16	2		5
Multiplier	8-bit by 8-bit multiplier	SMULT8	22		242

TTL macros

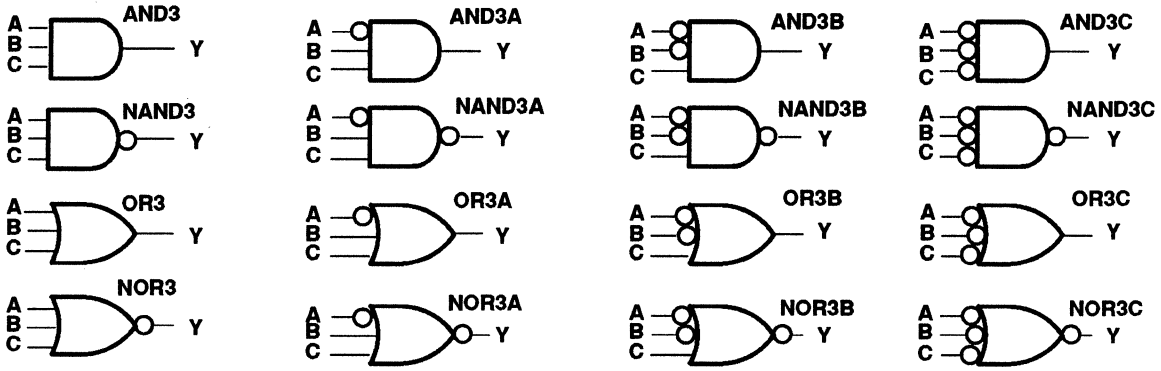
MACRO NAME	DESCRIPTION	LOGIC LEVELS	NO. OF MODULE(S)	
			SEQUENTIAL	COMBINATIONAL
TA00	2-input NAND	1		1
TA02	2-input NOR	1		1
TA04	Inverter	1		1
TA07	Buffer	1		1
TA08	2-input AND	1		1
TA10	3-input NAND	1		1
TA11	3-input AND	1		1
TA20	4-input NAND	1		2
TA21	4-input AND	1		1
TA27	3-input NOR	1		1
TA32	2-input OR	1		1
TA40	4-input NAND	1		2
TA42	4-to-10 decoder	1		10
TA51	AND-OR-Invert	1		2
TA54	4-wide, 2-input AND-OR-Invert	2		5
TA55	2-wide 4-input AND-OR-Invert	2		3
TA86	2-input exclusive OR	1		1
TA138	3-to-8 decoder with enable and active low outputs	2		12
TA139	2-to-4 decoder with enable and active low outputs	1		4
TA150	16-to-1 multiplexer with active low enable	3		6
TA151	8-to-1 multiplexer with enable and active high/low outputs	3		5
TA153	4-to-1 multiplexer	2		2
TA154	4-to-16 decoder with active low select	2		22
TA157	2-to-1 multiplexer with active low enable	1		1
TA160	4-bit decade counter with clear and load	4	4	8
TA161	4-bit binary counter with clear and load	3	4	6
TA164	8-bit serial in, parallel out shift register with clear	1	8	
TA169	4-bit up/down counter	6	4	14
TA174	Hex D-type flip-flop with clear	1	6	
TA175	Quadruple D-type flip-flop with clear	1	4	
TA190	4-bit up/down decade counter with up/down mode	7	4	31
TA191	4-bit up/down binary counter with up/down mode	7	4	30
TA194	4-bit bidirectional universal shift register	1	4	4
TA195	4-bit parallel access shift register	1	4	1
TA269	8-bit up/down binary counter	8	8	28
TA273	Octal register with clear	1	8	
TA280	Parity generator and checker	4		9
TA377	Octal register with active low enable	1	8	
TA688	8-bit identity comparator	3		9

HARD MACRO SYMBOLS



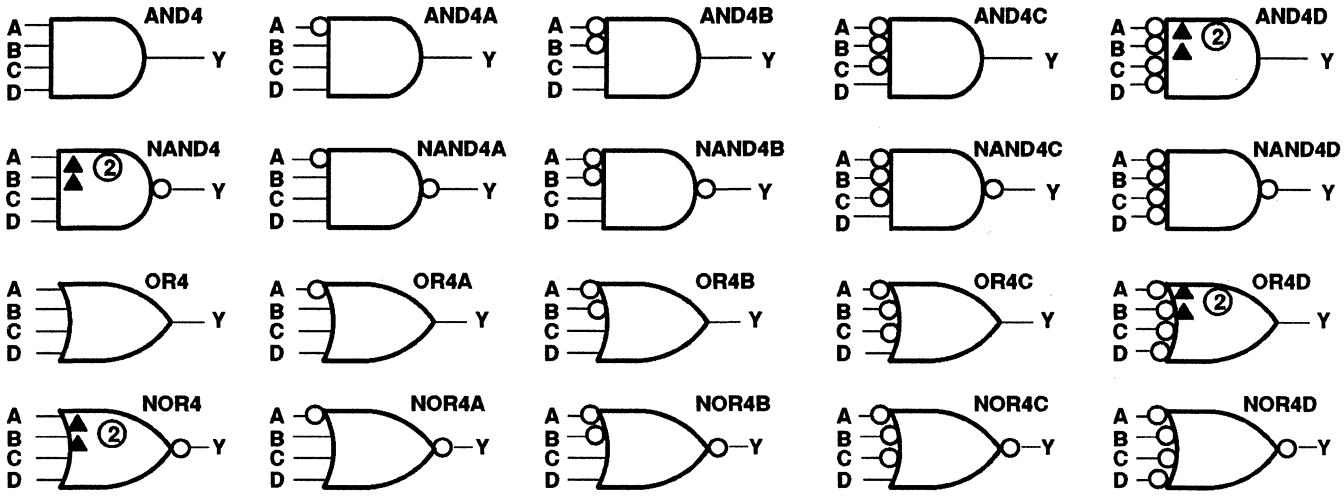
Module Count = 1

Figure 7. 2-Input Gates



Module Count = 1

Figure 8. 3-Input Gates

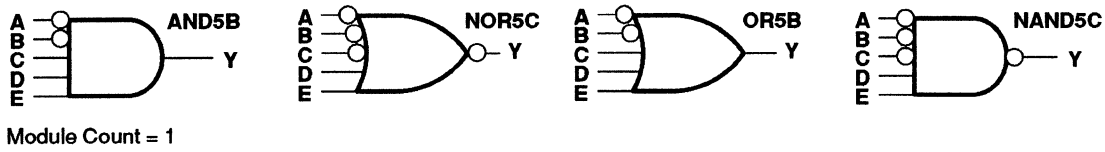


Module Count = 1 (unless otherwise noted)

② Indicates Module Count = 2 ▲ Indicates extra delay input

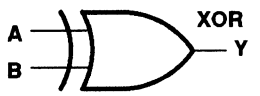
Figure 9. 4-Input Gates

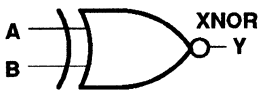
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265



Module Count = 1

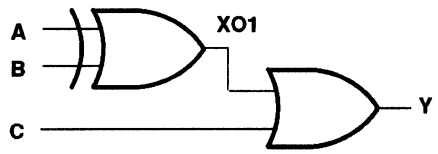
Figure 10. 5-Input Gates

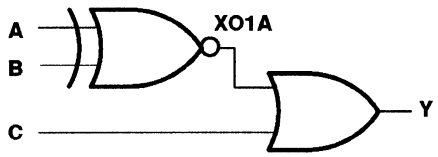




Module Count = 1

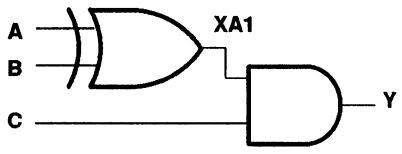
Figure 11. XOR/XNOR Gates

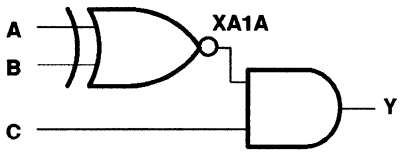




Module Count = 1

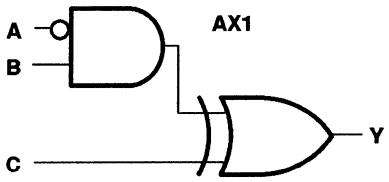
Figure 12. XOR-OR/XNOR-OR Gates



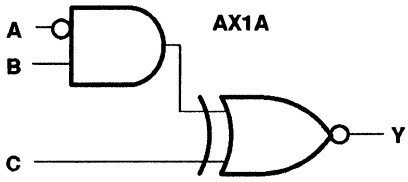


Module Count = 1

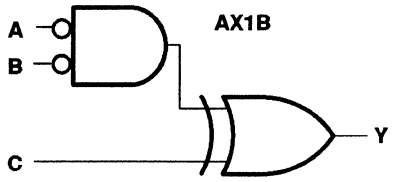
Figure 13. XOR-AND/ XNOR-AND Gates



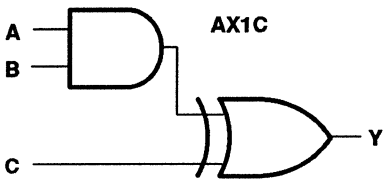
Module Count = 1



Module Count = 2

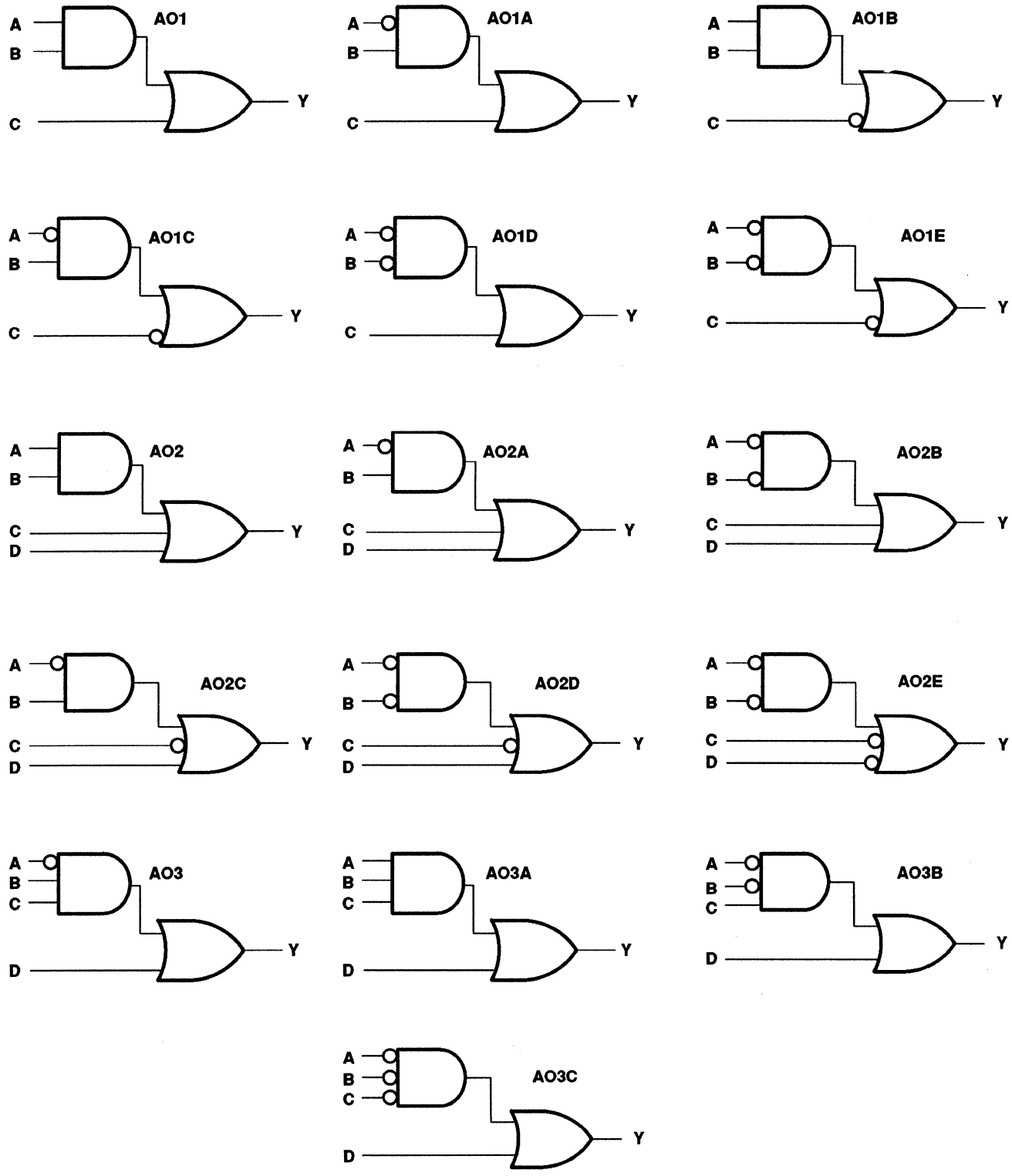


Module Count = 1



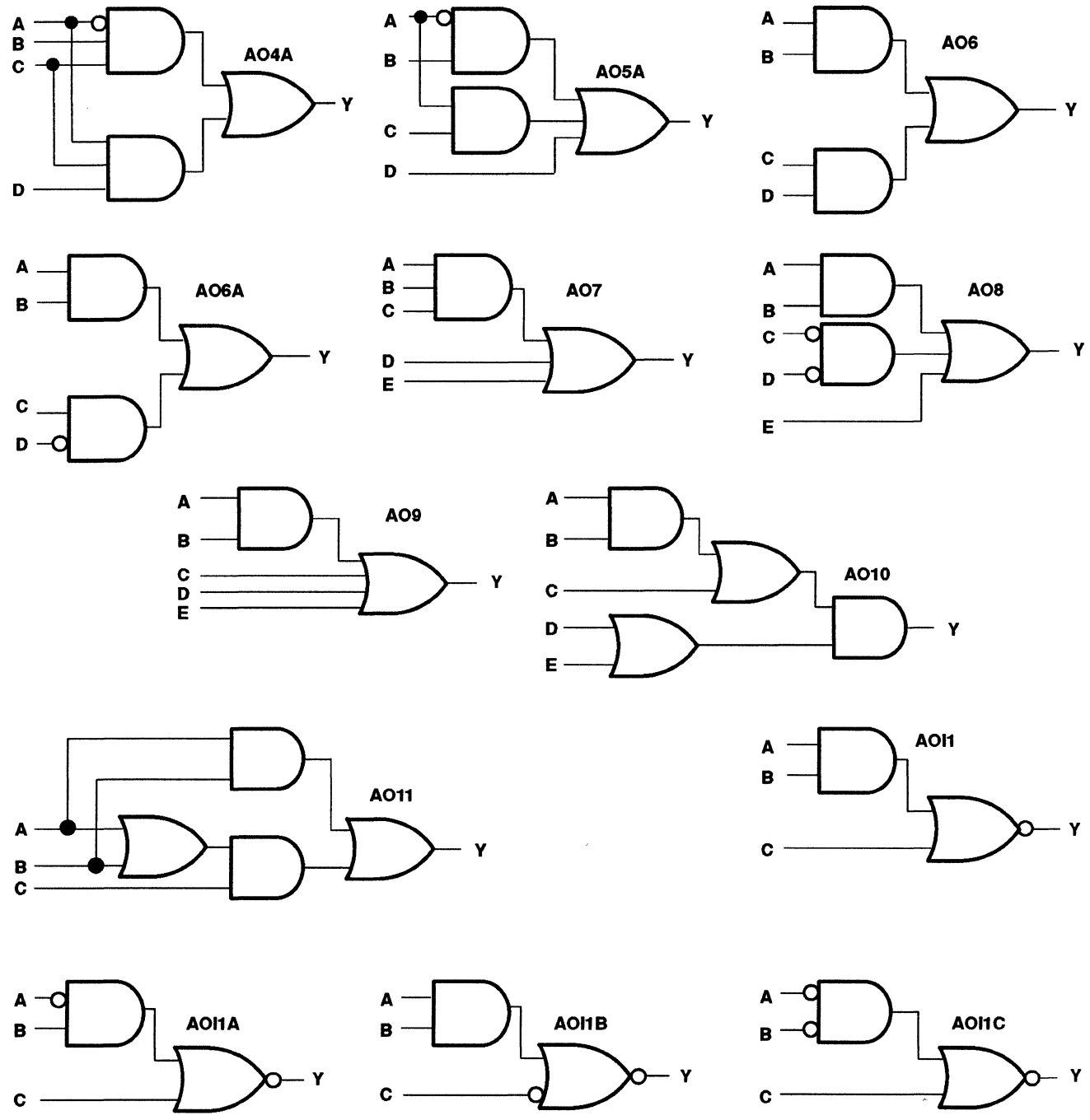
Module Count = 1

Figure 14. AND-XOR/AND-XNOR Gates



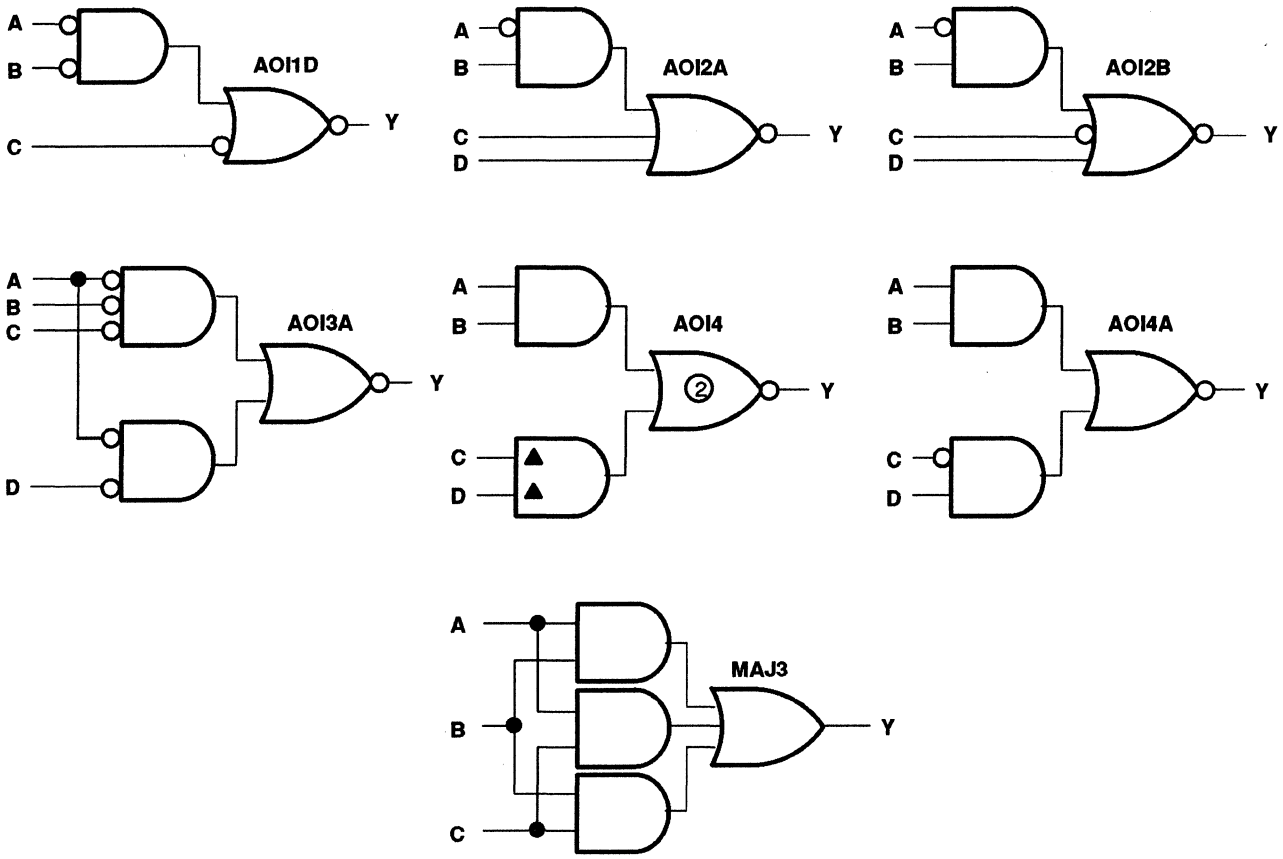
Module Count = 1

Figure 15. AND-OR/AND-NOR Gates



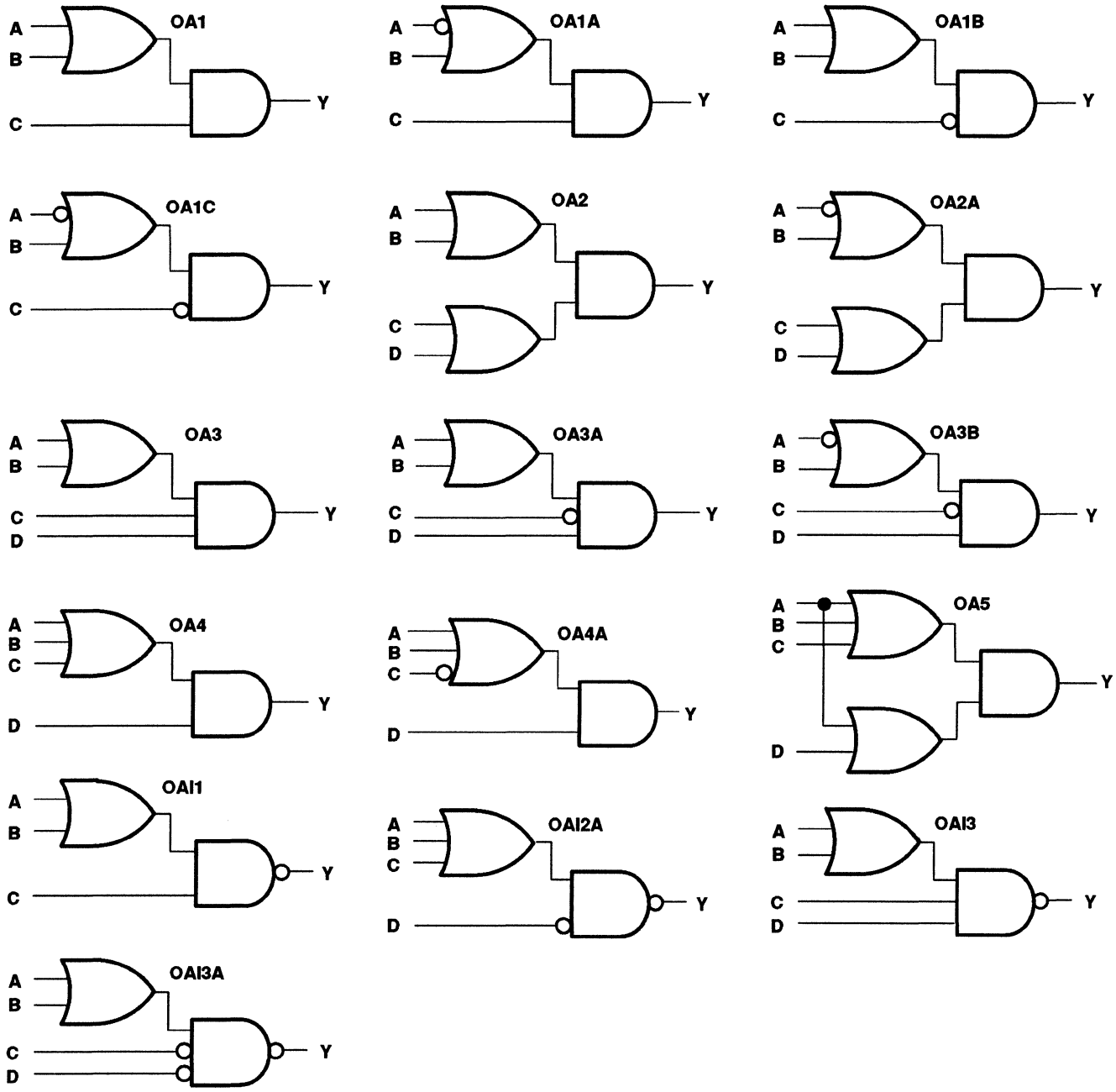
Module Count = 1

Figure 14. AND-OR/AND-NOR Gates (Continued)



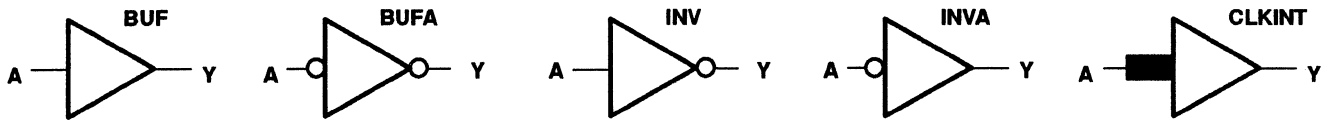
Module Count = 1 (unless otherwise noted)
② Indicates Module Count = 2
▲ Indicates extra delay input

Figure 14. AND-OR/AND-NOR Gates (Continued)



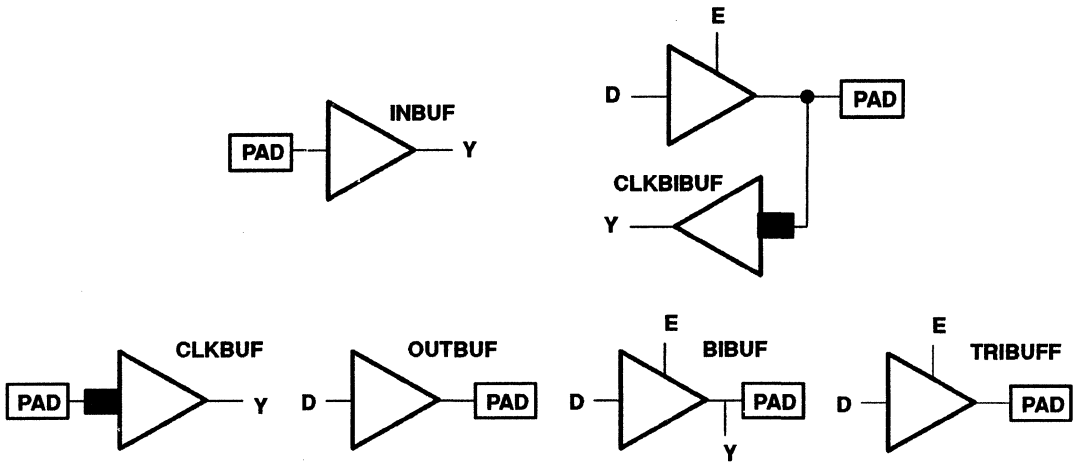
Module Count = 1

Figure 16. OR-AND/OR-NAND Gates



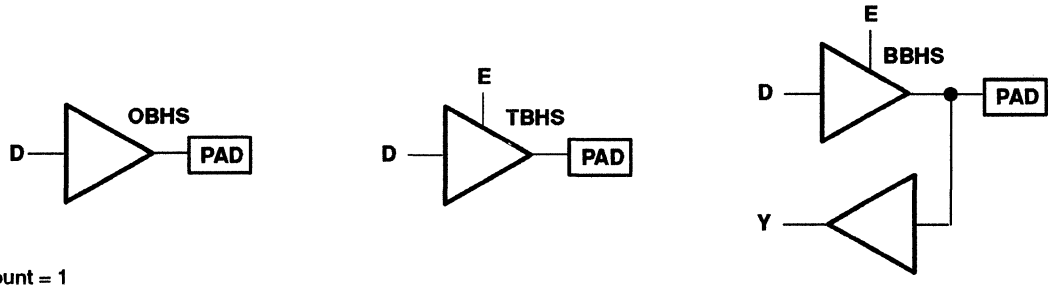
Module Count = 1

Figure 17. Buffers



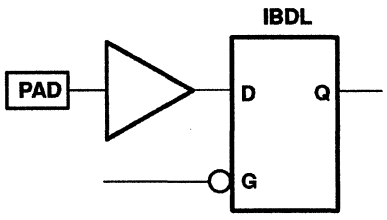
I/O Module Count = 1

Figure 18. I/O Buffers



I/O Module Count = 1

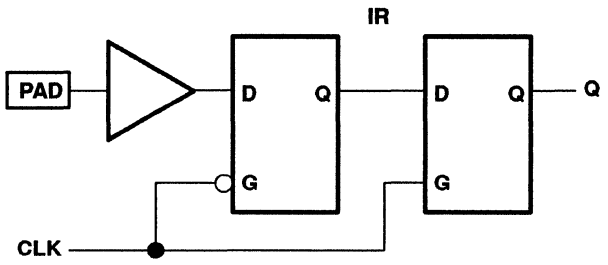
Figure 19. High-Slew Output Buffers



I/O Module Coiunt = 1

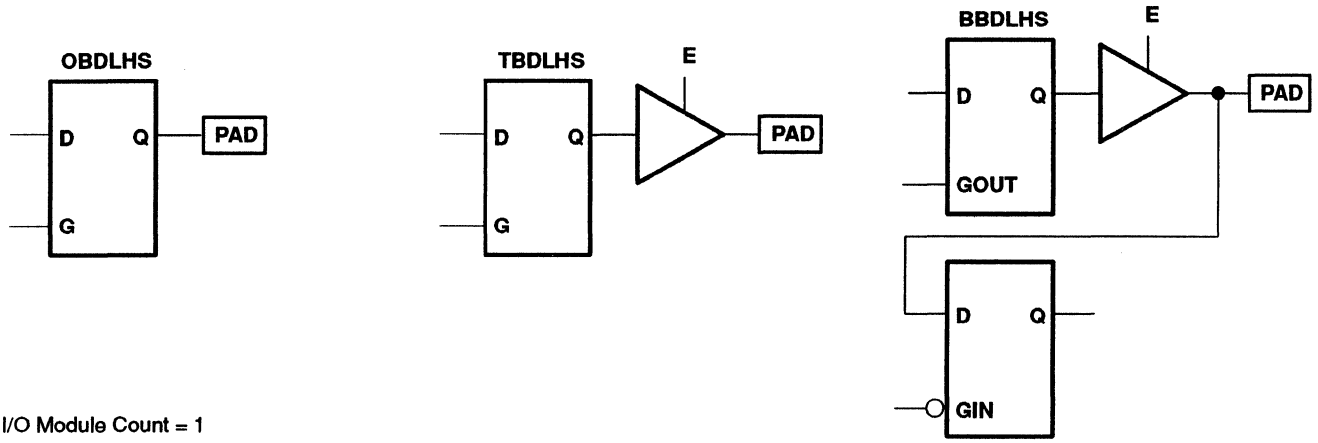
Figure 20. Input Buffer With Latch

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265



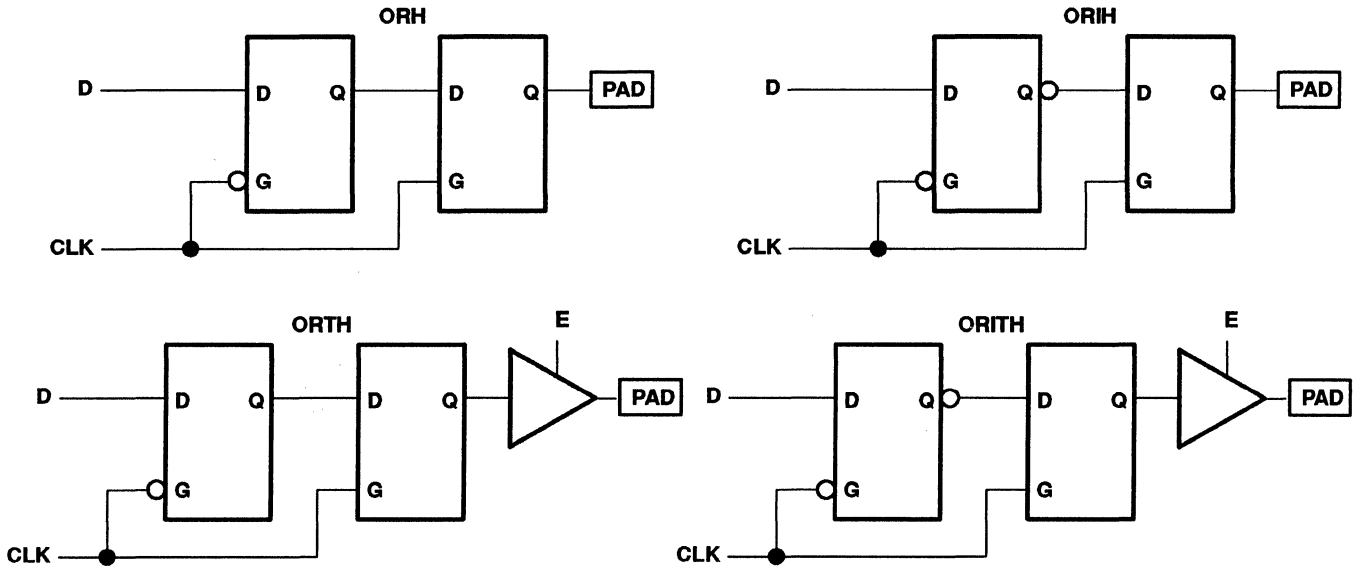
I/O Module Coiunt = 1

Figure 21. Input Buffer With Register



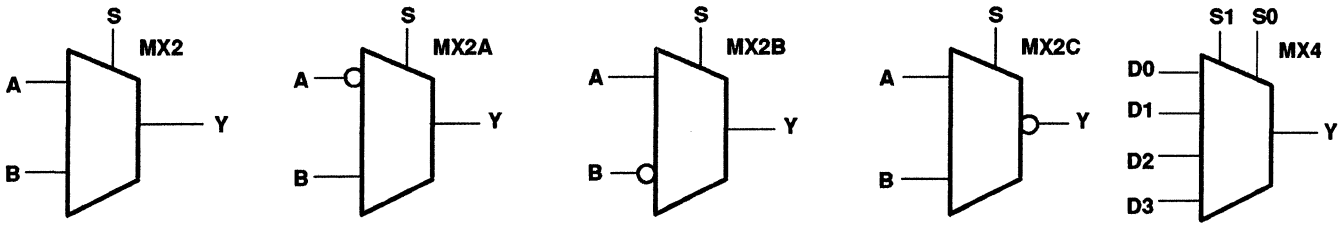
I/O Module Count = 1

Figure 22. High-Slew Output Buffers With Latches

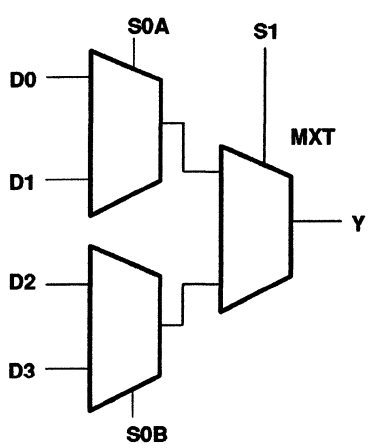


I/O Module Coiunt = 1

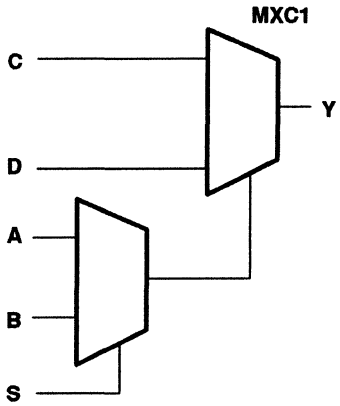
Figure 23. Output Buffers With Registers



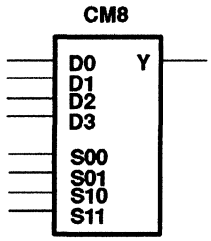
Module Count = 1



Module Count = 2

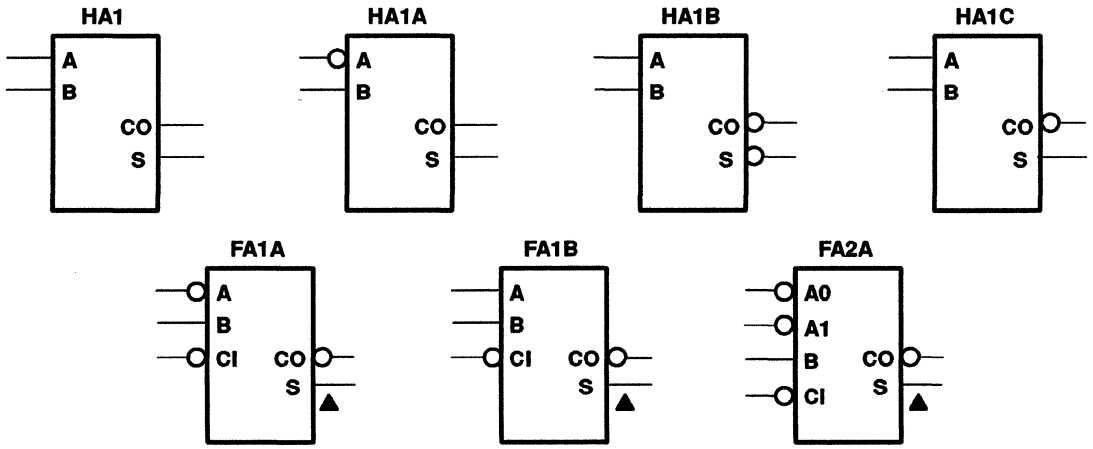


Module Count = 2



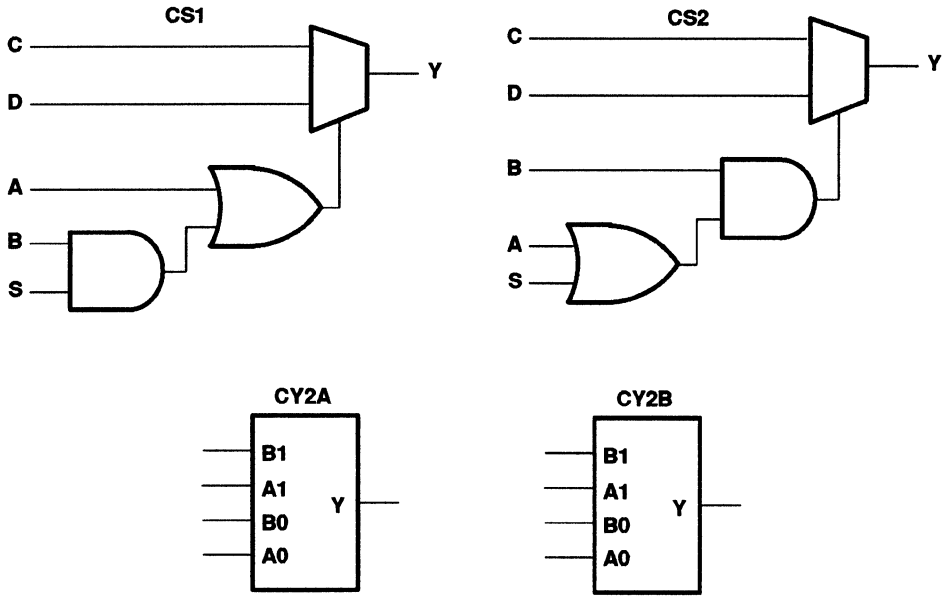
Module Count = 1

Figure 24. Multiplexers



Module Count = 2
▲ Indicates two logic module delay path

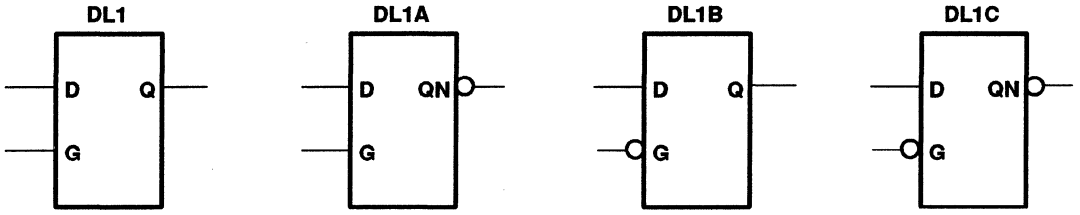
Figure 25. Adders



Module Count = 1

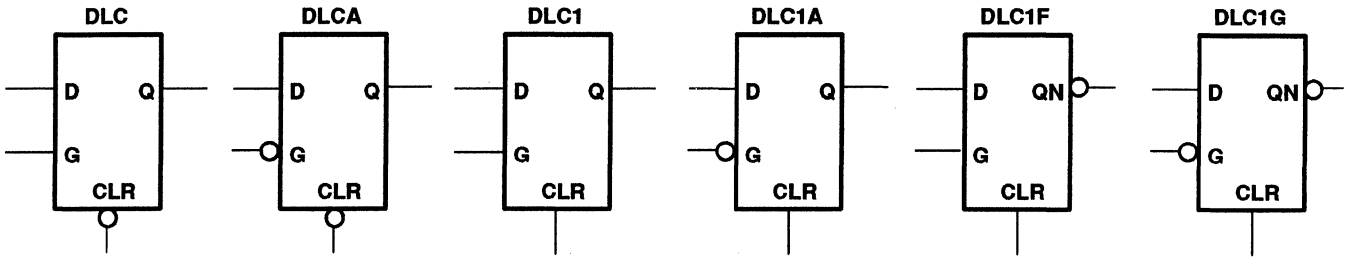
Figure 26. Boolean

D-TYPE LATCHES



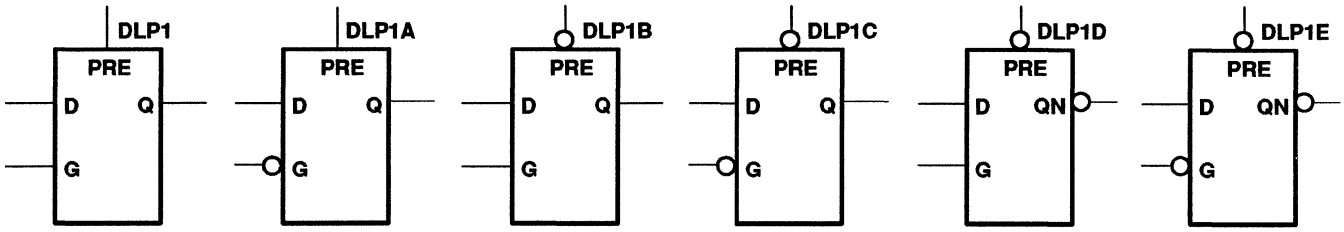
Module Count = 1

D-TYPE LATCHES WITH CLEAR



Module Count = 1

D-TYPE LATCHES WITH PRESET

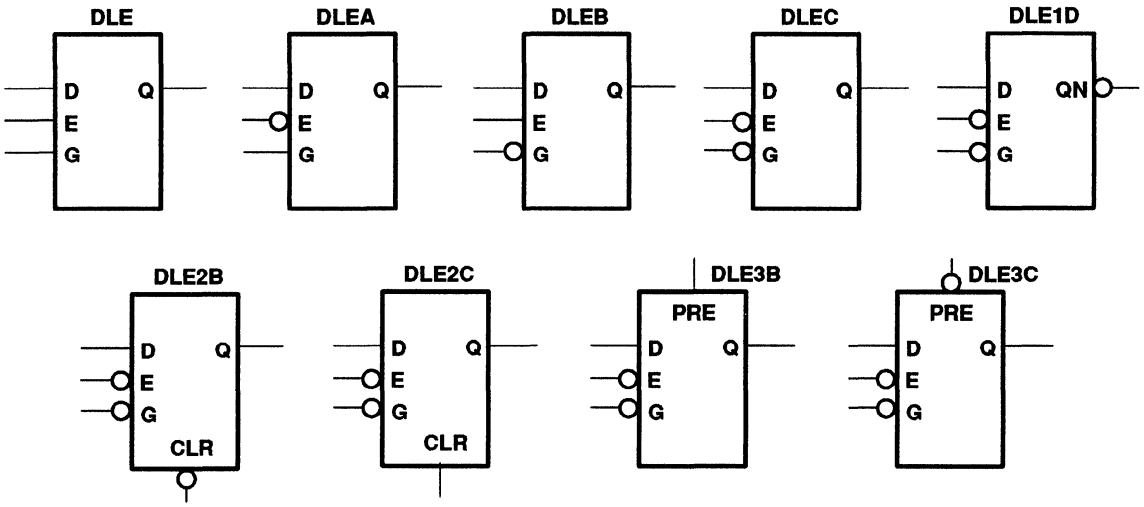


Module Count = 1

Figure 27. D-Type Latches

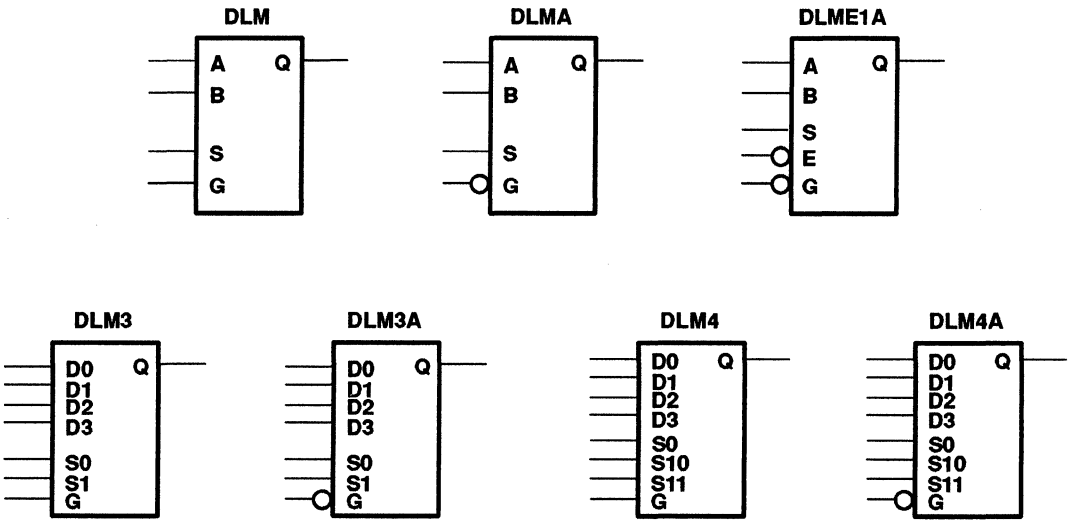
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D-TYPE LATCHES WITH ENABLE



Module Count = 1

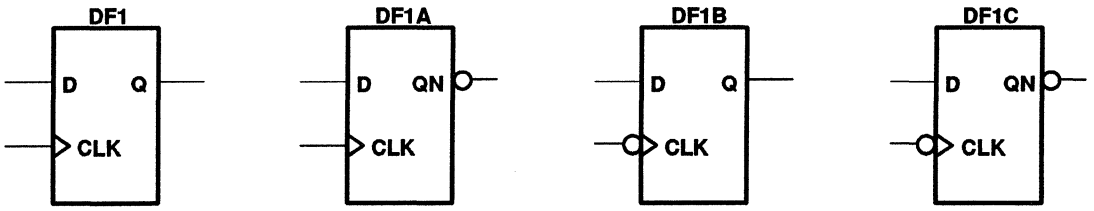
D-TYPE LATCHES WITH MULTIPLEXED INPUTS



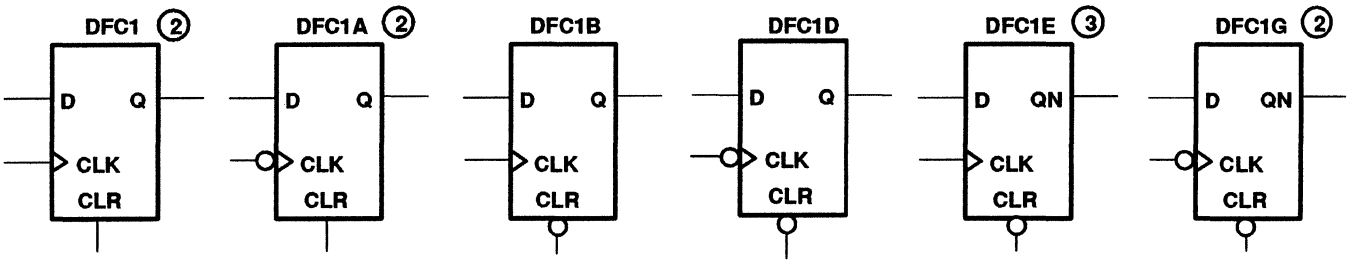
Module Count = 1

Figure 24. D-Type Latches (Continued)

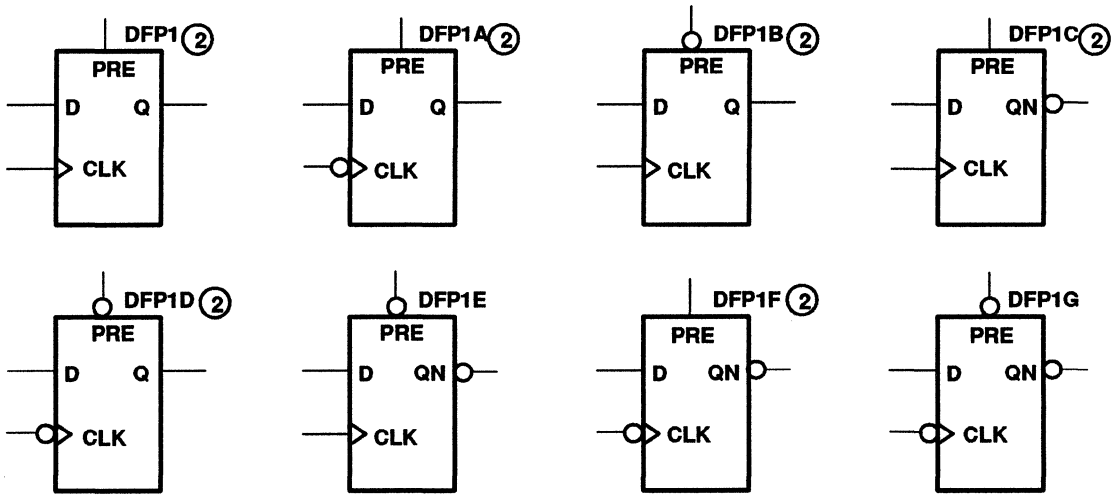
D-TYPE FLIP-FLOPS



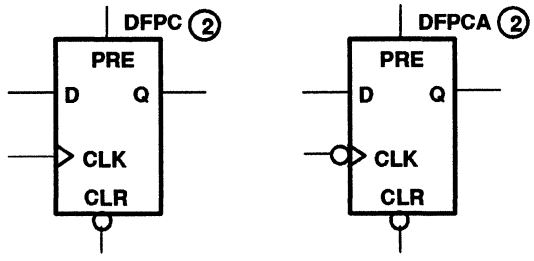
D-TYPE FLIP-FLOPS WITH CLEAR



D-TYPE FLIP-FLOPS WITH PRESET

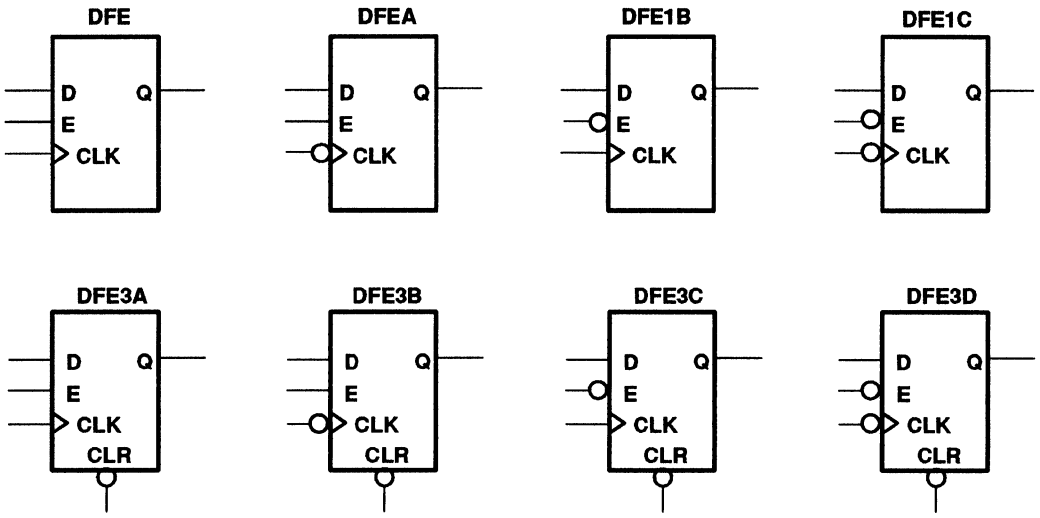


D-TYPE FLIP-FLOPS WITH PRESET AND CLEAR



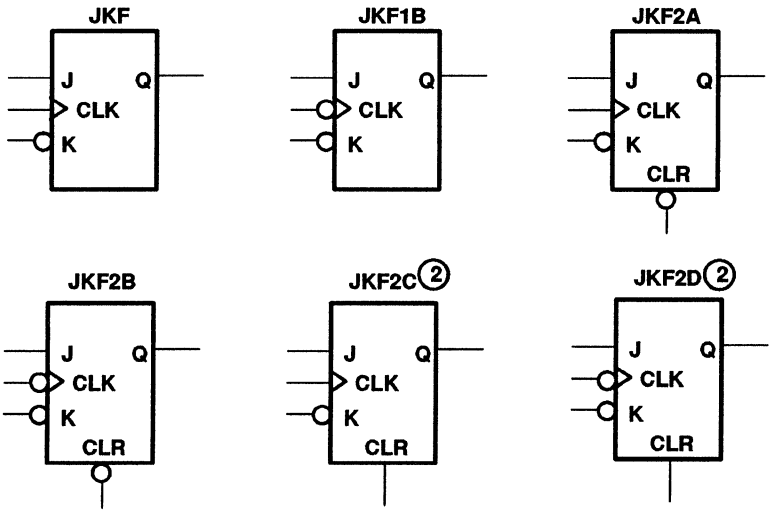
Module Count = 1 (unless otherwise noted)
② Indicates Module Count = 2, ③ Indicates Module Count = 3

Figure 28. D-Type Flip-Flops



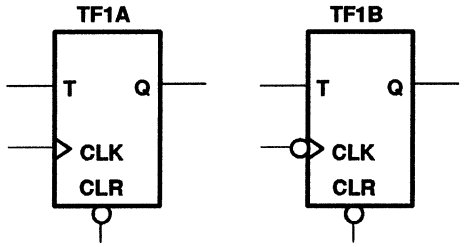
Module Count = 1

Figure 29. D-Type Flip-Flops With Enable



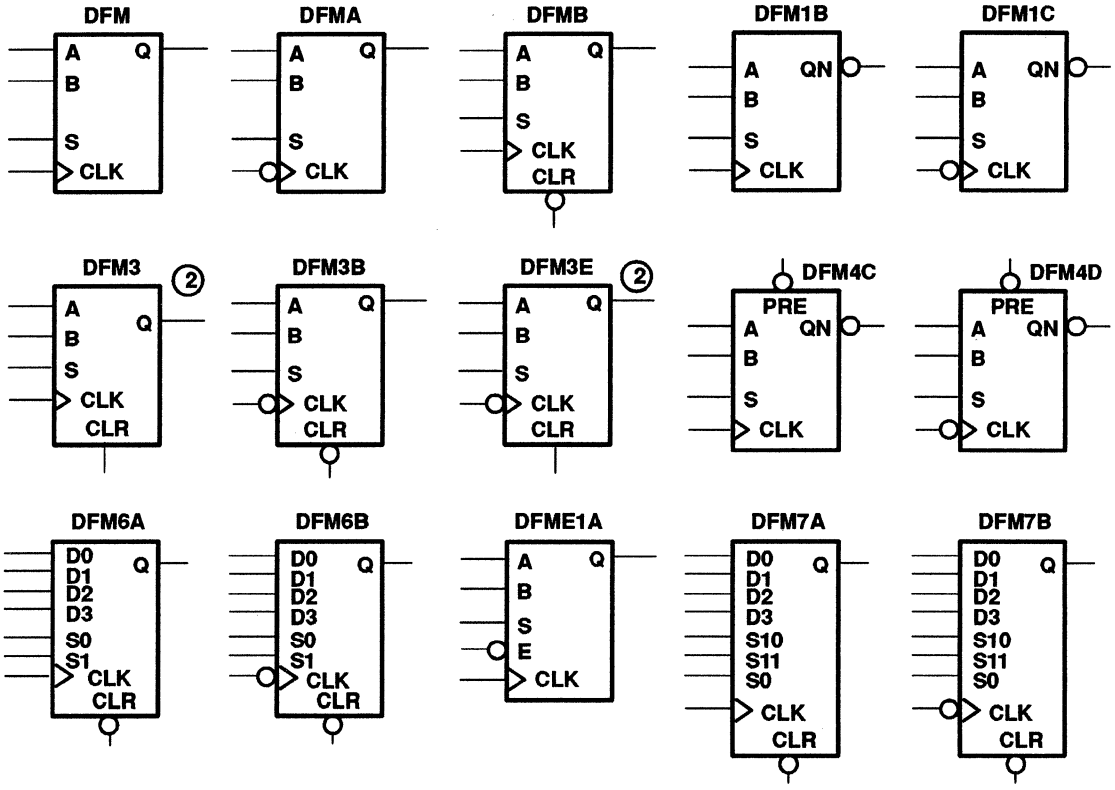
Module Count = 1 (unless otherwise noted)
(2) Indicates Module Count = 2

Figure 30. J-K Flip-Flops



Module Count = 1

Figure 31. Toggle Flip-Flips



Module Count = 1 (unless otherwise noted)
(2) Indicates Module Count = 2

Figure 32. Multiplexed-Input Flip-Flops

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

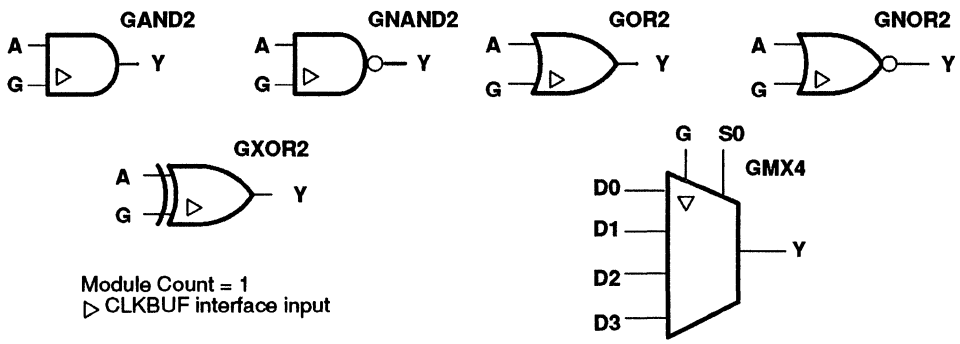
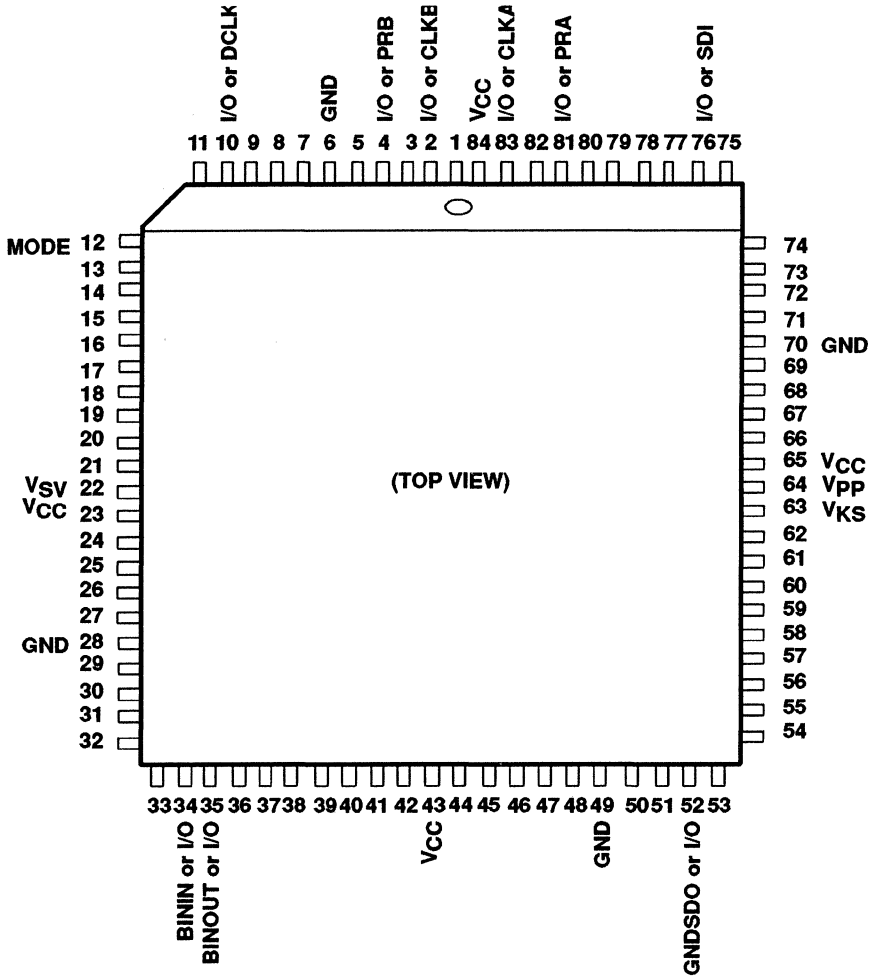


Figure 33. Clock Buffer (CLKBUF) Interface

package pin assignments

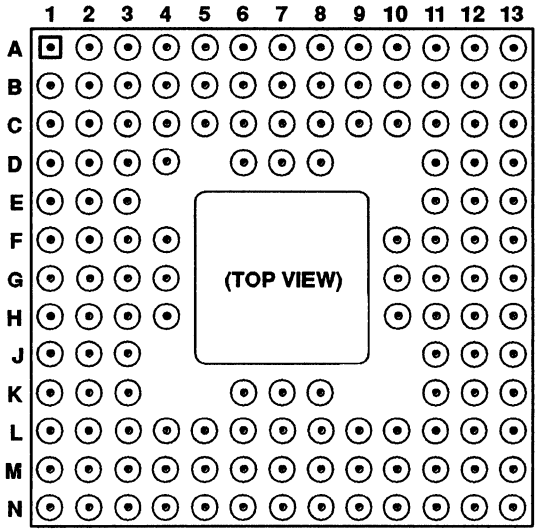


NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. V_{SV} must be terminated to V_{CC} except during programming.
D. V_{KS} must be terminated to circuit ground except during programming.
E. PRA and PRB, the diagnostic probe outputs, should remain open if not used as I/Os.
F. MODE must be terminated to circuit ground except during programming or debugging.†
G. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
H. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
I. All unidentified pins on the pin assignment drawings are standard I/Os.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 34. 84-Pin PLCC Pin Assignment

package pin assignments (continued)



I/O Pin Assignments for the 133-Pin Ceramic Pin Grid Array Package

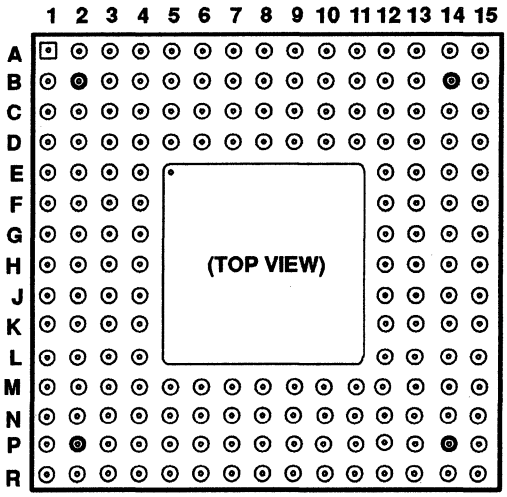
SIGNAL	LOCATION
PRA or I/O	B8
PRB or I/O	C6
MODE	A1
SDI or I/O	B12
SDO or I/O	N12
DCLK or I/O	C3
CLKA or I/O	B7
CLKB or I/O	B6
GND	E3, F4, J2, J3, L5, M9, L9, K12, J11, E12, E11, C9, B9, B5, C5
V_{CC}	G3, G2, L7, K7, G10, G11, D7, C7
V_{PP}	G13
V_{SV}	G4, G12
V_{KS}	H13

NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. V_{SV} must be terminated to V_{CC} except during programming.
D. V_{KS} must be terminated to circuit ground except during programming.
E. PRA and PRB, the diagnostic probe outputs, should remain open if not used as I/Os.
F. MODE must be terminated to circuit ground except during programming or debugging.†
G. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
H. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
I. All unidentified pins on the pin assignment drawings are standard I/Os.
J. Pin D4 is an orientation pin and is electrically isolated.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 35. 133-Pin CPGA Pin Assignment

package pin assignments (continued)



I/O Pin Assignments for the 176-Pin and 177-Pin Ceramic Pin Grid Array Package

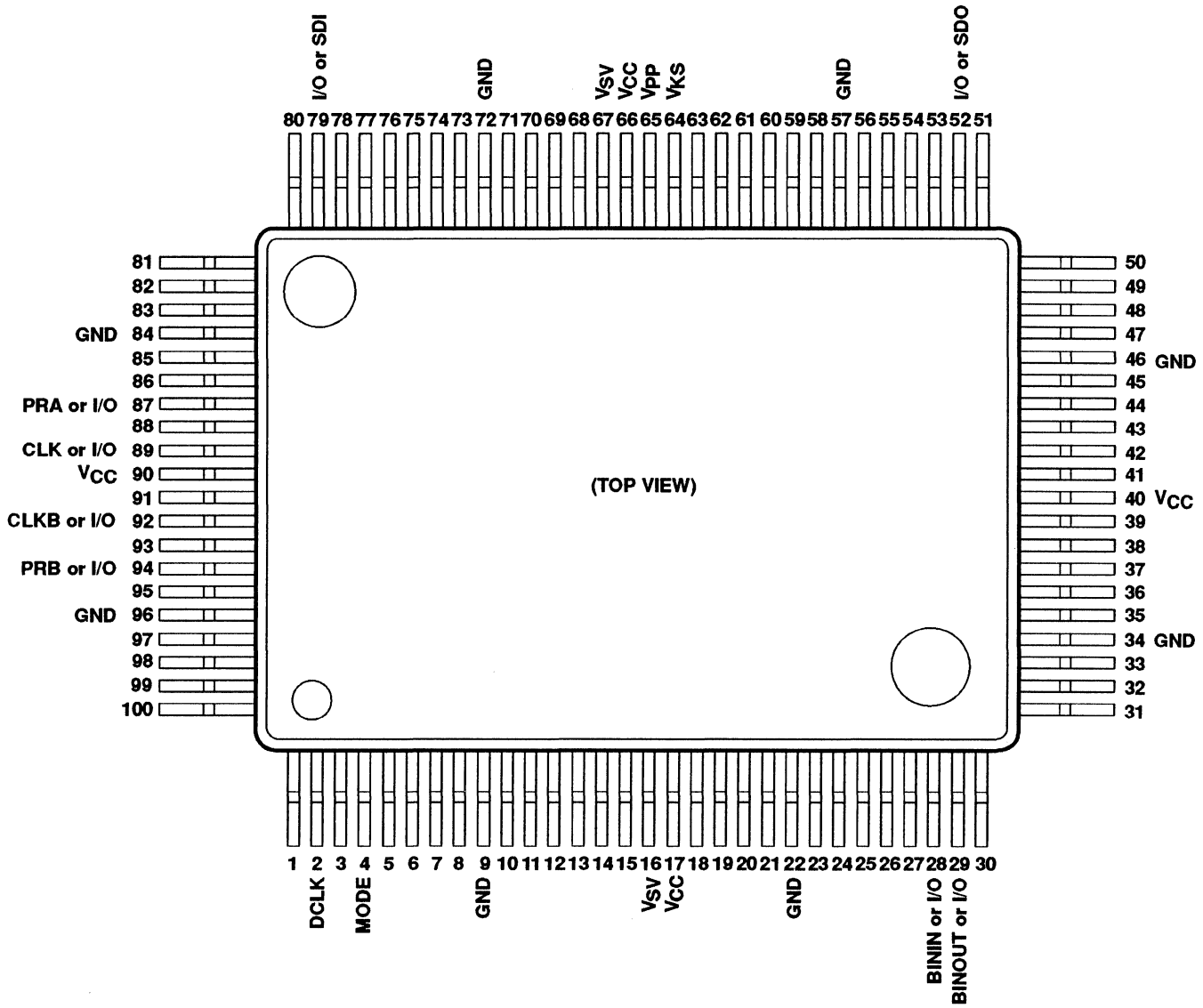
SIGNAL	SIGNALS
PRA or I/O	C9
PRB or I/O	D7
MODE	C3
SDI or I/O	B14
SDO or I/O	P13
DCLK or I/O	B3
CLKA or I/O	A9
CLKB or I/O	B8
GND	D4, E4, G4, H4, K4, L4, M4, M6, M8, M10, M12, K12, J12, H12, F12, E12, D12, D10, C8, D6
V_{CC}	F4, H3, J4, M5, N8, M11, H13, G12, D11, D8, D5
V_{PP}	J14
V_{SV}	H2, H14
V_{KS}	J13

NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. V_{SV} must be terminated to V_{CC} except during programming.
D. V_{KS} must be terminated to circuit ground except during programming.
E. PRA and PRB, the diagnostic probe outputs, should remain open if not used as I/Os.
F. MODE must be terminated to circuit ground except during programming or debugging.†
G. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
H. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
I. All unidentified pins on the pin assignment drawings are standard I/Os.
J. Pin E5 is an orientation pin on the 177-pin package only.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 36. 176-Pin and 177-Pin CPGA Pin Assignment

package pin assignments (continued)

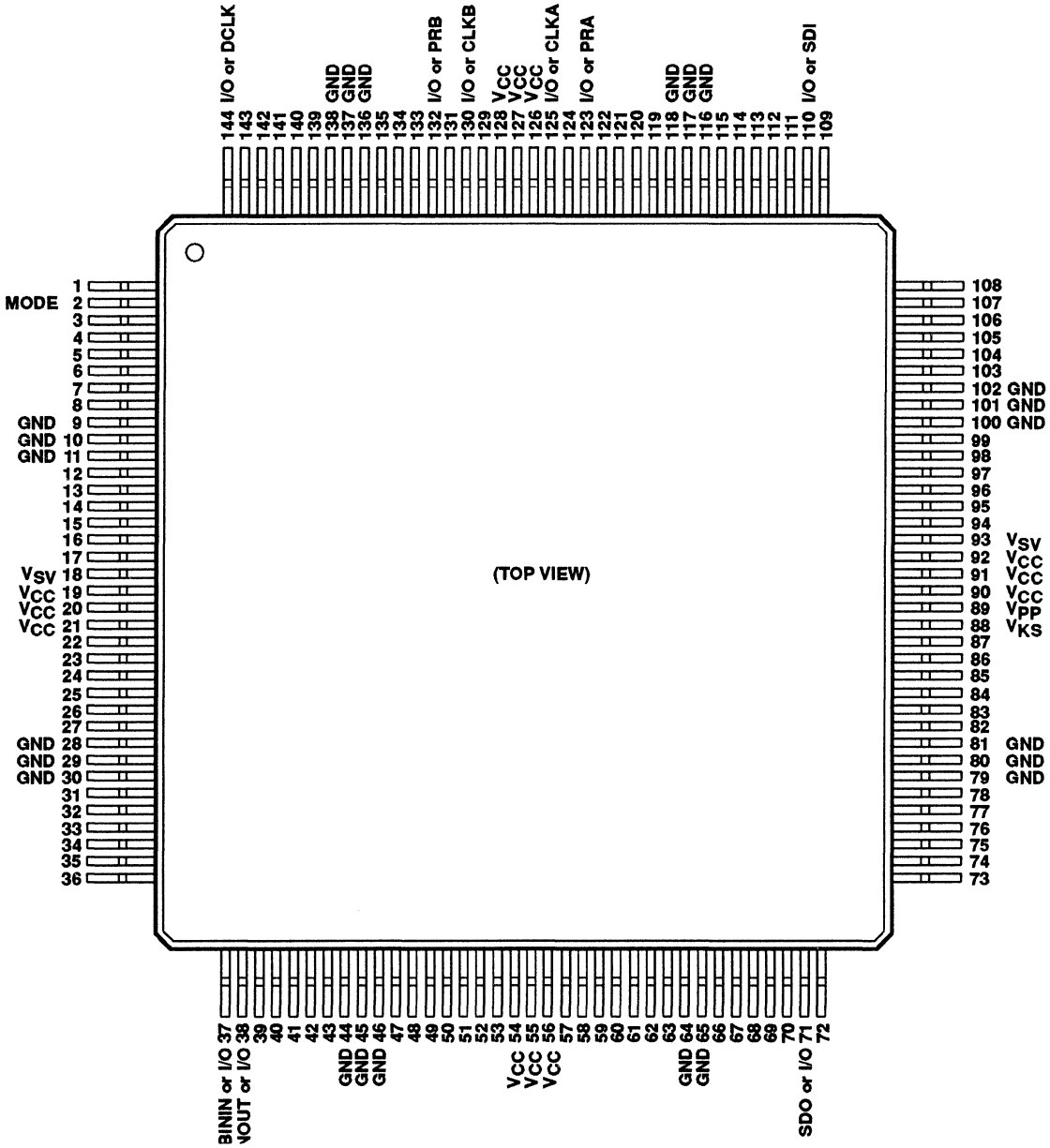


NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. V_{SV} must be terminated to V_{CC} except during programming.
D. V_{KS} must be terminated to circuit ground except during programming.
E. PRA and PRB, the diagnostic probe outputs, should remain open if not used as I/Os.
F. MODE must be terminated to circuit ground except during programming or debugging.†
G. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
H. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
I. All unidentified pins on the pin assignment drawings are standard I/Os.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 37. 100-Pin PQFP Pin Assignment

package pin assignments (continued)

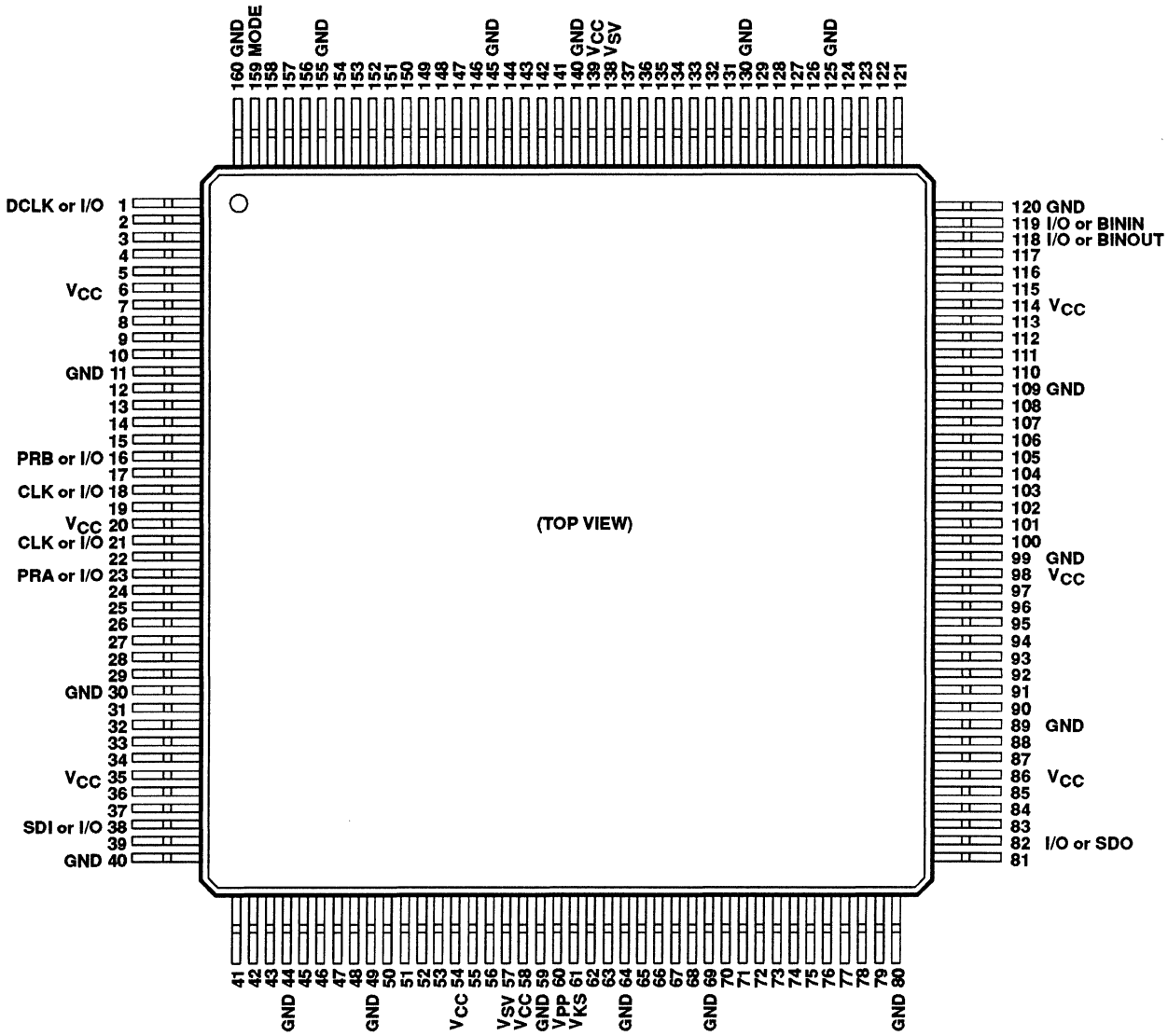


NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. V_{SV} must be terminated to V_{CC} except during programming.
D. V_{KS} must be terminated to circuit ground except during programming.
E. PRA and PRB, the diagnostic probe outputs, should remain open if not used as I/Os.
F. MODE must be terminated to circuit ground except during programming or debugging.†
G. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
H. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
I. All unidentified pins on the pin assignment drawings are standard I/Os.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 38. 144-Pin PQFP Pin Assignment

package pin assignments (continued)



NOTES: A. All pins marked GND are ground connections and must be connected to circuit ground.
B. V_{PP} must be terminated to V_{CC} except during programming.
C. V_{SV} must be terminated to V_{CC} except during programming.
D. V_{KS} must be terminated to circuit ground except during programming.
E. PRA and PRB, the diagnostic probe outputs, should remain open if not used as I/Os.
F. MODE must be terminated to circuit ground except during programming or debugging.†
G. SDI and DCLK should be terminated to circuit ground during normal operation if not used as I/Os.†
H. Unused I/O pins are automatically designated by the Action Logic System as outputs and should remain unconnected. Unused I/O pins are driven low by design.
I. All unidentified pins on the pin assignment drawings are standard I/Os.

† The security fuse must be programmed for SDI and DCLK to function as I/Os. For device debugging on the user's circuit board, MODE, SDI, and DCLK should be terminated to circuit ground through a 10-kΩ (or greater) resistor. They can be tied to ground if not debugging.

Figure 39. 160-Pin PQFP Pin Assignment

package pin assignments (continued)

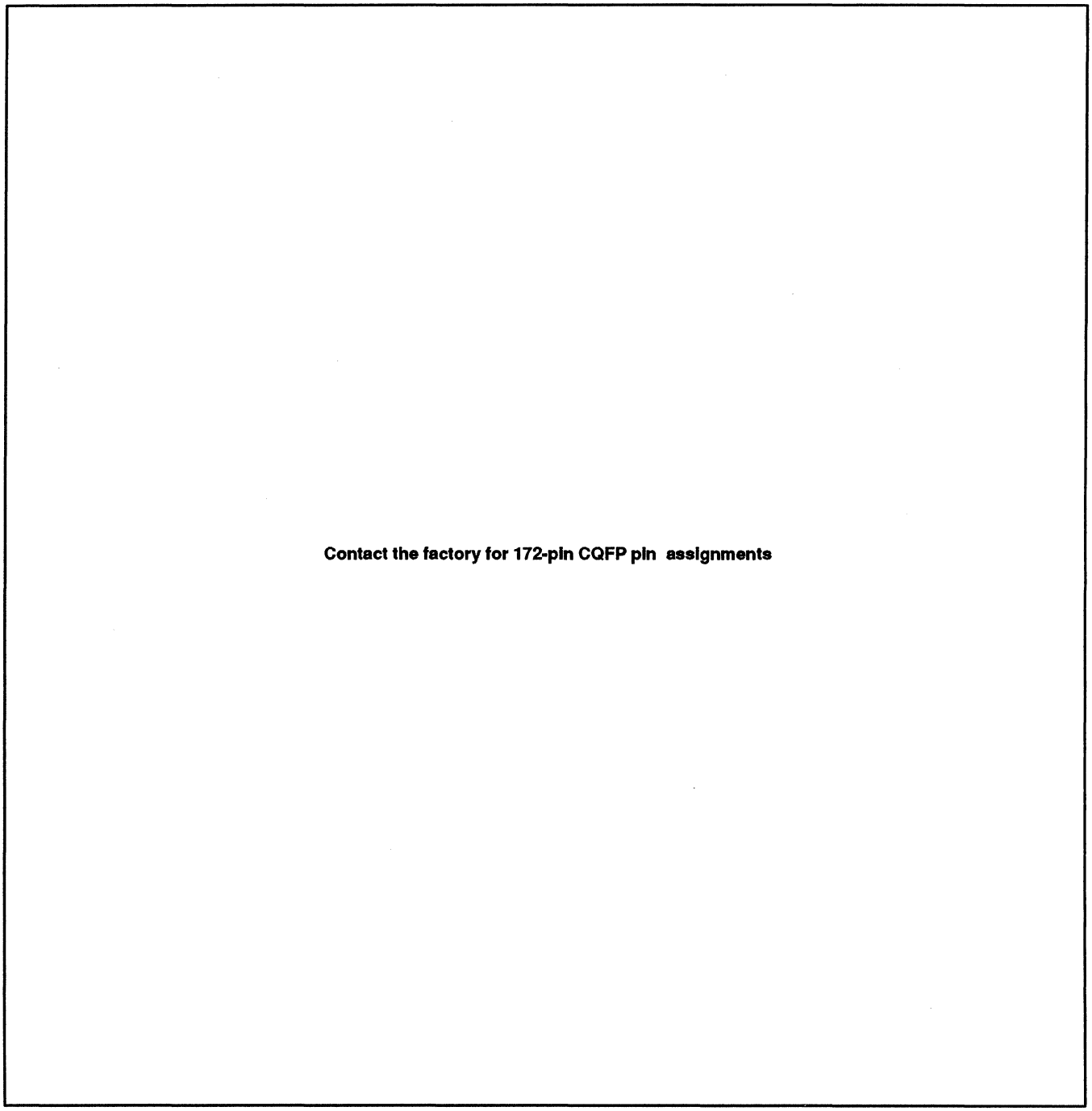
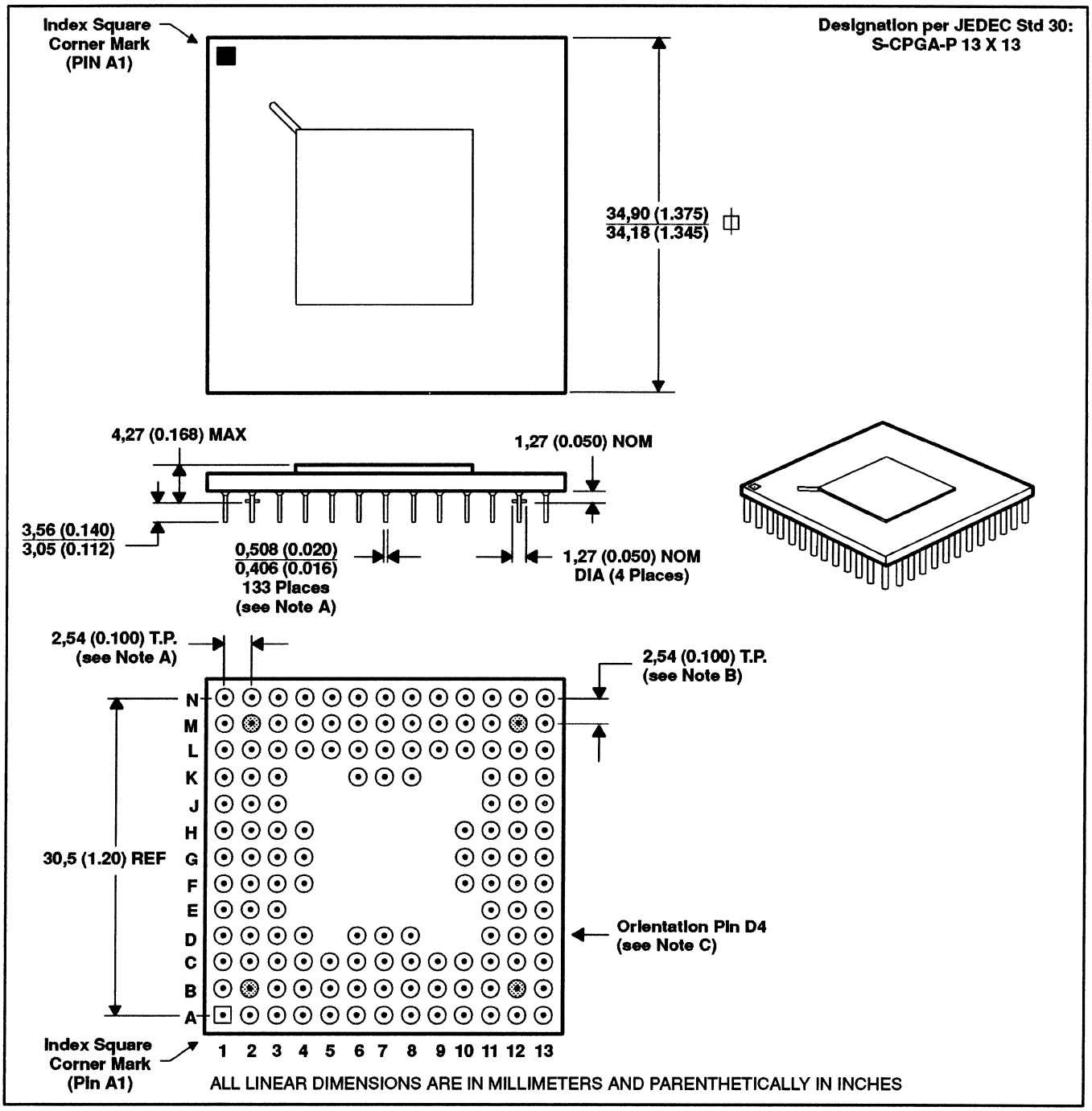


Figure 40. 172-Pin CQFP Pin Assignment

MECHANICAL DATA

133-Pin ceramic pin-grid-array package

This is a hermetically sealed ceramic package with metal cap and solder-coated pins.



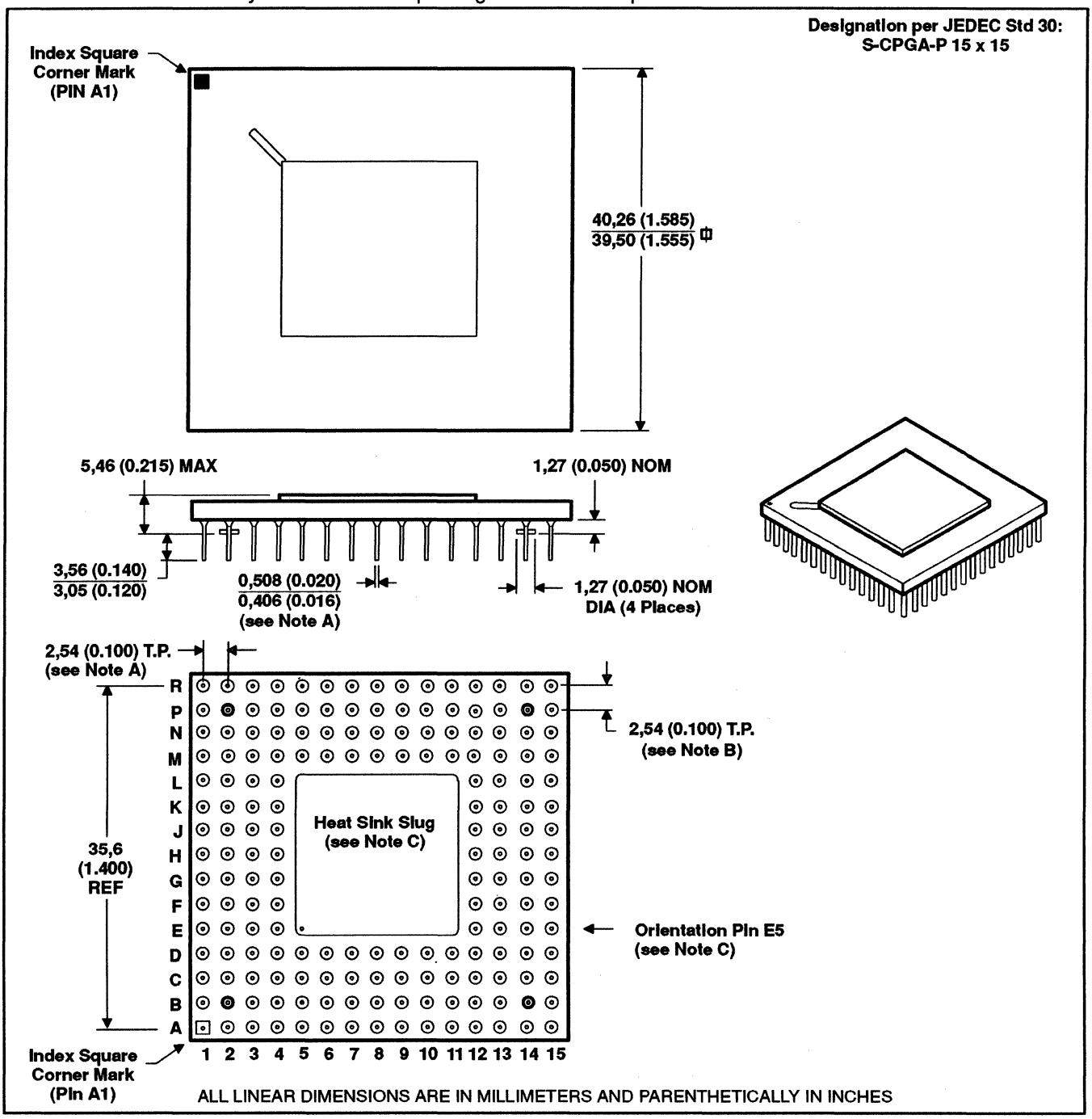
NOTES: A. The lead finish is solder coated. The dimensions do not include the solder finish.
B. Pin tips are located within 0,25 (0.010) diameter relative to each other at maximum material condition. Pin bases are located within 0,76 (0.030) diameter at maximum material condition relative to the center of the ceramic.
C. Orientation pin D4 is electrically isolated.

Figure 41. 133-Pin Ceramic Pin-Grid-Array Package

MECHANICAL DATA

176- and 177-pin ceramic pin-grid-array packages

This is a hermetically sealed ceramic package with metal cap.



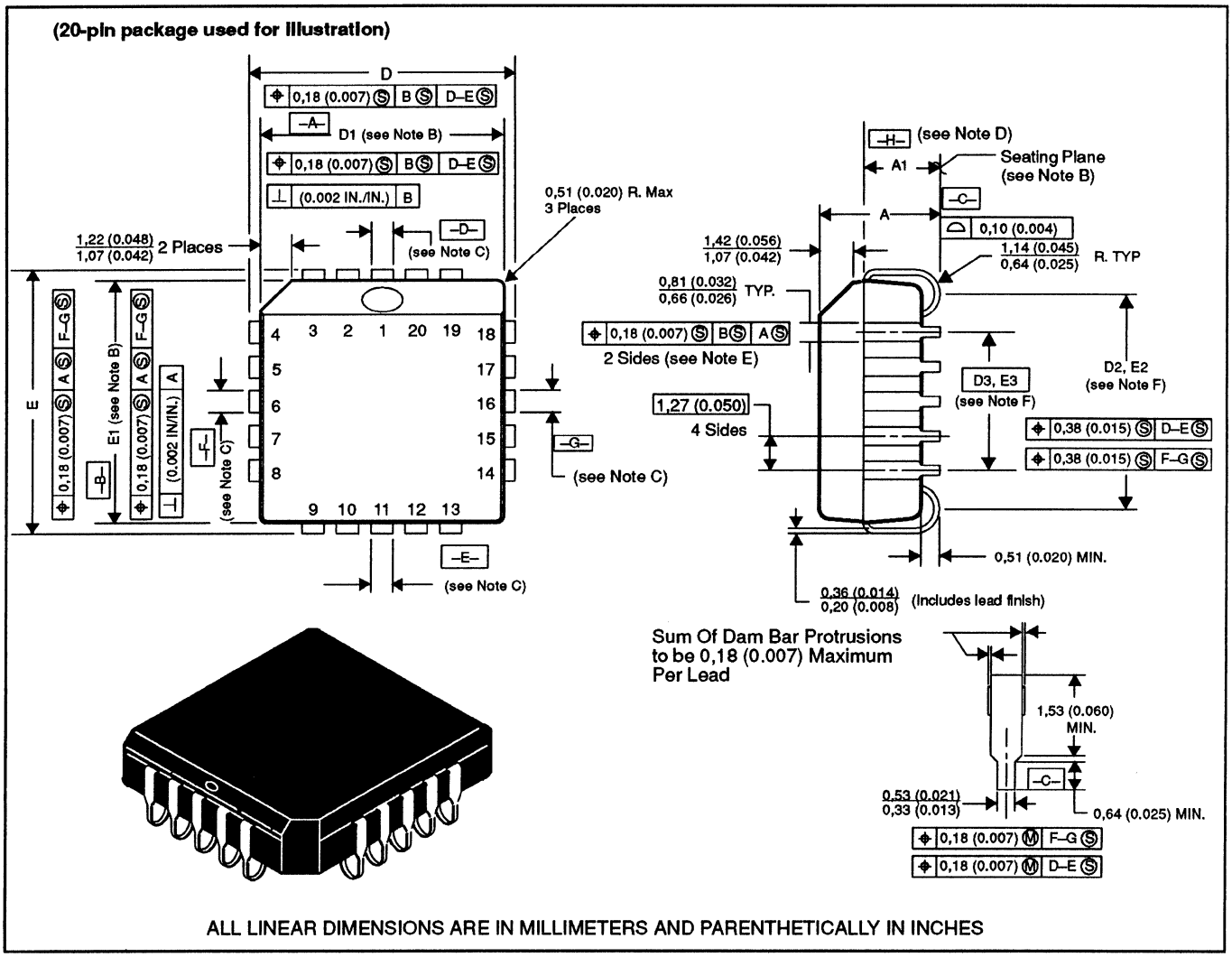
NOTES: A. Leads and external heatsink slugs surfaces are gold plated. Military version devices may have additional solder coated leads. Diagrams do not include the solder finish where applicable.

B. Pin tips are located within 0,25 (0.010) diameter relative to each other at maximum material condition. Pin bases are located within 0,76 (0.030) diameter at maximum material condition relative to the center of the ceramic.

C. Orientation pin E5 and the heat sink slug are at substrate ground. Pin E5 is available only for TPC1280GB-177.

Figure 42. 176- and 177-Pin Ceramic Pin-Grid-Array Packages

MECHANICAL DATA



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

JEDEC OUTLINE	DIMS / PINS	A MIN	A MAX	A1 MIN	A1 MAX	D, E MIN	D, E MAX	D1, E1 MIN	D1, E1 MAX	D2, E2 MIN	D2, E2 MAX	D3, E3 BASIC
MO-047AF	84	4,19 (0.165)	5,08 (0.200)	2,29 (0.090)	3,30 (0.130)	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.158)	27,69 (1.090)	28,70 (1.130)	25,40 (1.000)

NOTES: A. All dimensions conform to JEDEC Specification MO-047AA/AF. Dimensions and tolerancing are per ANSI Y14.5M-1982.

B. Dimension D1 and E1 do not include mold flash protrusion. Protrusion shall not exceed 0,25 (.010) on any side.

C. Datums D–E and F–G for center leads are determined at datum –H–

D. Datum –H– is located at top of leads where they exit plastic body.

E. Location to datums –A– and –B– to be determined at datum –H–

F. Determined at seating plane –C–

Figure 43. Plastic Leaded Chip Carriers

MECHANICAL DATA

Contact the factory for 172-pin CQFP mechanical data.

Figure 44. 172-Pin Ceramic Quad Flat Package

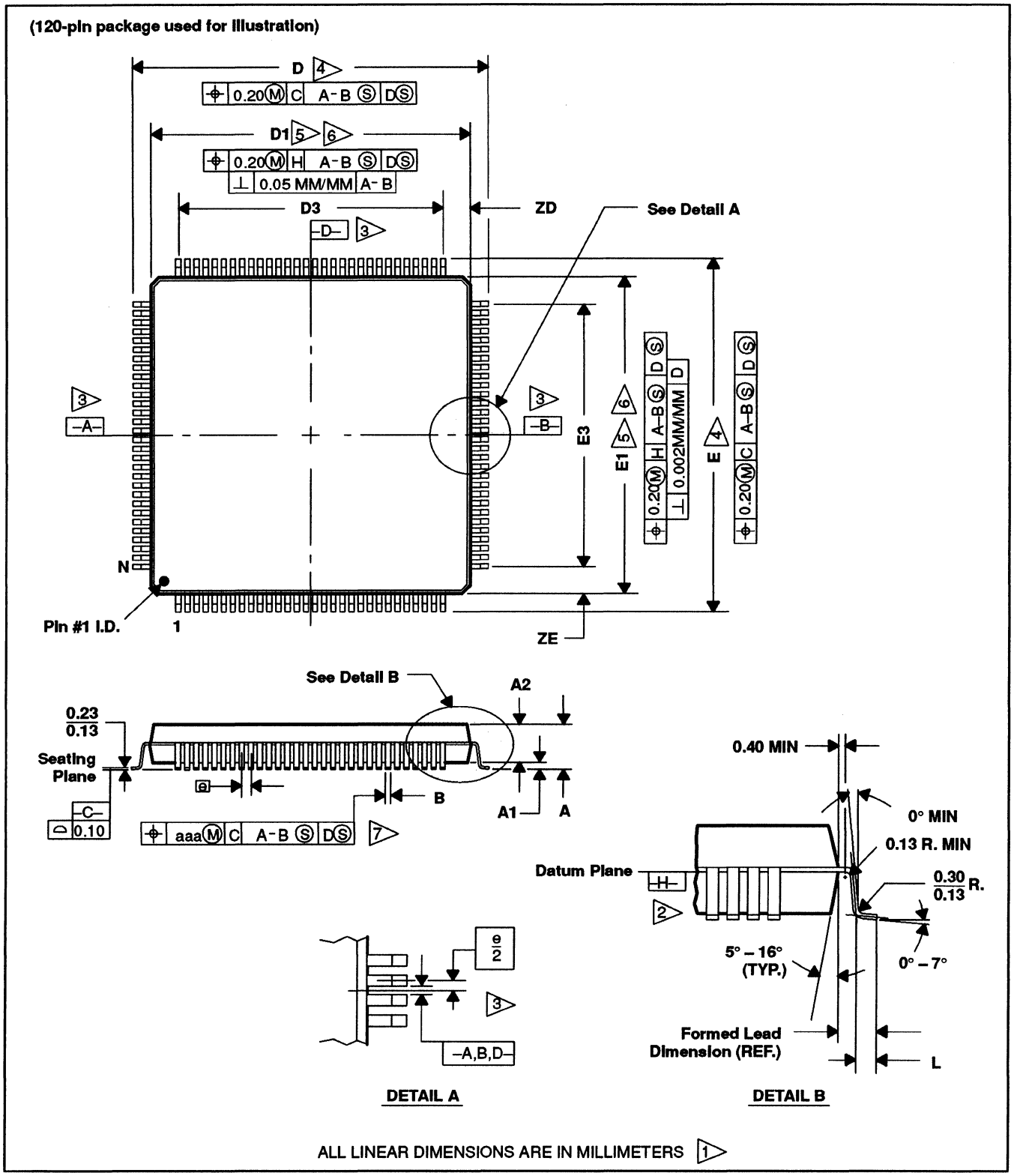


Figure 45. Plastic Quad Flat Packages

JEDEC OUTLINE	# PINS	PKG TYPE	A MAX	A1 MIN	A2 MAX MIN	D MAX MIN	D1 MAX MIN	D3 (REF)	ZD (REF)	E MAX MIN	E1 MAX MIN	E3 (REF)	ZE (REF)	L MAX MIN	e BASIC	B MAX MIN	aaa	ND	NE	FORMED LEAD DIM. (REF)
MO-108/CC-1	100	RECT	3,40	0,25	3,05 2,55	23,45 22,95	20,10 19,90	18,85	0,58	17,45 16,95	14,10 13,90	12,35	0,83	0,95 0,65	0,65	0,38 0,22	0,12	30	20	1,60
MO-108/DC-1	144	Square	4,07	0,25	3,67 3,17	31,45 30,95	28,10 27,90	22,75	2,63	31,45 30,95	28,10 27,90	22,75	2,63	0,95 0,65	0,65	0,38 0,22	0,12	36	36	1,60
MO-112/DD-1	160	Square	4,07	0,25	3,67 3,17	32,15 31,65	28,10 27,90	25,35	1,33	32,15 31,65	28,10 27,90	25,35	1,33	0,95 0,65	0,65	0,38 0,22	0,12	40	40	1,95

NOTES:
1. All dimensions are millimeters (mm), and the 100- and 144-pin packages conform to JEDEC specification MO-108 (issue A/October 1990), and the 160-pin package conforms to JEDEC specification MO-112 (issue A/August 1990). Dimensions and tolerancing per ANSI Y14.5M-1982.
2. Datum plane –H– is located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
3. Datums A–B and –D– for center leads are determined at datum –H– .
4. Determined at seating plane –C–
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 per side. Dimensions D1 and E1 do include mold mismatch and are determined at datum plane –H– .
6. Determined at datum plane –H–
7. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 total in excess of the B dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot. A minimum solder finish thickness of 0.0051 is guaranteed.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TI Worldwide Sales Offices

ALABAMA: Huntsville: 4960 Corporate Drive, Suite 150, Huntsville, AL 35805, (205) 837-7530.

ARIZONA: Phoenix: 8825 N. 23rd Avenue, Suite 100, Phoenix, AZ 85021, (602) 995-1007.

CALIFORNIA: Irvine: 1920 Main Street, Suite 900, Irvine, CA 92714, (714) 660-1200; **San Diego:** 5625 Ruffin Road, Suite 100, San Diego, CA 92123, (619) 278-9600; **Santa Clara:** 5353 Betsy Ross Drive, Santa Clara, CA 95054, (408) 980-9000; **Woodland Hills:** 21550 Oxnard Street, Suite 700, Woodland Hills, CA 91367, (818) 704-8100.

COLORADO: Aurora: 1400 S. Potomac Street, Suite 101, Aurora, CO 80012, (303) 368-8000.

CONNECTICUT: Wallingford: 9 Barnes Industrial Park So., Wallingford, CT 06492, (203) 269-0074.

FLORIDA: Altamonte Springs: 370 S. North Lake Boulevard, Suite 1008, Altamonte Springs, FL 32701, (407) 260-2116; **Fort Lauderdale:** 2950 N.W. 62nd Street, Suite 100, Fort Lauderdale, FL 33309, (305) 973-8502; **Tampa:** 4803 George Road, Suite 390, Tampa, FL 33634-6234, (813) 885-7588.

GEORGIA: Norcross: 5515 Spalding Drive, Norcross, GA 30092-2560, (404) 662-7967.

ILLINOIS: Arlington Heights: 515 West Algonquin, Arlington Heights, IL 60005, (708) 640-2925.

INDIANA: Carmel: 550 Congressional Drive, Suite 100, Carmel, IN 46032, (317) 573-6400; **Fort Wayne:** 103 Airport North Office Park, Fort Wayne, IN 46825, (219) 489-4697.

KANSAS: Overland Park: 7300 College Blvd., Lighton Plaza, Suite 150, Overland Park, KS 66210, (913) 451-4511.

MARYLAND: Columbia: 8815 Centre Park Dr., Suite 100, Columbia, MD 21045, (410) 964-2003.

MASSACHUSETTS: Waltham: Bay Colony Corporate Center, 950 Winter Street, Suite 2800, Waltham, MA 02154, (617) 895-9100.

MICHIGAN: Farmington Hills: 33737 W. 12 Mile Road, Farmington Hills, MI 48018, (313) 553-1581.

MINNESOTA: Eden Prairie: 11000 W. 78th Street, Suite 100, Eden Prairie, MN 55344, (612) 828-9300.

MISSOURI: St. Louis: 12412 Powerscourt Drive, Suite 125, St. Louis, MO 63131, (314) 821-8400.

NEW JERSEY: Iselin: Metropolitan Corporate Plaza, 485 Bldg E. U.S. 1 South, Iselin, NJ 08830, (908) 750-1050.

NEW MEXICO: Albuquerque: 2709 J. Pan American Freeway NE, Albuquerque, NM 87101, (505) 345-2555.

NEW YORK: East Syracuse: 6365 Collamer Drive, East Syracuse, NY 13057, (315) 463-9291; **Fishkill:** 300 Westage Business Ctr., Suite 140, Fishkill, NY 12524, (914) 897-2900; **Melville:** 48 South Service Road, Suite 100, Melville, NY 11747, (516) 454-6601; **Pittsford:** 2851 Clover Street, Pittsford, NY 14534, (716) 385-6770.

NORTH CAROLINA: Charlotte: 8 Woodlawn Green, Suite 100, Charlotte, NC 28217, (704) 527-0930; **Raleigh:** 2809 Highwoods Boulevard, Suite 100, Raleigh, NC 27625, (919) 876-2725.

OHIO: Beachwood: 23775 Commerce Park Rd., Beachwood, OH 44122-5875, (216) 765-7258; **Beavercreek:** 4200 Colonel Glenn Hwy., Suite 600, Beavercreek, OH 45431, (513) 427-6200.

OREGON: Beaverton: 6700 S.W. 105th Street, Suite 110, Beaverton, OR 97005, (503) 643-6758.

PENNSYLVANIA: Blue Bell: 670 Sentry Parkway, Suite 200, Blue Bell, PA 19422, (215) 825-9500.

PUERTO RICO: Hato Rey: 615 Mercantil Plaza Bldg., Suite 505, Hato Rey, PR 00919, (809) 753-8700.

TEXAS: Austin: 12501 Research Boulevard, Austin, TX 78759, (512) 250-6769; **Dallas:** 7839 Churchill Way, Dallas, TX 75251, (214) 917-1264; **Houston:** 9301 Southwest Freeway, Commerce Park, Suite 360, Houston, TX 77074, (713) 778-6592; **Midland:** FM 1788 & I-20, Midland, TX 79711-0448, (915) 561-7137.

UTAH: Salt Lake City: 2180 South 1300 East, Suite 335, Salt Lake City, UT 54106, (801) 466-8972.

WISCONSIN: Waukesha: 20825 Swenson Drive, Suite 900, Waukesha WI 53186, (414) 798-1001.

CANADA: Nepean: 301 Moodie Drive, Suite 102, Mallorn Centre, Nepean, Ontario, Canada K2H 9C4, (613) 726-1970; **Richmond Hill:** 280 Centre Street East, Richmond Hill, Ontario, Canada, L4C 1B1, (416) 884-9181; **St. Laurent:** 9460 Trans Canada Highway, St. Laurent, Quebec, Canada H4S 1R7, (514) 335-8392.

AUSTRALIA (& NEW ZEALAND): Texas Instruments Australia Ltd., 6-10 Talavera Road, North Ryde (Sydney), New South Wales, Australia 2113, 2-878-9000; 14th Floor, 380 St., Kilda Road, Melbourne, Victoria, Australia 3004, 3-696-1211; 171 Philip Highway, Elizabeth, South Australia 5112, 8 696-2066.

BELGIUM: Texas Instruments Belgium S.A./N.V., Avenue Jules Bordetlaan 11, 1140 Brussels, Belgium, (02) 242 30 80.

BRAZIL: Texas Instrumentos Electronicos do Brasil Ltda., Av. Eng. Luiz Carlos Berrini, 1461-11o. andar, 04571, Sao Paulo, SP, Brazil, 11-535-5133.

DENMARK: Texas Instruments A/S, Borupvang 2D, 2750 Ballerup, Denmark, (44) 68 74 00.

FINLAND: Texas Instruments OY, Ahertajantie 3, P.O. Box 86, 02321 Espoo, Finland, (0) 802 6517.

FRANCE: Texas Instruments France, 8-10 Avenue Morane-Saulnier, B.P. 67, 78141 Velizy-Villacoublay Cedex, France, (1) 30 70 1003.

GERMANY: Texas Instruments Deutschland GmbH., Haggertystrasse 1, 8050 Freising, (08161) 80-0; Kurfürstendamm 195-196, 1000 Berlin 15, (030) 8 82 73 65; Düsseldorfer Strasse 32, 6236 Eschborn 1, (06196) 80 70; Kirchhorster Strasse 2, 3000 Hannover 51, (0511) 64 68-0; Maybachstrasse II, 7302 Ostfildern 2 (Nellingen), (0711) 3403257; Gildehofcenter, Hollestrasse 3, 4300 Essen 1, (0201) 24 25-0.

HOLLAND: Texas Instruments Holland B.V., Hogehilweg 19, Postbus 12995, 1100 AZ Amsterdam-Zuidoost, Holland, (020) 5602911.

HONG KONG: Texas Instruments Hong Kong Ltd., 8th Floor, World Shipping Center, 7 Canton Road, Kowloon, Hong Kong, 737-0338.

HUNGARY: Texas Instruments Representation, Budaorsi ut 42, 1112 Budapest, Hungary, (1) 1 66 66 17.

IRELAND: Texas Instruments Ireland Ltd., 7/8 Harcourt Street, Dublin 2, Ireland, (01) 755233.

ITALY: Texas Instruments Italia S.p.A., Centro Direzionale Colleoni, Palazzo Perseo - Via Paracelso, 12, 20041 Agrate Brianza (Mi), Italy, (039) 63221; Via Castello della Magliana, 38, 00148 Roma, Italy, (06) 6572651; Via Amendola, 17, 40100 Bologna, Italy, (051) 554004.

JAPAN: Texas Instruments Japan Ltd., Aoyama Fuji Building 3-6-12 Kita-Aoyama Minato-Ku, Tokyo, Japan 107, 03-498-2111; MS Shibaura Bldg. 9F, 4-13-23 Shibaura, Minato-ku, Tokyo, Japan 108, 03-769-8700; Nissho-Iwai Bldg. 5F, 2-5-8 Imabashi, Chuou-ku, Osaka, Japan 541, 06-204-1881; Dai-ni Toyota Bldg. Nishi-kan 7F, 4-10-27 Meieki, Nakamura-ku, Nagoya, Japan 450, 052-583-8691; Kanazawa Oyama-cho Daiichi Seimei Bldg. 6F, 3-10 Oyama-cho, Kanazawa-shi, Ishikawa, Japan 920, 0762-23-5471; Matsumoto Showa Bldg. 6F, 1-2-11 Fukashi, Matsumoto-shi, Nagano, Japan 390, 0263-33-1060; Daiichi Olympic Tachikawa Bldg. 6F, 1-25-12, Akebono-cho, Tachikawa-shi, Tokyo, Japan 190, 0425-27-6760; Yokohama Business Park East Tower 10F, 134 Goudo-cho, Hodogaya-ku, Yokohama-shi, Kanagawa, Japan 240, 045-338-1220; Nihon Seimei Kyoto Yasaka Bldg. 5F, 843-2, Higashi-Shiokohji-cho, Higashi-iru, Nishinotoh-in, Shiokohji-dori, Shimogyo-ku, Kyoto, Japan 600, 075-341-7713; Sumitomo Seimei Kumagaya Bldg. 8F, 2-44 Yayoi, Kumagaya-shi, Saitama, Japan 360, 0485-22-2440; 2597-1, Aza Harudai, Oaza Yasaka, Kitsuki-shi, Oita, Japan 873, 09786-3-3211.

KOREA: Texas Instruments Korea Ltd., 28th Floor, Trade Tower, 159, Samsung-Dong, Kangnam-ku Seoul, Korea, 2-551-2800.

MALAYSIA: Texas Instruments Malaysia, Sdn. Bhd., Asia Pacific, Lot 36.1 #Box 93, Menara Maybank, 100 Jalan Tun Perak, 50050 Kuala Lumpur, Malaysia, 2306001.

MEXICO: Texas Instruments de Mexico S.A. de C.V., Alfonso Reyes 115, Col. Hipodromo Condesa, Mexico, D.F., 06170, 5-515-6081.

NORWAY: Texas Instruments Norge A/S, B.P. 106, Refstad (Sinsenveien 53), 0513 Oslo 5, Norway, (02) 155 090.

PEOPLE'S REPUBLIC OF CHINA: Texas Instruments China Inc., Beijing Representative Office, 7-05 CITIC Building, 19 Jianguomenwai Dajie, Beijing, China, 500-2255, Ext. 3750.

PHILIPPINES: Texas Instruments Asia Ltd., Philippines Branch, 14th Floor, Ba-Lepanto Building, Paseo de Roxas, Makati, Metro Manila, Philippines, 2-8176031.

PORTUGAL: Texas Instruments Equipamento Electronico (Portugal) LDA., Ing. Frederico Ulricho, 2650 Moreira Da Maia, 4470 Maia, Portugal, (2) 948 1003.

SINGAPORE (& INDIA, INDONESIA, THAILAND): Texas Instruments Singapore (PTE) Ltd., Asia Pacific, 101 Thomson Road, #23-01 United Square, Singapore 1130, 3508100.

SPAIN: Texas Instruments España S.A., c/Gobelas 43, Urbanizasion La Florida, 28023 Madrid, Spain, (1) 372 8051; c/Diputacion, 279-3-5, 08007 Barcelona, Spain, (3) 317 91 80.

SWEDEN: Texas Instruments International Trade Corporation (Sverigefilialen), Isafjordsgatan, Box 30, 164 93 Kista, Sweden, (08) 752 58 00.

SWITZERLAND: Texas Instruments Switzerland AG, Riedstr. 6, 8953 Dietikon, Switzerland, (01) 744 2811.

TAIWAN: Texas Instruments Taiwan Limited, Taipei Branch, 10th Floor, Bank Tower, 205 Tung Hua N. Road, Taipei, Taiwan, 10592, Republic of China, 2-713 9311.

TURKEY: Texas Instruments, DSEG MidEast Regional Marketing Office, Karum Center, Suite 442, Iran Caddesi 21, 06680 Kavaklidere, Ankara, Turkey, 4-468-0155.

UNITED KINGDOM: Texas Instruments Ltd., Manton Lane, Bedford, England, MK41 7PA, (234) 270 111.

TI Authorized North American Distributors

Alliance Electronics, Inc. (military product only)
Almac/Arrow
Anthem Electronics
Arrow/Schweber
Future Electronics (Canada)
Hall-Mark Electronics
Marshall Industries
Newark Electronics*
Wyle Laboratories
Zeus Components
Rochester Electronics, Inc. (obsolete product only)
*Not authorized for TI military products

TEXAS INSTRUMENTS

B0892

Printed in the U.S.A.