

TEXAS INSTRUMENTS
FIELD PROGRAMMABLE LOGIC DEPARTMENT
PROGRAMMING ALGORITHM SPECIFICATION

DEVICE FAMILY TIBPAL16XX
 DEVICES INCLUDED TIBPAL16LB-12, TIBPAL16R4-12, TIBPAL16R6-12, TIBPAL16R8-12
 TIBPAL16LB-15, TIBPAL16R4-15, TIBPAL16R6-15, TIBPAL16R8-15
 TIBPAL16LB-25, TIBPAL16R4-25, TIBPAL16R6-25, TIBPAL16R8-25

PROGRAMMING PROCEDURE:

Array fuses are programmed using a linear select method. Each fuse can be opened by selecting the appropriate (1 of 32) Input Line and then pulsing the correct (1 of 64) Product Line. The levels for selecting Input Lines and Product Lines are shown in Table 1-2.

- Step 1: Raise PGM ENABLE to V_{IH} .
- Step 2: Select an Input Line by applying appropriate levels to L/R and PI pins. Apply V_{IL} or V_{IH} to selected PI pin (See Table 1-2).
- Step 3: Select Product Line by applying appropriate levels to PA pins (See Table 1-2).
- Step 4: Raise V_{CC} to V_{IH} .
- Step 5: Blow the fuse by pulsing the appropriate PO pin to V_{IH} .
- Step 6: Return V_{CC} to 5 volts and pulse PGM VERIFY. The PO pin will exhibit a low output if the fuse is blown.

Four fuse locations can be verified simultaneously, however, fuses should be addressed and blown sequentially.

If the fuse is still intact, steps 4 thru 6 may be repeated until the fuse is successfully blown, not to exceed 4 retries. Do not apply additional pulses to a fuse once it is correctly programmed.

For Input and Product Line selection see Table 1-2.

For programming waveforms see Figure 1-1.

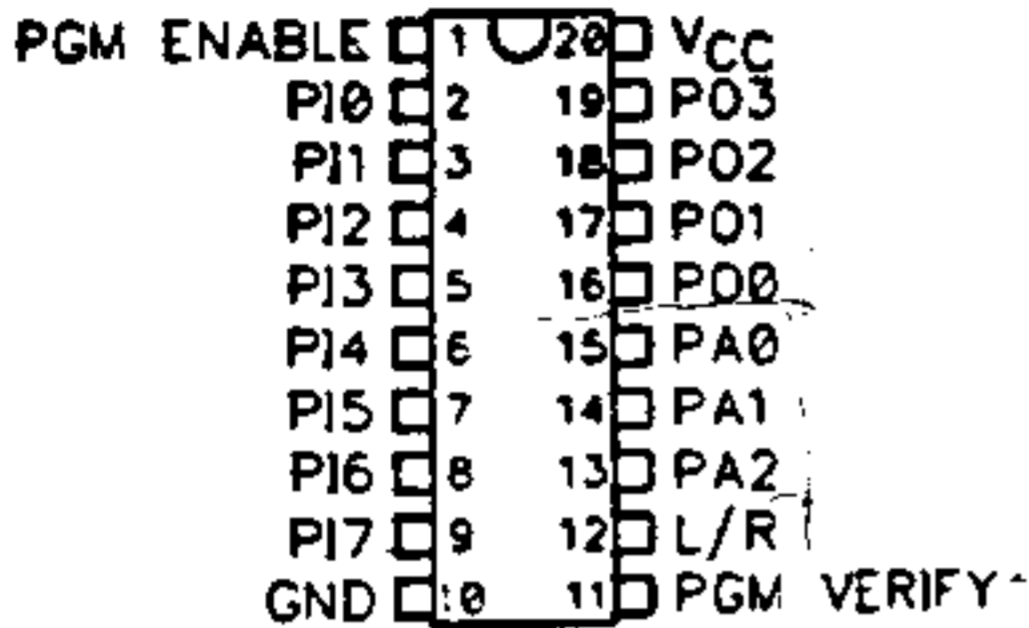
For Security Fuse programming see Figure 1-2.

PREPARED BY B. Cole TPAL16-1.DWG	DATE 09/22/86	TEXAS INSTRUMENTS		
CHECKED BY <i>Donald B. Shover</i>	DATE 04/12/88	TITLE: ALGORITHM SPECIFICATION TIBPAL16XX		
ENGINEER Jim Giddings	DATE 09/22/86			
APPROVED BY <i>Donald B. Shover</i>	DATE 04/29/88	REVISION C	A	PAL20002
RELEASED BY / /	DATE / /	LETTER C	SIZE A	SHEET 1 10

PIN ASSIGNMENTS IN PROGRAMMING MODE

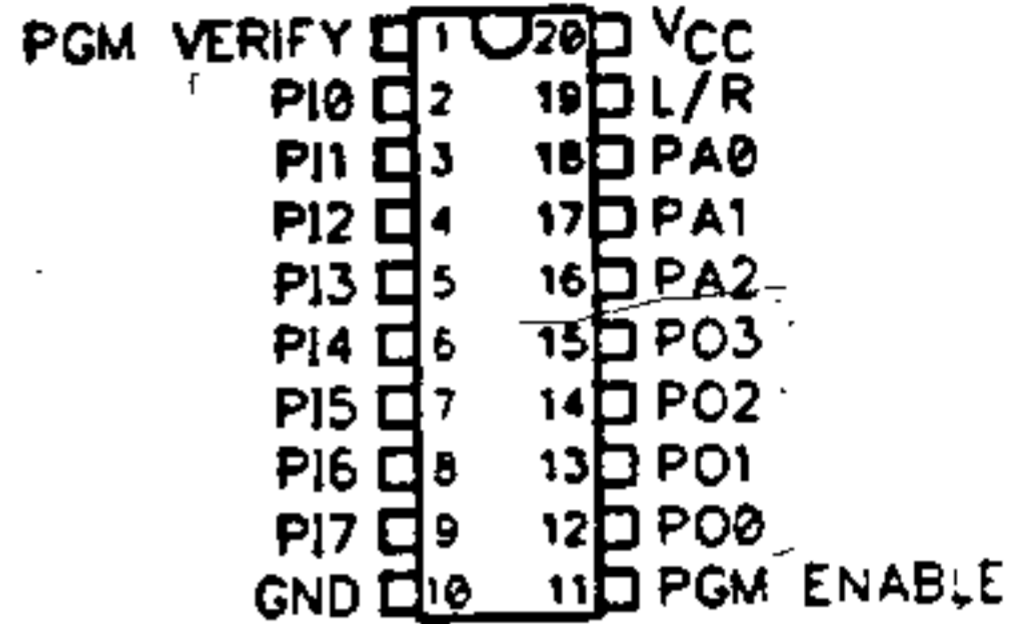
PRODUCT TERMS 0 THRU 31

(TOP VIEW)

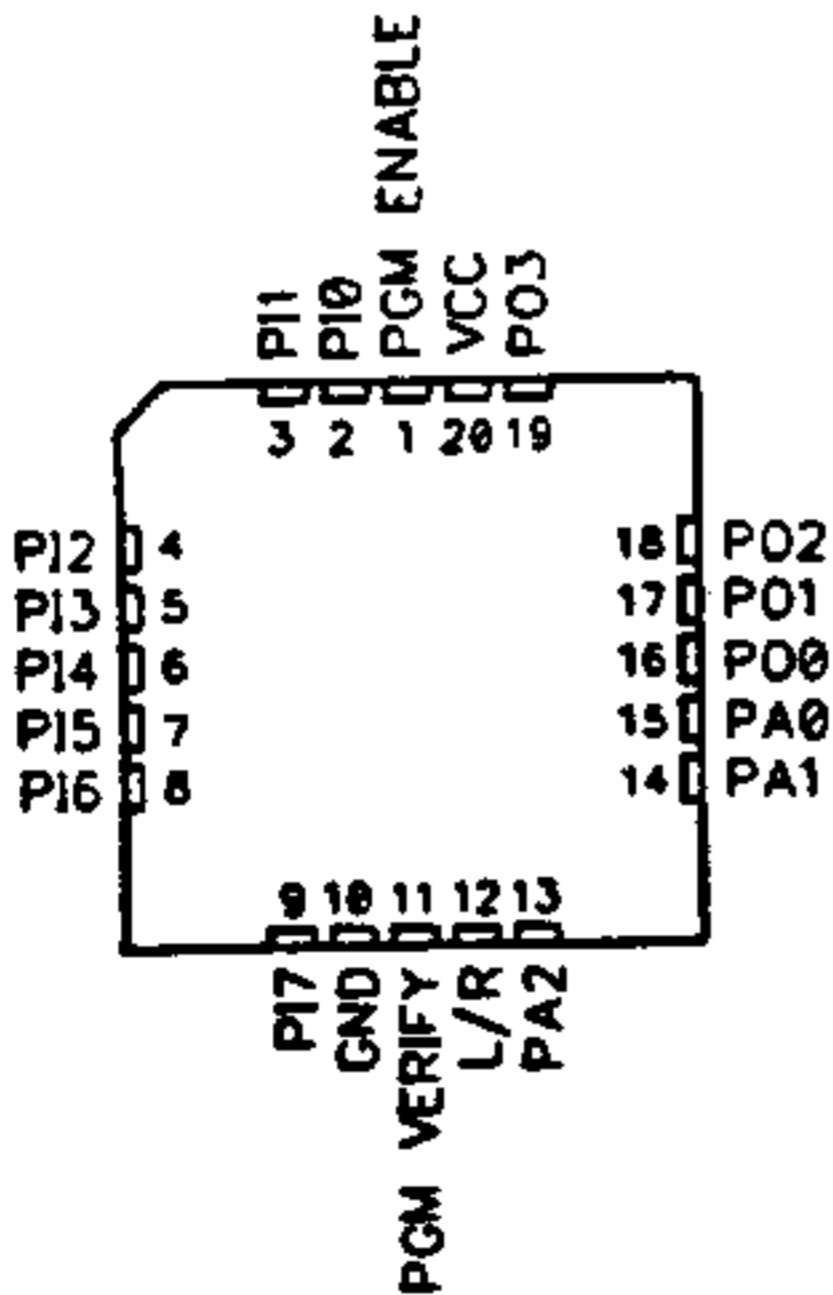


PRODUCT TERMS 32 THRU 63

(TOP VIEW)



(TOP VIEW)



(TOP VIEW)

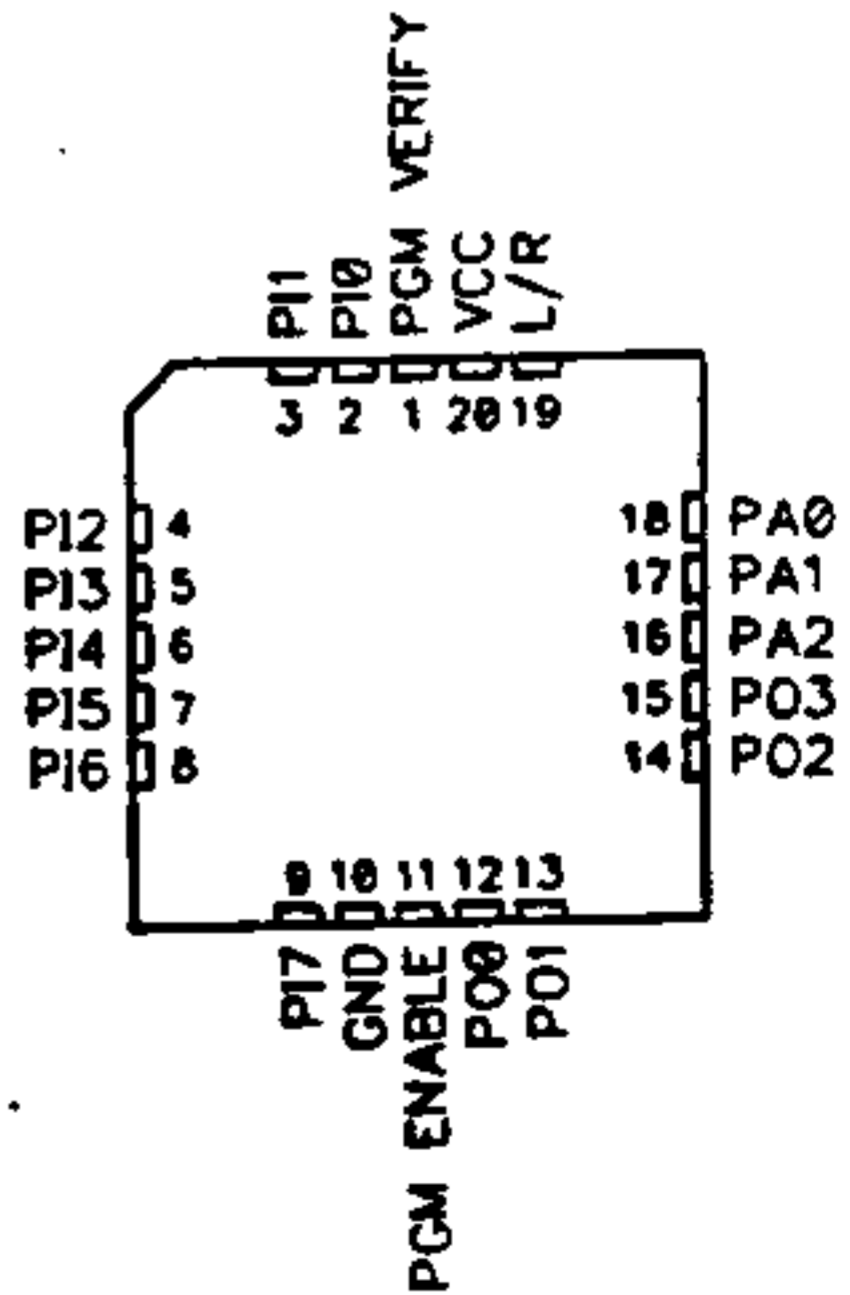


TABLE 1-1. PROGRAMMING PARAMETERS, TA = 25°C

PARAM	DESCRIPTION	MIN	NOM	MAX	UNIT
VCC	Verify-level supply voltage	4.75	5.00	5.25	V
V _{IH}	High-Level input voltage	2.40		5.50	V
V _{IL}	Low-level input voltage			0.50	V
V _{IHH}	Program-pulse voltage	10.25	10.50	10.75	V
V _{IHH}	Program-pulse voltage on PA pins during verify only	8.80	9.00	9.20	V
I _{IHH}	Program-pulse current		20	50	Ma
	PO		10	25	Ma
	PGM ENA, L/R		1.5	10	Ma
	PI, PA		250	500	Ma
	I _{CC}			50	Ma
t _{w1}	Program-pulse duration at PO	10		50	uS
	Prog.-pulse duty cycle, PO, VCC			25	%
t _{w2}	Pulse duration at PGM VERIFY	100			nS
t _{su}	Set-up time	100			nS
t _h	Hold time	100			nS
t _{d1}	Delay time from VCC to 5V to PGM VERIFY	100			uS
t _{d2}	Delay time from PGM VERIFY pulse to valid output	200			nS
	Voltage of pins 1 and 11 to open verify-protect (security) fuse	13.75	14.0	14.25	V
	current to open security fuse			400	Ma
t _{w3}	Security fuse pulse duration	20		50	uS
	VCC during security fusing		0	0.40	V

TABLE 1-2. INPUT/PRODUCT LINE SELECT

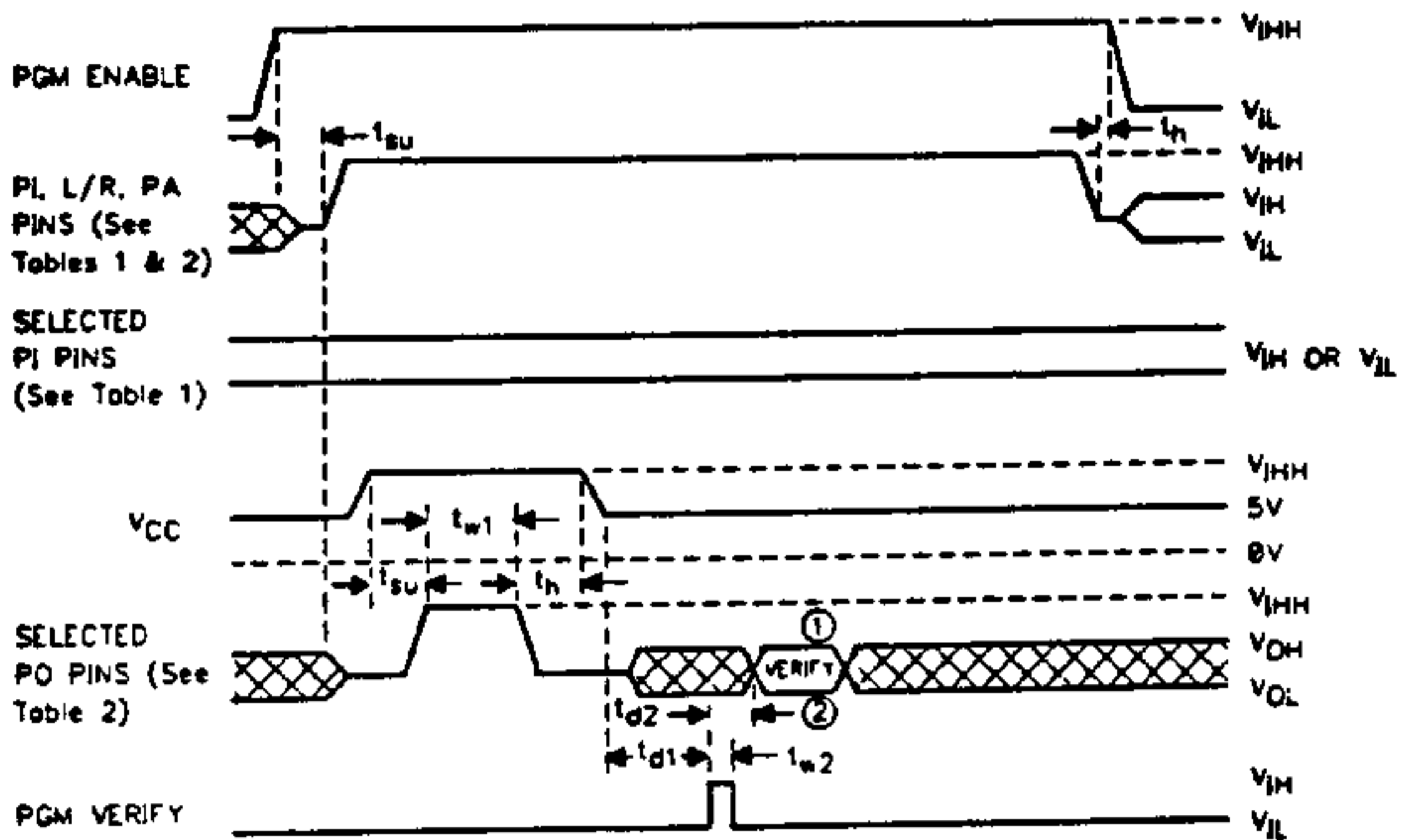
TABLE 1 - INPUT LINE SELECT

TABLE 2 - PRODUCT LINE SELECT

INPUT LINE NO.	PIN NAME									PRODUCT LINE NO.	PIN NAME						
	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	L/R		P00	P01	P02	P03	PA2	PA1	PA0
0	H	H	H	H	H	H	H	L	Z	0,32	Z	Z	Z	HH	Z	Z	Z
1	H	H	H	H	H	H	H	H	Z	1,33	Z	Z	Z	HH	Z	Z	HH
2	H	H	H	H	H	H	H	L	HH	2,34	Z	Z	Z	HH	Z	HH	Z
3	H	H	H	H	H	H	H	H	HH	3,35	Z	Z	Z	HH	Z	HH	HH
4	H	H	H	H	H	H	L	HH	Z	4,36	Z	Z	Z	HH	HH	Z	Z
5	H	H	H	H	H	H	H	HH	Z	5,37	Z	Z	Z	HH	HH	Z	HH
6	H	H	H	H	H	H	L	HH	HH	6,38	Z	Z	Z	HH	HH	HH	Z
7	H	H	H	H	H	H	H	HH	HH	7,39	Z	Z	Z	HH	HH	HH	HH
8	H	H	H	H	H	L	HH	HH	Z	8,40	Z	Z	HH	Z	Z	Z	Z
9	H	H	H	H	H	H	H	HH	HH	9,41	Z	Z	HH	Z	Z	Z	HH
10	H	H	H	H	H	L	HH	HH	HH	10,42	Z	Z	HH	Z	Z	HH	Z
11	H	H	H	H	H	H	H	HH	HH	11,43	Z	Z	HH	Z	Z	HH	HH
12	H	H	H	H	L	HH	HH	HH	Z	12,44	Z	Z	HH	Z	HH	Z	Z
13	H	H	H	H	H	H	HH	HH	Z	13,45	Z	Z	HH	Z	HH	Z	HH
14	H	H	H	H	L	HH	HH	HH	HH	14,46	Z	Z	HH	Z	HH	HH	Z
15	H	H	H	H	H	H	HH	HH	HH	15,47	Z	Z	HH	Z	HH	HH	HH
16	H	H	H	L	HH	HH	HH	HH	Z	16,48	Z	HH	Z	Z	Z	Z	Z
17	H	H	H	H	H	HH	HH	HH	Z	17,49	Z	HH	Z	Z	Z	Z	HH
18	H	H	H	L	HH	HH	HH	HH	HH	18,50	Z	HH	Z	Z	Z	HH	Z
19	H	H	H	H	H	HH	HH	HH	HH	19,51	Z	HH	Z	Z	Z	HH	HH
20	H	H	L	HH	HH	HH	HH	HH	Z	20,52	Z	HH	Z	Z	HH	Z	Z
21	H	H	H	H	H	HH	HH	HH	Z	21,53	Z	HH	Z	Z	HH	Z	HH
22	H	H	L	HH	HH	HH	HH	HH	HH	22,54	Z	HH	Z	Z	HH	HH	Z
23	H	H	H	H	H	HH	HH	HH	HH	23,55	Z	HH	Z	Z	HH	HH	HH
24	H	L	HH	HH	HH	HH	HH	HH	Z	24,56	HH	Z	Z	Z	Z	Z	Z
25	H	H	H	HH	HH	HH	HH	HH	Z	25,57	HH	Z	Z	Z	Z	Z	HH
26	H	L	HH	HH	HH	HH	HH	HH	HH	26,58	HH	Z	Z	Z	Z	HH	Z
27	H	H	H	HH	HH	HH	HH	HH	HH	27,59	HH	Z	Z	Z	Z	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	Z	28,60	HH	Z	Z	Z	HH	Z	Z
29	H	HH	HH	HH	HH	HH	HH	HH	Z	29,61	HH	Z	Z	Z	HH	Z	HH
30	L	HH	HH	HH	HH	HH	HH	HH	HH	30,62	HH	Z	Z	Z	HH	HH	Z
31	H	HH	HH	HH	HH	HH	HH	HH	HH	31,63	HH	Z	Z	Z	HH	HH	HH

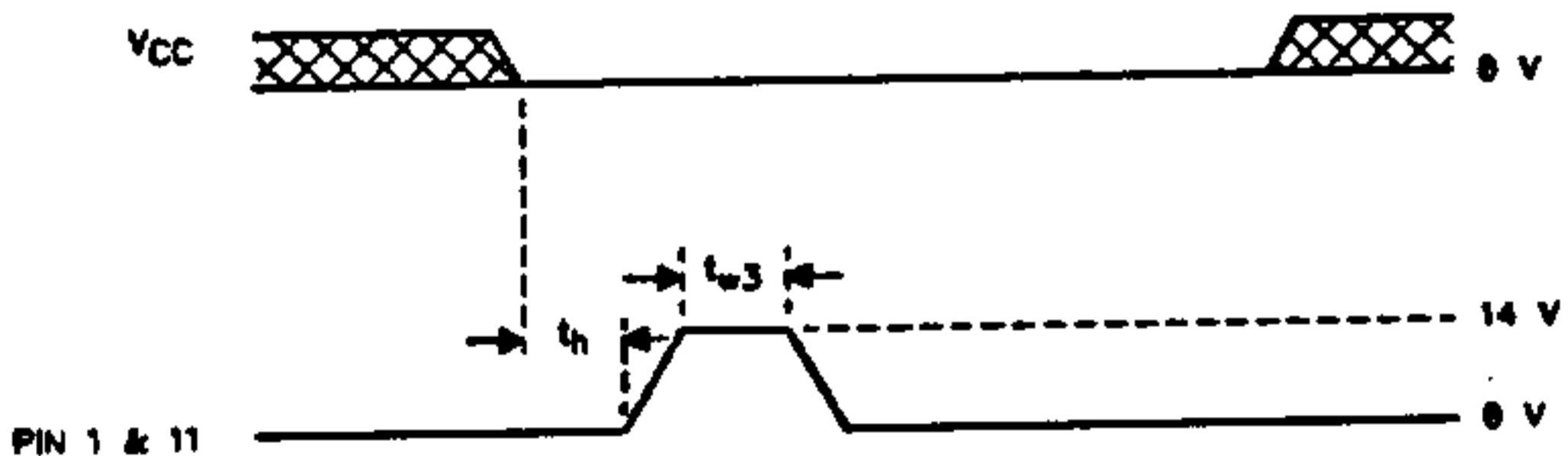
L = V_{IL} , H = V_{IH} , HH = V_{IHH} , Z = high impedance (e.g. 10 kΩ to 5V)

FIGURE 1-1, PROGRAMMING WAVEFORMS



- ① A high level during the verify interval indicates that programming has not been successful.
- ② A low level during the verify interval indicates that programming has been successful.

FIGURE 1-2, SECURITY FUSE WAVEFORMS



PROGRAMMING ALGORITHM TEMPLATE

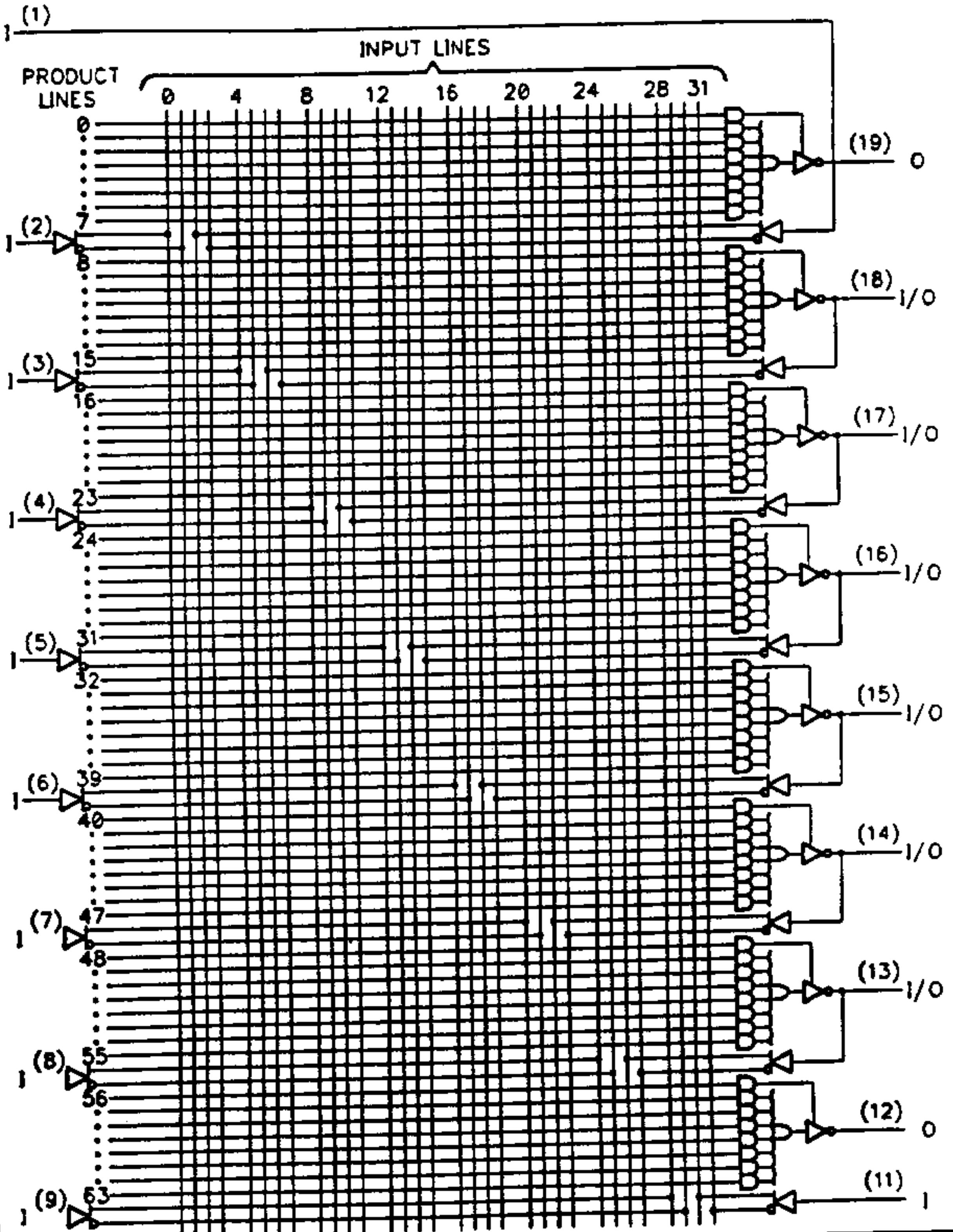
SPECIFICATION NUMBER PAL20002
DEVICE FAMILY TIBPAL16XX
INCLUDED DEVICES TIBPAL16L8,R4,R6,R8-12;15;25

PROGRAMMER INFO:

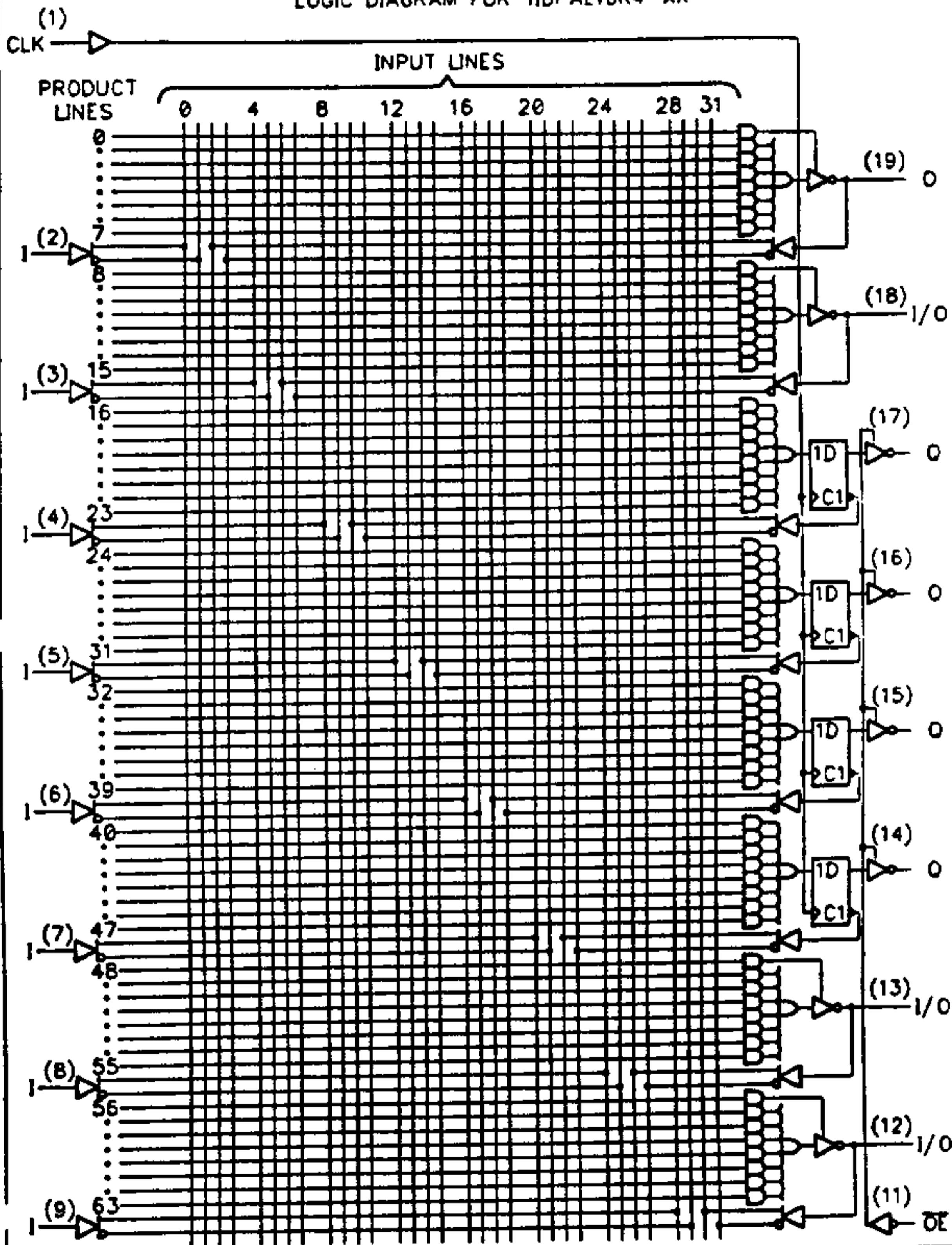
MANUFACTURER : _____ **MODEL:** _____ **ADAPTER #** _____
UPDATE VERSION : _____ **FW/SW P/N:** _____

PARAMETER	MIN	NOM	MAX	UNITS	ACTUAL
VCC - VERIFY LEVEL SUPPLY VOLTAGE	4.75	5	5.25	V	
VIH - HIGH LEVEL INPUT VOLTAGE	2.4		5.5	V	
VIL - LOW LEVEL INPUT VOLTAGE			0.5	V	
VIHH - PROGRAM-PULSE VOLTAGE (PG/EN)	10.25	10.5	10.75	V	
VIHH - PROGRAM-PULSE VOLTAGE (PI,L/R,PA)	10.25	10.5	10.75	V	
VIHH - PROGRAM-PULSE VOLTAGE (PO)	10.25	10.5	10.75	V	
VIHH - PROGRAM-PULSE VOLTAGE (VCC)	10.25	10.5	10.75	V	
VIHH - PROGRAM-PULSE ON PA PINS (VERIFY)	8.80	9.0	9.20	V	
tw1 - PROGRAM PULSE WIDTH AT PO	10		50	us	
tw2 - PGM VERIFY PULSE WIDTH	100			ns	
td1 - DELAY TIME (VCC (5V) TO PGM VERIFY)	100			us	
tsu - SET UP TIME (PG/EN-PI,L/R,PA)	100			ns	
tsu - SET UP TIME (VCC-PO)	100			ns	
th - HOLD TIME (PG/EN-PI,L/R,PA)	100			ns	
th - HOLD TIME (VCC-PO)	100			ns	
th - HOLD TIME -SECURITY (VCC-PIN1&11)	100			ns	
tw3 - SECURITY FUSE PULSE (PIN 1)	20		50	us	
tw3 - SECURITY FUSE PULSE (PIN 11)	20		50	us	
- SECURITY FUSE VOLTAGE (PIN 1)	13.75	14	14.25	V	
- SECURITY FUSE VOLTAGE (PIN 11)	13.75	14	14.25	V	

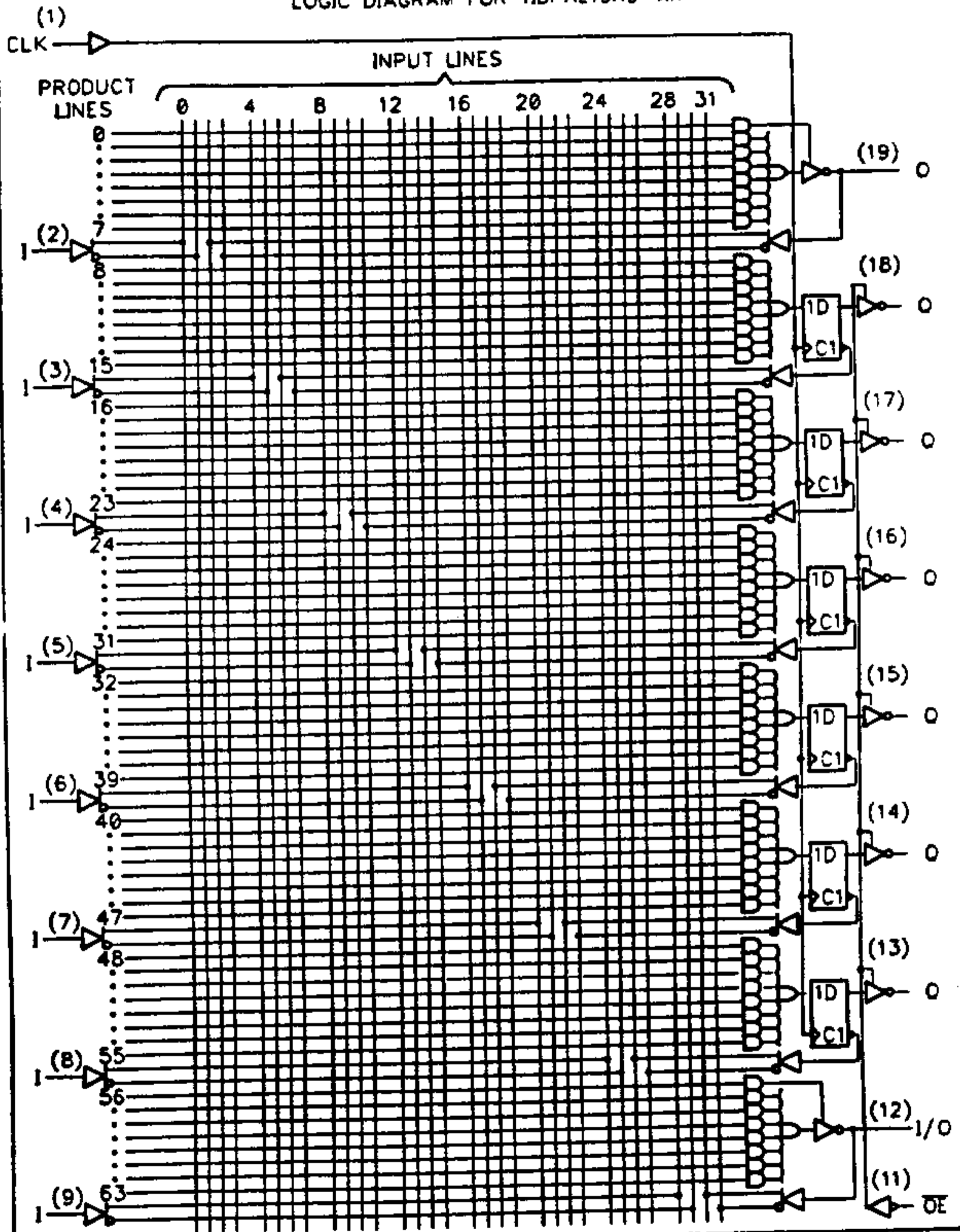
LOGIC DIAGRAM FOR TPAL16LB-XX



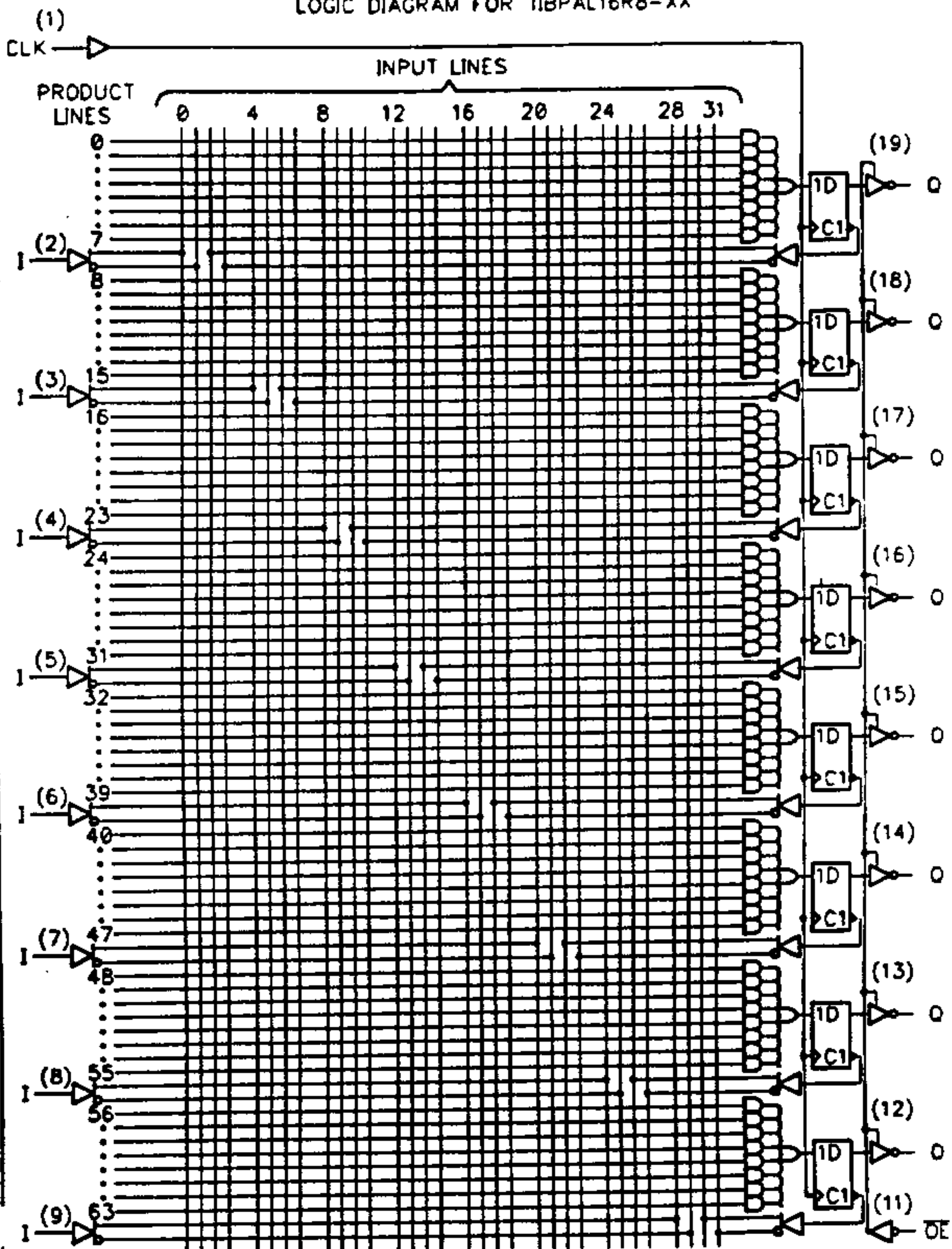
LOGIC DIAGRAM FOR TIBPAL16R4-XX



LOGIC DIAGRAM FOR T1BPAL16R5-XX



LOGIC DIAGRAM FOR TIBPAL16R8-XX



REVISION HISTORY

REVISION LTR.	DATE	ENGINEER	DESCRIPTION OF CHANGES
A	09-86	Michol	V _{CC} during verify to 5V only. V _{IH} min. to 2.4V. V _{IL} max to .5V. Return V _{IHH} to 10.5V. V _{IHH} on PA pins to 9V during verify.
B	06-87	Thomas	Table 1-1. Changed security fuse programming voltage to 14.0 V. Figure 1-2. Changed pin 1 to pins 1 and 11. Changed 21 V to 14.0 V. Deleted last waveform
C	03-88	Thomas	Added PLCC pinouts, Page 2. Added V _{CC} = 4.75 volts, Min. Added V _{CC} = 5.25 volts, Max.