SPWU001D

TMS380 Adapter Chipset User's Guide

Local Area Network Products

TEXAS INSTRUMENTS

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MANUAL REVISION HISTORY
TMS380 ADAPTER CHIPSET USER'S GUIDE

Document Release	Date	Software Release
Original Issue User's Guide	September 1985	RC0114
Manual Update A	October 1985	RC0114
Manual Update B	January 1986	RC011B
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The Adapter software release number may be found in the first location of the code (mapped at LAN Adapter bus address >C000). This corresponds to the first word of the PH ROM or the first word of external EPROM, if used.

Adapter software release RC011B has been fully tested by IBM and TI and is compatible with IEEE 802.5 and the IBM Token-Ring Network Architecture Reference, part number 6165877, February 1986.

Illustrations

The 16K bytes of on-chip software supports highly reliable token ring operation, extensive LAN management services, and thorough self-test diagnostics. The TMS380 chipset meets the critical requirements of LAN connections for 16- and 32-bit desktop workstations by supplying a high performance LAN adapter with reduced chip count, low power dissipation, and minimal use of circuit card area. The TMS380 LAN adapter chipset has been rigorously verified by Texas Instruments and IBM to provide a compatible foundation for OEMs and end users to build long-term LAN solutions with confidence.

The TMS380 chipset is fully supported with development tools, applications information, documentation, and courses through Texas Instruments' Regional Technology Centers.

1.2 The OSI Reference Model

The Open Systems Interconnection (OSI) model is a conceptual network structure defined by the International Organization for Standardization. The purpose of the OSI model is to promote the development of worldwide data-communications standardization.

Networks are partitioned into a series of layers to reduce their design complexity. These layers are hierarchical with each layer built upon its predecessor, thus shielding each layer from the details of how the services from the other layers are implemented. The OSI model is partitioned into seven layers. The bottom four layers of the model define the network and how it functions, and the top three layers define how the network is used. The seven-layer OSI model is shown below.

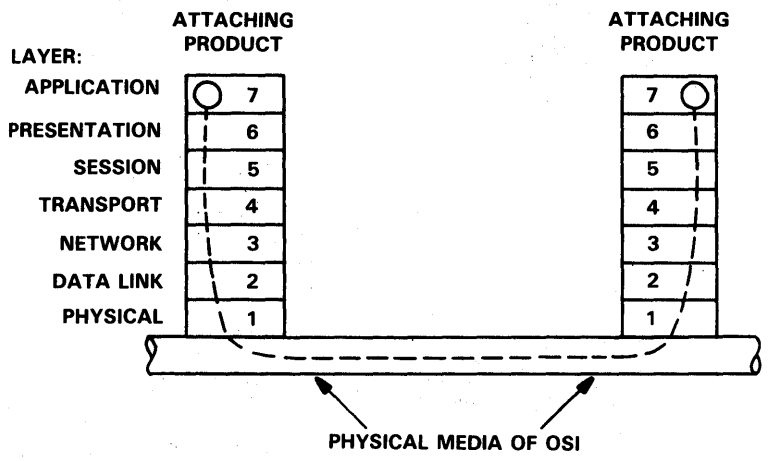


FIGURE 1-2. THE OSI REFERENCE MODEL

The illustration shows the relationship of the seven layers to one another and the path taken by communication between two attaching products.

The functions of the layers are described here in order, starting with the lowest.

- The **Physical** layer defines the mechanical and electrical connection.
- The **Data Link** layer defines the way data is formatted for transmission and how access to the network is controlled. This layer has been separated by the IEEE 802 standards committee into two sublayers: the Medium Access Control (MAC) sublayer and the Logical Link Control (LLC) sublayer. (The MAC sublayer is discussed in more detail in the next section.)

An adapter card, based on the TMS380 chipset, is used to attach products to the network. The adapter card enables connection to the network through twisted wire-pairs, referred to as a **lobe.**

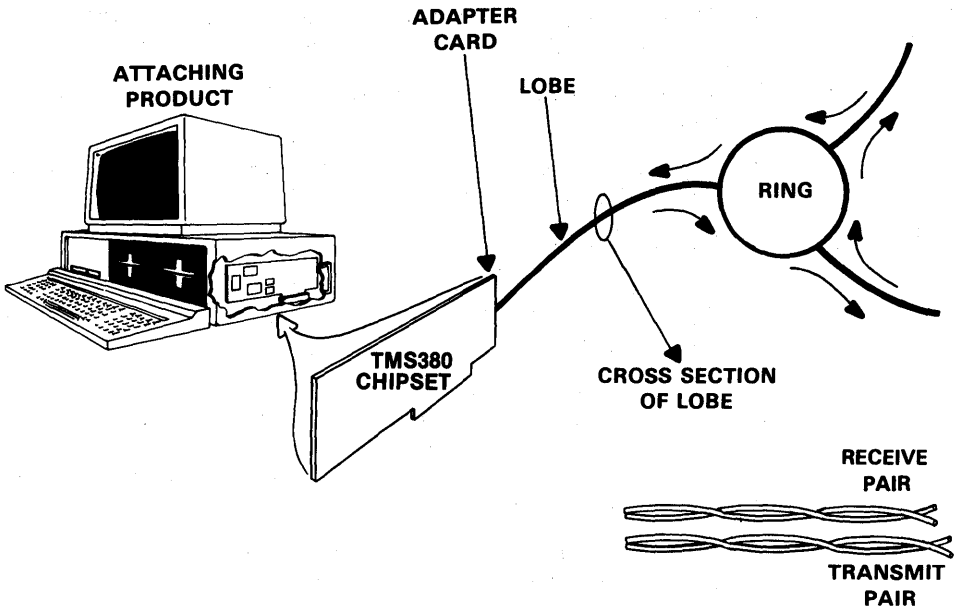


FIGURE 1-4. THE STAR-WIRED RING TOPOLOGY

The lobe connects to the ring through a wiring concentrator as shown in the illustration on the next page. In its basic form, a wiring concentrator consists of bypass relays that are normally closed, but which are switched on when an attaching product is inserted into the ring or switched off when an attaching product is de-inserted from the ring.

Each adapter card provides the insertion control to drive the relay for inserting into the ring. Products not powered on or lobes that have been damaged and cannot provide the insertion signal to the wiring concentrator are not inserted in the ring. This central concentration of the cable permits the star-wired ring LAN to be easily reconfigured, expanded, and diagnosed for problems.

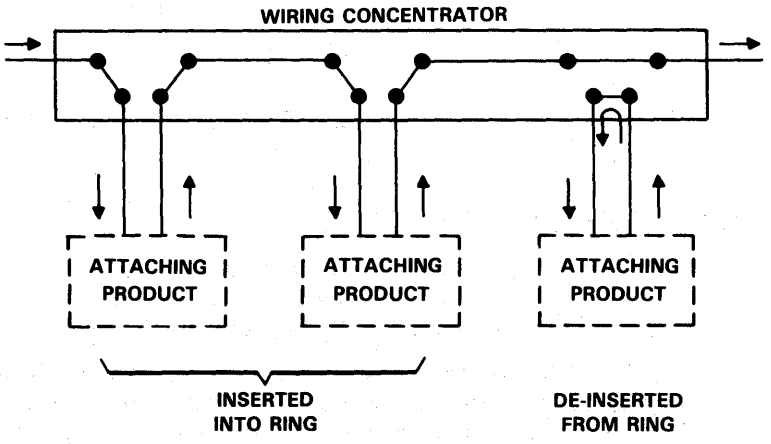


FIGURE 1-5. TOKEN RING WIRING CONCENTRATOR

1.5 LAN Adapter Architectures

As LANs evolved from the laboratory to the marketplace, designers recognized the importance of minimizing a LAN's overhead burden on the host system. To achieve this goal, autonomous adapter architectures were designed by adding a dedicated central processing unit (CPU), memory, and support circuits to the LAN attachment card.

Autonomous adapter architectures, as opposed to controller-based architectures with no CPU on the adapter card, are the dominant LAN design approach used today. However, because early LSI chips were targeted at LAN controller-based architectures, card designers were forced to use more chips and expend extra design effort to build an adapter card. Typical adapter cards designed around LAN controllers require a general-purpose microprocessor, RAM for buffering data, ROM for the protocol software and diagnostics, interface circuits for connecting to the media, an interface for connecting to the host system bus, and various glue circuits, as illustrated below.

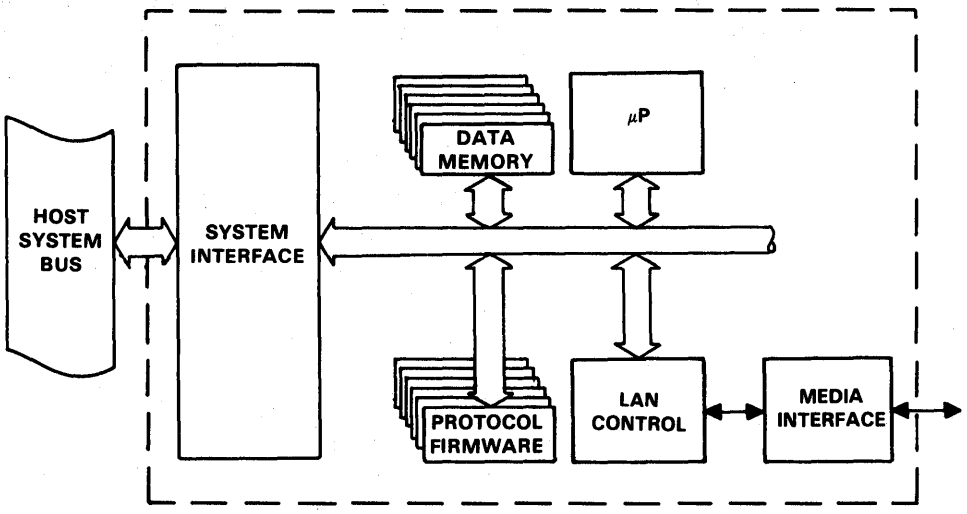


FIGURE 1-8. LAN CONTROLLER-BASED ADAPTER CARD ARCHITECTURE

The LAN controller-based approach to adapter card design suffers from high part count, high power dissipation, and wasteful use of printed circuit board area. More important, a fundamental drawback of the controller-based approach is that different adapter card designs, even those using the same LAN controller chip, do not necessarily work together on the same network. This places the burden of verifying compatibility with each card manufacturer, and eventually on the end user.

1.6.1 The System Interface

The TMS38030 System Interface (SIF) chip provides up to 40 megabits per second of data to the host system via DMA bus master transfers. The host system bus interface is selectable for two types of memory organization and control signals:

- 8-, 16-, and 32-bit members of the iAPX86 and Series 32000 microprocesor families
- 16- and 32-bit members of the 68000 microprocesor family

The System Interface is controlled through command blocks with a high-level command structure; for example, commands include TRANSMIT, RECEIVE, and READ ERROR LOG. (Additional details on SIF commands are provided with the examples in "Transmitting and Receiving a Frame.") The System Interface has a 24-bit address reach into the host system and a "scatter write-gather read" DMA feature that allows discontiguous memory blocks to be transferred and received via linked lists. Programmable burst transfers or cycle-steal operation and optional parity protection allow system designers to customize the TMS38030 to their particular bus.

1.6.2 The Communications Processor

The TMS38010 Communications Processor (CP) contains dedicated 16-bit CPU with 2.75K bytes of on-chip RAM. The Communications Processor executes the adapter software contained within the TMS38020. The on-chip RAM buffers the frames being transmitted and received. This high-performance CPU provides single-cycle arbitration of the 3 MHz LAN adapter bus for maximum adapter throughput. Up to 42K of expansion memory can be added to the LAN adapter bus. All on-chip RAM and expansion memory is parity protected.

1.6.3 The Protocol Handler

The TMS38020 Protocol Handler (PH) performs hardware-based protocol functions for a 4-megabit per second token ring LAN compatible with the IEEE 802.5 standard. An on-chip ROM contains 16K bytes of adapter software executed by the Communications Processor. This software supports reliable ring operation, LAN management services, and thorough diagnostic coverage of the adapter chipset.

The Protocol Handler implements differential Manchester encoding and decoding and frame-address recognition (group, specific, and functional). The Protocol Handler also contains state machines that capture tokens, transmit and receive frames, manage the adapter chipset buffer RAM, and provide token-priority controls.

Four DMA channels, two for transmit and two for receive, ensure high-speed frame transfer between the ring and the adapter's buffer RAM. Integrity of transmitted and received data is assured by cyclic redundancy checks (CRC), detection of differential Manchester code violations, and parity on internal data paths. All data paths and registers are parity-protected to assure functional integrity.

1.6.4 The Ring Interface

The TMS38051 and TMS38052, collectively the Ring Interface, are the Ring Interface Transceiver and Ring Interface Controller. These chips contain the digital and analog circuitry to connect the adapter chipset to a 4-megabit per second token ring LAN through separate receive and transmit channels.

The Ring Interface provides the clock for the ring when in active monitor mode and contains a phase lock loop for clock recovery, data detection, and phase alignment. The Ring Interface also provides the phantom drive signal to a wiring concentrator, a loop-back path for diagnostic testing, and error detection of wire faults.

The TMS380 adapter chipset also has the capability to allow the LAN to recover from soft errors and hard errors with minimal disruption to service. Soft errors, such as corrupted or lost tokens, are automatically handled by the adapter chipsets on the LAN. The adapter chipset that detects the error logs the condition and the LAN automatically recovers. The error condition and location is then reported to the host system and a network manager. Hard errors, such as a wire fault on the lobe or a bad receiver/transmitter on the adapter card, are also automatically isolated and resolved by the adapters on the LAN. These isolation and recovery processes are performed by the adapter chipset independent of the host system.

1.8 LAN Management Services

The TMS380 adapter chipset contains a wealth of LAN management services to build and manage reliable networks. These services are embedded in the chipset and operate independently of the attaching product.

The availability of a standard set of services enables vendors to build network management products that will operate with products independently developed by other manufacturers. Because these services are embedded in the adapter chipset, end users can confidently expand the network as requirements grow, without affecting the installed products.

The TMS380 LAN management services are provided by MAC frames that are exchanged between adapters on the ring. MAC frames are special frames that are used to control the operation of the ring; they do not transfer data.

The IEEE 802.5 standard defines six MAC frames that are used for basic ring operation. In addition to these six basic MAC frames, the TMS380 also contains MAC frames that are used with specified functional addresses on the LAN. There are over 20 MAC frames used to collect error reports automatically generated by adapter chipsets, monitor and modify the configuration of the LAN, and assign operating parameters to attached products.

The MAC frames processed by the TMS380 adapter chipset are listed below.

Response
Beacon
Ring Purge
Standby Monitor Present
Lobe Media Test
Change Parameters
Request Station Adress
Request Station Attachment
Request Initialization
Report Station State
Report Station Attachment
Report SUA Change
Report Monitor Error
Claim Token
Active Monitor Present
Duplicate Address Test
Transmit Forward
Remove Ring Station
Initialize Ring Station
Request Station State
Report Transmit Forward
Report Station Address
Report New Monitor
Report Ring Poll Failure
Report Error

1.9 Performance Features

LAN performance, as measured in user response time, is dependent on three factors: the physical data transfer rate and delays caused by the access protocols, the movement of data from the physical medium to the host system, and the efficiency of the host-based protocol software. The TMS380 adapter chipset provides features in all three of these areas.

During adapter chipset initialization, a host system configures the adapter interface. The adapter chipset can be initialized to match specific host system bus requirements. Examples of the initialization parameters include: interrupt conditions and frequency, buffer sizes and allocation of these buffers to either transmit or receive channels, expansion memory, and the setting of addresses. Command and status information is passed between the adapter and host system via two control blocks:

- System Command Block (SCB)
- System Status Block (SSB)

To transmit a frame, the host system first interrupts the adapter chipset. The adapter then DMA reads the System Command Block. The SCB contains the transmit command and the starting address of the transmit list that resides in host system memory. The adapter chipset then transfers the transmit list from the host system to the adapter's buffer RAM using DMA. Next, the adapter transfers the entire frame to the adapter RAM, and the adapter chipset captures a token and transmits the frame onto the LAN. The frame will circulate to the destination address, which copies the data and returns the frame to circulate on the LAN. When the frame returns to the originating adapter chipset, it is stripped and a token is released. The System Status Block is updated by the adapter and transferred to the host system.

This procedure is illustrated on the following page.

1.12 TMS380 User's Guide Organization

This User's Guide provides information about the TMS380 LAN adapter chipset for hardware and software engineers, network planners and architects. The hardware engineer will find the Application Examples in section 2, portions of Adapter Design in section 4, and the Data Sheets in Appendix A particularly useful. Software engineers should focus on Communications Services in section 3, portions of Adapter Design in section 4, and the Appendices. The network planner and architects should review portions of the entire User's Guide.

Section 2. Application Examples: This section contains examples of adapter card designs using the TMS380 adapter chipset. Design examples include an adapter card for IBM PC family (8 bit), a PC AT card, and 680XX-family interface example.

Section 3. Communications Services: This section describes the architecture, operation and services provided by the TMS380 adapter chipset as it relates to the Physical and Medium Access Control (MAC) layers, network management and security services, and error reporting.

Section 4. Adapter Design: This section describes the hardware and software interface as viewed from the host system, the ring interface, and the LAN adapter bus.

Section 5. Appendices: Appendix A contains data sheets on all the chips. Appendix B.1 contains a summary of the Medium Access Control (MAC) frames. Appendix B.2 illustrates a technique for implementing a 'burned in' address. Appendix B.3 contains ordering information and package mechanical data, followed by a Glossary of Terms in Appendix B.4.

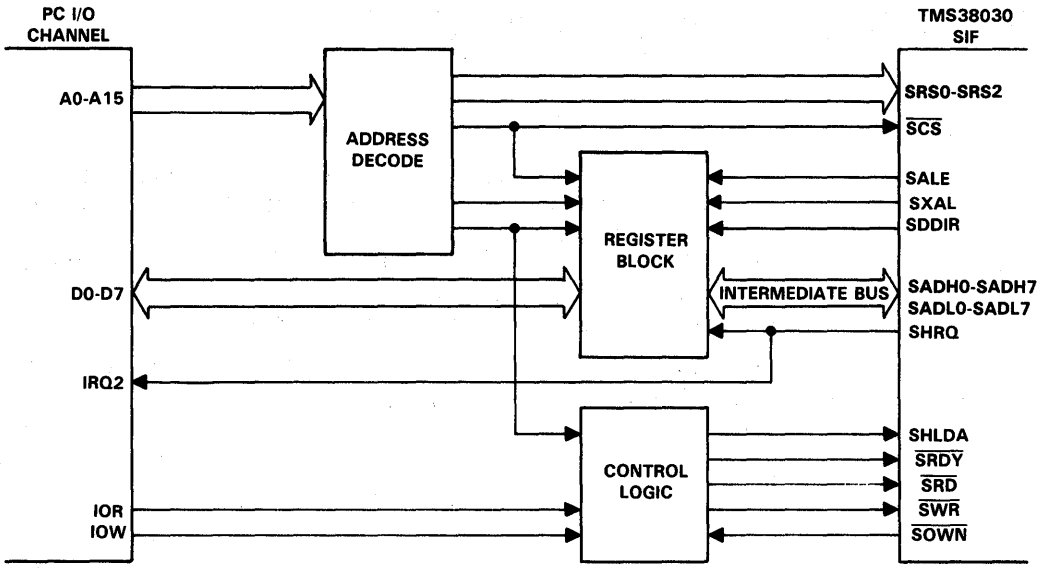


FIGURE 2-1. I/O MAPPED DESIGN BLOCK DIAGRAM

Data transfer between the PC and the LAN adapter card is a two-step process. The first step involves the transfer of a data byte to an external data register. During a data transfer from the Adapter to the PC, the TMS38030 writes data to this external register. During a data transfer from the PC to the Adapter, the PC writes data to the external register.

The second step involves reading the external data register by either the PC or the Adapter, depending on the direction of the transfer.

This two-step approach allows the PC to control its system bus while the TMS38030 controls an intermediate bus connected to the register block.

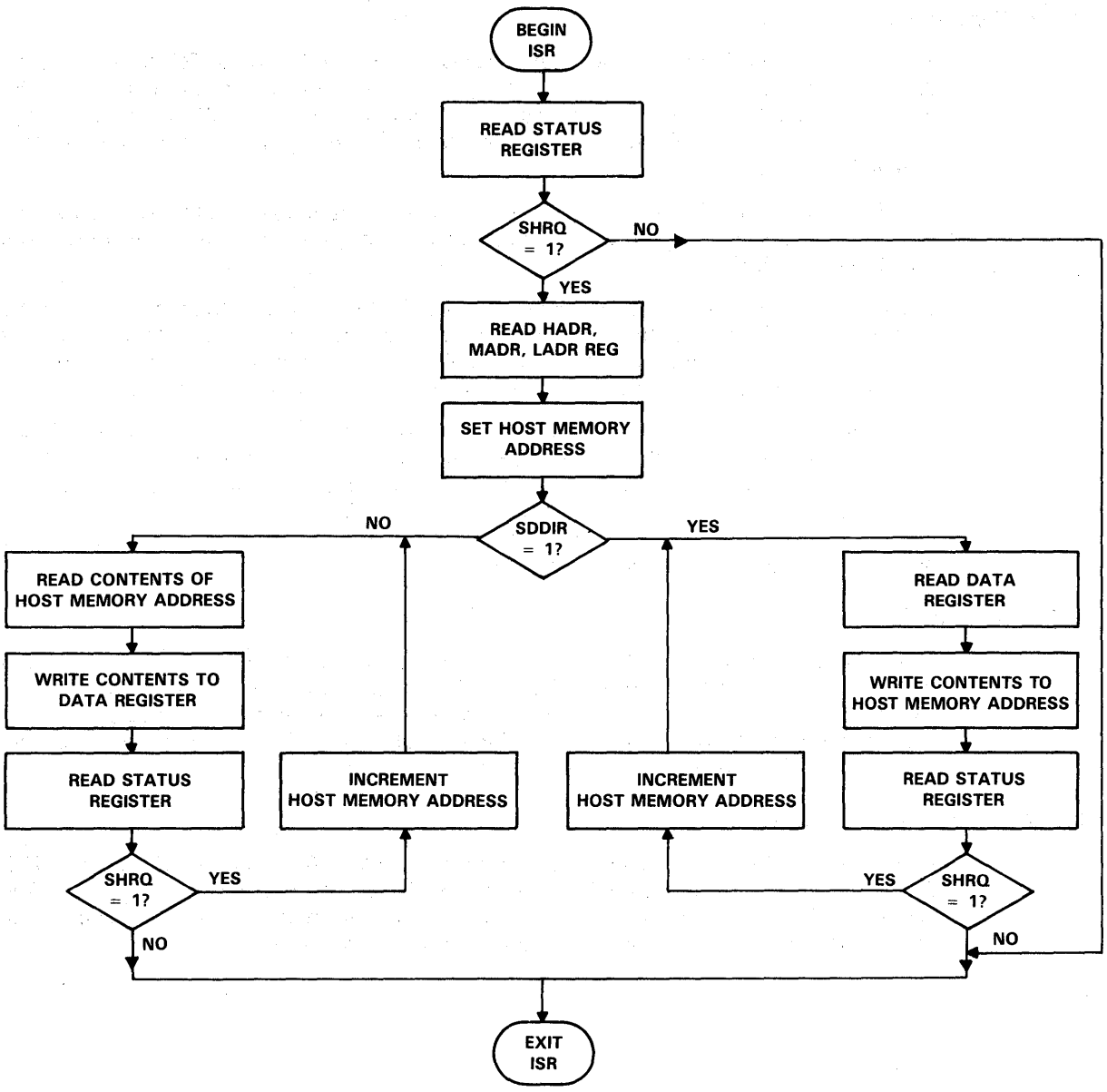


FIGURE 2-2. INTERRUPT SERVICE ROUTINE FLOWCHART — I/O MAPPED EXAMPLE

2.3.1.1 DMA Length Register

The length of DMA transfers is provided to the host bus by mapping the TMS38030's SDMALEN (System DMA Length) register, on the LAN Adapter bus, to a read-only register accessible to the PC CPU. This register is shown in the block diagram in Figure 2-3.

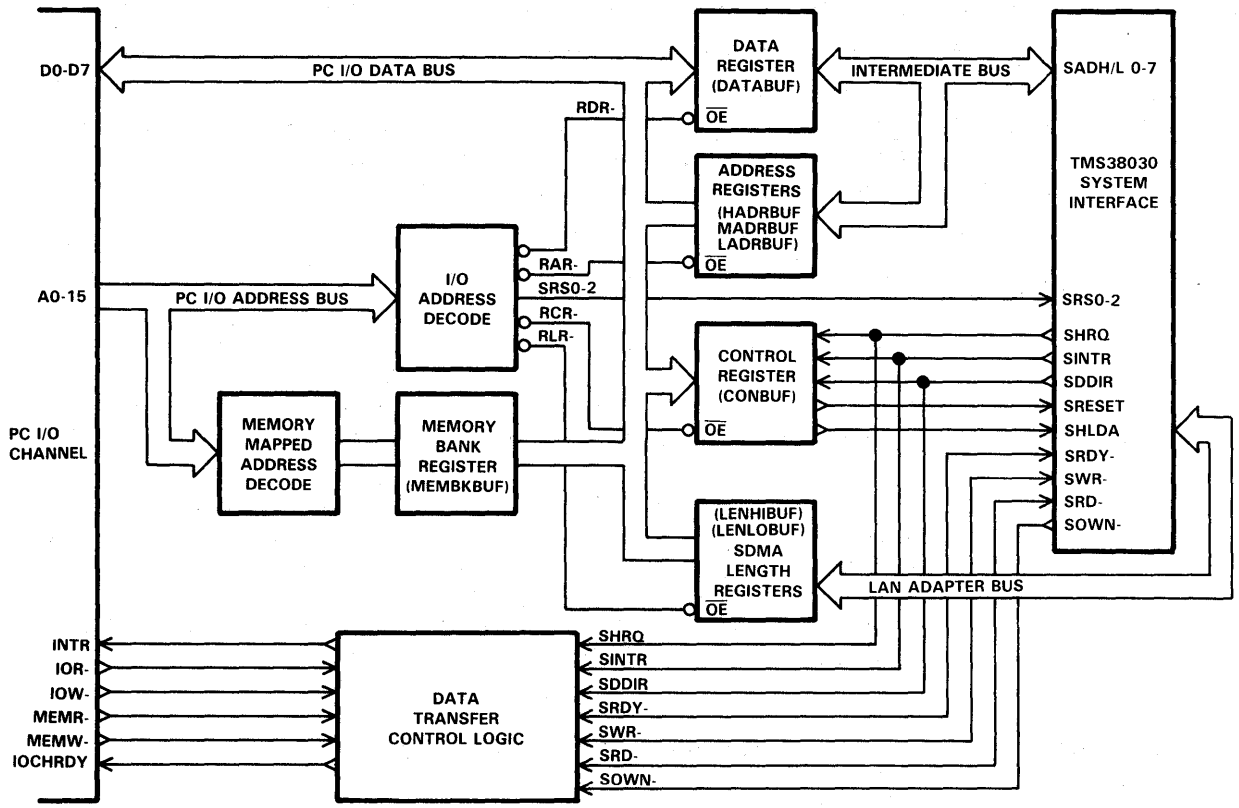


FIGURE 2-3. MEMORY MAPPED DESIGN BLOCK DIAGRAM

When the TMS38030 is initialized for a DMA transfer by the TMS38010 Communications Processor, the SDMALEN register will be loaded with the length of the transfer. This action, the TMS38010 writing to the SDMALEN register, will result in the read-only host bus register also being loaded. Thus, the PC CPU may read the length of the transfer for use by the string move instruction.

2.3.1.2 Memory Mapped Data Register

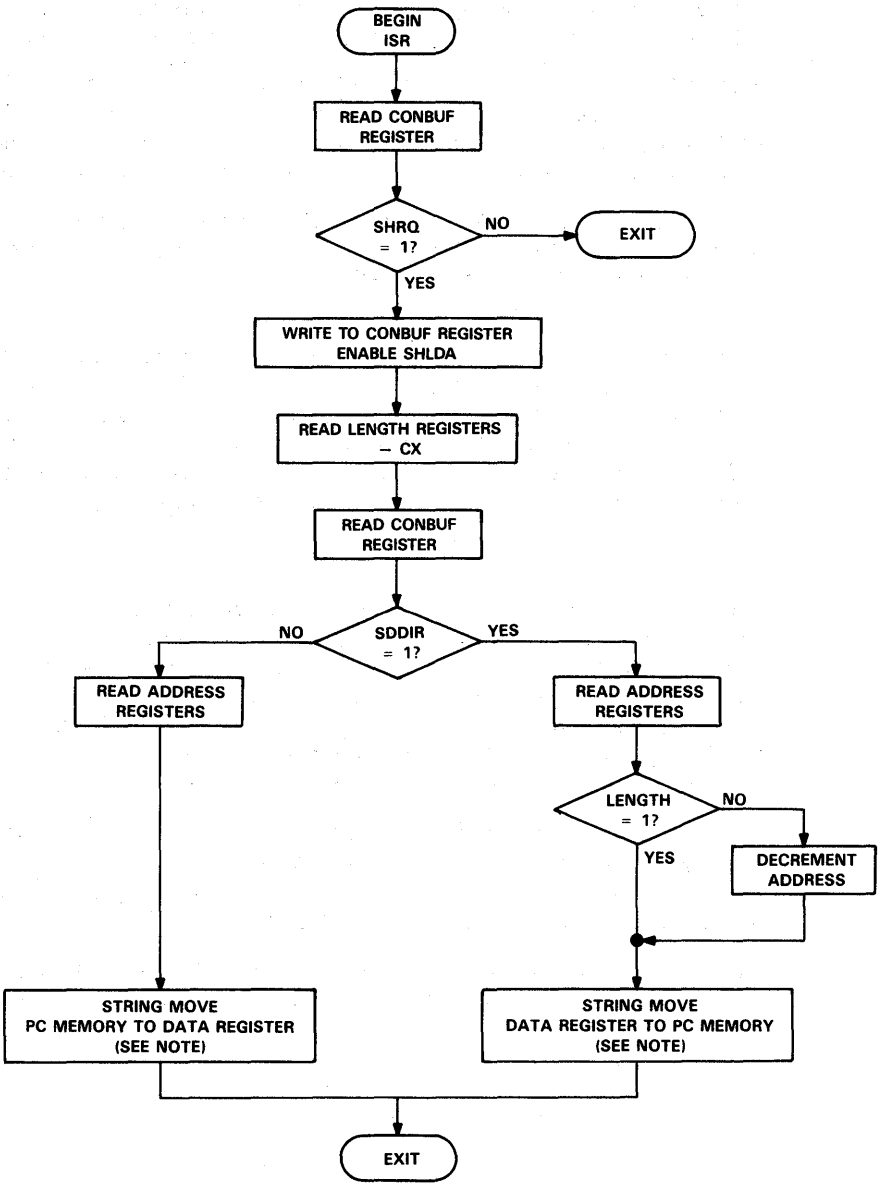
Like the I/O mapped example provided in Section 2.2, data transfer between the PC and the LAN adapter card is a two-step process. The first step involves the transfer of a data byte to an external data register. During a data transfer from the Adapter to the PC, the TMS38030 writes data to this external register. During a data transfer from the PC to the Adapter, the PC writes data to the external register.

The second step involves reading the external data register by either the PC or the Adapter, depending on the direction of the transfer.

This data register is mapped into the memory map of the PC so that a string move instruction may be used. This differs from the I/O mapped design example which described the data register residing in the I/O map of the PC. Using a string move instruction in lieu of input and output instructions reduces the number of bus cycles required to move a block of data thus increasing the overall bus throughput. This memory-mapped register is shown in Figure 2-3.

2.3.1.5 Interrupt Service Routine

When the TMS38030 begins a DMA transfer, the TMS38030 first takes SHRQ (hold request) active. This signal is fed into one of the PC's IRQ (interrupt request) signals. This causes the PC to be interrupted, and execution of an interrupt service routine is started. A flowchart of this interrupt service routine is shown in Figure 2-4.



NOTE: The string move instruction automatically increments the source and destination addresses for each byte until the CX register is decremented to zero.

FIGURE 2-4. INTERRUPT SERVICE ROUTINE FLOWCHART — MEMORY MAPPED EXAMPLE

2.4.1.3 Direct Memory Access

A DMA operation requires that the TMS38030 acquire control of the host system bus. The TMS38030 requests bus control by asserting SHRQ high, which corresponds to DRQ6 asserted on the host system bus. The host processor acknowledges the request by asserting DACK6 which is inverted in U9, the GLUE PAL, and presented to SHLDA of the TMS38030. Upon receiving SHLDA, the TMS38030 responds by asserting SOWN low, indicating bus ownership. SOWN acts to turn on the address transceivers U4, U6, and U7, and asserts MASTER, indicating to the host processor that the TMS38030 has control of the host system bus. SOWN also properly configures U5 for DMA signal directions. Upon gaining bus control, the TMS38030 drives SDDIR to provide proper direction of the data transceivers U3 and U4. On the first DMA cycle, the TMS38030 drives 24 bits of address with the highest byte latched by SXAL into U4. The middle and lower bytes are latched by SALE into U6 and U7, respectively. The TMS38030 asserts SRD or SWR depending upon whether a read or write transfer is in progress; these signals map to MEMR and MEMW through U5. The TMS38030 then asserts SDBEN to enable data transceivers U2 and U3. The cycle completes normally, unless wait states are inserted into the cycle by some system slave device deasserting IOCHRDY low. Ensuing cycles continue in the same manner; however, the highest address byte is not changed unless an address carry occurs from the low-order byte into the middle byte. The 74ALS161A synchronous 4-bit counter (U11) provides a hardware-based mechanism to limit DMA burst size to 15. This is necessary to allow periodic PC AT RAM refresh to occur. The counter will count 15 SALE transitions before asserting SBRLS. When SBRLS is asserted, the TMS38030 will relinquish control of the PC bus and will take SOWN inactive high. When SOWN goes high, the counter will be reset. The TMS38030 will immediately re-request the PC bus (assert SHRQ) following release of the bus. This hardware-based burst-size control offers a performance advantage over software-based burst size parameters passed during Adapter initialization. See Section 2.6 for a discussion of these performance issues.

To relinquish the host system bus, the TMS38030 deasserts SHRQ, tri-states its driven I/O signals and deasserts SOWN. This deasserts DRQ6 and MASTER of the host system bus, indicating that the bus is free.

2.4.1.4 Interrupt and Reset

The TMS38030 requests an interrupt by asserting SINTR high, which drives IRQ6 high indicating an interrupt request to the host system processor. The host processor clears the interrupt by writing a zero to the ninth most-significant-bit of the Interrupt Register.

The Adapter can be reset when the host processor asserts RESET DRV, which activates SRESET of the TMS38030.

2.5 68000 Bus Interface Example

This example illustrates an interface between the TMS38030 System Interface and a 68000-style bus. Because the TMS38030 provides a pin-strap selectible 680XX-type bus mode, this interface is implemented with a minimum of interface components. The performance of this interface is dependent upon the system bus throughput capability, but can approach 40 megabits-per-second from the Adapter to host memory. Because the 68000 does not have a multiplexed address/data bus, the address and data bus from the TMS38030 are de-multiplexed prior to presentation to the 68000 system bus. This example illustrates address/data bus demultiplexing using the bus control signals provided by the TMS38030 System Interface (SIF).

2.5.1 Theory of Operation

2.5.1.1 SIF Configuration

The TMS38030 is configured in 680XX mode by applying logic low to pin SI/$\overline{M}$. In this mode, the TMS38030 provides a 16-bit data path and 24 bits of address capable of addressing up to 16 megabytes of memory.

2.5.1.2 Bus Control

During DMA, addresses and data are multiplexed over the SAD lines of the TMS38030 requiring three 8-bit latches (74ALS373) and two transceivers (74ALS245) to demultiplex the address and data, as shown in Figure 2-6. The transceivers' direction is controlled by SDDIR which is low during Direct Input/Output (DIO) writes and Direct Memory Access (DMA) reads and high during DIO reads and DMA writes. The transceiver's output enables are driven by System Data Bus Enable ($\overline{SDBEN}$). The output enables in the address latches are driven by System Bus Owned ($\overline{SOWN}$) during DMA cycles. System Extended Address Latch (SXAL) of the SIF is used to latch the extended address bits. System Address Latch Enable (SALE) is used to latch the low address bits. In this example, the parity lines SPL and SPH are not used, and are pulled up by external resistors.

Another transceiver is used to control the bus signals between the TMS38030 and the host system. $\overline{SOWN}$ controls this transceiver's direction. When $\overline{SOWN}$ is active-low, the control lines are driven from the TMS38030. When $\overline{SOWN}$ is inactive-high, the control lines are driven from the system bus.

Addresses A3 through A23, as well as $\overline{AS}$ and R/$\overline{W}$, are decoded to drive $\overline{SCS}$ low during DIO cycles. Since the address mapping of the Adapter registers is system dependent, decoding is indicated by a block termed "decode". The least significant address lines, A1 and A2, are tied to SRS0 and SRS1, respectively, to select the TMS38030 registers.

In Figure 2-6, the interrupt request is set to the highest priority level (level 7) through a line driver (74ALS241). The system's Function Codes (FC0-2) are monitored to drive System Interrupt Acknowledge ($\overline{SIACK}$) when appropriate.

Note that the system must provide a pullup resistor on the $\overline{UDS}$ (upper data strobe), $\overline{LDS}$ (lower data strobe), R/$\overline{W}$ (read/write enable), $\overline{AS}$ (address strobe), $\overline{BGACK}$ (bus acknowledge), and $\overline{DTACK}$ (data transfer acknowledge) signals.

2.6 PC AT LAN Adapter Card: Performance Analysis

This section discusses parameter selections which determine the performance attained by a TMS380-based LAN adapter card for the IBM PC AT.

2.6.1 Test Environment

The results presented below are based on measurements of throughput rates (information field bits/second) when one TMS380 adapter is continuously transmitting on the token-ring under the following conditions.

1. The host system is an IBM PC AT with a 6 MHz system clock.
2. One TRANSMIT COMMAND is issued by the host.
3. Seven TRANSMIT PARAMETER LISTS are circularly chained.
4. Each TRANSMIT PARAMETER LIST contains one DATA COUNT FIELD which is used to transmit one frame.
5. Host software polls the VALID bit in the TRANSMIT COMMAND/STATUS field of the current TRANSMIT PARAMETER LIST to detect completion of frame transmission.
6. Upon detection of frame completion, host software sets the VALID bit (i.e., prepares the frame for retransmission, issues a TRANMIT VALID interrupt request, and begins polling the VALID bit of the next TRANSMIT PARAMETER LIST in the chain.

2.6.2 Performance Results

Although several parameters affect performance to some extent, the most significant factors are:

1. Internal Adapter Buffer Size
2. Number of Allocated Internal Adapter Buffers
3. Host/Adapter DMA Interface
4. Host Transmit List Management Technique

2.6.2.2 Number of Allocated Internal Adapter Buffers

Adapter performance is enhanced when the data for frame i + 1 is transfered from the host to the adapter while frame i is being transmitted onto the token ring. For this pipelining to occur, enough internal adapter buffers must be allocated to hold two frames. Figure 2-8 graphically depicts the implications of internal buffer count by plotting transmit throughput as a function of frame size when 28, 8, and 4 internal buffers of 512 bytes each are allocated. Note the degradation that takes place when the frame size becomes large enough that four 512 byte buffers cannot hold two frames (the second dip in the curve occurs when all four buffers are required to hold one frame).

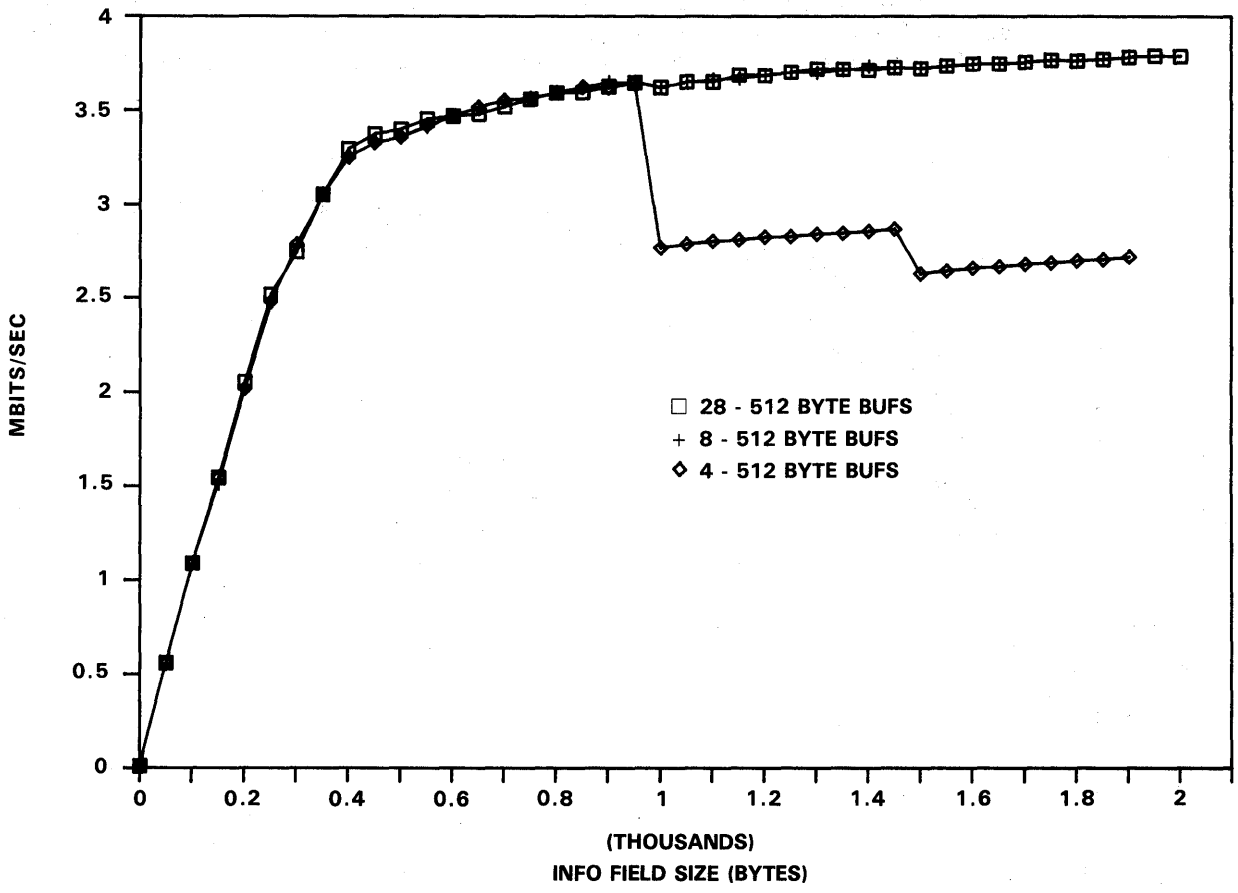


FIGURE 2-8. TRANSMIT THROUGHPUT — PC AT ADAPTER: INTERNAL BUFFER COUNT COMPARISON

Figure 2-10 plots transmit throughput as a function of frame size for the following DMA modes: Burst Size of 512 bytes; Burst Size of 512 bytes with an external hardware counter limiting the effective burst size to 18 bytes; Burst Size of 18 bytes; and Cycle-Steal. Note that when small burst sizes are required, performance is substantially improved by using an external hardware counter to limit the effective burst size.

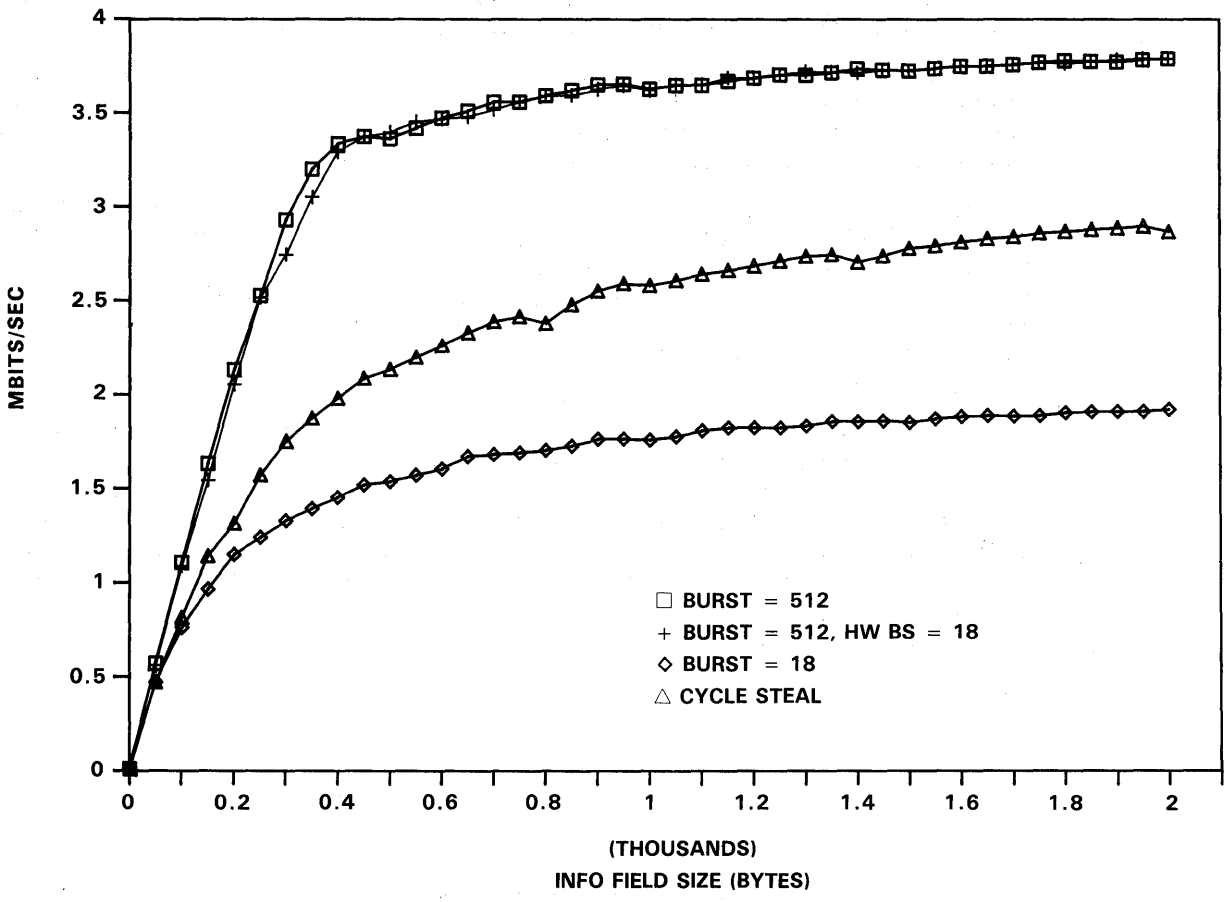


FIGURE 2-10. TRANSMIT THROUGHPUT — PC AT ADAPTER: DMA MODE COMPARISON — 512 BYTE BUFFERS

The TMS380 LAN Adapter, in addition to providing Physical layer and Medium Access Control layer services compatible with the IEEE Std 802.5 specification, provides a number of services which support the existence of a management product in the network. These services are referred to as the network management "agent" within the Adapter. Since these services are embedded within the Adapter's functionality, networks can be expanded while preserving earlier investments in attaching product hardware and software.

The TMS380 Adapter supports a network management product in two ways:

1. First, the Adapter in the attaching station which implements the network management function provides connectivity to the LAN. It recognizes information destined for, and passes the data to, the network management product.
2. Secondly, Adapters within attaching stations contain a logical agent for network management. Errors are automatically logged and reported; configuration changes are reported to the network manager; and the Adapter will respond to various requests from network management. All of this is performed transparent to the attached station. Thus, the burden of participating in network management is removed from the attaching product. Standardizing these network management services in silicon greatly reduces compatibility problems between different OEMs, and allows end users to expand their networks and add network management without changing their installed base of equipment.

A network management product can be divided into three logical entities: a Ring Error Monitor, a Network Manager, and a Ring Parameter Server.

Communications between these logical entities and the Adapter is via a special class of frames called Medium Access Control (MAC) frames. Since these functions need a "well known" address, a special type of address called a functional address is used to transmit the MAC frames to these functions. Table 3-1 illustrates the functional addresses assigned to the network management logical entities.

TABLE 3-1. NETWORK MANAGEMENT FUNCTIONAL ADDRESSES

ADDRESS	FUNCTION
>01	Active Monitor
>02	Ring Parameter Server
>08	Ring Error Monitor
>10	Network Manager
>100	Bridge

The MAC frames that are transmitted to and received from network management functions, as well as exchanged between Adapters themselves, contain an embedded "class" designator as part of the basic syntax of the MAC frame. Each MAC frame contains one source class designator and one destination class designator. Each designator is four bits in length providing for up to sixteen class designations. The class designators, as defined by the network management agent within the TMS380 Adapter, are shown in Table 3-2.

TABLE 3-3. SOURCE AND DESTINATION CLASS APPLICATIONS

SOURCE CLASS	DESTINATION CLASS	APPLICATION
>0	>0	Exchange of frames between Adapters for basic ring protocols. — Ring Poll — Ring Purge — Monitor Contention
>4	>0	Frames sent by the Network Manager to request specific action or request certain parameters from the Adapter.
>0	>4	Frames sent to the Network Manager in response to request frames being received or to report configuation changes in the ring (new station or new Active Monitor).
>0	>6	Error reporting MAC frames sent to a Ring Error Monitor.
>0	>5	A special MAC frame which requests initialization parameters from a Ring Parameter Server function.
>5	>0	MAC frames sent from the Ring Parameter Server to the Adapter, solicited or unsolicited by the Adapter.

3.2.1 Ring Error Monitor

A Ring Error Monitor (REM) serves as a collection point of error reports for network management. The network management agent in the Adapter supports a REM function with the following:

1. Adapters within the attached stations will count soft errors by the type of soft error which occurred (e.g. CRC errors, frame copied errors, etc.), and automatically report these errors to the REM (via its functional address). The Adapter does not care whether or not a REM is present on the network.
2. The Adapter that is the Active Monitor reports failure of the Ring Poll process to the REM.
3. Errors in the Active Monitor which are detected by the Active Monitor or a Standby Monitor are reported to the REM.

By using the information provided to the Ring Error Monitor, conditions which degrade the performance of the network may be efficiently detected, diagnosed, and corrected.

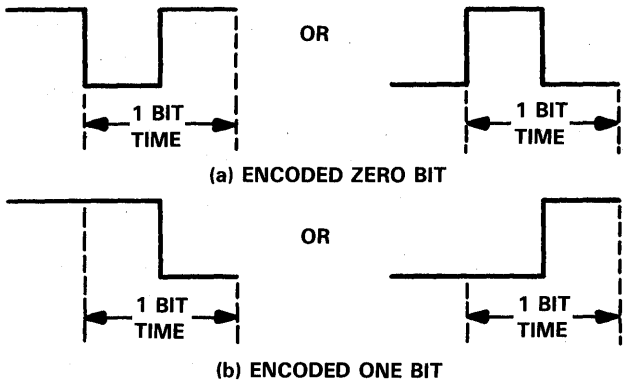


FIGURE 3-1. DIFFERENTIAL MANCHESTER CODE

Another advantage of Differential Manchester Code is that a violation of the coding rules may be easily detected for error detection purposes as well as for providing a convenient method of synchronizing bit streams. The Token Ring Adapter is designed to detect such violations. Figure 3-2 illustrates four possible violation patterns. These are designated V0 for the zero bit violation and V1 for the one bit violation. These patterns are used within starting delimiters and ending delimiters for frame and token boundary synchronization. They will be referenced later in this manual.

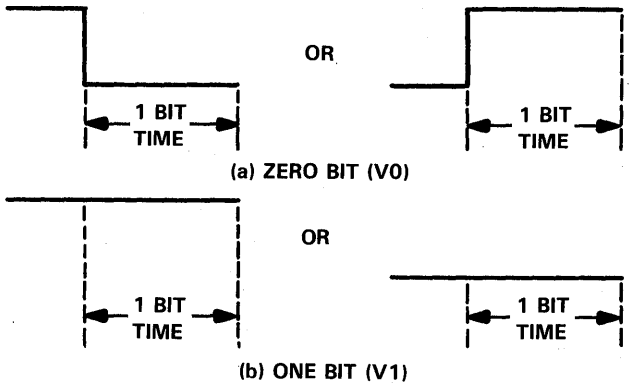


FIGURE 3-2. CODE VIOLATIONS

3.3.2 Ring Clocking

An Adapter, randomly designated via a contention process, provides master clocking to the ring by deriving its timebase from a crystal oscillator. This Adapter, as will be shown later, is called the Active Monitor. Any Adapter on the ring may assume the role of Active Monitor.

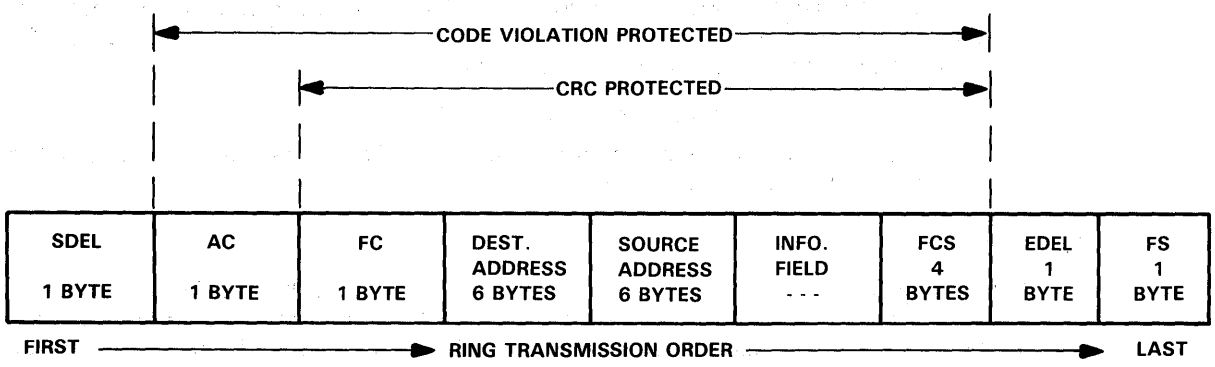
The remaining ring stations on the ring derive their timebase by phase synchronizing a voltage controlled oscillator to the incoming bit stream. This Phase Locked Loop (PLL) derived clock provides the necessary timebase from which the bit stream is received and transmitted by the Adapter.

3.4.2 Frame Format

The physical frame format is strictly defined by the Token Ring Architecture and consists of the following fields within the frame's bit stream:

1. Starting Delimiter Field (SDEL)
2. Physical Control Fields (PCF) consisting of the Access Control (AC) and Frame Control (FC) fields
3. Source and Destination Address Fields (SA/DA)
4. Information Field (data)
5. Frame Check Sequence Field (FCS)
6. Ending Delimiter (EDEL)
7. Frame Status Field (FS)

This frame format is shown in Figure 3-3. Note that this format is for frames in which the TOKEN INDICATOR bit is set to one. If a TOKEN INDICATOR bit is set to zero, indicating a token, the token format illustrated is circulated on the ring. In this manual, the terminology "frame" refers to a data stream as illustrated in Figure 3-3, with the TOKEN INDICATOR bit set to one.



TOKEN FORMAT:

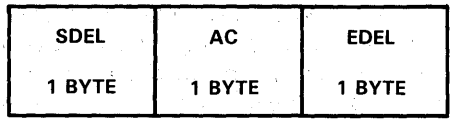


FIGURE 3-3. ADAPTER FRAME FORMAT

3.4.4.2 Frame Control Field - FC

The bit assignments and bit definitions of the Frame Control (FC) field byte are provided in Figure 3-6 below:

BIT 0	1	2	3	4	5	6	7
FRAME TYPE 0	FRAME TYPE 1	"0"	"0"	PCF ATTEN. 0	PCF ATTEN. 1	PCF ATTEN. 2	PCF ATTEN. 3

FIGURE 3-6. FC FIELD

BITS 0,1 FRAME TYPE BITS. These two bits indicate the frame type. Currently, the following frame types are defined:

00 MAC Control Frame

01 Non-MAC Control Frame

10 Reserved

11 Reserved

BITS 2,3 RESERVED. Bits 2 and 3 are always set to zero.

BITS 4-7 PCF ATTENTION CODE. These bits indicate those frames which are copied into a special internal buffer called the 'express buffer' upon reception. The values of the PCF Attention Code recognized by the Adapter are listed below. The PCF Attention code is examined for MAC frames only.

0001-Express Buffer

0010-Beacon

0011-Claim Token

0100-Ring Purge

0101-Active Monitor Present

0110-Standby Monitor Present

3.4.5 Source and Destination Address Fields

The addressing for ring frames is contained within the source and destination fields of the frame. The source and destination address fields are each six bytes in length. These conform to the general address format described in Section 3.5.

3.4.6 Information Field

The information field is a multi-byte field in which the data to be transported between ring stations is carried. The information field must be at least one byte in length. The maximum length of this field is on the order of 4027 bytes.

3.4.7 Frame Check Sequence

Following the information field, a 32-bit cyclic redundancy code (CRC) is appended to the frame to protect the frame control field, source and destination addresses, and the information field. The CRC field is generated from a polynomial and is accumulated serially as a frame is transmitted or received. When a frame is being repeated or copied by an Adapter, the received CRC field is compared to the calculated value to verify that the frame was copied without error. On transmit, the CRC field is appended to the transmitted

3.5 Ring Addressing

This section describes the format of media access level source and destination address fields and source routing concepts using routing information fields.

The addressing for ring frames is contained within the source and destination fields of the frame. The destination and source address fields are each six bytes in length and conform to the general address format shown in Figures 3-9 and 3-10 respectively.

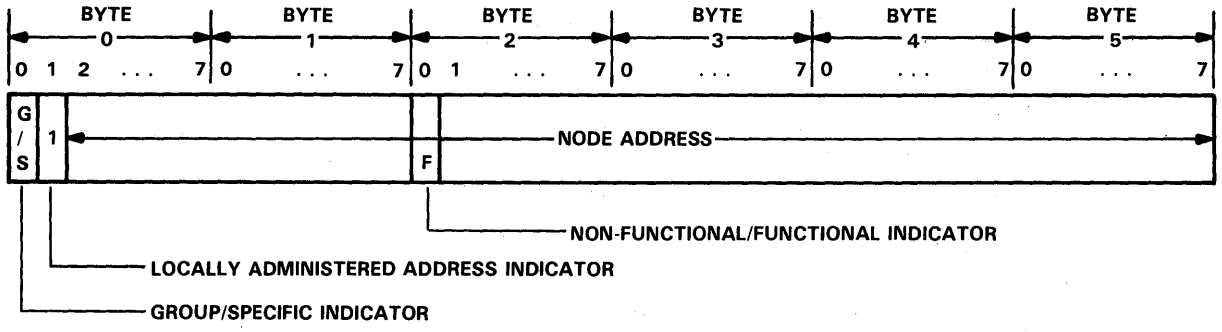


FIGURE 3-9. DESTINATION ADDRESS FORMAT

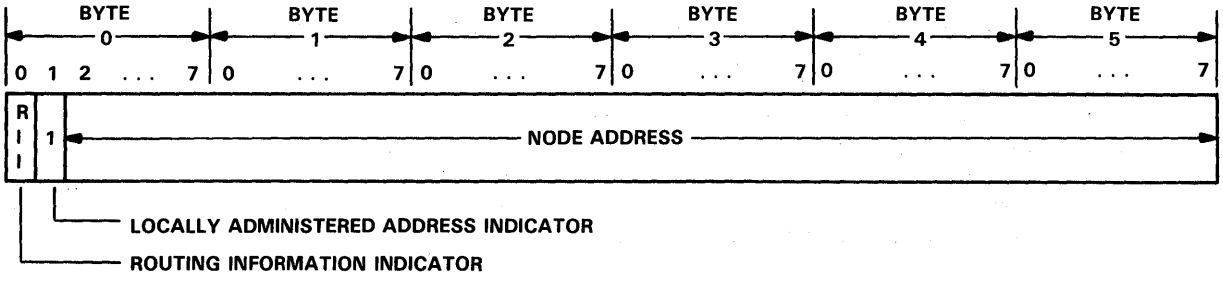


FIGURE 3-10. SOURCE ADDRESS FORMAT

The source and destination address differ in use of indicator bits within the frame format. The Group/Specific and Functional/Non-functional indicators are used for destination addresses only. All source addresses will be ring station specific addresses. Since all source addresses of transmitted frames will be the ring station specific address of the transmitting node, the most significant bit position of the source address is used to indicate the presence of a routing information field. The routing information field is a field of up to 18 bytes which follows the source address and precedes the information field of a frame.

3.5.1 Address Types

All addresses in the network are either locally administered addresses (byte 0, bit 1 set to one) or universally administered addresses (byte 0, bit 1 set to zero). Whether an address is locally or universally administered depends on whether address assignment is

c. Group - A group address is indicated by setting bit 0 of byte 2 to one. This type of Group Address is assigned at the discretion of the attached system. The address may be passed as one of the OPEN parameters.

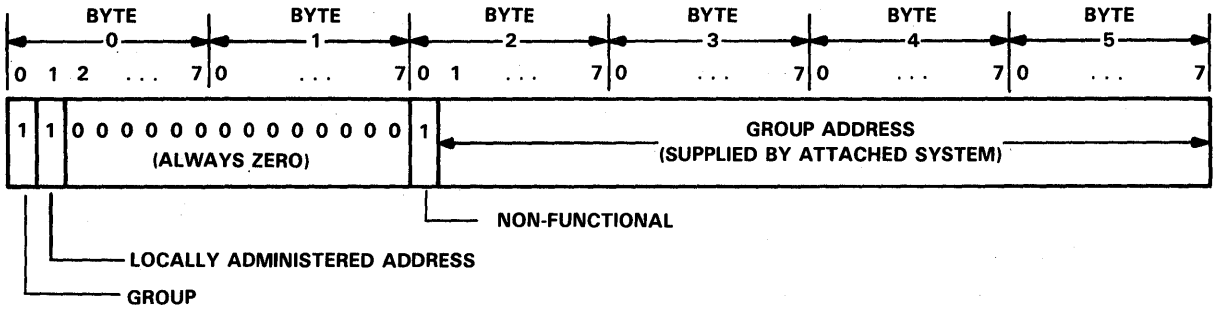


FIGURE 3-13. GROUP ADDRESS

2. Ring Station Specific Address - The primary address recognized by the Adapter. It is the address associated with the Physical Transmission Layer function. This address may be passed to the Adapter by the attached system during the OPEN command, or the Ring Station Address may be read from an attached ROM containing a burned-in address. (This is described in Appendix B.) If the attached system passes an all zeros ring station specific (or node) address during the OPEN command, the Adapter will use the burned-in address (BIA) supplied. This burned-in address allows address assignments to be integrated on the Adapter's card in a non-volatile (ROM) manner.

A ring station address assigned by the attached system or contained in BIA ROM must conform to the following format. Note that bits 0,1 of byte 0 must be set to 0,1 respectively. Violating these rules causes the Adapter to reject the address assignment with a node address error.

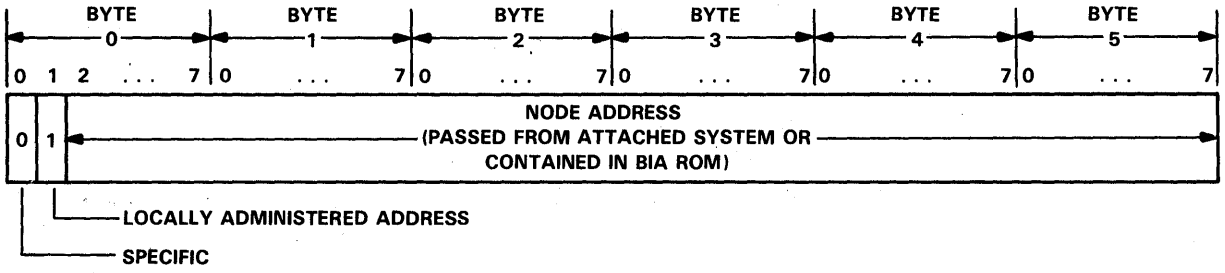


FIGURE 3-14. RING STATION ADDRESS FORMAT

3.6 Medium Access Control

3.6.1 Concept

The Token Ring Local Area Network calls for a comprehensive set of problem determination, resolution, and reporting functions, so that ring communication problems are rapidly diagnosed and automaticaliy corrected. As was introducted in Section 2, the MAC layer services provided by the Adapter allow compatible connectivity to the token ring LAN.

Operation of the MAC protocol is completely transparent to the host system attached to the Adapter. A special class of frames, known as MAC frames, are sent between Adapters to insure proper ring operation, to recover the ring from violations of normal protocols, and to report information to network management. These frames are originated by the Adapter software in response to internal timeouts, error conditions on the ring, or MAC frames received from a network manager or another ring station. MAC frames are transmitted without indication to the attached system. Furthermore, MAC frames that are received are acted upon by the Adapter itself, rather than being reported to the attached system, unless the passing of MAC frames from the Adapter to the attached system is explicitly requested by the attached system. Normally, an attached system will never need to send or receive a MAC frame. Processing of the MAC layer protocol entirely within the Adapter results in a lower workload on the attaching system and an increase in system performance.

The Adapter's MAC protocol is implemented with a number of independent software processes. These processes can be considered to be running concurrently. Each process will be described in detail in Section 3.8.

3.6.4 MAC Frame Source Address

The source address field always contains the ring station specific address of the originator of the frame.

3.6.5 MAC Frame Major Vectors

The Information Field in MAC frames handled by the Adapter consists of one Major Vector (MV). The Major Vector may contain one or more subvectors. When the Adapter constructs a MAC frame for transmission, the subvectors are placed in the frame, in order shown in the tables in Appendix B.1.

The Major Vector is made up of the following fields within the MAC frame information field:

MV LENGTH — The length in bytes of the entire Major Vector, including the length field.

MV CLASS — Defines the origin and destination class of the MV. The high-order four bits are the destination class and the low-order four bits are the source class.

The source class types are as follows:

>0 - Ring Station

>1 - LLC Manager

>4 - Network Manager

>5 - Ring Parameter Server

>6 - Ring Error Monitor

The destination class will always be Ring Station, >0, for MAC frames which are processed directly by the Adapter. Other destination classes will be passed on to the attached system if copied.

MV COMMAND — The Major Vector Command defines the function that the receiver is to perform. A list of Major Vector commands is shown in Table 3-4.

SUBVECTORS — Each Major Vector contains one or more subvectors. A subvector contains the following fields:

- SV LENGTH — The length of the subvector in bytes including the length field.
- SV TYPE — The type byte identifies the information found in the subvector value. The SV types recognized by the Adapter are shown in Table 3-5.
- SV VALUE — The information used to process the subvector.

3.6.6 MAC Frames Processed by the Adapter

Many MAC frames are processed automatically by the Adapter. Other MAC frames are passed to the attached system for processing by higher-level protocols. MAC frames processed automatically by the Adapter are those received with a destination class of Ring Station. If a response to a ring station class MAC frame is required, the MAC frame response is transmitted with a source class of Ring Station.

Some frames processed by the Adapter are also passed to the attached system. Three options specified during the open process allow MAC frames to be passed to the attached system after the Adapter has been inserted onto the ring:

- Pass Attention MAC frames. MAC frames that have an attention code (bits 4-7 of FC) greater than one are processed normally by the Adapter and then given to the attached system when one of the following conditions occur:
  - When the attention code is different from the last attention code greater than one.
  - When the source address in the MAC frame is different from the last source address received.
  - If it is a Beacon MAC frame, when the Beacon type subvector value is different from the Beacon type subvector value in the last Beacon MAC frame.
- Pass Adapter MAC frames. MAC frames are passed which have a Major Vector type not recognized by the Adapter. These will be passed to the attached system if this option is enabled. Otherwise, the Adapter responds by transmitting a negative response MAC frame.
- Pass Beacon MAC frames. If a Beacon MAC frame is received by the Adapter, it is passed to the attached system if the source address or Beacon Type Subvector is different from the last Beacon MAC frame received.

Table 3-6 describes briefly the MAC frames processed directly by the Adapter. These MAC frames will be introduced in more detail during the discussion in Section 3.8.

TABLE 3-6. MAC FRAMES PROCESSED BY THE ADAPTER (continued)

MAC FRAME	DESCRIPTION
REPORT RING POLL FAILURE	This frame is sent by the Active Monitor to the Ring Error Monitor to report a failure in the Ring Poll Process. This frame contains the address of the last station that responded in the Ring Poll Process before the Active Monitor detected the failure.
REPORT ERROR	This frame is used to report soft error events to the Ring Error Monitor.
REPORT STATION ADDRESS	This frame is sent by the Adapter in response to the Request Station Address MAC frame. The Request Station Address MAC frame is sent by the Network Manager.
REQUEST STATION STATE	This frame is sent by the Network Manager to request the Adapter to respond with a Report Station State MAC frame.
REQUEST INITIALIZATION	This frame is transmitted in Phase 4 of the Insertion Process to request operational parameters from the Ring Parameter Server.
REQUEST STATION ATTACHMENT	This frame is sent by the Network Manager to request the Adapter to respond with a Report Station Attachment MAC frame.
REQUEST STATION ADDRESS	This frame is sent by the Network Manager to request the Adapter to respond with a Report Station Address MAC frame.
REPORT TRANSMIT FORWARD	This frame is sent by the Adapter to the Network Manager functional address when a frame is forwarded and stripped by the Transmit Forward Process.
RESPONSE	This frame is used to send positive responses to frames that require acknowledgement, or to report errors in syntax in a MAC frame sent to the Adapter.
ACTIVE MONITOR PRESENT	This frame is transmitted by the Active Monitor when in the Ring Poll Process to request a Standby Monitor Present MAC frame from the nearest downstream neighbor from the Active Monitor.
STANDBY MONITOR PRESENT	This frame is used in the Ring Poll Process to respond to an Active Monitor Present or Standby Monitor Present MAC frame.
RING PURGE	This frame is used by the Active Monitor in the Ring Purge Process.

Only the first occurrence of an optional subvector is processed by the Adapter software. Any optional subvector that has already been found in the frame is ignored. The following describes the MAC frame syntax checking procedure:

1. The Routing Information field is checked to determine if the length is longer than 18 bytes or odd. If the length is greater than 18 or odd, the frame is ignored.
2. The length of the frame is checked to determine if it can contain a Major Vector Length and ID. If the length of the frame is too short (less than 4 bytes), a negative response of MAC Frame Data Field Incomplete is sent. Note that the source class, destination class, and the Major Vector command will be invalid in the response since the received frame was too short to contain them.
3. If the destination class is not zero, the frame is passed to the attached system, with no further syntax checking.
4. The command byte is checked to see if it is a Transmit Forward. If it is, no further syntax checking is done by this syntax checking routine.
5. The Major Vector Length is checked to determine if it is in the range of the received frame. If the length in the Major Vector ID does not agree with the length of the frame, a negative response of Major Vector Length Invalid is sent.
6. The Command byte in the Major Vector ID is checked to determine if it is greater than >10, the highest Major Vector ID handled by the Adapter. If the Adapter has been opened without the open option to pass Adapter MAC frames, a negative response is sent with a code of Major Vector Command Not Supported. If the open option is selected, the frame is passed to the attached system without further syntax checking.
7. If the Source Class in the class byte in the Major Vector ID is not valid for the command in the Major Vector ID, a negative response of Inappropriate Source Class is sent.
8. The subvectors are checked as follows:

   - If a subvector length is zero, than a negative response of Subvector Length Error is transmitted to the sender.
   - All required subvectors must be present. A response of Required Subvector Missing is transmitted if this is not the case.
   - If a subvector in the frame is marked as 'required' and is not a required subvector or is duplicated, a response of Unknown Required Subvector is sent.
   - Optional subvectors are ignored.

Assured Delivery Process

The Assured Delivery Process is intended to fulfill the following requirements:

1. To significantly improve the probability of, but not guarantee, the delivery of selected MAC frames.
2. To provide a mechanism that has a high probability of preventing duplicate copies of frames delivered to the frame's destination address.

The MAC frames which use this process are the Report Error MAC frame and the Report SUA Change frame.

This procedure uses the Address Recognized Indicator bit (ARI) and the Frame Copied Indicator (FCI) bits of the Frame Status (FS) field of the frame. An internal status bit (LFED) is also used which indicates a frame error occurred during the stripping of a transmit frame from the ring. The frame errors which may occur to set this bit include code violations and Frame Check Sequence (FCS) errors.

The Assured Delivery Process is defined by the following steps:

1. When a MAC frame is queued for transmission, a counter called the "Transmit Retry Counter" is initialized to four.
2. After a frame is transmitted and stripped, internal status is checked to determine if a corrupted free token was detected. If this did occur, proceed to step 4. If any other transmit error is detected then the process is terminated. If the internal status indicates normal transmitter completion of the transmit operation, continue with step 3.
3. If a MAC frame must be transmitted under the assured delivery process, then the ARI, FCI and LFED bits are checked. The table below shows the three conditions which must result in order to continue to step 4. With any other combinations, the frame is not re-transmitted and the process terminates.

	LFED	ARI1	FCI1	ARI2	FCI2
1)	0	1	0	1	0
2)	1	0	0	0	0
3)	1	1	0	1	0

4. The "Transmit Retry Counter" is decremented and if the counter is not zero, the frame is retransmitted and the process continues at step 2. If the counter is zero, the frame is not transmitted and the process terminates.

3.6.8 Response MAC Frames

A Response MAC frame is used to acknowledge receipt of one of the following MAC frames:

1. Change Parameters
2. Initialize Ring Station

This frame is also used in negative responses to syntax errors detected in any Adapter Destination Class MAC frame. The Adapter will not generate negative responses to MAC frames that have a source class of >0.

A Response Code subvector within the Response MAC frame carries additional response information. This Response Code subvector is of the following format.

3.7 Monitor Functions

An Adapter on the ring can be either an Active Monitor or a Stand-by Monitor. Only one Active Monitor is present on any ring; the remaining Adapters serve as Stand-by Monitors. The Active Monitor ensures normal token operation on the ring and provides the crystal-controlled master data clocking for data transmission. The Stand-by Monitors ensure that the Active Monitor is functioning properly and is still inserted on the Ring.

The Ring Purge Process is used by the Active Monitor to perform the recovery from a temporary error condition, to release a new token, and to return the ring to a known state.

The Ring Poll Process is initiated periodically by the Active Monitor to update the Upstream Neighbor's Address (UNA) in all adapters in the ring and to provide an indication to other stations in the ring that the Active Monitor is still active.

3.7.1 Active Monitor Functions

The role of the Active Monitor is to ensure normal token operation on the ring. An Adapter becomes the Active Monitor by active participation in the Monitor Contention Process. The Monitor contention process is discussed in Section 3.8.2. The Adapter that "wins" contention becomes the Active Monitor.

Upon successfully winning contention, the Active Monitor does the following:

1. Sets a bit in the TMS38020 Protocol Handler that:
   a. Provides master clocking for data transmission.
   b. Inserts a 30 bit time latency to guarantee a ring length which assures that a token can be circulated properly.
   c. Activates the circulating token removal hardware.
2. Executes the Ring Purge Process.
3. Starts the Ring Poll Process by activating an internal pacing times and queues an Active Monitor Present (AMP) MAC frame for transmission.
4. Transmits a free token of priority equal to the token reservation priority in the Ring Purge MAC frame last stripped by the Adapter.
5. Sets the Monitor Functional Address.
6. Activates a checking function that confirms that a good token is detected on the ring every 10 ms. This timer sets the maximum frame size on the order of 4048 bytes.
7. Queues a Report New Monitor MAC frame for transmission to the Network Manager.

The circulating token removal function operates as follows:

1. When tokens are released on the ring, bit 4 of the AC byte (the 'MC' bit) is transmitted as zero.
2. When an Adapter changes the token into a frame, it leaves the MC bit as zero. It indicates a frame by setting only bit 3 of AC (the 'TI' bit) to one.
3. When a frame or a token of priority greater than zero passes through the Active Monitor (which is in repeat mode), the monitor sets the MC bit.

3.7.2 Stand-by Monitor Functions

Any Adapter that is not the Active Monitor but has completed the Insertion Process will follow the procedures of the Stand-by Monitor. The function of the Stand-by Monitor is to monitor the events on the ring to determine if the Active Monitor is functioning properly.

The Stand-by Monitor Functions are disabled while the Adapter is in the Insertion, Beacon, or Monitor Contention Processes.

A station activates its Stand-by Monitor functions as follows:

- When the Adapter completes the Ring Insertion Process and did not "win contention" in Phase 1 of the Ring Insertion Process.
- When the Adapter receives a Ring Purge MAC frame while it is in Contention Repeat mode.
- When an inserted Active Monitor determines that another Adapter has assumed the functions of Active Monitor.

As a Stand-by Monitor, the station transmits on the ring using the clock derived from the incoming signal. It also deactivates the hardware mechanism for correcting circulating priority tokens and frames.

The following ring conditions are monitored by the Stand-by Monitor:

- GOOD TOKEN - The station verifies that a 'good' token is received at least once every 2.6 seconds. A 'good' token is defined as a token of priority zero, or a token of priority greater than zero followed by a frame with a priority field greater than zero.
- PERIODIC RING POLLS - The Adapter Receive Poll Timer detects the absence of Active Monitor Present (AMP) MAC frames. The Receive Poll timer is restarted when an AMP MAC frame is received. The absence of AMP MAC frames indicates there is no Active Monitor in the ring. If the Receive Poll Timer expires after 15 seconds, the Adapter enters the Monitor Contention Process in the Contention Transmit Mode.
- PROPER RING DATA FREQUENCY - The Adapter uses the 'Hardware Error Process' to check the frequency of the data on the ring. If a frequency error is detected by this process, it indicates that there is no Active Monitor or that the Active Monitor is not functioning properly. If a frequency error is detected, the Adapter enters the Monitor Contention Process in Contention Transmit mode.

3.7.2.1 Stand-by Monitor Exception Conditions

The following exception conditions cause the Adapter to de-activate the Stand-by Monitor functions and take these actions.

ACTIVE MONITOR ERRORS	If the Adapter detects an error in the Active Monitor, the Adapter enters the Monitor Contention Process in Contention Transmit Mode.
RECEIVE BEACON	The receiving station enters the Beacon Process in Beacon Repeat Mode.
CLAIM TOKEN FRAME	If the Adapter receives a Claim Token MAC Frame, the Adapter enters the Monitor Contention Process.
SIGNAL LOSS	If a signal loss is detected by the Adapter, it enters the Monitor Contention Process in Contention Transmit Mode.
WIRE FAULT	If a wire fault condition is detected by the Adapter, the Adapter de-inserts from the ring and sets the Lobe Wire Fault bit in Ring Status.

3.8.1 Notes on Reading the MAC Frame Tables

When each process is discussed, the MAC frames which are exchanged by the execution of that process are also provided in tabular format. These tables contain the following columns:

M-V NAME — This is the name of the MAC frame. Also provided is the hexadecimal value of the Major Vector (M-V) command. Hexadecimal numbers are preceded by a ">" sign.

DEST CLASS — The destination class is the four bit destination class field of the MAC frame Major Vector ID as previously introduced.

SOURCE CLASS — The source class is the four bit source class field of the MAC frame Major Vector ID. The source class value ranges from 0 through F. The source classes referenced in these tables are as follows:

>0 ..... RS - Ring Station (Adapter)
>4 ..... NM - Network Manager
>5 ..... RPS - Ring Parameter Server
>6 ..... REM - Ring Error Monitor

DEST ADDRESS — This is the destination address field of the MAC frame. The terminology used in this field is described below:

all sta — ALL STATIONS. This indicates a group broadcast address allowing all Adapters on the local ring to copy the frame.

F<fa> — FUNCTIONAL ADDRESS. This indicates that a destination address is the functional address of "fa" function, i.e. Network Manager, Ring Parameter Server, etc. The functional addresses are as follows:

RPS - Ring Parameter Server	>0002
REM - Ring Error Monitor	>0008
NM - Network Manager	>0010

MA — MY ADDRESS. This Adapter's specific address.

SA — SOURCE ADDRESS.

TARGET — A six byte destination address.

SUBVECTORS — The subvectors which are included in the MAC frame are listed in this column. The hexadecimal subvector type value is also provided. Two columns are used to indicate additional information:

3.8.2.1 *Applicable MAC Frames*

Table 3-9 describes the MAC frames which are used in this process.

TABLE 3-9. MONITOR CONTENTION PROCESS — APPLICABLE MAC FRAMES

M-V (FRAME) NAME	DESTINATION CLASS	SOURCE CLASS	DESTINATION ADDRESS	SUBVECTORS		
				R/O		
				XMT	RCV	NAME
>03 Claim Token	>0	>0	all stations	A A	O R	>0B Physical Drop >02 UNA
>25 Report New Monitor	>4	>0	F(NM)	A A A		>0B Physical Drop >02 UNA >22 Product ID
>28 Report Monitor Error	>6	>0	F(REM)	A A A		>30 Error Code: >0001 Monitor Err >0002 Dup. Mon. >0003 Dup. Addr. >0B Physical Drop >02 UNA

NOTE: A = always transmitted, R = required, O = optional

3

3.8.2.2 *Contention Transmit Mode*

The following list describes the conditions that cause a station to enter Contention Transmit mode and begin the Monitor Contention Process.

3.8.2.4 Adapters not in Monitor Contention

An Adapter not in Contention Transmit Mode and not in Contention Repeat Mode takes the following action when it receives a Claim Token MAC frame.

- If the source address in the frame is less than this Adapter's specific address, the Adapter is inserted, and the Adapter was OPENed with the Contender option then the Adapter enters Contention Transmit Mode. Otherwise, it enters Contention Repeat Mode.
- If the source address in the frame is equal to this Adapter's specific address, the frame is ignored.

3.8.2.5 Exception Events

The following events cause an Adapter to queue an error reporting MAC frame and enter Contention Repeat Mode:

1. An Active Monitor ring station that receives a Claim Token MAC Frame (a) de-activates its Active Monitor functions, (b) enters Contention Repeat mode, and (c) queues the Report Monitor Error MAC frame with an Error Code subvector value equal to >0001. This indicates that a Stand-by Monitor detected an error in the Active Monitor. This frame is transmitted after contention is resolved.
2. A ring station in Contention Transmit Mode that receives a Claim Token MAC frame with a source address equal to its specific address and a UNA address NOT equal to its UNA (a) enters Contention Repeat Mode and, when contention is resolved, (b) queues the Report Monitor Error MAC frame with an Error Code subvector value equal to >0003, indicating a duplicate address was detected in Monitor Contention.

The following exceptions cause an Adapter in Contention Transmit or Repeat Mode to enter the Beacon Transmit mode in the Beacon Process or abnormally terminate an OPEN command from the attached system.

1. If the Monitor Contention Timer expires (one second) and the Adapter has not completed phase 2 of the Insertion Process, the OPEN command is terminated with an error to the attached system. The Adapter is de-inserted from the ring.
2. If the Monitor Contention timer expires and the Adapter is in phase 3 or 4 of the Insertion Process or is inserted, the Adapter enters Beacon Transmit Mode.

If an Adapter is inserted and is in Contention Repeat or Transmit Mode, and receives a Beacon MAC frame, it enters the Beacon Process in Beacon Repeat Mode.

If an Active Monitor receives a Ring Purge MAC frame, it checks the source address of the frame to determine if it transmitted the frame. The reception of this frame by an Active Monitor which did not transmit the frame is an exception condition of the Active Monitor.

3.8.3.4 Exception Conditions

If the ring purge timer expires (one second), the Adapter enters the Monitor Contention Process in Contention Transmit Mode.

If the Adapter is in the Insertion Process when the ring purge timer expires, the Adapter is de-inserted and the OPEN command is terminated with an error message to the attached system.

3.8.4 Ring Poll Process

The Ring Poll Process enables each Adapter on the ring to acquire the six-byte specific address of its Upstream Neighbor Station. In this process each station transmits its specific address (6 bytes) and its physical drop number (4 bytes) to the next downstream station. Each station saves its UNA and if different from the previously saved UNA, queues for transmission a Report SUA Change MAC frame to the Network Manager.

This process allows an ordered list of stations on the network to be maintained by the Network Manager for network diagnostic purposes.

3.8.4.1 Applicable MAC Frames

Table 3-12 presents the MAC frames used by this process.

TABLE 3-12. RING POLL PROCESS — APPLICABLE MAC FRAMES

M-V (FRAME) NAME	DESTINATION CLASS	SOURCE CLASS	DESTINATION ADDRESS	SUBVECTORS		
				R/O		
				XMT	RCV	NAME
>05 Active Monitor Present (AMP)	>0	>0	all stations	A A	O R	>0B Physical Drop >02 UNA
>06 Standby Monitor Present (SMP)	>0	>0	all stations	A A	O R	>0B Physical Drop >02 UNA
>27 Report Ring Poll Failure	>6	>0	F(REM)	A		>0A SA of last AMP or SMP frame
>26 Report SUA Change	>4	>0	F(NM)	A A		>0B Physical Drop >02 UNA

NOTE: A = Always transmitted, R = Required, O = Optional

3.8.4.2 Ring Poll Procedure

The Active Monitor will transmit an Active Monitor Present (AMP) MAC frame whenever its poll timer expires (every 7 seconds) or at the end of the Ring Purge Process. The Active Monitor also resets an internal flag termed the 'poll complete flag'.

If the Active Monitor receives an AMP MAC frame from another Adapter, then two Adapters think they are the Active Monitor. The Active Monitor therefore resets its Active Monitor functions and queues for transmission a Report Monitor Error MAC frame to the REM with a subvector value indicating that a duplicate monitor was detected. The Adapter now responds to the received AMP MAC frame as a non-monitor station.

In order to detect streaming in the Adapter immediately upstream from the Active Monitor, the Active Monitor checks that it receives its own AMP MAC frame within 15 seconds of the last one. If it does not receive it, the Active Monitor will enter Monitor Contention in the Contention Transmit mode.

3.8.4.4 Standby Monitor Exception Conditions

In order to detect the failure of the Active Monitor, each Stand-by Monitor verifies that an AMP frame is received within fifteen seconds of the last one. If not, the Standby Monitor discards any frame(s) pending transmission and enters Monitor Contention in Contention Transmit Mode.

This fifteen second period is timed using the receive poll timer. This timer is only active in a Standby Monitor.

3.8.4.5 Exception Conditions-All Chapters

Insertion Phases 1 and 2

If the Ring Poll Procedure requires the transmission of a Report SUA Change or an SMP MAC frame, the transmission of these frames is delayed until Phase 3 of the Insertion Process.

Contention Transmit Mode or Beacon Transmit Mode.

Entry into either Contention Transmit Mode or Beacon Transmit Mode will cause the Adapter to purge any AMP or SMP MAC frames pending transmission.

Poll Frame Re-try

AMP or SMP MAC frames are not checked for successful transmission. An unsuccessful transmission will cause the poll cycle to terminate, but the Active Monitor will start a new poll cycle when the Poll Timer expires (7 seconds).

3.8.5 Beacon Process

The Beacon Process is used to recover the ring when a ring station has sensed that a hard error has occurred, rendering the ring inoperable. A station detecting a ring failure upstream transmits or "beacons" information in a MAC frame that isolates the error location.

The Beacon Process is started when an Adapter inserted in the ring detects that an Adapter's Monitor Contention Timer expired in the Monitor Contention Process, indicating that contention could not be resolved.

When a station beacons, all other stations on the ring enter either Beacon Transmit or Beacon Repeat Mode. In Beacon Transmit Mode, Beacon MAC frames are transmitted at 20 millisecond intervals, without waiting for a token. Idle zero bits are transmitted between frames. An Adapter not in the Beacon Process that receives a Beacon MAC frame enters Beacon Repeat mode. An Adapter in the Insertion Process will not enter the Beacon Process but will terminate the OPEN command with an error indicating that the ring is beaconing.

If the Adapter receives a Beacon MAC frame that it did not transmit but has a Beacon Type subvector value of equal or higher priority than the Beacon Type subvector value being transmitted by this Adapter, the Adapter enters Beacon Repeat Mode and clears the Beacon Transmit Bit in the Ring Status Register.

If the Adapter receives a Claim Token MAC frame the frame is ignored.

If the Adapter does not proceed to Monitor Contention mode while in Beacon Transmit Mode within 26 seconds, the Adapter will execute the Beacon Transmit Auto Removal Test. This test is only executed once while in the Beacon Process. The Adapter must return to normal operation before the Beacon Transmit Auto Removal Test can be executed again.

3.8.5.3 Beacon Repeat Mode

When the Adapter enters Beacon Repeat Mode, it sets to one the hard error bit in the Ring Status register. The Adapter repeats the incoming signal using the recovered ring clock.

The Adapter verifies that Beacon frames continue to be received in Beacon Repeat Mode. If no Beacon MAC Frame is received for a period of 200 milliseconds, the Adapter assumes that the conditions causing the beacon have been corrected. In this case, the Adapter resets to zero the Hard Error Bit in Ring Status, exits the Beacon Process and enters the Monitor Contention Process.

When a Beacon MAC frame is received, it is inspected to determine if the frame was sent by the upstream neighbor (Source Address of the frame is equal to this Adapter's UNA) or by the nearest downstream station (UNA in the frame is equal to this Adapter's address).

When Beacon frames are received by any Adapter, the following actions are taken:

- If eight consecutive Beacon MAC frames are received from the nearest downstream station (the UNA ID subvector in the received Beacon MAC frame is equal to the Adapter's specific address) the Adapter executes the Beacon Receive Auto Removal Test. This test can only be executed once while the Adapter is in the Beacon Process. The Adapter must return to normal operation before the Beacon Receive Auto Removal Test can be executed again.
- If the Beacon frames are not from the nearest downstream station, the following two checks are made:
  - If two consecutive Beacon MAC frames are received from the nearest upstream station, the Adapter activates its functions for marking and removing circulating frames. This marking and removing process is described in Section 3.7.1. The Adapter will also prevent itself from executing the Beacon Receive Auto Removal Test. If a circulating beacon frame is detected, the Adapter enters the Monitor Contention Process in Contention Transmit Mode.
  - If the Beacon MAC frame is not from the nearest upstream station, the Adapter disables its circulating frame removal functions.

If a Monitor Contention MAC frame is received, the Adapter resets the Hard Error Bit in Ring Status in the Protocol Handler, exits the Beacon Process and enters the Monitor Contention Process.

3.8.6 Hardware Error Process

The Hardware Error Process is used to detect the following error conditions:

- Wire Fault
- Frequency Error
- Ring Signal Loss

Two procedures are used to detect these error conditions, the Wire Fault Detection Procedure and the Ring Interface Error Detection Procedure. The Wire Fault Detection Procedure is used to detect Wire Fault conditions. The Ring Interface Error Detection Procedure is used to detect the Frequency Error condition and the Signal Loss condition.

3.8.6.1 Wire Fault Detection Procedure

A wire fault condition is indicated when the DC current on either wire of the transmit pair exceeds an abnormally high or low condition. This will be caused, for instance, if one of the lines is open or if any of them are shorted to ground. When a wire fault condition is verified to exist continuousiy for 5 seconds, the Lobe Wire Fault bit of the Ring Status register is set. The Adapter then physically de-inserts from the ring.

3.8.6.2 Frequency Error Detection Procedure

When the frequency of the incoming signal differs by more than 0.6% from the local crystal oscillator, a Frequency Error Condition is indicated. This is detected by an overflow or underflow condition of the elastic buffer.

3.8.6.3 Signal Error Detection Procedure

An incoming Ring Signal Loss is indicated when:

1. The incoming signal has insufficient signal energy (see Section 4.5.10); or
2. The incoming signal is grossly out of phase with the local phase-locked loop.

When conditions one or two are verified to be in effect for 200 milliseconds, the software indicates a Signal Loss Condition. If this occurs during the Ring Insertion Process (phases 1 and 2), the OPEN Command terminates with a Signal Loss error code. If the Adapter is in the Beacon Transmit Auto Removal process, the Adapter enters Beacon Transmit Mode. Otherwise, the Adapter enters Monitor Contention Transmit mode.

3.8.7 Ring Insertion Process

The Ring Insertion process is performed after Bring-Up Diagnostics and Initialization have been completed. An OPEN command, issued by the attached system, initiates the Ring Insertion Process. Before beginning Phase 0 of the Ring Insertion Process, the following defaults are set in the Adapter:

- The Physical Drop Number is set to zero.
- The Local Ring Number is set to zero.
- The Soft Error Report Timer Value is set to two seconds.
- The Enabled Function Classes Mask is set to permit all classes of MAC frames to be transmitted across the System Interface except for Ring Station (>0) and Ring Parameter Server (>5).
- The Allowed Access Priority is set to three (highest priority).
- All error counters are reset to zero.

3.8.7.1 Applicable MAC Frames

The Insertion Process uses the MAC frames described in Table 3-14.

TABLE 3-14. INSERTION PROCESS — APPLICABLE MAC FRAMES

M-V (FRAME) NAME	DESTINATION CLASS	SOURCE CLASS	DESTINATION ADDRESS	SUBVECTORS		
				R/O		NAME
				XMT	RCV	
>07 Duplicate Address Test	>0	>0	target	A		none
>08 Lobe Media Test	>0	>0	all zero	A A	N	>26 Wrap Data
>20 Request Initialization	>5	>0	F(RPS)	A A A A		>23 Adapter Software level >02 UNA >22 Product ID >21 Reserved
>0C Change Parameters	>0	>4	target		O O O O O O	>09 Correlator >03 Local Ring No. >04 Assign Phys. Drop number >05 Soft Error Report Timer Value >06 Enabled Function Class >07 Allowed Access Priority
>0D Initialize Ring Station	>0	>5	target		O O O O	>09 Correlator >03 Local Ring No. >04 Assign Phys. Drop Number >05 Soft Error Report Time Value

NOTE: A = Always transmitted, N = Not syntax checked, O = Optional

Upon completion of one of these events, Phase 1 is complete and the Adapter enters Phase 2, Address Verification. If the OPEN command is terminated because of an error condition during this phase, the Adapter is physically de-inserted from the ring.

Phase 1 Exception Events

Timeouts. If an Active Monitor is not detected within 18 seconds from the start of this process, the Adapter enters the Monitor Contention Process in Contention Transmit Mode.

If the Adapter enters the Monitor Contention Process and contention is not resolved within one second, the OPEN command is terminated and the Adapter reports to the attached system that the ring is beaconing.

If, after the Contention Process, the Adapter becomes the Active Monitor and performs the Ring Purge Process, and the Purge Process is not completed within one second, the OPEN command is terminated and the Adapter reports a ring failure to the attached system.

Receive Frame. If the Adapter receives an AMP or SMP MAC Frame, it will follow the normal procedure for Ring Poll and will exit Phase 1 and enter Phase 2 (Address Verification) of the Insertion Process. If the transmission of a SMP or a Report SUA Change MAC frame is required, however, the Adapter will delay the transmission until Phase 3 of the Insertion Process.

If a Claim Token MAC Frame is received and the Adapter has not started the Monitor Contention Process, then the Adapter will begin Contention Repeat Mode.

If a Beacon MAC frame is received, the OPEN command is terminated and the Adapter reports to the attached system that the ring is beaconing.

If a Remove Ring Station MAC frame is received, the OPEN command is terminated and the Adapter reports to the attached system that a remove was received.

All other MAC frames are processed normally.

3.8.7.4 Address Verification: Phase 2

Upon successful completion of Phase 1, the Address Verification phase is entered. The ring station address must be unique to this Adapter. This phase of the Insertion Process ensures that this address is not being used by another Adapter that is inserted in the ring.

The Duplicate Address Test MAC Frame is used for performing the address check. Note that the uniqueness check for all rings is not a function of the Adapter.

The Adapter sends a series of Duplicate Address Test MAC frames addressed to itself. If another station matches the local Adapter's address, then it will set to one the Address Recognized Indicator (ARI) bits of the frame. It may also set to one the Frame Copied Indicator (FCI) bits of the frame if the frame was copied. The Adapter will assume no other station matches its address when it receives two of its Duplicate Address Test MAC frames with both of the ARI and FCI bits set to zero.

If two frames are received with either the ARI or FCI bits set to one, the Adapter de-inserts itself from the ring and terminates the OPEN command with a Duplicate Node Address error code. Any other error condition will also cause the Adapter to de-insert from the ring.

After the station's address has been checked, the Adapter proceeds to Phase 3 (Participation in Ring Poll) of the Insertion Process.

Phase 3 Exception Events

Hardware Exceptions. If a signal loss is detected, the OPEN command terminates, the Adapter de-inserts, and the Adapter reports a signal loss to the attached system.

If a frequency error is detected, the OPEN command terminates, the Adapter is de-inserted and it reports a frequency error to the attached system.

Timeouts. If no AMP or SMP MAC frame is received with ARI=FCI='00' within 18 seconds, the Adapter terminates the OPEN command, de-inserts from the ring, and the Adapter reports a timeout error to the attached system.

If the Adapter enters the Monitor Contention Process and contention is not resolved within one second, the OPEN command is terminated and the Adapter reports to the attached system that the ring is beaconing.

If, after the contention process, the Adapter becomes the Active Monitor and performs the Ring Purge Process, and the Purge Process is not completed within one second, the OPEN command is terminated and the Adapter reports a ring failure to the attached system.

Receive Frame. If a Claim Token MAC Frame is received and the Adapter has not started the Monitor Contention Process, then the Adapter will go to Monitor Contention Repeat Mode.

If a Beacon MAC frame is received, the OPEN command terminates, the Adapter de-inserts, and the Adapter reports to the attached system that the ring is beaconing.

If a Remove Adapter MAC frame is received, the OPEN command terminates, the Adapter de-inserts, and the Adapter reports to the attached system that a remove has been received.

All other MAC frames are processed normally as if the Adapter were inserted.

3.8.7.6 Request Initialization : Phase 4

Upon successful completion of Phase 3, the Adapter enters the final step of the Insertion Process. The purpose of Phase 4 is to request additional operational parameters. These parameters are associated with each station on the ring. The parameters received in this process replace the default parameters set at the start of the Ring Insertion Process.

The Adapter sends a series of Request Initialization MAC frames to the Ring Parameter Server Functional address. If one is returned with the ARI or FCI bits set, this indicates that a Ring Parameter Server is present on the ring. In this case, the Adapter waits for an Initialize Ring Station MAC frame from the Ring Parameter Server or a Change Parameters MAC frame from the Network Manager.

The Transmit Forward Process allows multiple layers of frames to be sent between Adapters to test a path between ring stations. The embedded frame to be forwarded must be a Transmit Forward MAC frame. Adapters which enter the Transmit Forward Process (through receipt of a Transmit Forward MAC frame) will transmit a Report Transmit Forward MAC frame to the Network Manager functional address upon stripping the forwarded frame from the ring.

3.8.8.1 Applicable MAC Frames

Table 3-15 describes the MAC frames which are used by the Transmit Forward Process.

TABLE 3-15. TRANSMIT FORWARD PROCESS — APPLICABLE MAC FRAMES

M-V (FRAME) NAME	DESTINATION CLASS	SOURCE CLASS	DESTINATION ADDRESS	SUBVECTORS		
				R/O		
				XMT	RCV	NAME
>09 Transmit Forward	>0	>4	target		R	>27 Frame Forward
>2A Report Transmit Forward	>4	>0	F(NM)	A		>2A Transmit Status Code

A = Always transmitted, R = Required

3.8.8.2 Transmit Forward MAC Frame Format

The Transmit Forward MAC frame is illustrated in Figure 3-18.

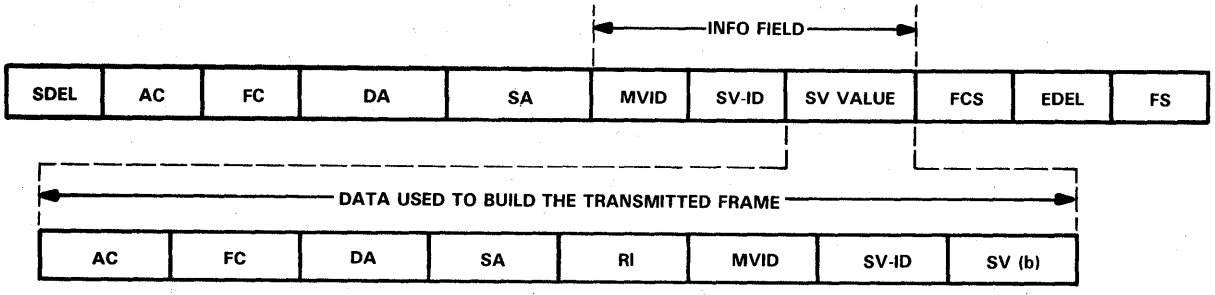


FIGURE 3-18. TRANSMIT FORWARD MAC FRAME

The subvector value (SV(b)) can have the same structure as the subvector value in the original frame. This data is transmitted as a frame by the ring station that receives this data.

The maximum length of a Frame Forward subvector is 254 bytes in a Transmit Forward MAC frame. The Adapter does not support length extension in this subvector.

TABLE 3-17. NETWORK MANAGEMENT REQUEST MAC FRAMES

M-V (FRAME) NAME	DESTINATION CLASS	SOURCE CLASS	DESTINATION ADDRESS	SUBVECTORS		
				R/O		
				XMT	RCV	NAME
>0E Request Station Address	>0	>4	target		O	>09 Correlator
>0F Request Station State	>0	>4	target		O	>09 Correlator
>10 Request Station Attachment	>0	>4	target		O	>09 Correlator

O = Optional

3.9.2.2 Network Management Response MAC Frames

The MAC frames originated by the Adapter in response to the request MAC frames shown in Table 3-17 are defined in Table 3-18.

TABLE 3-18. NETWORK MANAGEMENT RESPONSE MAC FRAMES

M-V (FRAME) NAME	DESTINATION CLASS	SOURCE CLASS	DESTINATION ADDRESS	SUBVECTORS		
				R/O		
				XMT	RCV	NAME
>22 Report Station Address	>4	>0	source address of received request frame	A A A A A A		>02 UNA >09 Correlator >0B Physical Drop >2B Group Address >2C Funct. Addr. >21 Reserved
>23 Report Station State	>4	>0	source address of received request frame	A A A		>09 Correlator >23 Adapter Software Level >29 Adapter Status Vector
>24 Report Station Attachment	>4	>0	source address of received request frame	A A A A A A		>09 Correlator >22 Product ID >2C Funct. Addr. >06 Enabled Funct. Classes >07 Allowed Access Priority >21 Reserved

A = Always transmitted

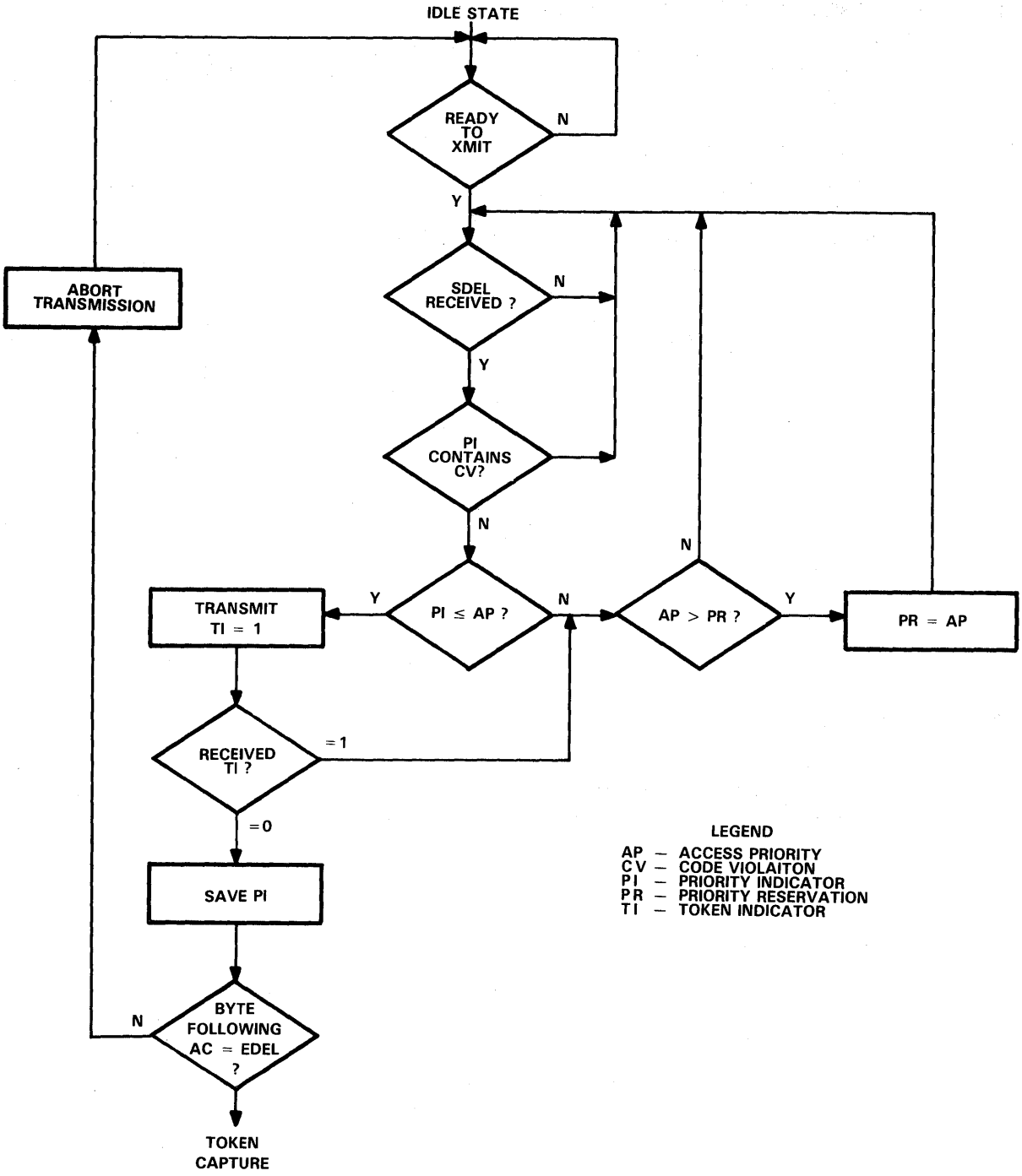


FIGURE 3-20 TOKEN CAPTURE FLOWCHART

Priority tokens may be released for transmission by the Priority State Machine when an Adapter has completed transmission of a frame, has stripped the frame, and subsequently releases a token. Since each ring station must have equal access to each token priority level, this state machine is responsible for assuring equal access, even in the event that access to a particular priority is interrupted by a higher priority. For this reason, this function is sometimes referred to as the "fairness" function.

To conceptually understand the priority control protocol, it is important to understand that the Adapter implements two independent but cooperating state machines: the Transmit Token Control State Machine (Section 3.10.2) and Priority Control state machine.

The Priority Control state machine utilizes the Priority Indicator (PI), Token Indicator (TI), and Priority Reservation (PR) fields of the the Access Control (AC) field AFTER the AC has been released from the Transmit Token Control state machine of the Adapter.

3.10.4.1 Priority State Machine

The Priority State Machine contains three major components:

1. Priority Control Delay.
2. The "new" last-in-first-out (LIFO) buffer.
3. The "old" last-in-first-out (LIFO) buffer.

The priority control delay is a nine bit delay introduced in the repeat path to allow the Priority State Machine to modify the Priority Indicator of the transmitted token, if a change is needed. This delay is only inserted when necessary to reduce this delay's effect on ring latency.

The "new" LIFO buffer is a four deep LIFO. Its last entry contains the priority to which the state machine last increased the token and from which the state machine has yet to decrease the token.

The "old" LIFO buffer also is a four deep LIFO. Its last entry contains the priority from which the state machine last increased the token and to which the state machine has yet to decrease the token.

With eight priority levels defined, the four entry limit on the LIFOs is sufficient. The Adapter can be responsible for up to four increases in the priority of the token.

The Priority State Machine is enabled when the Transmit Token Control issues a NEW token after stripping a transmitted frame from the ring. This state machine remains enabled until disabled, as described below.

TABLE 3-19. PRIORITY CONTROL STIMULI

STIMULI				OPERATION (NOTE 1)			
				NOT EMPTY STATE		EMPTY STATE	
PI<PR	PI="new"	PI<"new"	PR>"old"	TI=0	TI=1	TI=0	TI=1
0	0	0	0	Idle	Idle	REMOVE	Idle
0	0	0	1	Idle	Idle	REMOVE	Idle
0	0	1	0	CLEAR/REMOVE	CLEAR	**	**
0	0	1	1	CLEAR/REMOVE	CLEAR	**	**
0	1	0	0	POP/REMOVE	Idle	REMOVE	Idle
0	1	0	1	REPLACE	Idle	**	**
0	1	1	0	*	*	*	*
0	1	1	1	*	*	*	*
1	0	0	0	*	*	*	*
1	0	0	1	PUSH	Idle	PUSH	Idle
1	0	1	0	CLEAR/REMOVE	CLEAR	**	**
1	0	1	1	CLEAR/REMOVE	CLEAR	**	**
1	1	0	0	*	*	*	*
1	1	0	1	REPLACE	Idle	PUSH	Idle
1	1	1	0	*	*	*	*
1	1	1	1	*	*	*	*

Legend:
* — logically inconsistent
PI — Priority Indicator
TI — Token Indicator
"new" — last value pushed into "new" LIFO
"old" — last value pushed into "old" LIFO
Empty State — no entries on either the "new" or "old" LIFOs.
Not Empty State — entries on both the "new" and "old" LIFOs.
** — impossible because "new" = 0
PR — Priority Reservation

Note 1: If TI contains a code violation, the Priority Control remains idle

3.10.4.2 Priority Operation Example

This example assumes the existence of a three node ring with the following initial conditions.

1. Station A has a frame queued for transmission with an arbitrary Access Priority.
2. Station B has a frame queued for transmission with an Access Priority request of 4.
3. Station C has a frame queued for transmission with an Access Priority request of 6.
4. The initial location of the token is as shown in Figure 3-21. The token is priority-free and has no Priority Reservation specified.

This example uses a shorthand notation to represent the Priority Indicator (PI), Token Indicator (TI), and Priority Reservation (PR) of the circulating token or frame, as follows: PI/TI/PR. A zero in the TI position indicates a token, a one in this position indicates a frame. For Example:

4/0/0 - is a token of priority 4 with no reservation.
4/1/2 - is a frame of priority 4 with a reservation of 2.

Example - Step 2.

Referring to Figure 3-22, once the token is received by station A, it is used to transmit the enqueued frame. The token was captured because the PI was zero. At the point shown in the figure, the PI of the frame is still 0, the TI has now been set to one (indicating a frame), and the PR was left at zero.

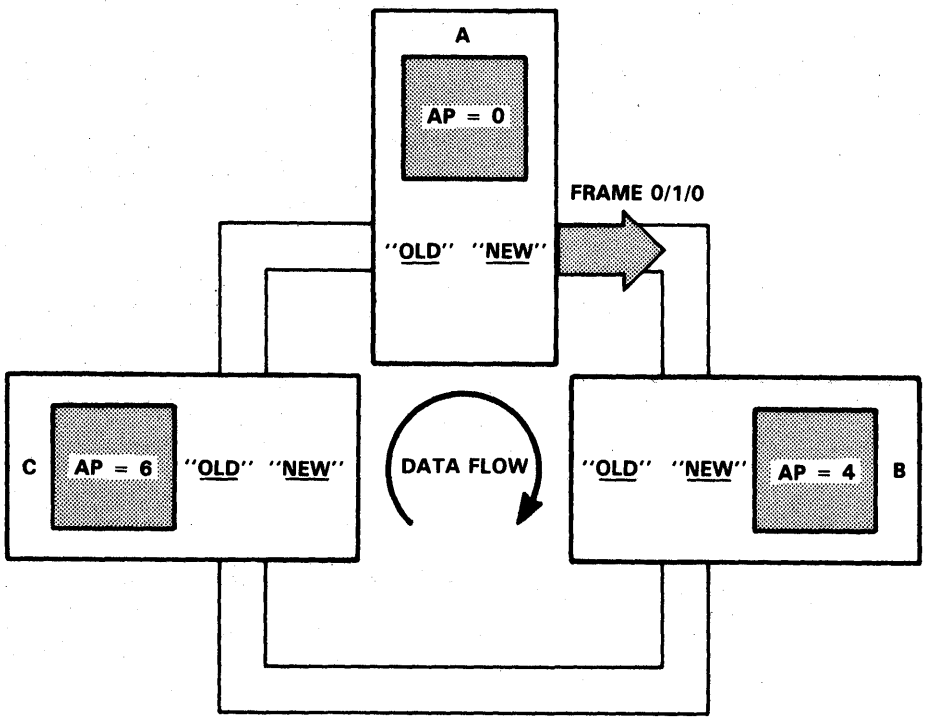


FIGURE 3-22. STATION A CAPTURES TOKEN AND BEGINS TRANSMISSION OF FRAME

Example - Step 4.

Referring to Figure 3-24, when station C receives the frame, it repeats the frame with a PR equal to 6. This is because Station C's enqueued frame has an access priority of 6 which is greater than the PR of the frame which was received. Thus, Station C also desires a priority token, but at a higher priority than Station B.

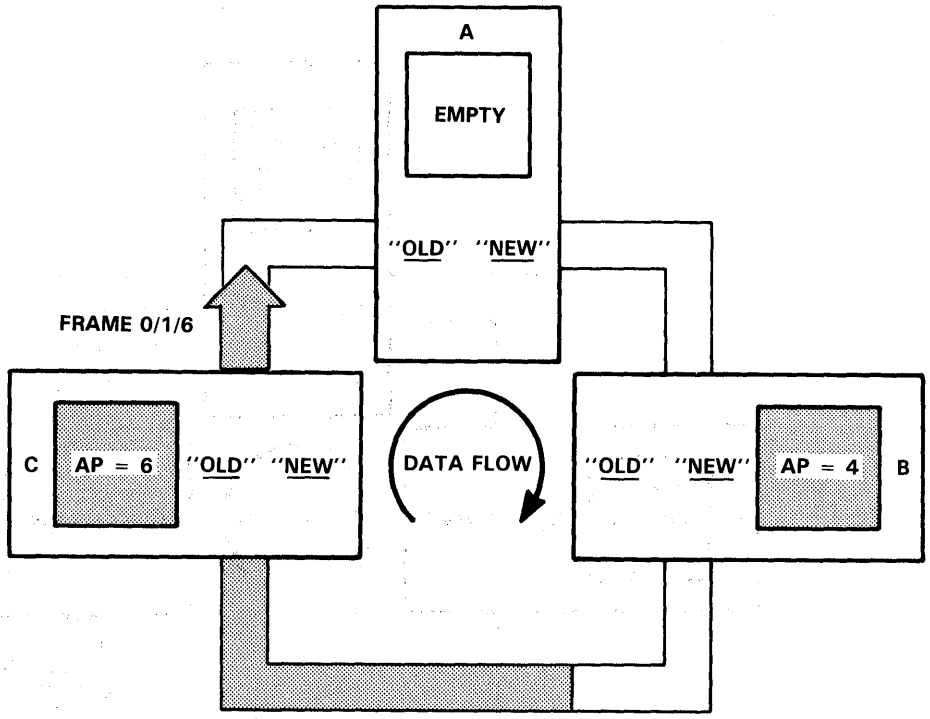


FIGURE 3-24. STATION C REPEATS FRAME AND CHANGES PR TO 6.

Example - Step 6.

Referring to Figure 3-26, Station A, having now stripped its frame from the ring, activates its Priority State Machine and releases a new token to the state machine. The Priority State Machine examines the PR field of the token and performs a PUSH operation on its 'new' and 'old' LIFO stacks (as can be determined from Table 3-19).

This PUSH operation results in 6 (the "new" token priority level) and 0 (the "old" priority level) being pushed into the "new" and "old" stacks, respectively.

The token now transmitted has the PI equal to 6, the TI equal to 0, and the PR equal to 0.

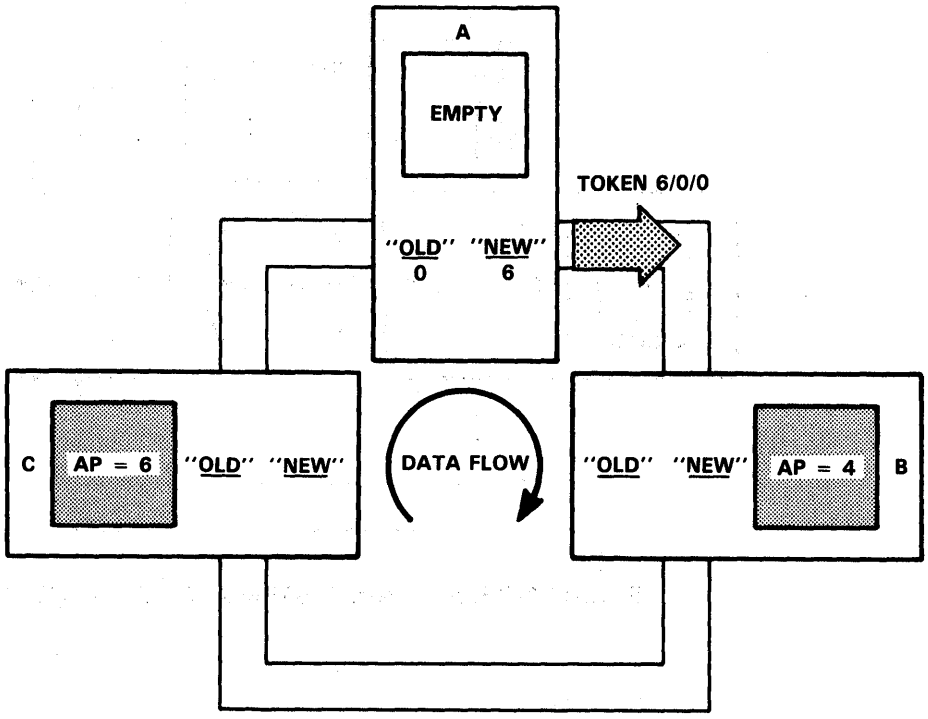


FIGURE 3-26. STATION A RELEASES A NEW TOKEN

Example - Step 8.

Referring to Figure 3-28, when Station C receives the priority 6 token, it now captures the token and begins transmitting its enqueued frame. The token was captured because the PI equaled the access priority of the enqueued frame.

Note that the PR field was left unchanged.

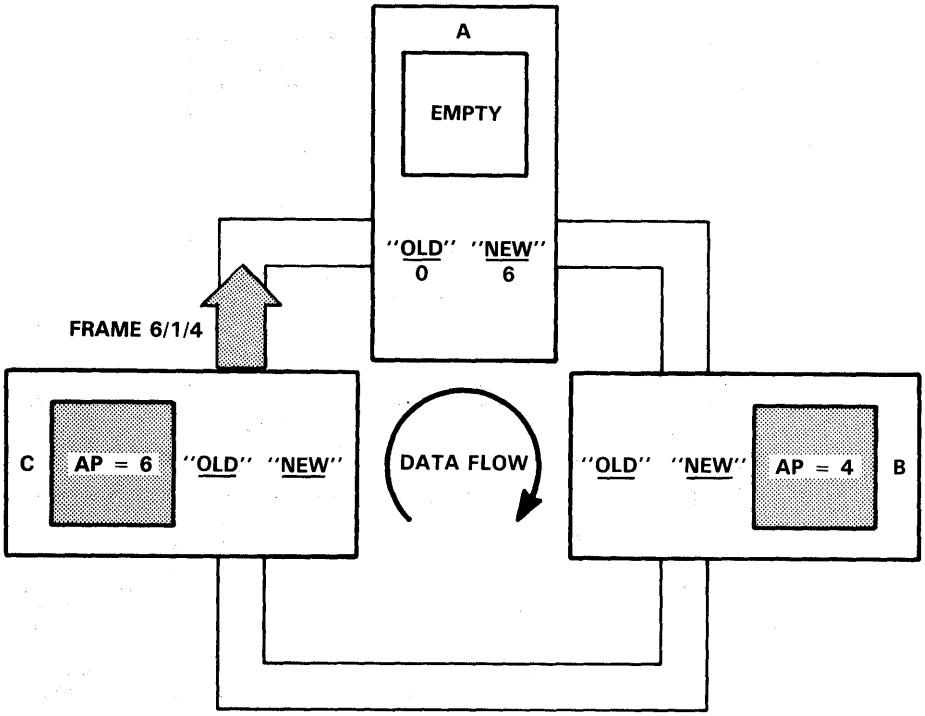


FIGURE 3-28. STATION C CAPTURES TOKEN AND BEGINS TRANSMISSION OF FRAME

Example - Step 10.

Referring to Figure 3-30, Station C receives the frame it transmitted and begins stripping the frame from the ring.

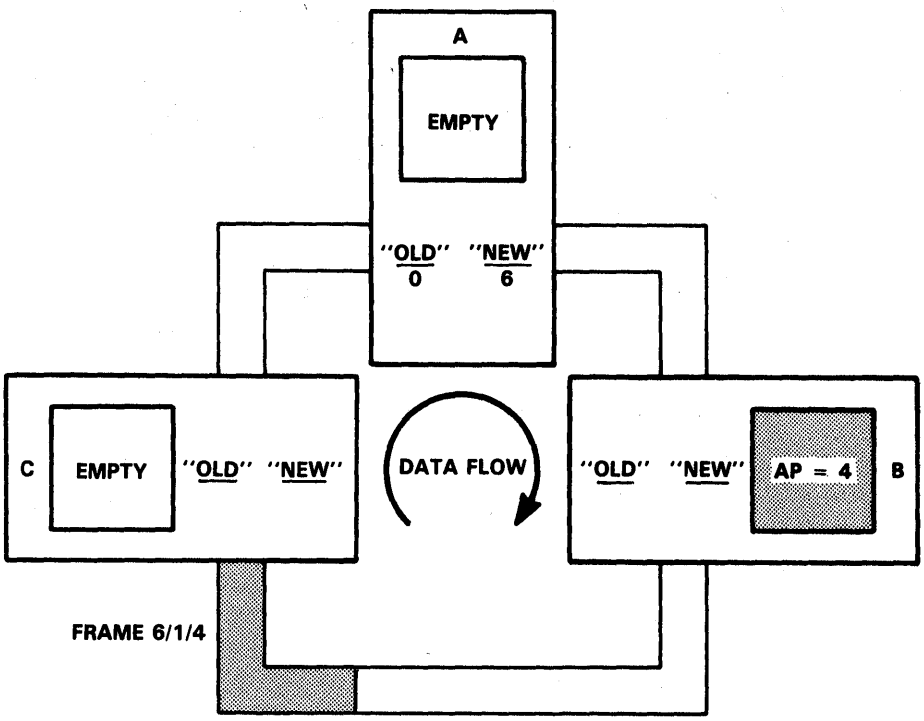


FIGURE 3-30. STATION C BEGINS STRIPPING THE FRAME FROM THE RING

Example - Step 12.

Referring to Figure 3-32, when Station A receives the token, it is passed to the Priority State Machine, which is still active. Because the PI is greater than the PR, the state machine concludes that a station requests that a priority token less than the current priority level be circulated. Thus, the state machine performs a REPLACE function on the stack (as can be determined by the stimuli conditions shown in Table 3-19), substitutes the PR for the PI, and transmits the token on the ring.

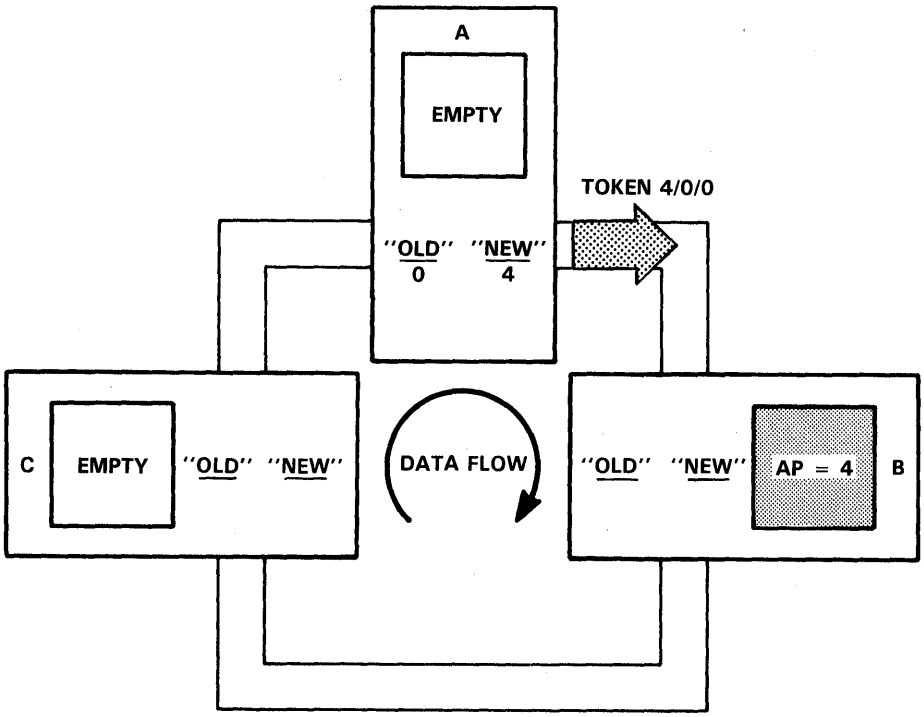


FIGURE 3-32. STATION A PERFORMS A REPLACE AND TRANSMITS THE TOKEN

Example - Step 14.

Referring to Figure 3-34, when the frame transmitted by Station B has completed circulation, Station B strips the frame from the ring.

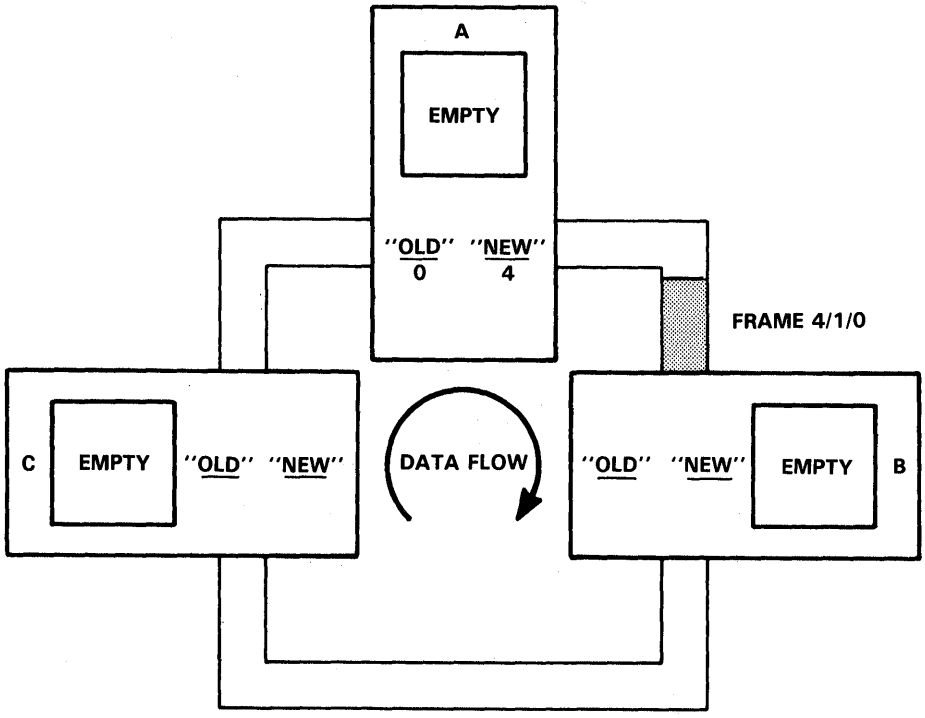


FIGURE 3-34. STATION B STRIPS ITS FRAME FROM THE RING

Example - Step 16.

Refering to Figure 3-36, when Station A receives the priority 4 token as sent from Station B, it is passed to the Priority State Machine. Because no other station requested a higher or lower priority level, the state machine performs a POP of its stacks and returns the token to its original priority-free state.

At this point, the ring is in a state similar to that shown in Figure 3-22.

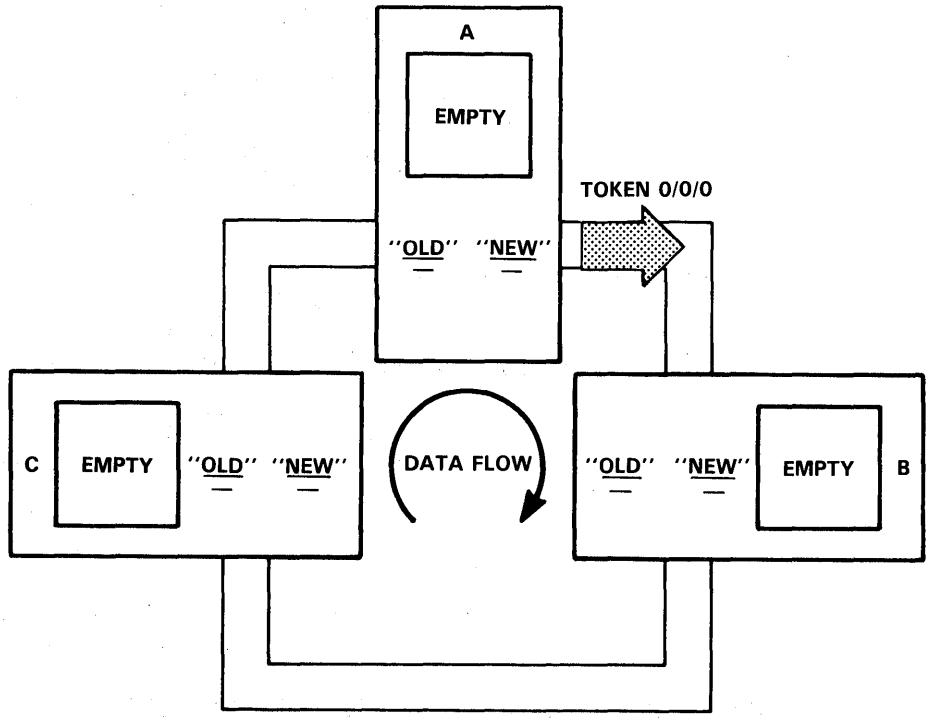


FIGURE 3-36. STATION A POPS ITS STACKS AND ISSUES PRIORITY-FREE TOKEN

This exercise provided a basic example of the priority operation of the Adapter. Note that each time the priority level of the token changes, each station on the ring is afforded equal opportunity to capture the token for frame transmission.

3.11.2 Attached Product Counters

The Attached Product Error Counters can be read by the attached system with the READ ERROR LOG Command.

The Attached Product Counters are incremented when:

1. A Soft Error is detected, and
2. The Adapter is inserted, and
3. The Adapter is in a normal state, and
4. The value of the counter does not equal 255.

When an error is detected and an Attached Product Counter is incremented from 254 to 255, the Counter Overflow Bit is set in Ring Status. The Attached Product Counters are reset when the counters are read by the attached system.

3.11.3 Isolating versus Non-Isolating Error Counters

The error counters maintained by the Adapter are defined as 'isolating' or 'non-isolating'. Isolating error counters isolate errors to a transmitting Adapter, a receiving Adapter, and the components (cabling, wiring concentrators) between those two adapters. These errors are counted only by the first detecting Adapter. Other adapters also detect these errors, but are prevented from counting these errors by the EDI (Error Detected Indicator) bit in the Ending Delimiter of the frame already being set to one by the detecting Adapter.

Non-isolating error counters count errors which could have been caused by any other Adapter on the ring (the fault cannot be isolated to a specific area of the ring). However, only the detecting Adapter counts the error.

3.11.4 Isolating Error Counters

The following are the Isolating Error Counters:

- Line Error Counter
- Burst Five Error Counter
- ARI/FCI Set Error Counter

3.11.5 Non-isolating Error Counters

The following are the non-isolating error counters:

- Lost Frame Error Counter
- Frame Copied Error Counter
- Receive Congestion Error Counter
- Token Error Counter

Table 3-22 defines the functions of these non-isolating error counters:

TABLE 3-22. NON-ISOLATING ERROR COUNTERS

CODE	DESCRIPTION
LOST FRAME ERROR	The lost frame error counter is contained in all Adapter configurations and is incremented when an Adapter is in transmit (stripping) mode and fails to receive the end of the frame it transmitted.
FRAME COPIED	The frame copied error counter is contained in all Adapter configurations and is incremented when an Adapter in the receive/ repeat mode recognizes a frame addressed to its specific address, but finds the ARI bits not equal to 00 (possible line hit or duplicate address).
RECEIVE CONGESTION	The receive congestion error counter is contained in all Adapter configurations and is incremented when an Adapter in the repeat mode recognizes a frame addressed to its specific address, but has no buffer space available to copy the frame (Adapter congestion).
TOKEN ERROR	This one-byte counter is contained in Active Monitor Adapter configurations and is incremented when the Active Monitor function detects an error with the token protocol as follows: 1. A token with priority of non-zero and the MONITOR COUNT bit equals one. 2. A frame and the MONITOR COUNT bit equals one. 3. No token or frame is received within a 10 millisecond window. 4. The starting delimiter/token sequence has a code violation (in an area where code violations must not exist).

3.12.1.2 Hard Error Reconfiguration

When hard errors occur on the ring, reconfiguration of the network is necessary to effect full recovery. Reconfiguration consists of removal or bypass of the faulty station(s) or cabling. Reconfiguration takes two forms: manual reconfiguration and automatic reconfiguration.

- Automatic Reconfiguration begins when the Adapter executes one of the Beacon Remove Functions (described in section 3.8) or when an internal hardware error is detected by the background diagnostics of the Adapter.
- Manual reconfiguration is necessary if the automatic reconfiguration functions have failed to recover the ring's normal token protocol. The fault location can be easily isolated by the beacon process.

3.12.1.3 Hard Error Recovery Time Lines

Hard errors can be classified as solid (fault invokes reconfiguration) or as intermittent (fault is removed from the ring before reconfiguration is required).

Solid Hard Error Recovery Time Line

Figure 3-37 illustrates the actions taken to recover from a solid hard error. Note that reconfiguration (either auto or manual) is required to re-establish a functional ring.

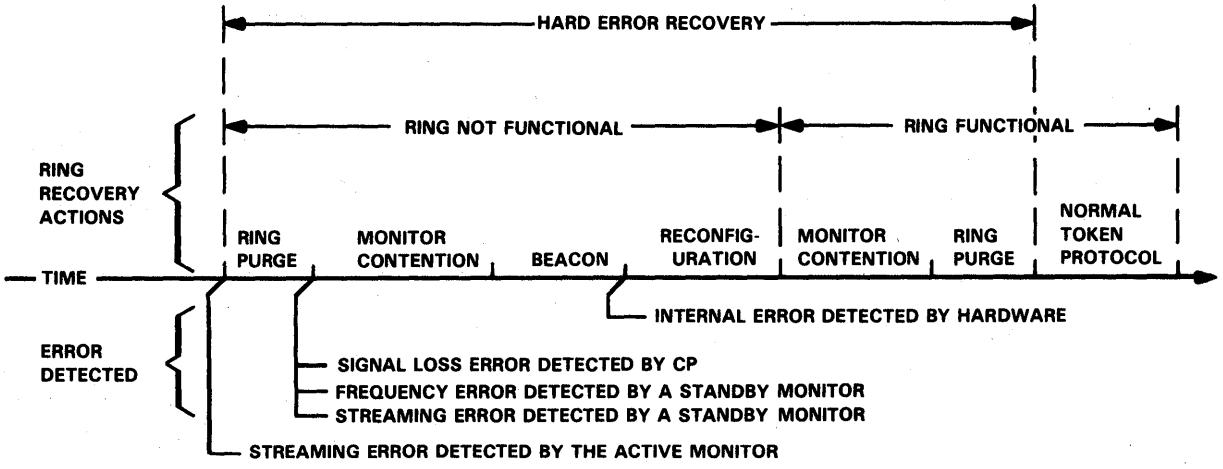


FIGURE 3-37. SOLID HARD ERROR RECOVERY TIME LINE

The following paragraphs define the terms used in Figure 3-37.

STREAMING ERROR detection by the Active Monitor causes the Adapter to enter Ring Purge, which fails, causing Monitor Contention, which also fails, causing Beacon Transmit Mode. When the condition causing streaming is removed, the ring is recovered using the Monitor Contention and Ring Purge Processes.

FREQUENCY ERROR detection by the Standby Monitor causes the Adapter to enter Monitor Contention, which if it fails, causes Beacon Transmit Mode (which requires reconfiguration). When the condition causing the frequency error is removed, the ring is recovered using the Monitor Contention and Ring Purge Processes.

TYPE 4 These errors require the Beacon, Monitor Contention, and Ring Purge functions to be executed.

The detection and recovery of lost frames caused by soft error conditions are not performed by the Adapter.

Type 1 Soft Errors

Type 1 errors consist of line errors, the multiple monitor condition, and the ARI/FCI set condition.

Line Errors. Each Adapter checks each frame copied or repeated for a valid FCS or a Manchester code violation. Adapters detecting these errors set the EDI (Error Detected Indicator) to one in the frame or token's ending delimiter.

If the received EDI bit is equal to zero, the Adapter increments its "Line Error Counter". If the received EDI bit is equal to one (line error previously detected by another Adapter), the counter is not incremented.

Multiple Monitors. When an Active Monitor receives a Ring Purge MAC frame or an AMP MAC frame that it did not transmit, it queues for transmission a Report Monitor Error MAC frame with an error code indicating the multiple monitor error. It then becomes a Standby Monitor and enters repeat mode. Note that this action may leave the ring without an Active Monitor. Another Standby Monitor will enter the Monitor Contention Process in this case.

ARI/FCI Set Error. Reception of more than one AMP or SMP MAC frame with ARI/FCI equal to zero without first receiving an intervening AMP MAC frame causes the Adapter to:

1. increment the 'ARI/FCI' Set Error Counter, and
2. terminate the Ring Poll Process (does not queue the SMP MAC frame).

This process leaves the Adapter downstream of a malfunctioning Adapter with an incorrect UNA (when the Ring Poll Process terminates), but Adapters downstream from the Active Monitor to the defective Adapter will have a correct UNA.

When an Adapter is unable to set the ARI/FCI bits upon receiving a frame, the following LAN functions do not operate correctly:

1. Higher-level protocols may not work correctly because of the inability of the Insertion Process to detect duplicate addresses.
2. A beacon transmitter may identify an incorrect upstream Adapter.
3. An Adapter MAC frame requiring Assured Delivery (Section 3.6.9.2) will not be assured when the destination Adapter fails to set the ARI/FCI bits.

Type 2 Soft Error

Type 2 soft errors consist of the burst 5 error, lost frame, multiple token, corrupted token, lost token, lost delimiter, circulating token, or circulating frame error conditions. These error conditions cause the Active Monitor to execute its Ring Purge Function and may cause frames to be lost.

Type 4 Soft Errors

The type 4 soft error is caused when Monitor Contention cannot be resolved. This error condition may also require hard error recovery.

This error condition or its resultant recovery may cause frames to be lost.

3.12.2.2 Soft Error Recovery Time Line

Figure 3-39 illustrates the recovery actions that take place as a function of time when one of the sort errors is detected.

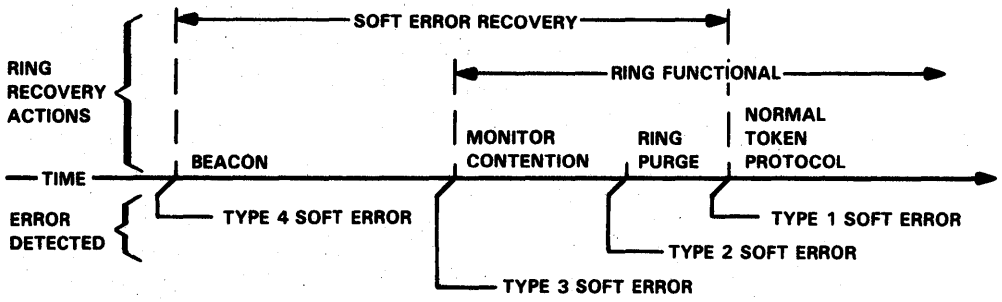


FIGURE 3-39. SOFT ERROR RECOVERY TIME LINE

3.12.3 Hard Error Recovery Examples

This section presents several examples of the hard error recovery process as previously described. The following examples are provided:

1. A signal loss is detected.
2. Transmit streaming is detected (not Claim Token MAC frames).
3. Receive streaming is detected (not Claim Token MAC frames).
4. Transmit streaming is detected (Claim Token MAC frames).
5. Two Adapters are transmitting streaming data (transmitter fault).
6. Two Adapters are receiving streaming data (receiver fault).

Case 2 - Receiver Malfunction

Adapter 185 detects a Signal Loss Error caused by its own receiver malfunction.

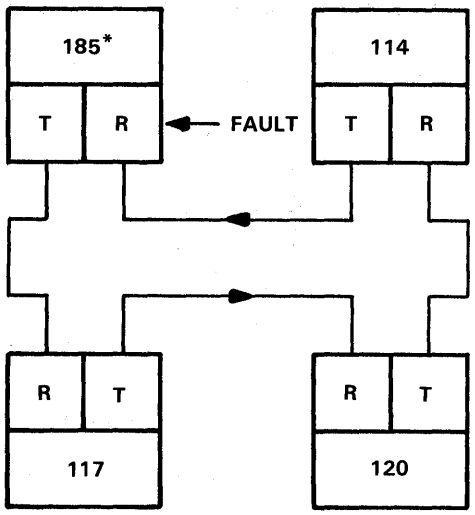


FIGURE 3-41. RECEIVER FAULT IN ADAPTER 185

1. Adapter 185 detects a Burst 4 error and transmits idles.
2. Adapter 185 detects a Burst 5 error.
3. The state of Adapters 114, 120 and 117 will vary depending upon which Adapter's token protocol timers expire first.
4. Adapter 185 detects the Signal Loss Error causing it to enter Contention Transmit Mode.
5. If Adapter 185 cannot resolve Monitor Contention, it enters Beacon Transmit Mode and transmits a Beacon MAC frame with a Beacon Type subvector equal to >0002 (signal loss).
6. Adapters 114, 120, and 117 enter Beacon Repeat Mode upon receiving the Beacon MAC frame from 185 with a lower error code.
7. Adapter 185 remains in Beacon Transmit Mode until it is removed from the ring by the Beacon Transmit Remove Function.

NOTE

Adapter 114 did execute the Beacon Receive Remove Function, but re-inserted into the ring since the Adapter's tests were successful.

8. Adapter 117 receives no Beacon frames for 200 milliseconds and so starts the Monitor Contention Process to recover the ring.

3.12.3.2 Transmit Data Streaming

Adapter 185 is transmitting data without regard to ring protocol (streaming data of any kind except Claim Token MAC frames). Adapter 185 does not respond to Ring Purge, but does recognize the Beacon MAC frame.

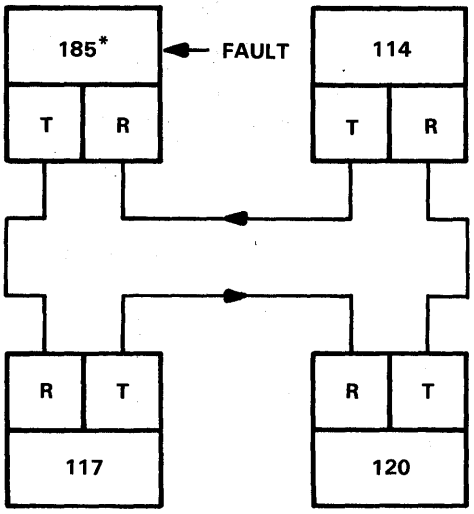


FIGURE 3-43. TRANSMITTER STREAMING FAULT IN ADAPTER 185

1. Depending on when their timers expire, any combination of Adapters may enter Monitor Contention repeat or transmit mode and start their internal watchdog timers for Monitor Contention (1 second).
2. Depending on when their contention timers expire, any combination of Adapters may enter Beacon Transmit Mode and transmit a Beacon MAC frame with a Beacon Type Subvector equal to >0003 (Adapters 117 never received a Claim Token MAC frame) or >0004 (Adapters received a Claim Token MAC Frame).
3. Adapter 117 detects a streaming data error, enters Beacon Transmit Mode and transmits a Beacon MAC frame with an error code of >0003 and a UNA identifying Adapter 185.
4. Adapters 114 and 120 enter Beacon Repeat Mode upon receiving the Beacon frame from Adapter 117 with a lower error code.
5. Adapter 117 remains in Beacon Transmit Mode until the streaming Adapter 185 is removed using the Beacon Receive Remove function.
6. Adapter 117 detects its own Beacon frames and enters the Monitor Contention Process to recover the ring.

3.12.3.4 Transmit Monitor Contention Streaming

Adapter 185 is transmitting Claim Token MAC frames without regard to ring protocol (streaming), and does not recognize the Ring Purge MAC frame (normal for a Monitor Contention transmitter), but receives the Beacon MAC frame.

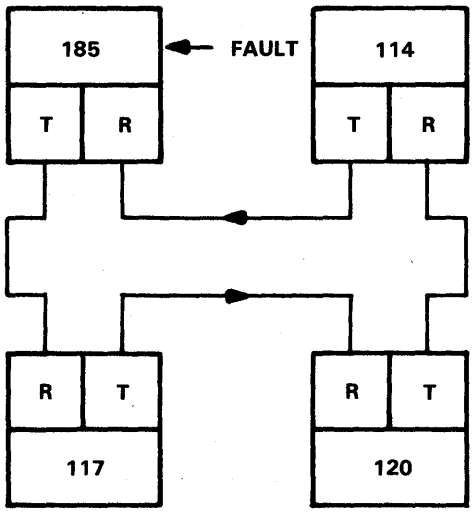


FIGURE 3-45. ADAPTER 185 STREAMING CLAIM TOKEN FRAMES

1. Adapters 114, 120, 117 all enter Monitor Contention repeat mode and start their watchdog timers (1 second) which limit the duration of the Monitor Contention Process.
2. Depending on when their timers expire, any combination of Adapters may enter Beacon Transmit mode and transmit a Beacon MAC frame with a Beacon Type Subvector (error code) equal to >0004 (Monitor Contention MAC frames have been received).
3. Adapter 117 detects the streaming Claim Token MAC frame error, enters Beacon Transmit Mode and transmits a Beacon MAC frame with an error code of >0004 and a UNA identifying Adapter 185.
4. Adapters 114 and 120 enter Beacon repeat mode upon receiving Adapter 117's Beacon MAC frame of an equal error code.
5. Adapter 117 remains in Beacon Transmit Mode until the streaming Adapter 185 is removed using the Beacon Receive Remove Function.
6. Adapter 117 detects its own Beacon frames and enters the Monitor Contention Process to recover the ring.

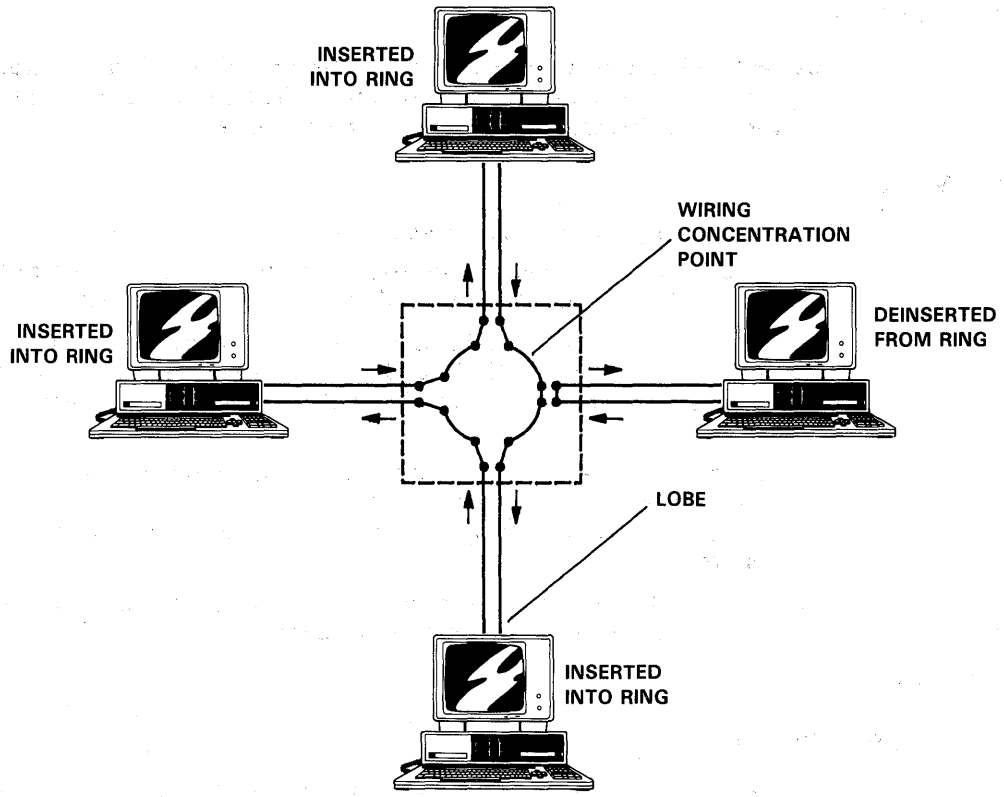


FIGURE 4-1. STAR-WIRED LOCAL AREA NETWORK

4.1.3.2 Adapter to Attached System Interface

The Adapter interface to the attached system is through the TMS38030 System Interface chip (SIF). This interface provides two user selectable modes: 808X mode and 680XX mode. These pin selectable modes allow the system designer flexibility in choosing the hardware interface most appropriate to his application. The 808X mode provides a compatible interface to the 808X series of CPU's, using either 8-bit or 16-bit data bus widths. The 680XX mode provides a compatible interface to the 680XX series of CPU's, with a 16-bit data bus width. Of course, the designer is not constrained to use these processor types in the attached system; the system designer should select the interface mode which best fits his system hardware.

The System Interface of the Adapter provides both direct I/O and DMA interfaces to the attached system. Direct I/O is used to handshake with the Adapter and to pass initialization parameters to the Adapter. All message transfers between the attached system and the ring are accomplished via the direct memory access interface. This provides for high-performance data transfer to and from the attached system.

COMMAND	CODE
OPEN	>0003
TRANSMIT	>0004
TRANSMIT HALT	>0005
RECEIVE	>0006
CLOSE	>0007
SET GROUP ADDRESS	>0008
SET FUNCTIONAL ADDRESS	>0009
READ ERROR LOG	>000A
READ ADAPTER BUFFER	>000B

FIGURE 4-4. ADAPTER COMMAND SET

4.1.5 Adapter Data Flow

The Adapter, at a high level of detail, performs these basic operations on the data stream passing through it on the ring:

1. Repeats the received data without copying the data.
2. Repeats and copies the received data.
3. Changes the state of single bits in the received data before re-transmitting it.
4. Originates the transmission of data on the ring.
5. Removes messages from the ring that it has previously transmitted.

The Adapter is made up of four functions; the Ring Interface (RI) circuit, the Protocol Handler (PH), the Communications Processor (CP), and the System Interface (SIF).

To insure integrity of the data flow between the attached system and the Adapter, each byte may be protected with a parity bit. In addition, the integrity of the data flow within the Adapter (i.e. on the Adapter Bus) is also assured with byte parity. Parity generation and checking to the System Interface is performed on both address and data types. Parity checking in this manner, coupled with protocol level data integrity checks, assures a high level of confidence in the validity of data transported on the ring.

A description of the data flow through the Adapter is described in the following paragraphs.

4.1.5.1 Receive Data Flow

On receive, data is taken from the local ring into the Ring Interface where it is re-shaped into distortion-free digital signalling elements. The Ring Interface performs no code conversion as its primary function is to provide synchronization to the received data stream and level translations to levels compatible with the Protocol Handler (TTL). Synchronization is achieved via an integrated phase-locked loop (PLL) which locks to the bit stream signalling rate. This clock is boundary aligned to the bit stream and is passed to the Protocol Handler for data extraction.

4.2 Adapter Interconnect

This section shows the interconnect of the TMS380 Adapter five chip set. The expansion of buffer RAM on the LAN Adapter bus is also described.

Figure 4-5 illustrates the interconnect schematic of the TMS38010 Communications Processor, the TMS38020 Protocol Handler, the TMS38030 System Interface, and the TMS38051 and TMS38052 Ring Interface components of the Adapter. This schematic also illustrates LAN Adapter bus memory expansion, which will be discussed in Section 4.2.1.

A discussion of the Ring Interface circuit containing the TMS38051, TMS38052, the watchdog timer, and burned-in address ROM is found in Section 4.5.

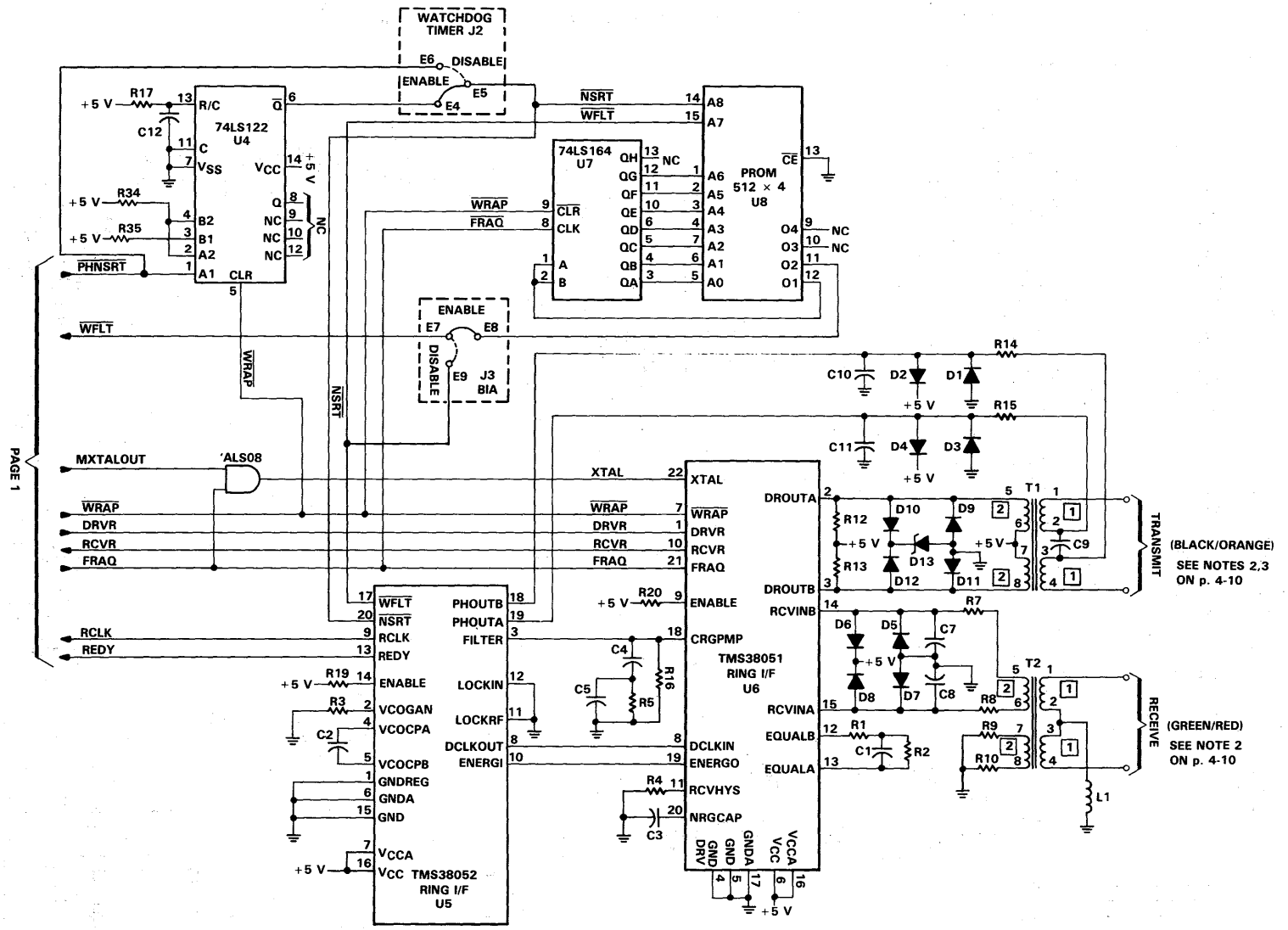
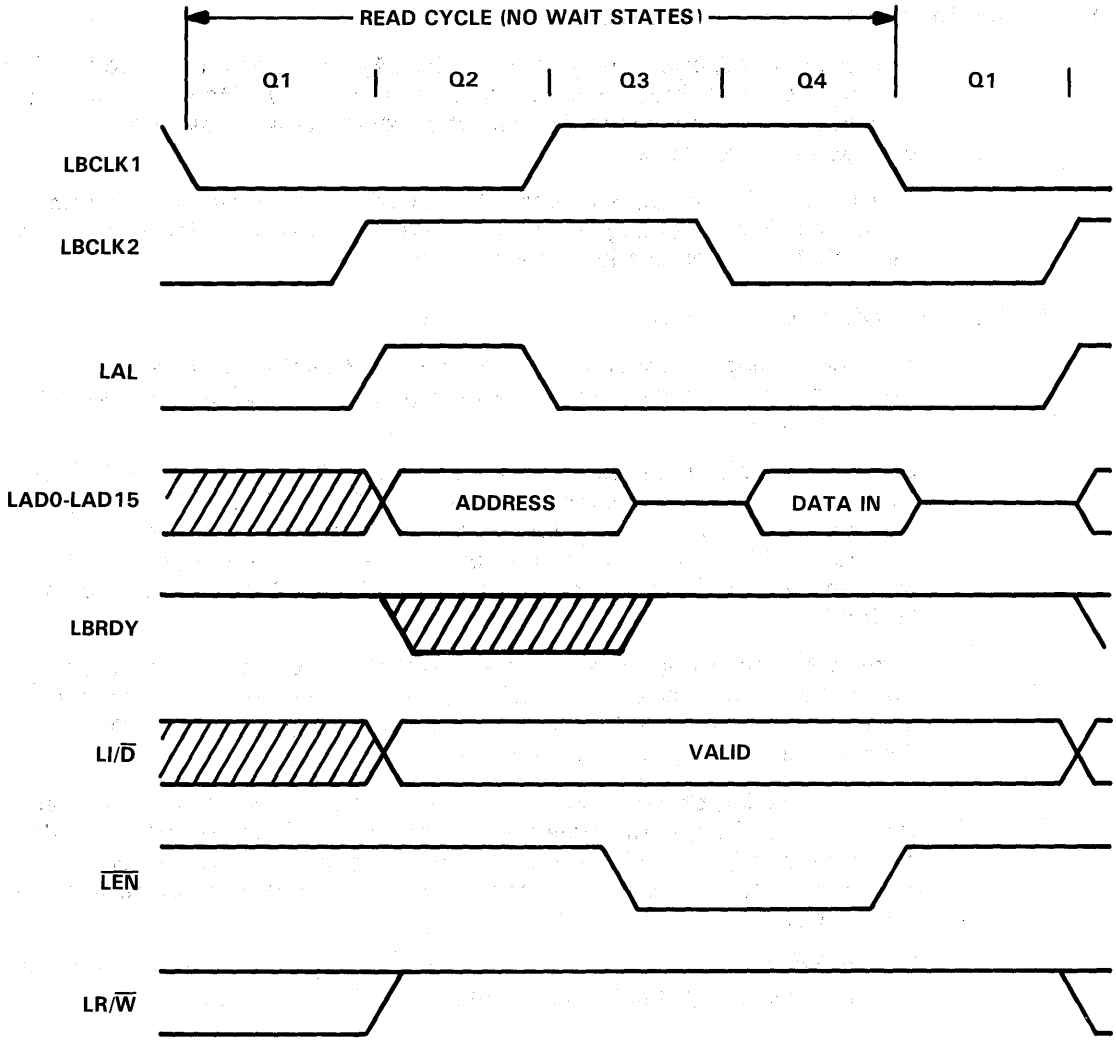


FIGURE 4-5. ADAPTER CHIP SET INTERCONNECT DIAGRAM (2 of 4)

LIST OF MATERIALS		
SYMBOL(S)	QTY	DESCRIPTION
C1	1	Capacitor, 180 pF, 5%
C2	1	Capacitor, 200 pF, 5%
C3	1	Capacitor, 6800 pF, 10%
C4	1	Capacitor, 8.2 μF, 10%
C5	1	Capacitor, 680 pF, 10%
C7, C8	2	Capacitor, 62 pF, 5%
C9	1	Capacitor, 0.1 μF, 10%
C10, C11	2	Capacitor, 8.2 μF, 20%
C12	1	Capacitor, 0.47 μF, 5%
D1-D4	4	Diode, 1N4004
D5-D12	8	Diode, 1N4148
D13	1	Diode, 1N5347B, 10 V, Zener
R1	1	Resistor, 121 Ω, 1%
R2	1	Resistor, 604 Ω, 1%
R3, R4	2	Resistor, 2.49 kΩ, 1%
R5	1	Resistor, 825 Ω, 1%
R7, R8	2	Resistor, 121 Ω, 1%
R9, R10	2	Resistor, 75 Ω, 1%
R12, R13	2	Resistor, 300 Ω, 5%
R14, R15	2	Resistor, 50 Ω, 5%, 2 W
R16	1	Resistor, 330 kΩ, 10%
R17	1	Resistor, 150 kΩ, 5%
R18	1	Resistor, 2.3 kΩ, 5%
R19-R25	3	Resistor, 4.7 kΩ, 10%
R27-R36	10	Resistor, 1 kΩ, 10%
L1	1	Coil, 56 μH, 10%
T1, T2	2	Transformer, PE63838-001 or TNI2837
Y1	1	Crystal, Oscillator KYOCERA KX0-01

NOTES:
1. Care must be exercised during card layout to assure that the capacitive loading differences between LBCLK1 and LBCLK2 does not exceed 10 pF.
2. No polarity is specified for the transmit or receive twisted pair. Therefore, signal connections to transformers T1 and T2 may be modified to accommodate specific PWB layouts.
3. No polarity is specified for signals PHOUTA and PHOUTB. Therefore, the connections on the transformer T1 are interchangeable.

FIGURE 4-5. ADAPTER CHIP SET INTERCONNECT DIAGRAM (4 of4)



(a) LAN ADAPTER BUS READ CYCLE

FIGURE 4-6. BASIC TIMING FOR LAN ADAPTER BUS TRANSFERS

4.2.1.4 Wait State Generation

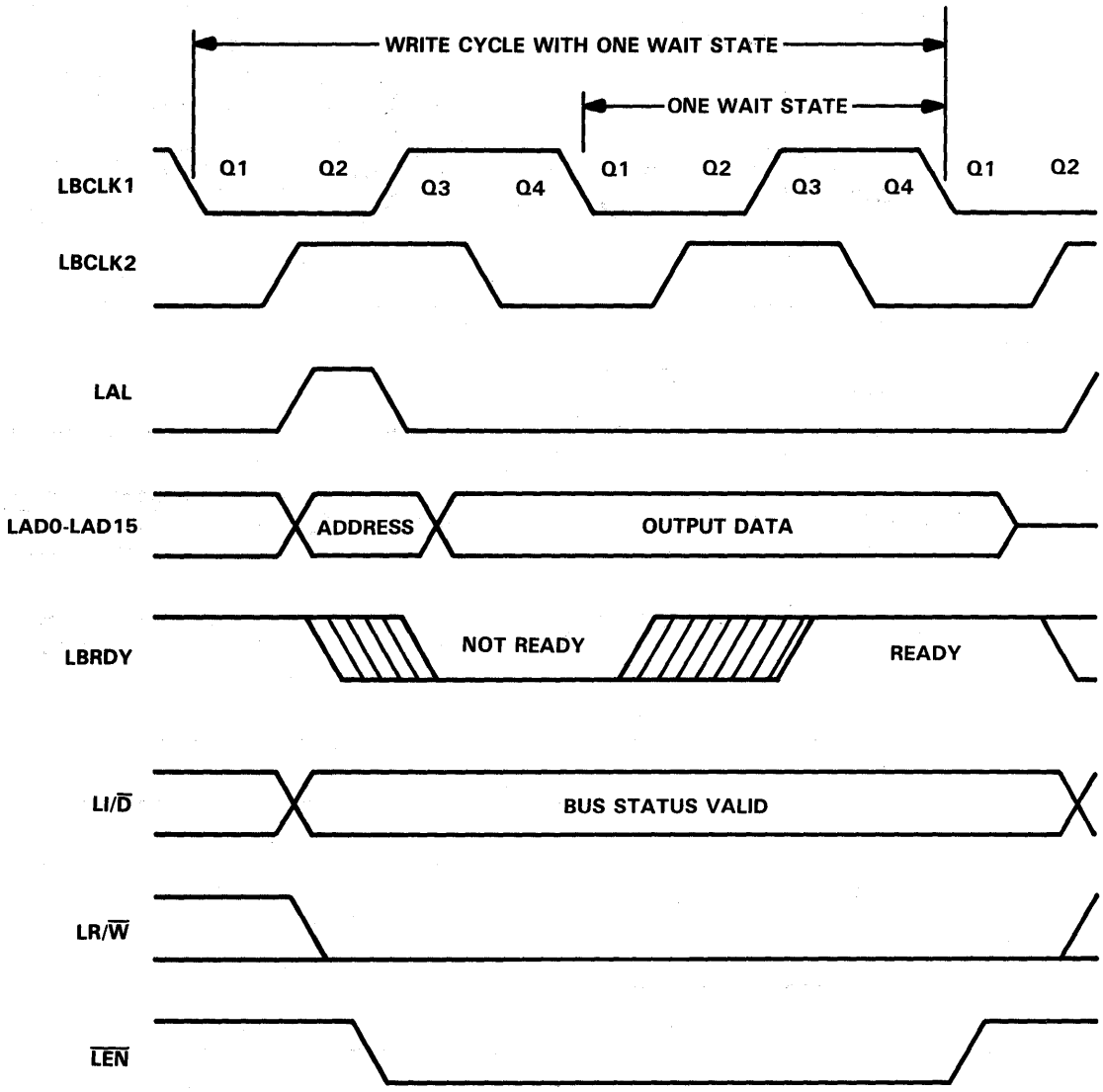
Each bus cycle is minimally one LBCLK period in duration, as shown in Figure 4-6, but can be extended by one additional LBCLK period to accommodate slow memories. An additional LBCLK period generated for this purpose is referred to as a "wait state". Wait states are permitted only for program store for the Communications Processor and are not allowed for RAM data storage.

The LBRDY signal may be driven low by either the bus master or the bus slave to extend LAN Adapter bus memory and internal bus cycles as shown in Figure 4-7. Whether the CP chip is master or slave, it will sample LBRDY as an input. The PH chip will sample LBRDY when it is accessed as a slave (i.e. an external master may request a wait state when accessing the PH ROM or a PH control register), but it will NOT honor wait states when it is the bus master. The master (on writes) or slave (on reads) will continue to drive output data as long as LBRDY is deasserted.

External circuitry may generate a wait state by driving LBRDY low (via open collector) before the falling edge of LBCLK2. Since wait states continue to be generated until LBRDY is driven high, LBRDY must be released in time to prevent a second wait state from occurring. As long as LBRDY is held low, the processor is forced to wait: it is frozen in its present microinstruction (or 'machine') state and is allowed to proceed to the next state. The CPU cannot respond to an interrupt request or bus request until LBRDY is released. This applies to non-memory as well as memory cycles controlled by the Communications Processor.

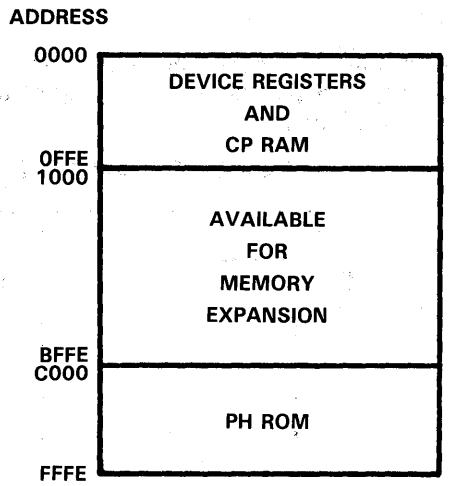
NOTE

When the Communications Processor accesses on-chip RAM or registers, LBRDY must not be driven low.



(b) LAN ADAPTER BUS WRITE CYCLE WITH WAIT STATE

FIGURE 4-7. LAN ADAPTER BUS TRANSFERS WITH ONE WAIT STATE (concluded)



NOTE: A15 on LAN Adapter memory cycles is always high.

FIGURE 4-8. LAN ADAPTER BUS MEMORY MAP

Figure 4-5 demonstrates how expansion RAM may be added to the Adapter. This expansion using HM6264 8K x 8 static RAM devices provides an additional 16K bytes of buffer for transmit and receive frames. The address is demultiplexed with two 'AS373 latches. Data is driven to/from the memory components with 'AS245 bus transceivers. The LR/$\overline{W}$ signal must be latched (shown with positive-edge triggered FF 'LS74) before being used as the direction signal to the AS245s, because LR/$\overline{W}$ may change before $\overline{LEN}$ is deasserted. $\overline{LEN}$ is used, in conjunction with address decode, to enable the '245s. The latched inversion of LR/$\overline{W}$ is NANDed with LBCLK1 to form the active-low write strobe to the RAMs. Appropriate decode circuitry forms the chip select to the memories. The 16K bytes of RAM are decoded starting at address location >4000.

Also shown in Figure 4-5 are sockets for EPROMs mapped starting at location >C000. The sockets allow the ROM space of the Protocol Handler to be displaced by external EPROMs. Thus, alternative programs (debug software or modified Adapter software) may be provided for the Communications Processor. Note that jumpers J1 and J4 must be set to disable the Protocol Handler ROM and enable the EPROM in this case.

The performance requirements for the memory devices shown in Figure 4-5 are calculated in Table 4-2. The calculations are made assuming a read cycle since the effect of the accumulated delays through the various buffers is more critical for a read cycle than for a write cycle. The access time requirement for the memory device used in each of these cases is calculated assuming worst-case component delays for all devices.

4.3.2 Direct I/O Interface

The direct I/O interface consists of four word-aligned (even address) address locations which are normally mapped into either the I/O or memory address space of the attached system. These address locations address a register set within the SIF through which the Adapter may be controlled by the attached system. The use of these registers by the attached system software will be discussed in detail in Section 4-4, System Software Interface. These registers are defined as follows:

- Interrupt Register
- Data Register
- Data Register with address auto-increment
- Address Register

These registers are selected with register select lines SRS0-SRS2. Register select SRS2 is used with the 808X-mode 8-bit data bus interface to select the even address or odd address byte to be transferred. With 16-bit 808X interfaces, SRS2 is used to select the even byte to be transferred during byte operations and $\overline{SBHE}$ is used to select the odd byte. Table 4-4 summarizes these registers:

TABLE 4-4. SIF REGISTER SELECTION

SRS0	SRS1	SRS2	REGISTER SELECTED
L	L	note	Data Register
L	H	note	Data Auto-increment Register
H	L	note	Address Register
H	H	note	Interrupt Register

NOTE: SRS2 is used to to address bytes in 8-bit mode.

4.3.2.1 808X Mode DIO Interface

808X mode is selected by tying the SI/$\overline{M}$ pin of the SIF to a high logic level as shown in Table 4-3. This mode facilitates interface to the 808X family of CPU's by reconfiguring the SIF pin functions to be compatible with these CPUs. In addition, the S8/$\overline{16}$ pin may be tied either low or high to select an 8-bit data bus or 16-bit data bus interface.

808X Mode DIO Data Organization

Because of differences between the byte ordering scheme defined by the 808X series CPU and the Adapter, care must be exercised to assure proper byte orientation when performing DIO operations in 808X mode.

Referring ahead to Figure 4-13, note that the 808X format defines byte 0 as the most-significant byte which resides on an even address boundary as the 'low' byte. Byte 1 is defined as the least-significant byte which resides on an odd address boundary as the 'high' byte. The Adapter assumes opposite convention with byte 0 and byte 1 on high and low bytes, respectively.

Thus, the attached system must swap bytes prior to transfer to or from the Adapter DIO registers to maintain proper orientation.

808X Interface Pins

Table 4-5 describes the functions of the system interface pins of the SIF when configured in 808X mode (SI/$\overline{M}$ tied high) for the direct I/O interface. Many of these pins are also defined in the DMA interface. Pins used for both DIO and DMA interfaces will be noted below, and Section 4.3.3 provides an explanation of the DMA interface.

808X Multiplexed and Non-Multiplexed Bus

Two direct I/O interfacing options are provided in 808X mode; multiplexed and non-multiplexed interfaces. The non-multiplexed option is suitable for expanded configurations in which the address/data bus from the 808X CPU has been demultiplexed into physically separate address and data lines. In this case, the system chip-select ($\overline{SCS}$) and the system register select (SRS0-SRS2) inputs are required to remain stable and valid for the duration of the access cycle.

The multiplexed option is provided to reduce the chip count in minimum-chip systems, in which the Adapter's SIF is interfaced directly to the the multiplexed address/data bus of the attached system. In this case, the system chip select ($\overline{SCS}$) and the system register select (SRS0-SRS2) inputs are latched within the SIF chip at the beginning of the cycle.

These two options are selected by use of the system register address strobe (SRAS) which serves as a latching signal in a multiplexed interface. In the 808X mode, the system chip select ($\overline{SCS}$) and the system register select (SRS0-SRS2) are fed into a transparent latch as they come on-chip. As long as the SRAS signal is at a high level, the outputs of the on-chip latch follow the inputs. When SRAS is brought low, the outputs of the latch are frozen at the levels present at the time of the falling edge of SRAS. For a non-multiplexed interface, SRAS is disabled by tying it inactive-high. If SRAS is coupled into the external address latch enable (ALE) of the 808X memory bus, a multiplexed interface may be configured.

808X in 16-bit Mode

When the S8/$\overline{16}$ pin is tied low, the System Interface (SIF) is configured for 16-bit mode. This mode provides full 16-bit data transfers between the Adapter and the attached system interface bus. Each of the four 16-bit registers is written or read in a single DIO access.

The address map of the 808X 16-bit interface is shown in Table 4-6.

TABLE 4-6. 808X 16-BIT ADDRESS MAP

(A1) SRS0	(A0) SRS1	$\overline{SBHE}$ = 0 MSB	SRS2 = 0 LSB
0	0	DATA	DATA
0	1	DATA/INC	DATA/INC
1	0	ADDRESS	ADDRESS
1	1	INTERRUPT	INTERRUPT

808X in 8-bit Mode

When the S8/$\overline{16}$ pin is tied high, the System Interface (SIF) is configured for 8-bit mode. In operating in 8-bit mode, each word register is written or read as a sequence of two bytes. During data transfers between the Adapter registers and the 808X interface, the even byte (SRS2 = 0) is written during the first bus cycle and the odd byte (SRS2 = 1) is written during the second cycle. In 808X processors, the even bytes and odd bytes correspond to the least significant and most significant bytes, respectively, of the memory word. Note that this is inconsistent with the Adapter's System Interface as the even addressed byte corresponds to the most significant byte and the odd address corresponds to the least significant byte. Thus, bytes must be swapped within host system memory before being written to the System Interface.

The address map of the 808X 8-bit interface is shown in Table 4-7.

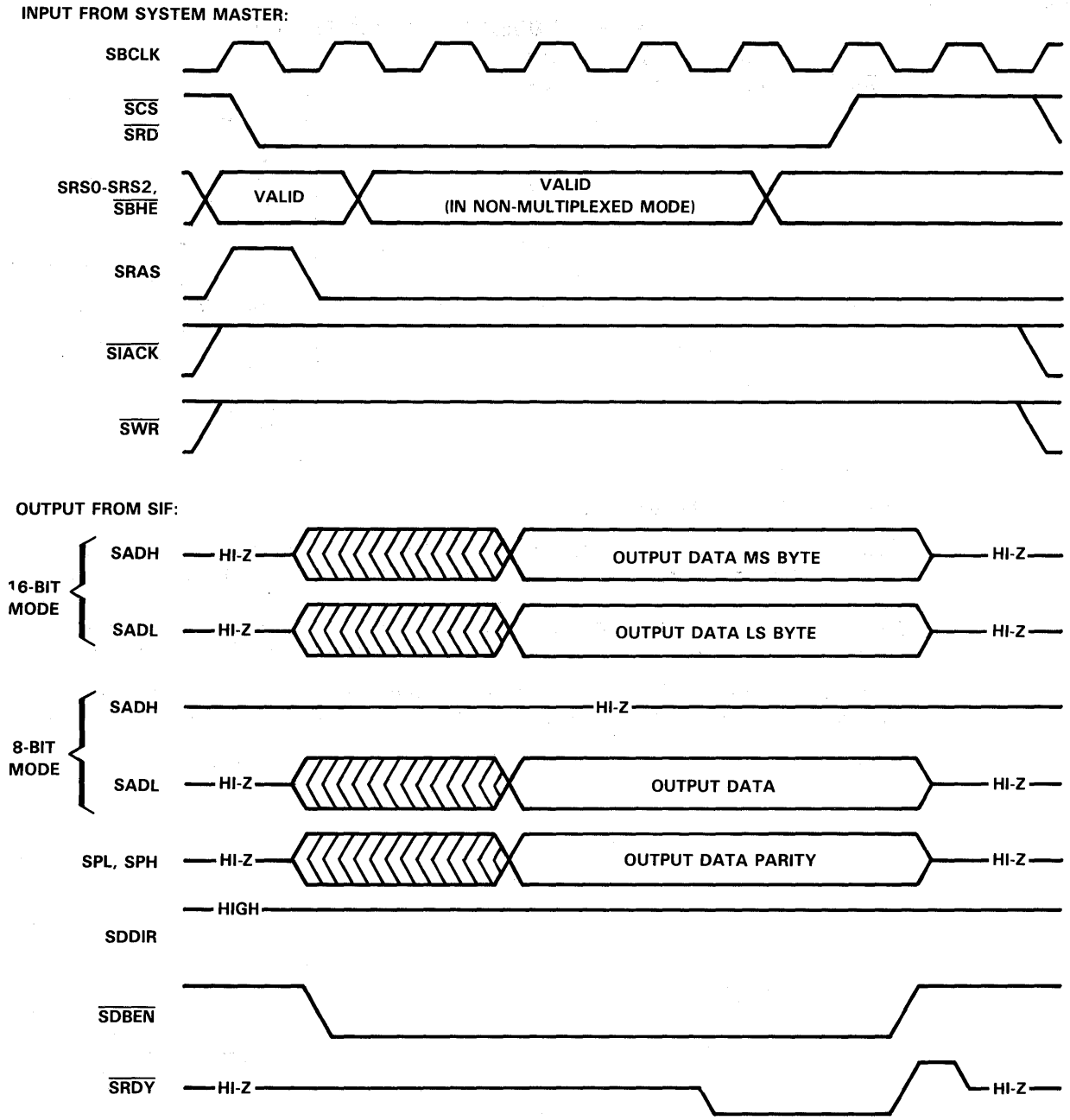


FIGURE 4-9. 808X DIO READ CYCLE

The timing illustrated in Figure 4-9 is described below:

1. In the quiescent state the system deasserts SCS, SIACK, SRD, and SWR. The SIF floats the SAD bus, and drives both SDDIR and SDBEN high. The SIF also floats its SRDY pin, but because SRDY has an internal pullup resistor (nominal 10K ohms) attached to it, the signal floats high (negated).

13. When the SIF detects that it has driven its $\overline{\text{SRDY}}$ signal high at the pin, it floats the signal, returning to the quiescent state.
14. The system must hold $\overline{\text{SRD}}$ negated for a minimum period before reaccessing the SIF. $\overline{\text{SCS}}$ must be negated between consecutive accesses to the same 16-bit register address (SRS0, SRS1 and SRS2 do not change). $\overline{\text{SCS}}$ may be kept asserted, however, between accesses to the two bytes of the same 16-bit register address (only SRS2 changes) but must be negated between accesses to two different 16-bit register addresses (SRS0 or SRS1 change). The system must also hold the previously inactive signals $\overline{\text{SWR}}$ and $\overline{\text{SIACK}}$ negated for a minimum period following a read operation.

The System Interface reloads the Data register after every write to the Address register. The SIF also writes the contents of the Data register to Adapter RAM after every write to the Data register. If the attached system attempts to read or write the Data register before this operation is complete, the $\overline{\text{SRDY}}$ line will remain inactive-high until the System Interface is prepared to complete the system bus cycle. Detail on this timing may be found in the TMS38030 System Interface data sheet.

808X DIO Write Cycle Sequence.

The sequence of events which occur during a direct I/O write cycle is shown next. A relational timing diagram is presented and is followed by a detailed description of the sequence. This sequence is based upon the non-multiplexed option described previously, however, it may apply as well to the multiplexed option with the exception that the chip-select and register select inputs must remain valid only until they are latched.

Specific timing as it relates to device switching characteristics is not presented here, but may be found in the TMS38030 System Interface data sheet.

Figure 4-10 depicts an 808X mode direct I/O write cycle:

2. Starting the DIO cycle, the system (bus master) asserts a register address on the $\overline{SBHE}$ and SRS0-SRS2 lines and asserts SRAS high. In 8-bit mode, $\overline{SBHE}$ is ignored.
3. The system asserts $\overline{SCS}$ low, keeping $\overline{SIACK}$ negated high.
4. The system optionally deasserts SRAS low, latching the SRS0-SRS2 and $\overline{SCS}$ inputs. SRAS may be tied high if the SRS0-SRS2 and $\overline{SCS}$ inputs can be held until $\overline{SRDY}$ is activated.
5. The system asserts $\overline{SWR}$ low, keeping $\overline{SRD}$ negated high. The system need not necessarily drive $\overline{SCS}$ before $\overline{SWR}$.
6. The SIF (bus slave), drives SDDIR low asynchronously from the activation of $\overline{SWR}$ and $\overline{SCS}$. This sets up the direction for the system bus drivers.
7. The SIF synchronizes $\overline{SCS}$ and all data strobes to the falling edge of SBCLK. When it samples both $\overline{SCS}$ and $\overline{SWR}$ low, it starts the internal register access. Due to an internal synchronizer circuit, $\overline{SCS}$ or $\overline{SWR}$ may be recognized low even if they fall after the falling edge of SBCLK.
8. On the third rising edge of SBCLK following the sample of $\overline{SCS}$ and $\overline{SWR}$ low, the SIF asserts $\overline{SDBEN}$ low, enabling the system bus lines onto the SIF SAD lines.
9. If the SIF is busy performing a read or write to internal Adapter memory as a result of an earlier DIO operation, it waits at this point until the internal operation is complete.
10. On the fifth rising edge of SBCLK (assuming no wait to complete a previously started DIO operation), the SIF latches the input data. On single-byte transfers, the half of the SAD bus not involved in the transfer is ignored, as shown below:

TABLE 4-9. 808X DIO WRITE DATA BUS CONTROLS

808X 16-BIT MODE WRITE			
BUS CONTROLS		SAD INPUTS	
$\overline{SBHE}$	SRS2	SADH, SPH	SADL, SPL
0	0	DATA MSB	DATA LSB
0	1	DATA MSB	don't care
1	0	don't care	DATA LSB
1	1 (†)	don't care	don't care
808X 8-BIT MODE WRITE			
BUS CONTROLS		SAD INPUTS	
$\overline{SBHE}$	SRS2	SADH, SPH	SADL, SPL
X	0	don't care	DATA LSB
X	1	don't care	DATA MSB

(†) Illegal input combination

11. After latching the input data, the SIF deasserts the $\overline{SDBEN}$ signal high, disabling the system bus onto the SAD bus.
12. After detecting that $\overline{SDBEN}$ is high at its output pin, the SIF activates $\overline{SRDY}$ by driving it low.

TABLE 4-10. INTERFACE PIN FUNCTIONS — 680XX MODE

PIN	FUNCTION
SI/$\overline{M}$	SYSTEM 808X/680XX MODE SELECT. This input must be tied low for 680XX mode.
S8/$\overline{16}$	SYSTEM 8/16 BIT BUS SELECT. This pin must be tied low when in 680XX mode.
$\overline{SCS}$	SYSTEM CHIP SELECT. This input must be asserted low prior to direct I/O read or write cycles by the attached system.
SRS0-SRS2	SYSTEM REGISTER SELECT. These inputs select the word or byte to be read or written during a direct I/O access.
SRNW	READ/NOT WRITE. This input pin serves as a control signal which is high to indicate a read cycle and low to indicate a write cycle. During DMA operations, this pin is driven as an output.
$\overline{SLDS}$	LOWER DATA STROBE. This input is used as the lower data strobe to select the lower (odd) byte for transfer on the 16-bit data bus. This pin is an output during DMA operations.
$\overline{SUDS}$	UPPER DATA STROBE. This pin is an active-low strobe indicating that data is transferred on the most significant byte of the system bus.
$\overline{SDSTACK}$	DATA TRANSFER ACKNOWLEDGE. This output is an active-low data transfer acknowledge used to signal to the bus master that a data transfer is complete. $\overline{SDTACK}$ is internally synchronized to SBCLK. This pin is an input during DMA operations.
SDDIR	SYSTEM DATA DIRECTION. This output provides a signal to the external data buffers indicating the direction in which data is moving. For DIO writes, SDDIR is low; for DIO reads, SDDIR is high. During DMA operations, this pin assumes opposite polarity (i.e. SDDIR is low for DMA reads and high for DMA writes). When the System Interface is not involved in a read or write operation, SDDIR is high by default.
$\overline{SDBEN}$	SYSTEM DATA BUS ENABLED. This output provides an active-low signal to the external data buffers which allows them to leave the high-impedance state and begin to transmit data. This pin is also driven during DMA operations.
SBCLK	SYSTEM BUS CLOCK. This is the external clock signal with which the SIF synchronizes its bus timing. For asynchronous buses, any TTL-level oscillator signal may be applied.
SADH0-SADH7	SYSTEM ADDRESS/DATA BUS — HIGH BYTE. This is the most significant byte of the 16-bit address/data bus. It is attached to the host system address/data bits 15-8 (using 680XX-standard bit numbering conventions). The most significant bit is SADH(0) and the least significant bit is SADH(7). This bus is driven as an output during DMA operations.
SADL0-SADL7	SYSTEM ADDRESS/DATA BUS — LOW BYTE. This is the least significant byte of the 16-bit address/data bus. It is attached to the host system address/data bits 7-0 (using 680XX-standard bit numbering conventions). The most significant bit is SADL(0) and the least significant bit is SADL(7). This bus is driven as an output during DMA operations.
SPH	SYSTEM PARITY HIGH. Contains an odd-parity bit for each data or address byte transmitted over SADH0-SADH7. This line is an output during DMA operations.
SPL	SYSTEM PARITY LOW. Contains an odd-parity bit for each data or address byte transmitted over SADL0-SADL7. This line is an output during DMA operations.

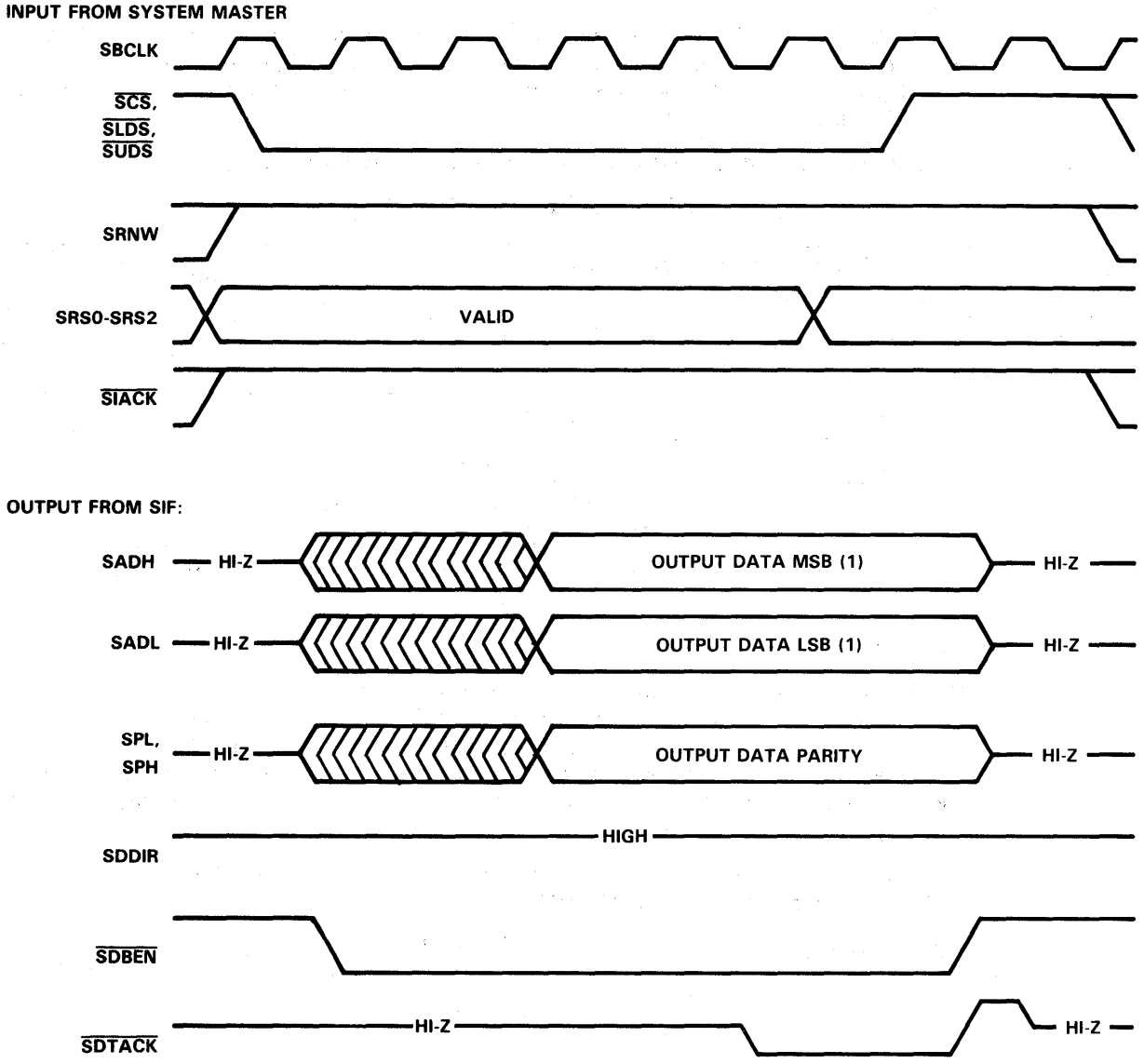


FIGURE 4-11. 680XX MODE DIO READ CYCLE TIMING

The timing illustrated in Figure 4-11 is described below:

1. In the quiescent state the system deasserts SCS, SIACK, SUDS, and SLDS. SRNW is undefined. The SIF floats the SAD bus, and drives both SDDIR and SDBEN high. The SIF also floats its SDTACK pin, but because it has an internal pullup resistor (nominal 10K ohms) attached to it, the signal floats high (negated).
2. Starting the DIO cycle, the system (bus master) asserts a register address on the SRS0-SRS2 lines, and drives SRNW high, indicating a read cycle. The SAS signal is an input to the SIF, but is not decoded.
3. The system asserts SCS low, keeping SIACK negated high.
4. The system asserts either one of SUDS or SLDS low for an 8-bit access, or both low for a 16-bit access.

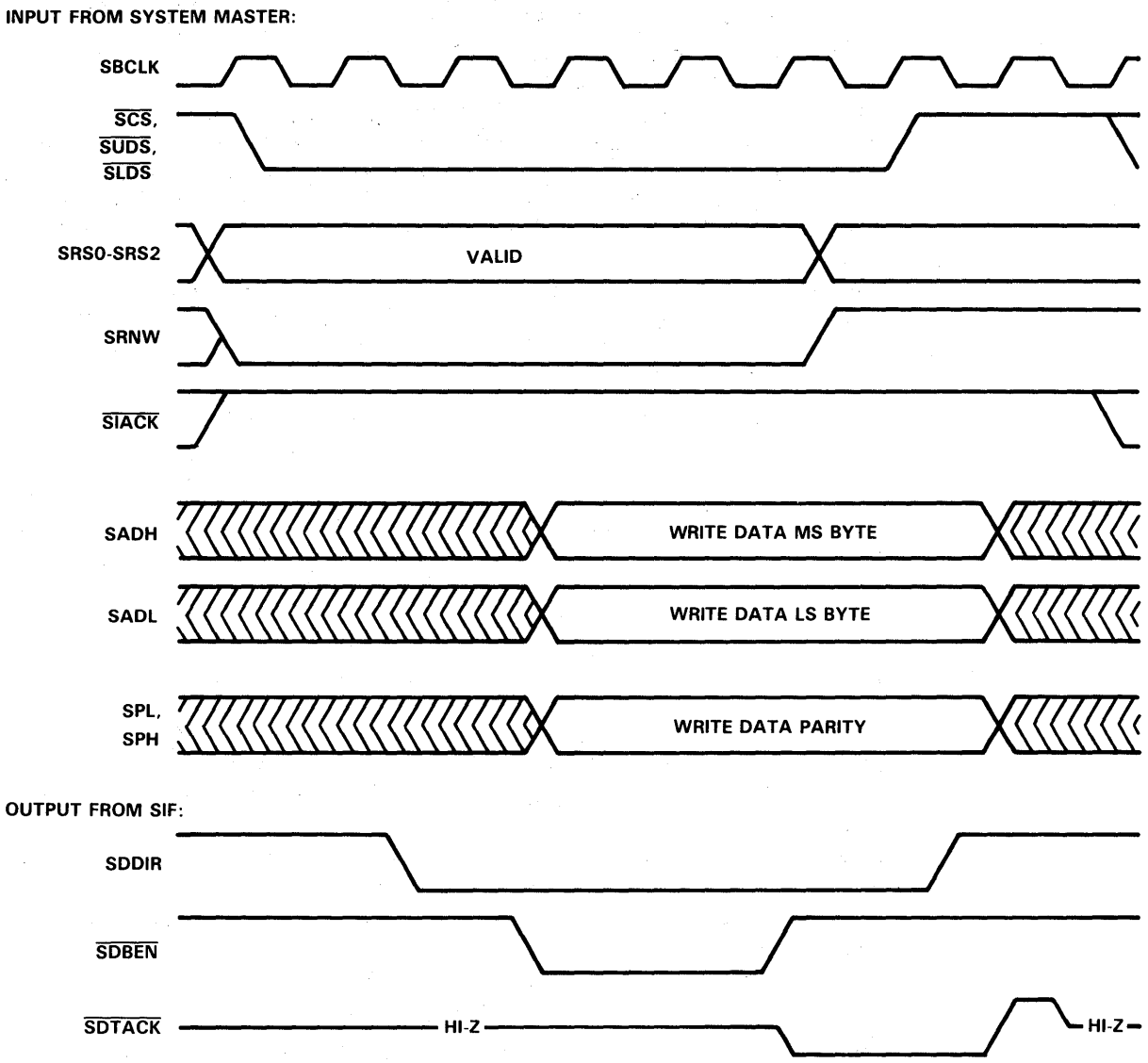


FIGURE 4-12. 680XX MODE DIO WRITE CYCLE TIMING

The timing illustrated in Figure 4-12 is described below:

1. In the quiescent state the system deasserts $\overline{SCS}$, $\overline{SIACK}$, $\overline{SUDS}$, and $\overline{SLDS}$. $\overline{SRNW}$ is irrelevant. The SIF floats the SAD bus, and drives both SDDIR and $\overline{SDBEN}$ high. The SIF also floats its $\overline{SDTACK}$ pin, but because it has an internal pullup resistor (nominal 10K ohms) attached to it, the signal floats high (negated).
2. Starting the DIO cycle, the system (bus master) asserts a register address on the SRS0-SRS2 lines, and drives SRNW low, indicating a write cycle. The $\overline{SAS}$ pin is an input to the SIF, but it is not decoded.
3. The system asserts $\overline{SCS}$ low, keeping $\overline{SIACK}$ negated high.
4. The system asserts either one of $\overline{SUDS}$ or $\overline{SLDS}$ low for an 8-bit access, or both low for a 16-bit access.

4.3.3 Direct Memory Access Interface

The DMA channel provides a full 24 bits of address with which to access up to 16 megabytes of system memory. The throughput capability of the DMA channel is matched to the host of the attached system and can exceed the throughput of the ring. The DMA channel can be programmed for either burst-mode or cycle-steal mode of operation.

Since only 16 bits of address can be output at any instant on the 16 address/data lines, the 8 most significant address bits must be multiplexed (and latched) separately from the lower 16 bits of address. The high order eight bits are called the 'extended' address bits of the DMA address. Two separate address latch enable signals are provided by the Adapter for demultiplexing of the address. For systems requiring only 16 bits of address, no external latch need be provided for the eight address extension bits, although they will still continue to be output by the Adapter.

The Adapter will perform an extra clock cycle (SBCLK) at the beginning of the DMA transfer to output the higher order 8 address bits. Thereafter, an extra cycle will be inserted only when the upper sixteen address bits are changed due to a carry propagated from the lower eight bits.

A parity bit is maintained for each byte of both address and data types on the address data bus. During DMA read cycles, the parity presented by the attached system is checked by the Adapter. During DMA write cycles, the generated parity bits will be output with the address/data. Parity checking may be disabled at Adapter initialization.

4.3.3.1 Burst/Cycle-Steal DMA Modes

Two modes of bus arbitration may be selected by the attached system: burst mode or cycle-steal mode. The method by which the attached system selects the DMA mode is explained in Section 4.4.

Burst Mode

During a burst-mode block DMA transfer, the SIF (System Interface) arbitrates for and obtains control of the attached system's memory bus and then retains the bus until one of the following conditions occurs: (1)the block transfer is completed, (2) a bus error ($\overline{\text{SBERR}}$) or a parity error is detected and parity error checking is enabled, or (3) the bus-release line from the attached system ($\overline{\text{SBRLS}}$) is asserted. During the time that the continuous transfer is in progress, successive word or byte transfers will occur 'back to back', i.e., with no idle SBCLK cycles between bus transfers. An exception will be the occasional SBCLK period (referred to as a TX cycle) used to update the extended-address latch, which occurs when the increment of the 24-bit DMA address counter causes a carry to ripple into its 16 MSBs.

Even if the SIF is unable to maintain the back-to-back DMA transfer rate, it will not release the bus temporarily to allow other devices to use the bus.

While the SIF is performing a burst-mode DMA block transfer, an external device can cause the SIF to release the system bus momentarily, with the DMA transfers resuming normally after the external device relinquishes the bus. An external device requests that the SIF release the bus by asserting an active-low signal to the SIF's $\overline{\text{SBRLS}}$ (bus release) input. The attached system should hold $\overline{\text{SBRLS}}$ active low until the SIF indicates the system bus has been released by deasserting $\overline{\text{SOWN}}$ high.

When the $\overline{\text{SBRLS}}$ input to the SIF is asserted and the SIF has deasserted $\overline{\text{SOWN}}$, the SIF will immediately re-request the bus to complete the interrupted DMA transfer. If the $\overline{\text{SBRLS}}$ input remains asserted (low) and the bus is subsequently granted to the SIF, the SIF will perform a single DMA cycle followed by re-releasing the bus by deasserting $\overline{\text{SOWN}}$ high. Thus, the $\overline{\text{SBRLS}}$ input during burst mode DMA serves as a 'mode select' driving the interface into cycle-steal mode during the time $\overline{\text{SBRLS}}$ is asserted low.

To provide a uniform way of referring to the two bytes in each word, the byte on the left is designated the "high" byte, and the byte on the right is designated the "low" byte. The impact of these conventions on the ordering of data bytes in memory is illustrated in Figure 4-14. Storing the string "ABCD" is shown for both the 680XX and 808X.

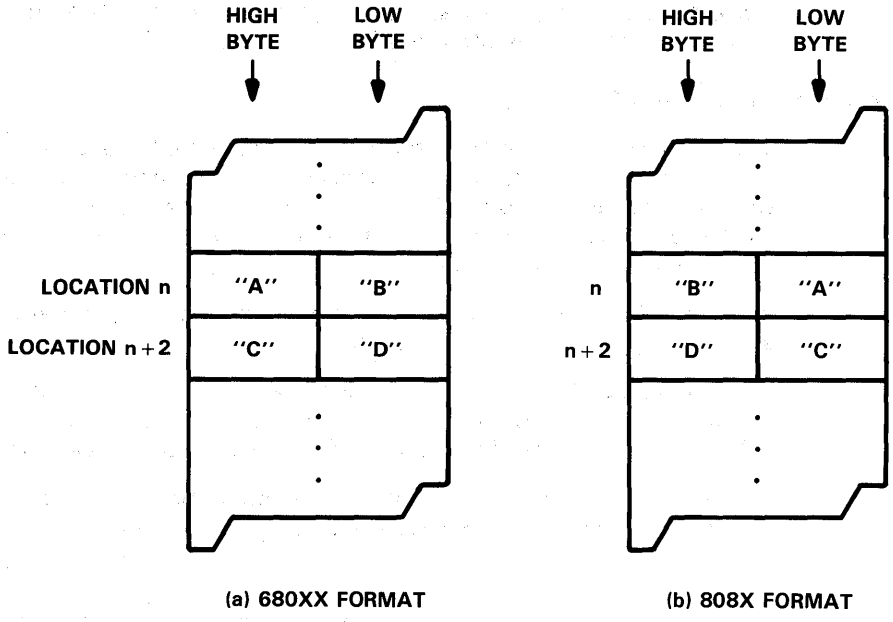


FIGURE 4-14. FORMATS FOR STORING CHARACTER STRING "ABCD" IN MEMORY

In 808X 8-bit mode, each DMA word transferred from the SIF to the user system is transmitted as a series of two bytes over the SADL0-SADL7 pins. DMA bytes are transferred in increasing byte address order on the system.

In 16-bit mode, each DMA word will be transferred as a 16-bit word if the data is aligned in attached system memory as it is in Adapter memory. Otherwise, 8-bit transfers are performed on the system bus. All DMA operations are performed to an even address in Adapter memory. DMA may be performed to an even or odd address in system memory. An even or an odd number of bytes may be moved.

With four independent binary cases, there are 16 possible cases for system DMA transfer.

1. The attached system host processor may use either 808X or 680XX data organization (selected with the SI/$\overline{M}$ strap pin);
2. The DMA starting address in system memory may be even or odd;
3. The number of bytes to be transferred may be even or odd; and
4. The transfer may be a read (system to Adapter) or write (Adapter to system) operation.

TABLE 4-14.SYSTEM DMA CYCLE DESCRIPTION-808X

HOST	STARTING SYSTEM ADDRESS	NUMBER OF BYTES TO MOVE	READ FROM OR WRITE TO SYSTEM	16-BIT SYSTEM BUS TRANSFER		LAN ADAPTER BUS TRANSFERS	
				SADH 0-7	SADL 0-7	LAD 0-7	LAD 8-15
808X	EVEN	EVEN	READ	B	A	A	B
				D	C	C	D
			WRITE	B	A	A	B
				D	C	C	D
		ODD	READ	B	A	A	B
				—	C*	C	—
			WRITE	B	A	A	B
				hi-z	C *	C	—
	ODD	EVEN	READ	A *	—		
				—	B *	A	B
				C *	—		
				—	D *	C	D
			WRITE	A *	hi-z	A	B
				hi-z	B *		
				C *	hi-z	C	D
				hi-z	D *		
		ODD	READ	A *	—		
				—	B *	A	B
				C *	—	C	—
			WRITE	A *	hi-z	A	B
				hi-z	B *		
				C *	hi-z	C	—

4.3.3.3 System DMA Address Latching

Figure 4-15 shows how the latches, used to capture address information from the SADL0-SADL7 and SADH0-SADH7 pins, are connected to the SIF.

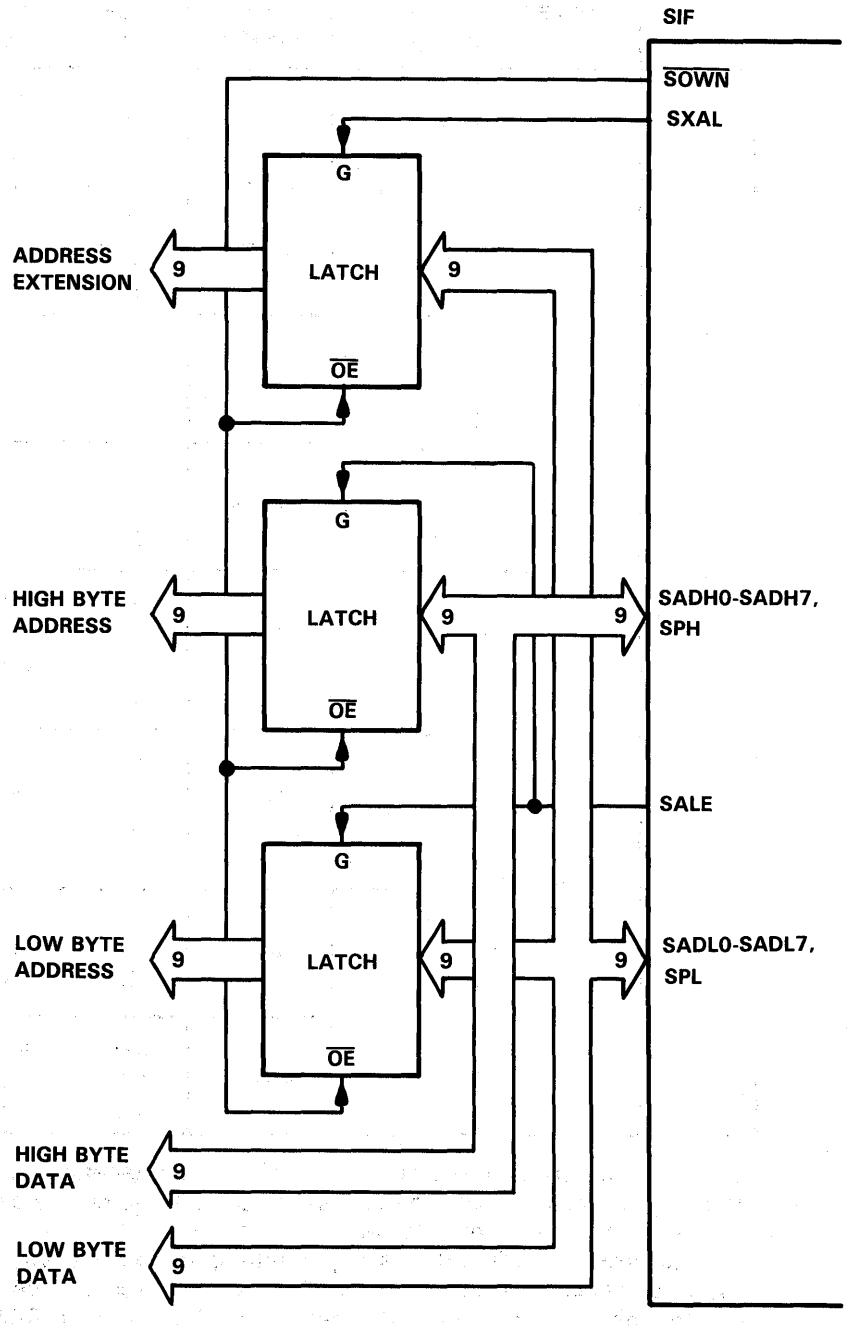


FIGURE 4-15. EXTERNAL TTL LATCHES DEMULTIPLEX ADDRESS/DATA BUS

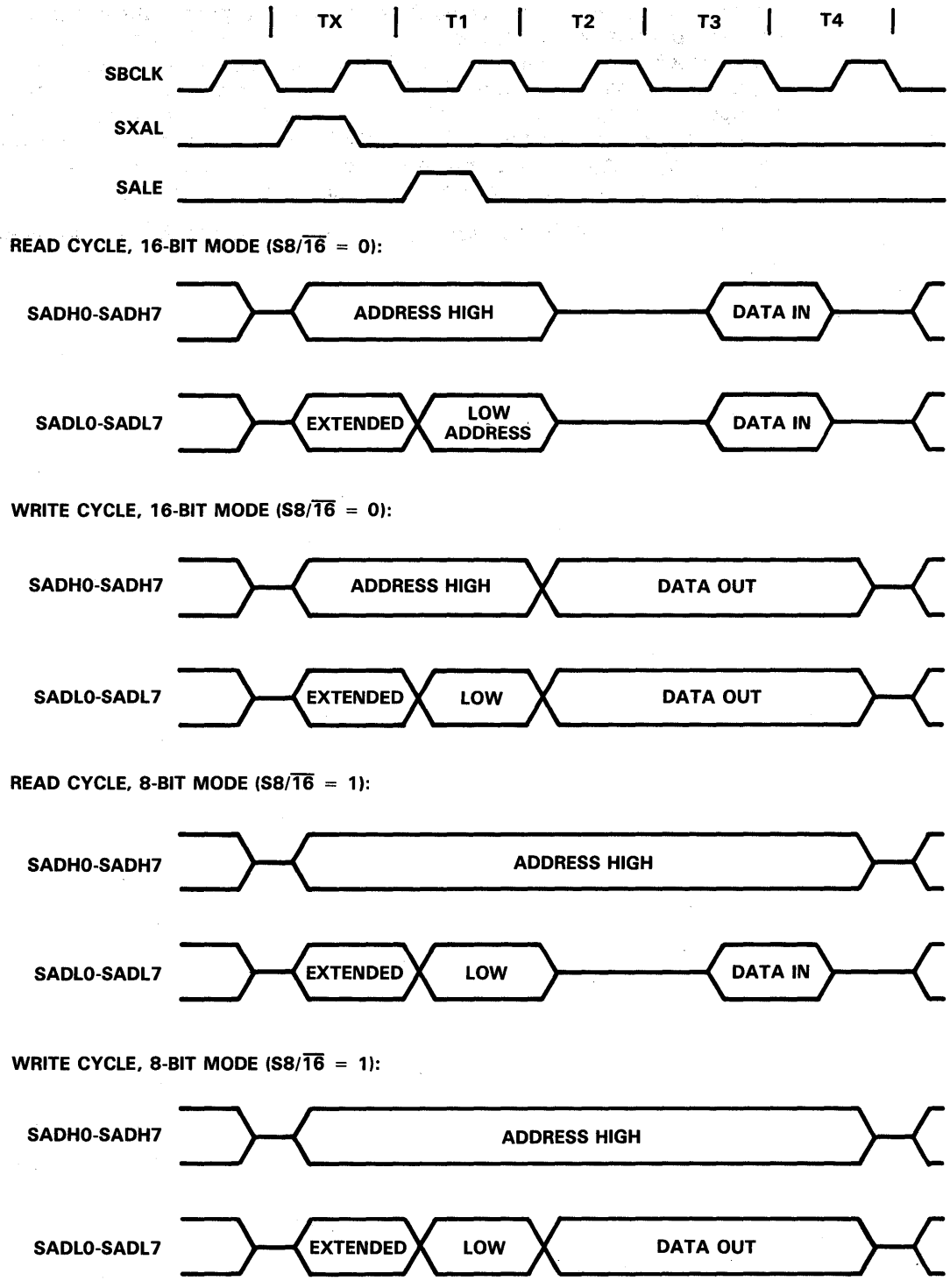


FIGURE 4-16. ADDRESS MULTIPLEXING FOR 8- AND 16-BIT MODES

TABLE 4-16. 808X DMA INTERFACE PIN FUNCTIONS

PIN	FUNCTION
$\overline{\text{SBHE}}$	SYSTEM BYTE HIGH ENABLE. This three-state output serves as an active-low byte-high-enable signal. This pin is an input during DIO operations.
$\overline{\text{SWR}}$	SYSTEM WRITE STROBE. This output is an active-low write strobe for DMA write operations. This pin is an input during DIO operations.
$\overline{\text{SRD}}$	SYSTEM READ STROBE. This output is an active-low read strobe for DMA read operations. This pin is an input during DIO operations.
$\overline{\text{SRDY}}$	SYSTEM BUS READY. This input serves as an active-low data transfer acknowledge signal which indicates to the DMA channel the completion of the bus cycle. During DIO operations, this pin is an output.
SALE	SYSTEM ADDRESS LATCH ENABLE. At the start of each DMA cycle, this output provides the enable pulse used to externally latch the sixteen LSBs of the address from the multiplexed address/data lines. Systems which implement parity on addresses also can use SALE to externally latch the parity bits (on SPH and SPL) for the sixteen LSBs of the DMA address.
SXAL	SYSTEM EXTENDED ADDRESS LATCH. This output provides the enable pulse used during DMA cycles, to externally latch the eight high-order address bits of the 24-bit system address. SXAL is activated prior to the first cycle of each block DMA transfer, and thereafter as necessary (whenever an increment of the DMA address counter causes a carry-out of the lower 8-bits). During cycle steal mode, SXAL is activated prior to each DMA transfer. Systems which implement parity on addresses also can use SXAL to externally latch the parity bit (available on SPL) for the DMA address extension byte.
SDDIR	SYSTEM DATA DIRECTION. This output provides a signal to the external data buffers, indicating the direction in which the data is moving. During DMA reads, SDDIR is low indicating input mode. During DMA writes, SDDIR is high indicating output mode.
$\overline{\text{SDBEN}}$	SYSTEM DATA BUS ENABLE. This output provides the active-low enable signal to external data bus buffers that causes them to leave the high-impedance state and begin transmiting data.
$\overline{\text{SOWN}}$	SYSTEM BUS OWNED. This output goes active-low during DMA cycles to indicate to external devices that the Adapter has control of the system bus. $\overline{\text{SOWN}}$ drives the enable signal of the bus transceiver chips which drive the address and bus control signals.
SBCLK	SYSTEM BUS CLOCK. This is the external clock signal to which the Adapter synchronizes its bus timing for both direct I/O and DMA transfers. For asynchronous buses, any oscillator signal may be applied.
SHRQ	SYSTEM HOLD REQUEST. This active-high output is used to request control of the system bus in preparation for a DMA transfer.

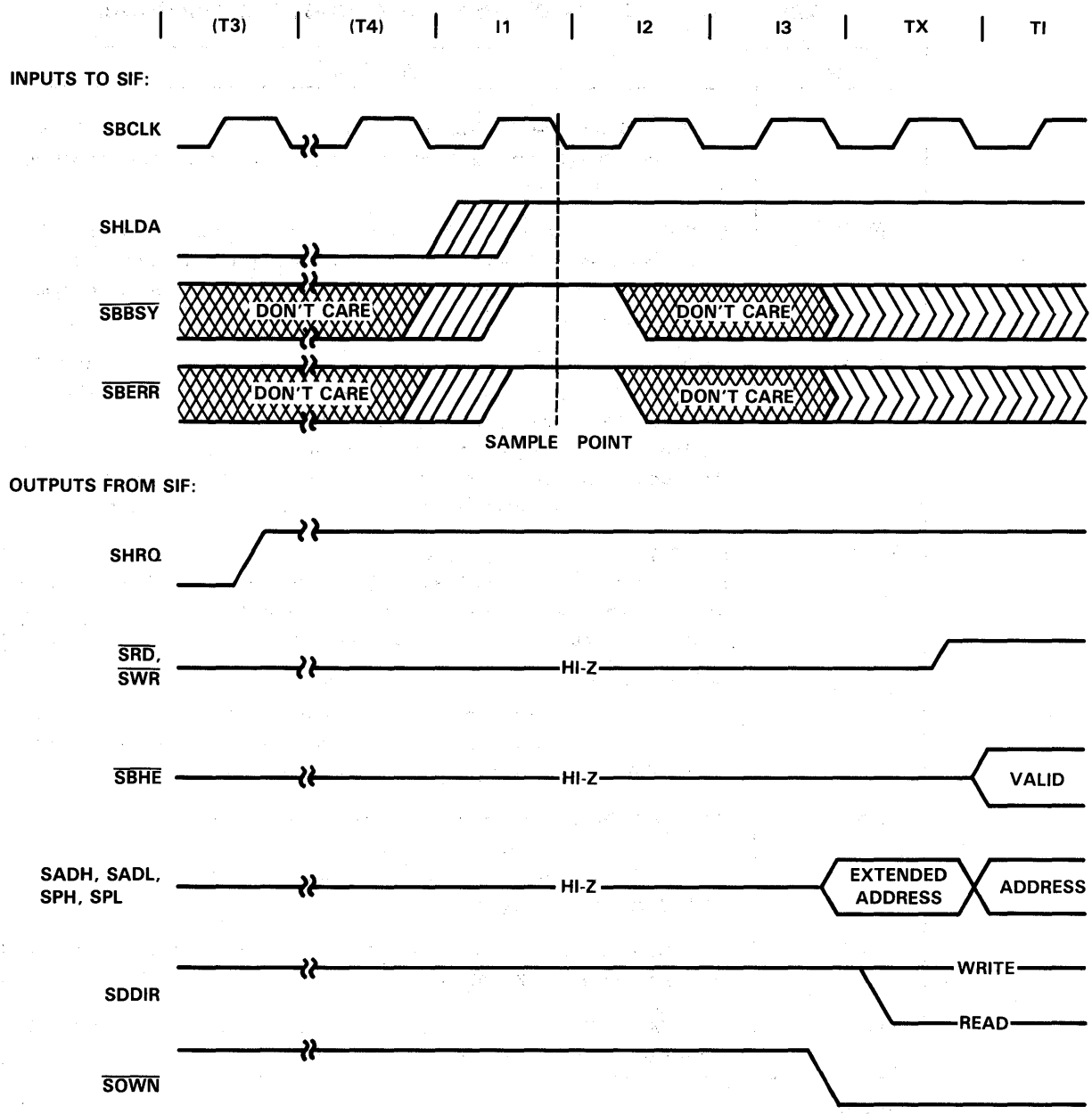


FIGURE 4-18. ADAPTER ACQUIRES SYSTEM BUS — 808X MODE

In Figure 4-18, the SIF arbitrates for and obtains control of the system bus in preparation for one or more DMA cycles. The sequence of operations is described below:

1. The SIF asserts SHRQ high on the rising edge of SBCLK.
2. When the system bus master completes its operation, it will assert SHLDA high.
3. The SIF samples several lines at the falling edge of SBCLK: its own SHRQ, and the asynchronous inputs SHLDA, $\overline{\text{SBBSY}}$ and $\overline{\text{SBERR}}$. If SHRQ, SHLDA, $\overline{\text{SBBSY}}$ and $\overline{\text{SBERR}}$ are all high at a sample time, the SIF will assert $\overline{\text{SOWN}}$ low on the second rising edge of SBCLK following the sample (I3 low).
4. The subsequent falling edge of SBCLK starts state TX of the first DMA cycle. The SIF drives the most significant 8 bits of the 24-bit DMA address on the SADL bus, and the next most significant eight bits on the SADH bus. Figure 4-18 depicts the address driven out on TX cycles.
5. On the next rising edge of SBCLK (TX high), the SIF drives SDDIR low for a read cycle or leaves it high for a write. It drives the bus controls $\overline{\text{SRD}}$ and $\overline{\text{SWR}}$ high.
6. On the next falling edge (TX low), the SIF drives the low eight bits of address on to the SADL bus and drives $\overline{\text{SBHE}}$ to its value for the transfer. It continues to drive the middle eight bits of address on the SADH bus.
7. On the next rising edge of SBCLK (T1 high), the SIF asserts $\overline{\text{SWR}}$ low for a write cycle.

Note that a minimum of three "idle" SBCLK cycles will occur in the bus handoff, where no data transfers are taking place.

Figure 4-19 demonstrates the timing when the SIF returns control of the system bus to the attached system. The sequence of operations is described below:

1. On the falling edge of SBCLK in state T4 of the last DMA transfer, the SIF does the following:
   a. Floats the bus controls $\overline{\text{SRD}}$ and $\overline{\text{SWR}}$;
   b. Drives $\overline{\text{SBHE}}$ high, and when it is has detected that the pin has reached a high level, tristates the signal;
   c. Tristates the SAD bus; and
   d. Drives SDDIR back high (if previously driven low for a read cycle).
2. On the next rising edge of SBCLK (I1 high), the SIF deasserts SHRQ by driving it low.
3. On the subsequent rising edge (I2 high), the SIF deasserts $\overline{\text{SOWN}}$ by driving it high.
4. Sometime after detecting that SHRQ is negated, the system deasserts SHLDA.
5. The SIF will not request the bus again until SHLDA is negated.

At least three "idle" SBCLK cycles will occur in this bus handoff.

At the start of the DMA read cycle shown in Figure 4-20, the SALE output strobes the contents of address/data lines SADH0-SADH7 and SADL0-SADL7 into an external latch (for example, 74LS373). 808X processors multiplex address and data in the same manner. Using the SIF's SALE output, the address/data bus can be demultiplexed with external latches to present to the system bus a non-multiplexed interface with separate address and data buses. Assuming that a transparent latch is used to capture the address from SADH0-SADH7 and SADL0-SADL7, the demultiplexed address presented to the system will have become valid prior to the falling edge of SALE. This is provided in order to support memories with as long an access time (from address valid) as possible.

In 808X mode, both byte and word DMA cycles are supported. The least-significant address bit, SADL7, is the equivalent of the 808X microprocessor's A0 address bit, used to select the low byte; the $\overline{\text{SBHE}}$ output is the equivalent of a 16-bit 808X processor's $\overline{\text{BHE}}$ signal. On single byte transfers (either reads or writes) the unused half of the SAD lines is placed in hi-z. In 8-bit 808X mode, data is transferred only over SADL0-SADL7 and the $\overline{\text{SBHE}}$ signal is kept high.

After the address has been latched, the SIF forces its address/data lines, SADH0-SADH7 and SADL0-SADL7, to high impedance, and also drives $\overline{\text{SRD}}$ active-low to enable the read data from the slave device onto the address/data lines. The read data is strobed into the SIF on the falling edge of the clock cycle marked "T3" in Figure 4-20, and $\overline{\text{SRD}}$ goes high to cause the slave device to remove its data from the bus.

808X DMA Write Cycles

The general timing sequence for a DMA write operation is shown in Figure 4-21.

At the start of the DMA write cycle shown in Figure 4-21, the SALE output strobes the contents of address/data lines SADH0-SADH7 and SADL0-SADL7 into an external latch (e.g., 74LS373). 808X processors multiplex address and data in the same manner. Using the SIF's SALE output, the address/data bus can be demultiplexed with external latches to present to the system bus a non-multiplexed interface with separate address and data buses. Assuming that a transparent latch is used to capture the address from SADH0-SADH7 and SADL0-SADL7, the demultiplexed address presented to the system will have become valid prior to the falling edge of SALE. This is provided in order to support memories with as long an access time (from address valid) as possible.

In 808X 16-bit mode, both byte and word DMA cycles are supported. The least-significant address bit, SADL7, is the equivalent of the 808X microprocessor's A0 address bit, used to select the low byte. The $\overline{\text{SBHE}}$ output is the equivalent of a 16-bit 808X $\overline{\text{BHE}}$ signal. On single byte transfers (either reads or writes) the unused half of the SAD lines is placed in hi-z. In 808X 8-bit mode, data is transferred only over SADL0-SADL7, and the $\overline{\text{SBHE}}$ signal is kept high.

After the address has been latched, the SIF drives the write data onto the address/data lines and also drives $\overline{\text{SWR}}$ active-low to indicate to slave devices that write data is available on the address/data lines. The $\overline{\text{SWR}}$ strobe shown in the figure is roughly two SBCLK periods in duration. The rising edge of $\overline{\text{SWR}}$ should be used by slave devices to latch the data from the address/data lines.

Slave devices which require longer access times should drive $\overline{\text{SRDY}}$ high prior to the falling clock edge at the end of "T2" in order to generate wait states. As long as $\overline{\text{SRDY}}$ remains high, the SIF will continue to generate wait states (T3 is repeated for each wait state requested by the slave device). When the slave has had sufficient time to complete the access, it drives $\overline{\text{SRDY}}$ low to allow the SIF to complete the DMA cycle.

The $\overline{\text{SDBEN}}$ and SDDIR outputs are provided to allow the SIF to interface easily to a system bus through a set of external data bus transceivers (such as the 74LS245). $\overline{\text{SDBEN}}$ is an active-low data bus enable signal used to turn on the transceivers, and SDDIR indicates the direction in which the data is to be transmitted. SDDIR is driven low to enable read data from the system bus into the SIF, and driven high to enable write data from the SIF onto the system bus.

4.3.3.5 680XX Mode DMA Interface

In 680XX mode, the SIF controls the bus in the same manner as a 680XX-type microprocessor.

Interface Signals

Table 4-17 describes the DMA interface functions of the System Interface (SIF) pins when configured in 680XX mode.

TABLE 4-17. 680XX DMA INTERFACE PIN FUNCTIONS (concluded)

PIN	FUNCTION
$\overline{\text{SOWN}}$	SYSTEM BUS OWNED. This output goes active-low during DMA cycles to indicate to external devices that the Adapter has control of the system bus. $\overline{\text{SOWN}}$ drives the enable signal of the bus transceiver chips, which drive the address and bus control signals.
SBCLK	SYSTEM BUS CLOCK. This is the external clock signal to which the Adapter synchronizes its bus timing for both direct I/O and DMA transfers. For asynchronous buses, any oscillator signal may be applied.
$\overline{\text{SBRQ}}$	SYSTEM BUS REQUEST. This active-low output is used to request control of the system bus in preparation for a DMA transfer.
$\overline{\text{SBRG}}$	SYSTEM BUS GRANT. This active-low input pin indicates that the DMA hold request has been acknowledged and DMA transfers may take place. It is internally synchronized to SBCLK.
$\overline{\text{SBBSY}}$	SYSTEM BUS BUSY. This input is sampled by the Adapter to be inactive-high before the system bus is driven. It is physically tied to the 68000-style Bus Grant Acknowledge ($\overline{\text{BGACK}}$).
SBRLS	SYSTEM BUS RELEASE. If this input is driven low during burst mode DMA transfers, it indicates that a higher-priority device requires control of the system bus and the Adapter should release control as soon as possible. Following bus release, the Adapter will immediately re-request the system bus. This pin effectively drives the interface from burst mode DMA to cycle-steal mode DMA. When cycle-steal mode DMA is being performed or if no DMA is being performed, this input is ignored.
$\overline{\text{SBERR}}$	SYSTEM BUS ERROR. This input is driven active-low during a DMA cycle to indicate to the Adapter that a bus error has occurred and the DMA operation should be abnormally terminated.
SADH0-SADH7	SYSTEM ADDRESS/DATA BUS — HIGH BYTE. This is the most significant byte of the 16-bit address/data bus. It is attached to the host system address/data bits 15-8 (using 680XX-standard bit numbering conventions). The most significant bit is SADH0 and the least significant bit is SADH7.
SADL0-SADL7	SYSTEM ADDRESS/DATA BUS — LOW BYTE. This is the least significant byte of the 16-bit address/data bus. It is attached to the host system address/data bits 7-0 (using 680XX-standard bit numbering conventions). The most significant bit is SADL0 and the least significant bit is SADL7.
SPH	SYSTEM PARITY HIGH. Contains an odd-parity bit for each data or address byte transmitted over SADH0-SADH7.
SPL	SYSTEM PARITY LOW. Contains an odd-parity bit for each data or address byte transmitted over SADL0-SADL7.

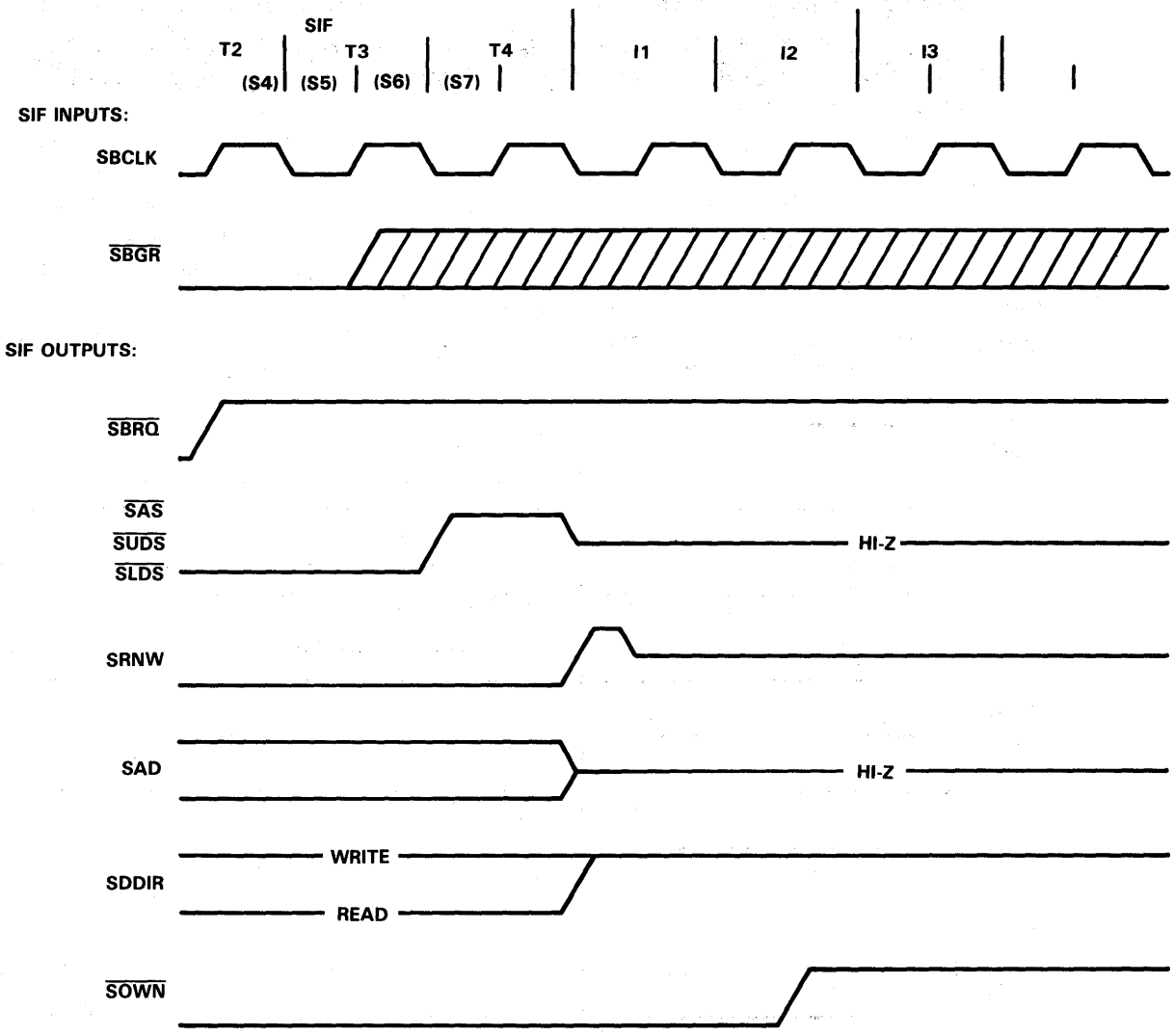


FIGURE 4-23. ADAPTER RETURNS SYSTEM BUS — 680XX MODE

In Figure 4-22, the SIF contends for and obtains control of the system bus in preparation for one or more DMA cycles. Before the SIF requests the bus, it verifies that SBGR is high at the falling edge of SBCLK. On the second rising edge of SBCLK following the SIF's sample of SBGR high, System Bus Request (SBRQ) is driven low by the SIF to request the bus. System Bus Grant (SBGR) is driven low by the processor to indicate its readiness to yield bus control to the SIF. The SIF samples several signals on the falling edge of SBCLK to determine when it may control the bus. Its own SBRQ must be low, SBGR must be low, and the following signals must be high: SBBSY, SBERR, SAS, SUDS, SLDS, and SDTACK. The asynchronous inputs SBBSY, SBGR, SBERR, and SDTACK are sampled on the falling edge of SBCLK. The SIF starts phase TX of its bus cycle on the second falling edge from the sample point at which all inputs are at the appropriate level.

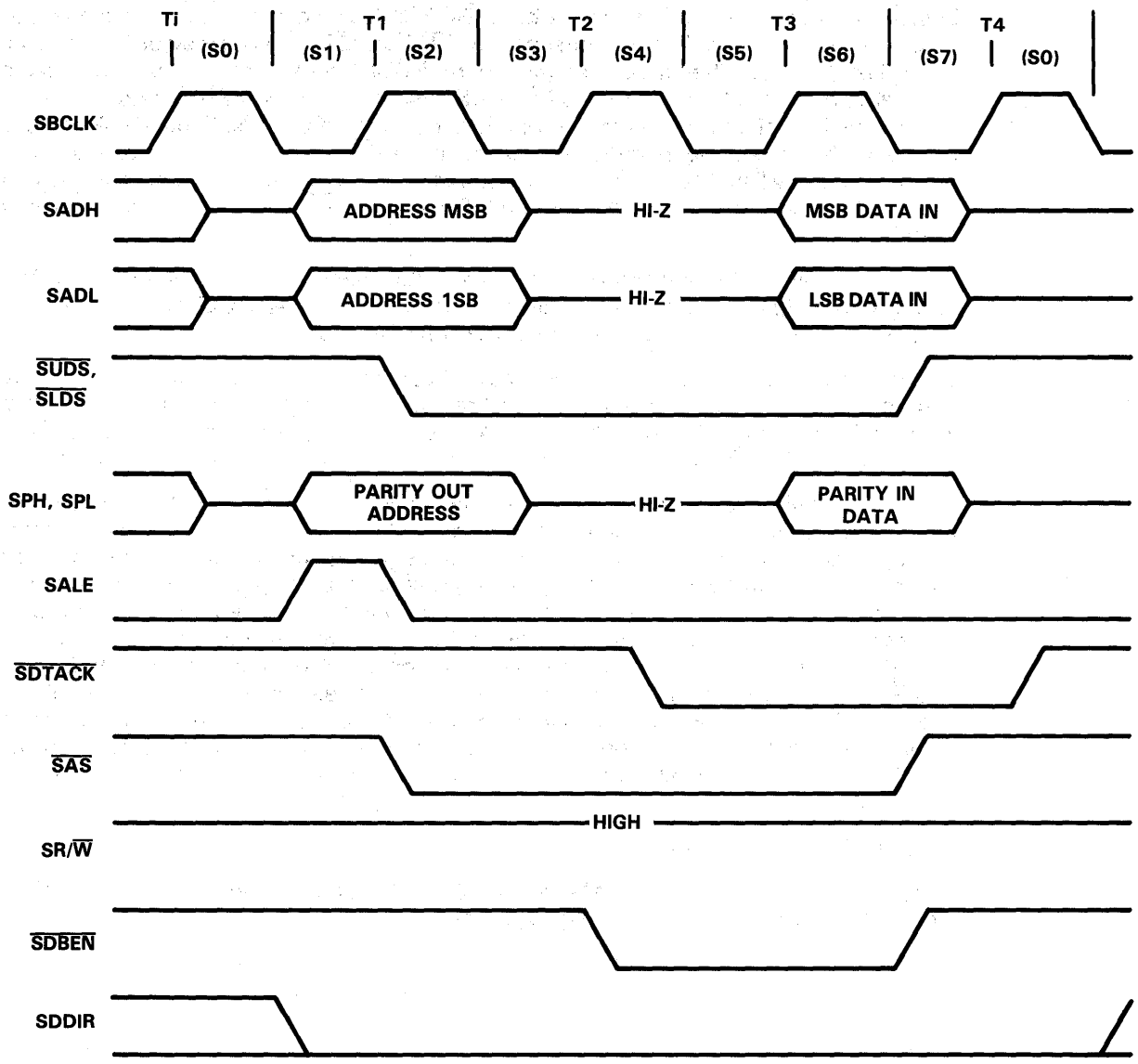


FIGURE 4-24. 680XX MODE DMA READ TIMING

At the start of the DMA read cycle shown in Figure 4-24, output System Address Latch Enable (SALE) strobes the contents of SADH0-SADH7 and SADL0-SADL7 into an external latch (e.g., 74LS373). Unlike the 680XX microprocessor, the SIF multiplexes address and data over the same physical I/O pins. However, the timing of SALE enables the address/data bus to be demultiplexed with external latches to present to the system bus a non-multiplexed interface whose signals and timing are similar to those of the 680XX. Assuming that a transparent latch is used to capture the address from the SAD pins of the SIF, the address at the outputs of the external latch will have become valid prior to the falling edge of $\overline{SAS}$ (System Interface Address Strobe).

At the start of the DMA write cycle shown in Figure 4-25, output System Address Latch Enable (SALE) strobes the contents of SADH0-SADH7 and SADL0-SADL7 into an external latch (e.g., 74LS373). Unlike the 680XX microprocessor, the SIF multiplexes address and data over the same physical I/O pins. However, the timing of SALE is such that the address/data bus can be demultiplexed with external latches to present to the system bus a non-multiplexed interface, whose signals and timing are similar to those of the 680XX. Assuming that a transparent latch is used to capture the address from the address/data pins of the SIF, the address at the outputs of the external latch will have become valid prior to the falling edge of $\overline{SAS}$ (System Interface Address Strobe).

SRNW goes low to indicate that a write operation is taking place. The falling edges of data strobes $\overline{SUDS}$ and $\overline{SLDS}$ occur one full clock after the falling edge of $\overline{SAS}$. SDDIR remains high during the cycle, and $\overline{SDBEN}$ goes low to enable the external data bus transceivers to drive the data output from the SADH0-SADH7 and SADL0-SADL7 pins of the SIF onto the system data bus. In certain cases, only a single byte is transferred when the SIF is in 16-bit mode. In these cases, the unused half of SAD is floated.

4.3.4 Adapter Interrupt Interface

Interrupts are used to communicate the start or end of many Adapter operations and attached system operations. The attached system interrupts the Adapter by writing a one to the MSB of the Interrupt register using the direct I/O interface. During the same write cycle to the Adapter, the attached system indicates the type, or purpose, of the interrupt through other bits in the Interrupt Register. This interrupt control by the attached system software will be discussed in Section 4.4.

Interrupts to the attached system from the Adapter are initiated by assertion of the SINTR/$\overline{SIRQ}$ (interrupt request) pin. To clear the interrupt, the attached system must clear the active state of the SINTR/$\overline{SIRQ}$ pin by writing a zero to bit 8 of the Interrupt Register with a DIO write cycle.

An optional interrupt vector may be obtained from the Adapter by asserting the Interrupt Acknowledge ($\overline{SIACK}$) pin. This causes a special bus operation known as an interrupt acknowledge cycle to occur, allowing the attached system to read the interrupt vector.

4.3.4.1 Interrupt Interface Pin Descriptions

Table 4-18 describes the Adapter pins used in the Adapter attached system interrupt interface.

TABLE 4-18. ADAPTER INTERRUPT PIN DESCRIPTIONS

PIN	DESCRIPTION
SINTR/$\overline{SIRQ}$	SYSTEM INTERRUPT REQUEST. The SIF activates this output to signal an interrupt to the attached system. In 808X mode, this pin is active-high; in 680XX mode it is active-low.
$\overline{SIACK}$	SYSTEM INTERRUPT ACKNOWLEDGE. This input is driven active-low by the attached system to acknowledge the interrupt request from the Adapter. The Adapter's SIF responds to this signal by gating its interrupt vector onto the system bus. System buses not requiring an interrupt cycle may strap $\overline{SIACK}$ high. Note that this does not clear the active level of the SINTR/$\overline{SIRQ}$ pin, as this level must be cleared by writing to the Interrupt register.

negated while Interrupt Acknowledge (SIACK) is asserted. The input signals on SRD/SUDS and SWR/SLDS must remain inactive-high for the duration of the sequence shown in Figure 4-26. The Register Select (SRS0-SRS2) inputs are ignored. The SIF does not check that Interrupt Request (SINTR/SIRQ) is also asserted when responding to an Interrupt Acknowledge (SIACK) pulse.

4.3.4.3 680XX Interrupt Acknowledge Sequence

The timing for the 680XX-mode interrupt acknowledge cycle is shown in Figure 4-27. The timing is virtually identical to a 680XX read cycle. Only the chip select differs; the Interrupt Acknowledge (SIACK) is used instead of Chip Select (SCS). The signal presented to the SIACK input of the SIF is decoded from the FC<0-2> and A<1-3> outputs of the 680XX microprocessor. The SIF does not check that SINTR/SIRQ is asserted when responding to an SIACK pulse.

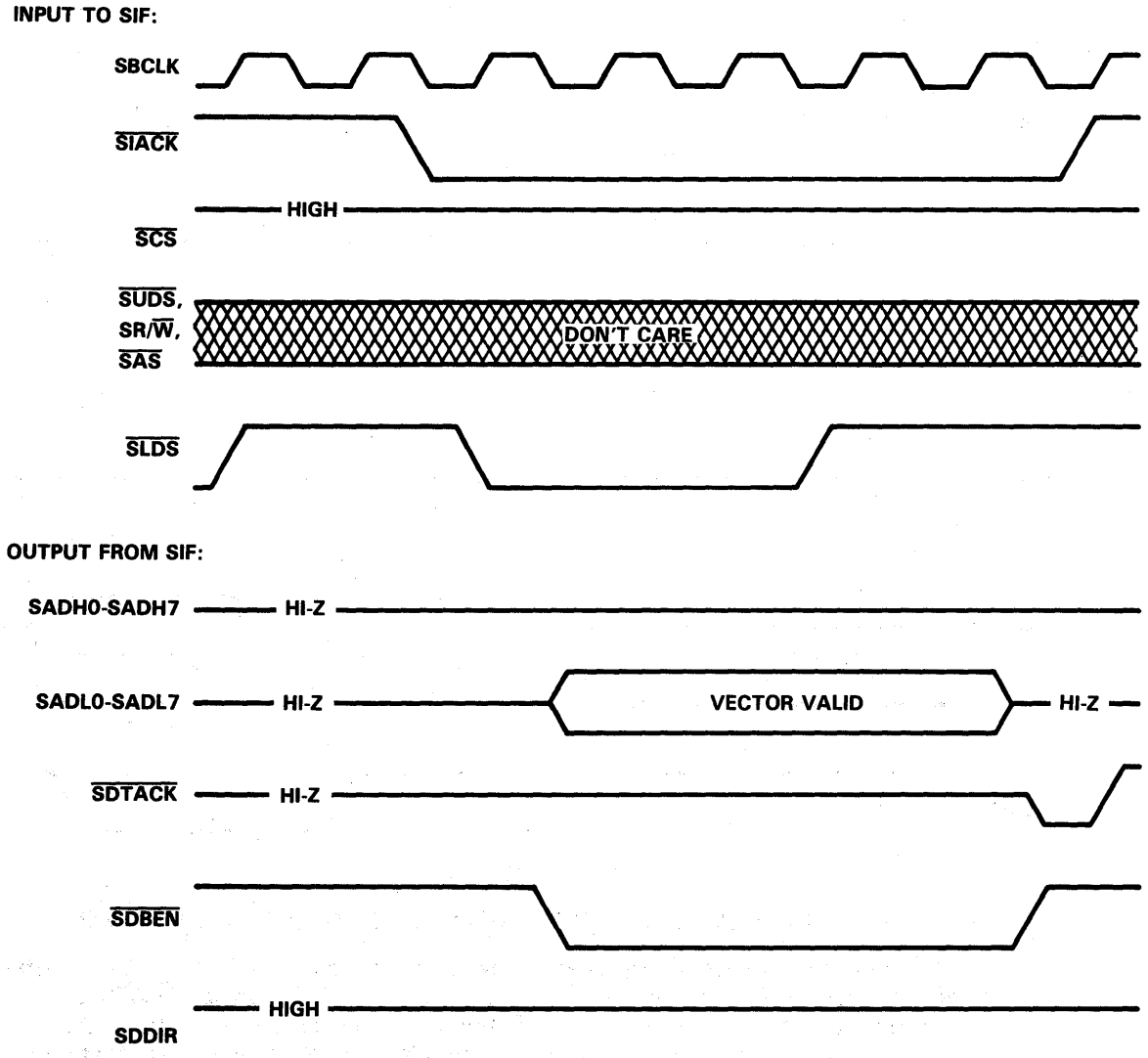


FIGURE 4-27. INTERRUPT ACKNOWLEDGE TIMING FOR 680XX MODE

RECEIVE LIST	The RECEIVE command requires that Receive List(s) be allocated within system memory. The memory allocation size is dependent upon the size and number of lists used in the application. The size of a receive list may be selected upon Adapter initialization to be either 14, 20, or 26 bytes in length. The number of lists is application dependent. A discussion on Receive Lists will be provided in Section 4.4.7.4.
TRANSMIT LIST	The TRANSMIT command requires that Transmit List(s) be allocated within system memory. The memory allocation size is dependent upon the size and number of lists used in the application. The size of a Transmit List may be selected upon Adapter initialization to be either 14, 20, or 26 bytes in length. The number of lists is application dependent.
PRODUCT ID	The OPEN command requires a pointer to an 18 byte Product ID as part of the open parameter list. The system software designer should reserve 18 bytes of system memory for this function. After the OPEN command completes, this memory may be released for other uses. Additional information on Product IDs may be found in the IBM Token-Ring Architecture Reference.

4.4.2 Register Descriptions

The registers within the System Interface (SIF) consist of four address locations as described in the hardware interface description. This section will describe in detail the functions performed by these registers.

4.4.2.1 Interrupt Register

The Interrupt Register is used to post interrupts to the Adapter as well as to read interrupt status information from the Adapter. It is important to note that bits 0-7 can be set to one but not reset to zero by the attached system. These bits, when set to one by the attached system, can only be cleared by the Communications Processor. Likewise, bit 8 can be reset to zero by the attached system but can only be set by the Communications Processor. Bits 9-15 can be read only by the attached system. These bits are set or reset by the Communications Processor.

TABLE 4-19. INTERRUPT REGISTER WRITE BIT FUNCTIONS

BIT	FUNCTION
BIT 0	INTERRUPT ADAPTER. Bit 0, when set to one, will cause an internal Adapter interrupt. This bit when set to zero has no effect. This bit will be cleared by the Adapter after the Adapter responds to the interrupt. The purpose of the interrupt is defined by the SSB CLEAR, EXECUTE, SCB REQUEST, RECEIVE CONTINUE, RECEIVE VALID, and TRANSMIT VALID bits described below. Note that bit 0 must be set for the Adapter to recognize bits 1 through 7.
BIT 1	ADAPTER RESET. Setting bit 1 to one forces an Adapter reset if bit 0 and bits 2-7 are also set to one. Following an Adapter Reset, the initialization procedure outlined in Section 4.4.5 should be followed. This reset function is a software command and certain conditions of hardware failure may prevent its execution.
BIT 2	SSB CLEAR. This interrupt request is used by the system to notify the Adapter that the System Status Block (SSB) is available for the Adapter to post additional status information. The SSB CLEAR bit should be set whenever an Adapter command is executed (Bit 3-Execute is set) to insure that command status will be seen in the System Status Block (SSB).
BIT 3	EXECUTE. This interrupt is used to initiate an Adapter command contained in the System Command Block (SCB). This block will be DMA read and executed by the Adapter.
BIT 4	SCB REQUEST. This interrupt is used to cause the Adapter to interrupt the attached system when the SCB is available for another command. The Adapter will return the SCB CLEAR interrupt code.
BIT 5	RECEIVE CONTINUE. This interrupt request signals the Adapter that buffers have been added to the Receive List Chain in the attached system's memory.
BIT 6	RECEIVE VALID. This interrupt request signals the Adapter that the condition causing List Processing suspension during receive has been cleared.
BIT 7	TRANSMIT VALID. This interrupt request signals the Adapter that the condition causing List Processing suspension during transmit has been cleared.
BIT 8	RESET SYSTEM INTERRUPT. Writing a zero to bit 8 will reset the Adapter-to-attached system interrupt (i.e. clearing the SINTR line). Writing a one to this bit has no effect. SSB CLEAR and INTERRUPT ADAPTER should always be set when this bit position is cleared.
BITS 9-15	RESERVED. These bits are ignored.

Reading from the Interrupt Register

A Direct I/O (DIO) read of the Interrupt Register will transfer a 16-bit word, which is used to examine status of the Adapter.

Figure 4-29 shows the bit assignments of the Interrupt Register when read by the attached system. Table 4-20 defines the functions of each bit.

TABLE 4-20. INTERRUPT REGISTER READ BIT FUNCTIONS (concluded)

BIT	FUNCTION
BIT 10	TEST. Bit 10 is set to one by the bring-up diagnostics following an Adapter reset. This bit is cleared when INITIALIZE (bit 9) is initially set.
BIT 11	ERROR. Bit 11 is set if the bring-up diagnostics detect an error or if there is an error during the initialization process. The error condition is specified in bits 12 through 15.
BITS 12-15	INTERRUPT CODE 0-2/ERROR CODE 0-3. Bits 12-14 define the Adapter-to-attached system interrupt reason code. The lower numerically the code value, the higher the interrupt priority. The 3-bit interrupt code is shown below: 000 ADAPTER CHECK. This interrupt code is used when the Adapter has encountered an unrecoverable hardware or software error. 010 RING STATUS. This interrupt code will be used if the SSB is updated with Ring Status. 011 SCB CLEAR. This interrupt code will be used following a SCB REQUEST interrupt when the SCB is clear. 100 COMMAND STATUS. This interrupt code will be used when the SSB is updated with command status for commands other than TRANSMIT and RECEIVE. This includes COMMAND REJECT STATUS. 101 RECEIVE STATUS. This interrupt code will be used if the SSB is updated with RECEIVE COMMAND STATUS. 110 TRANSMIT STATUS. This interrupt code will be used if the SSB is updated with TRANSMIT COMMANDS STATUS. Bits 12-15 are also used to indicate the error code resulting from the execution of bring-up diagnostics or the initialization process. These codes will be defined in the sections that discuss these operations.

4.4.2.2 Address Register

The Address register contains the address pointer for internal Adapter RAM accesses via the Data or Data/Auto-increment registers. All 16 bits can be read, although only bits 5-14 can be actually set/reset by the attached system. This allows the attached system to access a 2K byte block of the Adapter's internal RAM. The actual starting location of RAM which is read is a function of how the Adapter sets bits

4.4.4 Bring-up Diagnostics Verification

Before the Adapter can be initialized for proper operation, the attached system must verify that the bring-up diagnostics terminated normally. To do this the following procedure should be followed:

1. After either application of the $\overline{\text{SRESET}}$ signal, or writing a software reset (>FF00) to the Interrupt Register, the attached system should read the Interrupt Register until one of the following conditions has occurred:
   a. If the INITIALIZE bit is set to one, and the TEST bit is zero, and the ERROR bit is zero, then the INTERRUPT CODE bits (12-15) should also be zero. This indicates that the bring-up diagnostics completed successfully and the Adapter may now be initialized.
   b. If the TEST and the ERROR bits are set to one, the diagnostics have detected an unrecoverable hardware error. The bring-up error code may be read from bits 12-15. Table 4-21 lists the definitions of these error codes.
   c. If neither of the above conditions occur within three seconds of reset, there is a hardware error preventing completion of the diagnostic routines. It is recommended that the attached system reset and re-try this procedure three times. If still unsuccessful, an unrecoverable hardware error has occurred and the Adapter should be checked.

TABLE 4-21. BRING-UP DIAGNOSTIC ERROR CODES

ERROR CODE				ERROR CONDITION
12	13	14	15	
0	0	0	0	Initial Test Error
0	0	0	1	Adapter ROM CRC Error
0	0	1	0	Adapter RAM Error
0	0	1	1	Instruction Test Error
0	1	0	0	Context/Interrupt Test Error
0	1	0	1	Protocol Handler Hardware Error
0	1	1	0	System Interface Register Error

Following verification of the bring-up diagnostics, the attached system software may now continue with Adapter initialization.

4.4.5 Adapter Initialization

After verification that the Adapter's bring-up diagnostics completed normally, the system software must initialize the Adapter. This initialization involves the transfer of parameters to the Adapter using the DIO interface. These parameters specify:

- The address in the system memory of the System Command Block (SCB) and System Status Block (SSB).
- Interrupt control parameters.

Before the completion of the initialization process, the Adapter initiates a test of the DMA interface. These tests include:

- DMA writes to both the System Command Block and System Status Block.
- DMA reads from both the System Command Block and System Status Block to compare to expected results.

These DMA tests do not require any attached system software to execute, however, in the event these tests fail, the Adapter will return an error in the Interrupt Register.

The function of each of these bits is described in Table 4-22:

TABLE 4-22. INITIALIZATION OPTIONS FIELD BIT FUNCTIONS

BIT	FUNCTION
BIT 0	RESERVED. This bit must be set to one.
BITS 1-2	PARITY ENABLE. These bits should be set to one if the system bus provides odd parity on its data. If parity checking is not desired, these bits should be set to zero. If enabled, parity checking is performed on both DIO and DMA transfers between the Adapter and attached system.
BIT 3	BURST SCB/SSB. If this bit is set to one, the Adapter will transfer the SCB from the system and the SSB to the system in DMA burst mode. The burst size will be six bytes for the SCB read, two bytes for SCB clear, and eight bytes for SSB write. If this bit is set to zero, then these transfers will occur in cycle steal mode.
BIT 4	BURST LIST. If this bit is set to one, the Adapter will transfer transmit and receive lists from the system in DMA Burst Mode. The burst size will be a maximum of 26 bytes. If this bit is set to zero then cycle steal mode is selected.
BIT 5	BURST LIST STATUS. If this bit is set to one, the Adapter will transfer list status data to the system in DMA Burst Mode. The burst size will be two bytes. If this bit is set to zero, cycle steal mode will be selected.
BIT 6	BURST RECEIVE DATA. If this bit is set to one, the Adapter will transfer receive data to the system in DMA burst mode. The burst size is specified in the RECEIVE BURST SIZE field of the Initialization Block. If this bit is set to zero, cycle steal mode is selected.
BIT 7	BURST TRANSMIT DATA. If this bit is set to one, the Adapter will transfer transmit data from the system in DMA burst mode. The burst size is specified in the TRANSMIT BURST SIZE field of the Initialization Block. If this bit is set to zero, cycle steal mode is selected.
BITS 8-15	RESERVED. These bits must be set to zero.

Command Status Vector

This byte contains the interrupt vector that the Adapter places on the attached system bus when the SSB is updated with command status for commands other than transmit or receive. COMMAND REJECT STATUS will also use this vector.

Transmit Command Status Vector

This byte contains the interrupt vector that the Adapter places on the attached system bus when the SSB is updated with TRANSMIT COMMAND STATUS.

Receive Command Status Vector

This byte contains the interrupt vector that the Adapter places on the attached system bus when the SSB is updated with RECEIVE COMMAND STATUS.

Ring Status Vector

This byte contains the interrupt vector that the Adapter places on the attached system bus when the SSB is updated with RING STATUS.

5. Continue to read the Interrupt Register until one of the following occurs:
   a. The INITIALIZE, TEST, and ERROR bits are all zero. This condition indicates that initialization is complete without error. The SCB should contain >0000C1E2D48B and the SSB should contain >FFFFD1D7C5D9C3D4.
   b. If the ERROR bit is set, the initialization process has failed. The Interrupt Code bits 12-15 will contain the initialization error code. (These error codes are listed in Table 4-23.) The initialization procedure must be restarted from Adapter reset.
   c. If neither of the above conditions occurs within 10 seconds of loading the Parameter Initialization Block, there is a hardware error. It is recommended that the attached system reset the Adapter and re-try the initialization procedure three times. If still unsuccessful, there is an unrecoverable hardware error.

TABLE 4-23. ADAPTER INITIALIZATION ERRORS

ERROR CODE 12	13	14	15	ERROR CONDITION
0	0	0	1	Invalid Initialization Block. Twenty-two (22) bytes were not passed.
0	0	1	0	Invalid Options. This code is returned if the PARITY ENABLE Bits are not equal or the Reserved bits are not zero.
0	0	1	1	Invalid Receive Burst Count. The Receive Burst count is odd.
0	1	0	0	Invalid Transmit Burst count. The Transmit Burst count is odd.
0	1	0	1	Invalid DMA Abort Threshold. The DMA abort thresholds were specified as zero.
0	1	1	0	Invalid SCB. The SCB address was specified as odd.
0	1	1	1	Invalid SSB. The SSB address was specified as odd.
1	0	0	0	DIO Parity. A parity error occured during a DIO write operation.
1	0	0	1	DMA Timeout. The Adapter timed out (10 seconds) waiting for a test DMA transfer to complete.
1	0	1	0	DMA Parity Error. A parity error occurred during the DMA tests and the operation was tried unsuccessfully the number of times specified by the DMA Abort Threshold.
1	0	1	1	DMA Bus Error. The DMA test encountered a bus error and the operation was tried unsuccessfully the number of times specified by the DMA Abort Threshold.
1	1	0	0	DMA Data Error. Initialize DMA test failed due to a data compare error.
1	1	0	1	Adapter Check. The Adapter encountered an unrecoverable hardware error.

4.4.6 The Command and Status Block

Two fixed-address control blocks must be provided by the system: the System Command Block (SCB) and the System Status Block (SSB). The starting address of both blocks is passed to the Adapter during the initialization process as described in the previous section. Both blocks must be aligned on a word (even address) boundary.

In general, the attached system issues a command to the Adapter by loading the request in the SCB and interrupting the Adapter. The Adapter will then download the command (and any required parameters) through the System Interface DMA channel. If the SCB REQUEST bit (bit 4) of the Interrupt Register is set, the Adapter will interrupt the attached system after the command has been downloaded, indicating to the attached system that the SCB is available for additional commands.

then the SCB is available for use. If the Command Field is non-zero, an EXECUTE Interrupt request was issued or the SCB was altered in preparation for an EXECUTE Interrupt request subsequent to the SCB REQUEST. If SCB REQUEST is desired, it is recommended that either the SCB REQUEST be issued coincident with an EXECUTE Interrupt Request, or that the SCB alteration and EXECUTE Interrupt Request be performed only in response to SCB CLEAR.

A maximum of three commands may be executed simultaneously within the Adapter. A fourth command will not begin execution until there are less than three commands executing simultaneously. There may not be more than one transmit or receive command executed at one time. Thus the Adapter may be executing a TRANSMIT command, a RECEIVE command, and one other command.

4.4.6.2 Status Reporting: The System Status Block

The System Status Block (SSB) is eight bytes in length. It is the block in which the Adapter returns RING STATUS, COMMAND REJECT STATUS, and status upon completion of Adapter commands. The Adapter will always DMA write the entire eight bytes regardless of the actual length of the returned status. The unspecified status fields should be ignored in this case. The SSB is not used to return status for frame commands. The frame status information can be obtained in the parameter lists associated with RECEIVE and TRANSMIT commands. The SSB format is defined in Figure 4-33.

SSB ADDRESS		
	+ 0	COMMAND
	+ 2	STATUS 0
	+ 4	STATUS 1
	+ 6	STATUS 2

FIGURE 4-33. SYSTEM STATUS BLOCK FORMAT

The Command field is written to the SSB by the Adapter and is used to identify either RING STATUS, COMMAND REJECT STATUS, or the status of a general command. The Status fields contain the actual status information for the Command field.

Following the DMA operation to write the status information to the SSB, the Adapter will interrupt the attached system to indicate that the SSB contains valid status information. The attached system software should reset the Adapter-to-system interrupt and communicate to the Adapter that the SSB is clear and available for additional status posting. This is done by writing a one to the INTERRUPT ADAPTER and SSB CLEAR and a zero to the RESET SYSTEM INTERRUPT bit (bits 2 and 8 respectively) of the Interrupt Register.

RING STATUS Interrupt

The SSB will be loaded with the current ring status and an interrupt posted to the attached system when any of the following error interrupt conditions occur:

1. The Adapter detects a signal loss on the ring.
2. The Adapter is transmitting or receiving beacon frames to/from the ring. This interrupt condition may be disabled by setting bit 1 of the OPEN command options.
3. The Adapter transmits a Report Error MAC Frame. This interrupt error condition may be disabled by setting bit 2 of the OPEN command options.
4. An open or short circuit fault is detected by the Adapter.

TABLE 4-24. RING STATUS FIELD BIT FUNCTIONS

BIT	DESCRIPTION
BIT 0	SIGNAL LOSS. Bit 0, when set to one indicates that the Adapter has detected a loss of signal on the ring.
BIT 1	HARD ERROR. Bit 1, when set to one, indicates that the Adapter is presently transmitting or receiving beacon frames to or from the ring.
BIT 2	SOFT ERROR. Bit 2, when set to one, indicates that the Adapter has transmitted a Report Error MAC frame.
BIT 3	TRANSMIT BEACON. Bit 3, when set to one, indicates that the Adapter is transmitting beacon frames to the ring.
BIT 4	LOBE WIRE FAULT. Bit 4, when set to one, indicates that the Adapter has detected an open or short circuit in the lobe data path. The Adapter will be closed and at the state following Adapter initialization (waiting for an SCB command). The Attached System must wait 500 milliseconds before attempting to execute another OPEN command.
BIT 5	AUTO-REMOVAL ERROR. Bit 5, when set to one, indicates that the Adapter has detected an internal hardware error following the Beacon Auto-removal process and has de-inserted from the ring. The Adapter will be closed and at the state following Adapter initialization (waiting for an SCB command). The Attached System must wait 500 milliseconds before attempting to execute another OPEN command.
BIT 6	RESERVED. This bit is undefined.
BIT 7	REMOVE RECEIVED. Bit 7, when set to one, indicates that the Adapter has received a Remove Ring Station MAC frame request. The Adapter will be closed and at the state following Adapter initialization (waiting for an SCB command). The Attached System must wait 500 milliseconds before attempting to execute another OPEN command.
BIT 8	COUNTER OVERFLOW. Bit 8, when set to one, indicates that an Attached Product Counter has been incremented from 254 to 255.
BIT 9	SINGLE STATION. Bit 9, when set to one, indicates that the Adapter has sensed that it is the only station on the ring. This bit will be reset to zero when another station inserts into the ring.
BIT 10	RING RECOVERY. Bit 10, when set to one, indicates that the Adapter is either transmitting or receiving Claim Token MAC frames. This bit will be reset to zero when the Adapter receives a Ring Purge MAC frame.
BITS 11-15	RESERVED. Bits 11-15 will be set to zero.

COMMAND REJECT Status Interrupt

The SSB will be loaded with COMMAND REJECT STATUS if the Command Field or Address Field of the SCB are in error. The format of the SSB in this situation is shown in Figure 4-36. The Command Field of the SSB will be set to >0002. The Reject Command will be loaded with the Command Field of the offending SCB. Figure 4-37 defines the bit position within the Reject Reason Field.

SSB ADDRESS	**+0**	**>0002**
	+2	**REJECT REASON**
	+4	**REJECT COMMAND**

FIGURE 4-36. COMMAND REJECT SSB FORMAT

ADAPTER CHECK information may be obtained by writing the 16-bit Address Register with the address >05E0 and then reading the next consecutive eight bytes through the Data/Auto-increment register. The Adapter check status format is shown in Figure 4-38. The bit assignments are illustrated in Figure 4-39.

ADAPTER RAM >05E0 +	
0	ADAPTER CHECK
+ 2	PARAMETER 0
+ 4	PARAMETER 1
+ 6	PARAMETER 2

FIGURE 4-38. ADAPTER CHECK STATUS FORMAT

BIT 0	DIO PARITY
1	DMA READ ABORT
2	DMA WRITE ABORT
3	ILLEGAL OP CODE
4	LB PARITY ERROR
5	EM PARITY ERROR
6	SIF PARITY ERROR
7	PH PARITY ERROR
8	RECEIVE PARITY ERROR
9	XMIT PARITY ERROR
10	RING UNDERRUN
11	RING OVERRUN
12	INVALID INTERRUPT
13	INVALID ERROR INTERRUPT
14	INVALID XOP
LSB 15	RESERVED

FIGURE 4-39. ADAPTER CHECK FIELD BIT ASSIGNMENTS

Table 4-26 defines the bits in the 16-bit Adapter Check Field:

TABLE 4-26. ADAPTER CHECK BIT DEFINITIONS (concluded)

BIT	DEFINITION
BIT 11	RING OVERRUN. Bit 11 is set to one if the Adapter detects an internal DMA overrun when receiving from the ring.
BIT 12	INVALID INTERRUPT. Bit 12 is set to one if an unrecognized interrupt was generated internal to the Adapter. Parameters 0-2 will contain the Communications Processor registers R13, R14, and R15, respectively.
SIT 13	INVALID ERROR INTERRUPT. Bit 13 is set to a one if an unrecognized error interrupt was generated. Parameters 0-2 will contain Adapter registers R13, R14, R15.
BIT 14	INVALID XOP. Bit 14 is set to one if an unrecognized XOP request was generated in the Communications Processor's code. Parameters 0-2 will contain the Communications Processor registers R13, R14, and R15, respectively.
BIT 15	RESERVED. This bit should be ignored.

4.4.7 Adapter Commands

This section describes the Adapter SCB commands and subsequent error reporting. Table 4-27 lists the available Adapter commands.

TABLE 4-27. ADAPTER COMMAND SUMMARY

FUNCTION	COMMAND
OPEN	>0003
TRANSMIT	>0004
TRANSMIT HALT	>0005
RECEIVE	>0006
CLOSE	>0007
SET GROUP ADDRESS	>0008
SET FUNCTIONAL ADDRESS	>0009
READ ERROR LOG	>000A
READ ADAPTER BUFFER	>000B

BYTE 0	OPEN OPTIONS	
2	NODE ADDRESS (HIGH)	
4	NODE ADDRESS	
6	NODE ADDRESS (LOW)	
8	GROUP ADDRESS (HIGH)	
10	GROUP ADDRESS (LOW)	
12	FUNCTIONAL ADDRESS (LOW)	
14	FUNCTIONAL ADDRESS (LOW)	
16	RECEIVE LIST SIZE	
18	TRANSMIT LIST SIZE	
20	BUFFER SIZE	
22	EXP. RAM START ADDRESS	
24	EXP. RAM END ADDRESS	
26	XMIT BUFFER MIN COUNT	XMIT BUFFER MAX COUNT
28	PRODUCT ID ADDRESS (HIGH)	
30	PRODUCT ID ADDRESS (LOW)	

FIGURE 4-41. OPEN PARAMETER LIST

TABLE 4-28. OPEN PARAMETER FUNCTIONS

BYTE	FUNCTION
BYTE 0, 1	OPEN OPTIONS. The bit functions of the Open Options field are provided below: BIT 0 WRAP INTERFACE. Setting bit 0 to one on OPEN negates the Ring Insertion Process and causes all user transmit data to appear as user receive data. The data is transmitted on the lobe from the attached product to the wiring concentrator. This option can be used for system interface debug, system interface DMA testing, or lobe media testing. A CLOSE command must be issued to terminate WRAP mode. BIT 1 DISABLE HARD ERROR. If bit 1 is set to a one, the Ring Status HARD ERROR and TRANSMIT BEACON Interrupts will not be generated. BIT 2 DISABLE SOFT ERROR. If bit 2 is set to a one, the Ring Status SOFT ERROR Interrupt will not be generated.

TABLE 4-28. OPEN PARAMETER FUNCTIONS (concluded)

BYTE	FUNCTION
BYTES 8-11	GROUP ADDRESS. This 32-bit field specifies the Group Address and will cause the Adapter to receive messages that are sent to the Group Address. The GROUP ADDRESS can be any value. Bit 0 is ignored by the Adapter. Group Address recognition is disabled by specifying the GROUP ADDRESS as zero.
BYTES 12-15	FUNCTIONAL ADDRESS. This 32-bit field specifies the Functional Address Mask and will cause the Adapter to receive messages that are sent to the Functional Address. FUNCTIONAL ADDRESS bits 0 (the most significant bit), 30 and 31 are ignored by the Adapter. A zero value disables the Functional Address feature.
BYTES 16-17	RECEIVE LIST SIZE. This 16-bit field indicates the number of bytes the Adapter will read when obtaining a Receive List from the attached system. A decimal value of 0, 14, 20, or 26 is required. If zero, the default value of 26 is used.
BYTES 18-19	TRANSMIT LIST SIZE. This 16-bit field indicates the number of bytes the Adapter will read when obtaining a Transmit List from the attached system. A decimal value of 0, 14, 20, or 26 is required. If zero, the default value of 26 is used.
BYTES 20-21	BUFFER SIZE. This 16-bit field indicates the Adapter's internal buffer size in bytes. BUFFER SIZE must be greater than or equal to 96. The three low-order bits must be zero. If this field is zero, a default value of 112 bytes is used.
BYTES 22-23	EXPANSION RAM START ADDRESS. This 16-bit parameter defines an expansion RAM start address within the Adapter. This additional RAM may be used for transmit and/or receive buffers. If this field is zero, no external RAM is defined within the Adapter. If bit 15 is set to one, the existing internal TMS38010 RAM will not be used for transmit or receive buffers, defaulting to the expansion RAM. External RAM expansion must fall within the address range >1000 to >BFFF. The RAM start address must be on an eight-byte boundary minus two bytes (bits 13 and 14 are "11"). For example, if the expansion RAM starts at >4000, this parameter would be>4006. The expansion RAM and decode logic are tested, but if bad parity is detected, an ADAPTER CHECK Parity Error will be issued.
BYTES 24-25	EXPANSION RAM END ADDRESS. This 16-bit field specifies the ending address of Adapter expansion RAM. If the EXPANSION RAM START ADDRESS is zero, this field is ignored.
BYTE 26	TRANSMIT BUFFER MINIMUM COUNT. This byte parameter contains the number of Adapter buffers that are to be reserved as transmit buffers. These buffers will be reserved for transmit only and will never be used for receive. If zero is specified, no buffers are reserved for transmit. The minimum transmit buffer count must be equal to or less than the transmit maximum buffer count (byte 27).
BYTE 27	TRANSMIT BUFFER MAXIMUM COUNT. This byte parameter contains the maximum number of Adapter buffers that are to be used for transmit. A minimum of two buffers must be available for receive. If zero, a default value of six is used. The product of TRANSMIT BUFFER MAXIMUM COUNT and (BUFFER SIZE −8) determines the maximum size frame that the Adapter can transmit.
BYTES 28-31	PRODUCT ID ADDRESS. This 32-bit field contains a 24-bit address of the attached system Product ID. Eighteen bytes are read starting from the location specified during the OPEN command processing. After the OPEN command is complete, these 18 bytes in attached system memory may be released for other purposes. The bytes read are included in the product ID subvector of the Report Station Attachment MAC frame. This frame is transmitted in response to the Request Station Attachment MAC frame.

TABLE 4-30. OPEN PHASES AND OPEN ERROR CODES

BITS 8	9	10	11	OPEN COMMAND PHASES
0	0	0	1	Lobe Media Test
0	0	1	0	Physical Insertion
0	0	1	1	Address Verification
0	1	0	0	Participation in ring poll
0	1	0	1	Request Initialization
BITS 12	**13**	**14**	**15**	**OPEN ERROR CODES**
0	0	0	1	Function Failure
0	0	1	0	Signal Loss
0	1	0	1	Timeout
0	1	1	0	Ring Failure
0	1	1	1	Ring Beaconing
1	0	0	0	Duplicate Node Address
1	0	0	1	Request Initialization
1	0	1	0	Remove Received

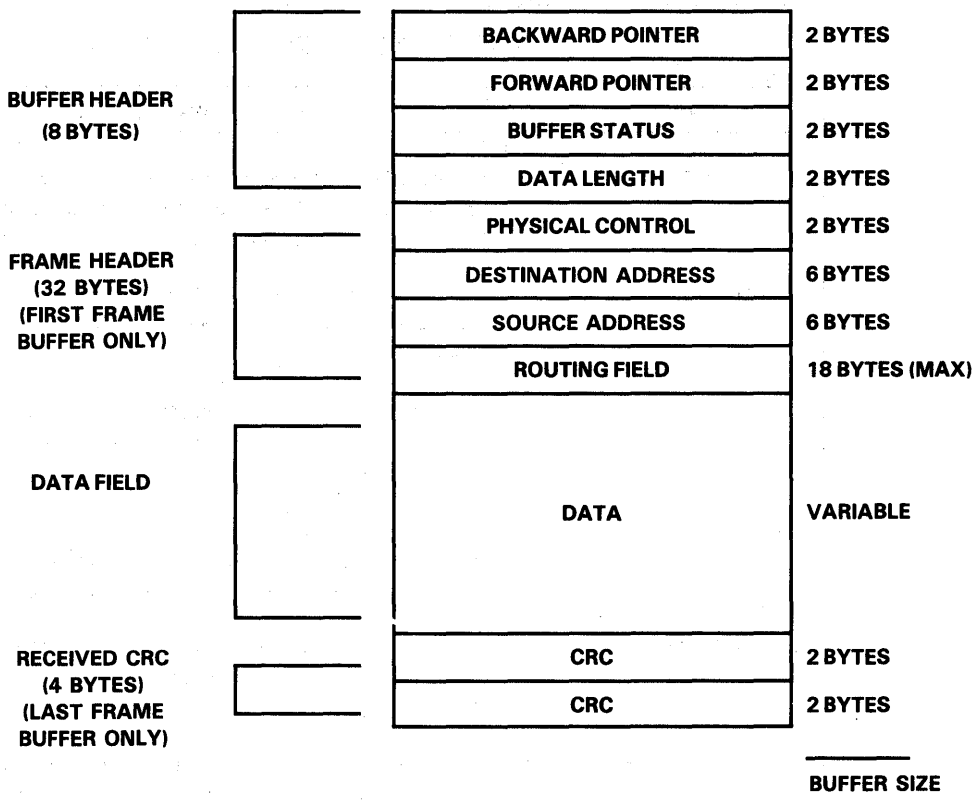


FIGURE 4-43. ADAPTER INTERNAL BUFFER FORMAT

Buffer Allocation

Without memory expansion, the Adapter has 1792 bytes of RAM available for a buffer pool for both the reception of frames from the ring media and transmission of frames to the ring media. When the attached system requests a frame transmission, buffers are taken from the buffer pool one at a time until the frame has been transferred to the Adapter. The user can specify a maximum number of these buffers to be used for transmission. The rest are dedicated receive buffers.

The TRANSMIT BUFFER MAXIMUM COUNT of the OPEN parameters must leave at least two buffers available to receive frames. A maximum of two transmit frames can be processed simultaneously by the Adapter. One will be enqueued for transmission while the other is transferred across the System Interface, or both frames can be enqueued for transmission.

The maximum number of buffers that can be taken for frame transmission is specified in the TRANSMIT BUFFER MAXIMUM COUNT of the OPEN parameters. If the system requests transmission of a single frame that causes the number of buffers required to transmit the frame, to exceed the TRANSMIT BUFFER MAXIMUM COUNT, the TRANSMIT command will be terminated with LIST ERROR.

Buffer Size

The 1792 bytes of RAM for a buffer pool will configure into sixteen 112-byte buffers. The default TRANSMIT MAXIMUM COUNT is six, allowing a transmit frame maximum information field size of 600 bytes including a 32 byte frame header and 4 byte CRC field. The attached system can alter the buffer size with the OPEN Command BUFFER SIZE parameter.

TABLE 4-32. ATTACHED SYSTEM FRAME FIELDS

FRAME	FIELD
AC	ACCESS CONTROL FIELD. This control field consists of the following bit functions: BITS 0-2 ACCESS PRIORITY. Bits 0-2 select the Access Priority for the frame. This value (0-3) must be less than or equal to the Allowed Access Priority. BITS 3-7 RESERVED. These bits should be reset to zero.
FC	FRAME CONTROL FIELD. This 8-bit field is defined in detail in Section 3. If the MAC Indicator bit is set to zero, the Enabled Function Class parameter is used to validate the Major Vector Source Class.
DESTINATION ADDRESS	This field is 48 bits wide and contains the address of the destination. The address format for this field is explained in Section 3. The address contained within this six-byte field must be organized in system memory with the highest order byte occupying the lowest system byte address and the lowest order byte occupying the highest system byte address.
SOURCE ADDRESS	This field is ignored with the exception of byte 0 bit 0 (the Routing Information Indicator). The Node Address that is supplied by the Burned-in Address (BIA) or passed during the OPEN command will be used for the remaining bits of the source address of the frame.
ROUTING FIELD	The Routing Field must be included if bit 0 of the Source Address field is set to one.
DATA	The Data portion is transmitted as specified by the attached system. The CRC, Ending Delimiter, and FS are appended to the data by the Adapter.

4

Transmit Command Block

The TRANSMIT command will be rejected with Adapter COMMAND REJECT STATUS if the Adapter has not been opened, if there is already an executing TRANSMIT command, or if the address passed in the SCB is not aligned on a 16-bit boundary.

The System Command Block for a TRANSMIT command is shown in Figure 4-45.

SCB ADDRESS	**+0**	**>0004**
	+2	**ADDRESS (HIGH)**
	+4	**ADDRESS (LOW)**

FIGURE 4-45. TRANSMIT SCB

TABLE 4-33. TRANSMIT PARAMETER LIST FIELDS

FIELD	DESCRIPTION
FORWARD POINTER	This 32-bit field contains a 24-bit address which is a pointer to the next Transmit Parameter List in the chain. When this address is ODD, it denotes that the current Transmit List is the last in the chain. The Adapter will continue to process Transmit Lists until it reads an ODD address. It will then wait for the last frame (list with ODD address) to be transmitted onto the ring. If the system updates the FORWARD POINTER before the last frame is transmitted, the Adapter will continue to process the Transmit Lists. If not, the TRANSMIT command will complete and another must be issued to continue. The system must update the FORWARD POINTER from the most significant byte to the least significant byte to ensure that the address is valid before changing to an EVEN address. Frames, not lists that define partial frames, should be added to the chain. The FORWARD POINTER should not be initialized to point to itself, as problems may occur due to the pipelined nature of list processing employed by the Adapter. Transmit Lists must be aligned on 16-bit boundaries. The Adapter will not alter this parameter.
FRAME SIZE	This 16-bit field contains the number of bytes to be transmitted as a frame. The FRAME SIZE value includes AC/FC, DESTINATION and SOURCE ADDRESS, the Routing Field, and the Information Field. FRAME SIZE does not include CRC, FS, or EDEL. This parameter is valid only for the Transmit List that has the FRAME START bit set, however, FRAME SIZE must NOT be zero in any list. The Adapter will not alter this parameter. A frame size of zero is not valid. The maximum frame size which can be transmitted is (BUFFER SIZE -8) $\times$ TRANSMIT BUFFER MAXIMUM COUNT.
DATA COUNT	This 16-bit field contains the number of bytes to be transmitted starting from the address defined in the DATA ADDRESS parameter. There can be a maximum of three DATA COUNT/DATA ADDRESS parameters to provide a gather write capability per Transmit List (not frame). If Bit 0 is zero, it is the last DATA COUNT in the Transmit List. Bit 0 of the third DATA COUNT is ignored. A DATA COUNT of 0 is permitted (with or without Bit 0 set). The sum of the used DATA COUNT parameters must equal the FRAME SIZE specified on the Start of Frame List. The DATA COUNT can be even or odd. The Adapter will not alter this parameter.
DATA ADDRESS	This 32-bit field contains the 24-bit address of the data to be transmitted. DATA ADDRESS may be even or odd. The Adapter will not alter this parameter.
TRANSMIT CSTAT	TRANSMIT COMMAND/STATUS. This 16-bit parameter is set by the attached system when the Transmit List is created. It is over-written by the Adapter to report frame completion status. When initially set by the attached system, this parameter field is referred to as the TRANSMIT CSTAT REQUEST field. After a frame completes transmission, the Adapter will overwrite bits in this field only in the list which starts the frame. These bits indicate the completion status of the frame. This parameter field is referred to as the TRANSMIT CSTAT COMPLETE. Note that command and status information within the TRANSMIT CSTAT field is associated with frames and not the TRANSMIT command directly.

Transmit Completion

An interrupt will be generated for the TRANSMIT command when:

- All the frames specified by the Transmit Parameter List Chain have been transmitted, or
- The TRANSMIT HALT command has completed, or
- A frame has been transmitted that had FRAME INTERRUPT set in CSTAT, or
- A list error is detected.

The SSB will be loaded as shown in Figure 4-47.

SSB ADDRESS		
	+ 0	>0004
	+ 2	XMIT COMPLETE
	+ 4	LIST ADDRESS (HIGH)
	+ 6	LIST ADDRESS (LOW)

FIGURE 4-47. TRANSMIT SSB

The Transmit Complete Field bit definitions are provided in the following table:

The attached system can create a chain of a fixed number of Transmit Lists, set the last list FORWARD POINTER to the address of the first list, and manipulate the VALID bits to initiate transmission.

When the Adapter reads a Frame Start List with the VALID bit reset to zero, it will suspend processing until a TRANSMIT VALID Interrupt Request is issued by the system by writing to the INTERRUPT ADAPTER (bit 0) and the TRANSMIT VALID (bit 7) bits of the Interrupt register. The system is not notified of this condition. The TRANSMIT VALID Interrupt should be issued when changing one or more VALID bits from zero to one, when the list is on the Transmit Chain.

The TRANSMIT VALID interrupt can be issued at any time and the Adapter will ignore the interrupt if it is not waiting for a VALID bit transition.

If a fixed Transmit Chain technique is utilized and more than one list is used to transmit a single frame, lists that do not have the FRAME START bit set should have the VALID bit reset to zero. Since the Adapter does not alter the CSTAT field for lists that are not Start of Frame, re-validating of the start of frame list will also release the remaining frame lists if the VALID bits were initially set.

A chain should not be made with a one frame list. Due to the pipelined nature of transmit list processing, (i.e. the first frame is transmitted while the second frame is concurrently DMAed from system memory) this technique can cause the Adapter to erroneously send the same frame twice.

The DATA ADDRESS parameters in the Transmit List can be on even or odd byte boundaries. If the Adapter is to read data from an even byte system address to an internal odd byte address (due to an odd Data Count), it will transfer a single byte and transfer the remaining data starting at an odd system address.

Since Transmit Lists can be added dynamically to the Transmit Chain, a test should be made following COMMAND COMPLETE to determine if the Adapter has processed all frames that the attached system has placed on the chain. If frames have been added to the chain subsequent to the TRANSMIT command, the FORWARD POINTER at the address contained in LIST ADDRESS should be examined following COMMAND COMPLETE. If the FORWARD POINTER is ODD, all frames have been transmitted. If the FORWARD POINTER is EVEN, another TRANSMIT command should be executed with the SCB pointer to the Transmit List Chain set equal to that FORWARD POINTER.

Transmit List Examples

Three examples (Figures 4-48 to 4-50) of possible list formats will be illustrated and all result in the transmission of a single 400-byte frame. Figure 4-50 is configured such that the attached system buffer space is appended to a 14-byte list.

The fourth example (Figure 4-51) illustrates two lists chained together to form the Transmit Chain for transmission of two frames.

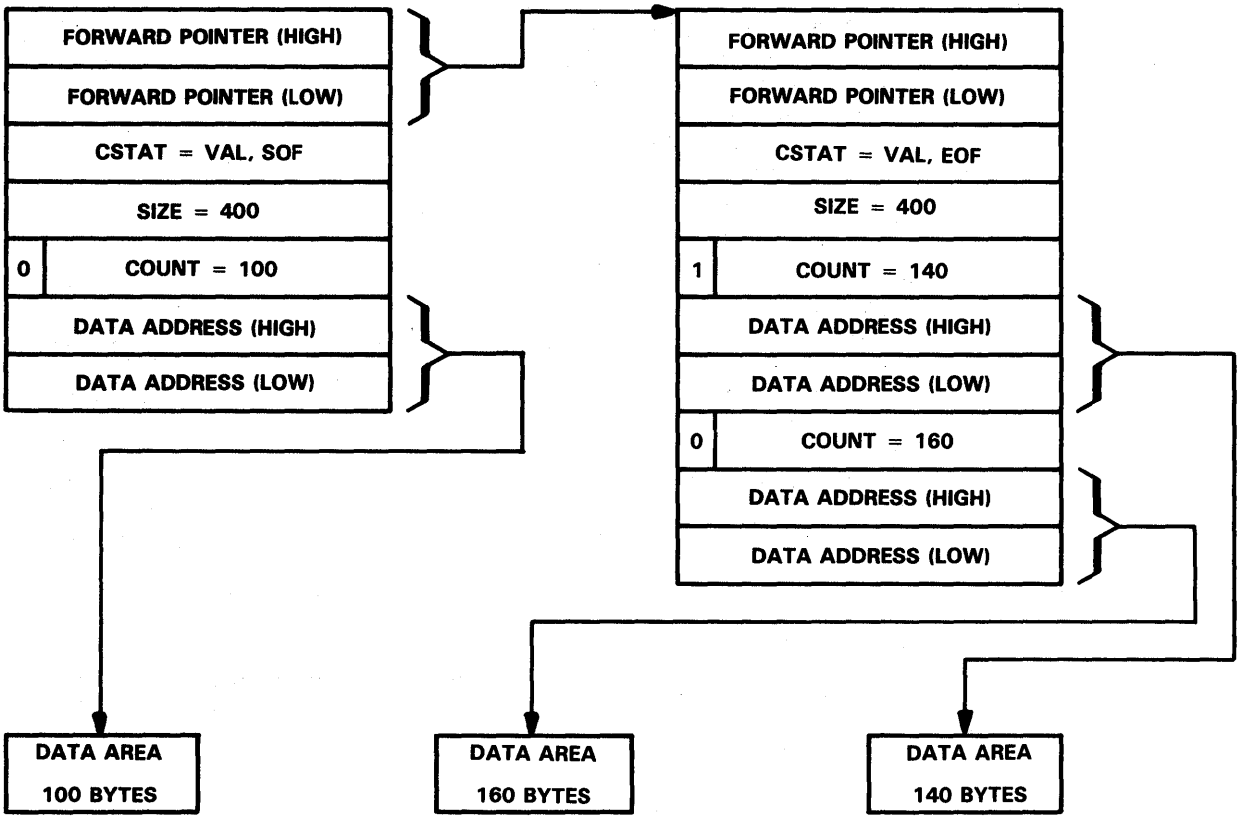


FIGURE 4-49. TRANSMIT LIST FORMAT: EXAMPLE 2

The 32-bit field following the COMMAND field of the SCB is read by the Adapter, but ignored.

4.4.7.4 RECEIVE Command

The RECEIVE command is used to receive frames from other stations on the ring. This command normally is issued only once (after OPEN), since receive data is dynamically added to a Receive Parameter List Chain. The RECEIVE command can be terminated by issuing the CLOSE command.

The logical format of received frames passed across the system interface is identical to the logical format of transmit frames, as shown in Figure 4-44.

The AC and FC, destination address and source address fields, are transferred to the attached system as they were received from the ring.

The Routing Field is passed to the attached system for all frames, if received. If the PAD ROUTING FIELD option is specified during OPEN,the routing field will be padded to 18 bytes. If the frame does not contain a Routing Field the field will still be padded to 18 bytes. The padding will not alter the contents of the system's data buffer.

The RECEIVE command will be rejected with Adapter COMMAND REJECT STATUS under the following conditions:

- If the Adapter has not been opened, or
- If there is already an executing RECEIVE command, or
- If the address passed in the SCB is not word aligned.

RECEIVE Command Block

The SCB for a RECEIVE command is shown in Figure 4-53.

SCB ADDRESS	+ 0	>0006
	+ 2	ADDRESS (HIGH)
	+ 4	ADDRESS (LOW)

FIGURE 4-53. RECEIVE COMMAND SCB

The 32-bit ADDRESS field contains a 24-bit address pointer to a Receive Parameter List Chain. The high-order byte of this field is ignored. This address must be word-aligned.

RECEIVE Parameter List

The attaching system creates a chained Receive Parameter List as shown in Figure 4-54. The address of the Receive Parameter list is in the RECEIVE command SCB. A single Receive Parameter List cannot be used to receive more than one frame. Several Receive Parameter Lists can be used to receive a single frame.

The Receive Parameter List is a 14, 20 or 26-byte data structure as shown in Figure 4-54.

TABLE 4-35. RECEIVE PARAMETER LIST FIELD DEFINITIONS

POINTER	DEFINITION
FORWARD POINTER	This 32-bit field contains a 24-bit address pointer to the next RECEIVE Parameter List in the chain. When this address is odd, it denotes that the current RECEIVE Parameter List is the last in the chain. The Adapter will DMA write a received frame into the address(es) specified in the RECEIVE List and then check the FORWARD POINTER. If it is odd, the Adapter will interrupt the system with a request to place additional lists on the chain. The Adapter will not terminate the RECEIVE command and will wait for a RECEIVE CONTINUE Interrupt Request to resume the receive operation. The attached system must update the FORWARD POINTER from the most significant byte to the least significant byte to ensure that the address is valid before changing to an EVEN address. Receive Lists must be aligned on 16-bit boundaries. The Adapter will not alter this parameter.
FRAME SIZE	This 16-bit field contains the number of bytes in the received frame. The Adapter will store this count in the Receive List which starts a new frame. FRAME SIZE includes AC, FC, Destination and Source Address, Routing Field (if any), pad length (if PAD ROUTING FIELD specified), and the Data Field. FRAME SIZE does not include CRC, FS, or EDEL.
DATA COUNT	This 16-bit field contains the maximum number of bytes that can be stored starting at the address defined in the DATA ADDRESS parameter. There can be a maximum of three DATA COUNT/DATA ADDRESS parameters to provide a scatter write capability per Received List (not frame). If bit 0 is cleared, it is the last DATA COUNT in the Receive List. Bit 0 of the third DATA COUNT is ignored. A zero DATA COUNT is permitted (with or without Bit 0 set). The DATA COUNT can be even or odd. The Adapter will not alter this parameter. If the PAD ROUTING FIELD option is specified during the OPEN command, then the first DATA COUNT in a Receive List used for start of frame must be at least 32. This allows space for the AC, FC, DESTINATION ADDRESS, SOURCE ADDRESS, and the ROUTING FIELD which will be padded to 18 bytes. If the DATA COUNT is less than 32, the option will be voided.
DATA ADDRESS	This 32-bit field contains the address of the data to be received. DATA ADDRESS may be even or odd. The Adapter will not alter this parameter.
RECEIVE CSTAT	RECEIVE COMMAND/STATUS. This 16-bit parameter is set by the attached system when the Receive List is created and is over-written by the Adapter to report frame completion status. When initially set by the attached system, this parameter field is referred to as the RECEIVE CSTAT REQUEST field. After receiving a frame, the Adapter will overwrite bits in this field only in the list which starts a frame and the list which ends a frame. However, if the last list used contained an odd FORWARD POINTER, then this field will not be written until additional lists are added to the chain (FORWARD POINTER made even and RECEIVE CONTINUE written to the Interrupt Register). These bits indicate the completion status of the frame. This parameter field is referred to as the RECEIVE CSTAT COMPLETE. Note that command and status information within the RECEIVE CSTAT field is associated with frames and not directly with the RECEIVE command.

RECEIVE Completion

An interrupt will be generated for the RECEIVE command when the Receive Parameter List chain has ended (odd address in FORWARD POINTER) or when a frame is copied into a list that has Frame Interrupt set in the CSTAT parameter. Note that the RECEIVE command NEVER terminates but rather enters a suspended state waiting for the RECEIVE VALID or the RECEIVE CONTINUE bits of the Interrupt register to be set.

The SSB upon receive completion will be loaded as shown in Figure 4-55.

SSB ADDRESS	**+ 0**	**>0006**
	+ 2	**RECEIVE COMPLETE**
	+ 4	**LIST ADDRESS**
	+ 6	**LIST ADDRESS**

FIGURE 4-55. RECEIVE COMMAND SSB

The RECEIVE COMPLETE Field bit definitions are provided in Table 4-36.

TABLE 4-36. RECEIVE COMPLETE FIELD BIT DEFINITIONS

BIT	DEFINITION
BIT 0	FRAME COMPLETE. Bit 0 is set to one to indicate that a frame has been received and the FRAME INTERRUPT or INTERFRAME WAIT bit was set in CSTAT. Since frames can be received and transferred faster than the attached system can respond to the interrupts and/or faster than the Adapter can cause the interrupts, the FRAME COMPLETE interrupt can report the completion of more than one frame at a time. The 32-bit LIST ADDRESS will contain the address of the last Receive List of the last frame transferred to the system. If lists with the FRAME INTERRUPT bit set are intermixed with lists that do not have FRAME INTERRUPT set, FRAME COMPLETE can include frames that did not have FRAME INTERRUPT set. FRAME COMPLETE will not be set with the RECEIVE SUSPENDED bit also set.
BIT 1	RECEIVE SUSPENDED. Bit 1 is set to one when the Adapter detects an odd address in the Receive Parameter List Chain. LIST ADDRESS will contain the address of the list that has an odd FORWARD POINTER. The attached system must update the FORWARD POINTER and issue a RECEIVE CONTINUE Interrupt Request in order to continue. RECEIVE SUSPENDED will not be set with the FRAME COMPLETE bit also set.
BITS 2-15	RESERVED. Bits 2-15 are reset to zero.

The examples (Figure 4-48 to Figure 4-51) for Transmit Parameter List Formats can also be applied to Receive Parameter Lists Formats.

An attached system can create a chain of a fixed number of Receive Parameter Lists by setting the last list FORWARD POINTER to the address of the first list, and manipulate the VALID bits appropriately to initiate reception.

CLOSE Command Block

The SCB for a CLOSE command is shown in Figure 4-56.

SCB ADDRESS	+ 0	>0007
	+ 2	---
	+ 4	---

FIGURE 4-56. CLOSE COMMAND SCB

The 32-bit field following the COMMAND field is read by the Adapter, but ignored.

CLOSE Completion

Upon close completion the SSB will be loaded with Close Completion status as shown in Figure 4-57.

SSB ADDRESS	+ 0	>0007
	+ 2	CLOSE COMPLETION

FIGURE 4-57. CLOSE COMMAND SSB

Table 4-37 describes the CLOSE COMPLETION field bit definitions.

TABLE 4-37. CLOSE COMPLETION FIELD BIT DEFINITIONS

BIT	DEFINITION
BIT 0	ADAPTER CLOSED. Bit 0 is set to one when the CLOSE command is completed.
BITS 1-15	RESERVED. Bits 1-15 are reset to zero.

4.4.7.6 SET GROUP ADDRESS Command

The SET GROUP ADDRESS command is used to set the Adapter Group Address if it is to be changed after OPEN. The SET GROUP ADDRESS command will be rejected with COMMAND REJECT STATUS if the Adapter is not open.

SET GROUP ADDRESS Command Block

The SCB for a SET GROUP ADDRESS command is shown in Figure 4-58.

SCB ADDRESS	+ 0	>0008
	+ 2	GROUP ADDRESS (HIGH)
	+ 4	GROUP ADDRESS (LOW)

FIGURE 4-58. SET GROUP ADDRESS COMMAND SCB

The 32-bit address following the COMMAND field in the SCB is the Group Address and is stored in the Adapter Group Address Register. Bit zero is ignored.

Table 4-39 describes the SET FUNCTIONAL ADDRESS Completion field bit definitions.

TABLE 4-39 SET FUNCTIONAL ADDRESS COMPLETION FIELD BIT DEFINITIONS

BIT	DEFINITION
BIT 0	COMMAND COMPLETE. Bit 0 is set when the SET FUNCTIONAL ADDRESS command is completed.
BITS 1-15	RESERVED. Bits 1-15 are reset to zero.

4.4.7.8 READ ERROR LOG Command

The READ ERROR LOG command is used to read and reset the Adapter Attached Product Error Log. After READ ERROR LOG command completion, the Error Log will be all zeros.

READ ERROR LOG Command Block

The SCB for a READ ERROR LOG command is shown in Figure 4-62.

SCB ADDRESS	+ 0	>000A
	+ 2	ADDRESS (HIGH)
	+ 4	ADDRESS (LOW)

FIGURE 4-62. READ ERROR LOG COMMAND SCB

The 32-bit ADDRESS field contains a 24-bit starting address location where the 14-byte Error Log will be written in attached system memory. The 14-byte Error Log table is shown in Figure 4-63. See Table 4-40 for a description of these error counts.

BYTE			
	+ 0	LINE ERROR	RESERVED
	+ 2	BURST ERROR	ARI/FCI ERROR
	+ 4	RESERVED	RESERVED
	+ 6	LOST FRAME ERROR	RECEIVE CONGESTION ERROR
	+ 8	FRAME COPIED ERROR	RESERVED
	+10	TOKEN ERROR	RESERVED
	+12	DMA BUS ERRORS	DMA PARITY ERRORS

FIGURE 4-63. ERROR LOG TABLE

READ ERROR LOG Completion

Upon completion of the READ ERROR LOG command, the SSB will be loaded with READ ERROR LOG completion status as shown in Figure 4-64.

SCB ADDRESS	+ 0	>000A
	+ 2	ERROR LOG COMPLETION

FIGURE 4-64. READ ERROR LOG COMMAND SSB

Table 4-41 describes the READ ERROR LOG COMPLETION field bit definitions.

TABLE 4-41. READ ERROR LOG COMPLETION FIELD BIT DEFINITIONS

BIT	DEFINITION
BIT 0	COMMAND COMPLETE. Bit 0 is set to one when the READ ERROR LOG command is completed.
BITS 1-15	RESERVED. Bits 1-15 are reset to zero.

4.4.7.9 READ ADAPTER BUFFER Command

The READ ADAPTER BUFFER command is used to transfer Adapter storage across the System Interface to attached system memory.

READ ADAPTER BUFFER Command Block

The SCB for a READ ADAPTER BUFFER command is shown in Figure 4-65.

SCB ADDRESS	+ 0	>000B
	+ 2	ADDRESS
	+ 4	ADDRESS

FIGURE 4-65. READ ADAPTER BUFFER COMMAND SCB

The 32-bit ADDRESS field contains a 24-bit address pointer to buffer space in the attached system memory. The system buffer space is shown in Figure 4-66.

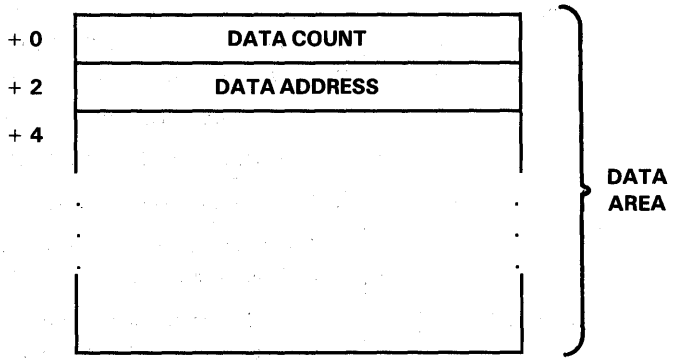


FIGURE 4-66. READ ADAPTER SYSTEM BUFFER SPACE

The 16-bit DATA COUNT field contains the number of bytes to read from the Adapter. The data will be stored starting at the DATA COUNT location which is at the beginning of the system's buffer space.

Table 4-43 describes the READ ADAPTER BUFFER Completion field bit definitions.

TABLE 4-43. READ ADAPTER BUFFER COMPLETION FIELD BIT DEFINITIONS

BIT	DEFINITION
BIT 0	COMMAND COMPLETE. Bit 0 is set when the READ ADAPTER BUFFER command is completed.
BITS 1-15	RESERVED. Bits 1-15 are reset to zero.

4.5 Ring Interface

Interface of the Adapter to the twisted pair cabling is via a Ring Interface circuit (RI), containing two bipolar MSI circuits and several discrete components. This section describes briefly the function of the Ring Interface circuit. The "TMS38051 and TMS38052 Ring Interface Circuits" data sheet should be consulted for additional detail on electrical characteristics.

4.5.1 TMS38051 and TMS38052 Components

The two bipolar MSI chips are an analog chip set which provide the IEEE 802.5 compatible interface functions required to transmit and receive data between the TMS38020 Protocol Handler (PH) and the token ring cabling.

These chips are referred to as the TMS38051 and the TMS38052; the TMS38051 Transceiver provides the transmit and receive functions while the TMS38052 Controller provides ring interface control functions.

The functional block diagram of the ring interface and the division of this function between the TMS38051 and the TMS38052 is illustrated in Figure 4-68.

4.5.2 Ring Interface Interconnect Schematic

Figure 4-69 illustrates a schematic suitable for implementating the ring interface function. Included in this schematic are all the necessary discrete components in addition to a 74LS164 and a 512 x 4 PROM for implementing the Adapter Burned-in-address (BIA), and a 74LS122 which serves as a watchdog timer.

Table 4-44 provides a list of discrete component values, tolerances, and part types.

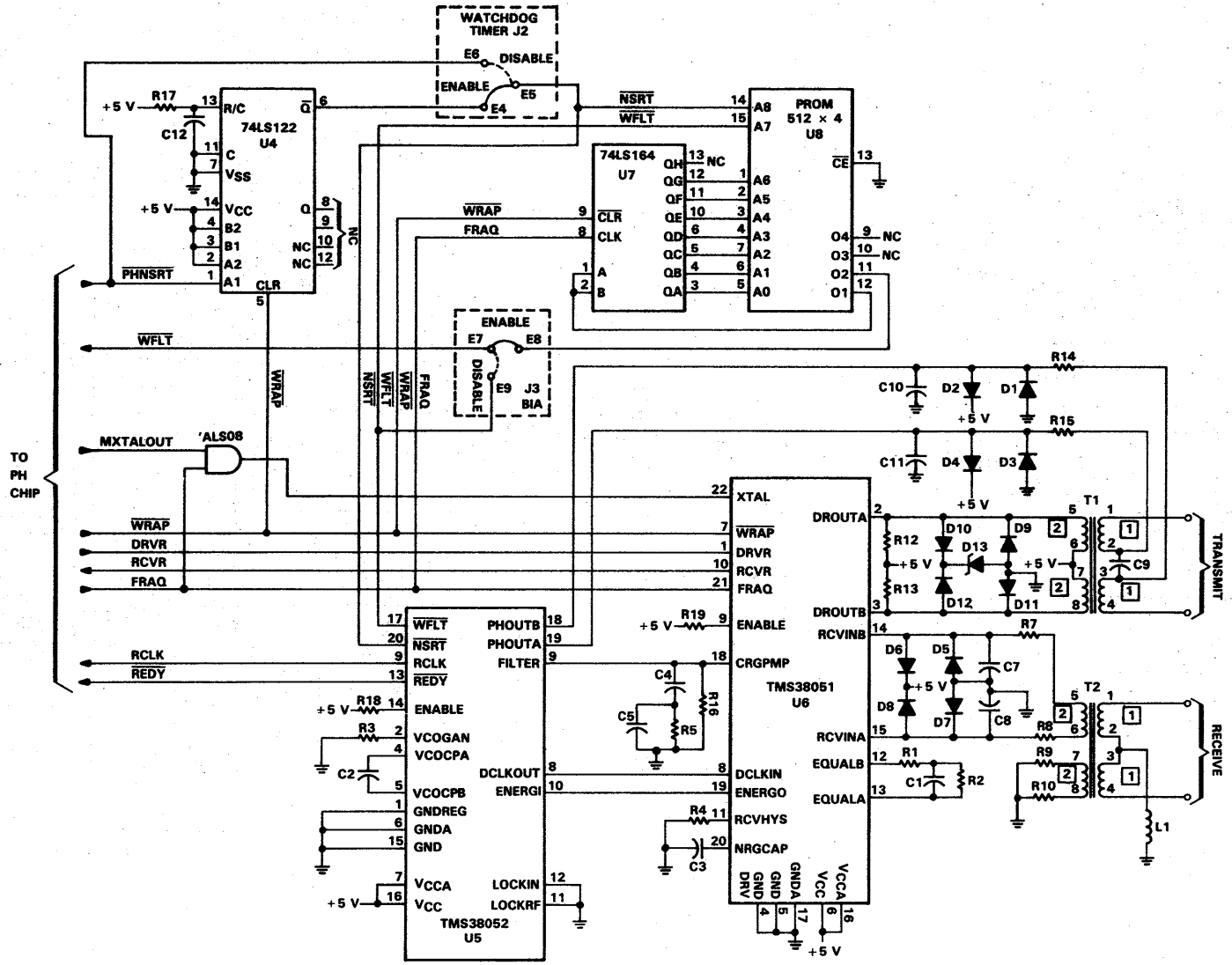


FIGURE 4-69. RING INTERFACE SCHEMATIC

The Adapter's program code toggles the $\overline{\text{PHNSRT}}$ line every 10 milliseconds whenever an inserted condition is desired. This maintains the state of $\overline{\text{NSRT}}$ active-low. If a condition exists which prevents the Communications Processor from toggling the $\overline{\text{PHNSRT}}$ signal, the one-shot times out and the Adapter is physically de-inserted from the ring.

This feature is added as an enhancement to ring reliability, avoiding the possibility that clock failure or code problems within an Adapter will cause ring corruption. If errors occur such that the TMS38010 Communications Processor cannot maintain a "heartbeat" on the $\overline{\text{PHNSRT}}$ line, the Adapter is automatically de-inserted from the ring.

4.5.4 Burned-in Address

The 512 x 4 PROM and the 74LS164 implement the burned-in address feature of the Adapter. This PROM is read by the Adapter upon power-on and will use the 48-bit address read as the node address if one is not passed during the OPEN command. Appendix B discusses the Burned In Address (BIA) in detail.

4.5.5 TMS38020 Protocol Handler to Ring Interface Signals

Table 4-45 describes the signals which exist between the Protocol Handler and the Ring Interface circuit.

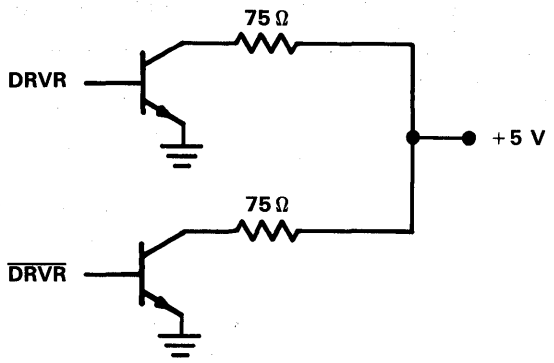


FIGURE 4-70. TMS38051 LINE DRIVER STAGE

4.5.7 Ring Interface Receiver

The receive channel of the TMS38051 provides functions for equalization, signal shaping and retiming of the received data. The TMS38051 is transformer coupled to the transmission media to reject any DC offsets in the differential signal. Receive circuitry within the TMS38051 independantly biases the two differential inputs, RCVINA and RCVINB, to VCC/2. A common mode rejection of 40 dB is provided for a 4 megabit per second transmission rate on the twisted pair. A low pass filter is included between the transformer and the TMS38051 to attenuate high frequency noise.

4.5.7.1 Equalization

The TMS38051 receive function utilizes a two state adaptive equalizer to compensate for the transmission line attenuation of high frequencies. The term "two state" is derived from the fact that the equalizer function is effective for low amplitude signals, and is transparent to high amplitude signals. Equalization is not needed for high amplitude signals because this is indicative of a short transmission line length. The two state nature of the equalizer is the result of nonlinearities within the equalizer circuit.

The external equalization components are used to set the transfer function of the equalizer and the signal level below which equalization is effective. At low frequencies, the low frequency equalizer gain is set by the sum of the two resistors, R1 and R2. At high frequencies the capacitor, C1, bypasses R2 and the equalizer gain is set by R1. With the components listed in Table 4-46, at 1.5 MHz the equalizer gain increases from its low frequency value to its high frequency value at a rate of 20 db per decade. Figure 4-71 illustrates the transfer function of the TMS38051 equalizer for low amplitude inputs.

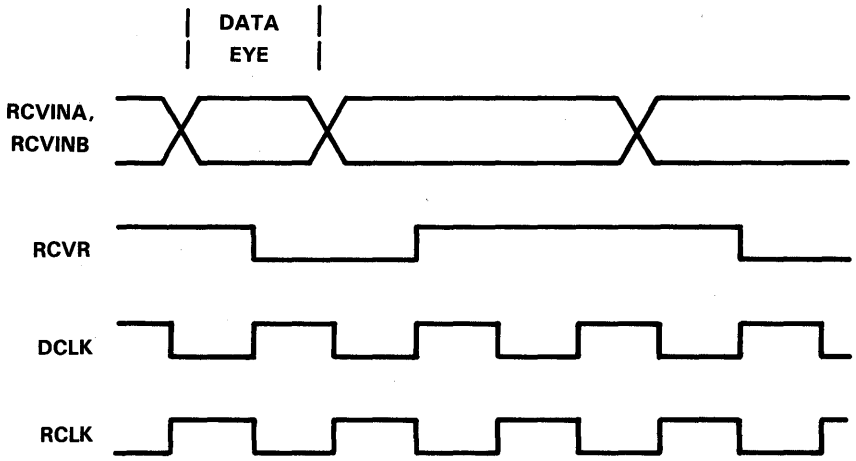


FIGURE 4-72. RECEIVE TIMING RELATIONSHIPS

4.5.8 Ring Interface Phase Locked Loop

The recovery of the 8 MHz data clock embedded in the received Differential Manchester encoded data is accomplished by a phase locked loop (PLL) that is integrated into the TMS38051 and TMS38052. The loop filter is the only function of the PLL that is implemented entirely in discrete components, although the transfer function of the voltage controlled oscillator is set via discrete components. The ring interface schematic diagram in Figure 4-69 implements a 2nd order phase locked loop with a bandwidth of 97.6 kHz and a loop damping factor of 25.7. A block diagram of the phase locked loop is shown in Figure 4-73. A description of each functional unit is provided in the following sections.

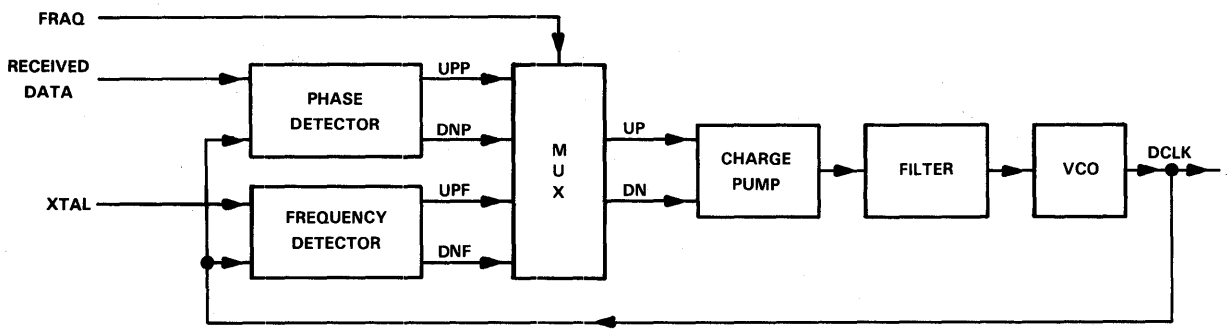


FIGURE 4-73. PHASE LOCKED LOOP BLOCK DIAGRAM

4.5.8.1 Voltage Controlled Oscillator

The recovered data clock, DCLK, that is used by the data retiming latch, the phase detector, and the frequency detector is generated by a voltage controlled oscillator (VCO) integrated into the TMS38052. The VCO function is broken into two stages. First, a voltage to current converter which converts the PLL filter voltage into a biasing

4.5.8.3 Frequency Detector

A frequency detector has been implemented in the ring interface PLL to bring the VCO frequency within the operating range of the PLL. This function is necessary because during startup and fault conditions, the VCO frequency can drift outside the pull in range of the PLL. The output of the frequency detector is a set of command lines, UPF and DNF, similar to to those of the phase detector. The signal FRAQ is used to multiplex the phase detector and the frequency detector outputs to the charge pump. The ring interface PLL is in frequency acquisition mode (frequency detector outputs selected) when FRAQ is asserted high.

The frequency detector charge pump controls are asserted somewhat differently than the phase detector charge pump controls. Unlike the phase detector, the frequency detector is activated by high to low transitions at the input. In the quiescent state, both UPF and DNF are deasserted. A falling edge on either DCLK or XTAL causes a rising edge on one of the control lines. DCLK falling causes DNF to rise and XTAL falling causes UPF to rise. The UPF or DNF line is returned to a low state upon detection of a falling edge on the input that did not cause the transition from low to high. For example, if DCLK caused DNF to rise, then the falling edge of DNF must be caused by XTAL. When XTAL and DCLK are locked, their falling edges will be coincident and both UPF and DNF will remain low. Figure 4-75 illustrates the frequency detector timing characteristics. Because the frequency detector is not always pulsing both DNF and UPF, The gain of the phase locked loop is much greater than in phase detection mode. This allows the VCO to rapidly acquire the frequency of XTAL when FRAQ is asserted.

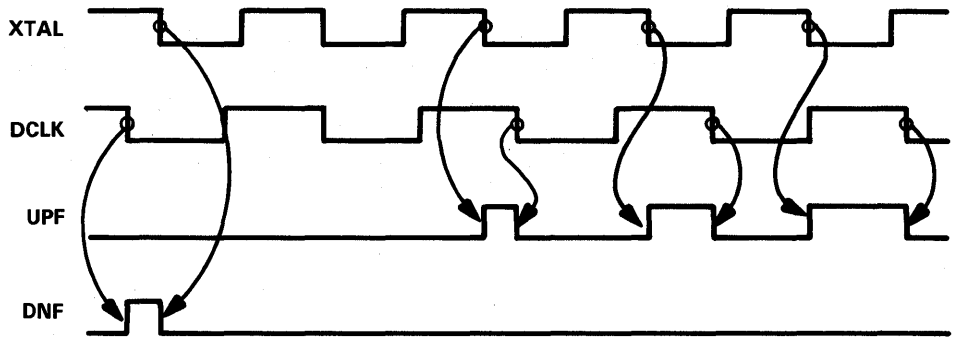


FIGURE 4-75. FREQUENCY DETECTOR TIMING CHARACTERISTICS

4.5.8.4 Charge Pump and Loop Filter

The charge pump converts the train of pulses that are output from the frequency/phase detector into a controlling current for the PLL filter. In response to a pulse on the UP line, the charge pump sources current to the loop filter, a pulse on DN causes the charge pump to sink current. The charge pump is specified to sink or source 0.4 mA ±15% for the duration of a pulse. The loop filter acts as an integrator of the charge pump current. When the VCO is phase aligned with the received data, the pulse widths of the UP and DN lines are equal. The net result is no change in the DC voltage on the PLL filter. The selection of loop filter components determine how the voltage at the VCO input responds when the current being sourced and sunk by the charge pump is not equal.

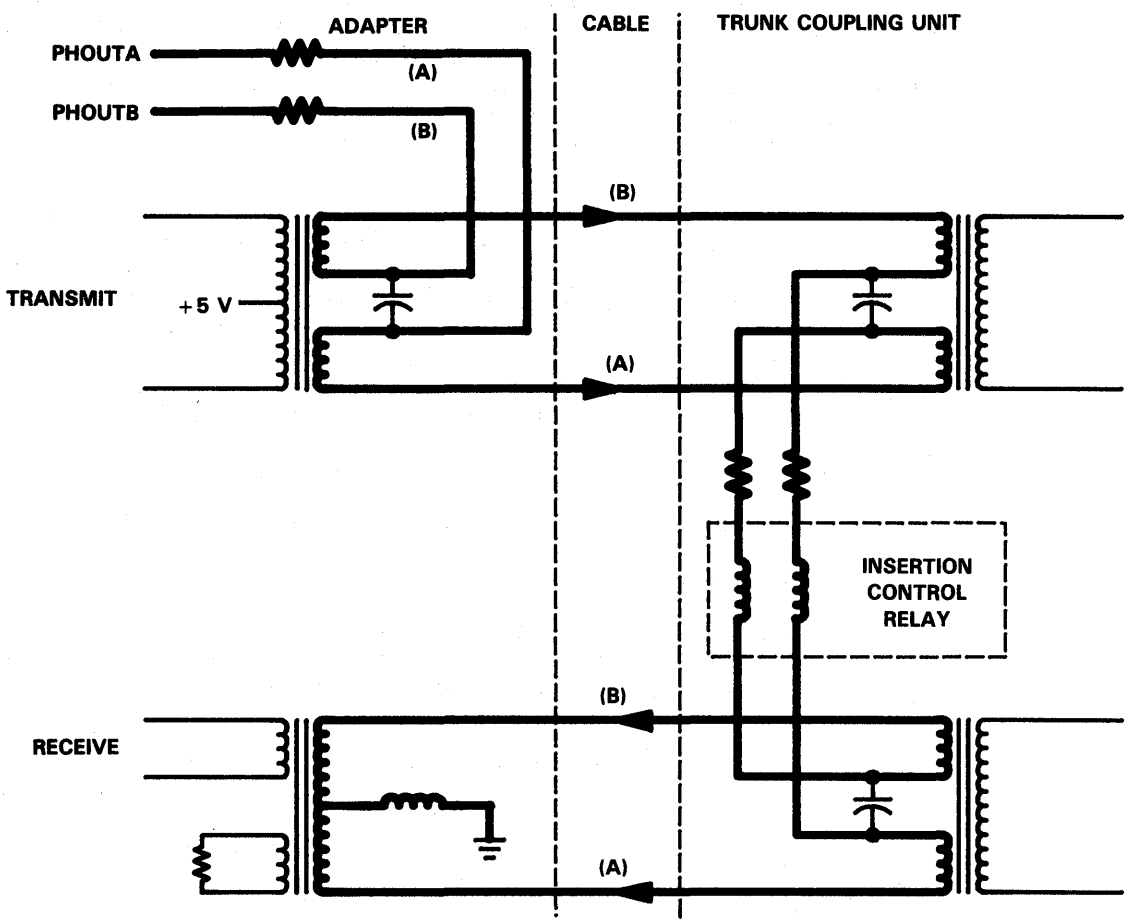


FIGURE 4-76. PHANTOM DRIVE PATH

A wire fault condition is detected by monitoring the current being supplied through the PHOUTA and PHOUTB pins. In the event that an abnormally high or low current, as specified in the TMS38051/TMS38052 Data Sheet, is detected on either phantom drive pin, the $\overline{\text{WFLT}}$ output is asserted.

pin descriptions

NAME	I/O	DESCRIPTION
$\overline{\text{LRESET}}$	I	TMS38010 Reset
LBCLK1, LBCLK2	O	Bus Clocks
$\overline{\text{LBSYNC}}$	I	Bus Synchronization. This pin is reserved and should be left unconnected.
LAL	I/O	Address Latch Enable
$\overline{\text{LEN}}$	I/O	Data Enable
LBRDY	I	Bus Ready. Used to force wait states on bus read/write cycles.
LIRQ0, LIRQ1, LIRQ2	I	Interrupt Request Level Request
$\overline{\text{LNMI}}$	I	Non-Maskable Interrupt (NMI) Request
$\overline{\text{LBRQ1}}$, $\overline{\text{LBRQ2}}$	I	Bus Request 1 and 2. Used by bus masters to request control of the bus.
$\overline{\text{LBGRI}}$, $\overline{\text{LBGR2}}$	O	Bus Grant 1 and 2
LAD0 - LAD15	I/O	Address/Data bus. LAD0 is the most-significant bit and LAD15 is the least-significant bit. LAD15 serves as a "Page Select" during the address phase of memory cycles.
LPH, LPL	I/O	Parity High Byte and Low Byte. Parity for data carried over LAD0-LAD15.
LI/$\overline{\text{D}}$	O	Instruction Fetch/Data Transfer Status Code
LR/$\overline{\text{W}}$	I/O	Read/Write signal
CLKDIV	I	This pin is reserved and should be tied to V_{CC}.
MXTALIN	I	Input to internal oscillator from crystal or external clock
MXTAL2	O	Connection to internal oscillator from crystal
MXTALOUT	O	Crystal Frequency Output. This frequency is MXTALIN/3.
$\overline{\text{TEST}}$, TEST0-TEST2	I	TMS38010 Test Pins. These pins should be left unconnected.
V_{CC}	I	5-V supply pins
V_{SS}	I	Ground pins

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description

The TMS38010 Communications Processor is a member of the TMS380 family of VLSI components which form a highly integrated Adapter used for attaching to a token ring local area network (LAN). The TMS38010 provides a high-performance CPU ideal for processing communications protocols. The TMS38010 provides 63 instructions, a 1408 x 18-bit RAM for communications data buffering and CPU workspace, and a general purpose timer for implementing software protocol timers. The TMS38010's architecture features hardware and software interrupts, memory-based registers for fast response to hardware and software interrupts, and a 333-ns machine cycle time. Bus arbitration is provided internal to the TMS38010 Communications Processor.

The TMS38010 Communications Processor, when coupled with the TMS38020 Protocol Handler, the TMS38030 System Interface, and the TMS38051 and TMS38052 Ring Interface Pair, forms a complete, integrated token ring LAN Adapter fully compatible with the IEEE Std 802.5-1985 Token Ring Access Method and Physical Layer Specifications for token ring networks.

architecture

The architecture of the TMS38010 Communications Processor consists of a 16-bit CPU, a LAN Adapter bus interface, a general purpose timer, control registers, and a 2.75K-byte buffer RAM.

central processing unit

The central processing unit (CPU) of the TMS38010 contains the arithmetic-logic unit (ALU), registers, and control store. This CPU features memory-to-memory architecture which can address up to 256K bytes of memory, logically divided into 128K bytes of data memory and 128K bytes of instruction memory. Using paging techniques, both the instruction and data spaces are paged into two 64K byte regions. This paging is accomplished via a page select output on the LAD15 pin during the address phase of memory cycles. The state of this pin is controlled through the CPU's status register.

arithmetic-logic unit (ALU)

The arithmetic-logic unit of the TMS38010 is 16 bits wide. The ALU performs all arithmetic and logical operations required during instruction execution. The ALU is partitioned into two 8-bit halves to accommodate byte operations. The bus interface only performs 16-bit wide transfers on the LAN Adapter bus, thus, the byte being operated upon may be modified while the unaffected byte is passed through unchanged.

internal registers

The CPU contains three registers used for programming: the Program Counter (PC), the Status Register (ST), and the Workspace Pointer (WP). The Program Counter contains the memory address of the next instruction word. The Status Register contains bits which signify the results of program comparisons, indicate program status conditions, and supply the interrupt mask to the interrupt priority circuits. The Workspace Pointer contains a memory address which defines the first word of a block of 16 words which define the Workspace Registers. These workspace registers are memory-resident working registers and are used as scratch and index registers similar to the internal registers of register-based architectures. By changing the value of the Workspace Pointer (as may occur when an interrupt occurs), a new set of registers is defined for efficient program context switches.

interrupts

Interrupts are presented to the TMS38010 via the LIRQ0, LIRQ1, and LIRQ2 interrupt request pins. These pins, when any one is active low for an entire LBCLK cycle, cause an interrupt request to be posted to the TMS38010's CPU. LIRQ0 (the most-significant bit) through LIRQ2 (the least-significant bit) present an interrupt level of one (all low) through level seven. When LIRQ0 through LIRQ2 are all high, no interrupt is requested. The prioritization of interrupts is done external to the TMS38010. In the TMS380 LAN Adapter, this function is performed by the TMS38030 System Interface.

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control registers

In addition to the GPTLATCH and GPTDATA register, the TMS38010 Communications Processor contains two additional 16-bit registers: the CP Control (CPCTL) register and the CP Status (CPSTS) register. These 16-bit registers are used by the CPU as follows: 1) to control the operation of the general purpose timer, 2) to test the parity of the LAN Adapter bus, and 3) to store status information with respect to the CPU. These registers are shown in Figure 1.

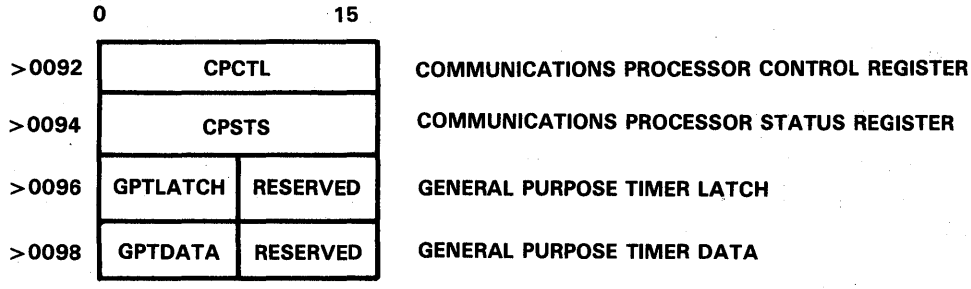

FIGURE 1. TMS38010 CONTROL REGISTERS

CPCTL register

The CPCTL register controls the general purpose timer and the LAN Adapter bus parity checker/generator. Four bits are defined; the remaining bits are reserved. These bits are defined in Table 1.

TABLE 1. CONTROL REGISTER BIT FUNCTIONS

BIT	NAME	DESCRIPTION
0	LPIEN	Local Parity Interrupt Enable
1	LPTST	Local Parity Test
2	GPTIEN	General Purpose Timer Interrupt Enable
3	GPTSTART	General Purpose Timer Start
4	RFLAG	Reset Flag. Cleared upon hardware reset.

CPSTS register

The CPSTS register provides additional status for the CPU, the status of the parity checkers, and the status of the general purpose timer. The bits of the CPSTS register are shown in Table 2.

TABLE 2. CPSTS REGISTER BIT VALUES

BIT	NAME	DESCRIPTION
0	ILLOP	Illegal Operation Interrupt Request
1	AFI	Arithmetic Fault Indicator
2	LPE	Local Parity Error
3	GPTINT	General Purpose Timer Interrupt
4	SWINT	Software Interrupt Indicator
5-11		Reserved
12	TEST0	Test 0 pin value
13	TEST1	Test 1 pin value
14	TEST2	Test 2 pin value
15	CLKDIV	CLKDIV pin value

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CPU instruction set summary (continued)

DUAL-OPERAND INSTRUCTIONS – REGISTER DESTINATION		
MNEMONIC	**MEANING**	**DESCRIPTION**
COC	Compare Ones Corresponding	Test (D) to determine if 1's are in each bit position where 1's are in (SA). If so, set appropriate bits in status register.
CZC	Compare Zeros Corresponding	Test (D) to determine if 0's are in each bit position where 1's are in (SA). If so, set appropriate bits in status register.
XOR	Exclusive OR	(D) XOR (SA) → (D)
MPY	Multiply	Multiply unsigned (D) by unsigned (SA) and place unsigned 32-bit product in D (most significant) and D + 1 (least significant).
DIV	Divide	If unsigned (SA) is less than or equal to (D), perform no operation and set status register bit 4. Otherwise, divide unsigned (D) and (D + 1) by unsigned (SA). Quotient → (D), remainder → (D + 1)
SIGNED MULTIPLY AND DIVIDE		
MNEMONIC	**MEANING**	**DESCRIPTION**
MPYS	Signed Multiply	Multiply signed 2's complement integer in register 0 by signed 2's complement integer in (SA) and place signed 32-bit product in register 0 (most significant) and register 1 (least significant).
DIVS	Signed Divide	If the quotient cannot be expressed as a signed 16-bit quantity (hex 8000 is a valid negative number), set the appropriate status register bits, otherwise, divide the signed 2's complement integer in register 0 and register 1 by the signed 2's complement integer at SA and place the signed quotient in register 0 and the signed remainder in register 1. The sign of the quotient is determined by algebraic rules. The sign of the remainder is the same as the sign of the dividend, and |REMAINDER| < |DIV|.
EXTENDED OPERATION		
MNEMONIC	**MEANING**	**DESCRIPTION**
XOP	Extended Operation	Performs a context switch. The address of the trap vector is calculated by (>0040 + 4 × D).
SINGLE-OPERAND INSTRUCTIONS		
MNEMONIC	**MEANING**	**DESCRIPTION**
B	Branch	SA → (PC)
BL	Branch and Link	(PC) → (WR11), SA → (PC)
BLWP	Branch and Load Workspace Pointer	(SA) → (WP), (SA + 2) → (PC), (old WP) → (new WR13), (old PC) → (new WR14), (old ST) → (new WR15). The LIRQ inputs are not tested upon completion of the BLWP instruction.
CLR	Clear	0 → (SA)
SETO	Set to Ones	FFFF → (SA)
INV	Invert	(SA) inverted → (SA)
NEG	Negate	− (SA) → (SA)
ABS	Absolute Value	|(SA)| → (SA)
SWPB	Swap bytes	Bits 0-7 of (SA) → bits 8-15 of (SA); bits 8-15 of (SA) → bits 0-7 of (SA)
INC	Increment	(SA) + 1 → (SA)
INCT	Increment by 2	(SA) + 2 → (SA)
DEC	Decrement	(SA) − 1 → (SA)
DECT	Decrement by 2	(SA) − 2 → (SA)
X	Execute	Execute instruction at SA

TERMS USED IN INSTRUCTION SUMMARY TABLES

TERM	DEFINITIONS
SA	Source Address
DA	Destination Address
W	Workspace Register
a → b	a is transferred to b
|n|	Absolute value of n
ST	Status Register
STn	Bit n of Status Register
PC	Program Counter
(SA)	Contents of source address
(DA)	Contents of destination address
(W)	Contents of workspace register
WP	Workspace Pointer
IOP	Immediate operand
LSB	Least-significant bit (byte)
MSB	Most-significant bit (byte)
WRn	Workspace Register n

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage range . . . . . −0.3 V to 20 V
Output voltage range . . . . . −2 V to 7 V
Operating free-air temperature range (see Note 2) . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES 1. Voltage values are with respect to V_{SS}.
2. Devices are tested in an environment in excess of 70°C to guarantee operation at 70°C. Case temperatures should be maintained at or below 90°C.

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electrical characteristics over full range of recommended operating conditions (unless otherwise noted) (concluded)

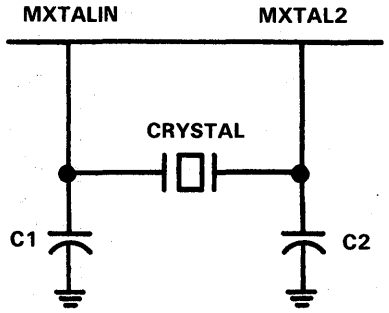
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL}	Low-level input current	$\overline{LEN}$, TESTO-TEST2, $\overline{TEST}$, $\overline{LBSYNC}$ (Notes 5 and 6)	V_I = 0.45 V			−700	μA
		All other inputs				−20	μA
I_{IH}	High-level input current		$V_I = V_{CC}$			20	μA
I_{CC}	Supply Current		V_{CC} = 5 V, T_A = 25° C		150		mA
			V_{CC} = 5.5 V, T_A = 0° C			305	mA
			V_{CC} = 5.5 V, T_C = 90°C			240	mA
C_I	Input capacitance	All inputs	f = 1 MHz, all other inputs at 0 V			15	pF

NOTES: 5. $\overline{LEN}$, TESTO-TEST2, and $\overline{LBSYNC}$ have internal pullups. They may be left unconnected, in which case they function as being high.
6. $\overline{LBSYNC}$ and $\overline{TEST}$ should be left unconnected.

CLOCK REQUIREMENTS AND TIMING

internal clock option

The internal oscillator is enabled by connecting a parallel-resonant crystal across MXTALIN and MXTAL2 (see Figure 2). MXTALOUT is one-third the crystal fundamental frequency. C1 and C2 should be chosen such that C2 is always equal to or greater than C1.



NOTE 7: C1 and C2 represent the total capacitance on these pins including strays and parasitics, but not the input capacitance of the device pins.

FIGURE 2. EXTERNAL CRYSTAL CONNECTIONS

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Crystal frequency, fx	0°C to 70°C		24		MHz
Crystal frequency tolerance				0.006	%
C1, C2		10	15	20	pF

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LAN ADAPTER BUS READ AND WRITE PARAMETERS

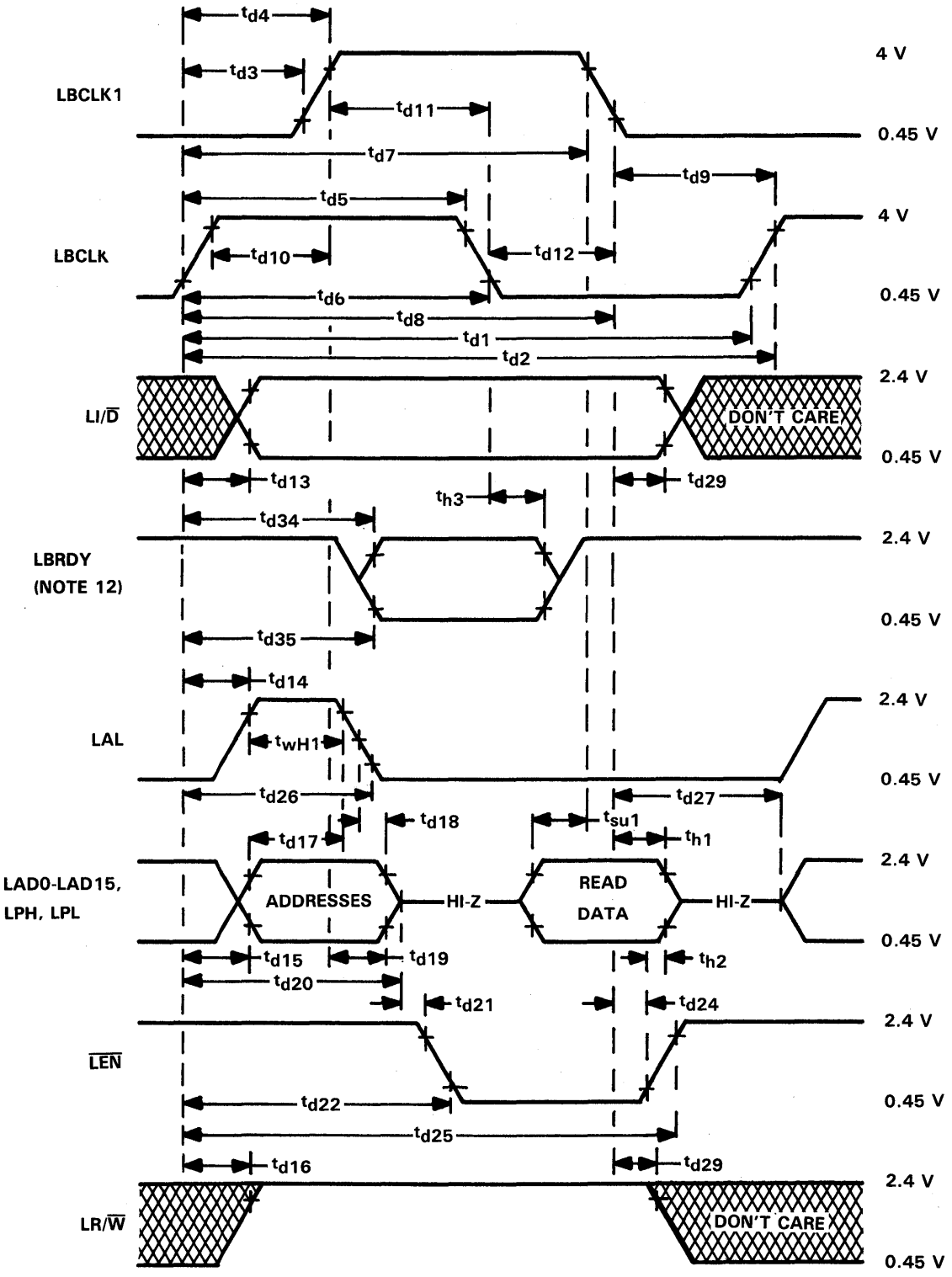
switching characteristics/timing requirements over recommended supply voltage range and operating free-air temperature range (see Figure 3)†

	PARAMETER	MIN	MAX	UNIT
t_{d13}	Delay time, LBCLK2 rise to LI/$\overline{D}$ valid		47	ns
t_{d14}	Delay time, LBCLK2 rise to LAL high		47	
t_{d15}	Delay time, LBCLK2 rise to address valid		47	
t_{d16}	Delay time, LBCLK2 rise to LR/$\overline{W}$ valid		47	
t_{wH1}	Pulse duration, LAL high	Q – 50		
t_{d17}	Delay time, address valid to LAL no longer high	Q – 50		
t_{d18}	Delay time, LAL fall to 1.3 V to address no longer valid	7		
t_{d19}	Delay time, LBCLK1 high to address no longer valid	7		
t_{d20}	Delay time, LBCLK2 rise to LAD, LPH, LPL high impedance in read cycle		Q + 74	
t_{d21}	Delay time, LAD, LPH, LPL high impedance to $\overline{LEN}$ no longer high in read cycle	0		
t_{d22}	Delay time, LBCLK2 rise to $\overline{LEN}$ low in read cycle		Q + 84	
t_{d23}	Delay time, LBCLK2 rise to $\overline{LEN}$ low in write cycle		Q + 47	
t_{d24}	Delay time, LBCLK1 low to $\overline{LEN}$ no longer low in read cycle	0		
t_{d25}	Delay time, LBCLK2 rise to $\overline{LEN}$ high in read cycle		3Q + 47	
t_{d26}	Delay time, LBCLK2 rise to LAL low		2Q – 12	
t_{d27}	Delay time, LBCLK1 low to LAD, LPH, LPL no longer high impedance in next cycle	80		
t_{d28}	Delay time, LBCLK2 rise to write data valid		3Q – 70	
t_{d29}	Delay time, LBCLK1 low to LI/$\overline{D}$, LR/$\overline{W}$ no longer valid	20		
t_{d30}	Delay time, LBCLK1 low to write data no longer valid	20		
t_{d31}	Delay time, LBCLK1 low to $\overline{LEN}$ no longer low in write cycle	20		
t_{d32}	Delay time, LBCLK1 low to $\overline{LEN}$ high in write cycle		80	
t_{d33}	Delay time, LBCLK2 rise to $\overline{LEN}$ no longer high in write cycle	Q – 4		
t_{su1}	Setup time, Read data valid to LBCLK1 no longer high	20		
t_{h1}	Hold time, read data valid after LBCLK1 low if t_{h2} not met	15		
t_{h2}	Hold time, read data valid after $\overline{LEN}$ no longer low if t_{h1} not met	0		
t_{d34}	Delay time, LBCLK2 rise to LBRDY high		2Q – 41	
t_{d35}	Delay time, LBCLK2 rise to LBRDY low		2Q – 21	
t_{h3}	Hold time, LBRDY valid after LBCLK2 low	80		

†This table is entitled switching characteristics/timing requirements because several of the parameters specified can be classified as characteristics or requirements depending on the mode of operation: bus slave or bus master. The values given are valid for both modes.

NOTE 9: Q = $0.25t_{c(LA)}$.

LAN Adapter bus read timing



NOTES: 11. The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for the other waveforms are 2 V and 0.8 V. The intermediate reference point for LAL is 1.3 V.
12. LBRDY should be maintained at a high state unless wait states are required.

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LAN ADAPTER BUS ARBITRATION PARAMETERS

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 3)

	PARAMETER	MIN	MAX	UNIT
t_{d36}	Delay time, LBCLK2 rise to $\overline{\text{LBGR1}}$, $\overline{\text{LBGR2}}$ valid		57	ns
t_{d37}	Delay time, LBCLK2 rise to $\overline{\text{LBGR1}}$, $\overline{\text{LBGR2}}$ no longer valid	−6		
t_{d38}	Delay time, LBCLK2 rise to LAL no longer driven low, TMS38010 releases bus	3Q − 15		
t_{d39}	Delay time, LBCLK2 rise to LAL high impedance, TMS38010 releases bus		4Q − 2	
t_{d40}	Delay time, LBCLK2 rise to LAL no longer high impedance, TMS38010 acquires bus	2Q − 9		
t_{d41}	Delay time, LBCLK2 rise to LAL driven low, TMS38010 acquires bus		3Q − 15	
t_{d42}	Delay time, LBCLK2 rise to $\overline{\text{LEN}}$ high impedance, TMS38010 releases bus		74	
t_{d43}	Delay time, LBCLK1 low to $\overline{\text{LEN}}$ no longer high impedance, TMS38010 acquires bus	80		
t_{d44}	Delay time, LBCLK2 rise to $\overline{\text{LEN}}$ driven high, TMS38010 acquires bus		74	
t_{d45}	Delay time, LBCLK1 low to LR/$\overline{\text{W}}$, LI/$\overline{\text{D}}$, LAD0-LAD15, LPH, and LPL high impedance, TMS38010 releases bus		80	
t_{d46}	Delay time, LBCLK1 low to LR/$\overline{\text{W}}$, LI/$\overline{\text{D}}$, LAD0-LAD15, LPH, and LPL no longer high impedance, TMS38010 acquires bus	80		

NOTE 9: Q = 0.25 $t_{c(LA)}$

timing requirements over recommended supply voltage range and operating free-air temperature range

	PARAMETER	MIN	MAX	UNIT
t_{d47}	Delay of $\overline{\text{LBRQ1}}$, $\overline{\text{LBRQ2}}$ from LBCLK1 low		56	ns
t_{h4}	Hold of $\overline{\text{LBRQ1}}$, $\overline{\text{LBRQ2}}$ after LBCLK1 rise	0		

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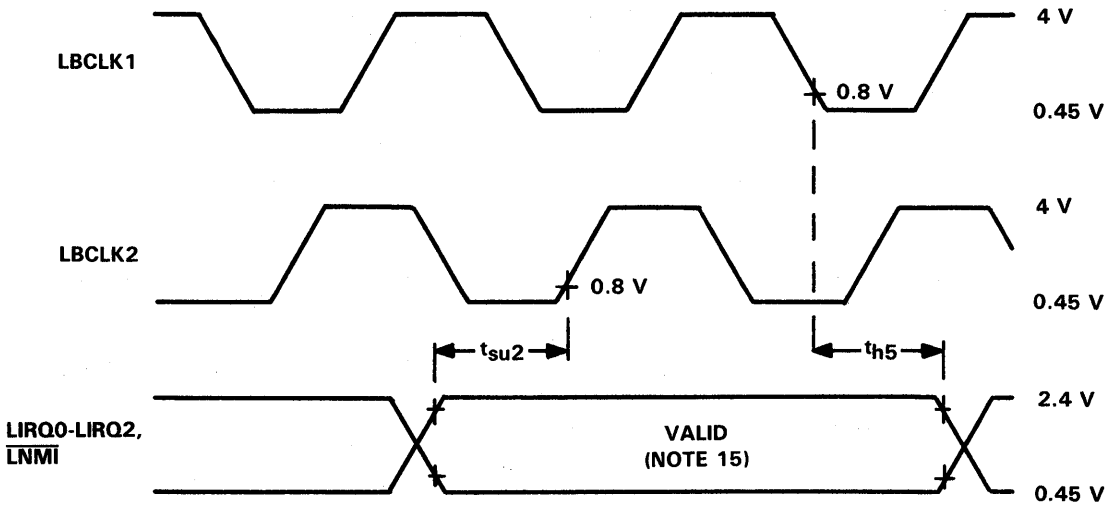
MISCELLANEOUS LAN ADAPTER BUS PARAMETERS

switching characteristics over recommended supply voltage range and operating free-air temperature range

	PARAMETER	MIN	MAX	UNIT
t_{su2}	Setup time, $\overline{LNMI}$ or LIRQ0-LIRQ2 valid prior to LBCLK2 rise to guarantee recognition	40		ns
t_{h5}	Hold time, $\overline{LNMI}$ or LIRQ0-LIRQ2 after LBCLK1 low to guarantee recognition	40		

interrupt timing



NOTES: 14. The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for LIRQ0-LIRQ2 and $\overline{LNMI}$ are 2 V and 0.8 V.

15. Inputs LIRQ0-LIRQ2 should not change state except during the window when LBCLK1 and LBCLK2 are BOTH low. To meet this requirement, a latch, clocked by the falling edge of LBCLK1, should be added between the LIRQOUT0-LIRQOUT2 outputs of the TMS38030 and the LIRQ0-LIRQ2 inputs of the TMS38010.

MISCELLANEOUS TIMING PARAMETERS

switching characteristics over recommended supply voltage range and operating free-air temperature range

	PARAMETER	MIN	MAX	UNIT
t_{d48}	Delay from reading minimum V_{CC} during power-up to valid LBCLK1, LBCLK2 with $\overline{LRESET}$ active		90	ms

timing requirements over recommended supply voltage range and operating free-air temperature range

	PARAMETER	MIN	MAX	UNIT
$t_{w(LRS)}$	$\overline{LRESET}$ pulse duration, asserted with minimum V_{CC} or greater applied, and valid LBCLK1 and LBCLK2	14		μs
$t_{r(LRS)}$	$\overline{LRESET}$ rise time		100	ns
$t_{r(VCC)}$	V_{CC} rise time from 1.2V to V_{CC} minimum	1		ms

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pin descriptions

NAME	I/O	DESCRIPTION
		LAN ADAPTER BUS INTERFACE PINS
LBCLK1, LBCLK2	I	Bus Clocks
$\overline{\text{LAL}}$	I/O	Address Latch Enable
$\overline{\text{LEN}}$	I/O	Data Enable
LBRDY	I/O	Bus Ready
$\overline{\text{PIRQ}}$	O	PH Interrupt Request
$\overline{\text{LBRQP}}$	O	Bus Request
$\overline{\text{LBGRP}}$	I	Bus Grant
LAD0 - LAD15	I/O	Address/Data bus. LAD0 is the most-signiticant bit, LAD15 is the least-significant bit.
LPH,LPL	I/O	Parity High/Parity Low
LI/$\overline{\text{D}}$	I/O	Instruction/Data Bus Status Code
LR/$\overline{\text{W}}$	I/O	Read/Not Write
$\overline{\text{PHRESET}}$	I	Reset
$\overline{\text{PHCS}}$	I	Chip Select
		RING INTERFACE PINS
DRVR	O	Transmitter Data
FRAQ	O	Frequency Acquisition Select
$\overline{\text{NSRT}}$	O	Insert Control
RCLK	I	Recovered Data Clock
RCVR	I	Received Data
$\overline{\text{REDY}}$	I	Ring Interface Ready
$\overline{\text{WFLT}}$	I	Wire Fault Detect
$\overline{\text{WRAP}}$	O	Wrap Select
PXTALIN	I	Ring Frequency Reference Clock
		MISCELLANEOUS PINS
$\overline{\text{PHTEST}}$	I	Module-in-Place Test Mode Select. This pin should be left unconnected.
V_{CC}		5-V supply pins.
V_{SS}		Ground pins.
V_{BB}		Substrate bias. This pin is reserved and should be left unconnected.
NC		Reserved. This pin should be left unconnected.

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description

The TMS38020 Protocol Handler integrates onto a single chip the hardware-based protocol functions for a 4 megabit per second token ring Local Area Network (LAN). An on-chip ROM contains 16K bytes of software used by the TMS38010 Communications Processor for implementation of a complete token ring Adapter function. The TMS38020 provides Differential Manchester encoding and decoding, frame address recognition, and includes state machine functions which capture free tokens, transmit and receive frames, manage the Adapter RAM buffers and provide token transmit and priority controls. Four DMA channels, two for transmit and two for receive, insure high-speed transfer of frames between the Adapter's buffer RAM and the ring. Integrity of transmitted and received data is provided by CRC generation and checking, detection of Differential Manchester code violations, and parity on internal data paths and at the LAN Adapter bus interface.

The TMS38020, when coupled with the TMS38010 Communications Processor, the TMS38030 System Interface, and the TMS38051 and TMS38052 Ring Interface chips, forms a highly integrated token ring LAN Adapter.

architecture

The TMS38020 Protocol Handler contains a bus master interface to the LAN Adapter bus for transfer of frame data between itself and LAN Adapter bus memory, a bus slave interface to the LAN Adapter bus for control by an external CPU, an interface to the Ring Interface circuit, and a 16K-byte ROM. Internal to the TMS38020 are several finite-state machine-implemented functions which provide bit-and frame-level processing of token protocols as well as control the flow of DMA data to and from buffer RAM resident on the LAN Adapter bus. The following paragraphs describe the blocks shown in the functional block diagram.

address compare state machine

The address compare state machine controls the recognition of addresses in a received frame (including stripped frames). A description of frame addressing methodology may be found in the Communications Services Section of the User's Guide.

CRC checker

This block contains a 32-bit feedback shift register for calculation of the cyclic redundancy code of frames received. The TMS38020 calculates the CRC for each frame that the TMS38020 receives. If the calculated CRC does not agree with the CRC value of the received frame, the TMS38020 sets an error indicator bit within the frame to flag the occurrence of the error. If the TMS38020 was copying the frame at the time the CRC error was detected (due to an address match), the TMS38020 notifies the LAN Adapter CPU of the error. Mathematically, the CRC is calculated by considering the checked bytes as a polynomial and dividing it modulo 2 by the following polynomial:

$$G(X) = X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^{8} + X^{7} + X^{5} + X^{4} + X^{2} + X^{1} + 1$$

CRC generator

The cyclic redundancy code (CRC) generator generates the CRC field to be inserted by the TMS38020 when transmitting. The procedure for generating CRC is identical to that described for the CRC checker.

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consists of a 7.5-baud (half-bit times) delay preceding the elastic buffer and a 22.5-baud delay succeeding it. The total delay through the TMS38020 when the Active Monitor mode is selected is 4-baud normal delay plus 19-baud for the priority delay plus 30-baud for the monitor delay plus 6-baud average elastic buffer delay. This delay totals 59 ± 6 baud.

monitor state machine

The monitor state machine controls the setting of the Monitor Count bit of busy or priority tokens which are repeated on the ring and the detection of token activity on the ring. This state machine is active when the TMS38020 is configured as an Active Monitor [MON bit of Ring Command 1 Register (RINGCMD1) is set].

priority delay and state machine

The TMS38020 provides control of seven levels of token priority. The priority state machine is responsible for controlling the token priority as defined by the protocol. The priority delay of 19 half-bit times is inserted when a station releases a token to allow the station to modify the token according to the priority protocol.

receive buffer manager

The receive buffer manager controls the receive buffer chaining operations on the LAN Adapter bus.

receive data manager

The receive data manager requests and acknowledges LAN Adapter bus cycles for DMA to write the received frame into memory on the LAN Adapter bus.

receive deserializer

The receive deserializer block is a 16-bit serial-in parallel-out shift register. The input is the sampled data from the ring. A serial parity generator unit calculates the parity for each eight bits shifted in and stores this parity with the parallel data. The 18 bits of data and parity are then loaded in parallel into the receive FIFO buffer.

receive DMA registers

The receive DMA registers are indicated in the functional block diagram by the names RCP, RTP, RADDR0, RADDR1, RLEN0, and RLEN1. These registers are managed by the receive buffer manager. Only the register RCP (receive chain pointer) may be accessed by external LAN Adapter bus masters. The remaining registers are not accessible by external bus masters. A brief description of these registers follows.

receive chain pointer (RCP)

This register contains the address of the buffer currently being filled with data from the ring.

receive temporary pointer (RTP)

The receive temporary pointer register contains the starting address of the buffer into which the receive DMA channel will store data when the buffer being used is full.

channel address registers (RADDR0, RADDR1)

The TMS38020 maintains two DMA channels for receive operations. The channel address register for both receive DMA channels contains the LAN Adapter bus address of the word being accessed by that channel.

channel length registers (RLEN0, RLEN1)

The channel length register for each of the two receive DMA channels contains the number of empty bytes left in the buffer currently being filled by that channel.

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transmit multiplexer

The transmit multiplexer selects either the CRC generator or transmit serializer output onto the transmit data path.

transmit parity checker

The transmit parity checker checks the parity of data transferred from the top of the transmit FIFO to the transmit serializer. It performs the final check of data before it is placed in the serializer.

transmit serializer

The transmit serializer is a 16-bit parallel-in, serial-out shift register. The shift register is loaded from the data at the top of the transmit FIFO, from the concatenation of the Start Delimiter (SDEL) and the fire token register (FTOK) or from a concatenation of the End Delimiter (EDEL) and the frame status (FS) register.

transmit timer

The TMS38020 contains a physical trailer timer (PTT). This timer provides a watchdog timer function for halting the frame strip process after transmitting a frame.

command and status registers

The command and status registers of the TMS38020 are registers which may be read/written through memory-mapped I/O by an external bus master on the LAN Adapter bus. These registers are mapped to LAN Adapter bus addresses as shown in Table 1.

ADDRESS	BITS		DESCRIPTION
	0 7	8 15	
>0100	RINGCMD0		RING COMMAND 0
>0102	RINGCMD1		RING COMMAND 1
>0104	RINGSTS		RING STATUS
>0106	INTSTAT		INTERRUPT STATUS
>0108	00†	PTTLATCH	PHYSICAL TRAILER TIMER LATCH
>010A	RCP		RECEIVE CHAIN POINTER
>010C	TCP		TRANSMIT CHAIN POINTER
>010E	FTOK	00‡	FIRE TOKEN

†Most-significant bits are reserved.
‡Least-significant bits are reserved.

FIGURE 1. TMS38020 COMMAND AND STATUS REGISTERS

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TABLE 3. RECEIVE OPTION BIT DECODE

ROPT0	ROPT1	DESCRIPTION
0	0	Copy frame if address match
0	1	Copy if MAC frame and address match
1	1	Copy all frames; set ARI and FCI only if address match.
1	0	Reserved. Must not be used.

ring status register (RINGSTS)

The RINGSTS register provides general ring status information, including ring interface status, error logging, and token validation. The bits of RINGSTS are defined in Table 4.

TABLE 4. RING STATUS (RINGSTS) REGISTER BIT FUNCTIONS

BIT	NAME	DESCRIPTION
0	NGO	Not Go (Signal Loss)
1	GTDET	Good Token Detect
2	ATDET	Any Token Detect
3	WFAULT	Wire Fault
4	EBOUF	Elastic Buffer Over/Under Flow
5-9		Reserved
10	MAC0	MAC Attention Code Bit 0
11	MAC1	MAC Attention Code Bit 1
12	MAC2	MAC Attention Code Bit 2
13	MAC3	MAC Attention Code Bit 3
14	RIDER0	FS Rider Control Bit 0
15	RIDER1	FS Rider Control Bit 2

interrupt status (INTSTAT)

The INSTAT register contains information concerning TMS38020 interrupts. This register provides interrupt vectoring, masking, and prioritization. The bits of INSTAT are defined in Table 5. Table 6 lists the decode for bits 11 through 14 (INTCODE0 through INTCODE3).

TABLE 5. INTERRUPT STATUS (INTSTAT) REGISTER BIT FUNCTIONS

BIT	NAME	DESCRIPTION
0	MIE	Master Interrupt Enable
1		Reserved
2	EORBE	End of Receive Buffer Interrupt Enable
3	EOTBE	End of Transmit Buffer Interrupt Enable
4	SLIE	Signal Loss Interrupt Enable
5-7		Reserved
8	ID0	Interrupt Source ID Bit 0
9	ID1	Interrupt Source ID Bit 1
10	ID2	Interrupt Source ID Bit 2
11	INTCODE0	Interrupt Code Bit 0
12	INTCODE1	Interrupt Code Bit 1
13	INTCODE2	Interrupt Code Bit 2
14	INTCODE3	Interrupt Code Bit 3
15	"0"	Always zero

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ADDRESS	NAME	DESCRIPTION
>0110	SAH	LOCAL SPECIFIC ADDRESS BITS 0-15
>0112	SAM	LOCAL SPECIFIC ADDRESS BITS 16-31
>0114	SAL	LOCAL SPECIFIC ADDRESS BITS 32-47
>0116		RESERVED. ALWAYS READ AS ZERO.
>0118	STRIPHI	STRIP ADDRESS BITS 16-31
>011A	STRIPLO	STRIP ADDRESS BITS 32-47
>011C	GNAHI	LOCAL GROUP ADDRESS BITS 0-15
>011E	GNALO	LOCAL GROUP ADDRESS BITS 16-31
>0120	>0000	RESERVED†
>0122	>0000	RESERVED†
>0124	>0000	RESERVED†
>0126	>0000	RESERVED†
>0128	>0000	RESERVED†
>012A	>0000	RESERVED†
>012C	FNAHI	FUNCTIONAL ADDRESS BITS 0-15
>012E	FNALO	FUNCTIONAL ADDRESS BITS 16-31

†These registers must be initialized to zero following power up.

FIGURE 2. ADDRESS COMPARE REGISTERS

buffer management

The TMS38020's buffer managers move frame data in and out of buffer RAM, located on the LAN Adapter bus, through one or more singly-linked buffers. These buffers are aligned on 8-byte boundaries and have the organization for transmit and receive as shown in Figure 3.

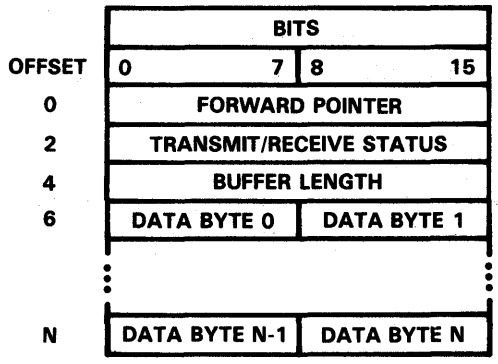

FIGURE 3. BUFFER ORGANIZATION

The forward pointer contains the address of the next buffer in a chain. The transmit/receive status field is used to report frame status. The length field contains the number of bytes in the data field of the buffer. This field is initialized by the LAN Adapter bus CPU.

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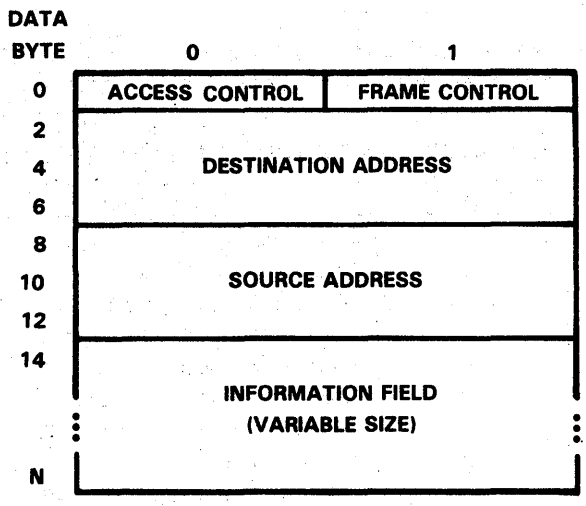

FIGURE 4. TRANSMIT DATA FORMAT

receive buffers

When the buffer organization shown in Figure 3 is used for receive frames, the status field has the bit functions shown in Table 9 in the last buffer in a chain used to receive the frame.

TABLE 9. RECEIVE STATUS FIELD BIT FUNCTIONS

BIT	NAME	FUNCTION
0	INUSE	In Use
1	LFED	Local Frame Error Detect
2	REDI	Received Error Detected Indicator
3	RCC0	Receive Completion Code Bit 0
4	RCC1	Receive Completion Code Bit 1
5	RCC2	Receive Completion Code Bit 2
6	RCC3	Receive Completion Code Bit 3
7	EOF	End of Frame Indicator
8	FS0	Receive Frame Status Bit 0
9	FS1	Receive Frame Status Bit 1
10	FS2	Receive Frame Status Bit 2
11	FS3	Receive Frame Status Bit 3
12	FS4	Receive Frame Status Bit 4
13	FS5	Receive Frame Status Bit 5
14		Reserved
15		Reserved

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TMS38020 ROM

The TMS38020 contains a 16K-byte ROM organized as 8K x 18 bits. Each byte contains an odd parity bit. The ROM is not used by internal TMS38020 logic but is accessed by the LAN Adapter bus CPU for program storage. This ROM contains object code for the TMS38010 Communications Processor. This ROM contains software which provides media access protocols compatible with IEEE Std 802.5-1985, protocol services for network management servers, and diagnostics which verify proper functionality of the TMS380 Token Ring Adapter.

Access to this ROM from the TMS38010 Communications Processor is in one or two LAN Adapter bus read cycles. A prefetch unit reads the word sequentially following the last word read so that sequential accesses occur with no wait states forced on the TMS38010. When access is nonsequential, the TMS38020 deasserts LBRDY in the first cycle to force the CPU to accept a wait state. On the second cycle, the TMS38020 asserts LBRDY and places the ROM data on the bus.

For testing purposes, the TMS38020 ROM should not be accessed for more than eight consecutive read cycles to successive (sequential) locations unless an intervening non-read cycle (one LBCLK cycle) or a non-sequential read cycle is performed.

When the TMS38020 is a bus slave, it will also respond if external circuitry deasserts LBRDY; it will continuously drive its output data (on reads) or delay modifying its internal register (on writes) until LBRDY is asserted high.

address decoding

The TMS38020 performs decoding of LAN Adapter bus addresses as shown in Table 12. Note that not all addresses are strictly decoded. For example, the TMS38020 does not decode address line A1 for ROM accesses at >C000. Thus, a memory read at address location >8000 is identical to an address read at location >C000. For this reason, expansion RAM on the LAN Adapter bus should negate $\overline{\text{PHCS}}$ whenever expansion RAM overlays memory addresses >8000 through >BFFF.

TABLE 12. TMS38020 ADDRESS DECODING

$\overline{\text{PHCS}}$	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	SELECTED TMS38020 LOCATION
H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	TMS38020 not selected
L	L	L	L	L	L	L	L	L	X	X	X	X	X	X	X	TMS38020 not selected
L	L	L	L	L	L	L	L	H	X	X	L	L	Int'l Decode			Command/Status Registers
L	L	L	L	L	L	L	L	H	X	X	L	H	Int'l Decode			Address Compare Registers
L	L	L	L	L	L	L	L	H	X	X	H	L	Int'l Decode			Compare Address Registers
L	L	L	L	L	L	L	L	H	X	X	H	H	Int'l Decode			Internal Test Registers
L	L	X	X	X	X	X	H	X	X	X	X	X	X	X	X	TMS38020 not selected
L	L	X	X	X	X	H	X	X	X	X	X	X	X	X	X	TMS38020 not selected
L	L	X	X	X	H	X	X	X	X	X	X	X	X	X	X	TMS38020 not selected
L	L	X	X	H	X	X	X	X	X	X	X	X	X	X	X	TMS38020 not selected
L	L	X	H	X	X	X	X	X	X	X	X	X	X	X	X	TMS38020 not selected
L	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	TMS38020 not selected
L	H	X	◄					Internal Decode							►	TMS38020 ROM

test mode

The TMS38020 features a module-in-place test mode for board-level testing with the TMS38020 in-circuit. This facilitates testing by bed-of-nails testers. This test mode is enabled by tying the $\overline{\text{PHTEST}}$ pin (pin 41) to ground and supplying clock inputs LBCLK1 and LBCLK2 per the timing requirements specification. This has the effect of driving all outputs of the TMS38020 to a high-impedance state. When not used for testing purposes, this pin should be left unconnected. An internal pullup drives this pin high when not externally connected.

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electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	All outputs	V_{CC} = 4.75 V, I_{OH} = 0.15 mA	2.4			V
V_{OL}	Low-level output voltage	All outputs	V_{CC} = 4.75 V, I_{OL} = Max			0.45	V
I_{OH}	High-level output current	All outputs	V_{CC} = 4.75 V, V_{OH} = 2.4 V			0.15	mA
I_{OL}	Low-level output current	DRVR	V_{CC} = 4.75 V, V_{OL} = 0.45 V			−1.2	mA
		LBRDY				−2.4	mA
		All other outputs				−1.7	mA
I_{OZL}	Off-state (high-impedance state) output current with low-level voltage applied, outputs only		V_O = 0.45 V			−50	μA
I_{OZH}	Off-state (high-impedance state) output current with high-level voltage applied, outputs only		V_O = 2.4 V			50	μA
I_{IL}	Low-level input current	$\overline{PHTEST}$ (Note 4)	V_I = V_{SS}, V_{CC} at 4.75 V−5.25 V			−700	μA
		All other inputs				−20	μA
I_{IH}	High-level input current	All inputs except $\overline{PHTEST}$ (Note 5)	V_{CC} at 4.75 V−5.25 V			20	μA
I_{CC}	Supply current		V_{CC} = 5 V, T_A = 25°C		110		mA
			V_{CC} = 5.25 V, T_A = 0°C			175	mA
			V_{CC} = 5.25 V, T_C = 80°C			125	mA
C_I	Input capacitance	LBCLK1, LBCLK2	f = 1 MHz, all other inputs at 0 V			20	pF
		RCVR, RCLK				10	pF
		All other inputs				15	pF

NOTES: 4. $\overline{PHTEST}$ has an internal pullup resistor implemented. It may be left unconnected; in this case it is interpreted as high.
5. I_{IH} for $\overline{PHTEST}$ is not specified because it will never be driven.

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LAN ADAPTER BUS READ AND WRITE PARAMETERS

timing requirements/switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 6)

	PARAMETER	MIN	MAX	UNIT
t_{d13}	Delay time, LBCLK2 rise to LI/$\overline{D}$ valid		47	ns
t_{d14}	Delay time, LBCLK2 rise to LAL high		47	
t_{d15}	Delay time, LBCLK2 rise to address valid		47	
t_{d16}	Delay time, LBCLK2 rise to LR/$\overline{W}$ valid		47	
t_{wH1}	Pulse duration, LAL high	Q−50		
t_{d17}	Delay time, address valid to LAL no longer high	Q−50		
t_{d18}	Delay time, LAL fall to 1.3 V to address no longer valid	7		
t_{d19}	Delay time, LBCLK1 high to address no longer valid	7		
t_{d20}	Delay time, LBCLK2 rise to LAD, LPH, LPL high impedance in read cycle		Q+74	
t_{d21}	Delay time, LAD, LPH, LPL high impedance to $\overline{LEN}$ no longer high in read cycle	0		
t_{d22}	Delay time, LBCLK2 rise to $\overline{LEN}$ low in read cycle		Q+84	
t_{d23}	Delay time, LBCLK2 rise to $\overline{LEN}$ low in write cycle		Q+47	
t_{d24}	Delay time, LBCLK1 low to $\overline{LEN}$ no longer low in read cycle	0		
t_{d25}	Delay time, LBCLK2 rise to $\overline{LEN}$ high in read cycle		3Q+47	
t_{d26}	Delay time, LBCLK2 rise to LAL low		2Q−12	
t_{d27}	Delay time, LBCLK1 low to LAD, LPH, LPL no longer high impedance in next cycle	80		
t_{d28}	Delay time, LBCLK2 rise to write data valid		3Q−70	
t_{d29}	Delay time, LBCLK1 low to LI/$\overline{D}$, LR/$\overline{W}$ no longer valid	20		
t_{d30}	Delay time, LBCLK1 low to write data no longer valid	20		
t_{d31}	Delay time, LBCLK1 low to $\overline{LEN}$ no longer low in write cycle	20		
t_{d32}	Delay time, LBCLK1 low to $\overline{LEN}$ high in write cycle		80	
t_{d33}	Delay time, LBCLK2 rise to $\overline{LEN}$ no longer high in write cycle	Q−4		
t_{su1}	Setup time, read data valid to LBCLK1 no longer high	20		
t_{h1}	Hold time, read data valid after LBCLK1 low if t_{h2} not met	15		
t_{h2}	Hold time, read data valid after $\overline{LEN}$ no longer low if t_{h1} not met	0		
t_{d34}	Delay time, LBCLK2 rise to LBRDY high		2Q−41	
t_{d35}	Delay time, LBCLK2 rise to LBRDY low		2Q−21	
t_{h3}	Hold time, LBRDY valid after LBCLK2 low	80		

†This table is entitled switching characteristics/timing requirements because several of the parameters specified can be classified as characteristics or requirements depending on the mode of operation: bus slave or bus master (DMA). The values given are valid for both modes.

NOTE 7: Q = $0.25t_c$(LA).

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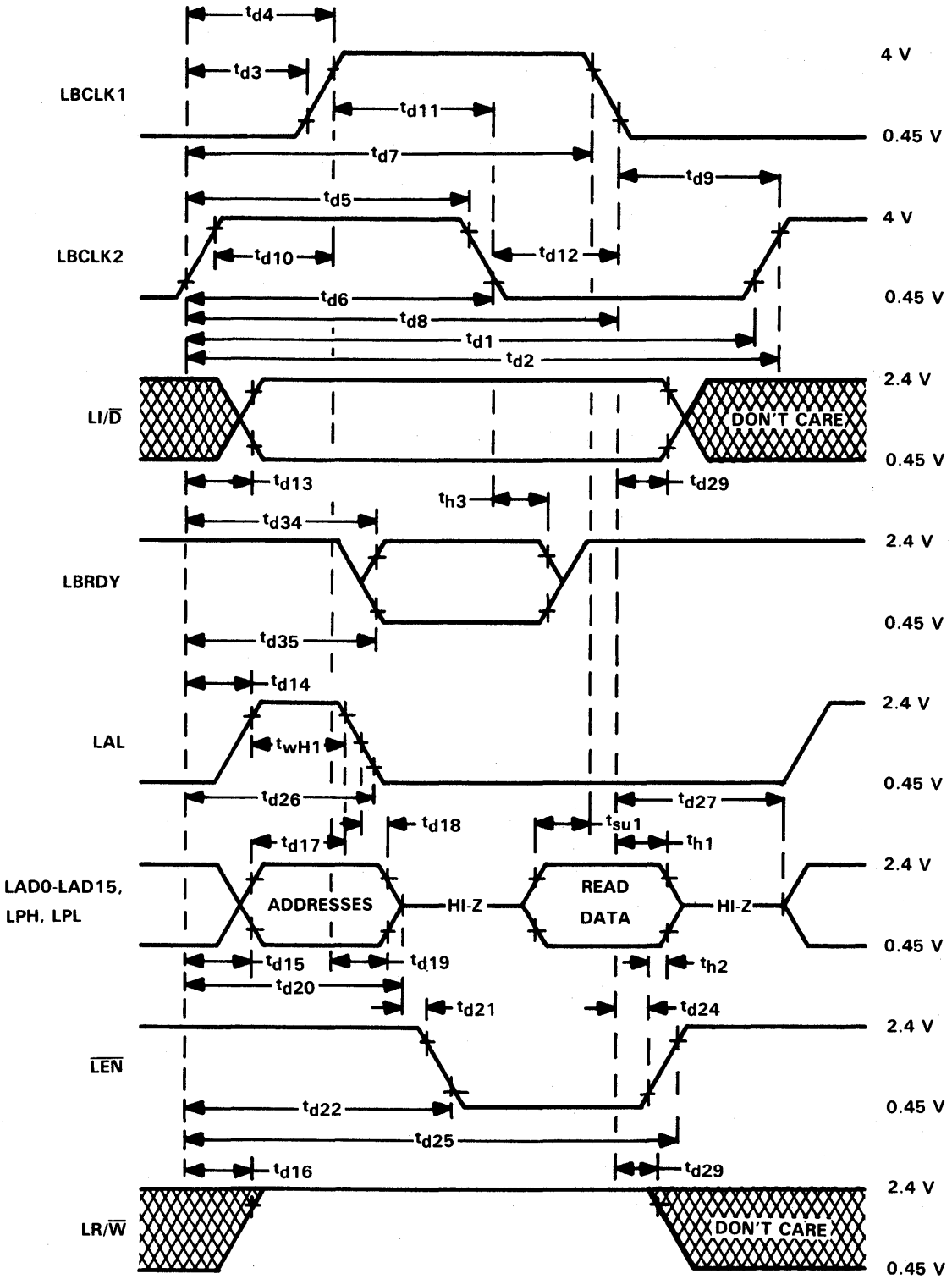
LAN Adapter bus read timing



NOTE 9: The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for the other waveforms are 2 V and 0.8 V. The intermediate reference point for LAL is 1.3 V.

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LAN ADAPTER BUS ARBITRATION PARAMETERS

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 6)

	PARAMETER	MIN	MAX	UNIT
t_{d36}	Delay of $\overline{\text{LBRQP}}$ from LBCLK1 low		48	ns
t_{d37}	Delay of $\overline{\text{LBRQP}}$ after LBCLK1 high	0		
t_{d38}	Delay time, LBCLK2 rise to LAL no longer high impedance by TMS38020	2Q – 9		
t_{d39}	Delay time, LBCLK2 rise to LAL driven low by TMS38020		3Q – 15	
t_{d40}	Delay time, LBCLK1 low to $\overline{\text{LEN}}$ no longer high impedance by TMS38020	80		
t_{d41}	Delay time, LBCLK2 rise to $\overline{\text{LEN}}$ driven high by TMS38020		74	
t_{d42}	Delay time, LBCLK1 low to LR/$\overline{\text{W}}$, LI/$\overline{\text{D}}$, LAD0-LAD15, LPH, and LPL no longer high impedance by TMS38020	80		

NOTE 7: Q = 0.25 $t_{c(LA)}$.

timing requirements over recommended supply voltage range and operating free-air temperature range

	PARAMETER	MIN	MAX	UNIT
t_{d43}	Delay time, LBCLK2 rise to $\overline{\text{LBGRP}}$ valid		2Q – 73	ns
t_{d44}	Delay time, LBCLK2 rise to $\overline{\text{LBGRP}}$ no longer valid	– 6		
t_{d45}	Delay time, LBCLK2 rise to LAL no longer driven low from old bus master	3Q – 15		
t_{d46}	Delay time, LBCLK2 rise to LAL high impedance from old bus master		4Q – 2	
t_{d47}	Delay time, LBCLK2 rise to $\overline{\text{LEN}}$ high impedance from old bus master		74	
t_{d48}	Delay time, LBCLK1 low to LR/$\overline{\text{W}}$, LI/$\overline{\text{D}}$ LAD0-LAD15, LPH, and LPL high impedance from old bus master		80	

NOTE 7: Q = 0.25 $t_{c(LA)}$.

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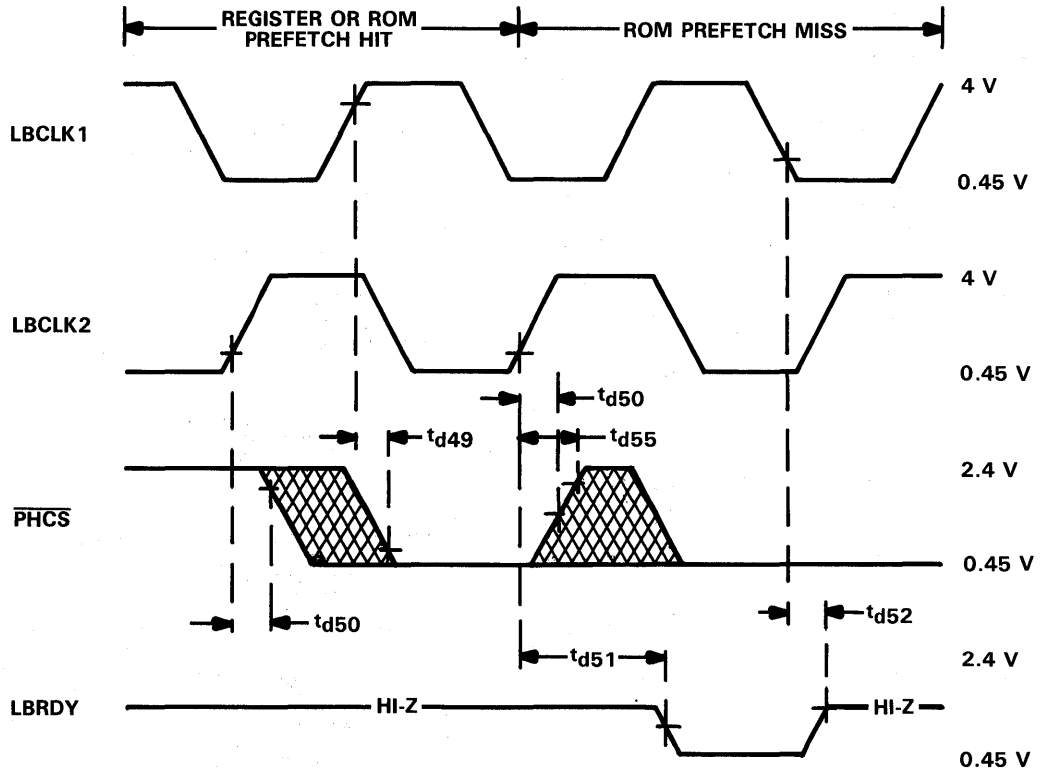
MISCELLANEOUS LAN ADAPTER BUS PARAMETERS

timing requirements over recommended supply voltage range and operating free-air temperature range

	PARAMETER	MIN	MAX	UNIT
t_{d49}	Delay time, LBCLK1 high to $\overline{PHCS}$ low		10	ns
t_{d50}	Delay time, LBCLK2 rise to $\overline{PHCS}$ no longer valid	0		
t_{d51}	Delay time, LBCLK2 rise to LBRDY driven low in ROM prefetch miss		145	
t_{d52}	Delay time, LBCLK1 low to LBRDY high impedance after ROM prefetch miss		45	
t_{d53}	Delay time, LBCLK2 rise to $\overline{PIRQ}$ valid		60	
t_{d54}	Delay time, LBCLK2 rise to $\overline{PIRQ}$ no longer valid	0		
t_{d55}	Delay time, LBCLK2 rise to $\overline{PHCS}$ high		Q-3	

NOTE 7: Q = 0.25 $t_{c(LA)}$.

$\overline{PHCS}$ and LBRDY timing



NOTE 10: The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for the other waveforms are 2 V and 0.8 V.

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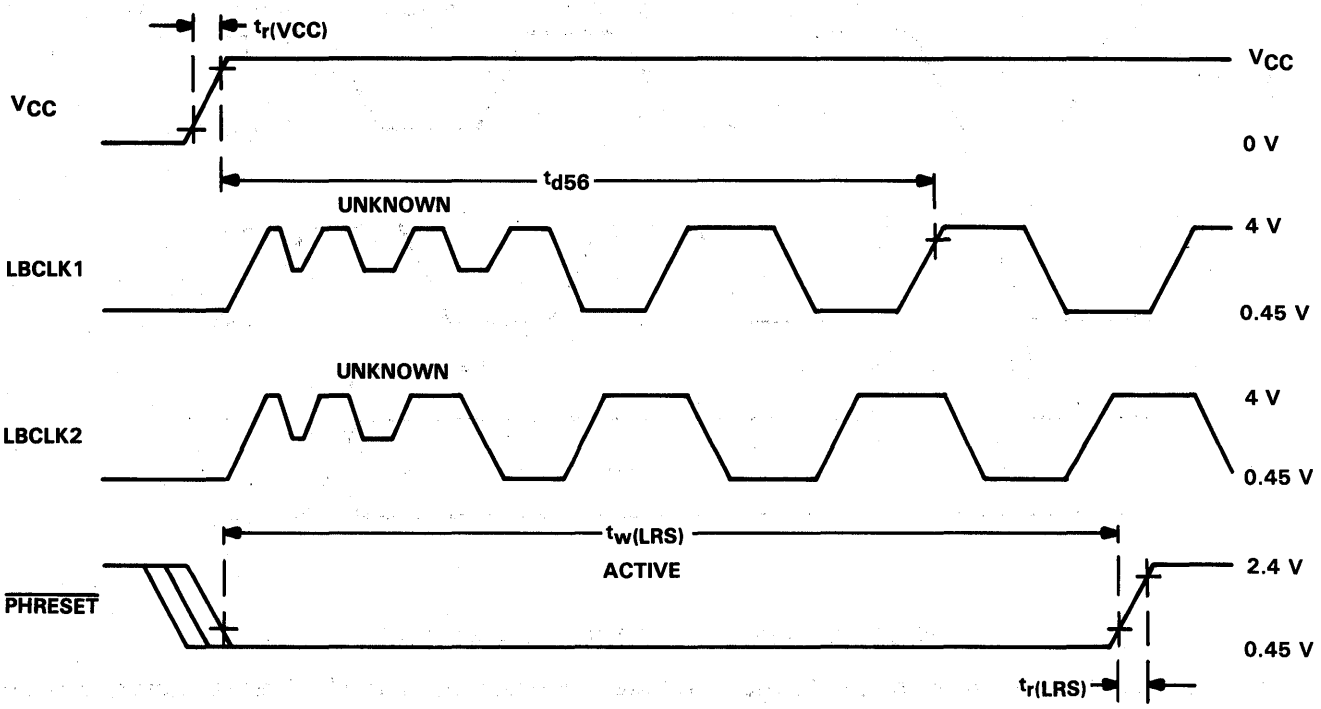
power-up, LBCLK, and $\overline{\text{PHRESET}}$ timing



NOTE 11: The timing reference points for V_{CC} are 4.5 V and 1.2 V. The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for $\overline{\text{PHRESET}}$ are 2 V and 0.8 V.

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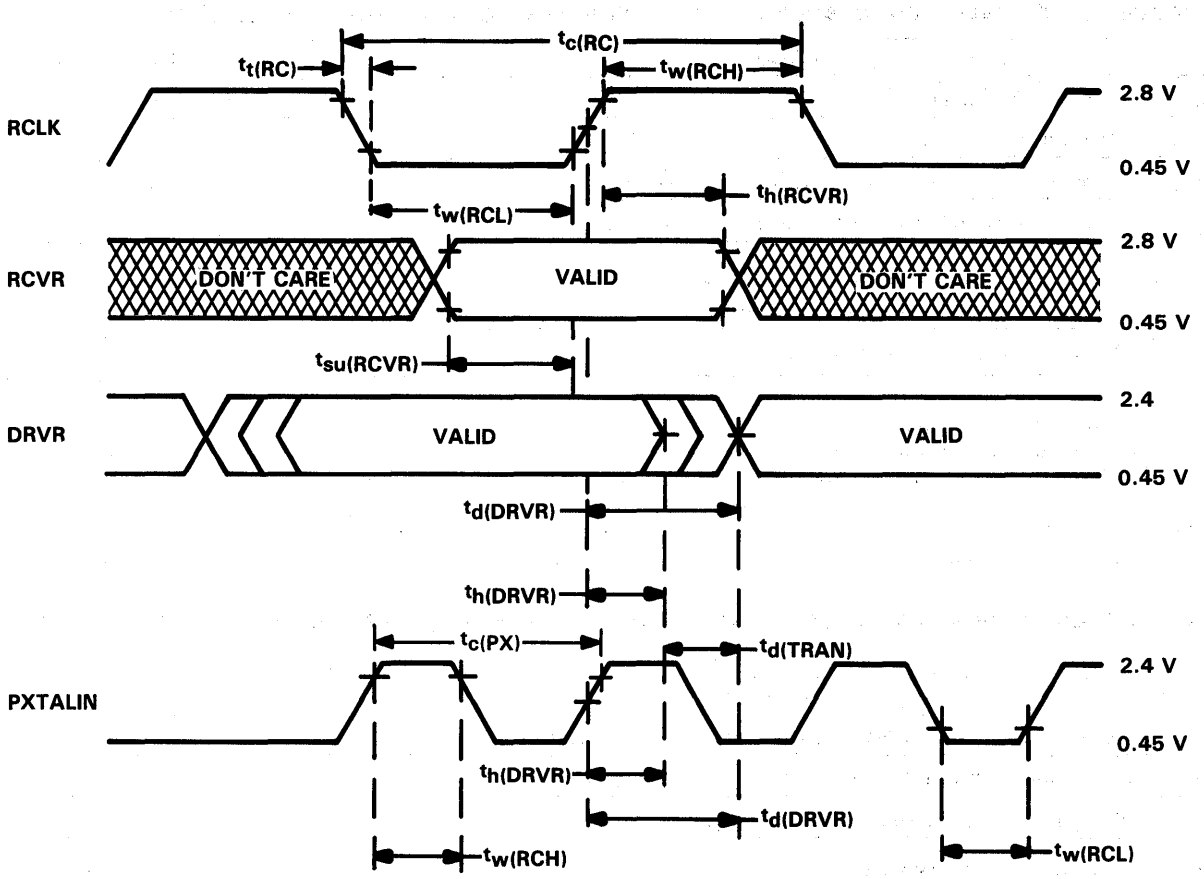
ring interface timing



NOTE 19: The timing reference points for RCVR and RCLK are 2.6 V and 0.6 V. The timing reference points for PXTALIN are 2 V and 0.8 V. The intermediate reference point for RCLK and DRVR is 1.5 V.

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pin descriptions

NAME	PIN	I/O	DESCRIPTION
			SYSTEM BUS ADDRESS/DATA PINS
SADH0	H7	I/O	System address/Data bus — High Byte. SADH0 is the most-significant bit
SADH1	K10	I/O	and SADH7 is the least-significant bit.
SADH2	J8	I/O	
SADH3	J7	I/O	
SADH4	K6	I/O	
SADH5	J6	I/O	
SADH6	K9	I/O	
SADH7	K8	I/O	
SADL0	J5	I/O	System Address/Data bus — Low Byte. SADL0 is the most-significant bit and SADL7
SADL1	H5	I/O	is the least-significant bit.
SADL2	G5	I/O	
SADL3	K4	I/O	
SADL4	F5	I/O	
SADL5	J4	I/O	
SADL6	H4	I/O	
SADL7	K3	I/O	
SPH	K7	I/O	System Parity High Byte
SPL	K5	I/O	System Parity Low Byte
			SYSTEM BUS CONTROL PINS
SI/$\overline{M}$	H8	I	808X/680XX Mode Select
S8/$\overline{16}$	H9	I	8/16-Bit Data Bus Select
$\overline{SRESET}$	H10	I	System Reset
$\overline{SCS}$	J2	I	Chip Select
SRS0	K2	I	Register Select 0 (MSB)
SRS1	H3	I	Register Select 1
SRS2	G4	I	Register Select 2 (LSB)
$\overline{SBHE}$/SRNW	K1	I/O	Byte High Enable (808X mode)/Read Not Write (680XX mode)
$\overline{SWR}$/$\overline{SLDS}$	H1	I/O	Write Strobe (808X mode)/Lower Data Strobe (680XX mode)
$\overline{SRD}$/$\overline{SUDS}$	G1	I/O	Read Strobe (808X mode)/Upper Data Strobe (680XX mode)
SRAS/$\overline{SAS}$	G3	I/O	Register Address Strobe (808X mode)/Memory Address Strobe (680XX mode)
$\overline{SRDY}$/$\overline{SDTACK}$	J1	I/O	Bus Ready (808X mode)/Data Transfer Acknowledge (680XX mode)
SALE	D3	O	Address Latch Enable
SXAL	D2	O	Extended Address Latch Enable
SBCLK	E2	I	System Bus Clock
			SYSTEM BUS DRIVER/RECEIVER CONTROL PINS
SDDIR	C2	O	Data Direction
$\overline{SDBEN}$	C1	O	Data Bus Enable
$\overline{SOWN}$	E5	O	System Bus Owned

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pin descriptions (concluded)

NAME	PIN	I/O	DESCRIPTION
			LAN ADAPTER BUS INTERRUPT PINS
LIRQIN0	G10	I	LAN Adapter Bus Interrupt Request 0 Input
LIRQIN1	F7	I	LAN Adapter Bus Interrupt Request 1 Input
LIRQIN2	F8	I	LAN Adapter Bus Interrupt Request 2 Input
LIRQOUT0	F6	O	LAN Adapter Bus Interrupt Request Output 0
LIRQOUT1	F10	O	LAN Adapter Bus Interrupt Request Output 1
LIRQOUT2	F9	O	LAN Adapter Bus Interrupt Request Output 2
$\overline{\text{LRESET}}$	G9	O	LAN Adapter Bus Reset
			LAN ADAPTER BUS ARBITRATION PINS
$\overline{\text{LBRQS}}$	A10	O	LAN Adapter Bus Request
$\overline{\text{LBGRS}}$	C8	I	LAN Adapter Bus Grant
			MISCELLANEOUS PINS
$\overline{\text{CHPTST}}$	J10	I	This pin is reserved and should be left unconnected.
$\overline{\text{TEST}}$	G8	I	Module-in-Place Test Mode Select
V_{BB}	D10		This pin is reserved and should be left unconnected.
NC	E6		This pin is reserved and should be left unconnected.
			POWER PINS
V_{CC}	J3		5-V power supply (All pins must be connected.)
V_{CC}	J9		
V_{CC}	E9		
V_{CC}	D7		
V_{CC}	D5		
V_{CC}	E3		
V_{SS}	C3		Ground pins (All pins must be connected.)
V_{SS}	E4		
V_{SS}	E1		
V_{SS}	F3		
V_{SS}	F4		
V_{SS}	H6		
V_{SS}	G6		
V_{SS}	G7		
V_{SS}	E8		
V_{SS}	E10		
V_{SS}	B9		
V_{SS}	C5		
V_{SS}	B1		

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description

The TMS38030 System Interface (SIF) connects two high-speed buses and provides DMA and direct I/O (DIO) transfer between these buses. The TMS38030 features a dual-port DMA channel and DIO registers that connect a host system bus transferring data up to 5 megabytes per second to the LAN Adapter bus operating at a 6 megabyte per second transfer rate. For added flexibility the host system bus can be pin-strap selected to either an 808X-type or 680XX-type bus allowing the designer to choose the bus configuration which best meets his application. When in 808X mode, the TMS38030 automatically handles byte swapping to meet the requirements of the 808X processor memory conventions. Four DIO registers on the host system bus are available for handshaking between the host system CPU and the LAN Adapter CPU. Full control of the TMS38030 is provided by nine 16-bit registers accessible from the LAN Adapter bus interface. Control lines on the host system bus interface reduce interface logic requirements by providing direct control of latches and drivers.

The TMS38030, when coupled with the TMS38010 Communications Processor, the TMS38020 Protocol Handler, and the TMS38051 and TMS38052 Ring Interface Circuits, forms a complete integrated Token Ring local area network adapter fully compatible with IEEE Std 802.5-1985 Token Ring Access and Physical Layer Specifications for Token Ring Networks.

architecture

The TMS38030 may be conceptually viewed as shown in Figure 1. The DMA controller differs from conventional DMA controllers in that DMA transfers occur from the memory of one bus to the memory of another bus versus DMA transfers on the same bus. The two buses are independent of each other in that timing of one bus may be asynchronous to the timing of the other. A direct I/O (DIO) (or memory-mapped I/O) interface on the host system bus may be used as a low-level handshake between the two CPUs as well as for posting interrupts from one CPU to the other.

The TMS38030 also contains an interrupt priority encoder for prioritizing up to seven interrupt levels for presentation to the LAN Adapter bus CPU (TMS38010 Communications Processor).

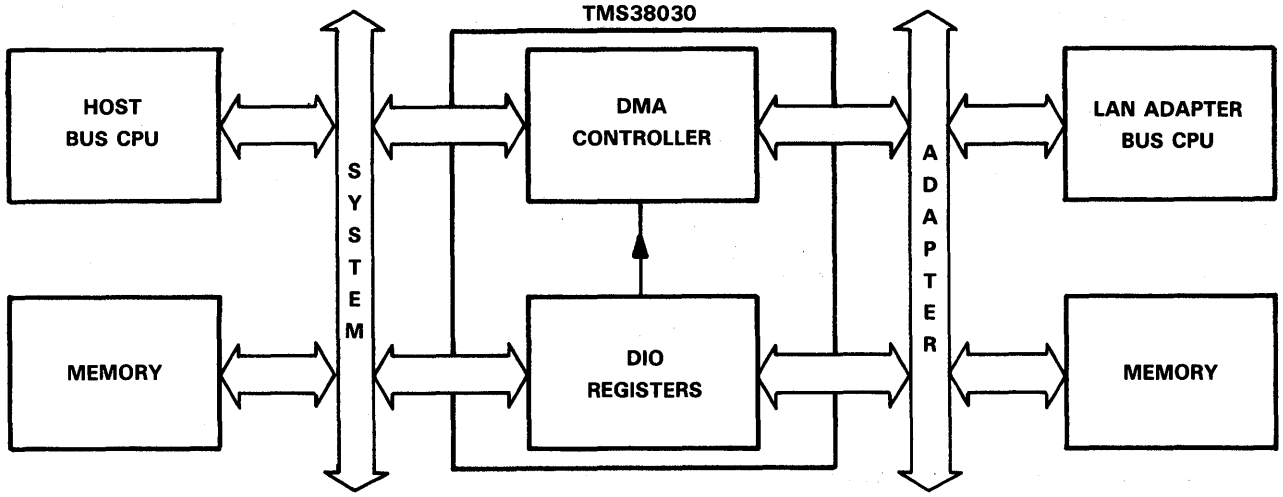

FIGURE 1. TMS38030 DMA CONTROL—CONCEPTUAL REPRESENTATION

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address register

The Address Register provides a pointer into LAN Adapter bus memory address space with which the host system processor may access data through either the Data Register or the Data Register with Autoincrement. Bits 5 through 14 may be set to any value by the host processor by writing the appropriate value to this register. Bits 0-4 and bit 15 may only be set/reset by the LAN Adapter bus CPU. This allows the LAN Adapter bus CPU to control host access to the LAN Adapter bus memory space within a 2K-byte window as defined by the setting of bits 0 through 4. Bit 15 is always set to zero as all data transfers on the LAN Adapter bus are 16-bit transfers (even addresses).

data registers

Two data registers provide read/write capability to the LAN Adapter bus memory address location pointed to by the Address Register. The host processor does not access these locations directly however, the TMS38030 performs LAN Adapter bus DMA operations to read or write the memory location as necessary.

When read, the Data Register returns the value found in the memory location pointed to by the Address Register. The TMS38030 will perform a DMA read of this location when this occurs. Writing to the Data Register will cause the data to be written to the LAN Adapter bus memory location as pointed to by the Address Register when the IOWEN bit of the SIF Control (SIFCTL) Register is set to one. The TMS38030 will perform a DMA write to this location when this occurs.

The Data Register with Autoincrement behaves identically to the Data Register; however, the Address Register is automatically incremented by two following each access (post increment). This feature is useful for the passing of parameter tables to sequential memory locations within the LAN Adapter bus memory space.

direct input/output

Read and write cycles to the direct I/O registers cannot occur simultaneously with DMA operation on the system bus because they share the same physical interface pins. However, a DIO access occurring between two successive bus cycles of a DMA cycle will not disrupt any DMA conditions existing within the TMS38030.

direct memory access

The direct memory access (DMA) channel of the system bus interface provides a full 24 bits of address with which to access up to 16 megabytes of system memory. The throughput capability of the DMA channel is matched to that of the host system through a host system supplied bus clock (SBCLK). The maximum DMA transfer rate corresponds to one word per four user system clock periods. DMA on the system bus may occur concurrently and asynchronously to DMA on the LAN Adapter bus.

When configured in 808X mode, the TMS38030 performs automatic byte swapping on data passed between the LAN Adapter bus and the host system bus. This is to compensate for the differing byte ordering conventions between the 808X-type processor and the LAN Adapter bus CPU. The LAN Adapter bus memory organization defines byte 0 of a 16-bit memory word to be the most-significant byte and byte 1 to be the least-significant. The 808X-type processor defines byte 0 of a 16-bit memory word to be the least-significant byte and byte 1 to be the most-significant. Byte swapping automatically corrects for this difference in convention. Byte swapping is not performed on DIO accesses.

The system bus DMA is controlled by the LAN Adapter bus CPU through the registers resident on the Adapter bus. The system bus DMA may be configured for system bus starting address, DMA length, burst or cycle-steal mode of operation and parity checking on DMA reads.

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SIFCTL register

The SIFCTL register controls all TMS38030 peripheral functions. Certain values are loaded to the bits of SIFCTL when the LAN Adapter bus CPU writes to address >0080. The current value of the bits are returned by reading the word at this location. Changes made to DMADIR, DMABURST, SPIEN, and SLPIEN bits have no effect on DMA operations already in progress. Such changes affect subsequent DMA operation. All bits of SIFCTL are set to zero when $\overline{\text{SRESET}}$ is activated. The bits of SIFCTL are summarized in Table 3.

TABLE 3. SIFCTL REGISTER BIT FUNCTIONS

BIT	NAME	DESCRIPTION
0	DMADIR	System DMA Direction
1	DMAENB	System DMA Enable
2	DMABURST	System DMA Burst Mode
3	DMAHALT	System DMA Halt
4	DMAIEN	System DMA Interrupt Enable
5	SPIEN	System Parity Interrupt Enable
6	SPTST	System Parity Test
7	SLPIEN	System Local Parity Enable
8	IOWEN	DIO Write Enable
9-15		Reserved

SIFACT register

The SIFACT register contains the system bus error flag, LAN Adapter bus and system bus parity error flags, and the DMA halt interrupt request bit. All bits of SIFACT are reset to zero at system reset. Table 4 summarizes the bit functions of the SIFACT register.

TABLE 4. SIFACT REGISTER BIT FUNCTIONS

BIT	NAME	DESCRIPTION
0		Reserved
1		Reserved
2	DIRQ	System DMA Halt Interrupt Request
3	SPE	System Parity Error - DIO
4	SDPE	System Parity Error - DMA
5	SDBE	System DMA Bus Error
6	LPEXM	LAN Adapter Bus Parity Error - External Master
7	LPESM	LAN Adapter Bus Parity Error - TMS38030 Master
8-15		Reserved

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TABLE 6. INTERRUPT REQUEST CODES

LIRQIN0	LIRQIN1	LIRQIN2	MEANING
0	0	0	Level-1 Interupt Request
0	0	1	Level-2 Interrupt Request
0	1	0	Level-3 Interrupt Request
0	1	1	Level-4 Interrupt Request
1	0	0	Level-5 Interrupt Request
1	0	1	Level-6 Interrupt Request
1	1	0	Level-7 Interrupt Request
1	1	1	No request

TMS38030 Generated Interrupts

The TMS38030 will assert an interrupt on the LIRQOUT0 through LIRQOUT2 pins as follows:

1. LAN Adapter bus or system bus parity errors are asserted on level 2.
2. The system DMA complete interrupt is asserted on level 6.
3. The interrupt request from the system bus (MSB of the interrupt register is set to one) is asserted on level 7.

test mode

The TMS38030 features a module-in-place test mode for board level testing with the TMS38030 in circuit. This facilitates testing by bed-of-nails testers. This test mode is enabled by tying the $\overline{\text{TEST}}$ pin to ground. This has the effect of driving all outputs of the TMS38030 to a high-impedance state. When not used for testing purposes, this pin should be left unconnected. An internal pullup drives the $\overline{\text{TEST}}$ pin high when not externally connected.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 2) . . . . . 7 V
Input voltage range . . . . . −0.3 V to 20 V
Output voltage range . . . . . −2 V to 7 V
Operating free-air temperature range (see Note 3) . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. Voltage values are with respect to V_{SS}.
3. Devices are tested in an environment in excess of 70°C to guarantee operation at 70°C. Case temperatures should be maintained at or below 85°C.

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electrical characteristics over full range of recommended operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	All outputs	V_{CC} = 4.5 V, I_{OH} = max	2.4			V
V_{OL}	Low-level output voltage	All outputs	V_{CC} = 4.5 V, I_{OL} = max			0.45	V
I_{OH}	High-level output current	$\overline{SBHE}$/SRNW, $\overline{SWR}$/$\overline{SLDS}$, $\overline{SRD}$/$\overline{SUDS}$, SRAS/$\overline{SAS}$, $\overline{SRDY}$/$\overline{SDTACK}$, SADH0-SADH7, SADL0-SADL7, SPH, SPL, SHRQ/$\overline{SBRQ}$ SINTR/$\overline{SIRQ}$, $\overline{SDBEN}$, SDDIR, SALE, SXAL, $\overline{SOWN}$	V_{CC} = 4.5 V, V_{OH} = 2.4 V			400	μA
		$\overline{LBRQS}$, $\overline{LRESET}$, LIRQOUT0-LIRQOUT2, LAL, $\overline{LEN}$, LI/$\overline{D}$, LR/$\overline{W}$, LAD0-LAD15, LPH, LPL				150	μA
I_{OL}	Low-level output current	$\overline{SBHE}$/SRNW, $\overline{SWR}$/$\overline{SLDS}$, $\overline{SRD}$/$\overline{SUDS}$, SRAS/$\overline{SAS}$, $\overline{SRDY}$/$\overline{SDTACK}$, SHRQ/$\overline{SBRQ}$, SINTR/$\overline{SIRQ}$	V_{CC} = 4.5 V, V_{OL} = 0.45 V			−2	mA
		SADH0-SADH7, SADL0-SADL7, SPH, SPL, SDDIR				−2.5	mA
		SALE, SXAL				−3.5	mA
		$\overline{SDBEN}$				−5	mA
		$\overline{SOWN}$				−5.5	mA
		$\overline{LBRQS}$, $\overline{LRESET}$, LIRQOUT0-LIRQOUT2, LAL, $\overline{LEN}$, LI/$\overline{D}$, LR/$\overline{W}$, LAD0-LAD15, LPH, LPL				−1.7	mA

Continued next page.

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LAN ADAPTER BUS READ AND WRITE PARAMETERS

switching characteristics/timing requirements over recommended supply voltage range and operating free-air temperature range (see Figure 3)

	PARAMETER	MIN	MAX	UNIT
t_{d13}	Delay time, LBCLK2 rise to LI/$\overline{D}$ valid		47	ns
t_{d14}	Delay time, LBCLK2 rise to LAL high		47	
t_{d15}	Delay time, LBCLK2 rise to address valid		47	
t_{d16}	Delay time, LBCLK2 rise to LR/$\overline{W}$ valid		47	
t_{wH1}	Pulse duration, LAL high	Q-50		
t_{d17}	Delay time, address valid to LAL no longer high	Q-50		
t_{d18}	Delay time, LAL fall to 1.3 V to address no longer valid	7		
t_{d19}	Delay time, LBCLK1 high to address no longer valid	7		
t_{d20}	Delay time, LBCLK2 rise to LAD, LPH, LPL high impedance in read cycle		Q+74	
t_{d21}	Delay time, LAD, LPH, LPL high impedance to $\overline{LEN}$ no longer high in read cycle	0		
t_{d22}	Delay time, LBCLK2 rise to $\overline{LEN}$ low in read cycle		Q+84	
t_{d23}	Delay time, LBCLK2 rise to $\overline{LEN}$ low in write cycle		Q+47	
t_{d24}	Delay time, LBCLK1 low to $\overline{LEN}$ no longer low in read cycle	0		
t_{d25}	Delay time, LBCLK2 rise to $\overline{LEN}$ high in read cycle		3Q+47	
t_{d26}	Delay time, LBCLK2 rise to LAL low		2Q−12	
t_{d27}	Delay time, LBCLK1 low to LAD, LPH, LPL no longer high impedance in next cycle	80		
t_{d28}	Delay time, LBCLK2 rise to write data valid		3Q−70	
t_{d29}	Delay time, LBCLK1 low to LI/$\overline{D}$, LR/$\overline{W}$ no longer valid	20		
t_{d30}	Delay time, LBCLK1 low to write data no longer valid	20		
t_{d31}	Delay time LBCLK1 low to $\overline{LEN}$ no longer low in write cycle	20		
t_{d32}	Delay time, LBCLK1 low to $\overline{LEN}$ high in write cycle		80	
t_{d33}	Delay time, LBCLK2 rise to $\overline{LEN}$ no longer high in write cycle	Q−4		
t_{su1}	Setup time, Read data valid to LBCLK1 no longer high	20		
t_{h1}	Hold time, read data valid after LBCLK1 low if t_{h2} not met	15		
t_{h2}	Hold time, read data valid after $\overline{LEN}$ no longer low if t_{h1} not met	0		
t_{d34}	Delay time, LBCLK2 rise to LBRDY high		2Q−41	
t_{d35}	Delay time, LBCLK2 rise to LBRDY low		2Q−21	
t_{h3}	Hold time, LBRDY valid after LBCLK2 low	80		

†This table is entitled switching characteristics/timing requirements because several of the parameters specified can be classified as characteristics or requirements depending on the mode of operation: bus slave or bus master (DMA). The values given are valid for both modes.

NOTE 6: Q = 0.25 $t_{c(LA)}$.

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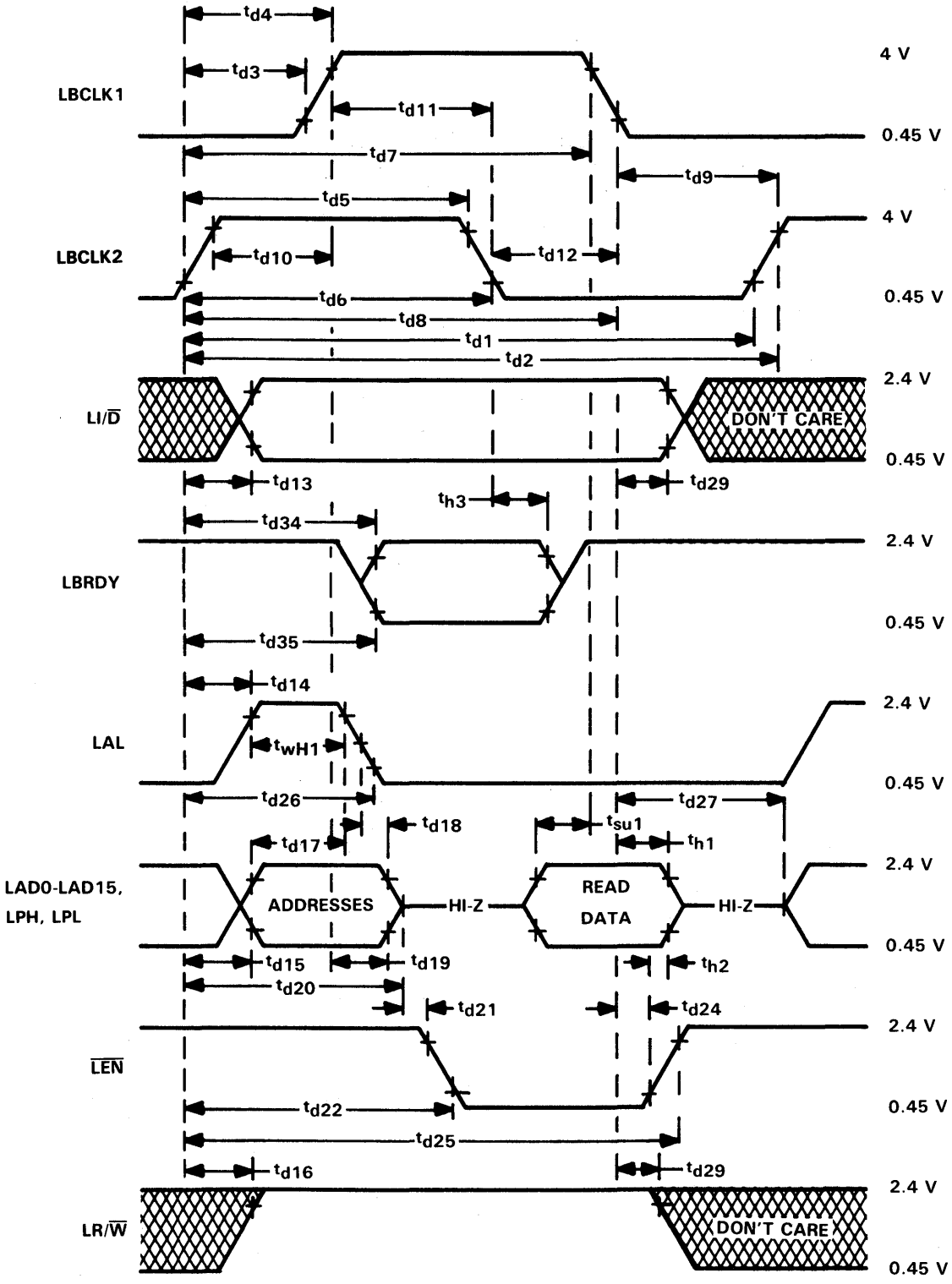
LAN adapter bus read timing



NOTE 8: The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for the other waveforms are 2 V and 0.8 V. The intermediate reference point for LAL is 1.3 V.

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LAN ADAPTER BUS ARBITRATION PARAMETERS

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 3)

	PARAMETER	MIN	MAX	UNIT
t_{d36}	Delay of $\overline{\text{LBRQS}}$ from LBCLK1 low		48	ns
t_{d37}	Delay of $\overline{\text{LBRQS}}$ after LBCLK1 rise	0		
t_{d38}	Delay time, LBCLK2 rise to LAL no longer high impedance by TMS38030	2Q−9		
t_{d39}	Delay time, LBCLK2 rise to LAL driven low by TMS38030		3Q−15	
t_{d40}	Delay time, LBCLK1 low to $\overline{\text{LEN}}$ no longer high impedance by TMS38030	80		
t_{d41}	Delay time, LBCLK2 rise to $\overline{\text{LEN}}$ driven high by TMS38030		74	
t_{d42}	Delay time, LBCLK1 low to LR/$\overline{\text{W}}$, LI/$\overline{\text{D}}$, LAD0-LAD15, LPH, and LPL no longer high impedance by TMS38030	80		

NOTE 6: Q = 0.25 $t_{c(LA)}$.

timing requirements over recommended supply voltage range and operating free-air temperature range

	PARAMETER	MIN	MAX	UNIT
t_{d43}	Delay time, LBCLK2 rise to $\overline{\text{LBGRS}}$ valid		2Q−73	ns
t_{d44}	Delay time, LBCLK2 rise to $\overline{\text{LBGRS}}$ no longer valid	−6		
t_{d45}	Delay time, LBCLK2 rise to LAL no longer driven low from old bus master	3Q−15		
t_{d46}	Delay time, LBCLK2 rise to LAL high impedance from old bus master		4Q−2	
t_{d47}	Delay time, LBCLK2 rise to $\overline{\text{LEN}}$ high impedance from old bus master		74	
t_{d48}	Delay time, LBCLK1 low to LR/$\overline{\text{W}}$, LI/$\overline{\text{D}}$, LAD0-LAD15, LPH, and LPL high impedance from old bus master		80	

NOTE 6: Q = 0.25 $t_{c(LA)}$.

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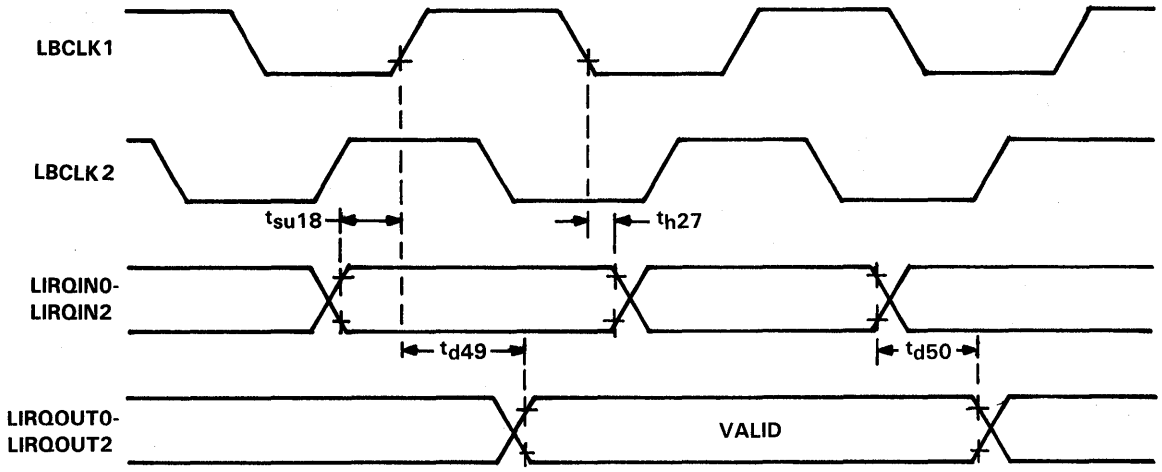
MISCELLANEOUS LAN ADAPTER BUS PARAMETERS

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 3)

	PARAMETER	MIN	MAX	UNIT
t_{d49}	Delay time, LBCLK1 rise to LIRQOUT0-LIRQOUT2 valid		140	ns
t_{su18}	LIRQIN0-LIRQIN2 setup before LBCLK1 rise	0		
t_{h27}	Hold time, LIRQIN0-LIRQIN2 after LBCLK1 low	0		
t_{d50}	Delay time, LIRQIN0-LIRQIN2 no longer valid to LIRQOUT0-LIRQOUT2 no longer valid	0		

interrupt timing



NOTE 10: LIRQOUTs may not follow LIRQINs because the TMS38030 prioritizes LIRQOUT0-LIRQOUT2 outputs between internal TMS38030 interrupts and LIRQIN0-LIRQIN2.

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switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 3) (concluded)

	PARAMETER	MIN	MAX	UNIT
t_{d74}	Delay from SBCLK high to bus request valid (Note 11)		60	ns
t_{wL1}	Pulse duration, $\overline{SRD}$ low	$2t_{c(SC)}-40$		
t_{wL2}	Pulse duration, $\overline{SWR}$ low	$2t_{c(SC)}-40$		
t_{su2}	Setup of address valid before SALE, SXAL no longer high	$t_{w(SCL)}-43$		
t_{su3}	Setup of address valid before $\overline{SAS}$ no longer high	$t_{w(SCL)}-32$		
t_{d75}	Delay from T2 high to $\overline{SDBEN}$ low in read cycle (Note 11)		80	
t_{d76}	Delay from T1 high to $\overline{SDBEN}$ low in write cycle (Note 11)		60	
t_{wL3}	Pulse duration, $\overline{SAS}$ on read and write; pulse duration, $\overline{SUDS}$ and $\overline{SLDS}$ on read	$2t_{c(SC)}+t_{w(SCH)}-50$		
t_{su4}	Setup of control signals HI-Z before $\overline{SOWN}$ no longer low	0		
t_{d77}	Delay from TX high to data strobes high, bus acquisition (Note 11)		70	
t_{h9}	Hold of data strobe HI-Z after $\overline{SOWN}$ low, bus acquisition	$t_{c(SC)}-70$		
t_{wL4}	Pulse duration, $\overline{SUDS}$ and $\overline{SLDS}$ on write	$t_{c(SC)}+t_{w(SCH)}-50$		
t_{d78}	Delay from $\overline{SRESET}$ low to $\overline{LRESET}$ low, V_{CC} at V_{CC} min		100	
t_{d79}	Delay from $\overline{SRESET}$ high to $\overline{LRESET}$ high		200	
t_{d80}	Delay from reaching minimum V_{CC} during power-up to valid SBCLK, LBCLK1, LBCLK2		90	ms

NOTE 11: Unless otherwise specified, for all signals specified as a maximum delay from the end of an SBCLK transition to the signal valid, the signal is also specified to hold its previous value (including HI-Z) until the start of that SBCLK transition.

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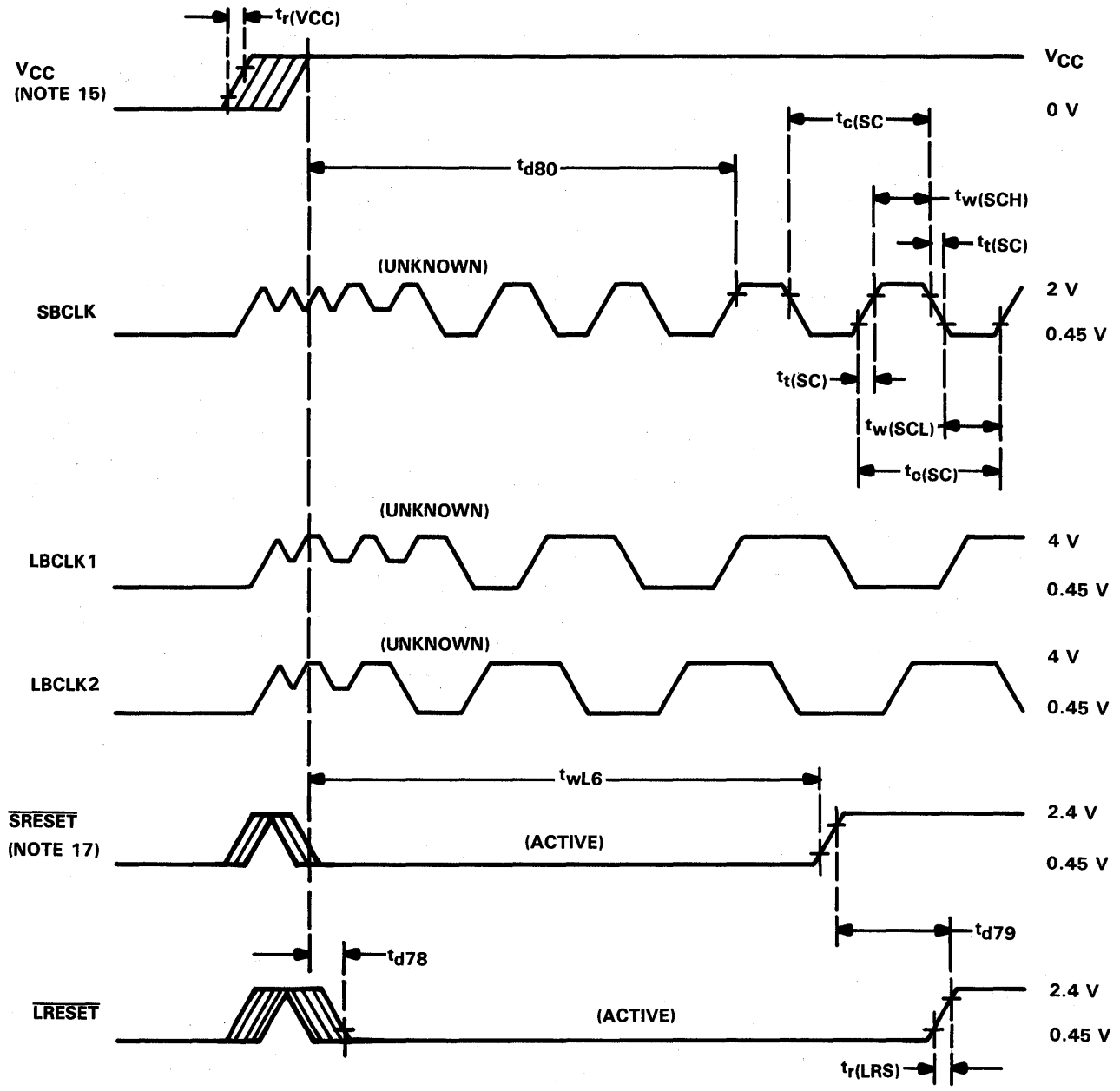
power-up, SBCLK, LBCLK, $\overline{\text{SRESET}}$, and $\overline{\text{LRESET}}$ timing

power on



NOTES: 15. A minimum one second interval between power off and power on is required for correct initialization of the TMS38030.
16. The timing reference points for LBCLK1 and LBCLK2 are 3 V and 0.8 V. The timing reference points for SBCLK, $\overline{\text{SRESET}}$, and $\overline{\text{LRESET}}$ are 2 V and 0.8 V. The timing reference points for V_{CC} are 4.5 V and 1.2 V.
17. During power-up, $\overline{\text{SRESET}}$ is undefined (asserted) prior to 1.2 V applied to the V_{CC} pins of the TMS38030. $\overline{\text{SRESET}}$ must remain asserted from V_{CC} = 1.2 V to V_{CC} minimum. The TMS38030 must not be accessed from either the system or LAN Adapter bus interface within 3 μs of the de-assertion of $\overline{\text{SRESET}}$. This is primarily a test limitation since currently available processors cannot violate this condition.

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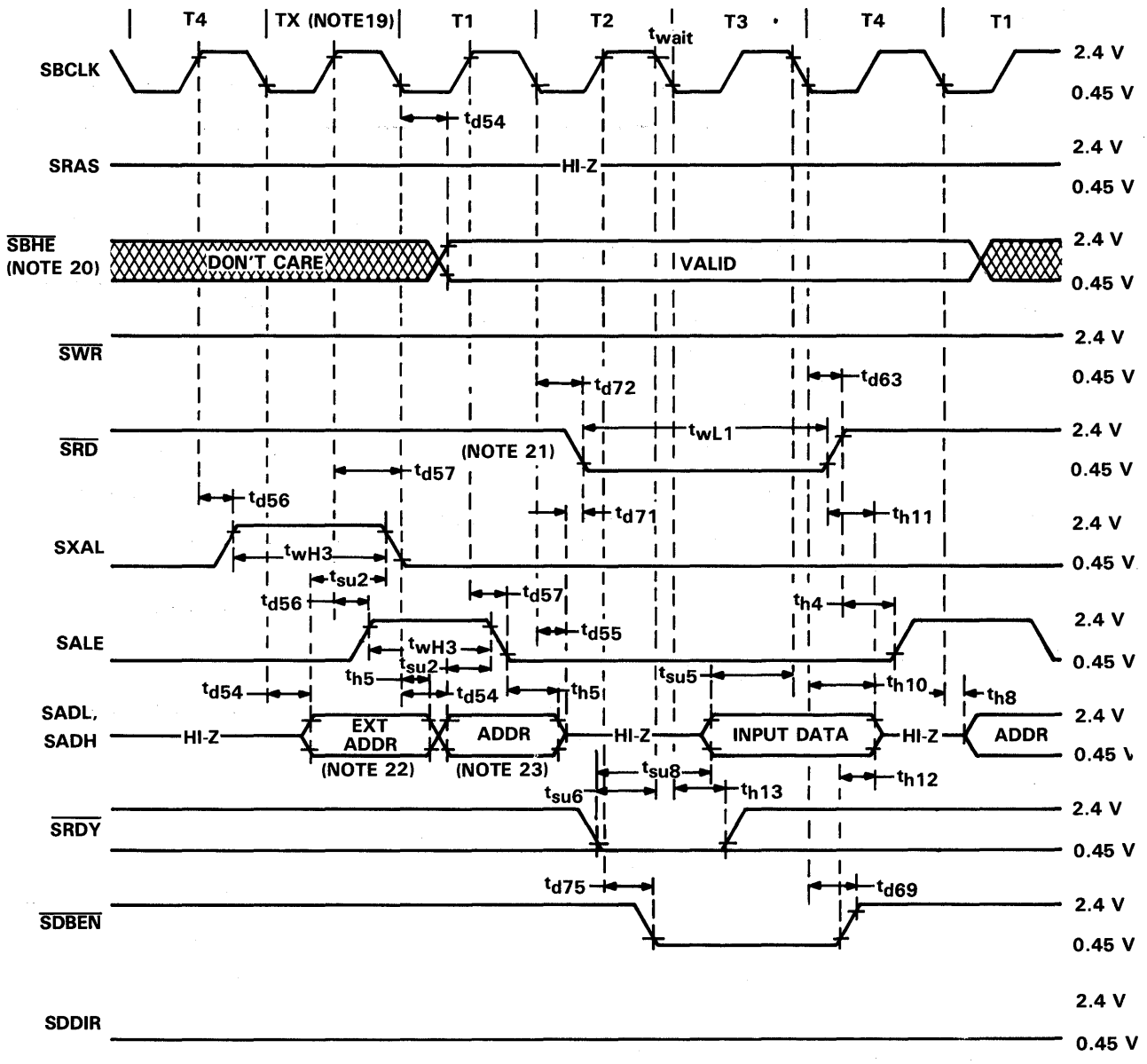
808X mode DMA read timing



NOTES: 19. In cycle-steal mode, state TX is present on every system bus transfer. In burst mode, state TX is present on the first bus transfer, and whenever the increment of the address carries beyond the least-significant 8 bits.
20. In 8-bit 808X Mode, $\overline{SBHE}$/SRNW is a don't care input during DIO and an inactive (high) output during DMA.
21. If the TX state is not present, $\overline{SAS}$, $\overline{SUDS}$, and $\overline{SLDS}$ are asserted in the T1 state.
22. In state TX, SADH continues to output the most-significant byte of the address.
23. In 8-bit mode, the most-significant byte of the address is maintained on SADH for T2, T3, and T4. The address is maintained according to t_{h6}, i.e., held after T4 high.

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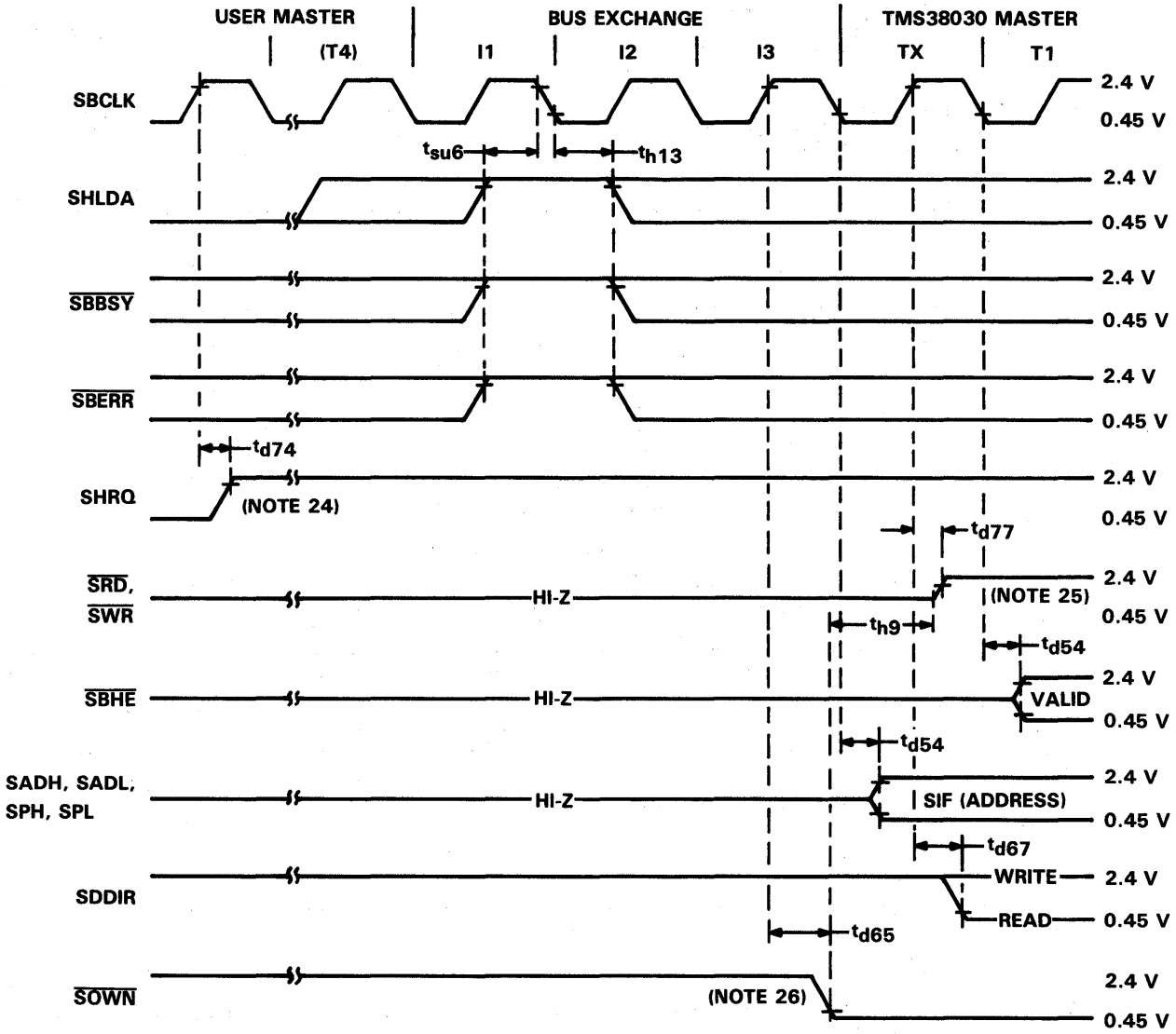
808X mode bus arbitration timing

TMS38030 takes control of system bus from user processor



NOTES: 24. SHLDA/$\overline{\text{SBGR}}$ must be sampled in its deasserted state on the falling edge of SBCLK. The TMS38030 will then assert SHRQ/$\overline{\text{SBRQ}}$ on the second subsequent rising edge of SBCLK.

25. When taking over the system bus, the TMS38030 drives all data strobes high for the time between T1 high and the edge at which the strobes are driven low. The logical value of the strobes in this period is not defined.

26. While TMS38030 DMA controls are active (i.e., $\overline{\text{SOWN}}$ is asserted), the $\overline{\text{SCS}}$ input is disabled.

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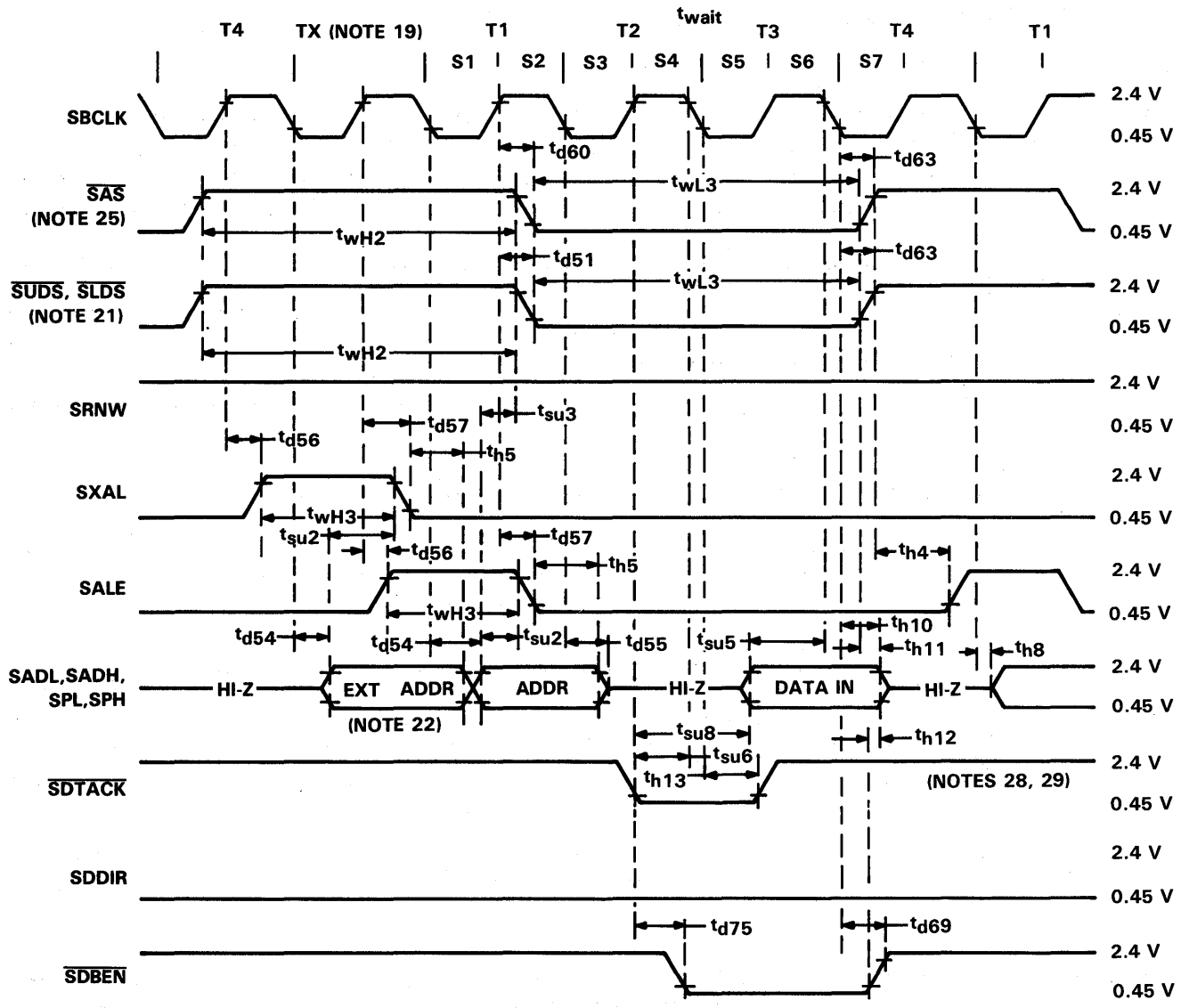
680XX mode DMA read timing



NOTES: 19. In cycle-steal mode, state TX is present on every system bus transfer. In burst mode, state TX is present on the first bus transfer, and whenever the increment of the address carries beyond the least-significant 8 bits.
21. If the TX state is not present, $\overline{SAS}$, $\overline{SUDS}$, and $\overline{SLDS}$ are asserted in the T1 state.
22. In state TX, SADH continues to output the most-significant byte of the address.
28. $\overline{SDTACK}$ is not sampled to verify that it is deasserted.
29. 680XX-style bus slaves hold $\overline{SDTACK}$ active until the bus master deasserts $\overline{SAS}$. In this case, the slave still meets t_{h13}.

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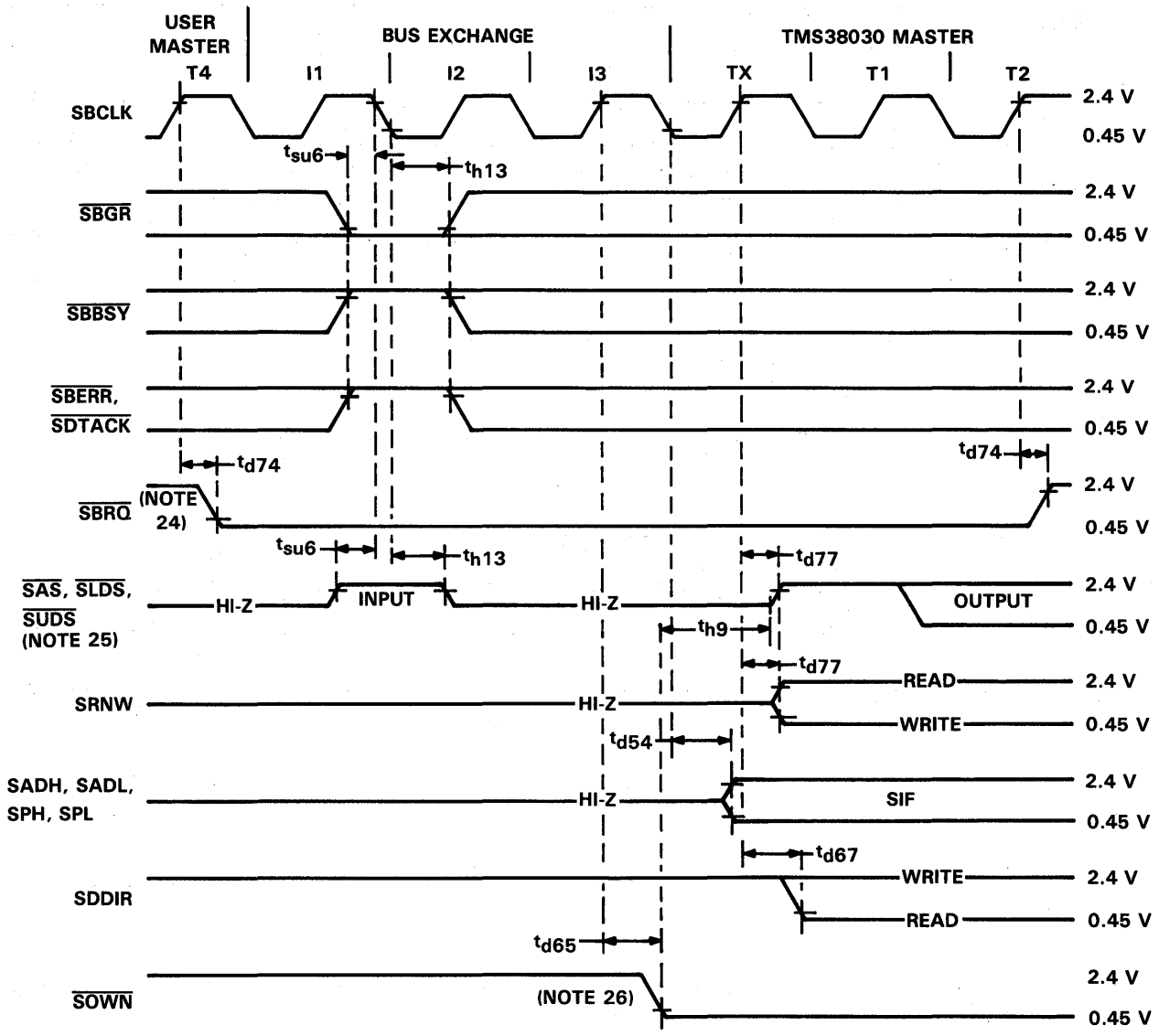
680XX mode bus arbitration timing

TMS38030 takes control of system bus from user processor



NOTES: 24. SHLDA/$\overline{\text{SBGR}}$ must be sampled in its deasserted state on the falling edge of SBCLK. The TMS38030 will then assert SHRQ/$\overline{\text{SBRQ}}$ on the second subsequent rising edge of SBCLK.

25. When taking over the system bus, the TMS38030 drives all data strobes high for the time between T1 high and the edge at which the strobes are driven low. The logical value of the strobes in this period is not defined.

26. While TMS38030 DMA controls are active (i.e., $\overline{\text{SOWN}}$ is asserted), the $\overline{\text{SCS}}$ input is disabled.

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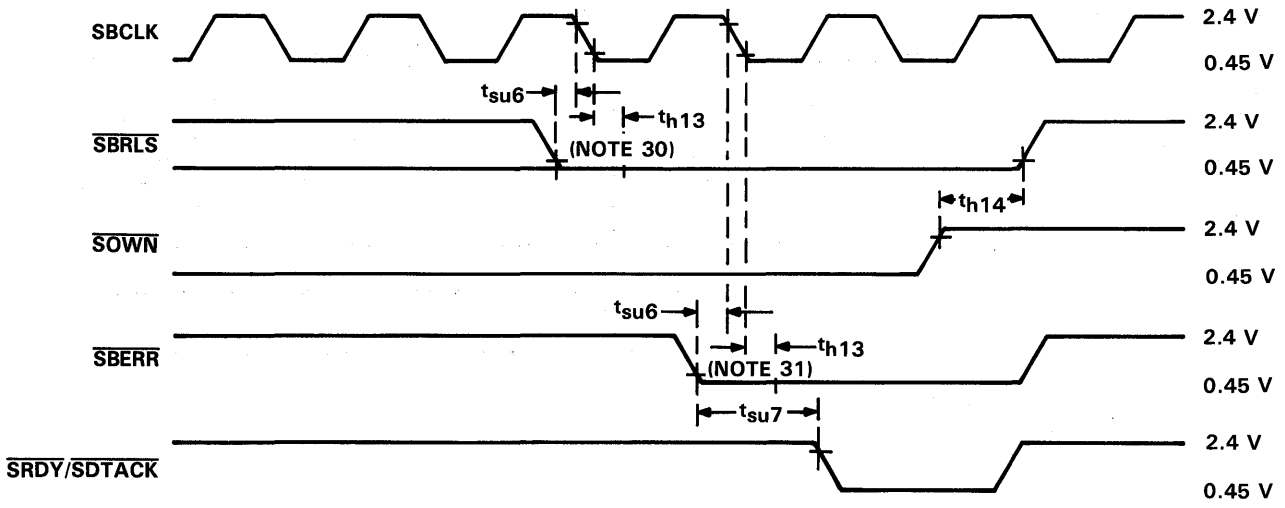
bus release and error timing



NOTES: 30. The TMS38030 ignores the assertion of $\overline{\text{SBRLS}}$ if it does not own the system bus. If it does own the system bus, then when it detects the assertion of $\overline{\text{SBRLS}}$ it will complete any internally started DMA cycle and relinquish control of the bus. If no DMA transfer has internally started, then the TMS38030 will release the bus before starting another.

If $\overline{\text{SBRLS}}$ is asserted prior to state T1, then that DMA cycle will be the last cycle before the TMS38030 releases the bus. If $\overline{\text{SBRLS}}$ is asserted after state T1 in a DMA cycle, the TMS38030 will complete the current cycle and the next cycle before releasing the system bus.

The TMS38030 will deassert SHRQ/$\overline{\text{SBRQ}}$ during state I1 of the bus exchange cycle. SHLDA/$\overline{\text{SBGR}}$ must be deasserted to cause the TMS38030 to re-request the bus.

31. If $\overline{\text{SBERR}}$ is asserted when the TMS38030 controls the system bus, then the current bus transfer is completed, regardless of the value of $\overline{\text{SRDY}}$/$\overline{\text{SDTACK}}$. In this case, the TMS38030 will then release control of the system bus. The TMS38030 ignores $\overline{\text{SBERR}}$ if it is not performing a DMA cycle. When $\overline{\text{SBERR}}$ is properly asserted, however, the TMS38030 releases the bus upon completion of the current bus transfer and halts all further DMA on the system side. The error is synchronized to the LAN Adapter bus and DMA stops on the LAN Adapter bus side. The value of SDMAADR, LDMAADR, and SDMALEN registers in the TMS38030 are not defined after a system bus error.

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timing requirements over recommended supply voltage range and operating free-air temperature range

	PARAMETER	MIN	MAX	UNIT
t_{wH4}	Pulse duration, data strobe high between DIO accesses	100		ns
t_{su11}	Setup of asynchronous input to SBCLK no longer high in order to guarantee recognition (Note 34)	35		
t_{h20}	Hold of asynchronous input after SBCLK low to guarantee strobe not recognized.	45		
t_{h21}	Hold of $\overline{SCS}$ or data strobe low after $\overline{SRDY}/\overline{SDTACK}$ no longer HI-Z (Note 35)	0		
t_{d93}	Delay from $\overline{SRDY}/\overline{SDTACK}$ low to either $\overline{SCS}$ or data strobe high (Note 36)		1000	
t_{wH5}	Pulse duration, SRAS high	40		
t_{su12}	Setup of write data valid before SBCLK no longer low (Note 37)	105		
t_{d94}	Delay from write strobe low to input write data valid (Note 37)		$4t_{c(SC)} + t_{w(SCL)} - 150$	
t_{h22}	Hold of write data valid after $\overline{SDBEN}$ NO LONGER LOW (Note 38)	0		
t_{su13}	Setup of SRS0-SRS2, $\overline{SCS}$ (not shown) and $\overline{SBHE}$ to SRAS no longer high	18		
t_{h23}	Hold of SRS0-SRS2, $\overline{SCS}$ (not shown) and $\overline{SBHE}$ after SRAS low	20		
t_{su14}	Setup of SRAS high to data strobe no longer high	42		
t_{su15}	Setup of register address before data strobe no longer high	20		
t_{h24}	Hold of register address valid after $\overline{SRDY}/\overline{SDTACK}$ no longer HI-Z (Note 35)	0		
t_{su16}	Setup of SRNW before data strobe no longer high	40		
t_{su17}	Setup of inactive data strobe high to active data strobe no longer high	100		
t_{h25}	Hold of SRNW after $\overline{SRDY}/\overline{SDTACK}$ no longer HI-Z (Note 38)	0		
t_{h26}	Hold of inactive data strobe high after active data strobe high	100		
t_{wH6}	Pulse duration, $\overline{SCS}$ and $\overline{SIACK}$ both high	100		
t_{wL7}	Pulse duration, $\overline{SIACK}$ low on first pulse of two pulses in 808X Mode	150		

NOTES: 34. For 680XX mode, skew between $\overline{SLDS}$ and $\overline{SUDS}$ must not exceed 10 ns. Providing this limitation is observed, all events referenced to a data strobe edge are to the later occurring edge. Events defined by two data strobe edges, parameter t_{wH4}, are measured between latest and earlier edges.

35. In 808X Mode, SRAS may be used to strobe the values of $\overline{SBHE}$, SRS0-SRS2 and $\overline{SCS}$. When used to do so, SRAS must meet parameter t_{su14} and $\overline{SBHE}$, SRS0-SRS2, and $\overline{SCS}$ must meet parameter t_{su13}. If SRAS is strapped high, then parameters t_{su14} and t_{su13} are irrelevant.

36. The system must provide sufficient delay between TMS38030's assertion of $\overline{SRDY}/\overline{SDTACK}$ and the system's deassertion of the data strobe(s) in order to allow the TMS38030 to hold SDDIR valid after $\overline{SDBEN}$ is inactive.

37. Write data is sampled on the fifth rising edge of SBCLK following the recognition of a write data strobe on a falling edge of SBCLK.

38. Since $\overline{SDBEN}$ is deasserted before $\overline{SRDY}/\overline{SDTACK}$ is asserted, external logic may remove write data when $\overline{SRDY}/\overline{SDTACK}$ is asserted. Register addresses and SRNW may also be deasserted when $\overline{SRDY}/\overline{SDTACK}$ is asserted. For testing purposes, the timing point "$\overline{SRDY}/\overline{SDTACK}$ no longer HI-Z" refers to the 2 V point of the falling edge of the $\overline{SRDY}/\overline{SDTACK}$ signal with a 10 kΩ pullup to V_{CC}.

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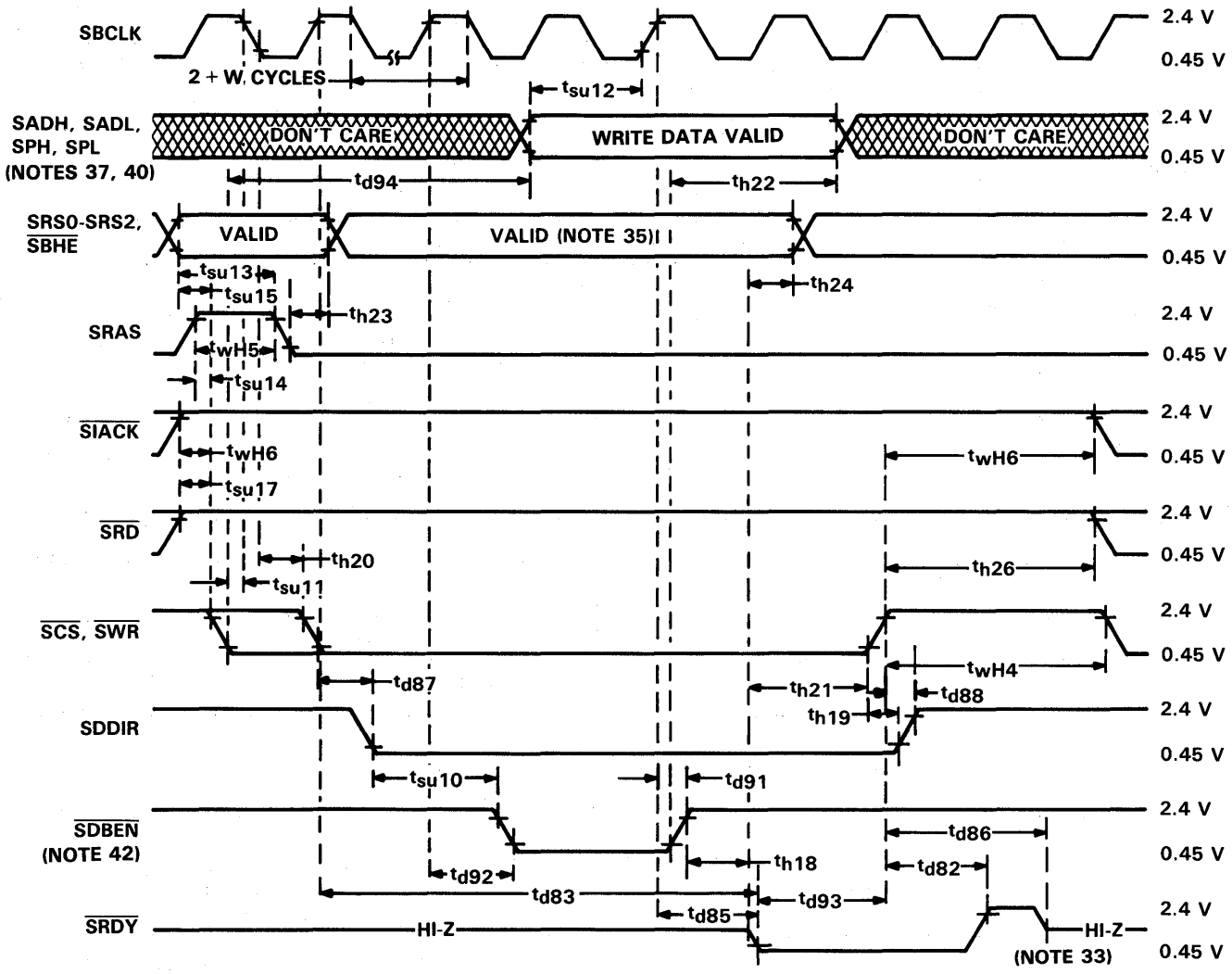
808X mode DIO write timing



NOTES: 33. Internal logic will drive $\overline{\text{SRDY}}/\overline{\text{SDTACK}}$ high and verify that it has reached a valid high level before tristating the signal.

35. In 808X Mode, SRAS may be used to strobe the values of $\overline{\text{SBHE}}$, SRS0-SRS2 and $\overline{\text{SCS}}$. When used to do so, SRAS must meet parameter t_{su14} and $\overline{\text{SBHE}}$, SRS0-SRS2, and $\overline{\text{SCS}}$ must meet parameter t_{su13}. If SRAS is strapped high, then parameters t_{su14} and t_{su13} are irrelevant.

37. Write data is sampled on the fifth rising edge of SBCLK following the recognition of a write data strobe on a falling edge of SBCLK.

40. In 8-bit mode DIO writes, the value placed on SADH is a don't care.

42. In a write cycle, $\overline{\text{SDBEN}}$ is asserted on the third rising edge of SBCLK following the sample of a write data strobe.

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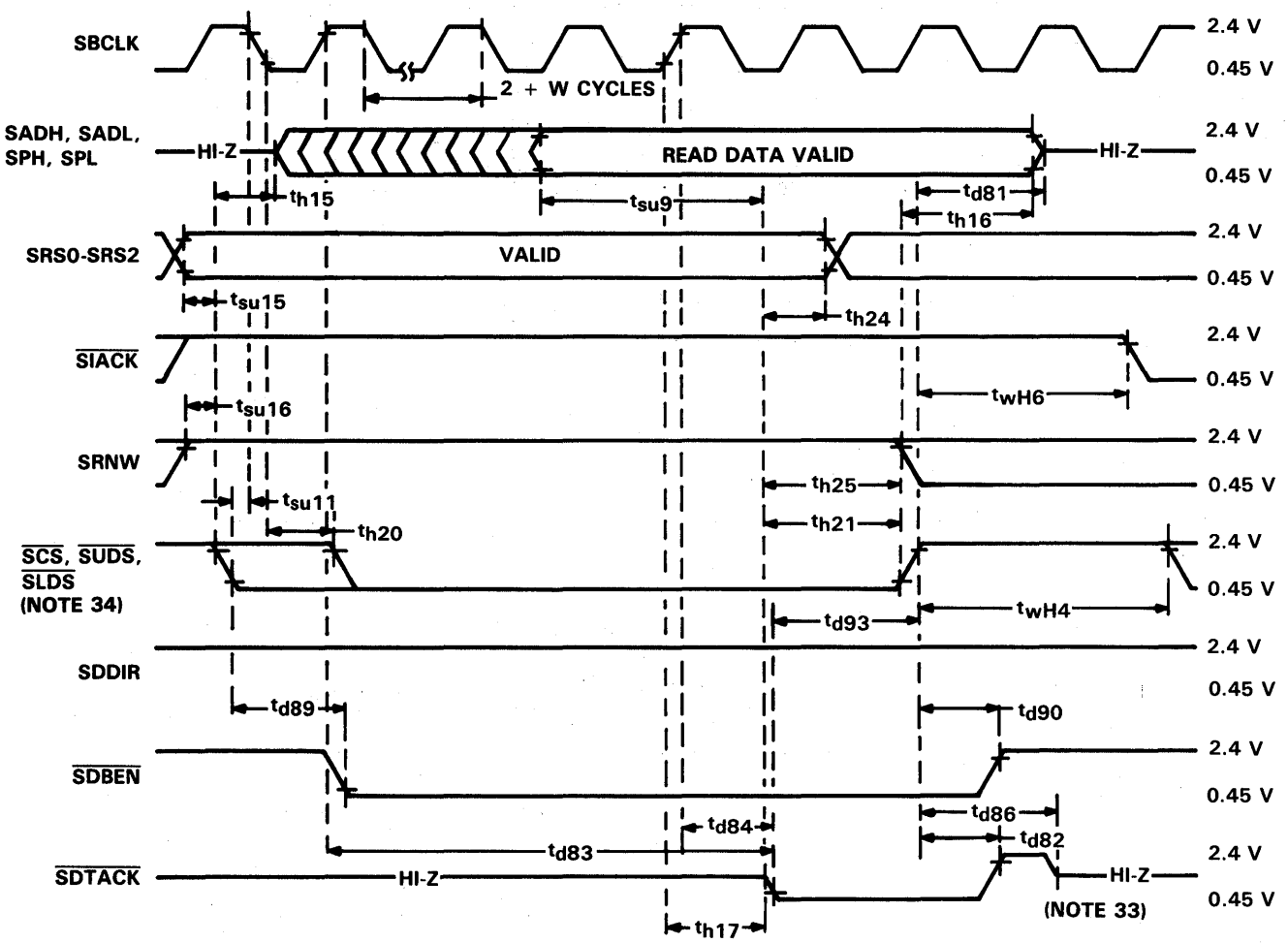
680XX mode DIO read timing

680XX master reads TMS38030 DIO register



NOTES: 33. Internal logic will drive $\overline{SRDY}/\overline{SDTACK}$ high and verify that it has reached a valid high level before tristating the signal.
34. For 680XX mode, skew between $\overline{SLDS}$ and $\overline{SUDS}$ must not exceed 10 ns. Providing that limitation is observed, all events referenced to a data strobe edge are to the later occurring edge. Events defined by two data strobe edges, parameter t_{wH4}, are measured between latest and earlier edges.

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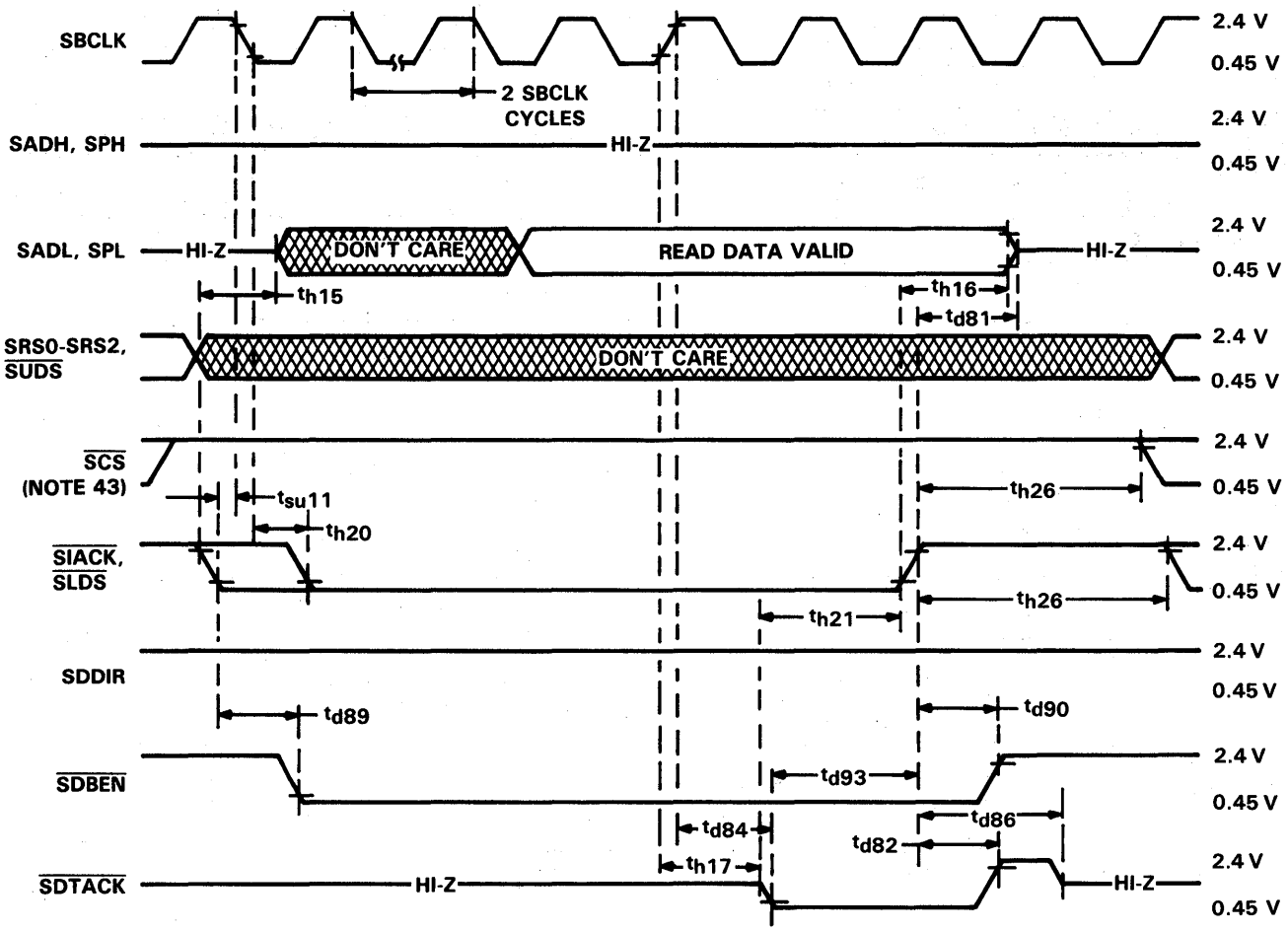
680XX mode interrupt acknowledge cycle timing

680XX master reads interrupt vector from TMS38030



NOTE 43: The "inactive" chip select is $\overline{\text{SIACK}}$ in DIO read and DIO write cycles, and $\overline{\text{SCS}}$ in interrupt acknowledge cycles.

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pin descriptions

TMS38051

NAME	I/O	DESCRIPTION
RCVINA	I	Receiver Input A
RCVINB	I	Receiver Input B
EQUALA	I	Equalization/Gain Point A
EQUALB	I	Equalization/Gain Point B
RCVHYS	I	Receiver Hysteresis Resistor
RCVR	O	Receive Data
DRVR	I	Driver Data Input
DROUTA	O	Driver Output A
DROUTB	O	Driver Output B
CHGPMP	O	Charge-Pump Output
DCLKIN	I	Data-Latch Clock
NRGCAP	I	Energy-Detect Capacitor
ENERGO	O	Energy-Detect Output Signal to TMS38052
$\overline{\text{WRAP}}$	I	Internal Wrap-Mode Control
ENABLE	I	Output-Enable Control
FRAQ	I	Frequency Acquisition Control
XTAL	I	Crystal-Oscillator Input
V_{CC}		General 5-V Power
V_{CCA}		Analog 5-V Power
GND		General Ground
GNDDRV		Ground for Driver Output
GNDA		Analog Ground

TMS38052

NAME	I/O	DESCRIPTION
$\overline{\text{NSRT}}$	I	Phantom-Driver Control
PHOUTA	O	Phantom-Driver Output A
PHOUTB	O	Phantom-Driver Output B
$\overline{\text{WFLT}}$	O	Wire-Fault Indicator
FILTER	I	Filter-Buffer Input
VCOGAN	I	VCO-Gain Resistor
VCOCPA	I	VCO Timing Capacitor Pin A
VCOCPB	I	VCO Timing Capacitor Pin B
RCLK	O	Recovered Clock
DCLKOUT	O	Data-Latch Clock
LOCKIN	I	Reserved, must be tied to ground.
LOCKRF	I	Reserved, must be tied to ground.
ENERGI	I	Energy-Detect Input Signal
$\overline{\text{REDY}}$	O	Ready Signal
ENABLE	I	Output-Enable Control
V_{CC}		General 5-V Power
V_{CCA}		Analog 5-V Power
GND		General Ground
GNDREG		Ground for Voltage Regulator
GNDA		Analog Ground

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description

The TMS38051 Ring Interface Transceiver and the TMS38052 Ring Interface Controller combine with passive components (Figure 1) to form a full duplex electrical interface compatible with IEEE Std 802.5-1985 Token Ring Access Method and Physical Layer Specifications. A 4 megabit per second Differential-Manchester-encoded data stream is received by the TMS38051 Ring Interface Transceiver and phase aligned using an on-chip phase-lock loop. Both the recovered clock and data are passed to the TMS38020 Protocol Handler for serial-to-parallel conversion. On transmit, the TMS38020 Protocol Handler provides the TMS38051 a TTL-level signal which is converted to the appropriate levels for transmission on the wiring media.

The TMS38052 contains the Voltage-Controlled Oscillator (VCO) for the Phase-Lock Loop (PLL), the phantom drive for control of relays contained within a Trunk-Coupling Unit (TCU), and error detection for wire faults in the cable connected to the TCU.

The TMS38051 and TMS38052, when coupled with the TMS38010 Communications Processor, the TMS38020 Protocol Handler, and the TMS38030 System Interface, form a highly integrated Token Ring LAN Adapter compatible with IEEE Std 802.5-1985 Token Access Method and Physical Layer Specifications.

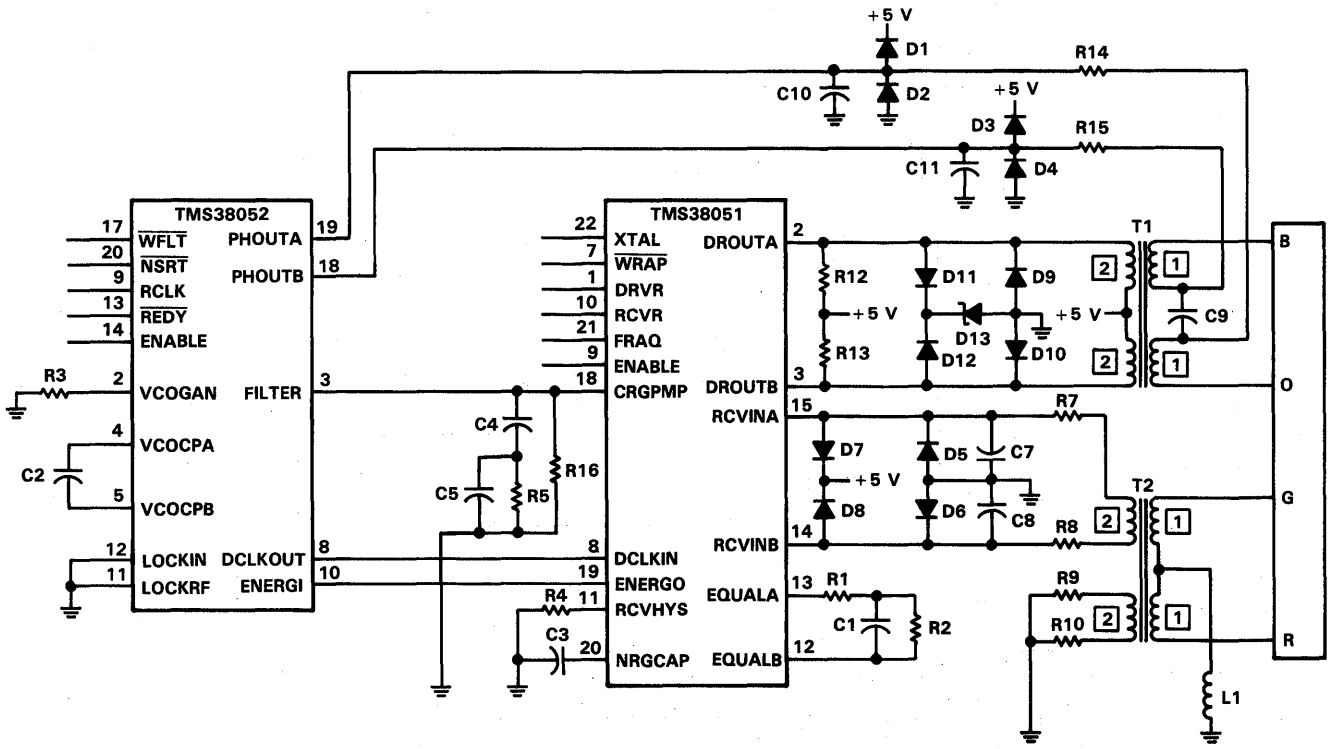

FIGURE 1. TOKEN RING INTERFACE CIRCUIT

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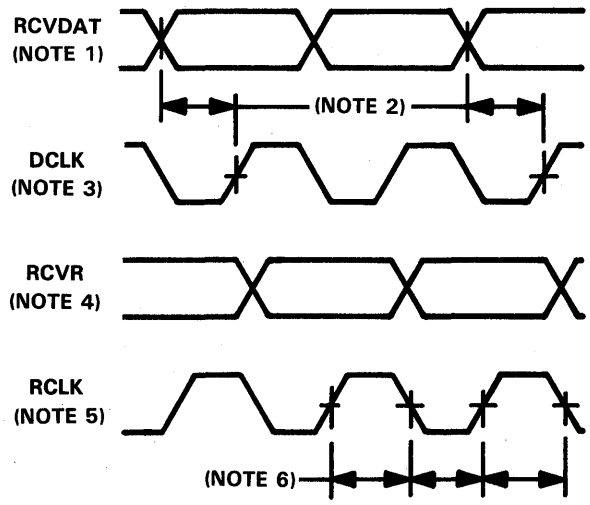
data buffer

The output of the receiver (the internal TMS38051 signal named RCVDAT) drives two internal circuits: a D-type flip-flop data buffer clocked by the VCO (DCLKIN) to sample the received data at the optimum time to generate the signal RCVR, and the phase detector used to control the VCO. RCVR is the retimed received data signal sent to the TMS38020 Protocol Handler for decoding of the Differential-Manchester-encoded data. RCLK is the clock used by the TMS38020 to sample RCVR. Logic state changes at RCVR occur at the rising edges of DCLK. Data is stable and may be sampled at the rising edges of RCLK. Data is delayed by the propagation delay of the receiver and data buffer plus one-half of an 8 MHz clock period from the receiver inputs to pin RCVR. The relative timing of these signals is indicated in Figure 2.

Static-timing offset is defined as the delay from a rising data transition (internally at RCVDAT) to the time data is sampled (rising transition at DCLKIN after buffering), minus 62.5 ns. At 4 megabits per second (8 MHz clock), an offset of zero is optimum sampling as this places the rising edge of the sampling clock in the middle of the data pulse. A positive offset represents late sampling.



NOTES: 1. Output of the receiver (internal signal derived from RCVIN pins)
2. PLL Static timing offset plus 62.5 ns
3. VCO clock to detectors and D-type flip-flop
4. Output of data buffer D-type flip-flop
5. Inverted clock to sample RCVR
6. Half clock period delays caused by internal latching.

FIGURE 2. RECEIVE DATA TIMING

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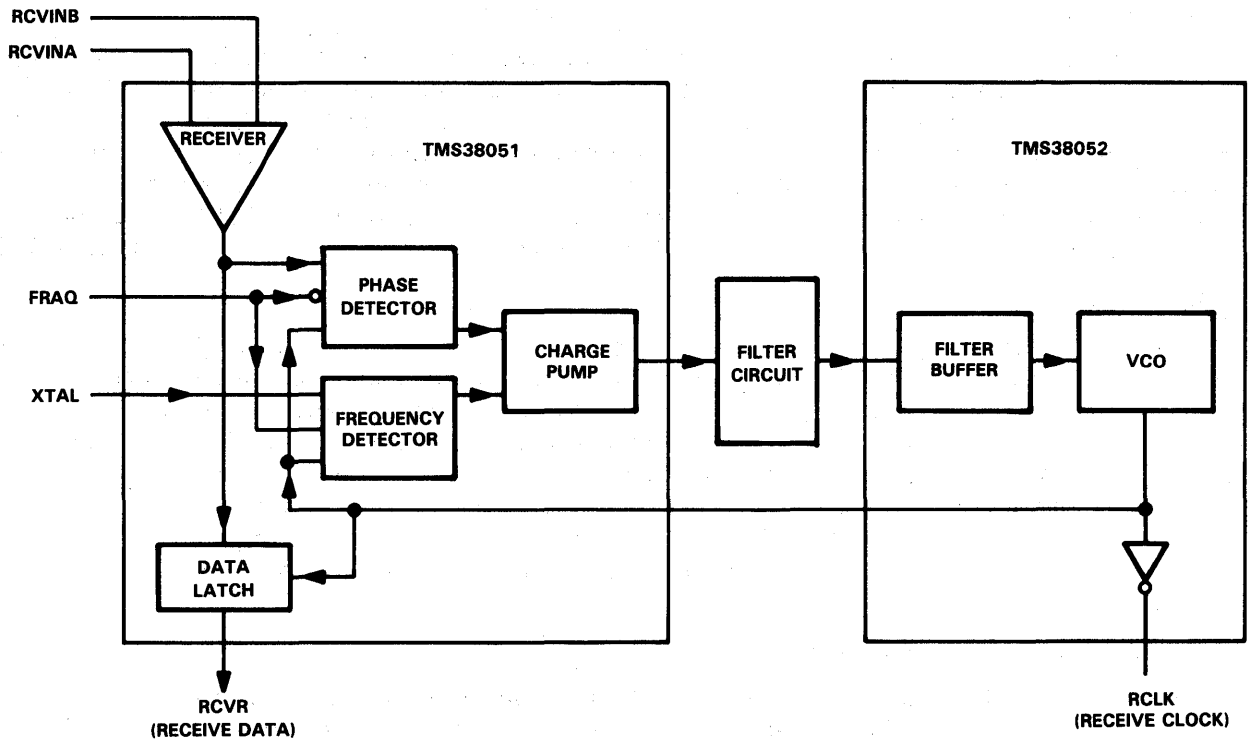

FIGURE 3. PHASE LOCK LOOP

phase and frequency detectors

The phase and frequency detectors are blocks of logic that generate control signals suitable for controlling the charge pump. The frequency detector will cause the voltage-controlled oscillator (VCO) frequency to be the same as the crystal-oscillator input, XTAL. The phase detector provides more accurate phase discrimination but could indicate a false lock where one frequency is a multiple of the other.

A multiplexer selects the required detection mode during insertion into the ring. The frequency-detection mode is selected by taking FRAQ high and the phase-detection mode is selected by taking FRAQ low. The phase or frequency detectors supply the necessary "charge" and "discharge" control signals to the charge pump. All gates not required for normal operation in either mode are prevented from switching to minimize the noise that might be coupled into the PLL.

charge pump

The output of either the phase detector or frequency detector drives the charge pump as selected by the FRAQ input. The charge pump drives the external filter (passive components R5, C4, and C5) and the filter-buffer input (FILTER). The charge pump has the ability to supply charge ("up" current into the filter) and to remove charge ("down" current out of the filter into the charge pump). A small amount of charge is required to provide the filter-buffer input current and any leakage in the external filter. Additional net charge affects the filter voltage. If the up current exceeds the down current, the voltage on the filter will increase, increasing the "controlled voltage" and the frequency of the VCO. The charge pump has two inputs so there are four possible states for the charge pump.

1. Pump up—current into the filter increasing the voltage.
2. Pump down—current out of the filter reducing the voltage.
3. No pump—high-impedance state, holding the voltage on the filter.
4. Pump up and pump down—both currents on, not allowed by the detector logic.

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4. In a transition from signal (at least 24 rising transitions in a 16 μs interval) to no signal (less than 3 rising transitions in 16 μs), the ENERGO transition time to a de-asserted state ($\overline{\text{REDY}}$ de-asserted) is 16 μs.

Note that for proper operation of the $\overline{\text{REDY}}$ output, the LOCKIN and LOCKRF pins must be tied together and grounded such that no more than ± 2 mV of differential signal occurs between these two pins.

test mode

The TMS38051 and TMS38052 feature a test mode for board-level testing with the components in circuit. This facilitates testing by board-of-nails testers. This test mode is enabled by tying the ENABLE pin to ground. This has the effect of driving all the TTL outputs and the phantom-drive outputs to a high-impedance state. The media-driver outputs (DROUTA and DROUTB) are not affected by this function. When the ENABLE pin is high, the TMS38051 and TMS38052 operate normally. When this pin is low, the circuit will continue to operate except that pins PHOUTA, PHOUTB, RCVR, $\overline{\text{WFLT}}$, RCLK and DCLKOUT are driven to the high-impedance state, and pin $\overline{\text{REDY}}$ is driven to the high state. Pin ENERGO is not affected by ENABLE.

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electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

TTL input

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	DRVR, $\overline{WRAP}$, ENABLE, FRAQ, XTAL, ENERGI, $\overline{NSRT}$, DCLKIN, FILTER	V_I = 2.7 V			20	μA
I_{IL}	Low-level input current	DRVR, $\overline{WRAP}$, ENABLE, FRAQ, XTAL, ENERGI, $\overline{NSRT}$, DCLKIN, FILTER	V_I = 0.4 V			−0.4	mA
V_{IK}	Input clamp voltage	DRVR, $\overline{WRAP}$, ENABLE, FRAQ, XTAL, ENERGI $\overline{NSRT}$, DCLKIN, FILTER	I_I = −12 mA			−1.5	V
I_I	Input current at maximum input voltage	DRVR, $\overline{WRAP}$, ENABLE, FRAQ, XTAL, $\overline{NSRT}$ DCLKIN, FILTER	V_I = 7 V			100	μA
		ENERGI	V_I = 5.5 V			100	μA

TTL output

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{WFLT}$, DCLKOUT	I_{OH} = −0.4 mA	2.5			V
		RCVR, RCLK	I_{OH} = −0.4 mA	2.8			V
		ENERGO, $\overline{REDY}$	I_{OH} = −0.1 mA	2.5			V
V_{OL}	Low-level output voltage	RVCR, $\overline{WFLT}$, RCLK, DCLKOUT, $\overline{REDY}$	I_{OL} = 4 mA			0.5	V
			I_{OL} = 1 mA			0.4	V
		ENERGO	I_{OL} = 0.5 mA			0.5	V
I_{OZH}	Off-state output current with high-level voltage applied	RCVR, $\overline{WFLT}$ RCLK, DCLKOUT	V_O = 2.7 V			100	μA
		$\overline{REDY}$				−1.5	mA
I_{OZL}	Off-state output current with low-level voltage applied	RCVR, $\overline{WFLT}$ RCLK	V_O = 0.4 V			−100	μA
		DCLKOUT		100		−600	μA
		$\overline{REDY}$				−1.5	mA
I_{OS}	Short-circuit output current	RCVR, $\overline{WFLT}$, RCLK, DCLKOUT	V_O = 0	−20		−100	mA
		ENERGO, $\overline{REDY}$		−0.5		−2	mA

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phantom driver

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	PHOUTA, PHOUTB	$I_{OH} = -1$ mA	4.1			V
			$I_{OH} = -2$ mA	3.8			V
I_{OS}	Short curcuit output current	PHOUTA, PHOUTB	$V_O = 0$, $\overline{NSRT} = V_{IL}$	−4		−20	mA
I_{OH}	High-level output current	PHOUTA, PHOUTB	$V_O = V_{CC}$, $\overline{NSRT} = V_{OH}$			100	μA
I_{OL}	Low-level output current	PHOUTA, PHOUTB	$V_O = 0$, $\overline{NSRT} = V_{IH}$			−100	μA
I_{OZH}	Off-state output current with high-level voltage applied	PHOUTA, PHOUTB	$V_O = 5.5$ V, ENABLE = V_{IL}			100	μA
I_{OZL}	Off-state output current with low-level voltage applied	PHOUTA, PHOUTB	$V_O = 0$, ENABLE = V_{IL}			−100	μA

wire fault (see Note 15)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output-normal condition	$\overline{WFLT}$	2.9 kΩ ≤ R_{L1} ≤ 5.5 kΩ, 2.9 kΩ ≤ R_{L2} ≤ 5.5 kΩ, See Note 16	2.5			V
Output-open condition	$\overline{WFLT}$	9.9 kΩ ≤ R_{L1}, 2.9 kΩ ≤ R_{L2} ≤ 5.5 kΩ, See Note 16			0.5	V
Output-short condition	$\overline{WFLT}$	R_{L1} ≤ 0.1 kΩ, 2.9 kΩ ≤ R_{L2} ≤ 5.5 kΩ, See Note 16			0.5	V

NOTES: 15. The wire-fault logic will recognize a load condition corresponding to greater than 9.9 kΩ to ground as an open-circuit fault, but will not recognize a load condition less than 5.5 kΩ to ground as an open. The wire-fault logic will recognize a load condition corresponding to less that 100 Ω to ground as a short-circuit fault, but will not recognize a load condition corresponding to greater than 2.9 kΩ to ground as a short. Figure 4 illustrates this with R_{L1} connected from PHOUTA to ground and R_{L2} connected from PHOUTB to ground.

16. R_{L1} is connected from pin 19 to ground; R_{L2} is connected from pin 18 to ground.

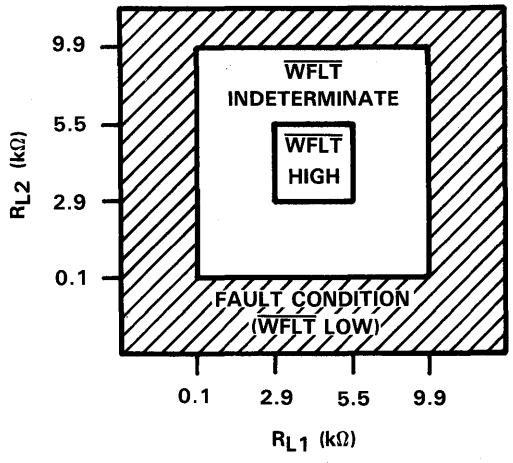

FIGURE 4. WIRE-FAULT PIN TEST

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filter buffer

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input current at FILTER	FILTER at 2 V – 3 V	–0.5		1.5	μA

energy detect

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage	NRGCAP	ENERGO low	0.5			V
V_{IH}	High-level input voltage	NRGCAP	ENERGO high			2	V
V_{HYS}	Energy detect hysteresis	NGRCAP	$V_{HYS} = V_{IH} = V_{IL}$	0.1			V
t_d	Delay time, ENERGI valid to $\overline{REDY}$ valid	ENERGI, REDY				1	μS

supply current

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	TMS38051	See Figure 7(a)			93	mA
			See Figure 7(a), V_{CC} = 5.5 V, t_c = 80°C			88	mA
		TMS38052	See Figure 7(b)			59	mA
			See Figure 7(b), V_{CC} = 5.5 V, t_c = 75°C			53	mA

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transmitter

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output rise time, t_r		DROUTA, DROUTB	$V_L = V_{CC}$, See Figures 9 and 11			20	ns
Output fall time, t_f						20	ns
Output asymmetry time, $t_A - t_B$		DROUTA, DROUTB	$V_L = V_{CC}$, See Figures 12 and 16			11	ns
Output skew time	$\frac{t_2 - t_1}{t_3 - t_4}$	DROUTA, DROUTB	$V_L = V_{CC}$, See Figures 12 and 16			5	ns

internal wrap

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_1	Signal-to-receiver voltage swing	DRVR = V_{IL} to V_{IH}, $\overline{WRAP}$ = V_{IL}, See Note 19 and Figures 8 and 9	150		500	mV
V_2	Noise signal voltage at driver	DRVR = V_{IL} to V_{IH}, $\overline{WRAP}$ = V_{IL}, See Note 20 and Figure 9			10	mV
t_{PHL}	Propagation delay, high-to-low-level output	DRVR = V_{IL} to V_{IH}, $\overline{WRAP}$ = V_{IL}, See Figures 9 and 15			45	ns
t_{PLH}	Propagation delay, low-to-high-level output	DRVR = V_{IL} to V_{IH}, $\overline{WRAP}$ = V_{IL}, See Figures 9 and 15			45	ns

NOTES: 19. Peak-to-peak voltage swing between EQUALA and EQUALB. The differential between RCVINA and RCVINB is held at 0.5 V to assure that the receiver signal does not affect wrap mode.
20. Peak-to-peak voltage swing between DROUTA and DROUTB. The differential between RCVINA and RCVINB is held at 0.5 V to assure that the receiver signal does not affect wrap mode.

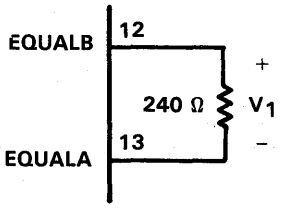

FIGURE 8

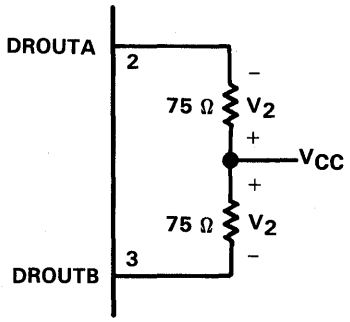

FIGURE 9

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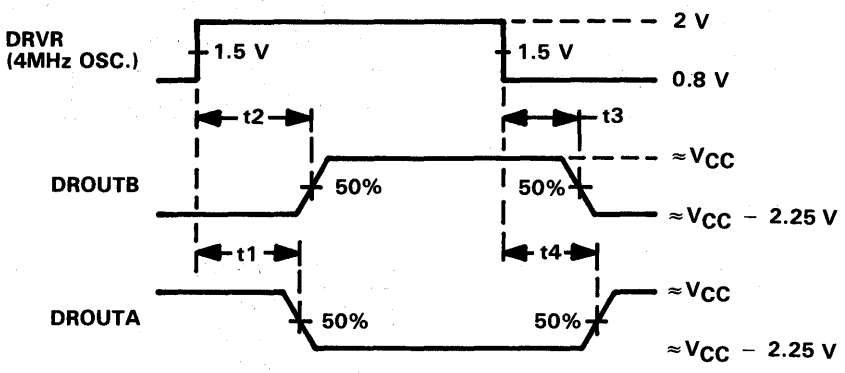

t_A	$\frac{t_1 + t_2}{2}$
t_B	$\frac{t_3 + t_4}{2}$

FIGURE 12. SKEW AND ASYMMETRY FROM DRVR TO DROUTA AND DROUTB

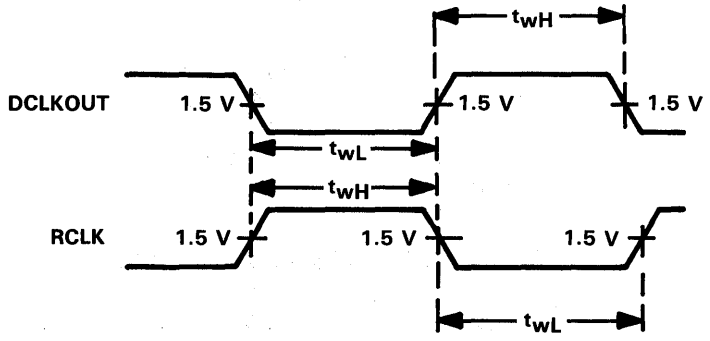

FIGURE 13. VCO ASYMMETRY

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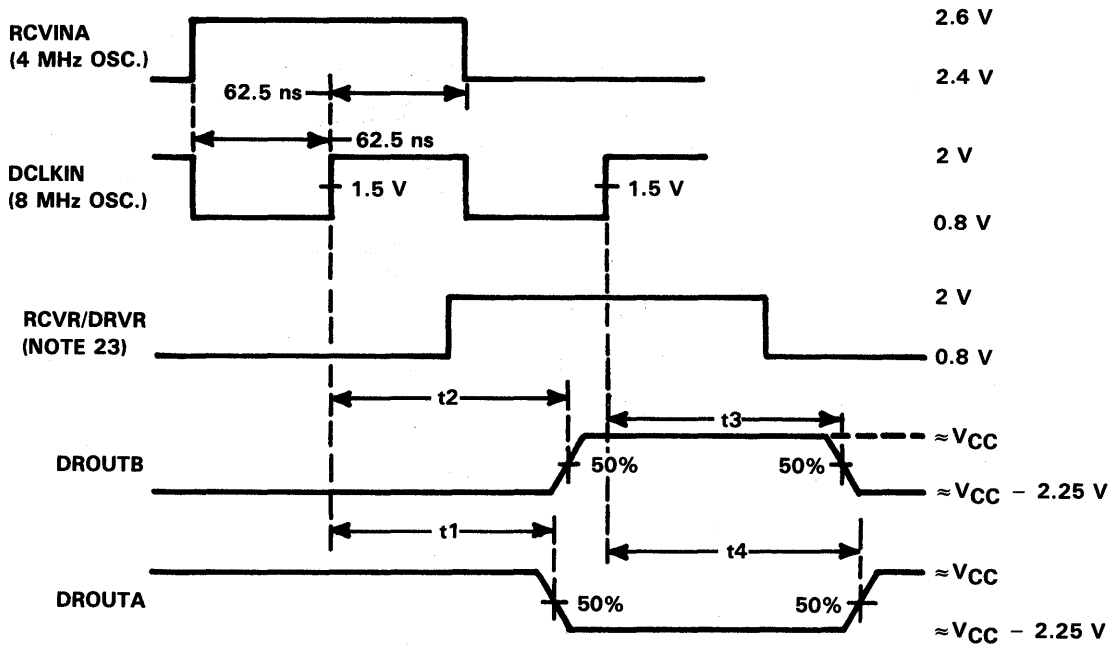

NOTE 23: For this test the RCVR output is tied directly to the DRVR input to test the asymmetry of the transmitter in a repeater configuration.

t_A	$\frac{t_1 + t_2}{2}$
t_B	$\frac{t_3 + t_4}{2}$

FIGURE 16. SKEW AND ASYMMETRY FROM DCLKIN TO DROUTA AND DROUTB

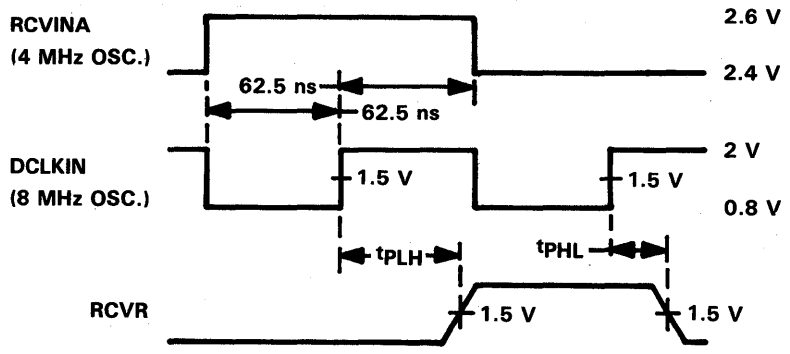

FIGURE 17. PROPAGATION DELAYS FROM DCLKIN TO RCVR

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TABLE B-1. MAC FRAME MAJOR VECTORS (continued)

M-V CMD	M-V (FRAME) NAME AND XMIT TYPE	DESTINATION CLASS	SOURCE CLASS	DESTINATION ADDRESS	SUBVECTORS		
					R/O		NAME
					XMT	RCV	
>05	Active Monitor Present (AMP) FC = >05	>0	>0	All Stations	A A	O R	Phys. Drop Number UNA
>06	Standby Monitor Present (SMP) (Type = Resp.) FC = >06	>0	>0	All Stations	A A	O R	Phys. Drop Number UNA
>07	Duplicate Address Test (Type = Orig.)	>0	>0	Target			None
>08	Lobe Media Test (Type = Orig.)	>0	>0	Zero	A	N	Wrap Data
>09	Transmit Forward	>0	any	Target		R	Frame Forward
>0B	Remove Ring Station FC = >01	>0	>4	Target			None
>0C	Change Parameters (ACK)	>0	>4	Target		O O O O O O	Correlator Local Ring Number Assign Phys. Drop Number Soft Error Report Timer Value Enabled Function Classes Allowed Access Priority

TABLE B-1. MAC FRAME MAJOR VECTORS (concluded)

M-V CMD	M-V (FRAME) NAME AND XMIT TYPE	DESTINATION CLASS	SOURCE CLASS	DESTINATION ADDRESS	SUBVECTORS		
					R/O		NAME
					XMT	RCV	
>24	Report Station Attachment (Type = Resp.)	>4	>0	Source Address of Received Request Frame	A A A A A		Correlator Product ID Functional Address Authorized Function Class Authorized Access Priority
>25	Report New Monitor (Type = Orig.)	>4	>0	F(NM)	A A A		Phys. Drop Number UNA Product ID
>26	Report SUA Change (Type = Resp.)	>4	>0	F(NM)	A A		Phys. Drop Number UNA
>27	Report Ring Poll Failure (Type = Orig.) FC = >01	>6	>0	F(REM)	A		Address of Last Ring Poll
>28	Report Monitor Error (Type = Orig.)	>6	>0	F(REM)	A A A		Physical Drop No. UNA Error Code: -Monitor Error -Duplicate Monitor -Duplicate Address
>29	Report Error (Type = Orig.)	>6	>0	F(REM)	A A A A		Physical Drop No. UNA Isolating Error Counts Non-isolating Error Counts
>2A	Report Transmit Forward	>4	>0	F(NM)	A		Transmit Status Code

TABLE B-2. MAC FRAME SUBVECTORS (concluded)

TYP	LEN†	SUBVECTOR NAME	VALUE
>23	>0C	Adapter Software Level	Level of the sending Adapter's software. Bytes 0-4: Feature Code Bytes 5-9: EC Level
>26	>xx	Wrap Data	Wrap Data (xx = variable length)
>27	>xx	Frame Forward	Frame to be forwarded. Includes: Access Control through last information byte.
>29	>08	Adapter Status Vector	Indication of the current state of the sending Adapter's software. (note 1)
>2A	>04	Transmit Status Code	Code indicating the strip status of a transmitted frame.
>2B	>06	Group Address	Group Address set in sending station. (Zero if not set)
>2C	>06	Functional Address	Functional Address Field set in the sending station.
>2D	>08	Isolating Errors	Byte 0 - Line Error 1 - Reserved 2 - Burst Error 3 - ARI/FCI Error 4 - Reserved 5 - Reserved
>2E	>08	Non-isolating Errors	Byte 0 - Lost Frame 1 - Receive Congestion 2 - Frame Copied Error 3 - Reserved 4 - Token Error 5 - Reserved
>30	>04	Error Code	Error Code defining the error condition. >0001 - Monitor Error >0002 - Duplicate Monitor >0003 - Duplicate Address

†Length in bytes of subvector value.

B.2 Burned-In Addressing Technique

This section describes the technique for programming a 512 x 4 PROM with a burned-in address. This address provides the Adapter with a 48-bit node address if a node address is not passed during the OPEN commamd.

B.2.1 Burned-in Address Format

The burned-in address must conform to that shown in the figure below. Note that bits 0 and 1 of byte 0 must be 01 as shown. If the burned-in address does not conform to this requirement, the OPEN command is abnormally terminated with a node address error.

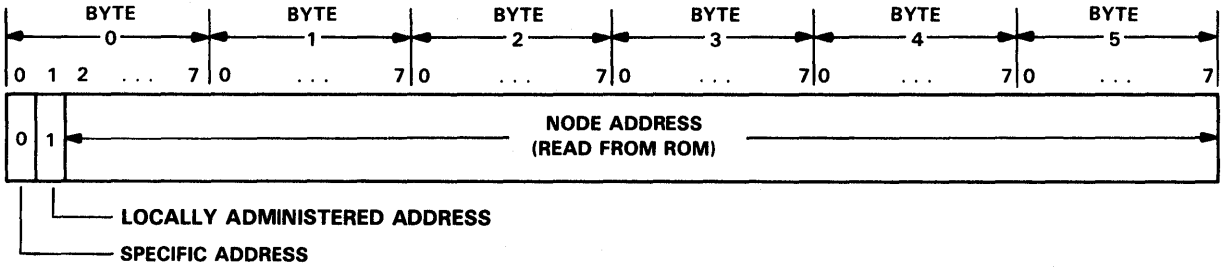


FIGURE B-1. BURNED-IN ADDRESS FORMAT

B.2.3 BIA Operation

Locating the Adapter's node address in ROM is called "burned-in addressing" because the address is non-changeable being "burned" into an on-board PROM. The PROM may be visualized as vertical columns with the address "burned" into the column connected to the Q2 output of the PROM. The columns of bits at Q3 and Q4 are programmed to all ones as these outputs are not connected to any external circuitry. Column Q1 is fed back to the serial inputs of the shift register to create the seven low-order address bits for the PROM.

When the TMS38020 Protocol Handler holds the $\overline{\text{NSRT}}$ signal low, the address to the PROM is held to the first 256 locations of the PROM. As can be seen in Table B-1, no burned-in address bits are encoded in the first 256 locations. When the $\overline{\text{WFLT}}$ line from the Ring Interface is low and the $\overline{\text{NSRT}}$ signal is low, the value returned to the Protocol Handler is zero (wire fault condition). When the $\overline{\text{WFLT}}$ line from the Ring Interface is high and $\overline{\text{NSRT}}$ is low, the $\overline{\text{WFLT}}$ value returned to the Protocol Handler is high. Thus, when the Ring Interface is in an insert state ($\overline{\text{NSRT}}$ is low), the value of $\overline{\text{WFLT}}$ from the Ring Interface is directly reflected to the Protocol Handler.

Whenever the Adapter is initialized, the TMS38010 Communications Processor will fetch the burned-in address from the BIA PROM. If the node address passed to the Adapter during the OPEN command is zero, the burned-in address will be used as the Adapter's Ring Station Address.

The Adapter software is configured to test to determine the presence of the burned-in address circuitry during each initialization sequence. This is done by attempting to read the PROM. The software provides a check to determine if the data represents the correct coding for a burned-in address PROM. It does not check the correctness of the address itself. An error in the address itself will cause the OPEN command to terminate with a node address error.

When this routine is executed, the Adapter is not inserted in the ring so $\overline{\text{NSRT}}$ is inactive-high. Thus, only the second 256 locations of the PROM will be addressed. Since during this time the $\overline{\text{WFLT}}$ line status is a "don't care" condition, the burned-in address and validation code must be put into the PROM twice. In Table B-1, two addresses are shown for each entry because of this condition.

B.2.4 PROM Address Programming

The Communications Processor reads the BIA through the Protocol Handler signal line $\overline{\text{WFLT}}$. Because this is an inverted input, the data outputs of the PROM must be inverted from their intended value for the address bits. The following table describes the content requirements for the BIA PROM.

TABLE B-3. BURNED-IN ADDRESS CONTENTS (2 of 5)

DECIMAL ADDR	PROM BINARY ADDRESS									ADDRESS SEQ	BURNED IN ADDRESS BIT	PROM OUTPUT				HEX OUTPUT
	A8	A7	A6	A5	A4	A3	A2	A1	A0			O4	O3	O2	O1	
	–	–	+	+	+	+	+	+	+					–	+	
			S	S	S	S	S	S	S			N	N	N	S	
			R	R	R	R	R	R	R			O	O	E	E	O
	N	W										T	T	W	R	U
	S	F	Q_G	Q_F	Q_E	Q_D	Q_C	Q_B	Q_A						I	T
	R	L										U	U	W	A	P
	T	T										S	S	F	L	U
												E	E	L		T
												D	D	T	A	
															D	
															R	
280/408	1	X	0	0	1	1	0	0	0	96	BIA47	1	1		0	
281/409	1	X	0	0	1	1	0	0	1	92	BIA43	1	1		1	
282/410	1	X	0	0	1	1	0	1	0	48	$\overline{\text{BIA47}}$	1	1		0	
283/411	1	X	0	0	1	1	0	1	1	75	BIA26	1	1		1	
284/412	1	X	0	0	1	1	1	0	0	102	CONST-0	1	1	0	0	C
285/413	1	X	0	0	1	1	1	0	1	59	BIA10	1	1		1	
286/414	1	X	0	0	1	1	1	1	0	108	CONST-0	1	1	0	0	C
287/415	1	X	0	0	1	1	1	1	1	114	CONST-0	1	1	0	0	C
288/416	1	X	0	1	0	0	0	0	0	87	BIA38	1	1		1	
289/417	1	X	0	1	0	0	0	0	1	52	BIA3	1	1		0	
290/418	1	X	0	1	0	0	0	1	0	23	$\overline{\text{BIA22}}$	1	1		1	
291/419	1	X	0	1	0	0	0	1	1	72	BIA23	1	1		0	
292/420	1	X	0	1	0	0	1	0	0	84	BIA35	1	1		0	
293/421	1	X	0	1	0	0	1	0	1	18	$\overline{\text{BIA17}}$	1	1		0	
294/422	1	X	0	1	0	0	1	1	0	46	$\overline{\text{BIA45}}$	1	1		1	
295/423	1	X	0	1	0	0	1	1	1	57	BIA8	1	1		0	
296/424	1	X	0	1	0	1	0	0	0	21	$\overline{\text{BIA20}}$	1	1		1	
297/425	1	X	0	1	0	1	0	0	1	16	$\overline{\text{BIA15}}$	1	1		0	
298/426	1	X	0	1	0	1	0	1	0	7	$\overline{\text{BIA6}}$	1	1		1	
299/427	1	X	0	1	0	1	0	1	1	9	$\overline{\text{BIA8}}$	1	1		0	
300/428	1	X	0	1	0	1	1	0	0	27	$\overline{\text{BIA26}}$	1	1		1	
301/429	1	X	0	1	0	1	1	0	1	11	$\overline{\text{BIA10}}$	1	1		0	
302/430	1	X	0	1	0	1	1	1	0	33	$\overline{\text{BIA32}}$	1	1		1	
303/431	1	X	0	1	0	1	1	1	1	39	$\overline{\text{BIA38}}$	1	1		0	
304/432	1	X	0	1	1	0	0	0	0	97	CONST-0	1	1	0	1	D
305/433	1	X	0	1	1	0	0	0	1	67	BIA18	1	1		0	
306/434	1	X	0	1	1	0	0	1	0	29	$\overline{\text{BIA28}}$	1	1		1	
307/435	1	X	0	1	1	0	0	1	1	93	BIA44	1	1		0	

TABLE B-3. BURNED-IN ADDRESS CONTENTS (4 of 5)

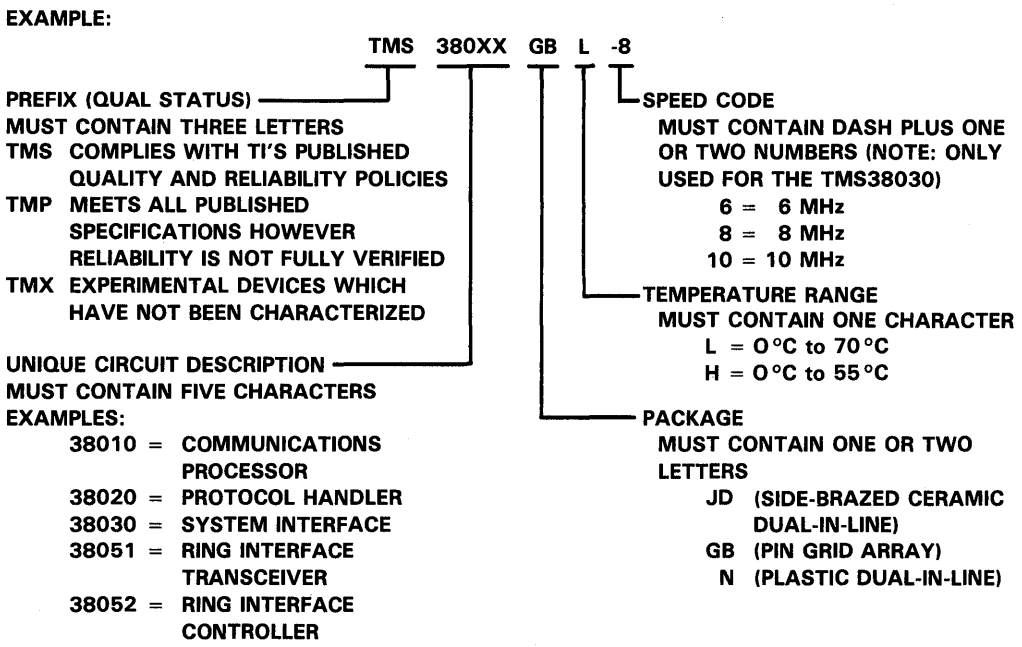
DECIMAL ADDR	PROM BINARY ADDRESS									ADDRESS SEQ	BURNED IN ADDRESS BIT	PROM OUTPUT				HEX OUTPUT
	A8	A7	A6	A5	A4	A3	A2	A1	A0			O4	O3	O2	O1	
	–	–	+	+	+	+	+	+	+					–	+	
			S	S	S	S	S	S	S			N	N	N	S	
			R	R	R	R	R	R	R			O	O	E	E	O
	N	W										T	T	W	R	U
	S	F	Q_G	Q_F	Q_E	Q_D	Q_C	Q_B	Q_A						I	T
	R	L										U	U	W	A	P
A	T	T								S		S	S	F	L	U
D										E		E	E	L		T
D										Q		D	D	T	A	
R															D	
															D	
															R	
335/463	1	X	1	0	0	1	1	1	1	113	CONST-0	1	1	0	1	D
336/464	1	X	1	0	1	0	0	0	0	51	BIA2	1	1		1	
337/465	1	X	1	0	1	0	0	0	1	22	$\overline{\text{BIA21}}$	1	1		0	
338/466	1	X	1	0	1	0	0	1	0	17	$\overline{\text{BIA16}}$	1	1		1	
339/467	1	X	1	0	1	0	0	1	1	45	$\overline{\text{BIA44}}$	1	1		0	
340/468	1	X	1	0	1	0	1	0	0	15	$\overline{\text{BIA14}}$	1	1		1	
341/469	1	X	1	0	1	0	1	0	1	8	$\overline{\text{BIA7}}$	1	1		1	
342/470	1	X	1	0	1	0	1	1	0	10	$\overline{\text{BIA9}}$	1	1		1	
343/471	1	X	1	0	1	0	1	1	1	38	$\overline{\text{BIA37}}$	1	1		1	
344/472	1	X	1	0	1	1	0	0	0	66	BIA17	1	1		1	
345/473	1	X	1	0	1	1	0	0	1	28	$\overline{\text{BIA27}}$	1	1		0	
346/474	1	X	1	0	1	1	0	1	0	12	$\overline{\text{BIA11}}$	1	1		1	
347/475	1	X	1	0	1	1	0	1	1	63	BIA14	1	1		0	
348/476	1	X	1	0	1	1	1	0	0	78	BIA29	1	1		1	
349/477	1	X	1	0	1	1	1	0	1	34	$\overline{\text{BIA33}}$	1	1		0	
350/478	1	X	1	0	1	1	1	1	0	40	$\overline{\text{BIA39}}$	1	1		1	
351/479	1	X	1	0	1	1	1	1	1	120	CONST-0	1	1	0	1	D
352/480	1	X	1	1	0	0	0	0	0	127	CONST-0	1	1	0	0	C
353/481	1	X	1	1	0	0	0	0	1	98	CONST-0	1	1	0	1	D
354/482	1	X	1	1	0	0	0	1	0	68	BIA19	1	1		0	
355/483	1	X	1	1	0	0	0	1	1	105	CONST-0	1	1	0	1	D
356/484	1	X	1	1	0	0	1	0	0	81	BIA32	1	1		1	
357/485	1	X	1	1	0	0	1	0	1	30	$\overline{\text{BIA29}}$	1	1		1	
358/486	1	X	1	1	0	0	1	1	0	94	BIA45	1	1		0	
359/487	1	X	1	1	0	0	1	1	1	112	CONST-0	1	1	0	1	D
360/488	1	X	1	1	0	1	0	0	0	50	BIA1	1	1		0	
361/489	1	X	1	1	0	1	0	0	1	44	$\overline{\text{BIA43}}$	1	1		1	
362/490	1	X	1	1	0	1	0	1	0	14	$\overline{\text{BIA13}}$	1	1		0	

B.3 Ordering Information, Package, Thermal and Mechanical Data

B.3.1 Ordering Instructions

Electrical characteristics presented in the data sheets in this publication, unless otherwise noted, apply for the circuit type listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this publication should include either a four-part or five-part number as explained in the following example.

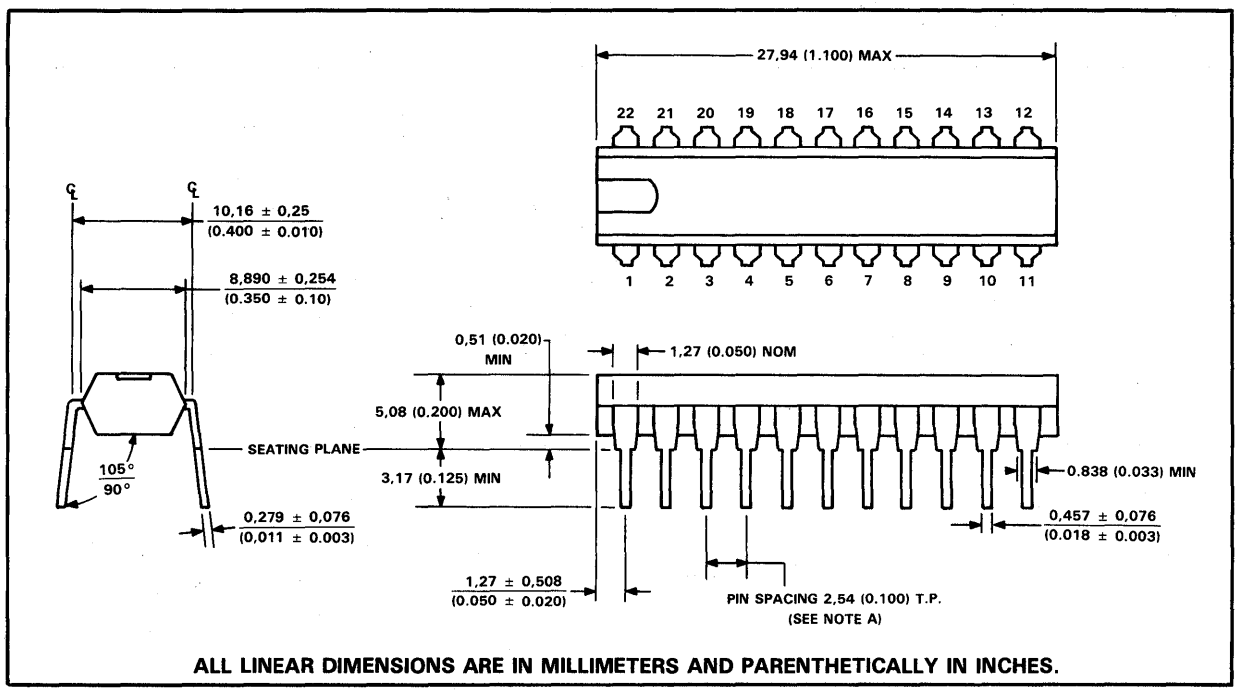


NOTE: The TMS38020 will include a ROM code level designator. (RC _ _ _ _).

B.3.2 Thermal Impedance Characteristics

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20-pin dual-in-line plastic package	76.6	33.0
22-pin dual-in-line plastic package	73.7	25.6
48-pin dual-in-line ceramic side-brazed package	40.5	8.8
100-pin pin grid array ceramic package	35.2	6.0

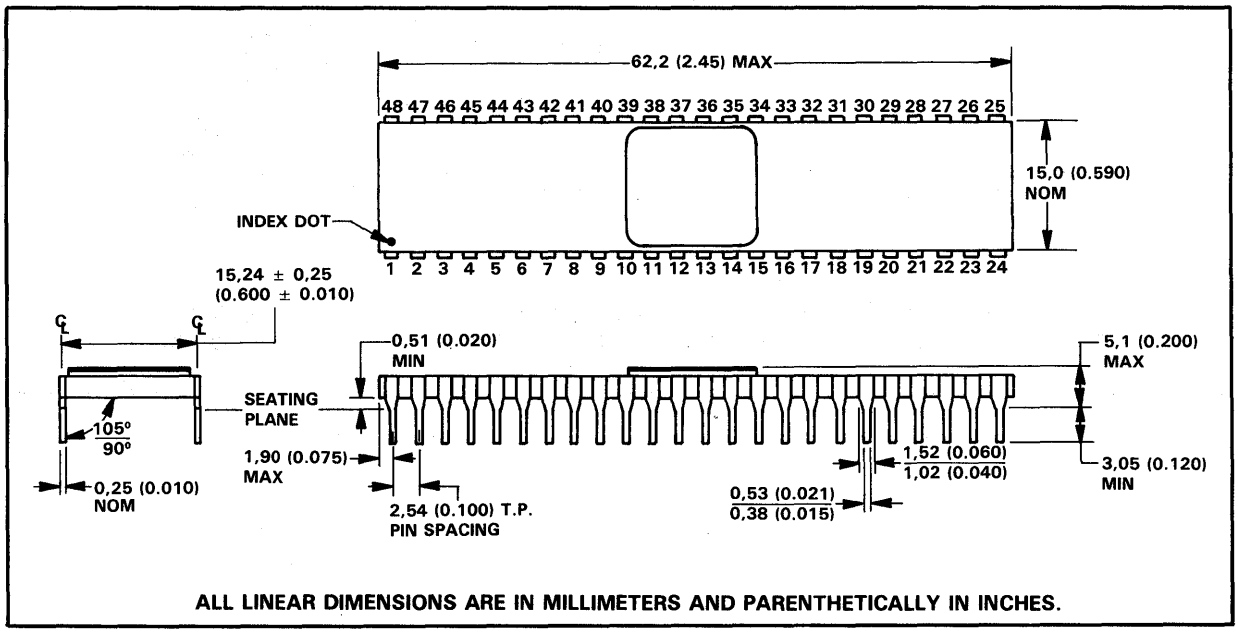
B.3.3.2 22-Pin Dual-in-Line Package (N Suffix)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

NOTE A: Each pin centerline is located within 0,25(0.010) of its true longitudinal position.

B.3.3.3 48-Pin Dual-in-Line Side-Brazed Package (JD Suffix)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

B.4 Glossary of Terms

ACCESS CONTROL
The Access Control (AC) field of a frame or token is the first octet of the Physical Control field. The AC contains the Priority Indicator (PI), Token Indicator (TI), Monitor Count (MC) and Priority Reservation (PR) fields of the frame or token.

ACCESS PRIORITY
The access priority of a frame enqueued for transmission is the maximum priority level of token that the Adapter will capture for transmission.

ACTIVE MONITOR
The active monitor is the Adapter responsible for providing clocking to the ring and other functions such as token error detection and recovery.

ADAPTER
The term "Adapter" refers to the Texas Instruments chip set consisting of the TMS38010 Communications Processor, TMS38020 Protocol Handler, TMS38030 System Interface, and TMS38051 and TMS38052 Ring Interface components.

ADAPTER SOFTWARE
Adapter software is software executed by the TMS38010 Communications Processor. This software provides IEEE 802.5 compatible Medium Access Control (MAC) services, network management support, and Adapter diagnostics. This software is in the ROM of the TMS38020 Protocol Handler.

ADDRESS
The logical location of a terminal, a peripheral device, node or any other unit or component in a network.

APPLICATION LAYER
A logical entity of the OSI model; the top of the seven-layer structure, generally regarded as offering an interface to, and largely defined by, the network user.

ATTACHED SYSTEM/ATTACHING PRODUCT
The attached system is the product which uses the Adapter to connect to the ring network; also referred to as the attaching product or the host system.

ATTENTION MAC FRAMES
Attention MAC frames are MAC frames received by the Adapter in which the attention field of the Frame Control field (FC) (bits 4-7) is greater than one. This condition causes an attention interrupt within the Adapter.

ATTENUATION
The difference (loss) between transmitted and received power, due to transmission loss through equipment lines or other communications devices.

ALLOWED ACCESS PRIORITY
The Allowed access priority is the highest access priority an attaching product may use when requesting a transmission.

ENABLED FUNCTION CLASSES
The Enabled Function Classes are the source classes a station is allowed to use in the transmission of MAC frames. These are the transmit Medium Access Control frames which may be passed from the attaching product to the Adapter for transmission.

BANDWIDTH
The range of frequencies that can pass over a given circuit. Generally, the greater the bandwidth, the more information that can be sent through the circuit in a given amount of time.

ERROR DETECTION
Code in which each data signal conforms to specific rules of construction so that departures from this construction in the received signals can be automatically detected.

FIBER OPTICS
A technology that uses light as an information carrier. Fiber optic cables are a direct replacement for conventional coaxial cable and wire pairs. The glass-based transmission facility occupies less physical volume for an equivalent transmission capacity, and the fibers are immune to electrical interference.

FLOW CONTROL
The capability of network nodes to manage buffering schemes in order to allow devices of differing data transmission speeds to communicate with each other.

FRAME
A collection of bits that contain both control information and data; the basic unit of transmission on a network. Control information is carried in the frame with the data to provide for such functions as addressing, sequencing, flow control and error control to the respective protocol levels. Can be of fixed or variable length.

FRAME CHECK SEQUENCE
The Frame Check Sequence (FCS) is a 32-bit field which follows the information field of a frame. This field contains a CRC value used to verify error-free transmission of the frame.

FRAME CONTROL
The Frame Control (FC) field of a frame or token is the second octet of the Physical Control field. The FC contains bits which define the frame as a MAC or non-MAC frame and the MAC frame attention code. This field is used by the TMS38020 Protocol Handler for frame processing.

FRAME FORMAT
The exact order and size of the various control and information fields of a frame, including header, address and data fields.

FRAME OVERHEAD
A measure of the ratio of the total frame bits occupied by control information to the number of bits of data, usually expressed as a percent.

FRAME STATUS
The Frame Status (FS) field of a frame is an octet appended after the ending delimiter of a frame which is used to indicate whether the destination address was recognized and whether the frame had been copied by the destination Adapter. This field is neither code-violation nor CRC-protected.

FUNCTIONAL ADDRESS
A form of group address which provides a "well known" address for network functions such as active monitor, ring error monitor, etc. Up to 31 unique functional addresses can be recognized by the TMS380 LAN Adapter.

GATEWAY
A special node that interfaces two or more dissimilar networks, providing protocol translation between the networks. A gateway is needed to connect two independent local area networks or to connect a local network to a long-haul network.

GROUP ADDRESS
An address which may be recognized by more than one node on the ring. A group address may be used for functions such as disk servers.

NETWORK
An interconnected group of nodes; a series of points, nodes, or stations connected by communications channels; the assembly of equipment through which connections are made between data stations.

NETWORK LAYER
In the ISO OSI Reference Model, the logical network entity that services the Transport layer; responsible for ensuring that data passed to it from the Transport layer is routed and delivered through the network.

NETWORK MANAGEMENT
Administrative services performed in managing a network, such as network topology and software configuration, downloading of software, monitoring network performance, maintaining network operations, and diagnosing and troubleshooting problems.

NETWORK MANAGER
A network entity which determines station status, collects configuration information, and measures network performance, among other things.

NODE
A station; a physical device that allows for the transmission of data within a network.

OPEN SYSTEMS INTERCONNECTION
OSI. Referring to the International Organization for Standardization's OSI Reference Model, a logical structure for network operations standardized within the ISO; a seven-layer network architecture being used for the definition of network protocol standards.

PHYSICAL CONTROL FIELD
PCF. The physical control field (PCF) is a field of a frame which follows the starting delimiter. The PCF consists of two 8-bit fields, the Access Control (AC) field and the Frame Control (FC) field.

PHYSICAL DROP NUMBER
The physical drop number is a facilities-defined number used to assist in performing network management functions. The physical drop number is provided to individual stations by a Ring Parameter Server or Network Manager if present on the ring.

PHYSICAL LAYER
In the OSI Reference Model the lowest level of network processing, below the Data Link layer, that is concerned with the electrical, mechanical and handshaking procedures over the interface that connects a device to a transmission medium; referring to an electrical interface, such as RS-232-C.

PRESENTATION LAYER
In the OSI Reference Model, that layer of processing that provides services to the Application layer, allowing it to interpret the data exchanged, and allowing it to structure data messages to be transmitted in a specific display and control format.

PROTOCOL
Formal set of rules governing the format, timing, sequencing, and error control of exchanged messages on a data network; may also include facilities for managing a communications link and/or contention resolution. A protocol may be oriented toward data transfer over an interface, between two logical units directly connected, or on an end-to-end basis between two end users over a large and complex network. Both hardware protocols and software protocols can be defined.

SERIAL INTERFACE
An interface which requires serial transmission, or the transfer of information in which bits composing a character are sent sequentially. Implies a single transmission channel.

SERVER
A processor which provides a specific service to the network. Examples of servers are: routing server - connects nodes and networks of like architectures; gateway server - connects nodes and networks of different architectures by performing protocol conversions; terminal server, print server and file server - provides an interface between compatible peripheral devices on a LAN.

SESSION
A connection between two stations that allows them to communicate; the logical connection between two network addressable units.

SESSION LAYER
In the OSI Reference Model, the network-processing layer responsible for binding and unbinding logical links between end users and maintaining an orderly dialogue between them; also responsible for naming of logical entities.

SOURCE
Originator of data.

SOURCE ROUTING
Method by which stations are addressed across multiple rings.

STAND-BY MONITOR
A stand-by monitor is any Adapter on the ring which is not currently the Active Monitor. The stand-by monitor functions are defined in the MAC protocol.

STAR
A network topology consisting of one central node with point-to-point links to several other nodes. Control of the network is usually located in the central node or switch, with all routing of network message traffic performed by the central node.

STATION
A network node.

SUBVECTOR
A subvector is part of the MAC frame Major Vector. The subvectors are subfields within the Major Vector used to carry specific information used to process the MAC frame. The subvector is composed of length, type, and value fields.

SYSTEM COMMAND BLOCK
The System Command Block (SCB) is a six-byte buffer used to hold the command to be executed by the Adapter and a 24-bit address pointer to a parameter block for the command.

SYSTEM INTERFACE
The TMS38030 System Interface (SIF) is a VLSI component of the Adapter chip set which functions as the Adapter's interface to the attached system.

SYSTEM STATUS BLOCK
The System Status Block (SSB) is an eight-byte buffer used by the Adapter to relay status information to the attached system, such as return codes of completed Adapter commands.

THROUGHPUT
The total useful information processed or communicated during a specified time period. Expressed in bits per second or bytes per second.

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