A Texas Instruments Application Report

MONOLITHIC INTERFACING IN COMPUTERS

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Abstract

The role of linear integrated circuits in computer applications is primarily that of interface. This paper discusses some of the newest circuits available to serve this market segment. Because of the broad scope of the market, this discussion is limited to three active areas–line circuits, memory drivers, and sense circuits. Representative circuits from each of these areas are used for illustration purposes.

1. INTRODUCTION

In the ten year history of the integrated circuit, most applications have been in the logic sections of digital computers. This was due to several factors–familar discrete logic circuits were readily translatable into integrated form because of their simplicity, low voltage and current requirements, and because of the highly repetitive usage of such circuits.

Some early attempts were made to implement other computer-system functions such as memory and peripheral circuits. The first really successful computer-system interface circuits were incorporated in the Minuteman II computer in early 1963 to perform the read/write and input/output functions. Since that time, improved IC techniques, processes, production capabilities, and circuit-design techniques have resulted in more attention to this market.

Computer-system interface circuits, Figure 1, hold the promise of being the next major market to be highly penetrated by the IC revolution. High performance circuits are now becoming available to satisfy the requirements of this market. This paper explores three areas of interest–line circuits, memory drivers, and sense circuits. Representative circuits from each area are used for purposes of illustration.

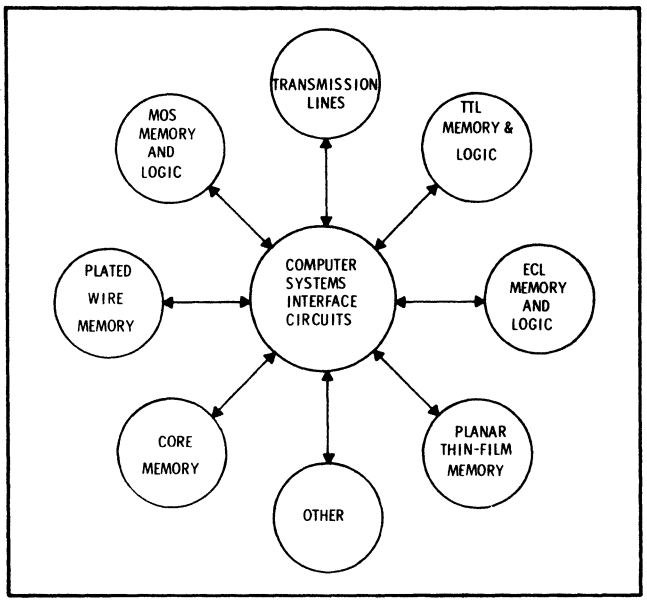

Figure 1 – Systems Interface Circuits Applications

2. LINE CIRCUITS

The noise margins of most logic circuits are adequate for the transmission of digital data over a distance of a few inches. The transmission of error-free data over longer lines in noisy environments, however, requires the use of special transmission-line drivers and receivers and the careful selection of a suitable transmission line. This is especially true when data transmission is between computer consoles or between a computer and remotely located peripheral equipment.

A study of the problem of data transmission indicates that the use of a terminated transmission line is desirable from a performance standpoint, since signal reflections are eliminated, allowing high-speed data transmission. A balanced or two-wire

system is desirable because system noise is primarily common-mode and can be rejected by a differential-input line receiver with adequate common-mode rejection properties.

Depending on the length of the transmission line, the costs of the line and of its installation can be influencing factors in the selection of the line. For short transmission lines, the use of relatively expensive shielded coaxial cable may be acceptable. For longer lines, however, the use of less expensive flat or twisted-pair cable is desirable. To further decrease the cost of a transmission system, a "party-line" system may be employed in which several line drivers and receivers share a common transmission line.

A suitable high-speed driver/receiver/line system designed for use with long transmission lines is almost universal since it can also be used to advantage with shorter lines or for low-speed data transmission. The following characteristics are desirable for such a system:

(1) High speed data transmission (> 10 MHz)

(2) Use of popular supply voltages

(3) Compatibility with popular logic

(4) High sensitivity (< 50 mV) at receiver input

(5) Receiver speed insensitive to overdrive

(6) High receiver input impedances

(7) High common-mode rejection at the receiver input

(8) Strobe capability for receiver

(9) Driver capable of driving low-impedance terminated lines

(10) Inhibit capability for driver, high output impedance in inhibit mode

A system satisfying these requirements is shown in the functional diagram of Figure 2. A balanced, twisted-pair transmission line is terminated at each extreme end in its characteristic impedance. The line terminations also bias both lines at a nominal positive level of a few hundred millivolts. The driver is composed of a stage that converts input logic levels to voltage levels that control a current switch. The current switch unbalances the voltage on the transmission lines resulting in a difference voltage at the receiver input.

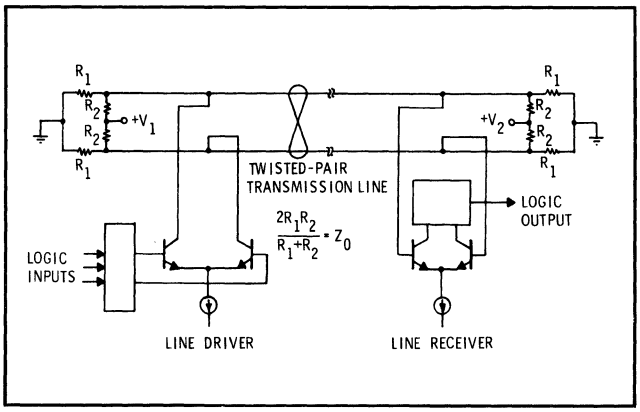

Figure 2 – A Basic High Speed Transmission System

The input stage of the receiver is a differential-input stage that exhibits high rejection of common-mode input signals. Intermediate stages convert the polarity of the input signal to the desired logic levels at the receiver output. It should be noted that the driver output is capable of rejecting common-mode signals induced on the line, thereby insuring error-free transmission and recovery of data.

An important feature of the system of Figure 2 is that provisions can be made for removing the driver output current from both lines. In this inhibit mode, another driver may be used to transmit data over the line. A strobe or gate provision on the receivers allows any driver to communicate with any or all enabled receivers while other drivers are inhibited and other receivers are strobed off. This system is shown in Figure 3. Line receivers and drivers may be connected anywhere along the line. It should be noted that line terminations are required only at the extreme ends of the lines. A single transmission line can therefore service several computer or peripheral equipment consoles.

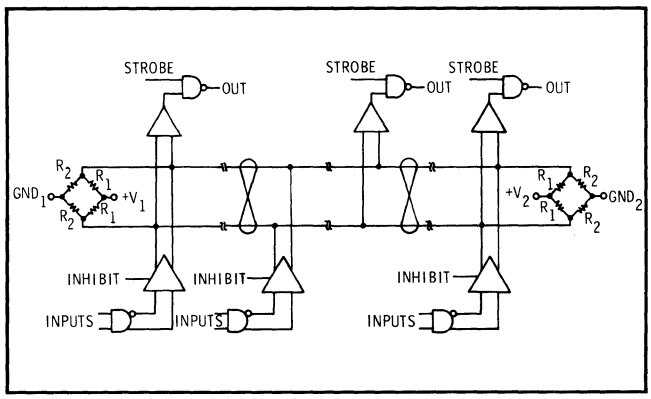

Figure 3 – Expansion of the Basic System to "Party-Line" Operation

A system of integrated line circuits is available using the concepts described above. These circuits are designed for compatibility with popular transistor-transistor logic (TTL) and for use with balanced, terminated transmission lines.

Each integrated line-driver package contains two of the drive circuits shown in Figure 4. The device designation for the monolithic dual driver is 75 109. The 75 109 driver circuit accepts TTL input levels and converts them into an output current supplied to one of the lines of the two-wire system. A gated current switch is used to select the driven line. A gate or inhibit input allows the output current to be removed from both lines for "party-line" operation.

The 75 109 driver circuit features low propagation delays (9 ns) for high-speed operation. The output current of 12 mA allows very long balanced transmission lines to be driven at normal line impedances (50 to 200 Ω). The resulting low-level differential signals minimize power dissipation. The most positive level at the bases of the driver output transistors allows at least - 3 V of noise

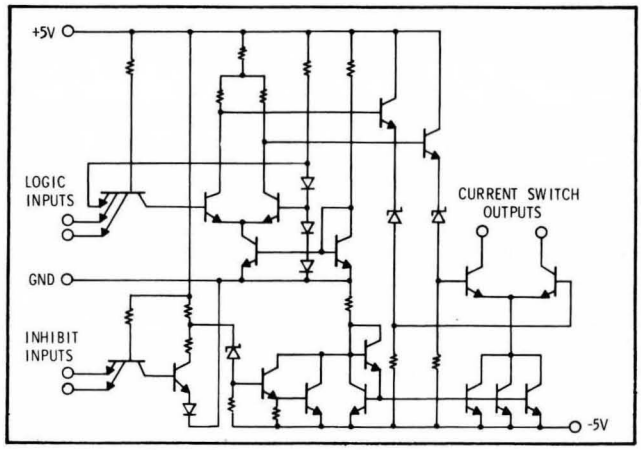

Figure 4 – 75 109 Line Driver Circuit

induced on the lines before saturation of the driver output transistor occurs. The high collector-emitter breakdown voltage of the output transistors allows up to +10 V of induced noise before transistor breakdown occurs.

In the inhibited mode, the outputs of the driver offer very little loading on the lines–the output impedance of OFF transistors and typical output currents of less than 30 μA.

A microphotograph of the 75 109 dual driver chip is shown in Figure 5. The chip size is 65 X 65 mils. The device is designed for fabrication in standard 14-pin packages and uses standard supplies of ± 5 volts. Device specifications apply over the temperature range of -55°C to 125°C.

The 75 107 is a dual line receiver designed to complement the 75 109 dual driver in balanced transmission line systems. Each of the 75 107 line receiver packages contains two of the circuits

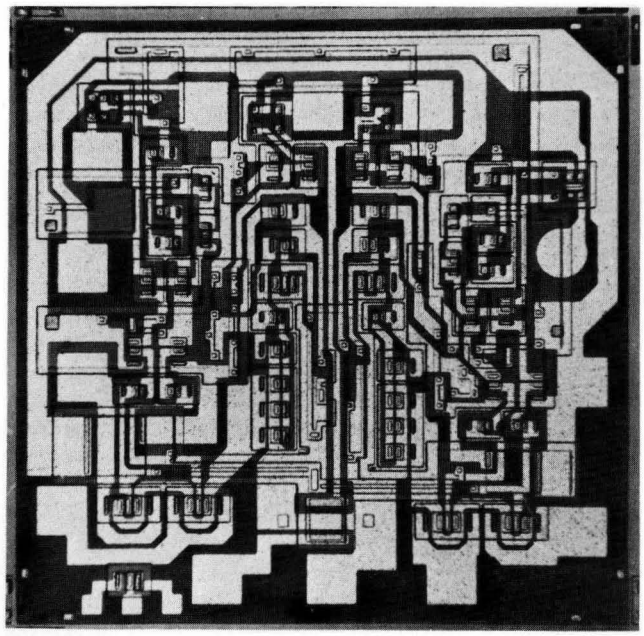

Figure 5 – Microphotograph of 75 109 Line Driver Chip

shown in Figure 6. The 75 107 circuit is designed to detect differential input signals as low as 20 mV in the presence of common-mode input noise in the range of ± 3 V. The 75 107 translates the polarity of the low-level differential input signal into high-level output logic levels compatible with TTL systems. Each receiver circuit also has TTL-compatible inputs used for strobing the receiver. One of these inputs allows independent strobing of the selected receiver. The other input is common to both receivers in the package and allows simultaneous strobing of both receivers for increased logic versatility.

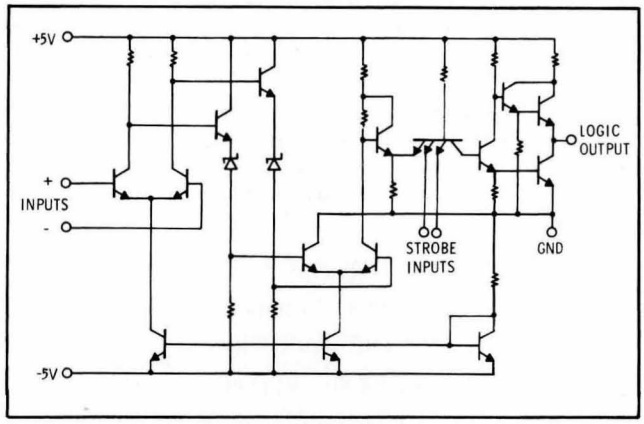

Figure 6 – 75 107 Line Receiver Circuit

The 75 107 receiver circuit features a nominal propagation delay of 17 ns, making it ideal for use in high-speed systems. The receiver delay is almost completely insensitive to overdrive voltages of greater than 10 mV. The circuit responds to input signals with repetition rates to 20 MHz.

The 75 107 input sensitivity, defined as the differential-input signal necessary to force the output to the logic threshold voltage level, is nominally 0 ± 3 mV. This sensitivity is particularly important when the receiver is used at the end of a very long transmission line where signal amplitude has deteriorated due to line effects. A receiver with this sensitivity also finds many other applications, such as comparators, sense amplifiers, level detectors, etc.

The common-mode input voltage range of the 75 107 is ±3 V, making it useful in all but the noisiest environments. In extremely noisy applications, input attenuators may be used to decrease the system common-mode noise to a tolerable level at the 75 107 inputs. Differential-input signals are reduced proportionally. However, the excellent input sensitivity of the 75 107 circuit allows the use of such attenuators in systems with high common-mode noise conditions. The attenuators could have been included in the 75 107 design, but they were intentionally omitted to increase the circuit versatility. The use of such attenuators adversely affects input sensitivity, propagation delay, power dissipation, and input impedance.

The input circuit of the 75 107 meets the requirements for low input currents (30 μA typical) and high input impedance. (5K Ω typical) for low loading on the lines – important considerations for "party-line" applications.

A microphotograph of the 75 107 chip is shown in Figure 7. The dual receiver circuit is fabricated on a 65 X 65 mil chip. The 75 107 is designed for fabrication in standard 14-pin integrated circuit packages. The device uses standard supplies of ±5 V and is specified for use over the temperature range of - 55°C to 125°C.

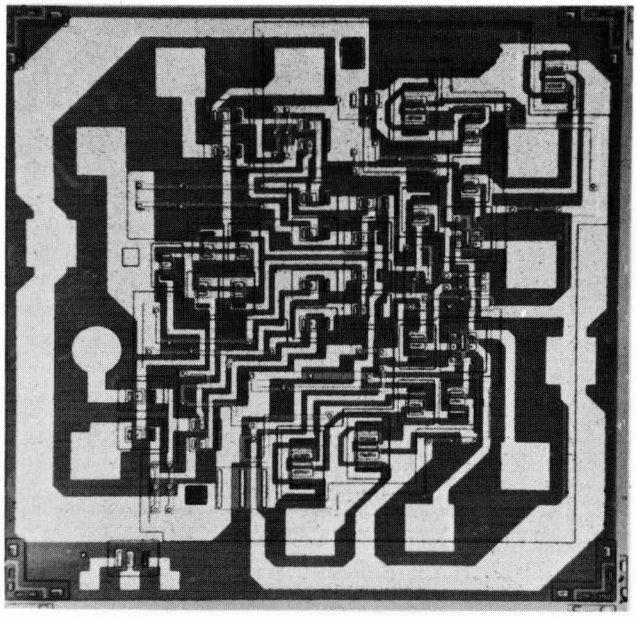

Figure 7 – Microphotograph of 75 107 Line Receiver Chip

The 75 109/107 line circuits have been used in balanced, terminated transmission line systems of several hundred foot lengths. The practical limit to the length of a transmission line is affected by many factors, one of the most important of which is line resistance. Voltage drops along long lines can be minimized by using large-diameter wire. For exceptionally long lines, receiver/driver repeaters may be used to reconstruct deteriorated waveforms before excessive degradation permits errors.

3. MEMORY DRIVERS

Two types of integrated memory drivers are available to serve this market. These are the high-current transistor array and high-current transistors with decode circuitry.

3.1 TRANSISTOR ARRAYS

High-current transistor arrays, both with and without integral logic decode circuitry, allow new design approaches in the memory drive area of computers. The increased attention toward thin-film memories–plated wire and flat film–organized in the 2D or linear-select configuration allows immediate widespread applications of such arrays.

The most obvious connection of memory driver transistors in arrays is shown in Figure 8. A single transistor is chosen by appropriate activation of a single base-select line and a single emitter-select line. The collector of the selected transistor drives a memory word line. In the 2D system the word current is of only one polarity. The state of stored data is determined by bit current polarity which overlaps the trailing edge of the word current.

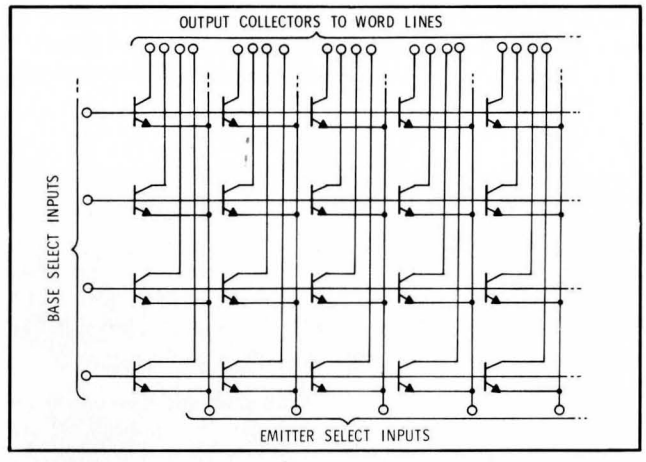

Figure 8 – Transistor Array for 2D Memory Applications

Collector-current amplitude and breakdown-voltage requirements of the transistors vary somewhat with the applications, but in general, word currents are in the 300-600 mA range with breakdown-voltage requirements in the 10-30 V range. Integrated bit-current drivers require the capability of bipolar drive and, in general, do not utilize large transistor arrays for implementation. Also, the number of bit drivers is much smaller than the number of word drivers–being proportional to the word length.

The 75 308 integrated circuit is an array of eight high-current transistors arranged in a 2 X 4 array as shown in Figure 9. Each

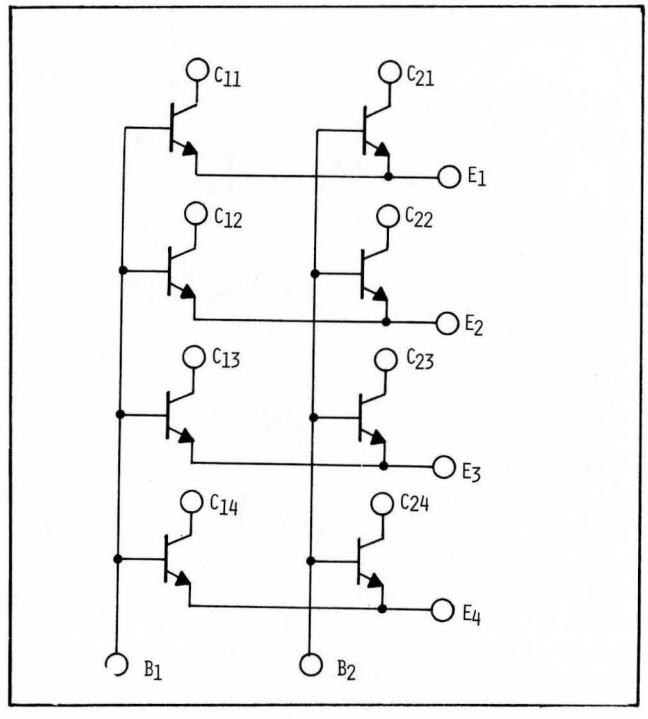

Figure 9 – 75 308 Transistor Array

transistor in the array is comparable to the 2N3724 and has the following typical characteristics at 25°C:

$V_{CE(Sat)}$	@	I_C = 500 mA	0.4 V
$V_{BE(Sat)}$	@	I_C = 500 mA	1.0 V
BV_{CEO}	@	I_C = 10 mA	20 V
BV_{CBO}	@	I_C = 10 μA	50 V
h_{FE}	@	I_C = 100 mA, V_{CE} = 2 V	30
h_{FE}	@	I_C = 400 mA, V_{CE} = 2 V	40
h_{FE}	@	I_C = 600 mA, V_{CE} = 2 V	30

3.2 TRANSISTORS WITH DECODE CIRCUITRY

Memory drivers for 2½D and 3D memories must be capable of bipolar current drive operation in the 300-600 mA range. Fewer drivers are used in these memory configurations than in 2D memories and integral logic decode circuitry can easily be implemented with the high-current output transistors.

The 75 324 integrated circuit is a monolithic memory driver designed specifically to replace traditional discrete transistor-transformer circuits in magnetic memory systems. The device, shown in the block diagram of Figure 10, contains two 400 mA source/sink switch pairs, with decoding from four address lines. Two of the address inputs (B and C) are used for mode selection, i.e., source or sink. The remaining address inputs (A and D) are used for switch-pair selection (W-X or Y-Z). Only one sink or source is permitted to be selected at one time in each 75 324 package to prevent excessive package power dissipation. Package selection and/or timing is performed at three additional logic inputs (E,F and G) designated as timing inputs.

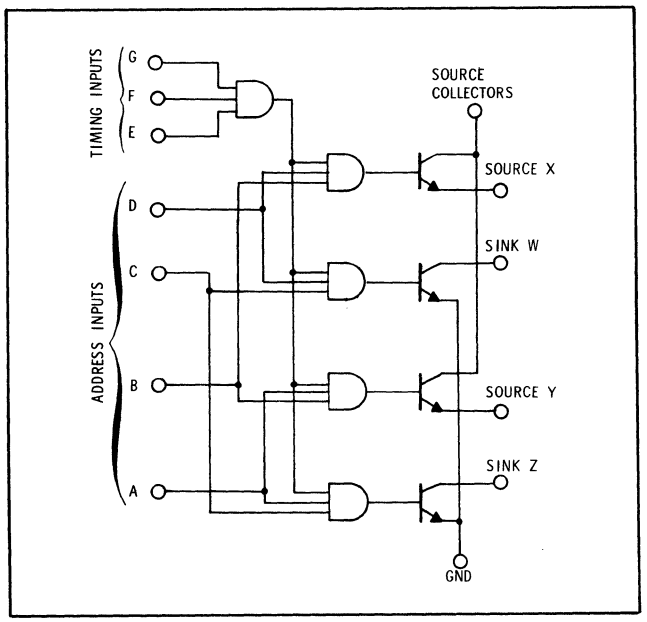

Figure 10 – 75 324 Monolithic Memory Driver Logic Diagram

A circuit schematic of the 75 324 is shown in Figure 11. The device requires 14 pin connections. The recommended supply voltage is +14 V. Drive current is provided by a higher supply voltage (typically +23 V) through a single external current-limiting resistor. This innovation reduces package power dissipation. The voltage at the 75 324 terminal is limited by an external diode clamp, thus reducing the device voltage requirements. Any of the 75 324 outputs may be shorted to ground without damage to the integrated circuit.

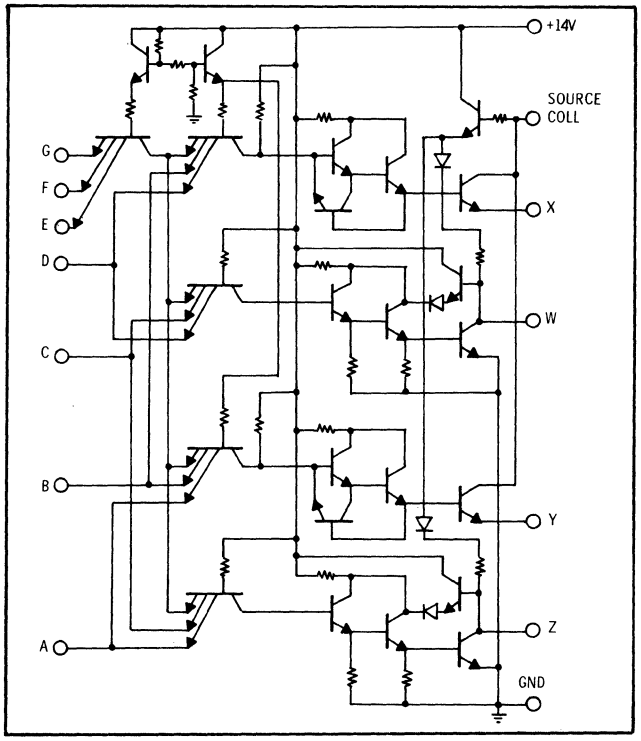

Figure 11 – Circuit Schematic of 75 324 Monolithic Memory Driver

The source circuit, shown with a sink circuit in Figure 12, is an emitter-follower output driven by a TTL input stage. During turn-on, the inductive load is pulled toward +14 V. Transient base drive current for the source is provided from the current-limiting resistor by the pseudo-Darlington connection. After the load current stabilizes, the Darlington diode, D_1, is reverse-biased and saturation of the source is maintained by the base drive resistor. During the turn-off transient, the turn-off transistor, Q_1, removes the base charge from the pseudo-Darlington pair and holds the source base at an OFF potential.

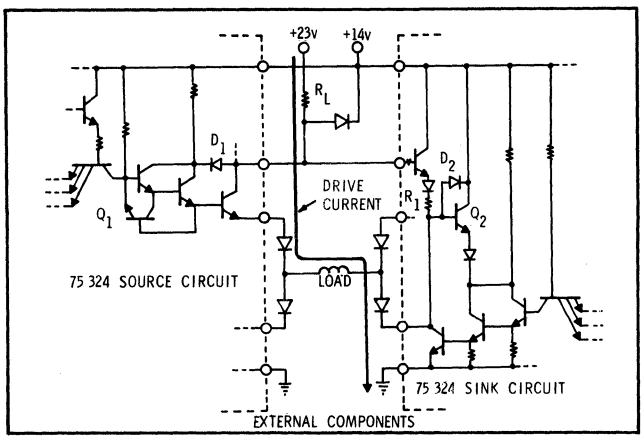

Figure 12 – 75 324 Source and Sink Circuit Connections in a Typical Application

The sink circuit of the 75 324 is composed of an inverting switch with transistor-transistor logic (TTL) inputs. Turn-on is enhanced by an over-drive transistor, Q_2, which provides transient base current for charging the transition and Miller capacitances of the sink. A stack discharge resistor, R_1, is disconnected when drive current is flowing. During turn-off, the drive current surges through a +14 V internal diode clamp, D_2, as line inductance energy is released.

The 75 324 is most useful when used in 2½D and 3D memory organizations. When coupled with external diode line selection matrices, 75 324's can provide the complete drive function for the memory. A typical drive-line selection scheme is illustrated in simplified form in Figure 13. Each address line is selected by a unique combination of drive and bus-line source/sink pairs, thereby supplying one coordinate of current to the memory planes in the 2½D or 3D system.

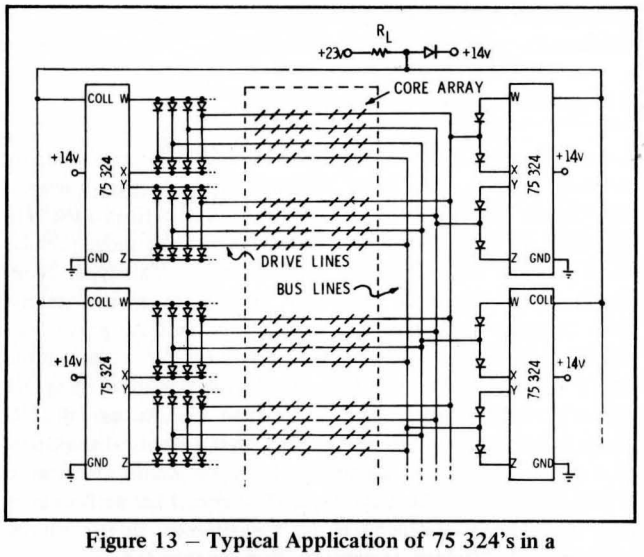

Figure 13 – Typical Application of 75 324's in a Memory Drive Line Selection Scheme

The truth table of Figure 14 indicates the input logic necessary to address a sink or source output.

INPUTS							OUTPUTS			
ADDRESS				TIMING			SINKS		SOURCES	
A	B	C	D	E	F	G	W	Y	X	Z
0	0	1	1	1	1	1	ON	OFF	OFF	OFF
0	1	0	1	1	1	1	OFF	OFF	ON	OFF
1	1	0	0	1	1	1	OFF	ON	OFF	OFF
1	0	1	0	1	1	1	OFF	OFF	OFF	ON
X	X	X	X	0	1	1	OFF	OFF	OFF	OFF
X	X	X	X	1	0	1	OFF	OFF	OFF	OFF
X	X	X	X	1	1	0	OFF	OFF	OFF	OFF

NOTES: 1. POSITIVE LOGIC

1 = HIGH VOLTAGE LEVEL ($\geq$3.5V)
0 = LOW VOLTAGE LEVEL ($\leq$1.0V)

2. X = LOGICAL 1 OR LOGICAL 0

3. ONLY ONE OUTPUT IS ALLOWED TO BE SELECTED AT ONE TIME

Figure 14 – 75 324 Truth Table

The 75 324 chip, shown in Figure 15, is approximately 60 X 120 mils in size and is fabricated using established epitaxial techniques and material of a resistivity comparable with linear integrated circuits. This permits higher collector-base breakdown voltages than required by most digital integrated circuits. Gold doping is utilized to reduce storage time.

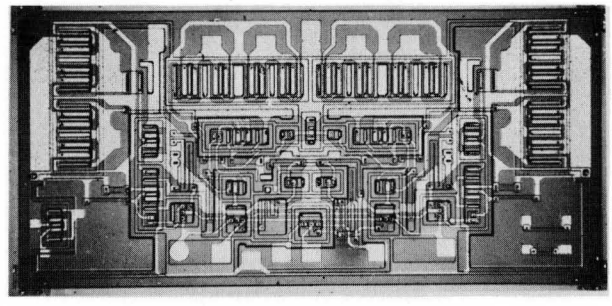

Figure 15 – Microphotograph of 75 324 Memory Driver Chip

A version of the 75 324 memory driver is utilized in the ICM-500 memory system being produced by the Computer Control Division of Honeywell. This system provides a 600-ns cycle time with a 370-ns access time. The system has a capacity of 8192 words of 36 bits and is organized in 2½D. The complete system is packaged in a 0.6 cubic foot enclosure and weighs 25 pounds, excluding power. The photographs of the ICM-500 memory in Figures 16 and 17 show external and internal layout features. Use of the integrated memory drivers allows all memory drive currents to be confined to printed-circuit wiring, resulting in consistent and well-defined electrical characteristics.

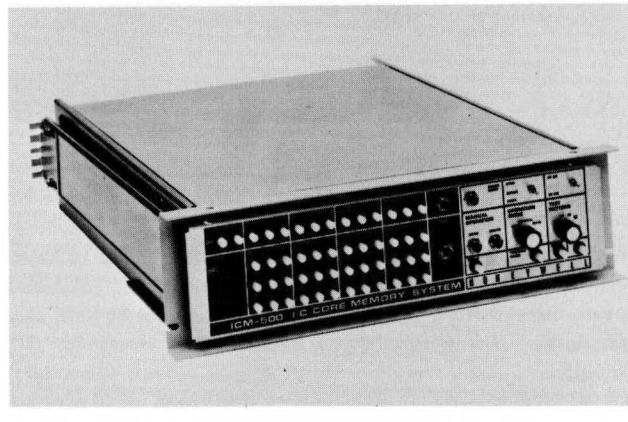

Figure 16 – External View of ICM-500 Memory

The elimination of transformer-coupled drive circuits results in improved memory performance and reduced memory volume.

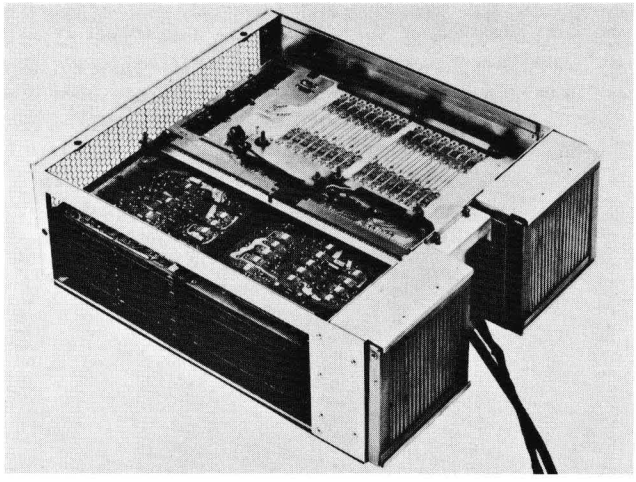

Figure 17 – Internal View of ICM-500 Memory Showing Board Layouts

An illustration of the reduction in circuit size is shown in Figure 18. The large circuit board performs the same function as the flat-pack encapsulated integrated 75 324 memory driver. The smaller board is equivalent to two of the fully integrated devices.

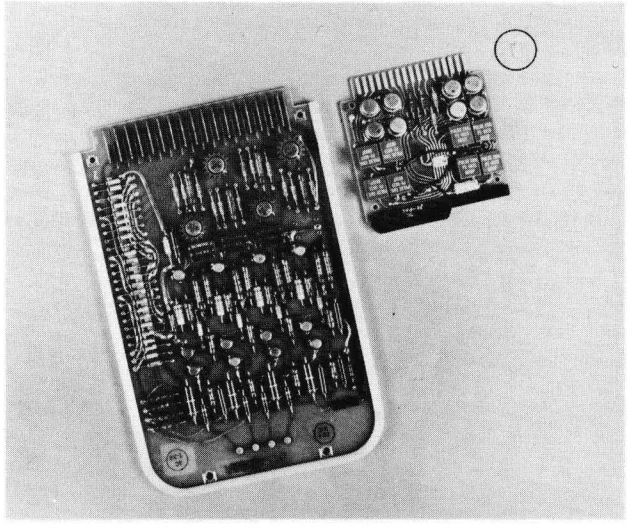

Figure 18 – Comparison of Integrated and Discrete Memory Drivers

The 75 324 can be used in other applications. Some of these include drum-memory head-selection schemes, transmission-line drivers, lamp drivers, relay drivers, etc. It can also be used as a base-emitter driver for large-scale transistor arrays for 2D memories.

4. SENSE AMPLIFIERS

Sense amplifiers for use with magnetic memories–ferrite cores, plated-wires, and planar films–must detect low-level differential input signals in the presence of common-mode noise. The sense signals usually follow a burst of high-amplitude differential noise generated by drive currents. At the present time, the dominant memory technology is ferrite cores. Both plated wires (cylindrical thin films) and planar thin films show promise for high-speed memories in the near future. The following table gives a comparison of signal characteristics of the three memory types:

Memory Type	Signal Type	Signal Width	Signal Amplitude	Cycle Time
Cores	Bipolar	100-300ns	8-50 mV	>500 ns
Plated wire	Unipolar	20-50ns	3-6 mV	>250 ns
Planar Films	Unipolar	5-30ns	1-2 mV	>150ns

Analysis of the sense signal characteristics reveals that the difficulty imposed on sensing circuitry increases by about an order of magnitude from cores to plated wires and another order from plated wires to planar films. Integrated sense circuits are available for use with each type of memory.

4.1 CORE MEMORY SENSE CIRCUITS

Integrated sense amplifiers have been available to serve the core memory market since 1964. Recent circuit designs, however, have made possible advances in both the performance and economy of these types of circuits. One of the most popular series of sense amplifiers now available is the 7520 type. These circuits use a "matched amplifier" concept to provide unique sense amplifier functions. It is well known that components of similar geometries built in close proximity on a monolithic circuit chip exhibit excellent thermal and electrical matching and tracking characteristics. The 7520 type circuits use this IC characteristic to advantage by building several identical amplifiers on a single chip, each exhibiting performance almost identical to others on the chip. The basic type 7520 circuit has performance that is relatively independent of temperature, power supply voltages, and diffusion parameters. Performance is based almost entirely on the ability of the process to produce matched components.

The popularity of Series 7520 circuits is due in part to performance and in part to the versatile functions available. The circuits are designed to be used with virtually any coincident-current (2½D or 3D) core memory now in production or design. Figures 19 through 22 show available Series 7520 sense amplifier functions.

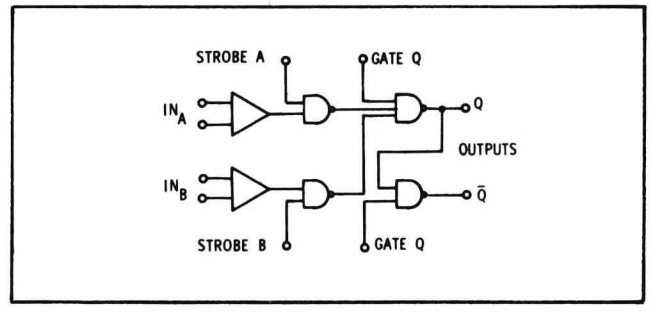

Figure 19 – Block Diagram of 7520

The 7520—the parent device shown in Figure 19—is a dual-preamplifier circuit useful for applications in memories of 8K or more words. The cascaded-gate outputs provide complementary TTL-compatible output levels. The gates may be connected as a latch to provide a simple memory data register function. The device features independent TTL-compatible strobe inputs for each sense preamplifier.

The 7522, Figure 20, is a dual-preamplifier device with an open-collector output. This output may be connected with

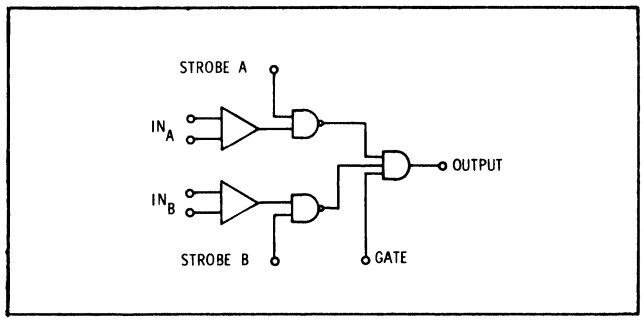

Figure 20 – Block Diagram of 7522

similar 7522 or 7520 outputs to provide the Wire-OR function, allowing a level of logic to be implemented without additional logic delay. The 7522 applications are similar to those of the 7520.

The 7524, Figure 21, is designed to be used with smaller memories– on the order of 4K words. The 7524 is two

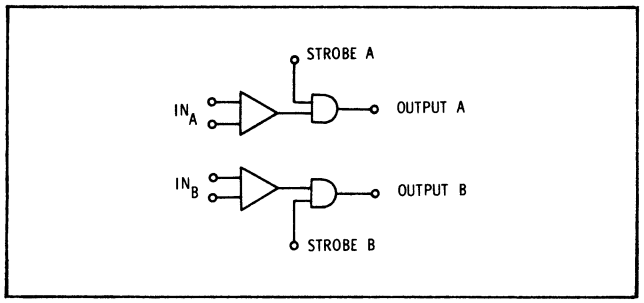

Figure 21 – Block Diagram of 7524

single-preamplifier sense amplifiers in a single package. Each of the sense channels features an independent strobe input.

The newest addition to the 7520 series of sense amplifiers is the 7526, shown in the block diagram of Figure 22. This device features dual preamplifiers and a complete output register with set and clear capabilities. Designed to service two 4K-word mats in an 8K-word memory, the 7526 offers advantages over other available integrated core memory sense amplifiers. One advantage is that the effective strobe window is extremely narrow regardless of the width of the strobe pulse. This is due to the use of a D-type flip-flop for the register. Information is entered into the flip-flop only when the positive edge of the clock-input pulse (supplied by the strobe pulse) passes through the clock-input threshold voltage level. For normal pulse rise times of less than 10 ns in TTL systems, the effective strobe width is a small percentage of this time. This reduces the critical strobe timing to one edge of the strobe waveform. Sense information cannot be entered into the flip-flop when the strobe is either high or low, but only in the positive edge.

A clear pulse is not necessary to restore the state of the flip-flop prior to the next strobe pulse. The flip-flop maintains stored data for 100% of the strobe duty cycle—entering new data at the start of each read cycle and maintaining it until the new read cycle or until the stored data is changed by use of the external clear or set inputs.

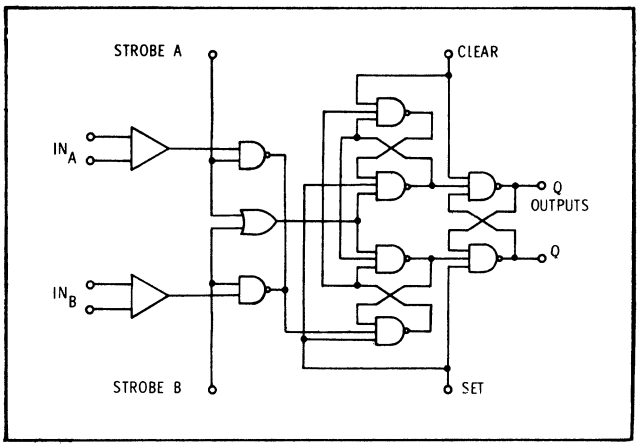

Figure 22 – Block Diagram of 7526

The device is fabricated on a 65 × 85 mil chip. This chip includes the capacitor necessary for compensating the 7520-type reference circuit to prevent oscillation. The 7526 is TTL-compatible and operates from ± 5 V supplies.

4.2 THIN-FILM SENSE CIRCUITS

The data stored in thin-film (wire or planar films) memory elements is sensed by the polarity of the output signal rather than by the amplitude as in 2½D or 3D core memories. Film memories are usually built in word-oriented or 2D type organizations. Because of the low level of the sense signals, particularly those from planar films, it is necessary to amplify the signals before they can be applied to a detector. An ac-coupled stage is necessary to get rid of dc-offset problems. High-speed transistor-transistor logic (TTL) or emitter-coupled logic (ECL) is desirable to take advantage of the high-speed capabilities of the memories.

The 5510 is an integrated linear wideband amplifier designed specifically for use as a sense preamplifier in thin-film memory systems. The bandwidth (40 MHz) and gain (40 dB) of this device with its excellent pulse response and overload recovery characteristics make it ideal for use in such applications.

The circuit diagram of the 5510 is shown in Figure 23. The device is fabricated on a 50 × 50 mil chip using established

linear-circuit processes. The power supplies for the device are ± 6V.

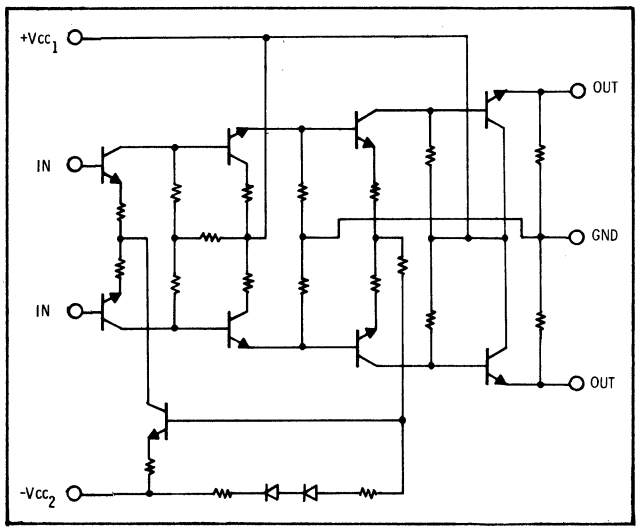

Figure 23 – Circuit Diagram of 5510

The 5510 is usually capacity-coupled to a detector circuit in memory applications. The coupling capacitor removes dc offset at the output of the 5510. In some applications, it may be necessary to employ dc-restore circuitry to remove the effects of dc-level shift introduced by the capacitor. The detector may be in the form of a logic circuit or a comparator. The detector provides additional gain and translates the signal into logic-compatible levels.

Devices such as the 7474 dual D-type TTL flip-flop have been utilized successfully as detectors. In one application, the data input of the flip-flop is biased at the midpoint between the logic levels such that the polarity of the output from one side of the 5510 can be detected. The clock input of the flip-flop is utilized as a strobe input. The 7474 provides complementary TTL-compatible output levels, preset and clear capabilities, and a memory data function. Similar applications of other circuits can be used to advantage with the 5510 in thin-film memory applications.

5. INTEGRATED CIRCUIT REQUIREMENTS

The advantages and limitations of integrated-circuit technologies are generally known and have been described in many excellent papers. Let it suffice to indicate here that those processes developed for linear IC's are, in general, adequate for use in fabricating most of the computer-system interface circuits. Breakdown voltages (collector-emitter) in the range of 15-25 V are adequate for most applications. One deviation from linear-circuit practice is the use of gold-doping to reduce storage time and therefore improve the response of saturated stages.

Computer-system interface circuits do not make large technological demands on processes. Limitations, rather are more acute in the areas of current density and packaging. High current requirements place new demands on interconnects–requiring wide metal patterns to reduce current densities to safe and reliable levels. Effective removal of heat from high power dissipation circuits such as memory drivers is difficult.

Most problems encountered when using high-current memory drivers are related to thermal management, lead inductance, and ground noise. The last two problems may be remedied by careful printed-circuit card layout with minimum-length signal lines and wide supply and ground leads. Multi-layered boards allow the luxury of using ground planes to separate signal lines.

When flat-pack packages are used, mounting of packages to a heat sink by a thermally conductive compound reduces thermal problems. If air flow is available, effective heat removal can be accomplished by mounting the package with the base up and with air flow perpendicular to the long axis of the package. Air-flow rates of 1000 fpm or more are recommended for effective heat removal. This can be accomplished readily with small "muffin" fans strategically located near the drive-circuit packages.

One of the problems almost always encountered when integrated circuits penetrate a new market segment is anticipated. This problem stems from the fact that an integrated circuit designed to implement a given function may be radically different from the discrete version. This is due to two factors. First, circuits cannot always be integrated on a one-to-one basis since some limitations and advantages in capabilities will be found. Secondly, monolithic circuits are often likely to be more complex, utilizing more components than is economically feasible in the discrete counterpart. Clever designs, exploiting fully the known advantages of monolithic components, result in circuits and sub-systems that can compete both economically and performance-wise with traditional equivalents.

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7. ACKNOWLEDGEMENT

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