TEXAS INSTRUMENTS

Advanced CMOS Logic

Designer's Handbook

1988

Advanced CMOS Logic Designer's Handbook

Contributors

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Introduction

Component manufacturers have expanded technology in search of the ultimate high-speed/low-power logic devices. The resulting improved logic products have led to end equipment with more functionality per unit volume, as well as systems that solve increasingly more complex problems.

At the same time, these advanced-performance logic devices have led to a more demanding design environment. Designers entering the realm of improved devices face stricter rules, smaller margins for error, and a greater variety of complications than they faced with lower performance products. They are forced to re-evaluate design techniques, product selection, board layout, and testing methods to meet the precise requirements of ever more sensitive devices.

Years of experience in ECL and advanced bipolar design have given designers some hard-earned lessons, but the field of new devices continues to grow. A need exists for a reference guide that spells out the technical issues confronted in advanced logic design and describes the methods for handling these issues. Texas Instruments has created the ''Advanced CMOS Logic Designer's Handbook'' in response to this need.

The topics addressed in the handbook are applicable to designing with most advanced logic families. However, Advanced CMOS Logic (ACL) is especially suited to illustrate the key technical issues, not only because it represents the latest entry into the upper echelon of devices, but because its development has increased awareness of advanced logic design challenges, such as the control of simultaneous switching noise.

The first four sections of the text provide an introduction to TI's EPIC™ ACL that serves as foundation for the discussion of design considerations in section five. Sections and topics in the handbook are as follows:

> Section 1 gives an overview of TI's EPIC™ ACL, including the issue of simultaneous switching noise and how TI solved the noise problem.
>
> Section 2 contains EPIC™ ACL datasheet parameters, mechanical package specifications for through-hole and surface mount, and an explanation of IEEE logic symbols.

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Section 3 includes device specifications and circuitry that illustrate some of the unique benefits of TI's EPIC™ ACL.

Section 4 addresses testing and characterization issues for ACL, including how to evaluate devices for simultaneous switching noise and how TI characterizes the ACL family.

Section 5 is devoted to PC board and system-level design considerations.

Section 6 contains reliability data for Texas Instruments EPIC™ ACL, information on cost of ownership, and ESD-handling guidelines.

We at Texas Instruments hope you find the "Advanced CMOS Logic Designer's Handbook" a useful reference tool for all your advanced logic design. If, during your design or evaluation effort, you need additional technical or application assistance, please contact our applications engineering group at (214) 868-7682.

Contents

Section		*Page*
1	**Overview**	**1-1**
1.1	EPIC™ Advanced CMOS Logic Design Considerations	1-1
1.1.1	Introduction	1-1
1.1.2	Simultaneous Switching Noise Effects of High-Speed Logic	1-1
1.1.3	Issue of Simultaneous Switching	1-1
1.1.4	The TI Simultaneous Switching Solution	1-3
1.1.5	Evaluation Results	1-6
1.1.6	Flow-Through Architecture	1-8
1.1.7	Device Pinouts	1-10
1.1.8	Symbolization	1-10
1.1.9	EPIC™ ACL Pinouts	1-11
1.1.10	Summary	1-22
2	**Data Sheet Information**	**2-1**
2.1	EPIC™ Advanced CMOS Logic Data Sheets	2-1
2.1.1	Introduction	2-1
2.1.2	Dissecting the ACL Data Sheet	2-1
2.1.3	Macro Description	2-2
2.1.4	Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)	2-2
2.1.5	Recommended Operating Conditions	2-5
2.1.6	Electrical Characteristics Over Recommended Free-Air Temperature Range	2-8
2.1.7	Timing Requirements	2-12
2.1.8	Switching Characteristics	2-15
2.1.9	Functional Testing	2-19
2.1.10	Summary	2-20

Section *Page*

2.2 ACL Mechanical Design Consideration 2-21
2.2.1 EPIC™ ACL Commercial Options 2-21
2.2.2 EPIC™ ACL Military Options 2-22
2.2.3 D014 and D016 Plastic "Small Outline" Packages . . . 2-23
2.2.4 DW020, DW024, and DW028 Plastic "Small Outline" Package 2-24
2.2.5 N014 Plastic Dual-In-Line Package 2-25
2.2.6 N016 Plastic Dual-In-Line Package 2-26
2.2.7 NT020 Plastic Dual-In-Line Package 2-27
2.2.8 NT024 and NT028 Plastic Dual-In-Line Package 2-28
2.2.9 FK020 and FK028 Ceramic Chip Carrier Packages 2-29
2.2.10 J014 Ceramic Dual-In-Line Package 2-30
2.2.11 J016 Ceramic Dual-In-Line Package 2-31
2.2.12 J020 Ceramic Dual-In-Line Package 2-32
2.2.13 JT024 Ceramic Dual-In-Line Package 2-33
2.3 Explanation of Logic Symbols 2-34
2.3.1 Introduction 2-34
2.3.2 Symbol Composition 2-34
2.3.3 Qualifying Symbols 2-36
2.3.4 Dependency Notation 2-42
2.3.5 Bistable Elements 2-55
2.3.6 Coders 2-58
2.3.7 Use of a Coder to Produce Affecting Inputs 2-60
2.3.8 Use of Binary Grouping to Produce Affecting Inputs 2-60
2.3.9 Sequence of Input Labels 2-60
2.3.10 Sequence of Output Labels 2-62

3 ACL Design Specifications 3-1

3.1 EPIC™ CMOS Logic Output Edge Control 3-1
3.1.1 Introduction 3-1
3.1.2 Reducing Voltage Spikes 3-1
3.1.3 Design Considerations 3-4
3.1.4 Circuit Design — Grading Turn-On 3-6
3.1.5 Circuit Design — Controlling Gate Voltage 3-9
3.1.6 Characteristics of OEC™ Design 3-10
3.1.7 Summary 3-12

Section *Page*

3.2 Advanced CMOS Logic Input Circuitry Characteristics 3-12
3.2.1 Introduction 3-12
3.2.2 ACL Input Circuitry 3-12
3.2.3 Input Current and Voltage 3-14
3.2.4 Proper Termination of Unused Inputs 3-17
3.2.5 Input Capacitance 3-17
3.2.6 Summary 3-19
3.3 Slow Input Transition Times 3-19
3.3.1 Introduction . . . . .
3.3.2 Relationship Between Charge, Voltage, and Capacitance 3-20
3.3.3 Dynamic Hysteresis 3-25
3.3.4 Summary 3-29
3.4 Metastable Characteristics 3-29
3.4.1 Introduction 3-29
3.4.2 Metastable Definition 3-29
3.4.3 Metastable Evaluation 3-30
3.4.4 Circuit Description 3-30
3.4.5 Test Circuit Limitations 3-32
3.4.6 The Metastability Equation 3-33
3.4.7 Metastability Test Results 3-34
3.4.8 Summary 3-36

4 Device Testing and Evaluation 4-1

4.1 Simultaneous Switching Considerations 4-1
4.1.1 Abstract 4-1
4.1.2 Introduction 4-1
4.1.3 Simultaneous Switching Phenomenon 4-2
4.1.4 Simultaneous Switching Noise System Effects 4-5
4.1.5 Simultaneous Switching System Considerations 4-8
4.1.6 Simultaneous Switching Evaluation 4-22
4.1.7 Conclusion 4-42
4.1.8 References 4-42
4.2 Automatic Test Equipment Characterization Procedures 4-43
4.2.1 Introduction 4-43
4.2.2 ACL Automatic Test Equipment Characterization 4-43
4.2.3 Correlation Unit Concept 4-45
4.2.4 Characterization Device Selection 4-50
4.2.5 Data Acquisition 4-50
4.2.6 Characterization Data Analysis 4-50
4.2.7 Limit Verification 4-52
4.2.8 Summary 4-55

Section *Page*

5 PCB and System-Level Considerations 5-1

5.1 EPIC™ Advanced CMOS Logic System Evaluation Board 5-1
5.1.1 Introduction 5-1
5.1.2 Description of System and Test Methods 5-1
5.1.3 Evaluation 5-4
5.1.4 System Evaluation Board Patterns 5-10
5.1.5 Definitions 5-11
5.1.6 Waveform Comparisons 5-13
5.1.7 Summary 5-15
5.2 Advanced CMOS Logic PCB Design Considerations 5-16
5.2.1 Introduction 5-16
5.2.2 High-Speed Logic System Environment 5-16
5.2.3 ACL Pinout Strategy 5-23
5.2.4 Simultaneous Switching Performance 5-24
5.2.5 Summary 5-27
5.2.6 References 5-27
5.3 Partial System Power-Down with CMOS Devices 5-28
5.4 CMOS Power Management 5-32
5.4.1 Introduction 5-32
5.4.2 Quiescent Power Consumption 5-32
5.4.3 High-Speed and Advanced CMOS Devices 5-33
5.4.4 TTL-Compatible CMOS Devices 5-33
5.4.5 Dynamic Power Consumption 5-35
5.4.6 Summary 5-40
5.5 Reprint of Super-Speed Pc-Board Interconnects 5-41
5.6 Reprint of High-Performance Logic Places New Demands on Backplane Interconnects 5-47
5.7 Reprint of The Role of Integrated Circuits Decoupling in Electromagnetic Compatibility 5-51

Section *Page*

6 Quality and Reliability 6-1

6.1 ACL Reliability Summary 6-1
6.1.1 Introduction 6-1
6.1.2 EPIC™ 1-μm CMOS Process 6-1
6.1.3 Qualification Testing 6-2
6.1.4 Accelerated Life Test 6-2
6.1.5 Bias Temperature Humidity Life Tests 6-4
6.1.6 Autoclave Test 6-5
6.1.7 Temperature Cycling 6-6
6.1.8 SNJ54AC Logic Family 6-7
6.1.9 Test Methods 6-7
6.1.10 Test Results 6-11
6.1.11 Summary 6-11
6.2 Adapted from "The Impact of IC Quality and Reliability on Cost of Ownership" 6-13
6.3 Reprint of Guidelines for Handling Electrostatic-Discharge Sensitive (ESDS) Devices and Assemblies 6-29

List of Illustrations

Figure	*Title*	*Page*
1.1-1	Pin Inductance for a 14-Pin Package, End-Pin Configuration	1-4
1.1-2	Pin Inductance for a 24-Pin Package, End-Pin Configuration	1-4
1.1-3	Vendor A Advanced CMOS '244 20-Pin Plastic DIP, 1 V_{CC}/1 GND, End-Pin Package	1-7
1.1-4	Vendor B Advanced CMOS '244 20-Pin Plastic DIP, 1 V_{CC}/1 GND, End-Pin Package	1-7
1.1-5	Texas Instruments 'AC11244 24-Pin Plastic DIP, 2 V_{CC}/4 GND, Center-Pin Package	1-8
1.1-6	Test Circuitry	1-8
1.1-7	Flow-Through Pinout Architecture for an 'AC11000 Device	1-9
1.1-8	Flow-Through Pinout Architecture for an 'AC11074 Device	1-9
1.1-9	Flow-Through Pinout Architecture for an 'AC11240 Device	1-9
1.1-10	Symbolization and Package Information	1-10
2.1-1	General Information	2-3
2.1-2	Absolute Maximum Ratings Table	2-4
2.1-3	Input and Output Clamp Circuits	2-5
2.1-4	Recommended Operating Conditions Table	2-6
2.1-5	Electrical Characteristics and Operating Characteristics Table	2-9
2.1-6	Timing Requirements Table	2-13
2.1-7	Load Circuit and Voltage Waveforms	2-14
2.1-8	Switching Characteristics Table	2-16
2.1-9	Load Circuit and Voltage Waveforms	2-18
2.2-1	Profiles of P-DIP Through-Hole and SOIC Surface-Mount Package Technologies	2-20
2.2-2	Profiles of C-DIP Through-Hole and LCCC Surface-Mount Package Technologies	2-21
2.3-1	Symbol Composition	2-35
2.3-2	Common-Control Block	2-36
2.3-3	Common-Output Element	2-36
2.3-4	G Dependency Between Inputs	2-43
2.3-5	G Dependency Between Outputs and Inputs	2-43
2.3-6	G Dependency with a Dynamic Input	2-44

Figure	*Title*	*Page*
2.3-7	ORed Affecting Inputs	2-44
2.3-8	Substitution for Numbers	2-45
2.3-9	V (OR) Dependency	2-45
2.3-10	N (Negate) (Exclusive-OR) Dependency	2-46
2.3-11	Z (Interconnectional) Dependency	2-47
2.3-12	X (Transmisson) Dependency	2-47
2.3-13	CMOS Transmission Gate Symbol and Schematic	2-47
2.3-14	Analog Data Selector (Multiplexer/Demultiplexer)	2-48
2.3-15	C (Control) Dependency	2-49
2.3-16	S (Set) and R (Reset) Dependencies	2-50
2.3-17	EN (Enable) Dependency	2-51
2.3-18	M (Mode) Dependency Affecting Inputs	2-52
2.3-19	Type of Output Determined by Mode	2-53
2.3-20	An Output of the Common-Control Block	2-53
2.3-21	Determining the Output's Function	2-53
2.3-22	Dependent Relationships Affected by Mode	2-54
2.3-23	A (Address) Dependency	2-55
2.3-24	Array of 16 Sections of Four Transparent Latches with 3-State Outputs Comprising a 16-Word × 4-Bit Randon-Access-Memory	2-56
2.3-25	Four Types of Bistable Circuits	2-57
2.3-26	Coder General Symbol	2-58
2.3-27	An X/Y Code Converter	2-59
2.3-28	An X/Octal Converter	2-59
2.3-29	Producing Various Types of Dependencies	2-60
2.3-30	Producing One Type of Dependency	2-60
2.3-31	Use of the Binary Grouping Symbol	2-61
2.3-32	Input Labels	2-61
2.3-23	Factoring Input Labels	2-61
2.3-34	Placement of 3-State Symbols	2-62
2.3-35	Output Labels	2-62
2.3-36	Factoring Output Labels	2-63
3.1-1	Competitor's Simultaneous Switching Performance in a DIP	3-2
3.1-2	Competitor's Simultaneous Switching Performance in an SOIC	3-3
3.1-3	Texas Instruments Simultaneous Switching Performance in an SOIC	3-4
3.1-4	Current Through a Transistor and Value of di/dt	3-5
3.1-5	CMOS Transistor Gate Layout	3-7
3.1-6	Equivalent Schematics	3-7
3.1-7	Effect of Added Pull-Downs on Thru-Current	3-8
3.1-8	"Distributed" N-Channel with Gate Voltage Control	3-9
3.1-9	SPICE Results — Simultaneous Switching OCTAL Device with Standard Lumped Output	3-10

Figure	*Title*	*Page*
3.1-10	SPICE Results — Simultaneous Switching with Distributed Output	3-11
3.2-1	54/74AC Input Circuit	3-13
3.2-2	54/74ACT Input Circuit	3-13
3.2-3	ESD Protection Circuit	3-14
3.2-4	Input Voltage vs Input Current	3-15
3.2-5	Input Current vs Ambient Temperature	3-15
3.2-6	Input Voltage vs Supply Current	3-16
3.2-7	Input Voltage vs Supply Current	3-17
3.2-8	Input Capacitance vs Input Voltage	3-18
3.2-9	Input Capacitance vs Ambient Temperature	3-18
3.3-1	Simple CMOS Inverter	3-19
3.3-2	Competitor AC244 Subjected to 100-ns Falling Edge with Eight Gates Switching Simultaneously	3-22
3.3-3	Competitor AC244 Subjected to 100-ns Falling Edge with Eight Gates Switching Simultaneously	3-23
3.3-4	Competitor AC244 Subjected to 100-ns Falling Edge with Eight Gates Switching Simultaneously	3-24
3.3-5	Competitor AC244 Subjected to 75-ns Falling Edge with Eight Gates Switching Simultaneously	3-24
3.3-6	Texas Instruments AC11244 Subjected to 100-ns Falling Edge with Eight Gates Switching Simultaneously	3-26
3.3-7	Texas Instruments AC11244 Subjected to 100-ns Falling Edge with Eight Gates Switching Simultaneously	3-27
3.3-8	Texas Instruments AC11244 Subjected to 100-ns Falling Edge with Eight Gates Switching Simultaneously	3-28
3.3-9	Texas Instruments AC11244 Subjected to 75-ns Falling Edge with Eight Gates Switching Simultaneously	3-28
3.4-1	Metastable Timing Diagram	3-30
3.4-2	Metastable Evaluation Test Circuit Schematic	3-31
3.4-3	Metastable Timing Diagram	3-32
3.4-4	Metastable Evaluation Test Circuit — Internal Delays	3-33
3.4-5	AC11074, ACT11074A, and HC74 Metastability Performance	3-35
4.1-1	End-Pin Simultaneous Switching Noise Waveform	4-2
4.1-2	RC Model of a CMOS Output for the High-to-Low Transition	4-3
4.1-3	Quiescent -Output Disturbance Voltage Waveforms	4-5
4.1-4	Application Report	4-7
4.1-5	Pulse Duration vs Pulse Amplitude	4-8
4.1-6	Laboratory Setup for Distributed Loading Evaluation	4-9
4.1-7	Peak Low-Level Output Voltage vs Distance	4-10
4.1-8	Peak Low-Level Output Voltage vs Distance	4-11
4.1-9	V_{OLP} Characterization Results for AC11008	4-11
4.1-10	V_{OLP} Characterization Results for AC00	4-12

Figure	*Title*	*Page*
4.1-11	Peak Low-Level Output Voltage vs Distance	4-12
4.1-12	Evaluation of Temperature Effects	4-13
4.1-13	Evaluation of Temperature Effects	4-14
4.1-14	Peak Low-Level Output Voltage vs Free-Air Temperature	4-15
4.1-15	Valley High-Level Output Voltage vs Free-Air Temperature	4-15
4.1-16	Valley High-Level Output Voltage vs Supply Voltage	4-16
4.1-17	Peak Low-Level Output Voltage vs Supply Voltage	4-16
4.1-18	Standard ACL Load Circuit	4-17
4.1-19	Load Capacitance vs Other Parameters	4-18
4.1-20	Propagation Delay Time vs Load Management	4-19
4.1-21	Loading Effect Evaluation, Low-Level Output Voltage/Peak Low-Level Output Voltage vs Low-Level Output Current	4-19
4.1-22	Loading Effects Evaluation, High-Level Output Voltage/Valley High-Level Output Voltage vs High-Level Output Current	4-20
4.1-23	Input Signal Offset Evaluation	4-21
4.1-24	Board Layout and Composition	4-23
4.1-25	Board Photograph	4-24
4.1-26	V_{OHV} and V_{OLP} Data for Two Cases	4-25
4.1-27	AC11240 Peak Low-Level Output Voltage vs Pin Location	4-26
4.1-28	Standard Simultaneous Switching Evaluation Circuit	4-27
4.1-29	V_{OHV} Nominal Measurement on 74AC11373	4-28
4.1-30	Peak Low-Level Output Voltage Nominal Measurement on 74AC11373	4-29
4.1-31	74AC11373 Passes Stored Data Test on the High Impedance to Low Transition (ZL)	4-30
4.1-32	74AC11373 Passes Stored Data Test on the High Impedance to High Transition (ZH)	4-31
4.1-33	Standard Simultaneous Switching Evaluation Circuit	4-32
4.1-34	Quiescent-Output Disturbance Voltage Waveforms	4-33
4.1-35	V_{OHV} Nominal Measurement on 74AC11373	4-34
4.1-36	V_{OLP} Nominal Measurement on 74AC11373	4-35
4.1-37	74AC11373 Passes Stored Data Test on the High Impedance to Low Transition (ZL)	4-36
4.1-38	74AC11373 Passes Stored Data Test on the High Impedance to High Transition (ZH)	4-37
4.1-39	Dynamic-Output Disturbance Voltage Waveform	4-38
4.1-40	Dynamic VOHV Nominal Measurement on 74AC11030	4-39
4.1-41	Dynamic VOLP Nominal Measurement on 74ACT11030	4-40
4.2-1	Bench Lab Data for an AC11000	4-44
4.2-2	Standard Deviation Verifications	4-46
4.2-3	Retest for Standard Deviation Verifications	4-48
4.2-4	Parametric Test of Multiple Groups over Temperature	4-51

Figure	*Title*	*Page*
4.2-5	Summary of All Y Coord (lot #6312542) Readings at 25°C	4-53
4.2-6	V_{OH} at 4.5 V vs Temperature	4-54
5.1-1	System Evaluation Board Block Diagram	5-2
5.1-2	Pulse Duration vs Amplitude	5-4
5.1-3	V_{OLP} vs Logic Family	5-5
5.1-4	V_{OLP} vs Switching Pattern	5-6
5.1-5	V_{OLP} vs Transmission Line	5-7
5.1-6	V_{OLP} vs Test Location	5-8
5.1-7	V_{OLP} vs Test Location	5-8
5.1-8	Quiescent Disturbance Voltage Waveforms	5-11
5.1-9	Oscilloscope Setting and Points of Measurement	5-12
5.1-10	Texas Instruments EPIC™ ACL	5-13
5.1-11	HCMOS	5-13
5.1-12	Vendor A	5-14
5.1-13	Vendor B	5-14
5.2-1	PCB Plane and Trace Impedance vs Frequency	5-17
5.2-2	Lines	5-19
5.2-3	Maximum Line Length vs Capacitance Loading	5-20
5.2-4	Transmission Line Termination Techniques	5-21
5.2-5	Crosstalk Magnitude Due to Various Line Separation	5-22
5.2-6	Flow-Through Architecture	5-24
5.2-7	74ACT11032 Simultaneous Switching Noise	5-25
5.2-8	74AC11032 Simultaneous Switching Noise	5-25
5.2-9	74ACT11074 Simultaneous Switching Noise	5-26
5.2-10	74AC11109 Simultaneous Switching Noise	5-26
5.2-11	'244 Simultaneous Switching Summary	5-27
5.3-1	Simplified ESD Structures for HC and ACL Devices	5-28
5.3-2	Example of Partial System Power-Down	5-29
5.3-3	Current Limiting for a Partial System Power-Down	5-30
5.3-4	Partial Power-Down with Bus Drivers	5-30
5.3-5	Current Limiting for Bus Drivers During Partial Power-Down	5-31
5.4-1	Basic CMOS Inverter	5-33
5.4-2	I_{CC} vs VIN	5-34
5.4-3	C_{pd} vs Input Rise and Fall Time	5-37
5.4-4	C_{pd} vs Input Frequency and V_{CC}	5-38
5.4-5	C_{pd} vs Temperature	5-39

Figure	*Title*	*Page*
6.1-1	EPIC™ 1-Micron CMOS Process	6-2
6.1-2	Dynamic Bias Life Test Circuit	6-4
6.1-3	Static Bias Life Test Circuit	6-4
6.2-1	Improving Quality Trend	6-14
6.2-2	Improving Reliability Trend	6-14
6.2-3	Reliability Bathtub Curve	6-18
6.2-4	Relationships of FR_Q, FR_E, and RE_I	6-19
6.2-5	Relationships of FR_E, FR_I, and $FR_{1st\ year}$ for Warranty Calculations	6-20

List of Tables

Table	*Title*	*Page*
1.1-1	Inductance vs Package Configuration	1-5
1.1-2	Number and Location of V_{CC}/GND Pins for ACL Packages	1-6
2.3-1	General Qualifying Symbols	2-37
2.3-2	Qualifying Symbols for Inputs and Outputs	2-39
2.3-3	Symbols Inside the Outline	2-41
2.3-4	Summary of Dependency Notation	2-56
3.1-1	20-Pin DIP and SOIC Package Lead Inductances	3-2
3.2-1	Advanced CMOS ICC Specifications	3-16
4.1-1	Comparison of Dual-in-Line (DIP) and Small Outline (SO) 20-Pin Package Parasitic Inductances and Percent Change in Switching Noise	4-14
4.1-2	Propagation Delay Effects Due to Simultaneous Switching	4-22
5.3-1	Absolute Maximum Values for I_O, I_{IK}, and I_{OK}	5-29
6.1-1	EPIC™ ACL Accelerated Life Test Results	6-3
6.1-2	Bias Temperature Humidity Life Test	6-5
6.1-3	Autoclave Test Results	6-6
6.1-4	Temperature Cycling Test Results	6-7
6.1-5	Group B Test Methods (Package Related Tests) SNJ54 ACL (Note 1)	6-8
6.1-6	Group C Test Methods (Die-Related Tests) SNJ54 ACL	6-9
6.1-7	Group D Test Methods (Package-Related Tests) SNJ54 ACL	6-10
6.2-1	Probability of Board Rework in %	6-16

1 Overview

1.1 EPIC™ Advanced CMOS Logic Design Considerations†

1.1.1 Introduction

Advanced CMOS Logic (ACL) has evolved into a product family featuring high performance characteristics normally associated with advanced high-speed bipolar. The major advantage provided by CMOS technology is the significant reduction in power consumption. ACL performance features include:

1. < 3 ns average gate performance
2. 24 mA output drive capability
3. Maximum operating frequency greater than 150 mHz
4. μW standby power consumption
5. Superior latch-up protection
6. Capable of electrostatic discharge protection in excess of 2000
7. CMOS and TTL logic level input capability.

1.1.2 Simultaneous Switching Noise Effects of High-Speed Logic

While the speed improvements in the advanced CMOS logic families offer obvious advantages, system-level complications may exist with some applications. For example, the improvement in propagation delay times has resulted in faster rise and fall times. The combination of fast rates and device package inductance creates the possibility of errant voltage spikes occurring during the switching of multiple outputs. TI refers to this occurrence as Simultaneous Switching Noise. The impact of these voltage noise spikes within a system can be extreme. The noise can cause loss of stored data, severe speed degradation, output glitches, and/or reduction in system noise immunity.

1.1.3 Issue of Simultaneous Switching

Simultaneous switching of multiple outputs occurs in most applications. Previously, simultaneous switching noise was not a major issue to CMOS/TTL Logic families. This was due to slower rise and fall times of the older logic families. However, with the emergence of advanced logic families: 74HC, 74ALS, 74F, 74AS, and 74AC/ACT, analysis of integrated circuit performance during simultaneous switching conditions becomes necessary.

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†Written by C. Hefner, R. Moore and M. Weinstein.

The advanced CMOS technology inherently causes fast edge rates as compared to bipolar TTL with the same speed performance range. Coupled with the rail-to-rail voltage swings inherent to CMOS logic, the susceptibility to large switching noise spikes becomes greater. Therefore, it is necessary to evaluate the contributing causes of noise during the simultaneous switching of multiple outputs.

The device physics of the actual package plays a fundamental role in the voltage noise spike. The major effect on a high-speed logic device is the induced voltage on the GND and V_{CC} pins caused by the transient currents resulting from switching capacitive loads.

$$V_L(t) = -L_p C_L \frac{d^2V_O(t)}{dt^2} \quad (1)$$

where:

V_L = voltage transient on the ground pin
L_p = self inductance of the ground pin
C_L = load capacitance
d^2V = change in the slope of the transition edge
dt = change in the time of the transition edge

To reduce the amplitude of the voltage spike sufficiently to minimize simultaneous switching noise effect, it is necessary to address two of the components in equation (1); (a) dv/dt and (b) L_p.

The dv/dt component of equation (1) is the change in the edge rates (rise/fall times) that is technology driven. The technology utilized determines the typical performance levels as well as the edge rates. All advanced CMOS manufacturers have similar output characteristics. Therefore, all advanced CMOS logic products will exhibit similar edge rates and, as a result, will be affected by the noise problems associated with fast edges and package inductance. Reducing the dv/dt component of equation (1) would increase the device propagation delay and/or reduce the output drive. This is not a reasonable solution due to the performance and transmission line driving capabilities needed by the family for high-frequency operations.

The other factor, the L_p component of equation (1), affects the noise generated. The amount of L_p component, or package inductance, is dependent upon lead lengths as well as the location of V_{CC} and GND pins in the package. By reducing the package inductance, the voltage spike is reduced without any adverse affects to device performance.

Noise spikes resulting from simultaneous switching of multiple outputs depend upon specific application variables. It is impractical for advanced CMOS vendors to specify and test every application condition likely to cause noise,

mainly because simultaneous switching effects cannot be accurately tested on production IC testers available. Some of the ways to minimize the effects of simultaneous switching are:

- Implement all circuits in Surface Mounted Technology (SMT)
- Add series damping resistors to outputs
- Use fewer outputs per package (e.g., four out of eight outputs).

None of these options are ideal. SMT will still experience noise levels above the TTL logic threshold level with end-pin V_{CC} and GND. Series damping resistors slow the propagation delay times as well as reduce the output drive current capability and increase the component count. Utilizing fewer outputs limits application usage and decreases logic density dramatically.

1.1.4 The TI Simultaneous Switching Solution

To decrease the magnitude of voltage noise generated in high-speed advanced CMOS logic during simultaneous switching of multiple outputs, TI has adopted a new pinout for its EPIC™ ACL family. The pinouts for both AC/ACT in all package types will incorporate center V_{CC} and GND pin(s). The center-pin configuration helps to reduce the effective package inductance that is directly related to the voltage noise spike caused during simultaneous switching of multiple outputs. Additional ground pins and supply pins have been added to the center-pin configuration to further reduce the magnitude of the voltage spikes. To further aid the designer in the implementation of ACL, Texas Instruments will utilize a new flow-through pinout architecture which will simplify circuit board layout. Inputs will surround V_{CC} pins, outputs will surround GND pins, and where possible, control pins will be strategically located at the ends of the package.

Use of the new center-pin packages for EPIC™ ACL instead of end-pin packaging allows the designer to minimize simultaneous switching noise effects without having to adopt extreme care and extensive engineering efforts to ensure reliable system performance.

As discussed, the largest contributing factor to the amount of package inductance is the length from the V_{CC} pin or GND pin to the die. Traditional pinouts place V_{CC} and GND pins at the opposite ends of the package, resulting in the maximum possible inductance through the lead frame. By relocating the V_{CC} and GND pin locations, the inductance can be significantly reduced. Figures 1.1-1 and 1.1-2 plot the pin inductance associated with each pin for both a 14-pin and 24-pin device in the plastic DIP and small outline (SO) packages. As expected, the lowest inductance occurs at the pin locations with the shortest lead length to the internal die. These pins are located at the center of the package. By placing V_{CC} and GND pins at the center of the package, the lead length is reduced from the die to the external package. This results in a significant reduction of the L_p factor of equation (1), directly decreasing the voltage noise spike.

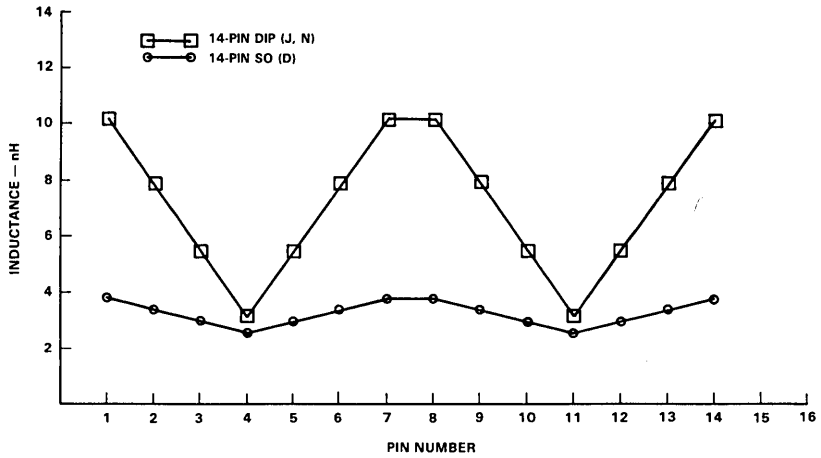


Figure 1.1-1. Pin Inductance for a 14-Pin Package, End-Pin Configuration

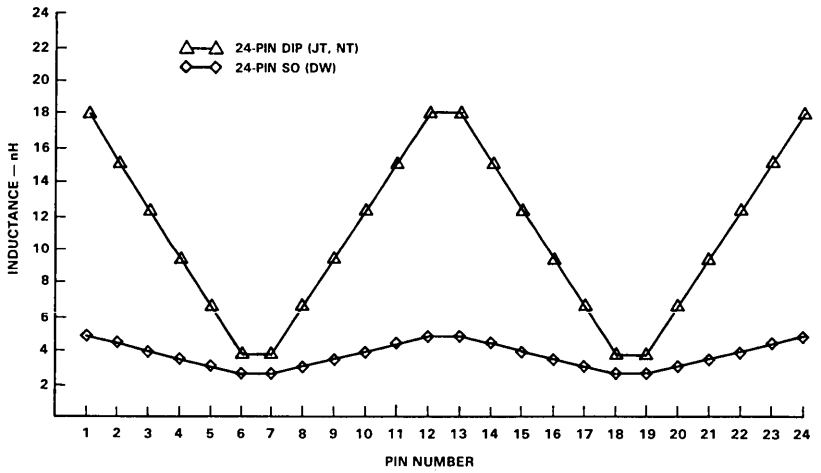


Figure 1.1-2. Pin Inductance for a 24-Pin Package, End-Pin Configuration

In order to offer a consistent switching performance across the EPIC™ ACL family, Texas Instruments continued its inductance analysis to determine if the number of V_{CC} and GND pins per package affects the amount of package inductance. It was found that the number of outputs is directly related to the noise amplitude. In functions with three or more outputs, TI added more V_{CC} and GND pins in order to offer an advanced CMOS family which would exhibit similar noise performance across the entire family breadth. The additional V_{CC} and GND pins accomplish this for TI.

As indicated in Table 1.1-1, the amplitude of the noise voltage is further reduced by increasing the number of V_{CC} and GND pins offered per package. A 20-pin DIP package with conventional end-pin pinout exhibits a significant level of inductance as compared to a 20-pin DIP with multiple V_{CC} and GND pins in the center of the package (13.7 nH vs 1.7 nH for V_{CC} and 1.1 nH for GND). With the SO(DW) package in Table 1.1-1, the package inductance is further reduced because the lead length is inherently shorter from V_{CC} or GND. Coupled with multiple V_{CC} and GND pins, the package inductance is reduced further (4.2 nH vs 1.2 nH for V_{CC} and 0.7 nH for GND).

Table 1.1-1. Inductance vs Package Configuration

TYPE PACKAGE	NUMBER OF PINS	POWER	V_{CC}/GND PIN NO.	EFFECTIVE POWER PIN INDUCTANCE L_p (nH)
DIP (J,N)	14	END	14/7	10.2
DIP (J.N)	14	CTR	11/4	3.2
SO (D)	14	END	14/7	3.8
SO (D)	14	CTR	11/4	2.6
DIP (J,N)	16	END	16/8	10.5
DIP (J,N)	16	CTR	12/4	3.3
DIP (J,N)	16	CTR	12,13/4,5	1.7
SO (D)	16	END	16/8	4.3
SO (D)	16	CTR	12/4	2.4
SO (D)	16	CTR	12,13/4,5	1.2
DIP (J,N)	20	END	20/10	13.7
DIP (J,N)	20	CTR	15/5	3.4
DIP (J,N)	20	CTR	15,16/4,5,6,7	1.7/1.1
SO (DW)	20	END	20/10	4.2
SO (DW)	20	CTR	15/5	2.4
SO (DW)	20	CTR	15,16/4,5,6,7	1.2/0.7
DIP (JT,NT)	24	END	24/12	18.1
DIP (JT,NT)	24	CTR	18,19/5,6,7,8	1.9/1.2
SO (DW)	24	END	24/12	4.9
SO (DW)	24	CTR	18,19/5,6,7,8	1.3/0.8
DIP (J,N)	28	END	28/14	21.0
DIP (J,N)	28	CTR	21,22/6,7,8,9	2.1/1.3
SO (DW)	28	END	28/14	5.4
SO (DW)	28	CTR	21,22/6,7,8,9	1.4/0.9

To optimize simultaneous switching performance of EPIC™ ACLs, TI determined the number of V_{CC} and GND pins to be employed per package. Using the new pinout configuration, the number of pins is directly related to the maximum number of outputs that can be simultaneously switched and to the package inductance that can be tolerated with the associated loads and edge rates. For DIPS and SMT packages, Table 1.1-2 indicates the number and locations of V_{CC} and GND pins per package. The use of centrally located V_{CC} and GND pins will enable designers to use EPIC™ ACL products in simultaneous switching applications with minimal noise effects.

Table 1.1-2. Number and Location of V_{CC}/GND Pins for ACL Package

PACKAGE PIN NO.	NO. OUTPUTS SWITCHING	GROUND PIN(S)	V_{CC} PIN(S)
14-Pin	1 or 2	Pin 4	Pin 11
16-Pin	1 or 2	Pin 4	Pin 12
16-Pin	3 or 4	Pin 4,5	Pin 12,13
20-Pin	1 or 2	Pin 5	Pin 15
20-Pin	3 or more	Pin 4,5,6,7	Pin 15,16
24-Pin	3 or more	Pin 5,6,7,8	Pin 18,19
28-Pin	3 or more	Pin 6.7.8.9	Pin 21,22

1.1.5 Evaluation Results

The measured data shown in Figures 1.1-3 through 1.1-5 supports the need for V_{CC} and GND pins to be located at the center of the package. The device utilized for this data was a '244 function, an octal buffer/line driver. The data was measured under typical system conditions, which consisted of a 5.5-V supply voltage with a 50-pF capacitor load operating at a temperature of 25 °C. The test circuit used is shown in Figure 1.1-6. The test performed demonstrates an excessive level of voltage produced during the condition of the output held low while seven outputs are simultaneously switched from high to low. The resulting instability can impact system integrity if not controlled. Similar results occur for low-to-high switching with one output held high.

Advanced CMOS '244 devices of two other manufacturers, Figure 1.1-3 and 1.1-4, were put through the same testing procedure, and a noise spike of greater than 2.0 V was generated. A 2.0-V spike reduced the effective noise margin by almost 90% which is unacceptable to many system designers because it violates the V_{IL} maximum specifications.

Figure 1.1-5 shows that the package chosen by TI for the advanced CMOS '244 function, 74AC11244, reduces the noise to a usable level. To gather this data, the test condition was simulated for the 74AC11244 device. Use

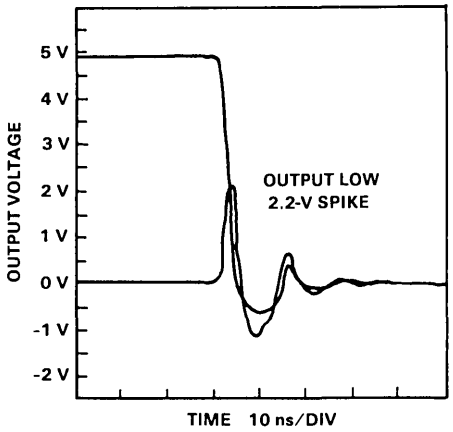


Figure 1.1-3. Vendor A Advanced CMOS '244 20-Pin Plastic DIP, 1 V_{CC}/1 GND, End-Pin Package

of the center-pin package controls the level of voltage noise produced, thus enabling the system designer to design with noise levels equal to or less than levels of advanced bipolar families currently in use. For this reason, TI has chosen to offer the EPIC™ ACL product line with center-pin V_{CC} and GND pins. In conjunction with TI, Signetics/Philips is also offering an advanced CMOS logic family with center-pin pinouts.

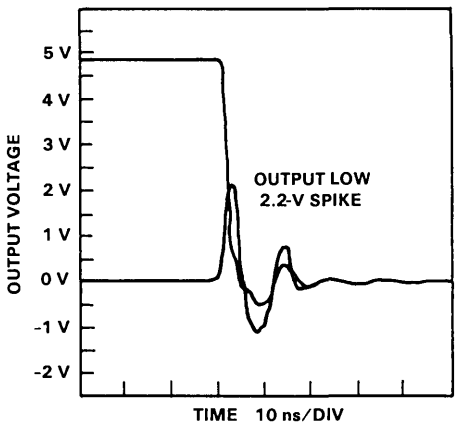
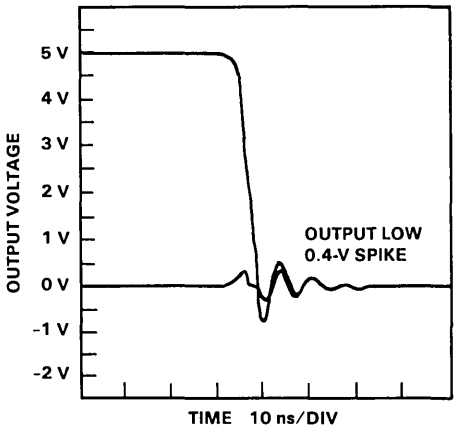


Figure 1.1-4. Vendor B Advanced CMOS '244 20-Pin Plastic DIP, 1 V_{CC}/1 GND, End-Pin Package



NOTE: Ground looping was not taken into account.

Figure 1.1-5. Texas Instruments 'AC11244 24-Pin Plastic DIP, 2 V_{CC}/4 GND, Center-Pin Package

1.1.6 Flow-Through Architecture

TI is not only offering the center-pin package to minimize simultaneous switching noise effects but has adopted a new flow-through pinout architecture to simplify system design and layout. Inputs will surround V_{CC} pins, outputs will surround GND pins, and control pins will be strategically located, where possible, at package ends. The new flow-through pinouts will

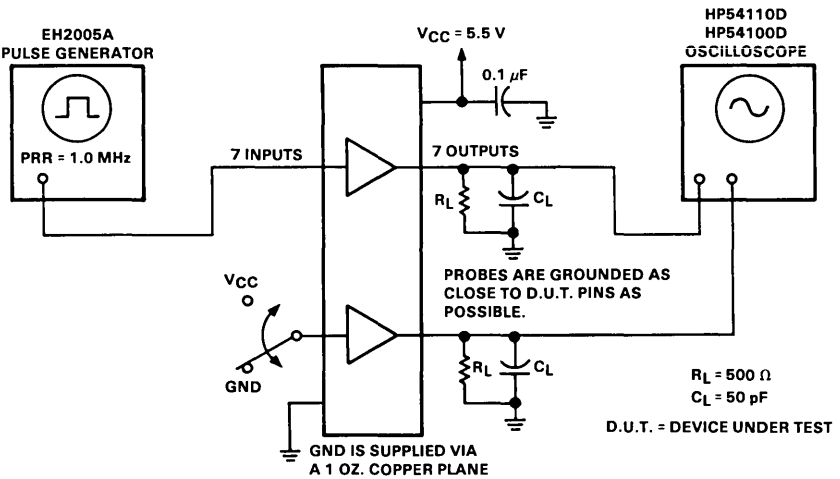


Figure 1.1-6. Test Circuitry

ease decoupling layout and enable designers to reduce interconnect line lengths, further enhancing system noise performance. New designs will be easier to implement. The flow-through pinout approach eases board layout as well as the process of system troubleshooting, because input and corresponding output signal pins are now located on opposite sides of the package.

Figures 1.1-7 through 1.1-9 show the new flow-through pinout diagrams for three functions: '00, quad gate; '74, flip-flop; and '240, an octal buffer/driver device.

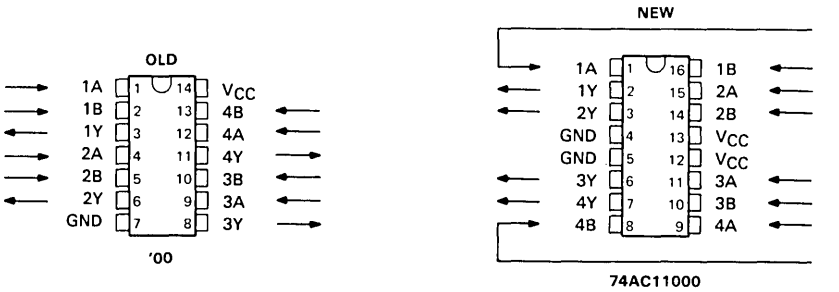


Figure 1.1-7. Flow-Through Pinout Architecture for an 'AC11000 Device

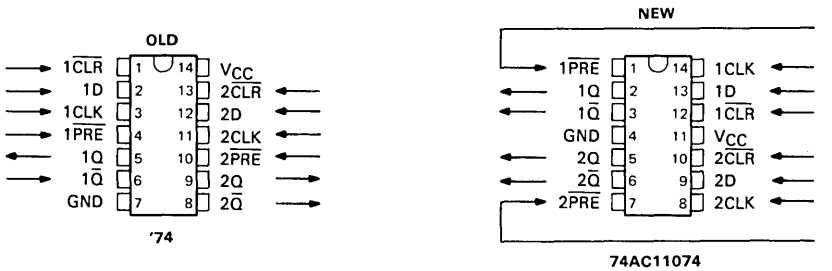


Figure 1.1-8. Flow-Through Pinout Architecture for an 'AC11074 Device

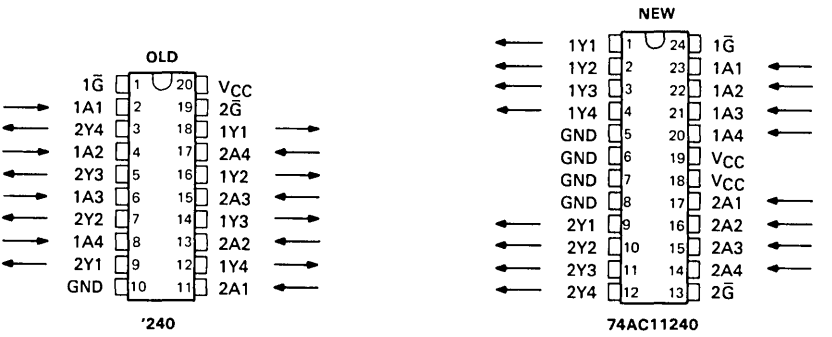


Figure 1.1-9. Flow-Through Pinout Architecture for an 'AC11240 Device

1.1.7 Device Pinouts

For the convenience of system design engineers, flow-through pinouts for each function in the EPIC™ ACL family are provided. Note that the 'ACT version has the identical pinout as its 'AC counterpart. All package types offered for the EPIC™ ACL family will incorporate the center-pin V_{CC} and GND pinouts provided for each function.

1.1.8 Symbolization

EPIC™ ACL devices will be designated 54/74AC11XXXYY where XXX indicates the device function (Note: '00 becomes '000) and YY indicates the package type: N, NT, D, DW, J, JT, or FK. For the TTL-compatible versions, substitute ACT for AC. The 11XXX has been adopted by both Texas Instruments and Signetics/Philips as the indicator for the center-pin configuration to differentiate the EPIC™ ACL product from existing advanced high-speed logic utilizing the old pinout configuration in the marketplace today. (See Figure 1.1-10.)

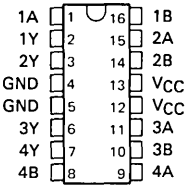
	74	AC	11	XXX	N
1	2	3	4	5	6

1. PREFIX
   - BLANK = STANDARD PRODUCT
   - SNJ = MIL-STD-883 PROCESSED
   - JANB = MIL-M-38510 PROCESSED
2. TEMPERATURE RANGE
   - 74 = COMMERCIAL/INDUSTRIAL
   - 54 = MILITARY
3. FAMILY CODE
   - AC = ADVANCED CMOS
   - ACT = TTL-COMPATIBLE ADVANCED CMOS
4. PIN DESIGNATOR
   - 11 = CENTER-PIN V_{CC}/GND
5. DEVICE TYPE
   NOTE: THIS IS A THREE-CHARACTER CODE,
   00 NOW = 000
6. PACKAGE CODE
   - N = PLASTIC DIP
   - NT = PLASTIC SLIM-LINE DIP
   - J = CERAMIC DIP
   - JT = CERAMIC SLIM-LINE DIP
   - D = PLASTIC SMALL OUTLINE
   - DW = PLASTIC WIDE BODY SMALL OUTLINE
   - FK = LEADLESS CERAMIC CHIP CARRIER

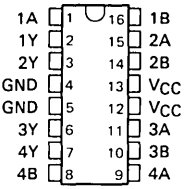
Figure 1.1-10. Symbolization and Package Information

1.1.9 EPIC™ ACL Pinouts

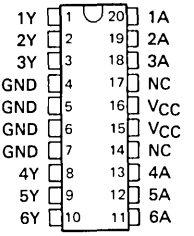
'AC11000, 'ACT11000
QUADRUPLE 2-INPUT
POSITIVE-NAND GATES
(TOP VIEW)



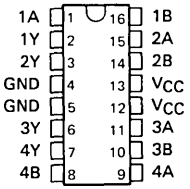
'AC11002, 'ACT11002
QUADRUPLE 2-INPUT
POSITIVE-NOR GATES
(TOP VIEW)



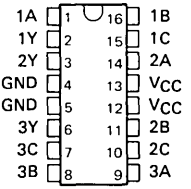
'AC11004, 'ACT11004
HEX INVERTERS
(TOP VIEW)



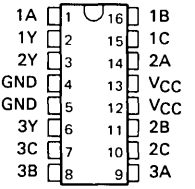
'AC11008, 'ACT11008
QUADRUPLE 2-INPUT
POSITIVE-AND GATES
(TOP VIEW)



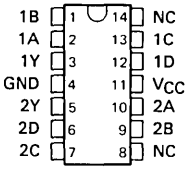
'AC11010, 'ACT11010
TRIPLE 3-INPUT
POSITIVE-NAND GATES
(TOP VIEW)



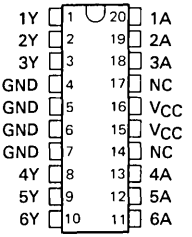
'AC11011, 'ACT11011
TRIPLE 3-INPUT
POSITIVE-AND GATES
(TOP VIEW)



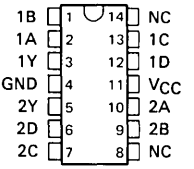
'AC11013, 'ACT11013
DUAL 4-INPUT GATES
(TOP VIEW)



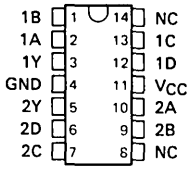
'AC11014, 'ACT11014
HEX INVERTERS
(TOP VIEW)



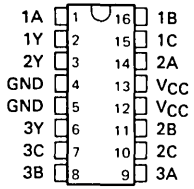
'AC11020, 'ACT11020
DUAL 4-INPUT
POSITIVE-NAND GATES
(TOP VIEW)



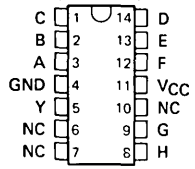
'AC11021, 'ACT11021
DUAL 4-INPUT POSITIVE-AND GATES
(TOP VIEW)



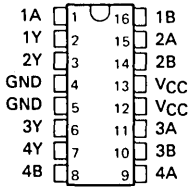
'AC11027, 'ACT11027
TRIPLE 3-INPUT POSITIVE-NOR GATES
(TOP VIEW)



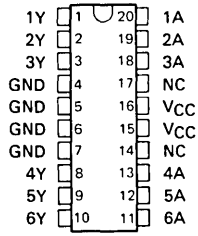
'AC11030, 'ACT11030
8-INPUT POSITIVE-NAND GATES
(TOP VIEW)



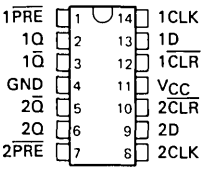
'AC11032, 'ACT11032
QUADRUPLE 2-INPUT POSITIVE-OR GATES
(TOP VIEW)



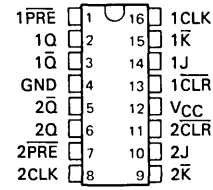
'AC11034, 'ACT11034
HEX NONINVERTERS
(TOP VIEW)



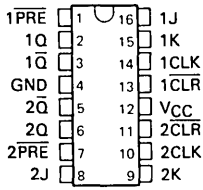
'AC11074, 'ACT11074
DUAL D-TYPE POSITIVE-EDGE TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET
(TOP VIEW)



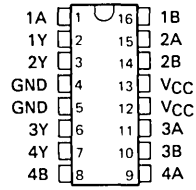
'AC11109, 'ACT11109
DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET
(TOP VIEW)



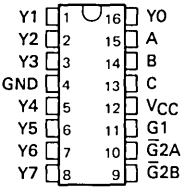
'AC11112, 'ACT11112
DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET
(TOP VIEW)



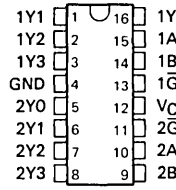
'AC11132, 'ACT11132
QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS
(TOP VIEW)



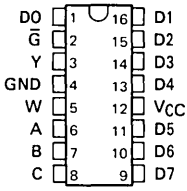
'AC11138, 'ACT11138
3-LINE TO 8-LINE
DECODERS/DEMULTIPLEXERS
(TOP VIEW)



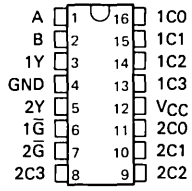
'AC11139, 'ACT11139
DUAL 2-LINE TO 4-LINE
DECODERS/DEMULTIPLEXERS
(TOP VIEW)



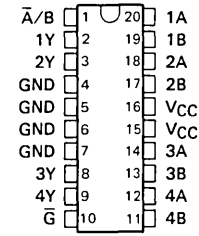
'AC11151, 'ACT11151
1 OF 8 DATA
SELECTORS/MULTIPLEXERS
(TOP VIEW)



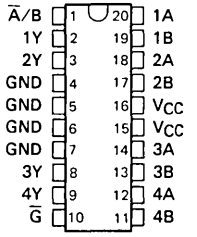
'AC11153, 'ACT11153
DUAL 4-LINE TO 1-LINE DATA
SELECTORS/MULTIPLEXERS
(TOP VIEW)



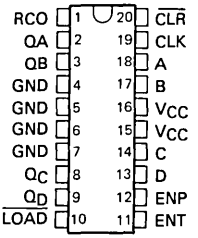
'AC11157, 'ACT11157
QUADRUPLE 1 OF 2
DATA SELECTORS/MULTIPLEXERS
(TOP VIEW)



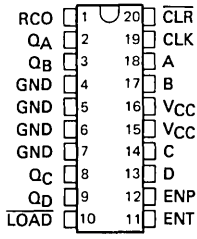
'AC11158, 'ACT11158
QUADRUPLE 1 OF 2 DATA
SELECTORS/MULTIPLEXERS
(TOP VIEW)



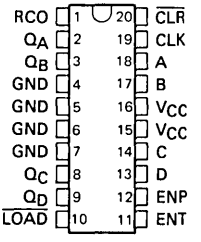
'AC11160, 'ACT11160
SYNCHRONOUS 4-BIT
BINARY COUNTERS
(TOP VIEW)



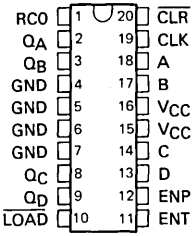
'AC11161, 'ACT11161
SYNCHRONOUS 4-BIT
DECADE COUNTERS
(TOP VIEW)



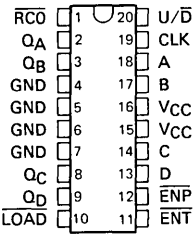
'AC11162, 'ACT11162
SYNCHRONOUS 4-BIT
BINARY COUNTERS
(TOP VIEW)



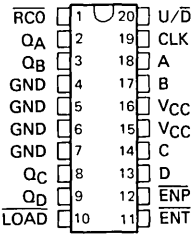
'AC11163, 'ACT11163
SYNCHRONOUS 4-BIT DECADE COUNTERS
(TOP VIEW)



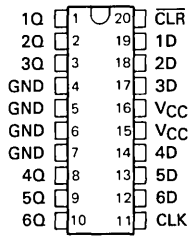
'AC11168, 'ACT11168
SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTERS
(TOP VIEW)



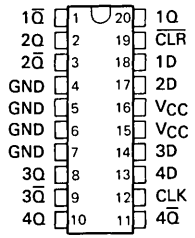
'AC11169, 'ACT11169
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS
(TOP VIEW)



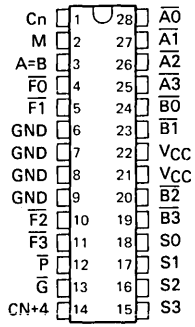
'AC11174, 'ACT11174
HEX D-TYPE FLIP-FLOPS WITH CLEAR
(TOP VIEW)



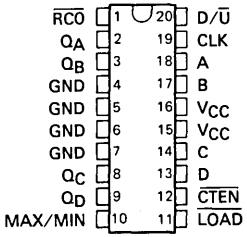
'AC11175, 'ACT11175
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR
(TOP VIEW)



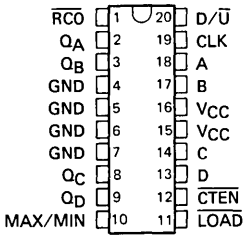
'AC11181, 'ACT11181
ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS
(TOP VIEW)



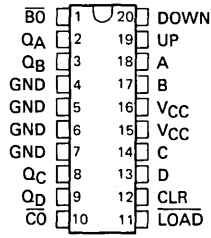
'AC11190, 'ACT11190
SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTERS
(TOP VIEW)



'AC11191, 'ACT11191
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS
(TOP VIEW)

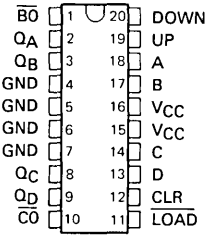


'AC11192, 'ACT11192
SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTERS (DUAL CLOCK WITH CLEAR)
(TOP VIEW)



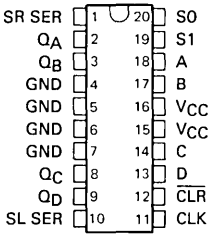
'AC11193, 'ACT11193
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS (DUAL CLOCK WITH CLEAR)

(TOP VIEW)



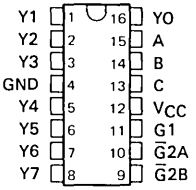
'AC11194, 'ACT11194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

(TOP VIEW)



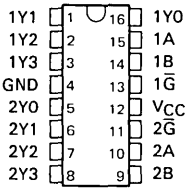
'AC11238, 'ACT11238
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

(TOP VIEW)



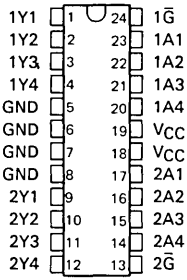
'AC11239, 'ACT11239
DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

(TOP VIEW)



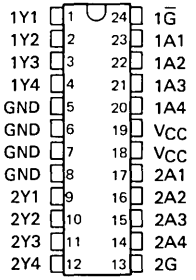
'AC11240, 'ACT11240
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

(TOP VIEW)



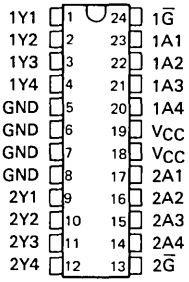
'AC11241, 'ACT11241
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

(TOP VIEW)



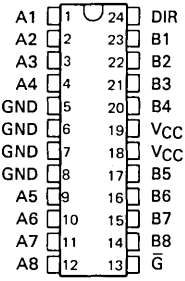
'AC11244, 'ACT11244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

(TOP VIEW)



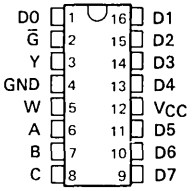
'AC11245, 'ACT11245
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

(TOP VIEW)

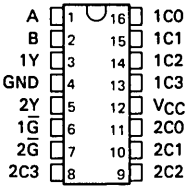


'AC11251 'ACT11251
1 OF 8 DATA SELECTORS/ MULTIPLEXERS WITH 3-STATE OUTPUTS

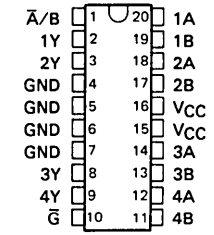
(TOP VIEW)



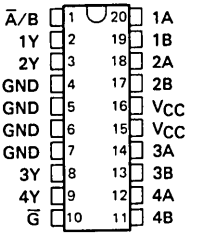
'AC11253, 'ACT11253
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS
(TOP VIEW)



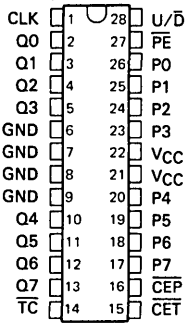
'AC11257, 'ACT11257
QUADRUPLE 1 OF 2 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS
(TOP VIEW)



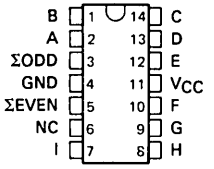
'AC11258, 'ACT11258
QUADRUPLE 1 OF 2 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS
(TOP VIEW)



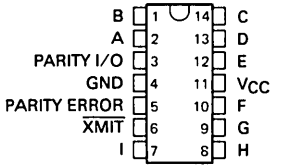
'AC11269, 'ACT11269
8-BIT BIDIRECTIONAL BINARY COUNTER
(TOP VIEW)



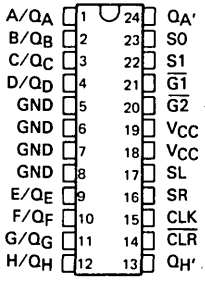
'AC11280, 'ACT11280
9-BIT PARITY GENERATORS/CHECKERS
(TOP VIEW)



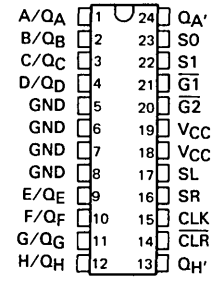
'AC11286, 'ACT11286
9-BIT PARITY GENERATORS/CHECKERS WITH BUS DRIVER PARITY I/O PORT
(TOP VIEW)



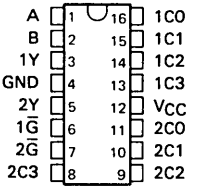
'AC11299, 'ACT11299
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS
(TOP VIEW)



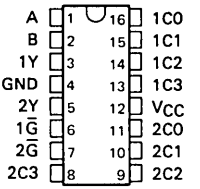
'AC11323, 'ACT11323
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS
(TOP VIEW)



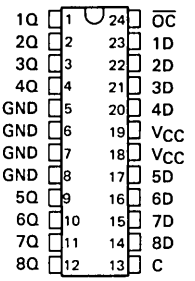
'AC11352 'ACT11352
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS
(TOP VIEW)



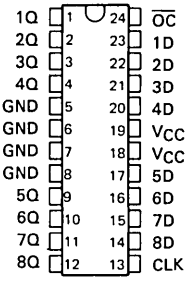
'AC11353, 'ACT11353
DUAL 1 OF 4 DATA SELECTORS/ MULTIPLEXERS WITH 3-STATE OUTPUTS
(TOP VIEW)



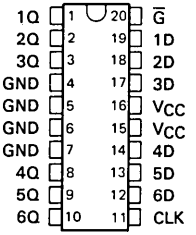
'AC11373, 'ACT11373
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



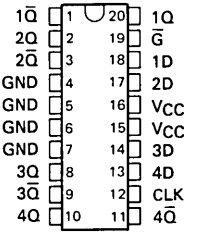
'AC11374, 'ACT11374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
(TOP VIEW)



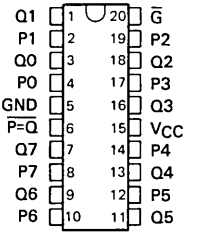
'AC11378, 'ACT11378
HEX D-TYPE FLIP-FLOPS WITH CLOCK ENABLE
(TOP VIEW)



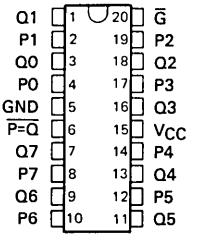
'AC11379, 'ACT11379
QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR
(TOP VIEW)



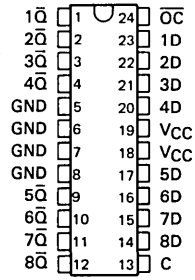
'AC11520, 'ACT11520
8-BIT IDENTITY COMPARATOR
(TOP VIEW)



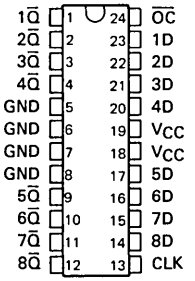
'AC11521, 'ACT11521
8-BIT IDENTITY COMPARATOR
(TOP VIEW)



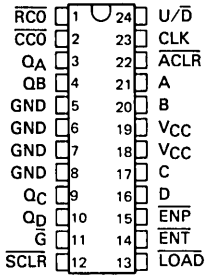
'AC11533, 'ACT11533
OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUT
(TOP VIEW)



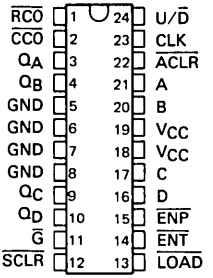
'AC11534, 'ACT11534
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUT
(TOP VIEW)



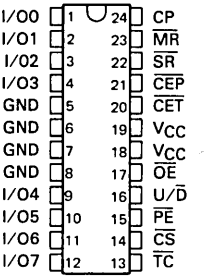
'AC11568, 'ACT11568
SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTERS WITH 3-STATE OUTPUTS
(TOP VIEW)



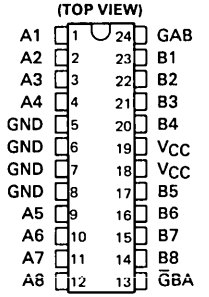
'AC11569, 'ACT11569
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS WITH 3-STATE OUTPUTS
(TOP VIEW)



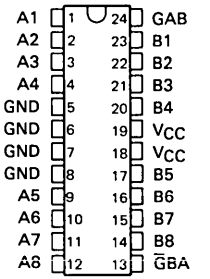
'AC11579, 'ACT11579
8-BIT BIDIRECTIONAL BINARY COUNTER WITH 3-STATE OUTPUTS
(TOP VIEW)



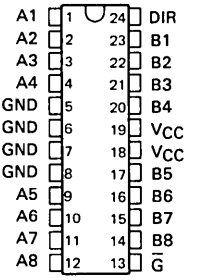
'AC11620, 'ACT11620
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



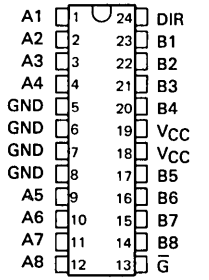
'AC11623, 'ACT11623
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



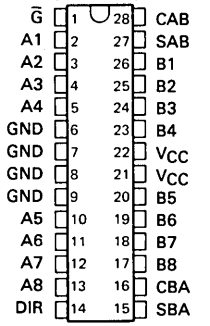
'AC11640, 'ACT11640
OCTAL BUS TRANSCEIVERS
(TOP VIEW)



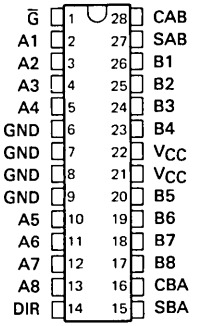
'AC11643, 'ACT11643
OCTAL BUS TRANSCEIVERS
(TOP VIEW)



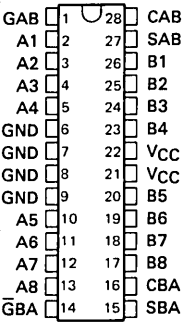
'AC11646, 'ACT11646
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS
(TOP VIEW)



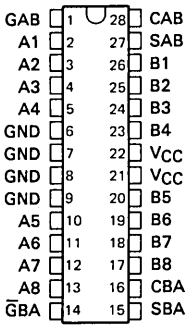
'AC11648, 'ACT11648
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS
(TOP VIEW)



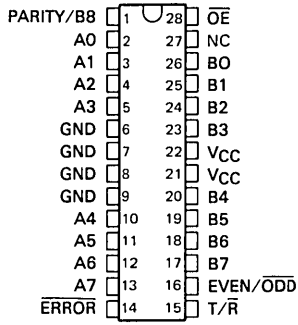
'AC11651, 'ACT11651
OCTAL BUS TRANSCEIVERS AND REGISTERS
(TOP VIEW)



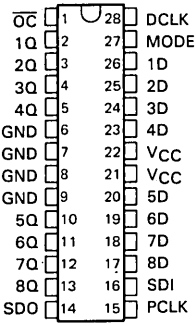
'AC11652, 'ACT11652
OCTAL BUS TRANSCEIVERS AND REGISTERS
(TOP VIEW)



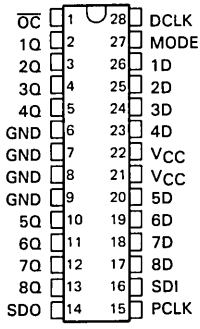
'AC11657, 'ACT11657
OCTAL BIDIRECTIONAL TRANSCEIVERS WITH 8-BIT PARITY GENERATOR/CHECKER AND 3-STATE OUTPUTS
(TOP VIEW)



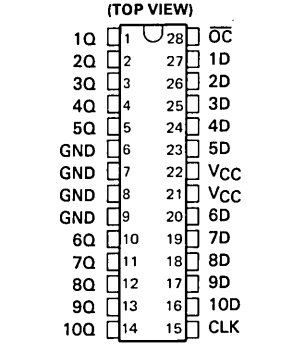
'AC11818, 'ACT11818
DIAGNOSTIC/PIPELINE REGISTER
(TOP VIEW)



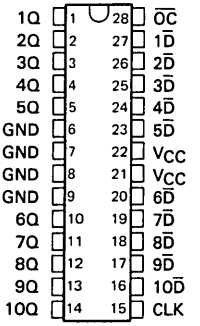
'AC11819, 'ACT11819
DIAGNOSTIC/PIPELINE REGISTER
(TOP VIEW)



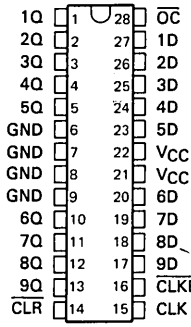
'AC11821, 'ACT11821
10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS
(TOP VIEW)



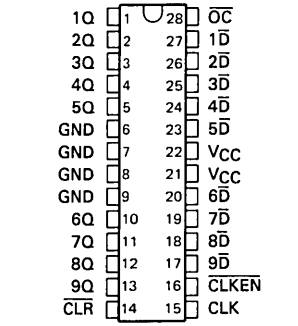
'AC11822, 'ACT11822
10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS
(TOP VIEW)



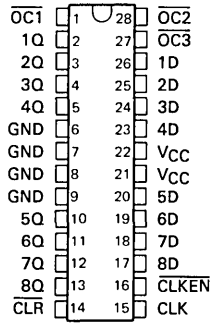
'AC11823, 'ACT11823
9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS
(TOP VIEW)



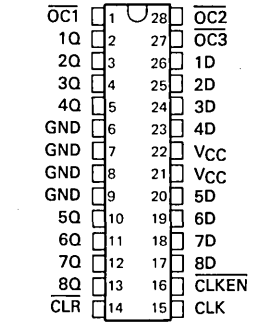
'AC11824, 'ACT11824
9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS
(TOP VIEW)



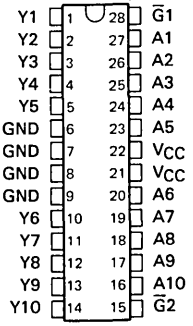
'AC11825, 'ACT11825
8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS
(TOP VIEW)



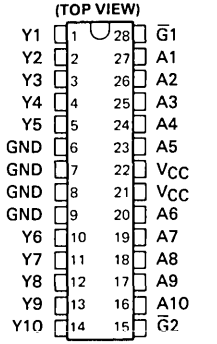
'AC11826, 'ACT11826
8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS
(TOP VIEW)



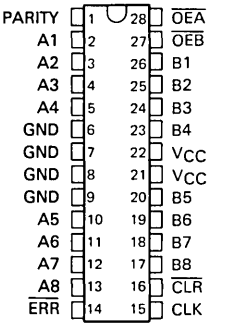
'AC11827, 'ACT11827
10-BIT BUFFERS WITH 3-STATE OUTPUTS
(TOP VIEW)



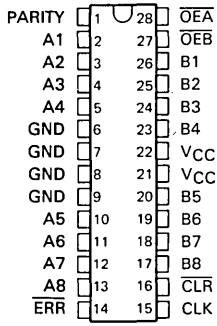
'AC11828, 'ACT11828
10-BIT BUFFERS WITH 3-STATE OUTPUTS
(TOP VIEW)



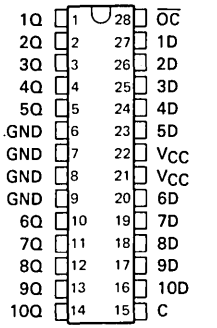
'AC11833, 'ACT11833
PARITY BUS TRANSCEIVERS
(TOP VIEW)



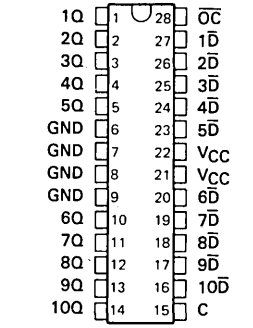
'AC11834, 'ACT11834
PARITY BUS TRANSCEIVERS
(TOP VIEW)



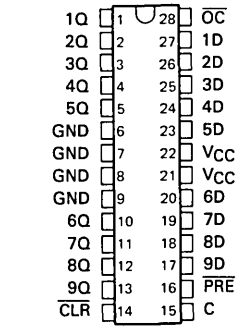
'AC11841, 'ACT11841
10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



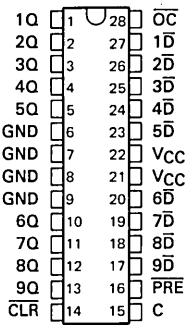
'AC11842, 'ACT11842
10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



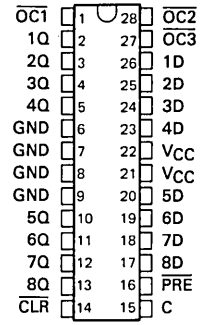
'AC11843, 'ACT11843
9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



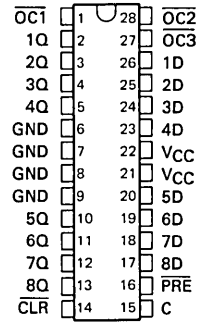
'AC11844, 'ACT11844
9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



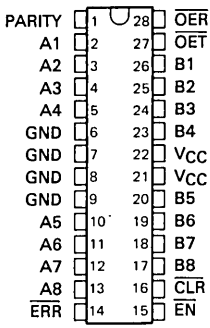
'AC11845, 'ACT11845
8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



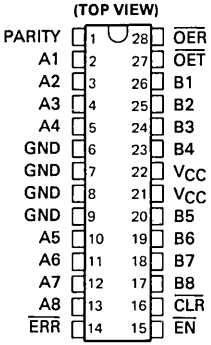
'AC11846, 'ACT11846
8-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



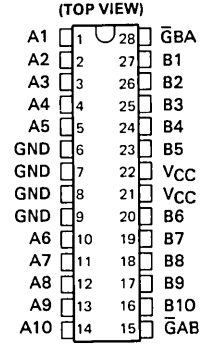
'AC11853, 'ACT11853
PARITY BUS TRANSCEIVERS
(TOP VIEW)



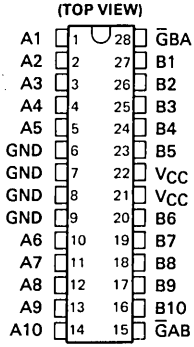
'AC11854, 'ACT11854
PARITY BUS TRANSCEIVERS
(TOP VIEW)



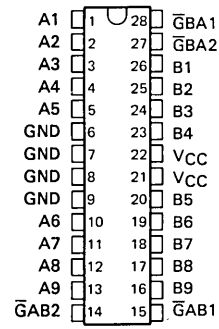
'AC11861, 'ACT11861
10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



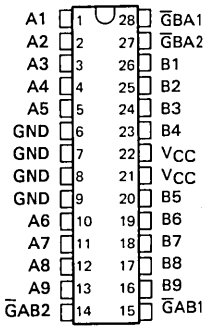
'AC11862, 'ACT11862
10-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



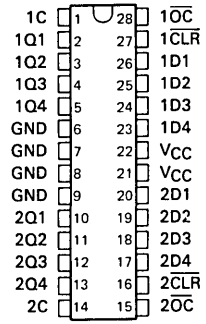
'AC11863, 'ACT11863
9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



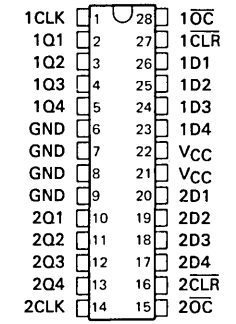
'AC11864, 'ACT11864
9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS
(TOP VIEW)



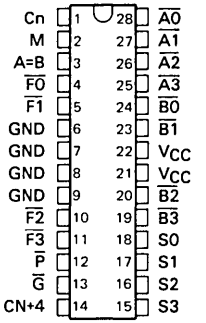
'AC11873, 'ACT11873
DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS
(TOP VIEW)



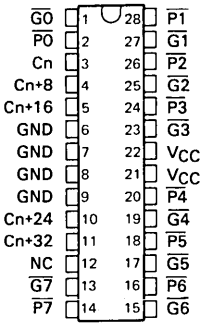
'AC11874, 'ACT11874
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS
(TOP VIEW)



'AC11881, 'ACT11881
ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS
(TOP VIEW)



'AC11882, 'ACT11882
32-BIT LOOK-AHEAD CARRY GENERATORS
(TOP VIEW)



1.1.10 Summary

Simultaneous switching of multiple outputs can greatly hinder system performance. By using the center-pin solution, as shown in this document, the system designer can now minimize output glitches, loss of stored data, and speed degradation. This also minimizes any reduction in system noise immunity from the noise problems associated with simultaneous switching of multiple outputs in high-speed logic. The designer can also implement a flow-through design with new flow-through pinout configuration of EPIC™ ACL.

2 Data Sheet Information

2.1 EPIC™ Advanced CMOS Logic Data Sheets†

2.1.1 Introduction

To assist component and system design engineers with Texas Instruments Advanced CMOS Logic (ACL) products, this application report is a brief synopsis of the information available from a typical ACL data sheet. Information will include a brief description of the terms, definitions, and testing procedures currently being used for commercial and military specifications. The symbols, terms, and definitions are all in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

2.1.2 Dissecting the ACL Data Sheet

The ACL data sheet presents pertinent technical information for a particular device and is organized for quick access. To describe the organization that is used in all ACL data sheets, this application report shows the dissection of a typical ACL data sheet. The 'AC11244‡ and the 'AC11074‡ data sheets are used as examples.

ACL data sheets are organized in the same manner as ALS or AS data sheets. There are six major sections contained in each data sheet. The sections are as follows:

1. Macro description
2. Absolute maximum ratings
3. Recommended operating conditions
4. Electrical characteristics
5. Timing requirements
6. Switching characteristics

Each of these sections is discussed in the following paragraphs.

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†Written by V. Klein and R. Schwartz

‡This report also highlights differences between 'AC11074 and 'AC11244, and their TTL-compatible counterparts, 'ACT11074 and 'ACT11244.

2.1.3 Macro Description

The first section of a data sheet (Figure 2.1-1) contains all of the general information for a device. This information will include:

1. Device number and title
2. Description of the main features and benefits of the device
3. Package options and pinouts. The center-pin V_{CC} and ground and the flow-through architecture are shown here. Actual package dimensions and other package information will be available in the mechanical data section of the ACL data book and are available in Section 2.2 of this handbook.
4. Description
5. Function table (if applicable). See Functional Testing paragraph.
6. Logic symbol in accordance with the ANSI/IEEE Std 91-1984 and IEC Publication 617-12
7. Product development stage note — a standard disclaimer used in conjunction with the words PRODUCT PREVIEW, PRODUCTION DATA, or ADVANCE INFORMATION on all pages.

2.1.4 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)

The absolute maximum ratings table (Figure 2.1-2) specifies the stress levels that, if exceeded, may cause permanent damage to the device. However, these are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Also, exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Absolute maximum ratings are not tested values. These are the values established by Texas Instruments beyond which Texas Instruments does not guarantee continued reliable operation of the device.

As the note in Figure 2.1-2 indicates, there are two absolute maximums that may be exceeded under the right conditions. The input and output voltage ratings, V_I and V_O, may be exceeded if the input and output maximum clamp current ratings, I_{IK} and I_{OK}, are observed.

All currents are defined with respect to conventional current flow into the respective terminal of the integrated circuit. This means that any current that actually flows out of the respective terminal will be considered to be a negative quantity.

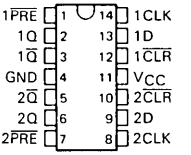
All limits are given according to the absolute-magnitude convention with a few exceptions. In this convention, maximum refers to the greater magnitude limit of a range of like-signed values; if the range includes both positive and

54AC11074, 74AC11074
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

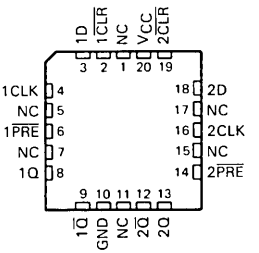
D2957, DECEMBER 1986 REVISED MARCH 1987

- New Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54AC11074 . . . J PACKAGE
74AC11074 . . . D OR N PACKAGE
(TOP VIEW)



54AC11074 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the Preset or Clear input sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the low-to-high transition of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

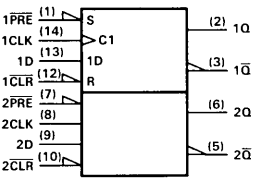
The 54AC11074 is characterized for operation over the full military temperature range of −55°C to 125°C. The 74AC11074 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high level).

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

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Figure 2.1-1. General Information

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to V_{CC} +0.5 V
Output voltage, V_O (see Note 1)	−0.5 V to V_{CC} +0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC})	±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±100 mA
Storage temperature range	−65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Figure 2.1-2. Absolute Maximum Ratings Table

negative values, both limit values are maximums. Minimum refers to the smaller magnitude limit of a range of like-signed values; if the range includes both positive and negative values, the minimum is implicitly zero. The most common exceptions to the use of the absolute magnitude convention are temperature and logic levels. Here zero does not represent the least possible quantity, so the algebraic convention is commonly accepted. In this case, maximum refers to the most positive (or least negative) value.

An explanation and definition of each of the items in the absolute maximum ratings table are provided in the following paragraphs.

2.1.4.1 Supply Voltage, V_{CC}

The maximum voltage that can safely be applied to the V_{CC} terminal with respect to the network ground of the device. Note that no data sheet parameters are guaranteed at the maximum voltage level.

2.1.4.2 Input Voltage, V_I

The maximum voltage that can safely be applied to an input terminal with respect to the network ground of the device. This maximum V_I specification may be exceeded if the input clamp current rating, I_{IK}, is observed.

2.1.4.3 Output Voltage, V_O

The maximum voltage that can safely be applied to an output terminal with respect to the network ground of the device. This maximum V_O specification may be exceeded if the output clamp current rating, I_{OK}, is observed.

2.1.4.4 Input Clamp Current, I_{IK} (V_I < 0 or V_I > V_{CC})

The maximum current that can safely flow into† an input terminal of the device at voltages below or above the normal operating range (see Figure 2.1-3).

†Current out of a terminal is given as a negative value.

2.1.4.5 Output Clamp Current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)

The maximum current that can safely flow into† an output terminal of the device at voltages below or above the normal operating range (see Figure 2.1-3).

2.1.4.6 Continuous Output Current, I_O ($V_O = 0$ To V_{CC})

The maximum output source or sink current that can safely flow into† an output terminal of the device at voltages below or above the normal operating range.

2.1.4.7 Continuous Current Through V_{CC} or GND Terminals

The maximum current that can safely flow into† the V_{CC} or GND terminals of the integrated circuit.

2.1.4.8 Storage Temperature Range

The range of temperatures over which a device can be stored without causing excessive degradation of its performance characteristics.

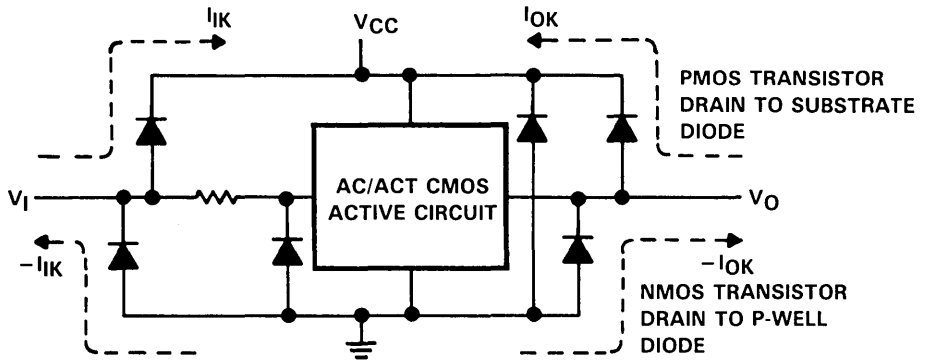


Figure 2.1-3. Input and Output Clamp Circuits

2.1.5 Recommended Operating Conditions

The Recommended Operating Conditions section of the data sheet (see Figure 2.1-4) sets the conditions over which Texas Instruments will guarantee device operation. The limits for items that appear in this section are used as test conditions for the limits that appear in the Electrical Characteristics, Timing Requirements, and Switching Characteristics sections.

†Current out of a terminal is given as a negative value.

recommended operating conditions

			54AC11074			74AC11074			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 2)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 2: No electrical or switching characteristics are specified at V_{CC} < 3 V. Operation between 2 V and 3 V is not recommended, but within that range, a device output will maintain a previously established logic state.

Figure 2.1-4. Recommended Operating Conditions Table

2.1.5.1 Supply Voltage, V_{CC}

This is the range of supply voltages for which operation of the logic element within specification limits is guaranteed. Figure 2.1-3 lists 3 V as the minimum V_{CC}. No electrical or switching characteristic is specified for V_{CC} less than 3 V. Operation between 2 V and 3 V is not recommended, but within that range a device output will maintain a previously established logic state.

2.1.5.2 High-Level Input Voltage, V_{IH}

This defines the more positive of the two ranges of values used to represent the binary variables. A voltage within this range corresponds to the logic-1 state in positive logic or the logic-0 state in negative logic. Only positive logic is used in ACL data sheets.

A minimum is specified that is the least positive value of input voltage for which the logic element is guaranteed to recognize that signal as a high-logic-level signal.

V_{IH} min is guaranteed for all inputs. Since V_{IH} min is used to set up V_{OH}, V_{OL}, I_{OZH}, and I_{OZL} tests, all possible combinations of input thresholds may not be verified. The nondata inputs (e.g., direction, clear, enable, and preset) may be considered unused inputs and may not be at threshold conditions. These inputs control functions that can cause all the outputs to switch simultaneously. The noise that can be generated by switching a majority of the outputs at one time can cause significant tester ground and V_{CC} movement. This can result in false test measurements.

2.1.5.3 Low-Level Input Voltage, V_{IL}

This defines the less positive of the two ranges of values used to represent the binary variables. A voltage within this range corresponds to the logic-0 state in positive logic or the logic-1 state in negative logic. Only positive logic is used in ACL data sheets.

A maximum is specified that is the most positive value of input voltage for which the logic element is guaranteed to recognize that signal as a low-logic-level signal.

V_{IL} max is guaranteed on all inputs. Since V_{IL} max is used to set up V_{OH}, V_{OL}, I_{OZH}, and I_{OZL} tests, all possible combinations of input thresholds may not be verified. The nondata inputs (e.g., direction, clear, enable, and preset) may be considered unused inputs and not be at threshold conditions. These inputs control functions that can cause all the outputs to switch simultaneously. The noise that can be generated by switching a majority of the outputs at one time can cause significant tester ground and V_{CC} movement. This can result in false test measurements.

2.1.5.4 High-Level Output Current, I_{OH} (Source Current)

This is the current into† an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OH} max is used as a test condition for V_{OH}. See V_{OH} testing for further details.

2.1.5.5 Low-Level Output Current, I_{OL} (Sink Current)

This is the current into† an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OL}max is used as a test condition for V_{OL}. See V_{OL} testing for further details.

2.1.5.6 Input Voltage, V_I

This is the range of input voltage levels over which the logic element is designed to operate.

V_I min and max are used as test conditions for the I_I, I_{CC}, ΔI_{CC}, C_i, and C_o tests. See these tests for further details.

2.1.5.7 Output Voltage, V_O

This is the range of output voltage levels over which the logic element is designed to operate.

V_O min and max are used as test conditions for I_{OZH} and I_{OZL}. See these tests for further details.

†Current out of a terminal is given as a negative value.

2.1.5.8 Input Transition Rise or Fall Rate, $\Delta t/\Delta v$

This is the rate of change of the input voltage waveform during a logic transition: low-to-high or high-to-low .

To avoid output waveform abnormalities, input voltage transitions should be within the range set forth in the recommended operating conditions. For more details on the effects of input edge transitions, consult Section 3.3 of this handbook.

2.1.5.9 Operating Free-Air Temperature, T_A

This is the range of temperatures over which the logic element is designed to operate.

As part of the standard testing procedure, 100% of the devices are subjected to high-temperature testing of electrical characteristics. The commercial device (74AC) is tested at 85°C. The military device (54AC) is tested at 125°C.

2.1.6 Electrical Characteristics Over Recommended Free-Air Temperature Range

The electrical characteristics section of the data sheet (see Figure 2.1-5) provides the guaranteed electrical characteristic limits of the device when tested under the conditions provided in the Recommended Operating Conditions Table as given specifically for each parameter.

2.1.6.1 High-Level Output Voltage, V_{OH}

This is the voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

V_{OH} is tested by establishing input conditions that should cause the output under test to be at a high level. The output is then forced to source the required current, as defined in the data sheet, and the output voltage is measured. The test is passed if the voltage is greater than V_{OH} min. The input voltage levels used to precondition the device are V_{IL} max and V_{IH} min as defined in the Recommended Operating Conditions. To simulate worst-case operation, all outputs are checked simultaneously, if possible. The unused inputs are at V_{IL} = 0 or V_{IH} = V_{CC} for AC devices and V_{IL} = 0 or V_{IH} = 3 V for ACT devices, depending on the desired state of the untested and tested outputs.

2.1.6.2 Low-Level Output Voltage, V_{OL}

This is the voltage at the output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

V_{OL} is tested by establishing input conditions that should cause the output under test to be at a low level. The output is then forced to sink the required current, as defined in the data sheet, and the output voltage is measured.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11244		74AC11244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −4 mA	3 V	2.58			2.4		2.48		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA†	5.5 V				3.85				
	I_{OH} = −75 mA†	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1		0.1	V
		4.5 V			0.1		0.1		0.1	
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA†	5.5 V					1.65			
	I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±10		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		160		80	μA
C_i	V_I = V_{CC} or GND	5 V		4						pF
C_o	V_O = V_{CC} or GND	5 V		10						pF

†Not more than one output should be tested at one time, and the duration of the test should not exceed 10 ms.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			54ACT11074		74ACT11074		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 μA	4.5 V	4.4			4.4		4.4		V
		5.5 V	5.4			5.4		5.4		
	I_{OH} = −24 mA	4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
	I_{OH} = −50 mA‡	5.5 V				3.85				
	I_{OH} = −75 mA‡	5.5 V						3.85		
V_{OL}	I_{OL} = 50 μA	4.5 V			0.1		0.1		0.1	V
		5.5 V			0.1		0.1		0.1	
	I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I_{OL} = 50 mA‡	5.5 V					1.65			
	I_{OL} = 75 mA‡	5.5 V							1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		80		40	μA
ΔI_{CC}§	One input at 3.4 V, Other inputs at GND or V_{CC}	5.5 V			0.9		1		1	mA
C_i	V_I = V_{CC} or GND	5 V		3.5						pF

‡Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
§This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 1 MHz	35	pF
		Outputs disabled		12	

Figure 2.1-5. Electrical Characteristics and Operating Characteristics Tables

The test is passed if the voltage is less than V_{OL} max. The input voltage levels used to precondition the device are V_{IL} max and V_{IH} min as defined in the Recommended Operating Conditions. To simulate worst-case operation, all outputs are checked simultaneously, if possible. The unused inputs are at V_{IL} = 0 or V_{IH} = V_{CC} for AC devices and V_{IL} = 0 or V_{IH} = 3 V for ACT devices, depending on the desired state of the untested and tested outputs.

2.1.6.3 Off-State Output Current, I_{OZ}

The electrical characteristic I_{OZ}, is verified utilizing two tests, I_{OZH} and I_{OZL}. Two tests are required in order to verify the integrity of both the P- and N-channel transistors.

2.1.6.3.1 Off-State Output Current with High-Level Voltage Applied, I_{OZH}

This is the current flowing into† a three-state output with input conditions established that, according to the product specification, will establish the high-impedance state at the output with a high-level voltage applied to the output.

This parameter is measured with other input conditions established that would cause the output to be at a low level if it were enabled.

I_{OZH} is tested by applying the specified voltage to the output and measuring the current into† the device with the output in the high- impedance state. Input conditions that would establish a low level on the output if it were enabled are V_{IL} = V_{IL} max and V_{IH} = V_{IH} min. Each output is individually tested. The unused inputs are at V_{IL} = 0 or V_{IH} = V_{CC} for AC devices and V_{IL} = 0 or V_{IH} = 3 V for ACT devices, depending on the desired state of the outputs not being tested.

2.1.6.3.2 Off-State Output Current with Low-Level Voltage Applied, I_{OZL}

This is the current flowing into† a three-state output with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a low-level voltage applied to the output.

This parameter is measured with other input conditions established that would cause the output to be at a high level if it were enabled.

I_{OZL} is tested by applying the specified voltage to the output and measuring the current into† the device with the output in the high-impedance state. Input conditions that would establish a high level on the output if it were enabled are V_{IL} = V_{IL} max and V_{IH} = V_{IH} min. Each output is individually tested. The unused inputs are at V_{IL} = 0 or V_{IH} = V_{CC} for AC devices, and or V_{IL} = 0 or V_{IH} = 3 V for ACT devices, depending on the desired state of the outputs not being tested.

†Current out of a terminal is given as a negative value.

2.1.6.4 Input Current, I_I

This is the current into† an input. It is tested with a V_{CC} voltage level and then a GND voltage level applied to the input. Therefore, it guarantees the maximum input current for any input voltage within the normal range of operation.

To simulate worst-case operation, inputs physically adjacent to the input under test are biased at V_{CC} or GND, whichever will increase leakage.

2.1.6.5 Supply Current, I_{CC}

This parameter is the current into† the V_{CC} supply terminal of an integrated circuit under static no-load conditions.

I_{CC} is tested by applying the specified V_{CC} level and measuring the current into† the device. The input levels used to condition the device are V_{IL} = 0 or V_{IH} = V_{CC} for AC devices and V_{IL} = 0 or V_{IH} = 3 V for ACT devices. The outputs of the device are open.

2.1.6.6 Supply Current Change, ΔI_{CC} (ACT Devices Only)

This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}. Thus, if n inputs are at voltages other than 0 V or V_{CC}, the increase in supply current will be n X ΔI_{CC}.

The change in supply current (ΔI_{CC}) is tested by applying the specified V_{CC} level, setting one input at 3.4 V and the other inputs at 0 V or V_{CC}, and then measuring the current into† the device. The outputs of the device are open.

2.1.6.7 Input Capacitance, C_i

This parameter is the internal capacitance at an input of the device. The values that are given are not tested values. They are typical values given for the benefit of the designer. These values are defined by the design and process of the device.

2.1.6.8 Output Capacitance, C_o

This parameter is the internal capacitance encountered at an output of the device. The values that are given are not tested values. They are typical values given for the benefit of the designer. These values are defined by the design and process of the device.

2.1.6.9 Power Dissipation Capacitance, C_{pd}

This parameter is the equivalent capacitance used in calculating the dynamic power dissipation for CMOS devices.

†Current out of a terminal is given as a negative value.

The dynamic power requirements for each device can be calculated by the equation:

$$P_d = (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma (C_L \times V_{CC}^2 \times f_o) \quad (1)$$

where: f_i = Input frequency in Hz
f_o = Output frequency in Hz
C_L = Load capacitance on output being measured
C_{pd} = Power dissipation capacitance

The term Σ is the summation of dissipations contributed by all the outputs, each loaded by C_L and switching at frequency f_o.

C_{pd} is a measure of the internal capacitances, given specifically for dynamic power consumption calculations. By measuring the power consumption of the device at a given frequency, C_{pd} can be calculated by the equation:

$$C_{pd} = (\text{Dynamic } I_{CC}/V_{CC} \times f_i) - C_L \quad (2)$$

The values given on the data sheet are typical values that are not tested. These values are defined by the design and process of the device.

For additional information on C_{pd} and power consumption of ACL devices, consult Section 5.4 of this handbook.

2.1.7 Timing Requirements

The timing requirement section of the data sheet (see Figure 2.1-6) is similar to the Recommended Operating Conditions section. This section addresses the timing conditions that are necessary to guarantee device functionality and only applies to sequential devices (e.g., latches and registers).

2.1.7.1 Clock Frequency, f_{clock}

This specification defines the range of clock frequencies over which a bistable device can be operated while maintaining stable transitions between logic levels at the outputs.

f_{clock} is tested by driving the clock input with a predetermined number of pulses, using a 50% duty cycle with transitions from 0 V to V_{CC} for AC devices and from 0 V to 3 V for ACT devices, at the f_{clock} max frequency specified in the data sheet. The output is then checked for the correct number of output transitions corresponding to the number of input pulses applied. The output is loaded as defined in the data sheet specifications. All other inputs use 0 V for V_{IL} or V_{CC} for V_{IH}. Each output is individually tested and not checked simultaneously with other recommended operating conditions or propagation delays. For counters, shift registers, or any other devices for which the state of the final output is dependent on the correct operation of the previous outputs, f_{clock} will be tested only on the final output, unless specified

timing requirements (see Figure 1)

			V_{CC} RANGE	T_A = 25°C		54AC11074		74AC11074		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		3.3 ±0.3 V	0	100	0	100	0	100	MHz
			5 ±0.5 V	0	125	0	125	0	125	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	3.3 ±0.3 V	4		4		4		ns
			5 ±0.5 V	4		4		4		
		CLK low or CLK high	3.3 ±0.3 V	5		5		5		
			5 ±0.5 V	4		4		4		
t_{su}	Setup time data before CLK↑	Data high or low	3.3 ±0.3 V	5		5		5		ns
			5 ±0.5 V	3.5		3.5		3.5		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	3.3 ±0.3 V	1		1		1		
			5 ±0.5 V	1		1		1		
t_h	Hold time data after CLK↑		3.3 ±0.3 V	0		0		0		ns
			5 ±0.5 V	0		0		0		

Figure 2.1-6. Timing Requirements Table

independently in the data sheet. Full functionality testing is not performed during f_{clock} testing or f_{max} testing.

2.1.7.2 Pulse Duration, t_w

This is the time interval between specified reference points on the leading and trailing edges of the pulse waveform. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.

Pulse duration is tested by applying a pulse to the specified input for a time period equal to the minimum specified in the data sheet. The pulse applied is 0 V to V_{CC} to 0 V or V_{CC} to 0 V to V_{CC} for AC devices and 0 V to 3 V to 0 V or 3 V to 0 V to 3 V for ACT devices. The device passes if the outputs switch to their expected logic levels and fails if they do not. The other inputs are at V_{IL} = 0 or V_{IH} = V_{CC} for AC devices and V_{IL} = 0 or V_{IH} = 3 V for ACT devices. Trip points used for timing measurements are shown in Figure 2.1-7. Pulse duration times are not checked simultaneously with other inputs or other Recommended Operating Conditions.

2.1.7.3 Setup Time, t_{su}

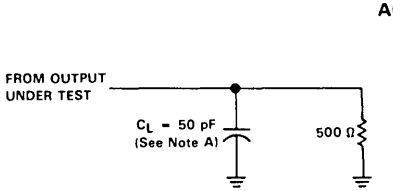
This is the time interval between the application of a signal that is maintained at a specified input terminal and a consecutive active transition at another specified input terminal.

The setup time is the actual time between two events and may be insufficient to accomplish the setup. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.

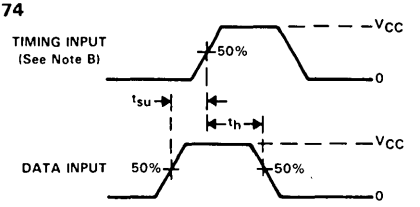
The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the logic element is guaranteed.

PARAMETER MEASUREMENT INFORMATION

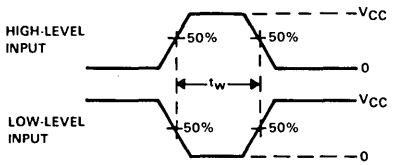
AC11074



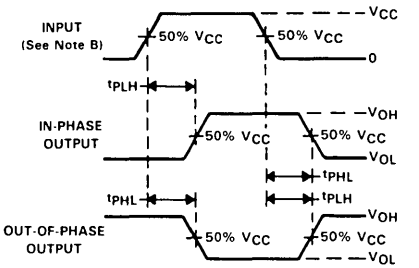
LOAD CIRCUIT



SETUP AND HOLD TIMES

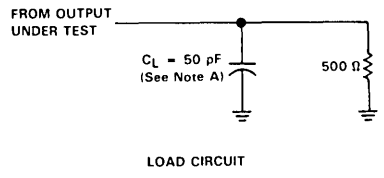


PULSE DURATION

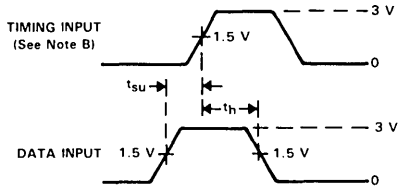


PROPAGATION DELAY TIMES

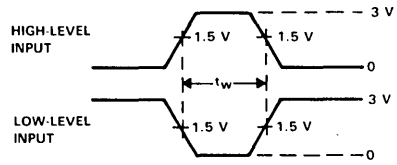
ACT11074



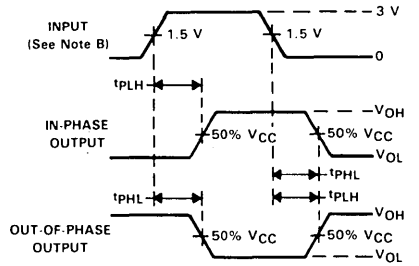
LOAD CIRCUIT



SETUP AND HOLD TIMES



PULSE DURATION



PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
For testing pulse duration: t_r = 1 to 3 ns, t_f = 1 to 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 2.1-7. Load Circuit and Voltage Waveforms

Setup is tested by switching an input to a fixed logic level at a specified time before the transition of the other input. The device passes if the outputs switch to their expected logic levels and fails if they do not. The other inputs are at V_{IL} = 0 or V_{IH} = V_{CC} for AC devices and V_{IL} = 0 or V_{IH} = 3 V for ACT devices. Trip points used for timing measurements are shown in Figure 2.1-7. Setup times are not checked simultaneously with other inputs or other Recommended Operating Conditions.

2.1.7.4 Hold Time, t_h

This is the interval during which a signal is retained at a specified input after an active transition occurs at another specified input.

The hold time is the actual time between two events and may be insufficient to accomplish the intended result. A minimum is specified that is the shortest interval for which correct operation of the logic element is guaranteed.

Hold time is tested by holding an input at a fixed logic level for the specified time after the transition of the other input. The device passes if the outputs switch to their expected logic levels and fails if they do not. The other inputs are at V_{IL} = 0 or V_{IH} = V_{CC} for AC devices and V_{IL} = 0 or V_{IH} = 3 V for ACT devices. Trip points used for timing measurements are shown in Figure 2.1-7. Hold times are not checked simultaneously with other inputs or other Recommended Operating Conditions.

2.1.8 Switching Characteristics

The switching characteristics section of the data sheet (see Figure 2.1-8) includes those parameters that specify how fast the outputs will respond to signal changes at the inputs under specified conditions of supply voltage, temperature, and load.

2.1.8.1 Maximum Clock Frequency, f_{max}

This parameter is the upper limit of the f_{clock} specification. With input conditions that should cause logic level changes at the output, f_{max} is the highest rate at which the clock input of a bistable circuit can be driven through its required sequence and still maintain stable transitions of logic level at the output. The parameter f_{max} is specified in the data sheet as a minimum. The circuit is guaranteed to operate up to the minimum frequency specified.

See f_{clock} for additional f_{max} testing information. Due to test-machine capability limitations, it may be necessary to test f_{max} or minimum recommended operating conditions (i.e., pulse duration, setup time, hold time) in accordance with the following paragraph.

The f_{max} parameter may be tested in either of two ways. One method is to simultaneously test the response to the symmetrical clock-high and clock-low pulse durations that correspond to the reciprocal of the total period of

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} RANGE	T_A = 25°C			54AC11244		74AC11244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3.3 ±0.3 V	1.5	7.1	9.3	1.5	10.8	1.5	10.2	ns
			5 ±0.5 V	1.5	4.9	6.7	1.5	7.7	1.5	7.3	
t_{PHL}			3.3 ±0.3 V	1.5	6.3	8.6	1.5	10.5	1.5	9.5	
			5 ±0.5 V	1.5	4.5	6.4	1.5	7.4	1.5	6.9	
t_{PZH}	$\overline{G}$	Y	3.3 ±0.3 V	1.5	8	10.7	1.5	12.9	1.5	11.8	ns
			5 ±0.5 V	1.5	5.4	7.7	1.5	9.3	1.5	8.5	
t_{PZL}			3.3 ±0.3 V	1.5	7.9	10.6	1.5	12.9	1.5	11.9	
			5 ±0.5 V	1.5	5.4	7.6	1.5	9.1	1.5	8.5	
t_{PHZ}	$\overline{G}$	Y	3.3 ±0.3 V	1.5	5.9	7.9	1.5	8.7	1.5	8.3	ns
			5 ±0.5 V	1.5	5.2	7	1.5	7.6	1.5	7.3	
t_{PLZ}			3.3 ±0.3 V	1.5	7.2	9.4	1.5	10.4	1.5	9.9	
			5 ±0.5 V	1.5	5.8	7.8	1.5	8.6	1.5	8.2	

switching characteristics, V_{CC} = 5 V ± 0.5 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54ACT11074		74ACT11074		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	125		100		100		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	1.5	5.7	8.9	1.5	10.1	1.5	9.6	ns
t_{PHL}			1.5	6.6	11.3	1.5	13.3	1.5	12.5	
t_{PLH}	CLK	Q or $\overline{Q}$	1.5	6	8.5	1.5	10	1.5	9.4	ns
t_{PHL}			1.5	5.7	8	1.5	9.4	1.5	8.8	

Figure 2.1-8. Switching Characteristics Table

the specified minimum value of f_{max}. The second method is to individually test the response to the minimum clock-high and clock-low pulse durations under specified load conditions. A pulse generator is used to propagate a signal through the device to verify device operation with the minimum pulse duration. When clock-high and clock-low pulse durations are equal to or less than the corresponding f_{max} pulse duration, f_{max} testing will suffice for the testing of clock-high and clock-low pulse durations.

2.1.8.2 Propagation Delay Time, High-to-Low-Level Output, t_{PHL}

Propagation delay time t_{PHL} is tested by generating a transition on the specified input that will cause the designated output to switch from a high logic level to a low logic level.

The transition applied is 0 V to V_{CC} or V_{CC} to 0 V for AC devices and 0 V to 3 V or 3 V to V_{CC} for ACT devices. Trip points used for the timing measurements are shown in Figure 2.1-7. Output loads used during testing are defined in the individual data sheets. Propagation delay time t_{PHL} is not checked simultaneously with other outputs or with other recommended operating conditions.

The time between the specified reference point on the input voltage waveform and the specified reference point on the output voltage waveform is measured.

2.1.8.3 Propagation Delay Time, Low-to-High-Level Output, t_{PLH}

Propagation delay time t_{PLH} is tested by generating a transition on the specified input that will cause the designated output to switch from a low logic level to a high logic level.

The transition applied is 0 V to V_{CC} or V_{CC} to 0 V for AC devices and 0 V to 3 V or 3 V to 0 for ACT devices. Trip points used for the timing measurements are shown in Figure 2.1-7. Output loads used during testing are defined in the individual data sheets. Propagation delay time t_{PLH} is not checked simultaneously with other outputs or with other recommended operating conditions.

The time between the specified reference point on the input voltage waveform and the specified reference point on the output voltage waveform is measured.

2.1.8.4 Output Enable Time (of a Three-State Output) to High Level, t_{PZH}

This parameter is the propagation delay time between the specified reference point on the input voltage waveform and the specified reference point on the output voltage waveform with the three-state output changing from a high-impedance (off) state to the defined high level.

Output enable time t_{PZH} is tested by generating a transition on the specified input that will cause the designated output to switch from a high-impedance state to a high logic level. Trip points used for the timing measurements are shown in Figure 2.1-9. Output loads used during testing are defined in the individual data sheets. Output enable time t_{PZH} is not checked simultaneously with other outputs or with other recommended operating conditions.

Outputs not being tested should be set to minimize switching currents.

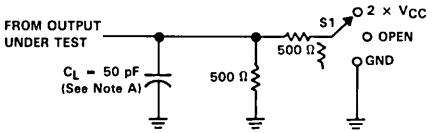
2.1.8.5 Output Enable Time (of a Three-State Output) to Low Level, t_{PZL}

This parameter is the propagation delay time between the specified reference point on the input voltage waveform and the specified reference point on the output voltage waveform with the three-state output changing from a high-impedance (off) state to the defined low level.

Output enable time t_{PZL} is tested by generating a transition on the specified input that will cause the designated output to switch from a high-impedance state to a low logic level. Trip points used for the timing measurements are shown in Figure 2.1-9. Output loads used during testing are defined in the individual data sheets. Output enable time t_{PZL} is not checked simultaneously with other outputs or with other recommended operating conditions.

Outputs not being tested should be set to minimize switching currents.

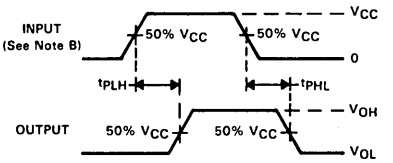
PARAMETER MEASUREMENT INFORMATION



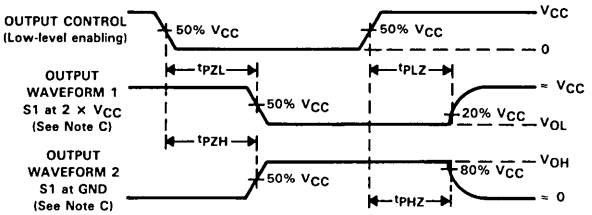
TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

AC11244

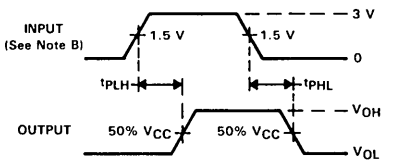


PROPAGATION DELAY TIMES

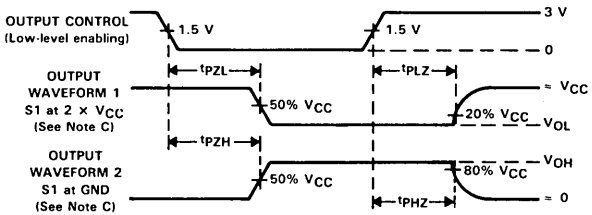


ENABLE AND DISABLE TIMES

ACT11244



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 2.1-9. Load Circuit and Voltage Waveforms

2.1.8.6 Output Disable Time (of a Three-State Output) from High Level, t_{PHZ}

This parameter is the propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

Output disable time t_{PHZ} is tested by generating a transition on the specified input that will cause the designated output to switch from a high logic level to the high-impedance state. The transition applied is 0 V to V_{CC} or V_{CC} to 0 V for AC devices and 0 V to 3 V or 3 V to 0 V for ACT devices. Trip points used for the timing measurements are shown in Figure 2.1-9. Output loads used during testing are defined in the individual data sheets. Output disable time, t_{PHZ}, is not checked simultaneously with other outputs or with other recommended operating conditions.

Outputs not being tested should be set to minimize switching currents.

2.1.8.7 Output Disable Time (of a Three-State Output) from Low Level, t_{PLZ}

This parameter is the propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

Output disable time t_{PLZ} is tested by generating a transition on the specified input that will cause the designated output to switch from a low logic level to high-impedance state. The transition applied is 0 V to V_{CC} or V_{CC} to 0 V for AC devices and 0 V to 3 V or 3 V to 0 V for ACT devices. Trip points used for the timing measurements are shown in Figure 2.1-9. Output loads used during testing are defined in the individual data sheets. Output disable time t_{PLZ} is not checked simultaneously with other outputs or with other recommended operating conditions. Outputs not being tested should be set to minimize switching currents.

2.1.9 Functional Testing

Functional testing is performed on logic devices by execution of a set of functional patterns located in the test program. These patterns are intended to guarantee operation and/or conformance to the function table, although, on some devices, not all possible combinations or sequential modes are tested. They are designed to simulate the operation of the device in an actual system.

The functional patterns are applied using transitions from 0 V to V_{CC} for AC devices and 0 V to 3 V for ACT devices. Pattern execution is typically at 10 MHz but may be higher on more complex devices utilizing larger pattern sets. The functional patterns are typically performed three times using V_{CC} = 4.5 V and V_{CC} = 5.5 V. The patterns are typically performed with trip points set at a value 200 mV less than V_{OH} min and a value 200 mV

greater than V_{OL} max, respectively. Additional functional testing with V_{CC} = 3 V is performed for AC devices only. The outputs are not fully loaded during the test with either I_{OL} max or I_{OH} max.

Problems are frequently created in functional testing when V_{IH} min and V_{IL} max are used as the input conditions to exercise the function table. V_{IH} min and V_{IL} max are input conditions that are used in parameter testing. The problems occur because of the noise that is present on the test heads of automated test equipment with long cables. Parameter tests (e.g., V_{OH}, V_{OL}, I_{OZH}, and I_{OZL}) are done at a relatively slow repetition rate. Any noise that is present on the test head will have settled out before the outputs are measured; however, during functional testing, the outputs are sensed before the ringing on the inputs has settled out and reached its final and correct state.

The use of V_{IH} = V_{CC} and V_{IL} = 0 V for AC devices and V_{IH} = 3 V and V_{IL} = 0 V for ACT devices during functional testing does not imply that devices are noise sensitive. The environment the devices see on a system printed circuit board is much less severe than noisy production test equipment.

2.1.10 Summary

The information in this section is provided so that the designer can derive the maximum amount of information about EPIC™ ACL devices from the device data sheets. Texas Instruments provides this information to ease the task of the designer in incorporating ACL products into new system designs. If there are questions or comments regarding the information presented, contact your local TI representative, call the TI ACL application group at (214) 868-7682, or address inquiries to:

Texas Instruments Incorporated
CMOS and Bipolar Marketing
Mail Station 8323
P.O. Box 655303
Dallas, TX 75265

2.2 ACL Mechanical Design Considerations†

2.2.1 EPIC™ ACL Commercial Options

For commercial use, TI EPIC™ ACL is being offered in traditional through-hole plastic dual-in-line package (P-DIP) and new surface-mount small-outline integrated circuit (SOIC) package options. Table 1 lists all EPIC™ ACL package options along with their appropriate mold compounds and lead-frame compositions. For commercial applications, only plastic packaging materials are used. All package options are characterized for operation from 40°C to 85°C.

Figure 2.2-1 presents profiles of both the P-DIP and SOIC technologies. The P-DIP through-hole and SOIC surface-mount have leads on two of the four package sides. The SOIC package leads extend out from the body with two right-angle bends. This profile resembles a sea gull in flight. From this profile, the name "gull wing" has been adopted for the package leads.

Table 2-1. EPIC™ ACL Commercial Package Options

PKG.	DESG.	REF.	TERMINAL COUNT	WIDTH		MOLD COMPOUND	LEAD FRAME
				mm	(mils)		
SOIC	D	2.2.3	14	3,81	(150)	PLASKON 7090	OLIN-C151‡
SOIC	D	2.2.3	16	3,81	(150)	PLASKON 7090	OLIN-C151‡
SOIC	DW	2.2.4	20	7,62	(300)	PLASKON 7090	OLIN-C151‡
SOIC	DW	2.2.4	24	7,62	(300)	PLASKON 7090	OLIN-C151‡
SOIC	DW	2.2.4	28	7,62	(300)	PLASKON 7090	OLIN-C151‡
P-DIP	N	2.2.5	14	7,62	(300)	PLASKON 7060	OLIN-C195
P-DIP	N	2.2.6	16	7,62	(300)	PLASKON 7060	OLIN-C195
P-DIP	N	2.2.7	20	7,62	(300)	PLASKON 7060	OLIN-C195
P-DIP	NT	2.2.8	24	7,62	(300)	PLASKON 7060	OLIN-C195
P-DIP	NT	2.2.8	28	7,62	(300)	PLASKON 7060	OLIN-C195

‡OLIN-C155 and TAMAC-4(KFC) are qualified for use with OLIN-C151 for EPIC™ ACL SOIC options.

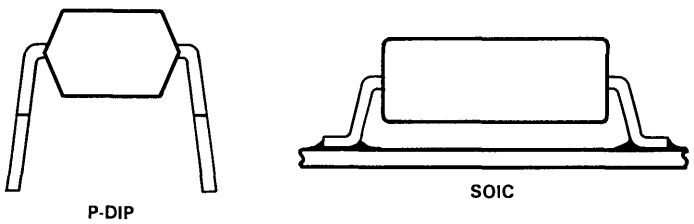


Figure 2.2-1. Profiles of P-DIP Through-Hole and SOIC Surface Mount Package Technologies

†Written by S. Perna

2.2.2 EPIC™ ACL Military Options

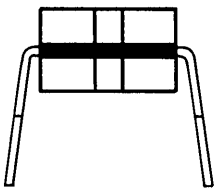
For military use, TI EPIC™ ACL is being offered in through-hole ceramic dual-in-line packages (C-DIP) and leadless ceramic chip carriers (LCCC). Table 2-2 lists all EPIC™ ACL package options along with their appropriate ceramic materials and lead-frame compositions. At the present time, there are plans to provide a 28-pin ceramic DIP for EPIC™ ACL. All military package options are characterized for operation from −55°C to 125°C.

Figure 2-.2-2 provides profiles of both the C-DIP and LCCC technologies. The LCCC has terminals on all four sides of the package instead of the usual leads. The 20-terminal package option is used for all EPIC™ ACL devices also housed in 14-, 16-, or 20-pin DIPs. The 28-terminal package option is used for all EPIC™ ACL devices also housed in 24- or 28-pin DIPs.

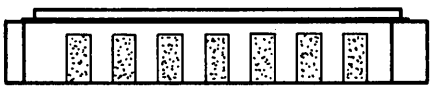
Table 2-2. EPIC™ ACL Military Package Options

PKG.	DESG.	REF.	TERMINAL COUNT	WIDTH		CERAMIC MATERIAL	LEAD FRAME
				mm	(mils)		
LCCC	FK	2.2.9	20†	8,89	(350)	Al_2O_3BLACK: 90-94%	–
LCCC	FK	2.2.9	28‡	11.43	(450)	Al_2O_3BLACK: 90-94%	–
C-DIP	J	2.2.10	14	7,62	(300)	Al_2O_3BLACK: 90-98%	ALLOY 42
C-DIP	J	2.2.11	16	7,62	(300)	Al_2O_3BLACK: 90-98%	ALLOY 42
C-DIP	J	2.2.12	20	7,62	(300)	Al_2O_3BLACK: 90-98%	ALLOY 42
C-DIP	JT	2.2.13	24	7,62	(300)	Al_2O_3BLACK: 90-98%	ALLOY 42
C-DIP	JD		28§	7,62	(300)	Al_2O_3BLACK: 90-98%	ALLOY 42

† LCCC 20-terminal package, used for all devices that fit in 14-, 16-, and 20-pin DIPs.
‡ LCCC 28-terminal package, used for all devices that fit in 24- and 28-pin DIPs.
§ This package option is in the design stage.



C-DIP



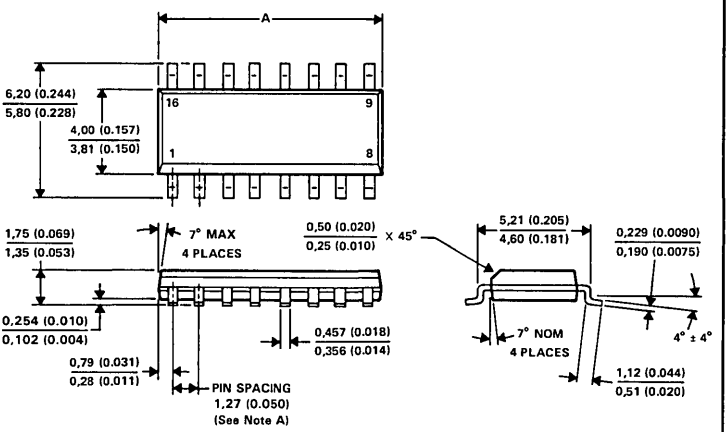
LCCC (28 TERMINAL)

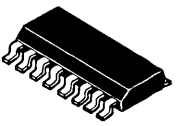
Figure 2.2-2. Profiles of C-DIP Through-Hole and LCCC Surface Mount Package Technologies

2.2.3 D014 and D016 Plastic "Small Outline" Packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D014
D016
(16-pin package used for illustration)





DESIGNATION / PINS / DIM	D008	D014	D016
	8	14	16
A MIN	4,80 (0.189)	8,55 (0.337)	9,80 (0.386)
A MAX	5,00 (0.197)	8,74 (0.344)	10,00 (0.394)

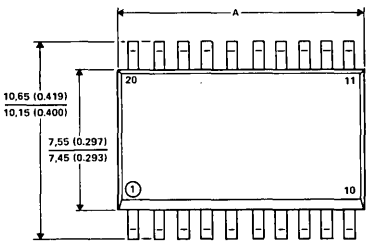
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

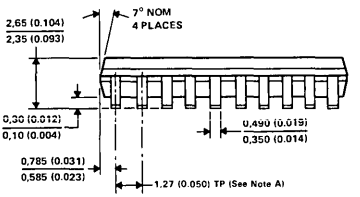
NOTES: A. Leads are within 0,25 mm (0.010 inch) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 mm (0.006 inch).
D. Lead tips to be planar within 0,051 mm (0.002 inch) exclusive of solder.

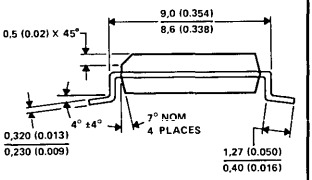
2.2.4 DW020, DW024, and DW028 Plastic "Small Outline" Packages

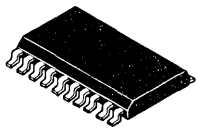
Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DW020
DW024
DW028
(20-pin package used for illustration)









DESIGNATION / PINS / DIM	DW016	DW020	DW024	DW028
	16	20	24	28†
A MIN	10,16 (0,400)	12,70 (0.500)	15,29 (0.602)	
A MAX	10,36 (0.408)	12,90 (0.508)	15,49 (0.610)	17,88 (0.707)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

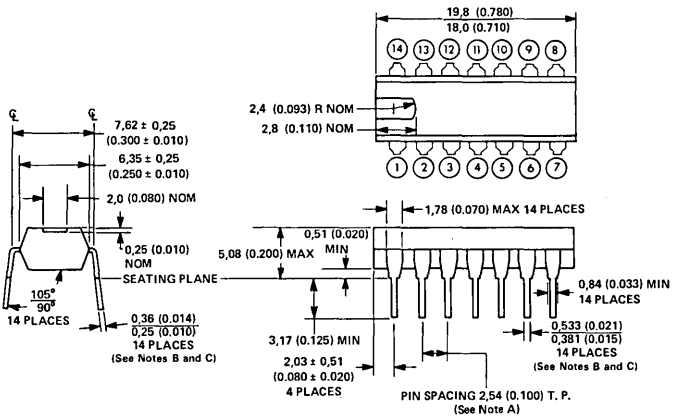
† The 28-pin package drawing is presently classified as Advance Information.

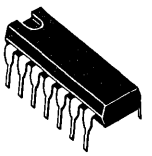
NOTES: A. Leads are within 0,25 mm (0.010 inch) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 mm (0.006 inch).
D. Lead tips to be planar within ±0,051 (0.002).

2.2.5 N014 Plastic Dual-In-Line Package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N014





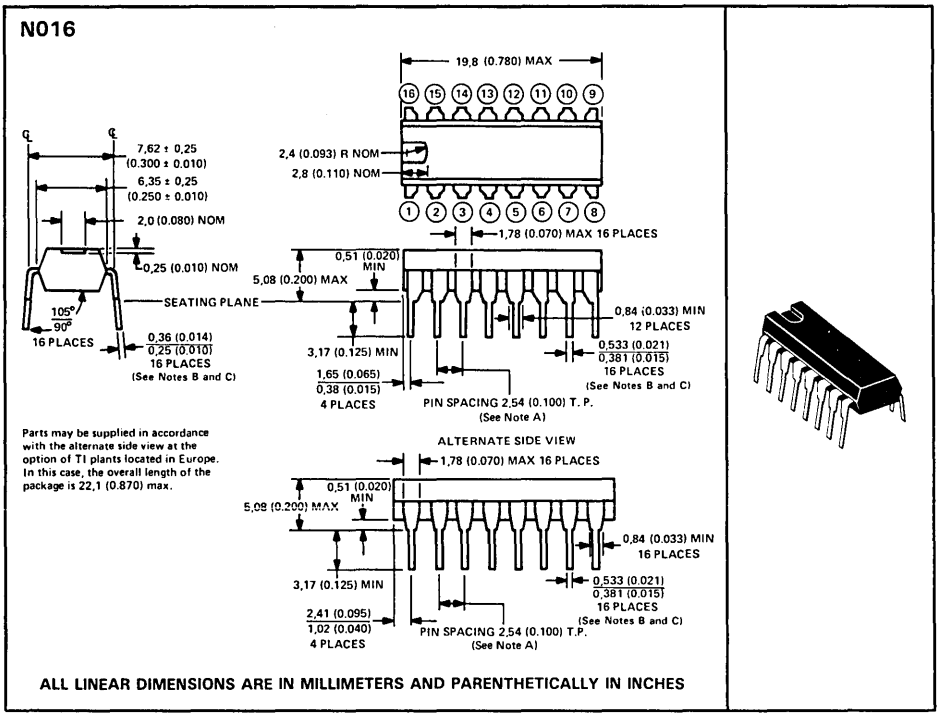
Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

2.2.6 N016 Plastic Dual-In-Line Package

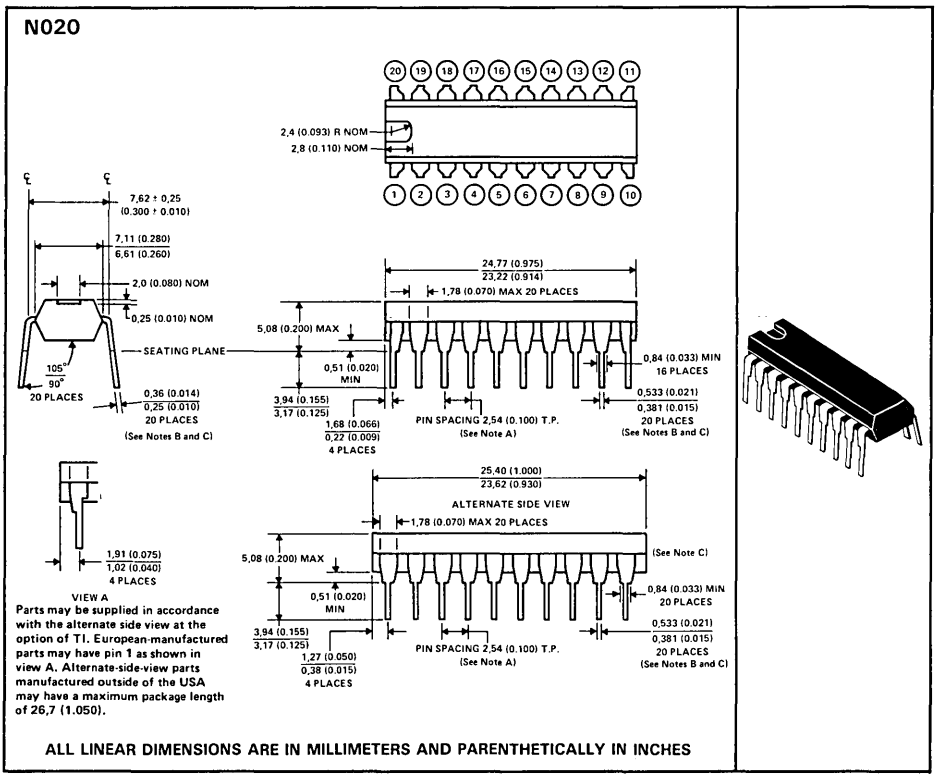
This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

2.2.7 N020 Plastic Dual-In-Line Package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Each pin centerline is located within 0,25 mm (0.010 inch) of its true longitudinal position.

B. This dimension does not apply for solder-dipped leads.

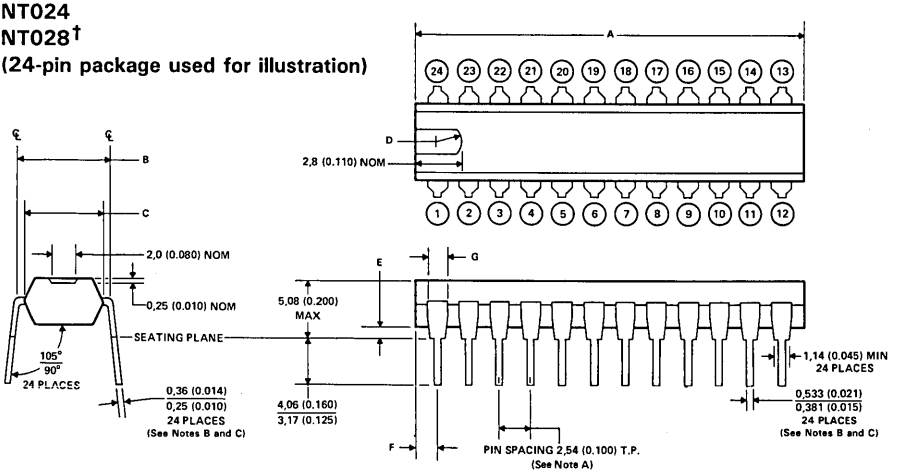
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

2.2.8 NT024 and NT028† Plastic DuaL-In-Line Packages

Each of these packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin and 28-pin packages, the letter N is used by itself since the 24-pin and 28-pin packages may be available in more than one row-spacing. For the 24-pin and 28-pin packages, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

NT024
NT028†
(24-pin package used for illustration)



DIM / DESIGNATION	A		B	C	D	E	F		G	
	MIN	MAX		MAX	R NOM	MIN	MIN	MAX	MIN	MAX
NT024	28,6 (1.125)	31,8 (1.250)	7,62 ± 0,25 (0.300 ± 0.010)	7,1 (0.280)	2,4 (0.093)	0.38 (0.015)	0,71 (0.028)	2,16 (0.085)	1,14 (0.045)	1,78 (0.070)
NT028†	34,0 (1.338)	37,1 (1.462)	7,88 ± 0,25 (0.310 ± 0.010)	6,86 (0.270)	1,02 (0.040)	0,51 (0.020)	0,51 (0.020)	2,03 (0.080)	1,02 (0.040)	1,78 (0.070)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† The 28-pin package drawing is presently classified as Advance Information.

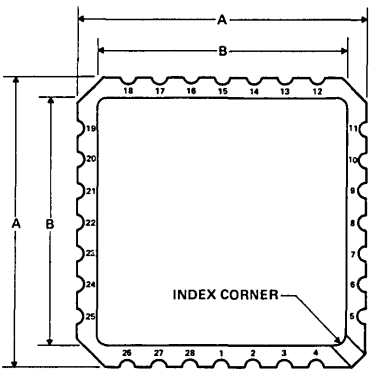
NOTES: A. Each pin centerline is located within 0.25 mm (0.010 inch) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

2.2.9 FK020 and FK028 Ceramic Chip Carrier Packages

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.

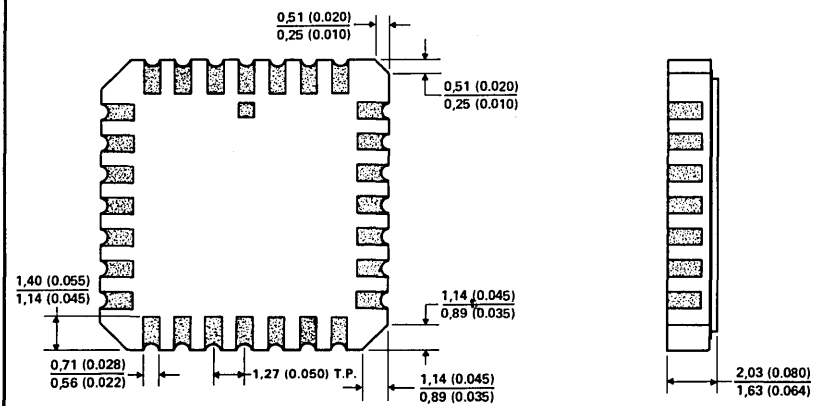
FK020
FK028
(28-terminal package shown)



CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS004CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)

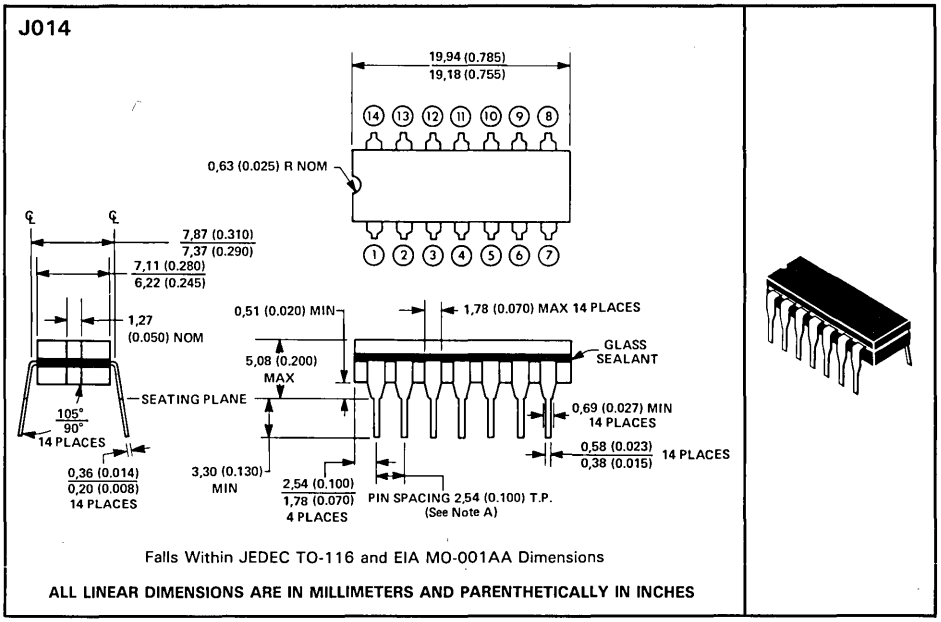
*All dimensions and notes for the specified JEDEC outline apply.



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

2.2.10 J014 Ceramic Dual-In-Line Package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

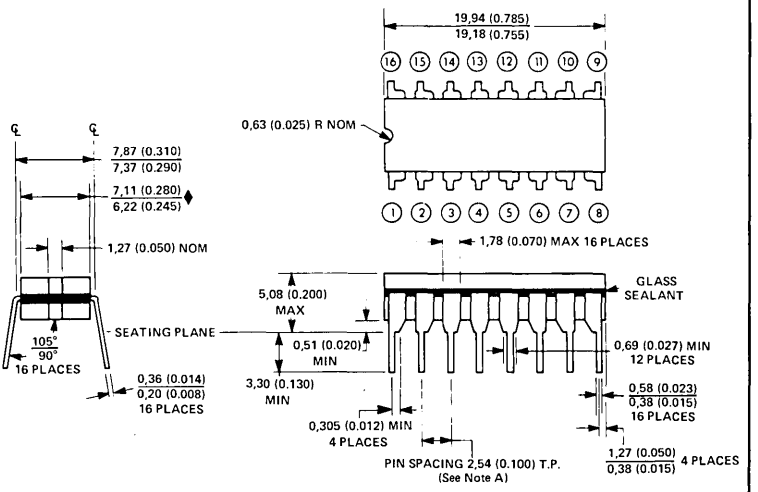


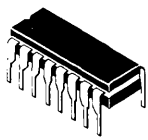
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

2.2.11 J016 Ceramic Dual-In-Line Package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

J016





♦ For memories of 64 bits and up, a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, and complex HCMOS parts, this maximum is 7,62 (0.300). All other dimensions apply without modification.

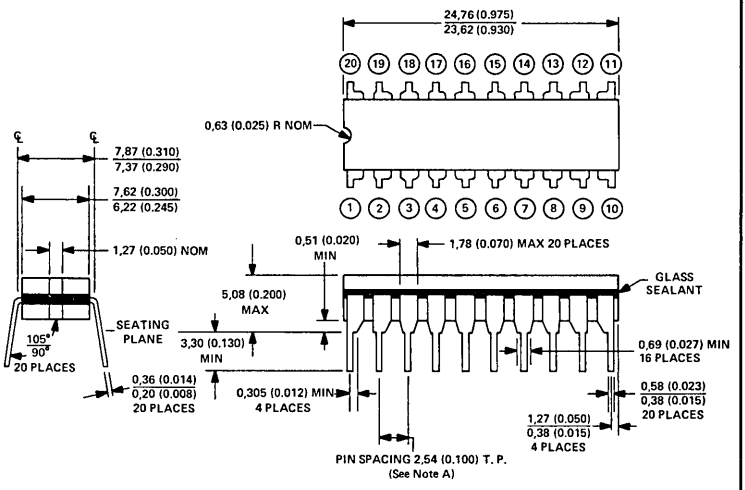
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

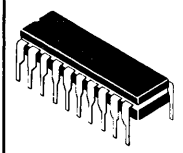
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

2.2.12 J020 Ceramic Dual-In-Line Package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

J020





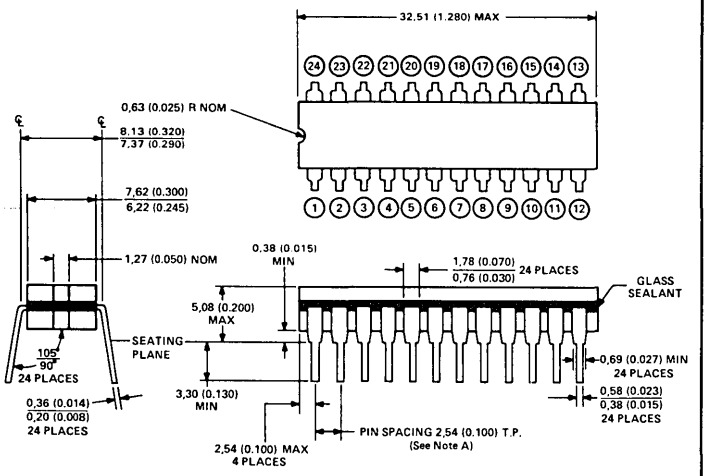
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

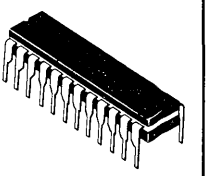
NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

2.2.13 JT024 Ceramic Dual-In-Line Package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the pins are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-diped'') pins require no additional cleaning or processing when used in soldered assembly.

JT024





ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

2.3 Explanation of Logic Symbols†

2.3.1 Introduction

The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be explained in section 2.3.4.

The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

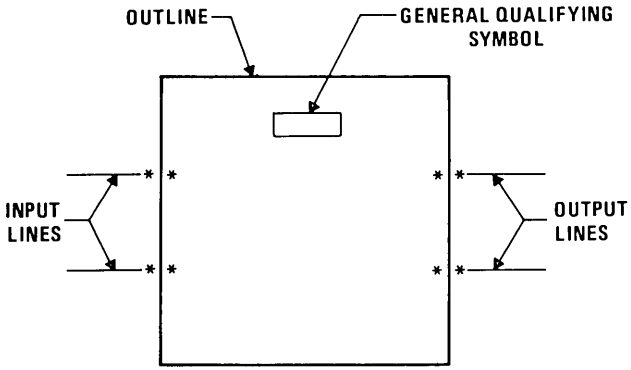
Internationally, IEC Technical Committee TC-3 has approved a new document (Publication 617-12) that consolidates the original work started in the mid 1960s and published in 1972 (Publication 117-15) and the amendments and supplements that have followed. Similarly for the USA, IEEE Committee SCC 11.9 has revised the publication IEEE Std 91/ANSI Y32.14. Now numbered simply IEEE Std 91-1984, the IEEE standard contains all of the IEC work that has been approved, and also a small amount of material still under international consideration. Texas Instruments is participating in the work of both organizations, and this document introduces new logic symbols in accordance with the new standards. When changes are made as the standards develop, future editions will take those changes into account.

The following explanation of the new symbolic language is necessarily brief and greatly condensed from what the standards publications now contain. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in various data books and the comparison of the symbols with logic diagrams, functional block diagrams, and/or function tables to further help that understanding.

2.3.2 Symbol Compositioin

A symbol comprises an outline or a combination of outlines together with one or more qualifying symbols. The shape of the symbol is not significant. As shown in Figure 2.3-1, general qualifying symbols are used to tell exactly what logical operation is performed by the elements. Table 2.3-1 shows general qualifying symbols defined in the new standards. Input lines are placed on the left and output lines are placed on the right. When an exception is made to that convention, the direction of signal flow is indicated by an arrow as shown in Figure 2.3-11.

† Written by F. A. Mann.



*Possible positions for qualifying symbols relating to inputs and outputs

Figure 2.3-1. Symbol Composition

All outputs of a single, unsubdivided element always have identical internal logic states determined by the function of the element except when otherwise indicated by an associated qualifying symbol or label inside the element.

The outlines of elements may be abutted or embedded in which case the following conventions apply. There is no logic connection between the elements when the line common to their outlines is in the direction of signal flow. There is at least one logic connection between the elements when the line common to their outlines is perpendicular to the direction of signal flow. The number of logic connections between elements will be clarified by the use of qualifying symbols, and this is discussed further under that topic. If no indications are shown on either side of the common line, it is assumed there is only one connection.

When a circuit has one or more inputs that are common to more than one element of the circuit, the common-control block may be used. This is the only distinctively shaped outline used in the IEC system. Figure 2.3-2 shows that, unless otherwise qualified by dependency notation, an input to the common-control block is an input to each of the elements below the common-control block.

A common output depending on all elements of the array can be shown as the output of a common-output element. Its distinctive visual feature is the double line at its top. In addition, the common-output element may have other inputs as shown in Figure 2.3-3. The function of the common-output element must be shown by use of a general qualifying symbol.

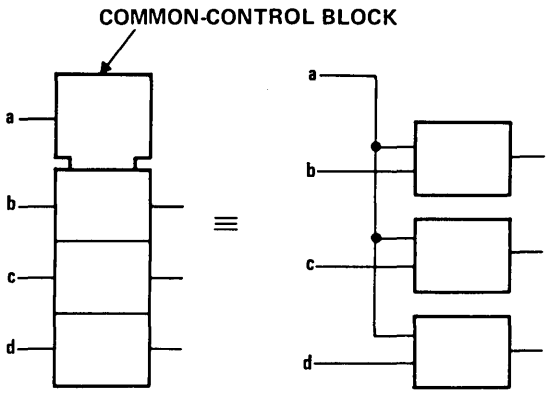


Figure 2.3-2. Common-Control Block

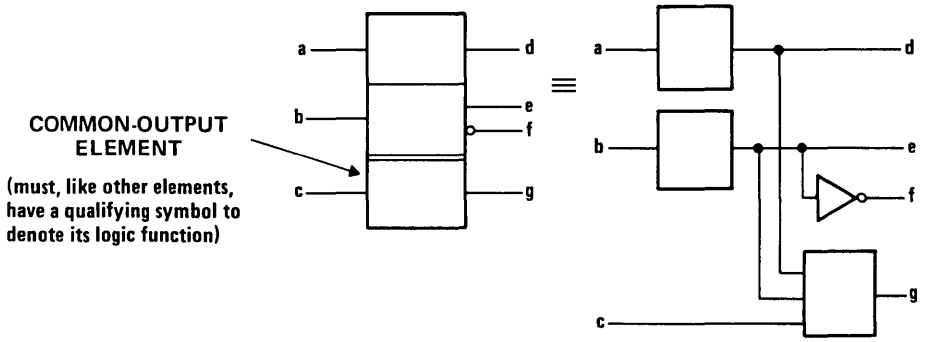


Figure 2.3-3. Common-Output Element

2.3.3 Qualifying Symbols

2.3.3.1 General Qualifying Symbols

Table 2.3-1 shows general qualifying symbols defined by IEEE Standard 91. These characters are placed near the top center or the geometric center of a symbol or symbol element to define the basic function of the device represented by the symbol or of the element.

Table 2.3-1. General Qualifying Symbols

SYMBOL	DESCRIPTION	CMOS EXAMPLE	TTL EXAMPLE
&	AND gate or function.	'HC00	SN7400
≥1	OR gate or function. The symbol was chosen to indicate that at least one active input is needed to activate the output.	'HC02	SN7402
=1	Exclusive OR. One and only one input must be active to activate the output.	'HC86	SN7486
=	Logic identity. All inputs must stand at the same state.	'HC86	SN74180
2k	An even number of inputs must be active.	'HC280	SN74180
2k + 1	An odd number of inputs must be active.	'HC86	SN74ALS86
1	The one input must be active.	'HC04	SN7404
▷ or ◁	A buffer or element with more than usual output capability (symbol is oriented in the direction of signal flow).	'HC240	SN74S436
⊓	Schmitt trigger; element with hysteresis.	'HC132	SN74LS18
X/Y	Coder, code converter (DEC/BCD, BIN/OCT, BIN/7-SEG, etc.).	'HC42	SN74LS347
MUX	Multiplexer/data selector.	'HC151	SN74150
DMUX or DX	Demultiplexer.	'HC138	SN74138
Σ	Adder.	'HC283	SN74LS385
P−Q	Subtracter.	*	SN74LS385
CPG	Look-ahead carry generator.	'HC182	SN74182
π	Multiplier.	*	SN74LS384
COMP	Magnitude comparator.	'HC85	SN74LS682
ALU	Arithmetic logic unit.	'HC181	SN74LS381
⌐⌐	Retriggerable monostable.	'HC123	SN74LS422
1⌐⌐	Nonretriggerable monostable (one-shot).	'HC221	SN74121
G ⌐⌐	Astable element. Showing waveform is optional.	*	SN74LS320
!G ⌐⌐	Synchronously starting astable.	*	SN74LS624
G! ⌐⌐	Astable element that stops with a completed pulse.	*	*
SRGm	Shift register. m = number of bits.	'HC164	SN74LS595
CTRm	Counter. m = number of bits; cycle length = 2^m.	'HC590	SN54LS590
CTR DIVm	Counter with cycle length = m.	'HC160	SN74LS668
RCTRm	Asynchronous (ripple-carry) counter; cycle length = 2^m.	'HC4020	*

*Not all of the general qualifying symbols have been used in TI's CMOS and TTL data books, but they are included here for the sake of completeness.

Table 2.3-1. General Qualifying Symbols (Continued)

SYMBOL	DESCRIPTION	CMOS EXAMPLE	TTL EXAMPLE
ROM	Read-only memory.	*	SN74187
RAM	Random-access read/write memory.	'HC189	SN74170
FIFO	First-in, first-out memory.	*	SN74LS222
I=0	Element powers up cleared to 0 state.	*	SN74AS877
I=1	Element powers up set to 1 state.	'HC7022	SN74AS877
Φ	Highly complex function; "gray box" symbol with limited detail shown under special rules.	*	SM74LS608

*Not all of the general qualifying symbols have been used in TI's CMOS and TTL data books, but they are included here for the sake of completeness.

2.3.3.2 General Qualifying Symbols for Inputs and Outputs

Qualifying symbols for inputs and outputs are shown in Table 2.3-2, and many will be familiar to most users, a likely exception being the logic polarity symbol for directly indicating active-low inputs and outputs. The older logic negation indicator means that the external 0 state produces the internal 1 state. The internal 1 state means the active state. Logic negation may be used in pure logic diagrams; in order to tie the external 1 and 0 logic states to the levels H (high) and L (low), a statement of whether positive logic (1 = H, 0 = L) or negative logic (1 = L, 0 = H) is being used is required or must be assumed. Logic polarity indicators eliminate the need for calling out the logic convention and are used in various data books in the symbology for actual devices. The presence of the triangular polarity indicator indicates that the L logic level will produce the internal 1 state (the active state) or that, in the case of an output, the internal 1 state will produce the external L level. Note how the active direction of transition for a dynamic input is indicated in positive logic, negative logic, and with polarity indication.

The internal connections between logic elements abutted together in a symbol may be indicated by the symbols shown in Table 2.3-2. Each logic connection may be shown by the presence of qualifying symbols at one or both sides of the common line, and, if confusion can arise about the number of connections, use can be made of one of the internal connection symbols.

The internal (virtual) input is an input originating somewhere else in the circuit and is not connected directly to a terminal. The internal (virtual) output is likewise not connected directly to a terminal. The application of internal inputs and outputs requires an understanding of dependency notation, which is explained in section 2.3.4.

Table 2.3-2. Qualifying Symbols for Inputs and Outputs

Logic negation at input. External 0 produces internal 1.

Logic negation at output. Internal 1 produces external 0.

Active-low input. Equivalent to  in positive logic.

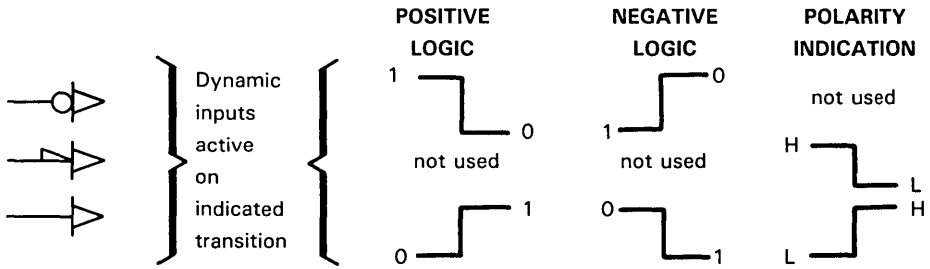
Active-low output. Equivalent to  in positive logic.

Active-low input in the case of right-to-left signal flow.

Active-low output in the case of right-to-left signal flow.

Signal flow from right to left. If not otherwise indicated, signal flow is from left to right.

Bidirectional signal flow.



Nonlogic connection. A label inside the symbol will usually define the nature of this pin.

Input for analog signals (on a digital symbol) (see Figure 2.3-14).

Input for digital signals (on an analog symbol) (see Figure 2.3-14).

Internal connection. 1 state on left produces 1 state on right.

Negated internal connection. 1 state on left produces 0 state on right.

Dynamic internal connection. Transition from 0 to 1 on left produces transitory 1 state on right.

Internal input (virtual input). It always stands at its internal 1 state unless affected by an overriding dependency relationship.

Internal output (virtual output). Its effect on an internal input to which it is connected is indicated by dependency notation.

In an array of elements, if the same general qualifying symbol and the same qualifying symbols associated with inputs and outputs would appear inside each of the elements of the array, then these qualifying symbols are usually shown only in the first element. This is done to reduce clutter and to save time in recognition. Similarly, large identical elements that are subdivided into smaller elements may each be represented by an unsubdivided outline. The SN54HC242 or SN54LS440 symbol illustrates this principle.

2.3.3.3 Symbols Inside the Outline

Table 2.3-3 shows some symbols used inside the outline. Note particularly that open-collector (open-drain), open-emitter (open-source), and 3-state outputs have distinctive symbols. An EN input affects all the external outputs of the element in which it is placed, plus the external outputs of any elements shown to be influenced by that element. It has no effect on inputs. When an enable input affects only certain outputs, affects outputs located outside the indicated influence of the element in which the enable input is placed, and/or affects one or more inputs, a form of dependency notation will indicate this (see 2.3.4.10). The effects of the EN input on the various types of outputs are shown.

It is particularly important to note that a D input is always the data input of a storage element. At its internal 1 state, the D input sets the storage element to its 1 state, and at its internal 0 state, it resets the storage element to its 0 state.

The binary grouping symbol will be explained more fully in section 2.3.8. Binary-weighted inputs are arranged in order, and the binary weights of the least significant and the most significant lines are indicated by numbers. In this document, weights of input and output lines will usually be represented by powers of two only when the binary grouping symbol is used; otherwise, decimal numbers will be used. The grouped inputs generate an internal number on which a mathematical function can be performed or that can be an identifying number for dependency notation (Figure 2.3-31). A frequent use is in addresses for memories.

Reversed in direction, the binary grouping symbol can be used with outputs. The concept is analogous to that for the inputs, and the weighted outputs will indicate the internal number assumed to be developed within the circuit.

Other symbols are used inside the outlines in accordance with the IEC/IEEE standards but are not shown here. Generally, these are associated with arithmetic operations and are self-explanatory.

When nonstandardized information is shown inside an outline, it is usually enclosed in square brackets [like these]. The square brackets are omitted when associated with a nonlogic input, which is indicated by an X superimposed on the connection line outside the symbol.

Table 2.3-3. Symbols Inside the Outline

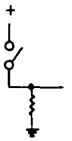
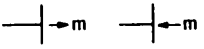
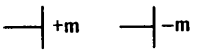
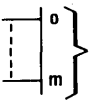
	Postponed output (of a pulse-triggered flip-flop). The output changes when input initiating change (e.g., a C input) returns to its initial external state or level. See paragraph 2.3.5.
	Bi-threshold input (input with hysteresis)
	N-P-N open-collector or similar output that can supply a relatively low-impedance L level when not turned off. Requires external pull-up. Capable of positive-logic wired-AND connection. 
	Passive-pull-up output is similar to N-P-N open-collector output but is supplemented with a built-in passive pull-up.
	N-P-N open-emitter or similar output that can supply a relatively low-impedance H level when not turned off. Requires external pull-down. Capable of positive-logic wired-OR connection. 
	Passive-pull-down output is similar to N-P-N open-emitter output but is supplemented with a built-in passive pull-down.
	Three-state output.
	Output with more than usual output capability (symbol is oriented in the direction of signal flow).
	Enable input When at its internal 1-state, all outputs are enabled. When at its internal 0-state, open-collector and open-emitter outputs are off, three-state outputs are in the high-impedance state, and all other outputs (i.e., totem-poles) are at the internal 0-state.
J, K, R, S	Usual meanings associated with flip-flops (e.g., R = reset to 0, S = reset to 1).
	Toggle input causes internal state of output to change to its complement.
	Data input to a storage element equivalent to: 
	Shift right (left) inputs, m = 1, 2, 3, etc. If m = 1, it is usually not shown.
	Counting up (down) inputs, m = 1, 2, 3, etc. If m = 1, it is usually not shown.
	Binary grouping. m is highest power of 2.

Table 2.3-3. Symbols Inside the Outline (Continued)

CT = 15	The contents-setting input, when active, causes the content of a register to take on the indicated value.
CT = 9	The content output is active if the content of the register is as indicated.
	Input line grouping . . . indicates two or more terminals used to implement a single logic input. e.g., The paired expander inputs of SN7450. 
"1"	Fixed-state output always stands at its internal 1 state. For example, see SN74185.

2.3.4 Dependency Notation

2.3.4.1 General Explanation

Dependency notation is the powerful tool that sets the IEC symbols apart from previous systems and makes compact, meaningful symbols possible. It provides the means of denoting the relationship between inputs, outputs, or inputs and outputs without actually showing all the elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function.

In the convention for the dependency notation, use will be made of the terms "affecting" and "affected." In cases where it is not evident which inputs must be considered as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the choice may be made in any convenient way.

So far, eleven types of dependency have been defined, and all of these are used in various TI data books. X dependency is used mainly with CMOS circuits. They are listed below in the order in which they are presented and are summarized in Table 2.3-4 following 2.3.4.12.

Section	Dependency Type or Other Subject
2.3.4.2	G, AND
2.3.4.3	General Rules for Dependency Notation
2.3.4.4	V, OR
2.3.4.5	N, Negate (Exclusive-OR)
2.3.4.6	Z, Interconnection
2.3.4.7	X, Transmission
2.3.4.8	C, Control
2.3.4.9	S, Set and R, Reset
2.3.4.10	EN, Enable
2.3.4.11	M, Mode
2.3.4.12	A, Address

2.3.4.2 G (AND) Dependency

A common relationship between two signals is to have them ANDed together. This has traditionally been shown by explicitly drawing an AND gate with the signals connected to the inputs of the gate. The 1972 IEC publication and the 1973 IEEE/ANSI standard showed several ways to show this AND relationship using dependency notation. While ten other forms of dependency have since been defined, the ways to invoke AND dependency are now reduced to one.

In Figure 2.3-4 input **b** is ANDed with input **a**, and the complement of **b** is ANDed with **c**. The letter G has been chosen to indicate AND relationships and is placed at input **b**, inside the symbol. A number considered appropriate by the symbol designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input **c**.

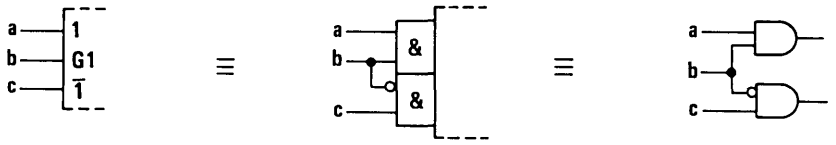


Figure 2.3-4. G Dependency Between Inputs

In Figure 2.3-5, output **b** affects input **a** with an AND relationship. The lower example shows that it is the internal logic state of **b**, unaffected by the negation sign, that is ANDed. Figure 2.3-6 shows input **a** to be ANDed with a dynamic input **b**.

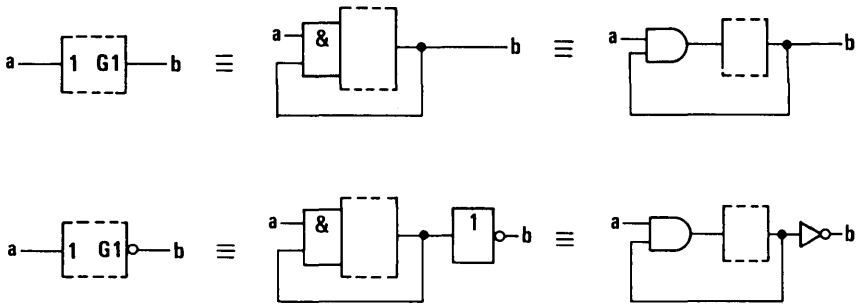


Figure 2.3-5. G Dependency Between Outputs and Inputs

Figure 2.3-6. G Dependency with a Dynamic Input

The rules for G dependency can be summarized thus:

> When a G*m* input or output (*m* is a number) stands at its internal 1 state, all inputs and outputs affected by G*m* stand at their normally defined internal logic states. When the G*m* input or output stands at its 0 state, all inputs and outputs affected by G*m* stand at their internal 0 states.

2.3.4.3 Conventions for the Application of Dependency Notation in General

The rules for applying dependency relationships in general follow the same pattern as was illustrated for G dependency.

Application of dependency notation is accomplished by:

1) labeling the input (or output) *affecting* other inputs or outputs with the letter symbol indicating the relationship involved (e.g., G for AND) followed by an identifying number, appropriately chosen, and
2) labeling each input or output *affected* by that affecting input (or output) with that same number.

If it is the complement of the internal logic state of the affecting input or output that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs (Figure 2.3-4).

If two affecting inputs or outputs have the same letter and the same identifying number, they stand in an OR relationship to each other (Figure 2.3-7).

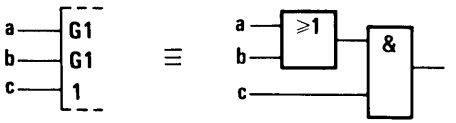


Figure 2.3-7. ORed Affecting Inputs

If the affected input or output requires a label to denote its function (e.g., "D"), this label will be *prefixed* by the identifying number of the affecting input (Figure 2.3-15).

If an input or output is affected by more than one affecting input, the identifying numbers of each of the affecting inputs will appear in the label

of the affected one, separated by commas. The normal reading order of these numbers is the same as the sequence of the affecting relationships (Figure 2.3-15).

If the labels denoting the functions of affected inputs or outputs must be numbers (e.g., outputs of a coder), the identifying numbers to be associated with both affecting inputs and affected inputs or outputs may be replaced by another character selected to avoid ambiguity, e.g., Greek letters (Figure 2.3-8).

Figure 2.3-8. Substitution for Numbers

2.3.4.4 V (OR) Dependency

The symbol denoting OR dependency is the letter V (Figure 2.3-9).

When a V*m* input or output stands at its internal 1 state, all inputs and outputs affected by V*m* stand at their internal 1 states. When the V*m* input or output stands at its internal 0 state, all inputs and outputs affected by V*m* stand at their normally defined internal logic states.

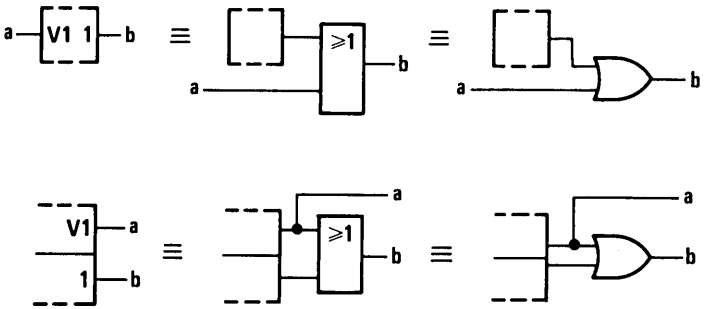


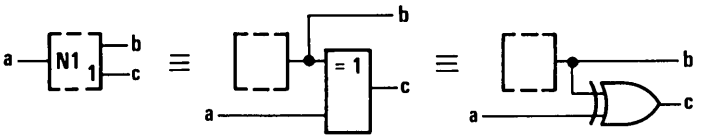
Figure 2.3-9. V (OR) Dependency

2.3.4.5 N (Negate) (Exclusive-OR) Dependency

The symbol denoting negate dependency is the letter N (Figure 2.3-10). Each input or output affected by an N*m* input or output stands in an Exclusive-OR relationship with the N*m* input or output.

When an N*m* input or output stands at its internal 1 state, the internal logic state of each input and each output affected by N*m* is the complement of

what it would otherwise be. When an N*m* input or output stands at its internal 0 state, all inputs and outputs affected by N*m* stand at their normally defined internal logic states.



If a = 0, then c = b
If a = 1, then c = $\bar{b}$

Figure 2.3-10. N (Negate) (Exclusive-OR) Dependency

2.3.4.6 Z (Interconnection) Dependency

The symbol denoting interconnection dependency is the letter Z.

Interconnection dependency is used to indicate the existence of internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

The internal logic state of an input or output affected by a Z*m* input or output will be the same as the internal logic state of the Z*m* input or output, unless modified by additional dependency notation (Figure 2.3-11).

2.3.4.7 X (Transmission) Dependency

The symbol denoting transmission dependency is the letter X.

Transmission dependency is used to indicate controlled bidirectional connections between affected input/output ports (Figure 2.3-12).

When an X*m* input or output stands at its internal 1 state, all input-output ports affected by this X*m* input or output are bidirectionally connected together and stand at the same internal logic state or analog signal level. When an X*m* input or output stands at its internal 0 state, the connection associated with this set of dependency notation does not exist.

Although the transmission paths represented by X dependency are inherently bidirectional, use is not always made of this property. This is analogous to a piece of wire, which may be constrained to carry current in only one direction. If this is the case in a particular application, then the directional arrows shown in Figures 2.3-12, 2.3-13, and 2.3-14 are omitted.

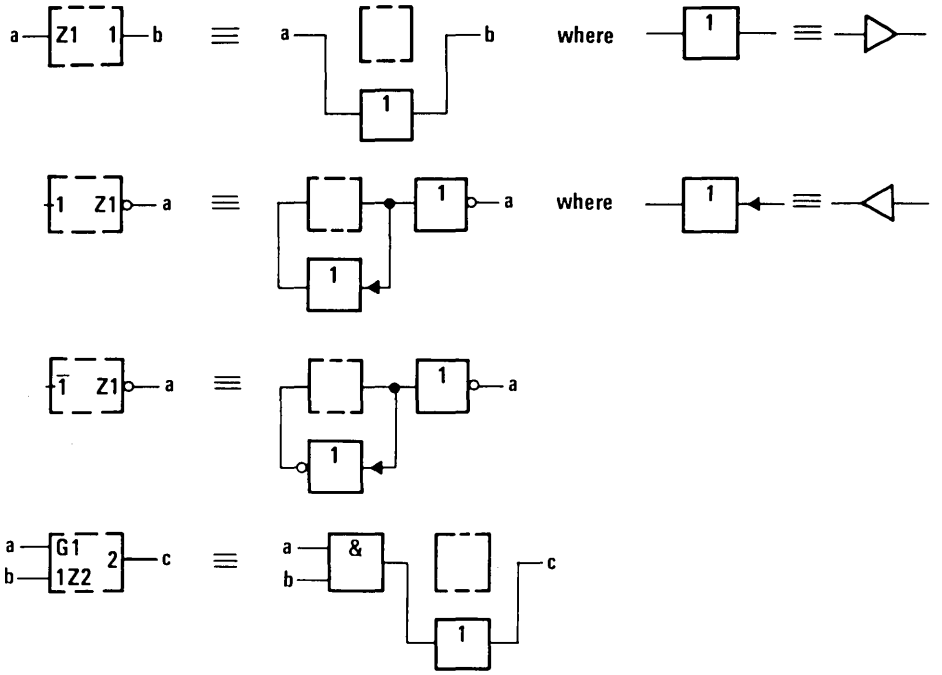
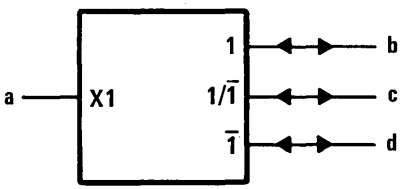


Figure 2.3-11. Z (Interconnection) Dependency



If a = 1, there is a bidirectional connection between b and c.

If a = 0, there is a bidirectional connection between c and d.

Figure 2.3-12. X (Transmission) Dependency

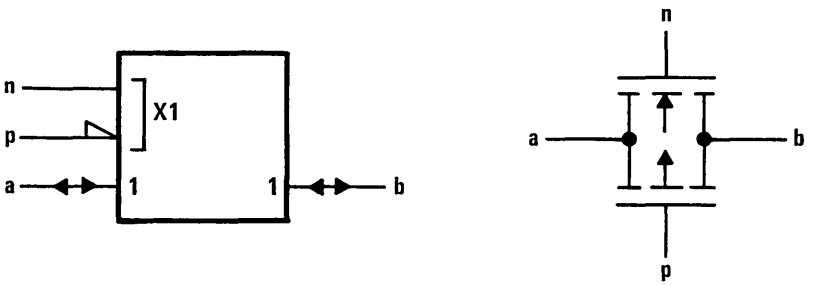


Figure 2.3-13. CMOS Transmission Gate Symbol and Schematic

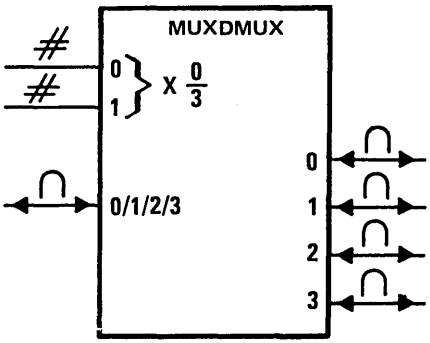


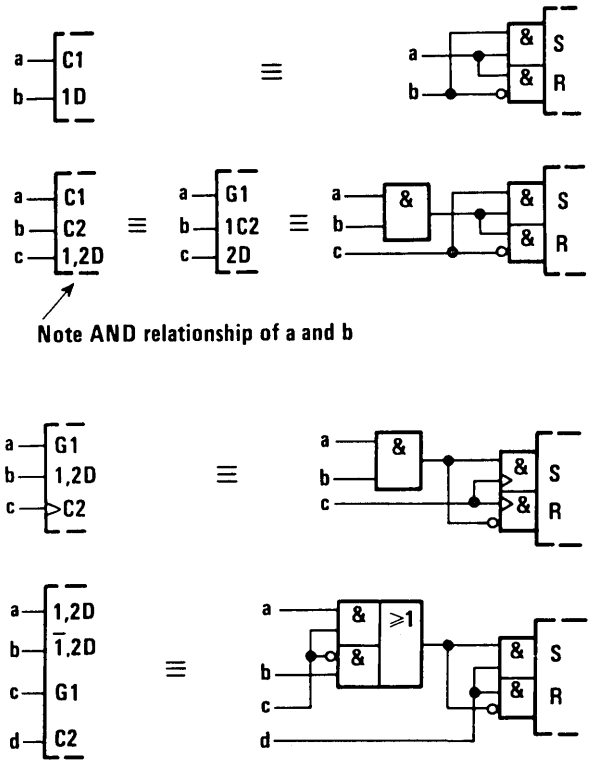
Figure 2.3-14. Analog Data Selector (Multiplexer/Demultiplexer)

2.3.4.8 C (Control) Dependency

The symbol denoting control dependency is the letter C.

Control inputs are usually used to enable or disable the data (D, J, K, R, or S) inputs of storage elements. They may take on their internal 1 states (be active) either statically or dynamically. In the latter case, the dynamic input symbol is used as shown in the third example of Figure 2.3-15.

When a C*m* input or output stands at its internal 1 state, the inputs affected by C*m* have their normally defined effect on the function of the element; i.e., these inputs are enabled. When a C*m* input or output stands at its internal 0 state, the inputs affected by C*m* are disabled and have no effect on the function of the element.



Input c selects which of a or b is stored when d goes low.

Figure 2.3-15. C (Control) Dependency

2.3.4.9 S (Set) and R (Reset) Dependencies

The symbol denoting set dependency is the letter S. The symbol denoting reset dependency is the letter R.

Set and reset dependencies are used if it is necessary to specify the effect of the combination R = S = 1 on a bistable element. Case 1 in Figure 2.3-16 does not use S or R dependency.

When an S*m* input is at its internal 1 state, outputs affected by the S*m* input will react, regardless of the state of an R input, as they normally would react to the combination S = 1, R = 0. See cases 2, 4, and 5 in Figure 2.3-16.

When an R*m* input is at its internal 1 state, outputs affected by the R*m* input will react, regardless of the state of an S input, as they normally would react to the combination S = 0, R = 1. See cases 3, 4, and 5 in Figure 2.3-16.

When an S*m* or R*m* input is at its internal 0 state, it has no effect.

Note that the noncomplementary output patterns in cases 4 and 5 are only pseudo stable. The simultaneous return of the inputs to S = R = 0 produces an unforeseeable stable and complementary output pattern.

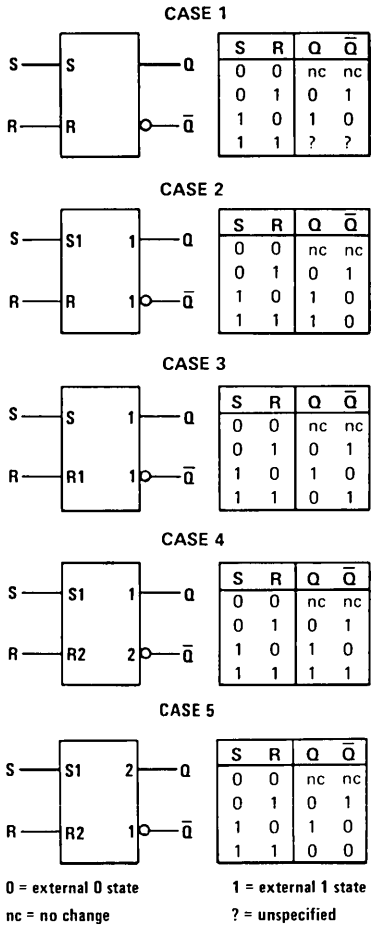
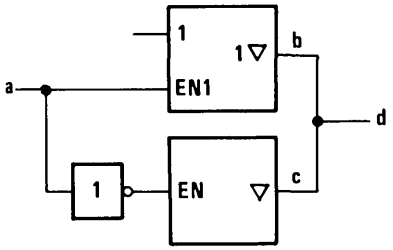


Figure 2.3-16. S (Set) and R (Reset) Dependencies

2.3.4.10 EN (Enable) Dependency

The symbol denoting enable dependency is the combination of letters EN.

An EN*m* input has the same effect on outputs as an EN input, see 2.3.3.3, but it affects only those outputs labeled with the identifying number *m*. It also affects those inputs labeled with the identifying number *m*. By contrast, an EN input affects all outputs and no inputs. The effect of an EN*m* input on an affected input is identical to that of a C*m* input (Figure 2.3-17).



If a = 0, b is disabled and d = c
If a = 1, c is disabled and d = b

Figure 2.3-17. EN (Enable) Dependency

When an EN*m* input stands at its internal 1 state, the inputs affected by EN*m* have their normally defined effect on the function of the element, and the outputs affected by this input stand at their normally defined internal logic states; i.e., these inputs and outputs are enabled.

When an EN*m* input stands at its internal 0 state, the inputs affected by EN*m* are disabled and have no effect on the function of the element, and the outputs affected by EN*m* are also disabled. Open-collector outputs are turned off, three-state outputs stand at their normally defined internal logic states but externally exhibit high impedance, and all other outputs (e.g., totem-pole outputs) stand at their internal 0 states.

2.3.4.11 M (MODE) Dependency

The symbol denoting mode dependency is the letter M.

Mode dependency is used to indicate that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

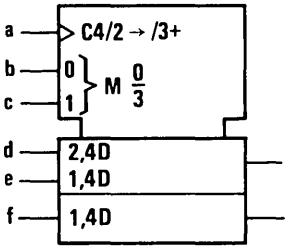
If an input or output has the same effect in different modes of operation, the identifying numbers of the relevant affecting M*m* inputs will appear in the label of that affected input or output between parentheses and separated by solidi (Figure 2.3-22).

2.3.4.11.1 M Dependency Affecting Inputs

M dependency affects inputs the same as C dependency. When an M*m* input or M*m* output stands at its internal 1 state, the inputs affected by this M*m* input or M*m* output have their normally defined effect on the function of the element; i.e., the inputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, the inputs affected by this M*m* input or M*m* output have no effect on the function of the element. When an affected input has several sets of labels separated by solidi (e.g., C4/2→/3+), any set in which the identifying number of the M*m* input or M*m* output appears has no effect and is to be ignored. This represents disabling of some of the functions of a multifunction input.

The circuit in Figure 2.3-18 has two inputs, **b** and **c**, that control which one of four modes (0, 1, 2, or 3) will exist at any time. Inputs **d**, **e**, and **f** are D inputs subject to dynamic control (clocking) by the **a** input. The numbers 1 and 2 are in the series chosen to indicate the modes so inputs **e** and **f** are only enabled in mode 1 (for parallel loading), and input **d** is only enabled in mode 2 (for serial loading). Note that input **a** has three functions. It is the clock for entering data. In mode 2, it causes right shifting of data, which means a shift away from the control block. In mode 3, it causes the contents of the register to be incremented by one count.



Note that all operations are synchronous.

In MODE 0 (b = 0, c = 0), the outputs remain at their existing states as none of the inputs has an effect.

In MODE 1 (b = 1, c = 0), parallel loading takes place thru inputs e and f.

In MODE 2 (b = 0, c = 1), shifting down and serial loading thru input d take place.

In MODE 3 (b = c = 1), counting up by increment of 1 per clock pulse takes place.

Figure 2.3-18. M (Mode) Dependency Affecting Inputs

2.3.4.11.2 M Dependency Affecting Outputs

When an M*m* input or M*m* output stands at its internal 1 state, the affected outputs stand at their normally defined internal logic states; i.e., the outputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, at each affected output any set of labels containing the identifying number of that M*m* input or M*m* output has no effect and is to be ignored. When an output has several different sets of labels separated by solidi (e.g., 2,4/3,5), only those sets in which the identifying number of this M*m* input or M*m* output appears are to be ignored.

Figure 2.3-19 shows a symbol for a device whose output can behave as either a 3-state output or an open-collector output depending on the signal applied to input **a**. Mode 1 exists when input **a** stands at its internal 1 state, and, in that case, the three-state symbol applies, and the open-element symbol has no effect. When **a** = 0, mode 1 does not exist so the three-state symbol has no effect, and the open-element symbol applies.

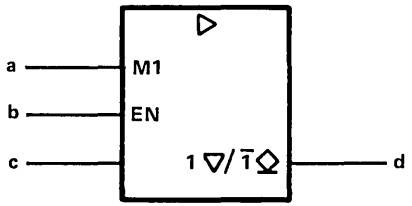


Figure 2.3-19. Type of Output Determined by Mode

In Figure 2.3-20, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 9. Since output **b** is located in the common-control block with no defined function outside of mode 1, the state of this output outside of mode 1 is not defined by the symbol.

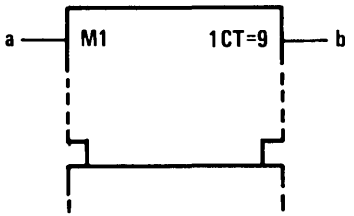


Figure 2.3-20. An Output of the Common-Control Block

In Figure 2.3-21, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 15. If input **a** stands at its internal 0 state, output **b** will stand at its internal 1 state only when the content of the register equals 0.

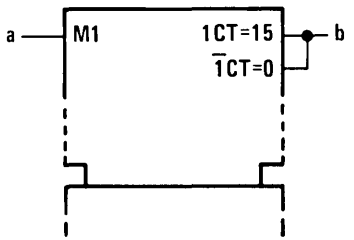


Figure 2.3-21. Determining an Output's Function

In Figure 2.3-22, inputs **a** and **b** are binary weighted to generate the numbers 0, 1, 2, or 3. This determines which one of the four modes exists.

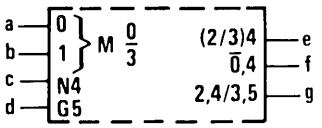


Figure 2.3-22. Dependent Relationships Affected by Mode

At output **e**, the label set causing negation (if **c** = 1) is effective only in modes 2 and 3. In modes 0 and 1, this output stands at its normally defined state as if it had no labels. At output **f**, the label set has effect when the mode is not 0 so output **e** is negated (if **c** = 1) in modes 1, 2, and 3. In mode 0, the label set has no effect so the output stands at its normally defined state. In this example, $\overline{0}$,4 is equivalent to (1/2/3)4. At output **g**, there are two label sets: the first set, causing negation (if **c** = 1), is effective only in mode 2; the second set, subjecting **g** to AND dependency on **d**, has effect only in mode 3.

Note that in mode 0 none of the dependency relationships has any effect on the outputs, so **e**, **f**, and **g** will all stand at the same state.

2.3.4.12 A (Address) Dependency

The symbol denoting address dependency is the letter A.

Address dependency provides a clear representation of those elements, particularly memories, that use address control inputs to select specified sections of a multildimensional array. Such a section of a memory array is usually called a word. The purpose of address dependency is to allow a symbolic presentation of the entire array. An input of the array shown at a particular element of this general section is common to the corresponding elements of all selected sections of the array. An output of the array shown at a particular element of this general section is the result of the OR function of the outputs of the corresponding elements of selected sections.

Inputs that are not affected by any affecting address input have their normally defined effect on all sections of the array, whereas inputs affected by an address input have their normally defined effect only on the section selected by that address input.

An affecting address input is labeled with the letter A followed by an identifying number that corresponds with the address of the particular section of the array selected by this input. Within the general section presented by the symbol, inputs and outputs affected by an A*m* input are labeled with the letter A, which stands for the identifying numbers, i.e., the addresses, of the particular sections.

Figure 2.3-23 shows a 3-word by 2-bit memory having a separate address line for each word and uses EN dependency to explain the operation. To select word 1, input **a** is taken to its 1 state, which establishes mode 1. Data can now be clocked into the inputs marked "1,4D." Unless words 2 and 3 are also selected, data cannot be clocked in at the inputs marked "2,4D" and "3,4D." The outputs will be the OR functions of the selected outputs; i.e., only those enabled by the active EN functions.

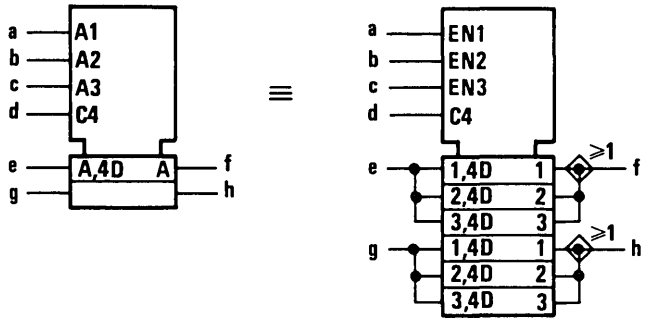


Figure 2.3-23. A (Address) Dependency

The identifying numbers of affecting address inputs correspond with the addresses of the sections selected by these inputs. They need not necessarily differ from those of other affecting dependency inputs (e.g., G, V, N, . . .), because, in the general section presented by the symbol, they are replaced by the letter A.

If there are several sets of affecting A*m* inputs for the purpose of independent and possibly simultaneous access to sections of the array, then the letter A is modified to 1A, 2A, ... Since they have access to the same sections of the array, these sets of A inputs may have the same identifying numbers. The symbols for 'HC170 or SN74LS170 make use of this.

Figure 2.3-24 is another illustration of the concept.

2.3.5 Bistable Elements

The dynamic input symbol, the postponed output symbol, and dependency notation provide the tools to differentiate four main types of bistable elements and make synchronous and asynchronous inputs easily recognizable (Figure 2.3-5). The first column shows the essential distinguishing features; the other columns show examples.

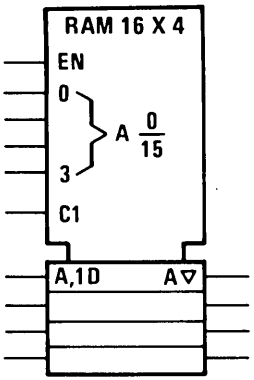


Figure 2.3-24. Array of 16 Sections of Four Transparent Latches with 3-State Outputs Comprising a 16-Word × 4-Bit Random-Access Memory

Table 2.3-4. Summary of Dependency Notation

TYPE OF DEPENDENCY	LETTER SYMBOL*	AFFECTING INPUT AT ITS 1-STATE	AFFECTING INPUT AT ITS 0-STATE
Address	A	Permits action (address selected)	Prevents action (address not selected)
Control	C	Permits action	Prevents action
Enable	EN	Permits action	Prevents action of inputs ◇outputs off ▽outputs at external high impedance, no change in internal logic state Other outputs at internal 0 state
AND	G	Permits action	Imposes 0 state
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Negate (Ex-OR)	N	Complements state	No effect
Reset	R	Affected output reacts as it would to S = 0, R = 1	No effect
Set	S	Affected output reacts as it would to S = 1, R = 0	No effect
OR	V	Imposes 1 state	Permits action
Transmission	X	Bidirectional connection exists	Bidirectional connection does not exist
Interconnection	Z	Imposes 1 state	Imposes 0 state

* These letter symbols appear at the AFFECTING input (or output) and are followed by a number. Each input (or output) AFFECTED by that input is labeled with that same number. When the labels EN, R, and S appear at inputs without the following numbers, the descriptions above do not apply. The action of these inputs is described under "Symbols Inside the Outline," see 2.3.3.3.

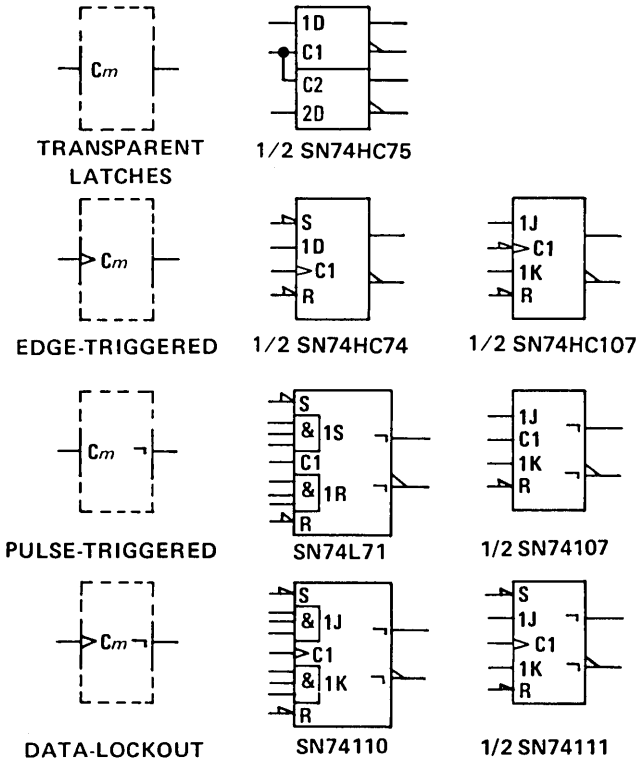


Figure 2.3-25. Four Types of Bistable Circuits

Transparent latches have a level-operated control input. The D input is active as long as the C input is at its internal 1 state. The outputs respond immediately. Edge-triggered elements accept data from D, J, K, R, or S inputs on the active transition of C. Pulse-triggered elements require the setup of data before the start of the control pulse; the C input is considered static since the data must be maintained as long as C is at its 1 state. The output is postponed until C returns to its 0 state. The data-lockout element is similar to the pulse-triggered version except that the C input is considered dynamic in that, shortly after C goes through its active transition, the data inputs are disabled, and data does not have to be held. However, the output is still postponed until the C input returns to its initial external level.

Notice that synchronous inputs can be readily recognized by their dependency labels (1D, 1J, 1K, 1S, 1R) compared to the asynchronous inputs (S, R), which are not dependent on the C inputs.

2.3.6 Coders

The general symbol for a coder or code converter is shown in Figure 2.3-26. X and Y may be replaced by appropriate indications of the code used to represent the information at the inputs and at the outputs, respectively.

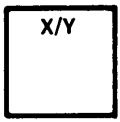


Figure 2.3-26. Coder General Symbol

Indication of code conversion is based on the following rule:

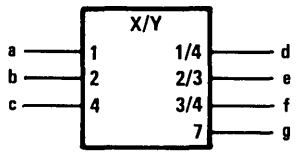
> Depending on the input code, the internal logic states of the inputs determine an internal value. This value is reproduced by the internal logic states of the outputs, depending on the output code.

The indication of the relationships between the internal logic states of the inputs and the internal value is accomplished by:

1) labeling the inputs with numbers. In this case, the internal value equals the sum of the weights associated with those inputs that stand at their internal 1-state, or by
2) replacing X by an appropriate indication of the input code and labeling the inputs with characters that refer to this code.

The relationships between the internal value and the internal logic states of the outputs are indicated by:

1) labeling each output with a list of numbers representing those internal values that lead to the internal 1-state of that output. These numbers shall be separated by solidi as in Figure 2.3-27. This labeling may also be applied when Y is replaced by a letter denoting a type of dependency



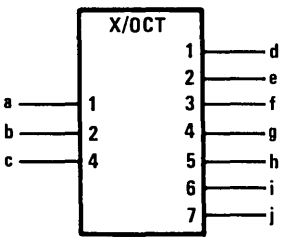
TRUTH TABLE

INPUTS			OUTPUTS			
c	b	a	g	f	e	d
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	1	1	0
1	0	0	0	1	0	1
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

Figure 2.3-27. An X/Y Code Converter

(see section 2.3.7). If a continuous range of internal values produces the internal 1 state of an output, this can be indicated by two numbers that are inclusively the beginning and the end of the range, with these two numbers separated by three dots (e.g., 4 . . . 9 = 4/5/6/7/8/9) or by

2) replacing Y by an appropriate indiction of the output code and labeling the outputs with characters that refer to this code as in Figure 2.3-28.



TRUTH TABLE

INPUTS			OUTPUTS						
c	b	a	j	i	h	g	f	e	d
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	1	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	1	0	0	0	0
1	1	0	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0

Figure 2.3-28. An X/Octal Code Converter

Alternatively, the general symbol may be used together with an appropriate reference to a table in which the relationship between the inputs and outputs is indicated. This is a recommended way to symbolize a PROM after it has been programmed.

2.3.7 Use of a Coder to Produce Affecting Inputs

It often occurs that a set of affecting inputs for dependency notation is produced by decoding the signals on certain inputs to an element. In such a case, use can be made of the symbol for a coder as an embedded symbol (Figure 2.3-29).

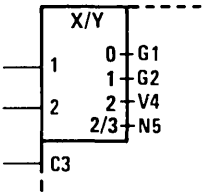


Figure 2.3-29. Producing Various Types of Dependencies

If all affecting inputs produced by a coder are of the same type as their identifying numbers shown at the outputs of the coder, Y (in the qualifying symbol X/Y) may be replaced by the letter denoting the type of dependency. The indications of the affecting inputs should then be omitted (Figure 2.3-30).

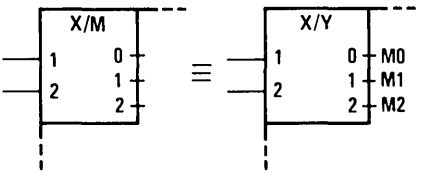


Figure 2.3-30. Producing One Type of Dependency

2.3.8 Use of Binary Grouping to Produce Affecting Inputs

If all affecting inputs produced by a coder are of the same type and have consecutive identifying numbers not necessarily corresponding with the numbers that would have been shown at the outputs of the coder, use can be made of the binary grouping symbol. *k* external lines effectively generate 2^k internal inputs. The bracket is followed by the letter denoting the type of dependency followed by m1/m2. The m1 is to be replaced by the smallest identifying number and the m2 by the largest one, as shown in Figure 2.3-31.

2.3.9 Sequence of Input Labels

If an input having a single functional effect is affected by other inputs, the qualifying symbol (if there is any) for that functional effect is preceded by the labels corresponding to the affecting inputs. The left-to-right order of these preceding labels is the order in which the effects or modifications must be applied. The affected input has no functional effect on the element if the logic state of any one of the affecting inputs, considered separately, would cause the affected input to have no effect, regardless of the logic states of other affecting inputs.

If an input has several different functional effects or has several different sets of affecting inputs, depending on the mode of action, the input may be shown as often as required. However, there are cases in which this method of

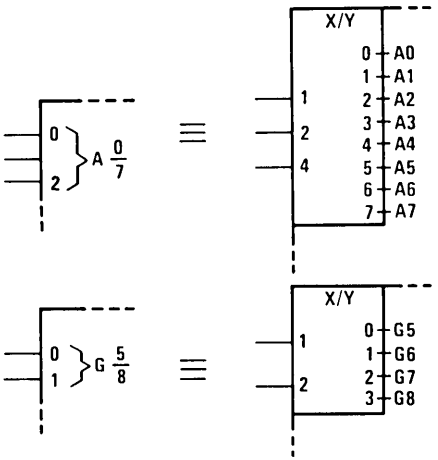


Figure 2.3-31. Use of the Binary Grouping Symbol

presentation is not advantageous. In those cases, the input may be shown once with the different sets of labels separated by solidi (Figure 2.3-32). No meaning is attached to the order of these sets of labels. If one of the functional effects of an input is that of an unlabeled input to the element, a solidus will precede the first set of labels shown.

If all inputs of a combinational element are disabled (caused to have no effect on the function of the element), the internal logic states of the outputs of the element are not specified by the symbol. If all inputs of a sequential element are disabled, the content of this element is not changed, and the outputs remain at their existing internal logic states.

Labels may be factored using algebraic techniques (Figure 2.3-33).

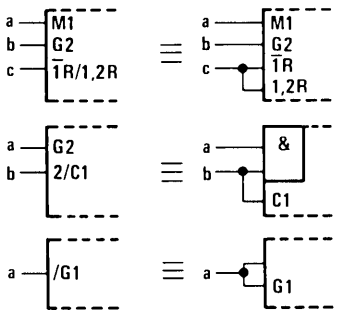


Figure 2.3-32. Input Labels

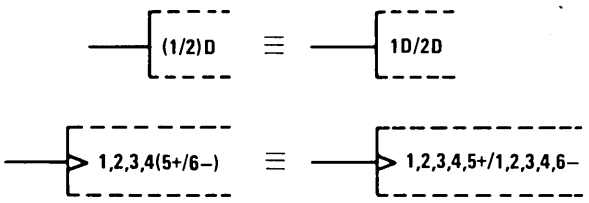


Figure 2.3-33. Factoring Input Labels

2.3.10 Sequence of Output Labels

If an output has a number of different labels, regardless of whether they are identifying numbers of affecting inputs or outputs or not, these labels are shown in the following order:

1) If the postponed output symbol has to be shown, this comes first, if necessary preceded by the indications of the inputs to which it must be applied
2) Followed by the labels indicating modifications of the internal logic state of the output, such that the left-to-right order of these labels corresponds with the order in which their effects must be applied
3) Followed by the label indicating the effect of the output on inputs and other outputs of the element.

Symbols for open-circuit or 3-state outputs, where applicable, are placed just inside the outside boundary of the symbol adjacent to the output line (Figure 2.3-34).

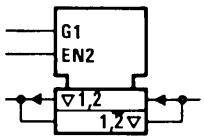


Figure 2.3-34. Placement of 3-State Symbols

If an output needs several different sets of labels that represent alternative functions (e.g., depending on the mode of action), these sets may be shown on different output lines that must be connected outside the outline. However, there are cases in which this method of presentation is not advantageous. In those cases, the output may be shown once with the different sets of labels separated by solidi (Figure 2.3-35).

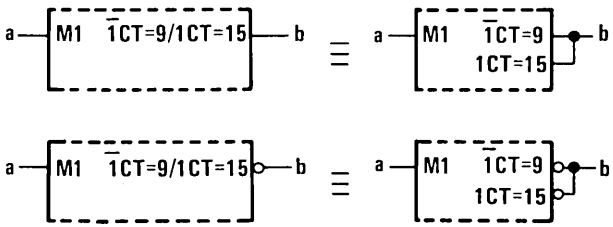


Figure 2.3-35. Output Labels

Two adjacent identifying numbers of affecting inputs in a set of labels that are not already separated by a nonnumeric character should be separated by a comma.

If a set of labels of an output not containing a solidus contains the identifying number of an affecting M*m* input standing at its internal 0 state, this set of labels has no effect on that output.

Labels may be factored using algebraic techniques (Figure 2.3-36).

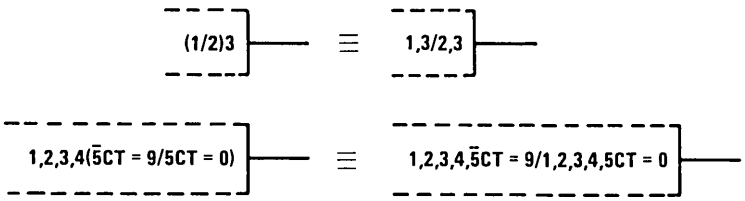


Figure 2.3-36. Factoring Output Labels

If you have questions on this Explanation of Logic Symbols, please contact:

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Dallas, Texas 75265

Telephone (214) 995-2659

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Institute of Electrical and Electronics Engineers, Inc.
IEEE Standards Office
345 East 47th Street
New York, N.Y. 10017

International Electrotechnical Commission (IEC) publications may be purchased from:

American National Standards Institute, Inc.
1430 Broadway
New York, N.Y. 10018

3 ACL Design Specifications

3.1 EPIC™ Advanced CMOS Logic Output Edge Control†

3.1.1 Introduction

Integrated circuits have become faster because of improvements in process technologoy. Switching-induced transients are a serious limitation on the speed of integrated circuits. Inductance in the ground and power supply (V_{CC}) leads of the package introduces large voltage swings on the silicon die because of the fast transitions of the output currents. For a CMOS output driving a capacitive load, the transient current i(t) is given by:

$$i = C \times dv/dt \qquad (1)$$

Voltage is related to inductance (L) and to the time rate of change of current (di/dt) by the equation:

$$v = -L \times di/dt \qquad (2)$$

These ground and V_{CC} spikes, or noise peaks, can appear at the output as false signals, severely limiting the usefulness of the faster devices. As more outputs of an IC are switched simultaneously, the effect is additive, resulting in more severe spikes, and further limiting the usefulness of multiple-output devices. Even unswitched outputs may have unacceptable spikes from V_{CC} and ground movement. This phenomenon is not unique to CMOS but applies to all advanced, high-speed integrated circuits.

3.1.2 Reducing Voltage Spikes

3.1.2.1 Reduction Through Package Method

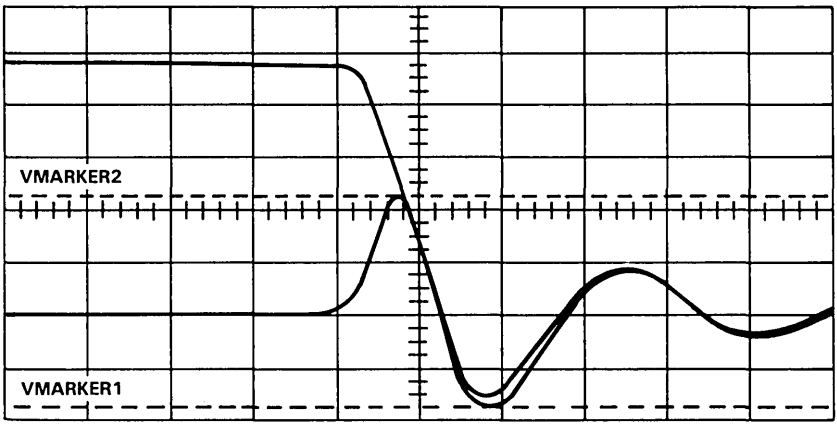
To reduce voltage spikes, the value of inductance (L) in the voltage equation can be lowered. Decreasing the overall size of the package, as was done in Small Outline Integrated Circuit (SOIC) packages, lowers inductance as shown in Table 3.1-1.

EPIC and OEC are trademarks of Texas Instruments Incorporated.
†Written by C. Spurlin and D. Stein.

Table 3.1-1. 20-Pin DIP and SOIC Package Lead Inductances

PIN	DIP	SOIC
1,10,11,20	13.7 nH	4.2 nH
2,9,12,19	11.1	3.8
3,8,13,18	8.6	3.3
4,7,14,17	6.0	2.9
5,6,15,16	3.4	2.4

The effects of these different inductance values on switching spike amplitudes are compared in Figures 3.1-1 and 3.1-2.



CH. 1 = 1.000 V/DIV
CH. 2 = 1.000 V/DIV
TIMEBASE = 5.00 ns/DIV
DELTA V = 4.000 V
VMARKER1 = −1.760 V
OFFSET = 2.000 V
DELAY = 30.400 ns
VMARKER2 = 2.240 V

TRIGGER MODE : Edge
ON POS. EDGE ON TRIG3

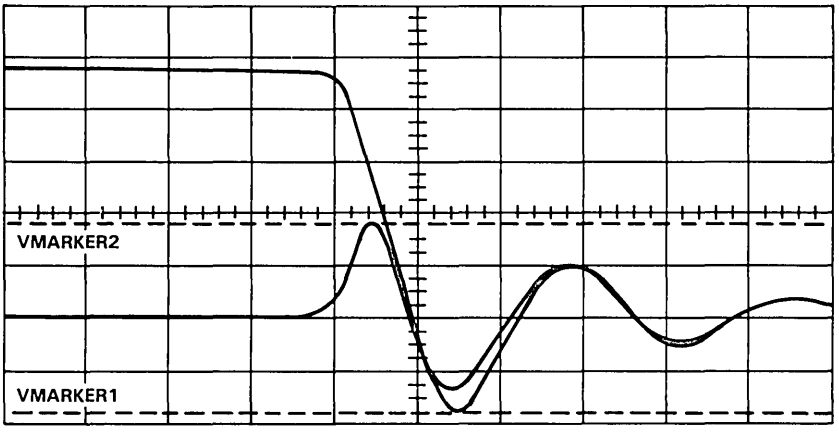
AC244 -1 DIP
V_{CC} = 5 V 25°C
7 SWITCHING, 1 LOW (PIN #18)
INPUTS 20% — 80% RAIL

TRIGGER LEVELS
TRIG3 = 746.0 mV
HOLDOFF = 70.000 ns

Figure 3.1-1. Competitor's Simultaneous Switching Performance in a DIP

These curves are actual lab data from another manufacturer's AC244 (8-output CMOS buffer/line driver) driving a load of 50 pF and 500 Ω to ground. One output was held low while the other seven were switched high to low. That is a typical simultaneous switching test to see the effects of V_{CC} or ground bounce on an unswitched output. The worst-case bounce usually

occurs on the highest-inductance end pins. Notice in Figure 3.1-1 that the noise amplitude in the DIP is 2.24 V, while in the SOIC package (Figure 3.1-2) it is 420 mV lower. While this reduction appears significant, it still does not guarantee reliable system operation.



CH. 1	= 1.000 V/DIV	AC244 SURFACE MOUNT
CH. 2	= 1.000 V/DIV	V_{CC} = 5 V 25°C
TIMEBASE	= 5.00 ns/DIV	7 SWITCHING, 1 LOW (PIN #18)
DELTA V	= 3.600 V	INPUTS 20% – 80% RAIL
VMARKER1	= –1.780 V	
OFFSET	= 2.000 V	SINGLE SWITCHING
DELAY	= 42.600 ns	t_{PLH} 2 to 18 5.60 ns
VMARKER2	= 1.820 V	t_{PHL} 2 to 18 5.25 ns
		TRIGGER LEVELS
TRIGGER MODE : Edge		TRIG3 = 56.00 mV
ON POS. EDGE ON TRIG3		HOLDOFF = 70.000 ns

Figure 3.1-2. Competitor's Simultaneous Switching Performance in an SOIC

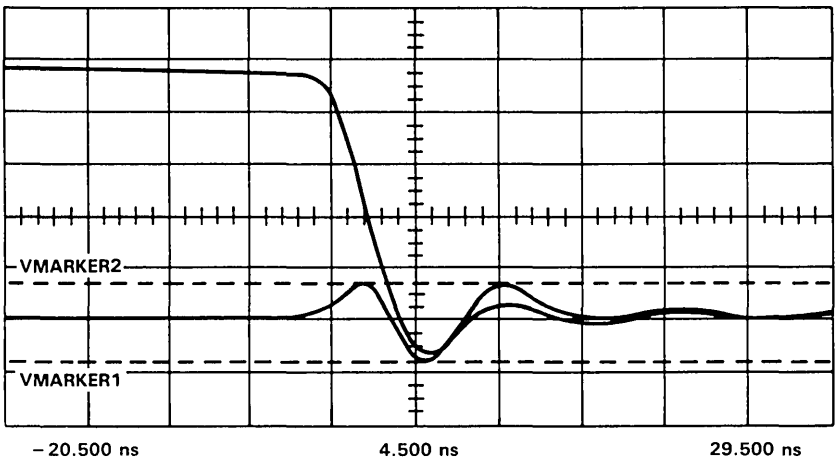
Since end pins have the highest inductance, another method of reducing spikes is to use the lower-inductance center pins for V_{CC} and ground. Inductance may be further reduced by using multiple center V_{CC} and ground pins. That is one of the strategies in the Texas Instruments Advanced CMOS Logic (ACL) family. Future advancements in packaging materials may lead to even lower inductances; however, because the device transition rates increase as package inductance decreases, other approaches must be explored.

3.1.2.2 Reduction Through Circuit Method

A CMOS circuit method can reduce the di/dt portion of the voltage equation by slowing the output rising and falling edges, and yet can maintain a

reasonable total propagation delay. That circuit method is referred to as OEC™, which is implemented on Texas Instruments ACL integrated circuits and for which Texas Instruments has several patents pending.

The improvement attained by this circuit can be seen by comparing Figure 3.1-3 with Figure 3.1-2. Figure 3.1-3 shows simultaneous switching waveforms for the Texas Instruments AC11244 employing OEC™ in a multiple-center-power-pin SOIC package.



CH. 1	= 1.000 V/DIV	TI AC11244 -1 SOIC
CH. 2	= 1.000 V/DIV	V_{CC} = 5 V 25°C
TIMEBASE	= 5 ns/DIV	7 SWITCHING, 1 LOW (PIN #1)
DELTA V	= 1.500 V	INPUTS 20% – 80% RAIL
VMARKER1	= -0.820 V	
OFFSET	= 2.000 V	
DELAY	= 4.500 ns	
VMARKER2	= 0.680 V	
		TRIGGER LEVELS
TRIGGER MODE : EDGE		TRIG3 = 750.0 mV
ON NEG. EDGE ON TRIG3		HOLDOFF = 70.000 ns

Figure 3.1-3. Texas Instruments Simultaneous Switching Performance in an SOIC

3.1.3 Design Considerations

When a transistor has been in the nonconducting or "off" state and is then turned on, the flow of charge through the transistor rises from zero to some final value that, if not externally limited, tends to depend on the size of the transistor. The rate of change of this current with respect to time (di/dt) can be quite high, especially as process technology continues to improve device speeds. Larger values of di/dt naturally produce larger voltage spikes.

Figure 3.1-4 shows the current through a transistor as it turns on and the resulting di/dt value over the same time period. Notice that di/dt rises from zero to a peak and then falls back to zero after the current through the transistor has reached steady-state value.

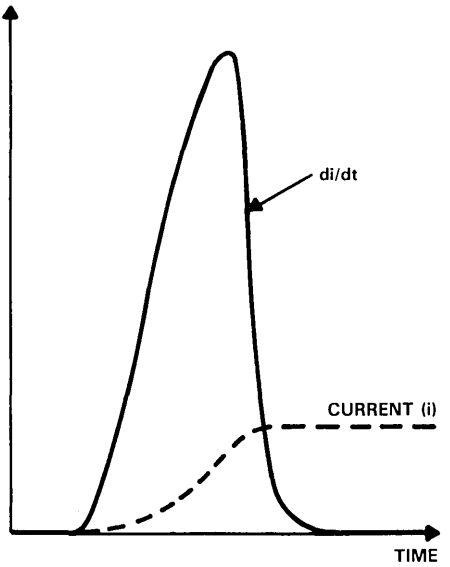


Figure 3.1-4. Current Through a Transistor and Value of di/dt

The di/dt peak could be reduced by making the output transistor smaller, lowering the steady-state value of current through the transistor, and slowing the rate at which it reaches that lowered value. However, compromising the current-handling capability of the product line is not an acceptable solution. Fan-out and loading specifications, propagation-delay considerations, and the ability to drive transmission lines require that outputs be sufficiently large.

Since reducing the output transistor size helps to reduce the peak di/dt factor, the large transistor could be split in half and only one part allowed to turn on at first. The di/dt would rise from zero to a lesser peak and then begin to fall back to zero. Now, the second half could be turned on. The di/dt value at this point would be the sum of the first half that is decreasing toward zero and the second half that is just beginning to increase. If the turn-on of the second half was delayed properly, the resulting maximum peak di/dt for the entire output transistor would be reduced. The output voltage waveform would show a slowing of the edge rate as the transistor turned on, which, in many cases, is a desirable feature in high-speed logic families if propagation delays are not excessive.

3.1.4 Circuit Design—Grading Turn-On

The circuit could be improved further by splitting the output transistor into many very small parts or subtransistors with sequential turn-on of each part. The steady-state value of current through just one small subtransistor is significantly less than the total. By splitting the total current into a series of smaller currents distributed over time, the effective di/dt is reduced. This successive turn-on of the subtransistors may be referred to as "graded" or "graduated" turn-on. Adjusting the number and size of subtransistors for different amounts of grading allows the designer to achieve the best compromise between reduced spikes and overall propagation delay.

The structure of a polysilicon gate MOS transistor permits a simple method to grade the turn-on. The transistor is a multisegment device with alternating sources and drains. A polysilicon gate runs between each source-drain pair. These gate segments are usually shorted in parallel by polysilicon interconnect or by contacts to metal so that the gate signal is applied to all segments simultaneously. That procedure can be modified to grade the turn-on by removing portions of the polysilicon gate to form a serpentine pattern, and by driving the gate from one end. (See Figure 3.1-5.) That arrangement uses the resistance of the polysilicon and the capacitance of each gate segment to form a distributed R-C network, which slows down the turn-on of each succeeding segment. That technique controls output edge rates, while maintaining high DC current-handling capability.

Figure 3.1-6(a) shows the equivalent circuit schematic for a MOS distributed-output transistor where each subtransistor represents one segment of the large, graded transistor, and each resistor represents the polysilicon gate resistance of that subtransistor.

Distributed transistor action provides an effective means for controlling di/dt noise in the CMOS circuit by slowing the output edge rates. However, the circuit as shown in Figure 3.1-6(a) has an undesirable slow turn-off in addition to the desired slow turn-on. With regard to power dissipation capacitance (C_{pd}) in a CMOS device, this slow turn-off is a major disadvantage.

When switching a CMOS output pair, one P-channel and one N-channel transistor both conduct until the desired "off" transistor turns completely off. The current shunted from the power supply to ground through this output pair is wasted because it does not contribute to driving the load. This thru-current can be minimized only by rapidly turning off all the segments. This is accomplished by evenly distributing several small, turn-off transistors along the polysilicon path of each output transistor. They are controlled by a signal that is the inverse of the one feeding the distributed gate. Figure 3.1-6(b) shows an output transistor with these small turn-off transistors.

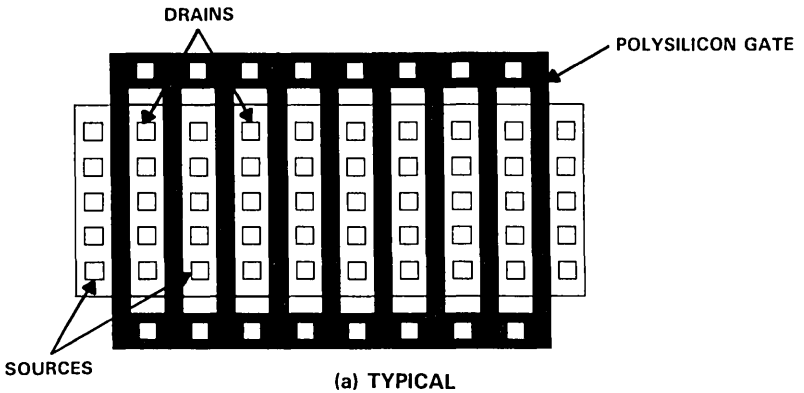


Figure 3.1-5. CMOS Transistor Gate Layout

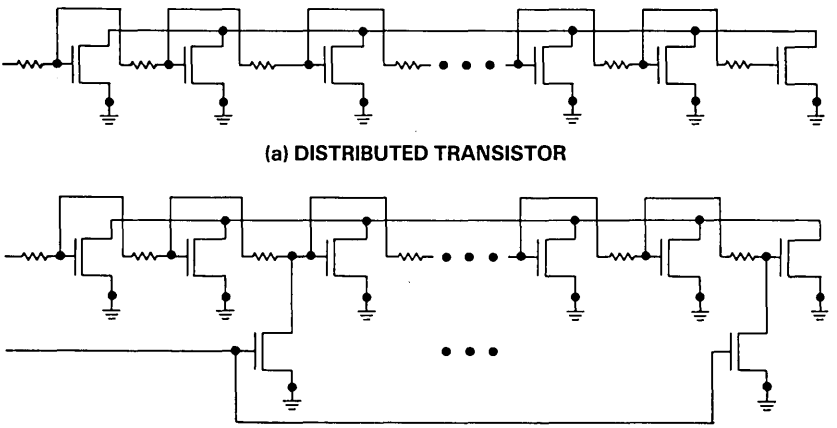


Figure 3.1-6. Equivalent Schematics

The small transistors do not increase the chip area significantly, since they replace the lumped transistor that is normally part of the predriver stage in a typical CMOS circuit. Thru-current improvement results are shown in Figure 3.1-7.

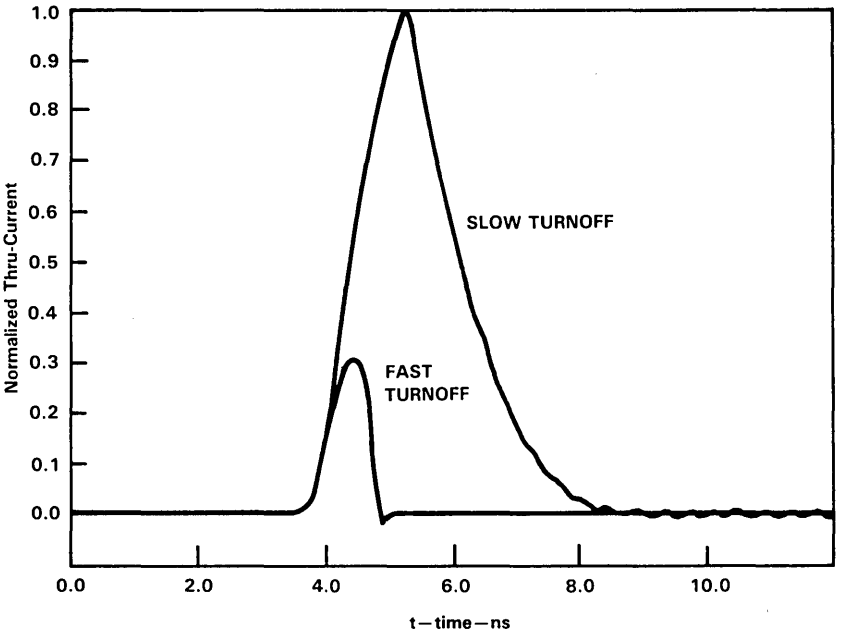


Figure 3.1-7. Effect of Added Pull-Downs on Thru-Current

Both transistors in a CMOS output are typically sized to handle the same amount of current. Because the current-handling ability of an N-channel transistor is higher than that of a P-channel transistor of the same size, a typical output pair can have an N-channel with approximately one-third the size of the P-channel. Because of its large size, the output P-channel transistor contains polysilicon gate material with enough distributed resistance and capacitance to provide an R-C time delay that is sufficient to grade the turn-on. By comparison, the serpentine polysilicon gate of the smaller N-channel has only one-third of the resistance and only one-third of the capacitance. The resulting R-C time constant product is roughly one-ninth of that for the P-channel gate. Without any extra measures, graded turn-on of the N-channel subtransistors would be only one-ninth as effective as it is for those of the P-channel. A silicided polysilicon gate material is used in Texas Instruments CMOS process to reduce the parasitic interconnection resistances, affording

shorter internal propagation delays. This low-resistivity gate material provides an R-C time delay in the N-channel output transistor that is too short to effectively grade the turn-on.

3.1.5 Circuit Design—Controlling Gate Voltage

Additional circuit design techniques are required to achieve a graded turn-on in the output N-channel that provides sufficient reduction in di/dt. Current through a MOS transistor can be limited by the amount of voltage applied to its gate. This is given by the basic MOS drain current equation:

$$Id = k\,[(Vg - Vt)\,Vds - Vds^2/2] \qquad (3)$$

Figure 3.1-8 shows a method for gate voltage control on the N-channel subtransistors. It uses a pull-down transistor and some logic to create a temporary I-R voltage drop across the length of the serpentine gate.

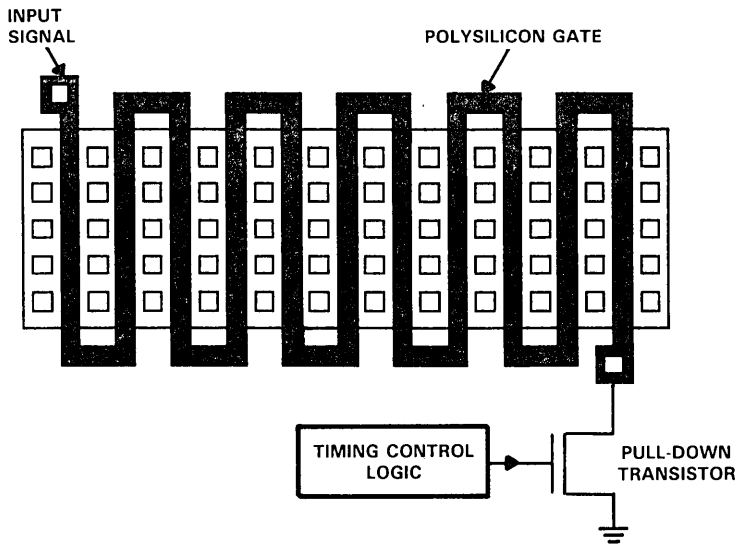


Figure 3.1-8. "Distributed" N-Channel with Gate Voltage Control

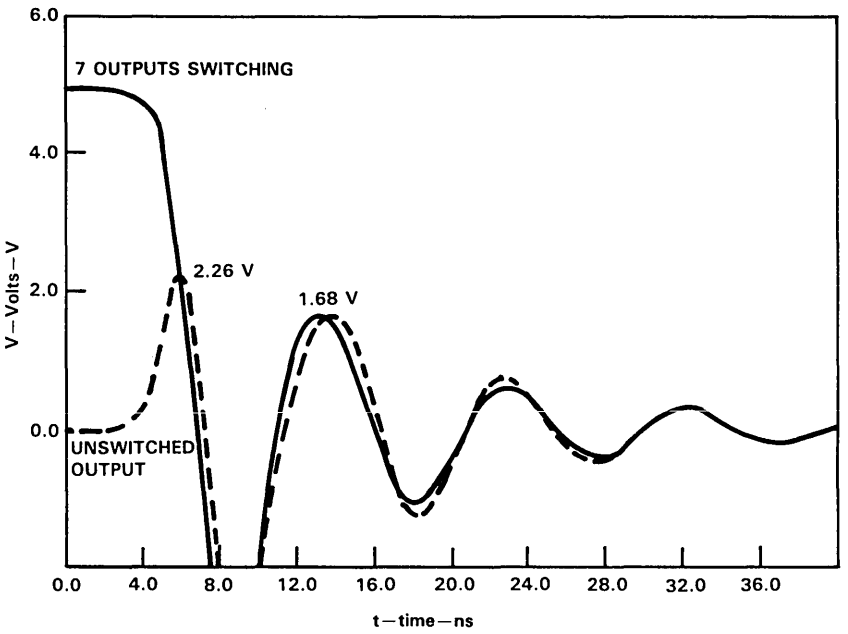
Notice that the pull-down transistor is attached to the far end of the serpentine gate opposite the end where the turn-on signal is applied. The logic circuit is able to turn on the pull-down transistor at the same time that the signal on the other end of the poly gate goes high, thus forcing an I-R voltage drop across the entire length of polysilicon gate material. Acting as a resistor divider, the gate material provides full gate voltage on only the first subtransistor and successively lower gate voltages on the following subtransistors, thereby

limiting the amount of current through them. The logic circuit must provide a delay that is controlled by time or a voltage level and then turn off the pull-down transistor, allowing the gate voltage on all the subtransistors to rise.

3.1.6 Characteristics of OEC™ Design

The Texas Instruments AC11244 has reduced switching noise in a multiple-center-power-pin package, because it employs OEC™ (as shown in Figure 3.1-3). No AC11244 circuit without OEC™ is available that could be used in a comparison of OEC™ vs lumped output performance; however, we can use SPICE to predict effects. In Figures 3.1-9 and 3.1-10, a comparison of output waveforms shows the advantage of OEC™.

Figure 3.1-9 shows two SPICE-simulated waveforms with typical noise spikes seen during simultaneous switching of an octal device (AC244) with center

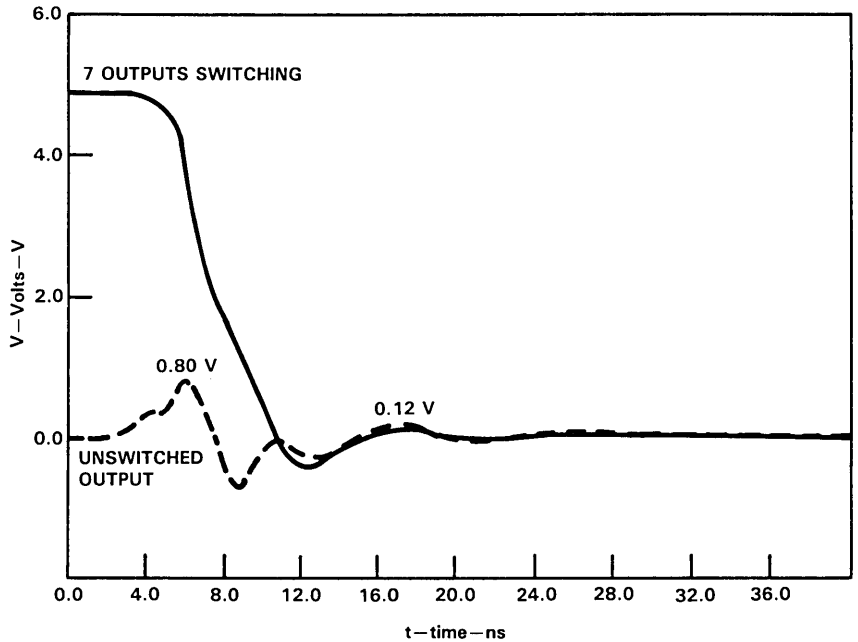


V_{CC} = 5 V
C_{LOAD} = 50 pF
R_{LOAD} = 500 Ω
TEMP = 25°C
PACKAGE = DUAL-IN-LINE

Figure 3.1-9. SPICE Results — Simultaneous Switching OCTAL Device with Standard Lumped Output

ground and V_{CC} pins and conventional, lumped outputs. One voltage waveform is from one of seven outputs that are switching simultaneously, and the other is from the eighth output that is not switching and should remain quiet. Notice that the noise spikes from the lumped output are large enough to cause false signals when presented at the input of other TTL and CMOS circuits. Improved simultaneous switching performance from the AC11244 is indicated in the SPICE-simulated waveforms shown in Figure 3.1-10.

These output waveforms are from the same eight-output circuit configuration, but with the addition of OEC™ design. The package model in both simulations is a multiple-center-power-pin Plastic Dual In-line Package (PDIP). A dramatic reduction in noise peak from 2.26 V to 0.8 V is realized in this example. This can mean the difference between an IC that provides reliable system performance and one that does not.



V_{CC} = 5 V
C_{LOAD} = 50 pF
R_{LOAD} = 500 Ω
TEMP = 25°C
PACKAGE = DUAL-IN-LINE

Figure 3.1-10. SPICE Results — Simultaneous Switching with Distributed Output

3.1.7 Summary

Processing technology for integrated circuits continues to improve. As feature sizes become ever smaller, device speeds increase, and the problem of switching-induced transients grows more severe. Along with improvements in packaging, circuit design methods for tailoring output transitions are necessary to solve the problem. The output edge control (OEC™) circuit described here is relatively simple, is easily implemented, and provides a good compromise between reduced switching spikes and overall propagation delay.

3.2 Advanced CMOS Logic Input Circuitry Characteristics†

3.2.1 Introduction

Texas Instruments Advanced CMOS Logic (ACL) family offers system designers the high-speed performance of advanced bipolar families such as 54/74F with the inherent advantages of low CMOS power consumption. This section presents the characteristics of Texas Instruments ACL device inputs. Items covered are unused inputs, input capacitance, and input current and voltage limits. The parameters of an ACL input must be understood so that the system design engineer can properly calculate fan-out and terminate unused portions of the circuit correctly as well as protect the input circuitry from potential damage due to excessive currents or voltages.

3.2.2 ACL Input Circuitry

There are two versions of input circuits for the Texas Instruments ACL family as shown in Figures 3.2-1 and 3.2-2. The 54/74AC input circuit is designed to have an input switching threshold of 50% V_{CC} while the 54/74ACT input circuit has a switching threshold of 1.5 V for a V_{CC} of 5.0 V. The 54/74AC devices are designed for use in pure CMOS applications while the 54/74ACT devices function as translators from TTL to CMOS applications. Both versions are designed to provide approximately 100 mV of hysteresis to increase their noise margins and to help ensure the devices will be free from oscillation with input transitions of ± 10 ns/V. In each case, hysteresis is provided via the inverter I_1 and the PMOS transistor Q_3.

The input circuitry incorporated in the ACL family also incorporates several components for input electrostatic discharge (ESD) protection. These components also function to clamp input voltages greater than V_{CC} or less than GND. The circuitry has an absolute maximum‡ DC input diode current rating of ± 20 mA which must not be exceeded. Figure 3.2-3 shows the circuitry used for ESD protection.

†Written by D. Powers.

‡Stresses beyond those listed under absolute-maximum ratings in any Texas Instruments data sheet may cause permanent damage to devices. Absolute-maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the recommended operating conditions portion of the data sheet is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

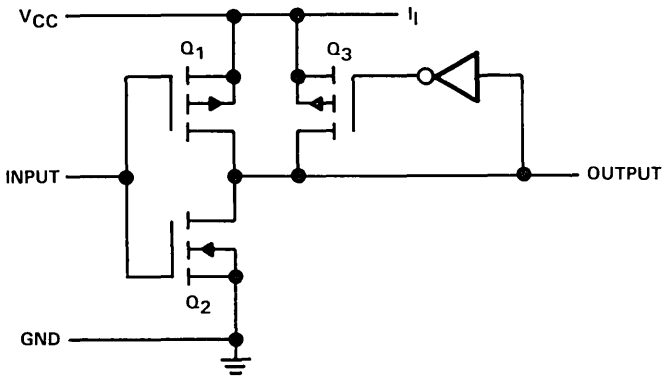


Figure 3.2-1. 54/74AC Input Circuit

The diffused PNP transistor cell is formed by placing a diffused p+ resistor in an n tank on a p− epi layer. This structure forms a diffused resistor, which is standard in ESD protection circuits for CMOS technologies as well as a diffused PNP transistor. The diffused PNP transistor interacts with the SCR input protection circuit to absorb ESD energy. This interaction forms the primary ESD protection circuit for an ACL input. The NMOS transistor Q_m is used to guarantee a low voltage at the internal gate input terminal as well as to provide a secondary level of ESD protection. The resistance of the emitter of the diffused transistor is used to limit the current flow through the NMOS transistor Q_m.

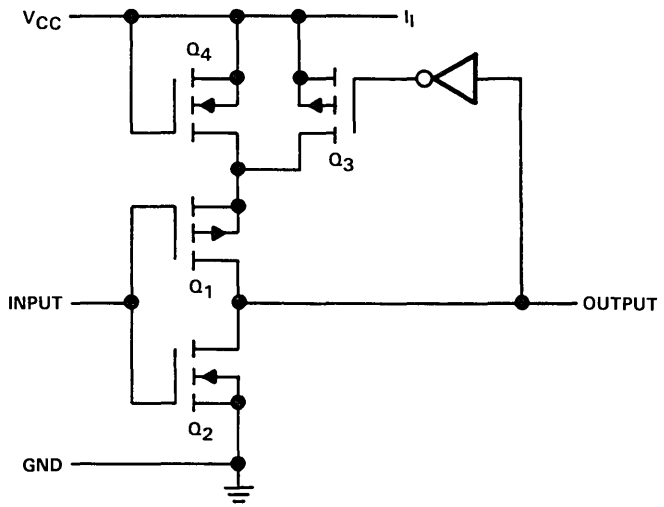


Figure 3.2-2. 54/74ACT Input Circuit

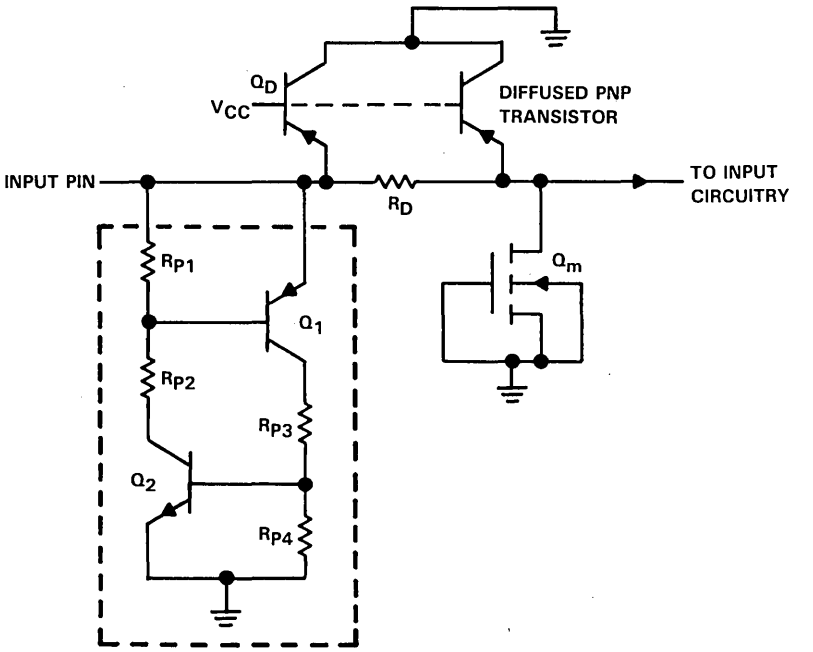


Figure 3.2-3. ESD Protection Circuit

3.2.3 Input Current and Voltage

The input current and voltage data sheet specifications are to a great extent determined by the input ESD circuitry. Positive input voltage will be clamped at about 0.7 V above V_{CC} by the base-emitter junction of the diffused PNP transistor. A negative voltage will likewise be clamped approximately 0.7 V below ground by the base-collector junction of Q_1 in the SCR input protection circuit and the NMOS transistor (Q_m).

The plot of input current versus input voltage is essentially that of a forward-biased diode as can be seen in Figure 3.2-4. This curve demonstrates that, although the JEDEC standard recommends an input voltage of between -0.5 V and V_{CC} + 0.5 V, the voltage entering the gate structure of the device will not exceed the clamp voltage. Given the clamping action of the input structure, the input current becomes the potentially damaging parameter when exceeding the absolute maximum input voltage specifications. Across the recommended input voltage range, the input current is typically under 50 nA.

Figure 3.2-5 shows the effect of temperature on input current. The maximum current level at 125 °C is considerably less than the 1 μA maximum proposed

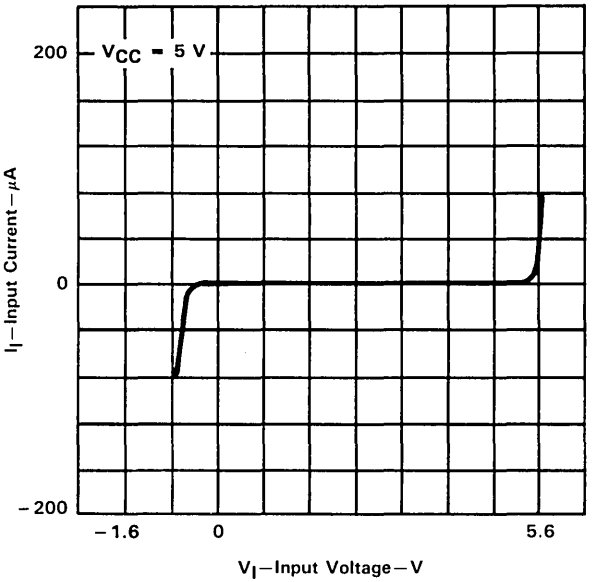


Figure 3.2-4. Input Voltage vs Input Current

by JEDEC. However, at the clamp voltage, the magnitude of the current can increase rapidly and easily reach a level harmful to the device. Texas Instruments recommends limiting maximum input current to less than 20 mA.

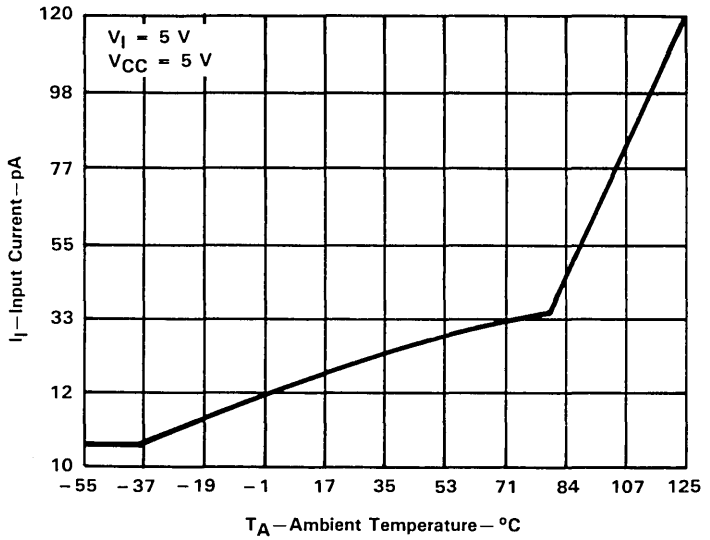


Figure 3.2-5. Input Current vs Ambient Temperature

54/74AC and 54/74ACT inputs do not have a current path from V_{CC} to GND when the input is lower than $V_{(Tn)}$ or higher than $V_{CC} - V_{(Tp)}$ where $V_{(Tn)}$ and $V_{(Tp)}$ are the threshold voltages of the N and P channel transistors. If the input voltage is between these two limits, a current will flow from V_{CC} to GND in the input stage. This can be shown by monitoring I_{CC} while sweeping the input voltage from 0.0 V to 5 V. Figure 3.2-6 and 3.2-7 show typical I_{CC} versus V_I performance for a 54/74AC and 54/74ACT input. Note the peak current flow occurs at the threshold of the input stage. This current is included in power dissipation calculations in the C_{pd} (power dissipation capacitance). The effects on power dissipation should be taken into account for devices operating in a dc mode in this region as discussed in the Power Management Summary, Section 5.4.

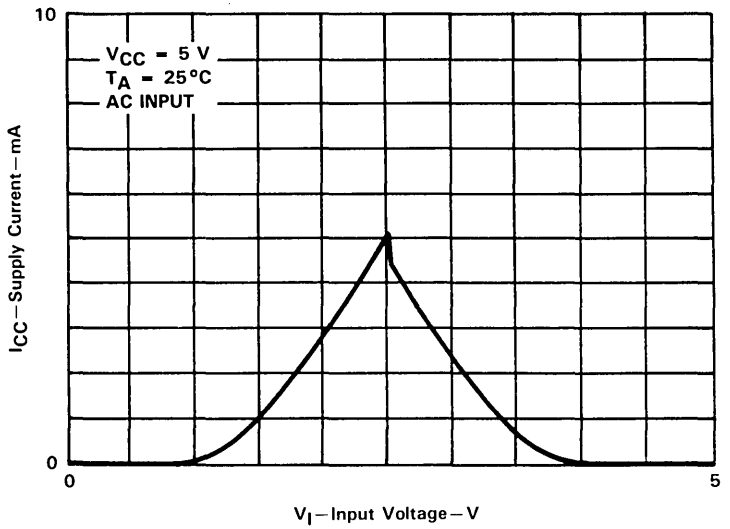


Figure 3.2-6. Input Voltage vs Supply Current

A 54/74ACT device can have a current path from V_{CC} to ground since a TTL high signal level can be typically 3.4 V. This current is reflected in the data sheet as an I_{CC} specification. This number is specified as a maximum number, as shown in Table 3.2-1, so that the system designer can properly calculate the system power requirements.

Table 3.2-1. Advanced CMOS Δ I_{CC} Specifications

PARAMETER	TEST CONDITION	SPECIFICATIONS					
		T_A = 25°C		54 SERIES		74 SERIES	
		MIN	MAX	MIN	MAX	MIN	MAX
ΔI_{CC}	V_{CC} – 2.1 V		0.9 mA		1.0 mA		1.0 mA

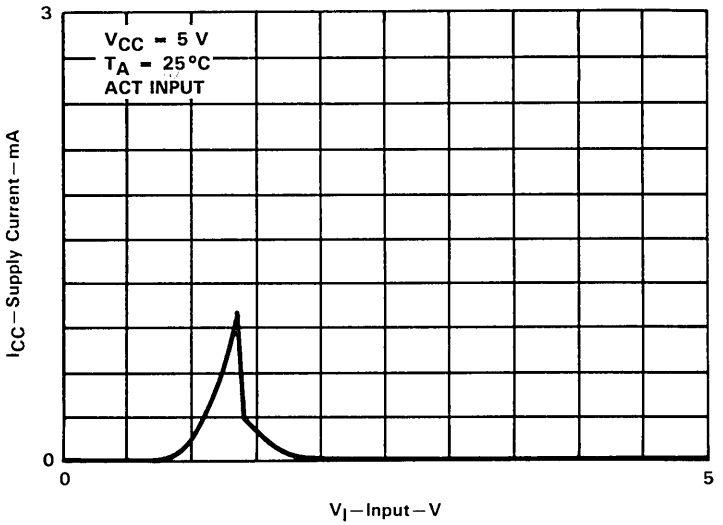


Figure 3.2-7. Input Voltage vs Supply Current

3.2.4 Proper Termination of Unused Inputs

AC/ACT devices have high-impedance inputs which must be terminated to prevent the input circuitry from floating into the linear operating region. Unused inputs not connected to V_{CC} or ground will follow any stray noise present on the pin, causing unpredictable circuit performance. Termination of unused inputs increases system reliability and minimizes power dissipation, optimizing the low-power characteristics of CMOS devices. Unused inputs can be connected to V_{CC} or ground through a 1 kΩ to 10 kΩ resistor, although this provides no advantage over directly tying the inputs to V_{CC} or ground. However, some devices in the ACL family have common I/O pins. When it is necessary to tie one of these I/O pins to V_{CC} or ground, a 10 kΩ resistor must be used. The direct connection of these pins to V_{CC} or ground could destroy the device.

3.2.5 Input Capacitance

Due to their high-impedance inputs, the AC/ACT devices draw little input current. Therefore, the limiting factor of ACL fan-out is input capacitance. Figure 3.2-8 shows a typical C_I versus V_I curve at 25 °C. The downward trend of the curve is due to the reverse bias on the input diodes in the ESD protection circuitry. The peak at the threshold voltage, $V_{CC}/2$, is due to the Miller-effect capacitance when the input inverter is in its linear region. The trend shown in Figure 3.2-8 as V_I varies remains constant for all levels of V_{CC}. However, across the operating temperature range, the capacitance can vary by as much as 0.3 pF as shown in Figure 3.2-9. A typical C_I value for 54/74AC and

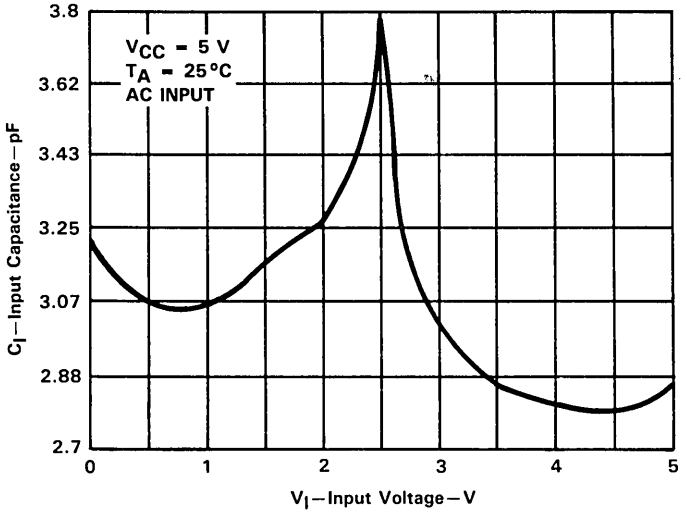


Figure 3.2-8. Input Capacitance vs Input Voltage

54/74ACT devices is 3.5 pF for the input in either a logic high or logic low state. The capacitances shown were obtained using an H-P 4191A Impedance Analyzer with a measurement frequency of 10 MHz.

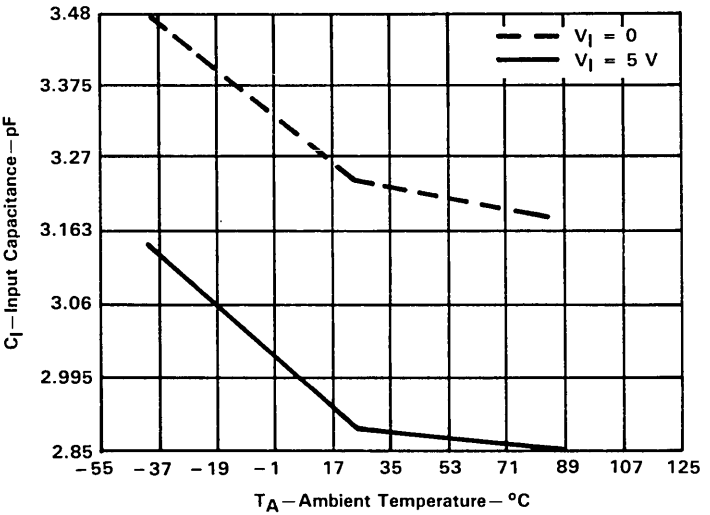


Figure 3.2-9. Input Capacitance vs Ambient Temperature

3.2.6 Summary

Texas Instruments Advanced CMOS Logic family offers CMOS and TTL-compatible input circuits which allow a designer maximum flexibility in his implementation. These two options are offered to the system designer with the benefits of low input currents, low input capacitance, and ESD protection.

3.3 Slow Input Transition Times†

3.3.1 Introduction

Advanced CMOS Logic (ACL) devices offer system designers the high-speed performance of bipolar technologies with the advantage of no quiescent power dissipation. Effective use of ACL devices requires careful system design with an awareness of the possible problems in a high-speed CMOS logic system. For example, slow input rise and fall times can cause problems in ACL systems. In order to understand how these problems may arise, as well as the solutions which can be implemented, the relationships between ACL output current transients, package inductance interactions, and on-chip recognition of input signal levels must be investigated.

The limiting factor in the speed of a CMOS integrated circuit is its ability to charge and discharge a capacitive load. Figure 3.3-1 shows a simple CMOS inverter with its output load modeled as a capacitor. The load capacitor makes instantaneous switching of logic levels impossible. For instance, the transition of the output from a high logic level to a low logic level requires the n-channel transistor to discharge the capacitor to ground. The transition of the output from a low to a high requires the p-channel transistor to charge the capacitor to the power supply voltage.

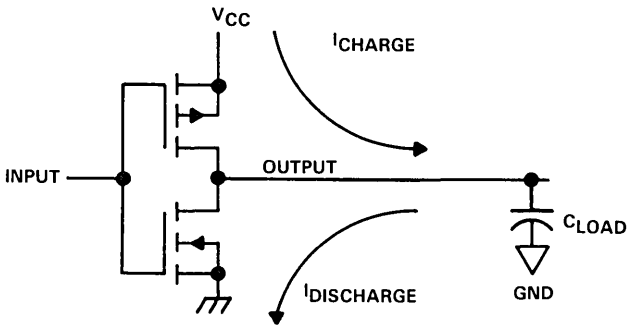


Figure 3.3-1. Simple CMOS Inverter

†Written by S. Abramson

3.3.2 Relationship Between Charge, Voltage, and Capacitance

Equation 1 describes the well-known relationship between charge, voltage, and capacitance. Differentiating both sides with respect to time yields the instantaneous relationship of charge and voltage described by Equation 2. As the capacitive load model indicates, CMOS inputs are driven by voltage rather than current. Switching speed performance is achieved, therefore, by maximizing the time rate of change of the voltage (dV/dt) across the load capacitor. The result, from Equation 2, is a maximum output current transient flowing through the integrated circuit (IC) when the output switches states.

$$Q = C \times V \tag{1}$$

where:

Q = Charge
C = Capacitance
V = Voltage

$$I = \frac{dQ}{dt} = C \times \frac{dV}{dt} \tag{2}$$

Current flow itself does not degrade performance. It is the interaction of the current flow with its physical surroundings that degrades system switching performance. The package encasing an integrated circuit has metallic leads allowing interconnection of the device to a circuit board. Each package lead and its bonding wire to the integrated circuit add inductance between the board and the integrated circuit. The output switching currents flow through these leads to the power supply and ground nodes causing inductive voltage spikes.

The relationship between the current transients and the inductive voltage at the node is defined by Equation 3. Texas Instruments has minimized the factor of lead inductance by locating the power and ground pins at the center of the integrated circuit package. However, large current transients at these nodes can still induce a voltage large enough to cause problems for input signals with slowly changing edges.

$$V_i = -L \times \frac{dI}{dt} \tag{3}$$

where:

L = Package inductance to reference node (V_{CC} or ground)
I = Current through reference node
V_i = Induced voltage at the reference node

Since the power supply and ground nodes are used as voltage references throughout an integrated circuit, these inductive voltage spikes affect the way signals appear to the internal gate structures. For instance, if the voltage at the ground node rises, the input signal will appear to decrease in magnitude. A slowly rising input causes the device to switch as it exceeds the input voltage threshold. If the output current transients cause a large enough inductive voltage spike on the ground node, the slowly rising input may appear to be driven back through the threshold. If worst-case conditions prevail, the slowly rising input will be repeatedly driven back through the threshold, resulting in output oscillation.

Worst-case conditions for slow input transition times are those that induce the largest magnitude of noise on the power nodes. The following three conditions will produce the worst-case performance for ACL systems incorporating slowly changing input signals.

1. Simultaneously switching all gates will produce the largest magnitude of output current transients.

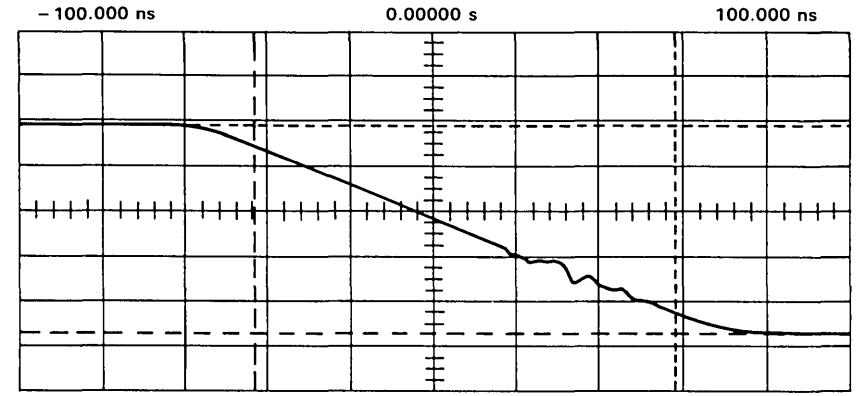
2. Maximum V_{CC} requires the largest voltage swing, maximizing dV/dt.

3. Minimum temperature ($-55\,°C$) operation increases output transistor performance, maximizing current transients and dV/dt.

A competitor's AC244, in its end-power-pinned package, subjected to a 100-ns falling edge with eight gates switching simultaneously is shown in Figure 3.3-2. Ambient temperature was 25 °C and V_{CC} was 4.5 V. Though not worst case, these conditions caused enough noise on the ground node to drive the low-going input back through the threshold once. The result was a 3.64-V glitch on the output. With an effective pulse width of 3.6 ns, the glitch may be interpreted as data in the next stage of the system.

Figure 3.3-3 displays the effects of increasing V_{CC} at the same ambient temperature of 25 °C. The output now contains two glitches and the pulse width of the first one has grown to 4.4 ns. The probability of an erroneous signal being introduced from a slowly changing input has increased significantly with increasing V_{CC}.

Worst-case conditions occur at ambient temperature of $-55\,°C$, supply voltage of 5.5 V, and eight gates switching at the same time. The output of a competitor's AC244 subjected to these conditions with an input falling edge rate of 100 ns is displayed in Figure 3.3-4. Incorporating a slowly changing input signal into an ACL system under these conditions would certainly introduce erroneous signal propagations throughout the system. Even at faster edge rates of 75 ns, as shown in Figure 3.3-5, it is probable that false signals will arise from the output perturbations.

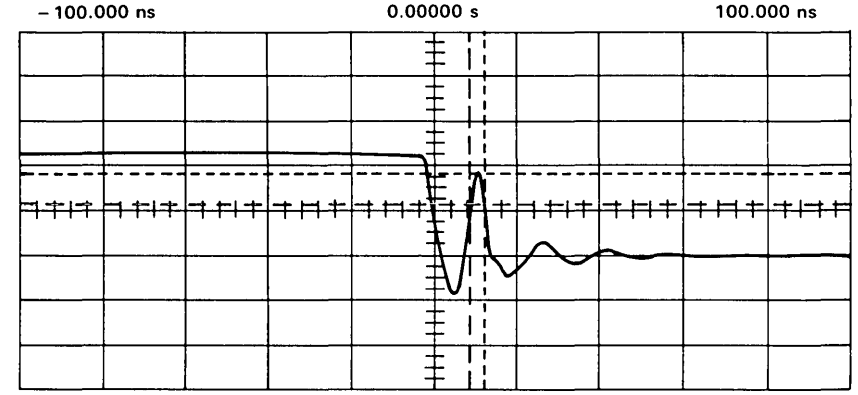


CH. 2 = 1.000 V/div
Timebase = 20.0 ns/div
Ch. 2 Parameters
Overshoot = 0.000 V

t_f = 101.490 ns
P-P V = 4.656 V
V_{CC} = 4.5 V, T_A = 25°C

Offset = 2.660 V
Delay = 0.00000 s
Preshoot = 31.25 mV

a. Input



Ch. 1 = 2.000 V/div
Timebase = 20.0 ns/div
Start = 8.400 ns
Vmarker1 = 2.240 V

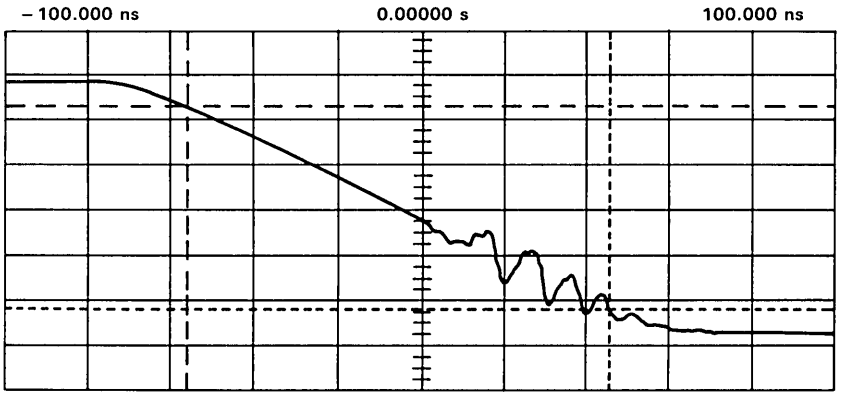
Stop = 12.000 ns
Vmarker2 = 3.640 V

Offset = 2.000 V
Delay = 0.00000 s
ΔT = 3.6000 ns
Δ V = 1.400 V

t_r, t_f = 100 ns, V_{CC} = 4.5 V, T_A = 25°C

b. Output

Figure 3.3-2. Competitor AC244 Subjected to 100-ns Falling Edge with Eight Gates Switching Simultaneously

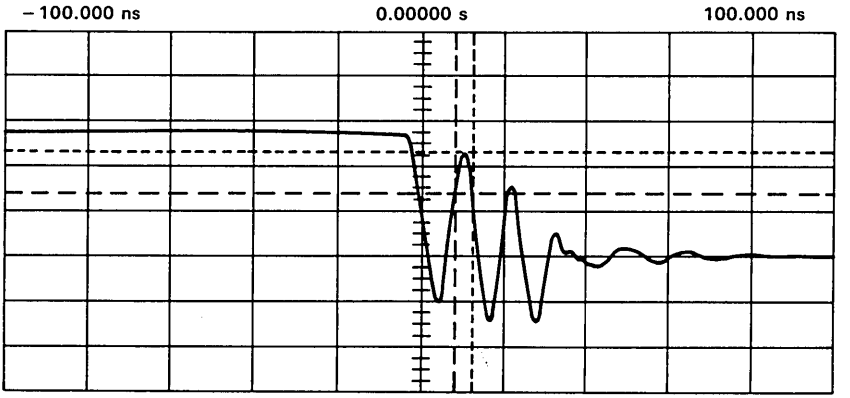


Ch. 2 = 1.000 V/div
Timebase = 20.0 ns/div
Ch. 2 Parameters
Overshoot = 0.000 V

t_f = 102.220 ns
P-P V = 5.625 V
V_{CC} = 5.5 V, T_A = 25°C

Offset = 2.660 V
Delay = 0.00000 s
Preshoot = 31.25 mV

a. Input



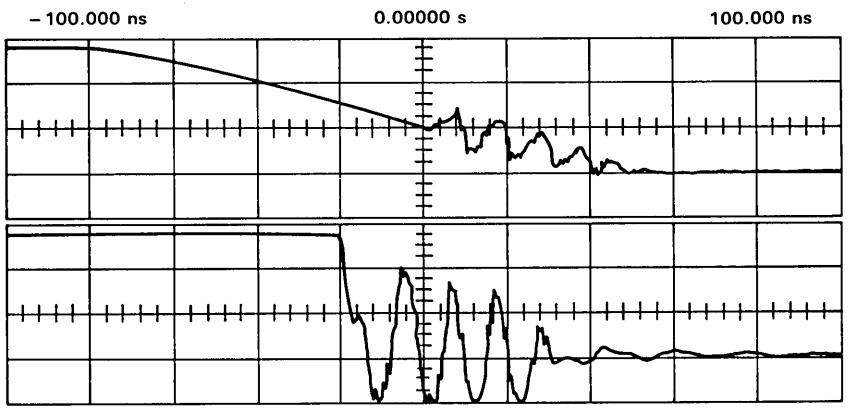
Ch. 1 = 2.000 V/div
Timebase = 20.0 ns/div
Start = 8.000 ns
Vmarker1 = 2.760 V

Stop = 12.400 ns
Vmarker2 = 3.640 V
t_r, t_f = 100 ns
V_{CC} = 5.5 V, T_A = 25°C

Offset = 2.000 V
Delay = 0.00000 s
ΔT = 4.400 ns
Δ V = 1.840 V

b. Output

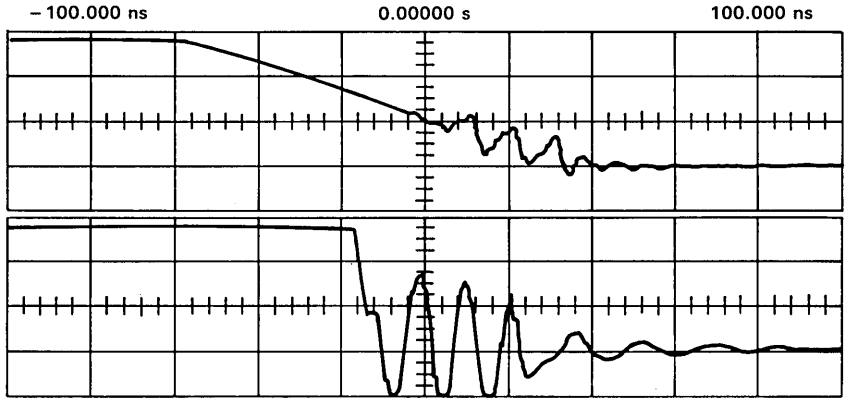
Figure 3.3-3. Competitor AC244 Subjected to 100-ns Falling Edge with Eight Gates Switching Simultaneously



Ch. 1 = 2.000 V/div Offset = 2.000 V
Ch. 2 = 2.000 V/div Offset = 2.000 V
Timebase = 20.0 ns/div Delay = 0.00000 s

t_r, t_f = 100 ns, V_{CC} = 5.5 V, T_A = –55°C

Figure 3.3-4. Competitor AC244 Subjected to 100-ns Falling Edge with Eight Gates Switching Simultaneously



Ch. 1 = 2.000 V/div Offset = 2.000 V
Ch. 2 = 2.000 V/div Offset = 2.000 V
Timebase = 20.0 ns/div Delay = 0.00000 s

t_r, t_f = 75 ns, V_{CC} = –5.5 V, T_A = –55°C

Figure 3.3-5. Competitor AC244 Subjected to 75-ns Falling Edge with Eight Gates Switching Simultaneously

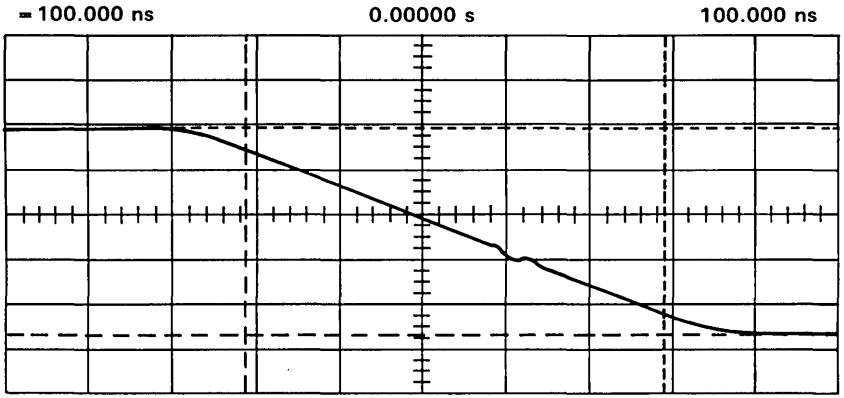
Traditionally, hysteresis has been used to counter the voltage variations of the input signal due to inductive voltage spikes on the reference nodes of the integrated circuit. In these circuits, a single input voltage threshold is not used. Rather, the input signal may vary over a set voltage range before it is recognized as a signal of the opposite logic polarity. Typically, input voltages are allowed to vary over a 100-mV to 800-mV range in hysteresis circuits. However, with high-speed integrated circuits, the inductive voltage spikes on the power supply and ground nodes can easily exceed a reasonable voltage threshold range.

3.3.3 Dynamic Hysteresis

In order to offer superior performance in applications that require incorporation of signals with slow transition times, Texas Instruments and Philips/Signetics have developed dynamic hysteresis and an innovative output structure for implementation in the EPIC™ ACL family. While the patented output edge control structures minimize the magnitude of inductive voltages at the power and ground nodes, the patented dynamic hysteresis circuit latches the input signal in input stages until these inductive voltages have subsided.

The dynamic hysteresis circuit triggers as the input is switched and provides a large amount of hysteresis. This hysteresis moves the threshold far enough that noise on the power or ground nodes will not cause the first stage of the gate to switch. After the noise on the ground or power node has sufficiently died away, the hysteresis is removed, and the gate is allowed to switch.

The complementing effects of Texas Instruments output edge control and input transition control, through dynamic hysteresis, are displayed in Figures 3.3-6, 3.3-7, 3.3-8, and 3.3-9. The Texas Instruments AC11244 was subjected to exactly the same conditions as the competitor end-power pin AC244. Superior performance is achieved even with worst-case conditions displayed in Figure 3.3-8.

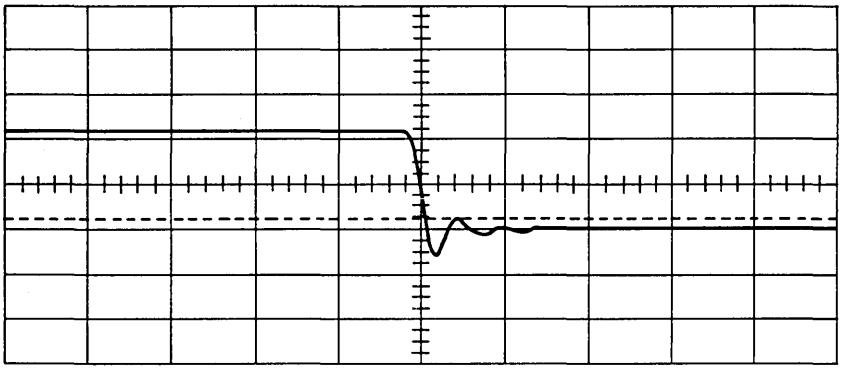


Ch. 2 = 1.000 V/div
Timebase = 20.0 ns/div
Ch. 2 Parameters
Overshoot = 0.000 V

t_f = 101.280 ns
P-P V = 4.656 V
V_{CC} = 4.5 V, T_A = 25°C

Offset = 2.660 V
Delay = 0.00000 s
Preshoot = 31.25 mV

a. Input



Ch. 1 = 2.000 V/div
Timebase = 20.0 ns/div
Vmarker1 = 2.240 V

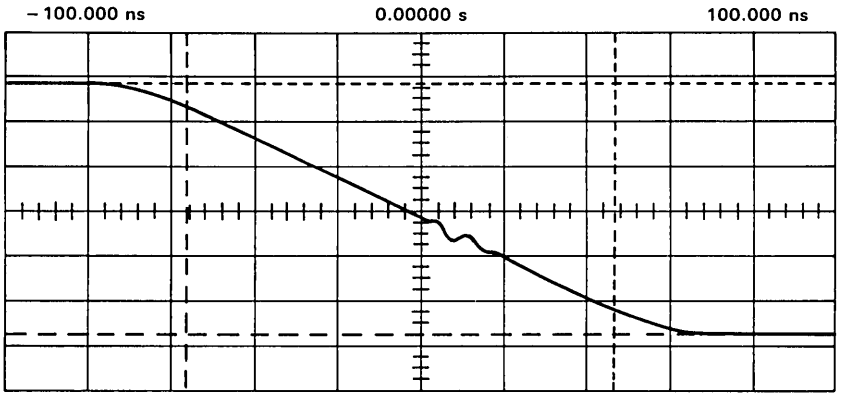
Vmarker2 = 440 mV

Offset = 2.000 V
Delay = 0.00000 s
ΔV = 1.400 V

t_r, t_f = 100 ns, V_{CC} = 4.5 V, T_A = 25°C

b. Output

Figure 3.3-6. Texas Instruments AC11244 Subjected to 100-ns Falling Edge with Eight Gates Switching Simultaneously

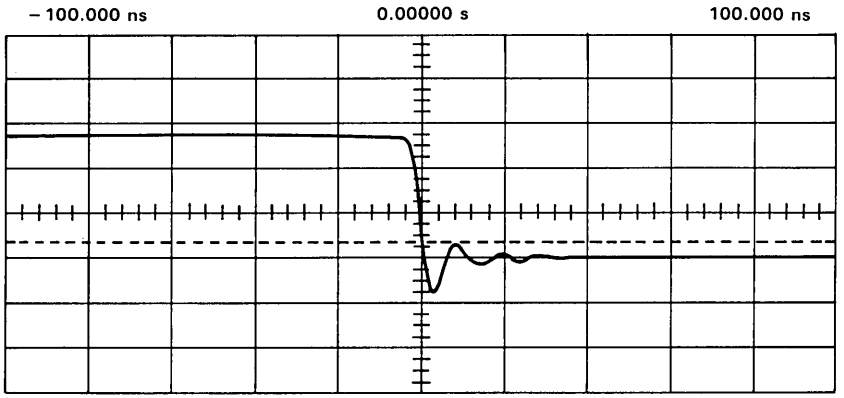


Ch. 2 = 1.000 V/div
Timebase = 20.0 ns/div
Ch. 2 Parameters
Overshoot = 0.000 V

t_f = 103.210 ns
P-P V = 5.625 V
V_{CC} = 5.5 V, T_A = 25°C

Offset = 2.660 V
Delay = 0.00000 s
Preshoot = 0.000 mV

a. Input



Ch. 1 = 2.000 V/div
Timebase = 20.0 ns/div
Vmarker1 = 0.000 V

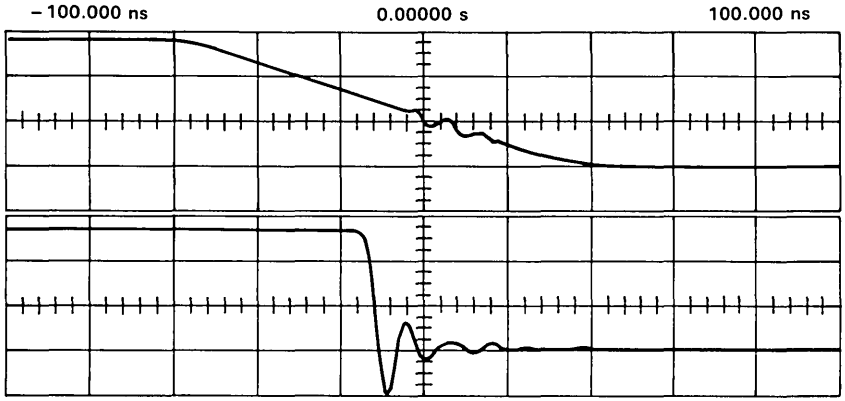
Vmarker2 = 680 mV

t_r, t_f = 100 ns, V_{CC} = 5.5 V, T_A = 25°C

Offset = 2.000 V
Delay = 0.00000 s
Δ V = 680 mV

b. Output

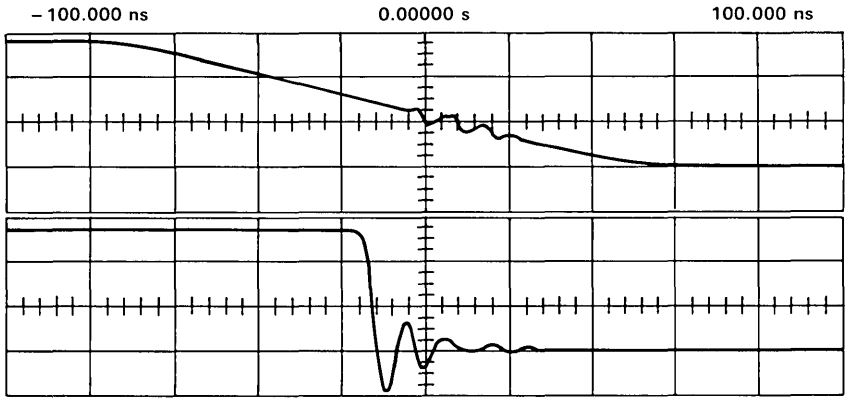
Figure 3.3-7. Texas Instruments AC11244 Subjected to 100-ns Falling Edge with Eight Gates Switching Simultaneously



Ch. 1 = 2.000 V/div Offset = 2.000 V
Ch. 2 = 2.000 V/div Offset = 2.000 V
Timebase = 20.0 ns/div Delay = 0.00000 s

t_r, t_f = 100 ns, V_{CC} = 5.5 V, T_A = −55°C

Figure 3.3-8. Texas Instruments AC11244 Subjected to 100-ns Falling Edge with Eight Gates Switching Simultaneously



Ch. 1 = 2.000 V/div Offset = 2.000 V
Ch. 2 = 2.000 V/div Offset = 2.000 V
Timebase = 20.0 ns/div Delay = 0.00000 s

t_r, t_f = 75-ns, V_{CC} = 5.5 V, T_A = −55°C

Figure 3.3-9. Texas Instruments AC11244 Subjected to 75-ns Falling Edge with Eight Gates Switching Simultaneously

3.3.4 Summary

As integrated circuit speeds increase with diminishing silicon geometries, problems with on-chip noise must be addressed. System designers must be made aware of these problems so that intelligent board layout and device selection will result in reliable end products. Texas Instruments is addressing these problems through innovation. Specifically, the EPIC™ ACL family of devices is offered in a center-power-pinned package commonly found in high-speed ECL systems. Innovative input and output structures provide increased immunity to inductive noise on the power nodes. Through implementation of these innovations, the EPIC™ ACL family of devices offers superior performance in systems that require incorporation of slowly changing input signals.

3.4 Metastable Characteristics†

3.4.1 Introduction

Familiar to every system designer is the problem of synchronizing two digital signals operating at different frequencies. This problem is typically solved by synchronizing one of the signals to the local clock through a flip-flop. However, this solution presents an awkward trade-off; the designer cannot guarantee the setup and hold-time specifications associated with the flip-flop will not be violated. The reaction of a flip-flop under this potential metastable condition influences the overall system reliability. This section gives the system designer a better understanding of the metastable characteristics pertaining to Texas Instruments Advanced CMOS Logic (ACL) Family.

3.4.2 Metastable Definition

When the setup or hold time of the flip-flop is violated, the device output response is uncertain. Presently, there is no circuit that can guarantee its reliable operation under this condition. The metastable state is defined as that time period when the output of a logic device is not at a logic level 1 (V_{OUT} greater than 70% of V_{CC} for CMOS), nor at a logic level 0 (V_{OUT} less than 30% of V_{CC} for CMOS), but instead is between 30% and 70% of V_{CC}. Since the input data is changing while it is being clocked, the system designer does not care if the flip-flop goes to either a high- or low-logic level, as long as the output does not hang up in the metastable region. The metastable characteristics for a particular flip-flop will determine how long the device stays in the metastable region. This concept is illustrated in the timing diagram of Figure 3.4-1.

†Written by R. Breuninger, M. Higgs, and R. Schwartz.

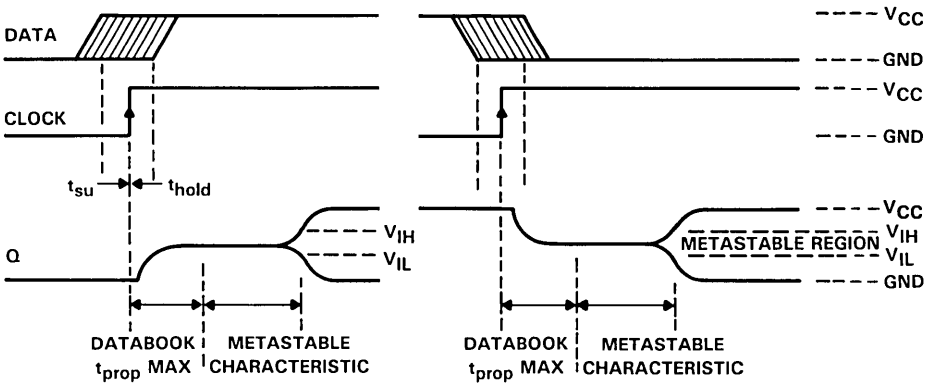


Figure 3.4-1. Metastable Timing Diagram

3.4.3 Metastable Evaluation

Evaluating the metastable characteristics for a particular flip-flop is not an easy task. The number of times that the output hangs up in the metastable region is extremely small compared to the total number of clock transitions that occur. In addition, the amount of time that the output actually spends in the metastable region varies depending on the technology in which the flip-flop is being implemented.

From a system-engineering standpoint, a designer cannot use the specified data sheet maximum for propagation delay when using the flip-flop as a data synchronizer. Instead, one needs to know how long to wait after the specified data sheet maximum before using the data to guarantee reliable system operation. Specifically, the designer needs to know for a certain Δt, the wait time between the clocking of the flip-flop and the time when the output, Q, will be considered valid, what will be the expected Mean Time Between Failures (MTBF).

Conventional test equipment is not designed to measure these parameters. A special test circuit has been developed for measuring MTBF and Δt. By formulating representative values for these two parameters through experimental evaluation, the system designer can make a rational decision about what type of flip-flop to use and how long to wait before using the data.

3.4.4 Circuit Description

The circuit in Figure 3.4-2 can be used to evaluate a flip-flop MTBF for a specific Δt. Two AD9685 voltage comparators are used to detect when the Q output of the device under test (DUT) is in the metastable state. This is

accomplished by comparing the output to both V_{IL} and V_{IH}. When the output voltage from the DUT is between V_{IL} and V_{IH} (in the metastable region), the comparators will be in opposite states. The outputs of the AD9685s are clocked (CBUS.CLK2) into an MC10131 at a specific Δt after the active edge of the DUT clock (CBUS.CLK1). Then the outputs of the MC10131 are exclusive-ORed through an 'ALS86 and clocked (CBUS.CLK3) into an 'AS74 flip-flop.

To maximize the possibility of forcing the DUT into a metastable state, the input signal must occur within a window defined by the setup and hold specifications of the DUT — the "jitter" window. The width of the "jitter" window should not exceed the setup-time plus the hold-time specification for the device.

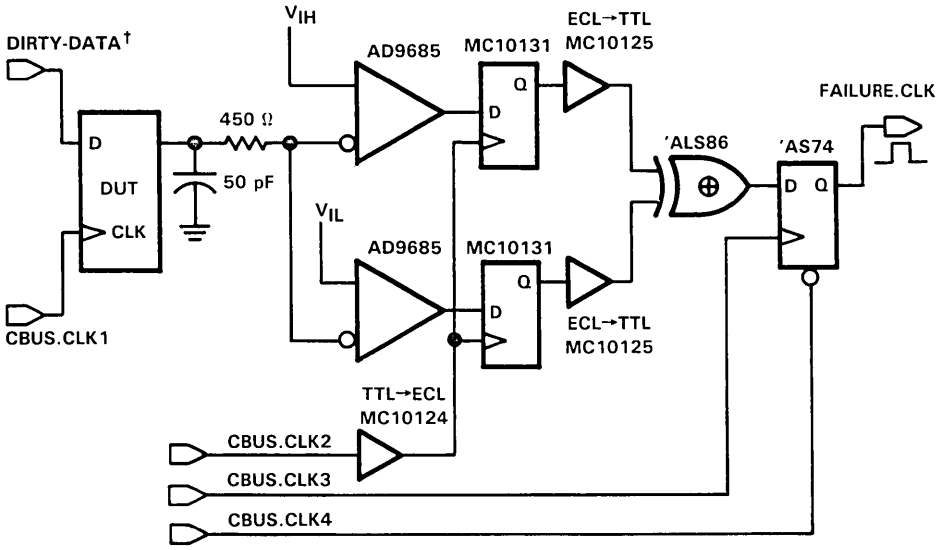


Figure 3.4-2. Metastable Evaluation Test Circuit Schematic

The worst-case condition occurs when the input data always violates the data setup and hold times. This relationship is shown in the timing diagram in Figure 3.4-3. Any other relationship of CBUS.CLK1 and DIRTY-DATA† will reduce the chances of setting up a metastable state in the flip-flop. Therefore, the worst-case condition for a given input data frequency will be one-half the DUT clock rate and in phase with the clock. By using this test circuit, the MTBF can be determined for several different Δt. Plotting this data on a semilog coordinate system shows the metastable characteristics of the flip-flop at the input data frequency that was used.

†Also may be known as "jitter."

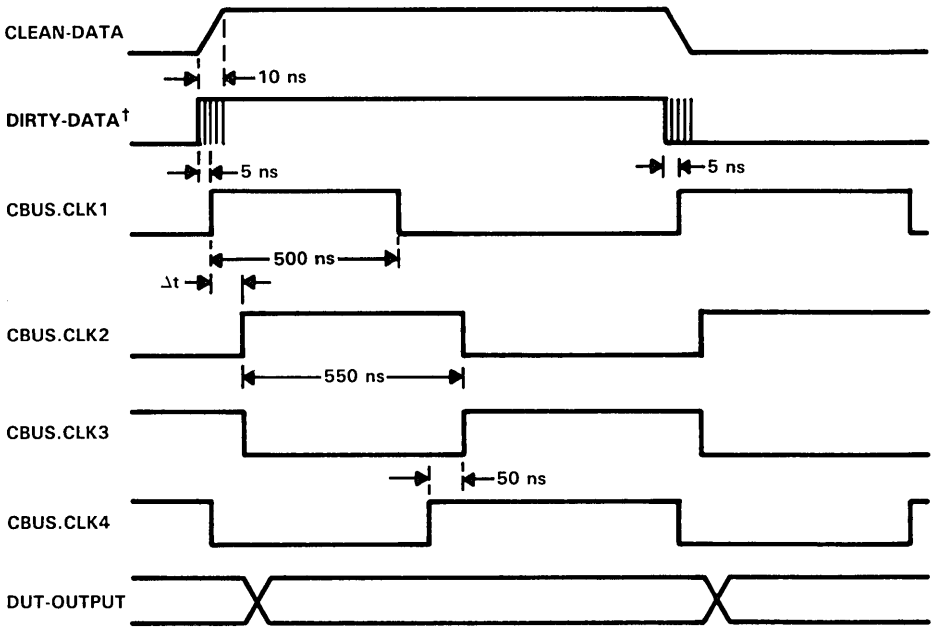


Figure 3.4-3. Metastable Timing Diagram

3.4.5 Test Circuit Limitations

Two factors considerably affect the accuracy of the results produced by the test circuit described above: the centering of the input data "jitter" around the input clock and the propagation delay of the AD9685 voltage comparators. If the "jitter" is not centered around the input clock, the probability of entering the metastable state is reduced, producing conditions which are not worst case.

The propagation delay of the voltage comparators adds a delay between the output of the DUT and the clocking of the data into the MC10131's after Δt. This causes a problem if the output of the DUT comes out of the metastable state, but the comparator outputs do not switch until after CBUS.CLK2 has clocked. The test circuit will record a failure when, in reality, the DUT came out of the metastable region before Δt. In addition, there must be an allowance for line propagation delays. The test results take these additional delays into account by subtracting their total delay from the Δt that was recorded. The delays for each part of the test circuit are shown in Figure 3.4-4.

†Also may be known as "jitter.

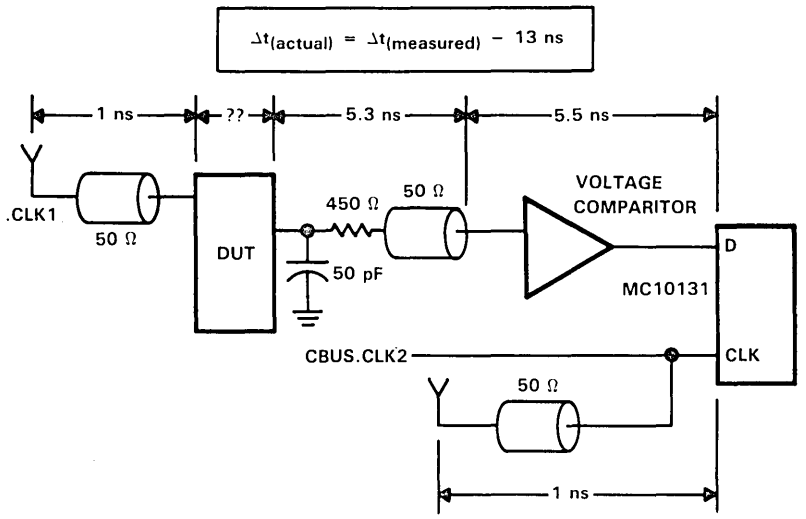


Figure 3.4-4. Metastable Evaluation Test Circuit — Internal Delays

3.4.6 The Metastability Equation

From the metastability graph, we can develop a MTBF equation as follows. If we assume a linear function on the semilog plot, the equation for the MTBF line is:

$$\log (\text{MTBF}) = a\Delta t + b$$

If the log base ℓ is converted to that of natural logs, the equation becomes:

$$\ln (\text{MTBF}) = a\Delta t + b$$

where a and b are new constants. Solving for MTBF yields:

$$\text{MTBF} = e^{(a\Delta t + b)}$$

or...

$$\text{MTBF} = Be^{A\Delta t}$$

or...

$$\frac{1}{\text{MTBF}} = Be^{-A\Delta t}$$

As the exponent Δt gets very small, the MTBF approaches its minimum B. The minimum MTBF occurs when a fail is present at every active edge of the DUT CLK. Thus, the constant B is a function of the frequency of the DUT CLK, f_{cp}; that is, CBUS.CLK1, as well as the frequency of the DUT DATA, f_{data}, the jitter window, and the alignment of the two signals. If the DUT is clocked at 1 MHz, the minimum MTBF will be 1 μs. Here it is assumed that the conditions for failure are present at every active edge of the CLK. That is, every edge of DIRTY-DATA is aligned with every active edge of CBUS.CLK. Refer to Figure 3.4-3.

In general, the presence of a jitter window will not ensure a failure. A failure will only occur when this environment is present and the DUT is sensitive to the environment (a device- or device-technology-dependent parameter). Thus the constant B can be modeled as follows,

$$B = C1 \times f_{data} \times f_{cp} \text{ (fails/second)}$$

where C1 is a function of the device technology of the DUT, f_{data} is the frequency at which the jitter window is present, and f_{cp} is the frequency at which the DUT is sampling data.

Finally, the constant A corresponds to the slope of the MTBF graph. It is a function of the technology as well. If we replace A with C2, the final metastability equation becomes:

$$\frac{1}{MTBF} = C1 \times f_{data} \times f_{cp} \times e^{-C2\Delta t}$$

3.4.7 Metastability Test Results

As stated earlier, the worst-case condition for the test circuit shown in Figure 3.4-2 occurs when the data setup and hold time is always violated. This occurs when the input data frequency is 0.5 times the DUT clock frequency. Therefore, the worst-case metastability equation can be written as:

$$\frac{1}{MTBF} = \tfrac{1}{2} f_{cp}^2 \times C1\, e^{(-C2\ \Delta t)}$$

The constants C1 and C2 describe the metastable characteristics of the device. From the experimental data graphs in Figure 3.4-5, these constants can be determined for each device family. As an example, the constants are solved below for the AC11074.

C2 is defined by the slope of the line. Picking two data points off the graph yields the following result. Multiplying by 2.302 converts the base of the logs from 10 to e.

$$C2 = \frac{\log 10^6 - \log 10^0}{15.63 - 10.95}(2.302) = \frac{6}{4.68}(2.302) = 2.95\ \text{sec}^{-1}$$

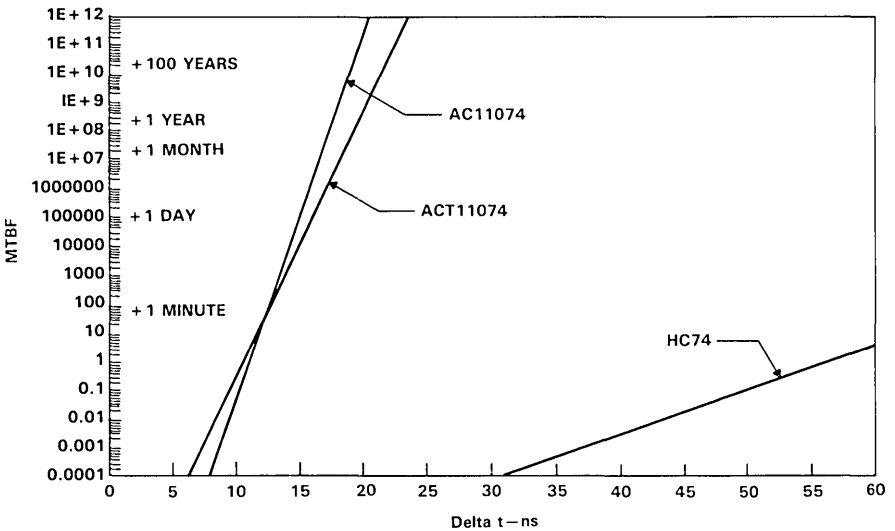


Figure 3.4-5. AC11074, ACT11074A, and HC74 Metastability Performance

By plugging C2 into the equation and using a data-point off the graph, C1 can be computed as follows:

$$\frac{1}{MTBF} = \tfrac{1}{2} f_{cp}^2 \times C1\, e^{(-2.95\,\Delta t)}$$

$$\frac{1}{1} = \tfrac{1}{2} (10^6)^2 \times C1\, e^{(-2.95 \times 10.95)}$$

$$C1 = 2.13 \times 10^2$$

Inserting C1 and C2 into the equation yields the metastable equation for the AC11074.

$$\frac{1}{MTBF} = \tfrac{1}{2} f_{cp}^2 \times 2.13 \times 10^2\, e^{(-2.95\,\Delta t)}$$

The metastability equations for the ACT11074 and the HC74 can be derived using the same procedure.

For ACT11074:

$$\frac{1}{MTBF} = \tfrac{1}{2} f_{cp}^2 \times 1.42 \times 10^{-2}\, e^{(-2.13\,\Delta t)}$$

For HC74:

$$\frac{1}{MTBF} = \tfrac{1}{2} f_{cp}^2 \times 2.19 \times 10^{-8}\, e^{(-0.161\,\Delta t)}$$

Given this worst-case equation, the system designer can determine the metastable characteristics for Texas Instruments ACL when using other input clock frequencies.

Also, for any given clock frequency, the designer can determine how long a wait state must be allotted to ensure reliable system performance under a condition conducive to metastability. When the designer considers how this test under constant metastable conditions relates to the metastable potential of the system being designed, an adequate MTBF can be determined for the particular system being developed. A designer can use this MTBF and, consulting either the metastability graph or the metastability equation, determine the needed Δt.

3.4.8 Summary

The metastable characteristics of a flip-flop used for data synchronization can greatly affect system reliability. Based on the information presented in this section, the system designer can make a rational decision about what type of flip-flop to use and what its metastable characteristics will be. The selection of what type of flip-flop to use must be based on the speed of the application. As a general rule, the faster the flip-flop, the better its metastable characteristics.

The graphs shown and equations derived represent a reasonable assumption about the metastable characteristics for Texas Instruments ACL family. However, it is strongly recommended that, when using flip-flops as data synchronizers, an adequate amount of guardband be allowed beyond the characteristics shown before sampling the output.

4 Device Testing and Evaluation

4.1 Simultaneous Switching Considerations†

4.1.1 Abstract

This section provides an understanding of the potential problems of multiple outputs switching and develops a standardized methodology for the evaluation of simultaneous switching. The effects of simultaneoulsy switching outputs on a multiple output device are examined from an historical point of reference as well as from a first order theoretical evaluation of the phenomena. The impact of several system parameters is evaluated for their effect upon the simultaneous switching performance of a CMOS logic device. A standardized test methodology for the evaluation of simultaneous switching effects is presented in Section 4.1.6.4. Section 4.1.6.6 provides a parts and vendor list for Texas Instruments ACL characterization boards. The results of this section are presented to assist the end user of ACL (Advanced CMOS Logic) devices in evaluating simultaneous switching effects.

4.1.2 Introduction

TTL and CMOS logic devices have evolved with decreases in geometries, power dissipation, and propagation delay. This evolution has allowed the system designer to develop end equipment with more functionality per unit volume as well as systems that solve increasingly complex problems. The benefits resulting from this technological evolution have been accompanied with some undesired results. As logic devices have become faster, output edge rates have increased from 5 ns/V to 1 ns/V. These faster slew rates can amplify system problems such as reflections on transmission lines, crosstalk between adjacent signal paths, and power supply noise.

The system engineer skilled in the art of high-speed logic design is aware of the system implications of higher switching speeds as well as the effect of switching multiple outputs simultaneously on a single device. The consequences of simultaneous switching include self-induced noise on inactive outputs, loss of data, and propagation delay degradation. These phenomena are found to some degree in all high-speed logic families. The 74ALS, 74F, and 74AS logic families were the first bipolar families in which simultaneous switching noise became a major issue. System design engineers developed techniques to deal with the levels of switching noise, typically 1.1-V glitches for octal devices, generated by this class of product.

† Written by S. Abramson, C. Hefner, and D. Powers.

Historically, CMOS logic has been somewhat immune to this class of problems since the state of the technology limited output drive and propagation delays. With the introduction of sub 2-μm gate lengths, CMOS logic devices are now capable of propagation delays and output drive levels equivalent to advanced bipolar logic devices, such as 74ALS and 74F. These performance levels place Advanced CMOS Logic (ACL) in the high-speed logic arena and have caused significant simultaneous switching noise problems for end-pin ACL devices. Figure 4.1-1 shows the level of simultaneous switching noise obtained for standard circuit design and packaging techniques.

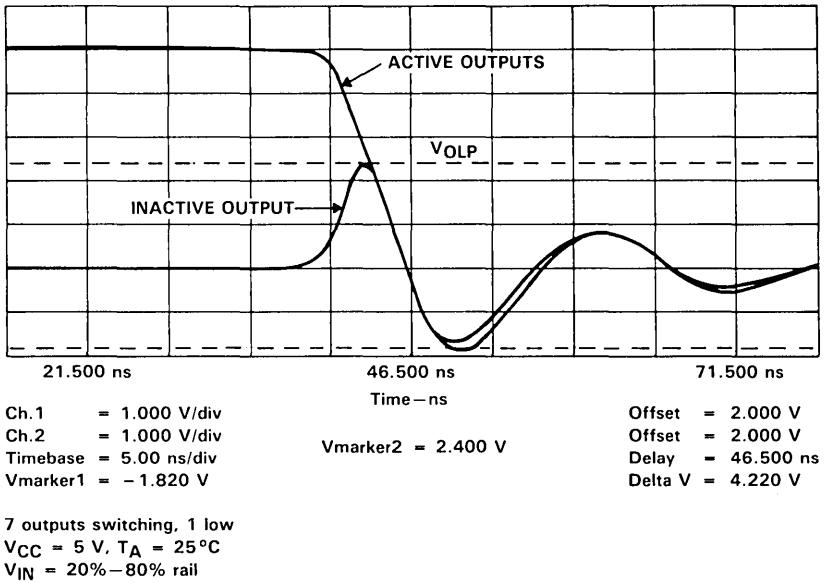


Figure 4.1-1. End-Pin Simultaneous Switching Noise Waveform

4.1.3 Simultaneous Switching Phenomenon

All CMOS logic devices operate by either charging or discharging capacitive loads. The load capacitor makes the instantaneous switching of logic levels impossible. This becomes apparent when one considers the MOS transistor has a finite "on" resistance through its conducting channel. Without the package parasitic inductance, an output structure for a single logic high to logic low transition can be modeled as an RC network as shown in Figure 4.1-2.

EPIC is a trademark of Texas Instruments Incorporated.

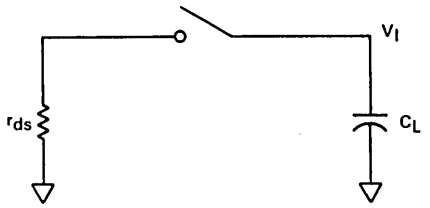


Figure 4.1-2. RC Model of a CMOS Output for the High-to-Low Transition

The value of the resistor is determined by the size of the output transistor. EPIC™ (Enhanced Performance Implanted CMOS) ACL output structures are optimized to drive capacitive loads of 50-pF and transmission lines of impedances less than 50 Ω. Not only are these outputs designed to enhance ac switching performance for capacitive loads and low-impedance lines, but they are designed to provide dc currents for CMOS and TTL loads. This optimization determines the output transistor sizing and yields values of channel resistance of 8 Ω to 12 Ω.

The current that flows in the circuit shown in Figure 4.1-2 can be modeled as Equation 1 which describes the relationship of current and voltage for a capacitor.

$$i = \frac{dq}{dt} = C\frac{dv}{dt} \qquad (1)$$

Considering the on resistance of the MOS transistor as shown in Figure 4.1-2 and solving for the charging/discharging current leads to the following relationship.

$$i = \frac{V_i}{r_{ds}} e^{-\frac{t}{r_{ds}C}} \qquad (2)$$

where

r = on resistance of the transistor
C = load capacitance
V_i = initial voltage on the capacitor at time zero (typically a V_{OH} or V_{OL})

The current flow and the interaction of this current with package parasitic impedances are the determining factors in the performance degradation observed when several outputs are switched simultaneously on a multiple output device. The package parasitics that affect device performance to the largest extent are the self and mutual inductances associated with each package lead and bond wire. For a pair of simple parallel conductors, the values for self and mutual inductance can be obtained from Equations 3 and 4.[1]

$$L_i = \frac{\ell}{I}\int_o^{\rho} B_\theta \left(\frac{r}{\rho}\right)^2 dr = \frac{\mu\ell}{8\pi} \quad (3)$$

$$M = \frac{\wedge}{I} = 5\ell\left[\ell n\left(\frac{\ell}{d} + \sqrt{1+\left(\frac{\ell}{d}\right)^2}\right) - \sqrt{1+\left(\frac{d}{\ell}\right)^2} + \frac{d}{\ell}\right] nh \quad (4)$$

Through the remainder of this section, the term inductance will refer to the total inductance on the pin; i.e., the sum of the self and mutual inductances. The output transient currents flow through these inductances between the Printed Circuit Board (PCB) V_{CC} and ground nodes, causing inductive voltage spikes on the silicon die.

The relationship between transient currents and the voltage induced on an inductor is defined in Equation 5. Using the time derivative of i from Equation 1 yields Equation 6, while using the time derivative of Equation 2 generates the equivalent expression in Equation 7.

$$V_L = -L\frac{di}{dt} \quad (5)$$

$$V_L = -L\,C\frac{d^2V_i}{dt^2} \quad (6)$$

$$V_L = \frac{V_i L}{r^2_{ds}C}\, e^{-\frac{t}{r_{ds}C}} \quad (7)$$

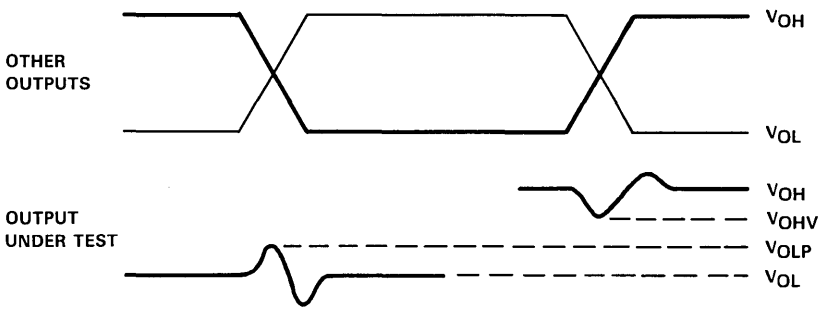
where

V_L = voltage induced upon the silicon die
L = total inductance on the pin
r = on resistance of the transistor
C = load capacitance
V_i = initial voltage on the capacitor at time zero (typically a V_{OH} or V_{OL})
d^2V/dt^2 = change in the slope of the transition edge

By inspection, it can be seen that the current that flows when N outputs are switched simultaneously is N times Equation 2. This relationship will hold true until the device begins to limit the transient current flow. As the above equations indicate, the induced voltage varies linearly with the total inductance on the pin. For this reason, the elimination of sockets and any other inductive components is required when using ACL devices. Texas Instruments has taken several steps to reduce the effects of simultaneous switching. In order to reduce the inductance term in Equations 5 through 7, Texas Instruments has introduced the EPIC™ ACL family in a center-pin package. This packaging

scheme reduces parasitic ground and power pin inductances by placing the ground and V_{CC} pins in the center of the package. Outputs are positioned around the ground pins to minimize the effective inductance of the outputs to ground and to provide a flow-through architecture. Texas Instruments has also introduced an innovative patent-pending Output Edge Control (OEC™) circuitry which essentially rounds off the upper and lower portions of the output edge while maintaining the rapid transition through the threshold region. The OEC™ is composed of several small transistors which turn on or off in rapid succession. Rounding the upper and lower edges reduces the change in the slope of the output edge which directly reduces the induced voltage of Equation 6. For a more detailed description of the OEC™ circuitry, see section 3.1.

Texas Instruments has taken these measures to improve the reliability of systems utilizing ACL devices. The implementation of center-pin power and ground, along with the OEC™, reduces the noise due to simultaneous switching and, therefore, the effort required for a system designer to implement ACL. The voltage induced on a quiescent pin during simultaneous switching will be referred to as V_{OLP} or V_{OHV} throughout the remainder of this section. V_{OLP} is defined as the maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs. V_{OHV} is defined as the minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs. Figure 4.1-3 shows V_{OHV} and V_{OLP}.



NOTES: A. V_{OHV} and V_{OLP} are measured with respect to ground reference near the output under test.
B. Input pulses have the following characteristics: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 1 ns.

Figure 4.1-3. Quiescent-Output Disturbance Voltage Waveforms

4.1.4 Simultaneous Switching Noise System Effects

In order to evaluate the effects of simultaneous switching noise effects in a system, both dc and ac noise margins must be considered. The dc noise

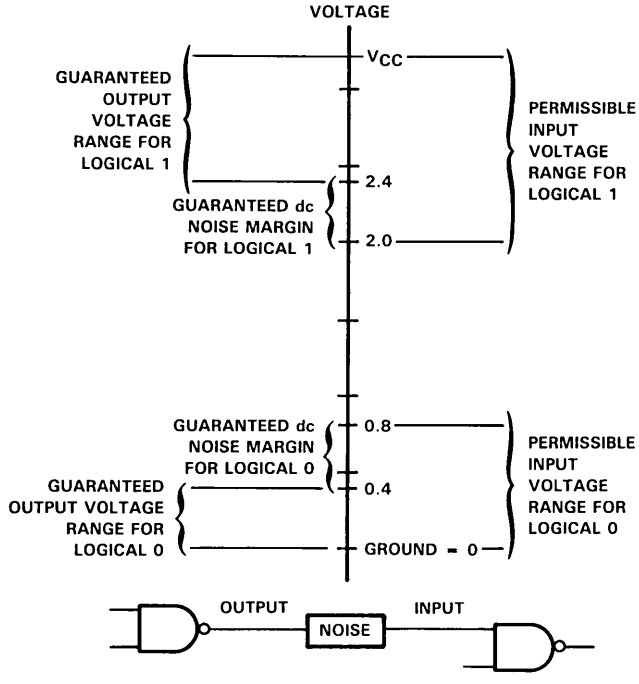
OEC is a trademark of Texas Instruments Incorporated.

margin is defined as the difference between the guaranteed logic state voltage limits of a driving gate and the voltage requirements of a driven gate.[2] Figure 4.1-4 graphically illustrates this for both TTL and CMOS devices. In general, the guaranteed dc noise margin is the difference between a V_{IL} and a V_{OL} or the difference between a V_{IH} and a V_{OH}. The dc noise margin for a low level is typically 0.4 V for TTL devices and 1.06 V for CMOS devices operating at 5 V V_{CC} and driving dc loads.

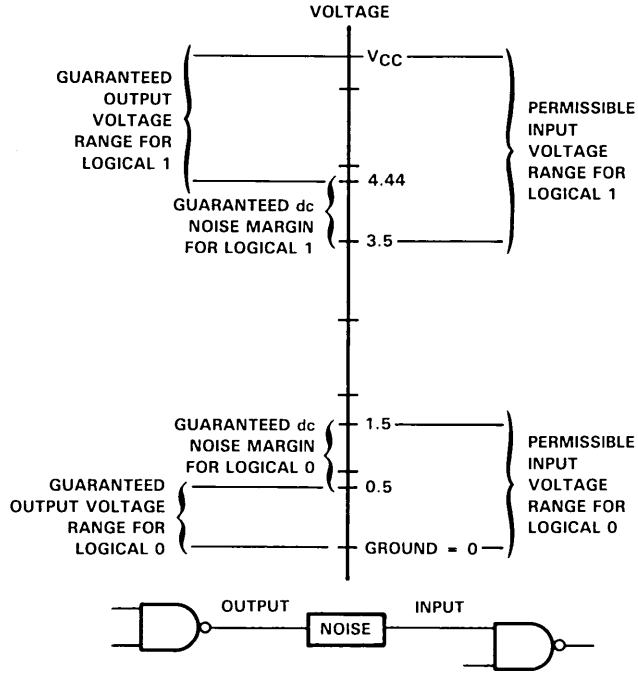
The guaranteed dc noise margin indicates that a noise excursion of 0.4 V for TTL devices or 1.06 V for CMOS devices is possible without propagating the noise through subsequent logic stages. Although the guaranteed noise margin of TTL devices is 0.4 V, a TTL input typically has a noise margin in excess of 1 V. TTL devices change states as the input voltage passes through a threshold voltage of about 1.5 V. Since a typical TTL V_{OL} is 0.25 V, an input can tolerate 1.25 V of noise before the false signal is propagated. In a system, this noise is comprised of crosstalk components, power plane noise as well as simultaneous switching glitches.[3,4]

The term dc noise margin may seem inappropriate when applied to noise, which in general, is an ac factor. For high-speed logic, signals with pulse widths of greater than 30 ns or 40 ns can be considered dc. As pulse durations shorten, a limit is reached where an input pulse can be shorter than the time required for a signal to propagate through the device. As this point is approached, pulses of greater amplitude are required to effect a change at the driven device output. Eventually, any pulse of reasonable amplitude will not be propagated.

End-pin ACL devices exhibit simultaneous switching noise pulse widths of 4 ns to 8 ns for pulse amplitudes of 1.7 V to 2.5 V. In order to evaluate the effect of noise with these characteristics, it is necessary to evaluate the ac noise margin of the receiving device. Figure 4.1-5 shows the ac noise margin 74F logic devices exhibit over a wide range of process and operating condition variances. Figure 4.1-5 shows a 74F device can erroneously switch for noise glitches with amplitudes of 1.75 V to 2.25 V and pulse duration of 1 ns to 5 ns. The erroneous switching performance of a device due to simultaneous switching-induced glitches will be adversely affected by other sources of system noise and levels of dc bias present at its input. These other factors reduce the ac noise margin inherent to the device.



(a) TTL dc Noise Margin



(b) CMOS dc Noise Margin at V_{CC} = 5 V Driving TTL Loads

Figure 4.1-4. Application Report

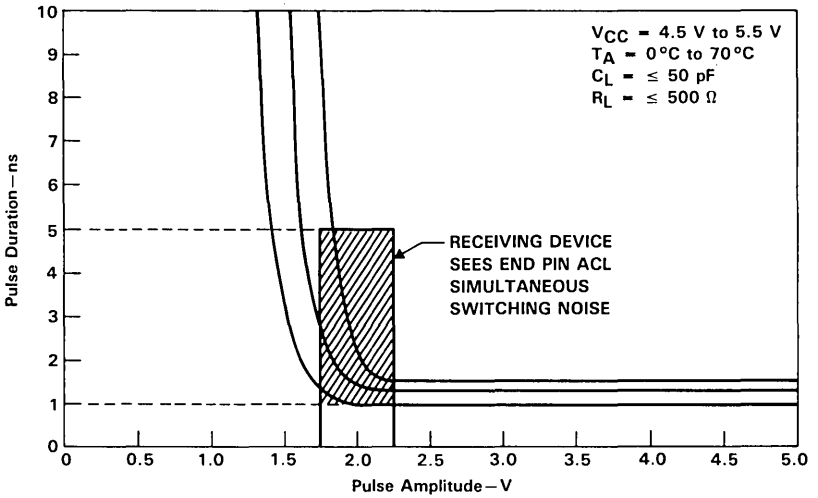


Figure 4.1-5. Pulse Duration vs Pulse Amplitude (Typical 74F Clock Pin Process and Operating Condition Variances)

4.1.5 Simultaneous Switching System Considerations

The first-order description of the simultaneous switching noise phenomenon of a simple circuit given in the previous sections is useful to illustrate the primary cause of the glitches. However, there are several environmental factors to be considered which cannot be described in simple mathematical terms. In order to evaluate the effects of these factors, experimental results are presented. Therefore, it also becomes critical to understand the relationship between system applications and characterization data.

The system implementation factors to be evaluated are

- Lumped capacitive loading at a distance
- Distributed capacitive loading at a distance
- Temperature
- Package options
- Power supply voltage
- Lumped ac and dc loading at the device
- Input signal offsets
- Input signal edge rates, and
- Circuit propagation delay effects.

4.1.5.1 Lumped and Distributive Loading (at a distance) Effects

Texas Instruments Advanced High-Speed Logic characterization boards are constructed with lumped output loads placed as near the DUT (device under test) as possible. This is necessary to obtain sufficiently clean signals for accurate measurement. Data that has been presented in this section was obtained using the standard procedure in sections 4.1.6.4 and 4.1.6.5 with characterization boards configured as described.

Typical system environments do not offer simple lumped loads at the device pins. If transmission lines between receiving devices are short, the environment that the output is driving can appear as lumped capacitive loads some distance away. Longer transmission lines, such as those encountered in bus applications, appear as distributed capacitive loads. In order to evaluate these effects, the circuit shown in Figure 4.1-6 was constructed. A quad-gate device was chosen to drive a 4-inch signal line to a 74HC241 receiver. Test points were defined at 1-inch increments along the signal paths.

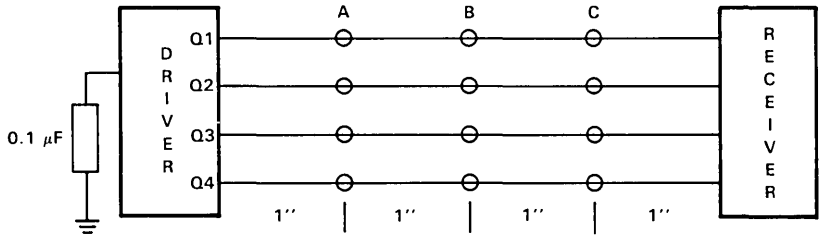


Figure 4.1-6. Laboratory Setup for Distributed Loading Evaluation

In testing the effects of lumped capacitive loading away from the device pins, 50-pF loads were placed at test points A or B, and V_{OLP} was recorded. As can be seen from Figures 4.1-7 and 4.1-8, the results of placing the lumped load 1 to 2 inches away from the device under test is a reduction in the magnitude of V_{OLP} at the output of the device under test. However, in a system environment as shown in Figure 4.1-6, the magnitude of V_{OLP} at the receiver is approximately the same as that obtained from a characterization board (Figures 4.1-9 and 4.1-10 can be used for comparison) with the standard loads placed very close to the device under test: for the 74AC00, V_{OLP} is approximately 1.25 V and for the 74AC11008, V_{OLP} is about 0.5 V.

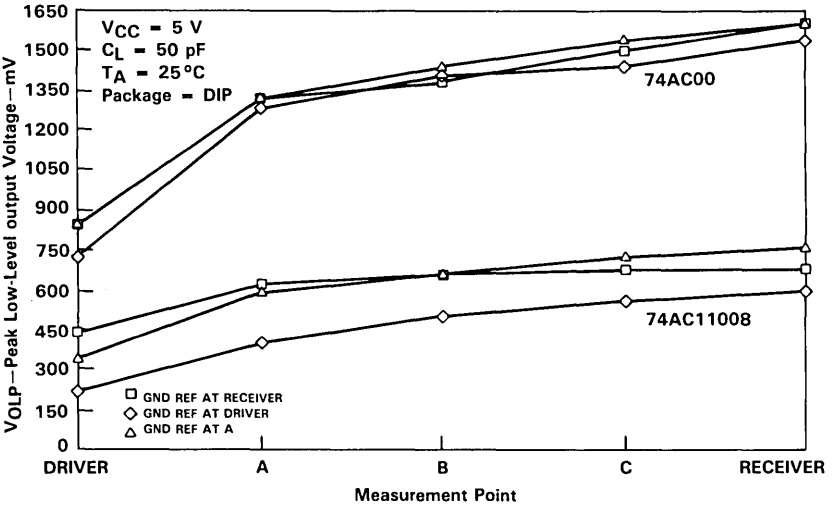


Figure 4.1-7. Peak Low-Level Output Voltage vs Distance (Lumped Capacitance at Point A)

To evaluate the impact of an output driving distributed capacitive loads such as multiple devices on a system bus, 15-pF capacitors were placed at test points A, B, and C (reference Figure 4.1-6). V_{OLP} was recorded for both an end pin 74AC00 and Texas Instruments 74AC11008. The results are shown in Figure 4.1-11. Once again, the magnitude of the switching noise is reduced at the output of the driving device, but at the receiver, the level of V_{OLP} is very near that obtained using an ACL simultaneous switching characterization board.

The major effect of placement of lumped and distributed capacitive loads at a distance away from the driving device is reduction of V_{OLP} or V_{OHV} at the output of the driver. In a system, this is not the point where a switching glitch would be most troublesome. The magnitude of V_{OLP} or V_{OHV} at the input of the receiver determines whether switching noise will cause a system failure. The values obtained from a system environment correlate very well with the values measured on an ACL simultaneous switching characterization board.

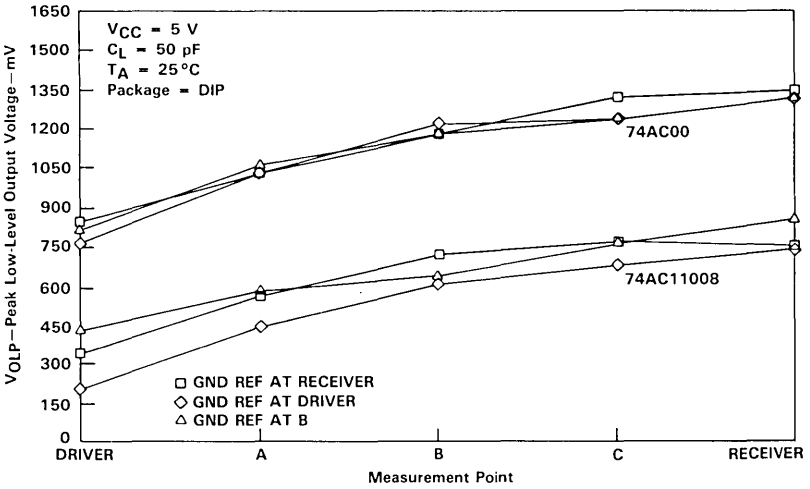


Figure 4.1-8. Peak Low-Level Output Voltage vs Distance (Lumped Capacitance at Point B)

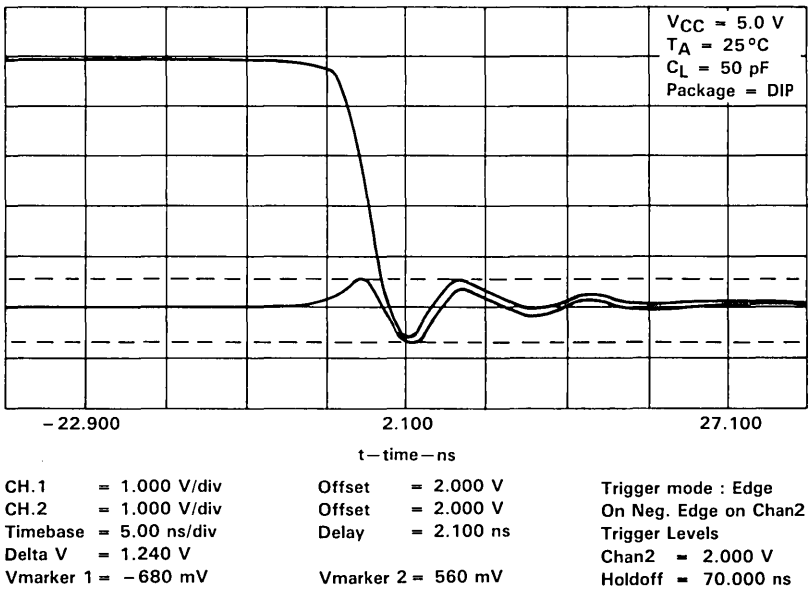
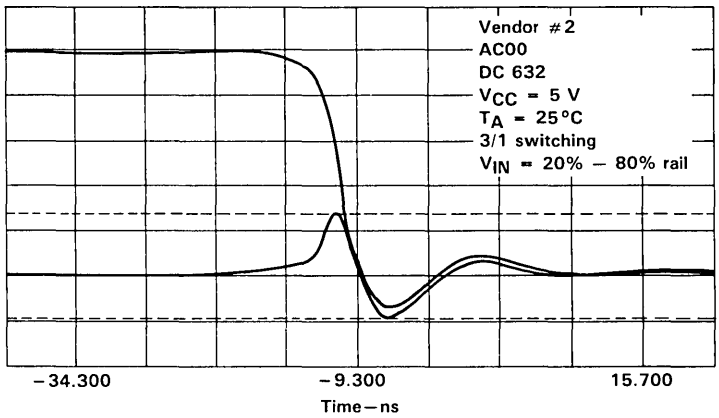


Figure 4.1-9. V_{OLP} Characterization Results for AC11008



CH.1 = 1.000 V/div
CH.2 = 1.000 V/div
Timebase = 5.00 ns/div
Delta V = 2.320 V
Vmarker 1 = –940.0 mV

Offset = 2.000 V
Offset = 2.000 V
Delay = –9.300 ns

Vmarker 2 = 1.380 V

Trigger mode : Edge
On Pos. Edge on Chan2
Trigger Levels
Chan2 = 2.000 mV
Holdoff = 70.000 ns

Figure 4.1-10. V_{OLP} Characterization Results for AC00

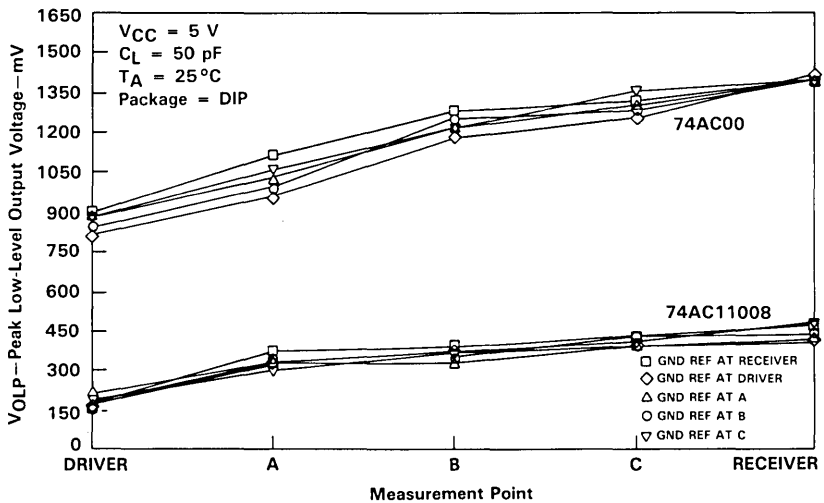


Figure 4.1-11. Peak Low-Level Output Voltage vs Distance (Distributed Capacitance)

4.1.5.2 Temperature Effects

Equation 6 illustrates the magnitude of the switching noise realized on a device's power or ground plane of a device during a simultaneous switching incident will be a function of output edge rate (dv/dt) of the device. As MOS (Metal Oxide Semiconductor) devices operate at lower temperatures, they become intrinsically faster. This is due to the inverse temperature dependence of electron and hole mobilities; i.e., as temperature decreases, mobilities increase.[5] Figures 4.1-12 through 4.1-15 illustrate the effects of temperature upon V_{OLP} and V_{OHV} for other manufacturers end-pin devices and Texas Instruments ACL devices. Quad gates as well as octal D-type latches are evaluated. Note the increased magnitude of V_{OLP} and the decreased value of V_{OHV} at lower temperatures.

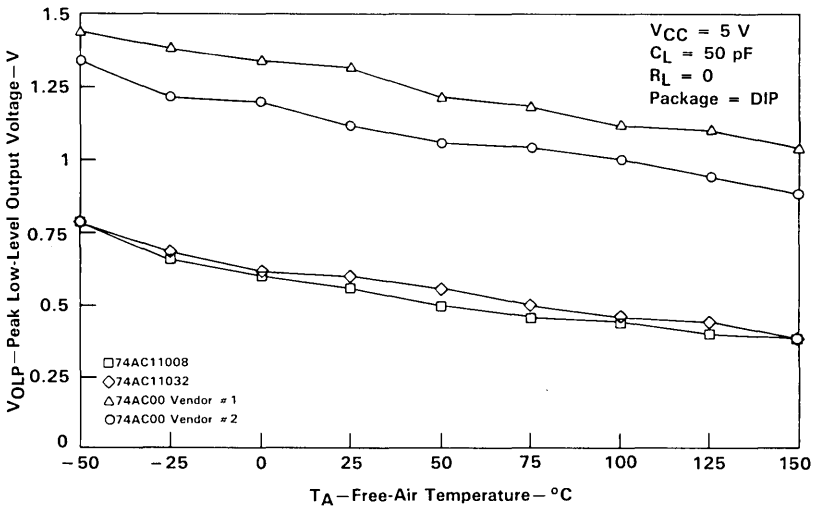


Figure 4.1-12. Evaluation of Temperature Effects (Peak Low-Level Output Voltage vs Free-Air Temperature)

4.1.5.3 Package Effects

Texas Instruments offers its EPIC™ ACL family functions in surface-mount packaging as well as traditional DIP (Dual-in-Line) packaging. Figures 4.1-14 and 4.1-15 also show the difference in the magnitude of the induced voltage between DIP and SO (Small Outline) packaged 74AC373 and 74AC11373

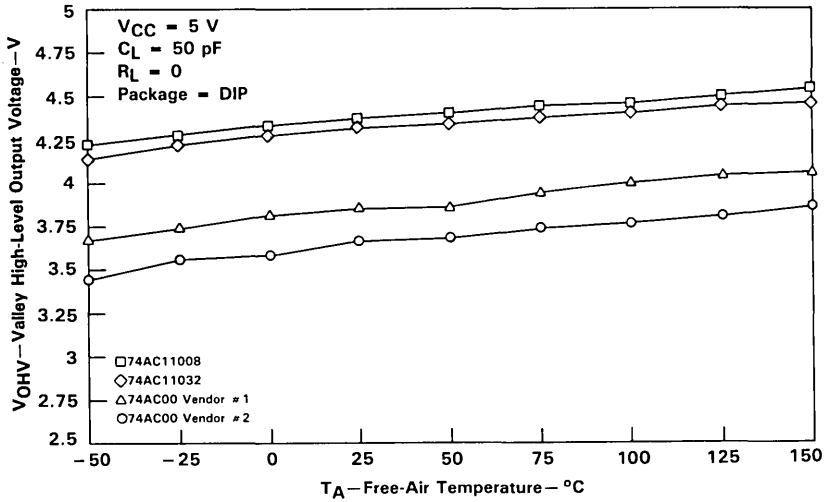


Figure 4.1-13. Evaluation of Temperature Effects (Valley High-Level Output Voltage vs Free-Air Temperature)

devices. A very important observation can be made based upon Figures 4.1-14 and 4.1-15. The reduction in the magnitude of V_{OLP} and V_{OHV} from DIP to SO packages does not track linearly with the reduction in package inductances as shown in Table 4.1-1.

Table 4.1-1 Comparison of Dual-in-Line (DIP) and Small Outline (SO) 20-Pin Package Parasitic Inductances and Percent Change in Switching Noise

PIN	DUAL-IN-LINE SELF-INDUCTANCE	SMALL-OUTLINE SELF-INDUCTANCE	DIP TO SO PERCENTAGE CHANGE		
			SELF-INDUCTANCE	END-PIN V_{OLP}	CENTER-PIN V_{OLP}
1	13.7 nH	5.8 nH	57%	18%	36%

The reason the magnitude of switching noise is not reduced proportionally to a reduction in package parasitics is the effective positive feedback which exists between the silicon die and the package ground or power pin inductances. A reduction in the package ground or power pin inductance reduces the debiasing effects of the induced noise on the transistors in the circuit. This allows the transistor to switch faster, generating larger dv/dt and more switching noise.

As shown in Figures 4.1-14 and 4.1-15, the use of devices with end-pin power and ground, whether in DIP or SO packages, will not allow for reliable system operation. Texas Instruments ACL family with its multiple center power pins offers noise performance compatible with reliable system performance in both dual-in-line and surface-mount packages.

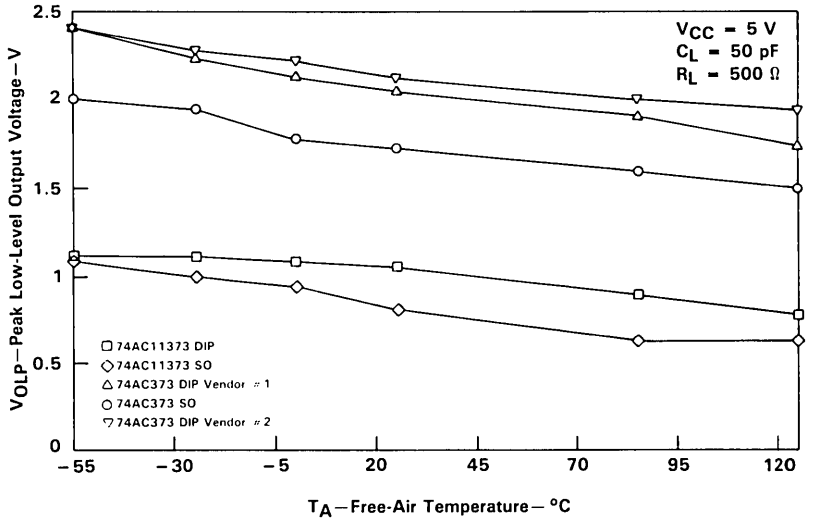


Figure 4.1-14. Peak Low-Level Output Voltage vs Free-Air Temperature

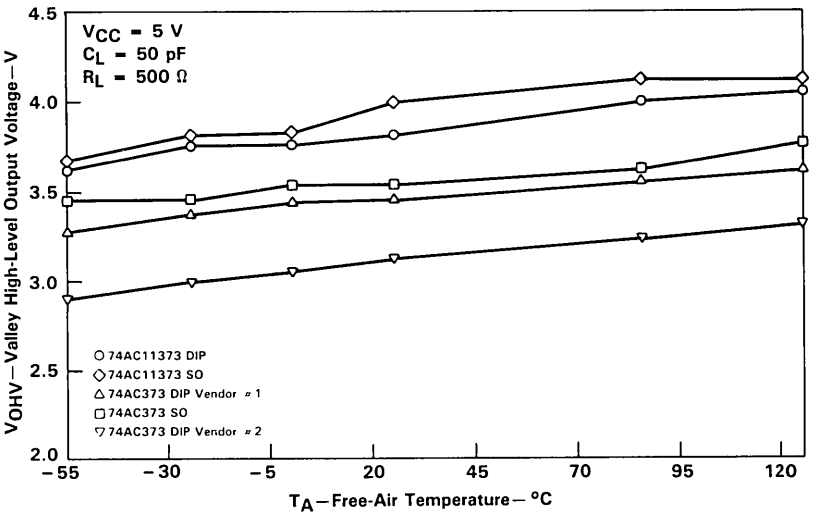


Figure 4.1-15. Valley High-Level Output Voltage vs Free-Air Temperature (74AC11373 Compared to End-Pin Product)

4.1.5.4 Power Supply Voltage Effects

The effects of V_{CC} voltage variances upon V_{OLP} and V_{OHV} are related to the magnitude of the output voltage signal swing or dv/dt (Equation 6). CMOS

output circuits switch from rail to rail; i.e., from V_{CC} to GND. Hence, the larger the V_{CC} voltage, the larger the switching noise generated. Figures 4.1-16 and 4.1-17 show this phenomenon for both V_{OLP} and V_{OHV}.

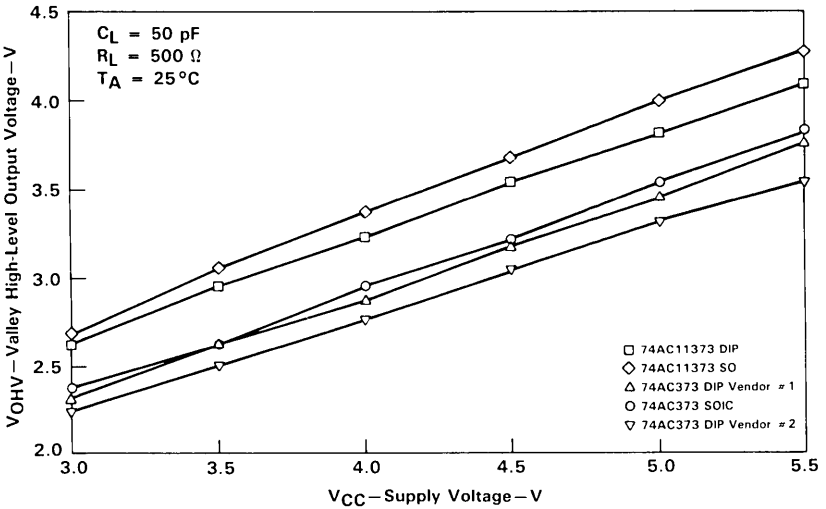


Figure 4.1-16. Valley High-Level Output Voltage vs Supply Voltage (74AC11373 Compared to End-Pin Product)

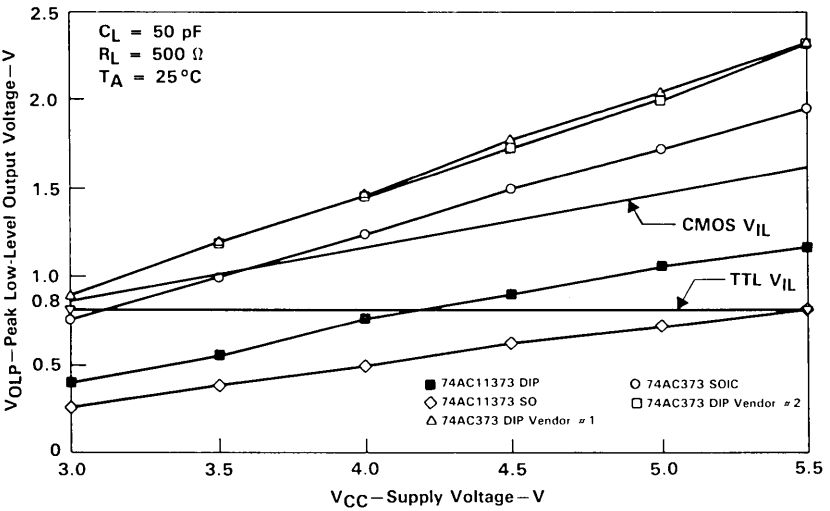
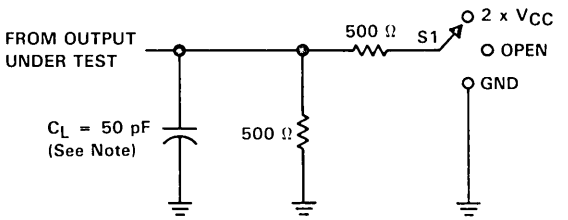


Figure 4.1-17. Peak Low-Level Output Voltage vs Supply Voltage (74AC11373 Compared to End-Pin Product)

The tradeoff for operation at lower V_{CC} to reduce switching noise is one of speed versus noise. Any advanced CMOS product in the market today has propagation delays specified at V_{CC} = 5 V as well as V_{CC} = 3.3 V. In general, the propagation delays of an ACL device are 40% slower during 3.3-V operation than at 5 V.

4.1.5.5 Lumped AC and DC Loading (at the device) Effects

Advanced high-speed logic devices are characterized, tested, and functionally guaranteed with a standard output loading of 50 pF and 500 Ω. Figure 4.1-18 shows the standard loads for the Texas Instruments ACL family. System environments generally offer a variety of capacitive and resistive loads, rather than simple 50-pF/500-Ω loads.



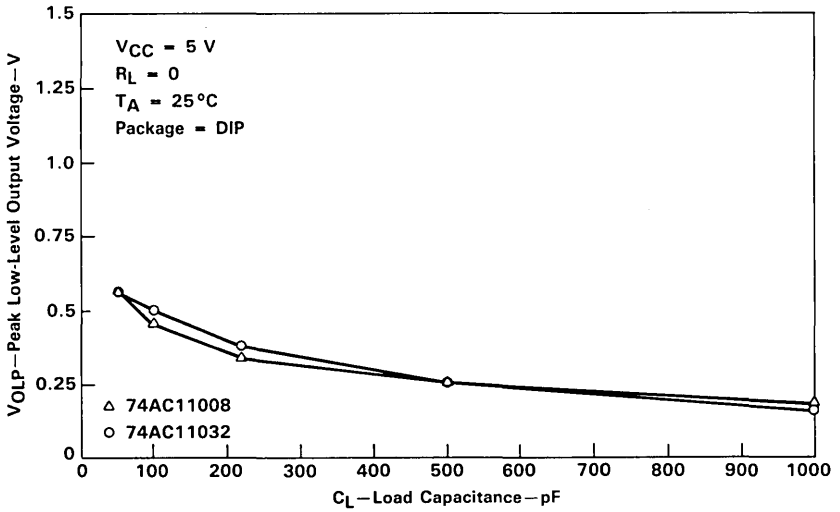
TEST	S1
t_{PLH}/t_{PHL}	OPEN
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

NOTE: C_L includes probe and jig capacitance.

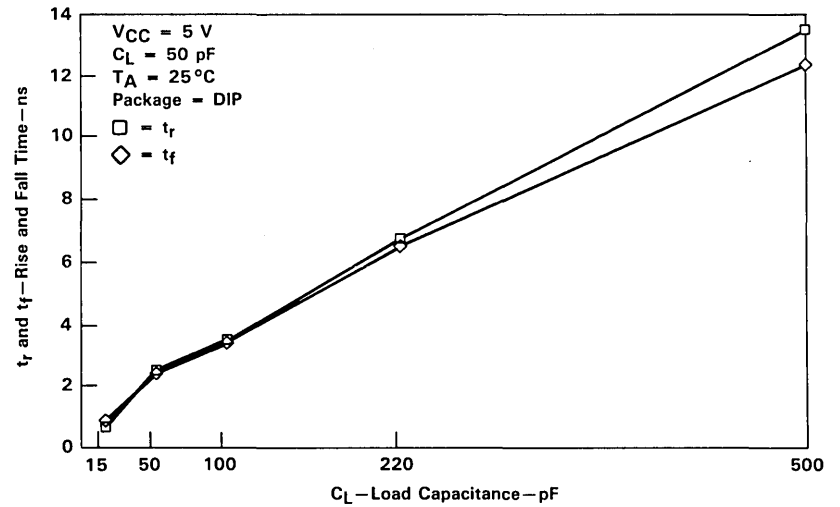
Figure 4.1-18. Standard ACL Load Circuit

Figure 4.1-19(a) shows the effect of additional lumped capacitances at device outputs upon the amount of noise generated during a switching incident. The reduction in the magnitude of V_{OLP} seems to invalidate Equation 6, which indicates the level of switching noise should be directly proportional to output capacitive loading. However, Equation 6 also indicates the magnitude of switching noise is proportional to the output waveform edge rate (dv/dt). The edge rate of an ACL output waveform is directly proportional to the capacitive load it is charging or discharging. As shown in Figure 4.1-1, a CMOS output circuit is simply a parallel RC network whose response time is given by the product of the output transistor channel resistance and the load capacitance. Figure 4.1-19(b) illustrates the increase in output edge rates due to the increase in the lumped capacitive loading at the output pins. Figure 4.1-20 displays the capacitive loading at the output pins and the effect of this edge roll-off on device propagation delays. The reduction in switching noise with increased capacitive loads is accomplished by reducing the switching speed of the circuits.

The standard load configuration of a 500-Ω resistor to ground simulates a system situation where a logic device must supply a finite dc current. The current may be caused by input current requirements for bipolar TTL devices or termination schemes used upon a bus. The 500-Ω resistor in the standard



(a) Loading Effect Evaluation, Peak Low-Level Output Voltage vs Load Capacitance



(b) AC11027 Load Capacitance vs Rise and Fall Times

Figure 4.1-19. Load Capacitance vs Other Parameters

load requires an ACL device operating at V_{CC} = 5 V to provide an output current of approximately 10 mA when the output is in the high state. This current is approximately half of the maximum rated 24-mA output current (I_{OL} or I_{OH}) of an ACL device.

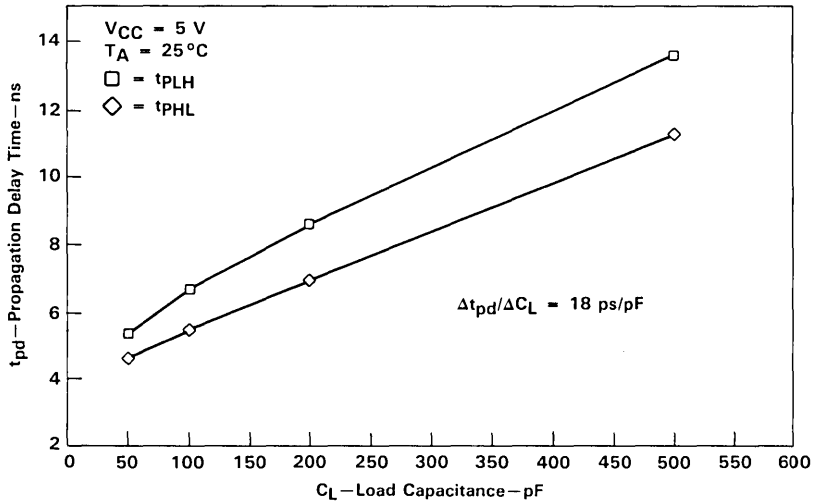


Figure 4-1-20. Propagation Delay Time vs Load Capacitance

In order to evaluate the effects of other finite dc currents upon V_{OLP} and V_{OHV}, simultaneous switching tests were performed over a wide range of I_{OL} and I_{OH} currents. Figures 4.1-21 and 4.1-22 depict only a slight increase in V_{OHV} and V_{OLP} for dc currents greater than 24 mA. These are expected

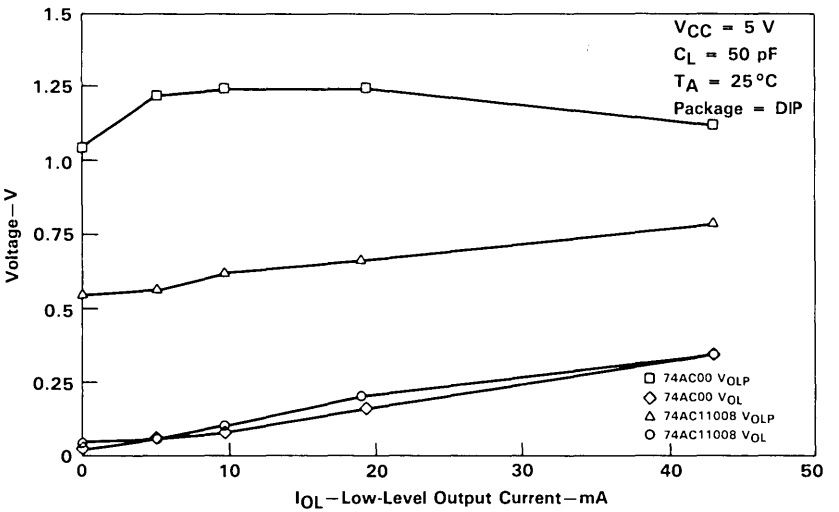


Figure 4.1.21. Loading Effect Evaluation, Low-Level Output Voltage/Peak Low-Level Output Voltage vs Low-Level Output Current

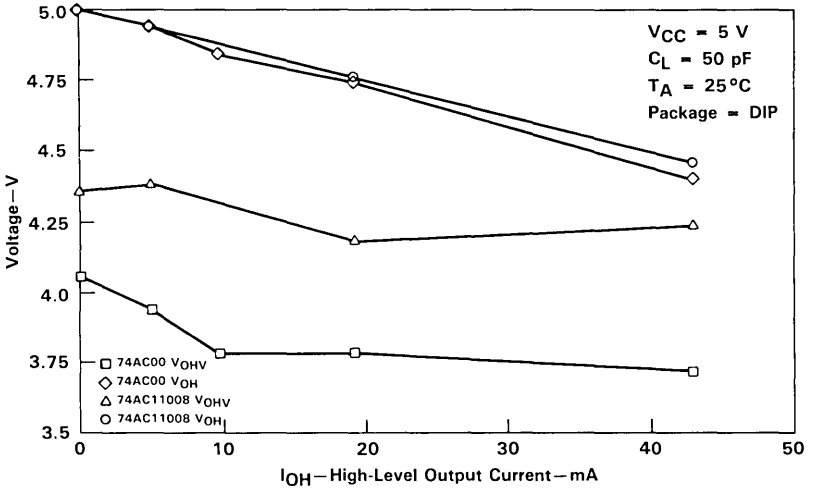


Figure 4.1-22. Loading Effects Evaluation, High-Level Output Voltage/ Valley High-Level Output Voltage vs High-Level Output Current

results, because although simultaneous switching is a function of transient current (ac), more charge must be moved during a switching incident when the output is loaded with a dc current.

4.1.5.6 Input Signal Offset Effects

In system operation, it can be argued that the occurrence of a perfectly simultaneous switching incident is unlikely to occur due to timing skews in signal paths and semiconductor devices. In order to evaluate a system environment with input signals skewed, an experiment was performed using quad gates. The input signals to each of three gates were supplied using different channels of a high-speed pulse generator while the fourth output on the device was held in a low state. Using the delays of the pulse generator, the input signals were skewed in 1-ns increments for all possible combinations of inputs. V_{OLP} was recorded for each test condition.

Figure 4.1-23 shows the results for an end-pin 74AC00 and Texas Instruments 74AC11032. Note the sinusoid response of V_{OLP} as a function of input signal offset. This effect is caused by the natural frequency of the parasitic tank circuit formed by the load capacitor, channel resistance of the output transistor, and the ground-pin inductance. For up to 10-ns input signal offsets, the level of V_{OLP} is essentially the same as that of a simultaneous switching incident. This illustrates that, even with large values of input signal skew, a device can exhibit large V_{OLP} and V_{OHV} values.

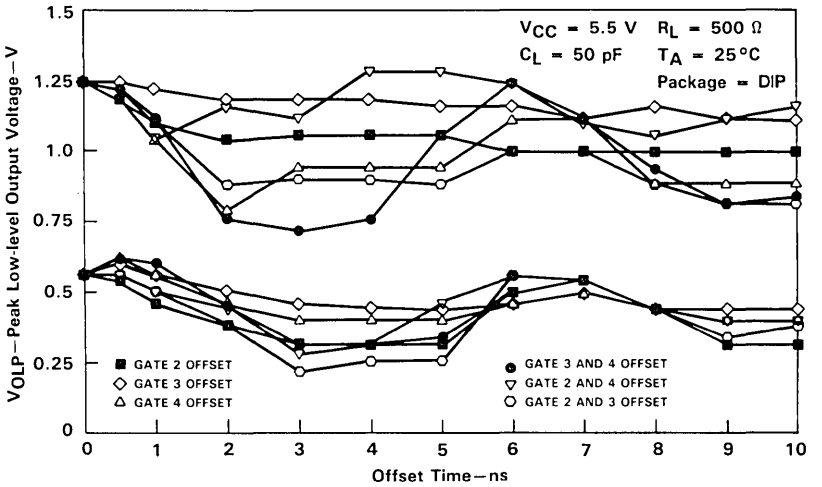


Figure 4.1-23. Input Signal Offset Evaluation (74AC00 vs 74AC11032)

4.1.5.7 Input Signal Edge Rates

The magnitude of V_{OLP} and V_{OHV} can depend upon the input signal transition time. In order to simulate simultaneous switching phenomenon, several inputs of a device may be tied together. Connecting inputs together can degrade input signal rise and fall times from the specified 3 ns to approximately 8 ns to 10 ns. Studies have been conducted to evaluate the effects of input signal edge rates upon V_{OLP} and V_{OHV}. It has been found that input signal edge rates from 1 ns to 10 ns do not affect the magnitude of V_{OLP} and V_{OHV}; however, it is important for input signals to be properly terminated as near the device as possible so that the input signal edge is monotonic on all input pins.

4.1.5.8 Propagation Delay Effects

The occurrence of a simultaneous switching incident can affect the propagation delay of an ACL device. As explained in a previous section, the amplitude of the voltage induced on the silicon die increases as the number of outputs switching simultaneously increases. This induced voltage artificially increases or decreases the threshold of the device. As the switching threshold varies, the time required for the signal to propagate from the input to the output varies accordingly, depending on the input transition and the phase of the ground bounce with respect to the transition.

Texas Instruments tests propagation delay effects due to simultaneously switching outputs in the design characterization process. This test is not a production test, but is performed only on the bench during characterization.

The test is performed at the nominal conditions of V_{CC} = 5 V and T_A = 25°C with standard data book loads and waveforms. A comparison is made of the propagation delay with 1, N/2, and N outputs switching simultaneously. The input transition edge is 3 ns. Propagation delay data for an AC11373 is included in Table 4.1-2. This data indicates that both t_{PLH} and t_{PHL} increase with the number of outputs switching. Table 4.1-2 includes data for an AC11244 switching in and out of a 3-state condition. The trend in this situation is for the propagation delay to decrease when switching into 3-state as the number of outputs switching increases, and to increase when switching out of 3-state.

Table 4.1-2 Propagation Delay Effects Due to Simultaneous Switching

AC11373, Output IQ	NUMBER OF OUTPUTS SWITCHING			AC11244, Output 1Y1	NUMBER OF OUTPUTS SWITCHING		
	1	4	8		1	4	8
t_{PLH}	6.69	7.65	8.88	t_{PZH}	6.43	6.91	7.60
t_{PHL}	6.27	6.70	7.51	t_{PHz}	6.03	5.82	5.70

The trends indicated from this data are common; however, the trends may vary from device to device, as well as from test fixture to test fixture. Skews in input edge signals and variance in input edge rates can affect the trends.

4.1.6 Simultaneous Switching Evaluation

The many factors influencing device simultaneous switching performance require careful consideration before a standard test methodology can be implemented. These factors can be grouped into test board considerations, measurement considerations, and characterization environment considerations.

Test board considerations include the physical makeup of the board and signal loading. Pin location, ground reference, and scope equipment are included in measurement considerations. Characterization environment considerations include power supply voltage, ambient temperature, and input signal characteristics. A standard simultaneous switching test methodology for the EPIC™ ACL family is presented in sections 4.1.6.4 and 4.1.6.5.

4.1.6.1 Test Board Considerations

The simultaneous switching test board is a multilayer, 50-Ω board displayed in Figures 4.1-24 and 4.1-25. A parts list with vendor information is provided in section 4.1.6.6. Multiple ground and V_{CC} planes minimize power node inductance and are commonly found in high-speed system boards. Signal

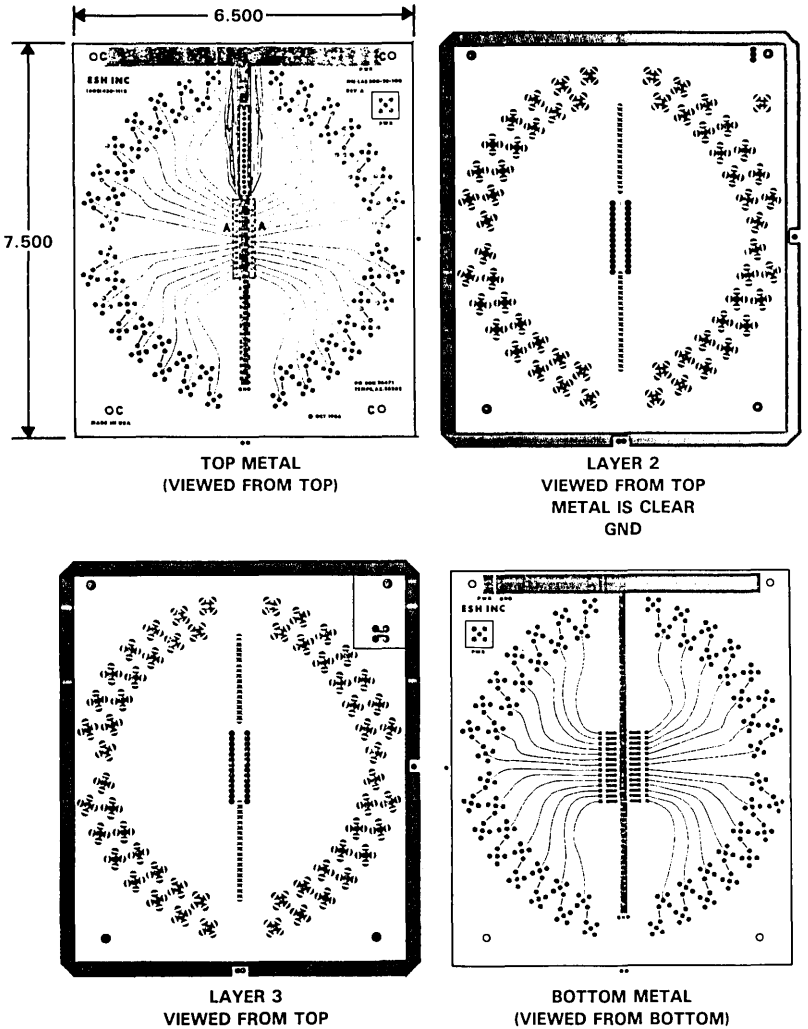


Figure 4.1-24. Board Layout and Composition

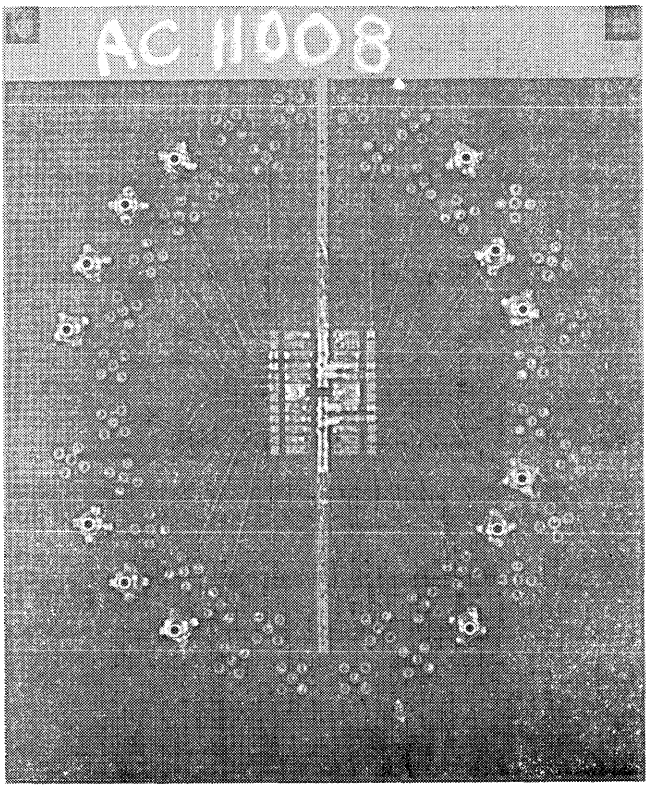
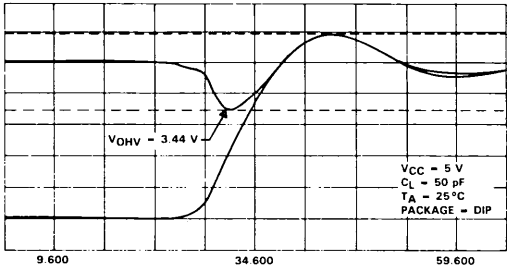


Figure 4.1-25. Board Photograph

traces run equal lengths to barrel connectors which offer a reduced inductance seat for the device under test. Though barrel connectors are not usually used in systems, data from another manufacturer's AC240 in Figure 4.1-26 shows that they yield the same results as a soldered device in Figure 4.1-26. Since logic gate switching can cause large current transients, a decoupling capacitor of 0.1 μF is used between the power rails.

Due to the high-speed signals that will be used to test the device, ac loading becomes a critical part of the setup. The device under test must not operate in an environment of mismatched transmission lines; therefore, in addition to the use of proper values for ac loading, the placement of the loads on the board is critical. For example, input signal traces are terminated in 50-Ω resistors at the device input pins, instead of at the Sealectro RF connector, for proper termination of the 50-Ω coax cables used to connect the SPG (Signal Pulse Generator) to the board. The termination at the device pins is easily accommodated through the use of the center ground strip on the simultaneous switching board (reference Figures 4.1-24 or 4.1-25). Output signal traces



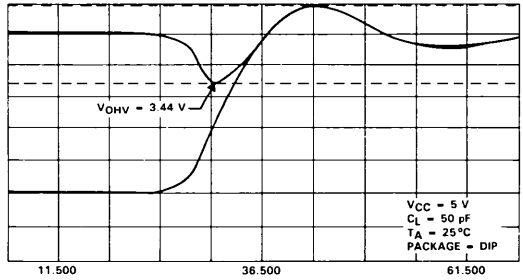
CH.1 = 1.000 V/div
CH.2 = 1.000 V/div
Timebase = 5.00 ns/div
Delta V = 2.500 V
Vmarker 1 = 3.440 V

Trigger mode : Edge
On Pos. Edge on Trig3
Trigger Levels
Trig 3 = 750.00 mV
Holdoff = 70.000 ns

Offset = 3.000 V
Offset = 3.000 V
Delay = 34.600 ns

Vmarker 2 = 5.940 V

Vendor #2
AC240
7/1 switching
V_{IN} = 20% – 80%



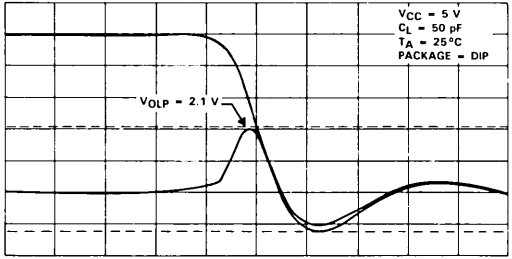
CH.1 = 1.000 V/div
CH.2 = 1.000 V/div
Timebase = 5.00 ns/div
Delta V = 2.460 V
Vmarker 1 = 3.440 V

Trigger mode : Edge
On Pos. Edge on Trig3
Trigger Levels
Trig 3 = 750.00 mV
Holdoff = 70.000 ns

Offset = 2.000 V
Offset = 2.000 V
Delay = 36.500 ns

Vmarker 2 = 5.900 V

Vendor #2
AC240
7/1 switching
V_{IN} = 20% – 80%

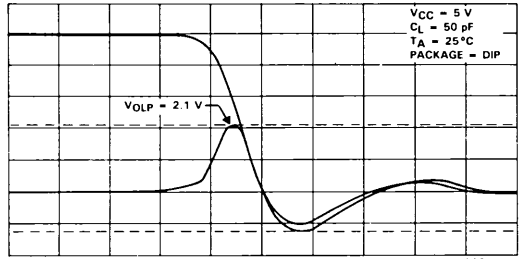


CH.1 = 1.000 V/div
CH.2 = 1.000 V/div
Timebase = 5.00 ns/div
Delta V = 3.320 V
Vmarker 1 = 1.260 V

Trigger mode : Edge
On Pos. Edge on Trig3
Trigger Levels
Trig 3 = 750.00 mV
Holdoff = 70.000 ns

Offset = 2.000 V
Offset = 2.000 V
Delay = 34.700 ns

Vmarker 2 = 2.060 V



CH.1 = 1.000 V/div
CH.2 = 1.000 V/div
Timebase = 5.00 ns/div
Delta V = 3.360 V
Vmarker 1 = –1.260 V

Trigger mode : Edge
On Pos. Edge on Trig3
Trigger Levels
Trig 3 = 750.00 mV
Holdoff = 70.000 ns

Offset = 2.000 V
Offset = 2.000 V
Delay = 36.800 ns

Vmarker 2 = 2.100 V

(a) Data Taken with Device in Barrel Connectors **(b) Data Taken with Device Soldered to Board**

Figure 4.1-26. V_{OHV} and V_{OLP} Data for Two Cases

are terminated with a 47-pF capacitor at the pin with a 450-Ω resistor in series with the trace. Correct ACL dc output resistive loading is achieved through either a 50-Ω terminator or a 50-Ω scope probe at the Sealectro RF connector.

4.1.6.2 Measurement Considerations

The device pin with the largest total inductance (i.e., self plus mutual) produces worst-case results and should be used as the test pin. The inductive noise versus pin location is displayed in Figure 4.1-27. As expected, the pins farthest from the center of the package have larger values of inductive noise. However, the worst-case noise may not be observed on the corner pins; rather it could occur on their adjacent neighbors. This is not surprising since corner pins can have a lower value of mutual coupling to active pins than their neighbors. This effect is negated by a much larger drop in the self-inductances as the pin locations get closer to the center of the package. Since different package types will exhibit slightly different characteristics, worst-case pin locations will vary with package and device type.

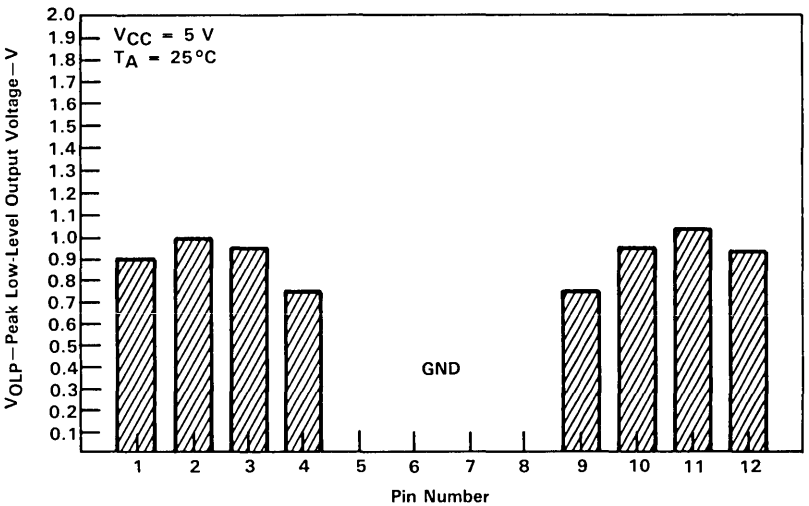


Figure 4.1-27. AC11240 Peak Low-Level Output Voltage vs Pin Location

The correct setup for accurate measurement of simultaneous switching events is displayed in Figure 4.1-28. The scope is an HP54110D with a 1-Ghz bandwidth. Scopes with smaller bandwidths are not recommended due to the high-frequency components of the inductive voltages that will be translated as data by high-speed logic devices. Probes are standard 50-Ω coax that attach to Sealectro RF connectors on the test board. These probes complete the 500-Ω resistive loading on the device output pins, and their

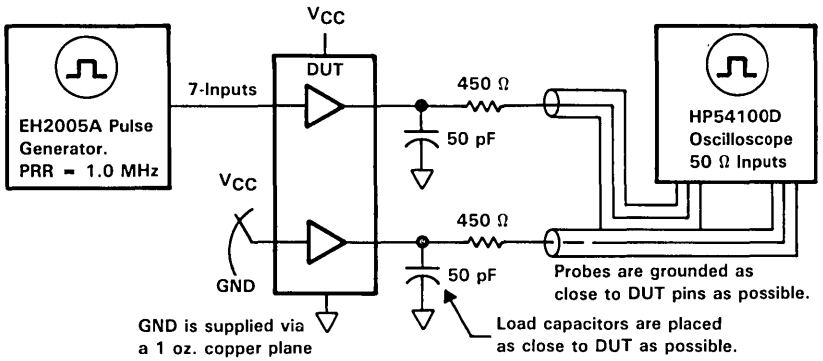


Figure 4.1-28. Standard Simultaneous Switching Evaluation Circuit

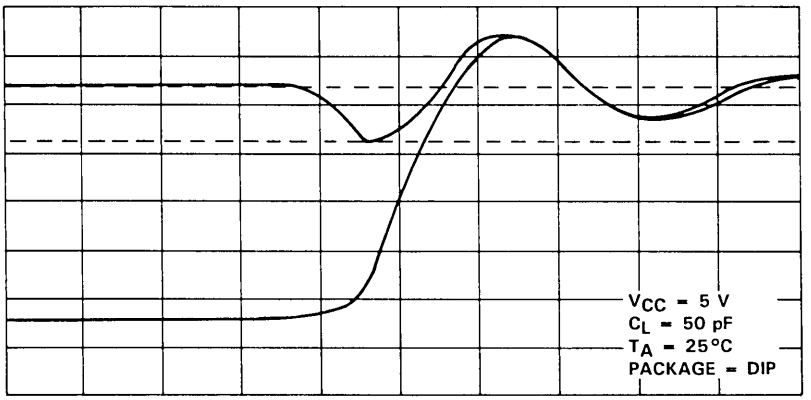
ground reference is the ground plane of the simultaneous switching board. This setup allows absolute measurement of the magnitude of the induced noise at a receiver input pin. Differential measurements from the output under test to the device under test ground pin do not indicate the true magnitude of the glitch seen by a receiving device and should not be used.

4.1.6.3 EPIC™ ACL Characterization Environment Considerations

The system environment affects device performance in many ways. For example, speed and power dissipation are a function of the power supply voltage, ambient temperature, and input signal edge rates. Since simultaneous switching performance is a function of output edge rate and transient output current, these factors also affect device simultaneous switching performance. Careful system designers require worst-case data and nominal data; therefore, a standard test methodology includes both data points. Texas Instruments characterizes EPIC™ ACL devices at nominal conditions of V_{CC} = 5 V and T_A = 25°C and worst-case conditions of V_{CC} = 5.5 V and T_A = −55°C, since the family is offered with military specifications. Commercial users should expect improved worst-case performance at the minimum specified temperature of −40°C. The procedure in section 4.1.6.4 is offered as a standard evaluation of simultaneous switching performance. It has been adapted specifically to the EPIC™ ACL family of devices, but testing other families requires only minor modifications of data sheet parameters such as maximum V_{CC}, input voltage swings, etc.

Sample nominal data from each of the three simultaneous switching tests are displayed in Figures 4.1-29, 4.1-30, 4.1-31, and 4.1-32. Correct data can only be obtained through careful use of a standard test methodology. The physical makeup of the test board, signal termination, test pin location, ground reference, and scope equipment are factors that must be considered. It is also important to recognize the system environment and consider power supply voltage, ambient temperature, and input signal characteristics. The

standard test methodology must be applicable to all families, bipolar or CMOS. Although the above procedure has been tailored to the EPIC™ ACL family of devices, minor modifications of V_{IH}, V_{IL}, and V_{CC} will allow application of this procedure to other families.

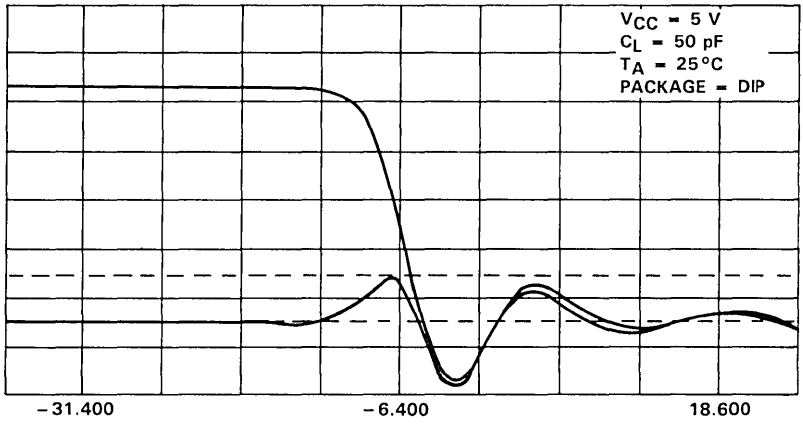


CH.1 = 1.000 V/div
CH.2 = 1.000 V/div
Timebase = 5.00 ns/div
Delta V = 1.120 V
Vmarker 1 = 3.740 V

Offset = 2.500 V
Offset = 2.500 V
Delay = 491.900 ns
Vmarker 2 = 4.860 V

Trigger mode : Edge
On Pos. Edge on Chan2
Trigger Levels
Chan2 = 20.00 mV
Holdoff = 70.000 ns

Figure 4.1-29. V_{OHV} Nominal Measurement on 74AC11373

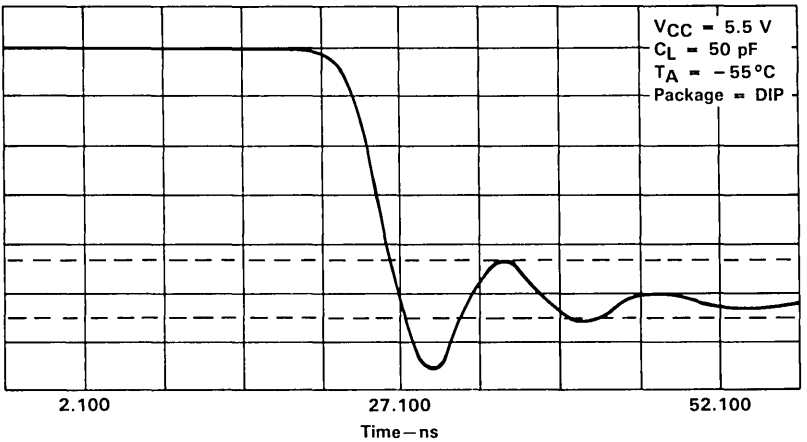


CH.1 = 1.000 V/div
CH.2 = 1.000 V/div
Timebase = 5.00 ns/div
CH. 1 Parameters

Trigger mode : Edge
On Pos. Edge on Chan2
Trigger Levels
Chan2 = 20.00 mV
Holdoff = 70.000 ns

Offset = 2.500 V
Offset = 2.500 V
Delay = -6.400 V
Preshoot = 920.0 mV

Figure 4.1-30. Peak Low-Level Output Voltage Nominal Measurement on 74AC11373



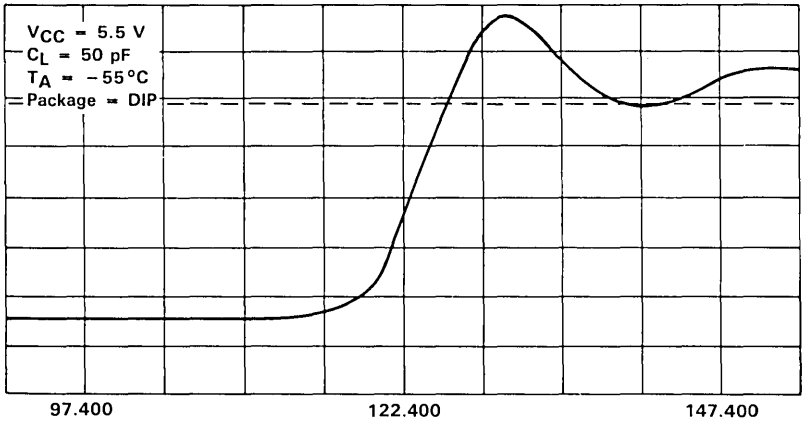
CH.2 = 1.000 V/div
Timebase = 5.00 ns/div
Delta V = 1.200 V
Vmarker 1 = 0.000 V

Offset = 2.500 V
Delay = 27.100 ns

Vmarker 2 = 1.200 V

Trigger mode : Edge
On Pos. Edge on Trig3
Trigger Levels
Trig3 = 250.0 mV
Holdoff = 70.000 ns

Figure 4.1-31. 74AC11373 Passes Stored Data Test on the High Impedance to Low Transition (ZL)



CH.2 = 1.000 V/div
Timebase = 5.00 ns/div
Delta V = 1.100 V
Vmarker 1 = 4.400 V

Offset = 2.500 V
Delay = 122.400 ns

Vmarker 2 = 5.500 V

Trigger mode : Edge
On Pos. Edge on Trig3
Trigger Levels
Trig3 = 2.000 V
Holdoff = 70.000 ns

Figure 4.1-32. 74AC11373 Passes Stored Data Test on the High Impedance to High Transition (ZH)

4.1.6.4 Simultaneous Switching Test Procedure

The simultaneous switching test is used to determine the magnitude of output disturbances during simultaneous switching of other outputs. In all cases except for devices with single outputs or single complementary outputs, the output under test is not switching. Paragraph 4.1.6.4.1 gives the procedure for evaluating this class of devices.

A procedure is also given for evaluating stored data integrity. Specifically, the stored data test consists of monitoring the output of one gate with a stored data bit while the other outputs are simultaneously switching. If the induced noise on the clock or latch enable pin is sufficient to clock or latch new data, a failure is recorded. Sample stored data integrity test data is shown in Figure 4.1-37. The input edge rate on all simultaneous switching tests is 3 ns.

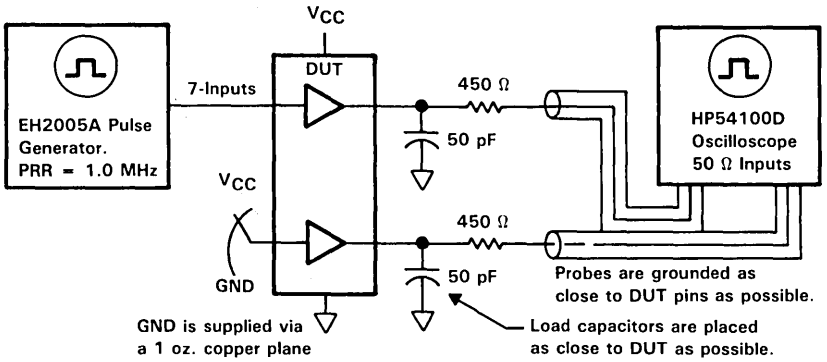
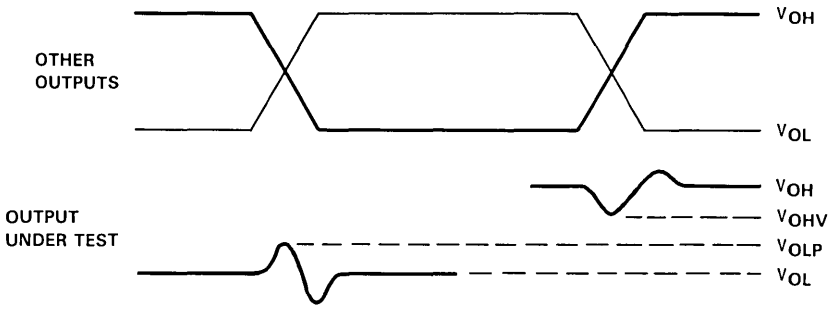


Figure 4.1-33. Standard Simultaneous Switching Evaluation Circuit

The terms V_{OHV} and V_{OLP} will be used to describe the output disturbance during simultaneous switching as shown in Figures 4.1-34 through 4.1-36. V_{OHV} is defined as the minimum (valley) high-level output voltage during switching. V_{OLP} is defined as the maximum (peak) low-level output voltage during switching of other outputs.



NOTES: A. V_{OHV} and V_{OLP} are measured with respect to ground reference near the output under test.
B. Input pulses have the following characteristics: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 1 ns.

Figure 4.1-34. Quiescent-Output Disturbance Voltage Waveforms

4.1.6.4.1 Simultaneous Switching Evaluation (Multiple Output Devices)

The simultaneous switching evaluation will be used to determine the magnitude of the disturbance on outputs that are not being switched, as well as stored data integrity for devices with multiple outputs.

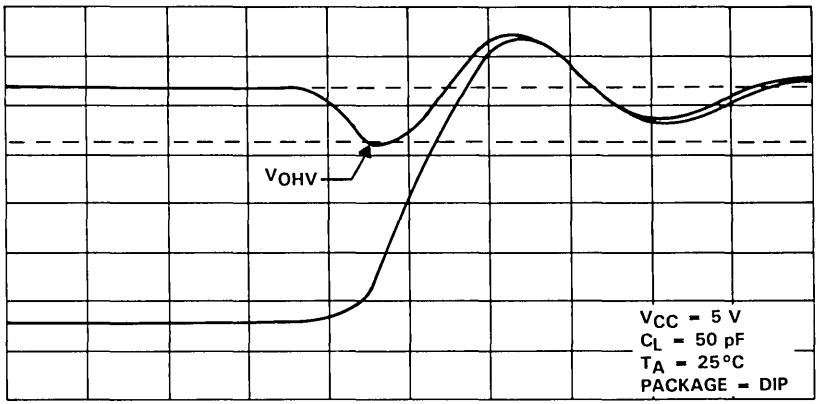
Simultaneous Switching Test Conditions

INPUT VOLTAGES	TEST CONDITIONS	LOAD CIRCUIT	TEST BOARD
V_{IH} = AC 80% V_{CC} ACT 2.5 V	V_{CC} = 5 V T_A = 25°C and	per data book spec	ESH 300-24 or ESH 300-28
V_{IL} = AC 20% V_{CC} ACT 0.5 V	V_{CC} = 5.5 V T_A = 55°C		

V_{OHV} and V_{OLP} are measured with respect to a ground reference near the output under test. Input pulses have the following characteristics: pulse repetition rate 1 MHz, t_r = 3 ns, and skew ≤ 1 ns.

4.1.6.4.2 Output High Disturbance Test

1. The output to be evaluated will be the output whose pin exhibits the largest magnitude of V_{OHV}.
2. Set input conditions so that the output under test is at a high-logic level.
3. Switch the remaining outputs and observe/record the unswitched output induced voltage, V_{OHV}. See Figure 4.1-35.
4. The outputs should be evaluated for standard t_{PLH} and t_{PHL} transitions as well as by taking the devices in and out of 3-state, if applicable.



CH.1 = 1.000 V/div
CH.2 = 1.000 V/div
Timebase = 5.00 ns/div
Delta V = 1.120 V
Vmarker 1 = 3.740 V

Trigger mode : Edge
On Pos. Edge on Chan2
Trigger Levels
Chan2 = 20.00 mV
Holdoff = 70.000 ns

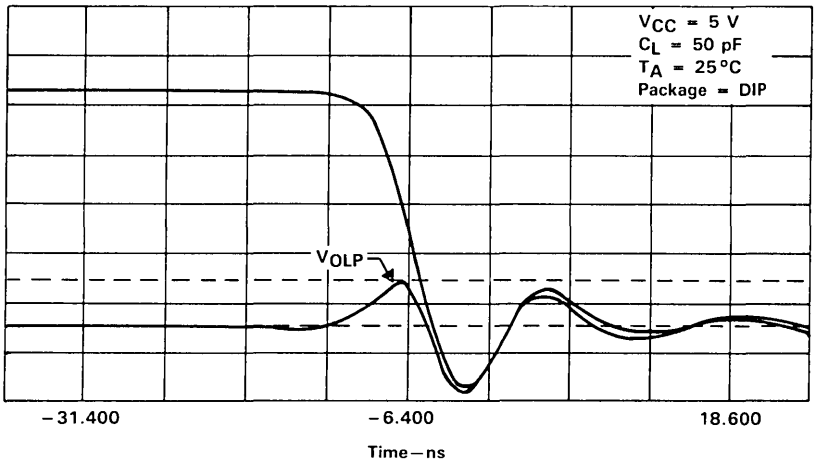
Offset = 2.500 V
Offset = 2.500 V
Delay = 491.900 ns

Vmarker 2 = 4.860 V

Figure 4.1-35. V_{OHV} Nominal Measurement on 74AC11373

4.1.6.4.3 Output Low Disturbance Test

1. The output to be evaluated will be the output whose pin exhibits the largest magnitude of induced voltage.
2. Set input conditions so that the output under test is at a low-logic level.
3. Switch the remaining outputs and observe/record the unswitched output induced voltage, V_{OLP}. See Figure 4.1-36.
4. The outputs should be evaluated for standard t_{PLH} and t_{PHL} transitions as well as by taking the devices in and out of 3-state, if applicable.



CH.1 = 1.000 V/div
CH.2 = 1.000 V/div
Timebase = 5.00 ns/div
CH. 1 Parameters

Trigger mode : Edge
On Pos. Edge on Chan2
Trigger Levels
Chan2 = 20.00 mV
Holdoff = 70.000 ns

Offset = 2.500 V
Offset = 2.500 V
Delay = -6.400 ns
Vmarker 2 = 920.0 V

Figure 4.1-36. V_{OLP} Nominal Measurement on 74AC11373

4.1.6.4.4 Stored Data Integrity

1. Devices with internal storage elements will also have this test performed in addition to the other output glitch evaluation tests. This test will be performed only with worst-case conditions of V_{CC} = 5.5 V, T_A = −55°C.
2. Store a known bit of data in an internal storage element. The element should be the element with the same output as the one used for V_{OHV} and V_{OLP} tests.
3. Switch all remaining outputs, or all outputs if possible, and check to see that data is not destroyed. The method of switching the outputs can vary from device to device. In the case of devices with 3-state outputs, the worst-case test will be to disable the output, pull the output to the opposite logic state of the enabled output, then enable the output. See Figures 4.1-37 and 4.1-38.
4. Storage of both high- and low-level data will be evaluated.

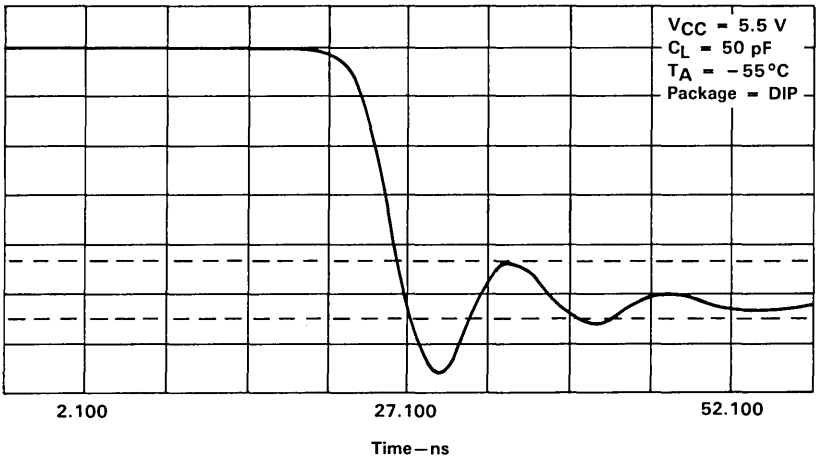
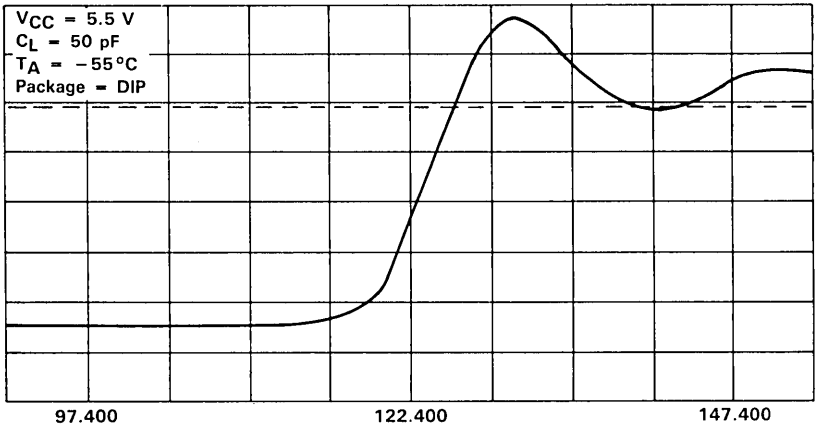


Figure 4.1-37. 74AC11373 Passes Stored Data Test on the High Impedance to Low Transition (ZL)



CH.2 = 1.000 V/div
Timebase = 5.00 ns/div
Delta V = 1.100 V
Vmarker 1 = 4.400 V

Offset = 2.500 V
Delay = 122.400 ns

Vmarker 2 = 5.500 V

Trigger mode : Edge
On Pos. Edge on Trig3
Trigger Levels
Trig3 = 2.000 mV
Holdoff = 70.000 ns

Figure 4.1-38. 74AC11373 Passes Stored Data Test on the High Impedance to High Transition (ZH)

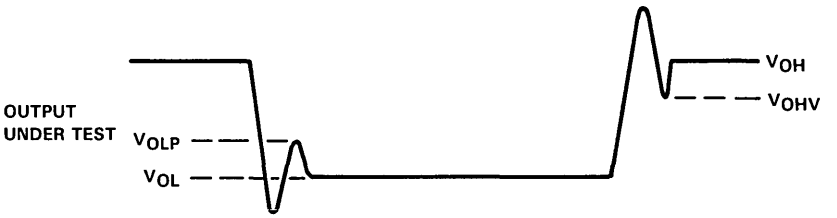
4.1.6.5 Simultaneous Switching Evaluation (Multiple Input Devices, Single or Complementary Outputs)

This simultaneous switching test will be used to determine the magnitude of an active output during multiple input switching of devices with a single or single complementary outputs.

Simultaneous Switching Test Conditions

INPUT VOLTAGES	TEST CONDITIONS	LOAD CIRCUIT	TEST BOARD
V_{IH} = AC 80% V_{CC} ACT 2.5 V	V_{CC} = 5 V T_A = 25°C and V_{CC} = 5.5 V TA = 55°C	per data book spec	ESH 300-24 or ESH 300-28
V_{IL} = AC 20% V_{CC} ACT 0.5 V			

V_{OHV} and V_{OLP} are measured with respect to a ground reference near the output under test. See Figure 4.1-39. Input pulses have the following characteristics: pulse repetition rate 1 MHz, t_r = 3 ns, t_f = 3 ns, and skew ≤ 1 ns.



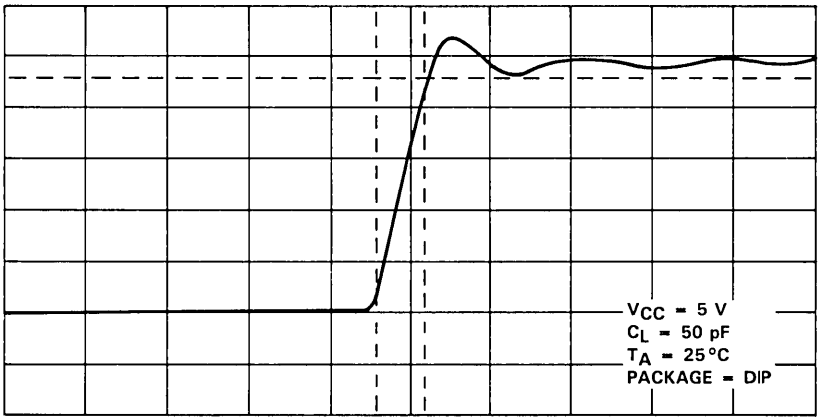
NOTES: A. V_{OHV} and V_{OLP} are measured with respect to ground reference near the output under test.

B. Input pulses have the following characteristics: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 1 ns.

Figure 4.1-39. Dynamic-Output Disturbance Voltage Waveform

4.1.6.5.1 Output Low-to-High Disturbance

Switch N-1 inputs with the Nth input held in the appropriate state to obtain a low-to-high transition on the output. See Figure 4.1-40.



CH.1 = 1.000 V/div
Timebase = 5.00 ns/div
Delta T = 3.070 V
Start = -2.170 ns
Delta V = 440.0 mV
Vmarker 1 = 4.560 V

Offset = 2.000 V
Delay = 0.00000 ns
Stop = 900 ps
Vmarker 2 = 5.000 V

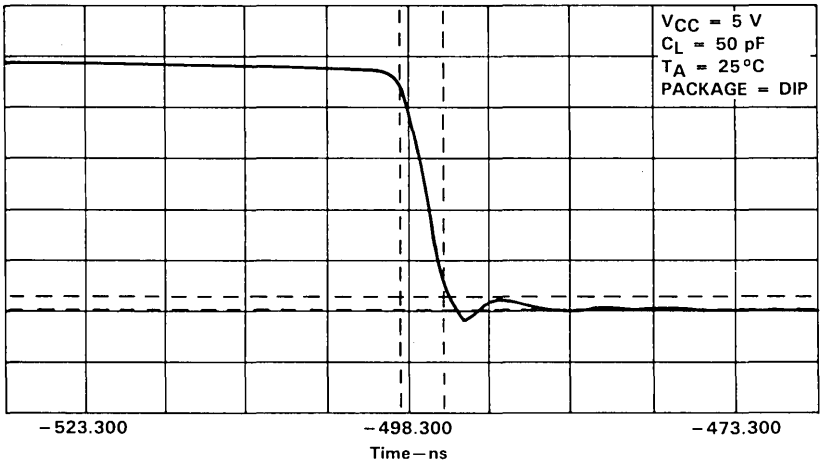
Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 3.200 V
Holdoff = 70.000 ns

7 INPUTS SWITCHING, 1 HIGH

Figure 4.1-40. Dynamic V_{OHV} Nominal Measurement on 74ACT11030

4.1.6.5.2 Output High-to-Low Disturbance

Switch N-1 inputs with the Nth input held in the appropriate state to obtain a high-to-low transition on the output. See Figure 4.1-41.



CH.1 = 1.000 V/div
Timebase = 5.00 ns/div
Delta T = 2.750 ns
Start = −498.810 ns
Delta V = 280.0 mV
Vmarker 1 = 0.000 V

Offset = 2.000 V
Delay = −498.300 ns
Stop = −496.060 ns
Vmarker 2 = 280.0 mV

Trigger mode : Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 3.200 mV
Holdoff = 70.000 ns

7 INPUTS SWITCHING, 1 HIGH

Figure 4.1-41. Dynamic V_{OLP} Nominal Measurement on 74ACT11030

4.1.6.6 ACL Simultaneous Switching Characterization Board Component List

COMPONENT	VENDOR	ORDER NO.
Lab board	ESH Inc. 3020 South Park Drive Tempe, Arizona 85282-3158 (602) 438-1112	LAB-300-24 or LAB-300-28
0.1-μF DIP capacitor and	Newark Electronics 10727 Plano Road Dallas, Texas 75238 (214) 340-3585	65F928
47-pF chip capacitor		81F2006
450-Ω and 50-Ω chip resistor	Erikson Sales 8350 Meadow Road Suite 184 Dallas, Texas 75231 (214) 739-5833	ERJ8EKF-4530
Noninsulated pin jacks and 50 Ω snap-on receptacles and terminators†	Powell Electronics 1933 Westridge Drive Las Colinas Irving, Texas 75062 (214) 550-0547	006-4820 51-043-0000 61-001-0900

† Terminators are converted to 50-Ω terminators in the lab.

The number of units ordered depends upon the number of outputs and inputs a device may have. All outputs have a 47-pF capacitor and a 450-Ω resistor in parallel between the output and ground. The capacitor is placed on the board as close to the device under test as possible on the opposite side of the board. Any output not terminated with a 50-Ω probe must be terminated with a 50-Ω load. Each input or set of inputs driven by a signal pulse generator must be terminated with a single 50-Ω resistor to ground. A 0.1-μF decoupling capacitor is connected between V_{CC} and ground.

4.1.7 Conclusion

Section 4.1 has presented a description of the simultaneous switching issues applicable to high-speed devices and systems. The phenomenon was described with a simple, first-order model to demonstrate the effect package parasitics and device physics have upon V_{OLP} and V_{OHV}. In order to give the designer a feel for system effects on V_{OLP} and V_{OHV}, several factors have been presented. These factors include:

- Power supply variances
- Temperature effects
- Package and pinout issues
- Ac and dc loading effects
- Distributed and lumped capacitive loading at a distance
- Input signal skews, and
- Input signal edge rates.

The purpose of the descriptions and data presented in this section is to allow the system design engineer to recognize the impact simultaneous switching noise may have upon a system. However, it is not realistic for Texas Instruments to totally characterize devices for every possible system environment. The final responsibility for implementing high-speed logic devices lies with the system designer. Texas Instruments has attempted to make this task as simple as possible by using innovative packaging techniques and circuit design techniques in the EPIC™ ACL family.

A standard test methodology has also been presented. This methodology has been developed in conjunction with Philips/Signetics (Texas Instruments codevelopers of the EPIC™ ACL family). This test method has been shown to correlate with the level of switching noise developed by a circuit in a system environment.

4.1.8 References

1. A.J. Rainal, "Computing Inductive Noise of Chip Packages," AT&T Bell Laboratories Technical Journal, Vol 63, No. 1, January 1984.
2. Robert L. Morris and John R. Miller, Editors, "Designing with TTL Integrated Circuits." Texas Instruments Electronic Series.
3. Michael A. Higgs, "AS Load Management," Texas Instruments, Application Report, 1987.
4. Charles Hefner, et al., "One Micron Advanced Logic," Wescon/86, Session 22, November 18-20, 1986.
5. William N. Carr and Jack P. Mize, Editors, "MOS/LSI Design and Application," Texas Instruments Electronic Series.

4.2 Automatic Test Equipment Characterization Procedures†

4.2.1 Introduction

Texas Instruments Advanced CMOS Logic (ACL) family is characterized for operation from −55°C to 125°C. Commercial devices, 74AC and 74ACT, are specified for a temperature range of −40°C to 85°C, and military versions, 54AC and 54ACT, are specified from −55°C to 125°C. Device functionality, ac parametric performance, and dc parametric performance are verified over the specified temperature range. The characterization of ACL devices is performed to create specifications that are accurate and usable from system conception and modeling to prototyping and production usage. The procedures used to characterize ACL are outlined to help the logic user to better understand how data sheet limits are generated.

4.2.2 ACL Automatic Test Equipment Characterization

The magnitude of data necessary to characterize a device for release dictates the use of automatic test equipment (ATE) to keep data acquisition to a period acceptable to allow timely new product introductions. Electrical characteristics such as V_{OH}, V_{OL}, and I_{OH} are easily measured on ATE to within mV or mA of accuracy and repeatability. The problem with using automatic testers to take propagation delay measurements in high-speed logic families is the inaccuracy of the data in comparison to bench propagation delay data.

An example of the problem can be observed by comparing a set of bench lab data for an AC11000 to a data log taken on ATE calibrated to manufacturer's specifications (see Figure 4.2-1). Comparing the lab data to the ATE data in the mean column, it can be seen that there can be a 2.29-ns change between the two in the offset column. The error represented by the 2.29 ns is 29 percent of the 7.92-ns reading that is being measured. Data used to set data sheet limits must have better than ±200 ps of accuracy, as compared to the bench, to provide accurate limits. The 2.29 ns of error proves the ATE, without further calibration, is an unacceptable tool for the characterization of high-speed logic.

To increase the accuracy of the ATE data to ±100 ps, in comparison to lab bench data, a correlation unit is used to further calibrate the ATE measurements. This will allow the characterization engineer to use the ATE for data acquisition.

† Written by A. L. George

DEVICE TYPE = AC11000
UNIT # = 1

READ NUMBER	TEST NUMBER	PIN FROM	PIN TO	LAB DATA	MEAN	OFFSET
01	1011	1	2	6.40 ns	6.45 ns	54.68 ps
02	1011	15	3	6.12 ns	6.79 ns	670.78 ps
03	1011	11	6	6.70 ns	7.05 ns	3.50.82 ps
04	1011	9	7	5.90 ns	5.95 ns	53.09 ps
05	1011	16	2	6.26 ns	6.07 ns	-187.88 ps
06	1011	14	3	6.72 ns	6.55 ns	-167.54 ps
07	1011	10	6	6.18 ns	5.69 ns	-490.86 ps
08	1011	8	7	6.44 ns	6.09 ns	-350.46 ps
09	1012	1	2	7.37 ns	5.83 ns	-1.54 ns
10	1012	15	3	7.89 ns	6.20 ns	-1.69 ns
11	1012	11	6	7.63 ns	6.33 ns	-1.30 ns
12	1012	9	7	7.55 ns	5.69 ns	-1.86 ns
13	1012	16	2	7.92 ns	5.63 ns	-2.29 ns
14	1012	14	3	7.57 ns	6.03 ns	-1.54 ns
15	1012	10	6	7.91 ns	5.72 ns	-2.19 ns
16	1012	8	7	7.23 ns	5.69 ns	-1.54 ns
17	1021	1	2	4.79 ns	5.22 ns	432.35 ps
18	1021	15	3	4.61 ns	5.72 ns	1.11 ns
19	1021	11	6	5.00 ns	5.84 ns	841.94 ps
20	1021	9	7	4.40 ns	4.76 ns	364.73 ps
21	1021	16	2	4.70 ns	4.93 ns	227.72 ps
22	1021	14	3	5.01 ns	5.24 ns	231.01 ps
23	1021	10	6	4.63 ns	4.47 ns	-162.93 ps
24	1021	8	7	4.73 ns	4.75 ns	24.65 ps
25	1022	1	2	5.32 ns	4.50 ns	-821.93 ps
26	1022	15	3	5.55 ns	4.91 ns	-642.04 ps
27	1022	11	6	5.45 ns	5.04 ns	-412.62 ps
28	1022	9	7	5.23 ns	4.28 ns	-947.60 ps
29	1022	16	2	5.55 ns	4.32 ns	-1.23 ns
30	1022	14	3	5.45 ns	4.60 ns	-853.85 ps
31	1022	10	6	5.51 ns	4.38 ns	-1.13 ns
32	1022	8	7	5.13 ns	4.26 ns	-872.10 ps
33	1031	1	2	4.55 ns	5.05 ns	499.45 ps
34	1031	15	3	4.41 ns	5.57 ns	1.16 ns
35	1031	11	6	4.75 ns	5.64 ns	894.12 ps
36	1031	9	7	4.19 ns	4.61 ns	415.01 ps

Figure 4.2-1. Bench Lab Data for an AC11000

DEVICE TYPE = AC11000
UNIT # = 1

READ NUMBER	TEST NUMBER	PIN FROM	PIN TO	LAB DATA	MEAN	OFFSET
37	1031	16	2	4.49 ns	4.78 ns	288.25 ps
38	1031	14	3	4.76 ns	5.08 ns	315.43 ps
39	1031	10	6	4.40 ns	4.29 ns	−110.23 ps
40	1031	8	7	4.52 ns	4.56 ns	35.36 ps
41	1032	1	2	4.98 ns	4.27 ns	−714.91 ps
42	1032	15	3	4.20 ns	4.67 ns	−527.96 ps
43	1032	11	6	5.10 ns	4.84 ns	−263.37 ps
44	1032	9	7	4.88 ns	4.01 ns	−870.14 ps
45	1032	16	2	5.18 ns	4.09 ns	−1.09 ns
46	1032	14	3	5.11 ns	4.33 ns	−799.07 ps
47	1032	10	6	5.12 ns	4.14 ns	−978.88 ps
48	1032	8	7	4.81 ns	4.02 ns	−789.48 ps
49	1041	1	2	4.44 ns	4.93 ns	486.36 ps
50	1041	15	3	4.30 ns	5.46 ns	1.16 ns
51	1041	11	6	4.61 ns	5.49 ns	878.80 ps
52	1041	9	7	4.06 ns	4.49 ns	433.65 ps
53	1041	16	2	4.39 ns	4.66 ns	269.56 ps
54	1041	14	3	4.65 ns	4.96 ns	306.74 ps
55	1041	10	6	4.29 ns	4.16 ns	−132.11 ps
56	1041	8	7	4.35 ns	4.40 ns	47.11 ps
57	1042	1	2	4.67 ns	4.06 ns	−605.66 ps
58	1042	15	3	4.88 ns	4.47 ns	−411.63 ps
59	1042	11	6	4.80 ns	4.67 ns	−130.42 ps
60	1042	9	7	4.56 ns	3.76 ns	−799.25 ps
61	1042	16	2	4.83 ns	3.87 ns	−958.48 ps
62	1042	14	3	4.79 ns	4.08 ns	−706.70 ps
63	1042	10	6	4.81 ns	3.92 ns	−885.75 ps
64	1042	8	7	4.50 ns	3.82 ns	−677.30 ps

Figure 4.2-1. Bench Lab Data for an AC11000 (Continued)

4.2.3 Correlation Unit Concept

The correlation unit is a device that is fully bench tested for ac parametric tests. Universal 50-Ω multilayer lab boards, which can be configured for all device types, are used to take the data on the bench. The unit(s) tested on the bench then become the ac delay time standard(s) for that device type. The data from the bench is stored in a file compatible with the ATE test program that contains the same propagation delay tests performed on the bench.

The correlation device and file can then be used to check the accuracy of the ATE and, more importantly, make the ac parametric readings comparable to bench data. Two necessary characteristics of the ATE make correction possible. The ATE must read ac parameters repeatedly, and the measurement error, as compared to the bench, must be consistent from device to device. Texas Instruments developed software, DEVOFF, checks multiple readings of the same transition to verify a standard deviation of less than 50 ps (see Figure 4.2-2). The standard deviations of the measurements are no greater than 15 ps. This shows the ATE is reading repeatability and is acceptable for characterization measurements.

DEVICE TYPE = AC11000
UNIT # = 1

READ NUMBER	TEST NUMBER	PIN FROM	PIN TO	MIN READING	MAX READING	DELTA	MEAN	STANDARD DEVIATION
01	1011	1	2	6.44 ns	6.46 ns	14.65 ps	6.45 ns	7.08 ps
02	1011	15	3	6.77 ns	6.80 ns	29.31 ps	6.79 ns	8.32 ps
03	1011	11	6	7.04 ns	7.06 ns	14.65 ps	7.05 ns	7.08 ps
04	1011	9	7	5.95 ns	5.95 ns	0.00 ps	5.95 ns	0.00 ps
05	1011	16	2	6.06 ns	6.08 ns	14.65 ps	6.07 ns	6.18 ps
06	1011	14	3	6.54 ns	6.57 ns	29.31 ps	6.55 ns	10.81 ps
07	1011	10	6	5.68 ns	5.69 ns	14.65 ps	5.69 ns	6.18 ps
08	1011	8	7	6.07 ns	6.10 ns	29.31 ps	6.09 ns	6.91 ps
09	1012	1	2	5.82 ns	5.83 ns	14.65 ps	5.83 ns	4.63 ps
10	1012	15	3	6.19 ns	6.22 ns	29.31 ps	6.20 ns	9.27 ps
11	1012	11	6	6.31 ns	6.34 ns	29.31 ps	6.33 ns	10.36 ps
12	1012	9	7	5.67 ns	5.71 ns	43.96 ps	5.69 ns	11.56 ps
13	1012	16	2	5.62 ns	5.64 ns	29.31 ps	5.63 ns	8.32 ps
14	1012	14	3	6.02 ns	6.05 ns	29.31 ps	6.03 ns	8.32 ps
15	1012	10	6	5.70 ns	5.73 ns	29.31 ps	5.72 ns	10.25 ps
16	1012	8	7	5.67 ns	5.70 ns	29.31 ps	5.69 ns	8.32 ps
17	1021	1	2	5.20 ns	5.23 ns	29.31 ps	5.22 ns	10.25 ps
18	1021	15	3	5.69 ns	5.73 ns	43.96 ps	5.72 ns	13.82 ps
19	1021	11	6	5.82 ns	5.85 ns	29.31 ps	5.84 ns	9.27 ps
20	1021	9	7	4.74 ns	4.78 ns	43.96 ps	4.76 ns	14.57 ps
21	1021	16	2	4.90 ns	4.95 ns	43.96 ps	4.93 ns	12.06 ps
22	1021	14	3	5.22 ns	5.26 ns	43.96 ps	5.24 ns	12.36 ps
23	1021	10	6	4.45 ns	4.48 ns	29.31 ps	4.47 ns	10.25 ps
24	1021	8	7	4.74 ns	4.77 ns	29.31 ps	4.75 ns	8.32 ps
25	1022	1	2	4.48 ns	4.51 ns	29.31 ps	4.50 ns	6.91 ps
26	1022	15	3	4.88 ns	4.93 ns	43.96 ps	4.91 ns	11.56 ps
27	1022	11	6	5.02 ns	5.05 ns	29.31 ps	5.04 ns	8.32 ps

Figure 4.2-2. Standard Deviation Verifications

DEVICE TYPE = AC11000
UNIT # = 1

READ NUMBER	TEST NUMBER	PIN FROM	PIN TO	MIN READING	MAX READING	DELTA	MEAN	STANDARD DEVIATION
28	1022	9	7	4.26 ns	4.29 ns	29.31 ps	4.28 ns	10.25 ps
29	1022	16	2	4.31 ns	4.33 ns	14.65 ps	4.32 ns	4.63 ps
30	1022	14	3	4.58 ns	4.61 ns	29.31 ps	4.60 ns	6.91 ps
31	1022	10	6	4.36 ns	4.38 ns	14.65 ps	4.38 ns	4.63 ps
32	1022	8	7	4.25 ns	4.27 ns	14.65 ps	4.26 ns	7.08 ps
33	1031	1	2	5.04 ns	5.05 ns	14.65 ps	5.05 ns	6.18 ps
34	1031	15	3	5.54 ns	5.57 ns	29.31 ps	5.57 ns	10.25 ps
35	1031	11	6	5.62 ns	5.65 ns	29.31 ps	5.64 ns	9.89 ps
36	1031	9	7	4.59 ns	4.62 ns	29.31 ps	4.61 ns	11.96 ps
37	1031	16	2	4.76 ns	4.79 ns	29.31 ps	4.78 ns	10.36 ps
38	1031	14	3	5.06 ns	5.09 ns	29.31 ps	5.08 ns	9.89 ps
39	1031	10	6	4.27 ns	4.30 ns	29.31 ps	4.29 ns	12.06 ps
40	1031	8	7	4.54 ns	4.57 ns	29.31 ps	4.56 ns	9.89 ps
41	1032	1	2	4.25 ns	4.28 ns	29.31 ps	4.27 ns	8.32 ps
42	1032	15	3	4.66 ns	4.68 ns	14.65 ps	4.67 ns	7.08 ps
43	1032	11	6	4.83 ns	4.85 ns	14.65 ps	4.84 ns	7.57 ps
44	1032	9	7	4.00 ns	4.03 ns	29.31 ps	4.01 ns	9.27 ps
45	1032	16	2	4.08 ns	4.09 ns	14.65 ps	4.09 ns	7.08 ps
46	1032	14	3	4.32 ns	4.33 ns	14.65 ps	4.33 ns	4.63 ps
47	1032	10	6	4.13 ns	4.14 ns	14.65 ps	4.14 ns	4.63 ps
48	1032	8	7	4.02 ns	4.03 ns	14.65 ps	4.02 ns	4.63 ps
49	1041	1	2	4.91 ns	4.94 ns	29.31 ps	4.93 ns	12.36 ps
50	1041	15	3	5.44 ns	5.47 ns	29.31 ps	5.46 ns	9.77 ps
51	1041	11	6	5.47 ns	5.50 ns	29.31 ps	5.49 ns	10.81 ps
52	1041	9	7	4.47 ns	4.50 ns	29.31 ps	4.49 ns	10.25 ps
53	1041	16	2	4.65 ns	4.67 ns	14.65 ps	4.66 ns	7.57 ps
54	1041	14	3	4.94 ns	4.97 ns	29.31 ps	4.96 ns	9.27 ps
55	1041	10	6	4.15 ns	4.17 ns	14.65 ps	4.16 ns	7.08 ps
56	1041	8	7	4.39 ns	4.40 ns	14.65 ps	4.40 ns	7.72 ps
57	1042	1	2	4.06 ns	4.07 ns	14.65 ps	4.06 ns	7.57 ps
58	1042	15	3	4.46 ns	4.47 ns	14.65 ps	4.47 ns	6.18 ps
59	1042	11	6	4.67 ns	4.67 ns	0.00 ps	4.67 ns	0.00 ps
60	1042	9	7	3.75 ns	3.76 ns	14.65 ps	3.76 ns	6.18 ps
61	1042	16	2	3.87 ns	3.87 ns	0.00 ps	3.87 ns	0.00 ps
62	1042	14	3	4.08 ns	4.08 ns	0.00 ps	4.08 ns	0.00 ps
63	1042	10	6	3.92 ns	3.94 ns	14.65 ps	3.92 ns	4.63 ps
64	1042	8	7	3.81 ns	3.83 ns	14.65 ps	3.82 ns	7.57 ps

Figure 4.2-2. Standard Deviation Verifications (Continued)

To show the improvement in accuracy, the AC11000 is retested after the ATE is calibrated using a correlation unit (see Figure 4.2-3). Comparing the lab data to the ATE data (offset log column), the largest absolute change is 21.98 ps. The acceptable criteria delta is 50 ps. The use of this technique has cut the maximum error for this device from 2.29 ns to 21.98 ps. The ATE can now be used to take characterization data on 10-times-larger groups of devices than could be done on the bench, in one-tenth the time, and obtain accurate results.

DEVICE TYPE = AC11000
UNIT # = 1

READ NUMBER	TEST NUMBER	PIN FROM	PIN TO	OFFSET/ LOG	LAB DATA	DELTA
01	1011	1	2	6.40 ns	6.40 ns	4.40 ps
02	1011	15	3	6.13 ns	6.12 ns	13.19 ps
03	1011	11	6	6.70 ns	6.70 ns	4.40 ps
04	1011	9	7	5.90 ns	5.90 ns	−0.00 ps
05	1011	16	2	6.26 ns	6.26 ns	2.93 ps
06	1011	14	3	6.72 ns	6.72 ns	−1.47 ps
07	1011	10	6	6.18 ns	6.18 ns	2.93 ps
08	1011	8	7	6.44 ns	6.44 ns	0.00 ps
09	1012	1	2	7.36 ns	7.37 ns	−13.19 ps
10	1012	15	3	7.89 ns	7.89 ns	−2.93 ps
11	1012	11	6	7.62 ns	7.63 ns	−7.33 ps
12	1012	9	7	7.54 ns	7.55 ns	−11.72 ps
13	1012	16	2	7.92 ns	7.92 ns	−1.46 ps
14	1012	14	3	7.57 ns	7.57 ns	1.47 ps
15	1012	10	6	7.90 ns	7.91 ns	−5.86 ps
16	1012	8	7	7.22 ns	7.23 ns	−13.19 ps
17	1021	1	2	4.78 ns	4.79 ns	−8.79 ps
18	1021	15	3	4.61 ns	4.61 ns	0.00 ps
19	1021	11	6	4.98 ns	5.00 ns	−17.58 ps
20	1021	9	7	4.39 ns	4.40 ns	−13.19 ps
21	1021	16	2	4.69 ns	4.70 ns	−10.26 ps
22	1021	14	3	5.00 ns	5.01 ns	−8.79 ps
23	1021	10	6	4.62 ns	4.63 ns	−5.86 ps
24	1021	8	7	4.72 ns	4.73 ns	−13.19 ps
25	1022	1	2	5.31 ns	5.32 ns	−14.65 ps
26	1022	15	3	5.54 ns	5.55 ns	−11.72 ps
27	1022	11	6	5.45 ns	5.45 ns	−1.47 ps
28	1022	9	7	5.22 ns	5.23 ns	−5.86 ps

Figure 4.2-3. Retest for Standard Deviation Verifications

DEVICE TYPE = AC11000
UNIT # = 1

READ NUMBER	TEST NUMBER	PIN FROM	PIN TO	OFFSET/ LOG	LAB DATA	DELTA
29	1022	16	2	5.54 ns	5.55 ns	−13.19 ps
30	1022	14	3	5.44 ns	5.45 ns	−14.65 ps
31	1022	10	6	5.50 ns	5.51 ns	−13.19 ps
32	1022	8	7	5.13 ns	5.13 ns	−4.40 ps
33	1031	1	2	4.54 ns	4.55 ns	−11.72 ps
34	1031	15	3	4.40 ns	4.41 ns	−8.79 ps
35	1031	11	6	4.74 ns	4.75 ns	−10.26 ps
36	1031	9	7	4.19 ns	4.19 ns	0.00 ps
37	1031	16	2	4.47 ns	4.49 ns	−21.98 ps
38	1031	14	3	4.74 ns	4.76 ns	−19.05 ps
39	1031	10	6	4.40 ns	4.40 ns	−4.40 ps
40	1031	8	7	4.50 ns	4.52 ns	−19.05 ps
41	1032	1	2	4.98 ns	4.98 ns	−1.47 ps
42	1032	15	3	5.19 ns	5.20 ns	−10.26 ps
43	1032	11	6	5.09 ns	5.10 ns	−5.86 ps
44	1032	9	7	4.87 ns	4.88 ns	−11.72 ps
45	1032	16	2	5.18 ns	5.18 ns	4.40 ps
46	1032	14	3	5.10 ns	5.11 ns	−13.19 ps
47	1032	10	6	5.11 ns	5.12 ns	−13.19 ps
48	1032	8	7	4.81 ns	4.81 ns	−1.47 ps
49	1041	1	2	4.43 ns	4.44 ns	−5.86 ps
50	1041	15	3	4.30 ns	4.30 ns	−0.00 ps
51	1041	11	6	4.59 ns	4.61 ns	−16.12 ps
52	1041	9	7	4.50 ns	4.06 ns	−5.86 ps
53	1041	16	2	4.38 ns	4.39 ns	−5.86 ps
54	1041	14	3	4.65 ns	4.65 ns	−2.93 ps
55	1041	10	6	4.29 ns	4.29 ns	−4.40 ps
56	1041	8	7	4.34 ns	4.35 ns	−7.33 ps
57	1042	1	2	4.66 ns	4.67 ns	−5.86 ps
58	1042	15	3	4.88 ns	4.88 ns	2.93 ps
59	1042	11	6	4.80 ns	4.80 ns	0.00 ps
60	1042	9	7	4.56 ns	4.56 ns	2.93 ps
61	1042	16	2	4.83 ns	4.83 ns	0.00 ps
62	1042	14	3	4.79 ns	4.79 ns	−0.00 ps
63	1042	10	6	4.81 ns	4.81 ns	−1.47 ps
64	1042	8	7	4.49 ns	4.50 ns	−8.79 ps

Figure 4.2-3. Retest for Standard Deviation Verifications (Continued)

4.2.4 Characterization Device Selection

The Texas Instruments ACL characterization material is selected from at least two separately started front-end lots. Slices from within each lot are selected for assembly, based on process, to show maximum variability within the lot. The data acquired from at least two lots are targeted to illustrate lot-to-lot variation. Traditionally, one lot of material has been used to set data sheet limits for logic devices. The high-speed propagation delays of ACL, and the need for data sheets representative of device operation, requires selection of material that includes manufacturing variations to set accurate data sheet limits.

4.2.5 Data Acquisition

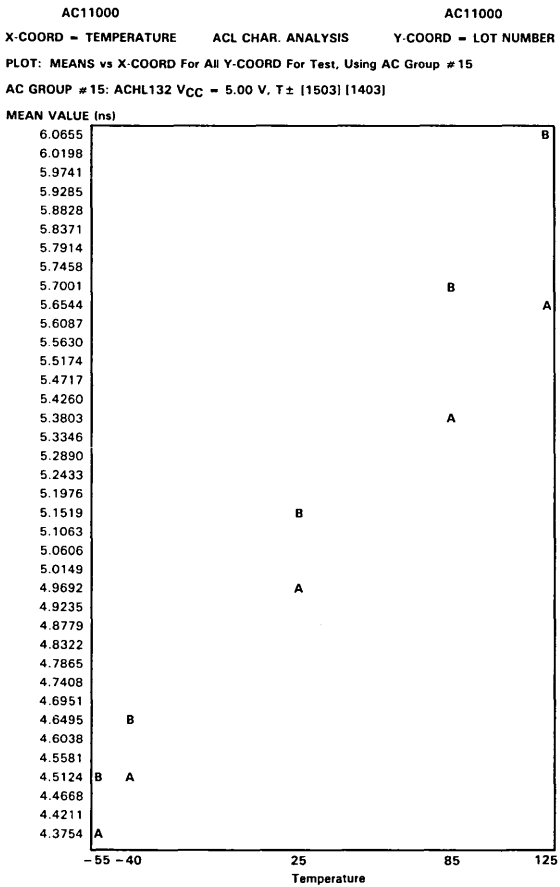
The ATE is calibrated for a device type using the correlation device and file. A verification of repeatability for performing propagation delays is performed using Texas Instruments software, DEVOFF. The limit for acceptance is ±50 ps. Failure to meet this test would constitute a recalibration to manufacturer's specifications and restart of the correlation process.

The selected groups of material from two front-end lots are tested at −55 °C, −40 °C, 25 °C, 85 °C, 125 °C. The ATE programs check the operational V_{CC} range of 3 V to 5.5 V for each data sheet parameter, where applicable. Tests that cannot be performed accurately enough on the ATE to set data sheet limits such as f_{max} and t_w are performed on the lab bench.

4.2.6 Characterization Data Analysis

Texas Instruments ACL characterization is done using a Texas Instruments developed data base manipulation program (CCAP) designed to extract graphical and statistical data. Data for a parametric test using multiple groups or lots of material can be plotted over temperature (see Figure 4.2-4). The data shown represents the t_{PLH} of the AC11000 for two lots of material over temperature at 5 V. The graph shows the nearly linear variance in propagation delays across temperature for each group of devices. The summary data shows statistical information for each lot of data.

The data base also provides for extracting individual readings for a specific device and temperature or groups of readings for a defined parameter and temperature. Figure 4.2-5 is a summary of all readings for Ycoord(lot) #6312542 at 25 °C. This illustrates that there were 30 devices in the sample and two pin pairs: pin 15 to pin 3 and pin 14 to pin 3. This is very useful for analyzing anomalies in the data. If readings fall outside of the normal distribution, they can be easily detected in this format.



SUMMARY: OVER ALL X-COORDs & Y-CORDs TEST :ACHL, USING AC GROUP #15

X-COORD	Y-COORD	MEAN READ	STD DEV	MEAN + 3SD	MEAN - 3SD	HIGH READ	LOW READ	#RDS
-55	#6289002	4.3754 ns	0.0673 ns	4.5775 ns	4.1734 ns	4.5058 ns	4.2344 ns	60
-55	#6312542	4.4945 ns	0.0504 ns	4.6458 ns	4.3431 ns	4.5710 ns	4.3740 ns	60
-40	#6289002	4.4969 ns	0.0696 ns	4.7058 ns	4.2881 ns	4.6375 ns	4.3368 ns	60
-40	#6312542	4.6286 ns	0.0517 ns	4.7839 ns	4.4733 ns	4.7174 ns	4.5058 ns	60
25	#6289002	4.9862 ns	0.0766 ns	5.2162 ns	4.7562 ns	5.1351 ns	4.8344 ns	60
25	#6312542	5.1460 ns.	0.0641 ns	5.3383 ns	4.9536 ns	5.2588 ns	5.0034 ns	60
85	#6289002	5.3948 ns	0.0988 ns	5.6913 ns	5.0982 ns	5.6912 ns	5.2149 ns	60
85	#6312542	5.6794 ns	0.1118 ns	6.0150 ns	5.3438 ns	5.8735 ns	5.4570 ns	60
125	#6289002	5.6538 ns	0.1059 ns	5.9718 ns	5.3358 ns	5.8589 ns	5.4278 ns	60
125	#6312542	6.0655 ns	0.1609 ns	6.5486 ns	5.5825 ns	6.3565 ns	5.7644 ns	60

THE FOLLOWING ARE OVERALL STATISTICS CALCULATED FROM THE ABOVE MEANS

MEAN:	5.0921 ns;	STANDARD DEVIATION:	0.5919 ns
LOW VALUE:	4.3754 ns;	HIGH VALUE:	6.0655 ns
LOWER LIMIT:	0.4994 ns;	UPPER LIMIT:	36.9545 ns

THE DATA WAS NOT SCREENED

Figure 4.2-4. Parametric Test of Multiple Groups over Temperature

The data is reduced and extrapolated to account for process variations not present in the characterization devices. The general equations for determining ac parametric minimum and maximum profiles are:

ac max profile = mean + 3 standard deviations + extrapolation value + ATE tolerance

ac min profile = mean − 3 standard deviations − extrapolation value − ATE tolerance

The extrapolation value is a factor to account for material that does exhibit the worst-case manufacturing variations. As an example, to generate a 5-V, 25°C profile from Figure 4.2-5, the mean + 3std is taken from the slower lot (#6312542).

5-V t_{PLH} max profile = 5.34 ns + extrapolation value + ATE tolerance

Assuming this is worst-case process material, for this calculation, the extrapolation value is not needed. Taking the ATE tolerance stated above of 50 ps, a maximum profile is calculated.

5-V t_{PLH} max profile = 5.34 ns + 0 ns + 0.05 ns = 5.39 ns

Once they are determined, the ac parametric minimum and maximum profiles are used to calculate the data sheet minimum and maximum limits.

The dc parameters are checked against the ACL dc data sheet that was established at the inception of the family. The limits are reviewed and tested for accuracy and manufacturability prior to finalization of the data sheet. An example of a dc V_{OH} at 4.5 V and 24 mA is shown in Figure 4.2-6. This ensures ACL data sheet limits are representative of the EPIC™ process and will not require changes in the future due to movements of the process within manufacturing limits.

4.2.7 Limit Verification

The finalization of an ACL data sheet is contingent on testing production quantities of a third front-end lot of devices using the proposed data sheet limits. Any device that fails the limits is evaluated and verified. The sample must pass 100 percent data sheet across temperature before the limits are finalized. This is another check to be sure the devices that the customer receives over the life of the family match the published data sheet.

AC11000 AC11000

X-COORD = TEMPERATURE ACL CHAR. ANALYSIS Y-COORD = LOT NUMBER

STATISTICAL SUMMARY FOR :ACHL, X-COORD 25, Y-COORD B, USING AC GROUP #15

STATISTICS WERE CALCULATED FROM THE FOLLOWING UNITS: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30

THE FOLLOWING READS WERE USED:

ACHL 32 1503: ACHL 32 1403:

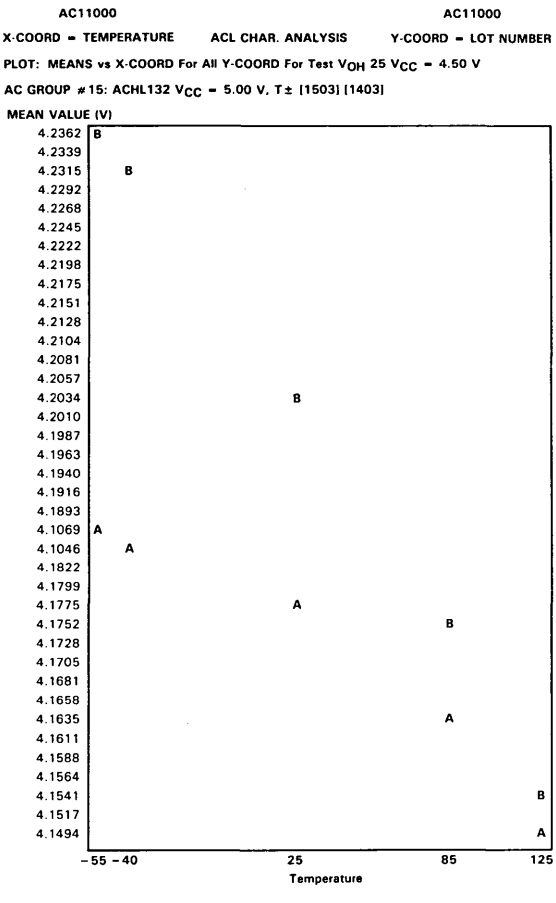
TOTAL SAMPLE SIZE: 60 READS

	ACHL 32 1503:	ACHL 32 1403:		ACHL 32 1503:	ACHL 32 1403:
1	5.9326	5.0540	16	5.1936	5.2442
2	5.0473	5.0832	17	5.1936	5.2442
3	5.0619	5.0979	18	5.2229	5.2588
4	5.0326	5.0686	19	5.1351	5.1857
5	5.0765	5.0979	20	5.1497	5.2003
6	5.1351	5.1564	21	5.1643	5.2149
7	5.0034	5.0686	22	5.1643	5.2442
8	5.0619	5.0979	23	5.1204	5.1857
9	5.0765	5.1418	24	5.1497	5.2296
10	5.1058	5.1418	25	5.1790	5.2442
11	5.1790	5.2588	26	5.1204	5.1710
12	5.1204	5.2003	27	5.1204	5.1857
13	5.1497	5.2003	28	5.0619	5.1125
14	5.1643	5.2296	29	5.1058	5.1564
15	5.1497	5.2149	30	5.1204	5.1710

MEAN:	5.1460 ns;	STANDARD DEVIATION:	0.0641 ns
LOW VALUE:	5.0034 ns;	HIGH VALUE:	5.2588 ns
LOWER LIMIT:	0.4994 ns;	UPPER LIMIT:	36.9545 ns

THE DATA WAS NOT SCREENED

Figure 4.2-5. Summary of All Y Coord (lot #6312542) Readings at 25°C



SUMMARY: OVER ALL X-COORDs & Y-CORDs FOR TEST V_{OH} 25

X-COORD	Y-COORD	MEAN READ	STD DEV	MEAN + 3SD	MEAN − 3SD	HIGH READ	LOW READ	#RDS
−55	#6289002	4.1870 V	0.0136 V	4.2278 V	4.1462 V	4.2123 V	4.1552 V	120
−55	#6312542	4.2362 V	0.0066 V	4.2562 V	4.2163 V	4.2557 V	4.2178 V	120
−40	#6289002	4.1856 V	0.0136 V	4.2264 V	4.1447 V	4.2123 V	4.1552 V	120
−40	#6312542	4.2305 V	0.0067 V	4.2506 V	4.2103 V	4.2507 V	4.2128 V	120
25	#6289002	4.1773 V	0.0131 V	4.2167 V	4.1379 V	4.2056 V	4.1502 V	120
25	#6312542	4.2031 V	0.0069 V	4.2238 V	4.1825 V	4.2206 V	4.1827 V	120
85	#6289002	4.1633 V	0.0131 V	4.2025 V	4.1241 V	4.1923 V	4.1351 V	120
85	#6312542	4.1754 V	0.0075 V	4.1978 V	4.1529 V	4.1905 V	4.1526 V	120
125	#6289002	4.1494 V	0.0138 V	4.1909 V	4.1079 V	4.1773 V	4.1176 V	120
125	#6312542	4.1549 V	0.0079 V	4.1785 V	4.1313 V	4.1727 V	4.1326 V	120

THE FOLLOWING ARE OVERALL STATISTICS CALCULATED FROM THE ABOVE MEANS

MEAN:	4.1863 V;	STANDARD DEVIATION:	0.0295 V
LOW VALUE:	4.1494 V;	HIGH VALUE:	4.2362 V
LOWER LIMIT:	3.7036 V;	UPPER LIMIT:	4.5545 V

THE DATA WAS NOT SCREENED

Figure 4.2-6. V_{OH} at 4.5 V vs Temperature

4.2.8 Summary

The Texas Instruments EPIC™ ACL Family is characterized to yield data sheets that minimize the need for derating curves or multiplication factors. The ac and dc parametric characteristics are given in each device function data sheet. The techniques used to characterize the family guarantees operation under data-sheet-stated conditions and guarantees that published ACL data sheets are representative of the production devices.

5 PCB and System-Level Considerations

5.1 EPIC™ Advanced CMOS Logic System Evaluation Board†

5.1.1 Introduction

The demand for higher-performance End Equipment forces component manufacturers to push the limits of technology. Designers want high-speed and low-power components that maintain or improve system reliability. Advanced CMOS Logic (ACL) offers high speed and low power to designers. Bipolar speeds, combined with low-power CMOS, invite previous users of Bipolar TTL Logic and HCMOS Logic to employ the new ACL families. To maintain system reliability, designers need to be aware of system parameters that have an effect on device performance. Also, the designer should be aware that differences exist between vendors of Advanced CMOS Logic.

When implementing a design using any high-speed logic family, several areas must be considered, or system performance may be compromised. A System Evaluation Board is used by Texas Instruments to study the system parameters of Advanced CMOS Logic. This test board simulates a variety of system environments under which a buffer or latch may be tested.

This document illustrates the effects of simultaneous switching outputs on system integrity along with various board parameters and their effect on system performance. The logic families in this study include Texas Instruments EPIC™ ACL and two vendors of conventional end-pin Advanced CMOS Logic, HCMOS, ALS and AS.

5.1.2 Description of System and Test Methods

The System Evaluation Board (see Figure 5.1-1) is designed to emulate a test environment typical of many system designs. The architecture simulates a Motherboard configuration which sends data and control lines through a buffer to a receiving device. On the board, seven data lines and one control line are buffered together through an octal buffer that will be the device under test. The data and control lines are received by an accumulator which keeps a running sum of the data patterns.

EPIC is a trademark of Texas Instruments Incorporated.
†Written by M. Higgs and P.G. Karr.

The evaluation board is a four-layer board with a 1-oz thick, copper ground and V_{CC} planes. All lines on the board correspond to a 50-Ω characteristic impedance. The components on the board are all CMOS technology with the exception of a TTL level 74F273 device. The 74F273 flip-flop is the receiving device from the test buffer. This presents the case of a CMOS device feeding a TTL device where mixing technologies may cause increased sensitivity to system noise.

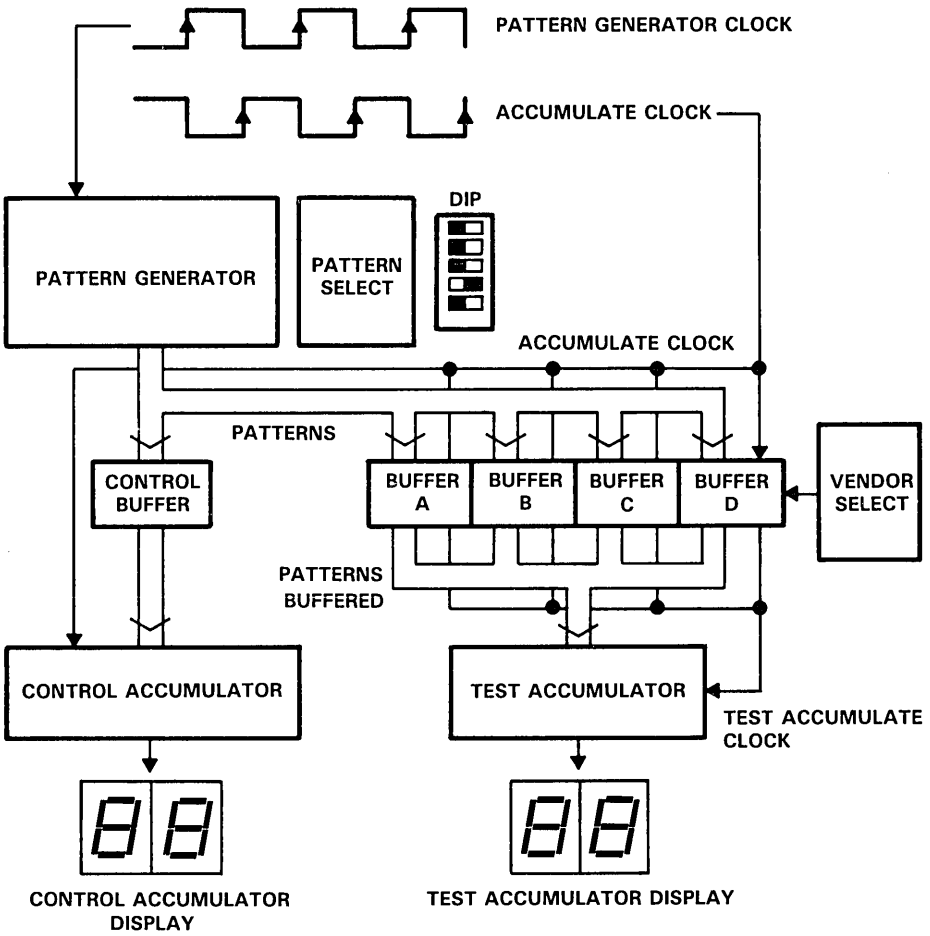


Figure 5.1-1. System Evaluation Board Block Diagram

5.1.2.1 Flow of Data on Board

To generate a 7-bit pattern (see Figure 5.1-1), the Pattern Generator (an EPROM with stored patterns) is clocked once per cycle. The 7-bit pattern is presented to the Control Buffer (HC373) and also to the buffer under test. Buffer A, B, C, or D may be selected as the Test Buffer with the Vendor Select Switch. The Control Buffer presents the data to the Control Accumulator. Similarly, the Test Buffer presents its data to the Test Accumulator. When clocked, each accumulator adds the buffered 7-bit data pattern to the running sum already in the accumulator.

5.1.2.2 Control Lines on Board

An accumulator clock is out of phase with the Pattern Generator Clock (see Figure 5.1-1). Each accumulator loads when its respective clock line is pulsed. This timing scheme alternately generates new data and then sends a triggering pulse on the accumulator clock line to add the new data to the running sum.

The Control Accumulator Clock line comes directly from the clock. This ensures the Control Accumulator is triggered only once per cycle. The Test Accumulator Clock line is passed through the test buffers with the data lines.

5.1.2.3 Simultaneous Switching

In any system, it is common that data lines to a buffer switch simultaneously. The Pattern Generator produces repeating patterns that switch all data lines simultaneously (see Section 5.1.4). As this happens, the buffer being tested may be affected by a phenomenon known as ground bounce resulting in a varying Peak low-level output voltage V_{OLP} (see Section 5.1.5 for definitions). Ground bounce occurs when the ground of the buffer changes in voltage (glitches) and affects any output lines that are supposed to be at the low state. If the output voltage of the Test Buffer glitches (measured as V_{OLP}) and exceeds the threshold voltage of the accumulator clock, then the Test Accumulator will add the data twice instead of once.

Figure 5.1-2 shows the input voltage pulse duration and amplitude necessary to trigger a 74F D-type flip-flop. The 74F273 device exhibits similar characteristics. A V_{OLP} level of 1.5 V is identified as the threshold input level at which the 74F273 device used on the System Evaluation Board will switch from low to high.

5.1.2.4 Visual Check of System Integrity

The running sum is displayed for both the Control Accumulator and the Test Accumulator. If the buffer under test behaves correctly, the two displays will match. If the two sums are different, the test buffer has glitched and the system has failed. A single failure is all it takes for any system to crash.

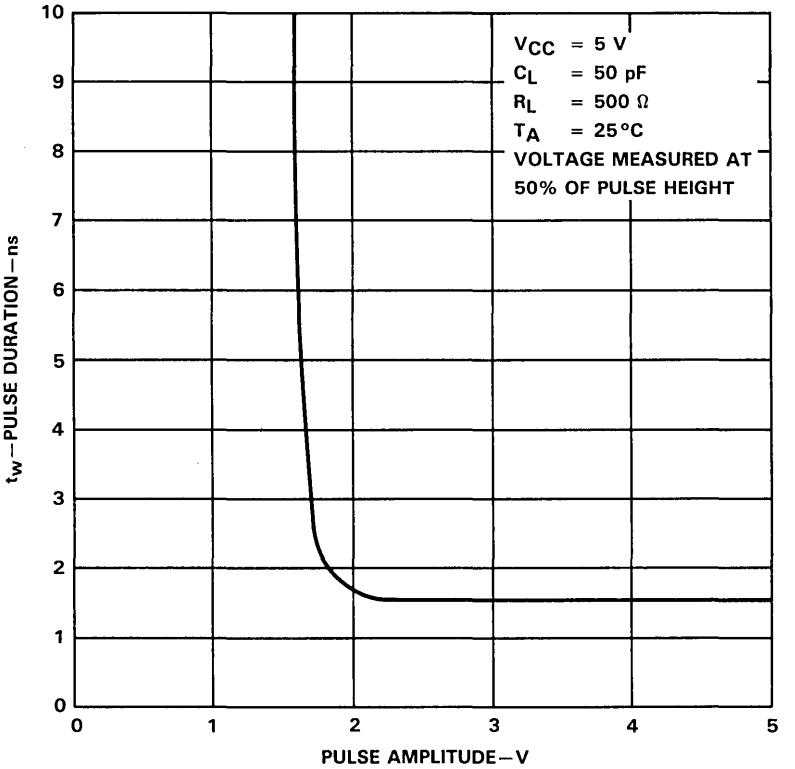


Figure 5.1-2. Pulse Duration vs Amplitude

5.1.2.5 Variation of System Evaluation Board Parameters

A 9-inch, 50-Ω transmission line may be added between the test buffer and the accumulator. Also, capacitors may be added to the transmission line to simulate a high fan-out environment.

Four different data patterns (see Section 5.1.4) may be selected by changing the DIP switch setting. By testing with various patterns, the effects they have on V_{OLP} can be studied. A frequency control switch is also placed on the board. The board may be tested at a clock speed of 1 MHz or 2 Hz to determine the effects of frequency on V_{OLP}.

5.1.3 Evaluation

For all evaluations, a 10-A power supply is used, and the system ground plane is used as reference. A Hewlett-Packard 54110A oscilloscope is used to measure V_{OLP} from the Test Accumulate Clock line. Oscilloscope waveforms

of the evaluations are shown in Figures 5.1-10 through 5.1-13. Unless otherwise noted, V_{CC} is 5.5 V, the clock rate is 1 MHz, and the repeating data pattern is 1111111 switching to 0000000 (each bit representing the logic state of one data line).

5.1.3.1 V_{OLP} vs Logic Family

The data shown in Figure 5.1-3 shows the effects of simultaneous switching on octal buffers. The devices in the test include those produced by two vendors of conventional end-pin Advanced CMOS Logic, HCMOS, ALS, AS, and Texas Instruments EPIC™ ACL devices. Three configurations of buffers are tested: the '244 buffer alone, the '373 used as a buffer, and the '244 buffer placed in series with and feeding into the '373 device. The Bipolar TTL devices (ALS and AS) are only tested with the combination '244 and '373. In these tests, the 9-inch transmission line is included with load capacitors added to simulate a high fan out.

For successful system operation, V_{OLP} must remain below the input threshold voltage of the accumulator clock (see Figure 5.1-3). Vendor A and Vendor B exhibit "glitches" or V_{OLP} above threshold and the system fails. The Texas Instruments EPIC™ ACL and HCMOS devices pass for all conditions. The ALS and AS devices exhibit the lowest V_{OLP}.

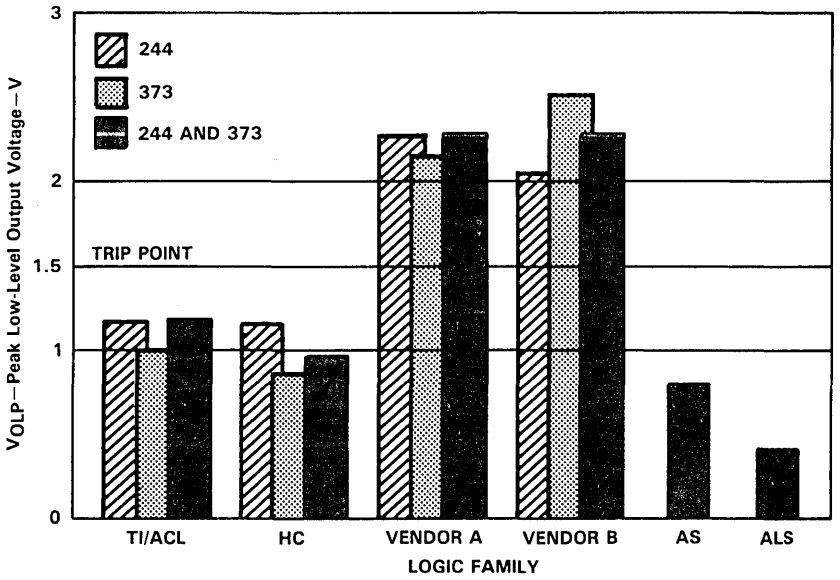


Figure 5.1-3. V_{OLP} vs Logic Family

This experiment illustrates that simultaneous switching noise is present in all high-speed logic devices. However, a system can operate normally with a conventional end-pin bipolar part, but the added noise from a conventional end-pin Advanced CMOS Logic device can cause the system to fail. The Texas Instruments EPIC™ ACL devices display V_{OLP} levels which allow successful system operation. This compares favorably with HCMOS and conventional end-pin bipolar devices.

5.1.3.2 Variations of the Simultaneous Switching Pattern

Figure 5.1-4 shows the relationship between V_{OLP} and the four different data patterns. A description of the patterns may be found in Section 5.1.4. The combination '244 and '373 buffer is used with the 9-inch, 50-Ω transmission line included. The load capacitors are not added to the line.

The pattern of 1111111 switching to 0000000 produces the greatest V_{OLP} for all vendors' parts. The other patterns show mixed V_{OLP} responses depending on which vendor is selected. The Texas Instruments EPIC™ ACL, and the HCMOS parts are successful for all patterns.

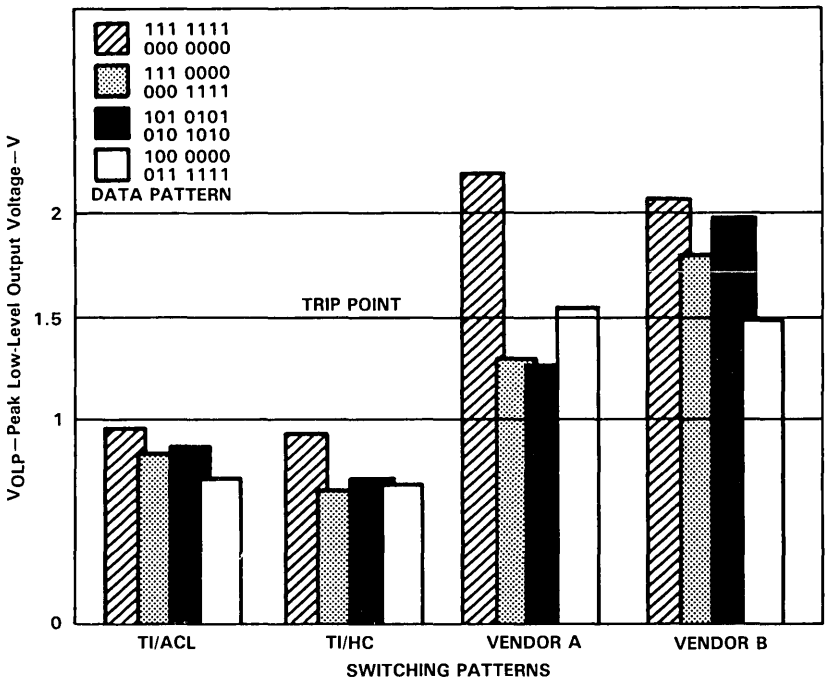


Figure 5.1-4. V_{OLP} vs Switching Pattern

This experiment indicates that even random simultaneous switching patterns cause unacceptable noise in conventional end-pin Advanced CMOS Logic. Vendor A and Vendor B exhibit V_{OLP} levels close to or over the trip point for all pattern variations.

5.1.3.3 Effects of Transmission Line

The addition of a 9-inch trace simulates an extended trace environment. This is common in many single-board systems and systems with backplanes. Adding 3-pF capacitors to the trace line simulates additional loads on the Test Buffer. The addition of the transmission line and load increases the instantaneous current required from the buffer.

Figure 5.1-5 indicates that the increased load increases the effects of simultaneous switching on the '244 and '373 buffer combination. Vendors A and B exceed the 1.5-V threshold for all cases with or without the load. The Texas Instruments EPIC™ ACL and the HCMOS devices maintain below threshold V_{OLP} for all cases. A typical board in a backplane adds 5- to 10-pF load. The 3-pF capacitors thus conservatively simulate sending data and a control line to a backplane.

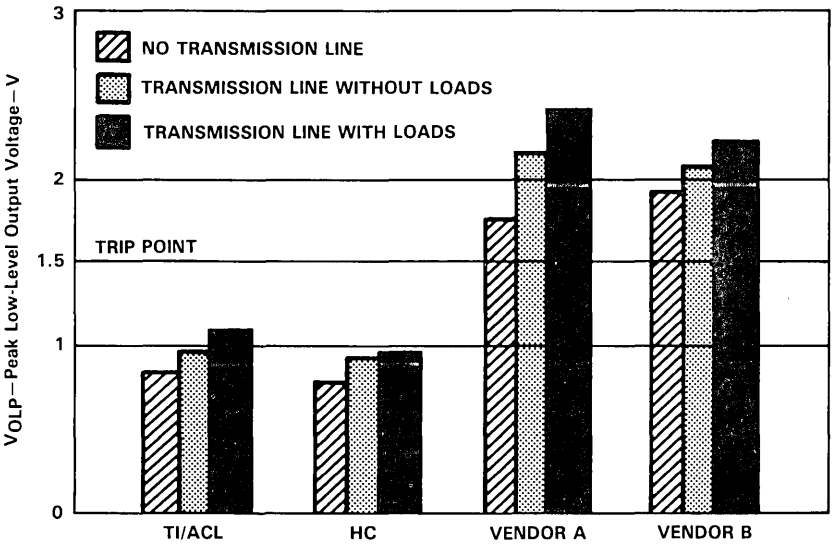


Figure 5.1-5. V_{OLP} vs Transmission Line

5.1.3.4 Device Position on Board

The HCMOS '373 device and the two other vendors' '373 devices are tested in each of three positions on the board. The 9-inch transmission line is not included. The first test of board position is done with V_{CC} set at 5 V.

A variance of ±0.1 V in V_{OLP} is found depending on the position in which the device is tested (see Figure 5.1-6). The slight variance in V_{OLP} does not show a consistent trend.

A study of transmission line length from the test buffer positions to the test accumulator was performed. It was found that position C has the longest transmission line length equal to that of the Texas Instruments EPIC™ ACL position. Positions A and B are equal in respect to line length to the Test Accumulator. This would contradict speculation that the small variance in line length is the major factor contributing to the difference in V_{OLP}.

From this experiment, it is concluded that variances of V_{OLP} may occur depending on where the device is located. A device which exhibits V_{OLP} close to the threshold voltage of a receiving device may work in some positions on the board and fail in others. This can be very frustrating. The HCMOS device is well under the threshold V_{OLP} value in all positions.

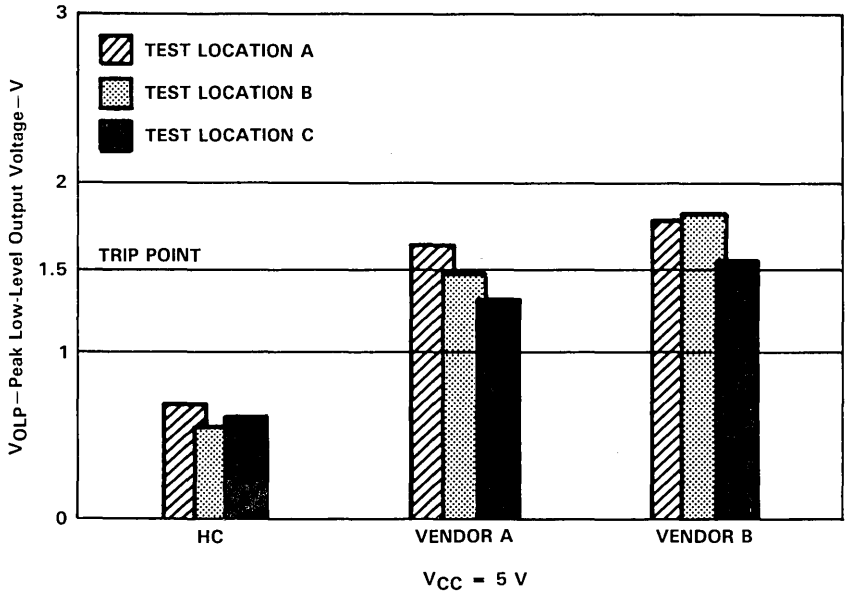


Figure 5.1-6. V_{OLP} vs Test Location

The V_{OLP} vs board position measurements are taken again with V_{CC} = 5.5 V. The other parameters remain the same.

The results (Figure 5.1-7) indicate that all vendors increase V_{OLP}. Vendor A and Vendor B exceed threshold voltage in all positions. The HCMOS device stays below the threshold voltage in all cases. This experiment indicates that V_{CC} plays a significant role in determining the level of simultaneous switching noise. As V_{CC} is increased, the level of simultaneous switching noise increases.

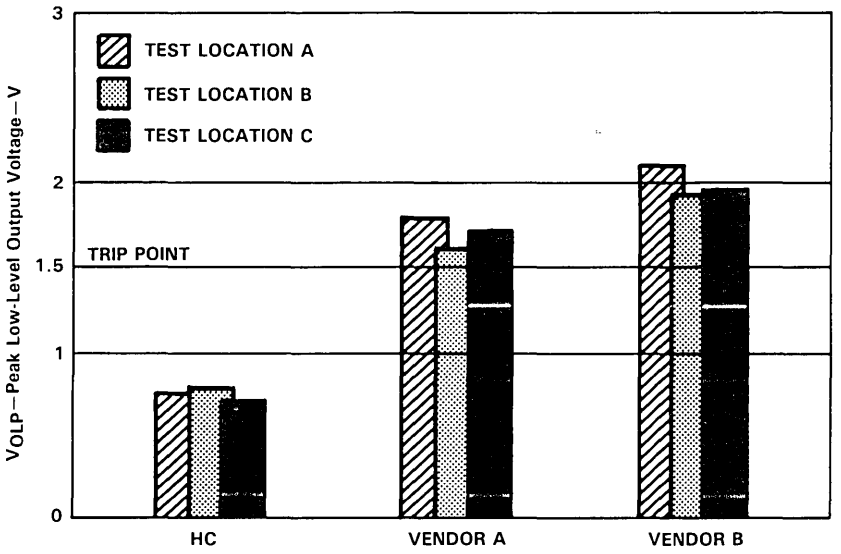


Figure 5.1-7. V_{OLP} vs Test Location

5.1.3.5 Frequency Effects

All previous experiments were performed at a clock frequency of 1 MHz. The clock frequency can be changed to a 2-Hz frequency rate. This speed does not allow an oscilloscope observation; however, the board can be operated at this speed and the two accumulator displays observed. If the two displays match, the system was successful. If the two displays do not match, the system failed.

With a frequency of 2 Hz, Vendor A and Vendor B glitch once every cycle on the Test Accumulator Display. The Texas Instruments EPIC™ ACL and HCMOS parts pass every time.

This experiment points out that V_{OLP} is not affected by the clock speed. Ground bounce is attributed to a combination of the fast transition rates or edge speed of the device outputs and the inductance of the package. For more information, please reference the application reports on Simultaneous Switching Considerations, Section 4.1, and PCB Design Considerations, Section 5.2.

5.1.4 System Evaluation Board Patterns

The following chart shows the patterns used for the System Evaluation Board. The seven least significant bits of the Switching Data Pattern represent the data on the seven System Evaluation Board data lines. DIP Switch settings are given in the chart, where 0 = off, 1 = on. Visual Display Mode will stop pattern generation for visual check after 256 patterns have been passed through the test buffer. Scope Hook-Up Mode continuously generates Switching Data Patterns to allow observation with an oscilloscope.

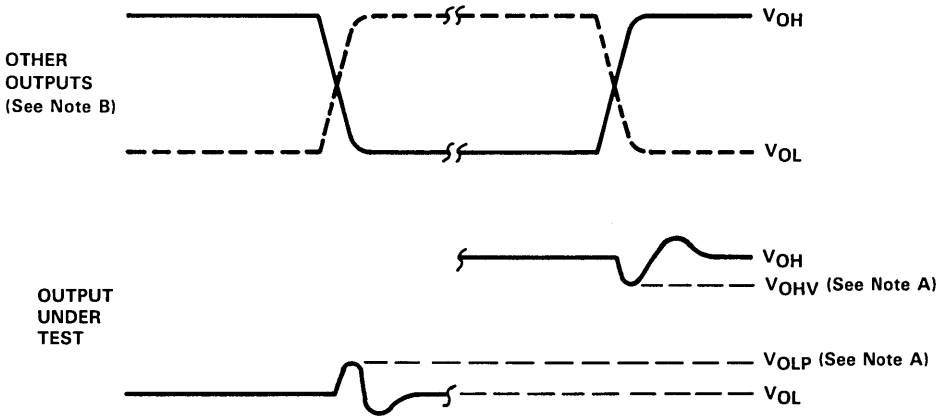
	DIP SWITCH SETTING	CORRECT LED DISPLAY	SWITCHING DATA PATTERNS
	SWITCH # 1 2 3 4 5 6 7	HEX	BINARY
Visual Display Mode	0 0 0 0 1 0 0	01	0000 0000 0111 1111
	0 0 0 1 1 0 0	F2	0000 1111 0111 0000
	0 0 1 0 1 0 0	82	0010 1010 0101 0101
	0 0 1 1 1 0 0	C2	0011 1111 0100 0000
Scope Hook-Up Mode	0 0 0 0 0 0 0	N/A	0000 0000 0111 1111
	0 0 0 1 0 0 0	N/A	0000 1111 1111 0000
	0 0 1 0 0 0 0	N/A	0010 1010 0101 0101
	0 0 1 1 0 0 0	N/A	0011 1111 0100 0000

5.1.5 Definitions

These terms and definitions are being submitted to the JEDEC council as a proposal for standardizing terms and definitions.

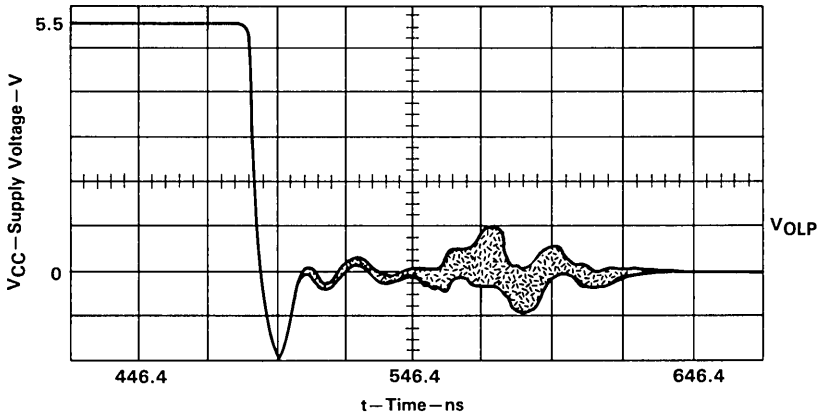
V_{OLP} — Peak low-level output voltage. The most positive (least negative) transient value of low-level output voltage at an output that is not switching while other outputs in the same package are switching. (See Figure 5.1-8.)

V_{OHV} — Valley high-level output voltage. The least positive (most negative) transient value of high-level output voltage at an output that is not switching while other outputs in the same package are switching. (See Figure 5.1-8.)



NOTES: A. V_{OHV} and V_{OLP} are measured with respect to ground reference near the output under test.
B. Input pulses have the following characteristics: PRR ≤1 MHz t_r = 3 ns, t_f = 3 ns, skew ≤1 ns.

Figure 5.1-8. Quiescent-Output Disturbance Voltage Waveforms



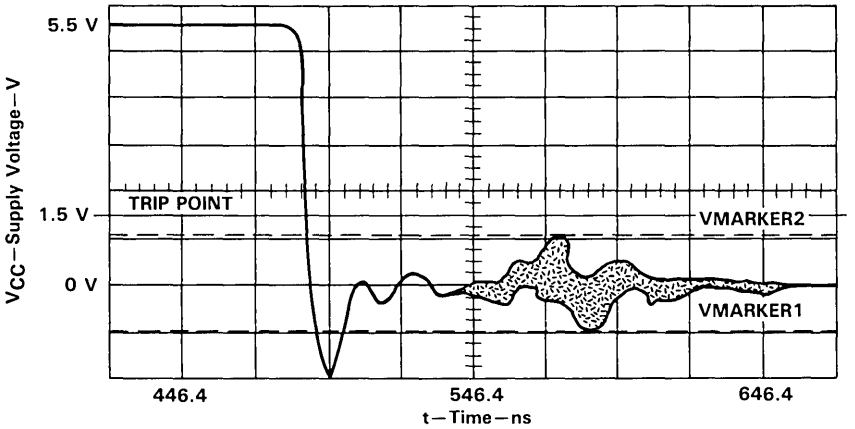
CHANNEL 1	= 1 V/div	OFFSET	= 2 V
TIMEBASE	= 20 ns/div	DELAY	= 546.4 ns
DELTA V	= –980 mV		
		VMARKER2	= 1.02 V

TRIGGER MODE	= EDGE ON POSITIVE EDGE ON CHANNEL 1
TRIGGER LEVELS	
CHANNEL 1	= 3.6 V
HOLDOFF	= 70 ns

A Hewlett-Packard HP54110A oscilloscope was used for all measurements.

Figure 5.1-9. Oscilloscope Setting and Points of Measurement

5.1.6 Waveform Comparisons

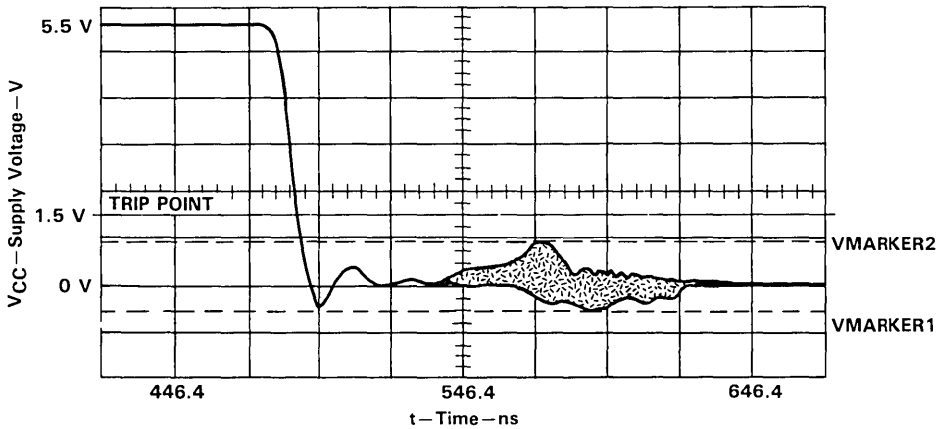


CHANNEL 1 = 1 V/div
TIMEBASE = 20 ns/div
DELTA V = 2 V
VMARKER1 = −980 mV

OFFSET = 2 V
DELAY = 546.4 ns

VMARKER2 = 1.02 V

Figure 5.1-10. Texas Instruments EPIC™ ACL



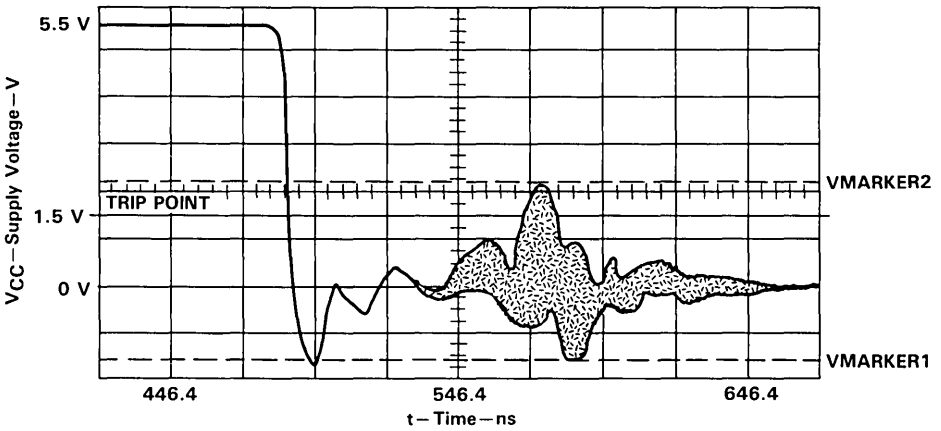
CHANNEL 1 = 1 V/div
TIMEBASE = 20 ns/div
DELTA V = 1.58 V
VMARKER1 = −700 mV

OFFSET = 2 V
DELAY = 546.4 ns

VMARKER2 = 880 mV

Figure 5.1-11. HCMOS

NOTE: For all waveforms shown, V_{CC} = 5.5 V. The buffer configuration is for the '373 only using a 9-inch transmission line with capacitor loading.

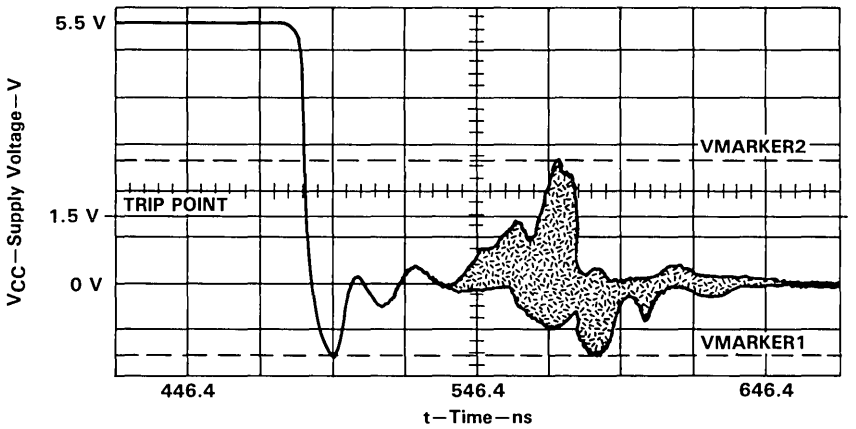


CHANNEL 1 = 1 V/div
TIMEBASE = 20 ns/div
DELTA V = 3.72 V
VMARKER1 = −1.58 V

OFFSET = 2 V
DELAY = 546.4 ns

VMARKER2 = 2.14 V

Figure 5.1-12. Vendor A



CHANNEL 1 = 1 V/div
TIMEBASE = 20 ns/div
DELTA V = 4.12 V
VMARKER1 = −1.6 V

OFFSET = 2 V
DELAY = 546.4 ns

VMARKER2 = 2.52 V

Figure 5.1-13. Vendor B

NOTE: For all waveforms shown, V_{CC} = 5.5 V. The buffer configuration is for the '373 only using a 9-inch transmission line with capacitor loading.

5.1.7 Summary

Advanced CMOS Logic gives the Logic Designer new considerations with respect to simultaneous switching. Conventional end-pin Advanced CMOS Logic families, although pin-for-pin compatible with traditional bipolar devices, cannot simply replace bipolar sockets. The noise produced from these devices causes output glitching which can be detrimental to system integrity.

A number of parameters have an effect on the simultaneous switching noise of the buffer under test. The following is a summary of parameters and their effect on V_{OLP}.

PARAMETER	V_{OLP} RESPONSE	CONVENTIONAL PIN ACL	TI EPIC™ ACL	CAUSE
Loading	Increase	Fail	Pass	Increased instantaneous current
Position on Board	±0.1 V	Pass/Fail	N/A HC = Pass	Unknown
V_{CC} Increase	Fail	Pass	Pass	V_{OLP} is a function of V_{CC}
System Clock Speed	No Effect	Fail	Pass	V_{OLP} is not a function of Clock Speed
Pattern	Various Responses	Pass/Fail	Pass	Different patterns cause incremental differences in current required

The results from this experiment indicate potential system noise problems with a single Advanced CMOS device on the board. A true high-speed application with multiple Advanced CMOS Logic devices could induce even greater system noise levels on the V_{CC} and Ground planes. This increased noise could further reduce the integrity of system performance.

Simultaneous switching causes some level of output glitching on all high-speed logic families. Conventional end-pin Advanced CMOS Logic devices induce a level of system noise which significantly affects system integrity. Texas Instruments addresses this problem at the device level to offer a solution to the designer. EPIC™ ACL from Texas Instruments allows the designer to maximize system performance without sacrificing system integrity.

5.2 Advanced CMOS Logic PCB Design Considerations†

5.2.1 Introduction

Texas Instruments Advanced CMOS Logic (ACL) family offers system designers a logic family with propagation delays equivalent to 54/74F Bipolar TTL Logic while supplying 24 mA of sink/source current. ACL flip-flops toggle rates have been observed greater than 200 MHz — substantially faster than bipolar 54/74F. The high-speed performance of the ACL family also includes the advantage of low CMOS power consumption.

With the emergence of ACL, as well as higher speed logic families such as 54/74AS, 54/74F and 54/74ALS, board-level design rules have become more stringent. In general, these criteria are similar to the ECL design considerations presented by William R. Blood in the *"MECL System Design Handbook."*[1] Michael A. Higgs and Ray Day have presented similar design guidelines for Advanced Schottky bipolar family.[2,3] Logic offers high-speed performance required by system designers, but, with this performance, care must be used in its application.

Design guidelines are presented for the implementation of ACL to assist in trouble-free system development. Items covered include recommendations for decoupling and transmission line termination. ACL's leadership flow-through architecture assists the design engineer in implementing high-speed logic without having to adopt unnecessary design efforts to ensure reliable system performance.

5.2.2 High-Speed Logic System Environment

Skilled designers realize the environment of a high-speed logic circuit must be controlled to ensure reliable system performance. Consideration must be given to power distribution, device decoupling, and signal integrity due to transmission line reflections and crosstalk, as well as system noise levels. Failure in any one of these areas can result in system performance that is less than the original design goals or worse, a nonusable system.

5.2.2.1 Power Distribution and Decoupling

To evaluate the effect of a high-speed device upon the power bus, consider an ACL device driving a 50-Ω transmission line. The device must provide approximately 80 mA of instantaneous current per output switched to drive the line. For an octal device, the current could be as high as 640 mA in 3 to 4 ns. Depending upon the impedance of the power bus, a large amount of noise can be generated due to the transient currents when an output changes logic states.

†Written by C. Hefner and W. A. Thompson.

In high-speed systems, power distribution should be done using V_{CC} and ground planes. The use of power planes reduces the amount of V_{CC} and system ground noise generated due to reduced interconnection impedances. This is illustrated by a comparison between the impedance of printed circuit board (PCB) planes and traces versus frequency in Figure 5.2-1.[4] Other added benefits of the power planes are increased component density, reductions in EMI radiations, and printed circuit board interconnection impedance control.

Decoupling requirements for any system are related to the amount of power bus noise that can be tolerated. For most cases, a circuit's susceptibility to power bus noise—caused by operation of other circuits connected to the same power bus—is inversely proportional to the conservatism with which noise immunity criteria are met.[5] With this in mind, some guidelines must be followed in establishing a decoupling strategy.

A general equation can be developed to calculate the decoupling capacitor value for an application requiring a logic device to supply a transient current to a capacitive load. The value of the decoupling required to limit the power bus noise to a given level can be given by:

$$C = \frac{I}{\frac{dV}{dt}} \qquad (1)$$

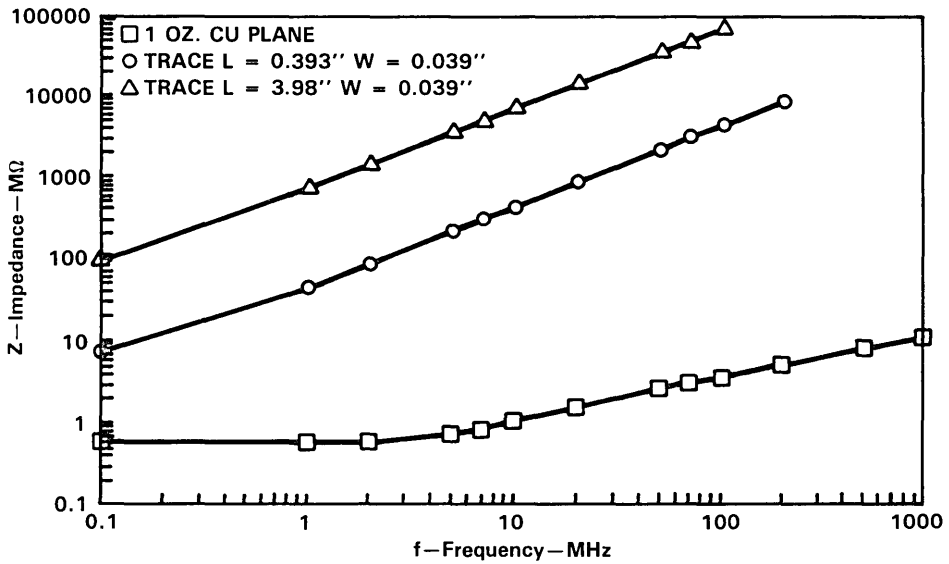


Figure 5.2-1. PCB Plane and Trace Impedance vs Frequency

where:

C = decoupling capacitor value
I = magnitude of the transient current
dV = V_{CC} tolerance
dt = output device rise and fall time

Overall, the method by which power is supplied to a high-speed circuit can affect its performance. Careful consideration must be made in the beginning of the design to ensure the power distribution network is transparent to the functionality of the system. This is accomplished by providing V_{CC} and ground planes as well as a decoupling capacitor for each high-speed logic package.

5.2.2.2 PCB Trace Characteristics

Most high-speed logic families have output signal edge rates that can cause interconnect wiring to appear as a transmission line. In general, any trace on a PCB can be considered to be a transmission line if the propagation delay of the line is long compared to the rise or fall time of the signal. Lines that have a short electrical length relative to the signal's rise or fall time do not jeopardize signal integrity due to excessive ringing or reflections. If a line's electrical length is such that signal integrity is affected, transmission line termination techniques must be used to ensure proper operation.

PCB traces usually considered in a high-speed system are strip lines and microstrip lines (Figure 5.2-2). Note, these configurations are relatively simple to obtain provided multilayer boards with power planes are used as previously recommended. The advantage of the two configurations is the characteristic impedance (Z_0) of the lines based upon the physical structure of the PCB. Z_0 can be calculated for the two types of lines using the geometric relationships and physical constants of the PCB material. Reference 1 develops the equations and gives an in-depth analysis of the lines' properties. Given a line of either type, a signal's propagation delay on the line can be calculated. Equations 1 and 2 give the delays of the microstrip and strip lines in ns/ft, respectively. Note the propagation delay of a line is not a function of the geometry of the line.[1]

$$t_{pd} = 1.017\sqrt{0.475e_r + 0.67} = Z_0C_0 \quad (2)$$

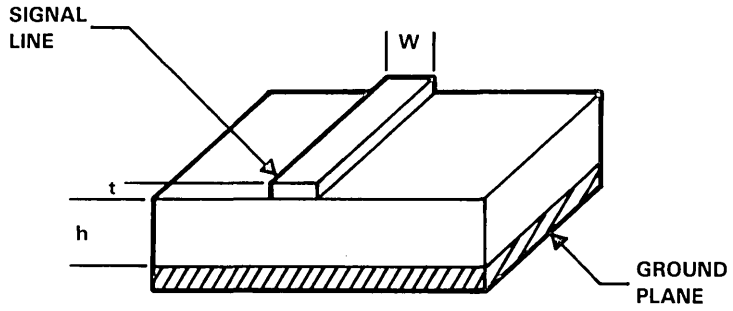
(Microstrip line propagation delay)

$$t_{pd} = 1.017\sqrt{e_r} = Z_0C_0 \quad (3)$$

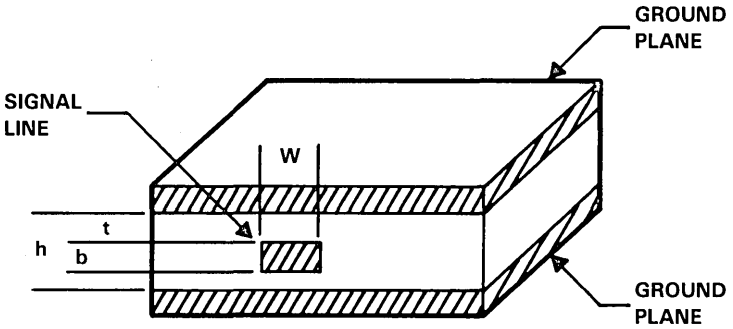
(Strip line propagation delay)

where:

e_r = the relative dielectric constant of the PCB material
Z_0 = the characteristic impedance of the line
C_0 = the capacitance per foot of line



(a) MICROSTRIP



(b) STRIP

Figure 5.2-2. Lines

For PCBs constructed of fiberglass epoxy material, the dielectric constant is roughly 5.0. Using this number in Equations 2 and 3 yields line propagation delays of 1.77 ns/ft for the microstrip line and 2.26 ns/ft for the strip line.

The maximum allowable line length, before termination is required to negate the effects of reflections, can be estimated by using the rule of thumb (Equation 4), provided the effects of capacitive loading are taken into account. Equation 4 is based upon a maximum signal undershoot of 12%.[1]

$$L_{max} = \frac{t_{edge}}{2\ t_{pd}} \qquad (4)$$

where:

L_{max} = maximum line length required to maintain signal integrity
t_{edge} = signal rise or fall time
t_{pd} = line's propagation delay

Given $t_{pd} = Z_0C_0$, the effects of additional capacitive loading can be derived. Additional capacitive loading $C_{(Load)}$ will affect the propagation delay of the strip and microstrip line as shown in Equation 5.

$$t_{pd(loaded)} = \frac{\sqrt{1 + C_{(Load)}}}{C_0} \quad (5)$$

Figure 5.2-3 shows the calculated maximum line length with respect to capacitive loading for a 50-Ω strip line and the output edge rates that are typically observed for an ac output across capacitive loading. This demonstrates that, as the edge rate is reduced due to capacitive loading effects, the maximum allowable line length increases.

The trend shown in Figure 5.2-3 is based upon actual edge rate data of a typical AC series device. It should be noted that, if the edge rate is held constant in Equation 4, the trend is reversed. That is, the maximum line length is reduced as capacitive loading is increased. This trend is not real since, for all logic devices, the output edge rate increases with additional capacitive loading.

Specific applications will have different maximum allowable line lengths depending upon acceptable undershoot criteria and the actual impedance of the PCB trace.

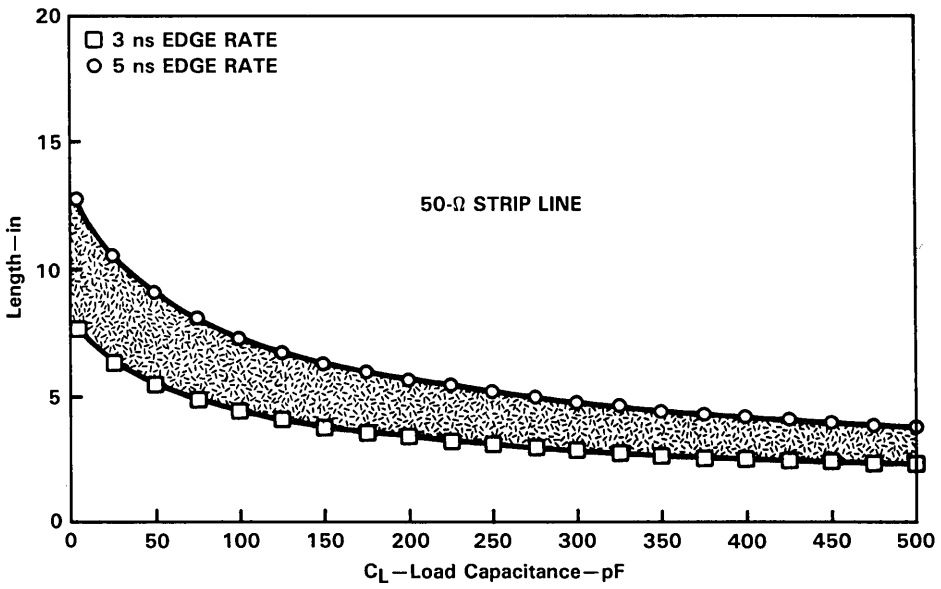


Figure 5.2-3. Maximum Line Length vs Capacitive Loading

5.2.2.3 Termination Techniques

For applications that require termination, two commonly used choices are either parallel or series termination. Figures 5.2-4(a) and 5.2-4(b) show the two techniques.

Parallel termination is accomplished by placing an impedance equal to the characteristic impedance of the line at the receiving end. This may be accomplished with the use of a parallel network as shown in Figure 5.2-4(a). The Thevenin equivalent of the two resistors is one resistor that can be designed to be equal to the characteristic impedance of the line. A properly parallel-terminated line sees no reflections since the terminating resistor equals the characteristic impedance.

Parallel terminations give the best speed performance for an interconnection and allow the use of distributed loads. The disadvantage of this technique is the dc power required by the network and the current that the ACL output would be required to supply. This can be overcome by the use of a capacitor as shown in Figures 5.2-4(c) and 5.2-4(d). Some care must be taken to choose the correct value for the capacitor. The impedance of the RC network should equal that of the characteristic impedance of the line, but the time constant for the network should be equivalent to the rise and fall time of the signal of the line.

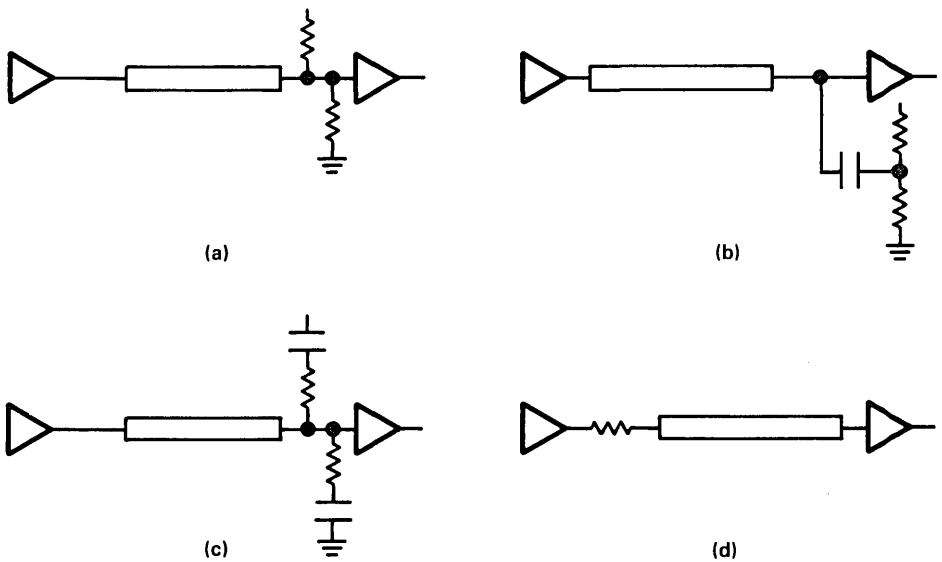


Figure 5.2-4. Transmission Line Termination Techniques

Series terminating or series damping is accomplished by placing a resistor in series with the output of the driver and the line as shown in Figure 5.2-4(b). The impedance of the series resistor and the driver's equivalent impedance damp the reflection from the receiver, provided their sum equals the characteristic impedance of the line.

Series termination has the advantage of not increasing the power of a system. The major disadvantages of series-terminated lines are as follows: voltage drops can develop across the resistor resulting in deterioration of noise margin; distributed loads cannot be used on a series-terminated line due to the single signal reflection that occurs from the receiving end of the line to the resistor; and, finally, the effect of lumped loading on propagation delays is magnified by a factor of 2 when comparing a series-terminated line to a similar parallel-terminated line.

5.2.2.4 Crosstalk

Crosstalk is the coupling of a signal from an active, signal-carrying line to a nearby quiet line. This coupling is caused by the mutual capacitance (C_m) and mutual inductance (L_m) that exist because of the proximity of the two lines.

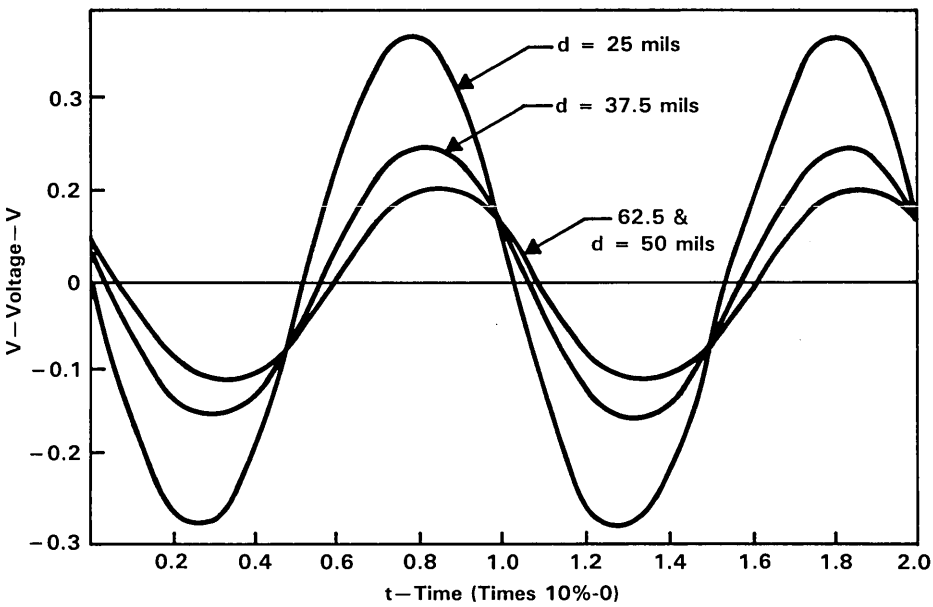


Figure 5.2-5. Crosstalk Magnitude Due to Various Line Separation

Crosstalk is best controlled in a system by understanding the critical factors affecting it; i.e., line length, line separation, and shielding effects. A summary of data in Figures 5.2-5 shows the effect for different line separation.

In general, crosstalk can be controlled by avoiding long, closely spaced, parallel traces. If this is not practical, ground lines can be interspersed between the signal-carrying lines to provide shielding. Another design guideline is to avoid running CLOCK, CLEAR or other control lines on the same plane as a data or address bus. Different signal-carrying planes on the board should be shielded from each other by V_{CC} or ground planes.

5.2.3 ACL Pinout Strategy

Engineers, throughout the electronics industry, who are currently designing with high-speed logic are aware of the problems caused by multiple outputs switching in a single device even when careful design effort goes into a PCB. Initial evaluations of Advanced CMOS preliminary designs and customer inputs regarding existing Advanced CMOS logic have led Texas Instruments to develop an industry solution to simultaneous switching problems.

The source of the simultaneous switching noise is the induced voltage on a silicon die's ground or V_{CC} plane due to the transient currents caused by switching capacitive loads. This can be described by the following equation:

$$V_L(t) = -L_P C_L \frac{d^2V_O(t)}{dt^2} \qquad (6)$$

where:

$V_L(t)$ = the voltage transient on the silicon die
L_P = the self-inductance of the package power pin
C_L = the load capacitance

$\frac{d^2V_O(t)}{dt^2}$ = the second derivative of the output voltage waveform with respect to time

From Equation 6, it can be seen that the voltage transient on the die's power plane $V_L(t)$ is proportional to the self-inductance of the power pin and the slew rate of the output waveform. The pin with the maximum self-inductance for a dual-in-line package is an end pin due to the long physical length of the leadframe interconnect. Advanced CMOS technologies drive edge slew rates of approximately 5 V in 3 ns. This slew rate and the large power pin self-inductances of a standard pinout product serve to make simultaneous switching a severe problem for Advanced CMOS.

As a result of analysis of the problem and customer consultation, Texas Instruments has adopted a leadership flow-through architecture pinout for the ACL family. This new pinout will provide functional device integrity and reliable system performance for both TTL and CMOS system interface. The pinouts, for both AC and ACT series devices, will incorporate center V_{CC} and ground pins as shown in Figure 5.2-6. The center-pin configuration reduces the power-pin effective inductance that directly relates to the system-level noise generated by high-speed logic families.

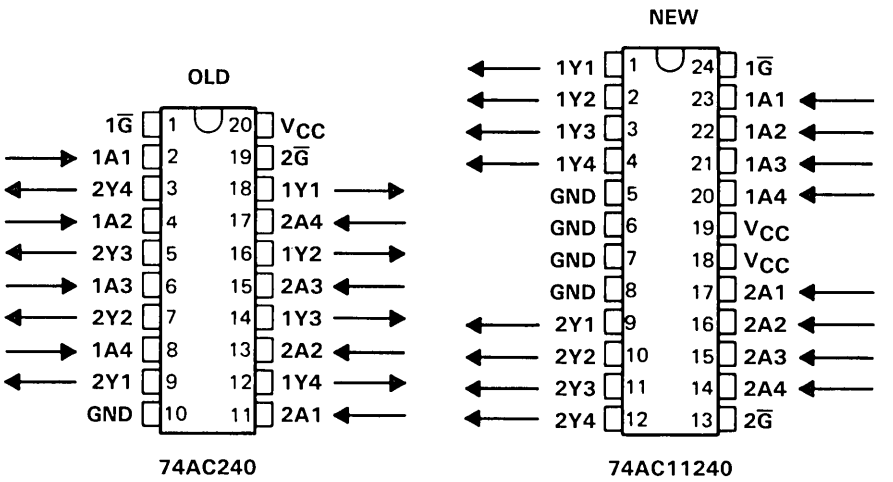


Figure 5.2-6. Flow-Through Architecture

5.2.4 Simultaneous Switching Performance

To demonstrate the effectiveness of the flow-through pinouts with center power pins, Figures 5.2-7, 5.2-8, 5.2-9, and 5.2-10 show the simultaneous switching noise obtained for the 74AC11032, 74ACT11074, and 74AC11109. The data shown is for devices packaged in dual-in-line (DIP) packages, V_{CC} = 5 V, and T_A = 25 °C. Note the noise spike height of the unswitched output in the low state is about 0.5 V for all three devices. Operation across guaranteed temperature and supply voltage ranges will typically only increase this number by 0.3 V. A comparison of the gate function shows that, for a similar device packaged in traditional end power pin DIPs, the ground noise spike is approximately 1.5 V with a similar degradation over the guaranteed V_{CC} and temperature range.

The noise spikes generated in traditional bus interface devices are even worse than those of gates and flip-flops. These bus interface devices include octal buffers as well as 9- and 10-bit devices. The performance of end power pin, DIP-packaged, octal devices is summarized in Figure 5.2-11. Included is data from various end-pin vendors compared to TI's center-pin version. The flow-through architecture of the ACL helps obtain simultaneous switching performance far superior to end-pin products.

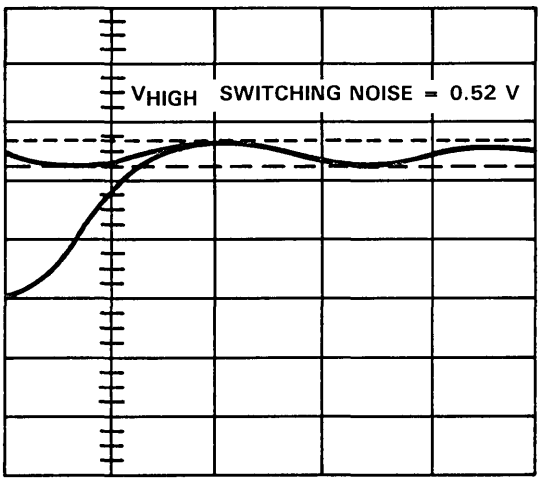


Figure 5.2-7. 74ACT11032 Simultaneous Switching Noise

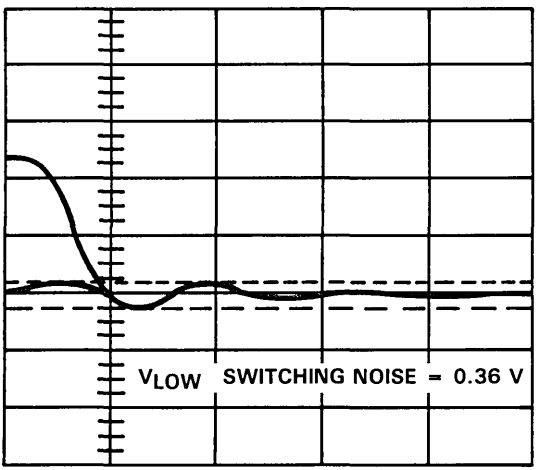


Figure 5.2-8. 74AC11032 Simultaneous Switching Noise

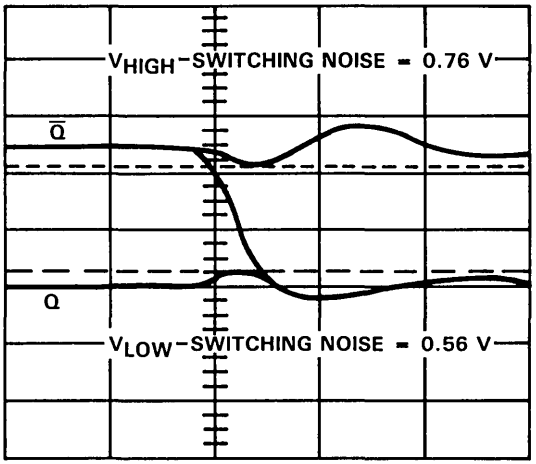


Figure 5.2-9. 74ACT11074 Simultaneous Switching Noise

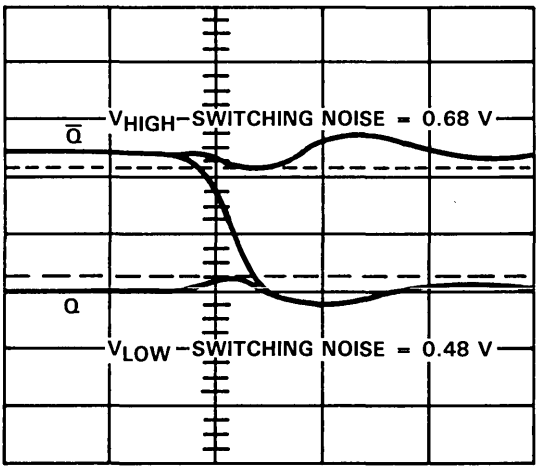


Figure 5.2-10. 74AC11109 Simultaneous Switching Noise

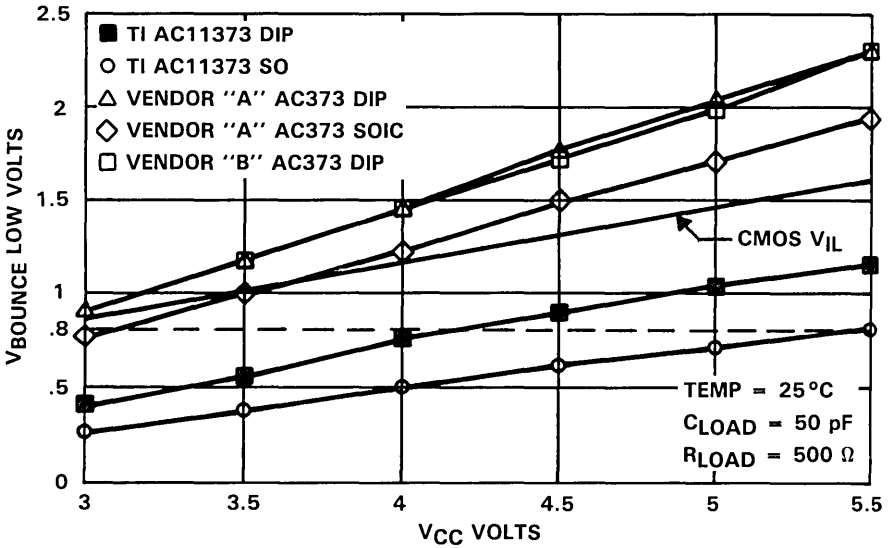


Figure 5.2-11. '373 Simultaneous Switching Summary

5.2.5 Summary

The introduction of ACL in flow-through architecture pinouts provides the design engineer a solution to high-speed logic noise problems. The leadership architecture allows the designer to concentrate on the environmental factors that can be controlled to provide a reliable system. These factors include power distribution and decoupling as well as PCB interconnect considerations. The effect of the flow-through pinouts is that, if normal care is taken in implementation, the system reliability will not be reduced due to excessive switching noise. In conclusion, ACL packaged in flow-through architecture will not place system reliability in jeopardy, as compared to traditional pinouts, due to excessive switching noise.

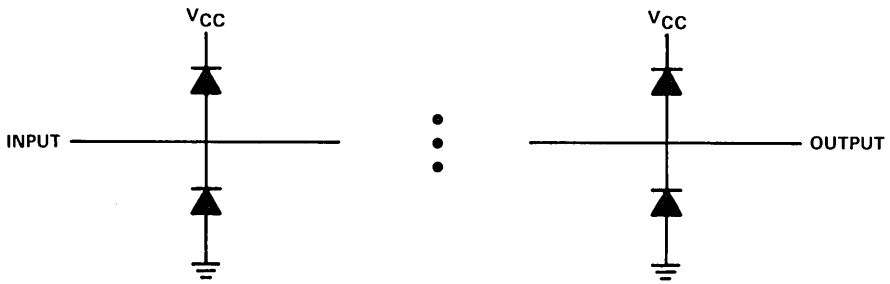
5.2.6 References

1. W. R. Blood, Jr. *MECL System Handbook*, 4th edition, Motorola Inc. (1983).
2. M. A. Higgs, *'AS Load Management*, Texas Instruments Incorporated, Application Report (1986).
3. R. Day, *Printed Circuit Board Design for Advanced Schottky Family*, University of Arkansas (1985).
4. D. R. J. White, *EMI Control in the Design of Printed Circuit Boards and Backplanes*, 3rd edition, Don White Consultants, Inc. (1982).
5. R. K. Keenan, Ph.D., *Decoupling and Layout of Digital Printed Circuits*, TKC Consulting Electronics Engineers (1985).

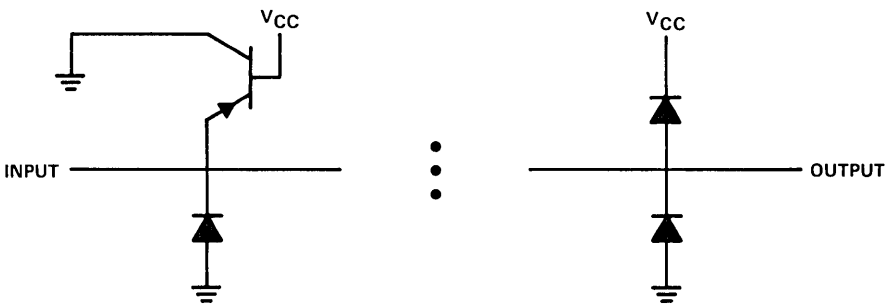
5.3 Partial System Power-Down with CMOS Devices†

CMOS devices offer a designer many desirable features, the most important one being a low power consumption. However, in some systems, a designer will find that even the low power consumption of CMOS is insufficient to meet power supply constraints. Therefore, some designers will utilize partial system power-down or multiple V_{CC} supplies to meet system power requirements.

Whenever a system incorporates the use of multiple V_{CC} supplies or partial power-down, the designer must take into account several important device parameters if High-Speed CMOS (HC) or Advanced CMOS Logic (ACL) devices are used. This is necessary to avoid excessive power dissipation and prevent damage to a device that could lead to degradation in the reliability of the device. These parameters are the continuous input and output diode currents (I_{IK} and I_{OK}) and the continuous output current (I_O). I_{IK} and I_{OK} refer to the continuous current that is flowing through the input and output electrostatic discharge (ESD) protection circuits. (Figure 5.3-1 shows functionally equivalent schematics of the ESD structures for HC and ACL devices.)



(a) HC EQUIVALENT ESD STRUCTURE



(b) ACL EQUIVALENT ESD STRUCTURE

Figure 5.3-1. Simplified ESD Structures for HC and ACL Devices

†Written by R. Curtis

I_O is the continuous current flowing through one of the two output transistors. Table 5.3-1 shows the absolute maximum ratings for I_{IK}, I_{OK}, and I_O for both HC and ACL devices, as listed on device data sheets.

To understand how I_{IK}, I_{OK}, and I_O can affect a system design, consider an example of a partial system power-down. Figure 5.3-2 shows a partial power-down situation where a device powered with V_{CC} = 5 V is driving a device without power applied. The input voltage to the nonpowered device exceeds V_{CC} by more than the threshold voltage (0.6 to 0.8 V), causing the ESD protection structure to conduct whenever the output of the driver is in a high state. Therefore, the driving device will power-up the receiving device and any other device sharing the same V_{CC} line. If no current limiting is provided, then the maximum I_O of the driving device and the maximum I_{IK} of the receiving device could be exceeded.

Table 5.3-1. Absolute Maximim Values for I_O, I_{IK}, and I_{OK}

PARAMETER	ABSOLUTE MAXIMUM	
	HIGH-SPEED CMOS (HC)	ADVANCED CMOS (ACL)
I_O	±25 mA (Standard) ±35 mA (High-Current)	±50 mA
I_{IK}	±20 mA	±20 mA
I_{OK}	±20 mA	±50 mA

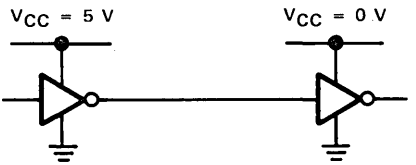
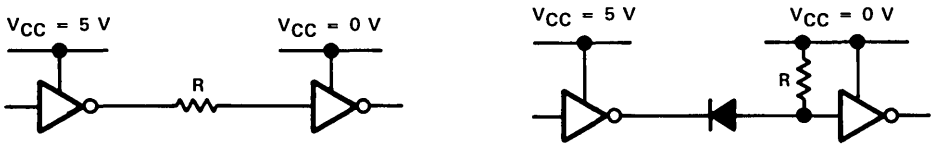


Figure 5.3-2. Example of Partial System Power-Down

Several methods are available to protect the driving and receiving devices during partial system power-down. If the driving device has three-state outputs, then placing the outputs in a high-impedance state will provide the best solution. However, if this is not a viable option, some method of current limiting must be provided. Figure 5.3-3 shows several methods that can be used, with current-limiting series resistors being the simplest. The value of the resistor is chosen to limit the current into the receiving device to less than 20 mA. The major drawback to using a current-limiting resistor is power dissipation. Another drawback is the effect that the resistor has on the input transition time at the receiving device during normal system operation. If the total capacitance of the interconnects and receiving devices is high (i.e., a

high-capacitance bus), then a current-limiting resistor will increase the input transition time. A system designer will have to ensure that the addition of the resistor will not increase the input transition time above the maximum input transition time of the receiving device.



(a) RESISTOR CURRENT LIMITING

(b) RESISTOR-DIODE CURRENT LIMITING

Figure 5.3-3. Current Limiting for a Partial System Power-Down

A second method of current limiting, shown in Figure 5.3-3, involves the use of a pull-up resistor and a diode. The advantage of this method is that it allows for the use of a large resistor, thereby holding power dissipation to a mimimum. The disadvantage of this method is that it requires the use of additional components and results in a higher value of V_{IL} at the receiving device.

A second example of how a partial power-down can cause unwanted operation is the case of two drivers connected to the same bus with one device powered down, as shown in Figure 5.3-4. In this case, the first bus driver will attempt to power-up the second bus driver and any other devices sharing the same V_{CC} line through the output ESD structure of the unpowered device.

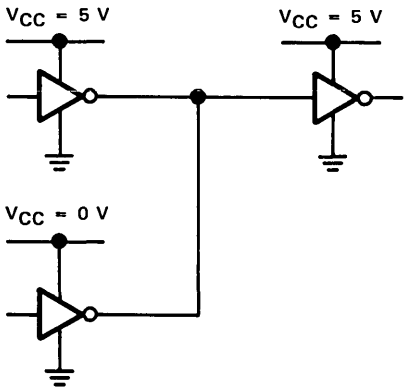
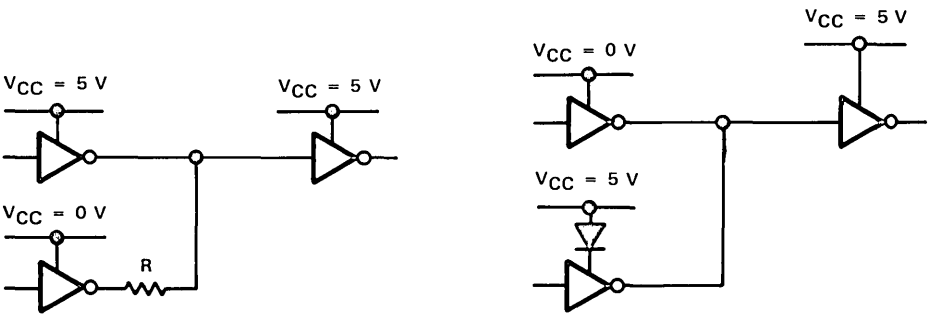


Figure 5.3-4. Partial Power-Down with Bus Drivers

Several methods are available to solve this type of problem. One method is simply to use a current-limiting resistor as outlined before. Another solution is to isolate the unpowered driver from the V_{CC} line by means of a diode between the power pin and the V_{CC} supply. If the unpowered device is a transceiver, then pull-up or pull-down resistors are required on the output control inputs to disable the outputs. Not disabling the transceiver outputs would allow the transceiver to power up the unpowered devices that are driven by its outputs. Whenever an isolating diode is used, the V_{CC} at the driver will always be a diode forward drop below the voltage of the supply, resulting in a degradation of V_{OH}. Figure 5.3-5 shows these circuit solutions.



(a) CURRENT-LIMITING RESISTOR

(b) DIODE ISOLATION (FOR A TRANSCSEIVER, DISABLE OUTPUTS)

Figure 5.3-5. Current Limiting for Bus Drivers During Partial Power-Down

Another example of a system that could require current-limiting protection is one that uses multiple V_{CC} supplies, or provides each card with its own onboard voltage regulator. If the V_{CC} supplies of two connecting devices differ by more than 0.5 Vdc, then a current-limiting scheme should be considered if the driving device is a CMOS device and is connected to the higher V_{CC}. This is necessary because V_{OH} of a CMOS device will be the same as V_{CC} whenever the I_{OH} requirement is very small. Therefore, the input ESD protection diode could conduct if the V_{CC} of the driver (or V_{OH}) exceeds the V_{CC} of the receiver by more than 0.5 Vdc. It should be pointed out that it is the resulting current flow that causes the degradation of the diode, not the voltage. Note: This applies only to supplies that vary by more than 0.5 Vdc. Dynamic switching currents could cause transient voltage spiking on V_{CC} lines such that a 0.5-V difference between supplies could easily exist. These transients will not cause a problem as long as their duration is short (less than 20 ns).

Partial system power-down offers a designer a convenient method to save on system power consumption. However, when a partial power-down scheme

is used, a designer must take steps to ensure that no damage occurs to devices and to avoid excessive power dissipation. The designer must also take similar precautions when using multiple V_{CC} supplies if the supplies of two connecting devices differ by more than 0.5 Vdc.

5.4 CMOS Power Management†

5.4.1 Introduction

The need for devices that consume a minimum amount of power was a major driving force behind the development of CMOS technologies. As a result, the one property of CMOS devices that is most well known is their low power consumption. However, for someone who is trying to minimize the power requirements of a board or a system, simply knowing that CMOS devices may use less power than equivalent devices from other technologies does not provide much help. It now becomes important to not only know how to calculate power consumption, but to understand how factors such as input voltage level, input rise time, and output loading affect the power usage of a device as well. The only way to effectively minimize power consumption is to understand what causes it.

To calculate power consumption in a CMOS device, break the total power requirement into its individual components. These components are:

- Quiescent or nonswitching power
- Dynamic or switching power.

The total power consumption of a device is the sum of these two components.

5.4.2 Quiescent Power Consumption

The quiescent power consumption for a CMOS device is the product of the supply voltage and the total supply current, or:

$$P_q = V_{CC} \times I_{CC}\ (\text{total})$$

I_{CC} (total) represents the current flowing through the n-channel and p-channel transistor pair that comprises the basic CMOS inverter (Figure 5.4-1). When the input voltage is at ground or V_{CC}, one transistor is fully on and one is fully off. In this case, I_{CC} (total) is simply the reverse leakage current flowing through the nonconducting transistor. This value is listed on device data sheets as I_{CC} and is specified as a maximum limit.

†Written by R. Curtis

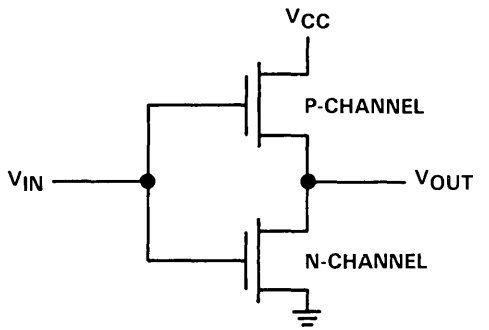


Figure 5.4-1. Basic CMOS Inverter

5.4.3 High-Speed and Advanced CMOS Devices

If the input voltage is at a value between ground and V_{CC}, then it is possible that both the n-channel and p-channel transistors are partially on. In this case, I_{CC} (total) is no longer a reverse leakage current, and its value will be determined by the magnitude of the input voltage. Figure 5.4-2 shows the variation in supply current for both High-Speed CMOS (HC) and Advanced CMOS (AC) devices as the voltage on one input is varied at room temperature (all other inputs are tied to V_{CC} or ground; outputs are open). As the input voltage approaches the threshold or switching point of a device (50% of V_{CC} nominal), I_{CC} increases steadily. It reaches its greatest value when the input voltage is at threshold. From Figure 5.4-2, it can be seen that the increase in I_{CC} is negligible and may be ignored as long as the input voltage is less than 1 V or greater than $V_{CC} - 1$ V.

5.4.4 TTL-Compatible CMOS Devices

In the case of CMOS devices with TTL-compatible input structures (HCT and ACT devices), the relationship between supply current and input voltage level must be given special attention. HCT and ACT devices are used to provide a direct interface between TTL drivers and CMOS receivers. They are necessary because the specified TTL V_{OH} level does not ensure that the minimum V_{IH} level of a CMOS input will be met. The threshold of a HCT or ACT device is shifted from 50% of V_{CC} to about 1.5 V, ensuring that the device will operate properly with an input signal switching at TTL levels.

However, the dependence of supply current upon input voltage levels holds true for HCT and ACT devices. If an input of a HCT or ACT device is driven by a TTL device, it is possible that the HCT or ACT device will use additional supply current whenever the input is high. This increase in supply current will occur whenever the V_{OH} of the TTL driver is low enough to cause both the p-channel and n-channel transistors, in the input of the HCT or ACT device, to be partially on. The increase in supply current will not occur when the TTL

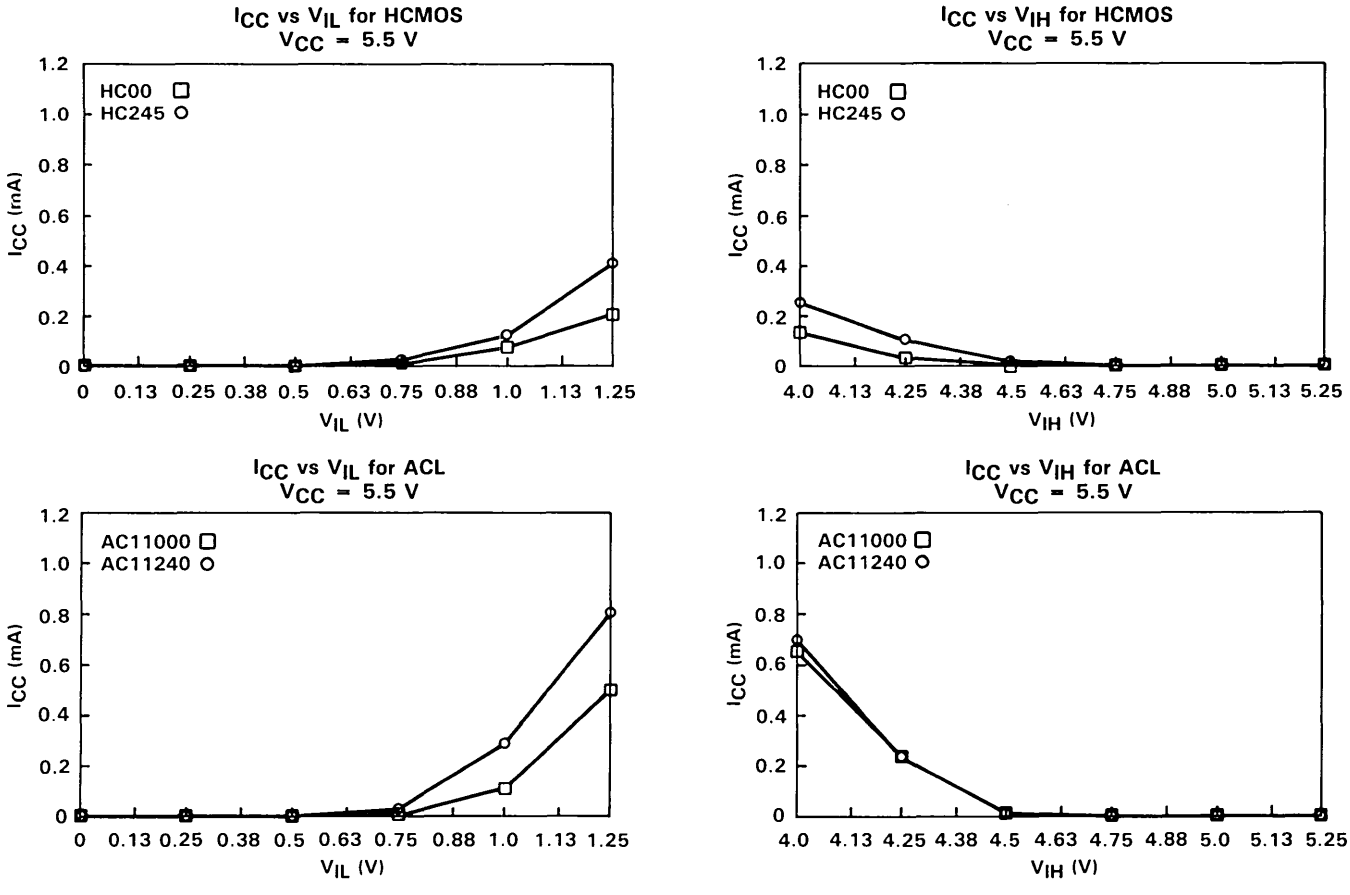


Figure 5.4-2. I_{CC} vs V_{IN}

device drives the input of the HCT or ACT device low because the V_{OL} of the TTL driver is low enough to ensure that the n-channel transistor is fully off. The increase in supply current that can occur when an input is driven by a TTL device is called ΔI_{CC}. ΔI_{CC} is specified as a maximum value on HCT and ACT data sheets on a per input basis.

The quiescent power consumed by CMOS devices is given by:

$$P_q = V_{CC} \times I_{CC} \text{ (total)}$$

For HC and AC devices, I_{CC} (total) is the value of I_{CC} specified on device data sheets plus any increase in I_{CC} due to input signal voltage levels. For most applications, the increase in I_{CC} due to input signal voltage level can be ignored whenever the input is driven by another CMOS device, unless the input voltage approaches the V_{IL} max or V_{IH} min limit. Input voltages less than 1 V or greater than $V_{CC} - 1$ V do not cause a significant increase in I_{CC} (total).

For HCT and ACT devices, I_{CC} (total) includes the increase in I_{CC} due to inputs being driven by TTL devices. It is calculated as:

$$I_{CC} \text{ (total)} = [N \times (\Delta I_{CC}) \times dc] + I_{CC}$$

where:

- N = number of inputs driven by a TTL device
- dc = duty cycle
- ΔI_{CC} = increase in supply current (specified on data sheet)
- I_{CC} = quiescent supply current (specified on data sheet)

5.4.5 Dynamic Power Consumption

For many applications, dynamic power usage accounts for most of the total power requirement for a CMOS device. To accurately determine the total power consumption of a CMOS device, it is necessary to develop a method that will allow the user to estimate the dynamic power usage in any given system. This is accomplished by specifying a value called power dissipation capacitance, or C_{pd}. C_{pd} allows a user to calculate the dynamic power usage of a device using the formula:

$$P_d = [C_{pd} \times V_{CC}^2 \times F_i] + \Sigma (C_L \times V_{CC}^2 \times F_o)$$

where:

- C_L = load capacitance on each output
- C_{pd} = power dissipation capacitance of the device (specified on device data sheet)
- F_i = input switching frequency
- F_o = output switching frequency

Dynamic power usage consists of two components:

1. Power used by the device as it switches states
2. Power required to charge any load capacitance.

Power consumption caused by the device switching logic states occurs because transistors fabricated on integrated circuits are not ideal. Parasitic capacitances exist on the chip; they must be charged and discharged. Additionally, there are short periods of time during switching when both the n-channel and p-channel transistors are partially on, resulting in current spiking between V_{CC} and ground. It is impossible to differentiate between power used to charge parasitic capacitances and current spiking; therefore, the value C_{pd} represents both.

The C_{pd} value for a particular device is determined by the standardized C_{pd} test procedure described in Appendix E of JEDEC Standard No. 7A. C_{pd} is calculated as a typical value from the formula:

$$C_{pd} = \frac{I_{CC}\ (\text{dynamic})}{V_{CC} \times F_i} - C_L$$

where:

F_i = input frequency (1.0×10^6)
V_{CC} = supply voltage (5 V nominal)
C_L = equivalent load capacitance (dependent upon number of outputs switching with a 50-pF load)
I_{CC} = current into the device (a measured quantity)

Devices separable into independent sections are measured on a "per section" basis. All others are measured on a "per device" basis. For example, C_{pd} for a quadruple 2-input NAND gate (HC00) is specified on a per gate basis, while C_{pd} for a synchronous 4-bit decade counter (HC160) is specified on a "per device" basis.

Since C_{pd} represents the power consumption due to current spiking, factors affecting current spiking also affect C_{pd}. One factor that could have a significant influence on C_{pd} is input rise and fall times. As input rise and fall times slow down, the amount of time that the p-channel and n-channel transistors are both partially ON increases. This results in an increase in the magnitude of the device switching current requirement, thereby increasing C_{pd}. The C_{pd} value, listed on device data sheets, was measured with a rise and fall time of 6 ns for HCMOS; 3 ns for ACL. Thus, a designer must be aware that input signals with slow rise and fall times could result in a device using more power than what had originally been expected. Figure 5.4-3 illustrates how C_{pd} varies as input rise and fall times increase.

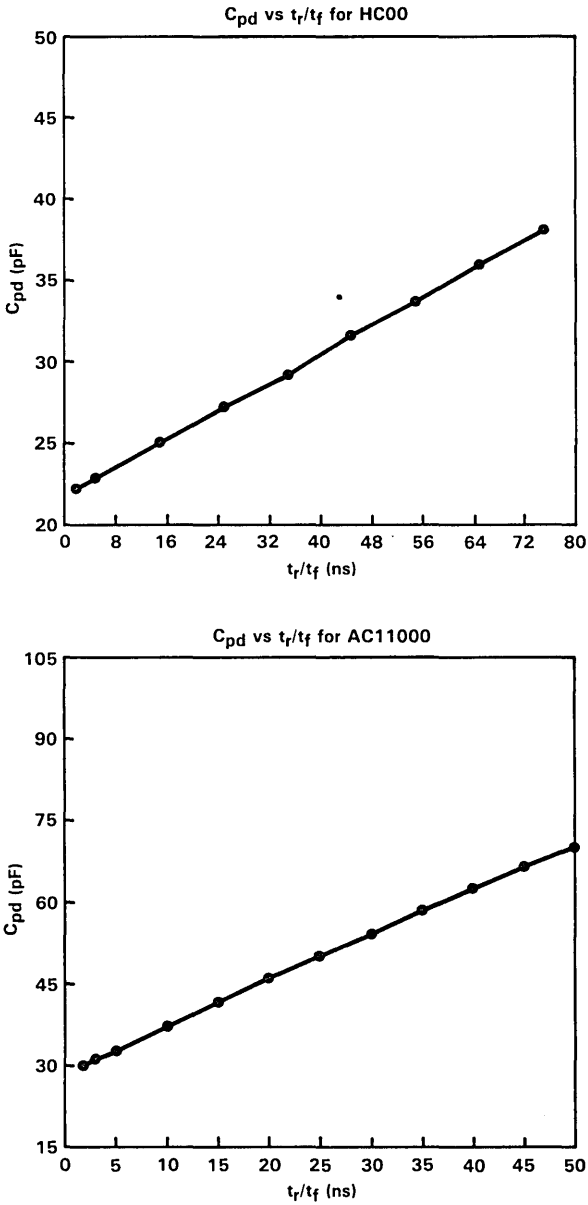
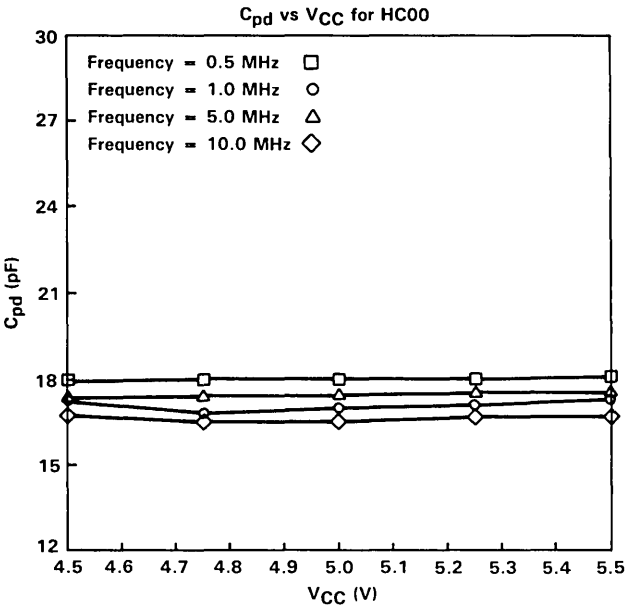


Figure 5.4-3. C_{pd} vs Input Rise and Fall Time



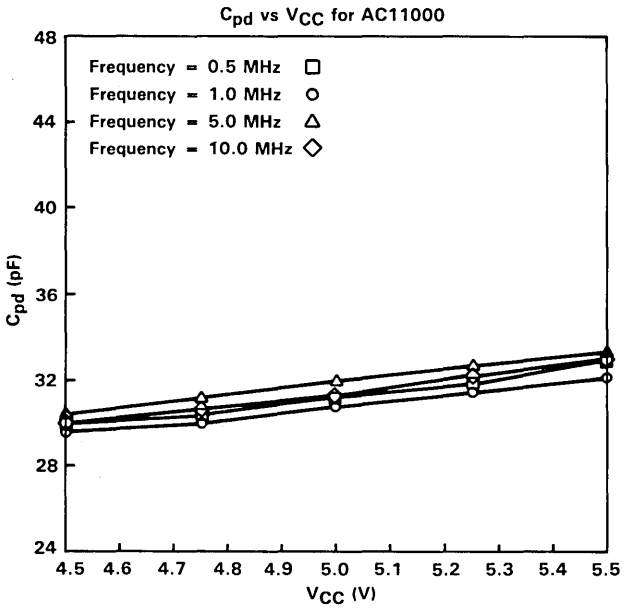


Figure 5.4-4. C_{pd} vs Input Frequency and V_{CC}

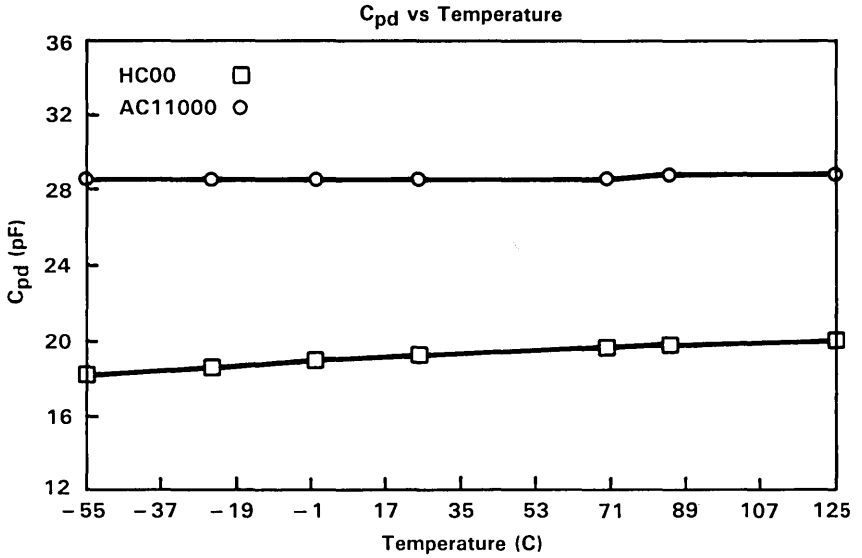


Figure 5.4-5. C_{pd} vs Temperature

The JEDEC test procedure for determining C_{pd} is performed at V_{CC} = 5 V, an ambient temperature of 25 °C, and a 1-MHz input frequency. To determine how C_{pd} varies under different conditions, tests are performed by varying supply voltage, temperature, and input frequency. Figures 5.4-4 and 5.4-5 show the results obtained when one condition varied and the others were held constant for both HCMOS and ACL. From the figures, it can be seen that the variance in C_{pd} is less than 10% as input frequency is varied between 500 kHz and 10 MHz; less than 5% as V_{CC} is varied between 4.5 and 5.5 V. A variation of less than 5% is also observed in C_{pd} as the ambient temperature varied from −55 °C to 125 °C.

The formula for dynamic power consumption also takes into account the power required to charge output load capacitance. The power needed to charge a load capacitance appears to a power supply as part of the total power requirement of the device. The formula for C_{pd} subtracts the load capacitance present when the test is performed, making the parameter independent of load capacitance. This yields a C_{pd} value that can be used to calculate the dynamic power consumption for devices driving either 50 pF or 150 pF.

5.4.6 Summary

The total power consumption of a CMOS device can be determined by adding the quiescent power and dynamic power requirements together. The following formulas can be used to calculate the total power consumption for CMOS devices:

For HC or AC

$$P_T = [V_{CC} \times I_{CC}\,(\text{total})] + [C_{pd} \times V_{CC}^2 \times F_i] + \Sigma\,(C_L \times V_{CC}^2 \times F_o)$$

For HCT or ACT

$$P_T = V_{CC} \times [I_{CC} + (N \times \Delta I_{CC} \times dc)] + [C_{pd} \times V_{CC}^2 \times F_i] + \Sigma\,(C_L \times V_{CC}^2 \times F_o)$$

where:

I_{CC} (total) = total quiescent current (usually I_{CC} from the device data sheet)
C_{pd} = power dissipation capacitance (from the device data sheet)
F_i = input frequency
C_L = output load capacitance
F_o = output frequency
N = number of inputs driven by a TTL device
dc = duty cycle
ΔI_{CC} = increase in supply current (specified on device data sheet)
I_{CC} = quiescent supply current (specified on device data sheet)

When trying to keep power consumption to an absolute minimum, remember input voltage levels and slow input rise and fall times can affect power usage. The least power usage occurs when input voltage levels are less than 1 V for V_{IL} and greater that $V_{CC} - 1$ V for V_{IH}, and input rise and fall times are less than 10 — 15 ns.

5.5 Reprint of Super-Speed Pc-Board Interconnects

Printed-circuit boards are no longer the simple, inexpensive interconnects they once were. Higher speed circuits and high-density packaging all call for special layout considerations, smaller traces, and many board layers. Designing these boards is no simple job.

By Larre Nelson
Marketing Manager
Augat Interconnection
Systems Group
Attleboro, Mass.

Fasten your seatbelts, because very-high-speed circuit interconnections are about to take engineers on a ride they'll never forget. There are places never heard of before, things never done before and a marvelous collection of exotic materials, processes and acronyms that are sure to keep everyone challenged.

The humble circuit-board interconnection, once merely a cheap mechanical platform, is becoming a critical element in the overall performance of very-high-speed systems. Designers, managers, and vendors that understand this will be the first to benefit from the remarkable advances in very-high-speed components, such as the VHSIC program and gallium arsenide (GaAs).

Most design and packaging engineers have discovered a profound but simple rule for very-high-speed circuit-board interconnections — keep them incredibly short. But there's more to it than running only short lines. The mechanical interconnections of very-high-speed logic take on the characteristics of passive devices in a high-frequency transmission line (like a waveguide in a microwave transmission line). Each of these passive elements must be carefully analyzed for its electrical effect on the signal characteristics, and carefully controlled in the manufacturing process to assure signal fidelity.

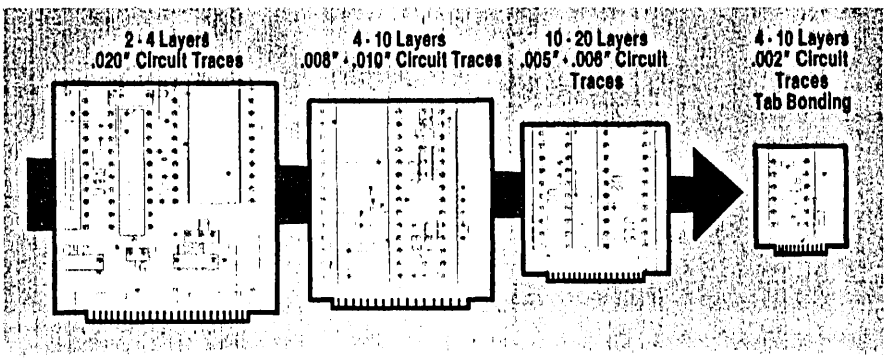
Even when two GaAs devices are placed as closely as 1 inch apart, the inter-device transmission-line propagation delay will still be nearly 200 ps — twice the 100-ps internal gate delay of a GaAs device. The resulting inter-device transmission line delay can neutralize any speed advantage gained by the use of the GaAs components.

Distributed capacitance along the path of a circuit-board signal line, combined with the lumped capacitance of neighboring vias, can cause additional propagation delays and enough variations in characteristic impedance to make a timing diagram useless. When high-speed circuit boards are made of materials with a high dielectric constant, the situation becomes even worse.

With signal rise times of GaAs components measured in picoseconds instead of nanoseconds, crosstalk becomes a monumental problem. It's controllable by adequate shielding of the signal lines, but shielding takes up space. Additional space makes the signal lines longer. And long signal lines result in greater propagation delays.

It's not even safe to assume that a high-speed signal will get from its source to its destination. Reflections due to impedance mismatches, and signal attenuation due to the material characteristics of the transmission lines and dielectric, can significantly distort a signal.

With all these worries, it's difficult to imagine the traditional circuit board being tossed into the arena of very-high-speed interconnections. But circuit board



It's no longer unusual to see complex, high-density boards that take advantage of as many as 20 layers or more, with trace widths as small as .005". Modern fabrication techniques, such as Tape Automated Bonding, reduce board and trace size still further, at the same time reducing the number of layers that are needed.

interconnections have come a long way from the early days of discrete wiring and single-sided circuit boards. Line dimensions have been reduced, the number of layers has increased and materials have changed. Terms like "eyelets" and "plated-through holes" are being replaced with "blind vias" and"Z-axis plated interconnects."

It's no longer unreasonable to find 10 to 20 layers, .018-inch vias and .005-inch line widths on signal layers. Additive processes and SMT components yield even .004-inch vias, .002-inch line widths and component lead pitches of .010-inch to .012 inch.

It's no longer assumed that glass/epoxy and copper are the materials of choice for a circuit board. Teflon, polyimide, Duroid, alumina and silicon dioxide are used instead. And gold, tungsten and aluminum are used instead of copper traces.

Even more significant than the interconnection's materials and dimensions is the use of the circuit board for more esoteric engineering purposes. Circuit boards can be made with metal cores for thermal management of the overall circuit. They can be made of multilayer co-fired alumina to provide a hermetic seal for each signal line. Mosaic Technology (Troy, Mich.) is even using a silicon wafer as the "circuit board" to keep the thermal coefficient of expansion (TCE) of the circuit board matched to the silicon dice, and to gain the highest possible density by using semiconductor photolithographic techniques.

Design Issues

Many of the difficulties experienced when interconnecting very-high-speed logic can be camouflaged if the interconnection is short. Reflections caused by end-of-line impedance mismatches occur early enough to avoid ringing, distributed capacitive loads (and the propagation delays they cause) are minimized because the capacitance of the line is too small to cause delays and crosstalk can't get started because the coupled lines aren't long enough.

Key strategies to keeping line lengths short include using very thin lines and multiple routing layers, avoiding vias and using components that do not require through-hole mounting. SMT components also offer some additional design freedom by allowing the use of blind and buried vias.

Propagation delays can also be reduced by using materials like Teflon, Duroid or polyimide that have lower dielectric constants. The formulas for calculating the correct characteristic impedance don't change, only the dielectric coefficients

change. But circuit-board manufacturing parameters change a lot. For example, Teflon is rarely used for multilayer construction because of the lack of associated drilling and lamination costs. Polyimide requires a higher temperature for its glass transition. A walk through a multilayer co-fired ceramic factory will reveal very few pieces of equipment or processes in common with a pc shop.

The requirement to control characteristic impedance on the signal lines at high frequencies leaves very little room for dimensional tolerances. Signal-line dimensions have to be very consistent, and they must maintain a very uniform distance from the influence of ground.

The undercutting and over-etching of a traditional, subtractive copper-etching process will cause high-frequency signals to travel on the skin of the signal line. Uncontrolled shrinkage in the ceramic firing process not only adversely affects flatness, but also changes the relationship of a signal line to its neighboring signal and ground influences. The resulting uncontrollable variations in characteristic impedance will either make the circuit useless, or will cause each unit to act in a unique manner: certainly an engineering headache.

The greatest cause of signal reflections for high-speed logic is the high end-of-line impedance encountered at the input pin of the receiving device. To minimize this effect, some designers are even placing end-of-line terminating resistors inside the semiconductor packages to keep the stubs as small as possible.

Very-high-speed logic presents a particularly interesting problem in controlling crosstalk. The necessity to package circuits densely and keep propagation delays to a minimum requires that signal lines be placed in close proximity to the minimum of distributed capacitance. It's a genuine breeding ground for crosstalk. Typically, the answer is a good ground plane (or multiple ground planes), but coaxial signal line construction is also used.

Most high-speed circuits have a greater than average need for good thermal management. Most component cooling is done by directly contacting the surface of the component with a cooling gas or liquid. However, circuit boards can also assist in thermal management. Some circuit boards have been "cored" like a radiator, to allow cooling fluids to pass inside. Some circuit boards have solid metal cores for convection cooling. Vias in this type of board can play a unique and useful role in distributing heat from the devices to the metal cores.

Simulation is also playing an important new role. Actual signal-line characteristics can be added to the net-lists of a schematic and timing diagrams can be compared. The resulting waveforms can be used to calculate worst-case timing or overall interconnection-capacitance budgets.

Traditional glass/epoxy circuit boards are not often used in very-high-speed applications. Restrictions in materials, routing techniques and manufacturing processes make the lines too long, and the propagation delays unacceptable, in many high-frequency uses. However, great improvements have been made possible through the use of SMT components. Removing the component mounting holes throughout the circuit board makes the signal-line routing easier and more dense, and reduces the undesirable capacitive effect of the plated-through holes on neighboring signal lines.

Progress is also being made in reducing the size of vias. Belie Circuits (Costa Mesa, Calif.) is using micro-drilling and precision electroplating techniques to obtain vias with a 10-1 aspect ratio on 10-layer boards (.0125-inch vias on

.125-inch-thick circuit boards). Small vias open up multilayer channels and reduce the capacitive effects of larger vias. That all adds up to denser layouts, shorter lines and shorter propagation delays.

But it's FR-4's dielectric constant (4.6) and its TCE that really act as roadblocks. The high TCE requires the use of strain-relieving leads on the components. But, these same leads have an undesirable inductive effect at high frequencies. Teflon and Duroid, with dielectric constants of 2.2 to 2.5, and polyimide, with a dielectric constant of 3.8, are far better suited for very-high-speed logic.

Polyimide is used in Augat Microtec's circuit boards, but not only because of its lower dielectric constant. Polyimide circuit boards also have a higher operating temperature (250°), and, because it's available as a prepreg, multilayer construction is possible.

The Microtec process, developed by Sandy Lebow and Dan Nogavich between 1974 and 1979 (when their company was known as Pactel), is a highly unconventional process for circuit-board fabrication that more closely resembles something found in the semiconductor business. By using additive plating, plasma etching and surface polishing, line widths can be as small as .002 inch and vias as small as .004 inch—nearly an order of magnitude improvement over the conventional processes.

Each layer of circuit interconnect or power plane is built on top of a previous layer in a sequential manner. Solid copper vias can be used for either interlayer, "Z-axis" signal interconnects or as thermal columns. When GaAs devices are used, signal line structures can be layered between ground planes and alongside ground barriers to form a "rectangular coaxial cavity" for a 360° ground shield. This not only gives excellent control of characteristic impedance, it also significantly reduces crosstalk. Fifty-ohms lines have been produced using signal lines that have a rectangular cross section of .004 inch × .001 inch on a pitch of .028 inch.

Multilayer, co-fired, ceramic chip carriers are very popular for pin-grid array (PGA) and surface-mounted device (SMD) packaging for a single die. Due to its low TCE and excellent hermeticity, ceramic substrates are also popular in hybrid and circuit-board applications, where environmental issues are important. Historically, the cofired ceramic manufacturing process has been very difficult to control, and substrates have been very limited in size. But Ceramic Systems (Anaheim, Calif.) is now producing 12-layer circuits up to 6 × 9 inches with .005-inch line widths. Although the signal-line densities are good enough for most high-frequency applications, ceramics are limited by the high dielectric constant of the alumina (9.9) and the high resistivity of the tungsten signal lines. Shrinkage of the ceramic in the firing process also makes the control of the characteristic impedance very difficult.

Kollmorgen has a variation of their popular Multiwire circuit boards that uses a coaxially constructed discrete wire instead of a "magnet" wire. The coaxial wire offers a controlled-impedance transmission line with low crosstalk, and it has a low-dielectric material. The wires are routed on the internal layers of the circuit board and brought to the surface of the circuit by vias to facilitate SMD mounting of the circuit board.

Published results for GaAs (or other very-high-speed logic) interconnections on

circuit boards are just starting to appear. And the seemingly endless barriers to progress are beginning to crumble.

Barry Gilbert of the Mayo Foundation (Rochester, Minn.) recently found that digital GaAs circuit performance on ceramic and polyimide substrates is dramatically different. Voltage Standing Wave Ratio (VSWR) measurements concluded that polyimide substrates have acceptable performance up to 6 to 8 GHz, but that the variations in characteristic impedance found in a multilayer ceramic substrate resulted in a frequency limit of only 3 GHz. They also found that placing the terminating resistors inside the substrate made a significant difference, increasing the frequency limit on the polyimide substrate from 6 GHz to 8 GHz.

Gigabit Inc. (Newbury Park, Calif.) is using multilayer polyimide substrates with equal length coaxial signal lines in the construction of their GaAs test fixtures. The test fixtures are connected to the signal generators with matched impedance cables and SMA connectors. The net result is a test fixture/device package with matched impedance, equal propagation delays per signal and insignificant skew.

5.6 Reprint of High-Performance Logic Places New Demands On Backplane Interconnects

When many signals are switching at the same time in a high-speed system, the effect on signal integrity can be staggering. Reducing crosstalk and noise can best be done where they are most often induced—at the motherboard/daughterboard connection.

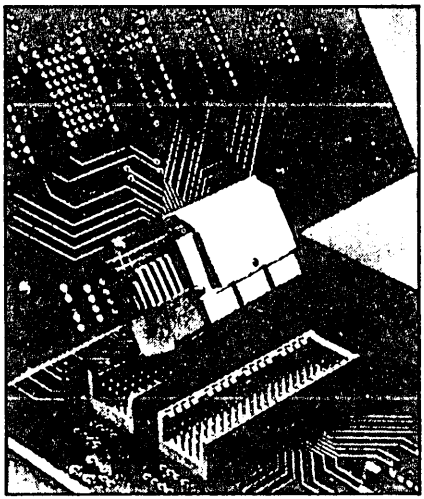
By Mark Gailus
and Christopher Heard
Development Engineers
Teradyne Connection Systems

Computer architectures for large word sizes, coupled with faster logic rise times, create special noise problems that can only be solved at the card-to-backplane connection.

Modern high-speed digital equipment typically is designed around a set of removable modules or daughtercards, which plug into and are interconnected by means of a high-density backplane containing rows of backplane connectors.

The noise problems that arise in daughtercards and printed circuit backplanes are generally well understood, as are the methods for their control. Crosstalk between signals, for example, can be limited by avoiding long parallel signal runs, and by incorporating ground and dc-voltage planes into cards and backplanes. These fixed-voltage layers also permit control of trace impedance and, together with the use of bypass capacitors, they serve to reduce noise on power and ground conductors.

Noise arising in backplane connectors, on the other hand, has received less attention. Future digital systems, which increasingly will use gate arrays and higher speed logic families, are likely to require greater numbers of backplane signal interconnections, coupled with faster signal rise times and a higher probability of simultaneous switching. These conditions can make control of connector-induced noise, in the form of crosstalk and ground bounce, a vital factor in maintaining signal integrity throughout the system.



This backplane connector has two integral ground planes to reduce crosstalk.

Simultaneous switching noise can be a problem at all packaging levels. When one line switches between cards, there is concern about signal reflections and crosstalk to neighboring lines. But, thanks to the

redundancy of ground interconnection, transient noise voltages across the ground interconnection are usually negligible.

This isn't the case when many lines switch simultaneously. First, simultaneous switching produces a high level of crosstalk to nearby quiet signal lines. If these are all lines in a synchronous data bus, high levels of transient noise frequently can be tolerated, provided that the signal levels settle adequately within one timing period.

A second, perhaps greater, concern that arises when many lines switch simultaneously is the possibility of significant noise induced onto quiet lines that aren't directly adjacent to the switching lines. This can happen because the distant lines share the same board-to board ground connections with the switching lines. Such noise can have disastrous consequences in the case of clock lines or other asynchronous control lines that connect to the same card.

Simultaneous switching noise currently is the subject of much discussion and effort in chip-to-card interconnections. A good example is the revised IC pinouts implemented by several manufacturers of high-speed CMOS logic to avoid "ground bounce" (see *EE Times*, Sept. 29, Page T44). This noise problem is a result of the finite inductance of chip-to-card ground and power connections.

When many output lines switch at the same time in the same direction, this inductance can cause local ground voltage on the semiconductor die to "bounce" with respect to ground on the printed circuit card. Basically, the same problem can occur in card-to-backplane interconnections, but the three-dimensional geometry, large number of parallel pins and absence of any reference ground plane in conventional backplane connectors makes analysis in terms of a lumped ground inductance less helpful.

These connectors typically consist of an array of signal contacts three or four rows wide by 15 or more inches long, and may contain more that 600 individual conductors. Defining the high-frequency electrical characteristics of such a connector is no simple task.

In a coaxial cable connector, the dimensions of the signal conductor and concentric ground shield are crucial to determining high-frequency properties such as impedance, capacitance and inductance. A large, multipin backplane connector, however, generally has no fixed ground-return structure. As a result, its characteristics for high-frequency signals are totally dependent on which pins in the connector are used for ground or fixed voltages.

In general, assigning more connector pins to ground will reduce noise because of the interconnection. Using more contacts for ground connections however, leaves fewer pins for routing signals, so that there's a trade-off between requirements for signal integrity and interconnect density.

Ground bounce cannot be solved on the daughtercard alone. To illustrate this, it is useful to distinguish between two different types of transient currents on the ground and fixed voltage conductors: supply current to the logic devices themselves, and the return currents associated with switching signal lines that run off the card.

When a logic buffer on a daughtercard switches its outputs, it draws a transient current through its power supply connections. CMOS usually has the highest such noise, ECL the least and TTL an intermediate value. Without adequate bypassing on the daughtercard: this transient current must be drawn through the connector from the backplane, resulting in noise

Put To The Test

It may be helpful to examine a simple hardware demonstration. This demonstration illustrates the effect of grounding within the board-to-board interface on system noise.

In this experiment, high-speed TTL bus transceivers (type 74F245) were used to drive a 32-line mini-backplane bus. Identical transceivers were set as receivers on a second card located 1 inch away along the mini-backplane. A split termination network (per VME spec) was used at both ends of the bus. Four lines of the 32, one in each row of the connector, were disabled and tied low.

These contracts were surrounded by switching lines and therefore represent worst-case near-line crosstalk conditions within the bus. In addition, four other quiet lines were located in a separate area of the connector to simulate critical clock or other asynchronous control lines outside the bus. Noise on these lines is known a "farline crosstalk".

In this test, the 32-bit bus is routed through an area of 8 4 pins. There are no signal pins dedicated to ground in this block of 32 pins. There is a "column" of ground located adjacent to this block of pins on each side, following the common practice of creating an electromagnetic "fence" shielding the 32-bit bus from the four asynchronous control lines.

Adding a single ground row to the contact pattern reduces crosstalk in all rows of the connector, especially in the rows closest to that ground plane.

When another row is added, crosstalk in the other rows is significantly reduced, because they too are near a ground plane. Crosstalk in the first two rows is also lower, resulting in uniformly lower crosstalk in all rows of the connector.

Careful attention to grounding in the connector is crucial to controlling noise in high-speed, TTL, 32-bit, board-to-board interconnections.

voltage across the connector. Providing adequate bypass across the connector. Providing adequate bypass capacitance on the transmitting daughtercard acts to confine high-frequency supply currents to the daughtercard, eliminating this source of noise.

When signal lines that run off the card are switched, however, there are always high-frequency transient currents in the connector ground and voltage connections. This noise is developed regardless of the particular logic family employed. It's simply a fact of life whenever signal transmission lines running off card are switched. To control this noise, it's crucial that adequate, distributed ground connections be provided between daughtercard and backplane.

A simplified theoretical explanation of "ground bounce" is that it's a voltage developed across the inductance of the daughtercard-to-backplane ground connection when the value of the ground current changes. In real-world systems, however, it's difficult to measure this noise directly.

Noise on ground connections inherently involves radiated electromagnetic fields.

Such fields interact with the probes used for any attempt at direct measurement of a differential ground voltage.

However, a more practical approach is available. The bottom-line effect of ground bounce on system performance is to induce noise on quiet lines in the system. If no such noise is induced, then ground bounce is not a concern. This suggests that a good way to evaluate the effects of ground bounce in an interface with many lines switching simultaneously between cards is to measure "far-line crosstalk," the noise picked up by quiet lines in the same interface but located at some distance from the switching lines.

5.7 The Role of Integrated Circuits Decoupling in Electromagnetic Compatibility

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For most electronic systems, the primary source of radiated emissions is the printed circuit boards contained within that system.* Because of long trace runs carrying transient currents with a sizeable high frequency (HF) spectral content, PC boards are efficient radiators of electromagnetic interference (EMI). However, PC boards can be designed that will fully comply with Federal Communications Commission (FCC) standards using techniques specifically addressing this problem. A 10 dB to 20 dB improvement is not unusual in a comparison of functionally identical boards, one of which is carelessly designed and the other designed to minimize EMI. Often this is the single most cost effective means of reducing emissions to an acceptable level.

Power Distribution and Signal Interconnects

There are usually two primary sources of EMI on a PC board—*signal interconnects and the power distribution system.* Signal interconnects include all signal traces, terminations and the signal lead frame members within Integrated Circuit (IC) packages. The power distribution system consists of all power and ground traces, power and ground planes, bulk decoupling capacitors, local decoupling capacitors and the power and ground lead frame members within the IC packages.

It is very difficult to predict the relative importance of these two sources. In some systems, power distribution related emissions can be the source of over 95% of total emissions measured to be out of compliance. Often, the opposite is true. Since metal-oxide semiconductors (MOS) draw large transient currents from the power distribution system during switching, and require very small inter-device currents for changing the gate voltage on other MOS devices, the power distribution system tends to have a more pronounced effect on EMI than in the case of transistor-transient logic (TTL)-based systems.** The inter-device currents in a TTL system are much larger; therefore, signal interconnects are often a major source of EMI. Boards using a variety of IC families would fall somewhere in between these two extremes.

Signal interconnect design and routing and its effects upon EMI have received considerable attention, whereas the power distribution system has not. Frequently, signal interconnects are routed first and then the power and ground traces are routed wherever they fit. Local decoupling capacitors may be left out entirely or placed at a distance from the ICs they service. This sort of power distribution system will be an efficient radiator of EMI and also may be noisy enough to upset the operation of the board itself. For a PC board to have low noise and minimum EMI, the power

*EDITOR'S NOTE: If input-output (I/O) cables are included within the system, they often radiate at levels higher than those associated with printed circuit boards (PCBs) due to the antenna-farm effect.

**EDITOR'S NOTE: On a gate-for-gate basis, complimentary metal-oxide semiconductor (CMOS) sinks considerably less current than TTL. However, the packaging density of many MOS devices is so much greater than TTL, the next total gate current of MOS devices frequently exceeds TTL chips.

distribution system must be designed with the same care that the signal interconnects receive.

Reducing EMI

The power distribution system would not radiate at all if there were only a dc current demand. Integrated circuits, however, draw large transient currents during logic switching. These current pulses have fast rise and fall times and therefore have significant spectral content within the FCC regulated band (30 MHz-1 GHz). The faster the IC, the larger the portion of the spectrum falling within the band. However, speed is critical in electronic systems so increasing rise and fall times to reduce EMI is not a viable solution.

The next best solution is to contain these high frequency pulses in the smallest closed loop area possible, since EMI is a function of loop geometry and frequency. This is generally accomplished by using a local decoupling capacitor for charge storage and short interconnects to the IC. As long as the impedance of this decoupling loop is much lower than that of the rest of the power distribution system, the high frequency components of the current will remain almost entirely within this loop, thereby minimizing EMI (see Fig. 1). When the impedance of the loop is no longer much lower than that of the rest of the system, some fraction of the high frequency component will be carried on the larger loop formed by the power distribution traces and higher emission levels will result.

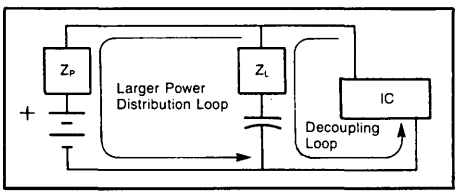


Figure 1. Power Distribution System Model.

The key, then, is to minimize the impedance of the capacitor and the interconnects. The capacitor, ideally, should have no lead inductance, low loss and stable capacitance through 200 MHz, and be as close to the IC as possible. Such a capacitor would have very low impedance and have an excellent ability to deliver current in the FCC regulated band.

Unfortunately, real capacitors are often far from the ideal. Most decoupling capacitors are Z5U grade barium titanate ceramic capacitors. Barium titanate is used because of its high dielectric constant which allows small capacitors to have relatively large capacitance values. This ceramic performs extremely well, both in terms of lossiness and capacitance, up to resonance which can vary from less than 1 MHz to nearly 20 MHz depending upon the formulation and packaging. Above resonance it becomes lossy and the capacitance begins to fall. This generally limits the effectiveness of a good Z5U capacitor to the 1 to 50 MHz frequency range.

Other dielectrics such as strontium titanate, NPO and some polymers have much better high frequency performance but have a low dielectric constant. This can make them unsuitable for low frequency (i.e., dc to 10 MHz) decoupling. There is, therefore, a tradeoff of high capacitance for low frequency decoupling versus low losses and stable capacitance for good high frequency decoupling.

If the PC board operates well with the relatively high levels of low frequency noise, which usually result from low-valued local decoupling capacitors, then they should be used as they do reduce emissions better than most high valued decoupling capacitors.

However, if this is not the case then some mix of the two types may be used. It is best to have the resonant frequency of the decoupling loop at or near the most troublesome frequency because the loop's impedance is lowest at that point. When mixing the two types of capacitors, do not put them next to each other as the high dielectric constant capacitor can damp the resonance of the more frequency stable, low-dielectric constant capacitor. In cases where the EMI problem is below 50 MHz, the best choice overall is a good, low inductance Z5U (or equivalent) capacitor because it combines excellent low frequency decoupling with reductions in radiated emissions up to that frequency.

All real capacitors also have some inductance. This inductance becomes the dominant component of the capacitor's impedance past resonance and therefore significantly affects high frequency performance. Most multi-layer capacitors have an intrinsic inductance of 5-8 nH because of their internal construction. There is on the market a series of flat, special decoupling capacitors and high capacitance PC board bus bars which, because of their parallel plate construction with integral taps, have an intrinsic impedance of 2 nH or less.

The impedance of the interconnect must also be minimized. This impedance is essentially inductive assuming normal copper thicknesses and trace widths; therefore, minimization of inductance is the key. The leads of the capacitor should be trimmed to an absolute minimum, for the least inductance. The interconnect traces should be short with the supply and return lines as wide as possible and preferably on opposite sides of the board aligned one above the other.

It can be difficult to place conventional decoupling capacitors close to the IC, particularly in systems with high packaging densities. For optimum EMI performance, a capacitor at each IC (or at least every other IC) is a necessity. This can cut packaging density by 5-20% depending on the exact configuration and type of capacitor used. The problem can be reduced by using flat capacitors of capacitive bus bars which share holes with the power and ground pins of the IC and take up no additional board space. Capacitive IC sockets can also be used in some applications to achieve higher packaging densities while placing the capacitor close to the IC.

Illustrative Example

To determine the effects of IC decoupling upon the radiated emissions of an electronic system, a simple PCB was fabricated which contained an Intel 8049 microcomputer IC, some driver transistors and a clock circuit. The 8049 ran a video game program contained in internal Read Only Memory (ROM). This circuit was selected because its radiated emissions would be largely attributable to the power distribution system. The board was operated in a 8.5 meter shielded chamber with a horizontally polarized antenna 90 cm above the board and on axis.

First, the board was run with no decoupling capacitors whatsoever. Figure 2 shows the radiated emissions for this test condition. Then 22 μF tantalum capacitor was placed at a distance of 13 cm from the 8049 chip for bulk decoupling. Figure 3 shows the relative emissions of this case versus no capacitors. By cutting down the decoupling loop by even this small amount, the emissions were reduced. Next, a 0.1 μF (MLC) Z5U capacitor was placed as close to the 8049 as possible (see Figure. 4). Substantial reductions in emissions are noted below 50 MHz with the greatest reductions in the 20 to 30 MHz range as shown in Figure 5.

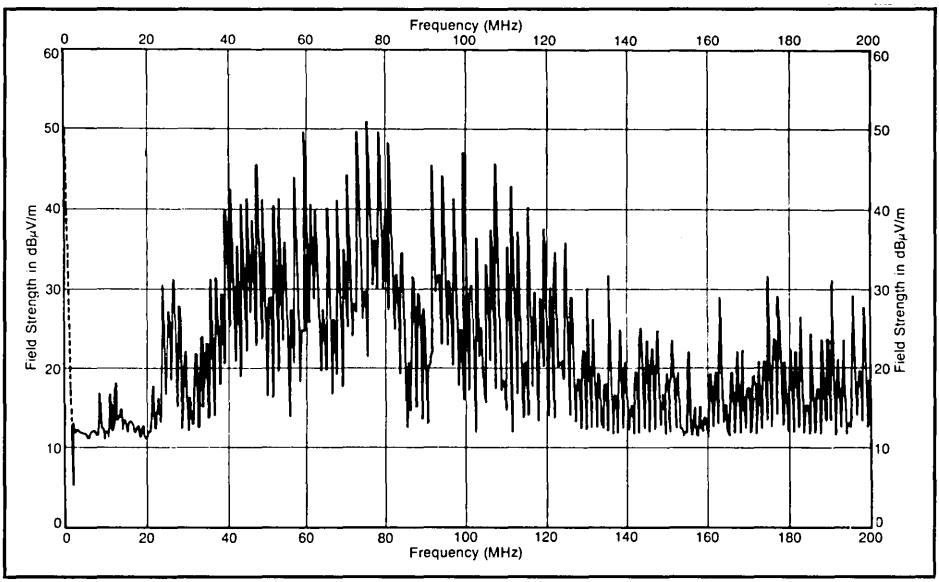


Figure 2. Radiated Emissions of the Test Board with No Decoupling Capacitors.

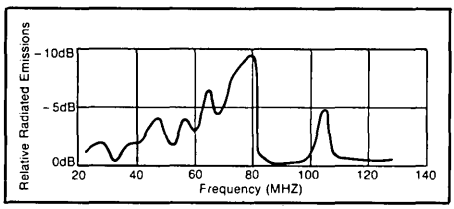


Figure 3. Relative Emissions of the Test Board with a 22 μF Bulk Decoupling Capacitor Versus None at All.

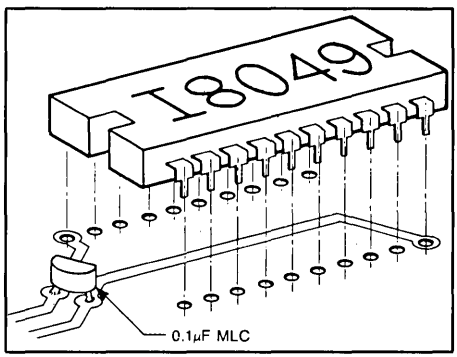


Figure 4. Decoupling Scheme Using a 0.1 μF MLC Capacitor.

Following the above test, the 0.1 μF capacitor was removed and a 0.03 μF Rogers MICRO/Q capacitor was placed under the IC (Figure 6). Due to its low inductive leads plus the fact that the field associated with traces has been eliminated, there exists substantial reductions (about 5 dB below 70 MHz and 2 dB above 70 MHz) as shown in Figure 7. The field is entirely contained within the capacitor, neglecting fringing effects which at these frequencies and a 25 mm dielectric thickness, is a good assumption. Capacitive PC board bus bars provide at least the same level of performance and, in most cases, an extra 1 to 3 dB reduction because they eliminate nearly all of the power and ground traces on the PC board. Lately, a special

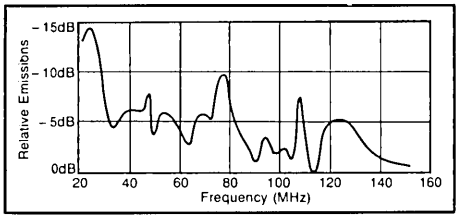


Figure 5. Relative Emissions of the Test Board with a 22 μF Bulk Decoupling Capacitor and a 0.1 μF MLC Local Decoupling Capacitor Versus No Decoupling.

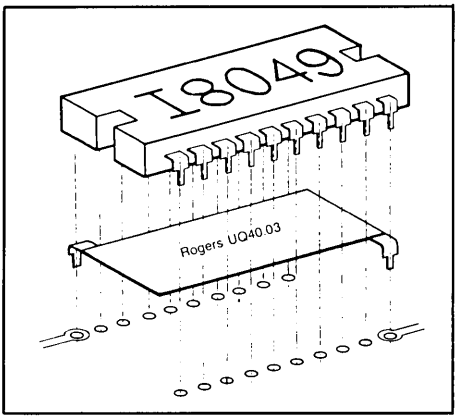


Figure 6. Decoupling Scheme Using a 0.03 μF Rogers MICRO/Q Capacitor.

900 pF flat capacitor utilizing a frequency stable dielectric was placed under the 8049. This capacitor, which resonates at approximately 50-60 MHz when serving a typical 40 pin DIP, substantially reduces emissions. It is particularly effective in the 20 to 80 MHz range (see Figure 8). The effect of this type of capacitor upon high frequency noise as measured on the PC board is shown in Figures 9 and 10. Figure 9 is the noise measured across the 8049 with the 0.1 μF MLC capacitor in place. Figure 10 is the same test except that

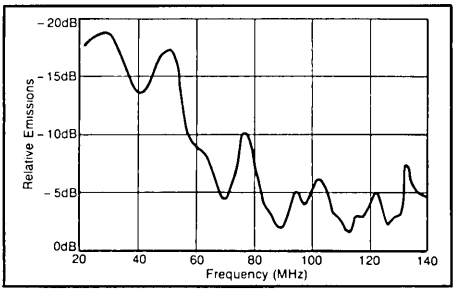


Figure 7. Relative Emissions of the Test Board with a 0.03 μF Rogers MICRO/Q™ Capacitor and a 22 μF Bulk Decoupling Capacitor Versus No Decoupling

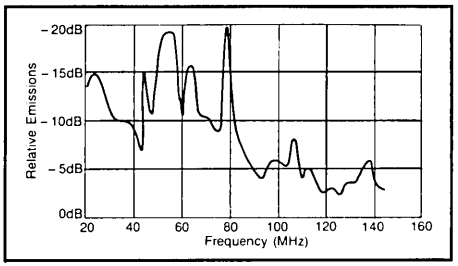


Figure 8. Relative Emissions of Test Board with a Special 900 pF Float Capacitor Manufactured by Rogers Corporation and a 22 μF Bulk Decoupling Capacitor Versus No Decoupling.

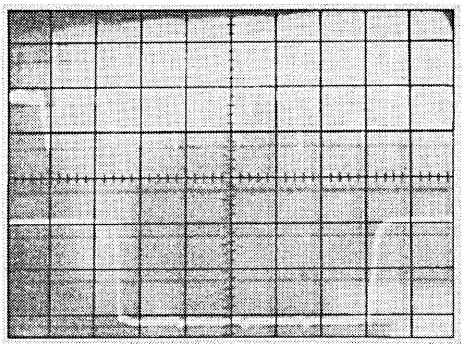


Figure 9. Noise on the Power Distribution System Using a 0.1 μF MLC Decoupling Capacitor (100 mV/div).

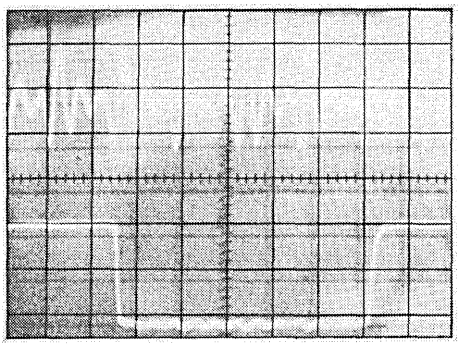


Figure 10. Noise on the Power Distribution System Using a Special 900 pF Flat Capacitor by Rogers Corporation Plus a 0.1 μF MLC Capacitor (100 mV/div).

the special 900 pF capacitor has been added (the 0.1 μF capacitor was still connected). The noise amplitude is virtually the same (approximately 300 mV) but the frequency spectrum has been shifted to a much lower frequency range. The board, therefore, radiates less EMI under these conditions.

Conclusions

Radiated emissions from PC boards come from some combination of emissions from the signal interconnects and the power distribution system. The design of both is very critical to the EMI performance of the PC board. One of the keys to good power distribution is proper IC decoupling. This is accomplished by minimizing the impedance of the decoupling loop to prevent high frequency noise from propagating on the power distribution trace system and, rather, confining it to as small a loop area as possible. To realize these goals, a low loss, low-inductance capacitor placed as close to the IC as possible and connected to the IC by low-inductance interconnects (traces or planes) is generally used. Flat capacitors and capacitive PC board bus bars are ideal for such applications because of their very low inductance. For this reason, they radiate less EMI than do conventional decoupling methods while having the added benefits of compactness and ease of retrofit.

Z5U capacitors can reduce EMI below 50 MHz while providing good low frequency decoupling. More frequency stable dielectrics produce good EMI at higher frequencies but at the expense of less efficient low frequency decoupling due to their lower dielectric constant. A combination of the two types can be used but they should not be placed side by side due to interactions that can negate the benefit of having a capacitor with frequency stability.

6 Quality and Reliability

6.1 ACL Reliability Summary†

6.1.1 Introduction

Texas Instruments places major emphasis on the quality and reliability of semiconductor products beginning with design and continuing through wafer fabrication, assembly, test, and final packaging. Stringent quality and reliability performance and manufacturing standards are defined prior to product design and release. Several product/process qualifications and evaluations are performed to ensure that these standards are met on every device released to market. This summary provides an overview of the technology and reliability performance of Texas Instruments capabilities in the EPIC™ Advanced CMOS Logic family.

6.1.2 EPIC™ 1-μm CMOS Process

Enhanced Performance Implanted CMOS (EPIC™), Texas Instruments 1-μm CMOS process, was derived from the technology used to develop the 1-megabit DRAM. Both high performance and high reliability are designed into the EPIC™ process. The design process is shown in Figure 6.1-1. Some of the features of the process are as follows:

- 1.0-μm gate length for sub-nanosecond on-chip propagation delays
- Silicide gate-source-drain to reduce internal interconnect resistance, allowing further speed enhancements
- Sidewall oxidation between gate-source and gate-drain to reduce internal capacitance, allowing further speed enhancements
- Epitaxial substrate layer for latch-up suppression
- Copper-doped aluminum metal to protect against electromigration, providing reliability enhancement
- Twin-well structure for high packing density, providing a vehicle for future LSI/VLSI product development.

†Written by T. Holmes.

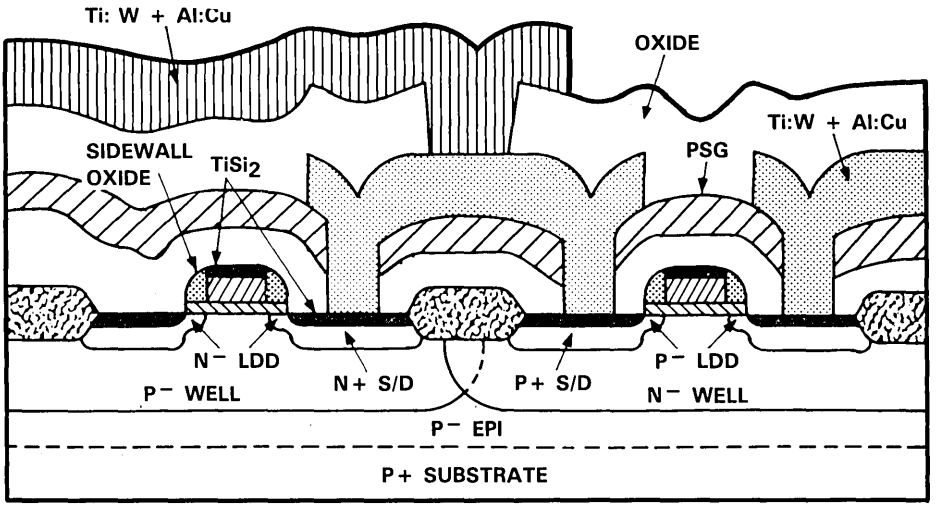


Figure 6.1-1. EPIC™ 1-Micron CMOS Process

6.1.3 Qualification Testing

Texas Instruments has a thorough qualification test program for EPIC™ ACL, as well as an ongoing reliability monitor. The reliability of EPIC™ ACL is measured by using the following major reliability tests.

1. Accelerated Life Tests
2. Bias Temperature Humidity Life Tests
3. Autoclave Tests
4. Temperature Cycling Tests

Numerous other tests are used to supplement the information provided by the major reliability tests. These additional tests include thermal shock, high-temperature storage, ESD sensitivity, thermal impedance, bond strength, lead bend and pull, solder heat, solderability, and flammability.

A description of these tests and a summary of the test results for typical EPIC™ ACL plastic devices are provided in the following paragraphs.

6.1.4 Accelerated Life Test

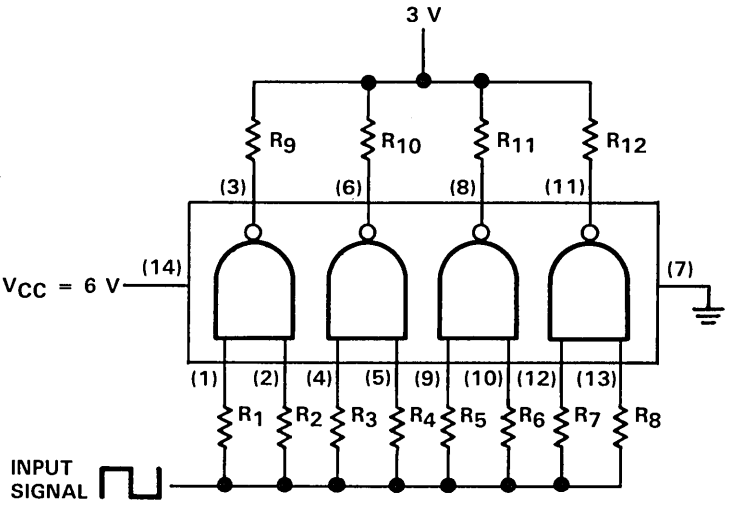
The accelerated life test is performed at elevated temperatures to simulate long-term operation and develop reliability data to predict field failure rates. The tests are conducted on EPIC™ ACL product using both dynamic and static bias techniques with 5.5 V applied and T_A = 125°C for dynamic and 150°C for static. A complete functional and 25°C dc parametric test is done at 0,

168, 500, and 1000 hours. The dynamic bias life test circuit shown in Figure 6.1-2 toggles the inputs from 0 to 5.5 V at 50 kHz. Each output is tied to 3 V through a 2-kΩ resistor. The static bias life test circuit (see Figure 6.1-3) sets the inputs and V_{CC} to 5.5 V, with the outputs allowed to float. Table 6.1-1 shows the life test results for the EPIC™ ACL family. Table 6.1-1 also lists the failure rate, in failure-in-time (FITs), using 0.96-eV activation energy.

Table 6.1-1. EPIC™ ACL Accelerated Life Test Results

				TEST INTERVAL IN HOURS: FAILURES/DEVICES ON TEST			
DEVICE	**CONDITION**	**T_A °C**	**LOTS**	**0**	**168**	**500**	**1000**
74AC11245	DYNAMIC	125	6	0/814	2/814	0/812	0/812
74AC11245	STATIC	150	6	0/1178	0/1178	0/1178	0/1178
74AC11000	STATIC	150	1	0/129	0/129	0/129	0/129
74AC11004	STATIC	150	1	0/129	0/129	0/129	0/129
74AC11008	STATIC	150	1	0/129	0/129	0/129	0/129
74AC11010	STATIC	150	2	0/258	0/258	1/258	1/257
74AC11011	STATIC	150	1	0/129	0/129	1/129	0/128
74AC11027	STATIC	150	1	0/129	0/129	0/129	0/129
74AC11030	STATIC	150	1	0/129	0/129	0/129	0/129
74AC11074	STATIC	150	1	0/129	0/129	0/129	0/129
Totals			21	0/3153	2/3153	2/3151	1/3149

Failure rate:	5.07 FITs (Failures/Billion hours)
Failure rate temperature:	55 °C
Activation energy:	0.96 eV
Acceleration factor:	125 °C — 393.781
	150 °C — 2060.481
Equivalent device hours:	1.130942E+09
Upper confidence level:	60%
Mean time between failures (MTBF):	1.226445E+09 hours or 140005 years



NOTES: 1. R_1 through R_{12} = 2 kΩ
2. Input Signal 0 to 5.5 V, 50% DUTY Cycle, 50 kHz.

Figure 6.1-2. Dynamic Bias Life Test Circuit

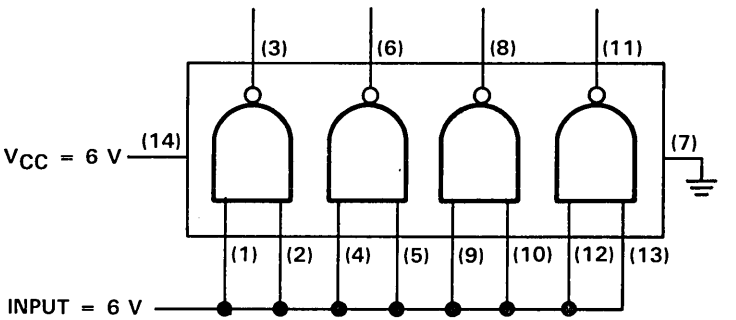


Figure 6.1-3. Static Bias Life Test Circuit

6.1.5 Bias Temperature Humidity Life Tests

Bias temperature humidity life testing is designed to evaluate the moisture-related performance of the package die combination. It is performed at a 5.5-V bias voltage at 85 °C and 85% relative humidity (RH) using the same circuit as the static bias life test. Electrical measurements are conducted at 0, 168, 500, and 1000 hours.

This is an accelerated test and uses stress levels considerably in excess of normal field use. The test is designed to accelerate moisture-related failure mechanisms occurring over many years of field use. Table 6.1-2 shows the results of bias temperature humidity life tests.

Table 6.1-2. Bias Temperature Humidity Life Test

		TEST INTERVAL IN HOURS: FAILURES/DEVICES ON TEST			
DEVICE	**LOTS**	**0**	**168**	**500**	**1000**
74AC11245	6	0/690	1/690	1/689	2/688
74AC11000	1	0/129	0/129	0/129	0/129
74AC11004	1	0/105	0/105	0/105	0/105
74AC11008	1	0/105	0/105	0/105	0/105
74AC11010	1	0/105	0/105	0/105	0/105
74AC11011	1	0/105	0/105	1/105	0/104
74AC11027	1	0/105	0/105	0/105	0/105
74AC11030	1	0/129	0/129	0/129	0/129
74AC11074	1	0/129	0/129	0/129	0/129
Totals	14	0/1602	1/1602	2/1601	2/1599

Failure Rate: 0.31% at 1000 hours
Condition: 85°C/85% Relative humidity with bias

6.1.6 Autoclave Test

The autoclave test is an environmental test of device reliability that involves exposing a device to an atmosphere of high-temperature, saturated steam under pressure. The device is exposed to 121 °C, 100% relative humidity at 15 psig. Unlike the bias humidity test, no electrical bias is applied to the device, and the test duration is somewhat shorter. Measurements are taken at 0, 96, 144, 192, and 240 hours.

This test measures the susceptibility of the device to galvanic corrosion and the chemical instability of the encapsulating material and its tendency to form electrolytes. Table 6.1-3 lists the results of the autoclave tests.

Table 6.1-3. Autoclave Test Results

		TEST INTERVAL IN HOURS: FAILURES/DEVICES ON TEST					
DEVICES	LOTS	0	96	144	192	240	384
74AC11245	5	0/364	0/364	0/364	0/364	0/364	1/364
74AC11000	1	0/77	0/77	0/77	0/77	0/77	0/77
74AC11004	2	0/129	0/129	0/129	0/129	0/129	0/129
74AC11008	2	0/104	0/104	0/104	0/104	0/104	0/104
74AC11010	2	0/129	1/129	0/128	0/128	0/128	0/128
74AC11011	1	0/52	0/52	0/52	0/52	0/52	0/128
74AC11020	1	0/77	0/77	0/77	0/77	0/77	0/77
74AC11027	1	0/52	0/52	0/52	0/52	0/52	0/52
74AC11030	1	0/77	0/77	0/77	0/77	0/77	0/77
74AC11074	1	0/77	0/77	0/77	0/77	0/77	0/77
74AC11240	1	0/77	0/77	0/77	0/77	0/77	0/77
74AC11373	1	0/77	0/77	0/77	0/77	0/77	0/77
Totals	19	0/1292	1/1292	0/1291	0/1291	0/1291	1/1291

Failure rate: 0.15%
Condition: 15 psig, 121 °C, 240 hours

6.1.7 Temperature Cycling

Temperature cycling is used to determine the compatibility of the materials used in device construction. The test requires cycling of the ambient temperature of the gas environment from a low temperature of −65 °C to a high temperature of 150 °C. These temperature extremes are not intended to simulate actual operation. They are intended to exaggerate any faults that might exist. No bias is applied to the device. Table 6.1-4 lists the results of the temperature cycling test.

Table 6.1-4. Temperature Cycling Test Results

		TEST INTERVAL IN CYCLES: FAILURES/DEVICES ON TEST			
DEVICE	LOTS	0	100	500	1000
74AC11245	5	0/1365	0/1365	0/1365	1/1365
74AC11004	2	0/390	0/390	0/390	0/390
74AC11008	2	0/390	0/390	0/390	0/390
74AC11010	2	0/390	0/390	0/390	0/390
74AC11011	1	0/195	0/195	0/195	0/195
74AC11020	1	0/129	0/129	0/129	0/129
74AC11027	1	0/195	0/195	0/195	0/195
74AC11030	1	0/195	0/195	0/195	0/195
74AC11074	1	0/129	0/129	0/129	0/129
74AC11240	1	0/129	0/129	0/129	0/129
74AC11373	1	0/129	0/129	0/129	0/129
Totals	18	0/3636	0/3636	0/3636	1/3636

Failure rate: 0.03%
Condition: −65°C/150°C

6.1.8 SNJ54AC Logic Family

The Military Products Department of Texas Instruments supplies military versions of the EPIC™ Advanced CMOS Logic family. Devices are available to the military temperature range or processed in compliance with MIL-STD-883C, Class B. All SNJ54 ACL devices are processed and screened per JEDEC STD 101.

6.1.9 Test Methods

MIL-STD-883, Method 5005, Class B is the guideline used for Groups B, C, and D testing to support Texas Instruments 883C, Class B processed integrated circuits program. Tables 6.1-5, 6.1-6, and 6.1-7 summarize the test methods used for Groups B, C, and D, respectively. For further information, refer to MIL-STD-883, Method 5005, Class B detail specification.

Table 6.1-5. Group B Test Methods (Package-Related Tests) SNJ54 ACL (see Note 1)

TEST	METHOD	MIL-STD-883 CONDITION	QUANTITY/ ACCEPT OR LTPD
Subgroup 1			
(a) Physical dimensions (see Note 2)	2016		2 (0)
Subgroup 2			
(a) Resistance to solvents (see Note 2)	2015		4 (0)
Subgroup 3			
(a) Solderability (see Note 3 & 4)	2003	Soldering Temperature of 245 ± 5°C	10
Subgroup 4		Failure criteria from	
(a) Internal visual and mechanical (see Note 5)	2014	design and construction requirements of applicable procurement document	1 (0)
Subgroup 5			
(a) Bond strength (see Note 6)			
(1) Thermocompression		(1) Test condition C or D	
(2) Ultrasonic or wedge	2011	(2) Test condition C or D	15

NOTES:
1. Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required.
2. Not required for qualification or quality conformance inspection where group D inspection is being performed on samples from the same inspection lot.
3. All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which have been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin fusing after burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than three devices be used to provide the number of leads required.
4. Leadless ceramic chip carrier devices are tested in accordance with MIL-STD-883 Rev B, and castellations are not included in the termination area inspected.
5. Test samples for internal visual and mechanical shall be selected at any point following seal operation, and following marking or re-marking (see 3.6.13 of MIL-M-38510). If sufficient electrical testing (including speed sort) is done after marking to verify the device types, the internal visual and mechanical test samples may be selected at any point following the seal.
6. Test samples for bond strength may, at the manufacturer's option, unless otherwise specified, be randomly selected prior to or following internal visual (PRESEAL) inspection specified in Method 5004, prior to sealing, provided all other specifications requirements are satisfied. Unless otherwise specified, the LTPD sample size for condition C or D is the number of bond pulls selected from a minimum number of four devices and, for condition F or H, is the number of die (not bonds) (see Method 2011).

Table 6.1-5. Group B Test Methods (Package-Related Tests) SNJ54 ACL (see Note 1) (Continued)

TEST	METHOD	MIL-STD-883 CONDITION	QUANTITY/ ACCEPT OR LTPD
Subgroup 6			
(a) Internal water vapor content (see Note 7)		Not applicable. No package 1018 desiccant used, performed in D-6.	3 (0) or 5 (1) (see Note 8)
Subgroup 7			
(a) Seal (see Note 9)			
(1) Fine	1014	As applicable	5
(2) Gross			

NOTES: 1. Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required.
7. This test is required only if the package contains a desiccant. Unless handling precautions for beryllia packages are available and followed, 6.1.5-5 Method 1018, procedure 3 shall be used. See Note 8 of Table 6.1-5 and paragraph 4 of Method 1018 regarding delay in implementation of this requirement.
8. Test three devices; if one fails, test two additional devices with no failures.
9. This test is not required if either the 100% screen or sample seal test is performed between 3.1.16 and 3.1.20 of Method 5004.

Table 6.1-6. Group C Test Methods (Die-Related Tests) SNJ54 ACL

TEST	METHOD	MIL-STD-883 CONDITION	QUANTITY/ ACCEPT OR LTPD
Subgroup 1		184 hours at 150°C or	
(a) Steady-state life test	1005	1000 hours at 125°C	5
(b) End-point electrical parameters		As specified in the TI data sheet electrical specifications	
Subgroup 2			
(a) Temperature cycling	1010	Test condition C	15
(b) Constant acceleration	2001	Test condition E min. Y_1 orientation only	
(c) Seal			
(1) Fine	1014	As applicable	
(2) Gross			
(d) Visual examination (see Note 1)			
(e) End-point electrical parameters		As specified in the TI data sheet electrical specifications	

NOTE 1: Visual examination shall be in accordance with Method 1010 or 1011.

Table 6.1-7. Group D Test Methods (Package-Related Tests) SNJ54 ACL

TEST	METHOD	MIL-STD-883 CONDITION	QUANTITY/ ACCEPT OR LTPD
Subgroup 1			
(a) Physical dimensions	2016		15
Subgroup 2 (see Note 1)			
(a) Lead integrity (see Note 2)	2004	Test condition B2 (lead fatigue)	15
(b) Seal 13 (see Note 3)			
(1) Fine	1014	As applicable	
(2) Gross			
Subgroup 3 (see Note 4)			
(a) Thermal shock	1011	Test condition B min. 15 cycles min.	15
(b) Temperature cycling	1010	Test condition C 100 cycles min.	
(c) Moisture resistance (see Note 5)	1004		
(d) Seal			
(1) Fine	1014	As applicable	
(2) Gross			
(e) Visual examination (see Note 6)		Per visual criteria of Methods 1004 and 1010	
(f) End-point electrical parameters (see Note 7)		As specified in the TI data sheet electrical specifications	
Subgroup 4 (see Note 4)			
(a) Mechanical shock	2002	Test condition B min.	15
(b) Vibration variable frequency	2007	Test condition A min.	
(c) Constant acceleration	2001	Test condition E min. Y_1 orientation only	
(d) Seal			
(1) Fine	1014	As applicable	
(2) Gross			
(e) Visual examination (see Note 6)			
(f) End-point electrical parameters		As specified in the TI data sheet electrical specification	

NOTES:
1. Electrical reject devices from the same inspection lot may be used for samples.
2. For leadless chip carrier packages only, use test condition D.
3. Seal test (Subgroup 2b) need be performed only on packages having leads exiting through a glass seal.
4. Devices used in Subgroup 3, "thermal and moisture resistance," may be used in Subgroup 4, "mechanical."
5. Lead bend stress initial conditioning is not required for leadless chip carrier packages.
6. Visual examination shall be in accordance with Method 1010 or 1011.
7. At the manufacturer's option, end-point electrical parameters may be performed after moisture resistance and prior to seal test.

Table 6.1-7. Group D Test Methods (Package-Related Tests) SNJ54 ACL (Continued)

TEST	METHOD	MIL-STD-883 CONDITION	QUANTITY/ ACCEPT OR LTPD
Subgroup 5 (see Note 1)			
(a) Salt atmosphere (see Note 5)	1009	Test condition A min.	15
(b) Seal			
(1) Fine (2) Gross	1014	As applicable	
(c) Visual examination		Per visual criteria of Method 1009	
Subgroup 6 (see Note 1)			
(a) Internal water-vapor content	1018	5000 ppm maximum water content at 100°C	3 (0) or 5 (1) (see Note 8)
Subgroup 7 (see Note 1)			
(a) Adhesion of lead finish (see Note 9,10)	2025		15
Subgroup 8 (see Note 11)			
(a) Lid torque (see Notes 1 and 11)	2024		5 (0)

NOTES:
1. Electrical reject devices from the same inspection lot may be used for samples.
5. Lead bend stress initial conditioning is not required for leadless chip carrier packages.
8. Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample (i.e., 3 or 5 devices) fails, a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes, the lot shall be accepted, provided the devices and data from both submissions are submitted to the qualifying activity along with five additional devices from the same lot.
9. The adhesion of lead finish test shall not apply for leadless chip carrier packages.
10. LTPD based on number of leads.
11. Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead, or package body (i.e., wherever frit seal establishes hermeticity or package integrity).

6.1.10 Test Results

Due to its recent introduction, only limited data is available for the SNJ54 ACL family. Please contact the factory for detailed information.

6.1.11 Summary

Texas Instruments has made a commitment to quality that ensures continued reliability testing of new CMOS devices as they are designed and introduced. This is illustrated by the excellent quality seen in EPIC™ ACL devices and shown in the data presented in this section. In addition, a quality watch program to continually monitor the quality and reliability of production devices is in place and guarantees a consistent product of the highest quality on an ongoing basis.

6.2 Adapted from "The Impact of IC Quality and Reliability on Cost of Ownership"†

Abstract

Usually, IC procurement is based on a number of factors such as cost, delivery, service, etc. However, all too often the cost portion of this procurement equation is limited to purchase price only. This can lead to incorrect procurement decisions if "cost" is a significant factor in the procurement equation. The cost which should be used is the cost of ownership which includes purchase price, in-house quality adders, in-house reliability adders, and field reliability (warranty) adders.

Cost of Ownership

The true cost of ownership of ICs extends well beyond the obvious purchase price. In fact, the quality and reliability adders which must be added to the purchase price in order to arrive at the true cost of ownership may significantly exceed the purchase price. Thus, the true cost of ownership might be many times greater than the purchase price.

The IC quality and reliability adders come from board and system rework costs plus 100% screening costs incurred by the OEM (original equipment manufacturer) because of less than perfect IC quality (zero rejects) and reliability (zero failure rate). While significant progress has been made in the last few years by IC manufacturers in improving quality and reliability (see Figures 6.2-1 and 6.2-2 for typical TI results), it is not yet feasible to ship ICs with perfect quality and reliability. Therefore, the level of imperfection shipped by each IC supplier determines the magnitude of the IC quality and reliability adders shown below:

- In-house IC quality costs
- In-house IC reliability costs
- Field IC reliability (warranty) costs.

†TI Technical Report #03-85-17, written by Don Denton.

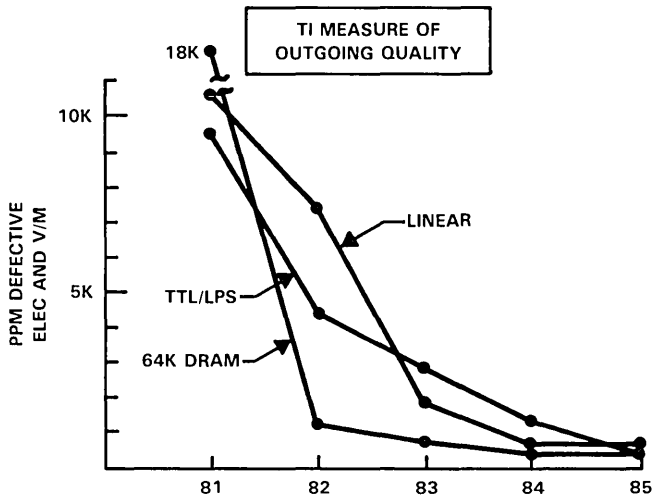


Figure 6.2-1. Improving Quality Trend

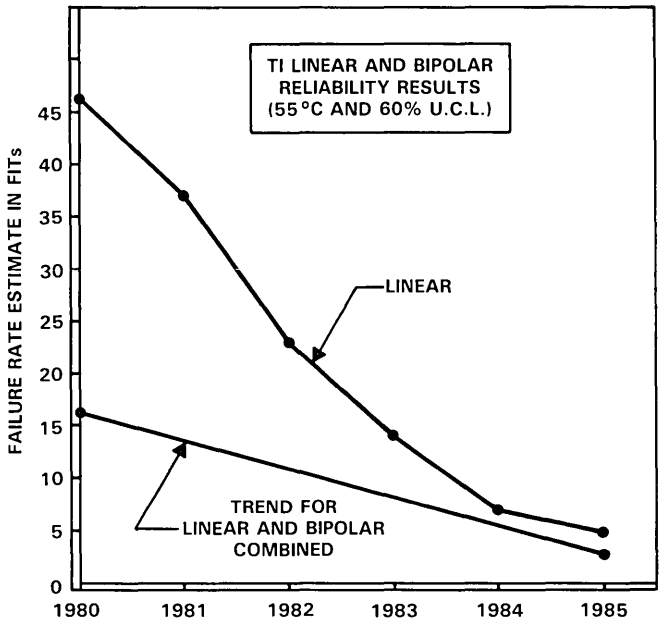


Figure 6.2-2. Improving Reliability Trend

Quality vs Reliability

It is important to distinguish the difference between quality and reliability. The terms are often used interchangeably, but they are different. Quality measures conformance to requirements at time "zero" in fraction defective.

$$\text{Quality} = \frac{\text{defects}}{\text{population}} \tag{1}$$

Reliability measures conformance to requirements after time "zero" as a rate in fraction defective per time period.

$$\text{Reliability} = \left(\frac{\text{defects}}{\text{population}}\right) / \text{ time period} \tag{2}$$

Based on equation (2), it could be said that reliability measures the change in quality with time. Quality is generally measured in PPM (parts per million) defective, while reliability is typically measured in FITs (failures/10^9 unit-hours).

In-House IC Quality Adder — Probability of Board Rework[1]

If perfect quality ICs were available, the OEM would not need any 100% screens or board rework operations to find and weed out defective devices. Even though industry quality levels are generally good (low PPM), this absolute defect level still impacts the OEM's board rework costs and his decision on 100% screens.

The major quality decision that the OEM must make is whether or not 100% screening is required. Many OEMs are moving toward a ship-to-stock program where all 100% incoming tests are eliminated. This approach is possible where the defect levels are very low. To determine how low is low enough, the probability of board rework must be calculated.

First, the binomial probability equation is used.

$$\text{Probability (no rework)} = \binom{n}{d} P^d Q^{n-d} \tag{3}$$

where

- n = units on board
- d = defects (for this case d = 0)
- P = decimal part of population defective
- Q = 1-P or decimal part of population good

See Table 6.2-1 for typical AOQ (average outgoing quality) and units/board values.

Table 6.2-1. Probability of Board Rework in %

UNITS ON BOARD	AOQ IN PPM				
	100	500	1000	5000	10,000
10	.10	.50	1.0	4.9	9.6
20	.20	1.0	2.0	9.5	18.2
30	.30	1.5	3.0	13.9	26.0
40	.40	2.0	3.9	18.2	33.0
50	.50	2.5	4.9	22.2	39.5
60	.60	3.0	5.8	25.9	45.3
70	.70	3.4	6.8	29.6	50.5
80	.80	3.9	7.7	33.0	55.2
90	.90	4.4	8.6	36.3	59.5
100	1.00	4.9	9.5	39.4	63.4

The probability of rework = 1-probability of no rework.

$$\text{Probability (rework)} = 1 - \binom{n}{o} P^o Q^{n-o} = 1 - Q^n \tag{4}$$

For a quality level of 1000 PPM, Q = 1 − .001 = .999. If the number of units on a board = 50, then Prob (rework) = 4.9%.

Next, the number of boards processed for a given time period — for example, one month — must be determined along with the average cost to rework a board. Assume that 1000 boards a month are processed and each board costs an average of $50 to repair.

This means that for a quality level of 1000 PPM with 50 units on a board, the monthly board rework cost estimate is

$$(1000 \text{ boards/month}) \times \left(4.9\% \frac{\text{reworked boards}}{\text{total boards}}\right) \times (\$50/\text{reworked board}) = \$2450/\text{month} \tag{5}$$

The decision on whether or not 100% incoming inspection is cost effective is determined by comparing the "cost of the screen" to the "savings resulting from the screen." When the following relationship holds

$$\text{cost savings} > \text{screening costs} \tag{6}$$

then the 100% incoming screen is cost effective. It is necessary to make an assumption regarding the improvement in quality, and the probability of board rework, that can be expected from the 100% incoming screen. For the purpose of this paper, it is assumed that the quality level can be improved by the 100% incoming inspection so that the probability of board rework will be reduced by 75%. This means that the quality level will be improved by about 80% (this varies somewhat with the number of units on the board).

Quality Cost Adder Calculation

The quality adder per unit (QA) is determined as follows. If 100% incoming inspection is not cost effective, then

$$QA_N = \frac{\text{total board rework cost without inspection}}{\text{total number of units}} \tag{7}$$

If 100% incoming inspection is cost effective, then

$$QA_E = \frac{\text{inspection cost}}{\text{unit}} + \frac{25\% \times (\text{total board rework cost without inspection})}{\text{total number of units}} \tag{8}$$

The 25% factor is used because it is assumed that 100% incoming inspection will reduce board rework by 75%.

Cost Adder for Maintaining an Inventory

With the advent of the just in time (JIT) manufacturing concept, the cost of maintaining an inventory for the supplier who cannot qualify for JIT must be considered as part of the total Cost of Ownership. A method for determining the cost-per-unit allocation for maintaining an inventory of parts is beyond the scope of this paper. However, for the purposes of the example at the end of the paper, it will be assumed that it costs $0.12/unit to maintain an 8-week inventory of parts which cannot qualify for JIT. The true cost for maintaining an inventory may vary widely from one company to another depending upon their cost structures.

Expected Failures — In-House and in the Field

In order to determine reliability adders, it is first necessary to find the number of expected failures which will occur both during in-house reliability testing and in the field during the first-year warranty period. Expected field failures (FF) are determined by the following equation:

$$FF = (\text{system-hours}) \times (\text{devices/system}) \times (\text{failures/device-hours}) \tag{9}$$

The failure rate (failures/device-hours) and system-hours must be converted to the same temperature. Also, the correct failure rate for the time period under investigation must be used. More will be said about this later.

Failure Rate Calculations and Assumptions

The well-known reliability bathtub curve, shown in Figure 6.2-3, has been used to represent the approximate shape of the instantaneous IC failure rate

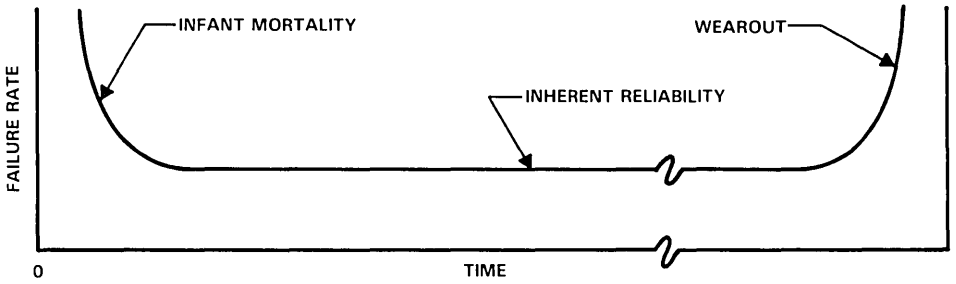


Figure 6.2-3. Reliability Bathtub Curve

from time zero to ultimate wearout with 100% failures. The system lifetime and operating conditions for most products are such that the right-hand wearout portion of the curve will never be experienced. For these products, after an initial period of high instantaneous failure rate, caused by infant mortality devices which have a tendency to fail early in life, a relatively flat portion of the curve is reached. This relatively flat portion of the curve is called inherent reliability (FR_I). It represents the reliability level which could be attained if the IC manufacturer could eliminate all infant mortality devices from his process. It also represents the reliability level that could be expected from an effective burn-in.

While it is recognized that IC failure rates follow the lognormal distribution[2] and are, therefore, not truly constant, the methodology of assuming a constant failure rate is still generally acceptable because it results in greatly simplified mathematical calculations and still provides reasonable accuracy.

Most major IC suppliers use this methodology for calculating the quoted failure rate estimates based on in-house reliability testing. Typically, reliability tests are run for 1000 (+8/−0) hours at 125 °C with one interim read point at 168 hours. The two failure rate estimates represent early life failure rate (FR_E) and quoted failure rate (FR_Q) and are:

$$FR_{168} = \frac{\text{failures}}{\text{units} \times 168} = FR_E \tag{10}$$

$$FR_{1000} = \frac{\text{cumulative failures}}{(\text{units}_{168} \times 168) + (\text{units}_{1000} \times 832)} = FR_Q \tag{11}$$

where

units_{168} = units completing 168 hours
units_{1000} = units_{168} − failures @ 168 hours

Developing the Model for the Reliability Cost of Ownership

A model can be developed by establishing a relationship among FR_Q, FR_E and FR_I at test temperature (typically, 125°C) and then derating them to a system-use temperature (typically, 55°C).

By extending the methodology of the previous section a little further, it is possible to derive three other variables which are needed to develop a model for cost-of-ownership analysis. The inherent reliability failure rate FR_I, which estimates the post burn-in failure rate, can be derived from the following equation

$$FR_Q = \left(\frac{EL}{1008}\right) \times FR_E + \left(1 - \frac{EL}{1008} \times FR_I\right) \quad (12)$$

where

EL = early life time period

This relationship is shown in Figure 6.2-4 and assumes that the quoted failure rate is an average of FR_E and FR_I.

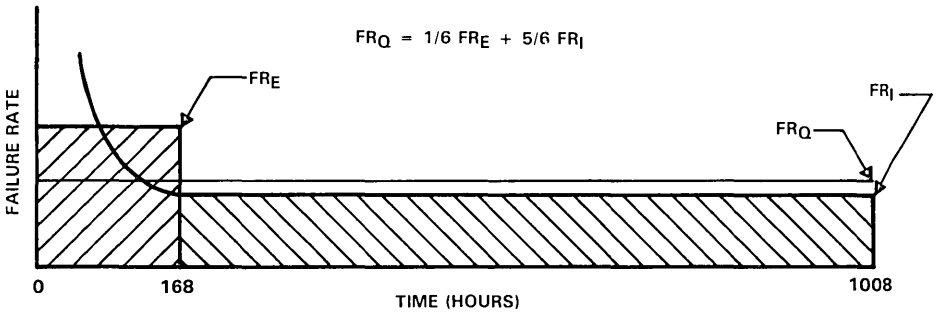


Figure 6.2-4. Relationships of FR_Q, FR_E, and FR_I

It is also possible to determine the failure rate improvement factor FR_{IMP} which could be expected from burn-in.[3,4]

$$FR_{IMP} = \frac{FR_Q - FR_I}{FR_Q} \quad (13)$$

Finally, the failure rate estimate for the first-year warranty period (without burn-in), $FR_{1st\ year}$, can be derived from the following equation

$$FR_{1st\ year} = \left(\frac{EL \times AF}{8760}\right) \times FR_E + \left(1 - \frac{EL \times AF}{8760}\right) \times FR_I \quad (14)$$

where

EL (early life) = 168 hours

and AF is the acceleration factor from the Arrhenius relationship.[5]

$$AF = e^{(+E/K)[(1/T_1) - (1/T_2)]} \quad (15)$$

where

E = activation energy
K = Boltzman's constant (8.61423×10^{-5} eV/K)
T_1 = absolute temperature of system operation
T_2 = absolute temperature of life test

A conservative activation energy (0.44eV) per Method 1015 of MIL-STD-883 is used in this case to relate test hours at 125 °C to equivalent hours at system temperature.

For 55 °C, which is a typical system temperature, the acceleration factor from equation (15) is 15.47 resulting in

$$FR_{1st\ year} = 0.3FR_E + 0.7FR_I \quad (16)$$

Figure 6.2-5 shows these relationships. Note that equation (16) is only good for 55 °C.

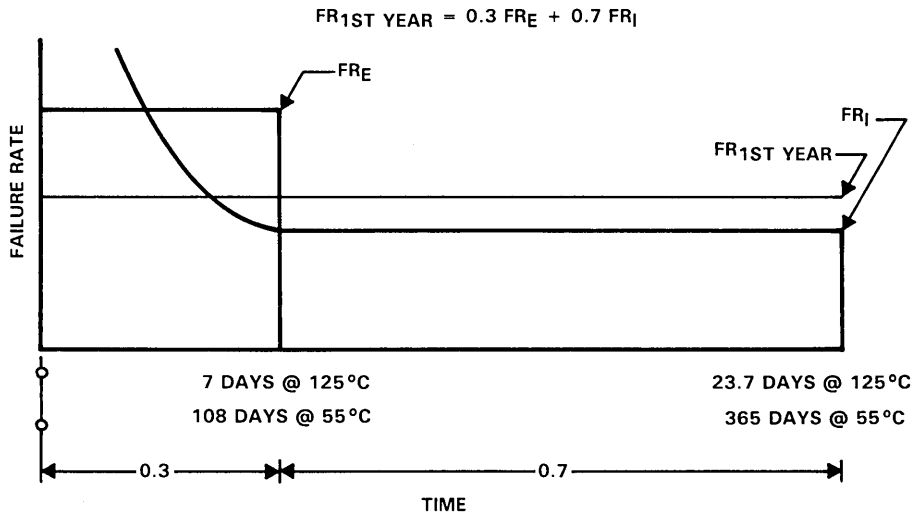


Figure 6.2-5. Relationships of FR_E, FR_I, and $FR_{1st\ year}$ for Warranty Calculations

OEM System Burn-In

Often, the OEM will perform some in-house, burn-in screen on the completed system. A typical burn-in screen might be for 48 hours at 55 °C. While this screen may be quite useful to detect assembly-related problems such as solderability, it is not very effective in screening out IC infant mortality devices unless the FR_E is very high. The reason is that the acceleration factor from the time and temperature used is not sufficient to yield many failures. The cost-of-ownership example shows how few failures this in-house screen generates.

In-House Reliability Costs

The in-house reliability adder per unit (IRA) is determined by using previously developed formulae. The expected failures from the in-house system burn-in are determined using equation (9) and substituting FR_E for failure rate. The total in-house system rework cost is the expected failures × system rework cost/failure. The in-house reliability adder is then

$$IRA = \frac{\text{total system rework cost}}{\text{total number of units}} \tag{17}$$

Field Reliability Cost

The first step is to determine the warranty cost of field failures during the first year. This requires a set of calculations assuming no component burn-in and then a second set of calculations assuming 100% component burn-in. To get expected field failures without burn-in, use equation (9) and substitute $FR_{1st\ year}$ for failure rate. Then use equation (9) and FR_I to calculate expected field failures with burn-in. Take the difference of these two numbers × cost to repair a field failure. This provides the delta field failure savings due to component burn-in. This delta field failure savings is then compared to the cost of 100% component burn-in. If the delta field failure savings are greater than the cost of 100% component burn-in, then burn-in is cost effective.

Reliability Cost Adder Calculation

If burn-in is not cost effective, the field reliability adder per unit (FRA) is calculated by

$$FRA_N = \frac{\text{(FF without burn-in)} \times \text{(cost per field failure)}}{\text{total number of units}} \tag{18}$$

If burn-in is cost effective, then

$$FRA_E = \frac{\text{burn-in cost}}{\text{unit}} + \frac{\text{(FF with burn-in)} \times \text{(cost/field failure)}}{\text{total number of units}} \tag{19}$$

Model Enhancements

A number of assumptions were made in order to develop the cost-of-ownership model. Additional data or experience may indicate that some of the assumptions should be changed for certain products. One area where additional data would be useful is in establishing a more precise time period for FR_E. The 168-hour time period was chosen in the model to represent FR_E because it is the standard time for burn-in and there was a large data base available. However, many products have already reached the FR_I portion of the failure rate curve after only 48 hours. If 48 hours was assumed to be the FR_E breakpoint, then equation (12) would become:

$$FR_Q = \left(\frac{48}{1008}\right) \times FR_E + \left(\frac{960}{1008}\right) \times FR_I \quad (20)$$

Also, it might be argued that, for the in-house system burn-in, the average FR_E might not be high enough to represent the expected instantaneous failure rate during the relatively short period of time typically used for system burn-in (e.g., 24 or 48 hours). To be conservative, it might be reasonable to use either 2× or 3× FR_E when calculating expected failures during in-house system burn-in. However, this would still result in relatively few failures during a short, 55 °C in-house system burn-in.

It might be desirable to change the model to a system operating temperature other than 55 °C. This can be done by using equation (14). If the period for FR_E is also changed to 48 hours, equation (14) now becomes

$$FR_{1st\ year} = \left(\frac{48 \times AF}{8760}\right) \times FR_E + \left(1 - \frac{48 \times AF}{8760}\right) \times FR_I \quad (21)$$

AF for the new system temperature would be calculated by using equation (15).

Equation Limits For Model Changes

There is a limit for equation (12) such that

if $EL \geq 1008$, then

$$FR_Q = FR_E \quad (22)$$

There is a limit for equation (14) such that

$$\text{if } \frac{EL \times AF}{8760} \geq 1 \text{ then}$$

$$FR_{1st\ year} = FR_E \quad (23)$$

Results of Model Changes

Finally, as system operating temperature increases and the early life time period EL decreases, the impact of burn-in on expected first-year failures is reduced. The reason for this is that the early life failure rate becomes a smaller part of the first-year failure rate with these changes.

Cost of Ownership Example

A cost-of-ownership example shows two hypothetical suppliers with different levels of quality and reliability and what impact this has on total cost of ownership.

The following assumptions have been made:

	SUPPLIER	
ASSUMPTION	**A**	**B**
Purchase Price	$.50	$.50
AOQ (PPM)	100	3500
Devices/Board	100	100
Boards/System	5	5
Systems/Month	100	100
Rework Cost/Board	$50	$50
100% Inspection Cost/Device	$.10	$.10
Cost/Unit to maintain inventory	$.00	$.12
In-House System Cost/Failure	$300	$300
In-House System Burn-in	48/hrs	48/hrs
FR_Q (FITs)	10	100
FR_E (FITs)	15	225
Burn-In Cost/Device	$.20	$.20
Repair Cost/Field Failure	$ 800	$ 800

Computer Printout Results†

The Total Cost of Ownership for Linear/Supplier "A"

FOR ONE MONTH'S PRODUCTION

PURCHASE PRICE	$ .5
QUALITY ADDER	$ .005
INVENTORY ADDER	$ 0
IN-HOUSE REL ADDER	$ 0
FIELD RELIABILITY ADDER	$ .08
TOTAL COST PER DEVICE	$ .585

THIS PRODUCT SHOULD BE CONSIDERED FOR SHIP-TO-STOCK

†Using TI Cost of Ownership Software

DETAIL PRINT OUT OF QUALITY VARIABLES FOR LINEAR/SUPPLIER "A"

AOQ (IN PPM)	100
UNITS/BOARD	100
BOARDS/MONTH	500
REWORK COST/BOARD ($)	50
PROBABILITY OF BOARD REWORK (%)	.9952009
NUMBER BOARDS REWORKED/MONTH	5
BOARD REWORK COST/MONTH ($)	250
INCOMING COST/UNIT ($)	.10
INCOMING INSPECTION COST/MONTH ($)	5000
100% INSPECTION REDUCES BOARD REWORK BY	.75
APROXIMATE BREAKEVEN AOQ (PPM)	3096
INCOMING COSTS > REWORK COSTS BY ($)	4750

DETAIL PRINT OUT OF RELIABILITY VARIABLES FOR LINEAR/SUPPLIER "A"

SYSTEM OPERATING TEMPERATURE (°C)	55
EARLY LIFE FAILURE RATE TIME (HOURS)	168
ACCELERATION FACTOR	15.47
QUOTED FR @ SYSTEM TEMP (FITs)	10
EARLY LIFE FR (FITs)	15
FR IMPROVEMENT FACTOR (%)	10.02401
FR 1ST YEAR (WITH NO BURN-IN) (FITs)	10.77842
INHERENT FAILURE RATE (FITs)	8.997599
COMPONENT BURN-IN COST/UNIT ($)	.20
IN-HOUSE SYSTEM BURN-IN TIME (HRS)	48
EXPECTED IN-HOUSE FAILURES	0
COST/IN-HOUSE SYSTEM FAILURE ($)	300
TOTAL COST FOR IN-HOUSE SYSTEM FAILURES ($)	0
EXPECTED FIELD FAILURES W/O BI	5
EXPECTED FIELD FAILURES WITH BI	4
DELTA (REDUCED) FAILURES DUE TO BURN-IN	1
REPAIR COST/FIELD FAILURE ($)	800
DELTA COST SAVINGS FROM BI ($)	800
TOTAL COMPONENT BURN/IN COST ($)	10000
BURN-IN WOULD INCREASE TOTAL COST BY ($)	9200

The Total Cost of Ownership for Linear/Supplier "B"

FOR ONE MONTH'S PRODUCTION

PURCHASE PRICE	$ .50
QUALITY ADDER	$ .137
INVENTORY ADDER	$ .12
IN-HOUSE REL ADDER	$ .006
FIELD RELIABILITY ADDER	$ .728
TOTAL COST PER DEVICE	$ 1.491

DETAIL PRINT OUT OF QUALITY VARIABLES FOR LINEAR/SUPPLIER "B"

AOQ (IN PPM)	3500
UNITS/BOARD	100
BOARDS/MONTH	500
REWORK COST/BOARD ($)	50
PROBABILITY OF BOARD REWORK (%)	29.57425
NUMBER BOARDS REWORKED/MONTH	148
BOARD REWORK COST/MONTH ($)	7400
INCOMING COST/UNIT ($)	.10
INCOMING INSPECTION COST/MONTH ($)	5000
100% INSPECTION REDUCES BOARD REWORK BY	.75
APROXIMATE BREAKEVEN AOQ (PPM)	3096
TOTAL COST SAVING FROM INCOMING INSPECTION ($)	550

DETAIL PRINT OUT OF RELIABILITY VARIABLES FOR LINEAR/SUPPLIER "B"

SYSTEM OPERATING TEMPERATURE (°C)	55
EARLY LIFE FAILURE RATE TIME (HOURS)	168
ACCELERATION FACTOR	15.47
QUOTED FR @ SYSTEM TEMP (FITs)	100
EARLY LIFE FR (FITs)	225
FR IMPROVEMENT FACTOR (%)	25.06002
FR 1ST YEAR (WITH NO BURN-IN) (FITs)	119.4605
INHERENT FAILURE RATE (FITs)	74.93998
COMPONENT BURN-IN COST/UNIT ($)	.20
IN-HOUSE SYSTEM BURN-IN TIME (HRS)	48
EXPECTED IN-HOUSE FAILURES	1
COST/IN-HOUSE SYSTEM FAILURE ($)	300
TOTAL COST FOR IN-HOUSE SYSTEM FAILURES ($)	300
EXPECTED FIELD FAILURES W/O BI	53
EXPECTED FIELD FAILURES WITH BI	33
DELTA (REDUCED) FAILURES DUE TO BURN-IN	20
REPAIR COST/FIELD FAILURE ($)	800
DELTA COST SAVINGS FROM BI ($)	16000
TOTAL COMPONENT BURN/IN COST ($)	10000
TOTAL COST SAVINGS REALIZED FROM BURN-IN ($)	6000

Summary

The cost of ownership adder difference between supplier "A" and supplier "B" is $0.906 (.991 vs .085). Another way to look at this is that the cost of ownership for supplier "B" is over 11X the cost of ownership for supplier "A". Recent data supplied to TI by a major customer verifies that a broad range does exist in cost of ownership between the best supplier and the worst supplier. Four product families were evaluated — LS, ALS, HCMOS, and FAST. The reliability cost of ownership as reported by this customer ranged from 3X to 14X between the best and worst suppliers for these four families.

Most equipment manufacturers have a good understanding of quality costs but not a good understanding of reliability costs. The reason for this is the difficulty and expense involved in tracking and analyzing field failures. However, with the tight competition in the electronics industry, equipment manufacturers are placing more emphasis on analyzing reliability costs as they search for ways to reduce total costs and increase profits while maintaining high quality and reliability of their products. With the advent of JIT, there is another cost factor (inventory) which must be examined along with the quality and reliability factors when calculating the total cost of ownership.

References

1. D. Denton, "Taking Fewer Steps Simplifies Program," *Quality*, September 1979, pp. 99-100.
2. D. S. Peck and O. D. Trapp, "Accelerated Testing Handbook," Bofors, Inc., San Mateo, California, 1981, pp. 2-4.
3. D. Denton and D. Blythe, "The Impact of Burn-in on IC Reliability," Proceedings of the National Conference and Workshop on Environmental Stress Screening of Electronic Parts, October 1985, pp. 59-67.
4. D. Pantic, "Questioning the Benefits of Burn-in," *Electronic Engineering*, July 1984, pp. 45-47.
5. D. Denton, "Program Converts Test Data Into Reliability Numbers," *Electronic Design*, August 19, 1982, pp. 157-164.

6.3 Reprint of Guidelines for Handling Electrostatic-Discharge Sensitive (ESDS) Devices and Assemblies†

Prepared by
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1 Scope

1.1 This specification establishes the requirements for methods and materials used to protect electronic parts, devices, and assemblies (items) susceptible to damage or degradation from electrostatic discharge (ESD). The electrostatic charges referred to in this specification are generated and stored on surfaces of ordinary plastics, most common textile garments, ungrounded people's bodies, and many other commonly unnoticed static generators. The passage of these charges through an electrostatic-sensitive part may result in catastrophic failure or performance degradation of the part.

1.2 The part types for which these requirements are applicable include, but are not limited to, those listed:

(a) All metal-oxide semiconductor (MOS) devices, e.g., CMOS, PMOS, etc.
(b) Junction field-effect transistors (JFET)
(c) Bipolar digital and linear circuits
(d) Op Amps, monolithic microcircuits with MOS compensating networks, on-board MOS capacitors, or other MOS elements
(e) Hybrid microcircuits and assemblies containing any of the types of devices listed
(f) Printed circuit boards and any other type of assembly containing static-sensitive devices.

1.3 Definitions

1.3.1 Antistatic material: ESD protective material having a surface resistivity between 10^9 and 10^{14} Ω/square.

1.3.2 Static dissipative material: Material having surface resistivity between 10^5 and 10^9 Ω/square.

1.3.3 Conductive material: ESD protective material having a surface resistivity of 10^5 Ω/square maximum.

1.3.4 Electrostatic discharge (ESD): A transfer of electrostatic charge between bodies at different electrostatic potentials caused by direct contact or induced by an electrostatic field.

† Written by D. Denton

1.3.5 Surface resistivity: An inverse measure of the conductivity of a material and is the resistance of unit length and unit width of a surface. Note: Surface resistivity of a material is numerically equal to the surface resistance between two electrodes forming opposite sides of a square. The size of the square is immaterial. Surface resistivity applies to both surface and volume conductive materials and has the value of Ω/square.

1.3.6 Volume resistivity: Also referred to as bulk resistivity. It is normally determined by measuring the resistance (R) of a square of material (surface resistivity) and multiplying this value by the thickness (T).

1.3.7 Ionizer: A blower that generates positive and negative ions, either by electrostatic means or by means of a radioactive energy source, in an airstream, and distributes a layer of low velocity ionized air over a work area to neutralize static charges.

1.3.8 Close proximity: For the purpose of this specification, is 6 inches or less.

1.4 Device Sensitivity per Test Circuit of Method 3015, MIL-STD-883

1.4.1 Devices are categorized according to their susceptibility to damage resulting from electrostatic discharge (ESD), and the type packaging required to adequately protect them.

1.4.1.1 Device electrostatic sensitivity

Category	ESD Sensitivity (V)	Minimum Protective Packaging
A	20-2,000	Antistatic Magazine & Conductive Bag/Box
B	> 2,000	Antistatic Magazine & Antistatic Bag

1.4.2 Devices are to be categorized by their sensitivity

1.4.3 Devices are to be protected from ESD damage from receipt at incoming inspection through assembly, test and shipment of completed equipment.

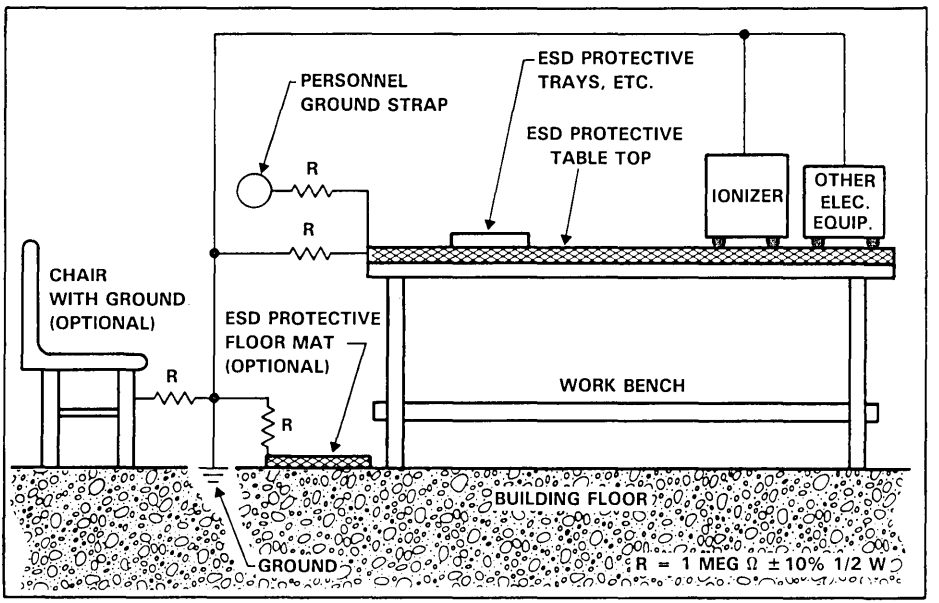
2 Applicable Reference Documents

2.1 The following reference documents of the latest issue in effect can provide additional information on ESD controls.

MIL-M-38510 Microcircuits, General Specification
MIL-STD-883 Test Methods and Procedures for Microelectronics
MIL-S-19491 Semiconductor Devices, Packaging of
MIL-M-55565 Microcircuits, Packaging of
DOD-HDBK-263 Electrostatic Discharge Control Handbook for Protection
DOD-STD-1686 Electrostatic Discharge Control Program
NAVSEA SE 003-11-TRN-010 Electrostatic Discharge Training Manual

3 Facilities for Static-Free Work Station

3.1 The minimum acceptable static-free work station shall consist of the work surface covered with an ESD protective material attached to ground through a 1.0 MΩ ± 10% resistor, an attached grounding wrist strap with integral 1.0 MΩ ± 10% resistor for each operator, and air ionizer(s) of sufficient capacity for each operator. The wrist strap shall be connected to the ESD protective material. Ground shall utilize the standard building earth ground, refer to Figure 1. Conductive floor tile along with conductive shoes may be used in lieu of the conductive wrist straps. The Site Safety Engineer must review and approve all electrical connections at the static-free work station prior to its implementation.



All electrical equipment sitting on the conductive table top must be hard grounded but must be isolated from the conductive table top.
NOTE: Earth ground is not computer ground or RF ground or any other limited type ground.

Figure 1. Static-Free Work Station

3.1.1 Air ionizer: Ionizers shall be positioned so that the devices at the static-free work stations are within a 4-foot arc measured by a vertical line from the face of the ionizer and 45 degrees on each side of this line.

3.2 General Grounding Requirements are to be in Accordance with Table I.

Table I. General Grounding Requirements

	TREATED WITH ANTISTATIC SOLUTION OR MADE OF CONDUCTIVE MATERIAL	GROUND TO COMMON POINT
Handling Equipment/Handtools	X	
Metal Parts of Fixtures & Tools/Storage Racks		X
Handling Trays/Tubes	X	
Soldering Irons/Bath		X
Table Tops/Floor Mats	X	X
Personnel		X Using Wrist Strap*

*With 1.0 MΩ ± 10% Resistor

3.3 Usage of Antistatic Solution in Areas to Control the Generation of Static Charges

3.3.1 The use of antistatic chemicals (antistats) should be a supplemental part of an overall organized ESD program. Any antistatic chemical application shall be considered as a means to reduce or eliminate static charge generation on nonconductive materials in the manufacturing or storage areas.

3.3.2 The application of any antistatic chemical in a clean room of class 10,000 or less shall not be permitted. Accordingly, any user of antistatic solutions must consider the following precautions:

3.3.2.1 Do not apply antistatic spray or solutions in any form to energized electrical parts, assemblies, panels, or equipment.

3.3.2.2 Do not perform antistatic chemical applications in any area when bare chips, raw parts, packages, and/or personnel are exposed to spray mists and evaporation vapors.

3.3.3 The need for initial application and frequency of reapplication can only be established through routine electrostatic voltage measurements using an electrostatic voltmeter. The following durability schedule is a reasonable expectation.

3.3.3.1 Soft surfaces (carpet, fabric seats, foam padding, etc.) each 6 months or after cleaning, by spraying.

3.3.3.2 Hard abused surfaces (floors, table tops, tools, etc.) each week (or day for heavy use) and after cleaning, by wiping or mopping.

3.3.3.3 Hard unabused surfaces (cabinets, walls, fixtures, etc.) each 6 months or annually and after cleaning, by wiping or spraying.

3.3.3.4 Company-furnished and maintained clothing and smocks, after each cleaning, by spraying or adding antistatic concentrate to final rinse water when cleaned.

3.3.4 The use of antistatic chemicals, their application, and compliance with all appropriate specifications, precautions, and requirements shall be the responsibility of the Area Supervisor where antistatic chemicals are used.

3.4 ESD Labels and Signs in Work Areas

3.4.1 ESD caution signs at work stations and labels on static-sensitive parts and containers shall be consistent in color, symbols, class, and voltage sensitivity identification, and appropriate instructions.

3.4.2 Signs shall be posted at all work stations performing any handling operations with static-sensitive items. These signs shall contain the following information.

> **CAUTION**
>
> **STATIC CAN DAMAGE COMPONENTS**
>
> Do not handle ESDS items unless grounding wrist strap is properly worn and grounded. Do not let clothing or plain plastic materials contact or come in close proximity to ESDS items.

3.4.3 Labels shall be affixed to all containers containing static-sensitive items at a place readily visible and proper for the intended purpose. Additionally, labels must be consistently placed on containers and packages at a standard location to eliminate mishandling.

3.4.4 Use only QC accepted and approved signs and labels to identify static-sensitive products and work areas.

3.4.5 The use of ESD signs and labels, and their information content shall be the responsibility of the Area Supervisor to assure consistency and compatibility throughout the static-sensitive routing.

3.5 Relative Humidity Control

3.5.1 Since relative humidity has a significant impact on the generation of static electricity, when possible, the work area should be maintained within the following relative humidity ranges: incoming/assembly/test/storage 50%-65% (ref. Ashrae, 55—74).

3.5.2 Where it is possible to control the relative humidity, it should be set for some value within the above range and maintained at that setting ±5% to avoid static voltage monitor variations.

4 Preparation for Working at Static-Free Work Station

4.1 A work station with a conductive work surface connected to ground through a 1.0 MΩ ± 10% resistor, a grounding wrist strap with the ground wire connected to the conductive

work surface, and an ionizer constitute a static-free work station (Figure 1). An operator is properly grounded when the wrist strap is in snug (no slack) contact with the bare skin, usually positioned on the left wrist for a right-handed operator. The wrist strap must be worn the entire time an operator is at a static-free work station.

4.1.1

> **CAUTION**
>
> Personnel shall never be attached to ground without the presence of the 1.0 MΩ ±10% series resistor in the ground wire.

4.2 Operators should first touch the grounded bench top before handling static-sensitive items. This precaution should be observed in addition to wearing the grounding wrist strap. If possible, operators should avoid touching leads or contacts even though grounded.

4.3 Operator's clothing should never make contact or come in close proximity with static sensitive items. Operators must be especially careful to prevent any static-sensitive items (being handled) from touching their clothing. Long sleeves must be rolled up or covered with antistatic sleeve protector banded to the bare wrist which shall "cage" the sleeve at least as far up as the elbow.

4.4 Only antistatic finger cots may be used when handling static-sensitive items.

4.5 Any person not properly prepared, as outlined in paragraphs 4.2, 4.3, and 4.4 while at or near the work station, shall not touch or come in close proximity with any static-sensitive items.

4.6 It is the responsibility of the operator and the Area Supervisor to ensure that the static-free work area is clear of unnecessary static hazards, including such personal items as plastic coated cups or wrappers, plastic cosmetic bottles or boxes, combs, tissue boxes, cigarette packages, and vinyl or plastic purses. All work-related items, including information sheets, fluid containers, tools, and parts carriers must be those approved for use at the static-free work station.

5 General Handling Procedures and Requirements

5.1 All static-sensitive items must be received in an antistatic/conductive container and must not be removed from the container except at a static-free work station. All protective folders or envelopes holding documentation (lot travelers, etc.) shall be made of nonstatic-generating material.

5.2 Each packing (outermost) container and package (internal or intermediate) shall have a bright yellow warning label attached, stating the following information or equivalent:

The warning label shall be legible and easily readable to normal vision at a distance of 3 feet.

5.3 Static-sensitive items are to remain in their protective containers except when actually in work at the static-free station.

5.4 Before removing the items from their protective container, the operator should:

5.4.1 Place the container on the conductive grounded bench top

5.4.2 Make sure the wrist strap fits snugly around the wrist and is properly plugged into the ground receptacle, then touch hands to the conductive bench top.

5.5 All operations on the items should be performed with the items in contact with the grounded bench top as much as possible. Do not allow conductive magazine to touch hard grounded test gear on bench top.

5.6 Ordinary plastic solder-suckers and other plastic assembly aids shall not be used.

5.7 In cases where it is impossible or impractical to ground the operator with a wrist strap, a conductive shoe strap may be used along with conductive tile/mats.

5.8 When the operator moves from any other place to the static-free station, the start-up procedure shall be the same as in paragraph 4.0.

5.9 The ionizer shall be in operation prior to presenting any static-sensitive items to the static-free station, and shall be in operation during the entire time period the items are at the station.

5.10 "Plastic snow" polystyrene foam, "peanuts," or other high-dielectric materials shall never come in contact with or be used around electrostatic sensitive items, unless they have been treated with an antistat (as evidenced by pink color and generation of less than $\pm$ 100 volts).

5.11 Static-sensitive items shall not be transported or stored in trays, tote boxes, vials, or similar containers made of untreated plastic material unless items are protectively packaged in conductive material.

6 Packaging Requirements

6.1 Packaging of static-sensitive items is to be in accordance with section 1.4.1. Tape and plain plastic bags are prohibited.

6.2 Outer and inner containers are to be marked as outlined in section 5.2.

6.3 Conductive magazines/boxes may be used in lieu of conductive bags.

7 Specific Handling Procedures for Static-Sensitive Items

7.1 Stockroom Operations

7.1.1 Containers of static-sensitive items are not to be accepted into stock unless adequately identified as containing static-sensitive items.

7.1.2 Items may be removed from the protective container (magazine/bag, etc.) for the purpose of subdividing for order issue only by a properly grounded operator at an approved static-free station as defined in sections 3.0 and 4.0.

7.1.3 All subdivided lots must be carefully repackaged in protective containers (magazine/bag, etc.) prior to removal from the static-free work station and labeled to indicate that the package(s) contain static-sensitive items. If it is suspected that a static-sensitive item is not adequately protected, do not transfer it to another container, return it to the originator for disposition unless the originator is a Customer. In that case, the QC Engineer should contact the Customer and negotiate an appropriate disposition.

7.1.4 It is the responsibility of the Stockroom Supervisor to ensure that all personnel assigned to this operation are familiar with handling procedures as outlined in this specification. A copy of this specification is to be posted in the vicinity so that it is accessible to the operators. Stock handlers and all others who might have occasion to move stock are to be instructed to avoid direct contact with unprotected static-sensitive items.

7.2 Module and Subassembly Operations

7.2.1 Static-sensitive items are not to be received from a stockroom, kitting, or machine insertion area unless received in approved static-protective packaging, and properly labeled to indicate that its contents are static sensitive.

7.2.2 All single station, progressive line manual assembly operators, and visual inspectors prior to wave soldering operations are to be properly grounded with a grounding wrist strap when handling static-sensitive items.

7.2.3 Progressive lines used as single stations where operators will be working on a mix of boards, both static-sensitive and nonstatic-sensitive, will require that all operators working on the line be properly grounded. This is necessary to accommodate the sliding of static-sensitive boards along the assembly bench or across positions not engaged in the assembly of this type board.

7.2.4 It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of non compliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding wrist straps properly (snugly in contact with bare skin).

7.3 Soldering and Lead-Forming Operations

7.3.1 All soldering machines, conveyors, cleaning machines, and equipment shall be electrically grounded to ensure that they are at the same ground potential as the grounded operators working on their stations. No machine surfaces exposed to static-sensitive items are to be above the ground potential.

7.3.2 All processing equipment shall be grounded, including all loading and unloading stations, that is, the stations before and after each piece of processing equipment.

7.3.3 All nonmetallic, static-generating components in the handling systems shall be treated to ensure protection from static.

7.3.4 All stations shall be identified by posting signs as outlined in section 3.5.

7.3.5 Operators are to be properly grounded with a grounding wrist strap during any handling, loading, unloading, inspection, rework, or proximity to static-sensitive items.

7.3.6 Unloading operators working at a grounded station shall place static-sensitive items into approved static-protective bags or containers.

7.3.7 All manual soldering, repair, and touch-up work stations on the solder line are to be static protected. Operators are to wear grounding wrist straps when working on static-sensitive items.

7.3.7.1 Only grounded-tip soldering/desoldering irons are allowed when working on static-sensitive items.

7.3.8 It is the responsibility of the Area Spervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding wrist straps properly (comfortably snug in contact with bare skin).

7.4 Electrical Testing Operations

7.4.1 All electrical test stations shall be static protected. Operators shall be properly grounded when working on these items.

7.4.2 Reused antistatic magazines must be monitored for maintenance of antistatic characteristics.

7.4.3 Devices should be in an antistatic/conductive environment except at the moment when actually under test.

7.4.4 Devices should not be inserted into or removed from circuits or tester with the power on or with signals applied to inputs to prevent transient voltages from causing permanent damage.

7.4.5 All unused input leads should be biased if possible.

7.4.6 Device or module repairs must be performed at static-free stations with the operator attached to a grounding wrist strap. Grounded-tip soldering irons shall be used when working on static-sensitive items.

7.4.7 Static-sensitive items shall be handled through all electrical inspections in static protective containers. Removal of the items from the protective containers shall be done at a static-free work station as outlined in section 4.0. The units must be returned to the containers before leaving the station.

7.4.8 All such items shall be shipped with an ESD warning label affixed as outlined in section 5.2.

7.4.9 It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly in contact with bare skin).

7.5 Packing Operations

7.5.1 Static-sensitive items are not to be accepted into the packing area unless they are contained in a static-protected bag or conductive container.

7.5.2 A static-sensitive item delivered to the packer within an approved container or bag and found to be in order regarding identification shall be packed in the standard shipping carton or other regular packaging material. Containers are to be labeled in accordance with section 5.2.

7.5.3 Any void-fillers shall be made of an approved antistatic material.

7.6 Burn-In Operations

7.6.1 Burn-in board loading and unloading of static-sensitive items shall be done at a static-free station.

7.6.2 Shorting clips/shorted connectors shall be installed on the board plug-in tab prior to loading any units into the board sockets. The clip/connector shall be taken off just prior to plugging the board into the oven connector.

The clip/connector shall be installed immediately upon removal of the board from the oven connector.

Installation and removal of the clip/connector shall be done by a properly grounded operator.

7.6.3 All automatic or semiautomatic loading and unloading equipment shall be properly electrically grounded.

7.6.4 It is the responsibility of the Area Supervisor to ensure that all personnel handling static-sensitive items are familiar with this procedure and fully aware of the damage or possible degradation of these units in the event of noncompliance. A periodic inspection should be made using an electrostatic voltmeter to assure that the static-free stations are in proper working order and to ensure that operators are wearing grounding straps properly (snugly in contact with bare skin).

NOTES

NOTES

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