TEXAS INSTRUMENTS

BiCMOS Bus Interface Logic

Data Book

1989

BiCMOS Bus Interface Logic Data Book

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Information contained in this databook supersedes all data for this technology published by TI in the United States of America before July 1989.

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INTRODUCTION

The new BiCMOS bus interface family from Texas Instruments can reduce system power consumption by up to 25% while maintaining enhanced speed and output drive. This family's combination of bipolar and CMOS technologies permits high-speed switching and drive currents of 24- or 64 mA for commercial applications and 20 or 48 mA for military applications, which are necessary for the high-capacitive loads and backplanes found in today's systems:

The BiCMOS family of bus interface products is designated SN54/74BCT, which includes latches, buffers, drivers, and transceivers to provide pin-for-pin compatibility for easy upgrades.

Features and benefits include:

- Advanced bipolar performance—supports 25- to 30-MHz cycle times
- Ability to drive high-capacitive loads:
  24- or 64-mA output drive current (commercial)
  20- or 48-mA output drive current (military)
- Low power consumption—approximately 95% power savings over bipolar devices
- Pin-for-pin compatibility with industry-standard functions

This book provides pertinent technical information on available BCT devices. Additionally, the General Information Section contains an alphanumerical index, functional index, and other useful information.

For more information on Texas Instruments BiCMOS bus interface products, please contact your local TI field sales office or authorized distributor, or call Texas Instruments at 1-800-232-3200.

Contents

† For more information on these devices, contact the factory.

LINE DRIVERS AND BUS TRANSCEIVERS

BUFFERS AND DRIVERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	NUMBER OF BITS	DEVICE TYPE	AVAILABLE
Noninverting Buffers, Drivers	8	'757	▲
		'760	●
Inverting Buffers, Drivers	8	'756	▲

25-Ω DRIVERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	NUMBER OF BITS	DEVICE TYPE	AVAILABLE
Noninverting Buffers, Drivers	8	'25757	▲
		'25760	▲
Inverting Buffers, Drivers	8	'25756	▲

BUFFERS AND DRIVERS WITH 3-STATE OUTPUTS

DESCRIPTION	NUMBER OF BITS	DEVICE TYPE	AVAILABLE
Quad Buffers/ Drivers with Independent Output Controls	4	'125	●
		'126	●
Noninverting Buffers/Drivers	8	'241	●
$\overline{W}$/Symmetrical $\overline{G}$ Inputs		'244	●
		'541	●
Inverting Buffers/Drivers	8	'240	●
		'540	●
Noninverting Buffers/Drivers	10	'2827A	●
		'29827A	●
Inverting Buffers/Drivers	10	'2828A	●
		'29828A	●

25-Ω LINE DRIVERS WITH 3-STATE OUTPUTS

DESCRIPTION	NUMBER OF BITS	TYPE OF LOGIC	DEVICE TYPE	AVAILABLE
Buffers/Drivers	8	True	'25241	▲
$\overline{W}$/Symmetrical $\overline{G}$ Inputs		True	'25244	▲
Buffers/Drivers	8	Inverting	'25240	▲

SPECIAL BUFFERS/DRIVERS

DESCRIPTION	NUMBER OF BITS	TYPE OF LOGIC	DEVICE TYPE	AVAILABLE
Buffers/Drivers with Parity Checker/ Generator	8	Inverting	'455	▲
		True	'456	▲

BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

DESCRIPTION	NUMBER OF BITS	TYPE OF LOGIC	DEVICE TYPE	AVAILABLE
Transceivers	8	True	'245	●
		Inverting	'620A	●
		True	'623	●
		Inverting	'640	●
Bus Transceivers with Registers	8	True	'543	●
		Inverting	'544	▲
		True	'646	●
		Inverting	'648	▲
		Inverting	'651	▲
		True	'652	●
Bus Transceivers with Parity Checker/ Generator	8 to 9	True	'29833	●
		Inverting	'29834	●
		True	'29853	●
		Inverting	'29854	●
Transceivers	9	True	'29863A	●
		Inverting	'29864A	●
	10	True	'29861A	●
		Inverting	'29862A	●
Latch Transceivers	8		'956	▲
			'957	▲
			'958	▲
			'959	▲

BUFFERS AND LINE DRIVERS/MOS MEMORY DRIVERS

DESCRIPTION	NUMBER OF BITS	DEVICE TYPE	AVAILABLE
Bus Drivers (Series Resistors)	8	'2240	●
		'2241	●
		'2244	●
Buffers (Series Resistors)	11	'2410	▲
		'2411	▲

● Denotes available product.

▲ Denotes planned new products. For product availability on these devices, contact the factory.

LINE DRIVERS AND BUS TRANSCEIVERS (Continued)

25-Ω BUS TRANSCEIVERS

DESCRIPTION	NUMBER OF BITS	TYPE OF LOGIC	PORT CONFIGURATION	DEVICE TYPE	AVAILABLE
Bus Transceivers	8	True	3-State; A = 25 Ω Line Drive	'25245	▲
Bus Transceivers	8	Inverting	3-State; A = 25 Ω Line Drive	'25620	▲
		True	B = 3-State; A = 25 Ω Drive, Open-Collector	'25621	▲
		Inverting	B = 3-State; A = 25 Ω Drive, Open-Collector	'25622	▲
		True	3-State; A = 25 Ω Line Drive	'25623	▲
Bus Transceivers	8	Inverting	3-State; A = 25 Ω Line Drive	'25640	▲
		True	B = 3-State; A = 25 Ω Line Drive, Open-Collector	'25641	▲
		Inverting	B = 3-State; A = 25 Ω Line Drive, Open-Collector	'25642	▲

FLIP-FLOPS

FLIP-FLOPS WITH 3-STATE OUTPUTS

DESCRIPTION	NUMBER OF BITS	TYPE OF LOGIC	DEVICE TYPE	AVAILABLE
D-Type, Edge-Triggered	8	True	'374	●
		Inverting	'534	●
		Inverting	'564	▲
		True	'574	▲
D-Type	10	True	'29821	●
		Inverting	'29822	▲

LATCHES AND REGISTERS

LATCHES WITH 3-STATE OUTPUTS

DESCRIPTION	NUMBER OF BITS	TYPE OF LOGIC	DEVICE TYPE	AVAILABLE
Transparent	8	True	'373	▲
			'573	▲
Transparent	8	Inverting	'533	▲
			'564	▲
Transparent	10	True	'29841	▲
		Inverting	'29842	●
	9	True	'29843	●
		Inverting	'29844	●
	8	True	'29845	●
		Inverting	'29846	●

REGISTERS

SHIFT REGISTERS

DESCRIPTION	NUMBER OF BITS	MODES				DEVICE TYPE	AVAILABLE
		S−	S	L	H		
Parallel-In Parallel-Out Bi-Directional	8	X	X	X	X	'299	▲
		X	X	X	X	'323	▲

NOTE: Modes; S− = S-R, S = S-L, L = Load, H = Hold

SIGN-PROTECTED REGISTERS

DESCRIPTION	NUMBER OF BITS	MODES				DEVICE TYPE	AVAILABLE
		S−	S	L	H		
Sign-Protected Registers	8	X		X	X	'322	▲

OTHER REGISTERS

DESCRIPTION	NUMBER OF BITS	DEVICE TYPE	AVAILABLE
Pipeline Register	8	'819	▲
Diagnostic/ Pipeline Register		'29818	▲
Registers	9	'29823	●
		'29824	▲
	8	'29825	▲
		'29826	▲

● Denotes available product.
▲ Denotes planned new products. For product availability on these devices, contact the factory.

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

C_i Input capacitance

The internal capacitance at an input of the device.

C_o Output capacitance

The internal capacitance at an output of the device.

C_{pd} Power dissipation capacitance

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$.

f_{max} Maximum clock frequency

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} Supply current

The current into* the V_{CC} supply terminal of an integrated circuit.

I_{IH} High-level input current

The current into* an input when a high-level voltage is applied to that input.

I_{IL} Low-level input current

The current into* an input when a low-level voltage is applied to that input.

I_{OH} High-level output current

The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} Low-level output current

The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OZ} Off-state (high-impedance-state) output current (of a three-state output)

The current flowing into* an output having three-state capability with input conditions established that, according to the production specification, will establish the high-impedance state at the output.

t_a Access time

The time interval between the application of a specified input pulse and the availability of valid signals at an output.

*Current out of a terminal is given as a negative value.

t_{dis} Disable time (of a three-state or open-collector output)

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ}. Open-collector outputs will change only if they are low at the time of disabling so $t_{dis} = t_{PLH}$.

t_{en} Enable time (of a three-state or open-collector output)

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: In the case of memories, this is the access time from an enable input (e.g., $\overline{G}$). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL}. Open-collector outputs will change only if they are responding to data that would cause the output to go low so, for them, $t_{en} = t_{PHL}$.

t_h Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} Propagation delay time

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. ($t_{pd} = t_{PHL}$ or t_{PLH}).

t_{PHL} Propagation delay time, high-to-low level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} Disable time (of a three-state output) from high level

The time interval between the specified reference points on the input and the output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{PLH} Propagation delay time, low-to-high-level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} Disable time (of a three-state output) from low level

The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} Enable time (of a three-state output) to high level

The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} Enable time (of a three-state output) to low level)

The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_{su} Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w Pulse duration (width)

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

V_{IH} High-level input voltage

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Low-level input voltage

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} High-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.

V_{OL} Low-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state-output
a..h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎏	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎏, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is not at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

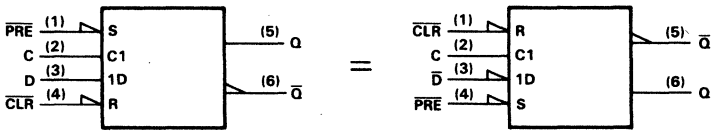
The truth table functional tests do not reflect all possible combinations or sequential modes.

D flip-flop and latch signal conventions

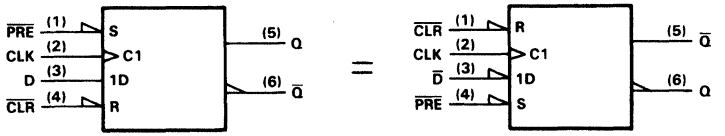
It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset (PRE). An input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active-low.

The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits $\overline{D}$ and Q.

In some applications, it may be advantageous to redesignate the data input from D to $\overline{D}$ or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown in parenthesis.



LATCH LATCH



FLIP-FLOP FLIP-FLOP

The figures show that when Q and $\overline{Q}$ exchange names, the Preset and Clear pins also exchange names. The polarity indicators ▷ on $\overline{PRE}$ and $\overline{CLR}$ remain, as these inputs are still active-low, but the presence or absence of the polarity indicator changes at D (or $\overline{D}$), Q, and $\overline{Q}$. Pin 5 (Q or $\overline{Q}$) is still in phase with the data input (D or $\overline{D}$); their active levels change together.

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In digital system design, consideration must be given to thermal management of components. The small size of the "small outline" package makes this even more critical. Figure 1 shows the thermal resistance of these packages for various rates of air flow.

The thermal resistances in Figure 1 can be used to approximate typical and maximum virtual junction temperatures for the BiCMOS family. In general, the junction temperature for any device can be calculated using Equation 1.

Typical junction temperature can be calculated using Equation 1 directly with typical values of I_{CC} taken from the data sheets and V_{CC} = 5 volts. To calculate maximum junction temperature, it is necessary to take into account the spread of I_{CC} values for a population.

Maximum junction temperature for all 54BCT parts can be calculated using Equation 1 with I_{CC} being the maximum value specified on the data sheet and V_{CC} = 5.5 volts. In fact, I_{CC} for Series 54 devices at the temperature extremes of −55°C to 125°C will be higher than for a Series 74 device at the temperature extremes of 0°C to 70°C. This is reflected in the limits specified for 74BCT devices, which are less than those specified for 54BCTdevices. The BCT family data sheets give a single maximum value for I_{CC}. If that value is used to calculate maximum junction temperature for series 74 devices, an unrealistically high value will result. Instead, Equation 2 can be used. This uses the factor 1.31 to scale the typical value of I_{CC} up to a practical maximum value for process variations and thermal effects.

JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
AIR VELOCITY

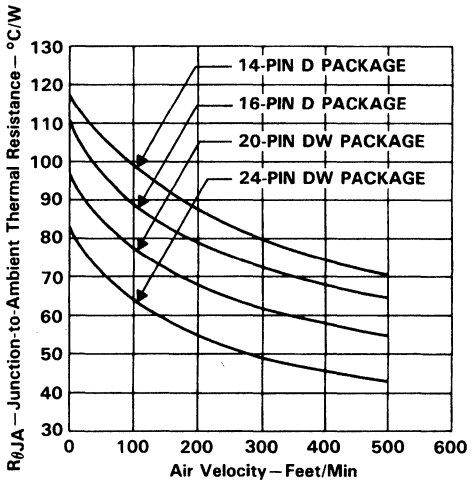


FIGURE 1

$$T_J = R_{\theta JA}(V_{CC} \bullet I_{CC} + N \bullet I_{OL} \bullet V_{OL}) + T_A \quad (1)$$

where

T_J = virtual junction temperature
$R_{\theta JA}$ = thermal resistance, junction to ambient air
V_{CC} = supply voltage (5 V for typical, 5.5 V for maximum)
I_{CC} = supply current
N = the number of outputs
I_{OL} = the low-level output current
V_{OL} = the low-level output voltage
T_A = the ambient air temperature

$$T_{Jmax} = R_{\theta JA}(5.5 \bullet 1.31 \bullet I_{CCtyp} + N \bullet I_{OL} \bullet V_{OL}) + T_A \quad (2)$$

Contents

BiCMOS Circuits
Released Products

TEXAS INSTRUMENTS

QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

D3133, SEPTEMBER 1988 REVISED MAY 1989

- **State of the Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C Method 3015**
- **Package Options Include Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These bus buffers feature independent line drivers with three-state outputs. Each 'BCT125 output is disabled when the associated $\overline{G}$ is high, and each 'BCT126 output is disabled when the associated G is low.

The SN54BCT125 and SN54BCT126 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT125 and SN74BCT126 are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

'BCT125
(EACH BUFFER)

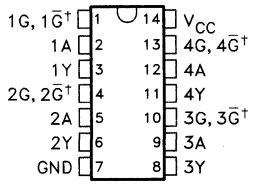
INPUTS		OUTPUT
$\overline{G}$	A	Y
L	H	H
L	L	L
H	X	Z

'BCT126
(EACH BUFFER)

INPUTS		OUTPUT
G	A	Y
H	H	H
H	L	L
L	X	Z

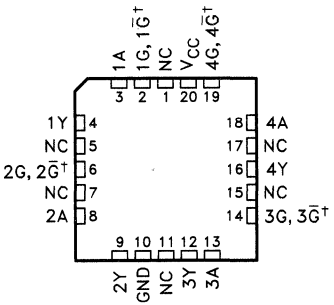
H = high level, L = low level, X = irrelevant

SN54BCT125, SN54BCT126 ... J PACKAGE
SN74BCT125, SN74BCT126 ... N PACKAGE
(TOP VIEW)



† $\overline{G}$ on 'BCT125; G on 'BCT126

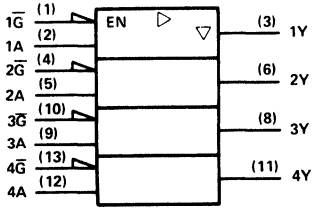
SN54BCT125, SN54BCT126 ... FK PACKAGE
(TOP VIEW)



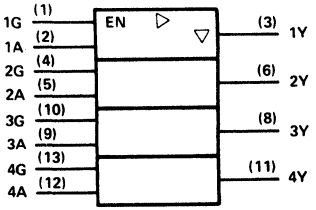
† $\overline{G}$ on 'BCT125; G on 'BCT126
NC—No internal connection

logic symbols‡

'BCT125

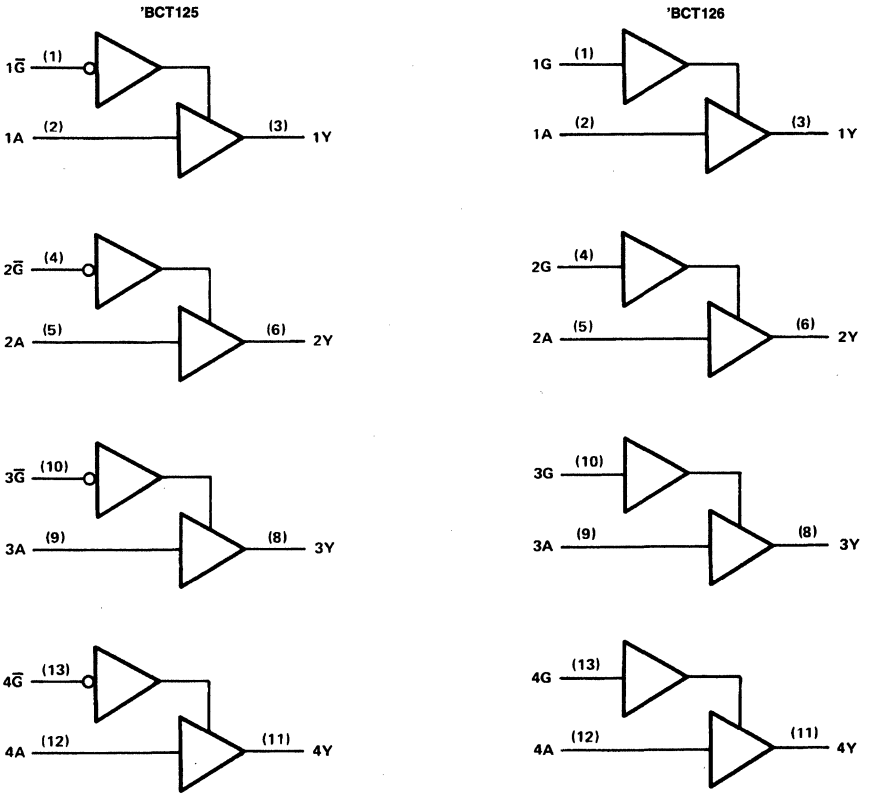


'BCT126



‡ These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages.

logic diagrams (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage (see Note 1) ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state: SN54BCT125, SN54BCT126 ..... 96 mA
SN74BCT125, SN74BCT126 ..... 128 mA
Operating free-air temperature range: SN54BCT125, SN54BCT126 ..... −55°C to 125°C
SN74BCT125, SN74BCT126 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN54BCT125 SN54BCT126			SN74BCT125 SN74BCT126			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT125			SN74BCT125			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = −12 mA	2	3.2					
		I_{OH} = −15 mA				2	3.1		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
		I_{OL} = 64 mA					0.42	0.55	
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			35			25	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−20			−20	μA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open		19	31		19	31	mA
I_{CCL}				46	49		46	49	
I_{CCZ}				6	12		6	12	
C_i	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		4			4		pF
C_o	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V		9			9		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT126			SN74BCT126			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = −12 mA	2	3.2					
		I_{OH} = −15 mA				2	3.1		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
		I_{OL} = 64 mA					0.42	0.55	
I_I	V_{CC} = 0 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			35			25	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−20			−20	μA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open		21	33		21	33	mA
I_{CCL}				35	51		35	51	
I_{CCZ}				5	8		5	8	
C_i	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		4			4		pF
C_o	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V		9			9		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

'BCT125 switching characteristics (see Figure 1)

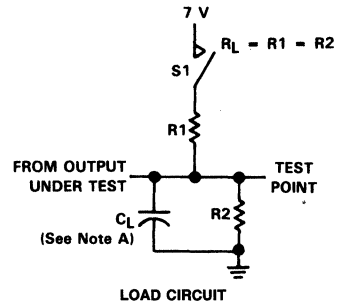
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT125			SN54BCT125		SN74BCT125		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.6	3.5	5.2	1.6	6	1.6	5.7	ns
t_{PHL}			2.7	5	6.9	2.7	8	2.7	7.7	
t_{PZH}	$\overline{G}$	Y	3.4	6.7	9	3.4	11.1	3.4	10.3	ns
t_{PZL}			5	8.2	10.4	5	12.8	5	11.7	
t_{PHZ}	$\overline{G}$	Y	3	5.8	7.4	3	9.4	3	8.9	ns
t_{PLZ}			2.8	5.5	7.3	2.8	9.9	2.8	8.6	

'BCT126 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT126			SN54BCT126		SN74BCT126		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	3.6	4.9	1.5	5.6	1.5	5.4	ns
t_{PHL}			2.7	5.3	6.9	2.7	7.7	2.7	7.4	
t_{PZH}	G	Y	2.6	4.8	6.4	2.6	7.2	2.6	7	ns
t_{PZL}			3.7	6.4	8.3	3.7	10.5	3.7	10	
t_{PHZ}	G	Y	3.2	6.6	8.2	3.2	9.6	3.2	9.1	ns
t_{PLZ}			3.4	6.5	8	3.4	12.3	3.4	10.7	

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

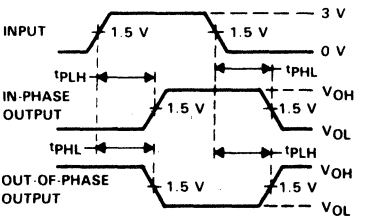
PARAMETER MEASUREMENT INFORMATION



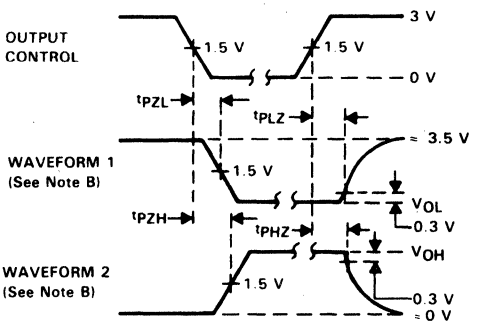
LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≥ 10 MHz, Z_O = 50 Ω, t_r = 2.5 ns, t_f = 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
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D3057, OCTOBER 1987—REVISED OCTOBER 1988

- **State of the Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **Comparable Speed and Improved Power Performance Relative to 54F/74F240**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

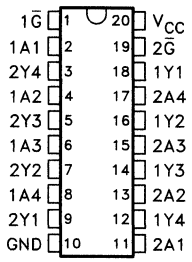
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT241 and 'BCT244, these devices provide a choice of selected combinations of inverting and non-inverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out and improved fan-in.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

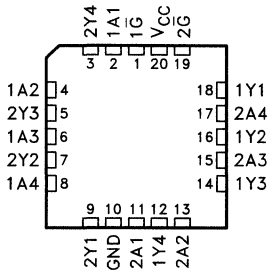
FUNCTION TABLE
(EACH BUFFER)

INPUTS		OUTPUT
$\overline{G}$	A	Y
L	H	L
L	L	H
H	X	Z

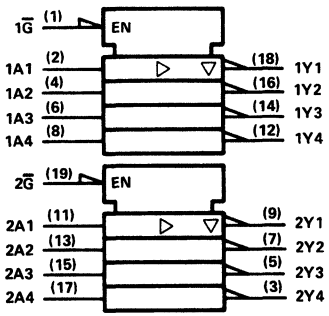
SN54BCT240 ... J PACKAGE
SN74BCT240 ... DW OR N PACKAGE
(TOP VIEW)



SN54BCT240 ... FK PACKAGE
(TOP VIEW)

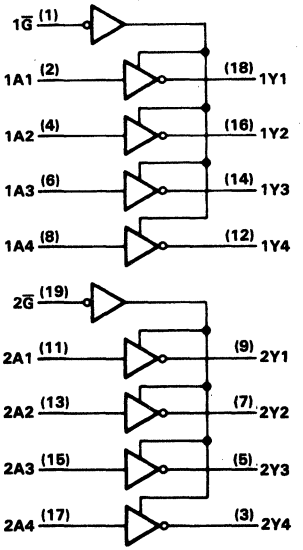


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage (see Note 1) ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Input clamp current ..... −30 mA
Current into any output in the low state: SN54BCT240 ..... 96 mA
SN74BCT240 ..... 128 mA
Operating free-air temperature range: SN54BCT240 ..... −55°C to 125°C
SN74BCT240 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN54BCT240			SN74BCT240			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

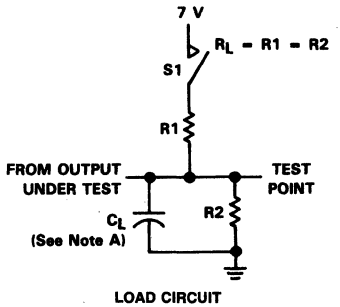
PARAMETER	TEST CONDITIONS		SN54BCT240			SN74BCT240			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = −12 mA	2	3.2					
		I_{OH} = −15 mA				2	3.1		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
		I_{OL} = 64 mA					0.42	0.55	
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−1			−1	mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open		19	31		19	31	mA
I_{CCL}				46	71		46	71	
I_{CCZ}				6	9		6	9	
C_i	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		6			6		pF
C_o	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V		11			11		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'BCT240			SN54BCT240		SN74BCT240		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	0.5	3.3	4.8	0.5	6.4	0.5	5.6	ns
t_{PHL}			0.4	1.8	3.5	0.4	4.5	0.4	4	
t_{PZH}	$\overline{G}$	Y	1	6.4	7.9	1	9.2	1	8.8	ns
t_{PZL}			1	7.5	9.4	1	10.8	1	10.5	
t_{PHZ}	$\overline{G}$	Y	1	6	6.8	1	8.5	1	8.1	ns
t_{PLZ}			1	6.7	8.1	1	10.6	1	9.5	

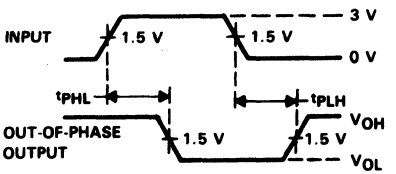
PARAMETER MEASUREMENT INFORMATION



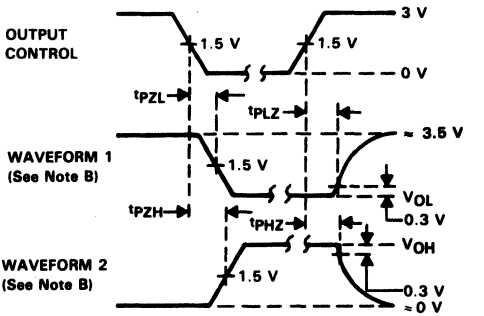
LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 2.5 ns, t_f = 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

D3057, OCTOBER 1987—REVISED OCTOBER 1988

- **State of the Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **Comparable Speed and Improved Power Performance Relative to '54F/74F241**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
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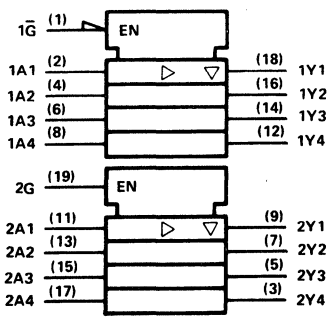
- **Dependable Texas Instruments Quality and Reliability**

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT240 and 'BCT244, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs.

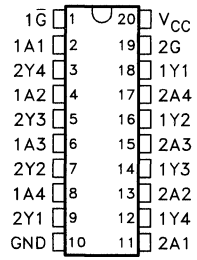
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

logic symbol†

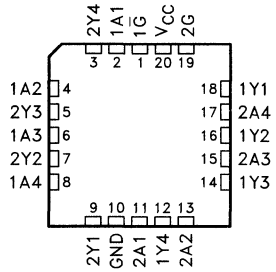


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54BCT241 ... J PACKAGE
SN74BCT241 ... DW OR N PACKAGE
(TOP VIEW)



SN54BCT241 ... FK PACKAGE
(TOP VIEW)



FUNCTION TABLES

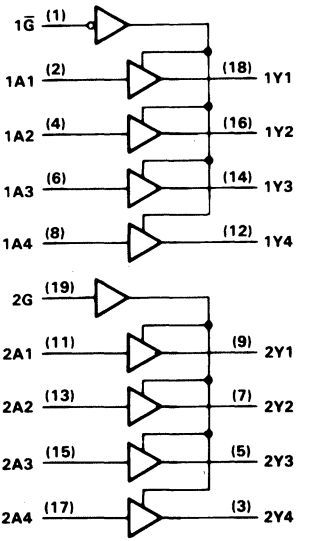
(EACH BUFFER IN FIRST SET)

INPUTS		OUTPUT
1G̅	1A	1Y
L	H	H
L	L	L
H	X	Z

(EACH BUFFER IN SECOND SET)

INPUTS		OUTPUT
2G	2A	2Y
H	H	H
H	L	L
L	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage (see Note 1) ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Input clamp current ..... −30 mA
Current into any output in the low state: SN54BCT241 ..... 96 mA
SN74BCT241 ..... 128 mA
Operating free-air temperature range: SN54BCT241 ..... −55°C to 125°C
SN74BCT241 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN54BCT241			SN74BCT241			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT241			SN74BCT241			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
			I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
			I_{OL} = 64 mA					0.42	0.55	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	1$\overline{G}$ or 2G	V_{CC} = 5.5 V, V_I = 0.5 V				−1			−1	mA
	Any A Input	V_{CC} = 5.5 V, V_I = 0.5 V				−1.6			−1.6	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CCH}		V_{CC} = 5.5 V, Outputs open	Outputs high		23	43		23	43	mA
I_{CCL}			Outputs low		53	85		53	85	mA
I_{CCZ}			Outputs disabled		4	10		4	10	mA
C_i		V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			6			6		pF
C_o		V_{CC} = 5 V, V_O = 2.5 V or 0.5 V			11			11		pF

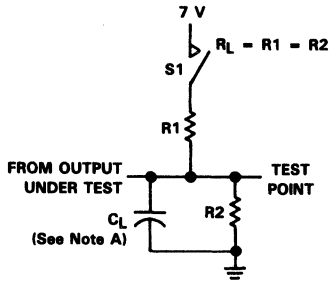
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX§				UNIT
			'BCT241			SN54BCT241		SN74BCT241		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	0.5	2.5	4.5	0.5	5.2	0.5	4.9	ns
t_{PHL}			1	3	5.4	1	6.3	1	5.9	
t_{PZH}	G or $\overline{G}$	Y	1	5.7	7.8	1	9.1	1	8.7	ns
t_{PZL}			1	5.2	8.6	1	10	1	9.4	
t_{PHZ}	G or $\overline{G}$	Y	1	5.8	6.8	1	8.4	1	8.1	ns
t_{PLZ}			1	7	8.1	1	11	1	9.9	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

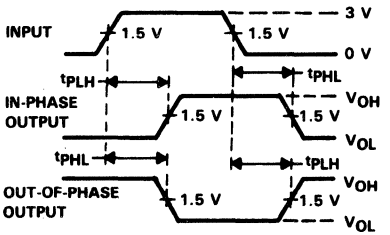
PARAMETER MEASUREMENT INFORMATION



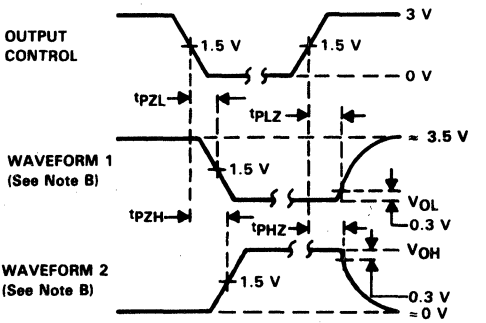
LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All Input pulses are supplied by the generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

D3057, OCTOBER 1987—REVISED OCTOBER 1988

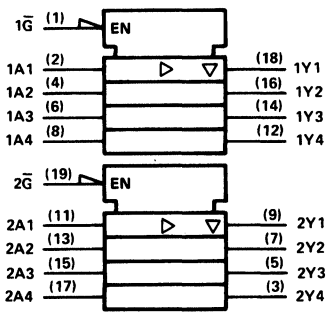
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce DC Loading**
- **State of the Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **Comparable Speed and Improved Power Performance Relative to 54F/74F244**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015**
- **Package Options Include "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT240 and 'BCT241, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs.

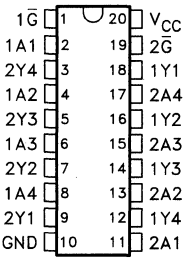
The SN54BCT244 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT244 is characterized for operation from 0°C to 70°C.

logic symbol†

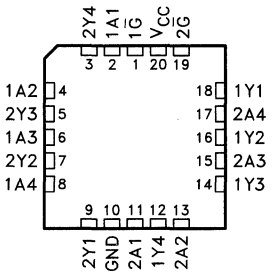


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54BCT244 ... J PACKAGE
SN74BCT244 ... DW OR N PACKAGE
(TOP VIEW)



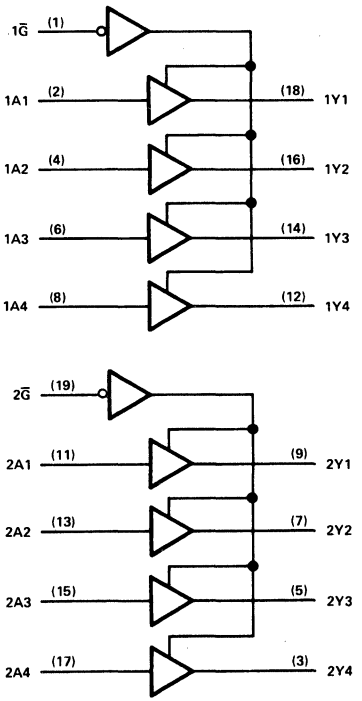
SN54BCT244 ... JK PACKAGE
(TOP VIEW)



FUNCTION TABLE

OUTPUT CONTROL	DATA INPUT	OUTPUT
$1\overline{G}$, $2\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state: SN54BCT244 ..... 96 mA
SN74BCT244 ..... 128 mA
Operating free-air temperature range: SN54BCT244 ..... −55°C to 125°C
SN74BCT244 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54BCT244			SN74BCT244			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT244			SN74BCT244			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = −12 mA	2	3.2					
		I_{OH} = −15 mA				2	3.1		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
		I_{OL} = 64 mA					0.42	0.55	
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−1			−1	mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CCH}	V_{CC} = 5.5 V	Outputs high		23	40		23	40	mA
I_{CCL}		Outputs low		53	80		53	80	mA
I_{CCZ}		Outputs disabled		4	10		4	10	mA

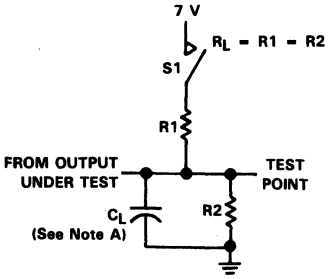
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX§				UNIT
			'BCT244			SN54BCT244		SN74BCT244		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.2	2.5	4.4	0.9	5.3	0.7	5	ns
t_{PHL}			1.7	3.2	5	1.4	6	1.4	5.5	
t_{PZH}	$\overline{G}$	Y	2	5.7	7.8	2	9	2	8.7	ns
t_{PZL}			2	5.9	8.1	2	9.4	2	8.9	
t_{PHZ}	$\overline{G}$	Y	2	5.4	6.7	2	8	2	7.7	ns
t_{PLZ}			2	6.1	7.6	2	9.8	2	8.9	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

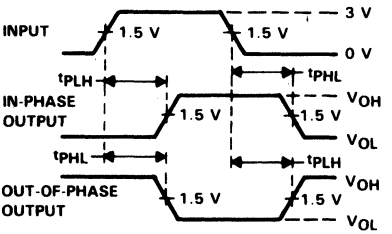
PARAMETER MEASUREMENT INFORMATION



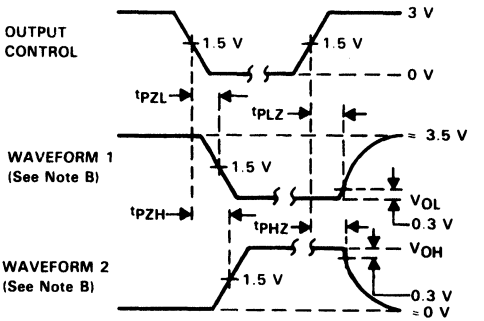
LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

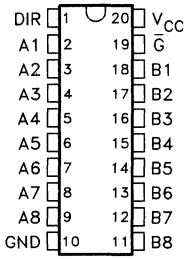
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All Input pulses are supplied by the generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

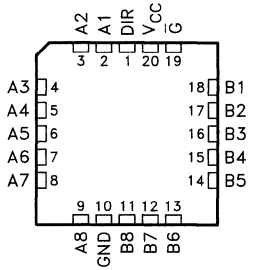
D3057, SEPTEMBER 1988—REVISED APRIL 1989

- **BiCMOS Design Substantially Reduces Standby Current**
- **3-State Outputs Drive Bus Lines Directly**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C Method 3015**
- **Comparable Speed and Improved Power Performance Relative to SN54F245, SN74F245**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54BCT245 ... J PACKAGE
SN74BCT245 ... DW OR N PACKAGE
(TOP VIEW)



SN54BCT245 ... FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. Implementing the control function minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can disable the device so that the buses are effectively isolated.

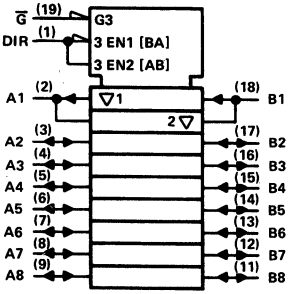
The SN54BCT245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT245 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

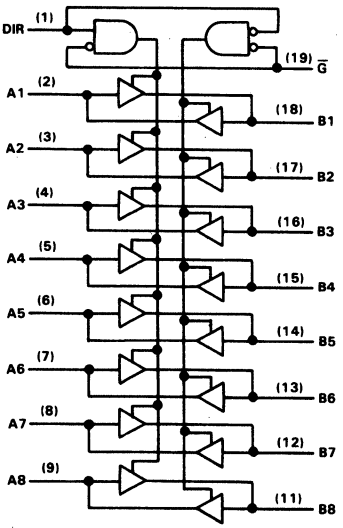
2 BiCMOS Circuits

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage (see Note 1) ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state: SN54BCT245 ..... 96 mA
SN74BCT245 ..... 128 mA
Operating free-air temperature range: SN54BCT245 ..... −55°C to 125°C
SN74BCT245 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			SN54BCT245			SN74BCT245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	A1–A8			−3			−3	mA
		B1–B8			−12			−15	mA
I_{OL}	Low-level output current	A1–A8			20			24	mA
		B1–B8			48			64	mA
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5.5 V (unless otherwise noted)

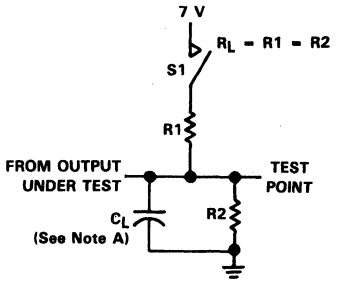
PARAMETER		TEST CONDITIONS		SN54BCT245			SN74BCT245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_{IK} = −18 mA			−1.2			−1.2	V
V_{OH}	Any A	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
			I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	Any B		I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
			I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
V_{OL}	Any A	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
	Any B		I_{OL} = 48 mA		0.38	0.55				
			I_{OL} = 64 mA					0.42	0.55	
I_I‡	A and B	V_{CC} = 5.5 V	V_I = 5.5 V			1			1	mA
	DIR and $\overline{G}$	V_{CC} = 5.5 V	V_I = 5.5 V			0.1			0.1	
I_{IH}‡	A and B	V_{CC} = 5.5 V,	V_I = 2.7 V			70			70	μA
	DIR and $\overline{G}$					20			20	
I_{IL}	A and B	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.65			−0.65	mA
	DIR and $\overline{G}$					−1.2			−1.2	
I_{OS}§	Any A	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
	Any B			−100		−225	−100		−225	
I_{CCH}		V_{CC} = 5.5 V,	See Note 2		36	57		36	57	mA
I_{CCL}		V_{CC} = 5.5 V,	See Note 2		57	90		57	90	
I_{CCZ}		V_{CC} = 5.5 V			10	15		10	15	
C_{in}	$\overline{G}$ and DIR	V_{CC} = 5.5 V,	V_I = 2.5 V or 0.5 V		7			7		pF
C_{IO}	A to B				9			9		
C_{IO}	B to A				12			12		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: I_{CCH} and I_{CCL} are measured in the A to B mode.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'BCT245			SN54BCT245		SN74BCT245		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	4.4	6	1	7.2	1	7	ns
t_{PHL}			1.5	4.8	6.6	1.5	7.6	1.5	7	
t_{PZH}	$\overline{G}$	A or B	1.5	8	9.4	1.5	11.2	1.5	10.9	ns
t_{PZL}			1.5	8	10.2	1.5	11.8	1.5	11.6	
t_{PHZ}	$\overline{G}$	A or B	1.5	5.8	8.3	1.5	9.7	1.5	9.3	ns
t_{PLZ}			1.5	5.1	7.8	1.5	9.6	1.5	9.1	

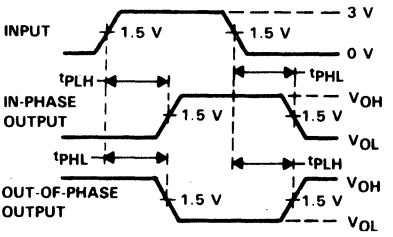
PARAMETER MEASUREMENT INFORMATION



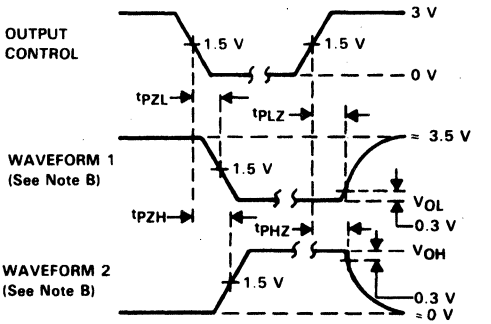
LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



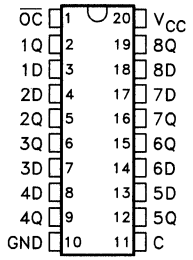
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All Input pulses are supplied by the generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

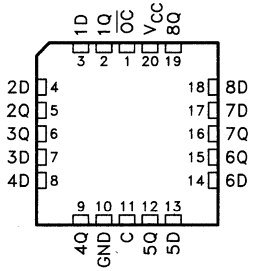
FIGURE 1. SWITCHING CHARACTERISTICS

- **8-Latches in a Single Package**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **State of the Art BiCMOS Design Significantly Reduces I_{CC}**
- **Comparable Speed and Improved Power Performance Relative to 54F/74F373**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C, Method 3015**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic Ceramic 300-mil DIPs**

SN54BCT373 ... J PACKAGE
SN74BCT373 ... DW OR N PACKAGE
(TOP VIEW)



SN54BCT373 ... FK PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'BCT373 are transparent D-type latches. While the enable (C) is high, the Q outputs will follow the data (D) inputs. When the enable is taken low, the Q outputs will be latched at the levels that were set up at the D inputs.

A buffered output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface components.

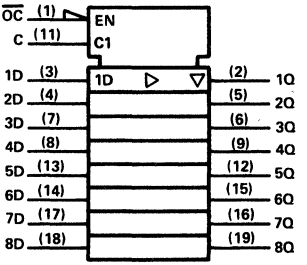
The output control ($\overline{OC}$) does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54BCT373 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT373 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each latch)

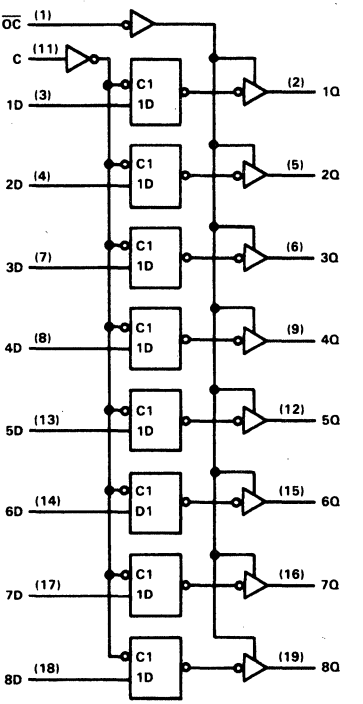
INPUTS			OUTPUT
$\overline{OC}$	ENABLE C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage (see Note 1) ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 7 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Input clamp current ..... −30 mA
Current into any output in the low state: SN54BCT373 ..... 96 mA
SN74BCT373 ..... 128 mA
Operating free-air temperature range: SN54BCT373 ..... −55°C to 125°C
SN74BCT373 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input negative-voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN54BCT373			SN74BCT373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT373			SN74BCT373			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = −12 mA	2	3.2					
		I_{OH} = −15 mA				2	3.1		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
		I_{OL} = 64 mA					0.42	0.55	
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50			50	μA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50			−50	μA
I_I	V_{CC} = 5.5 V, V_I = 5.5 V				0.4			0.4	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V				−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0		−100		−225	−100		−225	mA
I_{CCL}	V_{CC} = 5.5 V			37	60		37	60	mA
I_{CCH}	V_{CC} = 5.5 V			2	5		2	5	mA
I_{CCZ}	V_{CC} = 5.5V			5	8		5	8	mA
C_i	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			6			6		pF
C_o	V_{CC} = 5 V, V_O = 2.5 V or 0.5 V			11			11		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

timing requirements

		V_{CC} = 5V, T_A = 25°C		V = 4.5 V to 5.5 V, T_A = MIN to MAX§				UNIT
		'BCT373		SN54BCT373		SN74BCT373		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su}	Setup time, Data before enable C ↓	2		2		2		ns
t_h	Hold time, Data after enable C ↓	5.5		5.5		5.5		ns
t_w	Pulse duration, Enable C high	7.5		7.5		7.5		ns

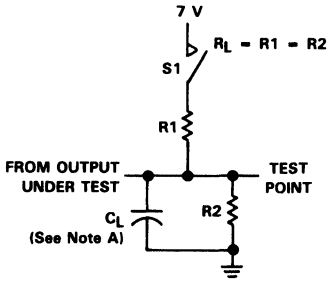
§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT373			SN54BCT373		SN74BCT373		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Any Q	2	5.9	7.7	1.5	10.1	2	9.3	ns
t_{PHL}	D	Any Q	2	6.7	8.5	1	10.3	1.5	9.5	ns
t_{PLH}	C	Any Q	2	6.2	8.2	2	10.1	2	9.3	ns
t_{PHL}	C	Any Q	2	5.9	7.8	2	9.2	2	8.8	ns
t_{PZH}	$\overline{OC}$	Any Q	1	7.8	9.6	1	12.3	1	11.8	ns
t_{PZL}	$\overline{OC}$	Any Q	1	8.2	10.2	1	12.5	1	12	ns
t_{PHZ}	$\overline{OC}$	Any Q	1	4.9	6.6	1	7.4	1	7	ns
t_{PLZ}	$\overline{OC}$	Any Q	1	5	6.7	1	8.1	1	7.4	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

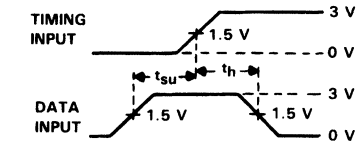
PARAMETER MEASUREMENT INFORMATION



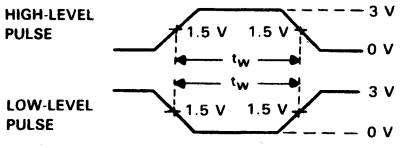
LOAD CIRCUIT 1 ALL OUTPUTS EXCEPT FOR ERROR FLAG

SWITCH POSITION TABLE

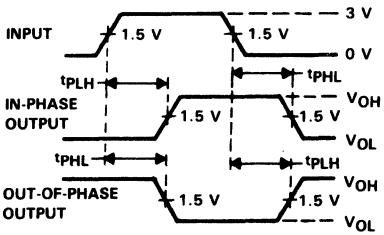
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



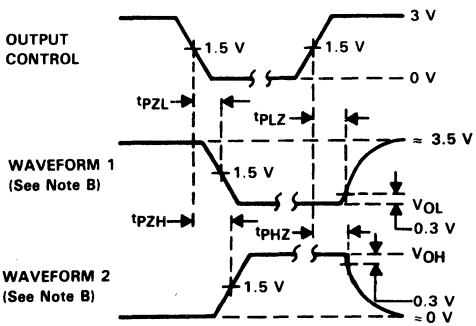
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 2.5 ns, t_f = 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

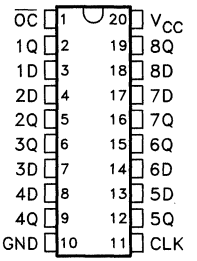
FIGURE 1. SWITCHING CHARACTERISTICS

SN54BCT374, SN74BCT374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

D3130, SEPTEMBER 1988—REVISED DECEMBER 1988

- **8 D-Type Flip-Flops in a Single Package**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **State of the Art BiCMOS Design Significantly Reduces I_{CC}**
- **Comparable Speed and Improved Power Performance Relative to 54F/74F374**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C Method 3015**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 3000-mil DIPs**

SN54BCT374 ... J PACKAGE
SN74BCT374 ... DW OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_O
L	H	X	Q_O
L	↓	X	X_O
H	X	X	Z

description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

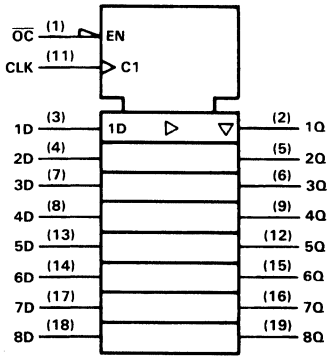
The eight flip-flops of the 'BCT374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic levels that were set up at the D inputs.

A buffered output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ($\overline{OC}$) does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

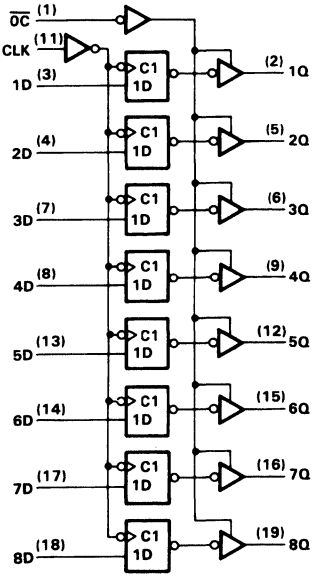
The SN54BCT374 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT374 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, or N packages.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage (see Note 1) ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Input clamp current ..... −30 mA
Current into any output in the low state: SN54BCT374 ..... 96 mA
SN74BCT374 ..... 128 mA
Operating free-air temperature range: SN54BCT374 ..... −55°C to 125°C
SN74BCT374 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN54BCT374			SN74BCT374			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT374			SN74BCT374			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = −12 mA	2	3.2					
		I_{OH} = −15 mA				2	3.1		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
		I_{OL} = 64 mA					0.42	0.55	
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50			50	μA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50			−50	μA
I_I	V_{CC} = 5.5 V, V_I = 5.5 V				0.4			0.4	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V				−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0		−100		−225	−100		−225	mA
I_{CCL}	V_{CC} = 5.5 V			37	60		37	60	mA
I_{CCH}	V_{CC} = 5.5 V			2	5		2	5	mA
I_{CCZ}	V_{CC} = 5.5 V			5	8		5	8	mA
C_i	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			6			6		pF
C_o	V_{CC} = 5 V, V_O = 2.5 V or 0.5 V			10			10		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

timing requirements

		V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX§				UNIT
		'BCT374		SN54BCT374		SN74BCT374		
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		70		70		70	MHz
t_{su}	Setup time, Data before CLK ↑	6.5		6.5		6.5		ns
t_h	Hold time, Data before CLK ↑	0		0		0		ns
t_w	Pulse duration, CLK high	7		8		7		ns

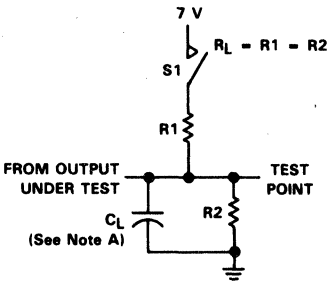
§ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT374			SN54BCT374		SN74BCT374		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			70			70		70		MHz
t_{PLH}	CLK	Q	2	7.2	9.1	2	11.6	2	10.6	ns
t_{PHL}			2	7.1	8.8	2	10.6	2	10	
t_{PZH}	$\overline{OC}$	Q	1	8.3	10.1	1	12.7	1	12.3	ns
t_{PZL}			1	8.6	10.6	1	13	1	12.7	
t_{PHZ}	$\overline{OC}$	Q	1	4.7	6.3	1	7.1	1	6.8	ns
t_{PLZ}			1	4.8	6.3	1	7.5	1	6.8	

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

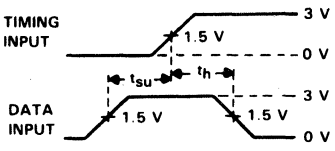
PARAMETER MEASUREMENT INFORMATION



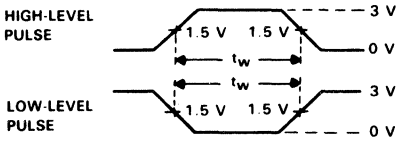
LOAD CIRCUIT

SWITCH POSITION TABLE

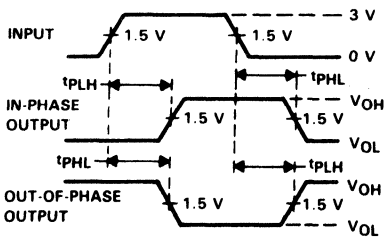
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



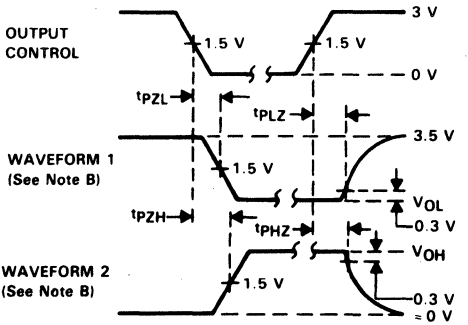
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

- **State of the Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce D-C Loading**
- **Data Flow-Through Pinout (All Inputs on Opposite Side from Outputs)**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These octal buffers and line drivers are designed to have the performance of the popular SN54BCT240/SN74BCT240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR gate so that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

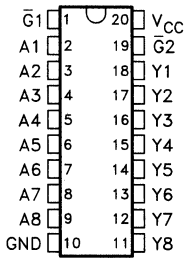
The SN54BCT540 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT540 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

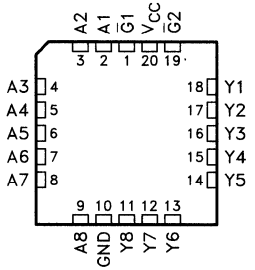
INPUTS			OUTPUT
$\overline{G}1$	$\overline{G}2$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

Z = High Impedance

SN54BCT540 ... J PACKAGE
SN74BCT540 ... DW OR N PACKAGE
(TOP VIEW)

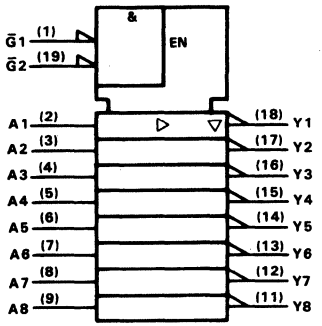


SN54BCT540 ... FK PACKAGE
(TOP VIEW)



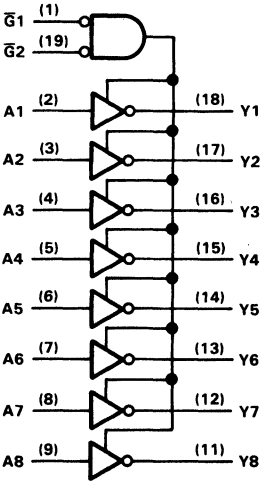
2 BiCMOS Circuits

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state: SN54BCT540 ..... 96 mA
SN74BCT540 ..... 128 mA
Operating free-air temperature range: SN54BCT540 ..... −55°C to 125°C
SN74BCT540 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54BCT540			SN74BCT540			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54BCT540			SN74BCT540			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = −12 mA	2	3.2					
		I_{OH} = −15 mA				2	3.1		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
		I_{OL} = 64 mA					0.42	0.55	
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50			50	μA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50			−50	μA
I_I	V_{CC} = 5.5 V, V_I = 5.5 V				0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V				−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V, V_O = 0		−100		−225	−100		−225	mA
I_{CCL}	V_{CC} = 5.5 V			45	71		45	71	mA
I_{CCH}	V_{CC} = 5.5 V			20	30		20	30	mA
I_{CCZ}	V_{CC} = 5.5 V			3	6		3	6	mA
C_i	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			6			5		pF
C_o	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			10			10		

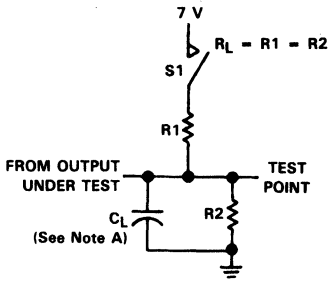
† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT540			SN54BCT540		SN74BCT540		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2.5	4.1	5.8	1.9	7.2	2	6.9	ns
t_{PHL}	A	Y	0.6	1.9	3.5	0.3	4.5	0.3	4	ns
t_{PZH}	$\overline{G}$	Y	4.8	6.8	8.9	4.1	10.4	4.1	10.1	ns
t_{PZL}	$\overline{G}$	Y	6	8	10	5.3	11.8	5.3	11.3	ns
t_{PHZ}	$\overline{G}$	Y	3.5	5.7	7.8	2.7	9.4	2.7	9	ns
t_{PLZ}	$\overline{G}$	Y	3.8	5.5	7.4	3.5	8.9	3.5	8.5	ns

† For conditions specified as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

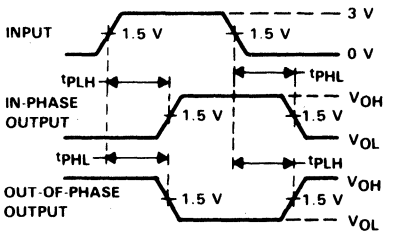
PARAMETER MEASUREMENT INFORMATION



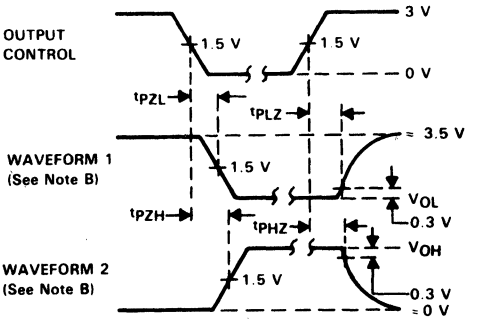
LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by the generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1. SWITCHING CHARACTERISTICS

- **State of the Art BiCMOS Design Significantly Reduces I_{CCZ}**
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- **P-N-P Inputs Reduce D-C Loading**
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- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These octal buffers and line drivers are designed to have the performance of the popular SN54BCT240/SN74BCT240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR gate so that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

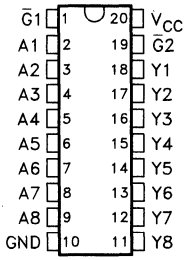
The SN54BCT541 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT541 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

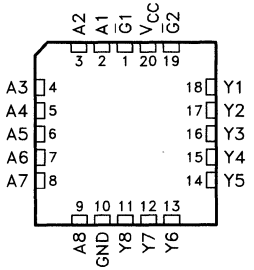
INPUTS			OUTPUT
$\overline{G}1$	$\overline{G}2$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Z = High Impedance

SN54BCT541 ... J PACKAGE
SN74BCT541 ... DW OR N PACKAGE
(TOP VIEW)



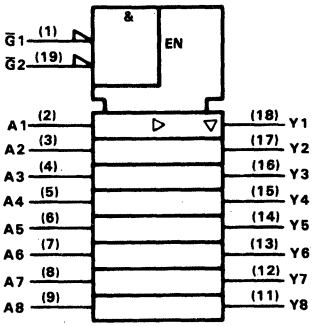
SN54BCT541 ... FK PACKAGE
(TOP VIEW)



2

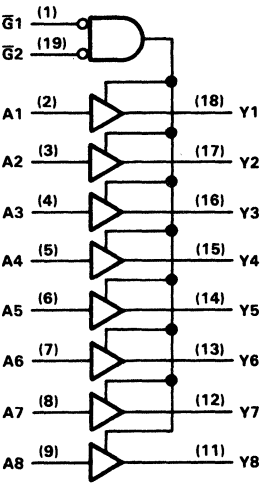
BiCMOS Circuits

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage (see Note 1) ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state: SN54BCT541 ..... 96 mA
SN74BCT541 ..... 128 mA
Operating free-air temperature range: SN54BCT541 ..... −55°C to 125°C
SN74BCT541 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN54BCT541			SN74BCT541			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

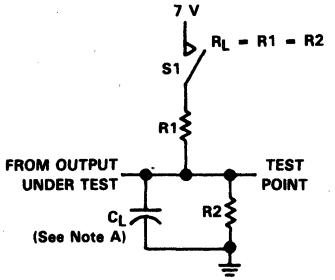
PARAMETER	TEST CONDITIONS†		SN54BCT541			SN74BCT541			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = −12 mA	2	3.2					
		I_{OH} = −15 mA				2	3.1		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
		I_{OL} = 64 mA					0.42	0.55	
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50			50	μA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50			−50	μA
I_I	V_{CC} = 5.5 V, V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V				−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V, V_O = 0		−100		−225	−100		−225	mA
I_{CCL}	V_{CC} = 5.5 V			47	72		47	72	mA
I_{CCH}	V_{CC} = 5.5 V			27	40		27	40	mA
I_{CCZ}	V_{CC} = 5.5 V			5	7		5	7	mA
C_i	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			5			5		pF
C_o	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			10			10		

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT541			SN54BCT541		SN74BCT541		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2.1	3.7	5.3	1.7	6.3	1.7	6	ns
t_{PHL}	A	Y	3.7	5.5	7.5	3.2	8.7	3.4	8.2	ns
t_{PZH}	$\overline{G}$	Y	5.3	7.2	9.3	4.4	11	4.6	10.7	ns
t_{PZL}	$\overline{G}$	Y	6	8	10.4	5.4	12.4	5.4	11.5	ns
t_{PHZ}	$\overline{G}$	Y	3.5	5.6	7.6	3	9.1	3	8.6	ns
t_{PLZ}	$\overline{G}$	Y	3.4	5.2	7.2	3	9.4	3	8.6	ns

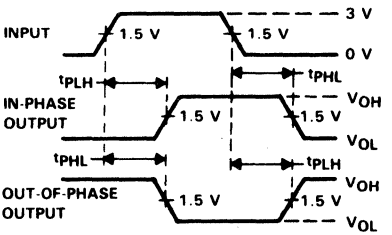
PARAMETER MEASUREMENT INFORMATION



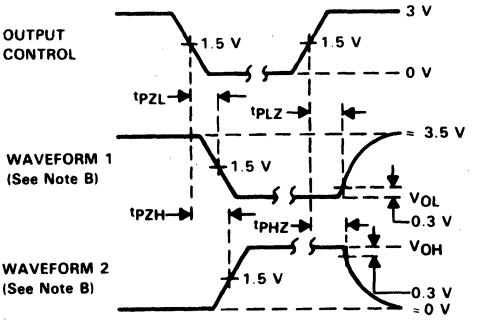
LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by the generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1. SWITCHING CHARACTERISTICS

- **3-State True Outputs**
- **Back-to-Back Registers for Storage**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Standard Plastic and Ceramic 300-mil DIPs**

description

The 'BCT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$ or $\overline{LEBA}$) and Output Enable ($\overline{GAB}$ or $\overline{GBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B Enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. Having $\overline{CEAB}$ low and $\overline{LEAB}$ low makes the A-to-B latches transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{GAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$ inputs.

The SN54BCT543 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT543 is characterized for operation from 0°C to 70°C.

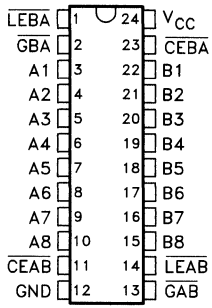
FUNCTION TABLE

INPUTS				OUTPUTS	LATCH STATUS
$\overline{GAB}$	$\overline{CEAB}$	$\overline{LEAB}$	DATA	B1 THRU B8	A TO B†
H	X	X	X	Z	OUTPUTS DISABLED
L	H	L	L	Z	OUTPUTS DISABLED
L	H	L	H	Z	DATA LATCHED
L	L	H	H	L	DATA LATCHED‡
L	L	H	H	H	
L	L	L	L	L	TRANSPARENT
L	L	L	H	H	

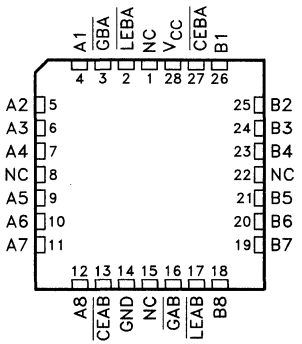
† A-to-B data flow is shown: B-to-A flow control is the same except uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$.

‡ Data present before low-to-high transition of $\overline{LEAB}$.

SN54BCT543 ... JT PACKAGE
SN74BCT543 ... DW OR NT PACKAGE
(TOP VIEW)

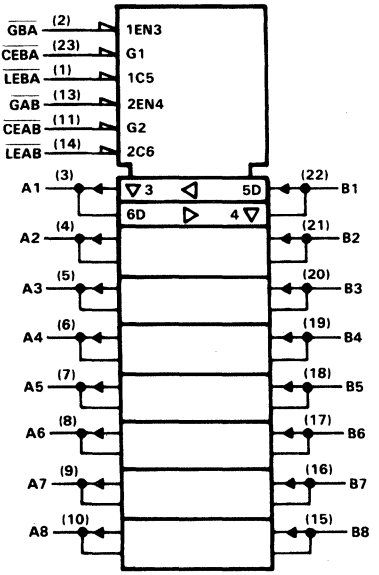


SN54BCT543 ... FK PACKAGE
(TOP VIEW)



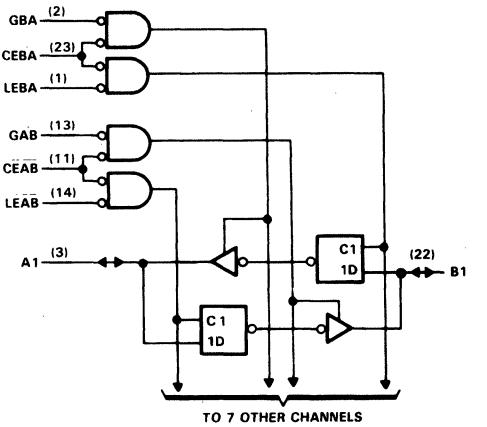
NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage (I/O ports) (see Note 1)	−0.5 V to 5.5 V
Input voltage (Excluding I/O ports) (see Note 1)	−0.5 V to 7 V
Voltage applied to any output in the high state	−0.5 V to V_{CC}
Input clamp current	−30 mA
Current into any output in the low state: SN54BCT543	96 mA
SN74BCT543	128 mA
Operating free-air temperature range: SN54BCT543	−55°C to 125°C
SN74BCT543	0°C to 70°C
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN54BCT543			SN74BCT543			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT543			SN74BCT543			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
			I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
			I_{OL} = 64 mA					0.42	0.55	
I_I		V_{CC} = 5.5 V, V_I = 5.5 V				0.4			0.4	mA
I_{IH}§	Control inputs	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
	A and B					70			70	
I_{IL}§	Control inputs	V_{CC} = 5.5 V, V_I = 0.5 V				−0.6			−0.6	mA
	A and B					−0.65			−0.65	
I_{OS}‡		V_{CC} = 5.5 V, V_O = 0		−100		−225	−100		−225	mA
I_{CCL}		V_{CC} = 5.5 V			45	71		45	71	mA
I_{CCH}		V_{CC} = 5.5 V			5	8		5	8	mA
I_{CCZ}		V_{CC} = 5.5 V			9	15		5	15	mA
C_i	Control inputs	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			6			6		pF
C_{io}	A and B	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			16			16		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

timing requirements

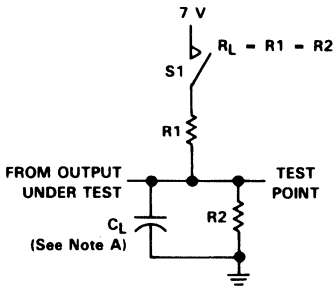
		V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN TO MAX†				UNIT
		'BCT543		SN54BCT543		SN74BCT543		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{su}	Setup time, data before latch enable ↑	4.5		4.5		4.5		ns
t_h	Hold time, data after latch enable ↑	1.5		1.5		1.5		ns
t_w	Pulse duration, latch enable low	7		7		7		ns

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN TO MAX†				UNIT
			'BCT543			SN54BCT543		SN74BCT543		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	5.7	7.5	2	9.9	2	8.8	ns
t_{PHL}			2	6.3	8.2	2	9.7	2	9.6	
t_{PLH}	$\overline{LE}$	A or B	2	8.2	10.3	2	13.9	2	12.9	ns
t_{PHL}			2	8.5	10.6	2	13.2	2	12.7	
t_{PZH}	$\overline{G}$	A or B	1	6.8	8.6	1	11.4	1	10.7	ns
t_{PZL}			1	8.7	10.8	1	12.8	1	12.3	
t_{PHZ}	$\overline{G}$	A or B	1	5.5	7.2	1	8.8	1	8.1	ns
t_{PLZ}			1	4.7	6.4	1	8.1	1	7.2	
t_{PZH}	$\overline{CE}$	A or B	1	7.6	9.8	1	12.8	1	12	ns
t_{PZL}			1	9.5	11.6	1	13.8	1	13.5	
t_{PHZ}	$\overline{CE}$	A or B	1	5.8	7.5	1	9.3	1	8.5	ns
t_{PLZ}			1	4.8	6.7	1	8.4	1	7.6	

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

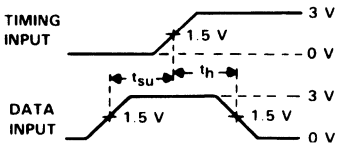
PARAMETER MEASUREMENT INFORMATION



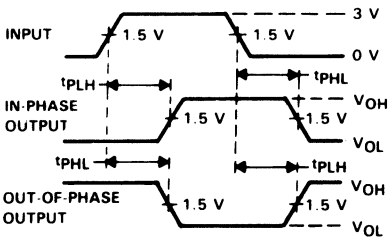
LOAD CIRCUIT

SWITCH POSITION TABLE

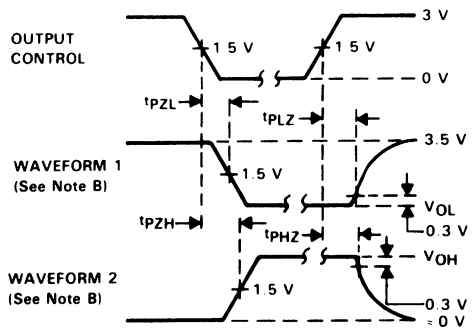
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 2.5 ns, t_f = 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

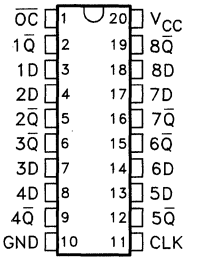
FIGURE 1. SWITCHING CHARACTERISTICS

SN54BCT534, SN74BCT534
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

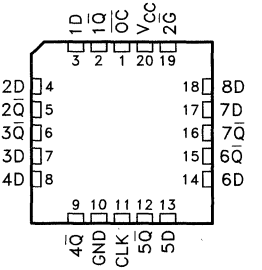
D3322, AUGUST 1989

- **8 D-Type Flip-Flops In a Single Package**
- **3-State Bus-Driving Inverting Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **State of the Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **Functionally Equivalent to 54F534 and 74F534**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C Method 3015**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54BCT534 ... J PACKAGE
SN74BCT534 ... DW OR N PACKAGE
(TOP VIEW)



SN54BCT534 ... FK PACKAGE
(TOP VIEW)



description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 'BCT534 are edge-triggered D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs will be set to the complement of the logic levels that were set up at the D inputs.

A buffered output-control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ($\overline{OC}$) does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

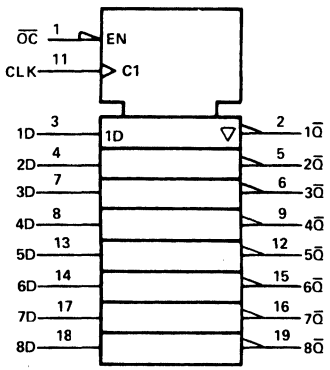
The SN54BCT534 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT534 is characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

FUNCTION TABLE
(each flip-flop)

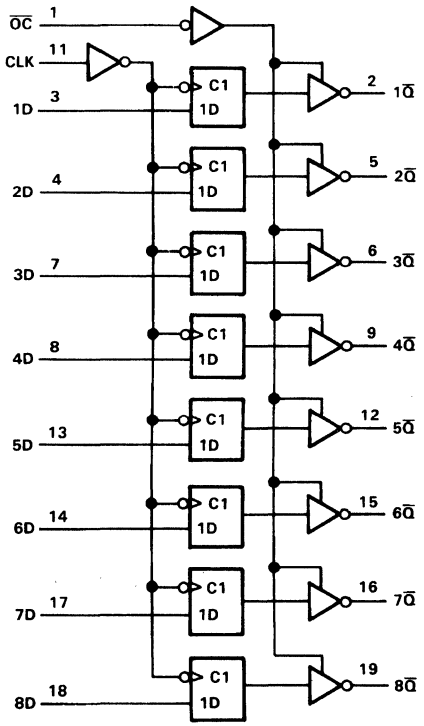
INPUTS			OUTPUTS
$\overline{OC}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage, V_I (see Note 1) ..... 0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Input clamp current ..... −30 mA
Current into any output in the low state: SN54BCT534 ..... 96 mA
SN74BCT534 ..... 128 mA
Operating free-air temperature range: SN54BCT534 ..... −55°C to 125°C
SN74BCT534 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		SN54BCT534			SN74BCT534			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT534			SN74BCT534			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = −12 mA	2	3.2					
		I_{OH} = −15 mA				2	3.1		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
		I_{OL} = 64 mA					0.42	0.55	
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50			50	μA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50			−50	μA
I_I	V_{CC} = 5.5 V, V_I = 5.5 V				0.4			0.4	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V				−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0		−100		−225	−100		−225	mA
I_{CCL}	V_{CC} = 5.5 V, V_O = 0			38	55		38	55	mA
I_{CCH}	V_{CC} = 5.5 V, V_O = 0			5	8		5	8	mA
I_{CCZ}	V_{CC} = 5.5 V, V_O = 0			4.5	7		4.5	7	mA
C_i	V_I = V_{CC} or GND, V_{CC} = 5 V			6			6		pF
C_o	V_O = V_{CC} or GND, V_{CC} = 5 V			10			10		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

timing requirements

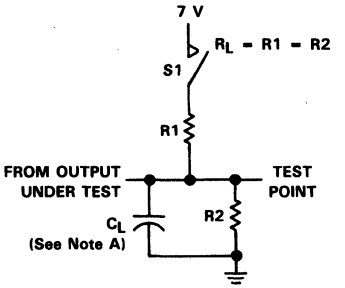
			V_{CC} = 5V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'BCT534		SN54BCT534		SN74BCT534		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	77	0	77	0	77	MHz
t_{su}	Setup time, before enable CLK ↑	Data high	6		6		6		ns
		Data low	9.5		9.5		9.5		
t_h	Hold time after CLK ↑	Data high	0		0		0		ns
		Data low	1		1		1		
t_w	Pulse duration	CLK high	6		6		6		ns
		CLK low	7		7		7		

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT534			SN54BCT534		SN74BCT534		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			77			77		77		MHz
t_{PLH}	CLK	$\overline{Q}$	3.3	6.7	9.6	3.3	12.8	3.3	11.4	ns
t_{PHL}			3.5	6.2	8.8	3.5	11	3.5	10	
t_{PZH}	$\overline{OC}$	$\overline{Q}$	3.9	7.6	10.3	3.9	13.1	3.9	12.5	ns
t_{PZL}			4.6	8.2	11.1	4.6	13.7	4.6	13.3	
t_{PHZ}	$\overline{OC}$	$\overline{Q}$	2.6	4.7	6.7	2.6	8	2.6	7.4	ns
t_{PLZ}			1.8	4.1	6.1	1.8	7.8	1.8	6.9	

† For conditions as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

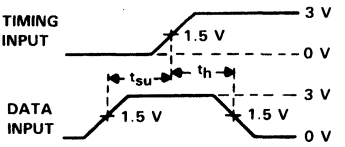
PARAMETER MEASUREMENT INFORMATION



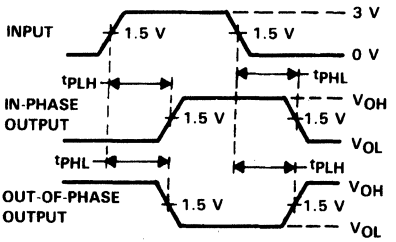
LOAD CIRCUIT

SWITCH POSITION TABLE

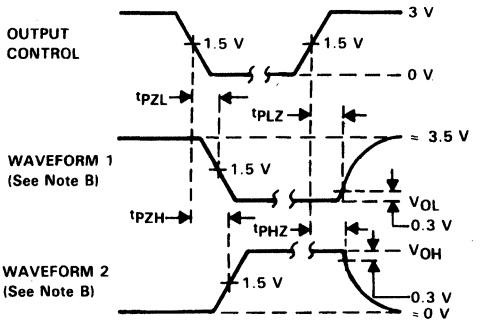
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 2.5 ns, t_f = 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

D3196, SEPTEMBER 1987—REVISED NOVEMBER 1988

- **State of the Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **P-N-P Inputs Reduce DC Loading**
- **Functionally Equivalent to 54F620 and 74F620**
- **ESD Protection Exceeds 2000 V per MIL-STD-833C Method 3015**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

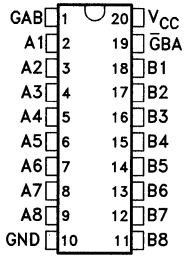
These octal bus transceivers are designed for asynchronous two-way communications between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

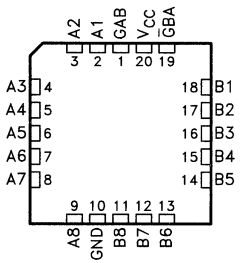
The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the octal bus transceivers the capability to store data by simultaneous activation of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. When both enable inputs are activated and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

The SN54BCT620A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT620A is characterized for operation from 0°C to 70°C.

SN54BCT620A . . . J PACKAGE
SN74BCT620A . . . DW OR N PACKAGE
(TOP VIEW)



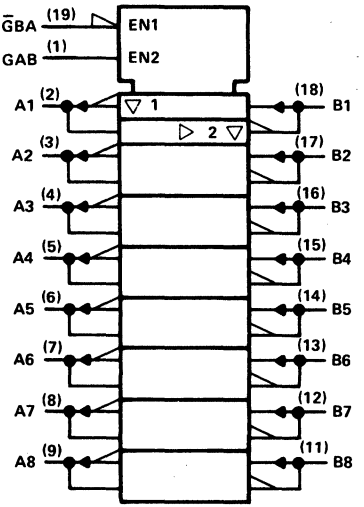
SN54BCT620A . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

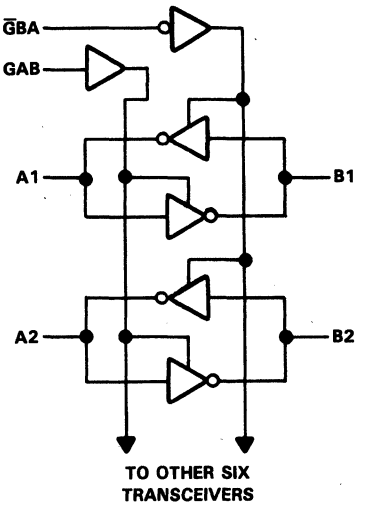
ENABLE INPUTS		OPERATION
$\overline{G}$BA	GAB	BCT620A
L	L	$\overline{B}$ data to A bus
H	H	$\overline{A}$ data to B bus
H	L	Isolation
L	H	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage (see Note 1): Control inputs	−0.5 V to 7 V
I/O ports	−0.5 V to 5.5 V
Voltage applied to any output in the disabled or power-off state	−0.5 V to 5.5 V
Voltage applied to any output in the high state	−0.5 V to V_{CC}
Input clamp current	−30 mA
Current into any output in the low state: SN54BCT620A	96 mA
SN74BCT620A	128 mA
Operating free-air temperature range: SN54BCT620A	−55°C to 125°C
SN74BCT620A	0°C to 70°C
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

			SN54BCT620A			SN74BCT620A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	Any A			−3			−3	mA
		Any B			−12			−15	mA
I_{OL}	Low-level output current	Any A			20			24	mA
		Any B			48			64	mA
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT620A			SN74BCT620A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Any A	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
			I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
	Any B	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
			I_{OH} = −12 mA	2	3.2					V
			I_{OH} = −15 mA				2	3.1		V
V_{OL}	Any A	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5				V
			I_{OL} = 24 mA					0.35	0.5	V
	Any B	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
			I_{OL} = 64 mA					0.42	0.55	V
I_I	A and B	V_{CC} = 5.5 V,	V_I = 5.5 V			1.0			1.0	mA
	GAB or $\overline{GBA}$	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}‡	A and B	V_{CC} = 5.5 V,	V_I = 2.7 V			70			70	μA
	GAB or $\overline{GBA}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}‡	A and B	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.65			−0.65	mA
	GAB or $\overline{GBA}$	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.60			−0.60	mA
I_{OS}§	Any A	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
	Any B	V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CCH}		V_{CC} = 5.5 V,	See Note 2		23	37		23	37	mA
I_{CCL}		V_{CC} = 5.5 V,	See Note 2		53	84		53	84	mA
I_{CCZ}		V_{CC} = 5.5 V			4	10		4	10	mA
C_i	GAB or $\overline{GBA}$	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		5			5		pF
C_{io}	A	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		9			9		pF
	B				12			12		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: I_{CCH} and I_{CCL} are measured in the A to B mode.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT620A			SN54BCT620A		SN74BCT620A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	0.6	3.4	5.2	0.6	6.2	0.6	5.8	ns
t_{PHL}			0.1	1.9	3.4	0.1	3.7	0.1	3.6	
t_{PLH}	B	A	0.9	4.1	6	0.9	7.2	0.9	6.9	ns
t_{PHL}			0.1	2	3.7	0.1	4	0.1	3.9	
t_{PZH}	$\overline{G}$BA	A	3.5	7.2	9.2	3.5	10.9	3.5	10.6	ns
t_{PZL}			3.7	7.6	9.9	3.7	11.5	3.7	11.1	
t_{PHZ}	$\overline{G}$BA	A	3.1	5.3	8.6	3.1	10.8	3.1	10	ns
t_{PLZ}			1.3	4.4	6.9	1.3	8.3	1.3	7.8	
t_{PZH}	GAB	B	2	5.3	6.7	2	7.9	2	7.4	ns
t_{PZL}			2.9	6.1	8.1	2.9	9.2	2.9	9	
t_{PHZ}	GAB	B	2.1	5.2	7	2.1	8.5	2.1	8.1	ns
t_{PLZ}			0.1	3.7	5.3	0.1	6	0.1	5.9	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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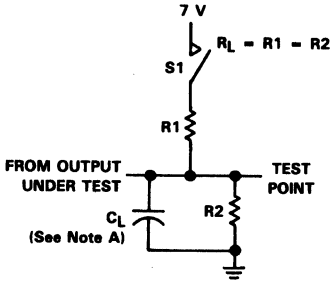
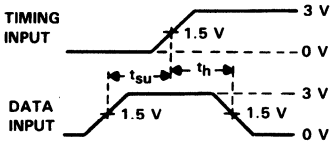
PARAMETER MEASUREMENT INFORMATION



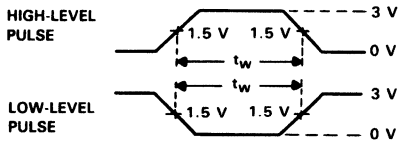
LOAD CIRCUIT

SWITCH POSITION TABLE

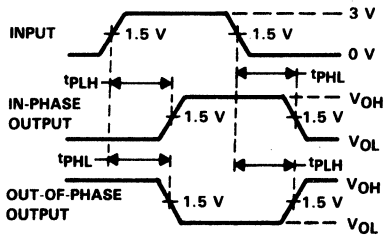
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



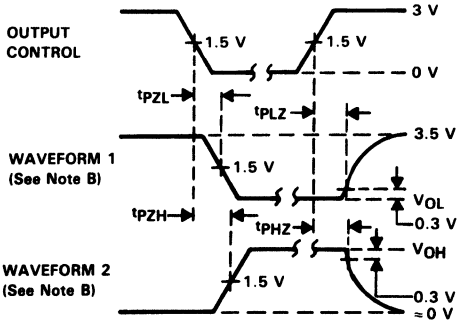
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

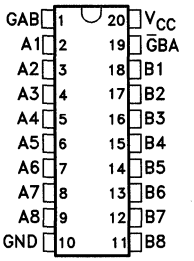
FIGURE 1. SWITCHING CHARACTERISTICS

SN54BCT623, SN74BCT623
OCTAL BUS TRANSCEIVERS

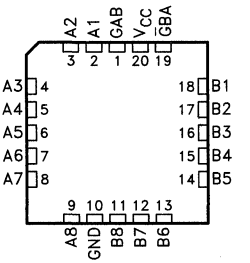
D3057, SEPTEMBER 1988—REVISED NOVEMBER 1988

- **State of the Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **Functionally Equivalent to SN54F623 and SN74F623**
- **ESD Protection Exceeds 2000 V per MIL-STD-833C Method 3015**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54BCT623 ... J PACKAGE
SN74BCT623 ... DW OR N PACKAGE
(TOP VIEW)



SN54BCT623 ... FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communications between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the octal bus transceivers the capability to store data by simultaneous activation of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. When both enable inputs are activated and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

The SN54BCT623 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT623 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

ENABLE INPUTS		OPERATION
$\overline{G}$BA	GAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation
L	H	B data to A bus
L	H	A data to B bus

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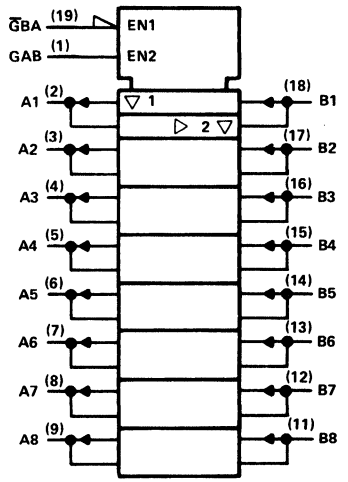
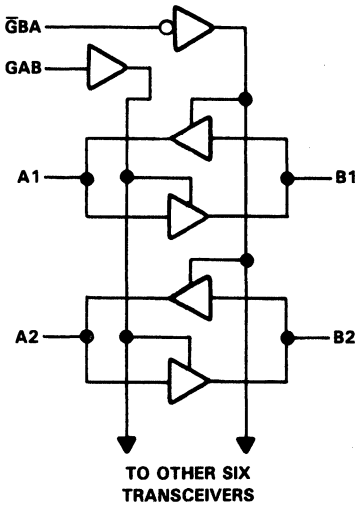
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage (see Note 1): Control inputs	−0.5 V to 7 V
I/O ports	−0.5 V to 5.5 V
Voltage applied to any output in the disabled or power-off state	−0.5 V to 5.5 V
Voltage applied to any output in the high state	−0.5 V to V_{CC}
Input clamp current	−30 mA
Current into any output in the low state: SN54BCT623	96 mA
SN74BCT623	128 mA
Operating free-air temperature range: SN54BCT623	−55°C to 125°C
SN74BCT623	0°C to 70°C
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

			SN54BCT623			SN74BCT623			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	Any A			−3			−3	mA
		Any B			−12			−15	
I_{OL}	Low-level output current	Any A			20			24	mA
		Any B			48			64	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT623			SN74BCT623			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Any A	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
			I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	Any B	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
			I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
V_{OL}	Any A	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
	Any B	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				
			I_{OL} = 64 mA					0.42	0.55	
I_I	A and B	V_{CC} = 5.5 V,	V_I = 5.5 V			1			1	mA
	GAB and $\overline{GBA}$	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}‡	A and B	V_{CC} = 5.5 V,	V_I = 2.7 V			70			70	μA
	GAB and $\overline{GBA}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	
I_{IL}‡	A and B	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.65			−0.65	mA
	GAB and $\overline{GBA}$	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	
I_{OS}§	Any A	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
	Any B	V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	
I_{CCH}		V_{CC} = 5.5 V,	See Note 2		33	53		33	53	mA
I_{CCL}		V_{CC} = 5.5 V,	See Note 2		58	92		58	92	mA
I_{CCZ}		V_{CC} = 5.5 V			6	11		6	11	mA
C_{in}	GAB and $\overline{GBA}$	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		5			5		pF
C_{io}	A	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		9			9		pF
C_{io}	B	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		12			12		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: I_{CCH} and I_{CCL} are measured in the A-to-B mode.

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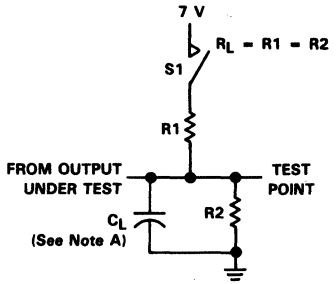
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT623			SN54BCT623		SN74BCT623		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	0.5	3.1	4.7	0.5	5.3	0.5	5.2	ns
t_{PHL}			1.7	4.9	6.9	1.7	7.6	1.7	7.4	
t_{PLH}	B	A	0.9	4.1	5.9	0.9	6.8	0.9	6.7	ns
t_{PHL}			1.8	5.3	7.6	1.8	8.3	1.8	8	
t_{PZH}	$\overline{G}$BA	A	3.1	6.8	9.1	3.1	10.7	3.1	10.6	ns
t_{PZL}			3.3	7.2	9.6	3.3	11.3	3.3	10.7	
t_{PHZ}	$\overline{G}$BA	A	1.9	6.1	8.3	1.9	10.6	1.9	9.8	ns
t_{PLZ}			1.1	4.6	7	1.1	8.1	1.1	7.8	
t_{PZH}	GAB	B	2	5	6.8	2	7.8	2	7.6	ns
t_{PZL}			2.7	6.2	8	2.7	9.3	2.7	8.9	
t_{PHZ}	GAB	B	1.1	4.6	6.5	1.1	8	1.1	7.7	ns
t_{PLZ}			0.3	3.2	6.3	0.3	7.2	0.3	7.1	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

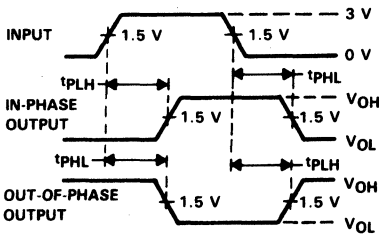
PARAMETER MEASUREMENT INFORMATION



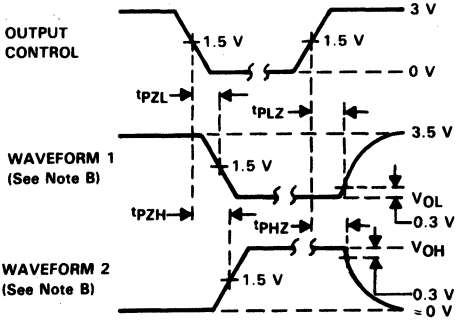
LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

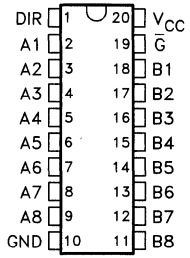
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

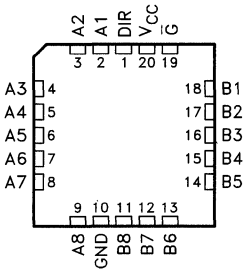
D3057, SEPTEMBER 1988—REVISED FEBRUARY 1989

- **BiCMOS Process with TTL Inputs and Outputs**
- **BiCMOS Design Substantially Reduces Standby Current**
- **Outputs Have Undershoot Protection Circuitry**
- **Power-Up High-Impedance State**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Package Options Include Plastic "Small Outline" Packages, Plastic Chip Carriers, and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54BCT640 ... J PACKAGE
SN74BCT640 ... DW OR N PACKAGE
(TOP VIEW)



SN54BCT640 ... FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated.

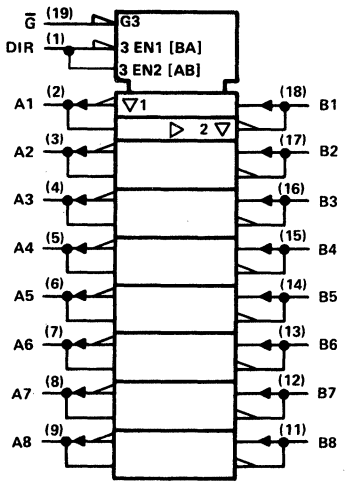
The SN54BCT640 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT640 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

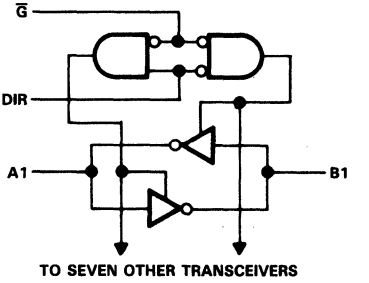
2 BiCMOS Circuits

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage (see Note 1) ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Input clamp current ..... −30 mA
Current into any output in the low state: SN54BCT640 ..... 96 mA
SN74BCT640 ..... 128 mA
Operating free-air temperature range: SN54BCT640 ..... −55°C to 125°C
SN74BCT640 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54BCT640			SN74BCT640			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				18			−18	mA
I_{OH}	High-level output current	A1–A8			−3			−3	mA
		B1–B8			−12			−15	
I_{OL}	Low-level output current	A1–A8			20			24	mA
		B1–B8			48			64	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT640			SN74BCT640			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Any A	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
			I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	Any B	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
			I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
V_{OL}	Any A	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
	Any B	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				
			I_{OL} = 64 mA					0.42	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			1.0			1.0	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}‡	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			70			70	μA
	A or B ports	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	
I_{IL}‡	Control inputs	V_{CC} = 5.5 V,	V_I = 0.5 V			−1.2			−1.2	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.60			−0.60	
I_{OS}§	Any A	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
	Any B	V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	
I_{CCH}		V_{CC} = 5.5 V,	See Note 1		23	37		23	41	mA
I_{CCL}		V_{CC} = 5.5 V,	See Note 1		53	84		53	94	mA
I_{CCZ}		V_{CC} = 5.5 V			4	10		4	11	mA

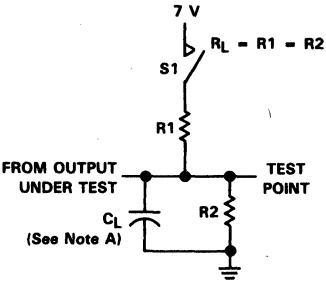
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 1: I_{CCH} and I_{CCL} are measured in the A to B mode.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX¶				UNIT
			'BCT640			SN54BCT640		SN74BCT640		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0.5	3.6	5.6	0.5	7	0.5	6.5	ns
t_{PHL}			0.5	1.9	3.4	0.5	3.8	0.5	3.7	
t_{PZH}	$\overline{G}$	A or B	2.6	6.4	8.9	2.6	10.5	2.6	10.2	ns
t_{PZL}			3.5	6.9	9.5	3.5	12.3	3.5	10.7	
t_{PHZ}	$\overline{G}$	A or B	1.4	5	7.9	1.4	12.2	1.4	10.2	ns
t_{PLZ}			1.5	4.3	6.8	1.5	8.3	1.5	7.8	

¶ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

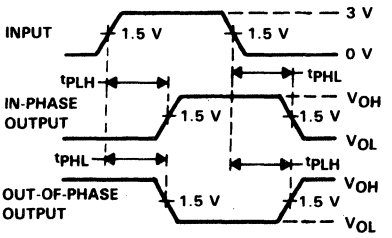
PARAMETER MEASUREMENT INFORMATION



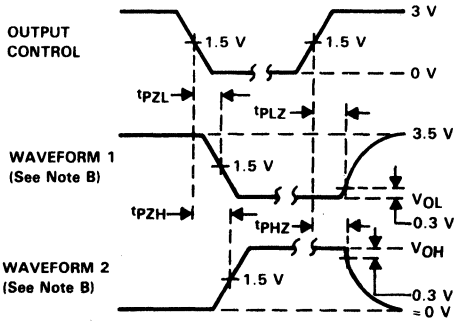
LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by the generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

AUGUST 1989

- **State of the Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **Dependable Texas Instruments Quality and Reliability**
- **Bus Transceivers/Registers**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

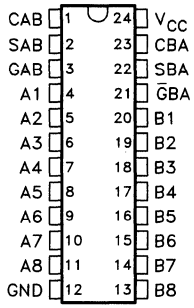
description

These devices consist of bus transceivers circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\overline{GBA}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

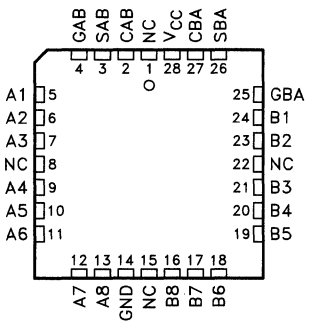
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{GBA}$. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The SN54BCT652 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT652 is characterized for operation from 0°C to 70°C.

SN54BCT652 ... JT PACKAGE
SN74BCT652 ... DW OR NT PACKAGE
(TOP VIEW)



SN54BCT652 ... FK PACKAGE
(TOP VIEW)



2

BiCMOS Circuits

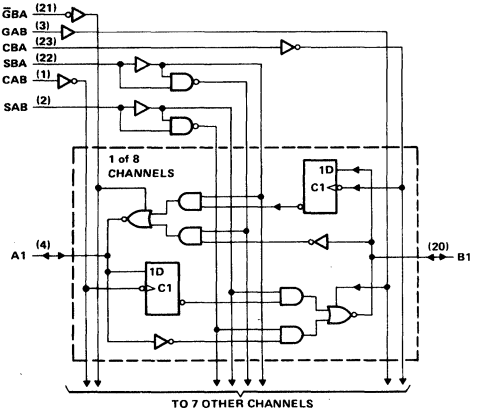
FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, Hold B
H	H	↑	↑	X∫	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, Store B
L	L	↑	↑	X	X∫	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

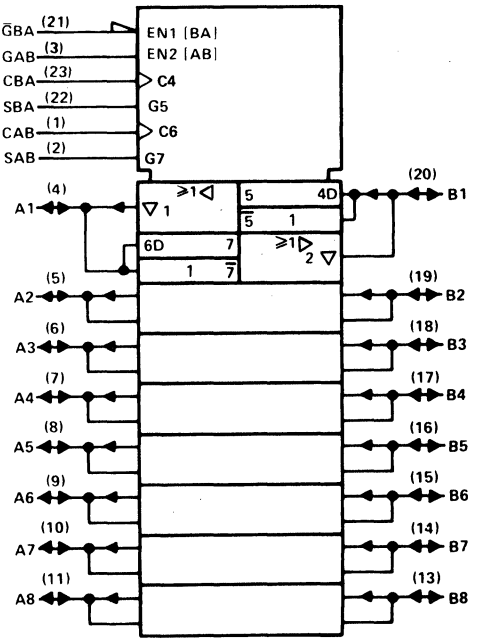
‡ The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input function are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock i.

∫ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.

logic diagram (positive logic)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for JT, DW, or NT packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage (I/O ports) ..... −0.5 V to 5.5 V
Input voltage (Excluding I/O ports) ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state: SN54BCT652 ..... 96 mA
SN74BCT652 ..... 128 mA
Operating free-air temperature range: SN54BCT652 ..... −55°C to 125°C
SN74BCT652 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54BCT652			SN74BCT652			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT652			SN74BCT652			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
			I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
			I_{OL} = 64 mA					0.42	0.55	
I_I	Control Inputs	V_{CC} = 5.5 V, V_I = 5.5 V				1			1	mA
	A or B	V_{CC} = 5.5 V, V_I = 5.5 V				1			1	
I_{IH}‡	Control Inputs	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
	A or B	V_{CC} = 5.5 V, V_I = 2.7 V				70			70	
I_{IL}‡	Control Inputs	V_{CC} = 5.5 V, V_I = 0.5 V				−1			−1	mA
	A or B	V_{CC} = 5.5 V, V_I = 0.5 V				−1			−1	
I_{OS}§		V_{CC} = 5.5 V, V_O = 0 V		−100		−225	−100		−225	mA
I_{CCL}		V_{CC} = 5.5 V, V_I = GND			43	69		43	69	mA
I_{CCH}		V_{CC} = 5.5 V, V_I = 4.5 V			6	10		6	10	mA
I_{CCZ}		V_{CC} = 5.5 V, V_I = GND			10	17		10	17	mA
C_I		V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			6			6		pF
C_{Io}		V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			14			14		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

timing requirements

			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'BCT652		SN54BCT652		SN74BCT652		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	77	0	77	0	77	MHz
t_w	Pulse duration	CBA or CAB high	6.5		6.5		6.5		ns
		CBA or CAB low	6.5		6.5		6.5		
t_{su}	Setup time, before CAB ↑ or CBA ↑	A or B	5		5		5		ns
t_h	Hold time, after CAB ↑ or CBA ↑	A or B	1		1		1		ns

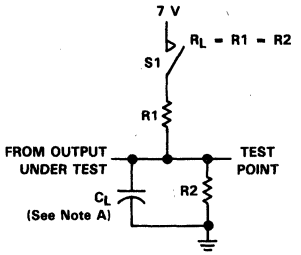
† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operation Conditions.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT652			SN54BCT652		SN74BCT652		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			77			77		77		MHz
t_{PLH}	CBA	A	2.6	6.9	8.9	2.6	11.6	2.6	10.5	ns
t_{PHL}			2.8	6.8	8.8	2.8	10.7	2.8	9.9	
t_{PLH}	CAB	B	2.6	6.9	8.9	2.6	11.6	2.6	10.5	ns
t_{PHL}			2.8	6.8	8.8	2.8	10.7	2.8	9.9	
t_{PLH}	A	B	1.7	5.8	7.5	1.7	10.3	1.7	8.9	ns
t_{PHL}			2.4	6.5	8.2	2.4	10	2.4	9.8	
t_{PLH}	B	A	1.7	5.8	7.5	1.7	10.3	1.7	8.9	ns
t_{PHL}			2.4	6.5	8.2	2.4	10	2.4	9.8	
t_{PLH}	SBA‡ (with B high)	A	3.5	8.8	10.8	3.5	14.2	3.5	13.1	ns
t_{PHL}			2.4	5.9	7.7	2.4	9.1	2.4	8.5	
t_{PLH}	SBA‡ (with B low)	A	3	7.6	9.7	3	12.4	3	11.3	ns
t_{PHL}			3.8	8.3	10.4	3.8	12.9	3.8	12.5	
t_{PLH}	SAB‡ (with A high)	B	3.5	8.8	10.8	3.5	14.2	3.5	13.1	ns
t_{PHL}			2.4	5.9	7.7	2.4	9.1	2.4	8.5	
t_{PLH}	SAB‡ (with A low)	B	3	7.6	9.7	3	12.4	3	11.3	ns
t_{PHL}			3.8	8.3	10.4	3.8	12.9	3.8	12.5	
t_{PZH}	$\overline{G}$BA	A	2.5	7.2	8.9	2.5	11.2	2.5	10.6	ns
t_{PZL}			3.2	8.1	10.1	3.2	12.6	3.2	12	
t_{PHZ}	$\overline{G}$BA	A	2.8	6.7	8.8	2.8	10.9	2.8	10	ns
t_{PLZ}			2.4	6.3	8.4	2.4	10.5	2.4	9.5	
t_{PZH}	GAB	B	1.5	5.4	7.1	1.5	8.7	1.5	8.1	ns
t_{PZL}			2.3	6.2	8.1	2.3	9.9	2.3	9.3	
t_{PHZ}	GAB	B	3.5	8.2	10	3.5	12.2	3.5	11.6	ns
t_{PLZ}			2.8	7.2	9.5	2.8	12	2.8	11.3	

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
‡ These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

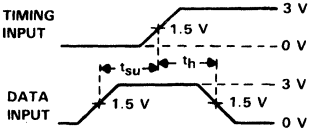
PARAMETER MEASUREMENT INFORMATION



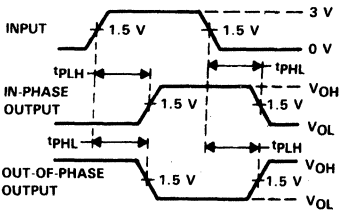
LOAD CIRCUIT

SWITCH POSITION TABLE

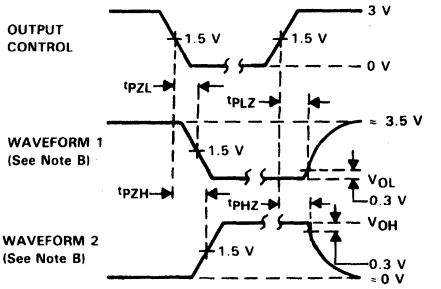
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 2.5 ns, t_f = 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

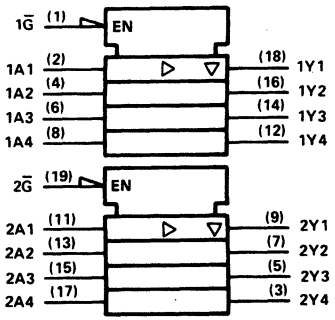
- **Open-Collector Version of 'BCT244**
- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V per MIL-STD-883C Method 3015**
- **Package Options Include "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT756 and 'BCT757, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs.

The SN54BCT760 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT760 is characterized for operation from 0°C to 70°C.

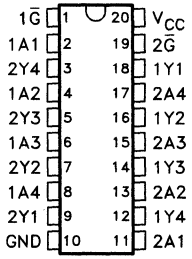
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

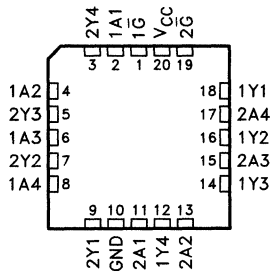
SN54BCT760 ... J PACKAGE
SN74BCT760 ... DW OR N PACKAGE

(TOP VIEW)



SN54BCT760 ... JK PACKAGE

(TOP VIEW)

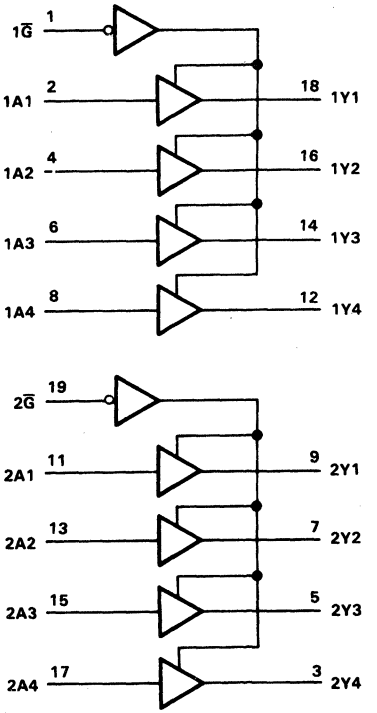


FUNCTION TABLE

OUTPUT CONTROL $\overline{G}$	DATA INPUT A	OUTPUT Y
H	X	Z
L	L	L
L	H	H

2 BiCMOS Circuits

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage, V_I (see Note 1) ..... −0.5 V to 7 V
Input current, I_I ..... −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state: SN54BCT760 ..... 96 mA
SN74BCT760 ..... 128 mA
Operating free-air temperature range: SN54BCT760 ..... −55°C to 125°C
SN74BCT760 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The negative input voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN54BCT760			SN74BCT760			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT760			SN74BCT760			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
I_{OH}	V_{CC} = 4.5 V, V_{OH} = 5.5 V				0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA			0.38	0.55				V
	V_{CC} = 4.5 V, I_{OL} = 64 mA						0.42	0.55	
I_I	V_{CC} = 5.5 V, V_I = 5.5 V				0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V				−1			−1	mA
I_{CC}	V_{CC} = 5.5 V, Outputs open	Outputs high		21	33		21	33	μA
		Outputs low		48	76		48	76	
C_i	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			6			6		pF
C_o	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			10			10		pF

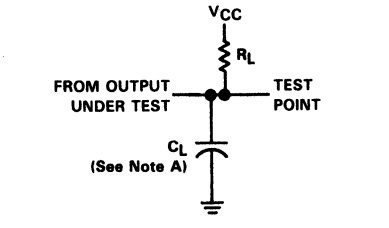
† All typical values are at V_{CC} = 5 V, T_A = 25°C.

'BCT760 switching characteristics (see Figure 1)

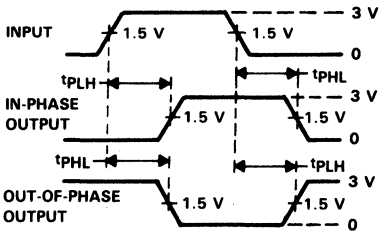
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX‡				UNIT
			'BCT760			SN54BCT760		SN74BCT760		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any A	Y	6.3	8	9.5	6.3	11.1	6.3	10	ns
t_{PHL}			2.1	4.3	6.5	2.1	7.7	2.1	7.2	
t_{PLH}	Any $\overline{G}$	Y	8.6	13	15.2	8.6	18.7	8.6	17.5	ns
t_{PHL}			3.2	6.2	8.9	3.2	10.4	3.2	9.9	

‡ For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

D3057, SEPTEMBER 1988—REVISED JULY 1989

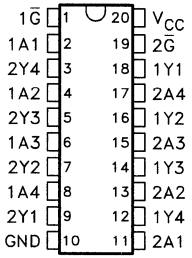
- **BiCMOS Design Substantially Reduces Standby Current**
- **Output Ports have Equivalent 33-Ω Series Resistors so No External Resistors are Required**
- **ESD Protection Exceeds 2000 V, MIL-STD-883C, Method 3015**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

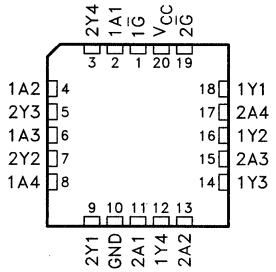
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT2241 and 'BCT2244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out and improved fan-in.

The SN54BCT2240 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT2240 is characterized for operation from 0°C to 70°C.

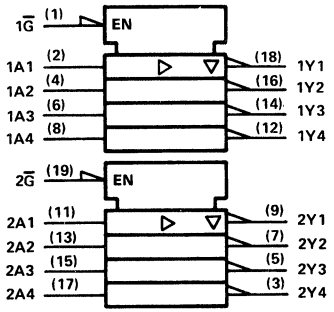
SN54BCT2240 . . . J PACKAGE
SN74BCT2240 . . . DW OR N PACKAGE
(TOP VIEW)



SN54BCT2240 . . . FK PACKAGE
(TOP VIEW)

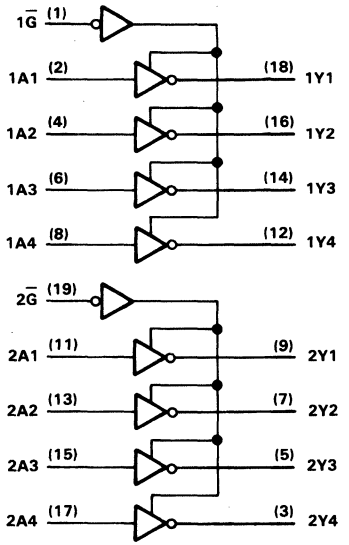


logic symbol†

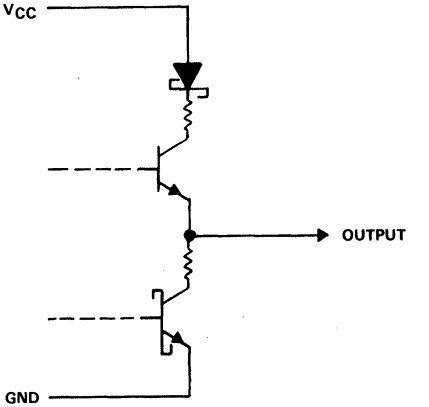


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of each output



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage (see Note 1) ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Input clamp current ..... −30 mA
Current into any output in the low state: SN54BCT2240 ..... 96 mA
SN74BCT2240 ..... 128 mA
Operating free-air temperature range: SN54BCT2240 ..... −55°C to 125°C
SN74BCT2240 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN54BCT2240			SN74BCT2240			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−12	mA
I_{OL}	Low-level output current			12			12	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

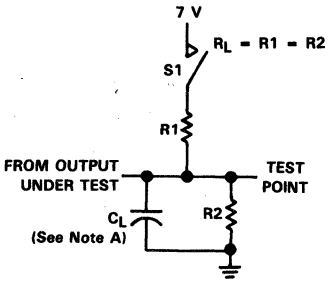
PARAMETER	TEST CONDITIONS		SN54BCT2240			SN74BCT2240			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_{OH} = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = −12 mA	2	3.2		2	3.2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 1 mA		0.15	0.5		0.15	0.5	V
		I_{OL} = 12 mA		0.35	0.8		0.35	0.8	
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−1			−1	mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open		19	32		19	32	mA
I_{CCL}				46	76		46	76	
I_{CCZ}				6	8		6	8	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX			UNIT
			'BCT2240			SN54BCT2240		SN74BCT2240	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	0.5	3.4	4.8	0.5	6.3	0.5	5.7	ns
t_{PHL}			0.5	2.8	4	0.5	4.6	0.5	4.4	
t_{PZH}	$\overline{G}$	Y	2.6	6.2	8.2	2.6	10.1	2.6	9.3	ns
t_{PZL}			4.3	8.8	10.9	4.3	12.9	4.3	12.4	
t_{PHZ}	$\overline{G}$	Y	2	5.3	7.1	2	9.2	2	8.7	ns
t_{PLZ}			2.2	6.7	8.5	2.2	12.2	2.2	10.6	

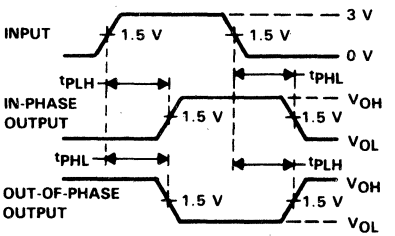
PARAMETER MEASUREMENT INFORMATION



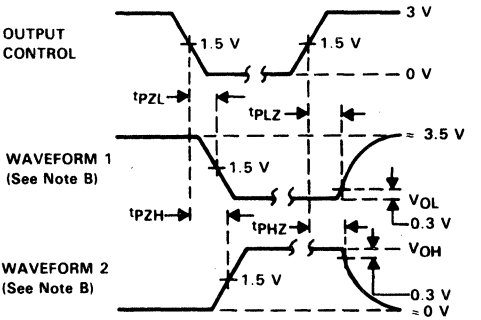
LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by the generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

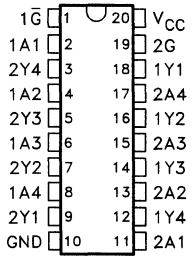
- **BiCMOS Design Substantially Reduces Standby Current**
- **Output Ports have Equivalent 33-Ω Series Resistors so No External Resistors are Required**
- **ESD Protection Exceeds 2000 V**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

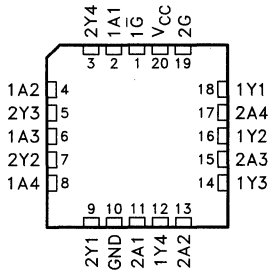
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT2240 and 'BCT2244, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out and improved fan-in.

The SN54BCT2241 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT2241 is characterized for operation from 0°C to 70°C.

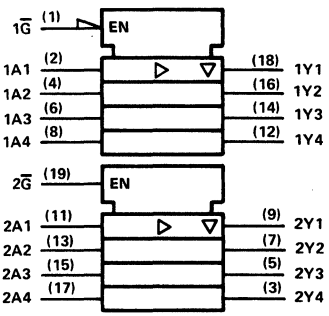
SN54BCT2241 ... J PACKAGE
SN74BCT2241 ... DW OR N PACKAGE
(TOP VIEW)



SN54BCT2241 ... FK PACKAGE
(TOP VIEW)

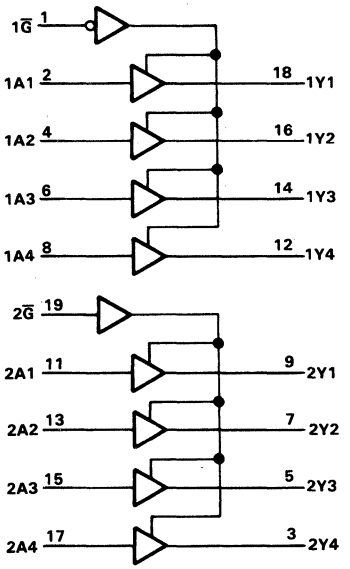


logic symbol†

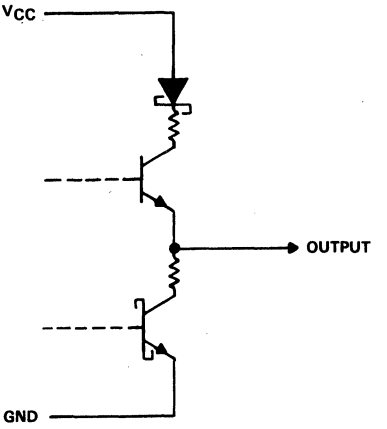


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of each output



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Operating free-air temperature ranges: SN54BCT2241 ..... −55°C to 125°C
SN74BCT2241 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54BCT2241			SN74BCT2241			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−12	mA
I_{OL}	Low-level output current			12			12	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

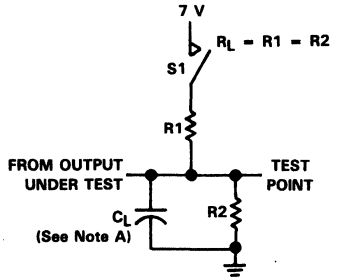
PARAMETER	TEST CONDITIONS		SN54BCT2241			SN74BCT2241			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_{OH} = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = −12 mA	2	3.2					
V_{OL}	V_{CC} = 4.5 V	I_{OL} = −12 mA		0.38	0.55				V
		I_{OL} = 12 mA					0.42	0.55	
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−1			−1	mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open		23	37		23	37	mA
I_{CCL}				37	76		37	76	
I_{CCZ}				6	9		6	9	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'BCT2241			SN54BCT2241		SN74BCT2241		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.1	3	4.4	1.1	5.1	1.1	4.9	ns
t_{PHL}			2.9	4.9	6.6	2.9	7.2	2.9	6.9	
t_{PZH}	G or $\overline{G}$	Y	2.7	6	7.8	2.7	9.4	2.7	8.9	ns
t_{PZL}			4.1	7.7	9.4	4.1	10.9	4.1	10.3	
t_{PHZ}	G or $\overline{G}$	Y	2.5	5.2	7.2	2.5	9.7	2.5	8.7	ns
t_{PLZ}			3.2	7.1	9.5	3.2	12.9	3.2	11.3	

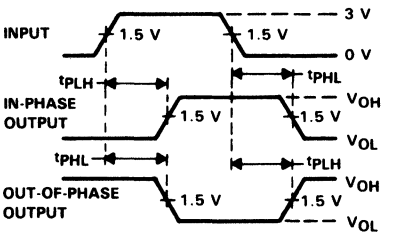
PARAMETER MEASUREMENT INFORMATION



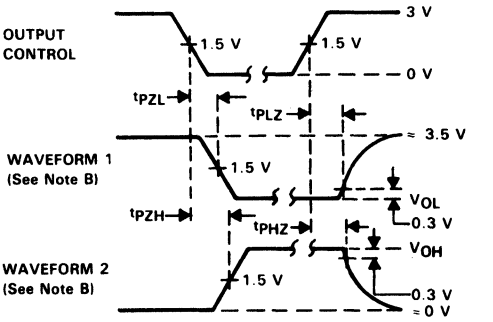
LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by the generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

- **BiCMOS Design Substantially Reduces Standby Current**
- **Output Ports have Equivalent 33-Ω Series Resistors so No External Resistors are Required**
- **ESD Protection Exceeds 2000 V, MIL-STD-883C, Method 3015**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

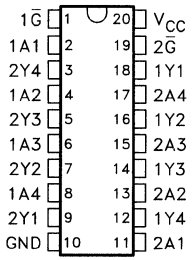
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'BCT2240 and 'BCT2241, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low input control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out and improved fan-in.

The SN54BCT2244 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT2244 is characterized for operation from 0°C to 70°C.

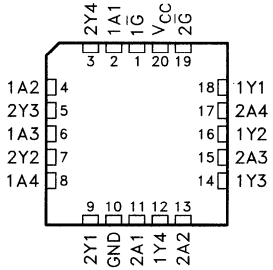
FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

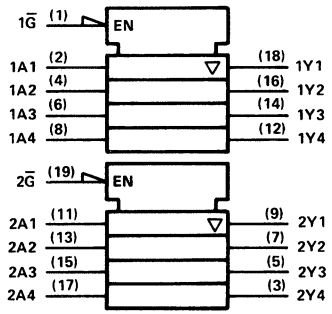
SN54BCT2244 ... J PACKAGE
SN74BCT2244 ... DW OR N PACKAGE
(TOP VIEW)



SN54BCT2244 ... FK PACKAGE
(TOP VIEW)

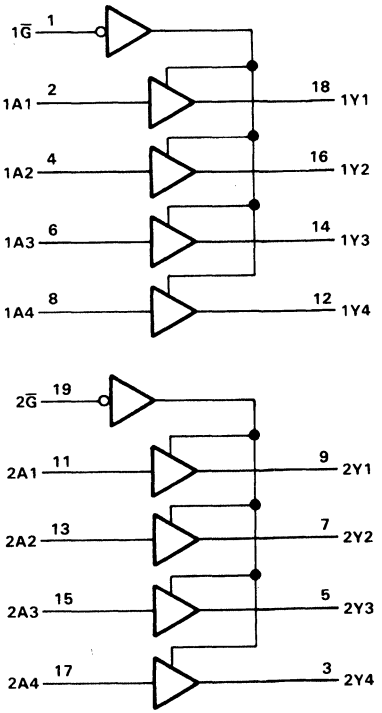


logic symbol†

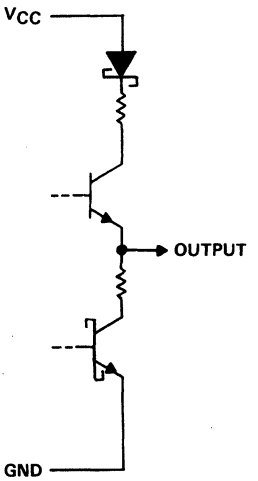


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of each output



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage (see Note 1)	−0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	−0.5 V to 5.5 V
Voltage applied to any output in the high state	−0.5 V to V_{CC}
Input clamp current	−30 mA
Current into any output in the low state: SN54BCT2244	96 mA
SN74BCT2244	128 mA
Operating free-air temperature range: SN54BCT2244	−55°C to 125°C
SN74BCT2244	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN54BCT2244			SN74BCT2244			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−12	mA
I_{OL}	Low-level output current			12			12	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

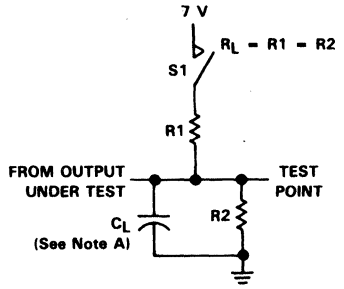
PARAMETER	TEST CONDITIONS		SN54BCT2244			SN74BCT2244			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.4			2.4			V
		I_{OH} = −12 mA	2			2			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 1 mA		0.15	0.5		0.15	0.5	V
		I_{OL} = 12 mA		0.35	0.8		0.35	0.8	
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−1			−1	mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open		23	37		23	37	mA
I_{CCL}				53	77		53	77	
I_{CCZ}				6.5	10		6.5	10	
C_i	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		6			6		pF
C_o	V_{CC} = 5 V,	V_O = 2.5V or 0.5 V		11			11		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			'BCT2244			SN54BCT2244		SN74BCT2244		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	0.5	3	4.4	0.5	5.2	0.5	4.9	ns
t_{PHL}			1.6	4.6	6.3	1.6	7.1	1.6	6.7	
t_{PZH}	$\overline{G}$	Y	2.4	6.1	7.7	2.4	9.1	2.4	8.7	ns
t_{PZL}			3.9	7.6	9.4	3.9	10.8	3.9	10.4	
t_{PHZ}	$\overline{G}$	Y	1.7	5.2	6.9	1.7	8.1	1.7	7.8	ns
t_{PLZ}			2.8	6.5	8.3	2.8	10.9	2.8	9.8	

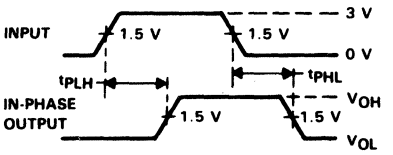
PARAMETER MEASUREMENT INFORMATION



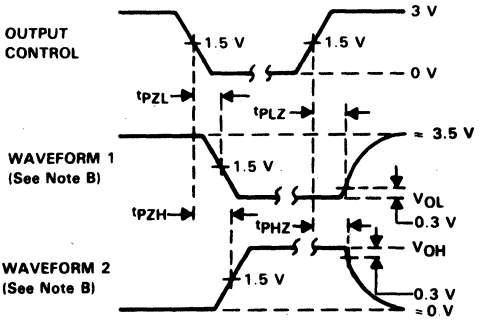
LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

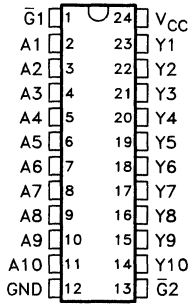
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by the generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

D2977, APRIL 1987—REVISED AUGUST 1989

- **BiCMOS Design Substantially Reduces Standby Current**
- **25-Ω Series Resistors at Outputs Significantly Reduce Overshoot and Undershoot**
- **Specifically Designed to Drive MOS DRAMs**
- **3-State Outputs**
- **Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

These 10-bit buffers and bus drivers are specifically designed to drive the capacitive input characteristics of MOS DRAMs. They provide high-performance bus interface for wide data paths or buses carrying parity.

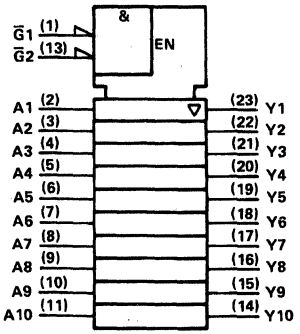
The three-state control gate is a 2-input positive NOR gate so if either $\overline{G}1$ or $\overline{G}2$ is high, all 10 outputs are in the high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down.

The SN74BCT2827A provides true data and the SN74BCT2828A provides inverted data at the outputs.

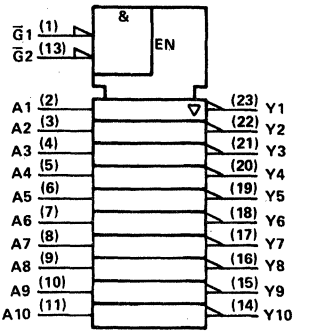
These devices are characterized for operation from 0°C to 70°C.

logic symbols†

SN74BCT2827A



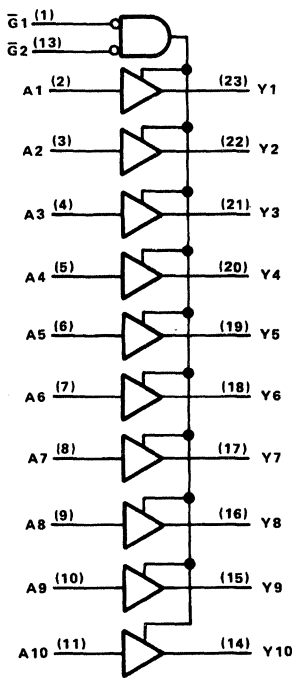
SN74BCT2828A



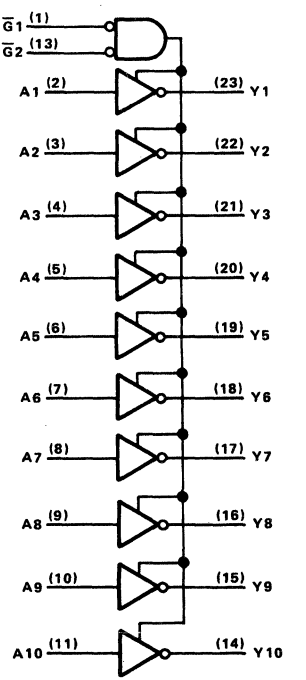
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

SN74BCT2827A



SN74BCT2828A



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage ..... 5.5 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −1 mA	V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.5	V
	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.8	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_{OL}	V_{CC} = 4.5 V,	V_O = 2 V	50			mA
I_{OH}	V_{CC} = 4.5 V,	V_O = 2 V	−35			mA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CCL}	V_{CC} = 5.5 V,	Outputs open		28	40	mA
I_{CCZ}	V_{CC} = 5.5 V,	Outputs open		4.5	8	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y		4	6	2	7	ns
t_{PHL}				6	8	2	9	
t_{PZH}	$\overline{G}$	Y		8	10	4	13	ns
t_{PZL}				11	14	6	17	
t_{PHZ}	$\overline{G}$	Y		8	12	4	15	ns
t_{PLZ}				7	11	3	13	

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage ..... 5.5 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−1	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

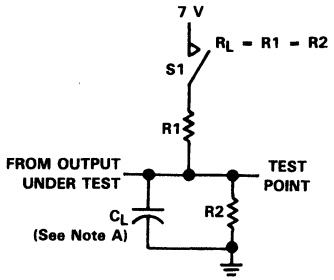
PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −1 mA	V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 1 mA		0.15	0.5	V
	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.35	0.8	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_{OL}	V_{CC} = 4.5 V,	V_O = 2 V	50			mA
I_{OH}	V_{CC} = 4.5 V,	V_O = 2 V	−35			mA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CCL}	V_{CC} = 5.5 V,	Outputs open		28	40	mA
I_{CCZ}	V_{CC} = 5.5 V,	Outputs open		3.5	6	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y		5	7	2	8	ns
t_{PHL}				5	7	2	8	
t_{PZH}	$\overline{G}$	Y		8	11	4	12	ns
t_{PZL}				10	14	6	16	
t_{PHZ}	$\overline{G}$	Y		10	14	4	16	ns
t_{PLZ}				8	12	3	14	

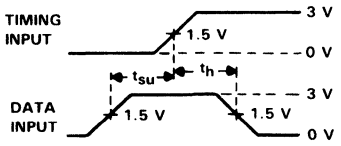
PARAMETER MEASUREMENT INFORMATION



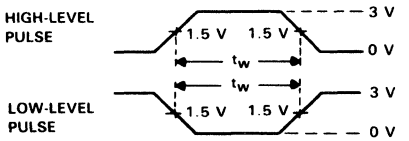
LOAD CIRCUIT

SWITCH POSITION TABLE

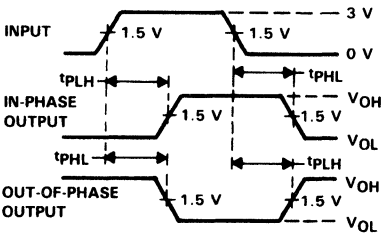
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



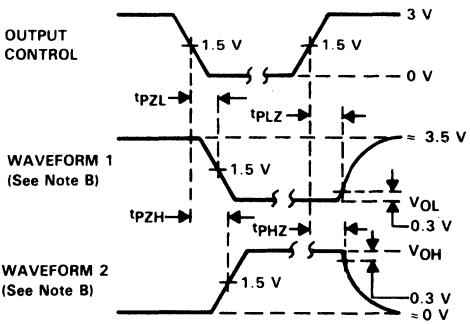
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by the generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

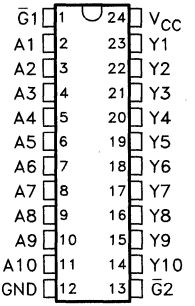
FIGURE 1. SWITCHING CHARACTERISTICS

SN74BCT29827A, SN74BCT29828A
10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS

D2977, APRIL 1987—REVISED JULY 1989

- **BiCMOS Design Substantially Reduces Standby Current**
- **Functionally Equivalent to Am29827, Am29828, SN74ALS29827, and SN74ALS29828**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce DC Loading**
- **Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic and Ceramic DIPs**
- **BiCMOS Process with TTL Inputs and Outputs**
- **Dependable Texas Instruments Quality and Reliability**

DW OR NT PACKAGE
(TOP VIEW)



description

These 10-bit buffers and bus drivers provide high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input positive NOR gate so if either $\overline{G}1$ or $\overline{G}2$ is high, all 10 outputs are in the high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down.

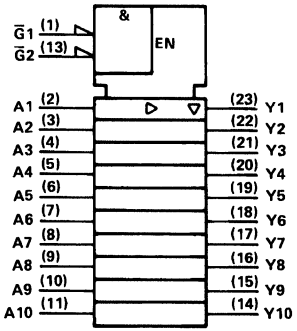
The SN74BCT29827A provides true data and the SN74BCT29828A provides inverted data at the outputs.

The SN74BCT29827A and SN74BCT29828A are characterized for operation from 0°C to 70°C.

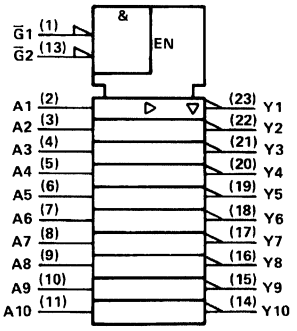
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic symbols†

SN74BCT29827A



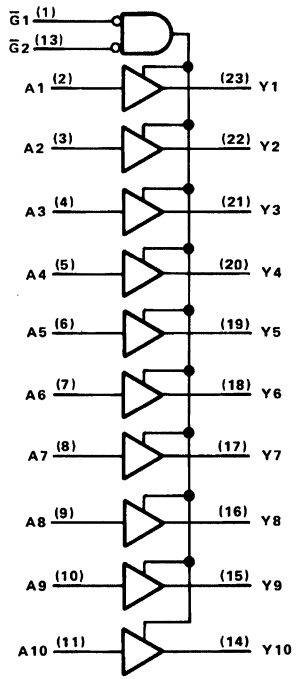
SN74BCT29828A



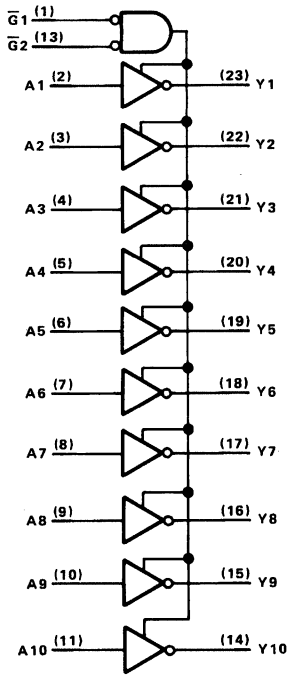
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

SN74BCT29827A



SN74BCT29828A



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage (all inputs and I/O ports) ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = MIN	I_{OH} = −15 mA	2.4			V
		I_{OH} = −24 mA	2			
V_{OL}	V_{CC} = MIN,	I_{OL} = 48 mA		0.35	0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.4 V			−20	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V			−0.2	mA
I_{OS}§	V_{CC} = MAX,	V_O = 0	−75		−250	mA
I_{CCL}	V_{CC} = MAX,	Outputs open		28	40	mA
I_{CCZ}	V_{CC} = MAX,	Outputs open		3.5	6	mA

† For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed 1 second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	1	3.5	6	1	7	ns
t_{PHL}			1	5	7	1	9	
t_{PZH}	$\overline{G}$	Y	2	7	10	2	12	ns
t_{PZL}			2	10	13	2	15	
t_{PHZ}	$\overline{G}$	Y	2	7	10	2	12	ns
t_{PLZ}			2	7	10	2	12	

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage (all inputs and I/O ports) ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

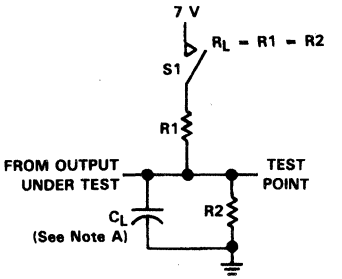
PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = MIN	I_{OH} = −15 mA	2.4			V
		I_{OH} = −24 mA	2			
V_{OL}	V_{CC} = MIN,	I_{OL} = 48 mA		0.35	0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.4 V			−20	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V			−0.2	mA
I_{OS}§	V_{CC} = MAX,	V_O = 0	−75		−250	mA
I_{CCL}	V_{CC} = MAX,	Outputs open		28	40	mA
I_{CCZ}	V_{CC} = MAX,	Outputs open		3.5	6.5	mA

† For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed 1 second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	1	3.5	6	1	7	ns
t_{PHL}			1	3.5	6	1	7	
t_{PZH}	$\overline{G}$	Y	2	7	9	2	11	ns
t_{PZL}			2	9	13	2	15	
t_{PHZ}	$\overline{G}$	Y	2	6	9	2	10	ns
t_{PLZ}			2	6	10	2	11	

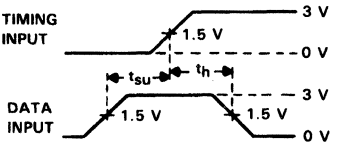
PARAMETER MEASUREMENT INFORMATION



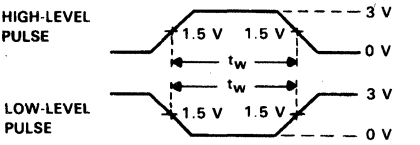
LOAD CIRCUIT

SWITCH POSITION TABLE

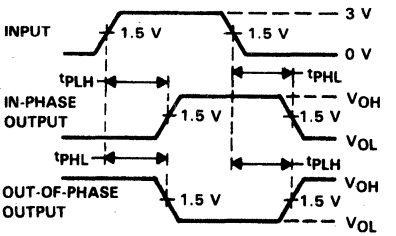
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



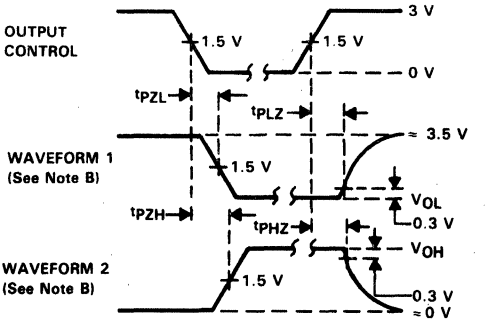
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

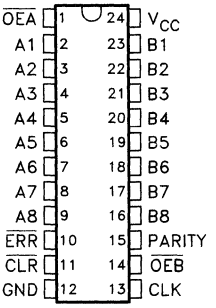
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1. SWITCHING CHARACTERISTICS

D3031, SEPTEMBER 1987—REVISED JULY 1989

- **BiCMOS Process with TTL Inputs and Outputs**
- **BiCMOS Design Reduces Standby Current**
- **Flow-Through Pinout (All Inputs on Opposite Side from Outputs)**
- **Functionally Equivalent to AMD Am29833, Am29834, 'ALS29833, and 'ALS29834**
- **High-Speed Bus Transceivers with Parity Generator/Checker**
- **Parity Error Flag with Open-Collector Output**
- **Has a Register for Storage of the Parity Error Flag**
- **Choice of True ('BCT29833) or Inverting ('BCT29834) Logic**
- **Package Options Include Plastic "Small Outline" Package and Standard Plastic 300-mil DIPs**

SN74BCT' . . . DW OR NT PACKAGE
(TOP VIEW)



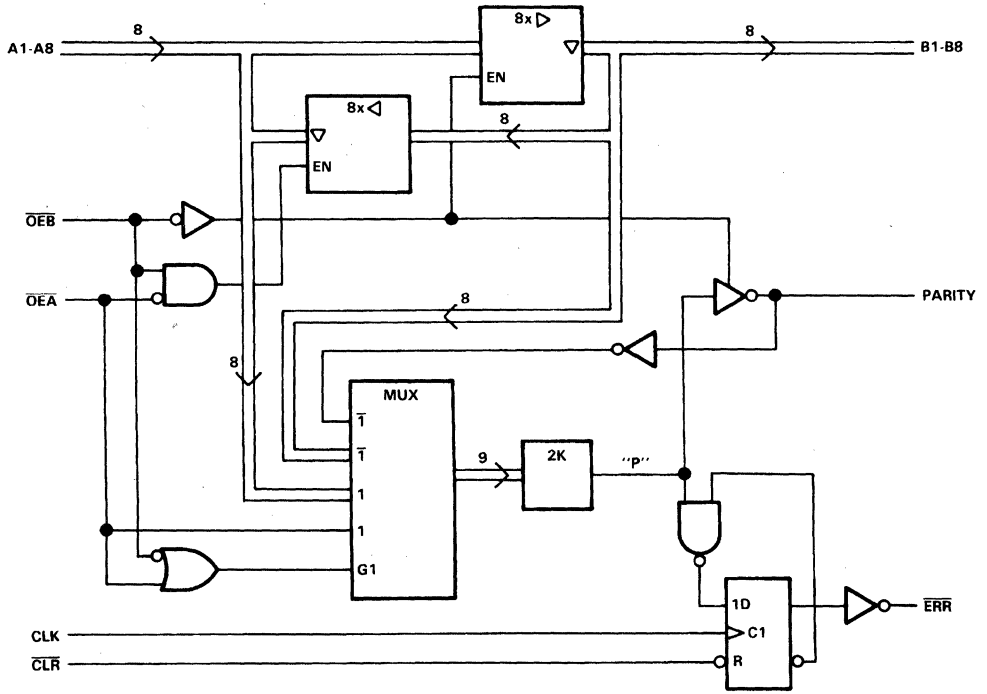
description

The SN74BCT29833 and SN74BCT29834 are 8-bit to 9-bit parity transceivers designed for two-way communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the $\overline{ERR}$ output will indicate whether or not an error in the B data has occurred. The output enable inputs $\overline{OEA}$ and $\overline{OEB}$ can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd output (PARITY) and monitors the parity of the I/O ports with an open-collector parity error flag ($\overline{ERR}$). $\overline{ERR}$ is clocked into the register on the rising edge of the CLK input. The error flag register is cleared with a low pulse on the $\overline{CLR}$ input. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The SN74BCT29833 and SN74BCT29834 are characterized for operation from 0°C to 70°C.

logic diagram (positive logic)

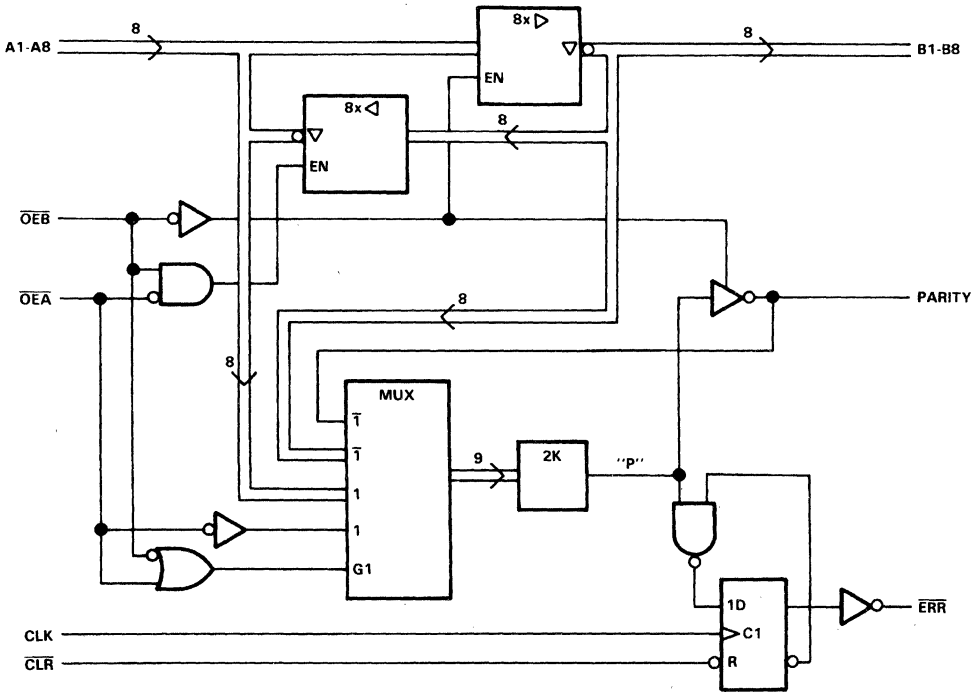


FUNCTION TABLE

INPUTS						OUTPUT & I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	CLK	Ai Σ of H's	Bi† Σ of H's	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A Data to B Bus and Generate Parity
H	L	H	↑	NA	Odd Even	B	NA	NA	H L	B Data to A Bus and Check Parity
X	X	L	X	X	X	X	NA	NA	H	Clear Error Flag Register
H	H	H L H H	No ↑ No ↑ ↑ ↑	X X Odd Even	X	Z	Z	Z	NC H H L	Isolation§
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A Data to B Bus and Generate Inverted Parity

NA = Not applicable, NC = No change, X = Don't care
†Summation of high-level inputs includes PARITY along with Bi inputs.
‡Output states shown assume the $\overline{ERR}$ output was previously high.
§In this mode, the $\overline{ERR}$ output, when clocked, shows inverted parity of the A bus.

logic diagram (positive logic)



FUNCTION TABLE

INPUTS						OUTPUT & I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	CLK	Ai Σ of H's	Bi† Σ of L's	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	$\overline{A}$	H L	NA	$\overline{A}$ Data to B Bus and Generate Parity
H	L	H	↑	NA	Odd Even	$\overline{B}$	NA	NA	H L	$\overline{B}$ Data to A Bus and Check Parity
X	X	L	X	X	X	X	NA	NA	H	Clear Error Flag Register
H	H	H L H H	No ↑ No ↑ ↑ ↑	X X Odd Even	X	Z	Z	Z	NC H L H	Isolation§
L	L	X	X	Odd Even	NA	NA	$\overline{A}$	L H	NA	$\overline{A}$ Data to B Bus and Generate Inverted Parity

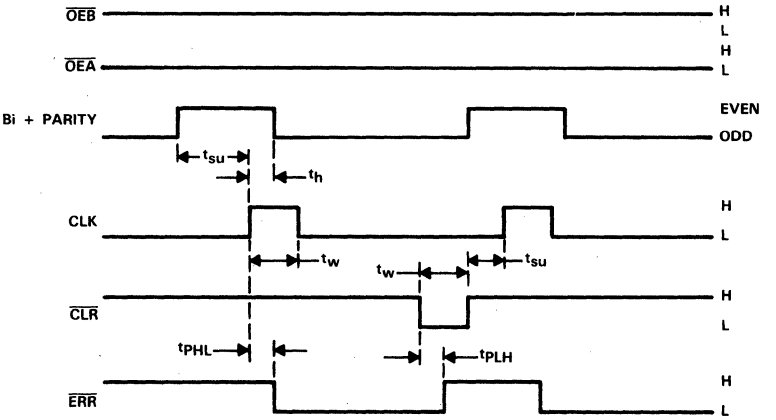
NA = Not applicable, NC = No change, X = Don't care

†Summation of low-level inputs includes PARITY along with Bi inputs.

‡Output states shown assume the $\overline{ERR}$ output was previously high.

§In this mode, the $\overline{ERR}$ output, when clocked, shows noninverted parity of the A bus.

error flag waveforms



ERROR FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT	FUNCTION
$\overline{CLR}$	CLK	POINT "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	
H	↑	H	H	H	SAMPLE
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	CLEAR

$\overline{ERR}_{n-1}$ represents the state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, CLK, or point "P".

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage ..... 7 V
Voltage applied to a disabled I/O port ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage, $\overline{ERR}$				2.4	V
I_{OH}	High-level output current				−24	mA
I_{OL}	Low-level output current				48	mA
t_w	Pulse duration	CLK high	10			ns
		CLK low	10			
		$\overline{CLR}$ low	10			
t_{su}	Setup time before CLK ↑	Bi and PARITY	12			ns
		$\overline{CLR}$ inactive	12			
t_h	Hold time, Bi and PARITY after CLK ↑		0			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	All inputs/outputs except $\overline{ERR}$	V_{CC} = 4.5 V	I_{OH} = −15 mA	2.4			V
			I_{OH} = −24 mA	2			
I_{OH}	$\overline{ERR}$	V_{CC} = 4.5 V,	V_{OH} = 2.4 V			20	μA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	mA
I_{IH}‡		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}‡	Data	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
	Control					−0.75	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	−75		−250	mA
I_{CCL}		V_{CC} = 5.5 V,	All Outputs Open		55	80	mA
I_{CCZ}					30	45	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed 1 second.

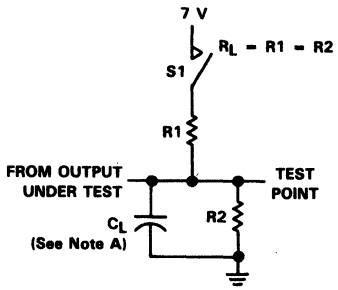
SN74BCT29833 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	5	7	1	8	ns
t_{PHL}			1.5	5	8	1.5	10	
t_{PLH}	A	PARITY	1.5	7	9	1.5	11	ns
t_{PHL}			1.5	10	13	1.5	15	
t_{PZH}	$\overline{OEA}$ or $\overline{OEB}$	A or B	2	11	15	2	19	ns
t_{PZL}			2	13	17	2	21	
t_{PHZ}	$\overline{OEA}$ or $\overline{OEB}$	A or B	2	8	11	2	15	ns
t_{PLZ}			2	10	14	2	17	
t_{PHL}	CLK	$\overline{ERR}$	1.5	7	10	1.5	12	ns
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	1.5	13	17	1.5	20	ns
t_{PLH}	$\overline{OEA}$	PARITY	1.5	10	13	1.5	15	ns
t_{PHL}			1.5	10	13	1.5	15	

SN74BCT29834 switching characteristics (see Figure 1)

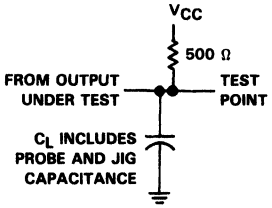
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	5	7	1	8	ns
t_{PHL}			1.5	4	6	1.5	7	
t_{PLH}	A	PARITY	1.5	10	13	1.5	15	ns
t_{PHL}			1.5	8	10	1.5	15	
t_{PZH}	$\overline{OEA}$ or $\overline{OEB}$	A or B	2	11	15	2	19	ns
t_{PZL}			2	15	19	2	21	
t_{PHZ}	$\overline{OEA}$ or $\overline{OEB}$	A or B	2	8	11	2	15	ns
t_{PLZ}			2	13	17	2	21	
t_{PHL}	CLK	$\overline{ERR}$	1.5	7	10	1.5	12	ns
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	1.5	13	17	1.5	18	ns
t_{PLH}	$\overline{OEA}$	PARITY	1.5	10	13	1.5	15	ns
t_{PHL}			1.5	10	13	1.5	15	

PARAMETER MEASUREMENT INFORMATION



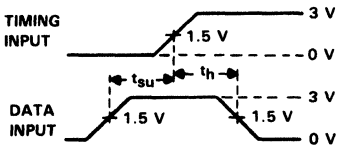
SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed

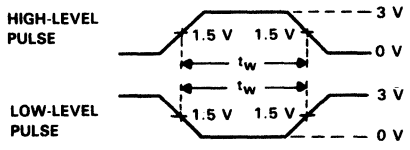


LOAD CIRCUIT 1 ALL OUTPUTS EXCEPT FOR ERROR FLAG

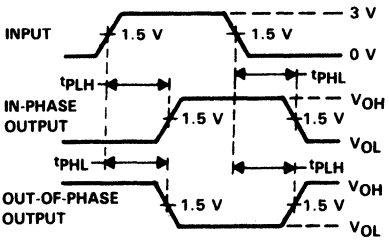
LOAD CIRCUIT 2 ERROR FLAG OUTPUT



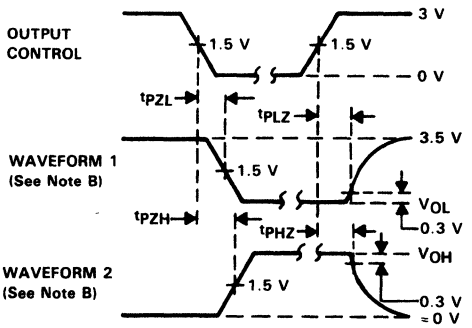
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

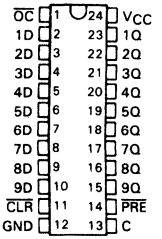
FIGURE 1

SN74BCT29843, SN74BCT29844
9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

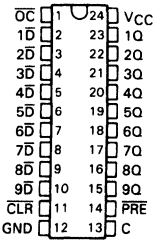
D3180, FEBRUARY 1989—REVISED JULY 1989

- **BiCMOS Process with CMOS Inputs and TTL Outputs Substantially Reduces Standby Current**
- **Input Has 50-kΩ Pullup Resistor**
- **Bus-Structured Pinout**
- **Functionally Equivalent to AMD Am29843A, Am29844A, 'ALS29843, and 'ALS29844**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Outputs Have Undershoot Protection Circuitry**
- **Power-Up High-Impedance State**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

SN74BCT29843 ... DW OR NT PACKAGE
(TOP VIEW)



SN74BCT29844 ... DW OR NT PACKAGE
(TOP VIEW)



description

These 9-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The nine latches are transparent D-type. The 'BCT29843 has noninverting data (D) inputs. The 'BCT29844 has inverting D inputs.

A buffered output control ($\overline{OC}$) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

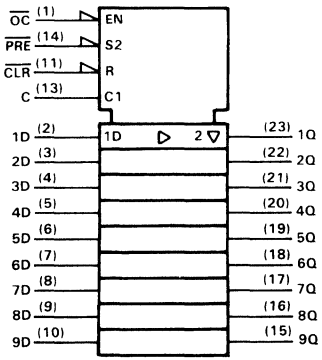
The SN74BCT29843 and SN74BCT29844 are characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

'BCT29843 FUNCTION TABLE

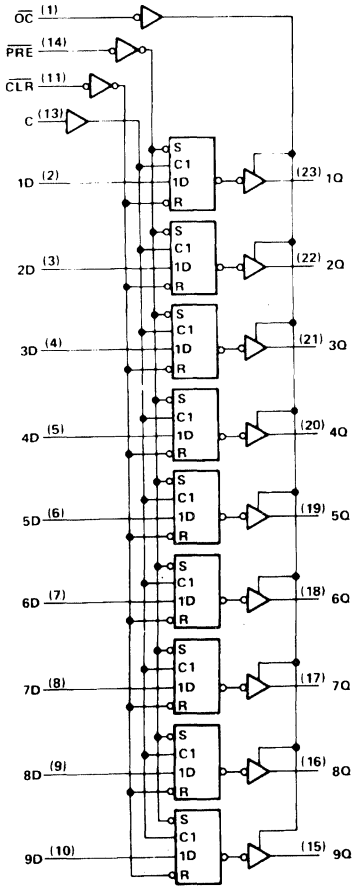
INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC}$	C	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_0
X	X	H	X	X	Z

'BCT29843 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'BCT29843 logic diagram (positive logic)

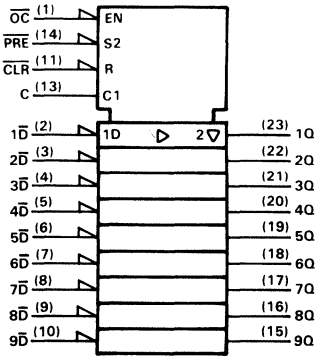


2 BiCMOS Circuits

'BCT29844 FUNCTION TABLE

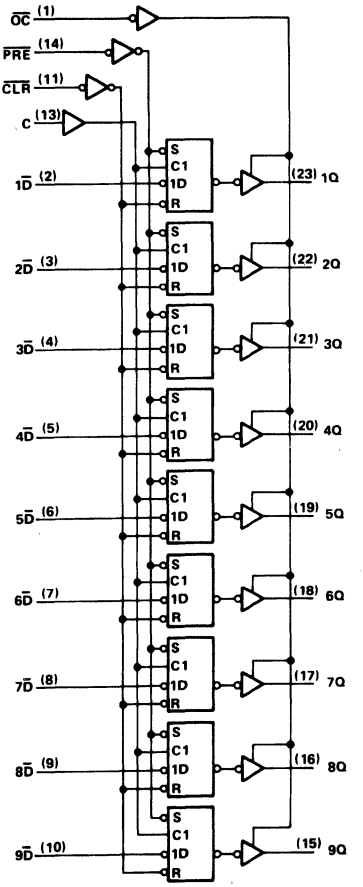
INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC}$	C	$\overline{D}$	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	H
H	H	L	H	H	L
H	H	L	L	X	Q_0
X	X	H	X	X	Z

'BCT29844 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'BCT29844 logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5		5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−24	mA
I_{OL}	Low-level output current				48	mA
t_w	Pulse duration	$\overline{PRE}$ low	7			ns
		$\overline{CLR}$ low	5			
		C high	4			
t_{su}	Setup time, before enable C ↓	Data	1.5			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive state	2			
t_h	Hold time, data after enable C ↓		3.5			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −15 mA		2.4	3.2		V
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA			0.35	0.5	V
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				20	μA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.4 V				−20	μA
I_I	V_{CC} = 5.5 V, V_I = 5.5 V				0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V		−10		−75	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.4 V				−0.2	mA
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0		−75		−275	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		3	7	mA
		Outputs low		24	35	
		Outputs disabled		3	7	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	Any Q	1.5	4.5	7	1.5	8	ns
t_{PHL}			1.5	5.7	8	1.5	9	
t_{PLH}	C	Any Q	1.5	6	8	1.5	10	ns
t_{PHL}			1.5	6	8	1.5	10	
t_{PLH}	$\overline{PRE}$	Any Q	1.5	6	10	1.5	12	ns
t_{PHL}			1.5	6	10	1.5	12	
t_{PLH}	$\overline{CLR}$	Any Q	1.5	6	10	1.5	12	ns
t_{PHL}			1.5	6	10	1.5	12	
t_{PZH}	$\overline{OC}$	Any Q	2	10	13	2	15	ns
t_{PZL}			2	10	13	2	15	
t_{PHZ}	$\overline{OC}$	Any Q	2	5	7	2	8	ns
t_{PLZ}			2	5	7	2	8	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

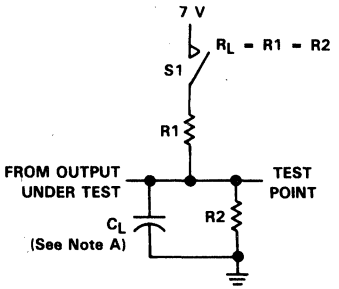
PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −15 mA		2.4	3.2		V
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA			0.35	0.5	V
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				20	μA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.4 V				−20	μA
I_I	V_{CC} = 5.5 V, V_I = 5.5 V				0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V		−10		−75	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.4 V				−0.2	mA
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0		−75		−275	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		3	7	mA
		Outputs low		24	35	
		Outputs disabled		3	7	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	Any Q	1.5	5.7	8	1.5	9	ns
t_{PHL}			1.5	4.5	7	1.5	8	
t_{PLH}	C	Any Q	1.5	6	8	1.5	10	ns
t_{PHL}			1.5	6	8	1.5	10	
t_{PLH}	$\overline{PRE}$	Any Q	1.5	6	11	1.5	12	ns
t_{PHL}			1.5	6	11	1.5	12	
t_{PLH}	$\overline{CLR}$	Any Q	1.5	6	11	1.5	12	ns
t_{PHL}			1.5	6	11	1.5	12	
t_{PZH}	$\overline{OC}$	Any Q	2	10	13	2	15	ns
t_{PZL}			2	10	13	2	15	
t_{PHZ}	$\overline{OC}$	Any Q	2	5	7	2	8	ns
t_{PLZ}			2	5	7	2	8	

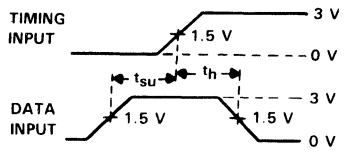
PARAMETER MEASUREMENT INFORMATION



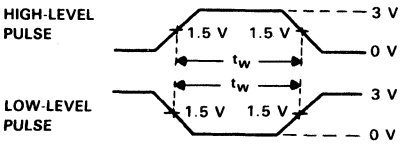
LOAD CIRCUIT

SWITCH POSITION TABLE

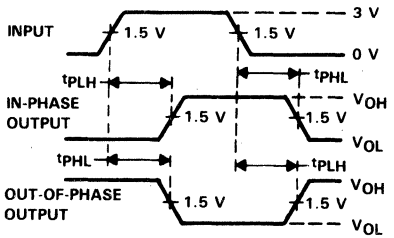
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



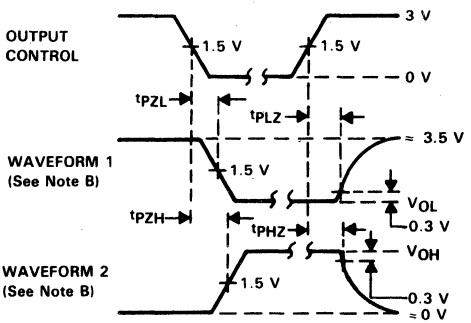
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



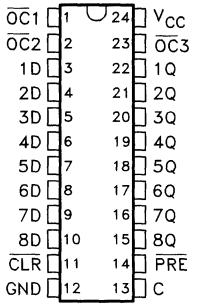
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

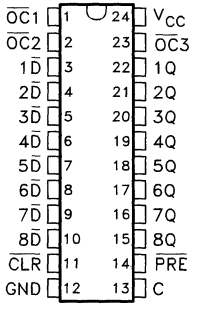
FIGURE 1. SWITCHING CHARACTERISTICS

- **BiCMOS Process with CMOS Inputs and TTL Outputs Substantially Reduces Standby Current**
- **Input Has 50-kΩ Pullup Resistor**
- **Bus-Structured Pinout**
- **Functionally Equivalent to AMD Am29845, Am29846, 'ALS29845, and 'ALS29846**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Power-Up High-Impedance State**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Package Options Include Plastic "Small Outline" Packages, Plastic Chip Carriers, and Standard Plastic 300-mil DIPs**

SN74BCT29845 ... DW OR NT PACKAGE
(TOP VIEW)



SN74BCT29846 ... DW OR NT PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type. The 'BCT29845 has noninverting data (D) inputs. The 'BCT29846 has inverting $\overline{D}$ inputs. Since $\overline{CLR}$ and $\overline{PRE}$ are independent of the clock, taking the $\overline{CLR}$ input low will cause the eight Q outputs to go low. Taking the $\overline{PRE}$ input low will cause the eight Q outputs to go high. When both $\overline{PRE}$ and $\overline{CLR}$ are taken low, the outputs will follow the preset condition.

The buffered output control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without

need for interface or pull-up components. The output controls do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74BCT29845 and SN74BCT29846 are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

'BCT29845

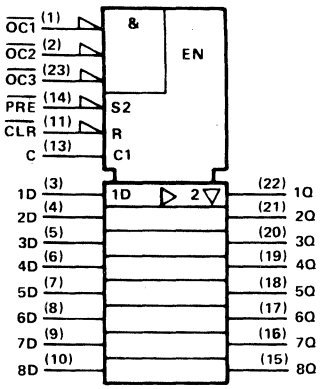
INPUTS							OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC1}$	$\overline{OC2}$	$\overline{OC3}$	C	D	Q
L	X	L	L	L	X	X	H
H	L	L	L	L	X	X	L
H	H	L	L	L	H	L	L
H	H	L	L	L	H	H	H
H	H	L	L	L	L	X	Q_0
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

'BCT29846

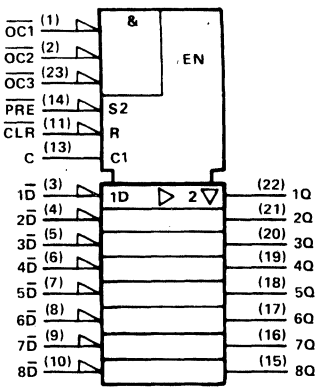
INPUTS							OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC1}$	$\overline{OC2}$	$\overline{OC3}$	C	$\overline{D}$	Q
L	X	L	L	L	X	X	H
H	L	L	L	L	X	X	L
H	H	L	L	L	H	L	H
H	H	L	L	L	H	H	L
H	H	L	L	L	L	X	Q_0
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

logic symbols†

'BCT29845



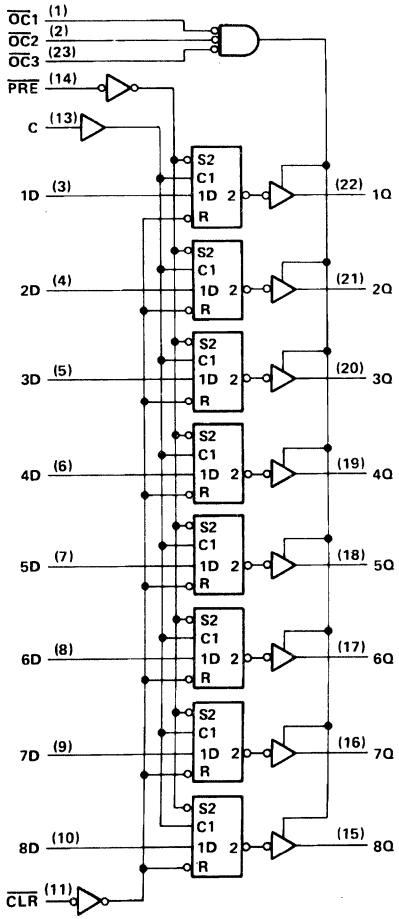
'BCT29846



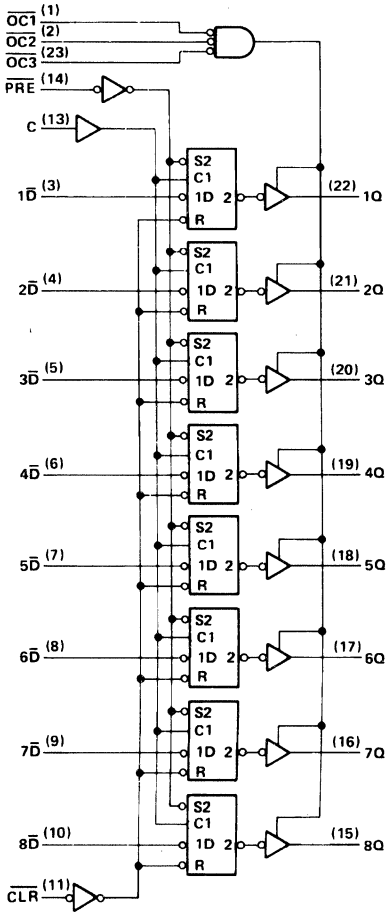
† These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

'BCT29845



'BCT29846



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... −0°C to 70°C
Storage temperature range ..... −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5		5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−24	mA
I_{OL}	Low-level output current				48	mA
t_w	Pulse duration	$\overline{PRE}$ low	7			ns
		$\overline{CLR}$ low	5			
		C high	4			
t_{su}	Setup time, before enable C ↓	Data	1.5			ns
		$\overline{PRE}$ or $\overline{CLR}$, inactive state	2			
t_h	Hold time, data after enable C ↓		3.5			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −15 mA		2.4	3.2		V
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA			0.35	0.5	V
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				20	μA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.4 V				−20	μA
I_I	V_{CC} = 5.5 V, V_I = 5.5 V				0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V		−10		−75	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.4 V				−0.2	mA
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0		−75		−275	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		3	7	mA
		Outputs low		24	35	
		Outputs disabled		3	7	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	Any Q	1.5	4.5	7	1.5	8	ns
t_{PHL}			1.5	5.7	8	1.5	9	
t_{PLH}	C	Any Q	1.5	6	8	1.5	10	ns
t_{PHL}			1.5	6	8	1.5	10	
t_{PLH}	$\overline{PRE}$	Any Q	1.5	6	11	1.5	12	ns
t_{PHL}			1.5	6	11	1.5	12	
t_{PLH}	$\overline{CLR}$	Any Q	1.5	6	11	1.5	12	ns
t_{PHL}			1.5	6	11	1.5	12	
t_{PZH}	$\overline{OC}$	Any Q	2	10	13	2	15	ns
t_{PZL}			2	10	13	2	15	
t_{PHZ}	$\overline{OC}$	Any Q	2	5	7	2	8	ns
t_{PLZ}			2	5	7	2	8	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

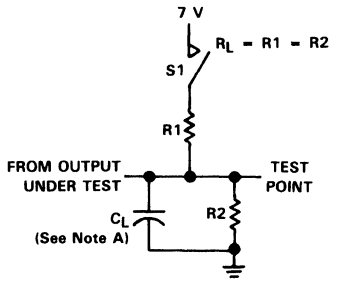
PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −15 mA		2.4	3.2		V
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA			0.35	0.5	V
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				20	μA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.4 V				−20	μA
I_I	V_{CC} = 5.5 V, V_I = 5.5 V				0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V		−10		−75	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.4 V				−0.2	mA
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0		−75		−275	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		3	7	mA
		Outputs low		24	35	
		Outputs disabled		3	7	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	Any Q	1.5	5.7	8	1.5	9	ns
t_{PHL}			1.5	4.5	7	1.5	8	
t_{PLH}	C	Any Q	1.5	6	8	1.5	10	ns
t_{PHL}			1.5	6	8	1.5	10	
t_{PLH}	$\overline{PRE}$	Any Q	1.5	6	11	1.5	12	ns
t_{PHL}			1.5	6	11	1.5	12	
t_{PLH}	$\overline{CLR}$	Any Q	1.5	6	11	1.5	12	ns
t_{PHL}			1.5	6	11	1.5	12	
t_{PZH}	$\overline{OC}$	Any Q	2	10	13	2	15	ns
t_{PZL}			2	10	13	2	15	
t_{PHZ}	$\overline{OC}$	Any Q	2	6	8	2	10	ns
t_{PLZ}			2	6	8	2	10	

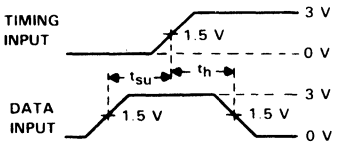
PARAMETER MEASUREMENT INFORMATION



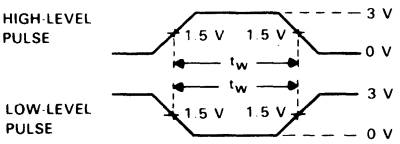
LOAD CIRCUIT

SWITCH POSITION TABLE

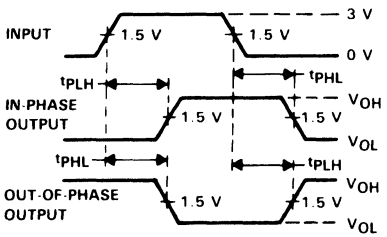
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



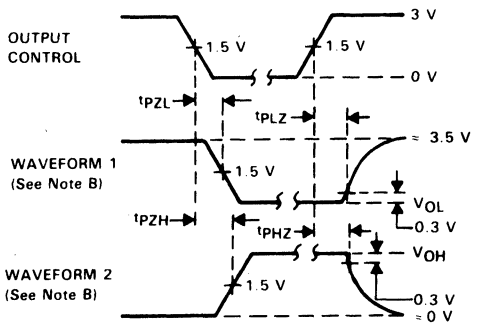
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by the generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

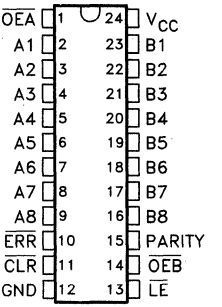
FIGURE 1. SWITCHING CHARACTERISTICS

SN74BCT29853, SN74BCT29854
8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

D3031, SEPTEMBER 1987—REVISED JULY 1989

- **BiCMOS Process with TTL Inputs and Outputs**
- **BiCMOS Design Reduces Standby Current**
- **Flow-Through Pinout (All Inputs on Opposite Side from Outputs)**
- **Functionally Equivalent to AMD Am29853 and Am29854**
- **High-Speed Bus Transceivers with Parity Generator/Checker**
- **Parity Error Flag with Open-Collector Output**
- **Choice of True ('BCT29853) or Inverting ('BCT29854) Logic**
- **Has a Latch for Storage of the Parity Error Flag**
- **Package Options Include Plastic "Small Outline" Package, Plastic Chip Carriers, and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN74BCT' ... DW OR NT PACKAGE
(TOP VIEW)



description

The SN74BCT29853 and SN74BCT29854 are 8-bit to 9-bit parity transceivers designed for two-way communication between data buses. When data is transmitted from the A to B bus, a parity bit is generated. When data is transmitted from the B to A bus with its corresponding parity bit, the $\overline{ERR}$ output will indicate whether or not an error in the B data has occurred. The output enable inputs $\overline{OEA}$ and $\overline{OEB}$ can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd output (PARITY), and monitors the parity of the I/O ports with an open-collector parity error flag ($\overline{ERR}$). $\overline{ERR}$ can be either passed, sampled, stored, or cleared from the latch using the $\overline{LE}$ and $\overline{CLR}$ control inputs. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The SN74BCT29853 and SN74BCT29854 are characterized for operation from 0°C to 70°C.

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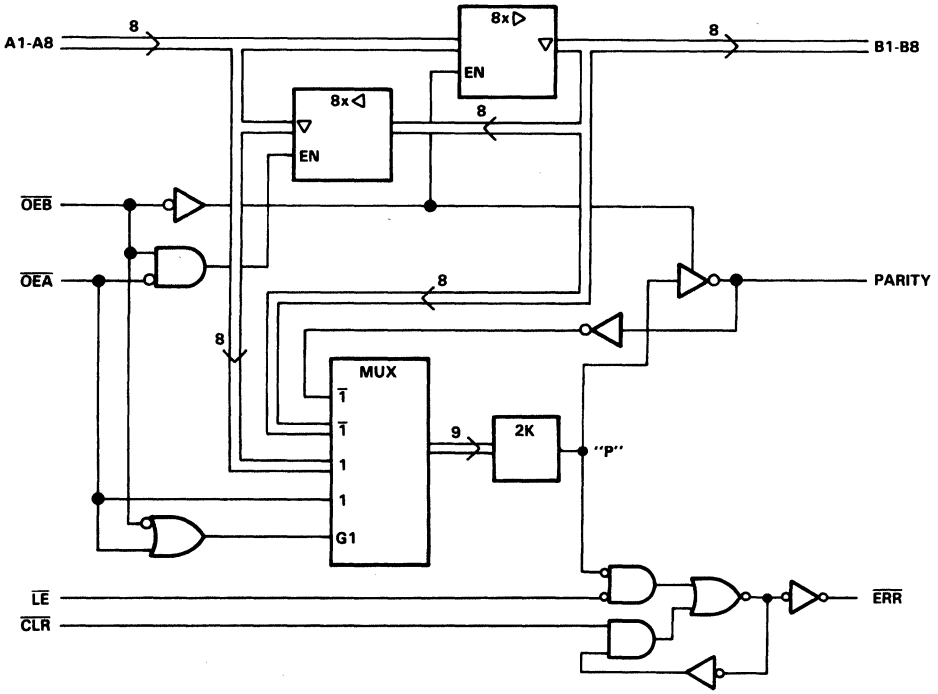
logic diagram (positive logic)

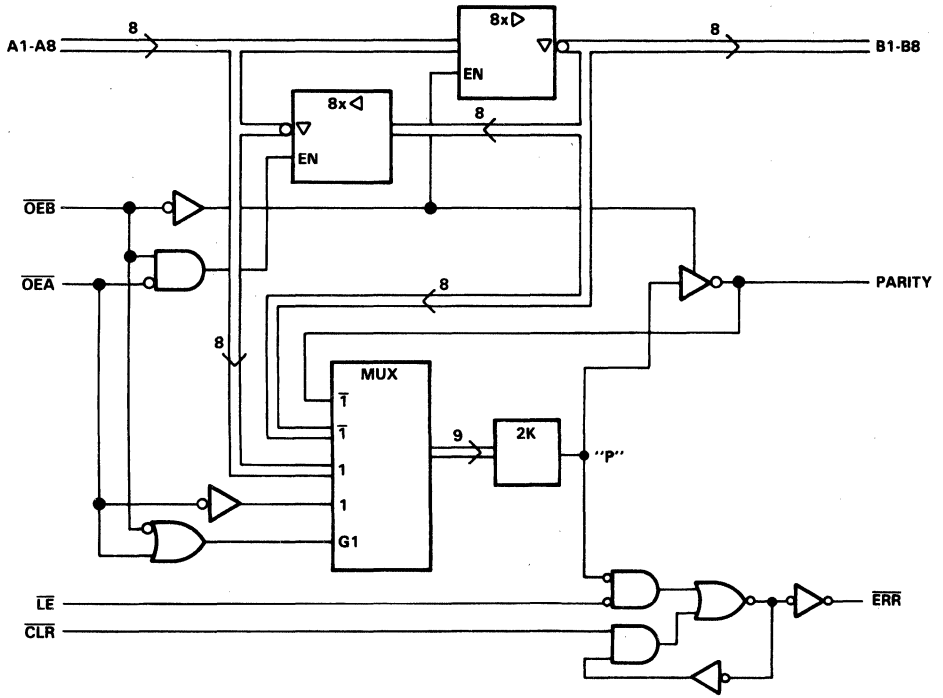


FUNCTION TABLE

INPUTS						OUTPUT & I/O				
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	$\overline{LE}$	Ai Σ of H's	Bi† Σ of H's	A	B	PARITY	$\overline{ERR}$‡	FUNCTION
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A Data to B Bus and Generate Parity
H	L	X	L	NA	Odd Even	B	NA	NA	H L	B Data to A Bus and Check Parity
H	L	H	H	NA	X	X	NA	NA	N-1	Store Error Flag
X	X	L	H	X	X	X	NA	NA	H	Clear Error Flag Register
H	H	H L X X	H H L L	X X L Odd H Even	X	Z	Z	Z	NC H H L	Isolation§ (Parity Check)
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A Data to B Bus and Generate Inverted Parity

NA = Not applicable, NC = No change, X = Don't care
†Summation of high-level inputs includes PARITY along with Bi inputs.
‡Output states shown assume the $\overline{ERR}$ output was previously high.
§In this mode the $\overline{ERR}$ output, when enabled, shows inverted parity of the A bus.

logic diagram (positive logic)



FUNCTION TABLE

INPUTS						OUTPUT & I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	$\overline{LE}$	Ai Σ of H's	Bi† Σ of L's	A	B	PARITY	$\overline{ERR}$‡	
L	H	X	X	Odd Even	NA	NA	$\overline{A}$	H L	NA	$\overline{A}$ Data to B Bus and Generate Parity
H	L	X	L	NA	Odd Even	$\overline{B}$	NA	NA	H L	$\overline{B}$ Data to A Bus and Check Parity
H	L	H	H	NA	X	X	NA	NA	N-1	Store Error Flag
X	X	L	H	X	X	X	NA	NA	H	Clear Error Flag Register
H	H	H L X X	H H L L	X X L Odd H Even	X	Z	Z	Z	NC H L H	Isolation§
L	L	X	X	Odd Even	NA	NA	$\overline{A}$	L H	NA	$\overline{A}$ Data to B Bus and Generate Inverted Parity

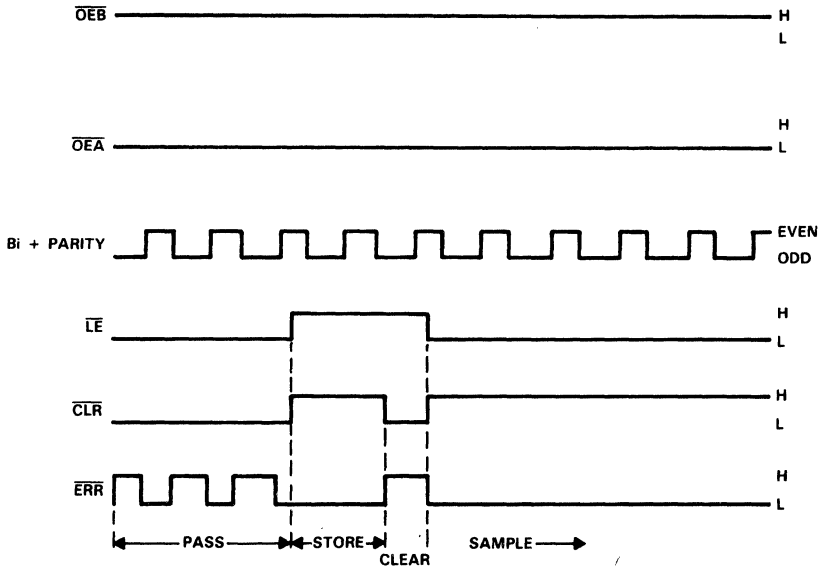
NA = Not applicable, NC = No change, X = Don't care

†Summation of low-level inputs includes PARITY along with Bi inputs.

‡Output states shown assume the $\overline{ERR}$ output was previously high.

§In this mode the $\overline{ERR}$ output, when enabled, shows noninverted parity of the A bus.

error flag waveforms



ERROR FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT	FUNCTION
$\overline{LE}$	$\overline{CLR}$	POINT "P"	$\overline{ERR}_{n-1}$†	$\overline{ERR}$	
L	L	L H	X	L H	PASS
L	H	L X H	X L H	L L H	SAMPLE
H	L	X	X	H	CLEAR
H	H	X	L H	L H	STORE

†$\overline{ERR}_{n-1}$ represents the state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, $\overline{LE}$ or point P.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage ..... 7 V
Voltage applied to a disabled I/O port ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage, $\overline{ERR}$				2.4	V
I_{OH}	High-level output current				−24	mA
I_{OL}	Low-level output current				48	mA
t_w	Pulse duration	$\overline{LE}$ low	10			ns
		$\overline{CLR}$ low	10			
t_{su}	Setup time before $\overline{LE}\downarrow$	Bi and PARITY	12			ns
t_h	Hold time, Bi and PARITY after $\overline{LE}\downarrow$		3			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	All inputs/outputs except $\overline{ERR}$	V_{CC} = 4.5 V	I_{OH} = −15 mA	2.4			V
			I_{OH} = −24 mA	2			
I_{OH}	$\overline{ERR}$	V_{CC} = 4.5 V,	V_{OH} = 2.4 V			20	μA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	mA
I_{IH}‡		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}‡	Data	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
	Control					−0.75	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	−75		−250	mA
ICCL		V_{CC} = 5.5 V,	All outputs open		55	80	mA
I_{CCZ}					30	45	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ These parameters include off-state output current for I/O ports only.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed 1 second.

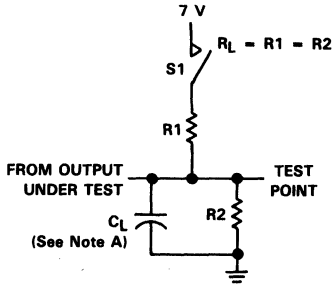
SN74BCT29853 switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	5	7	1	10	ns
t_{PHL}			1	5	7	1	10	
t_{PLH}	A	PARITY	1.5	10	13	1.5	15	ns
t_{PHL}			1.5	10	13	1.5	15	
t_{PZH}	$\overline{OEA}$ or $\overline{OEB}$	A or B	2	13	16	2	20	ns
t_{PZL}			2	13	16	2	20	
t_{PHZ}	$\overline{OEA}$ or $\overline{OEB}$	A or B	2	13	16	2	20	ns
t_{PLZ}			2	13	16	2	20	
t_{PHL}	$\overline{LE}$	$\overline{ERR}$	1.5	5	7	1.5	9	ns
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	1.5	11	14	1.5	15	ns
t_{PLH}	$\overline{OEA}$	PARITY	1.5	10	13	1.5	15	ns
t_{PHL}			1.5	10	13	1.5	15	
t_{PLH}	Bi/PARITY	$\overline{ERR}$	1.5	17	22	1.5	24	ns
t_{PHL}			1.5	10	13	1.5	16	

SN74BCT29854 switching characteristics (see Figure 1)

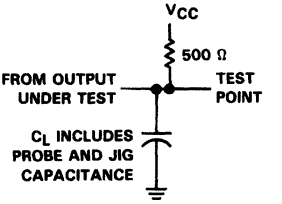
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	5	7	1	8	ns
t_{PHL}			1	5	7	1	8	
t_{PLH}	A	PARITY	1.5	10	13	1.5	15	ns
t_{PHL}			1.5	10	13	1.5	15	
t_{PZH}	$\overline{OEA}$ or $\overline{OEB}$	A or B	2	12	15	2	17	ns
t_{PZL}			2	13	16	2	19	
t_{PHZ}	$\overline{OEA}$ or $\overline{OEB}$	A or B	2	8	11	2	15	ns
t_{PLZ}			2	10	14	2	17	
t_{PHL}	$\overline{LE}$	$\overline{ERR}$	1.5	5	7	1.5	9	ns
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	1.5	11	13	1.5	15	ns
t_{PLH}	$\overline{OEA}$	PARITY	1.5	10	13	1.5	15	ns
t_{PHL}			1.5	10	13	1.5	16	
t_{PLH}	Bi/PARITY	$\overline{ERR}$	1.5	15	18	1.5	20	ns
t_{PHL}			1.5	10	13	1.5	15	

PARAMETER MEASUREMENT INFORMATION

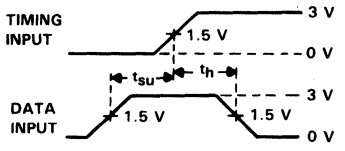


SWITCH POSITION TABLE

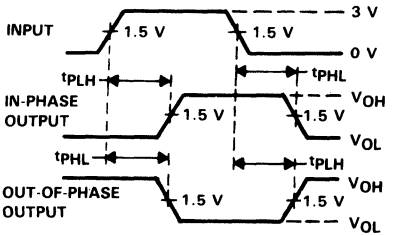
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



LOAD CIRCUIT 1 ALL OUTPUTS EXCEPT FOR ERROR FLAG

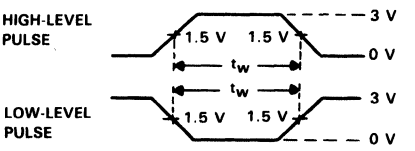


VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

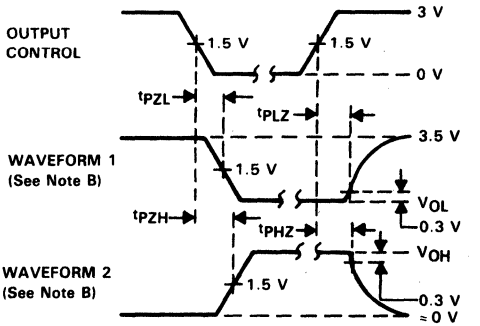


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

LOAD CIRCUIT 2 ERROR FLAG OUTPUT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

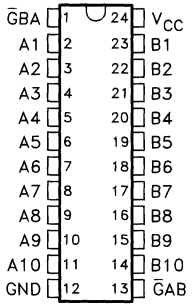
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1

D3161, NOVEMBER 1988—REVISED JULY 1989

- **BiCMOS Design Substantially Reduces Standby Current**
- **Functionally Equivalent to Am29861A, Am29862A, 'ALS29861, and 'ALS29862**
- **Choice of True ('BCT29861A) or Inverting ('BCT29862A) Logic**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DW OR NT PACKAGE
(TOP VIEW)



description

These 10-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs ($\overline{G}BA$ and $\overline{G}AB$).

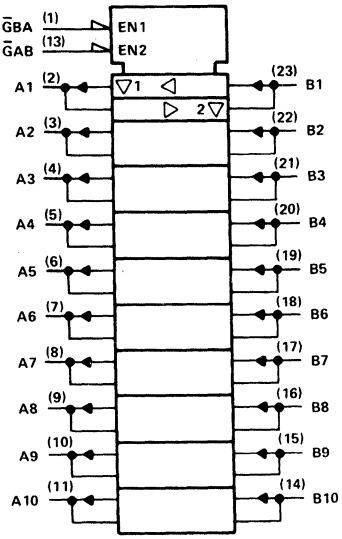
The outputs are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down.

The SN74BCT29861A and SN74BCT29862A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

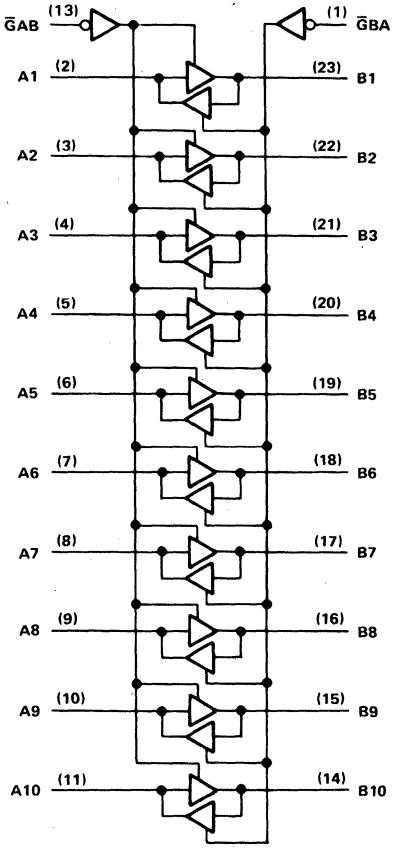
INPUTS		OPERATION	
$\overline{G}AB$	$\overline{G}BA$	'BCT29861A	'BCT29862A
L	H	A to B	$\overline{A}$ to B
H	L	B to A	$\overline{B}$ to A
H	H	Isolation	Isolation
L	L	Latch A and B (A = B)	Latch A and B (A = $\overline{B}$)

logic symbol†

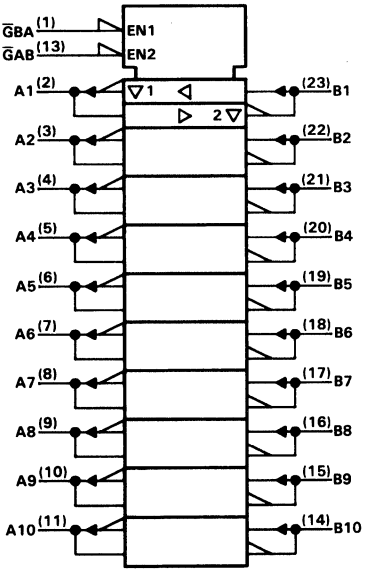


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

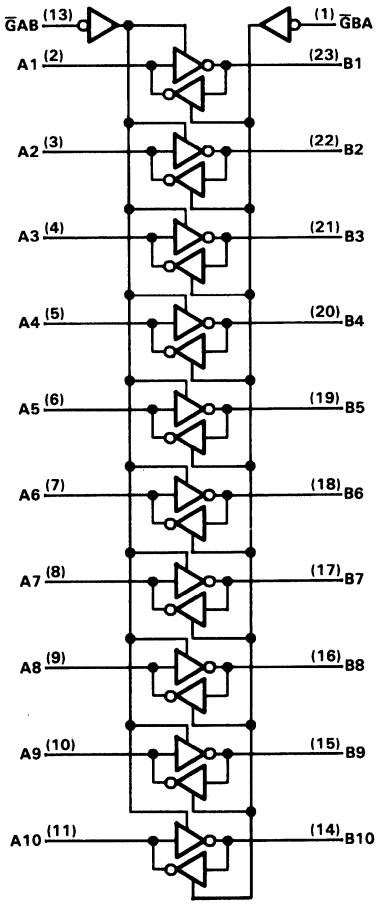


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage (all inputs and I/O ports) ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}		V_{CC} = 4.5 V	I_{OH} = −15 mA		2.4			V
			I_{OH} = −24 mA		2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				0.1	mA
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V				20	µA
	A or B port‡						20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V				−0.2	mA
	A or B port‡						−0.2	
$I_{O(off)}$§		V_{CC} = 0,	V_O = 2.9 V				0.1	mA
I_{OS}¶		V_{CC} = 5.5 V,	V_O = 0		−75		−250	mA
I_{CC}		V_{CC} = 5.5 V,		Outputs high		18	30	mA
				Outputs low		30	45	
				Outputs disabled		6.5	12	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the offstate output current.
§ $I_{O(off)}$ = Power-off bus leakage current.
¶ Not more than one output should be shorted at a time and duration of the short circuit should not exceed 1 second.

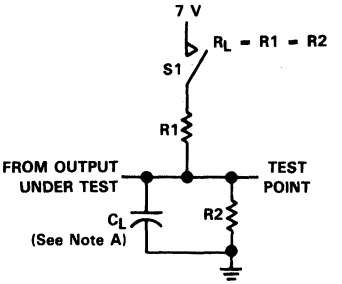
SN74BCT29861A switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	5	7	1	8	ns
t_{PHL}			1.5	5	7	1	8	
t_{PZH}	$\overline{G}AB$ or $\overline{G}BA$	A or B	2	7	10	2	11	ns
t_{PZL}			2	9	12	2	13	
t_{PHZ}	$\overline{G}AB$ or $\overline{G}BA$	A or B	2	6	9	2	10	ns
t_{PLZ}			2	6	9	2	10	

SN74BCT29862A switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	5	8	1	9	ns
t_{PHL}			1.5	5	7	1	8	
t_{PZH}	$\overline{G}AB$ or $\overline{G}BA$	A or B	2	7	10	2	11	ns
t_{PZL}			2	9	12	2	13	
t_{PHZ}	$\overline{G}AB$ or $\overline{G}BA$	A or B	2	6	9	2	10	ns
t_{PLZ}			2	6	9	2	10	

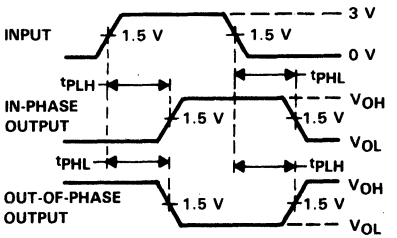
PARAMETER MEASUREMENT INFORMATION



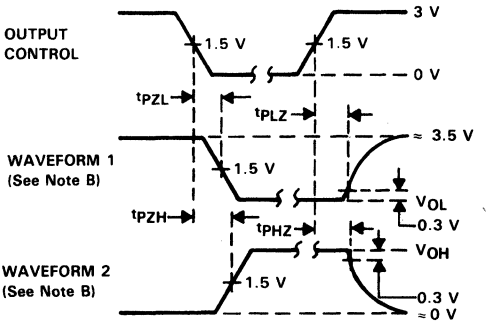
LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

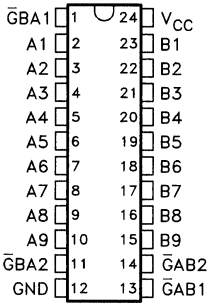
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by the generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1. SWITCHING CHARACTERISTICS

D3162, NOVEMBER 1988—REVISED FEBRUARY 1989

- **BiCMOS Design Substantially Reduces Standby Current**
- **Functionally Equivalent to Am29863A, Am29864A, 'ALS29863, and 'ALS29864**
- **Choice of True ('BCT29863A) or Inverting ('BCT29864A) Logic**
- **Power-Up High-Impedance State**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DW OR NT PACKAGE
(TOP VIEW)



description

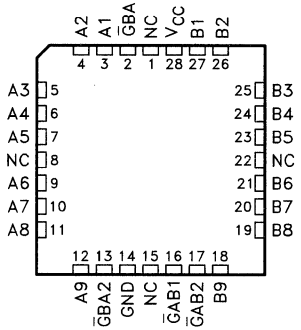
These 9-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs ($\overline{G}$BA1, $\overline{G}$BA2, $\overline{G}$AB1, and $\overline{G}$AB2).

The outputs are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down.

The SN74BCT29863A and SN74BCT29864A are characterized for operation from 0°C to 70°C.

FN PACKAGE
(TOP VIEW)

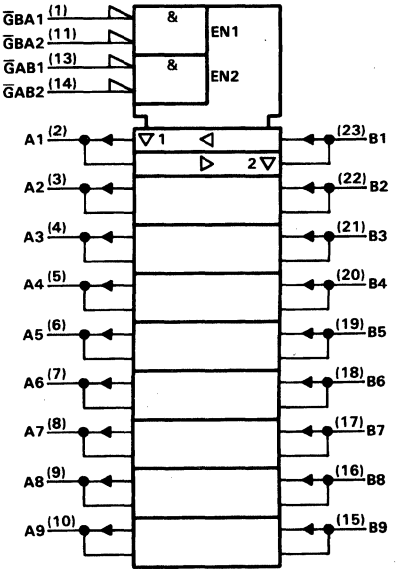


NC—No internal connection

FUNCTION TABLE

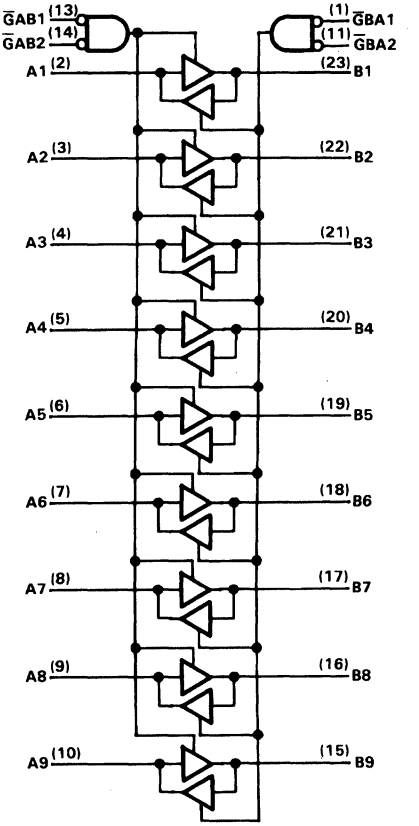
ENABLE INPUTS				OPERATION	
$\overline{G}AB1$	$\overline{G}AB2$	$\overline{G}BA1$	$\overline{G}BA2$	'BCT29863A	'BCT29864A
L	L	L	L	Latch A and B	Latch A and B
L	L	H	X	A to B	A to $\overline{B}$
L	L	X	H		
H	X	L	L	B to A	B to $\overline{A}$
X	H	L	L		
H	X	H	X	Isolation	Isolation
H	X	X	H		
X	H	X	H		
X	H	H	X		

logic symbol†

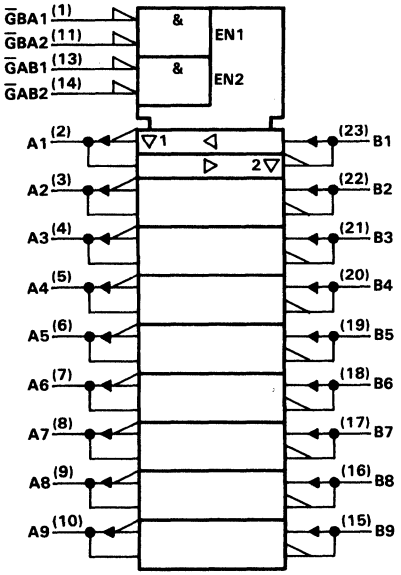


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

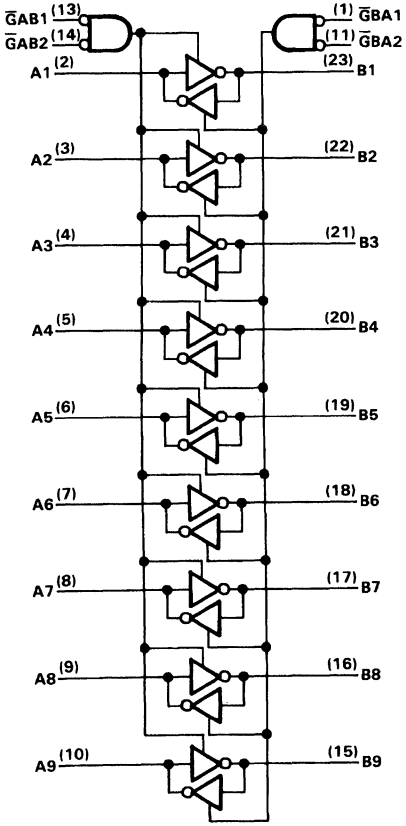


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage (all inputs and I/O ports) ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

2 BiCMOS Circuits

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}		V_{CC} = 4.5 V	I_{OH} = −15 mA		2.4			V
			I_{OH} = −24 mA		2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				0.1	mA
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V				20	μA
	A or B port‡						20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V				−0.2	mA
	A or B port‡						−0.2	
$I_{O(off)}$§		V_{CC} = 0,	V_O = 2.9 V				0.1	mA
I_{OS}¶		V_{CC} = 5.5 V,	V_O = 0		−75		−250	mA
I_{CC}		V_{CC} = 5.5 V		Outputs high		18	30	mA
				Outputs low		30	45	
				Outputs disabled		6.5	12	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ $I_{O(off)}$ = Power-off bus leakage current.
¶ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

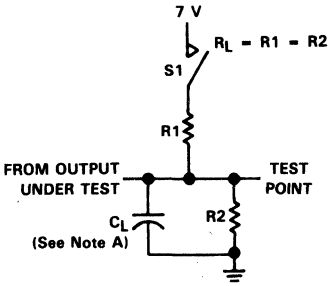
SN74BCT29863A switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	5	7	1	8	ns
t_{PHL}			1	5	7	1	8	
t_{PZH}	$\overline{G}$AB or $\overline{G}$BA	A or B	2	7	10	2	11	ns
t_{PZL}			2	9	12	2	13	
t_{PHZ}	$\overline{G}$AB or $\overline{G}$BA	A or B	2	6	9	2	10	ns
t_{PLZ}			2	6	9	2	10	

SN74BCT29864A switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	5	8	1	9	ns
t_{PHL}			1	5	7	1	8	
t_{PZH}	$\overline{G}$AB or $\overline{G}$BA	A or B	2	7	10	2	11	ns
t_{PZL}			2	9	12	2	13	
t_{PHZ}	$\overline{G}$AB or $\overline{G}$BA	A or B	2	6	9	2	10	ns
t_{PLZ}			2	6	9	2	10	

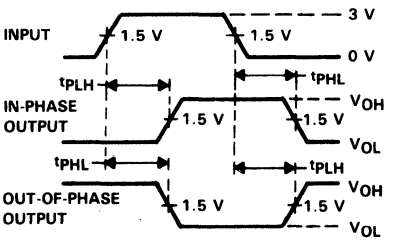
PARAMETER MEASUREMENT INFORMATION



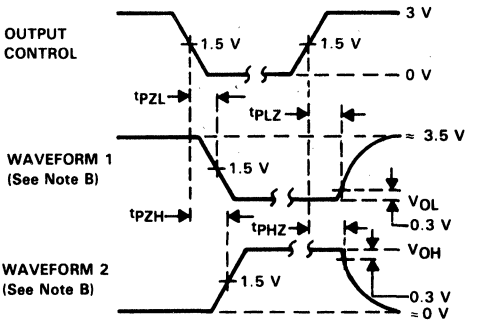
LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by the generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

FIGURE 1. SWITCHING CHARACTERISTICS

BiCMOS Circuits
Preliminary Data Sheets

TEXAS INSTRUMENTS

D3253, FEBRUARY 1989

- **State of the Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **3-State Inverting Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **High-Impedance State During Power Up and Power Down**
- **P-N-P Inputs Reduce D-C Loading**
- **Data Flow-Through Pinout (All Inputs on Opposite Side from Outputs)**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

This octal buffer and line driver is designed to have the performance of the popular SN64BCT240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR gate so that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

The outputs are in a high-impedance state during power up and power down while the supply voltage is less than approximately 3 V.

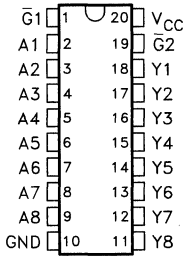
The SN64BCT540 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

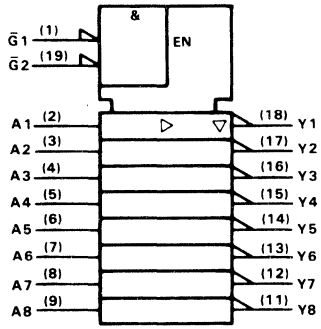
INPUTS			OUTPUT
$\overline{G}1$	$\overline{G}2$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

Z = High Impedance

SN64BCT540 ... DW OR N PACKAGE
(TOP VIEW)

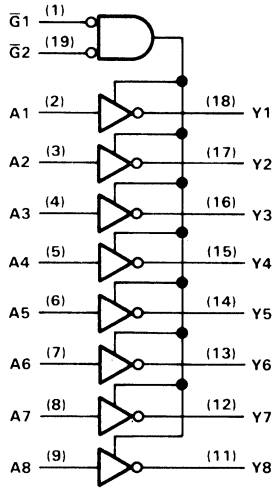


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage . . . . . −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state . . . . . 128 mA
Operating free-air temperature range . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

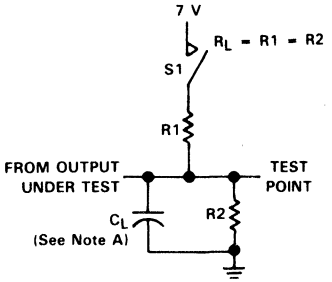
PARAMETER	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA					−1.2	V
V_{OH}	V_{CC} = 4.5 V		I_{OH} = −3 mA	2.4	3.3		V
			I_{OH} = −15 mA	2	3.1		
V_{OL}	V_{CC} = 4.5 V		I_{OL} = 64 mA		0.42	0.55	V
I_{OZH}	V_{CC} = 0 to 5.5 V, V_O = 2.7 V					50	μA
I_{OZL}	V_{CC} = 0 to 5.5 V, V_O = 0.5 V					−50	μA
I_{OZ}	$\overline{G}$ at 0.8 V, V_O = 2.7 V or 0.5 V	V_{CC} = 0 to 2.35 V (power up)				±50	μA
		V_{CC} = 2 V to 0 (power down)				±50	
I_I	V_{CC} = 5.5 V, V_I = 7 V					0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V					20	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V					−0.6	mA
I_{OS}§	V_{CC} = 5.5 V, V_O = 0			−100		−225	mA
I_{CCL}	V_{CC} = 5.5 V				45	71	mA
I_{CCH}	V_{CC} = 5.5 V				20	30	mA
I_{CCZ}	V_{CC} = 5.5 V				3	6	mA
C_i	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V				5		pF
C_o	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V				10		

switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, $R1$ = 500 Ω, $R2$ = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, $R1$ = 500 Ω, $R2$ = 500 Ω, T_A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	2.5	4.1	5.8	1.9	7.2	ns
t_{PHL}			0.6	1.9	3.5	0.3	4.5	
t_{PZH}	$\overline{G}$	Y	4.8	6.8	8.9	4.1	10.4	ns
t_{PZL}			6	8	10	5.3	11.8	
t_{PHZ}	$\overline{G}$	Y	3.5	5.7	7.8	2.7	9.4	ns
t_{PLZ}			3.8	5.5	7.4	3.5	8.9	

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

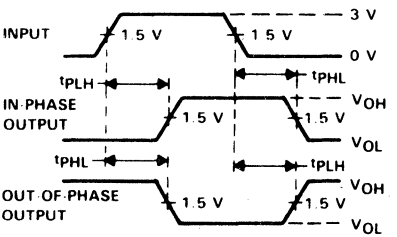
PARAMETER MEASUREMENT INFORMATION



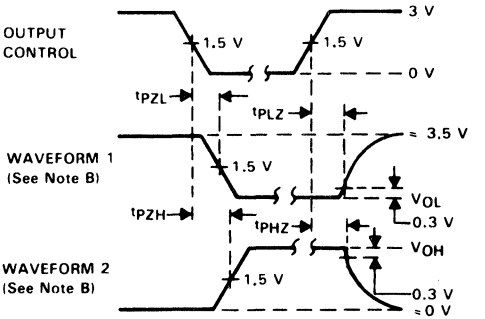
LOAD CIRCUIT

SWITCH POSITION TABLE

TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by the generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

- **3-State True Outputs**
- **Back-to-Back Registers for Storage**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Standard Plastic and Ceramic 300-mil DIPs**

description

The 'BCT544 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$ or $\overline{LEBA}$) and Output Enable ($\overline{GAB}$ or $\overline{GBA}$) inputs are provided for each register to permit independent control in either direction of data flow. For the SN54BCT544 and SN74BCT544 respectively, the A outputs are characterized to sink 20 or 24 mA while the B outputs are characterized for 48 or 64 mA. The 'BCT544 inverts data in both directions.

The A-to-B Enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. Having $\overline{CEAB}$ low and $\overline{LEAB}$ low makes the A-to-B latches transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{GAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$ inputs.

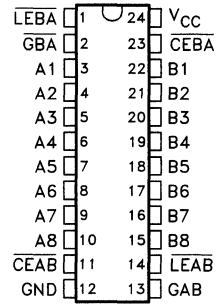
The SN54BCT544 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT544 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

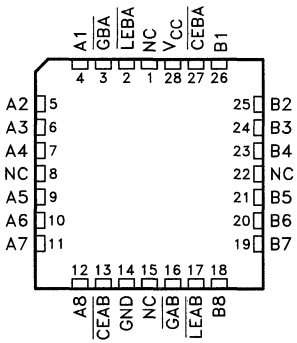
INPUTS $\overline{CEAB}$	INPUTS $\overline{LEAB}$	INPUTS $\overline{GAB}$	LATCH STATUS A to B†	OUTPUT BUFFERS B1 THRU B8
H	X	X	Storing	High Z
X	H		Storing	
X		H		High Z
L	L	L	Transparent	Current $\overline{A}$ Data
L	H	L	Storing	Previous‡ $\overline{A}$ Data

† A-to-B data flow is shown: B-to-A flow control is the same except uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{GBA}$.
‡ Before low-to-high transition of $\overline{LEAB}$.

SN54BCT544 ... JT PACKAGE
SN74BCT544 ... DW OR NT PACKAGE
(TOP VIEW)



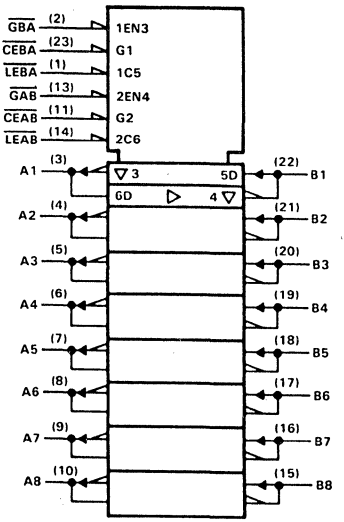
SN54BCT544 ... FK PACKAGE
(TOP VIEW)



NC—No internal connection

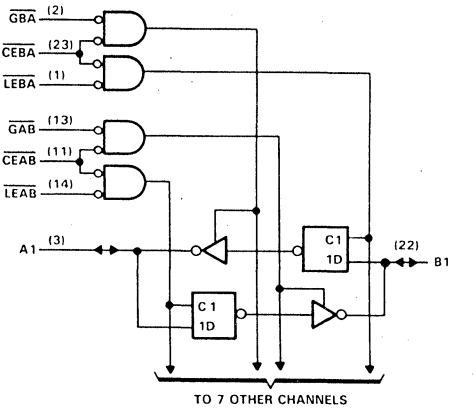
2 BiCMOS Circuits

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, (see Note 1)	−0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state	−0.5 V to 5.5 V
Voltage applied to any output in the high state	−0.5 V to V_{CC}
Input clamp current	−30 mA
Current into any output in the low state: SN54BCT544	96 mA
SN74BCT544	128 mA
Operating free-air temperature range: SN54BCT544	−55°C to 125°C
SN74BCT544	0°C to 70°C
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative voltage rating may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN54BCT544			SN74BCT544			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT544			SN74BCT544			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
		I_{OH} = −12 mA	2	3.2					
		I_{OH} = −15 mA				2	3.1		
V_{OH}	V_{CC} = 4.5 V	I_{OH} = 48 mA		0.38	0.55				V
		I_{OL} = 64 mA					0.42	0.55	
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50			50	μA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50			−50	μA
I_I	V_{CC} = 5.5 V, V_I = 7 V				0.6			0.6	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V				−0.6			−0.6	mA
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0		−100		−225	−100		−225	mA
I_{CCL}	V_{CC} = 5.5 V								mA
I_{CCH}	V_{CC} = 5.5 V								mA
I_{CCZ}	V_{CC} = 5.5 V								mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

timing requirements

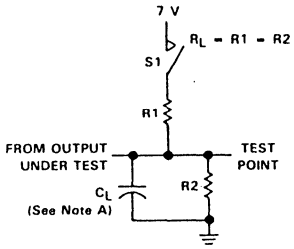
			V_{CC} = 5 V, T_A = 25°C		V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
			'BCT544		SN54BCT544		SN74BCT544		
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{su}	Setup time, data before latch enable	High or low							ns
t_h	Hold time, data after latch enable	High or low							ns

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX*				UNIT
			'BCT544			SN54BCT544		SN74BCT544		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A								ns
t_{PHL}										
t_{PLH}	$\overline{LEBA}$	A								ns
t_{PHL}										
t_{PLH}	$\overline{LEAB}$	B								ns
t_{PHL}										
t_{PZH}	$\overline{G}$ or $\overline{CE}$	A or B								ns
t_{PZL}										
t_{PHZ}	$\overline{G}$ or $\overline{CE}$	A or B								ns
t_{PLZ}										

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

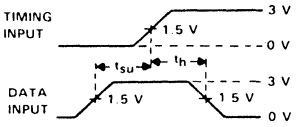
PARAMETER MEASUREMENT INFORMATION



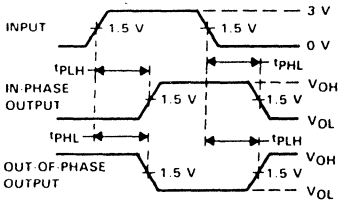
LOAD CIRCUIT

SWITCH POSITION TABLE

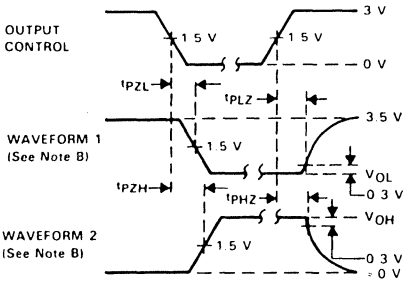
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by the generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

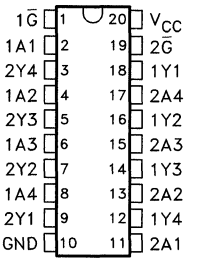
FIGURE 1. SWITCHING CHARACTERISTICS

SN54BCT756, SN74BCT756
OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

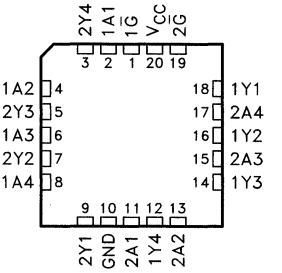
JULY 1989

- **Open-Collector Version of BCT240**
- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds 2000 V per MIL-STD-833C Method 3015**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54BCT756 ... J PACKAGE
SN74BCT756 ... DW OR N PACKAGE
(TOP VIEW)



SN54BCT756 ... FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for 3-state overlap protection. Taken together with the BCT757 and the BCT760, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low input control) inputs, and complimentary G and $\overline{G}$ inputs.

The SN54BCT756 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT756 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

OUTPUT CONTROL	DATA INPUT	OUTPUT
$1\overline{G}$, $2\overline{G}$	A	Y
L	H	L
L	L	H
H	X	Z

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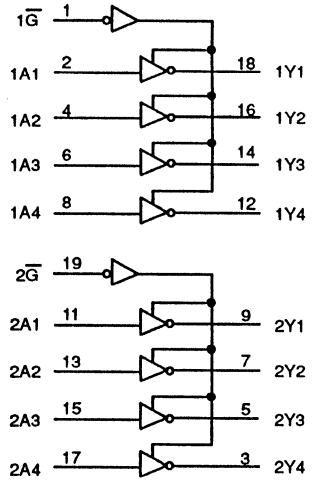
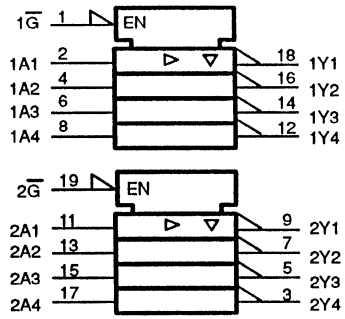
logic diagram (positive logic)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.5 V to 7 V
Input voltage, V_I (see Note 1)	−0.5 V to 7 V
Input current, I_I	−30 mA to 5 mA
Voltage applied to any output in the high state	−0.5 V to 5.5 V
Current into any output in the low state: SN54BCT756	96 mA
SN74BCT756	128 mA
Operating free-air temperature range: SN54BCT756	−55°C to 125°C
SN74BCT756	0°C to 70°C
Storage temperature range	−55°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input negative-voltage ratings may be exceeded if the input clamp current rating is observed.

recommended operating conditions

		SN54BCT756			SN74BCT756			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT756			SN74BCT756			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
I_{OH}	V_{CC} = 4.5 V, V_{OH} = 5.5 V				0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA			0.38	0.55				V
	V_{CC} = 4.5 V, I_{OL} = 64 mA						0.42	0.55	
I_I	V_{CC} = 5.5 V, V_I = 5.5 V				0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V				−1			−1	mA
I_{CC}	V_{CC} = 5.5 V, Outputs open	Outputs high		21	33		21	33	μA
		Outputs low		48	76		48	76	
C_i	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			6			6		pF
C_o	V_{CC} = 5 V, V_I = 2.5 V or 0.5 V			10			10		pF

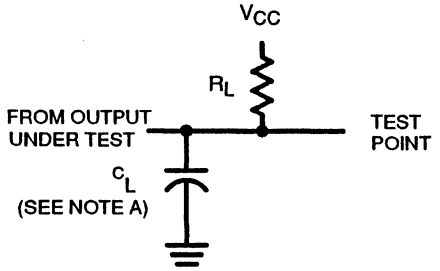
† All typical values are at V_{CC} = 5 V, T_A = 25°C.

'BCT756 switching characteristics (see Figure 1)

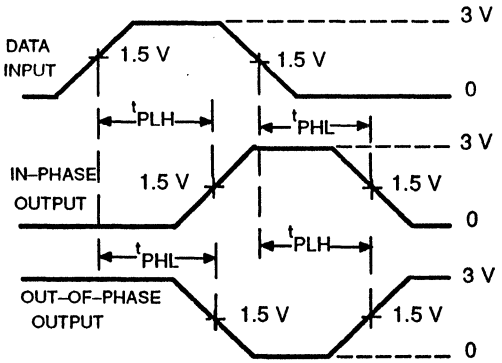
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX‡				UNIT
			'BCT756			SN54BCT756		SN74BCT756		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any A	Y		8						ns
t_{PHL}				4.3						
t_{PLH}	Any $\overline{G}$	Y		13						ns
t_{PHL}				6.2						

‡ For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one input transition per measurement.

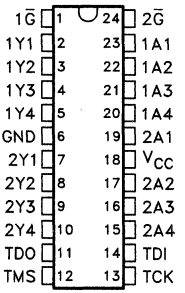
FIGURE 1. SWITCHING CHARACTERISTICS

SN54BCT8244, SN74BCT8244
SCAN TEST DEVICE WITH OCTAL BUFFER

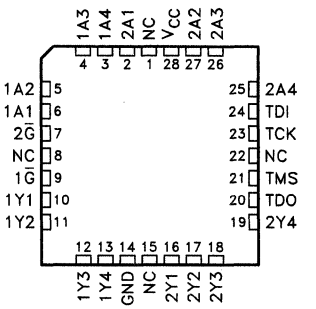
AUGUST 1989

- **Device is a member of Texas Instruments SCOPE™ Family of Testability Products**
- **Octal Test Integrated Circuit**
- **Compatible with the Proposed IEEE P1149.1 Serial Test Bus**
- **Functionally Equivalent to 54/74F244 and 54/74BCT244 in the Normal Function Mode**
- **Implements Optional "Test Reset" Signal on TAP by Recognizing a Double-High on TMS Pin**
- **Test Operation Synchronous to Test Access Port (TAP)**
- **16 Test Instructions—Conforms to the Proposed JTAG Boundary Scan—Provides Data Compression of Inputs—Provides Pseudo-Random Pattern Generation from Outputs—Output Toggle Boundary Mode—Outputs to High Impedance State Mode**
- **Package Options Include "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300 mil DIPs**

SN54BCT8244 ... JT PACKAGE
SN74BCT8244 ... DW OR NT PACKAGE
(TOP VIEW)



SN54BCT8244 ... FK PACKAGE
(TOP VIEW)



description

The SN54BCT8244 and SN74BCT8244 are members of Texas Instruments SCOPE™ testability IC family. This family of components blend test circuitry with standard logic functions to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire Test Access Port (TAP) interface.

In normal mode these devices are functionally equivalent to the SN54/74F244 and SN54/74BCT244 octal buffers. In normal mode the test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE octal buffers.

In test mode the normal operation of the SCOPE octal buffer is inhibited and the test circuitry is enabled to observe and control the device's I/O boundary. When enabled, the test circuitry can perform boundary scan test operations as described in the proposed JTAG/P1149.1 specification. Additionally, the test circuitry can perform other testing functions such as: parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

The SN54BCT8244 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT8244 is characterized for operation from 0°C to 70°C.

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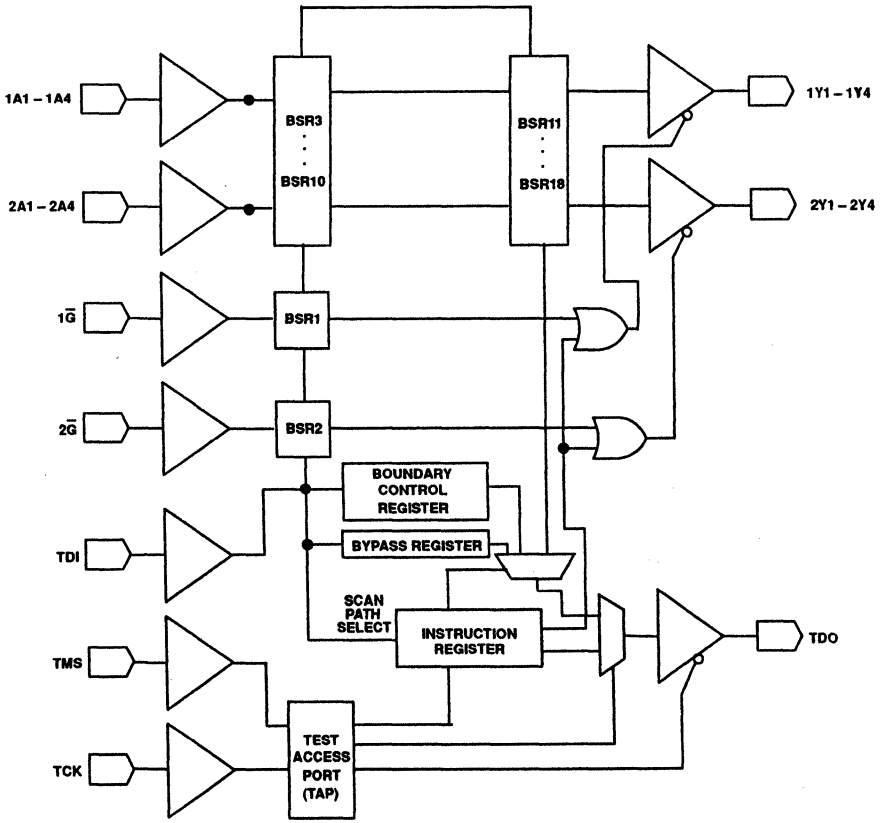
functional block diagram



FUNCTION TABLE

OUTPUT CONTROL	DATA INPUT	OUTPUT
1$\overline{G}$, 2$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state: SN54BCT8244 ..... 96 mA
SN74BCT8244 ..... 128 mA
Operating free-air temperature range: SN54BCT8244 ..... −55°C to 125°C
SN74BCT8244 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54BCT8244			SN74BCT8244			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IHH}	Double high-level input voltage	TMS	10.25	10.50	10.75	10.25	10.50	10.75	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				48			64	mA
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT8244			SN74BCT8244			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −3 mA		2.4	3.3		2.4	3.3		V
	V_{CC} = 4.5 V, I_{OH} = −12 mA		2	3.2					V
	V_{CC} = 4.5 V, I_{OH} = −15 mA					2	3.1		V
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA			0.38	0.55				V
	V_{CC} = 4.5 V, I_{OL} = 64 mA						0.42	0.55	V
I_I	V_{CC} = 5.5 V, V_I = 5.5V				0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
I_{IHH}	TMS	V_{CC} = 5.5V, V_I = 10.50 V			1			1	mA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.5 V				−1			−1	mA
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				50			50	μA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.5 V				−50			−50	μA
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0		−100		−225	−100		−225	mA
I_{CC}	V_{CC} = 5.5 V, Outputs open	Outputs high		5.5			5.5		mA
		Outputs low		52			52		mA
		Outputs disabled		2.3			2.3		mA
C_i	V_{CC} = 5.0 V, V_I = 2.5 V or 0.5 V								pF
C_o	V_{CC} = 5.0 V, V_O = 2.5 V or 0.5 V								pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

'BCT8244 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT8244			SN54BCT8244		SN74BCT8244		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK			20						MHz
t_{PLH}	ANY A	Y		5.9						ns
t_{PHL}	ANY A	Y		6.5						ns
t_{PLH}	TCK ↓	Y		11.5						ns
t_{PHL}	TCK ↓	Y		11						ns
t_{PLH}	TCK ↓	TDO		9.8						ns
t_{PHL}	TCK ↓	TDO		9.7						ns
t_{PZH}	ANY $\overline{G}$	Y		5.5						ns
t_{PZH}	TCK ↓	Y		13						ns
t_{PZH}	TCK ↓	TDO		8						ns
t_{PZL}	ANY $\overline{G}$	Y		7.7						ns
t_{PZL}	TCK ↓	Y		14						ns
t_{PZL}	TCK ↓	TDO		9.2						ns
t_{PHZ}	ANY $\overline{G}$	Y		7						ns
t_{PHZ}	TCK ↓	Y		13						ns
t_{PHZ}	TCK ↓	TDO		7						ns
t_{PLZ}	ANY $\overline{G}$	Y		6.7						ns
t_{PLZ}	TCK ↓	Y		13						ns
t_{PLZ}	TCK ↓	TDO		7.8						ns

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

NOTE 1: See General Information for load circuits and waveforms.

timing requirements (see Note 1)

		V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
		'BCT8244			SN54BCT8244		SN74BCT8244		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{clock}	TCK	0							MHz
t_w	Pulse duration TCK high or low								ns
t_{su}	Setup time, TMS before TCK ↑	9							ns
t_{su}	Setup time, TDI before TCK ↑	9							ns
t_{su}	Setup time, Any A before TCK ↑	9							ns
t_{su}	Setup time, Any $\overline{G}$ before TCK ↑	9							ns
t_h	Hold time, TMS after TCK ↑	5							ns
t_h	Hold time, TDI after TCK ↑	5							ns
t_h	Hold time, Any A after TCK ↑	5							ns
t_h	Hold time, Any $\overline{G}$ after TCK ↑	5							ns
t_{pu}	Wait time, power-up to TCK ↑	100							ns

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

NOTE 1: See General Information for load circuits and waveforms.

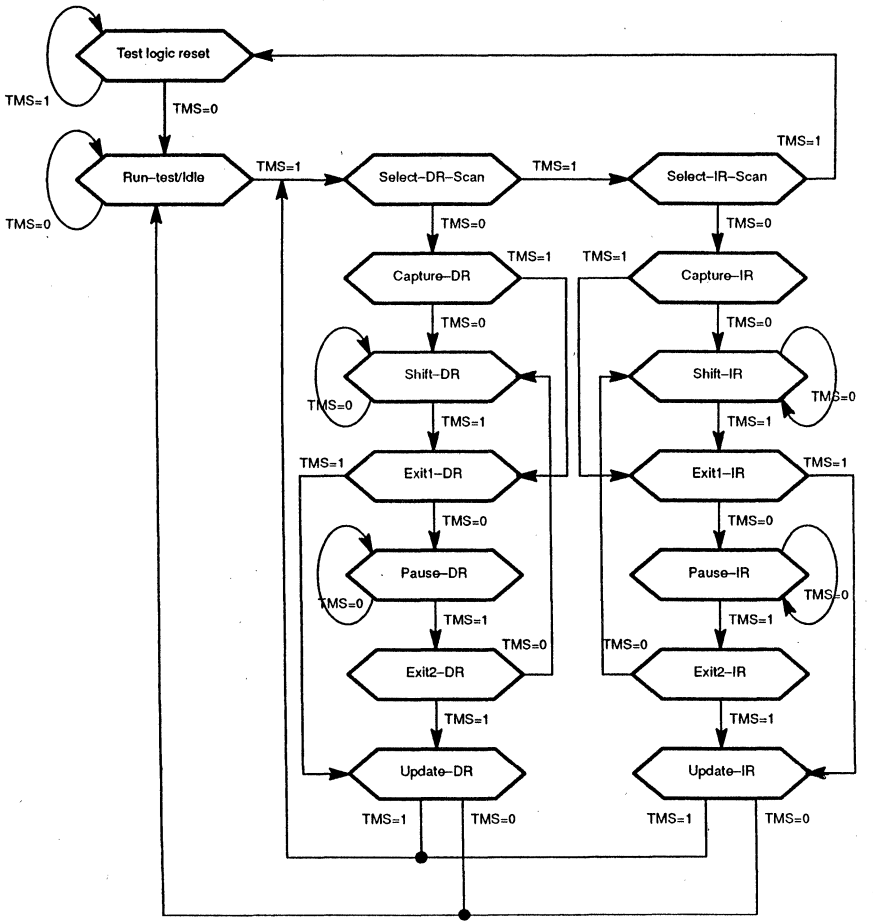


FIGURE 1. TAP STATE DIAGRAM

functional description

JTAG test information is conveyed by means of a 4-wire test bus. Test commands, test data, circuit state control instructions and synchronous control signals are all passed along the 4-wire bus. The function of the TAP is to extract the state control information and synchronous control signals from the 4-wire test bus, and generate the appropriate on-chip control signals for the JTAG test structures on the device. To accomplish this, the TAP cell monitors two signals from the 4-wire test bus—TCK (the JTAG Test Clock) and TMS (the JTAG Test Mode Select line). The functional block diagram on page 2 illustrates the JTAG 4-wire test bus and boundary scan architecture, and the relationship between the TAP cell, the 4-wire bus, and the various boundary scan test elements.

architectural elements

boundary scan register BSR0–BSR17

The boundary scan register contains eighteen (18) bits—one for each functional input or output pin of the device. FIGURE 2 illustrates the order of bits in the boundary scan register scan path. The boundary scan registers allow for board interconnect testing, defining conditions at the device logic periphery, and sampling data on the functional input or output pins without disturbing normal device operations.

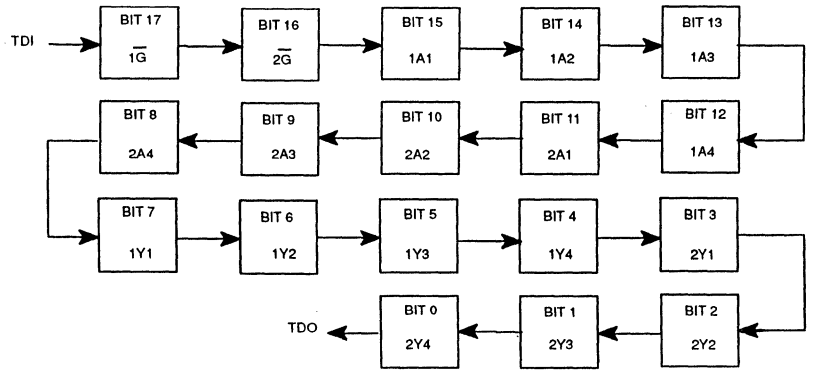


FIGURE 2. BOUNDARY SCAN REGISTER ORDER OF SCAN

bypass register

The bypass register contains one (1) bit for use when the device is in the bypass scan mode as defined in TABLE 3. FIGURE 3 illustrates the flow through the bypass register. This register provides a short one bit scan path through the device rather than scanning through the eighteen bit boundary scan register path. This is especially useful for decreasing test access times to a particular device on a board with several JTAG compatible devices which are not required for a specific test.

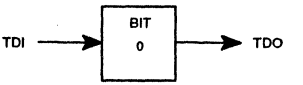


FIGURE 3. BYPASS REGISTER ORDER OF SCAN

test data register

The test data register contains two (2) bits used to control test operations occurring at the boundary. FIGURE 4 illustrates the order of bits in the test data register scan path.

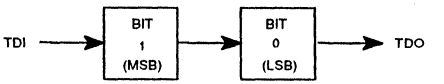


FIGURE 4. TEST DATA REGISTER ORDER OF SCAN

In addition to the boundary test instructions shown in TABLE 3, additional test operations shown in TABLE 1 can be performed when the run test opcode is installed in the instruction register. These test operations include: pseudo-random pattern generation (PRPG) and parallel signature analysis (PSA) as shown in TABLE 1 when the run test opcode is installed in the instruction register.

TABLE 1. RUN TEST OPCODES

OPCODE MSB → LSB	TEST
00	SAMPLE INPUTS/TOGGLE OUTPUTS
01	PRPG/16-BIT MODE
10	PSA/16-BIT MODE
11	SIMULTANEOUS PRPG AND PSA/8 BIT MODE

example

In order to implement the sample inputs/toggle outputs opcode from TABLE 1, a series of operations must be performed. Refer to FIGURE 1 to trace these operations through the TAP state diagram. The select-IR path is used to shift opcodes into the instruction register. The select-DR path is used to shift data into the boundary scan register or bypass register, or to shift opcodes into the test data register. To shift data or opcodes into the registers, after entering the appropriate shift-DR or shift-IR state TMS must be held low for enough TCK pulses to shift the correct number of bits into the registers.

First, the boundary read opcode (test or normal mode) must be loaded into the instruction register using the select-IR scan path, then the boundary scan registers may be initialized using the select-DR scan path. Load the test data register scan opcode (test or normal mode) into the instruction register using the select-IR scan path, then the sample inputs/toggle outputs opcode (00) may be entered into the test data register using the select-DR-scan path. Finally, the boundary run test opcode (test or normal mode) must be entered into the instruction register using the select-IR scan path. Exiting the select-IR-scan path to the run-test/idle state starts the outputs toggling. As long as the device remains in the run-test/idle state, each TCK pulse will cause the device's function outputs to toggle to the opposite state.

tap bits

Tap bit settings used for PSA and PRPG test operations are shown in TABLE 2. The use of these tap bits as well as the shift operations necessary to perform 8-bit and 16-bit PSA and PRPG test operations is described in FIGURE 5 through FIGURE 7.

TABLE 2. TAP BIT SETTINGS FOR PSA AND PRPG TEST OPERATIONS

OPERATION	MODE	TAP BITS A → Y
PSA	8-BIT	1A2, 1A3, 1A4, 2A4
	16-BIT	2A3, 1Y1, 1Y4, 2Y4
PRPG	8-BIT	1Y2, 1Y3, 1Y4, 2Y4
	16-BIT	2A3, 1Y1, 1Y4, 2Y4

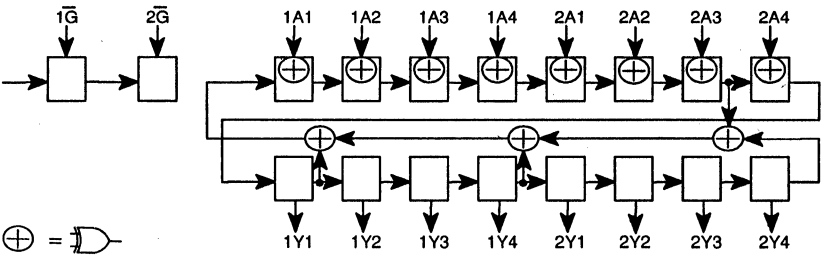


FIGURE 5. 16 BIT PSA CONFIGURATION DURING RUN TEST/IDLE STATE

A PSA operation on the 8 data inputs proceeds as the 8 data outputs are held static.

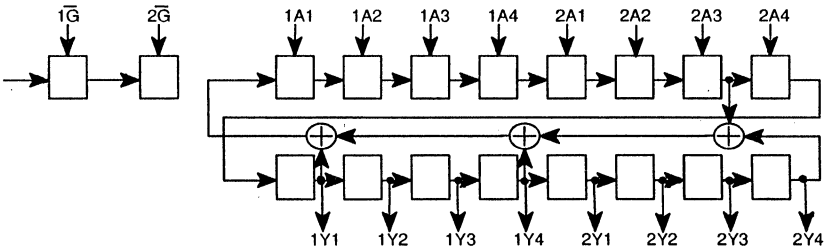


FIGURE 6. 16 BIT PRPG CONFIGURATION DURING RUN TEST/IDLE STATE

A PRPG operation from the 8 data outputs proceeds while the 8 data inputs are ignored.

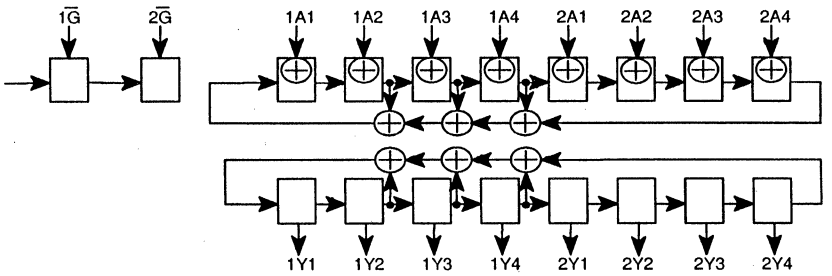


FIGURE 7. 8 BIT PSA AND PRPG CONFIGURATION DURING RUN TEST/IDLE STATE

Simultaneously, an 8 bit PSA operation proceeds on the 8 data inputs, while an 8 bit PRPG operation proceeds from the 8 data outputs.

instruction register

The test device instruction register is 8 bits in length. When in the Shift-IR state, data can be scanned into the register from the most significant bit (MSB) to the least significant bit (LSB) as shown in FIGURE 8. The instruction register controls the internal device structures and test operations according to the opcodes listed in TABLE 3.

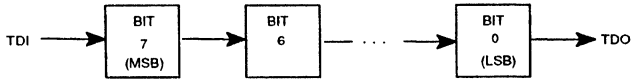


FIGURE 8. INSTRUCTION REGISTER ORDER OF SCAN

instruction set

The 'BCT8244 uses the 8-bit serial instruction register as its instruction input. TABLE 3 summarizes the 8-bit opcodes and corresponding tests.

TABLE 3. OPCODES (see Note 1)

OPCODE BIT 7–BIT 0 MSB-LSB	FUNCTION
X0000000	BOUNDARY SCAN
X0000001	ID REGISTER SCAN
X0000010	SAMPLE BOUNDARY
X0000011	BOUNDARY SCAN
X0000100	BYPASS SCAN MODE
X0000101	BYPASS SCAN MODE
X0000110	CONTROL BOUNDARY TO HIGH IMPEDANCE
X0000111	CONTROL BOUNDARY TO 1/0
X0001000	BYPASS SCAN MODE
X0001001	BOUNDARY RUN TEST/TEST MODE
X0001010	BOUNDARY READ/NORMAL MODE
X0001011	BOUNDARY READ/TEST MODE
X0001100	BOUNDARY SELF TEST/NORMAL MODE
X0001101	BOUNDARY TOGGLE OUTPUTS/TEST MODE
X0001110	TEST DATA REGISTER SCAN/NORMAL MODE
X0001111	TEST DATA REGISTER SCAN/TEST MODE
ALL OTHER	BYPASS SCAN MODE

X = Parity Bit (Even Parity)
NOTE 1: If Bit 4 through Bit 6 are all 0, then Bit 0 through Bit 3 are decoded as shown in TABLE 3.

The test functions which are identified in TABLE 3 and performed by the test integrated circuits are defined as follows:

boundary scan

A boundary scan of the boundary scan register is performed according to the methodology designated by the proposed JTAG or the proposed IEEE P1149.1 specifications. This instruction performs a combination of sample boundary and control boundary to 1/0 tests as specified below.

ID register scan

The test circuit is placed in the bypass mode as defined by JTAG in the absence of an ID Register. A logic 0 is loaded into the bypass register before scanning.

sample boundary

Data appearing at the device's function inputs and outputs is sampled and scanned out the TDO pin. This operation is performed in a functional mode without disturbing normal device operations.

control boundary to high impedance

The device's function outputs are placed in the high impedance state. The bypass register is selected in the scan path. Function inputs remain operational.

control boundary to 1/0

Function inputs and outputs are controlled by the boundary register. The bypass register is selected in the scan path.

boundary run test

Test operations controlled by the test data register are performed while the device is in the idle mode. Operations performed in this mode include the following:

parallel signature analysis of inputs

Data appearing on the device's data inputs is compressed by a parallel signature analysis (PSA) operation with fixed tap bits. Data shall be compressed into sixteen bits. The initial seed value for the PSA operation should be scanned into the boundary scan register prior to performing the test operation.

pseudo-random pattern generation from outputs

A pseudo-random data pattern (PRPG) is output from the outputs of the test device. The initial seed value for the PRPG should be scanned into the data register prior to performing the test operation.

simultaneous PSA and PRPG

An 8 Bit PSA of inputs and an 8 Bit PRPG from outputs is performed simultaneously as specified above.

sample inputs/toggle outputs

The devices inputs are sampled on successive rising edges of TCK, while the device's function output pins are toggled simultaneously on successive falling edges of TCK while the device is in the idle mode. This test is intended to be used for parametric testing and pattern generation purposes. The initial pattern should be scanned into the boundary scan register prior to performing the test operation.

boundary read (test mode and normal mode)

Data is scanned in and out of the boundary scan register without first preloading the boundary condition. This function is particularly useful after a PSA operation—the results can be scanned out for review by the test controller.

test data register scan (test mode and normal mode)

The test data register is selected for scan access.

boundary self test

The boundary scan register is preloaded with the inverted contents of the latch memory elements of each boundary scan register bit. The boundary scan register is then scanned out. Prior to performing this test known data should be scanned into the boundary scan register.

boundary toggle outputs

The device's function output pins are toggled simultaneously on successive TCK clock inputs. This test is intended to be used for parametric testing and pattern generation purposes. The initial pattern should be scanned into the data register prior to performing the test operation.

bypass scan mode

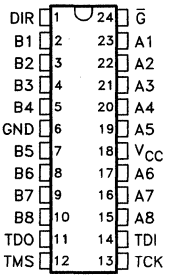
The bypass register is selected in the scan path and the device is placed in the normal mode.

SN54BCT8245, SN74BCT8245
SCAN TEST DEVICE WITH OCTAL TRANSCEIVERS

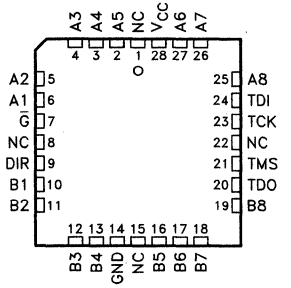
MAY 1989

- **Device is a member of Texas Instruments SCOPE™ Family of Testability Products**
- **Octal Test Integrated Circuit**
- **Compatible with the Proposed IEEE P1149.1 Serial Test Bus**
- **Functionally Equivalent to 54/74F245 and 54/74BCT245 in the Normal Function Mode**
- **Implements Optional "Test Reset" Signal on TAP by Recognizing a Double-High on TMS Pin**
- **Test Operation Synchronous to Test Access Port (TAP)**
- **16 Test Instructions—Conforms to the Proposed JTAG Boundary Scan—Provides Data Compression of Inputs—Provides Pseudo-Random Pattern Generation from Outputs—Output Toggle Boundary Mode—Outputs to High Impedance State Mode**
- **Package Options Include "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300 mil DIPs**

SN54BCT8245 ... JT PACKAGE
SN74BCT8245 ... DW OR NT PACKAGE
(TOP VIEW)



SN54BCT8245 ... FK PACKAGE
(TOP VIEW)



description

The SN54BCT8245 and SN74BCT8245 are members of Texas Instruments SCOPE™ testability IC family. This family of components blend test circuitry with standard logic functions to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire Test Access Port (TAP) interface. In normal mode these devices are functionally equivalent to the SN54/74F245 and SN54/74BCT245 octal transceivers. In normal mode the test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in normal mode does not affect the functional operation of the SCOPE octal buffers.

In test mode the normal operation of the SCOPE octal buffer is inhibited and the test circuitry is enabled to observe and control the device's I/O boundary. When enabled, the test circuitry can perform boundary scan test operations as described in the proposed JTAG/P1149.1 specification. Additionally, the test circuitry can perform other testing functions such as: parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

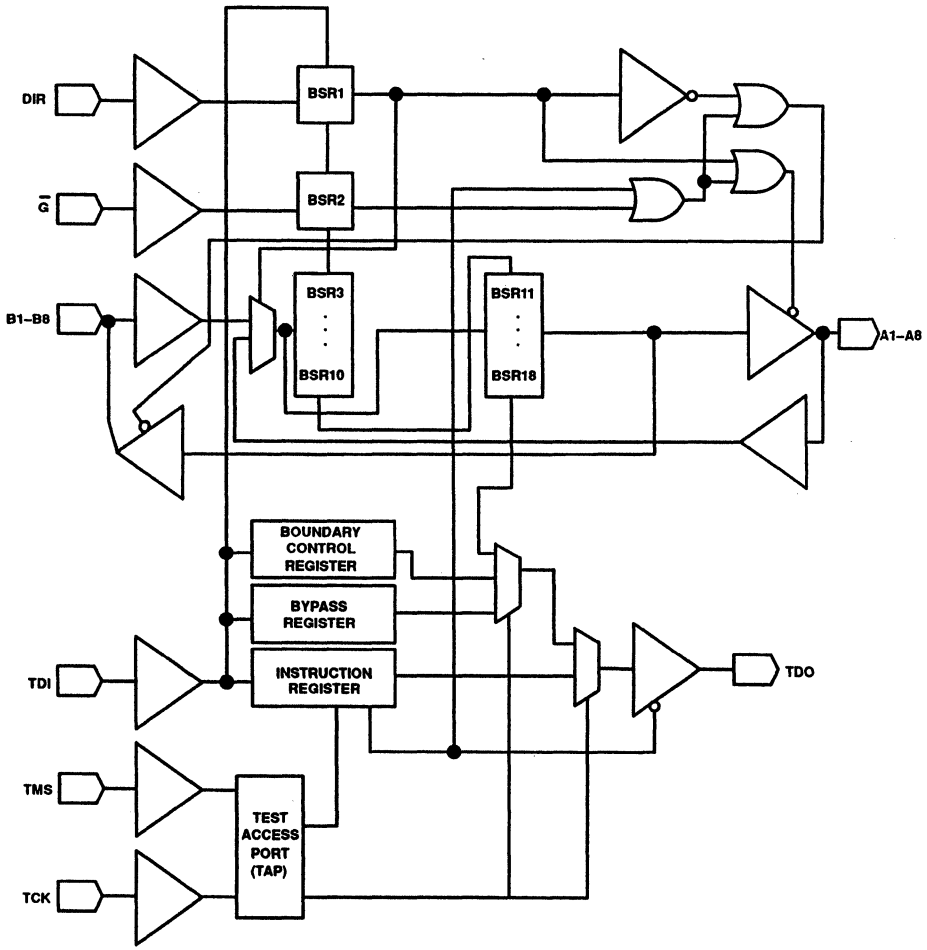
The SN54BCT8245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74BCT8245 is characterized for operation from 0°C to 70°C.

SCOPE™ is a trademark of Texas Instruments Incorporated.

NORMAL MODE FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

functional block diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input voltage ..... −0.5 V to 7 V
Voltage applied to any output in the disabled or power-off state ..... −0.5 V to 5.5 V
Voltage applied to any output in the high state ..... −0.5 V to V_{CC}
Current into any output in the low state: SN54BCT8245 (A1 thru A8) ..... 40 mA
SN54BCT8245 (B1 thru B8) ..... 96 mA
SN74BCT8245 (A1 thru A8) ..... 48 mA
SN74BCT8245 (B1 thru B8) ..... 128 mA
Operating free-air temperature range: SN54BCT8245 ..... −55°C to 125°C
SN74BCT8245 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			SN54BCT8245			SN74BCT8245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IHH}	Double high-level input voltage	TMS	10.25	10.50	10.75	10.25	10.50	10.75	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	A1 thru A8			−3			−3	mA
		B1 thru B8			−12			−15	
I_{OL}	Low-level output current	A1 thru A8			20			24	mA
		B1 thru B8			48			64	
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT8245			SN74BCT8245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	Any output	V_{CC} = 4.75 V, I_{OH} = −1 mA to −3 mA					2.7			V
	A1 thru A8	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		
			I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	B1 thru B8	V_{CC} = 4.5 V	I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
V_{OL}	A1 thru A8	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
	B1 thru B8	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				
			I_{OL} = 64 mA					0.42	0.55	
I_I	DIR and $\overline{G}$	V_{CC} = 5.5 V	V_I = 7 V			0.1			0.1	mA
	A and B	V_{CC} = 5.5 V	V_I = 5.5 V			1			1	
I_{IH}	A and B	V_{CC} = 5.5 V, V_I = 2.7 V				70			70	μA
	other	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	
I_{IHH}	TMS	V_{CC} = 5.5 V, V_I = 10.50 V				1			1	mA
I_{IL}	A and B	V_{CC} = 5.5 V, V_I = 0.5 V				−0.65			−0.65	mA
	other	V_{CC} = 5.5 V, V_I = 0.5 V				−1.2			−1.2	
I_{OS}‡	A1 thru A8	V_{CC} = 5.5 V, V_O = 0		−60		−150	−60		−150	mA
	B1 thru B8	V_{CC} = 5.5 V V_O = 0		−100		−225	−100		−225	
I_{CC}		V_{CC} = 5.5 V, Outputs open	Outputs high		5.5			5.5		mA
			Outputs low		52			52		
			Outputs disabled		2.3			2.3		
C_i		V_{CC} = 5.0 V, V_I = 2.5 V or 0.5 V								pF
C_{io}		V_{CC} = 5.0 V, V_O = 2.5 V or 0.5 V								pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

timing requirements (see Note 1)

		V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
		'BCT8245			SN54BCT8245		SN74BCT8245		
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{clock}	TCK	0							MHz
t_w	Pulse duration, TCK high or low								ns
t_{su}	Setup time, TMS before TCK ↑	9							ns
t_{su}	Setup time, TDI before TCK ↑	9							ns
t_{su}	Setup time, Any A or B before TCK ↑	9							ns
t_{su}	Setup time, $\overline{G}$ before TCK ↑	9							ns
t_h	Hold time, TMS after TCK ↑	1							ns
t_h	Hold time, TDI after TCK ↑	1							ns
t_h	Hold time, Any A or B after TCK ↑	1							ns
t_h	Hold time, $\overline{G}$ after TCK ↑	1							ns
t_{pu}	Wait time, power-up to TCK ↑	100							ns

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

NOTE 1: See General Information for load circuits and waveforms.

'BCT8245 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'BCT8245			SN54BCT8245		SN74BCT8245		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK			20						MHz
t_{PLH}	A or B	B or A		5.9						ns
t_{PHL}				6.5						
t_{PLH}	TCK ↓	A or B		11.5						ns
t_{PHL}				11						
t_{PLH}	TCK ↓	TDO		9.8						ns
t_{PHL}				9.7						
t_{PZH}	$\overline{G}$	A or B		6.2						ns
t_{PZL}				13						
t_{PZH}	TCK ↓	A or B		8						ns
t_{PZL}				7.7						
t_{PZH}	TCK ↓	TDO		14						ns
t_{PZL}				9.2						
t_{PHZ}	$\overline{G}$	A or B		7.5						ns
t_{PLZ}				13						
t_{PHZ}	TCK ↓	A or B		7						ns
t_{PLZ}				6.7						
t_{PHZ}	TCK ↓	TDO		13						ns
t_{PLZ}				7.8						

† For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: See General Information for load circuits and waveforms.

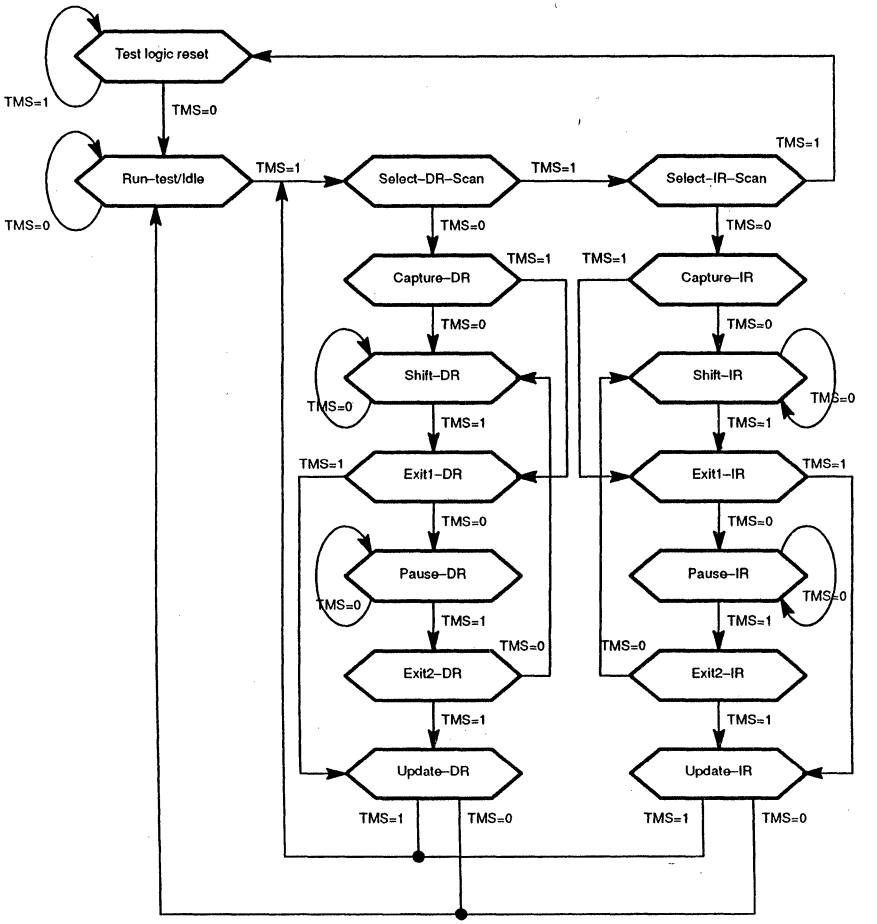


FIGURE 1. TAP STATE DIAGRAM

functional description

JTAG test information is conveyed by means of a 4-wire test bus. Test commands, test data, circuit state control instructions and synchronous control signals are all passed along the 4-wire bus. The function of the TAP is to extract the state control information and synchronous control signals from the 4-wire test bus, and generate the appropriate on-chip control signals for the JTAG test structures on the device. To accomplish this, the TAP cell monitors two signals from the 4-wire test bus—TCK (the JTAG Test Clock) and TMS (the JTAG Test Mode Select line). The functional block diagram on page 2 illustrates the JTAG 4-wire test bus and boundary scan architecture, and the relationship between the TAP cell, the 4-wire bus, and the various boundary scan test elements.

architectural elements

boundary scan register BSR0–BSR17

The boundary scan register contains eighteen (18) bits—one for each functional input or output pin of the device. FIGURE 2 illustrates the order of bits in the boundary scan register scan path. The boundary scan registers allow for board interconnect testing, defining conditions at the device logic periphery, and sampling data on the functional input or output pins without disturbing normal device operations.

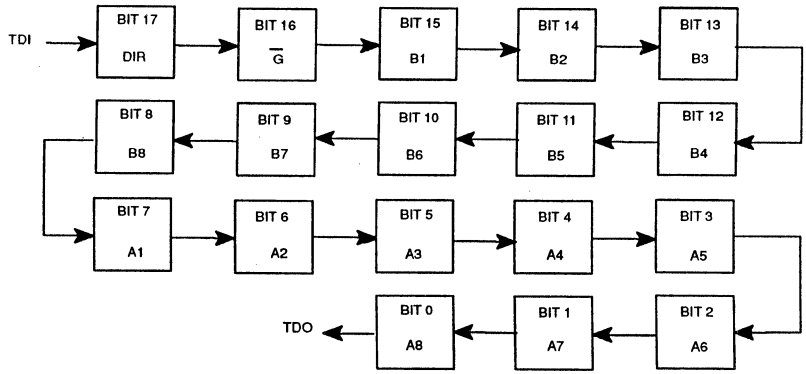


FIGURE 2. BOUNDARY SCAN REGISTER ORDER OF SCAN

bypass register

The bypass register contains one (1) bit for use when the device is in the bypass scan mode as defined in TABLE 3. FIGURE 3 illustrates the flow through the bypass register. This register provides a short one bit scan path through the device rather than scanning through the eighteen bit boundary scan register path. This is especially useful for decreasing test access times to a particular device on a board with several JTAG compatible devices which are not required for a specific test.

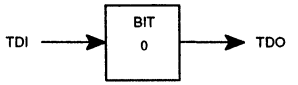


FIGURE 3. BYPASS REGISTER ORDER OF SCAN

test data register

The test data register contains two (2) bits used to control test operations occurring at the boundary. FIGURE 4 illustrates the order of bits in the test data register scan path.

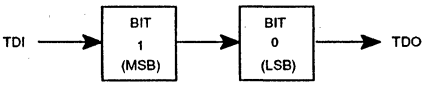


FIGURE 4. TEST DATA REGISTER ORDER OF SCAN

In addition to the boundary test instructions shown in TABLE 3, additional test operations shown in TABLE 1 can be performed when the run test opcode is installed in the instruction register. These test operations include: pseudo-random pattern generation (PRPG) and parallel signature analysis (PSA) as shown in TABLE 1 when the run test opcode is installed in the instruction register.

TABLE 1. RUN TEST OPCODES

OPCODE MSB → LSB	TEST
00	SAMPLE INPUTS/TOGGLE OUTPUTS
01	PRPG/16 BIT MODE
10	PSA/16 BIT MODE
11	SIMULTANEOUS PRPG AND PSA/8 BIT MODE

example

In order to implement the sample inputs/toggle outputs opcode from TABLE 1, a series of operations must be performed. Refer to FIGURE 1 to trace these operations through the TAP state diagram. The select-IR path is used to shift opcodes into the instruction register. The select-DR path is used to shift data into the boundary scan register or bypass register, or to shift opcodes into the test data register. To shift data or opcodes into the registers, after entering the appropriate shift-DR or shift-IR state TMS must be held low for enough TCK pulses to shift the correct number of bits into the registers.

First, the boundary read opcode (test or normal mode) must be loaded into the instruction register using the select-IR scan path, then the boundary scan registers may be initialized using the select-DR scan path. Load the test data register scan opcode (test or normal mode) into the instruction register using the select-IR scan path, then the sample inputs/toggle outputs opcode (00) may be entered into the test data register using the select-DR-scan path. Finally, the boundary run test opcode (test or normal mode) must be entered into the instruction register using the select-IR scan path. Exiting the select-IR-scan path to the run-test/idle state starts the outputs toggling. As long as the device remains in the run-test/idle state, each TCK pulse will cause the device's function outputs to toggle to the opposite state.

tap bits

Tap bit settings used for PSA and PRPG test operations are shown in TABLE 2. The use of these tap bits as well as the shift operations necessary to perform 8-bit and 16-bit PSA and PRPG test operations is described in FIGURE 5 through FIGURE 7.

TABLE 2. TAP BIT SETTINGS FOR PSA AND PRPG TEST OPERATIONS

OPERATION	MODE	TAP BITS A → Y
PSA	8-BIT	B2, B3, B4, B8
	16-BIT	B7, A1, A4, A8
PRPG	8-BIT	A2, A3, A4, A8
	16-BIT	B7, A1, A4, A8

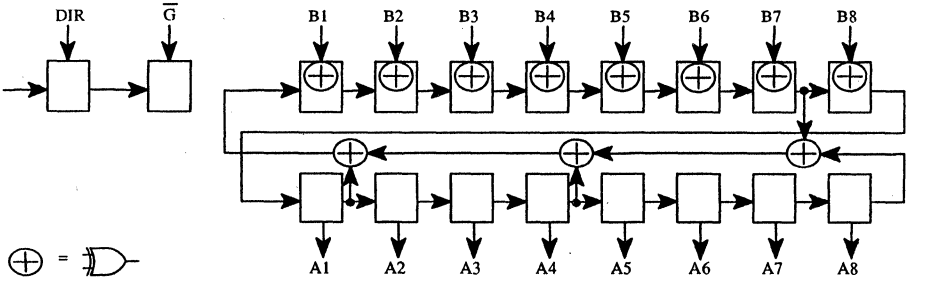


FIGURE 5. 16-BIT PSA CONFIGURATION DURING RUN TEST/IDLE STATE

A PSA operation on the 8 data inputs proceeds as the 8 data outputs are held static.

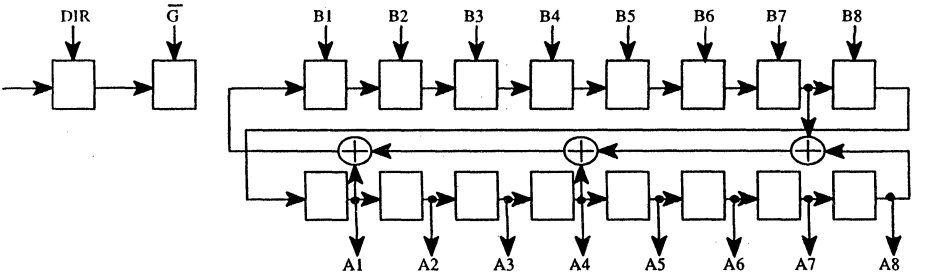


FIGURE 6. 16-BIT PRPG CONFIGURATION DURING RUN TEST/IDLE STATE

A PRPG operation from the 8 data outputs proceeds while the 8 data inputs are ignored.

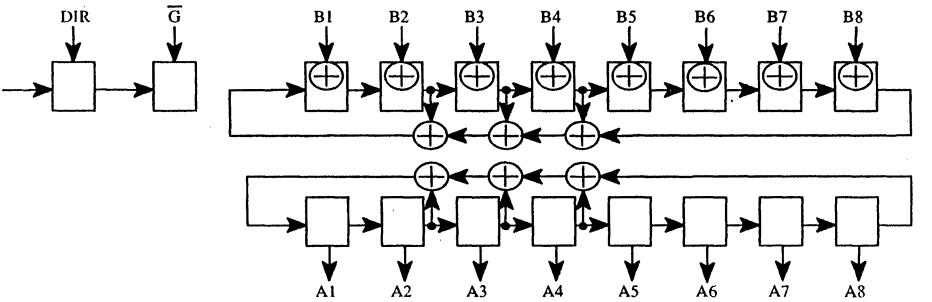


FIGURE 7. 8-BIT PSA AND PRPG CONFIGURATION DURING RUN TEST/IDLE STATE

Simultaneously, an 8-bit PSA operation proceeds on the 8 data inputs, while an 8-bit PRPG operation proceeds from the 8 data outputs.

instruction register

The test device instruction register is 8 bits in length. When in the Shift-IR state, data can be scanned into the register from the most significant bit (MSB) to the least significant bit (LSB) as shown in FIGURE 8. The instruction register controls the internal device structures and test operations according to the opcodes listed in TABLE 3.

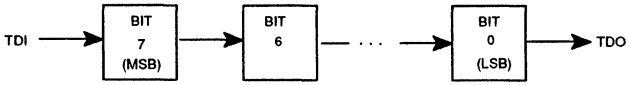


FIGURE 8. INSTRUCTION REGISTER ORDER OF SCAN

instruction set

The 'BCT8245 uses the 8-bit serial instruction register as its instruction input. TABLE 3 summarizes the 8-bit opcodes and corresponding tests.

TABLE 3. OPCODES (see Note 1)

OPCODE BIT 7–BIT 0 MSB-LSB	FUNCTION
X0000000	BOUNDARY SCAN
X0000001	ID REGISTER SCAN
X0000010	SAMPLE BOUNDARY
X0000011	BOUNDARY SCAN
X0000100	BYPASS SCAN MODE
X0000101	BYPASS SCAN MODE
X0000110	CONTROL BOUNDARY TO HIGH IMPEDANCE
X0000111	CONTROL BOUNDARY TO 1/0
X0001000	BYPASS SCAN MODE
X0001001	BOUNDARY RUN TEST/TEST MODE
X0001010	BOUNDARY READ/NORMAL MODE
X0001011	BOUNDARY READ/TEST MODE
X0001100	BOUNDARY SELF TEST/NORMAL MODE
X0001101	BOUNDARY TOGGLE OUTPUTS/TEST MODE
X0001110	TEST DATA REGISTER SCAN/NORMAL MODE
X0001111	TEST DATA REGISTER SCAN/TEST MODE
ALL OTHER	BYPASS SCAN MODE

X = Parity Bit (Even Parity)
NOTE 1: If Bit 4 through Bit 6 are all 0, then Bit 0 through Bit 3 are decoded as shown in TABLE 3.

The test functions which are identified in TABLE 3 and performed by the test integrated circuits are defined as follows:

boundary scan

A boundary scan of the boundary scan register is performed according to the methodology designated by the proposed JTAG or the proposed IEEE P1149.1 specifications. This instruction performs a combination of sample boundary and control boundary to 1/0 tests as specified below.

ID register scan

The test circuit is placed in the bypass mode as defined by JTAG in the absence of an ID Register. A logic 0 is loaded into the bypass register before scanning.

sample boundary

Data appearing at the device's function inputs and outputs is sampled and scanned out the TDO pin. This operation is performed in a functional mode without disturbing normal device operations.

control boundary to high impedance

The device's function outputs are placed in the high impedance state. The bypass register is selected in the scan path. Function inputs remain operational.

control boundary to 1/0

Function inputs and outputs are controlled by the boundary register. The bypass register is selected in the scan path.

boundary run test

Test operations controlled by the test data register are performed while the device is in the idle mode. Operations performed in this mode include the following:

parallel signature analysis of inputs

Data appearing on the device's data inputs is compressed by a parallel signature analysis (PSA) operation with fixed tap bits. Data shall be compressed into sixteen bits. The initial seed value for the PSA operation should be scanned into the boundary scan register prior to performing the test operation.

pseudo-random pattern generation from outputs

A pseudo-random data pattern (PRPG) is output from the outputs of the test device. The initial seed value for the PRPG should be scanned into the data register prior to performing the test operation.

simultaneous PSA and PRPG

An 8-Bit PSA of inputs and an 8-Bit PRPG from outputs is performed simultaneously as specified above.

sample inputs/toggle outputs

The devices inputs are sampled on successive rising edges of TCK, while the device's function output pins are toggled simultaneously on successive falling edges of TCK while the device is in the idle mode. This test is intended to be used for parametric testing and pattern generation purposes. The initial pattern should be scanned into the boundary scan register prior to performing the test operation.

boundary read (test mode and normal mode)

Data is scanned in and out of the boundary scan register without first preloading the boundary condition. This function is particularly useful after a PSA operation—the results can be scanned out for review by the test controller.

test data register scan (test mode and normal mode)

The test data register is selected for scan access.

boundary self test

The boundary scan register is preloaded with the inverted contents of the latch memory elements of each boundary scan register bit. The boundary scan register is then scanned out. Prior to performing this test known data should be scanned into the boundary scan register.

boundary toggle outputs

The device's function output pins are toggled simultaneously on successive TCK clock inputs. This test is intended to be used for parametric testing and pattern generation purposes. The initial pattern should be scanned into the data register prior to performing the test operation.

bypass scan mode

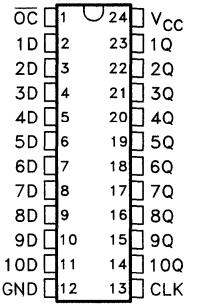
The bypass register is selected in the scan path and the device is placed in the normal mode.

SN74BCT29821, SN74BCT29822
10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

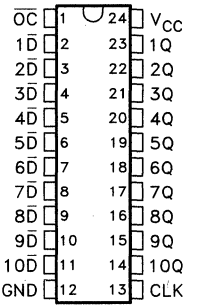
D3125, FEBRUARY 1989—REVISED JULY 1989

- **BiCMOS Process with CMOS Inputs and TTL Outputs Substantially Reduces Standby Current**
- **Input has 50-kΩ Pullup Resistor**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Power-Up High-Impedance State**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Functionally Equivalent to Am29821A, Am29822A, SN74ALS29821, and SN74ALS29822**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

SN74BCT29821 ... DW OR NT PACKAGE
(TOP VIEW)



SN74BCT29822 ... DW OR NT PACKAGE
(TOP VIEW)



description

These 10-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs on the 'BCT29821 will be true, and on the 'BCT29822 will be complementary to the data input.

A buffered output-control ($\overline{OC}$) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74BCT' family is characterized for operation from 0°C to 70°C.

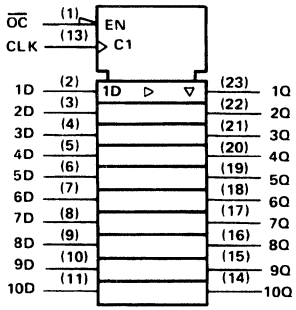
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

FUNCTION TABLE (EACH FLIP-FLOP)
'BCT29821

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†

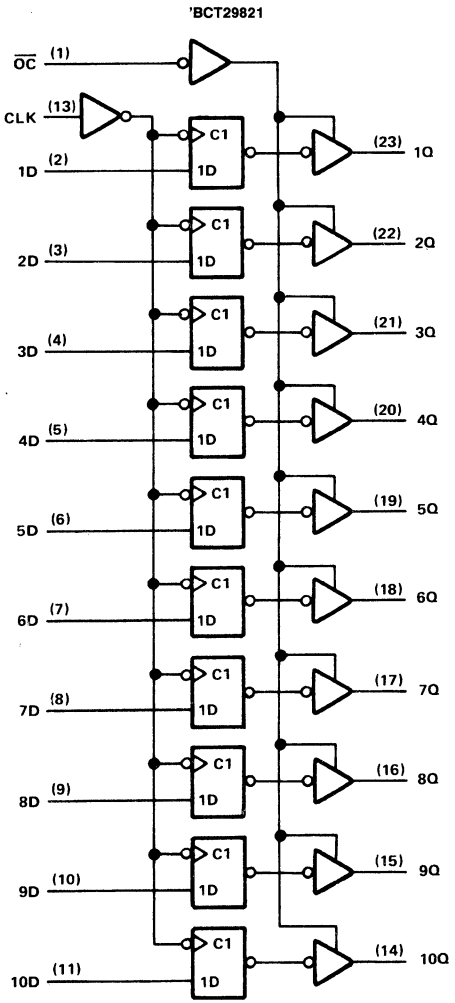
'BCT29821



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

'BCT29821

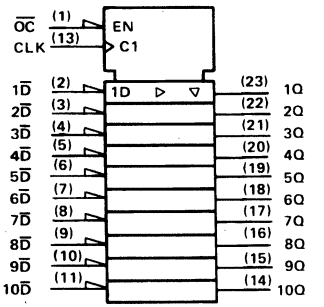


FUNCTION TABLE (EACH FLIP-FLOP)
'BCT29822

INPUTS			OUTPUT
$\overline{OC}$	CLK	$\overline{D}$	Q
L	↑	H	L
L	↑	L	H
L	L	X	Q_0
H	X	X	Z

logic symbol†

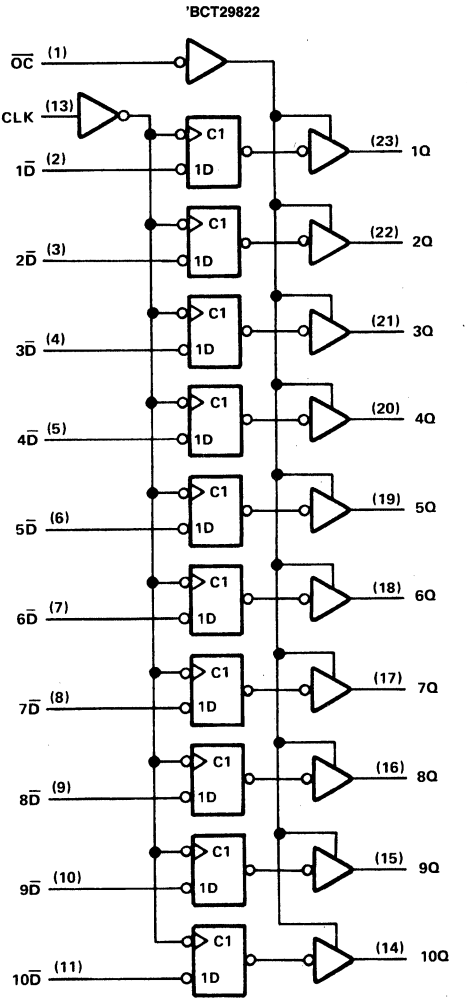
'BCT29822



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

'BCT29822



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−24	mA
I_{OL}	Low-level output current				48	mA
t_w	Pulse duration	CLK high	7			ns
		CLK low	7			
t_{su}	Setup time, data before CLK ↑		7			ns
t_h	Hold time, data after CLK ↑		1			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −15 mA		2.4	3.3		V
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA			0.35	0.5	V
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.4 V				20	μA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.4 V				−20	μA
I_I	V_{CC} = 5.5 V, V_I = 7 V				0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V		−10		−75	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.4 V				−0.2	mA
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0		−75		−250	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		6	10	mA
		Outputs low		25	35	
		Outputs disabled		2	6	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	1.5	7.5	10	1.5	12	ns
t_{PHL}			1.5	6.5	9	1.5	10	
t_{PZH}	$\overline{OC}$	Any Q	2	7.5	10	2	12	ns
t_{PZL}			2	9	12	2	13	
t_{PHZ}	$\overline{OC}$	Any Q	2	5	7	2	8	ns
t_{PLZ}			2	5	7	2	8	

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−24	mA
I_{OL}	Low-level output current				48	mA
t_w	Pulse duration	CLK high				ns
		CLK low				
t_{su}	Setup time, data before CLK ↑					ns
t_h	Hold time, data after CLK ↑					ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

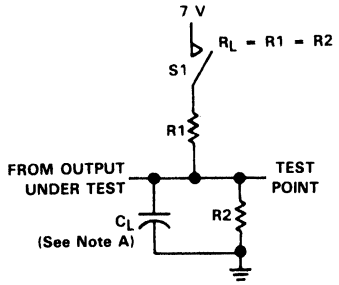
PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −15 mA		2.4	3.3		V
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA			0.35	0.5	V
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.4 V				20	μA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.4 V				−20	μA
I_I	V_{CC} = 5.5 V, V_I = 7 V				0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V		−10		−75	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.4 V				−0.2	mA
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0		−75		−250	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		6		mA
		Outputs low		25		
		Outputs disabled		2		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q		7.5				ns
t_{PHL}				6.5				
t_{PZH}	$\overline{OC}$	Any Q		7.5				ns
t_{PZL}				9				
t_{PHZ}	$\overline{OC}$	Any Q		5				ns
t_{PLZ}				5				

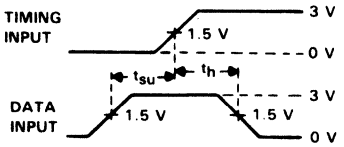
PARAMETER MEASUREMENT INFORMATION



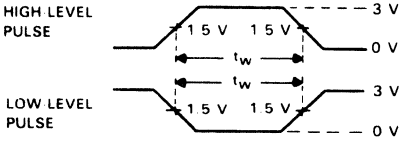
LOAD CIRCUIT

SWITCH POSITION TABLE

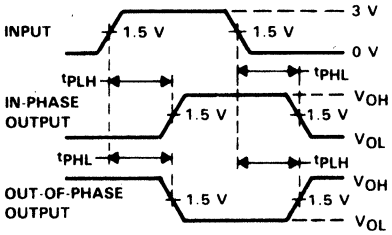
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



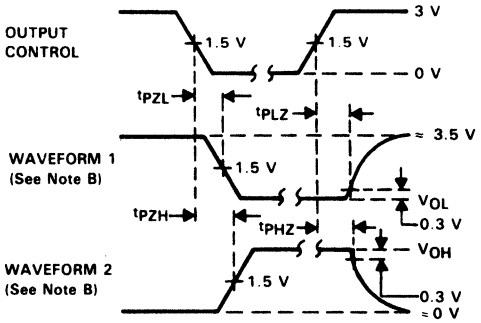
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by the generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

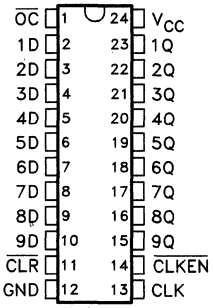
FIGURE 1. SWITCHING CHARACTERISTICS

SN74BCT29823, SN74BCT29824
9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

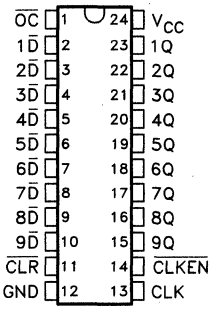
D3181, NOVEMBER 1988—REVISED JULY 1989

- **BiCMOS Process with TTL Inputs and Outputs**
- **BiCMOS Design Substantially Reduces Standby Current**
- **Functionally Equivalent to AMD Am29823, Am29824, 'ALS29823, and 'ALS29824**
- **Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity**
- **Power-Up High-Impedance State**
- **Buffered Control Inputs to Reduce DC Loading Effects**
- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

SN74BCT29823 ... DW OR NT PACKAGE
(TOP VIEW)



SN74BCT29824 ... DW OR NT PACKAGE
(TOP VIEW)



description

These 9-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

With the clock enable ($\overline{CLKEN}$) low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The 'BCT29823 has noninverting D inputs and the 'BCT29824 has inverting D inputs. Taking the $\overline{CLR}$ input low causes the nine Q outputs to go low independently of the clock.

A buffered output-control input ($\overline{OC}$) can be used to place the nine outputs in either normal logic state (high or low level) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops.

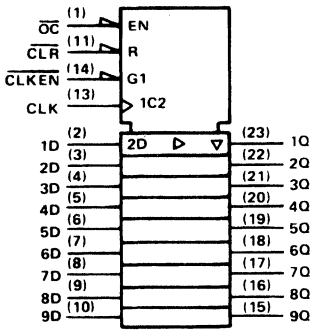
Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74BCT29823 and SN74BCT29824 are characterized for operation from 0° to 70°C.

FUNCTION TABLE

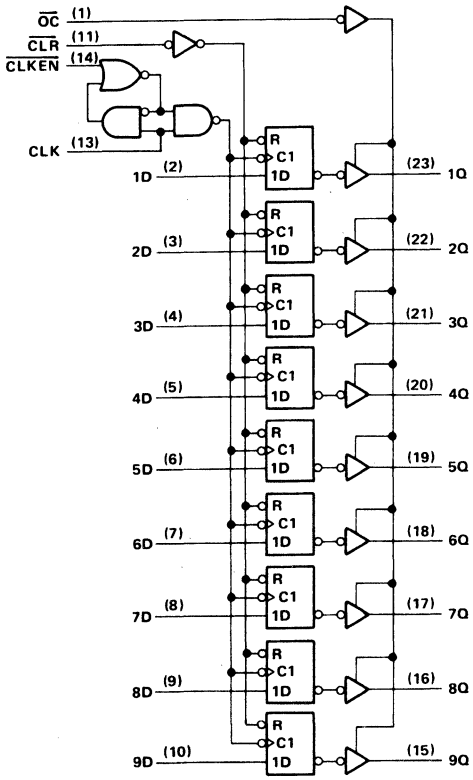
INPUTS					OUTPUT
$\overline{OC}$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

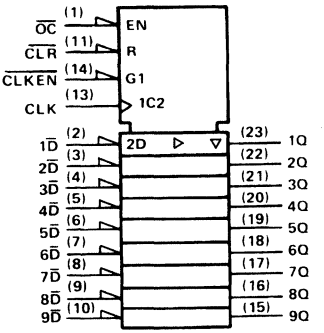
logic diagram (positive logic)



FUNCTION TABLE

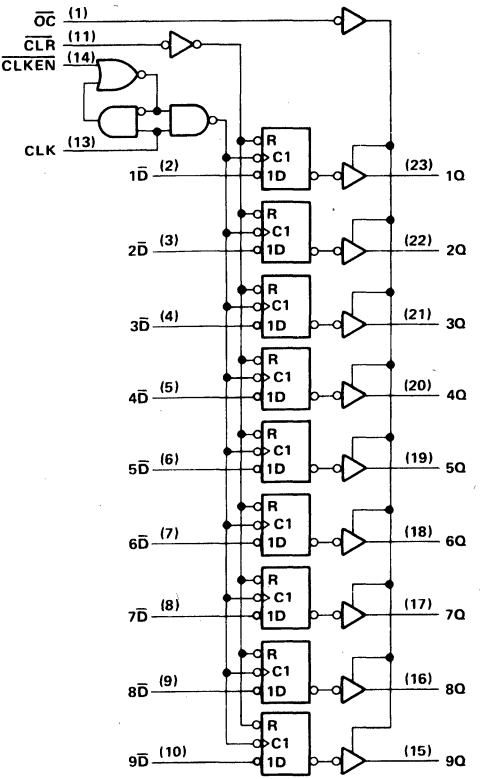
INPUTS					OUTPUT
$\overline{OC}$	CLR	CLKEN	CLK	$\overline{D}$	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−24	mA
I_{OL}	Low-level output current				48	mA
t_w	Pulse duration	$\overline{CLR}$ low	6			ns
		CLK high or low	7			
t_{su}	Setup time before CLK ↑	$\overline{CLR}$ inactive	2			ns
		Data	7			
		$\overline{CLKEN}$ high	6			
		$\overline{CLKEN}$ low	8			
t_h	Hold time	$\overline{CLKEN}$	0			ns
		Data	1			
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −15 mA		2.4	3.2		V
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA			0.35	0.5	V
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				20	μA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.4 V				−20	μA
I_I	V_{CC} = 5.5 V, V_I = 5.5 V				0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V		−10		−75	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.4 V				−0.2	mA
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0		−75		−250	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		6	10	mA
		Outputs low		25	35	
		Outputs disabled		2	6	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	1.5	7.5	10	1.5	12	ns
t_{PHL}			1.5	6.5	9	1.5	10	
t_{PHL}	$\overline{CLR}$	Any Q	1.5	7.5	10	1.5	12	ns
t_{PZH}	$\overline{OC}$	Any Q	2	7.5	10	2	12	ns
t_{PZL}			2	9	12	2	13	
t_{PHZ}	$\overline{OC}$	Any Q	2	5	7	2	8	ns
t_{PLZ}			2	5	7	2	8	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

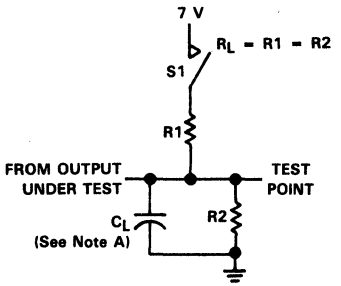
PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V, I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.5 V, I_{OH} = −15 mA		2.4	3.2		V
	V_{CC} = 4.5 V, I_{OH} = −24 mA		2			
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 48 mA			0.35	0.5	V
I_{OZH}	V_{CC} = 5.5 V, V_O = 2.7 V				20	μA
I_{OZL}	V_{CC} = 5.5 V, V_O = 0.4 V				−20	μA
I_I	V_{CC} = 5.5 V, V_I = 5.5 V				0.1	mA
I_{IH}	V_{CC} = 5.5 V, V_I = 2.7 V		−10		−75	μA
I_{IL}	V_{CC} = 5.5 V, V_I = 0.4 V				−0.2	mA
I_{OS}‡	V_{CC} = 5.5 V, V_O = 0		−75		−250	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		6		mA
		Outputs low		25		
		Outputs disabled		2		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q		7.5				ns
t_{PHL}				6.5				
t_{PHL}	$\overline{CLR}$	Any Q		7.5				ns
t_{PZH}	$\overline{OC}$	Any Q		7.5				ns
t_{PZL}				9				
t_{PHZ}	$\overline{OC}$	Any Q		5				ns
t_{PLZ}				5				

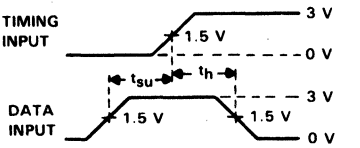
PARAMETER MEASUREMENT INFORMATION



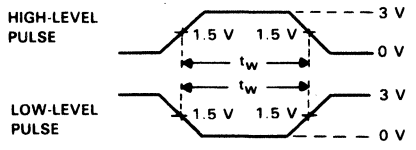
LOAD CIRCUIT

SWITCH POSITION TABLE

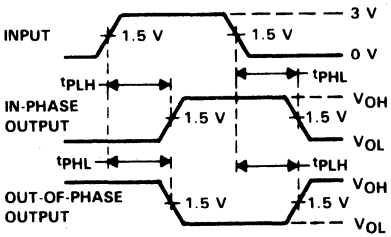
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



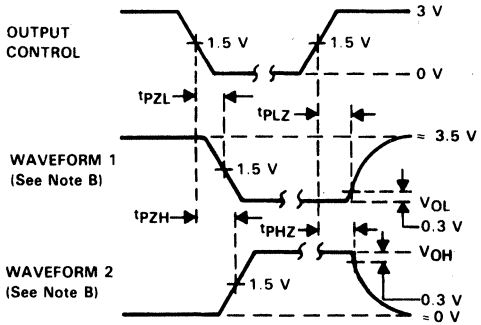
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



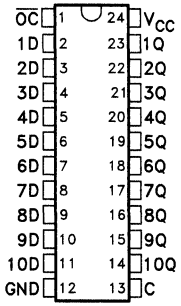
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by the generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

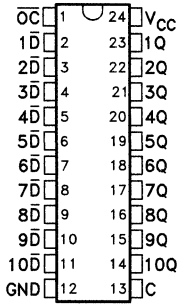
FIGURE 1. SWITCHING CHARACTERISTICS

- **BiCMOS Process with CMOS Inputs and TTL Outputs Substantially Reduces Standby Current**
- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Bus-Structured Pinout**
- **Input Has 50-kΩ Pullup Resistor**
- **Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity**
- **Buffered Control Inputs to Reduce DC Loading**
- **Power-Up High-Impedance State**
- **Functionally Equivalent to Am29841A, Am29842A, SN74ALS29841, and SN74ALS29842**
- **Package Options include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

SN74BCT29841 ... DW OR NT PACKAGE
(TOP VIEW)



SN74BCT29842 ... DW OR NT PACKAGE
(TOP VIEW)



description

These 10-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

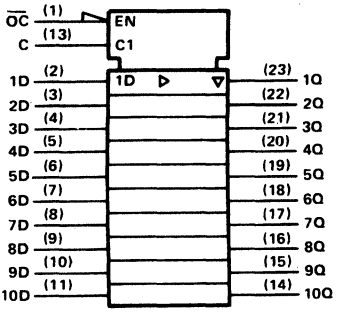
The ten latches are transparent D-type. The 'BCT29841 has noninverting data (D) inputs. The 'BCT29842 has inverting $\overline{D}$ inputs.

A buffered output control ($\overline{OC}$) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. The outputs are also in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered-down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN74BCT29841 and SN74BCT29842 are characterized for operation from 0°C to 70°C.

'BCT29841 logic symbol†

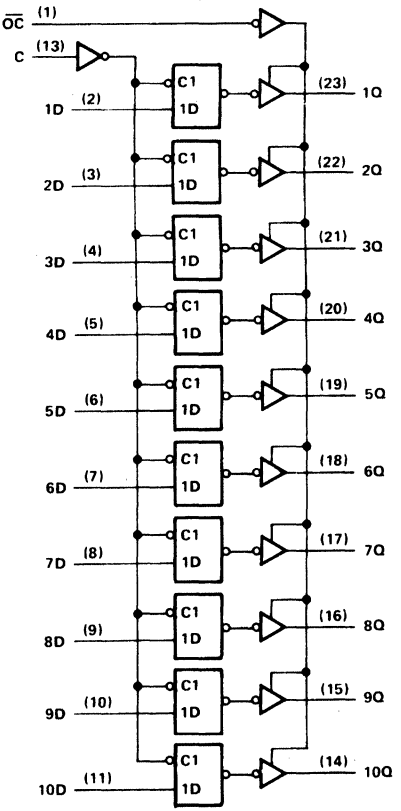


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

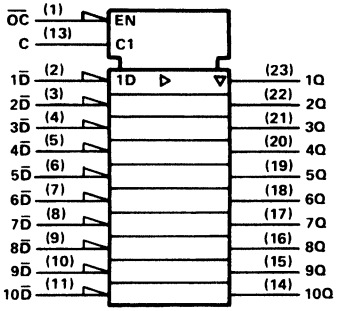
FUNCTION TABLE
'BCT29841

INPUTS			OUTPUT
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

'BCT29841 logic diagram (positive logic)



'BCT29842 logic symbol†

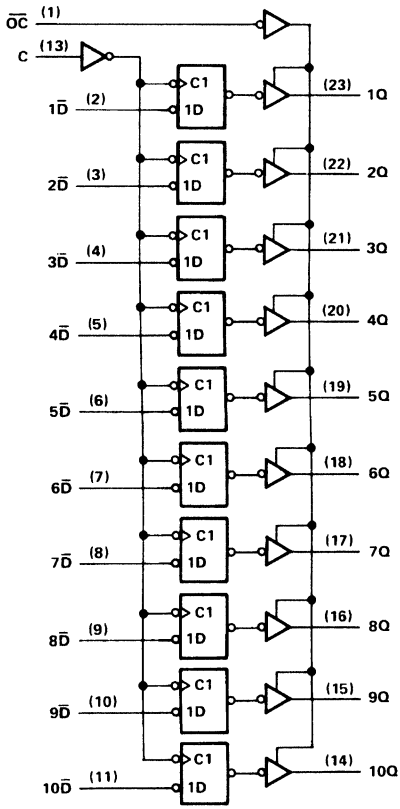


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
'BCT29842

INPUTS			OUTPUT
$\overline{OC}$	C	$\overline{D}$	Q
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

'BCT29842 logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage ..... 5.5 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
t_w	Pulse duration, enable C high	4			ns
t_{su}	Setup time, data before enable C ↓	1.5			ns
t_h	Hold time, data after enable C ↓	3.5			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −15 mA	2.4			V
		I_{OH} = −24 mA	2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	V
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V	−10		−75	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−75		−275	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		3	7	mA
		Outputs low		24	35	mA
		Outputs disabled		3	7	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	Q	1.5	4.5	7	1.5	8	ns
t_{PHL}			1.5	5.7	8	1.5	9	
t_{PLH}	C	Q	1.5	6	8	1.5	10	ns
t_{PHL}			1.5	6	8	1.5	10	
t_{PZH}	$\overline{OC}$	Q	2	10	13	2	15	ns
t_{PZL}			2	10	13	2	15	
t_{PHZ}	$\overline{OC}$	Q	2	5	7	2	8	ns
t_{PLZ}			2	5	7	2	8	

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
t_w	Pulse duration, enable C high	4			ns
t_{su}	Setup time, data before enable C ↓	1.5			ns
t_h	Hold time, data after enable C ↓	3.5			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

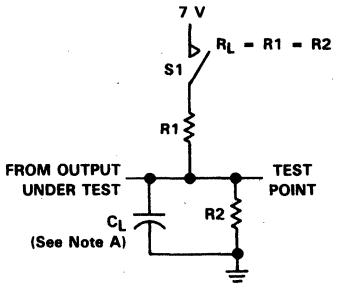
PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −15 mA	2.4			V
		I_{OH} = −24 mA	2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.5	V
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	μA
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V	−10		−75	mA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	−75		−275	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		3	7	mA
		Outputs low		24	35	mA
		Outputs disabled		3	7	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	D	Q	1.5	5.7	8	1.5	9	ns
t_{PHL}			1.5	4.5	7	1.5	8	
t_{PLH}	C	Q	1.5	6	8	1.5	10	ns
t_{PHL}			1.5	6	8	1.5	10	
t_{PZH}	$\overline{OC}$	Q	2	10	13	2	15	ns
t_{PZL}			2	10	13	2	15	
t_{PHZ}	$\overline{OC}$	Q	2	5	7	2	8	ns
t_{PLZ}			2	5	7	2	8	

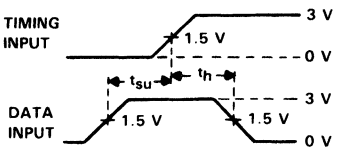
PARAMETER MEASUREMENT INFORMATION



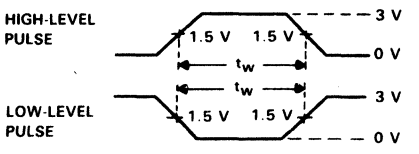
LOAD CIRCUIT

SWITCH POSITION TABLE

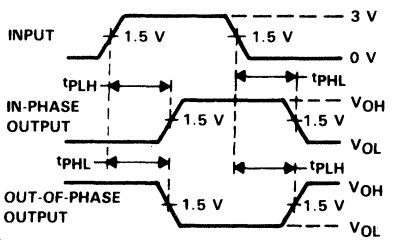
TEST	S1
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	Open
t_{PZL}	Closed
t_{PHZ}	Open
t_{PLZ}	Closed



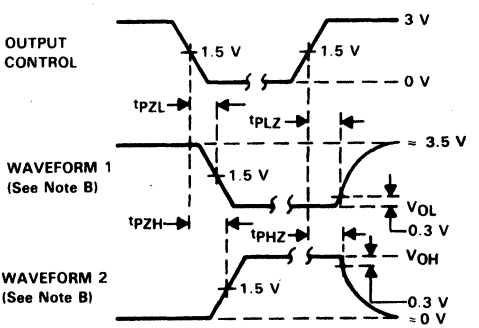
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one input transition per measurement.

FIGURE 1. SWITCHING CHARACTERISTICS

Contents

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

EXAMPLE: SN 54BCT240 J −00†

1. Prefix

MUST CONTAIN TWO TO FOUR LETTERS

SN	Standard Prefix
SNJ	MIL-STD-883 Processed and Screened per JEDEC Standard 101
JANB	MIL-M-38510 Processed

2. Unique Circuit Description

MUST CONTAIN SIX TO NINE CHARACTERS

Examples: 54BCT620
74BCT125
74BCT2240

3. Package

MUST CONTAIN ONE OR TWO LETTERS

J, JT, N, NT (Dual-in-line packages)‡
D, DW ("Small Outline" Packages)
FK (Leadless Ceramic Chip Carriers)
(From pin-connection diagram on individual data sheet)

4. Instructions (Dash No.)

MUST CONTAIN TWO NUMBERS

−00 No special instructions
−10 Solder-dipped leads (N and NT packages only)

† For tape and reel information contact the factory.

‡ These circuits in dual-in-line packages are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier. Please contact your TI sales representative for the method that will best suit your particular needs.

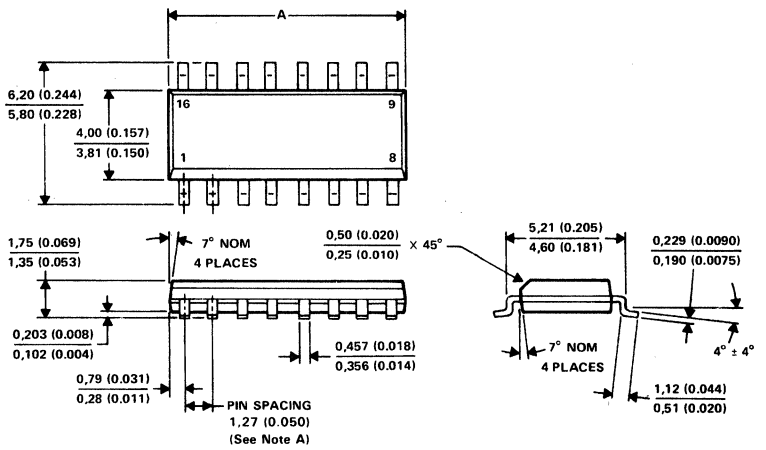
Dual-in-line (J, JT, N, NT)

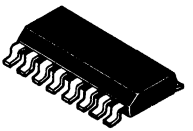
—Slide Magazines
—A-Channel Plastic Tubing
—Barnes Carrier (N only)
—Sectioned Cardboard Box
—Individual Plastic Box

D008, D014, and D016 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D008, D014, and D016
(16-pin package used for illustration)





DIM \ PINS	8	14	16
A MIN	4,80	8,55	9,80
	(0.189)	(0.337)	(0.386)
A MAX	5,00	8,74	10,00
	(0.197)	(0.344)	(0.394)

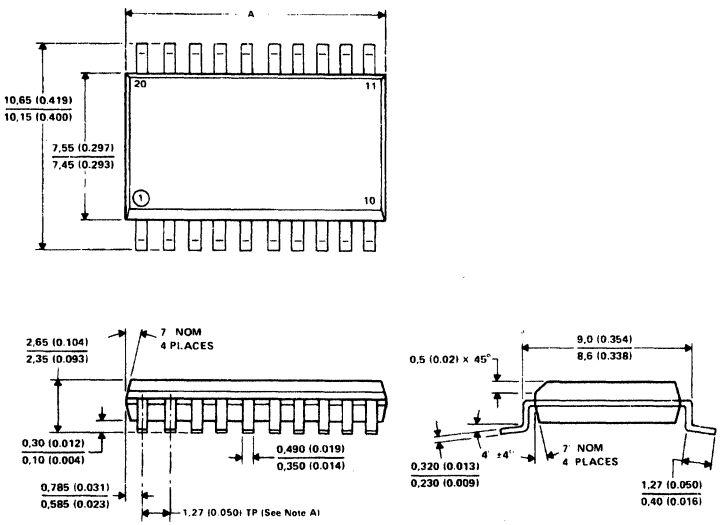
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

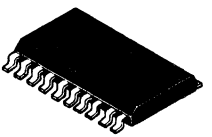
NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

DW016, DW020, DW024, and DW028 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DW016, DW020, DW024, and DW028
(20-pin package used for illustration)





DIM \ PINS	16	20	24	28†
A MIN	10,16	12,70	15,29	17,68
	(0.400)	(0.500)	(0.602)	(0.696)
A MAX	10,36	12,90	15,49	17,88
	(0.408)	(0.508)	(0.610)	(0.704)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

†The 28-pin package drawing is presently classified as Advance Information.

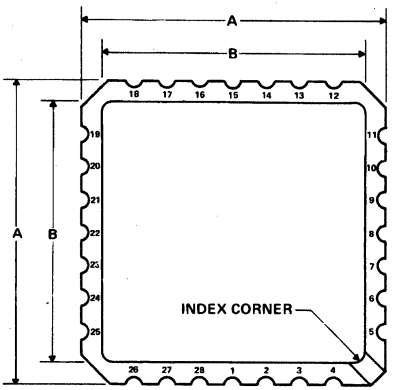
NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

FK020 and FK028 ceramic chip carrier packages

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.

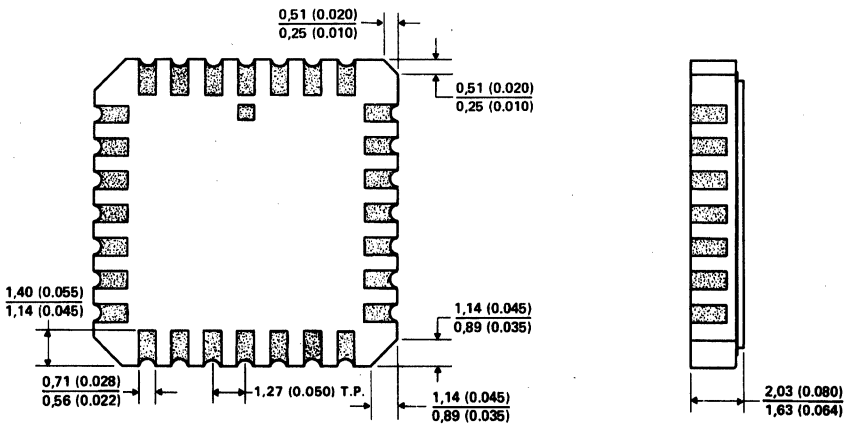
FK020 and FK028
(28-terminal package shown)



CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS004CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)

*All dimensions and notes for the specified JEDEC outline apply.

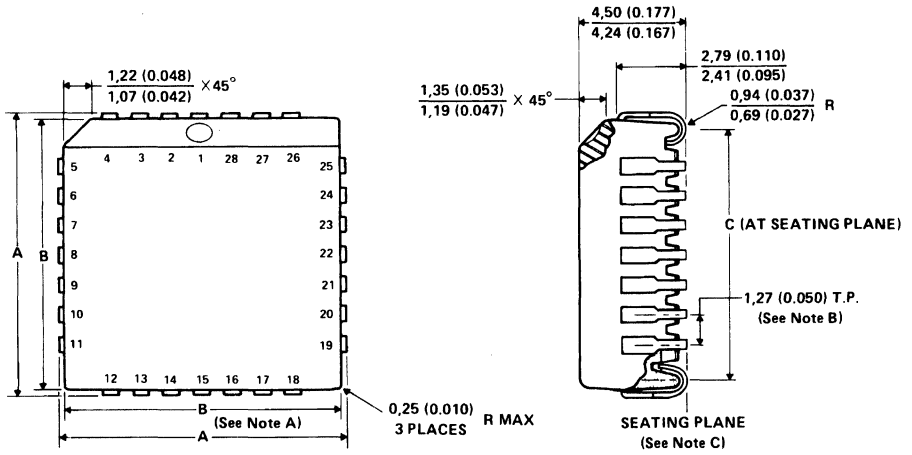


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

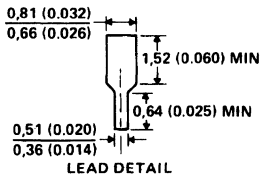
FN020, FN028, FN044, FN068, and FN084 plastic chip carrier packages

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN020, FN028, FN044, FN068, and FN084
(28-terminal package used for illustration)



NO. OF TERMINALS	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
20	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,87 (0.310)	8,38 (0.330)
28	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,41 (0.410)	10,92 (0.430)
44	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,49 (0.610)	16,00 (0.630)
68	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.956)	23,11 (0.910)	23,62 (0.930)
84	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.158)	27,69 (1.090)	28,70 (1.130)



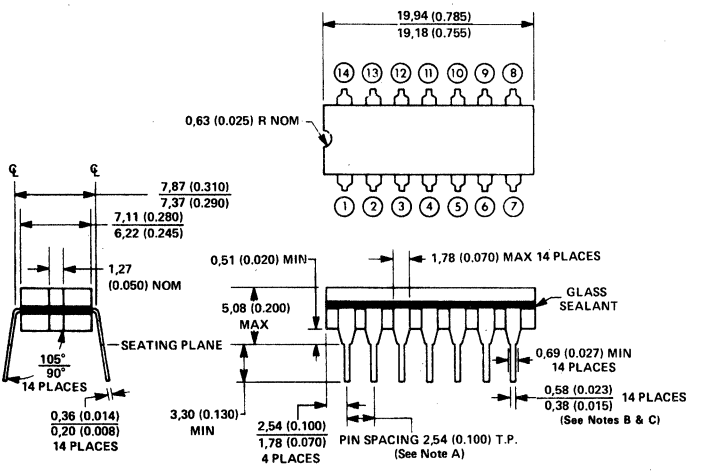
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

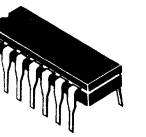
NOTES: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by dimension B.
B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.
C. The lead contact points are planar within 0,10 (0.004).

J014 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

J014





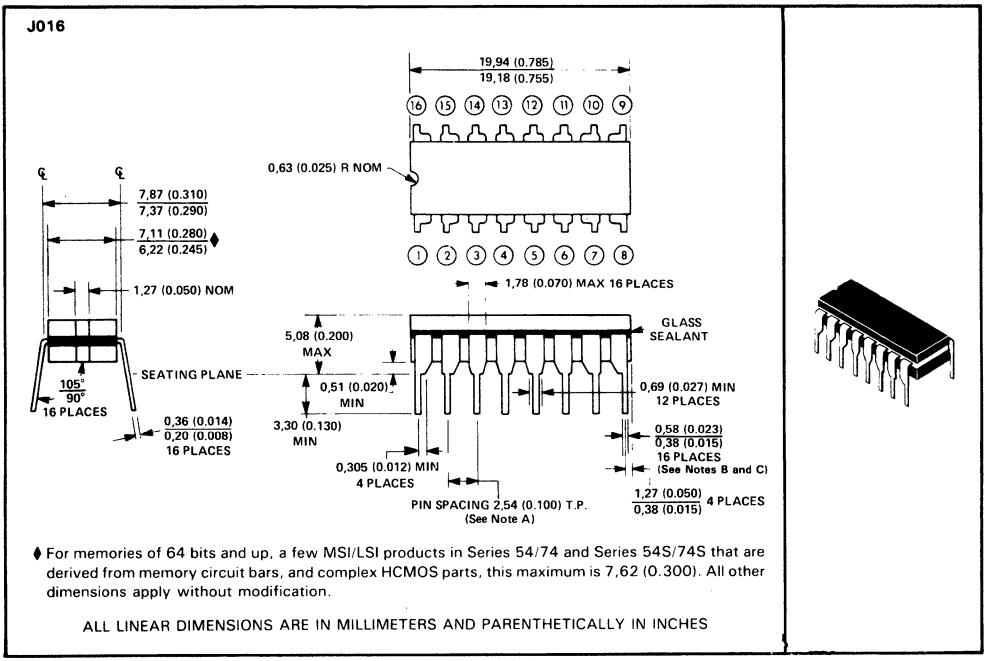
Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

J016 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



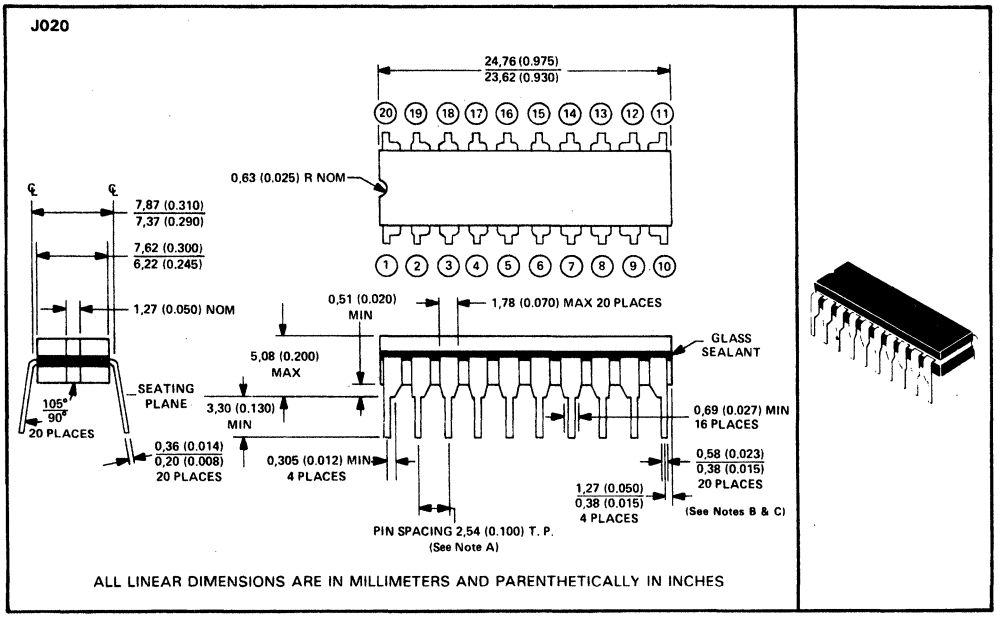
♦ For memories of 64 bits and up, a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, and complex HCMOS parts, this maximum is 7,62 (0.300). All other dimensions apply without modification.

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

J020 ceramic dual-in-line package

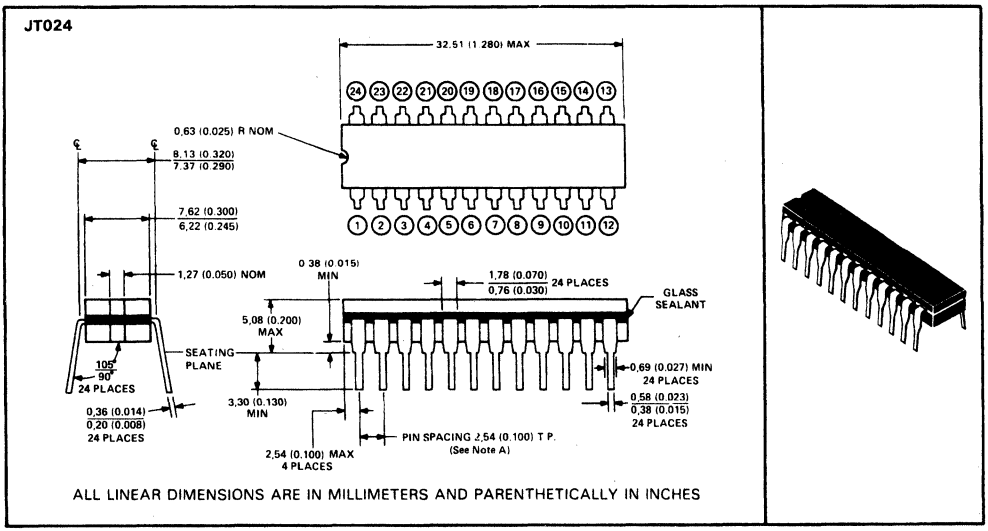
This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

JT024 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldering assembly.

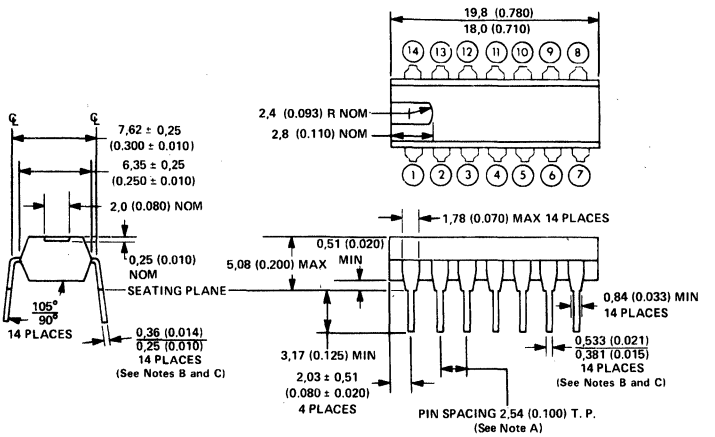


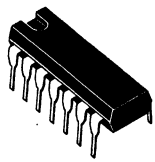
NOTE: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

N014 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N014





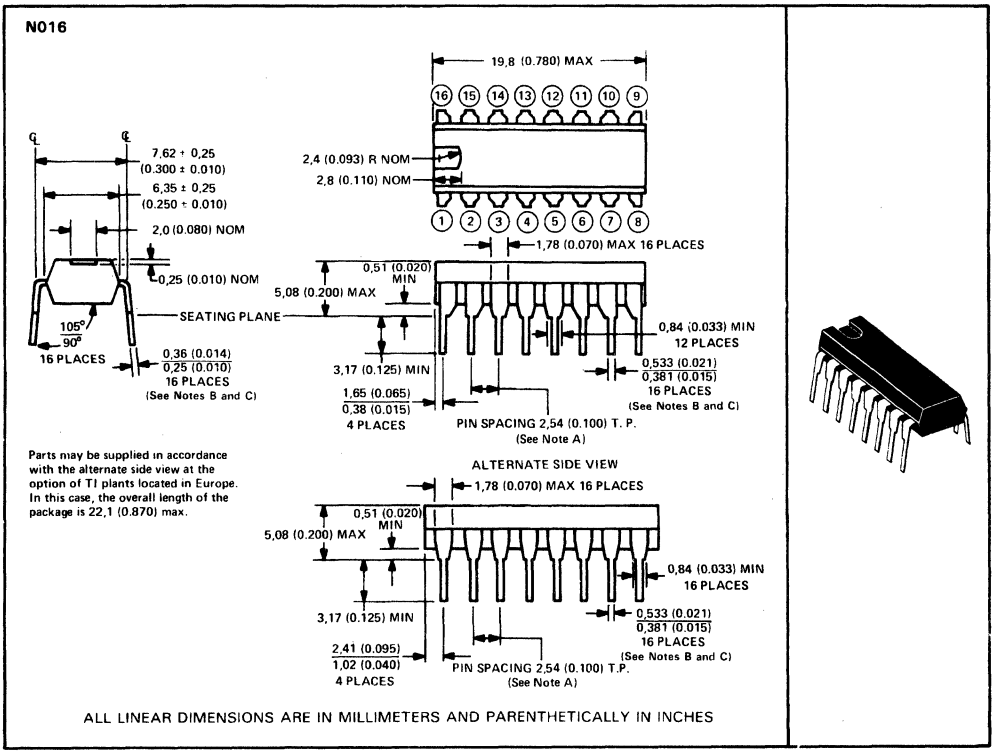
Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

N016 plastic dual-in-line package

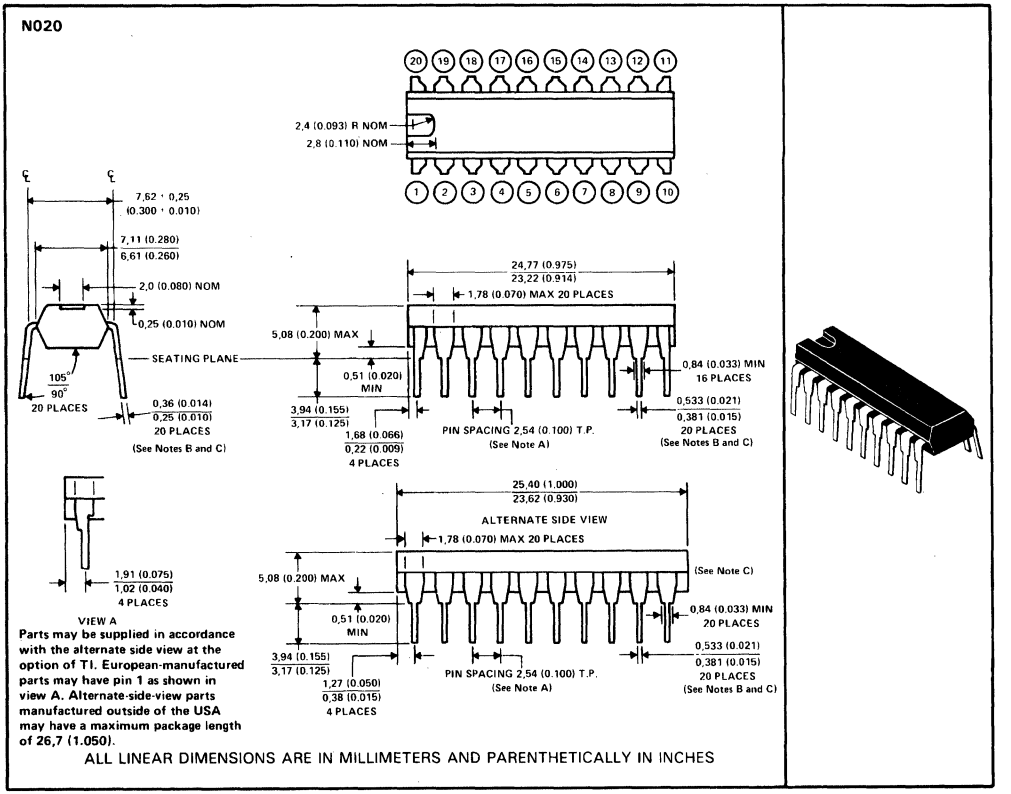
This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

N020 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

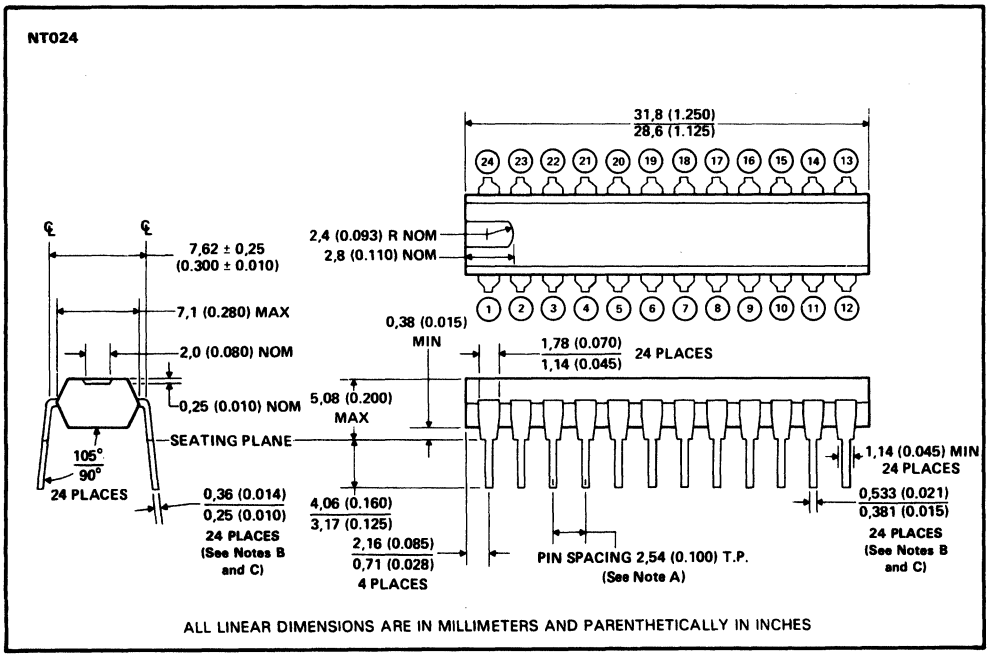


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

NT024 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

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